High efficiency reconfigurable RF power amplifiers in SOI CMOS technology for multi standard applications

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"It always seems impossible until it's done"

Nelson MANDELA

Contents

Introduction

During the last two decades, the cellular telecommunications have been expanding exponentially. This expansion has mainly been driven by the consumer needs for more diverse services. Each service addition was carried by a new standard generation. Furthermore, the obsolescence of old radio services, such as Terrestrial Analog Television, has released frequency bands that have been recently reallocated to cellular applications.

Following these trends, cellular devices are becoming more and more complex. The Front-End Module (FEM), which is the interface between the RF transceiver and the antenna, has to cope with the new standards (4G) while maintaining the compatibility with the former ones (2G, 3G). Inside the Front-End Module, the Power Amplifier (PA) is a major contributor to the performance of the FEM, but also to its complexity and energy consumption. Nowadays, a FEM can be required to address more than 10 frequency bands among all the current standards, often meaning numerous PA. Furthermore, the PA is required to be highly energy efficient.

Reducing the complexity and consumption of FEM can be done by using new PA architectures. Those architectures should handle several standards and bands using a limited number of PA with maximal efficiency in every operating mode. Reconfigurable PA seems to be promising for coping with these constraints and they are currently a major research subject.

While the traditional GaAs based technologies offer high PA performances, SOI CMOS technology offers a promising path for further integration of reconfigurable PA at reduced cost.

This thesis focuses on study and integration of a reconfigurable multi-mode multi-band power amplifier (MMPA) in SOI CMOS 130nm technology. The original solution proposed in this work represents a significant step toward the integration of high efficiency MMPA for cellular handset applications. This manuscript is divided in four chapters.

The First Chapter begins with a presentation of the context of this work. Issues associated with MMPA and performances of traditional MMPA architectures are introduced. The SOI CMOS technology used in this work for MMPA integration is also presented with a focus on the available power devices and passive elements.

In the Second Chapter, PA performances are first defined. A design methodology for saturated and linear PA integration is then proposed. Matching networks are critical for optimal PA operation. In order to realize tunable matching networks, tunable capacitors and mode switches are required. The design methodology of such devices is presented while ensuring the performance of the full architecture.

The Third Chapter focuses on the design of a new reconfigurable MMPA architecture and its integration in SOI CMOS.A focus is made on a reconfigurable power device and its implementation. Reconfigurability presents serious challenges for the design of PA the line-up and to ensure correct performance of the proposed architecture the required tradeoffs are presented. Then, implementation and measurement results of the developed SOI CMOS MMPA are presented and compared to state of the art.

The last Chapter presents a comparative study of two different high efficiency PA architectures based on supply and load modulation. The goal of this study is to determine the applications for which each technique is advantageous, both in terms of efficiency and linearity. Lastly, the design and SOI CMOS implementation of passive load modulation PA architecture is proposed. This demonstrator targets watt-level output power with high back-off efficiency improvement for cellular femto cell applications.

Chapter I: Context

I-1 Introduction

The first part of this chapter will present a brief history of cellular telecommunications from the second generation (2G) up to the current fourth generation (4G). The front-end module constraints associated with each standard will be given.

The second part will present the Front-End module with a focus on the power amplifier. Three power amplifier architectures, from the simplest Mode Specific architecture to the more advanced Converged architecture, will be presented. Afterwards, reconfigurable power amplifiers will be introduced.

The last part gives an overview of the SOI-CMOS 130 nm technology (STMicroelectronics) which has been chosen for the implementation of the designed circuits.

I-2 Cellular telecommunications evolution

Since the first deployment of cellular networks in the 80s, a lot of changes have been introduced in the cellular world. This first part will give information on the gradual transformation of mobile telecommunication standards with a focus on European Standards.

I-2.1. 2Gstandards

During the '90s, the cellular telecommunication market exploded. The users from the first generation (1G) analog standard rapidly saturated the cellular networks and the analog encoding was showing its limits in terms of data rate and security. At that time, two standards were studied: The Interim Standard 95 (IS-95, also called CDMA-One) developed by Qualcomm in the USA in the 900MHz and 1950MHz AMPS bands, and the Global System for Mobile Communications (GSM) introduced by the European Telecommunication Standardization Institute (ETSI) for the 835 MHZ and 1800MHz TACS bands.

The first breakthrough compared to the first generation was the use of more robust digital encoding compared to 1G. In the GSM standard, frequency duplex is used to differentiate between uplink and downlink transmission and Time Division Multiple Access (TDMA) is used to share each channel between 8 users. IS-95 takes advantage of Code Division Multiple Access (CDMA) to differentiate uplink and downlink communication and to share each channel between users. GSM is the most widespread 2G standard while IS-95 and its evolutions are only located in Northern America.

In the late 90's GSM was improved to General Packet Radio Service (GPRS), which allowed taking advantage of unused slots in order to improve the data rates. Later, in 2003, the Enhanced Data-rate for GSM Evolution (EDGE) was deployed. Using a new modulation scheme, its data rate is further improved.

Table 1: Characteristics of TX signals for GSM handsets.

Standard	Output Power @ antenna	Modulation
GSM (Low Band)	33dBm	GMSK (Constant Envelope)
GSM (High Band)	30dBm	

2G standards are still used nowadays for their robustness and capability to maintain communication on long ranges. However the evolution towards higher data rates has been allowed thanks to the introduction of 3G standard.

I-2.2. 3G standards

With the users starting to use their equipment in everyday life, more and more services were developed, especially media streaming and faster internet connections. In the beginning of the 21st century, Japan launched the first 3G standard: Wideband Code Division Multiple Access (W-CDMA). In the US, the evolution favored the CDMA 2000 standard, as an evolution of IS-95. The first major change with 3G was the allocation of new bands (around 2GHz). In the case of WCDMA, those bands were split in 5MHz channels and more complex Quadrature Amplitude Modulations (QAM) were introduced. By further improving controls, High Speed Packet Access (HSPA) was developed to improve data rates. Evolved HSPA (HSPA+) unlocked even higher data rates with QAM 64 and the introduction of Multiple Input Multiple Output (MIMO) systems.

Table 2: Characteristics of TX signal for 3G handsets.

Standard	Output Power @ antenna	Modulation	PAPR
W-CDMA Release'99	24dBm	HPSK (Amplitude & phase)	3.5dB
HSUPA		QAM (Amplitude & phase)	6.6dB

Today 3G is widely deployed around the world in urban areas where most of the population is concentrated. Following on its momentum, the search of even higher data-rates continued with the introduction of 4G standard.

I-2.3. 4G standards

4G marks the beginning of the Voice over IP (VoIP) in cellular communications. It should also be capable of supporting High Definition (HD) video streaming. For all these reasons, 4G must have access to very high mobile data rates. Two standards were created. First, World interoperability for Microwave Access (WiMAX) is the solution of the Institute of Electrical and Electronics Engineering (IEEE) and is a group of standards around mobile telecommunications. In Europe, the 3rd Generation Partnership Project (3GPP) developed a second solution: Long Term Evolution (LTE) standard which uses an Orthogonal Frequency Division Multiple Access (OFDMA). However, having difficulties to reach the required data rates, only LTE-Advanced (LTE-A) is considered as a 4G standard. 4G standards are characterized by a very high PAPR. The high PAPR is due to the efficient use of the spectrum to increase the data rates. Another specificity of LTE is the ability to adjust the bandwidth available per user between 1.4MHz and 20MHz according to the load on the network to further optimize the data-rate per user. Table 3 gives the equivalence between bandwidth and the number of Resource Blocks (RB) for LTE signals. Carrier aggregation technique, which has been introduced with LTE-A, is outside the scope of this work and is therefore not mentioned here.

Table 3: Bandwidth and Resource Blocks for LTE signals.

Bandwidth	1.4MHz	3MHz	5MHz	10MHz	15MHz	20MHz
Maximum Resource Blocks	6	15	25	50	75	100

Table 4: Characteristics of TX signal for 4G handsets.

Standard	Output Power @antenna	Modulation	PAPR
LTE	24dBm	QAM/QPSK	>6dB

Another major change with 4G is the increased number of frequency bands. As some obsolete wireless applications are no longer used, spectrum resource is freed. The new available bands are then redistributed among new applications such as 4Gcommunications. Figure 1shows all the Evolved Universal Terrestrial Radio Access (E-UTRA) Bands defined nowadays.

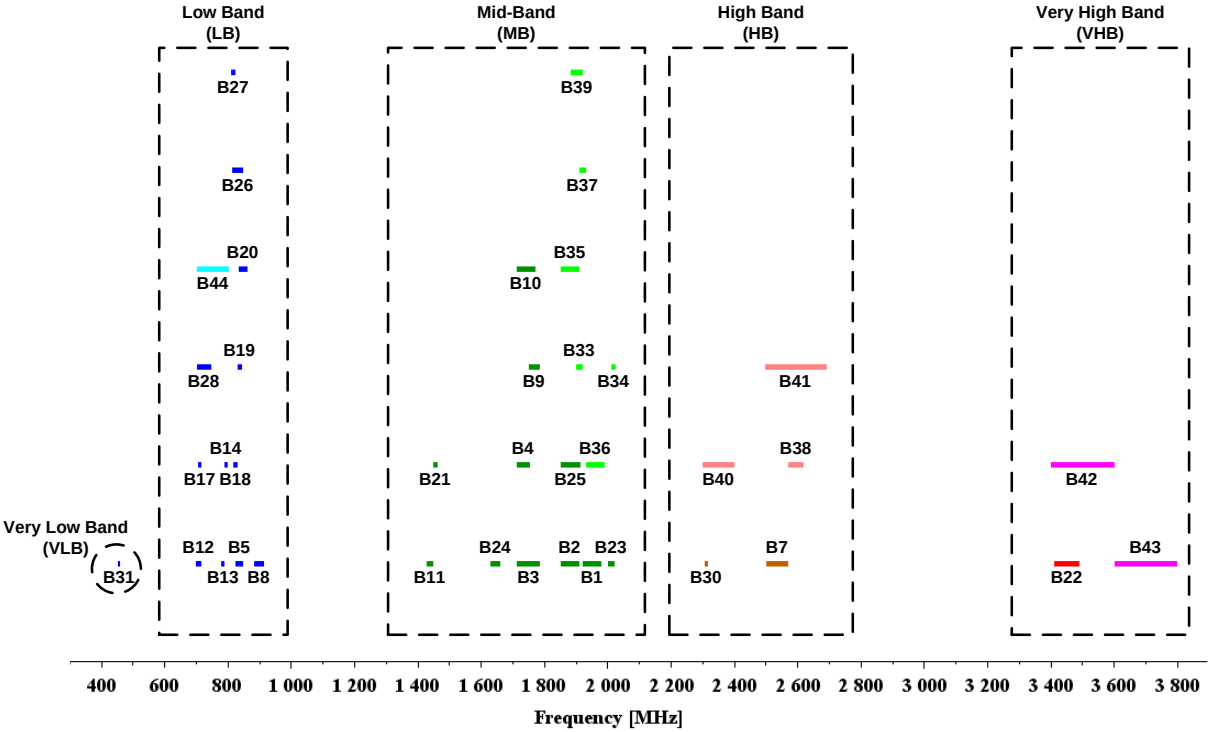


Figure 1: E-UTRA frequency bands (Uplink).

The graph shows 5 major frequency domains: Very Low Band (VLB), Low Band (LB), Mid-Band (MB), High Band (HB) and Very High Band (VHB). In total, there are 39 bands when grouping Frequency Division Duplex (FDD) bands– **B1** to **B31**– and Time Division Duplex (TDD) – **B33** to **B44**. In this thesis, the focus is made on the LB FDD bands (700-920MHz). Note that the methodologies presented further in this thesis can be transposed to higher frequency bands. Therefore, studying other bands does not add further research interest.

The user equipment has to follow the trend and the next part emphasizes on the consequences of this evolution on Front-End Module (FEM) and Power Amplifier Module (PAM) architectures.

I-3 Cellular RF Front End

I-3.1. RF Front End Module (FEM)

Nowadays, several RF blocks are required in a wireless cellular terminal. The RF transceiver is composed of all the elements required to either generate the RF signals containing the information to be transmitted, or decode the information by processing a received signal. The antenna is the frontier between the electric world and the radio waves.

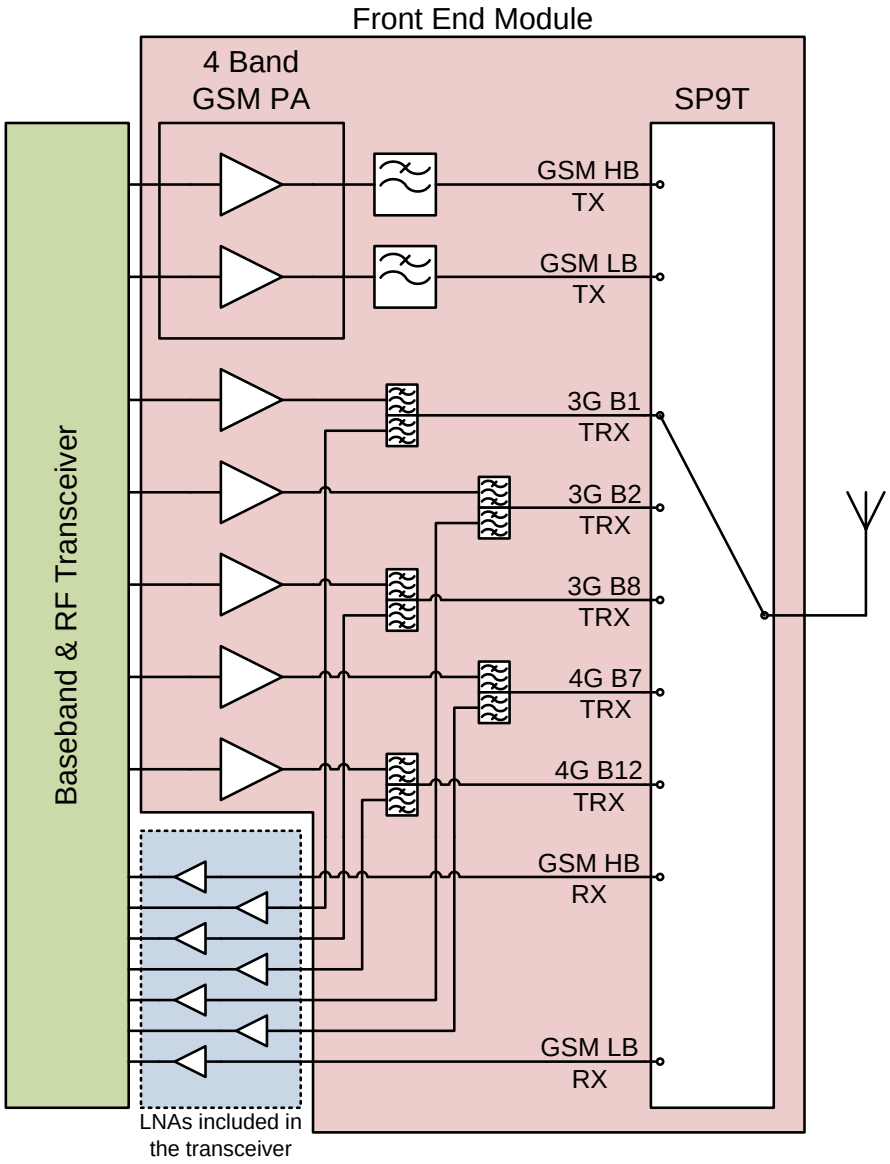


Figure 2: Multiband 2G/3G/4G FEM for FDD applications.

The RF Front-End Module (FEM), as shown in Figure 2, is the module that realizes all the operations between the transceiver and the antenna. It includes filters to select the frequencies that will be transmitted or received by the antenna, power amplifiers (PA) and RF switches. The Low Noise Amplifiers (LNAs), which are generally included in the transceiver, are used to obtain the desired sensitivity.

The RF FEM includes all the necessary circuitry to support different standard and bands. In this example, the transmit path (TX) for 2G is handled using a quad-band GSM PA associated with a High Band (HB) and Low Band (LB) low pass filters to limit the harmonics level. The receive path (RX) for 2G includes two Low Noise Amplifiers (LNA), one for the HB path and another one for the LB path. For 3G and 4G, the uplink and downlink communications are done simultaneously using Frequency Domain Duplex (FDD). Duplexer filters are used to separate TX and RX signals. Having more standards and bands to support means more RF circuits and brings new design challenges for the RF FEM. In this thesis, we will focus on the power amplifiers.

I-3.2. RF Power Amplifier Module (PAM)

PA modules are essential in radio links since the transmit RF signal needs to be amplified at a high enough level to ensure quality of the transmission. Traditionally, PA modules (PAM) were optimized for a dedicated operation. However, with the growing number of standards, this strategy is reaching its limits in terms of cost and complexity [Walsh09]. In the following paragraphs, the evolution of multimode multiband PAM architectures will be discussed.

A. PAM architectures

a. Mode Specific PA architecture

Historically, when a new band or standard was required, the manufacturers simply added a discrete "mode specific" PA line-up in the RF FEM, as shown in Figure 2. The advantage of such approach is to have the best performance for each mode/standard while paying for exactly what is required.

Table 5: Performance of commercial "Mode Specific" Power Amplifiers.

Reference	Standard	Output Power	Power Added Efficiency
[SKY77351-13]	**2G** (GSM)	35.5dBm	55%
[SKY77187]	**3G** (HSPA)	29dBm	40%
[SKY77709]	**4G** (LTE)	28dBm	36%

With the current evolution trend, this solution tends to be abandoned in favor of converged architectures which are more cost effective.

b. Converged PA architecture

In a converged PA architecture, the goal is to minimize the number of PA line-up while addressing multiple standard and frequency bands [Cheng11]. The block diagram of a converged PA architecture is shown in Figure 3.

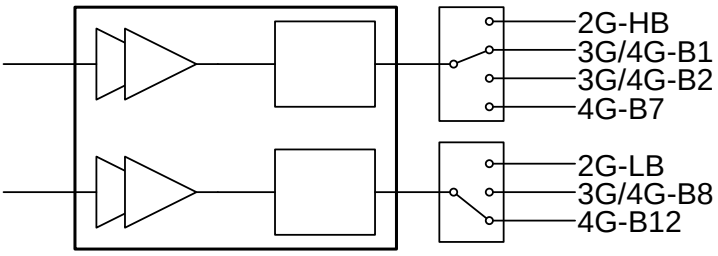


Figure 3: Converged PA Architecture.

Both PA line-ups must be able to reconfigure their operating mode according to the considered standard and frequency band. Tuning degrades to the performance of line-ups. Examples of performance for this type of PA are given in Table 6.

Table 6: Performances of converged 2G/3G PA with support of bands 5 and 8 [Kang13].

Mode	Pout	PAE	ACPR
2G (GSM)	34.5dBm	> 53%	-
2.5G (EDGE)	29.0dBm	> 27%	-58dBc
3G (WCDMA)	28.2dBm	> 41%	-39dBc

To implement such architecture, either wideband or reconfigurable PA is required. Wideband power amplifiers have the advantage to minimize the complexity but have degraded performance due to the required broadband matching networks. On the other hand, reconfigurable PA (RPA) offer better performance in every band at the cost of a higher complexity since tunable components are needed.

B. Reconfigurable PA

a. Reconfigurable multi-mode PA

As discussed in previously, the different cellular standards have different types of requirements. GSM standard requires high output power with low linearity constraints. Therefore, highly efficient saturated PAs operating near saturation can be used. Others standards, such as LTE, require lower power with high PAPR and linearity constraints. For this last application, linear PAs operating in linear mode are required.

PA with different operating modes (saturated or linear) is called multimode PA. Such PA can be realized by adjusting the bias, as shown in Figure 4[Kang08].

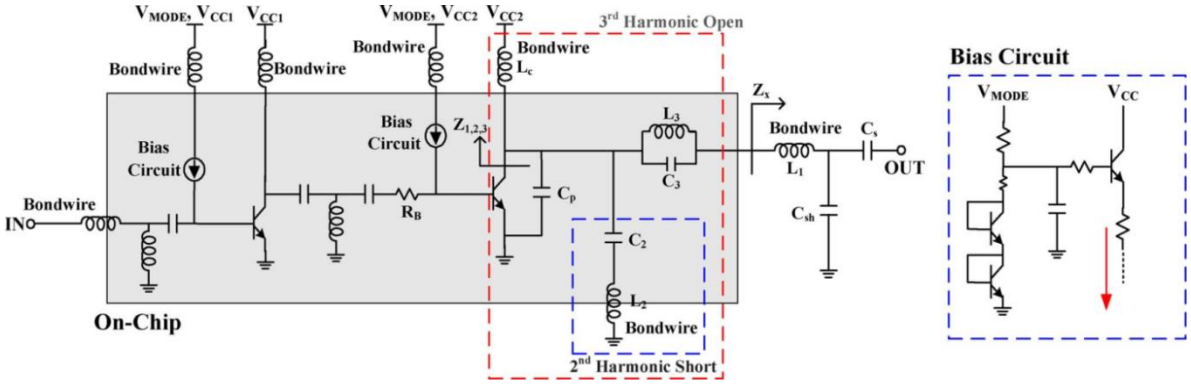


Figure 4: Multimode PA with saturated and linear operating modes [Kang08].

In this architecture, the bias current of the driver and output stages are adjusted according to V_{MODE} to operate in either linear or saturated mode. When operating for 2G signals (GSM), the bias is adjusted in both stages to maximize their efficiency and output powers. If the PA is required to operate linearly, for 2.5G (IS-95 CDMA) for instance, the two stages are biased for higher linearity at the expense of efficiency.

Improved multimode architectures make use of reconfigurable matching to adjust the load of the power stage and transistor sizing to achieve optimized performance for both operations [Kang13]. The schematic of such reconfigurable multimode PA architecture is depicted in Figure 5.In GSM mode, for which high power and efficiency are required, both Q3 and Q4 transistors participate to signal amplification and the Output Matching Network (OMN) is configured for Path-2 while Path-1 is in a high impedance mode. For 3G operation (UMTS), Q4 is switched-off and Q3 is the only active transistor of the output stage. The OMN is switched to Path-1 with Path-2 set to high impedance mode. In this configuration, the output stage is loaded by the optimal impedance for linear operation.

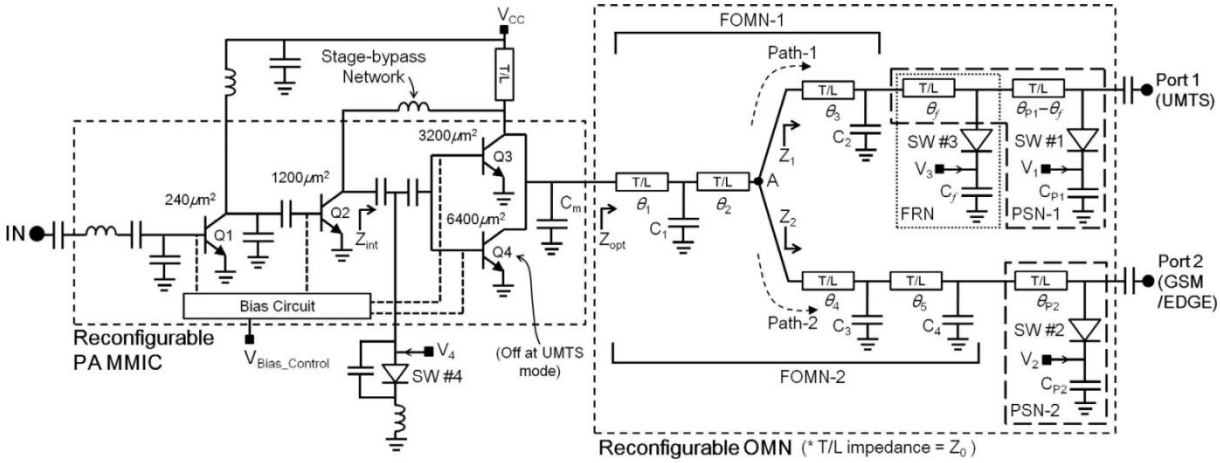


Figure 5: Reconfigurable multimode PA with transistor sizing and reconfigurable matching network [Kang13].

A summary of the performance of the two architectures is given in Table 7.

Table 7: State-of-the-art of reconfigurable multimode PA [Kang08] [Kang13].

Work	Operating Frequency	GSM Output Power	GSM Efficiency	Linear Standard	Linear Output Power	Linear Efficiency	Technology
[Kang08]	1880MHz	32.5dBm	64.7%	IS-95A CDMA	28dBm	39%	InGaP/GaAs 2 µm HBT
[Kang13]	900MHz 850MHz	34.5dBm	53.55%	Release'99 W-CDMA	28.2dBm	41%	InGaP/GaAs 2 µm HBT / PIN diode

Both PAs are adjusted for operating mode and power level in accordance with the targeted standard. In linear mode, both PA architectures meet a good tradeoff between linearity and efficiency.

b. Reconfigurable multi-band PA

As mentioned in section I-3.2.A.b, the trend for PA is to support several frequency bands with the same circuitry. The use of tunable matching networks allows such multiband PA solutions [Aref12] [Kang13].

In Figure 5, Path-1 for UMTS (3G) includes a frequency reconfigurable network (FRN) which allow PA performances optimization for 900MHz (SW #3 open) or 850MHz (SW #3 closed)..

In Figure 6 [Aref12] another multiband PA architecture using several reconfigurable matching elements is proposed. According to the number of shunt capacitors activated in the Tunable load Transformation network, this multiband PA architecture can be tuned from 1.6 GHz to 2.6 GHz, with optimal operation from 1.7 GHz to 2.1 GHz.

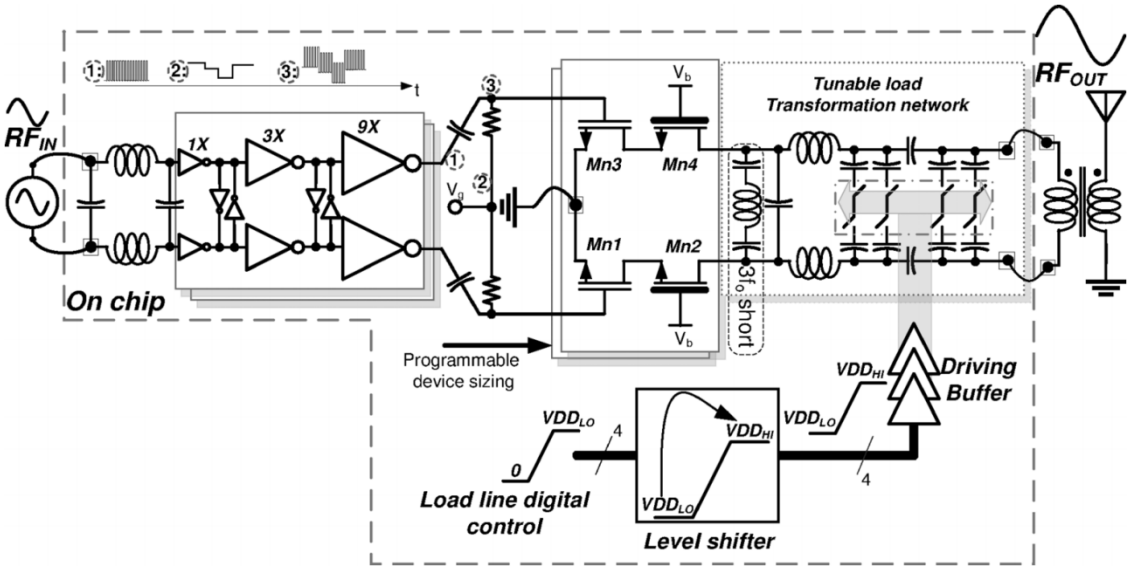


Figure 6: Simplified schematic of a multiband saturated PA [Aref12].

c. Reconfigurable PA with multiple power levels

1. Back-off efficiency

One of the major challenges of the 21st century for cellular application is the enhancement of PA efficiency. For cellular networks it is required to produce components compliant with environmental norms and consuming power only when required. In handset application, talk-time and battery life time are directly affected by PA power consumption, PA being one of the most power consuming block of the FEM. Therefore the PA must operate with the highest possible efficiency. Traditional PA architectures are optimized to be the most efficient at maximum power (P_{max}). Figure 7 shows the Power Added Efficiency (PAE) of a traditional PA as a function of output power (Pout).

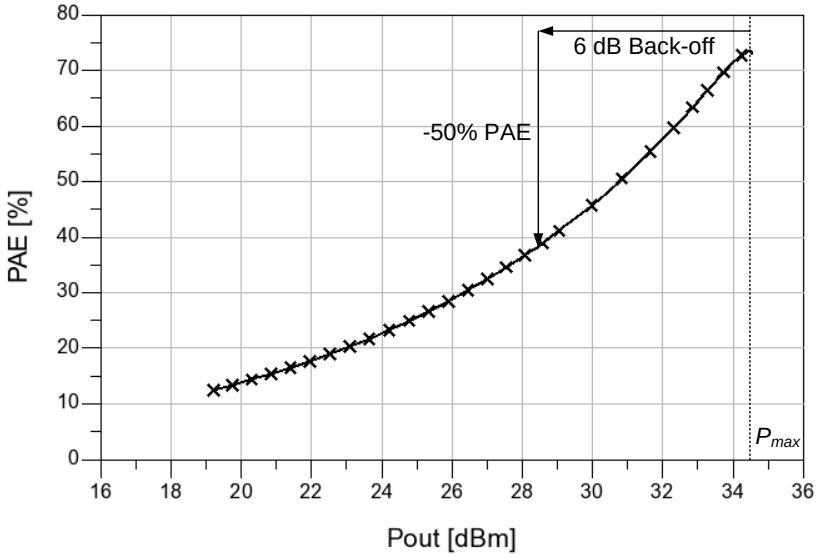


Figure 7: PAE vs. Output Power (Pout) for a traditional PA architecture.

In this graph we can notice that efficiency drops for low output power levels. In this example, if the required power is four times lower (6dB power back-off) than P_{max}, PAE is reduced by a factor of two.

For constant envelope signals, PA linearity is not a concern and the PA line-up can be reconfigured in static manner to optimize its efficiency at each back-off power. PA efficiency can be optimized for different power levels while using multi-state architecture as shown in Figure 8.

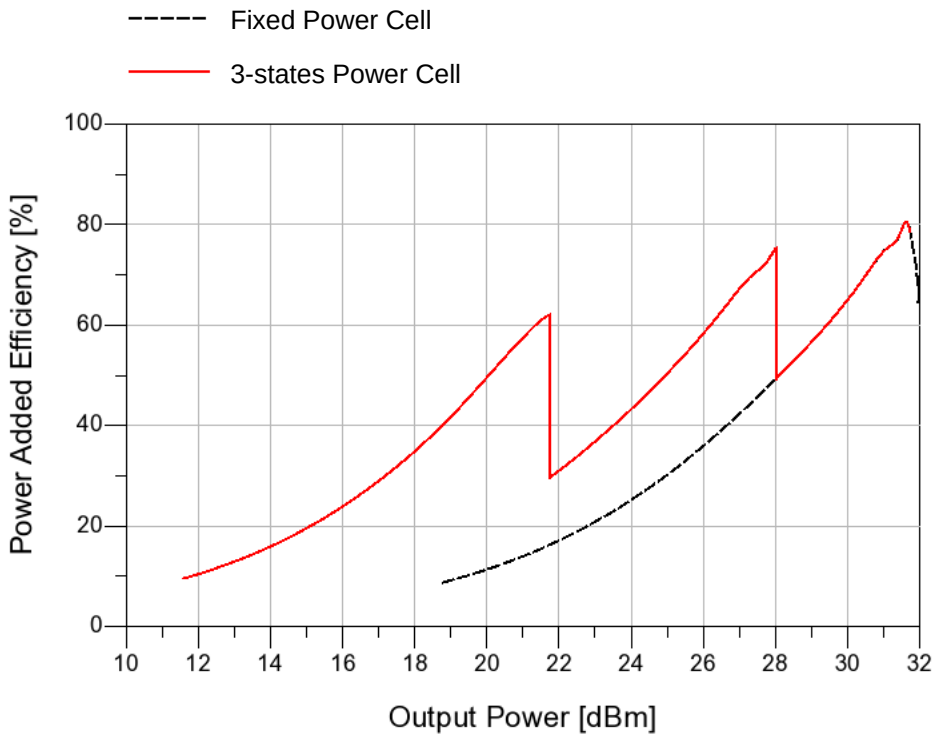


Figure 8:PAE evolution vs. Output Power in a multi-power mode PA

Generally, the use of 3 states is sufficient for a correct improvement of efficiency. The added circuitry is simple and easy to drive. The static reconfiguration of PA efficiency is commonly done with transistor re-sizing and stage bypass architectures.

2. *Power transistor re-sizing*

One type of PA architecture takes advantage from the bias strategy of segmented power devices. For a given power level, only the minimum number of power cell is biased [Kim04] [Kim11a]. The unused power cells are switched off to improve the overall efficiency of the PA. The block schematic of a PA architecture with power transistor re-sizing using 2 output cells is presented in Figure 9.

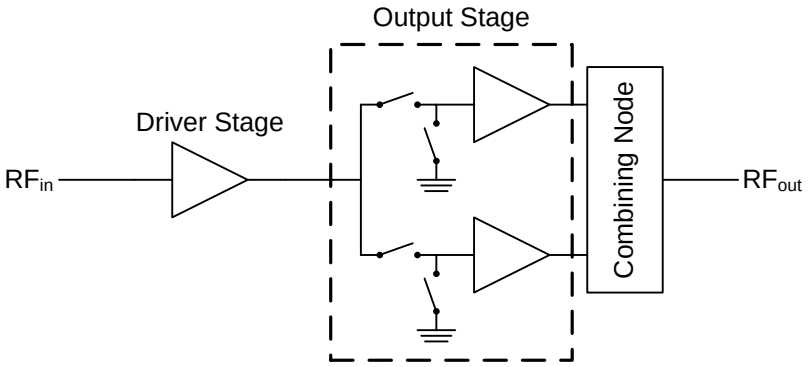


Figure 9: PA architecture with power transistor re-sizing.

In this example, when the PA is required to deliver the maximum output power, both cells are used. If half of the power is required, one cell is switched off by switching its input to ground. A drawback of this architecture is that the output impedance of the switched cell can disturb the active cell. Therefore, the combining node must be carefully designed. Table 8 gives some state-of-the-art performances for such architecture.

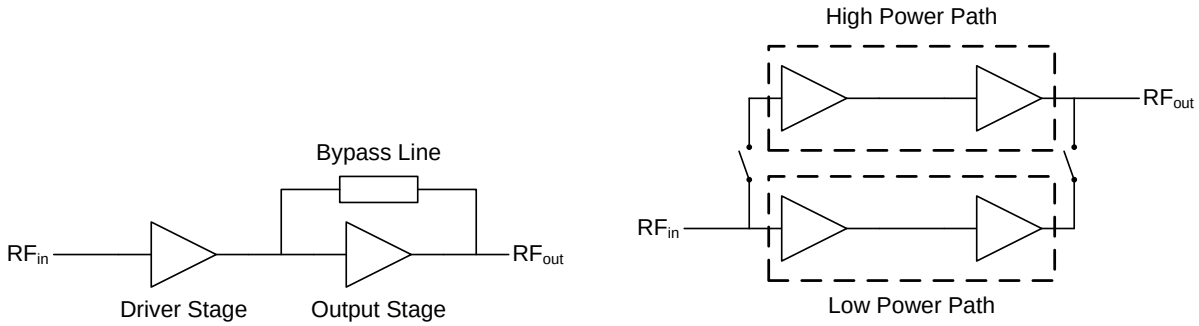
Table 8: State-of-the-art PA architecture with power transistor re-sizing.

Work	Maximum Output Power (P_{max})	Efficiency at P_{max}	Back-off power (P_{BO})	Efficiency at P_{BO}	Efficiency Improvement *	Technology
[Kim04]	27dBm	36%	16dBm	15%	+83%	InGaP/GaAs HBT
[Kim11a]	31dBm	34.8%	20dBm	14%	+43%	0.18 µm CMOS

* Comparing the back-off efficiency of architecture with and without transistor re-sizing

3. *Stage bypass*

Instead of segmenting the active device and switching off unused power cells, it is possible to implement several line-ups in the same PA architecture. Each line-up is optimized for a given power range. By switching between these line-ups, or bypassing them, the PA can have optimal efficiency at different power levels. Examples of PA architectures using stage-bypass are shown in figure 10.



Bypass Line Architecture

Switched Paths Architecture

Figure 10: PA stage bypass using line (left) or switch (right).

In the first example (left), the output stage is switched off for low power operation and the bypass line transfers the signal directly from the driver stage to the PA output [Kang13]. In this type of architecture, special care must be taken when designing the bypass line to minimize its influence in high power mode. In high power mode, the impedance of the bypass line is several times higher than the load impedance of the output stage and the input impedance of the output stage is lower than the input impedance of the bypass line. In low power mode, when the output stage is deactivated, the input and output impedance of this stage become higher than that of the bypass line.

In the second example (right), two PA line-ups are present and have been optimized independently for either high power of low power operation [Jun13]. The switches are used to select one path or the other according to the required power, the unused path being biased off. In this case, the switches are sized to have minimal loss in both modes. Switches can be used to bypass stages, line-ups or even both [Hau10]. Table 9 gives a state-of-the-art of different stage-bypass PA architectures.

Table 9: State-of-the-art of Stage-bypass PA architectures.

Work	High output power (Phigh)	Efficiency at Phigh	Low output power (Plow)	Efficiency at Plow	Total Efficiency Improvement *	Technology
[Hau10]	28.5bdBm	42%	17dBm	22%	+175%	InGaP/GaAs HBT + pHEMT switches
[Jun13]	26dBm	28%	16dBm	16%	+86%	0.35 µm SiGe BiCMOS
[Kang13]	28.2dBm	41%	16dBm	17.4%	+117%	InGaP/GaAs 2 µm HBT + PIN diode

* Comparing the back-off efficiency of architecture with and without stage bypassing

Transistor re-sizing and stage bypass architectures offer good improvement but are limited when used to amplify varying envelope signals. With such signals, the PA suffers from efficiency degradations as shown in Figure 11 since the average power (P_{avg}) of the modulated signal is lower than the peak power (P_{peak}) where efficiency is maximized.

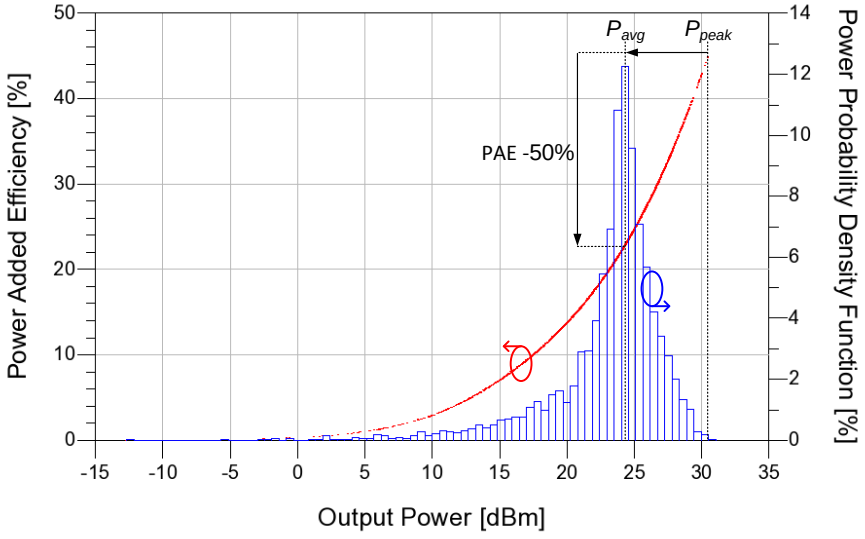


Figure 11:PAE evolution vs. Output Power in a traditional Power Amplifier

As can be seen, the PA operates most of the time at back-off power. In this graph, the efficiency at P_{avg} is decreased by 50% compared to the maximal efficiency. The following equation gives the expression to calculate the average efficiency when amplifying a modulated signal [Popovic14].

$$\langle PAE \rangle = \frac{\int PDF(P_{out}) \cdot PAE(P_{out}) dP_{out}}{\int PDF(P_{out}) dP_{out}} \qquad \text{Equation 1}$$

Using this equation, it is possible to see that average efficiency of the PA optimized at the maximum output power will be degraded when amplifying a signal using a complex modulation. To improve the efficiency of the PA, it becomes necessary to improve the instantaneous efficiency by providing dynamic reconfiguration of PA characteristics.

d. High efficiency PA architectures

PA architectures based on supply or load impedance modulation allow dynamic efficiency enhancement.

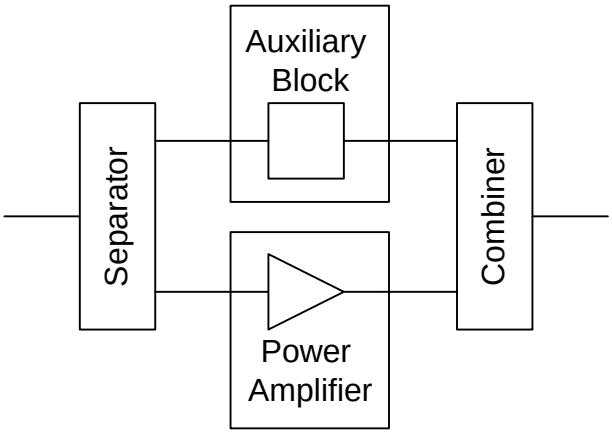


Figure 12: Block schematic of high efficiency PA architecture [ref]

Such PA architecture can be represented by the block diagram shown in Figure 12 and inspired by [Popovic14]. The power amplifier is the main cell of the architecture. The auxiliary block allows control of PA supply or load impedance. The separation block divides the input signal in two parts. The first one is the signal to be amplified by the power amplifier. The second part is the information used by the auxiliary block to realize control. The actuation takes place in the combination block. The actuation signal optimizes the operation of the power amplifier to achieve high efficiency.

1. Supply modulation

i. Envelope Tracking

The envelope tracking power amplifier (ETPA) takes advantage of an Envelope Amplifier to modify the supply voltage of a linear PA according to the envelope level[Yan11][Kim11b]. The simplified schematic of an ETPA is shown in Figure 13.

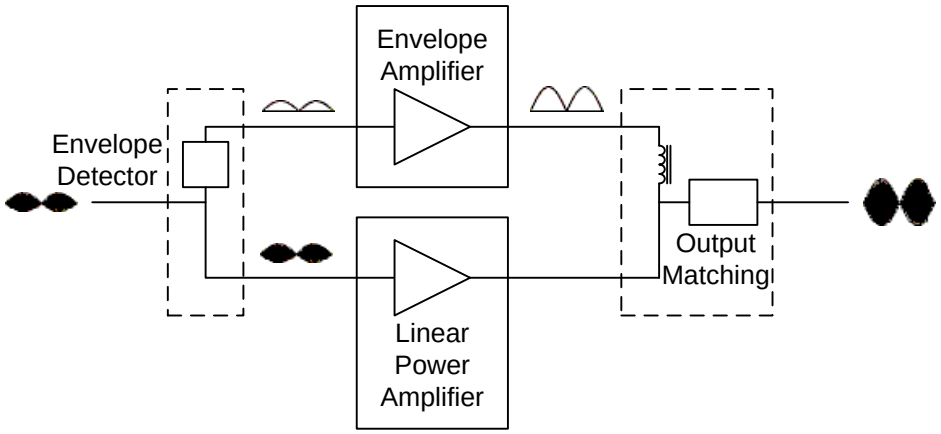


Figure 13: Block schematic of Envelope Tracking Power Amplifiers

The Envelope Detector is used to extract the envelope of the input RF signal. While the power amplifier amplifies the RF signal, the envelope amplifier shapes the supply signal V_{DD} to optimize PA efficiency as a function of envelope level. The relation between the varying envelope RF signal and varying supply signal is called envelope shaping. Different shaping strategies can be adopted to optimize PA performances. The recombination consists in applying the shaped supply voltage to the power amplifier supply input. The output signal of the ETPA is therefore an amplified version of the input signal with an optimized DC consumption.

The synchronization of the variable supply voltage and RF signal should be ensured to limit non-linearity. Efficiency of the envelope amplifier is critical since efficiency of the ETPA is given by Equation 2.

$$\eta_{ETPA} = \eta_{PA} * \eta_{DC/DC} \qquad \text{Equation 2}$$

From this equation, it can be seen that low efficiency of the envelope amplifier can lead to lower overall efficiency than the PA in a stand-alone configuration.

ii. Envelope Elimination and Restoration

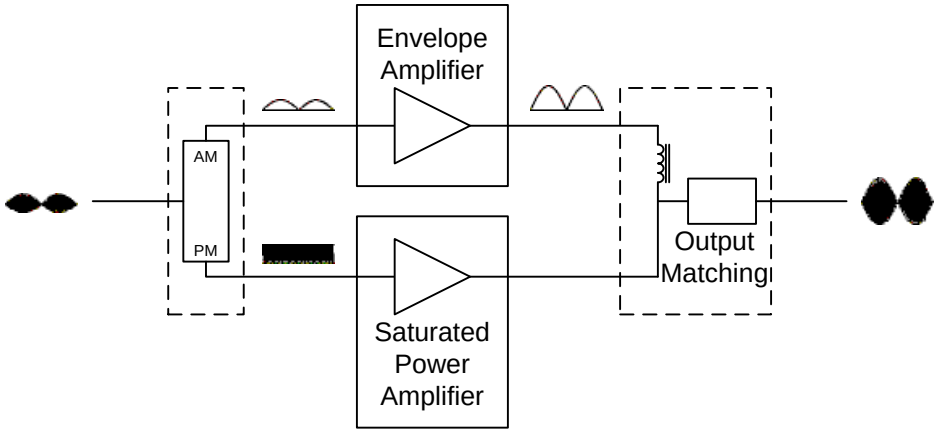


Figure 14: General schematic of the Envelope Elimination and Restoration Power Amplifier

The block schematic of an Envelope Elimination and Restoration (EER) PA is shown in Figure 14. This architecture is very similar to the envelope tracking. There is however significant differences in its operation. The EER PA uses a total separation of the Amplitude Modulation (AM) and Phase Modulation (PM) of the complex signal [Pinon08] [Kim10]. The AM signal is sent to the envelope amplifier to generate the supply signal of a saturated PA. The DC/DC converter in the case of EER has more precision constraint than ETPA as the shaped supply is used to restore the AM component of the modulation to the output signal.

The PM signal is amplified by the PA. As this signal has a constant envelope, the PA can be designed for a highly efficient switching class. The full modulation is restored thanks to the supply voltage of the PA which will be the image of the signal Envelope. Synchronization between the shaped supply and the amplified PM signals is crucial. The least synchronization issue can lead to high distortion of the output signal. Also, the efficiency of the envelope amplifier cannot be neglected in the overall efficiency of an EER PA, as it was the case for the ETPA.

2. *Load Modulation*

i. *Doherty Power Amplifiers*

The Doherty Amplifier uses an "active load-pulling" mechanism. The block schematic of the architecture is shown in Figure 15. Two power cells are required in Doherty Amplifiers [Kitahara11] [YuTing14]. The main amplifier is designed for Class-AB operation. The peaking amplifier is biased for a more efficient Class-C operation.

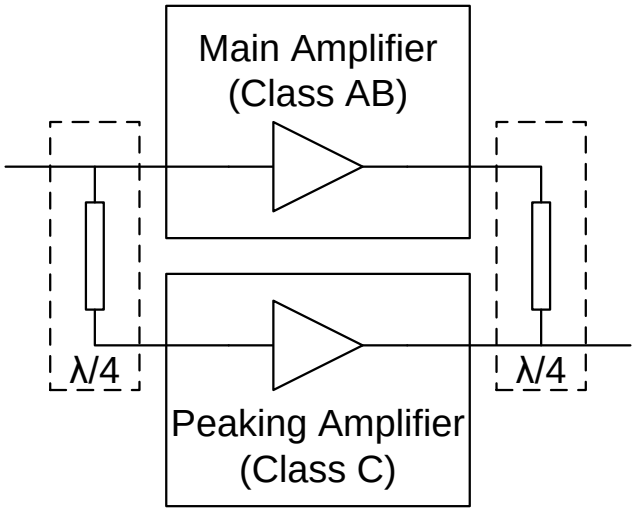


Figure 15: Block schematic of Doherty Amplifiers

Between low to medium power levels, the peaking amplifier is off while the Class-AB main amplifier is operating alone. Once the main amplifier reaches it saturation output level, the peaking Class-C amplifier turns on. As it occurs, more current is flowed into the load and, and then the load viewed by the main amplifier through the quarter-wave transformer decreases. As the load viewed by the main amplifier is decreased, the current delivered by this amplifier increases while the voltage is maintained to its maximum value. Doing so increases the dynamic of the main amplifier towards high power.

Doherty Amplifiers requiring two amplifier stages, the surface area can be significant. Moreover, the need for quarter-wave transformers does not facilitate the integration of such architecture.

ii. Passive Load Modulation

The passive load modulation is the passive equivalent of the Doherty Amplifier. The general schematic of such architecture is given in Figure 16.

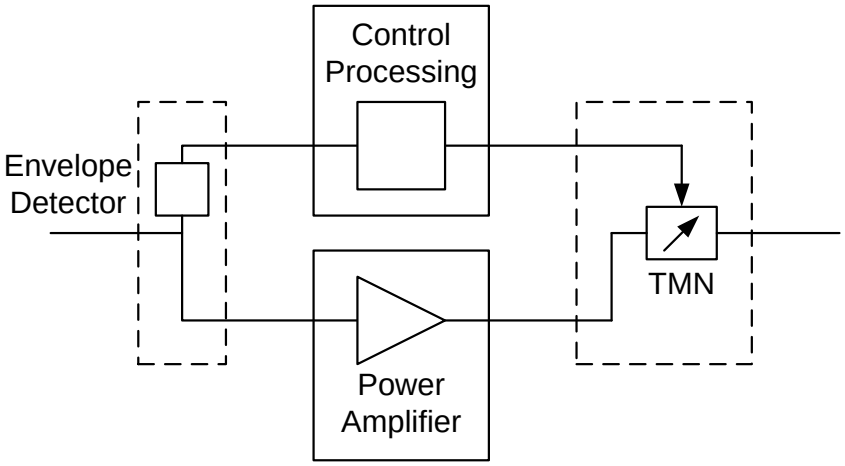


Figure 16: Passive Load Modulation Power Amplifier block schematic

This architecture relies on a Tunable Matching Network (TMN) to modify the load impedance viewed by the PA [Yue12] [Andersson12]. The TMN is actuated by a control signal generated from the envelope information. This can either be done by detecting the envelope of the RF signal or by directly using the baseband information.

$$\eta_{tot} = \eta_{PA+CTRL} \cdot IL_{TMN} = \frac{P_{out}}{P_{DC_{PA}} + P_{DC_{CTRL}}} \cdot IL_{TMN} \qquad \text{Equation 3}$$

The drawback of this technique is the increased loss in the TMN compared to a fixed network. A rough estimation of the loss impact is given in Equation 3. In this formula, the efficiency of the power amplifier should include the consumption of the control processing block $P_{DC\,CTRL}$. Moreover, the loss of the TMN (IL_{TMN}) should not be too high in order to not decrease the overall efficiency. Furthermore, bad synchronization between the TMN actuation and RF signal can lead to distortion in the RF signal.

3. Impact on linearity

All the architecture presented above can distort the signal. In that case, a linearization technique can be added in order to meet the linearity requirement of the considered standard. The consumption of the linearization circuit impacts the efficiency of the full architecture. In the case of handset PA, the consumption of the linearization circuit mitigates the efficiency enhancement [Cripps06].

Table 10presents a state-of-the-art of high efficiency PA architectures using supply and load modulation, for both handset and base station applications.

Table 10: High efficiency PA architecture with supply/load modulation.

Work	Architecture	Application	Max. Output Power (P_{max})	Efficiency at P_{max}	Back-off	Efficiency at Back-off
[Kitahara11]	Doherty	Base Stations	55dBm	50%	8dB	48%
[YuTing14]			54.7dBm	56%	6dB	48%
[Yue12]	Load Modulation		40.4dBm	60%	7.5dB	60%
[Andersson12]			38dBm	60%	8dB	45%
[Yan11]	Envelope Tracking		41dBm	63%	11dB	57%
[Kim11b]		Handset	33dBm	66%	10dB	62%
[Pinon08]	Envelope Elimination & Restoration		28dBm	61%	8dB	48%
[Kim10]			27dBm	59%	7dB	54%

As can be seen in the table, PA efficiency can be highly improved using those architectures.

Reconfigurable power architectures improve power amplifier and either the supported modes, bands or power level. By using new technologies for implementing reconfigurable power amplifiers, better integration and cost reduction can be achieved, as shown in the next section.

I-4 SOI CMOS technology overview

Today, the main technology used in PA design for handset applications is GaAs HBT since it offers the best PA performance in terms of output power, gain, efficiency and linearity. However its main drawback is a lower yield and a higher cost compared to Very Large Scale Integration (VLSI) Silicon technologies. Furthermore, the co-integration of digital control circuitry is not realistic in GaAs. Table 11 summarizes the advantages and drawbacks of different PA integration technologies.

Table 11: Technology Comparison.

Technology	Cost	Passive Quality Factor	RF Power Device Performance	Digital Performance
CMOS	++	- -	-	+
BiCMOS	+	- -	+	+
SOI CMOS	+	-	+	++
GaAs HBT	- -	-	++	-
Module	++	++	N/A	N/A

Today, most PAM and FEM are designed using several technologies as shown in Figure 17.

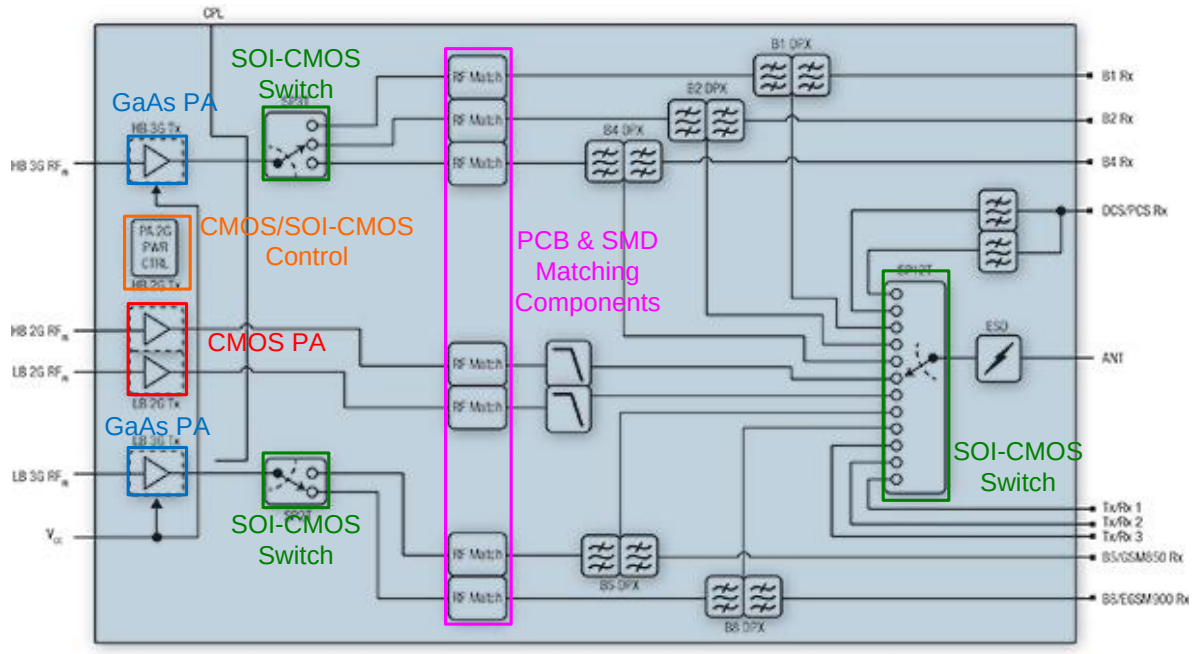


Figure 17: Used technologies in high performance FEM [ASN13].

In this module, there are 2 GaAs PAs for linear operation and a quad-band CMOS PA for GSM. The control part is implemented either in a Silicon on Insulator (SOI) or Bulk CMOS technology, as cost effective technologies for digital integration. Matching networks use Surface Mounted Device (SMD) capacitors and distributed lines on the laminate substrate of the module. Duplex filters (DPX) are implemented using Surface Acoustic Wave (SAW) or Bulk Acoustic Wave (BAW) technologies. Acoustic Wave technologies are currently the most effective solutions to realize low insertion loss and high TX/RX isolation with sharp band edges.

The combination of all these different technologies implies added assembly costs for the manufacturers. In order to reduce this assembly costs, the use of a single technology with competitive performances and lower cost compared to GaAs and high integration capabilities appears necessary. Recent progresses in SOI CMOS technologies make this technology a good candidate for PA/FEM integration [Andia10].

I-4.1. RF devices

A. RF switch

SOI NMOS devices allow implementation of low loss and high isolation RF power switches [Carrara09]. Switch performances are related to the on-state resistance (R_{on}) and off-state capacitance (C_{off}) of NMOS devices. In this work, a SOI CMOS 130nm process with six metal layers has been used. This industrial SOI CMOS process from STMicroelectronics presents a Ron.Coff product of **310fs** with on-state resistance of **1Ω.mm**.

B. LDMOS transistor

The Laterally Diffused MOS (LDMOS) transistor allows high voltage operation with high robustness thanks to the drain extension [Reynier09] and is becoming more and more prominent in the field of RF power applications. In the selected SOI CMOS technology, the LDMOS transistor is characterized by a transition frequency (Ft) of **36GHz** and a breakdown voltage (BVds) of

13V[ST15].A cross-section view of this device is shown in Figure 18.With this power device, high efficiency PA has been demonstrated [Giry13].

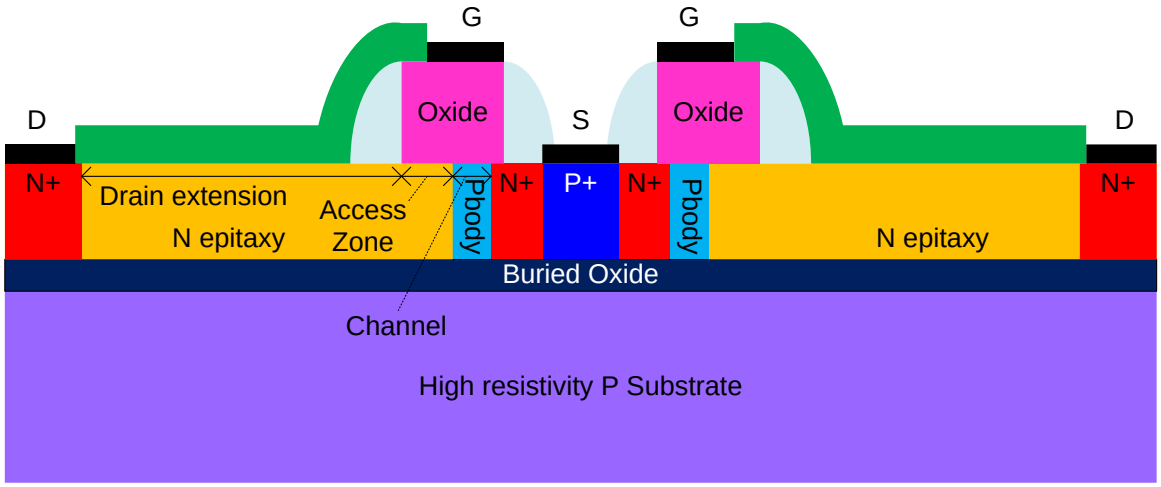


Figure 18: Cross-section of a LDMOS transistor.

C. *Inductors*

In cellular PA applications, wavelength is too high (few centimeters) to obtain high inductance values using transmission lines. Planar inductors with high quality factor (Q) can be obtained in SOI CMOS technology thanks to the high resistivity substrate [Andia10]. Planar inductors can be realized with two distinct approaches, as shown in Figure 19.

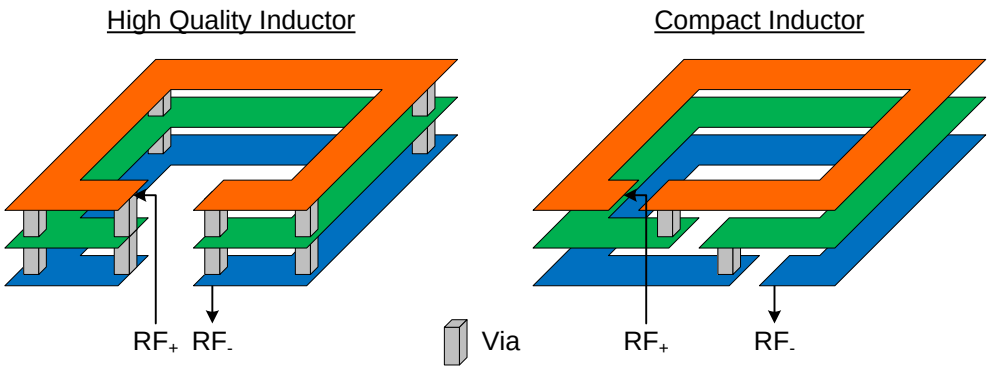


Figure 19: Simplified structure of a high Q inductor (left) and compact inductor (right) implemented with 3 metal layers and 1 turn per metal level.

The high Q implementation (left in Figure 19) uses metal stack to achieve low ohmic loss. Combined with wide lines, such inductors can achieve high quality factors (>**10**). However, they tend to be area consuming and are generally limited to low inductance values (<**2nH**).

The compact implementation (right in Figure 19) takes advantage of the multiple metal layers available in the technology. By realizing one elementary coil per layer and then connecting the layers in series, it is possible to implement high inductance values (>**5nH**). The drawback of this implementation is the high series resistance, leading to limited quality factors (<**5**). These inductors are generally used for RF/analog blocks where insertion loss is not critical.

D. Capacitors

In this work, Metal-Insulator-Metal (MIM) and Metal-Oxide-Metal (MOM) capacitors have been used.

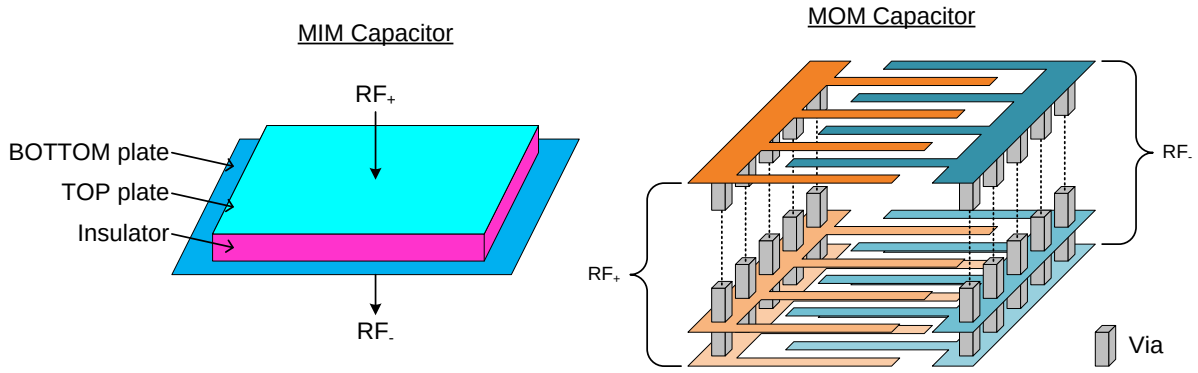


Figure 20: MIM capacitor (left) and interdigitated MOM capacitor (right).

MIM capacitor (left in Figure 20), is a vertical structure. It uses a high dielectric constant insulator material between a metal top plane and a metal bottom plane to realize compact high capacitance values. The drawback of this structure is the low break-down voltage (<**10V**). These capacitors can be used for analog blocks or low voltage RF path.

Interdigitated MOM capacitor (right in Figure 20) is a horizontal structure composed of interdigitated metal fingers. This structure is less compact than MIM capacitor, due to the lower dielectric constant of the oxide, but offers very high breakdown voltages (>**50V**). For high power RF paths, the MOM capacitor is preferable to MIM capacitor thanks to its inherent higher breakdown voltage.

I-4.2. Through Silicon Via

Through Silicon Via (TSV) can be realized after post-processing of SOI CMOS wafers as shown in Figure 21.

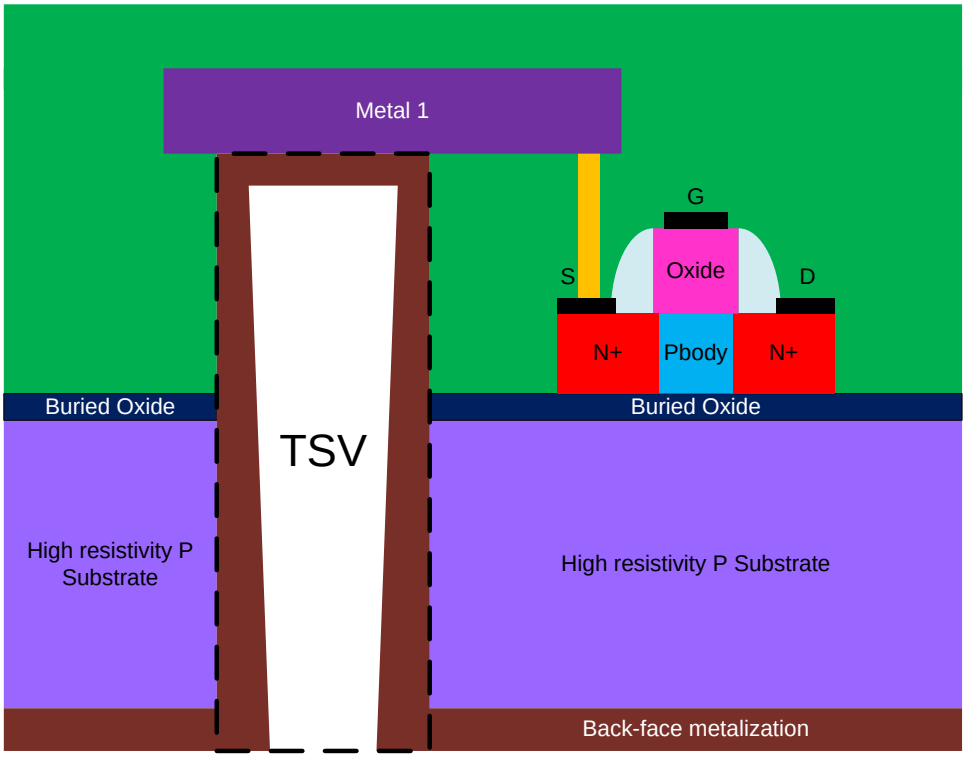


Figure 21: Simplified Cross-section view of a TSV connected to the source of a MOS transistor.

Power amplifiers suffer from parasitic inductor to ground which lead to performance degradation. Thanks to TSV inductance to ground can be drastically reduced. Another beneficial effect of TSV is the mitigation of thermal issues. The high performance of SOI is obtained thanks to the buried oxide which isolates active devices from the silicon substrate. This is however done at the cost of thermal dissipation, which leads to increased temperature and can degrade the time to failure of active devices. TSV copper metallization offer a low thermal path to the backside of the chip.

I-5 Conclusion

Multiple cellular standards and frequency bands have emerged over the past 3 decades and today Front End Modules and Power Amplifier Modules face increasing challenging requirements. Current PA architectures are limited and reconfigurable PA appears as a good candidate to address multimode multiband requirements with reduced size and cost. Therefore, design and implementation of a reconfigurable MMPA in SOI CMOS technology is proposed in the following part.

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Chapter II: Power Amplifier Design

1 Introduction

The previous chapter presented the context of this work as well as a state of the art of reconfigurable RF power amplifiers (PA). The design of reconfigurable PA requires first a basic knowledge of classic power amplifier design.

The following chapter first presents definitions and main characteristics commonly used in power amplifier design. The parameters presented in this part are used throughout the proposed research work and main buildings blocks for power amplifier design are presented.

An analytical analysis of different PA operating classes is then carried on in order to find trade-offs for the design of active stages. Two different cases are considered since saturated and linear PA designs need different optimizations regarding their respective specifications. Saturated PA are used for constant envelope signals, such as GSM. The main focus of the design is therefore the maximization of the efficiency. Linear PA are used for complex modulated signals with varying envelope and phase, such as 3G or 4G signals. This type of signal requires specific linearity performance which depends onto the considered standard. These linearity constraints can be used with proposed method in order to find the best trade-off.

The matching networks are used to present optimal source and load impedances to the active stage, thus ensuring their proper operation. Matching networks in this work are split in unit L-Cells. The number and size of these unit elements can be determined by using bandwidth and insertion loss requirements.

Matching networks can be made reconfigurable using tunable components such as switched capacitors. Therefore, the design of switched capacitor banks taking into account that those components must operate under high power levels is also presented.

Finally, the design of a single pole multiple throw RF switch is introduced in section II-5 since it represents a critical building block of multiband PA design.

II-1 Power amplifier characteristics

PA designers have to find optimal trade-off between gain, output power, linearity and efficiency. The Simulated response of linear PA optimized for 3G applications is shown in Figure 22.

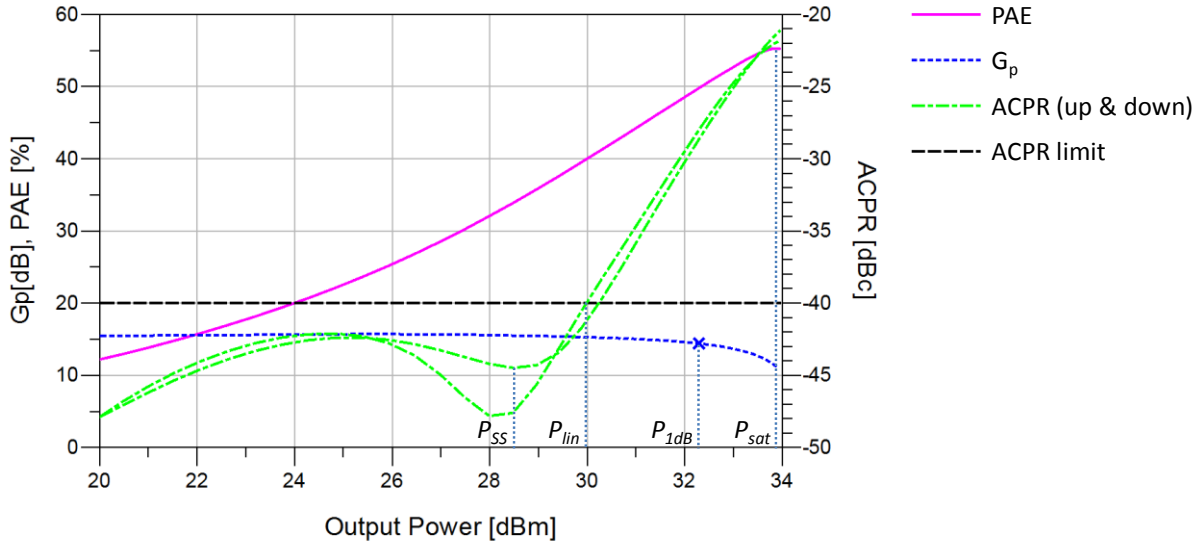

Figure 22: Gain, ACPR and power added efficiency performance of a 3G power amplifier

II-1.1. Power gain

From Figure 23, the power gain (G_P) of the amplifier is the ratio of the output power (P_{out}) over the input power (P_{in}) as expressed by Equation 4.

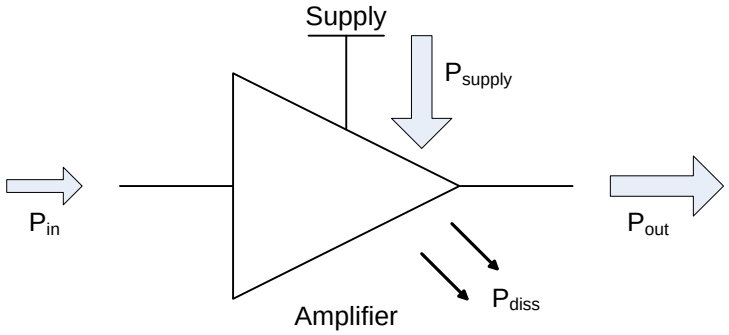

Figure 23: Schematic representation of the power flowing in and out of a power amplifier.

$$G_P = \frac{P_{out}}{P_{in}} \qquad \text{Equation 4}$$

Figure 24 depicts a power amplifier together with its source and load impedances as well as all the different power expressions along the amplifier stage.

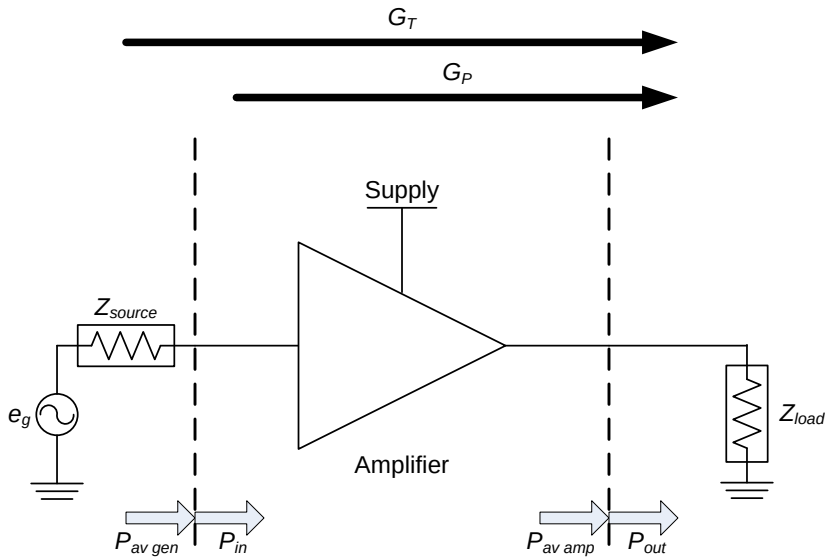

Figure 24: Power amplifier with source and load impedances.

On this schematic, the input power is delivered to the PA by a power source characterized by a RF voltage e_g and source impedance Z_{source}. The amplified output signal is delivered to the load impedance Z_{load}. The transducer gain is the ratio between the output power and the available power from the generator (Equation 5).

$$G_T = \frac{P_{out}}{P_{av_{gen}}} \qquad \text{Equation 5}$$

In order to avoid reflection at the input of the power amplifier, the source impedance should be matched to the conjugate input impedance of the amplifier. In that case, $P_{in} = P_{av\ gen}$ and $G_T = G_P$.

II-1.2. Efficiency

Due to dissipated power P_{diss}, only part of the supplied power is contributing to the amplification. Efficiency is a measure of the DC power conversion to RF power. In PA design, we define two different expressions for efficiency. The first is the drain efficiency, which is given by Equation 6.

$$\eta = \frac{P_{out}}{P_{supply}} \qquad \text{Equation 6}$$

The power added efficiency (*PAE*) takes into account the input power as shown in Equation 7. Note that using Equation 8, *PAE* can also be expressed as a function of η and G_p.

$$PAE = \frac{P_{out} - P_{in}}{P_{supply}} \qquad \text{Equation 7}$$

$$PAE = \eta \cdot \left(1 - \frac{1}{G_p}\right) \qquad \text{Equation 8}$$

Using this equation, it becomes clear that the higher G_p, the closer *PAE* is to η. The objective for the PA designer is to maximize PAE. Efficiency is a critical parameter when comparing different PA design. In this work, when efficiency is mentioned without further indication, it is referring to *PAE*.

II-1.3. Linearity

Linearity is another critical parameter which has to be traded-off with efficiency in PA design. A power amplifier is not operating linearly most of the time as large signal operation leads to non linearity.

A. Compression and saturation

Compression and saturation can be observed on the gain characteristic of a power amplifier. Figure 25 shows the output power and power gain as a function of input power.

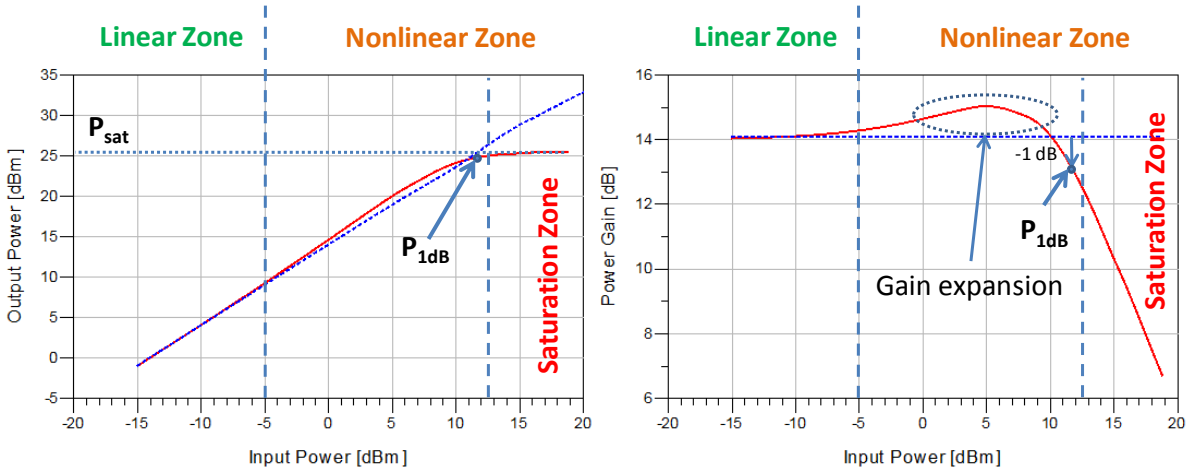

Figure 25: Output Power (left) and Power Gain (right) versus Input Power of a medium power amplifier.

On this figure, two domains can be distinguished. The first one is the linear zone, for which the gain is constant. Operation in this zone is also called Small Signal operation as the magnitude of RF signal is small enough to ensure linear operation.

The non-linear zone is characterized by variations of gain according to the input power. When the amplifier operates in this zone, gain expansion and/or compression (*AM/AM* distortion) occurs; as well as phase shift (*AM/PM* distortion). The 1dB compression point (P_{1dB} *or* IP_1) is the point at which the gain is 1dB lower than the ideal linear gain extrapolation, shown in dotted line on Figure 25.

Under specific conditions, the PA can show gain expansion. On Figure 25, between -5dBm and 10dBm of input power, where the gain is higher than the small signal gain. This condition can be exploited to boost the gain of the power amplifier and therefore increase the P_{1dB}.

Another specific region can be defined inside the non-linear zone and is called saturation zone. In this range, the output power of the PA is saturated at a maximum value (P_{sat}).

B. Inter-modulation

Inter-modulation distortion can be observed by injecting two tones at the input of the PA device and by observing the output spectrum of the PA. Figure 26 shows such response for orders limited to 3.

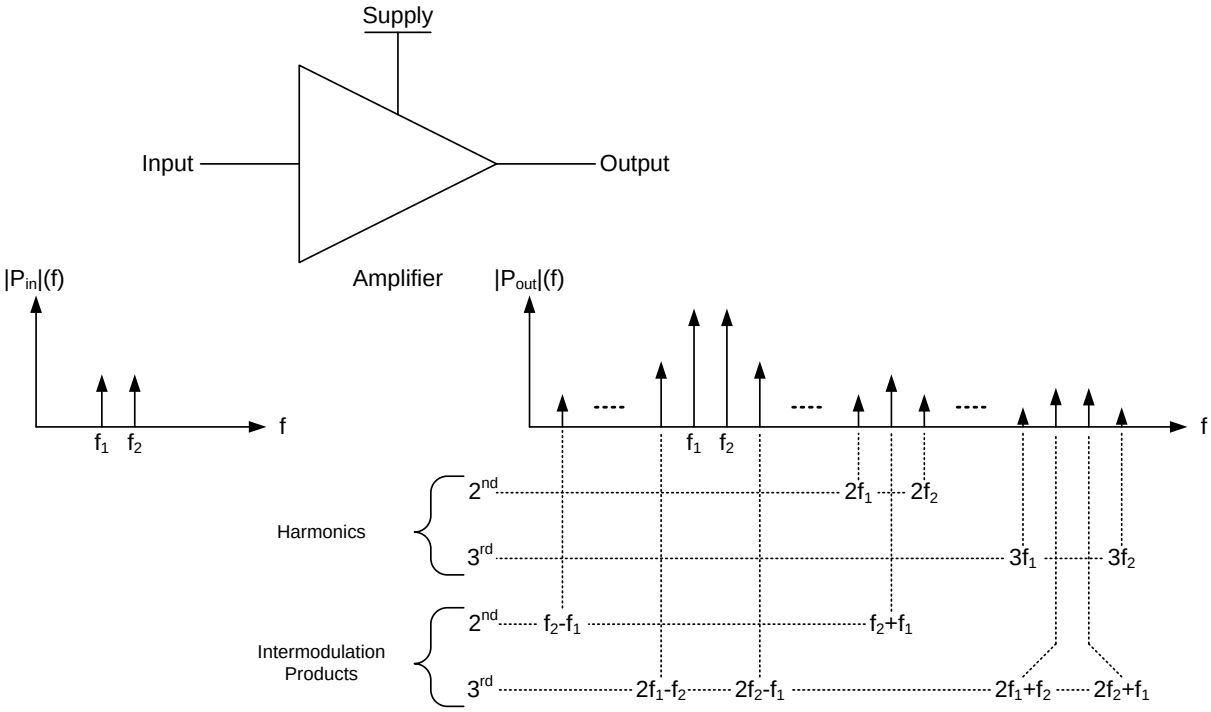

Figure 26: Illustration of the inter-modulation distortion of a power amplifier.

As can be seen on the figure, the 3rd order inter-modulation distortion (*IMD₃*) products are close to the fundamental frequencies. Considering the two fundamentals represent the desired signal bandwidth, or channel, IMD_3 represents signal leakage in adjacent channels. Therefore, IMD_3 constitute another criterion to quantify non-linearity of a PA device. Figure 27 shows a schematization of IMD_3 quantification.

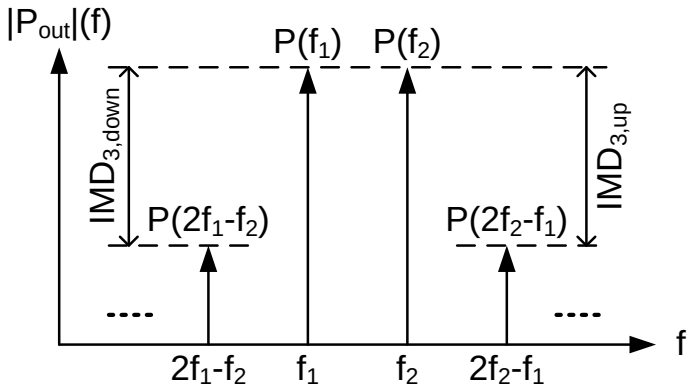

Figure 27: Two tone PA response showing 3rd Order Inter-Modulation Distortion

The *IMD₃* "up" is the difference between the higher tone and the higher *IMD₃*, see Equation 9. Equivalently, the same definition can be given for the *IMD₃*, "down", see Equation 10.

$$IMD_{3_{up}}[dBc] = P(2f_2 - f_1)[dBm] - P(f_2)[dBm] \quad \text{Equation 9}$$

$$IMD_{3_{down}}[dBc] = P(2f_1 - f_2)[dBm] - P(f_1)[dBm] \quad \text{Equation 10}$$

It is worth noting that *IMD₃* may be asymmetric due to memory effects [Carvalho02]. One side may show a higher level of *IMD₃* than the other.

C. PA linearity under complex modulated signal

Former standards such as GSM were based on signal using only phase modulation of the baseband signal. In new standards, in order to have better spectral efficiency for new generations, amplitude and phase of the baseband signal are both modulated. A comparison of the GMSK signal used 2G and the QPSK signal used in W-CDMA is done in the following section.

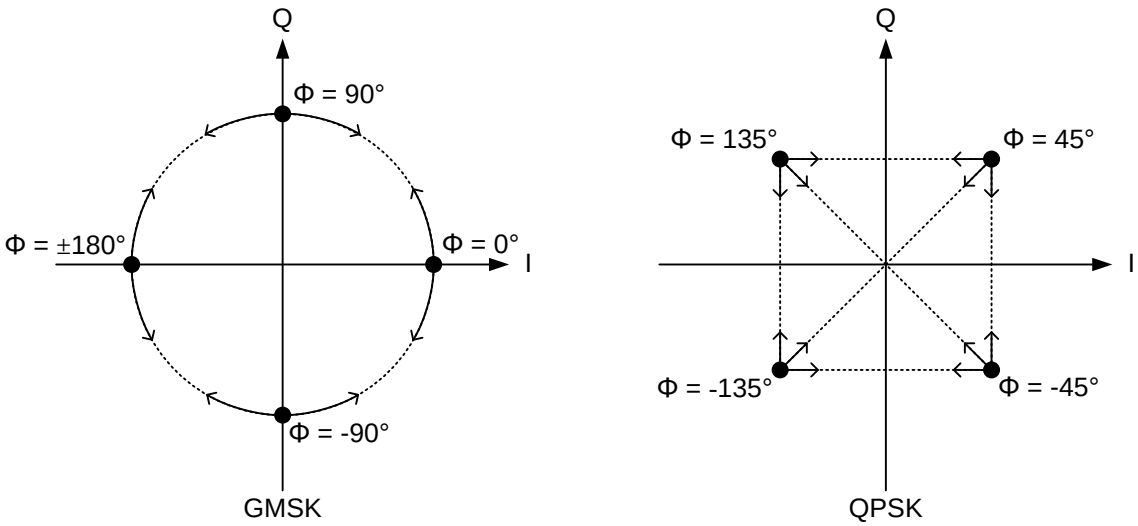

Figure 28: Constellation diagrams of a GMSK signal (left) and QPSK signal (right)

The GMSK signal is generated to allow phase shifts while maintaining constant amplitude. For instance, when the signal is at phase 90°, the next symbol will either have a phase of 0° of 180°. While changing from one symbol to another, the amplitude of the signal is kept constant. The constant amplitude of the signal is represented by the dotted circle on the diagram.

For QPSK, there is no specific signal processing to avoid transitions through 0. For instance, if the signal is at phase -45°, the next symbol's phase can be 45°, -135° or even 135°. As there is no means to ensure the signal will maintain its amplitude, in any transition the signal's amplitude will vary, as represented by the dotted square and diagonal lines.

Due to the PA's amplitude distortion (*AM/AM*) and phase distortion (*AM/PM*) when operated in the non-linear zone, out-of-band and in-band distortion happen

a. Adjacent Channel Power Ratio & Alternate Channel Power Ratio

Spectral regrowth or Adjacent Channel Leakage, defined by Adjacent Channel Power Ratio (*ACPR*) and Alternate Channel Power Ratio (*AltCPR*) are the result of *AM/AM* and *AM/PM* distortion. Figure 29 shows the spectrum of 3G signal after amplification by the PA.

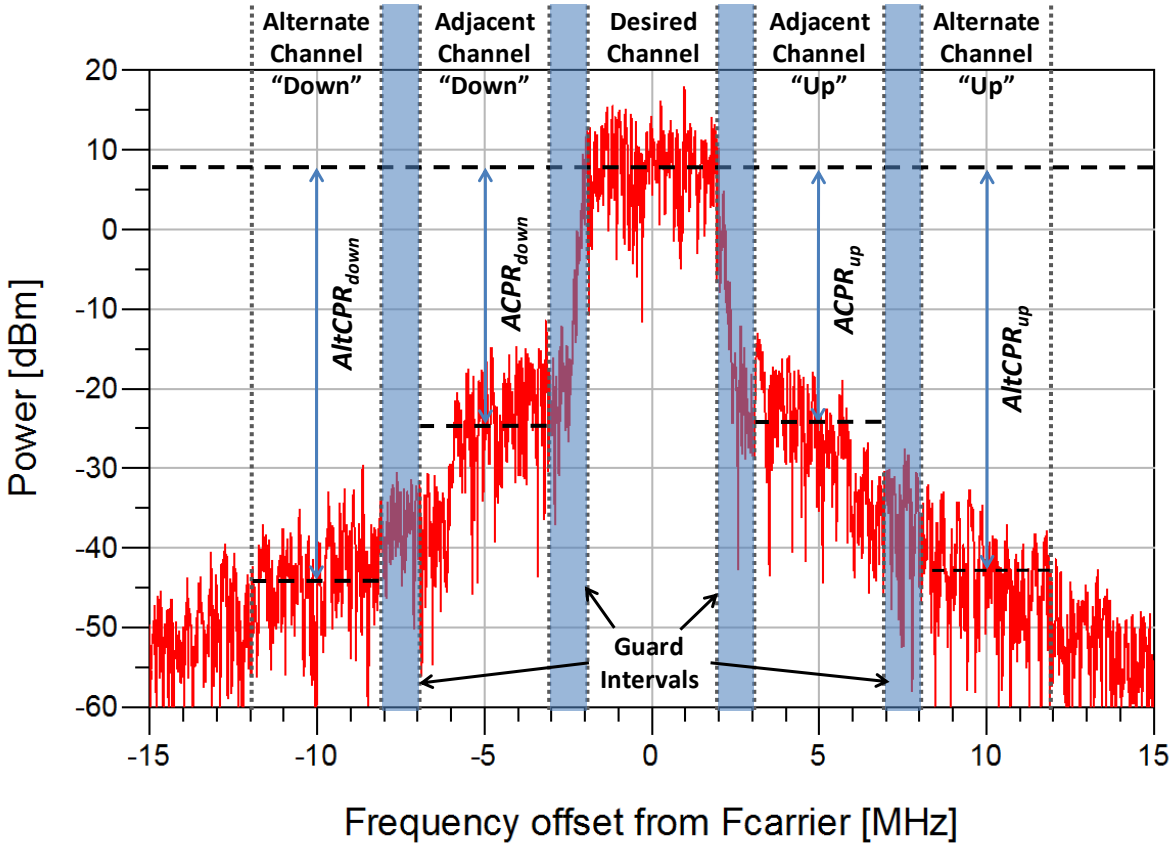

Figure 29: Spectrum of 3G signal after amplification showing spectral re-growth

It is important to note that each channel corresponds to a potential frequency allocation for a user. If the power emitted in an adjacent channel is too high, the user occupying this channel can have his signal jammed. *ACPR* and *AltCPR* are the quantification of the average power generated in the adjacent and alternate channels compared to the average power in the amplified channel. They are defined in Equation 11 and Equation 12, where *x* stands for either "up" or "down".

$$ACPR_x[dBc] = \langle P_{adj_x} \rangle [dBm] - \langle P_{chan} \rangle [dBm] \quad \text{Equation 11}$$

$$AltCPR_x[dBc] = \langle P_{alt_x} \rangle [dBm] - \langle P_{chan} \rangle [dBm] \quad \text{Equation 12}$$

In order to avoid interference between users, the cellular standards give limitations for *ACPR*. The output power level for which this *ACPR* limit is reached is called linear power (P_{lin}).

b. Error Vector Magnitude

Non-linearity of the power amplifiers leads to distortion inside the amplified channel. The result can be observed on the constellation diagram. Figure 30 shows an example of distortion using a QPSK signal.

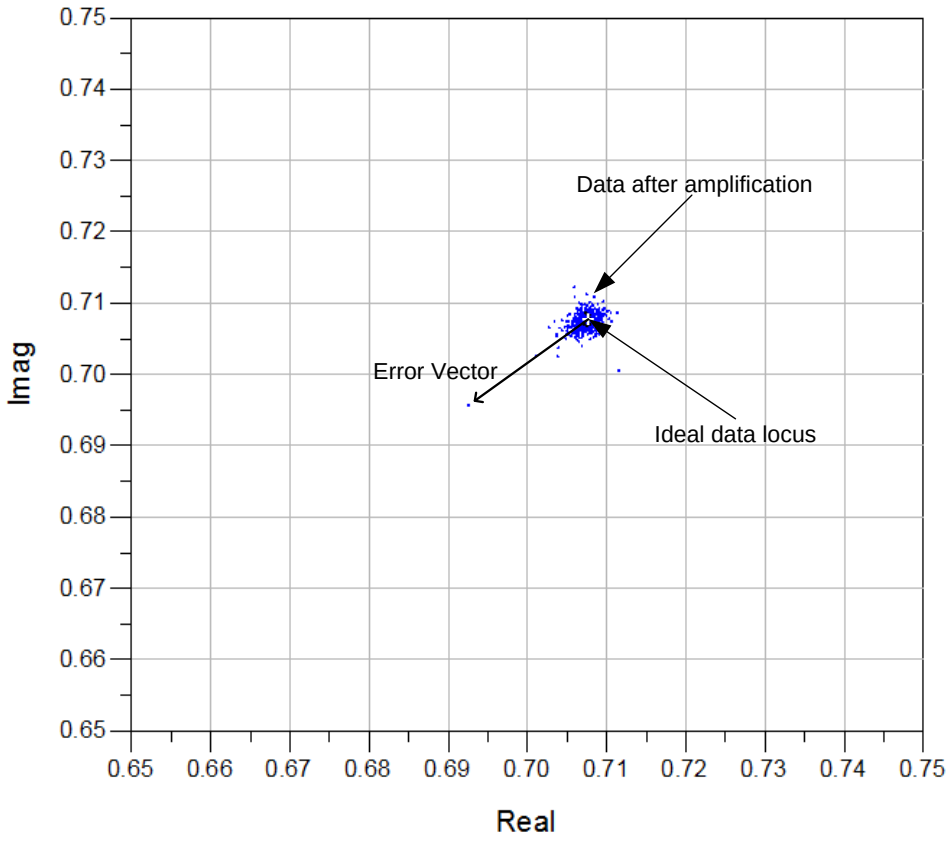

Figure 30: Constellation of a QPSK signal after amplification through non-linear PA

The picture shows the ideal locus of the constellation (white **+** symbol). After amplification, the measured constellation symbols have spread around the ideal locus because of the in-band distortion, as shown using blue dots on the picture. The error vector is defined as the vector difference between the ideal locus of the symbol and the outmost point of the real data. The Error Vector Magnitude (*EVM*) quantifies the error made when amplifying the signal.

In order to ensure correct transmission of the signals, standards often define an EVM specification.

The design of power amplifier is described in the following sections by taking into account the parameters defined previously.

II-2 Power stage design

Performances of a PA are mainly determined by the power stage. In this part, the design of the power stage is described. First, the LDMOS transistor model and design parameters are described. Afterwards, different operating classes are introduced, and then a design methodology is proposed for saturated and linear power stage.

II-2.1. LDMOS transistor model

The study and design methodology use the LDMOS transistor model depicted in Figure 31.

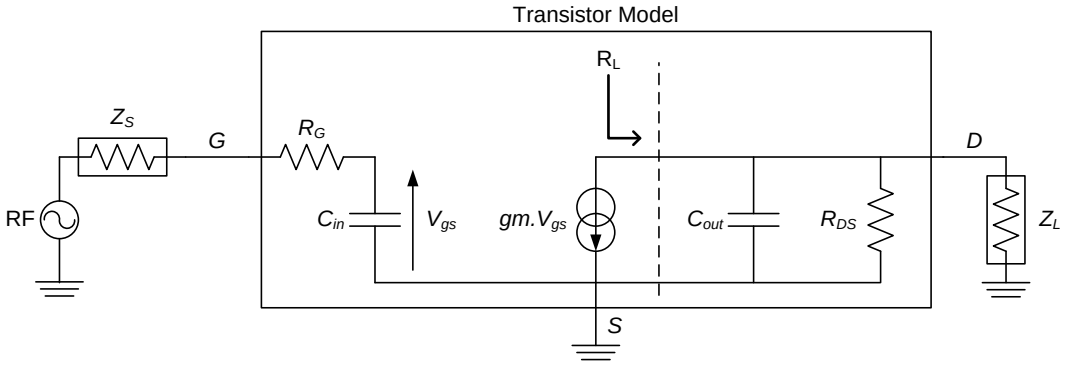

Figure 31: LDMOS transistor model used in the study.

This model is derived from the small signal model where the gate drain capacitance is distributed in C_{in} and C_{out} using Miler's formulae as shown in Equation 14 and Equation 15.

$$A = -gm \cdot \frac{R_L \cdot R_{DS}}{R_L + R_{DS}} \quad \text{Equation 13}$$

$$C_{in} = C_{GS} + (1 + A)C_{GD} \quad \text{Equation 14}$$

$$C_{out} = C_{DS} + \left(1 + \frac{1}{A}\right) C_{GD} \quad \text{Equation 15}$$

As shown in Figure 31, to ensure the equivalent load viewed by the current source ($gm.V_{gs}$) is the optimal load impedance R_L, the load impedance Z_L of the LDMOS transistor has to compensate the impact of C_{out} and R_{DS}, as shown in Equation 17.

$$R'_L = \frac{R_{DS}R_L}{R_{DS} - R_L} \quad \text{Equation 16}$$

$$Z_L = \frac{R'_L}{1 - jR'_L C_{out}\omega} \quad \text{Equation 17}$$

The design parameters, such as R_L and the width of the LDMOS transistor, are determined using the application requirements.

II-2.2. Design parameters

PA design starts with the required saturated output power P_{sat}, which is expressed as a function of the output RF voltage (V_{RF}) and the output RF current (I_{RF}) in the current source plan, as shown in Equation 18.

$$P_{sat} = Re\left\{\frac{V_{RF}I^*_{RF}}{2}\right\} \quad \text{Equation 18}$$

The optimal load resistance to present to the current source of the LDMOS transistor is determined with Equation 19.

$$R_{L_{opt}} = \frac{V_{RF}}{I_{RF}} \qquad \text{Equation 19}$$

From this expression, the optimal load of the LDMOS transistor can be rewritten as Equation 20.

$$R_{L_{opt}} = \frac{(mag\{V_{RF}\})^2}{2P_{sat}} \qquad \text{Equation 20}$$

Finally, the efficiency of the device at the saturation is calculated thanks to P_{sat} and P_{DC} (see Equation 21) where I_{dq} is the quiescent DC current of the device and V_{DD} the supply voltage. The final efficiency expression is given in Equation 22.

$$P_{DC} = V_{DD} I_{dq} \qquad \text{Equation 21}$$

$$\eta = \frac{P_{sat}}{P_{DC}} = \frac{Re\{V_{RF} I_{RF}^*\}}{2V_{DD} I_{dq}} \qquad \text{Equation 22}$$

The RF voltage is limited by the load line of the LDMOS transistor and the I_{ds}/V_{ds} characteristic of the LDMOS transistor, as shown in Figure 32.

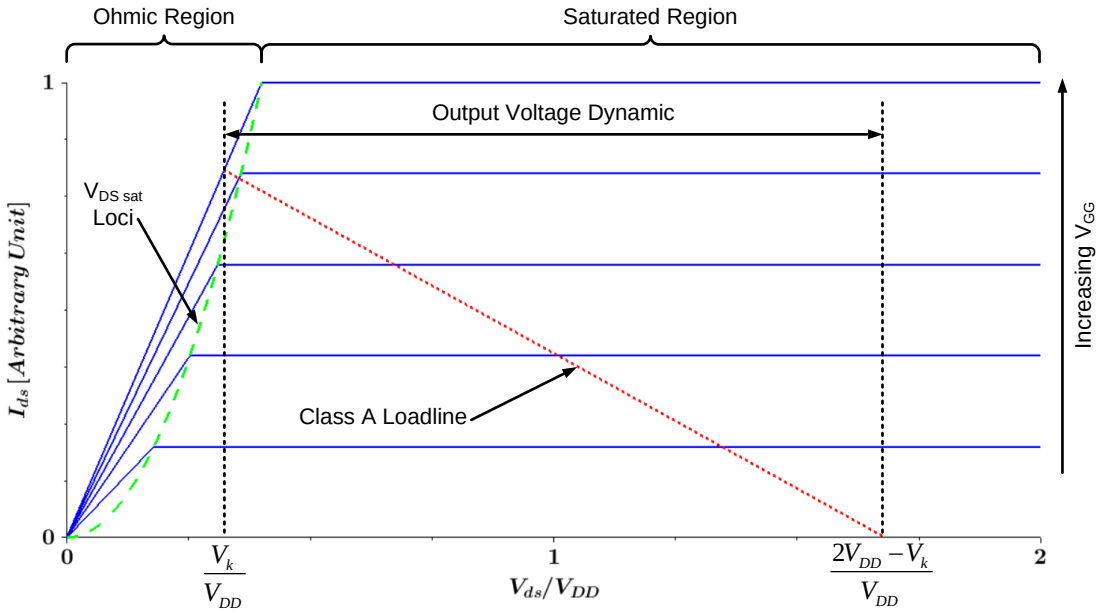

Figure 32: Linearized I_{DS} vs.V_{DS} characteristic (solid lines) and load line (dotted line) of a common source LDMOS transistor.

As can be seen in the figure, the knee voltage V_k is due to the on-state resistance R_{on} presented by the LDMOS transistor in the Ohmic region and expressed as Equation 23.

$$V_k = R_{on} \cdot I_{max} \qquad \text{Equation 23}$$

V_k limits the RF voltage dynamic at the drain of the LDMOS transistor as well as impacting efficiency and linearity. It is therefore a parameter that will need careful setting when designing a PA.

The study of operating classes depending on the bias voltage V_{GG} gives information on the frequency distribution of the voltage and current of the current source. We can therefore deduce the expected efficiency and linearity performance of the device as well as its optimal load.

II-2.3. Classes of operation

Operating class study allows an analytic determination of power stage efficiency and linearity. Figure 33 depicts the LDMOS transistor model used to study the operating classes.

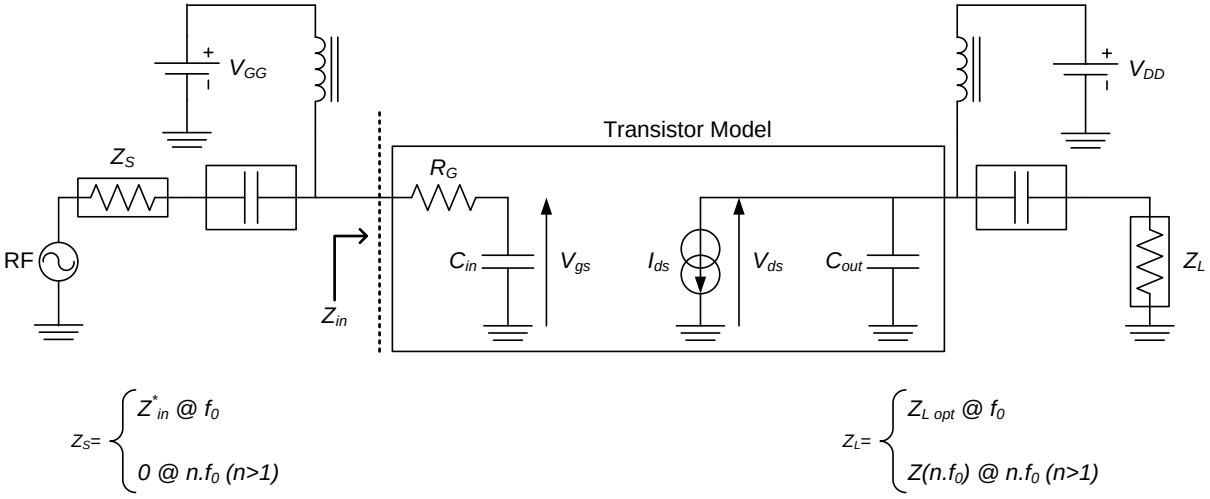

Figure 33: LDMOS transistor model used for the study on operating classes.

Classes of operation are defined by the waveforms of the input RF voltage V_{gs}, the output RF voltage V_{ds} and output RF current I_{ds} of the transistor [Hallman32]. As can be seen on the figure, the source impedance Z_S shorts all the harmonic frequencies (Z_S ($n.f_0$) = 0). This ensures that V_{gs} is a single tone sine wave at the fundamental frequency (f_0). Sinusoidal classes are characterized by a sinusoidal V_{ds}. This is realized by shorting the voltage harmonics (Z_L *(n.f0) =0*). For the non-sinusoidal classes, appropriate harmonic terminations must be presented to the LDMOS transistor according to the desired class.

A. Sinusoidal Classes

The differences among the sinusoidal classes come from the behavior of I_{ds}. This behavior is set by the DC bias voltage V_{GG}. Figure 34 shows the output RF current response in classes A, AB, B and C according to the corresponding DC bias V_{GG} (V_A, V_{AB}, V_B or V_C) and input voltage amplitude.

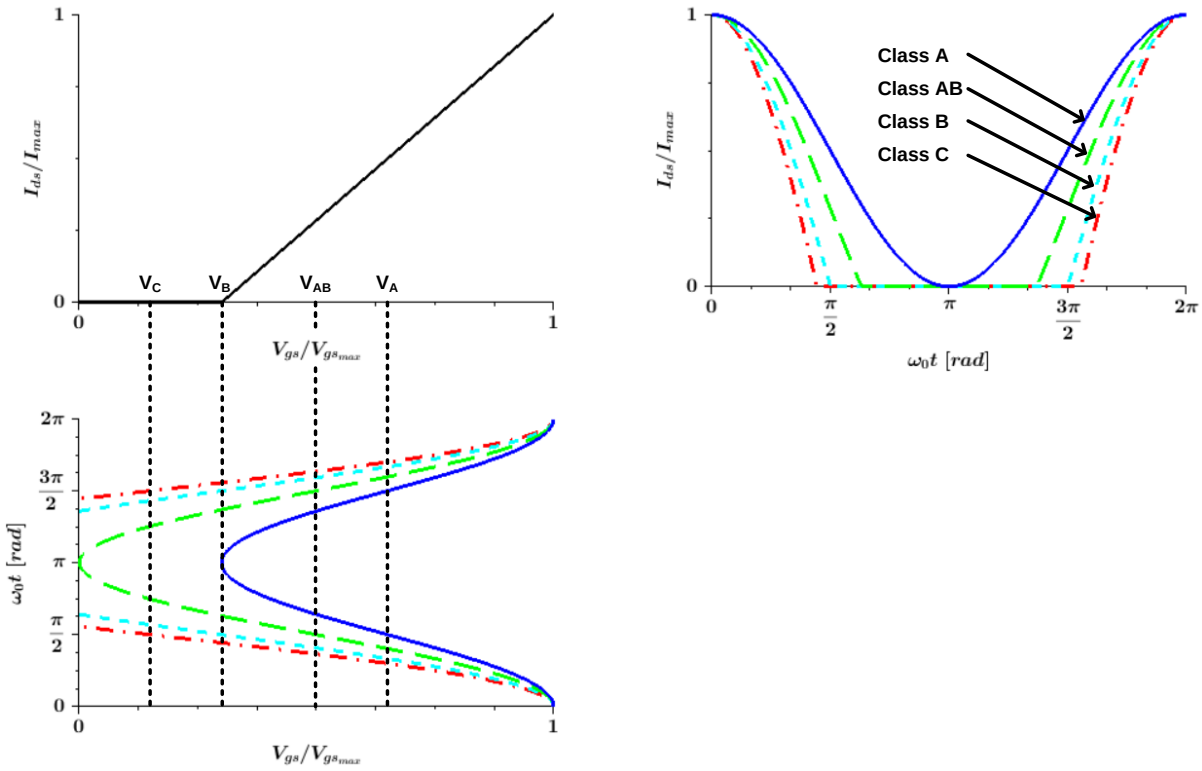

Figure 34: Input and output waveforms for Class A, AB, B and C

The conduction angle φ corresponds to the period of time where the LDMOS transistor is conducting (I_{DS}>0) and is a function of the gate bias voltage and input voltage excursion as shown in the following Table 12, where V_{th} is the threshold voltage of the LDMOS transistor and $V_{GS\,max}$ is the maximum gate-source voltage.

Table 12: Aperture and conduction angles and DC bias voltage for classes A, AB, B and C

Class	Conduction Angle	Bias Voltage V_{GG}
A	$\varphi = 2\pi$	$V_A = \frac{V_{GS_{max}} + V_{th}}{2}$
AB	$\pi < \varphi < 2\pi$	$V_{th} < V_{AB} < \frac{V_{GS_{max}} + V_{th}}{2}$
B	$\varphi = \pi$	$V_B = V_{th}$
C	$0 < \varphi < \pi$	$V_C < V_{th}$

In the following section, we consider two different models for the LDMOS transistor drain current I_{DS}. The first model is a "linear" model where I_{DS} is a linear function of V_{GS}, as shown in Equation 24.

$$I_{ds}(t) = \begin{cases} I_{max}\left[\frac{V_{GS}(t) - V_{th}}{V_{GS_{max}} - V_{th}}\right] \; if \; V_{th} < V_{GS}(t) < V_{GS_{max}} \\ 0 \; if \; V_{GS}(t) < V_{th} \end{cases} \quad \text{Equation 24}$$

The second model is a "quadratic" model where I_{DS} is a quadratic function of V_{GS}, as shown in Equation 25.

$$I_{ds}(t) = \begin{cases} I_{max}\left[\frac{V_{GS}(t) - V_{th}}{V_{GS_{max}} - V_{th}}\right]^2 \; if \; V_{th} < V_{GS}(t) < V_{GS_{max}} \\ 0 \; if \; V_{GS}(t) < V_{th} \end{cases}$$ Equation 25

The simulated response of a LDMOS transistor and the two considered models are shown in Figure 35.

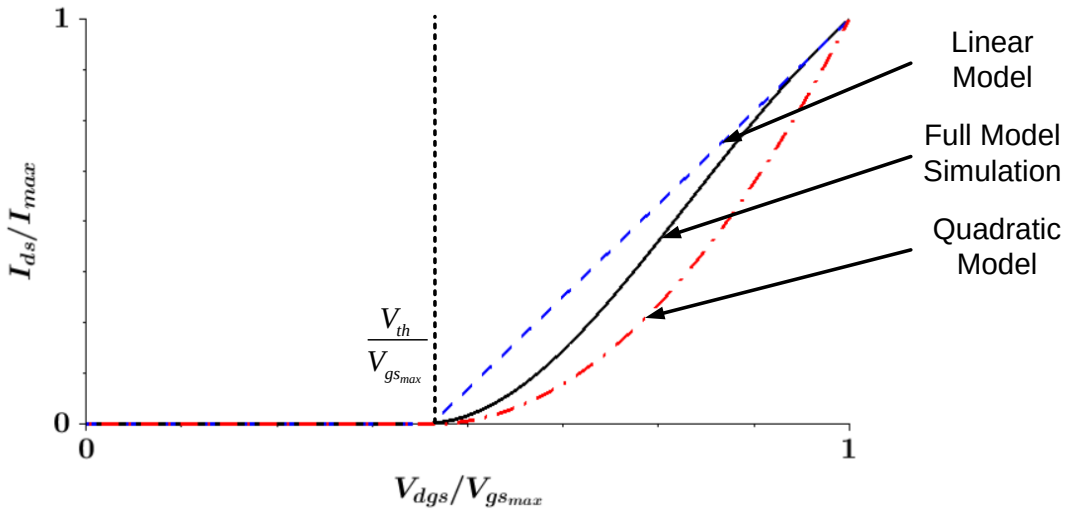

Figure 35: Response of the LDMOS transistor model, linear model and quadratic model.

These two models can be rewritten using the conduction angle. The expressions are shown in Equation 26 for the linear model and Equation 27 for the quadratic model.

$$I_{ds}(t) = I_{max}\left[\frac{cos(\omega \cdot t) - cos\left(\frac{\varphi}{2}\right)}{1 - cos\left(\frac{\varphi}{2}\right)}\right]$$ Equation 26

$$I_{ds}(t) = I_{max}\left[\frac{cos(\omega \cdot t) - cos\left(\frac{\varphi}{2}\right)}{1 - cos\left(\frac{\varphi}{2}\right)}\right]^2$$ Equation 27

As the minimum V_{ds} is V_k and the DC voltage is V_{DD}, the voltage magnitude V_m at *f0* can be written as shown in Equation 28.

$$V_m = V_{DD} - V_k$$ Equation 28

The harmonic distribution of the I_{ds} and V_{ds} are functions of φ as shown in Table 13, Table 14 and Table 15 where the Fourier coefficients of the drain voltage and current are given for the linear and quadratic models, considering a maximum current I_{max} (calculation given in Appendix A).

Table 13: DC components of each signals

Signal	DC coefficient
Voltage V_{ds}[0]	V_{DD}
Current I_{ds}[0] (Linear model)	$\frac{I_{max}}{\pi}\cdot\left[\frac{\sin\left(\frac{\varphi}{2}\right)-\frac{\varphi}{2}\cos\left(\frac{\varphi}{2}\right)}{1-\cos\left(\frac{\varphi}{2}\right)}\right]$
Current I_{ds} [0] (Quadratic model)	$\frac{I_{max}}{\pi}\cdot\frac{1}{\left(1-\cos\left(\frac{\varphi}{2}\right)\right)^2}\cdot\left[\frac{\varphi}{2}+\frac{\varphi}{4}\cos(\varphi)-\frac{3}{4}\sin(\varphi)\right]$

Table 14: Fundamental components of each signals

Signal	Fundamental coefficient
Voltage V_{ds} [f_0]	$V_m = V_{DD} - V_k$
Current I_{ds} [f_0] (Linear model)	$\frac{I_{max}}{2\pi}\cdot\left[\frac{\varphi-\sin(\varphi)}{1-\cos\left(\frac{\varphi}{2}\right)}\right]$
Current I_{ds} [f_0] (Quadratic model)	$\frac{2I_{max}}{\pi}\cdot\frac{1}{\left(1-\cos\left(\frac{\varphi}{2}\right)\right)^2}\cdot\left[\frac{3}{4}\sin\left(\frac{\varphi}{2}\right)-\frac{\varphi}{2}\cos\left(\frac{\varphi}{2}\right)+\frac{1}{12}\sin\left(\frac{3\varphi}{2}\right)\right]$

Table 15: Harmonic components of each signals

Signal	DC coefficient
Voltage V_{ds}[$n.f_0$]	0
Current I_{ds}[$n.f_0$] (Linear model)	$\frac{I_{max}}{\pi}\cdot\frac{1}{1-\cos\left(\frac{\varphi}{2}\right)}\cdot\left[\frac{\sin\left((n+1)\frac{\varphi}{2}\right)}{n+1}+\frac{\sin\left((n-1)\frac{\varphi}{2}\right)}{n-1}\right]$
Current I_{ds}[$n.f_0$] (Quadratic model)	$\begin{cases}\frac{2I_{max}}{\pi}\cdot\frac{1}{\left(1-\cos\left(\frac{\varphi}{2}\right)\right)^2}\cdot\left(\frac{\varphi}{8}-\frac{1}{6}\sin(\varphi)+\frac{1}{48}\sin(2\varphi)\right) & \text{for } n=2 \\ \frac{2I_{max}}{\pi}\cdot\frac{1}{\left(1-\cos\left(\frac{\varphi}{2}\right)\right)^2}\cdot\frac{(4-n^2)\sin\left(n\frac{\varphi}{2}\right)+(n-1)(n-2)\sin\left(n\frac{\varphi}{2}\right)\cos(\varphi)+3n\sin\left((n-2)\frac{\varphi}{2}\right)}{n(n^2-1)(n^2-4)} & \end{cases}$

Expressions of the RF output power (P_{RF}) and DC power (P_{DC}) are given by Equation 29 and Equation 30.

$$P_{RF} = \frac{k_{i_1}\cdot I_{max}\cdot(V_{DD}-V_k)}{2} \quad \text{Equation 29}$$

$$P_{DC} = k_{i_0}\cdot I_{max}\cdot V_{DD} \quad \text{Equation 30}$$

Where

$$k_{i_0} = \frac{I_{ds}[0]}{I_{max}} \quad \text{Equation 31}$$

$$k_{i_1} = \frac{I_{ds}[f_0]}{I_{max}}$$ Equation 32

Then drain efficiency η can be expressed as (Equation 33).

$$\eta = \frac{k_{i_1}}{2k_{i_0}}\left(1 - \frac{V_k}{V_{DD}}\right) = \eta_0\left(1 - \frac{V_k}{V_{DD}}\right)$$ Equation 33

In this expression, the impact of V_k on the overall efficiency appears. η_0 being only dependent on $k_{i\,0}$ and $k_{i\,1}$. Table 16 shows the expression of η_0 for the linear and quadratic models.

Table 16: Expression of η_0

Model	Expression
Linear	$\eta_0 = \frac{\varphi - \sin(\varphi)}{4\left[\sin\left(\frac{\varphi}{2}\right) - \frac{\varphi}{2}\cos\left(\frac{\varphi}{2}\right)\right]}$
Quadratic	$\eta_0 = \frac{\frac{3}{4}\sin\frac{\varphi}{2} - \frac{\varphi}{2}\cos\left(\frac{\varphi}{2}\right) + \frac{1}{12}\sin\left(\frac{3\varphi}{2}\right)}{\frac{\varphi}{2} + \frac{\varphi}{4}\cos(\varphi) - \frac{3}{4}\sin(\varphi)}$

The two expressions are plotted in Figure 36.

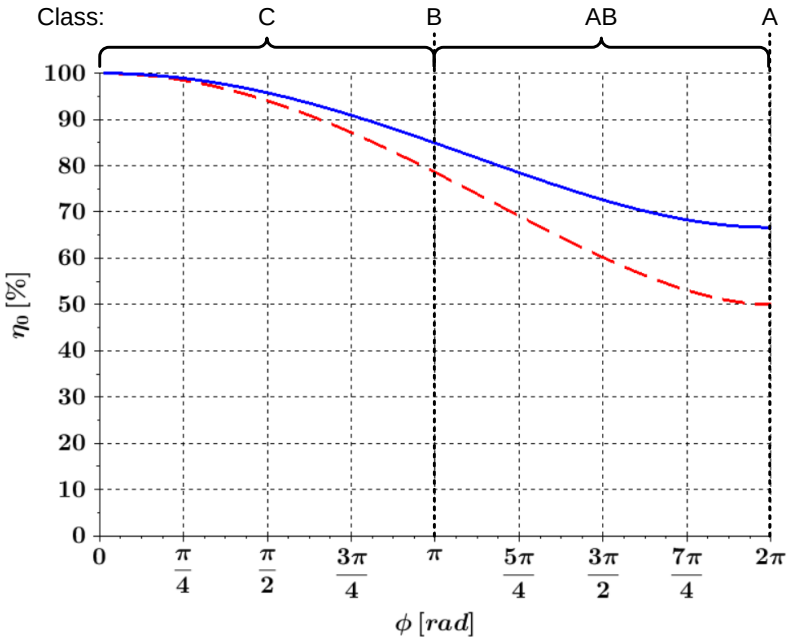

Figure 36: Comparison of the drain efficiency obtain with both model according to the class using the linear model (red dashed line) and quadratic model (solid blue line).

When comparing the two models, the linear model gives a lower estimation of the drain efficiency, especially for high φ values. By reducing φ, it is possible to improve the efficiency but at the expense of linearity since the harmonics content increases, as shown in Figure 37.

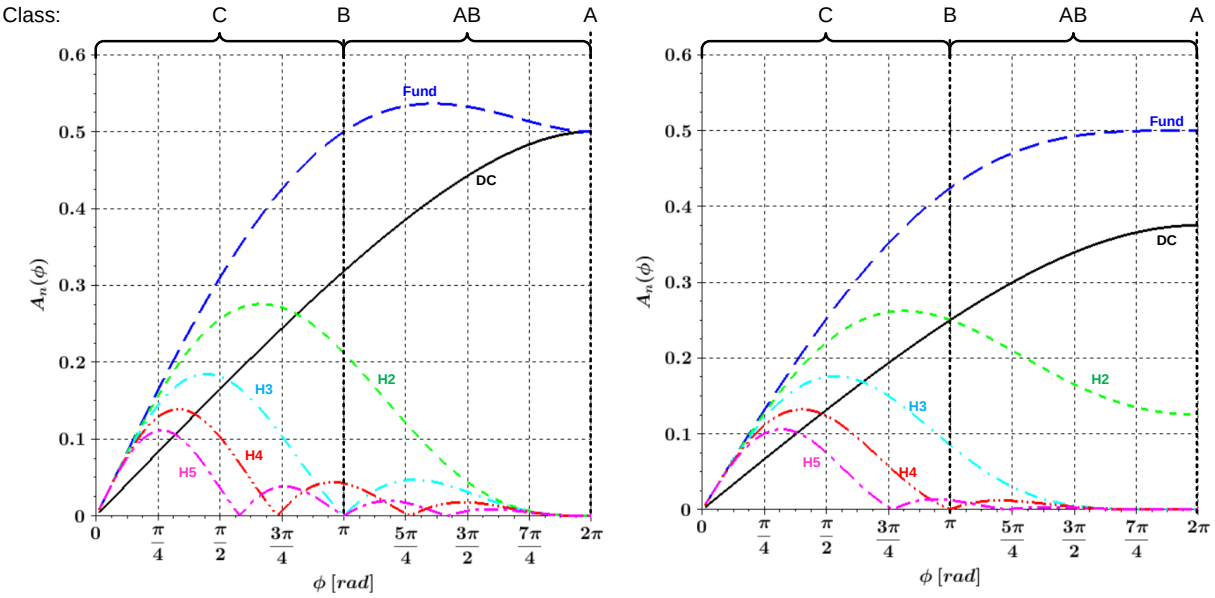

Figure 37: Calculated first 5 harmonic components of sinusoidal classes using the linear model (left) and quadratic model (right) versus the conduction angle Φ.

The figure shows the calculated harmonic components of the RF current I_{ds} versus φ using both the linear model and quadratic model. For both models, it can be seen that in class A, the harmonic content is minimal. As φ is reduced, the harmonic content of the current increases and becomes maximal in class C.

B. Classes F and F-1

In non sinusoidal classes, the output voltage V_{ds} is not limited to a sinus waveform. With other waveforms shaping [Cripps06], such as square or half sinusoidal waveforms, the frequency distribution is different. Therefore, with similar DC consumption, higher RF power at f_0 can be generated. The efficiency is thus higher. On the other hand, due to the required harmonic terminations for shaping V_{ds} and I_{ds}, the linearity is decreased.

Two classes will be studied in this paragraph: Class F and Class F^{-1} [Kim11]. First, Class F which is characterized by a square RF voltage V_{ds} and a half rectified sine RF current I_{ds} waveform. This is achieved using harmonic terminations. The second harmonic is terminated by a short, forcing a null voltage at the second harmonic. The third harmonic is terminated by an open, nullifying the current at the second harmonic.

The inverse Class F, also noted Class F^{-1} reverses the definitions of the output RF voltage and current: the current is a square wave while the voltage is a half rectified sine wave. The second harmonic in this case is terminated by an open while the third harmonic is terminated by an open.

In both Class F and Class F^{-1}, the LDMOS transistor conducts current for half a period, which is equivalent to have $\varphi = \pi$.

The Fourier coefficients for Class F and Class F^{-1} are given in Table 17 and Table 18, based on the calculation of Appendix B.

Table 17: DC components of voltage and current in Class F and Class F^{-1}

Signal	DC coefficient in Class F	DC coefficient in Class F^{-1}
Voltage V_{ds}[0]	V_{DD}	V_{DD}
Current I_{ds}[0]	$\frac{I_{max}}{\pi}$	$\frac{I_{max}}{2}$

Table 18: Fundamental components of voltage and current in Class F and Class F^{-1}

Signal	Fundamental coefficient in Class F	Fundamental coefficient in Class F^{-1}
Voltage V_{ds} [f_0]	$\frac{4}{\pi}(V_{DD}-V_k)=\frac{4V_m}{\pi}$	$\frac{\pi}{2}(V_{DD}-V_k)=\frac{\pi V_m}{2}$
Current I_{ds} [f_0]	$\frac{I_{max}}{2}$	$\frac{2I_{max}}{\pi}$

Using those coefficients, it is possible to determine the fundamental distribution coefficient k_{v1} for the fundamental frequency of the voltage RF signal, see Equation 34. Similarly, DC current and fundamental distribution coefficients can be expressed as Equation 35 and Equation 36.

$$k_{v1}=\frac{V_{ds}(f_0)}{(V_{DD}-V_k)}=\frac{V_{ds}(f_0)}{V_m} \quad \text{Equation 34}$$

$$k_{i_0}=\frac{I(DC)}{I_{max}} \quad \text{Equation 35}$$

$$k_{i_1}=\frac{I(f_0)}{I_{max}} \quad \text{Equation 36}$$

Using those coefficients it is possible to write the drain efficiency as follows in Equation 37.

$$\eta=\frac{k_{i_1}\cdot k_{v1}}{2k_{i_0}}\left(1-\frac{V_k}{V_{DD}}\right)=\eta_0\left(1-\frac{V_k}{V_{DD}}\right) \quad \text{Equation 37}$$

By casting the impact of V_k aside, we can calculate η_0 in each class, see Table 19.

Table 19: Exact and approximated η_0 for classes deep AB, F and F-1, for each current model

Operation Class	Deep Class AB		Class F		Class F^{-1}	
Value	*Exact*	*Approximation*	*Exact*	*Approximation*	*Exact*	*Approximation*
Linear Model	$\frac{\pi}{4}$	79%	1	100%	1	100%
Quadratic Model	$\frac{8}{3\pi}$	85%				

This table shows that using either class F or F^{-1}, the ideal drain efficiency of the power stage can be risen to 100% for the same conduction time. This means using different spectral distribution of the signals allows higher efficiency for a degraded linearity due to the waveforms.

In the two previous sections, the theoretical efficiency attainable for chosen sinusoidal and non sinusoidal classes was evaluated. While offering high linearity, the sinusoidal classes offer limited efficiency. Conversely, the non sinusoidal classes degrade linearity to offer high efficiency. The definitions of the classes presented here can be used as the basis of power stage design, as will be shown in the following parts.

II-2.4. Saturated PA

To optimize power stage performances, the optimal load impedance as well as the width W_G of the power LDMOS transistor must be determined. These parameters depend on P_{sat}, the operating class, the supply voltage. The flowchart in Figure 38 depicts the different steps considered in the design of the power stage.

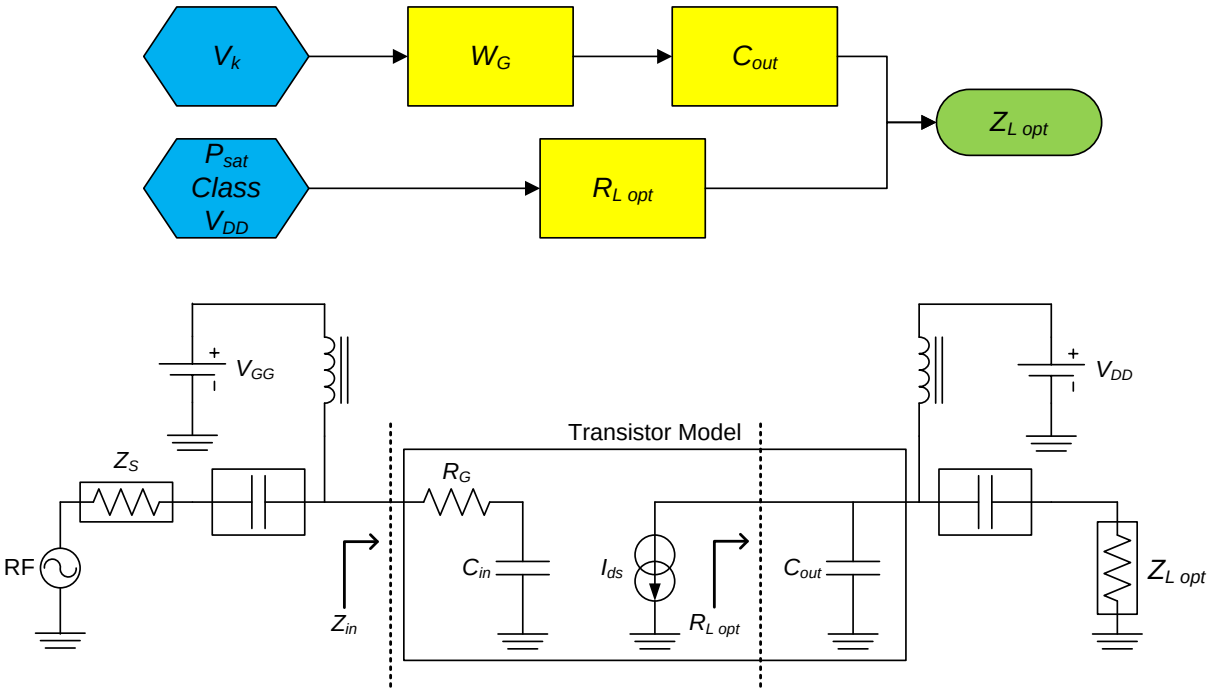

Figure 38: Power device sizing methodology and LDMOS transistor model.

By expressing I_{max} as a function of V_m and P_{sat}, we have:

$$I_{max} = \frac{2P_{sat}}{k_{i_1} k_{v_1} V_m} \qquad \text{Equation 38}$$

$$R_{on} = \frac{k_{i_1} k_{v_1} V_m V_k}{2P_{sat}} \qquad \text{Equation 39}$$

The required LDMOS transistor width W_G for a given P_{sat} is given by Equation 40 where *RonW* is the on-state resistance per gate width and $k_{i\,1}$ and $k_{v\,1}$ are the fundamental distribution coefficient for voltage and current defined previously.

$$W_G = \frac{R_{on} W}{R_{on}} = \frac{2P_{sat} \cdot R_{on} W}{k_{I_1} k_{V_1} V_m V_k} \qquad \text{Equation 40}$$

$R_{L\,opt}$ is determined using $k_{v\,1}$by replacing V_{RF} by $k_{v\,1}V_m$ in Equation 20, as shown in Equation 41.

$$R_{L_{opt}} = \frac{\left(k_{v_1}V_m\right)^2}{2P_{sat}} \qquad \text{Equation 41}$$

Figure 39 shows W_G and $R_{L\,opt}$ for classes AB, F and F^{-1} versus P_{sat}.

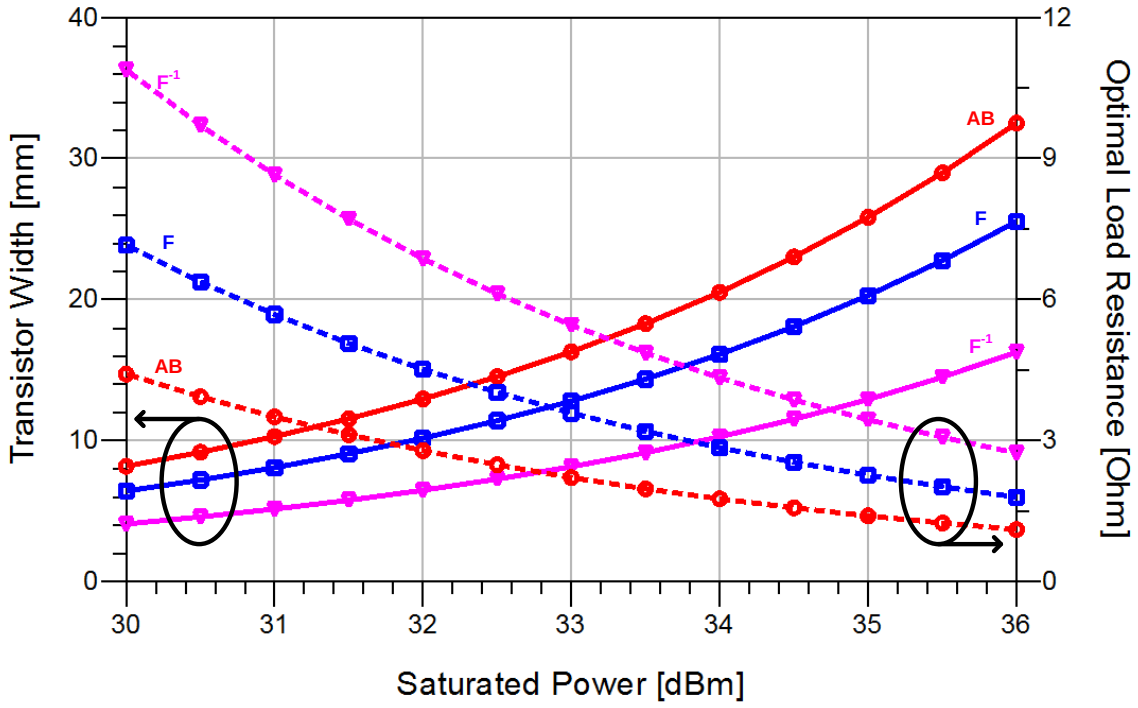

Figure 39: Required LDMOS transistor width and optimal load resistance versus saturated power

Class-F^{-1} can provide as much power as a Class-F for a reduced device size and an increased load. A smaller LDMOS transistor leads to more compact layout with reduced parasitic elements while higher load impedance leads to lower loss in the output matching network.

In order to maximize G_T, the source impedance of the PA should be matched to its input impedance. As described in Appendix C, the input impedance of the device is given by Equation 42, where R_G is the gate resistance, C_{in} the input capacitance, gm the transconductance and L_S the source inductance of the LDMOS transistor.

$$Z_{in} = \left(R_G + \frac{gm \cdot L_S}{C_{in}}\right) + j \cdot \left(L_S\omega - \frac{1}{C_{in}\omega}\right) \qquad \text{Equation 42}$$

This expression takes the parasitic inductance connecting the source of the LDMOS transistor to the ground L_S. However, the parasitic of inductance of the TSV being extremely low

(≈**50 pH**), its impact is considered negligible at the frequency of operation. Therefore the source impedance of the device should be simplified according to Equation 43.

$$Z_S = R_G - \frac{j}{C_{in}\omega} \qquad \text{Equation 43}$$

In this section, the LDMOS transistor sizing and source and load impedance determination have been described. This methodology is however based on a small signal model for design ease. When operated in large signal, the LDMOS transistor operates slightly differently. Thanks to load pull and source pull simulations, the optimal source and load impedance are adjusted to ensure the optimal performance of the device in large signal.

A. Load-Pull and Source-Pull simulations

Source and Load Pull consists in sweeping the source and load impedances respectively of a device to determine its characteristics under large signal excitation. It is then possible to plot contours of constant characteristics on a Smith chart. Figure 40 shows an example of a load pull simulation.

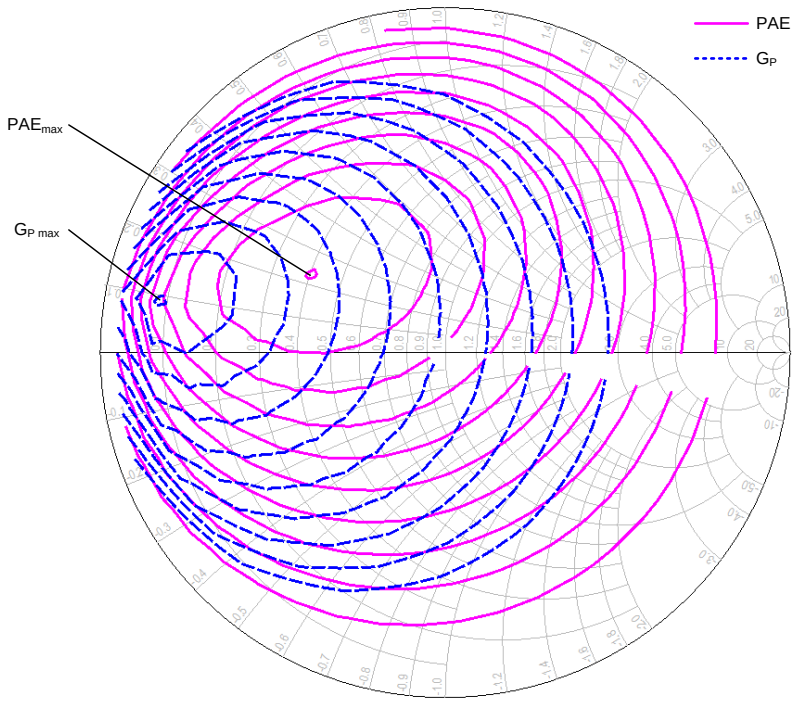

Figure 40: Load Pull contours for power gain (Gp) and power added efficiency(PAE) characteristics

In this simulation, the load impedance Z_{load} is swept over the smith chart. By calculating the gain and efficiency of the LDMOS transistor for a given frequency and input power, iso-gain and *PAE* contours can be plotted on the smith chart. As can be seen on the chart, optimum points for efficiency (PAE_{max}) and power gain ($G_{p\,max}$) correspond to different optimal load impedance. Generally a trade-off has to be found in order to determine the adequate load impedance for given specifications.

Harmonic source and load pull may also be used to determine the optimal load termination at the harmonic frequencies [Stancliff79].

B. Application of the method to saturated PA design for GSM

For GSM application, the PA has to deliver **35.5dBm** in GSM850 and GSM900 frequency bands. To overcome output matching network loss, the power stage has to deliver an output power of **36dBm**.

Previously, it has been showed that Class-F^{-1} can provide high efficiency with higher load impedance and smaller device size than Class F for a given output power (P_{sat}) and supply voltage (V_{DD}). Table 20 summarizes LDMOS transistor sizing and load impedance obtained for a targeted saturated power of **36dBm** at **900MHz** under **3.3V** voltage supply.

Table 20: LDMOS transistor sizing for Class-F-1 PA design

Class	W_G	$R_{L_{opt}}$	C_{out}	$Z_{L_{opt}}(f_0)$	$Z_{L_{opt}}(2f_0)$	$Z_{L_{opt}}(3f_0)$
F^{-1}	22mm	2.7Ω	24pF	2.5 + j0.8	Open	Short

Table 21 gives the optimal source and load impedances obtained after source and load pull optimization.

Table 21: Optimal source and load impedances after source and load pull

$Z_{L_{opt}}(f_0)$	$Z_{L_{opt}}(2f_0)$	$Z_{L_{opt}}(3f_0)$
2 + j	Open	Short

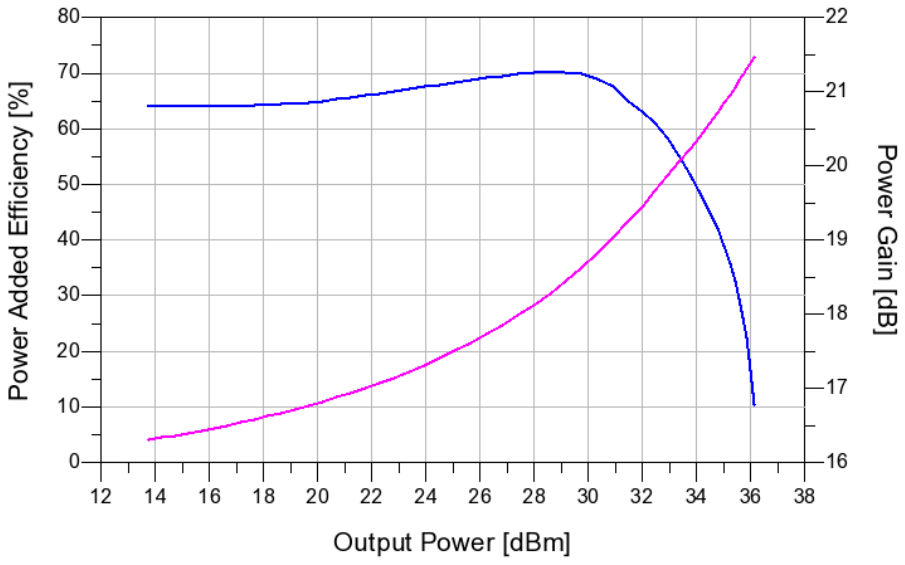

Figure 41: Simulated power added efficiency and power gain of the power cell

Figure 41 shows the simulated performance of a **22mm** LDMOS power cell with source and load impedances given in Table 21. As can be seen on the graphs, the power stage can deliver up to **36dBm** of output power with an associated efficiency and power gain of **72%** and **17dB** respectively.

II-2.5. Linear PA

The flow chart of the design of linear PA is shown in Figure 42. As can be seen in the flow chart, design of linear PA is similar to saturated PA design. The main difference between the saturated and linear PA comes from the power back-off necessary to ensure the required linearity level. As shown in Equation 44, the back-off considered between the average linear output power P_{lin} and the saturated power P_{sat} is the Peak to Average Power Ratio (*PAPR*). Knowing the PAPR in the application, P_{sat} can be determined.

$$P_{sat} = P_{lin} + PAPR$$ Equation 44

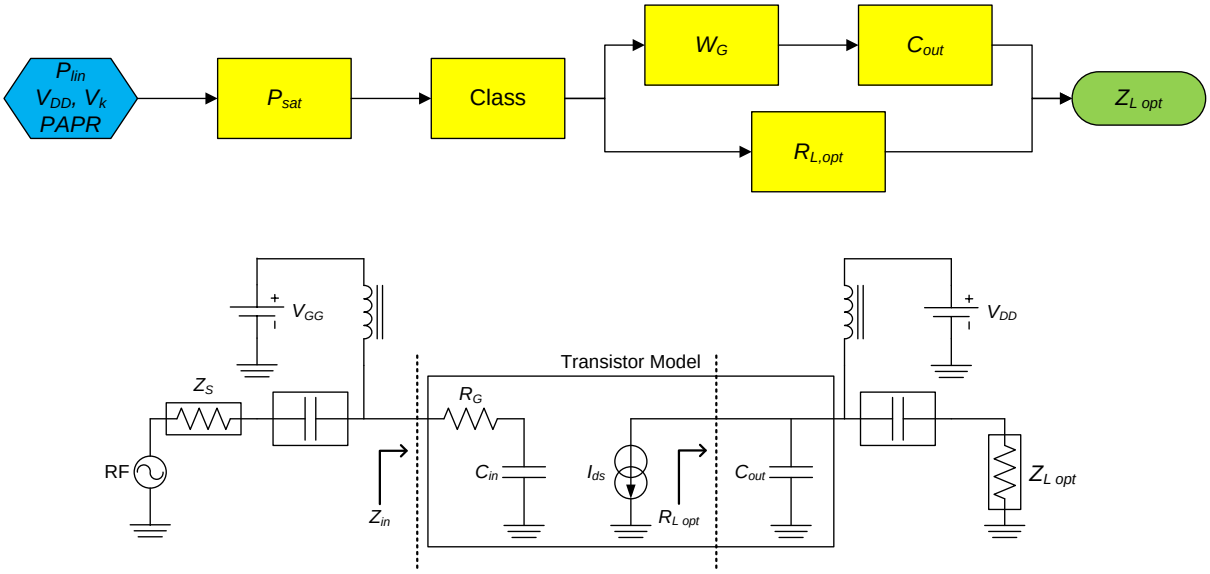

Figure 42: Linear PA design flowchart

As an example, consider the design of a WCDMA PA. For WCDMA application, the required output power is **29dBm**. To overcome loss of the output matching network, the power stage has to deliver **30dBm** of output power. For WCDMA signal (Rel99), output power is defined at a maximum ACLR level of **-40dBc** which approximately corresponds to a maximum IMD_3 level of -**30dBc**. For WCDMA, the corresponding PAPR is **3.5dB**, which gives a saturated power of **33.5dBm**.

After determining P_{sat}, the appropriate class should be selected. The can be done using the sweet-spot [Kim10]. The sweet-spot P_{SS} is the power level at which the linearity is maximal in the power sweep as shown in Figure 43 for a PA under 2-Tone excitation.

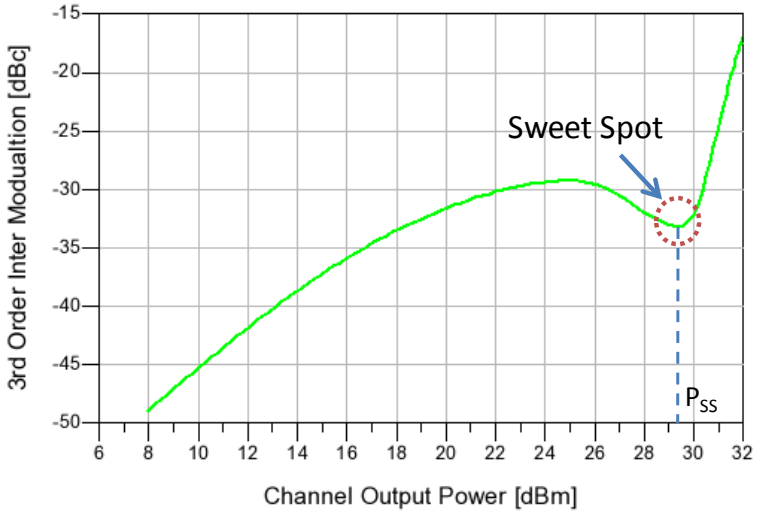

Figure 43: Sweet spot of a PA under 2-tone excitation

By analyzing the behavior of class AB, F and F^{-1} at P_{SS}, an optimal trade-off can be determined. The following table shows the simulated performance of a LDMOS transistor sized for P_{sat} = **33.5dBm** under **3.3V** supply voltage.

Table 22: Power device performance at Sweet Spot

Class	**PAE @ Sweet Spot**	**W**
Deep class-AB	50%	25mm
Class-F	58%	20mm
Class-F^{-1}	39%	12mm

As can be seen on the table, the sinusoidal Deep Class-AB requires a larger power stage than the other classes while achieving lower power gain. The efficiency is intermediate between Class-F and Class-F^{-1}. Class-F provides the highest efficiency with an intermediate gain and size. Finally, Class-F^{-1} has the highest gain performance with the lowest LDMOS transistor size but with poor linear efficiency.

Using the efficiency at sweet spot as a figure of merit, we can see that class F is the best trade-off in this case and is selected for the following example.

Table 23 gives the source and load impedance values determined by source and load pull. Note that these values are lower than those calculated using the simplified model (Figure 39).

Table 23: Source and load impedances after source and load pull

$Z_{L_{opt}}(f_0)$	$Z_{L_{opt}}(2f_0)$	$Z_{L_{opt}}(3f_0)$
2.6	Short	Open

The simulated performance of the power stage obtained with these source and load impedances and a Rel99 input signal is given in Figure 44.

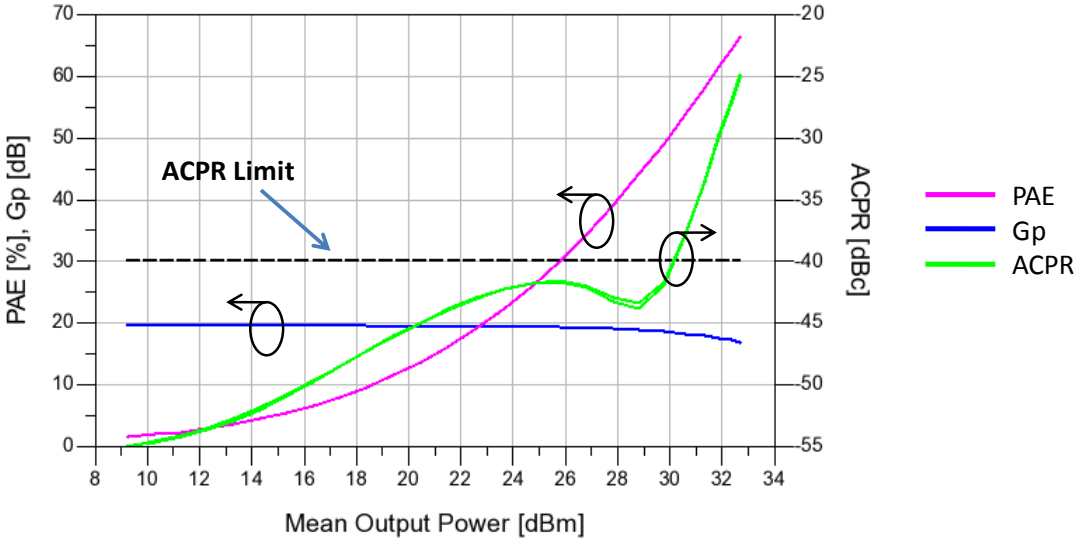

Figure 44: Simulated ACLR performance of the Class F power stage under Rel99 signal.

For a maximum ACLR level of **-40dBc**, the power stage can deliver up to **30dBm** with a corresponding efficiency of **50%.**

For LTE signal, PAPR and bandwidth are higher but ACPR specifications are relaxed since a maximum ACLR level of **-35dBc** can be tolerated. The power stage has been simulated with a 20MHz LTE signal and the obtained results are presented in Figure 45.

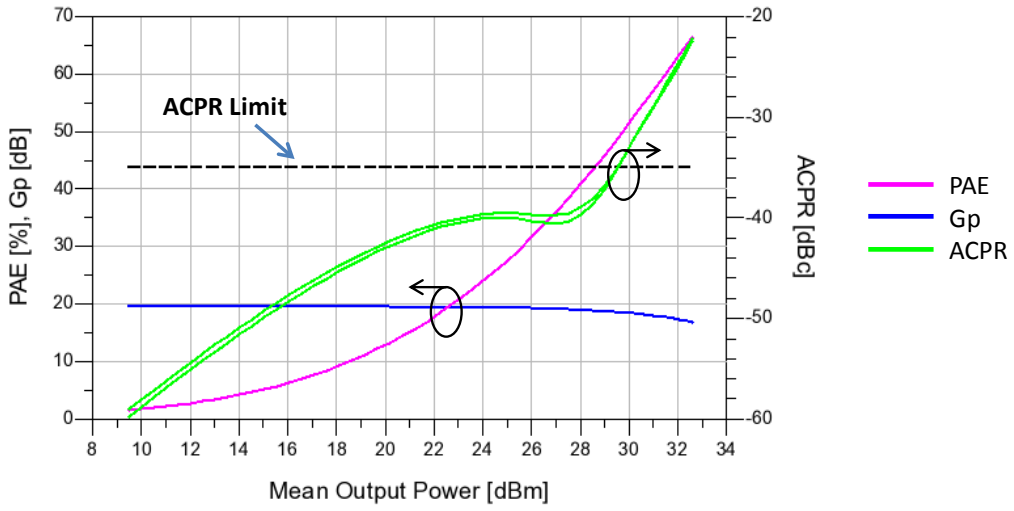

Figure 45: Simulated ACLR performance of the Class F power stageunder20MHz LTE signal

For a maximum ACLR level of **-35dBc**, the power stage can deliver up to **29.5dBm** with a corresponding efficiency of **47%**.

II-3 Output matching network design

The output matching network (OMN) is generally used at the output of the power stage to transform the system impedance, usually **50Ω**, into the optimal load impedance of the PA ($Z_{L\,opt}$) at the fundamental frequency f_0. It may also include harmonic terminations. This network should present low insertion loss (*IL*) in order to avoid degradation of the overall efficiency and output power. Transformed impedances must be maintained over a sufficiently wide bandwidth (*BW*) so that the device can operate over the specified band without performance degradation.

The design of the OMN is conditioned by the targeted *BW* and insertion losses *IL* which strongly depend on the quality factor of the passive devices (Q_{comp}). Figure 46 presents the flowchart of the matching network design considered in this work.

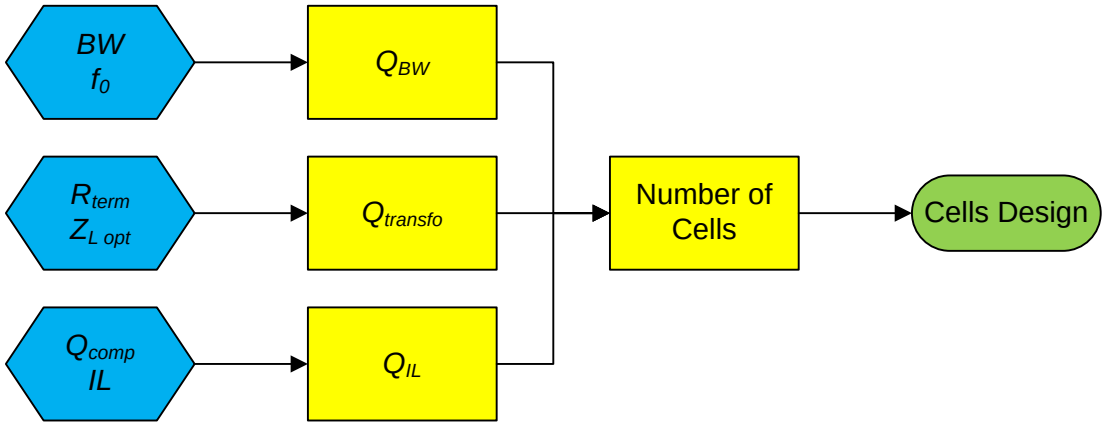

Figure 46: matching network design methodology

From f_0, *BW*, *IL* and Q_{comp}, two calculations of the matching network's Q-Factor (Q_{BW} and Q_{IL}) can be done, as shown in Equation 45 and Equation 46 [Hayward03].

$$Q_{BW} = \frac{f_0}{BW} \qquad \text{Equation 45}$$

$$Q_{IL} = Q_{comp}\left(1 - 10^{\frac{IL[dB]}{20}}\right) \qquad \text{Equation 46}$$

The transformation Q-factor ($Q_{transfo}$) is calculated as shown in Equation 47 and depicts the transformation constraint of the network, where R_{term} is the termination resistance (usually **50Ω**) and R_L is the real part of $Z_{L\,opt}$ [Han06].

$$Q_{transfo} = \sqrt{\frac{R_{term}}{R_L} - 1} \qquad \text{Equation 47}$$

$Q_{transfo}$ should be lower than Q_{BW} and Q_{IL} to ensure both the BW and IL requirements are met. The network is therefore divided in *N* L-Cells, *N* being the number required to ensure each cell's transformation Q-factor $Q_{transfo\,Cell}$ is lower than Q_{BW} and Q_{IL}.

$$Q_{transfo_{Cell}} = \sqrt[N]{Q_{transfo}} \qquad \text{Equation 48}$$

Using this division formula, we ensure a balanced distribution of the transformation ratio among the cells. This division requires specific intermediate impedances as shown in Figure 47 and Equation 49.

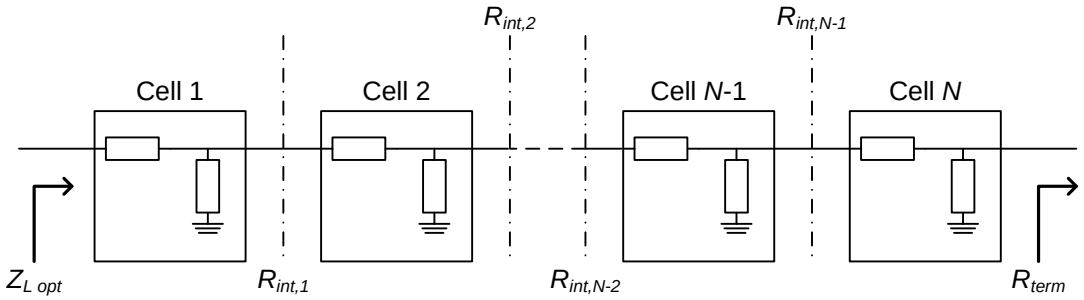

Figure 47: Intermediate impedances in a multi-cell network

$$Q_{transfo_{Cell}} = \sqrt{\frac{R_{int_1}}{R_L} - 1} = \cdots = \sqrt{\frac{R_{int_{N-1}}}{R_{int_{N-2}}} - 1} = \sqrt{\frac{R_{term}}{R_{int_{N-1}}} - 1} \qquad \text{Equation 49}$$

The imaginary part of $Z_{L\,opt}$ is correctly synthesized by adjusting the first series element of Cell 1. The intermediate impedance can be calculated recursively by using Equation 49. For instance, when two cells are required to create the network, the intermediate resistance is the geometric mean value of R_L and R_{term}. Each cell can be then calculated independently and combined with the others to create the full network.

II-4 Tunable capacitor design

Reconfigurable matching networks used for reconfigurable PA design need tunable capacitors. The chosen solution in this thesis is switched capacitor arrays. The design of such component is based on the required capacitance values, the desired overall quality factor and the operating frequency.

The elementary cell is depicted in Figure 48 and is composed of a capacitor in series with a MOS switch.

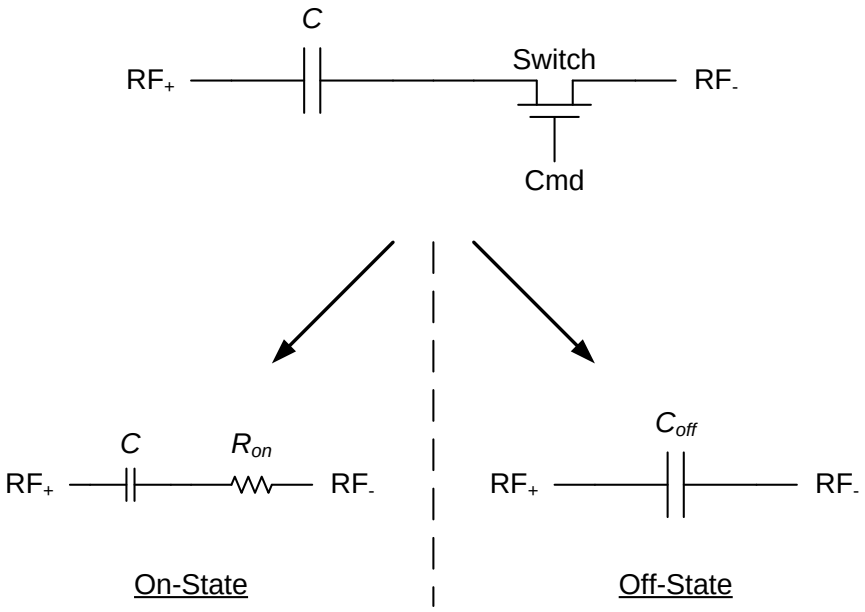

Figure 48: Tunable capacitor elementary cell

The capacitance calculation is described in the following parts. According to the capacitance C value and its quality factor (Q_C), the branch is designed to obtain the desired minimum overall quality factor Q_{branch}. The overall quality factor is at its minimum value when all the switches are on.

For a given switch technology, a figure of merit (*FOM*) for switch design is determined in Equation 50, where R_{on} is the on-state resistance of the switch and C_{off} is the off-state capacitance of the switch.

$$FOM = R_{on}C_{off} = R_{on}W\frac{C_{off}}{W} \qquad \text{Equation 50}$$

Knowing C, Q_C and Q_{branch} at the operation frequency, the required on-state resistance of the switch and finally the width of the MOS transistor is calculated by the Equation 51 – detailed calculation is presented in Appendix D.

$$W_{sw} = \frac{2\pi F_0 \cdot C \cdot Q_c \cdot Q_{branch} \cdot R_{on}W}{Q_c - Q_{branch}} \qquad \text{Equation 51}$$

II-4.1. Switched capacitor bank

The schematic of a switched capacitor bank is given in Figure 49.

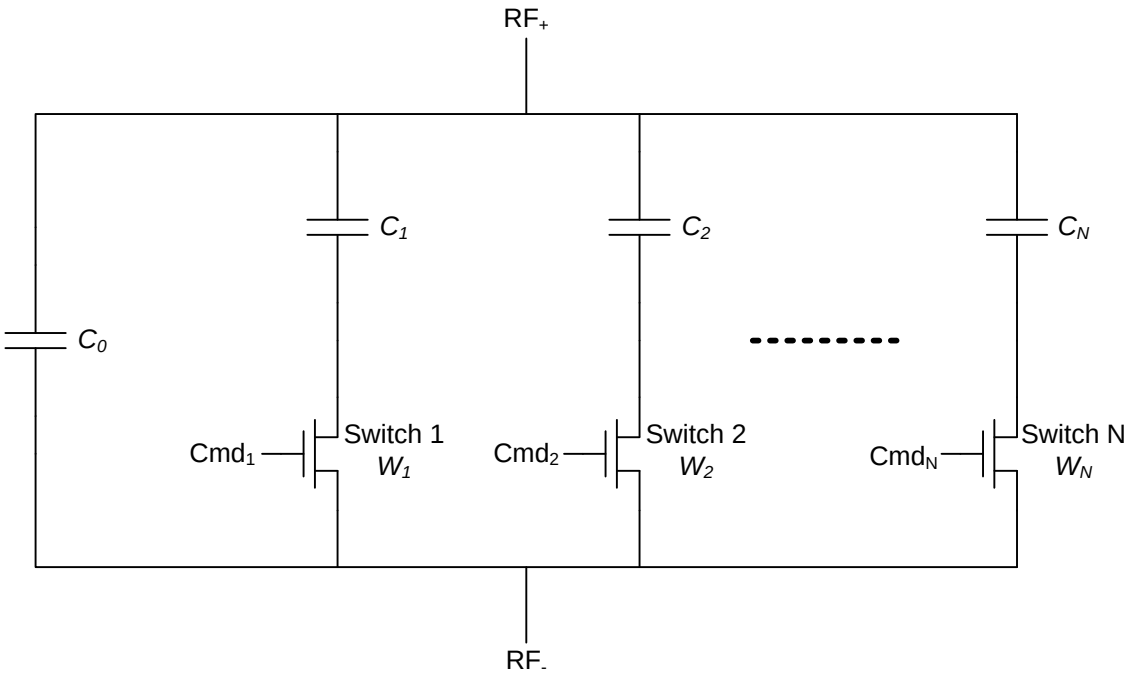

Figure 49: Schematic of a switched capacitor bank.

Equations 52 to 55 give the relation between the capacitance of each branch and their state – on or off – to obtain the equivalent capacitance.

$$C_0 + C_{1_{off}} + C_{2_{off}} + \cdots + C_{n_{off}} = C_{val_1} \quad \text{Equation 52}$$

$$C_0 + C_{1_{on}} + C_{2_{off}} + \cdots + C_{n_{off}} = C_{val_2} \quad \text{Equation 53}$$

$$C_0 + C_{1_{on}} + C_{2_{on}} + \cdots + C_{n_{off}} = C_{val_3} \quad \text{Equation 54}$$

$$\vdots$$

$$C_0 + C_{1_{on}} + C_{2_{on}} + \cdots + C_{n_{on}} = C_{val_m} \quad \text{Equation 55}$$

Those equations can be used to evaluate the capacitance step of each branch by calculating $C_{i\,on}$ - $C_{i\,off}$. The following equations show the application to 3 capacitance values.

$$C_{1_{on}} + C_{1_{off}} = C_{val_2} - C_{val_1} \quad \text{Equation 56}$$

$$C_{2_{on}} + C_{2_{off}} = C_{val_3} - C_{val_2} \quad \text{Equation 57}$$

We consider that the off-state capacitance $C_{i\,off}$ is a fraction of the on-state capacitance $C_{i\,on}$, see Equation 58.

$$C_{i_{off}} = k_{on/off} C_{i_{on}}$$ Equation 58

By setting $k_{on/off}$ as a tradeoff between expected interconnection parasitic and off-state capacitance of the MOS transistor, the capacitance of each branch can be determined as the following equations.

$$C_1 = \frac{C_{val_2} - C_{val_1}}{k_{on/off}}$$ Equation 59

$$C_2 = \frac{C_{val_3} - C_{val_2}}{k_{on/off}}$$ Equation 60

C_0 is then determined by subtracting C_1 and C_2 from the maximal capacitance, see Equation 61.

$$C_0 = C_{val_3} - C_1 - C_2$$ Equation 61

Once all the branches' capacitance values have been determined, each independent branch can be fully sized from the desired Q_{branch} using the methodology presented in the previous part. Another application that is worth studying is the binary weighted switched capacitor array.

The switched capacitor array should be able to withstand high power. When submitted to high power, the different branches may withstand high RF voltage (V_{RF}). While the switch is on, only the capacitor (C) withstands the full excursion of the RF voltage. The required number of capacitors in series (N_C) is obtained by considering the breakdown voltage ($V_{bk\,C}$) of each unity capacitor (C_u). Then, the capacitance values of each capacitor C_u must be multiplied by the number of capacitors to obtain the same overall capacitance C.

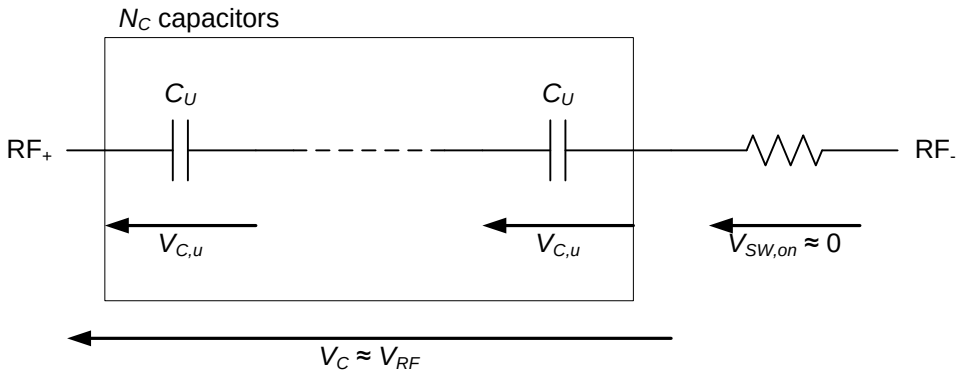

Figure 50:Voltage distribution across a capacitor branch in on-state

$$N_C = \frac{V_{RF}}{V_{bk_C}}$$ Equation 62

$$C_u = C \cdot N_C$$ Equation 63

In off-state, the voltage across a capacitor branch is split between *C* and the switch. Therefore, several MOS transistor must be stacked [Carrara09] to keep each MO transistor in safe operation ($V_{SW,u}<V_{bk\ MOS}$ where $V_{bk\ MOS}$ is the breakdown voltage of a MOS device).

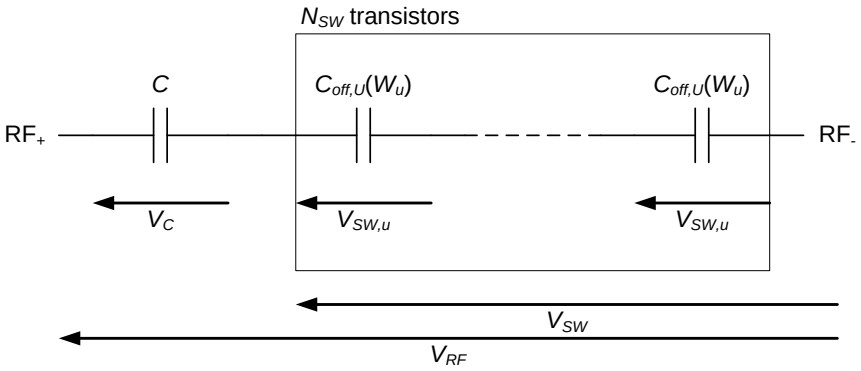

Figure 51:Voltage distribution across a capacitor branch in off-state

$$V_{SW} = V_{RF}\frac{C}{C + C_{off}} \qquad \text{Equation 64}$$

$$N_{SW} = \frac{V_{SW}}{V_{bk_{MOS}}} \qquad \text{Equation 65}$$

$$W_u = W_{SW} \cdot N_{SW} \qquad \text{Equation 66}$$

II-5 RF switch design

The single pole multiple throws (SPnT) devices is the basic RF device used to route the RF signal according to the mode and band of a MMPA [Scuderi08]. Figure 52 shows the simplified architecture of a SPnT.

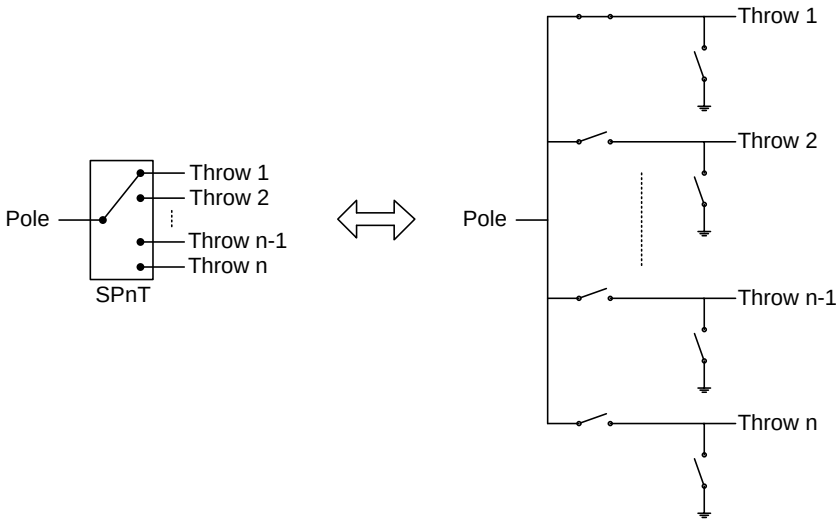

Figure 52: Example of a SPnT architecture

Main specifications of a SPnT are insertion losses (*IL*) and isolation (*Iso*).

II-5.1. SP1T

Both switches must be sized to ensure the required level of *IL* and *Iso*. *IL* is mainly governed by the design of the series switch while the combination of both switches ensures the *Iso*. The equivalent schematic of the elementary SP1T cell in on and off modes is given in Figure 53.

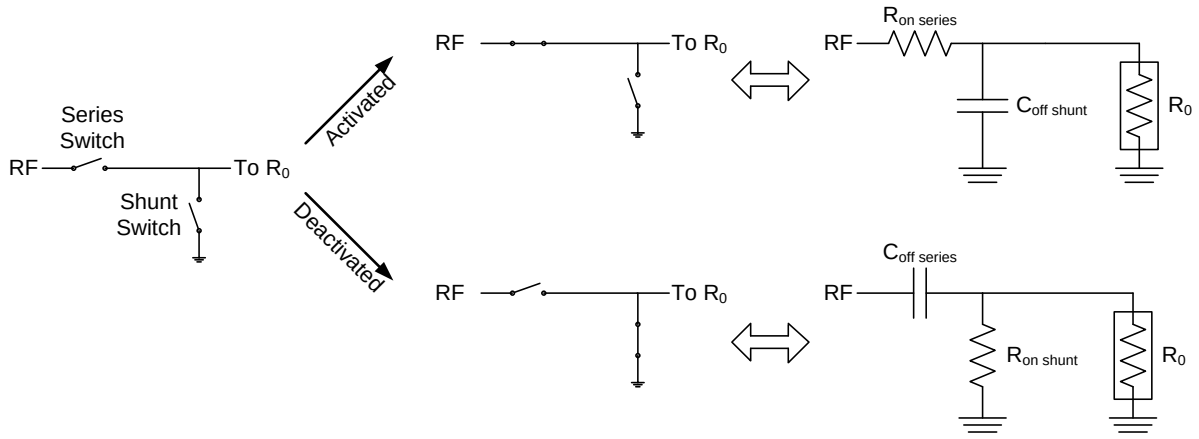

Figure 53: Equivalent schematics of the SP1T in "on" mode (upper) and "off" mode (bottom)

It is possible to express the insertion loss of the SP1T in "on" mode using Equation 67 [Huang01] which obtained by neglecting the influence on the off-state capacitance of the shunt switch ($C_{off\ shunt}$).

$$IL[dB] = 10\log\left[\left(1+\frac{R_{on_{series}}}{2R_0}\right)^2\right] \qquad \text{Equation 67}$$

This equation allows a first sizing of the series switch through the determination of the on-state resistance ($R_{on\ series}$).

Isolation may be expressed with Equation 68.

$$Iso[dB] = -10\log\left[\left(\frac{2R_{on_{shunt}}C_{off_{series}}\omega}{1+\frac{R_{on_{shunt}}}{R_0}}\right)^2 + \left(R_0 C_{off_{series}}\omega\right)^2\left(1+\frac{2R_{on_{series}}}{R_0}\right)\right] \qquad \text{Equation 68}$$

Using this formula, the width of the shunt switch (W_{shunt}) can be determined.

Insertion loss expression including the impact of $C_{off,\ shunt}$ is given by Equation 69 [Huang01].

$$IL[dB] = 10\log\left[\left(1+\frac{R_{on_{series}}}{2R_0}\right)^2 + \left(\frac{(R_0+R_{on_{series}})C_{off_{shunt}}\omega}{2}\right)^2\right] \qquad \text{Equation 69}$$

As an example, we study the design of a SP1T operating at **800MHz**. Targeted insertion losses are **0.25dB** and isolation **30dB**. From Equation 67, the calculated width of the series switch W_{series} is **340µm**. Similarly, the calculated width of the shunt switch W_{shunt} is **50µm**, obtained using Equation 68. Equation 69 is used to verify and adjust the W_{series} and W_{shunt}. This verification leads to

the same size for both switches. We conclude that in that case, the simplified previous equations are sufficient to size the SP1T. The frequency response of the designed SP1T is shown in Figure 54.

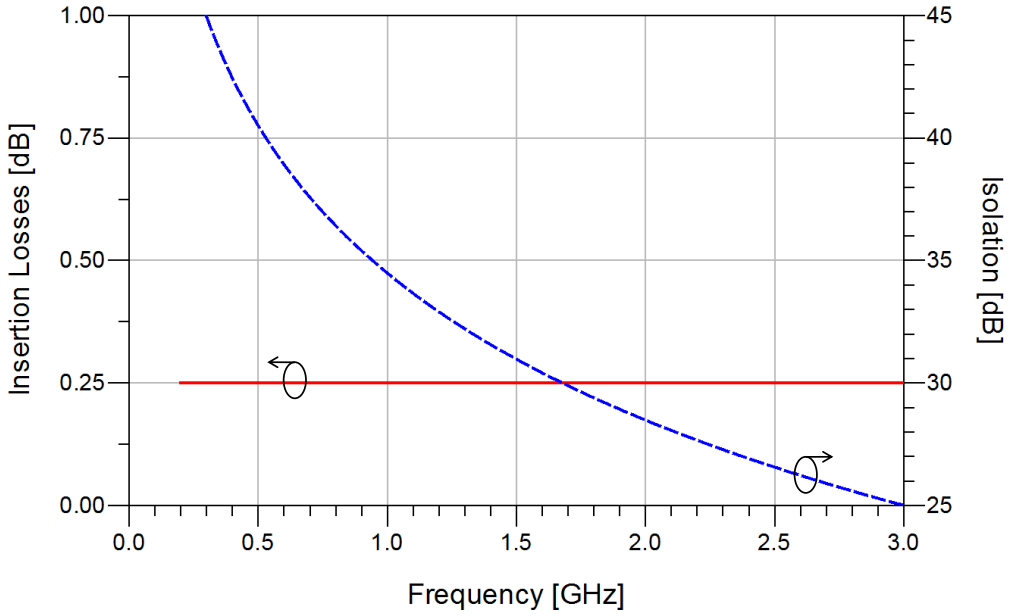

Figure 54: Insertion Loss and isolation of SP1T

II-5.2. SPnT

When building a SPnT, n SP1T structures are put in parallel while attaching the different poles together. In that case, the equivalent schematic for the activated throw and deactivated throws is different, see Figure 55.

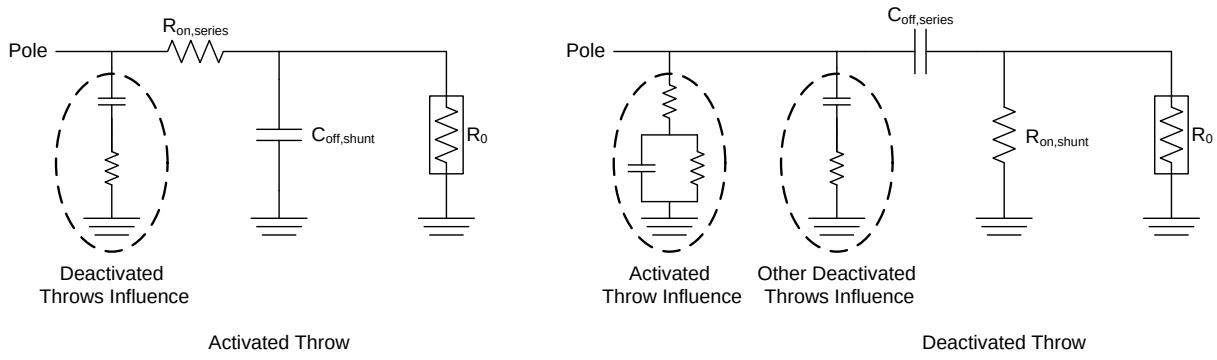

Figure 55: Equivalent schematics of the activated throw (left) and deactivated throws (right) of a SPnT

As can be seen on the figure, a parasitic network is added on the pole in both the activated and deactivated throws. These parasitic networks lead to an increase of insertion loss with the number of output path as shown in Figure 56.

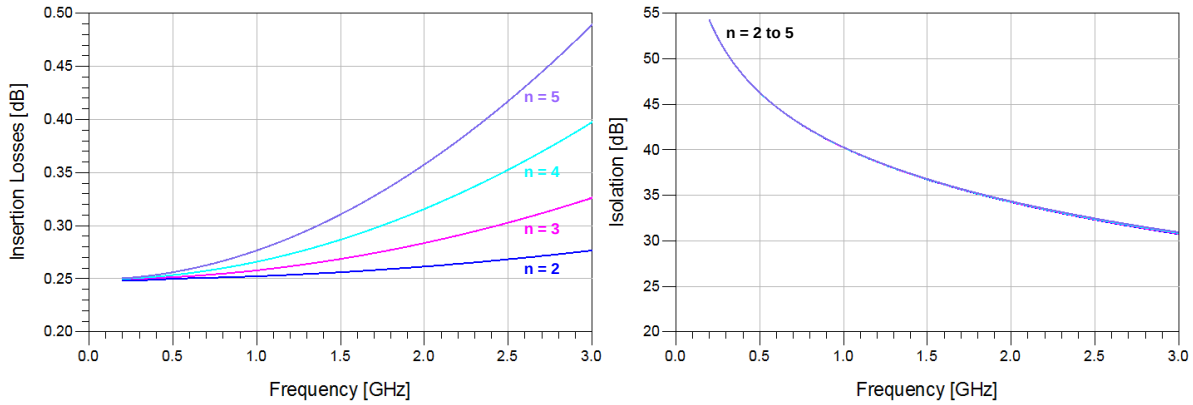

Figure 56: Insertion loss (left) and isolation (right) of a SPnT for n=2 to 5

II-6 Conclusion

In this chapter we reminded the characteristics that are specific to power amplifier design, including power performances as well as the linearity-efficiency trade-off. Methodologies have been described for saturated and linear power amplifiers design. Through the study of operating classes, LDMOS transistor pre-sizing for a specific application was described. Using load pull simulation, the pre-sizing can then be refined to maximize performances.

Matching networks constitute the second main part of power amplifier architectures. The design strategy for those circuits as implemented in this work was also described. By dividing the networks in unit L-Cells, full matching networks designed for specific bandwidth and insertion losses can be implemented.

In order to make the matching networks reconfigurable, the switched capacitor has been presented as a tunable component. Based on the quality factor and capacitance value requirements, two possible implementations can be done. A technique to ensure the capacitors can withstand high power levels was also presented.

A brief description of SPnT design was also proposed as this device is required for the architecture proposed in the following chapter. This part was kept simple while ensuring sufficient needed performance for the circuits developed in this work.

All those definitions and building blocks constitute the backbone of the architectures presented in Chapter 3 and Chapter 4. The next chapter deals with the application of those methods for reconfigurable power amplifier design.

II-7 References

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Chapter III: Reconfigurable Multi-Mode Multi-Band Power Amplifier Design

III-1 Introduction

Reconfigurable PA architectures are the best solutions to increase the integration level and reduce the cost of multimode multiband power amplifiers (MMPA). In this chapter, a new reconfigurable MMPA architecture is proposed and implemented in SOI CMOS technology.

The architecture of the reconfigurable MMPA is first presented, as well as the strategy used to handle multiple modes and frequency bands. The power output stage is the major contributor to the large signal PA performances together with the output matching network. The power stage uses LDMOS transistor sizing to handle the power requirements in saturated and linear modes. The tunable output matching network is optimized to realize optimal matching in the targeted frequency bands.

Assembling the driver and output stage has an impact on the overall PA performance. Anticipating the degradation in terms of efficiency helps setting the requirements for the driver stage, inter-stage matching network and input matching network. A trade-off is chosen to limit the overall performance degradation associated to the driver stage. Afterwards, the input matching network is designed to ensure a maximal power transfer to the driver's input in every mode.

The design of the inter-stage matching consists in choosing the adequate topology that can realize optimal inter-stage matching. The focus during this design step is to ensure that optimal source impedance is presented to the power stage, thus avoiding performance degradation. A trade-off for the value of load impedance of the driver stage is then found to ensure correct overall performance.

In order to operate properly in linear mode, the architecture requires an adequate biasing strategy. A bias circuit limiting memory effects is proposed. Source harmonic termination is combined with the bias circuit to reach a more compact design.

Finally, the performance of the proposed reconfigurable PA architecture is assessed through measurement and compared with the state of the art.

III-2 Reconfigurable MMPA architecture

The objective of this work is to design a single PA line-up that can be used for 2G/3G/4G standards in low E-UTRA frequency bands ranging from 700MHz to 920MHz. Two problems are to be considered: the reconfiguration in mode and the reconfiguration in band.

The reconfiguration in mode impacts both the design of the active elements and the matching networks. The active elements must be sized adequately for the various power, linearity and efficiency performances in every mode. Concerning matching networks, the main impact comes from the different impedances that must be presented to the load and source of the stages for the different modes.

The frequency reconfiguration mainly impacts the matching networks. The matching networks therefore need to provide the correct impedances at the various frequency bands.

The targeted performance for the proposed reconfigurable PA line-up is given in Table 24.

Table 24: Targeted performance in each mode.

Mode	Output Power	ACPR	PAE
2G	35dBm	-	>50%
3G	28.5dBm	-40dBc	>40%
4G	28.5dBm	-35dBc	>35%

The power stage requires proper resizing in order to handle the two different power levels between 2G and 3G/4G operation. Linearity and efficiency in each mode are mainly optimized through matching. To achieve power gain higher than **25dB** at least 2 stages are required. A block schematic of the proposed architecture is presented in Figure 57 in which all the blocks are reconfigurable.

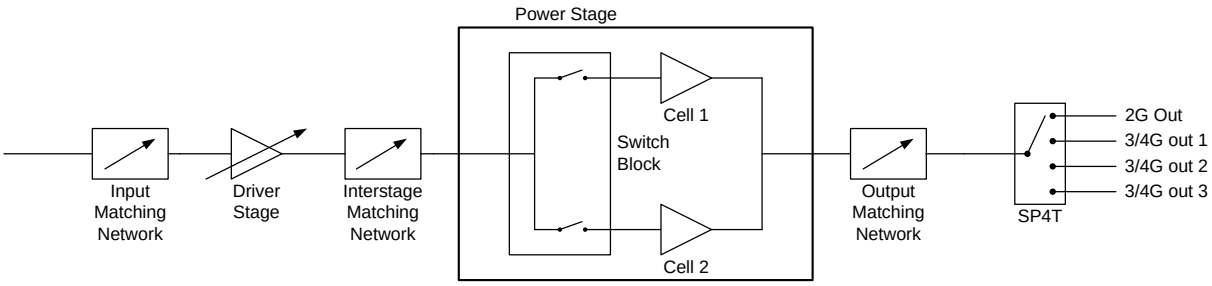


Figure 57: Block schematic of the reconfigurable MMPA.

Several strategies can be adopted to address the different E-UTRA frequency bands located between **700MHz** and **920MHz**.

The networks can be designed as a wide band network to cover the full macro-band without reconfiguration [Pornpromlikit10]. However, such wideband networks add a high level of loss and complexity, due to the number of required cells. Furthermore, performances are degraded around the edges of the frequency band where the impedances viewed by the stages become different from the nominal value. The wideband solution is therefore not the optimal solution.

Another approach consists in designing the networks for narrow band operation at a specified band [Ali10]. This strategy can provide a good selectivity inside a given band but requires wide range of reconfiguration values to cover the whole frequency range. Another disadvantage of this solution lies in the narrow bandwidth, needing a very high Q-Factor for the network (Q_{Net})

leading to higher insertion loss, as shown in Equation 70. The components' quality factor (Q_{Comp}) is lowered with the increase of the reconfiguration range for each component.

$$IL = 10\log\left(1 - \frac{Q_{Net}}{Q_{Comp}}\right) \qquad \text{Equation 70}$$

An intermediate solution consists in grouping all the FDD bands of the considered frequency range in a limited number of frequency bands, each being addressed by one network configuration. The number of reconfiguration states is limited as the bandwidth of each network. Figure 58 depicts one possible frequency band splitting in 3 bands: **700MHz**, **800MHz** and **900MHz**.

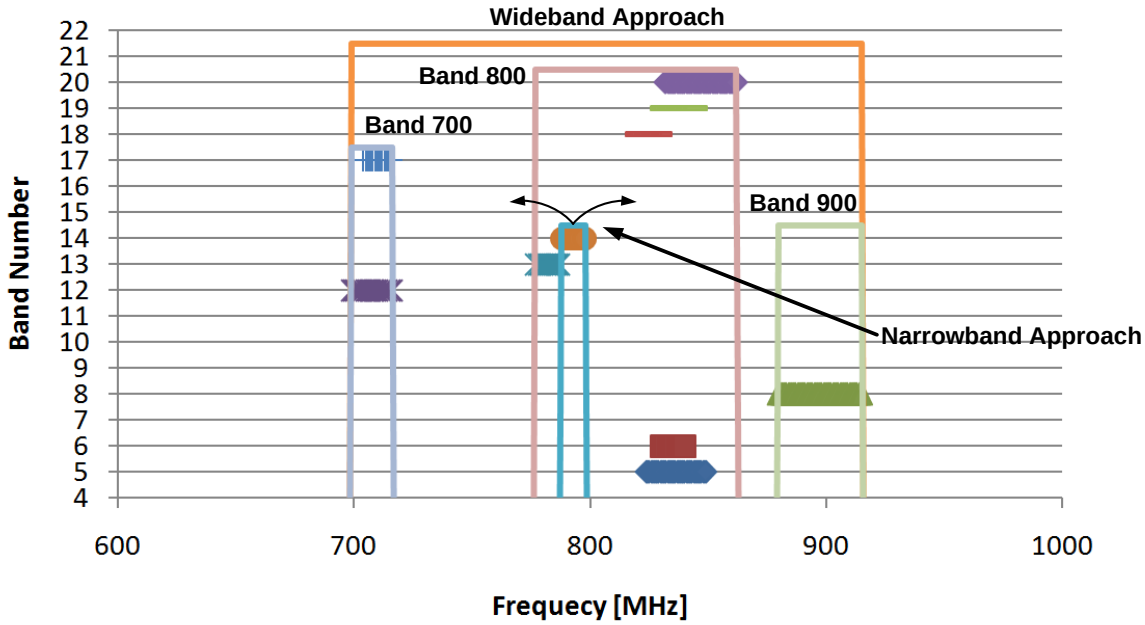


Figure 58: Macro-band division.

Due to the frequency division in 3 bands, the PA has three distinct outputs for 3G/4G mode as shown on Figure 57. FEM architecture requires a dedicated path for 2G operation [Kim14]. Hereafter, the design of blocks of the MMPA architecture is presented.

III-3 Reconfigurable MMPA design

First, the global MMPA specifications are translated into specifications for the output matching network (OMN) and power stage. Afterwards, the specifications for the inter-stage matching network (IntMN), the driver stage and the input matching network (IMN) are deduced from the performance of the output stage.

III-3.1. Reconfigurable power stage design

The reconfigurable PA has to cover the low E-UTRA frequency bands ranging from 700MHz to 920MHz for 2G, 3G and 4G modes. Table 25 shows the specifications for the power stage based on the MMPA specifications and OMN insertion losses (IL_{OMN}).

Table 25: Required performances of the power stage in each mode.

Mode	P_{out}	ACPR	PAE	IL_{OMN}
2G	36dBm	-	>50%	0.5dB
3G	29dBm	-40dBc	>40%	
4G	29dBm	-35dBc	>40%	

By referring to Chapter 2, the optimal operating class and size of the power stage can be determined for each mode. For 2G mode, saturated operation is best suited and as seen in Chapter 2 optimal class is Class-F^{-1} and the corresponding LDMOS transistor size is **26mm** under **3.3V** supply voltage.

For 3G and 4G modes, linear operation is required to ensure optimal *ACPR* performance and as seen also in Chapter 2, Class F provides an optimized tradeoff between efficiency and linearity. The optimal LDMOS transistor size in this mode is **20mm**.

The required LDMOS transistor size being different in each mode, the power stage is chosen to be reconfigurable. Two cells are implemented with a SP2T switching device allowing selection of one cell or both [Yin14]. In order to balance the RF signal between the two cells, we choose to slightly oversize the power cell for the saturated mode to **40mm** in order to have two identical LDMOS transistor cells. Figure 59 depicts the structure of the power cell.

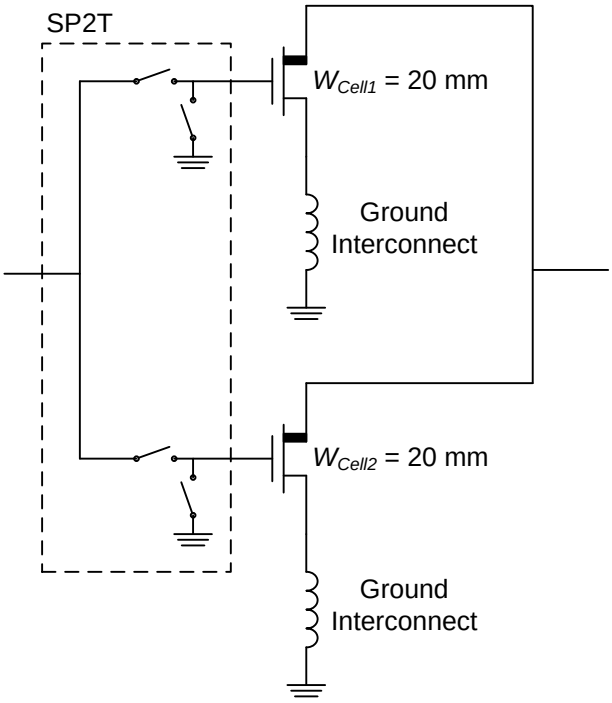


Figure 59: Reconfigurable power stage.

By switching the LDMOS transistor size, the power stage can handle the power requirements for both saturated and linear operation. The next constraint for the power stage is the frequency band reconfiguration. Using the method from Chapter 2, optimal load and source impedances are first determined through calculation for the different frequency bands and optimized through load-pull and source-pull simulations. Figure 60 shows the calculated and simulated optimal load impedance ($G_{L\,opt}$) for both saturated mode and linear mode as a function of the operating frequency.

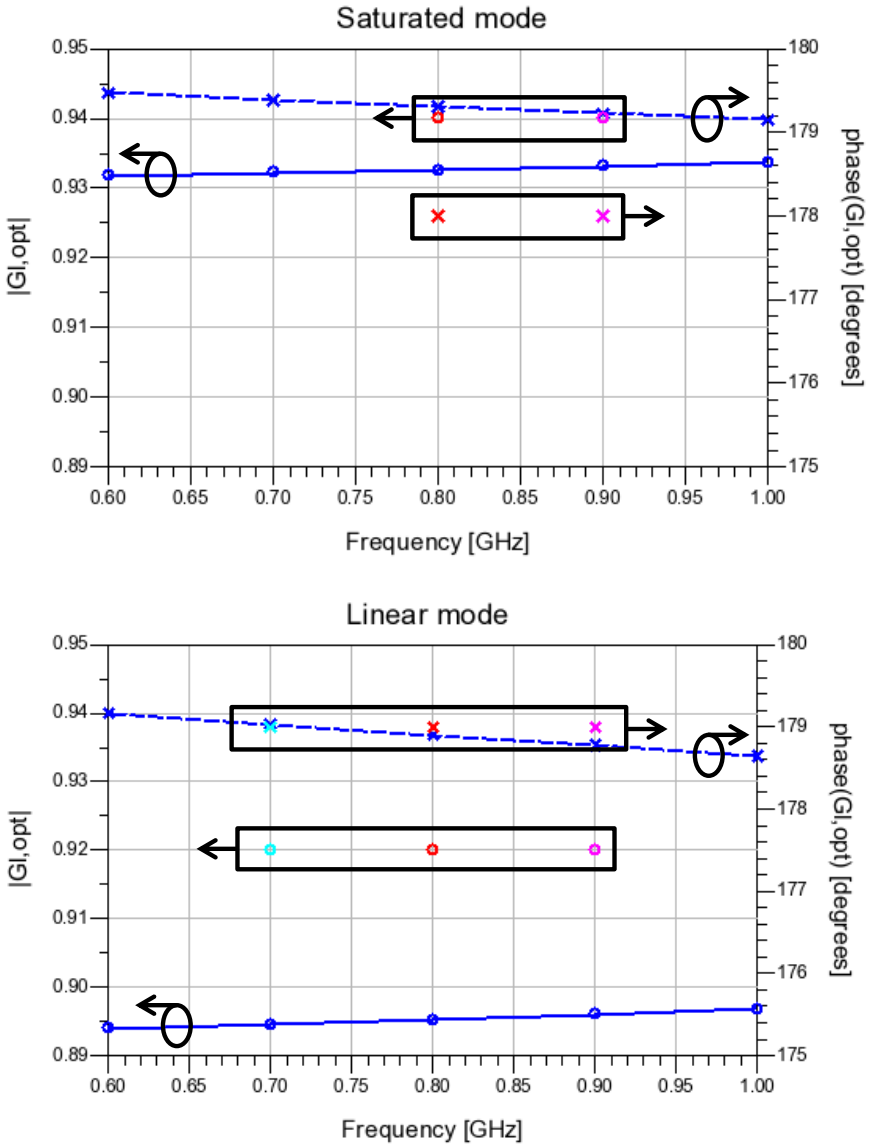


Figure 60: Simulated optimal load impedance versus frequency in saturated mode (top) and linear mode (bottom).

The solid line shows the magnitude of $G_{L\,opt}$ whereas the dashed lines show the phase of $G_{L\,opt}$ in degrees. The graphs show that the variation of $G_{L\,opt}$ versus frequency is limited so that we can consider a constant $G_{L\,opt}$ from **700MHz** to **900MHz** without PA performance degradation.

The transition between each mode is realized using a SP2T. The design of the SP2T is critical as it can deeply impact the performance of the power stage. The series switch is designed to provide minimal insertion loss (<**0.05dB**) while the parallel switch provides **30dB** isolation between the two cells.

Switch sizes in such configuration are **4.5mm** for the series switch and **0.5mm** for the shunt switch.

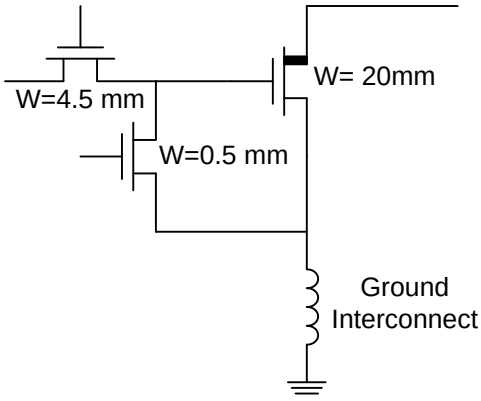


Figure 61: Power cell with input switch.

Due to the specific implementation of the power stage, the optimal impedances at the source and load must be adjusted in order to compensate the gate, drain and source interconnections of the LDMOS transistor. Figure 62 shows the networks including the parasitic of interconnections at the input and output of the cell in saturated mode.

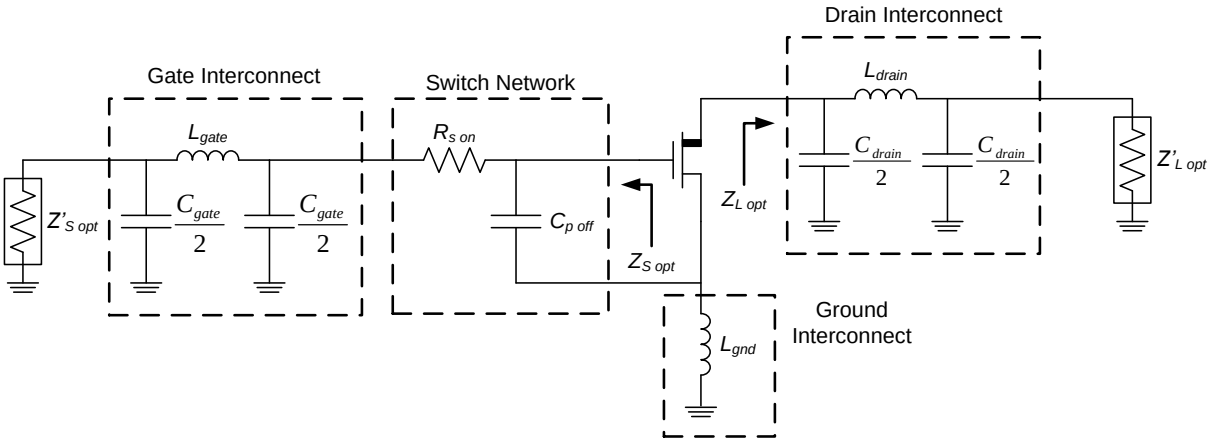


Figure 62: Equivalent interconnection network of the power cell in saturated mode.

The source and load impedances ($Z'_{S\,opt}$ and $Z'_{L\,opt}$ respectively) must be tuned in order to obtain the optimal load and source impedances in the reference planes of the LDMOS transistor ($Z_{S\,opt}$ and $Z_{L\,opt}$ respectively).

In linear mode, the interconnection network is more complex since the off-state cell brings additional parasitic. The equivalent interconnect network viewed by the active cell is depicted in Figure 63.

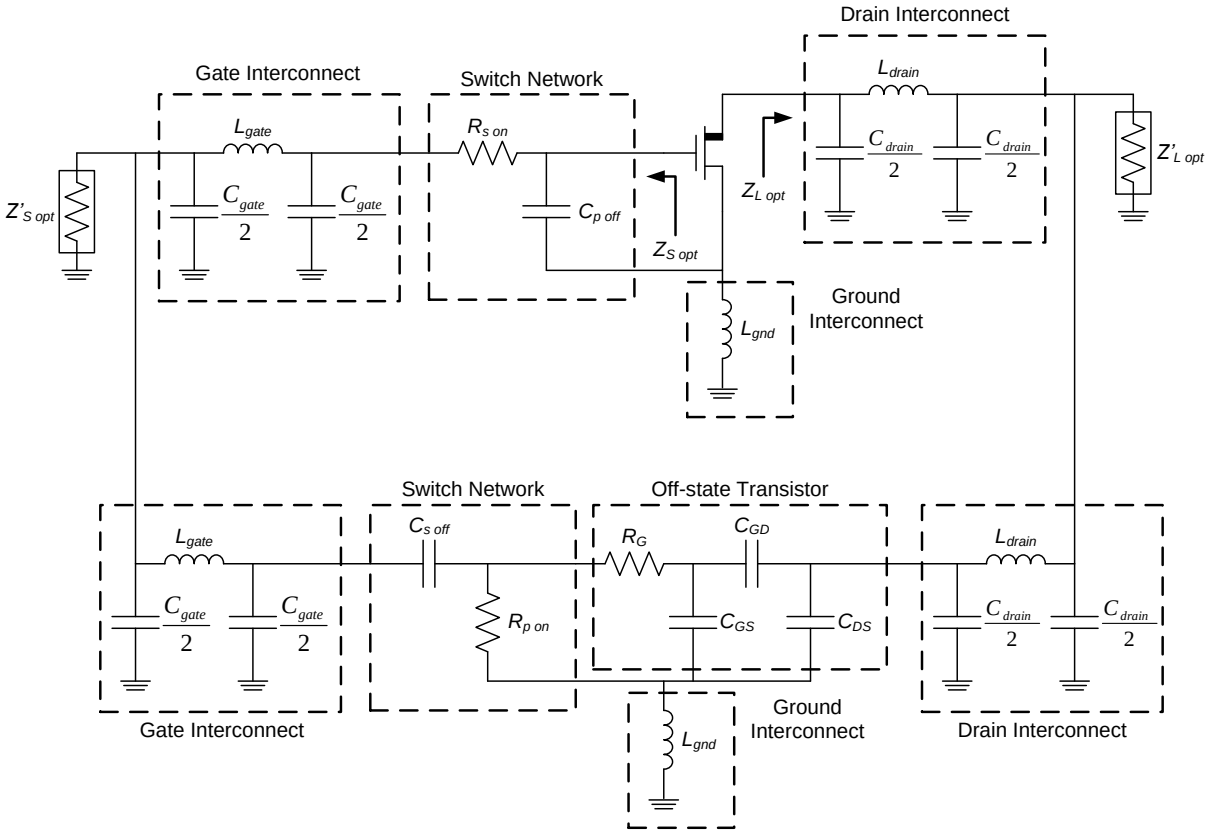


Figure 63: Equivalent interconnection network of the power cell in linear mode.

The power stage has been simulated in large signal, with a CW signal and a W-CDMA Release'99 test signal for saturated and linear mode respectively after source and load tuning. Figure 64 and 9 show the performance of the power cell at **800MHz** in saturated and linear mode respectively.

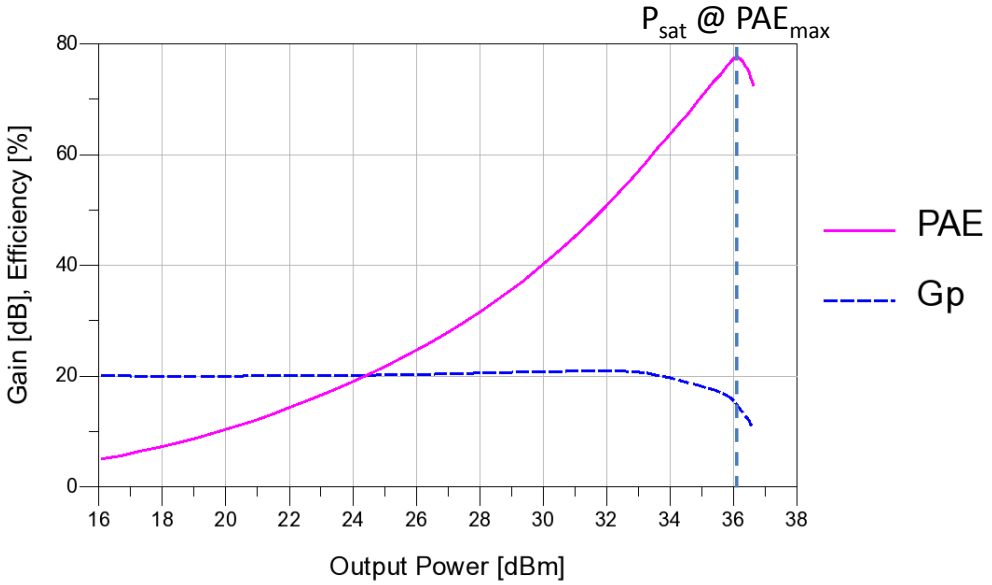


Figure 64: Simulated PAE and power gain of the power cell in saturated mode.

In saturated mode, a maximum efficiency of **78%** is obtained for a saturated power (P_{sat}) of **36dBm**.

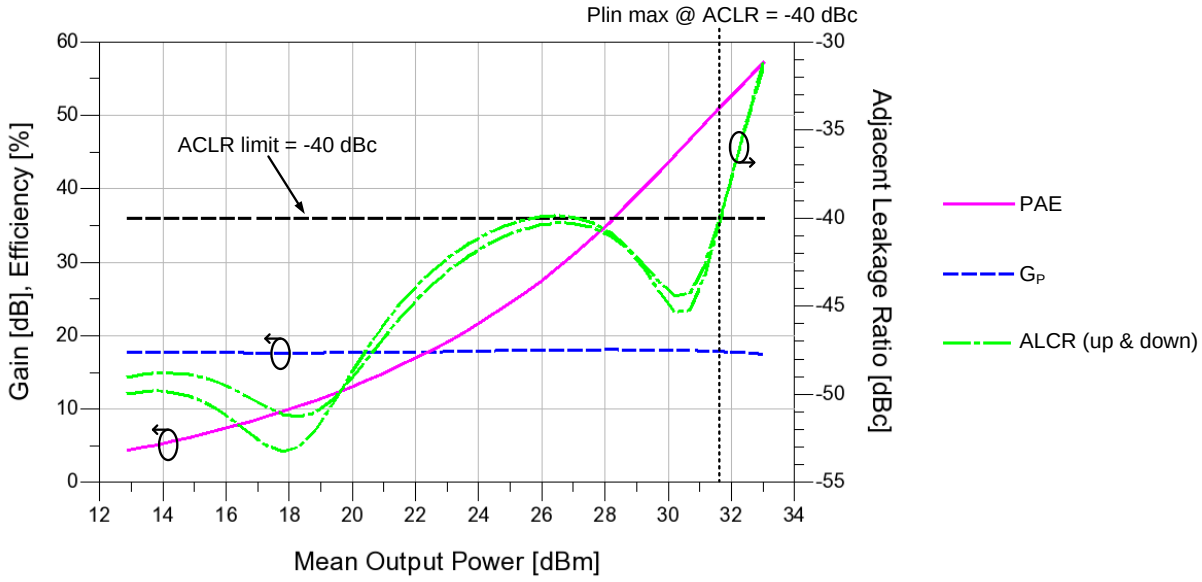


Figure 65: Simulated PAE and power gain (left) ACPR (right) of the power cell in linear mode.

In linear mode, an efficiency of **51%** is obtained for a linear power of **31.6dBm** (ACPR = **-40dBc**). Table 26 summarizes the simulated performances of the power stage for the different modes and frequency bands.

Table 26: Simulated performance of the power stage in saturated and linear modes

Mode	Band	P_{sat} / P_{lin}	PAE	G_p
Saturated	**GSM-800**	36.3dBm	78%	15.2dB
	GSM-900	36.4dBm	77%	13.4dB
Linear	**700MHz**	31.6dBm	49%	19.9dB
	800MHz	31.6dBm	51%	17.9dB
	900MHz	31.6dBm	52%	16.4dB

III-3.2. Reconfigurable output matching network design

The reconfigurable output matching network (OMN) allows adjusting the load impedance of the power cell for the different modes and frequency bands.

A. Network topology

The output matching network is used to transform the **50Ω**load termination into the optimal load impedance for the different modes and frequency bands with the required performance summarized in Table 27, where Q_{BW} is defined as Equation 71.

$$Q_{BW} = \frac{f_0}{BW} \qquad \text{Equation 71}$$

Table 27: required Q-Factor as a function of the frequency band.

Band	Band 700	Band 800	Band 900
Bandwidth (*BW*)	17MHz	85MHz	35MHz
f_0	707.5MHz	819.5MHz	897.5MHz
Q_{BW}	42	10	26

In order to realize matching, we first need to calculate the transformation Q-Factor ($Q_{Transfo\ OMN}$) defined as follows in Equation 72.

$$Q_{Transfo_{OMN}} = \sqrt{\frac{50}{R_{L_{opt}}} - 1} \qquad \text{Equation 72}$$

In order to meet both the frequency and IL requirements, $Q_{Transfo\ OMN}$ should be lower than the desired Q_{BW} and Insertion Loss Q-Factor (Q_{IL}). The number of cells in the network is chosen to verify this condition. The optimal load impedances are given in Table 28.

Table 28: Optimal load impedance in saturated and linear modes.

Mode	Saturated	Linear
$R_{L\ opt}$	2.1Ω	2.9Ω
$Q_{Transfo\ OMN}$	4.78	4.03

In our case, the maximum $Q_{Transfo\ OMN}$ (**4.78**) is lower than the lowest Q_{BW} (10). In this case, 1 cell is sufficient to meet the frequency requirements.

Q_{IL} is determined from the desired insertion loss (*IL*) and the minimum components Q-Factor (Q_{Comp}) with Equation 68.

$$Q_{IL} = Q_{Comp}\left(1 - 10^{\frac{-IL[dB]}{20}}\right) \qquad \text{Equation 73}$$

By considering Q_{Comp} targeted *IL*are**40** and is **0.5dB respectively**, Q_{IL} is equal to **2.23**. Since $Q_{Transfo\ OMN}$ is higher than Q_{IL}, one cell is not sufficient to meet the requirements. By adding a second cell, $Q_{Transfo\ OMN}$ is reduced to **2.2**, thus meeting both frequency and loss requirements.

The chosen network structure is shown in Figure 66

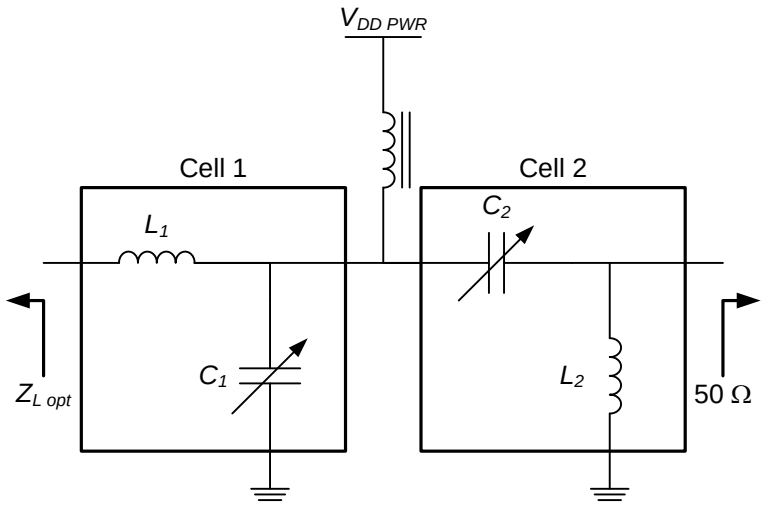


Figure 66: output matching network architecture

This topology takes advantage of the series capacitor C_2 to block the DC signal while providing the supply voltage $V_{DD\ PWR}$ to the power stage through a choke inductor connected between the two cells of the network. The component values required to address every mode of the network are given in Table 29.

Table 29: Component values of the output matching network

Mode	C_1	C_2	L_1	L_2
Lin-700	32.8pF	11.1pF	1.2nH	6.2nH
Lin-800	28.7pF	9.7pF	1nH	5.5nH
Lin-900	25.5pF	8.6pF	0.9nH	4.9nH
Sat-800	39.0pF	10.0pF	0.8nH	4.8nH
Sat-900	34.7pF	9.0pF	0.7nH	4.3nH

The network has to be reconfigurable to address the different modes and frequency bands with the same network topology. Inductors are set to fixed values giving a trade-off between the optimal load impedances in the different modes. After optimization, L_1 is set to **1.1nH** and L_2 to **5.5nH**.

The reconfiguration function of the network is provided tunable capacitors [Park14]. The corresponding for each values mode and frequency band are shown in Table 30.

Table 30: Capacitor values.

Capacitor	Lin-700	Lin-800	Lin-900	Sat-800	Sat-900
C_1	36pF	29.7pF	25.5pF	39.0pF	31pF
C_2	11.5pF	9.7pF	8.6pF	14.0pF	12pF

To check the validity of the topology, a preliminary S-Parameters simulation is done to verify the matching in every configuration. The inductor Q-Factor (Q_L) is set to **40** and the tunable capacitor Q-Factor (Q_C) is set to **80**.

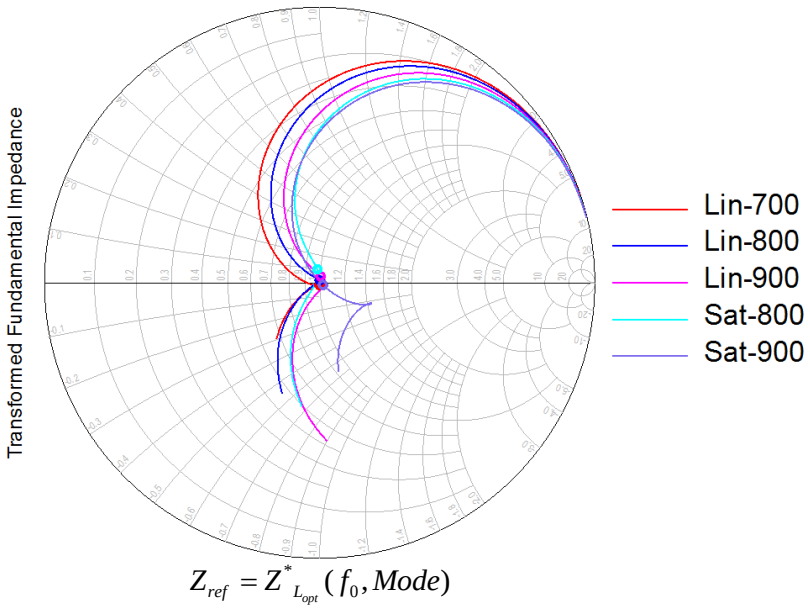


Figure 67: Simulated input impedance of the output matching network normalized by the optimal load impedance in each mode and band (Z_{ref}).

For all modes and bands, the matching is correctly realized as shown in Figure 67.

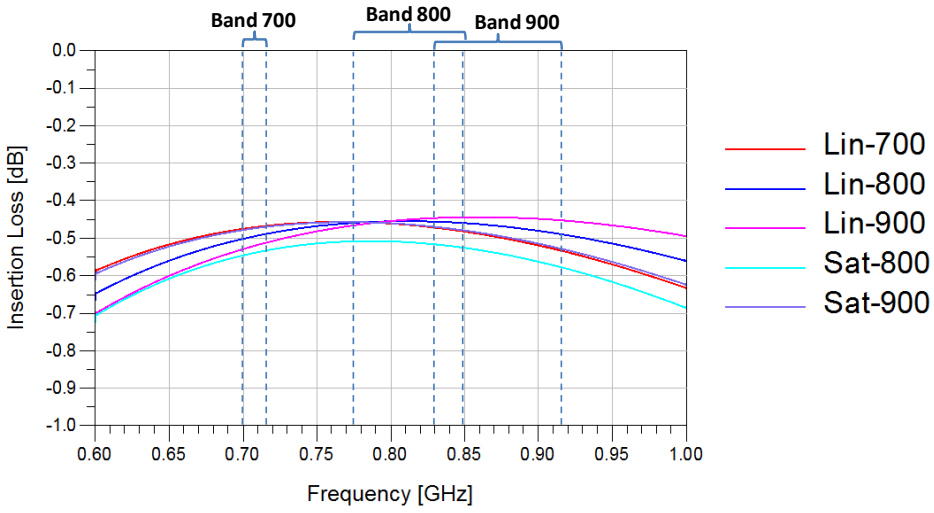


Figure 68: Simulated insertion loss of the output matching network as a function of frequency

The simulated insertion loss of the output network is presented in Figure 68, showing insertion loss between **-0.4dB** and **-0.5dB** in the frequency range of interest.

B. Harmonic termination

In **Error! Reference source not found.**, optimal load impedances at harmonic frequencies ere determined to improve the large signal performance of the power stage. A harmonic termination can be realized to obtain the correct phase of load impedance, as shown in Figure 69.

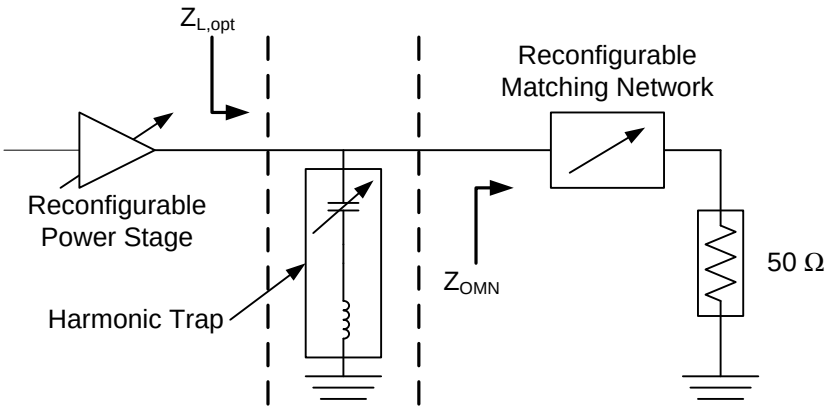


Figure 69: Harmonic termination using a series LC resonator

The harmonic trap is the main element used to realize the matching at the second harmonic. The optimal impedance at the second harmonic $Z_{L\,opt}$ ($2f0$) is obtained as shown in Equation 74.

$$Z_{L_{opt}}(2f_0) = \frac{Z_{OMN}(2f_0) \cdot Z_{trap_{H2}}(2f_0)}{Z_{OMN}(2f_0) + Z_{trap_{H2}}(2f_0)} \qquad \text{Equation 74}$$

In order to efficiently terminate the 2nd harmonic for each mode and frequency band, we determine an initial value for the trap capacitance and inductance. The trap is equivalent to a shunt capacitor at the fundamental frequency f_0 and must present a high impedance at $f_0 = f_{res}/2$. By considering the trap impedance is ten times higher than the optimal load at f_0, we can calculate an initial value for the capacitance C_{trap} using Equation 75; see Appendix E for detailed calculation.

$$C_{trap} = \frac{3}{80 \cdot \pi \cdot f_0 \cdot \left|Z_{L_{opt}}(f_0)\right|} \qquad \text{Equation 75}$$

The calculated trap capacitance is **4pF**. The trap inductance is then determined to provide series resonance at $2f_0$, using Equation 76.

$$L_{trap} = \frac{1}{C_{trap} \cdot (2\pi f_0)^2} \qquad \text{Equation 76}$$

The inductance for this trap is **2.2nH**. The response of the matching network combined to the trap is then simulated. The insertion loss of the network is presented in Figure 70 and the impedances presented by the network in Figure 71 with Q_C = **80** and Q_L = **40**.

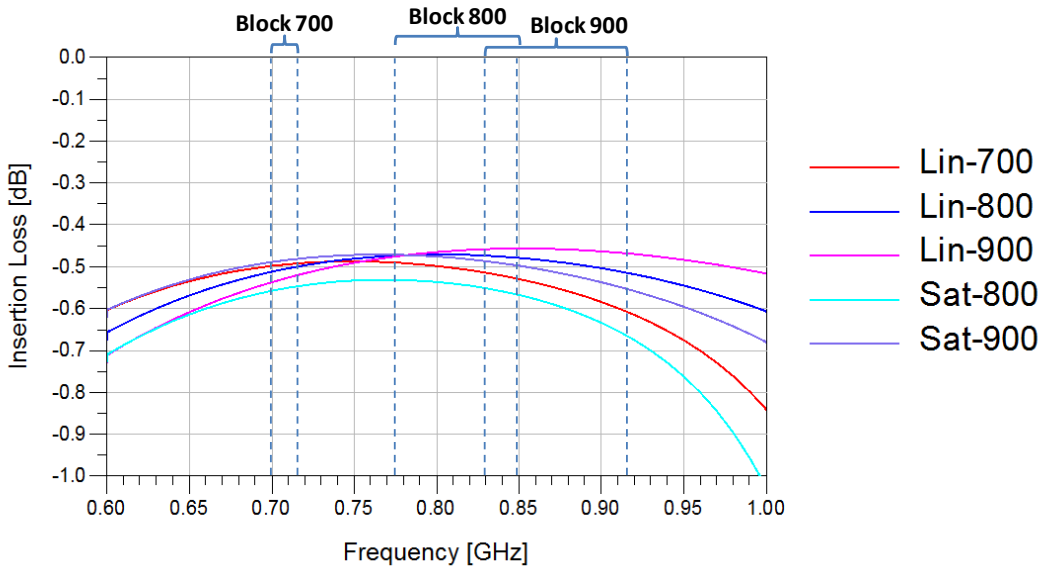


Figure 70:Insertion Losses of the matching network combined with the 2nd harmonic trap

The impact of the trap on the insertion loss is limited: the losses are kept between **-0.47dB** and **-0.57dB**.

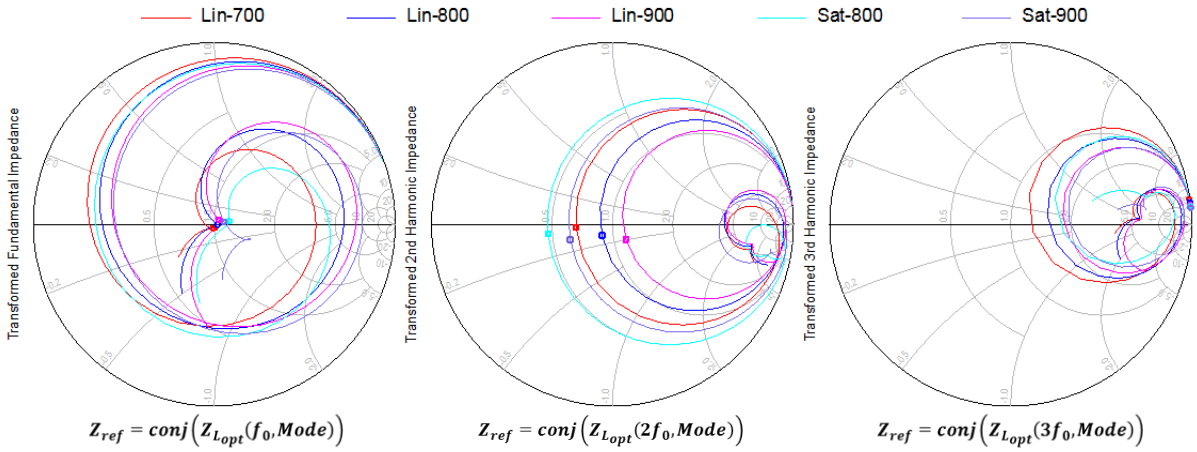


Figure 71: Simulated impedance presented to the power stage by the output matching network and harmonic trap at the fundamental, 2nd harmonic and 3rd harmonic frequencies normalized by the optimal load impedance in each mode, band and harmonic (Z_{ref}).

The left chart shows the load impedance normalized by the optimal load impedance at the fundamental frequency while the central and right charts show the load impedance at the second harmonic and the third harmonic respectively. As can be seen on the graphs, optimal load impedance at the2nd harmonic is correctly generated as the marks are located near the center of the central chart, while impedance matching at f_0 is preserved. Matching at the 3rd harmonic is not optimal. The following study shows the impact of an additional harmonic trap at $3f_0$, by comparing the power stage performances with and without such harmonic termination.

The simulated performances of the power stage for a Rel99 modulated signal are given in Figure 72.

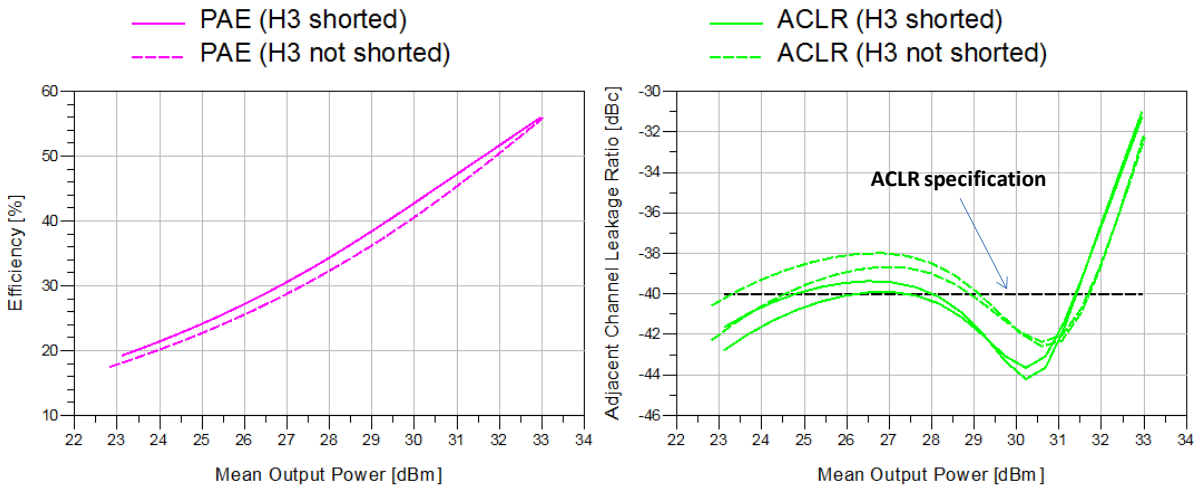


Figure 72: Efficiency (left) and ACPR (right) responses of the power stage for a Release'99 signal at 800MHz with and without harmonic trap at the 3rd harmonic

At **31.5dBm** output power, efficiency is **50%** with optimal 3rd harmonic termination and **48%** without optimal 3rd harmonic termination. This efficiency benefit is justifies the use of a third harmonic termination, under the condition that the insertion loss does not increase. The two options will now be compared in terms of network insertion loss. The schematic of the full matching network including the 3rd harmonic termination is given in Figure 73.

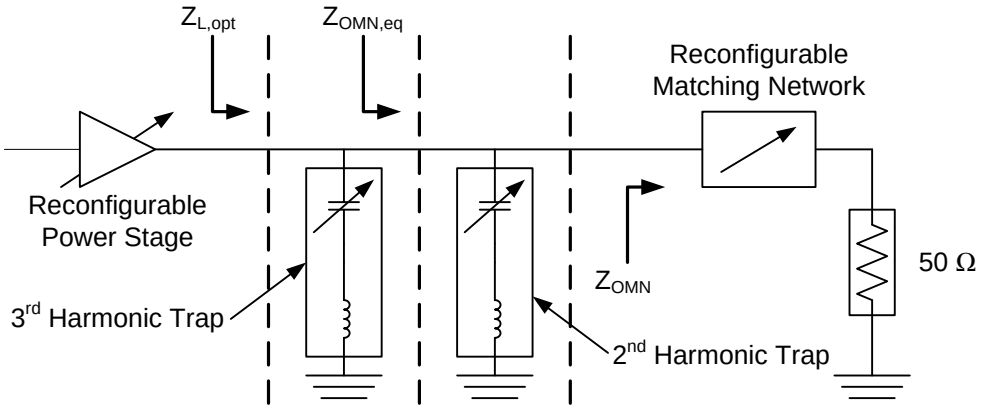


Figure 73: 3rd harmonic termination using a second series LC resonator

To design the 3rd harmonic termination, we use the same approach as before. After adjustments of the fundamental and 2nd harmonic networks to compensate the impact of the 3rd harmonic trap, the S-parameters of the full matching network are simulated. Matching and insertion loss for the different modes and bands are shown in Figure 74 and Figure 75 with Q_C = **80** and Q_L = **40**.

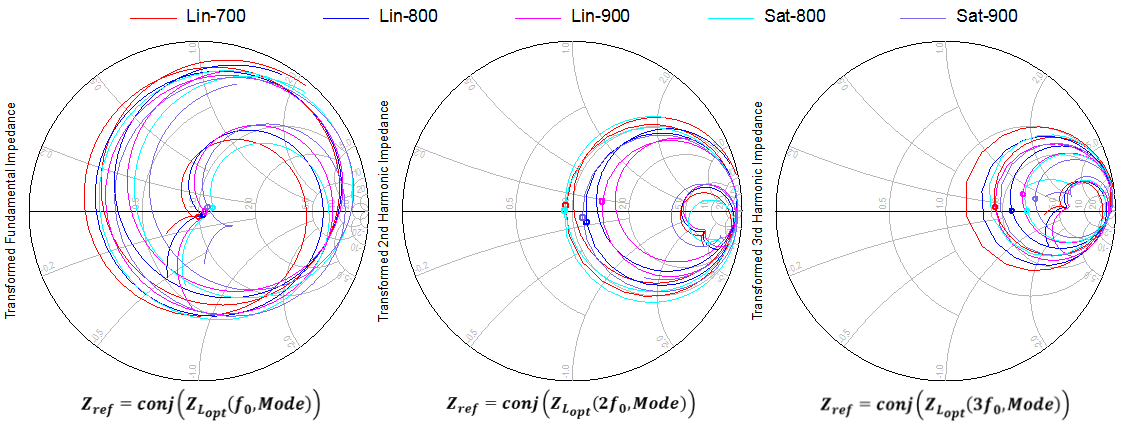


Figure 74: Impedance presented to the power stage by the output matching network and harmonic traps at the fundamental, 2nd harmonic and 3rd harmonic frequencies

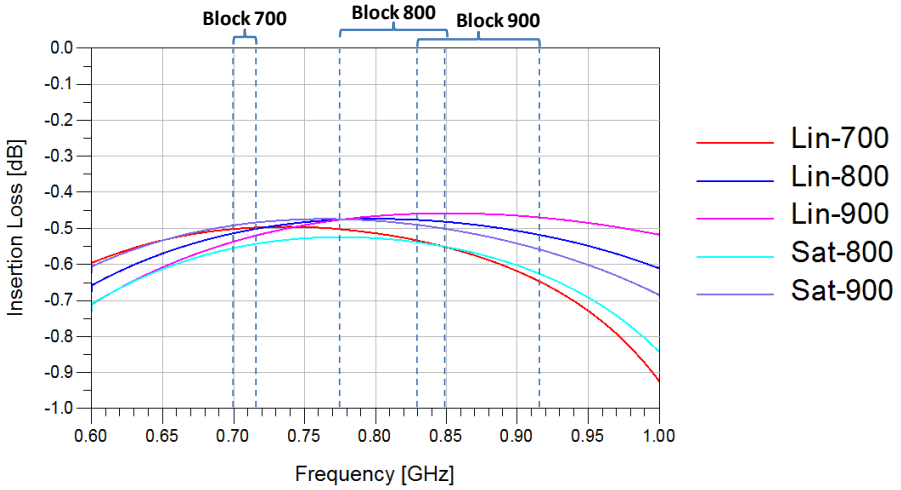


Figure 75: Insertion losses of the OMN combined with the 2nd and 3rd harmonic traps

As can be seen in Figure 74, proper impedance matching is obtained at f_0 (left), $2f_0$ (center) and $3f_0$ (right). Insertion loss with the addition of a 3rd harmonic trap are ranging from **-0.5dB** to **-0.6dB**. . A summary of the simulated performances of the output assembly, combining the power stage (PWR), the output matching network (OMN) and harmonic traps at $2f_0$ and $3f_0$, is given in Table 31.

Table 31: Simulated performance in saturated and linear mode

Mode	Band	P_{sat} / $P_{lin,max}$	PAE	G_p	IL_{OMN}
Saturated	GSM800	35.4dBm	71%	12.6dB	-0.6dB
	GSM900	35.4dBm	69%	12.3dB	-0.6dB
Linear	700MHz	30.7dBm	41%	18.5dB	-0.5dB
	800MHz	30.4dBm	41%	17.1dB	-0.5dB
	900MHz	30.4dBm	42%	15.8dB	-0.5dB

In saturated mode, the assembly can deliver **35.5dBm** of output power with efficiency higher than **69%**. In linear mode, linear output power is higher than **30.4dBm** with more than **41%**efficiency.

C. Mode and band switch

Following the methodology presented in Chapter 2, a SP4T is designed with targeted insertion loss and isolation of 0.2dB and 30dB respectively for the different modes and frequency bands. A schematic of the SP4T is given in Figure 76.

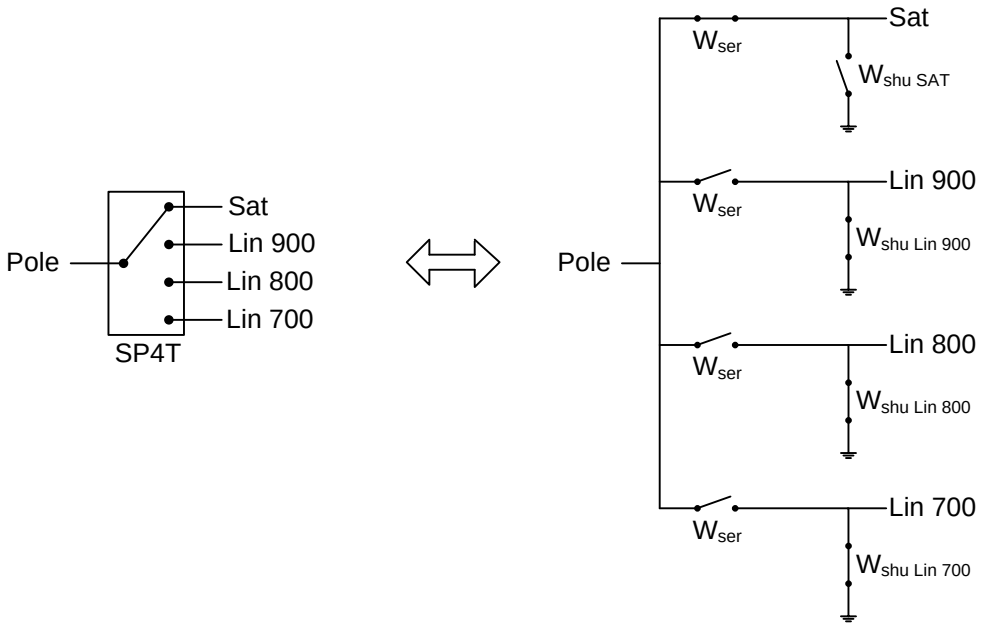


Figure 76: Schematic of the SP4T at the output of the reconfigurable power amplifier

Each path is dedicated to one mode and frequency, except for the saturated mode where a single path is used for both frequency bands. The different switches are sized to obtain the desired insertion losses and isolation. Sizes of the different series switches (W_{ser}) are identical. The sizes of the switches are given in Table 32.

Table 32: Switches sizes of the SP4T

Switch	**W_{ser}**	**$W_{shu\ Sat}$**	**$W_{shu\ Lin\ 900}$**	**$W_{shu\ Lin\ 800}$**	**$W_{shu\ Lin\ 700}$**
Width	700 µm	80 µm	70 µm	50 µm	25 µm

The SP4T presents insertion loss lower than **0.2dB** for the different paths with a minimum isolation of **30dB** between the different paths.

The SP4T is then simulated with the OMN and harmonic terminations in order to adjust the entire network and ensure adequate matching as shown in Figure 77.

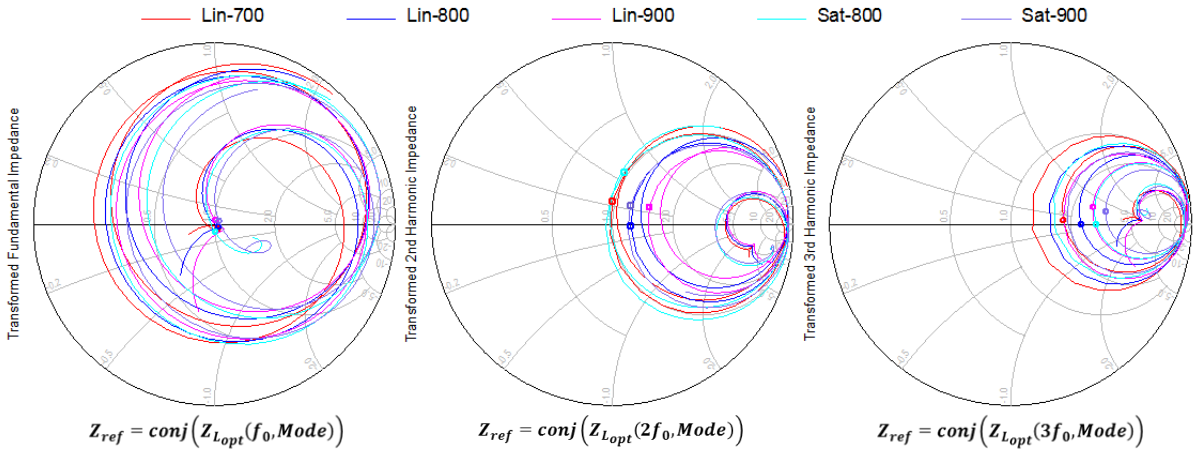


Figure 77: Impedance presented to the power stage by the combination of output matching network, harmonic traps and SP4T at the fundamental, 2nd harmonic and 3rd harmonic frequencies.

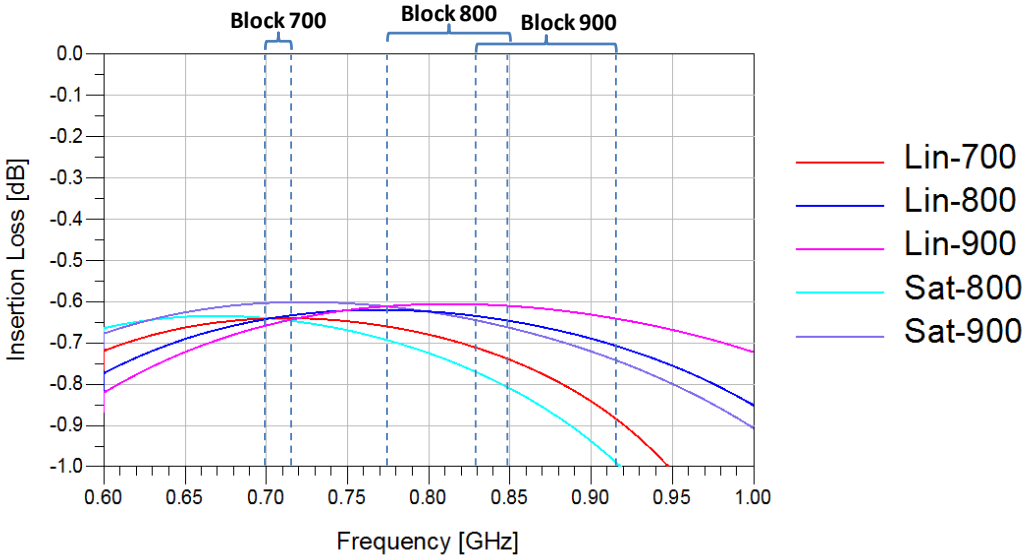


Figure 78: Insertion losses of the full matching network in each mode and frequency band

As can be seen in Figure 77, proper impedance matching is obtained at f_0 (left), $2f_0$ (center) and $3f_0$ (right). As shown in Figure 78, insertion loss is kept below **0.8dB**.

Table 33 summarizes the performance of the output assembly after adjusting the OMN.

Table 33: Simulated performance of the output sub-assembly including the SP4T in saturated and linear mode

Mode	Band	P_{sat} / P_{lin}	PAE	G_p	IL_{OMN}
Saturated	GSM800	36dBm	67%	12.5dB	0.8dB
	GSM900	35.4dBm	66%	12.3dB	0.7dB
Linear	700MHz	30.6dBm	41%	18.3dB	0.6dB
	800MHz	30.2dBm	40%	17.0dB	0.6dB
	900MHz	29.9dBm	39%	16.1dB	0.6dB

In saturated mode an output power higher than **35.4dBm** can be delivered with efficiency higher than **65%**. In linear mode efficiency is greater than **39%** for output power higher than **29.9dBm**.

D. Tunable capacitor design

In order to implement the reconfigurable matching network, 5 capacitances value are required for each capacitor. The tunable capacitor schematic presented in Figure 79 uses a thermometer code to synthesize 5 capacitance values, as shown in Table 34, where $C_{val\,1}$ to $C_{val\,5}$ designate the 5 capacitance values in increasing order.

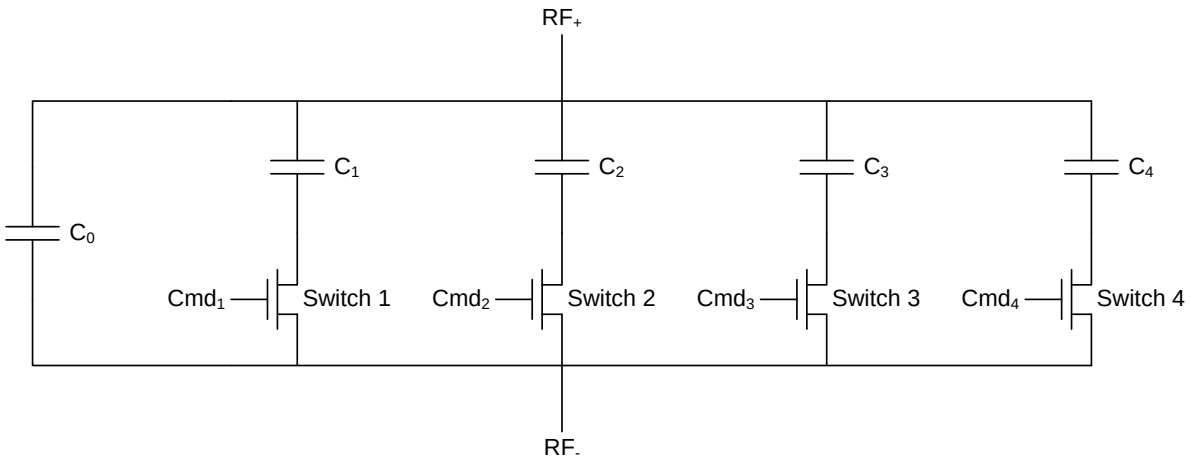


Figure 79: Schematic of a tunable capacitor

Table 34: State of the switches according to the capacitance value

Capacitance Value	Switch 1 state	Switch 2 state	Switch 3 state	Switch 4 state
$C_{val\,1}$	OFF	OFF	OFF	OFF
$C_{val\,1}$	ON	OFF	OFF	OFF
$C_{val\,1}$	ON	ON	OFF	OFF
$C_{val\,1}$	ON	ON	ON	OFF
$C_{val\,1}$	ON	ON	ON	ON

Using the methodology presented in Chapter 2, each switched capacitor branch is sized to handle a capacitance step. For illustration, the capacitance values for the first capacitor of the OMN ($C_{1\,OMN}$) and its capacitance steps is reminded in Table 35.

Table 35: Capacitances values and increments for the output matching network and the 2nd harmonic trap

Capacitor	$C_{val\,1}$	**1st step**	$C_{val\,2}$	**2nd step**	$C_{val\,3}$	**3rd step**	$C_{val\,4}$	**4th step**	$C_{val\,5}$
$C_{1\,OMN}$	25.5pF	4.2pF	29.7pF	1.3pF	31.0pF	5.0pF	36.0pF	3.0pF	39pF

The ratio between the off-state and on-state capacitances of a branch is set to **0.25**. Targeting a capacitance quality factor Q_C of **80**, it is possible to determine the required capacitance C_i and the MOS transistor size $W_{i\,SW}$ for each branch, where i designate the number of the branch. The sizing of the switched capacitors of C_1 in the OMN is shown in Table 36.

Table 36: Required component parameters for the realization of C_1 in the output matching network

Branch	C_i	$W_{i\,SW}$	$C_{i\,off}$
1	5.60pF	3.8mm	1.33pF
2	1.73pF	1.2mm	0.40pF
3	6.67pF	4.6mm	1.59pF
4	4.00pF	2.4mm	0.94pF

By summing the values in the $C_{i\,off}$ column, it can be seen that a capacitance $C_0$of 21.2pF is required to correctly generate $C_{val\,1}$. Using the same methodology, it is possible to size all the capacitors required in the matching network and harmonic terminations.

Once all the capacitors have been sized, a simulation of the voltages involved in the circuit is done to determine the required number of MOS stacked to avoid breakdown. Table 37 summarizes the number of MOS transistor stacked in each device.

Table 37: Required number of MOS transistor required in stacks in the output subassembly

$C_{1\,OMN}$	$C_{2\,OMN}$	$C_{trap\,H2}$	$C_{trap\,H3}$	SP4T switches
5	5	6	6	8

The output assembly with the varactors is then simulated to verify its performances. The results are shown in Table 38 for the CW and R'99 signals.

Table 38: Simulated performance in saturated an linear mode

Band	P_{sat}/ P_{lin}	PAE	G_p	IL_{OMN}
GSM-800	36dBm	68%	13.7dB	-0.8dB
GSM900	35.5dBm	69%	13.2dB	-0.7dB
700MHz	30.5dBm	39%	19.7dB	-0.6dB
800MHz	30.2dBm	40%	18.4dB	-0.6dB
900MHz	29.6dBm	39%	16.6dB	-0.7dB

III-3.3. Driver stage design

Performances of the driver depend on the gain of the power stage and the insertion loss of the inter-stage matching network.

To ensure proper operation of the power stage, the driver stage has to be more linear than the power stage. When operating in linear mode, the maximum ACPR level of the driver stage is set to **-43dBc**.

The efficiency requirement of the driver stage depends on the targeted overall efficiency. The overall efficiency $\eta_{overall}$ is given by Equation 77. The first term represents the contribution of the power stage and output matching network and the second one represents the contribution of the driver stage together with matching networks.

$$\eta_{overall} = \left(\frac{1}{\eta_{PWR} \cdot IL_{OMN}} + \frac{1}{IL_{IntMN} \cdot IL_{OMN} \cdot \eta_{DRV} \cdot G_{PWR}} \right)^{-1} \qquad \text{Equation 77}$$

G_{PWR}, and η_{DRV} are the gain of the power stage and the efficiency of the driver respectively, IL_{OMN} and IL_{IntMN} are the insertion losses of the output matching network (OMN) and inter-stage matching network (IntMN) respectively. Those two last parameters are dependent on the networks

topologies and quality factor of their constitutive components. In order to limit the degradation of the overall efficiency, efficiency of the driver must verify Equation 79.

$$\eta_{DRV} \geq \left(\left(\frac{1}{\eta_{overall}} - \frac{1}{\eta_{PWR} \cdot IL_{OMN}} \right) \cdot IL_{IntMN} \cdot IL_{OMN} \cdot G_{PWR} \right)^{-1} \qquad \text{Equation 78}$$

In saturated mode, drain efficiency and power gain of the power stage are ***81%*** and ***14dB*** respectively, while OMN insertion loss is ***-0.7dB***. In this mode, minimum driver efficiency as a function of IL_{IntMN} is given in Figure 80.

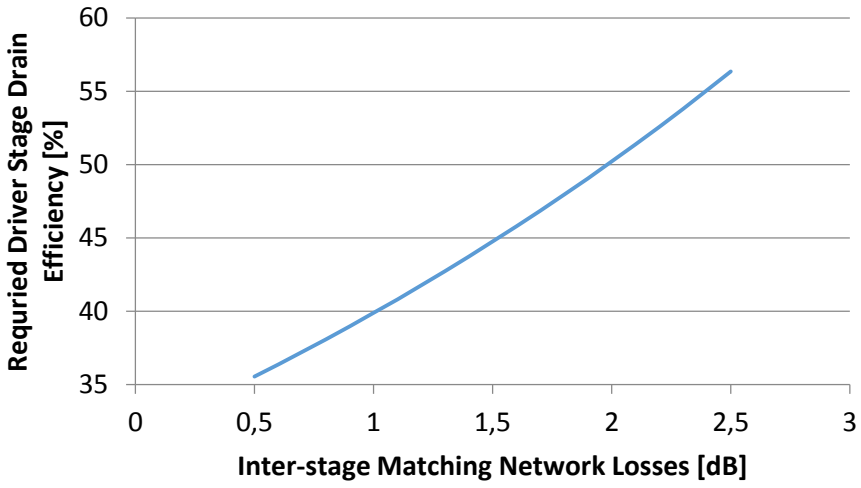


Figure 80: Minimum driver drain efficiency as a function of the inter-stage matching network insertion loss(IL_{IntMN}) in saturated mode

From this graph, we can determine the minimum efficiency of the driver for given IL_{IntMN}. Assuming IL_{IntMN} is **2dB** in saturated mode, the driver efficiency has to be higher than **50%**. Table 39 summarizes the requirements for the driver in both linear and saturated mode.

Table 39: Requirements of the driver stage according to the Interstage matching insertion loss

Mode	IL_{IntMN}	$P_{out_{DRV}}$	PAE_{DRV}	$ACLR_{DRV}$
2G	-2dB	24dBm	>50%	N/A
3G	-2dB	17dBm	>18%	-43dBc
4G	-2dB	17dBm	>15%	-38dBc

A schematic of the driver cell is presented in Figure 81. The driver cell is optimized to meet requirements in terms of large signal performance and impedance levels. Using design method presented in Chapter 2, size of the driver is set to 4mm.

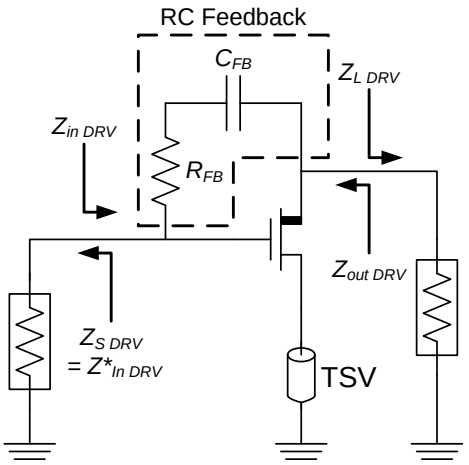


Figure 81: Schematic of the driver stage with RC feedback

Optimization of the driver cell then follows different steps. First, conjugate matching ($Z_{S\ DRV} = Z^*_{in\ DRV}$) is realized at the input to maximize the power gain. Second, a RC feedback is added to provide stability in the operating frequency band. While $Z_{S\ DRV} = Z^*_{in\ DRV}$ and the stability is maintained, $Z_{L\ DRV}$ is chosen to optimize driver performances.

Optimization has been done with a class-F driver in both saturated and linear modes, which is obtained by providing a short circuit at the second harmonic and an open circuit at the third harmonic. The feedback resistance R_{FB} has been set to **80Ω**.

Driver efficiency is **55%** and **22%** in saturated and linear mode respectively, allowing **60%** and **40%** efficiency for the whole PA line-up in saturated and linear modes.

III-3.4. Input matching network design

The chosen topology for the input matching network (IMN) is presented in Figure 82.

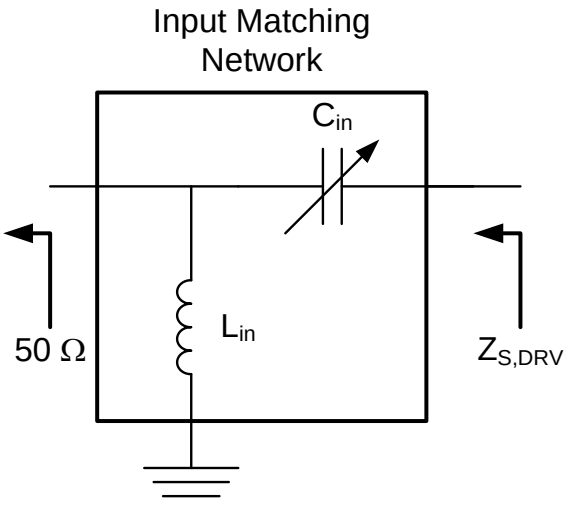


Figure 82: Topology of the input matching network

The transformation Q-Factor being smaller than the OMN's (**2.30**), a single L-C cell is enough to obtain the required bandwidth with limited insertion loss. Table 40 summarizes the capacitance values (C_{in}) for an inductance value of **4.1nH**.

Table 40: IMN Capacitor value according to the mode for a 4.1nH inductance

Mode	Lin-700	Lin-800	Lin-900	Sat-800	Sat-900
C_{in}	21.0pF	15.7pF	13.5pF	18.0pF	12.0pF

The different capacitance values are obtained through the implementation of a switched capacitor network. The simulated performances are presented in Figure 83.

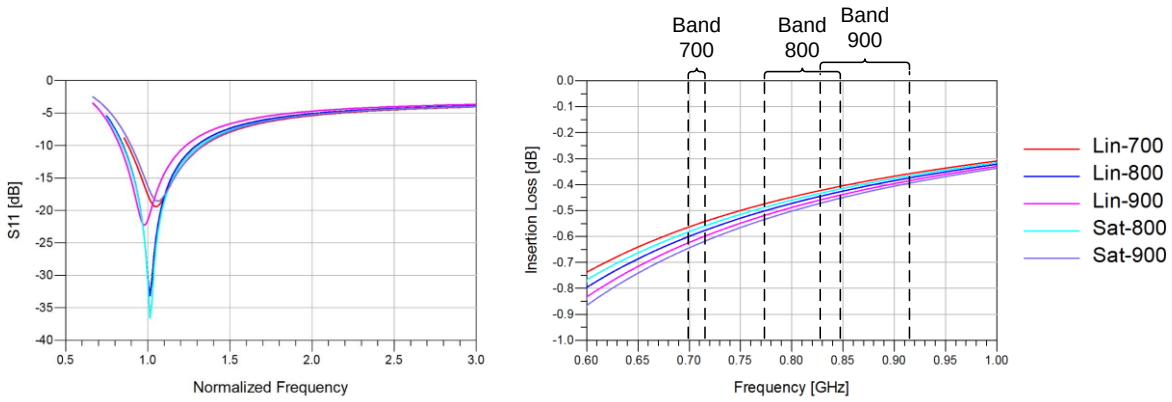


Figure 83: S_{11} (left) and insertion loss (right) of the input matching network for the different modes and bands

The simulation results show that the input matching is better than **-10dB** over the different frequency bands. Maximum insertion loss of the network is less than **0.6dB** with Q_L = **5** and Q_C=**40**.

The simulated performances of the driver stage together with the input matching network are given in Table 41.

Table 41: Simulated performance of the driver stage with input matching in saturated and linear modes.

Band	P_{sat}/P_{lin}	PAE	G_p	IL_{IMN}
GSM-800	24.4dBm	52%	10.4dB	-0.51dB
GSM-900	24.2dBm	51%	10.4dB	-0.60dB
700MHz	20.4	33%	12.3dB	-0.45dB
800MHz	20.0dBm	31%	12.1dB	-0.45dB
900MHz	20.2dBm	32%	12.4dB	-0.44dB

In saturated mode, the driver can deliver more than **24dBm** of output power with efficiency greater than **50%**. In linear mode, the linear output power is greater than **20dBm** with more than **30%** efficiency.

III-3.5. Inter-stage matching network design

The topology of the inter-stage matching network needs to provide adequate matching between the power stage and the driver stage. Four topologies have been studied as shown in Figure 84.

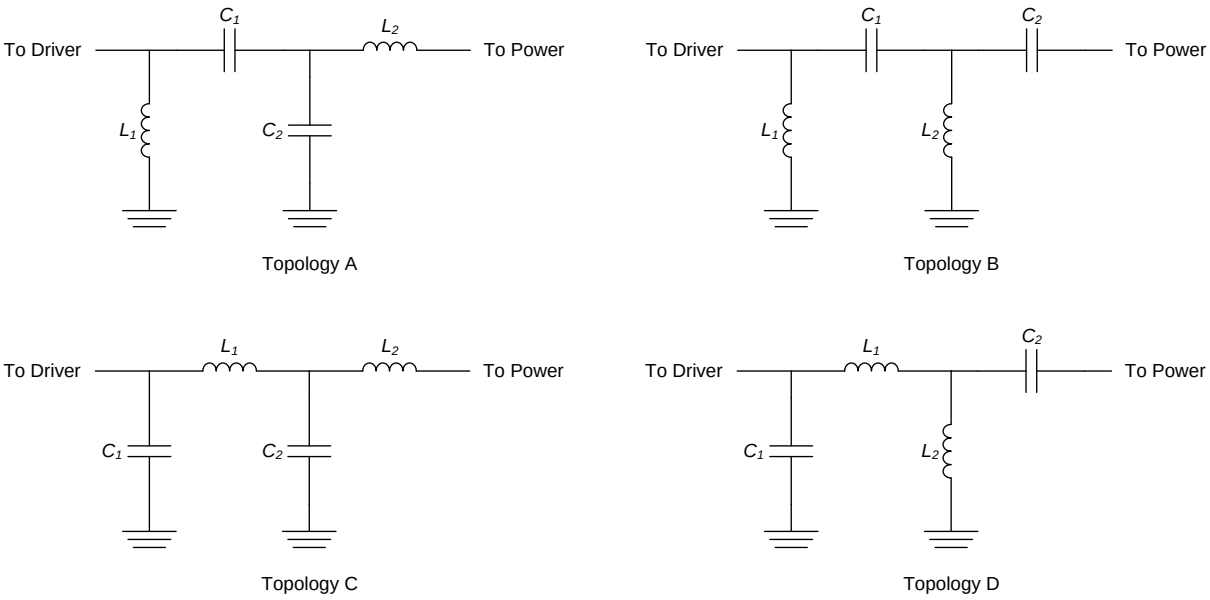


Figure 84: Inter-stage matching network topologies.

All those networks are composed of two L-cells, allowing the insertion of two varactors C_1 and C_2. These four networks are first compared for linear mode at **800MHz** in order to decide which topology performs the best for the chosen application. After optimization at **800MHz**, the simulated results for the different network configurations in linear mode are given in Figure 85. For the simulation, the quality factor of inductors was set to **10** while the quality factor of capacitors was **80**.

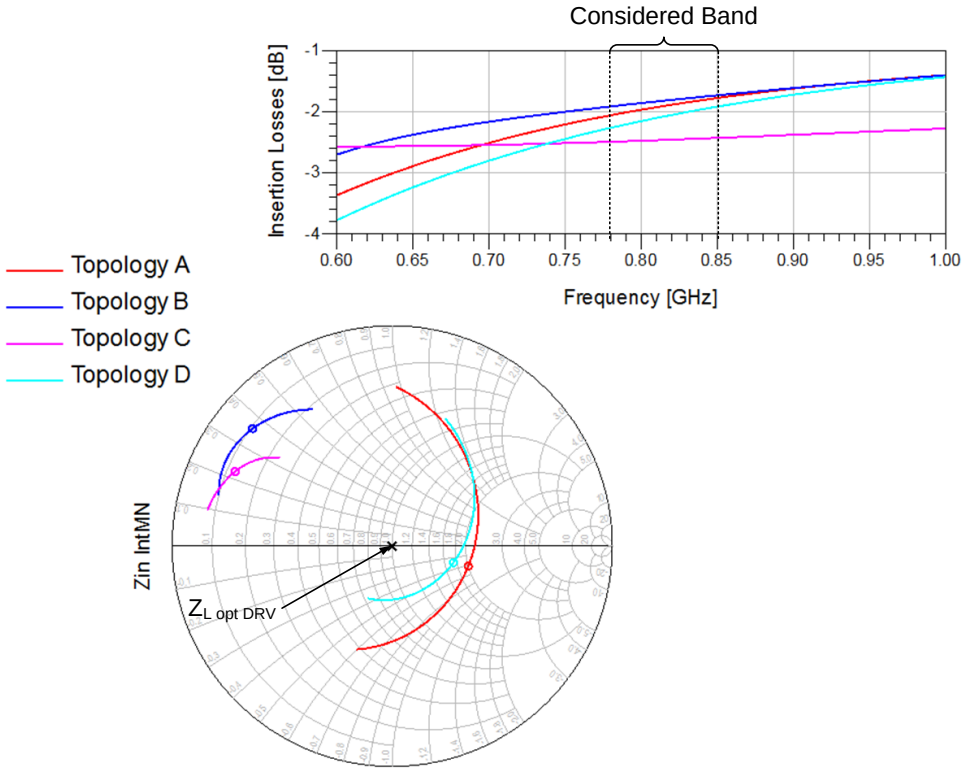


Figure 85: Insertion loss (top) and impedances seen at the input (bottom)

All topologies except topology C show insertion losses between **2.0dB** and **2.2dB** in the considered band. Matching at the output of the driver stage varies according to the network topology. The impedances presented by topologies B and C are located on the periphery of the Smith chart and are not well suited. Topologies A and D provide better matching. Topology A has lower losses than topology D but matching presented to the driver stage is better with topology D. Therefore, the topology D is chosen to realize the inter-stage matching network, whose corresponding components values are given in Table 42.

Table 42: Component values of the inter-stage matching network

Mode	C_1	C_2	L_1	L_2
Lin-700	12pF	55pF	1.65nH	1.25nH
Lin-800	7.7pF	45pF		
Lin-900	5.0pF	38pF		
Sat-800	5.0pF	55pF	1.3nH	0.95nH
Sat-900	3.5pF	45pF		

The network requires two inductance values. Tunable inductors are implemented using fixed inductors in parallel with a switched capacitor, see Figure 86.

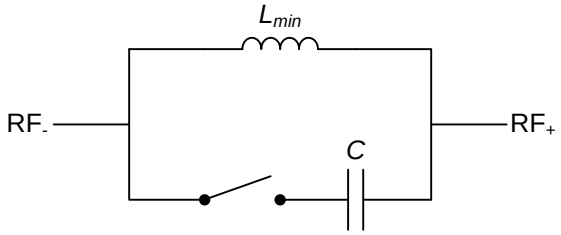


Figure 86: Implementation of a tunable inductor

When the capacitor is off, the minimum inductance value (L_{min}) is obtained. When the capacitor is on, the inductance value is increased to L_{eq}, as defined in Equation 79 where f_0 is lower than f_{res}.

$$L_{eq} = \frac{L_{min}}{1 - \left(\frac{f_0}{f_{res}}\right)^2} \text{ where } f_{res} = \frac{1}{2\pi\sqrt{L_{min}C}} \qquad \text{Equation 79}$$

Using the following equations, the capacitances associated with L_1 and L_2 are determined.

$$C = \frac{1}{L_{min} \cdot \frac{2\pi f_0}{\sqrt{1-\frac{L_{min}}{L_{eq}}}}} \qquad \text{Equation 80}$$

The required parallel switched capacitors are **6.5pF** for L_1 and **10pF** for L_2. C_1 and C_2 are realized using switched capacitor as previously described.

III-3.6. Reconfigurable MMPA line-up implementation

The reconfigurable MMPA architecture was implemented in a SOI-CMOS 130 nm technology through the design of two circuits, see the block schematic in Figure 87.

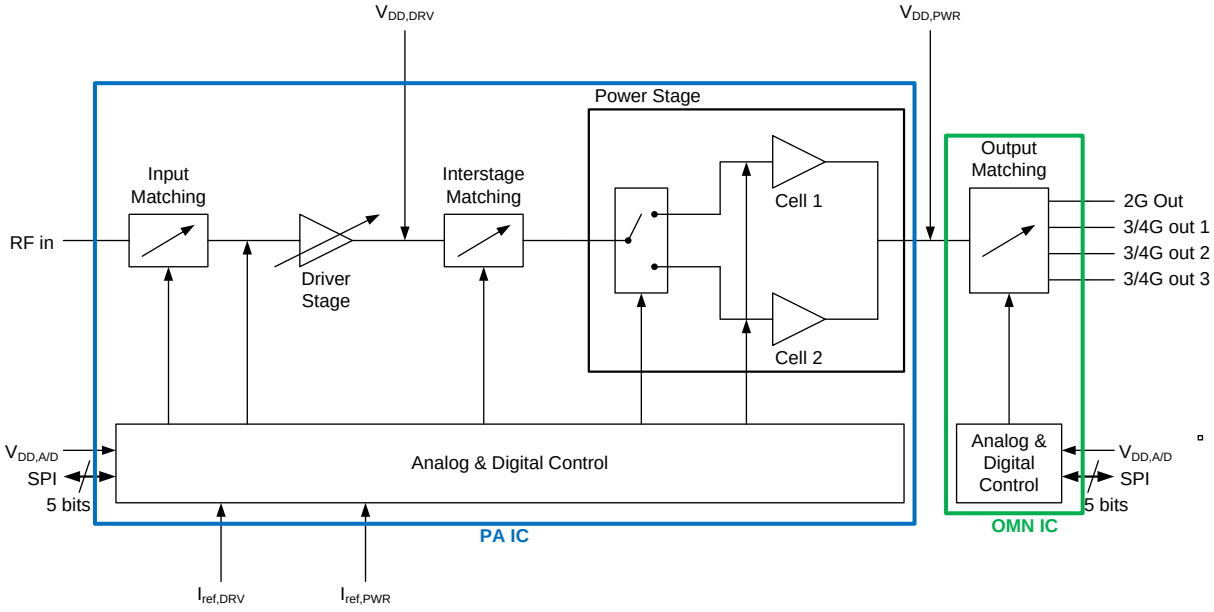
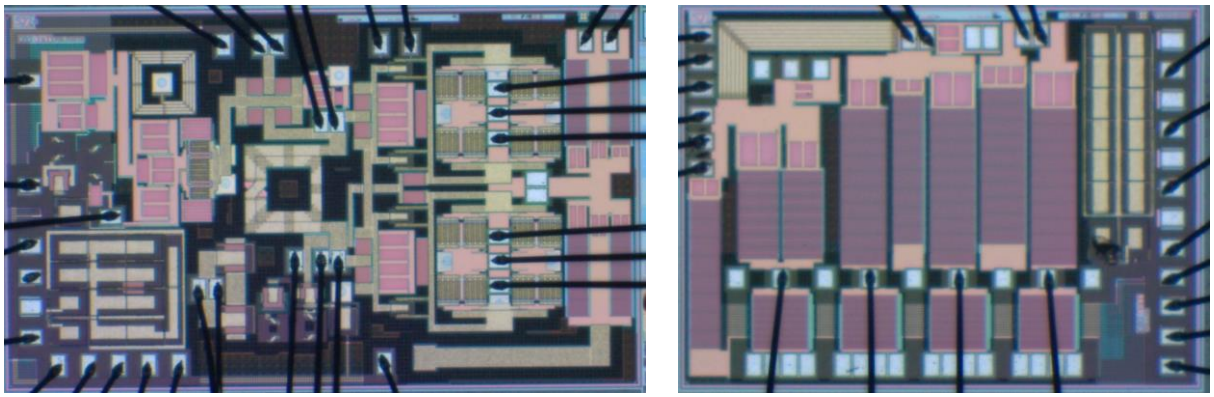


Figure 87: Block schematic of the implementation of the MMPA architecture.

The first integrated circuit (IC) includes the power and driver stages, inter-stage and input matching networks, and bias and control circuits (PA IC). The second one (OMN IC) integrates the output matching network including the output SP4T. Both ICs are shown in Figure 88.



(a) (b)

Figure 88: Photographs of the two circuits: PA (a) and OMN (b)

The full MMPA test board is depicted in Figure 89.

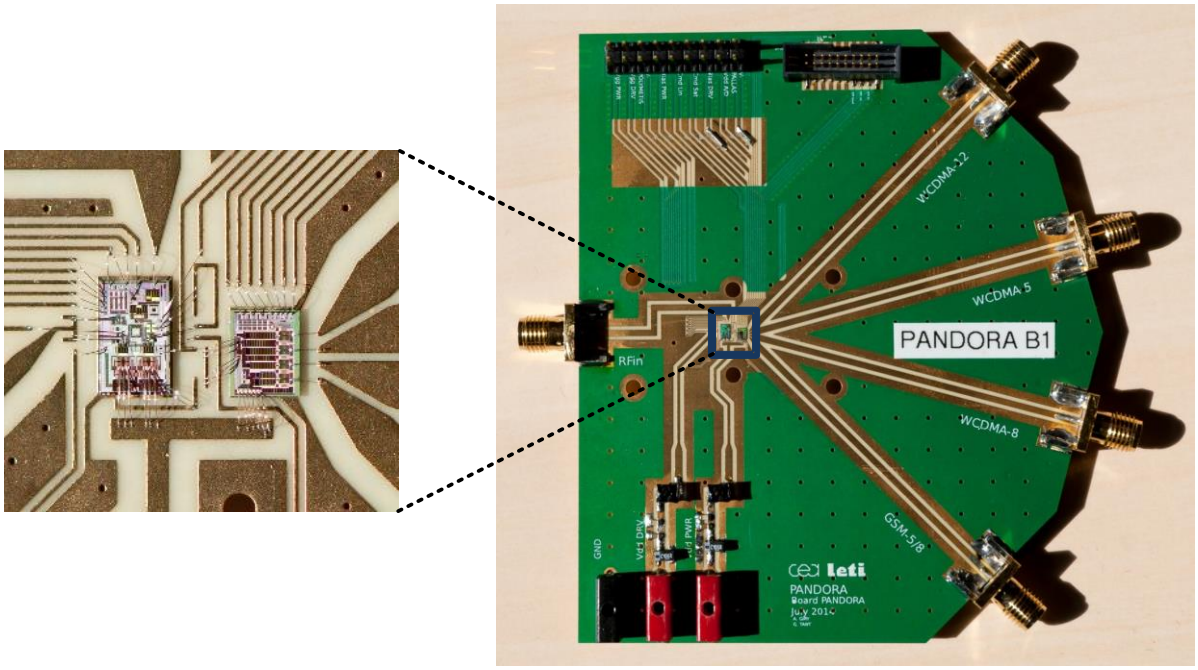


Figure 89: Photograph of the test board

The full MMPA line-up was simulated with a **3.3V** supply voltage. The saturated mode has been simulated in CW and the linear mode with a W-CDMA release'99 test signal. Table 43 gives the simulated performances of MMPA line-up for the different modes and bands.

Table 43: Simulated performance of the reconfigurable MMPA.

Mode	P_{sat} / P_{lin}	PAE
Sat-800	35.0dBm	58%
Sat-900	34.9dBm	51%
Lin-700	30.2dBm	38%
Lin-800	30.1dBm	37%
Lin-900	29.6dBm	35%

All the modes meet the targeted performance.

III-4 Measured performances

The measurement set-up is shown in Figure 90. It includes DC supplies for the driver stage ($V_{DD\ DRV}$), the power stage ($V_{DD\ PWR}$), and the Analog & Digital Control ($V_{DD\ A/D}$). SPI signals are generated using a National Instrument PXIe 6548 card driven with LabView. According to the type of measurements, a Vector Network Analyzer or the combination of a Signal Generator and a Spectrum Analyzer are used for the RF measurement.

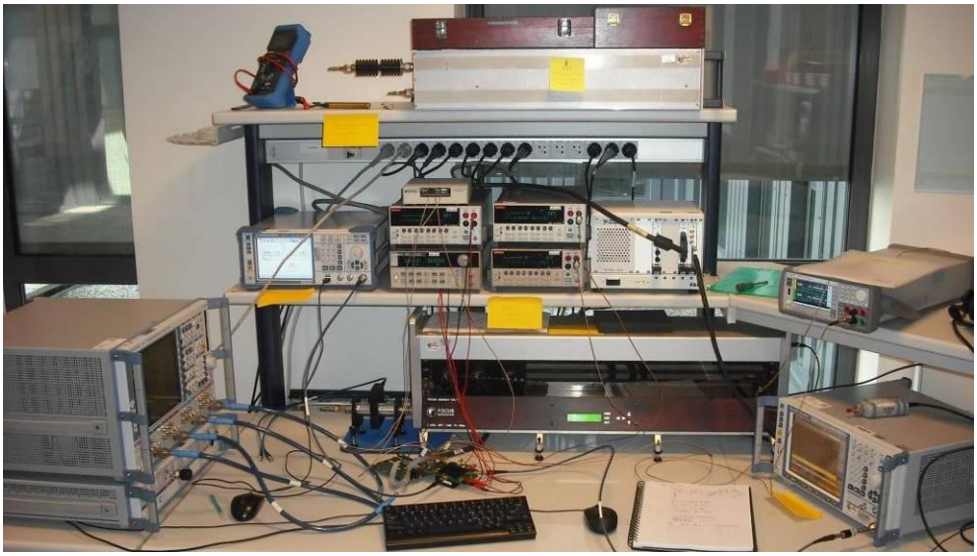


Figure 90: Photograph of the test bench for reconfigurable MMPA characterization

The two ICs are tested independently before measuring the full line up.

III-4.1. Power amplifier characterization

A dedicated board has been designed to measure the performance of the PA IC in a stand-alone condition. The board includes a matching network which is tuned according to the desired mode and band in order to synthesize $Z_{L\,opt}$.

The PA is tested under a 3.3V supply voltage in S-Parameters and large signal conditions. A comparison between the retrofitted simulated and measured S-Parameters in linear and saturated mode at 900MHz is given in Figure 91.

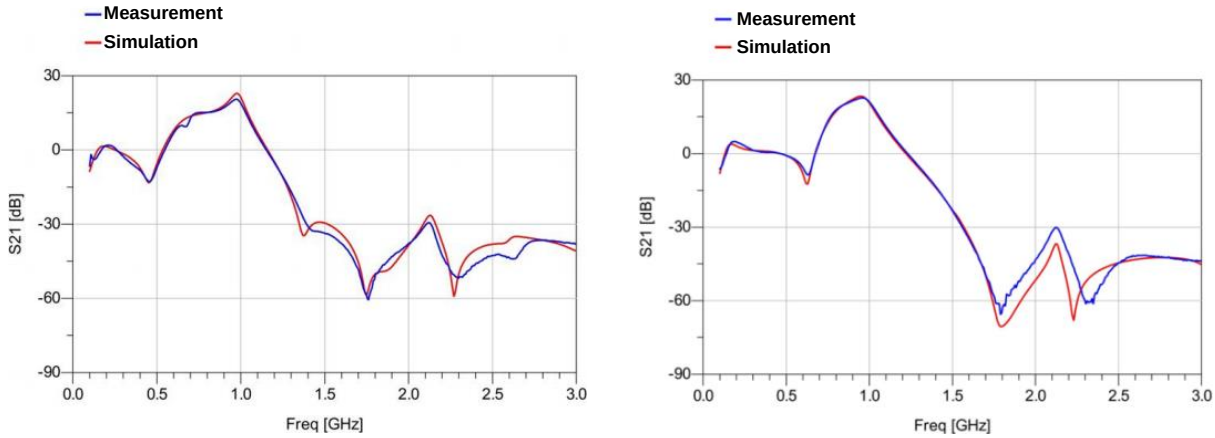


Figure 91: Measured (blue) vs. simulated (red) S-Parameters of the MMPA in linear mode (left) and saturated mode (left) at 900MHz.

Very good correlation between measurements and simulations are observed on a wide frequency range. The model of the MMPA is therefore valid. *PAE* of the MMPA measured in large signal CW in saturated and linear modes is shown in Figure 92. At **800MHz**, the measured maximum *PAE* is **67%** at **35dBm** output power, while at **900MHz**, the *PAE* is **58%** at **36dBm** output power.

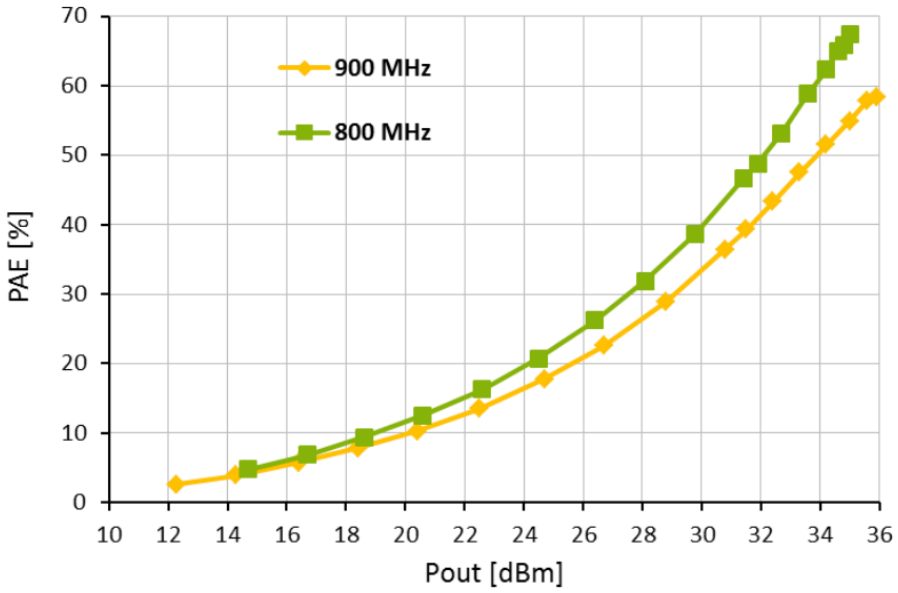


Figure 92: CW measurements of the PA IC in saturated mode.

Linear mode is also tested with a CW signal. The results are presented in Figure 91.

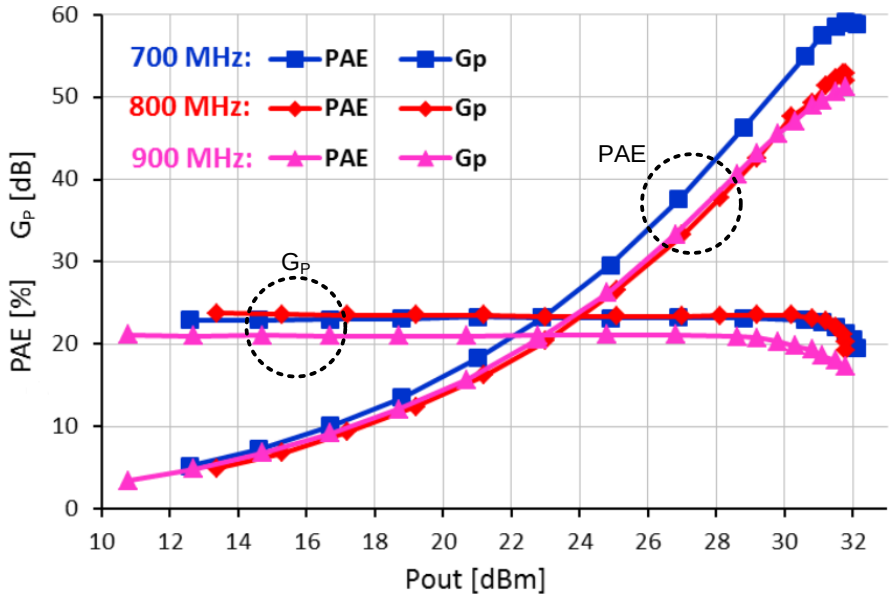


Figure 93: CW measurements of the PA IC in linear mode.

The output compression point is **31.5dBm**, **31.2dBm** and **30.1dBm** respectively at **700MHz**, **800MHz** and **900MHz** with **59%**, **51%** and **47%***PAE*. These results are summed up and compared to the state of the art in Table 44.

Table 44: Performance summary and comparison with the state of the art.

Reference		[Kang14]	[Kim14a]	[Li11]	This work
Standards		2G/3G/4G	3G/4G	3G/4G	2G/3G/4G
Frequencies [MHz]	Low Band	850/900	800	800	700/800/900
	Medium Band	-	-		-

	High Band		1800/2000	1900/2300	2400	-
Saturated Mode	PAE @ P_{sat} [%]	800MHz	52	-	-	67
		900MHz	53	-	-	58
	P_{sat} [dBm]	800MHz	35.1	-	-	35
		900MHz	34.8	-	-	36
Linear Mode	PAE @ P_{1dB} [%]	700MHz	-	-	-	59
		800MHz	≈43 (3G) ≈40 (4G)	33 @ 26dBm	55	51
		900MHz	≈45 (3G) ≈45 (4G)	-	-	47
	P_{1dB} [dBm]	700MHz	-	-	-	31.5
		800MHz	≈28.3 (3G) ≈28 (4G)	28 @ P_{max}	24.4	31.2
		900MHz	≈28.5 (3G) ≈28.5 (4G)	-	-	30.1
Supply Voltage [V]			3.5	3.3	4.2	3.3
Supply Modulation			None	Hybrid-EER	ET	None
Technology			2 µm InGaP/GaAs	0.18 µm CMOS SOI	0.35 µm BiCMOS SiGe	0.13 µm CMOS SOI
Circuit Area [mm²]			35	4	1.65	2.5

The proposed reconfigurable MMPA shows better saturated mode efficiency under 3.3V than the state of the art and higher linear mode P1dB. These results are promising and demonstrate the relevance of the SOI CMOS technology for high performance reconfigurable MMPA integration.

III-4.2. Output matching network characterization

The output matching network has also been tested in stand-alone using a dedicated test-board. Figure 94 shows the measured insertion loss of the OMN IC in the different modes.

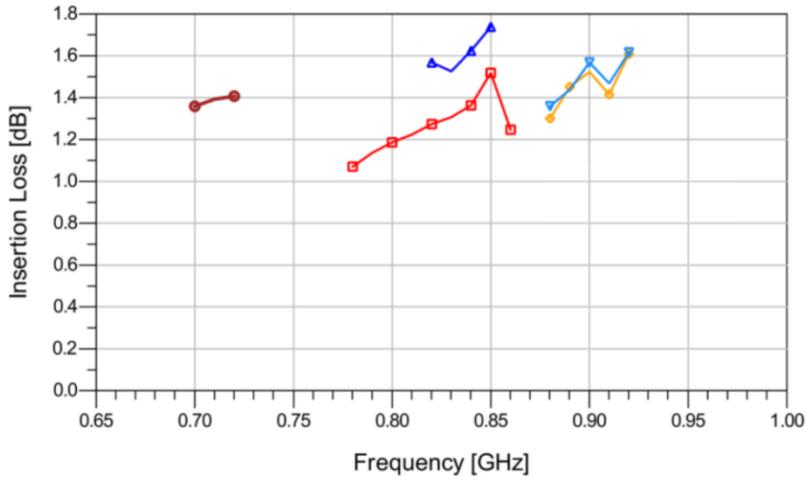


Figure 94: Measured insertion loss in each mode (Linear Mode at 700MHz (circles), at 800MHz (squares), at 900MHz (diamond) and saturated mode at 800MHz (triangle) and at 900MHz (reversed triangle))

Measured insertion loss is **0.8dB** higher than initially simulated, but lower than **1.7dB** in every mode. Analysis of the circuit shows that the quality factor of the MOM capacitors involved in the switched capacitor arrays is lower than predicted. Furthermore, study of the layout shows that some interconnects have higher series resistance than anticipated. A retro-simulation of the OMN in

saturated mode at **800MHz** after adjustment is presented in Figure 95 and compared to measurements. The figure validates the study of the IC.

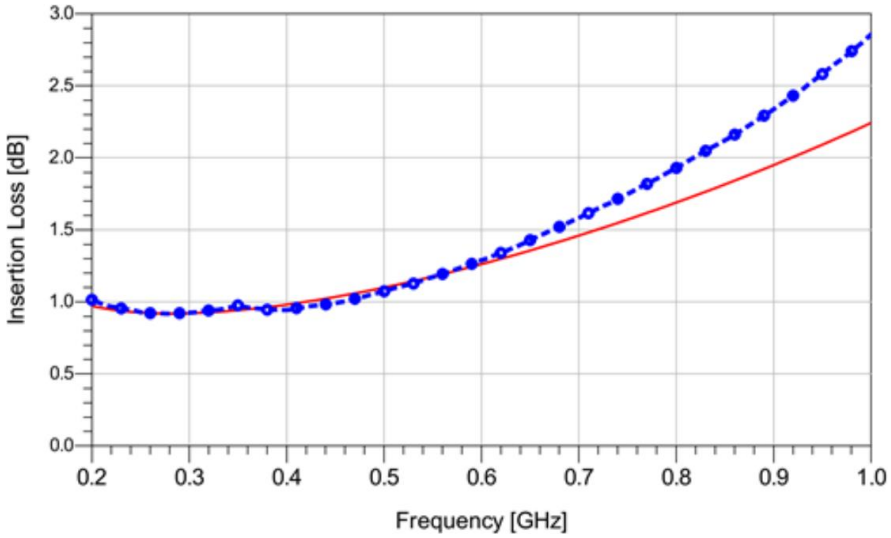


Figure 95: Retro-simulated (blue dotted line) vs. measured IL of the OM in saturated mode at 800MHz.

As a last performance assessment, Figure 96 shows the measured input impedance versus simulated value.

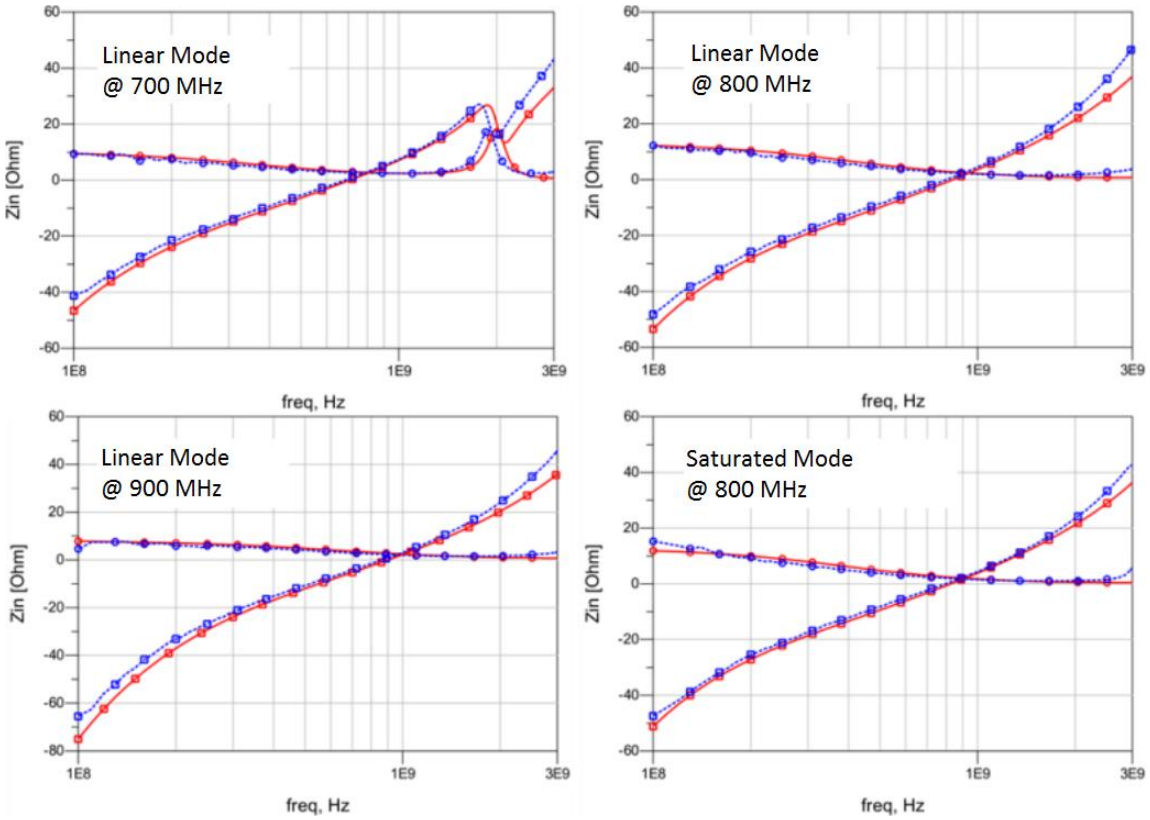


Figure 96: Measured (blue dotted lines) vs. simulated (red solid lines) input impedance of the OMN IC in its different configurations (real part in circles, imaginary part in squares).

As can be seen on the figure, a good similarity is obtained over wide frequency range for every mode despite the high insertion loss. The performance of the OMN IC is summarized and compared with devices based on BST capacitors (A) and PIN diodes (B) in Table 45. Note that only few other works have been reported so far.

Table 45: OMN IC performance summary and comparison with other works.

Reference	Number of ports	Z_{in} [Ω]	*IL* [dB]	Area [mm²]	Frequency [MHz]
This work	4	1.9 + j1 (Sat.) 2.7 + j0.7 (Lin)	1.1 – 1.7	1.5	700 – 920
[Tombak07]	1	3.4 - j1.9 4.3 + j1	1.4 – 1.6 1.8 – 2.1		820 – 920 1700 – 2000
[Kang15]	2 3	- -	- -	10 10	820 – 920 1700 – 2000

III-4.3. MMPA line-up characterization

Continuous Wave (CW) measurements have been done to check the large signal behavior of the MMPA. The measured CW performances for every mode of the PA are shown in Figure 97.

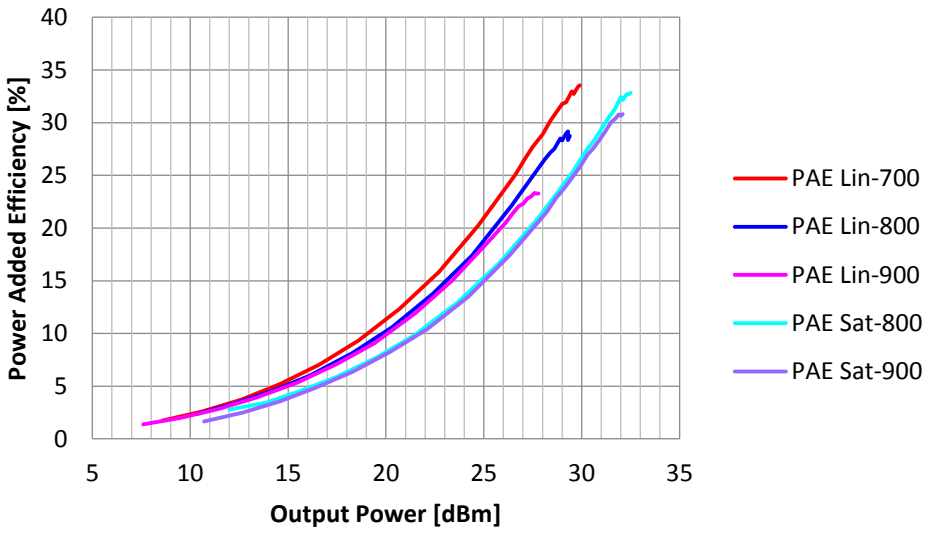


Figure 97: Measured PAE and power gain under CW signal

In saturated mode, the MMPA delivers **32.5dBm** output power with **33%** efficiency at **800MHz** and **32.1dBm** output power with **31%** efficiency at **900MHz**. In linear mode, at **700MHz**, **800MHz** and **900MHz** respectively, P_{1dB} is **29.2dBm**, **28.9dBm** and **26.8dBm** with **32%**, **29%** and **22%** efficiency.

This degraded performance comes from the assembly of both chips. Indeed, the MMPA IC and OMN IC are connected together with a micro-strip line and bondwires that takes part in the matching. Inaccurate sizing of this interconnection leads to incorrect load impedance for the MMPA in every mode. Combined with the increase IL in the OMN, the output power is decreased by more than 3dB in saturated mode and 2dB in linear mode.

To correct this issue, this interconnection on the board should be tuned or redesigned to improve the output matching of the MMPA. This work was not done due to a lack of time at the end of the study.

Nonetheless, the previous results show the potential of the 130 nm SOI CMOS process for the design of 2G/3G/4G reconfigurable power amplifiers. With more precise passive and interconnect models, the design process could become more accurate and even better performance could be achieved.

III-5 Conclusion

This chapter has described the design of an integrated SOI CMOS reconfigurable MMPA for the low E-UTRA bands, ranging from 700MHz to 900MHz, for 2G, 3G and 4G standards. The output power stage uses a reconfiguration in size to handle the different requirements of the saturated and the linear modes. The optimal load impedances in each mode and band are synthesized using a reconfigurable output matching network.

The output matching network is actuated using switched capacitor banks. Reconfigurable harmonic terminations are included to optimize the performance of the power stage. A SP4T at the output of the circuit allows routing the signal to the proper output according to the targeted standard and band.

The PA driver is sized according to the performance of the power stage combined with the output matching network. The input matching network and inter-stage matching network were designed using the same methodology as the output matching network. The input matching network uses a simple topology to ensure maximum power transfer to the driver stage. The inter-stage matching network's topology has been chosen to ensure that the optimal source impedance of the output stage is correctly generated while ensuring proper operation of the driver stage.

The bias circuit is optimized to provide low baseband impedance to the stages, thus limiting the memory effects.

The power amplifier was implemented in 2 integrated circuits. The power amplifier circuit shows performance at the state of the art in terms of output power and efficiency.

The output matching circuit provides the targeted impedances, for a lower surface when compared to the literature. Lower quality factor in MOM capacitors and higher resistance in interconnections however translates in insertion losses slightly higher than expected. This was demonstrated by post-simulations.

The full assembly is composed of both integrated circuits mounted on test board. It suffers from the insertion loss issues in the output matching circuit. The performance is also decreased due to imprecision in the combining line implemented on the board which participates in synthesizing the optimal load impedance of the power stage. Nonetheless, output powersof**30dBm** in linear mode and **32dBm** in saturated mode have been measured. The chosen technology is therefore considered as a promising candidate for integrating reconfigurable MMPA. Further investigation on the assembly of the two circuits and improved layout of the output matching network could help reaching the targeted performance.

The next chapter describes PA architectures to improve efficiency.

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Chapter IV: Study of High Efficiency PA architectures

IV-1 Introduction

The previous chapter presented concepts and design of a reconfigurable multi-mode multi-band power amplifier. However, efficiency optimization at back-off power was not considered, the proposed reconfigurable MMPA being optimized only at maximum power in each mode and band.

In this chapter efficiency enhancement at back-of power using PA architectures with supply or load impedance modulation are studied.

A comparison of Envelope Tracking and Passive Load Modulation techniques are presented. A detailed study of Load Modulation is described and a functional prototype is proposed. The design methodology of a Tunable Matching Network for this architecture is also proposed.

IV-2 PA efficiency enhancement

In this section both Envelope Tracking (ET) and passive Load Modulation (LM) techniques will be compared on a Class-F power cell. Figure 98 shows the efficiency improvement that can be obtained with each technique compared to the power cell with fixed supply voltage and load impedance.

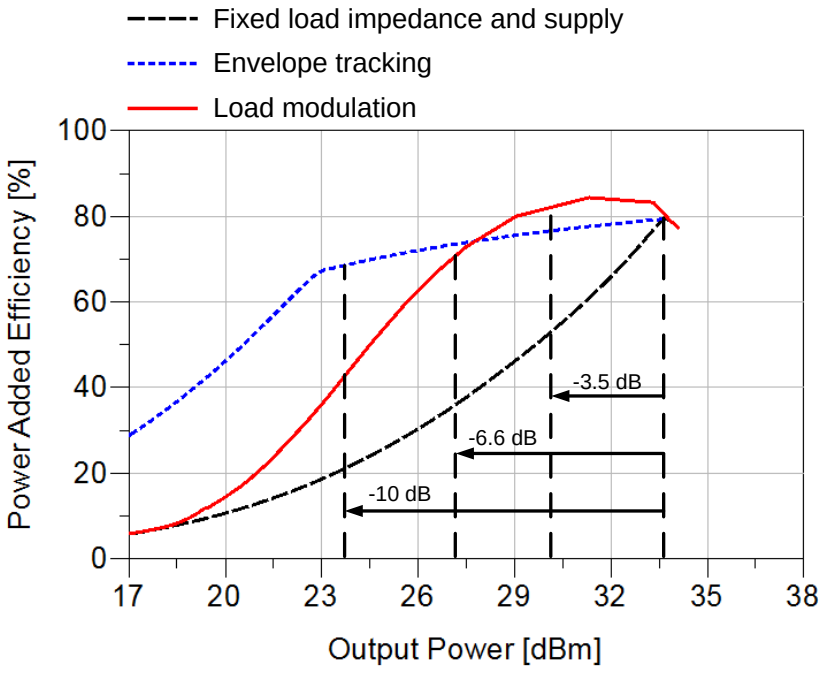

Figure 98: PA efficiency for fixed supply and load and , ET and LM configurations

With each technique efficiency in back-off can be highly improved. However, according to the considered back-off, several situations may occur. Up to 3.5dB back-off, LM performs better than ET. At 6.6dB back-off, both techniques lead to equivalent improvement. For higher back-offs ET becomes the better choice to improve efficiency.

IV-2.1. Efficiency enhancement limitations

In order to understand efficiency limitations of the LDMOS transistor in back off, we can express drain efficiency as a function of its on-state resistance (R_{on}) and output capacitor (C_{out}).

During the RF cycle, part of the RF power is dissipated in the on-state resistance (R_{on}), so that part of the drain efficiency can be expressed as [Rijs06]:

$$\eta_{series} = 1 - \frac{V_k}{V_{DD}} = \frac{1}{1 + \gamma_S \frac{R_{on}}{R_L}} \qquad \text{Equation 81}$$

Where R_L is the optimal load resistance that is presented to the current source of the LDMOS transistor and γ_k is a coefficient depending on the operating class of the LDMOS transistor as explained in Chapter 2.

Some RF power is also dissipated in the parasitic resistance associated with the output capacitance, so that other part of drain efficiency can be expressed as [Rijs06]:

$$\eta_{parallel} = \frac{1}{1 + \gamma_P \omega^2 C_{out}^2 R_P R_L} \qquad \text{Equation 82}$$

Where γ_P is a coefficient depending on the operating class of the LDMOS transistor and RP is given by Equation 83.

$$R_P = \frac{R_{ds} \cdot C_{out}^2}{(\omega_0 \cdot R_{ds})^2 + C_{out}^2} \qquad \text{Equation 83}$$

The two previous losses are involved in the drain efficiency expression as given by

$$\eta_{total} = \eta_{ideal} . \eta_{series} . \eta_{parallel} \qquad \text{Equation 84}$$

A. Limitation with envelope tracking

The load impedance R_L required for high power amplification being small compared to the equivalent parallel parasitic resistance R_P, we can consider that parallel loss can be neglected.

At low power, the knee voltage's contribution on the other hand increases as V_{DD} becomes smaller: the ratio V_k/V_{DD} increases, therefore η_k decreases. The overall efficiency therefore decreases.

B. Limitation with load modulation

With load modulation, R_L increases when the output power decreases so that η_k increases as can be observed in Figure 98 up to 6dB back-off. As R_L increases, it becomes comparable to R_P. Therefore, a greater part of the RF power is dissipated by R_P and $\eta_{parallel}$ induce a drop in efficiency from the medium to low power region. In the low power region, the parallel loss is so high that LM technique does not induce better efficiency than the fixed load power cell.

IV-3 Supply and load modulation PA design

When considering complex modulated signals, linearity has to be considered. Figure 99shows the gain and phase response of the power cell for fixed supply and load impedance, and with ET and LM used to maximize efficiency.

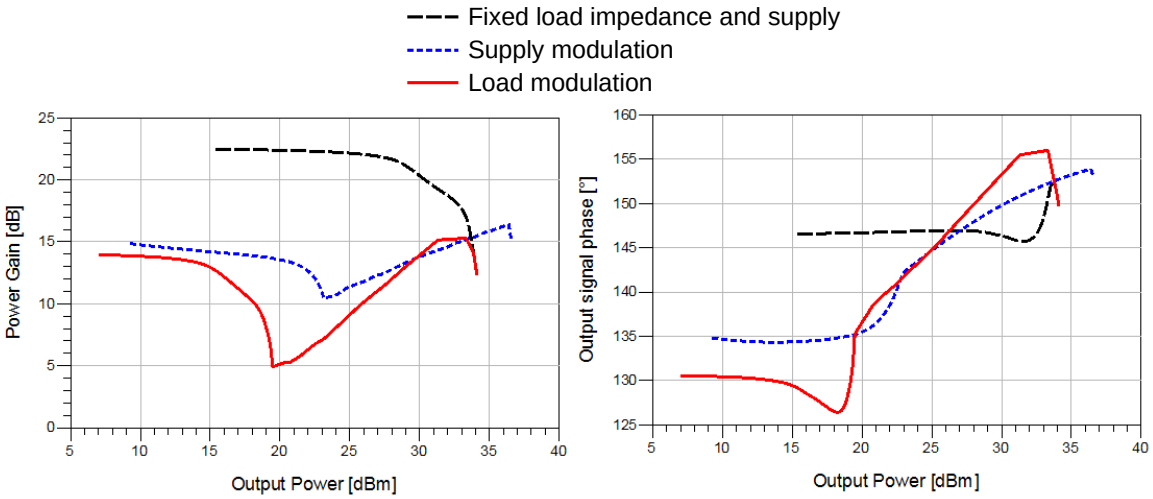

Figure 99: Amplitude (left) and phase (right) response of the power cell for fixed supply and load impedance (black dashed line), ET (blue dotted line) and LM (red solid line) configurations.

As can be seen, maximization of efficiency at medium and low power leads to poor linearity. The gain with fixed load impedance and supply shows an amplitude variation of less than **1dB** up to the output 1-dB compression point (P_{1dB}) of **28.5dBm**, with a corresponding phase variation of less than **0.4°**.

With ET, a gain variation of **4.4dB** is observed up to the same output power with a phase variation of **14°**. With LM, a gain variation of **4.9dB** is observed up to the same output power with a phase variation of **24°**.

With such ET and LM optimizations, digital pre-distortion (DPD) becomes necessary in order to satisfy linearity specifications. Unfortunately, DPD requires DC power consumption that can be comparable to the consumption of the power device itself, hence limiting the overall efficiency of the architecture [Nujira12].

IV-3.1. Envelope Tracking

Optimized envelope shaping which represents the relation between the supply voltage and the RF power level can be used to preserve linearity. By choosing a shaping function which provides constant gain over the desired power range, high linearity together with high efficiency can be obtained.

Figure 100 depicts the efficiency, gain response and phase response of a power cell for three configurations:

- Fixed load impedance and supply voltage (3.3V)
- ET with optimized envelope shaping to maximize efficiency
- ET with isogain shaping

For ET, the supply voltage is modulated between **1.5V** and **4V**.

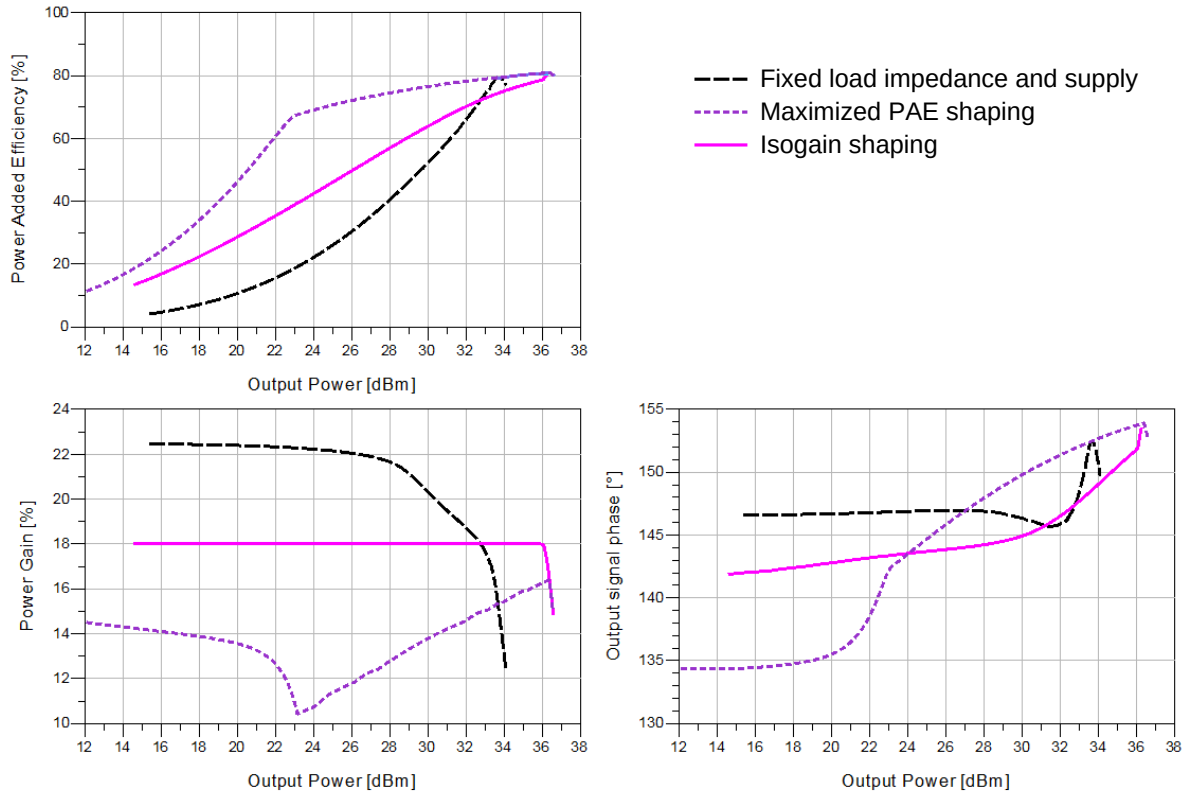

Figure 100: Efficiency (top left), gain (bottom left) and phase (bottom right) comparison between the stand alone cell, ET power cell with maximum efficiency shaping and ET power cell with isogain shaping.

Envelope information which is extracted using an envelope detector is transferred to an envelope shaping block where the detected envelope power is compared to the power levels stored in a shaping data file. The corresponding supply voltage is then applied to the power cell. In order to quantify the achievable PAE improvement, the power cell using ET with isogain shaping (ET cell) is compared to the fixed supply cell for 3G (Figure 101) and 4G (Figure 102) signals

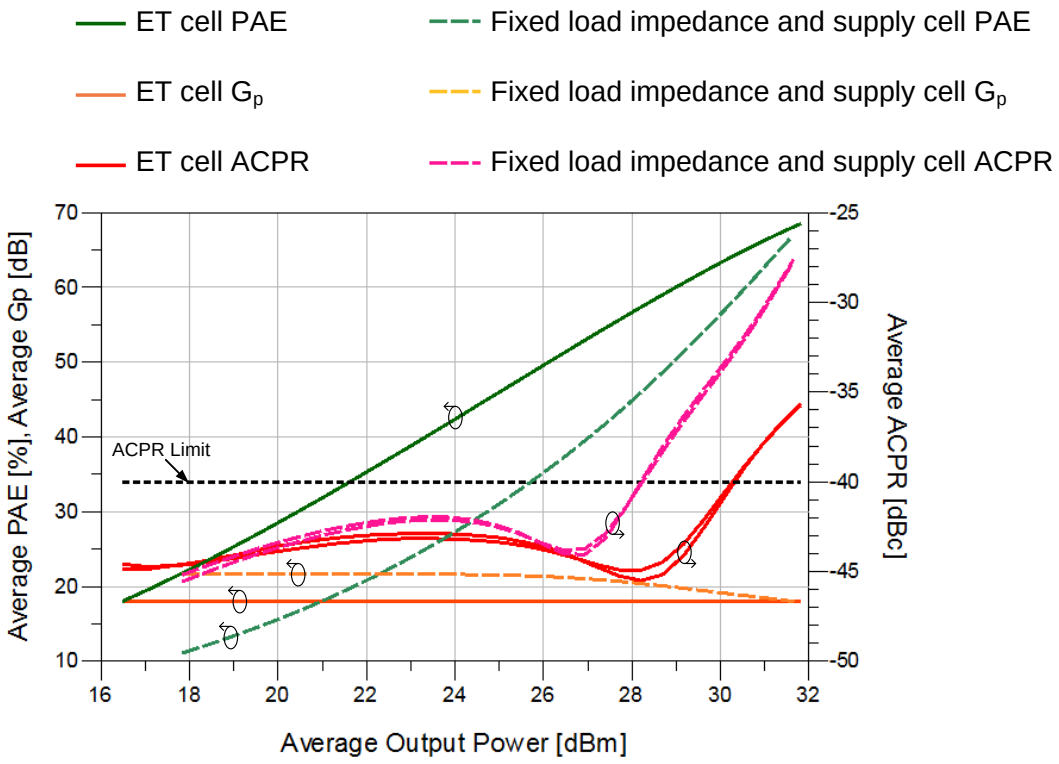

Figure 101: Simulated performance of the ET power cell with a Release'99 signal at 835MHz.

As can be seen on the graph, the linear power (P_{lin}), for which ACPR (red) is kept below the required limit, is higher in the case of the ET cell (**30.3dBm**) compared to the fixed supply power cell (**28.2dBm**). Lastly, the PAE (green) at P_{lin} is higher for the ET cell, **64%** compared to **46%**. At **24.3dBm** output power (**6dB** back-off), the efficiency of the ET cell is **43.7%**, which is a **50%** improvement. To ensure the overall efficiency is improved, the efficiency of the supply modulator $\eta_{modulator}$ of the ET cell must be higher than a limit value. The performance of both cells and required $\eta_{modulator}$ are summarized in Table 46.

Table 46: Simulated performance of the ET PA with a Rel'99 signal @ 835MHz (ACPR = -40dBc).

	P_{lin}	<PAE> @ P_{lin}	$<PAE_{3dB\ BO}>$	$<PAE_{6dB\ BO}>$	$<PAE_{10dB\ BO}>$
Fixed supply power cell	28.2dBm	46%	41%	29%	16%
ET cell	30.2dBm	64%	54%	44%	29%
Efficiency Improvement	-	+39%	+32%	+52%	+81%
$\eta_{modulator}$	-	>72%	>76%	>66%	>55%

This table shows that the ET power cell requires a supply modulator with efficiency greater than 76% to get improved overall efficiency.

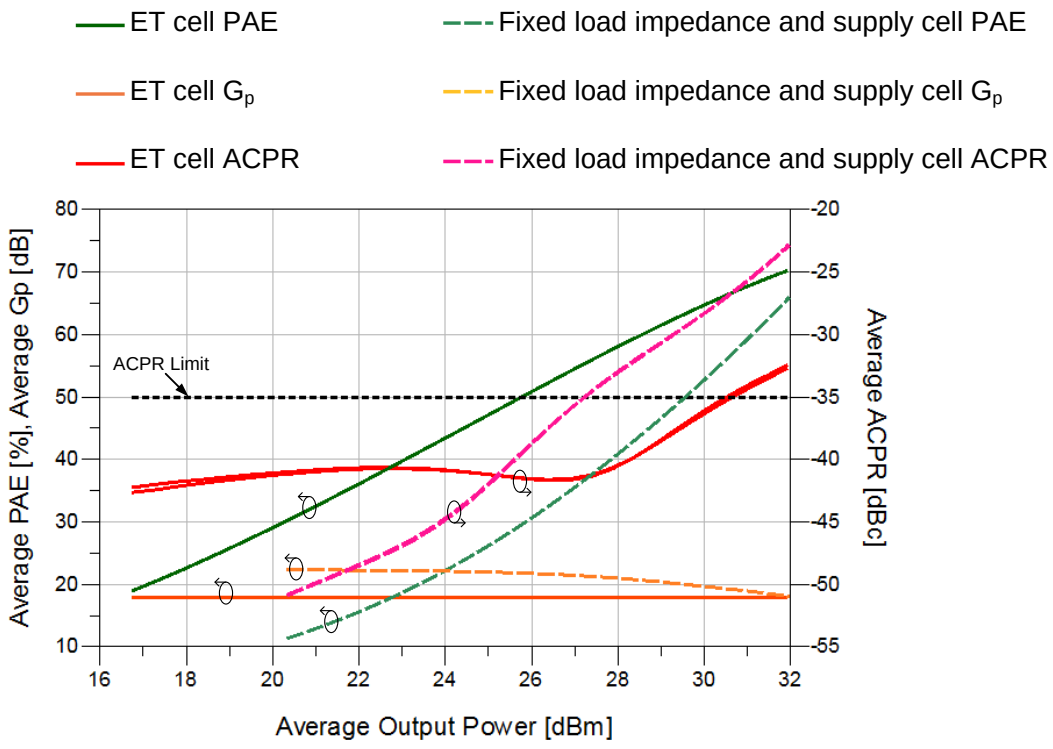

Figure 102: Simulated performance of the 18dB Isogain ET power cell stimulated with a 20MHz bandwidth (100 RB) LTE signal at 835MHz.

The results with LTE (4G) signals are coherent with the previous simulations. The isogain ET power cell allows satisfying ACPR constraints up to **30.5dBm** with **66%** efficiency while the fixed supply power cell is limited to **27.3dBm** with **37%** average efficiency. As before, the performance of both cells and required $\eta_{modulator}$ are summarized in Table 47.

Table 47: Simulated performance of the ET PA with a 20MHz LTE signal @ 835MHz (ACPR = -35dBc).

	P_{lin}	<PAE> @ P_{lin}	$<PAE_{3dB\ BO}>$	$<PAE_{6dB\ BO}>$	$<PAE_{10dB\ BO}>$
Fixed supply power cell	27.3dBm	37%	38%	25%	12%
ET cell	30.5dBm	66%	56%	46%	31%
Efficiency Improvement	-	+78%	+47%	+84%	+158%
$\eta_{modulator}$	-	>56%	>68%	>54%	>39%

The supply modulator however can have a non negligible impact on the achievable efficiency improvement. In the case of the LTE operation, the modulator should have a minimum efficiency higher than 68% to ensure the overall efficiency is higher than that of the stand-alone cell. Substantial efficiency and linearity improvement can be obtained using envelope tracking and isogain envelope shaping.

IV-3.2. Load Modulation

Similarly to isogain envelope tracking, the cell was simulated in CW with a varying load (LM cell) to obtain a constant gain and the corresponding values of load were store in a Trajectory file. Figure 103compares the efficiency, gain response and phase response of the fixed supply and load power cell with LM cell with isogain trajectory and with LM cell maximized efficiency trajectory.

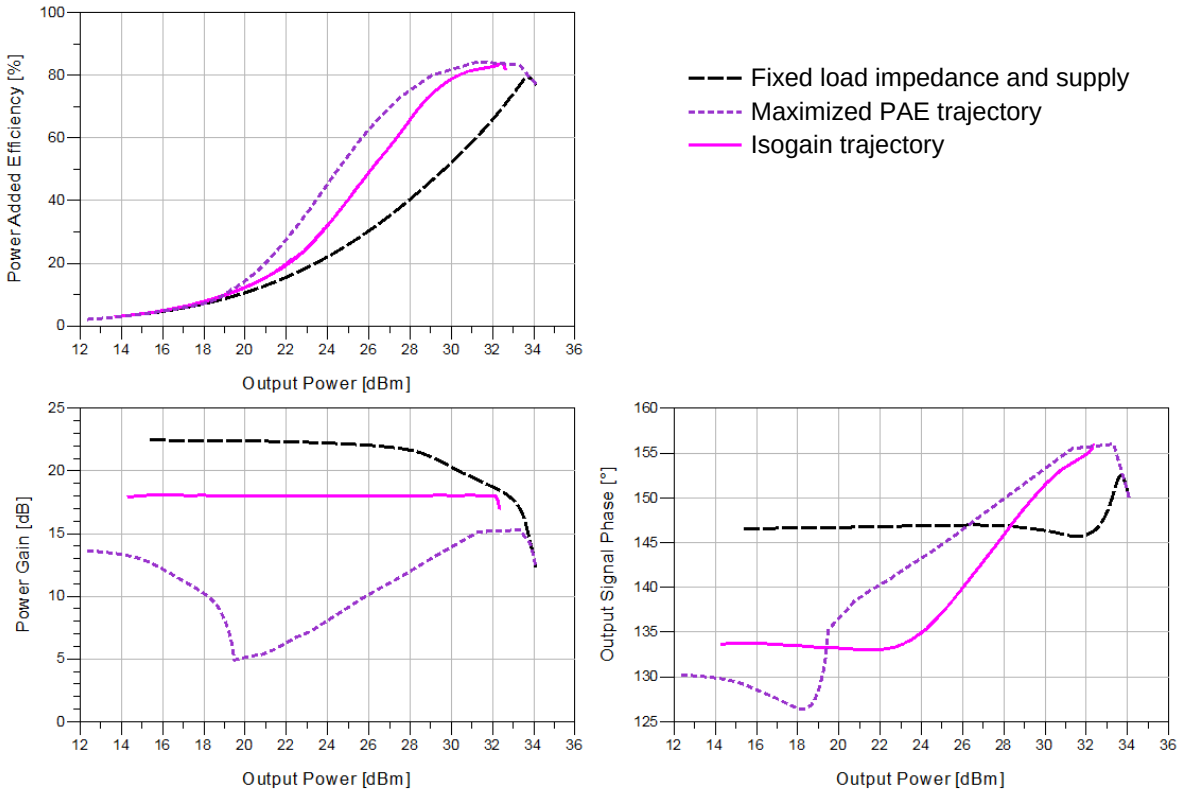

Figure 103: Efficiency (top left), gain (bottom left) and phase (bottom right) comparison between the stand alone cell, LM power cell with maximum efficiency trajectory and LM power cell with isogain trajectory.

The performances obtained with LM cell with isogain trajectory are different from the corresponding ET power cell. Whatever the power level, the efficiency of the LM cell shows a high efficiency improvement. The **18dB** isogain load trajectory has an IP1 at **32.3dBm** with an efficiency of **84%**, which is **23.5%** higher than the fixed supply and load power cell at the same power level. At a **6dB** back-off, the LM power cell efficiency is **51%**, compared to the fixed power cell efficiency about **32%**, which is an improvement of **59%**.

There is however an issue with the phase characteristics of the LM power cell. The phase variations can however be as high as 23° up to 32.3dBm output power. The isogain load trajectory might not be sufficient to ensure linear amplification with high efficiency. In order to verify the linearity of the cell, its response when amplifying a 3G Release'99 signal has been tested.

As for the ET power cell, envelope information is extracted using an envelope detector. A load controller receives the envelope information and the information is then processed using a Trajectory Data file to set the load impedance providing isogain. The simulation results are given in Figure 104.

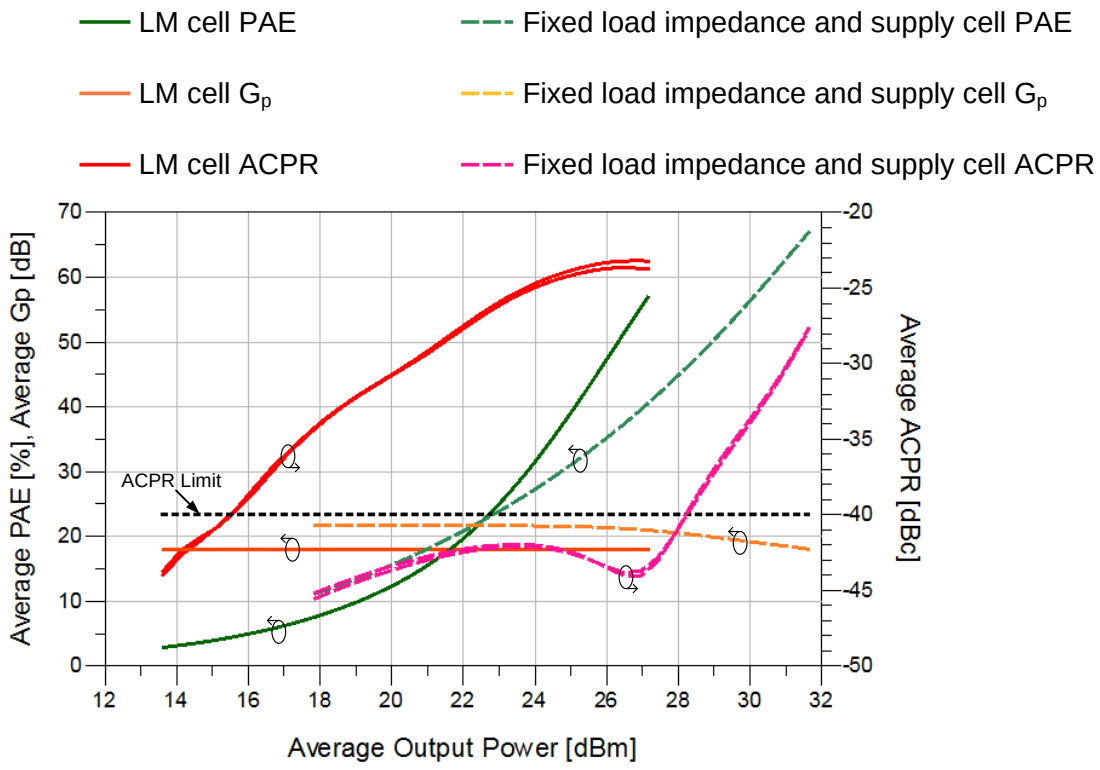

Figure 104: Simulated performance of the 18dB Isogain LM power cell stimulated with a Release'99 signal at 835MHz.

As can be seen on the figure, ACPR does not meet linearity specifications above 15.6dBm. The ACPR may be impacted by the poor AM/PM performance of the LM cell, which is higher than that of the fixed power cell.

These results show that load modulation requires linearization in order to satisfy linearity specifications.

IV-4 Design and implementation of a load modulated PA architecture

In this section, the implementation of a load modulation power cell will be presented. This architecture is designed to address Band 1, from 2.11GHz to 2.17GHz, with a maximum saturated power of 33dBm.

The first part of this section will be dedicated to the choice of the load trajectory, on which the architecture is based. In the second part, the architecture and the implementation of the Tunable Matching Network (TMN) will be described. The simulation results will be shown in the third part before a discussion over the experimental result in the fourth part.

A. Determination of the load trajectory

The architecture is based on the LDMOS power cell previously presented and optimized using the calculations described in Chapter 2 and load pull simulations to operate with maximal efficiency a 33.5dBm. This cell has been characterized over the considered power range to determine the load trajectory. The load trajectory is the set of load impedance leading to optimal efficiency at each power level.

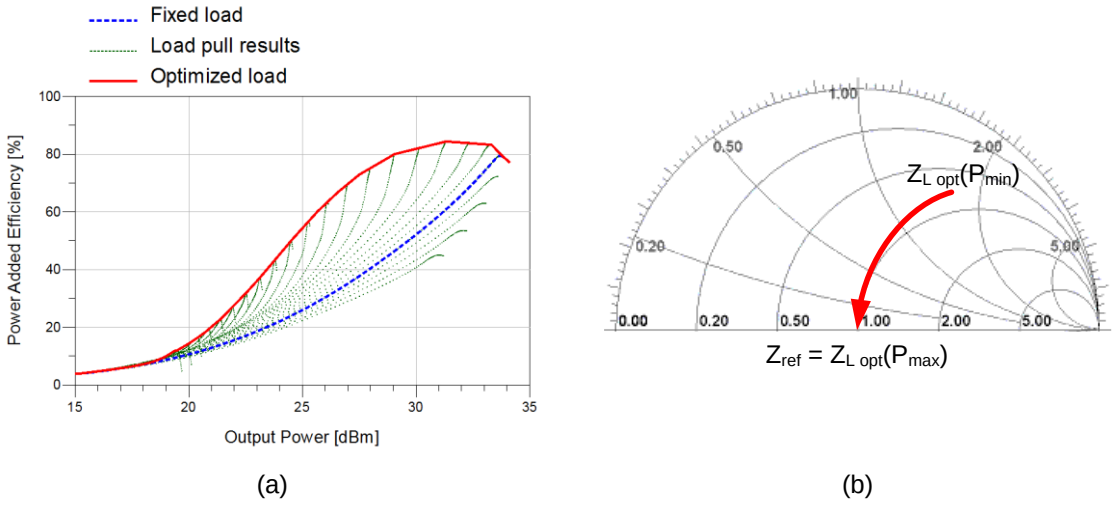

Figure 105: Power added efficiency after load pull simulations (a) and load trajectory for optimal efficiency (b)

Figure 105 (a) shows the PAE results of the load pull simulation (green dots) together with the response of the fixed load power cell (dotted blue line). The red solid line represents the achievable efficiency with variable load impedance for each power level. The corresponding load trajectory is shown in Figure 105 (b).

B. Load Modulation Architecture implementation

The proposed architecture is shown in Figure 106. It is composed of the power cell, matched to an input 50Ω termination thanks to the input matching network. The load trajectory is synthesized thanks to the output matching network. It is composed of a fixed network and a tunable matching network (TMN).

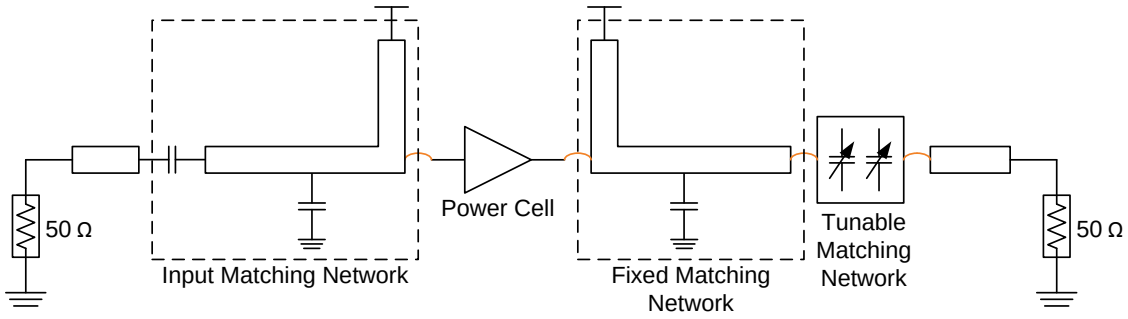

Figure 106: Simplified schematic of the load modulation architecture

The fixed matching network is used to raise the impedance level before the TMN in order to reduce the required tuning range of the capacitors. As will be discussed, higher tuning range for the tunable capacitors leads to higher loss in the output matching network. The following parts will discuss the design of TMN.

a. Requirements

The impedance presented at the input of the TMN is required to cover the load trajectory previously determined. In order to correctly realize this, two tunable capacitors (C_{serial} and $C_{parallel}$) are required, as shown in Figure 107.

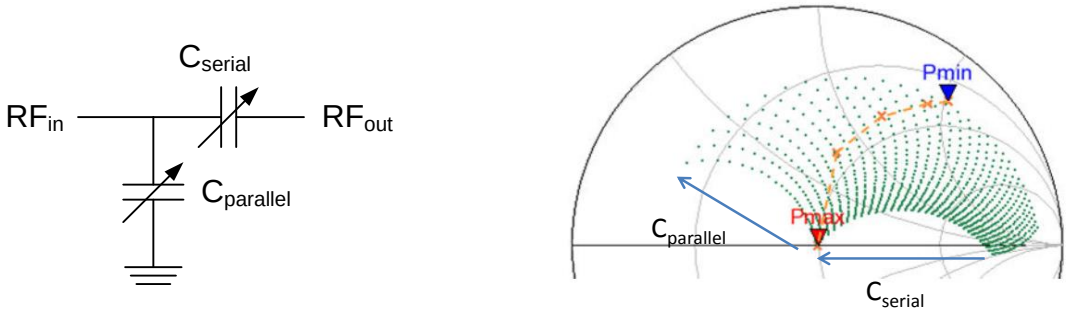

Figure 107: Schematic and simulated states of the tunable matching network (green), Load trajectory (orange) in a smith chart referenced by the optimal load impedance after the fixed matching network

The span of the green dots in the smith chart corresponds to a variation of both capacitors with **0.5pF**<$C_{parallel}$<**2.8pF**and **1.6pF**< C_{serial}<**2.8pF**with minimum quality factor of 50.

b. Design of the tunable capacitors

The tunable capacitors are implemented as binary weighted switched capacitor array. Such switched capacitor array allows the selection of discrete values between a minimum capacitance value (C_{min}) and a maximum capacitance value (C_{max}) [Im13] [Ranta13]. The general schematic of a binary weighted switched capacitor array is given in Figure 108.

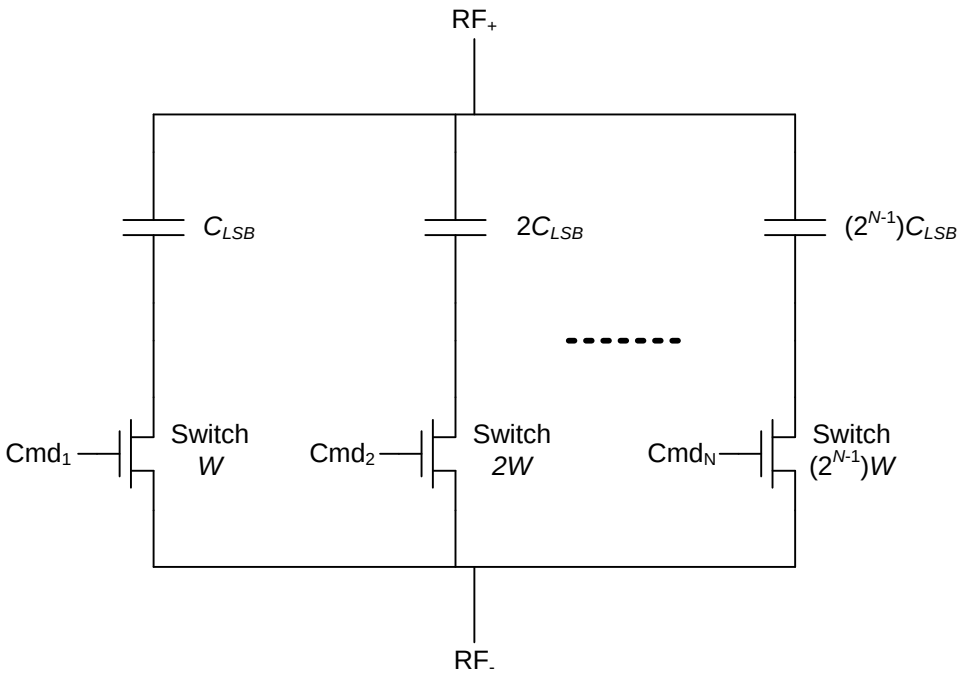

Figure 108: Schematic of a binary weighted switched capacitor array

The number of branches *N* determines the resolution and the number of states N_{states} of the capacitor.

$$N_{states} = 2^N \qquad \text{Equation 85}$$

There is a tradeoff between the tuning ratio *M* of the tuning capacitor and the minimum quality factor Q_{min} for a given technology and operation frequency, as shown in Equation 86 – demonstration in Appendix G.

$$Q_{min} = \frac{Q_C}{1 + (M-1) \cdot Q_C \cdot FOM \cdot \omega_0} \text{ with } M = \frac{C_{max}}{C_{min}} \quad \text{Equation 86}$$

The LSB branch capacitor is calculated according to the following equation.

$$C_{LSB} = \frac{C_{max}}{2^N - 1} \quad \text{Equation 87}$$

For the TMN of the load pull PA, *N*=5 branches of tunable capacitor are required in order to have a sufficient resolution. This leads to 32 states per capacitor as shown in Equation 85. The schematic of a tunable capacitor is reminded in Figure 109.

$$N_{states} = 2^N \quad \text{Equation 88}$$

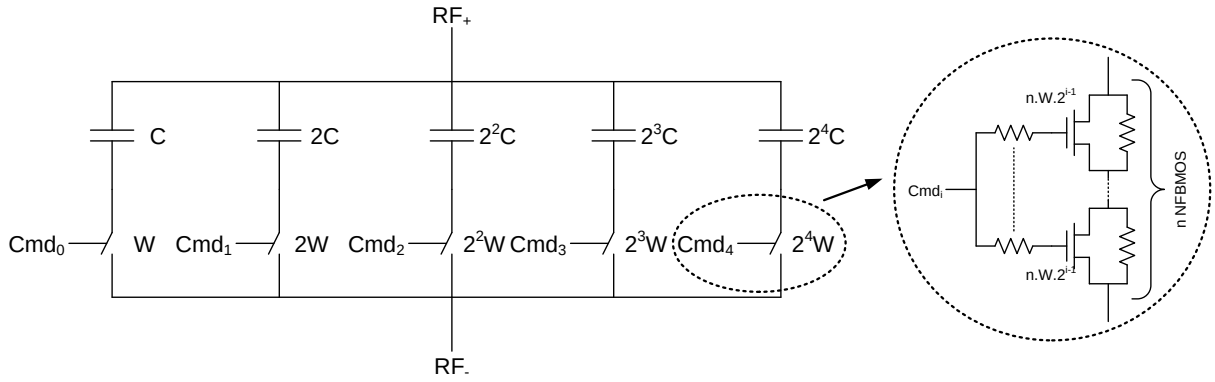

Figure 109: Schematic of binary weighted switched capacitor bank used as a tunable capacitor.

The tuning ratio of the capacitor allows the calculation of the minimal quality factor of the capacitor using Equation 89. From this equation, a graph of the achievable quality factor according to the tuning ratio $M=C_{max}/C_{min}$ and operation frequency considering a technology figure of merit (*FOM*) of **310fs** can be obtained, see Figure 110. From this graph, we can see that to implement a tunable capacitor varying between 0.5 pF and 2.8 pF, with the tuning ratio M of 5.6, the minimum quality factor must be equal to 50 as fixed previously.

$$Q_{min} = \frac{1}{(M-1) \cdot FOM \cdot \omega_0} \; with \; M = \frac{C_{max}}{C_{min}} \quad \text{Equation 89}$$

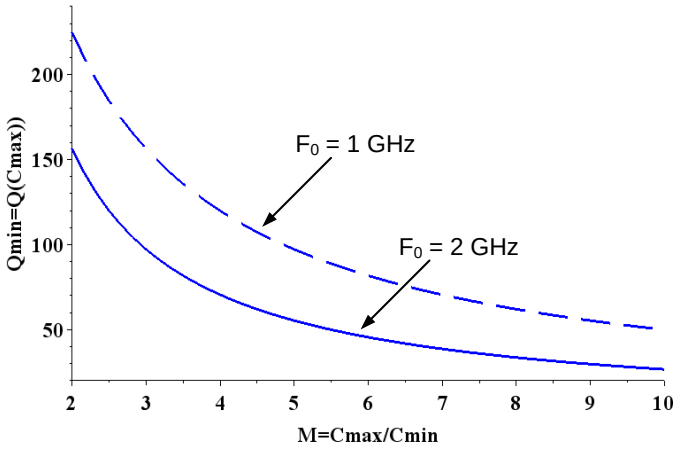

Figure 110: Minimum quality factor of the binary weighted switched capacitor bank according to its tuning ratio and frequency.

The minimum quality factor corresponds to the equivalent quality factor of the tunable capacitor when all the branches are on, giving the maximum capacitance value C_{max}. By setting the same quality factor among all branches, it is possible to size the elements of the branches using the less significant bit (LSB) capacitor. A reminder of the sizing of C_{LSB} and W is given in Equation 90 and Equation 91 respectively.

$$C_{LSB} = \frac{C_{max}}{2^N - 1} \qquad \text{Equation 90}$$

$$W = \frac{\omega_0 \cdot C_{LSB} \cdot Q_c \cdot Q_{min} \cdot R_{on} W}{Q_c - Q_{min}} \qquad \text{Equation 91}$$

Once C_{LSB} and W have been calculated, the number of MOS transistor to stack in the switch is determined to ensure high power handling. The LSB branch is then replicated using weighting coefficients indicated on Figure 109for each branch. The equivalent capacitance and quality factor can afterwards be simulated (Figure 111).

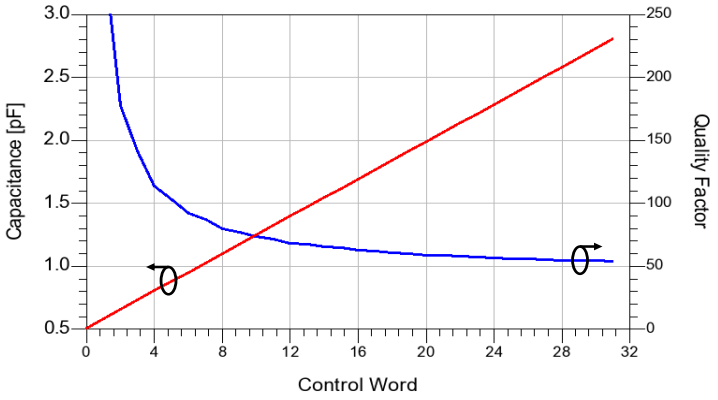

Figure 111: Simulated capacitance and quality factor of a tunable capacitor of the TMN for the 32 control states

On this graph, the equivalent capacitance and quality factor of the tunable capacitance is represented as a function of the integer value of the control word. As can be seen on the figure, the capacitance range is correctly synthesized and the minimum quality factor is 55.

In order to add symmetry in the implementation of the tunable capacitors' chip, both the serial and parallel capacitors are the same. They are integrated together with logic control circuitry, which allows the selection of capacitance values through an integrated SPI interface, in SOI CMOS 130 nm technology. A microphotograph of the die is shown in Figure 112.

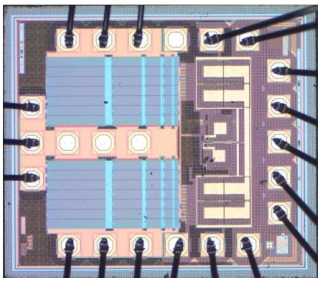

Figure 112: Microphotograph of the TMN die

The simulated performance of the architecture using this tunable capacitor circuit will be discussed in the following paragraph.

C. Simulation results

In order to verify the operation of the architecture, the CW response of the power cell and its matching networks were simulated in large signal at 2.14 GHz under a 4V supply voltage for the 1024 states of the TMN. Figure 113 shows the insertion loss of the TMN according to the state of the network and the output power of the line-up.

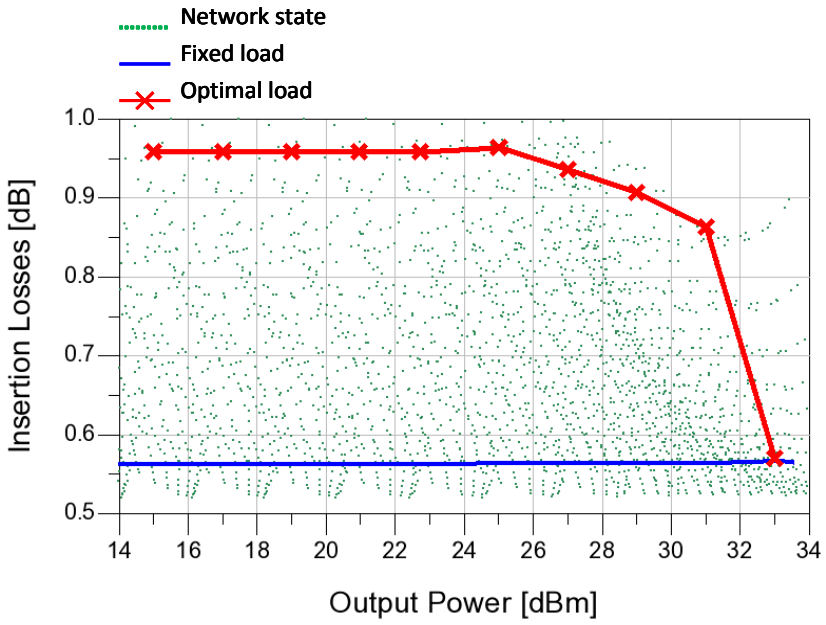

Figure 113: Simulated insertion losses of the Tunable Matching Network in a Continuous Wave simulation

In the picture, the blue curve corresponds to the response of the line-up when the network is configured to maintain the optimal load impedance to the power cell for the maximum output power. In that case, the insertion is kept constant at 0.56dB. When the load is modulated by the TMN, the insertion loss increases but is kept below 1dB. So, compared to a fixed output matching, the reconfiguration of the network adds limited extra loss.

Figure 114 presents the simulated overall efficiency of the amplifier in every configuration (green dots). A maximum efficiency of **65%** is achieved for a peak output power of 33.5dBm. With optimally tuned load (red crossed lines), efficiency is **46%** at **7.5dB** back-off versus **46%** with a fixed load impedance (blue line), which corresponds to a **53%** improvement. The efficiency improvement is higher than 50% for a 6 to 12dB back-off.

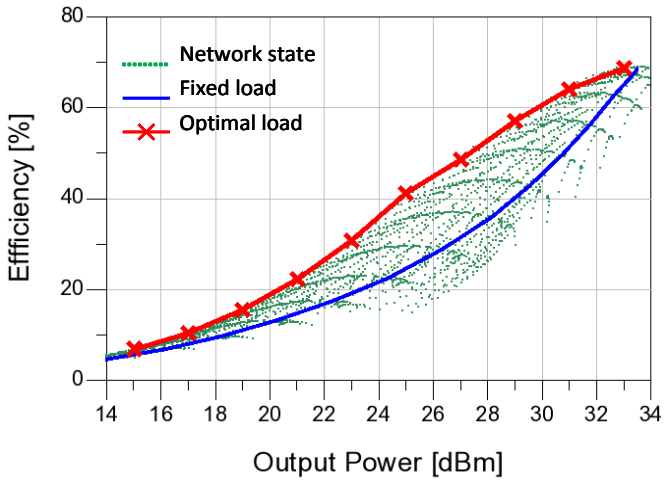

Figure 114: Simulated energy efficiency of the line-up as a function of output power in a Continuous Wave simulation

D. Measured performance

In order to measure the line-up, a test board using Rogers 4003Csubstrate was designed. The input and fixed networks were realized using Co-Planar lines with Ground plane (CPWG) lines, CPWG stubs and SMD capacitors. Both the power cell and TMN dies were mounted using a Chip-On-Board (COB) assembly. The final assembly is presented in Figure 115.

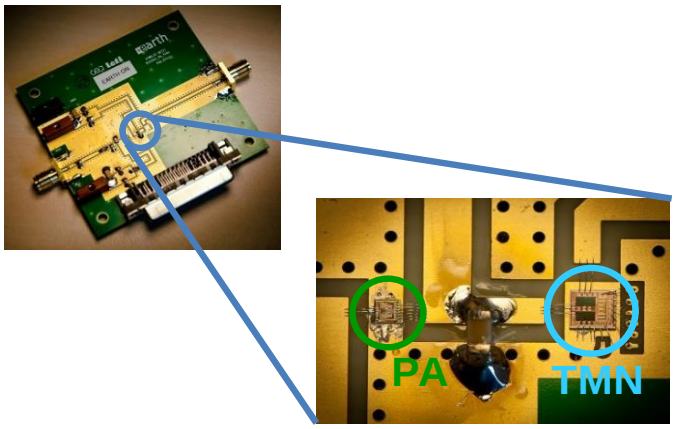

Figure 115: Photograph of the test board (left) with a zoom on the Power Cell and TMN circuits (right)

A comparison between measured and simulated *S* parameters is shown in Figure 116 for a 4V voltage supply and a 110mA quiescent current.

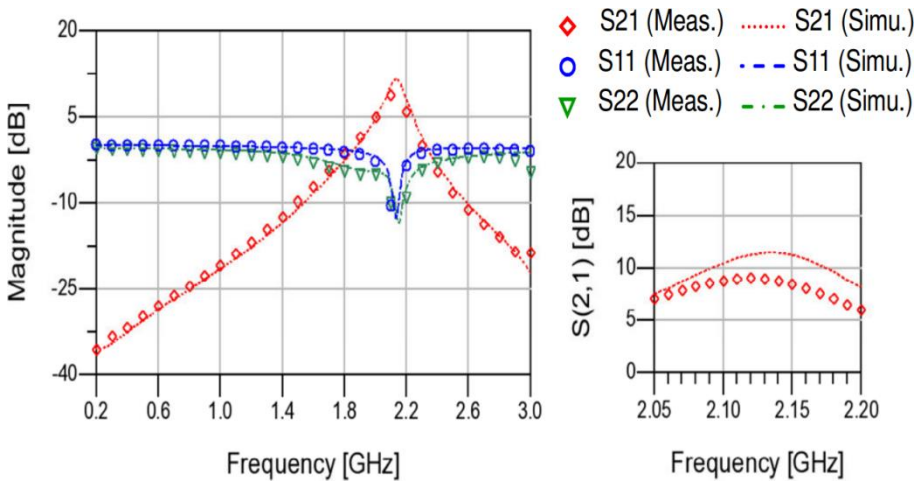

Figure 116: Comparison between measured and simulated S parameters

As can be seen, a good agreement between measurement and simulation is obtained up to 3GHz, except at 2.14 GHz where a 2.5dB difference can be observed on S_{21}. This difference is attributed to the TMN which presents higher loss than expected. Indeed, due to non-optimal layout, the branches of the shunt capacitor present a degraded quality factor value of 30 instead of the expected 50 value.

The measured efficiency is presented in Figure 117. A maximum efficiency of 34% is obtained at a 31.5dBm peak power. By de-embedding the TMN loss, saturated output power of the LDMOS power stage is 33.5dBm with a corresponding drain efficiency of 54%. By tuning the load impedance of the power stage, efficiency is improved by more than 50% for a 6 to 12dB back-off.

The 1.5mW consumption added by the TMN's control block is negligible compared to the overall consumption.

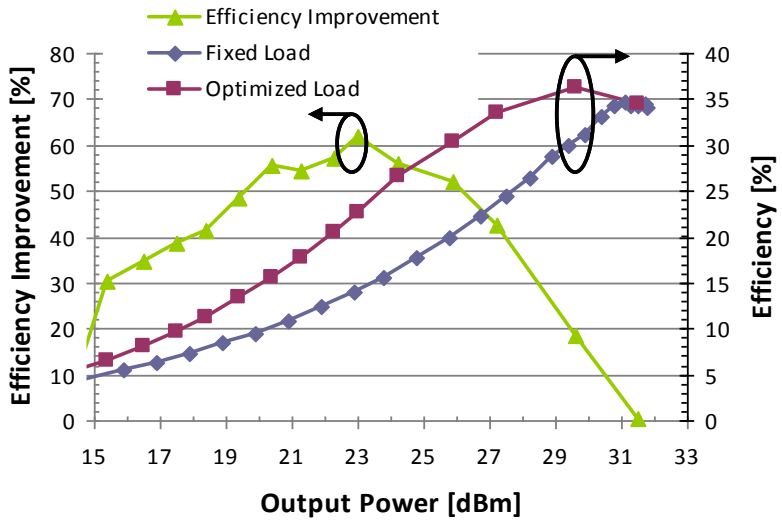

Figure 117: Measured PA efficiency with passive load modulation

Despite higher TMN loss than expected, the proposed PA achieves higher output power and back-off efficiency improvement than previously reported SOI CMOS power amplifier with passive load modulation [Carrara09] as shown in Table 48.

Table 48: Comparison between the proposed amplifier and [5]

Reference	Freq. [GHz]	Pmax [dBm]	Efficiency improvement		
			3dB back-off	7dB back-off	10dB back-off
[Carrara09]	2.4	23.9	30%	34%	20%
This work	2.14	31.5	30%	55%	55%

Incorrect estimation of the layout parasitic of the TMN during the implementation of the overall circuit including the power cell and TMN led to an underestimation of the insertion loss. Consequently, the overall efficiency of the line-up was severely affected, even if the de-embedded performances of the power cell were roughly as expected. Nevertheless, it is important to see the high improvement in back-off efficiency compared to the fixed load configuration.

This study, realized in a static domain does not account for dynamic operation. For dynamic control of the TMN, the synchronization between the input power and TMN control must be ensured and all the capacitors must change simultaneously. If this is not the case, the intermediate states of the TMN can distort the RF signal, which can lead to high EVM.

This means that the speed constraints in the design of the control circuitry can be strong taking into account the consumption requirements in order not to reduce the overall efficiency. Finally, according to the chosen load trajectory, as it was the case for envelope tracking, linearization technique can be required to ensure the low ACLR and low EVM. According to the complexity of the linearization implemented in the architecture, the overall efficiency can, once again, be impacted.

IV-5 Conclusion

In this chapter, PA efficiency enhancement has been studied. The efficiency decreases in traditional power amplifier at back-off. By varying either the supply voltage (envelope tracking technique: ET) or load impedance (load modulation technique: LM), the efficiency can be enhanced. However, both techniques apply to limited back-off ranges.

Concerning envelope tracking, the use of isogain envelope shaping is a way to improve efficiency without resorting to linearization. Simulation results show that this method is particularly efficient when amplifying complex signals such as W-CDMA release 99 and LTE. On the contrary, load modulation using isogain shaping degrades linearity. Therefore, in this case, a linearization technique is mandatory.

A load modulation power amplifier has been designed to assess the feasibility of this technique using the chosen SOI CMOS 130nm technology. After defining the load trajectory, a tunable network topology is chosen in order to adjust the load impedance of the power cell. The tunable capacitors of the tunable network were implemented as binary weighted switched capacitor banks. A prototype was realized and showed promising efficiency enhancement, higher than 50% for back-offs comprised between 6 to 12dB, with a 31.5dBm maximum output power despite higher loss in the tunable network than expected.

As a perspective, the study on high efficiency power amplifiers can be pursued by the study of architecture combining both ET and LM. Before transmission, according to the required average output power, the load of the power amplifier can be actuated thanks to a tunable matching network (static actuation). During the transmission, in order to handle the varying envelope, a supply modulator with isogain envelope shaping can ensure linear amplification of the signal with high efficiency.

IV-6 References

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Conclusion and perspective

In this research work, an original design methodology for saturated and linear PA design which allows pre-sizing of power cells and determination of optimal load impedances for a reconfigurable PA design has been proposed. It has been shown that Class F^{-1} provides high performance for saturated PA design, whereas Class F is best suited for linear PA design. Matching networks are another critical part of reconfigurable PA. In order to make the matching networks reconfigurable, switched capacitor arrays were described and their design methodology presented.

Then, an original reconfigurable MMPA architecture has been proposed and implemented, taking leverage of a SOI CMOS 130nm technology. The proposed solution represents a significant step toward the silicon integration of high performance MMPA and initial measured results illustrate the relevance of the proposed architecture. The measured prototype delivers up to 35dBm and 30dBm of output power in saturated and linear mode respectively, with more than 58% and 47% efficiency respectively. Compared to state of the art, the proposed reconfigurable PA presents higher linear power and efficiency. Concerning the full PA line-up assembly including the reconfigurable MMPA with the reconfigurable output matching network, imprecision in the on-board interface design between both circuits has led to downgraded measured performance. A short term perspective would be the study and redesign of this interface to optimize performances. In addition, this work could be transposed to higher frequency bands in order to design a MMPA module addressing different cellular frequency bands.

In addition, high efficiency PA architectures based on supply and load modulation have been explored. The use of supply or load modulation allows maximizing the efficiency at back-off power but generally at the expense of linearity. By adopting an iso-gain optimization scheme, it has been shown that envelope tracking can provide high efficiency together with high linearity without using complex digital pre-distortion. With load modulation, it has appeared that linearization is necessary whatever the optimization scheme, making it inappropriate for handheld devices for which linearization techniques currently consume too much power. In order to assess the performance of load modulation in SOI CMOS technology, a passive load modulation PA demonstrator for 4Gfemto-cell applications was designed. A SOI CMOS tunable matching network has been design to provide optimal load trajectory to the PA at back-off power. Substantial efficiency improvement was reached with this device. The PA delivers 31.5dBm output power with efficiency improvement higher than 50% for back-off power levels ranging from 7dB to 12dB. This prototype is one of the first SOI CMOS PA delivering watt-level output power with high efficiency improvement at back-off. Perspective for this demonstrator is to optimize the layout of the tunable capacitors to improve the performance. The control circuitry of this device could also be studied and optimized to allow dynamic control of the device. This circuit could take the digital information of the digital front-end and decode it to optimize the configuration of the TMN according to the expected output signal. Another possibility would be to process the envelope of the signal, which would be a challenge in terms of high speed electronics.

The work developed in this thesis is part of a larger research problematic: reduce the cost of RF front-end modules by making its constitutive elements reconfigurable and by integrating them in a low cost technology. The work presented in this thesis can be extended to a larger scope. A first perspective consists in realizing a full high band and low bang reconfigurable multi-mode multi-band power amplifier in a single SOI CMOS module. The design methodology presented in this thesis is also applicable to the high frequency bands, allowing the design of the second line-up. The remaining work would then be an optimization problem of the different elements to achieve the best performance.

The high efficiency techniques should also be added to the full architecture to ensure high efficiency at power back-off. This can be done by adding a three state matching network at the output of both line-up and a high efficiency DC/DC converter. The three states matching network would allow pre-selection of the power level before transmission. The DC/DC converter would be used to implement an iso-gain envelope tracking technique to improve dynamically the efficiency of the device.

Towards a wider interest, the study on reconfiguration could be conducted on the full RF front-end by including the antenna, antenna tuner and switches. A system study with all these elements could reveal combinations of reconfigurable elements that lead to tremendous performance improvements. A co-design strategy would then be mandatory to efficiently exploit this study and create a fully reconfigurable front-end module. As SOI CMOS technology has a lot of potential for the integration of reconfigurable elements, it is logical that the use of this technology can be expanded on the full front-end module. The work presented in this thesis was the first steps towards the full implementation of SOI CMOS reconfigurable cellular RF front-end modules.

Published work

International conferences

[1] **G. TANT**, A. GIRY, P. FERRIS, G. PARES, J.-D. ARNOULD, J.-M. FOURNIER, C. RAYNAUD, P.VINCENT, « A SOI CMOS Reconfigurable Output Matching Network for Multimode Multiband Power Amplifiers », IEEE International Microwave Symposium, 2015.

[2] **G. TANT**, A. GIRY, J.-D. ARNOULD, J.-M. FOURNIER, P.VINCENT, « A 2.14GHz Watt-level Power Amplifier with Passive Load Modulation in a SOI CMOS technology », IEEE European Solid State Circuits Conference, pp. 189-192, 2013.

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National conferences

[4] **G. TANT**, P. FERRIS, A. GIRY, J.-D. ARNOULD, J.-M. FOURNIER, P.VINCENT, « Un réseau d'adaptation reconfigurable en technologie CMOS SOI pour amplificateur de puissance multimode multibandes », Journées Nationales Microondes, Bordeaux, 2015.

[5] P. FERRIS, **G. TANT**, D. PARAT, A. GIRY, J.-D. ARNOULD, J.-M. FOURNIER, « Un amplificateur de Puissance Multimode Multibande reconfigurable en technologie CMOS SOI », Journées Nationales Microondes, Bordeaux, 2015.

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Appendices

Appendix A: Fourier Coefficient Calculations

Useful integrals

The six integrals calculated hereafter will be useful for calculating Fourier coefficients.

- $I_1 = \int_0^{\alpha} \cos^2(\theta)\, d\theta = \int_0^{\alpha} \frac{1+\cos(2\theta)}{2} d\theta = \frac{1}{2}\left(\int_0^{\alpha} d\theta + \int_0^{\alpha} \cos(2\theta)\, d\theta\right)$

$$I_1 = \frac{1}{2}\left(\alpha + \frac{\sin(2\alpha)}{2}\right)$$

- $I_2 = \int_0^{\alpha} \cos^2(2\theta)\, d\theta = \int_0^{\alpha} \frac{1+\cos(4\theta)}{2} d\theta = \frac{1}{2}\left(\int_0^{\alpha} d\theta + \int_0^{\alpha} \cos(4\theta)\, d\theta\right)$

$$I_2 = \frac{1}{2}\left(\alpha + \frac{\sin(4\alpha)}{4}\right)$$

- For $n \neq 1, I_3(n) = \int_0^{\alpha} \cos(\theta)\cos(n\theta)\, d\theta = \int_0^{\alpha} \frac{\cos([n-1]\theta) + \cos([n+1]\theta)}{2} d\theta$
$= \frac{1}{2}\left(\int_0^{\alpha} \cos([n-1]\theta)\, d\theta + \int_0^{\alpha} \cos([n+1]\theta)\, d\theta\right)$

$$I_3(n) = \frac{1}{2}\left(\frac{\sin([n-1]\alpha)}{n-1} + \frac{\sin([n+1]\alpha)}{n+1}\right) \text{ with } n \neq 1$$

- For $n \neq 2, I_4(n) = \int_0^{\alpha} \cos(2\theta)\cos(n\theta)\, d\theta = \int_0^{\alpha} \frac{\cos([n-2]\theta) + \cos([n+2]\theta)}{2} d\theta$
$= \frac{1}{2}\left(\int_0^{\alpha} \cos([n-2]\theta)\, d\theta + \int_0^{\alpha} \cos([n+2]\theta)\, d\theta\right)$

$$I_4(n) = \frac{1}{2}\left(\frac{\sin([n-2]\alpha)}{n-2} + \frac{\sin([n+2]\alpha)}{n+2}\right) \text{ with } n \neq 2$$

- For $n \neq 2, I_5(n) = \int_0^\alpha \cos^2(\theta)\cos(n\theta)\,d\theta = \int_0^\alpha \frac{1+\cos(2\theta)}{2}\cos(n\theta)\,d\theta$
$= \frac{1}{2}\left(\int_0^\alpha \cos(n\theta)\,d\theta + \int_0^\alpha \cos(2\theta)\cos(n\theta)\,d\theta\right) = \frac{1}{2}\left(\frac{\sin(n\alpha)}{n} + I_4(n)\right)$

$$I_5(n) = \frac{1}{2}\left(\frac{\sin(n\alpha)}{n} + \frac{1}{2}\left(\frac{\sin([n-2]\alpha)}{n-2} + \frac{\sin([n+2]\alpha)}{n+2}\right)\right) \text{ with } n \neq 2$$

- $I_5(1) = \int_0^\alpha cos^2(\theta)\,cos(\theta)\,d\theta = \frac{1}{2}\left(sin(\alpha) + \frac{1}{2}\left(\frac{sin(3\theta)}{3} - sin(-\alpha)\right)\right) = \frac{1}{2}\left(\frac{3}{2}sin(\alpha) + \frac{1}{2}\left(\frac{sin(3\alpha)}{3}\right)\right)$

$$I_5(1) = \frac{1}{4}\left(3\sin(\alpha) + \frac{\sin(3\alpha)}{3}\right)$$

- $I_6 = \int_0^\alpha \cos^2(\theta)\cos(2\theta)\,d\theta = \int_0^\alpha \frac{1+\cos(2\theta)}{2}\cos(2\theta)\,d\theta = \frac{1}{2}\left(\int_0^\alpha \cos(2\theta)\,d\theta + \int_0^\alpha \cos^2(2\theta)\,d\theta\right)$
$= \frac{1}{2}\left(\frac{\sin(2\alpha)}{2} + I_2\right) = \frac{1}{2}\left(\frac{\sin(2\alpha)}{2} + \frac{1}{2}\left(\alpha + \frac{\sin(4\alpha)}{4}\right)\right)$

$$I_6 = \frac{1}{4}\left(\alpha + \sin(2\alpha) + \frac{\sin(4\alpha)}{4}\right)$$

Half raised sine wave

Consider the periodic function *H* with a period π, defined over [-π ; π] as follows:

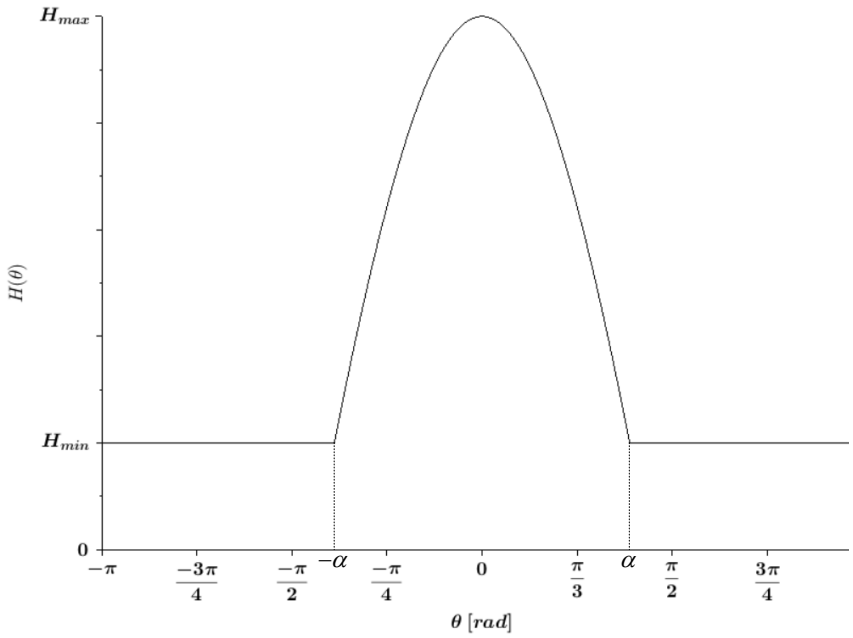
$$H(\theta)\begin{cases} A_H\cos(\theta)+B_H \text{for } |\theta|\le\alpha \\ H_{min} \text{ for } |\theta|>\alpha \end{cases}$$

With

$$A_H=\frac{H_{max}-H_{min}}{1-\cos(\alpha)}$$

And

$$B_H=\frac{H_{min}-H_{max}\cos(\alpha)}{1-\cos(\alpha)}$$



Note that *H* is even. Therefore calculation of the Fourier coefficients can be simplified by calculating integrals over [0 ; π] instead of [-π ; π]. Moreover, there are only cosine components and no sine components in the calculation of the coefficients.

- The DC coefficient is calculated as follows.

$$H_0(\alpha)=\frac{1}{\pi}\int_0^{\pi}H(\theta)\,d\theta=\frac{1}{\pi}\left(\int_0^{\alpha}(A_H\cos(\theta)+B_H)\,d\theta+\int_{\alpha}^{\pi}H_{min}\,d\theta\right)$$

$$H_0(\alpha)=\frac{1}{\pi}(A_H\sin(\alpha)+B_H\alpha+H_{min}[\pi-\alpha])$$

Note that if $H_{min}=0$, we obtain

$$A_H=\frac{H_{max}}{1-\cos(\alpha)}\ \text{and}B_H=\frac{-H_{max}\cos(\alpha)}{1-\cos(\alpha)}=-A_H\cos(\alpha)$$

Therefore

$$H_0(\alpha)=\frac{1}{\pi}(A_H\sin(\alpha)-A_H\alpha\cos(\alpha))=\frac{A_H}{\pi}[\sin(\alpha)-\alpha\cos(\alpha)]$$

$$\text{if } H_{min}=0 \text{ then } H_0(\alpha)=\frac{H_{max}}{\pi(1-\cos(\alpha))}(\sin(\alpha)-\alpha\cos(\alpha))$$

- The fundamental coefficient is calculated as follows.

$$H_1(\alpha) = \frac{2}{\pi}\int_0^{\pi} H(\theta)\cos(\theta)\,d\theta = \frac{2}{\pi}\left(\int_0^{\alpha}(A_H\cos^2(\theta) + B_H\cos(\theta))\,d\theta + \int_{\alpha}^{\pi} H_{min}\cos(\theta)\,d\theta\right)$$
$$= \frac{2}{\pi}\left(A_H I_1 + \int_0^{\alpha} B_H\cos(\theta)\,d\theta + \int_{\alpha}^{\pi} H_{min}\cos(\theta)\,d\theta\right)$$

$$H_1(\alpha) = \frac{2}{\pi}\left(\frac{A_H}{2}\left(\alpha + \frac{\sin(2\alpha)}{2}\right) + B_H\sin(\alpha) - H_{min}\sin(\alpha)\right)$$

Note that if $H_{min}=0$, we obtain

$$A_H = \frac{H_{max}}{1-\cos(\alpha)} \text{ and} B_H = \frac{-H_{max}\cos(\alpha)}{1-\cos(\alpha)} = -A_H\cos(\alpha)$$

Therefore

$$H_1(\alpha) = \frac{2}{\pi}\left(\frac{A_H}{2}\left(\alpha + \frac{\sin(2\alpha)}{2}\right) - A_H\sin(\alpha)\cos(\alpha)\right) = \frac{2A_H}{\pi}\left(\frac{1}{2}\left(\alpha + \frac{\sin(2\alpha)}{2}\right) - \frac{\sin(2\alpha)}{2}\right)$$
$$= \frac{A_H}{\pi}\left(\alpha + \frac{\sin(2\alpha)}{2} - \sin(2\alpha)\right)$$

$$\text{if } H_{min} = 0 \text{ then } H_1(\alpha) = \frac{H_{max}}{\pi(1-\cos(\alpha))}\left(\alpha - \frac{\sin(2\alpha)}{2}\right)$$

- The n^{th} harmonic coefficient is calculated as follows.

$$H_n(\alpha) = \frac{2}{\pi}\int_0^{\pi} H(\theta)\cos(n\theta)\,d\theta = \frac{2}{\pi}\left(\int_0^{\alpha} A_H\cos(\theta)\cos(n\theta) + B_H\cos(n\theta)\,d\theta + \int_{\alpha}^{\pi} H_{min}\cos(n\theta)\,d\theta\right)$$
$$= \frac{2}{\pi}\left(A_H I_3(n) + \int_0^{\alpha} B_H\cos(n\theta)\,d\theta + \int_{\alpha}^{\pi} H_{min}\cos(n\theta)\,d\theta\right)$$

$$H_n(\alpha) = \frac{2}{\pi}\left(\frac{A_H}{2}\left(\frac{\sin([n-1]\alpha)}{n-1} + \frac{\sin([n+1]\alpha)}{n+1}\right) + B_H\frac{\sin(n\alpha)}{n} - H_{min}\frac{\sin(n\alpha)}{n}\right)$$

Note that if $H_{min}=0$, we obtain

$$A_H = \frac{H_{max}}{1-\cos(\alpha)} \text{ and} B_H = \frac{-H_{max}\cos(\alpha)}{1-\cos(\alpha)} = -A_H\cos(\alpha)$$

Therefore

$$H_n(\alpha) = \frac{2}{\pi}\left(\frac{A_H}{2}\left(\frac{\sin([n-1]\alpha)}{(n-1)} + \frac{\sin([n+1]\alpha)}{(n+1)}\right) - A_H\cos(\alpha)\frac{\sin(n\alpha)}{n}\right)$$
$$= \frac{A_H}{\pi}\left(\frac{\sin([n-1]\alpha)}{(n-1)} + \frac{\sin([n+1]\alpha)}{(n+1)} - \frac{2\cos(\alpha)\sin(n\alpha)}{n}\right)$$

$$\text{if } H_{min} = 0 \text{ then } H_n(\alpha) = \frac{H_{max}}{\pi(1-\cos(\alpha))}\left(\frac{\sin([n-1]\alpha)}{(n-1)} + \frac{\sin([n+1]\alpha)}{(n+1)} - \frac{2\cos(\alpha)\sin(n\alpha)}{n}\right)$$

Half squared sine wave

Consider the periodic function *Q* with a period π, defined over [-π ; π] as follows:

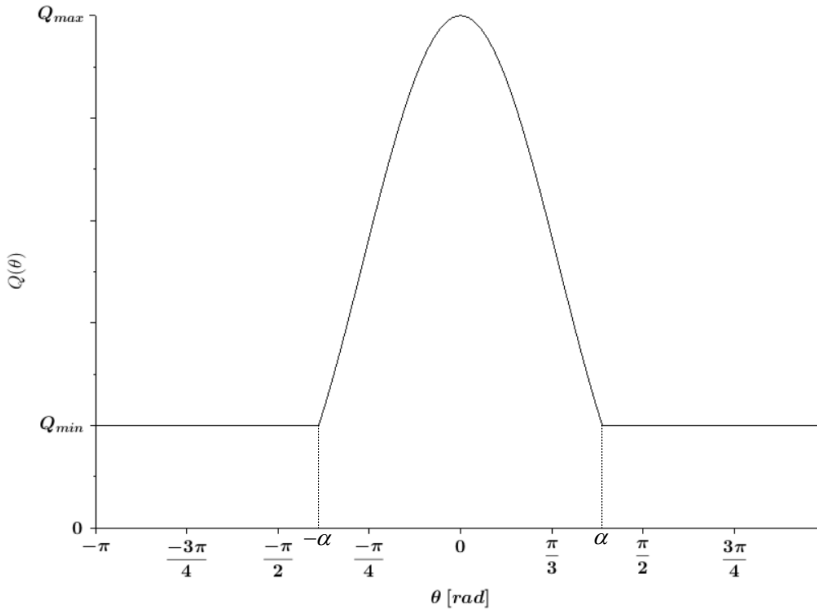
$$Q(\theta)\begin{cases}\left(A_Q\cos(\theta)+B_Q\right)^2 \text{for } |\theta|\le\alpha\\ Q_{min} \text{ for } |\theta|>\alpha\end{cases}$$

With

$$A_Q=\frac{\sqrt{Q_{max}}-\sqrt{Q_{min}}}{1-\cos(\alpha)}$$

And

$$B_Q=\frac{\sqrt{Q_{min}}-\sqrt{Q_{max}}\cos(\alpha)}{1-\cos(\alpha)}$$



Note that *Q* is even. Therefore calculation of the Fourier coefficients can be simplified by calculating integrals over [0 ; π] instead of [-π ; π]. Moreover, there are only cosine components and no sine components in the calculation of the coefficients.

- The DC coefficient is calculated as follows.

$$Q_0(\alpha)=\frac{1}{\pi}\int_0^{\pi}Q(\theta)\,d\theta=\frac{1}{\pi}\left(\int_0^{\alpha}A_Q^2\cos^2(\theta)+2A_QB_Q\cos(\theta)+B_Q^2\,d\theta+\int_{\alpha}^{\pi}Q_{min}\,d\theta\right)$$

$$=\frac{1}{\pi}\left(A_Q^2I_1+\int_0^{\alpha}2A_QB_Q\cos(\theta)\,d\theta+\int_0^{\alpha}B_Q^2\,d\theta+\int_{\alpha}^{\pi}Q_{min}\,d\theta\right)$$

$$Q_0(\alpha)=\frac{1}{\pi}\left(\frac{A_Q^2}{2}\left(\alpha+\frac{\sin(2\alpha)}{2}\right)+2A_QB_Q\sin(\alpha)+B_Q^2\alpha+Q_{min}[\pi-\alpha]\right)$$

Note that if $Q_{min}=0$, we obtain

$$A_Q=\frac{\sqrt{Q_{max}}}{1-\cos(\alpha)}\ \text{and}B_Q=\frac{-\sqrt{Q_{max}}\cos(\alpha)}{1-\cos(\alpha)}=-A_Q\cos(\alpha)$$

Therefore

$$Q_0(\alpha)=\frac{1}{\pi}\left(\frac{A_Q^2}{2}\left(\alpha+\frac{\sin(2\alpha)}{2}\right)-2A_Q^2\cos(\alpha)\sin(\alpha)+A_Q^2\cos^2(\alpha)\,\alpha\right)$$

$$=\frac{A_Q^2}{\pi}\left(\frac{\alpha}{2}+\frac{\sin(2\alpha)}{4}-\sin(2\alpha)+\alpha\frac{1+\cos(2\alpha)}{2}\right)=\frac{A_Q^2}{2}\left(\frac{\alpha}{2}+\frac{\alpha}{2}-\frac{3\sin(2\alpha)}{4}+\alpha\cos(2\alpha)\right)$$

$$\text{if } Q_{min} = 0 \text{ then } Q_0(\alpha) = \frac{Q_{max}}{\pi(1-\cos(\alpha))^2} \cdot \left(\alpha - \frac{3\sin(2\alpha)}{4} + \frac{\alpha\cos(2\alpha)}{2}\right)$$

- The fundamental coefficient is calculated as follows.

$$\begin{aligned} Q_1(\alpha) &= \frac{2}{\pi}\int_0^{\pi} Q(\theta)\cos(\theta)\,d\theta \\ &= \frac{2}{\pi}\left(\int_0^{\alpha} A_Q^2\cos^2(\theta)\cos(\theta) + 2A_Q B_Q\cos^2(\theta) + B_Q^2\cos(\theta)\,d\theta + \int_{\alpha}^{\pi} Q_{min}\cos(\theta)\,d\theta\right) \\ &= \frac{2}{\pi}\left(A_Q^2 I_5(1) + 2A_Q B_Q I_1 + \int_0^{\alpha} B_Q^2\cos(\theta)\,d\theta + \int_{\alpha}^{\pi} Q_{min}\cos(\theta)\,d\theta\right) \end{aligned}$$

$$Q_1(\alpha) = \frac{2}{\pi}\left(\frac{A_Q^2}{4}\left(3\sin(\alpha) + \frac{\sin(3\alpha)}{3}\right) + A_Q B_Q\left(\alpha + \frac{\sin(2\alpha)}{2}\right) + B_Q^2\sin(\alpha) - Q_{min}\sin(\alpha)\right)$$

Note that if $Q_{min}=0$, we obtain

$$A_Q = \frac{\sqrt{Q_{max}}}{1-\cos(\alpha)} \text{ and} B_Q = \frac{-\sqrt{Q_{max}}\cos(\alpha)}{1-\cos(\alpha)} = -A_Q\cos(\alpha)$$

Therefore

$$\begin{aligned} Q_1(\alpha) &= \frac{2}{\pi}\left(\frac{A_Q^2}{4}\left(3\sin(\alpha) + \frac{\sin(3\alpha)}{3}\right) - A_Q^2\cos(\alpha)\left(\alpha + \frac{\sin(2\alpha)}{2}\right) + A_Q^2\cos^2(\alpha)\sin(\alpha)\right) \\ &= \frac{2A_Q^2}{\pi}\left(\frac{3}{4}\sin(\alpha) + \frac{\sin(3\alpha)}{12} - \alpha\cos(\alpha) - \frac{\sin(2\alpha)\cos(\alpha)}{2} + \sin(\alpha)\cos^2(\alpha)\right) \\ &= \frac{2A_Q^2}{\pi}\left(\frac{3}{4}\sin(\alpha) + \frac{\sin(3\alpha)}{12} - \alpha\cos(\alpha) - \sin(\alpha)\cos^2(\alpha) + \sin(\alpha)\cos^2(\alpha)\right) \end{aligned}$$

$$\text{if } Q_{min} = 0 \text{ then } Q_1(\alpha) = \frac{2Q_{max}}{\pi(1-\cos(\alpha))^2}\left(\frac{3}{4}\sin(\alpha) - \alpha\cos(\alpha) + \frac{\sin(3\alpha)}{12}\right)$$

- The 2nd harmonic coefficient is calculated as follows.

$$Q_2(\alpha) = \frac{2}{\pi}\int_0^{\pi} H(\theta)\cos(2\theta)\,d\theta$$

$$= \frac{2}{\pi}\left(\int_0^{\alpha} A_Q^2\cos^2(\theta)\cos(2\theta) + 2A_QB_Q\cos(\theta)\cos(2\theta) + B_Q^2\cos(2\theta)\,d\theta + \int_{\alpha}^{\pi} Q_{min}\cos(2\theta)\,d\theta\right)$$

$$= \frac{2}{\pi}\left(A_Q^2 I_6 + 2A_QB_QI_3(2) + \int_0^{\alpha} B_Q^2\cos(2\theta)\,d\theta + \int_{\alpha}^{\pi} Q_{min}\cos(2\theta)\,d\theta\right)$$

$$Q_2(\alpha) = \frac{2}{\pi}\left(\frac{A_Q^2}{4}\left(\alpha + \sin(2\alpha) + \frac{\sin(4\alpha)}{4}\right) + A_QB_Q\left(\sin(\alpha) + \frac{\sin(3\alpha)}{3}\right) + B_Q^2\frac{\sin(2\alpha)}{2} - Q_{min}\frac{\sin(2\alpha)}{2}\right)$$

Note that if $Q_{min}=0$, we obtain

$$A_Q = \frac{\sqrt{Q_{max}}}{1-\cos(\alpha)} \text{ and} B_Q = \frac{-\sqrt{Q_{max}}\cos(\alpha)}{1-\cos(\alpha)} = -A_Q\cos(\alpha)$$

Therefore

$$Q_2(\alpha) = \frac{2}{\pi}\left(\frac{A_Q^2}{4}\left(\alpha + \sin(2\alpha) + \frac{\sin(4\alpha)}{4}\right) - A_Q^2\cos(\alpha)\left(\sin(\alpha) + \frac{\sin(3\alpha)}{3}\right) + A_Q^2\cos^2(\alpha)\frac{\sin(2\alpha)}{2}\right)$$

$$= \frac{2A_Q^2}{\pi}\left(\frac{\alpha}{4} + \frac{\sin(2\alpha)}{4} + \frac{\sin(4\alpha)}{16} - \cos(\alpha)\sin(\alpha) - \frac{\cos(\alpha)\sin(3\alpha)}{3} + \frac{(1+\cos(2\alpha))\sin(2\alpha)}{4}\right)$$

$$= \frac{2A_Q^2}{\pi}\left(\frac{\alpha}{4} + \frac{\sin(2\alpha)}{4} + \frac{\sin(4\alpha)}{16} - \frac{\sin(2\alpha)}{2} - \frac{\cos(\alpha)\sin(3\alpha)}{3} + \frac{\sin(2\alpha)}{4} + \frac{\cos(2\alpha)\sin(2\alpha)}{4}\right) = \frac{2A_Q^2}{\pi}\left(\frac{\alpha}{4} + \frac{\sin(4\alpha)}{16} - \frac{\sin(2\alpha)}{6} - \frac{\sin(4\alpha)}{6} + \frac{\sin(4\alpha)}{8}\right)$$

$$= \frac{2A_Q^2}{\pi}\left(\frac{\alpha}{4} - \frac{\sin(2\alpha)}{6} + \frac{\sin(4\alpha)}{48}\right)$$

$$\text{if } Q_{min} = 0 \text{ then } Q_{n2}(\alpha) = \frac{2Q_{max}}{\pi(1-\cos(\alpha))^2}\left(\frac{\alpha}{4} - \frac{\sin(2\alpha)}{6} + \frac{\sin(4\alpha)}{48}\right)$$

- The n^{th} harmonic coefficient is calculated as follows.

$$Q_n(\alpha) = \frac{2}{\pi}\left(\int_0^{\alpha} A_Q^2\cos^2(\theta)\cos(n\theta) + 2A_QB_Q\cos(\theta)\cos(n\theta) + B_Q^2\cos(n\theta)\,d\theta + \int_{\alpha}^{\pi} Q_{min}\cos(n\theta)\,d\theta\right)$$

$$= \frac{2}{\pi}\left(A_Q^2 I_5(n) + 2A_QB_QI_3(n) + \int_0^{\alpha} B_Q^2\cos(n\theta)\,d\theta + \int_{\alpha}^{\pi} H_{min}\cos(n\theta)\,d\theta\right)$$

$$Q_n(\alpha)=\frac{2}{\pi}\left(\frac{A_Q^2}{2}\left(\frac{\sin(n\alpha)}{n}+\frac{1}{2}\left(\frac{\sin([n-2]\alpha)}{n-2}+\frac{\sin([n+2]\alpha)}{n+2}\right)\right)+A_QB_Q\left(\frac{\sin([n-1]\alpha)}{n-1}+\frac{\sin([n+1]\alpha)}{n+1}\right)+B_Q^2\frac{\sin(n\alpha)}{n}-H_{min}\frac{\sin(n\alpha)}{n}\right)$$

Note that if $Q_{min}=0$, we obtain

$$A_Q=\frac{\sqrt{Q_{max}}}{1-\cos(\alpha)}\ \text{and}B_Q=\frac{-\sqrt{Q_{max}}\cos(\alpha)}{1-\cos(\alpha)}=-A_Q\cos(\alpha)$$

Therefore

$$\begin{aligned}Q_n(\alpha)=&\frac{2}{\pi}\left(\frac{A_Q^2}{2}\left(\frac{\sin(n\alpha)}{n}+\frac{1}{2}\left(\frac{\sin([n-2]\alpha)}{n-2}+\frac{\sin([n+2]\alpha)}{n+2}\right)\right)\right.\\&\left.-A_Q^2\cos(\alpha)\left(\frac{\sin([n-1]\alpha)}{n-1}+\frac{\sin([n+1]\alpha)}{n+1}\right)+A_Q^2\cos^2(\alpha)\frac{\sin(n\alpha)}{n}\right)\\&=\frac{2A_Q^2}{\pi}\left(\frac{\sin(n\alpha)}{2n}+\frac{1}{4}\left(\frac{\sin([n-2]\alpha)}{n-2}+\frac{\sin([n+2]\alpha)}{n+2}\right)\right.\\&\left.-\cos(\alpha)\left(\frac{\sin([n-1]\alpha)}{n-1}+\frac{\sin([n+1]\alpha)}{n+1}\right)+\frac{(1+\cos(2\alpha))\sin(n\alpha)}{2n}\right)\\&=\frac{2A_Q^2}{\pi}\left(\frac{\sin(n\alpha)}{n}+\frac{1}{4}\left(\frac{\sin([n-2]\alpha)}{n-2}+\frac{\sin([n+2]\alpha)}{n+2}\right)\right.\\&\left.-\left(\frac{\sin([n-1]\alpha)\cos(\alpha)}{n-1}+\frac{\sin([n+1]\alpha)\cos(\alpha)}{n+1}\right)+\frac{\sin(n\alpha)\cos(2\alpha)}{2n}\right)\\&=\frac{2A_Q^2}{\pi}\left(\frac{\sin(n\alpha)}{n}+\frac{1}{4}\left(\frac{\sin([n-2]\alpha)}{n-2}+\frac{\sin([n+2]\alpha)}{n+2}\right)\right.\\&-\left(\frac{\sin(n\alpha)+\sin([n-2]\alpha)}{2(n-1)}+\frac{\sin([n+2]\alpha)+\sin(n\alpha)}{2(n+1)}\right)\\&\left.+\frac{\sin([n-2]\alpha)+\sin([n+2]\alpha)}{4n}\right)\\&=\frac{2A_Q^2}{\pi}\left(\sin(n\alpha)\left[\frac{1}{n}-\frac{1}{2(n-1)}-\frac{1}{2(n+1)}\right]+\sin([n-2]\alpha)\left[\frac{1}{4n}-\frac{1}{2(n-1)}-\frac{1}{4(n-2)}\right]\right.\\&\left.+\sin([n+2]\alpha)\left[\frac{1}{4n}-\frac{1}{2(n+1)}-\frac{1}{4(n+2)}\right]\right)\\&=\frac{2A_Q^2}{\pi}\left(-\sin(n\alpha)\frac{1}{n(n^2-1)}+\sin([n-2]\alpha)\frac{1}{2n(n-1)(n-2)}\right.\\&\left.+\sin([n+2]\alpha)\frac{1}{2n(n+1)(n+2)}\right)\\&=\frac{2A_Q^2}{\pi}\left(\frac{(4-n^2)\sin(n\alpha)+\frac{(n+1)(n+2)\sin([n-2]\alpha)}{2}+\frac{(n-1)(n-2)\sin([n+2]\alpha)}{2}}{n(n^2-1)(n^2-4)}\right)\\&=\frac{2A_Q^2}{\pi}\left(\frac{(4-n^2)\sin(n\alpha)++\frac{(n-1)(n-2)(\sin([n+2]\alpha)+\sin([n-2]\alpha))}{2}+3n\sin([n-2]\alpha)}{n(n^2-1)(n^2-4)}\right)\end{aligned}$$

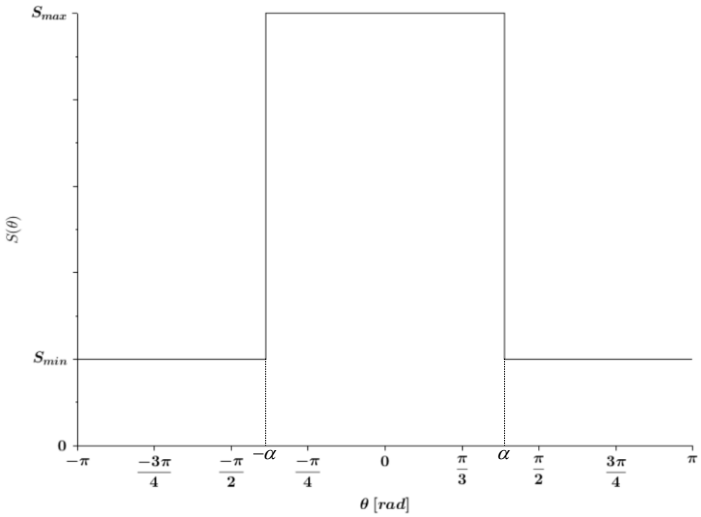
if $Q_{min}=0$ then

$$Q_n(\alpha)=\frac{H_{max}}{\pi(1-\cos(\alpha))}\left(\frac{(4-n^2)\sin(n\alpha)+(n-1)(n-2)\sin(n\alpha)\cos(\varphi)+3n\sin\big((n-2)\alpha\big)}{n(n^2-1)(n^2-4)}\right)$$

Square wave

Consider the periodic function *S* with a period π, defined over [-π ; π] as follows:

$$S(\theta)\begin{cases} S_{max} \text{for } |\theta| \leq \alpha \\ S_{min} \text{ for } |\theta| > \alpha \end{cases}$$



Note that *S* is even. Therefore calculation of the Fourier coefficients can be simplified by calculating integrals over [0 ; π] instead of [-π ; π]. Moreover, there are only cosine components and no sine components in the calculation of the coefficients.

- The DC coefficient is calculated as follows.

$$S_0(\alpha) = \frac{1}{\pi}\int_0^{\pi} S(\theta)\, d\theta = \frac{1}{\pi}\left(\int_0^{\alpha} S_{max}\, d\theta + \int_{\alpha}^{\pi} S_{min}\, d\theta\right)$$

$$S_0(\alpha) = \frac{1}{\pi}(S_{max}\alpha + S_{min}[\pi - \alpha])$$

Note that if $S_{min}=0$, we obtain:

$$\text{if } S_{min} = 0 \text{ then } S_0(\alpha) = \frac{S_{max}}{\pi}\alpha$$

- The fundamental coefficient is calculated as follows.

$$S_1(\alpha) = \frac{2}{\pi}\int_0^{\pi} S(\theta)\cos(\theta)\, d\theta = \frac{2}{\pi}\left(\int_0^{\alpha} S_{max}\cos(\theta)\, d\theta + \int_{\alpha}^{\pi} S_{min}\cos(\theta)\, d\theta\right)$$

$$S_1(\alpha) = \frac{2}{\pi}(S_{max}\sin(\alpha) - S_{min}\sin(\alpha))$$

Note that if $S_{min}=0$, we obtain:

$$\text{if } S_{min} = 0 \text{ then } S_1(\alpha) = \frac{2S_{max}}{\pi}\sin(\alpha)$$

- The n^{th} harmonic coefficient is calculated as follows.

$$S_n(\alpha) = \frac{2}{\pi}\int_0^{\pi} S(\theta)\cos(n\theta)\,d\theta = \frac{2}{\pi}\left(\int_0^{\alpha} S_{max}\cos(n\theta)\,d\theta + \int_{\alpha}^{\pi} S_{min}\cos(n\theta)\,d\theta\right)$$

$$S_n(\alpha) = \frac{2}{\pi}\left(S_{max}\frac{\sin(n\alpha)}{n} - S_{min}\frac{\sin(n\alpha)}{n}\right)$$

Note that if $S_{min}=0$, we obtain:

$$\text{if } S_{min} = 0 \text{ then } S_n(\alpha) = \frac{2S_{max}}{n\pi}\sin(n\alpha)$$

Appendix B: Current and voltage coefficients calculation in non-sinusoidal classes

Class F

In class F, the current wave form is defined by function $H(\theta)$ for $\alpha = \pi/2$ and $H_{min} = 0$.

Therefore

- $I_{ds}[0] = H_0\left(\frac{\pi}{2}\right) = \frac{H_{max}}{\pi} = \frac{I_{max}}{\pi}$

$$I_{ds}[0] = \frac{I_{max}}{\pi}$$

- $I_{ds}[f_0] = H_1\left(\frac{\pi}{2}\right) = \frac{H_{max}}{\pi} \cdot \frac{\pi}{2} = \frac{I_{max}}{2}$

$$I_{ds}[f_0] = \frac{I_{max}}{2}$$

In class F, the voltage wave form is defined by function $S(\theta)$ for $\alpha = \pi/2$. Moreover, $V_{DS}[0]$ is forced to V_{DD} by the supply and $S_{min}=V_k$ due to the on-state resistance of the transistor.

Therefore

- $V_{ds}[0] = S_0\left(\frac{\pi}{2}\right) = \frac{1}{\pi}\left(S_{max}\frac{\pi}{2} + S_{min}\frac{\pi}{2}\right) = \frac{S_{max} + V_k}{2} = V_{DD}$

Therefore

$$S_{max} = 2V_{DD} - V_k$$

- $V_{ds}[f_0] = S_1\left(\frac{\pi}{2}\right) = \frac{2}{\pi}(S_{max} - S_{min}) = \frac{2}{\pi}(2V_{DD} - V_k - V_k) = \frac{4}{\pi}(V_{DD} - V_k)$

$$V_{ds}[f_0] = \frac{4}{\pi}(V_{DD} - V_k)$$

Class F-1

In class F-1, the current wave form is defined by function $S(\theta)$ for $\alpha = \pi/2$ and $S_{min} = 0$.

Therefore

- $I_{ds}[0] = S_0\left(\frac{\pi}{2}\right) = \frac{1}{\pi} \cdot S_{max}\frac{\pi}{2} = \frac{I_{max}}{2}$

$$I_{ds}[0] = \frac{I_{max}}{2}$$

- $I_{ds}[f_0] = S_1\left(\frac{\pi}{2}\right) = \frac{2S_{max}}{\pi} = \frac{2I_{max}}{\pi}$

$$I_{ds}[f_0] = \frac{2I_{max}}{\pi}$$

In class F, the voltage wave form is defined by function $H(\theta)$ for $\alpha = \pi/2$. Moreover, $V_{DS}[0]$ is forced to V_{DD} by the supply and $H_{min}=V_k$ due to the on-state resistance of the transistor.

Therefore

- $V_{ds}[0] = H_0\left(\frac{\pi}{2}\right) = \frac{1}{\pi}\left(A_H + B_H\frac{\pi}{2} + H_{min}\frac{\pi}{2}\right) = \frac{1}{\pi}\left(H_{max} - H_{min} + H_{min}\frac{\pi}{2} + H_{min}\frac{\pi}{2}\right)$
$= \frac{H_{max}}{\pi} + \frac{(\pi-1)}{\pi}V_k = V_{DD}$

Therefore

$H_{max} = \pi V_{DD} - (\pi - 1)V_k$

Then

$A_H = \pi V_{DD} - (\pi - 1)V_k - V_k = \pi V_{DD} - \pi V_k + V_k - V_k$

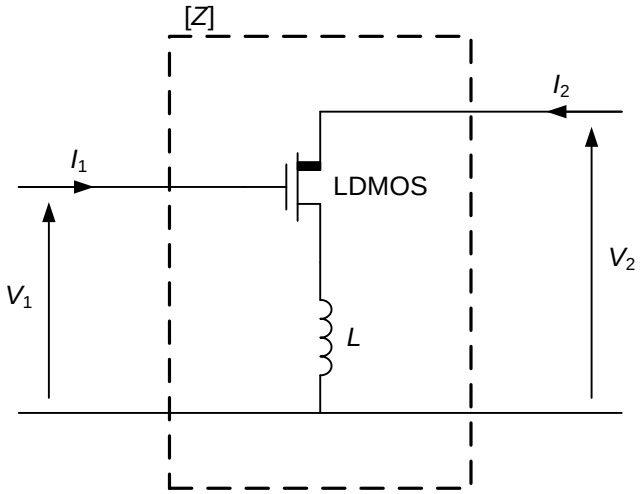
$$A_H = \pi(V_{DD} - V_k) \text{ and} B_H = V_k$$

- $V_{ds}[f_0] = H_1\left(\frac{\pi}{2}\right) = \frac{2}{\pi}\left(\frac{A_H}{2} \cdot \frac{\pi}{2} + B_H - H_{min}\right) = \frac{A_H}{2} + V_k - V_k = \frac{\pi(V_{DD} - V_k)}{2}$

$$V_{ds}[f_0] = \frac{\pi}{2}(V_{DD} - V_k)$$

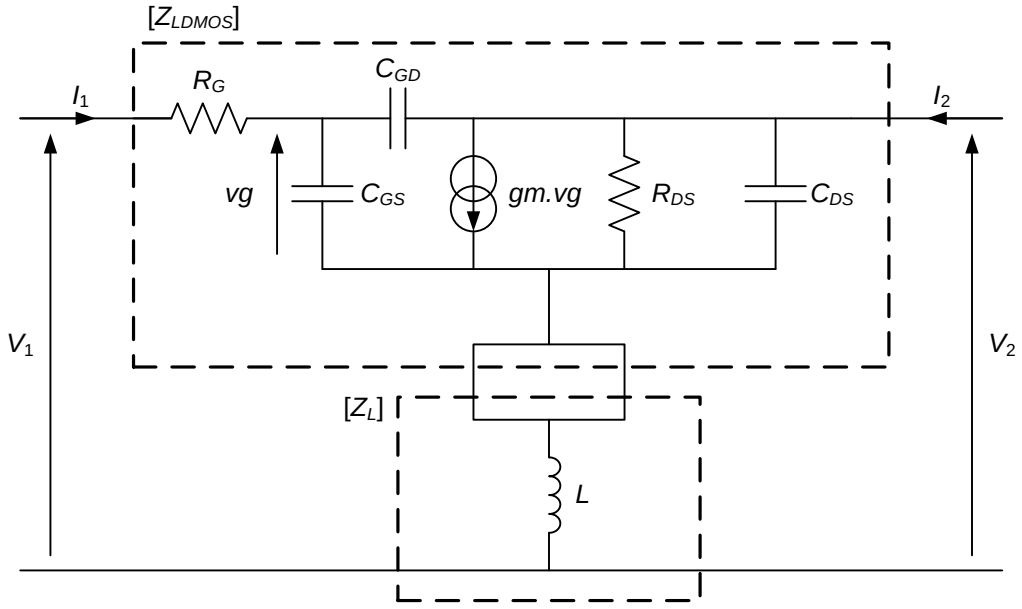
Appendix C: Determination of the input impedance of a transistor according to the degeneration inductance

Consider the following schematic, where [*Z*] is the impedance matrix of the circuit.



$$[Z] = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$$

We can analyze the following equivalent schematic for the transistor, with [Z_{LDMOS}] is the impedance matrix of the transistor and [Z_L] is the impedance matrix the degeneration inductance.



The input impedance of the device can then be calculated according the parameters of [*Z*] and the load impedance Z_{load}

$$Z_{in} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22} - Z_{load}}$$

The degeneration inductance *L* is part of both the input and output meshes, therefore creating a series feedback. Parameters of [*Z*] can then be obtained as

$$[Z] = [Z_L] + [Z_{LDMOS}]$$

Nodal analysis leads to

$$[Z_L] = \begin{bmatrix} jL\omega & jL\omega \\ jL\omega & jL\omega \end{bmatrix}$$

And

$$[Z_{LDMOS}] = \begin{bmatrix} Z_{LDMOS_{11}} & Z_{LDMOS_{12}} \\ Z_{LDMOS_{21}} & Z_{LDMOS_{22}} \end{bmatrix}$$

With

$$Z_{LDMOS_{11}} = R_G + \frac{1}{j\omega\left[\left(C_{gs} + C_{gd}\right) + \frac{C_{gd}(gm - j\omega C_{gd})}{g_{DS} + j\omega(C_{ds} + C_{gd})}\right]}$$

$$Z_{LDMOS_{12}} = \frac{C_{gd}}{g_{DS} + j\omega\left(C_{ds} + C_{gd}\right)} \cdot \frac{1}{\left(C_{gs} + C_{gd}\right) + \frac{C_{gd}(gm - j\omega C_{gd})}{g_{DS} + j\omega(C_{ds} + C_{gd})}}$$

$$Z_{LDMOS_{21}} = -\frac{gm - j\omega C_{gd}}{j\omega\left[g_{DS} + j\omega\left(C_{ds} + C_{gd}\right)\right]} \cdot \frac{1}{\left(C_{gs} + C_{gd}\right) + \frac{C_{gd}(gm - j\omega C_{gd})}{g_{DS} + j\omega(C_{ds} + C_{gd})}}$$

$$Z_{LDMOS_{22}} = -\frac{C_{gs} + C_{gd}}{g_{DS} + j\omega\left(C_{ds} + C_{gd}\right)} \cdot \frac{1}{\left(C_{gs} + C_{gd}\right) + \frac{C_{gd}(gm - j\omega C_{gd})}{g_{DS} + j\omega(C_{ds} + C_{gd})}}$$

By considering that C_{GD} is negligible, we obtain

$$[Z] = \begin{bmatrix} R_G + \frac{1}{j\omega C_{gs}} + jL\omega & jL\omega \\ -\frac{gm \cdot R_{DS}}{j\omega C_{gs}} + jL\omega & R_{DS} + jL\omega \end{bmatrix}$$

Therefore

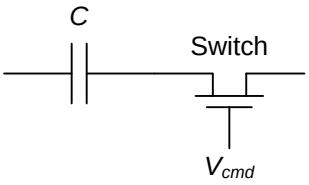
$$Z_{in} = R_G + \frac{1}{j\omega C_{gs}} + jL\omega - \frac{jL\omega\left(jL\omega - \frac{gm \cdot R_{DS}}{j\omega C_{gs}}\right)}{R_{DS} + jL\omega - Z_{load}}$$

Considering $R_{DS} >> Z_{load}$ and $R_{DS} >> L\omega$, we finally obtain

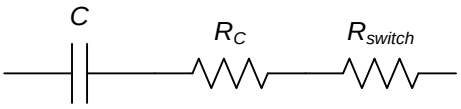
$$Z_{in} = R_G + \frac{gm \cdot L}{C_{gs}} + jL\omega\left(1 - \frac{1}{LC_{gs}\omega^2}\right)$$

Appendix D: Calculation of the required transistor width in a switched capacitor branch

Consider the following schematic of a switched capacitor branch.



We need to determine the width of the transistor used as a switch in order to ensure a sufficient quality factor for the branch (Q_{branch}). Note that Q_{branch} is minimal when the switch is turned on thanks to the control voltage V_{cmd}. In that configuration, we have the following equivalent schematic.



R_C is the parasitic resistance of capacitor C, defined by its quality factor Q_C as follows:

$$R_C = \frac{1}{2\pi f_0 Q_C C}$$

R_{switch} is the on-state of the switch defined according to the transistor width (W_{SW}) and the technology parameter $R_{on}W$ as follows:

$$R_{switch} = \frac{R_{on}W}{W_{SW}}$$

To ensure the value of Q_{branch}, we need:

$$R_C + R_{switch} = \frac{1}{2\pi f_0 Q_{branch} C}$$

Therefore

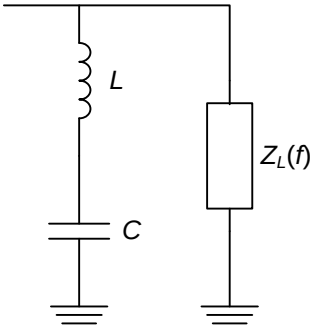
$$R_{switch} = \frac{1}{2\pi f_0 Q_{branch} C} - R_C = \frac{1}{2\pi f_0 Q_{branch} C} - \frac{1}{2\pi f_0 Q_C C} = \frac{Q_C - Q_{branch}}{2\pi f_0 Q_C Q_{branch} C} = \frac{R_{on}W}{W_{SW}}$$

And finally

$$W_{SW} = \frac{2\pi f_0 Q_C Q_{branch} C \cdot R_{on}W}{Q_C - Q_{branch}}$$

Appendix E: Determination of the capacitance of a second harmonic trap not interfering with the fundamental impedance

Consider the following configuration.



L and *C* form a harmonic trap that resonates at f_{res} defined as two times the fundamental frequency f_0. We therefore have

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} = 2f_0$$

The impedance of the trap is defined as

$$Z_{trap}(f) = j2\pi fL - \frac{j}{2\pi fC} = \frac{-j}{2\pi fC}(1 - LC(2\pi f)^2) = \frac{-j}{2\pi fC}\left(1 - \left(\frac{2\pi f}{2\pi f_{res}}\right)^2\right) = \frac{-j}{2\pi fC}\left(1 - \left(\frac{f}{f_{res}}\right)^2\right)$$

If we want $|Z_{trap}(f_0)|=10|Z_L(f_0)|$, then

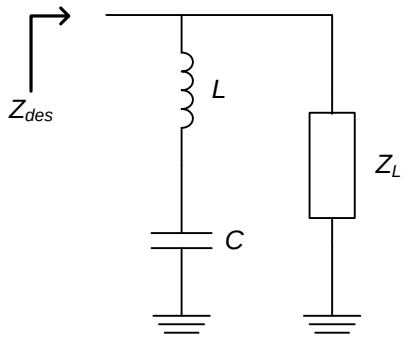
$$Z_{trap}(f_0) = \frac{1}{2\pi fC}\left(1 - \left(\frac{f_0}{f_{res}}\right)^2\right) = 10|Z_L(f_0)| = \frac{1}{2\pi fC}\left(1 - \left(\frac{1}{2}\right)^2\right) = \frac{1}{2\pi fC}\cdot\frac{3}{4} = \frac{3}{8\pi fC}$$

Therefore

$$C = \frac{3}{80\pi f|Z_L(f_0)|}$$

Appendix F: Calculation of the trap capacitor according to the trap inductance and parallel impedance

Consider the following schematic



L and *C* form a harmonic trap. Z_{des} is defined as

$$Z_{des} = \frac{Z_{trap} \cdot Z_L}{Z_{trap} + Z_L} \text{ with } Z_{trap} = j2\pi fL - \frac{j}{2\pi fC}$$

Therefore

$$Z_{trap} = \frac{Z_L \cdot Z_{des}}{Z_L - Z_{des}} = j\left(2\pi fL - \frac{1}{2\pi fC}\right)$$

So

$$2\pi fC = \frac{1}{2\pi fL - |Z_{trap}|}$$

Then

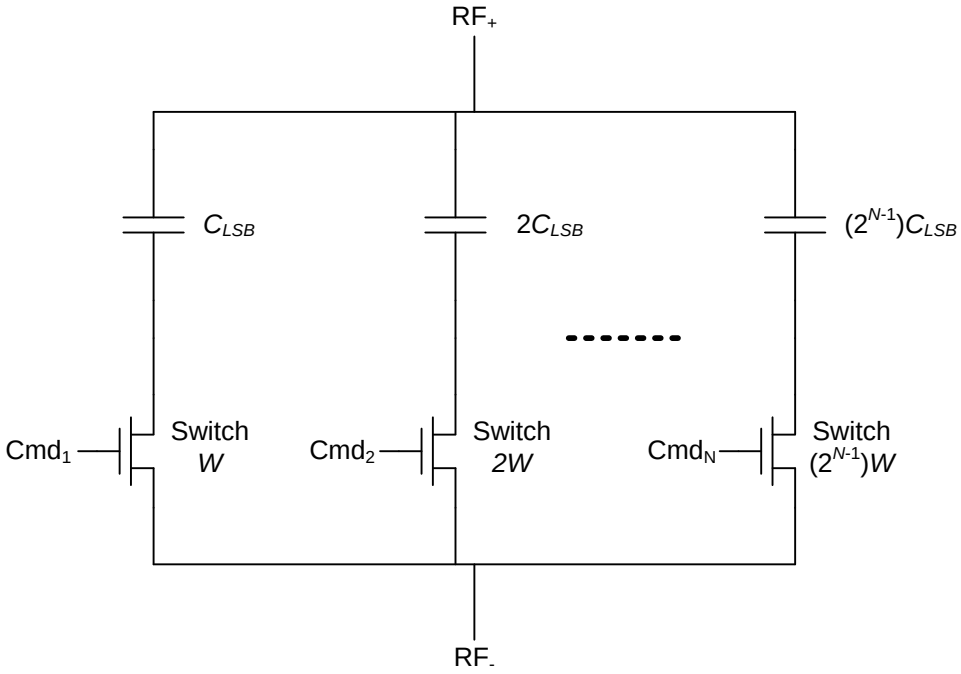
$$C = \frac{1}{2\pi f\left(2\pi fL - |Z_{trap}|\right)}$$

Otherwise

$$C = \frac{1}{2\pi f\left(2\pi fL - \left|\frac{Z_L \cdot Z_{des}}{Z_L - Z_{des}}\right|\right)}$$

Appendix G: Calculation of the minimum Q-factor of a binary weighted switched capacitor bank

Consider the binary weighted switched capacitor bank depicted in the schematic below.



The maximum capacitance is obtained when all the branches are activated. Therefore

$$C_{max} = \sum_{n=1}^{N} 2^{n-1} C_{LSB} = (2^N - 1) C_{LSB}$$

The minimum capacitance value is obtained when all the branches are deactivated. Therefore:

$$C_{min} = \sum_{n=1}^{N} 2^{n-1} \frac{C_{LSB} C_{off}}{C_{LSB} + C_{off}} = (2^N - 1) \frac{C_{LSB} C_{off}}{C_{LSB} + C_{off}}$$

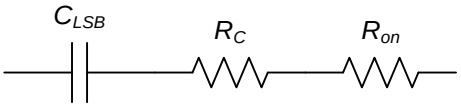
We then have

$$\frac{C_{max}}{C_{min}} = M = \frac{(2^N - 1) C_{LSB}}{(2^N - 1) \frac{C_{LSB} C_{off}}{C_{LSB} + C_{off}}} = \frac{C_{LSB}\left(C_{LSB} + C_{off}\right)}{C_{LSB} C_{off}} = \frac{C_{LSB}}{C_{off}} + 1$$

Therefore

$$\frac{C_{LSB}}{C_{off}} = M - 1$$

The minimum quality factor (Q_{min}) is equal to the quality factor of one branch in on-state. For instance, if we consider the first branch, when in on-state we have the following equivalent schematic.



We have

$$R_C = \frac{1}{2\pi f_0 Q_C C_{LSB}} = \frac{1}{\omega_0 Q_C C_{LSB}}$$

The minimum quality factor is then

$$Q_{min} = \frac{1}{\omega_0 (R_C + R_{on}) C_{LSB}} = \frac{1}{\omega_0 \left(\frac{1}{\omega_0 Q_C C_{LSB}} + R_{on}\right) C_{LSB}} = \frac{1}{\frac{1}{Q_C} + \omega_0 R_{on} C_{LSB}} = \frac{Q_C}{1 + \omega_0 Q_C R_{on} C_{LSB}}$$
$$= \frac{Q_C}{1 + \omega_0 Q_C R_{on} C_{LSB} \frac{C_{off}}{C_{off}}} = \frac{Q_C}{1 + \omega_0 Q_C R_{on} C_{off} \frac{C_{LSB}}{C_{off}}}$$

And finally

$$Q_{min} = \frac{Q_C}{1 + \omega_0 Q_C FOM (M - 1)}$$

Figure index

Table index

List of acronyms and abbreviations

ACPR	Adjacent Channel Power Ratio
ACLR	Adjacent Channel Leakage Ratio
AltCPR	Alternate Channel Power Ratio
AltCLR	Alternate Channel Leakage Ratio
AM	Amplitude Modulation
AM/AM	Amplitude to Amplitude distortion
AM/PM	Amplitude to Phase distortion
AMPS	Advanced Mobile Phone System
BAW	Bulk Acoustic Wave
BW	Bandwidth
BO	Back-off
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DPX	Duplex Filter
EDGE	Enhanced Data-rates for GSM Evolution
EER	Envelope Elimination and Restoration
ETPA	Envelope Tracking PA
ETSI	European Telecommunications Standard Institute
E-UTRA	Evolved Universal Terrestrial Radio Access
EVM	Error Vector Magnitude
FEM	Front-End Module
FDD	Frequency-Division Duplexing
FRN	Frequency Reconfigurable Network
GaAs	Gallium Arsenide
GSM	Global System for Mobile
GMSK	Gaussian Minimum Shift Keying
GPRS	General Packet Radio Service
HB	High Band
HEPA	High Efficiency Power Amplifier
HSPA	High Speed Packet Access
HSPA+	Evolved HSPA
HSDPA	High Speed Packet Downlink Access
HSUPA	High Speed Packet Uplink Access
IEEE	Institute of Electrical and Electronics Engineers
IL	Insertion Loss
IMD_3	3rd order Inter-Modulation product
IS-95	Interim Standard 95
LB	Low Band
LDMOS	Laterally Diffused Metal Oxide Semiconductor (transistor)
Lin.	Linear (Mode)
LNA	Low Noise Amplifier
LTE	Long Term Evolution
LTE-A	LTE-Advanced
LMPA	Load Modulation Power Amplifier
MB	Mid-band
MIM	Metal Insulator Metal (capacitor)
MIMO	Multiple Input Multiple Output
MMPA	Multi-mode multi-band power amplifier
MOM	Metal Oxide Metal (capacitor)
MOS	Metal Oxide Semiconductor (transistor)
OFDMA	Orthogonal Frequency Division Multiple Access
OMN	Output Matching Network
PA	Power Amplifier
PAM	Power Amplifier Module
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
PM	Phase Modulation
Q	Quality factor
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RB	Resource Block
RF	Radiofrequency
RX	Reception Path
RMN	Reconfigurable Matching Network
Sat.	Saturated (Mode)
SAW	Surface Acoustic Wave
Si	Silicon
SMD	Surface Mounted Device
SOI	Silicon on Insulator
SPnT	Single Pole n Throw(s)
TACS	Total Access Communication System
TDD	Time-Division Duplexing

TDMA	Time Division Multiple Access
TMN	Tunable Matching Network
TSV	Through Silicon Via
TRX	Transmission / Reception Path
TX	Transmission Path
UMTS	Universal Mobile Telecommunications System
VHB	Very High Band
VLB	Very Low Band
VLSI	Very Large Scale Modulation
VoIP	Voice over Internet Protocol
W-CDMA	Wideband Code Division Multiple Access
WiMAX	World interoperability for Microwave Access

Abstract

This work focuses on the study and integration of a reconfigurable multi-mode multi-band power amplifier (MMPA) supporting 2G/3G/4G at several frequency bands in SOI CMOS 130nm technology. Current hybrid MMPA modules take advantage of multiple technologies, in particular GaAs for power devices. This adds to the cost and complexity of radiofrequency front-end modules. The original solution presented in this thesis is a significant step toward the integration of MMPA compared to the state of the art and initial results illustrates the relevance of the proposed architecture. A study on PA efficiency under 3G / 4G modulated signals is also presented by comparing load and supply modulation PA architectures.

First, the context and state of the art are presented. A design methodology based on the study of different operating classes is then presented, which allows pre-sizing of power cells and optimal load impedance determination for high efficiency reconfigurable PA design.

The proposed PA design methodology led to the implementation of PA demonstrators integrated in SOI CMOS 130nm technology. The first demonstrator is a two stage reconfigurable MMPA operating from 700MHz to 900MHz and supporting saturated and linear modes. The power stage comprises two SOI LDMOS power cells that are activated according to the desired mode. Tunable matching networks based on switched capacitor arrays allow optimization of the MMPA performance according to the mode and band. The measured prototype delivers up to 35dBm of output power in saturated mode with more than 58% efficiency. In linear mode, the measured output power exceeds 30dBm with efficiency higher than 47%. Compared to initial simulations, some differences were observed. In particular, underestimation of losses associated with MOM capacitors and sub-optimal interconnections are the root cause of the observed discrepancies.

The second demonstrator is a passive load modulation PA architecture. It includes a SOI LDMOS power cell and a tunable matching network made of high power binary weighted switched capacitor arrays. The tunable matching network allows presenting an optimal load trajectory to the PA in order to maximize its back-off efficiency. Measured efficiency enhancement is higher than 55% compared to a fixed load configuration for 7dB to 11dB power back-offs.

Keywords: *Power Amplifiers (PA), multi-mode multi-bande PA (MMPA), reconfigurable PA, SOI CMOS, LDMOS*

Résumé

Cette thèse porte sur l'étude et l'intégration en technologie SOI CMOS d'un circuit amplificateur de puissance multimode multibande (MMPA) reconfigurable capable d'adresser les modes 2G/3G/4G sur plusieurs bandes de fréquences. Les modules MMPA actuels (modules hybrides) reposent sur l'utilisation de plusieurs technologies, en particulier la technologie GaAs en ce qui concerne les chaines d'amplification, et représentent une part importante du coût et de l'encombrement d'une tête d'émission radiofréquences. La solution originale proposée dans cette thèse représente une avancée significative en termes d'intégration par rapport à l'état de l'art et les premiers résultats mesurés démontrent la pertinence de l'architecture proposée. Une étude sur l'optimisation du rendement énergétique au niveau de l'étage de puissance en présence de signaux modulés en amplitude et phase de type 3G et 4G est également proposée. Cette étude adresse les potentialités des techniques de modulation de la charge et de l'alimentation et permet de comparer les deux approches.

Après une présentation du contexte et de l'état de l'art, une méthodologie de conception originale reposant sur l'étude de différentes classes de fonctionnement est proposée. Cette méthodologie permet en particulier de pré-dimensionner les cellules de puissance reconfigurables ainsi que leurs impédances de source et de charge en fonction des contraintes de puissance et de linéarité dans les différents modes pour avoir le meilleur rendement. Elle permet aussi de choisir les topologies de réseaux d'adaptation accordables pertinentes.

Ces études ont conduit à la réalisation de deux démonstrateurs intégrés en technologies SOI CMOS 130 nm. Le premier prototype est un amplificateur multimode et multibande reconfigurable à deux étages capable de fonctionner en mode saturé et en mode linéaire pour des bandes de fréquence situées entre 700MHz et 900MHz. L'architecture proposée est composée d'un étage de puissance reconfigurable constitué de deux cellules de puissance de type LDMOS pouvant être activées ou non en fonction du mode adressé. Différents réseaux d'adaptation accordables à base de capacités commutées utilisant des transistors NMOS à body flottant permettent une optimisation des performances du MMPA en fonction du mode et de la bande de fréquence. Avec ce prototype, des puissances de sortie de 35dBm en mode saturé et 30dBm en mode linéaire ont été mesurées avec des rendements correspondants supérieurs respectivement à 58% et 47%. Par rapport aux simulations initiales, des différences ont été observées puis analysées afin d'en identifier l'origine. Notamment, la surestimation du facteur de qualité des capacités MOM dans les réseaux de capacités commutées et des interconnections sous optimales sont la cause des écarts observés.

Le deuxième prototype est un amplificateur de puissance à modulation de charge passive intégrée. Cet amplificateur repose sur une cellule de puissance de type LDMOS associée à un réseau d'adaptation accordable à base de capacités commutées capables de supporter une puissance supérieure à 33dBm. Ce réseau permet de présenter à l'étage de puissance une trajectoire de charge optimale en fonction de la puissance de sortie. Avec ce prototype, une amélioration du rendement supérieure à 55% par rapport à la configuration utilisant une charge constante a été mesurée pour un recul en puissance compris entre 7dB et 11dB.

Mots clés : *Amplificateurs de puissance (PA), PA multimode multibande (MMPA), PA reconfigurable, SOI CMOS, LDMOS*