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Dwight José Cabrera Salas

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de l'université de Bordeaux

École doctorale Sciences Physiques et de l'Ingénieur

Spécialité Électronique

Préparée au laboratoire de l'Intégration du Matériau au
Système

Par Dwight Cabrera

LOW PHASE NOISE MM-WAVE FREQUENCY GENERATION FOR BACKHAULING APPLICATIONS ON BICMOS TECHNOLOGY

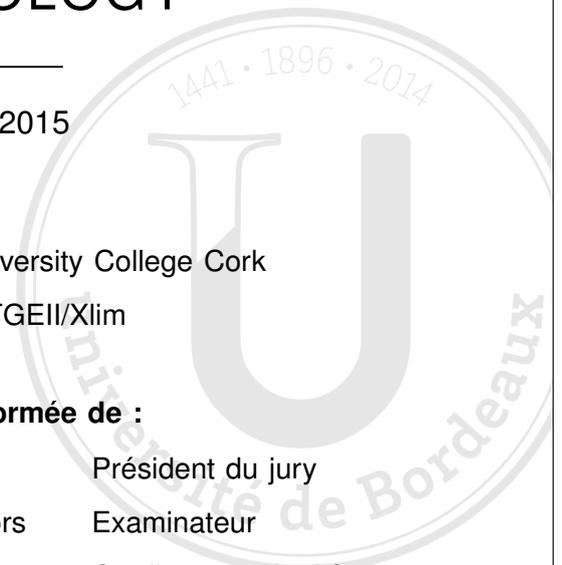
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"...Sometimes to look closely, it is better to look from afar"

RC13

Thèse réalisée
dans le Laboratoire de l'**Intégration du Matériaux au Système** de
Bordeaux
au sein de l'équipe *Circuits et Systèmes Numériques*
du groupe **Conception**.

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RÉSUMÉ

Titre: Générateurs de fréquence millimétrique à faible bruit de phase destinés à des applications backhauling sur une technologie BiCMOS.

Cette thèse porte sur l'analyse et la conception de générateurs de fréquence millimétrique à faible bruit de phase destinés à des applications de communication sans fil de très haut débit sur une technologie BiCMOS $0.25\ \mu\text{m}$. Spécifiquement, des applications *backhauling* sont visées sur le protocole de communication P2P (*point-to-point*), pour un système de radio hétérodyne (à faible fréquence intermédiaire) approprié pour les bandes entre 30–38GHz et de faible profondeur de modulation (2-3 bits /symbole). Une étude rigoureuse du comportement du bruit de phase en $1/f^2$ d'un oscillateur contrôlé en tension (du type paire différentielle croisée) en fonction de la fréquence d'oscillation est développée. Des facteurs essentiels pour la conception de ces oscillateurs tels que la plage de fréquence et la charge de la paire croisée sur le résonateur sont pris en compte dans l'analyse. L'étude révèle que lorsque la fréquence augmente, l'oscillateur passe à travers deux régimes d'opération différents, ici appelés région Q_L -limited et région Q_C -limited, qui résultent de la dépendance du facteur de qualité du résonateur à sa partie inductive (pour les basses fréquences d'oscillation) et sa partie capacitive (pour les hautes fréquences d'oscillation). De plus, l'impact de la plage de fréquence sur l'évolution du bruit de phase en $1/f^2$ a été considéré en utilisant un circuit classique à base d'un varactor et d'un condensateur du type MiM. Des équations simples et précises ont été calculées pour les paramètres du circuit afin d'obtenir une fréquence centrale souhaitée avec la variation de la capacité requise. Pour ce circuit, il a été démontré (et vérifié à travers des simulations du circuit) que le pire scénario du facteur de qualité peut être associé à la constante de temps d'un condensateur. Ce dernier a permis d'estimer aisément le facteur de qualité minimal de la partie capacitive du résonateur LC de l'oscillateur, pour une plage de fréquence donnée, en fonction de la fréquence d'oscillation. D'une manière similaire, et basée sur une analyse à petit signal, la constante de temps de la capacité de

sortie de la paire croisé a été déterminée. Notamment cette constante de temps présente un comportement constant sur une large gamme de fréquences, ce qui permet d'évaluer facilement son facteur de qualité. Cette étude fournit les bases théoriques qui permettent l'évaluation du bruit de phase en $1/f^2$ d'une source de signal basée sur un oscillateur en mode fondamental, super-harmonique ou sous-harmonique. En effet, la supériorité des oscillateurs sous-harmoniques est démontrée et des équations simples sont proposées pour déterminer la performance maximale et les conditions dans lesquelles elles peuvent être atteintes. Enfin, un système de génération de signal est ainsi conçu et vérifié par des mesures sur un prototype. Le système est composé d'un VCO sous-harmonique suivi d'un tripleur de fréquence (ILFT) –verrouillé par injection. Le circuit est implémenté sur une technologie SiGe:C BiCMOS $0.25\ \mu\text{m}$. Le tripleur implémente une configuration à émetteur commun, polarisé en courant, qui exploite la seconde harmonique du VCO afin d'améliorer l'efficacité de la génération du signal responsable de verrouiller le ILFT. A 30.8 GHz, le système atteint un bruit de phase de $-112\ \text{dBc/Hz}$ à 1 MHz d'offset. La consommation totale de courant est de 38 mA pour une tension d'alimentation de 2.5V. Un deuxième prototype a été réalisé pour un système de génération multibande, offrant ainsi trois sorties RF à 18 GHz, 34 GHz et 68 GHz. Avec une plage de fréquence de 10% (mesurée par rapport à la fréquence centrale) pour chaque sortie RF. Le bruit de phase mesuré à 1 MHz d'offset est respectivement de $-113\ \text{dBc/Hz}$, $-107\ \text{dBc/Hz}$ et $-100\ \text{dBc/Hz}$.

Mots Clés

Bruit de Phase, multiplication de fréquence, diviseur de fréquence, amplification, oscillateurs, fréquence millimétrique, verrouillage par injection, BiCMOS

ABSTRACT

This thesis deals with the analysis and design of Low phase Noise Local-Oscillator (LO) sources suitable for backhauling applications on the frequencies 30-38GHz. The LO is intended to be used in a low-IF architecture for low order modulations (2-3 bits/symbol). This work was developed in collaboration with NXP Semiconductors at CAEN, France, within the project RF2THz of the European program CATRENE.

The original contributions in this work include a rigorous study of the $1/f^2$ phase-noise characteristics of the VCO (bipolar cross-coupled pair Voltage-Controlled-Oscillator) with the oscillating frequency. Key factors in the design of VCOs such as tuning range and the tank load given by the cross-coupled pair are considered in the analysis. The study reveals that as the frequency scales, the VCO passes through two different zones, named the *QL-limited* and the *QC-limited* region, that results from the dependence of the resonator quality factor on its inductive part (for low oscillating frequencies) and its capacitive part (for high oscillating frequencies). Moreover, the impact of the tuning range on the $1/f^2$ phase noise evolution was captured by using a classical circuit based on an AC-coupled varactor and a MiM capacitor. Simple and accurate equations were derived for the circuit parameters in order to achieve a desired central frequency with the required capacitance variation. For this circuit, it is demonstrated (and verified through circuit simulations) that the lowest quality factor scenario can be associated to the time-constant of a lossy capacitor. The latter allows to estimate easily the minimum quality factor of the capacitive part of the VCO LC tank, for a given tuning range, as a function of the oscillating frequency. In a similar way, and based on a small signal analysis, the time-constant of the output capacitance of the bipolar cross-coupled pair was derived. Interesting, this time constant shows a constant behavior over a wide frequency range, thereby allowing to estimate easily its quality factor. This study set the bases for an analytical framework that enables the evaluation of the $1/f^2$ phase noise performances of local oscillator sources working either on fundamental, super-harmonic or sub-harmonic mode. The superiority in terms of $1/f^2$ phase noise of local oscillators

based on sub-harmonic oscillators is thus demonstrated and simple equations are derived to determine the maximum performance and the conditions on which this can be achieved.

Finally, a signal generation system intended for a low-IF point-to-point fixed radio system in the Ka-Band band is thus designed and verified through prototype measurements. The system is composed by a sub-harmonic VCO followed by an injection-locked frequency tripler (ILFT) and it is designed in a $0.25\ \mu\text{m}$ BiCMOS SiGe:C technology. The ILFT implements a cascode current-biased common emitter configuration that exploits the second harmonic of the VCO to enhance the efficiency in the generation of the injecting signal responsible for the ILFT locking. At 30.8 GHz, the system achieves a phase noise of $-112\ \text{dBc/Hz}$ at 1 MHz offset. The total current consumption is 38 mA for a supply voltage of 2.5 V. A second prototype is designed for a multiband LO generation, providing thus three RF outputs at 18 GHz, 34 GHz and 68 GHz. With a measured tuning range of 10% for each RF output, the measured phase noise at 1 MHz is $-113\ \text{dBc/Hz}$, $-107\ \text{dBc/Hz}$ and $-100\ \text{dBc/Hz}$ respectively.

Keywords

Phase Noise, frequency multiplier, frequency divider, power amplification, oscillator, millimeter wave, injection-locking, VCO, BiCMOS

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A mis padres, familia y Manue.

CHAPTER 1

INTRODUCTION

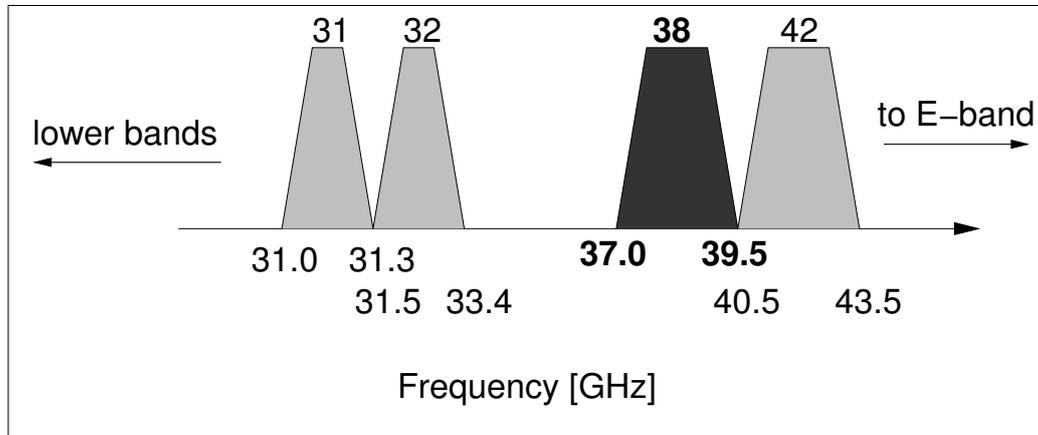


Figure 1.1: Point-to-Point (P2P) frequency bands [2].

Low noise millimeter wave frequency generation has received great interest by the academic research in recent years. Thanks to the advancements in BiCMOS process technology, the operating frequency of MOS and bipolar transistors has scaled to the mm-wave range allowing the miniaturization of radar and imaging systems at these frequencies. Moreover, it has permitted the integration of high-bit rate communication systems [3] and enabled the opportunity for fully integrated solutions of new wireless communication standards for mm-wave radio links, like the Point-to-Point (P2P) standard [2]. Radio-links operating in the P2P standard can achieve high-data-rate communications, allowing applications such as wireless backhauling (depicted in the figure 1.2) [4].

In the 31-42 GHz bands (see figure 1.1), the P2P standard offers channel bandwidths of less than 112 MHz. Modulation schemes such as QAM enable high data rates but impose stringent specifications in the RF front-end in terms of linearity, signal-to-noise ratio and LO phase noise.

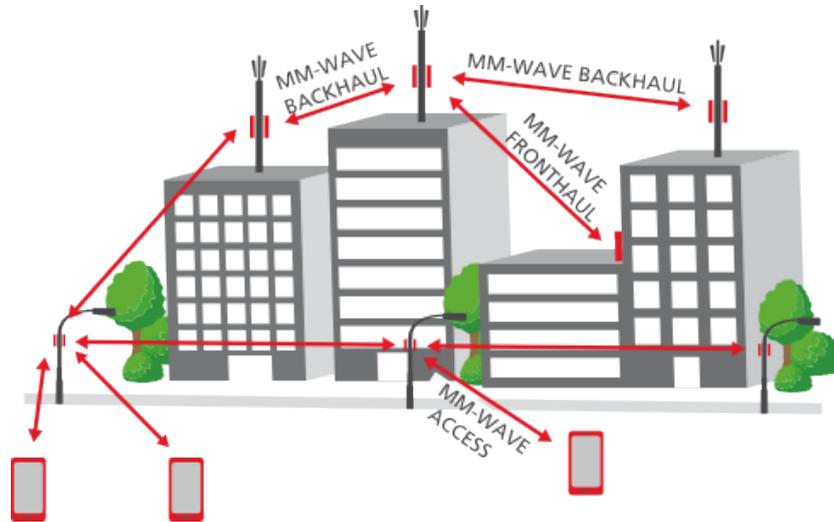


Figure 1.2: Wireless backhauling [5].

1.1 Objective of the thesis

This thesis deals with the analysis and design of Low phase Noise Local-Oscillator (LO) sources suitable for P2P applications in the 30-38 frequency band (see Fig. 1.1). The LO, which is intended to be applied in a low-IF architecture for low order modulations (2-3 bits/symbol), should attend the specifications summarized in the table I. The design proposes a LO signal with central frequency f_o and two additional outputs operating a $f_o/2$ and $2 \times f_o$.

This work was developed in collaboration with NXP Semiconductor at CAEN, France, within the project RF2THz of the European program CATRENE.

TABLE I
SUMMARIZED SPECIFICATIONS OF A LO SOURCE FOR A LOW-IF P2P APPLICATIONS IN THE 38GHz BAND.

Parameter	Specification
Technology	QUBIC4Xi (SiGe:C 0.25 μ m)
Central Frequency	34 GHz
Tuning range	10%
Tuning Voltage Range	0.5V - 4.5V
SSB Phase Noise @ 1MHz	> -107 dBc/Hz
RF output power at f_o	> 0 dBm
RF output power at $f_o/2$	> 0 dBm
RF output power at $2 \times f_o$	—
Supply current	< 120 mA

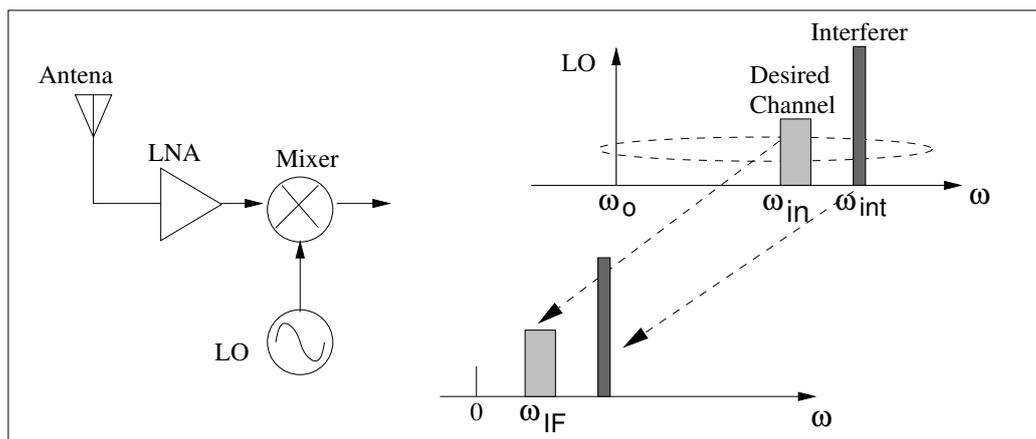


Figure 1.3: Downconversion in a receiver front-end.

1.2 The Local Oscillator (LO) in a radio system

Local Oscillators (LO) are used in radio system in both upconversion and downconversion paths. As an example, in the figure 1.3 a simplified down-conversion chain is depicted. The chain is composed by an antenna, a Low Noise Amplifier (LNA), a mixer and the LO with oscillating frequency ω_o . As depicted in the figure, an input signal located in the channel at ω_{in} is thus mixed with the LO producing a signal at a frequency

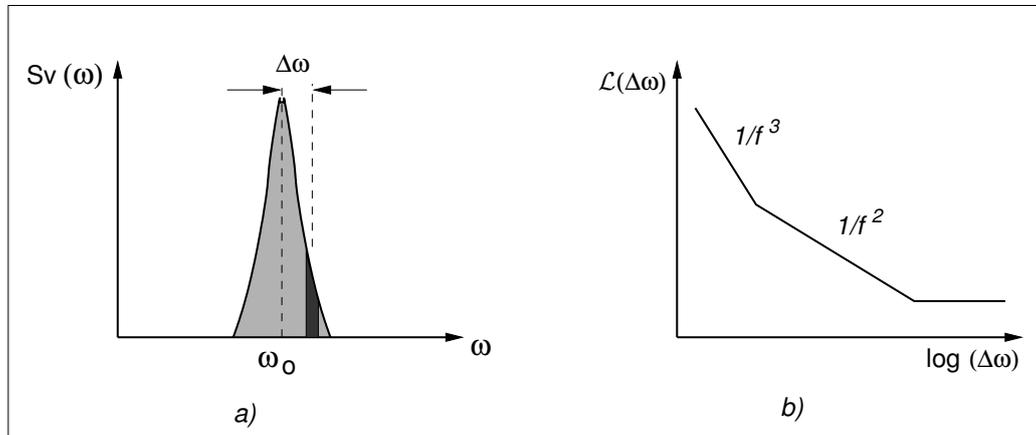


Figure 1.4: a) Typical measured PSD of the signal generated by a VCO. b) A typical phase noise plot.

ω_{IF} . From the figure it is obvious that not only the desired channel is downconverted, but all signals from the output of the LNA. In the figure an in-band interferer located at ω_{int} it is also downconverted.

From the system point of view, the main design specifications on a LO are therefore the purity of its output and its frequency range of operation. Additionally, the oscillator needs adequate driving capabilities to its consecutive block stage.

1.2.1 Phase Noise

From the figure 1.3, the output signal of the LO can be defined as:

$$v_{osc}(t) = V_o \sin(\omega_o t) \quad (1.1)$$

As it is clear from equation (1.1) it is expected that the signal power is located in the single frequency ω_o , however a real oscillating signal has the spectrum as in the figure 1.4, where the signal power is indeed distributed around ω_o . The cause for this distribution of the signal power around ω_o is the intrinsic noise present in the active and passive devices that composes oscillator. The phase noise $\mathcal{L}(\Delta\omega)$ is defined as the ratio

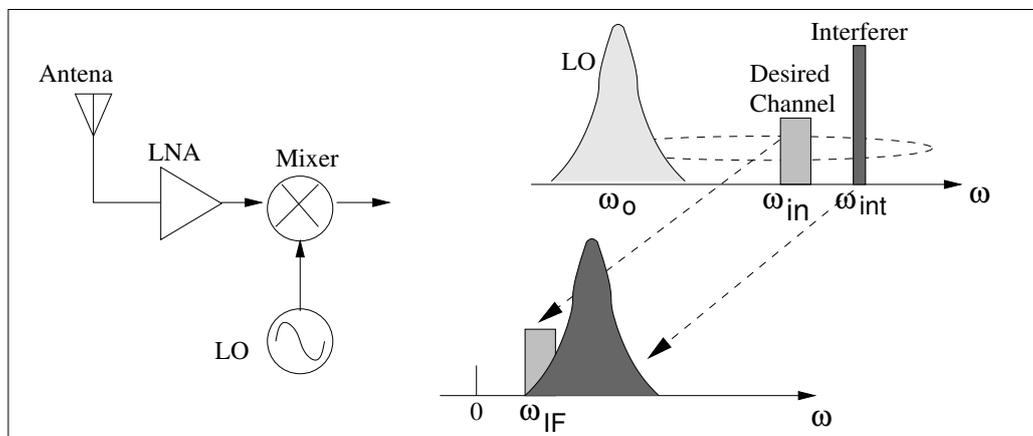


Figure 1.5: Effect of phase noise.

between the signal power \mathcal{P} at an offset frequency $\Delta\omega$ from ω_o , measured either in the upper or lower band, to the power of the signal at ω_o .

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log_{10} \left[\frac{\mathcal{P}(\omega_o + \Delta\omega)}{\mathcal{P}_{\omega_o}} \right] \quad (1.2)$$

In the case of an ideal LO signal, as in the figure 1.3, the phase noise is a minus infinitely large value. The figure 1.4 shows the phase noise behavior of a typical free-running LO as a function of $\Delta\omega$ in a logarithmic scale. From the figure three regions are distinguished: in the first and second region the phase noise decreases at a ratio of $1/f^3$ and $1/f^2$ respectively. The last region correspond to large frequency offsets and the phase noise flatten out. Such a floor may be due to the noise associated with any active elements (such as buffers) placed after the LO, or it can even reflect limitations in the measurement instrumentation itself [6].

1.2.2 Effect of phase noise

The effect of the phase noise in a LO is illustrated in the figure 1.5 based on a downconversion chain of the figure 1.3. Now the mixing action between the input signal (located at ω_{in} and ω_{int}) with the LO causes a broadened spectrum of both the desired

channel and the in-band interferer, having as a consequence that when the interferer is downconverted it corrupts the desired signal. The LO phase noise must then be small enough so that it produces negligible corruption.

1.3 State of the art of LO sources in the mm-wave frequencies and below

The table II summarized the tendency in oscillators at mm-wave frequencies. All the references in the table correspond to LC oscillators. In general LC oscillators are preferred thanks to its better phase noise performance. The table is ordered by the central frequency, having on the top the oscillator with the highest frequency. It can be observed that the phase noise at 1MHz increases as the oscillating frequency increases. It can be also verified that CMOS technology offers lower power consumption and higher FOM than BiCMOS technologies. From the table, the trade-off between phase noise and tuning range can be also verified. Indeed, higher tuning ranges implies higher phase noise.

TABLE II
PERFORMANCES SUMMARY OF STATE-OF-THE-ART SIGNAL SOURCES.

Ref.	Process	Freq [GHz]	TR%	Pdiss [mW]	PN@ 1MHz [dBc/Hz]	FOM*
[7]	0.35 μ m Bipolar	80	30	162.5	-97	173
[8]	0.18 μ m BiCMOS	52.5	26.5	132	-108	181.2
[9]	0.13 μ m CMOS	35	26	11	-101	
[10]	0.13 μ m BiCMOS	28	30	10.5	-104	182.7
[11]	0.13 μ m CMOS	26.9	2	5	-113	194
[12]	0.25 μ m BiCMOS	17.4	4.6	30	-113	183
[13]	0.25 μ m BiCMOS	13.1	5.1	93	-123	185.6

*Defined as: $FOM = -PN + 20 \times \log_{10}(f_o/f_{off}) - 10 \times \log_{10}(P[\text{mW}])$

1.4 Process Technology

This work is developed in the SiGe:C BiCMOS process QUBIC4XI from NXP featuring NPN transistors with transit frequency (f_t) of 216GHz and f_{max} of 177GHz [14]. NMOS and PMOS devices with 0.25 μ m minimum channel length are available. Among others this high-speed BiCMOS technology also offers:

- vertical NPN bipolar transistors, both high speed and high voltage versions,
- poly-silicon resistors,
- differential diode-varactor,
- capacitors (including high density MIM capacitor),

TABLE III
TYPICAL VALUES OF THE HIGH SPEED NPN BIPOLAR TRANSISTOR.

Parameter	Value
Peak f_t [GHz]	216
f_{MAX} [GHz]	177
BV_{CEo} [V]	1.5
BV_{CB0} [V]	5.2
h_{FE}	1800
V_A [V]	24

- high performance inductors,
- and 5 layers of metal interconnect.

The table III summarizes some characteristics of the high speed NPN bipolar transistor.

1.5 Organization of the Document

This document is organized as follows. In Chapter 2, the fundamentals of LC oscillators are reviewed. In chapter 3, a phase noise optimization strategy for LC oscillators is fully described. In Chapter 4, the design of two prototypes as well as measurement results for two prototypes are presented. Finally in Chapter 5, the conclusions of this work are summarized.

CHAPTER 2

FUNDAMENTALS IN LC OSCILLATORS

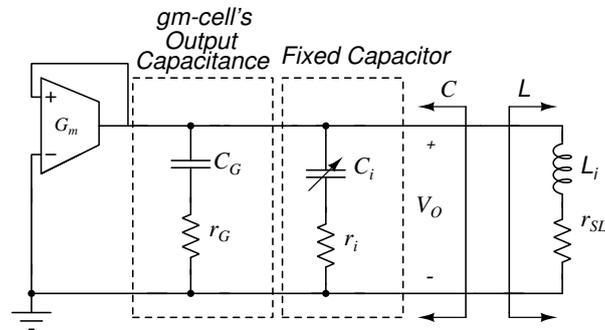
In this chapter the fundamentals of LC oscillators are reviewed. In the first section LC Oscillators are introduced. The chapter follows describing the principles that governs the injection-locking phenomenon in oscillators. Then the quality factor of LC resonators are reviewed. Finally, the chapter ends reviewing the phase noise in LC oscillators.

2.1 LC oscillators

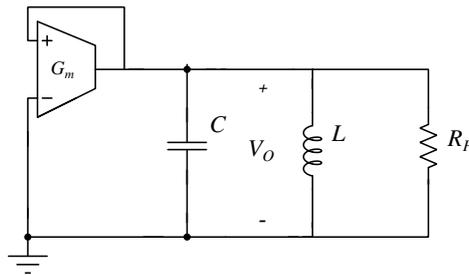
LC oscillators has been frequently used as LO sources in wireless communication systems thanks to its low phase noise capabilities. An LC oscillator can be represented by a lossy tank and a *energy-restoring* circuit that provides the necessary energy to compensate the energy loss in the resonator. To start-up the oscillations, the energy provided needs to be higher than the energy dissipated by the resonator. The oscillation reach an steady state as the amount of energy provided equals the energy dissipated by the lossy resonator [6].

Figure 2.1(a) shows a generic representation of a LC oscillator. In the figure, the transconductance cell (gm-cell) connected in a positive feedback works as the *energy-restoring* circuit. The output impedance of the gm-cell is mostly capacitive and can be represented by a series r_G - C_G connection. A fixed capacitor (represented by C_i and r_i) and inductor (represented by L_i and r_{sl}) set the resonant frequency of the oscillator. Note that even when this conceptual oscillator is based on simplified models of its components, it collects the fundamental actors that determine the performance of real implementations. A more simplified representation is presented in the figure 2.1(b) where the component losses are captured by the parallel resistance R_p and the total inductance and capacitance are captured by a parallel LC circuit.

Among the existing circuit topologies for LC oscillators, single-ended (colpitts, Clap, Hartely, etc.) or differential (Cross-coupled pair, Colpitts, etc) can be found.



(a)



(b)

Figure 2.1: a) Generic LC oscillator. b) Simplified view of a LC oscillator

In the later category the cross-coupled differential pair has been widely used in RF applications.

2.1.1 NPN cross-coupled pair LC (voltage-controlled) oscillator

The standard configuration of this circuit is presented in figure 2.2. Considering the process technology used in this work and introduced in the chapter 1, due to the higher transition frequency f_t the high-speed NPN transistor is preferred over either the NMOS or PMOS counterpart. A DC-decoupling network composed of C_f , r_f and v_b

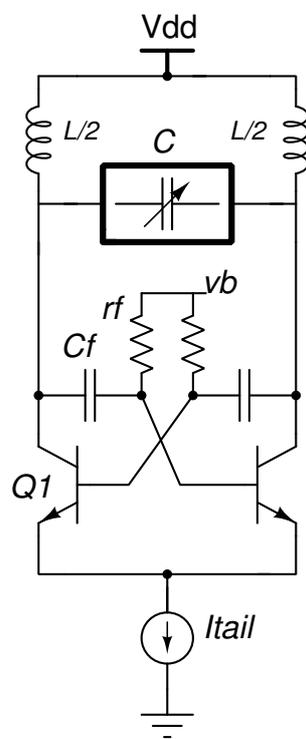


Figure 2.2: NPN cross-coupled LC (voltage-controlled) oscillator.

allows a differential output swing while keeping at 0V the maximum forward voltage of the base-collector junction of each transistor, hence keeping the transistors out of the saturation region. Referring to the breakdown voltages presented in the table III in the chapter 1, with an adequate selection of I_{tail} a differential amplitude of 1.4V for $V_{dd}=2.5V$ can be obtained in the circuit without putting the devices out of its "safe operating area" [15]. Note that I_{tail} is selected such that it provides the needed energy to start-up the oscillations and to set the amplitude of the output signal. In the circuit C and L set the oscillating frequency. By changing the value of the capacitance C , normally controlled by a voltage, the oscillating frequency can be tuned given the name of voltage-controlled oscillator.

The start-up condition for low frequencies¹ can be given as:

$$\frac{g_m}{2} > \frac{1}{R_p} \quad (2.1)$$

where g_m is the transconductance of the transistors. The amplitude of the output signal (differential) can be given as:

$$V_o = \frac{4}{\pi} I_{tail} R_p \quad (2.2)$$

¹In chapter 3, a small signal analysis is developed and the equivalent differential transconductance is derived for higher frequencies.

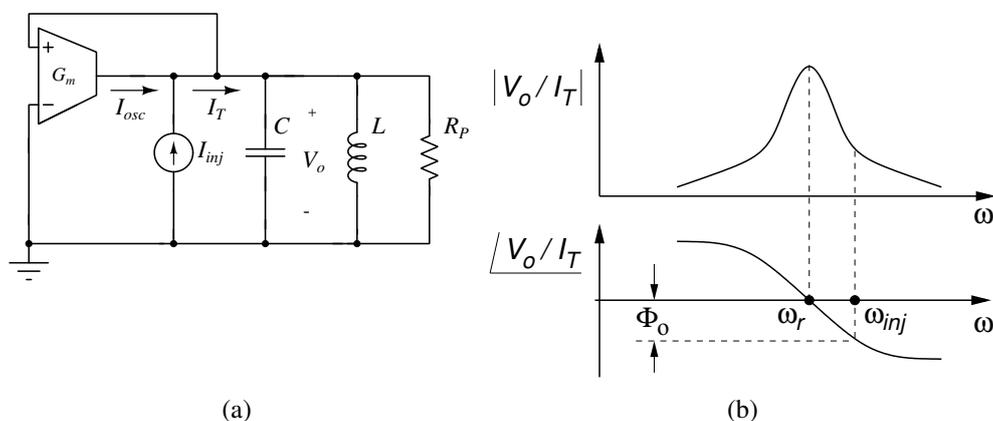


Figure 2.3: a) Conceptual LC oscillator under injection. b) Open-loop characteristics of the resonator: (Top) Magnitude response. (Bottom) Phase response.

2.2 Injection-locked LC oscillators

The principle that governs the coupling in oscillators is known as injection-locking [16]. Injection-locking has found numerous applications including among others: frequency division, quadrature generation, signal synthesis. This phenomenon is illustrated in the Fig. 2.3(a). In the figure, a given oscillator with oscillating frequency ω_r is being perturbed by the signal I_{inj} with frequency ω_{inj} ; this injecting signal can be placed deliberately or being the result of an unwanted coupling. If the amplitude and frequency of I_{inj} meet certain conditions the circuit indeed can oscillate at ω_{inj} and then it is said that the oscillator is *locked* to I_{inj} .

This phenomenon can be explained as follows. The signal I_{inj} introduces a phase shift Φ_o between the voltage sensed by the gm-cell and the current entering into the resonator I_T . If injection-locking occurs, to keep the positive feedback² the resonator adds an opposite phase shift by oscillating at ω_{inj} providing thus the necessary conditions for steady oscillations; this is illustrated in the figure 2.3(b). Indeed, there is a

² Or in other words, to have a total phase shift in the loop of 360° .

maximum (and minimum) frequency on which I_{inj} locks the oscillator and is the result of the maximum (and minimum) phase shift that the resonator is able to provide. Thus, injection-locking occurs for frequencies ω_{inj} that resides in $\pm\omega_L$ around ω_r , with:

$$\omega_L = \omega_r - \omega_{inj} = \frac{\omega_r}{2Q_{FL}} \frac{I_{inj}}{I_{osc}} \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2}}} \quad (2.3)$$

with Q_{FL} being the quality factor of the tank. Moreover, in the locked condition the phase shift θ between I_{inj} and I_{osc} can be obtained from³ :

$$\sin(\theta) = \sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2}} \quad (2.4)$$

One important characteristic in the locked condition, is that the phase of the locked oscillator follows the phase of the injection signal. If a "clean" I_{inj} signal is used, then the phase noise of the oscillator would improve up to the locking range. At the edge of the lock, the injected signal cannot correct for the phase noise.

On the other hand, and in a more general scenario, under the action of the injecting signal I_{inj} , the oscillator output can expressed as:

$$v_{osc}(t) = V_o \cos(\omega_{inj}t + \theta) \quad (2.5)$$

and it follows that:

$$\frac{d\theta}{dt} = \omega_r - \omega_{inj} - \omega_L \sin(\theta) \quad (2.6)$$

Eq. (2.6) was originally derived in [17] and is known as the Adler's equation. It allows to determine the dynamics of the oscillator under small injecting signals. In the locked condition $d\theta/dt=0$ and Eq. (2.6) yields the same result as in (2.3) for $I_{inj} \ll I_{osc}$. For $d\theta/dt \neq 0$ the equation (2.6) must be solved, having in general that θ is a function of

³Here it is assumed that I_{osc} is in phase with V_o .

time; this condition is known as *injection-pulling* and it is said that the oscillator is being *pulled* by I_{inj} . Furthermore, depending on how far ω_{inj} is from $\omega_r \pm \omega_L$ the oscillator could be in a *quasi-lock* or *fast-beat* state [16].

2.3 Quality Factor of LC resonators

For reasons that will be further reviewed in chapter 3, at millimeter wave frequencies the quality factor of LC resonators are dominated by its capacitive part, and the later tends to degrade as the tuning range increases. On the other hand (as it will be explained in chapter 3 as well) it is desirable to design a VCO around a single inductor.

Thus, in this section we provide a study to estimate the *minimum* quality factor of the capacitive part of a LC resonator, for a fixed inductor and for different tuning ranges. The main result of this section is to show that for a given inductor and tuning range, it is possible to associate the time constant τ of a lossy capacitor, with the minimum quality factor of the arrangement of a MiM capacitor and a varactor. Thus making possible to estimate the minimum quality factor of the resonator capacitive part as a function of the *oscillating frequency*. The results obtained provide accurate predictions and give a starting point useful in the qualitative analysis performed in the chapter 3.

To facilitate the study, the effects of parasitics are neglected. However, in real designs its impact have to be carefully considered.

2.3.1 Switched-capacitor bank (SCB) vs fixed capacitor and a varactor

In the case of VCOs at RF frequencies, previous works have revealed that switched capacitor banks are a suitable alternative to minimize the impact of the tuning range on the phase noise of the oscillator [18–20]. For mm-wave frequencies new constraints appear that limit the application of SCBs on the design of low noise VCOs and consequently making the design more challenging. The following characteristics are particularly important in mm-wave LC-VCOs:

1. The resonator quality factor depends mainly on the capacitive part.

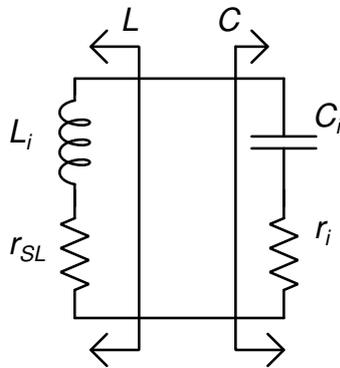


Figure 2.4: A Parallel LC resonator.

2. The low order value for the capacitors needed, makes parasitic capacitances (due to interconnections, inductor, gm-cell and capacitive input of next stage) to play a critical role. Not only the amount of parasitics involved is important, but also its quality factor.
3. Additionally, the performance of MOS-based switches degrades with the frequency. This behavior gets worst for long channel MOS transistors.

The conjunction of these characteristics makes that, to cope with a targeted tuning range, mm-wave VCOs usually rely only on fixed capacitors and varactors. For these reasons, the analysis here developed uses a fixed capacitor and AC-coupled varactor to give a targeted tuning range. However, for a given oscillating frequency the suitability of SCB should be considered.

2.3.2 The LC resonator

The most simple representation of real LC resonator is depicted in the figure 2.4. The resonant frequency of the circuit can be obtained as:

$$\omega_r = \frac{1}{\sqrt{LC}} \quad (2.7)$$

For L and C , the following can be written [6]:

$$L = L_i \left(1 + \frac{1}{Q_L^2} \right) \quad (2.8)$$

$$C = C_i \frac{Q_C^2}{Q_C^2 + 1} \quad (2.9)$$

The quality factor of the inductor and capacitor, Q_L and Q_C respectively, are given by:

$$Q_L = \frac{\omega_r L_i}{r_{SL}} \quad (2.10)$$

$$Q_C = \frac{1}{\omega_r r_i C_i} \quad (2.11)$$

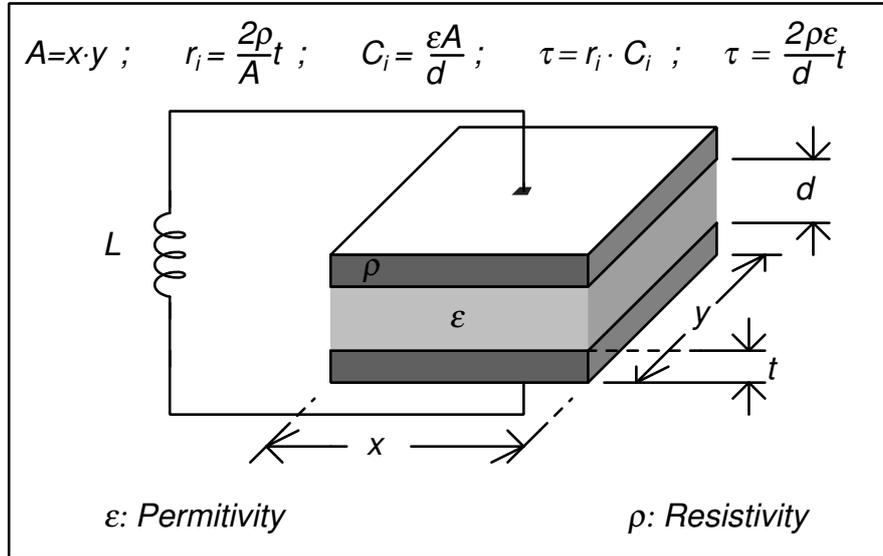
In (2.11), the quality factor can be expressed in terms of τ the time constant of the capacitor, given by $\tau = r_i C_i$. Then Q_C takes the form:

$$Q_C = \frac{1}{\omega_r \tau} \quad (2.12)$$

Note from (2.7) and (2.9), that if by setting a different resonant frequency with C_i , the τ of the capacitor does not change, then its quality factor can be found easily with (2.12) from the value of the resonant frequency. From simulated results, given at the end of the section for a practical case, it was found that it is possible to find a τ_{MiM} and τ_{var} that approximates the quality factor of MiM capacitors and differential diode varactors. Moreover, it was found that, given an inductor in the resonator, a time constant τ_i can be associated with a tuning range specification. Thus, making possible to estimate the minimum value of Q_C for different oscillating frequencies.

The case of a parallel-plate capacitor

A generic parallel-plate capacitor is presented in the Fig. 2.5 in which its capacitance is only set by changing its surface A . In this capacitor the series resistance is given

Figure 2.5: Time constant τ of a parallel-plate capacitor.

by the intrinsic resistance r_i of the plates. This resistance is inversely proportional to the transversal area of the current propagation, A , and is proportional to the thickness t . Since the capacitance C_i is set by changing A , then the product $r_i C_i$ is constant. Therefore, the quality factor of this capacitor will follow the expression in (2.12) when resonating with a given inductor.

The case of a MiM capacitor

In figure 2.6(a), a simplified 3D view of a MiM capacitor is depicted. This simplified representation corresponds to the MiM capacitor of the BiCMOS technology described in chapter 1. Due to reliability issues [21], and different from the parallel-plate capacitor, in a MiM capacitor the access to the bottom plate is not taken perpendicular to the surface A but laterally (see Fig. 2.6(b)). This means that its time constant τ_{MiM} scales with the size of the capacitor and consequently bigger capacitors come with lower qualities factor.

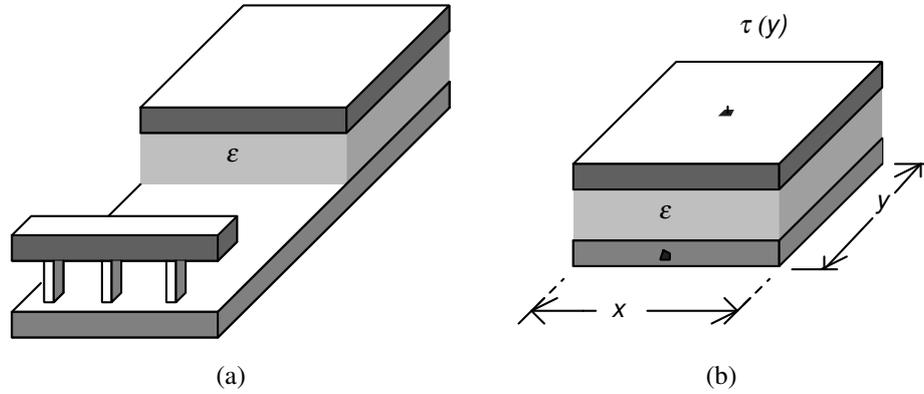


Figure 2.6: (a) Simplified 3D view of a MiM capacitor. (b) Simplified view indicating the connections. As the connection to the bottom plate is taken laterally, its time constant τ tends to increase as the capacitor increases.

2.3.3 Using a fixed capacitor and a varactor for a targeted tuning range.

For a given central frequency f_o , the tuning range is defined as [6]:

$$TR = 2 \frac{f_{max} - f_{min}}{f_{max} + f_{min}} \times 100 \quad (2.13)$$

From equation (2.7), a capacitance C_{min} and C_{max} are needed to have a maximum (f_{max}) and minimum (f_{min}) frequency. Thus, for a given tuning range a ΔC can be associated:

$$\Delta C = C_{max} - C_{min} \quad (2.14)$$

In a given technology, the ratio (β) between the maximum and minimum varactor capacitance can be considered constant [22, 23].

$$\beta = c_{max}/c_{min} \quad (2.15)$$

Being c_{max} and c_{min} the maximum and minimum capacitance for a given varactor size. The capacitance variation dc of a given varactor size can be expressed in terms of β in Eq. (2.15):

$$\begin{aligned} dc &= c_{max} - c_{min} \\ &= (\beta - 1)c_{min} \end{aligned} \quad (2.16)$$

The average varactor capacitance, c_o , can be expressed as:

$$\begin{aligned} c_o &= \frac{c_{max} + c_{min}}{2} \\ &= \frac{c_{min}(\beta + 1)}{2} \end{aligned} \quad (2.17)$$

having that c_{min} can be expressed as:

$$c_{min} = \frac{2c_o}{\beta + 1} \quad (2.18)$$

replacing (2.18) in (2.16):

$$dc = 2c_o \frac{\beta - 1}{\beta + 1} \quad (2.19)$$

which allows to express the average varactor capacitance as a function of β and its capacitance variation:

$$c_o = \frac{dc}{2} \frac{\beta + 1}{\beta - 1} \quad (2.20)$$

Now, if the capacitance variation ΔC in Eq. (2.14), is given by a varactor, then its average capacitance is:

$$c_o = \frac{\Delta C}{2} \frac{\beta + 1}{\beta - 1} \quad (2.21)$$

The different values of capacitance in the previous equations are represented in the figure 2.7. Note that in most cases an additional capacitance C_{fn} (usually with high

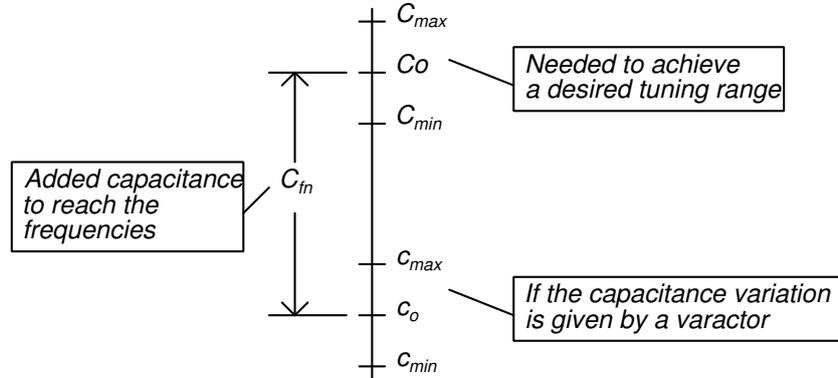


Figure 2.7: Representation of how to achieve a desired tuning range with a varactor and a fixed capacitance. The quantities depicted in the figure are described in the Eqs. (2.13)-(2.22)

quality factor) is added in parallel to reach the desired frequencies. Thus,

$$C_{fn} = \frac{C_{max} + C_{min}}{2} - \frac{\Delta C}{2} \frac{\beta + 1}{\beta - 1} \tag{2.22}$$

And the zero bias junction capacitance of the varactor c_{jo} is:

$$\begin{aligned} c_{jo} &= c_{max} \\ &= \Delta C \frac{\beta}{\beta - 1} \end{aligned} \tag{2.23}$$

AC-coupled varactor

The varactor can be coupled to the resonator either capacitively or magnetically (through the secondary of a transformer for example). The schematic of an AC-coupled varactor is presented in the figure 2.8(a). In the schematic it is also shown the fixed capacitance C_{fn} , described in the previous section. For a parallel inductance L of 97pH, the table I shows the value of C_{fn} and c_{jo} needed to a targeted tuning range of 10% for a central frequency of: 11, 16, 23, 31, 40, 60 GHz. In the table the values of C_{max} and C_{min} are also presented.

The table II shows the results obtained using for C_{fn} a MiM capacitor and for c_{jo}

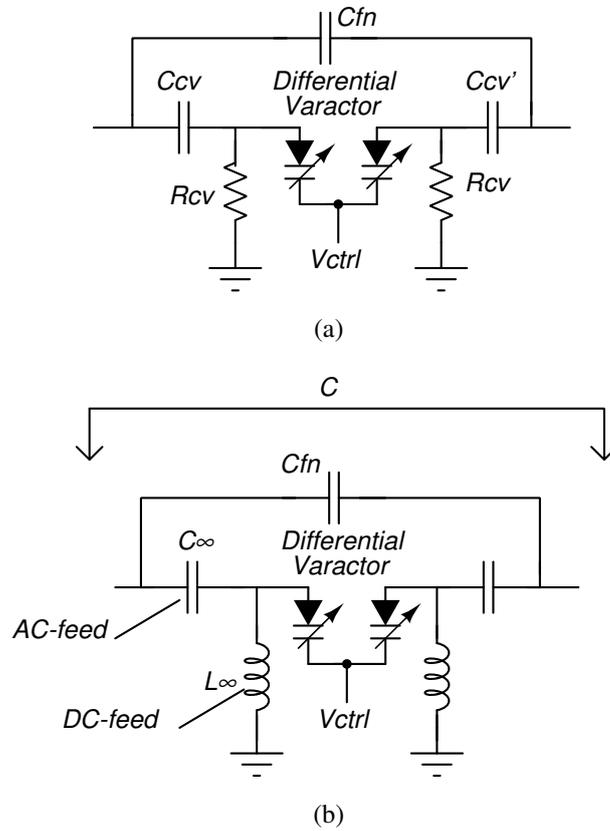


Figure 2.8: (a) Schematic of an AC-coupled varactor. (b) Schematic used for the simulations.

TABLE I
 FIXED CAPACITOR C_{fn} AND VARACTOR c_{jo} TO HAVE A TR OF 10% OVER DIFFERENT
 OSCILLATING FREQUENCIES FOR A PARALLEL INDUCTANCE L OF 97pH.

f_o [GHz]	$f_{o,min}$ [GHz]	$f_{o,max}$ [GHz]	C_{max} [fF]	C_{min} [fF]	C_{fn} [fF]	c_{jo} [fF]
11	10.45	11.55	2400	1950	1460	933
16	15.2	16.8	1130.26	925.23	689.24	441.02
23	21.85	24.15	547	447.8	333.54	213.4
31	29.45	32.55	301	246.5	183.6	117
40	38	42	180.84	148.0	110.28	70.57
60	57	63	80.37	65.79	49.01	31.36

TABLE II

SIMULATED RESULTS OF THE ARRANGEMENT OF c_{jo} AND C_{fn} OF THE TABLE I USING A DIFFERENTIAL VARACTOR AND A MIM CAPACITOR. C_{max} AND C_{min} CORRESPOND TO THE SIMULATED TOTAL CAPACITANCE FOR VCTRL 0.5V AND 4.5V RESPECTIVELY.

c_{jo} [fF]; W×L×NP [μm^2]	capMiM [fF]; W×L [μm^2]	C_{max} [fF]	C_{min} [fF]
934.5; 65×4×3	1459; 17.3×17	2200	1840
441.6; 46×4×2	689; 12×11.55	1044	871.6
213.5; 45×3.95	334; 8×8.325	504.2	421.5
117.7; 25×3.9	183.4; 6×6.05	277	231.8
70.8.7; 14.6×4	110.2; 4.5×4.8	166	139.2
31.6; 10×2.5	49.4; 4.5×2.1	74.4	62.8

a differential varactor. The circuit in figure 2.8(b) is used to evaluate the analysis of the previous section. An ideally high capacitance (1uF) is used to couple the varactor. Similarly an ideally high inductance (1uH) provides the ground reference to the varactor differential terminals. Thus, the voltage V_{ctrl} provides the reverse bias voltage of the varactor. The values of C_{max} and C_{min} obtained are in close agreement with the values needed (table I). Small redesign is needed to achieve the targeted values. The main differences come from:

- To have a better quality factor, C_{max} was simulated for V_{ctrl} of 0.5V instead of 0V, therefore the varactor do not achieve its maximum capacitance as predicted by Eq. (2.23).
- Parasitic capacitance, in both devices, from the terminals to ground will reduce the differential capacitance.
- The finite quality factor of both C_{fn} and c_{jo} would imply higher values to achieve the desired parallel capacitance as predicted by Eq. (2.9).

The simulated quality factor at the minimum and maximum frequency ($f_{o,min}$ and $f_{o,max}$) is presented in table III. The associated τ for the minimum frequency is also presented. Note that $\tau = 1/(\omega_r Q)$.

TABLE III

SIMULATED QUALITY FACTOR OF THE CIRCUIT IN THE FIG. 2.8(B), FOR THE CIRCUIT PARAMETERS IN THE TABLE II, AT THE MINIMUM AND MAXIMUM FREQUENCY. THE ASSOCIATED τ FOR THE MINIMUM FREQUENCY IS ALSO PRESENTED.

$f_{o,min}$ [GHz]	$f_{o,max}$ [GHz]	$Q_{fo,min}$	$\tau_{i,min}$ [fs]	$Q_{fo,max}$
10.45	11.55	42	362	94.8
15.2	16.8	31.52	332	73.5
21.85	24.15	22.53	323	53.6
29.45	32.55	17.8	303	42.5
38	42	14.1	297	33.8
57	63	10.71	260	24.8

In the figure 2.9 the quality factor at $f_{o,min}$ is presented as well as the quality factor of the MiM cap and varactor at the same frequency. Note for the MiM cap that the simulated points indicates an equivalent τ that decreases with bigger capacitors sizes. Remarkably, at $f_{o,min}$ the varactor, which is at its maximum capacitance, can be well approximated by $\tau_{var}=844.53 \times 10^{-15}$ s. Finally, a $\tau_i=310.7 \times 10^{-15}$ s can be used to describe the capacitive quality factor for a tuning range of 10%.

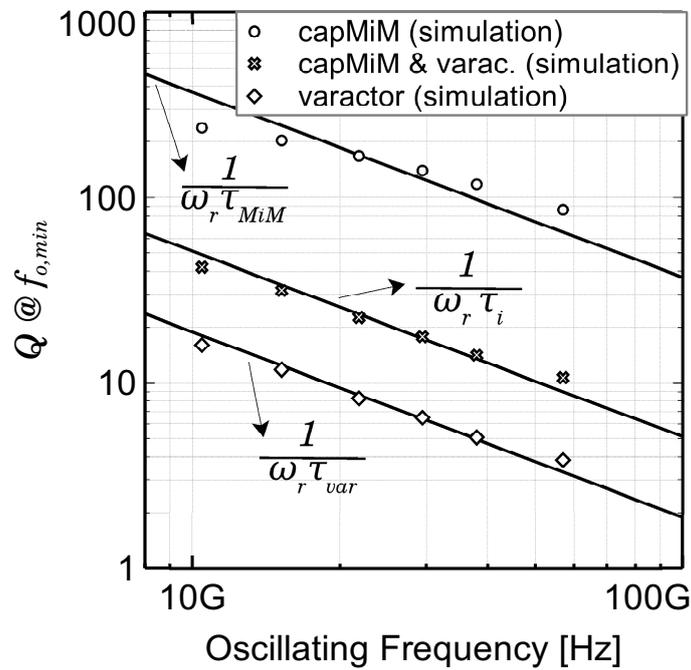


Figure 2.9: Simulated quality factor at $f_{o,min}$ of the arrangement of a fixed capacitor and varactor in the Fig. 2.8(b), according to the circuit parameters in the table II. The quality factor of the varactor and MiM capacitor are also presented. The solid line represent the quality factor obtained as in Eq. (2.12) for $\tau_{MiM}=42.9 \times 10^{-15} s$; $\tau_i=310.7 \times 10^{-15} s$; $\tau_{var}=844.53 \times 10^{-15} s$.

2.4 Phase Noise

The analysis of the phase noise of electrical oscillators has been addressed from different perspectives. The fundamental physical picture of the phase noise, which reveals the basic mechanisms that origins phase noise in oscillators, is for example notably exposed in [24,25]. On the other hand, there is the numerical side, which is concerned with the algorithms and methods usually implemented in CAD tools that enable the evaluation of the phase noise of oscillators directly from circuit simulations [26–29]. Finally, the phase noise of electrical oscillators can also be analyzed from the circuit design perspective [30–33]. The aim of this approach is to reveal the mechanisms in which the noise of the elements of an oscillator are transformed into phase noise. Among the theories proposed, the models by Lesson [30] and Hajimiri [32] have proven to be effective in the analysis and design of oscillators.

In particular, the model by Lesson [30] considers the oscillator as a LTI⁴ system. This model has been used for years as it allows to make qualitative analysis; however its applicability in real designs is seriously limited as it depends on unknown fitting factors. Alternatively, the Hajimiri model [32] considers the oscillator as a LTV (Linear, Time-Variant) system. This model has proven to be effective in describing the phase noise in electrical oscillators. Among others, this theory has enabled not only the possibility to obtain symbolic expressions for the phase noise of common oscillators topologies, but also to determine the contribution of a particular device into the phase noise of the oscillator. This is the case for the works in [1, 34, 35] where colpitts, and cross-coupled pair in both the Bipolar or CMOS versions have been analyzed. Specifically, the work [1] determines the $1/f^2$ phase noise of the NPN bipolar cross-coupled LC oscillator, the oscillator topology used in this work.

In this chapter, the phase noise model proposed by Hajimiri [32] is briefly reviewed

⁴Linear, Time-Invariant.

and the phase noise of the conceptual oscillator in Fig. 2.1(b) is derived. Finally, the main results of the work in [1] for the $1/f^2$ phase noise of the Bipolar cross-coupled LC oscillator are presented.

2.4.1 Review of a LTV phase noise model

Considering the oscillator in the figure 2.10, where $i(t)$ is a perturbation and C represent the equivalent capacitance at the output nodes, the Hajimiri-Lee phase noise model starts from a fundamental observation that applies to any oscillator. *After the action of a momentary perturbation on the oscillator, the effects on the amplitude of the oscillating signal vanishes with time⁵, contrary to what happens to the signal phase, in which a "phase excess" appears and continues indefinitely. Moreover, this phase shift shows a linear and time-variant response with the charge injected by the perturbation.*

This observation is illustrated in figure 2.11 in the case of a generic electrical oscillator; here the initial output signal $v_{osc}(t) = V_o \sin(\omega t)$, being V_o the amplitude of the signal, is perturbed by an impulse current causing fluctuations in both amplitude and phase. The perturbed output signal can be expressed by:

$$v_{osc}(t) = V(t) \sin(\omega t + \phi(t)) \quad (2.24)$$

where $V(t)$ and $\phi(t)$ represent the amplitude and phase fluctuations. As it is illustrated in the figure, after a given time the amplitude recovers its initial state but a phase excess remains in the oscillating signal. Then, according to the Eq. (2.24):

$$V(t) \rightarrow V_o \quad (2.25)$$

$$\phi(t) \rightarrow \Delta\Phi \quad (2.26)$$

⁵This particular behavior of the amplitude is an inherent consequence of the energy restoring circuit, which is present in any real oscillator as represented in figure 2.10.

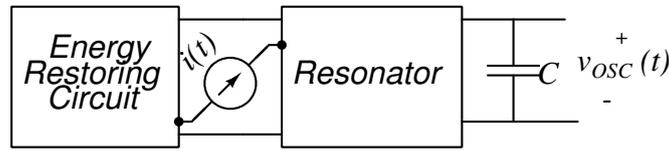


Figure 2.10: Generic electrical oscillator perturbed by $i(t)$.

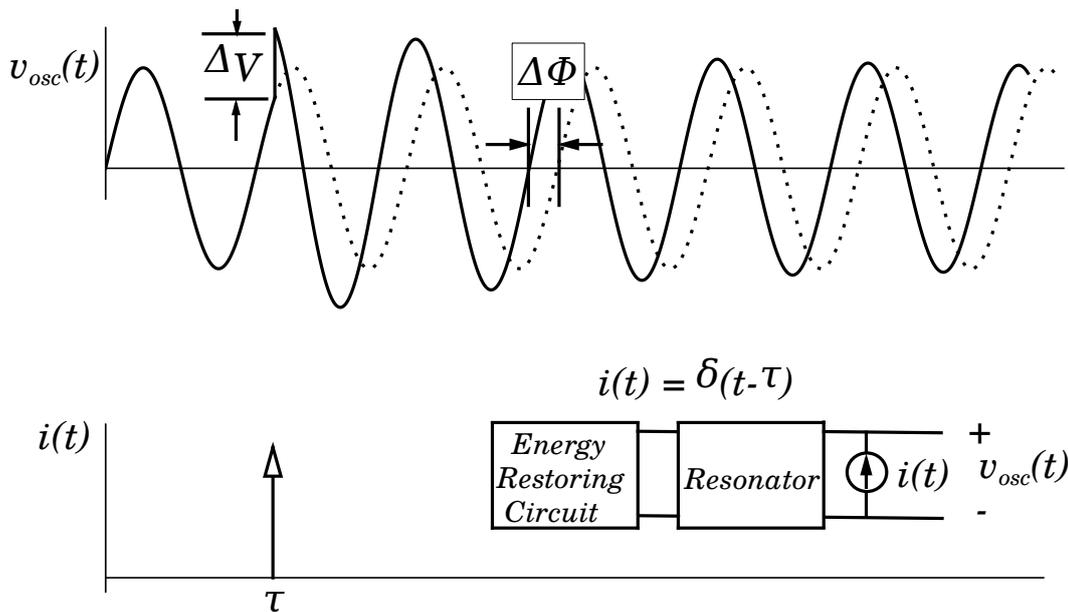


Figure 2.11: Response of an oscillator under a momentary perturbation.

Given this behavior of oscillators, the following general conclusions can be stated:

1. The phase noise of an oscillator can be obtained by determining the phase excess of the oscillating signal caused by the perturbation $i(t)$.
2. The phase excess can be expressed in terms of the unit impulse response injected into the nodes on which the perturbing signal is being acting.

These conclusions provide the basis for the mathematical formulation of the phase noise.

To appreciate the time-variant nature of oscillators, the response of an ideal LC os-

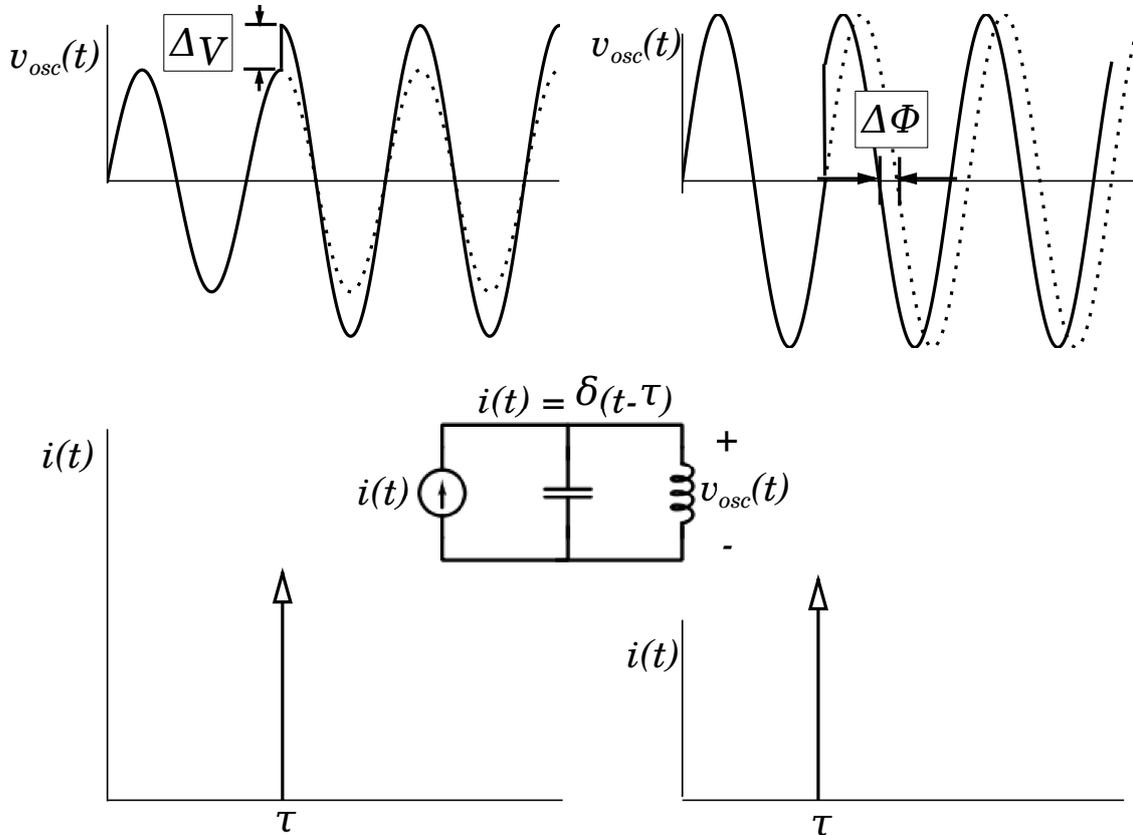


Figure 2.12: Response of an ideal LC oscillator to an impulse current. On the left, the impulse is applied when the oscillation has its maximum amplitude causing no phase excess in the signal. On the right, the impulse is applied when the amplitude crosses zero and only causing a phase excess.

cillator is illustrated in the figure 2.12 to the most pronounced cases: when an impulse current is applied at the moment of peak oscillation there are no phase perturbation⁶. But when the same impulse current is applied when the amplitude crosses zero, the perturbation on the phase is maximum. This dependence of the phase fluctuations with the time at which the impulse current is applied, gives the time-variant nature to oscillators. Indeed, this behavior is captured by the *impulse sensitivity function* (ISF) represented as $\Gamma(x)$.

⁶Observe that in this case the amplitude perturbation gets its maximum but as it was previously stated, the perturbation vanishes with time

The impulse sensitivity function. *The impulse sensitivity function (ISF), represented as $\Gamma(x)$, is a frequency and amplitude independent periodic function, which describes how much phase excess results when an unit impulse at time $t = \tau$ is applied.*

In a real oscillator the ISF depends on the waveform of the output signal and its actual expression can be obtained in a symbolic closed-form expression or it can be estimated directly from circuit simulations [32]. For the later, an impulse current is applied between two nodes of the oscillator at different times $t = \tau$, collecting for each case the resulting phase excess of the oscillating output signal (in steady state). At the end, a function $\Delta\Phi(\omega\tau)$ will be obtained and from this function the ISF is derived as:

$$\Gamma(\omega\tau) = \frac{\Delta\Phi(\omega\tau)}{\frac{\Delta q}{q_{max}}} \quad (2.27)$$

where Δq is the total charge injected by the impulse current and q_{max} the maximum charge displacement across the equivalent capacitance C as in the figure 2.10.

Based on the definition of the ISF, the unit impulse response for excess phase can be expressed as:

$$h_{\phi}(t, \tau) = \frac{\Gamma(\omega\tau)}{q_{max}} u(t - \tau) \quad (2.28)$$

The excess phase $\phi(t)$ caused by an input signal $i(t)$ can be calculated as the convolution of $i(t)$ with $h_{\phi}(t)$:

$$\phi(t) = \int_{-\infty}^{\infty} h_{\phi(t)}(t, \tau) i(\tau) d\tau = \frac{1}{q_{max}} \int_{-\infty}^t \Gamma(\omega\tau) i(\tau) d\tau \quad (2.29)$$

Note that since the $\Gamma(\omega\tau)$ is periodic, as can be noted from (2.27), it can be expanded in a Fourier series

$$\Gamma(\omega\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega\tau + \theta_n) \quad (2.30)$$

and using (2.30), a more convenient expression for Eq. (2.29) is obtained:

$$\phi(t) = \frac{1}{q_{max}} \left[\frac{c_o}{2} \int_{-\infty}^t i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^t i(\tau) \cos(n\omega\tau) \tau \right] \quad (2.31)$$

This expression gives the phase excess of the oscillation as it is perturbed by $i(t)$. As it is notorious from Eq. (2.24), the impact of $i(t)$ on $v_{osc}(t)$ results in a phase modulated signal [36].

Based on the equation (2.31), the figure 2.13 illustrates the process in which a given perturbation $i(t)$ results in a modulation of the phase of the signal v_{osc} . Basically, the signal $i(t)$ is successively downconverted by each harmonic component of $\Gamma(\omega\tau)$ and after being integrated, all components are added forming $\phi(t)$. The last block in the chain represents the phase modulation undertaken in $v_{osc}(t)$. This block representation allows to illustrate several revealing conclusions when the input perturbation $i(t)$ corresponds to a noise source in the oscillator. Indeed, it can be demonstrated that:

1. By reducing the value of the coefficients of the harmonic components of $\Gamma(\omega\tau)$, the conversion ratio between the input noise and the perturbations $\phi(t)$ are reduced.
2. Regarding the spectrum of $i(t)$, the filtering action (lowpass) of the integrators makes that only the noise around the harmonic frequencies of $\Gamma(\omega\tau)$ are effectively "downconverted" into $\phi(t)$.

In the case of an input noise current with a power spectral density $\overline{i_n^2}/\Delta f$, which for example represents the thermal noise of a device in the oscillator, and using Eq. (2.31) and (2.24) and taking the sideband power of v_{osc} at $\Delta\omega$ to the power at the fundamental frequency, the phase noise is finally obtained as:

$$\mathcal{L}(\Delta\omega) = 10 \log_{10} \left(\frac{\overline{i_n^2} \Gamma_{rms}^2}{2q_{max}^2 \Delta\omega^2} \right) \quad (2.32)$$

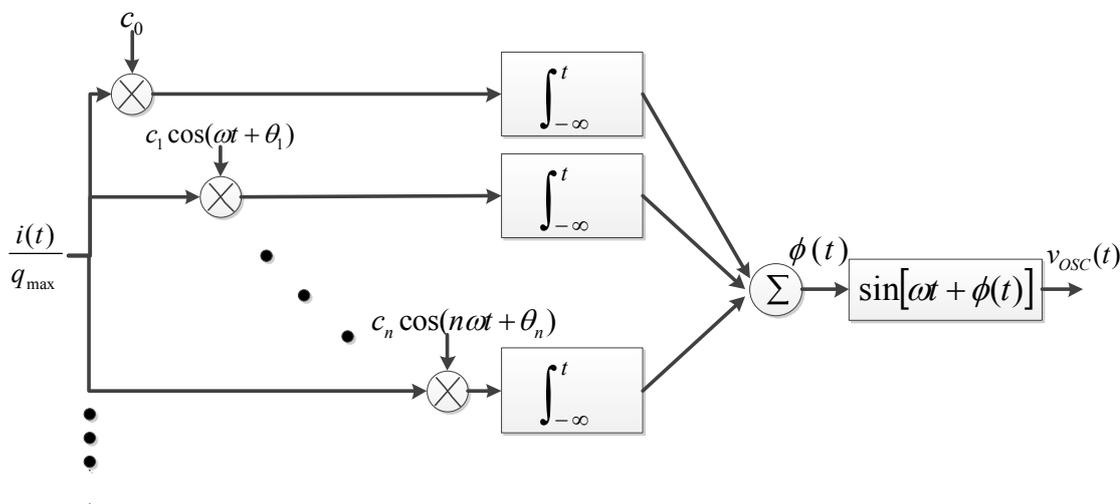


Figure 2.13: Block diagram illustrating how the perturbing signal $i(t)$ results in a phase modulation of the oscillating signal, v_{osc} , responsible for the oscillator phase noise.

where Γ_{rms} is the RMS (root-mean-squared) value of the ISF associated to $\overline{i_n^2}/\Delta f$. From the equation (2.32), it is possible to identify 3 different ways to decrease the the phase noise caused by the current $\overline{i_n^2}/\Delta f$:

- By decreasing the power of the noise signal $\overline{i_n^2}$ (filtering),
- By increasing the amplitude of the output signal, so the charge q_{max} increases due to $q_{max} = CV_{max}$.
- By decreasing the conversion factor between the device noise and the resulting phase noise in the output signal, i.e. by decreasing the factor Γ_{rms}^2 .

Note that new oscillator topologies exploiting specifically the third strategy have been recently published [37–39].

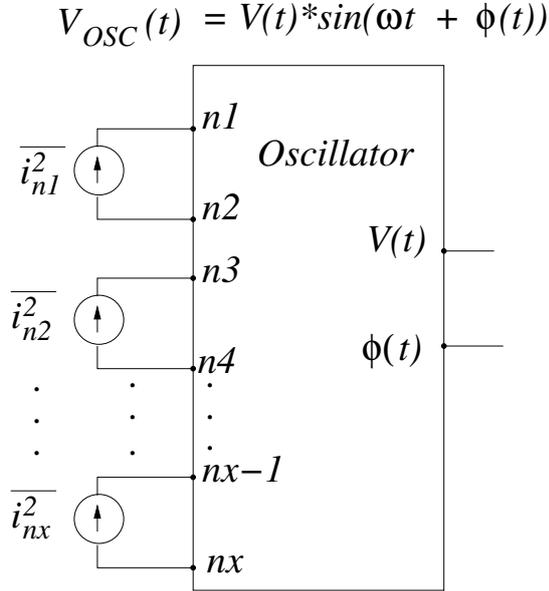


Figure 2.14: Input/Output representation of an oscillator. The noise sources are represented as current noise sources, injected in internal nodes of the oscillator.

A LTV model of an oscillator

As illustrated in figure 2.14, an oscillator can be modeled as a system with n inputs (each associated with one noise source) and two outputs, $V(t)$ and $\phi(t)$ as in Eq. (2.24). The noise sources, which are given in a current noise form, are injected at specific nodes of the oscillator. Therefore, according to analysis in the previous section there will be an ISF associated to each noise source. Since the relation between a given input noise and the fluctuations in phase, $\phi(t)$, corresponds to a linear and time-variant system, the superposition principle applies. Therefore, the resulting $\phi(t)$ due to all noise inputs with power spectral density: $\overline{i_{n1}^2}/\Delta f, \dots, \overline{i_{nx}^2}/\Delta f$, can be found as the sum of each contributions separately. Thus, the phase noise of the oscillator can be expressed as:

$$\mathcal{L}(\Delta\omega) = 10 \log_{10} \left(\frac{\sum_{i=1}^n \frac{\overline{i_{n,i}^2}}{\Delta f} \Gamma_{rms,i}^2}{2q_{max}^2 \Delta\omega^2} \right) \quad (2.33)$$

Cyclostationary Noise Sources

Since the currents and voltages are periodic functions in an oscillator, there will be noise sources in which its power spectral density will change periodically with time. Being $\Gamma_i(\omega t)$ the ISF of a noise current applied to the node i , if a cyclostationary noise current $\overline{i_{n,i}^2}/\Delta f$ is applied at the same node, its power spectral density can be expressed as:

$$\frac{\overline{i_{n,i}^2}}{\Delta f} = \frac{\overline{i_{n,i}^{\prime 2}}}{\Delta f} \cdot \alpha_n^2(\omega t) \quad (2.34)$$

where $\overline{i_{n,i}^{\prime 2}}/\Delta f$ is stationary, and $\alpha(\omega t)$ captures the cyclostationary nature of the noise source. Then the ISF of this cyclostationary noise source, $\Gamma_{eff,i}(\omega t)$, can be expressed as:

$$\Gamma_{eff}(\omega t) = \Gamma(\omega t) \cdot \alpha(\omega t) \quad (2.35)$$

and the equation (2.33) is then rewritten in a more general sense as:

$$\mathcal{L}(\Delta\omega) = 10 \log_{10} \left(\frac{\sum_{i=1}^n \frac{\overline{i_{n,i}^{\prime 2}}}{\Delta f} \Gamma_{rms,eff,i}^2}{2q_{max}^2 \Delta\omega^2} \right) \quad (2.36)$$

2.4.2 Phase Noise of the conceptual LC oscillator

The advantage of determining the phase noise of the conceptual oscillator of the figure 2.15 (previously introduced in the chapter 1), is that the phase noise of several LC oscillators correspond to a scaled version of the phase noise of this oscillator. This observation, which is evident in the phase noise model proposed by Lesson [30], holds under the a LTV analysis as well [1, 32, 34, 35]⁷.

Remembering that the transconductance cell G_m in the figure 2.15 is ideal, the total noise in the circuit can be associated to the noise caused by R_p . The thermal noise

⁷Indeed, this will be the case as long as the ISF of a given noise source in the oscillator can be related to the ISF of the noise associated to R_p , the equivalent parallel resistance of the LC resonator.

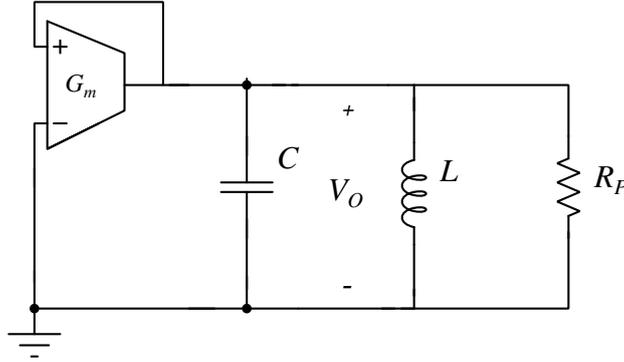


Figure 2.15: Simplified view of a generic LC oscillator.

current $\overline{i_{n,R_p}^2}$ associated to this resistance has a power spectral density given by:

$$\overline{i_{n,R_p}^2}/\Delta f = 4k_B T \frac{1}{R_p} \quad (2.37)$$

where k_B , T are the Boltzmann constant and temperature in kelvin respectively. Considering an output voltage given by $v_{osc} = V_O \sin(\omega t)$, the associated ISF for a noise current in parallel to the resonator is found to be [32]:

$$\Gamma(\omega\tau) = \cos(\omega\tau) \quad (2.38)$$

From Eq. (2.38) It is easy to show that:

$$\Gamma_{rms}^2(\omega\tau) = \frac{1}{2} \quad (2.39)$$

Then, using (2.32) for (2.37) and (2.39), the phase noise at the frequency offset $\Delta\omega$ is

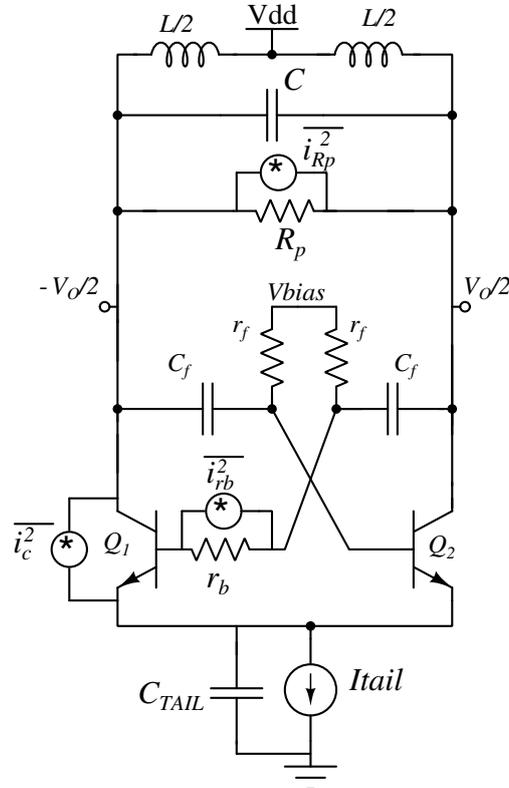


Figure 2.16: Simplified schematic of the NPN bipolar cross-coupled LC oscillator with the noise current sources being considered in the LTV analysis in [1]

given by:

$$\mathcal{L}(\Delta\omega) = 10 \log \left[\frac{k_B T}{R_p q_{max}^2 \Delta\omega^2} \right] \quad (2.40)$$

2.4.3 $1/f^2$ Phase Noise of the Bipolar cross-coupled LC Oscillator [1].

A simplified schematic of the oscillator is presented in figure 2.16. In the figure the noise sources considered are represented. For the transistors, only the shot noise and the thermal noise associated to the base resistance are considered; it has been observed that they are dominant in common oscillator designs. Indeed, it can be shown that this

will be the case as more current is being driven by the cross-coupled pair. Note that because of the symmetry only the noise sources for one transistor are represented, but the noise of both are considered in the analysis. The expression for $\overline{i_c^2}$ and $\overline{i_{r_b}^2}$ are given respectively by:

$$\overline{i_c^2} = 2qI_c(\omega t)\Delta f \quad (2.41)$$

$$\overline{i_{r_b}^2} = 4k_B T \frac{1}{r_b} \Delta f \quad (2.42)$$

where $I_c(\omega t)$ is the collector current. Note that $\overline{i_c^2}$ is a cyclostationary noise source.

As for the conceptual oscillator of the previous section, the noise in the LC resonator can be estimated from the thermal noise $\overline{i_{R_p}^2}$ of the equivalent parallel resistance R_p given by the equation (2.37):

$$\overline{i_{n,R_p}^2} = 4k_B T \frac{1}{R_p} \Delta f$$

After determining the effective ISF function, and its RMS value, for each noise current in the equations (2.41) – (2.4.3) ⁸, the $1/f^2$ phase noise is:

$$\mathcal{L}(\Delta\omega) = 10 \log_{10} \left(\frac{k_B T}{R_p C^2 V_o^2 \Delta\omega^2} \left(1 + \frac{1}{2n} + \frac{I_{tail} r_b}{3n V_T} \right) \right) \quad (2.43)$$

where n is the voltage divider from the output node and the base of the transistors. Several observations can be made from this equation:

- As it is evident from the first factor in the equation, the phase noise of the bipolar LC cross-coupled oscillator is a scaled version of the phase noise of the oscillator in Fig. 2.15.
- The contribution of the shot noise does not depend of the transistor size.

⁸More details can be consulted in the reference [1].

- The contribution of the base resistance increases as the tail current increases.
- For a correct evaluation of the phase noise, the load given by the cross-coupled pair to the resonator has to be considered in R_p . As described in the next chapter, this is of particular importance in mm-wave frequencies.

Considering that the $1/f^2$ phase noise of the bipolar LC cross-coupled oscillator is a scaled version of the conceptual oscillator in Fig. 2.15, the later will be used to determine the intrinsic behavior of the $1/f^2$ phase noise as a function of the oscillating frequency. This question, which is addressed in the next chapter, is fundamental to determine the suitability of the use of a VCO followed by a frequency multiplier in the generation of low phase noise signals at the mm-wave frequencies.

CHAPTER 3

PHASE NOISE OPTIMIZATION IN FREQUENCY GENERATION

One of the fundamental challenges in designing low phase noise mm-wave LC-based oscillators is the inherent degradation of the quality factor of the resonator, which is given by its capacitive part and decreases asymptotically with the frequency. This leads to an exacerbation of the trade-off between the tuning-range and the phase noise, making the design even more challenging.

Several published works have showed that this fundamental trade-off could be treated separately by the use of low frequency oscillators followed by frequency multipliers [40, 41]. In these systems the phase noise specification is met by the low-frequency oscillator and the tuning range will depend on the bandwidth of the frequency multiplier. Exists however, in the best case, a penalization of $20 \times \log_{10}(n)$ in the phase noise of the resulting signal after the multiplication by a factor n . Thus, while operating at lower frequencies, the phase noise performance has to be low enough to compensate this factor. Even when the feasibility of these systems have been verified, there are still several questions that should be deeply addressed in order to fully exploit its phase noise capabilities in a given process technology. Moreover, the performances of recent bipolar technology have enabled the design of frequency multipliers, either in push-push or injection-locked mode with adequate output power, suitable for their applications in the design of fully integrated signal sources in the mm-wave range. Thus, given a targeted frequency it is desirable to determine in which conditions a system based on frequency multiplication (or division) would be a better option in terms of phase noise when compared to a fundamental oscillator.

In this chapter a general study is developed, based on the LC oscillator of Fig. 2.1(a) in the chapter 2, that allows to address this issue. In particular, it is determined the improvement that can be obtained with systems based on lower (higher)-frequency VCOs followed by frequency multipliers (dividers) and under which conditions this improvement can be achieved.

This chapter is organized as follow. In the first section the effects of the oscillating

frequency on the $1/f^2$ -phase noise of a conceptual LC oscillator are studied. The results obtained enable the evaluation, in terms of phase noise, of different types of systems for frequency generation. Finally, the implications of using a bipolar cross-coupled pair as the gm-cell is addressed and design guides are derived.

3.1 Effects of the Oscillating Frequency on the $1/f^2$ phase noise of a LC-oscillator

In order to evaluate the suitability of the use of oscillators followed by frequency multipliers in the generation of low phase noise signals, the question arises of determining the intrinsic behavior of the $1/f^2$ -phase noise of LC-oscillators as a function of the oscillating frequency. This question is addressed here analytically for a circuit design perspective, based on the well known conceptual oscillator of Fig. 3.1. The circuit is composed by a noiseless and linear transconductance cell (gm-cell) with a series $r_G - C_G$ network as its output impedance; and a parallel LC-resonator which in turn is composed by (both lossy) inductor and capacitor. The later is denoted in the figure as a *fixed capacitor* and its role is to set the oscillating frequency. This approach is essential in this analysis, as the oscillating frequency is not considered as an independent variable but as the resonant frequency of the circuit itself. Then, given a capacitance range for this fixed-capacitor, the resonator quality factor, the oscillator phase noise, as well as the contribution of each resonator component into the phase noise, can be obtained as a function of the oscillating frequency. Note that to keep the analysis close to a real circuit-design scenario, r_i , the resistance in series to C_i should capture the capacitance variations. Here we consider that the *time constant* of the fixed-capacitor is constant for all possible values of C_i , i.e., $r_i C_i = \tau_i = \text{constant}$ ¹. On the other hand, C_G and r_G are

¹Indeed, from the section 2.3 in the chapter 2, this simple scalable model for r_i captures the essence of a two-parallel plates capacitor and it is a good approximation for Metal-Insulator-Metal (MiM) capacitors.

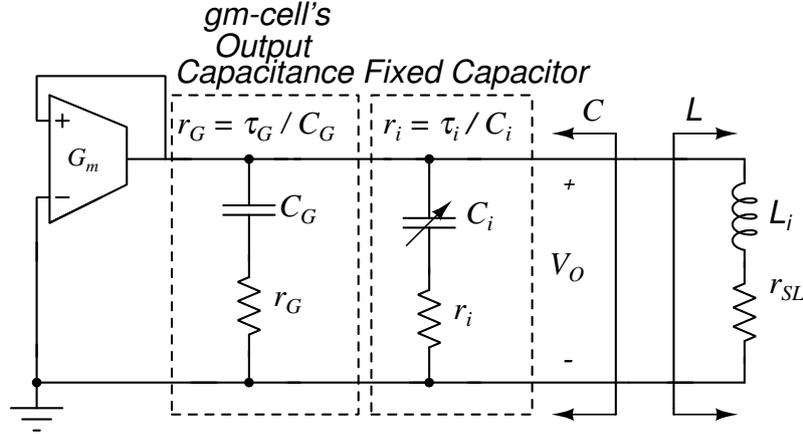


Figure 3.1: LC oscillator used for the analysis. By sweeping the value of the fixed capacitor it is possible to evaluate: the loaded quality factor and the phase noise at 1MHz versus the oscillating frequency as in Eq. (3.8).

TABLE I
TYPICAL VALUES OF THE ELEMENTS IN THE OSCILLATOR OF THE FIGURE 3.1.

Component	Value
V_o	$1.4/\sqrt{2}$ [V]
L	97 [pH]
r_{SL}	305 [m Ω]
C_i	$1 \text{ [fF]} \leq C_i \leq 100 \text{ [pF]}$
τ_i	77×10^{-15} [s]
C_G	50 [fF]
r_G	20 [Ω]
$Temp$	27 [$^{\circ}$ C]

assumed constant with the oscillating frequency. Indeed, as it is shown in section 3.3, the time constant (τ_G) of the differential output of the NPN bipolar cross-coupled pair shows a constant value over a broad frequency range.

On the other hand, considering that r_i , r_{SL} and r_G are the only sources of noise, the total phase noise in the $1/f^2$ region of the signal V_o can be expressed by the well known

expression [42]:

$$\mathcal{L}(\Delta\omega) = 10 \log_{10} \left(\frac{k_B T}{R_p q_{max}^2 \Delta\omega^2} \right) \quad (3.1)$$

where k_B is the Boltzmann constant; T is the temperature in Kelvin degrees; R_p is the equivalent parallel resistance of the circuit; q_{max} is the peak charge stored in the equivalent parallel capacitance of the resonator (C); and $\Delta\omega$ is the frequency offset from ω_r at which the phase noise is being considered. In (3.1) the parallel resistance R_p can be given in terms of the loaded quality factor of the resonator, Q_{FL} , defined as:

$$\frac{1}{Q_{FL}} = \frac{1}{Q_L} + \frac{1}{Q_C} \quad (3.2)$$

where Q_L and Q_C are the quality factor² of the inductor and equivalent capacitance respectively. With,

$$Q_C = \frac{Q_i}{1 + \frac{C_G}{C_i} \frac{Q_i}{Q_G}} + \frac{Q_G}{1 + \frac{C_i}{C_G} \frac{Q_G}{Q_i}} \quad (3.3)$$

where Q_i and Q_G are the quality factor of C_i and C_G respectively. And,

$$Q_L = \frac{\omega_r L}{r_{SL}}; Q_i = \frac{1}{\omega_r \tau_i}; Q_G = \frac{1}{\omega_r \tau_G}; \quad (3.4)$$

$$C = \frac{C_i}{1 + \frac{1}{Q_i^2}} + \frac{C_G}{1 + \frac{1}{Q_G^2}} \quad (3.5)$$

Additionally, being V_o the peak voltage in the resonator then:

$$q_{max} = C V_o \quad (3.6)$$

Finally, from Eq. (3.6) and considering that $Q_{FL} = \omega_r C R_p$, the phase noise in equation (3.1) can be rewritten as a function of the oscillating frequency, ω_r :

$$\mathcal{L}(\omega_r) = 10 \log_{10} \left(\frac{k_B T \omega_r}{Q_{FL} C V_o^2 \Delta\omega^2} \right) \quad (3.7)$$

²Defined as $Q = \text{Im}\{Z\}/\text{Re}\{Z\}$

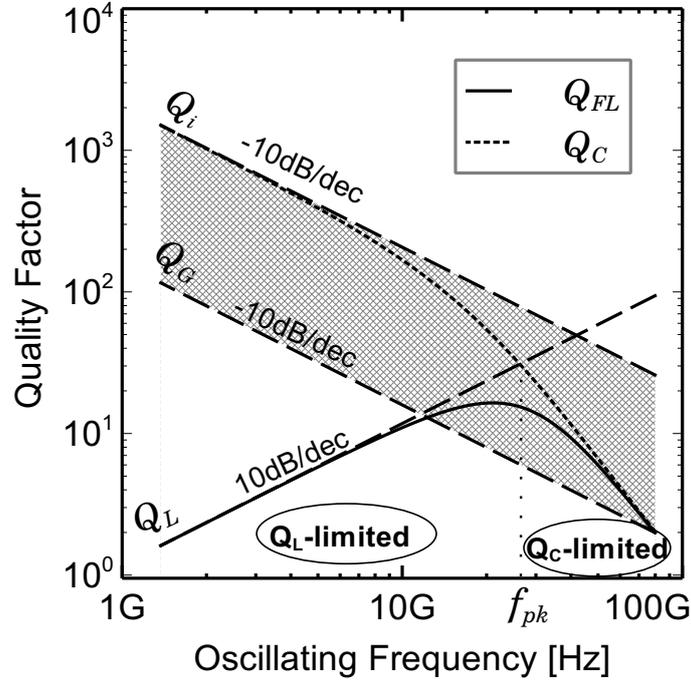


Figure 3.2: Loaded quality factor (Q_{FL} in Eq. (3.2)) versus the oscillating frequency Eq. (3.8). The contribution of each element of the resonator is also illustrated according to Eq. (3.3) and (3.4). The values used for the elements in the circuit are in the table I.

This compact representation of Eq. (3.7) allows analyzing the impact of different design parameters on the phase noise of the oscillator. A direct observation from (3.7) is that for a given oscillating frequency a higher equivalent capacitance is always favorable in terms of the phase noise³. Indeed, a higher capacitance decreases the sensitivity of the oscillator to phase perturbations when a noisy current is injected into the resonator [32].

In the next sections different parameters of the oscillator will be analyzed as a function of the oscillating frequency, which in turn is set with the fixed capacitor according to the component values in the Table I.

³The maximum suitable capacitance however will be limited by the minimum reliable inductance that can be implemented

3.1.1 Loaded quality factor vs Oscillating frequency

By replacing the equations (3.3) and (3.4) in (3.2) the dependency of the loaded quality factor with the oscillating frequency is obtained. Note that the equation (3.2) is valid in a general sense, as it collects the inductive and capacitive behaviors in the resonator independently of their particular frequency response. Obviously the quality factors in the equation (3.4) are valid only for the models of the components depicted in Fig. (3.1), but even when more elaborated models are used, these simplified models capture the general frequency response of the resonator elements and allow a qualitative analysis of the circuit. The resonant frequency of the conceptual oscillator in Fig. 3.1 is given by the equation (3.8).

$$\omega_r^2 = \frac{1}{2L^2(\tau_i^2 C_G + \tau_G^2 C_i) - 2L(\tau_i \tau_G)^2} \left[L(\tau_G^2 + \tau_i^2) - L^2(C_i + C_G) - r_{SL}^2(\tau_G^2 C_i + \tau_i^2 C_G) + \sqrt{SR1 + SR2} \right] \quad (3.8)$$

with

$$SR1 = \left[L^2(C_i + C_G) - r_{SL}^2(\tau_G^2 C_i + \tau_i^2 C_G) \right]^2$$

$$SR2 = L \left[\tau_G^2 - \tau_i^2 \right] \left[2L^2(C_i - C_G) + L(\tau_G^2 - \tau_i^2) + 2r_{SL}^2(\tau_i^2 C_G - \tau_G^2 C_i) \right]$$

Two key properties can be derived from the equations of the loaded quality factor (Q_{FL} in Eq. (3.2)) and the quality factor of the equivalent capacitance (Q_C in Eq. (3.3)).

1. Considering the reciprocal response between Q_L and Q_C ⁴, for lower oscillating frequencies Q_{FL} is always upper-limited by Q_L ; similarly for higher oscillating

⁴While Q_L increases with the frequency Q_C decreases asymptotically.

frequencies Q_{FL} is upper-limited by Q_C . These limits pose lower bounds on the minimum phase noise of the oscillator.

2. For any value of C_i and C_G the quality factor of the equivalent parallel capacitance, Q_C , will always resides in the region limited by Q_i and Q_G .

These two properties as well as the quality factors defined in equations (3.2) - (3.4) are graphically illustrated in Fig. 3.2 for the circuit parameters in the Table I. Indeed, Q_{FL} is not only upper-limited by Q_L and Q_C but it is also well approximated by them as the frequency deviates from f_{pk} , the frequency at peak Q_{FL} . These two different behaviors of the resonator quality factor are labeled in the figure as Q_L -limited and Q_C -limited. The frequency at peak Q_{FL} , f_{pk} , divides these two regions. Moreover, in the Q_L -limited region, Q_{FL} is limited by an increasing line 10 dB/dec. Note that as the resonant frequency is obtained by changing C_i while τ_i is constant, Q_i and Q_G decreases at -10 dB/dec. Finally, note that for reasonable values of the elements of this generic oscillator, resonant frequencies in the millimeter-wave range will put the resonator in the Q_C -limited region.

3.1.2 Phase Noise vs Oscillating frequency

The previous analysis of the loaded quality factor of the resonator are mapped into equation (3.7) to analyze the phase noise of the oscillator, denoted $\mathcal{L}(Q_{FL})$. To find the contribution of each element of the resonator into the phase noise, Q_{FL} in (3.7) is replaced by the respective quality factor of the elements defined in the equations (3.3) and (3.4). Thus the factors $\mathcal{L}(Q_C)$, $\mathcal{L}(Q_L)$, $\mathcal{L}(Q_i)$, $\mathcal{L}(Q_G)$ are systematically obtained and their values are plotted in the Fig. 3.3 for the example being considered. As expected, in the Q_L -limited and Q_C -limited regions, $\mathcal{L}(Q_L)$ and $\mathcal{L}(Q_C)$ poses lower bounds on the phase noise, indeed the phase noise is well approximated by these factors. It can be verified for the example being considered that in the Q_L -limited region the

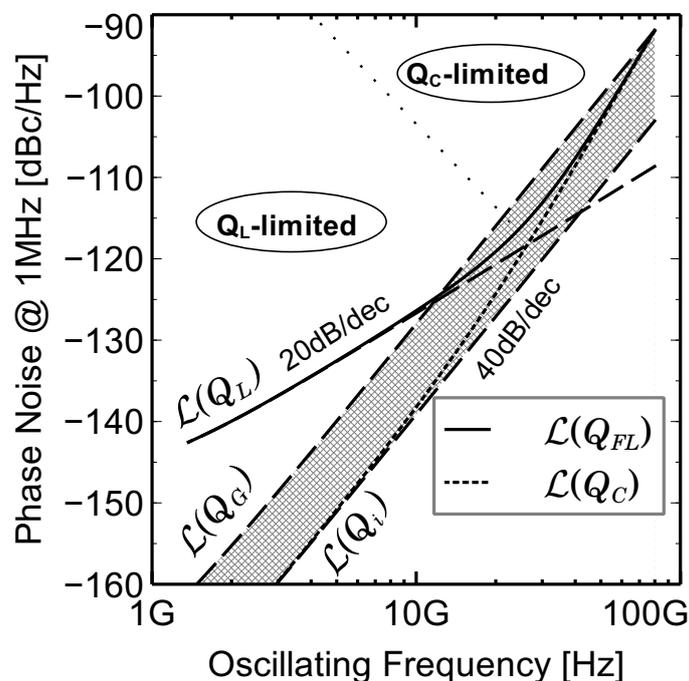


Figure 3.3: Phase noise of the oscillator in Fig. 3.1 as a function of the oscillating frequency as in Eq. (3.8). The contribution of each element of the oscillator is also illustrated. The values used for the elements in the circuit are in the table I.

phase noise follows an increasing behavior of 20 dB/dec. On the other hand, in the Q_C -limited region, the phase noise is constrained by the quality factor of the capacitive impedance of the gm-cell and the fixed-capacitor, i.e., $L(Q_i)$, $L(Q_G)$ each of them increasing at 40 dB/dec with the oscillating frequency.

In general, for a given inductor in the conceptual LC oscillator, the intrinsic behavior of its phase noise is an increasing function with the oscillating frequency, caused not only by the increment in frequency itself and the degradation of the resonator quality factor, but also for the reduction of the equivalent capacitance of the resonator. The combination of these effects are evident in the equation (3.7) with the factor $\omega_r/(Q_{FL}C)$.

Furthermore, the Q_L -limited and Q_C -limited regions results in different design approaches for LC oscillators. For example, improving the quality factor of inductors has lower impact on the phase noise performance of an LC oscillator in the Q_C -limited re-

gion. Indeed, as in the Q_C -limited region the phase noise depends on the quality factor of the capacitive terms the well known trade-off between phase noise and tuning range is exacerbated in this region. This trade-off is analyzed in more detail in the next section by letting the quality factor of the fixed capacitor to vary from Q_G to an ideally high value.

3.1.3 Description of the design space of Q_C

Let's define the worst quality factor that C_i could have as the quality factor of the output capacitance of the gm-cell, thus from the equations (3.2) and (3.3) $Q_C = Q_G = Q_i$ and $\tau_i = \tau_G$. Under this condition Q_{FL} follows Q_G as illustrated in Fig. 3.4(a) for the example being considered. Note that Q_{FL} is now limited by a 10 dB/dec and -10 dB/dec lines.

On the other hand, the maximum achievable Q_C , which is denoted $Q_{C,limit}$, is found by letting Q_i to increase infinitely, i.e. $\tau_i = 0$. In this case, the equation (3.3) simplifies to:

$$Q_{C,limit} = \left[\frac{1}{\tau_G \omega_r} \left(1 + \frac{C_i}{C_G} \right) \right] \times \left[1 + \frac{\tau_G^2}{1 + C_G/C_i} \omega_r^2 \right] \quad (3.9)$$

where $Q_{C,limit}$ can have different shapes according to the values C_G and τ_G .

Thus, the design space for Q_C is limited by Q_G and $Q_{C,limit}$ as illustrated in the Fig. 3.4(b); the design space is represented by a shaded region. From the figure it is observed that $Q_{C,limit}$ keeps decreasing at -30dB/dec until the maximum oscillating frequency is achieved.

Following the same analysis of the previous section, the phase noise of the oscillator for $\tau_i = \tau_G$ is illustrated in the Fig. 3.4(a). This case is particularly interesting because it states the limit in which the resonator's quality factor is being degraded by the output capacitance of the gm-cell. Similarly, as illustrated in the Fig. 3.4(b), based on the design space of Q_C it can be assessed the limits on the minimum phase noise that the

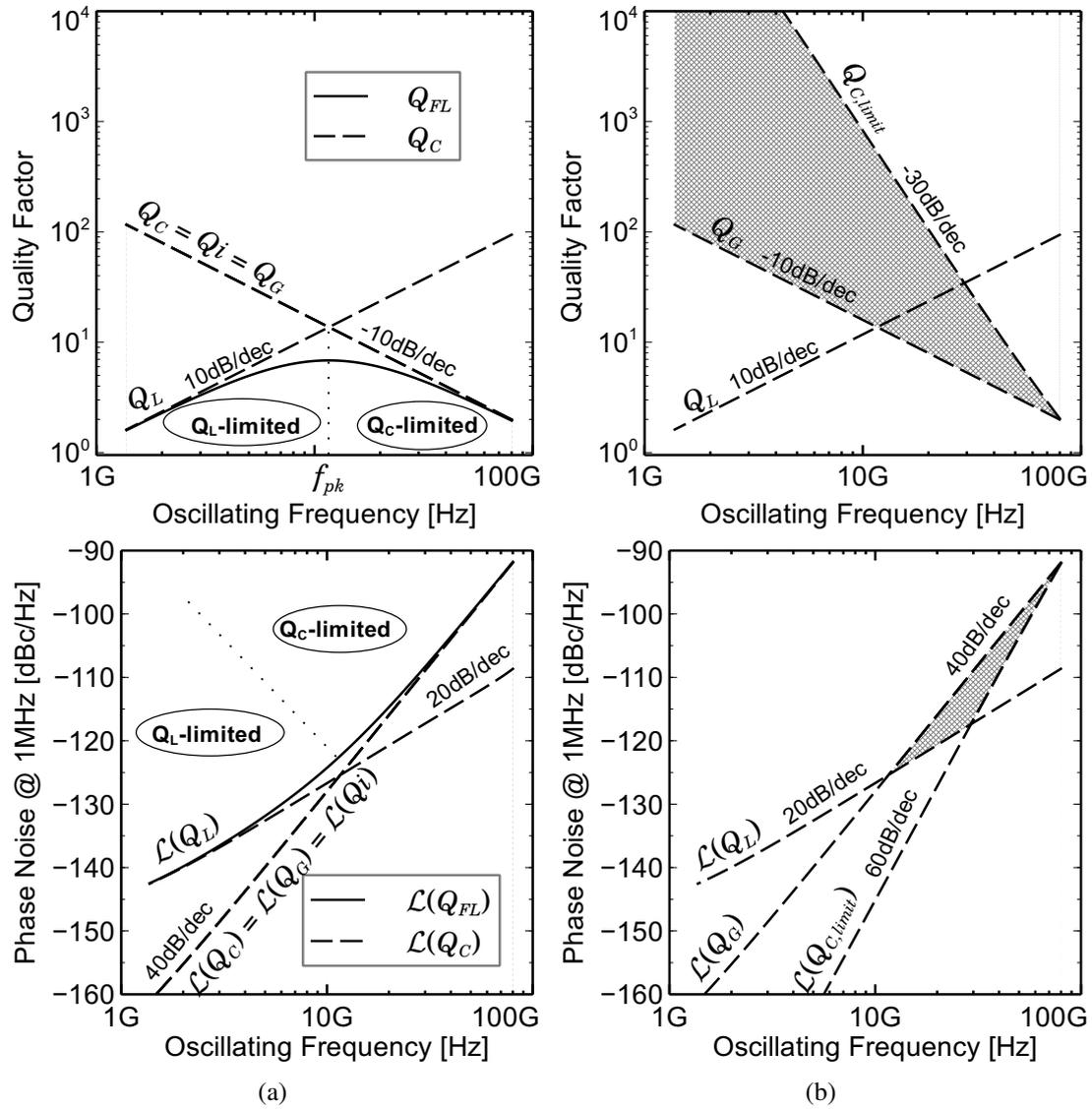


Figure 3.4: Impact of the quality factor of the fixed capacitor, Q_i , on the quality factor of the equivalent capacitance C and phase noise at 1MHz. The influence of the gm-cell output impedance is illustrated as well. (a) Case when $Q_i=Q_G$. (b) Case when $Q_G \leq Q_i \leq \infty$ for $\tau_G=1000 \times 10^{-15}$.

oscillator could have in the Q_C -limited region if the quality factor of the fixed capacitor starts to increase from Q_G to infinity.

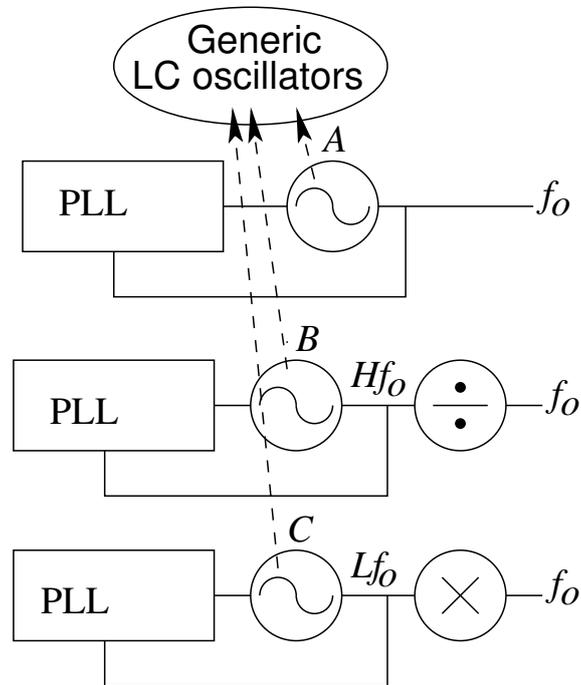


Figure 3.5: Frequency generation systems based on: fundamental, super-harmonic and sub-harmonic oscillators.

3.2 Fundamental, super-harmonic and sub-harmonic oscillators as signal sources: a $1/f^2$ phase-noise perspective

The results obtained in the previous section are used here to derive design guides for signal sources based on LC oscillators. In Fig. 3.5 three different systems to generate the same target frequency (f_o) are presented. Since the oscillators in the figure are not tuned at the target frequency, the oscillator *A* is referred as a fundamental oscillator; *B* as a super-harmonic oscillator; and *C* as a sub-harmonic oscillator. Several design metrics could be used to evaluate each particular system, among others: frequency tuning, power consumption, spectral purity, locking range, jitter, phase noise, etc. The metric to be used will depend on the specific application of the system. Systems based on sub-

harmonic oscillators followed by frequency multipliers have been commonly used in the generation of low phase noise signals in the mm-wave range. It has been observed that these systems have lower phase noise when compared to systems based on fundamental oscillators. This improvement has been commonly attributed to a better quality factor of the resonator while operating at lower frequencies. Even when this observation has been widely verified experimentally [41, 43], there are still important questions that remain open. Specifically what is the maximum improvement that can be achieved and under which conditions this improvement can be achieved, or in other words, for a given target frequency how to choose the sub-harmonic frequency that leads to a maximum improvement.

These issues are addressed here by considering that the oscillators in the Fig. 3.5, namely A , B and C with oscillating frequencies and phase noise at 1MHz given by: (f_o, \mathcal{L}_A) , (Hf_o, \mathcal{L}_B) and (Lf_o, \mathcal{L}_C) respectively, correspond to one conceptual oscillator of the Fig. 3.1. All oscillators have the same signal amplitude, gm-cell and inductor in the resonator. For each oscillator the *fixed capacitor* is set according to (3.8) to establish the desired oscillating frequency. For the oscillator B and C , it follows that: $Hf_o = n \times f_o$ and $Lf_o = f_o/n$ respectively.

In figure 3.6, a practical graphical analysis is performed to evaluate the phase noise performance of the systems in Fig. 3.5. Let's consider the case when f_o and n puts all oscillators in the Q_C -limited region and $\tau_i = \tau_G$, i.e., the *fixed capacitor* and the gm-cell output capacitance have the same quality factor. The phase noise at 1MHz of each oscillator is represented in the Fig. 3.6 by white circles. The phase noise was obtained according to the equations (3.2) - (3.7) for $\tau_i = \tau_G$ and the values of the Table I. As expected, the phase noise of the oscillators lies in an increasing line of 40 dB/dec. The operation of division and multiplication on the frequency is represented by 2 dotted axis with a slope of 20dB/dec intersecting B and C , respectively. These axis will define the path that the phase noise of each oscillator will follow after the respective

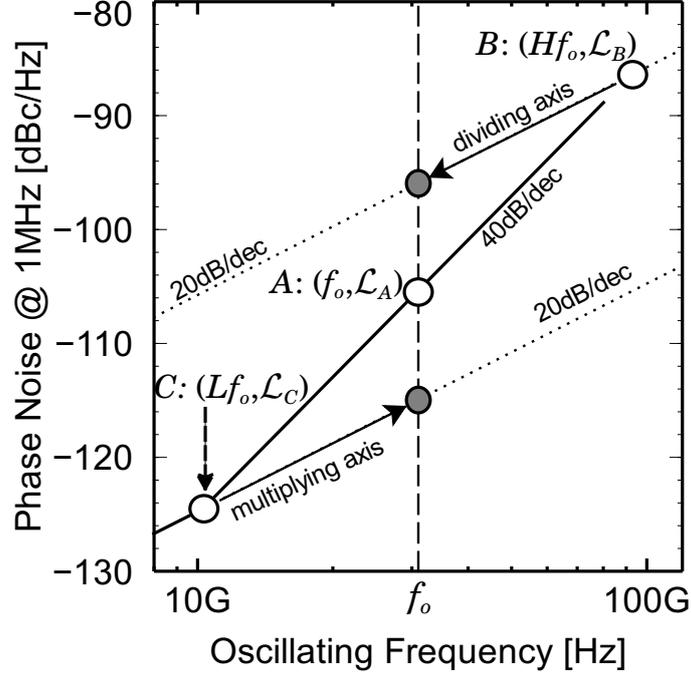


Figure 3.6: Visualization diagram of the phase noise of the 3 systems for frequency generation. $f_o = 31\text{GHz}$, $Lf_o = f_o/3$, $Hf_o = 3 \times f_o$.

frequency operation. Here it is assumed that after the frequency operations the resulting phase noise changes according to the factor $20 \times \log_{10}(n)$. The phase noise at 1MHz of the resulting signal, at the desired output frequency, is found at the intersection of the multiplication/division path with the axis of the target frequency (indicated by dark circles in the figure). From the figure, it is evident the better phase noise capabilities of a system based on a sub-harmonic and a frequency multiplier over the other approaches. Indeed, this will be the case as long as the target frequency lies on the Q_C -limited region, since in this region the phase noise increases at a proportion higher than 20 dB/dec with the oscillating frequency. The improvement in phase noise by using a sub-harmonic oscillator followed by a multiplier-by- n over a fundamental oscillator can be obtained as:

$$\Delta\mathcal{L}(n) = \mathcal{L}(\omega_o) - [\mathcal{L}(\omega_o/n) + 20 \log_{10}(n)] \quad (3.10)$$

with $\omega_o = 2\pi f_o$. Using the equation (3.7), then (3.10) results in:

$$\Delta\mathcal{L}(n) = 10 \log_{10} \left(\frac{Q_{FL}(\omega_o/n)C_{sub}}{nQ_{FL}(\omega_o)C_o} \right) \quad (3.11)$$

where Q_{FL} is the loaded quality factor in (3.2) and C_{sub} and C_o are the values of the effective parallel capacitance defined in (3.5) needed to set ω_o and ω_o/n as the oscillating frequency of the oscillators. For a given target frequency, the maximum phase noise improvement as well as the value of n can be obtained from (3.11), as

$$\frac{d}{dn}[\Delta\mathcal{L}(n)] = 0 \quad (3.12)$$

A more convenient graphical method is described as follows. Based on the figure 3.6, further improvement on the phase noise is expected as the frequency Lf_o decreases. However, as Lf_o decreases the oscillator C enters in the Q_L -limited region \mathcal{L}_C will approach $\mathcal{L}(Q_L)$. $\Delta\mathcal{L}_{max}$ is achieved at the frequency in which the phase noise starts decreasing at 20 dB/dec. This behavior is illustrated in Fig. 3.7 for the example being discussed. Here an attempt of using $Lf_o = f_o/10$ gives no further improvement. Indeed, from the diagram the maximum phase noise improvement can be estimated as:

$$\Delta\mathcal{L}_{max} = 20 \log_{10} \left(\frac{f_o}{f_{pk}} \right) \quad (3.13)$$

the estimation is more accurate as $f_o \gg f_{pk}$.

Note that if the desired output frequency f_o lies in the Q_L -limited region, no benefits are expected in using a sub-harmonic oscillator. Moreover, no benefits in terms of phase noise is expected in a system based on a super-harmonic oscillator and frequency divider. The results obtained are summarized as follows:

Sub-harmonic oscillator followed by an harmonic multiplier: When compared to a fundamental oscillator at the desired frequency, if the targeted frequency f_o is

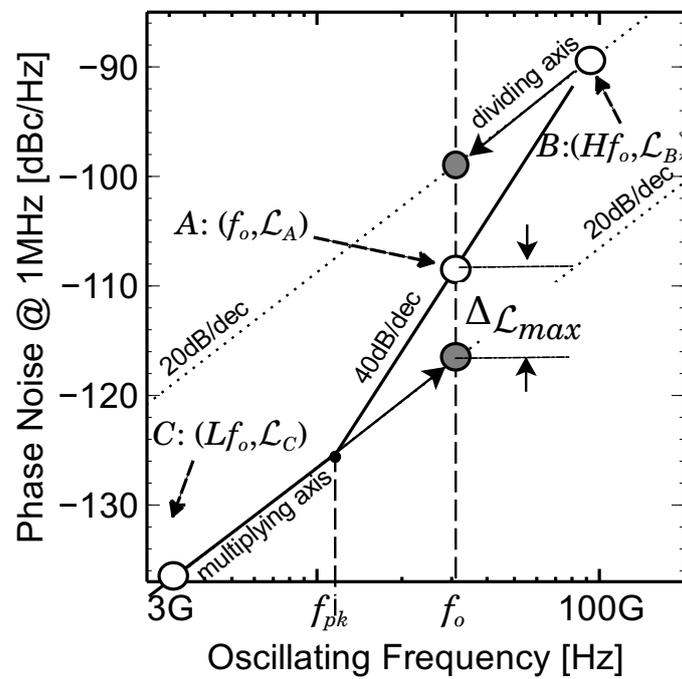


Figure 3.7: Visualization diagram of the phase noise of the 3 systems of frequency generation of Fig. 3.5: $f_o = 31\text{GHz}$, $Lf_o = f_o/10$ and $Hf_o = 3 \times f_o$. The maximum phase noise improvement $\Delta\mathcal{L}_{max}$ is graphically illustrated in the figure.

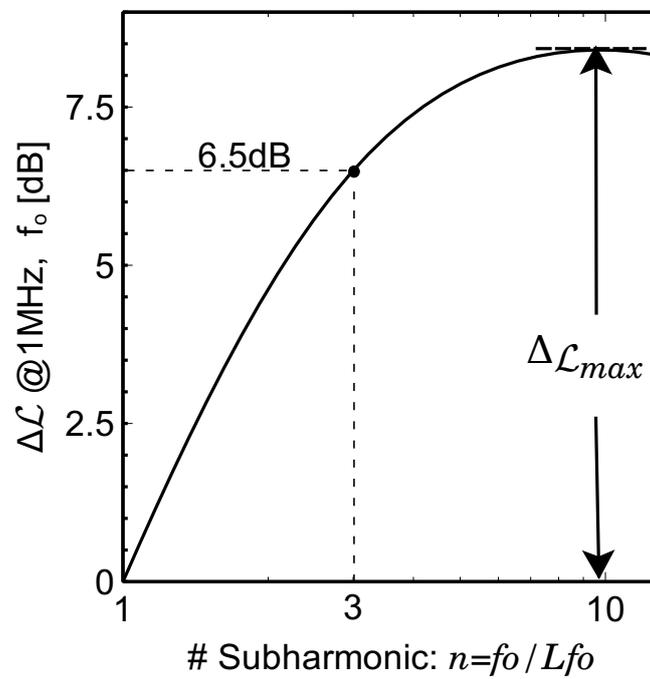


Figure 3.8: Improvement in the phase noise at 1MHz by using a system composed of a subharmonic oscillator and an ideal frequency multiplier-by- n over a fundamental oscillator at 31GHz.

higher than f_{pk} a phase noise improvement is expected. The magnitude of the improvement can be found with the Eq. (3.11). For the case when $Q_i = Q_G$, the maximum phase noise improvement is given by (3.13).

Super-harmonic oscillator followed by a frequency divider: Compared to a fundamental oscillator at the desired frequency, the phase noise degradation that a super-harmonic oscillator would have will lead to any phase noise improvement.

For the example being considered, the Fig. 3.8 shows the phase noise improvement at 1MHz, using Eq. (3.11), for $f_o = 31\text{GHz}$ versus the frequency of the sub-harmonic oscillator. Note that the maximum improvement tends to the value predicted by the Eq. (3.13) as n increases. Note that for $n = 3$, i.e., using an oscillator at 10.33GHz and a frequency tripler, results in an phase noise improvement of 6.5dB.

3.3 Calculating τ_G for the bipolar cross-coupled pair

A simplified view of the gm-cell used in [44] and introduced in the chapter 2 for the VCO is presented in Fig. 3.9. A DC-decoupling network composed of C_f and r_f was used to allow a differential amplitude of 1.4V while keeping at 0V the maximum forward voltage of the base-collector junction of each transistor, hence keeping the transistors out of the saturation region. As it is obvious from section 3.2, by determining the output *time constant* of the gm-cell (τ_G) it is possible to describe the design space for the loaded quality factor Q_{FL} as in the figure 3.4(b). However, note that for an adequate description of the phase noise in the $1/f^2$ region, the contribution of the cross-coupled pair have to be considered [1].

Considering the magnitudes of the signals involved in the cross-coupled pair and its voltage/current dependent capacitances, a large signal analysis should be performed to determine τ_G ; however to obtain a closed form equation from such analysis is not

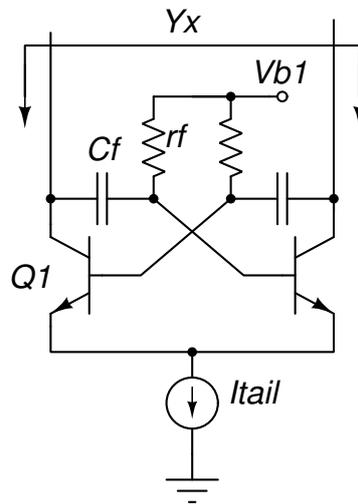


Figure 3.9: Schematic view of the bipolar cross-coupled pair used as the gm-cell.

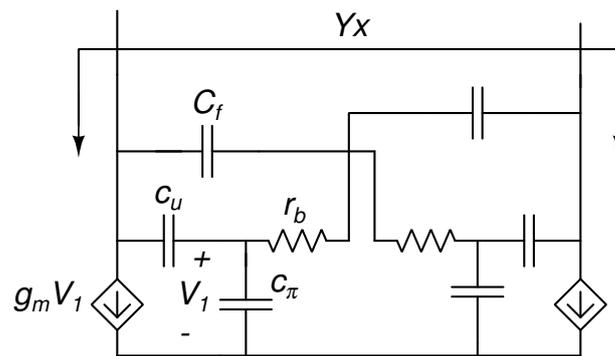


Figure 3.10: Simplified small-signal circuit of the bipolar cross-coupled pair in Fig. 3.9.

an easy task. Instead, a more instructive small signal analysis is conducted in this section based on a simplified equivalent circuit of the transistor that considers: the base resistance (r_b), transconductance (g_m), base-collector (c_u) and base-emitter (c_π) capacitances. The small-signal equivalent circuit of the cross-coupled pair is presented in Fig. 3.10. The real part of the differential input admittance Y_x is given by Eq. (3.14) and the equivalent parallel capacitance, C_{GP} , is given by Eq. (3.15).

$$\operatorname{Re}\{Y_x\} = \frac{G_x + G_T}{2D_x} \quad (3.14)$$

$$C_{GP} = \frac{\operatorname{Im}\{Y_x\}}{j\omega} = \frac{C_x + C_y}{2D_x} \quad (3.15)$$

with,

$$G_x = -\left(g_m + \omega^2 c_u c_\pi r_b\right) \left(1 + \frac{c_u + c_\pi}{C_f}\right) \quad (3.16)$$

$$G_T = \frac{c_u g_m}{C_f} \left(1 + \frac{c_u + c_\pi}{C_f}\right) + \omega^2 r_b (c_u + c_\pi) \times \left(4c_u + c_\pi + c_u g_m r_b + \frac{c_u c_\pi}{C_f}\right) \quad (3.17)$$

$$D_x = \left[1 + \frac{c_u + c_\pi}{C_f}\right]^2 + \left[\omega r_b (c_u + c_\pi)\right]^2 \quad (3.18)$$

$$C_x \approx g_m r_b (c_u + c_\pi) + 4c_u + c_\pi + g_m r_b c_u \quad (3.19)$$

$$C_y = \omega^2 c_u c_\pi r_b^2 (c_u + c_\pi) \quad (3.20)$$

Note from Eq. (3.14) that besides a negative transconductance given by Eq. (3.16), the cross-coupled pair contributes with a differential parallel resistive load, r_{GP} , given by $r_{GP} = 2D_x/G_T$. Moreover, considering the equivalence between the quality factor of the series and parallel representation of a lossy capacitor, τ_G can be obtained from:

$$\omega r_{GP} C_{GP} = \frac{1}{\omega \tau_G} \quad (3.21)$$

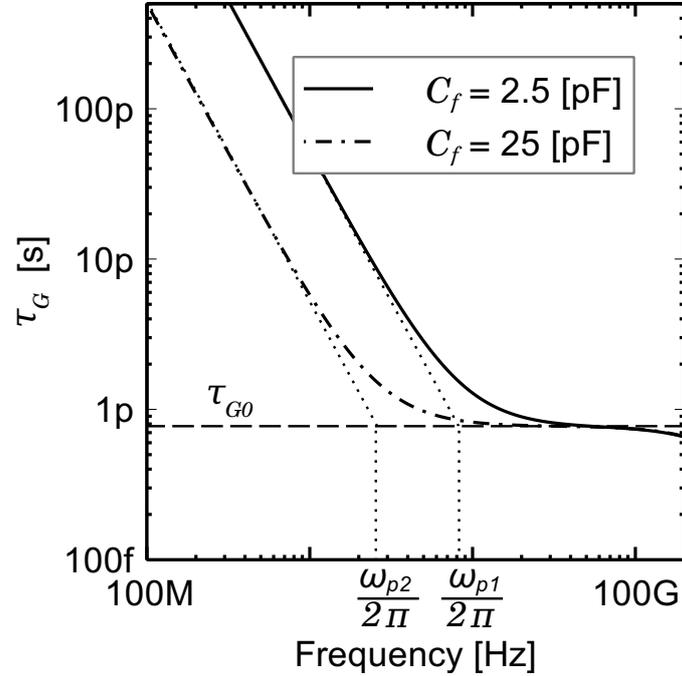


Figure 3.11: τ_G vs frequency according to equation the (3.22) of the cross-coupled pair of the Fig. 3.9. $Q1$ is a $0.3\mu\text{m}\times 2.3\mu\text{m}\times 4$ NPN transistor. $C_f=2.5\text{pF}$, $r_f=1\text{k}\Omega$. $Itail$ is set to the peak- f_t current of the transistor.

resulting in,

$$\tau_G(\omega) \approx \tau_{G0} \left(\frac{\omega_p^2}{\omega^2} + 1 \right) \quad (3.22)$$

with,

$$\frac{1}{\omega_p^2} \simeq r_b(c_u + c_\pi)(4c_u + c_\pi + g_m r_b c_u) \frac{C_f}{c_u g_m} \quad (3.23)$$

and,

$$\tau_{G0} \simeq \frac{r_b(c_u + c_\pi)(4c_u + c_\pi + c_u g_m r_b)}{g_m r_b(2c_u + c_\pi) + 4c_u + c_\pi} \quad (3.24)$$

In Fig. 3.11, τ_G as in equation (3.22) is plotted as a function of frequency for two different values of C_f , the AC-coupling capacitance in the Fig. 3.9. The small signal parameters of the transistors correspond to its operating point obtained after DC-simulations of the cross-coupled pair in Fig. 3.9 using the MEXTRAM 504.7 model

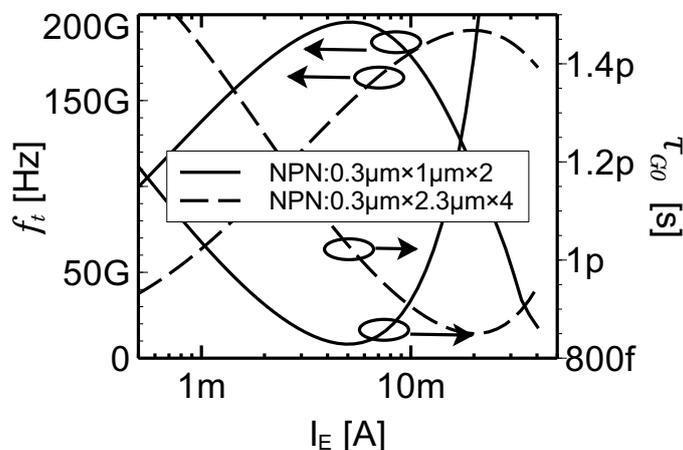


Figure 3.12: f_t and τ_{G0} as in Eq. (3.24) for different emitter current I_E for two different transistor sizes. The transistor parameters correspond to the operating point information obtained after a DC-simulations (sweeping I_{tail}) of the circuit in the Fig. 3.9. $C_f=2.5\text{pF}$ and $r_f=1\text{k}\Omega$.

provided by the foundry [45] for the NPN transistors. The current source I_{tail} was set to the current where the transistors achieve its maximum f_t . As observed in the figure, τ_{G0} (860×10^{-15} s) is indeed a good approximation for τ_G in the frequency range from 10GHz to 100GHz for $C_f=2.5$ pF. The voltage divider given by C_f and the input impedance at the base of the transistors results in a virtual increase of the load in the cross-coupled pair and the later translates in an increase of τ_G for $\omega < \omega_p$. This is verified by observing that as C_f increases ω_p decreases as illustrated in the figure.

To see the dependence of τ_{G0} with the operating point of the transistors, in Fig. 3.12 the equation (3.24) was evaluated and plotted for different emitter currents given by DC-simulations of the cross-coupled pair in the Fig. 3.9, sweeping the value of I_{tail} for two transistor sizes. Remarkably, for both transistors sizes, τ_{G0} gets its minimum as the transistor achieves its maximum f_t , thus proving the coherence of the analysis.

The results obtained in this chapter [46] will be used in the next chapter in the design of low phase noise signal sources in the 30-40 GHz frequency bands.

CHAPTER 4

LOW PHASE NOISE SIGNAL SOURCES BASED ON A SUB-HARMONIC VCO AND AN INJECTION-LOCKED FREQUENCY TRIPLER

4.1 Introduction

The recent advancements in silicon-germanium (SiGe) heterojunction transistors (HBTs) have enabled the development of circuits and methods for oscillators working near the transit frequency of the transistors. These signal sources have allowed integrated solutions for radar and imaging applications in millimeter-wave frequencies [47, 48]. The phase noise performances of millimeter wave signals continue to be significantly challenging for integrated implementations of new communication standards at these frequencies [2]. As demonstrated in the chapter 2 - 3 the trade-off between phase noise and frequency tuning range becomes more evident at mm-wave frequencies as the tank's quality factor is dominated by the capacitive part which decreases exponentially with frequency. In chapter 3 it was demonstrated that in the case of the NPN cross-coupled oscillator this fundamental trade off can be treated separately by the use of sub-harmonic oscillators followed by frequency multipliers. In these systems, the phase noise specification is met by the sub-harmonic oscillator and the tuning range depends on the bandwidth of the frequency multiplier.

In this chapter, signal sources composed for a low-IF point-to-point fixed radio system in the Ka-Band band is presented. Based on the target specifications in 1, a phase noise at 1 MHz better than -107 dBc/Hz was found to be sufficient for the targeted application. In this chapter, the design of two signals sources are discussed in detail. In the first one, the concepts and methods for the design of a system composed by a sub-harmonic VCO followed by an injection-locked frequency tripler (ILFT) is introduced. Experimental results are presented. In the second part, based on the proposed techniques a multiband LO generation is designed; experimental results are presented.

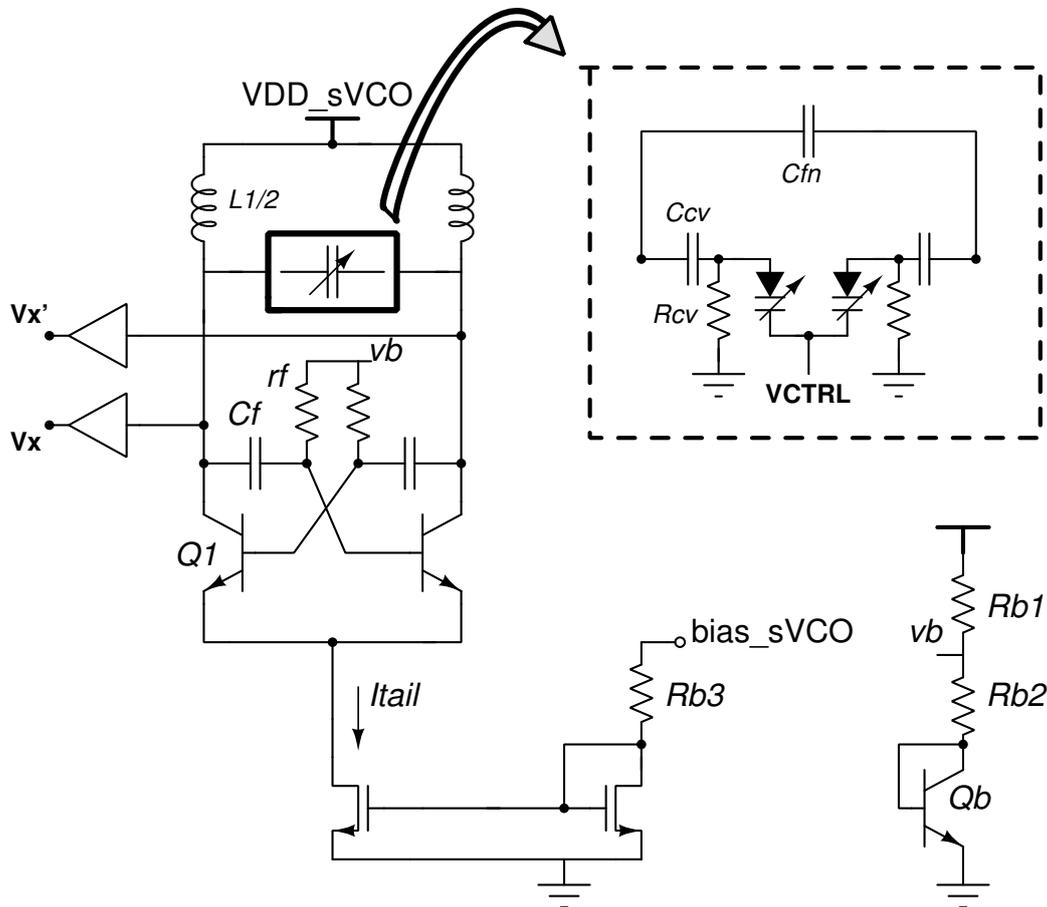


Figure 4.1: NPN cross-coupled pair LC-VCO.

4.2 The performance of a fundamental LC-VCO

An initial design using NPN cross-coupled pair LC-VCO of the Fig. 4.1 is developed to evaluate its performance. The test is performed in a realistic scenario where the oscillator is loaded by a buffer (a pair of emitter-followers) and the bias voltage and currents are generated internally. The resonator is based on an octagonal/one-turn 97pH spiral inductor¹ with an arrangement of a MiM capacitor and an ac-coupled varactor.

¹Smallest inductor provided by design kit.

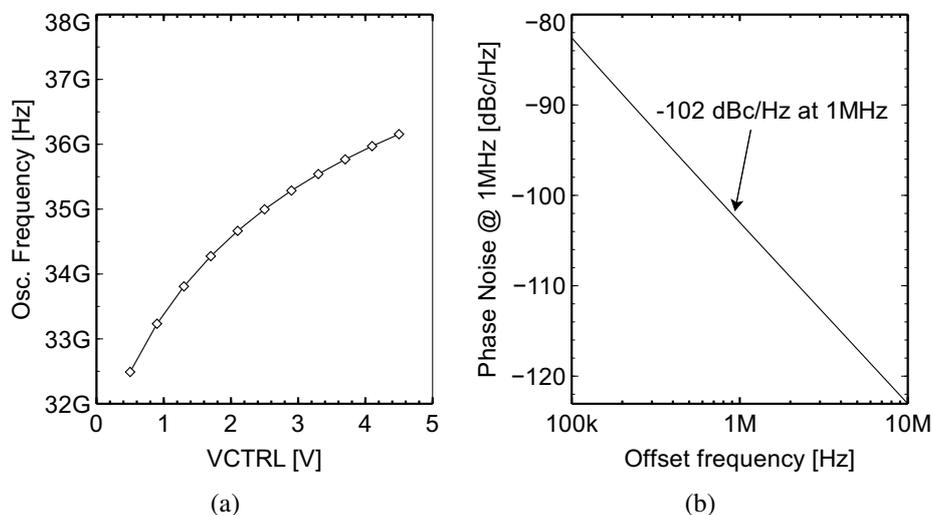


Figure 4.2: Performance of the oscillator in Fig. 4.1: a) Frequency range vs the control voltage. b) Simulated phase noise for VCTRL:0.5V.

The oscillator has NPN transistors: $0.3\mu\text{m} \times 2.3\mu\text{m} \times 2$. With $r_f = 1\text{k}\Omega$ and $C_f = 1\text{pF}$. For $v_b = 995\text{mV}$, a differential amplitude of 1.4V is obtained for $I_{tail} = 10.8\text{mA}$. The figure 4.2 shows the frequency range (a TR of 10% for VCTRL: 0.5 - 4.5V) and the phase noise at 1MHz for the worst case scenario, i.e., at 32.5GHz (VCTRL=0.5V). Indeed, within the frequency range of the VCO the worst phase noise at 1MHz is -102; 5dB far from the design target.

4.3 Design of a sub-harmonic VCO followed by an injection-locked frequency tripler (ILFT)

The suitability of a system based on a sub-harmonic VCO and a harmonic frequency multiplier is performed based on the oscillator of figure 3.1 in the chapter 3. The sub-harmonic VCO implements the same octagonal/one-turn 97pH spiral inductor and differential amplitude of 1.4V. Indeed, the values in the table I in the chapter 3 corresponds to the design variables used for the analysis. Note that the factor $\sqrt{2}$ in the amplitude ac-

counts for the conversion between a differential output to a single-ended one [49]. The LR model of the inductor is obtained such that its quality factor at 33GHz correspond to that of the spiral inductor used. The value of C_G was obtained from simulations and r_G correspond to a $\tau_G=1000 \times 10^{-15}$ [s]. Based on the results of the section 3.2 of the chapter 3, a sub-harmonic VCO and a frequency tripler is thus selected. However, in order to make a good interpretation to the phase noise improvement as obtained in the section 3.2, it is important to make two remarks:

1. The improvement as plotted in the Fig.3.8 corresponds to the case when a fixed capacitor with quality factor of $1/\omega_r\tau_G$ is used to set the oscillating frequencies. It was verified that quality factors such that are in fact a worst case scenario since, for the 97pH spiral inductor used, it is possible to design an arrangement of diode-varactor and MiM capacitor with quality factor higher than $1/\omega_r\tau_G$.
2. The analysis that led to the equation (3.11) does not consider the noise contribution of the gm-cell. For the NPN cross-coupled pair, higher I_{tail} current and base resistance r_b lead to higher noise contribution of the transistors [1].

4.3.1 Sub-harmonic VCO

The figure 4.3 shows the schematic of the sub-harmonic VCO. Considering the lower frequency band, an arrangement of varactors and switched-capacitors were use to set a 10% of tuning range. The same 97pH octagonal/one-turn spiral inductor was used. A 1.4V differential amplitude was achieved for $I_{tail}=18$ mA. The oscillator output is buffered using a pair of emitter-followers. The inductor $L2$ is used to filter high frequency noise coming from the bias circuit. The capacitor Cx is used to induce a pulsed-like waveform in the current trough the transistors, thus improving the DC-to-RF efficiency of the oscillator; similar to the class-C oscillator [50]. The fixed capacitance Cfn was implemented with a high Q MIM (Metal-Insulator-Metal) capacitor. The size

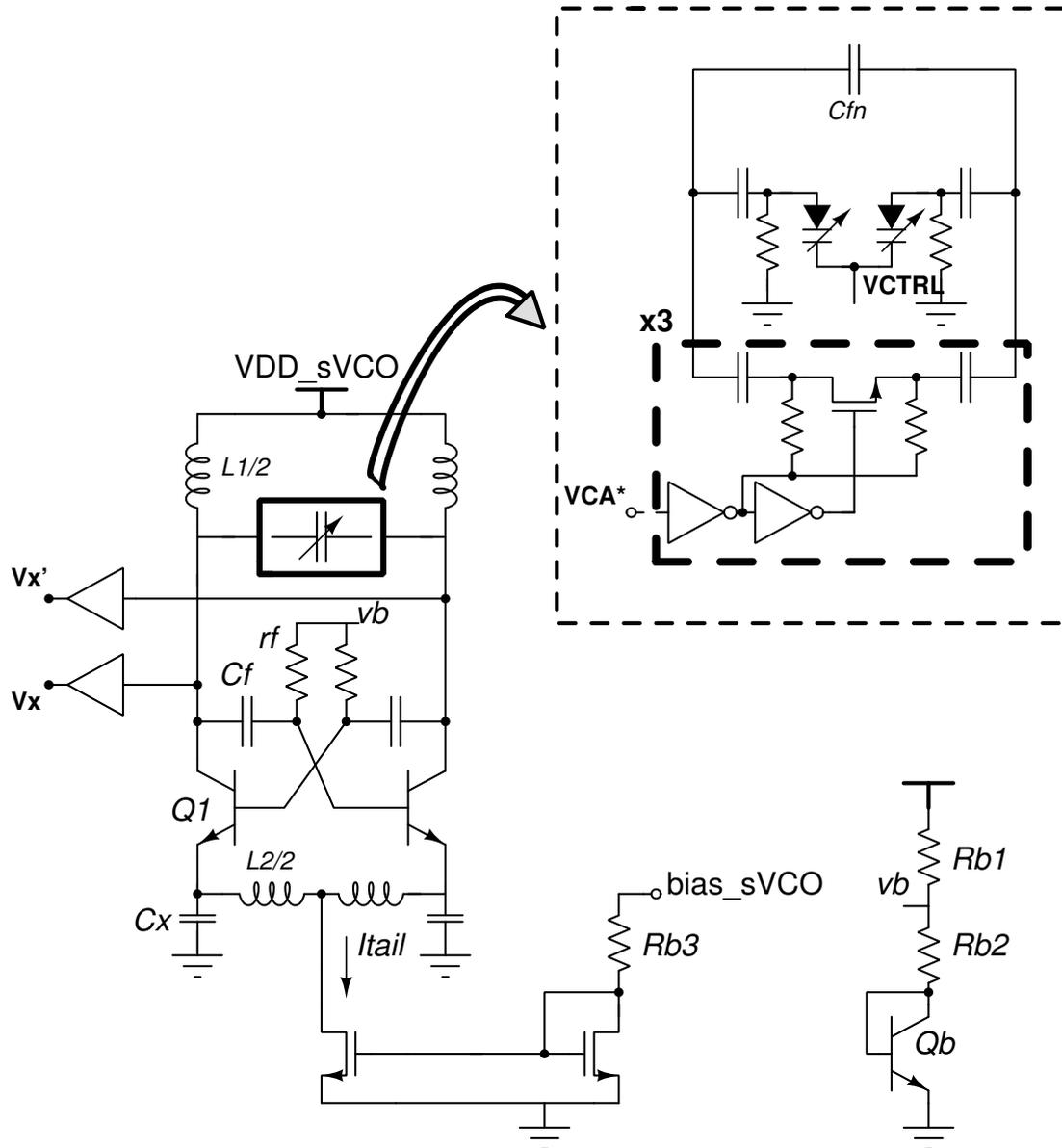


Figure 4.3: Simplified schematic view of the sub-harmonic VCO.

of the MOS switches was optimized to minimize its ON-resistance, and to not degrade the given tuning range when in the off-state. Transistor Q1 is a high-speed NPN of size $0.3\mu\text{m} \times 2.3\mu\text{m} \times 4$. Figure 4.4 shows the simulated frequency range of the VCO and the phase noise at 1MHz for all digital words of the switched capacitors. As observed

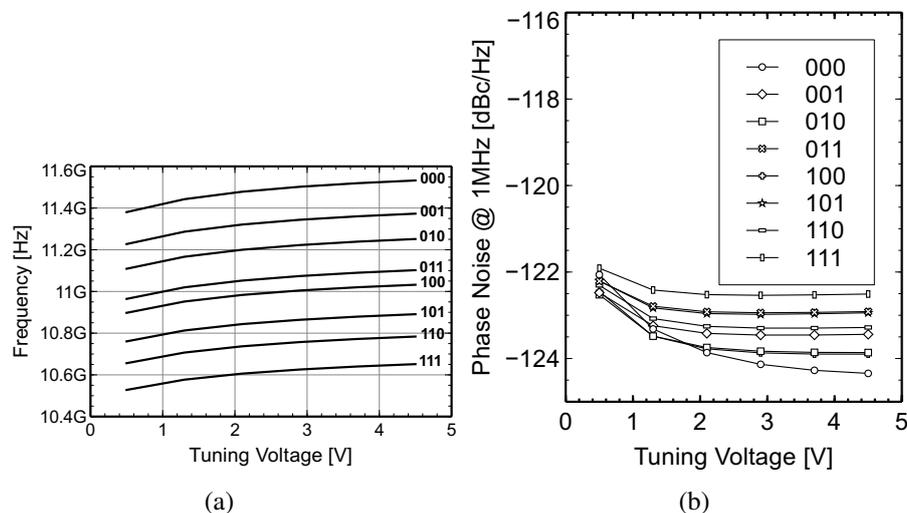


Figure 4.4: Simulated performance of the oscillator in Fig. 4.3 vs the VCTRL for all digital words of the switched capacitors. a) Frequency range. b) Phase Noise at 1MHz.

the maximum phase noise in the frequency range is -122dBc/Hz was obtained. With a multiplication-by-3 a factor of $20 \times \log_{10}(3) = 9.5\text{dB}$ should be added, having after the multiplication a maximum phase noise at 1MHz of -112.46dBc/Hz in all the frequency band. Compared to the initial attempt with a fundamental oscillator, it means 10dB of improvement in the phase noise.

4.3.2 Injection Locked Frequency Tripler (ILFT)

To accomplish with the frequency multiplication, a novel ILFT is proposed. The ILFT implements a cascoded current-biased common emitter configuration that exploits the second harmonic of the VCO output to enhance the efficiency in the generation of the injecting signal responsible for the locking of the system [44].

The circuit is based on the current-pulses generator of Fig. 4.5 and the injection-locked oscillator (ILO) of Fig. 4.6, which is tuned at $3 \times f_{VCO}$. If $3 \times f_{VCO}$ lies in the locking range of the ILO, the third harmonic component ($I_{3f_{VCO}}$) of the pulsed current I_{cx} will lock the ILO. To adjust the frequency range where the ILFT will be

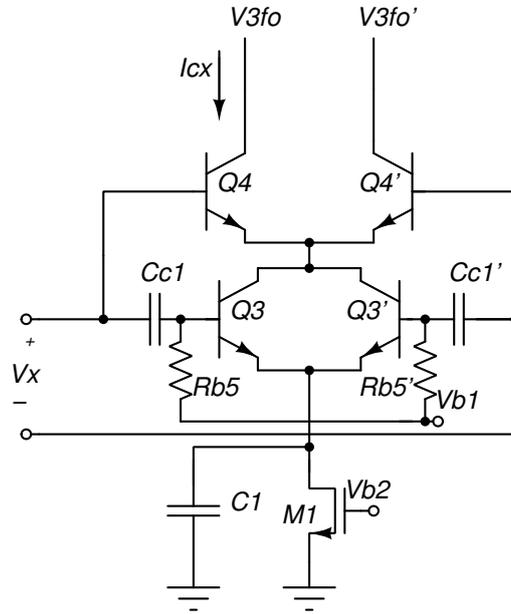


Figure 4.5: Schematic view of the Harmonic current generator.

locked to the input signal, a diode varactor was used to set its free running frequency. Furthermore, as predicted by the equation (2.3) in chapter 2, the locking-range of the circuit can be tuned by changing the magnitude of $I_{3f_{vco}}$ and I_{ILO} (see Fig. 4.6) which in turn correspond to I_{inj} and I_{osc} in (2.3). Indeed, this can be effectively done by changing the DC current through the transistors M1 and M2 in the figures 4.5 and 4.6 respectively. These capabilities in the circuit provide flexibility to set the locking range of the ILFT.

The pulsed current generator is based on the current-biased emitter/collector coupled transistors ($Q3-Q3'$) biased in class A/B. Current pulses at twice the frequency of the input signal ($2 \times f_{vco}$) are injected by transistors $Q4-Q4'$ to the ILO at f_{vco} . Compared to a voltage-biased single transistor in common emitter configuration (*conf1* showed in Fig. 4.7(a)), the current-biased topology was found to be more effective to generate a higher 3rd harmonic component for a given input voltage and frequency. The cascoded

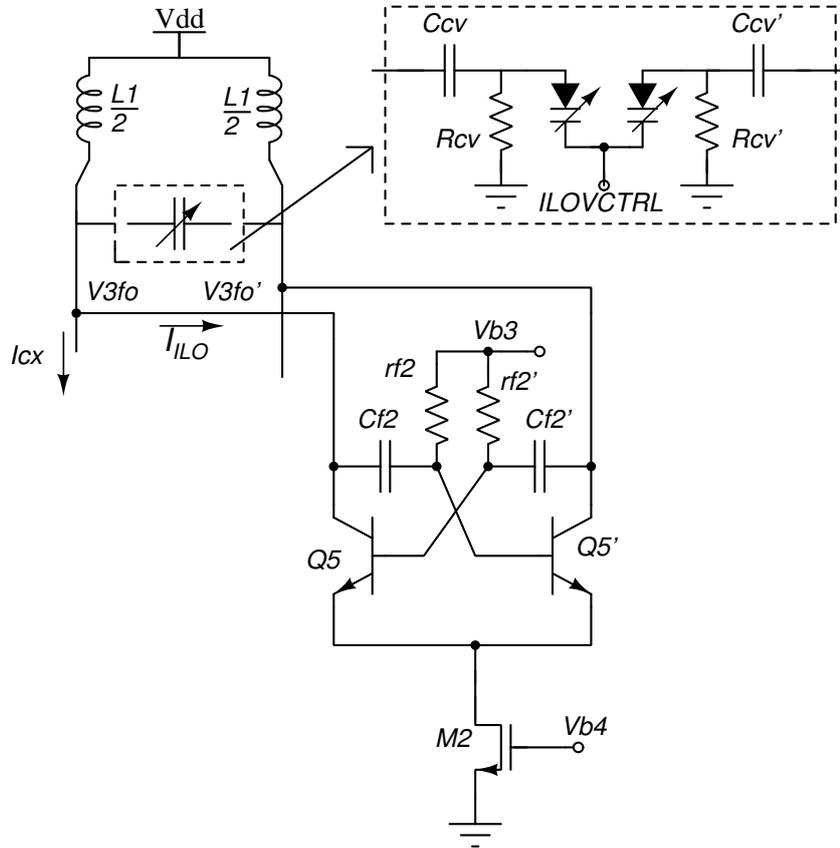


Figure 4.6: Schematic view of the injection-locked oscillator (ILO).

version of the current-biased transistor, *conf2*, is shown in Fig. 4.7(b).

The relative increment on the magnitude of $I_{3f_{vco}}$ by using the circuit *conf2* over the circuit *conf1* is plotted for several emitter areas (Fig. 4.8(a)). A maximum increment of 25% was verified. These results, which are based on harmonic-balance simulations, were obtained using the MEXTRAM 504.7 model of the transistor provided by the foundry [45]. In the simulations, the same input signal was applied and all transistors have the same size. The input signal is composed by a sinusoidal voltage at 12GHz and its 2nd harmonic at 24GHz with voltage magnitudes of 400mV and 50mV respectively². In the simulations, the average of I_{cx} for both topologies was kept the same. Note

² These values correspond to the simulated output voltage (single ended) of the VCO in Fig. 4.3

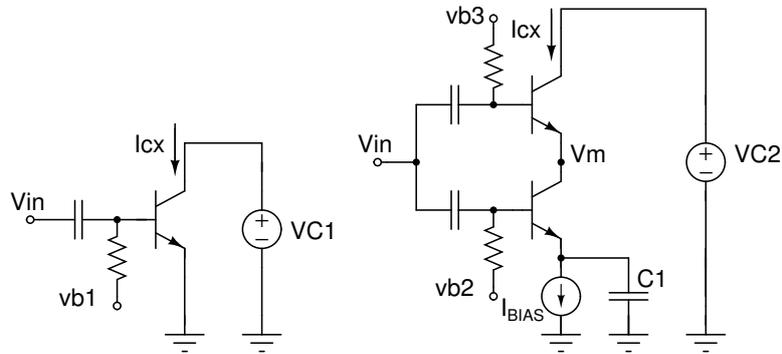


Figure 4.7: (a) Voltage-biased common emitter: *conf1*. (b) Cascoded current-biased common emitter: *conf2*

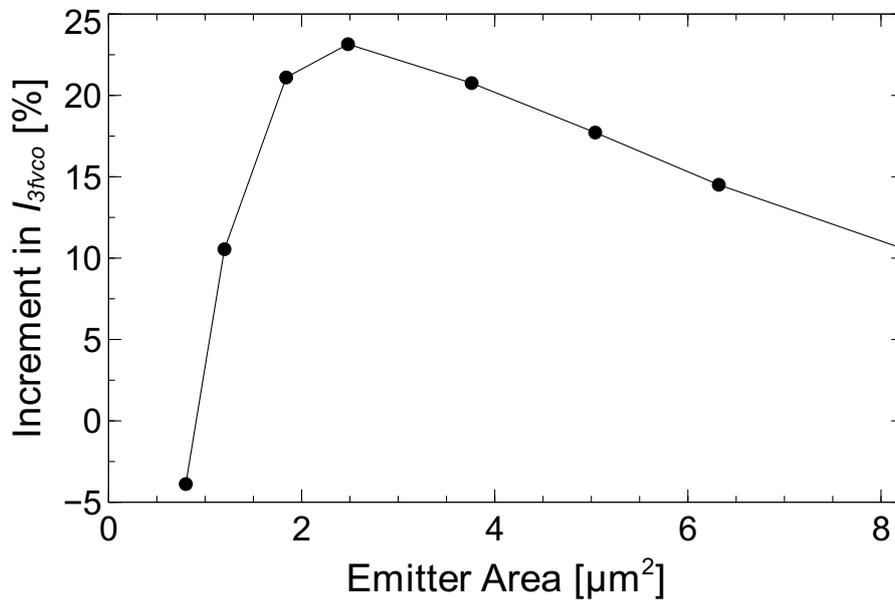


Figure 4.8: Simulation-based comparison of the relative increment in $I_{3f_{vco}}$ by using the circuit in Fig. 4.7(b) over the circuit in Fig. 4.7(a). All transistors have the same size.

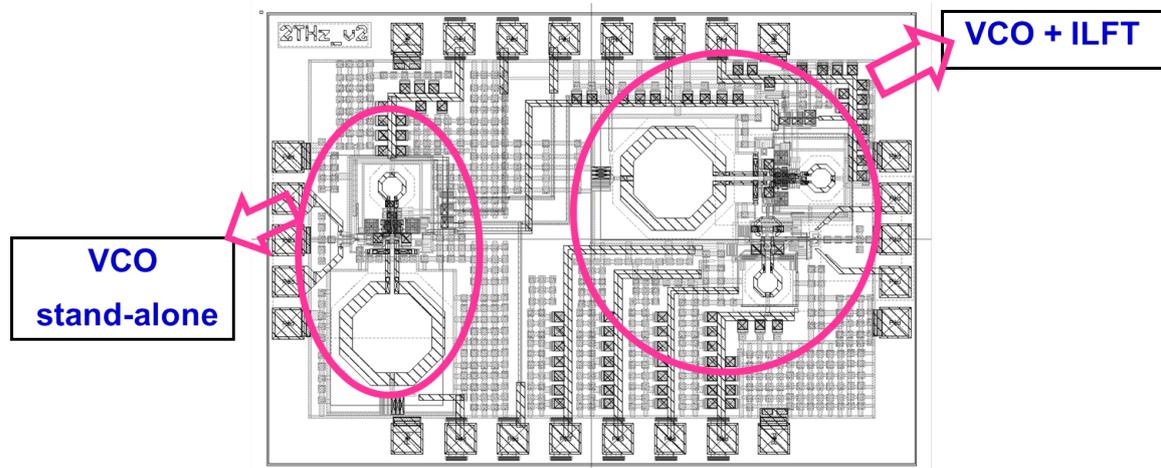


Figure 4.10: Top view of the layout of the prototype. Size: $800\mu\text{m}$ by $1200\mu\text{m}$.

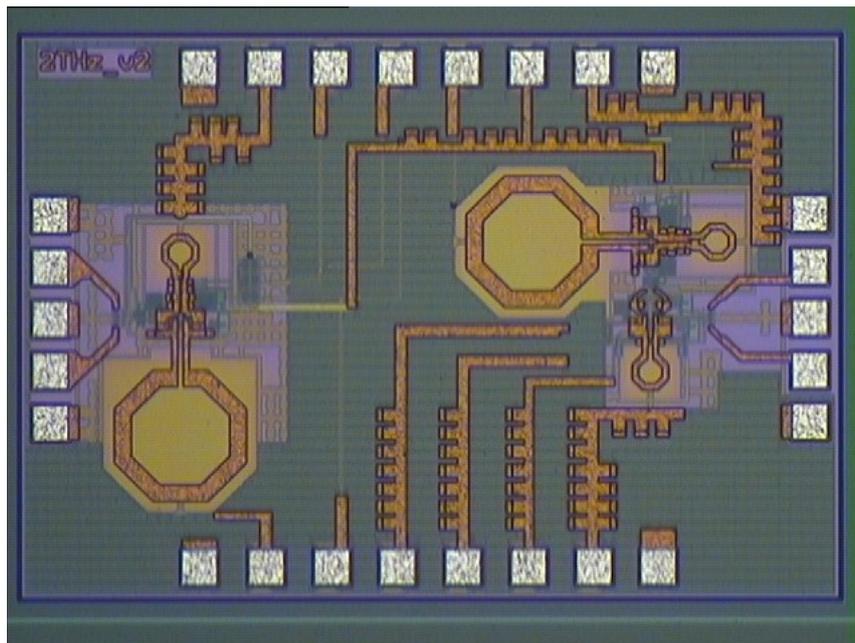


Figure 4.11: Photograph of the fabricated chip. Chip size: $800\mu\text{m}$ by $1200\mu\text{m}$.

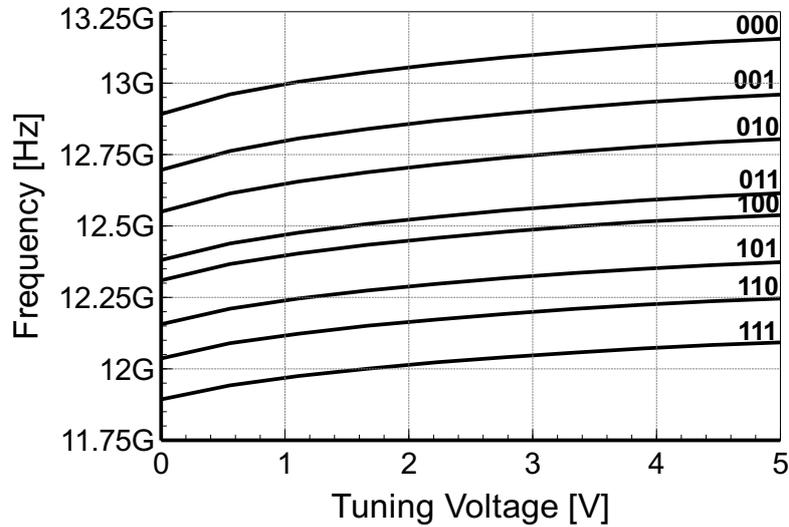


Figure 4.12: Measured tuning Range of the VCO.

4.5 Measurements

VCO

A picture of the fabricated circuit is presented in figure 4.11. The standalone version of the VCO was characterized first in a probe station. A R&S®FSU26 spectrum analyzer was used for the phase noise and frequency tuning characterization. External DC supplies were used to power the VCO. The RF signal was measured on die using a fully differential (GSGSG) probe, on which a 50Ω load was connected to one output and the other connected to the spectrum analyzer. The whole VCO consumed 28mA for a supply voltage of 2.5V. The core consumes 18mA (bias circuit 3mA) and its output buffer 10mA. Fig. 4.12 shows the tuning range for all values of the switching capacitors. The tuning voltage was varied from 0V to 5V. Fig. 4.13 shows the measured phase noise at 1MHz offset over the tuning range. A FOM³ of 184.7 at 12.8GHz is obtained. This result compares well with state-of-the-art VCOs (Table I).

³Defined as: $FOM = -PN + 20 \times \log_{10}(f_o/f_{off}) - 10 \times \log_{10}(P[mW])$

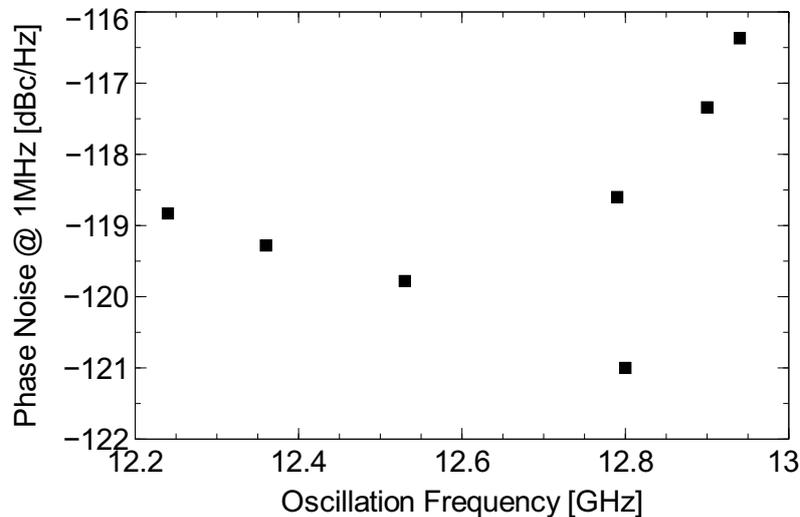


Figure 4.13: Measured phase noise at 1 MHz over the frequency range of the VCO

VCO+ILFT

In a second step, the system composed of the VCO and the ILFT was characterized. Initial measurement tests was developed in a probe station, using the same network analyzer and a down conversion harmonic mixer. The ILFT consumed 10 mA from a 2.5 V supply. The frequency range of the locked system went from 30.72 to 33.6GHz. This measurement setup was suitable to measured the DC characteristics of the circuit and the locking range. However, the amount of DC connections made it non-viable for an adequate phase noise measurement. The causes can be attributed to loop ground issues [53].

A new measurement setup was implemented to overcome this issue. The die was bonded to a PCB and a set of batteries and low-noise low-dropout (LDO) regulators were used to power up the circuit (see figure 4.14). The measurement setup is presented in figure 4.15. Although this setup provided low-noise DC sources, it lacks the flexibility to set the whole frequency range of the VCO. The characterization was done for a fixed frequency of the VCO. The power spectrum and the phase noise of the locked ILFT at

TABLE I
COMPARED TO OTHER WORKS

Ref.	Process	Freq [GHz]	TR [%]	Pdiss [mW]	PN@1MHz [dBc/Hz]	FOM*
[7]	0.35 μ m Bipolar	80	30	162.5	-97	173
[8]	0.18 μ m BiCMOS	52.5	26.5	132	-108	181.2
[9]	0.13 μ m CMOS	35	26	11	-101	
[10]	0.13 μ m BiCMOS	28	30	10.5	-104	182.7
[11]	0.13 μ m CMOS	26.9	2	5	-113	194
[12]	0.25 μ m BiCMOS	17.4	4.6	30	-113	183
[52]	0.25 μ m BiCMOS	14.24	9.1	123	-118	185.6
[13]	0.25 μ m BiCMOS	13.1	5.1	93	-123	185.6
This Work1 [44] VCO only	0.25 μ m BiCMOS	12.8	9	70	-121	184.7
This Work1 [44] VCO+ILFT	0.25 μ m BiCMOS	30.8	9	95	-112	

*Defined as: $FOM = -PN + 20 \times \log_{10}(f_o/f_{off}) - 10 \times \log_{10}(P[mW])$

30.88 GHz is shown in Fig. 4.16 and Fig. 4.17; its measured phase noise at 1 MHz is -112dBc/Hz. When compared to the figure 4.13, the system is in a locked condition for frequencies lower than the free running frequency of the VCO. This behavior was also found in simulations of the circuit.

The results obtained for the system are summarized in the table II. A comparison with other works is presented in the table I.

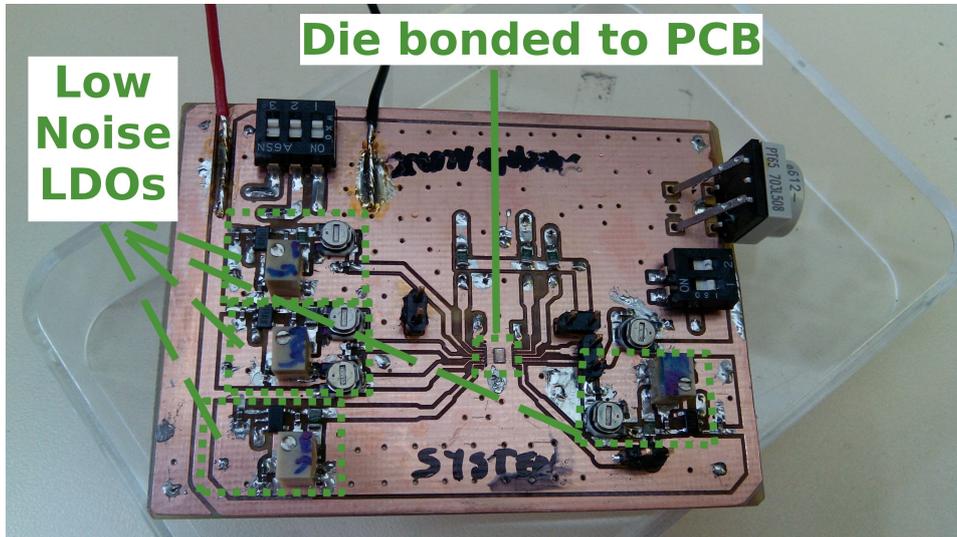


Figure 4.14: Die bonded to PCB. Low-noise LDOs are highlighted.

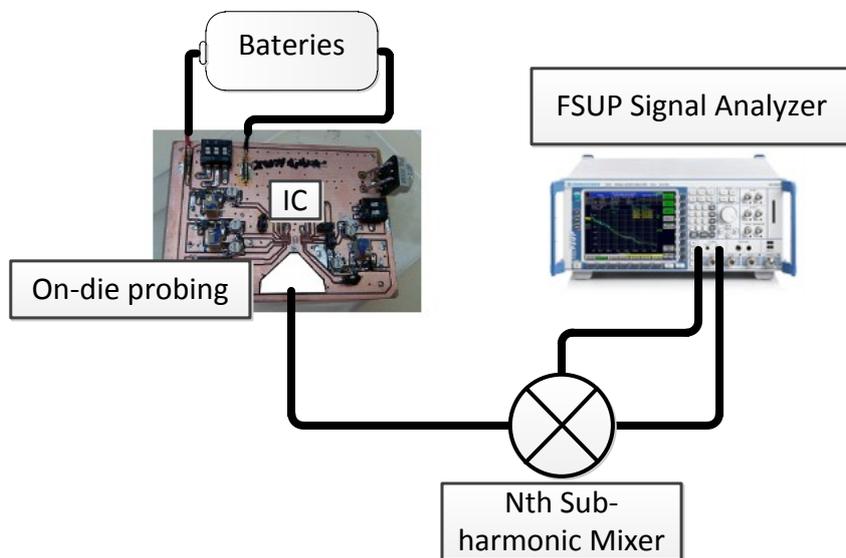


Figure 4.15: Die bonded to PCB. A setup composed of Low Noise LDOs powered by batteries were used as Power supply for the circuit.

TABLE II
SUMMARIZED PERFORMANCE OF THE SYSTEM VCO+ILFT

Parameter	Performance
Technology	QUBIC4Xi (SiGe:C 0.25 μ m)
Frequency	30.8 GHz
Tuning range	9%
Tuning Voltage Range	0.5V - 4.5V
SSB Phase Noise @ 1MHz	-112 dBc/Hz
RF output power at 30.8GHz	-7 dBm
Supply current	38 mA
VDD	2.5V

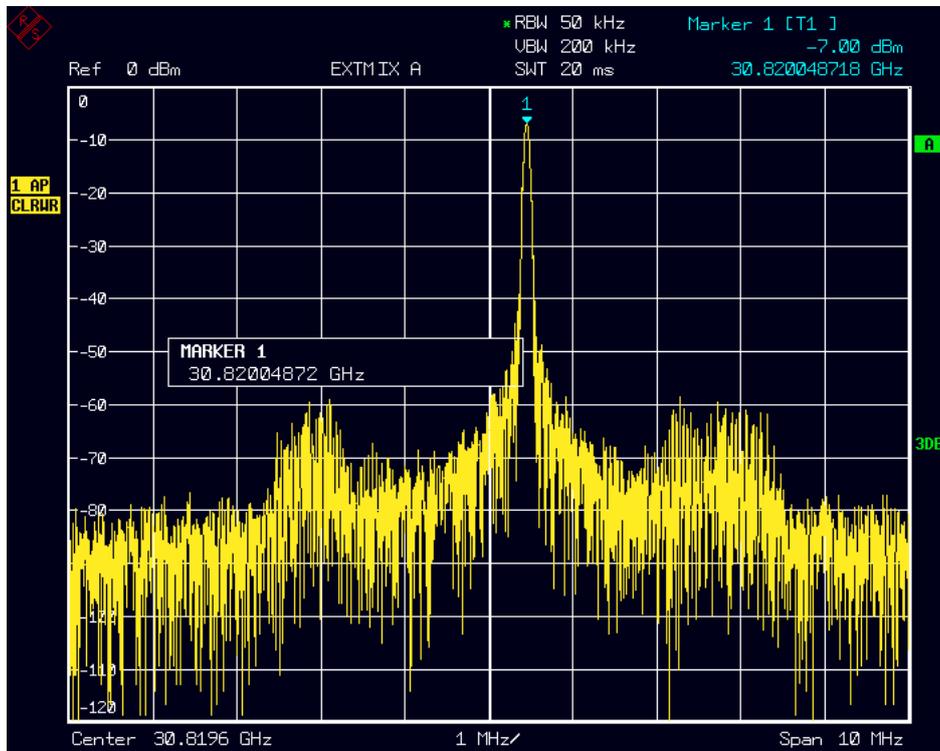


Figure 4.16: Measured spectrum of the ILFT when locked to the VCO.

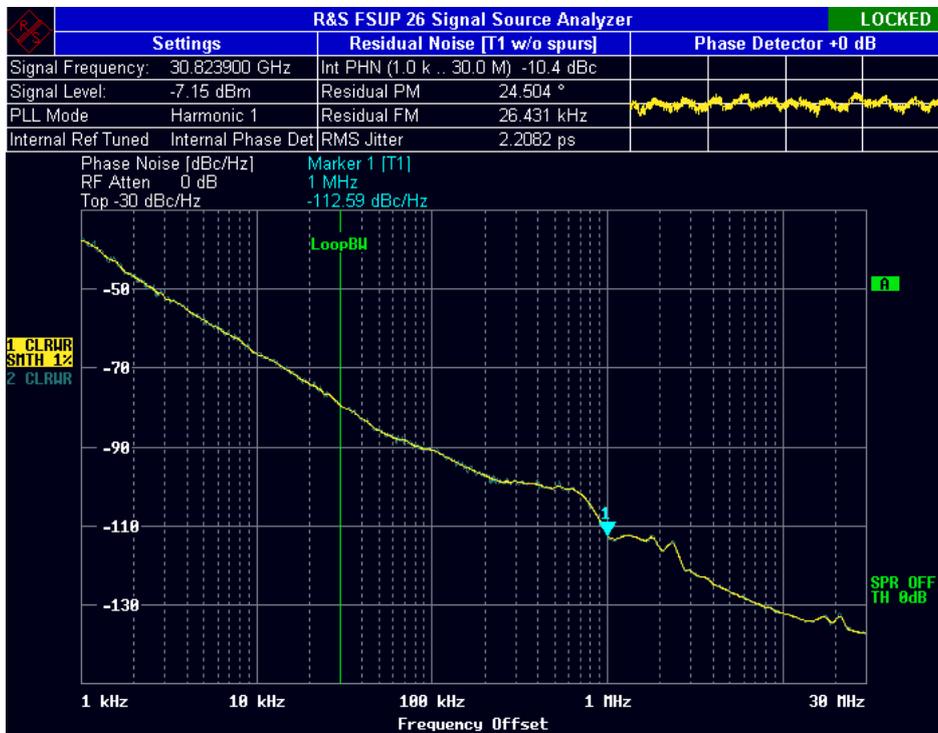


Figure 4.17: Measured phase noise at 1 MHz of the ILFT when locked to the VCO.

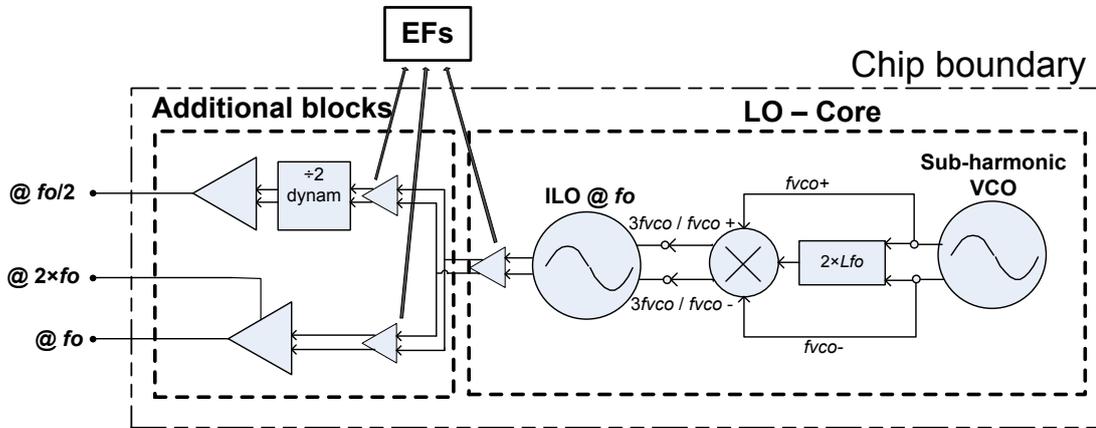


Figure 4.18: Blocks description of a multiband generation.

4.6 Multiband LO generation

The previous blocks proves the feasibility to generate a low phase noise LO signal, even in the low-end millimeter wave frequencies, from sub-harmonic oscillator and a harmonic frequency multiplier. This signal is used as reference for a multiband generation system providing signals at $f_o/2$ and $2 \times f_o$ and thus extending the functionality of the circuits and methods proposed. Starting from the blocks already designed, a re-design of the metal interconnections was enough to tune the central frequency at 34GHz for a simulated tuning range of 10%.

A block description of the system is depicted in figure 4.18, the figure shows the different signal paths. The $f_o/2$ signal is generated from a frequency divider and then followed by an output buffer which provides the driving capabilities and output power for a 50Ω RF output. Similarly, an output buffer is implemented to provide proper signal power (to a 50Ω load) to the f_o signal. The signal at $2 \times f_o$ is taken directly from this buffer.

As it is highlighted in the figure 4.18, emitter-followers (EFs) are used to distribute the signals among the different blocks, serving as well as inter-stage buffers that pro-

vides isolation to the LO-core. The wideband nature of the emitter-followers were preferred over tuned amplifiers that could be impacted from process variations that could result in strong attenuation of the desired signals. Electromagnetic simulations were used to characterize the interconnections at the f_o and $2 \times f_o$ signal paths.

4.7 Frequency divider (div-by-2)

Frequency dividers can be classified in static, injection-locked or regenerative. Static dividers have in general wide input frequency range but at mm-wave frequencies, this comes with a high power consumption due to the charging/discharging dynamics for the input/output capacitances involved in the circuit [31,54]. On the other hand, even at mm-wave frequencies the injection-locked dividers can have low power consumption but a reduced input frequency range. Finally, regenerative dividers are a good compromise between the previous categories. It has moderate input frequency range and power consumption. This topology is used as the first divider in high division factors for mm-wave applications [7, 55]. For aforementioned characteristics the Miller divider was selected as the divide-by-two block of the figure 4.18.

4.7.1 Miller divider

This circuit is based on the regenerative principle. A conceptual block representing the principle of operation is depicted in the Fig. 4.19. The transimpedance amplifier (TIA) performs two roles: to give a low-pass filtering action in the loop and to provide gain in the pass band [56]. Under proper operation of the circuit, at the mixer output the main frequency components are $f_{in} - f_{out}$ and $f_{in} + f_{out}$ ⁴. The upper band component is filtered by the TIA, having at the output the following relation for the steady state

⁴In the case of a double-balanced mixer its odd harmonics are also present.

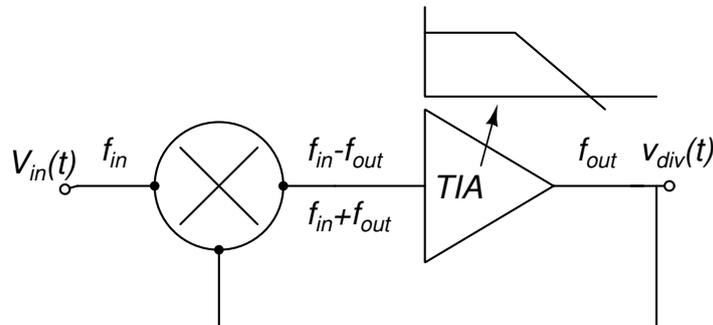


Figure 4.19: Miller frequency divider with Transimpedance amplifier (TIA).

response:

$$f_{out} = f_{in} - f_{out}$$

$$f_{out} = \frac{f_{in}}{2}$$

In a real circuit scenario a signal at $f_{in}/2$, caused either at the power-up state or by any small signal perturbation, will be present in the loop and then the regenerative action of the loop builds and sustains this signal [57]. The maximum input frequency (f_{max}) for proper division is mainly determined by the frequency (f_u) at which the closed-loop gain (limited by both the mixer and the TIA) falls to unit. The minimum input frequency is given by $f_{max}/3$; otherwise the upper frequency band after the mixer is not suppressed by the filter action of the TIA and the circuit fails to divide [31].

The schematic view of the divider at the transistor level is depicted in Fig. 4.20, it is based on the implementation in [56]. The mixer uses a double-balanced Gilbert cell and the TIA a differential pair with resistive feedback followed by two emitter-followers. The circuit used for the bias voltages is in the figure 4.21.

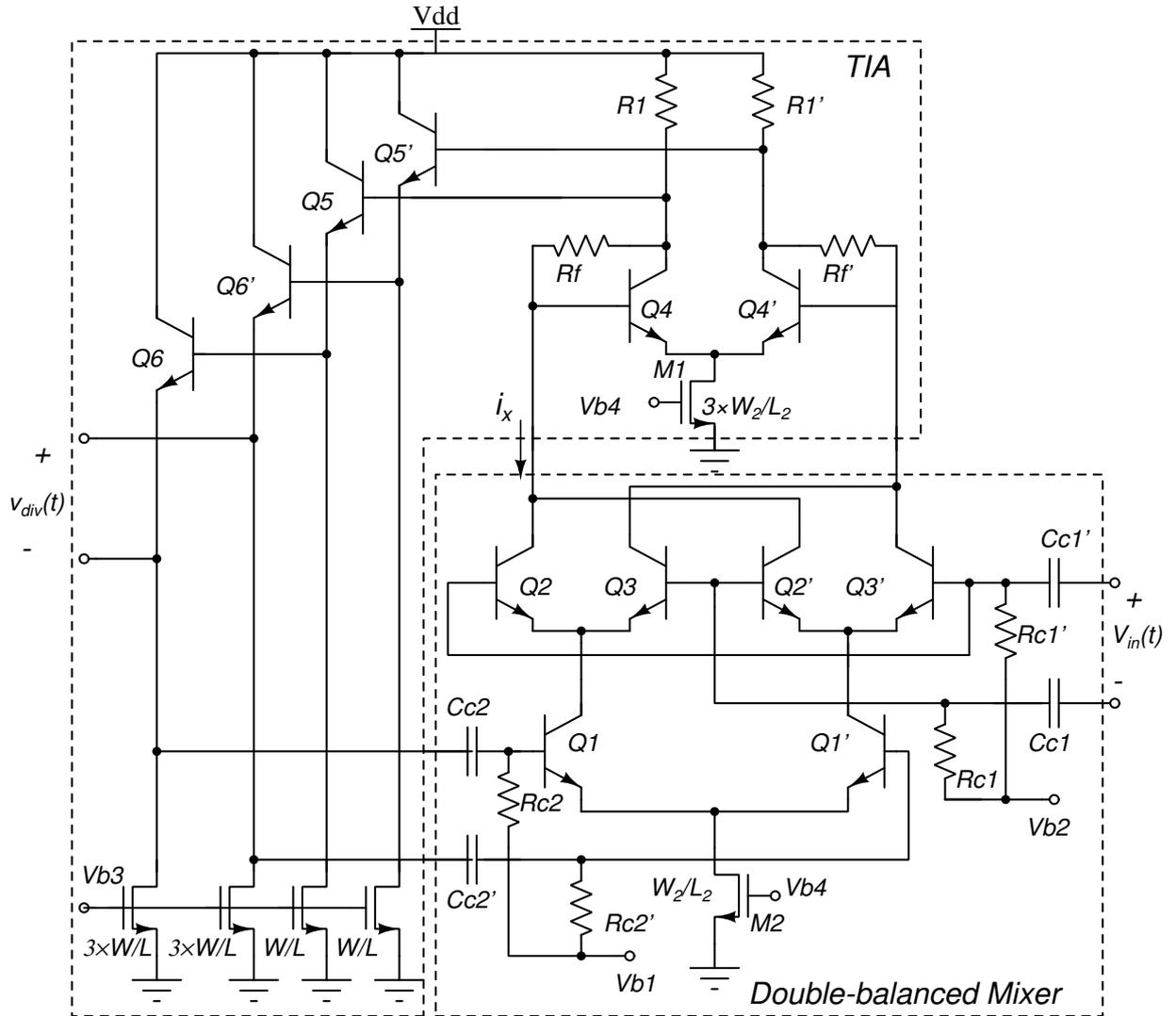


Figure 4.20: Schematic view of the Miller divider.

Transimpedance amplifier (TIA)

The sensitivity of the divider⁵ and the input frequency range are defined by the gain and the cutoff frequency of the loop. For a given bias current of the TIA the loop gain can be increased by increasing both $R1$ and Rf or by increasing the bias current of the transconductance stage in the double-balanced mixer. The cutoff frequency of the loop

⁵Defined here as the lower input voltage for proper division.

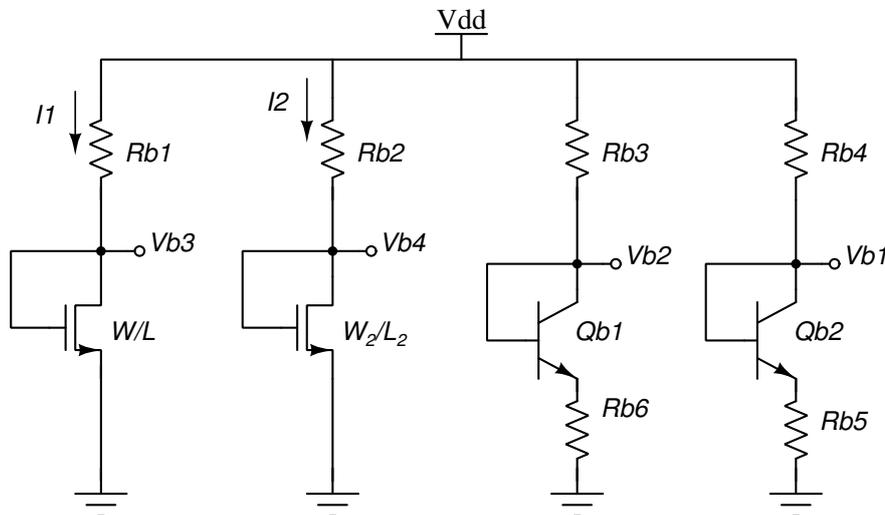


Figure 4.21: Bias circuit for the Miller divider.

gain is determined by both the mixer and the TIA. In the TIA, increasing its bias current increase its cutoff frequency. Note that $R1$, Rf , $I1$ (the DC current passing through M1) and $I2$ (the DC current passing through M2) should be carefully chosen to let enough voltage room for the V_{ds} voltage of the bias transistor M1.

Double-balanced mixer

The Gilbert cell consists of a differential voltage-to-current converter, called transconductance stage, and a switching quad formed by two cross-coupled differential pairs. The transconductance stage is formed by the transistors $Q1$ and $Q1'$, and the switching pairs by transistors $Q2$, $Q3$, $Q2'$ and $Q3'$. The switching quad is driven by the buffered output of the ILFT according to the Fig. 4.18 and the transconductance stage by the output of the TIA as in the figure 4.19. Considering that:

1. the magnitude of the input signal V_{in} with frequency f_{in} , is capable of turning on/off the switching quad,
2. the output conductance of the transistors is negligible,

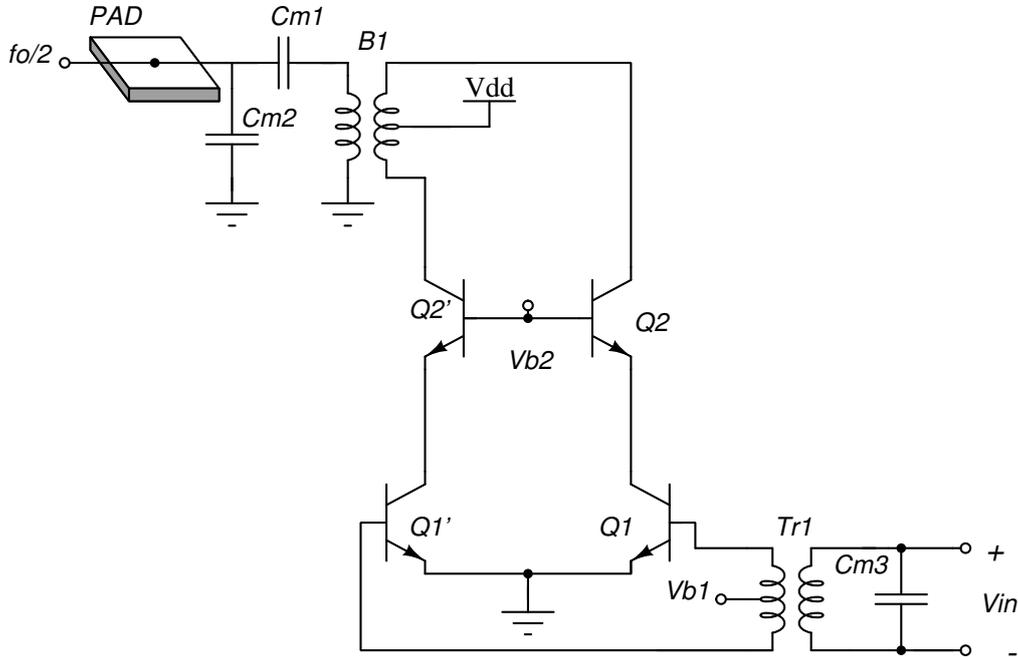


Figure 4.22: Schematic view of the output buffer for the 18GHz output.

then, the magnitude of the small signal current i_x , as in the Fig. 4.20, at the frequency $f_{in}/2$ is given by [58]:

$$i_x = -\frac{g_m}{\pi} v_{div} \quad (4.1)$$

being v_{div} the output signal of the TIA according to the Fig. 4.19.

4.8 Output buffers

The designs are based on a cascode amplifier biased in class A of the figures 4.22 and 4.23. This topology provides good input/output port isolation while providing adequate power gain [58]. In both buffers, for a power supply of 2.5V, 20 mA (10 mA per branch) of DC current was enough to provide an output signal power higher than 3dBm over a 50Ω load. In both buffers, the common-emitter transistor is a high-speed NPN with

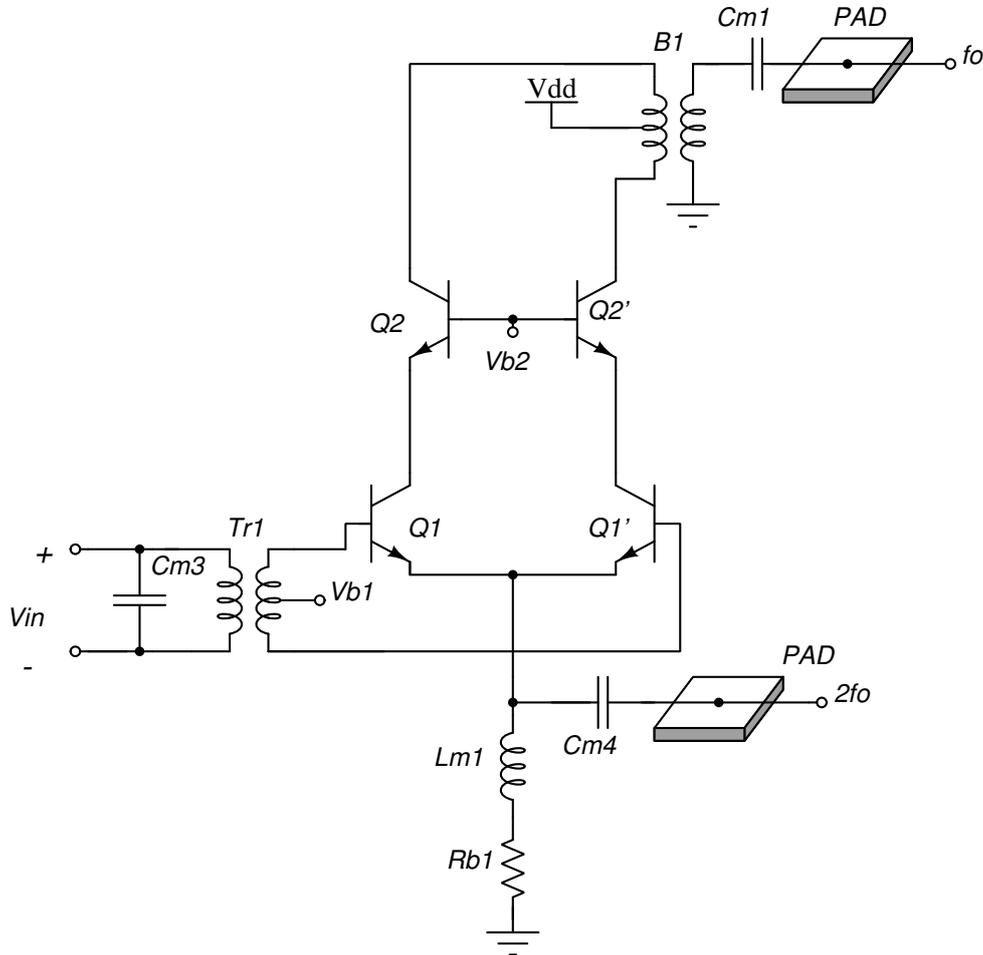


Figure 4.23: Schematic view of the output buffer for the 36GHz output. An output at 72GHz is derived.

emitter area set to achieve the maximum f_t . For the cascode transistor a high-voltage NPN was used. Since the previous stage of the buffers are emitter-follower (i.e., a stage with low output impedance), a strategy based on strong matching [59] is used. In the strong matching technique a low output (input) impedance is matched with a high input (output) impedance. Thus, a high input impedance of the buffers is targeted. This was accomplished by resonating (at the frequency of interest) the capacitive input impedance of the buffers with a parallel inductance. The differential nature of the signals led naturally to the use of a transformer. In both designs 1:1 transformer is used. As

observed in the figures 4.22 and 4.23, the center tap at the secondary winding is used to bias the buffers.

In both buffers, the output matching network is accomplished using baluns. Indeed, after a load-pull analysis the optimum impedance Z_{opt} at the transistors collectors is found. The matching network use the balun to transform the 50Ω load to Z_{opt} .

Electromagnetic (EM) simulations of the PAD were performed to characterize it. The results of the EM simulation, s-parameters (for different frequencies in a broad frequency range) were taken into account during the simulations and all the stages of the design, including the design of the input/output matching network. In a similar way, EM simulations for the interconnections associated to the layout were performed and considered in the design of both input/output matching networks of the 36GHz buffer. For the 18GHz buffer, a similar approach was used but, due to its lower frequencies, the impact of the interconnections in the layout was evaluated using RLC extraction.

By taking the output of the common emitter node (Fig. 4.23) the signal at $2 \times f_o$ can be obtained. This technique is inspired from the frequency doubler described in [60]. Note that the resistance $Rb1$ sets the current in the amplifier. The inductance $Lm1$ and capacitance $Cm4$ were set to maximize the output power. This modification to the buffer proves to be enough for a simulated output power of -15dBm in the frequency band.

4.9 System Integration and Layout considerations

In figure 4.24 the schematic view of the multiband LO generation with the PADs assignment for the supply, bias and tuning voltages. The whole system has three RF ports at f_o , $f_o/2$ and $2 \times f_o$. Note that all blocks in the system work in differential mode until the output buffers on which the differential to single-ended conversion in f_o and $f_o/2$ signal paths takes place. As observed in the figure, the blocks do not share a single

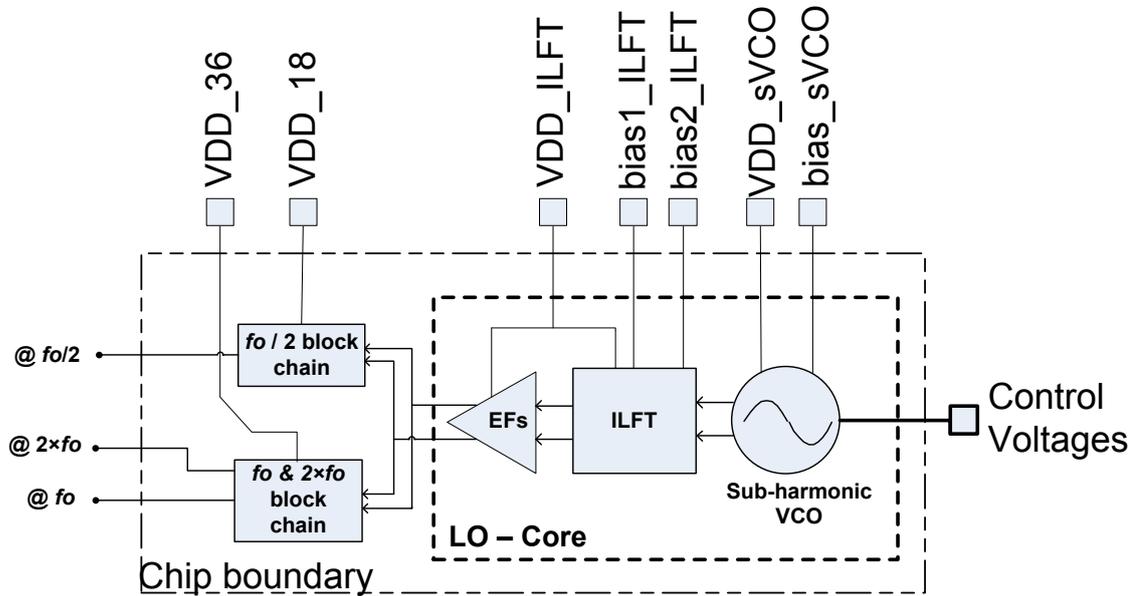


Figure 4.24: Schematic view of the multiband LO generation with PADS assignment for the Supply, bias and control voltages.

voltage supply (VDD). This was intended in order to have flexibility to enable/disable the main blocks of the system during the measurements.

In Fig. 4.25, the layout of the system is presented. Since input (output) matching network at the output buffers implements transformers (baluns), a highly compact layout and an area efficient arrangement of the blocks was achieved. It is important to highlight that a 50Ω load have to be connected to the f_o and $f_o/2$ ports before the power-up and during the measurements. Baluns could constantly and continuously charge the PAD's capacitance to high voltages. The placement and routing between the blocks were carefully performed having in the center of the chip the LO-core, composed by the VCO and the ILFT. The block chain for the f_o and $f_o/2$ signals were each one disposed at opposite sides of the die thus minimizing unwanted coupling between the ports. In the same manner, the DC-pads and the $2 \times f_o$ signal are opposed each other.

Three GSG PADs correspond to the RF outputs. Different to the previous prototype (see figure 4.10) all DC-pads were located at the same side of the die, this arrangement allows the use of a single DC multi-contact wedge for fully on-die characterization of the circuit. Moreover, all DC-pads have ESD protections⁶ to overvoltages between *line-to-ground*, i.e. the excess charge of the line is conducted to the global ground net. Since the different blocks do not share a the same VDD, no ESD protection from *VDD-to-line* were used.

On the other hand, considering the amount of signals present, bypass capacitors (MiM capacitors) were used at several DC-bias points in order to minimize unwanted signal coupling. Furthermore, electromagnetic simulations were performed to characterize (via small signal s-parameters) the interconnections in the f_o and $2 \times f_o$ block chain. These s-parameters information were feedback during the post-layout simulations. In the case of the $f_o/2$ block chain, due its lower frequency, RLC extraction was used to model the interconnections.

A picture of the fabricated circuit is showed in figure 4.26.

⁶Provided as standard-cells from the foundry.

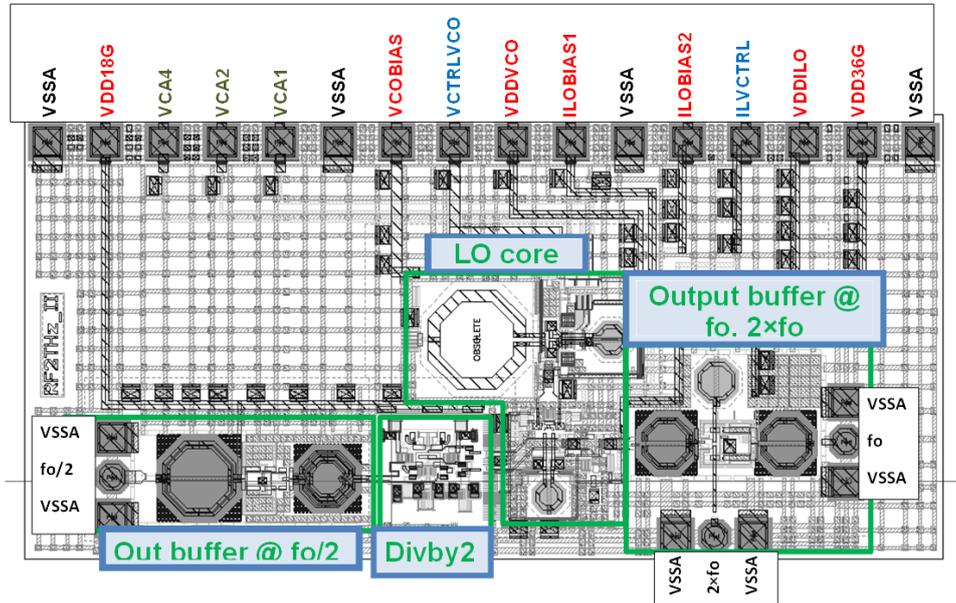


Figure 4.25: Top view layout for a multiband LO generation. Size without PADS: $2000 \times 750 \mu\text{m}^2$

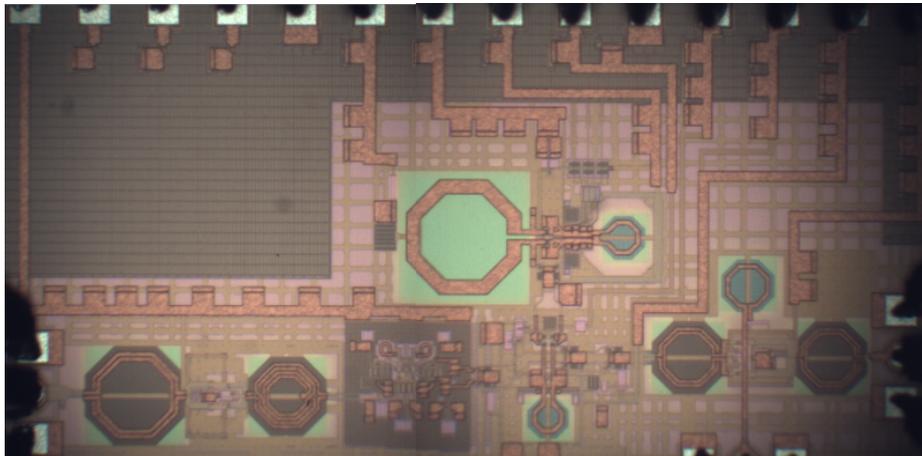


Figure 4.26: Micro-photograph of the fabricated circuit. Size without PADS: $2000 \times 750 \mu\text{m}^2$

4.10 Measurements

On-die measurements were performed for the characterization of the circuit. The measurement setup is depicted in figure 4.27. Since all matching networks associated

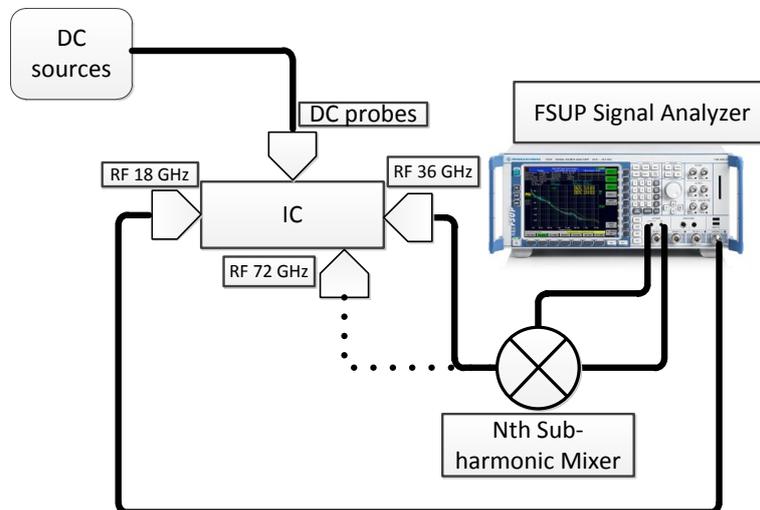


Figure 4.27: Measurement setup for the multiband LO generation.

to each RF ports are capacitively coupled to their respective GSG PADS, the signals can be directly connected to the equipment avoiding the use of bias tee. As can be observed in the figure, the two channels of the signal analyzer were used. Indeed, similar to the previous tests in section 4.5, the channel that allows a frequency extension, by using a sub-harmonic mixer, was used to measure either the signal at f_o or $2 \times f_o$.

A DC multi-contact wedge from *Picoprobe* was used to provide the required DC-voltages of the circuit. The wedge provides 16 DC probe needles, each one with a high quality 10nF bypass capacitor within close proximity to the probe tip, therefore minimizing the associated series inductance. The figure 4.28 shows a picture of the setup as well as the equipment used.

Finally, all tests were performed for a temperature of 25°C and the nominal voltage for the supply and bias voltages of the blocks (see figure 4.24) is 2.5V.

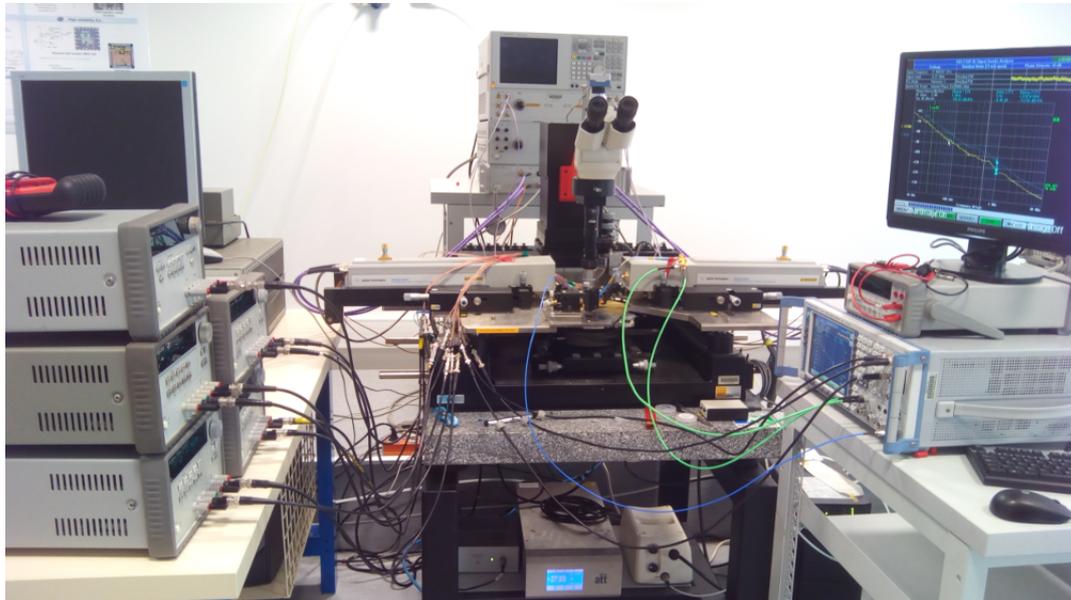


Figure 4.28: Measurement setup.

f_o -port

In order to verify the functional characteristics of the system, the unlocked condition was first verified. For this, the sub-harmonic VCO was disabled by setting its bias and supply voltage to 0V. The measured spectrum in the unlocked state is presented in figure 4.29. As expected, in the unlocked condition the response of the free-running ILFT, after being amplified, is present at the f_o -port. The free-running frequency of the ILFT was 32GHz. The measured phase noise in the unlocked condition is presented in the figure 4.30. The phase noise at 1MHz of the 32GHz signal is -86.43dBc/Hz.

In the next test, the sub-harmonic VCO was enabled and set to its maximum frequency; the figure 4.31 presents the measured spectrum. A measured signal power of 3.69dBm was measured. Note however that since the 1dB output compression point of the sub-harmonic mixer used in the measurements is 3dBm (see figure 4.27), the maximum output power at the f_o -port could not be verified. In order to verify the spectral purity at close-in frequencies, the figure 4.32 shows the measured spectrum for a lower

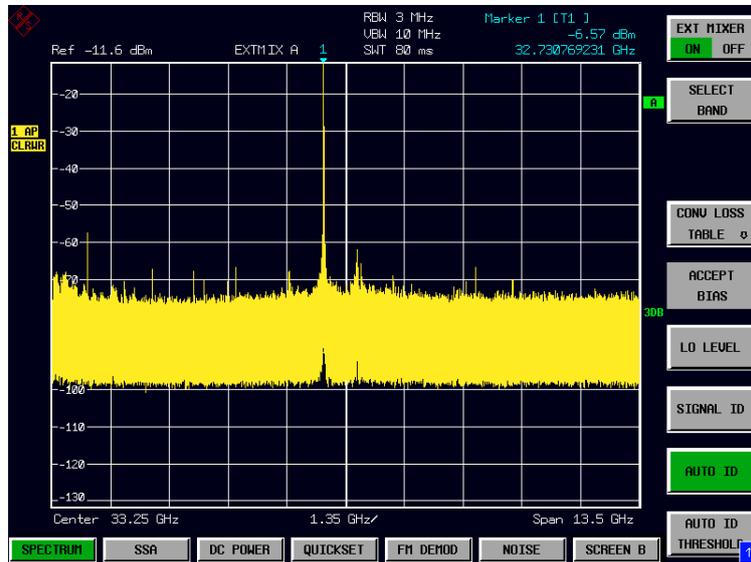


Figure 4.29: Measured spectrum at the f_o -port in the unlocked condition: "sub-harmonic VCO"–off.



Figure 4.30: Measured Phase Noise at the f_o -port in the unlocked condition: "sub-harmonic VCO"–off.

frequency-Span. Remarkably, the most significant spurious signal is ~ 35 dB lower than the desired signal. The measured phase noise of the locked system is presented in the figure 4.33. The measured phase noise at 1MHz offset is -107.72 dBc/Hz. Remarkably,

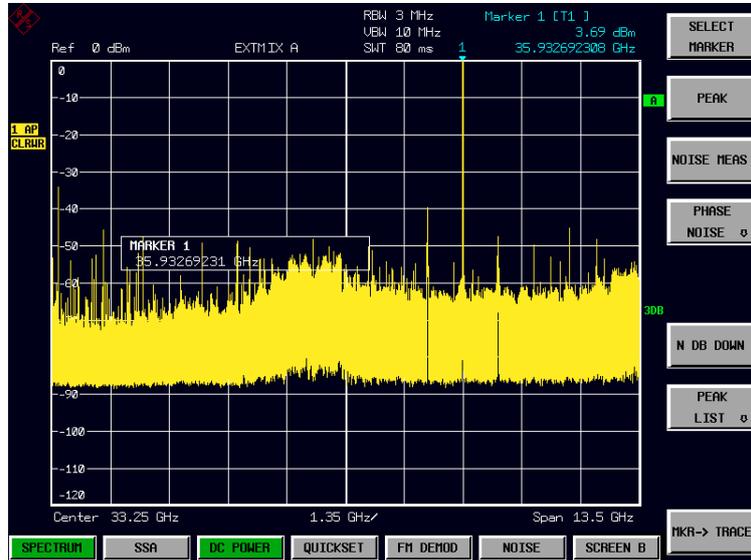


Figure 4.31: Measured spectrum at the f_o -port in the locked condition at 36GHz.

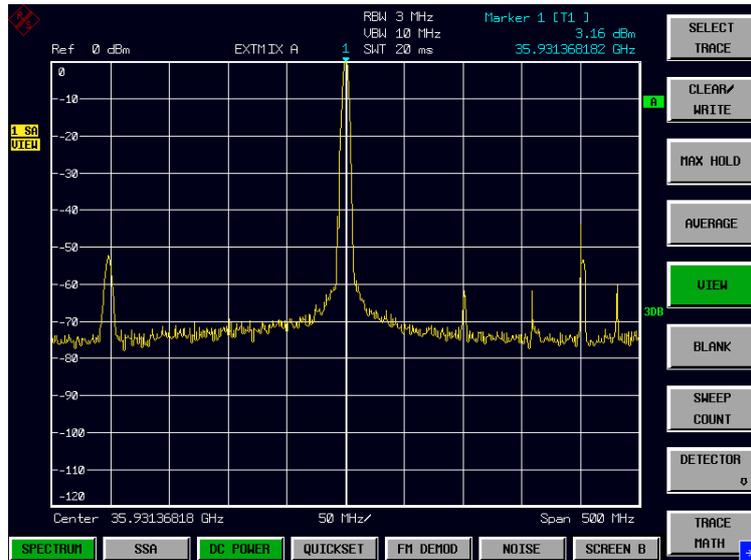


Figure 4.32: Measured spectrum (close-in) at the f_o -port in the locked condition.

compared to the unlocked condition the phase noise of the locked system improved by more than 20dB. The measured frequency range at the f_o -port for the different frequencies of the sub-harmonic VCO are presented in the figure 4.34. The output spectrum at 33.14GHz is presented in the figure 4.35.

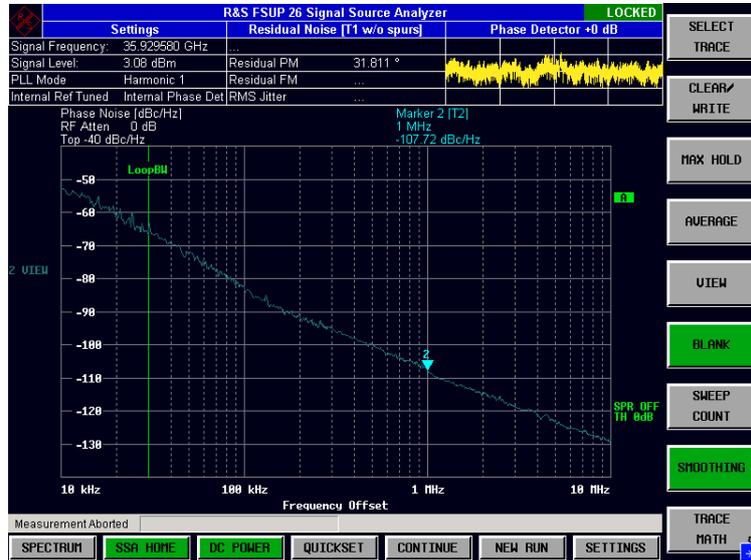


Figure 4.33: Measured phase noise at the f_o output in the locked condition.

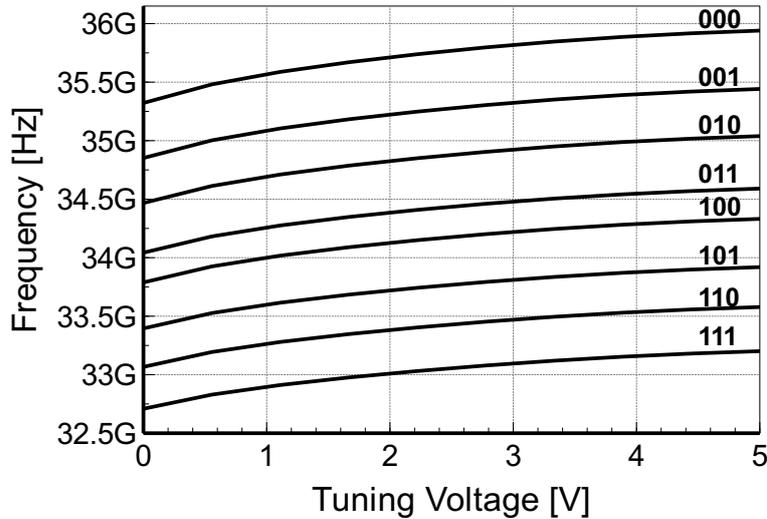


Figure 4.34: Frequency range at the f_o -port.

$f_o/2$ and $2 \times f_o$ ports

The figure 4.36 presents the measured spectrum at the $f_o/2$ -port when LO-Core is set to the maximum frequency. An attenuation of 8dB was measured for the cables from the RF probes to the signal analyzer. Considering this attenuation the signal power at

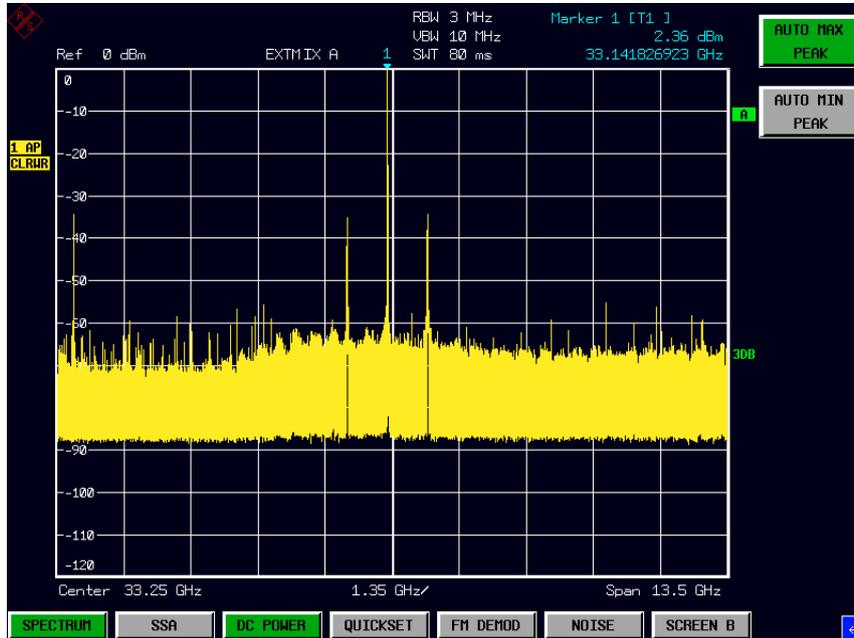


Figure 4.35: Measured spectrum at the f_o -port in the locked condition at 33.14GHz.

18GHz was around 0dBm. The phase noise of this signal is presented in the figure 4.37. At 1MHz offset the phase noise is -113 dBc/Hz. In the figure, the phase noise at 1MHz of the 36GHz signal at f_o -port was hold. The difference between both is very close to the theoretical $20 \times \log_{10}(2)$ factor. Finally, the figure 4.38 shows the phase noise of the 67GHz signal taken at the $2 \times f_o$ port. At 1MHz a phase noise of -100 dBc/Hz was obtained. Considering the wire attenuation, the measured signal power was -20dBm in the frequency band.

The results obtained for the system are summarized in the table III. As observed, the design targets were almost obtained when compared with the table II in chapter 1. In particular the system proposed consumes 10mA more than the target specification. Indeed, the emitter-follower stages used as inter-stage buffers accounted for almost 25% of the whole current consumption. A comparison with other works is presented in the table IV.

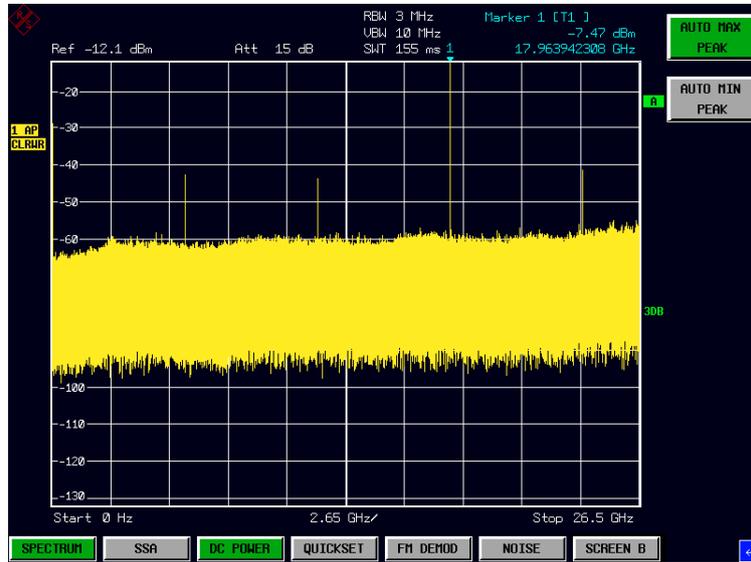


Figure 4.36: Measured spectrum at the $f_o/2$ -port at 18GHz.

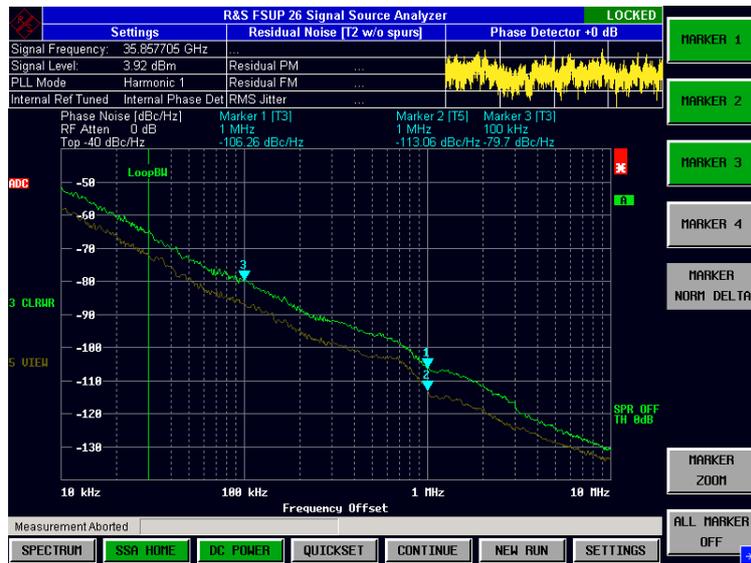


Figure 4.37: Measured Phase Noise at 1MHz of the 18GHz and 36GHz signal at the f_o and $f_o/2$ ports respectively.



Figure 4.38: Measured Phase Noise at 1MHz of the 67GHz signal at the $2 \times f_o$ port.

TABLE III
SUMMARIZED PERFORMANCE OF A MULTIBAND LO SOURCE FOR A LOW-IF P2P APPLICATIONS IN THE 38GHZ BAND.

Parameter	Performance
Technology	QUBIC4Xi (SiGe:C 0.25 μ m)
Frequencies	36, 18, 72 GHz
Tuning range	9%
Tuning Voltage Range	0.5V - 4.5V
SSB Phase Noise @ 1MHz @ 36GHz	-107 dBc/Hz
SSB Phase Noise @ 1MHz @ 18GHz	-113 dBc/Hz
SSB Phase Noise @ 1MHz @ 67GHz	-100 dBc/Hz
RF output power at 36GHz	> 3 dBm
RF output power at 18GHz	0 dBm
RF output power at 67GHz	-20dBm
Supply current	130 mA
VDD	2.5V

TABLE IV
MULTIBAND LO SYSTEM OF THIS WORK COMPARED TO OTHER WORKS

Ref.	Process	Freq [GHz]	TR [%]	Pdiss [mW]	PN@1 MHz [dBc/Hz]
[7]	0.35 μ m Bipolar	80	30	162.5	-97
[8]	0.18 μ m BiCMOS	52.5	26.5	132	-108
[9]	0.13 μ m CMOS	35	26	11	-101
[10]	0.13 μ m BiCMOS	28	30	10.5	-104
[11]	0.13 μ m CMOS	26.9	2	5	-113
[12]	0.25 μ m BiCMOS	17.4	4.6	30	-113
[52]	0.25 μ m BiCMOS	14.24	9.1	123	-118
[13]	0.25 μ m BiCMOS	13.1	5.1	93	-123
This Work2 @ f_o		36	9		-107.72
This Work2 @ $f_o/2$	0.25 μ m	18	9	325	-113.06
This Work2 @ $2 \times f_o$	BiCMOS	67	9		-100

CHAPTER 5

CONCLUSIONS

In this dissertation, concepts and methods for the design of low phase noise signal sources at millimeter wave frequencies have been studied.

The fundamental causes for the degradation of the $1/f^2$ phase noise in LC oscillators as the oscillating frequency scales were identified. Indeed, as the oscillating frequency scales:

1. The quality factor of the LC resonator passes from being dominated by the quality factor of the inductive part to be dominated by the quality factor of its capacitive part.
2. At least for spiral inductors, its minimum reliable size does not downscale easily, thus the capacitive part of LC resonators tends to decrease.

Direct consequences from the later are:

1. LC oscillators with low capacitances results in higher phase noise. Since the resonator is intrinsically more sensitive to phase perturbations.
2. For lower capacitances, the quality factor of the resonator capacitive part is more sensitive (in terms of quality factor) to parasitic capacitances, like the capacitance of the active devices in the oscillator or output buffers for example.

On the other hand, for a given inductor and tuning range, it was shown in chapter 2 that it is possible to associate time constant τ of a lossy capacitor, with the minimum quality factor of the arrangement of a MiM capacitor and a varactor. Thus making possible to estimate the minimum quality factor of the resonator capacitive part as a function of the oscillating frequency. This characteristic was used in chapter 3 to estimate the minimum $1/f^2$ phase noise of a conceptual LC oscillator as a function of the oscillating frequency. With this analysis it was possible to determine analytically under which conditions a fundamental oscillator or a sub-harmonic (super-harmonic) oscillator followed by a frequency multiplier (divider) would be better in terms of the phase noise to generate a

signal at frequency f_o . Furthermore, the design aspects related to the use of a cross-coupled as the gm-cell were studied revealing that the time constant of its capacitive load shows a constant behavior over a wide range of frequencies.

Finally, in chapter 4 the design of a signal source in the Ka-band based on a sub-harmonic VCO and a injection-locked frequency tripler (ILFT) intended for Low-IF P2P applications is presented. In particular, the proposed ILFT exploits the second harmonic of the VCO to enhance the generation efficiency of the injecting signal responsible for the locking of the ILFT. In a first prototype, with a frequency range of 30.72 to 33.6 GHz, the system achieved a measured phase noise at 1 MHz from a 30.8 GHz carrier frequency of -112dBc/Hz for 90mW of power consumption (Vdd=2.5V).

In a second prototype, a multiband generation was designed. The system provides three RF outputs at f_o , $f_o/2$ and $2 \times f_o$ with 9% of tuning range. The measured output power at 36GHz, 18GHz and 67GHz was 2.36dBm, 0dBm and -20dBm respectively. For the same frequencies the phase noise at 1MHz was -107 dBc/Hz, -113dBc/Hz and -100dBc/Hz respectively. The total power consumption was 325mW (Vdd=2.5).

5.1 Perspectives

- In order to use the signal sources here designed in a RF front-end, the sub-harmonic oscillator have to be locked within a PLL. Thus a fully frequency synthesizer solution can be obtained. Consequently, the design of a PLL constitutes a natural evolution of this work.
- To extend the techniques and methods developed in this work for other LC oscillator topologies, as the Colpitts or Clap oscillators. With a higher power consumption, these oscillators have shown higher oscillating frequencies when compared with the cross-coupled LC oscillator [60, 61]. By locking these oscillators with a sub-harmonic oscillator, low phase noise sources at higher frequencies could be

obtained.

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