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Spécialité de doctorat (Génie Electrique)

Par

Mr Chenjiang YU

Technologies de fabrication pour les convertisseurs
de puissance intégrés

(Technologies for integrated power converters)

Thèse présentée et soutenue à GeePs, 11 rue Joliot Curie, Gif sur Yvette, le 13/12/2016 :

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Titre : Technologies de fabrication pour les convertisseurs de puissance intégrés

Mots clés : Convertisseur de puissance, gestion thermique, technologie de packaging

Résumé : Les convertisseurs électroniques de puissance sont aujourd'hui très largement utilisés dans tous les domaines de la conversion d'énergie. Ils sont des outils désormais incontournables de tout processus de gestion des transferts de l'énergie électrique depuis les puissances les plus faibles (quelques mW) jusqu'à plusieurs dizaines voire centaines de MW. Le domaine de l'électronique de puissance subit actuellement une double mutation liée aux possibilités offertes par les technologies d'intégration d'une part et l'arrivée de nouveaux composants à semi-conducteur de puissance de type grand-Gap d'autre part.

Dans cette thèse supportée par l'ANR, nous avons étudié et évalué les potentialités associées à l'intégration de composants de puissance traditionnels (Silicium) et à base de matériaux grands Gap (GaN). Nous avons, pour cela, développé des procédés de fabrication destinés à l'intégration de composants GaN à structure latérale et de composants Silicium à structure verticale. Le contexte applicatif de cette thèse est celui de l'accroissement du niveau d'électrification dans les avions de nouvelle génération.

Pour les composants grand Gap de type GaN à structure latérale (basse tension), nous avons proposé un nouveau procédé de report sur substrat céramique (DBC) et nous avons démontré que cette solution permettait d'améliorer considérablement la gestion thermique de ces composants.

Sur la base de ces structures, nous avons également présenté et évalué des méthodes de modélisation permettant la conception de ces dispositifs. Cette modélisation, utilisant des méthodes numériques de type éléments finis ou des méthodes analytiques, traite de deux aspects de la conception : la prédétermination du comportement thermique et la prédétermination du comportement électrique et CEM (en ce qui concerne les aspects conduits). Pour les composants à structures verticales (haute tension), nous avons démontré la faisabilité technologique d'une solution alternative aux packagings traditionnels (assemblage sur DBC et connexion par fils de Bonding). Le process proposé permet, par enterrement des puces dans le PCB, de réaliser une interconnexion 3D permettant de réduire les inductances parasites de boucle très largement dues aux inductances parasites des fils de Bonding. Ceci a pu être démontré sur un prototype de convertisseur complet. Ce procédé d'enterrement des puces s'avère donc particulièrement adapté dans le cas de composants à commutation très rapide.

Title : Technologies for integrated power converters

Keywords : Power converter, thermal management, packaging technology

Abstract: Power Electronic converters are now widely used in all areas of energy conversion. They are tools that cannot be ignored in any process of managing electrical energy transfers from the lowest powers levels (a few mW) to several tens or even hundreds of MW. Power electronics technologies are currently undergoing a double mutation linked to the possibilities offered by integration technologies on the one hand and the arrival of new Wide-Band-Gap power semiconductor components on the other hand.

In this thesis supported by the French ANR, we studied and evaluated the potentialities associated with the integration of traditional power components (Silicon) as well as those based on Wide-Band-Gap materials (GaN). We have developed new technological processes for the integration of GaN components with a lateral structure and silicon components with a vertical structure. The application context of this thesis is linked to the problematic of increasing the level of electrification in new generation of aircrafts.

For Wide-Band Gap GaN type power devices with a lateral structure (low voltage), we proposed a new method of device-attachment to a metalized ceramic substrate (DBC) and we demonstrated that this solution made it possible to considerably improve the thermal management of these components.

On the basis of these structures, we also presented and evaluated modeling methods allowing the design of the whole packaging. This modeling, using numerical tools based on finite element method or analytical equations, deals with two aspects of the design: the predetermination of the thermal behavior and the predetermination of the electrical and electromagnetic behavior (with regard to the conducted aspects).

For components with vertical structures (high voltage), we have demonstrated the technological feasibility of an alternative solution to traditional packaging (assembly on a DBC substrate and electrical connection by wire bonding process). The proposed process allows, by embedding the power dies in the PCB, to carry out a 3D interconnection making it possible to reduce the parasitic loop inductances mainly linked to the parasitic inductances of the bondwires. This has been demonstrated on a converter prototype. Embedding power devices is thus particularly suitable in the case of components with very fast switching capabilities.

Remerciements

Sur cette page dédiée aux remerciements je souhaite m'adresser à toutes les personnes qui m'ont aidé à grandir dans l'univers des sciences et des technologies durant ces trois années de thèse.

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Résumé en français

Contexte de l'étude

Au cours des dernières années, l'électricité est devenue de plus en plus importante dans le domaine aéronautique. En fait, le concept de l'avion «plus électrique» induit une forte amélioration potentielle par rapport aux systèmes hydrauliques et pneumatiques classiques, principalement par la simplification de la maintenance, l'amélioration de l'efficacité et de la réduction de l'effort de développement et du coût d'exploitation [1].

Au-delà des applications ciblées qui en ont bénéficié, comme par exemple les avions suivants : A380, B787, A400M et A350 (contrôle de vol électrique, distribution alternatif à fréquence variable, etc.), les programmes correspondants ont permis d'identifier les évolutions architecturales pour améliorer les performances des avions civils futurs. Cela concerne en particulier l'utilisation d'une distribution électrique à courant continu haute tension appelée "HVDC".

Ce mode de distribution, rendue possible par l'évolution de l'électronique de puissance, a offert des perspectives multiples, comme un gain de poids de la distribution (câbles et protections), l'interopérabilité du réseau HVDC avec plusieurs sources, en particulier avec le réseau basse tension LVDC 28V. C'est cette liaison HVDC-LVDC qui est au cœur du projet ETHAER présenté dans ce mémoire. Cependant, l'introduction massive de l'électronique de puissance dans un contexte très restrictif, qui impose des contraintes importantes en matière de compétitivité, de performance et de fiabilité des équipements, s'accompagne de nombreuses difficultés.

La résolution de cette équation compliquée impose, d'une part, la définition d'une approche multi-domaine basée sur une approche de conception 3D incluant les problématiques technologiques et normatives (thermique, CEM) mais également fonctionnelle (contraintes associées à l'intégration au système), d'autre part, l'utilisation de nouvelles solutions (topologies de conversion, lois de contrôle spécifiques associées) et de technologies émergentes (intégration hybride, composants grand Gap SiC, GaN, ...).

La perspective globale offerte par cette démarche est principalement la diminution du coût de développement, de production et d'exploitation ainsi que l'optimisation de la maintenance et l'amélioration de la sécurité.

Description du projet et travaux réalisés

Le projet "ANR ETHAER" est à la frontière entre la recherche fondamentale et industrielle. Le domaine étudié est celui de l'électronique de puissance dans le contexte de l'avion plus électrique, domaine ayant concentré beaucoup d'activités de recherche ces 5 dernières années. Il vise à contribuer à la définition de convertisseurs électroniques de puissance pour les avions de la prochaine génération (2015-2025). Pour atteindre cet objectif, ETHAER se concentre sur une fonction électrique spécifique très limitée :

l'interconnexion entre les réseaux électriques de bord, à savoir le réseau 28V et le réseau haute tension +/- 270V DC.

Ce projet comporte une forte composante expérimentale et technologique, ce qui s'est traduit par la réalisation de nombreux démonstrateurs. Dans ce projet, le choix a été fait de proposer et d'évaluer de nouvelles architectures de convertisseurs basés sur des topologies dites multicellulaires.

La réalisation pratique d'un convertisseur multicellulaire est basée sur un certain nombre de défis technologiques. La recherche de la fiabilité et l'augmentation de la densité de puissance impose de proposer et développer de nouvelles technologies d'intégration et de packaging. Les niveaux de puissance visés nous conduisent tout naturellement à envisager des technologies d'intégration hybride plutôt que monolithique, ces dernières n'étant envisageables que pour de très faibles puissances. Comme l'association série / parallèle de composants ou de convertisseurs élémentaires dans les nouvelles topologies que nous proposons implique une augmentation considérable du nombre d'interconnexions, nous nous sommes tournés vers des solutions compatibles avec des méthodes de fabrication appelés «collectives», par opposition aux méthodes classiques «individuelles» utilisées pour l'assemblage de convertisseurs. Le coût et le temps de réalisation de ces procédés classiques (par ex. le Wire Bonding) sont proportionnels au nombre d'interconnexions étant donné qu'ils sont réalisés de manière séquentielle. Pour les méthodes dites "collectives", la durée de réalisation change peu, et le coût est plutôt lié à la surface / volume du système.

Parmi les technologies matures utilisées dans le domaine de l'électronique de puissance, le PCB (Printed Circuit Board) répond aux contraintes techniques pour les petite et moyenne puissances (quelques centaines de Watts jusqu'à quelques kW), le DBC (Bonded Copper Direct) est pour sa part utilisé aux puissances élevées. Dans le projet ETHAER, une intégration originale en deux étapes est proposée. La première est basée sur la technologie DBC et la seconde est la composition des deux technologies PCB, DBC.

La partie la plus importante du développement réalisé sur la technologie DBC est liée à l'interconnexion des puces sur le substrat (DBC). L'objectif ici est d'éviter l'utilisation des fils de liaison (fils de Bonding) puisque ces liaisons sont une cause importante de défaillance dans les modules de puissance. Dans le cas des composants verticaux, nous sommes à la recherche d'une solution alternative à cette liaison par fils de bonding. Dans la solution proposée, l'interconnexion peut être établie par l'intermédiaire d'un substrat flexible ou bien par métallisation selon un procédé d'électrodéposition.

Le mémoire de thèse est divisé en trois parties, hors conclusion et perspectives, présentant successivement :

- un état de l'art des techniques de packagings actuels utilisés en électronique de puissance. Ce chapitre permet de mettre en évidence les limites d'utilisation associées à chacune de ces technologies et de présenter certains procédés utilisés dans les process de fabrication des assemblages de puissance
- de nouveaux packaging basse tension et les procédés de fabrication associés. Ceux-ci sont basés sur des composants à semi-conducteur GaN à structure latérale. Dans cette partie, sont également présentées et évaluées, les méthodes de modélisation utilisées en vue de la conception de ces dispositifs. Cette modélisation, utilisant des méthodes numériques de type éléments finis ou des méthodes analytiques, traite de

deux aspects de la conception : la prédétermination du comportement thermique et la prédétermination du comportement électrique et CEM (en ce qui concerne les aspects conduits)

- un niveau type de packaging destiné aux composants à semi-conducteur à structure verticale et donc utilisable dans des applications de conversion en haute tension. Sont présentés dans cette partie : - le procédé de fabrication original proposé ; - l'évaluation des performances de ce packaging en terme de performances électriques ; - la réalisation d'un convertisseur dc – dc complet à partir de ce procédé et l'analyse de son fonctionnement

Les principaux résultats

Packaging basse tension pour composant latéraux de type GaN

Trois prototypes basse tension ont été réalisés (voit fig. 1). Ces prototypes ont permis de mettre au point les procédés de fabrication. Ils sont réalisés autour d'un seul composant actif de type GaN à structure latérale et permettent de réaliser une comparaison des performances thermiques de chaque assemblage.

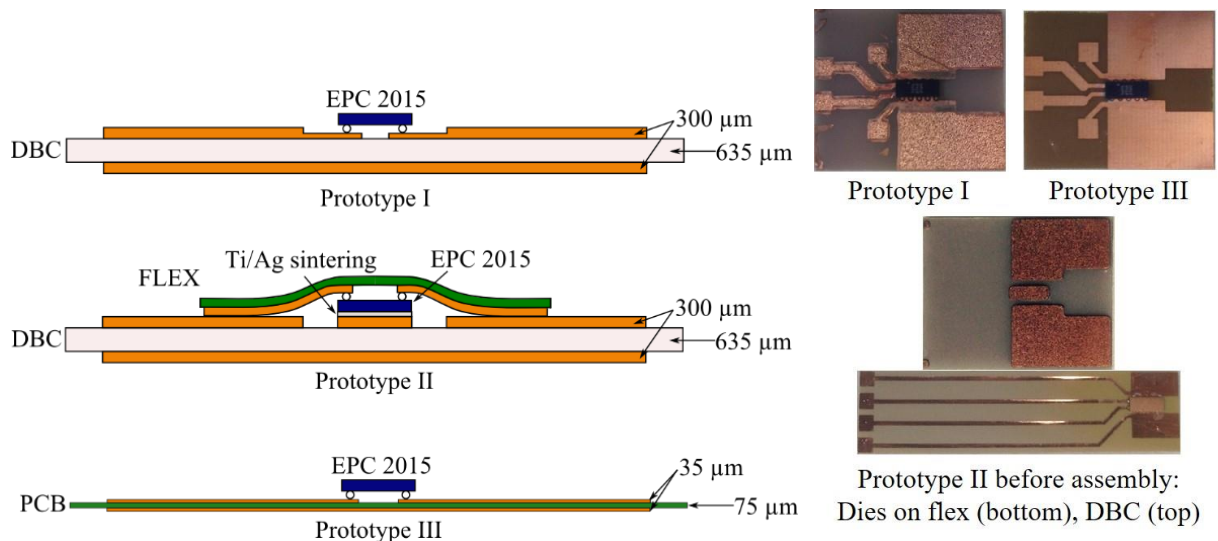


Figure 1 : Vue en coupe et photographie des 3 prototypes

Ces prototypes ont permis :

- De développer une technique de double gravure permettant la mise en œuvre sur DBC (substrats céramiques) de composants possédant des distances entre électrodes théoriquement incompatibles avec ce type de technologie

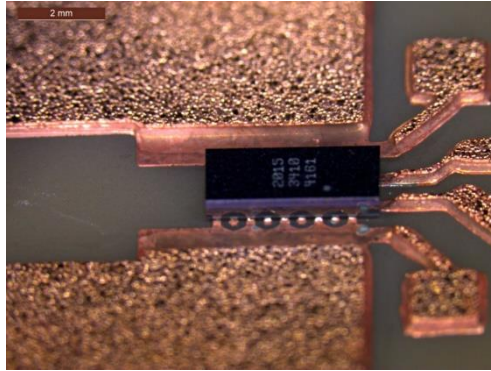
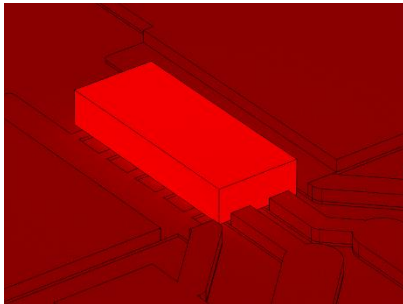


Figure 2 : Substrat céramique gravé par la technique de double gravure et exemple d'utilisation avec un composant GaN EPC

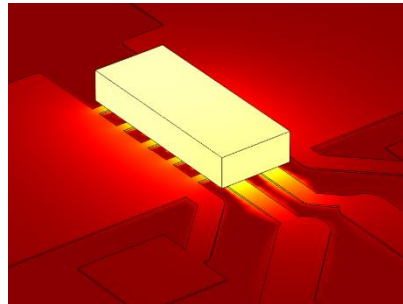
- De démontrer l'intérêt de ce report sur substrat céramique en matière de performances thermiques. Il est ainsi démontré l'intérêt du packaging proposé vis-à-vis de l'état de l'art actuel basé sur des technologies PCB

Report Flip-chip sur Al_2O_3



Tmax: 72.345 °C

Flip-chip on PCB



Tmax: 208.86 °C

Figure 3 : Comportement thermique de l'assemblage sur substrat céramique mis en forme par la technique de double gravure et comparaison avec la technologie traditionnelle sur PCB

- De mettre en place les outils de modélisation thermique et électrique et de réaliser des comparaisons expérimentales permettant une validation des outils

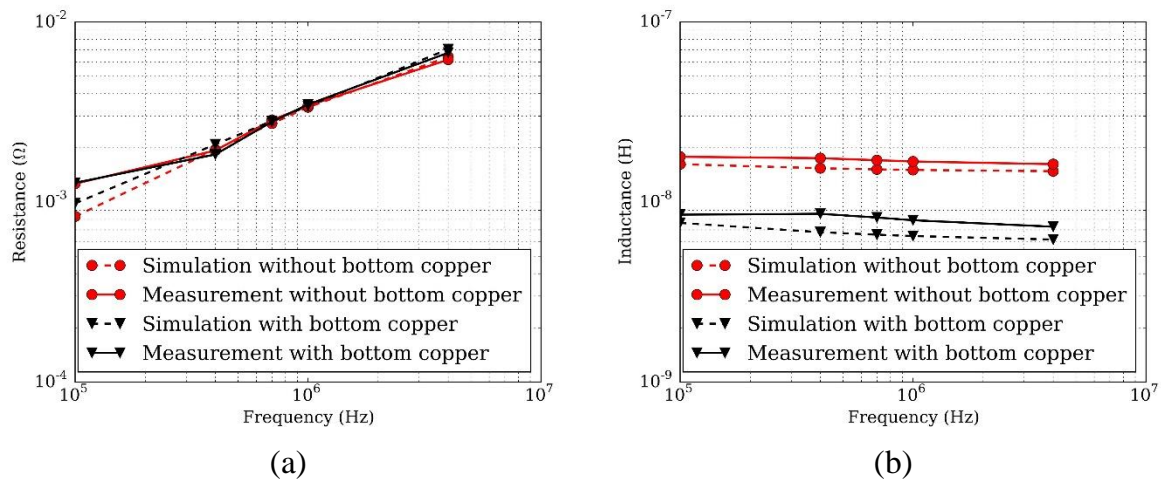


Figure 4 : Comparaison entre simulation et mesure de la valeur de la résistance et de l'inductance de boucle d'une cellule de commutation

Sur ce principe une cellule de commutation complète a pu être réalisée. Cette cellule comprend deux transistors GaN, le Driver permettant de piloter les deux composants en mode demi-pont et les capacités de découplage.

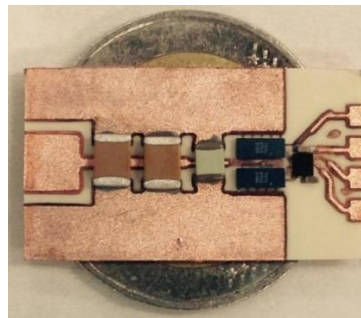


Figure 5 : Convertisseur élémentaire de type demi-pont construit sur substrat DBC en utilisant la technique de double gravure

Ce convertisseur élémentaire a permis d'analyser les performances électriques et électromagnétiques des packagings céramiques proposés. Il a ainsi été démontré que l'accroissement de la valeur de l'inductance de câblage associé aux contraintes technologiques du packaging céramique, accroissement occasionnant une augmentation des pertes par commutation, a un effet moins important qu'attendu. Ceci est analysé comme étant lié à l'effet d'écrantage apporté par la métallisation inférieure du substrat DBC et que l'accroissement des pertes de commutation est largement compensé par l'amélioration importante des performances thermiques du module utilisant la technologie proposée.

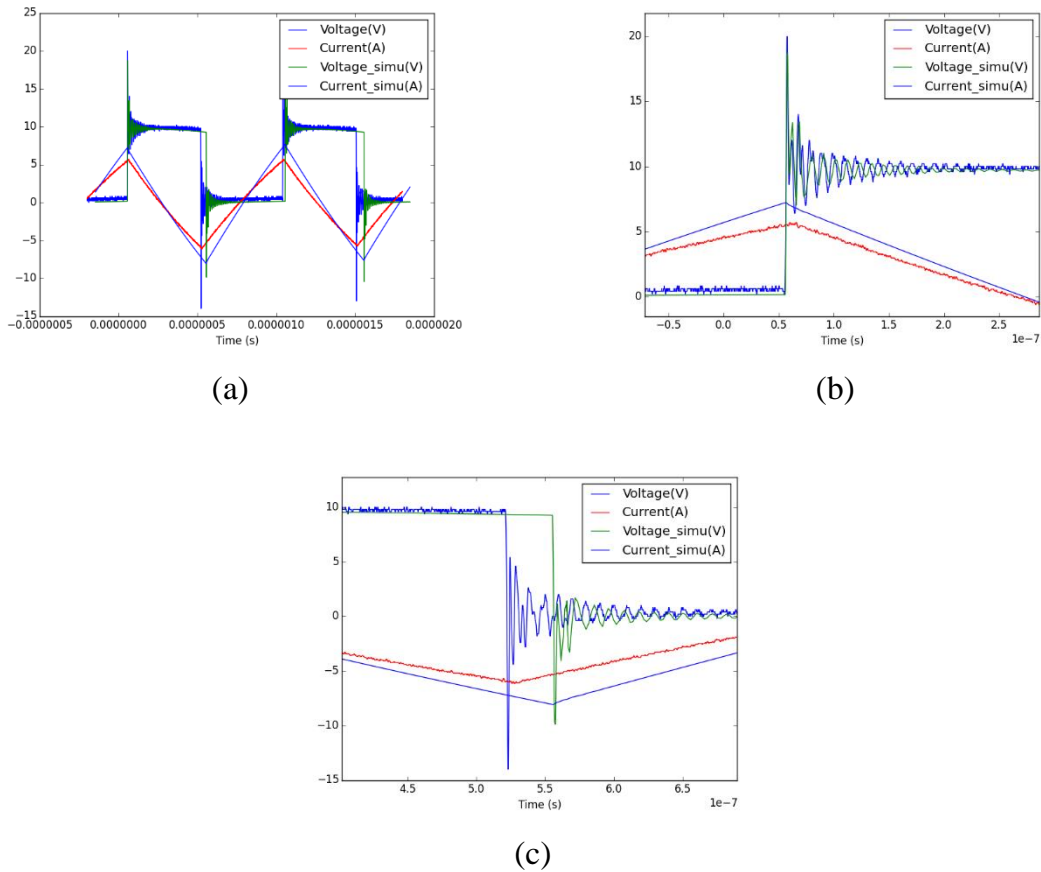
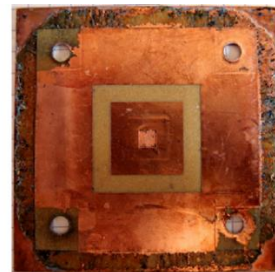
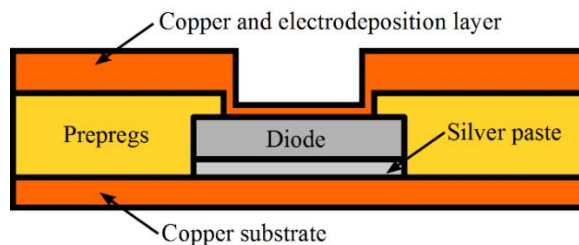


Figure 6 : Comparaison des signaux électriques simulés et mesurés sur le dispositif expérimental

Packaging haute tension adapté aux composants de puissance à structure verticale

Deux prototypes ont été réalisés (voit fig. 7). Ces prototypes ont permis de mettre au point les procédés de fabrication. Ils sont réalisés autour d'un seul composant actif (une diode 600V) à structure verticale et permettent de tester les différentes options du process de fabrication et d'évaluer l'évolution des performances électriques en fonction du mode de prise de contact électrique sur la partie supérieure du composant.



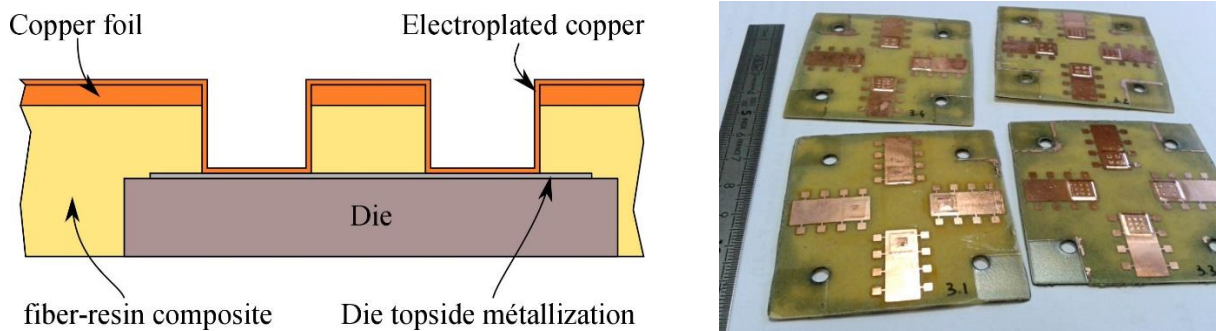


Figure 7 : Vue en coupe et photographie des 2 prototypes

Ces prototypes ont permis :

- De développer le procédé d'enterrement de puce de puissance

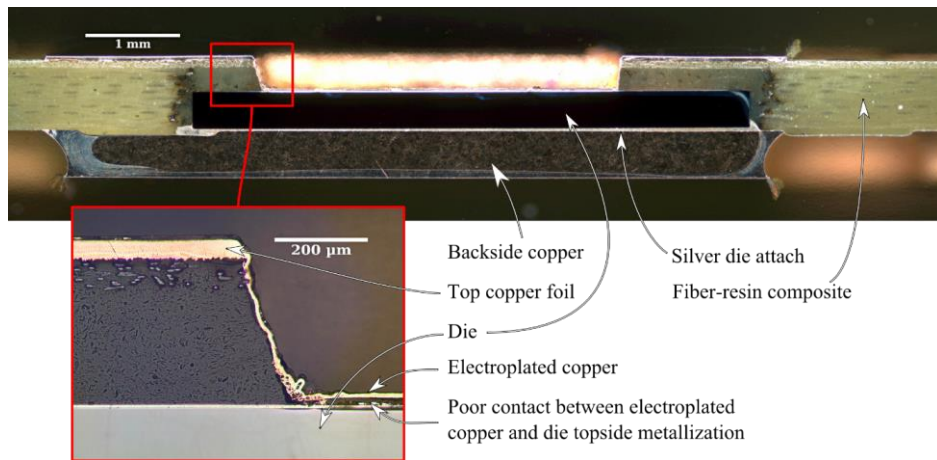


Figure 8 : Vue en coupe d'un prototype : diode à structure verticale enterrée dans le PCB avec prise de contact sur la partie supérieure du composant

- D'évaluer l'évolution des performances électriques du composant après enterrement dans le PCB

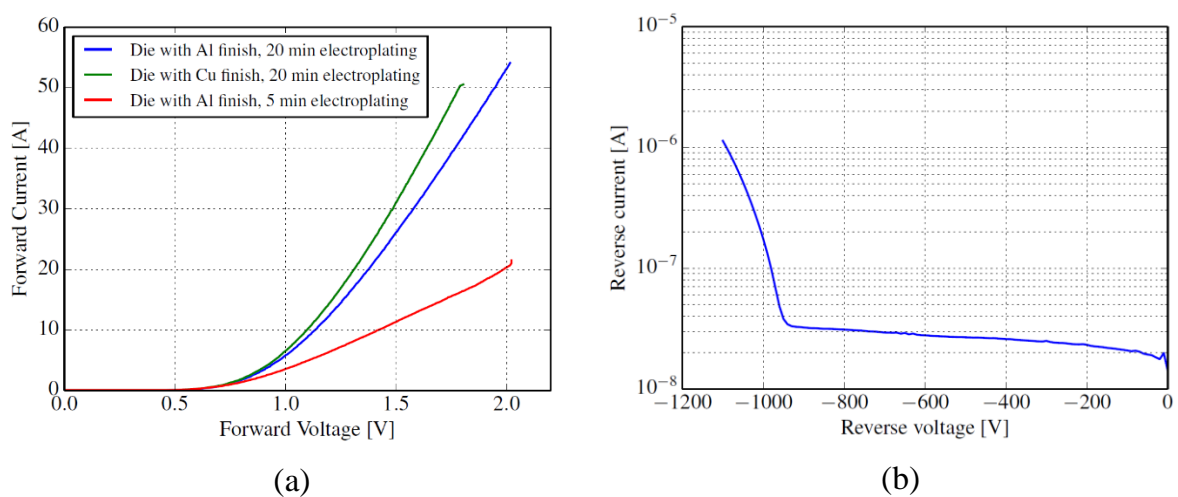


Figure 9 : Comportement électrique de la diode à l'état passant (a) et à l'état bloqué (b)

- D'évaluer et analyser plusieurs modes de prise de contact électrique en partie haute

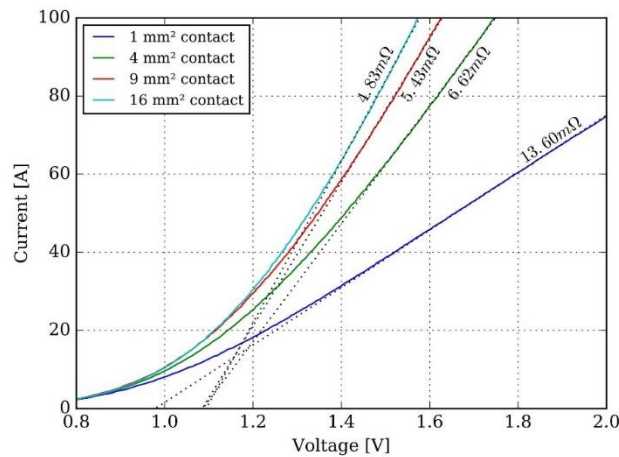


Figure 10 : Caractéristiques à l'état passant d'une diode enterrée en fonction du mode de prise de contact

Sur ce principe une cellule de commutation complète a pu être réalisée. Cette cellule comprend deux transistors IGBT et deux diodes.

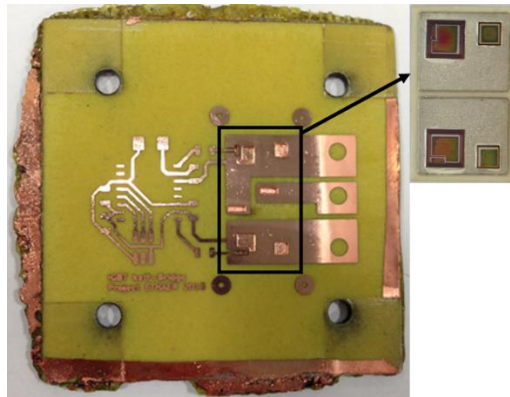


Figure 11 : Convertisseur élémentaire de type demi-pont construit par procédé d'enterrement de puces à structures verticales (IGBTs + diodes)

Le travail réalisé dans cette partie a permis de démontrer la faisabilité technologique d'une solution alternative aux packagings traditionnels des composants verticaux (assemblage sur DBC et connexion par fils de Bonding). Le process proposé permet, par enterrement des puces dans le PCB, de réaliser une interconnexion 3D permettant de réduire les inductances parasites de boucle très largement dues aux inductances parasites des fils de Bonding. Ceci a pu être démontré par simulation sur le prototype de convertisseur complet de la fig. 11. Ce procédé d'enterrement des puces s'avère donc particulièrement adapté dans le cas de composants à commutation très rapide.

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General Introduction

In the recent years, the electricity has become more and more important in the aeronautic domain. In fact, the “more electric” aircraft concept induces a strong potential improvement compared to the conventional hydraulic and pneumatic systems, mainly by the simplification of the maintenance, the improvement of the efficiency and the reduction of the development effort [1].

Beyond the targeted applications which have benefited such as A380, B787, A400M and A350 (control of electric flight, alternative current distribution with variable frequency, etc.), the corresponding programs have allowed to identify the architectural evolutions to improve the performances of future civil airplanes. This concerns especially the utilization of an electric distribution of high voltage direct current called “HVDC”.

This mode of distribution, made possible by the evolution of the power electronics, offered different perspectives such as a weight saving of the distribution (cables and protections), or the interoperability of the HVDC network with several sources, in particular with the low voltage network LVDC 28V. It is this HVDC-LVDC liaison which will be the core of the ETHAER project presented here. However, the massive introduction of power electronics in a very restrictive context, which requires competitive, efficient, and reliable equipment, is a complex problem.

The resolution of this complicated equation impose, on one hand, the definition of a multi-domain approach based on the 3D environmental (thermal, CEM) and functional conception, and on the other hand, the utilization of new solutions (topologies, control laws) and of emergent technologies (hybrid integration, Wide Bandgap components SiC, GaN ...).

The global perspective offered by this approach is mainly the decrease of the cost of development, production and exploitation.

The “ANR ETHAER” project is at the boundary between fundamental and industrial research. It addresses the field of Power Electronics, in the context of the more electric aircraft, which has been concentrating a lot of research for the past 10 years. It aims to contribute to the definition of electronic power converters for next-generation aircrafts (2025). To achieve this objective, ETHAER focuses on a very constrained, specific electrical function: the interconnection between onboard electrical networks, namely 28V and +/-270V DC bus. This involves a significant experimental and technological part that will lead to the realization of demonstrators. The choice was done to propose and evaluate multicellular converters topologies.

The practical realization of a multicellular converter is based on a number of technological challenges. The research of increased reliability and power density requires improvements of the integration and packaging technology. The considered power leads us naturally to think about the hybrid technology rather than the monolithic integration technology which is possible only for very small power levels. Also, the converter topologies developed during this project rely on the series/parallel association of components or elementary converters. This results in an increase of the interconnection count. Therefore, we are interested in the manufacturing methods called “collectives”, by opposition to the classical “individual” methods used for the assembly of converters. The realization cost and time of these classical methods (ex. Wire bonding) is proportional to

the interconnection number since they are realized sequentially. When a collective process is used, the duration of whole realization changes little with the number of interconnections, and the cost is mostly related to the surface/volume of the system.

Among the mature technologies used in the power electronics domain, the PCB (Printed Circuit Board) technology addresses small and medium power (a few hundreds of Watts up to a few kW), and DBC (Direct Bonded Copper) based technology is dedicated to medium and high power.

In this thesis, we propose two alternatives to classical packaging technologies. The first one is dedicated to low voltages power converters using low profile GaN FET semiconductors. The main goal is here the thermal improvement of commonly used technologies using PCB substrate. In our proposal, a mixed technology based on both DBC and PCB substrates will be presented and assessed. The second one investigate a packaging solution for high-voltage vertical structure power-semiconductors. For such devices, DBC technology is commonly used. The most important issue in DBC technology is linked to interconnection of the dies on the DBC substrate. In the second part of this thesis, our objective is to avoid the use of bonding wires since these bondings represent an important cause of failure and degrade electrical and electromagnetic performances of power modules. We propose an alternative technological solution to the widely used wire bonding in which the dies are buried within a PCB substrate and interconnections are established by electroplating.

This thesis report is divided in four parts:

- The first chapter firstly presents the technological and general context of this work. Then, a state-of-the-art of power packaging in 2D power module as well as different 3D solutions will be presented and a critical analysis underlining their utilization limits, will be conducted. At the end of this chapter, typical fabrication processes will be introduced;
- The second chapter deals with low voltage packaging designed for lateral GaN FETs. Different solutions are proposed and the corresponding fabrication processes will be presented. In this chapter, we also present electromagnetic and thermal analyses of the proposed structures. These analyses are based on Pspice and COMSOL Multiphysics models, and experimental characterizations;
- The third chapter presents a high voltage packaging dedicated to vertical devices based on embedding PCB technology. The common fabrication process is firstly presented followed by a comparison and performance analysis of different electrical contact strategies at the top of a power die. At last, a half-bridge prototype fabricated with the proposed technology is presented;
- The last part is dedicated to the general conclusion and gives some perspectives.

CHAPTER 1. State-of-The-Art

1.1 Introduction

After a recall on power converters constitutive and main issues, this first chapter presents the state of the art on packaging. The role and different constitutive elements of a 2D module with the principal failure mechanism will be firstly introduced. Then some new interconnection solutions will be presented. At last, typical fabrication processes will be introduced.

1.2 Power Converters

Power converters are used for electric energy processing. They allow to convert this energy from different given forms (DC, AC, low or high voltage, etc.) to another. A power converter integrates a combination of power electronic components and a driver circuit for the actively switchable power semiconductors.

1.2.1 Active Components

In the power electronics domain, the active components are usually power semiconductors and are the elementary part of power converters. From a packaging point of view, a power semiconductor contains three main parts:

- The semi-conductor material with a thickness between a few tens and a few hundreds of micrometers.
- The metallic electrodes on the upper face and lower face.
- The passivation layer on the upper face. It usually contains an organic layer with limited temperature capability

The Silicon (Si) material based semiconductors have the largest market share because silicon is a mature and very well established technology. However, these components have some noticeable limitations such as lower blocking voltage, switching frequencies, efficiency and reliability. At present, the Si-based device cannot operate above 200 °C or with very high voltage (Si IGBT limited to 6.5kV). Switching losses and conduction losses of Si technologies reduce dramatically the efficiency of power converters, which requires additional cooling system and passive components [2].

As the Si technology has approached its theoretical limits, power devices made out of Wide bandgap (WBG) material such as Gallium nitride (GaN) and Silicon carbide (SiC) have emerged as alternatives for power applications. These materials have superior electrical characteristic compared with Si, such as lower switching loss, higher maximum operation junction temperature and thermal conductivity. These advantages allow the power converters to operate at higher frequencies and higher ambient temperature. Some of the principal characteristics for these wide band gap materials as well as for Si are shown in Table 1.1 and in Figure 1.1.

Property	Si	6H-SiC	4H-SiC	GaN
Bandgap, E_g (eV)	1.12	3.03	3.26	3.45
Dielectric constant, ϵ_r	11.9	9.66	10.1	9
Electric Breakdown Field, E_c (kV/cm)	300	2500	2200	2000
Electron Mobility, μ_n (cm ² /V.s)	1500	500	1000	1250
Thermal Conductivity, λ (W/cm.K)	1.5	4.9	4.9	1.3
Saturated Electron Drift Velocity, v_{sat} ($\times 10^7$ cm/s)	1	2	2	2.2

Table 1.1: Physical characteristic of Si and main wide bandgap semiconductors [3]

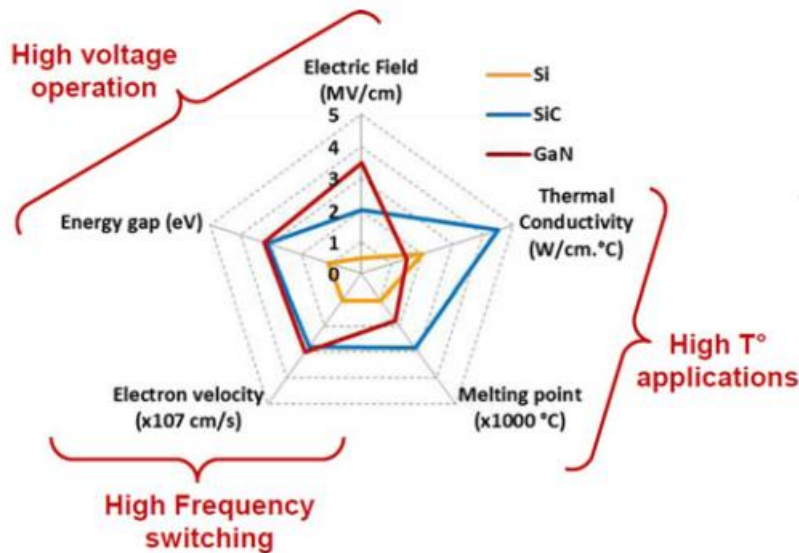


Figure 1.1: Summary of Si, SiC and GaN relevant material properties [4]

However, the fabrication cost of wide bandgap semiconductor is relatively high, and the technology is not yet mature, so the Si-based components still have a large market.

1.2.1.1 GaN power devices

“The electronics revolution of the 20th century was driven by the invention of the transistor and integrated circuit employing silicon semiconductor technology. Hence, silicon can be considered the first generation semiconductor. The wireless and information revolution ignited at the turn of the 20th to 21st century was made possible by the utilization of the semiconductor laser and microwave transistor based on the second generation semiconductors, gallium arsenide, and indium phosphide. At the start of the 21st century, the wide bandgap semiconductors, SiC and GaN are emerging as the third generation of semiconductors [5].” GaN-based is one of the third generation wide-bandgap materials, and is developing rapidly. Its better physical and chemical properties have made up the weak points of last two generation semiconductor materials (Si, GaAs). Most developing GaN devices have lateral structure because they are based on the high electron mobility transistor (HEMT) structure, which uses an AlGaN/GaN heterojunction structure [6, 7]. In this

structure, the polarization field at the AlGa_N/Ga_N heterointerface generates a high-concentration 2-D electron gas (2DEG) with high carrier mobility, and thus significantly reduces the on-state resistance [8, 9]. The Ga_N devices can be switched faster with lower switching losses [10, 11]. It is very important because a higher frequency converter means a smaller size of passive components, which can largely affect the power density of a module.

There are two types of Ga_N transistors available on the market: the depletion mode Ga_N component, and the enhancement mode Ga_N FETs. Both of depletion mode and enhancement mode Ga_N transistors are lateral devices. Figure 1.2 and Figure 1.3 show the similar structure of these two structures.

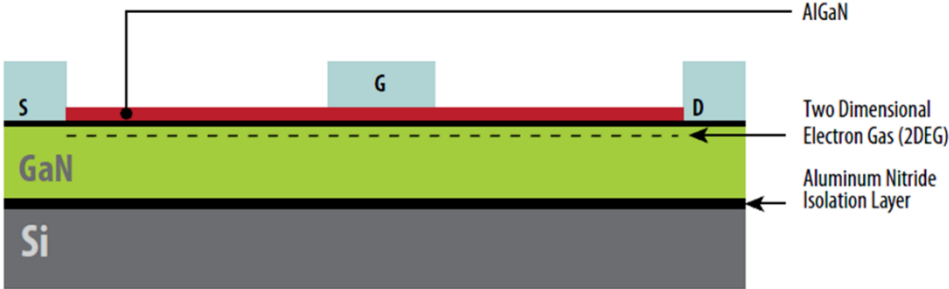


Figure 1.2: Depletion mode Ga_N transistor [12]

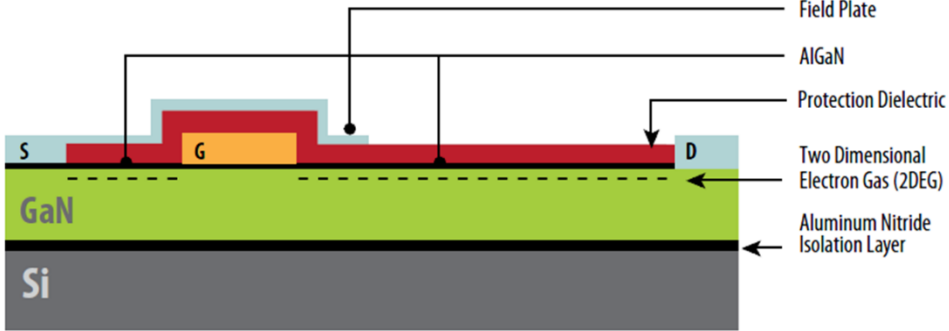


Figure 1.3: Enhancement mode Ga_N transistor [12]

In depletion mode, a transistor’s electrode is placed on top of the AlGa_N layer in order to deplete the 2DEG. This gate is formed as a Schottky contact to the top surface. The Schottky barrier becomes reverse-biased and the electrons underneath are depleted when applying a negative voltage to this contact. To turn this device off, a negative voltage is required.

For enhancement mode transistors, the gate electrode forms a depletion region under the gate. A positive voltage is applied to the gate to turn the FET on, as for turning on an n-channel, enhancement mode power MOSFET.

The most important difference between these two modes is that the depletion Ga_N is normally in conducting state, it needs a negative voltage to turn off; whereas the enhancement Ga_N is normally in off state and it requires a positive voltage to turn on. As a consequence, in power conversion applications, the disadvantage of depletion mode devices is that a negative bias must first be applied to the device at startup of the power converter, otherwise a short circuit will occur. On the other hand, enhancement mode does not have this problem, with zero bias on the gate, transistor is off at startup and will not conduct current.

1.2.1.2 SiC power devices

Compared to the GaN, SiC material has much better thermal conductivity. This technology is also more mature. It has undergone a great development since 1987 with the foundation of CREE Inc., which is the major supplier of SiC wafers. Another difference between the GaN and SiC devices is that GaN transistors have a lateral structure, whereas the structure of SiC devices is usually vertical, as it is common with Si power components.

SiC exists in a variety of polymorphic crystalline structures called polytypes e.g, 3C-SiC, 6H-SiC, and 4H-SiC. Presently 4H-SiC is generally preferred in power device fabrication. Due to its higher performance, SiC material is proved to be a promising replacement of Si in the various applications:

- High voltage Schottky diodes (600, 1200V and above) [13];
- High voltage MOSFET and IGBT (600, 1200V and above) [14];
- The operation with higher frequency and higher temperature than Si [15, 16];

A Schottky barrier diode (SBD) is formed by a metal-semiconductor junction shown in Figure 1.4. This structure was used by the earliest SiC Schottky diodes. However, the Schottky diodes show a positive temperature factor. Therefore, as the temperature increases, so do the losses (because of the decrease of the carrier mobility). The phenomenon is the cause of thermal-runaway, which can lead the destruction of the device [17].

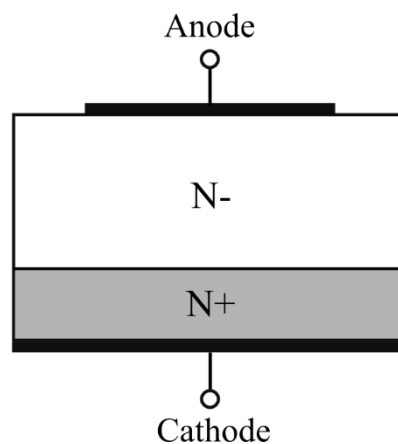


Figure 1.4: Structure of a Schottky diode [18]

An alternative device concept, called the Merged Pin Schottky (MPS) (illustrated in Figure 1.5) has been developed over the past decades [19]. It is based on the Schottky barrier diode, and a bipolar junction is added. This junction is not activated during the normal function due to its higher threshold voltage (in the range of 3V, while it is 1V for the SBD). It brings a better stability during overload transients.

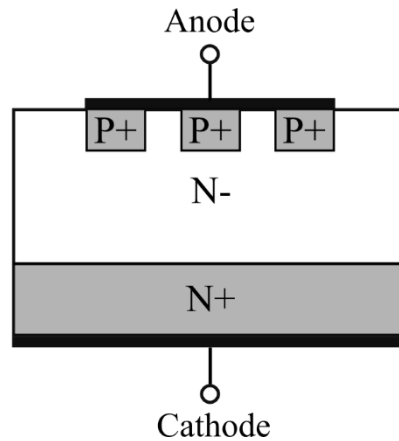


Figure 1.5: Structure of a Merged PiN Schottky (MPS) diode [18]

The SiC MOSFET reduces switches losses compared with silicon MOSFETs and IGBTs. One reason is that the high voltage SiC MOSFET does not have the tail current losses found with IGBTs [20]. In addition, the SiC MOSFET supports a high current density so it has smaller die size which results in lower capacitance than with silicon MOSFETs.

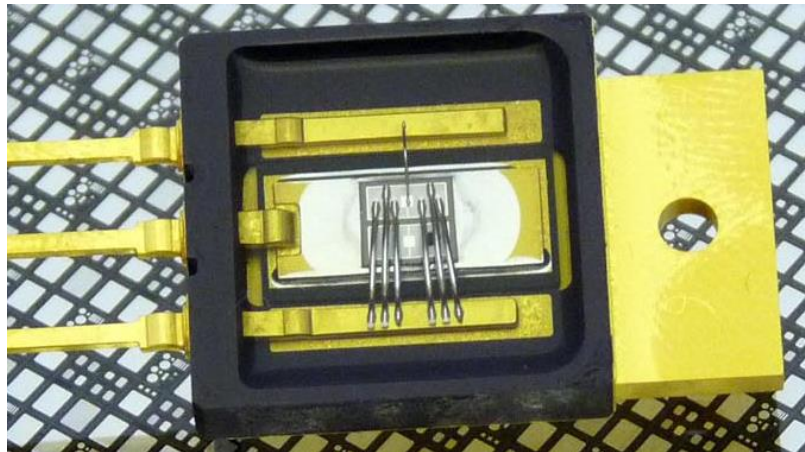


Figure 1.6: An example of SiC power MOSFET [21]

The SiC MOSFET offers advantages over conventional silicon devices, enabling high system efficiency and /or reduction in system size, weight and cost through its higher frequency operation [22]. Compared to the best silicon IGBTs, the SiC devices will improve system efficiency up to 2% and operate at 2-5 times the switching frequencies. Higher component efficiency also results in lower operating temperature [23].

1.2.2 Switching cell

The power electronic is a switching electronic: ideally, an opened or closed interrupter cannot dissipate any energy. Therefore, it is possible to transfer the energy between an input source and an output load, and to control this energy transfer. In each switching cycle, a quantity of energy is transferred or stored between the input and output. A switching cell (Figure 1.7) connects or disconnects these two sources using semiconductors power switches. In a switching cell, the semiconductors can be either controlled switches or a controlled switch and a diode.

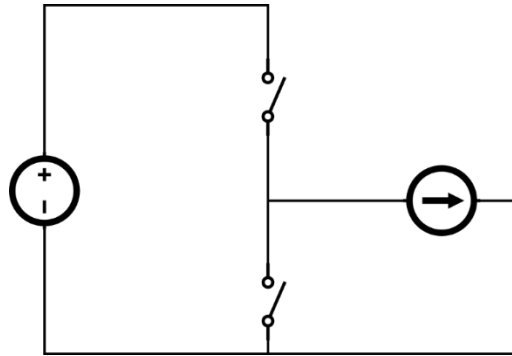


Figure 1.7: A switching cell diagram

1.2.2.1 Parasitic elements and their issues

In addition to the two semiconductors, each connection is associated with a parasitic resistance, inductance, and capacitance. These parasitic elements created by the interconnections are not the only undesirable elements, power semiconductors also introduce parasitic capacitances in the circuit, which are usually much larger than those of the tracks [24].

A certain parasitic inductance may be quite helpful during the turn-on transition of the switch – by acting to limit any current spike in the switch. But it can also be harmful due to the high voltage spike it creates across the switch at turn-off (as it releases its stored magnetic energy). On the other hand, a parasitic capacitance present across the switch for example, can be helpful at turn-off but unhelpful at turn-on, as it will dissipate its stored electrostatic energy inside the switch.

In the following paragraphs, an overview on relevant parasitic properties and their influence on switching losses and EMI in a switching cell will be given.

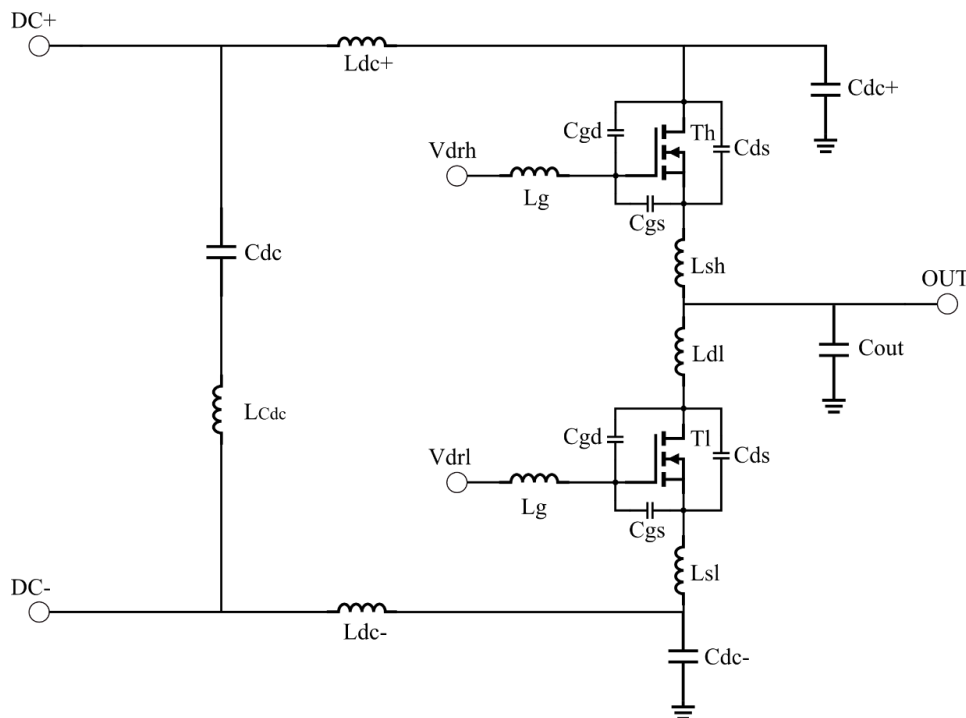


Figure 1.8: Parasitic elements of in switching cell [25]

The gate inductance L_g

This element is the inductance between driver and component. It can increase the impedance of the driver circuit and also produces the un-ideal oscillation with the input capacitance of semiconductor. It is usually high (tens to hundreds of nanohenrys) because the control circuits are often separated from the power components (on a printed circuit board above the module). An efficient remedy is to choose a short, low inductance connection between driver and semiconductor.

A low impedance of gate circuit is necessary to prevent the undesirable switching of power components: in Figure 1.8, when T_h turns on, the drain's potential of T_1 (V_{DI}) increase dramatically. A current proportional to dV_{DI}/dt will then pass through C_{GD} of T_1 . If the impedance of gate circuit of T_1 is low enough, it will absorb most of this current, and the gate-source voltage of T_1 will remain below the threshold voltage of component. If it is not the case, T_1 will turn on, leading to a series arm short circuit. This problem is particularly important for the SiC or GaN components, for which C_{GD} capacitances are very large [10, 26].

The source inductance L_s

The L_s inductance depends on connection method between the transistor source and the driver circuit. Due to the fast di/dt in the transistor, voltages will be induced in L_s and will lead to inverse feedback in the driver circuit. This will decelerate the charging process of the gate-source capacitance during turn-on or the discharging process of the gate-source capacitance during turn off, resulting in a significant increase of the switching times and therefore switching losses. However, we can note that this inverse feedback effect of the source may be used to limit the drain current di/dt in the case of short circuits near the modules.

The power loop inductance $L_D+L_S+L_{DC}+L_C$ (L_{tot})

The drain inductance stores electromagnetic energy ($\frac{1}{2}L_{tot}I^2$) when the corresponding transistor is in conducting state. In a hard switching circuit, this energy will be dissipated during the opening of the transistor, leading to turn off over voltage and a significant switching loss increase. L_D will also form an oscillating circuit with the stray capacitors of the power components. Therefore, this inductance must have the lowest possible value. As for the control circuit, the capacitors of the DC bus are usually placed away from the power modules (for practical reasons, or thermal reasons, as capacitors have lower temperature limits than power semiconductors). In consequence, L_{DC} can reach several tens of nanohenrys.

The output parasitic capacitance

This capacitance is formed between the output conductor (phase) and the surrounding ground (metallic housing, chassis, heatsink...), it is subjected to strong voltage variations during the transistors' switching. The common mode current will cross this capacitor and return to the input voltage source through an exterior circuit (metallic housing, chassis...), represented in the figure 1.7 with the "ground" symbol. This common mode loop is not easily controlled, and common mode current can pass through sensitive equipment.

In the case of a classical power module, which use a metallized ceramic substrate, C_{out} is in the range of several tens to hundreds of picofarads, but can reach a much more

important value according to the load connected to the converter (ex. a shielded cable linked to an electric motor). In extreme cases, C_{out} may involve a reduction of the switching speed.

Electromagnetic interferences

The switching cell is an important source of EMI disturbance particularly at high frequencies. To determine the generated interference level, two basic categories were proposed[27]:

- Common mode currents
- Differential mode currents

Common mode (CM) currents are mainly caused by C_{OUT} parasitic capacitor. As described above, the current flowing through this capacitor will return through the source via an external path. As a consequence, the currents through the DC+ and DC- terminals of the converter are no longer equal (with an opposite direction). This is equivalent to a current flowing in the same direction in both terminals, hence the same “common-mode current”. Therefore, a solution to reduce this CM current is to reduce this capacitance by improving the package.

The research in [28] has shown another relevant mechanism for the common mode interference. If the parasitic elements of supply lines in a power module are not symmetrical, the differential mode current is partially transformed into a common mode voltage. To reduce this effect, the stray inductance L_{dc+} and L_{dc-} , as well as the stray capacitance C_{dc+} and C_{dc-} of the supply lines should be equal.

Another solution is based on common mode filtering capacitors. They offer a shorter path for the common-mode current to return, and therefore allow to confine the common mode currents within the converter, hence avoiding the disturbance of external sensitive equipment [29].

The HF differential mode current also has to be prevented from going out of the module. This can be achieved by using a high frequency DC link capacitor in the package [28], and a HF filter (inductors).

1.2.3 Multicell power converter

The increase of the number of switching cells is necessary in high current or high voltage applications, because it allows the distribution of the voltage and the current constraints between several semiconductors or switching cells. Voltage regulator module (VRM) widely uses multicell parallel buck converters (Figure 1.9), but other emerging applications fields for these topologies are provided by systems connected to low-voltage energy sources and storage elements as photovoltaic (PV) arrays [30], fuel cells, batteries, ultra-capacitors [31], especially when these systems are embarked in mobile systems (e.g for transport applications) and weight and space savings are required.

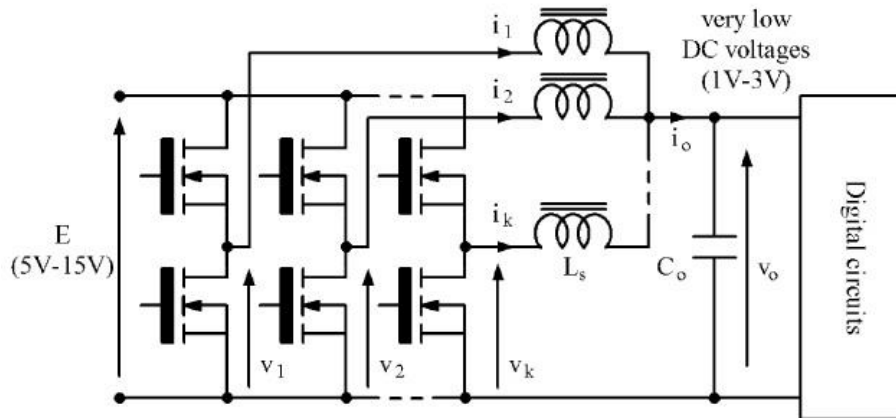


Figure 1.9: Example of an interleaved VRM converter with uncoupled inductors [32]

In classical interleaved multicell parallel converters, the inductor current ripple in each phase is still large and the inductor current ripple frequency is unchanged. An improvement proposed in [33] consists in the association of two cells using two output inductors magnetically coupled. Despite this coupling, the magnetic devices stay mainly an inductor and must be designed in this way; in particular, it requires an air gap and experiences eddy currents. The other solution is based on the introduction of coupling transformers (or intercell transformers - ICT) that are built by the association of elementary transformers (separate transformers) or realized on a monolithic magnetic core (monolithic transformer). A study shows that for the ICT solutions, the average induction in the transformer core is very low and the induction ripple value can be close to the saturation induction. The magnetic core volume is therefore much smaller than that of the equivalent uncoupled inductors [34]. A further advantage is the absence of air gap and the low DC induction component which allows to make the best use of materials that cannot be introduced in inductor solutions. Figure 1.10 shows a comparison of the phase current ripple for uncoupled inductors solution and intercell transformers. In both solutions, the output current ripple is strictly identical.

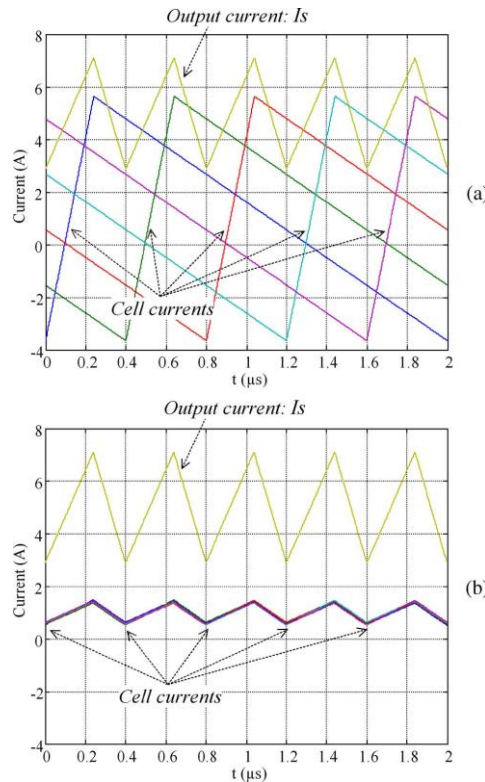


Figure 1.10: Output and winding currents for (a) uncoupled inductors and (b) InterCell transformer [35].

An improvement of ICT topologies has also been presented. Indeed, in case of supplying each output branch with a regular phase shifted voltage system, the ICT topologies (either monolithic or with separate transformers) leads to oversized magnetic cores. That can be emphasized by considering the transversal flux of a monolithic ICT transformer supplied by a balanced sinusoidal voltage system. It has been demonstrated that this oversizing problem can be solved by modifying the phase sequence [32]. A theoretical study, principally dealing with associations of separate transformers is proposed in [35].

The use of ICTs in the industry and their investigation by the scientific community is now growing. New structures are proposed offering insulation capabilities. In the field of insulated power converters, *flyback* converters are mainly used in low power applications. However, many applications require a power that cannot be handled by a classical *flyback* topology. Using the principle of multicell power converter, an original topology of interleaved *flyback* (Figure 1.11) compatible with higher power has been introduced in [36]. A test bench with 7 cells using a separated intercell transformer has been realized to validate the theoretical analysis and to demonstrate the feasibility of such converters with a high number of cells. To reach high power density, [37] proposed a design method specifically elaborated for the ICT. This design method is based on the area product calculation of generic core shapes for which sizes vary according to a homothetic law. It is precisely described in [38]. A prototype of 28V/10kW using planar cores and 8 power cells has been realized to validate the design process. The test results confirm the good potential of the multicell ICT *flyback* converter and valid the method to design this topology.

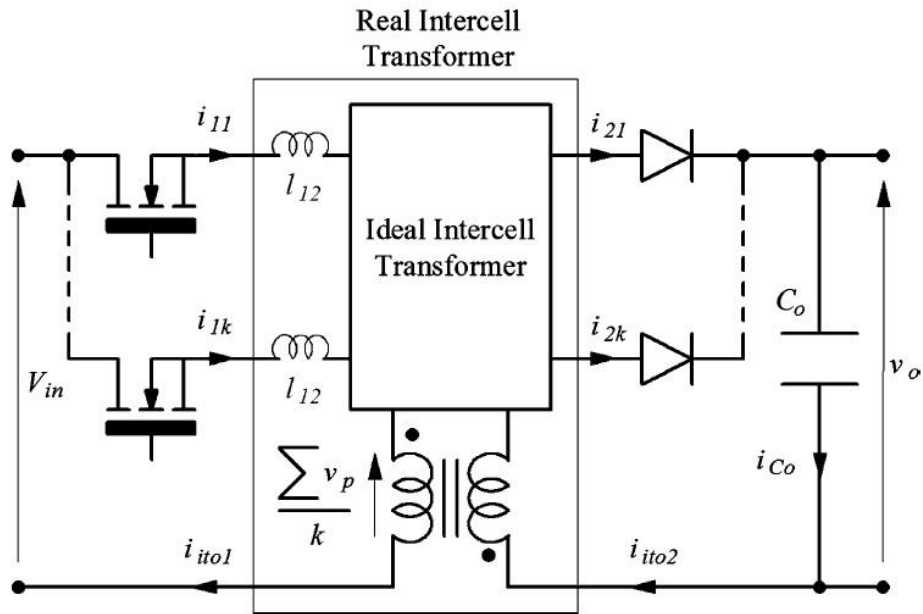


Figure 1.11: Interleaved flyback using IT [36]

However, even if this topology allows to reach high power densities, it suffers from some drawbacks. The main drawback is due to the difficulty to manage the transformers leakage energy as well as magnetic energy in the connections. To overcome this drawback, new topologies have been proposed, one of them is the so-called Buck or Boost topology which is actually design and tested in ANR ETHAER (see Figure 1.12)

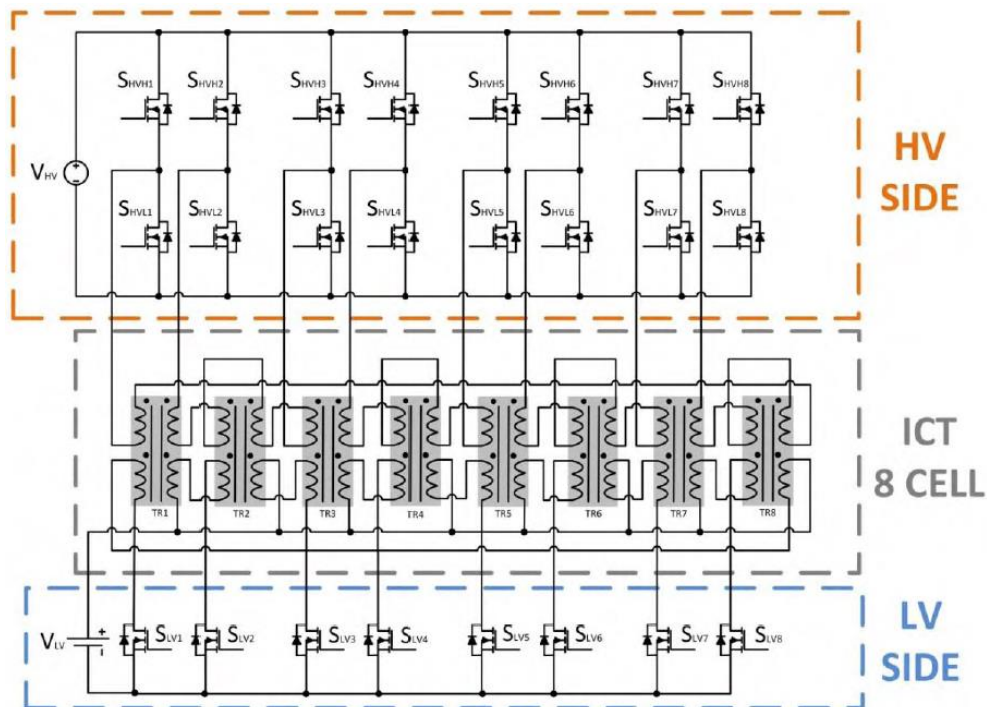


Figure 1.12: Buck or Boost (BoB) topology [39]

We can notice that this topology is also multicellular offering the same interest of other multicellular topologies in the field of power density. Nevertheless, such topologies as well as all multicell converters requires a lot of semiconductors and interconnections between the different cells. To reach an efficient design with a high power integration capability, it

is necessary to develop new multicell packaging offering the advantages of “collective” fabrication and inter-connection management. This packaging should also allow to control the thermal and electromagnetic disturbances. This topic, namely the power packaging of the multicell power converter is addressed in the ANR ETHAER project. It is the topic of the present memoir.

1.3 Power Packaging

The power dies are at the « heart » of a power converter, but they cannot function without the packaging. It is the packaging which protects the dies and isolates them from their environment, evacuates the heat they dissipate and establishes the electrical interconnections. In order to meet the demand for higher power density with excellent electrical, thermal and mechanical performance, improvement of new packaging technology is required.

The packaging can ensure at least four broad functions [40]:

- **Mechanical hold:** to allow to maintain the chips, while protecting them from their environment (dust, water, fingers...).
- **Thermal management:** to evacuate the power loss from the dies to the environment.
- **Electric isolation:** to ensure the isolation between different potentials in the circuit.
- **Electric connections:** to establish the internal but also external connections (terminals).

These functions are essential, as we can see in the next paragraphs, the packaging is usually the limiting point for the performance of power converters.

1.3.1 2D Packaging

1.3.1.1 Structure

The constitution of a 2D packaging as shown in Figure 1.13 will be presented in this paragraph. The bottom side of the dies are soldered onto the Cu layer of a DBC (*Direct Bond Copper*) type substrate.

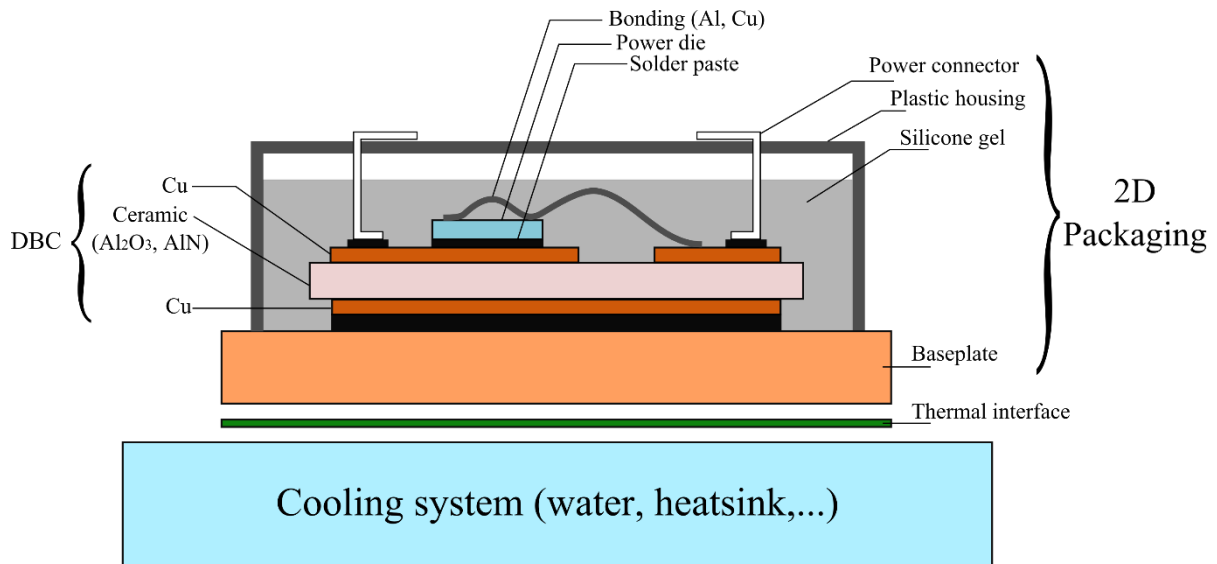


Figure 1.13: Cross-section of a 2D module

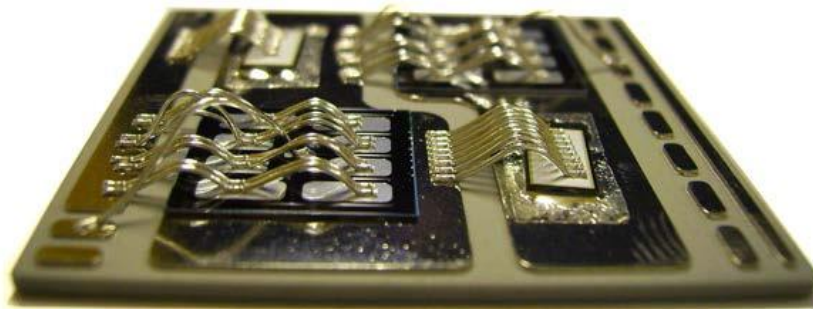


Figure 1.14: example of 2D package inverter arm (Doc. University of Nottingham)

The classic substrate in electronic is the Printed Circuit Board (PCB), assembled with numerous layers of glass fiber and copper layers by lamination. This technology allows the batch-processed manufacturing and low cost fabrication. However, it is not suitable for power electronic design, except for the discrete components of low power because of its poor thermal performance with a thermal conductivity lower than $1\text{W/m}\cdot\text{K}$. Besides, its maximum operation temperature is usually less than $200\text{ }^\circ\text{C}$ and its Coefficient of Thermal Expansion (CTE) is large, in the range of $60\text{ ppm}/^\circ\text{C}$ [40].

Another potential solution for the medium power domain (a few kilowatts) is the Insulated Metal Substrate (IMS). In this technology, a thin single-layer printed circuit is bonded on a metal baseplate, usually Al because of its low cost. The insulated layer of the IMS substrate ($100\text{ }\mu\text{m}$) is much thinner than that of PCB (1.6 mm) so the thermal performance is much better. But it is not a satisfying solution for high temperature application either, as its CTE is close to that of the aluminum ($23.6\text{ ppm}/^\circ\text{C}$) and its operation temperature is limited by its organic dielectric.

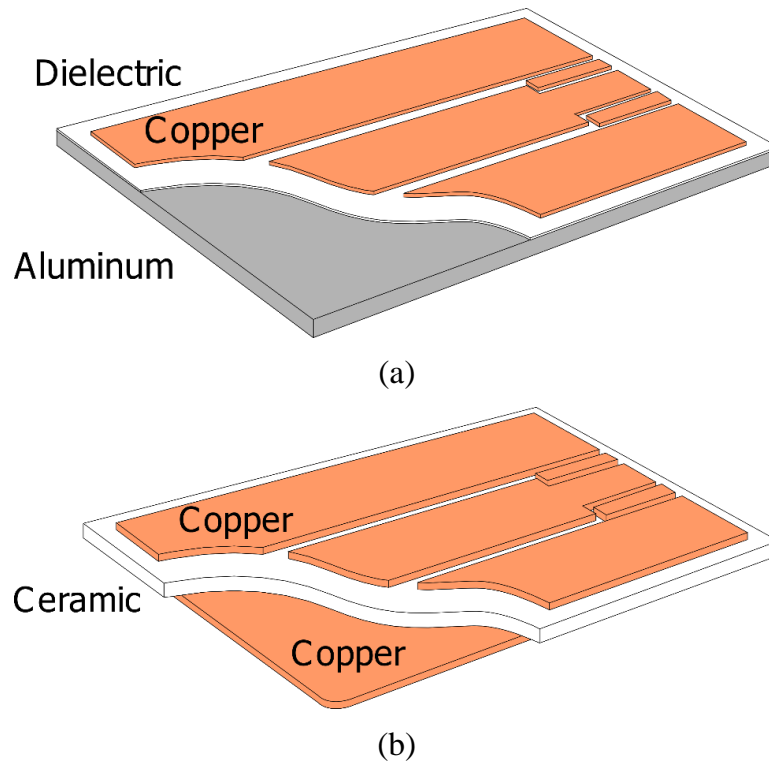


Figure 1.15: (a) IMS substrate structure, (b) DBC substrate structure [40]

In order to meet the thermal requirements of power electronics applications, a substrate based on ceramic material seems an attractive solution due to its good thermal property with a CTE close to that of the power dies. The DBC substrate contains two copper layers and separated by an insulating layer which can be alumina or aluminum nitride. The role of DBC substrate is to provide the interconnections to form an electrical circuit on the bottom side of the dies, and to ensure heat transfer of the components. This substrate ensure also the overall mechanical strength of the structure. The available ceramic materials are listed in Table 1.2.

Ceramic	Thermal conductivity (W/m·K)	CTE (ppm/°C)	Flexural strength (MPa)	Dielectric strength (kV/mm)	Relative cost
Al ₂ O ₃ (96%)	24	6.0	317	12	1
Al ₂ O ₃ (99%)	33	7.2	345	12	2
AlN	150 to 180	4.6	360	15	4
Si ₃ N ₄	70	3.0	932	12	2.5
BeO	270	7.0	250	10	5

Table 1.2: Principal properties of available substrate [41]

As we can see in the table, the alumina (Al_2O_3) exists in various purity level (typically 96% and 99%), this material has the lowest cost, but its thermal conductivity is relatively low (only 24 W/m·K for 96% and 33 W/m·K for 99%). For high performance application, the Aluminum Nitride (AlN), whose thermal conductivity is 150 to 180 W/m·K, is preferred. In addition, it offers a CTE close to that of the chips (CTE of Silicon for example, is 4.68 ppm/°C). The Silicon Nitride (Si_3N_4) is a promising ceramic, with an important flexural strength of 932 MPa. This allows to use it without any baseplate, which can reduce the module size [40]. The last material is the Beryllium oxide (BeO), it has an excellent thermal conductivity of 270 W/m·K (10 times than that of Alumina) but is often avoided because of its toxicity when its powder is ingested or inhaled.

The active components are attached to the substrate by soldering. This technology is based on the melting of an alloy (under vacuum or under reducing atmosphere to prevent oxidation). In the liquid state, this alloy will form new alloys or intermetallics with the attached pieces. After cooling and solidification, the mechanical bond is obtained.

The interconnection, located on the top side of the dies (or between the die and external connectors), are usually realized by wire bonding. The high current switched by the power components (up to 200 A on a 10×10 mm chip) requires interconnections with a very low resistance. In order to achieve this, a number of wire bonding with large diameter ($\approx 300 \mu\text{m}$) are paralleled (see Figure 1.14). In this wire, the used metal quantity is really important. These wires can be realized in gold, aluminum, silver or copper, but the aluminum is the most used by the manufacturers due to its low cost and sufficient low resistance. To reduce the resistance further, another solution is to replace the paralleled wire bonding, by ribbons, which have a larger cross-section on contact area with the die. A typical dimension for ribbons is 200 μm thick and 2 mm wide [42]. The assembly is finished by encapsulating the dies and their interconnects in some silicone gel. To maintain the junction temperature of components below a critical value, the power module is fixed on a cooling system.

1.3.1.2 Limiting points

From the functional point of view, the most important limiting factor in the 2D structure is the impossibility of double-side cooling. That is because of the presence of bonding wires on upper side of components. This side cannot be exploited to improve the thermal exchange between chip and exterior environment.

The second limiting point is the important parasitic inductance of bonding wire, which is between 6 nH and 16 nH [43]. This parasitic inductance will contribute to a voltage overshoot during active components switch-off, which may damage them, disturb their control signals [43] and increase their switching time. This is especially true for wide-bandgap devices, which can be operated at higher switching speed and higher switching frequency.

Another point is the degradation of the module caused by aging mechanisms and thermo-mechanical fatigue. Figure 1.16 shows an example of fatigue cracks formed in the die-attach of a power module. Two materials with different CTE are assembled. When the module is operating under varying temperature, the interface between both materials (one subjected to compressive stress and the other to extension) will experience a shear stress. It is this stress, repeated many times during the operating lifetime of a module, that cause aging phenomena, and then the possible delamination of interfaces, or cracks of some layers [40].

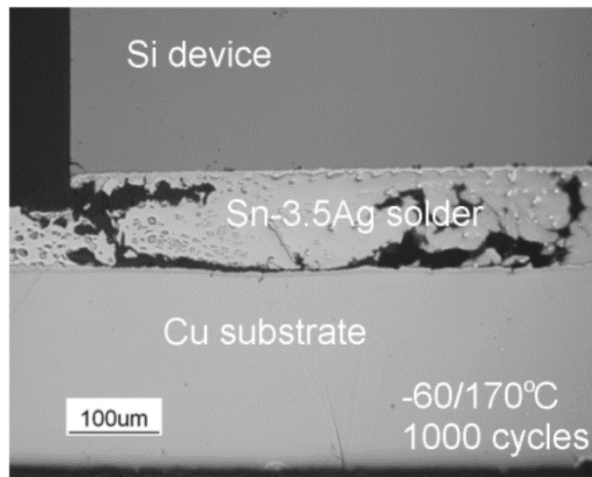


Figure 1.16: fatigue cracks in soldering between the Si die and the metallic part of a DBC substrate [44]

Thermo-mechanical aging can appear in different parts of a power module:

- Bonding wires [45]
- Interface between bonding wires and metal part of substrate [46]
- Soldering between the device and metal part of substrate (Figure 1.16) [44]
- Ceramic of the substrate [47]. This could cause the delamination of the metal layers (Figure 1.17)

In the case of bond wires, the solution, which is able to limit this degradation phenomenon, is to deposit a polymer resin on the foot of the wire [48]. Regarding the substrate, there are also two solutions, one is to reduce the thickness of the metallization layer [49] and the other is to etch the pattern to form dimples, on the edge of the leads [50] (shown in Figure 1.18).

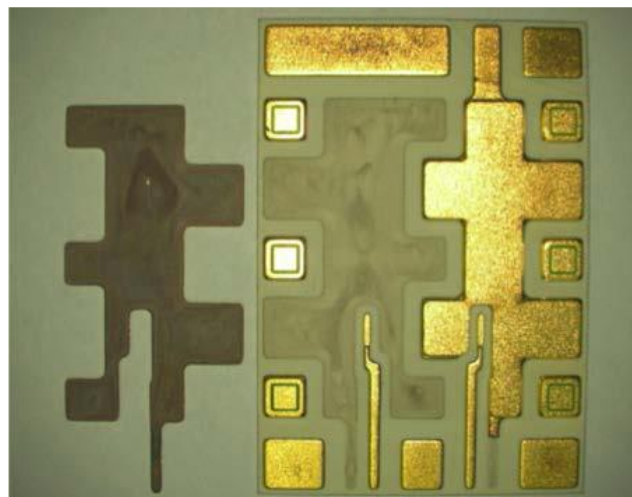


Figure 1.17: Delamination of metal layer of a metallized ceramic substrate (Doc. University of Nottingham)

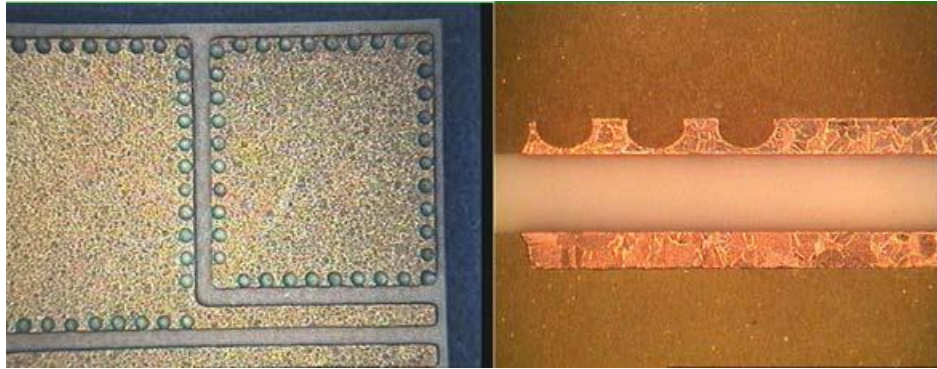


Figure 1.18: photograph of “dimples”, etched pattern for increasing the thermal cycle [50]

1.3.2 3D Packaging

Over the last decade, wire-bonding has been the dominant interconnection technique for power devices due to its maturity. However, in the area of high-power or high-temperature applications, there are a lot of limitations concerning high stray inductances, mechanical damage or mutual coupling effects [51]. In addition, the two-dimensional packaging structure has limited heat-dissipation capability. In order to improve electrical and thermal characteristics and to reduce package size, researchers and manufacturers have focused on non-wirebond three-dimensional (3D) packaging solutions.

1.3.2.1 Metal post interconnection technology

The metal post interconnection technology is based on copper posts which are soldered on to the bonding pads of the processed devices. One of this 3D assembly is called the metal post-interconnected parallel-plate structure (MPIPPS).

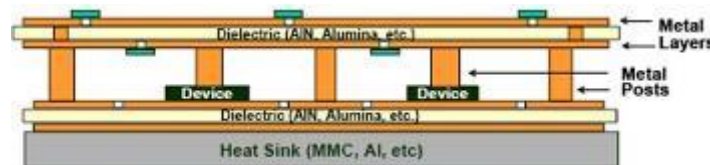


Figure 1.19: MPIPPS module [51]

Elimination of the wire bonds significantly reduces the inductance generated by the interconnections. A study shows that a copper post generates only 1.27 nH [51] [52]. Additionally, the copper post can be machined to maximize the contact area with the bondable surface of the die, further reducing the overall inductance. Another important objective of the MPIPPS design is to improve the heat dissipation capability of the package. This technology allows a double side cooling, and some of the heat dissipated by the devices can be removed through the copper posts [53]. Thermal modeling of the MPIPPS module and a comparable wire-bond module showed that the maximum junction temperature on the IGBT chips in the MPIPPS module can be lowered than the wire-bonded module by 17 °C [51].

1.3.2.2 Solder bump interconnection technology

The solder bumping interconnection is based on the deposition of flip-chip solder bump on the power device [54]. The solder bump can be made of lead-free Pn/Sn, Sn/Ag or Au

(Figure 1.20). This technology is used in the micro-electronic domain to decrease the assembly size and improve its electrical and thermal performance. Besides, several semiconductor manufacturers develop their power components with this technology in order to reduce the parasitic inductance and voltage drop for very low voltage components (Fig.1.6).

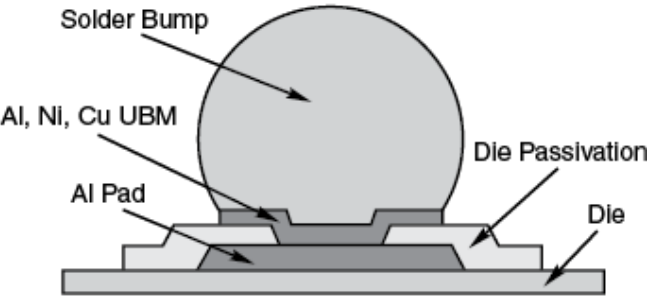


Figure 1.20: Solder bump interconnection [21]

In an effort to further optimize solder bump connections, a novel triple-stacked solder-bump geometry was developed [55] for enhanced reliability of the joints. This geometry involves additional solder deposition and reflow steps and the use of several alloy types with different melting points to form the stacked structure whereas common flip-chip interconnections make use of a single reflow process to produce a solder bump. The construction process seems more complex, but it provides the ability to control the joint height and shape while maintaining compatibility with surface mount technology. In a production environment, it may be possible to do away with the extra alloys and reduce the number of reflows into a single step. Different solder alloys with different melting temperatures are needed to preserve joints formed in a previous reflow. The stacked joint can either have an hourglass or barrel shape, shown in Figure 1.21.

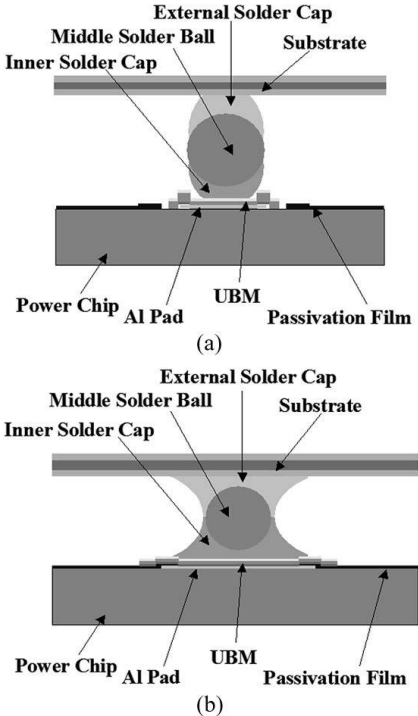


Figure 1.21: Stacked solder joint configurations. (a) Triple-stack barrel shape. (b) Triple-stack hourglass shape [51].

To improve the reliability of solder bumps and protect them from contamination, the so-called underfill is used to fill in the gaps between the chip and the substrate. A further advantage is that the life cycle of solder joint could be between 10 and 100 times longer than that without underfill [56], because the underfill reduces the mechanical load on the solder interconnects. Like other solder contact technologies, the solder bump technology allows a double-side cooling of the chip. The thermal resistance is much lower than wire bonding. A study [57] shows that a 1 mm² solder bump of 1 mm high has a thermal resistance of 19.6 K/W and an electrical resistance of 0.15 mΩ. whereas a wire bonding with a diameter of 254 μm and a length of 3 mm has a thermal resistance of 254.8K/W and an electrical resistance of 2.6 mΩ. Furthermore, this study showed that the solder bump interconnection has a lower parasitic inductance (less than 0.2 nH) than that of the bonding wires (2.6nH)

1.3.2.3 Dimple array interconnection technology

The dimple-array interconnect (DAI) (shown in Figure 1.22) is a 3D packaging technique, where the electrical interconnection is established by the formation of solder bumps between device electrodes and the preformed array of dimples on a flexible metal sheet (thickness between 50 μm and 400 μm) [57, 58]. The result is a low-profile planar interconnection that is suitable for multilayer integration with other components. The soldered dimples form interconnecting joints that take the natural shape of an hourglass. Which enhances the reliability of the joint compared to a barrel-shaped geometry. With the exception of fabricating the dimpled copper sheet, the DAI process follows the typical solder joint fabrication process. Copper is the preferred material for the dimpled metal sheet due to a favorable combination of low cost, ease of formability, and high electrical and thermal conductivity.

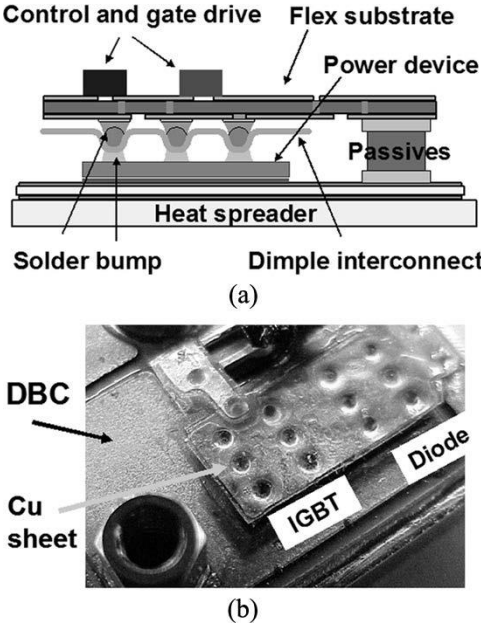


Figure 1.22: (a) Implementation of the DAI in an integrated 3-D power module. (b) Section of a DAI half-bridge power module showing the dimpled copper sheet over the IGBT and diode.

This technology offers better thermal and electrical performances than the solder bump interconnection technology, a dimple array of 1 mm² section and 0.33 mm height has a

thermal resistance of 6.5 K/W and an electrical resistance of 48 $\mu\Omega$ while a solder bump of 1 mm² section and 1 mm height has a thermal resistance of 19.6 K/W and an electrical resistance of 150 $\mu\Omega$ [57]. Furthermore, the parasitic inductance of a DAI interconnect is lower than that of a bonding wire (the module with DAI interconnect has lower switching loss than the module with wire-bonding [59]). Due to the concave shape of its solder, the DAI interconnect is less sensitive to the thermomechanical constraints than the solder bump [59, 60]. As for the solder bump interconnection, some underfill can be deposited around the dimple array in order to improve its reliability and avoid contamination.

1.3.2.4 Direct solder interconnection technology

The direct solder interconnection technology consists in soldering the top and the bottom side of the chip on a ceramic substrate [51]. Figure 1.23 shows a 3D assembly where the source and gate side of a MOSFET were attached simultaneously with the drain side using large area lead-free solder paste (Sn- 3.5Ag) [51]. This technology is easier to implement compared to other soldering-based interconnection. Besides, because the direct solder is thin (about 100 μm) and has the same area as the die, this type of interconnection has a lower thermal and electric resistance [51]. Furthermore, this approach enables dual-side cooling. Figure 1.24 shows a comparison of the temperature distribution in the solder bump and direct solder packages obtained by thermal analysis where a heat dissipation of 8 W was used for the power MOSFET, and an equivalent heat-transfer coefficient of 1000 W/m K from both surfaces of the DBC substrates was assumed [61].

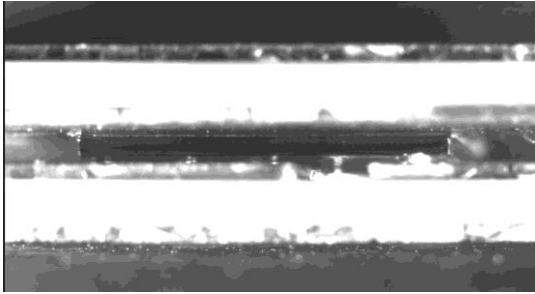


Figure 1.23: DS interconnected device attached to DBC substrates [61]

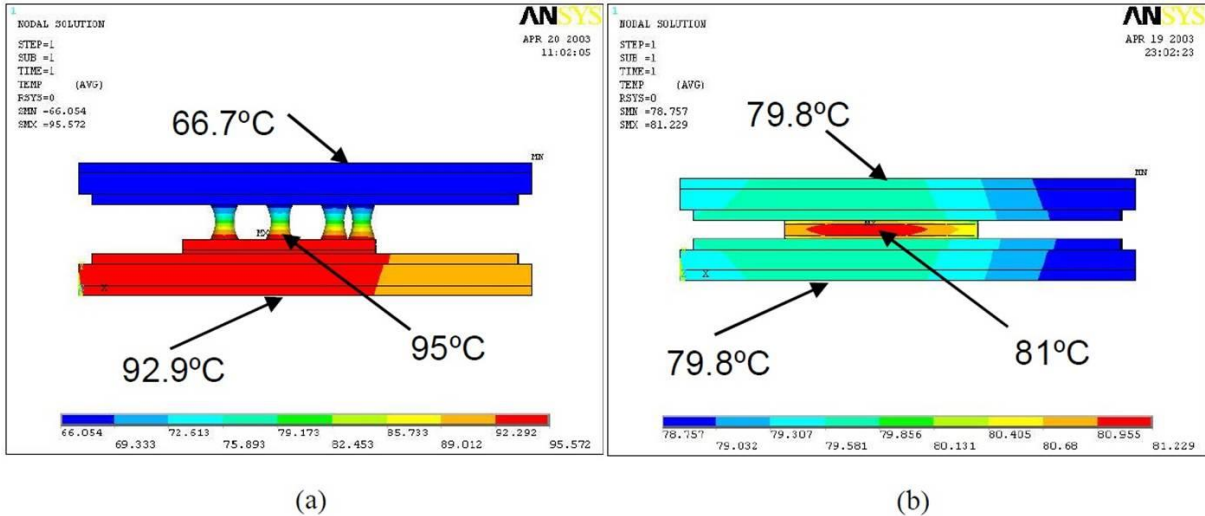


Figure 1.24: Temperature distribution of (a) the Direct Solder and (b) Solder Bump packages during the same operation and (double-sided) cooling conditions [61]

This analysis with the software ANSYS shows that the device operating temperature is about 95 °C and that 2.24 W (28%) of heat are dissipated through the top DBC, while in the Direct Solder package, the device operating temperature is about 81 °C and dissipates about 4 W (50%) through the top DBC. This result proves that thanks to the area of direct solder interconnection being more significant than that of solder bump interconnection, the thermal resistance of the direct solder package is lower than that of solder bump package. However, a study shows that direct solder technology seems less reliable than solder bump technology [61].

1.3.2.5 Embedded power technology

The embedded power technology [62] developed by CPES employs a planar integration technology, in which an integrated power chip is built by embedding chips in a coplanar ceramic substrate with a metallization providing both power chips bonding, and second-level interconnect wiring (Figure 1.25). The thickness of the copper metallized layer can vary from 75 μm to 125 μm [63].

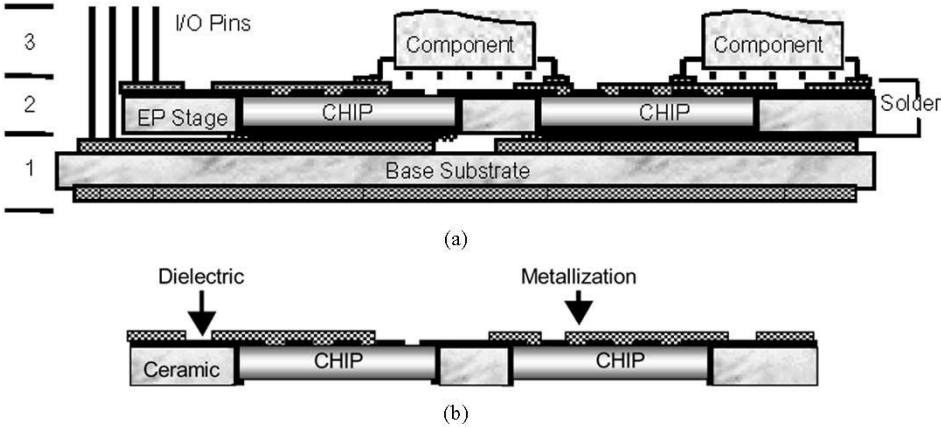


Figure 1.25: Structural schematic of (a) an embedded power module and (b) an integrated power chips stage [62]

In [64], electrical characterization shows that the embedded power module considerably reduces (more than 10 times) the packaging parasitics compared to the wire bonding technology. It has been demonstrated that such embedded power module has a better thermal performance than wire bonded modules. However, the reliability needs to be considered because of the higher density of power dissipation.

1.3.2.6 Press Pack technology

The Press Pack technology consists in connecting the top side of the chip on the copper plate through a pressed contact. Between the copper plate and the chip's top side, a buffer layer in molybdenum is added in order to reduce constraints on the chip's metal part. This structure does not have the solder or bonding wires except for the control circuit, and it allows a double-side cooling of the chip. Furthermore, it ensures an excellent reliability and functioning time [65]. The classical versions of the press-pack, however, are not suited to multi-chip applications, as they are designed to host a single device (a wafer-sized diode or thyristor).



Figure 1.26: Photography of a Press-pack module (Dynex Semiconductor)

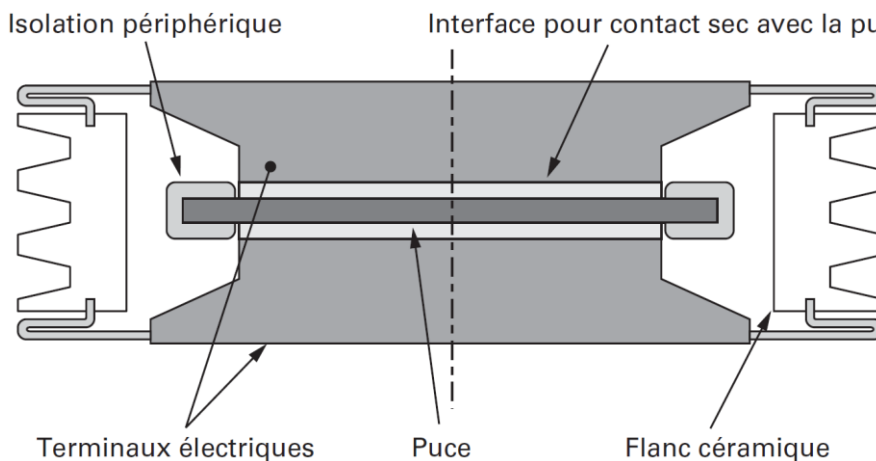


Figure 1.27: Cross section of Press-pack module [40]

The G2Elab laboratory proposed a different version of this technology [66] (as shown in Figure 1.28). Two chips are assembled one on top of the other within the same module. The top side of the chips are connected to the copper plate by pressing. This technology does not need the bonding wires reducing thereby the parasitic inductance.

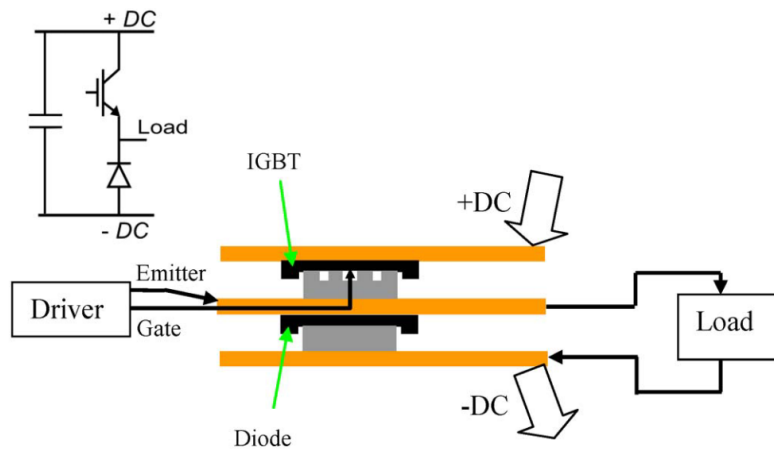


Figure 1.28: Switching cell by using the Press-Pack technology [66]

1.3.2.7 Spring contact technology

This technology is developed by *Semikron*. Among different products, they have developed a power module (*MiniSKiip*) which uses springs to establish the electrical contact

between the control part and the power circuit [67]. There are several spring types and they are chosen according to mechanical and electrical requirements. In the *MiniSKiip* module illustrated in Figure 1.29, a special spring shape is used, which is able to support currents up to 20 A. This technology improves the assembly resistance to thermal cycling [68] but it doesn't provide double side cooling of the chips.

Figure 1.30 presents another spring contact technology called "spring pressure contact" using a beryllium-copper type spring [69]. This material is selected due to its high thermal conductivity, high strength and high fatigue-resistance. The spring, made of BeCu, offers a certain flexibility that help reducing thermal stress compared to other 3D packaging technologies. The spring is gold-plated to reduce electrical resistance and prevent oxidation. It is also important to add a Cu/Au layer on the top side of the Al chip. This technology offers double side cooling capability, the top side cooling is possible through the spring. However, the spring is relatively long, creating a high thermal resistance path. The bottom DBC substrate is therefore the main power dissipation path. Even if the electric path is quite long in the springs, the parasitic inductance of "Spring Pressure Technology" is three times lower than that of the "wire bonding technology". Nevertheless, the reliability of this technology is not yet totally demonstrated.



Figure 1.29: The *MiniSKiip* module with spring contacts [70]

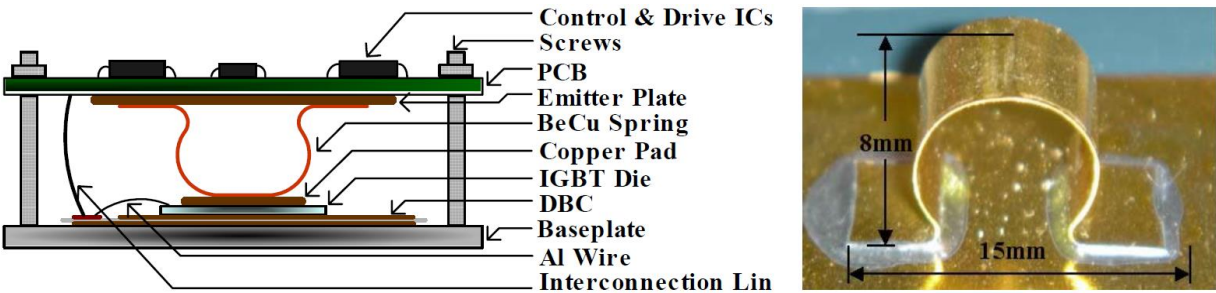


Figure 1.30: Spring pressure contact technology [69]

1.3.2.8 PCB technology

A solution to make converters more compact is based on flex PCBs technology: Advantages offered by this technology linked to its ability to be rolled around the larger

components [71] or folded in a sophisticated fashion [72]. Such approach may make thermal management difficult, and seems more suited to low-power converters (up to a few hundred watts). Another possible use of the flex PCB is as direct replacement for the wirebonds: the power semiconductor dies are attached to a ceramic substrate, and a flex PCB is attached on the top of the devices. This flex PCB also provides the interconnections between the topside of the dies and the ceramic substrate if needed. Such a solution requires dies with a suitable topside metal [55] (most power dies have an aluminum layer, which is suited to wirebonding, but not to soldering or sintering). Compared to wirebonds, the flex PCB offers higher interconnect density [73], especially because it can have several layers. Furthermore, auxiliary components (such as the gate drivers) can be mounted directly on the flex PCB [74]. An example of power modules that use flex PCB instead of wirebonds is given by *Semikron* [75] (shown in Figure 1.31).

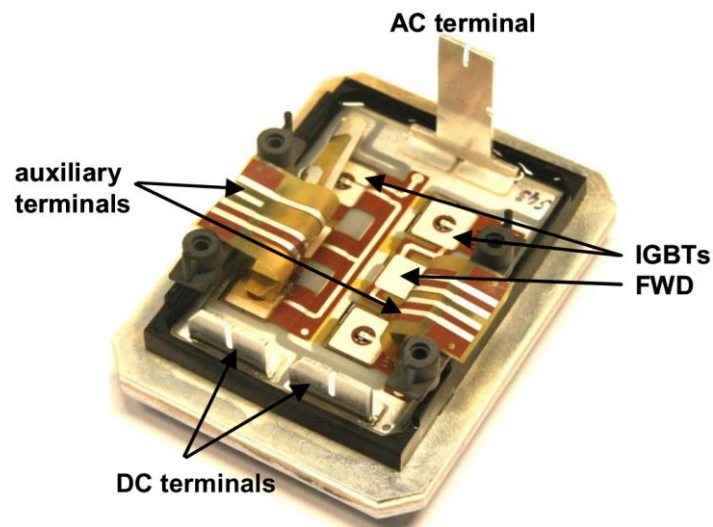


Figure 1.31: Photo of a 400A, 600V dual IGBT SKiN device [75]

Another set of solutions is based on rigid PCBs rather than flex. Rigid PCBs are thicker (from a few hundred of microns up to a few millimeters), so it is possible to integrate devices within the PCB. For example, various manufacturers sell dielectric layers that can be stacked in a multilayer PCB to form capacitors [9]. An example (shown in Figure 1.32) of a converter integrating such capacitive layers is given in [76]. In this paper, the authors also embed some magnetic layers to form an “embedded Passive Integrated Circuit” (emPIC). However, most papers focus on integrating the active rather than the passive devices in the PCB. This allows for a shorter distance between the active die and the cooling system. PCBs have poor thermal conductivity (usually lower than 1 W/m.K, as compared to 24 W/m.K for alumina or 150 W/m.K for AlN ceramics), and power semiconductor devices generates a high thermal power density (100 W/cm² or more).



Figure 1.32: Thin 60-W offline converter with PCB integrated transformer and capacitors [76]

Some researchers do not use the PCB technology, but the structure they propose offer many features of PCB embedding. For example, in [77], power dies are attached on a DBC and integrated in a ceramic frame. In [78], a polyimide (*Kapton*) layer is used around the dies. Finally, the “*SiPLIT*” technology [79], uses some steps of the PCB technology (lamination, electroplating) to form a power module with very low parasitic inductances. A list of commercially-available, PCB integration technologies for active devices (not limited to power devices) is given in [80]. Many of these technologies were developed through the European projects “Hermes” and “Hiding Dies”, or through the German project “*HiLevel*”. These projects included work on the manufacturing technology, on the design tools, and on validation [81].

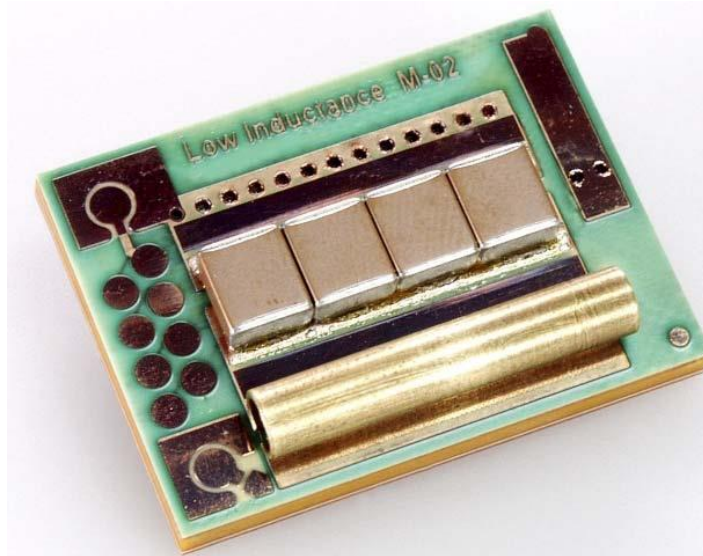


Figure 1.33: Manufactured module with DC-link capacitors and current measurement [82]

In particular, one of the demonstrators of the “*HiLevel*” project included a 50 kW inverter for hybrid cars. It is described in [83]: the dies are attached to a thick copper layer (no DBC substrate used here), and then embedded in a multilayer PCB. The pads of the dies are then exposed by removing some of the PCB material with a laser. In [82], the exposition of the pads is performed by mechanically grinding away some of the PCB materials. The resulting converter offers very low parasitic inductances, and allows for very close decoupling, as the decoupling capacitors are mounted directly over the power semiconductor dies.

1.3.3 Conclusion

In this section, the functions of the power packaging and principle elements of a classical “2D” packaging are firstly shown. Some limiting points of this kind of packaging are then given. These limitations lead the creation of new “3D” interconnection solutions which have advantages in thermal management and electrical performances. However, the reliability of these solutions needs to be improved.

Among these solutions, the PCB technology is very attractive for us, especially for electrical interconnection. Due to its low inductance interconnects which allows the lower switching losses than the classical wire-bonding interconnection. Its multi-layer structure and small pitch allow high interconnect density. Auxiliary components (drivers, capacitors, etc.) can be soldered directly on the PCB, which reduce furthermore the package size. Despite these interesting points in power electronics domain, PCB substrate has very low thermal conductivity. As a consequence, we will use the DBC substrate for heat dissipation.

1.4 Fabrication Process

The thesis work focuses mainly on the fabrication technology for integrated power converter. Therefore it is necessary to present some of typical fabrication processes we will use in the laboratory.

1.4.1 Solder

There are two soldering stages in a “classical” power module: the first one attaches the chips and the terminals to the substrate, and the second one attaches the substrate to the baseplate. These two stages are realized successively. The melting point of the alloys utilized for these two stages should be different, to avoid the melting of the first stage during the soldering of the second [40]. In practice, it is necessary to choose alloys whose melting points difference is at least 40 °C [84].

The soldering process of these two stages is operated in the following method:

1. Placement of the soldering paste between the two elements by screen printing.
2. Reflow by following the adapted temperature profile of the alloy. The control of the melting profile allows to limit the formation of intermetallics which will weaken the solder.
3. Cooling down to the room temperature.

In the most common applications, the chips are soldered on the substrate by melting an alloy of lead (90 to 99%), with a melting point of 300 °C. In order to attach the substrate, the alloy type “SAC” alloy (a lead-free alloy containing Tin -Sn-, silver -Ag- and copper – Cu-) with a melting point slightly above 200°C is used.

Lead-containing alloys are currently phased-out due to RoHS (Restriction of Hazardous Substances) regulations. Once the alloys based on lead are removed, the remaining high-temperature alloys will principally be based on gold (AuSn, AuGe, AuSi). These alloys are expensive (they contains more than 80% of gold), and their implementation is more complicated than the lead-based solders: they form fragile intermetallic compounds and require a careful control of the process parameters to prevent the formation of voids

[85]. We can also cite the alloys based on zinc or bismuth, however, these alloys seem actually seldom used, due to an even more complicated implementation [86].

1.4.2 Sintering

Sintering, especially of the silver, is a promising technology for power electronic packaging. It is becoming an attractive alternative to soldering, especially for high temperature applications. The classic solder technology has very low melting point (below 250°C). With the development of the wide band gap semiconductors, the junction temperature will increase to more than 200°C. The process of sintering happens totally in a solid phase. The assembly material is a powder, which is processed at a moderate temperature (usually inferior than 300°C). The diffusion mechanisms push the powder particles to join and form a solid joint with a melting temperature of 961 °C in the case of silver.

Different kind of silver pastes exists at present: the most common ones, industrially utilized for example by *Semikron* [87], contain silver particles of micrometric dimension (1 to 20 µm). These pastes require the application of an important pressure (in the range of 40 MPa, which means 4000N on a chip of 1 cm²). This requires a suitable tool to avoid damaging the components [88]. The second type has nanometric particles [89] (in the range of a few tens of nanometers), much more reactive and allowing in theory to sinter without the assistance of mechanical pressure.

1.4.3 PCB technology

A PCB has two main parts: the substrate (the board) and the printed circuit (the copper traces). The substrate provides the mechanical supports and electrical isolation. A broad range of substrate materials can be found in PCB designs. A common type is FR-4 (Flame Retardant, “4” means the glass reinforced material), which is a glass-fiber-epoxy laminate.

The PCB manufacturing starts with a copper clad substrate as shown in Figure 1.34. A rigid substrate is a C-stage laminate (fully cured epoxy). A substrate can have copper on one or both sides. This copper clad substrate is also called “core” and can be used to fabricate multilayer boards. In such boards, the cores are glued together with one or more layers of a partially cured epoxy (“prepreg” or B-stage laminate) as shown in Figure 1.35.

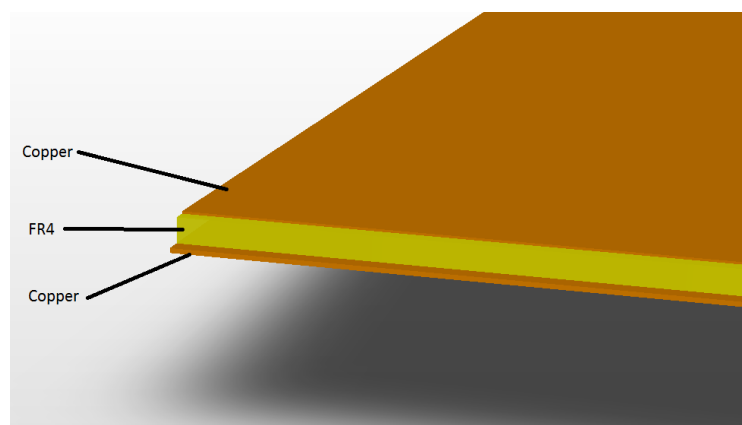


Figure 1.34: Double-sided copper clad FR4 substrate [90]

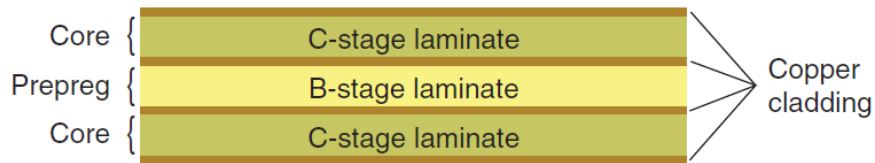


Figure 1.35: Cores and prepreg [91]

The prepreg is a glass fabric pre-impregnated with resin. The majority of the resins used in PCBs are thermosetting resins, and mainly used ones are epoxies. Other thermosetting resins such as polyimide or polyester are also used [92]. Glass fabrics are formed by weaving glass yarns. Figure 1.36 illustrates two different glass type. The left one is a “1080” (which is used in this thesis work) having small glass fiber diameter and a high resin content. The right one concerns a “7628” style which has a larger fiber diameter and lower resin content. Both of these glass styles are E-glass (“E” because of initial electrical application) which is the most common type. The number (“1080” or “7628”) is the norm which is standardized by the Association Connecting Electronics Industries (IPC) in the document IPC-EG-140 linking to the thickness of the glass fiber. More glass style and their specifications in the E-glass can be found in [93]. Other glass types available include S-glass, R-Glass, T-Glass, D-glass and SI-glass. The difference between these styles is their composition (SiO_2 , CaO , Al_2O_3 , etc.). Another material used for reinforcing the resin can be a non-woven aramid paper as shown in Figure 1.37, which is chosen for its low CTE (x, y) (6-9 ppm/ $^\circ\text{C}$ from Arlon 55NT [94]), its good dielectric strength and chemical resistance [92].

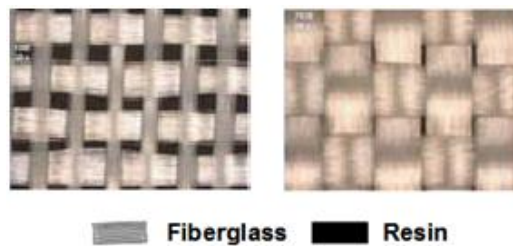


Figure 1.36: Glass fabric composition [95]



Figure 1.37: Non-woven aramid (photo Courtesy of Dupont)

The copper traces on a PCB can be formed by removing the unwanted copper parts. There are two common methods to realize this: chemical etching and mechanical milling. Chemical etching is more used due to the possibility of large scale manufacturing. This method will be used in this thesis work. Mechanical milling is usually used for smaller production.

In order to etch the unwanted copper part, the wanted copper should be protected. This protection is provided by a polymer coating (photoresist) which is deposited onto the copper layer. This photoresist layer is then formed into the desired circuit through a process called photolithography. This process contains two steps: exposing the photoresist to ultraviolet (UV) light and developing it. There are two photoresist types: positive and negative. When positive resist is exposed to UV light, the coating can be removed from the copper. In the contrary, negative resist maintains from UV light. A mask is used to expose the desired part of the photoresist, which is placed on top of the photoresist. It contains the dark areas which block the UV light and the transparent part which receive the UV light. After the exposing of the photoresist, the PCB substrate is washed in a chemical solution called developer. In the case of positive resist, the exposed resist is removed by the developer. In the case of negative resist, the unexposed resist is removed. Afterwards, the board is sprayed with an acid solution which etches away the copper foil. The copper that is protected by the photoresist material is unaffected by the acid. A typical fabrication process is shown in Figure 1.38.

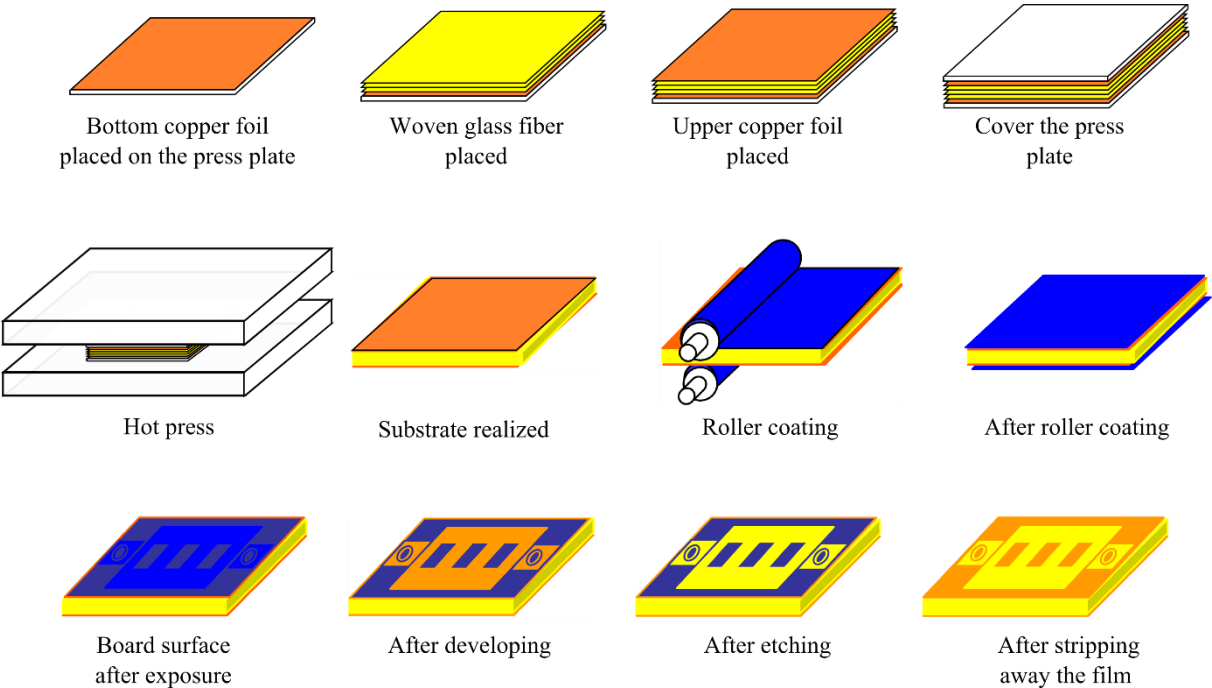


Figure 1.38: Fabrication process of PCB [96]

1.5 Conclusion

In this chapter, some important features of the power converters are firstly presented. The active components, the switching cell and its parasitic elements are introduced in the first section. The multicell power converter topology proposed and developed for the ETHAER project is also presented.

A detailed presentation of the “2D” package is then given. Each element in the package is defined. The advantages and some limiting factors are presented. The bonding wires and the soldering paste are the two main points which limit the performance due to thermal or electromagnetic issues.

The second part of this chapter focuses on the “3D” packages which are developed to solve the thermal or electromagnetic problems. According to these 3D structures, we can highlight their advantages comparing to classical planar modules. In planar modules, as shown in Figure 1.14, the heat dissipation can only be realized in one direction, from the chip to the heatsink. The silicone gel which encapsulate the chip is a poor heat conductor (the conductivity is normally less than 1 W/m.K), and only the bottom side of the module is connected to the heatsink. In a 3D module, the heat can be evacuated through both the upper side and the bottom side of the package. It is then theoretically possible to reduce the thermal resistance of the package by half. In order to minimize the thermal resistance, the electric insulation layer placed at the interface of the module should have the highest possible thermal conductivity but a high dielectric strength.

The electrical wires and the connectors of the planar module generate non-negligible parasitic inductance (in the range of 10nH for the wires, several tens of nanohenrys in total [66]). For vertical dies, reducing the stray inductances usually requires to improve the connection on the top side of the chip where the wires connect the chip with other elements. Removing these wires allows to reduce the distance between the components and the auxiliary circuits, and therefore allows to reduce the parasitic inductance. Currently we can observe that there is a tendency toward power integration using printed circuit technology: connections of the top side by a flexible board, or embedding the chips and passive components in a multi-layer printed circuit. A part of this thesis work will use this PCB technology to realize the integration of power converters.

At the end of this chapter, we presented some of typical fabrication processes that will be used in the next chapters.

CHAPTER 2. Low voltage packaging with GaN FETs

2.1 Introduction

As introduced in the first chapter, a new multicell power converter topology has been proposed, for the Buck or Boost Converter Unit (BBCU) dedicated to the DC power network. In the targeted application, this converter manages the interconnection between the low-voltage (28 V) and high voltage (540 V) networks in an aircraft. Given the large difference in voltage between both networks, we can assume that different semiconductor technologies will be used on each side of the transformer. In this chapter, we will focus on the packaging technology for the low voltage side, for which we will be using GaN transistors. We will firstly introduce the packaging concept, which relies on using ceramic substrates, and the issues associated with GaN transistors. Then, we will present the fabrication process of the prototypes. Finally, the thermal and electric performance will be analyzed by experimental tests and FEM simulations.

2.2 Proposed structures

2.2.1 Presentation of the GaN components

The low voltage packaging uses the lateral GaN transistors manufactured by EPC. These eGaN FETs (enhancement mode, 40V - 33A) shown in Figure 2.1, have a very small die size ($4075 \times 1602 \times 685 \mu\text{m}$), and a low on-state resistance ($R_{\text{DS(on)}}=4 \text{ m}\Omega$). They have a Si substrate, with all the terminals on the same side of the power die. These terminals have an interleaved layout, and are equipped with solder bumps for “flip-chip” mounting.

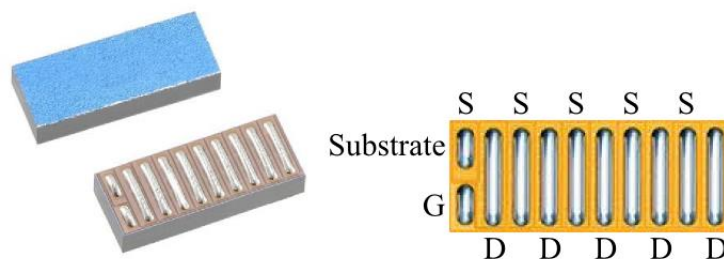


Figure 2.1: EPC GaN transistor [97]

Figure 2.2 and Figure 2.3 show the typical output characteristics, the transfer characteristics, the curves of $R_{\text{DS(on)}}$ versus V_{GS} for various drain current values and the curves of $R_{\text{DS(on)}}$ versus V_{GS} for various temperatures. These figures come from the datasheet of the device. The GaN transistor is off for $V_{\text{GS}} = 0\text{V}$ (normal-off behavior) and fully on for $V_{\text{GS}} = 5\text{V}$. The typical threshold voltage V_{Th} is 1.4V. This value is lower than that of Si MOSFET components which is typically 2.5V.

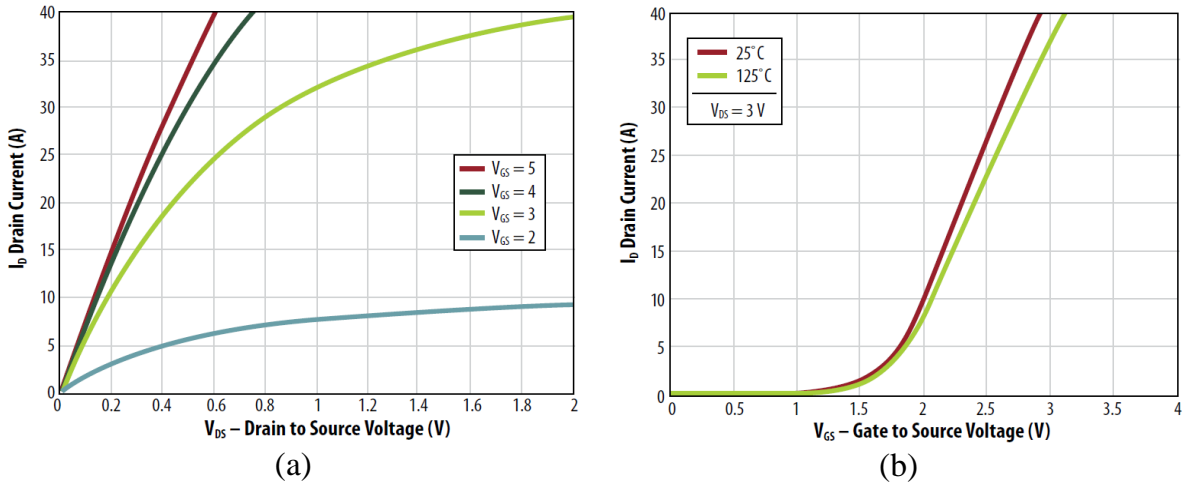


Figure 2.2: (a) $I_D(V_{DS})$, (b) $I_D(V_{GS})$ [98]

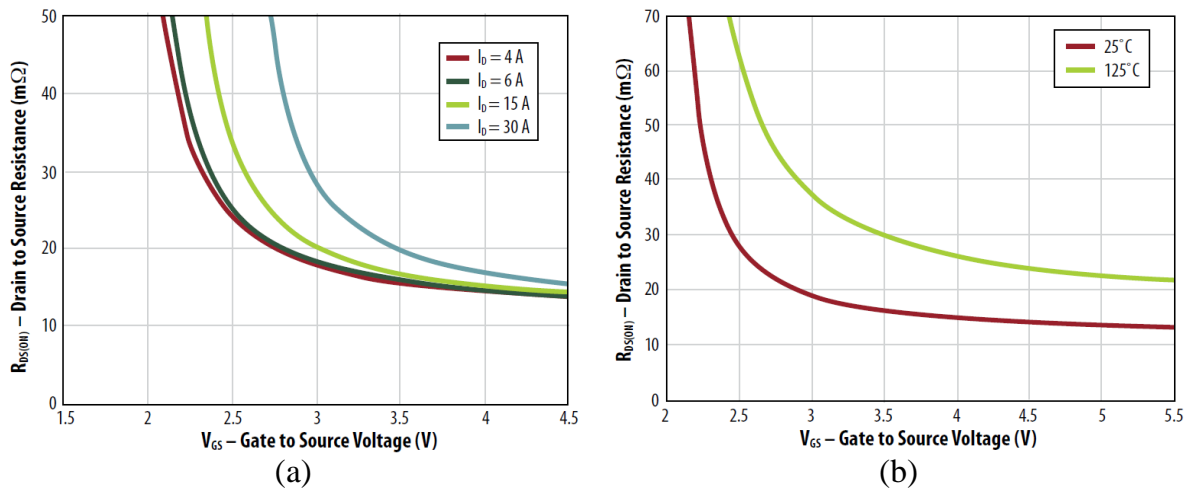


Figure 2.3: (a) $R_{DS(on)}(V_{GS})$ with different I_D , (b) $R_{DS(on)}(V_{GS})$ with different temperature [98]

These GaN transistors can accept a control voltage (V_{GS}) between -5V and 6V. Beyond 6V, the component will be damaged. This value is much lower than that of standard Si power MOSFETs, which is 20V. Texas Instruments propose a control circuit dedicated to the e-mode GaN transistors. This control circuit (LM5113), shown in Figure 2.4, allows to drive both the high-side and low-side devices in a half bridge configuration. The high-side bias voltage is generated using a bootstrap circuit and is internally clamped at 5.2V, which prevents the gate voltage from exceeding the maximum gate-source voltage rating of enhancement mode GaN FETs. The input of the LM5113 are TTL logic compatible, and can withstand input voltages up to 14V regardless of its supply voltage.

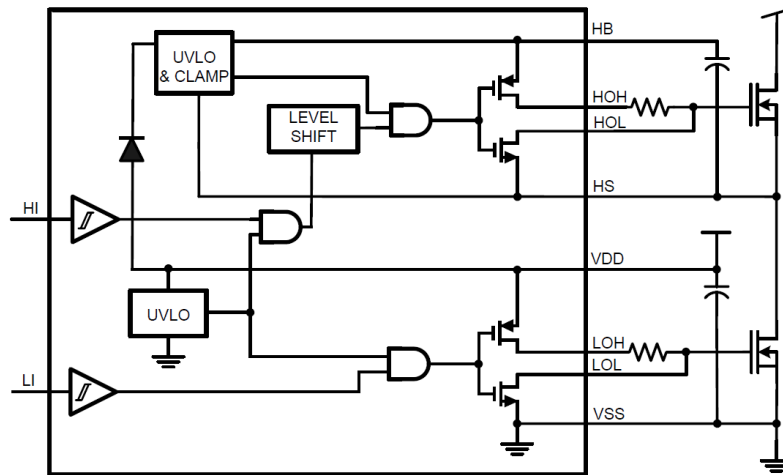


Figure 2.4: LM5113 control circuit [99]

The circuit layout is crucial to the optimum performance, TI gives the following considerations for using the LM5113 [99]:

- “The first priority is to confine the high peak currents that charge and discharge the GaN FETs gate into a minimal physical area. This will decrease the loop inductance. Therefore, the GaN FETS should be placed close enough to the driver.”
- “The high current path includes the bootstrap capacitor, the local ground reference VDD bypass capacitor and low-side GaN FET. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area is important.”
- “The parasitic inductance in series with the source of the high-side FET and low-side FET can impose excessive negative voltage transients on the driver. It is recommended to connect HS pin and VSS pin to the respective source of the high-side and low-side transistors with a short and low-inductance path.”
- “To prevent excessive ringing on the input power bus, good decoupling practices are required by placing low ESR ceramic capacitors adjacent to the GaN FETs.”

According to these considerations, a proposed layout for a half bridge converter is shown in Figure 2.5.

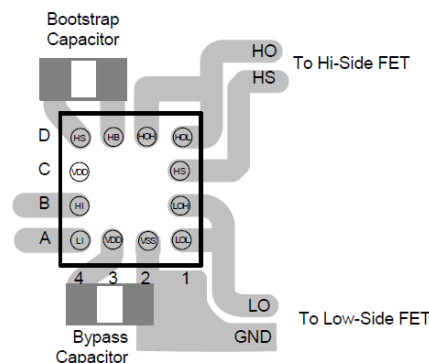


Figure 2.5: Proposed layout for LM5113 [99]

2.2.2 Thermal and electrical issues of package

As the EPC GaN transistors are lateral devices, all terminals (solder bumps) are located on the same side of the die. This is efficient from an electrical point of view, with very short distances between the active area of the GaN transistor and the other components of the converter. From a thermal point of view, however, this is not so efficient: the bumps have limited thermal conductivity, and cover only a fraction of the die surface area. Therefore, before realizing the final module, it is worth firstly comparing the thermal performance of GaN transistors cooled either through their bumps (topside cooling) or through their silicon substrate (backside cooling) to choose the better solution.

Another important element to improve the thermal performance is to choose an appropriate substrate. In fact, to enable the high switching speed available from the eGaN FETs, the PCB substrate is usually be used for its low inductance interconnect (in the case of multilayer PCBs). However, this substrate is usually dedicated to small power application and it has poor thermal conductivity. A widely used substrate in power electronics domain is the ceramic substrates (especially DBC, for Direct Bonded Copper), which are preferred for medium to large power packages (from kW to MW). In particular, alumina (Al_2O_3) is commonly used and offers thermal conductivities of 24 to 33 W/mK. The dielectric strength of ceramic is lower (from 10 to 15 kV/mm) than that of typical epoxy-based FR4 PCBs (54kV/mm). Therefore, PCBs may be thinner than alumina substrates for the same insulation rating. From a thermal point-of-view, however, the possible difference in thickness is not sufficient to make up for the difference in thermal conductivity. Thermal vias are often used to reduce the thermal resistance of PCBs, but they are electrically conducting.

Three functioning prototype designs are fabricated to compare the cooling solutions for GaN transistors. Their cross-section structures are shown in Figure 2.6. In the first configuration (prototype I), GaN transistors were flip-chip-mounted on a DBC substrate with an alumina layer of 635 μm . A special etching technique was used to achieve the high resolution (200 μm pitch) required to mount the transistors. In the second configuration (prototype II), the backside of the transistors was attached to the DBC substrate. This required grinding down the silicon substrate of the transistors, to reduce their thickness and to remove the marking. A Ti/Ag layer was deposited on the silicon substrate, and the dies were attached to the DBC substrate using silver sintering. A flex substrate is used on the topside for the electrical interconnects. The third configuration (prototype III) is the classical flip-chip mounting on PCB (albeit on a much thinner PCB than usual, to improve its thermal performance), used as a basis for comparison. The three prototypes are shown in Figure 2.7.

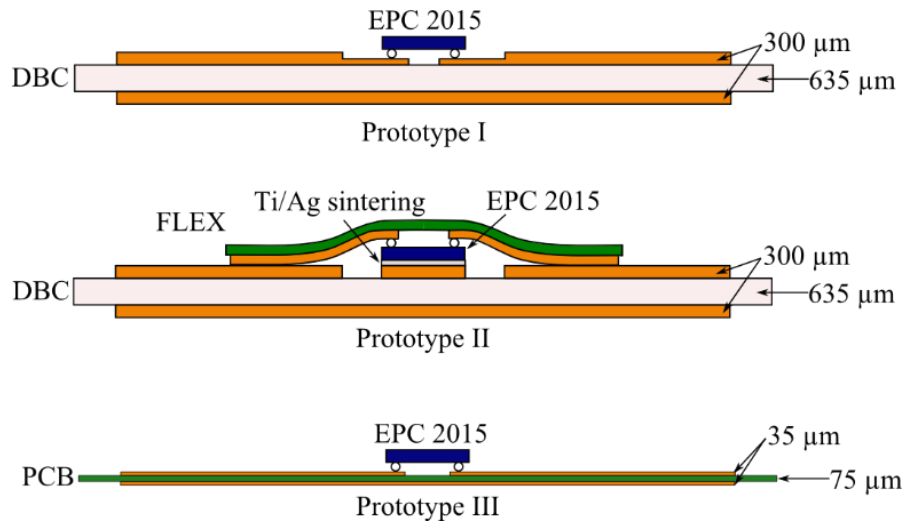


Figure 2.6: Cross-section of the three prototypes

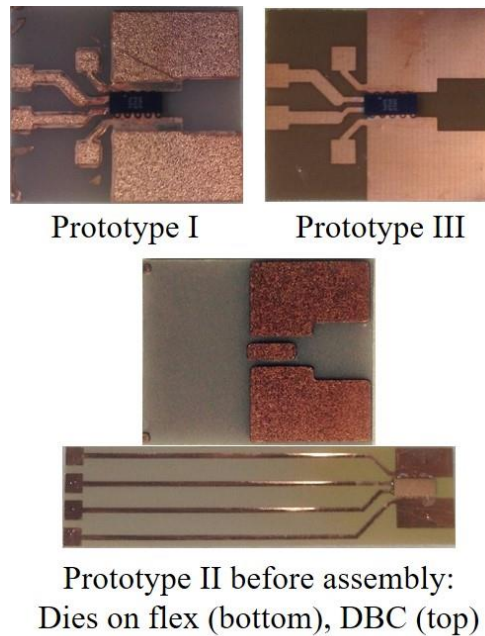


Figure 2.7: Photographs of the three prototypes

2.3 Fabrication process

This section will firstly present some common steps in the fabrication process of all prototypes. Then, the techniques that are specific to each prototype will be introduced in the following paragraphs.

2.3.1 DBC preparation

Different steps are required to produce the final substrate. The global process is illustrated in Figure 2.8 (details regarding the individual steps are given in the next sections).

- Step 1: As the available equipment does not allow the treatment of samples more than 7.62 cm in diagonal, standard plain DBC mastercards (Rogers Curamik, 190 ×

130 mm²), are cut into 50 × 50 mm² parts (called “substrates” in the rest of the process flow description). The cutting is performed on a cut-off saw (Struers Secotom 10), equipped with a diamond blade (150 mm diameter) adapted to the ceramic material, with a rotation speed of 3000 tr/min and a forward speed of 0.5 mm/s. The substrates are then cleaned for the following steps.

- Step 2: A photolithography is realized on the substrates:
 - A photoresist (Microchemicals Dip Coating) is applied on the substrate, by dip coating.
 - Exposure: The two sides of the substrate are exposed to ultraviolet (UV) through a first mask set.
 - Development: The substrate is then dipped in a developer. The photoresist area that were exposed to the UV are dissolved (positive resin).
- Step 3: The substrate is etched in ferric chloride, using a spray system (Bernier Electronik PR2030). In some cases (as for prototype I), the objective is to remove only 250 μm out of the 300 μm thick copper layer in the places which are not protected with the resin. This etching steps takes approximately 15 minutes (each duration depends on the activity of the ferric chloride solution). For the other prototypes, the exposed copper is etched all the way down to the ceramic. The substrate is cleaned again after the etching.

This list show a general process of the preparation of DBC substrate, some steps will be detailed in the following paragraphs.

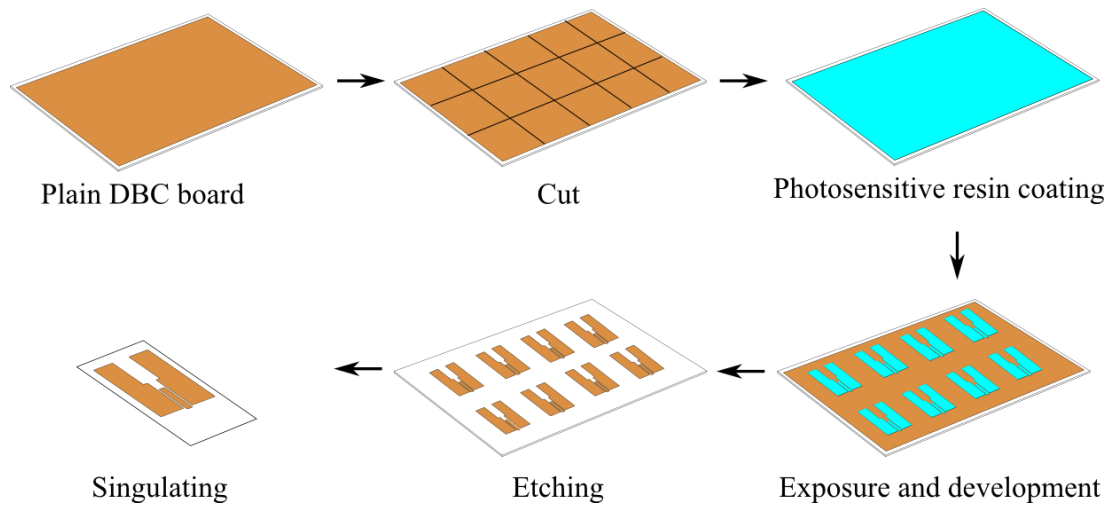


Figure 2.8: Fabrication process of DBC

2.3.1.1 Substrate cleaning

Cleaning is a fundamental step of the process. Before covering the substrate by resin or photosensitive film, it is very important to ensure that the substrate is clean enough. In fact, a dirty substrate will yield a poor coating by the resin. The particles or the residues left on the surface may create small holes in the deposited layer.

Therefore the substrate must be cleaned at least twice during the fabrication process: once between steps 1 and 2, and a second time at the end of the process before the chip soldering.

The substrate cleaning process is constituted of six steps described below:

- 2 minutes in 30 mL of acetone for removing the lubricants and the grease from the substrate. This bath can also be used to remove the photoresist present on the substrate after copper etching.
- 2 minutes in 30 mL of ethanol to eliminate the residues left by the acetone.
- Rinsing with deionized water before dipping in the acid.
- 2 minutes in 30 mL 10% hydrochloric acid in order to deoxidize the copper of the substrate.
- Rinsing with deionized water to remove all the acid trace of the substrate.
- 2 minutes in 30 mL of ethanol which allows a better drying of the substrate because the ethanol is more volatile than the water.
- Drying with nitrogen

The solvents (acetone and ethanol) are placed in a heating ultrasonic bath during the whole process. The heat and the vibration created by the ultrasound allow to remove some recalcitrant traces rapidly.

2.3.1.2 Photolithography

Photoresist application of substrate

This first step is realized with the “MC Dip Coating” liquid photoresist from Microchemicals. It is deposited on a DBC substrate by a custom-built “dip coater” designed in Ampere laboratory [100]. Its photo and main function are illustrated in Figure 2.9. The substrate, maintained by a crocodile clip, is dipped into a beaker containing the resin, and then is extracted with a controlled and constant speed. According to the documentation, it is recommended to deposit this resin with a speed between 5 mm/s and 8 mm/s in order to get a homogeneous layer. Previous tests shown that good results were achieved for a speed of 6 mm/s for the input and the extraction speed. Once the extraction finished and the machine stopped, the substrate is kept motionless for 1 minute and 30 second to allow the resin to smooth. After this pause, the substrate is dried at 100 °C in an oven (UNB 100 Figure 2.10) for 5 minutes.

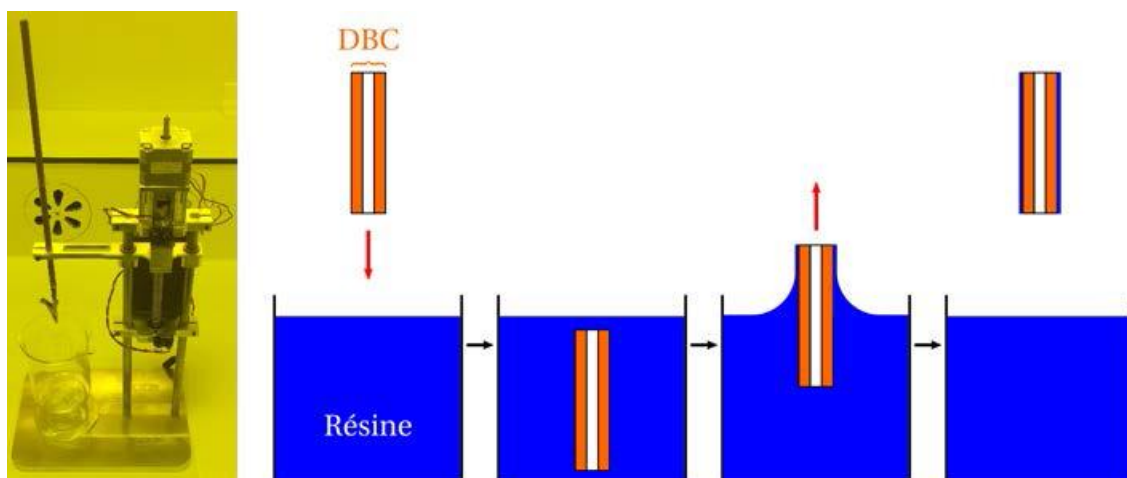


Figure 2.9: Photography of the dip coater, and principle of operation [100]



Figure 2.10 : UNB 100 Universal Oven used for “dip coating” [101]

Exposure

The exposure is the second step of the photolithography. It consists in exposing some areas of a photosensitive product, to an ultraviolet radiation of wave length $\lambda = 365 \mu\text{m}$. The pattern to form is defined by a plastic mask. The exposition generates chemical modifications in the irradiated zone. The solubility of this zone changes according to the type of product used, for creating a latent image:

- Positive: the exposed areas become more soluble and are eliminated by the developer. It is the case of the resin used here (Microchemicals MC Dip Coating). The non-exposed areas remain.
- Negative: The exposed areas become less soluble and resist to the developer, which removes the non-exposed areas.

The insolation is realized by a mask aligner Q-2001 CT (Quintel Corporation) (shown in Figure 2.11). For a positive photoresist, as used here, the mask is designed to that the patterns we want to form in the resin are black on the mask and the areas where the resin will be eliminated are transparent on the mask.



Figure 2.11 : Mask aligner Q-2001 CT

In this step, the fundamental parameter to set is the exposition time to ultraviolet radiation. A bad exposition (much longer or much shorter than required) creates problems during the development. In order to avoid these issues, it is necessary to define the exposition time for the photosensitive product utilized. A previous test shows the best result with our setup is 90 s.

Development

The development is the last operation of photolithography. As mentioned previously, in this step, the exposed substrate is dipped in a suitable developer, to dissolve the non-exposed areas of the photoresist. The developer (ma-D 331, micro resist technology) is used to develop the MC Dip coating resin. The substrate is dipped in 30 mL developer for 1 minute and 30 seconds.

2.3.2 Reflow Soldering

The LGA package reduces die size and improves electric performance but introduces mounting challenges. The EPC GaN package utilizes an interleaved structure, with an alternance of drain and source connections. The pad pitch is 400 μm , with 200 μm spacing between pads. Consequently, the manufacturers recommends a reflow process for mounting this kind of device (as opposed to hand soldering). Furthermore, as the LGA package must be mounted in a “flip chip” fashion, an alignment system is required to position it accurately over the copper pattern. The soldering machine we use is shown in Figure 2.12. This machine can ensure proper alignment between dies and substrate. In order to guarantee the adhesion of component and to avoid the local oxidation of the copper, some tacky flux is dropped on the chip contact area just before the component placement. A thermocouple (TC) is been attached near the component to measure the actual substrate temperature in real time. The solder reflow profile for DBC and PCB is shown in Figure 2.13 (a) and (b). Top Heater and Bottom Heater correspond to the temperature of the heating elements of the soldering equipment (ZEVAC ONYX 21) shown in Figure 2.12. The TC corresponds to the actual thermocouple measurement on the substrate. Due to its superior thermal performance, the DBC substrate require much more energy to achieve the reflow temperature (TC = 250°C). This machine also allows to remove the components, for repair operations.



Figure 2.12: ZEVAC ONYX 21 Flip-chip bonder [102]

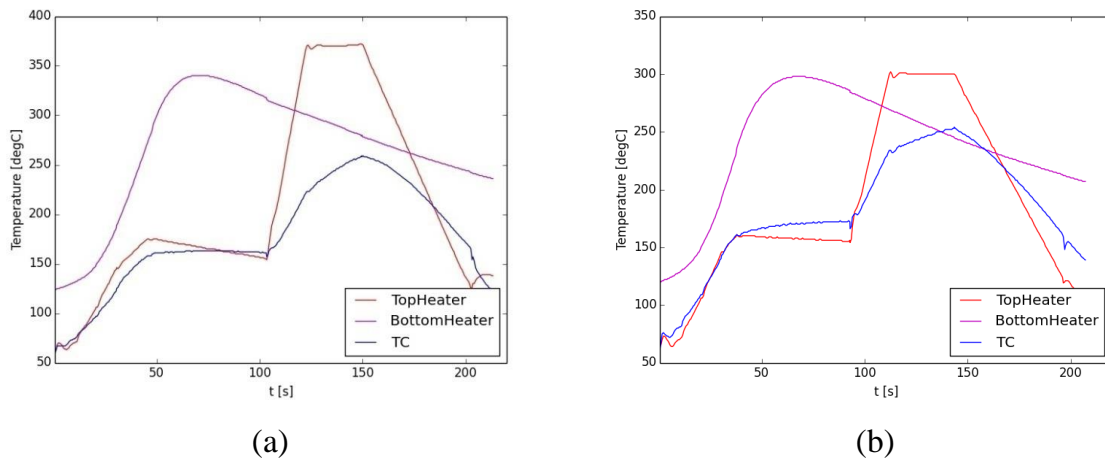


Figure 2.13: Reflow soldering process for DBC (a) and PCB (b). The substrate temperature (TC) is first brought between 160 and 170°C (pre-heating) and then above the liquidus of the solder bumps (217°C) for a short time (1 min), for the actual soldering.

2.3.3 Prototype I: Flip-chip with DBC

For this prototype, a dual-step etching of DBC is required. This allows for using thick copper on most of the surface (for low electric resistance) while having thin copper (high resolution) around the GaN die. Indeed, the spacing between the bumps of the LGA package is 200 μm only, while the copper thickness of the DBC used here is 300 μm . Achieving a sufficiently high aspect ratio (i.e. achieving sufficiently vertical copper edges) would be impossible with the standard etching technique. To reduce the thickness of the copper layer down to 50 μm around the LGA locations eases the requirements, it becomes easier to ensure a proper separation between the tracks.

In order to realize the double etching, two masks have been designed (shown in Figure 2.14). The first mask is used to protect only the areas where the copper retains its full thickness (300 μm). The second mask protects both the thick and thin copper areas (the thin areas are the places where the LGA packages are to be mounted). The etching time is 11m30s for the first step. This removes approximately 250 μm out of the 300 μm thick copper layer. A presentation of this process is shown in Figure 2.15. After cleaning, a new resin coat is applied, exposed (using the second mask), and developed. The second etching only lasts 2m30s, enough to remove the remaining 50 μm of copper where needed and reach the ceramic. The etching result is shown in Figure 2.16. Once the substrates are etched and cleaned, GaN transistors are soldered.

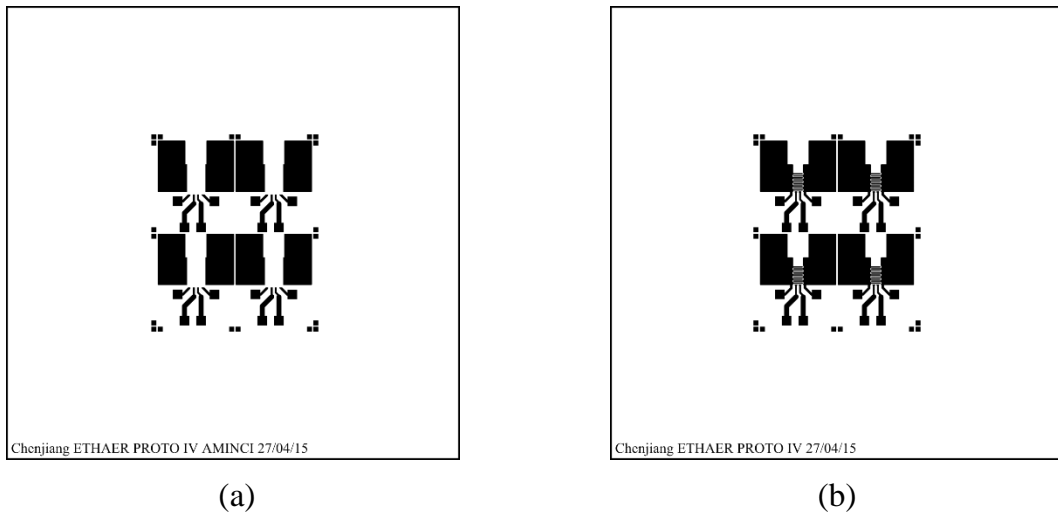


Figure 2.14: (a) First mask for dual-step etching, (b) Second mask

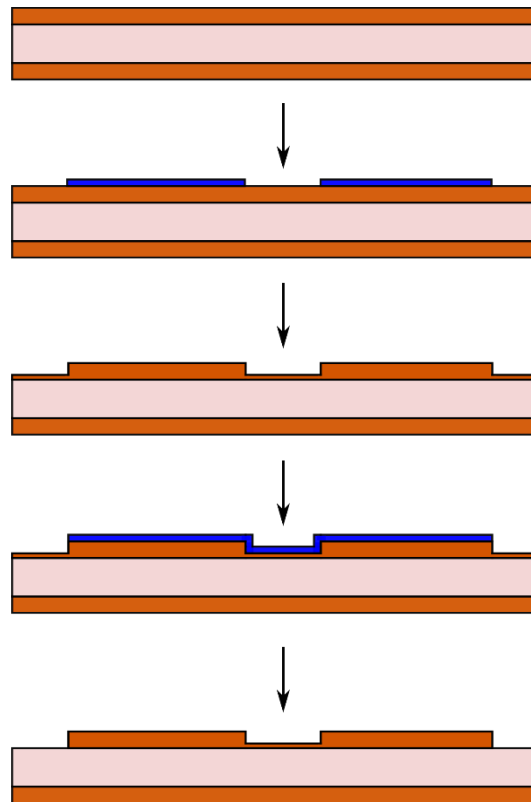


Figure 2.15: Fabrication process for dual-step etching

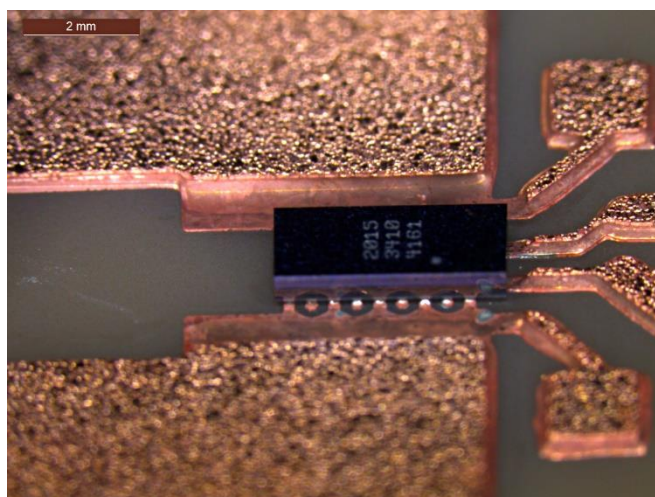


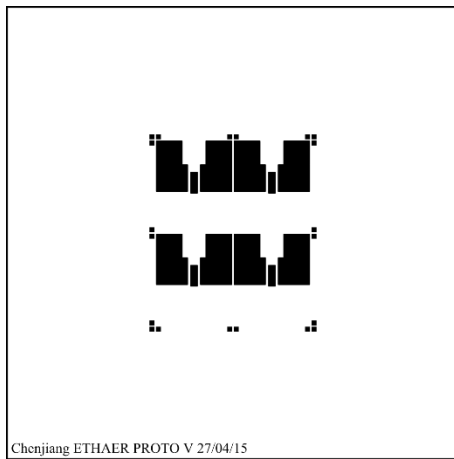
Figure 2.16: Dual-step etching result

2.3.4 Prototype II: “Flip flip” chip on DBC

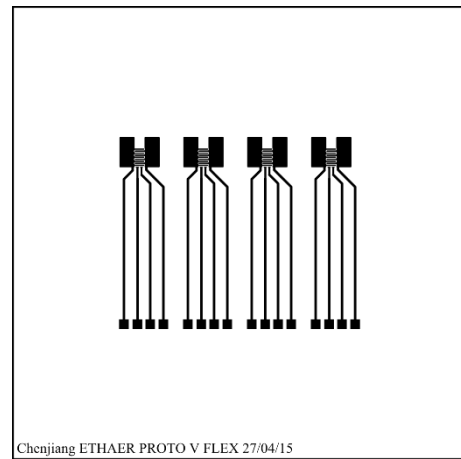
The standard mounting of the EPC transistors is called “flip-chip”, as the devices are turned downwards, so their bumps touch the DBC substrate. Here, we flip them once again so that the silicon substrate touches the DBC, hence the name “flip-flip-chip”. The realization of the “flip flip” chip prototype can be divided into two parts, the soldering of the components to a flex substrate (required to provide interconnects to the transistors) and the sintering of the components/flex assembly to the DBC substrate.

The first part begins with the grinding down of the silicon substrate of the GaN transistors. This is necessary to remove the marking at the back of the die, and to reduce the thermal resistance of the device by making the silicon substrate thinner. The components are first bonded on a sample holder (Struers' AccuStop) shown in Figure 2.18(b) by utilizing some mounting wax (Buehler crystalbond). Then, the holder is put on a polishing machine (MECATECH 334) shown in Figure 2.18(a) with a P1200-grade grit paper. An example of polishing result for EPC2015 is shown in Figure 2.19. The next step is to metallize the backside of the polished part. This is done in an EVA300 PVD system. 50 nm Ti and 150 nm Ag are deposited by evaporation. Afterwards, the chips are soldered to the flex substrate by using process described in section 2.3.2, the mask for flex substrate is shown in Figure 2.17(b).

The second part uses silver sintering technology at low temperature and low pressure. This technology was selected because it offers excellent electrical and thermal conductivity compared traditional solders. Also, this process can be performed at 200 °C, which prevents the melting of the bumps of the GaN devices (their melting point is 217°C). The DBC substrate is firstly etched (single step etching, as there is no need for high resolution here) with the mask shown in Figure 2.17(a). Then, the selected Ag paste (NBE Tech Nanotach-X) is applied on the DBC by screen printing. Following this, the soldered GaN transistors and flex substrate are placed onto the paste. Finally, the DBC substrate is subjected to a heated mechanical press, where the silver sinter layer is formed. The total process can be seen in Figure 2.20.



(a)

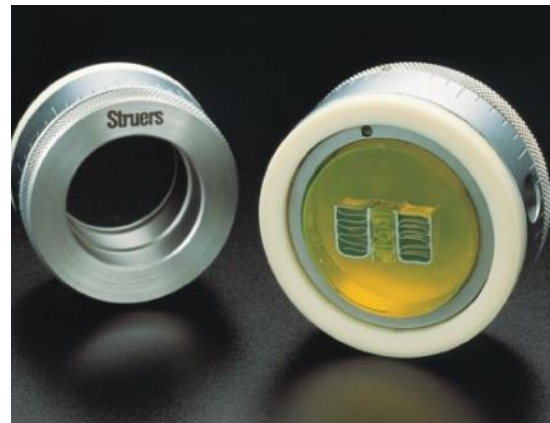


(b)

Figure 2.17: (a) Mask for DBC etching, (b) Mask for flex substrate etching



(a)



(b)

Figure 2.18: (a) MECATECH 334 polishing machine [103], (b) Struers' AccuStop sample holder [104]

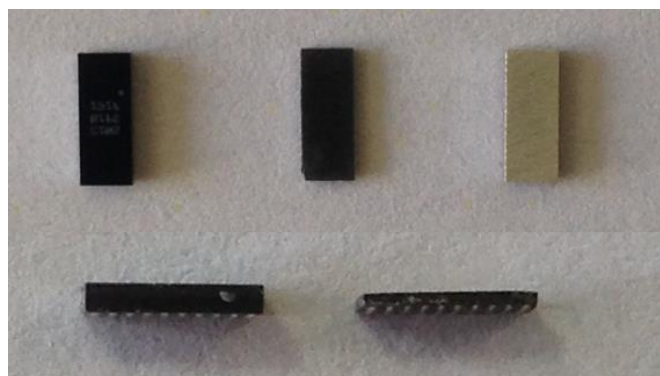


Figure 2.19: Polished GaN transistors. Top line: top view of the devices before grinding, after grinding, and after Ti/Ag PVD plating. Bottom line: side view of the devices before and after grinding. Original device size is $4075 \times 1602 \times 685 \mu\text{m}$.

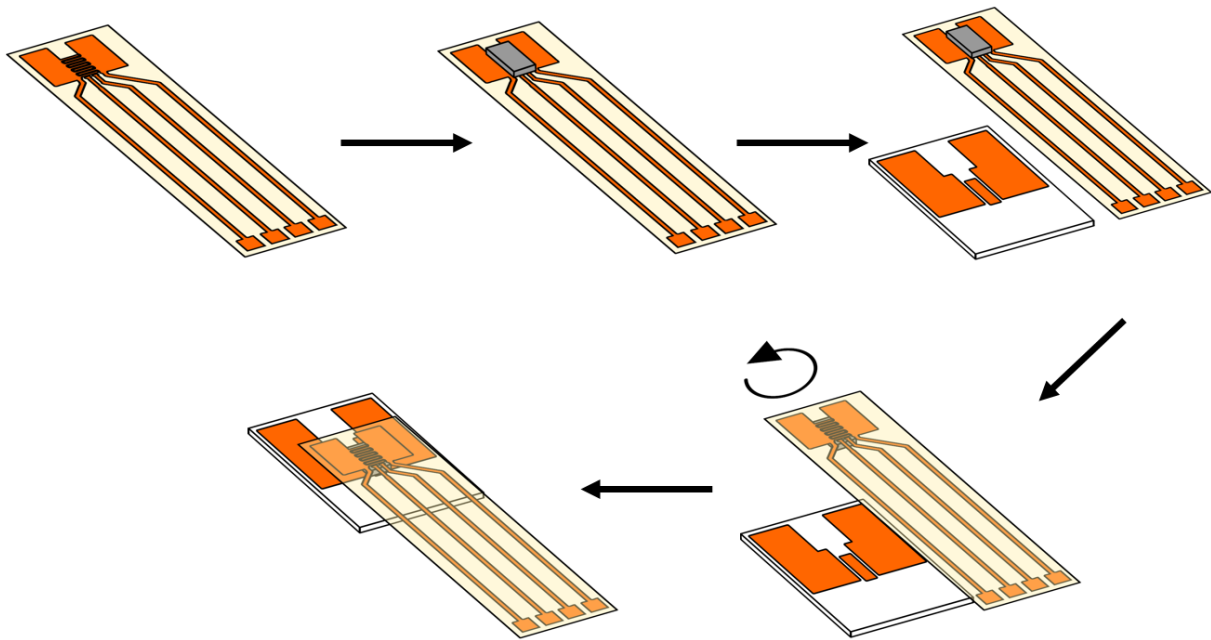


Figure 2.20: Fabrication process for flip flip-chip prototype

2.3.5 Prototype III: Flip-chip on PCB

The fabrication process of this prototype is nearly the same as the one with DBC, but without the second etching. The PCB substrate is fabricated by using a heating press with only one prepreg layer and two copper layers on both sides. This results in a very thin (and therefore more thermally efficient) substrate (laminated thickness: approximately $70\ \mu\text{m}$). The detailed process for PCB manufacturing will be presented in the next chapter.

2.3.6 Conclusion

In this section, the fabrication process for each GaN prototype was presented, including the DBC etching, reflow soldering. In particular, two new processes have been introduced: the “dual step” etching of copper, to allow the mounting of fine pitch devices, and the “flip-flip” configuration, for the backside cooling of the devices. All prototype have comparable layout and size, and in all cases, the objective was to have the lowest thermal resistance (either by using a ceramic material (Al_2O_3 or AlN), or by having as little laminate material as possible (in the case of the FR4). In the next sections, these prototypes are compared from a thermal and electrical point of view.

2.4 Thermal analysis

A power electronic device is sensitive to its junction temperature. When the junction temperature exceeds the functional limit, the device cannot operate in a normal way. It is also well known that the failure rates of semiconductor chip increases exponentially as the junction temperature rises [105]. Even when operating in their Safe Operating Area, some devices (as it is the case with the GaN transistor under investigation) tend to have better performances at low temperatures. As a consequence, the thermal management of the semiconductor devices is a key element of a design. Power dissipation during operation of

the power module induces an increase of the junction temperature. The temperature raise depends on the amount of power dissipation and on the thermal resistance from junction to case and from case to substrate and from this to ambient. This section presents the thermal management we investigate for the prototypes. It begins with a recall of the different types of thermal transfer. Then, the thermal data obtained by Finite Element Method (FEM) will be given and discussed.

2.4.1 Thermal conduction

“The flow of heat from a region of higher temperature to a region of lower temperature within a solid, stationary liquid, or static gaseous medium is termed *conduction heat transfer*, and occurs as a result of direct energy exchange among the molecules. It can be interpreted as a transmission by the thermal agitation. Conduction is described by the Fourier equation, which in one-dimensional form, is expressed as:

$$q = -kA \frac{dT}{dx}$$

Where q is the heat flow (W), k is the thermal conductivity (W/mK), A is the cross-sectional area for heat flow (m²), and dT/dx is the temperature gradient in the direction of heat flow (K/m). [106]”

2.4.2 Thermal convection

“The transfer of heat from a solid to a fluid in motion occurs by a mode termed *convection*. Heat transfer by convection includes two mechanisms: exchange among nearly stationary molecules adjacent to the solid surface, as occurs in heat conduction, and the transport of heat away from the solid surfaces by the bulk motion of the fluid. The relationship that is commonly used to describe convective heat transfer presumes a linear dependence of heat flow on the temperature difference between the surface and fluid, and is referred to as *Newton’s Law of cooling* or :

$$q = hA(T_s - T_f)$$

Where h (W/m²K) is the heat transfer coefficient, A is the exposed surface area, T_s is the surface temperature and T_f is the bulk temperature of the nearby fluid. [106]”

2.4.3 Thermal Radiation

“Radiation heat transfer occurs as a result of the emission and absorption of the energy contained in electromagnetic waves or photons. Thermal radiation can occur across a vacuum or any medium that is transparent to infrared wavelengths. Unlike conduction and convection, radiative heat transfer between two surfaces, or between a surface and its surroundings, is not linearly dependent on the temperature difference. Instead, thermal radiation is governed by the difference between the sources and sink temperatures raised to the fourth power, as:

$$Q = \varepsilon\sigma A(T_1^4 - T_2^4)$$

Where ε is the emissivity, σ is the Stefan-Boltzmann constant, equal to 5.67×10^{-8} W/m²K⁴. [106]”

2.4.4 FEM analysis

Although the junction temperature can be calculated with the equations introduced above, the complex geometry, involving different materials makes it impossible to find an analytical solution. An alternative solution is the use of the Finite Element Method (FEM), using a simulation software, COMSOL Multiphysics. The COMSOL model is established in five steps.

- Step 1 – Describe the structure, and the boundary conditions
- Step 2 – Chose the equation set to be solved (“choosing the physics”)
- Step 3 – Mesh the domain
- Step 4 – Configure the study parameters, and run the calculations
- Step 5 – Analyze the results

The geometry of the model can be described using COMSOL itself, though it’s not an ideal tool for generating complex 3D geometry. Software dedicated to 3D design such as SolidWorks, Autocad or MATLAB can be used. From some specific files format (ODB++, a standard file format for electronic design, which can be generated by many PCB routing software), the designed geometry file can be uploaded in COMSOL. Outside air domains are typically not a part of CAD geometry, but they are required for some FEM analysis. They can be added by creating a sphere which surrounds the CAD geometry. Such air volumes are required for electromagnetic simulations, as the corresponding field extends beyond the boundaries of the prototype. For thermal simulations, we only simulate heat transfer by conduction in the prototype, so we don’t need to describe its environment (no air volume is required).

The last step of generating the structure is the Form Union or Assembly step. According to the document of COMSOL [107], “the Form Union and Form Assembly both merges the geometric objects into a single object. When using Form Union, the software generates a composite object that consists of connected domains separated by shared boundaries between the neighboring entities. When using Form Assembly, the software groups the objects into a single object that contains a collection of disconnected domains. While the default Form Union method results in a connected mesh across the domains, the mesh after Form Assembly is disconnected.” In our case, we need to insure the continuity of electromagnetic field between domains, the Form Union is required in our problem.

2.4.5 Thermal simulation of GaN prototypes

As mentioned in the introduction of this chapter, three GaN prototypes have been designed and assembled. In a similar way, three finite elements models, corresponding to these prototypes, have been built. For each case, the geometry, the boundary conditions and the results will be presented. The aim of this simulation is to evaluate the thermal performance of the three prototypes by a numerical method. These simulations will be validated with experimental measurements.

The geometry of the model is drawn firstly using the SolidWorks software, and then imported in COMSOL. For both configurations (PCB and DBC), we consider that the prototypes are attached on a heatsink through a layer of thermal interface material (TIM). The equations to solve are described in the heat transfer module of COMSOL. This module

includes modeling of all mechanisms involved in heat transfer including conduction, convection, and radiation.

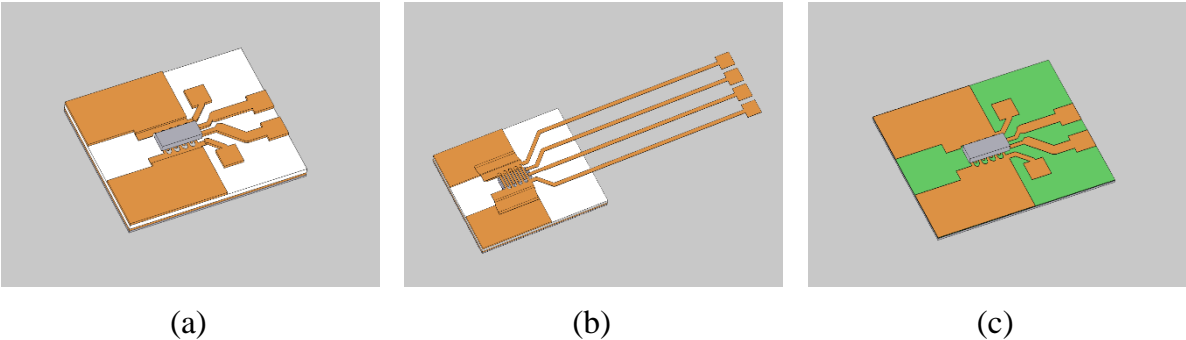


Figure 2.21 : COMSOL geometry of the three prototypes: flip chip on DBC, “flip-flip”-chip on DBC, and flip chip on PCB. All three prototypes are attached to a large heatsink (grey) using a layer of thermal interface material

In the simulations, the power loss for the heat source is set to 10 W, distributed over the surface of the transistor which hosts the solder bumps. This is because in a GaN transistor, most of the heat is dissipated in the GaN layer. The silicon substrate only has a mechanical function. An equivalent heat-transfer coefficient of 8 W/(m² K) [106] is used to define the interaction between the outer surfaces of the components and the substrate with ambient air. This heat transfer coefficient value corresponds to a heat exchange using natural convection in air. In the simulation, the bottom surface of the heatsink and ambient air temperature are assumed as the reference temperature equal to 27 °C. The materials used in the simulation are listed in Table 2.1, is assumed for all external surfaces of the models.

Table 2.1: Thermal conductivity values used in the simulation

Material	Thermal conductivity (W/m K)	Material	Thermal conductivity (W/m K)
Copper	400 [106]	Prepreg	0.4 [108]
Ceramic	27 [109]	Ag paste	200 [110]
GaN Bumps	62 [21]	TIM	2 [21]
GaN Encapsulation (Si)	130 [106]	Heatsink (Al)	160 [106]

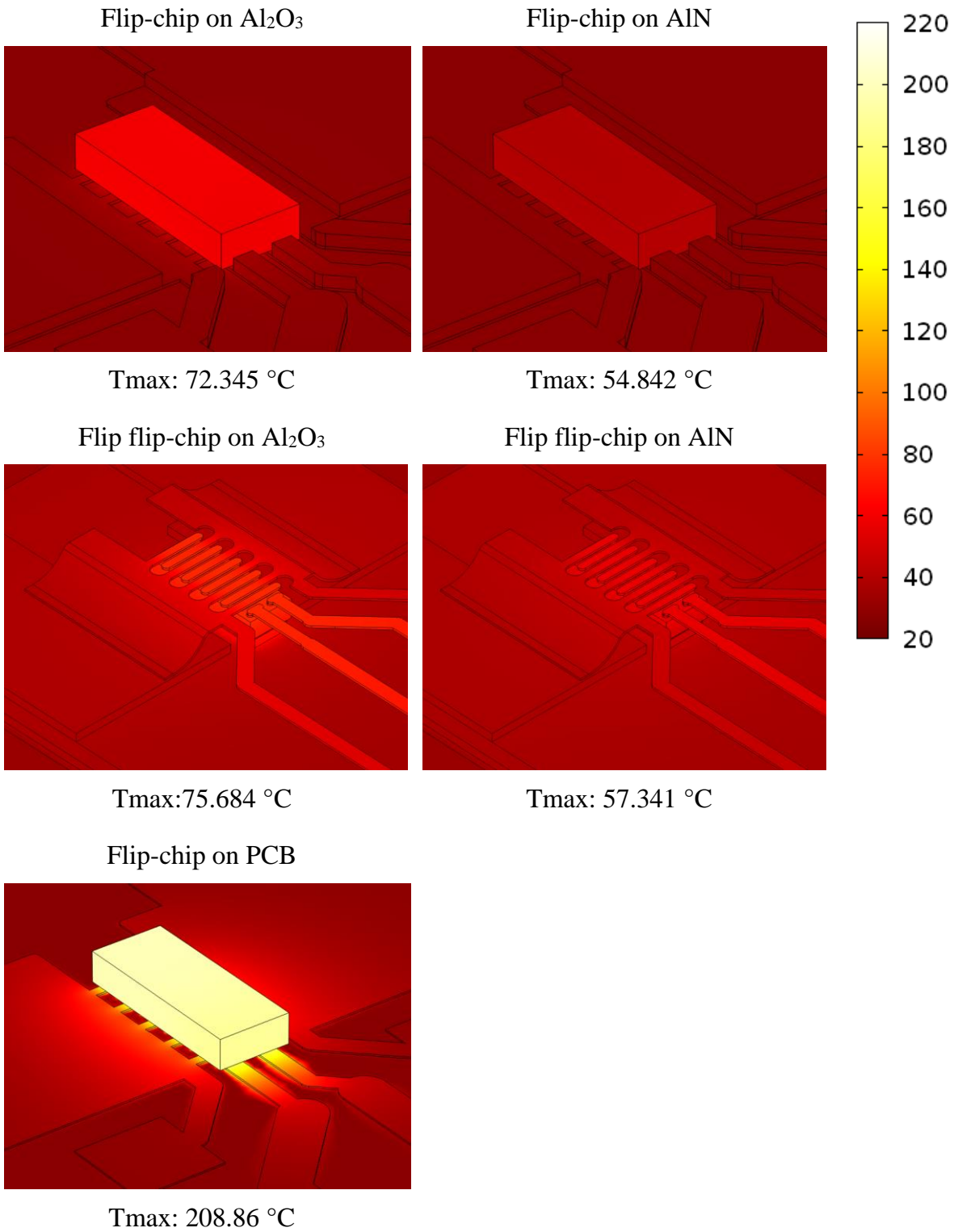


Figure 2.22: Thermal simulation results for GaN prototypes

Table 2.2: Thermal simulation results for DBC and PCB

Prototype	Flip-chip on Al ₂ O ₃	Flip-chip on AlN	Flip flip-chip on Al ₂ O ₃	Flip flip-chip on AlN	Flip-chip on PCB
Thermal conductivity (K/W)	4.5	2.8	4.8	3	18.2

The calculated temperature distributions in the three prototype are show in Figure 2.22. According to these simulation results, the DBC (Al₂O₃ or AlN) has much better thermal performance than the PCB, despite using a much thicker ceramic (635 μm) than the PCB (70 μm of glass-epoxy composite). The thermal resistance of the prototype on PCB is between 4 and 6 times higher than that of any ceramic version.

The ceramic material AlN has better thermal conductivity than Al₂O₃, for this reason, the AlN prototypes have a lower junction temperature than those with Al₂O₃. The “flip-flip-chip” prototypes, where the heat is evacuated through the silicon substrate of the transistor to the DBC, has a little higher thermal resistance compared to the flip-chip prototypes (where the heat flows through the bumps of the transistor). This means that the larger joint area between the die and the substrate (in the case of the “flip-flip” prototypes) is not sufficient to compensate for the longer cooling path: the thermal resistance of the silicon substrate is higher than the thermal resistance of the solder bumps.

2.4.6 Experimental characterizations

Some experimental measurements are also performed to validate the FEM simulation. These measurements aim at characterizing the thermal resistance R_{Th} of the three GaN prototypes, shown in Figure 2.6. Three elements are required to measure the R_{Th} , which are the junction temperature T_j , the ambient temperature T_a , and the dissipated power of the device P . The measurement procedure is to heat the components with a controlled dissipated power until the junction temperature is stable. Figure 2.23 shows the heat flow from junction to ambient, and the relation between these elements is shown below:

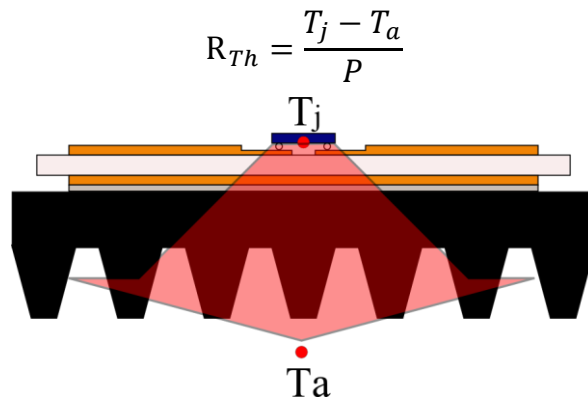


Figure 2.23: Heat flow from junction to ambient

The junction temperature should be monitored during the device operation. In the traditional silicon MOSFETs, there are three temperature sensitive parameters that have been used as indicators of this temperature: the threshold voltage of the body diode, the gate

threshold voltage ($V_{GS(TH)}$) and the on-resistance (R_{DSon}). However, EPC GaN FETS do not have a bipolar junction and the gate threshold voltage is very low. Furthermore, $V_{GS(TH)}$ has little dependence on the junction temperature [111]. Therefore, in this study, R_{DSon} is proposed for the measurement of the junction temperature. R_{DSon} is an excellent indicator because it is actually measuring the heat rise in the exact physical location where the heat is being generated.

In order to calibrate R_{DSon} , a thermal conditioner has been used (Thermonics T2500/E). The calibration curve (Figure 2.24) is acquired using a Tek371 curve tracer in pulsed mode, using a high current (to 30A). Such high current is required because of the very low R_{DSon} of the GaN transistor under study ($4\text{ m}\Omega$). The calibration curve shows that R_{DSon} has a clear dependency on the junction temperature, and is therefore an accurate way of monitoring the junction temperature of a GaN transistor.

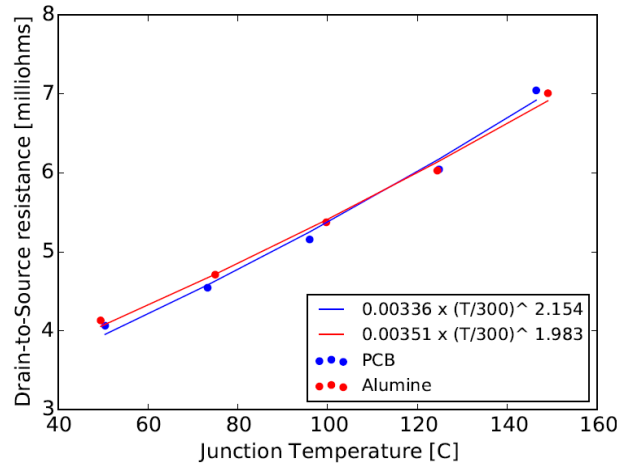


Figure 2.24: Calibration Curve (R_{dson} as a function of T)

For the measurement of the thermal resistance, we used the test circuit in Figure 2.25: the temperature rise in the Device Under Test (DUT) is estimated by monitoring the drain-to-source resistance of the transistor as a large current (up to 40A) flows in the component. When the GaN transistor is in the off-state, the current flows through some silicon Schottky diodes. When the GaN transistor turns on, the voltage drop falls below the threshold voltage of the diodes. Therefore, all the current then flows through the GaN transistor. The resistors R in series with the power supply are used for the stabilization of the current when the GaN transistor switches state. The voltage between Drain and Source (V_{ds}) is measured by a precision voltmeter (Keithley 2010) and the current I_d is measured by a current probe (Tektronix TC-0030). The layout of the prototypes allows a 4-point voltage measurement directly at the terminals of the transistor, to achieve high measurement accuracy. The prototypes are mounted on a $15 \times 15\text{ cm}^2$ heatsink, with a sil-pad interface and are maintained using a clamping system. The temperature of the ambient air is measured with a thermocouple after a 40 minutes stabilization. The test bench is shown in Figure 2.26. Using the measurement data, it is possible to calculate the value of R_{DSon} (V_{DS}/I_D) and the value of the power dissipated by the device ($V_{DS} \times I_D$). The junction temperature can be estimated from the R_{DSon} value by using the calibration data where

$$T_j = \left(\frac{R_{DSon}}{0.00336} \right)^{\frac{1}{2.154}} \times 300 \text{ (for PCB) or } T_j = \left(\frac{R_{DSon}}{0.00351} \right)^{\frac{1}{1.983}} \times 300 \text{ (for Alumina)}$$

The results are presented in Table 2.3. For the PCB prototype, the maximum continuous current achievable is 25 A (above this value, the device enters thermal runaway, as its on-state resistance increases with temperature). For the DBC (Al_2O_3) prototype, the 40 A value listed in Table 2.3 is limited by the test system. As a consequence, although the GaN transistors are designed to be mounted in PCB, it is shown that a ceramic substrate offers a substantial gain regarding thermal management.

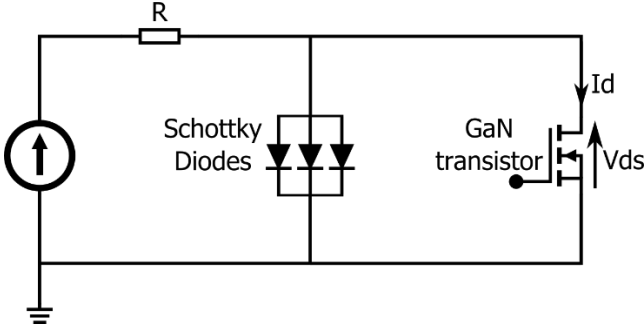


Figure 2.25: Circuit diagram used for the transient thermal characterization

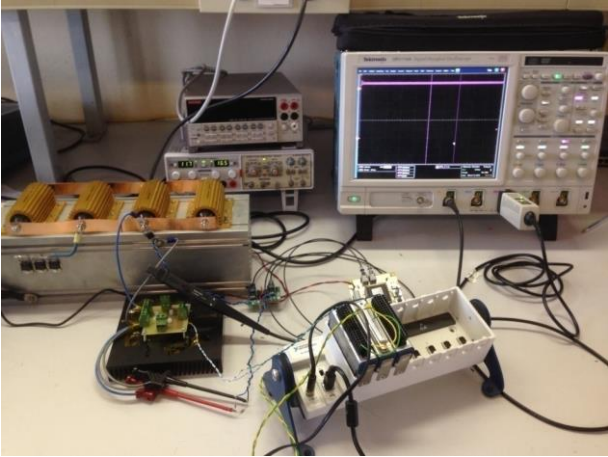


Figure 2.26: Test bench for thermal characterization

Table 2.3: Thermal performance, for PCB and DBC

	I_D (A)	POWER (W)	T_J ($^{\circ}\text{C}$)	R_{Th} (Experimental)	R_{Th} (Simulation)
PCB	25	3.9	125	25 K/W	18 K/W
Al_2O_3	40	7.46	73	6.2 K/W	4.5 K/W

As we can see in the table, the experimental results correspond to the simulation, although they are not the same. Because of the measurement precision, we are not able to find any difference between the Al_2O_3 and AlN materials experimentally. This can be solved by improving the control of the thermal interface (monitoring the pressure), or by using another temperature sensitive parameter with a better measurement sensitivity than R_{DSon} . The measurement of the flip-flip-chip were not successful either. One reason is the insufficient thickness of the copper of the flex substrate which has a large resistance compared to the R_{dson} of the devices, hence making measurement difficult. Another issue is that during the fabrication, the copper tracks of the flex substrate are pressed against the

sharp edges of the GaN transistors, producing open circuits. Initially, the test bench was designed for dynamic characterization (Z_{th}), but the measurement accuracy (using a 16-bit acquisition system NI9205) was found too low to capture the voltage variations between the drain and source terminal of the GaN device (in particular for the short time range, below 1 ms).

2.4.7 Conclusion

In this section, the thermal performance of each GaN prototype was analyzed. We have firstly presented the different heat transfer mechanisms, including conduction, convection and radiation. Then, the FEM study with COMSOL Multiphysics and experimental characterization for these prototypes were presented. The results prove that the ceramic substrate have a much better thermal performance than that of the PCB, with a thermal resistance 4 times lower. This proves that despite their small surface area, the solder bumps are not the main limiting factor regarding the thermal management of these GaN transistors: a large gain can be achieved by selecting a suitable substrate for the circuit. This is confirmed by the “flip flip-chip” prototype, which does not have any advantage compared to the more standard flip-chip mounting: a larger contact between the GaN transistor and the substrate is not sufficient to compensate for the thermal resistance of the silicon substrate of the transistor (even thinned down).

2.5 Electromagnetic and electric study

As introduced in the first chapter, the parasitic elements in a switching cell (shown in Figure 2.27) will generate high switching losses and electromagnetic disturbance. In order to study this issue, this section will analyze the electromagnetic performance of the switching cell, based on FEM simulations, and on an analytical approach. These analysis provides partial impedance values that can be used in a PSpice simulation for a time domain simulation of the device electrical behavior.

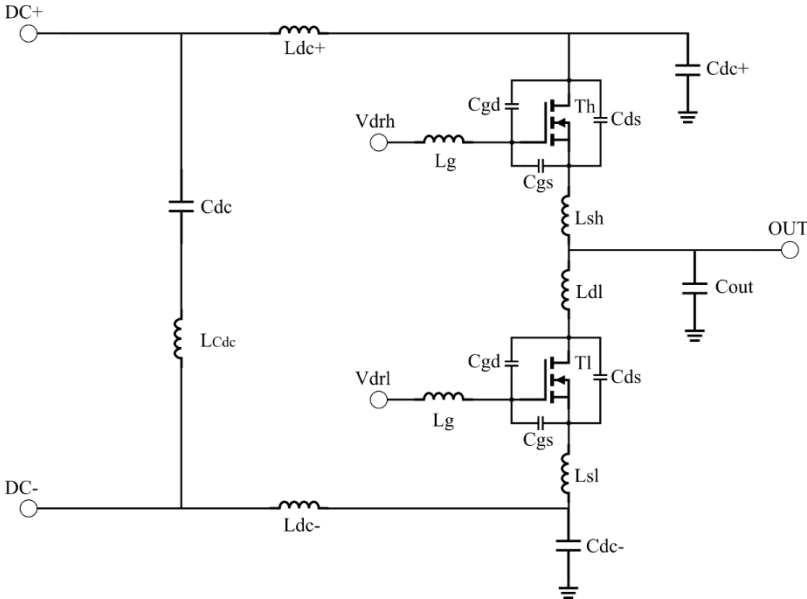


Figure 2.27: Parasitic elements of a switching cell

2.5.1 Half-bridge demonstrator

The half bridge demonstrator for low voltage is composed by two GaN transistors EPC2014 or EPC2015, one TI driver LM5113 with bypass and bootstrap capacitors, and three decoupling capacitors. The ceramic substrate (alumina) is prepared with the dual-step etching technique described above for the areas that receive the GaN transistors and the driver. The layout is designed according to the recommendations of TI for GaN transistors and LM5113 driver [99]. The circuit diagram is shown in Figure 2.28 and an example of the corresponding prototype is illustrated in Figure 2.29.

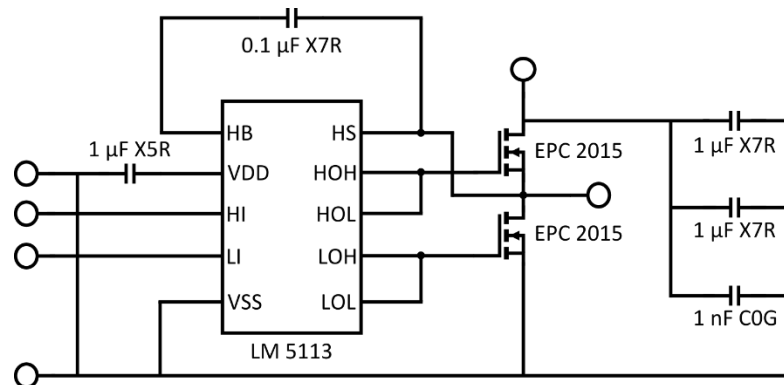


Figure 2.28: Circuit diagram of the half-bridge demonstrator

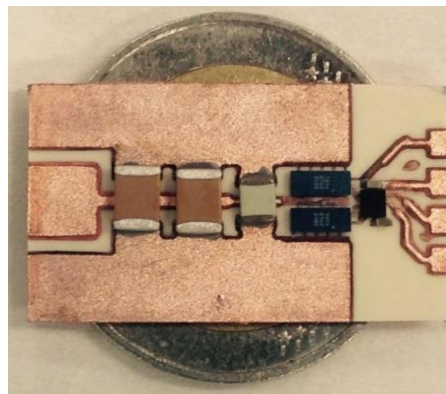


Figure 2.29: Photograph of the half-bridge demonstrator. The TI5113 gate driver is the black square on the right of the substrate (with 4 connecting pads for power supply and driving signals of each transistor).

2.5.2 Electromagnetic analysis

In this section we investigate the consequences of routing the half bridge circuit on DBC, which has a single copper layer that can be patterned. On a PCB, an optimal design would use the first inner layer of a multilayer PCB as a power loop return path. As the current return path is located directly underneath the top power layer, this design leads to a lower loop inductance (from 1 nH down to 0.4 nH when using this inner layer [112]). With a DBC substrate, only one copper layer is available to route the signals, so the input capacitors and transistors must be placed on the same plane and close enough to minimize the size of the power commutation loop. However, there is a second copper layer in the DBC structure. Even though this layer is not available for routing (this layer usually remains

plain), it may contribute to reduce the stray inductances of the circuit. This effect is studied further in this section.

For electromagnetic field modeling, the AC/DC module of COMSOL Multiphysics is used. This module gives the possibility to extract the loop inductance and resistance of an electrical circuit from its geometry. These values are the desired parameters for an electrical simulation. In a FEM analysis, the electromagnetic behavior of a device can only be calculated, if the external electromagnetic energy can be defined. For this purpose, an external air domain must be described. It must be large enough to not disturb the solution, but it must have a reasonable size so as not to increase too much the number of additional unknown elements. To simulate an infinite volume of air while limiting the number of unknowns, we surrounded the air filled with the PML (Perfectly Matched Layer) [113]. This overlays absorb the radiated waves and avoid the reflections. It must be arranged around the air area.

The solution is calculated using the Magnetic Fields (MF) solver in the frequency domain, over the entire system excepting a gap created between two terminals. This void gap is required to define special boundary conditions. On these boundaries, we can define currents or voltages and calculate the equivalent impedance of the circuit.

COMSOL gives the simulation results at different frequencies. At low frequencies, the skin and proximity effects are not very significant. For these simulations, copper domains are fully included in the simulation. A “Single-turn coil” strategy is used and the voltage is imposed at the loop boundaries. For very high frequency, a thin mesh is required, making the problem too complex and no longer computable. The solution is to exclude the copper domain in the FEM simulation. As the currents only flow at the periphery of the conductors, the plain copper traces can be numerically replaced by equivalent boundary conditions, by introducing equivalent surface impedances [114].

Prior to the simulation, the global geometry must be meshed. The steep radial scaling of the infinite elements layer (PML) requires a swept mesh to maintain a reasonably effective element quality. The mesh for this infinite elements layer does not require very fine size. However, due to some small edges in the prototype geometry, the Minimum element size should be set small enough to solve these parts. A very dense mesh was applied especially to the small surface between copper and ceramic. As a consequence, the remaining structures use “Free Tetrahedral” with the size set to “Extra Fine”.

2.5.2.1 Wire bonding prototype

First, in order to validate the good coherence between simulation results and experimental measurements, a prototype with no active devices (only copper tracks and two bond wires) has been fabricated. The fabrication process of this prototype includes etching of the DBC substrate (described in paragraph 2.3.1) and wirebonding with aluminum wires (placed using the TPT30 wirebonder available at 3DPHI). Electromagnetic simulations were performed with COMSOL Multiphysics FEM software.

This test vehicle is shown in Figure 2.30. The objective is to compare simulation and experimental results of self-impedance and mutual inductance.

As it is not easy to draw the wire geometry directly in COMSOL, we have created them with a Matlab script (Annex A) and then imported the generated geometry in COMSOL. The geometry is presented in Figure 2.31, it is composed by two symmetrical parts. Each

part contains two copper areas connected by one bond wire. This prototype allow both, the determination of the impedance of each half part of the DBC and that of the trans-impedance between the two parts. To obtain the self-impedance, only one part of the circuit was fed with a 1V voltage. For the mutual impedance, a voltage of 1V was applied on one circuit, and the second part was set to behave like a load circuit. The simulation results of self-impedance and mutual impedance are presented in Figure 2.34 and Figure 2.35.

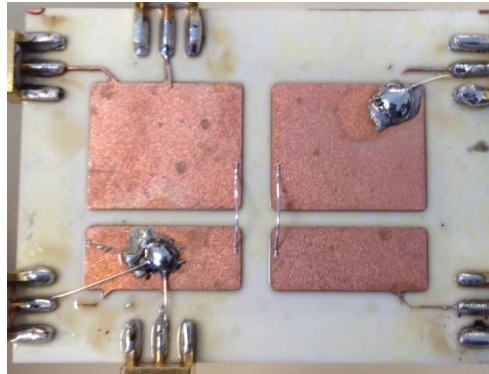


Figure 2.30: Photograph of the prototype used to validate the simulation method. It consists in 4 copper tracks, connected using two bond wires (center of the picture). High frequency SMA connectors are soldered on the edge of the substrate for connection with the test equipment.

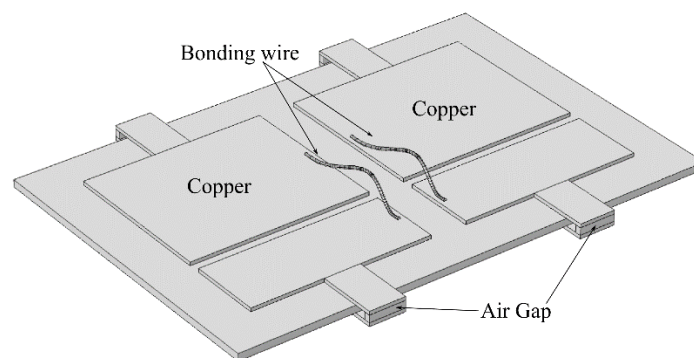


Figure 2.31: COMSOL structure of wire-bonding prototype

Two experimental measurements were performed using a Keysight 4294A impedance analyzer. The first one gives the impedance and argument of Z_{11} which is the self-impedance of each part. The second measurement is the impedance and argument of Z_{21} giving the mutual impedance of the two parts. In order to achieve good accuracy, a 4-wire sensing method was used. Figure 2.33 shows the electrical connections for each measurement. For Z_{11} , a current was applied through terminals J1 and J4, and the voltage measurement was done between J2 and J3. This measurement gives the impedance curve shown in the same figure of the simulation result (Figure 2.34). The Z_{21} impedance was obtained by measuring the voltage between J5 and J6, while the current source remained connected to J1 and J4. The corresponding impedance curve is shown in Figure 2.35.

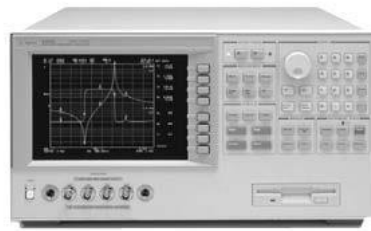


Figure 2.32: Keysight 4294A

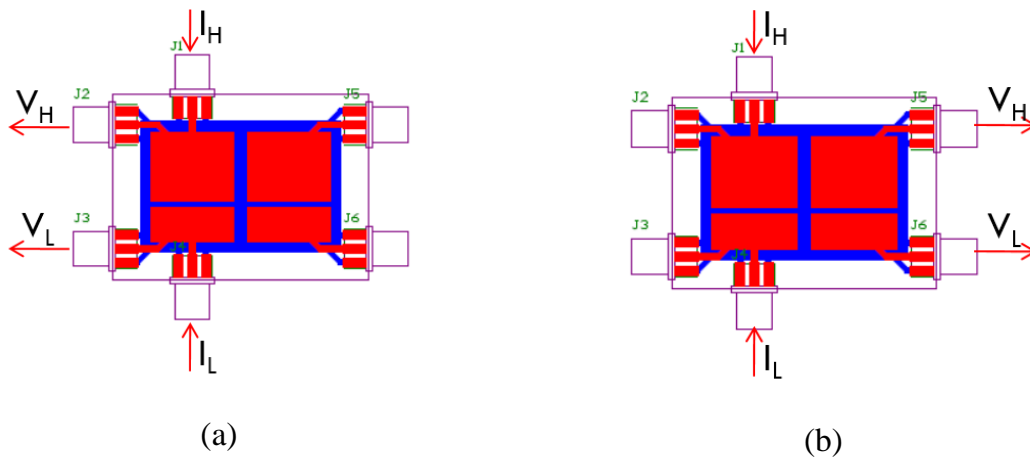


Figure 2.33: Impedance measurement configuration for the wire-bonded DBC prototype

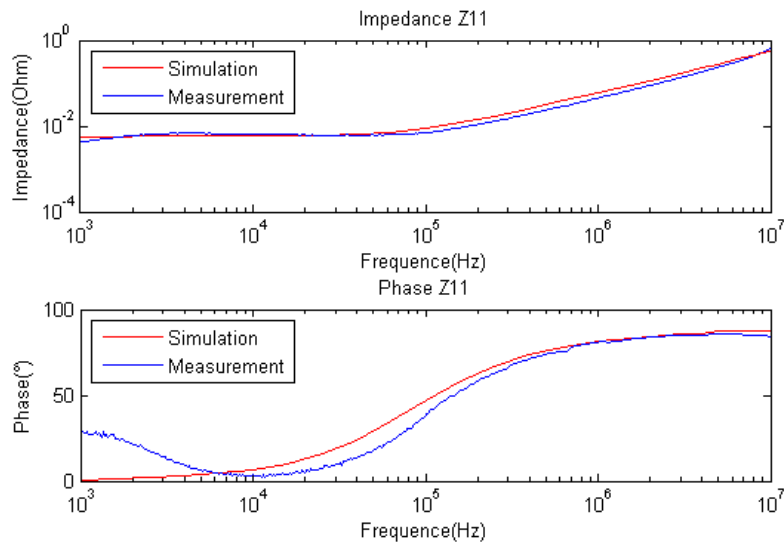


Figure 2.34: FEM simulation and measurement results for Z11 impedance (module and phase)

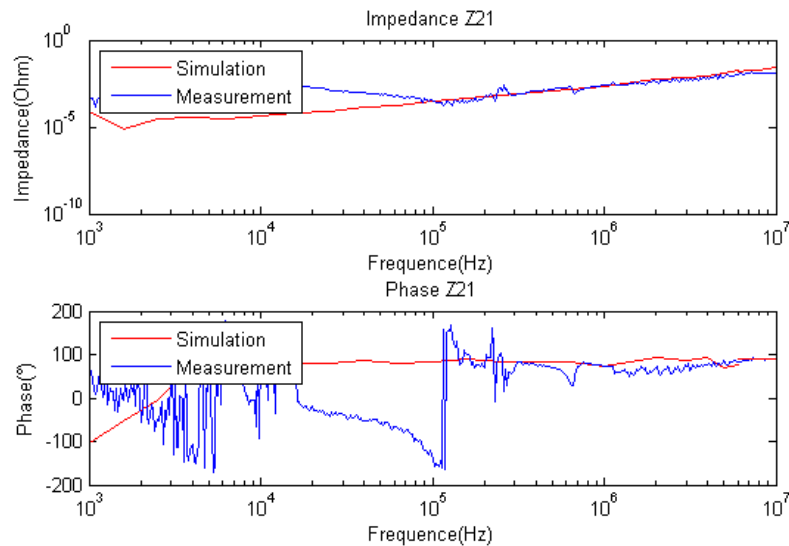


Figure 2.35: FEM simulation and measurement results for Z21 impedance (module and phase)

We can notice the good agreement between simulation and measurement for the self-impedance Z11. The mutual impedance Z21 is very low and actually out of the range of the used impedance analyzer (hence the very noisy measurements in Figure 2.35). Because of insufficient noise margin the measurement cannot be exploited, and one can only say that they are compatible with the simulation results. Nevertheless the good results obtained for the self-impedance Z11, even if this value is very low, validate the use of COMSOL Multiphysics for the electromagnetic study of this thesis.

2.5.2.2 GaN Prototypes

In this section, we consider the half-bridge structure, built with two EPC 2015 transistors and some decoupling capacitors mounted on a DBC substrate.

In this circuit, the high frequency power loop contains the input capacitors, top switch, bottom switch and all the interconnections between these devices. With the significant reduction in stray inductance provided by the LGA package, the layout becomes the major contributor to the loop parasitic inductance, and therefore, to the switching losses and EMI generation. The thickness of the ceramic layer and the bottom metallization layer have significant effect to the total inductance of the circuit, therefore, the first step of this simulation is to study this effect. The FEM simulated geometry is shown in Figure 2.36. In this simulation, the semiconductor devices are replaced by a copper domain. The voltage are applied at two terminals defined at the boundaries of the injection gap.

The layout under investigation is presented in Figure 2.36. Two loops are considered: a “large” loop, where the current flows across the full length of the DC link tracks, and a “short” loop, corresponding to the path of the current supplied by the rightmost DC capacitor. The large loop inductance is used to compare simulation and experimental results (as it results in a larger inductance which is easier to measure), while the short loop corresponds to the high frequency path of current during switching.

Two test vehicles are implemented on a DBC substrate: the first version has a plain layer of copper on its backside, while this layer is removed on the second version. The two

versions are prepared in a similar way, with short circuits replacing the GaN dies. An inductance measurement is performed using the Keysight 4294A impedance analyzer (shown in Figure 2.32). A photograph of one of the DBC substrates with the connections for inductance measurement is given in Figure 2.37.

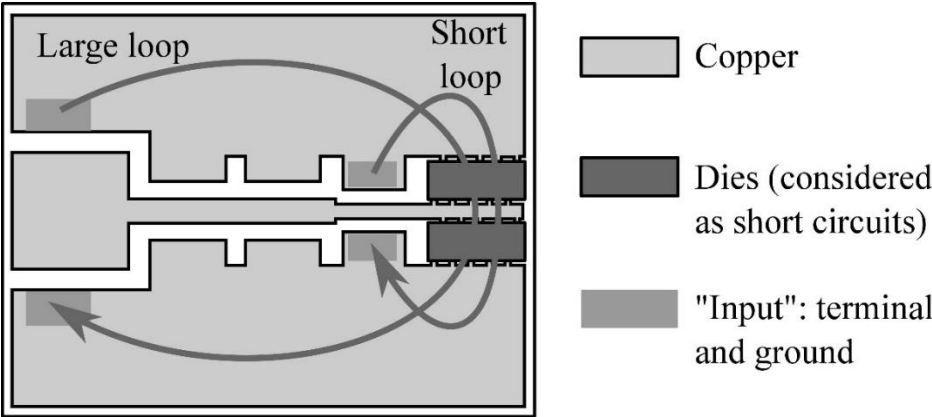


Figure 2.36: Layout of the prototype used for electromagnetic characterization, with the location of the terminal considered for inductance estimation. The upper and lower copper tracks are the + and – DC links, while the middle track is the output of the half-bridge. The three tooth-like patterns on the left of the dies are the locations of the DC decoupling capacitors.

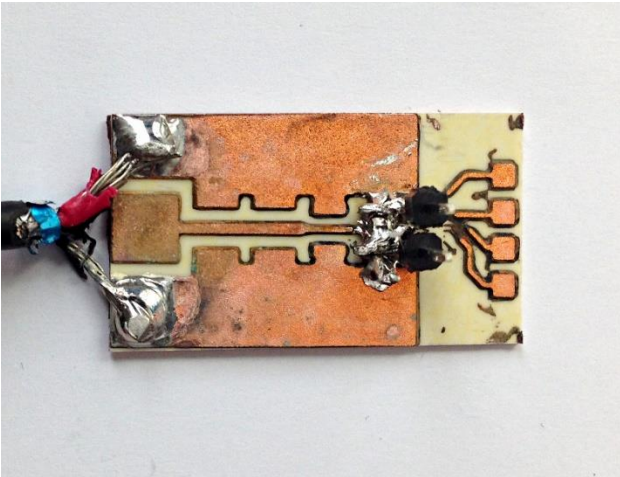


Figure 2.37: Test vehicle for inductance measurement

The FEM model of the two test vehicles is built using COMSOL, the main geometry is imported from a CAD file which is created by Solidworks.

The study is set up to use a frequency domain where the frequency sweeps from 100 kHz to 4 MHz. The comparison between experimental and simulation results presented in Figure 2.38 shows that they are in good agreement. The backside copper layer has a strong effect, as it reduces the inductance by a factor of two, with negligible consequence on the resistance.

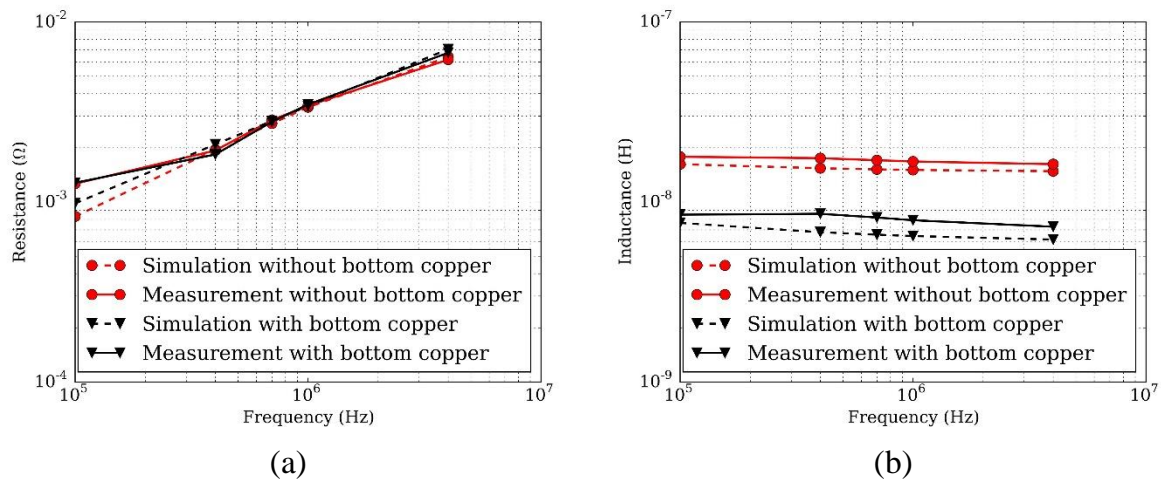


Figure 2.38: Resistance and inductance along the “large loop”, obtained by simulation and measurement, for DBCs with and without backside copper

The simulations are shown for four set of DBC structures: the prototype with different thickness of ceramic layer ($250\ \mu\text{m}$, $380\ \mu\text{m}$, $630\ \mu\text{m}$), and the prototype without the bottom copper layer. The resistance and inductance values are shown in Figure 2.39.

The screening effect offered by the backside copper is related to the insulating material thickness. A simulation study for the “short loop” is presented in Figure 2.39 and shows that the inductance increases with the ceramic thickness. This is because the mutual inductance between the top and bottom copper layers decreases when the ceramic thickness increases. According to the mirror image method, the total inductance equals to the difference between the self-inductance of the top side circuit and the mutual inductance. As a consequence, the total inductance is larger when the ceramic layer is thicker. For a ceramic layer of $250\ \mu\text{m}$, inductances of less than 2nH are achievable. This is still much more than an optimized PCB [112], but this value is low enough.

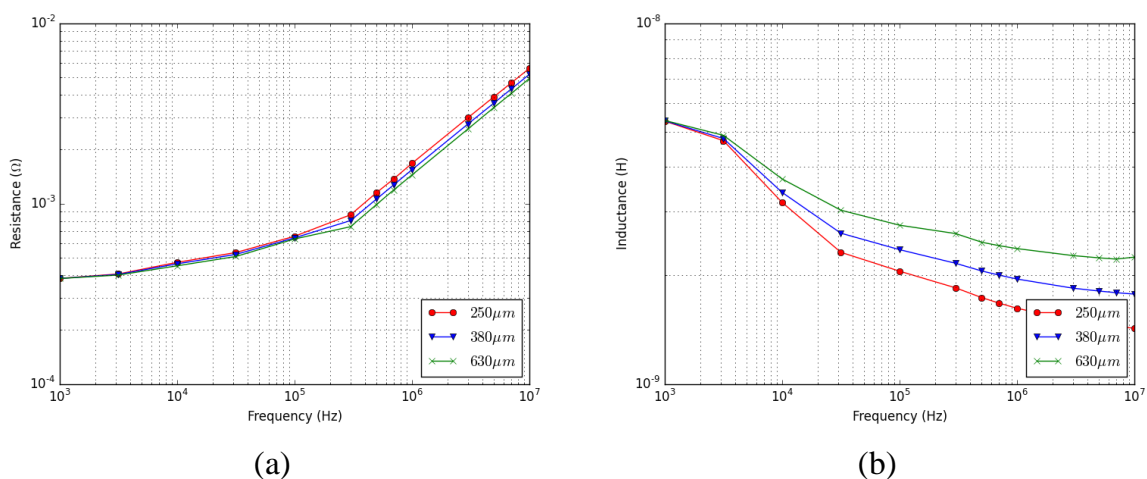


Figure 2.39: Simulation of different ceramic thickness

2.5.2.3 Analytical approach for partial inductance

A circuit simulation requires to decompose the loop inductances into partial inductances (one or more per copper track, depending on the number of terminals it connects). This can be done by using other software tools (Q3D, InCa3D, etc), or by an analytical approach. In this section, we use this latter solution based on that proposed by [115] will be presented.

At high frequencies, the current distribution over the conductor cross section is no longer uniform, this is caused by skin and proximity effects. In order to determine the analytical value of the corresponding impedance, [115] developed a method in which the cross section of a rectangular conductor is analytically divided into separated “subbars”, as illustrated in Figure 2.40. The number of divisions along the width is NW and the number of divisions along the thickness is NT . Each subbar dimension is $\Delta t = t/NT$ and $\Delta w = w/NW$. However, the calculation complexity increases with the frequency as the transversal sizes of each subbar must be lower than the skin depth. To overcome this problem we propose, in this section an evolution of this method where the problem size do not depends on the frequency. In the proposed method, rather than using many subbars, we cut the rectangular conductor into only three bars of different sizes as shown in Figure 2.41, where l , w and t correspond respectively to the length, the width and the thickness. In the following developments, δ represents the skin depth which can be calculated by:

$$\delta = \sqrt{\frac{1}{\sigma \mu \pi f}}$$

Where σ is the electric conductivity, μ the magnetic permeability, and f the frequency.

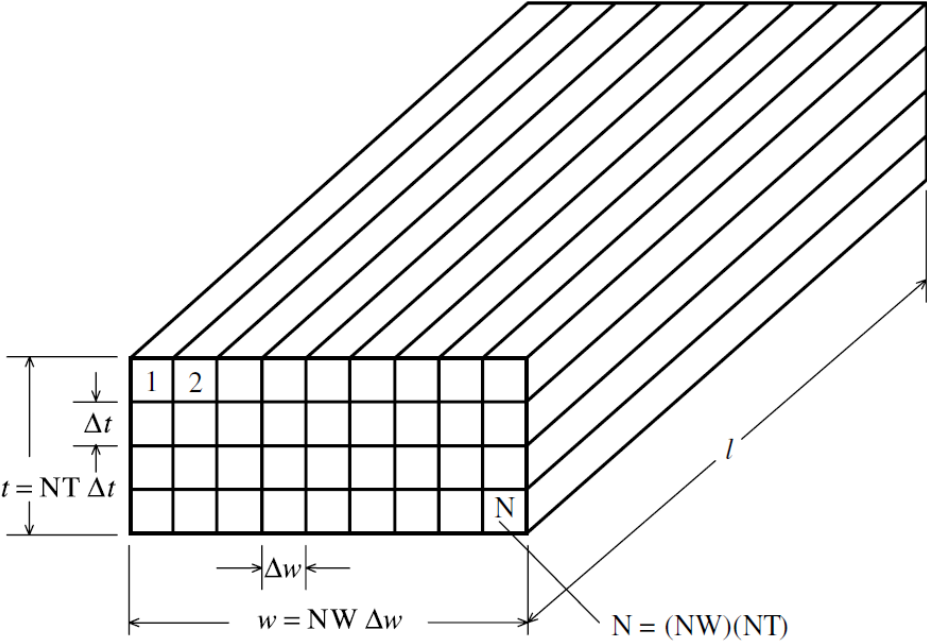


Figure 2.40: “subbars” decomposition for a rectangular cross section conductor

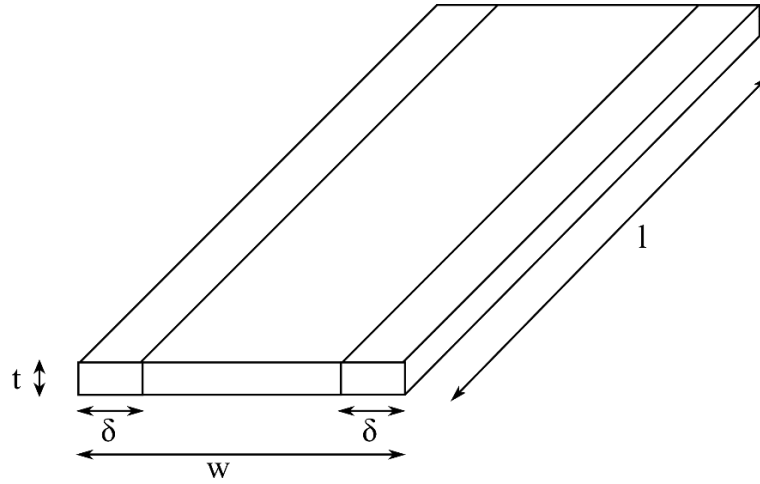


Figure 2.41: Proposed simplified “subbars” cross section

The mutual partial inductance between two parallel tracks proposed by [115] is shown in the equation below. The different parameters used in this equation are illustrated in Figure 2.42. The self-inductance can be calculated with the same formula while considering that a and b equal to 0. Here, q_1 to q_4 correspond to $a-w_1$, $a+w_2-w_1$, $a+w_2$, a ; r_1 to r_4 correspond to $b-t_1$, $b+t_2-t_1$, $b+t_2$, b ; and s_1 to s_4 correspond to $l+s+m$, $s+m$, s , $l+s$.

$$M_p = \frac{\mu_0}{4\pi} \frac{1}{w_1 t_1 w_2 t_2} \left[\begin{array}{cc} [f(x, y, z)] & \begin{array}{c} a - w_1, a + w_2 \\ (x) \end{array} \\ \begin{array}{c} a + w_2 - w_1, a \\ (y) \end{array} & \begin{array}{c} b - t_1, b + t_2 \\ (z) \end{array} \end{array} \right] \begin{array}{c} l + s + m, s \\ s + m, l + s \end{array}$$

Where

$$\left[\begin{array}{cc} [f(x, y, z)] & \begin{array}{c} q_1, q_3 \\ (x) \end{array} \\ \begin{array}{c} q_2, q_4 \\ (y) \end{array} & \begin{array}{c} r_1, r_3 \\ (z) \end{array} \end{array} \right] \begin{array}{c} s_1, s_3 \\ s_2, s_4 \end{array} = \sum_{i=1}^4 \sum_{j=1}^4 \sum_{k=1}^4 (-1)^{i+j+k+1} f(q_i, r_j, s_k)$$

And

$$\begin{aligned}
f(x, y, z) = & \left(\frac{y^2 z^2}{4} - \frac{y^4}{24} - \frac{z^4}{24} \right) x \ln \frac{x + \sqrt{x^2 + y^2 + z^2}}{\sqrt{y^2 + z^2}} \\
& + \left(\frac{x^2 z^2}{4} - \frac{x^4}{24} - \frac{z^4}{24} \right) y \ln \frac{y + \sqrt{x^2 + y^2 + z^2}}{\sqrt{x^2 + z^2}} \\
& + \left(\frac{x^2 y^2}{4} - \frac{x^4}{24} - \frac{y^4}{24} \right) z \ln \frac{z + \sqrt{x^2 + y^2 + z^2}}{\sqrt{x^2 + y^2}} \\
& + \frac{1}{60} (x^4 + y^4 + z^4 - 3x^2 y^2 - 3y^2 z^2 - 3x^2 z^2) \sqrt{x^2 + y^2 + z^2} \\
& - \frac{xyz^3}{6} \tan^{-1} \frac{xy}{z\sqrt{x^2 + y^2 + z^2}} \\
& - \frac{xy^3z}{6} \tan^{-1} \frac{xz}{y\sqrt{x^2 + y^2 + z^2}} \\
& - \frac{x^3yz}{6} \tan^{-1} \frac{yz}{x\sqrt{x^2 + y^2 + z^2}}
\end{aligned}$$

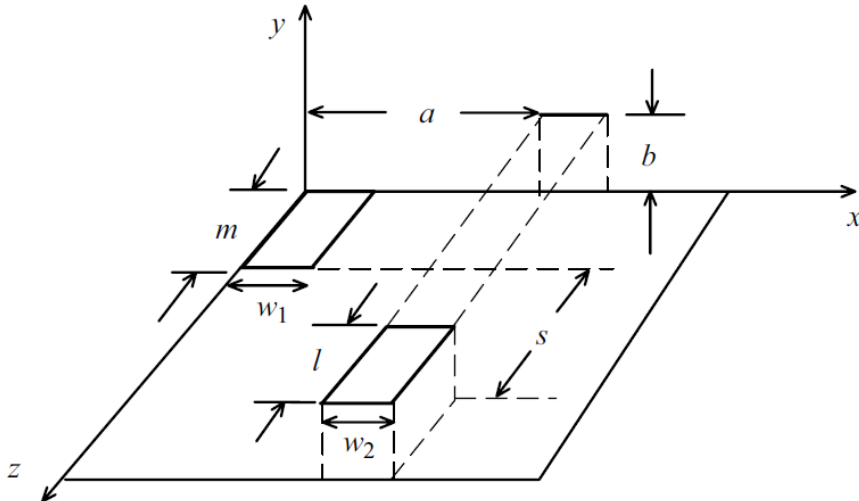


Figure 2.42: Mutual partial inductance between two conductors

In order to confirm this simplified approach, the short loop (shown in Figure 2.36) is studied. Firstly, we consider only the top copper layer therefore eliminating the screening effect. The equivalent geometry of the two conductors are represented shown in Figure 2.43.

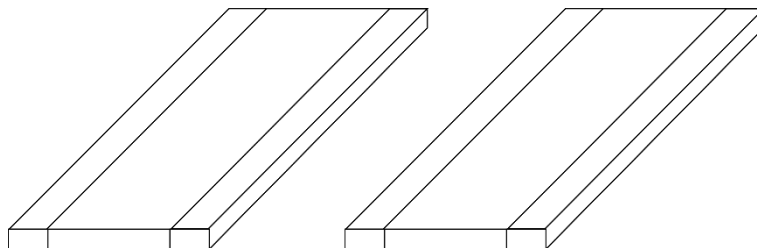


Figure 2.43: Equivalent geometry without bottom copper

The loop inductance and resistance values for frequencies ranging from 100 Hz to 100 MHz is given below in Figure 2.44. The simulation results obtained with COMSOL are also presented for comparison. As we can see, the resistance and inductance results are relatively close to each other for the two methods at low frequencies.

In fact, when the skin depth has a value larger than the conductor thickness and smaller than the width of the conductor, which means $w > \delta > t$, the results of the two methods are in good agreement, with an error of less than 10%. However, with the increase of frequency, the skin depth becomes smaller than the conductor thickness, and the current distribution changes. For such high frequencies, the current distribution is no longer uniform at both sides of the track. The current mainly flows in the four corners of the track. The analytical configuration should be modified as presented in Figure 2.45. For these high frequencies, the Figure 2.41 geometric decomposition leads to a higher error (26% at 10 MHz). As the computation of the four corners analytical solution is a little longer and time consuming, the corresponding formulation for this configuration will not be developed in this thesis work.

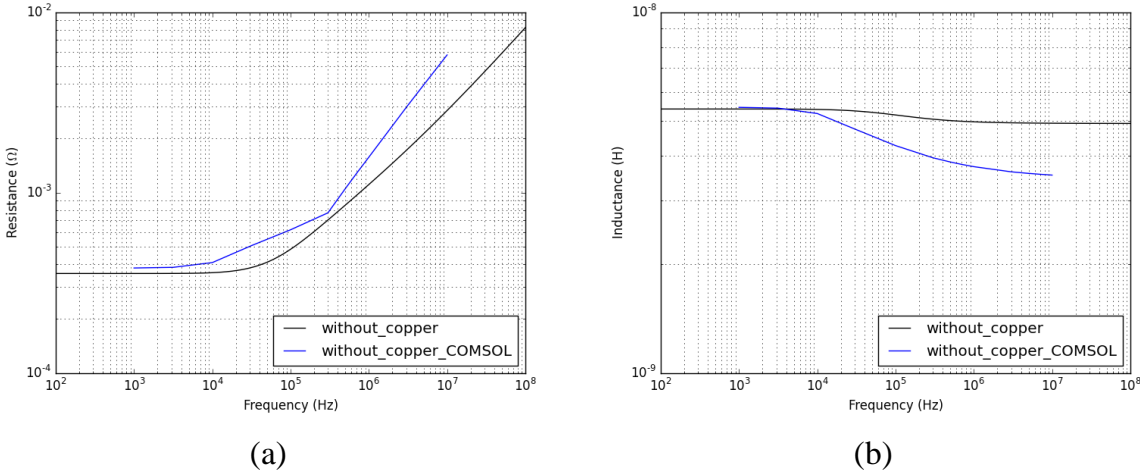


Figure 2.44: Resistance and inductance values without bottom copper for analytic calculation and COMSOL simulation

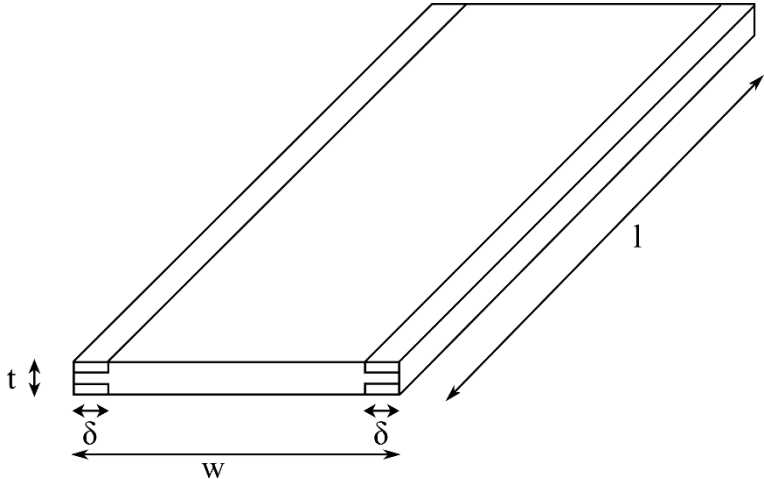


Figure 2.45: Current distribution at high frequencies ($\delta < t$)

The next step is the modeling of the screen effect due to the bottom side copper layer. In order to study this effect, the method of mirror images will be employed. The basic idea of this method is to remove the ground plane, and calculate the value of impedances using the virtual image of each conductors as shown in Figure 2.46. The virtual conductor must

be at twice the distance between the conductor and the ground plane, it must also be crossed by a current with the same intensity but with a reversed flowing direction.

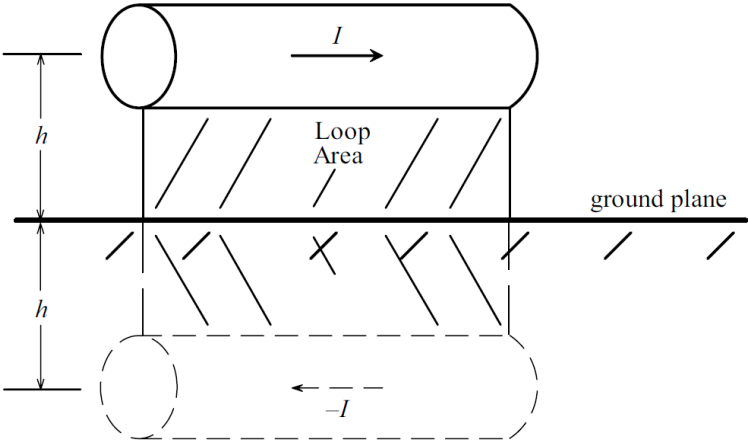


Figure 2.46: Transmission line with ground plane

In our study, the virtual tracks are at a distance $s = 2e$ between the real tracks and the virtual ones where e is the ceramic thickness. According to the mirror images method, the equivalent geometry is given in Figure 2.47. Using the proposed analytical method, the impedance of the “short” loop for different ceramic thickness can be calculated. It is given in Figure 2.48. In this figure, results obtained with analytical calculation and finite elements simulations are compared. At high frequencies, where the screen effect layer is effective, the stray inductance error is less than 5%. At lower frequency, the previous method (without the screen effect) should be used. Indeed, the mirror images method gives correct results when the screen thickness is much higher than the skin depth. The copper thickness in our application equals $300 \mu\text{m}$, this condition will be verified for a frequency much higher than 47 kHz.

The global impedance calculated with the analytical method is obtained by summing the circuit partial impedances. Whereas COMSOL only gives the global loop impedance, the analytical method allows to define a partial inductance for each sub-circuit. As the global impedance given by the two methods are similar (although on a limited frequency range only), we can consider that we can have confidence in the analytic approach and we will use this method in the following to calculate the partial impedances of the circuit.

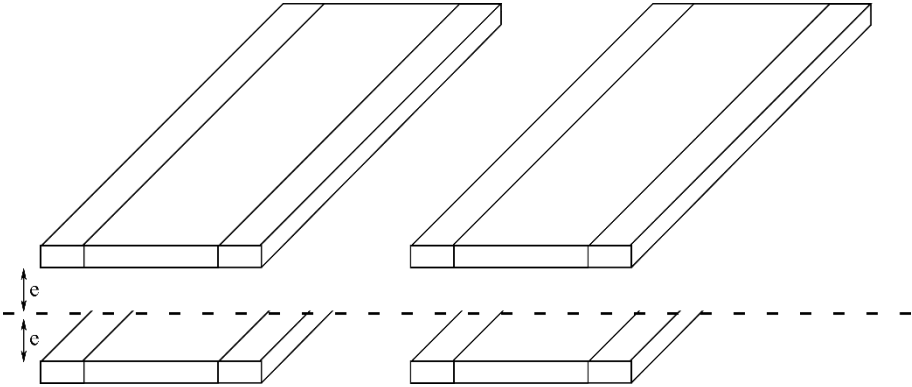


Figure 2.47: Equivalent geometry with bottom copper

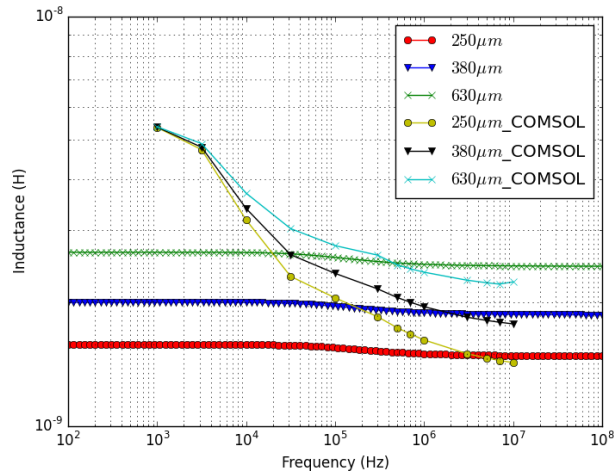


Figure 2.48: Inductance values with bottom copper layer; Analytic calculation and COMSOL simulation

2.5.3 Electric analysis

2.5.3.1 Electrical Simulation

From the previous section, the partial elements of the circuit can be calculated using an analytical approach. These partial elements can now be used in a circuit simulator in order to evaluate the electrical or EMI constraints. Some values such as over voltages, conduction losses, or switching losses can be evaluated with such simulations.

In this section, simulation results using the Pspice simulator will be presented for the half-bridge prototype. We will focus on the analysis of the switching losses influenced by the loop inductance at high frequencies and the common mode performance.

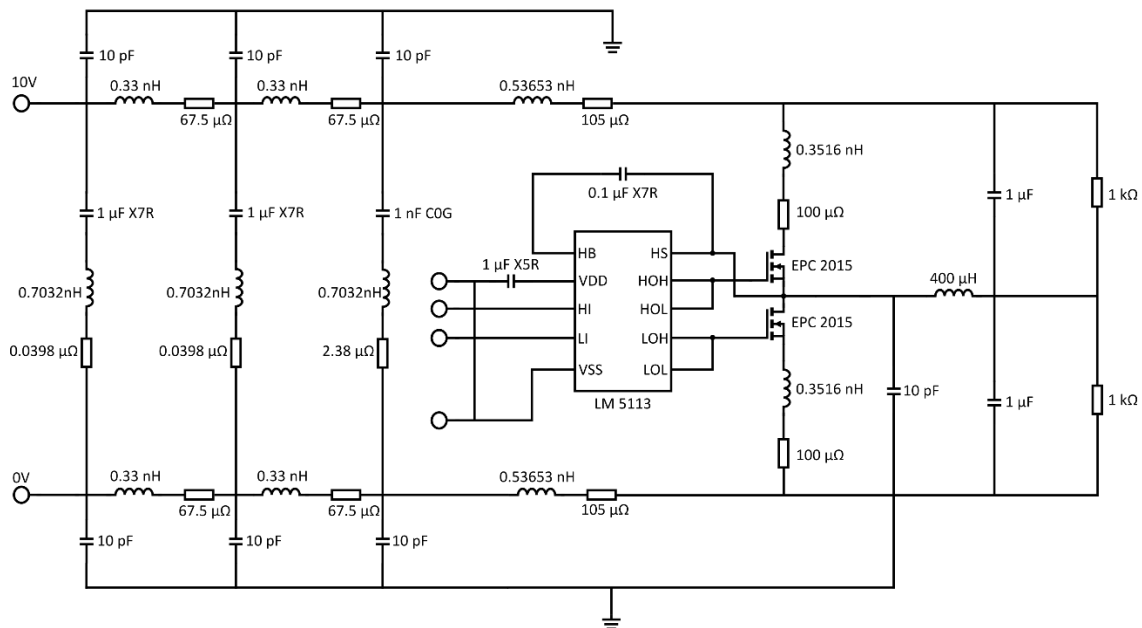


Figure 2.49: Electrical circuit for Pspice simulation

The simulated circuit as shown in Figure 2.49 uses the spice model for each electronics component. The spice model of the EPC 2015 and LM5113 are supplied by the component manufacturers. The stray inductances and resistances of the loop are calculated with the analytical equations as presented in section 2.5.2.3. The three decoupling capacitors are modeled as ideal capacitors in series with their Equivalent Series Resistance (ESR), ESR can be calculated using following formula:

$$ESR = \frac{\tan \delta}{2\pi f C}$$

Where f is the switching frequency, C the capacitance and $\tan \delta$ the tangent of the loss angle which is provided by the supplier. This loss factor depends on the dielectric type used in the capacitors. In our case, the ESRs are 2.38 mΩ for the 1nF capacitor, and 0.0398mΩ for both 1μF capacitors.

Another important element is the stray capacitance between each copper track and the backside copper layer. These capacitances have an important effect on the common mode performances. To calculate these stray capacitances, we use the classical “plane capacitor” formula, where A is the surface, d , the ceramic thickness (600 μm), ϵ_0 , the electric constant ($\epsilon_0=8.85e^{-12}$) and ϵ_r , the relative static permittivity of the ceramic ($\epsilon_r=10$).

$$C = \epsilon_0 \epsilon_r \frac{A}{d}$$

We used a simple LR circuit as the charge, the inductance and the resistance are set to 1 μH and 1 Ω to get a stable current of 6 A. The frequency is set to 1 MHz.

The loop inductance at high frequencies has a significant influence on the switching speed of the device and the peak voltage at turn-off. During the turn-on period, the drain current increases, resulting in a positive di/dt through the loop inductance, which induces a positive voltage. This induced voltage decreases the effective voltage on the device and slows down the current rise. If the voltage remains low during turn-on, this can reduce the switching loss. During the switchin-off, the drain current falls and produces a negative di/dt through the loop inductance and induces a negative voltage. This voltage increases the effective voltage of the device and slow the current falling slope. This results in higher switching losses. Figure 2.50 shows the switching losses versus loop inductance value. The total loop inductance varies from 0.4 nH to 2 nH (the ratio between the various partial inductances remains constant). The results proves that the loop inductance has a large effect on converter turn-off loss, as the circuit dissipates twice more power for a 2 nH loop inductance as it dissipates for a 0.4nH one.

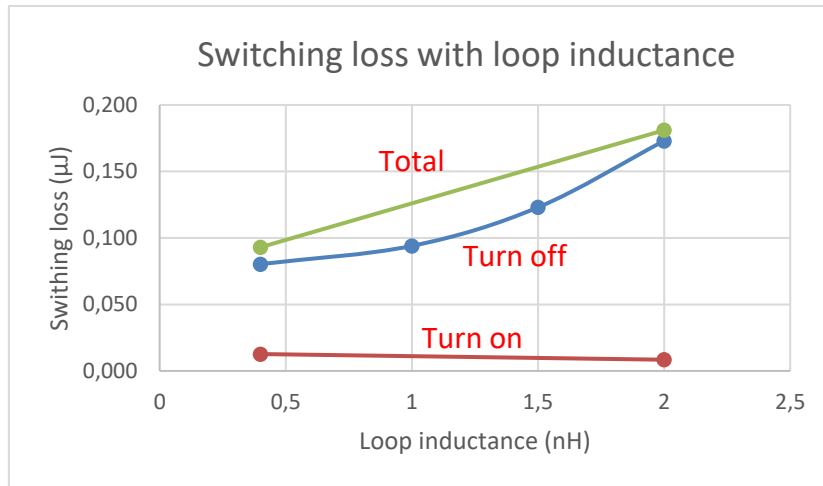


Figure 2.50: Switching loss of the circuit in Figure 2.49 with the variation of loop inductance (simulation)

We can also simulate the common mode and differential mode current i_{DM} , i_{CM} and voltage $v_{LISN1} = v_L$, $v_{LISN2} = v_N$ by adding a Line Impedance Stabilization Network (LISN) whose model is shown in Figure 2.51. The relation connecting these voltages to the currents is:

$$V_L = -50(i_{dm} + i_{cm}/2)$$

$$V_N = +50(i_{dm} - i_{cm}/2)$$

The simulation results are shown in Figure 2.52, The simulation proves that in case of the bottom side copper layer substrate, conduction emission are mainly due to common mode current. Indeed, from 3 MHz to 30 MHz the LISN voltages are equal to 25 times the common mode current. Conversely, the common mode current has no effect on the conduction EMI level when there is no bottom side copper layer. In this configuration, the EMI level is totally defined by the differential mode current which is filtered by the decoupling capacitor.

These simulations prove that if the bottom side copper layer improves the loop inductance and therefore the turn-off loss, it also degrades the EMI level of the converter. This phenomena is due to the parasitic capacitance which formed by the top side and the bottom side copper layers through the insulation ceramic layer of the DBC.

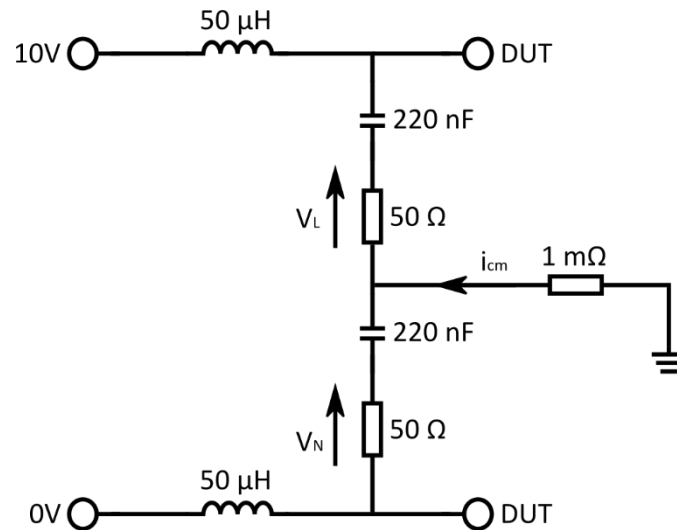


Figure 2.51: Line Impedance Stabilization Network

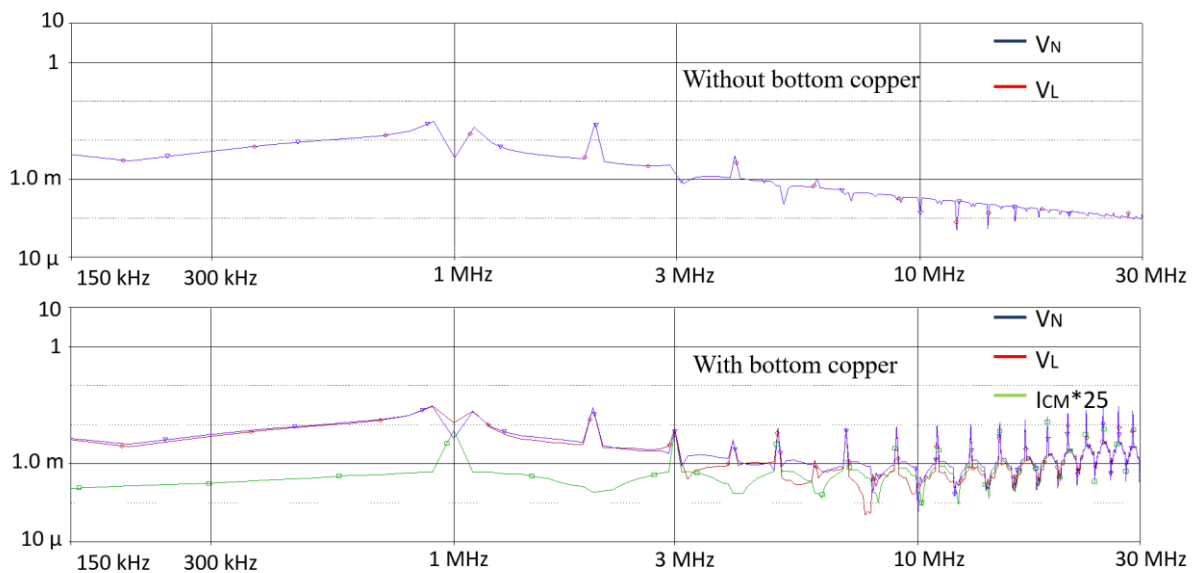


Figure 2.52: Common mode disturbance simulation results

2.5.3.2 Experimental characteristics

To characterize the electric performance, we firstly used the development board EPC9001 (shown in Figure 2.53) which is rated a 40 V maximum device voltage, 15 A maximum output current. It contains two EPC 2015 transistors in a half-bridge configuration using the Texas Instruments LM5113 gate driver, supply and bypass capacitors, plus a timing circuit to generate control signals (in particular the dead time between the upper and lower switches) The complete block diagram of the circuit is given in Figure 2.54.



Figure 2.53: Development board EPC9001

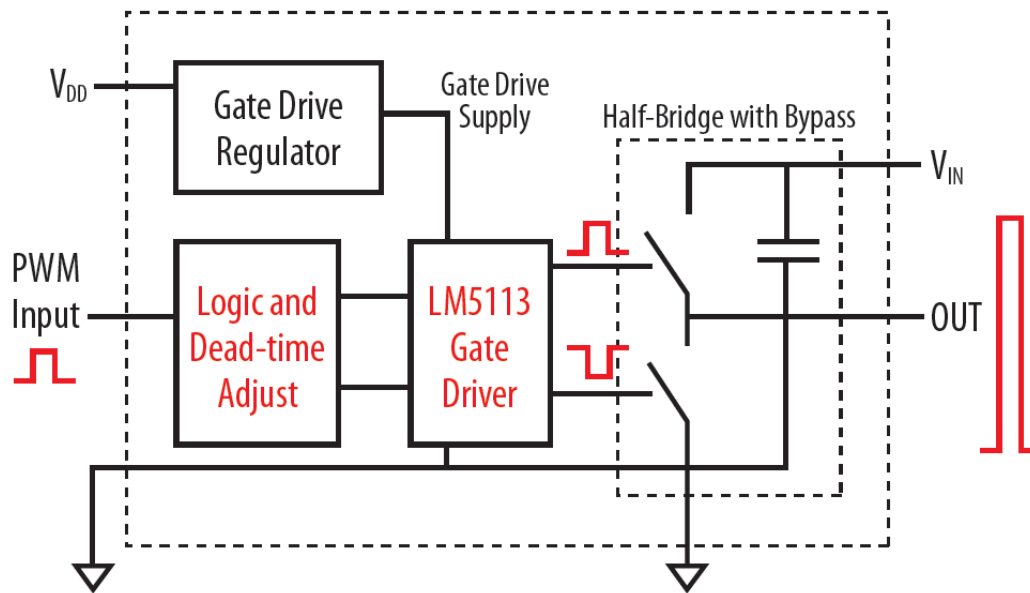


Figure 2.54: Block Diagram of EPC9001 Development Board

For the tests, the control of the DBC half-bridge demonstrator is connected on the gate driver regulator and dead-time generator of the EPC9001 evaluation board. The input signals are generated by a Hameg HM8035 with 1 MHz frequency and 450 ns pulse width. The charge is a small circuit with a capacitive divider (1 μF film, 10 μF tantalum, 1 $\text{k}\Omega$ by path), connected between DC+ and DC- and an air inductance between the output of the prototype and midpoint of the capacitive divider. The current is measured with a Tektronix TCP0030 current probe on the inductive load, and the voltage is measure with a Tektronix P5139 probe on the middle point, with a very short ground lead. The circuit diagram and test bench are presented in Figure 2.55 and Figure 2.56. The measurement is realized with a 10V DC bus, and the switching current is 5.8 A. The experimental results are shown in Figure 2.57(a).

In order to compare the experimental results, we set the same condition for the Pspice simulation, and the results are shown in Figure 2.57. This comparison proves that the proposed modelling approach is satisfying for modelling the switching performances.

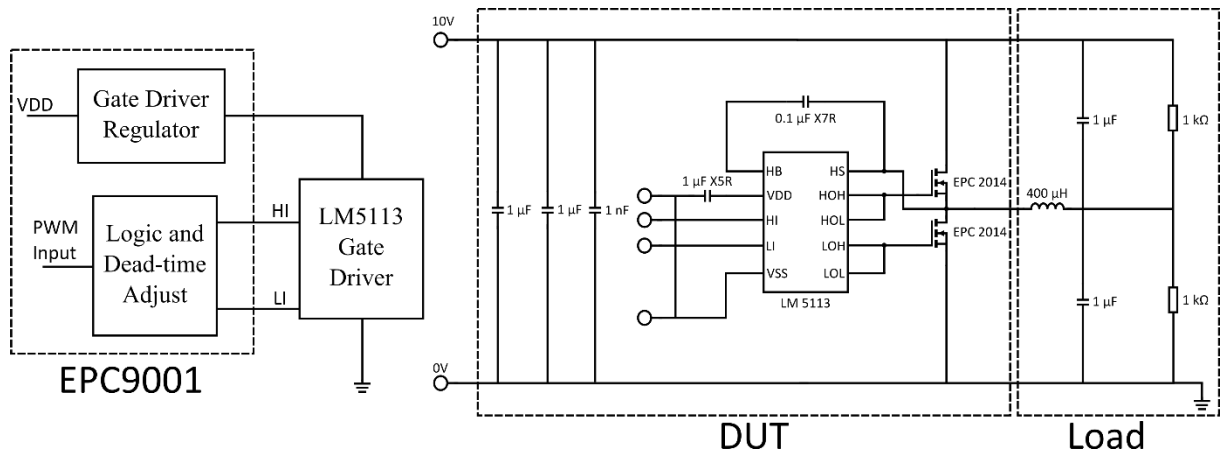


Figure 2.55: Circuit diagram used for electric characterization

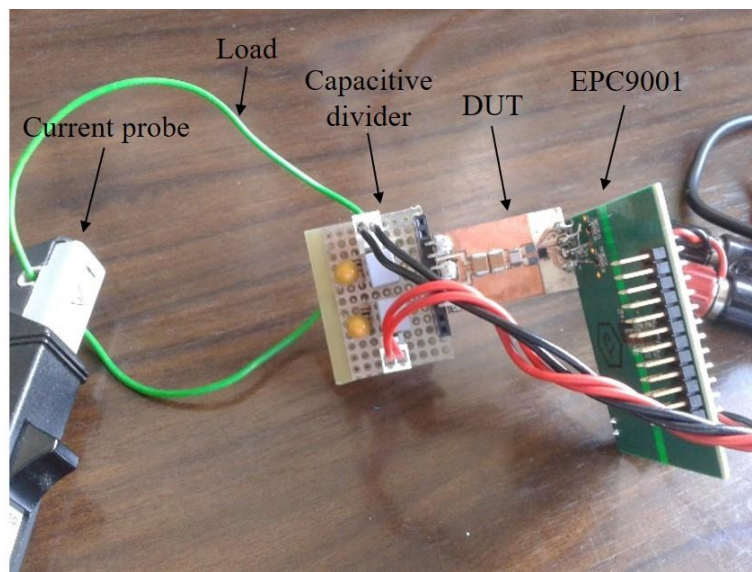


Figure 2.56: Test bench for DBC half-bridge prototype

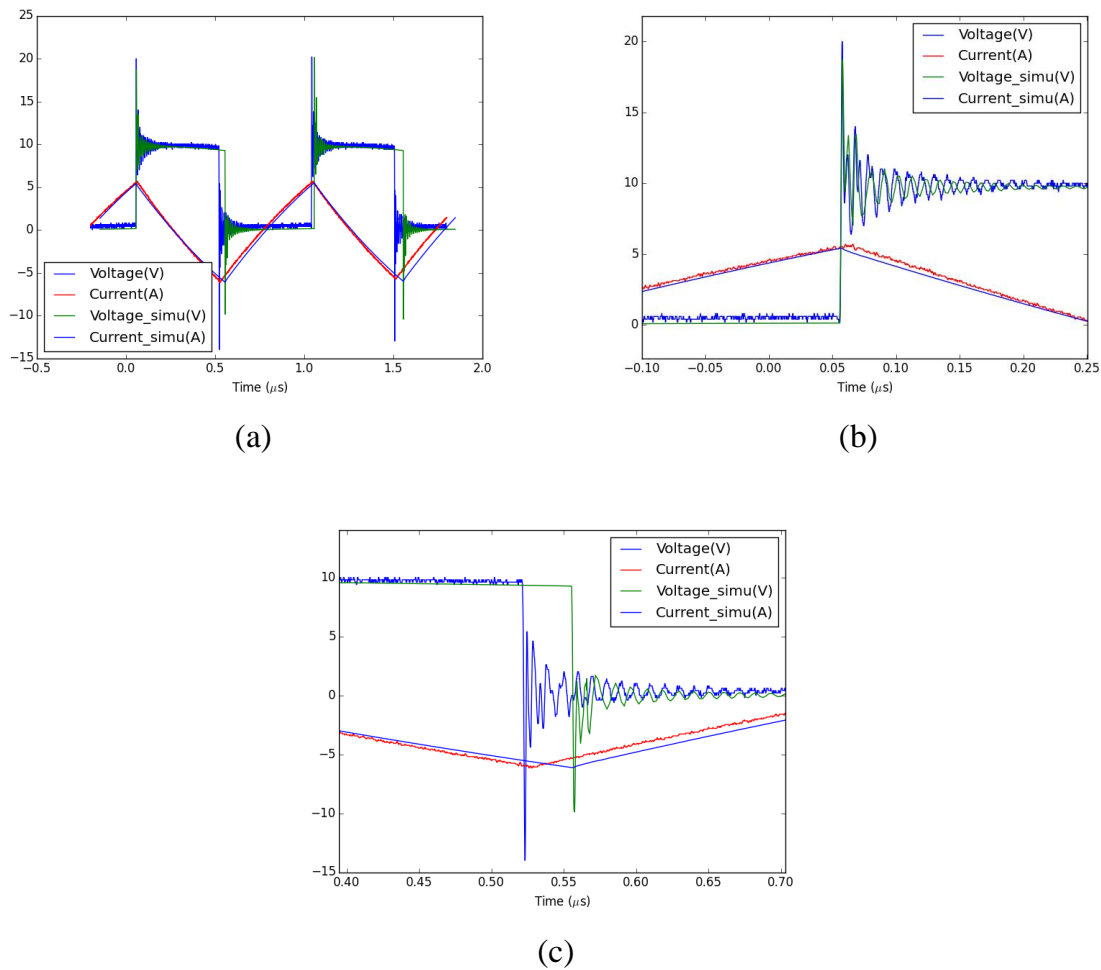


Figure 2.57: Experimental and simulation results for this DBC half-bridge prototype. (a) Switching waveform for 2 periods, (b) Zoom for turn-off part of low side transistor, (c) Zoom for turn-on part of low side transistor

2.6 Conclusion

In this chapter, three test vehicles were introduced to study the thermal management of GaN devices. Their fabrication processes were described, and the important steps were detailed. The thermal performance of these prototypes was analyzed using FEM simulation and experimental characterization. In the second part of the chapter, the electromagnetic and electric performances were analyzed.

Although the GaN transistors are designed to be mounted on a PCB substrate, the thermal analysis proves that a ceramic substrate offers a substantial gain regarding thermal management (4-fold reduction). Compared to the flip-chip mounted prototype, the flip-flip chip configuration, which dissipates the heat through the silicon substrate of the die, does not have significantly better thermal performance. Besides, this prototype requires more fabrication steps and it is more difficult to realize than the classical flip-chip configuration.

In terms of the electromagnetic performance, the parasitic inductances can be largely mitigated by reducing the ceramic thickness. Low values can be achieved (<2 nH) using a

thin ceramic (250 μm) and a bottom copper layer. They remain larger than when using a multilayer PCB with a suitable layout, but should be acceptable in many cases.

The DBC is therefore an attractive substrate for the high current converters, as the slightly higher switching losses caused by the parasitic inductance will be more than counterbalanced by the dramatic reduction in thermal resistance, and by the lower conduction losses (thanks to much thicker copper layers).

CHAPTER 3. High Voltage Packaging with vertical components

3.1 Introduction

In the previous chapter, we introduced the GaN lateral component and its packaging technique. In contrast with these lateral devices which are dedicated to low-voltage applications, most power devices have a vertical structure, especially when considering high voltage (1000 V and more). The classical two dimensional packaging uses bonding wires for vertical components, which represents an important failure cause [116-118], and generates large parasitic inductances [43]. In this chapter, we will focus on a new packaging technique for vertical power devices, based on embedding them in a printed circuit board. As presented in chapter 1.

3.2 Proposed structures for the analysis of the contact

We have designed two test vehicles to study the PCB interconnection: in the first, a single diode is buried in the FR4 layer, for the development of the technology, and simple characterization. The cross-section and a picture of a fabricated prototype are shown in Figure 3.1.

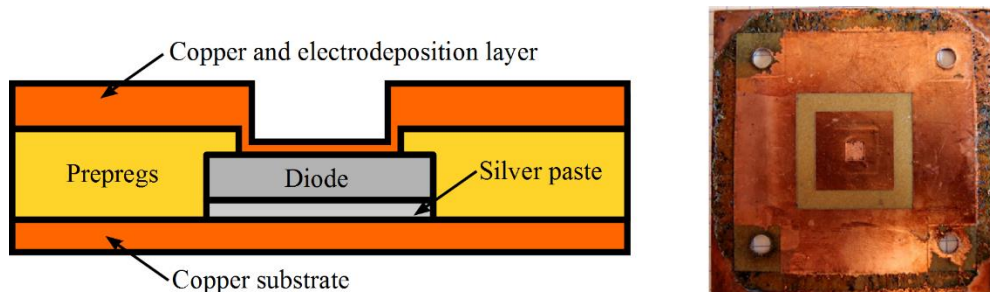


Figure 3.1: Cross-section and realization of a diode embedded in PCB

The second set of prototypes consists of four 600V, $6 \times 6 \text{ mm}^2$ dies embedded in PCB with various contact layouts (from 1 to 16 mm^2 , in 1 to 9 contact areas). These prototypes are used to evaluate the effect of the contact layout on the resistance of the interconnects. The layout of the test vehicles is designed to allow for 4-point measurements. A photograph of some of the test vehicles used in this study is visible in Figure 3.2.

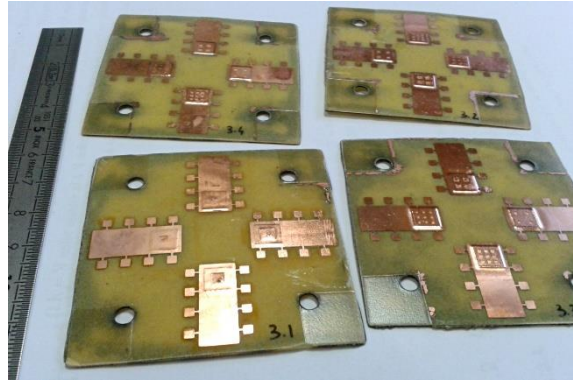


Figure 3.2: Left: some of the test vehicles, with 4 embedded diodes each.

3.3 Fabrication process

The embedding process is summarized in Figure 3.3 and described below. It is performed in-house using prototype-scale equipment.

First, the dies are prepared: most dies currently available on the market have an aluminum topside finish, which, as we will show later, is not compatible with our embedding technology. A copper layer must therefore be deposited prior to the embedding. This is performed by evaporating an adhesion layer of titanium (50 nm) and copper (150 nm or 500nm) through a shadow mask in a PVD system (electron beam system EVA300, Alliance concept). The workflow for embedding is as follows:

- a) The die to be embedded is attached to a copper or DBC substrate using silver sintering. With solder, the die would float on a liquid layer during reflow, and could move slightly. With silver-sintering, which is a solid-state technology, the die remains exactly at the same position throughout the process. This is important as the die is no longer visible once embedded. Silver sintering is performed without pressure (in an oven), using material from Heraeus (Microbond ASP295-series).
- b) The outline of the die is laser-cut in layers of prepreg (FR4 Isola 370HR), which are stacked on the substrate (alignment holes are also present on the prepreg layer and the substrate, to register with the alignment pins in the pressing system). Some more prepreg layers are stacked on top of the die (Arlon 55NT, non-woven aramid material is used instead of FR4 because it leaves fewer residues after the laser ablation that comes later in the process). A 35 μm -thick copper foil is placed on top of the stack.
- c) The stack is then laminated, in a hot press (90 minutes, 195 °C, 13 bars).
- d) A window is etched in the copper above the die. This is performed using standard PCB photolithography (the PCB is laminated with dry-film photoresist, exposed through a mask, developed, and then etched using ferric chloride). This step requires careful alignment with the die, which is no longer visible (hence the need for silver sintering in step (a)). The registering of the mask is performed using the alignment holes used in step (b).
- e) The fiber-resin composite which is exposed through the window in the copper is ablated using a CO₂ laser (Gravograph LS100EX 60 watt). As copper is not affected

by the laser, this step is fairly robust: the alignment is provided by the window in the topside copper foil, and the ablation stops as soon as the laser hits the copper metallization of the die. Therefore, there is no need for a very accurate control of the laser parameters.

- f) Finally, a new coat of copper is applied by electroplating (standard “metallized holes” PCB process, using chemistry from Bungard).

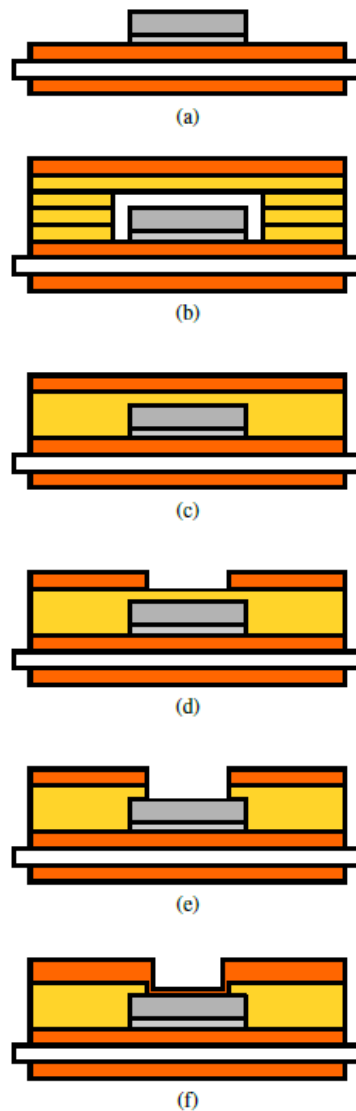


Figure 3.3: Fabrication process of embedding technique

3.3.1 PCB materials used in fabrication

3.3.1.1 Isola PCL370HR and Arlon 55NT

The FR4 and aramid material we used here is from Isola (PCL370HR) and Arlon (55NT). These materials are chosen by 3DPHI platform due to their good performance. The PCL370 HR is a 180 °C glass transition temperature (T_g) FR-4 system (where the transition temperature of FR4 is normally 125°C to 130 °C [119]) for multilayer PCB

applications where the thermal performance and reliability are required. This material is used in the stacking to match the die thickness. 55NT is an epoxy laminate and prepreg system, reinforced with a non-woven aramid substrate. It has a glass transition temperature of 170 °C. This material leave fewer residues after laser ablation, but it is more expensive than FR4, which is why it was not used for the whole prepreg stack. Some parameters of these two kinds of materials are shown in Table 3.1.

Table 3.1: Material properties of PCL370HR and 55NT [94, 108]

Material	Electric strength (kV/mm)	Thermal Conductivity (W/mK)	Arc Resistance (s)	Glass Style	Resin Content
PCL370HR	54	0.4	115	1080	66%
55NT	48.8	0.2	165	E220	49%

3.3.1.2 Release film and press-pads

A recommended lamination lay-up is shown in Figure 3.4, some layers are added to those constituting the multi-layer circuit: A release film (Pacoplus, from Pacothane technologies), prevent the resin of the prepregs from adhering to the platens of the press. The pressing mats (Pacopad, also from Pacothane technologies), equalize the pressure from the press to compensate for possible differences in thickness in the multi-layer stack.

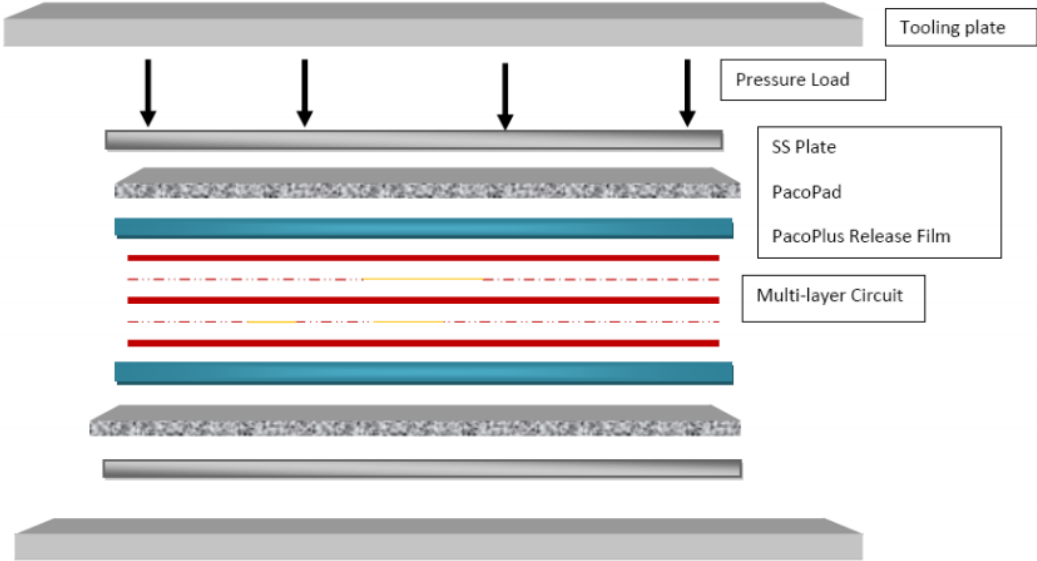


Figure 3.4: Recommended lamination lay-up [120]

3.3.2 Chemical Ag deposition

Ag sintering (the process used to attach the die to the copper substrate) works better on Ag-finished surfaces. While the dies usually have an Ag finish on their backside (and are therefore compatible with the Ag sintering process), this is not the case of our bare-Cu substrates. It is recommended to deposit a metallization layer based on Ag to get a suitable surface for sintering [121]. Here, we use a wet process to coat the copper substrates with a

layer of Ag. This process is before the sintering of the die (Figure 3.3 (a)). An example of such Ag deposition result is shown in Figure 3.5. The deposition steps are given as following [122].

- Step 1 – Cleaning and micro attack: Clean the substrate with sulfuric acid and ammonium persulfate for 30 to 60 seconds under 25 to 35 °C.
- Step 2 – Rinsing: Static Rinse of the substrate with the deionized (DI) water.
- Step 3 – Pre-dip: Thoroughly clean equipment with cleaner and thoroughly rinse.
- Step 4 – Plating Bath: Repeat Pre-dip procedure until the addition of ALphaSTAR 300B. Fill the rest of the tank with DI water and heat to operating temperature (48 – 54 °C).

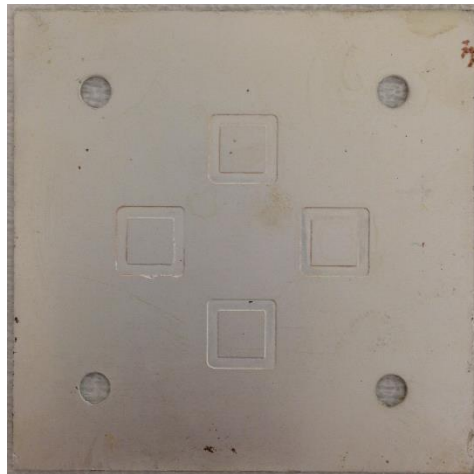


Figure 3.5: An example of silver deposition on a copper plate. The 4 holes register with the alignment pins of the press platen for lamination. The 4 engraved squares are used to position the dies in the sintering step.

3.3.3 Chip preparation

As we will demonstrate later, a preparation step is necessary on the dies to improve the result of copper electrodeposition. In fact, the standard material of the chip's topside finish is aluminum which is more compatible with aluminum wire bonding than with copper electroplating. This could lead to adhesion issues during the electrodeposition, or to a poor quality deposit. In this step, layers of titanium (Ti)/copper (Cu) are deposited on the upper face of the chips by physical vapor deposition. The materials to deposit are placed in crucibles situated on the bottom of the equipment and the samples to metallize are fixed on a turntable on the top. Each of the crucibles, is heated by an electron beam and the material they contain evaporates. The material condensates on the dies (as well as on all the surfaces of the chamber)

Before the deposition, some preparation is necessary. Firstly, the chips are cleaned with some acetone and ethanol in a heating ultrasonic bath. Then, the chips are masked to control the metallization region. For each chip, the deposition must not cover the edge passivation, otherwise it will short circuit the chip.

The masking is realized by a custom shadow mask as shown in Figure 3.6(a). It is used for the metallization of three different chip types: a Si diode, a SiC diode and a Si IGBT (which were used for works described later in this chapter). The chips are placed in the

footprint corresponding to their type. Twenty seven footprints are available for each chip type. Once the chips are placed, they are maintained in position by some polyimides adhesive tape (Figure 3.6(b)). The metallization is then deposited on the upper face of the chips by passing through the windows of the mask (Figure 3.6(c)). Figure 3.7 shows an IGBT with 150/500 μm Ti/Cu finish.

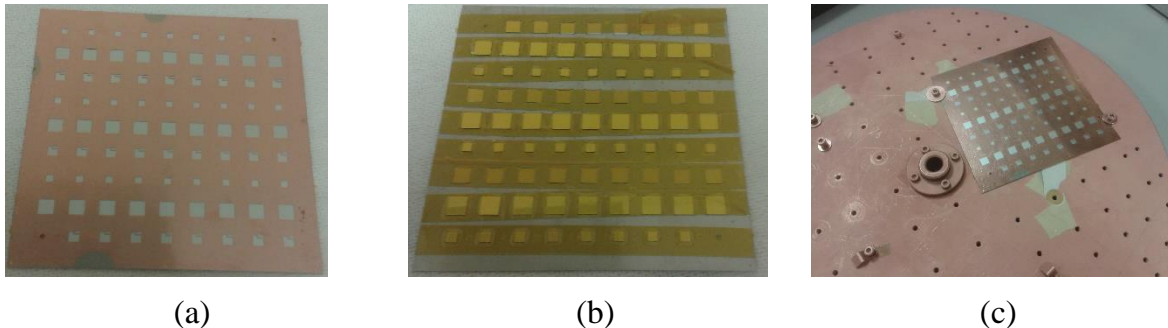


Figure 3.6: Shadow mask: front (a), showing the openings where the Ti/Cu layers will be applied. Back, showing the dies in their locating pockets, kept in place using polyimide tape. The mask attached to the PVD system support, ready for deposition (c). The mask is made out of two stainless steel plate (laser cut and bonded together by DB Products), and measures 100x100 mm².

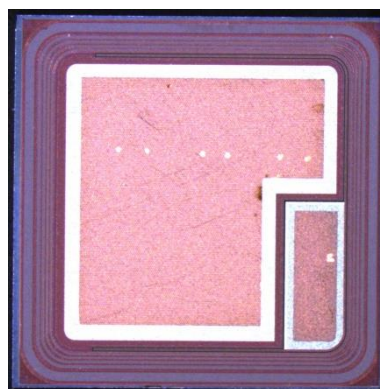


Figure 3.7: An IGBT with Ti/Cu finish

3.3.4 Ag Sintering

The process of attaching the chips by Ag sintering is relatively simple: on the metal part of an electronic substrate cleaned beforehand, we deposit a silver paste layer by screen printing (shown in Figure 3.9 (a)) with a 50 or 100 μm thickness (according the utilized stencil) to ensure a uniform deposit thickness. The chips are then placed onto the fresh paste with a “pick and place” machine (shown in Figure 3.8). Finally, the substrate is placed on a heated press (shown in Figure 3.9 (b)) or in an oven depending on whether pressure assistance is required or not (both processes are possible with the paste we use, Heraeus LTS 295). The assembly cycle include two stage. The first one takes place at a moderate temperature (80 to 150 $^{\circ}\text{C}$), and the objective is to evaporate the organic component of the paste, in order to only keep the silver powder. The second step, with a higher temperature (230 to 300 $^{\circ}\text{C}$), performs the actual sintering. Once the assembly finished, a pure silver joint is obtained.

The Ag sintering technology allows an accurate positioning as the die will not move during the process (as opposed to soldering, where displacements can occur during the reflow). The sintering joint also has some of the excellent electric and thermal quality of the silver, best conductor among the metals (sintered layers have a thermal conductivity of 200 W/m.K and electric resistivity of 2.6 nΩ.cm [110]).

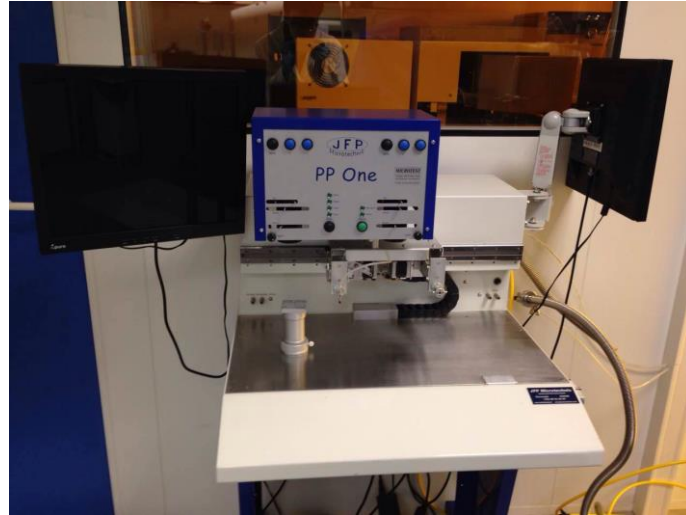


Figure 3.8: Photography of “pick and place” machine

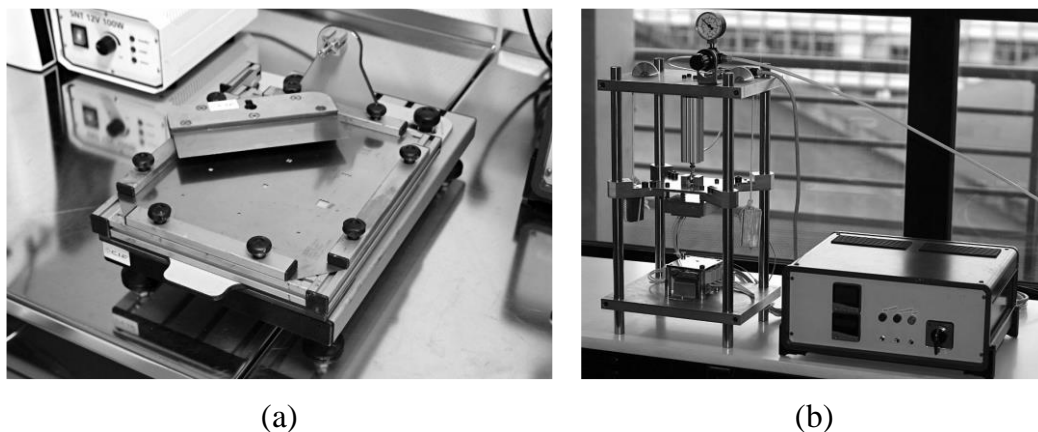


Figure 3.9: Photography of screen printing machine and heated press used for sintering

3.3.5 Detailed description of the process

3.3.5.1 PCB embedding

- Step 1: The different PCB fabrication materials (prepregs PCL370HR and Arlon 55NT, release film Pacothane Plus) are firstly cut by a CO₂ laser. Their shapes are shown in Figure 3.10. The cutout of 370HR is 1 mm larger than the diode. The non-woven material 55NT has no cutout for the diode, as it is used as the topmost layer, the one that covers the diode. The release film Pacothane plus has the same shape as the 55NT layer (shown in Figure 3.11) but a little larger (5 mm for each side). The number of the prepreg layers depends on the thickness of the die and prepreg type, the calculation method will be presented after. A copper layer of 35 μm and two Pacopad layer are cut in a suitable shape with a sharp knife.

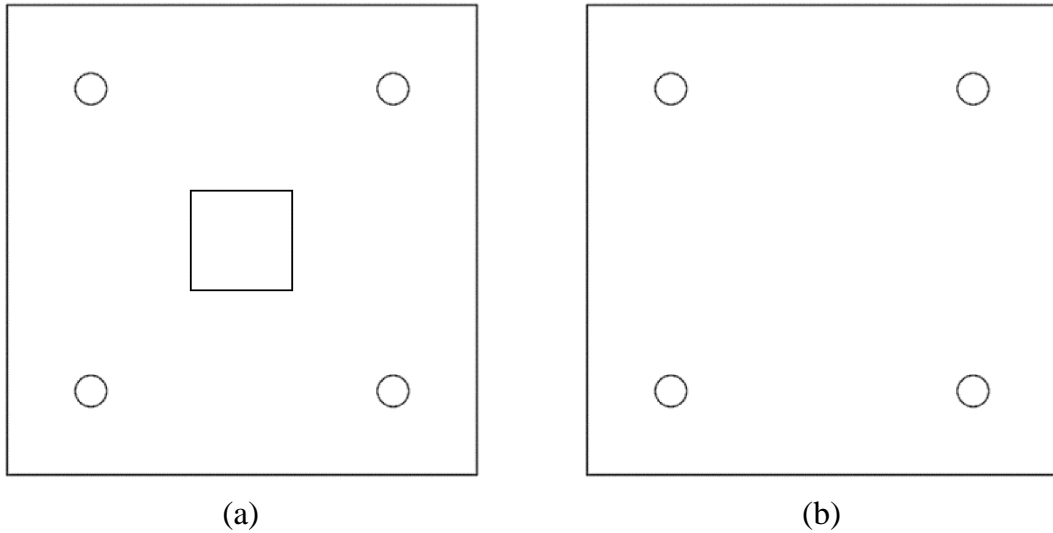


Figure 3.10: (a) Cutout of PCL370HR, (b) Cutout of 55NT and pacothane plus

- Step 2: Mounting all the materials on the Stainless-steel support with the order shown in Figure 3.11.

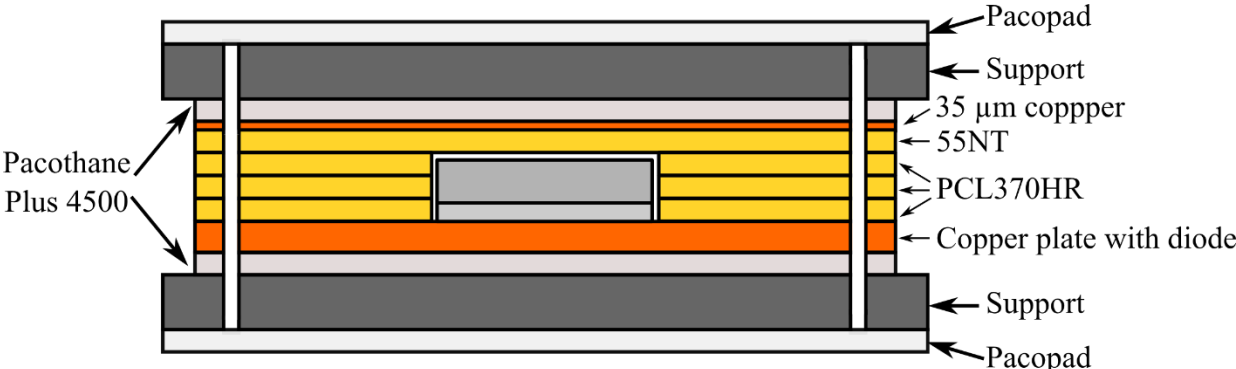


Figure 3.11: stack-up for the lamination of the PCB, corresponding to step (b) in Figure 3.3.

- Step 3: The support is then placed in a heated press (Figure 3.12), with the temperature profile shown in Figure 3.13.



(a)



(b)

Figure 3.12: (a) Inox support for press, with 4 registration pins for the alignment of the various layers from Figure 3.10, (b) the heating press used for PCB embedding

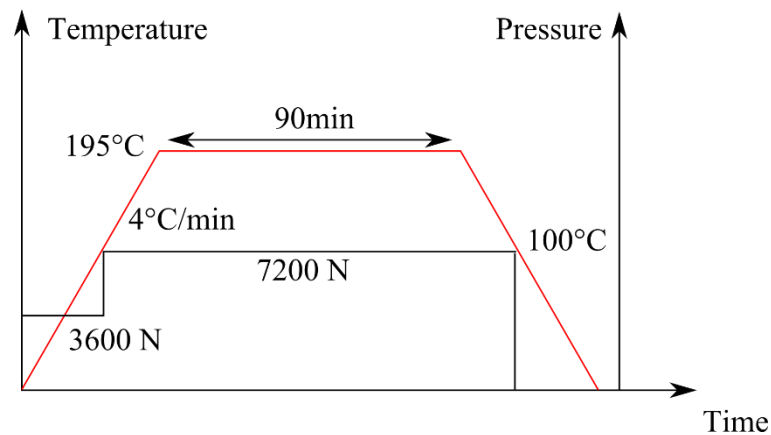


Figure 3.13: Temperature profile for PCB embedding. The PCB measures 60x60 mm², a force of 3600 newtons corresponds to a pressure of 1 Mpa (approximately 10 bars). 7200 N corresponds to 2 Mpa (20 bars)

The number of prepreg layers used depends on the thickness of the component. However, the thickness of the prepreg changes after lamination, as some of the resin flows out of the glass fiber material. This is due to several factors. Unlike copper, prepreg thickness varies across the width of panel. It is usually thickest at the center and thinnest at the edges [123]. Most of the variation can be accounted for if calculations are done for the thickest and thinnest possible outcome. Many parameters must be considered to calculate the final thickness of a prepreg layer:

- Glass style: the glass style used is the primary determinant of prepreg thickness. The Table 3.2 lists 3 glass styles used in the market and their characteristics.

Table 3.2: Characteristics of different glass styles [95]

Glass style	Density (g/cc)	Thickness (mm)	Basis Weight (g/m ²)
106	2.54	0.038	25
1080	2.54	0.064	49
2116	2.54	0.097	109

- “Resin content: this is a simple percentage, based on weight, of resin to glass. From resin density, glass density, glass basis weight and resin content, we can calculate the initial thickness range (Ho) for any given prepreg style using the following equation, where Wg is the Unit glass basis weight in g/m², RD is the Resin Density, GD is the Glass Density and RC is the Resin Content [123].”

$$H_o = \frac{W_g}{GD * 1 - \frac{RC/RD}{\frac{RC}{RD} + (100 - RC)/GD}}$$

Another method to obtain the thickness after lamination is proposed by Isola. It uses a software tool named Multical¹ which is designed to calculate insulation distance between the copper conductor tracks as well as the total thickness within the multilayer for the products offered by Isola. In this tool, we can choose the prepreg type, the copper thickness, and its percentage (as some of the copper is etched away to form the layout, only a fraction of the copper layer remains) determine the number of prepreg layers required during the lamination. Figure 3.14 shows an example using this program to calculate one prepreg layer thickness of the PCL370HR with the glass style 1080.

¹ <https://isodesign.isola-group.com/multical>

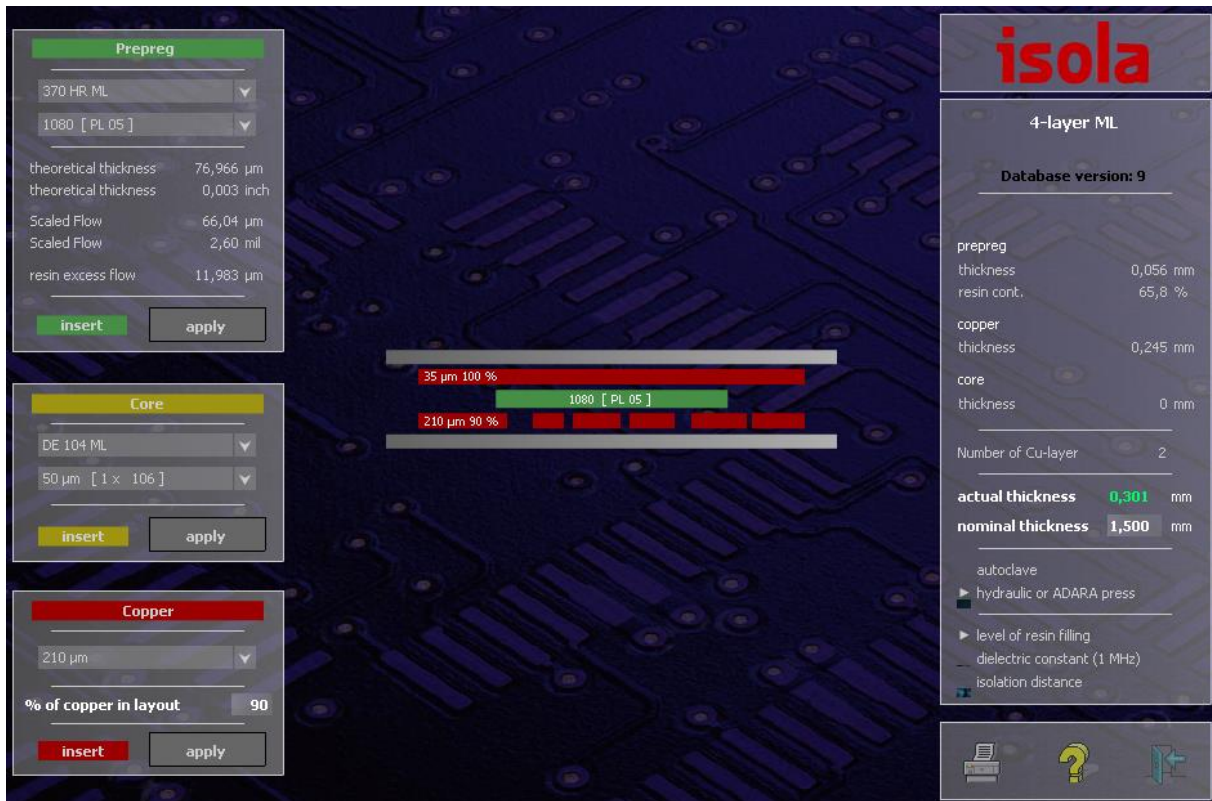


Figure 3.14: An example of the digital tool Multical by isola

3.3.5.2 Etching

After lamination, the topside copper layer is etched away to open a window corresponding to the pads of the embedded die. This step requires proper alignment with the die, but this remains less demanding than any High-Density Interconnect (HDI) multi-layer PCB, which are commonplace nowadays. A positioning accuracy of 100 µm is sufficient to match the smallest pad size of a power die (typically the gate contact on a MOSFET or an IGBT, which is designed to be connected with a 100-125 µm wedge wirebond).

Preparation

The PCB substrate is initially heated in an oven with a temperature of 70°C for 15 min. Then a layer of photosensitive film (Dupont Riston T220) is attached to the PCB substrate by a laminator. Its photo and its function are shown in Figure 3.15. The substrate and the film are pressed together between two heated contra-rotating rolls. The distance between these two rolls is changeable in order to adjust the applied pressure. The temperature of the rolls is set to 80-90 °C.

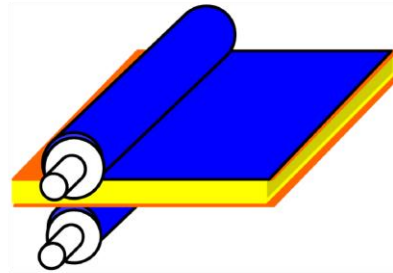


Figure 3.15: Photography of a film laminator and its principle function [96]

Exposure

This step is realized by a double UV-Exposure unit – DFT 3040 (C.I.F). Its photo and that of one of the masks used during the fabrication process are shown in Figure 3.16. The Riston T220 is a negative type film, therefore, the patterns that we want to form are transparent on the mask and the zone where the film will be eliminated are black. The exposure time is set to 22 s.

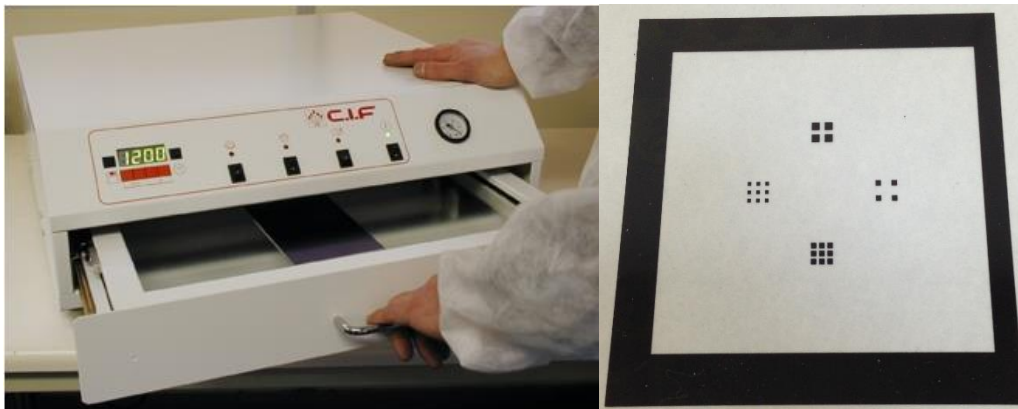


Figure 3.16: Photography of exposure machine [21] and a mask example

Development

According to its documentation [124], the film Riston T220 is developed in sodium carbonate (Na_2CO_3) for 3 minutes. The operation temperature of this step is 25 – 27 °C. As the film is negative, the non-exposed parts are eliminated by the developer.

3.3.6 Laser ablation

Laser ablation of the laminate material is performed on a Gravograph LS100EX (shown in Figure 3.18) 60 watt CO₂ laser. For a given material, the ablation is controlled by three parameters: the sweep speed of the beam (i.e the moving speed of the laser), the power of the laser beam, and the number of passes. Two preliminary tests were performed on an aluminum surface (same material as the topside metallization of the die) regarding the effect of the sweep speed and power of the beam. In the first test, we fixed the speed to 80% of the maximum value, and changed the power from 55% to 95%. The second test

fixed the power to 75% and swept the speed from 80% to 40%. The results of these two tests are illustrated in Figure 3.19 and Figure 3.20. They showed that the parameters of the laser had little influence on the quality of the result, providing the beam is slow enough or powerful enough to remove the organic material. In all cases, we did not observe any change in the appearance of the aluminum. This is very interesting, as it demonstrates a very good selectivity of the laser ablation: it easily removes the laminate, but stops completely once it reaches the die. Another advantage of this good selectivity is that we can use the laminated copper layer as a mask for the laser ablation process: there is no need for accurate alignment of the laser with the chips; a coarse positioning is sufficient, providing the laser sweeps an area larger than the openings in the copper layer (shown in Figure 3.17). As the ablation is performed in air, cleaning in isopropanol is required to remove some residues. We have also tried using a protective atmosphere (N_2 injected using a nozzle located near the laser head) which was expected to help reducing these residues, however, we did not note any improvement in results compared to the air.

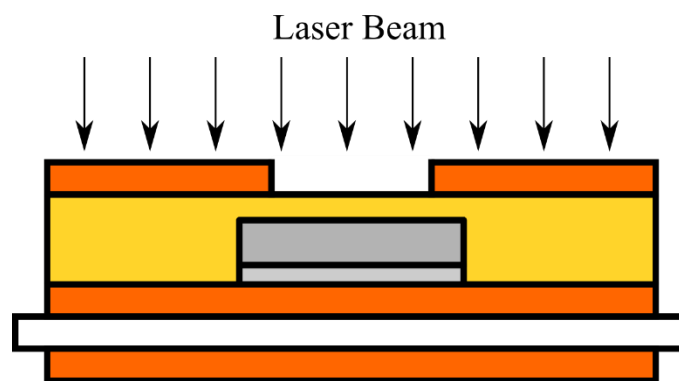


Figure 3.17: Copper layer as alignment mask



Figure 3.18: Gravograph LS100EX laser

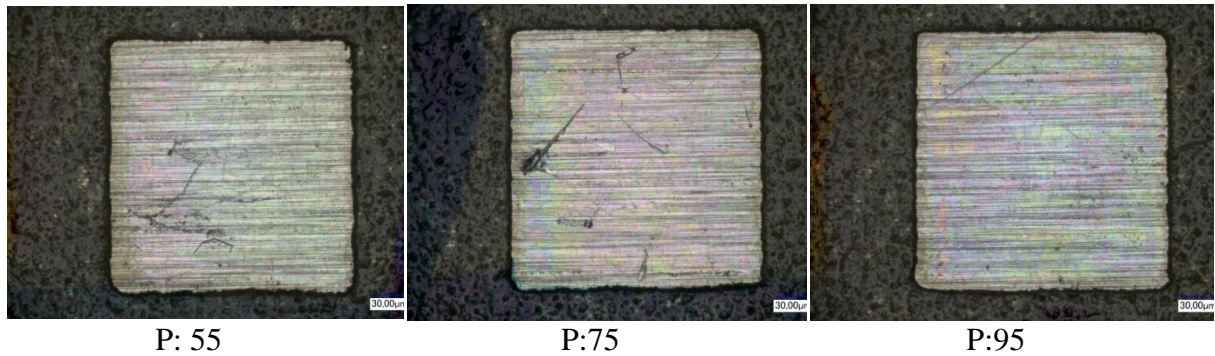


Figure 3.19: photos of aluminum surface after laser ablation with different power values, for a sweep speed of 80%. No difference in appearance of the aluminum surface is noted.

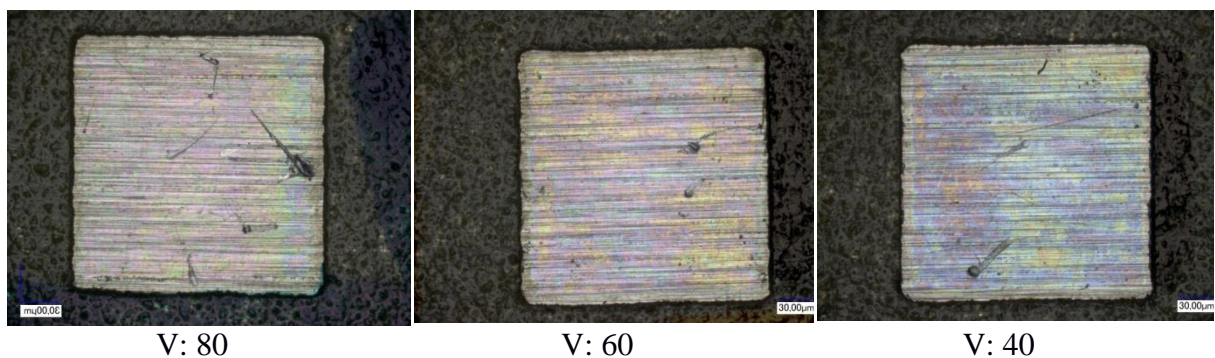


Figure 3.20: photos of aluminum surface after laser ablation with different speed values, for a power of 75%. No difference in appearance of the aluminum surface is noted.

3.3.7 Metallization

The last step of the embedding process is the electroplating of a copper layer over the entire surface of the PCB, including the die cutouts (Figure 3.3(f)). We use a standard “plated-through-hole” process (Bungard) [125].

- Step 1: 7 minutes in the DS270 solution with agitation, and a temperature of 65 to 70 °C.
- Step 2: Static Rinse of the PCB substrate for 1 minute and then spray rinse for another 1 minute.
- Step 3: 1 minute in the DS400 solution with agitation. This step is realized at ambient temperature. The DS400 solution is used as a pre-dip before the Activator DS500.
- Step 4: 7 minutes in the DS500 solution with a slow agitation and in the room temperature.
- Step 5: Repeat the Step 2.
- Step 6: 4 minutes in the DS650 solution with a temperature of 45 °C. The DS650 solution is an intensifier.
- Step 7: Spray rinse for 1 minute.
- Step 8: 20 minutes (this is the standard electroplating time value, it can be adjusted depending on the copper thickness desired, and this time corresponds a copper thickness off 15 μm) in the copper bath CU400. The flowing current is 2.5A/dm².
- Step 9: Spray rinse for 1 minute.

The cross-section of a metallization example is presented in Figure 3.21. We can see clearly the vertical walls in epoxy layers,

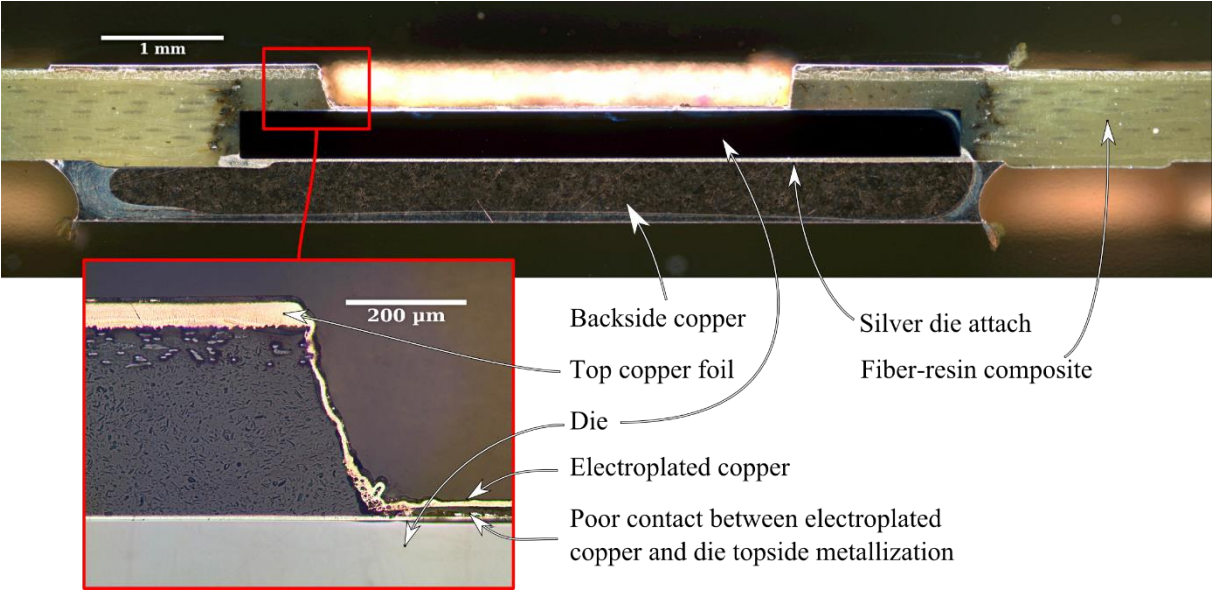


Figure 3.21: Cross-section of a sample after metallization, taken at the edge of the exposed pad. The wall of the copper electroplated on the die is clearly visible

In order to evaluate the effect of the die topside metal composition, two series of tests have been performed. The first set is the comparison of different plating times. The surface roughness of the metal on top of the dies was measured using a stylus profilometer. Figure 3.22 shows the roughness measurement for the aluminum topside finish of the die, this measurement is a reference for comparing the metallization performance.

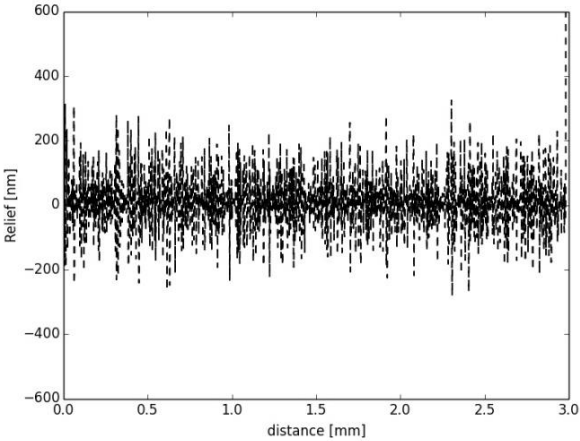
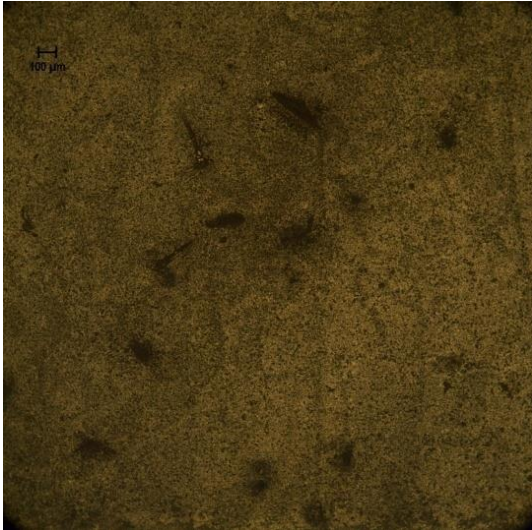
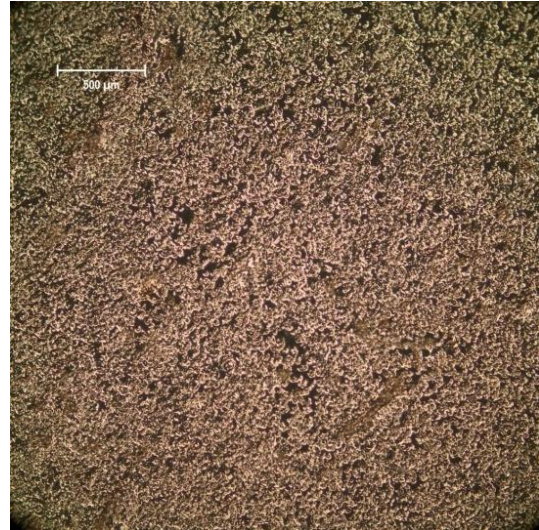


Figure 3.22: Roughness measurement for aluminum topside finish of the die before metallization

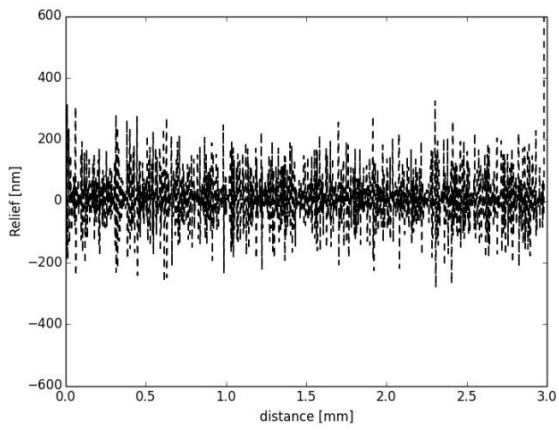


5 min copper plating on aluminum

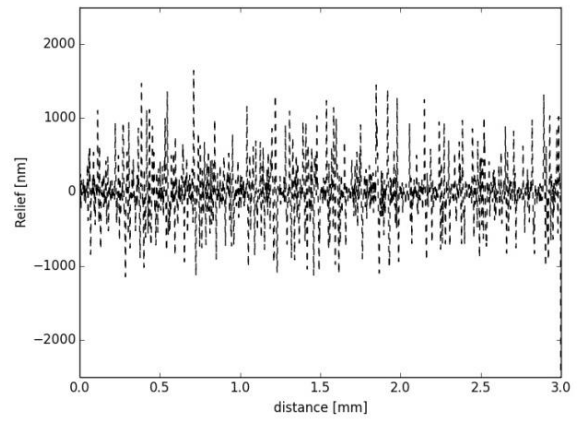


30 min copper plating on aluminum

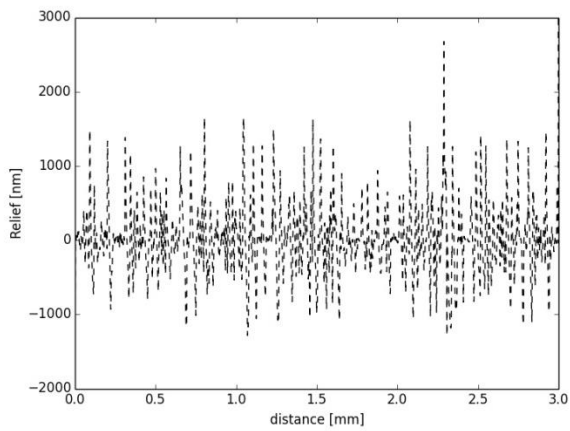
Figure 3.23: Photo of the metallization surface on aluminum with different copper plating times



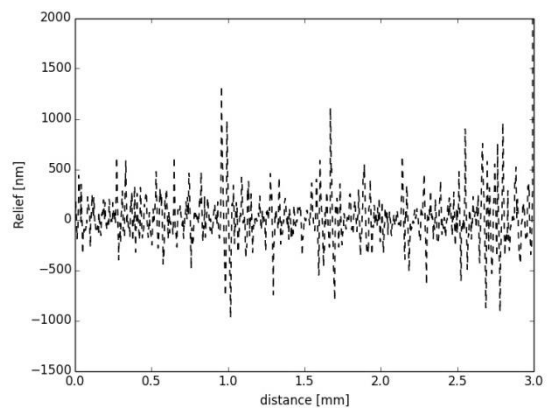
Aluminum topside before copper plating



5 min copper plating on aluminum



20 min copper plating on aluminum



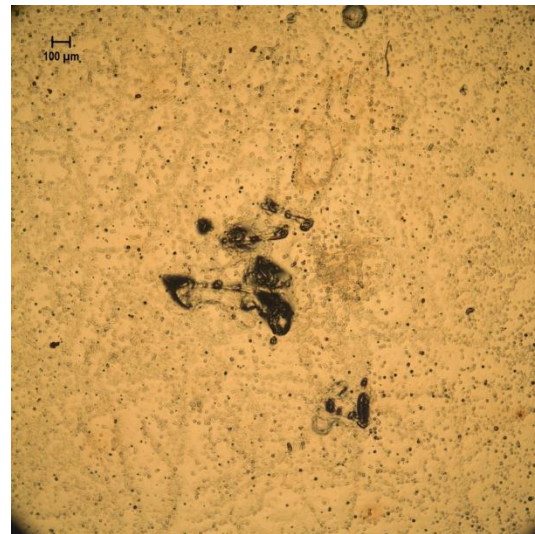
30 min copper plating on aluminum

Figure 3.24: Roughness measurements of the copper surface on aluminum with different plating times

This first series of tests concerns an aluminum chip topside with different plating step durations. 20 minutes is a standard metallization time, however, the roughness is not ideal. As a consequence, we have also realized 5 minutes and 30 minutes metallization. As we can see in the images, the metallization of 30 minutes is brighter than which of the 5 minutes, however, the surface of these two samples are not very smooth. According to the roughness measurement, most of the relief in the case of 30 minutes is concentrated in the range from -500 nm to +500 nm, in the case of 5 minutes, the relief is around from -1000 nm to +1000 nm. The surface roughness of these three metallization times are much worse than that of the aluminum topside before copper plating.

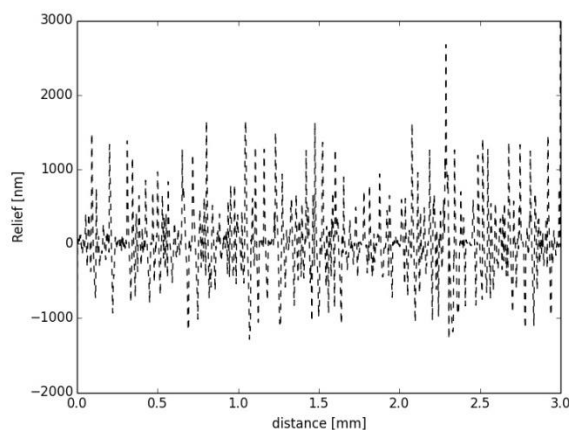


20 min copper plating on aluminum

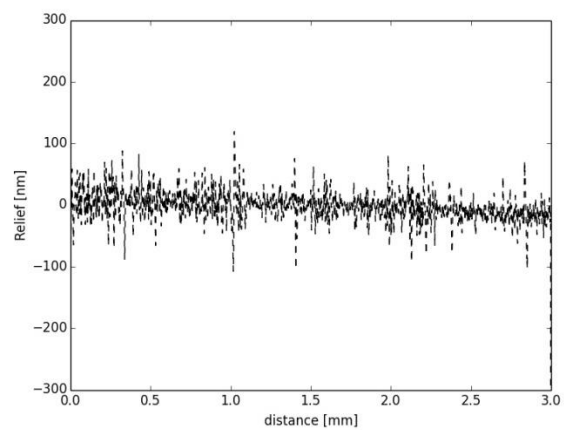


20 min copper plating on copper

Figure 3.25: Photo of the metallization surface for dies with aluminum and copper finish with 20 minutes metallization



20 min copper plating on aluminum



20 min copper plating on copper

Figure 3.26: Roughness measurement on metallization surface for aluminum and copper finish with 20 minutes metallization

The second series of tests is about two dies as described in the section 2.3.2: the first set was used as supplied (with an aluminum topside finish), while the second set received a PVD plating (50 nm Ti/140nm Cu) over its aluminum topside metallization. The copper plating time is 20 minutes for both of them. The results show that the assembly with the

second chip seems satisfying (visual control, the copper surface is shiny, while it is dull for the first chip) and its roughness is about 10 times less than that of the first chip.

As a consequence, and despite it requires an extra processing step, a Ti/Cu plating of the dies seems necessary to improve the quality of the topside contact in our embedding process. This is in agreement with some of the processes described in the introduction, which require copper-finished dies. These are becoming more common nowadays, because of the development of copper wirebonds, but they remain a minority compared to aluminum-finished dies.

3.4 Static characterization of the embedded diode

The static characterization of some embedded diode samples (shown in Figure 3.27) is presented in Figure 3.28. The forward characteristic is acquired using a Tektronix 371 tracer, with 4-points connections to the PCB substrate. The tests are performed in air without any additional passivation. The forward results (shown in Figure 3.28(a)) indicates that die finish and electroplating time have a strong effect on characteristic, the diode with copper finish and 20 minutes electroplating has lower resistance than the two others. This confirms a better quality of the electroplated copper when using Ti/Cu-finished dies.

The reverse characteristic (Figure 3.28(b)) was measured using a Keithley 2410 high-voltage SMU up to 1100V (limited by the equipment). A second measurement was performed using the Tektronix 371A in high voltage mode. This second measurement is much less accurate, but indicates that the breakdown voltage of this embedded die occurs at around 1350 V, which is consistent with the 1200 V rating of the diode. This shows that no arcing was detected, and that the embedding of the die constitutes a satisfying encapsulation. Further work is required to assess this encapsulation, especially in presence of moisture or after thermal cycling.

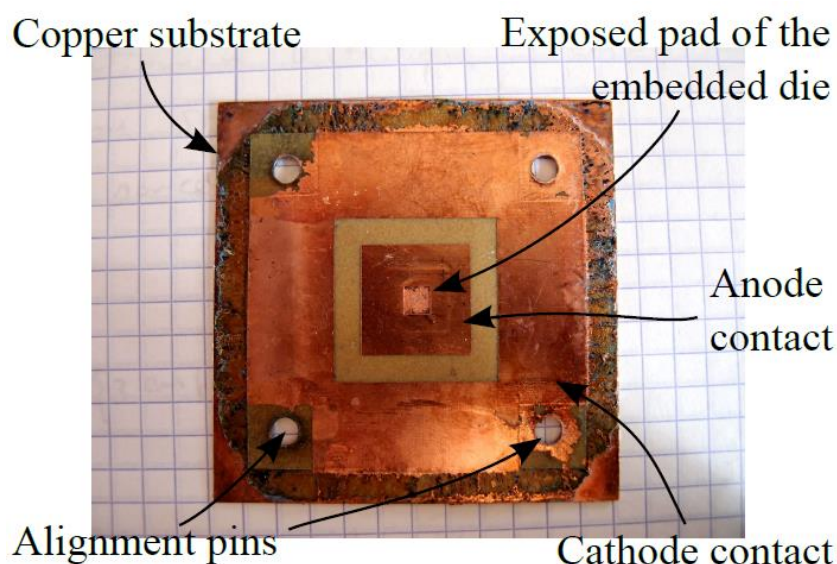


Figure 3.27: Sample used for electrical characterization (60×60 mm²).

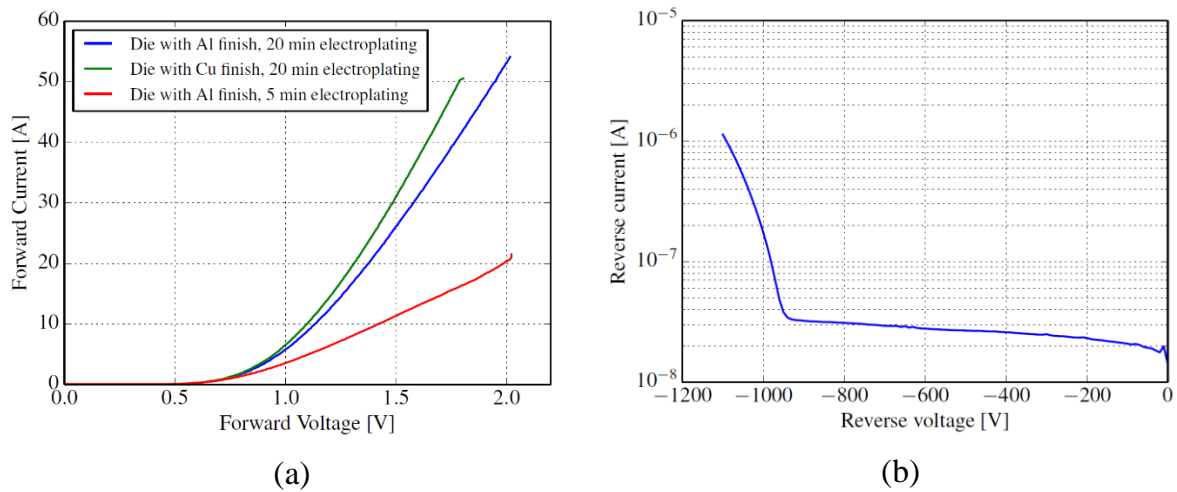


Figure 3.28: Electrical test of an embedded diode

3.5 Analysis of electric contact

As presented above, the manufacturing parameters have a strong impact on the electrical resistance of the contact. Here, we assess the effect of the shape of this contact, for Ti/Cu-finished dies. In fact, a non-homogeneous current distribution could cause a hot spot in the chip, and produce its destruction in the extreme case [126]. Even without reaching such extremes, a low contact resistance is desirable, and it is interesting to find what is the effect of the layout of the contact has on the resistance. In this chapter, we will focus on the contact resistance and current distribution in a diode embedded in PCB, as a function of the layout of its topside contact. We demonstrate that by choosing a suitable contact layout, it is possible to achieve a very low contact resistance.

Figure 3.29 presents a 3-D view of the test vehicles (the fiber-resin composite which encapsulates the dies is not show for better clarity). Here, 4 openings were made in the topside copper layer, resulting in 4 contact “wells” with the die. A cross section shows in Figure 3.30 that the copper layer is thicker on top (because it is formed by a $35\ \mu$ copper foil, on top of which some more copper is electroplated). The walls and floor of the wells are only formed by the electroplated copper and are therefore thinner ($7\ \mu$).

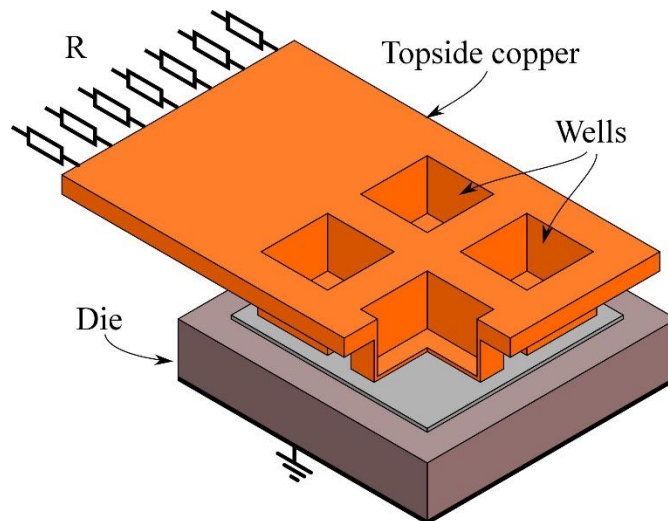


Figure 3.29: 3D view of the test vehicles

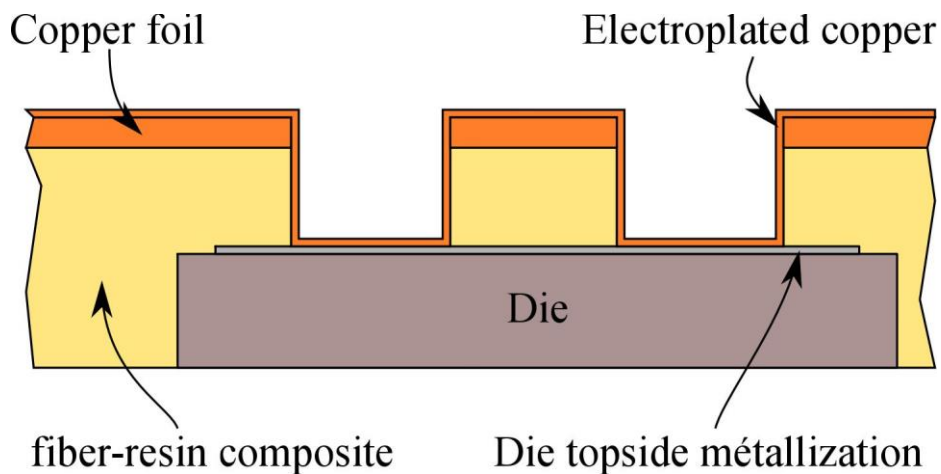


Figure 3.30: Cross-section of the second test vehicle

As a consequence, the layout of the wells is expected to have an influence on the resistance of interconnects: small wells take leave more (thick) topside copper, but offer small contact area with the die. A single well can maximize the contact area with the die, but removes a large part of the topside copper, and only has limited wall surface on the wells. A small, single well will result in a poor current distribution on the die surface. For practical reasons, not all the configurations can be made. In particular, we fixed a minimum well dimension of $1 \times 1 \text{ mm}^2$, and left a 1 mm margin on the edge of the diode (we consider a $4 \times 4 \text{ mm}^2$ useable area out of a $6 \times 6 \text{ mm}^2$ die).

3.5.1 Modelling

The calculation of the contact resistance is performed using a Python script (ANNEX B). The conductors in the structure are divided in $100 \times 100 \text{ }\mu\text{m}$ elements in which unidirectional current flow is assumed. These elements are connected to form an equivalent resistance network, and calculations based on the modified nodal analysis² are performed

² <http://www.swarthmore.edu/NatSci/echeeve1/Ref/mna>

to simulate the current distribution. A 2-D circuit diagram is presented in Figure 3.31. It shows the various resistances considered in the calculations:

- R_{top} is the resistance of the top copper layer, whose thickness is that of the initial copper foil (35 μm), plus the electroplated copper layer (here 7 μm);
- R_{wall} is the resistance of the “walls” and the “floor” of the wells. Here, the thickness considered is that of the electroplated copper only, and the well are 40 μm deep;
- R_{Al} is the resistance of the aluminum topside metal layer (3 μm thick) of the die (the thin PVD Ti/Cu layers are considered negligible);
- R_{die} is the equivalent resistance of the die. We consider the silicon to be uniformly doped at 10^{19} cm^{-3} , corresponding to a resistivity of $6 \cdot 10^{-5} \Omega\text{m}$, with a die thickness of 400 μm . This is very coarse assumption, which causes probably most of the mismatch between the resistance values in simulation and experiment;
- R_{access} is a resistance added between the voltage source and the nodes on one of the edges of the top copper layer. Its value is chosen equal to R_{top} ;
- R_{cont} is the contact resistance between the copper layers and the die. By default, it is considered negligible (1 $\text{n}\Omega$).

In each of the layer, the resistance of each element is simply calculated as

$$R = \frac{\rho l}{dw}$$

With ρ the resistivity of the material (16.78 $\text{n}\Omega\text{m}$ for copper, 28.2 $\text{n}\Omega\text{m}$ for aluminum, 65 $\text{n}\Omega\text{m}$ for silicon), l the length of an element, d its thickness, and w its width.

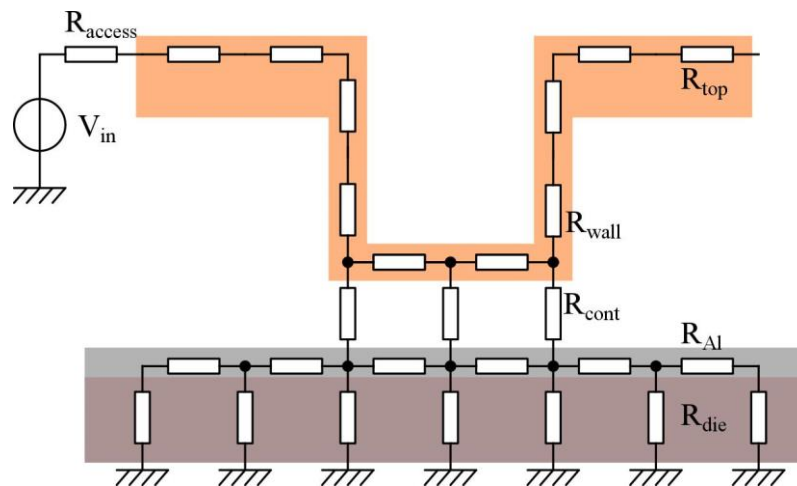


Figure 3.31 : 2-D view of the resistance network used to represent the test vehicles.

The results of the calculations for the various configurations of the test vehicles are presented in Figure 3.32, and the corresponding resistance values are given in Table 3.3.

Table 3.3: Contact resistance for the different layouts presented in Figure 3.32

Number of contacts	Surface (mm ²)	Resistance (mΩ)	Image in Figure 3.32
1	1	3.80	(a)
1	4	2.16	(b)
1	9	1.55	(c)
1	16	1.32	(d)
4	4	1.40	(e)
4	9	1.26	(f)
7	9	1.13	(g)

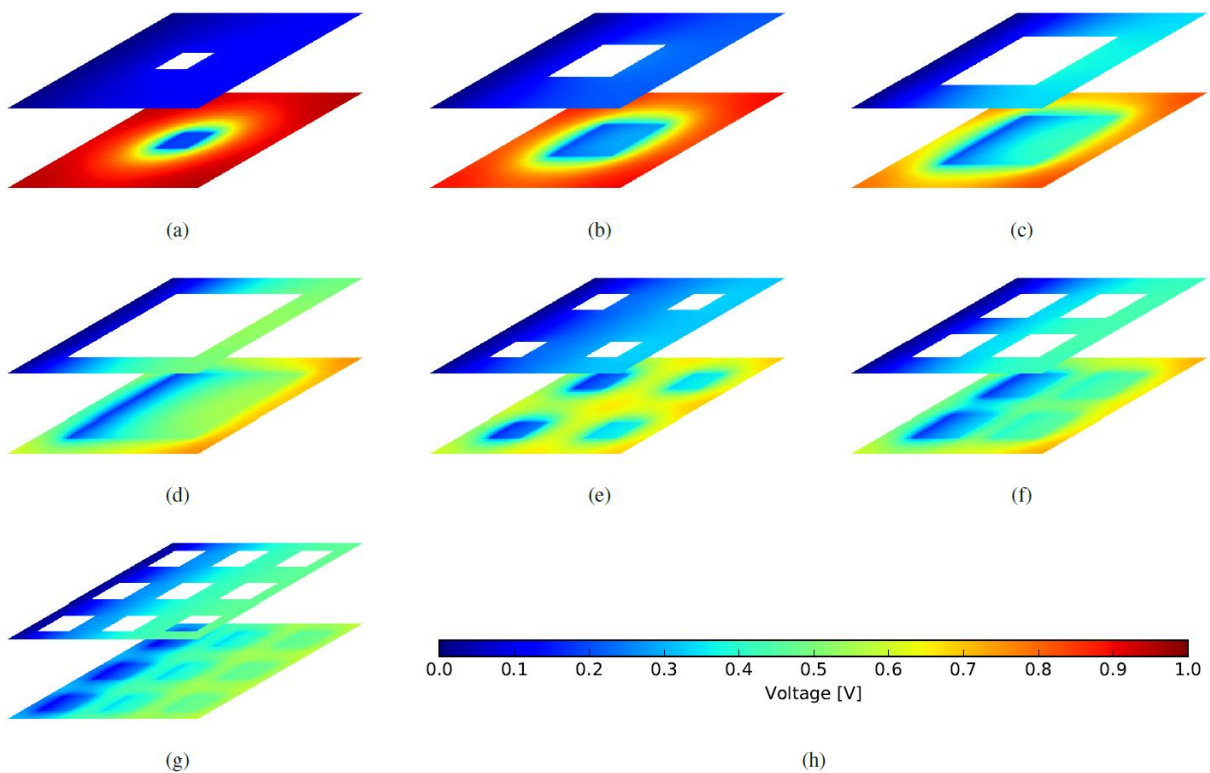


Figure 3.32: Simulation of the voltage distribution on the PCB top copper layer and on the topside metallization of the die, for various contact layout configurations (the walls are not shown). Current is injected on the left side on the top metallization, and on the backside of the die

3.5.2 Experimental measurement

Experimental characterization of the test vehicles (an example is shown in Figure 3.33) was performed using a Tektronix 371A Curve tracer, using 4-point connections and pulse

mode, with maximum current of 100 A. Two sets of curve are given in Figure 3.34 and Figure 3.35. From these measurements, we identified the dynamic resistance of the diode. As a comparison, earlier studies [127] found that a packaged (TO247) version of the diode has a dynamic resistance of 4.4 m Ω .

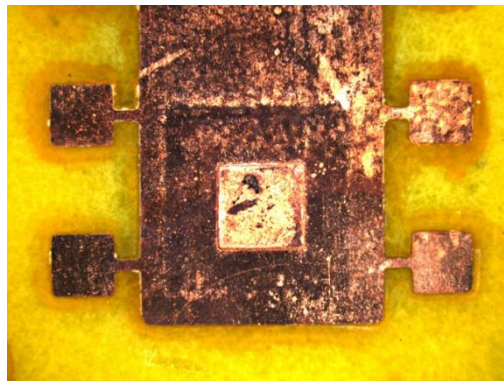


Figure 3.33: Close-up of one of the embedded dies, with a contact window of 3 \times 3 mm²

The resistance values obtained experimentally are presented in Table 3.4. They are much higher than the calculated ones: between 16.5 m Ω and 4.38 m Ω experimentally, versus 3.8 m Ω - 1.13 m Ω in simulation. This can be due to several factors: many parameters of the simulation are based on assumptions, and in particular the equivalent resistance of the diode itself is probably not correct. Another issue might be the contact resistance between the aluminum topside metal of the diode and the electroplated copper (this is discussed below).

However, even with this large difference between experiments and calculation, some conclusions can be drawn:

- The surface plots in show that when a single well is used, most of the voltage drop occurs on the topside metal of the die. This is especially true for 1 mm² wells. As the well grows, the resistance drops 4 times in measurements (from 16.5 m Ω at 1 mm² down to 4.65 m Ω at 16 mm²) and 3 times in simulation (from 3.8 m Ω to 1.32 m Ω).
- Multiple contacts allow for a better current spreading over the die metallization, even with smaller contact area: in table 1, 4 and 9-contact versions (the last three lines of the table) offers resistance of 1.4 to 1.13 m Ω , comparable to that of a single well with 16 mm² area, with a fourth to a half of the surface (4 or 9 mm²). Similar results can be observed from the experiments in table 2, although with more variation.
- The poor contact between the electroplated layer and the die topside metallization, visible in the close-up view in Figure 3.21 is probably responsible for a large part of the difference between the simulations and measurements. Running the simulations with a much higher contact resistance value (1 Ω instead of 1 n Ω for a 100 \times 100 μ m² element) results in calculated values much closer to the measurements (between 2.3 and 17 m Ω).
- In theory, it is possible to achieve contact resistance much lower than those obtained with wirebonds (4.4 m Ω). The best measurements described in Table 3.4 are already better than regular wirebonded devices, despite the poor copper/die interface.

Investigations shows that the poor quality of the electroplated/die interface seems to be caused by the plating process: after the laser ablation, the exposed surface of the die retains a copper color (Ti/Cu PVD layers were applied to the dies prior to embedding). The plating process, however, uses a series of baths, some of which having aggressive action to ensure the surface to be plated are clean. It is probably one of those bath which degrades the PVD layers and causes poor adhesion between the die and the electroplated copper. Increasing the thickness of the PVD copper layer from 150 nm to 500 nm helped reduce the resistance form 9.89 mΩ for a 4 mm² contact down to 5.64 mΩ (all the results presented here are with 500 nm PVD copper layer).

Table 3.4: Resistance measurements. 2 test vehicles were used for the “single contact” cases, 3 test vehicles were used for the remaining

Number of contacts	Surface (mm ²)	Resistance (mΩ)	Min (mΩ)	Max (mΩ)
1	1	16.5	13.6	19.15
1	4	5.64	4.66	6.62
1	9	4.85	4.26	5.43
1	16	4.65	4.48	4.83
4	4	5.38	4.49	5.72
4	9	4.38	4.14	4.55
7	9	5.18	4.27	5.80

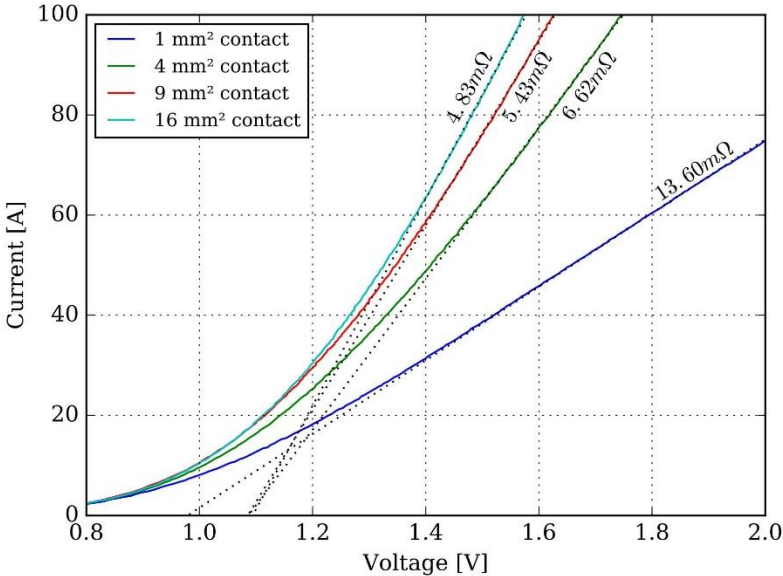


Figure 3.34: Forward characteristic measured on test vehicle which comprises single well layouts with a surface ranging from 1 to 16 mm²

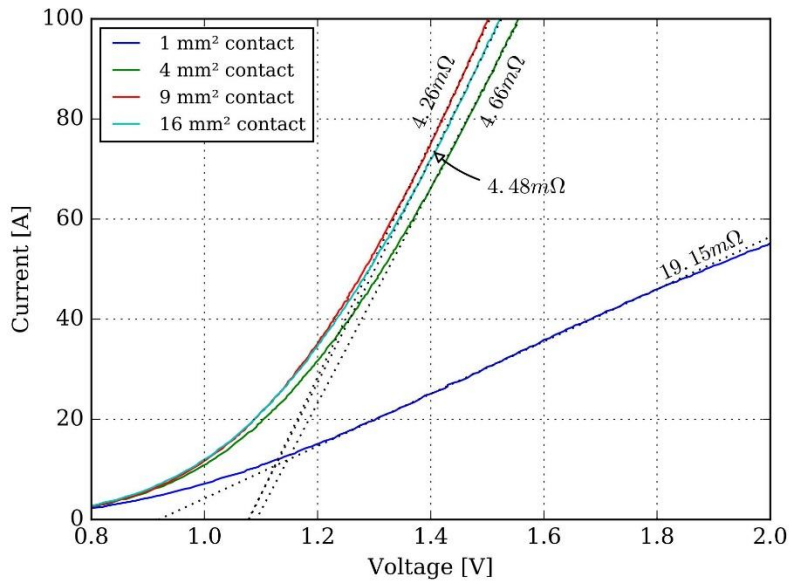
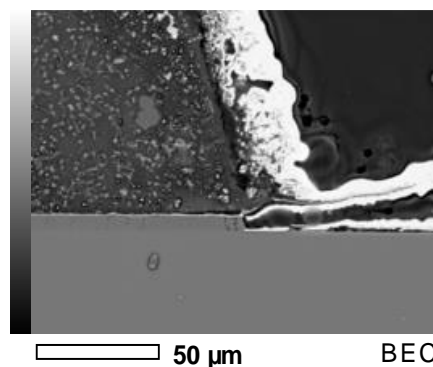


Figure 3.35: Forward characteristic measured on test vehicle with the same layout as the test vehicle shown in Figure 3.34. Here, the 9 mm² contact is found to offer a lower resistance than the 16 mm² contact

In order to find the potential problems in the fabrication of this prototype, the scanning electron microscope (SEM) used. This type of microscope uses the electrons beam to scan the sample, producing the information about sample's surface topography and composition. Figure 3.36 (a) shows the microscopic photo of the cross section of the prototype, as we can see, the interface between the metallization and the top side layer of the die is not perfect yet, the contact between this two parts is not well established. Figure 3.36 shows the Cu element in this photo, we can notice that the region between the metallization and the die is black, this means that there is no copper in this part. Figure 3.36 (c) shows the Al element in the photo, which normally covers all the topside of the die. However, we can see that the Al part located below the window has been removed, this is because the chemical attack during the Cu electroplating.



(a)

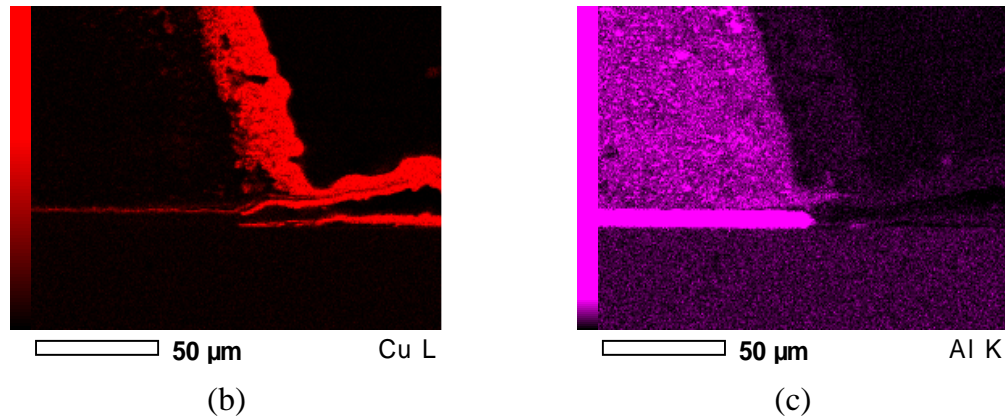


Figure 3.36: SEM analysis for the half-bridge prototype, (a) the microscopic photo, (b) Cu element in the photo, (c) Al element in the photo

3.5.3 Conclusion

In this section, we have firstly introduced the embedding process we used in the laboratory, based on prototyping-scale PCB equipment. Some important steps in this process are presented. The laser ablation works very well to remove the prepreg materials through a window in the metal layer. The Ti/Cu metallization of the topside of the die prior to embedding is very important, as it improves the copper electroplating. This electroplating step is not yet satisfying, as it creates a poor interface between copper and die, but reasonable contact resistances are achieved yet. The analysis of the effect of the contact area and its layout has been realized. It indicates that it is more important to distribute the contacts over the die surface than to have large contact surfaces. With a proper layout, the contact resistances can be lower than those achieved with aluminum wirebonds.

3.6 Half bridge prototype

The last section has proved that the embedding technology allows to achieve very low interconnect resistances, providing the topside contact the dies allow for a good spreading of the current. The resistances are lower than those offered by standard thick-wire aluminum wirebonds, although improvements are required at the electroplated copper/die interface. According to this performance, a half-bridge power module based on the PCB embedded technology has been designed. Considering the high voltage application, we will use the 1200 V power components. The IGBT we used has been already studied in the laboratory and it has a large gate surface which can facilitate the fabrication. The diode in parallel with the IGBT is a SiC device for its good switching performance. The prototype also includes the driver and its auxiliary parts for the demonstration and a DBC substrate is used in order to have a better cooling capability of the power devices.

The electric circuit diagram and a photograph of a fabricated example are shown in Figure 3.37 and Figure 3.38. The fabrication process of this prototype is nearly the same as the two test vehicles introduced before in this chapter. The main differences here are the use of Electronic Design Automation (EDA) tools to route this more complex circuit and generate the fabrication files, and the more complex contact pattern, as we have 4 smaller

dies to embed, some of which have small gate contacts. In order to realize this prototype, we used a CAD tool named Kicad to draw the layout and generate the masks. This tool allows automatic routing, adaptable design rules and generation of the manufacturing data such as position of dies, cavities, or laser drilling at once. At the moment, however, Kicad is not designed to handle devices embedded in PCB (as do some CAD tools, such as Altium).

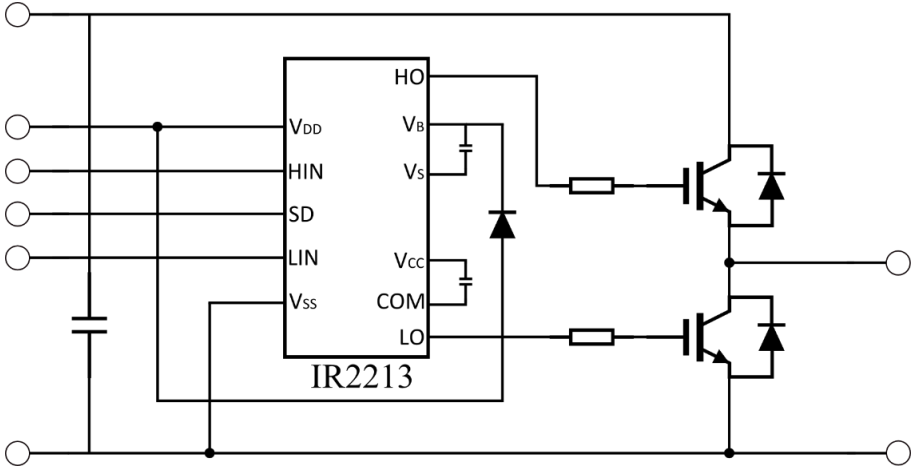


Figure 3.37: Electric circuit diagram of the half-bridge prototype

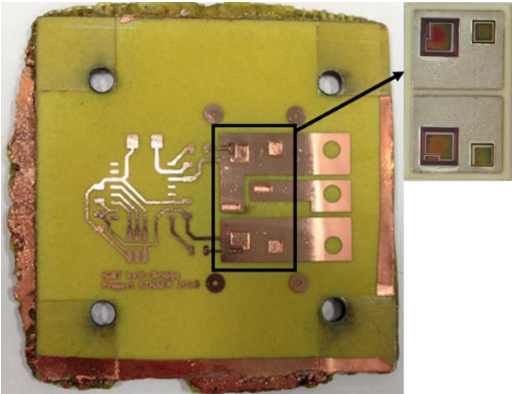


Figure 3.38: Photograph of a half-bridge module. The DBC (with 2 IGBTs and 2 SiC diodes) is shown in the upper right corner prior to embedding.

3.6.1 Layout adaption for component surface

To ensure the proper operation of the module, it is necessary to provide good contacts on both sides of the power components. From a geometry point of view, the electric contact between the bottom side of the chips and the DBC substrate does not present any practical issue. It is the contacts with the top copper layer that must be focused upon. We present here the specific features of the IGBT and diode we used.

3.6.1.1 IGBT

The switches we used for the half-bridge module is an IGBT rated at 1200V/15A from International Rectifier (IR). Its dimension is $4.9 \times 4.9 \text{ mm}^2$ and it is $190 \mu\text{m}$ thick. An image of its topside surface geometry is presented in Figure 3.39 to understand the potential difficulties. Compared to other vertical IGBTs, the gate of this one is large enough ($2.01 \times$

0.8 mm²) for our relatively coarse alignment capability, where the tolerance can reach more than 500 μm. It is located in the corner of the die.

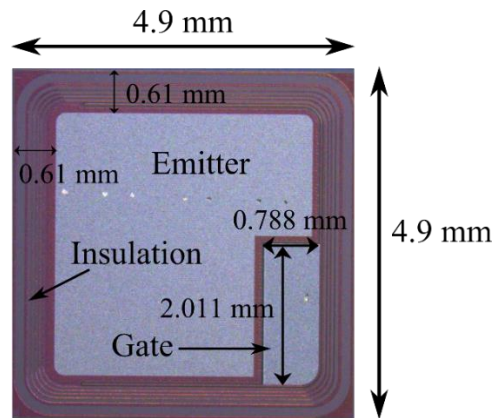


Figure 3.39: 1200V/15A Si IGBT

3.6.1.2 Diode

The diode used here is from CREE, with the reference of CPW4-1200S020B, 1200V/20A, a dimension of 3.08 × 3.08 mm² and a thickness of 377 μm. It is shown in Figure 3.40. We can notice that the metallization does not cover all the top surface of the component. As with the IGBT, the periphery is designed to sustain the blocking voltage of the device. Therefore, the embedding process should left these edge protections untouched.

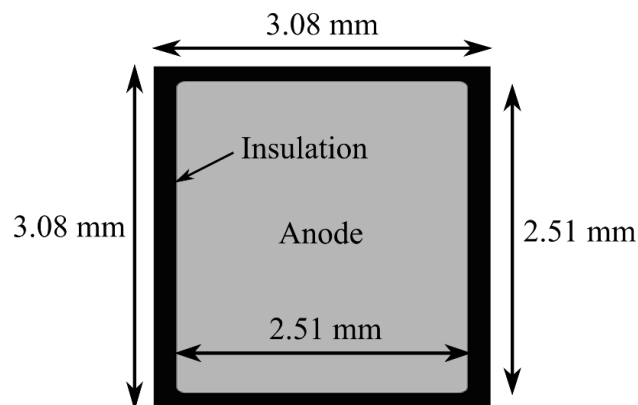


Figure 3.40: 1200V/20A SiC diode

3.6.2 Process flow

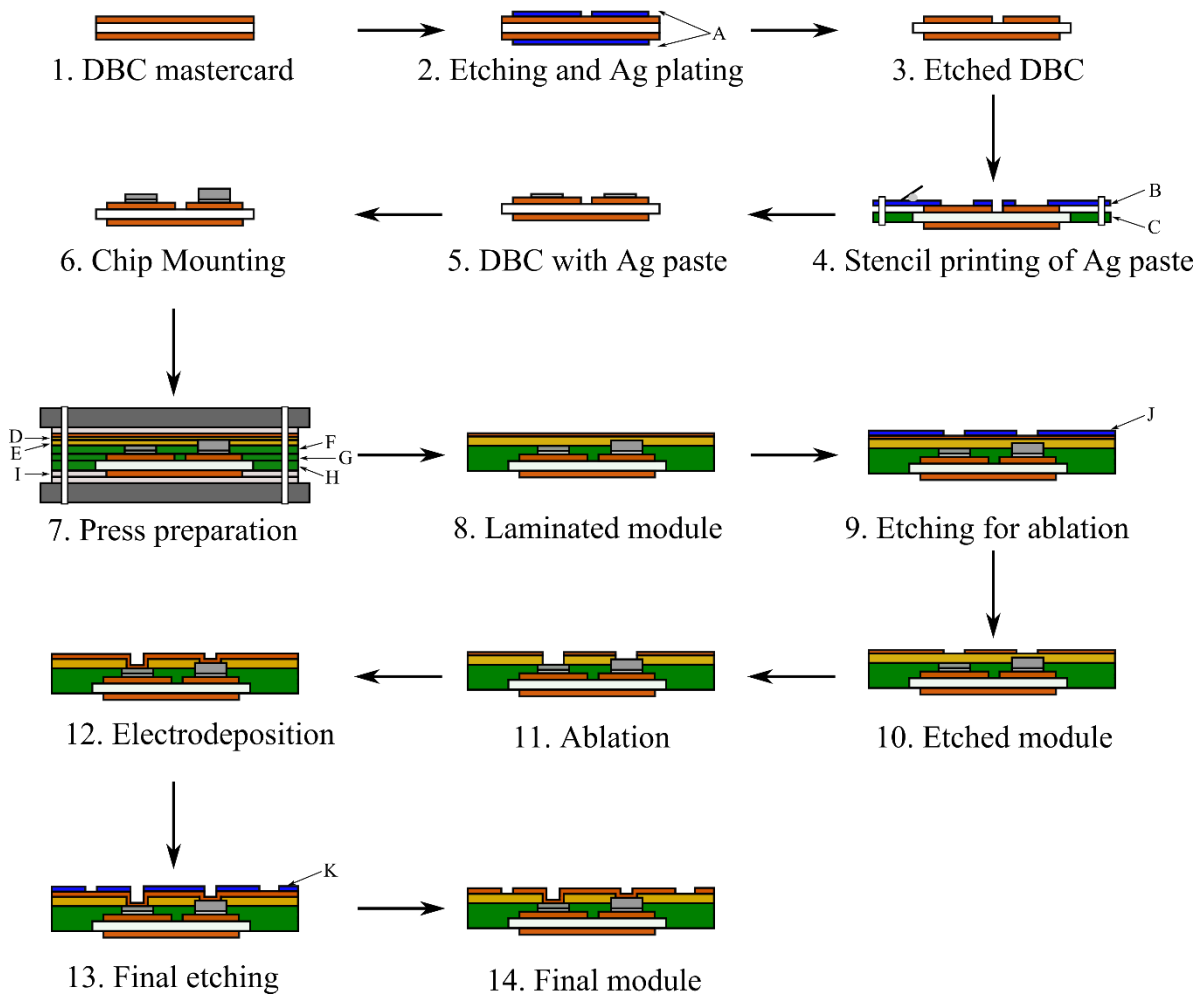


Figure 3.41: Fabrication process flow of the half-bridge prototype

Figure 3.41 shows the fabrication process of the half-bridge prototype. The letters from A to K represent pieces used in fabrication, and these pieces will be presented in the next section and shown in Figure 3.42. This process is nearly the same as described in the section 3.3, however, as this prototype needs better accuracy for component assembly, we have created a special mask (B) and a support (C) for Ag sintering.

The topside and bottom side copper of the DBC are firstly etched with the suitable mask (A) and Ag deposited. Many individual substrates are made at once (panelized design) using on a DBC mastercard. The ceramic of the mastercard is then cut half-way using a wafer saw (Disco DAD 3220), and cleaved to form groups of 6 individual DBC substrates. Then, the power components are assembled by Ag sintering, the mask (B) and the support (C) are designed for sintering 6 DBC substrate at once, and to provide suitable alignment. After that, the DBC substrates are singulated (by cleaving) and one of them is stacked with different layers (PCL 370HR, Arlon 55NT, Pacoplus 4500, etc). The form of different layers correspond the letter from D to I. Next, the topside copper is etched (with the mask J) and the Arlon layers are ablated. Afterwards, the electrodeposition is realized. Finally, the total electric circuit is formed by etching with the mask K.

3.6.3 Manufacturing data generation

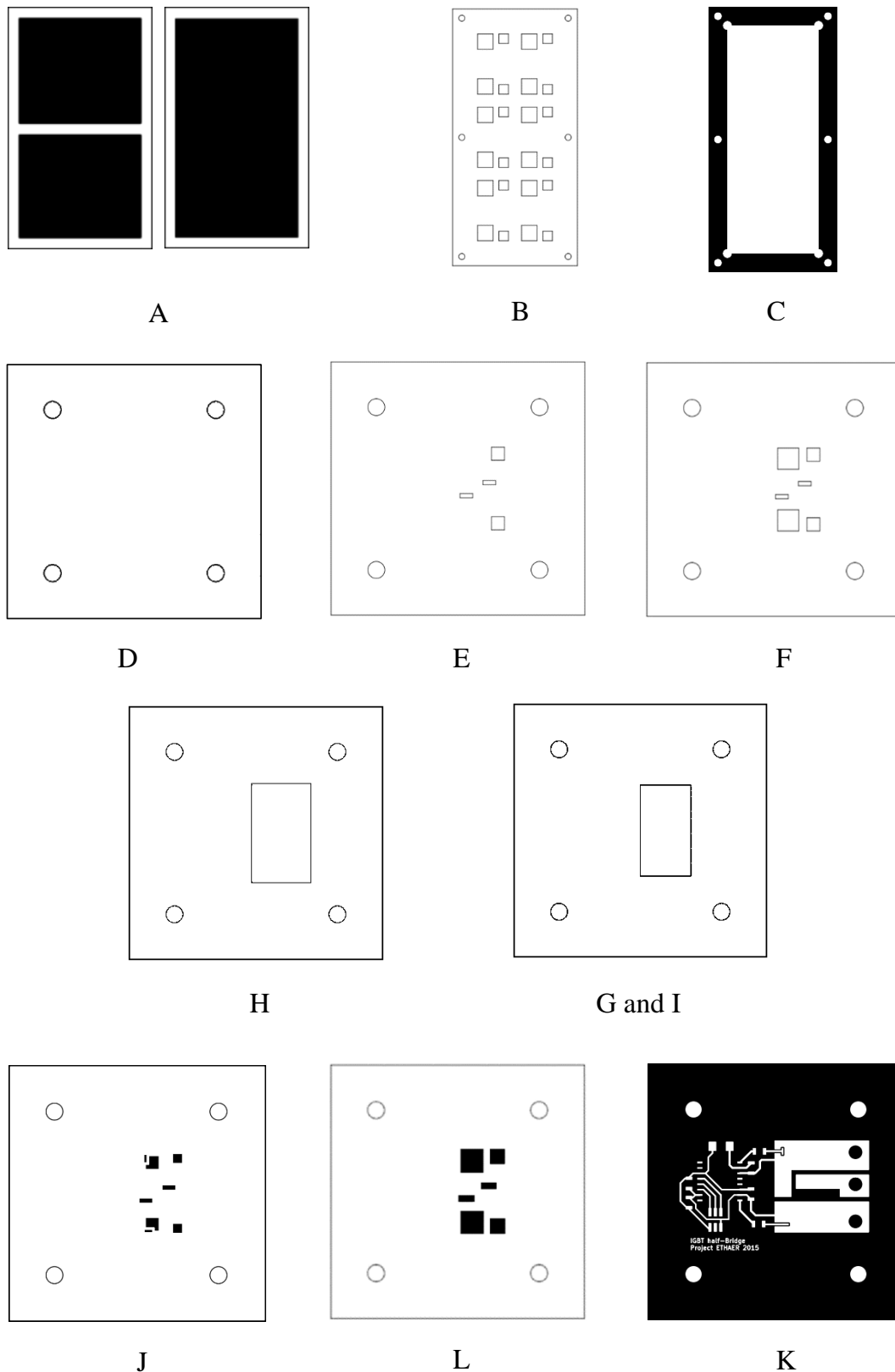


Figure 3.42: Pieces used in fabrication

The manufacturing data comprises two file types, the Gerber file for etching the circuit and the DXF file for laser cutting. Both of them can be exported from Kicad. Figure 3.42

shows all the fabrication pieces required for this prototype, these pieces will be presented in the following paragraphs.

In Kicad, once the electric circuit diagram is drawn, we choose the footprint corresponding to each component. However, Kicad provides limited components' footprints and they are usually standard Surface Mount Device (SMD) footprints, where all terminals are located on a single plane. Furthermore, these devices are mounted on the external surfaces of the PCB, not embedded in it. In our case, we need vertical interconnections (terminals placed on top of each other). Therefore, we have to create suitable footprints for the vertical power components (IGBT, diodes). The PCB type we used here is a classical double side PCB which contains only the topside and the bottom side copper layer. The different layers designed in Kicad are shown in Figure 3.43.

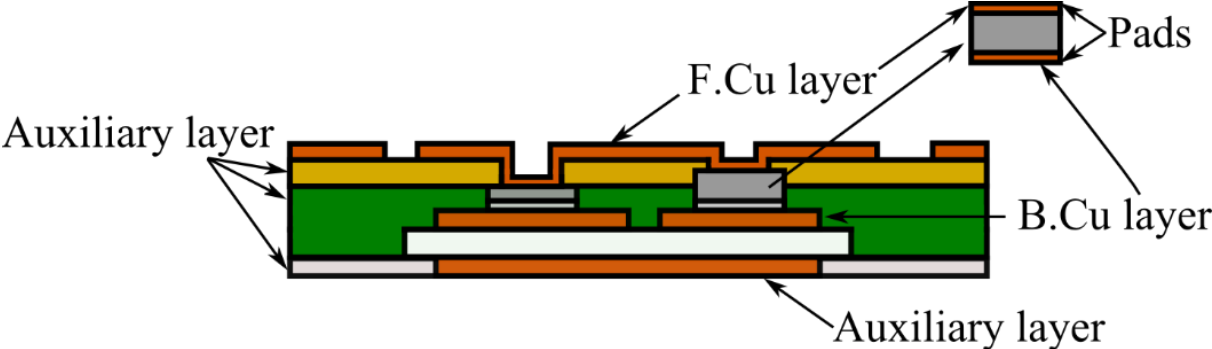


Figure 3.43: different layers designed in Kicad

We start with the DBC etching mask. The topside and the bottom side copper form are shown in Figure 3.42(A), the top side copper uses B.Cu layer and the bottom side uses an auxiliary layer named F.Paste. In order to panelize the fabrication, these two mask files are then plotted to SVG file format and processed with Inkscape³. The panelized masks are shown in Figure 3.44. The alignment points at each edge are used for accurate cut.

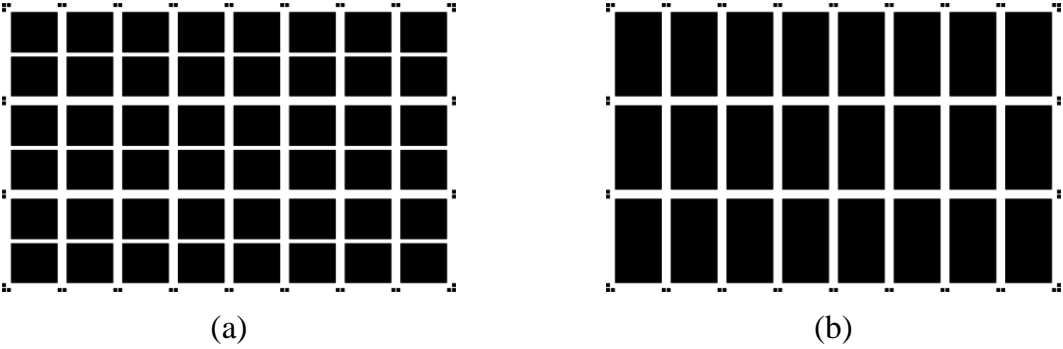


Figure 3.44: Panelized DBC etching masks, (a) top side, (b) bottom side

³ Inkscape is a software designed to edit vector graphics. It is not intended for manipulation of accurate drawings such as the masks used here. However, it has excellent capability regarding the handling of many file formats. In particular, SVG (a vector graphics file format intended for illustration) can readily be exported from kicad and converted in DXF.

The footprints of the power components are created with the Module Editor of Kicad, the topside pads (emitter and gate of the IGBT, anode of the diode) of the die is set to F.Cu (front copper) layer and the bottom pad (collector of the IGBT, cathode of the diode) is set to B.Cu (bottom copper) layer.

Metalized vias can be used to establish the electrical interconnects between different layers. However, because of the buried die and ceramic substrate, these vias cannot be realized (in our process, via would mechanically drilled). As a consequence, a new component has been created. We defined a $0\ \Omega$ resistor in the circuit. Its footprint, just like for the power components, has two pads, one with the F.Cu layer and the other with the B.Cu layer. This component is actually a well extending from the front copper all the way to the bottom copper (i.e the DBC).

To ensure the alignment of the DBC substrate (and therefore of the dies) during the embedding process, we need to register it with the Inox platen of the press. This is achieved by laser-cutting a layer of release film Pacothane plus 4500 with both the alignment pins of the platen and a cutout for the bottom side copper of the DBC. Pacothane plus 4500 has been chosen for this purpose because it will not adhere to the prepreg material and because it is easily to remove after lamination. In addition, it has the same thickness as the DBC's copper layer. The cutout form is shown in Figure 3.42 (G). To match the thickness of the ceramic and top side copper of the DBC, we use PCL370HR prepreg layers which can improve the module rigidity. The cutout for matching ceramic layer is shown in Figure 3.42 (H). The copper and ceramic thickness we used here is $300\ \mu\text{m}$, we need 6 prepreg layers for each part. In Kicad, we use two auxiliary layers (B.Silks and F.Mask) to generate these two pieces. Their design is exported as DXF for laser cutting.

The thickness of the diode is larger than that of the IGBT, as a consequence, we need more prepreg layers for embedding the diode. However, as the additional layers will cover the IGBT and will be ablated, we use here the non-woven Arlon 55NT material for these additional layers (as explained above, this materials leave fewer residues after laser ablation than does the 370HR). The cutout of the prepreg material 370HR used for embedding the IGBT is shown in Figure 3.42 (F), which is set to an auxiliary layer (F.Paste) in Kicad. The Figure 3.42 (E) shows the cutout of the 55NT, where the holes for IGBTs are deleted. These layers are also exporter as DXF for laser cutting. According to the thickness of the IGBT and the diode, we need 5 layers for the HR370 prepreg and 3 layers for the 55NT prepreg.

After lamination, the topside copper needs to be etched to open the windows above the die. Figure 3.42 (J) shows the etching mask for this step. The size of the windows is smaller than the real pad size and depend on the tolerance of some steps. This will be introduced in the next section.

The laser ablation file is shown in Figure 3.42 (L), the black parts are the ablation region.

Finally, the layout will be etched with the mask shown in Figure 3.42 (K). The power part is located on the right side of the module where the power components are embedded. The left part contains the driver and some auxiliary elements such as gate resistors, outside connectors, bootstrap components, etc.

3.6.4 Design Tolerance

As introduced above, the windows above the chips should be smaller than the real pad in order to avoid the damaging the passivation of the die (as it could be be attacked by the laser). However, if the window is too small, the fiber-resin composite cannot be totally ablated, which results in no electrical contact. In the case of the two test vehicles introduced in section 3.2, as the pad surface of diode is large enough, the size of the window is easily defined. On the contrary, in the half-bridge prototype, the IGBT gate pad has a very small surface, the window above this pad should be studied to have a suitable size. As a consequence, it requires to know the tolerance of the fabrication process.

During the fabrication of the half-bridge prototype, the tolerance mainly comes from the die alignment on the DBC. Ag sintering comprises three steps, the screen printing of the Ag paste, the set of the dies by “pick and place” machine and the sintering. The tolerance comes mainly from the first and the second step. In the first step, the support (shown in Figure 3.42(C)) for Ag sintering was designed exactly the same dimension as that of the total 6 individual DBC substrates, and the tolerance is from the step where these individual substrates were cut from the DBC mastercard, which can lead 200 μm tolerance. The second step, where the dies were placed by “pick and place” machine, has better tolerance which is 100 μm . However, these tolerances are not always along the same direction, it is therefore just a reference for the mask design. Such inaccuracy would not be acceptable for mass production, as it would result in poor yield. However, in our case, the objective is to provide a demonstration, and manufacturing yield is not considered.

Figure 3.45 shows the window size above the gate pad of the IGBT, which is defined to 1.7mm \times 0.5 mm and the real size of this pad is 2.011 mm \times 0.788 mm. However, after laser ablation through this window, the dimension is much smaller which is less than 1.5 mm \times 0.1 mm. This is because the laser beam cannot ablate all the surface through such small window, it still exists some polyimide around the corners and the edges.

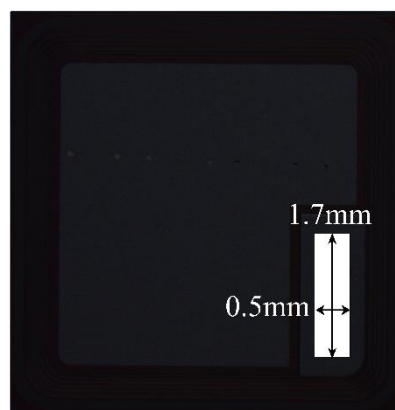


Figure 3.45: Window size above the gate pad of IGBT.

3.6.5 FEM simulation

The power loop inductance for the vertical interconnection is difficult to measure, as it would require a specific power module (one without the embedded devices). Therefore, we use FEM simulation to calculate this value with COMSOL Multiphysics, introduced in the previous chapter. As with the half-bridge prototype with GaN device, we created here a simple geometry which only considers the power path of the module. The geometry, shown in Figure 3.46, is drawn with Solidworks. The bronze parts represent the copper layer of the DBC, the green is for the prepreg, and the white is the air gap. A current of 1A was injected

in the circuit. The study is set up to use a frequency domain where the frequency sweeps from 100 kHz to 4 MHz. The simulations conditions (air box, etc.) are identical to those described in chapter 2.

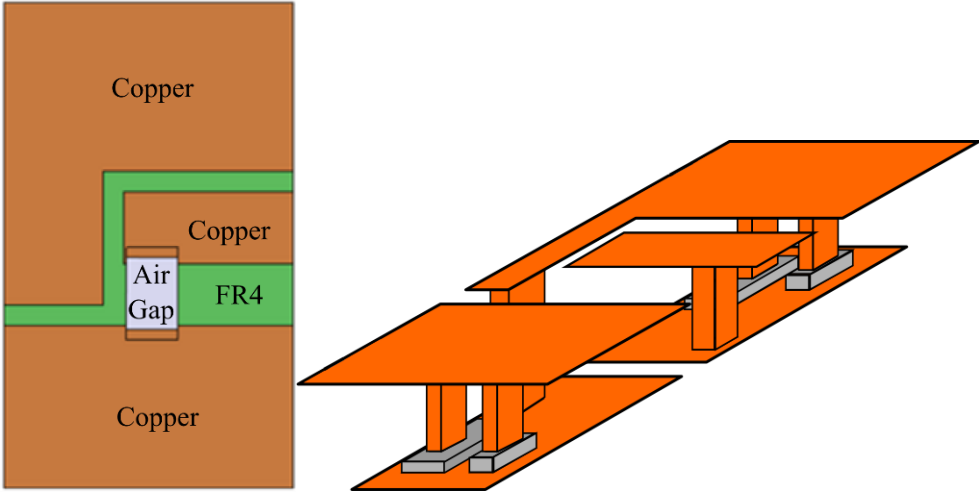


Figure 3.46: Electromagnetic analysis geometry for the half-bridge prototype. On the left side, a drawing presents the same structure with an expanded vertical scale, for the sake of visibility.

The simulation results for loop inductance is shown in Figure 3.47. It proves that the loop inductance with 3D interconnection is much lower than the conventional 2D wire bonding interconnection which is in the range of 10 nH for a single connection [66]. We can note that this inductance decrease with the rise of frequency, and is lower than 3 nH at high frequencies.

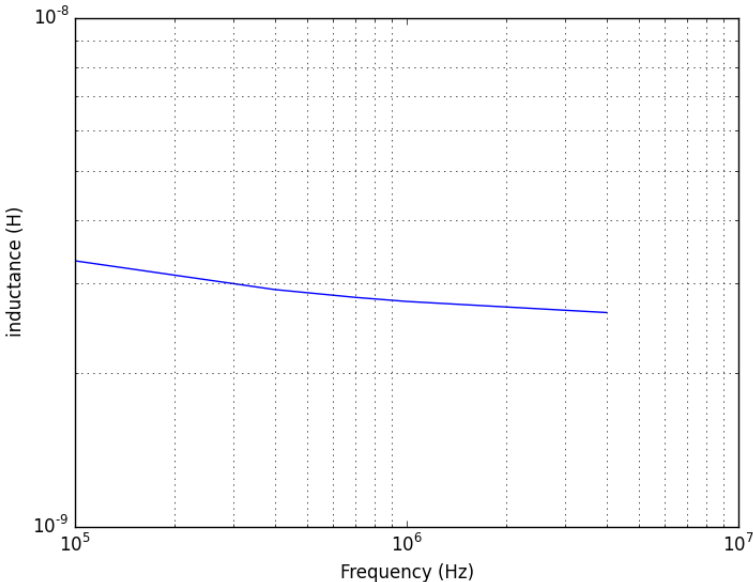


Figure 3.47: Simulation results for loop inductance of the PCB-embedded half bridge.

3.6.6 Experimental characterization

We have fabricated several half-bridge prototypes until now. An example is shown in Figure 3.48. Unfortunately, none of these demonstrators could work successfully. In all the prototypes, the electrical contacts on anodes and cathodes of the two diodes are always established although their quality is not sufficient. However, the contact on the gate of the IGBTs is always fugitive. This proves the good alignment of the process, but the contact quality must be greatly improved. According to this, we have only tested some well-connected components to see the influence of the embedding process. Figure 3.49 (a) shows the direct characteristics of a functional diode of a prototype. The measurement is made with a Tektronix 371 curve tracer. The results show that the diode works correctly provided to limit the maximum current to 6A. If we increase the current, the curve begins to disrupt after a moment, this may come from the poor contact quality of the die, which is due to the thickness of the Ti/Cu layer obtained by an evaporation process for the diodes and IGBTs of our prototypes. Indeed, the thickness of the layer is only 50nm/150nm of Ti/Cu, which is not sufficient for a good electroplating. Figure 3.49 (b) shows the direct characteristics of a functional IGBT for different gate voltages. These results demonstrates the proper functioning of this IGBT.

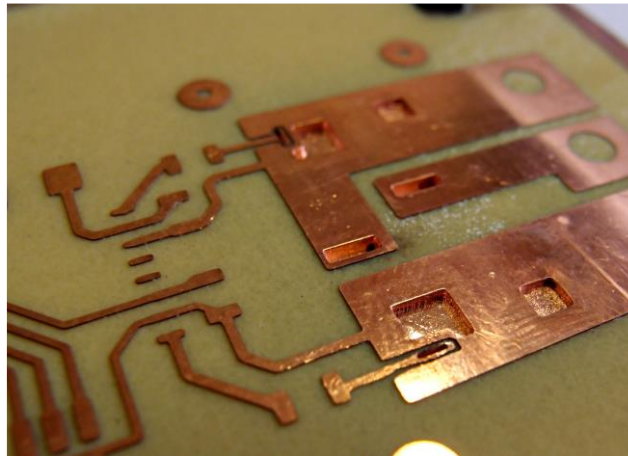


Figure 3.48: A fabricated example of the half-bridge prototype

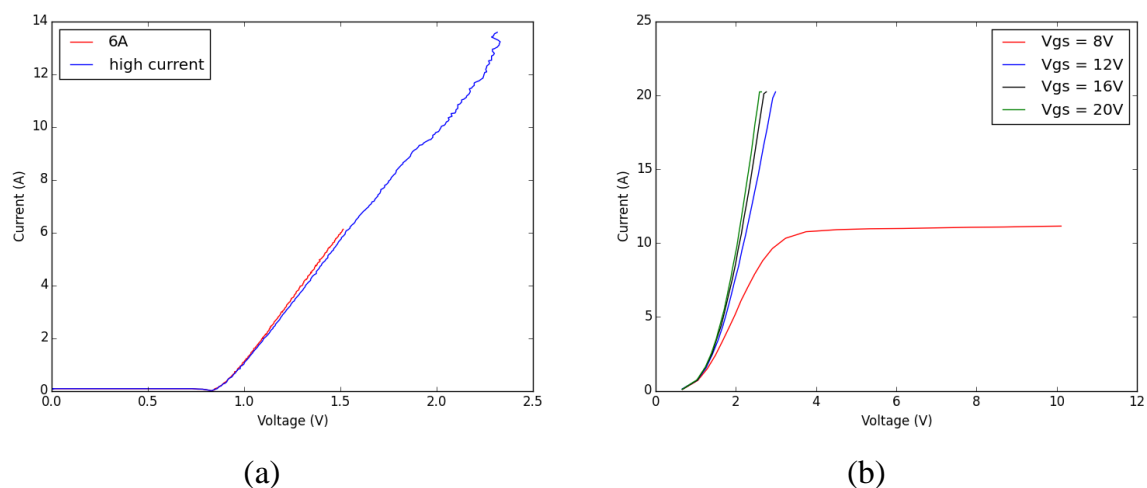


Figure 3.49: Direct characteristics of the working (a) diode, (b) IGBT in one of the half-bridge prototype

3.6.7 Improvement

In order to make this half-bridge prototype operate, we can broaden the window size for laser ablation above the gate pad, this could help the laser to ablate as much as the prepreg materials. The thickness of the evaporated Ti/Cu layer of the die should be increased (up to 1 μm) to have a better copper electroplating. Another approach is to perform the metallization later in the process, by sputtering after laser ablation and before electroplating. This can replace the step of activation (the deposition of palladium to make all surfaces conductive), as we suspect this step damages the aluminum metallization of the dies). In this case, the only wet process remaining would be the copper electroplating. A photo of the ablated window received a sputtering of 900 nm Cu is shown in Figure 3.50.

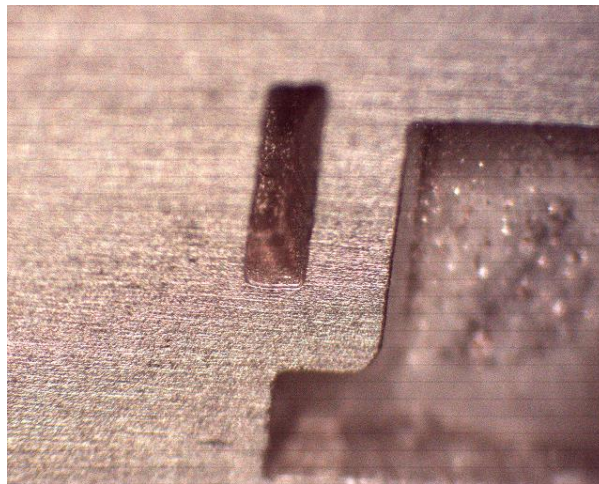


Figure 3.50: A photo of the ablated window received a sputtering of 900 nm Cu

3.7 Conclusion

In this chapter, we have firstly introduced an alternative solution to the classical 2D vertical components package, which is using the PCB technology to embed the components in the substrate. This technique allows a 3D interconnection which can decrease the parasitic inductance in the loop. In order to develop and study this technology, we have created two test vehicles and a half-bridge switching cell. The first test vehicle is designed to understand the materials and manipulations in embedding process, the second one is used for studying the current distribution in the diode. The half-bridge prototype is more representative of an actual application, as it includes not only diodes, but also transistors and their gate driver circuit. The detailed presentation of each fabrication step for the embedding technology is then presented. The FEM simulation proves that the PCB technology brings an electric interconnection with very low loop inductance compared to the conventional wire bonding module.

The power devices embedding is a very promising technology which allows the custom design at die level. Due to its low inductance interconnects, it can be used with fast switching devices to reduce switching losses. Another advantage is that the contact resistance with the die can be largely decreased by choosing an appropriate contact layout. The embedding process is a relatively simple process which can be easily implemented in

a laboratory. As the fabrication files are generated by a numerical CAD tool, this process can easily be included in a classical design flow.

Conclusion and perspectives

In the context of changing onboard electrical networks in future aircrafts, the ANR project ETHAER, which supported this thesis, aims to design a $28\text{V}/\pm 270\text{V}$ multicell Buck Boost Converter Unit (BBCU). In order to take full advantage of this multicell topology and to get better thermal and electromagnetic performances, it is necessary to develop new packaging suited to the high interconnect count inherent to multicell structures. To build high density converters, the traditional silicon power semiconductors are no longer usable because they have already approached their theoretical limits. It is therefore interesting to choose power components based on wide bandgap materials such as Gallium nitride (GaN) and Silicon carbide (SiC). As the BBCU topology contains both a High Voltage (HV) and a Low Voltage (LV) stage, two different integration solutions are proposed. The LV stage is based on lateral GaN devices mounted on a DBC substrate, and the HV stage is based on vertical components buried in PCB and also mounted on a DBC substrate.

The current researches focus on the development of new technological solutions adapted to new wide-bandgap power semiconductor devices and more severe operating environment. As, planary 2D integration has serious limits because of the bonding wires, an alternative solution is to use 3D packaging to improve the electrical interconnections in the power module. 3D integration improves electrical performances (reduction of the parasitic loop inductance). In this 3D integration context, we can also notice that there is a trend in power integration technologies toward use of printed circuit technology (PCB). The main advantages of such substrates are linked to its small track size and small pitch as well as its multilayer and embedding devices ability allowing to drastically reduce the length of interconnections.

Despite the improvement in conversion efficiency, the active devices dissipate a lot of heat (100 to $300\text{ W}/\text{cm}^2$). Besides, in the case of lateral GaN transistors, the bumps have limited thermal conductivity, and cover only a fraction of the die surface area. This could hinder the heat dissipation of the die. In this regard, it is worth comparing the thermal performance of GaN devices cooled either through their bumps (topside cooling) or through their silicon substrate (backside cooling). We also compare the thermal performance of dies mounted on ceramic substrate and on a more standard PCB substrate. To realize this study, three prototypes have been fabricated. In the first configuration, GaN transistors are flip-chip mounted on the DBC substrate. As the footprint of the GaN transistor is very small ($200\text{ }\mu\text{m}$ pitch), a special etching technique was used to achieve this high resolution. In the second prototype, the backside of the transistors is attached to the DBC. The silicon substrate of the transistors are grinded down to reduce their thickness and to remove the marking. A Ti/Ag layer was deposited on the silicon substrate to improve the Ag sintering which realizes the attachment of the die to the DBC. A flex substrate is used on the top-side to provide electrical interconnects from the bumps to the substrate tracks. The third one is the classical flip-chip mounting on PCB. A FEM analysis using COMSOL Multiphysics is firstly used to study the thermal issue. The simulation results proves that the DBC has much better thermal performance than the PCB, due to its lower thermal resistance. The second prototype, in which the heat diffuses through the encapsulation to the DBC substrate, has a little higher thermal resistance compared to the first prototype (where the heat flows through the bumps of the transistor). This proves that: the thermal resistance of the silicon substrate

is higher than the thermal resistance of the solder bumps. Experimental measurements are also realized to compare with the FEM simulation.

The thermal analysis has proven that DBC substrate has much better thermal performance than PCB, with a total thermal resistance 5 times lower. From an electrical point of view, the thick copper layers of DBC offer lower resistance interconnects, but only one copper layer can be patterned to form a circuit, resulting in a planar layout with longer interconnects than for PCB and therefore to higher electrical and EMI constraints. Therefore, the electrical performances of DBC substrate are an issue for wide-band-gap power devices and their high switching speeds. To study this issue, a half-bridge structure with two GaN transistors, their associated gate drivers and some decoupling capacitors has been fabricated on a DBC substrate. In a first step, we studied the impact of the bottom side copper of the DBC on the loop inductance and resistance. It has been shown that the copper layer has an important influence, as it reduces the loop inductance by a factor of two, with negligible consequences on the resistance. The second study analyses the evolution of the loop inductance with the thickness of the ceramic. According to the results, the loop inductance increases with the ceramic thickness. For a ceramic layer of 250 μm , inductances of less than 2 nH are achievable. This is however still much more than an optimized PCB (0.4 nH), but might be acceptable in some cases. Finally, in order to calculate the partial inductances, an analytical approach has been proposed. The calculated partial inductances are used in a circuit simulator to evaluate electrical and EMI constraints in our prototype.

Regarding the high-voltage side of the converter, which uses vertical devices, the conventional electrical interconnections are usually established by wire-bonding. This involves large stray inductances and thereby generates high switching losses. To avoid this, the length of interconnects must be reduced. PCB technology offer this possibility. But in power electronics devices, the DBC substrate is classically used for better heat dissipation. We propose a new packaging technology where DBC and PCB are used together. The fabrication process we used in the laboratory begins with the preparation of the DBC etching. The power components are then attached to the DBC by Ag sintering. The following steps are similar to the classical PCB fabrication process, which consists in lamination, laser ablation and etching. A first diode prototype has proved the feasibility of this process, and the static characterization proved that the embedding of the die constitutes a satisfying encapsulation.

In high power applications, a strong current flows in the module. Therefore, it is necessary to have a low contact resistance. Some prototypes have been designed to analyze the influence of contact area and shape. A theoretical calculation based on the modified nodal analysis and an experimental characterization using 4-point connections are performed. The results show that multiple contacts allow for a better current spreading over the die metallization, even with smaller contact area. Because of the poor contact between the electroplated layer and the die topside metallization, there is an important difference between the simulations and the measurements. Despite this, the best measurements are already better than regular wire bonded devices.

According to the performance of PCB technology, a high voltage (1200 V) half-bridge power module has been designed. In this prototype, an Electronic Design Automation (EDA) tools has been used to route the more complex circuit and generate the fabrication files. This tool allows automatic routing, adaptable design rules and generation of the manufacturing data such as position of dies, or laser drilling at once. However, no fully working prototype has been built at the time of writing, but this should be solved in rapidly.

Short term future projects: In this thesis, due to the low precision of thermal characterization realized on GaN prototypes, we were not able to observe any difference in the thermal performances of AlN and Al₂O₃ substrates. In order to solve this problem, we have to improve the control of the thermal interface by using another temperature sensitive parameter with better thermal precision. The flip-flip-chip prototype also needs to be completed. It is necessary to use a flex substrate with thicker copper (up to 70 μm) layer and improve the low-temperature sintering process. Some steps in PCB embedding technique also need to be improved. Firstly, the thickness of the evaporated Ti/Cu layer of the die should be increased (up to 1 μm) to have a better copper electroplating. Another approach is to perform the metallization later in the process, by sputtering after laser ablation and before electroplating. This can replace the step of activation (the deposition of palladium to make all surfaces conductive), as we suspect this step damages the aluminum metallization of the dies). In this case, the only wet process remaining would be the copper electroplating.

Long term future projects: This thesis focuses mainly on the integration of active components. The next step should be the integration of passive components, which should help reducing the package size further. This could be realized by adding magnetic layers and capacitive layers during the PCB fabrication process. Resistance should also be realized by printing resistive pastes. Until now, the most complicated circuit we built was just a half-bridge which is only a basic element in a power converter. A so-called Buck or Boost topology was actually designed and tested in ETHAER project. This topology is a multicellular power converter which requires a lot of semiconductor devices and many interconnections between the cells. It requires not only switching cells, but also interconnects with large passive components and control. Such an advanced structure must therefore be designed.

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Annex A

Wire bonding geometry script :

```
% param?tres
Longueur = 9e-3;
Hauteur = 2e-3;
%Rayon_Wire = 350e-6;
Rayon_Wire = 150e-6;

%Position = Hauteur / Longueur;
Position = 0.7;
% cercle principal
Cercle.Rayon = 3*Hauteur / 4;
Cercle.Centre.x = 0;
Cercle.Centre.y = Hauteur/4;

% coordonn?es du fil de bonding
Wire.x = -(1-Position)*Longueur;
Wire.y = Rayon_Wire;

Pr(1).x = Wire.x;
Pr(1).y = 0;

Pr(6).x = Position*Longueur;
Pr(6).y = 0;

% D1C : distance Pr1 Centre du cercle
D1C = sqrt(Pr(1).x^2+Cercle.Centre.y^2);

% D12 : Distance Pr1 Pr2
D12 = sqrt(Pr(1).x^2+Cercle.Centre.y^2-Cercle.Rayon^2);
Alpha1 = asin(Cercle.Centre.y/D1C)+asin(Cercle.Rayon/D1C);

% D6C : distance Pr6 Centre du cercle
D6C = sqrt(Pr(6).x^2+Cercle.Centre.y^2);
```

```

% D56 : Distance Pr5 Pr6
D56 = sqrt(Pr(6).x^2+Cercle.Centre.y^2-Cercle.Rayon^2);
Alpha6 = asin(Cercle.Centre.y/D6C)+asin(Cercle.Rayon/D6C);

%Pr2.x = Pr(1).x+D12*cos(Alpha1);
%Pr2.y = D12*sin(Alpha1);

Pr(2).x = Cercle.Centre.x-Cercle.Rayon*sin(Alpha1);
Pr(2).y = Cercle.Centre.y+Cercle.Rayon*cos(Alpha1);

Wire(2).x = Pr(2).x-Rayon_Wire*sin(Alpha1);
Wire(2).y = Pr(2).y+Rayon_Wire*cos(Alpha1);

Wire(3).x = 0;
Wire(3).y = Hauteur+Rayon_Wire;

Pr(4).x = Cercle.Centre.x+Cercle.Rayon*sin(Alpha6/2);
Pr(4).y = Cercle.Centre.y+Cercle.Rayon*cos(Alpha6/2);

Wire(4).x = Pr(4).x+Rayon_Wire*sin(Alpha6/2);
Wire(4).y = Pr(4).y+Rayon_Wire*cos(Alpha6/2);

%Pr5.x = Pr6.x-D56*cos(Alpha6);
%Pr5.y = D56*sin(Alpha6);

Pr(5).x = Cercle.Centre.x+Cercle.Rayon*sin(Alpha6);
Pr(5).y = Cercle.Centre.y+Cercle.Rayon*cos(Alpha6);

Wire(5).x = Pr(5).x+Rayon_Wire*sin(Alpha6);
Wire(5).y = Pr(5).y+Rayon_Wire*cos(Alpha6);

Wire(6).x = Pr(6).x;
Wire(6).y = Rayon_Wire;

for ind = 1:6
    x(ind) = Wire(ind).x;
    y(ind) = Wire(ind).y;

```

```

end;

N_Spline = 98;

xx = linspace(x(1),x(6),N_Spline);
yy = spline(x,[0 y 0],xx);

xxi = [xx(1)-Longueur/10 xx xx(N_Spline)+Longueur/10];
yyi = [yy(1) yy yy(N_Spline)];

figure(1);
hold off;
plot(xxi,yyi,'b');

import com.comsol.model.*
import com.comsol.model.util.*
model = ModelUtil.create('Model');
geom1 = model.geom.create('geom1', 3);
xxi = xxi - 0.0035;
yyi = yyi + 0.001;
% xxi(100) = -0.0005;
% xxi = [xxi 0];
% yyi = [yyi 0.001];
% xxi = [-0.0086 xxi];
% yyi = [0.001 yyi];
zzi = ones(1,100)*0;
degree = ones(1,99)*1;
table = [xxi yyi];
wp1 = geom1.feature.create('wp1', 'WorkPlane');
wp1.set('quickplane', 'xz');
wp1.set('quicky', '0.001');
c1 = wp1.geom.feature.create('c1', 'Circle');
c1.set('r', '125e-6');
c1.set('pos', '0.0001, 0');
ic1 = geom1.feature.create('ic1', 'InterpolationCurve');
% ic1 = geom1.feature.create('ic1', 'BezierPolygon');
% ic1.set('type', 'open');

```

```
%ic1.set('degree', 2);
%ic1.set('p', table);
ic1.set('source', 'vectors');
ic1.set('x', xxi).set('y', yyi).set('z', zzi);
ic1.set('rtol', 5e-3);
swe1 = geom1.feature.create('swe1', 'Sweep');
swe1.set('rtol', 0.001);
swe1.set('align', 'moveface');
swe1.set('adjustlen', 0.1);
swe1.set('reversedir', 'on');
swe1.selection('face').set('wp1.c1', 1);
swe1.selection('edge').set('ic1(1)', 1);
swe1.set('grep', 'spline');
model.geom('geom1').run;
```

Annex B

Contact area analysis script:

```
#!/usr/bin/python
# -*- coding: utf-8 -*-

from __future__ import division
from scipy import *
from numpy import *
#matplotlib n'est pas sur le cluster de calcul
#from matplotlib.pyplot import *
#import resource
import time
""" implémentation de la méthode nodale modifiée (MNA, Modified Nodal Analysis)
pour le calcul de la résistance équivalente d'une puce enterrées"""

# huitième version: enregistrement des données pour lancement en série. Ne fonctionne pas sur le cluster
parce que scipy n'y est pas installé
begin = time.time()
n=60 # discrétisation du côté de la plaque
m=60# discrétisation de la puce
l=100e-6 #length of one element
d=200e-6 # depth of the post (or well)
resist_copper=16.78e-9 #resistivity of copper
resist_aluminium=28.2e-9 #resistivity of aluminium
resist_silicon=6e-5 # resistivity of 1e19 cm-3 doped silicon
thick_aluminium=3e-6 #thickness of die topside aluminium
thick_electroplated_copper=17e-6 #thickness of the electroplated copper layer
thick_top_copper=17e-6 #thickness of the copper sheet before electroplating
thick_silicon=400e-6 #thickness of die
#R=0.01 # résistance d'un noeud à l'autre pour les noeuds situés au centre de la plaque
R=resist_copper*/(thick_top_copper+thick_electroplated_copper*1)
#Rext=1 # résistance entre les noeuds externes et l'équipotentielle en bordure
Rext=R
#Rgnd=1# résistance connectant certains noeuds à la masse
#Rwall=1 # résistance des murs verticaux des posts
```

```

Rwall=resist_copper*d/(thick_electroplated_copper*1)
#Rpost=.01 #resistance of the top (or bottom) of the posts
Rpost=resist_copper*1/(thick_electroplated_copper*1)
#Ralu=1. # resistance of the aluminium topside metal
Ralu=resist_aluminium*1/(thick_aluminium*1)
#Rdiode=1. # resistance of the elementary diode
Rdiode=resist_silicon*thick_silicon/1**2
Rcontact = 1e-9 # contact resistance between the posts and the die
V=1. # tension de la source reliée à l'équipotentielle

#read the task ID from SGE, to detect which post parameters to select.
index=5
#post_parameters=[[1, 1, 28],[2, 2, 14],[4,4,7],[7,7,4], [14, 14, 2], [28,28, 1]]
post_parameters=[[10, 10, 1],[20, 20, 1],[30,30,1],[40,40,1], [10, 20, 2], [15,10, 2]]
[post_width,post_spacing,post_count] = post_parameters[index]

def generate_posts(post_width, post_spacing, post_count, n):
    posts=zeros((n,n), dtype=int8) # the posts matrix contains the position of the posts
        # 0 if we're not on a post, 1 if we are.
    post_area_width=post_count*post_width+(post_count-1)*post_spacing
    post_margin=int((n-post_area_width)/2)
    post_vector=ones(post_width) #generate a 1D vector with the post patterns
    for i in range(post_count-1):
        post_vector=concatenate((post_vector, zeros(post_spacing)), axis=1)
        post_vector=concatenate((post_vector, ones(post_width)), axis=1)
    if post_margin<1:
        raise ValueError('post area wider than top copper plate')
    for i in range(post_area_width):
        for j in range(post_area_width):
            posts[post_margin+i, post_margin+j]=post_vector[i]*post_vector[j]
    return posts

def generate_top_conductance_matrix(n,posts):
    """ génère une matrice de taille n**2xn**2 qui donne toutes les résistances
    entre deux noeuds"""
    conductance_matrix=zeros((n**2,n**2), dtype=float64)

```

```

for i in range(n):
    for j in range(n):
        if (i==0 or i==n-1): # nous sommes en bordure haut ou bas de la plaque
            if (j==0 or j==n-1): # nous sommes dans les coins
                pass
            else: #sur les bords haut et bas, mais pas sur les coins
                conductance_matrix[i+(j-1)*n,i+j*n]=-1/R
                conductance_matrix[i+(j+1)*n,i+j*n]=-1/R
                conductance_matrix[i+j*n,i+(j-1)*n]=-1/R
                conductance_matrix[i+j*n,i+(j+1)*n]=-1/R
        if (j==0 or j==n-1):
            if (i!=0 and i!=n-1):
                # on est sur les bords gauche et droite, mais pas dans les coins:
                conductance_matrix[i+j*n-1,i+j*n]=-1/R
                conductance_matrix[i+j*n+1,i+j*n]=-1/R
                conductance_matrix[i+j*n,i+j*n-1]=-1/R
                conductance_matrix[i+j*n,i+j*n+1]=-1/R
        if (i!=0 and i!=n-1 and j!=0 and j!=n-1):
            if posts[i,j]:#we are on a post
                if posts[i-1,j]: #now we explore the values of posts around this point
                    R1=Rpost
                else: R1=Rwall
                if posts[i+1,j]:
                    R2=Rpost
                else: R2=Rwall
                if posts[i,j-1]: #now we explore the values of posts around this point
                    R3=Rpost
                else: R3=Rwall
                if posts[i,j+1]:
                    R4=Rpost
                else: R4=Rwall
            else: # we are not on a post
                if posts[i-1,j]: #now we explore the values of posts around this point
                    R1=Rwall
                else: R1=R
                if posts[i+1,j]:
                    R2=Rwall

```



```

else: R2=R
if posts[i,j-1]: #now we explore the values of posts around this point
    R3=Rwall
else: R3=R
if posts[i,j+1]:
    R4=Rwall
else: R4=R
conductance_matrix[i+j*n-1,i+j*n]=-1/R1
conductance_matrix[i+j*n+1,i+j*n]=-1/R2
conductance_matrix[i+n*(j-1),i+j*n]=-1/R3
conductance_matrix[i+n*(j+1),i+j*n]=-1/R4
conductance_matrix[i+j*n,i+j*n-1]=-1/R1
conductance_matrix[i+j*n,i+j*n+1]=-1/R2
conductance_matrix[i+j*n,i+n*(j-1)]=-1/R3
conductance_matrix[i+j*n,i+n*(j+1)]=-1/R4
return conductance_matrix

```

```

def generate_die_conductance_matrix(m):
    conductance_matrix=zeros((m**2,m**2), dtype=float64)
    for i in range(m):
        for j in range(m):
            if (i==0 or i==m-1): # nous sommes en bordure haut ou bas de la plaque
                if (j==0 or j==m-1): # nous sommes dans les coins
                    pass
                else: #sur les bords haut et bas, mais pas sur les coins
                    conductance_matrix[i+(j-1)*m,i+j*m]=-1/Ralu
                    conductance_matrix[i+(j+1)*m,i+j*m]=-1/Ralu
                    conductance_matrix[i+j*m,i+(j-1)*m]=-1/Ralu
                    conductance_matrix[i+j*m,i+(j+1)*m]=-1/Ralu
            if (j==0 or j==m-1):
                if (i!=0 and i!=m-1):
                    # on est sur les bords gauche et droite, mais pas dans les coins:
                    conductance_matrix[i+j*m-1,i+j*m]=-1/Ralu
                    conductance_matrix[i+j*m+1,i+j*m]=-1/Ralu
                    conductance_matrix[i+j*m,i+j*m-1]=-1/Ralu
                    conductance_matrix[i+j*m,i+j*m+1]=-1/Ralu
            if (i!=0 and i!=m-1 and j!=0 and j!=m-1):

```

```

    conductance_matrix[i+j*m-1,i+j*m]=-1/Ralu
    conductance_matrix[i+j*m+1,i+j*m]=-1/Ralu
    conductance_matrix[i+m*(j-1),i+j*m]=-1/Ralu
    conductance_matrix[i+m*(j+1),i+j*m]=-1/Ralu
    conductance_matrix[i+j*m,i+j*m-1]=-1/Ralu
    conductance_matrix[i+j*m,i+j*m+1]=-1/Ralu
    conductance_matrix[i+j*m,i+m*(j-1)]=-1/Ralu
    conductance_matrix[i+j*m,i+m*(j+1)]=-1/Ralu
for i in range(m**2): #ajout du terme diagonal et d'une résistance à la masse
    # sur chaque noeud.
    conductance_matrix[i,i]=-sum(conductance_matrix[i,:])+1/Rdiode
return conductance_matrix

def generate_top_G_with_posts2(n,posts,conductance_matrix):
    """generate the G matrix for the copper plate with posts"""
    # création de la matrice des conductances (G)
    # suivant http://www.swarthmore.edu/NatSci/echeeve1/Ref/mna/MNA3.html
    G=zeros((n**2+1, n**2+1), dtype=float64)
    G[n**2,n**2]=4*n/Rext # the voltage source is connected to all the edges of the plate.
    G[0:n**2,0:n**2]=conductance_matrix
    for i in range(n**2):
        G[i,i]=-sum(conductance_matrix[i,:])-G[i,i]
    for i in range(n):
        for j in range(n):
            if (i==0 or i==n-1): # nous sommes en bordure haut ou bas de la plaque
                if (j==0 or j==n-1): # nous sommes dans les coins
                    G[i+j*n,i+j*n]=G[i+j*n,i+j*n]+2/Rext
                    G[i+j*n,n**2]=-2/Rext
                    G[n**2,i+j*n]=-2/Rext
                else: #sur les bords haut et bas, mais pas sur les coins
                    G[i+j*n,i+j*n]=G[i+j*n,i+j*n]+1/Rext
                    G[i+j*n,n**2]=-1/Rext
                    G[n**2,i+j*n]=-1/Rext
            if (j==0 or j==n-1):
                if (i!=0 and i!=n-1):
                    # on est sur les bords gauche et droite, mais pas dans les coins:

```

```

        G[i+j*n,i+j*n]=G[i+j*n,i+j*n]+1/Rext
        G[i+j*n,n**2]=-1/Rext
        G[n**2,i+j*n]=-1/Rext
    #if (i!=0 and i!=n-1 and j!=0 and j!=n-1):
    # # on est au milieu du circuit
    # if posts[i,j]: # on est sur un post, on rajoute une résistance
    # # vers la masse sur le terme diagonal
    # G[i+j*n,i+j*n]=G[i+j*n,i+j*n] +1/Rgnd
return G

def plot_die_voltage(vecteur_tensions):
    surface=vecteur_tensions.reshape((m,m))
    matshow(surface)#, fignum=100, cmap=cm.gray)
    show()

def calculate_coordinates(post_width, post_spacing, post_count, width):
    """ calculates the position of the posts in a width**2 matrix """
    post_area_width=post_count*post_width+(post_count-1)*post_spacing
    post_margin=int((width-post_area_width)/2)
    post_coordinates=[]
    temp=reshape(generate_posts(post_width, post_spacing, post_count, width), width**2)
    for i in range(len(temp)):
        if temp[i]:
            post_coordinates.append(i)
    return post_coordinates

print "generation of top conductance matrix"
posts=generate_posts(post_width, post_spacing, post_count, n)
conductance_matrix=generate_top_conductance_matrix(n,posts)
Gtop=generate_top_G_with_posts2(n,posts, conductance_matrix)
conductance_matrix=None
end_first_step=time.time()
print "generation of die conductance matrix"
#set_printoptions(threshold='nan')
Gdie=generate_die_conductance_matrix(m)
end_second_step=time.time()

```

```

print "preparation of matrices for solving"
# create a G matrix as follows:
# Gtop ... Gtop .... ..
# ... ..
# Gtop ... Gtop .... ..
# .... .. Gdie ... Gdie
# .... ..
# .... .. Gdie ... Gdie
G=zeros((n**2+1+m**2,n**2+1+m**2), dtype=float32)
G[0:n**2+1,0:n**2+1]=Gtop
G[n**2+1:n**2+1+m**2,n**2+1:n**2+1+m**2]=Gdie
Gtop=None
Gdie=None
# now add the contact resistances between posts and die
# calculation of the coordinates of the posts on top and die
post_contacts = (post_count*post_width)**2 # number of point of contact between top plate and
top_post_coordinates=calculate_coordinates(post_width, post_spacing, post_count, n)
die_post_coordinates=calculate_coordinates(post_width, post_spacing, post_count, m)
for i,coord_top in enumerate(top_post_coordinates):
    coord_die = die_post_coordinates[i]+n**2+1
    G[coord_top, coord_top]=G[coord_top, coord_top]+1/Rcontact
    G[coord_die, coord_die]=G[coord_die, coord_die]+1/Rcontact
    G[coord_top, coord_die]=-1/Rcontact
    G[coord_die, coord_top]=-1/Rcontact

# matrices de connexion des sources (une seule, au point V)
B=zeros((n**2+1+m**2,1),dtype=float32)
C=zeros((1,n**2+1+m**2), dtype=float32)
B[n**2,0]=1
C[0,n**2]=1
# on forme maintenant la matrice z=[[i,e]] avec
i=zeros((n**2+1+m**2,1), dtype=float64)
e=zeros((1,1), dtype=float64)
e[0,0]=V
z=concatenate((i,e),axis=0)
i=None
e=None

```

```

# puis celle des sources dépendantes
D=zeros((1,1), dtype=float32)
# on forme maintenant la matrice A:
# A=[[G,B][C,D]]
A=concatenate((concatenate((G, B), axis=1),concatenate((C,D), axis=1)),axis=0)
G=None
B=None
C=None
D=None
end_third_step=time.time()
print "solve"
solution=linalg.solve(A, z)
print solution.dtype
print "resistance=",1/solution[-1]
print "execution time:", time.time()-begin
print "top matrix:", end_first_step-begin, "; die matrix:", end_second_step-end_first_step, "; matrix
generation:", end_third_step-end_second_step, "; solving:", time.time()-end_third_step
#print resource.getrusage(resource.RUSAGE_SELF).ru_maxrss, "kB"

# save data to disk:
save("%s_solution" %index, solution)

#plot_die_voltage(solution[-m**2-1:-1])

```