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THÈSE PRÉSENTÉE
POUR OBTENIR LE GRADE DE
DOCTEUR DE
L'UNIVERSITÉ DE BORDEAUX

ÉCOLE DOCTORALE de Sciences Physiques et de l'Ingénieur
SPÉCIALITÉ Électronique

Par Jorge Daniel AGUIRRE MORALES

**Characterization and Modeling of Graphene-based Transistors
towards High Frequency Circuit Applications**

Sous la direction de : Thomas ZIMMER
(Co-encadrant : Sébastien FRÉGONÈSE)

Soutenue le 17 Novembre 2016

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For Amaury, my sister and my parents.

“Graphene is the hero we deserve, but not the one we can use right now. So we will research it. Because it's worth it. Because it is not our hero.

It is a silent guardian, a watchful protector. The dark slice”

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Title: Characterization and Modeling of Graphene-based Transistors towards High Frequency Circuit Applications

Abstract:

This work presents an evaluation of the performances of graphene-based Field-Effect Transistors (GFETs) through electrical compact model simulation for high-frequency applications. Graphene-based transistors are one of the novel technologies and promising candidates for future high performance applications in the beyond CMOS roadmap. In that context, this thesis presents a comprehensive evaluation of graphene FETs at both device and circuit level through development of accurate compact models for GFETs, reliability analysis by studying critical degradation mechanisms of GFETs and design of GFET-based circuit architectures.

In this thesis, an accurate physics-based large-signal compact model for dual-gate monolayer graphene FET is presented. This work also extends the model capabilities to RF simulation by including an accurate description of the gate capacitances and the electro-magnetic environment. The accuracy of the developed compact model is assessed by comparison with a numerical model and with measurements from different GFET technologies.

In continuation, an accurate large-signal model for dual-gate bilayer GFETs is presented. As a key modeling feature, the opening and modulation of an energy bandgap through gate biasing is included to the model. The versatility and applicability of the monolayer and bilayer GFET compact models are assessed by studying GFETs with structural alterations.

The compact model capabilities are further extended by including aging laws describing the charge trapping and the interface state generation responsible for bias-stress induced degradation.

Lastly, the developed large-signal compact model has been used along with EM simulations at circuit level for further assessment of its capabilities in the prediction of the performances of three circuit architectures: a triple-mode amplifier, an amplifier circuit and a balun circuit architecture.

Keywords: bilayer, compact model, graphene, monolayer, reliability, Verilog-A.

Titre : Caractérisation et Développement des Modèles Compacts pour des Transistors en Graphène pour des Applications Haute Fréquence

Résumé :

Ce travail présente une évaluation des performances des transistors à effet de champ à base de graphène (GFET) grâce à des simulations électriques des modèles compacts dédiés à des applications à haute fréquence. Les transistors à base de graphène sont parmi les nouvelles technologies et sont des candidats prometteurs pour de futures applications à hautes performances dans le cadre du plan d'action « au-delà du transistor CMOS ». Dans ce contexte, cette thèse présente une évaluation complète des transistors à base de graphène tant au niveau du dispositif que du circuit grâce au développement de modèles compacts précis pour des GFETs, de l'analyse de la fiabilité, en étudiant les mécanismes critiques de dégradation des GFETs, et de la conception des architectures de circuits basés sur des GFETs.

Dans cette thèse nous présentons, à l'aide de certaines notions bien particulières de la physique, un modèle compact grand signal des transistors FET à double grille à base de graphène monocouche. Ainsi, en y incluant une description précise des capacités de grille et de l'environnement électromagnétique (EM), ce travail étend également les aptitudes de ce modèle à la simulation RF. Sa précision est évaluée en le comparant à la fois avec un modèle numérique et avec des mesures de différentes technologies GFET. Par extension, un modèle grand signal pour les transistors FET à double grille à base de graphène bicouche est présenté. Ce modèle considère la modélisation de l'ouverture et de la modulation de la bande interdite (bandgap) dues à la polarisation de la grille. La polyvalence et l'applicabilité de ces modèles compacts des GFETs monocouches et bicouches ont été évalués en étudiant les GFETs avec des altérations structurelles.

Les aptitudes du modèle compact sont encore étendues en incluant des lois de vieillissement qui décrivent le piégeage de charges et la génération d'états d'interface qui sont responsables de la dégradation induite par les contraintes de polarisation. Enfin, pour évaluer les aptitudes du modèle compact grand signal développé, il a été implémenté au niveau de différents circuits afin de prédire les performances par simulations. Les trois architectures de circuits utilisées étaient un amplificateur triple mode, un circuit amplificateur et une architecture de circuit « balun ».

Mots-Clés : bicouche, fiabilité, graphène, modèle compact, monocouche, Verilog-A.

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INTRODUCTION

The discovery of the appealing electronic and physical properties of graphene was first achieved by isolating single layers of graphene from graphite in the last decade [1]. Since then, Graphene Field-Effect Transistors (GFETs) have been studied extensively as a central element to complement and extend silicon-based electronics for future high-performance circuit applications. Among the several carbon allotropes, graphene appears to be advantageous for high-speed electronics because of its 2-D structure that can provide very high carrier mobilities. Besides, a major advantage of graphene lies in its compatibility for integration into the existing process fabrication flow of silicon-based technologies. Despite being in an early stage of development, several recent works targeting high-frequency applications using graphene-based devices have been proposed. With a similar motivation, this thesis presents a comprehensive study of GFET devices in order to realize accurate electrical compact model solutions for future high-speed circuit design.

A) Background

Ever since, the first functional Field-Effect Transistor (FET) was reported in 1952 [2], the improvement of the performances by making the electronic components smaller, faster and cheaper has been a constant motivation for the electronics industry over several decades. In his attempt to predict the future, Gordon Moore proposed in 1965 what was later called the Moore's law [3] where he predicted that the number of transistors in an integrated circuit doubles approximately every two years. Since then, all the semiconductor industries have diligently followed this law in their manufacturing process. However, in the last few years, Moore's law has started to seem unattainable as the size of the silicon transistors has been shrunk down to the atomic scale. With the drastic

scaling down of transistors, the normal laws of physics would be impacted by quantum effects and new technological challenges [4] arise as a consequence, which sets a limit to further development. Therefore, a strategy to overcome these limitations has been introduced and is known as “More Moore” (Figure 0.1). This strategy focuses on enhancing the performances of the devices further by introducing new technology processes without altering its functional principle such as by introducing strained silicon [5] or high-K gate insulators [6]. In addition, a second trend named “More-than-Moore” (Figure 0.1) has been introduced and it is characterized by the diversification of the semiconductor-based devices. This means that digital and non-digital functionalities such as analog signal processing, sensors, actuators, biochips, etc. are integrated into compact systems in order to extend the range of applications fields.

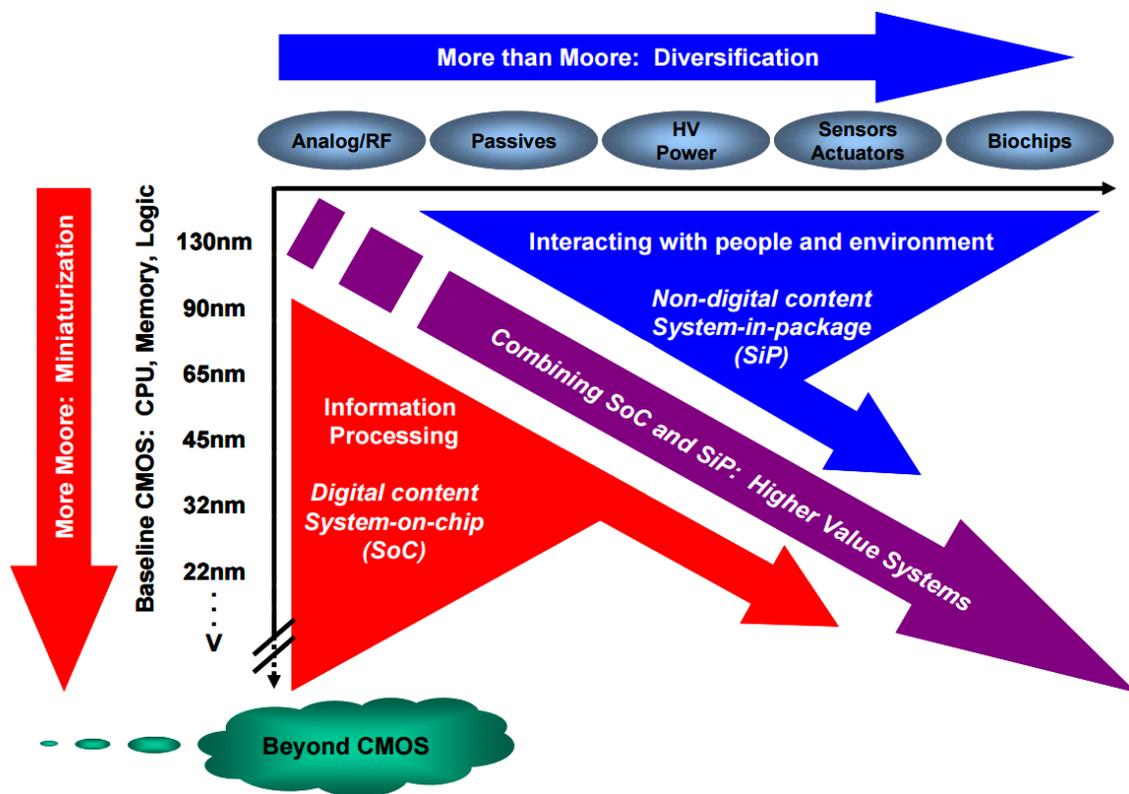


Figure 0.1: Trend in the International Technology Roadmap for Semiconductors. “More Moore” stands for miniaturization of the digital functions, “More than Moore” stands for the functional diversification and “Beyond CMOS” stands for future devices based on completely new functional principles [7].

A third strategy known as “Beyond CMOS” (Figure 0.1) has also been introduced that suggests the replacement of CMOS technology. Therefore, the scientific community has been intensively searching for alternate means in order to propose new materials and device architectures. Consequently, since the first report of the isolation of single atom thick graphene layers by

Novoselov *et al.* [1], graphene has become the center of attention in beyond CMOS community due to its very promising properties such as high carrier mobilities, thus making graphene seem suitable for RF (Radio-Frequency) applications.

B) Carbon-based Devices for Nanoelectronics

In the last few decades, the family of known carbon allotropes has been significantly extended. In addition to the well-known carbon allotropes (coal, diamond and graphite), new allotropes (Figure 0.2) have been investigated for electronics such as buckminsterfullerene [8] (1985), carbon nanotubes (CNT) [9] (1991) and graphene [1] (2004).

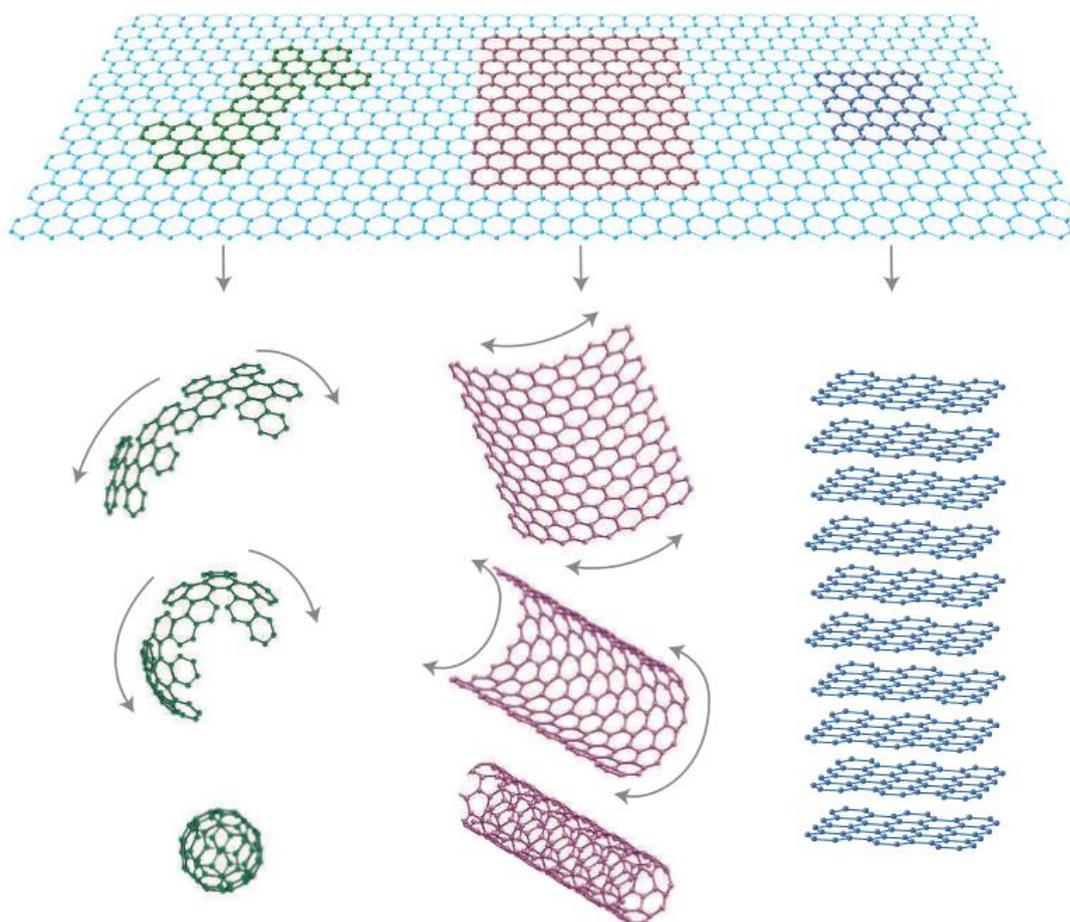


Figure 0.2: Carbon allotropes: buckminsterfullerene, carbon nanotubes (CNTs) and graphene [10]

Although buckminsterfullerene has been considered for FET fabrication [11], still little is known about the actual properties of buckminsterfullerene-based FET. On the other hand, physics of CNTs are quite extensively studied and the CNTs can be categorized into two groups: single walled CNTs and multi-walled CNTs. Several works have demonstrated the potential of CNT for

future generation integrated circuits such as high current densities [12], high thermal conductivity [13] and tensile mechanical strength [14]. Therefore, numerous works exploiting the advantageous properties of CNT for FET fabrication have been proposed [15], [16].

Graphene, although first believed to be chemically unstable, was finally synthesized in 2004 [1] and since then it has been focus of enthusiasm of several groups in the research community. In addition, the first Graphene FET (GFET) device was reported in 2007 by Lemme *et al.* [17]

Graphene, a 2-D material that can deliver very high carrier mobilities, has specific advantages in its integration to the current fabrication process flow. Several graphene FET fabrication processes have been proposed so far such as mechanical exfoliation [18], liquid phase and thermal exfoliation [19], [20], chemical vapor deposition (CVD) [21] and synthesis on SiC [22]. Among these techniques, chemical vapor deposition appears to be a more viable solution towards graphene-based electronic applications.

One of the most remarkable properties of graphene for electronics is its very high carrier mobility at room temperature [23]. In the absence of ripples and charged impurities, a carrier mobility in excess of 2×10^6 cm²/V·s has been reported [24], [25]. In perspective, carrier mobilities of 1400 cm²/V·s and 8500 cm²/V·s have been obtained for conventional silicon CMOS [26] and gallium arsenide [27], respectively. On the downside, large-area graphene is a gapless material, therefore the applicability of large-area graphene to digital applications is severely compromised and thus it is not suitable for logic applications.

Therefore, in the last few years enormous efforts have been carried out in order to inspect the properties of graphene in high frequency applications. To this end, GFETs with intrinsic cut-off frequencies as high as 350 GHz [28] and 300 GHz [29] have been reported. However, due to the absence of current saturation and high access resistances, the extrinsic cut-off frequencies, f_T , and maximum oscillation frequency, f_{max} , are below 50 GHz. In comparison to other technologies, cut-off frequencies of 485 GHz for 29 nm silicon MOSFET [30], of 660 GHz for 20 nm mHEMT [31] and of 100 GHz for 240 nm CNT FET [32] have been obtained, which highlights that graphene has still to reach the pinnacle of its performance.

C) Motivation of this thesis

High-frequency applications based on graphene FETs have been emerging in the last few years [33]–[45]. With that in mind, the objective of this thesis is to provide accurate solutions for GFET modeling in DC and RF operation regimes. In addition, time-to-market and fabrication costs

being two critical aspects, this thesis covers some of the immediate reliability concerns to assess the maturity of the technology and provides accurate modeling of failure mechanisms responsible for transistor degradation over the circuit lifetime. Finally, as a first step towards high-frequency circuits based on GFETs, different circuit architectures based on GFETs are proposed and studied through simulation in order to predict the circuit performances.

D) Thesis Outline

This thesis is organized into four chapters:

Chapter 1 presents a compact model for monolayer GFETs. The chapter starts by a brief introduction to the physics of monolayer graphene including its energy band structure and its density of states. Then, the chapter presents the state of the art of the compact model evolution. Later, a detailed description of the developed compact model suitable for DC and RF simulation is presented. Since the devices considered in this work have gate lengths higher than 100 nm, the presented compact model is based on the classical drift-diffusion transport approach. Next, the compact model has been validated through comparison with DC and RF measurements from two different technologies (exfoliated and CVD-grown graphene). Moreover, electro-magnetic simulations (EM) have been carried out in order to extract the values of parasitic elements due to the BEOL (Back-End of Line). Finally, the validity and potential of the model have been corroborated by measurements on a different GFET technology with different structure procured through collaboration with the University of New Mexico.

Chapter 2 presents a compact model for bilayer GFETs. Similarly to Chapter 1, the chapter starts by a brief introduction to the physics of Bernal stacked bilayer graphene. A state of the art of models for bilayer GFETs is then provided. Next, the different attributes of the model are described in detail. The model has been validated through comparison with measurements from literature. Finally, the potential of the proposed model has been further studied by validation through comparison with artificially stacked bilayer graphene devices procured through collaboration with the University of Siegen.

Chapter 3 addresses the extension of the compact model presented in Chapter 1 to account for critical degradation issues of graphene FET devices. This part of the work has been carried out in collaboration with Chhandak Mukherjee, a post-doctoral researcher at IMS laboratory. The chapter starts by a state of the art of reliability studies on graphene FETs. Next, aging studies are performed via stress measurements and aging laws have been implemented in the compact model. Finally, the

accuracy of the aging compact model is validated through comparison with reported bias-stress measurement results as well as aging measurements carried out at IMS Laboratory.

Chapter 4 presents three different circuit architectures based on GFET devices in order to explore the circuit level simulation capabilities of the compact models presented in Chapter 1 and Chapter 2. First, a triple mode amplifier based on bilayer graphene FET is presented and studied through simulation. Next, the performances of an amplifier using a SiC GFET are evaluated through comparison of measurement results with simulation results. Finally, a balun architecture based on SiC GFETs is presented and its performances have been evaluated through EM-SPICE co-simulations.

Finally, the conclusion provides an overview of this work and perspectives for further works.

Chapter 1

MONOLAYER GFET COMPACT MODEL

Graphene, the first of the so-called 2-D materials, continues to grow as a central material for future high-performance graphene Field-Effect Transistors (GFET) circuit applications owing to its appealing electronic properties. Thereby, development of models providing an insight into the carrier transport in GFET devices is highly desirable. This chapter provides a brief introduction to the physics of monolayer graphene followed by a description of the primary aspects relevant for modeling of Monolayer GFETs (m-GFETs) towards circuit design applications. Then, an overview of the state of the art of existing compact models for Monolayer GFETs is presented. Next, the developed compact model and its different modules are presented. Thereafter, the accuracy of the model has been validated through comparison with measurements of two different GFET technologies that include exfoliated graphene FETs reported by [46] and CVD-grown graphene FETs acquired in collaboration with the University of Lille [47]. Finally, the potentials of the m-GFET model have been evaluated through measurement on a novel GFET technology procured in collaboration with the University of New Mexico.

A) Physics of graphene

1. Energy Band Structure

Carbon is the 15th most abundant element on Earth and many different carbon based structures can be found in nature or be synthesized due to the flexibility of its bonding. Graphene is

a one atom thick 2-D carbon allotrope and has a hexagonal structure of sp²-bonded atoms as shown in Figure 1.1a.

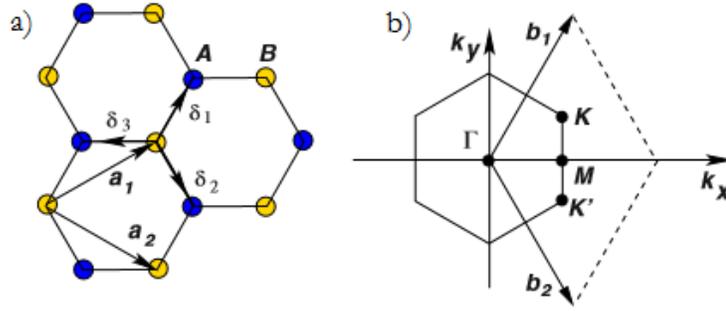


Figure 1.1. a):Graphene honeycomb lattice structure and b) : Brillouin zone[48].

In Figure 1.1, \mathbf{a}_1 and \mathbf{a}_2 are the lattice unit vectors and δ_1 , δ_2 and δ_3 are the nearest neighbor vectors. The two points K and K' in Figure 1.1b are called the Dirac points. The lattice vectors can be written as [48]:

$$\mathbf{a}_1 = \frac{a}{2}(3, \sqrt{3}) \quad \mathbf{a}_2 = \frac{a}{2}(3, -\sqrt{3}) \quad (1)$$

with $a \approx 1.42 \text{ \AA}$ being the carbon-carbon distance.

Graphene possesses an unusual energy band structure relative to conventional semiconductors. Considering a tight binding Hamiltonian for electrons in graphene, and assuming that electrons can hop to both the nearest- and the next-nearest-neighbor atoms; the energy bands can be derived as the following relations [48]:

$$E_{\pm}(\mathbf{k}) = \pm t \sqrt{3 + f(\mathbf{k}) - t' f(\mathbf{k})} \quad (2)$$

$$f(\mathbf{k}) = 2 \cdot \cos(\sqrt{3}k_y a) + 4 \cdot \cos\left(\frac{\sqrt{3}}{2}k_y a\right) \cos\left(\frac{3}{2}k_x a\right) \quad (3)$$

where $t = 2.8 \text{ eV}$ is the nearest neighbor hopping energy, t' is the next nearest-neighbor hopping energy and \mathbf{k} is the wave vector. Figure 1.2 shows the resultant electronic band structure.

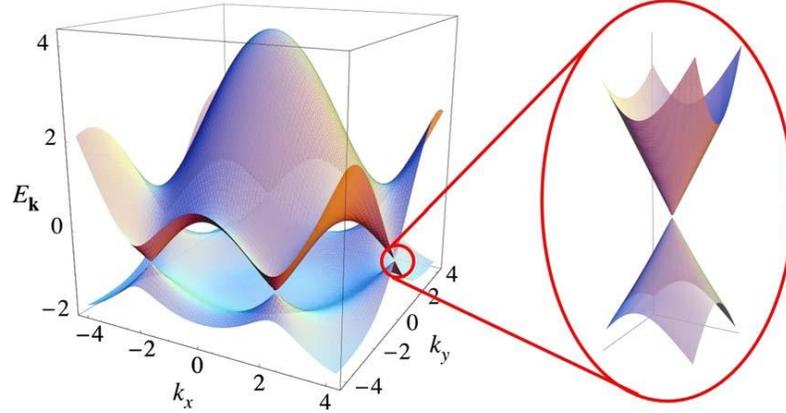


Figure 1.2. Electronic band structure of graphene [48]

Moreover, the inset in Figure 1.2 shows that the valence and conduction bands meet at particular points known as Dirac points. Thereby, graphene is classified as a semimetal due to the absence of an energy bandgap. Based on (2) and (3), the energy dispersion of mobile carriers close to the Dirac point (in the first Brillouin zone) can be approximated to a linear expression given by [49]:

$$E_{\pm}(\mathbf{k}) = s\hbar v_F |\mathbf{k}| \quad (4)$$

where \hbar is the reduced Planck constant and s stands for the conduction band when positive and likewise stands for the valence band when it is negative. v_F is the Fermi velocity given by $v_F = 3at/2\hbar$ which could be approximated to $v_F \approx 10^6 \text{ m/s}$.

2. Density of States and Carrier Sheet Densities

The Density of States (DOS) describes the number of states available for occupation per interval of energy. Derived from the tight-binding Hamiltonian for electrons in graphene, an analytical expression for the Density of States can be obtained which has been plotted in Figure 1.3a [48]. From Figure 1.3b, close to the Dirac point, the Density of States can be approximated by a linear function given as [49]:

$$\rho_{Gr}(E) = \frac{g_s g_v}{2\pi(\hbar v_F)^2} |E| \quad (5)$$

where $g_s = 2$ and $g_v = 2$ are the spin and degeneracy factors, respectively.

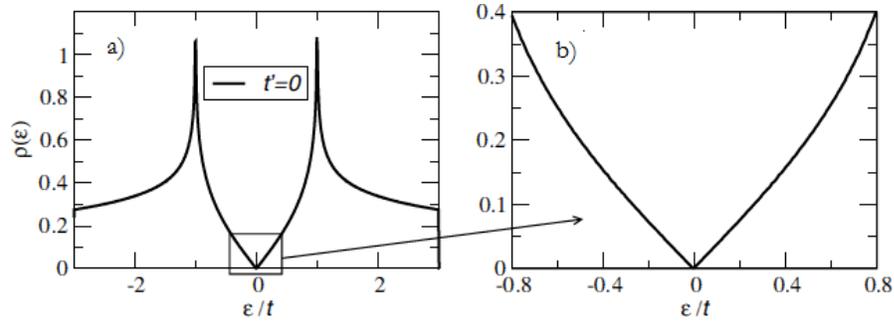


Figure 1.3. a) Density of States per unit cell as a function of energy for $t' = 0$ and b) Zoom in to the Density of States close to the neutrality point [48]

B) Physical Modeling of GFETs

As 2-D materials, in particular graphene, are more frequently being used to constitute electronic devices, the development of accurate representative electrical compact models is required for advantageous circuit design. In the following, a detailed description of our developed compact model is presented.

Our developed compact model is based on the conventional Dual Gate Monolayer Graphene Field-Effect Transistor (m-GFET) structure with monolayer graphene as the channel material. The m-GFET structure is shown in Figure 1.4. The monolayer graphene film is located between a top-gate dielectric (ϵ_{top} , t_{top}) and a back-gate dielectric (ϵ_{back} , t_{back}). The source and drain ohmic contacts as well as the top-gate stack are located on top of the structure. The back-gate stack consists of the back-gate dielectric and the substrate.

In the following subsections, the principal factors for developing an m-GFET model are described.

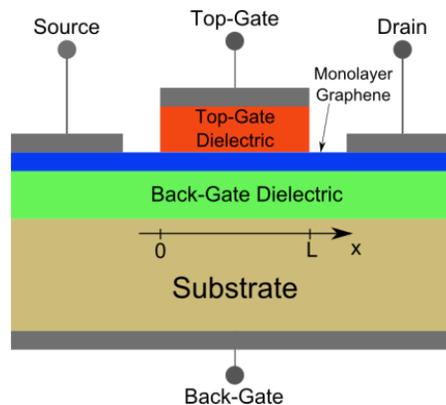


Figure 1.4. Cross-sectional view of the m-GFET structure

1. The Quantum Capacitance

The quantum capacitance, first introduced by Serge Luryi in 1988 [50], is an important modeling parameter to consider, especially in a two plate capacitor, with one of the plates having a finite Density of States such as in graphene [51]. Hence, to properly describe the top-gate capacitance, C_G , one needs to account for this finite Density of States of graphene by considering a quantum capacitance, C_q , in series with the electrostatic top-gate capacitance C_{top} ($= \frac{\epsilon_0 \epsilon_{top}}{t_{top}}$) as shown in Figure 1.5. Here, ϵ_{top} and t_{top} are the dielectric constant and the thickness of the top-gate dielectric. Importantly in some cases, especially for ultrathin high-K dielectrics, the quantum capacitance becomes dominant over the electrostatic top-gate capacitance rendering its modeling essential.

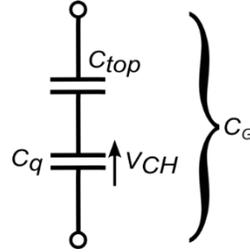


Figure 1.5: Top-Gate Capacitance, C_G

For graphene, considering that the carrier distributions in the channel follow a Fermi-Dirac distribution, the quantum capacitance, C_q , is given by [49]:

$$C_q = \frac{2q^2 k_B T}{\pi (\hbar v_F)^2} \ln \left\{ 2 \left[1 + \cosh \left(\frac{q V_{CH}}{k_B T} \right) \right] \right\} \quad (6)$$

where q is the electronic charge, k_B is the Boltzmann constant, T is the room temperature and V_{CH} is the channel voltage.

2. Differentiation of Carrier Transport Behavior

Much of the interest in graphene as a channel material resides in its very high intrinsic carrier mobilities which could be as high as $2 \times 10^6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for suspended graphene [25] as well as because of the possibility of modulating the carrier density as a function of an electric field [17]. However, during the fabrication of the gate dielectric, defects in the graphene lattice at the gate-dielectric/graphene interface are formed which considerably decrease the intrinsic carrier mobility due to scattering [52].

In addition, different carrier mobilities for holes and electrons arising from slightly different effective masses may cause an asymmetry in the transport behavior of electrons and holes often discerned in the transfer characteristics of the m-GFETs. Moreover, holes and electrons present different cross-sections for impurity scattering [53], [54] which can make the asymmetry further prominent. Moreover, due to the effect of the substrate, the carrier mobility differs for electrons and holes [55].

Furthermore, the parasitic series resistance (Figure 1.6), which includes both the contact resistance, R_C , and the access resistance, R_{Access} , is an important factor contributing to this asymmetry since depending on the polarity of the channel carrier, the charge transfer between the graphene sheet and the metal contacts leads to the creation of either a p-p or p-n junction enhancing the asymmetry in the m-GFET transfer characteristics [56].

Hence, an accurate description of the different electron and hole transport behavior in the graphene channel is required.

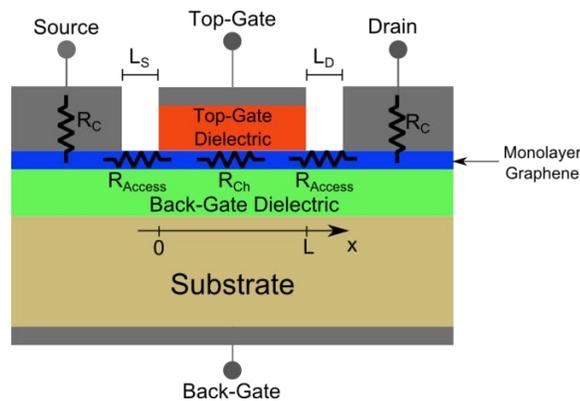


Figure 1.6: Cross-sectional view of the m-GFET structure with definition of the parasitic series resistances

3. The Saturation Velocity

Under an applied external electric field induced by the applied bias conditions, the carriers in the graphene channel move with a drift velocity written as:

$$v_{drift} = \mu E \quad (7)$$

where μ is the carrier mobility and E the applied electric field. However, Monte Carlo simulations [57]–[59] have shown that when the electric-field is increased, (7) is no longer valid and the drift velocity shows a soft-saturation (Figure 1.7) [60], which for a fixed value of temperature could be approximated by the following expression [61]:

$$v_{drift} = \frac{\mu E}{\left[1 + \left(\frac{\mu |E|}{v_{sat}}\right)^\beta\right]^{1/\beta}} \quad (8)$$

with v_{sat} being the saturation velocity of carriers and β a fitting parameter. The saturation velocity, v_{sat} is given by [46]:

$$v_{sat} = \frac{\Omega}{\sqrt{\pi\delta}} \quad (9)$$

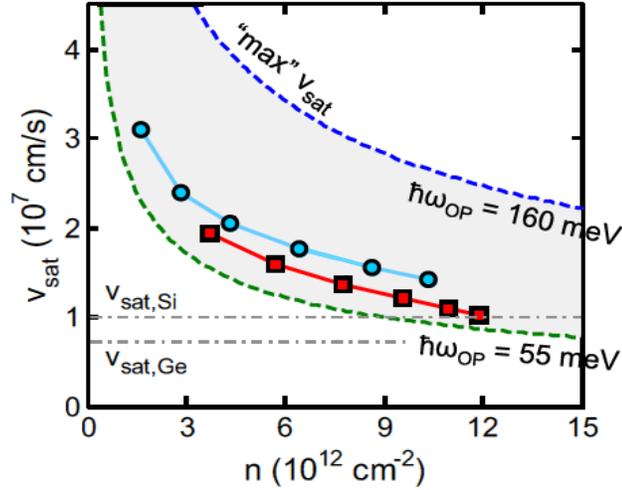


Figure 1.7: Saturation velocity dependency on the carrier density [60] (modified). The red line represents the saturation velocity for $T = 80$ K and the blue line for $T = 300$ K.

Here, (9) considers that the velocity saturation occurs through highly coupled phonon scattering. Since very high coupling to the phonons exists, the electrons are immediately scattered when they obtain the energy threshold necessary for phonon emission. In (9), $\hbar\Omega$ is the effective optical phonon energy and δ the carrier density. As seen in Figure 1.7, the saturation velocity is an important modeling parameter owing to its carrier concentration dependency limited by two mechanisms: The upper limit of the saturation velocity is due to pure graphene which is represented in the model by optical phonon energy of 160 meV; However, the dominant lower limit of the saturation velocity is defined by the substrate phonons (for example, SiO₂ substrate phonons with energy of 55 meV as shown in Figure 1.7).

4. Small-Signal Parameters

One of the high potential applications of graphene-based devices is in RF telecommunications owing to its beneficial properties. Therefore, it is important to study the high-frequency operation of graphene transistors. In most RF applications such as amplifiers, GFETs are

operated in the ON state and an AC small-signal is used as input. The RF performance of a GFET is characterized in terms of its small-signal parameters, such as the transconductance, g_m , the output conductance, g_{ds} , the gate-to-source capacitance, C_{GS} , and the gate-to-drain capacitance, C_{GD} . Thereby, an accurate model is required to precisely represent the mutual capacitances among the gate, source and drain.

C) The Electrical Compact Models

Following the research in the last few years, which is expected to continue in the near future, graphene has been studied to develop system level integrated circuits. Thus, it's highly desirable to develop a physics-based model capable of providing insight into the carrier transport in graphene devices. As a consequence, several models have been developed in the last few years which can be divided into two major groups: physical models and analytical models.

Physical models [62]–[69] provide a better understanding of the carrier transport in the GFET devices. However, being physics-based, their computation time is distinctly higher and their implementation complicated. To name a few : Pugnaghi *et al.* [62] proposed a semi-analytical model for GFETs in the ballistic limit and Champlain [63] presented a theoretical examination of thermal statistics, electrostatics and electrodynamics of GFETs. Moreover, in [64], Champlain presented a small-signal model for GFETs derived from a physical description of the GFET's operation. Ryzhii *et al.* [65] presented a device model that includes the Poisson equation with the weak nonlocality approximation. Thiele *et al.* [66] considered a different modeling approach in which the drain voltage is obtained for a given drain current into the device.

Analytical models [46], [70]–[87] provide sufficient accuracy while considerably reducing the computation time. A common form of analytical models, which is often used by designers for the ease of integration into circuit design flow, is an electrical compact model. The compact models are sufficiently simple and accurate in order be implemented in standard simulators useful for circuit designers and computer aided design. Figure 1.8 shows the evolution of the different analytical models in the last few years. IMS Laboratory from University of Bordeaux has been a major contributor in providing accurate compact models for GFETs since 2012.

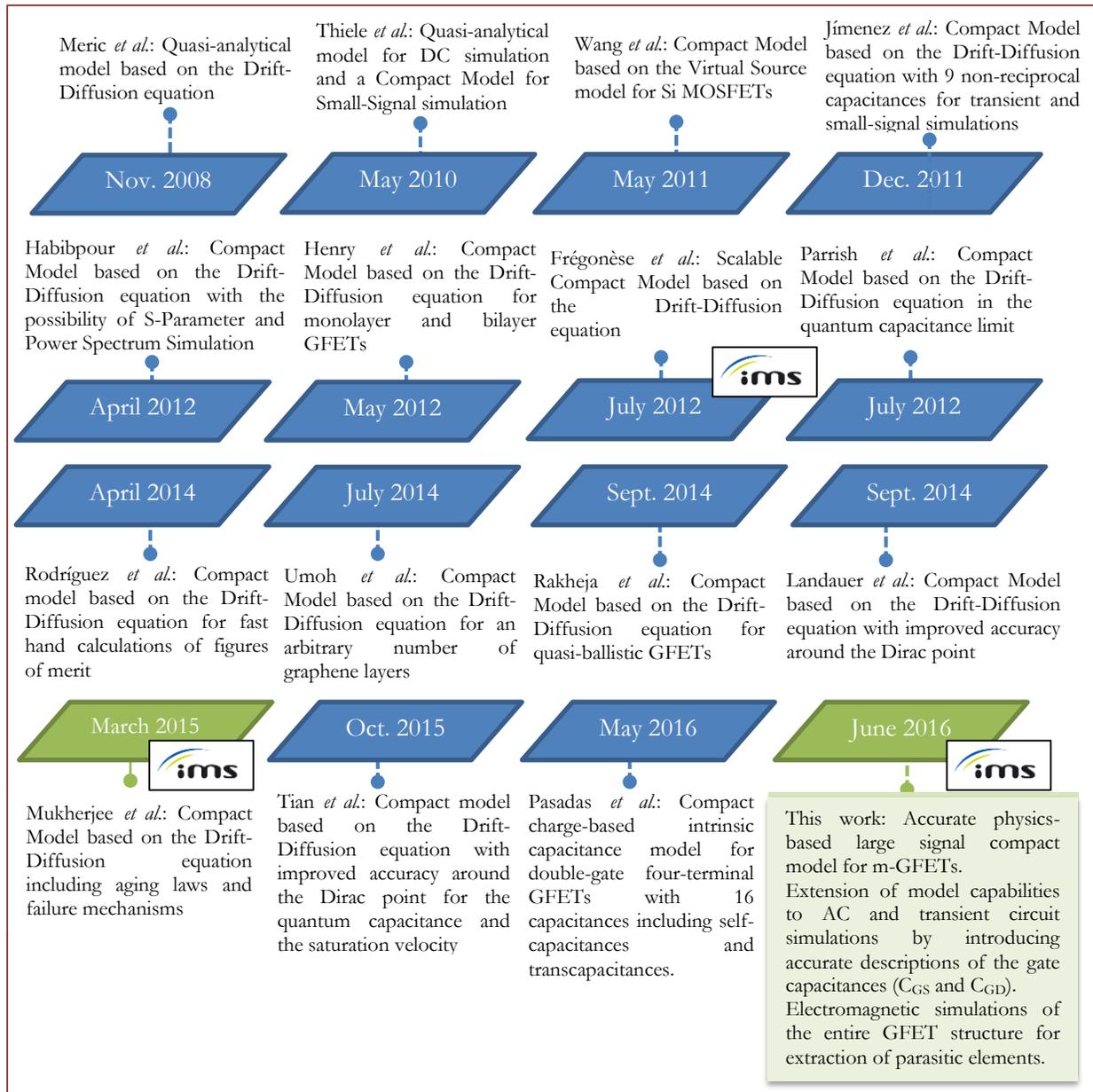


Figure 1.8: Timeline of Compact Model Development

In addition, Table 1 summarizes the key characteristics of each of the models mentioned above. It also highlights where this work stands relative to the models developed thus far.

Table 1: Summary of GFET Compact Model Development

Author	Quantum Capacitance	Different electron and hole mobilities	Access Resistances	Effect of the Back-Gate	Saturation Velocity	RF Simulation	RF Comparison with Measurement
Meric <i>et al.</i> [46]	$C_q \propto \sqrt{n}$	No	No	Yes	Yes, carrier concentration dependent	No	No
Thiele <i>et al.</i> [70]	$C_q \propto V_{CH} $	No	Yes, fitting parameters	Yes	Yes, carrier concentration dependent	No	No
Wang <i>et al.</i> [71]		Yes	Yes, tunable through the effect of the back-gate	Yes	Yes	No	No
Jímenez <i>et al.</i> [72], [73]	$C_q \propto V_{CH} $	No	Yes, fitting parameters	Yes	Yes, carrier concentration dependent in [72]. No, in [73]	It presents nine non-reciprocal capacitances for transient and small-signal simulation	No comparison with measurements
Habibpour <i>et al.</i> [74]	$C_q \gg C_{top}$ valid except for ultrathin top-gate dielectrics	Yes	Different contact resistances are considered when the channel is n- or p-type	No	Yes, carrier concentration dependent	Yes	S-Parameter and Power Spectrum Measurements
Henry <i>et al.</i> [75]	$C_q \propto \sqrt{n}$	No	Yes, Schottky barrier effective resistances	Yes	Yes, carrier concentration dependent	No	No
Parrish <i>et al.</i> [76]	$C_q \ll C_{top}$ in the quantum capacitance	No	No	No	Yes, considered to be material constant	No	No

	limit						
Frégonèse <i>et al.</i> [77], [78]	$C_q \propto V_{CH} $	No	Yes, fitting parameters	No	Yes, carrier concentration dependent	Yes	Yes
Rodríguez <i>et al.</i> [79]	$C_q \propto V_{CH} $	No	Yes, fitting parameters	No	Yes, carrier concentration dependent	Yes	No
Umoh <i>et al.</i> [80]	Separate quantum capacitances ($C_q \propto V_{CH} $) for each layer separated by interlayer capacitances	Yes	Yes, fitting parameters different for holes and electrons	Yes	No	No	No
Rakheja <i>et al.</i> [81]	$C_q \propto \sqrt{V_{CH}^2}$	No	Yes, different contact resistances for n- and p-type channels	Yes	Yes	No	No
Landauer <i>et al.</i> [82]	Weighting function for the quantum capacitance to improve accuracy around the Dirac point	No	Yes, constant contact resistances	Yes	Yes, two region model	No	No
Mukherjee <i>et al.</i> [83]	$C_q \propto V_{CH} $	Yes	Yes, differential resistances across the Schottky junction	Yes	Yes, carrier concentration dependent	No	No
Tian <i>et al.</i> [84]	Weighting function for the quantum capacitance to	Yes, carrier density dependent mobilities	Yes, fitting parameters	Yes	Yes, approximation fitting the two region model by	No	No

	improve accuracy around the Dirac point				[82]		
Iannazzo <i>et al.</i> [85]	$C_q \propto V_{CH} $ Optimization of the model presented in [78]	No	Yes, fitting parameters	No	Yes, carrier concentration dependent	No	No
Pasadas <i>et al.</i> [86], [87]	$C_q \propto V_{CH} $	No	Yes, fitting parameters	Yes	Constant	Yes	Comparison to numerical simulations of the capacitances. Benchmarked against high-performance and ambipolar electronics' circuits.
This Work [88], [89]	$C_q \propto V_{CH} $	Separation of the hole and electron contributions to the total drain current	Yes, considered to be different for holes and electrons and modulated through the back-gate bias	Three different models for the contact/access resistances	Yes, carrier concentration dependent	Extension of model capabilities to AC and transient circuit simulations by the introduction of an accurate description of the gate capacitances	Extensive validation through comparison with measurements. Electromagnetic simulations of parasitic elements.

D) A Large-Signal Monolayer Graphene Field-Effect Transistor Compact Model for RF-Circuit Applications (This Work) [88], [89]

Despite being in an early stage of development, several works targeting high-frequency applications using graphene-based devices have been proposed, such as amplifiers [33]–[35], mixers [36]–[40], frequency receivers [41], ring oscillators [42], terahertz detectors [43], [44] and even balun architectures [45]. With the continuing development of graphene-based RF circuits, models that are able to accurately describe the GFET behavior in the high frequency domain are quite essential.

To address these issues, in this work, an accurate physics-based large signal compact model for m-GFETs suitable for both DC and RF circuit simulations is presented. Since the devices considered in this work have lengths higher than 100 nm, the presented compact model is based on the classical drift-diffusion transport approach. The proposed model has been implemented in Verilog-A. A separation of the hole and electron contributions to the total drain current has been considered without diminishing the accuracy around the Dirac point in addition to an improved accuracy in the branch current descriptions. In addition, the effect of the back-gate on the induced carrier density and access resistances is considered. Furthermore, the model capabilities have been extended to AC and transient circuit simulations by including an accurate description of the gate capacitances (C_{GS} and C_{GD}). Electromagnetic (EM) simulations of the entire GFET structure have been performed to extract the values of the parasitic elements.

The compact model is based on the conventional dual-gate FET structure presented in Figure 1.4. The back-gate stack includes the back-gate dielectric and the substrate. The different model components are described in the following subsections.

1. The Carrier Densities

Considering Fermi-Dirac distribution and based on the 2-D DOS of monolayer graphene in (5), the 2-D electron and hole gas sheet densities in graphene can be written as:

$$n = \int_0^{+\infty} \rho_{Gr} \cdot f_{FD}(E) dE = \frac{2}{\pi(\hbar v_F)^2} \int_0^{+\infty} \frac{E}{1 + \exp\left(\frac{E - E_F}{k_B T}\right)} dE \quad (10)$$

$$p = \int_{-\infty}^0 \rho_{Gr} \cdot [1 - f_{FD}(E)] dE = \frac{2}{\pi(\hbar v_F)^2} \int_0^{+\infty} \frac{E}{1 + \exp\left(\frac{E + E_F}{k_B T}\right)} dE \quad (11)$$

where f_{FD} is the Fermi-Dirac distribution, k_B , the Boltzmann constant, T , the room temperature and E_F , the Fermi level.

Under the effect of a given set of bias conditions, a voltage drop, $V_{CH}(x)$, across the quantum capacitance, C_q , is created. The channel voltage, $V_{CH}(x)$, along the channel at a distance x causes a variation in the Fermi level. Here, the Fermi level is considered to vary proportionally with the channel voltage and thus $E_F = q \cdot V_{CH}$ where q is the electronic charge. The net carrier sheet density, Q_{net} , stored in the quantum capacitance can be written as:

$$Q_{net}(x) = q \cdot (p - n) = Q_p - Q_n = \frac{2q}{\pi} \left(\frac{k_B T}{\hbar v_F} \right)^2 [F_{FD_1}(\eta) - F_{FD_1}(-\eta)] \quad (12)$$

where F_{FD_j} is the Fermi-Dirac integral for an order j given by:

$$F_{FD_j}(\eta) = \frac{1}{\Gamma(j+1)} \int_0^{+\infty} \frac{\mu^j}{1 + \exp(\mu - \eta)} d\mu \quad (13)$$

with $\eta = \frac{E}{k_B T}$ and $\mu = \frac{E_F}{k_B T}$. $\Gamma(n) = (n-1)!$ is the Gamma function.

2. The Quantum Capacitance

The quantum capacitance, C_q , accounts for the finite Density of States in a material. Therefore, C_q , is in series with the geometric electrostatic top-gate capacitance. Because of the low values of C_q in graphene, it has a considerable impact in the total gate-capacitance. The quantum capacitance is defined as the derivative of the net carrier sheet density, Q_{net} , with respect of the channel voltage, V_{CH} , as in an ordinary capacitor and it can be written as in (6). However, to considerably simplify the electrostatics calculations, it is helpful to assume $q \cdot |V_{CH}| \gg k_B T$ and thus the quantum capacitance can be written as [49]:

$$C_q(x) = \frac{2q^2 k_B T}{\pi (\hbar v_F)^2} \ln \left\{ 2 \left[1 + \cosh \left(\frac{q V_{CH}(x)}{k_B T} \right) \right] \right\} \xrightarrow{q \cdot V_{CH} \gg k_B T} C_q = \frac{2q^2 q \cdot |V_{CH}(x)|}{\pi (\hbar v_F)^2} \quad (14)$$

Yet, in the vicinity of Dirac point, (14) underestimates the carrier density (Figure 1.9) resulting in a diminished accuracy. Nonetheless, in order to keep the compact model simple, the quantum capacitance is further considered to vary linearly as a function of the channel voltage as suggested by (14).

Finally, under this approximation, the net carrier density, Q_{net} , is written as:

$$C_q(x) = -\frac{dQ_{net}(x)}{dV_{CH}} \Rightarrow Q_{net}(x) = -\int C_q dV_{CH} = -\frac{q^2 q \cdot |V_{CH}| V_{CH}}{\pi (\hbar v_F)^2} \quad (15)$$

The negative sign of C_q in (15) can be explained as follows [70]: a more positive gate voltage and in turn a more positive V_{CH} leads to a more negative charge in the graphene channel.

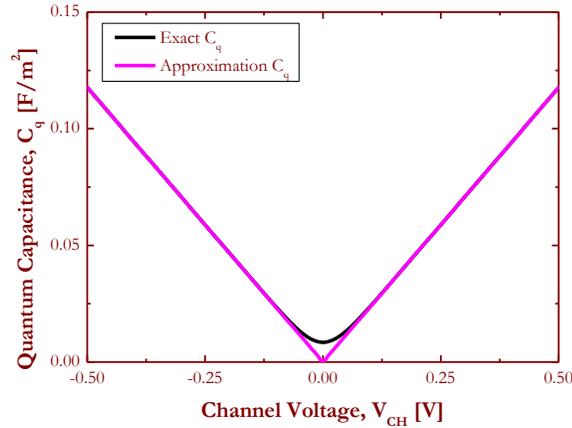


Figure 1.9: Quantum Capacitance, C_q , versus Channel Voltage, V_{CH}

3. The Channel Voltage

Considering the GFET structure in Figure 1.4, an equivalent capacitive circuit can be established as in Figure 1.10.

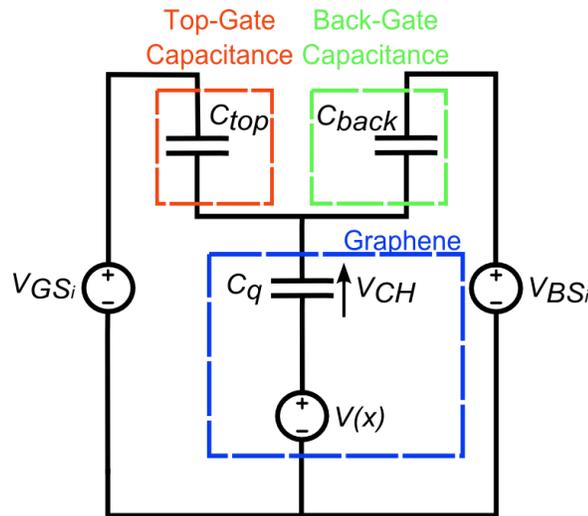


Figure 1.10 : Equivalent capacitive circuit of the m-GFET structure

In Figure 1.10, V_{GS_i} and V_{BS_i} represent the top-gate-to-source voltage and the intrinsic back-gate-to-source intrinsic voltages, respectively; V_{CH} represents the voltage across the quantum capacitance and $V(x)$ the voltage drop in the graphene channel due to intrinsic drain-to-source voltage, V_{DS_i} . $V(x)$ varies from $V(0) = 0$ at $x = 0$ to $V(L) = V_{DS_i}$ at $x = L$.

Applying Kirchoff's relation to the equivalent capacitive circuit shown in Figure 1.10, the following can be written:

$$Q_{net}(x) + q \cdot N_F = (Q_{TG}(x) + Q_{BG}(x)) \quad (16)$$

where $Q_{TG}(x)$ and $Q_{BG}(x)$ are top-gate and back-gate induced charges given by:

$$Q_{TG}(x) = C_{top} \cdot [V_{GS_i} - V(x) - V_{CH}(x)] \quad (17)$$

$$Q_{BG}(x) = C_{back} \cdot [V_{BS_i} - V(x) - V_{CH}(x)] \quad (18)$$

N_F accounts for the additional charge due to impurities or doping of the channel. $C_{top} = \frac{\epsilon_0 \epsilon_{top}}{t_{top}}$ and $C_{back} = \frac{\epsilon_0 \epsilon_{back}}{t_{back}}$ are the top- and back-gate capacitances, respectively. Here, $(\epsilon_{top}, \epsilon_{back})$ and (t_{top}, t_{back}) are the dielectric constants and thicknesses of the dielectric layers. Based on (15)-(18), a second-degree equation for the channel voltage can be written and its solutions are given by:

$$V_{CH}(x) = \text{sign} \left(Q_{tot} - C_{eq} V(x) \right) \frac{-C_{eq} + \sqrt{C_{eq}^2 + 4\alpha |Q_{tot} - C_{eq} V(x)|}}{2\alpha} \quad (19)$$

with $\alpha = \frac{q^3}{\pi(\hbar v_F)^2}$, $C_{eq} = C_{top} + C_{back}$, $Q_{tot} = Q_{top} + Q_{back} + Q_F$, $Q_{top} = C_{top} V_{GS_i}$, $Q_{back} = C_{back} V_{BS_i}$ and $Q_F = q N_F$.

Because of the absence of energy bandgaps in graphene, ambipolar conduction in m-GFET devices is not uncommon. Unlike conventional MOSFET devices where the charges responsible for the drain current are either holes for p-MOSFETs or electrons for n-MOSFETs, in ambipolar devices the conduction across the graphene channel is assisted by either electrons ($\forall x \in [0, L], V_{CH}(x) > 0$), holes ($\forall x \in [0, L], V_{CH}(x) < 0$) or a combination of both ($\exists x_0 \in [0, L], V_{CH}(x_0) = 0$). This implies that, the channel voltage, $V_{CH}(x)$, determined from the bias conditions as depicted in (19), controls whether the channel is n-type, p-type or ambipolar.

Considering the channel voltage, V_{CH} , to be positive the channel is full of electrons and thus the following can be assumed based on (15):

$$\begin{aligned} Q_{net}(x) &= Q_p(x) - Q_n(x) \approx -Q_n(x) \Rightarrow Q_n(x) = \alpha V_{CH}^2 \\ Q_p(x) &\approx 0 \end{aligned} \quad (20)$$

where Q_n and Q_p are the hole and electron charge contributions, respectively. Figure 1.11a is a representative image with standard values displaying the net carrier density, Q_{net} , and the channel voltage, V_{CH} , variation along the channel.

Similarly, when V_{CH} is negative, and thus the channel is full of holes, the following approximation is valid:

$$Q_{net}(x) = Q_p(x) - Q_n(x) \approx Q_p(x) \Rightarrow Q_p(x) = \alpha V_{CH}^2 \quad (21)$$

$$Q_n(x) \approx 0$$

Similarly, Figure 1.11b illustrates the channel voltage and the net carrier density when the channel is p-type.

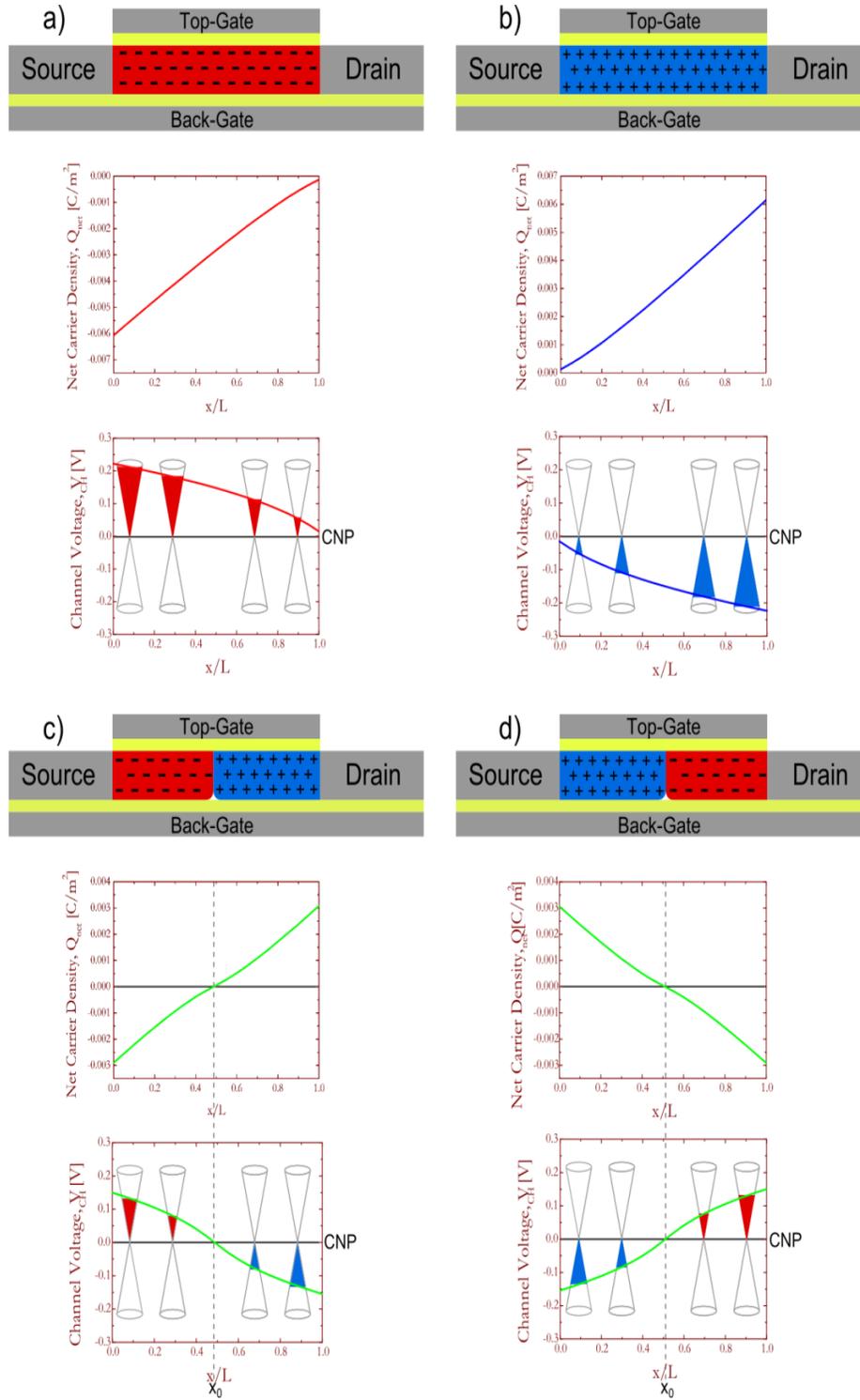


Figure 1.11: GFET channel conditions a) n-type channel, b) p-type channel, c) n-type to p-type channel and d) p-type to n-type channel. CNP is the charge neutrality point.

However, when $(\exists x_0 \in [0, L], V_{CH}(x_0) = 0)$ is valid, ambipolar conduction occurs. Considering the case in Figure 1.11c, where a transition occurs from an n-type channel to a p-type channel, the following expressions can be written:

$$\begin{aligned} \forall x \in [0, x_0], V_{CH}(x) > 0 &\Rightarrow Q_n(x) = \alpha V_{CH}^2(x) \text{ and } Q_p(x) = 0 \\ \forall x \in (x_0, L], V_{CH}(x) < 0 &\Rightarrow Q_p(x) = \alpha V_{CH}^2(x) \text{ and } Q_n(x) = 0 \end{aligned} \quad (22)$$

Equivalently, when a transition occurs from a p-type channel to an n-type channel (Figure 1.11d), the following can be assumed:

$$\begin{aligned} \forall x \in [0, x_0], V_{CH}(x) > 0 &\Rightarrow Q_p(x) = \alpha V_{CH}^2 \text{ and } Q_n(x) = 0 \\ \forall x \in (x_0, L], V_{CH}(x) < 0 &\Rightarrow Q_n(x) = \alpha V_{CH}^2 \text{ and } Q_p(x) = 0 \end{aligned} \quad (23)$$

4. The Drain-to Source Current

Based on the drift-diffusion theory of transport, the drain-to-source current, I_{DS} , can be written as:

$$I_{DS} = -W \cdot Q(x) \cdot v_{drift}(x) \quad (24)$$

where $Q(x)$ is the carrier density in the channel at a position x from the source, $v_{drift}(x)$ is the drift velocity of carriers and W the gate width. In (24), the drain-to-source current is assumed to be constant at any point x in the channel.

Considering a soft-saturation of the drift velocity as in (8) and assuming $\beta = 1$, (24) is further written as:

$$I_{DS} = -W \cdot Q(x) \cdot \frac{\mu E}{1 + \frac{\mu |E|}{v_{sat}}} \xrightarrow{E = -\frac{dV(x)}{dx}} -W \cdot Q(x) \cdot \frac{\mu \left(-\frac{dV(x)}{dx}\right)}{1 + \frac{\mu \left|-\frac{dV(x)}{dx}\right|}{v_{sat}}} \quad (25)$$

where μ is the average carrier mobility.

Integrating by separation of the x-dependent terms on one side and V-dependent terms on the other side, the drift-diffusion drain-to-source current, I_{DS} , is given by:

$$I_{DS} = \mu W \frac{\int_0^{V_{DSi}} |Q| dV}{L + \mu \left| \int_0^{V_{DSi}} \frac{1}{v_{sat}} dV \right|} \quad (26)$$

Although, (26) considers an average carrier mobility, μ , that accounts for most of the ambipolar GFET operations, in several cases, different electron and hole transport behavior in the graphene channel is observed and expression (26) is no longer valid. To expand the model capabilities and account for an asymmetric conduction behavior, different mobilities for holes and

electrons must be considered implying different levels of contribution to the total drain current. To consider the aforementioned, the total drain current has been assumed to be the sum of the electron and hole contributions:

$$I_{DS} = I_{DS_n} + I_{DS_p} \quad (27)$$

Equation (27) is used specifically to account for the ambipolar conduction in the graphene channel. The total current is the sum of the electron and hole currents and the calculation of the I_{DS_n} and I_{DS_p} are self-consistent regarding the direction of the current flow for each branch. Considering for example when the channel is entirely n-type and the current flows from the drain to source for V_{GS} and V_{DS} both being positive. On the other hand, for the same V_{DS} , if V_{GS} becomes sufficiently negative, the channel becomes entirely p-type and holes are pushed from the drain to the source maintaining the same direction of the hole current as that of the electron. In either of these cases, there is negligible contribution of the minority carrier that also has the same direction of current flow as that of the majority carriers. Lastly, when $V_{GS} \approx V_{Dirac}$, the charge neutrality point is located within the channel and the same direction for the electron and hole currents is maintained. In addition to this, a significant electron-hole recombination takes place which however does not cause energy dissipation due to the gapless nature of graphene.

5. The Residual Carrier Density

Scanning Tunneling Microscopy (STM) studies [90], [91] have shown the presence of electron and hole puddles in the graphene layer. These electron and holes puddles are the result of the inevitable presence of disorder in the graphene layer. They account for the anomalously finite conductivity, however minimal, observed around the Dirac point. This unexpected behavior has been attributed to first, mesoscopic corrugations (ripples) [92], [93] leading to a fluctuating Dirac point, and second, to charged impurities leading to an inhomogeneous carrier density [94], [95].

Considering that the areas of the hole and electron puddles are equal in size, the spatial electrostatic potential is simplified as a step function with a peak to peak value of $\pm\Delta$ as shown in Figure 1.12. The residual carrier density due to electron and hole puddles is written as:

$$n_{puddle} = \frac{\Delta^2}{\pi(\hbar v_F)^2} \quad (28)$$

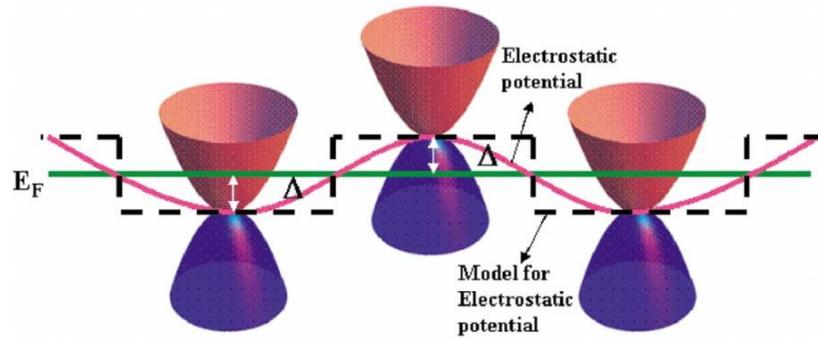


Figure 1.12: Spatial inhomogeneity of the electrostatic potential [96]

6. The Parasitic Series Resistances

As described in Section B), the parasitic series resistances including the access resistances and contact resistances are important parameters that need to be properly modelled as they represent a serious issue leading to degradation of the GFET performance, especially when the device dimensions are scaled down [97]. In fact, scaling down the channel increases the drain current level while, the parasitic series resistances are not scaled down and eventually the parasitic series resistance can dominate the total resistance in highly scaled devices. Moreover, most of the GFET devices have access resistances which are not optimized, i.e. the graphene in the access regions has a low carrier density (given by the quality of graphene and process) leading to a highly resistive access. In order to increase the carrier density within the access regions, one can build a back-gate or generate defects in the access region [98].

Thereby, here, three different models (empirical, Schottky barrier height and Back-Gate charge modulation) are proposed to accurately describe the effect of the parasitic series resistances, R_S and R_D , on the GFET performance. For ease of implementation and as a first attempt, an empirical model has been developed in order to account for the different access resistance whether the graphene in the source/drain access region is n-type or p-type. Later, in order to give a physical interpretation to the empirical model, a Schottky barrier model has been developed. In this model, the access resistances are modeled as a function of the barrier height between the metal and the graphene interface accounting for different graphene sheet polarities. Moreover, a third model has been proposed accounting for the charge modulation in the access regions due to the effect of the back-gate voltage. In the following, the proposed models for the parasitic series resistances are described in detail.

a) Empirical Model

This model considers that, because of the back-gate effects as well as due to possible doping during the metallization, the graphene regions underneath the metal contacts can be either n-type or p-type and thus, a junction is formed at the drain and the source sides. It follows that, depending on the channel's polarity, different parasitic series resistances need to be considered. For this, first an empirical model is considered based on a smoothing function which considers a transition between a resistance, $R_{(S,D)_{n0}}$, when the channel is n-type and a resistance, $R_{(S,D)_{p0}}$, when the channel is p-type.

The aforementioned smoothing function can be written empirically as:

$$f_{SmR} = \frac{1}{1 + \exp\left(\frac{I_{DSn} - I_{DSp}}{\varphi}\right)} \quad (29)$$

where I_{DSn} and I_{DSp} are the electron and hole contributions to the drain current, respectively and φ is a fitting parameter. The width-normalized source and drain parasitic series resistances are given by:

$$\begin{aligned} R_{S_0} &= R_{S_{n0}} \cdot (1 - f_{SmR}) + R_{S_{p0}} \cdot f_{SmR} \\ R_{D_0} &= R_{D_{n0}} \cdot (1 - f_{SmR}) + R_{D_{p0}} \cdot f_{SmR} \end{aligned} \quad (30)$$

b) Schottky Barrier Model

The parasitic series resistances are considered to be different according to whether the channel is n-type or p-type. The contact resistances can be modeled as a function of the barrier height, Φ_B , between the metal and the graphene interface. The barrier height changes with the graphene sheet polarity, *i.e.*, on either side of the Dirac point, and hence different barrier heights are considered in case of the electron (Figure 1.13a) and the hole carriers (Figure 1.13b).

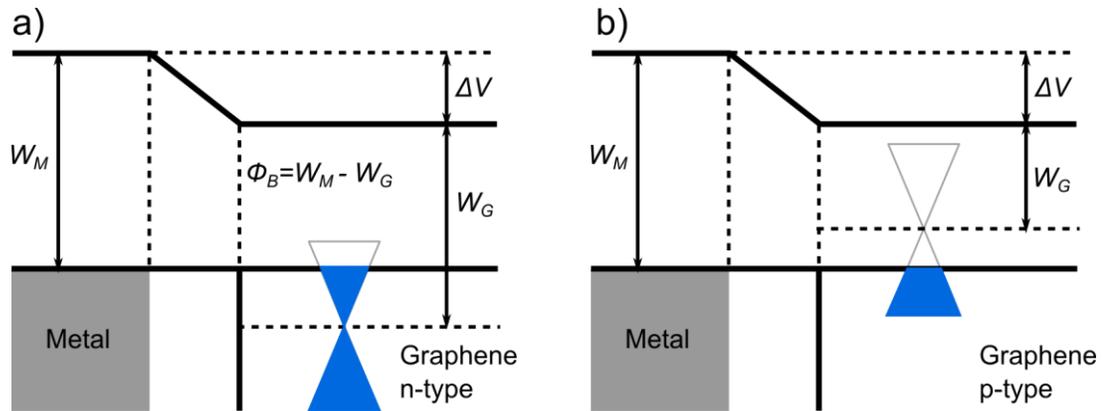


Figure 1.13: Schottky junction formation between the metal and a) n-type or b) p-type graphene channel

Assuming the Richardson's model for the Schottky junction current, it can be written as [99], [100]:

$$I = A^*T^2 \exp\left(-\frac{q\Phi_B}{k_B T}\right) \left[\exp\left(-\frac{qV_A}{k_B T}\right) - 1 \right] \quad (31)$$

with V_A being the applied voltage across the junction and A^* , the Richardson's constant. The differential resistance is given as:

$$r = \left[\frac{qA^*T}{k_B} \exp\left(-\frac{q\Phi_B}{k_B T}\right) \exp\left(-\frac{qV_A}{k_B T}\right) \right]^{-1} = r_0 \exp\left(\frac{q\Phi_B}{k_B T}\right) \quad (32)$$

Therefore, here, the source and drain parasitic resistances can be written as a sum of the differential resistances across the Schottky junction and the metal contact resistance. Considering, the graphene in the source access region to be n-type, the source parasitic resistance is given by:

$$R_{S_0} = R_{C_{S_0}} + r_{S_{0n}} \exp\left(\frac{q\Phi_{B_{S_n}}}{k_B T}\right) \quad (33)$$

where $\Phi_{B_{S_n}}$ is the barrier height between the metal and the graphene(n-type) interface in the source access region. Equivalently, when the source access region is p-type, the source parasitic resistance is:

$$R_{S_0} = R_{C_{S_0}} + r_{S_{0p}} \exp\left(\frac{q\Phi_{B_{S_p}}}{k_B T}\right) \quad (34)$$

where $\Phi_{B_{S_p}}$ is the barrier height between the metal and the graphene (p-type) interface in the source access region. Similarly, in the drain access region, the parasitic series resistance when the drain access region is n-type or p-type is given respectively by:

$$R_{D_0} = R_{C_{D_0}} + r_{D_{0n}} \exp\left(\frac{q\Phi_{B_{D_n}}}{k_B T}\right) \quad (35)$$

$$R_{S_0} = R_{C_{D_0}} + r_{D_{0p}} \exp\left(\frac{q\Phi_{B_{D_p}}}{k_B T}\right) \quad (36)$$

where $(R_{C_{S_0}}, R_{C_{D_0}})$ are the source and drain contact resistances due to the metal, respectively. $(r_{S_{0n}}, r_{D_{0n}}, r_{S_{0p}}, r_{D_{0p}})$ are functions of the voltage difference (V_A) across the access region, but for simplicity, they are assumed to be model parameters considering transfer lengths under the contacts to be insignificant.

c) Back-Gate Charge Modulated Series Resistances

In the drain and source access regions, contact resistances ($R_{C_{S0}}, R_{C_{D0}}$) as well as vertical electric-field-induced modulation of the access resistances ($R_{S_{Ac}}, R_{D_{Ac}}$) are considered. The applied vertical electric field results in the modulation of the charge density in the graphene access regions uncovered by the top-gate stack, thereby these access resistances are only affected by the back-gate and vary independently of the top-gate voltage.

Based on the applied bias conditions, an equivalent capacitive circuit of the m-GFET structure in the access regions is shown in Figure 1.14. In the source access region, a Kirchhoff's relation based on the equivalent capacitive circuit shown in Figure 1.14a can be written as follows:

$$Q_S + q \cdot N_{F_S} = -Q_{BS} \quad (37)$$

where Q_S is the charge stored in the quantum capacitance given by (15), N_{F_S} is the net doping of the graphene layer in the access region and Q_{BS} is the back-gate induced charge given by:

$$Q_{BS} = C_{back} \cdot (V_{BS_i} - V_{CH_{BS}}) \quad (38)$$

with $V_{CH_{BS}}$, being the voltage across the quantum capacitance in the source access region.

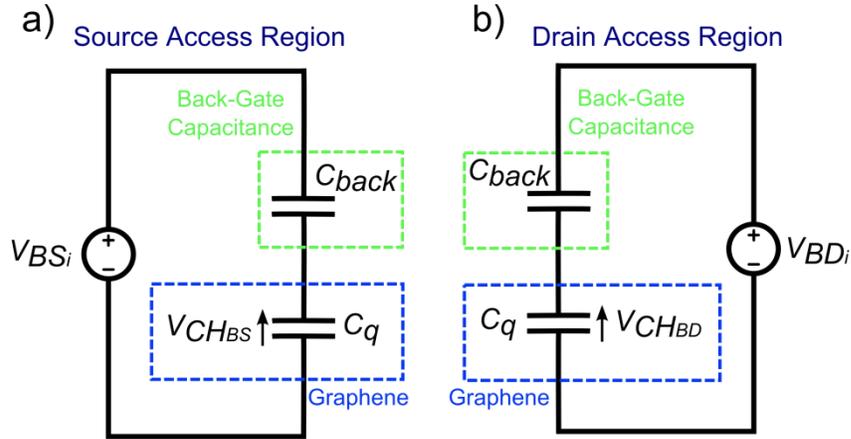


Figure 1.14: Equivalent capacitive circuit of the m-GFET a) source and b) drain access regions

Based on (37)-(38), a second degree equation for $V_{CH_{BS}}$ can be written and its solutions are given by:

$$V_{CH_{BS}} = \text{sign}(Q_{tot_S}) \frac{-C_{back} + \sqrt{C_{back}^2 + 4\alpha|Q_{tot_S}|}}{2\alpha} \quad (39)$$

with $Q_{tot_S} = Q_{back_S} + Q_{F_S}$, $Q_{back_S} = C_{back}V_{BS_i}$ and $Q_{F_S} = qN_{F_S}$.

When electrons are accumulated in the source access region ($V_{CHBS} > 0$), the self-consistent solutions of equations (37) and (39), allows the calculation of the net charge density in the access region, Q_S . The resistance of the source access region is assumed to vary inversely with the induced carrier density due to the effect of the back-gate bias. Thus, the width-normalized parasitic series resistance can be written as the sum of contact resistance and the modulated access resistance as:

$$R_{S_0} = R_{S_{c0}} + \frac{L_S}{\mu_{n_S}(|Q_S| + q \cdot n_{BS})} \quad (40)$$

where μ_{n_S} is the mobility of electrons in the source region, n_{BS} is a residual charge density in the access region and L_S is the source access length.

Similarly, when holes are accumulated in the source access region ($V_{CHBS} < 0$), the width-normalized parasitic series resistance is written as:

$$R_{S_0} = R_{S_{c0}} + \frac{L_S}{\mu_{p_S}(|Q_S| + q \cdot p_{BS})} \quad (41)$$

Here, μ_{p_S} is the hole mobility in the source region and p_{BS} is the residual charge density in the access region.

Similarly to the formulations of the equations (37)-(41), equations for the drain parasitic series resistances can be established based on the equivalent capacitive circuit shown in Figure 1.14b.

7. Gate resistance - Scalable Model

Developing a scalable model is as desirable as it is important for identifying the physical parameters dominantly affected by scaling. Here, the model is scaled with respect to the channel length, L , the channel width, W , and the number of fingers, N_{Fng} . The effect of the gate resistance is significant in RF range as it could lead to an increased thermal noise as well as a reduction of the maximum available gain. The gate resistance depends directly on the physical structure (layout) of the device and at high frequency, it can be modeled as a distributed R-C circuit. Thus, based on transmission-line theory, the gate resistance is given by:

$$R_g = R_{sh} \frac{W}{3LN_{Fng}} \quad (42)$$

where R_{sh} is the gate sheet resistance in Ω/\square .

8. Gate Capacitances

To extend the model capabilities to AC and transient circuit simulations, an accurate description of the gate-to-source, C_{GS} , and the gate-to-drain, C_{GD} , capacitances also needs to be incorporated in the model.

First, an explicit dependence of the total charge in the channel needs to be derived as a function of the node voltages ($V_{GS_i}, V_{BS_i}, V_{DS_i}$) and thus given as follows:

$$Q_{channel} = W \int_0^L (Q_{net} + q \cdot n_{puddle}) dx \quad (43)$$

where n_{puddle} is the residual carrier density due to puddle formation as described in Section 5. For a finite drain-to source voltage, V_{DS_i} , the total gate capacitance is defined as follows [101]:

$$C_{GG} = C_{GS} + C_{GD} = \left(\frac{\partial Q_{channel}}{\partial V_{GS_i}} \right)_{V_{DS_i}=\text{constant}} \quad (44)$$

Based on (44) and considering that $V_{GD_i} = V_{GS_i} - V_{DS_i}$, the gate-to-source, C_{GS} , and gate-to-drain, C_{GD} , capacitances can be written as:

$$C_{GD} = \left(\frac{\partial Q_{channel}}{\partial V_{GD_i}} \right)_{V_{GS_i}=\text{constant}} = - \left(\frac{\partial Q_{channel}}{\partial V_{DS_i}} \right)_{V_{GS_i}=\text{constant}} \quad (45)$$

$$C_{GS} = \left(\frac{\partial Q_{channel}}{\partial V_{GS_i}} \right)_{V_{DS_i}=\text{constant}} + \left(\frac{\partial Q_{channel}}{\partial V_{DS_i}} \right)_{V_{GS_i}=\text{constant}} \quad (46)$$

A simplified large-signal circuit representation of the intrinsic transistor is given in Figure 1.15. The bulk connection has been omitted for sake of clarity. Doing so, the total capacitances between the back-gate and the source and the back-gate and the drain are neglected. In fact, considering a thick back-gate dielectric, which is usually the case, the following equation can be written:

$$\frac{1}{C_{eq}} = \frac{1}{C_{back}} + \frac{1}{C_q} \approx \frac{1}{C_{back}} \quad (47)$$

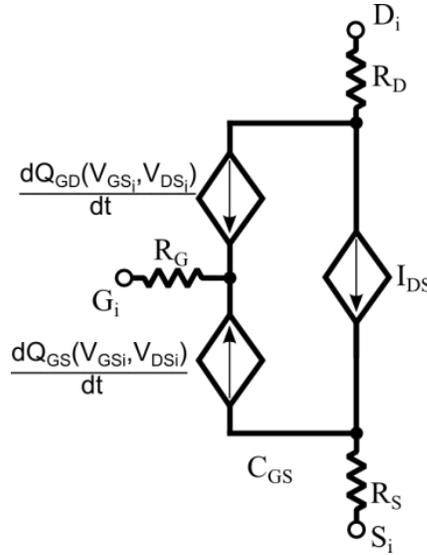


Figure 1.15: Intrinsic Large-Signal Equivalent Circuit

Moreover, in Figure 1.15, Q_{GD} and Q_{GS} are the gate-to-drain and gate-to-source charges, respectively given by:

$$Q_{GD} = C_{GD} \cdot V_{GD_i} \quad (48)$$

$$Q_{GS} = C_{GS} \cdot V_{GS_i} \quad (49)$$

9. Numerical Model [102]

In addition to the compact model, a numerical model (Octave/Matlab) has additionally been developed. The numerical model is based on:

- Non-linear System Solver
- Trapezoidal Numerical Integration
- Numerical Differentiation

This numerical model is implemented using the exact solution of the quantum capacitance in (6) and thus, the compact model has been benchmarked against the numerical model to evaluate its accuracy, particularly due to the considered simplifications. Figure 1.16 shows a block diagram describing the implementation of the numerical model. Moreover, the numerical model allows the extraction of intermediate variables such as the variation of the channel voltage, the saturation velocity and the carrier density along the channel. However, the numerical model being an iterative model with self-consistent calculations, the computation time becomes considerably higher compared to that of the compact model.

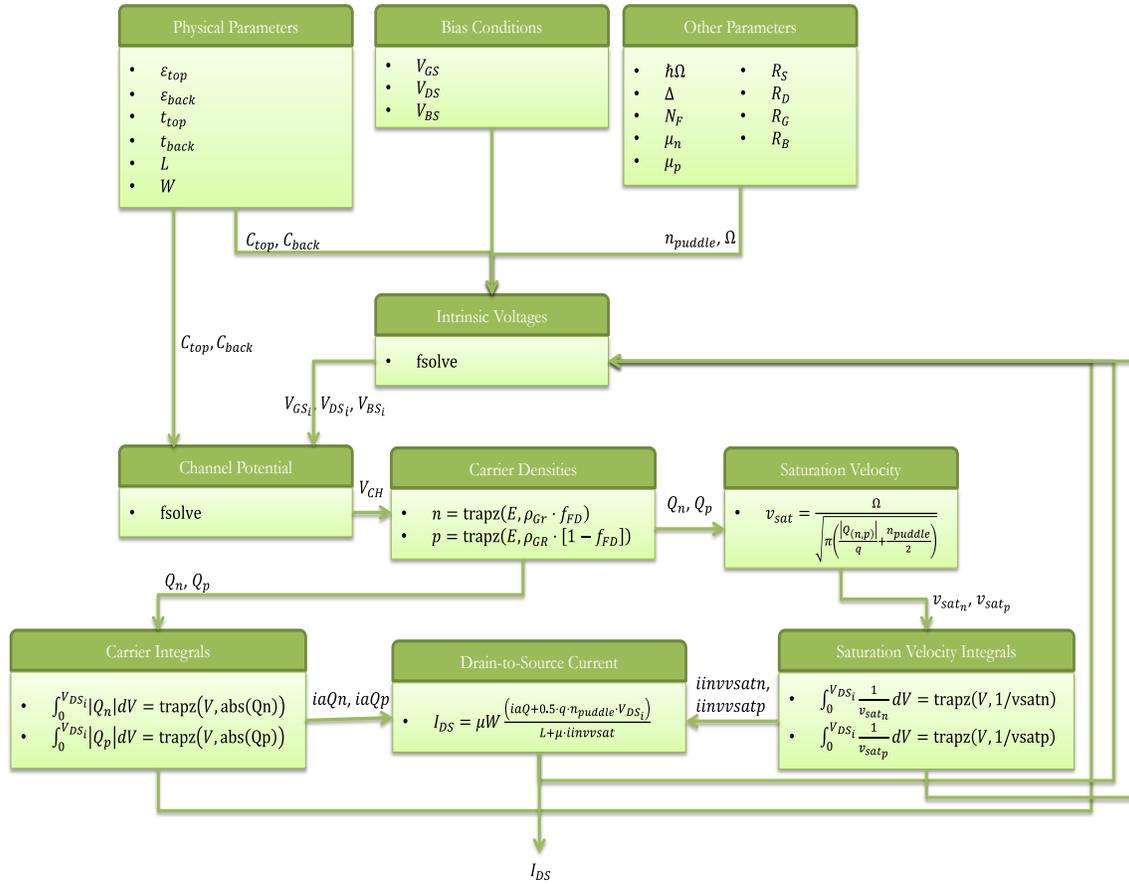


Figure 1.16: Numerical Model Block Diagram; the model utilizes three main functions: ‘fsolve’ to solve non-linear system equations, ‘trapez’ to calculate numerical integrations and ‘diff’ to perform numerical differentiations.

10. Compact Model Implementation

Developing compact models for standard circuit simulators implies developing analytical equations to accurately represent the internal physics of the device. In this section, the implementation of the model is described in accordance with the definitions in previous sections. The model equations have been implemented in Verilog-A for it to be fully compatible with standard circuit simulators.

a) The Drain-to-Source Current

The total drain-to-source current is considered to be sum of the electron and hole contributions which, based on (26) and (28) are written as:

$$I_{DS(n,p)} = \mu_{(n,p)} W \frac{\int \left(|Q_{(n,p)}| + q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_{(n,p)} \left| \int \frac{1}{v_{sat(n,p)}} dV \right|} \quad (50)$$

with $\mu_{(n,p)}$ being the electron/hole mobility. Following from (9), $v_{sat(n,p)}$, the electron/hole concentration-dependent saturation velocity, is given by:

$$v_{sat(n,p)} = \frac{\Omega}{\sqrt{\pi \left(\frac{|Q_{(n,p)}|}{q} + \frac{n_{puddle}}{2} \right)}} \quad (51)$$

The term $n_{puddle}/2$ in (50) and (51) accounts for an even distribution of the residual carrier density in electron and hole puddles.

Eq. (19) indicates that the sign of $V_{CH}(x)$ is determined by the sign of the term:

$$z(x) = Q_{tot} - C_{eq}V(x) \quad (52)$$

Thereby, as explained in Section 3, if $z(x=0)$ and $z(x=L)$ both remain positive, the channel polarity is n-type and the current conduction is supported mostly by electrons (Figure 1.11a). Therefore, based on (20) and (26), the electron and hole current contributions are written as:

$$I_{DSn} = \mu_n W \frac{\int_0^{V_{DSi}} \left(\alpha V_{CH}^2 + q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_n \left| \frac{1}{\Omega} \int_0^{V_{DSi}} \sqrt{\frac{\pi \alpha}{q} V_{CH}^2 + \frac{\pi n_{puddle}}{2}} dV \right|} \quad (53)$$

$$I_{DSp} = \mu_p W \frac{\int_0^{V_{DSi}} \left(q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_p \left| \frac{1}{\Omega} \int_0^{V_{DSi}} \sqrt{\frac{\pi n_{puddle}}{2}} dV \right|} \quad (54)$$

Similarly, when $z(x=0)$ and $z(x=L)$ are both negative and the current conduction is dominated by holes (Figure 1.11b), expressions for the electron and hole current contributions can be derived as:

$$I_{DSn} = \mu_n W \frac{\int_0^{V_{DSi}} \left(q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_n \left| \frac{1}{\Omega} \int_0^{V_{DSi}} \sqrt{\frac{\pi n_{puddle}}{2}} dV \right|} \quad (55)$$

$$I_{DSp} = \mu_p W \frac{\int_0^{V_{DSi}} \left(\alpha V_{CH}^2 + q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_p \left| \frac{1}{\Omega} \int_0^{V_{DSi}} \sqrt{\frac{\pi \alpha}{q} V_{CH}^2 + \frac{\pi n_{puddle}}{2}} dV \right|} \quad (56)$$

However, when $z(x = 0)$ and $z(x = L)$ are different in sign, a change in the carrier type takes place at the charge neutrality point ($x = x_0$) within the channel as shown in Figure 1.11c and d. In these cases, the integrals in (50) are separated for two segments of the channel on either side of the charge neutrality point, having opposite polarities.

In the case of Figure 1.11c, when a transition from an n-type channel to a p-type channel exists, the electron and hole contributions are expressed as:

$$I_{DS_n} = \mu_n W \frac{\int_0^{V_0} \left(\alpha V_{CH}^2 + q \cdot \frac{n_{puddle}}{2} \right) dV + \int_{V_0}^{V_{DS_i}} \left(q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_n \left| \frac{1}{\Omega} \left(\int_0^{V_0} \sqrt{\frac{\pi\alpha}{q}} V_{CH}^2 + \frac{\pi n_{puddle}}{2} dV + \int_{V_0}^{V_{DS_i}} \sqrt{\frac{\pi n_{puddle}}{2}} dV \right) \right|} \quad (57)$$

$$I_{DS_p} = \mu_p W \frac{\int_0^{V_0} \left(q \cdot \frac{n_{puddle}}{2} \right) dV + \int_{V_0}^{V_{DS_i}} \left(\alpha V_{CH}^2 + q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_p \left| \frac{1}{\Omega} \left(\int_0^{V_0} \sqrt{\frac{\pi n_{puddle}}{2}} dV + \int_{V_0}^{V_{DS_i}} \sqrt{\frac{\pi\alpha}{q}} V_{CH}^2 + \frac{\pi n_{puddle}}{2} dV \right) \right|} \quad (58)$$

Equivalent expressions for the electron and hole current contributions, when a transition from a p-type channel to an n-type channel occurs, are written as:

$$I_{DS_n} = \mu_n W \frac{\int_0^{V_0} \left(q \cdot \frac{n_{puddle}}{2} \right) dV + \int_{V_0}^{V_{DS_i}} \left(\alpha V_{CH}^2 + q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_n \left| \frac{1}{\Omega} \left(\int_0^{V_0} \sqrt{\frac{\pi n_{puddle}}{2}} dV + \int_{V_0}^{V_{DS_i}} \sqrt{\frac{\pi\alpha}{q}} V_{CH}^2 + \frac{\pi n_{puddle}}{2} dV \right) \right|} \quad (59)$$

$$I_{DS_p} = \mu_p W \frac{\int_0^{V_0} \left(\alpha V_{CH}^2 + q \cdot \frac{n_{puddle}}{2} \right) dV + \int_{V_0}^{V_{DS_i}} \left(q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_p \left| \frac{1}{\Omega} \left(\int_0^{V_0} \sqrt{\frac{\pi\alpha}{q}} V_{CH}^2 + \frac{\pi n_{puddle}}{2} dV + \int_{V_0}^{V_{DS_i}} \sqrt{\frac{\pi n_{puddle}}{2}} dV \right) \right|} \quad (60)$$

where V_0 is the channel voltage at the charge neutrality point (which can be calculated by equating $z(x)$ to zero, thereby yielding to $V_0 = Q_{tot}/C_{eq}$).

To implement the compact model in Verilog-A, analytical solutions for integrals (53)-(60) have been developed and are presented in Appendix A.

b) Gate Capacitances

After some algebraic manipulations (shown in the Appendix A) based on (44)-(46), one can write:

$$C_{GG} = -2\alpha W C_{top} \int_0^L \frac{|V_{CH}|}{2\alpha |V_{CH}| + C_{eq}} dx \quad (61)$$

$$C_{GD} = -2\alpha W C_{eq} \frac{dV}{dV_{DSi}} \int_0^L \frac{|V_{CH}|}{2\alpha|V_{CH}| + C_{eq}} dx \quad (62)$$

$$C_{GS} = 2\alpha W \left(C_{eq} \frac{dV}{dV_{DSi}} - C_{top} \right) \int_0^L \frac{|V_{CH}|}{2\alpha|V_{CH}| + C_{eq}} dx \quad (63)$$

where dV/dV_{DSi} is the rate of change of the potential variation due to V_{DSi} . In this work, this quantity has been considered to be a fitting parameter varying from -1 to 1. A common integral term (referred to as *Int* in the following) in (61)-(63) can be seen and given by:

$$Int = \int_0^L \frac{|V_{CH}|}{2\alpha|V_{CH}| + C_{eq}} dx \quad (64)$$

To calculate this integral, the inverse of the electric-field should be introduced: $E = -dV(x)/dx$ which based on (25) can be written as:

$$\text{if } V_{CH} \geq 0 \text{ and } \frac{dx}{dV} \geq 0 \quad \frac{dx}{dV} = \frac{\mu_n W}{I_{DS}} (Q_n + q \cdot n_{puddle}) - \frac{\mu_n}{v_{sat_n}} \quad (65)$$

$$\text{if } V_{CH} \geq 0 \text{ and } \frac{dx}{dV} < 0 \quad \frac{dx}{dV} = \frac{\mu_n W}{I_{DS}} (Q_n + q \cdot n_{puddle}) + \frac{\mu_n}{v_{sat_n}} \quad (66)$$

$$\text{if } V_{CH} < 0 \text{ and } \frac{dx}{dV} \geq 0 \quad \frac{dx}{dV} = \frac{\mu_p W}{I_{DS}} (Q_p + q \cdot n_{puddle}) - \frac{\mu_p}{v_{sat_p}} \quad (67)$$

$$\text{if } V_{CH} < 0 \text{ and } \frac{dx}{dV} < 0 \quad \frac{dx}{dV} = \frac{\mu_p W}{I_{DS}} (Q_p + q \cdot n_{puddle}) + \frac{\mu_p}{v_{sat_p}} \quad (68)$$

As depicted from (65)-(68), the term dx/dV introduces a mobility-dependence. When the channel is entirely n- or p-type (determined by the sign of V_{CH}), (61)-(63) consider a single channel segment for the integrals as in (53)-(56). Consequently, for example when $V_{CH} \geq 0$, the common integral term, *Int*, while considering unipolar conduction is written as:

$$Int = \int_0^{V_{DSi}} \frac{|V_{CH}|}{2\alpha|V_{CH}| + C_{eq}} \cdot \left[\frac{\mu_{(n,p)} W}{I_{DS}} (Q_{(n,p)} + q \cdot n_{puddle}) - \frac{\mu_{(n,p)}}{v_{sat_{(n,p)}}} \right] dV \quad (69)$$

On the other hand, in case of ambipolar conduction, (61)-(63) consider two segments of the channel having opposite polarities, on either side of a transition point (*i.e.* V_0) where the charge polarity reverses (*e.g.* n-type to p-type) as in (57)-(60). Considering, as an example, the case when a transition from an n-type to a p-type channel occurs and $\frac{dx}{dV} \geq 0$, the integral term *Int* is written as:

$$\begin{aligned}
Int = & \int_0^{V_0} \frac{V_{CH}}{2\alpha V_{CH} + C_{eq}} \cdot \left[\frac{W}{I_{DS}} (Q_n + q \cdot n_{puddle}) - \frac{\mu_n}{v_{sat_n}} \right] dV \\
& + \int_{V_0}^{V_{DS_i}} \frac{-V_{CH}}{-2\alpha V_{CH} + C_{eq}} \cdot \left[\frac{W}{I_{DS}} (Q_p + q \cdot n_{puddle}) - \frac{\mu_p}{v_{sat_p}} \right] dV
\end{aligned} \tag{70}$$

The solutions for the integrals (61)-(63) are also shown in Appendix A.

E) Results & Discussion

In order to validate the compact model described in the previous sections, measurement results from two relevant m-GFET technologies have been compared with the model simulations.

1. Columbia University's Device

The first device [46] consists of exfoliated graphene located on a thick SiO₂ layer (285 nm), grown on a heavily doped silicon wafer which acts as a back-gate. It has a 15 nm HfO₂ top-gate dielectric ($\epsilon_r = 16$). The channel length is 1 μm and the width is 2.1 μm .

Figure 1.17a presents the comparison between the measured transfer characteristics, and the results from simulation of the compact model and the numerical model. A distinct asymmetry of the hole and electron branches can be observed. Additionally, the branch currents calculated from the numerical and the compact models match closely; however, around the Dirac point, a slight difference is noticeable. This difference can be attributed to the usage of a simplified quantum capacitance equation (14) in the compact model implementation whereas for the numerical model the exact solution of (6) is considered. However, taking a closer look, the RMS error of the compact model is found to be 3.5 % whereas for the numerical model it is of 2 %; therefore, from a practical viewpoint, this assumption does not yield a substantial modeling error. Also, when the drain-to-source voltage is increased, a shift in the Dirac voltage towards more negative top-gate voltages is observed. The maximum achieved I_{ON}/I_{OFF} current ratio is ~ 2 which is limited by the gapless nature of graphene. Figure 1.17b shows the transconductance ($g_m = \frac{dI_{DS}}{dV_{GS}}$) of the device, depicting good accuracy between the models even for the second order quantities.

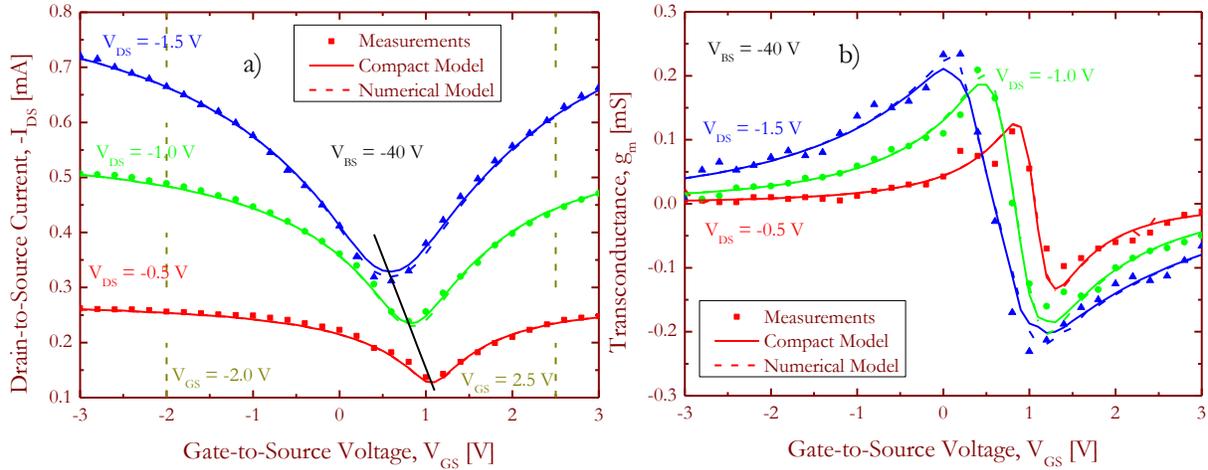


Figure 1.17: Comparison of the measured (symbols) a) transfer characteristic (I_{DS} - V_{GS}) and b) transconductance (g_m - V_{GS}) with the numerical model (dashed lines) and the compact model results (solid lines) for $V_{BS} = -40$ V and $V_{DS} = -0.5$, -1.0 and -1.5 V.

Figure 1.18 shows the variation of the channel voltage, the carrier densities and the saturation velocities along the channel for two different top-gate voltages (indicated as vertical dashed lines in Figure 1.17a). Considering the plots on the left of Figure 1.18 for $V_{GS} = -2$ V and thus in the hole branch of the transfer characteristic: as V_{DS} increases, the channel voltage V_{CH} becomes more negative (as suggested by (19)) and since $Q_{net} \approx Q_p = \alpha V_{CH}^2$, the hole density p is increased (due to an increase in the magnitude of V_{CH}). The saturation velocity, being $\propto \frac{1}{\sqrt{p}}$, decreases when the hole density is increased. Therefore, the drain-to-source current is increased as V_{DS} increases.

Similarly, in the electron branch (on the right of Figure 1.18), when $V_{GS} = 2.5$ V: as V_{DS} is increased, the channel voltage is reduced and thus the electron density n is reduced. Hence, the drain-to-source current increases as V_{DS} increases. As it can be seen from Figure 1.18; not only the absolute channel voltage, but also the variations of the channel voltage (for different V_{DS} voltages) are noticeably higher at the drain side in comparison to the source side. This is owing to the source being grounded and V_{DS} being applied at the drain node.

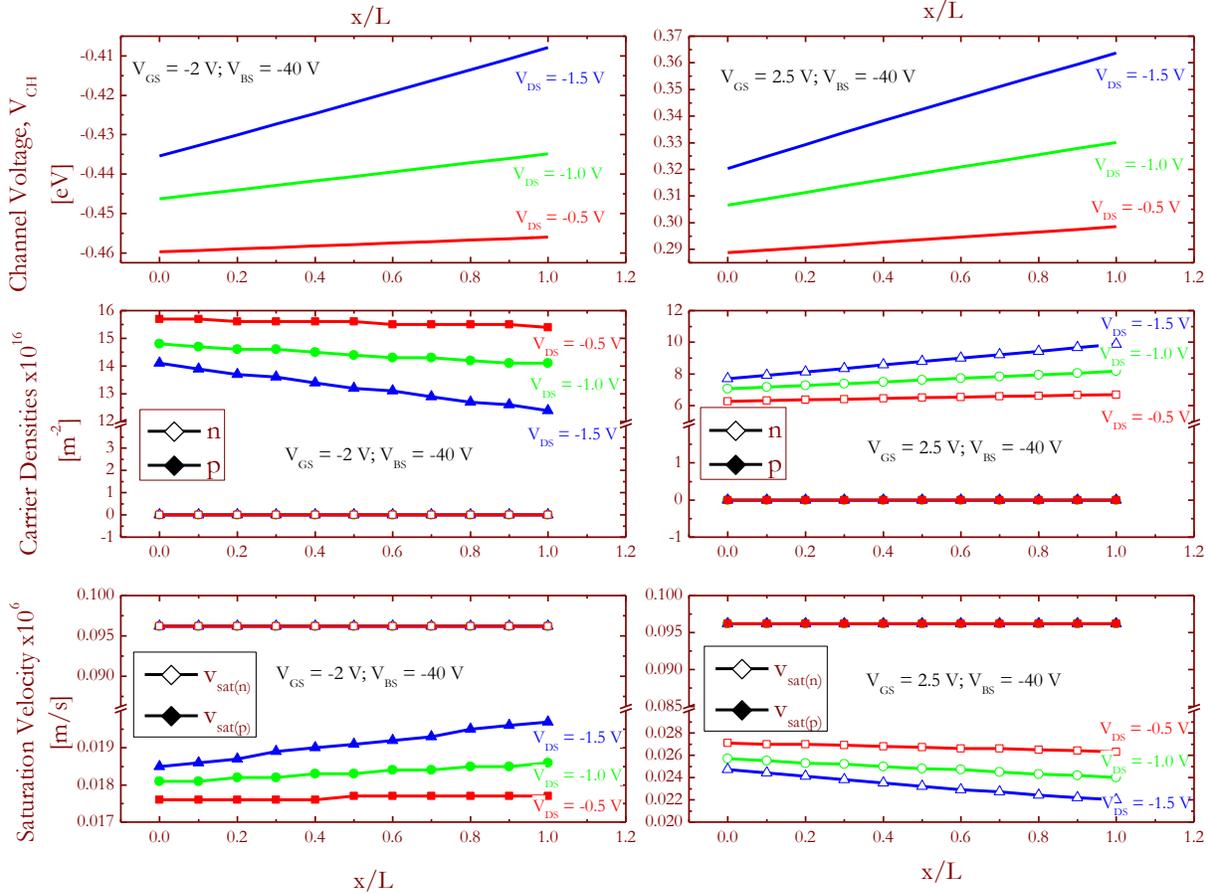


Figure 1.18: Nature of the Channel Voltage, Carrier Densities, Saturation Velocities extracted from the numerical model for $V_{BS} = -40$ V, $V_{DS} = -0.5, -1.0$ and -1.5 V and (left) $V_{GS} = -2$ V and (right) $V_{GS} = 2.5$ V. The carrier density and saturation velocity for electrons are given in hollow symbols and for holes in solid symbols.

On the other hand, Figure 1.19 shows the variation of the channel voltage, the carrier densities and the saturation velocity along the channel under two different values of the back-gate voltage. Considering the plots in the left half of Figure 1.19 for $V_{GS} = -2$ V, the GFET operation is defined by the hole branch of the transfer characteristic: as V_{BS} becomes more negative, the channel voltage subsequently becomes more negative and hence more holes are accumulated in the channel due to the negative back-gate-to-source voltage. Thus, a higher current flows from the source to the drain end owing to the negative drain-to-source voltage.

Likewise, considering the electron branch, (in the right half of Figure 1.19) for $V_{GS} = 2.5$ V: as V_{BS} becomes more negative, the electron density in the channel is reduced due to a decreased channel voltage. Therefore, the absolute value of I_{DS} , (flowing from the source to the drain) decreases.

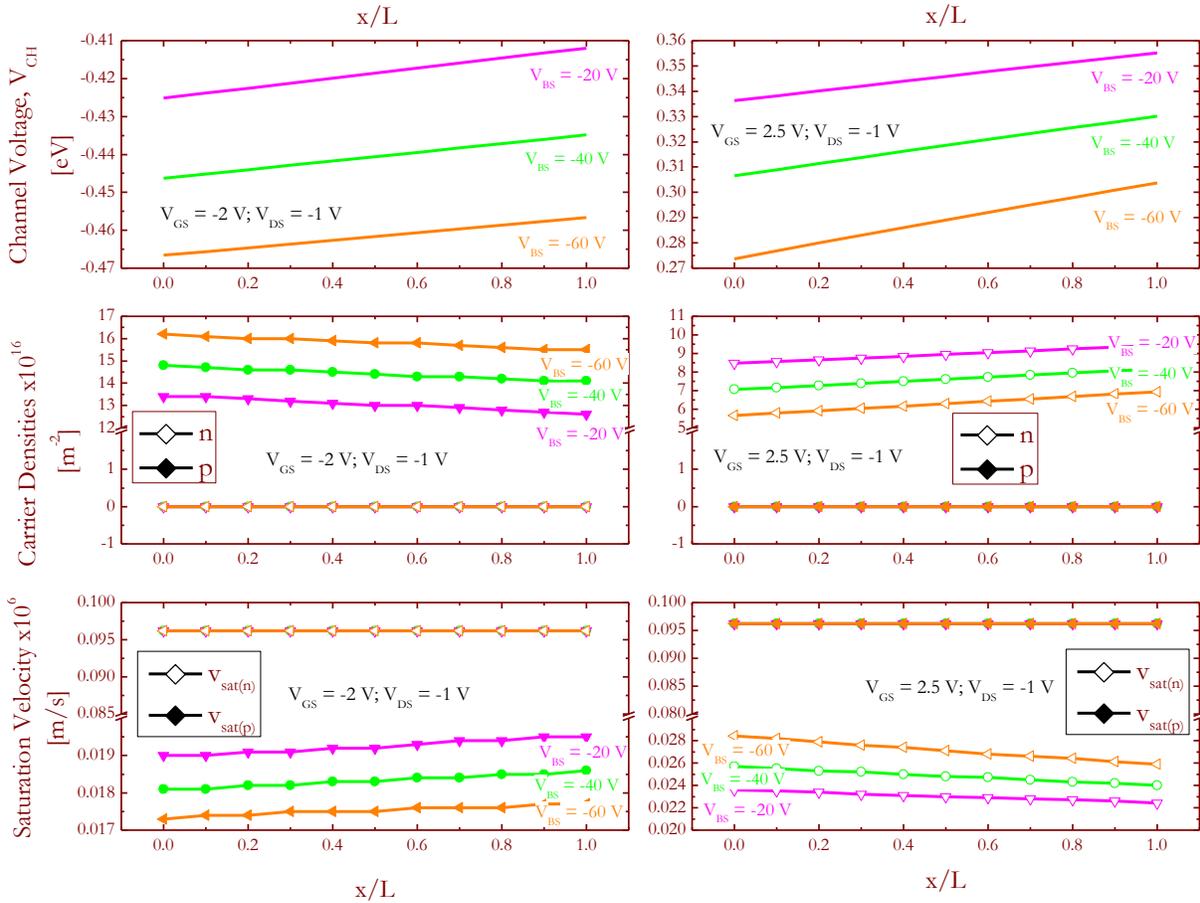


Figure 1.19: Nature of the Channel Voltage, Carrier Densities, Saturation Velocities extracted from the numerical model for $V_{DS} = -1\text{ V}$, $V_{BS} = -20, -40$ and -60 V and (left) $V_{GS} = -2\text{ V}$ and (right) $V_{GS} = 2.5\text{ V}$. The carrier density and saturation velocity for electrons are given in hollow symbols and for holes in solid symbols.

Figure 1.20 illustrates the nature of the channel voltage, the carrier densities and the saturation velocities along the channel at $V_{GS} = V_{Dirac}$ (shown by a solid black line in Figure 1.17a). As observed, the channel voltage is negative at the source end giving rise to the accumulation of holes and depletion of electrons in the channel and it becomes positive at the drain end where electrons are accumulated. Therefore, the channel is ambipolar and a recombination point for electrons and holes exists within the channel, where no energy is released due to the gapless nature of graphene.

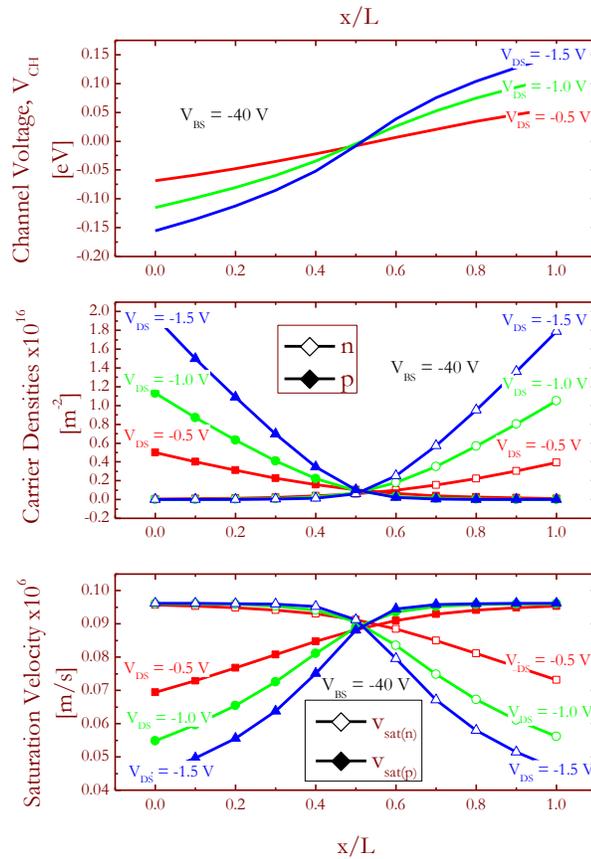


Figure 1.20: Nature of the Channel Voltage, Carrier Densities, Saturation Velocities extracted from the numerical model for $V_{GS} = V_{Dirac}$, $V_{BS} = -40$ V and $V_{DS} = -0.5, -1.0$ and -1.5 V. The carrier density and saturation velocity for electrons are given in hollow symbols and for holes in solid symbols.

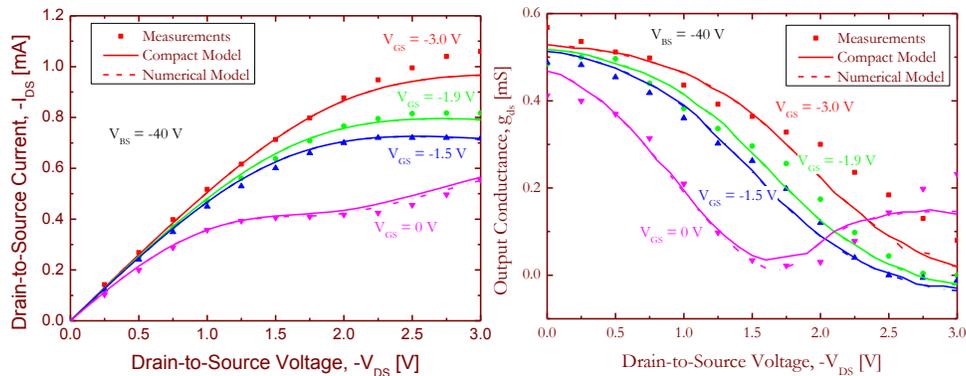


Figure 1.21: Comparison of the measured (symbols) a) output characteristic (I_{DS} - V_{DS}) and b) output conductance (g_{ds} - V_{DS}) with the numerical model (dashed lines) and the compact model results (solid lines) for $V_{BS} = -40$ V and $V_{GS} = 0, -1.5, -1.9$ and -3.0 V.

Figure 1.21a presents a comparison of the measured output characteristics from [46] with the corresponding compact model and the numerical model results. As seen in Figure 1.21a, for $V_{GS} = 0$ V, the drain-to-source current shows a “kink” signifying the presence of an ambipolar channel.

Figure 1.21b shows the output conductance $\left(g_{ds} = \frac{dI_{DS}}{dV_{DS}}\right)$ of the device showing good accuracy between the models and measurements. The maximum intrinsic voltage gain of the device, $A_V = \frac{g_m}{g_{ds}}$, is of around 10 which is still not close enough to the performance requirements of advanced RF devices where an intrinsic voltage gain of $A_V = 30$ is typically targeted [4] for devices with sub-100 nm gate length. The lower gain is due to the poor current saturation observed in monolayer GFET devices due to the absence of an energy bandgap. In addition, as the channel length is scaled down, the intrinsic voltage gain worsens since the velocity saturation due to carrier scattering gets suppressed, preventing current saturation.

Table 2 summarizes the m-GFET dimensions and the other additional parameters used for the modeling. An empirical model described in Section 6 for the parasitic series resistances has been considered for this particular GFET.

Table 2: Dimensions and Parameters of the modeled m-GFET [46]

Dimension/Parameter	Value
L	1 μm
W	2.1 μm
t_{top}	15 nm
t_{back}	285 nm
ϵ_{top}	16 (HfO ₂)
ϵ_{back}	3.9 (SiO ₂)
μ_n	1600 cm ² /V·s
μ_p	1100 cm ² /V·s
Δ	62.5 meV
N_F	-4.7×10^{12} cm ⁻²
$\hbar\Omega$	45 meV
$R_{S_{n0}} = R_{S_{p0}}$	1.7×10^{-3} $\Omega \cdot \text{m}$
$R_{D_{n0}} = R_{D_{p0}}$	2.5×10^{-3} $\Omega \cdot \text{m}$

2. University of Lille's CVD Device

The second device under test has been fabricated with CVD-grown graphene transferred on a Si/SiO₂ substrate [47]. The CVD m-GFET has two back-gate fingers with a coplanar access structure making it suitable for RF measurements. Due to the air exposure, oxidation has led to the growth of an Al₂O₃ layer of ~ 3 nm. The source and the drain ohmic contacts of a Ni/Au alloy were

- The Short Standard corresponds to a short circuit between the signal and the ground
- The Load Standard corresponds to a 50Ω load placed between the signal and the ground
- The Thru Standard corresponds to a transmission line placed between Port 1 and Port 2

Figure 1.23 is a closer view at the SOLT standards.



Figure 1.23: Closer View at the SOLT Standards

b) Electro-Magnetic Simulations

On-wafer SOLT calibration kit's goal is to remove the effect of the wiring and the probes from the RF characteristics of the GFET. However, at high frequencies, the frequency-dependent impedances are still present in the measurement due to the effect of the BEOL (Back-En of Line). Hence, University of Lille provided on-wafer de-embedding structures (Open-Pad, Mute and Short) to assess the influence of these BEOL on the measurements and eventually to remove these parasitic effects.

To evaluate the complete RF behavior of an m-GFET from a simulation point of view, a design kit has been developed, which includes compact model simulation of the m-GFET intrinsic behavior and the electro-magnetic (EM) simulations of the BEOL structures (using Keysight ADS Software).

EM simulations of specific test structures (Open-Pad, Mute and Short) have been carried out to extract the values of the parasitic elements, using the GDS layout of the fabricated CVD m-GFET substrate that utilizes a high quality Si substrate for RF circuits with a resistivity of $5000 \Omega \cdot \text{cm}$. Figure 1.24 illustrates the substrate model used for EM simulations. The MUTE test structure corresponds to an entire m-GFET structure where only the graphene layer is absent.

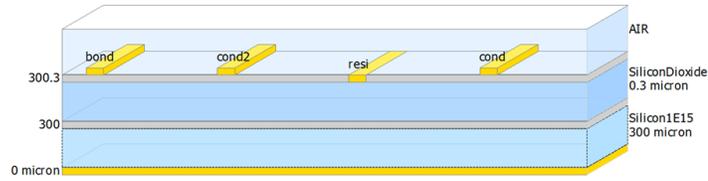


Figure 1.24: Substrate Model and Structure used for EM Simulation

Figure 1.25 shows the EM simulated Open-Pad, Mute and Short test structures. It is to be noticed that the Mute structure shown in Figure 1.25b includes the Pads, thereby to account only for the capacitance contribution of the Mute structure (without the Pad contributions), the following operation on the Y matrix of the two-port GFET network is considered:

$$Y_{mute-deembedded} = Y_{mute} - Y_{Open-Pad} \quad (71)$$

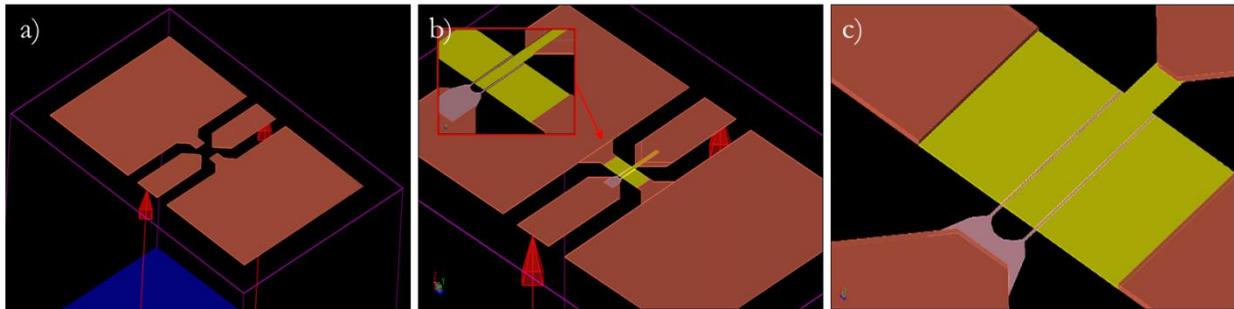


Figure 1.25: a) Open-Pad, b) Mute and c) Short EM test structures

Table 3 compares the extracted values of the parasitic elements from EM simulation and measurements. Here, C_{ij} signifies the parasitic capacitance of a structure between the ports i and j of its two-port network representation.

Table 3: Passive Elements extracted values for the CVD m-GFET

Extracted Value	CVD m-GFET [47]	
	Measurement	Simulation
Open-Pad Structure		
C_{11}	10 fF	10 fF
C_{12}	3 fF	4 fF
C_{22}	8 fF	10 fF
Mute Structure		
C_{11}	10 fF	11 fF
C_{12}	5 fF	6 fF
C_{22}	10 fF	11 fF
Short Structure		
L_G	Structure not available	100 pH
L_D		100 pH

To account for the frequency-dependent impedances at high frequencies due to the BEO, the extracted values from EM simulation have been included in the Keysight ICCAP software as lumped elements in the circuit netlist for simulation of the entire m-GFET structure.

Figure 1.26 shows the large-signal equivalent circuit of the m-GFET under measurement conditions. The capacitances of the Mute structure shown in Figure 1.26 are de-embedded from the Open-Pad capacitances. The equivalent circuit representation of the bias-tees accounting for the measurement environment is also indicated in Figure 1.26.

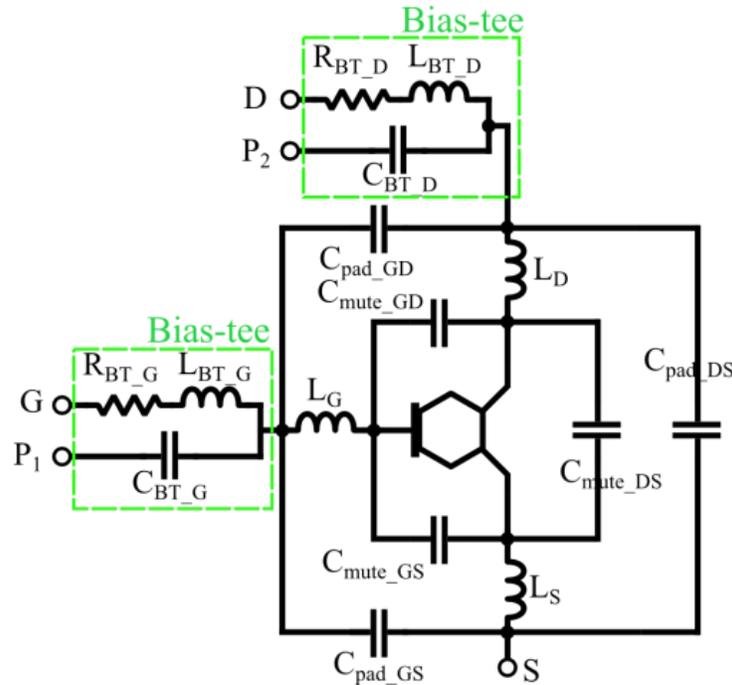


Figure 1.26: Large-Signal equivalent circuit of the m-GFET in measurement conditions.

c) DC and S-Parameter Results

Figure 1.27 and Figure 1.28 show the comparison of the DC measurement characteristics (I_{DS} - V_{GS} , g_m - V_{GS} and I_{DS} - V_{DS}) with the compact model simulation results. A very good agreement is observed in the DC transfer and output characteristics as well as for the transconductance. The maximum achieved I_{ON}/I_{OFF} current ratio of the device is ~ 1.4 .

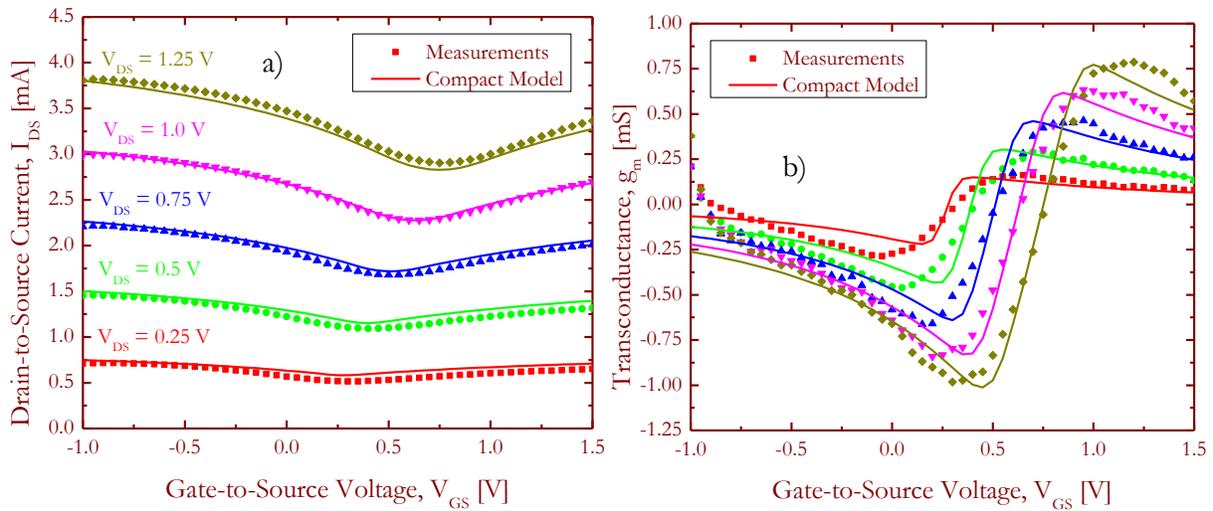


Figure 1.27: Comparison of the measured (symbols) a) transfer characteristic (I_{DS} - V_{GS}) and b) transconductance (g_m - V_{GS}) with the compact model (solid lines) for V_{DS} varying from 0.25 V to 1.25 V in steps of 0.25 V.

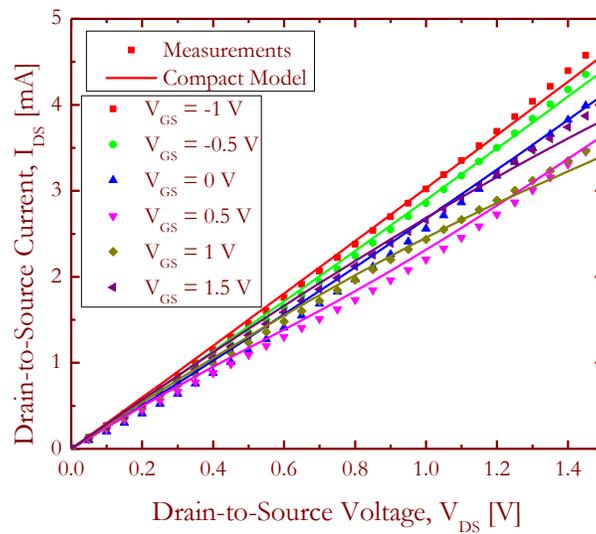


Figure 1.28: Comparison of the measured (symbols) output characteristics (I_{DS} - V_{DS}) with the compact model (solid lines) for V_{GS} varying from -1 V to 1.5 V in steps of 0.5 V.

Figure 1.29 displays a zoom on the curve in Figure 1.27a for $V_{DS} = 1$ V showing a significant improvement in the accuracy by considering the two-mobility model presented in this work over the single mobility model presented in our previous works [78].

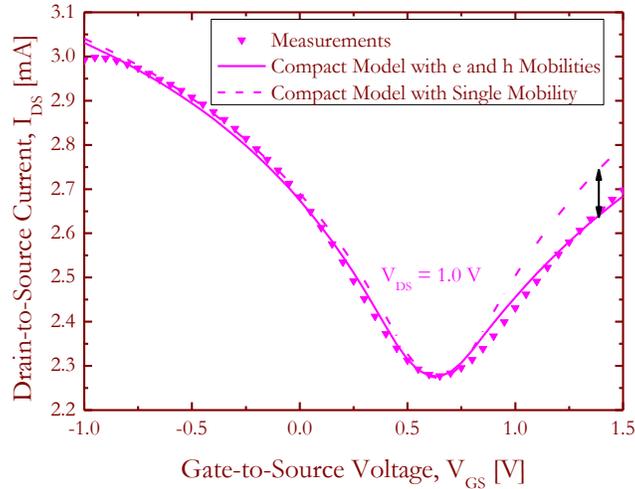


Figure 1.29: Comparison of the compact model presented in this work (solid lines) with the compact model presented in previous works (dashed lines) [78].

To extend the validation of the compact model for RF measurements, the S-Parameter measurements on the CVD m-GFET are compared with the AC simulation of the large-signal m-GFET compact model. Figure 1.30 shows the Smith chart containing the four S-Parameters from both measurement and simulation at two different bias conditions depicting a very good accuracy over a wide frequency range (400 MHz to 40 GHz), thus validating the large-signal model's accuracy in high frequency circuit simulations.

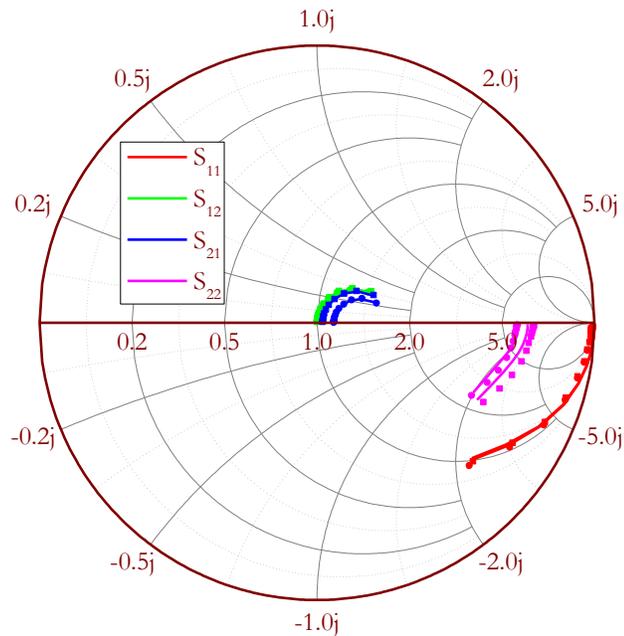


Figure 1.30: Comparison of the S-Parameter measurements (symbols) with the compact model (solid lines) for $V_{GS} = 250$ mV and $V_{DS} = 500$ mV and 1.5 V for a frequency range of 400 MHz to 40 GHz.

Figure 1.31 shows the extracted gate-capacitances, C_{GS} and C_{GD} , and $|Y_{21}|$ as a function of bias ($V_{DS} = 0.5$ V and V_{GS} varying from -1 to 1.5 V) at a fixed frequency value ($freq = 4$ GHz). A fair agreement is observed over the considered bias range. In Figure 1.31a, the presence of a Dirac point can be observed in the gate capacitances, C_{GS} and C_{GD} , which is due to the quantum capacitance C_q of the graphene channel because C_q is very small compared to the top-gate capacitance, C_{top} . Since the top-gate dielectric is very thin, the effect of the quantum capacitance, C_q , can clearly be observed in the gate capacitances, C_{GS} and C_{GD} , thereby resulting in a prominent Dirac point .

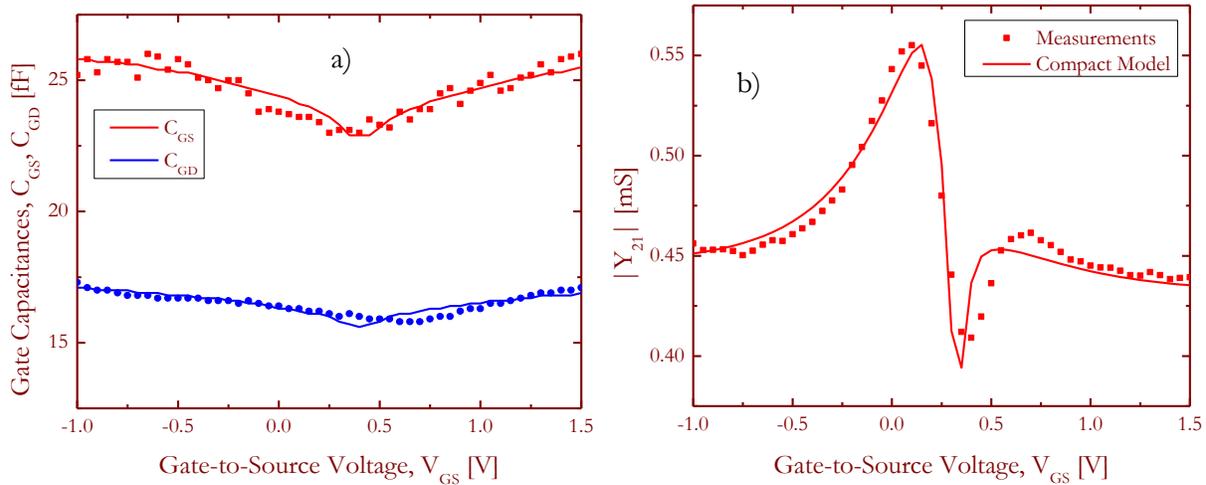


Figure 1.31: Comparison of the extracted a) Gate Capacitances (C_{GS} , C_{GD}) and b) $|Y_{21}|$ from measurements (symbols) as a function of bias (V_{GS} varying from -1 V to 1.5 V and $V_{DS} = 500$ mV) at $freq = 4$ GHz with the compact model (solid lines).

Figure 1.32 shows the cut-off frequency, f_T , as function of the drain-to-source current, I_{DS} for V_{GS} varying from -1 to 1.5 V and $V_{DS} = 500$ mV extracted at $freq = 4$ GHz. The maximum cut-off frequency of the CVD m-GFET (without de-embedding) is observed to be around 2.2 GHz in the hole-branch. The higher f_T in the hole-branch is possibly caused due to a higher mobility of the holes compared to the electrons.

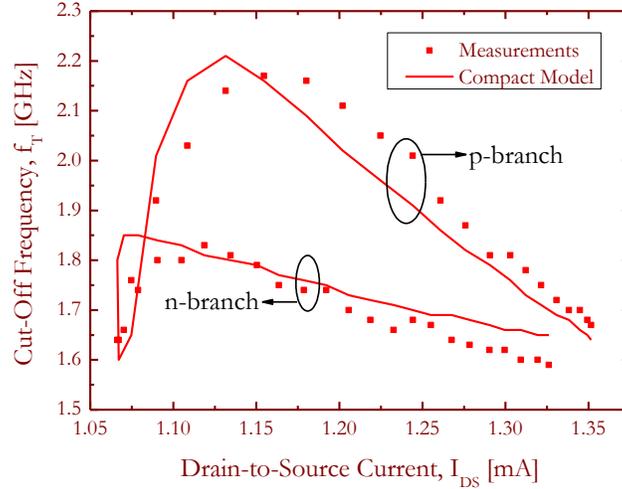


Figure 1.32: Comparison of the extracted cut-off frequency, f_T , from measurements (symbols) as a function of the drain-to-source current at freq = 4 GHz with the compact model (solid lines).

The extracted parameters used for the compact model simulation are listed in Table 4. To model the above mentioned device, the empirical model described in Section 6 for the parasitic series resistances has been considered.

Table 4: Dimensions and Parameters of the modeled m-GFET [47]

Dimension/Parameter	Value
L	300 nm
W	24 μm
t_{top}	3 nm
ϵ_{top}	9.1 (Al_2O_3)
μ_n	320 $\text{cm}^2/\text{V}\cdot\text{s}$
μ_p	430 $\text{cm}^2/\text{V}\cdot\text{s}$
Δ	35 meV
N_F	$-3.3 \times 10^{12} \text{ cm}^{-2}$
$\hbar\Omega$	85 meV
v_F	$0.7 \times 10^6 \text{ m/s}$
R_{sh}	5 Ω/\square
$N_{\mathcal{F}ng}$	2
$R_{S_{n0}} = R_{S_{p0}}$	$3.1 \times 10^{-3} \Omega\cdot\text{m}$
$R_{D_{n0}} = R_{D_{p0}}$	$3.5 \times 10^{-3} \Omega\cdot\text{m}$
dV/dV_{DS_i}	0.325
(R_{BT_G}, R_{BT_D})	3 Ω
(C_{BT_G}, C_{BT_D})	1 F
(L_{BT_G}, L_{BT_D})	100 mH
$(C_{pad_{GS}}, C_{mute_{GS}})$	(10, 1) fF

$(C_{pad_{GD}}, C_{mute_{GD}})$	(4, 2) fF
$(C_{pad_{DS}}, C_{mute_{DS}})$	(10, 1) fF

F) Application- DUT from University of New Mexico [103]

The validity and potential of the model have been corroborated by measurements on a different GFET technology procured through collaboration with the University of New Mexico. Modifications have been considered in order to account for structural differences. In the following, the objectives and salient features of this work are presented.

Over the last years, Graphene (Gr)/Germanium (Ge) has shown a tremendous potential for application in graphene synthesis [104]–[107], analog electronics [108] and infrared (IR) detection [109]. Specifically, germanium is an excellent catalyst for chemical vapor deposition of continuous graphene layers [104], [105] as well as nanoribbon with sub-10 nm width [110]. In addition, single layer graphene transferred on a Ge substrate exhibits remarkably low sheet resistivity [108]. Finally, Graphene/Ge Schottky junctions show photovoltaic characteristics with enhanced sensitivity to IR light [109].

Despite the increasing body of literature on graphene on Ge, the physical and electronic structure of the Gr/Ge interface is still poorly characterized and lateral transport in this material combination is not well-understood. Characterization of top-gate graphene FETs is one route to investigate the lateral transport of graphene on Ge.

For simplicity of implementation, the numerical theoretical model presented in Section E) has been used and modified to compare the transport properties of Gr and Gr/Ge-FETs and to extract the carrier mobilities in the Graphene channels.

1. Device Description [103]

A Germanium layer was transferred from a GOI (Germanium on Insulator) wafer to a 285 nm SiO₂/p⁺Si substrate. After defining mesas, a single layer graphene sheet was transferred to Ge/SiO₂/p⁺Si and SiO₂/p⁺Si. Channel regions and electrodes were defined through standard top-down processing. The highly doped Si substrate and 285 nm thermally grown SiO₂ layers serve as gate electrode and gate dielectric, respectively. Figure 1.33a shows the overall fabrication flow of the Gr/transferred Ge-FETs. Optical micrograph of the processed transistors is shown in Figure 1.33b. Figure 1.33c compares the representative (I_{DS} - V_{GS}) at a constant V_{DS} for the graphene, Gr/transferred Ge and transferred Ge devices.

2. Device Modeling

In order to compare the transport in the GFETs and Gr/Ge-FETs, an accurate electrostatic description is necessary to compute the charges in the graphene layer. For simplicity of implementation at the cost of computation time, the numerical model presented in Section E) has been used. The numerical model is dedicated for the m-GFET structure presented in Figure 1.4.

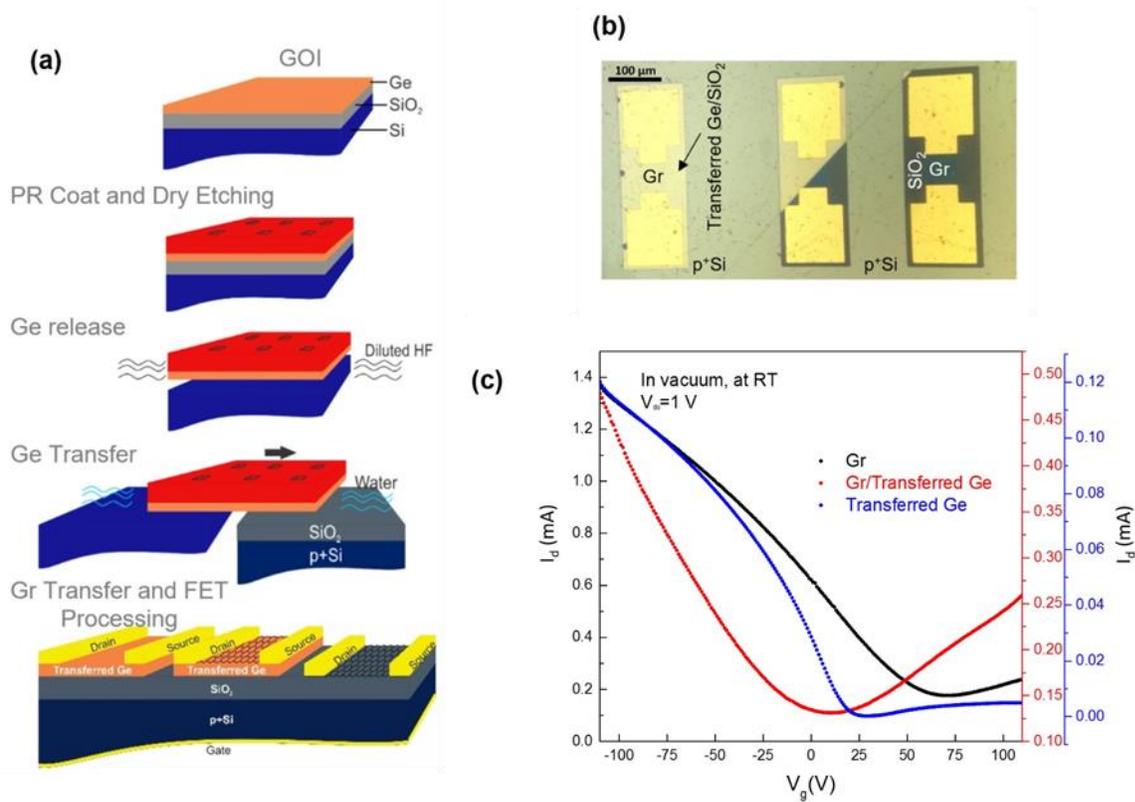


Figure 1.33: a) The overall fabrication route of Gr/transfered Ge FETs. b) Top-view optical micrograph of the fabricated FETs. c) Linear scale (I_{DS} - V_{GS}) recorded at $V_{DS} = 1$ V obtained in vacuum (10^{-6} Torr) and room temperature [103].

First, a finite DOS has been considered for the graphene layer close to the Dirac point due to disorder from quasi-localized defects [111] given by:

$$\rho'_{Gr} = \begin{cases} \frac{g_s g_v}{2\pi(\hbar v_F)^2} |E|, & |E| \geq E_0 \\ \frac{g_s g_v}{2\pi(\hbar v_F)^2} E_0, & |E| < E_0 \end{cases} \quad (72)$$

where E_0 is the energy limit of disorder beyond which the electron DOS starts to dominate over the disorder DOS. Figure 1.34 schematically represents the modified DOS.

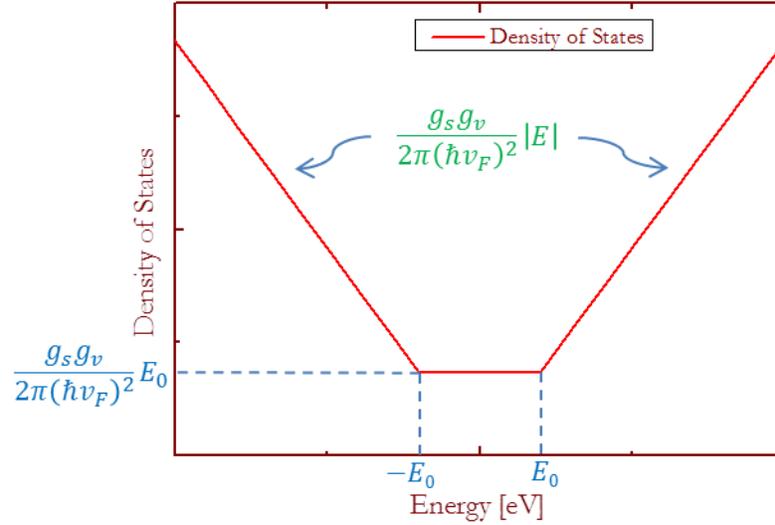


Figure 1.34: Modified DOS considering a finite value close to the Dirac point.

Then, for the Gr/Ge-FET structure, the charge in the Ge layer has to be considered as:

$$Q_{Ge} = C_{GE} \cdot V_{Ge} + \Delta Q_{inv} \quad (73)$$

where C_{Ge} is the capacitance of the Ge insulating layer, V_{Ge} is the voltage drop across the Ge layer and ΔQ_{inv} is the additional charge due to the inversion layer of the metal oxide semiconductor (MOS) stack. Based on the equivalent capacitive circuit presented in Figure 1.10, a simplified equivalent capacitive circuit (without back-gate) is shown in Figure 1.35 including the capacitance of the Ge insulating layer.

Applying Kirchhoff's law to the equivalent capacitive circuit in Figure 1.35, one can write the following equation:

$$Q_{net}(x) + q \cdot N_F = -Q'_{TG}(x) \quad (74)$$

where $Q'_{TG}(x)$ are top-gate induced charges (including the Ge layer) given by:

$$Q'_{TG}(x) = C'_{top} \cdot [V_{GSi} - V(x) - V_{CH}(x)] \quad (75)$$

C'_{top} is the equivalent top-gate capacitance of the top-gate dielectric and the germanium stack given by

$$C'_{top} = \frac{C_{top} \cdot C_{Ge}}{C_{top} + C_{Ge}} \left(1 + \frac{C_{inv}}{C_{Ge}} \right) \quad (76)$$

The total charge in the Ge layer is composed of two terms that correspond to the insulating (C_{Ge}) and the inversion (C_{inv}) layer charges.

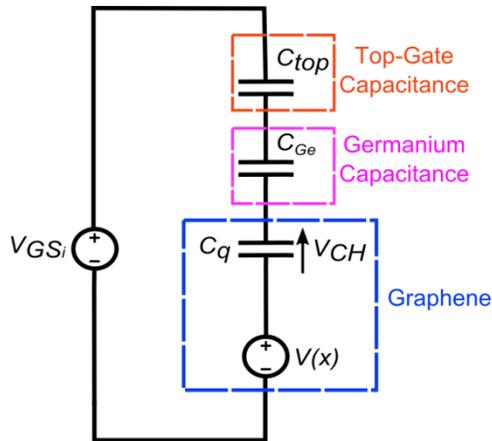


Figure 1.35: Equivalent capacitive circuit for the Gr/Ge-FET structure.

Therefore, to account for this modification in the already existing compact model, the term C_{top} in (19) needs to be replaced by C_{top}' given by (76).

Sentaurus TCAD simulator has been used to extract the carrier density in the Ge inversion layer, which is later used to calculate the channel voltage in Gr/Ge-FET. For this, a calibration procedure has been considered by defining the Schottky barrier heights for the drain and source contacts in addition to the adjustment of the Germanium doping and the mobility of carriers in the inversion layer. From the simulation results, the charge in the inversion layer can be extracted. A linear approximation (Figure 1.36) of the charge is sufficient to evaluate the charge in the Germanium layer, thus yielding $C_{inv} = 135 \mu F/m^2$.

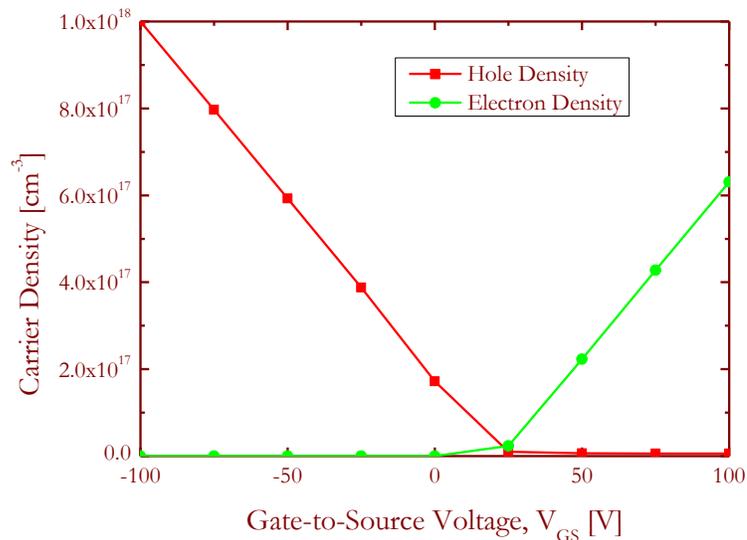


Figure 1.36: Carrier density (electron and hole) in the Ge region of the Ge-FET.

Using the technological parameters (FET dimensions) and the extracted value for C_{inv} , one can extract the average channel voltage as a function of V_{GS} from the numerical model as shown in Figure 1.37.

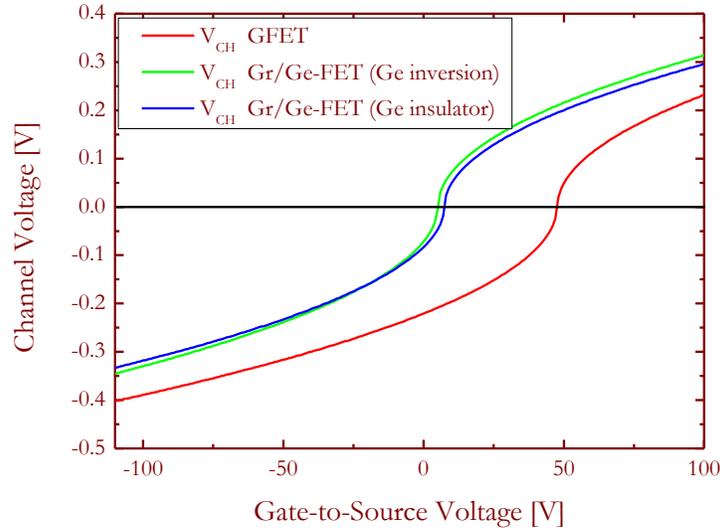


Figure 1.37: Channel Voltage in the graphene layer versus the Gate-to-Source Voltage. The Gr/Ge-FET structure has been simulated with (green line) and without (blue line) considering the inversion charge, C_{inv} .

It can be discerned from Figure 1.37 that the modulation of V_{CH} in Gr/Ge-FET is of the same order of magnitude as the modulation of V_{CH} in the GFET despite the presence of the Ge layer, due to comparable equivalent-oxide-thicknesses in the two structures ($EOT = 285$ nm for the GFET and $EOT = 309$ for the Gr/Ge-FET). Considering the inversion layer, only a small increase in the V_{CH} modulation is observed. By fitting the numerical model simulation to the experimental data of the FET transfer characteristics (Figure 1.38), the carrier mobilities have been extracted.

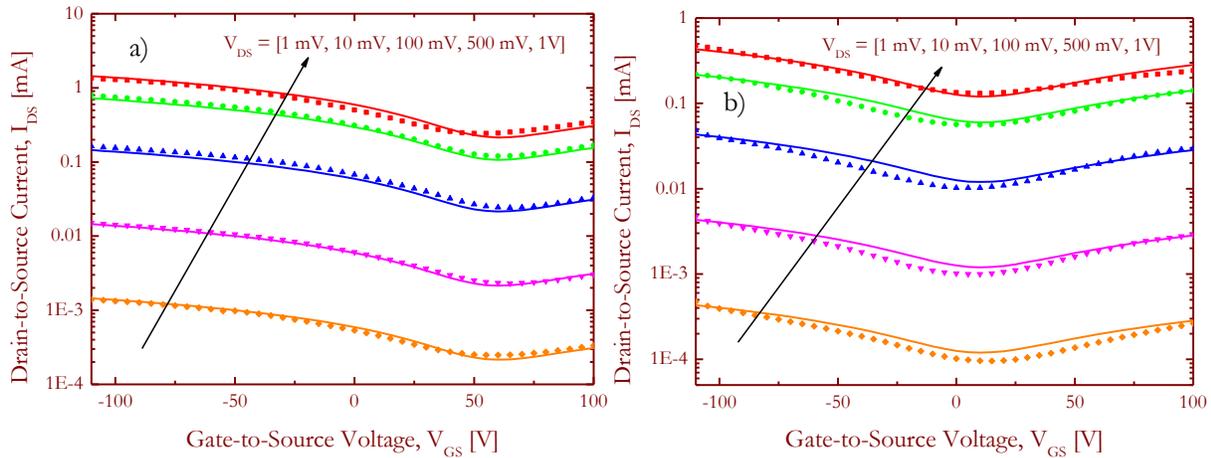


Figure 1.38: Transfer Characteristics for the a) GFET and b) Gr/Ge-FET for different $V_{DS} = 1$ mV, 10 mV, 100 mV, 0.5 V and 1 V. Measurement (symbols) and model (solid lines).

For the GFET, the electron and hole mobilities were found to be 297 $\text{cm}^2/\text{V}\cdot\text{s}$ and 803 $\text{cm}^2/\text{V}\cdot\text{s}$, respectively. For the Gr/Ge-FET, assuming an inversion layer, the electron and hole mobilities were found to be 240 $\text{cm}^2/\text{V}\cdot\text{s}$ and 340 $\text{cm}^2/\text{V}\cdot\text{s}$, respectively. Table 5 recapitulates the

parameters used for the GFET and Gr/Ge-FET modeling. The general observation is that the Gr/Ge-FETs have a balanced electron and hole mobilities compared to the GFET where the carrier mobilities are much more asymmetric. In fact, the surface quality of the transferred Germanium could be responsible of the lower carrier mobilities in the Gr/Ge-FET. Besides, the Dirac point of the Gr/Ge-FETs is adjusted to near zero making them advantageous for low-power applications over the GFETs.

Table 5: Set of modeling parameters for the GFET and Gr/Ge-FET

Dimension/Parameter	GFET	Gr/Ge-FET
L	60 μm	60 μm
W	60 μm	60 μm
t_{top}	285 nm	285 nm
ϵ_{top}	3.9 (SiO ₂)	3.9 (SiO ₂)
t_{Ge}	-	100 nm
ϵ_{Ge}	-	15.8 (Ge)
μ_n	297 cm ² /V·s	240 cm ² /V·s
μ_p	803 cm ² /V·s	340 cm ² /V·s
Δ	120 meV	120 meV
N_F	-3.8×10^{12} cm ⁻²	-3.8×10^{12} cm ⁻²
$\hbar\Omega$	50 meV	50 meV
$R_{S_{n0}} = R_{S_{p0}}$	3×10^{-3} $\Omega\cdot\text{m}$	3×10^{-3} $\Omega\cdot\text{m}$
$R_{D_{n0}} = R_{D_{p0}}$	3×10^{-3} $\Omega\cdot\text{m}$	3×10^{-3} $\Omega\cdot\text{m}$
E_0	0.2 eV	0.2 eV
C_{inv}	-	135 $\mu\text{F}/\text{m}^2$

G) Conclusion

In this chapter, a brief introduction to the physics of graphene followed by the state of the art of developed models for m-GFET has been presented. Then, the physical large-signal compact model developed for dual-gate m-GFETs based on the 2-D DOS of monolayer graphene has been presented by describing in detail each of the different model components. The proposed model considers both ambipolar and unipolar regimes by including a separate branch currents from the electron and hole contributions to the total drain-to-source current, thus achieving a better description of the asymmetric transport behavior and hence increasing the accuracy of the model. Analytical expression of the model equations have been derived and implemented in Verilog-A to ensure model compatibility with standard circuit simulators. The developed model has been demonstrated to be both comprehensive and accurate and it has been extensively validated through

comparison with DC and RF measurements from a long-channel m-GFET technology over an extended frequency range and bias conditions. The values of the parasitic elements extracted from electromagnetic simulation of dedicated test structures have been added to the compact model for improved AC simulation capabilities. Thus, the model presents an accurate assessment of both intrinsic and extrinsic electrical behavior of m-GFETs at high frequency range of operation, rendering it optimal for RF circuit design. Finally, the study of a third GFET has been presented in order to assess the versatility and applicability of the model under modification of the GFET structure.

Chapter 2

BILAYER GFET COMPACT MODEL

Over the last few years, graphene has been receiving a lot of attention as a possible complementary solution to overcome the limitations of present day technologies towards future high performance applications. However, despite its very promising properties, large-area graphene presents a semi-metal behavior posing a critical drawback for digital applications due to the absence of an energy bandgap. To address this shortcoming, researchers have come up with different alternatives, two widely popular solutions being bilayer graphene and graphene Nanoribbons (GNRs), in order to induce an energy band-gap through structural maneuvering. In this chapter, we have focused on bilayer graphene transistors, and especially Bernal stacked bilayer graphene which has been demonstrated as a possible solution to open an energy bandgap. First, a brief introduction to the physics of bilayer graphene will be presented. Then, the compact model developed for bilayer graphene Field-Effect Transistors (b-GFETs) will be illustrated. Next, the accuracy of the model will be validated through comparison to measurements obtained from literature. Finally, the potential of the b-GFET model will be tested through comparison of model simulation and measurement results from an artificially stacked bilayer GFET technology obtained through collaboration with the University of Siegen.

A) Opening an Energy Bandgap

Different approaches to open an energy bandgap in graphene have been proposed [112]. In Graphene Nanoribbons (GNRs) large-area graphene is confined into a quasi-one-dimensional system creating an energy bandgap dependence on the GNR width and its crystallographic orientation (Figure 2.1). However, GNRs present a severe technological challenge from the aspect of

lithographic processes as very narrow and smooth edges are required in order to obtain a steady and high enough energy bandgap. Theoretical studies have shown the possibility of achieving energy bandgaps in the range of 0.5 eV for GNRs, for a nanoribbon width of 2.4 nm [113]. However, experimentally, energy bandgaps up to ~ 200 meV have been reported for GNRs as narrow as ~ 15 nm [114].

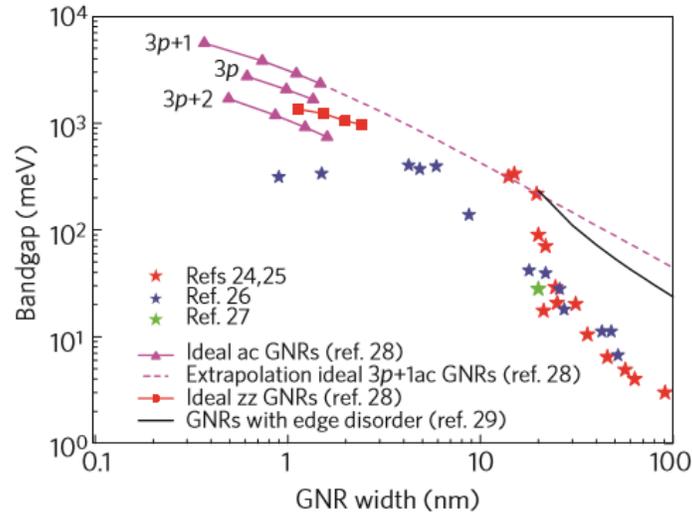


Figure 2.1: Energy bandgap versus GNR width [115]

A second way to open an energy bandgap would be to apply strain on the graphene layer. Raman spectrum studies of strained graphene have shown that a tunable energy bandgap of ~ 300 meV that can be achieved by applying a 1% uniaxial strain (Figure 2.2) [116].

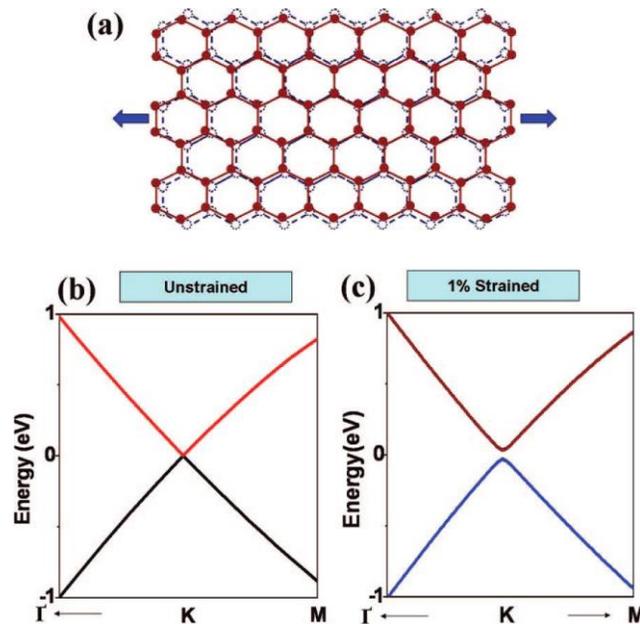


Figure 2.2: a) Schematic representation of the effect of uniaxial tensile stress on graphene. Energy band structure of a) unstrained graphene and b) 1% tensile strained graphene [116].

A third alternative is to apply a vertical electric field to bilayer graphene. Among these three techniques, the latter is the most promising and most feasible from a technological point of view and thus the focus of this work. In recent years, GFETs which utilize Bernal stacked bilayer graphene (where half of an atom lies directly over the center of a hexagon in the lower graphene sheet whereas the other half of the atom lies over another atom, see Figure 2.3) as channel material have been reported to exhibit saturation in the output characteristics [117]–[121]. This is because, in presence of external vertical electric fields, a small tunable energy bandgap of the order of a few hundreds of meV opens up in Bernal stacked bilayer graphene [119]–[121]. This causes the corresponding output characteristics to saturate because of the lowering of the off-state current for the bilayer GFETs compared to the monolayer GFETs.

1. Energy Band Structure of Bilayer graphene

Similar to large-area graphene, bilayer graphene, having a lattice structure of two graphene layers arranged in an A2-B1 Bernal stacking (Figure 2.3), has a gapless band structure in unbiased conditions. However, it has been demonstrated that, by applying a vertical electric field perpendicular to the graphene layer, bilayer graphene exhibits a tunable energy bandgap. The energy bandgap in A2-B1 Bernal stacked bilayer graphene arises from the forming of pseudospins between the layers, thus making it possible to electrically induce an energy bandgap [122]. For sufficiently high perpendicular electric fields, energy bandgaps of ~ 200 meV can be achieved [119], [123].

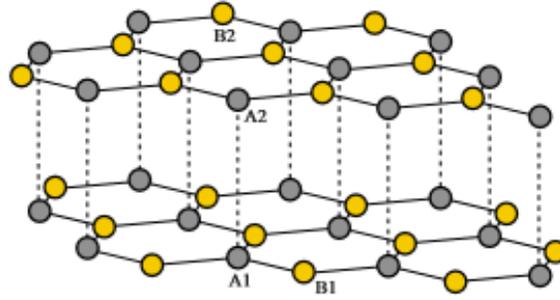


Figure 2.3: Schematic of the A2-B1 Bernal stacked bilayer lattice [124]

As the name suggests, bilayer graphene has two graphene layers, but the electronic band structure is quite different from single layer graphene. Considering a tight binding Hamiltonian for electrons in bilayer graphene, the band energies of bilayer graphene can be written as [124]:

$$E_{\pm}(\mathbf{k}) = \pm \frac{U_1 + U_2}{2} \cdot \sqrt{|f(\mathbf{k})|^2 + \frac{U^2}{4} + \frac{t_{\perp}^2}{2} \pm \frac{1}{2} \sqrt{4(U^2 + t_{\perp}^2)|f(\mathbf{k})|^2 + t_{\perp}^4}} \quad (77)$$

where U_1 and U_2 are the potential energies of the first and second graphene layers, respectively, $U = U_1 - U_2$, t_{\perp} is the interlayer hopping parameter, $\mathbf{k} = k_x \widehat{\mathbf{k}}_x + k_y \widehat{\mathbf{k}}_y$ is the wave vector and $f(\mathbf{k})$ is given by:

$$f(\mathbf{k}) = t \cdot \exp\left(ik_x \frac{a}{2}\right) \left[2 \cos\left(\frac{k_y a \sqrt{3}}{2}\right) + \exp\left(-3ik_x \frac{a}{2}\right) \right] \quad (78)$$

Here, t is the in-plane hopping parameter and a is the distance between two carbon atoms. Figure 2.4 shows the energy band structure of large-area graphene, GNR, and unbiased and biased bilayer graphene. When bilayer graphene is subjected to a vertical electric-field, an energy bandgap opens and the energy bands take on the so-called Mexican-hat shape.

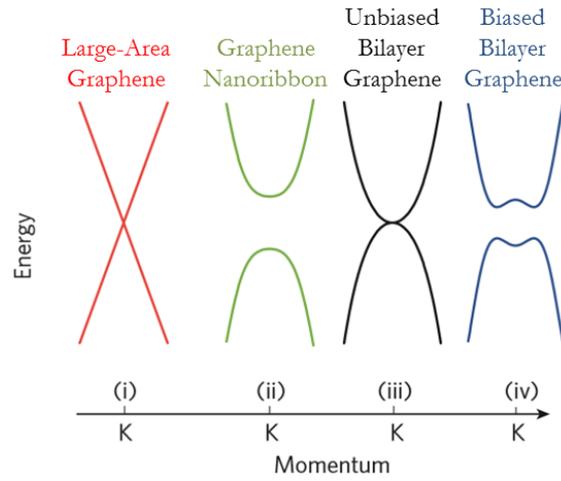


Figure 2.4: Energy band structure around the first Brillouin zone of large area-graphene, GNR, unbiased and biased bilayer graphene [115].

2. Density of States of Bilayer Graphene

The 2-D Density of States (DOS) of bilayer graphene considers the absence of any available occupational states inside the energy bandgap and a constant value outside the bandgap, unlike monolayer graphene, where the DOS is proportional to the Fermi level, E_F . Hence, the 2-D DOS for bilayer graphene can be written as [96]:

$$\rho_{Bi-Gr}(E) = \frac{2m_{eff}}{\pi\hbar^2} \left[H\left(E - \frac{E_g}{2}\right) + H\left(E + \frac{E_g}{2}\right) \right] \quad (79)$$

where m_{eff} is the effective mass, H is the Heaviside step function and E_g is the energy bandgap. Figure 2.5 shows schematically the DOS of biased bilayer graphene.

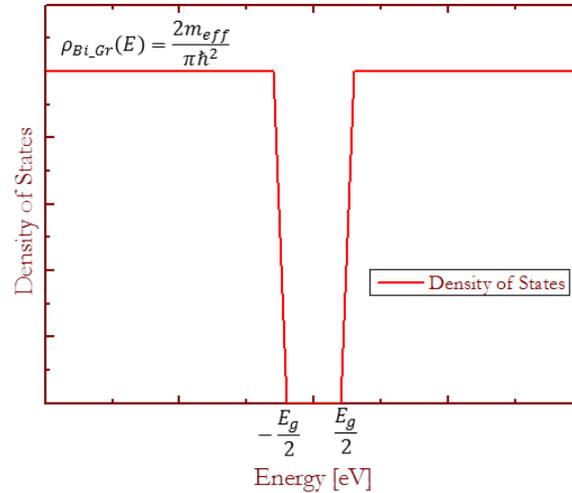


Figure 2.5: Schematic representation of the DOS of biased bilayer graphene.

B) State of the Art

Till now, only a few models for bilayer GFETs (b-GFETs) have been proposed. To name a few, a semi-analytical model based on the effective mass approximation and ballistic transport for b-GFETs has been proposed by Cheli *et al.* [125]. Ryzhii *et al.* [126] proposed an analytical model incorporating both ballistic and collision-dominated electron transport. Electrical compact models for b-GFETs have been reported by Umoh *et al.* [80] and Henry *et al.* [75] (detailed description in Figure 1.8 and Table 1).

C) An Accurate Physics-Based Compact Model for Dual-Gate Bilayer Graphene FETs (This Work) [127], [128]

In this work, an accurate and physics-based large-signal compact model of b-GFETs has been proposed and implemented in Verilog-A for circuit-level simulation. In contrast to the approach presented in [80], a more physically reliable solution has been presented by considering a single quantum capacitance for the bilayer graphene that captures the physics of bilayer graphene with an improved accuracy and the model has been validated for a wide range of bias conditions to fully assess its capabilities.

The developed compact model is based on a dual-gate FET structure using a bilayer graphene film as channel material. The bilayer graphene film is located between a top and a back gate-dielectric as shown in the schematic in Figure 2.6. The source and drain ohmic contacts as well as the top-gate stack are located on top of the bilayer graphene channel. The back-gate stack is

composed of a dielectric and a substrate acting as its back-gate. In this structure, the access resistances of the BGFET are modulated by the back-gate through electrostatic doping.

In the next subsections, the different attributes of the model are described in detail.

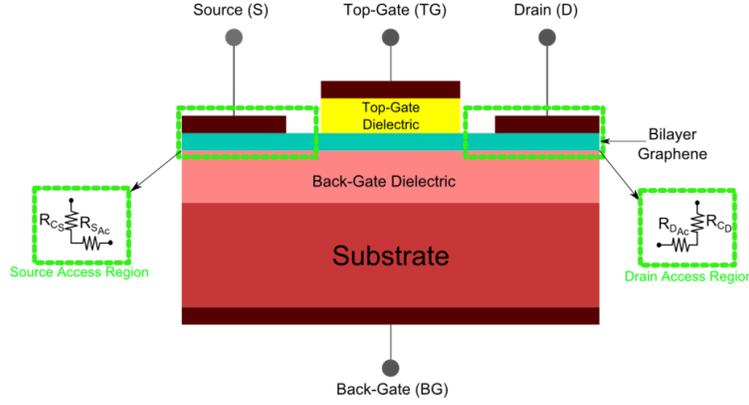


Figure 2.6: Cross sectional view of the b-GFET structure including parasitic access resistances

1. The Energy Bandgap

Under the effect of the applied top-gate and back-gate biases, an average vertical displacement field, D_{AV} , creates the opening of a tunable energy bandgap, E_g . An empirical relation has been used to describe a linear dependence of the energy bandgap as a function of the average displacement electric field. This simplified relation reasonably fits the self-consistent tight binding model calculations presented in [120] (refer to Figure 2.7) and yet preserves reasonable accuracy in the model calculations. Thus, the energy bandgap is given by:

$$E_g = \kappa \cdot D_{AV} \quad (80)$$

where κ is a model parameter whose value has been set as 8.74×10^{-11} eV·m/V.

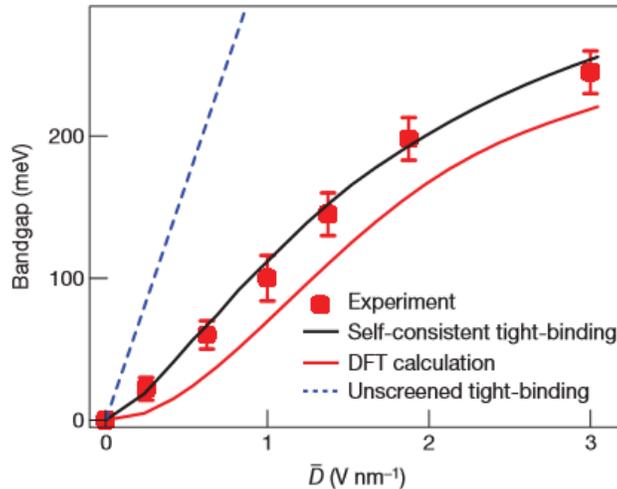


Figure 2.7: Electric-field dependence of tunable energy bandgap in graphene bilayer [120]

The average vertical displacement field is given by:

$$D_{AV} = \frac{D_t + D_b}{2} \quad (81)$$

where D_t and D_b are the top-gate and back-gate vertical displacement fields, respectively, given by:

$$D_t = -\frac{\varepsilon_{top} \cdot (V_{GS_i} - V_{tg_0})}{t_{top}} \quad (82)$$

$$D_b = \frac{\varepsilon_{back} \cdot (V_{BS_i} - V_{bg_0})}{t_{back}} \quad (83)$$

V_{tg_0} and V_{bg_0} are the offset voltages of the Dirac point due to initial environment carrier doping.

2. The Carrier Densities

In order to derive expressions for the carrier sheet densities as a function of the applied top-gate and back-gate voltages, a Fermi-Dirac distribution of carriers has been considered in the channel. Regarding the mid bandgap as the energy reference, the hole and electron sheet densities are written as:

$$n = \int_0^{+\infty} \rho_{Bi-Gr} \cdot f_{FD}(E) dE = \frac{2m_{eff}}{\pi\hbar^2} \left[E - k_B T \ln \left(1 + \exp \left(\frac{E - E_F}{k_B T} \right) \right) \right]_{E_g/2}^{+\infty} \quad (84)$$

$$p = \int_{-\infty}^0 \rho_{Bi-Gr} \cdot [1 - f_{FD}(E)] dE = \frac{2m_{eff}}{\pi\hbar^2} \left[E - k_B T \ln \left(1 + \exp \left(\frac{E + E_F}{k_B T} \right) \right) \right]_{E_g/2}^{+\infty} \quad (85)$$

where f_{FD} is the Fermi-Dirac distribution. Here, the effective mass is considered to be $m_{eff} = A \cdot m_e$, where m_e is the electron mass and A is a fitting parameter. The Fermi energy level along the channel is considered to be proportional to the voltage drop across the quantum capacitance, C_q . The net carrier sheet density, Q_{net} , stored in the quantum capacitance can be written as follow:

$$Q_{net} = q \cdot (p - n) = Q_p - Q_n \quad (86)$$

Under the assumption that $q \cdot V_{CH} \gg k_B T$, based on (84) and (85), the net carrier sheet density can be approximated and written as:

$$Q_{net}(x) \approx \begin{cases} \frac{2qm_{eff}}{\pi\hbar^2} \left[-q \cdot V_{CH}(x) + \text{sign}(V_{CH}) \cdot \frac{E_g}{2} \right], & q \cdot |V_{CH}| \geq \frac{E_g}{2} \\ 0, & q \cdot |V_{CH}| < \frac{E_g}{2} \end{cases} \quad (87)$$

Thus, the quantum capacitance, defined as the derivative of the net carrier density with respect to the voltage along the channel, V_{CH} , is given by:

$$C_q = -\frac{dQ_{net}(x)}{dV_{CH}} = \begin{cases} \frac{2q^2 m_{eff}}{\pi \hbar^2}, & q \cdot |V_{CH}| \geq \frac{E_g}{2} \\ 0, & q \cdot |V_{CH}| < \frac{E_g}{2} \end{cases} \quad (88)$$

Figure 2.8 shows a typical representation of the variation of net carrier sheet density as a function of the channel voltage for different energy bandgap values. As observed, when the energy bandgap is zero, the net carrier density is linear. However, when an energy bandgap is opened, the net carrier density is zero inside the energy bandgap and scales linearly with V_{CH} , for high channel voltages.

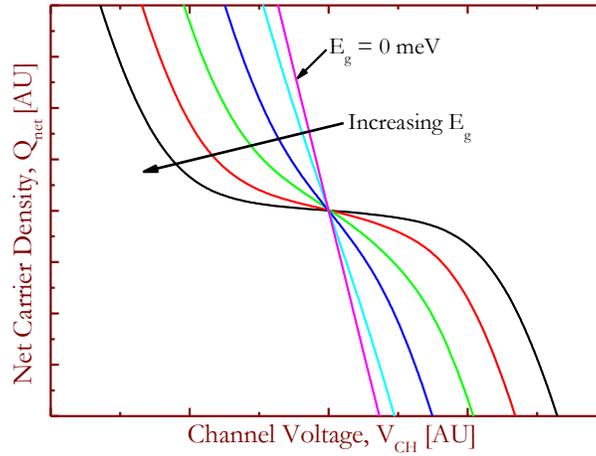


Figure 2.8: Illustration of the Net Carrier Sheet density as a function of the Channel Voltage for different energy bandgap values.

3. The Channel Voltage

The achievable energy bandgaps being small, ambipolar conduction in b-GFET devices still remains a possibility. Under the effect of a set of bias voltages, (V_{GS}, V_{DS}, V_{BS}) , a channel voltage, V_{CH} , along the channel is produced causing a variation in the Fermi level. The bilayer graphene channel is defined to be n-type if the Fermi level all along the channel is closer to the conduction band minimum, E_C , which is mathematically equivalent to $q \cdot V_{CH} \geq E_g/2$. Similarly, the channel is defined to be p-type if the Fermi level is close to the valence band maximum, E_V , which is mathematically equivalent to $q \cdot V_{CH} \leq -E_g/2$. Ambipolar conduction is observed when a transition between these two states occurs at some bias inside the graphene channel.

An equivalent capacitive circuit based on the vertical cross section of the b-GFET structure presented in Figure 2.6 is shown in Figure 2.9.

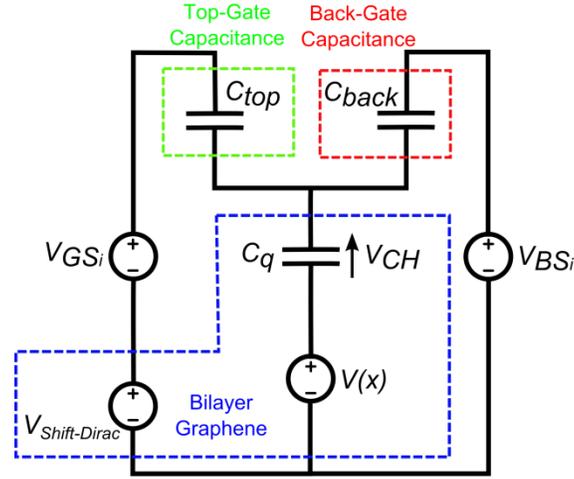


Figure 2.9: Equivalent capacitive circuit of the b-GFET structure

C_{top} and C_{back} are top- and back-gate capacitances, respectively and V_{GS_i} and V_{BS_i} are the top- and back-gate voltages, respectively. To account for the shift in the Dirac point due to the applied back-gate bias, V_{BS} , the voltage source $V_{Shift-Dirac}$ is introduced, which is analogous to the shift of the threshold voltage under the effect of the back-gate bias in conventional MOSFETs. $V(x)$ is the voltage drop along the graphene channel due to the intrinsic drain-to-source voltage, V_{DS_i} at a position x .

Based on the equivalent capacitive circuit in Figure 2.9, the following Kirchhoff's relation can be written:

$$Q_{net}(x) + q \cdot N_F = -(Q_{TG}(x) + Q_{BG}(x)) \quad (89)$$

where Q_{TG} and Q_{BG} are the induced charges due to the top- and back-gate, respectively. N_F accounts for the initial doping of the bilayer graphene channel. Q_{TG} and Q_{BG} are written as:

$$Q_{TG}(x) = C_{top} \cdot [V_{GS_i} - V(x) - V_{CH}(x) + V_{Shift-Dirac}] \quad (90)$$

$$Q_{BG}(x) = C_{back} \cdot [V_{BS_i} - V(x) - V_{CH}(x)] \quad (91)$$

When electrons are the majority carriers in the graphene channel and thus $Q_{net} \approx -Q_n$, combining equations (87)-(91), the channel voltage can be written as:

$$q \cdot V_{CH} \geq \frac{E_g}{2} \Rightarrow V_{CH} = \frac{Q_{tot} - C_{eq} \cdot V(x) + \frac{C_q E_g}{2q}}{C_{eq} + C_q} \quad (92)$$

Equivalently, when the holes are the majority carriers in the channel ($Q_{net} \approx Q_p$), the channel voltage, V_{CH} , is written as follows:

$$q \cdot V_{CH} \leq -\frac{E_g}{2} \Rightarrow V_{CH} = \frac{Q_{tot} - C_{eq} \cdot V(x) - \frac{C_q E_g}{2q}}{C_{eq} + C_q} \quad (93)$$

with $C_{eq} = C_{top} + C_{back}$, $Q_{tot} = Q_{top} + Q_{back} + Q_F + Q_{Shift-Dirac}$, $Q_{top} = C_{top} V_{GS_i}$, $Q_{back} = C_{back} V_{BS_i}$, $Q_F = qN_F$ and $Q_{Shift-Dirac} = C_{top} V_{Shift-Dirac}$.

Inside the energy bandgap, i.e. $-E_g/2 < q \cdot V_{CH} < E_g/2$, no charges are induced by the channel potential and thus it can be written as:

$$q \cdot |V_{CH}| \leq \frac{E_g}{2} \Rightarrow V_{CH} = \frac{Q_{tot} - C_{eq} \cdot V(x)}{C_{eq}} \quad (94)$$

4. The Shift in the Dirac Voltage

As the back-gate voltage, V_{BS} , becomes more negative, more positive charges are induced close to the back-gate thereby inducing more negative charges close to the graphene channel on the top side of the back-gate dielectric. Thus, higher values of V_{GS} are required to obtain the channel charge inversion, resulting in a shift in the Dirac point, $V_{Shift-Dirac}$, towards the positive direction. Similarly, when the back-gate voltage becomes more positive, more positive charges are induced close to the graphene channel on the top side of the back-gate dielectric. As a result a higher negative top-gate voltage is needed to obtain charge neutrality in the channel. Thereby, in this case the shift in the Dirac voltage, $V_{Shift-Dirac}$, will be towards the negative direction. In both cases, the induced charge in the graphene channel will saturate eventually (the total induced charge will be high enough to repel further accumulation of similar charges eventually maintain a steady state value) as the magnitude of the V_{BS} keeps on increasing. Thus, the shift in the Dirac voltage will saturate eventually as described by an empirical exponential model:

$$V_{Shift-Dirac} = V_1 + V_2 \cdot \exp\left(-\frac{|V_{BS_i}|}{V_3}\right) \quad (95)$$

where V_1 , V_2 and V_3 are constants.

5. The Residual Carrier Density

Considering an equal distribution of the residual carrier density in hole and electron puddles, and including the effect of the opening of an energy bandgap, the residual carrier density is written as [96]:

$$n_{puddle} = \frac{2m_{eff}}{\pi\hbar^2} k_B T \left\{ \ln \left[1 + \exp \left(\frac{-\frac{E_g}{2} + \Delta}{k_B T} \right) \right] + \ln \left[1 + \exp \left(\frac{-\frac{E_g}{2} - \Delta}{k_B T} \right) \right] \right\} \quad (96)$$

Here, Δ represents the height of the step peak to peak function considered for the spatial electrostatic potential as in Figure 1.12. A direct dependence of the energy bandgap on the top- and back-gate bias conditions induces a consequent variation of the residual carrier density.

6. The Parasitic Series Resistances

In the access regions, contact resistances ($R_{C_{S0}}, R_{C_{D0}}$) and the access region resistances ($R_{S_{Ac}}, R_{D_{Ac}}$) are considered as shown in Figure 2.6. The bilayer graphene layer in the access regions, which is not covered by the top-gate stack, presents a series access resistance which is only affected by the back-gate voltage through electrostatic doping.

In the graphene access regions, the opening of an energy bandgap is also attributed only to the effect of the back-gate bias. Thereby, in the drain access region, the energy bandgap can be written as:

$$E_{g-D} = \kappa \cdot D_{b-D} \quad (97)$$

Similarly, in the source access region, the energy bandgap is represented as:

$$E_{g-S} = \kappa \cdot D_{b-S} \quad (98)$$

where κ is a parameter set to 8.74×10^{-11} eV·m/V as in (80). The displacement fields in the drain and source access regions, D_{b-D} and D_{b-S} , respectively are given by:

$$D_{b-S} = \frac{\epsilon_{back} \cdot (V_{BS_i} - V_{bg_{0-S}})}{t_{back}} \quad (99)$$

$$D_{b-D} = \frac{\epsilon_{back} \cdot (V_{BD_i} - V_{bg_{0-D}})}{t_{back}} \quad (100)$$

where $V_{bg_{0-S}}$ and $V_{bg_{0-D}}$ are the offset voltages of the Dirac point due to initial environmental carrier doping. V_{BS_i} and V_{BD_i} are the intrinsic back-gate-to-source and back-gate-to-drain voltages, respectively.

Based on the applied bias conditions, an equivalent capacitive circuit of the b-GFET structure for the access regions is shown in Figure 2.10.

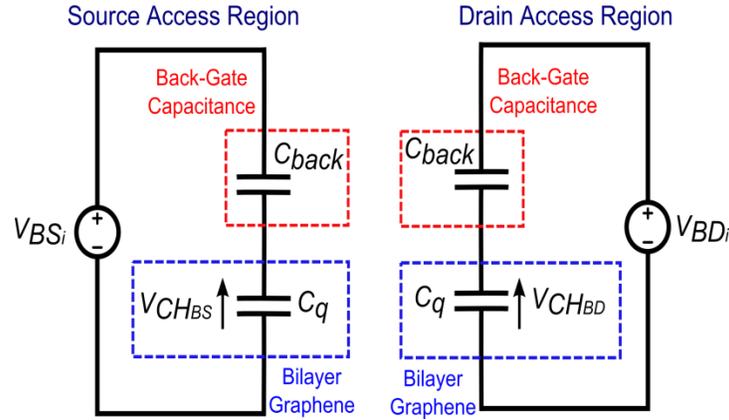


Figure 2.10: Equivalent capacitive circuit of the b-GFET access regions

In the source access region, a Kirchoff's relation based on the equivalent capacitive circuit shown on the right of Figure 2.10 can be written as follows:

$$Q_S + q \cdot N_{FS} = -Q_{BS} \quad (101)$$

where N_{FS} is the net doping of the bilayer graphene layer under the access region, Q_S is the total charge stored in the quantum capacitance and Q_{BS} is the charge induced by the back-gate given by:

$$Q_{BS} = C_{back} \cdot (V_{BSi} - V_{CHBS}) \quad (102)$$

with V_{CHBS} being the voltage across the quantum capacitance in the source access region. It is important to notice that V_{CHBS} is supposed to be constant along the length of the access region opposite to the variation along the channel length of V_{CH} .

When electrons are accumulated in the source access region, the V_{CHBS} can be written based on equations (87), (101) and (102) as:

$$V_{CHBS} = \frac{Q_{back_S} + Q_{FS} + \frac{C_q E_{g-S}}{2q}}{C_{back} + C_q} \quad (103)$$

with $Q_{back_S} = C_{back} V_{BSi}$ and $Q_{FS} = q N_{FS}$.

The self-consistent solutions of equations (87) and (103), allows the calculation of the net charge density in the access region, Q_S . When electrons are accumulated in the source access region, the width-normalized parasitic series access resistance is given by:

$$R_{S_0} = R_{S_{C_0}} + \frac{L_S}{\mu_{n_S} W (|Q_S| + q \cdot n_{BS})} \quad (104)$$

where $R_{S_{C0}}$ is the series source contact resistance, μ_{n_S} is the mobility of electrons in the source region, n_{BS} is a residual charge density in the access region and L_S is the source access length.

The expression above considers that the resistance of the source access region varies inversely with the induced carrier density due to the effect of the back-gate bias.

Similarly, when holes are accumulated in the source access region, $V_{CH_{BS}}$ is written as:

$$V_{CH_{BS}} = \frac{Q_{back_S} + Q_{F_S} - \frac{C_q E_{g-s}}{2q}}{C_{back} + C_q} \quad (105)$$

Leading to a source access resistance of:

$$R_{S_0} = R_{S_{C0}} + \frac{L_S}{\mu_{p_S} W (|Q_S| + q \cdot p_{BS})} \quad (106)$$

Here, μ_{p_S} is the hole mobility in the source region and p_{BS} is the residual charge density in the access region.

Similar to the formulations of the equations (101)-(106), equations for the drain parasitic series resistance can be established based on the equivalent capacitive circuit shown on the right of Figure 2.10.

7. Compact Model Implementation

Following the different modules presented in the previous sections, here, the implementation of the model analytical equations is described for it to be realized in Verilog-A.

As described in the previous chapter, the total drain-to-source current, I_{DS} , is written as the sum of the electron and hole contributions which are given by:

$$I_{DS(n,p)} = \mu_{(n,p)} W \frac{\int \left(|Q_{(n,p)}| + q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_{(n,p)} \left| \int \frac{1}{v_{sat(n,p)}} dV \right|} \quad (107)$$

where $v_{sat(n,p)}$ is the electron/hole saturation velocity given by:

$$v_{sat(n,p)} = \frac{\Omega}{\sqrt{\pi \left(\frac{|Q_{(n,p)}|}{q} + \frac{n_{puddle}}{2} \right)}} \quad (108)$$

Based on (92) and (93), one can introduce the following intermediate variable:

$$z(x) = Q_{top} + Q_{back} + Q_F + Q_{Shift-Dirac} - C_{eq} V(x) \quad (109)$$

A closer inspection of equations (92) and (93), reveals that the sign of V_{CH} is determined by the condition whether $z(x)$ is lower or higher than the term $\frac{C_q E_g}{2q}$. Thereby, considering the channel to be entirely n-type, which is equivalent to $z(x=0)$ and $z(x=L)$ being both positive and bigger than the term $\frac{C_q E_g}{2q}$, the electron and hole current contributions are written as:

$$I_{DSn} = \mu_n W \frac{\int_0^{V_{DSi}} \left(\left| C_q V_{CH} - \frac{C_q E_g}{2q} \right| + q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_n \left| \frac{1}{\Omega} \int_0^{V_{DSi}} \sqrt{\frac{\pi}{q} \left| C_q V_{CH} - \frac{C_q E_g}{2q} \right| + \frac{\pi n_{puddle}}{2}} dV \right|} \quad (110)$$

$$I_{DSp} = \mu_p W \frac{\int_0^{V_{DSi}} \left(q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_p \left| \frac{1}{\Omega} \int_0^{V_{DSi}} \sqrt{\frac{\pi n_{puddle}}{2}} dV \right|} \quad (111)$$

Similarly, when the channel is p-type (equivalent to $z(x=0)$ and $z(x=L)$ being both negative and smaller than the term $-\frac{C_q E_g}{2q}$), the electron and hole current contributions are:

$$I_{DSn} = \mu_n W \frac{\int_0^{V_{DSi}} \left(q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_n \left| \frac{1}{\Omega} \int_0^{V_{DSi}} \sqrt{\frac{\pi n_{puddle}}{2}} dV \right|} \quad (112)$$

$$I_{DSp} = \mu_p W \frac{\int_0^{V_{DSi}} \left(\left| -C_q V_{CH} - \frac{C_q E_g}{2q} \right| + q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_p \left| \frac{1}{\Omega} \int_0^{V_{DSi}} \sqrt{\frac{\pi}{q} \left| -C_q V_{CH} - \frac{C_q E_g}{2q} \right| + \frac{\pi n_{puddle}}{2}} dV \right|} \quad (113)$$

However, when $z(x=0)$ and $z(x=L)$ are different in sign, a change in the carrier polarity occurs within the channel. In these cases, the integrals (107) are separated for two segments of the channel on either side of the energy bandgap limits.

Considering the case when a transition from an n-type to a p-type channel occurs, the electron and hole current contributions are:

$$I_{DSn} = \mu_n W \frac{\int_0^{V_{E_g^+}} \left(\left| C_q V_{CH} - \frac{C_q E_g}{2q} \right| + q \cdot \frac{n_{puddle}}{2} \right) dV + \int_{V_{E_g^-}}^{V_{DSi}} \left(q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_n \left| \frac{1}{\Omega} \left(\int_0^{V_{E_g^+}} \sqrt{\frac{\pi}{q} \left| C_q V_{CH} - \frac{C_q E_g}{2q} \right| + \frac{\pi n_{puddle}}{2}} dV + \int_{V_{E_g^-}}^{V_{DSi}} \sqrt{\frac{\pi n_{puddle}}{2}} dV \right) \right|} \quad (114)$$

$$\begin{aligned}
& I_{DSp} \\
&= \mu_p W \frac{\int_0^{V_{Eg}^+} (q \cdot n_{puddle}) dV + \int_{V_{Eg}^-}^{V_{DSi}} \left(\left| -C_q V_{CH} - \frac{C_q E_g}{2q} \right| + q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_n \left| \frac{1}{\Omega} \left(\int_0^{V_{Eg}^+} \sqrt{\frac{\pi n_{puddle}}{2}} dV + \int_{V_{Eg}^-}^{V_{DSi}} \sqrt{\frac{\pi}{q} \left| -C_q V_{CH} - \frac{C_q E_g}{2q} \right| + \frac{\pi n_{puddle}}{2}} dV \right) \right|} \quad (115)
\end{aligned}$$

where $V_{Eg}^+ = \frac{Q_{tot}}{C_{eq}} - \frac{E_g}{2q}$ and $V_{Eg}^- = \frac{Q_{tot}}{C_{eq}} + \frac{E_g}{2q}$ are the limits of the energy bandgap for which $q \cdot V_{CH} = \frac{E_g}{2}$ and $q \cdot V_{CH} = -\frac{E_g}{2}$, respectively.

Equivalent expressions for the electron and hole current contributions, when a transition between a p-type to an n-type channel exists, can be written as:

$$\begin{aligned}
& I_{DSn} \\
&= \mu_n W \frac{\int_0^{V_{Eg}^+} (q \cdot n_{puddle}) dV + \int_{V_{Eg}^-}^{V_{DSi}} \left(\left| C_q V_{CH} - \frac{C_q E_g}{2q} \right| + q \cdot \frac{n_{puddle}}{2} \right) dV}{L + \mu_n \left| \frac{1}{\Omega} \left(\int_0^{V_{Eg}^+} \sqrt{\frac{\pi n_{puddle}}{2}} dV + \int_{V_{Eg}^-}^{V_{DSi}} \sqrt{\frac{\pi}{q} \left| C_q V_{CH} - \frac{C_q E_g}{2q} \right| + \frac{\pi n_{puddle}}{2}} dV \right) \right|} \quad (116)
\end{aligned}$$

$$\begin{aligned}
& I_{DSp} \\
&= \mu_p W \frac{\int_0^{V_{Eg}^+} \left(\left| -C_q V_{CH} - \frac{C_q E_g}{2q} \right| + q \cdot \frac{n_{puddle}}{2} \right) dV + \int_{V_{Eg}^-}^{V_{DSi}} (q \cdot n_{puddle}) dV}{L + \mu_n \left| \frac{1}{\Omega} \left(\int_0^{V_{Eg}^+} \sqrt{\frac{\pi}{q} \left| -C_q V_{CH} - \frac{C_q E_g}{2q} \right| + \frac{\pi n_{puddle}}{2}} dV + \int_{V_{Eg}^-}^{V_{DSi}} \sqrt{\frac{\pi n_{puddle}}{2}} dV \right) \right|} \quad (117)
\end{aligned}$$

Analytical solutions for the integrals in (110)-(117) have been developed and presented in detail in Appendix B.

D) Results & Discussion

In order to validate the capability of the developed compact model, comparisons with measurements from literature have been made and are presented in this section. Szafranek *et al.* in [117] presented a dual-gate b-GFET device fabricated on a Si/SiO₂ substrate with Ni contacts, an Al₂O₃ top-gate dielectric and a Ti/Ni top-gate electrode. Highly p-doped Si wafers with 90 nm thermally grown SiO₂ was used as substrate.

Figure 2.11 shows the comparison of the measured transfer characteristics and transconductance with the results from simulation of the compact model for different back-gate

voltages. An RMS error of the compact model is found to be of 7 %. As observed in Figure 2.11a, the Dirac point of the transfer characteristics moves towards more positive top-gate voltages as V_{BS} decreases, varying exponentially with V_{BS} (not shown here) as expressed by (95). In addition, higher I_{ON}/I_{OFF} current ratios are observed for more negative back-gate voltages. Particularly, in this device, the maximum I_{ON}/I_{OFF} current ratio is of ~ 17 .

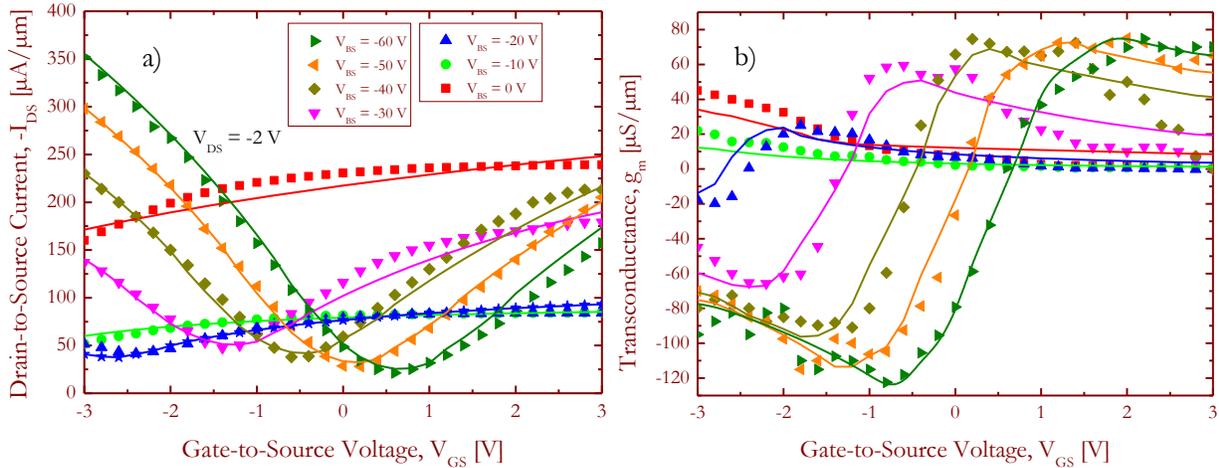
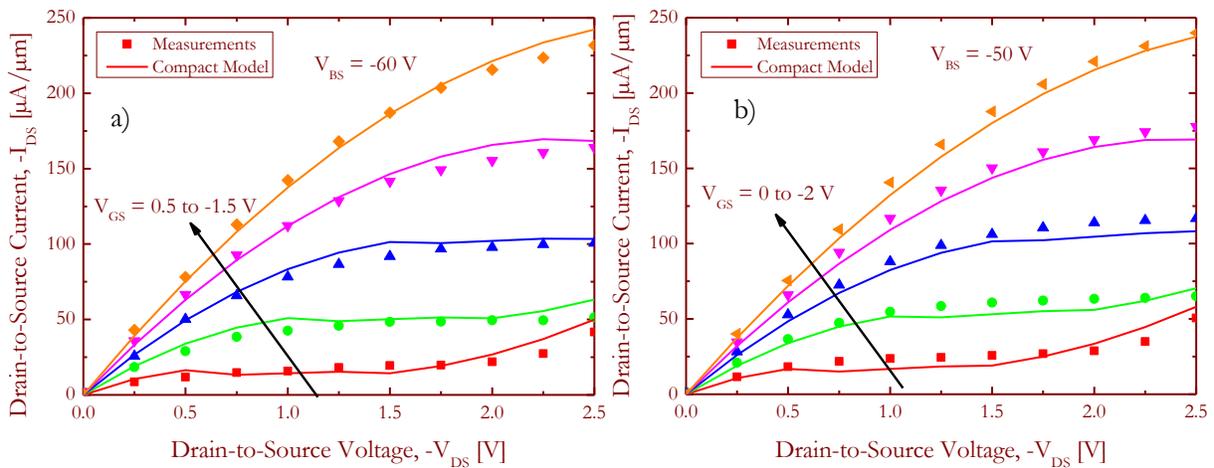


Figure 2.11: Comparison of the measured (symbols) [117] a) transfer characteristics (I_{DS} - V_{GS}) and b) transconductance (g_m - V_{GS}) with the compact model (solid lines) for $V_{DS} = -2$ V and V_{BS} varying from 0 V to -60 V.



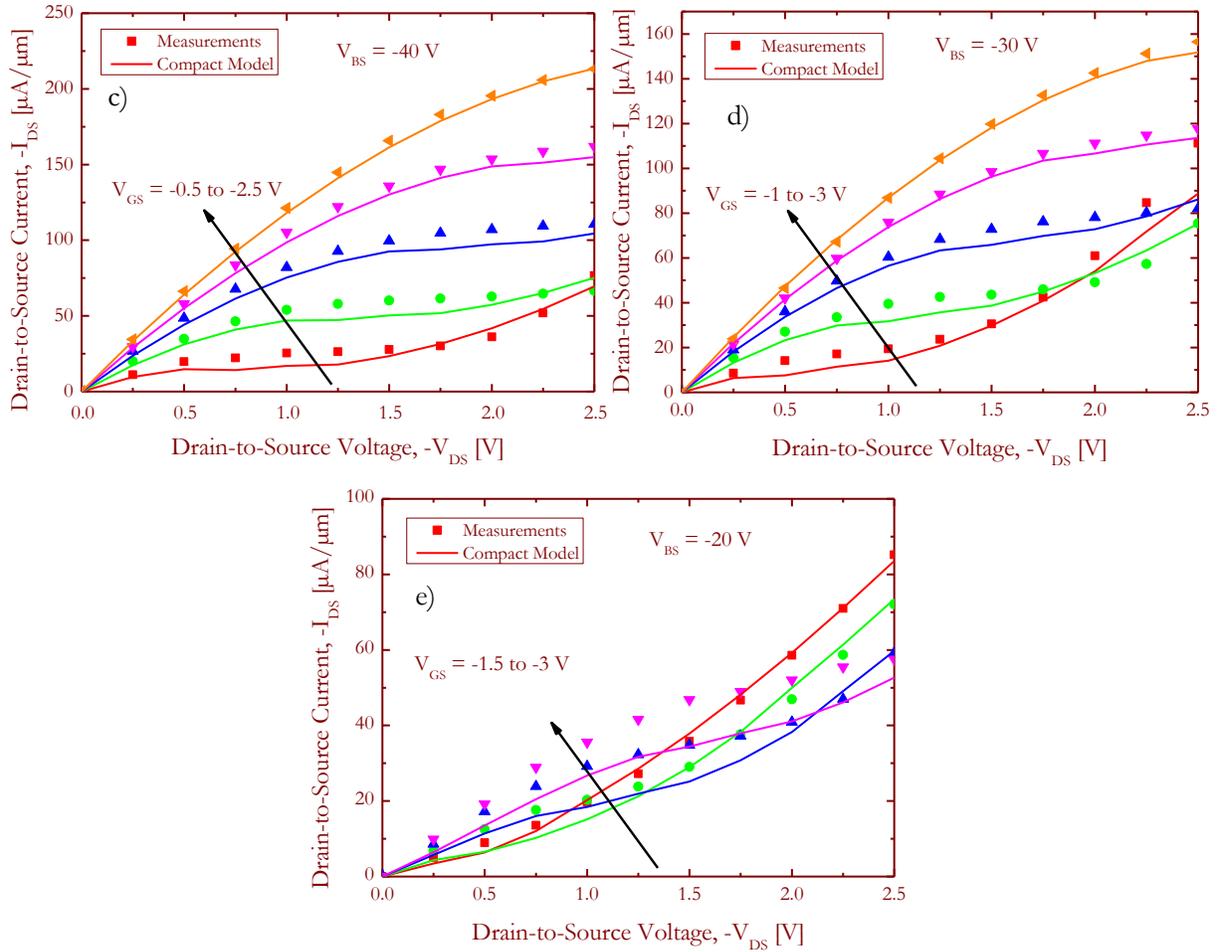


Figure 2.12: Comparison of the measured (symbols) [117] output characteristics (I_{DS} - V_{DS}) with the compact model (solid lines) for different V_{GS} voltages and V_{BS} varying from 0 V to -60 V.

Figure 2.12 presents the comparison of the measured output characteristics and the compact model simulation results. In comparison to the m-GFET devices presented in Chapter 1, the output characteristics in Figure 2.12 present a much more pronounced drain-to-source current saturation, which could be attributed to the opening of an energy bandgap. The kink in the drain-to-source current that signifies the presence of ambipolar conduction is more prominent for lower back-gate voltages.

In comparison to the m-GFET devices presented in Chapter 1, the presented b-GFET device presents an intrinsic voltage gain, A_V , highly dependent on the back-gate voltage. For $V_{BS} = -20$ V, A_V is found to be of ~ 6 whereas for $V_{BS} = -60$ V, an A_V of ~ 35 is observed.

Table 6 lists the extracted compact model parameters as well as the b-GFET dimensions. The offset voltages of the Dirac point due to initial environmental carrier doping, V_{tg_0} and V_{bg_0} , lead to the opening of an energy bandgap varying from 23 meV to 230 meV.

Table 6: Dimensions and Parameters of the modeled b-GFET [117]

Dimension/Parameter	Value
L	4 μm
t_{top}	8 nm
ϵ_{top}	9.1 (Al_2O_3)
t_{back}	90 nm
ϵ_{back}	3.9 (SiO_2)
L_S	3 μm
L_D	3 μm
μ_n	260 $\text{cm}^2/\text{V}\cdot\text{s}$
μ_p	397 $\text{cm}^2/\text{V}\cdot\text{s}$
A	0.037 [96]
N_F	$2.41 \times 10^{13} \text{ cm}^{-2}$
$\hbar\Omega$	54 meV
Δ	55 meV
(V_{tg_0}, V_{bg_0})	(-5.45, 43.1) V
(V_1, V_2, V_3)	(3.48, -4.35, 23.6) V
R_{Sc0}	11.95 $\mu\Omega\cdot\text{m}$
R_{Dc0}	570 $\Omega\cdot\text{m}$
N_{FS}	$5 \times 10^{12} \text{ cm}^{-2}$
N_{FD}	$5 \times 10^{12} \text{ cm}^{-2}$
μ_{nS}	2700 $\text{cm}^2/\text{V}\cdot\text{s}$
μ_{pS}	2560 $\text{cm}^2/\text{V}\cdot\text{s}$
μ_{nD}	3320 $\text{cm}^2/\text{V}\cdot\text{s}$
μ_{pD}	3150 $\text{cm}^2/\text{V}\cdot\text{s}$
n_{BS}	$-2.25 \times 10^{11} \text{ cm}^{-2}$
p_{BS}	$20.36 \times 10^8 \text{ cm}^{-2}$
n_{BD}	$1.38 \times 10^{13} \text{ cm}^{-2}$
p_{BD}	$-37 \times 10^8 \text{ cm}^{-2}$

The agreement between the model and the measurements for ambipolar conduction in the transfer characteristics (Figure 2.11) as well as in the linear and saturation regimes of the output characteristics (Figure 2.12) validates the assumptions and thereby the accuracy of our developed model. In summary, a very good agreement between the developed compact model and b-GFET measurements has been achieved (with a RMS error $< 10\%$) over a wide range of bias.

E) Application- DUT from University of Siegen [129]

Although the use of Bernal stacked bilayer graphene as channel material in GFETs is quite promising, it lacks in another major technological advancement: scalability. This is because large-area growth of Bernal stacked bilayer graphene using chemical vapor deposition (CVD) is still in its infancy. For current state of the art of b-GFET technologies, the controlled growth of Bernal stacked bilayers is very hard to achieve beyond a size of few hundred micrometers [130]. This limits the mass manufacturability and scalability of Bernal-stacked bilayer graphene FETs, two of the key requirements for beyond CMOS technologies. This encourages graphene researchers to look for alternate feasible approaches. One of the possible ways is to use CVD grown monolayer to fabricate bilayer graphene, by artificially stacking two large-area graphene sheets. The GFET technology developed by the University of Siegen follows such an approach which is quite promising in the sense that growth of CVD monolayer graphene is one of the most viable and relatively mature GFET technologies, which one can obtain from large-area graphene sheets on an industrial scale [131].

1. Device fabrication [129]

Here, CVD-grown monolayers, which are polycrystalline in nature, are artificially stacked to fabricate a bilayer and hence, they constitute a system with random crystallographic orientations. Therefore, the absence of an energy bandgap and thus, of a tunable I_{ON}/I_{OFF} ratio in artificially stacked bilayer GFETs (bi-GFETs) can be distinguished from that of the Bernal-stacked bilayer GFETs.

Thermally oxidized (85 nm) p-doped Si <100> wafers with boron dopant concentration of $3 \times 10^{15} \text{ cm}^{-3}$ were diced and used as substrate materials. The artificially stacked bilayer graphene was transferred on to the substrate with the help of a PMMA (poly methylmethacrylate) support layer. After removing the PMMA layer support layer on top of this stack, channels were patterned using oxygen plasma assisted reactive ion etching (RIE). Source and drain contacts were defined using optical lithography with 20 nm Cr/80 nm Au stack thermally evaporated and lifted off in acetone. 10 nm thick e-beam evaporated SiO_2 formed the top-gate dielectric layer, while a 100 nm thick thermally evaporated Al layer formed the top-gate. A cross sectional schematic of the bi-GFET device is shown in Figure 2.13a, and Figure 2.13b shows the optical micrograph of a typical fabricated device at the University of Siegen.

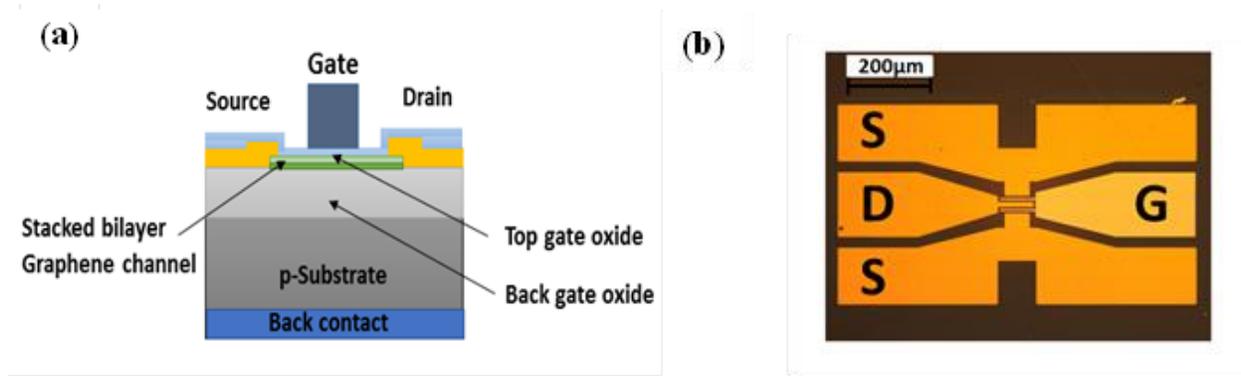


Figure 2.13: a) Cross sectional schematic of stacked bilayer graphene FET (BIGFET) and b) Optical Micrograph showing a completed device after final lift-off step [129]

2. Modelling of DC Characteristics

As the bi-GFET devices have micrometer sized dimensions, they can be studied under the classical drift-diffusion transport approach. Therefore, the experimental data was fitted using our developed b-GFET compact model (presented Section C). However, the DUTs being artificially stacked bilayer GFET devices, it has been considered that under a vertical displacement field, no energy bandgap opening is induced, and thus it has been set to zero. Although the energy bandgap opening being set to zero, the 2-D DOS in (79) remains valid.

Figure 2.14 shows the bi-GFET measured transfer and output characteristics fitted against the compact model by tuning the parameters accordingly within the limits of justification except for the value of $V_{Shift-Dirac}$. A very good fit with a RMS error always lying below 10 % was obtained. This close fit with experimental data could only be obtained when the factors describing the shift in the Dirac voltage, $V_{Shift-Dirac}$, are set to a non-physical value (Table 7). The required values of $V_{Shift-Dirac}$ are non-physical since, compared to a Bernal-stacked bilayer GFET, the shift in the Dirac point in the bi-GFET device is much smaller. It has been found that the expected range of Dirac voltage shift is (0, 15) V, whereas the measured range was only of (0, 600) mV.

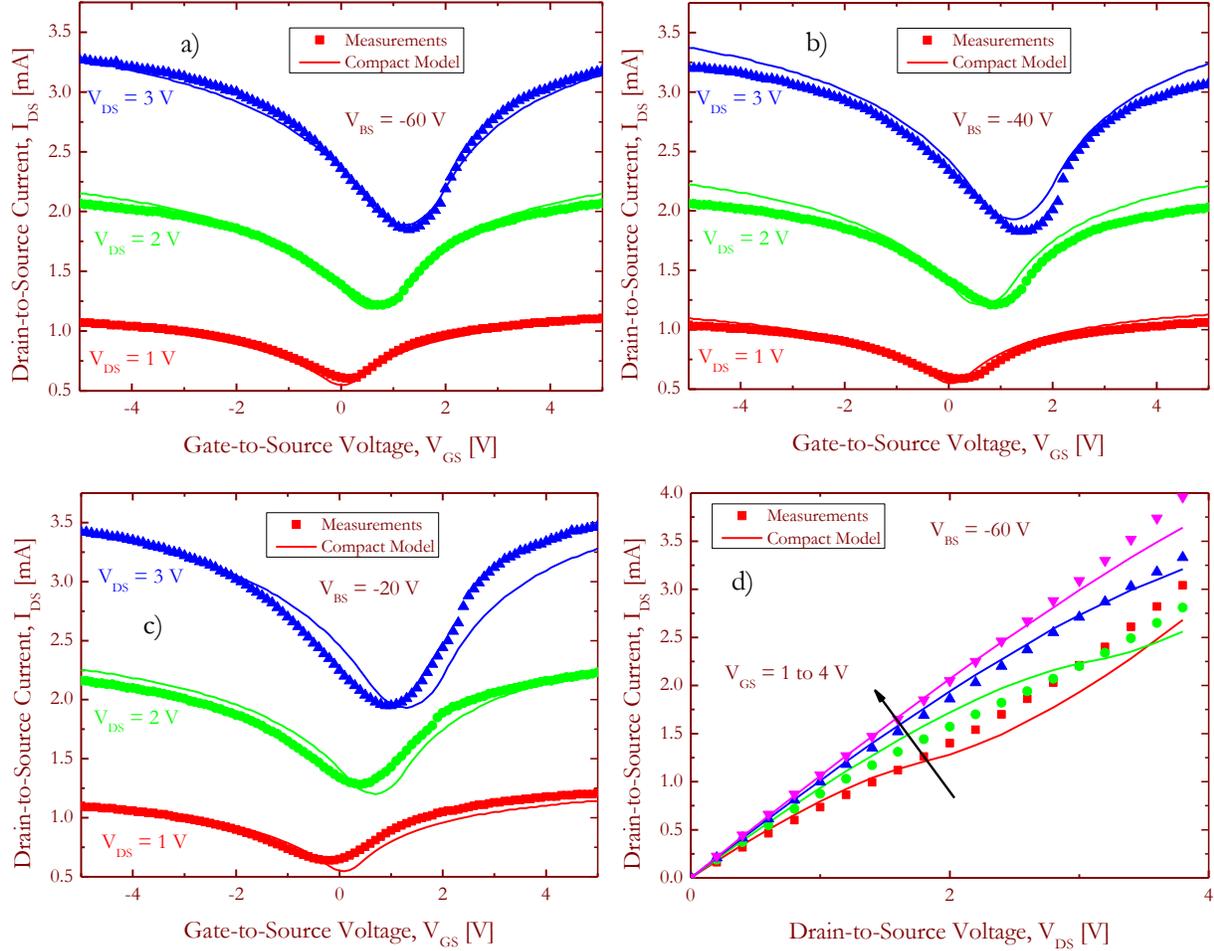


Figure 2.14: Comparison of the measured (symbols) transfer characteristics (I_{DS} - V_{GS}) for $V_{DS} = 1$ to 3 V and a) $V_{BS} = -60$ V, b) $V_{BS} = -40$ V and c) $V_{BS} = -20$ V with the compact model (solid lines). Comparison of the measured (symbols) d) output characteristics (I_{DS} - V_{DS}) for $V_{GS} = 1$ to 4 V and $V_{BS} = -60$ V

Table 7: Dimensions and Parameters of the modeled bi-GFET

Dimension/Parameter	Value
L	12 μm
W	60 μm
t_{top}	10 nm
ϵ_{top}	3.9 (SiO ₂)
t_{back}	85 nm
ϵ_{back}	3.9 (SiO ₂)
μ_n	830 cm ² /V·s
μ_p	610 cm ² /V·s
Δ	51 meV
N_F	1.5×10 ¹² cm ⁻²
A	0.037 [96]

$\hbar\Omega$	50 meV
$V_{Shift-Dirac}$	(0, 15)V
R_{Sc0}	27 m Ω ·m
R_{Dc0}	18 m Ω ·m

As mentioned before, the measured data in Figure 2.14 shows a very small shift in the Dirac voltage (in the order of 600-800 mV) with the applied back-gate voltage ($V_{BS} = -20$ to -60 V) as compared to a shift in the Dirac voltage of ~ 3 V in the case of a b-GFET (presented in Section D) having a tunable energy bandgap of (23, 230) meV when V_{BS} is varied from -60 to 60 V. This shows that, for the bi-GFET device, the effect of the back-gate voltage on the shift in the Dirac voltage is very limited. Using the compact model for a better understanding, it can be concluded that in order to keep the shift in the Dirac voltage within physical limits, an effective back-gate oxide thickness value of 1-2 μm is needed. However, ellipsometry measurements have confirmed the presence of an 85 nm back-gate oxide. These observations indicate the presence of an electric field shielding factor such as a small capacitance from the substrate. There could be two possible causes for this. One of them could be the presence of a very high back-gate leakage current which in turn, undermines the effect of the back-gate voltage, while the other could be the presence of a depletion region under the back-gate, which effectively shields the effect of the back-gate voltage on the channel. However, the former possibility has been dismissed since the measured back-gate leakage currents are only of the order of a few pA. In order to explore the latter possibility, TCAD simulations of the bi-GFET have been carried out.

It has been found that indeed an inversion/accumulation/depletion region is formed under the back-gate oxide/graphene interface, with a substrate doping concentration dependent thickness of the order of a few hundred nanometers up to a few micrometers as the applied back-gate voltage is applied. Figure 2.15 shows the results of the TCAD simulations for a few substrate doping densities.

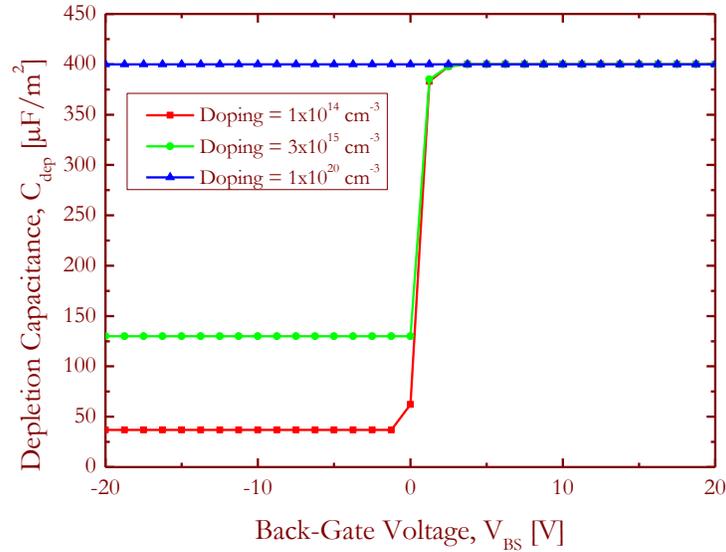


Figure 2.15: TCAD Simulation results – Formation of a depletion capacitance in presence of external back-gate voltages for different substrate doping densities.

Moreover, as the carrier concentration in the channel is varied under different applied back-gate voltages, the depth of the depletion region into the bulk of the substrate also varies as shown in Figure 2.16. This inversion/accumulation/depletion region results in an additional capacitive element leading, to a significantly reduced back-gate voltage induced shift in the Dirac voltage observed in these bi-GFET devices.

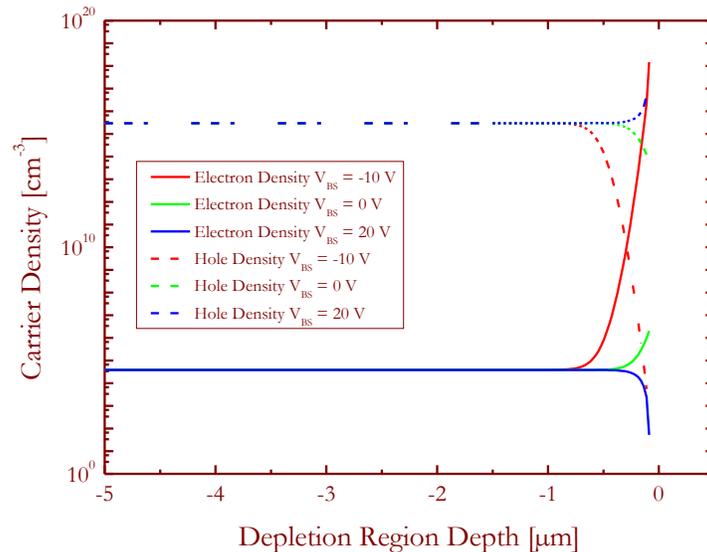


Figure 2.16: TCAD Simulation results – Formation of a depletion region up to a certain depth for different back-gate voltages

F) Conclusion

A physics-based accurate large-signal compact model for Dual-Gate Bilayer Graphene FETs based on the drift-diffusion equation has been developed and implemented in Verilog-A. In addition, the developed model is completely compatible with commercial circuit simulation environments. A comprehensive analysis of the conduction mechanisms in bilayer graphene FETs is presented. Analytical equations for different mechanisms such as bias- dependence of the bandgap and the back-gate bias dependence of access resistances are taken into account in the model to accurately describe the physical mechanisms. A very good agreement between our developed model and with measurement data from literature has been demonstrated for a large range of bias conditions. Also, the compact model has been used as a tool for analysis of artificially stacked bilayer devices, thus proving its versatility.

Chapter 3

RELIABILITY-AWARE CIRCUIT DESIGN

In the last decade, the fascinating physical and electrical properties of graphene have received significant attention from the semiconductor community considering graphene as a promising candidate for future high performance graphene circuits, critical reliability issues need to be addressed. In fact, fabricated ICs that fail the qualification criteria have to be redesigned and passed through the reliability requirements that requires additional time and cost. Time-to-market and fabrication costs are two critical aspects for the success of any technology and therefore, besides improving the reliability of the technology, reliability-aware circuit architectures are highly desirable, involving gain or offset compensation loops to account for transistor degradation over the circuit lifetime [132]. For efficient design, accurate simulation and modeling of the failure mechanisms responsible for transistor degradation are mandatory. Keeping that in mind, this chapter addresses the extension of the model presented in Chapter 1 to account for critical degradation issues of graphene FET devices.

A) State of the Art

Till now, there have been a few reports on reliability studies in graphene FETs [133]–[136]. Two well-known degradation mechanisms are charge trapping in the gate insulator [135]–[138] and the defect creation (interfacial states) in the channel or gate insulator [139], [140]. Defect state creation is accompanied by a change in the slope of the current due to mobility degradation, while charge trapping simply causes a shift in the transfer characteristics due to the traps located in the interface or bulk dielectric layers. Both the aging studies in [135] and [136] reflect bias-temperature

instability (BTI) which is a well-known degradation mechanism quite often reported for conventional MOSFET technologies. Most of the well-known works that extensively analyze the stress-relaxation dynamics attribute the creation of interface states and oxide charges as the main reason for device degradation following bias temperature stress. In the works of Huard *et al.* [141], the recoverable component is attributed to hole trapping while the permanent component is explained by the creation of interface states. However, recent works by Grasser *et al.* [142] suggested that a single charge trapping-dominated theory is more universal and versatile. Models for stochastically distributed reliability mechanisms have been proposed [143], [144] and even recently it has been suggested the random telegraph noise (RTN) and BTI are due to similar defects [145]. Although, such extensive analyses are rare for graphene based FETs, development of an analytical aging compact model that will follow in the footsteps of the MOSFET BTI theories could become the first step towards efficient reliability analysis for graphene technologies.

B) Experimental Details of Aging Tests

In [135], [136], stress-induced degradation in GFETs has been studied using aging test with the devices under constant back-gate voltage stress for long duration, while the evolution of their transfer characteristics were recorded periodically.

For the GFET device reported in [135], the graphene layers have been transferred onto a heavily doped silicon substrate with thermally grown 90-nm SiO₂ back-gate dielectric. For the device reported in [136] the graphene layer has been prepared by using inductively coupled plasma CVD.

Liu *et al.* [135] reported on the positive bias stress-induced shift in the back-gate transfer characteristics (I_{DS} - V_{BS}), denoted by ΔV_T , and its dependence on back-gate bias stress $V_{BS, stress}$. It has been shown that ΔV_T increases with a power law dependence in the early stage of stressing and gets saturated for long stress time. In a similar work, Lee *et al.* [136] reported on reliability of the back-gate CVD-grown graphene FETs fabricated under prolonged back-gate bias stress. Both the results reported by [135] and [136] are consistent with each other showing identical degradation behavior under back-gate stress voltage and show no apparent change in the subthreshold slope, implying negligible mobility degradation.

In the bias stress measurements reported in [135], the ΔV_T shift of the GFETs is demonstrated under positive back-gate bias stress, ($V_{BS, stress}$) at room temperature for a stress period up to 1000s. Here, ΔV_T is defined as the back-gate voltage shift at a constant drain current, $I_{DS} = (I_{max} + I_{min})/2$, where I_{max} and I_{min} are the maximum and minimum drain currents. The

I_{DS} - V_{BS} curve is observed to shift toward positive back-gate voltages with increasing stress time, t_{stress} (shown in Figure 3.1)

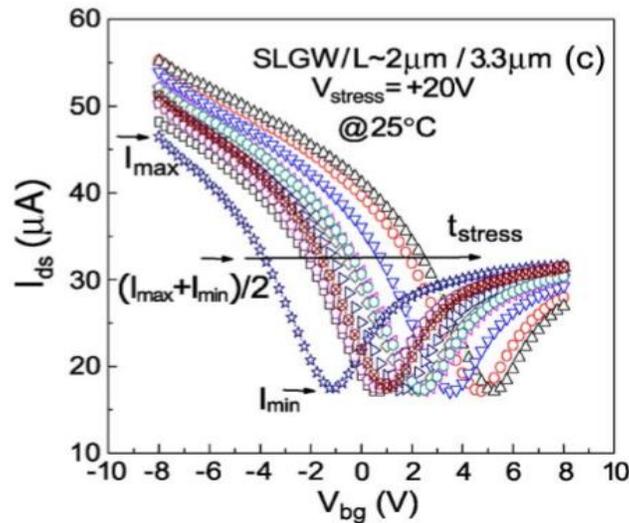


Figure 3.1: Schematic of ΔV_T shift under positive bias stress [135]

In [135], the degradation is mainly attributed to hole trapping in bulk SiO_2 or at the graphene/ SiO_2 interface, and trap generation in bulk SiO_2 . It is theorized that the shift, ΔV_T , saturates after long stress time due to unavailability of further broken bonds that were responsible of charge trapping. Figure 3.2 shows the ΔV_T at different stress voltages as a function of stress time.

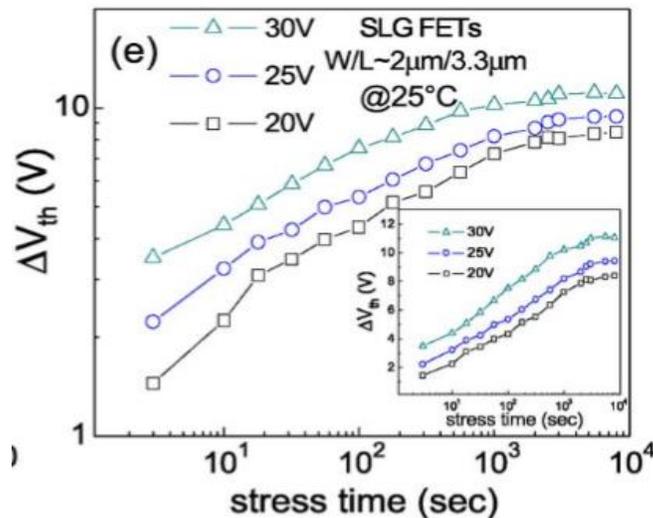


Figure 3.2: Time evolution of ΔV_T at various positive stressing V_{BS} at 25 °C [135]

In [136], the applied back-gate bias stress, $V_{BS, stress}$, was interrupted at fixed times to record the transfer characteristics (I_{DS} - V_{BS}) of the GFETs at a drain bias of -10 mV by sweeping the back-gate bias from -10 to 10 V, while the source electrode was grounded (Figure 3.3).

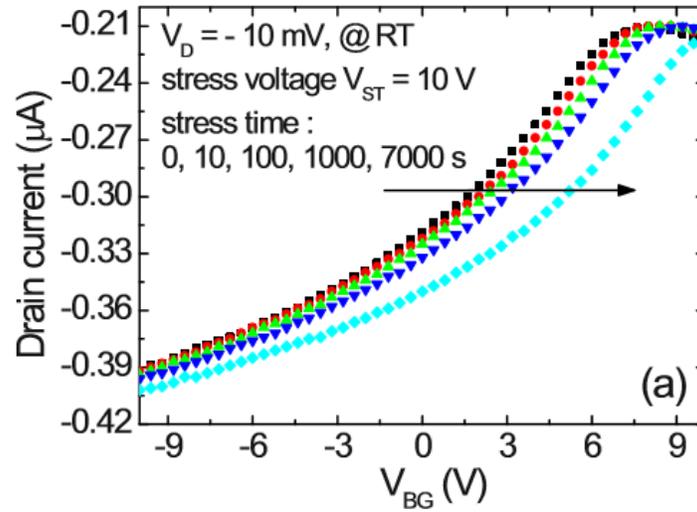


Figure 3.3: Transfer characteristics I_{D_S} - V_{B_S} curves shift under a constant voltage stress of 10 V [136]

The experimental results in [136] (Figure 3.3) also demonstrate that the time dependence of ΔV_T , which also reflects the shift in the Dirac point (Figure 3.4), is in agreement with the stretched-exponential time dependent equation defined as [137]:

$$\Delta V_T = \Delta V_{MAX} \left[1 - \exp\left(-\left(\frac{t}{\tau}\right)^\delta\right) \right] \quad (118)$$

where ΔV_{MAX} is the maximum shift of the transfer characteristics, τ represents the characteristic trapping time of carriers, and δ is the stretched-exponential exponent parameter.

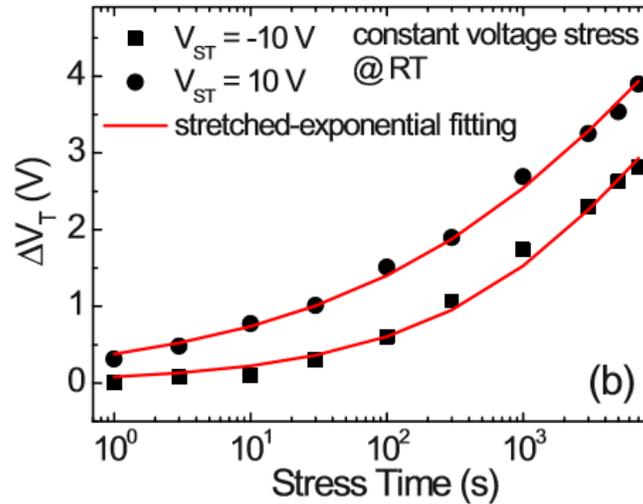


Figure 3.4: Time dependence of ΔV_T under constant gate stress biases (V_{ST}) of 10 and -10 V [136] at room temperature (RT).

Figure 3.5 shows the evolution of ΔV_T under dynamic stresses ($V_{B_S, stress} = -10$ V) with a duty cycle of 0.5 and a period of 2000 s [136]. It can be observed that ΔV_T increases during the stress

phase and decreases during the recovery phase but does not fully recover for a given recovery time of 10^3 s. The time constant of the stress phase is smaller than that of the recovery phase, indicating that a part of the trapped charges is located in deep traps of the dielectric, and remain relatively stable.

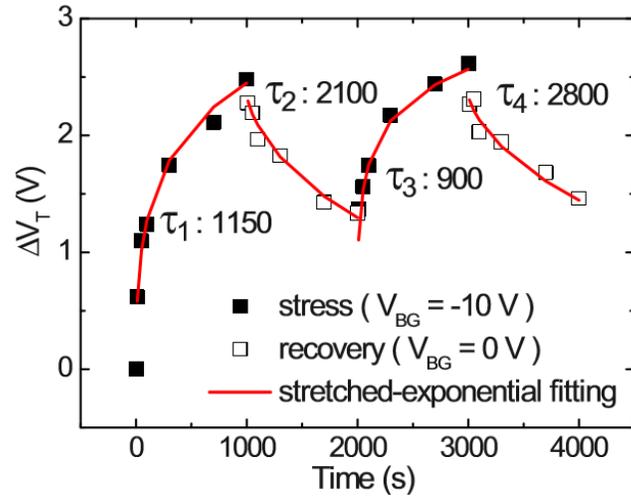


Figure 3.5: Time dependence of ΔV_T under dynamic stresses with a duty cycle of 0.5 and a period of 2000 s [136]

The third set of GFETs under test are CVD GFET devices reported in [146], [147] measured at IMS Laboratory that consist of large scale monolayer graphene grown by CVD on Cu foils and transferred over pre-patterned back-gated devices on Si/SiO₂ substrate.

The aging measurements performed at IMS Laboratory of the CVD GFETs [146], [147] were carried out at fixed positive top-gate bias stress ($V_{GS, stress}$) of 2 V and the measured I_{DS} - V_{GS} characteristics show both a shift as well as a mobility degradation (reflected by the change in slope of the current-voltage curve in Figure 3.6) which can be attributed to both carrier trapping and interfacial state creation [140]. The aging measurements were performed for 3000 s and the transfer characteristics were recorded after every 1000 s. In this case, there is a positive charge build up at the graphene-SiO₂ interface and electron trapping at the top-gate dielectric. Evidently, the electron trapping being dominant, a shift in the transfer characteristics towards the negative bias direction is observed (Figure 3.6), as opposed to the previous results reported in Figure 3.1 and Figure 3.3 for a back-gate stress voltage.

The devices in [136] and [146], [147] are the same, technology wise, and their degradations were similar. All the results from literature introduced previously as well as the measurements carried out at IMS Laboratory have been considered together for improving the applicability of the aging model presented in the following.

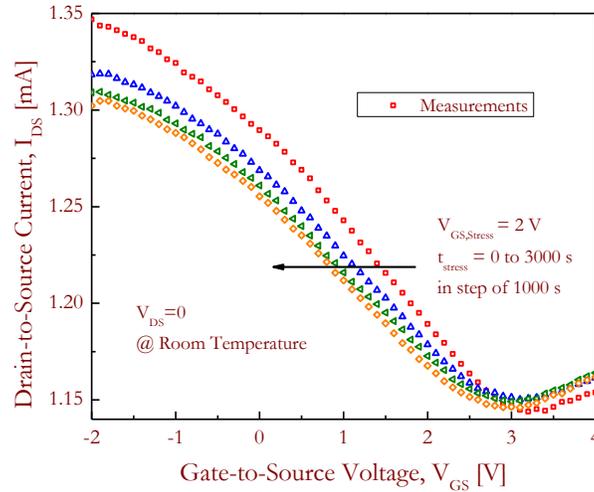


Figure 3.6: Evolution of I_{DS} - V_{GS} as a function of stress time for CVD GFETs [146], [147]

C) Aging Compact Model (This Work) [83]

For the development of the aging compact model, physics of two principle degradation mechanisms were considered which are described in details in the next subsections.

1. Trap Generation

When a positive top-gate bias stress, $V_{GS, stress}$, is applied, negative charges (electrons) are trapped in the dielectric layer. The trapped electrons act as a negative electrostatic gate and cause the transfer characteristic I_{DS} - V_{GS} to shift towards negative V_{GS} voltages, as in the case of the CVD GFET devices [146], [147] (Figure 3.6), described in the schematic shown in Figure 3.7. On the other hand, a positive charge layer, which acts as an effective positive electrostatic back-gate, could build up at the graphene-substrate interface (back-gate) in response to a positive $V_{GS, stress}$.

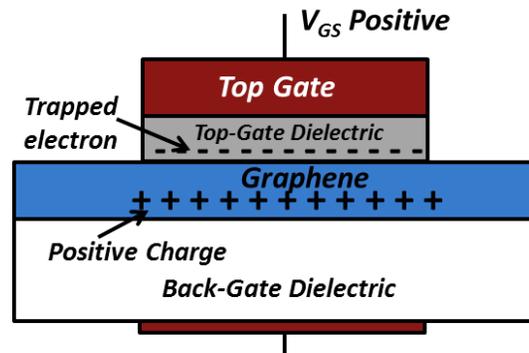


Figure 3.7: Electron and hole trapping in the graphene channel in response to a top-gate stress voltage

The opposite happens for a positive $V_{BS, stress}$, as shown in [135]: there is a negative charge build up near the back-gate electrode and hole trapping at the graphene-SiO₂ interface causing the transfer characteristic $I_{DS}-V_{BS}$ to shift towards positive V_{BS} (Figure 3.8).

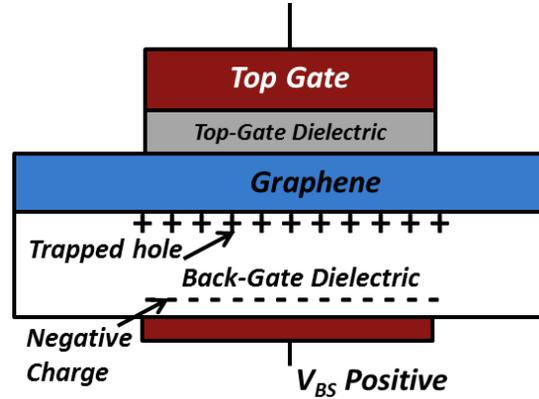


Figure 3.8: Electron and hole trapping in the graphene channel in response to back-gate stress voltage

The behavior of the shift of the transfer characteristic (ΔV_T shift) was derived from the logarithmic [148] and stretched-exponential time-dependent models [137] based on the charge trapping mechanism. The logarithmic model does not indicate redistribution of trapped interface charges, contrary to the stretched-exponential time dependence model that considers the increased emission of trapped charges towards energy states located deep in the bulk dielectric, for longer stress time t and larger stress field [136]. The trap redistribution is further assisted by the dangling bond edges in the gate dielectric that act as transport states for lower energy trapped charges [137]. For the aging module in the GFET aging compact model, a similar charge trapping mechanism has been adopted in which the rate of the charge trapping can be written as [138], [139]:

$$\frac{dN_{trap}}{dt} = \frac{1}{\tau} (N_{SS} - N_{trap}) \quad (119)$$

where N_{trap} is the trap density, τ is the characteristic trapping time constant, and N_{SS} is the steady-state trap density at infinite time. The basis of the charge saturation is that with long stress time, all the broken bonds that act as trap centers are filled [135]. The solution of this differential equation gives:

$$N_{trap} = N_{SS} \left[1 - \exp\left(-\left(\frac{t}{\tau}\right)\right) \right] \quad (120)$$

which is similar in form with the equation (118) for ΔV_T , and therefore, the stretched exponent, δ , can be introduced as a fitting parameter:

$$N_{trap} = N_{SS} \left[1 - \exp \left(- \left(\frac{t}{\tau} \right)^\delta \right) \right], \quad N_{SS} = f(V_{stress}) \quad (121)$$

The trap density in (121) has been implemented in the aging compact model using equation (19) (presented in Chapter 1) for the channel potential, V_{CH} , as:

$$V_{CH}(x) = \text{sign} \left(Q_{tot} - C_{eq}V(x) \right) \frac{-C_{eq} + \sqrt{C_{eq}^2 + 4\alpha |Q_{tot} + q \cdot N_{trap} - C_{eq}V(x)|}}{2\alpha} \quad (122)$$

Equation (122) has been used to perform transient simulations to obtain the results. To model the V_T shift at different stress voltages, the N_{SS} parameter needs to be a function of the stress voltage. N_{SS} can be defined empirically as:

$$N_{SS} = N_1 + N_2 V_{GS, stress}^{\alpha_1} - N_3 V_{BS, stress}^{\alpha_2} \quad (123)$$

where N_1 , N_2 , N_3 , α_1 , and α_2 are fitting parameters. The aging compact model also includes the recovery period, in which the trap density is described by the same stretched-exponential model as:

$$\frac{dN_{trap}}{dt} = - \frac{N_{trap}}{\tau_{recovery}} \quad (124)$$

In the recovery period, N_{trap} is defined as:

$$N_{trap} = N_{SS} \exp \left(- \left(\frac{t}{\tau_{recovery}} \right)^\delta \right) \quad (125)$$

The reversible nature of the V_T shift indicates that the relaxation behavior is associated with the detrapping of the previously trapped charges.

2. Interface State Generation

In some GFETs, there is also significant mobility degradation (reflected by the modification in slope of the transfer characteristics) due to bias stress. A positive top-gate bias stress will create negative interface states at the graphene-dielectric interface along with electron trapping (similar to Figure 3.7) (these two components may be active together to cause both current degradation and voltage shift). The electrons and interface states act as a negative electrostatic gate, which decreases the effective electrical field in the graphene channel for the same gate supply voltage compared with the condition without interface factors, leading to a decrease in I_{DS} [140]. Consequently, to include interface trap generation, the model has been modified by adding the interface state density, and

thereby causing modifications in the source and drain access resistances [149]. The rate of interface state generation can be written as [139]:

$$\frac{dN_{it}}{dt} = A_1 \cdot \exp(A_2 E_{ox}) \quad (126)$$

Here, A_1 and A_2 are fitting parameters and the oxide stress field E_{ox} is a function of the interface state density [139] given by:

$$E_{ox} = E_{ox_0} - \frac{qN_{it}}{C_{top}} \quad (127)$$

Effectively, the stress time-dependent interface state density can be written in the general form derived as [139]:

$$N_{it} = N_{it_0} \log\left(1 + \frac{t}{\tau_S}\right) \quad (128)$$

where τ_S is the interface state time constant and N_{it_0} is consistent with the unit of interface state density but with a fitting parameter value. The interface state density modulates the source and drain access resistances as:

$$R'_{D_0} = R_{D_0} + r_{dt} \cdot FLAG_{interface} \frac{N_{it}}{Q_{fit}} \quad (129)$$

$$R'_{S_0} = R_{S_0} + r_{st} \cdot FLAG_{interface} \frac{N_{it}}{Q_{fit}} \quad (130)$$

where r_{st} , r_{dt} and Q_{fit} are fitting parameters and R_{S_0} and R_{D_0} are the parasitic series resistances for the unstressed devices presented in Chapter 1 Section D). $FLAG_{interface}$ is set to 1 for stress-induced mobility degradation and to 0 for unstressed conditions.

D) Aging Compact Model Validation

The developed aging compact model has been validated through comparison with the results from [135] and [136] and with measurements performed at IMS Laboratory of CVD GFETs [146], [147].

1. Charge Trapping Model

The experimental data obtained from [136] is compared with equations (121) and (122) from the aging compact model simulations and the results show very good agreement, as shown in Figure 3.9.

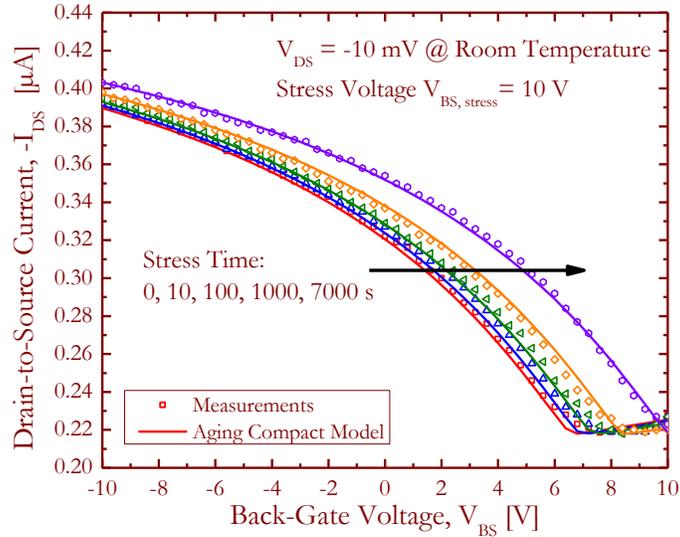


Figure 3.9: Comparison of the GFET back-gate transfer measurements [136] characteristics with the aging compact model.

Transient simulations were performed for a time duration of 7000 s and the obtained shift (ΔV_T) is compared with the reported results for a back-gate stress voltage of 10 V at room temperature. The extracted time constant τ is ~ 4450 s and the stretched exponent is 0.36 in this case. The hole trapping can be attributed to the shift of the Dirac point (or ΔV_T) as the characteristics do not show any significant mobility degradation. A positive applied back-gate stress will cause hole emission in the graphene channel, and thereby shift the transfer characteristic curves towards positive V_{BS} due to hole trapping. The opposite happens for a negative back-gate stress voltage and the extracted time constant τ is ~ 4100 s and the stretched exponent is 0.48. ΔV_T from the aging compact model and the experimental data (from [136]) is shown in Figure 3.10, which show very good agreement.

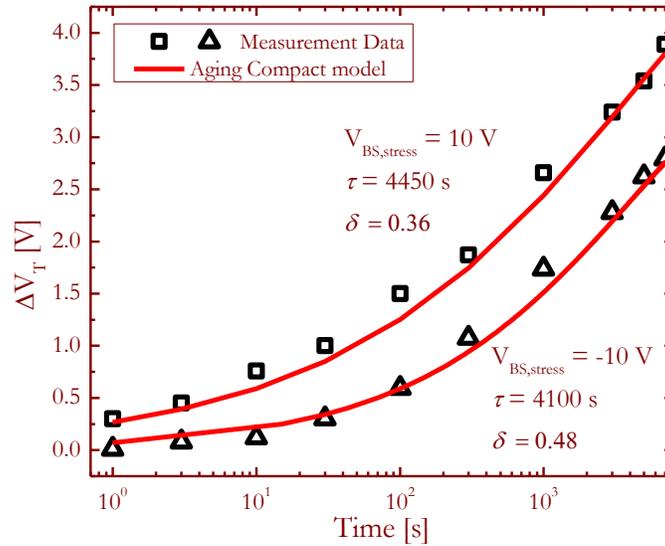


Figure 3.10: Evolution of ΔV_T as a function of stress time for GFETs at different polarities of stress voltages [136]

Figure 3.11 shows the evolution of V_T shift under dynamic stresses ($V_{BS, stress} = -10$ V) with a duty cycle of 0.5 and a period of 2000 s. For the recovery period, (125) is activated. The extracted time constants (Figure 3.11) also agree well with the results in [136].

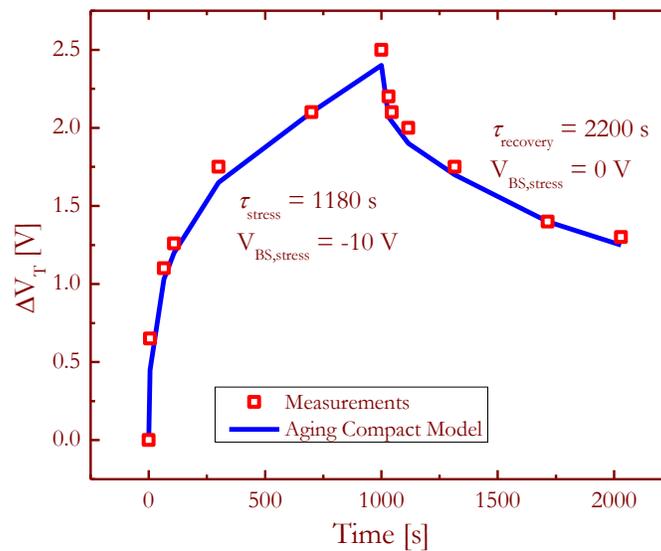


Figure 3.11: Evolution of ΔV_T [36] under dynamic stresses with a duty cycle of 0.5 and a period of 2000 s.

The measurements reported in [135] have been also described by equations (121) and (122) from the aging compact model. In this case, also, the transfer characteristics exhibit a shift towards the positive V_{BS} indicating hole trapping. The results shown in Figure 3.12 compare the aging compact model simulations with the experimental results in [135] for a back-gate stress voltage of 20

V at room temperature, showing very good agreement for a time constant of 244 s and a stretched exponent of 0.36.

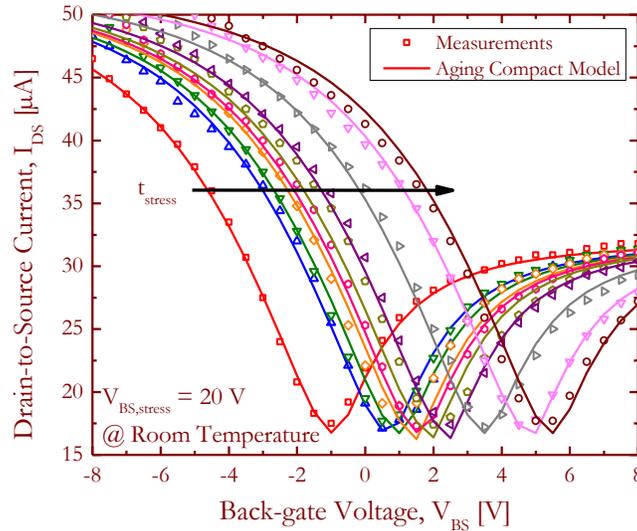


Figure 3.12: GFET back-gate measured transfer characteristics [135] (I_{DS} - V_{BS}) at different stress times

Figure 3.13 compares ΔV_T at the drain-to-source current $I_{DS} = (I_{max} + I_{min})/2$ (which is 36 μA in this case) for different back-gate stress voltages showing both measurements [135] and simulations. It is observed that for higher stress voltages, τ decreases. The aging compact model reveals different values of τ at different values of the stress voltages. The shorter time constants denote a faster response from the traps, i.e., increased emission of trapped charges towards deep states in the bulk dielectric due to the higher stress field [136].

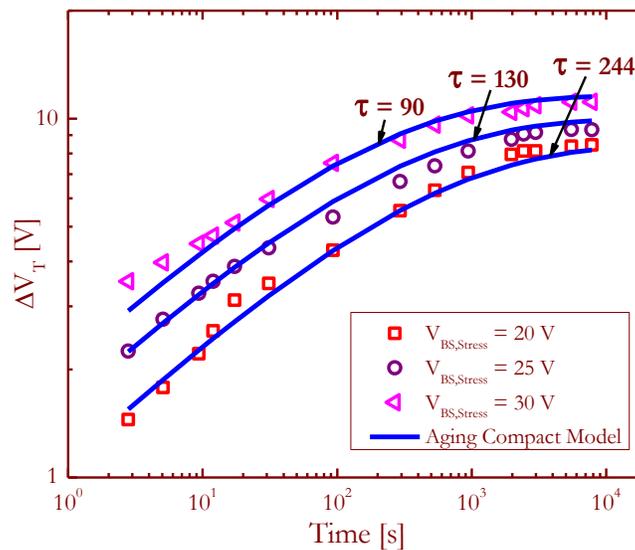


Figure 3.13: ΔV_T as a function of stress time for GFET (measurements from [135]) at different back-gate bias stresses

2. Unified Model combining Charge Trapping and Interface State Generation

For the CVD GFET devices [146], [147] measured at IMS Laboratory, the unstressed device has been modeled using the initial compact model presented in Chapter 1 showing a very good agreement between the measurement and the simulation. The experimental results obtained from the CVD devices under top-gate voltage stress are compared with equations (121) and (122) from the aging compact model as shown in Figure 3.14a. In this case, electron trapping has been considered as suggested by the mechanisms shown in Figure 3.7 and Figure 3.8. It is interesting to note that if the simulation does not consider mobility degradation, there is poor agreement with the measurements at higher currents (Figure 3.14a). Next, the interface state generation has been considered by including equations (128)-(130) in the simulation of the same results as in Figure 3.14a. Clearly, the modified aging compact model describes the results significantly better in Figure 3.14b compared to Figure 3.14a, indicating the presence of some interface state generation in the device, also due to electrical stress. The following parameters have been extracted: a τ of 750 s, a δ of 0.9 s and a τ_S of 6000 s.

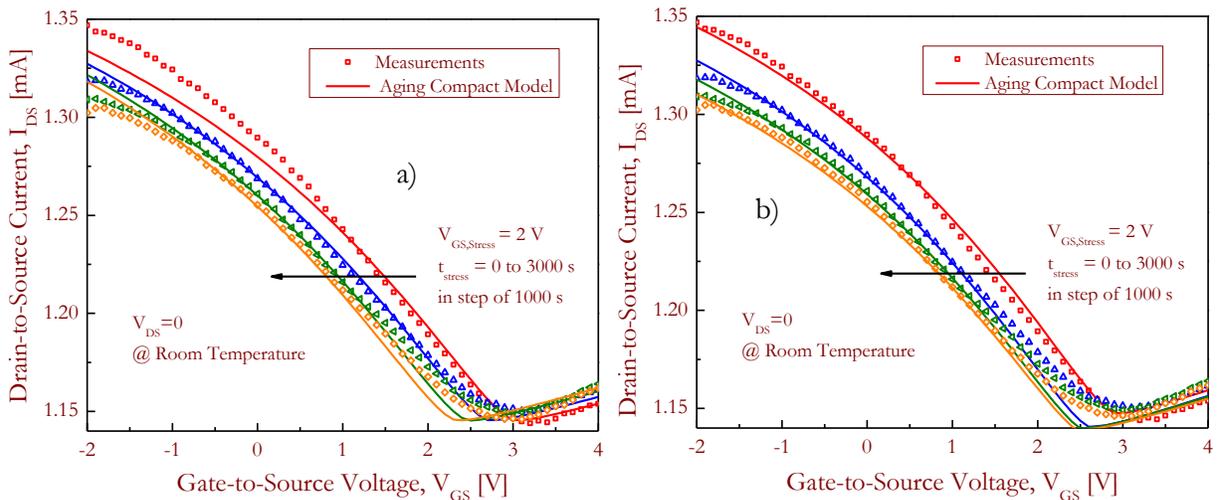


Figure 3.14: Measurement of CVD GFET and comparison with the a) aging compact model including charge trapping and b) unified model including charge trapping and interface state generation [146], [147]

E) Conclusion

A comprehensive aging and reliability analysis for Graphene FETs is presented involving electrical bias-stress measurements and development of an aging compact model. The contributions from both the charge trapping and interface state generation have been described in detail, for

accurate modeling of the bias-stress induced degradation in the GFETs. The developed aging compact model agrees reasonably well with the experimental results for different technologies as well as biasing conditions, thus proving its versatility. Following the physics based approach described in this work (validated on transistor level) the methodology may be extended to circuit level. The aging laws can be implemented in commercial available circuit simulators such as Spectre (Cadence environment) and the impact of aging-induced degradation on the overall circuit can be studied. This methodology can be implemented for reliability-aware graphene circuit design.

Chapter 4

CIRCUIT DESIGN

So far, numerous research groups have focused on the development of high performance Graphene Field-Effect Transistors to approach millimeter-wave operation by improving its intrinsic high frequency performance. In order to inspect the capabilities of GFET devices at circuit level, several GFET-based circuits have been reported. Several circuits, including amplifiers [33]–[35], mixers [36]–[40], frequency receivers [41], ring oscillators [42], detectors [43], [44] and balun architectures [45] have been proposed till date. The importance of the GFET compact models presented in the previous chapters lies in their potential to be incorporated in simulators for circuit design. Thus, in this chapter, three different circuit applications based on GFET devices are presented to explore the circuit level simulation capabilities of the compact model.

A) Triple Mode Amplifier

Because of the ambipolar nature of graphene, graphene FETs present a higher range of functionality compared to unipolar semiconductor devices. As a first demonstration, a triple-mode single-transistor amplifier [150] based on the Dual-Gate Bilayer Graphene FET presented in Chapter 2 Section D) has been designed. The amplifier can operate in three different modes: common-drain, common-source and frequency multiplication mode by taking advantage of the ambipolar nature of the b-GFET. If the top-gate of the b-GFET is biased at the Dirac point and a sinusoidal AC signal is superimposed on the gate bias, full-wave rectification can be obtained at the output [151]. Figure 4.1 shows the schematic of triple-mode single transistor bi-GFET amplifier.

The supply voltage V_{DD} is set to 2 V, V_{BS} to -50 V and the load resistor R_{load} to 1 k Ω . The source is connected to the ground. The input voltage, V_{in} , is a combination of a fixed DC voltage, V_{bias} , and a small sinusoidal AC signal, V_{ac} . The gate-to-source voltage, $V_{GS} = V_{in}$, is therefore $V_{bias} + V_{ac}$.

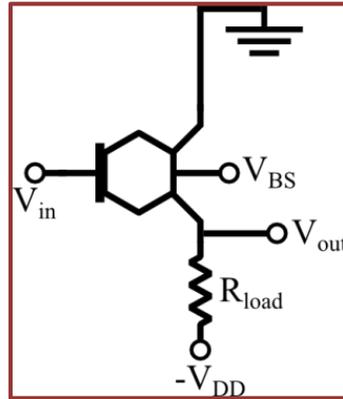


Figure 4.1: Schematic of the triple-mode single transistor amplifier

Depending on the relationship between V_{bias} and the Dirac voltage of the device, V_{Dirac} , three different modes of operation can be established as illustrated in Figure 4.2

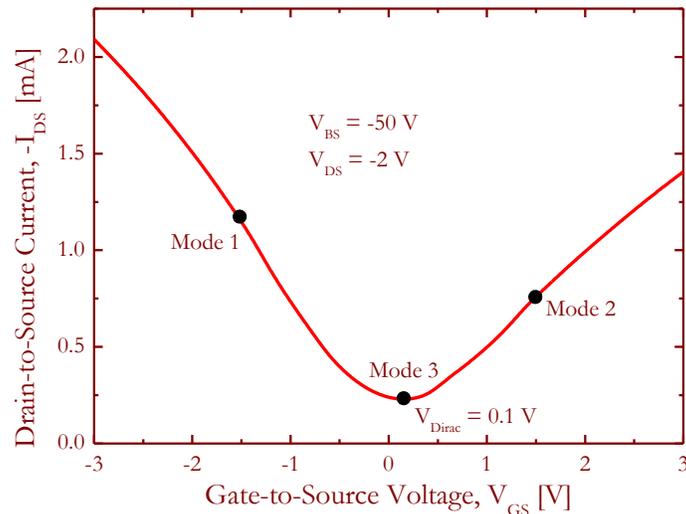


Figure 4.2: Transfer characteristic (I_{DS} - V_{GS}) of b-GFET schematically showing the three bias voltages representing the three modes of operation

In the following, the three modes of operation are introduced in detail:

1. Mode 1: Common-Source Mode

In this mode; the b-GFET is biased in the hole branch ($V_{bias} = -1.5$ V) of the transfer characteristic (Figure 4.2). During the positive phase of V_{ac} , the magnitude of the drain-to-source current decreases and as a result the voltage across the load resistance decreases and the output

voltage, V_{out} , approaches $-V_{DD}$. Similarly, in the negative phase of V_{ac} , the magnitude of the drain-to-source current increases and thus, the output voltage increases. Therefore, the output voltage has the same frequency but is 180° out of phase with the input signal. The amplifier's voltage gain being negative, the amplifier is configured in the common-source mode. Figure 4.3 shows the input and output voltages of the amplifier when configured in the common-source mode.

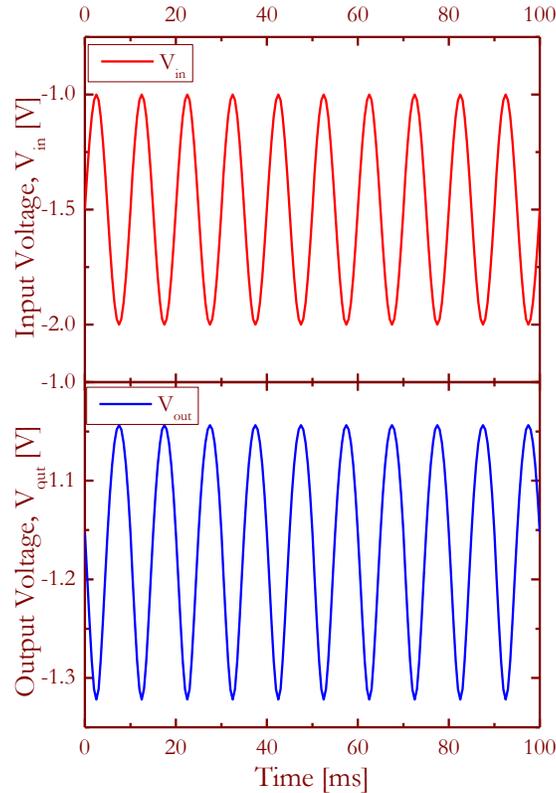


Figure 4.3: Amplifier's Input and Output Voltages when configured in the common-source mode and $V_{bias} = -1.5$ V

2. Mode 2: Common-Drain Mode

In this mode; the b-GFET is biased in the electron branch ($V_{bias} = 1.5$ V) of the transfer characteristic (Figure 4.2). In the positive phase of V_{ac} , the magnitude of the drain-to-source current increases. As a result, the voltage across the load resistance increases as well, and causes the output voltage to increase. Similarly, in the negative phase of V_{ac} , the magnitude of the drain-to-source current decreases resulting in the output voltage (V_{out}) approaching $-V_{DD}$. Therefore, the output voltage has the same frequency and is in phase with the input signal. The amplifier's voltage being positive, the amplifier is configured in the common-drain mode. Figure 4.4 shows the input and output voltages of the amplifier when configured in the common-drain mode.

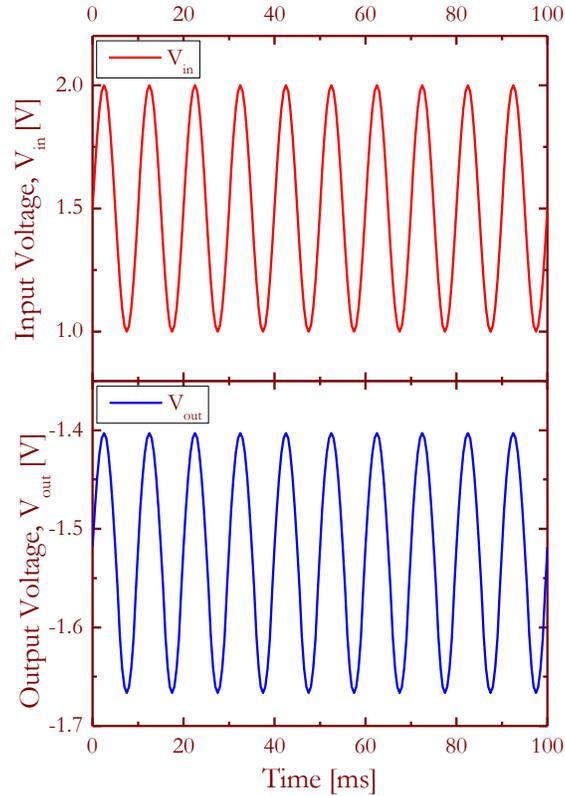


Figure 4.4: Amplifier's Input and Output Voltages when configured in the common-drain mode and $V_{bias} = -1.5$ V

3. Mode 3: Frequency Multiplication Mode

In this mode, the b-GFET is biased at the Dirac point ($V_{bias} = 0.1$ V) of the transfer characteristic (Figure 4.2). In the positive phase of V_{ac} , as discussed previously, the amplifier is configured in the common-drain mode with a positive voltage gain. Similarly, in the negative phase of V_{ac} , the amplifier is configured in the common-source mode with a negative voltage gain. In summary, in the positive half-cycle of V_{ac} , the output voltage is in phase with the input voltage whereas in the negative half-cycle of V_{ac} , the output voltage is 180° out of phase with respect to the input voltage. As a result, the frequency of the output signal is doubled compared to that of the input signal hence, enabling frequency multiplication. Figure 4.5 shows the input and output voltages of the amplifier when configured in the frequency multiplication model.

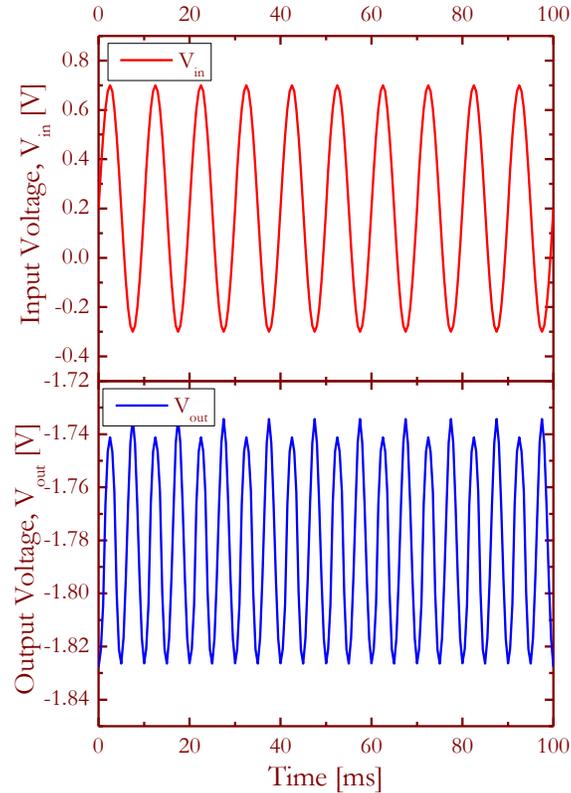


Figure 4.5: Amplifier's Input and Output Voltages when configured in the frequency multiplication mode and $V_{bias} = 0.1$ V

B) Amplifier Design with a SiC Graphene Field-Effect Transistor

In the last few years, some works have been proposed that explored the amplifying characteristics of graphene. J. Lee *et al.* [152] implemented a GFET power amplifier on a printed-circuit board (PCB) where the maximum achievable gain was reported to be 1.3 dB at 380 MHz, after adjusting the values of the passive elements. Andersson *et al.* [153] reported a GFET microwave amplifier using a matching inductor on the gate. It operates at 1 GHz with a power gain of 10 dB and a noise figure of 6.4 dB. Yu *et al.* [34] reported an MMIC (Monolithic Microwave Integrated Circuit) Ku band amplifier based on bilayer epitaxial graphene. The fabricated graphene amplifier shows a power gain of 3.4 dB at 14.3 GHz and a minimum noise figure of 6.2 dB.

While most of the devices show a positive maximum available gain up to the GHz range, it should be noted that in most of the fabricated GFET's, the absence of current saturation in the DC output characteristics prevents voltage amplification. As a consequence, the $|S_{21}|$ power gain is lower than unity at 50 Ω impedance at very low frequencies. In order to use the power amplification

capacity of the GFET devices, one needs to introduce a source impedance matching circuit even at moderate frequencies [153].

Here, a SiC m-GFET [154] has been studied for the design and implementation of an amplifier circuit. A design procedure combining experimental measurements and ADS-simulation has been proposed to evaluate the performances of the SiC GFET-based amplifier. As a first attempt, in order to avoid the dicing of the SiC wafer, an input-matching circuit for the amplifier is connected to the transistor through RF probes using SMA connectors.

1. DC and S-Parameter characteristics of the SiC GFET

The amplifier circuit is based on a SiC m-GFET [154] having a typical gate length of 270 nm, an effective gate width of 48 μm with two fingers of 24 μm each and a 12 nm Al_2O_3 gate dielectric layer (shown in Fig. 1). Source and drain ohmic contacts are metallized with Ni/Au (50/300 nm).

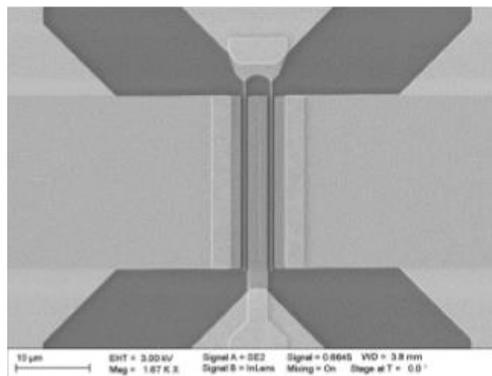


Figure 4.6: SEM image of SiC m-GFET [154]

On-wafer measurements were carried out using a semi-automatic probe station equipped with 40 GHz Microtech's $|Z|$ probes following the procedure described in Figure 1.22. The DC and S-Parameter measurements of the m-GFET were performed with the Semiconductor Analyzer (HP 4155A) and the Vector Network Analyzer (Rohde&Schwarz ZVA67). The measured transfer ($I_{\text{DS}}-V_{\text{GS}}$) and output ($I_{\text{DS}}-V_{\text{DS}}$) characteristics of the SiC m-GFET are shown in Figure 4.7. In fact, the Dirac point from the transfer characteristics (Figure 4.7a) cannot be seen within the measurement range. This shift is most likely due to the n-type doping of the graphene layer and possibly due to the atmospheric doping of the graphene channel during the growth of the graphene layer. In addition; the output characteristics in Figure 4.7b does not show a distinct current saturation. The compact model simulation results are also illustrated in Figure 4.7 in comparison with the measurement which shows good accuracy.

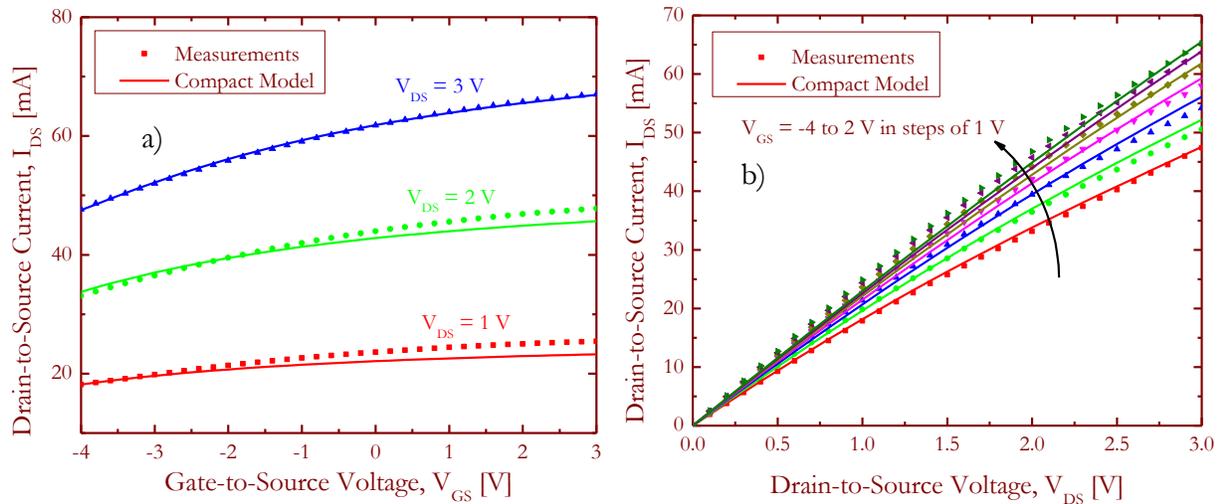


Figure 4.7: Comparison of the measured a) transfer (I_{DS} - V_{GS}) and b) output (I_{DS} - V_{DS}) characteristics of the SiC m-GFET [154] with the compact model

For the S-Parameter measurements of the m-GFET, the reference plane is set at the probe contacts through SOLT calibration in order to measure the m-GFET transistor including the access lines and the pads. The m-GFET S-Parameters have been measured for a frequency range of 100 MHz to 40 GHz. Figure 4.8 show the S-Parameters at the optimum bias conditions ($V_{DS} = 4$ V and $V_{GS} = -3$ V) from both measurement and simulation, demonstrating a good accuracy.

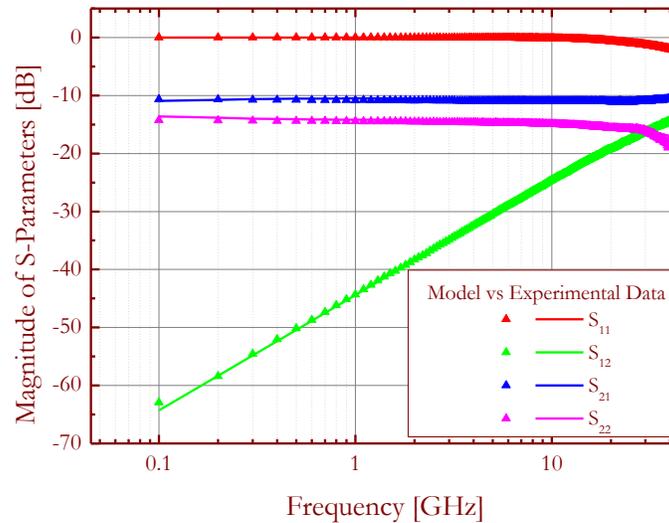


Figure 4.8: Comparison of S-Parameter magnitude in dB obtained from measurements (symbols) with the compact model (solid lines) for $V_{DS} = 4$ V and $V_{GS} = -3$ V for a frequency range of 100 MHz to 40 GHz

Figure 4.9 shows the Smith chart containing the four measured S-Parameters at three different bias conditions. The S_{11} parameter in Figure 4.9 gives an insight into the feasibility of adapting an isolated m-GFET to the 50Ω impedance by moving the S_{11} parameter to the matching

load point [155]. For low frequency ranges, S_{11} is close to the open-circuit point on the Smith Chart which makes the input matching very difficult whereas for high frequencies above 10 GHz (see Figure 4.9), the matching becomes easier.

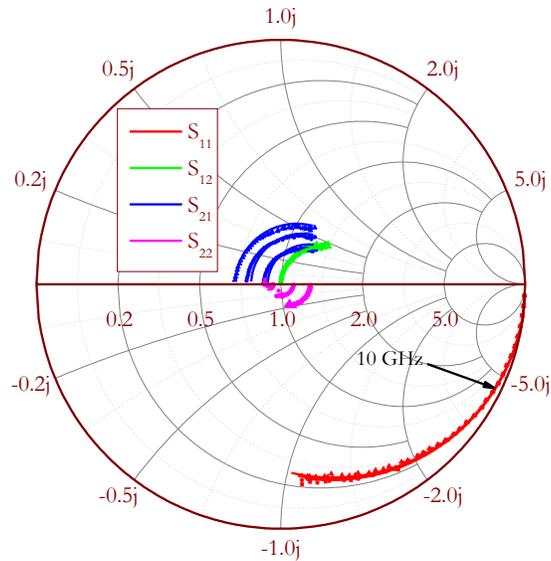


Figure 4.9: Comparison of S-Parameter measurements obtained from measurements (symbols) with the compact model (solid lines) for $V_{GS} = -2$ V and $V_{DS} = 1$ to 3 V for a frequency range of 1 GHz to 40 GHz

The electrical large-signal compact model established in Chapter 1 has been used for the simulation of the electrical characteristics. In addition to the large-signal compact model, the parasitic elements extracted from measurements as well as from electromagnetic simulations (as described in Chapter 1 Section E) were used for compact model simulation. Table 8 compares the extracted values of the parasitic elements obtained from both EM simulation and measurements.

Table 8: Passive Elements extracted values for the SiC m-GFET

Extracted Value	SiC m-GFET [154]	
	Measurement	Simulation
Open-Pad Structure		
C_{11}	10 fF	8 fF
C_{12}	3 fF	3 fF
C_{22}	10 fF	8 fF
Mute Structure		
C_{11}	Structure not available	11 fF
C_{12}		12 fF
C_{22}		8.5 fF
Short Structure		
L_G	Structure not available	30 pH

L_D	30 pH
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Comparisons of the measurements with the compact model simulations are shown in Figure 4.7, Figure 4.8 and Figure 4.9. A very good agreement over a wide frequency range is obtained. The extracted parameters used for the compact model simulation are listed in Table 9. To model the m-GFET device, the empirical model for the parasitic series resistances (described in Chapter 1) has been considered.

Table 9: Dimensions and Parameters of the modeled SiC m-GFET [154]

Dimension/Parameter	Value
L	270 nm
W	48 μm
t_{top}	12 nm
ϵ_{top}	9.1 (Al_2O_3)
μ_n	240 $\text{cm}^2/\text{V}\cdot\text{s}$
μ_p	690 $\text{cm}^2/\text{V}\cdot\text{s}$
Δ	70 meV
N_F	$2.36 \times 10^{13} \text{ cm}^{-2}$
$\hbar\Omega$	75 meV
v_F	10^6 m/s
R_{sh}	0.33 Ω/\square
$N_{\mathcal{F}ng}$	2
$R_{S_{n0}} = R_{S_{p0}}$	$0.47 \times 10^{-3} \Omega\cdot\text{m}$
$R_{D_{n0}} = R_{D_{p0}}$	$1.26 \times 10^{-3} \Omega\cdot\text{m}$
dV/dV_{DS_i}	0.150
(R_{BT_G}, R_{BT_D})	(3, 2) Ω
(C_{BT_G}, C_{BT_D})	1 F
(L_{BT_G}, L_{BT_D})	100 mH
$(C_{pad_{GS}}, C_{mute_{GS}})$	(8, 3) fF
$(C_{pad_{GD}}, C_{mute_{GD}})$	(3, 9) fF
$(C_{pad_{DS}}, C_{mute_{DS}})$	(8, 0.5) fF

Figure 4.10 shows the extracted gate-capacitances, C_{GS} and C_{GD} , as a function of V_{GS} for different V_{DS} voltages.

Figure 4.11 shows the current gain, $|H_{21}|$, and the unilateral power gain, U , as a function of frequency for both measurement and simulation. The maximum cut-off frequency of the SiC m-GFET (without de-embedding) is observed to be around 9 GHz whereas the maximum oscillation frequency is around 10 GHz. After de-embedding, the maximum cut-off frequency of the SiC m-

GFET is observed to be around 15.70 GHz whereas the maximum oscillation frequency is near 22 GHz.

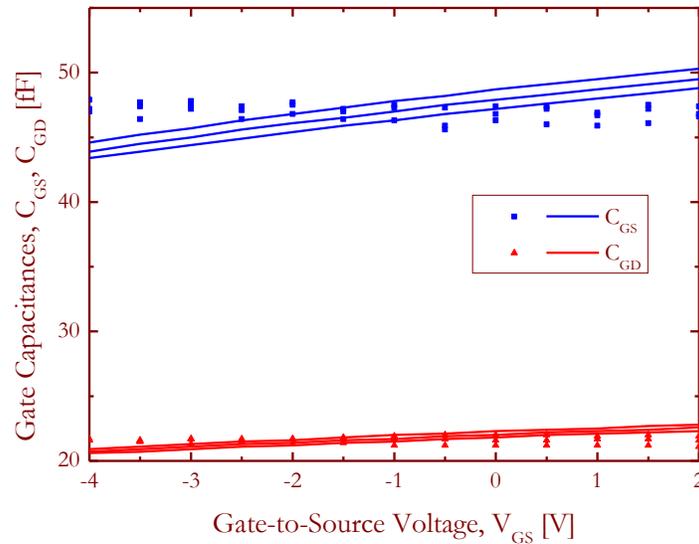


Figure 4.10: Comparison of the extracted gate capacitances, C_{GS} and C_{GD} , from measurements and from compact model simulation as a function of V_{GS} for $V_{DS} = 1$ to 3 V.

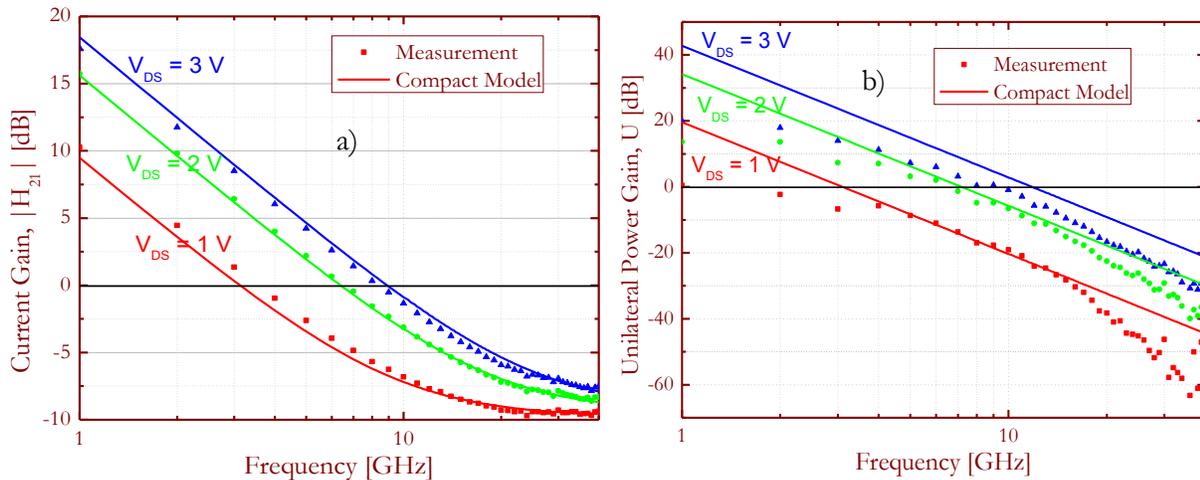


Figure 4.11: Comparison of the extracted a) Current Gain ($|H_{21}|$) and b) Unilateral Power Gain (U) extracted from measurements and from compact model simulation as a function of frequency for $V_{GS} = -2$ V and $V_{DS} = 1$ to 3 V.

The unilateral power gain indicates that the SiC m-GFET can amplify in the GHz range. Nevertheless, Figure 4.8 shows the poor amplification capabilities of the SiC m-GFET with a 50Ω source impedance. It can also be seen that the magnitude of the S_{21} parameter is ~ -10 dB, meaning that the device does not have power amplification in this case, and needs an input impedance matching circuit to achieve such performance.

2. Amplifier Circuit Design

In order to design the amplifier to satisfy the desired performance criteria, one needs to consider a so-called hybrid circuit (that includes RF probes, input-matching circuit and the SiC m-GFET). In order to do so, a model to account for each passive element (input-matching circuit and RF probes) is developed. For measuring and validating each circuit block, the Agilent ENA Network Analyzer has been calibrated up to the SMA cables.

First, a model of the RF probes (shown in the inset of Figure 4.14) has been developed. For this, the S-Parameters of the probe heads placed on a 1.14 ps standard Thru structure from a calibration substrate have been measured. Figure 4.12 shows the RF probe measurement bench schematically.

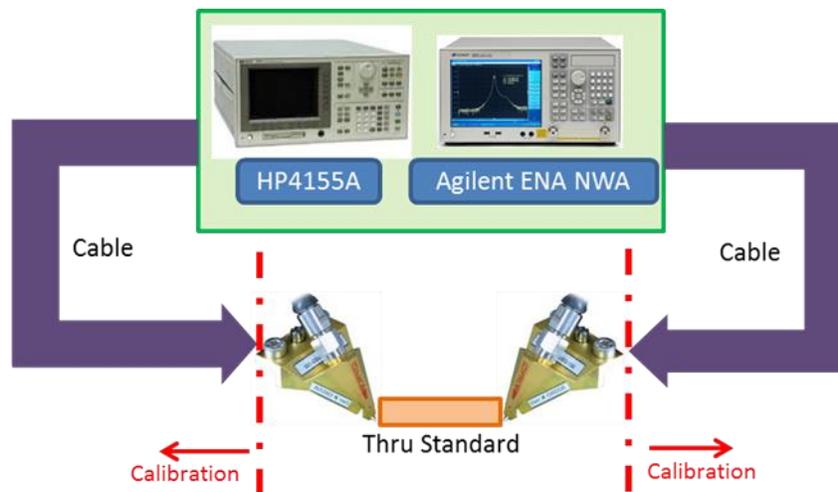


Figure 4.12: $|Z|$ RF Probe measurement bench

As a basic approach to represent the RF behavior of the probe heads in the ADS-simulation environment, they have been modeled as an assembly of CoPlanar WaveGuide (CPWG) line and a series resistance as shown in Figure 4.13.

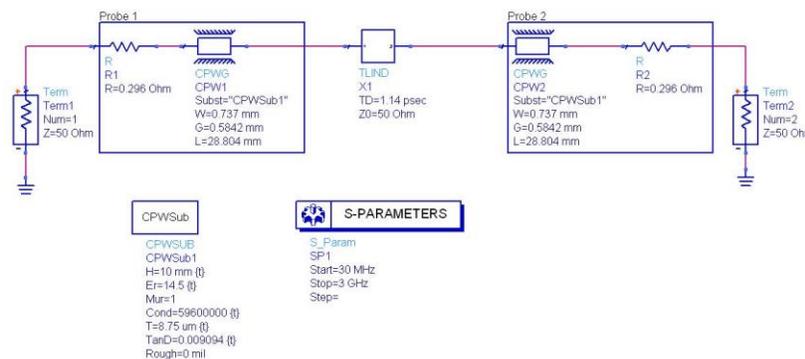


Figure 4.13: ADS-Simulation model of the Probe-Thru-Probe system

The probe heads introduce a large phase shift which has to be taken into account for circuit simulation. Figure 4.14 shows the S-Parameter measurements and the ADS-simulation using the developed model.

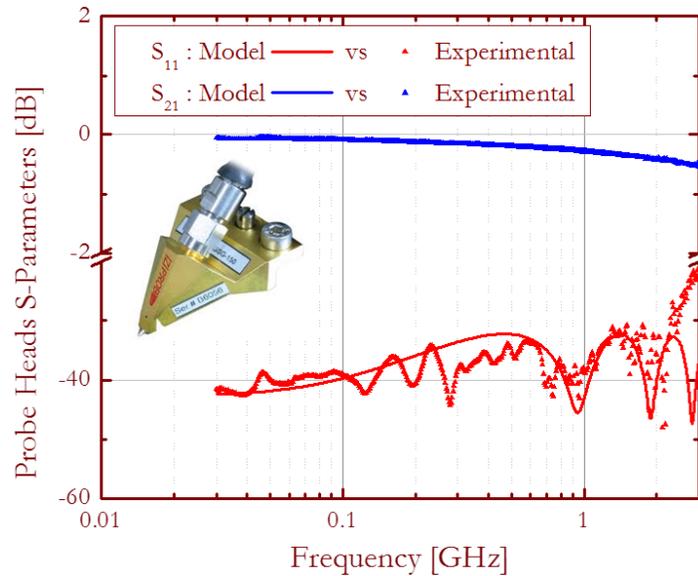


Figure 4.14: Comparison of the probe head S-Parameter measurements with the developed model on a 1.14 ps thru standard

The input matching circuit (shown on the left of Figure 4.15) formed by a 100 nH inductance manufactured by Coilcraft and two 22 pF capacitances, has been fabricated on a 1.28 mm Rogers substrate (dielectric constant of 10.2) suitable for RF applications. The LC circuit is interconnected through 50 Ω CPWG lines on a 2 cm \times 2 cm substrate having line widths of 1.020 mm and a gap between the line and the ground plane of 1.090 mm. It best matches the assembly of the probe heads and the SiC m-GFET at a frequency of 200 MHz. A model for the CPWG lines of the PCB circuit has been developed as shown on the right of Figure 4.15.

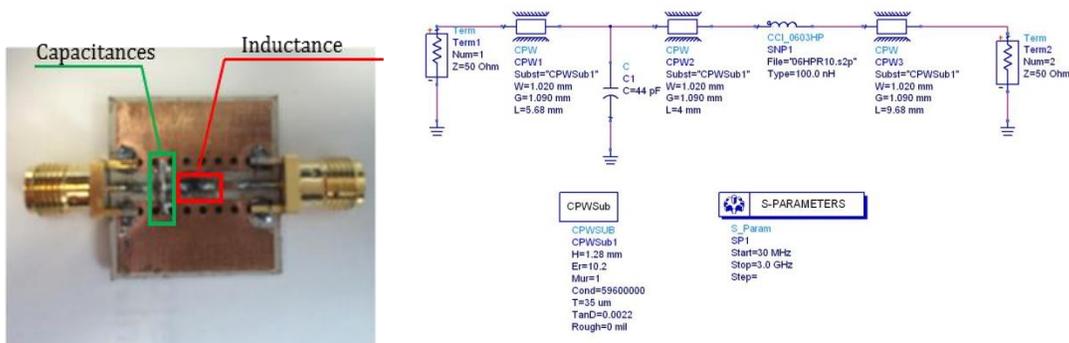


Figure 4.15: (Left) Fabricated PCB Input-matching circuit and (Right) Developed model of the PCB circuit

Figure 4.16 shows the S-Parameter results of the input matching circuit from experimental measurements and ADS simulation.

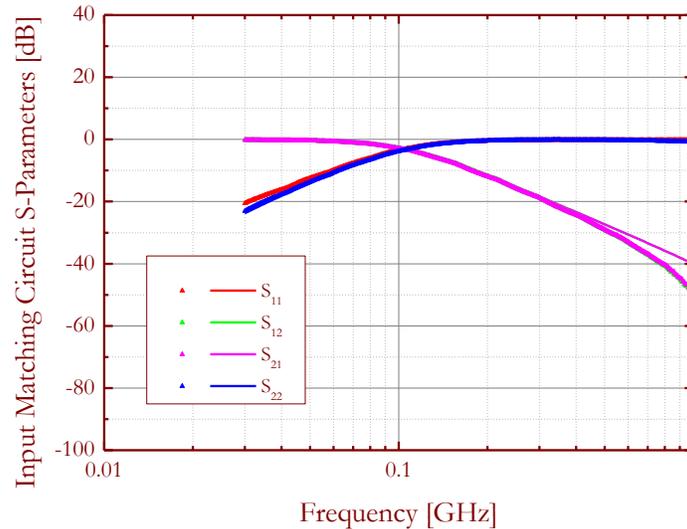


Figure 4.16: Comparison of the LC input-matching circuit measurements (symbols) with the developed model (solid lines).

3. Results

The previous individual blocks (probe heads, input-matching circuit and SiC m-GFET, also called a hybrid circuit) constituting the complete m-GFET amplifier circuit in ADS (Figure 4.17) are compared to the performances of the experimental amplifier (Figure 4.18). For the bias conditions $V_{GS} = -3.0$ V and $V_{DS} = 4.0$ V, a good agreement between the experimental and simulation circuit is achieved (Figure 4.19). The achieved power gains ($|S_{21}|$) are 1.840dB@191MHz and 1.525dB@200MHz, for the experimental and simulation circuits, respectively.

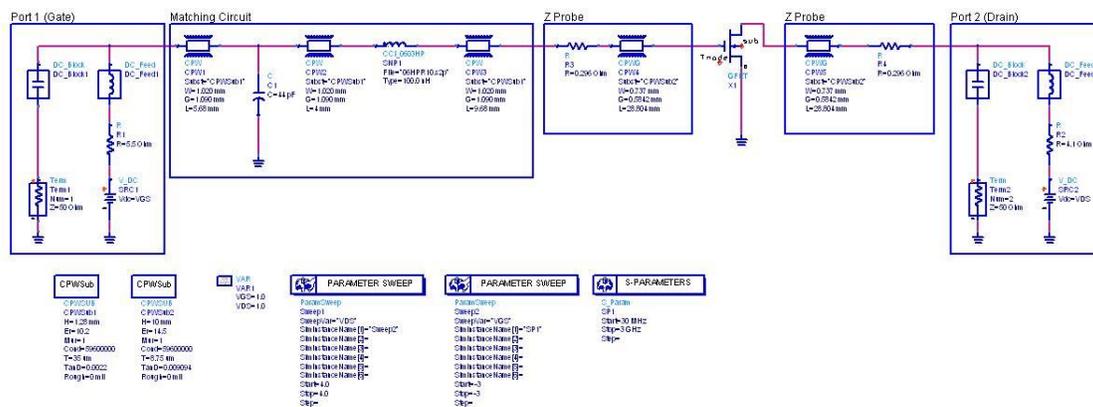


Figure 4.17: ADS Simulation SiC GFET Amplifier Circuit

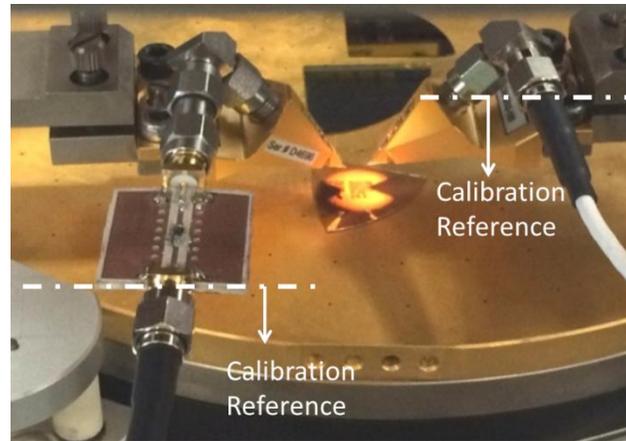


Figure 4.18: Experimental SiC m-GFET circuit amplifier

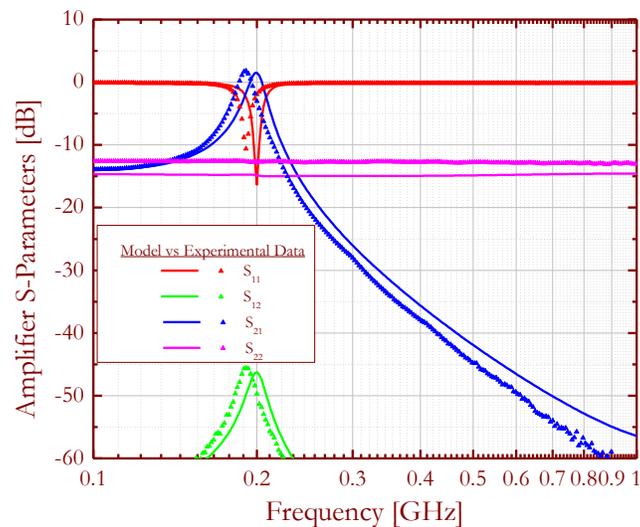


Figure 4.19: Comparison of the SiC m-GFET amplifier measurements (symbols) and the simulation (solid lines) circuit results for $V_{DS} = 4$ V and $V_{GS} = -3$ V

As demonstrated by the results in terms of power and gain, the association of the probe heads to the SiC m-GFET complicates the impedance matching. It adds an excessive phase variation on S_{11} and S_{21} parameters which results in a very sensitive circuit and narrow frequency amplification bands. For example, by removing the probe head contributions from the ADS-simulation and adjusting the LC elements in the input-matching circuit (assuming that the amplifier is fabricated on an MMIC and using hybrid models for the passive elements), a S_{21} power gain of 4.8 dB at ~ 2.4 GHz can be obtained as shown in Figure 4.20.

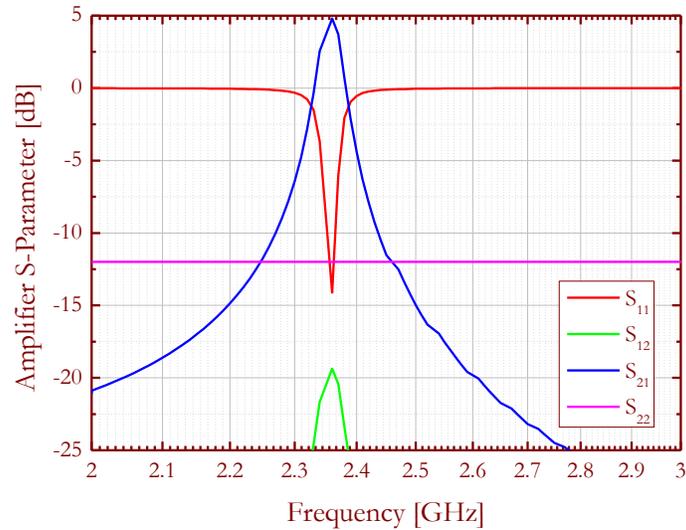


Figure 4.20: S-Parameter of the SiC m-GFET amplifier obtained from ADS-simulation of the assembly of the input-matching circuit and the SiC m-GFET

From the fabrication point of view, an improvement of the current saturation seems to be of utmost importance. Different approaches can be explored. Firstly, a reduction of the access resistance would lead to a higher internal electric field in the channel and it would help in reaching carrier velocity saturation. The access resistances can be reduced using access self-alignment and a proper choice of the metal contact. Secondly, an improvement of the mobility can lead to a faster saturation of the carrier velocity.

C) Balun Circuit Architecture

One of the key concepts for circuit design at very high frequency is the use of differential electronic signals [45]. Balun architectures provide the possibility to transform a single-ended signal into differential signals. From a circuit point of view, differential topologies offer several advantages such as immunity to common-mode noise or, reduction of even-order distortion, for example.

Here, an active balun architecture has been considered based on a differential pair. Thus, to further assess the capabilities of the compact model, EM-SPICE co-simulations have been performed using the developed compact model described in Chapter 1. The GFET balun circuit architecture presented in [45] (Figure 4.21) has been adopted in this study, where a single-ended signal is converted to a differential signal using two SiC m-GFETs (presented in Section B). In this architecture, the active loads (made with SiC m-GFET transistors) are connected to each of the drains on one end and to a power supply on the other end. V_{DD} is positively biased while V_{SS} is negatively biased. Both gates and both sources are connected together. The differential output signals

are measured at the drains (V_{DS1} and V_{DS2}). The supply voltage V_{DD} is set to 3.3 V and V_{SS} to -5 V. The input signal is set to 0.2 V at 1 MHz and is applied to the common gate terminal.

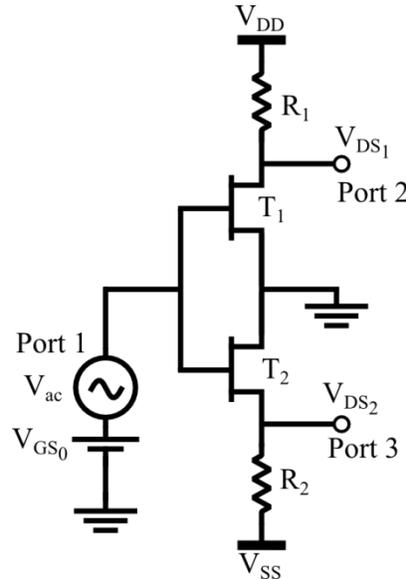


Figure 4.21: Schematic circuit diagram of the SiC m-GFET balun architecture

S-Parameter simulations of the balun circuit architecture were performed in the EM simulation environment (as described in Chapter 1). Figure 4.22 shows the EM structure of the GFET balun architecture used for post-layout simulation.

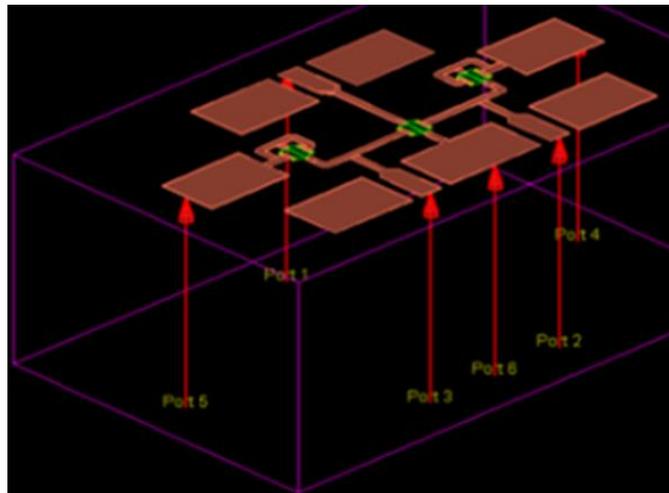


Figure 4.22: EM structure used for post-layout simulation of the GFET balun architecture

The frequency range of the simulation was set from 100 MHz to 10 GHz. Figure 4.23 shows the 180° phase shift between Port 2 and Port 3 of the balun. In addition, Figure 4.23 shows the influence of the Back-End of Line (BEOL) on the balun circuit performance. Evidently, inclusion of the BEOL results in an increase of the phase imbalance of the balun beyond 1 GHz, owing to its capacitive nature.

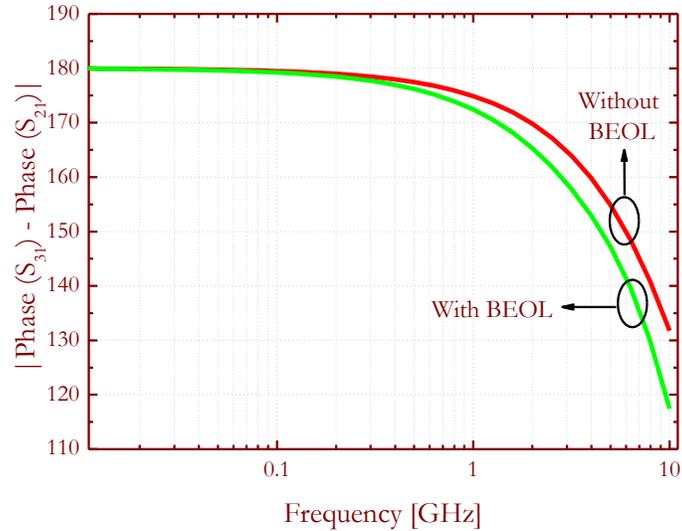


Figure 4.23: Phase Shift between Port 2 and Port 3 (in green: simulation with BEOL and in red: without BEOL)

Figure 4.24 shows the two complementary output signals of the balun corresponding to the applied input signal. A nearly perfect amplitude balance for the two output signals can be observed.

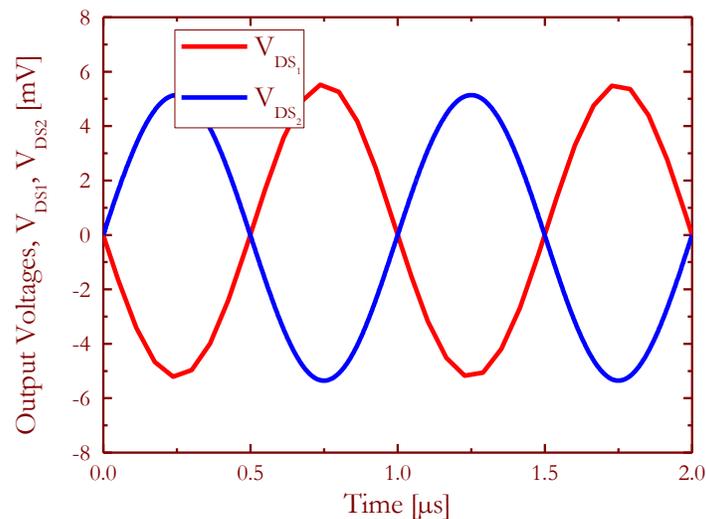


Figure 4.24: Balun's Output Voltages V_{DS1} and V_{DS2} for and input voltage of 0.2 V at 1 MHz

D) Conclusion

In this chapter, three different circuit architectures based on GFET devices have been presented where the unique properties of graphene FET as a viable circuit element are assessed. First, the ambipolar nature of graphene has been considered for evaluating the performance of a triple-mode amplifier.

Secondly, for accurate prediction of the performances of a SiC GFET as a circuit amplifier, a design procedure involving electrical measurements and ADS-simulation has been developed and optimized in order to inspect the full potential of the SiC GFET for power amplification. Employing the probe heads leads to a significant reduction of the amplification band, indicating that the fabrication of the SiC GFET and the input-matching circuit using MMIC might achieve the superior amplifying properties predicted by the ADS-simulation by reducing the gain loss due to parasitics.

Finally, EM-SPICE co-simulations allowed the assessment of the SiC m-GFET in a balun circuit architecture and provided an insight into the influences of the parasitics on the circuit performances, due to the presence of Back-End of Line.

CONCLUSIONS & PERSPECTIVES

This thesis presents an evaluation of the performances of graphene-based transistors projected as a possible candidate for future high-frequency applications for the beyond CMOS roadmap through electrical compact model simulations. In this context, the main contribution of this thesis can be summarized in three different axes of study: electrical compact modeling of graphene-based FETs, study of critical degradation mechanisms of GFETs and GFET-based circuit design.

Concerning the first direction of study, this thesis provides a physics-based large-signal compact model for dual-gate monolayer GFETs which accurately accounts for the ambipolar and unipolar regimes by introducing a branch separation of the contributions of holes and electrons to the total drain current. A classical drift-diffusion transport was considered since the GFET devices, have gate lengths higher than 100 nm, and therefore, ballistic transport was not considered. The compact model was developed based on the 2-D DOS of monolayer graphene and importantly, it has been developed for it to be suitable for DC and RF simulation by accurately describing the bias-dependent gate capacitances. Simplification assumptions to the analytical model equations (validated through comparison with a numerical model), were considered which from a practical viewpoint did not yield a substantial modeling error. The model was therefore implemented in Verilog-A and thus it is ready to be used in standard simulators for circuit design. Moreover, three different approaches to model the effect of the parasitic series resistance were presented and physical interpretations were provided. Furthermore, electro-magnetic simulations of specific test structures are introduced that can estimate the actual performances of GFET devices by accounting for the parasitics introduced by the electro-magnetic environment. In addition, the model was extensively validated through comparison with measurement from two different technologies. A third GFET was used in order to

assess the versatility and applicability of the model under modification of the GFET structure. The model was modified in order to account for the behavior of an additional germanium layer on the GFET structure. In fact, Germanium has been used as an interface layer below graphene and the GFET structure has been studied for a better understanding of the impact of Germanium on the quality of the interface and the carrier mobility.

In addition, an accurate large-signal model for dual-gate bilayer GFETs was presented. As a key modeling feature, the opening and modulation through gate biasing of an energy bandgap was included to the model. Moreover, the ambipolar and unipolar regimes of the graphene in the access regions that are not covered by the top-gate stack were considered. A physical explanation and analogy to conventional MOSFETs was presented for the observed shift in the Dirac voltage under applied back-gate bias which was included to the compact model. The compact model was validated through comparison with measurements from literature and its validity through a large variety of bias conditions and frequency ranges was proven. Also, the compact model was used as an analysis tool for the study of artificially stacked bilayer graphene, thus proving its versatility.

As the second direction of study, aging and reliability analysis of GFETs was presented. This study involved electrical bias-stress measurements and the extension of the compact model capabilities by including aging laws. Bias-stress induced degradation in the GFETs was attributed to two different mechanisms: charge trapping and interface state generation. Moreover, the versatility of the developed aging compact model was validated through comparison with experimental results from different technologies.

Finally, in the last direction of study, the applicability for circuit design of the developed monolayer and bilayer GFET compact models was evaluated. First, the unipolar and ambipolar operation regimes were used for the design of a triple-mode amplifier based on a single bilayer GFET. Second, the study of the performances of a circuit amplifier based on a SiC GFET was presented that provided some insight, through measurement and simulation, into the maturity and potential of the technology for possible application in power amplification. Models for input matching circuit and measuring probes were developed in order to evaluate their impact in the performances of the circuit amplifier. The expected performances of an optimized circuit amplifier were predicted based on electrical simulations. Lastly, the developed compact model along with EM simulations was considered for the further assessment of its capabilities in the prediction of circuit performances. In particular, EM-SPICE co-simulations were used to provide an understanding of the degradation of the circuit performances due to the effect of the Back-End of Line.

In conclusion, this work presented a comprehensive analysis of graphene FETs starting from device to circuit level and even addressed immediate reliability issues, envisioning graphene as a possible candidate for beyond CMOS alternatives. Provided the maturity of graphene, it has yet to evolve much more and thus, future works should be directed to that end. In the following, some of the several promising avenues of research are suggested to extend the study of graphene-based devices and circuit architectures further in the future.

- To extend the model capabilities to multilayer graphene FETs by accounting for the interlayer capacitances, for example.
- To study the performances through simulation and fabrication of an improved circuit amplifier fabricated on an MMIC for inspection of the actual performances and limitations of the technology.
- To extend the physics-based aging and reliability study from the transistor level to the circuit level. Also, to study the impact of aging-induced degradation on the overall circuit performances. Some progress along these lines is already underway, for example, the first fabricated on-chip GFET balun circuit is under development in collaboration with the University of Lille.
- To fabricate and to measure a balun circuit architecture in order to validate the expected performances achieved through simulation.
- To study of the influence of self-heating on the GFET performances by including an additional node to the compact model netlist similar to the conventional SPICE implementation. This needs to be followed by the extraction of isothermal electrical characteristics from measurements, to validate the model accuracy.
- Lastly, the model for bilayer GFETs accounts for a parabolic energy band structure, thus it can be extended to other 2-D materials having similar energy band structure such as MoS₂, for example.

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APPENDIX A

Analytical expressions for the integrals presented in (53)-(60) have been developed for implementation in Verilog-A by considering the following change in variable:

$$u[V(x)] = \sqrt{C_{eq}^2 + 4\alpha|Q_{tot} - C_{eq}V(x)|} \quad (131)$$

A common integral term in the numerator of (53), (56)-(60) can be observed and its integral is given by:

$$\int V_{CH}^2 dV = -\frac{1}{8\alpha^3 C_{eq}} \frac{z}{|z|} \left[\frac{C_{eq}^2 u^2}{2} - \frac{2C_{eq}u^3}{3} + \frac{u^4}{4} \right] \quad (132)$$

where z is given by (52).

In a similar way, the integral of the common term in the denominator of (53), (56)-(60) is given by:

$$\begin{aligned} & \int \sqrt{\frac{\pi\alpha}{q} V_{CH}^2 + \frac{\pi n_{puddle}}{2}} dV \\ &= -\frac{1}{2\alpha C_{eq}} \sqrt{\frac{\pi}{4\alpha q}} \frac{z}{|z|} \left\{ \alpha q C_{eq} n_{puddle} \ln \left[\sqrt{(u - C_{eq})^2 + 2\alpha q n_{puddle}} \right. \right. \\ & \quad \left. \left. - (u - C_{eq}) \right] \right. \\ & \quad \left. - \frac{1}{6} [C_{eq}(u + C_{eq}) - 2(u^2 + 2\alpha q n_{puddle})] \sqrt{(u - C_{eq})^2 + 2\alpha q n_{puddle}} \right\} \end{aligned} \quad (133)$$

For the integrals in (61)-(63), based on the change of variable ($dx \rightarrow dV$) in (65)-(68), the common integral term referred as *Int* is given by:

$$\begin{aligned} Int &= \int \frac{|V_{CH}|}{2\alpha|V_{CH}| + C_{eq}} dx = -\frac{z}{|z|} \frac{\mu_{(n,p)} W}{64\alpha^3 C_{eq} I_{DS(n,p)}} (u - C_{eq})^4 \\ & \quad - \frac{z}{|z|} \frac{q\mu_{(n,p)} W n_{puddle}}{16\alpha^2 C_{eq} I_{DS(n,p)}} (u - C_{eq})^2 \\ & \quad + \frac{z}{|z|} \frac{\frac{dV}{dx}}{\left| \frac{dV}{dx} \right|} \frac{q\mu_{(n,p)}}{3\alpha\Omega C_{eq} \pi} \left[\frac{\pi}{4\alpha q} (u - C_{eq})^2 + \frac{\pi n_{puddle}}{2} \right]^{\frac{3}{2}} \end{aligned} \quad (134)$$

APPENDIX B

Analytical solutions for the integrals in the numerator of (110), (114), (116) are given by:

$$\int \left| C_q V_{CH} - \frac{C_q E_g}{2q} \right| dV = -\frac{C_q}{C_{eq}(C_{eq} + C_q)} \left[\frac{z^2}{2} - \frac{C_{eq} E_g}{2q} z \right] \quad (135)$$

where z is given by (109).

For the integrals in the denominator of (110), (114) and (116), the solutions are:

$$\begin{aligned} \int \sqrt{\frac{\pi}{q} \left| C_q V_{CH} - \frac{C_q E_g}{2q} \right| + \frac{\pi n_{puddle}}{2}} dV \\ = -\frac{2q}{3C_{eq}C_q\pi} \left[\frac{C_q\pi z}{q} + (C_{eq} + C_q) \frac{\pi n_{puddle}}{2} - \frac{C_{eq}C_q\pi E_g}{2q^2} \right]^{\frac{3}{2}} \end{aligned} \quad (136)$$

Similarly, for the integrals in the numerator of (113), (115) and (117), the analytical solutions are given by:

$$\int \left| -C_q V_{CH} - \frac{C_q E_g}{2q} \right| dV = \frac{C_q}{C_{eq}(C_{eq} + C_q)} \left[\frac{z^2}{2} + \frac{C_{eq} E_g}{2q} z \right] \quad (137)$$

And for the denominators in (113), (115) and (117), the solutions for integrals are:

$$\begin{aligned} \int \sqrt{\frac{\pi}{q} \left| C_q V_{CH} - \frac{C_q E_g}{2q} \right| + \frac{\pi n_{puddle}}{2}} dV \\ = \frac{2q}{3C_{eq}C_q\pi} \left[-\frac{C_q\pi z}{q} + (C_{eq} + C_q) \frac{\pi n_{puddle}}{2} - \frac{C_{eq}C_q\pi E_g}{2q^2} \right]^{\frac{3}{2}} \end{aligned} \quad (138)$$

LIST OF PUBLICATIONS

International Journals

1. **Aguirre-Morales, J. D.**, S. Frégonèse, C. Mukherjee, C. Maneux, and T. Zimmer. “A Large-Signal Monolayer Graphene Field-Effect Transistor Compact Model for RF-Circuit Applications” *IEEE Transactions on Electron Devices* (under review)
2. A. Kazemi, F. Cavallo, **J.D. Aguirre-Morales**, S. Frégonèse, S. Vaziri, M. Zamiri, N. Dawson, et al. “Lateral Charge Transfer in Graphene/germanium Heterostructures” (in progress)
3. **Aguirre-Morales, J. D.**, S. Frégonèse, C. Mukherjee, C. Maneux, and T. Zimmer. “An Accurate Physics-Based Compact Model for Dual-Gate Bilayer Graphene FETs.” *IEEE Transactions on Electron Devices* 62, no. 12 (December 2015): 4333–39.
4. Mukherjee, C., **J. D. Aguirre-Morales**, S. Frégonèse, T. Zimmer, and C. Maneux. “Versatile Compact Model for Graphene FET Targeting Reliability-Aware Circuit Design.” *IEEE Transactions on Electron Devices* 62, no. 3 (March 2015): 757–63

International Conferences

1. **Aguirre-Morales, J. D.**, S. Frégonèse, C. Mukherjee, C. Maneux, T. Zimmer, W. Wei and H. Happy, “Physics-Based Electrical Compact Model for Monolayer Graphene FETs” in 2016 *46th European Solid State Device Research Conference (ESSDERC)*, 240–243, 2016.
2. **Aguirre-Morales, J. D.**, S. Frégonèse, C. Mukherjee, C. Maneux and T. Zimmer, “A New Physics-Based Compact Model for Bilayer Graphene Field-Effect Transistors” In *2015 45th European Solid State Device Research Conference (ESSDERC)*, 180–83, 2015.
3. Mukherjee, C., **J. D. Aguirre-Morales**, S. Frégonèse, T. Zimmer, C. Maneux, H. Happy, and W. Wei. “Characterization and Modeling of Low-Frequency Noise in CVD-Grown Graphene FETs.” In *2015 45th European Solid State Device Research Conference (ESSDERC)*, 176–79, 2015.
4. **J. D. Aguirre-Morales**, S. Frégonèse, A. D. D. Dwivedi, T. Zimmer, M. S. Khenissa, M. M. Belhaj, and H. Happy, “Towards amplifier design with a SiC graphene field-effect transistor,” presented at the *Ultimate Integration on Silicon (EUROSIOI-ULIS), 2015 Joint International EUROSIOI Workshop and International Conference on*, 2015, pp. 93–96.

5. Frégonèse, S., **J. Daniel Aguirre Morales**, M. de Matos, C. Maneux, and T. Zimmer. “Graphene FET Evaluation for RF and mmWave Circuit Applications.” In *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2920–23, 2015.
6. C. Mukherjee, **J. D. Aguirre-Morales**, S. Frégonèse, T. Zimmer and C. Maneux, “Statistical Study on the Variation of Device Performance in CVD-grown Graphene FETs”, In *Proc. Graphene Conf Toulouse*, France 2014.
7. **J.D. Aguirre-Morales**, C Mukherjee, Sébastien Frégonèse, C Maneux, T Zimmer, “Analytical Study of Performances of Bilayer and Monolayer Graphene FETs based on Physical Mechanisms”, In *Proc. Graphene Conf Toulouse*, France 2014.