Optimization of Epitaxial Ferroelectric Pb(Zr0.52,Ti0.48)O3 Thin-Film Capacitor Properties

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Numéro d'ordre: 2014-49

ÉCOLE CENTRALE DE LYON

THÈSE

En vue de l'obtention du

DIPLÔME DE DOCTORAT DE L'ECOLE CENTRALE DE LYON

Spécialité : Matériaux

Présentée et soutenue publiquement par

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Thèse préparée à l'Institut des Nanotechnologies de Lyon

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Acknowledgements

This work would have remained unfinished without the help of numerous people. I give my thankfulness to all these great people.

First and foremost I would thank Prof. Yves ROBACH. Without his guidance, I couldn't finish this work on time. In the beginning, he guided me into the oxide field. And at the end, he showed me how to develop a logical well-structured thesis. Through the research, he is always helpful and of great patience. Outside academy, his kindnesses have made my living in this country much easier.

Then I would like to thank Bertrand VILQUIN. Growing oxides with highly crystalline structures requires great caution and profound understanding of materials. Bertrand is a master of almost every machine. Trained by Bertrand to use every required equipment in clean-room, I was able to manipulate all the machines alone. Numerous discussions with Bertrand helped me determine the research direction and achieve objectives.

By his extensive experiences, Nicolas BABOUX has guided me out of the thorns of electric-property identification. By setting up the equipments in an innovative way, we were able to assess the specific characteristic, making further improvement of oxide fabrication much easier. The codes written by Nicolas were really enjoyable, which have greatly reduced the tedious work of data processing. The discussions were often inspired, many of which have greatly optimized my earlier mediocre method.

Being a member of epitaxy group for three years is my great pleasure. From day one, everyone was so helpful and supportive and language barrier has been greatly reduced. Every colleague has a remarkable experience of the undefeated MBE. Michel and Guillaume definitely lead a great team. JB and Claude can fix every problem without delay. Phillippe is a super responsible guard for everyone's safety. There has been so many happiness and amusement to work with all PhD fellows, from the veteran NIU Gang, who has introduced most of the equipments to me in his last days in lab, to the newbies Hélène and Baba and Jeanne, who will definitely do a better work in the coming years. It is of great joy to work in the same team with JB2 and Lamis for the entire study. I give my best wish to Lucie and Nasser, who will conquer every difficulty to obtain their degrees this year. A big thank to Hélène for her generousness. My wish also goes to Rahma, Marie, Benjamin and Amaury, and you can still enjoy your life for another year. Special thanks to YIN Shi and Jose for their great help, especially of XRD. I wish you all continue doing great job.

Electric measurement is limited in micro-scale. With the help of Nano-caracterisation group in INSA, we have achieved in manipulating electric signals in nano-scale, offering much more insight. Thanks for the excellent PFM images from Simon and David, which were better and better in the end of the

study. David's AFM images offered incomparable clearness. The discussion with Brice has helped me understand how PFM works.

I thank Radek, Pierre, Aziz and Brice for their brilliant work. Their maintenance keeps all the machines in great condition with least interruption. Their substantial experiences of every detail can always bring the machine back when I made a mistake or I was stuck.

I am thankful to Raphaël and Laurent for their IT support. I also thank our wonderful secretaries Thérèse, Patricia and Sylvie, who have fixed a great deal of non-scientific problems, making our research work less stressful.

Three years in Lyon, I've made some friends, not many but they are all great people. I hope you all can enjoy your life and work in the following years. Hope to meet you again.

I would like to express my gratitude to China Scholarship Council for its financial support. Without its help, nothing could happen.

Special thanks to QQ. The discussions can usually pull me out of the closed mind, creating much more possibilities.

I express my hearty thanks to the unconditional support of my parents in all these years, back to primary school. 25 years' study, they are always trying their best to give me the best opportunities.

And, I thank my girlfriend for the company, patience and disturbance during these years in the other side of English Channel.

Abbreviations

1T-1C	one transistor and one capacitor
2T-2C	two transistors and two capacitors
3D	3 dimensional
AC	alternating current
ADP	$(NH_4)H_2PO_4$
AFM	atomic force microscopy
BFO	$BiFeO_3$
BOE	buffered oxide etching
BSTO	$(Ba,Sr)TiO_3$
BTO	$BaTiO_3$
C-E	capacitance-field
CMOS	complementary metal-oxide semiconductor
CPE	converse piezoelectric effect
CSD	chemical solution deposition
C-V	capacitance-voltage
CVD	chemical vapor deposition
DC	direct current
D-C	Du-Chen (model)
DRAM	dynamic random access memory
DW	domain wall
EEPROM	electrically erasable read-only memory
FeRAM	ferroelectric random access memory
FN	Fowler-Nordheim (tunnelling)
FP	Frenkel-Poole (emission)
FTJ	ferroelectric tunnel junction
FWHM	full width at half maximum
GASH	$C(NH_2)Al(SO_4)\cdot 6H_2O$
ITO	tin-doped In_2O_3
I-O	Ishibashi-Orihara (model)
I-V	current-voltage

J-E	current-field
KDP	KH_2PO_4
L-Y-D	Landauer-Young-Drougard (model)
MBE	molecular beam epitaxy
MEMS	microelectromechanical systems
MERAM	magnetoelectric random access memory
MFM	metal-ferroelectric-metal
MFSFET	ferroelectric semiconductor field effect transistor
MOCVD	metal-organic chemical vapor deposition
MPB	morphotropic phase boundary
P-E	polarization-field
PFM	piezoresponse force microscopy
P-K	Pulvari-Kuebler (model)
PLD	pulsed laser deposition
PN	refers to the calculation method fro PUND measurement (using the current response to pulse P and pulse N)
PUND	positive up negative down, refers to the characterization method and calculation method (using the current response difference between pulse P and U and between pulse N and D)
PVD	physical vapor deposition
PVDF	poly vinylidene fluoride
PZT	$Pb(Zr,Ti)O_3$
RF	radio frequency
RSM	reciprocal space mapping
RMS	root mean square
RTA	rapid thermal annealing
SCLC	space-charge-limited current
SOI	silicon-on-insulator
SRAM	static random access memory
SRO	$SrRuO_3$
STO	$SrTiO_3$
TEM	transmission electron microscopy
XRD	X-ray diffraction
XRR	X-ray reflectivity

Symbols

A	area of a capacitor	μm^2
A_0	positive constant	
A^*	Richardson constant	$Am^{-2}K^{-2}$
a	lattice parameter along x-axis	Å
a'	accommodation or mutual diffusion length	nm
α	the slope of reciprocal of C_l as a function of thickness	
α	activation field	kV/cm
B	susceptance (imaginary part of Y)	S
b	lattice parameter along y-axis	Å
b	$= ln(1/2)$	
β	intercept of the plot of reciprocal of C_l as a function of thickness	
β_{FP}	positive constant	
β_{FN}	positive constant	
β_{SE}	positive constant	
C	capacitance	F
c	lattice parameter along z-axis	Å
C_{CW}	Curie-Weiss constant	K^{-1}
C_l	linear capacitance	F
C_p-G	parallel circuit mode	
γ	constant	
γ	wall energy	eV
γ_B	binding energy between wall and defects	eV
D	Dimensionality of domain motion	
d	thickness of PZT film	nm
d	the spacing between planes in the atomic lattice	Å
d_{eff}	thickness of dead layer	nm
δ	constant	
E	electric field	kV/cm
E_c	coercive field	kV/cm

E_c^n	negative coercive field	kV/cm
E_c^p	positive coercive field	kV/cm
$(\|E_c^p\| + \|E_c^n\|)/2$	mean value of E_c^p and E_c^n	kV/cm
E_d	depolarization field	kV/cm
E_{if}	field formed inside the interface layer	kV/cm
ΔE_{ac}	activation field of electrons	kV/cm
ε_0	relative	$8.85419 \times 10^{-12}\, F/m$
ε_{opt}	optical permittivity	
ε_r	relative permittivity	
ε_r'	real part of relative permittivity	
ε_r''	imaginary part of relative permittivity	
$\varepsilon_{r_{dl}}'$	relative permittivity dead layer	
ε_{r_l}'	linear part of relative permittivity	
ε_∞	relative permittivity when frequency is infinite	
F	free energy	J
f	equivalent frequency of PUND measurement	Hz
f_0	limiting switching frequency	Hz
G	conductance (real part of Y)	S
g_n	coefficient of the n-th term in free energy equation	
ΔG^*	critical nucleation energy	eV
$\hbar$	reduced Planck constant or Dirac constant	$6.58212 \times 10^{-16}\, eV \cdot s$
θ	angle between the incident ray and the scattering planes	$^\circ$
I_P	current response to pulse P	A
I_U	current response to pulse U	A
I_N	current response to pulse N	A
I_D	current response to pulse D	A
I_{P-U}	$= I_P - I_U$	A
I_{N-D}	$= I_N - I_D$	A
I_d	current due to dielectric polarization	A
I_l	leakage current	A
I_d^n	current due to dielectric polarization under negative voltage	A
I_d^p	current due to dielectric polarization under positive voltage	A
I_l^n	leakage current under negative voltage	A
I_l^p	leakage current under positive voltage	A

J	current	$\mu A/cm^2$
J_P	current response to pulse P	$\mu A/cm^2$
J_U	current response to pulse U	$\mu A/cm^2$
J_N	current response to pulse N	$\mu A/cm^2$
J_D	current response to pulse D	$\mu A/cm^2$
J_{P-U}	$= J_P - J_U$	$\mu A/cm^2$
J_{N-D}	$= J_N - J_D$	$\mu A/cm^2$
J_s^{tot}	current with domain switching in I-V measurement	$\mu A/cm^2$
J_{ns}^{tot}	current without domain switching in I-V measurement	$\mu A/cm^2$
J_d	current due to dielectric polarization	$\mu A/cm^2$
J_l	leakage current	$\mu A/cm^2$
J_s	current due to domain switching	$\mu A/cm^2$
k	parameter in I-O model	
k_B	Boltzmann's constant	$8.61733 \times 10^{-5}\, eVK^{-1}$
κ	constant	
λ	wavelength of the X-ray	Å
m	positive constant	
m^*	effective carrier mass	kg
μ	carrier mobility	$cm^2/(V \cdot s)$
μ_n	mobility of electrons	$cm^2/(V \cdot s)$
μ_p	mobility of holes	$cm^2/(V \cdot s)$
n	diffraction order	
n	positive constant	
n	reflective index	
ν	rate constant	
P	polarization	$\mu C/cm^2$
P_P	polarization response to pulse P	$\mu C/cm^2$
P_U	polarization response to pulse U	$\mu C/cm^2$
P_N	polarization response to pulse N	$\mu C/cm^2$
P_D	polarization response to pulse D	$\mu C/cm^2$
P^n	the difference polarization response between pulse N and pulse D	$\mu C/cm^2$
P^p	the difference polarization response between pulse P and pulse U	$\mu C/cm^2$
P_r	remnant polarization	$\mu C/cm^2$
P_s	saturation polarization	$\mu C/cm^2$

$P^{\star}$	maximum displacement	$\mu C/cm^2$
ΔP	polarization change effected by the passing domain wall	$\mu C/cm^2$
q	elementary charge	$1.60218 \times 10^{-19}\, C$
q_x	reciprocal space along x-axis	Å^{-1}
q_z	reciprocal space along z-axis	Å^{-1}
R_p	parallel resistance	Ω
R_s	series resistance	Ω
R^*	critical radius of the bulge in domain motion	m
r_c	radius of nucleus	m
T	temperature	K or $^\circ$
T_0	transition temperature	K or $^\circ$
T_c	Curie temperature	K or $^\circ$
t_d	delay time	s
t_{dec}	period of voltage from 0 to $-V_{max}$	s
t_{inc}	period of voltage from 0 to $+V_{max}$	s
t_{int}	period between identical neighboring pulses	s
t_R	recombination time	s
t_r	period between opposite neighboring pulses	s
τ	density of recombination centers	
V	voltage	V
V_{ac}	alternating voltage	V
V_c	coercive voltage	V
V_{max}	maximum voltage applied on the capacitor	V
V_s	step change of voltage	V
Φ_M	electrode work function	eV
Φ_B	ferroelectric-electrode barrier	eV
$\Delta\Phi$	lowered amount of barrier	eV
χ	electron affinity	eV
ω	angle between the reflected ray and the scattering planes	$^\circ$
Y	admittance (reciprocal of impedance) in the parallel circuit	S

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General Introduction

The outstanding properties of ferroelectric materials such as polarization hysteresis, large dielectric constant and piezoelectric effect can all be applied in electronic devices. Among these applications, non-volatile memories utilizing the ferroelectric thin films have captured great attentions due to their potential low power consumption and high operation speed. To realize the large scale integration of ferroelectric thin-film memories, which are competitive with various current dynamic random access memories and static random access memories, a comprehensive study of ferroelectric thin-film capacitors has been carried out. Our study includes two parts: the fabrication of epitaxial ferroelectric thin-film capacitors; and effective electrical measurements for the understanding of leakage currents and switching dynamics. The structure of this thesis is described as follows:

Chapter 1 is dedicated to the background of ferroelectric materials, including: historical research, applications, principles of ferroelectricity, $Pb(Zr_{1-x},Ti_x)O_3$ (PZT) properties and the state-of-the-art of PZT deposition techniques. Then the motivation of this work is provided.

Chapter 2 introduces the two different deposition methods (sputtering and sol-gel) for PZT and patterning technique used for top electrodes. The routinely used electrical measurements (current-voltage, capacitance-voltage and ferroelectric hysteresis loop) are presented in details. In the last, the principle and procedures of PFM (piezoelectric force microscopy) measurement are introduced.

Chapter 3 describes the growth details of PZT capacitors by sputtering and sol-gel, respectively. The physical properties in terms of crystallinity and surface morphologies of each layer are shown here.

Chapter 4 compares the leakage current, relative permittivity and hysteresis loops of capacitors obtained from both deposition methods with different thicknesses and different top electrodes. Then the PFM results of these PZT films are provided.

Chapter 5 studies the electrical properties of PZT capacitors in details. Firstly, the frequency dependence of coercive field is investigated and the results is fitted according to different models. Secondly, the different contributions in a ferroelectric hysteresis loop are separated. Thirdly, hysteresis loop and capacitance results measured at various temperatures are presented. At last, the relaxation and imprint properties are shown.

Chapter 1

Background and Motivation

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1.1 Historical

The phenomenon of pyroelectricity, or the property of some materials, exhibiting a temperature dependent spontaneous electric dipole moment, was first recorded back to 314 BC. Theophratus noted that a stone, called *lyngourions* in Greek, could attract sawdust (Richards and Caley 1956). In the eighteenth and nineteenth centuries many experiments were carried out in an attempt to characterize the pyroelectric effect quantitatively. These studies eventually led to the discovery of piezoelectricity, which is the production of electrical polarization by application of stress, by J. Curie and P. Curie in 1880.

It was not until 1920 that J. Valasek recognized ferroelectricity by experiments (Valasek 1921). He discovered that Rochelle salt (first produced in about 1675, in La Rochelle, France) exhibited a spontaneously polarized phase which was similar to the already discovered ferromagnetism. An extremely large dielectric constant and piezoelectric response appeared near Curie temperature T_c. The term ferroelectricity was not commonly used before early 1940s because Rochelle salt had been the only ferroelectric material for more than one decade. The detailed crystal structure of Rochelle salt was unknown and seemed complicated. Between 1935 and 1938, a series of ferroelectrics were produced. Scientists discovered that the crystals that were isomorphous to potassium dihydrogen phosphate, KH_2PO_4 (KDP), seemed to show ferroelectricity below T_c. The only exception was ammonium salts, *e.g.*, $(NH_4)H_2PO_4$ (ADP), which was found to be antiferroelectric 20 years later. These newly discovered ferroelectric series exhibited a much simpler crystal structure, which facilitated theoretical understanding of ferroelectricity (Lines and Glass 2001).

After the discovery of KDP series, one decade passed without experimental breakthrough. It was thought that a hydrogen bond was prerequisite for a ferroelectric. However ferroelectricity was found in barium titanate $BaTiO_3$ (BTO) (Wul and Goldman 1945). The discovery was important to the study on ferroelectricity for: 1) BTO was a ferroelectric without hydrogen bonds; 2) the crystal structure was perovskite with very high symmetry and had only 5 atoms per unit cell; 3) it was chemically and physically stable; 4) it exhibited ferroelectricity at room temperature; 5) BTO was among the largest single class of all ferroelectrics−the oxygen octahedral ferroelectrics made up from basic BO_6 building blocks (von Hippel 1950, Kwei *et al.* 1993, Scott 2007). Owing to its exceptional properties, BTO had been the most investigated ferroelectric material for decades. Later ferroelectric behavior was found in $KNbO_3$, $KTaO_3$ (Matthias 1949), and in $LiTaO_3$, $LiCbO_3$ (Matthias and Remeika 1949) and in $PbTiO_3$ (Shirane *et al.* 1950).

In the mid-fifties of last century, $C(NH_2)Al(SO_4)\cdot 6H_2O$ (GASH) was found to be ferroelectric. Its isomorphs were found to be ferroelectrics soon though T_c was not observed since they decomposed before phase transition. Soon the number of discovered ferroelectrics passed 100 (Lines and Glass 2001). In the 1950s demand for high-capacity computer memories emerged and ferroelectrics seemed to be prime candidates for their bistable polarization used for binary memories. However the problems of reliability and fatigue hampered their application. Eventually magnetic and semiconductor memories were favored.

In 1960s and 1970s, intense studies on ferroelectrics were carried out. During the second half of the 1960s, a large number of new ferroelectrics were discovered. Application of these materials for optical devices evolved. At the same period, since the progress in integrated Si devices advanced, interest of using ferroelectric thin films for non-volatile memories emerged.

In 1980s, processing of complex ferroelectric oxides advanced as sol-gel-derived thin ferroelectric film was achieved (Blum and Gurkovich 1985, Dey *et al.* 1987). In 1987, ferroelectric memory integrated with silicon complementary metal-oxide semiconductor (CMOS) was demonstrated (Eaton *et al.* 1988).

Considerable interest was given to ferroelectrics in 1990s. The possibility of using ferroelectric thin films as nonvolatile memories and new microelectromechanical systems (MEMS) attracted significant interest. However, problems of fatigue and aging hindered its development for memories but piezoelectric MEMS had been in mass production for a variety of devices.

Now the known ferroelectrics are more than 1000, many of which are neither hydrogen bonded nor oxides (Izyumskaya *et al.* 2007, Scott 2007). In the beginning of this new century, miniaturization has been an essential method to increase the performance of single crystal ferroelectric thin film. First-principle has helped further understand ferroelectric properties (Meyer and Vanderbilt 2002, Diéguez *et al.* 2004).

In recent years, interests of designing innovative electronic devices based on coupling between ferroic orders emerged. Ferroelectricity can be utilized to modulate magnetic properties like: controlling the Curie temperature across an interface; turning magnetism on and off; altering the spin polarization of

electrons and changing exchange coupling between magnetic layers (Kanki *et al.* 2006, Bibes 2012). Bismuth ferrite, $BiFeO_3$ (BFO) has captured a significant amount of attention for its exceptional properties. So far, BFO is the only potential candidate that exhibits both antimagnetism with a Néel temperature of 640 K and strong ferroelectricity up to 1100 K. The structure of magnetoelectric random access memories (MERAMs) is demonstrated (Bibes and Barthélémy 2008), which can store 4 logic states per unit. Besides, energy harvester based on the piezoelectricity attracts many interests in recent years (Bowen *et al.* 2014).

1.2 Applications

Since the discovery of ferroelectricity in Rochelle salt, the research on ferroelectrics has been closely linked to device applications. Rochelle salt was widely used for microphones for its largest piezoelectric effect at that time. In 1940s, Rochelle salt was employed as sound transducer (transfers sound pressure into electrical charges) for submarine sonar systems but then was replaced by the more stable ADP (Massa 1989) during World War II. Since its discovery, it seemed to be a perfect candidate for computer memory elements. A polarization of 10 $\mu C/cm^2$ corresponds to $\sim 10^{14}$ electrons/cm^2, so in principle a high density storage with high signal-to-noise ratio could be achieved. The potential of this device was not realized for its short-term fatigue, less well-defined coercive field and a hysteresis loop with not sufficient square shape (Scott and Paz de Araujo 1989, Uchino 2000). In 1960s, a burst of activity accompanied the discovery of a large amount of ferroelectrics. During this period, the development of ferroelectric as memories, optical devices and thermal detectors steadily increased (Lines and Glass 2001). In 1970s, transparent ceramics were developed which offered possible electro-optic applications. Study on single crystals emerged in this period but devices were still limited to bulk ceramics for their much lower costs. From 1984, when ferroelectric thin films were fabricated and integrated into semiconductor chips, research started focusing on thin film ferroelectrics (Scott 2007). In late 1980s, development of ferroelectric random access memories started. Ferroelectric random access memory (FeRAM) has been commercialized since late 1990s but remains a relatively small part of the overall semiconductor market. The problem of fatigue and imprint hinders it from replacing dynamic random access memory (DRAM) although FeRAM exhibits lower power consumption and theoretical faster read/write period (Ishiwara *et al.* 2004). Another type of ferroelectric memory is metal ferroelectric semiconductor field effect transistor (MFSFET), which was proposed before the conventional capacitor-type memory. As the polarization of the ferroelectric changes, the drain current differs which can be used as binary states of a memory unit. Comparing to FeRAM, the "read" operation is non-destructive, but the fabrication cost is higher.

The major application of ferroelectrics is for capacitors, utilizing their high dielectric constants around the curie temperature. Recently, since conventional Si micro-machining technology coupled with silicon oxide and metal, is limited in its ability to produce fine-scale capacitors, ferroelectric seems to be a better alternative and draws a lot attention (Ishiwara *et al.* 2004). Energy harvesting is also a topic

Table 1.1: Applications of ferroelectric materials.

Ferroelectricity	Pyroelectricity	Piezoelectricity	Electro-optical properties
FeRAM	Infrared detector	Microphone	Picture memory device
MFSFET	Temperature sensor	Sonar	Eye protection application
	Infrared image sensor	Pressure sensor	Waveguide modulator
	Impedance amplifier	Accelerometer	Variable optical attenuator
		Gyroscope	Polarization controller
		Vibrator	Tunable optical filter
		Ultrasonic transducer	
		Resonator	
		Surface acoustic wave device	
		Transformer	
		Actuator	
		Ultrasonic motor	
		Energy harvester	

of intense interest since it provides a route for the realization of autonomous and self-powered low-power electronic devices, *e.g.*, wireless sensor networks. Most energy harvesters transform mechanical energy to electric power using piezoelectricity of the material. The use of pyroelectric materials to generate electrical energy from temperature fluctuations is also a research topic (Bowen *et al.* 2014).

Since all ferroelectrics are pyroelectrics and all pyroelectrics are piezoelectrics, ferroelectrics can be employed in devices using their different properties. Ferroelectrics have also received intense interest due to their high optical transparency and remarkable optical nonlinearity for photonic devices. Table 1.1 lists the devices which use ferroelectrics as the major functioning parts (Haertling 1999, Uchino 2000, Lines and Glass 2001, Ishiwara *et al.* 2004, Setter *et al.* 2006a).

FeRAM

Over the past two decades, FeRAM has evolved from a concept to a commercial memory product used in a variety of consumer and industrial applications, *e.g.*, smart cards, power meters, printers and video games. Compared to other types of nonvolatile memory, such as electrically erasable read-only memory (EEPROM) and battery-backed static random access memory (SRAM), FeRAM exhibits low power consumption, high read/write endurance, fast read-write access and long-term retention (Ishiwara *et al.* 2004). The first FeRAM was invented in 1988 using PZT. The FeRAM cell consisted of two transistors and two capacitors (2T–2C). Most commercial FeRAM devices currently available employ a 2T–2C cell with a 0.5 μm minimum CMOS feature size. The large cell factor (110) for a 2T–2C device can be reduced by changing the architecture to 1T–1C type. With this change the reference cell is excluded from unit cell in 1T–1C and a single reference cell is used for the entire memory. The quality requirement in terms of switchable polarization, retention and cycling endurance is higher in 1T–1C than

Table 1.2: The roadmap for 1T-1C FeRAM memory and target requirements (Ishiwara *et al.* 2004).

Generation (μm)	0.5 (current)	0.35	0.25	0.18	0.13	0.1
Architecture	2T-2C	1T-1C	1T-1C	1T-1C	1T-1C	1T-1C (3D)
Density (Mb)	1	16	64	256	512	2000
PZT thickness (nm)	200	180	140	100	80	65
Capacitor area (μm^2)	3.0	$1.5 \sim 1.0$	$1.0 \sim 0.5$	$0.33 \sim 0.13$	$0.14 \sim 0.07$	$0.06 \sim 0.03$
Cell factor	63	$63 \sim 30$	$30 \sim 15$	$20 \sim 8$	$16 \sim 8$	$12 \sim 6$
Cell size (μm^2)	15.8	$8.0 \sim 3.7$	$1.9 \sim 0.9$	$0.65 \sim 0.26$	$0.27 \sim 0.14$	$0.12 \sim 0.06$
Operating voltage (V)	5/3.3	3.3	2.5	1.8	1.5	1.2
Read/write (cycles)	$10^{10}/10^{16}$	10^{16}	10^{16}	10^{16}	10^{16}	10^{17}
Data retention (yr)	10	10	10	10	10	10
Switching time (ns)	<10	<10	<10	<10	<5	<5
Access time (ns)	70	50	30	20	15	10
Active current (mA)	<15	<15	<15	<15	<15	<15
Energy/bit (pJ)	2.3/1.4	0.68	0.19	0.04	0.02	0.02

in 2T–2C. Additional decrease in cell factor can be achieved by building the capacitor on top of a plug which contacts an underlying access-control transistor (Ishiwara *et al.* 2004). Table 1.2 lists the road map for 1T–1C FeRAM and the requirements for feature sizes down to 0.1 μm.

MEMS

Kinetic energy can be harvested by MEMS through piezoelectricity. Figure 1.1 demonstrates a cantilever generator. When the cantilever deflects due to external vibrations (*e.g.,* shaking), charges are generated by the ferroelectric film.

There is a lot of interest in developing human-powered energy-harvesting devices. Studies has shown that a 68 kg man walking at 3.5 mph can produce 67 W power (Fischer 1987). Although not all this energy can be harvested, a group at MIT put a PZT generator in an insole gathering 8.4 mW. Boeing is developing seats for its airplanes that could harvest the motion of passengers. This energy could be used to power the outlets for laptops and cellphones (Carter and Norton 2013).

An advantage of piezoelectric generators is that they are scalable: they can be combined to generate more power and also can be scaled down even to nano-scale to create localized power sources. The performance of energy harvesting is directly related to the piezoelectric coefficients, but the applied stress or strain is also an important factor. The energy output depends on the ability of the piezoelectric material to sustain an applied force or to repeatedly undergo a recoverable strain. The limits in the strength and elasticity of these materials may be the dominant factors in performance rather than piezoelectric coefficients (Starner and Paradiso 2004).

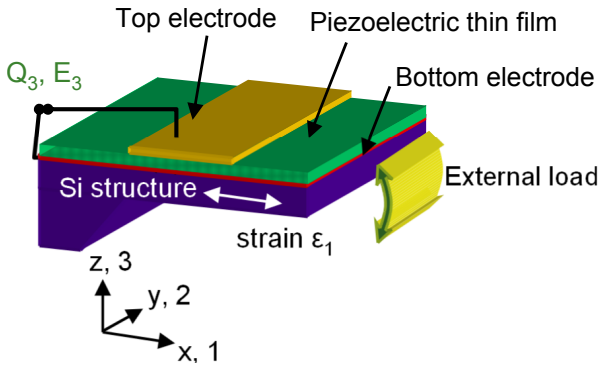

Figure 1.1: Schematic of piezoelectric cantilever vibration harvester (Muralt 2004).

1.3 Ferroelectricity

Ferroelectricity originates from the asymmetricity of crystals. There are 32 crystal classes and 11 of them possess a center of symmetry, which exhibit no polar properties. If a uniform stress is applied to these 11 classes of centrosymmetric crystals, the resulting small movement of charge is symmetrically distributed in a manner that relative displacements are fully compensated. Of the remaining 21 non-centrosymmetric classes, all except one exhibit electrical polarity when subject to stress. The effect (and also its converse, the production of strain by application of an electric field) is linear, with reversal of the response under reversal of the stimulus, and is termed piezoelectric effect. Of the 20 piezoelectric classes, 10 are pyroelectric. They possess a spontaneous polarization under certain temperatures. The amplitude of the dipole moment varies when temperature changes. Among pyroelectric crystals, ferroelectrics can be distinguished for the fact that they possess permanent polarization in the absence of electric field and the polarization can shift from one state to another by electric field (when it is sufficient large).

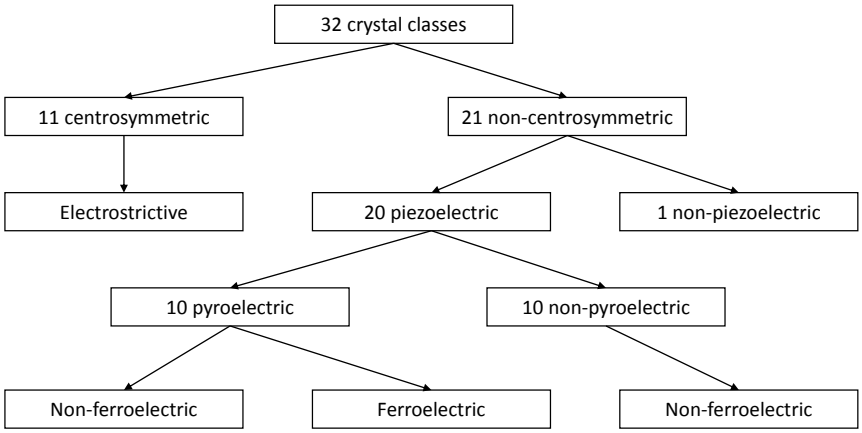

Figure 1.2: Grouping of crystal classes (Defaÿ 2013).

Figure 1.3 shows the displacement in pyroelectrics, ferroelectrics and antiferroelectrics. A pyroelectric displacement is independent on external field, but only on temperature. Ferroelectric shows a irreversible displacement which remains after the applied field is removed when $T < T_c$. Antiferroelectric has neighboring lines of ions displaced in opposite directions when $T < T_c$ and shows no remnant

polarization when the applied field is removed.

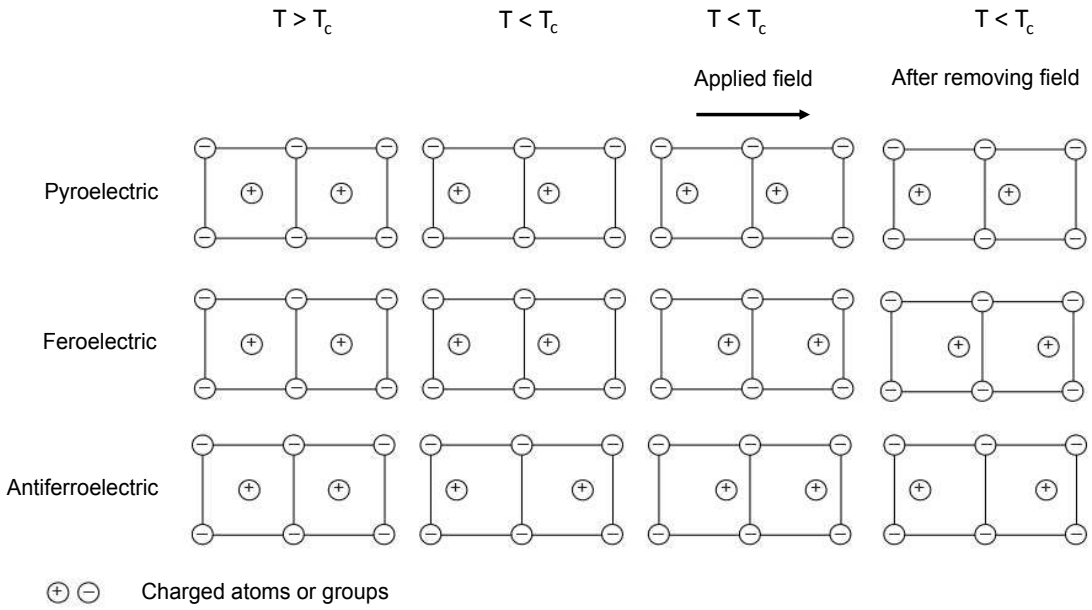

Figure 1.3: Schematic representation of structural phase transition and dipole movement in response to field of pyroelectrics, ferroelectrics and antiferroelectrics. Image adapted from Kittel (2004).

The ferroelectricity of ABO_3 type perovskite-crystals origin from B-site ion shift. Figure 1.4 shows the crystalline structure of $Pb(Zr_{1-x},Ti_x)O_3$ (PZT). Above Curie temperature T_c, PZT is paraelectric (polarized under field and removal of field resulting in zero polarization) and the crystal is cubic. B-site ions are in the center of the lattice and the polarization is zero. Below T_c, PZT lattice is tetragonal. B-site ions have two stable locations, either slightly above the center or below it. If dipoles in all lattices are in the same direction, the material shows a polarization of the same direction. When this polarized PZT is subject to a sufficient antiparellel electric field, the dipoles will be forced to change direction. The shift of B-site ions between the two stable states is the origin of the ferroelectricity in perovskite ferroelectrics.

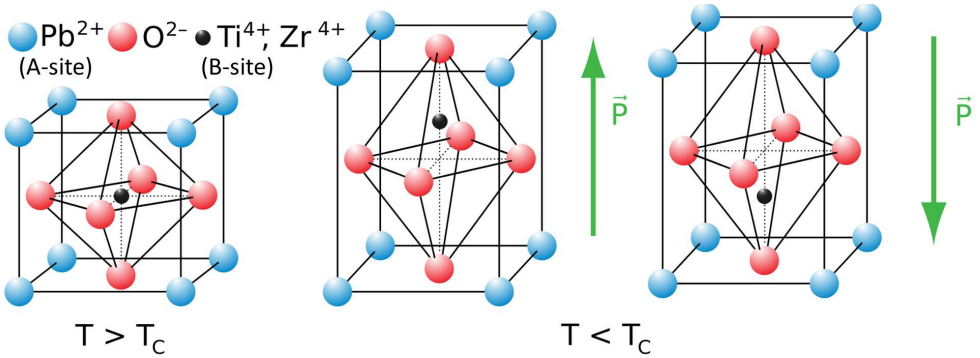

Figure 1.4: Schematic of PZT crystalline lattice and the origin of permanent dipole in tetragonal lattice. Image adapted from Wikipedia (2010).

Landau-Ginzburg-Devonshire Theory

The behavior of ferroelectrics is often modeled by free energy. In Landau-Ginzburg-Devonshire theory, the free energy F can be expanded in a power series (Kittel 2004):

$$F(P;T,E) = -EP + g_0 + \frac{1}{2}g_2P^2 + \frac{1}{4}g_4P^4 + \frac{1}{6}g_6P^6 + \cdots \tag{1.1}$$

where the coefficients g_n are temperature dependent, T is temperature in K and E is external electric field. Odd powers are not included due to the symmetry reason. The value of P in thermal equilibrium condition is given by the minimum of F. At applied electric field E, the equilibrium polarization satisfies the condition:

$$\frac{\partial F}{\partial P} = -E + g_2P + g_4P^3 + g_6P^5 + \cdots \tag{1.2}$$

To obtain a ferroelectric state we must suppose that g_2 passes through zero at some temperature T_0:

$$g_2 = \gamma(T - T_0) \tag{1.3}$$

γ is a positive constant, which equals to $1/\varepsilon_0 C_{CW}$. ε_0 is permittivity of free space ($8.85419 \times 10^{-12}\, F/m$) and C_{CW} is Curie-Weiss constant.

Second-order Transition

If g_4 is positive, g_6P^5 and higher order terms can be neglected. When $E = 0$, it is found:

$$\gamma(T - T_0)P_s + g_4P_s^3 = 0 \tag{1.4}$$

So either $P_s = 0$ or $P_s^2 = (\gamma/g_4)(T_0 - T)$. For $T \geq T_0$, $P_s = 0$. T_0 here equals Curie temperature T_c. For $T < T_0$, the minimum free energy F in zero field is at:

$$|P_s| = (\gamma/g_4)^{1/2}(T_0 - T)^{1/2} \tag{1.5}$$

The phase transition schema is plotted in Figure 1.5. The transition is a second-order transition because P goes continuously to 0 at T_0. The order of transition in PZT depends on its composition (Haun *et al.* 1989).

First-order Transition

If g_4 is negative, the transition is first order and P_s goes to 0 abruptly. g_6 is retained and taken as positive. Otherwise, F will go to minus infinity. The equilibrium condition for $E = 0$ is given by

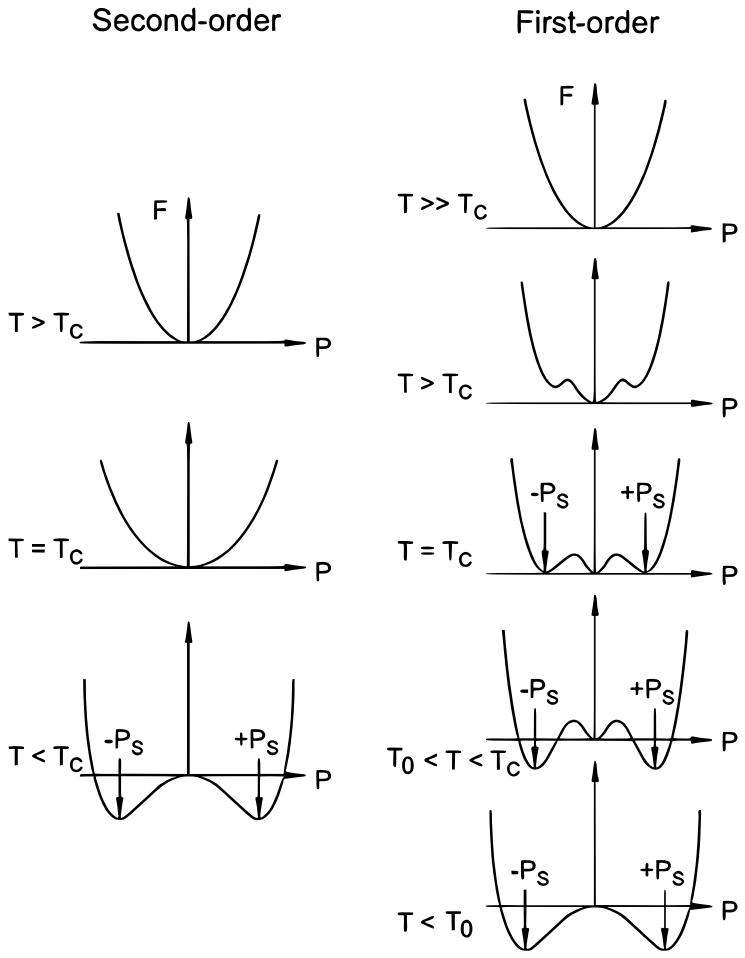

Figure 1.5: Free energy for second-order and first-order phase transition (Kittel 2004).

Equation (1.2):

$$\gamma(T - T_0)P_s - |g_4|P_s^3 + g_6P_s^5 = 0 \tag{1.6}$$

So either $P_s = 0$ or

$$\gamma(T - T_0)P_s - |g_4|P_s^32 + g_6P_s^4 = 0 \tag{1.7}$$

Curie temperature T_c is related to T_0 by:

$$T_c = T_0 + \frac{3}{16}\frac{g_4^2}{\gamma g_6} \tag{1.8}$$

This indicates that when $T_0 < T < T_c$, there will still be two stable polarization states. The transition is plotted in Figure 1.5.

The double well potential is entirely consistent with the hysteresis behavior of ferroelectrics. Figure 1.6 illustrates the connection between ferroelectric switching and double-well potential. Starting from the state polarized downward, which is corresponding to the state that polarization in the left side of the double-well potential. When a positive field is applied to the ferroelectric, the right side of the double well deepens and the left side becomes shallower. As the field increase to an amount large enough, the barrier between the two wells disappears and the polarization switches to the up state. A larger field will cause the right side deepens and left side shallower, and polarization increases. The amount of polarization will reach a saturated value as field continues increasing.

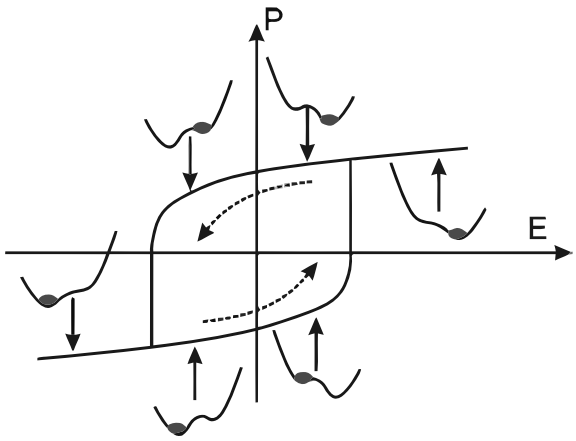

Figure 1.6: The ferroelectric hysteresis loop, associated with potential subject to an applied field (Callori 2013).

1.4 PZT Properties

Lead zirconate titanate $Pb(Zr_{1-x},Ti_x)O_3$ (PZT) is a solid solution whose crystalline structure and properties varies with the ratio of $PbZrO_3$ and $PbTiO_3$. $PbTiO_3$ undergoes a first-order phase transition from cubic paraelectric phase to tetragonal ferroelectric phase as temperature decreases passing 490 °C. At room temperature: $a = b = 3.904$ Å, $c = 4.152$ Å (Iijima *et al.* 1986). $PbZrO_3$ is antiferroelectric. At room temperature $PbZrO_3$ is orthorhombic with lattice parameters: $a = 5.886$ Å, $b = 11.749$ Å and $c = 8.248$ Å (Kong *et al.* 2001). T_c is 230 °C, at which temperature a transition from cubic paraelectric phase to orthorhombic antiferroelectric phase occurs. Figure 1.7 shows the phase diagram of PZT solid solution, first obtained by Jaffe *et al.* (1971). Above T_c, PZT is cubic over the whole range of compositions. Below T_c, PZT in Ti-rich region is tetragonal and in Zr-rich region is rhombohedral (two phases HT and LT, depending on the temperature). When x is close to 1, there is a region in which PZT is orthorhombic and the solid solution is antiferroelectric.

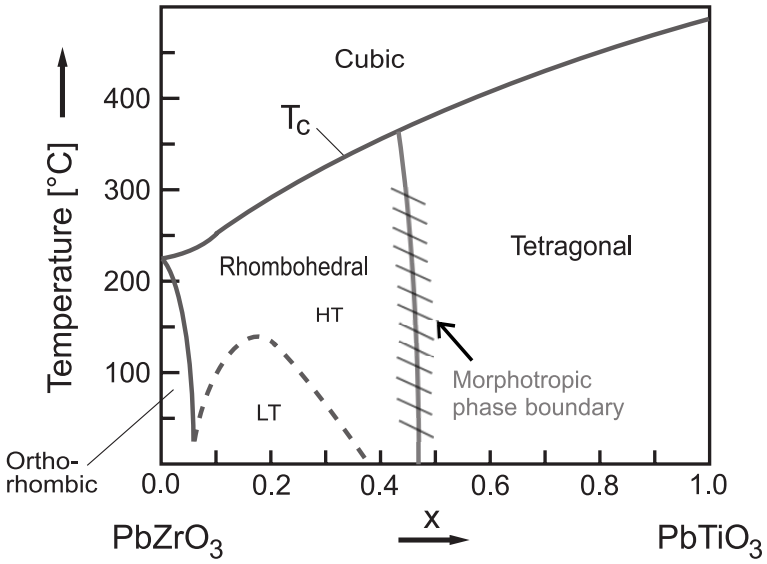

Figure 1.7: Phase diagram of PZT. Strokes denote the MPB. Image adapted from Waser *et al.* (2006).

The most prominent feature of the phase diagram is the existence of "morphotropic phase boundaries" (MPB). In the vicinity of this region, the crystal structure changes abruptly with dielectric constant and electromechanical coupling coefficient becoming maximum. Figure 1.8 shows the dielectric constant and coupling coefficient of PZT as a function of Zr/Ti ratio. The reason why PZT of this composition shows excellent dielectric response and high electromechanical coupling coefficient has not been fully understood. In tetragonal $PbTiO_3$, there are 6 possible domain states from $< 100 >$ direction and in rhombohedral $PbZrO_3$, there are 8 possible domain states from $< 111 >$ direction. All these 14 possible domain states are equally favorable energetically. The enhanced properties near MPB was attributed to this large amount of possible polarization direction (Damjanovic and Demartin 1997, Hoffmann *et al.* 2001). However, the apparent continuous phase transitions through the MPB region from tetragonal to rhombohedral are not allowed by symmetry. High resolution of X-ray powder diffraction on homogeneous

sample of high quality revealed that a narrow stripe of monoclinic phase existed between tetragonal and rhombohedral phases (Noheda *et al.* 2000ab). Thus in the MPB region, the transition from tetragonal to rhombohedral phase is mediated by a monoclinic phase acting as a "bridge". Close to the MPB, the piezoelectric elongation of the unit cell occurs along the directions associated with the monoclinic distortion instead of the rhombohedral and tetragonal polar directions, indicating the high dielectric property arises from the monoclinic phase (Guo *et al.* 2000). The width of the MPB stripe is not well defined because of the difficulty in preparing samples of high compositional homogeneity.

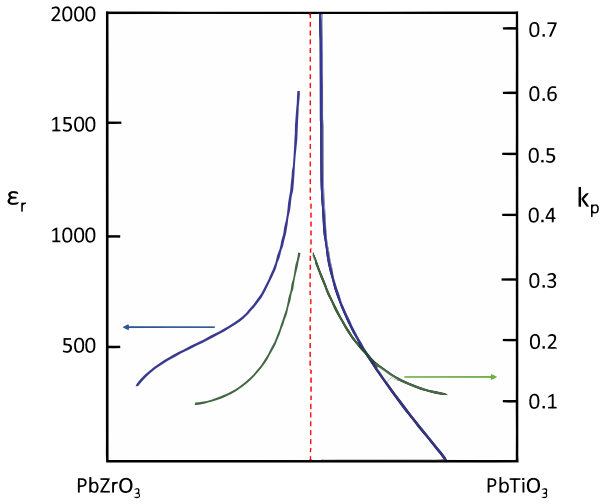

Figure 1.8: Dielectric constant and electromechanical coupling coefficient of PZT as a function of Zr/Ti ratio. Image adapted from Carter and Norton (2013).

Ahart *et al.* (2008) showed that even a pure compound ($PbTiO_3$) could display a MPB under pressure ($10 \sim 20\ GPa$). In the MPB region, large piezoelectric effects were also observed. Their first-principle calculations were consistent with the experimental results. According to their study even at room pressure a pure compound with MPB-like behavior maybe exist, which would lead to great advances in electromechanical applications.

Choice of PZT(52/48)

For the fabrication of FeRAM, many ferroelectric materials have been investigated, among which PZT and $SrBi_2Ta_2O_9$ are the two main materials studied for their high remnant polarization and low coercive field (Kingon 1999, Scott 2000, Schwarzkopf and Fornari 2006). Although PZT is in commercial production, both materials have disadvantages which have limited their evolutions into mass productions. For PZT, the main problem is fatigue for capacitors with common platinum electrodes. However, this problem has been greatly eased by using oxide electrodes such as IrO_2, RuO_2 and $SrRuO_3$ (Asano *et al.* 2003, Masuda and Nozaka 2003). SBT does not show any fatigue phenomenon up to 10^{13} cycles (Scott 2000). SBT also has a lower coercive field, which enables an lower operating voltage. But the high process temperature (about 750 °C) for SBT makes it difficult to process in conjunction with silicon devices (Park *et al.* 1999). And the crystallization temperature for PZT is less than 650 °C, making it

possible for implementing PZT capacitors on CMOS logic circuits.

The phase of $Pb(Zr_{1-x},Ti_x)O_3$ varies with its composition and its properties change accordingly. The polarization direction of a rhombohedral phase PZT ($x < 0.48$) is neither perpendicular to the plane, nor parallel to the plane, making it not practical for memory use. When x varies from 0.48 to 1, PZT phase changes from MPB to tetragonal and remnant polarization increases from 30 $\mu C/cm^2$ to 55 $\mu C/cm^2$, accordingly. However, coercive field increases noticeably, making low operating voltage more difficult (Foster *et al.* 1997). Thus we chose PZT(52/48) for its sufficient remnant polarization and low coercive field. INL is involved in projects employing PZT for MEMS as sensors and energy harvesters and PZT(52/48) has an outstanding piezoelectric coefficient compared to other compositions.

Polycrystalline vs Epitaxial

Before 2000 due to technical limitations, most studies on PZT thin films concentrated on its polycrystalline phase and now most research works are dedicated to monocrystalline phase for its superior polarization, higher piezoelectric coefficient and better interface with substrate. Since polycrystalline films usually consist of randomly-oriented crystalline grains, they must be poled in order to preferentially orient the ferroelectric polar domains (Ramesh 1997). As monocrystalline phase has all the domains appropriately-oriented, its ferroelectric, pyroelectric and piezoelectric response are all better than that of polycrystalline PZT. Monocrystalline phase exhibits high macroscopic uniformity, which makes miniaturization of devices possible.

Polycrystalline film contains many grains of usually different orientations. Grain boundaries are formed between grains. Compared to monocrystalline phase, which possesses no grain boundaries, the leakage current increases several orders of magnitude and the fatigue endurance and breakdown voltage are reduced (Lee and Joo 2002). The polycrystalline PZT films is reported to show a non-square hysteresis loops, in which the coercive field was not well defined. This implies that a higher operating voltage is required (Setter *et al.* 2006b).

If PZT film is deposited on a substrate with small lattice mismatch, epitaxial growth can be achieved. Since it is monocrystalline, grain boundaries are avoided and its ferroelectric properties are improved due to the single orientation of almost all domains. TEM (transmission electron microscopy) observation has also revealed that contrary to polycrystalline film the interface between the epitaxial PZT layer and the underlying layer is clean and flat; no obvious diffusion between these two layers was observed (Scott 2000). If the in-plane lattice parameter of substrate is slightly smaller than that of PZT, the increased tetragonality (for tetragonal PZT, $x > 0.48$) is enhanced by the clamping force from the substrate, thus improving its ferroelectric performance.

Based on these information, our aim is to grow epitaxial PZT(52/48) capacitors.

1.5 PZT Deposition: State of the Art

For the deposition of PZT thin films, a variety of techniques are employed, like sol-gel, sputtering, pulsed laser deposition (PLD), metal-organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) (Izyumskaya *et al.* 2007). Of them, sol-gel, sputtering and PLD are the three most studied methods for PZT growth.

Sol-gel

Sol-gel is the most employed PZT deposition method for its simple procedure, low cost and large step coverage and good composition control. Before 1990, most sol-gel-derived PZT films were polycrystalline. Talin *et al.* (2002) demonstrated deposition of epitaxial PZT(52/48) films on STO/Si with extremely smooth and highly ordered surfaces. Gong *et al.* (2004) epitaxially deposited Nb-doped PZT(60/40)(001) on Nb-doped STO(001) and PZT(60/40)(111) on STO(111). Square-like hysteresis loops were obtained and the remnant polarization of these two films were 72 $\mu C/cm^2$ and 66 $\mu C/cm^2$, respectively. The coercive field were 64 kV/cm and 41 kV/cm, respectively.

Several routes have been proposed to improve the film quality. Meng *et al.* (2000) replaced Zr-alkoxides with zirconium nitrate, to reduce the relative content of organics in the precursor solution. By modifying the solution, the shrinkage of the film reduced during the thermal treatment, thus reducing the formation of cracks. The coercive field was as low as 45 kV/cm but the remnant polarization was only 11 $\mu C/cm^2$.

Some efforts have been given to lower the process temperature. Perez (2004) demonstrated that at 500 °C, PZT(52/48) was crystallized by distilling the Pb precursor multiple times after dissolving in 2-methoxyethanol and increasing the drying temperature. This procedure provided high chemical homogeneity, thus increasing crystallinity. The remnant polarization and coercive field were 30 $\mu C/cm^2$ and 60 kV/cm, respectively.

Wu *et al.* (2006) reported that by adding perovskite PZT nanopowders as seeds into precursor solution, the post annealing could be performed either at lower temperature or for shorter period. The seeded film showed relatively higher crystallinity than unseeded films.

Thick PZT film, prepared by multiple spin coating and annealing processes, often show an oscillating chemical profile. Calame and Muralt (2007) demonstrated that by using gradient-composition solutions for different spin coating layers for compensation, an almost gradient-free 2-μm-thick film was obtained. Its piezoelectric coefficient was larger than the gradient counterpart.

Sputtering

Sputtering has been successful using elemental and alloy targets for the deposition of ferroelectric materials. Usually the deposition rate is low (< 5 nm/min). In recent years, sputtering for PZT has focused on epitaxial growth as well as coverage of large areas.

Through an off-axis magnetron sputtering, Gariglio *et al.* (2007) deposited 15-nm-thick totally strained PZT(20/80) film on Nb-doped STO substrate. He also found that when the film thickness exceeded 80 nm, it turned to be relaxed. By using a 12-inch ceramic PZT target, Masuda *et al.* (2001) achieved depositing PZT on a 6-inch substrate. Film thickness and Pb content uniformity showed very low variations.

By controlling O_2/Ar ratio and heating rate in post annealing, highly oriented (111) and (100) PZT films have been achieved on Pt/Ti/SiO_2/Si by Kalpat and Uchino (2001). PZT(111) showed a remnant polarization of 25 $\mu C/cm^2$ and coercive field of 65 kV/cm while for PZT(100), the corresponding results were 20 $\mu C/cm^2$ and 35 kV/cm.

When PZT thickness exceeds $\sim$ 30 nm, it will relax on substrate (Gariglio *et al.* 2007), which will reduce the ferroelectric properties since the tetragonality decreases. Callori (2013) demonstrated a method to keep PZT strained on substrate by depositing $PbTiO_3$/$SrRuO_3$ superlattice structure. This ferroelectric of more than 100 nm could remain strained on substrate. However the hysteresis loops were not square and the remnant polarization was only 20 $\mu C/cm^2$, less than that of recently reported $PbTiO_3$ films (Izyumskaya *et al.* 2007).

PLD

PLD have been intensely investigated for its capacity of growing high quality epitaxial PZT films in recent years. To increase the uniformity, a rotating target and oblique angle of incidence are often employed. The most promising characteristics of PLD for oxide growth are little difference between the film and ceramic target. In addition, high oxygen gas pressure is feasible during growth, which can suppress oxygen vacancies produced due to the volatility of lead in the form of PbO (Izyumskaya *et al.* 2007).

Pintilie *et al.* (2007) reported high quality epitaxial PZT(20/80) films deposited on $SrRuO_3$. Square-like hysteresis loops were obtained with remnant polarization as high as 105 $\mu m/cm^2$.

Usually, the coverage of PLD is very poor due to the form of the plume. Nguyen *et al.* (2011) reported a PZT deposition on a 4-inch silicon-on-insulator (SOI) wafer. The thickness variation was less than 5%.

Vrejoiu *et al.* (2007) succeeded in depositing PZT(40/60)/PZT(60/40) superlattices on SRO/STO. The PZT of $\sim$ 175 nm exhibited a high remnant polarization of 50 $\mu C/cm^2$.

Lee *et al.* (2008) demonstrated by using ultrathin anodic aluminum oxide masks, arrays of individually addressable PZT(20/80) nanocapacitors with a density of 176 $Gb/inch^2$ were achieved on Pt/MgO substrates. Retention measurements showed that these nanocapacitors ensured long-term stability of polarization for more than 74 h.

1.6 Motivation

FeRAM-based devices have the potential to capture the majority of the non-volatile memory market, as well as to penetrate SRAM and DRAM markets. The fabrication of ***electrode***/***ferroelectric***/***electrode*** capacitor was studied in this work, which is the key component of FeRAM. PZT was chosen for its superior ferroelectric property and high T_c even though lead is not environment-friendly (other materials will be studied in future work). As low power consumption is a merit for mass application, PZT thickness in this work was limited to less than 200 nm to lower operating voltage.

Two deposition techniques were employed to fabricate PZT thin film of the same composition for comparison. Sol-gel deposition is more mature with relatively simple process and a low cost. Sputtering offers better homogeneity and large coverage. By varying the deposition parameters, the quality of sputtered film can be precisely controlled. Since the crystalline quality of ferroelectric film greatly influences capacitor properties, great attention was paid to the film growth procedure.

The purpose of this work is to fabricate state-of-the-art PZT capacitors as thin as possible with high qualities in terms of good crystallinity, low coercive voltage, stable spontaneous polarization, low relaxation, high retention, good fatigue performance and no imprint and to build an effective electrical characterization techniques to investigate switching dynamics and leakage current. After the optimization of epitaxial PZT growth on bulk STO, the whole technique can be transfered to Si substrate with STO buffer layer in order to adapt the silicon-based platform. The composition of PZT(52/48) was chosen also for the future study of MEMS for its outstanding piezoelectric coefficient.

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Chapter 2

Experimental Techniques

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In this chapter, two film growth techniques employed in this work, sputtering and sol-gel, will be presented firstly. The principles of characterization for structural, morphological and electrical properties will be introduced then.

2.1 Film Growth Techniques

Two different deposition routes were employed for the fabrication of ferroelectric PZT capacitors. And a lift-off process was used for the deposition of top electrode. In this section, these three techniques will be presented.

2.1.1 Sputtering

Vacuum based thin film deposition technologies can be classified into two major categories: physical vapor deposition (PVD) and chemical vapor deposition (CVD). In PVD techniques, single atom or small

clusters occur on the substrate surface independently of the source process. In CVD techniques, molecular species chemically react at the substrate surface resulting in a condensed film as well as the emission of volatile by-products (Powell and Rossnagel 1999).

Sputtering "knocks off" the material to be sputtered via high energy, ionized atoms. Physical sputtering is driven by energy and momentum exchange between ions and atoms in the target. Figure 2.1 illustrates the process of sputtering. Positively charged ions (usually ionized inert gas such as Ar^{+}) from plasma are accelerated by the electrical field superimposed on the target and strike on the target. During the collision, the kinetic energy and momentum of the ions transfers and distributes among many atoms in the target. A small fraction of target atoms/ions are dislodged as part of the collision chain. Sputtered target atoms travel to the substrate which is usually several *cm* away and adhere to it, forming a thin film. The bombardment of the cathode with ions caused emission of secondary electrons, which are then accelerated toward the anode and gain enough energy to ionize more gas atoms.

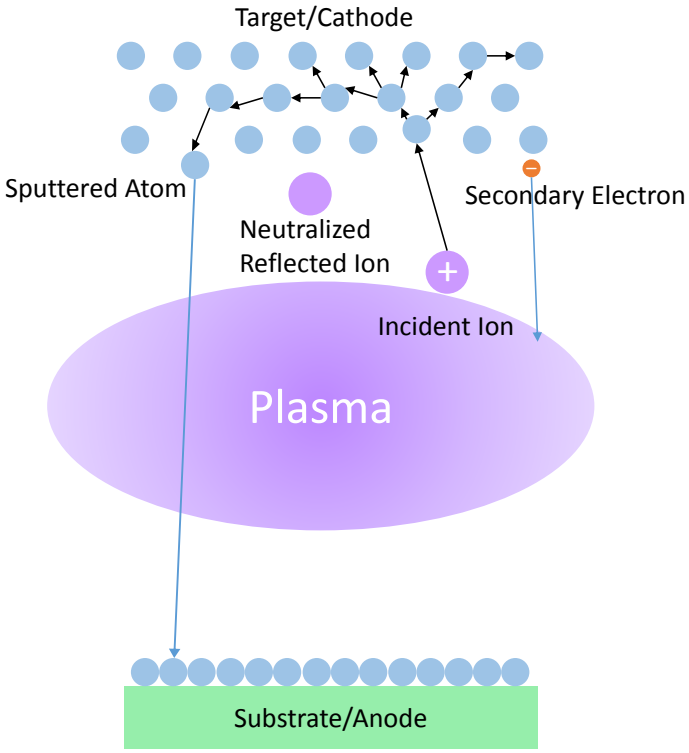

Figure 2.1: Schematic of sputtering process.

DC (direct current) plasma is used for conductive material deposition. Ions are neutralized after gaining electrons from the cathode. To produce highly insulating oxides, RF (radio frequency) power is applied to avoid the build-up charges on the insulative target surfaces, which lowers the deposition rate. Compared with DC powered sputtering, RF sputtering increases the deposition rate (as well as for conductive material deposition), lowers the required voltage and is compatible with the use of reactive gas, such as oxygen. 13.56 MHz is the most commonly used frequency for commercial sputtering application. Sputtering sources often utilize magnetron to confine charged plasma particles near the target. This

can enhance both the efficiency of initial ionization process and allowing a plasma to be generated at lower pressures (Rossnagel *et al.* 1998). In this work, *Alliance Concept AC450* sputtering machine in RF magnetron mode was employed for both PZT and electrode growth.

The advantages of sputtering deposition are (Mattox 2010):

- Ability to deposit a wide variety of metals, insulators, alloys and composites. Especially practical for materials with high melting points.
- Large area coverage (the cost of large target can be high, overlapping mosaic tiles, rods can replace single planar target).
- High step coverage.
- Reproducible deposition control.
- In-situ cleaning of substrate by reversing the potential.

And the disadvantages of sputtering deposition are:

- Due to its relatively violent bombardment, active control for layer-by-layer growth is difficult compared to pulsed laser deposition.
- Inert sputtering gases may be built into the growing film as impurities.
- Most of the sputtering energy is transfered to heat in the target.
- Targets are often expensive.
- Some targets are fragile and may be broken by non-uniform heating.

2.1.2 Sol-gel

Sol-gel process is a chemical solution deposition (CSD) technique used for the fabrication of ceramics and organic-inorganic hybrids. In the initial stages, Budd *et al.* (1985) demonstrated sol-gel process for the formation of perovskite oxide thin film. Since then, a large variety of perovskite-related compounds have been synthesized as thin films by sol-gel, such as $PbTiO_3$ (Blum and Gurkovich 1985), $BaTiO_3$ (Kamalasanan *et al.* 1991), $SrBi_2Ta_2O_9$ (Boyle *et al.* 1996), $Pb(Mg_{1/3}Nb_{2/3})O_3$ (Okuwada *et al.* 1989), $(La,Sr)MnO_3$ (Taguchi *et al.* 1992).

Figure 2.2 illustrates the sol-gel process. In our *Mitsubishi Materials* sol-gel solution, lead acetate anhydrous, zirconium precursor and titanium precursor are dissolved in 1-butanol, with the ratio Pb:Zr:Ti = 110:52:48. 10% excess of lead is the compensation to its loss during the thermal treatment due to the volatility of PbO. A few droplets of PZT solution are drizzled over the substrate through a pipette. The substrate is rotated at high speed (normally from 1000 to 8000 rpm) during 15 $\sim$ 30 s. Following the

spin-coating, the film is dried at 325 °C on a heater for 5 min. The drying (also called calcination or pyrolysis) oxidizes the organic ligands bonded to the metal atoms and vaporizes the 1-butanol solvent leaving an amorphous PZT film. The thickness of one spin-coating film is $30 \sim 80$ nm, depending on the rotation speed. To obtain a thicker film, multiple spin-coatings are required. When the desired thickness is achieved, the sample is crystallized in an oxygen-purged rapid thermal annealing (RTA) system at 650 °C for 1 min. Every RTA step can crystallize a film of less than 150 nm. To fabricate a thicker PZT film, RTA is required for every 3 or 4 amorphous layers (< 150 nm) before performing following cycles of spin-coating.

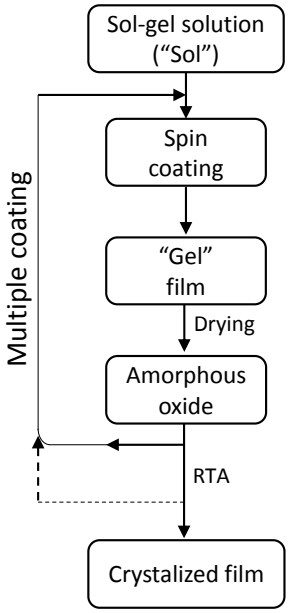

Figure 2.2: Schematic of sol-gel process.

The main advantages of sol-gel technique are the relatively low cost and the excellent control of film composition through the adjustment of precursor solution stoichiometry. Other advantages include easy fabrication process, high growth rate and large area coverage compared to sputtering, PLD and MBE. The disadvantages of sol-gel process include the difficulty of fabricating ultrathin film (< 30 nm) and coating 3D surface (Schwartz *et al.* 2004).

2.1.3 Lithographic Patterning

To fabricate top electrodes for the capacitors, lithography with reversal mask was employed. The advantage of using reversal lift-off is that after reversal the sidewall slope forms an undercut profile which avoids destroying the adjacent electrode in the development step.

The procedure of reversal lift-off is depicted in Figure 2.3 and described as follows:

1. Several drops of reversal resist *AZ5214E* are drizzled on the sample followed by 30 s of rotation at the speed of 5000 rpm . Then a soft bake is performed at 110 °C on a hot plate to drive off solvents

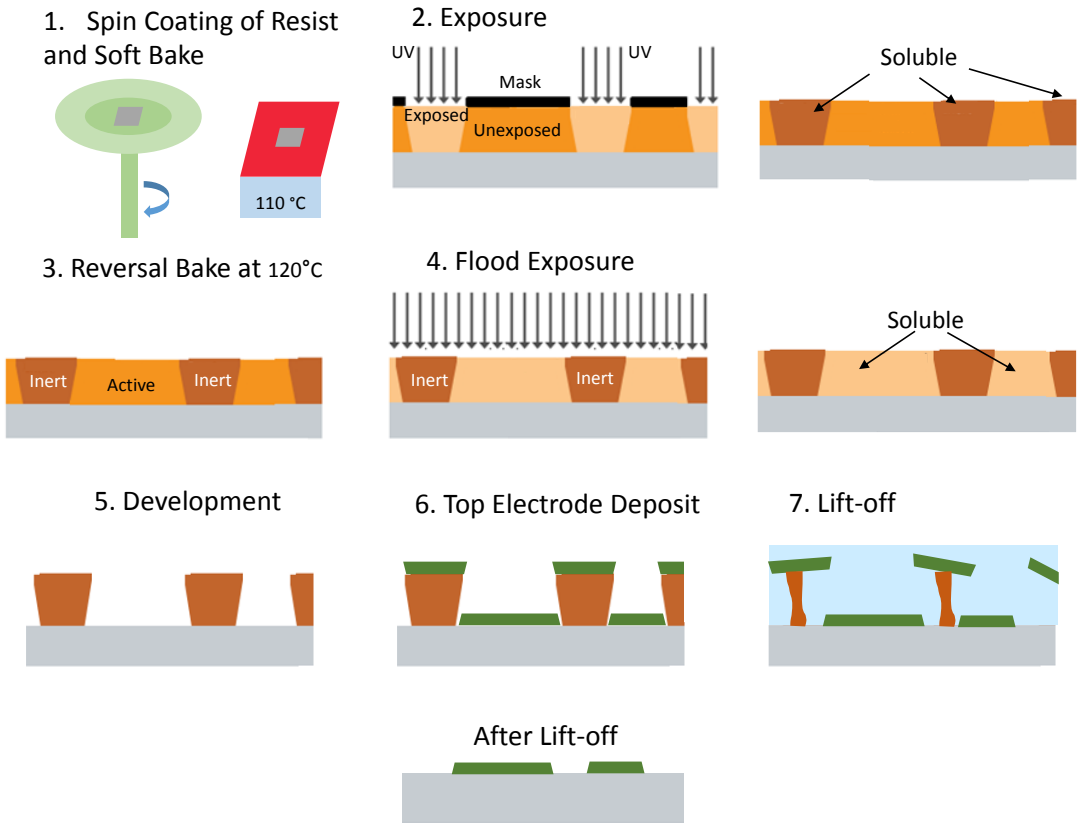

Figure 2.3: Reversal lift-off procedure for the deposition of top electrode.

and to solidify the film.

2. Resist is exposed to UV under reversal mask during 3 s. The photo active compound diazonaphtoquinone sulfonate in the exposed parts releases N_2 molecules and turn to be indene carboxylic acid, thus soluble in alkaline developer.

3. Reversal bake at 120 °C during 2 min make the exposed areas in last step inert while the unexposed areas remaining photo-active.

4. Flood exposure of 20 s turns unexposed areas in the 2nd step soluble.

5. The sample is immersed in *AZ 726 MIF* developer (component: tetramethylammonium hydroxide) during 40 $\sim$ 50 s to remove the alkaline soluble areas and then in deionized water to remove the developer residues.

6. Top electrode is sputtered on the sample surface at ambient temperature.

7. Developer-inert resist is removed by immersing the sample in acetone with ultrasonic during several minutes (then acetone is removed by ethanol).

2.2 Characterization Techniques

Film structure directly influences the ferroelectricity of the capacitors. Surface morphology has a great influence on the quality of film. Since a "sandwich" capacitor includes two interfaces between the ferroelectric and the two electrodes and one interface between the bottom electrode and the substrate, small roughness of each surface is the prerequisite of the high quality of subsequent film. We are now going to introduce the instruments for examining the structure and morphology.

2.2.1 Structural Analysis

X-ray diffraction (XRD) is commonly used in material science for probing the atomic and molecular structure of a crystal. XRD is a non-destructive analytical technique.

Since the wavelength of X-ray is comparable to the unit-cell spacing in crystals, X-ray can be diffracted from crystals which have regularly repeating atomic structures. Scattered X-rays interfere with each other either constructively or destructively, producing a diffraction pattern on a detector. The resulting wave interference pattern is the basis of diffraction analysis, which is called Bragg diffraction. When the phase shift is a multiple of 2π, the interference is constructive, which can be expressed by Bragg's law (Guinier 2013):

$$n\lambda = 2dsin\theta \tag{2.1}$$

where n is an integer, representing the diffraction order, λ is the wavelength of the X-ray, d is the spacing between planes in the atomic lattice and θ is the angle between the incident ray and the scattering planes. A diffraction pattern is obtained by measuring the intensity of scattered waves as a function of scattering angle. Figure 2.4 shows the geometry of *Rigaku SmartLab* 4-circle diffractometer. The X-ray sources are Cu $K\alpha_1$ photons, with a wavelength of 1.5406 Å. A 2-bounce Ge (220) monochromator is used to reduce the beam divergence, improving signal to noise ratio.

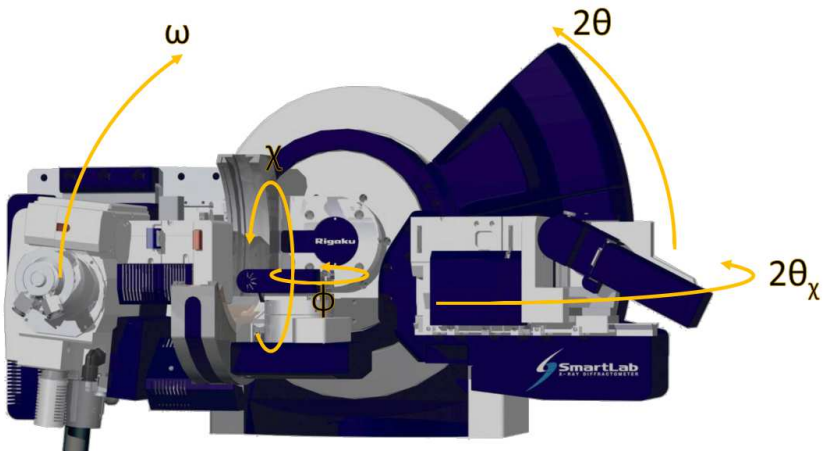

Figure 2.4: Geometry of *Rigaku SmartLab* 4-circle diffractometer.

To measure out-of-plane lattice parameter, $2\theta/\omega$ scan is performed. Scanning through ω axis around (002) peak, a "rocking curve" is obtained, which can be used to evaluate the out-of-plane mosaicity of the thin film. For in-plane measurement, instead of $2\theta/\omega$ scan and ω scan, $2\theta_\chi/\phi$ scan and ϕ scan are used to extract the in-plane lattice parameter and evaluate the in-plane mosaicity, respectively. A combination of $2\theta/\omega$ scan and ω scan is sometimes required to reveal the strain state of thin film by performing asymmetric scan. X-ray is also used to obtain the thin film thickness through X-ray reflectivity (XRR). XRR scan is similar to $2\theta/\theta$ scan, but has a very small incident angle (usually $0 \sim 5°$). For incident angles greater than a critical angle θ_c, the X-ray beam partially penetrates into the film and partially reflect from the surface. The interference between the rays reflected from the surface of the film and the bottom of the film results in interference fringes. By using Fourier transform, the thickness, roughness and density of the layer can be obtained.

2.2.2 Morphological Analysis

Atomic force microscopy (AFM) is a technique to obtain topographies and other surface informations from a variety of samples. AFM works by scanning a tip along the sample surface. When the tip is brought into proximity of a sample, forces between the tip and the surface lead to cantilever deflection according to Hooke's law. The deflection of the cantilever due to forces acting on the tip is detected by a laser focused on the back of the cantilever. The laser is reflected on a distant photodiode. The movement of the laser spot on the photodiode reveals the sample's topography along with other informations. The sample is mounted on a piezoelectric scanner, which precisely maintains the distance between the tip and the surface or the force on the tip. *Veeco CP-II* is used to carry out AFM measurement. Figure 2.5 shows the schematic of AFM operation.

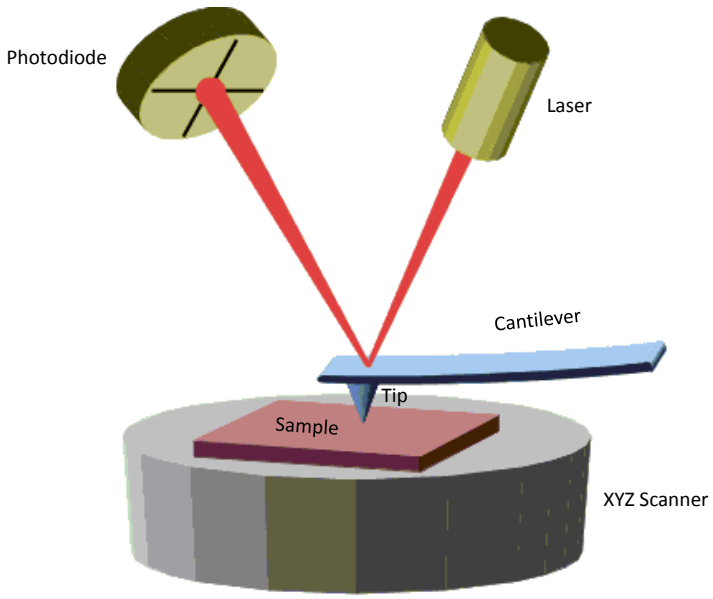

Figure 2.5: Schematic of AFM operation. Image adapted from Web (2014).

According to the nature of the tip motion, AFM operation is described in three modes:

- **Contact mode:** The tip is "dragged" across the surface. The defection of the cantilever is kept constant. In this mode, the image is heavily influenced by frictional and adhesive forces.
- **Non-contact mode:** The tip does not contact the surface but is oscillated at the resonance frequency. The amplitude of the oscillation is kept constant. In non-contact mode, image quality can be reduced by the surface contaminant (*e.g.*, water) .
- **Tapping mode:** The tip oscillates up and down as non-contact mode. But at each oscillation downward, the tip touches the surface. The oscillation amplitude is maintained. This method of "tapping" lessens the damage done to the surface compared to contact mode and provides higher resolution compared to non-contact mode. In this work, most of the surface morphologies were measured through tapping mode.

2.2.3 Electrical Characterization

Microscale electrical characterizations of ferroelectrics are widely used to evaluate the properties of the capacitors, including: current-voltage measurement, capacitance-voltage measurement and hysteresis loop measurement. Nano-scale PFM measurement provides the opportunity to investigate domain switching behavior with a resolution of several nm.

2.2.3.1 Current-Voltage

Low leakage current is an essential prerequisite for a ferroelectric film. It depends on the mobility of free electronic charges in the ferroelectric. An applied voltage results in a leakage current flow through the capacitor. The current-voltage (I-V) measurement is performed by applying a step shaped voltage waveform from 0 to $+V_{max}/-V_{max}$, as shown in Figure 2.6. The measurement was carried out by *Agilent 4156B Semiconductor parameter analyzer*. Current response is recorded after performing a voltage of the same waveform to avoid the domain switching current. At each voltage step (V_s), current is monitored after a short period (delay time, t_d). In this work, $t_d = 0$ was employed since we did not observe significant difference of leakage by varying t_d.

A typical leakage characteristic is shown in Figure 2.7. According to the amount of leakage, the insulated property of a ferroelectric can be evaluated. By fitting the leakage current to equations of different charge transport mechanisms, the dominant transport mechanism can be found.

2.2.3.2 Capacitance-Voltage

Ferroelectrics exhibit a nonlinear relative permittivity ε_r, which is dependent on field, frequency and temperature. For an ideal ferroelectric, ε_r as a function of field is shown in Figure 2.8. ε_r shows 2 narrow

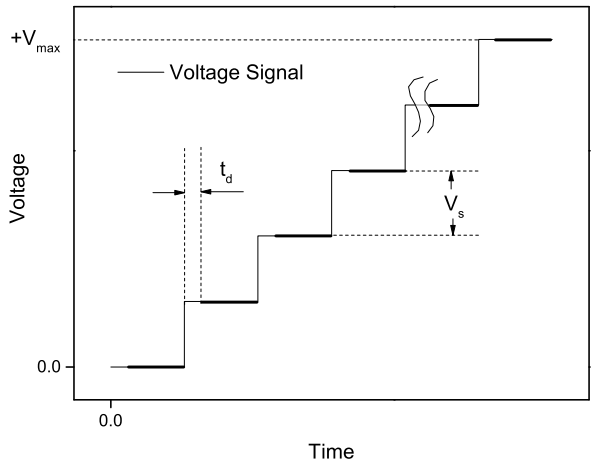

Figure 2.6: Voltage waveform for typical I-V measurement.

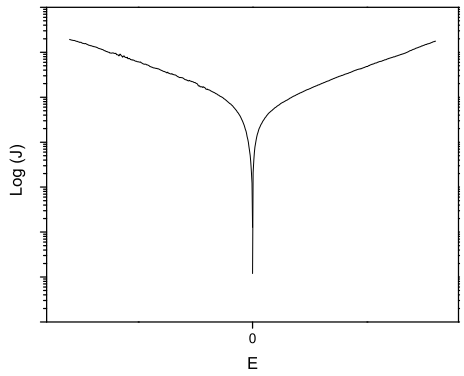

Figure 2.7: Typical J-E curve of a ferroelectric capacitor.

peaks in two small regions around the coercive field E_c. The peak value is relatively much higher than ε_r at other field, which is near 0. This occurs because during switching, a small field change results in a very large change in polarization (Brennan 1992). Peak value can exceeds 5000 for a high quality ferroelectric (even higher ε_r is achieved by Erbil *et al.* (1996)). Peak value of ε_r is frequency dependent. As frequency increase, it decreases and attains to a constant limiting value. It can be explained by the behavior of dipole movement. As frequency increases, dipoles begin to lag behind the change of the field and the accumulation of charges at the interfaces between the sample and the electrode drops (Saif *et al.* 2011). ε_r is also temperature dependent. Elevated temperature disturbs the alignment of dipoles, resulting in a decrease in the peak value of ε_r.

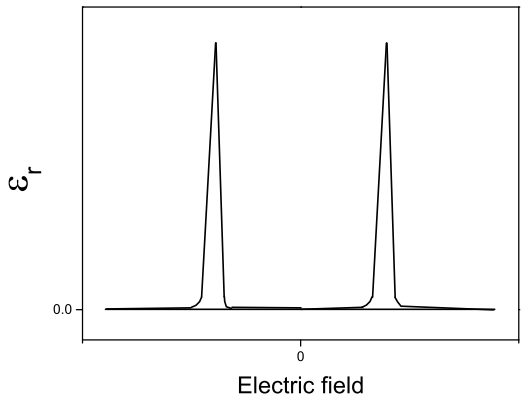

Figure 2.8: ε_r as a function of field for an ideal ferroelectric. Image adapted from Evans (2010).

To perform the capacitance-voltage (C-V) measurement, *HP 4284A Precision LCR meter* was used. The ferroelectric is under a DC bias voltage (the waveform is similar to that used in I-V measurement), whereas the capacitance is tested with a small AC field. The circuit is shown in Figure 2.9. As the capacitance of a ferroelectric capacitor is small (usually less than 10 nF), it yields large reactance. This implies that the effect of the parallel resistance (R_p) has relatively more significance than that of the series resistance (R_s). The low value of resistance represented by R_s has negligible significance compared with the capacitive reactance, so the parallel circuit mode C_p-G is employed for ferroelectric.

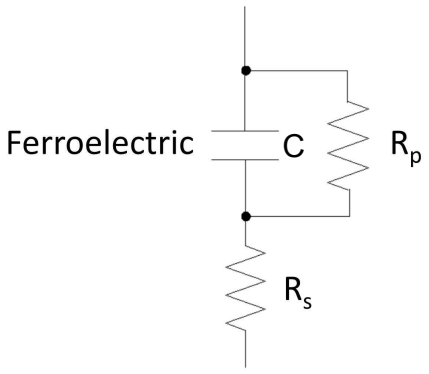

Figure 2.9: C-V measurement circuit.

The admittance (reciprocal of impedance) in the parallel circuit is:

$$Y = G + jB = G - 2\pi f C_p j \quad (j^2 = -1) \tag{2.2}$$

Through $\varepsilon_r = Cd/\varepsilon_0 A$ (d is the thickness of ferroelectric and A is the area), ε_r can be obtained and be expressed in two parts: real component ε_r' and imaginary component ε_r''.

$$\varepsilon_r = \varepsilon_r' - j\varepsilon_r'' \tag{2.3}$$

$$\varepsilon_r' = Gd/\varepsilon_0 A \tag{2.4}$$

$$\varepsilon_r'' = |B|d/\varepsilon_0 A \tag{2.5}$$

ε_r'' is attributed to bound charge and dipole relaxation phenomena, which gives energy loss. Loss tangent is used as quality factor, which is the ratio of ε_r'' to ε_r' (or $|B|/G$).

C-V curve shape of real ferroelectric is not like Figure 2.8 but resembles Figure 2.10, which contains three parts (Mihara *et al.* 1992, Evans 2011): a linear part ε_{r_l}', independent of voltage and frequency; the upper non-linear part (with 2 peaks), linked to ferroelectric switching behavior; the lower linear part, linked to paraelectricity (polarization disappears when external applied field is removed).

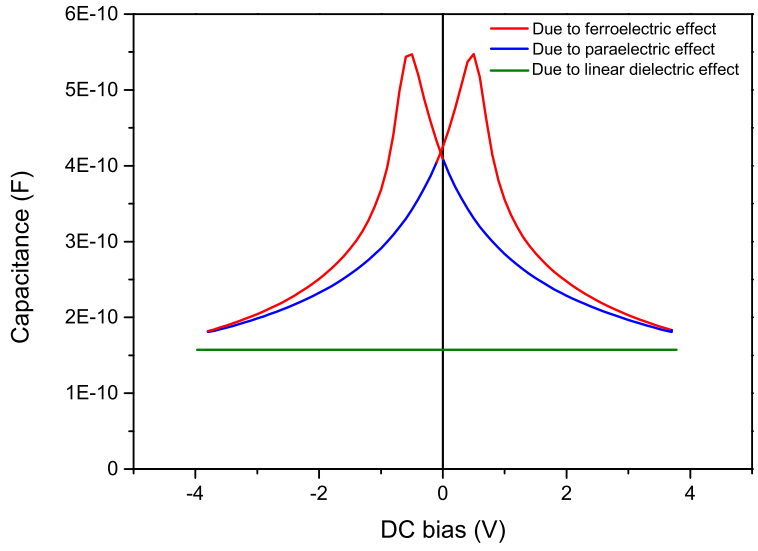

Figure 2.10: Schematic of different contributions in a C-V curve. Data from 190-nm-thick sputtered PZT capacitor with SRO top electrode.

2.2.3.3 P-E Hysteresis Loop

Not long after the discovery of ferroelectricity in Rochelle salt (Valasek 1921), the switchable polarization in ferroelectric materials has been usually measured by a Sawyer-Tower set-up (Sawyer and Tower 1930), which is still widely used nowadays. Sawyer and Tower used a Braun tube to obtain oscillograms, which was made by 2 pairs of plates: one pair to steer the beam in X and the other in Y. A 60 Hz sinuous alternative signal was used to switch the polarization in Rochelle salt. By measuring the deflections in Y axis, polarization-electric field (P-E) hysteresis loops were obtained.

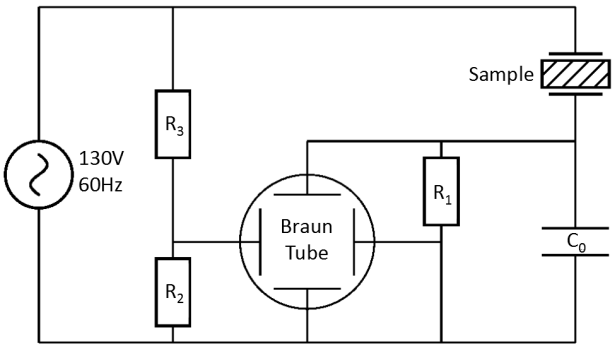

Figure 2.11: Schematic connection of Sawyer-Tower circuit in 1930. $C = 0.7\ Mf$; $R_1 = 450000\ \Omega$; $R_2 = 3180\ \Omega$; $R_3 = 31800\ \Omega$. Image adapted from Wikipedia (2010).

Later as the techniques advance, Braun tube has been replaced by the much powerful oscilloscope and a versatile generator is also employed in the circuit, as shown in Figure 2.12. Sinuous, triangle and square signals can be used to trigger the switching in ferroelectrics. However, a major limitation in Sawyer-Tower circuit is: it measures charges flowing through the capacitance as a whole, including the charges due to switchable property of ferroelectrics, the charges due to the change of external voltage and the part due to leakage current. If with another circuit, these different contributions can be separated, a further understanding of ferroelectric properties can be achieved.

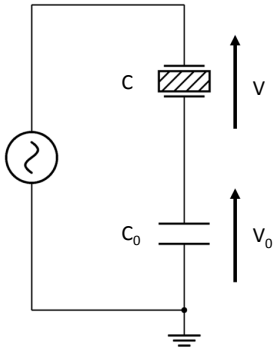

Figure 2.12: Schematic connection of Sawyer-Tower circuit nowadays.

PUND (Positive Up Negative Down) has been used since the end of last century to extract the P-E hysteresis loop which is only due to the domain motion together with the loop with whole contributions as

that from Sawyer-Tower set-up. Figure 2.13 shows the input voltage signal of PUND pulse trains. In this work, a triangle wave is used to switch the domains. The PUND pulse train programed by LabView is generated by *NF WF1966* 2-channel generator. The currenr response was recorded by *Nicolet INTEGRA-40* oscilloscope after the amplification stage by *KEITHLEY 428* current amplifier. t_{inc} is the period to increase the drive voltage from 0 to V_{max}. t_{dec} is the period of inverse course and usually they are the same. t_{int} is the interval period between two same pulse. t_r is the period between inverse pulses.

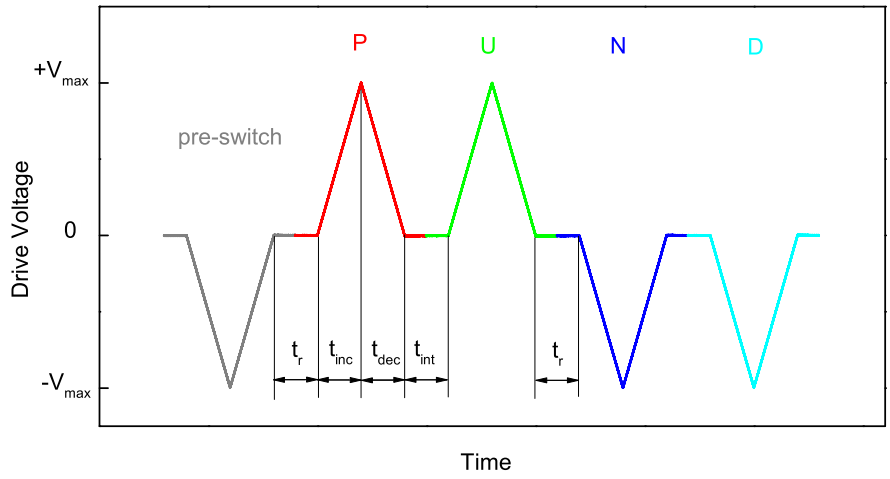

Figure 2.13: PUND pulse train signal.

In a PUND pulse train, the first negative pre-switch voltage acts to switch the domains downward (if the voltage is higher than coercive voltage). Then the first the positive voltage "P" switches the domain upward, which includes the contribution due to the domain motion and other parts. Subsequently a second positive voltage "U" is employed to measure the contribution not due to the domain motion. By subtracting the charges during the pulse "U" from the charges during the pulse "P", the switching-up charges can be measured. Combining this with the negative half, a PUND hysteresis loop is formed. By integrating the charges during P and N pulse, a PN loop is obtained which is equivalent to Sawyer-Tower loop and has almost identical shape and characteristic values. Figure 2.14 shows the circuit in PUND measurement. Different from Sawyer-Tower circuit, the charge is not recorded directly, thus the hysteresis loop can not display on the oscilloscope simultaneously. Instead, current response to the whole pulse train is recorded and charges are obtained by integrating the response under each pulse. Amplitude of V_{max} and PUND pulse frequency are manipulated directly in the generator. Retention quality of a ferroelectric capacitor is investigated by varying t_r.

Figure 2.15 shows the corresponding currents to PUND pulse train. For a good ferroelectric, I_U is much smaller than I_P. When the sample is leaky, I_U is considerably high and even can be much bigger than I_{P-U}.

I_P (or I_N) contains three parts: switching current I_{P-U} (or I_{N-D}); non-switching current I_d, which is due to the dielectric polarization of the capacitor (as the drive voltage changes, an amount of

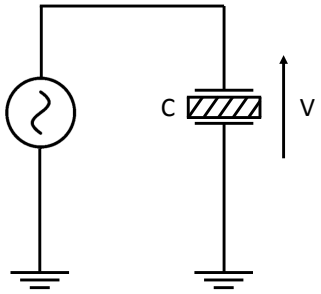

Figure 2.14: Schematic connection of the circuit used in PUND measurement.

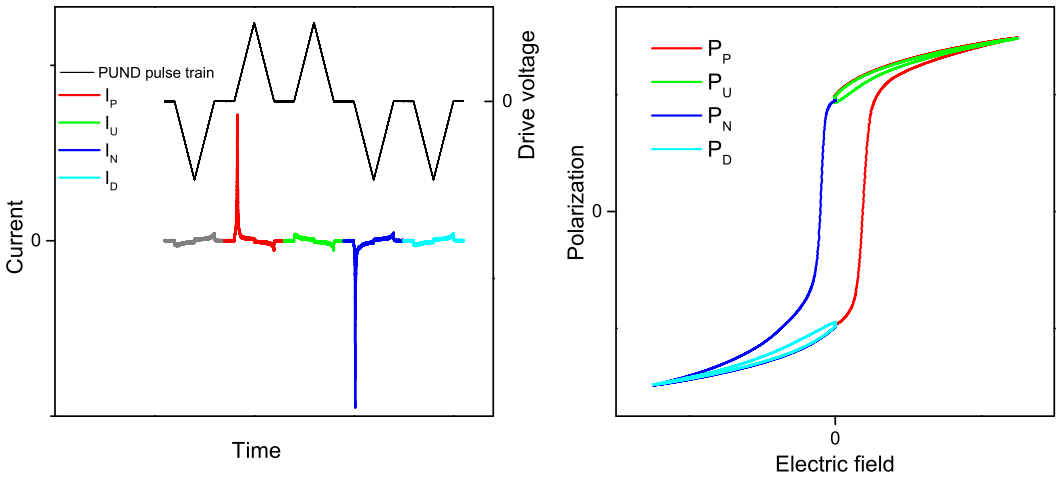

Figure 2.15: Drive voltage, corresponding currents and polarizations in PUND measurement.

charges flow to the opposite direction); and leakage current I_l, which is almost negligible in Figure 2.16. And their relations are:

$$I_P = I_{P-U} + I_U \quad (I_N = I_{N-D} + I_D) \tag{2.6}$$

$$I_U = I_d^p + I_l^p \quad (I_D = I_d^n + I_l^n) \tag{2.7}$$

PUND loop can be extracted by combining

$$P^p = \frac{1}{A}\int I_{P-U}\,\mathrm{d}t \quad and \quad P^n = \frac{1}{A}\int I_{N-D}\,\mathrm{d}t \tag{2.8}$$

PN loop can be extracted by combining

$$P^p = \frac{1}{A}\int I_P\,\mathrm{d}t \quad and \quad P^n = \frac{1}{A}\int I_N\,\mathrm{d}t \tag{2.9}$$

where A is the area of the electrode ($100 \times 100\mu m^2$ for all measurements in this work unless stated otherwise); P^p and P^n are polarization in positive part and negative part, respectively.

Figure 2.16 shows the PUND loop, PN loop and corresponding currents I_{P-U} and I_{N-D}. From PUND loop, remnant polarization P_r and coercive field E_c are extracted. From PN loop, maximum polarization $P^\star$ is extracted. In this example, $P^\star$ is about 50% bigger than P_r. If a ferroelectric is more leaky than this one (which can be caused by inferior film quality, approximation to breakdown voltage or elevated temperature), I_U (or I_D) will be much larger and $P^\star$ is driven up to be many times larger than P_r. So for a good ferroelectric (P_r from PUND loop and from PN loop are identical), $P^\star$ is the maximum displacement at V_{max}, containing both remnant part P_r and non-remnant part. For a leaky ferroelectric, besides these two parts $P^\star$ also contains the contribution from leakage.

High voltage/current ratio of amplifier is favorable to increase the signal/noise ratio. However, non-zero current may be observed due to the artifact of the amplifier, resulting in incomplete hysteresis loop. This problem can be solved by frequently pressing the "Correct" button or subtracting the average current at 0 V. Square waveform of PUND pulse signal provides higher voltage increasing rate compared to triangular waveform. With PUND pulse train, contributions from domain motion and from leakage can be separated, which makes the evaluation of a ferroelectric capacitor easier and more accurate.

2.2.3.4 Piezoresponse Force Microscopy

Piezoresponse force microscopy (PFM) is a variant of AFM that images and manipulates ferroelectric domains. The PFM technique is based on the converse piezoelectric effect (CPE). As all ferroelectrics exhibit piezoelectricity, an electric field applied on a ferroelectric results in changes of dimension. To

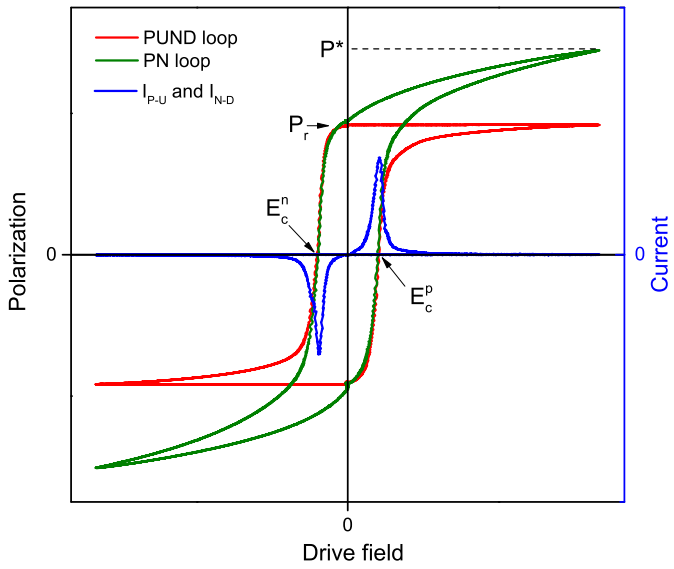

Figure 2.16: PUND loop, PN loop and corresponding currents.

detect the polarization orientation, a conductive tip is in contact with the ferroelectric surface and an alternating voltage is applied on the tip. In response to the electrical stimulus, the domain beneath the tip expands if the polarization is parallel to the electrical field. And the domain contracts when it is anti-parallel to the field. By comparing the amplitude and phase of the tip to the driving signal, the information of the domain can be obtained (Alexe and Gruverman 2004). Figure 2.17 illustrates the ideal phase and amplitude to a 180° domain ferroelectric.

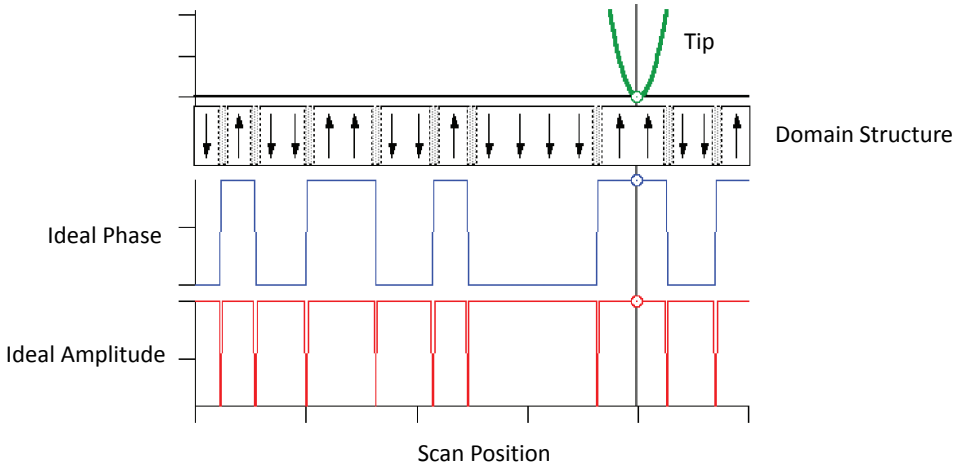

Figure 2.17: Ideal output phase and amplitude in PFM imaging. Image adapted from Proksch and Kalinin (2008).

The above method of using phase signal to map the orientation of out-of-plane orientation of a ferroelectric is called PFM imaging, which is frequently used to investigate domain switching behaviors. For PZT in this work, vertical PFM imaging was employed since the PZT film was crystallized in 00l direction. First domains of different direction are "written" by a voltage higher than coercive voltage

sweeping on the PZT film. Then the switching information is "read" by PFM imaging according to the principle described above. The standard procedure is as follows:

1. Scan a square with various DC bias voltage to determine the coercive voltage.
2. Determine the size of area to be studied (such as $5 \times 5\,\mu m^2$, or $20 \times 20\,\mu m^2$). Scan a square on the surface with a sufficient DC bias voltage applied to the tip to switch all the opposing domains thus all domains will point to the same direction. The signal is read by an AC bias.
3. Scan a smaller square inside the previous one with opposite drive voltage to force all scanned domains to point to the opposite direction.
4. Depending on the quality of the film and the scan size, an even smaller square of scan inside the previous zone with the opposite drive voltage to the last one can be performed. Squares scanned with opposite drive voltage will present contrast in phase and amplitude. Contrast nearby a smaller square is usually less obvious because of the increasing difficulty in switching the domain without poling the nearby ones.
5. Retention is investigated by writing 2 or 3 different size of squares on the surface as step two and read the signal some time later.

By performing PFM imaging, topography, phase and amplitude can be obtained simultaneously. Based on the same principle, local domain can be switched by applying a field larger than coercive field. This technique is called PFM spectroscopy, in which a small AC signal is carried by a square wave which steps in magnitude with time. As the square wave passes coercive field, domain switches which can be detected by the AC signal. The voltage signal is shown in Figure 2.18. Step period and interval period can be varied.

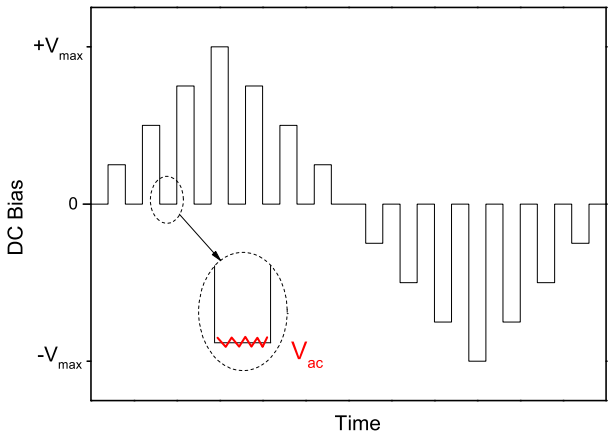

Figure 2.18: Drive voltage for PFM spectroscopy.

The hysteresis loop is obtained through the phase response. Figure 2.19 shows a typical phase response and amplitude response in PFM spectroscopy. Based on the fact that PFM spectroscopy manipulates domain locally, this technique can investigate the domain switching behavior in nano-scale, much smaller than in PUND measurement.

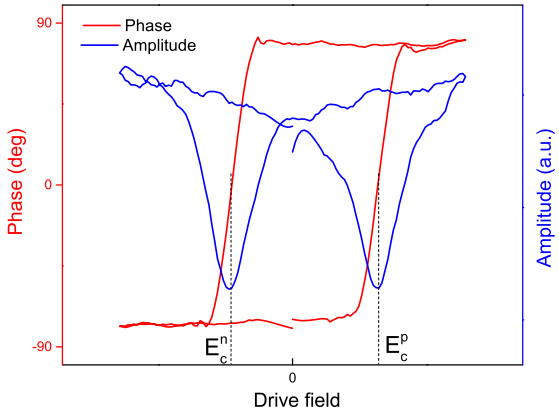

Figure 2.19: Phase and amplitude response in PFM spectroscopy.

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Chapter 3

Fabrication and Structural Characterizaton

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The aim of this chapter is to present the growth details of epitaxial $Pb(Zr_{0.52},Ti_{0.48})O_3$, which is in the region of MPB, on $SrTiO_3$ (STO) substrate with an interlayer of $SrRuO_3$ (SRO) as bottom electrode by two growth routes, sputtering and sol-gel. The crystal structure of both bottom electrode and PZT film were characterized by XRD. AFM was performed for morphological characterization of each layer.

The capacitor stack structure is ***top electrode*/*PZT*/*bottom electrode*/*substrate***, which is often labeled as metal-ferroelectric-metal (MFM) stack. First, STO (001) was chosen as substrate for its shared perovskite structure, slightly smaller lattice parameter (-3.68% of PZT 52/48 a-axis lattice

parameter) which can increase PZT tetragonality by the clamping force applied. SRO was selected as bottom electrode for its conductive property, compatible structure (pseudo-cubic), close lattice parameter (between STO and PZT), which could facilitate the hetero-epitaxial growth and its chemical stability. For both growth routes (sputtering and sol-gel), PZT films have been grown from less than 50 *nm* to around 200 *nm* in order to investigate the thickness influence and to figure out the thinnest workable PZT capacitor. As the metal-ferroelectric interface plays an important role on the PZT properties and different metallic materials exhibit different work functions, three conductive materials, SRO, Pt and ITO (indium tin oxide) have been employed as top electrode to study their influence on PZT capacitor's electric properties.

In this work, every capacitor was fabricated from bottom to top in four steps: 1) preparation of STO substrate; 2) deposition of bottom electrode; 3) deposition of PZT film through sputtering or sol-gel (both required a post annealing for crystallization); 4) deposition of top electrode (another post annealing was required for its crystallization). Growth conditions, including temperature, plasma voltage for sputtering; rotational speed and acceleration for sol-gel, have been varied for optimization. The details of each step will be presented in the following sections.

3.1 Substrate Preparation

Before depositing SRO bottom electrode, a chemical treatment was applied to the STO (001) substrate to obtain atomic plane with single termination. Figure 3.1 shows the surface morphology of as-received STO substrate. Irregular terraces of roughly 2 Å revealed the alternating terminations of SrO and TiO_2. Blurred morphology indicated that contamination (H_2O and CO_2) worsened the surface.

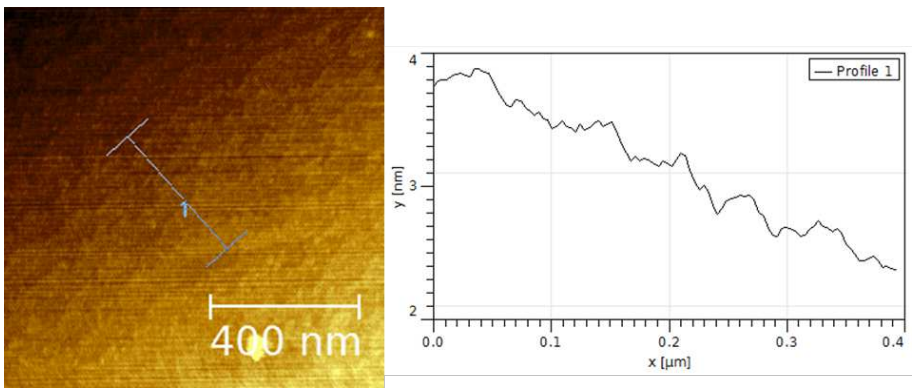

Figure 3.1: Topography of as-received STO substrate.

Rough surface with two different terminations increases the difficulty of hetero-epitaxial growth, causing more defects in the interface and degrading the film crystal structure. Besides, the growth rate of SRO on the two terminations is found to be different (Koster *et al.* 2012), which may further increase the surface roughness. Kawasaki *et al.* (1994) first invented an acidic etching procedure to obtain an atomic flat surface of STO by removing the top SrO layer and contaminations. Now it becomes a standard

procedure for thin film growth on oxide substrate as well as on silicon substrate for removing SiO_2.

Abrupt surface is obtained by using the different chemical properties of the two terminations. SrO reacts with CO_2 and H_2O, forming $SrCO_3$ and $Sr(OH)_2$, respectively (Ohnishi *et al.* 2004), which can be dissolved in HF. TiO_2 is very stable in water and its solubility in HF is much smaller than SrO. Thus HF can be used to effectively remove the top-most SrO layer and the $Sr(OH)_2$.

Our modified treatment procedure based on Kawasaki's study is described as follows:

1. Rinse in acetone during 10 *min* with ultrasonic.
2. Rinse in ethanol during 10 *min* with ultrasonic.
3. Rinse in deionized water during 10 *min* with ultrasonic.
4. Immerse in pure BOE (buffered oxide etching solution) during 20 *s*.
5. Rinse in three beakers of deionized water, each for 1 *min*.
6. Rinse in ethanol during 3 *min* with ultrasonic.
7. Dry up with N_2 gun.
8. Anneal at 950 °C in O_2 for 10 *h* with furnace pre-heated to avoid contaminations.

The final annealing is implemented to totally remove the remnants in previous treatments and to facilitate the re-crystallization of top-most layer. The duration of etching and annealing can be modified depending on the miscut angle of the substrate surface (small miscut angle substrate requires less etching duration). Figure 3.2 shows the surface morphology of STO substrate after treatment. Flat TiO_2 surface with terraces of single unit cell replaces the mixture of SrO and TiO_2.

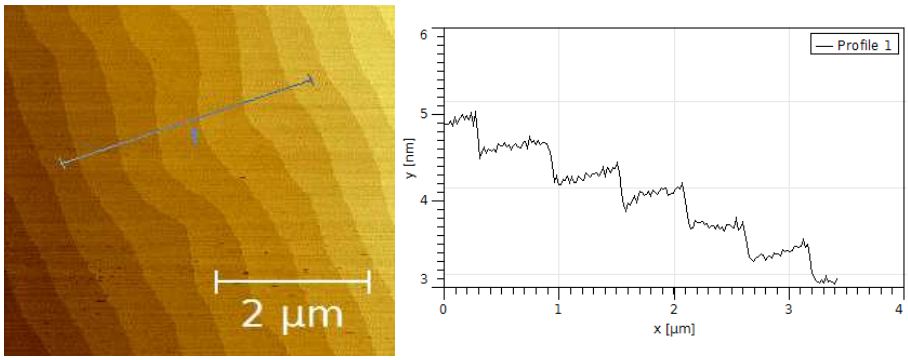

Figure 3.2: Topography of STO substrate after chemical treatment.

3.2 Deposition of SRO

In this section, at first, the properties of SRO will be introduced. Then the optimization by varying deposition conditions will be presented. At last, the structure characteristics of deposited SRO as bottom electrode will be presented.

3.2.1 Choice of SRO as Bottom Electrode

SRO was chosen as the bottom electrode for all the capacitors in this work for its: a) conductive property without doping; b) high chemical stability; c) comparable perovskite structure, providing a good lattice matching with both STO substrate and PZT thin film.

Hetero-structures of ferroelectric thin films are attractive for the lack of detrimental grain boundaries and SRO makes it achievable. Since Eom *et al.* (1992) successfully grew epitaxial SRO layer on STO substrate two decades ago, SRO has been widely applied as a conducting layer on complex oxide studies. SRO is grown by various approaches, mostly by pulsed laser deposition (PLD) (Wu *et al.* 1993, Rijnders *et al.* 2004, Lee *et al.* 2004), sputtering (Eom *et al.* 1993, Jiang *et al.* 1998, Gan *et al.* 1999), molecular beam epitaxy (MBE) (Tian *et al.* 2007) and metal organic chemical vapor deposition (MOCVD) (Takahashi *et al.* 2002). PLD can achieve good quality through layer-by-layer deposition (Choi *et al.* 2001), but the coverage is usually very poor (Defay 2013). In this work, SRO is deposited by sputtering for its much larger achievable area and higher homogeneity compared to PLD.

SRO exhibits good conductivity. At room temperature, the resistivity of SRO (100 nm) is around 220 $\mu\Omega \cdot cm$ (Klein *et al.* 1996).[1] Allen *et al.* (1996) observed that from T_c ($\sim$ 160 K) to 1000 K, the resistivity of SRO was linearly dependent on temperature, which is important for electrode application. SRO is chemically and thermally stable. In oxidizing or inert gas atmospheres, it is stable up to 1200 K (Bensch *et al.* 1990).

Of the well-known ruthenates series $Sr_{n+1}Ru_nO_{3n+1}$, $SrRuO_3$ is the infinite-layer compound ($n = \infty$), having an orthorhombic structure at room temperature, with lattice parameters $a_0 = 5.5670$ Å, $b_0 = 5.5304$ Å, $c_0 = 7.8446$ Å, (Jones *et al.* 1989, Gan *et al.* 1999). It also exhibits a lightly distorted pseudo-cubic perovskite structure with lattice parameter $a_{pc} = 3.93$ Å, $\alpha = \beta = 90°$, and $\gamma = 89.6°$. The lattice mismatch of SRO and STO is exceptionally small (1.01%) and the lattice mismatch of SRO and PZT is also fairly small (2.80%), which facilitates the hetero-epitaxial growth of PZT on STO.

The crystallographic relationship between the orthorhombic and the pseudo-cubic structures is illustrated in Figure 3.3. The orthorhombic distortion arises from the rotation of RuO_6 octahedrons around $[001]_{pc}$ and $[010]_{pc}$ at room temperature.[2] At 547 °C, the orthorhombic phase of bulk SRO transforms to tetragonal phase with RuO_6 octahedrons rotated only around $[001]_{pc}$. When rising to 677 °C, it transforms into cubic phase with RuO_6 octahedrons no more rotated. And for about 50-nm-thick epitaxial SRO film, orthorhombic-cubic transition[3] temperature decreases to 280 °C due to the strain applied by STO substrate (Choi *et al.* 2010).

To obtain high quality hetero-epitaxial structure, SRO has to be grown on a STO substrate with single termination. Contamination will increase the defects in the interface. Besides, SRO grows faster on B-site termination (Koster *et al.* 2012). Different growth rate causes non-uniform morphology, which

[1] The resistivity of 110-nm-thick Pt film is 12 $\mu\Omega \cdot cm$ (Aaltonen *et al.* 2003).
[2] In this dissertation, the Miller indices for SRO are based on the pseudo-cubic structure.
[3] It is difficult to discriminate the tetragonal and cubic phases because it involves only small oxygen atom displacements with RuO_6 octahedrons rotated around SRO [001] direction(Vailionis *et al.* 2007).

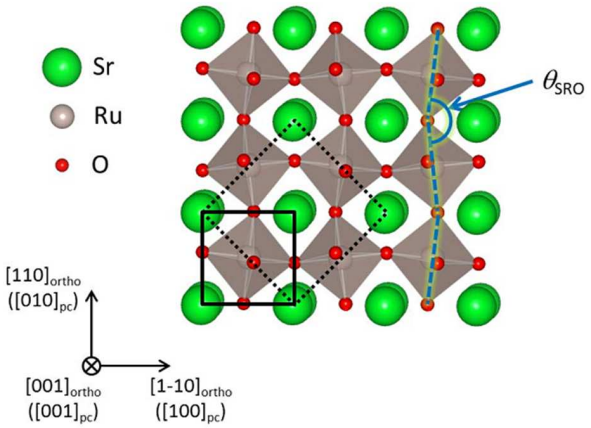

Figure 3.3: Crystal structure of SRO. SRO has a Pbmn orthorhombic pervoskite structure with $\sqrt{2}a_{pc} \times \sqrt{2}a_{pc} \times 2a_{pc}$ unite cell Dimensions, where a_{pc} denotes the pseudo-cubic lattice parameter. The black dotted and solid squares represent the unite cell of orthorhombic and pseudo-cubic structures, respectively. Oxygen octahedral tilt angle θ_{SRO} is illustrated by the blue dash lines (Aso *et al.* 2013).

will also result in more defects in the subsequent film growth.

3.2.2 Optimization of SRO Growth

All SRO films were deposited on (001) STO substrates by an in-axis sputtering machine. As stated, substrate temperature, plasma voltage, chamber pressure and gas composition all impact the property of deposited thin film. First, we studied the influence of the substrate temperature. Four SRO films were deposited at different temperatures[4] from 460 °C to 675 °C on as-received (001) STO substrates[5] during 75 *min*. Plasma voltage were all kept at 109 *V*, chamber pressure at 0.005 *mbar*, gas composition of 50 *sccm* Ar/5 *sccm* O_2. Figure 3.4 shows out-of-plane $2\theta/\omega$ scans and rocking curves of these four SRO films. The two SRO deposited at relatively lower temperatures showed much smaller intensity of SRO (002)[6] peak compared with the other two, indicating that relatively small amount of SRO was crystallized when at less than 600 °C. SRO deposited at 620 °C had more crystalline SRO comparing to the one at 675 °C. And the Kiessig fringes around SRO (002) peak of the one at 620 °C indicated the low roughness of the SRO film surface.

From the rocking curves of these four SRO films, a narrow sharp peak with higher intensity and a broad peak with lower intensity were observed for the two SRO films deposited at relatively lower temperatures. The broad peak indicated that part of the SRO crystal structure exhibited high mosaicity. The broad peak disappeared at higher temperature. The peak of the SRO film deposited at 620 °C had highest intensity and narrowest full width at half maximum (FWHM), indicating its best quality of these four films.

[4] At each temperature, two or three SRO were deposited at the same time, film deposited at same temperature showed similar results.

[5] To investigate the influence of substrate temperature, thick SRO film ($\sim$ 100 *nm*) were deposited to mainly study the crystalline quality. Substrates were only cleaned by acedone and ethanol, not chemically treated by BOE solution.

[6] According to Jiang *et al.*'s work (1998) on SRO's orientation on vicinal (001) STO, 95% SRO exhibited (001) domain and 5% possessed (010) or (100). In this work, we use (001) as the out-of-plane direction of deposited SRO for simplicity.

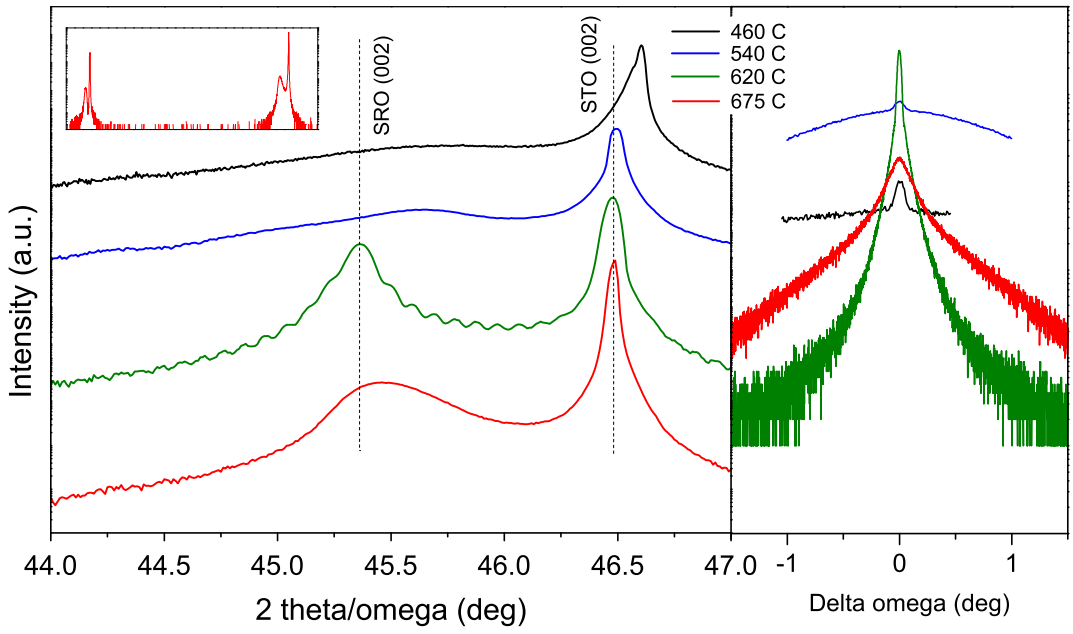

Figure 3.4: Out-of-plane $2\theta/\omega$ scans and rocking curves around (002) of SRO films deposited at different temperatures. Inset shows $2\theta/\omega$ scan of SRO deposited at 675 °C from 20° to 50°. Deposition parameters as follows, voltage: 109 V; chamber pressure: 0.005 $mbar$; gas composition: 50 $sccm$ Ar/ 5 $sccm$ O_2, duration: 75 min. Inset shows $2\theta/\omega$ scan of SRO deposited at 675 °C from 20° to 50°.

The reason why SRO film deposited at 620 °C was better crystallized than that deposited at 675 °C is not clear. Many groups' optimal substrate temperature for SRO deposition by sputtering is higher than 675 °C (Hou *et al.* 1995). 675 °C is the maximum achievable temperature for our sputtering machine and it takes around 50% time ($\sim$ 40 min) to increase from 620 °C to 675 °C and sometimes the sputtering machine could only reach $\sim$ 650 °C after $\sim$ 100 min heating. It is reasonable to attribute the reduced quality either to the diffused Sr to the STO surface during the heating (before deposition) or to the bigger temperature variation at maximum substrate temperature. It also should be noted that the substrate temperature is indirectly measured by a thermocouple. Reduced calibration may result in some deviations. Later work showed SRO film on vicinal STO deposited at 620 °C always exhibited slightly higher intensity of SRO (002) peak and slightly smaller mosaicity (the difference also depended on the film thickness).

X-ray reflectivity (XRR) was performed to extract the film thickness. The thicknesses of the SRO films deposited at 600 °C and 675 °C were 102.4 nm and 97.4 nm, respectively. The thickness of the other two cannot be measured due to their rough surface morphologies (about 100-nm-thick film with rough surface is hard to obtain oscillations in XRR spectrum). From sputtering depositions of SRO, PZT and Pt, it was found that higher temperature caused reduced deposition rate, which could be attributed to the higher mobility and lower adhesion of species to the substrate at higher temperature. Compared with the SRO film deposited at room temperature (at the same conditions used for the four films above), the deposition rate reduced about 25% when at 650 °C.

Out-of-plane lattice parameter were extracted from $2\theta/\omega$ scan by fitting the SRO (002) peaks. Full

width at half maximum values (FWHM) were extracted from the rocking curve scans. Both are plotted in Figure 3.5. SRO film deposited at 460 °C and 540 °C showed similar out-of-plane lattice parameter and similar FWHM (0.09°). Film deposited at 620 °C and 675 °C had larger out-of-plane lattice parameters, indicating that they might be better strained on STO substrates. Mosaicity of SRO deposited at 620 °C was much smaller than that of other three.

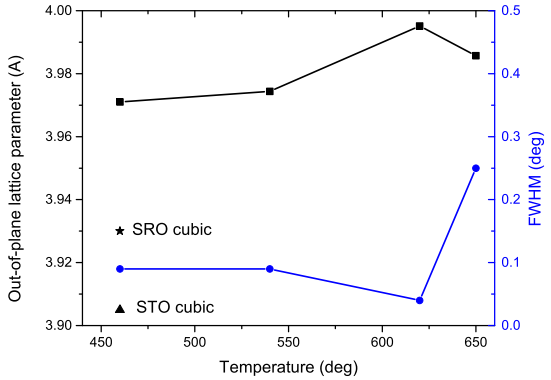

Figure 3.5: Out-of-plane lattice parameters and mosaicity of SRO deposited at different temperatures.

Surface morphologies, as shown in Figure 3.6, revealed that SRO surfaces exhibited islands of more than 10 nm in height on films deposited at 460 °C and 540 °C. The roughness (root-mean-square, RMS) of these two films were 3.23 nm and 7.03 nm, respectively. SRO film deposited at 620 °C exhibited flat surface with RMS of 0.36 nm. The film deposited at the highest temperature (675 °C) had a RMS of 1.90 nm with peak-to-valley of $3 \sim 6$ nm.

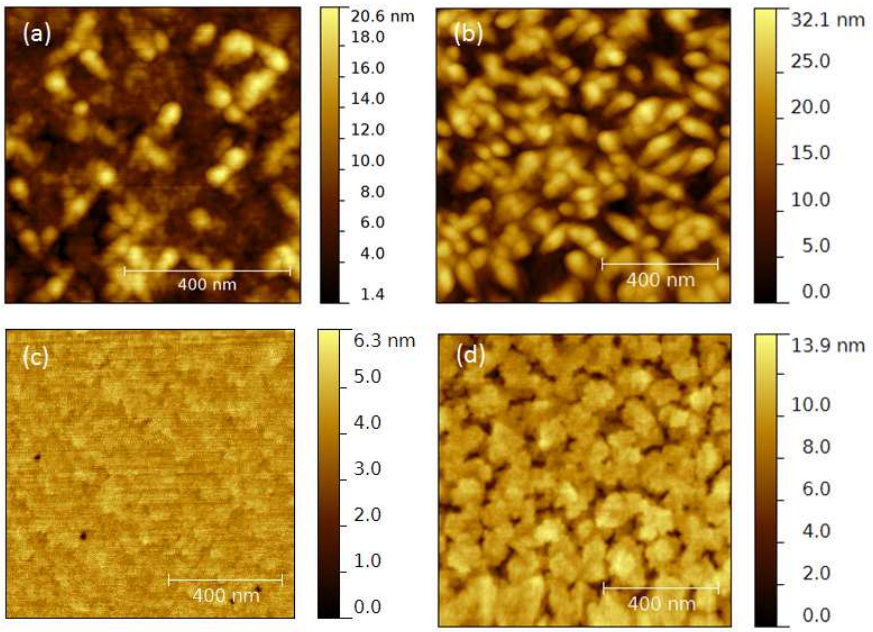

Figure 3.6: Surface morphologies of SRO films deposited at the substrate temperature of (a) 460 °C; (b) 540 °C; (c) 620 °C; (d) 675 °C.

Other deposition parameters such as plasma voltage, pressure and gas composition have also been examined. At 620 °C ∼ 650 °C, plasma voltage mainly affects the deposition rate (higher voltage higher deposition rate) and has little influence in crystalline quality and surface morphology (results shown in next section); chamber pressure has been varied from 0.005 *mbar* to 0.1 *mbar*, and deposition rate was found to be inversely proportional to chamber pressure, as shown in Figure 3.7. One possible reason is that as pressure increases the amount of flux increases correspondingly and the mean free path for sputtered species from the target is reduced. As a result, more collisions occur before the sputtered species reach the substrate, thus reducing the deposition rate. In this study, process pressure was kept at 0.005 *mbar* for all SRO film growth; Oxygen proportion has been tested from 9.1% to 20%, but no obvious difference has been observed.

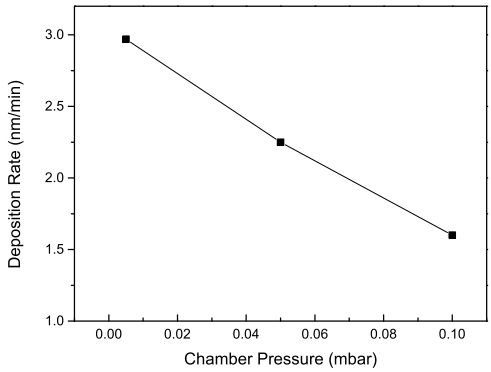

Figure 3.7: Deposition rate at different chamber pressures. All three SRO film were deposited at 620 °C ∼ 650 °C, with voltage of 173 *V* and gas composition of 50 *sccm* Ar / 5 *sccm* O_2.

Based on the studies above, the standard sputtering condition for SRO is: voltage, 109 *V*; substrate temperature, 620 °C;[7] chamber pressure, 0.005 *mbar* and gas composition, 50 *sccm* Ar /5 *sccm* O_2. The deposition rate is ∼ 1.4 *nm/min*.

3.2.3 Growth of SRO with Terraces on Vicinal STO

Since interface significantly influences the properties of thin film and the density of defects, the importance of preparing a flat SRO surface for the subsequent growth of PZT can never be overemphasized. A great effort has been put to produce SRO with terraces of single unit cell in height. As stated, lower plasma voltage can reduce the deposition rate, allowing the attached atoms on the substrate have more time to reorganize, thus reducing the surface roughness. But lower deposition rate also means that the film is kept at high temperature for longer time, which may cause Sr to emerge to the surface, hence making the deposition rate inhomogeneous at different locations (Koster *et al.* 2012).

In order to find the suitable deposition rate to grow SRO film with terraces of single unit cell

[7] When we deposited SRO as bottom electrode in following sections, all SRO were deposited at a temperautre between 620 °C and 650 °C. The reason we did not always use the optimal temperature (620 °C) is that we found this result after we started fabricating PZT capacitors. The quality degradation of SRO deposited at 640 °C ∼ 650 °C was very small for film of less than 30 *nm* on vicinal STO.

in height as bottom electrode, three SRO depositions of $\sim 10\ nm$ have been processed on vicinal STO substrates using the standard sputtering condition mentioned in previous section except that the voltage was changed to achieve different deposition rates. Plasma voltages were 70 V, 87 V and 109 V respectively for the three depositions. Out-of-plane $2\theta/\omega$ scan and rocking curve measurements have been performed for these SRO films, as shown in Figure 3.8. $2\theta/\omega$ scan unveiled only $(00l)$ oriented SRO grown on STO substrate for all three films. Intensity of SRO (002) peaks in $2\theta/\omega$ scans were very similar, indicating same amount of SRO were crystallized. However the rocking curve showed that SRO film deposited at 70 V had much lower mosaicity. Out-of-plane lattice parameters and mosaicities are shown in Table 3.1. As plasma voltage decreases, deposition rate dropped significantly and out-of-plane lattice parameter c_{SRO} slightly decreased.

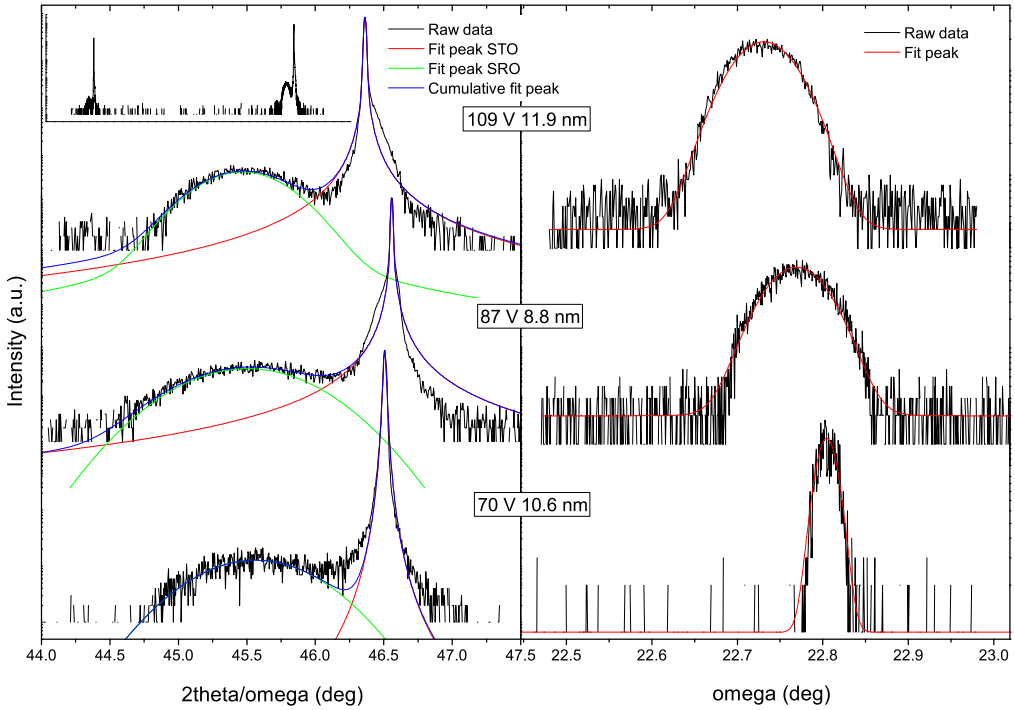

Figure 3.8: Out-of-plane $2\theta/\omega$ scans and rocking curves of SRO deposited at different voltages. Insect shows $2\theta/\omega$ scan of SRO deposited at 109 V from 20 ° to 50 °.

Deposition rate was greatly influenced by plasma voltage. Every drop of $\sim 20\ V$ reduced the deposition rate in $\sim 50\%$ (see Table 3.1). At 70 V, deposition rate was only 0.228 nm/min.

Surfaces of all three films (in Figure 3.9) showed terraces with single unit cell in height. The terraces of the film deposited at 70 V were slightly more obvious than that of the other two. The roughness of three films were all $\sim 0.3\ nm$, as shown in Table 3.1.

Bottom electrode for a PZT capacitor thickness is usually between 20 nm and 100 nm (Vrejoiu *et al.* 2006, Sambri *et al.* 2012, Eom *et al.* 1993, Bruchhaus *et al.* 1991).[8] As $\sim 10\ nm$ SRO is not

[8] Lee *et al.* (2007) deposited PZT(20/80) on 4-nm-thick SRO coated STO and obtaines square hysteresis loops with remnant polarization of 85 $\mu C/cm^2$.

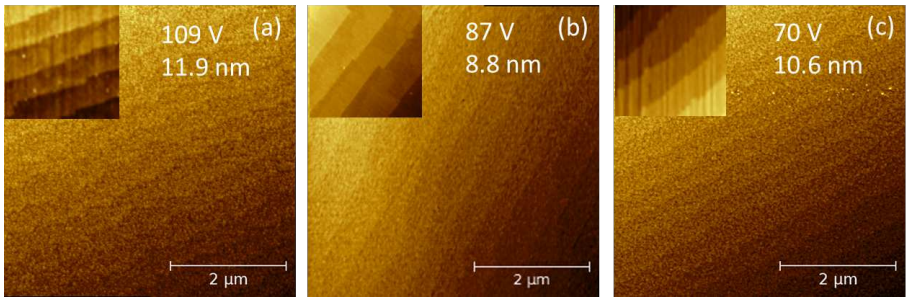

Figure 3.9: Surface morphologies of SRO films deposited on vicinal (001) STO substrates. (a) 11.9 *nm* SRO deposited at 109 *V*; (b) 8.8 *nm* SRO deposited at 87 *V*; (c) 10.6 *nm* SRO deposited at 70 *V*; (all films were deposited at 650 °C with chamber pressure of 0.005 *mbar* and a gas composition of 50 *sccm* Ar and 5 *sccm* O_2). Insets show the corresponding STO surface morphologies after chemical treatment.

Table 3.1: Lattice parameters, surface morphologies, deposition rate of SRO of ∼ 10 *nm* deposited at different plasm voltages.

Voltage (V)	Thickness (nm)	RMS (nm)	Deposition rate (nm/min)	c_{SRO} (Å)	FWHM (°)
109	11.9	0.27	0.992	3.987	0.09
87	8.8	0.34	0.489	3.983	0.08
70	10.6	0.35	0.228	3.980	0.03

thick enough for the use of bottom electrode, several thicker SRO films were deposited on vicinal STO substrates to investigate the maximum achievable thickness of SRO film with terraces of single unit cell in height. As shown in Figure 3.10, at 109 *V*, after deposition of 18.9-*nm*-thick SRO, terraces disappeared. At 70 *V*, SRO of 27.7 *nm* exhibited clear terraces of single unit cell in height, but terraces disappeared when the thickness increased to 32.8 *nm*. At this deposition condition, the maximum thickness of SRO film with terraces of single unit cell in height is ∼ 30 *nm*. Deposition rate, surface roughness, out-of-plane lattice parameter and FWHM can be found in Table 3.2.

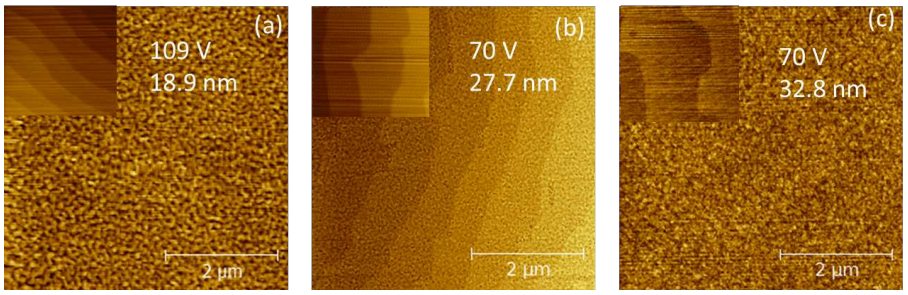

Figure 3.10: Surface morphologies of SRO of (a) 18.9 *nm* deposited at 109 *V*; (b) 27.7 *nm* deposited at 70 *V*; (c) 32.8 *nm* deposited at 70 *V*. All deposition were carried out at 650 °C, and thickness were measured by XRR. The insets show the corresponding surface morphologies after chemical treatment of STO substrates.

Since 27.7 *nm* was approaching the maximum thickness at which terraces could be achieved, terraces were not achieved every time though the deposition conditions were kept same. If we continue lowering the plasma voltage, deposition duration will be too long (it took 100 *min* to deposit the 27.7-*nm*-thick SRO film).

Koster *et al.* (1999), Bachelet *et al.* (2008) demonstrated an effective method to grow thick films with terraces of single cell in height without decreasing deposition rate by PLD. The crucial step is to

Table 3.2: Parameters extracted from XRD and AFM and deposition rates.

Thickness (nm)	Voltage (V)	Deposition rate (nm/min)	RMS (nm)	Peak-to-Valley (nm)	c_{SRO} (Å)	FWHM (°)	Terrace
18.9	109	1.050	0.45	1-2	4.004	0.09	
27.7	70	0.277	0.54	1-2	3.984	N/A	√
32.8	70	0.273	0.52	1-1.5	3.999	0.10	
35	70	0.269	0.24	0.3-1.5	3.986	0.10	√

intervene intervals every several minutes into the deposition process. At the start of the deposition, large numbers of 2D nuclei form small islands on the surface. Due to the limited mobility of the adatoms and short-time for relaxation, after the arrival of new atoms, the growth mode changes from layer-by-layer mode to multilevel 2D growth mode, forming larger islands. With the increasing surface roughness, finally film is growing in 3D mode. An interval following a period of deposition allows the adatoms to have more time for relaxation and keep the surface smoothness. The island size is kept small and multilevel growth is prevented. Bachelet achieved ~ 60 nm SRO with terraces of single unit cell in height.

A deposition of SRO film during 130 min at 70 V with 15 min interval was carried out. During the 15 min interval, the plasma was stopped and other conditions (pressure, gas composition and substrate temperature) were kept unchanged. Figure 3.11 shows the surface morphology of this film. Terraces of single unit cell were clear. The surface roughness was only 0.24 nm, smaller than the 27.7-nm-thick SRO deposited without interval. And grain size was smaller than that of the 27.7-nm-thick one (from smaller scale of AFM results, not provided here). Extracted data of deposition rate, roughness and FWHM are shown in Table 3.2.

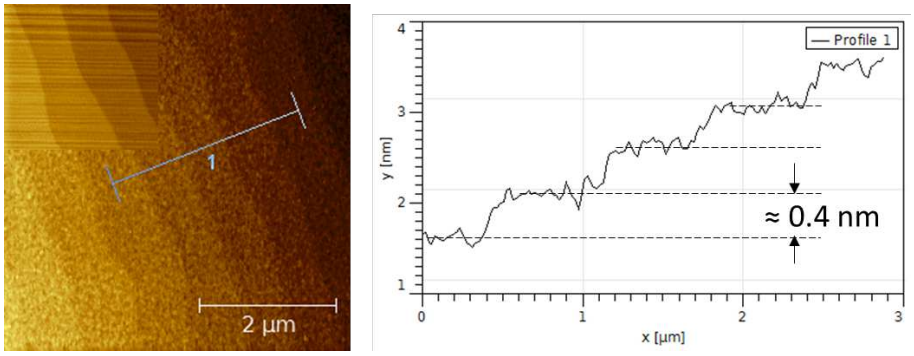

Figure 3.11: Surface morphologies of 35 nm SRO deposited during 130 min with a 15 min interval in the middle. The insect shows the surface morphology after chemical treatment of STO substrate.

Figure 3.12 shows the XRR result of this SRO film. Fitted curve revealed that the bottom SRO layer (deposited before the interval) had a slightly bigger thickness (17.8 nm) than the top SRO layer (17.2 nm, deposited after the interval). This is probably because the growth on the vicinal STO substrate was slightly easier than on the relatively rougher SRO surface at the beginning of the second half deposition. According to the XRR fitting result, the alternating peak intensities indicated that the density of top SRO layer (deposited after the 15 min interval) was about 9% higher than that of the bottom one.

Reciprocal space mapping (RSM) around the (103) reciprocal lattice points were performed (Fig-

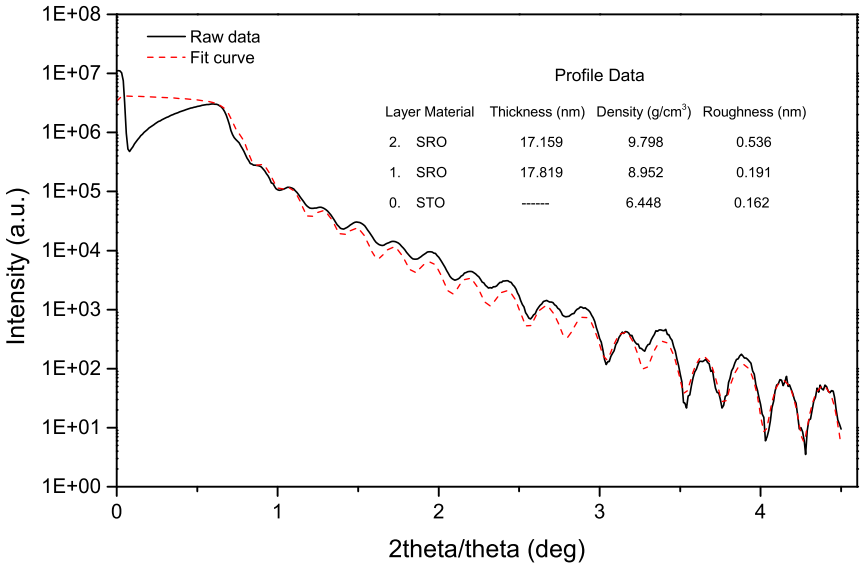

Figure 3.12: XRR result and fitting to 35-*nm*-thick SRO deposited during 130 *min* with 15 *min* interval in the middle.

ure 3.13). The in-plane lattice parameter of the SRO deposited with 15 *min* interval was slightly smaller than that of the 27.7 *nm* SRO film deposited without interval, and was almost as same as that of STO substrate, indicating that SRO deposited with interval was almost totally strained on STO substrate.

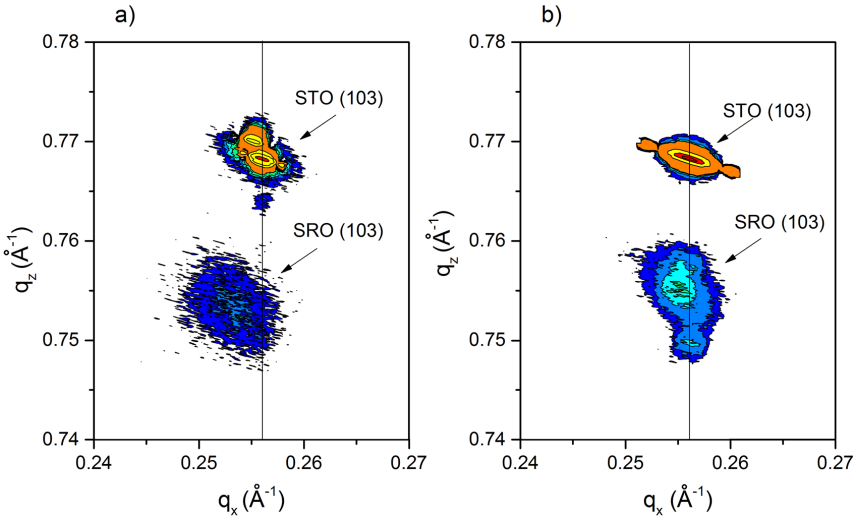

Figure 3.13: RSM around (103) reciprocal lattice points of a) 27.7 *nm* SRO deposited during 100 *min*; b) 35 *nm* SRO deposited during 130 *min* with 15 *min* interval in the middle. Both SRO were deposited at 70 *V* at 650 °C substrate and shows terraces of single unit cell in height.

With more intervals, deposition at higher rate can achieve same quality of SRO film of same thickness.

Table 3.3: Thickness, deposition conditions and morphology parameters of SRO bottom electrodes.

	PZT Thickness (nm)	SRO Thickness (nm)	Voltage (V)	Deposition Rate (nm/min)	RMS (nm)	Peak-to-Valley (nm)	Terrace
Sputtering	40.5	27.5	70	0.275	0.63	$1.5 \sim 2$	
	120.6	26	70	0.260	0.63	$1.5 \sim 2$	
	136	25.5	70	0.255	0.66	$1.5 \sim 2$	
	190	35	70	0.269	0.24	$0.3 \sim 1.5$	$\surd$
Sol-gel	33	~ 85	109				
	67	85	109	1.417	0.84	$1 \sim 3$	
	100	~ 85	109				
	133	~ 85	109				
	200	~ 85	109				

3.2.4 SRO Growth as Bottom Electrode

Nine SRO films were deposited on vicinal STO substrates as bottom electrodes for PZT capacitors (four was later used for sputtered PZT capacitors and five for sol-gel-derived PZT capacitors). For the three thinner sputtered PZT capacitor, SRO of $\sim$ 26 nm[9] were deposited (at same condition as in Figure 3.10 (b), but no terraces were observed), and SRO of 35 nm (with terraces, same sample as shown in Figure 3.11) was deposited for 190-nm-thick PZT capacitor. For all five sol-gel-derived PZT capacitors, SRO of $\sim$ 85 nm[10] were deposited. Table 3.3 presents the detailed SRO thicknesses for all nine capacitors.

SRO deposited at same condition showed almost identical surface morphology, only one topography is provided. Figure 3.14 a) shows the surface morphology of SRO used for 40.5-nm-thick, 120.6-nm-thick and 136-nm-thick sputtered PZT capacitors; Figure 3.14 b) for 190-nm-thick sputtered PZT capacitor; Figure 3.14 c) for five sol-gel-derived PZT capacitors. The 35-nm-thick SRO (with terraces) exhibited smaller grains compared to the islands in other SRO surfaces. Its surface roughness (RMS) was also smaller than others, as shown in Table 3.3 with growth parameters and peak-to-valley values.

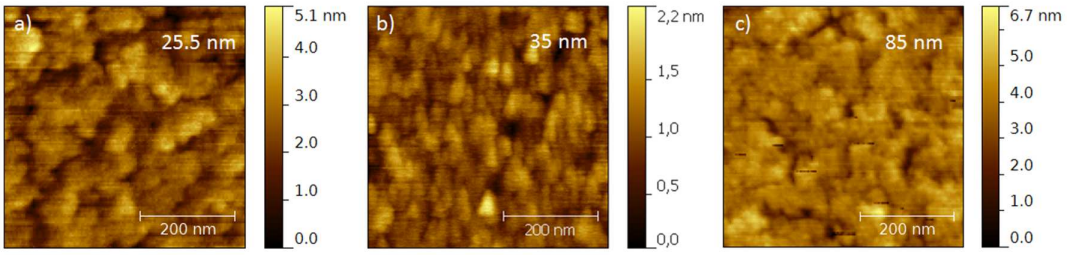

Figure 3.14: Surface morphologies of SRO bottom electrode for a) 40.5-nm-thick, 120.6-nm-thick and 136-nm-thick sputtered PZT capacitors; b) 190-nm-thick sputtered PZT capacitor; c) five sol-gel-derived PZT capacitors.

Out-of-plane $2\theta/\omega$ scan was performed after the deposition of PZT layer and will be provided in

[9] All three SRO films were deposited at the same time, thickness exhibited $\sim$1.5 nm variation due to the different location on the substrate holder.

[10] XRR measurement was performed to one of these five films. The thickness variation is within 2 nm according to our previous depositions at the same condition.

next section with that of PZT in Tables 3.4 and 3.6.

The resistivity of the 85-nm-thick SRO was measured by 4-point probes method. Linear relationship of the applied current and the measured voltage was observed in the whole measurement range. The extracted resistivity was 300 $\mu\Omega \cdot cm$, which was in agreement with reported result (Klein *et al.* 1996).

3.3 PZT Growth by Sputtering

In recent years, high quality hetero-epitaxial PZT films have been achieved through PLD by several groups (Ramesh *et al.* 1991, Vrejoiu *et al.* 2006, Lee *et al.* 2008). In this study, sputtering has been chosen as the growth route for its larger coverage than PLD. The PZT sputtering started from the optimization of deposition conditions.

3.3.1 Optimization of PZT Growth by Sputtering

At the beginning, attempts have been tried to grow monocrystalline PZT directly by varying deposition conditions (plasma voltage, substrate temperature, chamber pressure, gas composition). However the deposited PZT film turned out to be amorphous regardless of deposition condition. Thus a post annealing was always required to realize the transformation form amorphous phase to crystalline phase.

3.3.1.1 Temperature Influence

Temperature is the most crucial parameter, because at too low substrate temperature absorbed species on the substrate surface have less energy to diffuse, making a good crystallization difficult during the subsequent annealing process (Li *et al.* 2009) and too high substrate temperature will cause lead evaporation in the form of PbO, resulting in the formation of pyrochlore phase (Dana *et al.* 1991, Lee *et al.* 1996, Chen and Chen 1998). Six PZT films were deposited on 85-nm-thick SRO coated STO substrates with substrate temperature varying from room temperature[11] to 650 °C. All PZT were deposited at 71 V during 20 min. The gas composition was 50 $sccm$ Ar and no oxygen. The chamber pressure was 0.005 $mbar$. The thicknesses were about 60 $\sim$ 80 nm, and the thickness showed an inverse temperature dependence.

Out-of-plane $2\theta/\omega$ scans were performed for all six samples both before and after a rapid thermal annealing (RTA) at 650 °C during 30 s in oxygen. Before RTA, no crystalline PZT phase was observed except the one deposited at 650 °C, in which a pyrochlore phase was observed around 33.9 °. Figure 3.15 shows out-of-plane $2\theta/\omega$ scan of these six samples after RTA. PZT deposited from room temperature to 540 °C all crystallized in (00l) direction after RTA. The pyrochlore phase in PZT deposited at 650 °C remained after RTA, although Kwok and Desu (1992) has reported RTA could change pyrochlore phase into perovskite phase.

[11] Room temperature refers to the condition that the heater is off.

Focusing on the PZT (002) peak, its highest intensity appeared in the PZT deposited at 150 °C and 300 °C. At room temperature and 460 °C, its intensity decreased slightly. As substrate temperature increased to 540 °C, only a fraction of amorphous PZT phase transfered to crystalline phase by RTA.

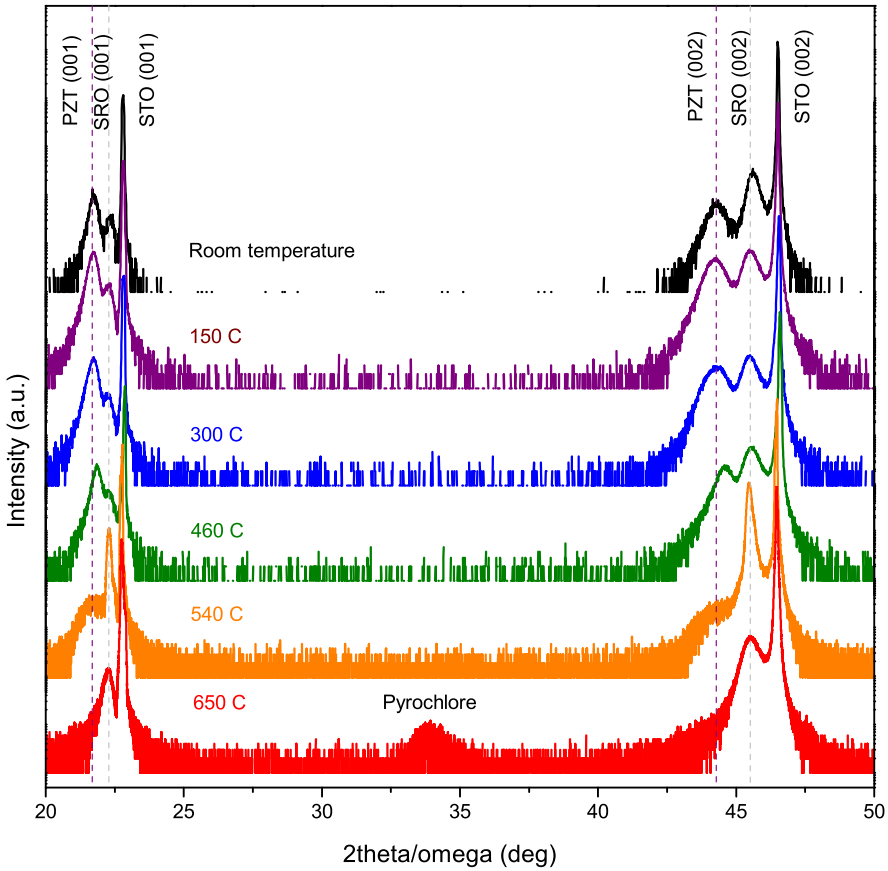

Figure 3.15: Out-of-plane $2\theta/\omega$ scans of PZT films deposited at different temperatures during 20 *min* on 85-*nm*-thick SRO on as-received (001) STO substrates. Deposition parameters as follows, voltage: 71 *V*; chamber pressure: 0.005 *mbar*; flux: 50 *sccm* Ar and 0 *sccm* O_2.

Figure 3.16 presents the rocking curves of these PZT films. FWHM were 1.58, 1.71, 2.60, 1.85 for PZT deposited at 150 °C, 300 °C, 460 °C and 540 °C, respectively. The mosaicity of PZT deposited at 460 °C is larger than the other three.

The leakage current measurement of these PZT as capacitor with an area of 100 × 100 μm^2 was performed, showing that only the PZT deposited at 300 °C was well insulated and all other five capacitors were leaky. Thus 300 °C was chosen as the substrate temperature for later growth of sputtered PZT capacitor.

3.3.1.2 Gas Composition Influence

The influence of gas composition has also been investigated. In the previous section, all the six PZT films were deposited in 100% Ar atmosphere. Another two PZT were deposited, one in 20% O_2/80% Ar and another in 100% O_2 to compare with the previous ones. Other deposition parameters and deposition

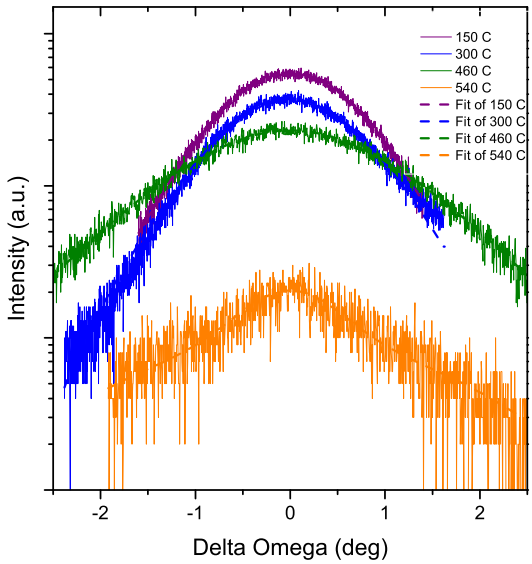

Figure 3.16: Rocking curves around (002) of PZT films deposited at different temperatures during 20 *min* on 85-*nm*-thick SRO on as-received (001) STO substrates.

duration were kept same (70*V*, 0.005 *mbar*, 300 °C, 20 *min*). Figure 3.17 shows the out-of-plane $2\theta/\omega$ scan results of these two PZT films after RTA. No crystalline PZT phase formed when the sputtering gas contained 20% O_2. When the sputtering gas contained only O_2, only a fraction of PZT formed perovskite structure and a small amount of pyrochlore phase was also observed.

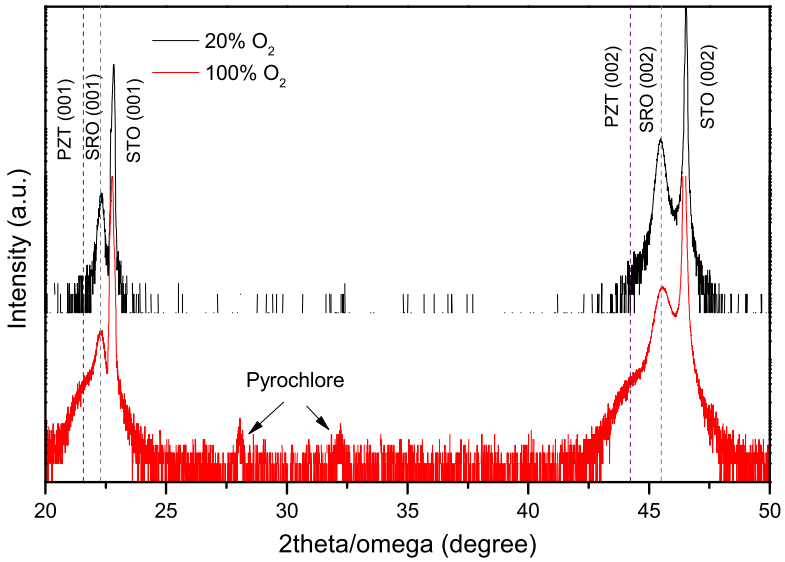

Figure 3.17: Out-of-plane $2\theta/\omega$ scans of PZT deposited in two different gas compositions: 20% O_2/80% Ar; 100% O_2. At both conditions the total gas flux quantity was kept at 50 *sccm*.

The gas composition had a huge impact on the crystallization process. 100% Ar (50 *sccm*) was chosen as standard PZT sputtering condition.

3.3.1.3 Plasma Voltage Influence

Plasma voltage has also been modified to investigate its influence on the crystallization of PZT. One PZT film of 91 nm was deposited at 50 V (during 163 min) and another of $\sim$ 40 nm was deposited at 138 V (during 19 min), both followed by RTA. Substrate temperature was 300 °C and other parameters were kept same as in Section 3.3.1.1. Figure 3.18 shows the out-of-plane $2\theta/\omega$ scan results of these two PZT films after RTA. At 50 V, crystalline PZT (00l) was formed and its intensity was high, indicating large amount amorphous PZT was crystallized after RTA. At 138 V, PZT (00l) was formed, accompanied with several different pyrochlore phases, which were formed due to the low surface mobility at high deposition rate (Scott 2000). The out-of-plane lattice parameter c_{PZT} of PZT deposited at 50 V extracted from PZT (002) peak was 4.067 Å, much smaller than PZT deposited at 71 V in section Section 3.3.1.1, which was 4.089 Å. It indicated that PZT deposited at 50 V was probably more relaxed due to the low deposition rate. c_{PZT} of PZT deposited at 138 V was 4.091 Å.

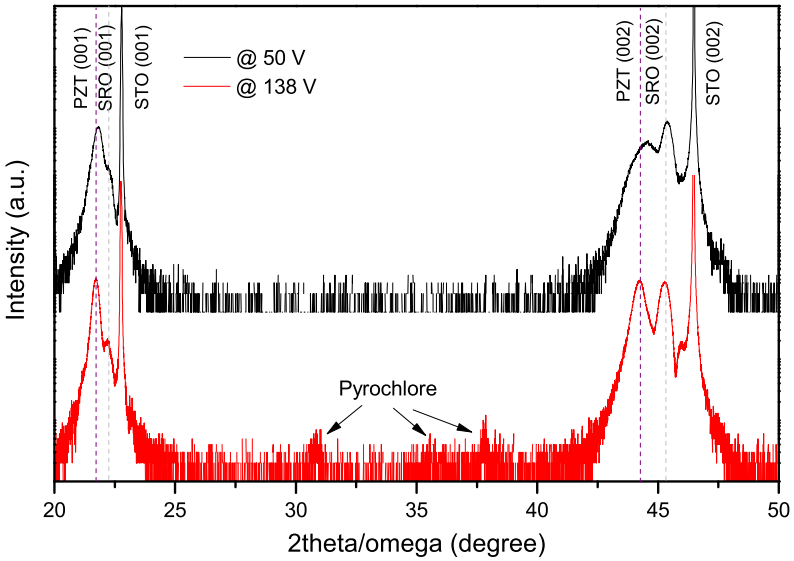

Figure 3.18: Out-of-plane $2\theta/\omega$ scans of PZT deposited at 50 V and at 138 V. The peak at 46° corresponds to bulk SRO, which might be the result of PZT bombardment on the SRO surface at high plasma voltage.

Compared to SRO sputtering, plasma voltage showed much greater impact in crystallization in PZT sputtering. 71 V was chosen as the PZT plasma voltage.

3.3.2 Growth and Structural Characterization of Sputtered PZT

After modifying the substrate temperature, gas composition and plasma voltage (chamber pressure has not been varied, a typical pressure of 0.005 $mbar$ was applied to PZT sputtering process), four PZT films of different thicknesses from 40.5 nm to 190 nm were deposited on SRO/STO. The miscut angle of these STO substrate is $\sim$ 0.05°. Different thicknesses were achieved by adjusting the deposition duration. Deposition condition was: at 71 V, in a 0.005 $mbar$ chamber with 50 $sccm$ Ar on 300 °C substrates.

Table 3.4: Out-of-plan lattice parameters and mosaicities of sputtered PZT films and underlying SRO films.

PZT Thickness (nm)	SRO Thickness (nm)	c_{PZT} (Å)	c_{SRO} (Å)	FWHM (PZT) (°)	FWHM (SRO) (°)
40.5	27.5	4.070	4.000	1.30	0.10
120.6	26	4.093	4.001	1.08	0.10
136	25.5	4.084	4.009	1.01	0.11
190	35	4.084	3.978	1.20	0.09

Out-of-plane 2theta/omega scans and rocking curve measurements were carried out for these four PZT films, presented in Figure 3.19. All these PZT films were mono-crystalline in (00l) direction. No pyrochlore phase was observed. Out-of-plane lattice parameters and FWHM were extracted from PZT (002) peaks, as shown in Table 3.4. All PZT films had similar out-of-plane lattice parameter. Mosaicity of these films were also similar.

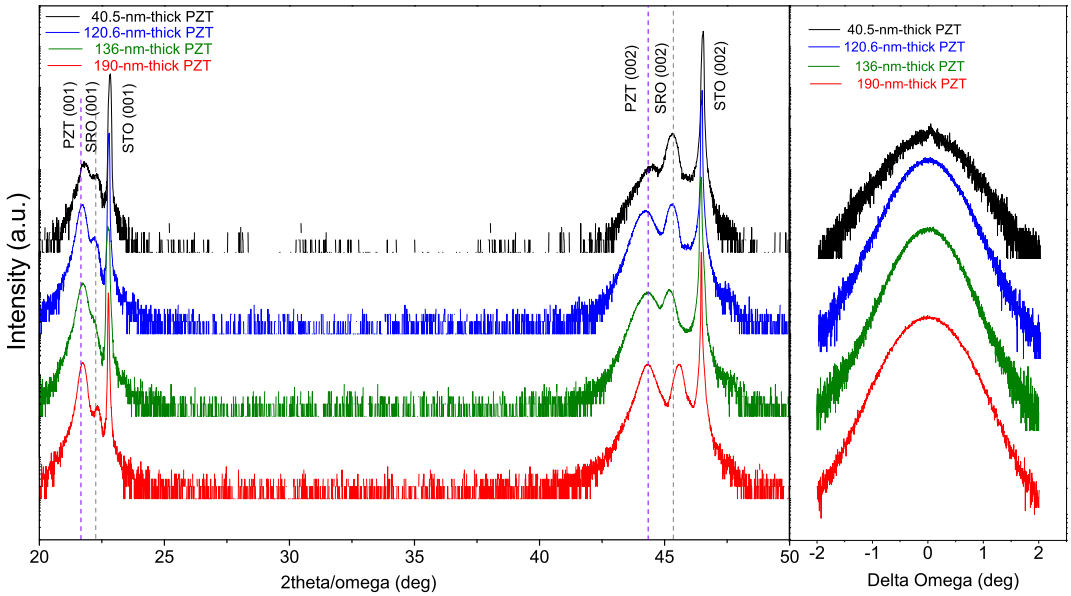

Figure 3.19: Out-of-plane $2\theta/\omega$ scans and rocking curves around (002) of PZT films of different thicknesses deposited on SRO/STO. Out-of-plane $2\theta/\omega$ scan was carried out from 20° to 50° and no pyrochlore phase was observed.

ϕ scan of 360° around (103) plane of STO, SRO and PZT was performed for the 190-nm-thick sputtered capacitor, as shown in Figure 3.20. The overlapping of the four peaks from one material on the peaks of the other materials indicated that both the PZT layer and SRO layer were grown epitaxially.

For the 190 nm PZT film, RSM was performed around the (103) reciprocal lattice points, as shown in Figure 3.21. The in-plane lattice parameter a_{PZT} and out-of-plane lattice parameter c_{PZT} extracted from this figure were 4.075 Å and 4.084 Å, respectively.

Surface morphologies of these four sputtered PZT are presented in Figure 3.22 (surface morphologies of underlying SRO is shown in Figure 3.14 a) and b)). Roughness (RMS) of all four PZT films were less than 1 nm. Grain size of these 4 PZT films were almost identical, $20 \sim 30$ nm. Parameters extracted from AFM measurements are presented in Table 3.5.

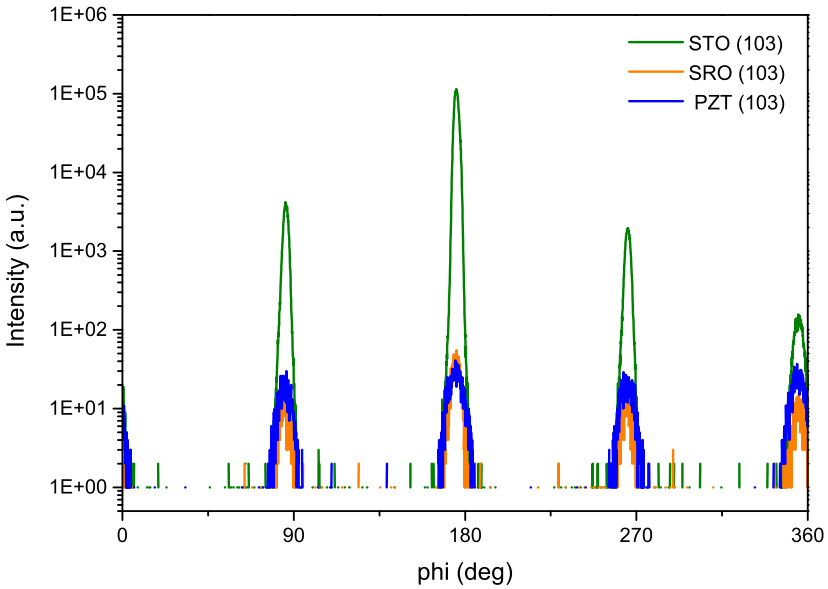

Figure 3.20: 360° ϕ scan of (103) plane of STO substrate, SRO layer and PZT layer of 190-nm-thick sputtered capacitor.

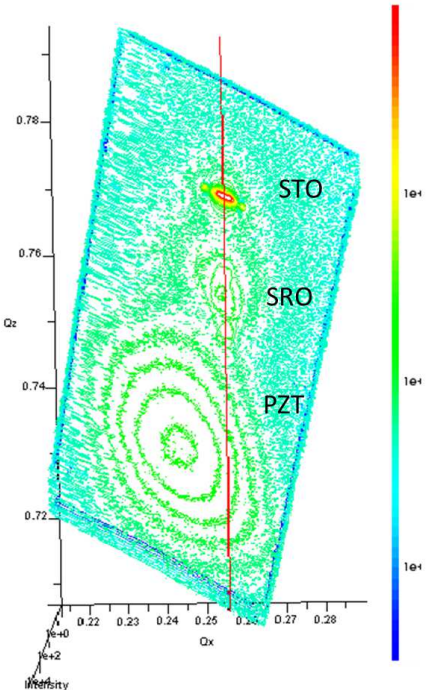

Figure 3.21: RSM around (103) reciprocal lattice points for 190-nm-thick sputtered PZT sample.

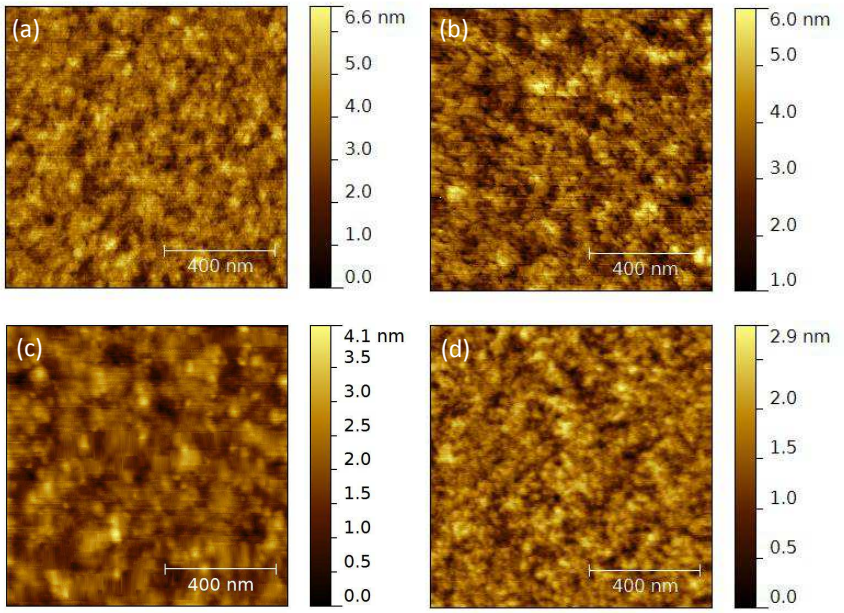

Figure 3.22: Surface morphologies of sputtered PZT of various thicknesses. All topographies were obtained before the deposition of top electrode except 136-nm-thick PZT which was measured after the deposition of top electrode.

Since 190-nm-thick PZT was deposited on a SRO film with terraces of single unit cell in height, its PZT surface roughness was smaller than other three thinner PZT films. And blurred terraces[12] with same width was observed, as shown in Figure 3.23. As PZT thickness was about 50 times of the unit cell height and surface peak-to-valley value was even larger than unit cell height, the observed blurred terraces of the same form before deposition indicated that the growth mode of PZT in this deposition condition was layer-by-layer.

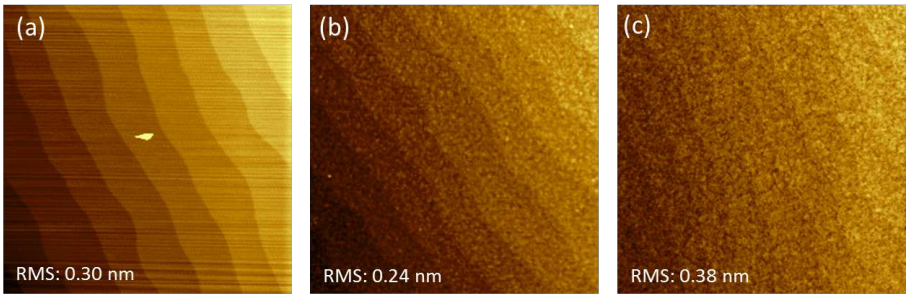

Figure 3.23: Surface morphologies of 190-nm-thick PZT capacitor: (a) substrate after chemical treatment; (b) after deposition of 35-nm-thick SRO during 130 min with 15 min interval in the middle; (c) after deposition of 190-nm-thick PZT. (scanning area: 5 $\mu m \times 5\ \mu m$)

3.4 PZT Growth by Sol-gel

Sol-gel process for growing PZT film was the most widely used method since 1980s for its simplicity, low cost and large area coverage (Yi *et al.* 1988, Dey and Zuleeg 1990, Melnick *et al.* 1990). The growth

[12] More than 10 topographies were measured at different locations of this PZT film and all showed blured terraces.

Table 3.5: Surface morphology parameters of sputtered PZT films of different thicknesses (surface roughness before the deposition of PZT is presented here also).

PZT thickness (nm)	SRO thickness (nm)	RMS (SRO) (nm)	RMS (PZT) (nm)	Grain Size (nm)	Peak-to-valley (nm)
40.5	27.5	0.63	0.77	$20 \sim 30$	$1 \sim 3$
120.6	26	0.63	0.73	$20 \sim 30$	$1 \sim 2.5$
136	25.5	0.66	0.48	$20 \sim 30$	$1 \sim 1.5$
190	35	0.24	0.38	$20 \sim 30$	$0.4 \sim 1.8$

conditions have been highly developed. In this work, PZT film was also fabricated through sol-gel method to compare with sputtered PZT.

3.4.1 Optimization of PZT Growth by Sol-gel

The growth procedure of PZT by sol-gel solution is only slightly modified according to the suggested procedure by sol-gel solution supplier *Mitsubishi Materials* (see flowchart in Figure 2.2). Acceleration and rotational speed of spin coating have been tested on STO substrates before growing PZT capacitors.

Firstly, acceleration rate is an important parameter, concerning the solution diffusion process. At low acceleration from 500 $rpm/s \sim 2000$ rpm/s, the solution could not totally diffuse over the surface, and it turned out to be a visible bumpy topography. A high acceleration 5000 rpm/s was chosen for the spin coating procedure.

Secondly, rotational speed of 6000 rpm, 3000 rpm and 1500 rpm have been tested. It turned out that rotational speed not only had an effect on the thickness of the film, but also led to the formation of different phases. A separation of phase was observed at lower rotational speed. XRD analysis indicated a rotation-dependent structural phase, i.e., a phase transition from tetragonal phase for the 6000 rpm film to a bi-phase (tetragonal + pseudo-cubic[13]) structure for the 3000-rpm and 1500-rpm films. RSM around (103) reciprocal space points are provided in Figure 3.24. The thickness of 6000-rpm, 3000-rpm and 1500-rpm PZT film were 33 nm, 45 nm and 65 nm, respectively. Ellipsometry pointed out the stoichiometric ratio of Ti/Zr decreased from bottom to top for the 1500 rpm grown thicker PZT (Liu *et al.* 2014).

For the purpose of producing monocrystalline PZT, rotational speed of 6000 rpm was chosen as standard procedure. Each rotational cycle lasted 15 s as the suggested procedure. After every spin coating, the sol was dried on a heater at 325 °C for 5 min. A post annealing was carried out after each $3 \sim 4$ spin coating cycles at 650 °C in oxygen for 1 min (see process flowchart in Figure 2.2).

3.4.2 Growth and Structure Characterization of Sol-gel-derived PZT

Four PZT films of different thicknesses were deposited on the 85-nm-thick SRO (shown in Figure 3.14 c)) with the conditions described in previous section. The thicknesses were simply controlled by varying

[13]The corresponding phase in bulk PZT of the same composition is rhombohedral phase.

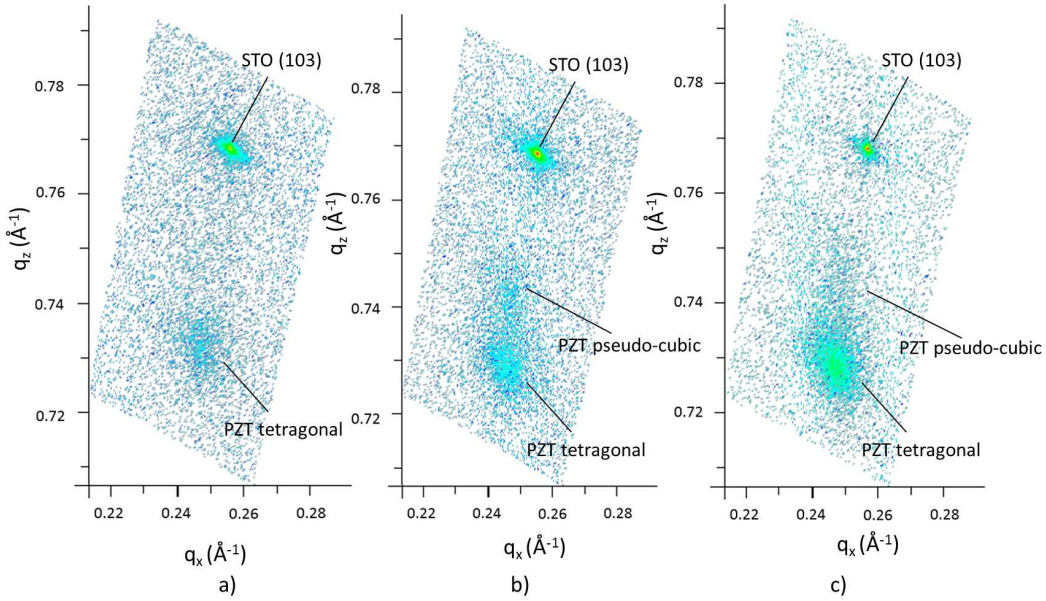

Figure 3.24: RSM around (103) reciprocal lattice points of PZT deposited at the rotational speed of a) 6000 *rpm*; b) 3000 *rpm*; c) 1500 *rpm*.

the numbers of spin coating cycle. Four depositions of 1, 2, 4 and 6 cycles were carried out and the corresponding thicknesses[14] are 33 *nm*, 67 *nm*, 133 *nm* and 200 *nm*. For the 33 *nm*, 67 *nm* and 133 *nm* PZT, only one RTA was carried out after required thickness was obtained. For the 200 *nm* one, another RTA was imposed after three spin coating cycles.

Top electrode for these samples required another RTA of 1 *min* for its crystallization. To compare the influence of this 2nd annealing (1st is the annealing for PZT crystallization), another PZT of 100 *nm* was fabricated and annealed in the same way in the 1st annealing. 2nd annealing for the top electrode of this 100-*nm*-thick PZT was carried out in a tubular furnace in air during 3 *h* instead of 1 *min* RTA in oxygen.

Out-of-plane $2\theta/\omega$ scans and rocking curve measurements were carried out for these five samples, as shown in Figure 3.25. All PZT films crystallized only in $(00l)$ direction except the 100-*nm*-thick one, in which a fraction of pyrochlore phase also formed. The mosaicity of 100-*nm*-thick PZT was 1.74 °, much bigger than that of others.

A ϕ scan of 360° around (103) plane of STO, SRO and PZT was performed for the 200-*nm*-thick sol-gel-derived capacitor, as shown in Figure 3.26. The overlapping of peaks indicated that both the PZT layer and SRO layer were grown epitaxially.

Out-of-plane lattice parameters and mosaicities were extracted from Figure 3.25, as shown in Table 3.6. c_{SRO} of 100-*nm*-thick PZT sample was much smaller, compared to others and its value of 3.939 Å was close to SRO bulk value, 3.93 Å, indicating it was mostly relaxed on STO substrate. All SRO were deposited in same condition and 200-*nm*-thick PZT experienced once more RTA than others

[14]Thickness of one spin coating cycle film was measured by XRR. Thickness of multiple spin coating cycles is simply to multiply the number of cycles by 33 *nm*.

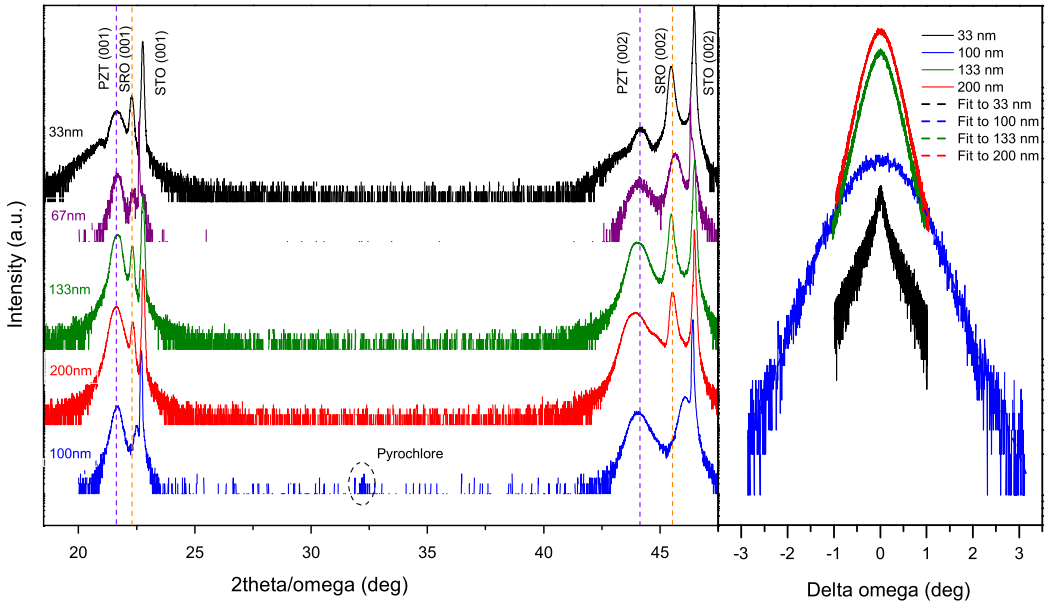

Figure 3.25: Out-of-plane $2\theta/\omega$ scans and rocking curves around (002) of sol-gel-derived PZT of different thicknesses. A small peak at 44.8° of 200-nm-thick PZT is observed, which corresponds to a-domain PZT (4.04 Å).

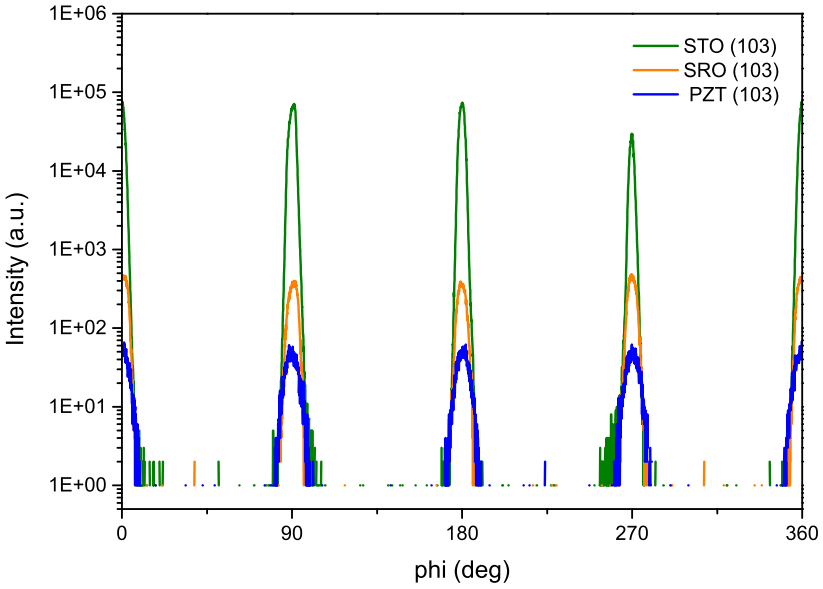

Figure 3.26: 360° ϕ scan of (103) plane of STO substrate, SRO layer and PZT layer of 200-nm-thick sol-gel-derived capacitor.

Table 3.6: Out-of-plan lattice parameters and mosaicities of sol-gel-derived PZT films and underlying SRO films.

PZT Thickness (nm)	SRO Thickness (nm)	c_{PZT} (Å)	c_{SRO} (Å)	FWHM (PZT) (°)	FWHM (SRO) (°)
33	~ 85	4.097	3.986	0.35	0.09
67	85	4.104	3.972	N/A	N/A
133	~ 85	4.110	3.984	0.73	0.06
200	~ 85	4.119	3.981	0.75	0.09
100[15]	~ 85	4.108	3.939	1.74	0.36

during the sol-gel procedure but still exhibited similar c_{SRO} as 33-nm-thick, 67-nm-thick and 133-nm-thick did. It is reasonable to attributed the abnormal c_{SRO} in 100-nm-thick PZT sample to the long annealing duration for the top electrode. During this 2nd annealing, SRO layer was thermally activated and the process of recrystallization was accompanied by relaxation. Due to this destructive annealing, the mosaicity of 100-nm-thick PZT was bigger than that of others and during the recrystallization pyrochlore phase was formed.

From Table 3.6, it is noticed that c_{PZT} increased slightly with thickness. Usually tetragonality (c/a) shows an inverse thickness dependence (Lee *et al.* 2007), due to the reducing clamping effect from the substrate on the epitaxial film. Nagarajan's work (Nagarajan *et al.* 1999 2006) on PLD-derived PZT showed that, as thickness varied under ~ 150 nm, c_{PZT} was almost stable. And as thickness continued increasing, c_{PZT} was obviously reduced in the order of 0.02 Å. Another possible reason for the stable c_{PZT} with thickness here can be derived from the varying chemical profile in sol-gel-derived PZT. Sol-gel-derived PZT usually exhibits a gradient of composition. Calame and Muralt (2007) showed within one spin coating layer of 250 nm, Zr/(Zr+Ti) ratio varied from 0.45 to 0.60. Thus from the bottom to top of each spin coating layer, tetragonality decreased as Zr/(Zr+Ti) increased. And a_{PZT} at the bottom of each spin coating layer was smaller than a_{PZT} at the top. A clamping force was applied on the top of the layer by the bottom of the layer above, thus the tetragonality was kept as thickness increased. It is also possible that the PZT might be totally relaxed, in which condition tetragonality would not change with thickness.

Surface morphologies of these five samples were measured by AFM, as shown in Figure 3.27 (surface morphologies of underlying SRO was shown in Figure 3.14 c). All samples exhibited good topography with RMS less than 1 nm except the 100-nm-thick PZT, confirming the destructive effect of the long annealing duration. Grain size of 100-nm-thick PZT was $2 \sim 3$ times bigger than that of other four samples. It can be assumed that before the 3 h annealing, 100-nm-thick PZT exhibited a similar crystalline structure and topography as others and the destructive annealing changed the PZT physical properties. Bigger grains were formed during the recrystallization.

Grain density of the 133-nm-thick PZT was much smaller compared to 33-nm-thick, 67-nm-thick and 200-nm-thick PZT. Figure 3.27 (c) was obtained before the 1 min RTA for top electrode. After

[15] Annealed for 3 h for top electrode instead of 1 min RTA, which was applied to other sol-gel-derived PZT films and sputtered PZT films.

Table 3.7: Roughness and grain size of sol-gel-derived PZT surfaces.

PZT Thickness (nm)	SRO Thickness (nm)	RMS (SRO) (nm)	RMS (PZT) (nm)	Grain Size (nm)	Peak-to-valley (nm)
33	~ 85		0.38	$10 \sim 20$	$0.5 \sim 3$
67	85	0.84	0.46	$25 \sim 35$	$1 \sim 2$
133	~ 85		0.41	$20 \sim 40$	$0.5 \sim 2$
200	~ 85		0.66	$15 \sim 20$	$0.5 \sim 2$
100	~ 85		1.63	$50 \sim 70$	$2 \sim 4$

this 2nd RTA, grain densities of the 133-nm-thick PZT was found to be at the level of 200-nm-thick PZT while performing PFM measurement. As sol-gel-derived PZT crystallizes from bottom through the thickness to top, forming columnar grains (Amanuma *et al.* 1994), the low grain density was attributed to the insufficient annealing during the sol-gel growth. The 133-nm-thick PZT only experienced once RTA for crystallization as the 33-nm-thick and 67-nm-thick PZT did and the 200-nm-thick PZT underwent twice RTA. The annealing for top electrode crystallized the amorphous phase of 133-nm-thick PZT near the surface, increasing its surface grain density. RMS results and grain sizes of these five samples are provided in Table 3.7.

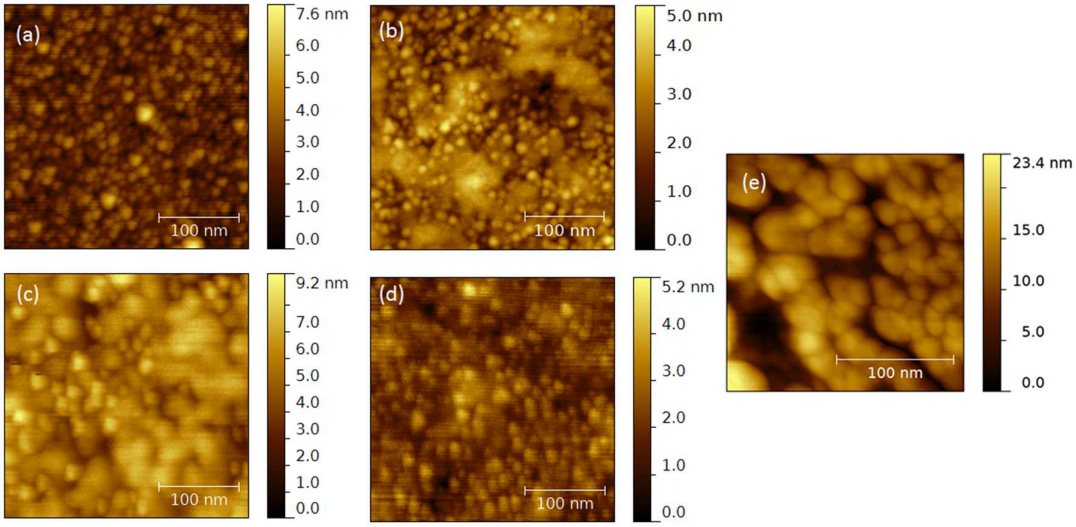

Figure 3.27: Morphologies of sol-gel-derived PZT films of (a) 33 nm, (b) 67 nm, (c) 133 nm, (d) 200 nm and (e) 100 nm .

3.5 Growth of Top Electrodes

After SRO bottom electrode and PZT film were deposited, top electrode was fabricated through reversal lift-off procedure (depicted in Figure 2.3). Three conductive materials, SRO, Pt and ITO, were employed as top electrode to investigate their influences on capacitor's electrical properties. Pintilie *et al.*'s work (2012) suggested that different top electrodes generated different amount of top interface traps, which affected the leakage current of the capacitor thus forming different ferroelectric hysteresis loops.

All three top electrodes were deposited by sputtering at room temperature. The thickness was around 150 nm. Through the reversal mask, six different sizes ($100\times100\mu m^2$, $150\times150\mu m^2$, $200\times200\mu m^2$, $300\times300\mu m^2$, $400\times400\mu m^2$, $600\times600\mu m^2$) of top electrodes were deposited in arrays. To crystallize the top electrode, SRO and Pt experienced 1 min RTA at 650 °C in oxygen, crystallizing in (00l) and (111) direction, respectively. ITO required a different annealing procedure for crystallization (Morgan *et al.* 1998, Rogozin *et al.* 2004, Higuchi *et al.* 1994). RTA at 250 °C during 1 min in oxygen was performed for ITO crystallization. In_2O_3 (222) was observed in out-of-plane $2\theta/\omega$ scan.

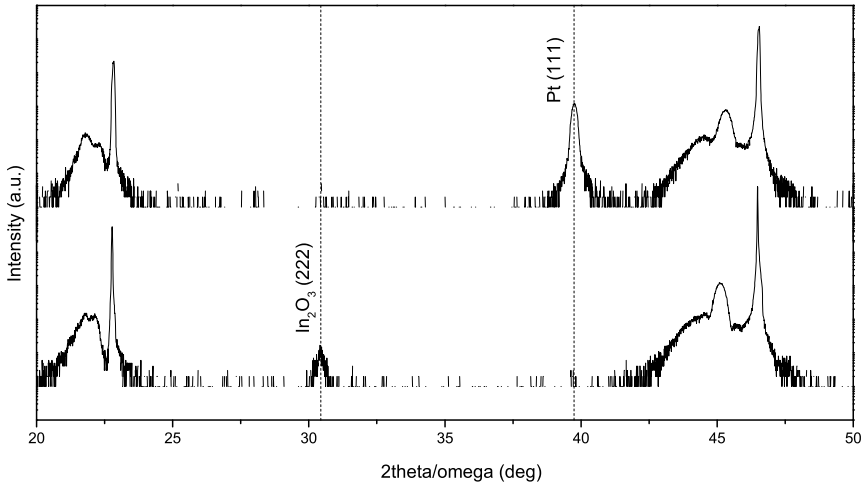

Figure 3.28: Out-of-plane $2\theta/\omega$ scan of capacitors after the deposition of top electrode.

Since the SRO top electrode was same as bottom, a sample with the stack SRO/PZT/STO was fabricated to verify the crystalline structure of the top SRO. Top SRO was found to crystalline also in (00l) direction, with reduced amount of crystal structure compared to the bottom SRO.

Due to the size of sample, only large ones (1×1 cm^2) were fabricated with three different top electrodes. For a capacitor with three types of top electrodes, the three conductive materials were deposited in the sputtering chamber by covering part of the surface. Then the samples were cut into two parts, one with ITO top electrode and another with SRO and Pt top electrodes. Two parts experienced different RTA as described above. Table 3.8 lists the top electrodes of each capacitor.

3.6 Summary

In this chapter, the growth details of PZT capacitors both by sputtering and by sol-gel have been presented. Epitaxially grown PZT were achieved both by sputtering and by sol-gel. Out-of-plane parameter c_{PZT} in sol-gel-derived PZT ($\sim$ 4.11 Å) was larger than that of sputtered PZT ($\sim$ 4.09 Å). In both cases, PZT were relaxed on SRO/STO. But the degree of relaxation was unknown. Further study of the Zr/Ti ratio in depth or deposition on a substrate with big mismatch will help understand the strain state between PZT and SRO. Mosaicity of sol-gel-derived PZT ($\sim$ 0.75°) was about 25% smaller than that of

Table 3.8: Top electrode types for each PZT capacitors.

	PZT Thickness (nm)	SRO-top	Pt-top	ITO-top
Sputtering	40.5	√	√	√
	120.6	√	√	√
	136	√	√	√
	190	√	√	
Sol-gel	33	√		
	67	√		
	133	√	√	
	200	√	√	
	100	√		

sputtered PZT.

Grain size and surface roughness of PZT morphology from both growth routes were comparable. Through sputtering, high quality PZT with layer-by-layer growth mode was achieved on a SRO film with terraces of single unit cell in height. And its surface roughness was smaller than both sputtered PZT deposited on SRO without terraces and sol-gel-derived PZT.

Sol-gel-derived PZT is highly reproducible in terms of crystal structure and surface morphology. Sputtered PZT in same conditions of various thicknesses also showed similar crystalline structure and surface morphologies and deposition rate was similar with a variation less than 10%. But several times (less than 20%), the deposition rate could decrease as big as 40%. One possible reason is that the PZT target is frequently loaded and unloaded due to the overwhelming demands for deposition of different materials. The condition of the target (like electrical contact between the target and voltage generator) may change even we keep using the same target holder. Further optimization is required to stabilize the deposition rate to improve the reproductivity of sputtered-PZT films.

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Chapter 4

Electrical Characterization

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In this chapter, firstly, leakage current of both sputtered and sol-gel-derived PZT capacitors will be presented and be fitted according to different charge transport mechanisms. Secondly, relative permittivity of these capacitors will be reported. Then, P-E loops of these capacitors will be presented,

and P_r and E_c at different fields will be shown. At last, PFM results of these ferroelectric films will be demonstrated.

4.1 Leakage Current

Leakage current is a crucial issue in ferroelectric capacitors concerning reliability such as thermal breakdown. In an ideal capacitor the conductance of an insulating film is assumed to be null. Real insulators, however, show some degree of carrier conduction when the electric field or temperature is sufficiently high (also some contributions across the interface). For a ferroelectric thin film capacitor, the leakage current can be very large, even covering the contribution of polarization. Therefore, to study the mechanism of charge transport in ferroelectric thin films is of great importance.

Ferroelectrics are often treated as insulators. Many works (Robertson 2000, Doolittle *et al.* 2003, Pintilie and Alexe 2005) regard ferroelectrics as wide bandgap semiconductors, making it easy to adapt well founded theories for semiconductors. However, how to include the semiconductivity is still a difficult problem when analyzing experimental data. Simplified models based on semiconductivity may ignore important effects or limit the range of parameters. For instance, polarization is considered as two uniform sheets of opposite charges posing at a distance ("dead" layer, non-ferroelectric) from the ferroelectric-metal interface (Dawber *et al.* 2003). Zubko *et al.*'s work (2006b) found that this assumption will become invalid when space charge level exceeds $\sim 10^{19}\, cm^{-3}$.

Typically, PZT is p-type in bulk and the metal-ferroelectric interface can be n-type due to oxygen deficiency (Yarmarkin *et al.* 2000, Smyth 1996). Scott (2000) stated that in all ferroelectric thin-film capacitors the conduction was predominantly due to electrons injected from the cathode, not due to holes, despite the p-type character of the film. But Stolichnov *et al.*'s work (1998) on Pt/PZT/Pt capacitors showed the conduction was supported by holes. Wouters *et al.* (1995) also found that the hole barrier was smaller than the electron barrier in their study on Pt/PZT/Pt capacitors.

Scott (2000) pointed out that n-type perovskite ferroelectric films could be formed when growing in reducing atmospheres. When oxygen is lost in the form of neutral O_2, it leaves behind electrons, thus the vacancies turn out to be donors. The binding energy is around 1.0 eV. In appearance n-type perovskite has a darker outlook compared to p-type.

4.1.1 Leakage Current Mechanisms

Charge transport in a metal-ferroelectric-metal (MFM) capacitor is usually complicated and composed of various mechanisms since electrons, holes and ions can all contribute to it, resulting in nonlinear integral equations for total leakage current. Among these mechanisms, many are borrowed directly from the theories for metal-semiconductor junction. Pintilie and Alexe (2005) classified these mechanisms into two groups: (i) interface-dominant mechanisms: Schottky emission and Fowler-Nordheim tunneling (FN); (ii)

Bulk-dominant mechanisms: ohmic contact, Frenkel-Poole emission (FP), space-charge-limited currents (SCLC) and ionic conduction. For an ultra-thin ferroelectric capacitor, a ferroelectric tunnel junction (FTJ) is formed and the dominant conduction mechanism is direct electron tunneling (Kohlstedt *et al.* 2005, Tsymbal and Kohlstedt 2006).

The regular method to identify which mechanism is involved in one or a series of specific samples is to fit different models to the experimental data. Sometimes more than one mechanism fit the data. Measurements at different temperatures or of different thickness samples may help further identify the conduction mechanism.

In the following sections we will first present I-V characteristics of the sputtered capacitors and sol-gel-derived ones. Then we will fit each transport mechanism[1] to our data. According to the fitting result, we will see which mechanism is compatible with the leakage current.

4.1.1.1 Interface-dominant Mechanisms

4.1.1.1.1 Schottky Emission (SE)

Schottky emission process is the carrier transport of electrons with sufficient energy to overcome the ferroelectric-electrode barrier $\Phi_B = \Phi_M - \chi$. Φ_M is electrode work function (voltage difference between its conduction band and vacuum level, around 4.8 eV for SRO (Scott 2000) and χ is electron affinity of PZT (voltage difference between its conduction band and vacuum level, around 3.5 eV (Scott 2000). Φ_M(Pt) = 5.7 eV (Michaelson 1977) and Φ_M(ITO) = 4.4 eV (Park *et al.* 1996).

However the required energy to go over the barrier is lowered due to image-field correction. Schottky attributed the phenomenon to the attraction between the electrons already injected to the ferroelectric from the cathode and the electrons still at the cathode. The lowered amount is (Sze and Ng 2006):

$$\Delta\Phi = \left(\frac{qE}{4\pi\varepsilon_{opt}\varepsilon_0}\right)^{1/2} \tag{4.1}$$

It should be noted that E is the maximum field drop in the junction, which might be ten times of the average field. Due to the lack of knowledge about the maximum field drop, the average field (V/d) was used instead for all the calculations in this work. $\Delta\Phi$ is about 0.8 eV (Scott 2000). Thus the barrier between the bottom SRO and PZT film is around 0.5 eV. ε_{opt} is the optical permittivity of the ferroelectric. ε_{opt} may be smaller than ε_∞ (relative permittivity when frequency is infinite, usually the minimum relative permittivity of the material). During the emission, if the electron transition time from the interface to barrier maximum is shorter than the dielectric relaxation time, the medium does not have enough time to be polarized, and $\varepsilon_{opt} < \varepsilon_\infty$ is expected (Sze and Ng 2006).

[1] Since the I-V measurement was carried out in a static way and ionic conduction is a transient phenomenon, it was excluded from the transport mechanism.

According to Sze and Ng (2006), the leakage current of Schottky emission is:

$$J = A^* T^2 exp\left[\frac{-q\left(\Phi_B - \sqrt{qE/4\pi\varepsilon_{opt}\varepsilon_0}\right)}{k_B T}\right] \tag{4.2}$$

where A^* is Richardson constant, q is elementary charge and k_B is Boltzmann's constant. At a given temperature, $ln(J) \propto (\beta_{SE}/T)E^{0.5}$. The slope $(\beta_{SE}/T) = q^{3/2}/(k_B T\sqrt{4\pi\varepsilon_{opt}\varepsilon_0})$ and ε_{opt} can be extracted from the data.

4.1.1.1.2 Fowler-Nordheim Tunneling (FN)

Tunneling is the most common conduction mechanism through good insulators under high field. Different from direct tunneling, FN tunneling only crosses a partial width of the barrier. The interface acts as a thin blocking contact in thermal equilibrium. At low voltages, virtually the entire applied voltage is across the interface thus a very high field is built up. When this field is high enough (about 400 kV/cm for ferroelectric oxides (Scott 2000)), electrons can flow through the barrier (Sze and Ng 2006). This tunneling is mainly dependent on the field at the interface and independent of temperature[2] (Lampert and Mark 1970). The tunneling current is given by (Sze and Ng 2006):

$$J \propto E^2 exp\left[-\frac{4(2m^*)^{1/2}}{3\hbar}\frac{(q\Phi_B)^{3/2}}{qE}\right] \tag{4.3}$$

where $\hbar$ is reduced Planck constant or Dirac constant, equal to the Plank constant divided by 2π and m^* is effective carrier mass. According to Equation (4.3), $ln(J/E^2) \propto -\beta_{FN}(1/E)$. The slope $\beta_{FN} = 4(2m^*)^{1/2}q^{1/2}\Phi_B^{3/2}/3\hbar$.

4.1.1.2 Bulk-dominant Mechanisms

4.1.1.2.1 Ohmic Conduction For all PZT capacitors, leakage current at high fields exhibits non linear characteristics, especially for well insulated capacitors. But in low field range, a linear part is usually observed. According to Sze and Ng (2006), leakage current due to ohmic conduction is given by:

$$J \propto E\, exp\left(\frac{-\Delta E_{ac}}{k_B T}\right) \tag{4.4}$$

where ΔE_{ac} is activation field of electrons.

4.1.1.2.2 Frenkel-Pool Emission (FP)

For electrons which are generally trapped in local sites, thermal fluctuation can give them enough energy to get out and move to conduction band. This is the mechanism of Frenkel-Poole emission. Under

[2] Providing Φ_B is independent of temperature.

electric field, the electrons need less energy to get into conduction band as they are pulled by the field. The leakage current is (Sze and Ng 2006):

$$J \propto E\, exp\left[\frac{-q\left(\Phi_B - \sqrt{qE/\pi\varepsilon_{opt}\varepsilon_0}\right)}{k_B T}\right] \tag{4.5}$$

At a given temperature, $ln(J/E) \propto (\beta_{FP}/T)E^{0.5}$. $\beta_{FP} = q^{3/2}/(k_B T\sqrt{\pi\varepsilon_{opt}\varepsilon_0}) = 2\beta_{SE}$. The barrier reduction here is roughly twice as in the case of Schottky emission, since the barrier lowering is about twice due to the immobility of the positive charge (Scott 2000).

4.1.1.2.3 Space-Charge-Limited Current (SCLC)

The space-charge-limited current (SCLC) results from carriers injected into the ferroelectric, where no compensating charge is present (Sze and Ng 2006). Pointed out by Scott (2000), after reaching a threshold, the leakage current is no more limited by the mechanisms mentioned above but by the injected space charges.[3] At high field range, ejected electrons are distributed over a region of space, forming a continuum of charges. As the SCLC is formed, the amount of excess carriers won't affect the current. Traps in the film can lower the drift mobility, thus lowering SCLC (Lampert 1956, Many and Rakavy 1962). When trap densities is as high as $10^{18}\, cm^{-3}$, SCLC is lowered to almost unmeasurable level (Rose 1955).

According to Mott-Gurney law (Mott and Gurney 1948), the SCLC is given by:

$$J(V) = \frac{9\varepsilon_{opt}\mu V^2}{8d^3} \tag{4.6}$$

where μ is the carrier mobility.

SCLC dependency on film thickness d is not accurate. Instead, an accommodation or mutual diffusion length a' is excluded for correction. Thus thickness is replaced by $(d - 2a')$ (Scott 2000). Mayer's work on Si indicates that a' is about 10% of d (Mayer *et al.* 1965).

Lampert gave more precise theoretical equations for SCLC. And two different equation are assigned to different field regions (Lampert and Mark 1970).

In the relatively low field range, the current is given by:

$$J(V,d) = \frac{9}{8} q t_R \mu_n \mu_p \tau V^2 d^{-3} \tag{4.7}$$

where t_R is recombination time, μ_n and μ_p are the mobility of electrons and holes, and τ is the density of recombination centers.

[3] SCLC densities in solids are orders of magnitude less than those in vacuum tubes (Scott 2000).

Table 4.1: Possible conduction mechanisms in ferroelectric capacitors(Sze and Ng 2006).

Dominated by	Process	Expression	Dependence (E, T or d)
Interface	Schottky emission	$J = A^* T^2 exp\left[\frac{-q\left(\Phi_B - \sqrt{qE/4\pi\varepsilon_{opt}\varepsilon_0}\right)}{k_B T}\right]$	$\propto T^2 exp\left(+\beta_{SE}\sqrt{E}/T - q\Phi_B/k_B T\right)$
	Fowler-Nordheim tunneling	$J \propto E^2 exp\left[-\frac{4(2m^*)^{1/2}}{3\hbar}\frac{(q\Phi_B)^{3/2}}{qE}\right]$	$\propto E^2 exp(-\beta_{FN}/E)$
Bulk	Ohmic conduction	$J \propto E\, exp\left(\frac{-\Delta E_{ac}}{k_B T}\right)$	$\propto E exp\,(-\beta_{OC}/T)$
	Frenkel-Pool emission	$J \propto E\, exp\left[\frac{-q\left(\Phi_B - \sqrt{qE/\pi\varepsilon_{opt}\varepsilon_0}\right)}{k_B T}\right]$	$\propto E exp\left(+2\beta_{SE}\sqrt{E}/T - q\Phi_B/k_B T\right)$
	Space-charge-limited current	$J = A_0 \frac{V^n}{d^m}$	$\propto E^n d^{-(m-n)}$

β_{SE}, β_{FN}, β_{OC}, A^*, A_0, m and n are positive constants.

In higher voltage range, the current regime changes to:

$$J(V,d) = \frac{125}{18}\varepsilon_0\varepsilon_{opt}t_R\mu_n\mu_p V^3 d^{-5} \tag{4.8}$$

The cube-law at higher field is due to double injection (Lampert and Mark 1970). Scott *et al.*'s work (1994) on PZT showed transition from V^2 to V^3 and V to V^3 directly were both possible. The transition field between the V^2-dependence and V^3-dependence is given by (Scott 2000):

$$V_{th} = constant\,\frac{d^2}{2\mu_n\mu_p} \tag{4.9}$$

Rose's theoretical work (1955) indicates that the voltage dependence of a even higher power is possible:

$$J(V,d) = A_0\frac{V^n}{d^m} \tag{4.10}$$

where A_0, n and m are all constants. n can exceed 3 when the space charge density approaches a uniform distribution between cathode and anode. Shin *et al.*'s work (1999) on sol-gel-derived PZT capacitor showed that n was 5.06 (at 40 °C).

4.1.1.3 Summary

According to the five charge transport mechanisms described above, Table 4.1 lists the equations of each mechanism and corresponding dependence parameters.

4.1.2 Leakage Current of Sputtered Capacitors and Fitting Results

Figure 4.1 shows the J-E characteristics of sputtered PZT of various thicknesses from 40.5 nm to 190 nm with SRO top electrode. Forward J_l (response to voltage applied from 0 to V_{max}) and reverse J_l (response to voltage applied from 0 to $-V_{max}$) were identical for all four capacitors. J_l of 40.5-nm-thick capacitor was about 4 orders of magnitude bigger than other three thicker capacitors.

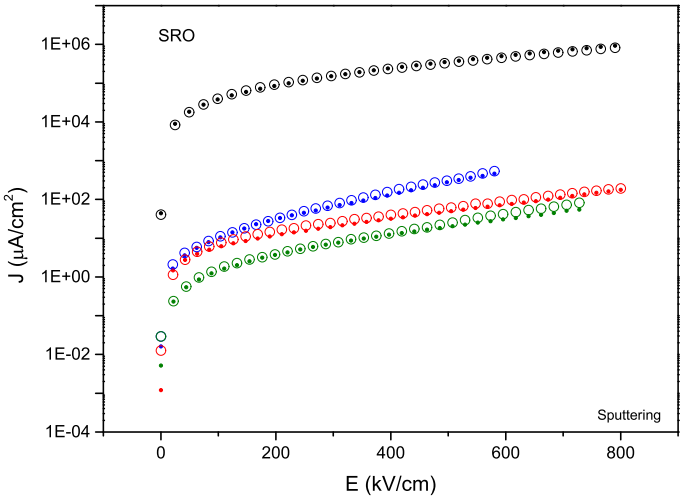

Figure 4.1: J-E characteristics of sputtered PZT capacitors with SRO top electrode. Forward J-E is plotted with filled circles and reverse J-E with open circles. 40.5 nm in black, 120.6 nm in blue, 136 nm in olive and 190 nm in red.

In Figure 4.1, the three thicker capacitors have similar amount of leakage current at same field. The variation of leakage is not only due to the thickness. The leakage current of capacitors on the same sample at different locations also varies slightly. Figure 4.2 shows the forward J-E characteristics of 190-nm-thick sputtered PZT capacitors with SRO top electrode at seven different locations. The variation range is same to that of the three thicker capacitors in Figure 4.1. Since it was inappropriate to investigate the thickness dependence with only one J-E curve for each sample, we only extracted the slopes of the curves as they always kept the same shape. In the leakage current investigation, thickness dependence is neglected. The dependence of thickness can be achieved by measuring a large amount of capacitors systematically on the same sample or several samples with same thickness and the size of capacitor should be small enough to minimize the influence of defects. Pintilie *et al.*'s work (2007) on PZT(20/80) deposited by PLD showed that films with thickness varying from 50 nm to 230 nm exhibited similar amount of leakage current.

Figure 4.3 shows the J-E characteristics of these sputtered PZT capacitors with Pt top electrode and ITO top electrode. As the "sandwich" structure was no more symmetric, forward J-E curve differed from reverse J-E curve, but the difference was insignificant. J_l of 40.5-nm-thick capacitor with Pt top electrode and ITO electrode was much smaller, compared to the same capacitor with SRO top electrode. Generally, thin capacitor (less than 50 nm) exhibited relatively higher J_l. We attribute this to the difference of defect density. PZT forms columnar grains from bottom to top during the crystallization.

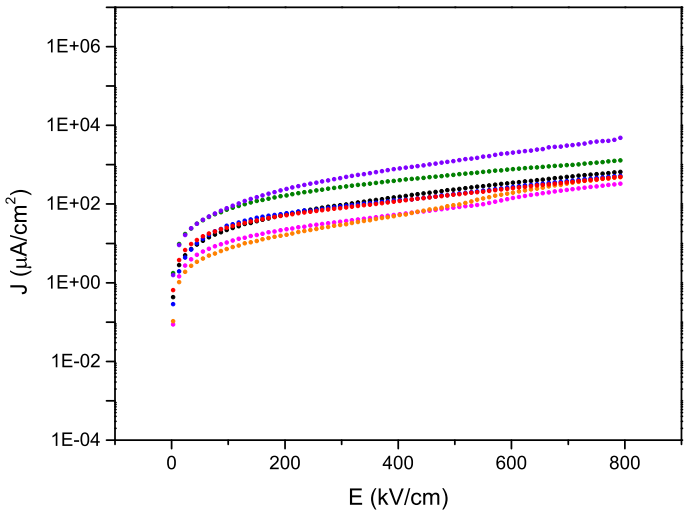

Figure 4.2: Forward J-E characteristics of 190-nm-thick sputtered PZT capacitor with SRO top electrode on seven different locations.

As thickness decreases, the density of defects which penetrate the thickness increases, thus J_l increases. Our J-E measurement was carried out on $100 \times 100 \mu m^2$ large capacitors for all the samples, and the defect density is different from capacitor to capacitor even on the same sample for sub–50 nm capacitor. For 40.5-nm-thick sample, about 80% of the capacitors exhibited insufficient insulated characteristics. For the three thicker samples, the amount of J_l were similar when top electrode changed.

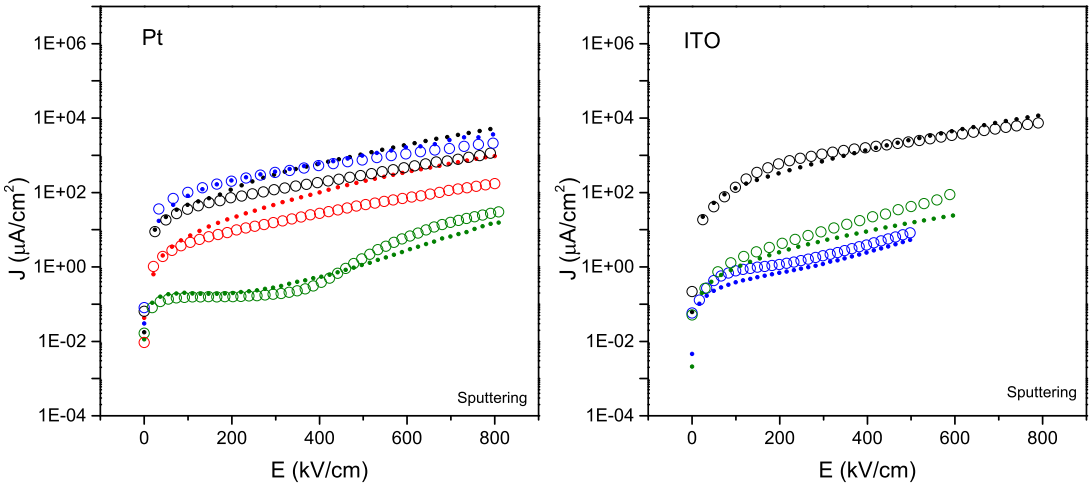

Figure 4.3: J-E characteristics of sputtered PZT capacitors with Pt top electrode (left) and ITO top electrode (right). Forward J-E is plotted with filled circles and reverse J-E with open circles. 40.5 nm in black, 120.6 nm in blue, 136 nm in olive and 190 nm in red.

The impact of top electrode on leakage current was minor. Capacitors of three different top electrodes showed leakage of similar quantity and shape. Forward J-E curve and reverse J-E curve were of little difference and were exact the same for SRO/PZT/SRO capacitors. Now we are going to fit various models with only forward J_l.

Schottky Emission

Figure 4.4 shows the leakage current of four sputtered capacitors with SRO top electrode. From 40 kV/cm to 800 kV/cm, $ln(J_l)$ is linearly dependent on $E^{0.5}$. The slopes $\beta_{SE}/T = q^{1.5}/k_B T\sqrt{\pi\varepsilon_{opt}\varepsilon_0}$ of four curves were extracted and ε_{opt} for four capacitors were calculated, presented in Table 4.2.

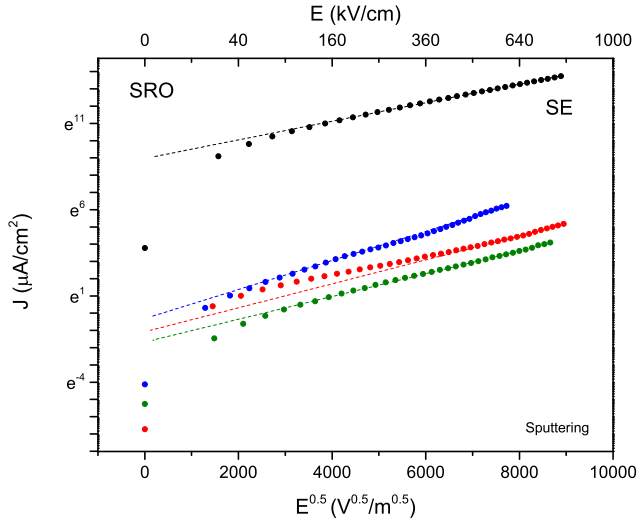

Figure 4.4: Leakage characteristics of sputtered PZT capacitors with SRO top electrode plotted in $ln(J) - E^{0.5}$ form. 40.5 nm in black, 120.6 nm in blue, 136 nm in olive and 190 nm in red.

Leakage currents of capacitors with Pt top electrode and ITO top electrode are presented in Figure 4.5 and ε_{opt} were extracted and presented in Table 4.2. The starting point of linear dependency for 136-nm-thick capacitor with Pt top electrode and for 120.6-nm-thick capacitor with ITO top electrode were higher than others. The bumps observed in these two samples at low field range were due to the dielectric polarization. Since these bumps were small, they were usually covered by leakage current (more discussion in next subsection).

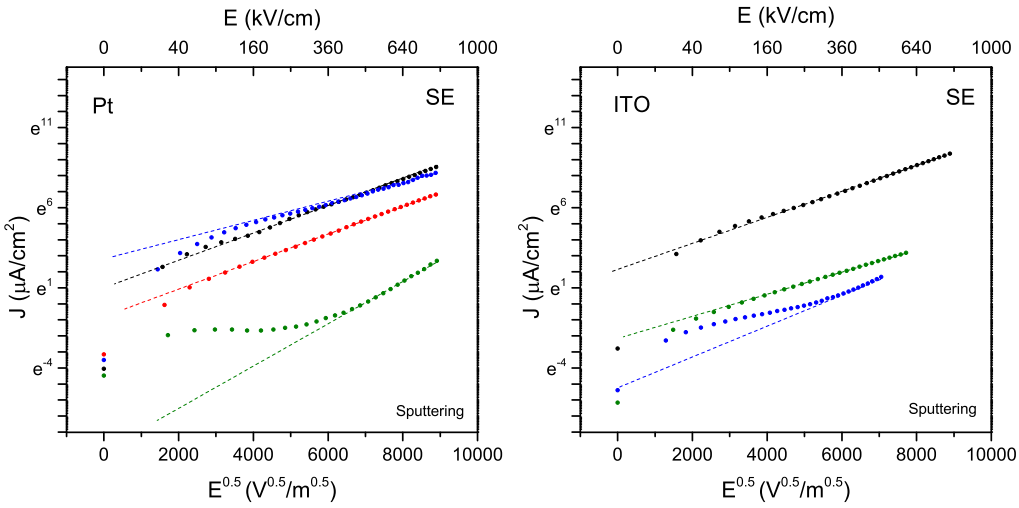

Figure 4.5: Leakage characteristics of sputtered PZT capacitors with Pt top electrode (left) and ITO top electrode (right) plotted according to Schottky emission. 40.5 nm in black, 120.6 nm in blue, 136 nm in olive and 190 nm in red.

$\varepsilon_{opt} = n^2$, where n is refractive index. According to Huang *et al.* (2000), Deineka *et al.* (2001),

Table 4.2: ε_{opt} of sputtered PZT capacitors extracted according to Schottky emission.

PZT Thickness (nm)	$10^4\times$slope	$10^4\times$slope	$10^4\times$slope	ε_{opt}	ε_{opt}	ε_{opt}
Top electrode	SRO	Pt	ITO	SRO	Pt	ITO
40.5	5.4 ± 0.1	8.2 ± 0.2	8.1 ± 0.3	7.3 ± 0.1	3.2 ± 0.1	3.3 ± 0.1
120.6	8.4 ± 0.1	6.7 ± 0.2	8.9 ± 0.3	3.0 ± 0.3	4.8 ± 0.1	2.7 ± 0.1
136	6.7 ± 0.2	13.8 ± 0.3	7.0 ± 0.2	4.7 ± 0.1	1.1 ± 0.1	4.4 ± 0.1
190	5.7 ± 0.2	8.7 ± 0.3	N/A	6.5 ± 0.2	2.8 ± 0.1	N/A

Table 4.3: m^* extracted by estimating $\Phi_B = 0.5\,eV$.

PZT thickness (nm)	$10^{-7}\times$ Slope	m^*/m
40.5	- 1.80 ± 0.2	$(1.1 \pm 0.1) \times 10^{-4}$
120.6	-3.2 ± 0.2	$(3.6 \pm 0.1) \times 10^{-4}$
136	- 8.7 ± 0.3	$(2.6 \pm 0.1) \times 10^{-3}$
190	-9.7 ± 0.4	$(3.3 \pm 0.1) \times 10^{-3}$

Peng *et al.* (2011), n for PZT is about 2.3 $\sim$ 3.1, thus ε_{opt} is about 5.3 $\sim$ 9.6. The extracted ε_{opt} are consistent with these experimental results.

Fowler-Nordheim Tunneling

Figure 4.6 plots the leakage current according to Fowler-Nordheim tunneling. From $\sim$ 650 kV/cm to 800 kV/cm, leakage current is $ln(J/E^2)$ proportional to $1/E$. By estimating $\Phi_B \approx 0.5eV$, m^* are extracted and presented in Table 4.3. As m^* is out of the range, FN is excluded from the charge transport mechanism.

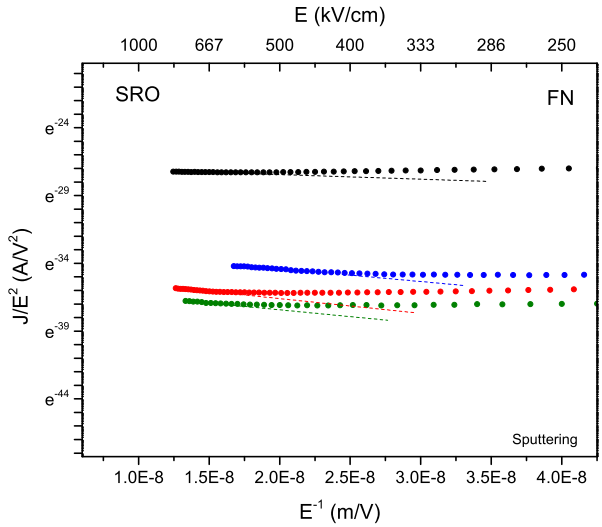

Figure 4.6: Leakage characteristics of sputtered PZT capacitors with SRO top electrode plotted in $ln(J/E^2) - E^{-1}$ form. 40.5 nm in black, 120.6 nm in blue, 136 nm in olive and 190 nm in red.

Leakage current of sputtered PZT capacitors with Pt top electrode and ITO top electrode showed similar linear dependency at high field and the extracted m^* had similar small values. Fowler-Nordheim tunneling is excluded from the charge transport mechanism.

Ohmic Conduction

Figure 4.7 shows that below ~120 kV/cm, current was linearly dependent on field. When field passed 120 kV/cm, leakage current increased more rapidly. The different slopes are attributed to the same reason, stated before. For relatively thick (> 100 nm)capacitors, the slopes were of little difference. For 40.5-nm-thick capacitor, the slope was much larger. It may be due to the increased density of defect penetrating the thickness.

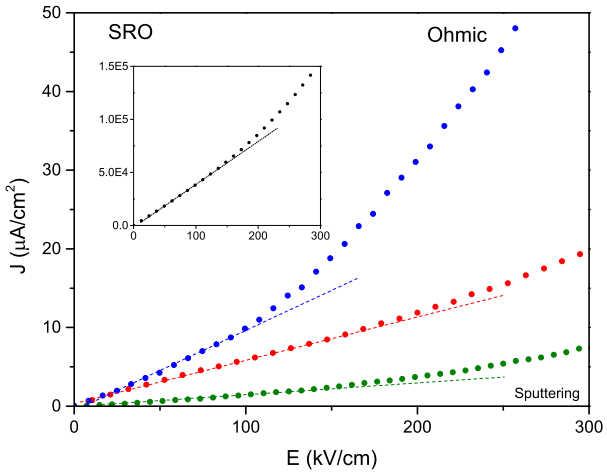

Figure 4.7: Leakage characteristics of sputtered PZT capacitors with SRO top electrode at low field. 40.5 nm in balck, 120.6 nm in blue, 136 nm in olive and 190 nm in red.

Leakage currents of sputtered capacitors with Pt top electrode and ITO top electrode are plotted in Figure 4.8. They showed similar behaviors.

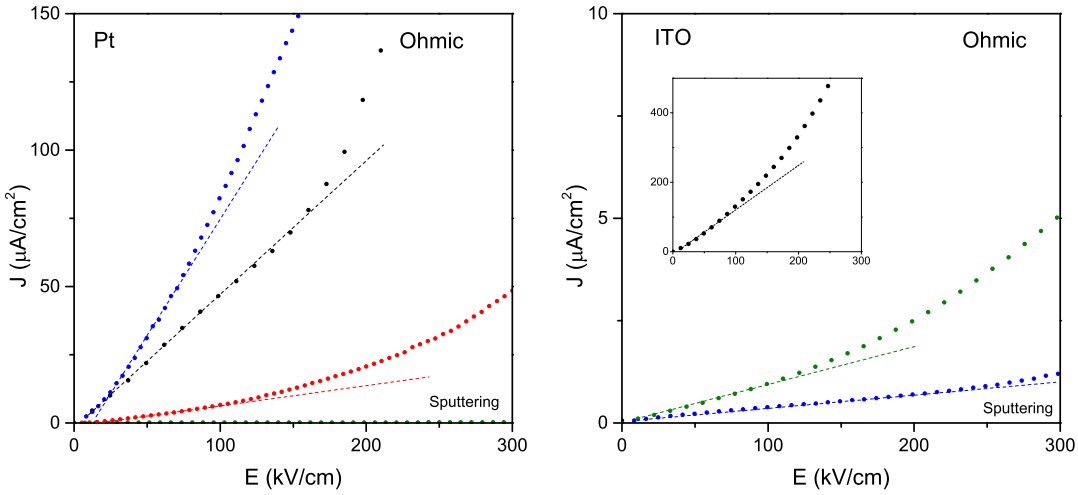

Figure 4.8: Leakage characteristics of sputtered PZT capacitors with Pt top electrode and ITO top electrode at low field. 40.5 nm in balck, 120.6 nm in blue, 136 nm in olive and 190 nm in red.

For all sputtered capacitors of different thicknesses with different top electrodes, linear dependence on field had been observed at low field. Sze and Ng (2006) stated at low voltages, current was carried by thermally excited electrons hopping from one isolated state to the next. This mechanism yields an ohmic

characteristic, linearly dependent on field, indicating at low field, the predominant charges are thermally generated.

Frenkel-Pool Emission

Leakage currents are plotted according to Frenkel-Pool emission in Figure 4.9. From 360 kV/cm to 800 kV/cm there was a linear dependency and ε_{opt} were extracted and presented in Table 4.4.

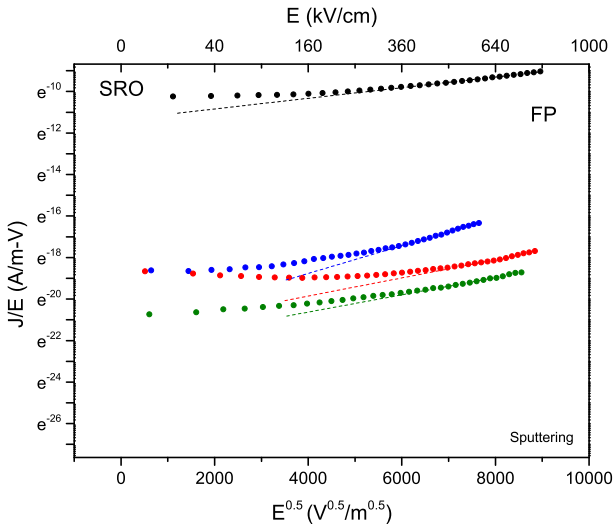

Figure 4.9: Leakage characteristics of sputtered PZT capacitors with SRO top electrode plotted in $ln(J/E) - E^{0.5}$ form. 40.5 nm in balck, 120.6 nm in blue, 136 nm in olive and 190 nm in red.

For capacitors with Pt top electrode and ITO top electrode, leakage currents are plotted in Figure 4.10 in $ln(J/E)$ vs $E^{0.5}$ form and extracted ε_{opt} are presented in Table 4.4.

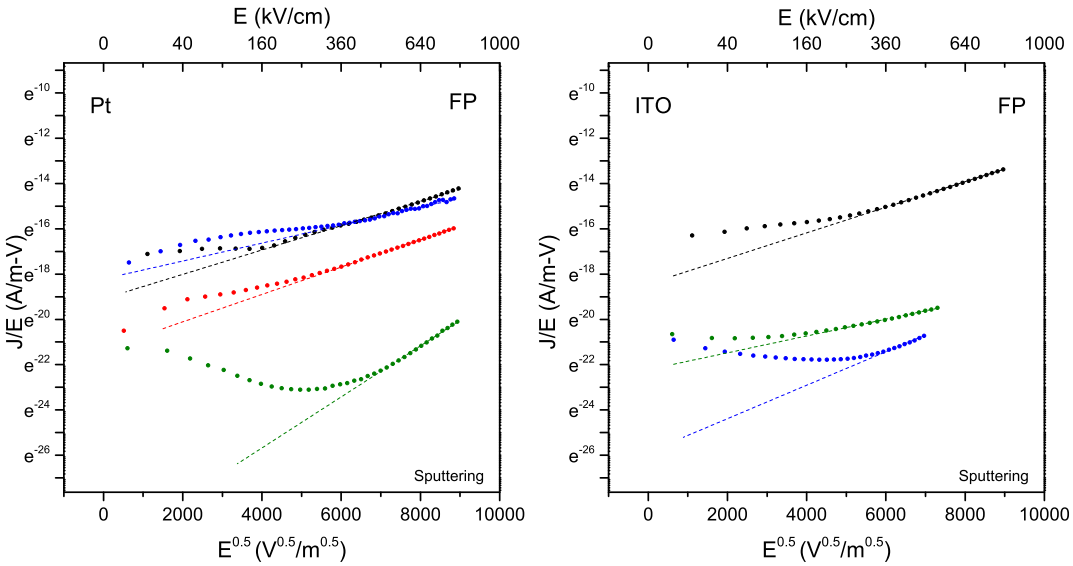

Figure 4.10: Leakage characteristics of sputtered PZT capacitors with Pt top electrode and ITO top electrode plotted in $ln(J/E) - E^{0.5}$ form. 40.5 nm in balck, 120.6 nm in blue, 136 nm in olive and 190 nm in red.

Compared with the fitting to Schottky emission in Figure 4.4 and Figure 4.5, both showed good

Table 4.4: ε_{opt} of sputtered PZT capacitors extracted according to Frenkel-Pool emission.

PZT Thickness (nm)	$10^4\times$ slope	$10^4\times$ slope	$10^4\times$ slope	ε_{opt}	ε_{opt}	ε_{opt}
Top electrode	SRO	Pt	ITO	SRO	Pt	ITO
40.5	2.7 ± 0.1	5.3 ± 0.2	5.6 ± 0.1	129.0 ± 5.0	30.0 ± 1.0	28.0 ± 0.5
120.6	6.8 ± 0.1	4.3 ± 0.1	7.1 ± 0.3	18.0 ± 0.3	47.0 ± 2.2	4.1 ± 0.2
136	4.1 ± 0.2	11.3 ± 0.1	4.1 ± 0.2	55.0 ± 3.0	6.7 ± 0.1	52.0 ± 2.6
190	4.2 ± 0.2	5.9 ± 0.1	N/A	47.0 ± 2.0	25.0 ± 0.4	N/A

fitting quality from 300 to 800 kV/cm, and Schottky emission showed a better fit at medium field (100 $\sim$ 300 kV/cm). ε_{opt} extracted from the fitting to SE was much smaller than that from the fitting to FP. The extracted ε_{opt} from FP was much larger than the experimental results from Huang *et al.* (2000), Deineka *et al.* (2001), Peng *et al.* (2011). Thus interface-dominant SE is more consistent with the data at medium and high field than bulk-dominant FP emission.

Space-Charge-Limited Current

Figure 4.11 shows the leakage currents of sputtered PZT capacitors with SRO top electrode plotted in $log-log$ form. Starting from $\sim 200\, kV/cm$, $J \propto E^2$. At higher field ($400 \sim 600\, kV/cm$), the dependence transfered to E^3 except the 40.5-nm-thick capacitor.

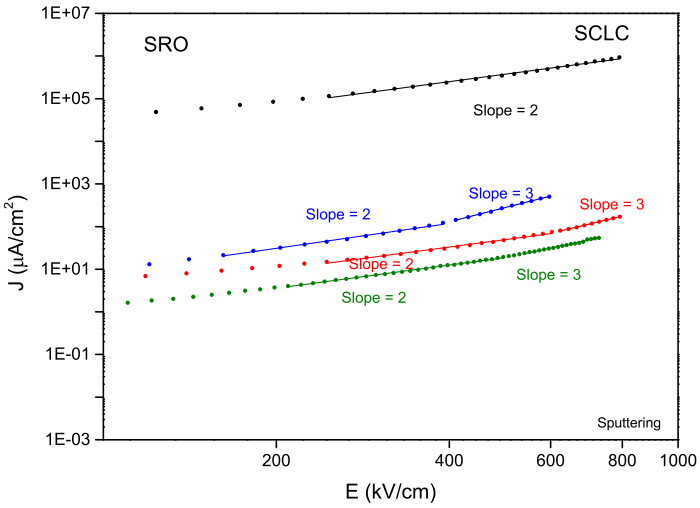

Figure 4.11: Leakage characteristics of sputtered PZT capacitors with SRO top electrode plotted in $logJ - logE$ form. 40.5 nm in black, 120.6 nm in blue, 136 nm in olive and 190 nm in red.

Figure 4.12 shows the leakage current of 4 sputtered PZT capacitors with Pt top electrode and ITO top electrode plotted in $log - log$ form. The dependency on E was similar to SRO-top-electrode capacitors. The transition field from E^2 to E^3 was also $\sim 400 kV/cm$. For 136-nm-thick capacitor with Pt top electrode, leakage dependence on field transfered from E^2 to E^5 directly.

As stated before, the thickness dependence is impossible to investigate with only one J-E curve from each capacitor, since leakage varies from capacitor to capacitor of same thickness. So the quantitative investigation of thickness dependence on leakage current was not carried out.

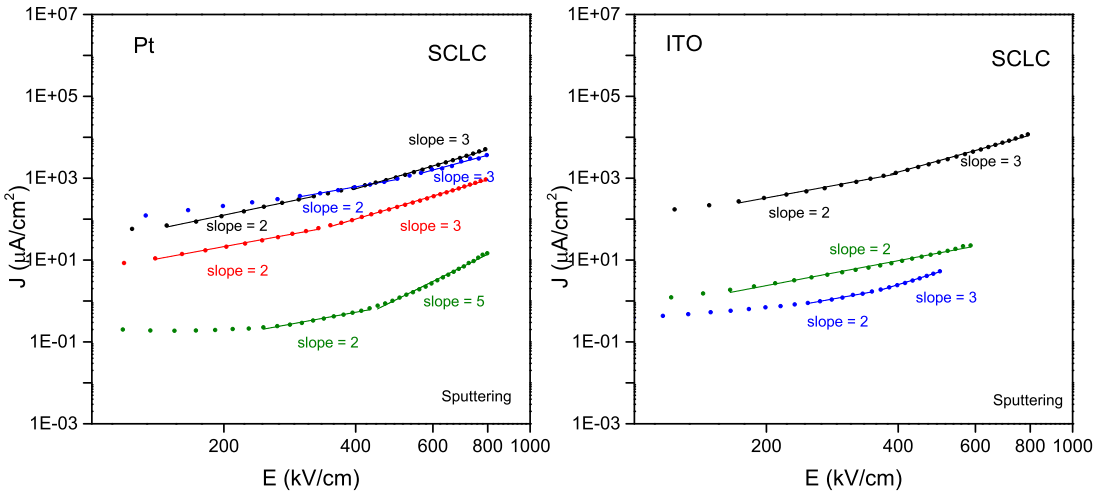

Figure 4.12: Leakage characteristics of sputtered PZT capacitors with Pt top electrode (left) and ITO top electrode (right) plotted in $logJ - logE$ form. 40.5 nm in balck, 120.6 nm in blue, 136 nm in olive and 190 nm in red.

According to the fitting results with different mechanisms, Figure 4.13 shows the well fitted region of each mechanism. Interface-dominant SE mechanism was well fitted to the data in large range (from $\sim$ 50 to 800 kV/cm) and the extracted ε_{opt} was consistent with experimental results; Ohmic conduction was fitted to the data from 0 to $\sim$ 150 kV/cm ; SCLC was fitted to the data in two regimes in the range of $\sim$ 200 to 800 kV/cm, E^2 in lower range and E^3 in higher range; FN was not compatible as the extracted m^* was out of range even it was fitted to the data from $\sim$ 600 to 800 kV/cm ; FP was well fitted to the data from $\sim$ 200 to 800 kV/cm, but extracted ε_{opt} was out of the experimental range.

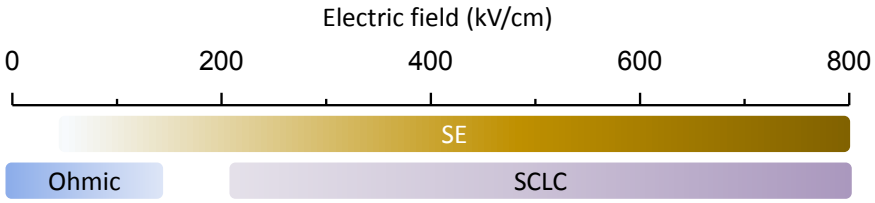

Figure 4.13: Well fitted charge transport mechanisms in different field ranges for sputtered PZT capacitors.

Top electrode was found to have little influence on charge transport, so we estimate that the top electrode interface has little influence to leakage. The 40.5-nm-thick sputtered capacitor showed much larger leakage compared to other thicker capacitors. At $\sim$ 200 to 800 kV/cm, both Schottky emission and space-charge-limited current fitted the data, and further study at various temperatures may detect the appropriate mechanism.

4.1.3 Leakage Current of Sol-gel-derived Capacitors and Fitting Results

Figure 4.14 shows I-V characteristics of sol-gel-derived PZT capacitors of various thicknesses from 67 nm to 200 nm with SRO top electrode and Pt top electrode. (More than three 33-nm-thick capacitors with SRO top electrode were all too leaky to be measured.) For 67-nm-thick, 133-nm-thick and 200-nm-

thick PZT capacitors, J-E curves were different from that of sputtered ones; leakage current were not symmetric for both SRO-top-electrode and Pt-top-electrode capacitors; below 300 kV/cm, leakage was quite small and from 400 kV/cm upward leakage increased rapidly. The 100-nm-thick capacitor, which experienced 2 h annealing in furnace, exhibited similar J-E curve as sputtered capacitors and the forward and reverse J-E curves were symmetric for it. Top electrode also showed minor influence on leakage current. In Figure 4.14, as top electrode changed from SRO to Pt, J-E curves did not change obviously for 133-nm-thick and 200-nm-thick capacitors.

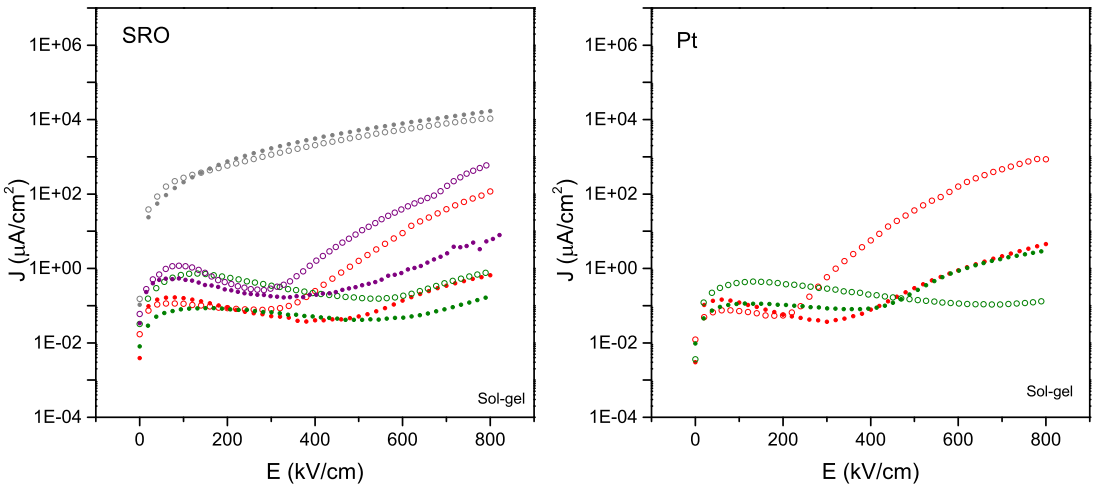

Figure 4.14: J-E characteristics of sol-gel-derived PZT capacitors. Forward J-E is plotted with filled circles and reverse J-E with open circles. 67 nm in black, 133 nm in olive, 200 nm in red and 100 nm in grey.

Between 100 and 300 kV/cm, there was a "negative resistance region" for 67-nm-thick, 133-nm-thick and 200-nm-thick capacitors. They are usually due to double injection or trap filling and trap emptying (Ridley and Watkins 1961, Ridley 1963, Scott *et al.* 1994). The 100-nm-thick capacitor, which experienced much longer annealing for the crystallization of top electrode, did not show the negative resistance. In Figure 4.3, we notice that leakage current of 136-nm-thick sputtered capacitor with Pt top electrode in the range between 100 and 300 kV/cm also showed a similar shape, but the Resistance did not drop to negative. These abnormal leakages actually were much smaller ($2 \sim 3$ orders of magnitude less) than the "normal" leakages. We attributed these bumps between 0 and 200 kV/cm to dielectric polarization. As an external field was applied to the capacitor, corresponding dielectric polarization was formed. At the beginning point of measurement, the field change was the highest, thus a large amount of dielectric polarization occurred between 0 and 200 kV/cm. Then as the field change was stable, the current due to dielectric polarization was also stable. This current J_d was relatively small and was usually covered by the leakage current part J_l. So only when the capacitor was well insulated, we could observe the "negative resistance region". In chapter 5, the leakage current will be further analyzed, according to which, the current J_U (or J_D, current response to pulse "U" or pulse "D" in PUND measurement) is equivalent[4] to J_d. Figure 4.15 shows J_U in PUND measurement. From the ratio of J_U in PUND

[4] $J_U = J_l + J_d \approx J_d$, because leakage current in dynamic PUND measurement is relatively much smaller for a good insulated capacitor.

Table 4.5: ε_{opt} of sol-gel-derived PZT capacitors extracted according to Schottky emission.

PZT Thickness (nm)	$10^4\times$ slope	$10^4\times$ slope	$10^4\times$ slope	$10^4\times$ slope	ε_{opt}	ε_{opt}	ε_{opt}	ε_{opt}
Direction of E	forward	reverse	forward	reverse	forward	reverse	forward	reverse
Top electrode	SRO	SRO	Pt	Pt	SRO	SRO	Pt	Pt
67	15.3 ± 1.0	22.9 ± 0.2	N/A	N/A	1.1 ± 0.1	0.4 ± 0.1	N/A	N/A
133	12.0 ± 1.0	13.0 ± 0.5	15.2 ± 2.0	N/A	1.3 ± 0.1	1.4 ± 0.1	0.8 ± 0.1	N/A
200	13.8 ± 1.0	23.5 ± 0.5	15.5 ± 1.0	22.3 ± 2.0	1.0 ± 0.1	0.4 ± 0.1	0.9 ± 0.1	0.5 ± 0.1
100	6.4 ± 0.2	6.6 ± 0.2	N/A	N/A	4.4 ± 0.1	6.2 ± 0.2	N/A	N/A

measurement to J_d in I-V measurement in Figure 5.12, the equivalent maximum value of J_d is ~ 1.2 $\mu m/cm^2$, which is compatible to the bump peak observed in Figure 4.14. Thus in our case, in this region the resistance is not negative. The bump is due to dielectric polarization and it can only be observed when leakage current is less than ~ 1 uA/cm^2 in this region.

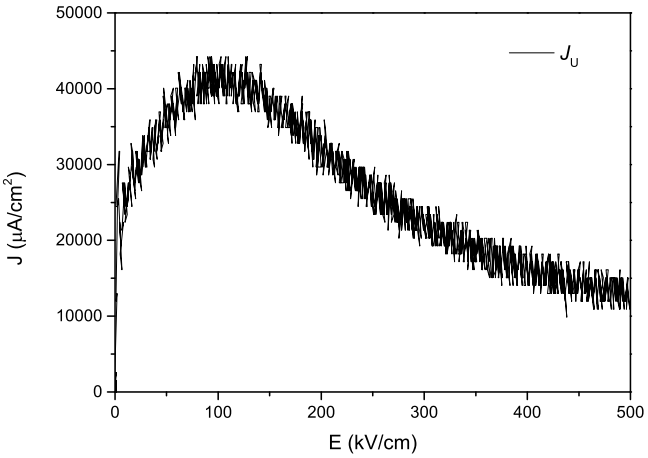

Figure 4.15: J_U from PUND measurement. Data from 200-nm-thick sol-gel-derived capacitor with Pt top electrode.

Now, we will plot the leakage according to each charge transport mechanism. Because J_d is difficult to be separated from leakage current,[5] leakage current fitting was performed to $(J_l + J_d)$.

Schottky Emission

Figure 4.16 plots the leakage in $ln(J)$ vs $E^{0.5}$ form. Linear fitting was applied to the curves and ε_{opt} was extracted, as shown in Table 4.5. According to Huang *et al.* (2000), Deineka *et al.* (2001), Peng *et al.* (2011), only the ε_{opt} of 100-nm-thick capacitor was in the range. Thus SE is excluded from the charge transport mechanism.

Fowler-Nordheim Tunneling

Figure 4.17 plots the leakage of sol-gel-derived capacitors with SRO top electrode in $ln(J/E^2)$ vs

[5] Set a sufficient delay time in I-V measurement can exclude J_d.

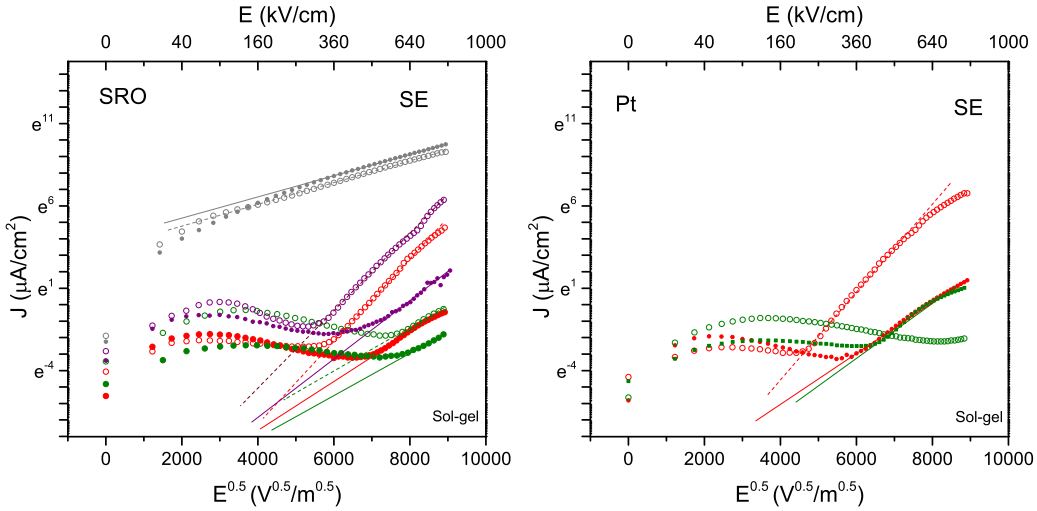

Figure 4.16: Leakage characteristics of sol-gel-derived PZT capacitors with SRO top electrode (left) and Pt top electrode (right) plotted in $ln(J) - E^{0.5}$ form. Forward I-V is plotted with filled circles and reverse I-V with open circles. 67 nm in black, 133 nm in olive, 200 nm in red and 100 nm in grey.

E^{-1} form. Linear fitting was applied to the high field range. However the extracted m^*/m was between 5×10^{-7} and 1×10^{-4} (estimating $\Phi_B = 0.5\, eV$), which was out of the range. Similar m^* were found from Pt-top-electrode capacitors. So FN tunneling is also excluded from the charge transport mechanism.

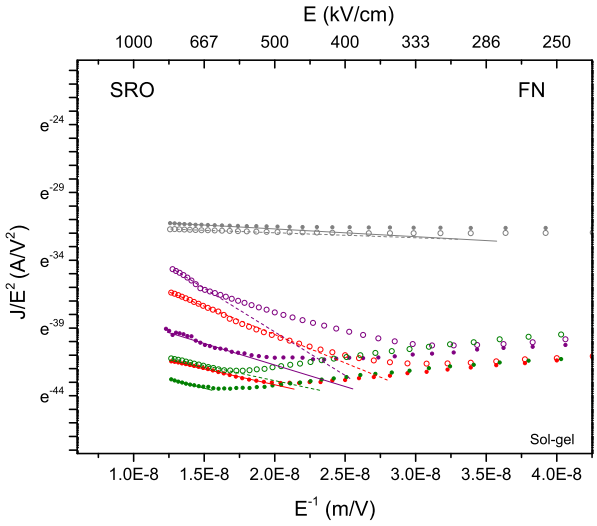

Figure 4.17: Leakage characteristics of sol-gel-derived PZT capacitors with SRO top electrode plotted in $ln(J/E^2) - E^{-1}$ form. Forward I-V is plotted with filled circles and reverse I-V with open circles. 67 nm in black, 133 nm in olive, 200 nm in red and 100 nm in grey.

Ohmic Conduction

Figure 4.18 shows the J-E curves of sol-gel-derived capacitors with both SRO top electrode and Pt top electrode at low field range. Leakage current was linearly dependent on field from 0 to 30 kV/cm, which was smaller than the range of sputtered capacitors. This is because the smaller leakage current is partly covered by the current due to dielectric polarization.

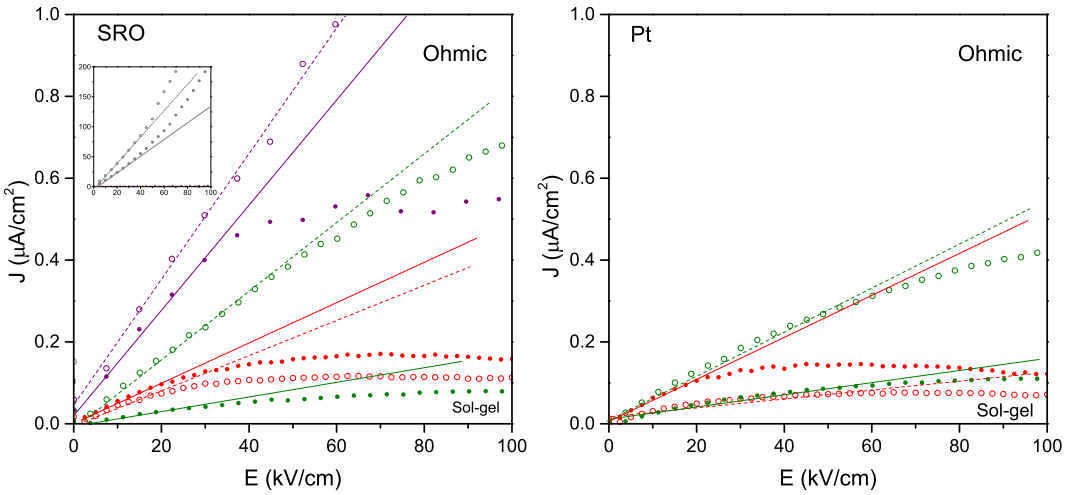

Figure 4.18: Leakage characteristics of sol-gel-derived PZT capacitors with SRO top electrode and Pt top electrode at low field. Forward I-V is plotted with filled circles and reverse I-V with open circles. 67 nm in black, 133 nm in olive, 200 nm in red and 100 nm in grey.

Frenkel-Pool Emission

Figure 4.19 plots the leakage in the form of J/E vs $E^{0.5}$ according to FP emission. 100-nm-thick capacitor showed a much smaller slope, compared to other three capacitors. From ~450 to 800 kV/cm, linear fit was applied to all curves and Table 4.6 lists the extracted ε_{opt}. Except the 100-nm-thick capacitor, all ε_{opt} were in the range according to the experiments of Huang *et al.* (2000), Deineka *et al.* (2001), Peng *et al.* (2011). Thus FP is compatible to the charge transport mechanism in the field between ~450 to 800 kV/cm.

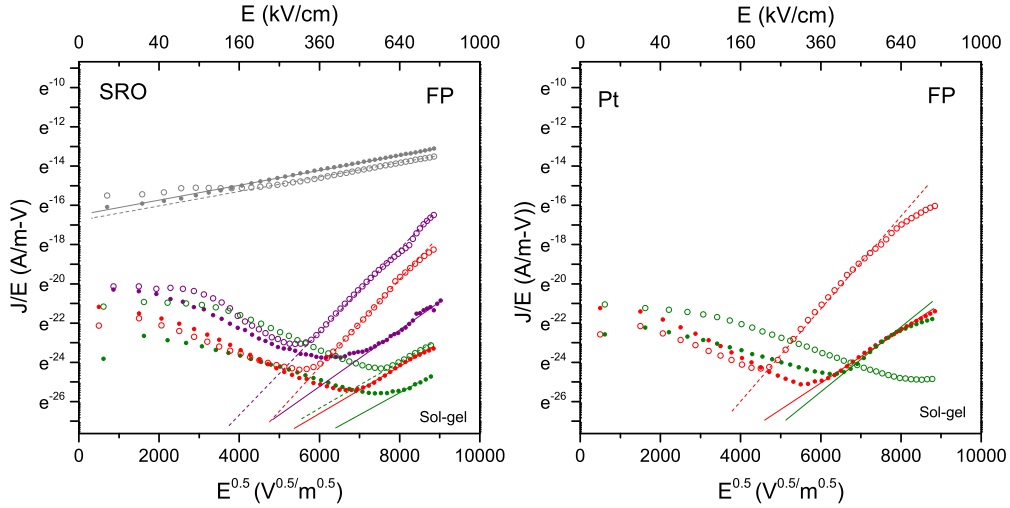

Figure 4.19: Leakage characteristics of sol-gel-derived PZT capacitors with SRO top electrode (left) and Pt top electrode (right) plotted in $ln(J/E) - E^{0.5}$ form. Forward I-V is plotted with filled circles and reverse I-V with open circles. 67 nm in black, 133 nm in olive, 200 nm in red and 100 nm in grey.

Space-Charge-Limited Current

Figure 4.20 plots the leakage in $log - log$ form. The slope was much bigger than that of sputtered

Table 4.6: ε_{opt} of sol-gel-derived PZT capacitors extracted according to Frenkel-Pool emission.

PZT Thickness (nm)	$10^4\times$ slope	$10^4\times$ slope	$10^4\times$ slope	$10^4\times$ slope	ε_{opt}	ε_{opt}	ε_{opt}	ε_{opt}
Direction of E	forward	reverse	forward	reverse	forward	reverse	forward	reverse
Top electrode	SRO	SRO	Pt	Pt	SRO	SRO	Pt	Pt
67	14.5 ± 1.0	20.1 ± 1.0	N/A	N/A	4.1 ± 0.3	2.1 ± 0.1	N/A	N/A
133	10.4 ± 2.0	11.1 ± 2.0	14.4 ± 2.0	N/A	7.9 ± 1.5	7.0 ± 1.3	4.1 ± 0.6	N/A
200	12.5 ± 2.0	20.2 ± 2.0	12.7 ± 1.0	20.8 ± 2.0	5.5 ± 0.9	1.7 ± 0.2	5.3 ± 0.4	2.0 ± 0.2
100	3.8 ± 1.0	3.8 ± 1.0	N/A	N/A	60.5 ± 16.0	59.8 ± 16.0	N/A	N/A

capacitors in Figure 4.11 except the 100-nm-thick capacitor. SCLC is consistent with the experimental data in the range from ∼500 to 800 kV/cm.

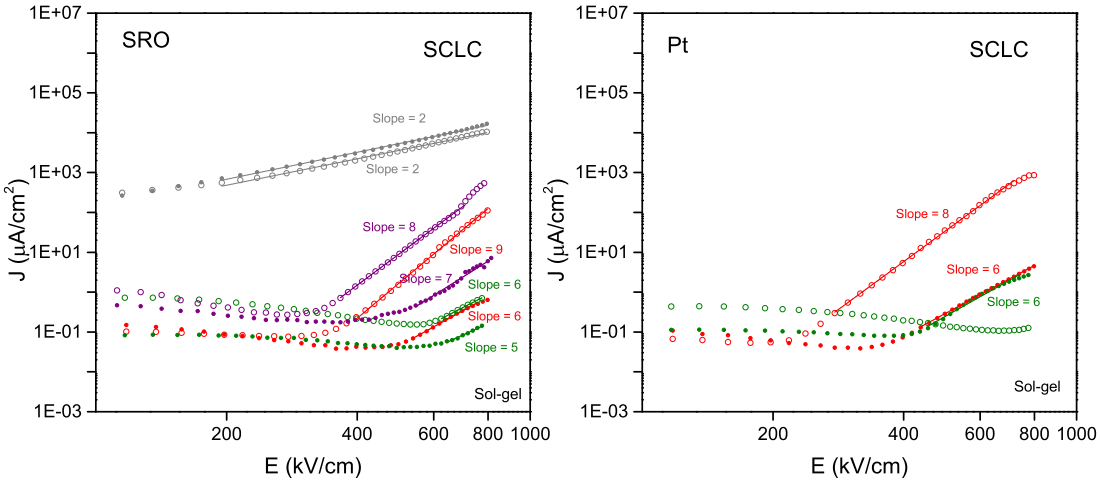

Figure 4.20: Leakage characteristics of sol-gel-derived PZT capacitors with SRO top electrode (left) and Pt top electrode (right) plotted in $logJ - logE$ form. Forward I-V is plotted with filled circles and reverse I-V with open circles. 67 nm in black, 133 nm in olive, 200 nm in red and 100 nm in grey.

According to the fitting results above, the well fitted mechanisms are plotted in Figure 4.21. In low field range (0 to 30 kV/cm), Ohmic conduction was compatible; In high field range (from ∼ 500 to 800 kV/cm), both FP and SCLC were well fitted to the data. In the range between 50 kV/cm and 500 kV/cm, due to the existence of J_d, none of the mechanisms mentioned above satisfied the leakage current. We extended the fitting range of ohmic conduction, FP and SCLC with dash lines. 33-nm-thick capacitor was too leaky to be measured. Top electrode also showed little influence on leakage as it did for sputtered capacitors.

4.1.4 Conclusion

Low leakage currents were observed for sputtered PZT capacitors with a thickness between 100 nm and 200 nm. The amount of current density were compatible with reported results for high quality PZT capacitors (Zubko *et al.* 2006a, Vrejoiu *et al.* 2006, Pintilie *et al.* 2007, Boerasu *et al.* 2013). For sol-gel-derived capacitors, under 300 kV/cm the leakage were even one or two orders of magnitude smaller

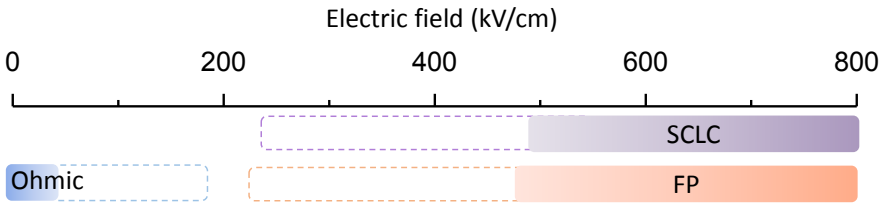

Figure 4.21: Well fitted charge transport mechanisms in different field ranges for sol-gel-derived PZT capacitors. Areas inside the dash lines means that in this field range leakage current is possibly due to this charge transport mechanism.

than sputtered capacitors but at higher field it increased faster. By fitting various models to the leakage currents, it was found that charge transport mechanism was complicated, varying with applied field range. At low field ($0 \sim 100\,kV/cm$) J_l of both sputtered and sol-gel-derived capacitors showed a linearly dependent on V, which was due to Ohmic conduction. From $\sim 200\,kV/cm$ to $800\,kV/cm$, SCLC was well fitted for capacitors of both types. In this range, other transport mechanisms were also successfully fitted to the data (SE for sputtered capacitors and FP for sol-gel-derived capacitors). Capacitors of sub–50 nm exhibited much higher leakage or were even too leaky to be measured with the top electrode size of 100 $\times$ 100 μm^2.

Theoretically, bulk and interface properties can be separated by testing capacitors with asymmetric electrodes. According to the results of sputtered capacitors, J-E curves were totally symmetric from capacitors with symmetric structure SRO/PZT/SRO. Even for Pt/PZT/SRO structure, J-E curves were almost symmetric. For sol-gel-derived samples, J-E curves were not symmetric for SRO/PZT/SRO capacitors and change of top electrode did not affect on the J-E curves. So the influence of top electrode on leakage current is very small. We also notice that among all well fitted models (see Figures 4.13 and 4.21), only Schottky emission (for sputtered capacitors) was interface-dominant mechanism.

Under high voltage, the breakdown was always from the top electrode (negative branch of J_l surged), probably due to the fact that more defects existed in the top interface. It is estimated that that bottom electrode provides a better morphology, thus the bottom interface has less defects than the top one.

Usually, leakage current J_l consists contributions from several different conduction mechanisms. For example, V^2 dependency of J_l may be due to the double injection or single injection in the trap-filled limit. Vertical jumps in a $J(V)$ curve can arise from breakdown or from field-induced emptying of filled traps (Scott 2000). Due to the complexity of transport mechanisms, $J(V)$, $J(T)$, $J(d)$ and $J(t)$ measurements together would help distinguish the different mechanisms.

4.2 Capacitance-Voltage Characteristics

The "butterfly" shape of a Capacitance-voltage (C-V) curve is the signature of ferroelectrics. C-V measurement is routinely used to obtain the permittivity of the ferroelectrics. Ferroelectric capacitors with high relative permittivity permit the electronic industry to continue increasing the chip bit-density since

their areas can be reduced as relative permittivity increases.

Capacitance was measured through the method illustrated in chapter 2. It is reported in many articles (Zhou and Newns 1997, Stengel and Spaldin 2006) that a dead layer is formed at ferroelectric-electrode interface due to the presence of defects, thus the film is divided into two parts: effective ferroelectric with thickness d_{eff} and thickness of the sum of the two dead layers at the two interfaces d_{dl}. Dead layer's relative permittivity $\varepsilon'_{r_{dl}}$ is much smaller than that of the effective part. d_{dl} is first evaluated and then ε'_r of PZT is extracted.

The linear capacitance C_l (mostly from the effective part) can be expressed by:

$$\frac{1}{C_l} = d_{eff}\frac{1}{\varepsilon_0\varepsilon'_{r_l}A} + d_{dl}\frac{1}{\varepsilon_0\varepsilon'_{r_{dl}}A} = \alpha d_{eff} + \beta \tag{4.11}$$

where ε_0 is the permittivity of free space, A is the surface of the capacitor. α and β (> 0) are the slope and intercept of the plot of reciprocal C_l as a function of thickness.

ε'_{r_l} can be extracted from the slope α. Then d_{eff} can be extracted by:

$$d_{eff} = \left(\frac{1}{C_l} - \beta\right)/\alpha \tag{4.12}$$

And the relative permittivity, ε'_r, of PZT capacitor can be obtained by:

$$\varepsilon'_r = \frac{Cd_{eff}}{\varepsilon_0 A} \tag{4.13}$$

where C is the measured capacitance from C-V measurement.

4.2.1 Relative Permittivity of Sputtered Capacitors

Capacitance-voltage (C-V) characteristics were performed at 1 kHz for sputtered PZT capacitors with SRO top electrode, as shown in Figure 4.22. Loss tangent of three thicker capacitors were between 0.01 and 0.1 as field varies. For 40.5-nm-thick capacitor, loss tangent exceeded 10 at high field. Loss tangent exhibited similar value for capacitors with same thickness as top electrode changed and in the following of this section, they will not be provided.

According to Equations (4.11) and (4.12), to obtain the linear capacitance ε'_{r_l} and effective thickness d_{eff} of the PZT capacitors, reciprocals of the linear capacitance C_l of these four capacitors were extracted and plotted in Figure 4.23.

By fitting the reciprocals of C_l in Figure 4.23, ε'_{r_l} was found to be 179 $\pm$ 15 and d_{dl} was about $1 \sim 2$ nm for all these four sputtered capacitor with SRO top electrode. Then ε'_r of PZT capacitors can be obtained by Equation (4.13). ε'_r of these four sputtered capacitors with SRO top electrode were extracted, as shown in Figure 4.24. Maximum permittivity seemed to be similar for SRO-top-electrode

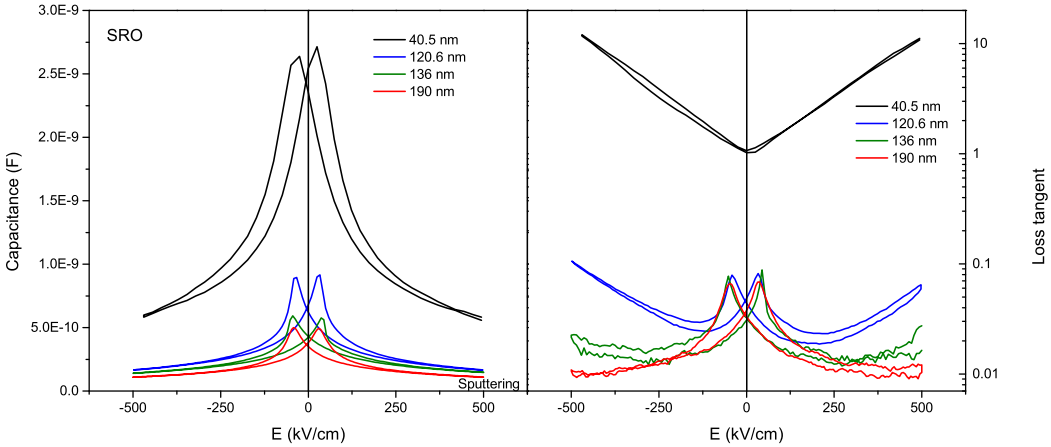

Figure 4.22: Capacitance-field curves and loss tangent of sputtered PZT capacitors with SRO top electrode.

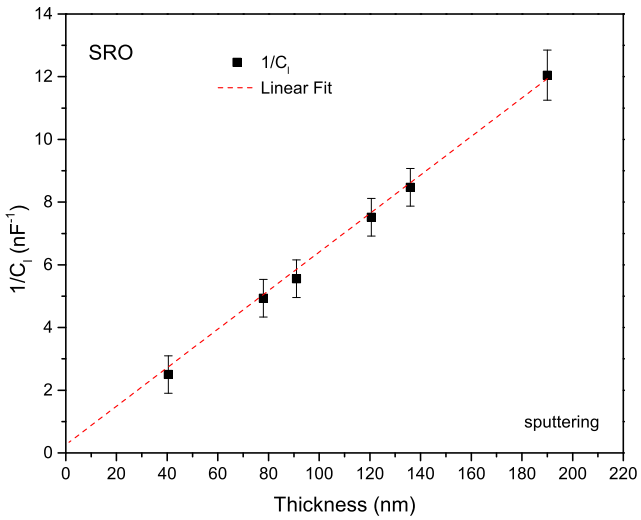

Figure 4.23: Reciprocal of C_l as a function of thickness of sputtered capacitors with SRO top electrode. (Data of 78-nm-thick and 91-nm-thick sputtered capacitor deposited in the same condition are added.)

sputtered capacitors.[6]

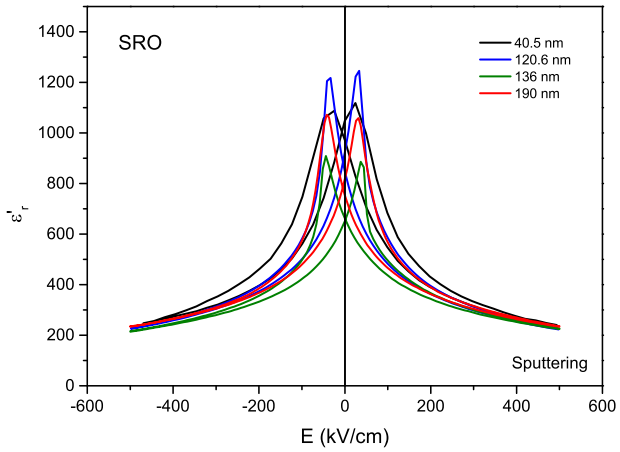

Figure 4.24: ε'_r as a function of field of sputtered PZT capacitors with SRO top electrode.

Then we extracted the linear permittivity ε'_{r_l} for Pt-top-electrode and ITO-top-electrode sputtered PZT capacitors, by calculating the slope of C_l's reciprocals, as shown in Figure 4.25. ε'_{r_l} for capacitors with Pt top electrode and ITO top electrode were 173 ± 15 and 155 ± 15, respectively.

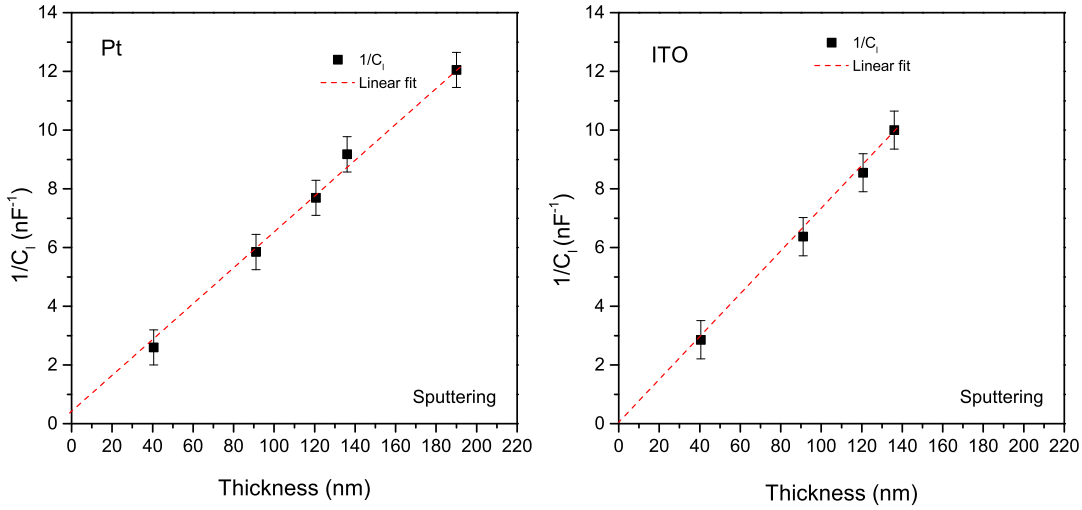

Figure 4.25: Reciprocal of C_l as a function of thickness of sputtered capacitors with Pt top electrode (left) and ITO top electrode (right).

d_{dl} was less than 3 nm for all these capacitors. Plot of ε'_r for sputtered capacitors with Pt top electrode and ITO top electrode is provided in Figure 4.26.

Sputtered PZT with Pt top electrode had similar permittivity as that of SRO-top-electrode capacitors in all thicknesses. ITO-top-electrode capacitors exhibited a much smaller permittivity.

[6] Different from the variation in J-E curves, C-E curves are much more reproducible for all capacitors with same thickness. So thickness dependence can be investigated here.

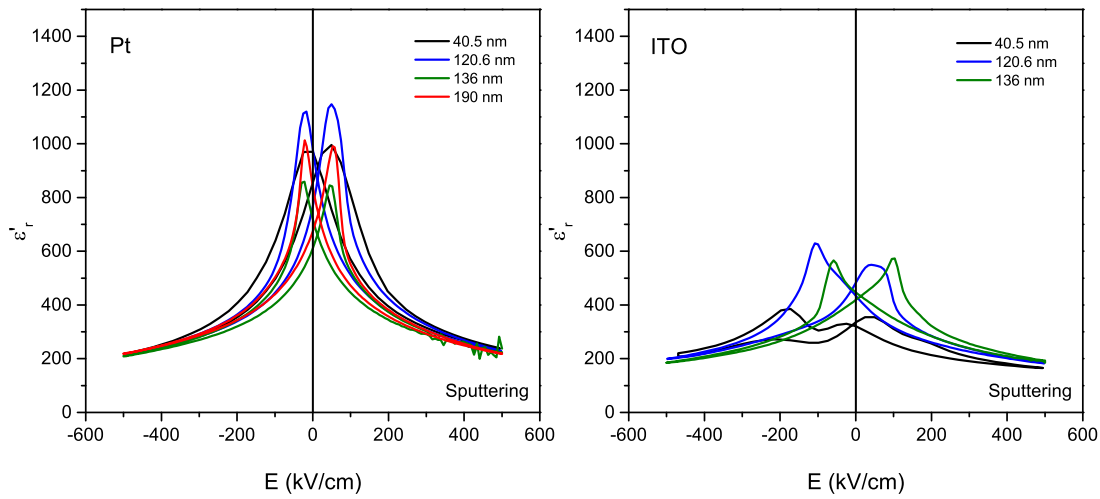

Figure 4.26: ε'_r as a function of field of sputtered PZT capacitors with Pt top electrode (left) and ITO top electrode (right).

4.2.2 Relative Permittivity of Sol-gel-derived Capacitors

C-V curves of sol-gel derived PZT capacitors have also been measured. Linear capacitances C_l of five capacitors of different thicknesses were extracted from C-V curves and their reciprocals are plotted in Figure 4.27. Linear permittivity ε'_{r_l} were extracted to be 178 ± 15 for SRO-top-electrode capacitors and 174 ± 15 for Pt-top-electrode capacitors. Loss tangent for all these capacitors with both top electrodes were similar, with values between 0.01 and 0.1 as field varied, same to that of sputtered capacitors.

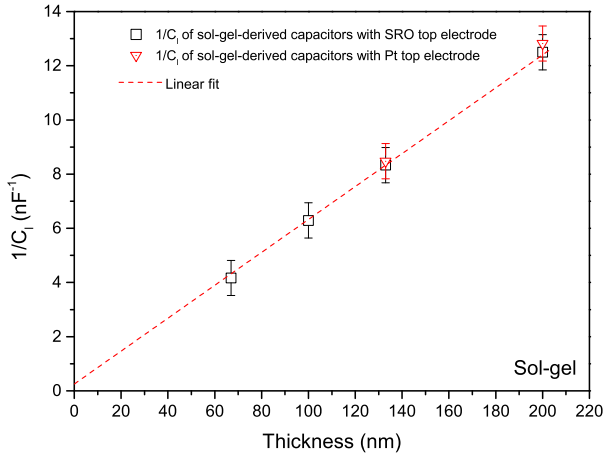

Figure 4.27: Reciprocal of C_l as a function of thickness of sol-gel-derived capacitors with SRO top electrode and Pt top electrode.

Dead layer thickness d_{dl} was $0.5 \sim 3\,nm$. ε'_r are plotted in Figure 4.28. Different from sputtered PZT, ε'_r of sol-gel-derived PZT with SRO top electrode showed a thickness dependency, thicker capacitor having smaller maximum of ε'_r.

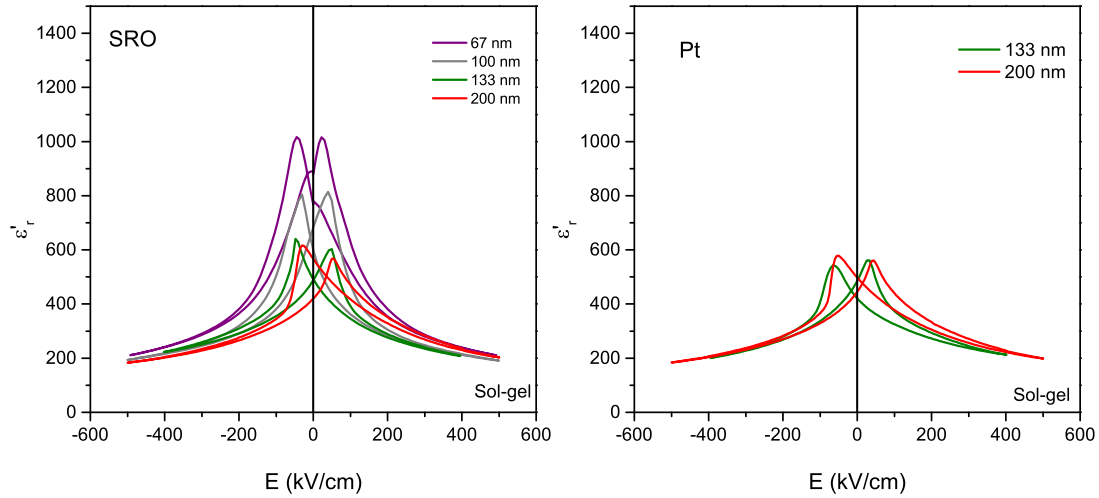

Figure 4.28: ε'_r as a function of field of sputtered PZT capacitors with SRO top electrode (left) and Pt top electrode(right).

4.2.3 Conclusion

Through C-V characteristics of the PZT capacitors, it is found that: 1) ε'_{r_l} was almost invariable for both sputtered and sol-gel-derived capacitors with various top electrodes ($\sim$ 170) ; 2) Maximum relative permittivity of sputtered capacitors showed no thickness dependency. The value was between 900 and 1300, which were in agreement with reported results (Perez 2004, Klee *et al.* 2010, Boerasu *et al.* 2013); 3) Maximum relative permittivity of sol-gel-derived capacitors (with SRO top electrode) decreased with thickness and maximum relative permittivity of thicker sol-gel-derived capacitors was much smaller than that of sputtered capacitors with equivalent thicknesses; 4) Dead layer thickness was less than 3 nm for all capacitors; 5) Loss tangent of sputtered capacitors and sol-gel-derived capacitors were similar (0.01 $\sim$ 0.1, except the leaky 40.5-nm-thick sputtered capacitor), regardless of top electrode. Film of sub–50 nm with 100 $\times$ 100 μm^2 top electrode exhibited considerably reduced qualities (40.5-nm-thick sputtered capacitor was extremely lossy and 33-nm-thick sol-gel-derived capacitor was too leaky to be measured).

4.3 Ferroelectric Hysteresis Loops

Hysteresis P-E loop is the unique feature of ferroelectrics. Measuring the P-E loop of a ferroelectric capacitor allow us to evaluate its ferroelectric properties. Large P_r and low E_c are favorable for the fabrication of ultrathin capacitors of high reliability.

4.3.1 P-E loops of Sputtered Capacitors

P-E loops have been obtained from these sputtered PZT capacitors with SRO top electrode by PUND measurement (details in Chapter 2), plotted in Figure 4.29. The three thicker PZT capacitors exhibited proper hysteresis loops, while the 40.5-nm-thick capacitor showed a proper PUND loop but a huge ring-like PN loop, indicating that the huge leakage current covered the switching current. Thanks to PUND

set-up, we can separate different contributions.

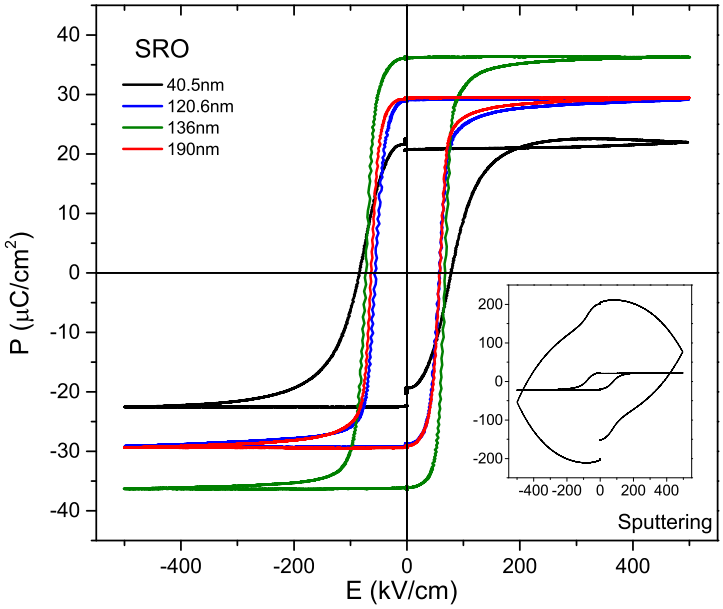

Figure 4.29: PUND loops of sputtered capacitors with SRO top electrode. Inset shows the PUND loop and PN loop of 40.5-nm-thick capacitor with SRO top electrode.

PUND measurements at various voltages were performed for the three thicker PZT films with SRO top electrode (40.5-nm-thick capacitor was too leaky to be measured at higher voltages). P_r and E_c were extracted from PUND loops, as shown in Figure 4.30. Polarization was saturated starting from 300 kV/cm to 900 kV/cm for 120-nm-thick and 190-nm-thick PZT, with the variation within 1 $\mu C/cm^2$ (136-nm-thick PZT has been measured only at 500 kV/cm).

In Figure 4.30, E_c were symmetric from 100 kV/cm to 500 kV/cm for all sputtered PZT capacitors. Under higher voltage, 190-nm-thick PZT showed a higher E_c^n.

Figure 4.31 presents the PUND loops of these capacitors with Pt top electrode and ITO top electrode, measured at 500 kV/cm. 40.5-nm-thick capacitor with Pt top electrode was not as leaky as that with SRO top electrode, but still had a much smaller P_r compared to that of thicker capacitors. And it also turned to be leaky under higher electric field. All ITO-top-electrode capacitors exhibited a much larger E_c, which will be discussed in chapter 5 .

P_r and E_c extracted from PUND measurements at various electric field are shown in Figure 4.32 for both Pt-top-electrode and ITO-top-electrode capacitors. 190-nm-thick capacitor with Pt top electrode also exhibited saturated P_r from 300 kV/cm to 800kV/cm. All three Pt-top-electrode capacitors showed a considerable positive asymmetricity (or imprint) in PUND loop in all measured fields. This difference between E_c^p and E_c^n was attributed to the asymmetric stack structure of the capacitor (Al-Shareef *et al.* 1995). The asymmetricity for ITO-top-electrode capacitors were not obvious given their large E_c.

Generally, it is observed that E_c decreases as thickness increases. But the thickness range in this work is very limited (40.5 $\sim$ 190 nm), and quantitative relation between coercive field and thickness could

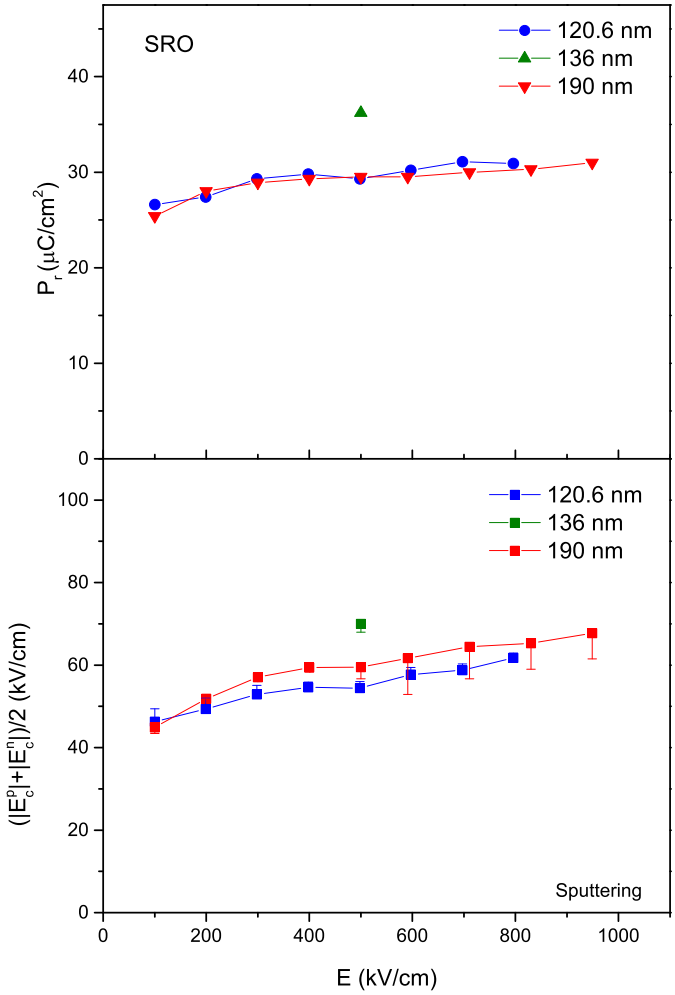

Figure 4.30: P_r and E_c as a function of field for sputtered capacitors with SRO top electrode. For the plot of E_c, mean value of positive coercive field E_c^p and negative coercive field E_c^n is plotted. Error bar is used to indicate the degree of asymmetricity of hysteresis loop (asymmetricity $= E_c^p - E_c^n$). Positive value means the loop shifts along positive direction on field-axis ($E_c^p > E_c^n$).

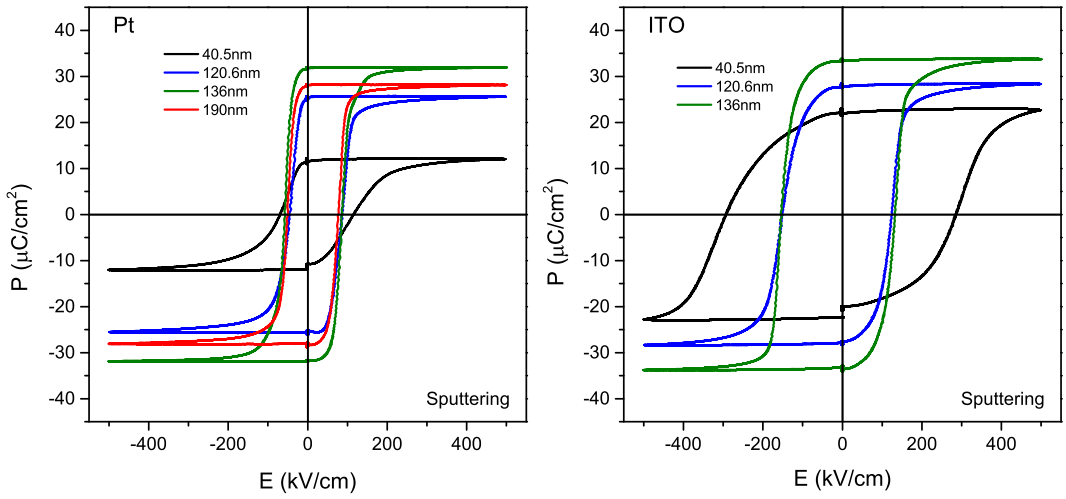

Figure 4.31: PUND loops of sputtered capacitors with Pt top electrode (left) and ITO top electrode (right).

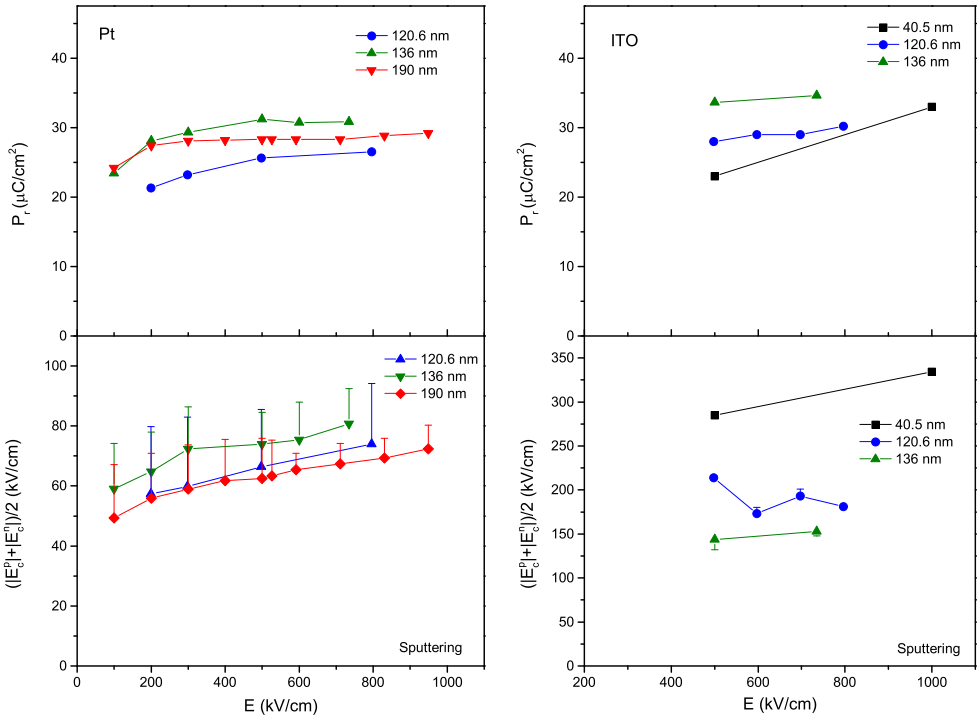

Figure 4.32: P_r and E_c as a function of field for sputtered capacitors with Pt top electrode (left) and ITO top electrode (right).

not be extracted precisely. There is a semi-empirical scaling law,

$$E_c \propto d^{-2/3} \tag{4.14}$$

Equation (4.14) is successful in describing the thickness dependence on E_c in the last several decades for films of $100\,nm \sim 200\,\mu m$ (Scott 2000). According to some variations (Janovec 1958, Kay and Dunn 1962) of this thickness dependence, the external charges are assumed to reside on a plane of negligible thickness at the interfaces, compensating for the polarization inside the ferroelectric. However, in realistic cases charges are distributed over a small finite region in the metallic electrodes. This spatial charge distribution leaks to a voltage drop in the metallic electrodes, and a compensating depolarization potential across the ferroelectric film is formed to ensure the whole structure is equipotential (Mehta 1973). Equation (4.14) expects much higher E_c for ultrathin (<10 nm) ferroelectric capacitors, which is inconsistent with experimental data. Dawber *et al.* (2003) included the depolarization field E_d, and his modified scaling law well fitted the data from 1 nm to 1 μm for polyvinylidene fluoride (PVDF) ferroelectric film. Compared to Dawber's data for PZT from 50 nm to 5 μm (Dawber *et al.* 2003), which was well fitted ($log(E_c) \propto -0.66\,log(d)$), our data from SRO-top-electrode and Pt-top-electrode sputtered capacitors is in the same fitting line.

4.3.2 P-E loops of Sol-gel-derived Capacitors

Four sol-gel-derived PZT capacitors (except the 33-nm-thick capacitor, which showed huge leakage current) have been also investigated under PUND pulse trains. PUND loops were measured as maximum electric field was kept at 500 kV/cm , as shown in Figure 4.33.[7] From the shape of hysteresis loops, we noticed that capacitors with thickness more than 100 nm had more square-like loop, indicating the domain motion occurred in a narrow electric field range near coercive field.

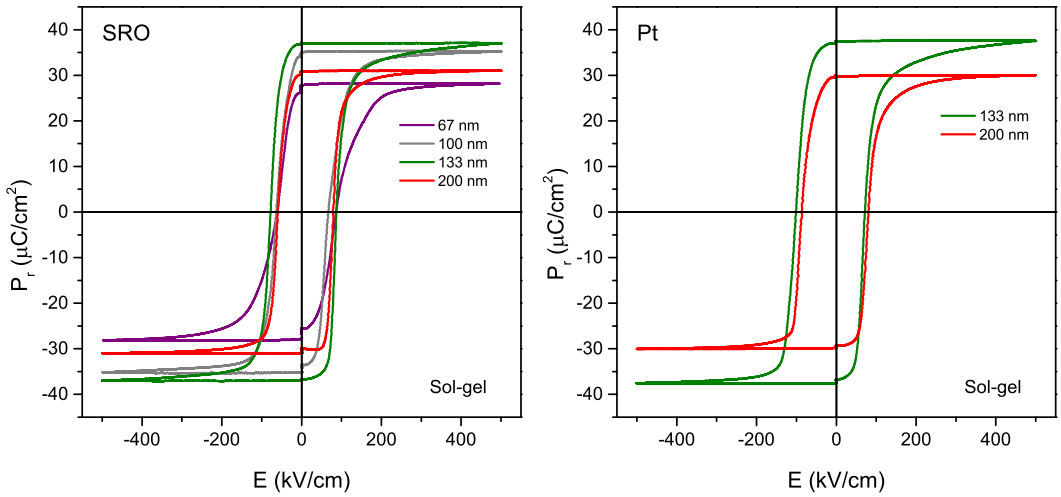

Figure 4.33: PUND loops of sol-gel-derived capacitors with SRO top (left) electrode and Pt top electrode (right).

These sol-gel-derived capacitors have also been measured at various voltages. P_r and E_c were extracted, as shown in Figure 4.34. For the 67-nm-thick PZT capacitor, P_r increased almost linearly as drive voltage increased. For 100-nm-thick, 133-nm-thick, increment of P_r was smaller as V_{max} increased. P_r of 200-nm-thick capacitor exhibited much better saturation quality.

Sol-gel-derived capacitors with SRO top electrode exhibited symmetric PUND loops or loops with small asymmetricity. Pt-top-electrode sol-gel-derived capacitors exhibited negative asymmetricity ($|E_c^p| < |E_c^n|$), which was opposite to the positive asymmetricity, observed in sputtered capacitors with Pt top electrode. The value of E_c was comparable to that in sputtered capacitors.

At 2250 kV/cm, the 200-nm-thick capacitor with SRO top electrode broke down, and the same sample with Pt top electrode broke down at 2925 kV/cm. It was usually found that Pt-top-electrode capacitors had higher breakdown field.

4.3.3 Conclusion

By performing PUND measurement, the switching behavior of these ferroelectric capacitors have been investigated. Except sub–50 nm capacitors, all showed PUND loops with square-like shapes. P_r were between 25 and 40 $\mu C/cm^2$ for all capacitors except sub–50 nm ones, which were among the highest

[7] P_r of 200-nm-thick capacitor increased to 40 $\mu C/cm^2$ after various measurements (sometimes at elevated temperature) after 3 months. The reason was unknown. P_r of other samples, which have been measured much less, did not change.

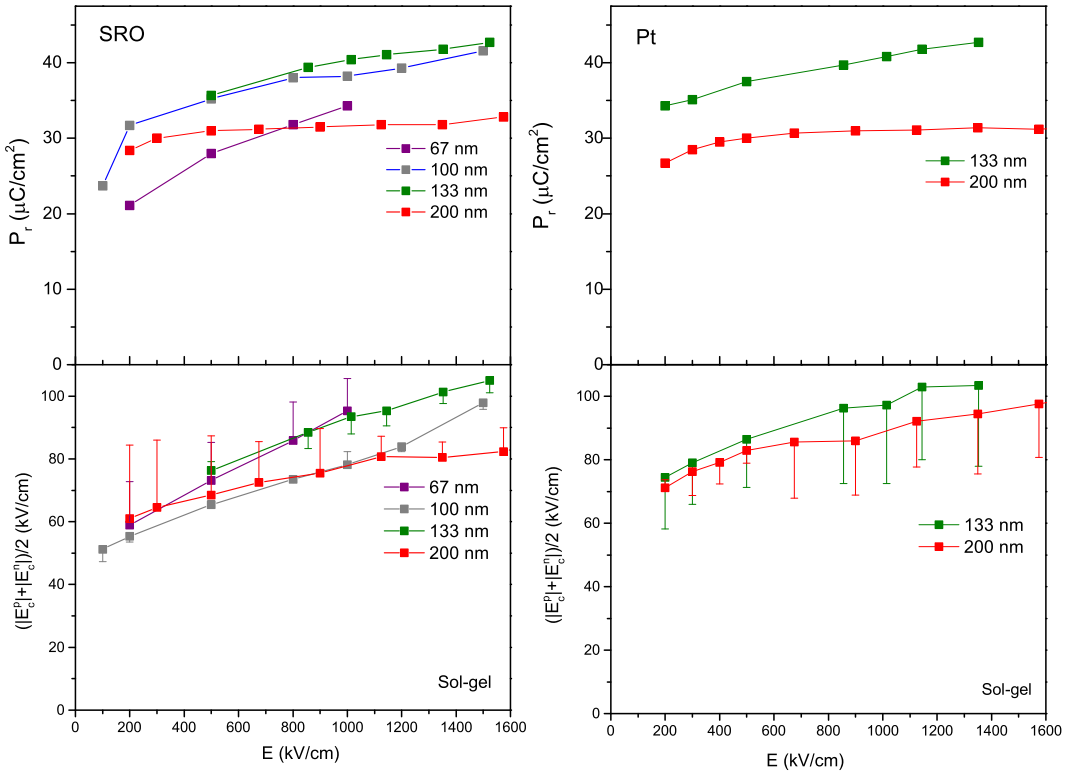

Figure 4.34: P_r and E_c as a function of field for sol-gel-derived capacitors with SRO top electrode (left) and Pt top electrode (right).

values in recent reported results for thin-film PZT(52/48) capacitor (Lee *et al.* 2005, Kim *et al.* 2006, Chen *et al.* 2007, Dekkers *et al.* 2009). Along with the I-V and C-V results, we found that PZT film of both growth routes with a thickness more than 100 nm exhibited excellent electrical properties in terms of low leakage, high maximum relative permittivity, small loss tangent and high remnant polarization.

Asymmetric stack structure affected imprint property of the capacitor. However the asymmetricity in sputtered Pt/PZT/SRO capacitors and in sol-gel-derived Pt/PZT/SRO capacitors were opposite. Thicker capacitor was better saturated under higher field than thinner ones. These capacitors can stand 1000 kV/cm without obvious degradation.

No obvious dependence of P_r on thickness was observed, which might due to our limited thickness range. The relatively smaller P_r exhibited in thin capacitors (40.5-nm-thick sputtered capacitor and 67-nm-thick sol-gel-derived capacitor) was attributed to their worse quality (may be higher throughout-thickness defect densities). Kim *et al.*'s work (2006) on PZT(52/48) showed that P_r increased from only 3 $\mu C/cm^2$ to 50 $\mu C/cm^2$ as thickness varied from 40 nm to 1.5 μm. However, Kijima's study on PZT ranging from 25 nm to 100 nm showed almost identical P_r (22 $\mu C/cm^2$) for all capacitors (Ishiwara *et al.* 2004). Larsen *et al.*'s work (1994) on PZT(51/49) of various thicknesses (from 120 nm to 690 nm) showed similar P_r for all capacitors ($\sim$ 20 $\mu C/cm^2$). Yanase *et al.*'s work (1999) on totally strained BTO showed that from 12 nm to 79 nm, the variation of P_r was very small and he attributed the thickness dependence of ferroelectricity to the imperfection of the crystal structure at the ferroelectric-metal interfaces.

4.4 Piezoresponse Force Microscopy

Macro-scale ferroelectric characterization techniques (I-V, C-V, PUND) are of limited capacities in studying domain-level properties of ferroelectric thin films. The application of PFM permits non-destructive, high resolution, local imaging at nano-scale, providing us an unique opportunity for the investigation of domain dynamics. As the scale decreases to the size of a tip, huge leakage current in macro-scale characterization can be greatly reduced or avoided. PFM can also be easily used to investigate the stability of the switched domains (retention measurement).

4.4.1 PFM Imaging of Sputtered PZT Films

Figure 4.35 shows the topography, amplitude and phase response of the 190-nm-thick[8] sputtered PZT film after "writing". The clear contrast shown in phase image indicated that the film was piezoelectric and the domains were manipulated by the voltage applied on the film. The three squares from big to small were written by a voltage of 5 V, –5 V and 5 V one by one. We notice that the most outside zone which had not been not written showed a phase response similar to the zone which was written by –5V. This similarity indicated that after the film was fabricated, it showed a strong polarization preference for the upward direction. Same result was observed by Jung *et al.* (2005) for their as-fabricated $PbTiO_3$. According to Ahn *et al.*'s work (2005) on $PbTiO_3$, all as-fabricated film with a thickness more than 12 nm exhibited upward polarization.

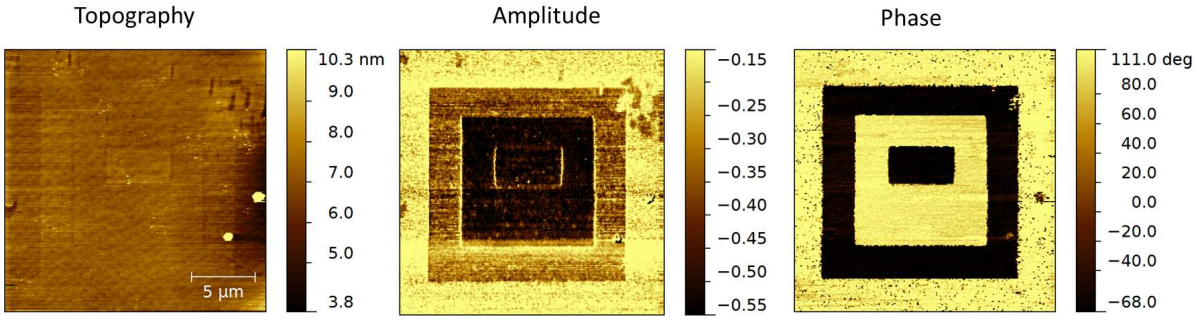

Figure 4.35: PFM images of 190-nm-thick sputtered PZT film.

4.4.2 Switching Spectroscopy of Sputtered PZT Films

Figure 4.36 shows the PFM switching spectroscopy of 190-nm-thick sputtered PZT film. Both the phase loop and amplitude loop (direction: anticlockwise) were obtained by taking the average of 10 loops from different locations on the film. The difference between the top and the bottom in the phase loop was around 180°, indicating that the c-domains in the PZT film were switched up and down by the drive voltage. The response of amplitude showed a drop near the coercive field to almost zero, at which point,

[8]The PFM imaging of other sputtered PZT films have not been carried out yet. Retention quality of these sputtered PZT also has not been measured.

the polarization was about zero.

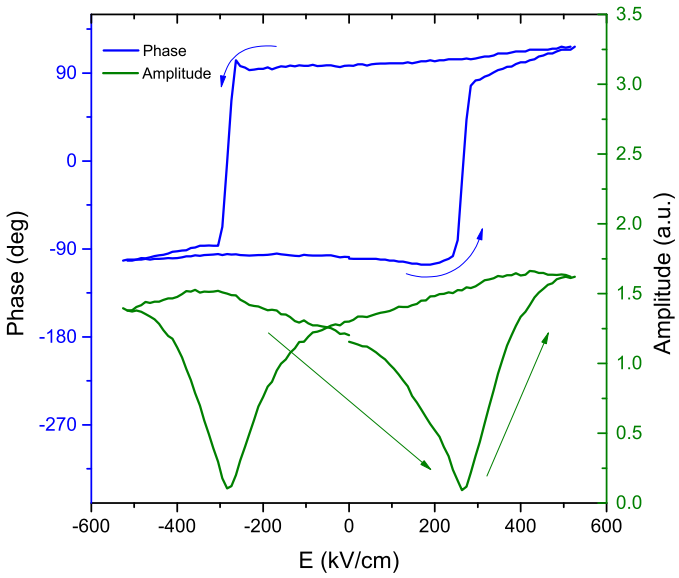

Figure 4.36: PFM loops of 190-nm-thick sputtered PZT film.

4.4.3 PFM Imaging of Sol-gel-derived PZT Films

PFM study of sol-gel-derived films were also carried out. Figure 4.37 shows the topography, amplitude response and phase response of five sol-gel PZT films. All these films showed clear contrast in squares written by opposite DC bias voltages in phase response except the 100-nm-thick film, which was annealed in tubular furnace for 3 hours (other four only experienced short time RTA annealing). We have to bear in mind that 33-nm-thick PZT film in Macro measurement was too leaky to be tested. As PFM studies nano-scale domain properties, ferroelectric film which is leaky in macro-scale measurement still can clearly demonstrate converse piezoelectric effect and ferroelectric property. It was noticed that all non-written areas (the most outside part) of the four sample (except 100-nm-thick one) had a positive polarization, which was the as-fabricated state of these films, similar to sputtered films. For 100-nm-thick PZT film, its reduced response compared to other films indicated the long period annealing changed the crystalline structure which affected its domain behaviors.

The converse piezoelectric effect that 200-nm-thick PZT film exhibited was more obvious than others, indicated by the sharp contrast and homogeneous color both in positive- and negative-voltages-written areas in phase response. This was compatible with its good PUND shape and more saturated polarization quality. For 33-nm-thick, 67-nm-thick and 133-nm-thick films, the contrast in phase were less strong than that in 200-nm-thick PZT film.

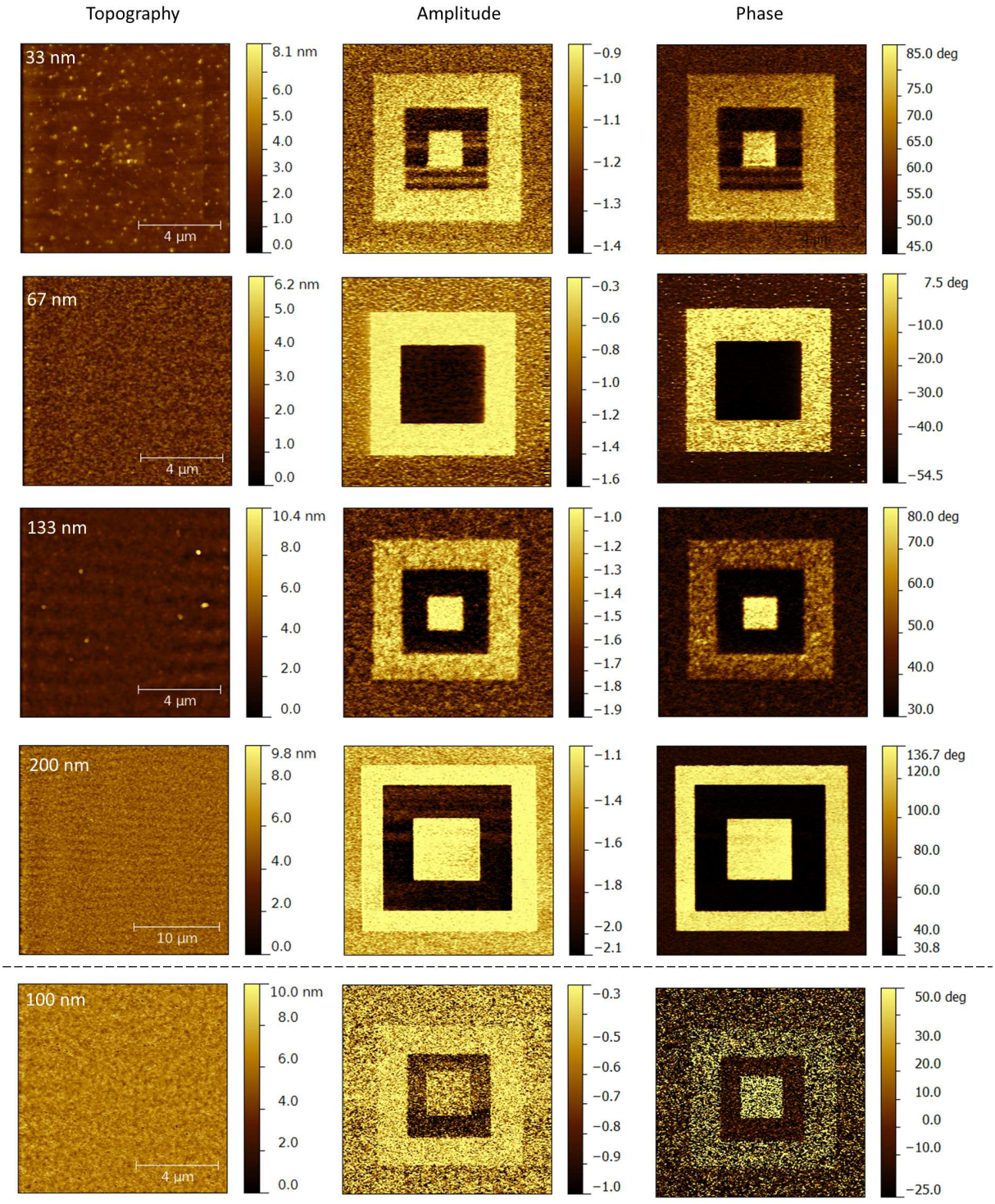

Figure 4.37: PFM images of sol-gel-derived PZT films of various thicknesses after writing opposite squares. (100-nm-thick PZT is listed apart from others for the reason that it has experienced 3 h post annealing while others have experienced only 1 min RTA.)

4.4.4 Switching Spectroscopy of Sol-gel-derived PZT Films

Figure 4.38 shows the PFM switching spectroscopies of the five PZT films. All of these five PZT films showed the typical response of piezoelectric material both in amplitude and in phase.

For the 33-nm-thick film, which was too leaky to be measured in macro-scale measurements, coercive electric field was as big as 1000 kV/cm while the others range from 100 kV/cm to 250 kV/cm. The much higher observed E_c might be due to leakage, since the film was much leaky than others and a large amount of charges might flow across the film during the measurement, forming a fake high E_c.

4.4.5 Retention of Sol-gel-derived PZT Films

All domains in five samples were re-read after some time to check the retention quality. Figure 4.39 shows the phase response to the AC drive bias.

The phase response of 200nm-thick film showed no degradation after 3 h which was much better than the slightly reduced contrast in the three thinner films.

100-nm-thick PZT film acted differently. The central up-domain remained pointing upward without any relaxation as time passed while the down-domains switched upward gradually, indicating that even the domains could be manipulated by external field but the domains exhibited a strong upward preference. Just after 5 min of writing, a lot down-domains have already switched back. After 4 h, most of its domains have switched upward. The bad quality of 100-nm-thick film was directly linked to the damaging annealing in furnace for 3 h.

4.4.6 Conclusion

Film of about 200 nm PZT fabricated by both routes showed great converse piezoelectric effect while thinner sol-gel-derived films exhibited reduced converse piezoelectric effect. All as-fabricated PZT films showed an upward polarization. This might be due to the clamping force from underlying SRO layer. 200-nm-thick sol-gel-derived film showed high retention without and degradation after 3 h while thinner sol-gel-derived films exhibited degraded retention quality. Long period post annealing in furnace showed a destructive effect on the film piezoelectricity.

4.5 Summary

In this chapter, the electrical properties of both sputtered and sol-gel-derived capacitors have been investigated. All films (except sub–50 nm) showed low leakage, regardless of growth route and top electrode. At low field range, sol-gel-derived capacitors showed one or two orders of magnitude lower leakage. Charge transport mechanism has been analyzed by fitting various models to leakage data and the fitting results showed that at different field range the dominant mechanism was different, showing the complexity of

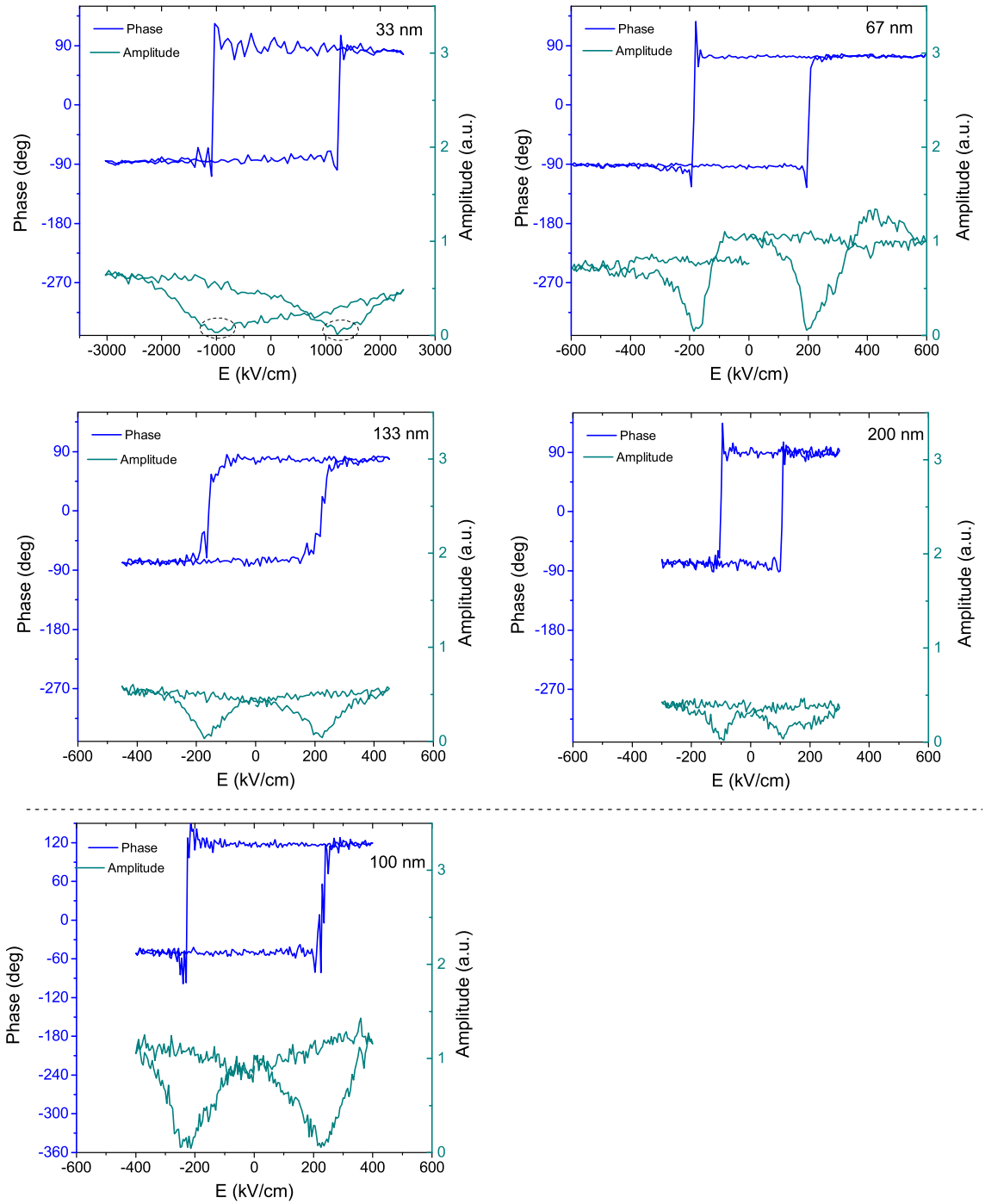

Figure 4.38: PFM loops of sol-gel-derived PZT films of various thicknesses. (100-*nm*-thick PZT is listed apart from others for the reason that it has experienced 3 *h* post annealing while others have experienced only 1 *min* RTA.)

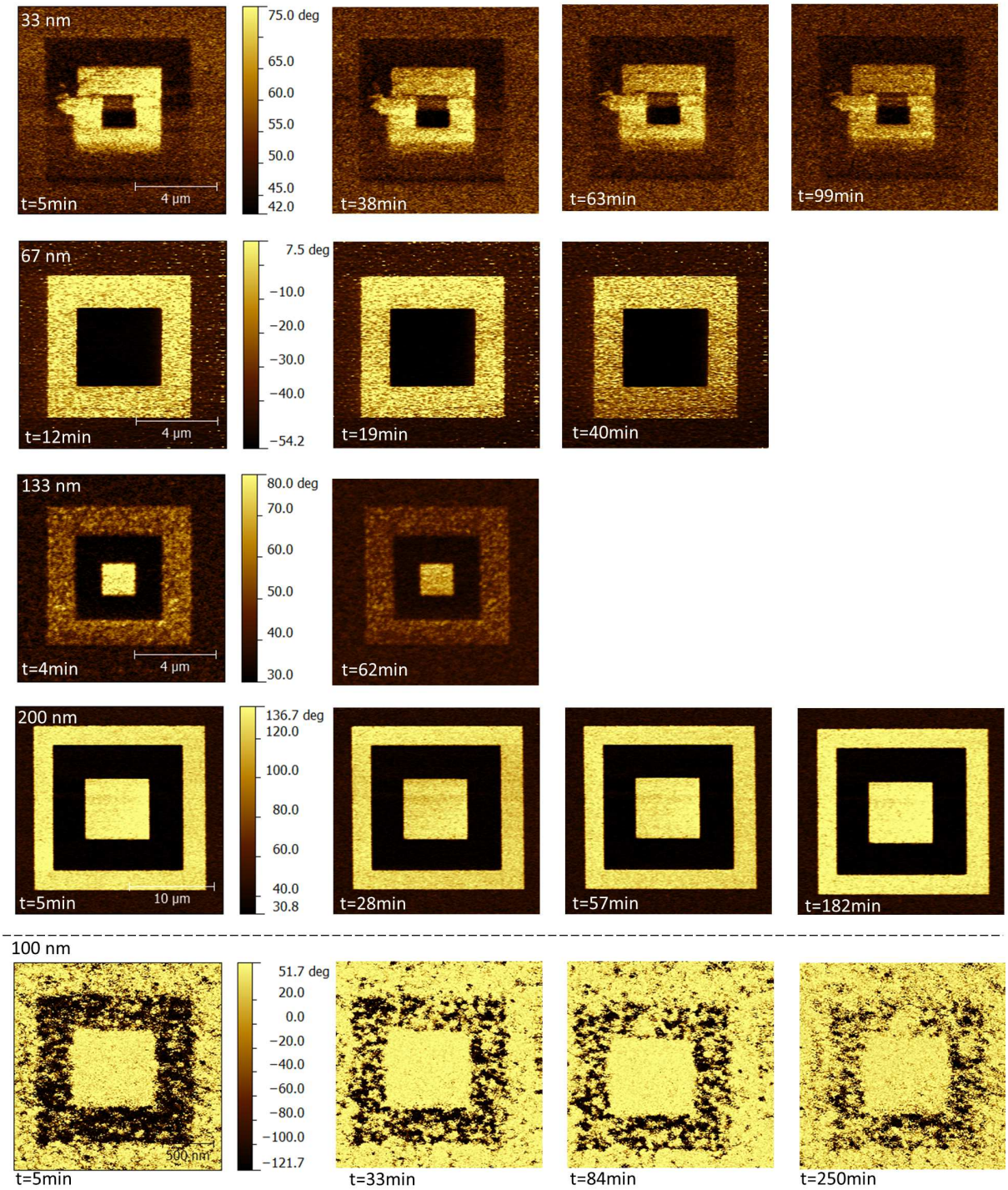

Figure 4.39: PFM retention of sol-gel-derived PZT films of various thicknesses. (100-*nm*-thick PZT is listed apart from others for the reason that it has experienced 3 *h* post annealing while others have experienced only 1 *min* RTA.)

charge transport mechanism in ferroelectrics. Maximum of relative permittivity were between 600 and 1300, which were in agreement with literature for PZT(52/48). Thickness of dead layer was estimated to be less than 3 nm for all capacitors, meaning that very few defects existed at the interface. All capacitors with PZT of 100 to 200 nm exhibited square-like P-E loops. P_r of all capacitors (except sub–50 nm) were between 25 and 40 $\mu C/cm^2$, which were in good agreement with reported results. Capacitors with symmetric structure SRO/PZT/SRO showed no imprint, regardless of growth route; capacitors with Pt top electrode showed some degree of imprint; capacitors with ITO top electrode showed broadened P-E loops. PZT capacitors of about 200 nm of both types showed great saturation quality. 200-nm-thick sol-gel-derived film showed good converse piezoelectric effect and long period retention without degradation while thinner ones showed inferior qualities.

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Chapter 5

Detailed Studies of PZT Capacitor Electrical Properties

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In the previous chapter, leakage currents, capacitances and P-E loops of PZT capacitors were presented. In this chapter, P-E loops measured at different frequencies will be presented, accompanied by the fitting results to different models. The contributions of charges during domain switching will be analyzed through the comparison between static I-V, C-V measurements and dynamic PUND measurements. E_c will be further studied by carrying out PUND measurement at different temperatures. At the end, the imprint property will be analyzed.

5.1 Frequency Dependence of Coercive Field

P-E loops are usually measured at line frequencies of 60 Hz (USA) or 50 Hz (Europe) by Sawyer-Tower method for convenience. With readily accessible apparatuses, reproducible values of E_c and P_r can be extracted. In this work, we used PUND measurement for its ability to separate the switching part from the whole charge flows. The hysteresis loops were routinely measured at an equivalent frequency of 250 Hz. The frequency of PUND measurement is defined as follows, one cycle contains the non-zero drive voltage part of pulse "P" and pulse "N", thus $f = 1/4t_{inc}$, as illustrated in Figure 5.1. E_c is found to be frequency dependent. Since ferroelectric capacitors will be employed as memories, which operates at hundreds of MHz, it seems essential to figure out their exact relationship. In practical applications, a small V_c (relative big E_c for an ultrathin film can also provides a small coercive voltage V_c) at high frequency is favorable to memory applications, since computer memory components usually work under several volts. For a 100-nm-thick ferroelectric capacitor with $E_c = 100kV/cm$, V_c is 1 V but the operating voltage is usually about three times of V_c to ensure that all domains are switched.

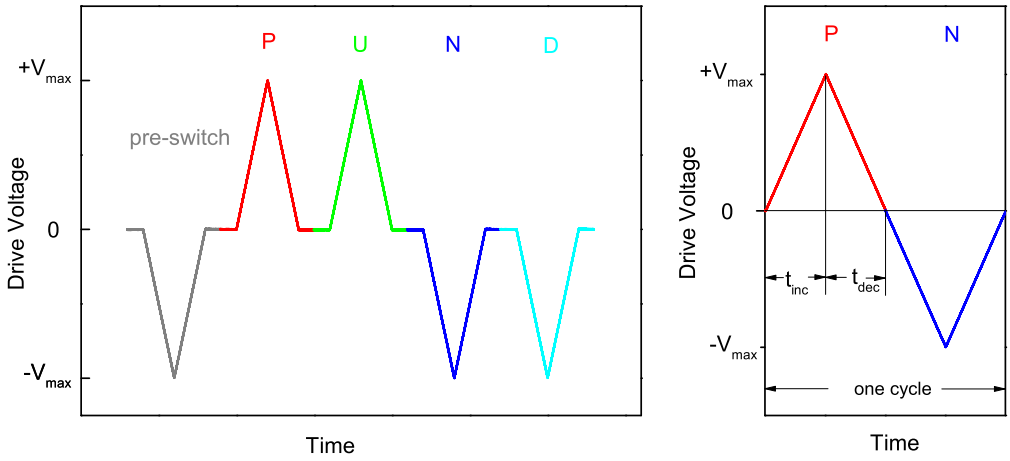

Figure 5.1: Definition of frequency in PUND measurements. Left shows a complete voltage signal of PUND measurement and right defines one cycle of signal.

The reason that why E_c is dependent on frequency is that domain switching takes a short period to accomplish. When the input signal frequency is too high, short voltage rising time t_{inc} leaves domains insufficient time to achieve switching. Thus a longer period is needed to accomplish switching, which means higher E_c is observed. Domain switching involves domain wall motion except at extremely high fields or extremely small capacitors (Scott 2000). Domain motion encounters a certain resistance or viscosity which increases with frequency.

Figure 5.2 shows PUND loops measured at different frequencies. As frequency decreased from 250 kHz to 250 Hz (t_{inc} increased from 10 μs to 1 ms), E_c was greatly reduced and P_r kept unchanged. When the input frequency continued dropping to 25 Hz, the change in E_c was indistinguishable and P_r increased a little. This is because a small amount of domains which were non-switchable at relatively high frequency switched due to the long lasting field applied on the capacitor. And $P^\star$ increased 30% (in

PN loop) due to the increased leakage current (indicated by larger I_U and I_D).

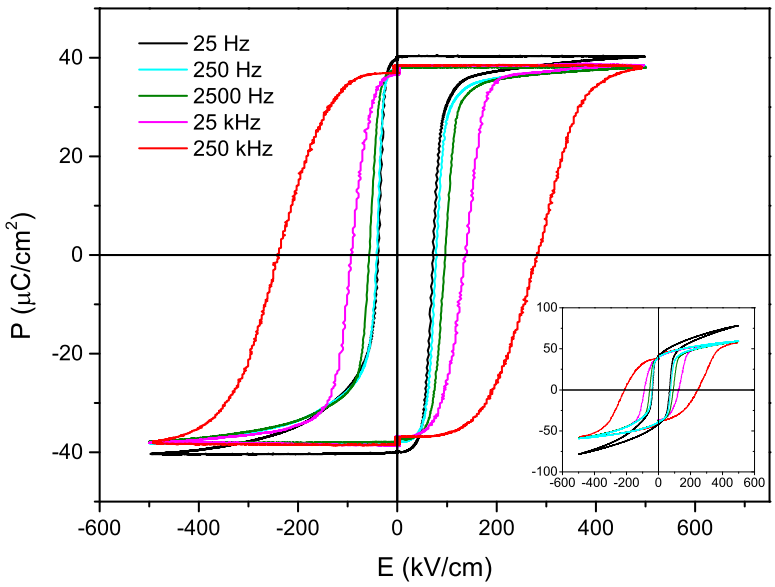

Figure 5.2: PUND loops of 200-nm-thick sol-gel-derived PZT capacitor with Pt top electrode measured at various frequencies. Inset shows the corresponding PN loops.

Due to the apparatus limit, we could not collect the output current when f exceeded 250 kHz. According to Hashimoto *et al.* (1994) , at even higher frequency, E_c will exceed the maximum input field and only part of the domains will switch, thus P_r will drop and PUND loop looks like an irregular oval.

E_c extracted from PUND loops are plotted in Figure 5.3. Measurement at various frequencies was carried out on a 200-nm-thick sol-gel-derived PZT capacitor with Pt top electrode. Positive asymmetricity was observed at all frequencies measured. When f increased from 0.025 Hz to 50 Hz, E_c kept stable. As f continued increasing, E_c increased in a roughly exponential manner.

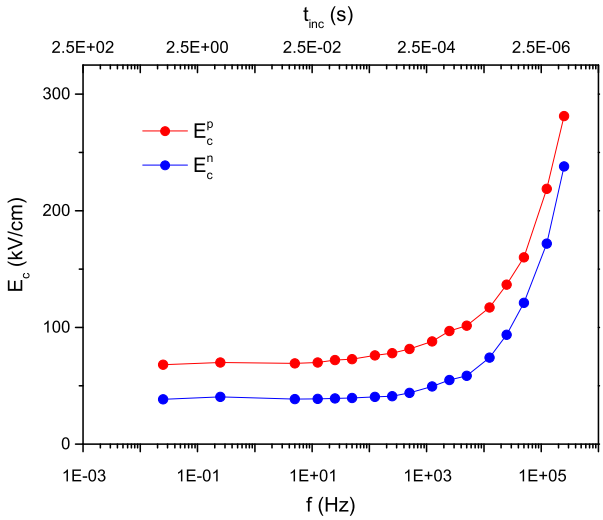

Figure 5.3: E_c as a function of frequency. Data from 200-nm-thick sol-gel-derived PZT capacitor with Pt top electrode.

Jung *et al.* (2002) described the different stages in domain switching process, as shown in Figure 5.4. When a reversal field (bigger than E_c) is applied on a ferroelectric capacitor, needle-like nucleus form near the interface between electrode and PZT and often at imperfect sites (Merz 1954). Then new domains grow throughout the thickness, accompanied by domain wall (DW) movement (forward or lateral, depending on the material). In the last several decades, there have been several models proposed to describe this frequency dependence, giving different importance to nucleation and DW movement. Now we will introduce these models and then fit them to our data.

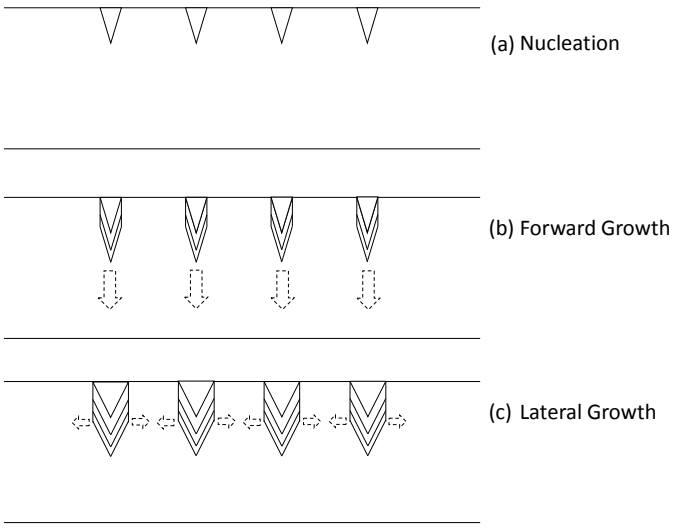

Figure 5.4: Domain switching stages. Nucleation, usually at anode or cathode. (b) Needle-like domains move parallel to the applied field; (c) Lateral growth. The speed-limiting parameter can be (a), (b) or (c) for different materials (Ishiwara *et al.* 2004).

5.1.1 I-O Model

Ishibashi and Orihara's model (Ishibashi and Orihara 1995) is based on the Kolmogorov-Avrami model (Kolmogorov 1991, Avrami 1939 1940 1941). In I-O model, the limiting factor in switching is assumed to be domain wall movement, including both forward and sideways growth (Scott 2006).

In I-O model, the relation between E_c and f is described as follows:

$$E_c \propto f^{\frac{D}{k}} \tag{5.1}$$

where D is dimensionality of domain motion and k is a parameter connected with input signal waveform. Dimensionality $D = 1$ means that domain boundary moves along one direction after the formation of plate-like nuclei; $D = 2$ means that the boundary moves two dimensionally after forming cylindrical nuclei; $D = 3$ means that the boundary moves three dimensionally after forming spherical nuclei, illustrated in Figure 5.5 (Ishibashi and Takagi 1971).

In Figure 5.6, our result is plotted in $log - log$ form according to Equation (5.1). No linear fit

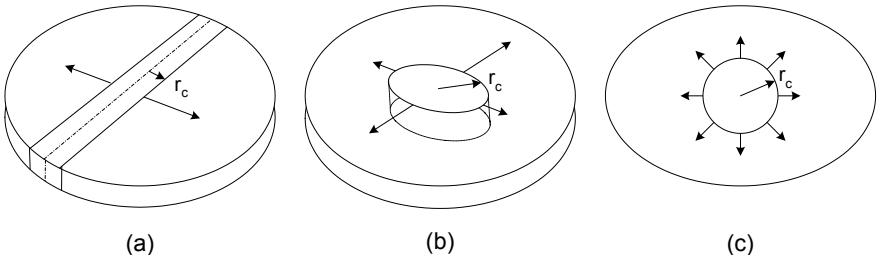

Figure 5.5: Dimensionality of domain growth. (a), (b) and (c) are correspondent to one, two and three dimensional cases, respectively. r_c is the radius of nucleus. (Prasertchoung 2006)

is possible to meet the data. Jung *et al.* (2002) showed a good fit to PZT, BTO, SBT and KNO_3 by applying I-O model to their data. However, the frequency range of their data was limited between 100 Hz to 100 kHz.

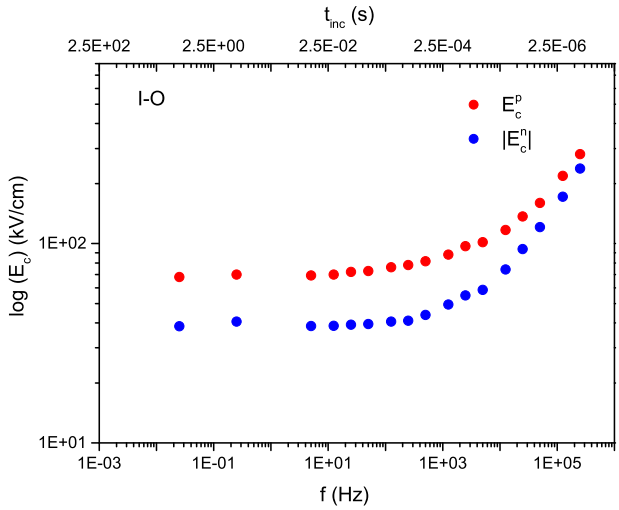

Figure 5.6: Plot of E_c at various frequencies according to I-O model.

5.1.2 D-C Model

Du and Chen (1997) built a model based on a different assumption from I-O model. Though domain wall movement are still considered, the speed-limiting factor is assumed to be nucleation. They assume under low field domain walls are immobile because they are trapped in potential well. Domain wall needs to nucleate a bulge to escape the potential well. The bulge is assumed to have a shape of spherical cap with a wall energy of γ. Trapped walls have a energy of $(\gamma - \gamma_B)$, where γ_B is the binding energy between wall and defects.

When the bulge is at a critical radius of R^*, the critical nucleation energy is:

$$\Delta G^* = \frac{4\pi {\gamma_B}^2 \gamma}{(E\Delta P)^2} \tag{5.2}$$

where ΔP is the polarization change effected by the passing domain wall, which equals to $2P_r$ for a fully polarized case.

As domain switching is assumed to be essentially affected by nucleation, domain wall sweeping time is short compared to the nucleation motion via the bulge formation. Switching rate under an AC field, is given by:

$$f = f_0 \exp\left(-\frac{\Delta G^*}{k_B T}\right) \tag{5.3}$$

where k_B is Boltzmann constant and T is temperature in K.Thus we can obtain:

$$lnf = lnf_0 - \frac{1}{k_B T}\left[\frac{\pi {\gamma_B}^2 \gamma}{{P_r}^2}\right]\frac{1}{E_c} \tag{5.4}$$

where f_0 is the limiting switching frequency, above which the critical bulge can not form and the switching motion will be hindered.

The model was fitted to our data, as shown in Figure 5.7. D-C model provided a good fit from 50 Hz up to 250 kHz. However this model did not predict the limit of E_c at low frequency. As frequency varied in the range under 50 Hz, no obvious change happened in E_c, which was incompatible with D-C model.

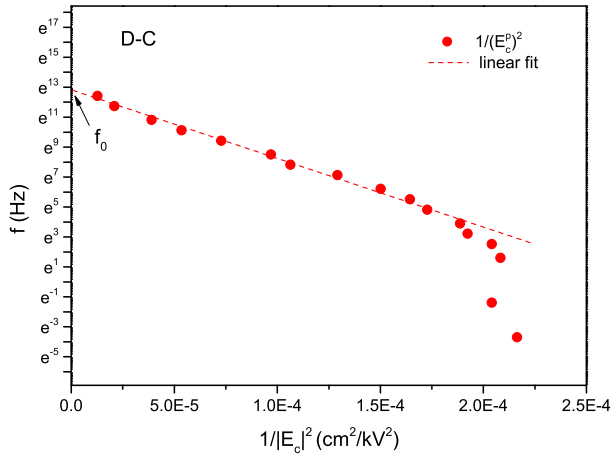

Figure 5.7: Plot of E_c at various frequencies according to D-C model. (E_c^n is not plotted here, which shows similar result.)

According to Poykko and Chadi (1999), Ganpule *et al.* (2001), Tybell *et al.* (2002), γ is about 0.1 $\sim$ 0.2 J/m^2. From the slope in Figure 5.7, we obtained that $\gamma_B = 0.068 \sim 0.095\ J/m^2$.

From the intercept in Figure 5.7, the limiting switching frequency f_0 was also extracted to be 400 kHz (the corresponding $t_{inc} = 0.625\ \mu s$). 400 kHz is much smaller than the speed of memories used nowadays. Tsurumi *et al.* (2001) have measured frequency dependence for PZT capacitors of different sizes and have found f_0 was dependent on the capacitor size. Small capacitor exhibited a higher f_0. As the capacitor area in this work is $100 \times 100\,\mu m^2$, which is relatively huge comparing to the capacitors in commercial use. For capacitor with lateral size of sub-micron, f_0 can increase several orders of magnitude.

5.1.3 L-Y-D Model

In L-Y-D (R. Landauer, D. R. Young and M. E. Drougard) theory (Landauer *et al.* 1956), nucleation is considered as extremely unimportant because domains do not contribute to the displacement current until they are created (Jung *et al.* 2005). In L-Y-D model, E_c is related with the ramp rate, $\mathrm{d}E(t)/\mathrm{d}t$, as follows:

$$ln\left(\frac{\mathrm{d}E(t)}{\mathrm{d}t}\right) = ln\left[\frac{\nu E_c}{b}\sum_{k=1}^{n}(-1)^{k+1}\frac{k!E_c^k}{\alpha^k}\right] - \frac{\alpha}{E_c} \tag{5.5}$$

where ν is a rate constant which is independent of field and polarization, $b = ln(1/2)$ and α is activation field, which is related to the threshold field needed to initiate nucleation. Equation (5.5) is practical for triangular input form since the rise rate is kept constant.

Figure 5.8 shows the fitting result of L-Y-D model to our data. According to this fit, $n = 3$ for both curves. L-Y-D model had a good fit in all frequency range and succeeded in predicting a minimum limit for E_c as frequency continued decreasing when passing 50 Hz.

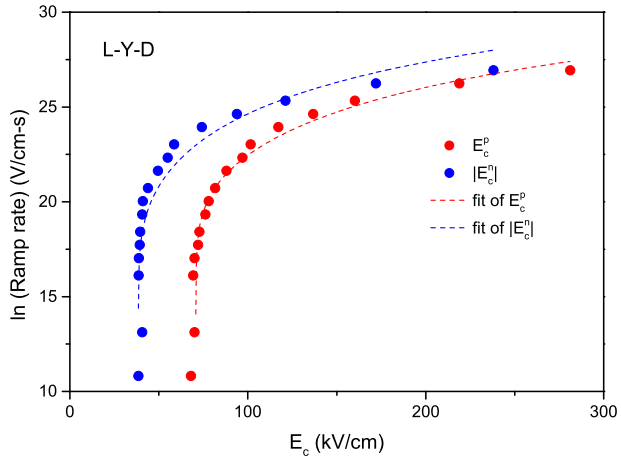

Figure 5.8: Plot of E_c at various frequencies according to L-Y-D model.

5.1.4 P-K Model

Pulvari and Kuebler (1958) assumed that domains nucleated on the cathode or anode and propagated through the thickness. In P-K model both nucleation and domain wall motion are considered important. E_c and ramp rate are related as follows:

$$ln\left(\frac{\mathrm{d}E(t)}{\mathrm{d}t}\right) = ln\left(\kappa E_c^2\right) - \frac{\alpha}{E_c} + \delta \tag{5.6}$$

where κ is proportional to the displacement mobility and is dependent on temperature and film thickness. Fitting result is shown in Figure 5.9.

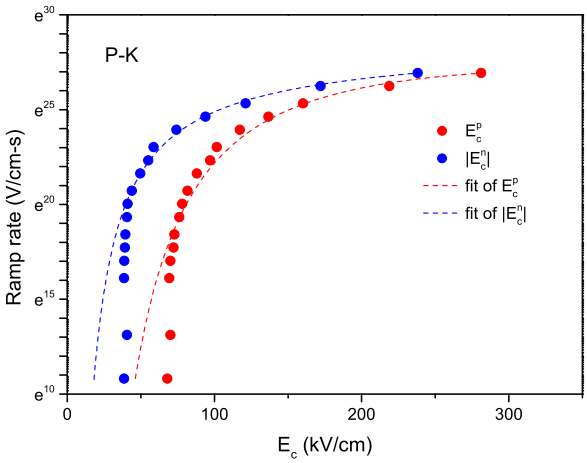

Figure 5.9: Plot of E_c at various frequencies according to P-K model

Table 5.1: Fitting quality and suitable capacitor sizes of four different models.

Model		I-O	D-C	L-Y-D	P-K
Limiting factor		DW	nucleation	DW	DW & nucleation
Fitted range	Low ($\leq 50\ Hz$)			$\surd$	
	Middle ($50 \sim 250k\ Hz$)		$\surd$	$\surd$	$\surd$
Suitable for (size of capacitor)		N/A	N/A	large	large and small

Between 50 Hz and 400 kHz P-K model was well fitted to the data but was not successfully fitted to the low frequency range.

5.1.5 Conclusion

E_c was found to be frequency dependent and it can be several times bigger at high frequency. P_r was stable at different frequencies as long as applied field exceeds E_c. After applying four models to our data, which have different emphases on nucleation or domain wall movement, the fitting results showed L-Y-D have the best fit in all frequency range measured and was successful in predicting the minimum limit of E_c at low frequency. However, sub–50 Hz is not useful for memory devices. D-C, L-Y-D and P-K model all exhibited good fit to the data from 50 Hz to 400 kHz. I-O model failed to fit the data. D-C model clearly pointed out the limiting frequency f_0. Table 5.1 presents the features of 4 models and the fitting quality of each model.

As the capacitor size decreases below a critical area, the limiting factor shifts to nucleation as there are less nucleation sites. P-K model is more applicable for small capacitors comparing to L-Y-D model. Jung *et al.*'s work (2005) showed that P-K model fitted better than L-Y-D model (measured in the range between 1 kHz and 1 MHz). Because in L-Y-D model, nucleation is considered to be unimportant.

Scott (2006) estimated the critical lateral area to be $100\,\mu m^2$ for KNO_3 and $1\,\mu m^2$ for PZT.

Prasertchoung's work (2006) on polycrystalline PZT capacitors from 225 μm^2 to 0.19 μm^2 showed that with a quasi-square PUND drive pulse, P_r of capacitors with different sizes exhibited similar value ($\sim 30\ \mu C/cm^2$). Switching time was in the range of ns for all capacitors and smaller capacitors exhibited faster switch, but of the same order.[1] Activation field α dropped dramatically as the size of capacitor dropped.

5.2 Different Contributions in P-E Loop

PUND measurement separates the switching part (I_{P-U} and I_{N-D}) from the non-switching part (I_U and I_D). In this section we will investigate these two parts quantitatively through the comparison of I-V measurement with switching part and the comparison of C-V measurement with non-switching part. This allows us to further understand the shape of a P-E loop.

5.2.1 Switching Part

In the previous chapter, the leakage currents were recorded in the condition that the capacitor had experienced applied field of the same sign (positive or negative). Thus all the domains had already been switched and no switching charges flowed during the I-V leakage measurement. If a reversal field ($> E_c$) is applied to the capacitor prior to the I-V measurement, a small peak will be observed, as shown in Figure 5.10. The two ramps are due to the domain switching movement.

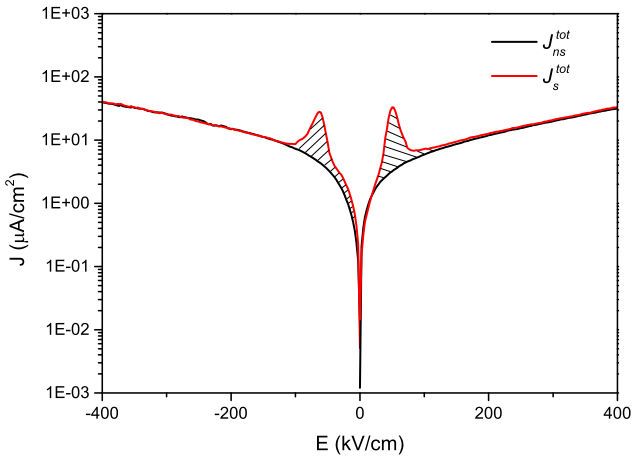

Figure 5.10: Leakage current of normal I-V measurement and and I-V measurement with domain switching.

The current with switching, J_s^{tot}, consists of three parts: switching current, J_s; leakage current, J_l; and dielectric current, J_d, which is due to the dielectric polarization of the capacitor. These three components are illustrated in Figure 5.11.

[1] He stated that the obtained switching time might be of the set-up, not of the PZT.

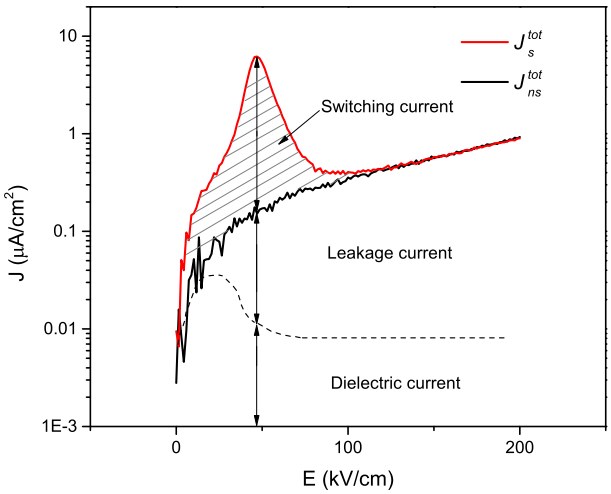

Figure 5.11: Schematic of three compositions of J_s^{tot}.

The switching current J_s can be obtained by performing twice I-V measurement with domain pre-switched to the same and opposite direction.

$$J_s = J_s^{tot} - J_{ns}^{tot} \tag{5.7}$$

$J_{ns}^{tot} = J_l + J_d$. Compared to leakage current J_l, non-switching current J_d is usually very small and omitted, thus $J_{ns}^{tot} \approx J_l$. J_d can be roughly estimated by performing an I-V measurement (without switching) with increasing voltage and another with decreasing voltage. Since leakage current J_l is usually much bigger than J_d, it is difficult to obtain J_d precisely.

Since J_s from I-V measurement and J_{P-U} and J_{N-D} from PUND measurement are both due to the domain switching behavior, the amount of polarization from both measurement should be the same. Figure 5.12 depicts these two kinds of current. First we notice that, the amount of J_{P-U} (or J_{N-D}) is about 4 orders of magnitude larger than that of J_s. The great difference in quantity is because that the field was applied in different ways in these two measurements. In dynamic PUND measurement, field was applied with a frequency of 250 Hz. In static I-V measurement, the equivalent frequency was only 0.0125 Hz. Secondly, it is found that E_c from I-V measurement was smaller than that from PUND measurement. This is because domain switching was relatively slow comparing to the field varying rate in dynamic PUND measurement. But in the static I-V measurement, at each voltage, the long step period allows more domains to be switched. It is also clear that the peaks from both measurements have the same shape. The peak in positive field are wider and has a smaller maximum value in both measurements. Lastly, as the capacitor has a asymmetric structure Pt/PZT/SRO, $|E_c^p| > |E_c^n|$ is observed in both cases.

By integrating J_s, a P-E loop is obtained, as shown in Figure 5.13 along with PUND loop and PN loop. (Since the J_l and J_d is very small in Figure 5.12, $J_s \approx J_s^{tot}$). This P-E loop have almost the same

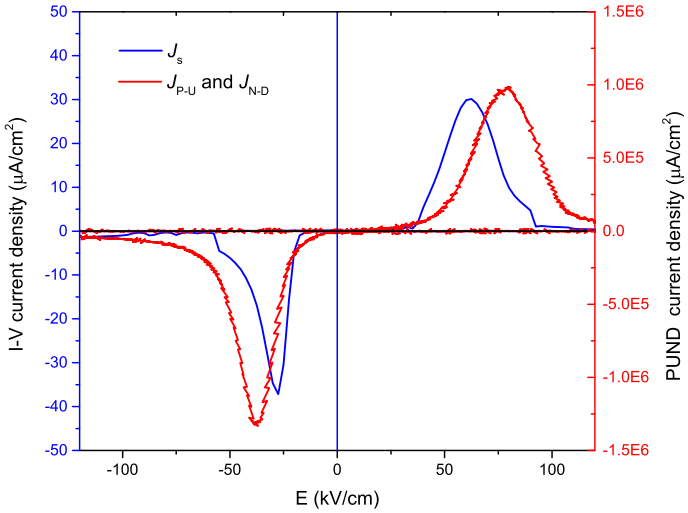

Figure 5.12: Comparison of I-V leakage current and switching current J_s in PUND measurement. Data from 200-nm-thick sol-gel-derived PZT capacitor with Pt top electrode.

shape as PUND loop except that E_c from this loop are slightly smaller than those of PUND loop, due to the different frequencies in two measurements.

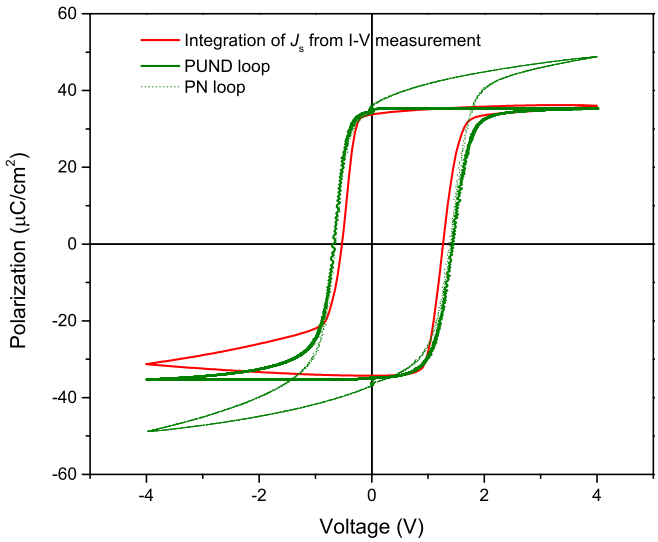

Figure 5.13: Comparison of integration of J_s in I-V measurement with PUND loop and PN loop. Data from 200-nm-thick sol-gel-derived PZT capacitor with Pt top electrode.

As we can see from Figure 5.13, for the P-E loop, integrated of J_s, when field passes E_c, polarization is almost stable. This means that the capacitor is well saturated at about $2E_c$ and higher field does not cause noticeable domain switching. This means that the difference between this P-E loop and PN loop is not due to the domain switching. (The maximum value in PN loop, $P^\star$, is usually called saturation polarization, which is usually not correct.) In this case, J_l is almost zero, and the part $(P^\star - P_r)$ is mainly due to the dielectric polarization of the capacitor.

Theoretically, P_r from the P-E loop, integrated of J_s, should be slightly larger than that of

PUND loop. Because when the applied field passes E_c by a margin, all switchable domains align their directions with the long lasting field. Then the ferroelectric capacitor is well saturated in this condition. In Figure 5.13, we notice that the P_r from the P-E loop, integrated of J_s, actually is slightly smaller than that of PUND loop. This is due to the I-V measurement. The realistic current response to each voltage step is non-linear, as shown in Figure 5.14. However the measured current is constant under each voltage step. Even we set delay time $t_d = 0$, there might be a small amount of charges which could not be measured at the beginning of each step due to limit of response speed.

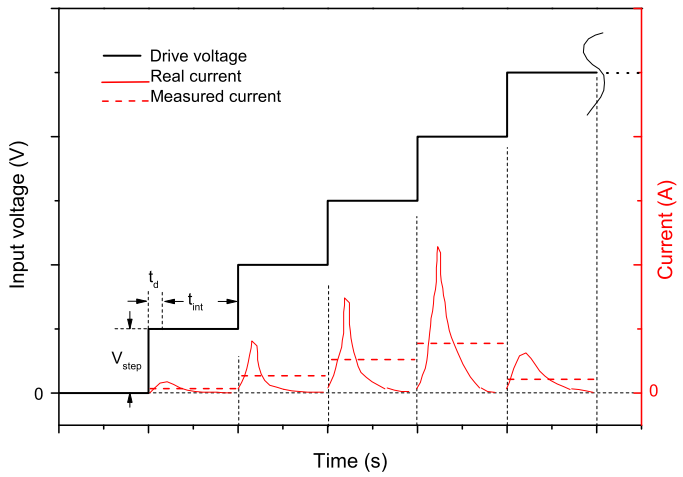

Figure 5.14: Schematic of I-V measurement with switching. t_d was set to be 0 if not stated.

I-V leakage current measurement at various temperatures was also performed for the same capacitor, as shown in Figure 5.15. E_c slightly dropped with temperature, which was in consistent with the PUND measurement results at various temperatures (see Figure 5.19).

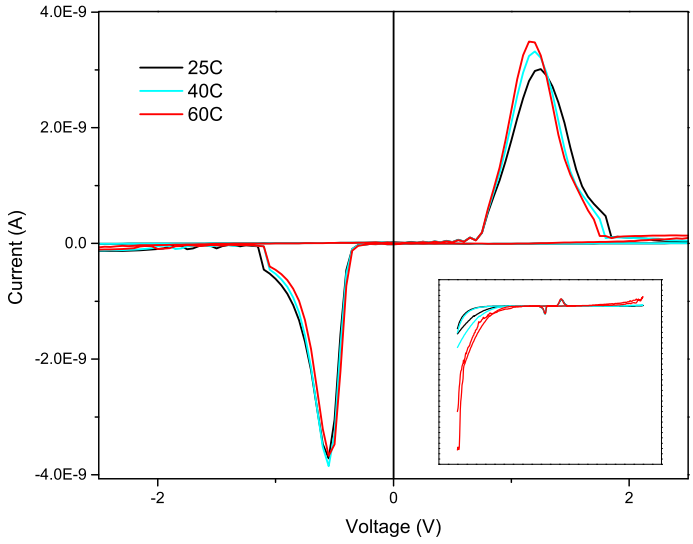

Figure 5.15: J_s^{tot} at various temperatures. Data from 200-nm-thick sol-gel-derived PZT capacitor with Pt top electrode.

The switching peaks in I-V measurement are rarely reported (we have only found the the reports

from Ryu (1999) and Evans (2011)), because a pre-switch field is usually applied to the capacitor when measuring leakage current, as we did in chapter 4. The reason also can be the large leakage (*e.g.*, 40.5-nm-thick sputtered PZT capacitor), which will mask the small switching current (only several nA for a $100 \times 100\,\mu m^2$ capacitor). And even a high quality capacitor can exhibit relatively high leakage current.[2] It may also be due to the measurement set-ups. Peaks will disappear when delay time t_d is big enough (0.5 s for our sol-gel-derived capacitors) as all domain switching behaviors complete during this period.

5.2.2 Non-Switching Part

As stated in the previous subsection, PUND loop is the manifestation of domain switching exclusively and the polarization between P_r and $P^\star$ (maximum polarization in PN loop) is due to dielectric polarization (not due to paraelectric polarization). We use (PN-PUND) loop to evaluate this part, which is obtained by sutracting PUND loop from PN loop. C-V measurement meters the capacitance of an insulator. Now we are going to compare the measured result quantitatively from these two methods since both of them originate from dielectric polarization.

In Figure 5.16, P-E curves of three types of dielectrics are plotted with correspondent C-E curves. For a simple dielectric, polarization is a linear function of external field with a constant capacitance, as shown is Figure 5.16 (a). For a paraelectric, at lower electric field it exhibits a higher dP/dE slope, due to the formation of non-permanent dipoles, as shown in Figure 5.16 (b); at higher electric field, it shows only linear dielectric effect. Figure 5.16 (c) shows the P-E loop and C-E curve of a ferroelectric. A ferroelectric capacitor can be deemed as a paraelectric with memory.

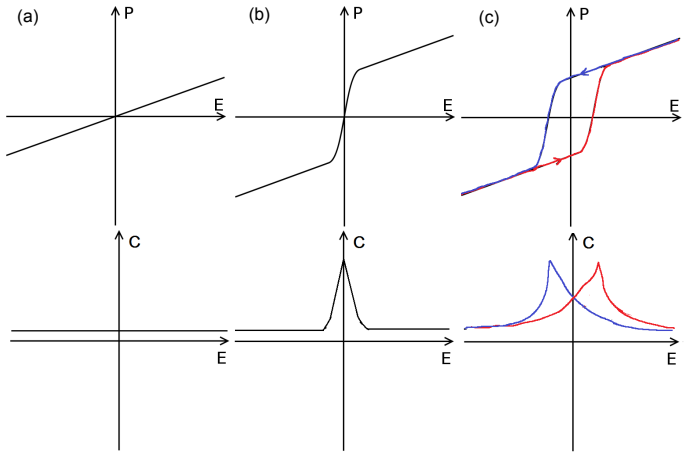

Figure 5.16: P-E curve and corresponding C-V curve of three different types of capacitors. (a) simple capacitor; (b) paraelectric capacitor; (c) ferroelectric capacitor.

Polarization P due to dielectric effect can be extracted from C-V measurement by equation:

$$P = \frac{\int C(V)\mathrm{d}V}{A} \tag{5.8}$$

[2] Pintilie (2011), Vrejoiu *et al.* (2006) demonstrated that a high quality epitaxial PZT showed a larger leakage current comparing to defective PZT. They stated that the reason can be the higher mobility in high quality PZT than in the defective film.

where A is the area of the capacitor.

Figure 5.17 depicts the P-E loop, integrated of capacitance and PUND loop, PN loop. The difference between PN loop and PUND loop, (PN-PUND) loop is also plotted here by integrating I_U and I_D. P-E loop, integrated of capacitance resembles the (PN-PUND) loop but the slope in (PN-PUND) loop is higher in low field range.

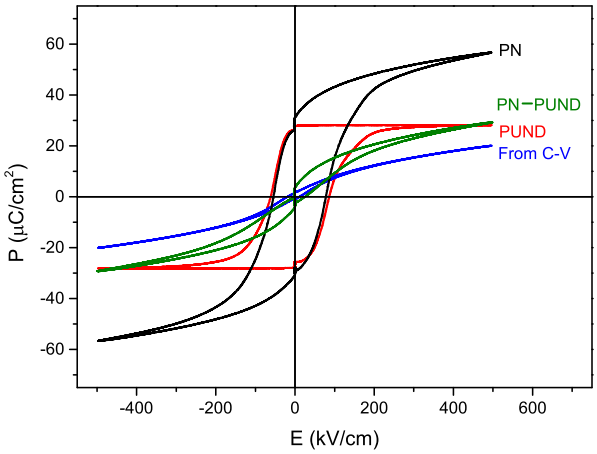

Figure 5.17: P-E loop, extracted from C-V curve, compared with PUND loop, PN loop and (PN-PUND) loop. Data from 67-nm-thick sol-gel-derived PZT capacitor with SRO top electrode.

I_U and I_D can also be converted to capacitance by equation:

$$C = I\frac{\mathrm{d}t}{\mathrm{d}V} \tag{5.9}$$

Figure 5.18 shows this C-V curve, extracted from I_U and I_D and C-V curve measured at three different frequencies. The four curves shared the same linear capacitance C_l at high voltage. If we compare the capacitance at $V = 0$, the value from the curve, extracted from I_U and I_D (no switching happens), is higher than that from the three C-V curves. The difference could arise from: a) additional leakage current J_l in I_U and I_D (usually insignificant compared to J_s in a high quality capacitor,[3] but can be comparable to J_d; b) different measurement methods used in the two measurement. In static C-V measurement, a DC bias varied discontinuously with a constant step and a small AC agitation of certain voltage was applied to the capacitor. While in dynamic PUND measurement, I_U and I_D were transient currents acquired by varying the applied voltage continuously without domain switching.

[3]For all the capacitors in this thesis, leakage current was quite small in PUND measurement at $E_{max} < 1000\,kV/cm$, except 40.5-nm-thick sputtered capacitor and 33-nm-thick sol-gel-derived capacitor.

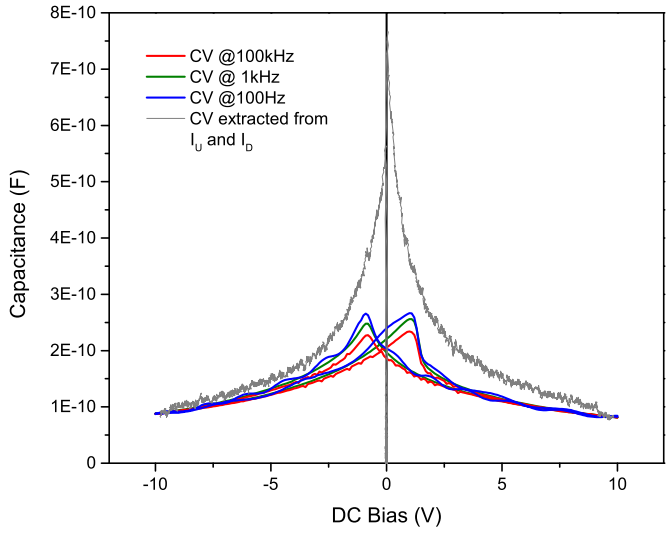

Figure 5.18: C-V curve extracted from J_P and J_U in PUND measurement, compared with C-V curves measured at three frequencies. Data from 200-nm-thick sol-gel-derived PZT capacitor with Pt top electrode.

5.2.3 Conclusion

A usually seen P-E loop (PN loop here) has been separated into three parts: PUND part which is the integration of switching charges; (PN-PUND) part, which is due to the dielectric polarization; and contributions from leakage. For a well insulated capacitor, the leakage contribution is very small. For a slightly leaky capacitor, $P^\star$ is apparently bigger than that of its insulated equivalent.

By comparing I-V and C-V measurement results with PUND measurement results quantitatively, we have found that two bumps in I-V measurement are due to domain switching behavior and the difference between PN loop and PUND loop is due to the dielectric polarization of the capacitor.

The peak shape and location in I-V curve and C-V curve are close connected to PUND loop shape. For example, wider peak in I-V curve or in C-V curve (see the curve of 40.5-nm-thick capacitor in Figure 4.24) means field need to pass E_c by a margin to switch all the domains. Similarly, PUND loop shows a less square-like shape (dP/dE is smaller) for this type of capacitor (see the loop of 40.5-nm-thick capacitor in Figure 4.29).

By combining P-E loop extracted from J_s in I-V measurement and P-E extracted from capacitance, we can obtain a similar loop to PN loop. The main difference is that E_c is smaller due to the reasons mentioned before. Pintilie *et al.* (2006) showed that E_c measured by static method[4] is smaller than that in normal dynamic mode and it was compatible with the E_c in I-V and C-V results.

[4]A certain field is appled to the capacitor after a poling precedure. The amount of polarization is calculated by integrating the current. Procedure is repeated with varying the field. A P-E loop can be obtained by connecting the polarization at each field. Detailed procedure in Pintilie *et al.* (2012).

5.3 Electrical Characterization at Various Temperatures

PUND measurement has also been carried out at low temperature under vacuum circumstance and on a heated substrate holder in air. Figure 5.19 shows PUND loops of 200-nm-thick sol-gel-derived PZT capacitor with Pt top electrode measured at various temperatures. P_r decreased with temperature due to pyroelectric effect. And E_c also decreased with temperature. Pyroelectric coefficient was calculated to be as large as $-50\,nC/cm^2K^{-1}$, equivalent to the reported value $-48\,nC/cm^2K^{-1}$ (Xiao *et al.* 2008) and bigger than $-18\,nC/cm^2K^{-1}$ of PZT(30/70), reported by Zhang and Whatmore (2001).

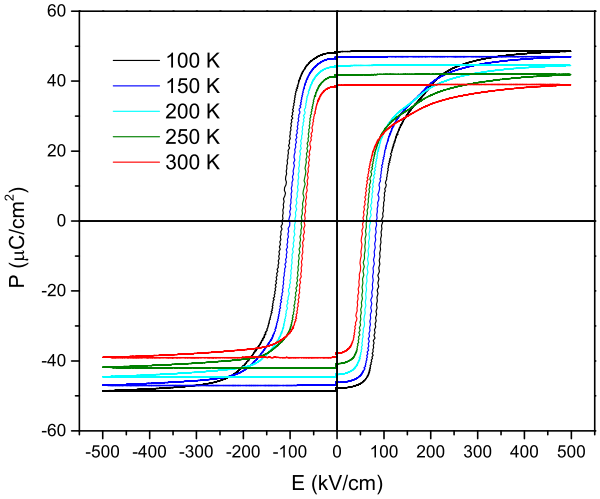

Figure 5.19: PUND loops measured at various temperatures. Data from 200-nm-thick sol-gel derived PZT capacitor with Pt top electrode.

The transition of PZT from cubic phase to tetragonal or rhombohedral phase is either of first order or of second order (see Landau-Ginzburg-Devonshire theory in chapter 1), depending on the composition of PZT (see Figure 5.20). According to Haun *et al.* (1989), PZT(52/48) transition is of second order.

From Equation (1.3) we know that for a second order transition, remnant polarization P_r can be expressed by:

$$P_r^2 = \frac{\gamma(T_c - T)}{g_4} = \frac{T_c - T}{g_4 \varepsilon_0 C_{CW}} \tag{5.10}$$

where g_4 is Landau-Ginzburg-Devonshire coefficient, C_{CW} is Curie-Weiss constant. Figure 5.21 plots the P_r^2 vs. T. From the linear fitting result, the x-intercept indicates that $T_c \approx 385\,°C$. This is consistent with the phase diagram in Figure 1.7 and in agreement with our XRD measurement from room temperature to 800 °C on a sol-gel-derived PZT film (not provided in this dissertation).

C-V measurement has also been carried out on the same sample from 100 K to 473 K, plotted in Figure 5.22. As temperature increased, maximum of ε_r' increased and the linear part did not change. E_c decreased with temperature, which was consistent with the PUND results in Figure 5.19.

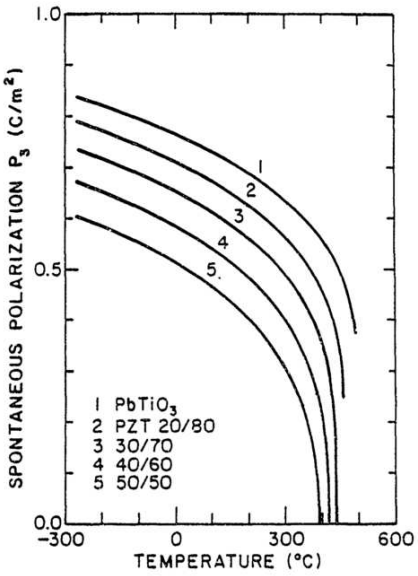

Figure 5.20: Polarization as a function of temperature for PZT of various compositions. $PbTiO_3$ and PZT(20/80) are of first order transition while PZT(30/70), PZT(40/60) and PZT(50/50) are of second order transition (Haun *et al.* 1989).

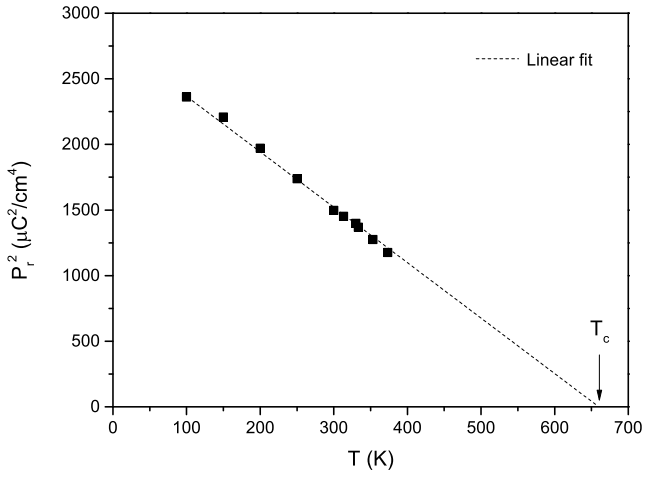

Figure 5.21: P_r^2 as a function of temperature. Data from 200-nm-thick sol-gel derived PZT capacitor with Pt top electrode.

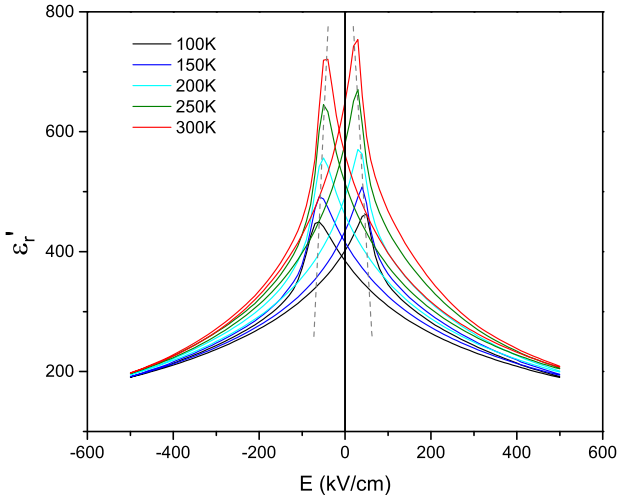

Figure 5.22: ε'_r as a function of temperature. Data from 200-nm-thick sol-gel derived PZT capacitor with Pt top electrode.

Susceptibility χ of the ferroelectric satisfies the Curie-Weiss law, as described by (Zubko *et al.* 2006):

$$\frac{1}{\varepsilon'_r \varepsilon_0} \approx \frac{1}{\chi} = \frac{2(T_c - T)}{\varepsilon_0 C_{CW}} \tag{5.11}$$

The reciprocals of ε'_r (at $E = 0$) extracted from Figure 5.22 are plotted in Figure 5.23. By fitting the data, the Curie-Weiss constant C_{CW} was extracted to be $4.56 \times 10^5\, K^{-1}$ and $4.20 \times 10^5\, K^{-1}$ for the results measured at low temperature and at high temperature, respectively, which is similar to $4.44 \times 10^5\, K^{-1}$, reported by Zubko *et al.* (2006).

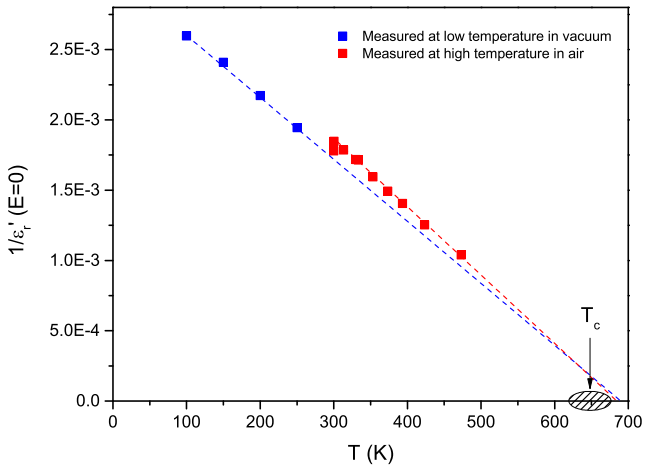

Figure 5.23: Reciprocals of ε'_r as a function of temperature. Data from 200-nm-thick sol-gel derived PZT capacitor with Pt top electrode. Low temperature measurement was carried out in vacuum and high temperature measurement was carried out in air.

As temperature approaches to T_c, ε'_r will be several times bigger than that at room temperature (Haun *et al.* 1989), but its value will not become several orders of magnitude larger. Thus in Figure 5.23, T_c should be on the left proximity to the x-intercept from the linear fitting. The value of this extracted T_c is consistent with T_c extracted from PUND measurement in Figure 5.21.

5.4 Relaxation

As ferroelectric capacitor is mainly used in memories, relaxation and retention are important parameters since a memory should have a high stability. Stored information in the capacitor should remain for enough long period without obvious decay.

In the PUND measurement, the period between the opposite drive voltages is t_r (see Figure 2.13). In chapter 4, $t_r = 1\,ms$ for all the measurements. t_r has been varied from 1 ms to 60 s to investigate the relaxation of the capacitor (the period between pulse "P" and "U" and between "N" and "D", t_{int}, was kept as 1 ms, see Figure 2.13). Figure 5.24 shows the remnant polarization P_r as a function of t_r. As t_r increased from 1 ms to 100 ms, P_r dropped from 26 to 20 $\mu C/cm^2$ and after ~ 5 s P_r was stable at around 18 $\mu C/cm^2$, which was 69.2 % of P_r at $t_r = 1$ ms. This suggested that relaxation did happen in a short period after the domain switching had completed. The remained polarization was still big enough to be distinguished from different states.

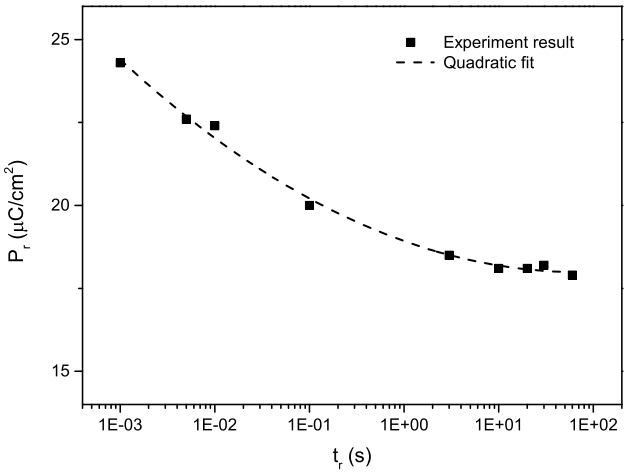

Figure 5.24: Relaxation of polarized domains. Data from 100-nm-thick sol-gel-derived PZT with SRO top electrode. This 100-nm-thick capacitor experienced twice annealing in furnace for 3 h for the crystallizations of PZT and top electrode, which is not the same 100-nm-thick capacitor mentioned in previous chapters.

It should be noted that the measurement was carried out on a sol-gel-derived capacitor, which experienced 3 h annealing for both the crystallization of PZT film and the crystallization of top electrode. According to the results in chapter 4, long duration annealing in furnace could damage both the crystalline structure of both bottom SRO layer and PZT film. Thus the relaxation quality of other capacitors discussed before should be better than this one.

Retention is the ability of a ferroelectric capacitor to retain the polarization sign and the magnitude originally written. It is a measure of self-life, as opposed to fatigue, which measures loss of polarization after repetitive switching. Retention is an even more crucial issue, concerning the reliability of the ferroelectric capacitor. For practical applications, the retention time must be longer than 10 years (Ishiwara *et al.* 2010).

Retention losses occur when the back-switching happens from the interface and penetrates through the thickness. Gruverman and Tanaka (2001) stated that the presence of a polarization-independent built-in bias at the interface of ferroelectric and bottom electrode triggered the back-switching of domains. It is found that at elevated temperatures, retention losses are more obvious Shimada *et al.* (1997).

Since retention measurement is greatly time-consuming, due to limitations we have not carried out this measurement on the PZT capacitors.

5.5 Imprint

Imprint describes the preference of one polarization state over the other. Imprint leads to a shift of P-E loop on the field axis, and strong imprint can cause a loss of P_r. Imprint can lead to a read/write failure of the capacitor.

For the explanation of imprint in ferroelectric capacitors, there are mainly two types of mechanism: defect dipole alignment model (Arlt and Neumann 1988); interface screening (Grossmann *et al.* 2002). In the former model, an internal bias is assumed to exist due to the gradual alignment of defect dipoles consisting of acceptor ions and oxygen vacancies. When the domains are switched by an external field, these aligned defect dipoles remain in their positions, causing a shift of P-E loop. In the later model, a thin layer with suppressed ferroelectric properties is assumed to exist in the interface between the ferroelectric and electrodes (depicted in Figure 5.25). An electric field E_{if} is formed inside the interface layer. E_{if} is responsible for the charge separation within the interface which is due to Frenkel-Poole emission (Ishiwara *et al.* 2010). Grossmann *et al.*'s work (2002) showed great agreement between experiment and simulation.

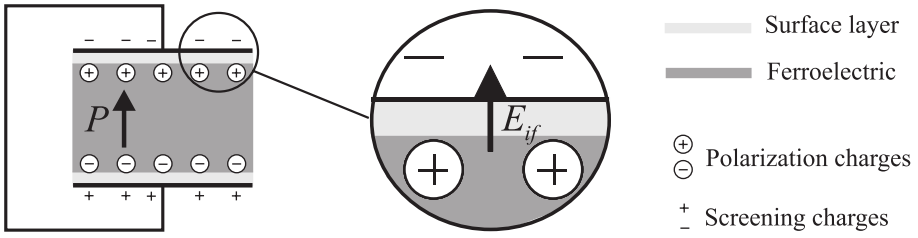

Figure 5.25: Interface screening model for imprint. (a) A sketch of a ferroelectric capacitor with thin interface layers; (b) An enlargement of the interfacial region, showing the driving force of E_{if} of imprint (Ishiwara *et al.* 2010).

5.5.1 Influence of Top Electrode

In chapter 4, the P-E loops of sputtered and sol-gel-derived PZT capacitors with three different top electrodes (SRO, Pt, ITO) have been presented (see Figures 4.29, 4.31 and 4.33). Generally, capacitors with SRO top electrode showed symmetric PUND loop; Sputtered PZT capacitors with Pt top electrode showed positive asymmetric PUND loops ($|E_c^p| > |E_c^n|$) while sol-gel-derived PZT capacitors with Pt top electrode showed negative asymmetric PUND loops ($|E_c^p| < |E_c^n|$); The symmetricity of sputtered PZT capacitors with ITO top electrode were not obvious given their much larger E_c. The defect dipole alignment model is not consistent with these results because the model is based on the bulk properties of the ferroelectric. According to the interface screening model, it can be assumed that E_{if} of the Pt/PZT interface is different from that of the SRO/PZT interface, thus causing a shift in P-E loops of capacitors with Pt top electrode. The reason of the opposite shift of P-E loops in Pt/PZT/SRO capacitors grown by different routes is not clear.

It should be noted that for the capacitors with symmetric stack structure, SRO/PZT/SRO, the SRO above and beneath are not of the same quality. The bottom SRO was deposited at around 620 °C on STO substrate. It was crystalline without post annealing. The top SRO was deposited at room temperature on relatively rougher PZT layer. An additional post annealing was required to crystallize the amorphous top SRO and XRD result showed the amount of crystalline SRO on top was much less compared to that of the bottom SRO.

Capacitors with ITO top electrode always showed a much bigger E_c (see Figure 4.31), which was unfavorable. It should be noted that ITO was annealed at 250 °C in N_2 during 1 *min* by RTA. SRO and Pt top electrodes were annealed in O_2 at 650 °C for 1 *min* by RTA. This difference may also cause the broadening of its P-E loop.

5.5.2 Influence of Post Annealing

To verify the influence of post annealing, two capacitors, one with SRO top electrode and another with Pt top electrode, part of both experienced the RTA at 650 °C in O_2 and another part of both experienced the RTA, which was designed for ITO top electrode. The PUND results and ε_r' are shown in Figure 5.26.

For capacitors, both with SRO top electrode and with Pt top electrode, the annealing at 250 °C in N_2 broadened the PUND loop. After both annealing procedures, P_r were similar and the maximum value of ε_r' was smaller in 250 °C N_2 RTA, which was similar to the reduced ε_r' of capacitors with ITO top electrode (see Figure 4.26).

We noticed that the the different annealing procedure showed different effect in imprint. For capacitors with SRO top electrode, P-E loop was always symmetric after 2nd annealing in O_2. But when the annealing was performed in N_2, the imprint was so great that the domains strongly preferred to switch "down" when external field was removed. A deformed PUND loop was obtained (blue dash in Figure 5.26). By applying a positive offset voltage (mean value of the two coercive voltages) to the whole

PUND pulse trains, a proper PUND loop was obtained.

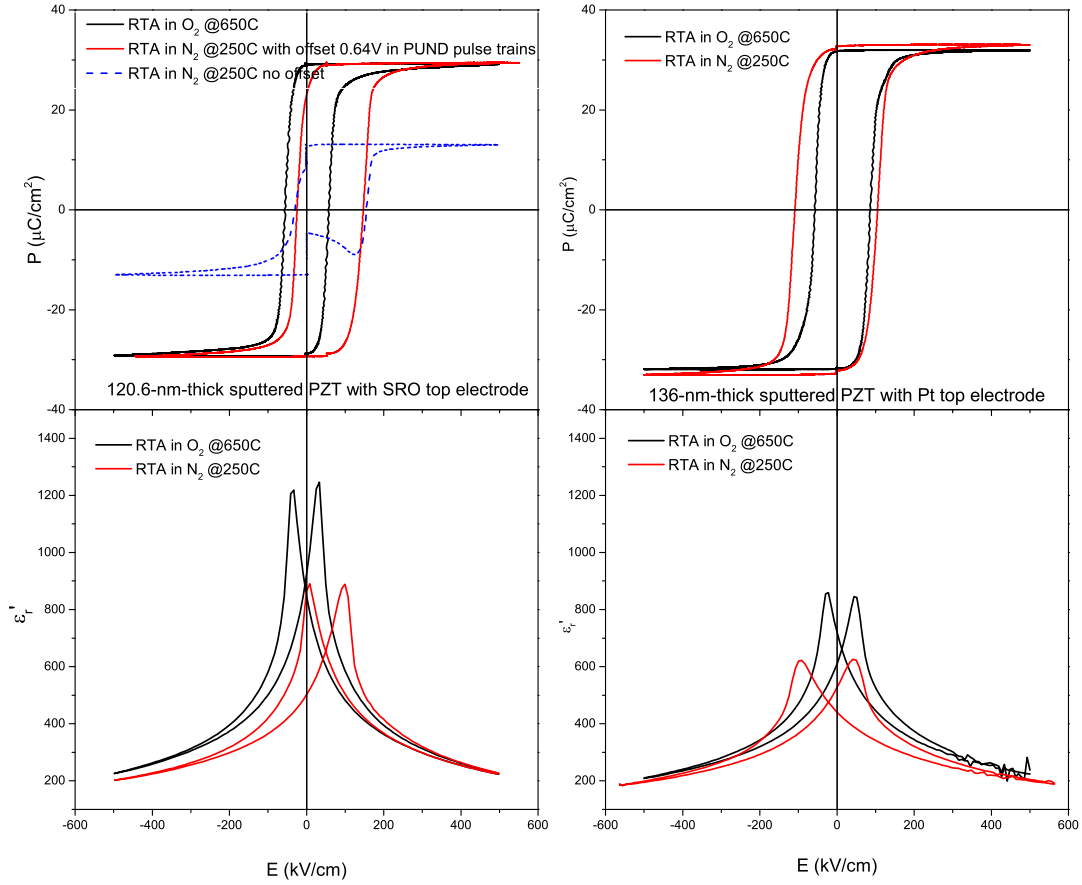

Figure 5.26: PUND loop and ε'_r of puttered capacitors experienced different 2nd RTA.

To further study the impact of annealing, we fabricated a capacitor with SRO top electrode without performing RTA to top electrode. It is found that the PUND loop showed a big positive asymmetricity and $(|E_c^p| + |E_c^n|)/2$ was around 200 kV/cm which was about twice of usually observed value. The maximum value of ε'_r was found to be greatly reduced ($\sim$ 35% less) without performing second annealing. (The result was not provided here.)

Since top electrodes were deposited at room temperature by sputtering and they were amorphous before RTA, it can be assumed that after the RTA the interface between the top electrode and PZT film was changed thus the field formed inside the interface, E_{if}, also changed, shifting the P-E loops.

According to these results, the much bigger E_c and reduced ε'_r observed in capacitors with ITO top electrode might due to the 2nd RTA instead of the use of ITO.

5.5.3 Influence of Bottom Electrode Thickness

The thickness of bottom electrode SRO varied form 25 nm to 85 nm for all the capacitors presented in chapter 4, and all SRO/PZT/SRO capacitors exhibited symmetric P-E loops without obvious imprint.

The thickness of top electrode was much thicker ($\sim$ 150 nm) to sustain the microprobe while carrying out electrical measurements. Since thinner bottom electrode can reduce the roughness of its surface and are more strained on substrate, high quality epitaxial growth for ferroelectric layer can be easier on a thinner bottom electrode.

A 200-nm-thick sol-gel-derived capacitor with bottom electrode of only 18.9 nm was fabricated to compare the influence of bottom electrode thickness, when it dropped to less than 20 nm. Figure 5.27 shows the PUND loops of this sample and the PUND loops of another 200-nm-thick sol-gel-derived capacitor with 85-nm-thick bottom electrode (the same sample mentioned in chapter 4 and in previous sections of this chapter) for comparison. The capacitor with 18.9-nm-thick bottom electrode with SRO top electrode exhibited an obvious shift of PUND loop. ε_r' of both capacitors were found to be similar (not provided here).

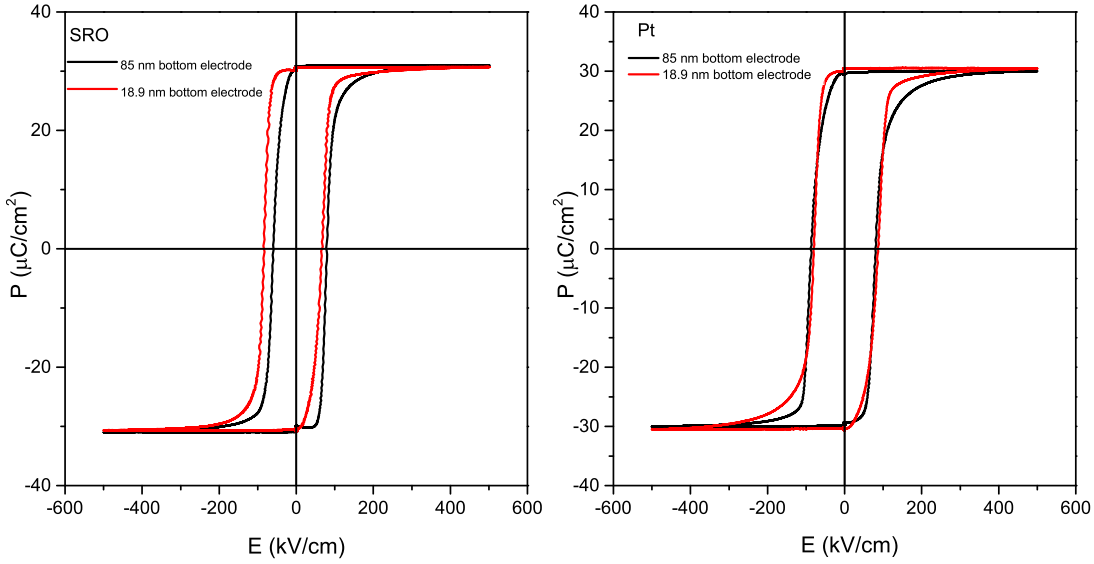

Figure 5.27: PUND loops of a 200-nm-thick capacitor with 85-nm-thick bottom SRO layer and of another 200-nm-thick capacitor with 18.9-nm-thick bottom SRO layer. Left shows the PUND loops of these two capacitors with SRO top electrode. Right shows the PUND loops of these two capacitors with Pt top electrode.

Figure 5.28 shows the P_r and E_c extracted from PUND measurements at various voltages of these two capacitors with different thick bottom electrodes. P_r from both sample (both with SRO top electrode and Pt top electrode) were found to be identical. But the result of E_c showed that the thickness of bottom electrode did have an impact on the imprint quality of the capacitor. For the capacitor with 18.9-nm-thick bottom SRO layer with Pt top electrode, the imprint was very small, which was different from the result we observed previously from capacitors with relatively thicker bottom electrodes.

According to these results, we found that SRO/PZT/SRO capacitor exhibited no imprint when bottom SRO electrode exceeded 25 nm; and when bottom SRO was less than 18.9 nm, SRO/PZT/SRO capacitor showed imprint but Pt/PZT/SRO showed no imprint. Capacitor with no imprint of both symmetric and asymmetric stack structure can be fabricated by varying the bottom electrode thickness.

[5]This sample is the same shown in Figure 4.34.

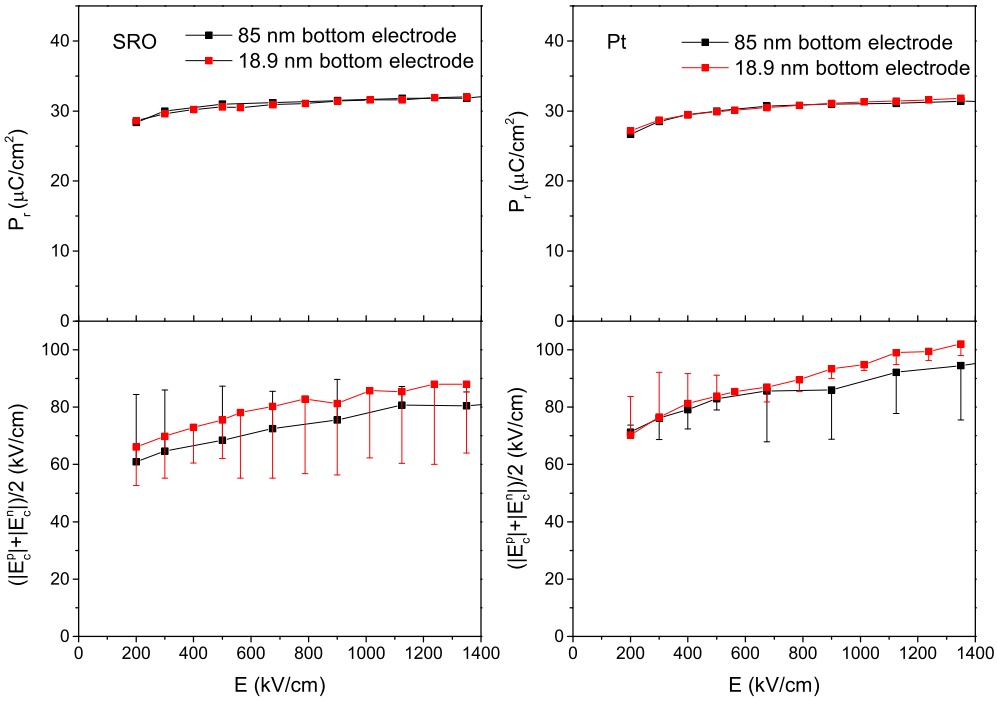

Figure 5.28: P_r and E_c of PUND loops from two 200-nm-thick[5] capacitor with bottom electrode of different thickness, measured at various fields. Left shows the results of these two capacitors with SRO top electrode. Right shows the results of these two capacitors with Pt top electrode.

Further study is needed to find out the minimum bottom electrode thickness at which it can both acting as a good electrode and prevent diffusion.

5.6 Summary

In this chapter, frequency dependence of E_c was investigated and it is found that higher frequency increased E_c but did not change P_r. Four models have been applied to the experimental results: D-C, L-Y-D and P-K model all showed a good fit in the range from 50 Hz to 250 kHz and L-Y-D model (only considering domain wall movements) successfully predicted the minimum limit of E_c at frequencies below 50 Hz.

A typical P-E loop was decomposed into two parts (for a good insulated capacitor, the contribution from leakage is negligible): ferroelectric polarization and dielectric polarization, by comparing I-V and C-V with PUND results quantitatively. P_r^2 was found to linearly decrease with temperature and maximum of ε_r' was found to increase with temperature, which were consistent with literature. Imprint property of the capacitors have been investigated through three aspects: top electrode, post annealing and the thickness of bottom electrode. They all showed influences on imprint.

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Conclusion and Perspectives

In this thesis, PZT(52/48) capacitors grown by two methods, sputtering and sol-gel, were studied. For each method, the thickness of capacitors varied from sub–50 nm to ~ 200 nm to investigate the thickness effect and find out the thinnest workable PZT capacitor. In order to investigate the influence of top electrode, three different conductive materials (SRO, Pt and ITO) were employed.

Initial work was on the optimization of sputtering SRO as bottom electrode. By varying deposition conditions, a set of parameters were obtained for growing smooth (RMS < 1.0 nm) SRO film with high crystallinity and low mosaicity ($\sim 0.1°$). In order to grow epitaxial SRO layer by layer on vicinal STO, which offers flat interface with subsequent PZT film and reduces defect densities, we further lowered the plasma voltage and introduced an interval in the middle of sputtering process. In this condition, SRO layer of more than 30 nm with terraces of single unit cell in height was achieved. In the next growth stage, by optimizing deposition conditions, epitaxial PZT films were achieved by both methods. Smooth surface (RMS < 0.8 nm) were obtained for all films and the mosaicity of sputtered PZT films were about 1.1°, which was about 25% bigger than that of sol-gel-derived films. By lowering the plasma voltage and posing an interval into the middle of sputtering process, a 190-nm-thick PZT film (RMS = 0.38) even exhibited terraces of single unit cell in height.

After the fabrication process, electrical properties of these capacitors were investigated through current-voltage (I-V), capacitance-voltage (C-V) and hysteresis loop measurements (PUND) and piezoresponse force microscopy (PFM). For capacitors with a PZT layer of $100 \sim 200$ nm, which was well insulated, the amount of leakage did not show thickness dependence. By fitting various charge transport models to the leakage data, we found that: at low field range, leakage was due to ohmic conduction for both types of capacitors; at higher field range, the leakage mechanisms were different for the capacitors made by different routes. Due to the complexity of leakage current in ferroelectrics, two mechanisms fitted this field range for both types of capacitors. Top electrode seemed to have very small influence on leakage current. The thickness of dead layer for all capacitors was found to be less than 3 nm. Maximum relative permittivity ε'_r of all capacitors were between 600 and 1300, which were compatible with previous reports.

P_r of capacitors with a thickness of $100 \sim 200$ nm was between 30 and 40 $\mu C/cm^2$, which were in great agreement with reported results. Thicker capacitors showed better saturation quality than thinner ones. For PZT with a thickness of around 200 nm, P_r exhibited a high saturation quality for both types of capacitors. PFM results revealed that 200-nm-thick sol-gel-derived PZT showed better piezoelectricity

and longer retention than thinner sol-gel-derived PZT films. It was found that E_c was highly dependent on frequency. Three different models were successfully fitted to E_c at different frequencies. Imprint property was found to be dependent on three aspects: top electrode (or stack structure asymmetricity); post annealing procedure; and bottom electrode thickness.

To summarize, we have developed procedures to grow high quality epitaxial PZT films on SRO/ STO templates through two routes. By building an effective electrical set-up, domain switching behaviors and leakage current mechanisms of these films have been evaluated. Of both growth routes, films of 100 $\sim$ 200 nm have shown low leakage, considerable P_r and convincing switching proofs of 180° domains while films of $\sim$ 200 nm have shown better electrical qualities in terms of retention and saturation. Sub–50 nm films have shown inferior qualities.

The precise composition of our PZT films is unknown despite the fact that the sputtering target and sol-gel solution both contains PZT(52/48). Sol-gel-derived PZT film has been reported to have a gradient composition, which reduces its piezoelectricity. Chemical contents could be analyzed in depth in future, and the diffusion will also be clear especially for ultralthin bottom electrode (< 20 nm), which can help us further optimize deposition procedures to improve the PZT quality.

To further understand the charge transport mechanisms, I-V measurement at various temperatures need to be added since more than one model fit the data in high field range now. For PUND measurements, the wave form used in this thesis was triangular. To increase the switching speed, quasi-square signal with high ramp rate could be employed, which is usually used in commercial devices. By analyzing the switching current, switching time can be extracted, which is an important factor for FeRAM devices. Maximum of switching current should be analyzed because it affects the reliability of the device.

According to our results, for a 100-nm-thick PZT capacitor, with E_c about 70 kV/cm, the operating voltage is about 2 V (about $3E_c$). However, at high frequency the required operating voltage is much higher since E_c is frequency dependent. This undesirable high operating voltage is mainly due to our large capacitor surface ($100 \times 100\,\mu m^2$). According to Tsurumi's work, E_c is strongly dependent on capacitor area. With a new acquired mask for lithography, the area of top electrode can be reduced by more than 3000 times thus E_c at the same frequency can be greatly reduced. Besides, fabrication of smaller capacitors will allow us to study the size effect of area. As a result of the decreasing lateral size, defect density in each capacitor drops, making the realization of thinner workable capacitor possible, thus reducing the operating voltage. With the current large area, capacitor with a thickness under 100 nm is vulnerable to high leakage. For ultrathin PZT film, which is strained on substrate, many properties such as MPB region and T_c will shift due to the compressive force and its ferroelectricity may be enhanced.

Fatigue is one of the most important factors for FeRAM devices, which we have not yet studied. Capacitors with Pt top electrode usually showed degraded switching behaviors after 10^4 cycles. Oxide electrodes such as IrO_2, RuO_2 and $SrRuO_3$ could greatly improve fatigue property to 10^{10} cycles without degrading. Fatigue quality of these capacitors with different top electrodes will be investigated in next work.

In this thesis, all capacitors on the same sample share the same PZT film. The drawback of this structure is crosstalk, which may greatly reduce the memory reliability especially when the memory element density increases. With existing lithographic techniques, the area of capacitor is hard to reduced to less than 0.01 μm^2. To fabricate individual addressable ultrahigh-density ferroelectric memories, new lift-off masks should be investigated. To produce individual capacitors, the mask should stand high deposition temperature and can be easily removed without damaging the ferroelectric elements. A Korean group has succeeded in fabricating PZT capacitors with diameter of 64 nm, density of 176 $Gb/inch^2$ by using anodic aluminum oxide membranes with regular pores.

Further studies on MEMS for sensors, energy harvesters will be based on this work by using the magnificent piezoelectricity of PZT(52/48). By replacing bulk STO substrate with STO buffered Si substrate, which is compatible with the current production technology, the integration of epitaxial PZT on Si and its properties will be studied. For FeRAM application, PZT(20/80) is a better candidate because it offers a mismatch of 1.19% on STO substrate (0.57% mismatch with bulk SRO), which could be more easily strained than PZT(52/48) does (our PZT films were relaxed). PZT(20/80) also offers a higher P_r and strained state will further improve its ferroelectric property.

Even though PZT offers great piezoelectricity, pyroelectricity and ferroelectricity and highly tunable properties by varying Zr/Ti ratio and has already been commercialized in a variety of devices, there is a strong impetus to find alternative lead-free materials of compatible properties due to the harmful effects of lead. In further works, BTO, BSTO and other materials will be introduced.

Optimization of Epitaxial Ferroelectric $Pb(Zr_{0.52},Ti_{0.48})O_3$ Thin-Film Capacitor Properties

Abstract

With the intensive use of modern microelectronic devices in numerous areas, there is an increasing demand for non-volatile memories. FeRAM (ferroelectric random access memory) is one of the most potential next-generation memories for its ultra-low power consumption and high read/write rate. Among various ferroelectrics, PZT ($Pb(Zr_{1-x},Ti_x)O_3$) exhibits high remnant polarization and low coercive field, which make it a promising candidate for FeRAM.

In this dissertation, PZT(52/48) layers of various thicknesses (from 33 nm to 200 nm) have been epitaxially grown on $SrTiO_3$ substrate, with a $SrRuO_3$ interlayer as bottom electrode, using two deposition methods for comparison: sol-gel and sputtering. Three different conductive materials ($SrRuO_3$, Pt and ITO) have been deposited as top electrode. The objective was a detailed study of the electrical and ferroelectric properties of these MFM (metal-ferroelectric-metal) capacitors, with a particular investigation of the influence of elaboration conditions and electrode material on leakage currents and domain switching dynamics.

Sputtered and sol-gel-derived PZT capacitors showed similar properties: Above a minimum workable thickness of about 100 nm for a $100 \times 100\,\mu m^2$ PZT capacitor, they showed low leakage current, high maximum relative permittivity ($600 \sim 1300$) and high remnant polarization ($30 \sim 40\ \mu C/cm^2$). The dominant leakage current mechanisms were identified by fitting the results, showing different contributions as a function of electric field. PFM (piezoresponse force microscopy) characterizations confirmed the existence of ferroelectric domains of opposite directions. Coercive field was found to be highly dependent on work frequency. Besides, imprint properties were found to be dependent on top electrode, annealing procedure and bottom electrode thickness.

***Key words**: PZT ($Pb(Zr_{1-x},Ti_x)O_3$), SRO ($SrRuO_3$), ferroelectric, piezoelectric, sputtering, sol-gel, FeRAM, XRD, leakage current, I-V, C-V, P-E, PFM (piezoresponse force microscopy)*

Optimization des Propriétés de Structures Capacitives à Base de Films Minces Ferroélectricques Épitaxiés de $Pb(Zr_{0.52},Ti_{0.48})O_3$

Résumé

Avec l'usage intensif de dispositifs microélectroniques modernes, il existe un besoin croissant de mémoires non volatiles. La FeRAM (mémoire ferroélectrique à accès aléatoire) est une des mémoires de nouvelle génération les plus prometteuses en raison de sa faible consommation et de sa vitesse élevé de lecture/écriture. Parmi les différents matériaux ferroélectriques, le PZT ($Pb(Zr_{1-x},Ti_x)O_3$) présente une polarisation rémanente élevée et un faible champ coercitif qui en font un candidat de choix pour les FeRAM.

Dans cette thèse, la croissance épitaxiale de couches de PZT (52/48) d'épaisseurs variables (33 $\sim$ 200 nm), sur un substrat de $SrTiO_3$ et une électrode inférieure interfaciale de $SrRuO_3$, a été réalisé par deux méthodes pour comparaison : pulvérisation cathodique et sol-gel. Trois matériaux conducteurs différents ($SrRuO_3$, Pt et ITO) ont été utilisés comme électrode supérieure. L'objectif a été une étude détaillée des propriétés électriques et ferroélectriques de ces structures MFM (métal-ferroélectrique-métal), avec une attention particulière sur l'influence des conditions d'élaboration et de la nature des électrodes sur le courant de fuite et la dynamique de basculement de domaines.

Les capacités élaborées par pulvérisation ou sol-gel présentent des caractéristiques semblables : Au-delà d'une épaisseur minimum d'environ 100 nm, pour une structure capacitive à base de PZT de $100 \times 100\,\mu m^2$, elles montrent un faible courant de fuite, une permittivité relative maximale élevée (600 $\sim$ 1300) et une polarisation rémanente élevée (30 $\sim$ 40 $\mu C/cm^2$). Les mécanismes dominants dans le courant de fuite ont été identifiés par un fit des résultats, manifestant différentes contributions en fonction du champ électrique. Des caractérisations par PFM (microscopie à force piézoélectrique) confirme l'existence de domaines ferroélectriques de directions opposées. Il est aussi montré que le champ coercitif dépend fortement de la fréquence de travail. D'autre part, les propriétés d'impression dépendent de l'électrode supérieure, de la nature du recuit et de l'épaisseur de l'électrode inférieure.

***Mots clefs**: PZT ($Pb(Zr_{1-x},Ti_x)O_3$), SRO ($SrRuO_3$), ferroélectric, piézoélectric, pulvérisation, sol-gel, FeRAM, XRD, currant de fuite, I-V, C-V, P-E, PFM (microscopie à force piézoresponse)*