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ECOLE DOCTORALE DE SCIENCE PHYSIQUES ET DE L’INGENIEUR
SPÉCIALITÉ ELECTRONIQUE

Par Thomas JACQUET

Reliability of SiGe :C HBTs operating at 500 GHz: characterization and modeling

Sous la direction de Cristell MANEUX
et de Niccolò RINALDI

Soutenue le 7 décembre 2016
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Titre : Mécanismes de défaillance des transistors bipolaires SiGe fonctionnant jusqu’à 500 GHz : Caractérisation et modélisation

Résumé :

Le sujet de cette thèse est l’analyse de la fiabilité des transistors bipolaires à hétérojonction SiGe:C et des circuits intégrés associés. Dans ce but, un modèle compact prenant en compte l’évolution des caractéristiques des transistors SiGe:C a été développé. Ce modèle intègre les lois de vieillissement des mécanismes de défaillance des transistors identifiés lors des tests de vieillissement. Grâce aux simulations physiques TCAD complétées par une analyse du bruit basses fréquences, deux mécanismes de dégradations ont été localisés. En effet, selon les conditions de polarisation, des porteurs chauds se retrouvent injectés aux interfaces du transistor. Ces porteurs chauds ont suffisamment d’énergie pour dégrader l’interface en augmentant progressivement leurs densités de pièges. L’une des deux interfaces dégradées se situe au niveau de l’’’espaceur’’ émetteur-base dont l’augmentation de la densité de piège dépend des porteurs chauds créés par ionisation par impact. L’autre interface dégradée se situe entre le silicium et le STI dont l’augmentation de densité de pièges dépend des porteurs chauds générés par ionisation par impact et/ou par génération Auger. En se basant sur ces résultats, une loi de vieillissement a été incorporée dans le modèle compact HICUM. En utilisant ce modèle, l’étude de l’impact des mécanismes de défaillance sur un circuit amplificateur faible bruit a été menée. Cette étude a montré que le modèle compact intégrant les lois de vieillissement offre la possibilité d’étudier la fiabilité d’un circuit complexe en utilisant les outils de conception standard permettant ainsi de diminuer le temps de conception global.

Mots clés : HBT SiGe:C, Fiabilité à long-terme, Dégradation par porteur chaud, Modélisation compact

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Title : Reliability of SiGe :C HBTs operating at 500 GHz: characterization and modeling

Abstract :

The SiGe:C HBT reliability is an important issue in present and future practical applications. To reduce the design time and increase the robustness of circuit applications, a compact model taking into account aging mechanism activation has been developed in this thesis. After an aging test campaign and physical TCAD simulations, one main damage mechanism has been identified. Depending on the bias conditions, hot carriers can be generated by impact ionization in the base-collector junction and injected into the interfaces of the device where trap density can be created, leading to device degradation. This degradation mechanism impacting the EB/spacer interface has been implemented in the HICUM compact model. This compact model has been used to perform reliability studies of a LNA circuit. The CPU simulation time is not impacted by the activation of the degradation compact model with an increase in computation time lower than 1%. This compact model allows performing a reliability analysis with conventional circuit simulators and can be used to assist the design of more robust circuits, which could help in reducing the design time cycle.

Keywords : SiGe :C HBT, long-term reliability, hot carriers degradation, compact modeling

Title : Affidabilità di transistori bipolari a etero giunzione SiGe:C operanti a 500 GHz: caratterizzazione e modelli

Abstract :

L'affidabilità dei transistori a eterogiunzione SiGe:C è un aspetto molto importante nella progettazione circuitale, sia per le tecnologie attuali che per quelle in fase di sviluppo. In questo lavoro di tesi è stato sviluppato un modello compatto in grado di descrivere i principali meccanismi di degrado, in modo da contribuire alla progettazione di circuiti relativamente più robusti rispetto a tali fenomeni, ciò che potrebbe favorire una riduzione dei tempi di progetto. A seguito di una campagna sperimentale e di un'analisi con tecniche TCAD, è stato identificato un meccanismo principale di degrado. In particolari condizioni di polarizzazione, i portatori ad elevata energia generati per ionizzazione a impatto nella regione di carica spaziale, possono raggiungere alcune interfacce del dispositivo e ivi provocare la formazione di trappole. Solo la generazione di trappole relativa allo *spacer* emettitore-base è stata considerata nella formulazione del modello, essendo il fenomeno più rilevante. Il modello è stato utilizzato per effettuare alcuni studi di affidabilità di un amplificatore a basso rumore. Il tempo computazionale non è significativamente influenzato dall'attivazione del modello di degrado, aumentando solo dell'1%. Il modello sviluppato è compatibile con i comuni programmi di simulazione circuitale, e può essere impiegato nella progettazione di circuiti con una migliore immunità rispetto ai fenomeni di degrado, contribuendo così a un riduzione dei tempi di progetto.

Keywords : transistori a eterogiunzione SiGe:C, portatori ad elevata energia, modello compatto

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Unité de recherche

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Résumé Substantiel :

La fiabilité des transistors SiGe:C modernes est un critère important pour le développement de futures applications, en particulier dans le domaine millimétrique. La fiabilité des transistors est étudiée à travers des tests de vieillissement. Ces tests donnent une estimation de la fiabilité caractérisant une technologie de transistor SiGe:C. Cependant, ces résultats de test sont difficilement utilisables pour prédire l'évolution des caractéristiques des transistors sous des conditions de polarisations dynamiques impactant les performances des circuits. C'est donc pour prédire l'évolution des caractéristiques des transistors dans une application que nous avons développé un modèle compact prenant en compte l'activation de mécanismes de vieillissement.

Afin de caractériser l'évolution des caractéristiques électriques des composants, deux campagnes de vieillissement ont été réalisées sur les transistors SiGe :C fabriqués par Infineon Technology AG. Les tests de vieillissement ont été réalisés sur des structures en émetteur commun à des points de polarisations dans et au-delà de l'aire de sécurité de fonctionnement. La première campagne de vieillissement a été réalisée au point de polarisation P1, P2 et P3 sur un banc de test dédié. Les tracés de Gummel en direct et en inverse ont été mesurés durant ces tests de vieillissement à intervalles de temps prédéfinis. Les tests de vieillissement et les mesures DC ont été réalisés directement sur le banc dédié, sans action supplémentaire sur les composants afin de garantir l'intégrité des tests.

La seconde campagne de mesures a été réalisée avec un testeur sous pointe. C'est pourquoi, contrairement à la première campagne, un seul composant a été vieilli à la fois. Cette campagne de vieillissement a été menée pour deux points de polarisation, P23 et P2. Les mêmes caractéristiques électriques DC ont été mesurées que lors de la première campagne.

Le courant de base du tracé de Gummel en direct augmente avec le temps de vieillissement pour les points de polarisation P2P3 durant la première campagne et pour le point de polarisation P23 durant la seconde campagne. Pour ces points de polarisation, la tension collecteur-émetteur est supérieure à BV_{ceo}. De plus, aux faibles niveaux d'injection, le courant de base des composants vieillis aux points de polarisations P2 and P23 (Vce=2V) présentent la même évolution avec la même dynamique temporelle. Le courant de base augmente durant les premières heures de vieillissement avant d'atteindre une valeur constante. La dynamique de cette évolution et la valeur finale dépendent des conditions de polarisation, plus précisément de la valeur de la tension collecteur-émetteur.

Pour les composants vieillis aux points de polarisations P12 et P23, une augmentation du courant de base du tracé de Gummel en inverse est observée. Le courant de base augmente pour le composant vieilli en P12 et atteint une valeur constante après 1h. Pour le composant vieilli sous P23, nous observons une évolution du courant de base similaire à celui observé pour le tracé de Gummel en direct. Cette augmentation du courant de base du tracé de Gummel en inverse semble activée pour un fort courant de collecteur.

Le bruit basse-fréquence des transistors SiGe :C a été analysé. Les origines physiques et la localisation des sources de bruit ont pu être identifiées. Nous avons démontré que l'évolution de la densité de bruit basse-fréquence peut aussi être utilisé comme indicateur de défaillance.

En effet, le bruit basse-fréquence a été évalué pour les composants vieillis sous deux points de polarisation différents jusqu'à 72h pour un courant de base I_b égale à 0.1µA, 1µA et 10µA. Le bruit basse fréquence pour le composant vieilli sous P12 ne montre aucune variation significative durant le temps de vieillissement, ce qui est en accord avec les mesures DC. Pour le composant vieilli en P23, le bruit basse-fréquence pour Ib égal à 1µA et 10µA ne présente aucune variation significative alors que, pour Ib=0.1µA, le bruit basse-fréquence présente une variation. Nous avons montré que les variations de la partie Génération-recombinaison (G-R) du bruit BF à la même source que l'évolution du courant de base du tracé de Gummel en direct.

Cette corrélation entre bruit basse-fréquence et tracé de Gummel en direct peut être expliquée par la création de pièges dans le composant. L'augmentation de la densité de pièges a un impact sur la partie G-R du bruit BF et sur le courant de base à faible injection observé sur le tracé de Gummel. La localisation et l'origine des pièges sont difficiles à extraire de ces résultats.

Afin de déterminer les origines physiques des mécanismes de défaillance, des simulations 2D TCAD ont été menées. Un modèle hydrodynamique avec des paramètres de transport optimisés pour Sentaurus TCAD a été utilisé. Après une calibration des profils de dopage et des paramètres du modèle, des simulations ont été menées pour confirmer les hypothèses des mécanismes de dégradations activés pendant les tests de vieillissement sous différentes conditions de polarisation.

Pour les composants soumis à une tension Vce supérieure à BVceo, P2, P2 et P23, une variation du courant de base pour le tracé de Gummel en direct a été observée. Du fait de la valeur importante de Vce, des porteurs chauds sont générés par ionisation par impact. Ces porteurs chauds sont injectés à l'interface entre l'émetteur-base et le Spacer avec suffisamment d'énergie pour rompre les liaisons covalentes à l'interface, augmentant la densité de pièges. Cette augmentation de la densité de pièges à l'interface EB-Spacer provoque une augmentation du courant de base du tracé de Gummel en direct aux faibles niveaux d'injection.

Pour les composants vieillis au point de polarisation P23 et P12, une variation du courant de base pour le tracé de Gummel en inverse a été observée. Cette augmentation du courant de base est attribuée à l'activité de pièges à l'interface entre le Silicium et le STI. Les pièges de l'interface STI/Si sont attribués à deux mécanismes de défaillance différents :

- Pour les conditions de polarisation associé à des tensions V_{ce} supérieures à BV_{ceo}, l'ionisation par impact peut être le mécanisme dominant,
- Pour les conditions de polarisation associée à des tensions V_{ce} inférieures à BV_{ceo}, et à fort courant, les recombinaisons Auger peuvent être le mécanisme dominant.

En se basant sur ces mécanismes de dégradations, une loi de vieillissement a été proposée prenant en compte les conditions de polarisation. Cette loi de vieillissement décrit l'évolution des dégradations de l'interface EB-Spacer, en fonction des conditions de polarisations et du temps de vieillissement. Pour intégrer cette loi de vieillissement dans le code Verilog-A du modèle compact, la dérivée de cette loi de vieillissement est calculée.

Pour implémenter la loi de vieillissement dans un modèle compact, le modèle HICUM a été choisi. Ce modèle a été choisi par le projet DOTSEVEN pour simuler les transistors SiGe:C. Le modèle compact HICUM a l'avantage de décrire de nombreux phénomènes physiques régissant les transistors SiGe:C. Pour implémenter la loi de vieillissement, le paramètre I_{REpS} a été utilisé. Ce courant correspond à la partie du courant de base correspondant à de l'interface EB-Spacer. I_{REpS} a été convertie en variable selon la loi de vieillissement.

En utilisant ce modèle compact, une simulation de fiabilité d'un amplificateur faible bruit à 4 étages a été réalisée. L'activation de la loi de vieillissement n'a pas d'impact significatif sur le temps de simulation , soit une augmentation du temps de simulation inférieure à 1%. En prenant en compte les dégradations de l'interface EB-Spacer en fonction des conditions de polarisation de chacun des transistors, le signal de sortie du circuit ne présente pas de variation significative avec le temps en dépit de l'augmentation du courant de base de certains transistors du dernier étage . Ces résultats montrent la robustesse du circuit face aux dégradations de l'interface EB-Spacer. D'un point de vue de la méthodologie d'analyse de la fiabilité, la possibilité d'évaluer l'évolution de chaque transistor a été démontrée avec un faible impact sur le temps de simulation. De ce fait, cette méthodologie apporte un outil d'évaluation de la fiabilité supplémentaire.

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Chapter 1 State of the art of SiGe:C HBT reliability

1.1. General introduction

The first bipolar transistor has been developed in 1947 by J. Bardeen, W. Shockley et W. Brattain. Since this invention, semiconductor industry has witnessed exceptional growth and achievements in integrated circuit (IC) manufacturing. The evolution of the bipolar technology, following Moore laws [Moor_1975], has been driven by the device downscaling until now.

The development of the Silicon Germanium based Heterojunction Bipolar Transistor starts in 1987 [Lyer_1987]. Based on band-gap engineering, modern Silicon (Si) Germanium (Ge) HBT have been developed to extend the performance of standard silicon based transistors. The Heterojunction Bipolar Transistor is a solution to develop ultra-speed applications. Compared to III-V HBTs, SiGe HBTs allow for a higher level of integration and a lower cost. More specifically, SiGe HBTs allow a really good integration level in BiCMOS technology where analog and digital signals can be processed on the same System-on-Chip (SoC). These advantages of SiGe HBTs compared to other technologies, make the SiGe HBT technology the perfect candidate to develop low-cost and highly integrated terahertz applications.

In Europe, several projects have been launched to develop SiGe:C HBT technology. During the DOTFIVE project [Dotfive_online], the operating frequency of SiGe:C HBT has been pushed toward 0.5 THz. This project has been followed by the DOTSEVEN project [Dotseven_online] to further improve the operating frequency up to 0.7 THz and envisage future terahertz applications in the 0.1 to 1 THz frequency range. To give an example, a terahertz receiver front-end based on SiGe:C HBT technology [Ojef_2010], opens new opportunities like THz imaging. These applications cover a wide range of domains, like security, high speed wireless communication or medical imaging. The reliability of these applications appear also as a challenge which has been considered in the DOTSEVEN project.

Indeed, SiGe:C technology improvements are performed by shrinking the structure dimensions to reduce the parasitic elements and by improving the doping profile. Among several consequences, these improvements lead to the increase of hot carrier generation. This increase of hot carriers can worsen device reliability through the degradation of the device interfaces [Sass1_2014] leading to the onset of failure mechanisms.

In this context, a new tool for designers has been proposed in this Thesis: The compact model takes into account the relevant failure mechanisms. This new tool, already used for III-V devices [Ardo_2012], could help designers to enhance performance of future applications with a limited impact on reliability.

1.2. Terahertz semiconductor technologies

1.2.1. Terahertz application

The SiGe:C technology has been developed for millimeter wave (mm-wave) or terahertz applications which lie in the frequency range between microwaves and infrared light, corresponding to the 0.3 THz and 3 THz frequency range. Terahertz signals can penetrate many materials. This ability of terahertz signals therefore can be used for medical imaging with a limited damage to organic tissues as compared to X-ray.

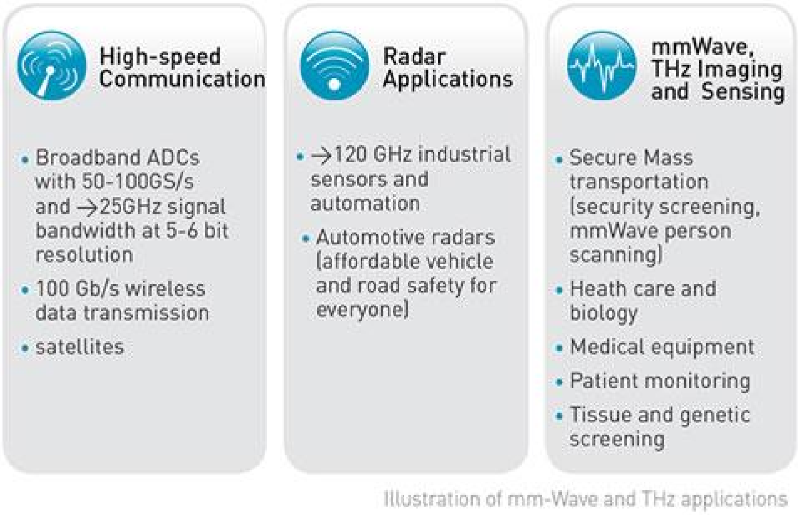


Figure 1 mm-Wave applications proposed by DOTSEVEN project

A large number of mm-wave applications (Figure 1) are possible, including THz imaging and sensing for biology and medical sciences [Taba_2015], non-destructive evaluation [Fuka_2015], homeland security [Fede_2005]. Ultra-high-speed communications appears to be a major application market [Akyi_2014].

1.2.2. Terahertz semiconductor technologies

1.2.2.1. General overview

Diodes and transistors are the two semiconductor electronic devices used to implement terahertz systems. Diodes have already been widely employed for various terahertz systems. Impact avalanche transit time (IMPATT) diodes, Gunn diodes, and resonant tunneling diodes (RTDs) are widely employed as sources [Mile_2007]. Whereas Schottky barrier diodes are a popular choice to detect terahertz signals [Sank_2005].

However, as an active device, transistors can be better integrated in multistage systems than diodes. Therefore, the main focus lies on the development of high speed transistors integrated in complementary metal oxide semiconductor (CMOS) or in III-V technologies.

To characterize the RF performance of a transistor technology, two figures of merits are commonly used, the transit frequency (F_t) and the maximum oscillation frequency (F_{max}). The transit frequency (F_t) corresponds to the unity gain cut-off frequency in the common emitter configuration which is the frequency where the small-signal current gain β_F equals unity [Gumm_1969]. The maximum oscillation frequency (F_{max}) corresponds to the frequency at which the unilateral power gain becomes unity.

For RF circuit design, the F_{max} FoM, corresponding to operating frequency limit of the device, is the most used to characterize the device ability to develop terahertz applications. However, the maximum oscillation frequency is sensitive to device layout and more difficult to extract than the transit frequency. Therefore, F_t is the most frequently used to characterize and compare device technologies [Rieh_2009].

1.2.2.2. III-V technology

Widely used transistor technologies for terahertz applications are the HBT (Heterojunction Bipolar Transistor) and the HEMT (High Electron Mobility Transistor) III-V device technology. The record of RF performance has been reached for the III-V InP HEMT technology with an F_{max} at 1.2THz [Lai_2007]. For the 0.25µm InP HBT technology [Urte_2010], the published RF characteristics F_t/F_{max} are equal to 392GHz and 859GHz, respectively, at I_c=13mA. Therefore, this technology is a good candidate to develop terahertz application. Moreover, the high speed of III-V transistors comes along with an excellent noise figure (NF).

However, the hole mobility of III-V devices is low in comparison with the silicon value. Hence, complementary logic blocks as in CMOS technology are rather hard to design. Moreover, the expensive and small wafers and the low reliability of these devices, increase the fabrication costs reducing the attractiveness of this technology for high volume applications. These arguments make silicon the favorable technology for large scale applications despite the lower performances. Therefore, high performance SiGe HBTs integrated in a BiCMOS technology appears as a promising solution.

1.2.3. SiGe:C Technology

SiGe HBTs provide a higher current driving capability, higher linearity, larger transconductance g_m, lower 1/f noise property, excellent reliability, better device matching and superior performance in comparison with the standard silicon metal oxide semiconductor field effect transistors (MOSFETs) [Rieh_2009]. This makes them ideal devices for microwave power applications [Ruck_2012], [Chev_2012]. Therefore, several companies have chosen to integrate their high performance SiGe HBTs in a lower cost CMOS process (BiCMOS) which allows an improved functionality but at the same time increases process complexity due to HBT integration.

In contrast with high speed III-V technologies, the intrinsic material properties of Si limits the device operation speed. Nevertheless, SiGe HBT technology continues to gain momentum. Optimized device structure along with aggressive scaling lead to reduce the gap of RF performances with III-V devices (F_t=300GHz, F_{max}=500GHz [Hein_2010]) as reported within project DOTFIVE [Dotfive_online]. In the follow up project DOTSEVEN [Dotseven_online], the performance of SiGe has been pushed to a higher frequency (F_{max}=570GHz

[Bock_2015]). Moreover, SiGe:C HBT has been integrated in a new BiCMOS technology to replace expensive III-V components in radar production [Knap_2012].

1.3. Bipolar safe operating area

1.3.1. Physical limits

Bipolar transistor technologies have been developed to achieve new applications in the terahertz range, like terahertz communications [Song_2011]. However, all bipolar devices, like SiGe:C HBT, suffer from various feedback mechanisms, which may cause instability and device failure. To avoid the activation of these mechanisms, a Safe Operating Area (SOA) has been defined. As explain in [Rina_2005] [Rina_2006], self-heating and impact ionization are two main mechanisms limiting the operation of bipolar transistors. A clear understanding of these mechanisms is thus an obvious prerequisite for the designers and technologists, in order to exploit the maximum circuit performances achievable with a given technology.

1.3.2. Thermal runaway

One of the well-known damaging mechanisms is the thermal runaway activated by the self-heating of the device [Rina_2005] [Liou_1994]. When bipolar transistors operate at high power, the increase of junction temperature causes the intrinsic carrier concentration to increase. As a result, the collector current increases. At high power operations, the I_c-V_{be} curve can bend backwards at high currents. Once the device hits the bend-over point, two possible operating points appear in its current-voltage characteristics, leading to the device instability.

To estimate the junction temperature of the device, and therefore the thermal runaway activation, the thermal resistance, R_{th}, of the device is used. A simple equation (equation 1.1) is used to estimate the junction temperature:

$$\text{[illegible]} = \text{[illegible]} + \text{[illegible]} \cdot \text{[illegible]} \qquad 1.1$$

To avoid the destruction of the device, bias conditions must be defined within the safe operating area to avoid this thermal runaway.

1.3.3. Avalanche effect

A second limit of the safe operating area is the avalanche effect, [Rina_2006]. Under large reverse bias conditions, a large electric field takes place in the base-collector junction. This high electric field accelerates electrons from the emitter to the collector. When carriers are injected in the base-collector space charge region, they can gain enough energy to create free electron-hole pairs via collision with bound electrons (impact ionization) [Lu_1989]. These carriers can subsequently generate new electron-hole pairs. This creation of electron-hole pairs results in a hole current which is back injected in the base yielding a negative base current. In a similar way as the thermal runaway, an instability condition occurs in the device, and possibly cause the destruction of the device.

One parameter used to characterize the activation of the impact ionization effect is the open-base breakdown voltage (BV_{ceo}). BV_{ceo} corresponds to the collector-emitter voltage when the base current equal to 0A and therefore represents the upper limit of the collector-emitter voltage under forced base current conditions.

1.3.4. Safe operating area

The limits of the SOA are mainly defined by two mechanisms, self-heating, leading to thermal runaway and impact ionization, leading to avalanche effect. The safe operating area is thus limited by these two mechanisms. As explained in [Rina_2006][Lee_2006], the combined effect of impact ionization and self-heating is complex. Different experimental methodologies have been developed to define the SOA limits, like the one presented in [Cism_2010]. This methodology consists in measuring the J_c-V_{ce} curves in specific bias configurations to avoid the destruction of the device.

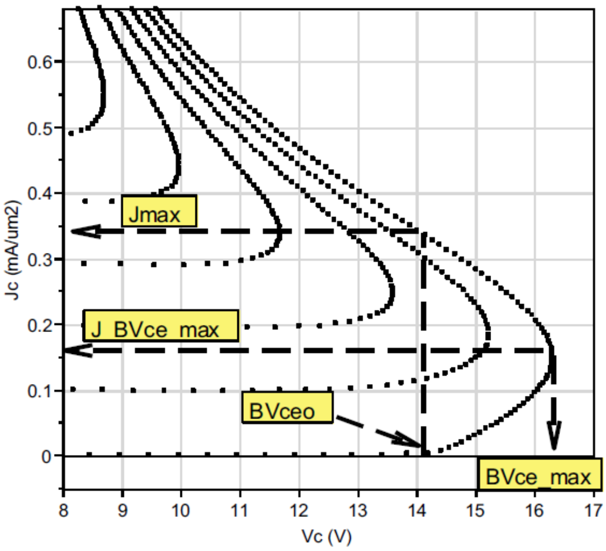


Figure 2 HBT J_c -V_{ce} curve. Breakdown parameters of the device are reported in the figure. Picture from [Cism_2010]

A typical J_c-V_{ce} curve measured using this methodology is presented Figure 2. On this J_c-V_{ce} curse, the snap-back behavior of the device, an instability effect, can be observed. Using this curve, the breakdown parameters of the HBT can be extracted, like BV_{ceo} corresponding to maximum collector voltage while the collector current is substantially low. J_max corresponds to the maximum current achievable in the snap-back branch at BV_{ceo}. Another breakdown parameter, the maximum collector voltage BV_{ce_max}, can also be extracted using the same curve with the associated current density $J\_BV_{ceo\_max}$.

Based on the extraction of breakdown voltage and taking into account self-heating and impact ionization, a safe operating area can be defined. Figure 3 shows the limits of the safe operating area of a NPN device on thick film SOI with effective area equal to 0.25x10µm². The safe operating area is limited by three physical mechanisms. The first one is electromigration at low V_{ce} and extremely high J_c. Electromigration impacts the back end of line, by degrading metal interconnections. For medium V_{ce} and high J_c, the SOA is limited by the self-heating of the device. At higher V_{ce} and lower J_c, impact ionization limits the SOA.

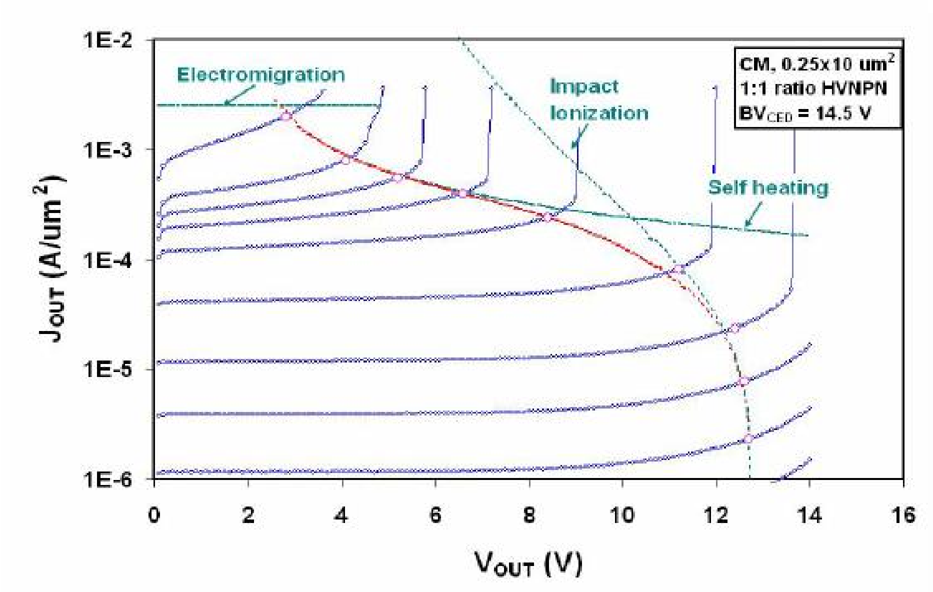


Figure 3 Safe Operating Area of bipolar transistor showing different physical limits.
Picture from [Kim_2007], SOA of a SiGe HBT on SOI.

1.4. Reliability of modern SiGe:C HBT

1.4.1. SiGe:C HBT SOA

1.4.1.1. Improvements of SiGe:C HBT and impact on SOA

To improve the figures of merit F_t and F_{max}, the device structure has to be downscaled [Schr1_2011] [Schr2_2011]. In this publication, the “ultimate” limit of SiGe HBT has been studied by simulation, based on physical and application oriented considerations. The resulting SiGe HBT has a F_t/F_{max} at 1.98THz@J_c=139mA/µm² and 0.98THz @J_c=168mA/µm², respectively.

As mentioned in the previous section, the SOA is limited by self-heating and avalanche effect. These two effects are characterized by the thermal resistance for self-heating and by BV_{ceo} for avalanche effect. The BV_{ceo} is estimated between 1V and 1.2V, and the thermal resistance around 76000K/W. These values could considerably reduce the SOA of future SiGe devices.

For present SiGe:C devices, the thermal resistance is not yet too high to limit practical applications, around 2000K/W for STMicroelectronics SiGe:C HBT [Ales_2010]. However, BV_{ceo} has decreased for advanced SiGe:C HBT. Indeed, the BV_{ceo} is measured at 1.5V for Infineon technology SiGe:C HBT exhibit F_t/F_{max}= 240GHz/380GHz at J_c=10mA/µm² [Chev_2011].

Hence, the downscaling of SiGe:C HBT reduces BV_{ceo}, limiting the SOA. This limit of V_{ce}, lower than BV_{ceo}, has a huge impact on future application performances, like the power amplifier with a lower output voltage swing and therefore a lower output power.

1.4.1.2. Extending SOA

The BV_{ceo} is measured in an "extreme" condition, the open base configuration, which is rarely the case in real applications. As proposed by [Rick_2001] and [Kraf_2005], the SOA can be extended above this value if some bias conditions are respected. Figure 4 from [Rick_2001] illustrates the evolution of the output characteristics as a function of the driving conditions. When the device is controlled by the base current, the instability occurs at $V_{ce} = BV_{ceo}$, confirming the previously mentioned limit of the SOA. For base voltage controlled device, the instability occurs at a collector-emitter voltage higher than BV_{ceo} and lower than BV_{cbo} and for an even higher V_{ce} for an emitter current controlled device.

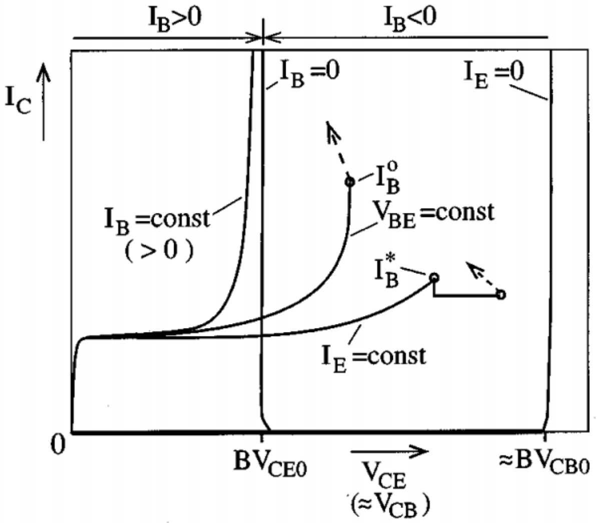


Figure 4 Influence of the impact ionization on the output characteristics for constant I_b, V_{be} and I_e.
Picture from [Rick_2001].

To reach a voltage higher than BV_{ceo}, the device has to be controlled by the base voltage or the emitter current with a low external base resistance to allow excess carriers, generated by impact ionization, to flow out. According to these observations, [Kraf_2005] proposed to extend the safe operating area above BV_{ceo} taking into account the external base resistance and the temperature of the device.

1.4.2. Aging tests of SiGe:C HBT in the SOA

The safe operating area corresponds to the limits of bias conditions of SiGe:C HBT. The SOA is defined to avoid the destruction of the device due to instability effects leading to catastrophic destruction. However, this not warrants the device from degradations occurring while it is biased within the SOA. Indeed, the device also suffers from wear-out mechanisms that generally decrease the current gain, and ultimately limit the device lifetime.

1.4.2.1. Reverse stress test

The studies of bipolar transistor aging begun at the end of the eighties [Josh_1987]. The main issue at that time was to assess degradation for a strongly reverse biased emitter-base junction, since the reverse BE breakdown voltage (at the BE perimeter) had declined to below 1V and a reverse-biased EB junction may occur in circuit operation. When the EB junction is subject to a sufficiently high reverse voltage, the current flowing through the BE perimeter junction is mainly due to band-to-band tunneling. In these conditions it was suggested that the main degradation mechanism was related to hot holes, [Gogi_2000]. This kind of aging tests is still performed on modern bipolar transistors.

A reverse stress test has been performed by [Sass2_2014] on IHP 0.13µm SiGe BiCMOS technology exhibiting a peak cut-off frequency F_t of 240 GHz and a F_{max} of 300 GHz [Ruck_2010]. The samples have been stressed at V_{eb} equal to 3.75, 4.00, 4.25 and 4.50V hence always above the reverse open-collector breakdown voltage BV_{ebo} estimated at 1.7V for this process. The applied stress conditions, rather extreme and very far from the usual device bias conditions, caused the acceleration of the degradation and, thereby, allow an estimation of the transistor time-to-failure (TTF).

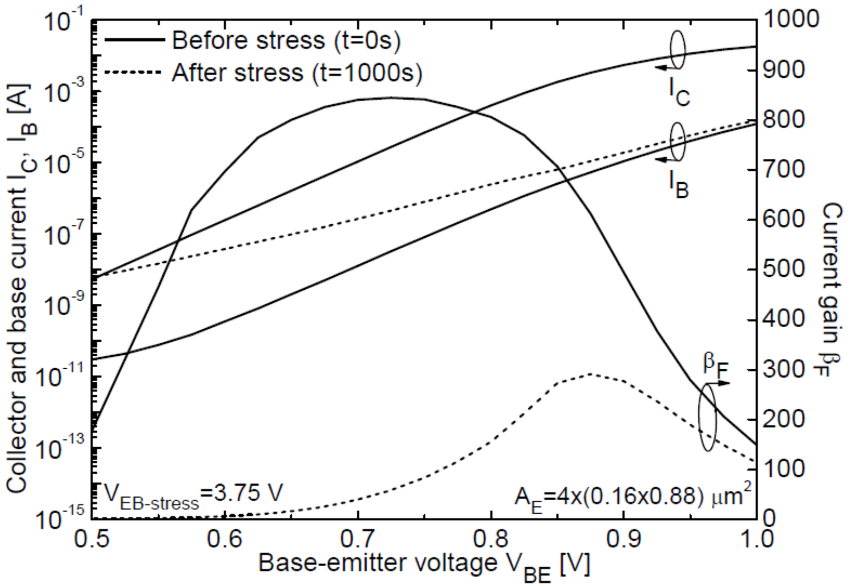


Figure 5: Current (left) and current gain (right) measured at Vcb=0V of one SiGe:C device before and after reverse stress test at $V_{eb\text{-stress}}$= 4.0V for 1000s. Picture from [Sass2_2014]

A typical result of reverse stress test is represented Figure 5. After 1000s at V_{eb}=3.75V, the collector current remains almost constant while the base current increases, consequently, the current gain $\beta_F=I_c/I_b$ decreases. This evolution of DC characteristics has been explained by the large reverse current during the stress test. This reverse current, which is primarily confined to the emitter perimeter region, under the influence of localized electrical fields can generate hot carriers. These hot carriers can damage the Si-SiO_2 interface by increasing the interface trap density at this interface.

1.4.2.2. Mixed-mode degradation

During the 2000 decade, a new degradation mode of SiGe:C HBT has been reported which is more appropriate to device operation in mixed-signal circuit applications, [Zhan_2002]. Mixed-mode degradation occurs when a high collector current density and a high collector-base voltage are imposed simultaneously to the device. In this case, hot carriers are generated by impact ionization in the base-collector space charge region. Some of the carriers may be redirected towards oxide-silicon interfaces, either at the emitter-base sidewall or at the shallow trench. Then, if carriers have enough energy when they reach the interface, they may create defects.

Results of mixed-mode stress test has been reported in [Zhu_2005] for SiGe HBT exhibiting a transit frequency of 120GHz [Jose_2001]. For mixed-mode stress, the device is biased in a common-base mode under variable forced emitter current and collector-base conditions. The stress tests usually range from 1msec to 1000 sec.

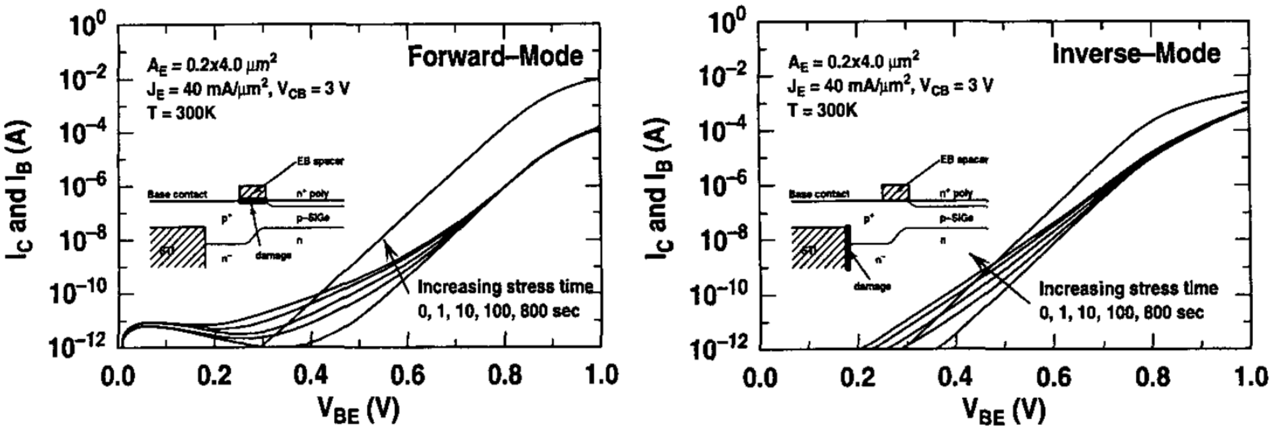


Figure 6 Forward-mode and inverse-mode Gummel plot evolution during mixed-mode stress test of a device aged at V_{cb}=3V and J_E=40mA/µm². Pictures from [Zhu_2005].

A typical forward-mode Gummel plot and an inverse-mode Gummel plot are shown in Figure 6 from [Zhu_2005] for a device aged at V_{cb}=3V and J_e=40mA/µm². For both Gummel plots, the base current increases with the stress time. The increase of the base current in the forward-mode Gummel plot is attributed to the degradation of the EB-spacer interface damage, while the base current increase in the inverse-mode Gummel plot corresponds to STI/Si interface damage.

1.4.3. Long-term reliability

Reverse stress tests and mixed-mode stress tests have been performed to estimate the robustness of device. The main goal of these stress tests is the evaluation of the time-to-failure of the device by extrapolation of the degradation at circuit bias conditions. One limit of these stress tests is the estimation of device characteristics evolution as a function of bias conditions during the circuit operating time.

Based on the same conclusion, [Fisc_2014] has proposed to study the long-term reliability of SiGe:C HBT. This methodology is based on the observed base current evolution and can be described as follows:

- traps created at the EB spacer oxide interface cause an increase in the non-ideal forward-mode base current due to additional Shockley-Read-Hall (SRH) recombination current.
- traps annihilated by thermal recovery (self-annealing). This reaction is thermally activated and when hot carrier injection is switched off annealing can occur through thermal recovery.

Altogether this leads to complex dynamics of trap generation and annealing. The characterization of trap generation as a function of bias conditions has been reported in [Fisc_2015] for mixed-mode and reverse stress tests for SiGe:C HBT from IHP's 0.13µm BiCMOS technology exhibiting a F_t/F_{max} equal to 250/300 GHz, respectively. The increase of the base current and the reduction of the device current gain has been reported in Figure 7 for both long-term stress tests.

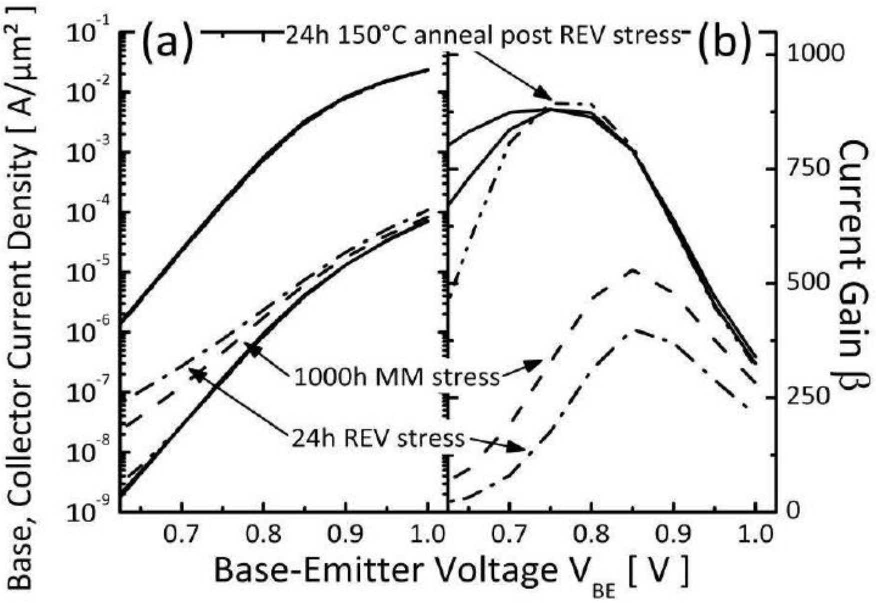


Figure 7 forward Gummel chracteristics (a) and current gain (b) before and after Mixed-mode and reverse long-term stress tests and a 24h post stress aneal. Picture from [Fisc_2014].

To characterize the annealing of trap density by thermal recovery, the 100h reverse stress test was followed by a high temperature anneal at 150°C. An almost full recovery of the base current is then observed after 24h.

Ultimately, HBT degradation is the result of the interplay between trap creation (aging) and annihilation (recovery). This is already obvious for DC stress but the consequence for the HBT during its duty cycle in a given circuit is more complex. In power amplifiers for example, the HBT operating bias point quickly switches between two extremes: the state of low V_{cb} and high J_c (annealing region) and the state of high $V_{ce} > BV_{ceo}$ and low J_c (aging region) as indicated in the inset of Figure 8. In Figure 8, 1000 switching cycles are then compared with 1000s of pure DC stress.

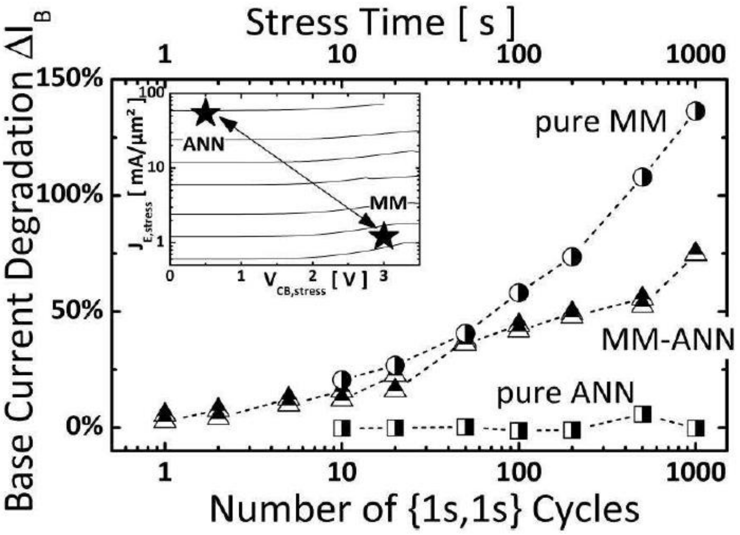


Figure 8 HBT degradation during pure MM and high-current (ANN) stress and 1s cycles between both states (MM-ANN). Inset shows the stress load conditions. Picture from [Fisc_2014].

After 100 cycles, the resulting base current increase stays well below that of pure mixed-mode stress. Aging of the device in the mixed-mode state occurs but meanwhile, the high-T_j state yields a significant annealing.

This experimental long-term analysis of mixed-mode and reverse SiGe HBT base current degradation shows that aging is a complex function of the electrical load, local temperature, and particularly of stress-time. Device degradation in circuit applications is the result of the interplay between trap creation (aging) and annihilation (recovery), depending of the bias conditions.

1.5. This thesis

1.5.1. Long-term reliability modeling

The modern SiGe:C HBT reliability is mainly affected by hot carrier degradation, increasing with device downscaling and more severe operating conditions. The reliability of SiGe:C HBTs is historically studied through stress tests. These stress tests have been realized to estimate the time-to-failure of the device by applying extreme bias conditions and tracking the evolution of device characteristics. The advantage of these techniques is the estimation of the device life time on the basis of short-term results with stress-times up to few hours. However, as described in section 1.4.3 of this chapter, the device bias conditions in circuit operation switching between extreme conditions leads to over-estimate the degradation of the device.

This difference between stress tests and real circuit operating conditions is also studied in the MOS technology which is also affected by hot carrier degradation. In MOS devices, hot carrier injection affects the gate interface. For this device, a long-term circuit aging models have been proposed, e.g. [Zhen_2009]. The model proposed by [Zhen_2009] takes into account the specificity of the application, active and sleep modes, to estimate the reliability of circuit. However, this model is used for digital applications with only two device states, ON or OFF, while bipolar technology is used for analog applications with a wide range of bias conditions.

To estimate the SiGe:C HBT reliability for these applications, the bias conditions in the circuit have to be taken into account. In [Ardo_2012] it has been proposed to estimate hot carrier degradation in practical circuit applications by implementing the aging laws in the transistor compact model. This methodology provides an accurate description of device reliability by computing degradation laws directly in the compact model. Due to its straightforward implementation into commercial computer-aided design (CAD) flows, this method allows circuit-designers to realize a reliability-aware circuit architecture at the early stage of the design procedure, well before circuit fabrication.

1.5.2. Organization of this thesis

This thesis is organized as follows:

Chapter 2 Aging tests This chapter presents the aging tests used to characterize the damage mechanisms of the SiGe:C HBT fabricated by Infineon technology AG. After a description of the samples used during this work, aging stress tests are presented. Results of the aging tests performed at different bias conditions are then presented.

Chapter 3 Low-frequency noise The low-frequency noise is studied before aging tests with a description of its different components. The low-frequency noise is then used as an additional parameter to analyze degradation effects. Actually, low-frequency noise is sensitive to evolution of trapped carrier in the device. The evolution of LF-noise can help to characterize and locate trapped charge in the structure. Therefore, LF-noise has been measured during aging tests.

Chapter 4 Physical simulation with TCAD This chapter describes the physical simulation performed to identify the physical origin of damage mechanisms. The SiGe:C structure has been drawn using Sentaurus TCAD software. The physical origin of the damage mechanisms and their impact on the DC characteristics of the device is described. An equation describing the evolution of damage mechanisms is then proposed.

Chapter 5 Compact model This chapter describes the implementation of the aging laws in the HBT compact model. The aging laws have been integrated into the compact model. To test the aging compact model, a reliability analysis has been performed on a LNA circuit.

Chapter 6 Conclusion Majors results of this work are summarized.

Chapter 2 Aging tests

Description and results

2.1. Introduction

The first step to develop a compact model including the aging laws is a proper characterization of the damage mechanisms occurring in the SiGe:C HBT detail in section 2.2. In literature, to characterize damage mechanisms, conventional stress tests are performed. These conventional stress tests are performed in specific bias configurations such as the reverse stress test [Gogi_2000].

These stress tests are performed at aggressive bias conditions to accelerate device damage mechanisms. The advantage of this bias conditions, very far from the safe operating area borders, is the shorter stress time required to produce significant degradation. Based on accelerated test results, the time-to-failure of the device technology can be estimate. Results of stress test performed on the SiGe:C HBTs studied during this thesis, have been performed and published in [Sass1_2014]. In this study, relatively short stress times and aggressive bias conditions are considered.

In order to study long-term reliability in circuit operating conditions it is necessary to develop a compact model including the aging laws. Therefore, a long-term stress tests has been proposed and detailed in the section 2.3 of this chapter. Bias conditions are adapted to applications targeted by DOTSEVEN project [Dotseven_online] and a large stress test time is reached, up to 1000h. In section 2.4, the long-term aging test results are reported and analyzed according to the bias conditions.

2.2. SiGe:C technology

2.2.1. Infineon SiGe:C technology

During the DOTFIVE project [Dotfive_online], AC characteristics of Infineon SiGe:C HBT technology fabricated in the 200nm node have been pushed up to the terahertz range. To obtain such AC performances, a conventional architecture with vertical base link is used. The architecture specification is described in [Chev_2011], which summarizes the remarkable optimization of the architecture from Infineon technology AG. The fabrication of this device is based on a conventional double-polysilicon self-aligned architecture with epitaxial growth of the base (DPSA-SEG), detailed in Figure 9. To improve the transit frequency and the maximum oscillation frequency, the germanium profile of the base and the doping of the emitter and collector, Figure 10, are optimized to decrease transit times. Additionally, the size of the base-emitter spacer has been shrunk to reduce the base access resistance.

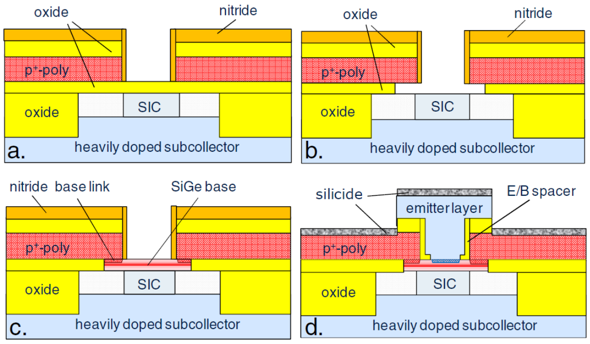


Figure 9: Conventional DPSA-SEG HBT process. Pictures from [Chev_2011]

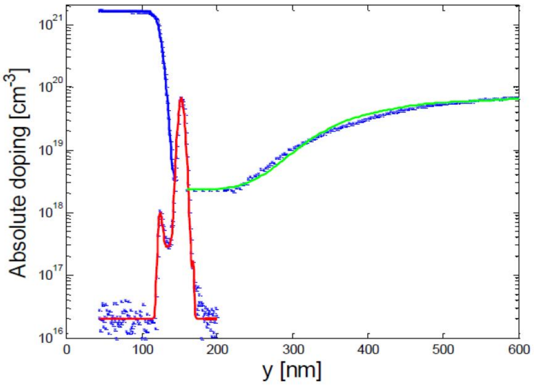


Figure 10: Germanium profile of the base (red line) and doping profile of the emitter (blue line) and collector (green line).

Based on this optimized architecture, a scaled HBT has been integrated in a 130nm technology node (B7HF500), which is the device considered in this thesis work. This transistor exhibits a W_{ew} equal to 230nm and a W_e of 130nm (Figure 11). HBTs feature a collector-emitter breakdown voltage of 1.5V and a collector-base breakdown voltage of 5.5V. The pinched base resistance is 2.6 kW/sq and the maximum β is 1300 at V_{be}=0.6 V.

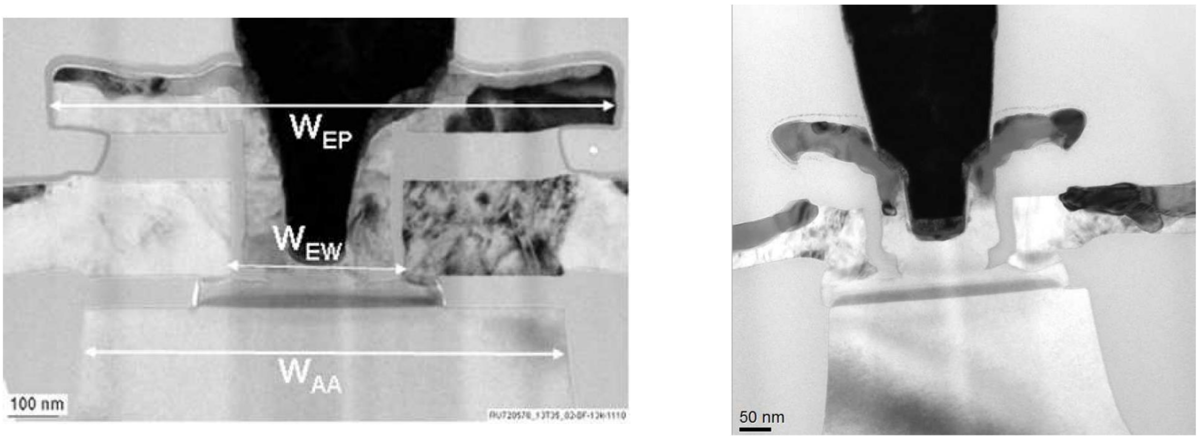


Figure 11 TEM picture of B7HF200 and B7HF500 transistor. Pictures from [Chev_2011].

They provide a f_T of 240 GHz, a f_{max} of 380 GHz at J_C = 10 mA/µm^2 (Figure 12) and a ring-oscillator gate delay time t_D of 2.38 ps measured on 53-stage CML ring-oscillators operating at a collector current density of 14mA/µm^2 [Knap_2010].

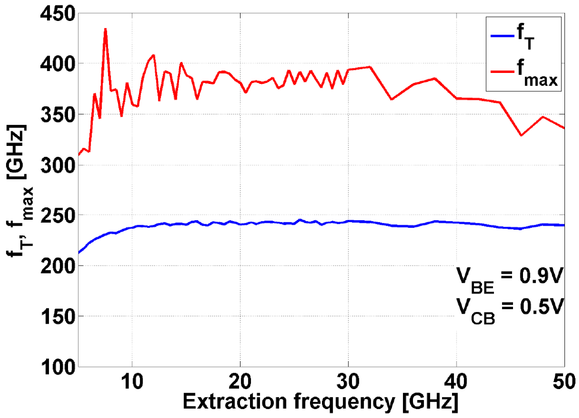


Figure 12: F_t and F_{max} of studied HBT for different extraction frequency. Pictures from [Chev_2011].

2.2.2. Thermal resistance extraction

One limit of SiGe:C HBTs is the thermal runaway due to the self-heating (see Chapter 1 section 1.3.2). Thermal runaway is characterized by a critical junction temperature of the component. Besides, associated with long-term reliability, thermal recovery could occur in the device, limiting the impact of damage mechanism on DC electrical characteristics as described in [Fisc_2014]. To characterize the junction temperature of the device, and therefore possible recovery or thermal runaway, the device thermal resistance R_{th} has to be determined.

To extract the R_{th} parameter, different methodologies can be used [Meno_2005], [Mane_2004], [Hout_2004], [Suli_2005], [Gran_2007], [Nodj_2009]. The selected methodology to extract the thermal resistance is detailed in [Gran_2007]. This methodology developed in IMS lab can be explained in two steps.

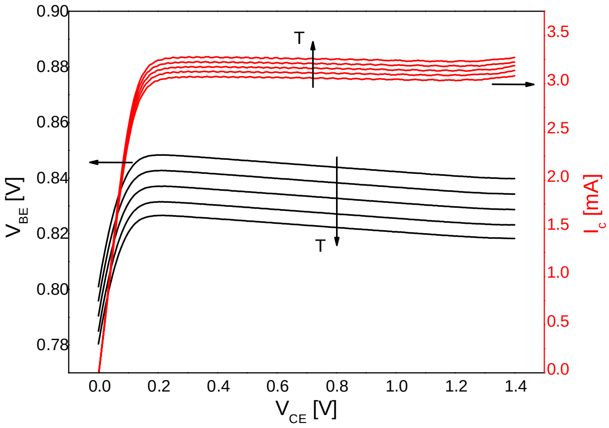


Figure 13 Base emitter voltage and collector current function of the collector emitter voltage at constant base current of SiGe:C HBT under test for different ambient temperatures

The first step consists in measuring the collector current I_c and the base emitter voltage V_{be} as a function of the collector-emitter voltage V_{ce}. This measurement is performed at different controlled ambient temperatures T_i between 300K and 370K at a constant base current I_b. The base current value is sufficiently high to activate the self-heating and low to avoid a significant ohmic drop across the access base resistance. Results of these measurements performed on the SiGe:C HBT under investigation in this thesis have been reported in Figure 13. These results show an increase of the collector current I_c with the temperature when V_{be} decreases.

$$T_i = T_j - P_{diss} \cdot R_{th} \qquad 2.1$$

With $$P_{diss} = V_{ce} \cdot I_c + V_{be} \cdot I_b \qquad 2.2$$

The second step consist in plotting the dependence of the ambient temperature T_i as a function of the dissipated power. Using equation 2.1, T_i as a function of the dissipated power is represented Figure 14. The slope of these curves correspond to the thermal resistance R_{th}, equation 2.1.

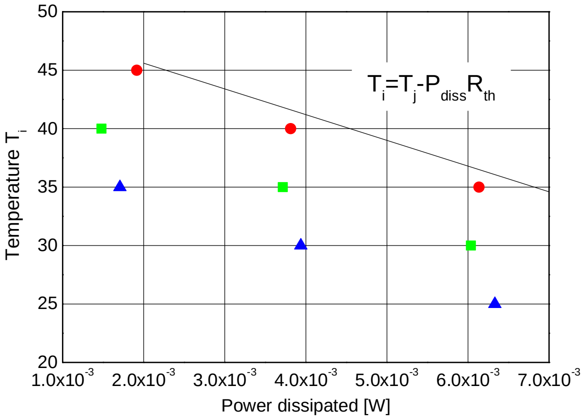


Figure 14 Junction temperature as a function of dissipated power for different values of V_{be}

Figure 14 shows the results for SiGe:C device under investigation in this thesis. The evaluated R_{th} is 2200K/W for CBEBC samples. This value is consistent with the thermal resistance extracted in [Ales_2010], ranging between 1691 and 2306K/W, as a function of the deep trench depth, for SiGe:C HBT manufactured by STMicroelectronics with almost same size (Ae=0.13x9.88µm²).

2.2.3. Samples

Samples manufactured by Infineon technology AG, presented in Table 1, have been used to perform the reliability investigations. Every sample has a double collector and double emitter configuration (CBEBC). This CBEBC configuration is chosen to limit the self-heating effect and to optimize the homogenous distribution of the electric field in the structure. The test structures used to perform the stress tests are designed for RF measurement with a ground-signal-ground pad (GSG pad). Furthermore, samples have an emitter-common configuration with the emitter and the substrate connected to the ground pad.

Name	Draw dimension		Effective dimension		Number of device in parallel	Reference in module AC_NPNHS11 (TD4)
	We	Le	We	Le		
Size 1	0.2µm	1µm	0.13µm	0.93µm	9	TAS010C20
Size 2	0.2µm	2.8µm	0.13µm	2.73µm	3	TAS028C20
Size 3	0.2µm	10µm	0.13µm	9.93µm	1	TAS100C20

Table 1: HBT size under stress test

Size 1 and size 2 samples are composed of 9 HBTs and 3 HBTs in parallel, respectively, whereas the size 3 device is a single device. To perform stress tests, only size 3 devices have been used. Indeed, the analysis of stress test results is much more complex for multiple devices of size 1 and size 2.

2.3. Long-term aging stress procedure

Modern SiGe:C HBTs suffer from degradation mechanisms while the device is biased in the safe operating area [Zhan_2002], [Fisc_2015]. Degradation mechanisms are responsible of the wear-out of device performance with time. To characterize device degradation, a long-term stress test procedure has been defined below.

2.3.1. Methodology

To perform the aging tests, stress is applied to the common-emitter test structures. Bias conditions have been chosen at the limit of the SOA. Compared to conventional stress tests, the aging time is considerably increased, several minutes in conventional stress test compared to 1000h for this aging stress test. For the chosen stress conditions, a large aging time is necessary to observe an impact on device electrical characteristics; not accelerated by drastic stress conditions like in conventional stress tests.

To characterize the evolution of the electrical characteristics, measurements have been performed at defined stress times during the aging tests. Due to the long aging time, a logarithm scale is used to define the stress time between each measurement. The aging times are reported in Table 2. The stress time corresponds to the time between each DC characterization and the cumulative aging time to the total time. The aging time is up to 1000h, depending on the evolution of DC characteristics.

Stress time [h]	0	1	2	4	10	7	12	12	24	48	130	250	250	250
Cumulative time [h]	0	1	3	7	17	24	36	48	72	120	250	500	750	1000

Table 2: Stress time and cumulative time used for the first aging campaign

2.3.2. Electrical characterization during aging test

During the stress test, device electrical characteristics evolve according to the stress conditions. To characterize this evolution, different DC measurements are performed. Depending on their physical locations, the damage mechanism can affect one or several electrical characteristics between each stress time. In the following we detail the electrical characteristics measured between each stress time.

2.3.2.1. Forward Gummel plot

Forward Gummel plots are performed by keeping the base and the collector contacts at the same voltage, so as to keep the base-collector voltage at 0V (V_{bc}= 0V), see Figure 15. The base current and the collector current are measured for several values of the base-emitter voltage, V_{be}.

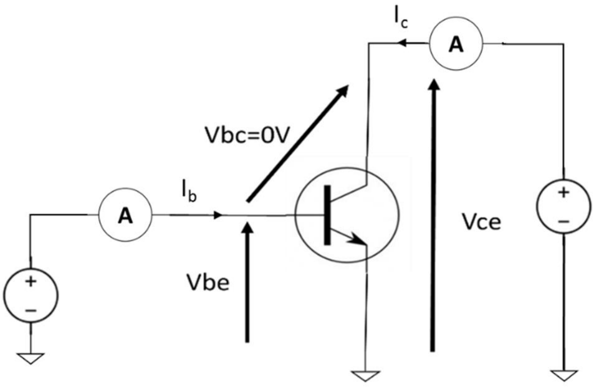


Figure 15: Forward Gummel plot configuration

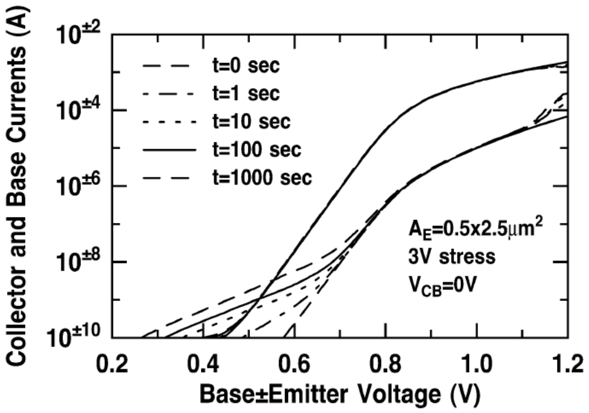


Figure 16: Example of forward Gummel evolution during time of first generation of SiGe:C device aged in reverse stress test. Picture from [Cress_2004].

As reported in literature, i.e.[Cress_2004] (see Figure 16), the forward Gummel plot is affected by the aging test, a reverse stress test in this example. Variations of the forward Gummel plot can be the result of different damage mechanisms, like contact degradation and degradation of the Silicon/Polysilicon interface. The damage can be inferred from the observed modification in the forward Gummel plot. In Figure 16, for example, the increase of the base current at low-injection levels indicates a degradation of the emitter-base spacer interface.

In the forward Gummel measurements in this work, the base-emitter voltage and the collector-emitter voltage are biased at the same bias to keep V_{bc}=0V (V_b=V_c). V_{be} and V_{ce} range between 0.4V to 1V with a step of 7mV while the collector current (I_c) and the base current (I_b) are measured for each step.

2.3.2.2. Reverse Gummel plot

The second electrical characteristics measured at different stress times is the reverse Gummel plot. To measure the reverse Gummel plot, the emitter-base voltage is maintained at 0V, V_{eb}=0V. To obtain this condition, the emitter-collector voltage and the base-collector voltage are kept at the same value, see Figure 17. The emitter current and the base current are measured for different values of the base-collector voltage (V_{bc}). As for the forward Gummel plot, depending on the injection level, the evolution of the reverse Gummel plot during aging tests can provide an indication of the activated ohmic drop damage mechanism. As an example, Figure 18 represents the evolution of the reverse Gummel plot of InP HBTs after a storage test.

Since the SiGe:C HBTs have the emitter and the substrate connected to the ground pad, it’s impossible to realize the configuration describe earlier to perform reverse Gummel plots. To obtain V_{be}=0V, the base voltage is fixed to 0V. A negative collector voltage is applied between 0V and -1V to obtain a positive base-collector voltage. Since the substrate is connected to the ground pad as well as the emitter, this configuration causes a forward biasing of the substrate collector junction. Thus, a substrate current is added to the collector current. However, since during the aging test, the substrate collector junction is reverse biased, the substrate current can be considered constant and thus the emitter-substrate current evolution attributed to base-collector junction.

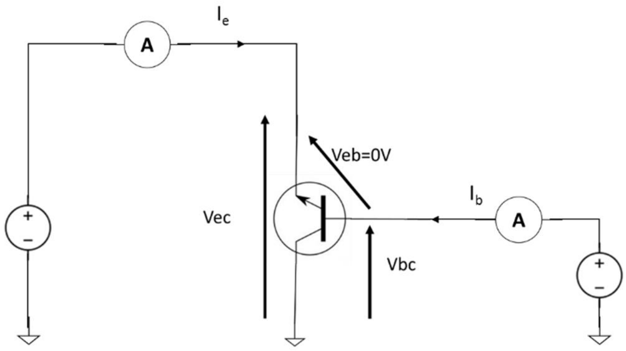


Figure 17: Reverse Gummel plot configuration

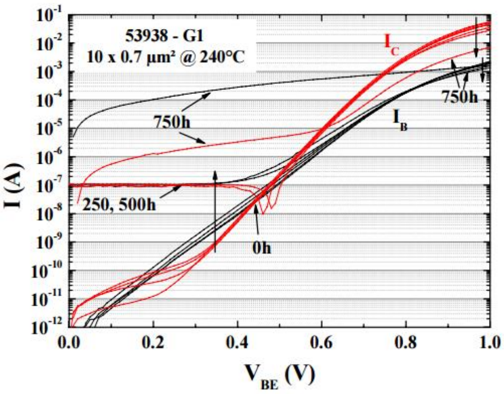


Figure 18: Example of evolution of reverse Gummel plot of InP transistor after storage test @ 240°C. Picture from [Kone_2011]

2.3.2.3. Low-frequency noise measurement

The low-frequency noise measurement at constant V_{ce} and constant base current (I_b) can be also used as a means to characterize the damage mechanisms in the device. As described in [laba_2004], the LF-noise measurement evolution depends on the damage mechanism occurring at the device interfaces. Therefore, the generation-recombination component of low-frequency noise evolution during time indicates a variation of the trapped charge in the device.

Low-frequency noise evolution during the aging time is an additional means to confirm the nature of the damage mechanisms. This behavior is more detailed in the Chapter 3 of this thesis.

2.3.3. Bias conditions

For the first aging campaign, three bias conditions have been chosen. Blue dots in Figure 19 show bias conditions along the limit of the SOA. Since these conditions are close to the SOA edges, the simulated output characteristics with calibrated HICUM model are shown in Figure 19. The first bias conditions P1 has been defined at V_{ce}=1V below the BV_{ceo} (measured at 1.5V) but with a high collector current density J_c=10mA/µm^2 (I_c= 12.91 mA for size 3 HBT). The second bias conditions P3 has been defined for a large collector-emitter voltage V_{ce}=3V, twice the BV_{ceo}. To keep this bias point in the safe operating area, the collector current density is fixed at J_c=1mA/µm^2 (I_c= 1.29mA for size 3 HBT). An intermediate bias conditions P2 is defined between these bias points, V_{ce}=2V and J_c=5mA/µm^2 (I_c= 6.45mA for size 3 HBT).

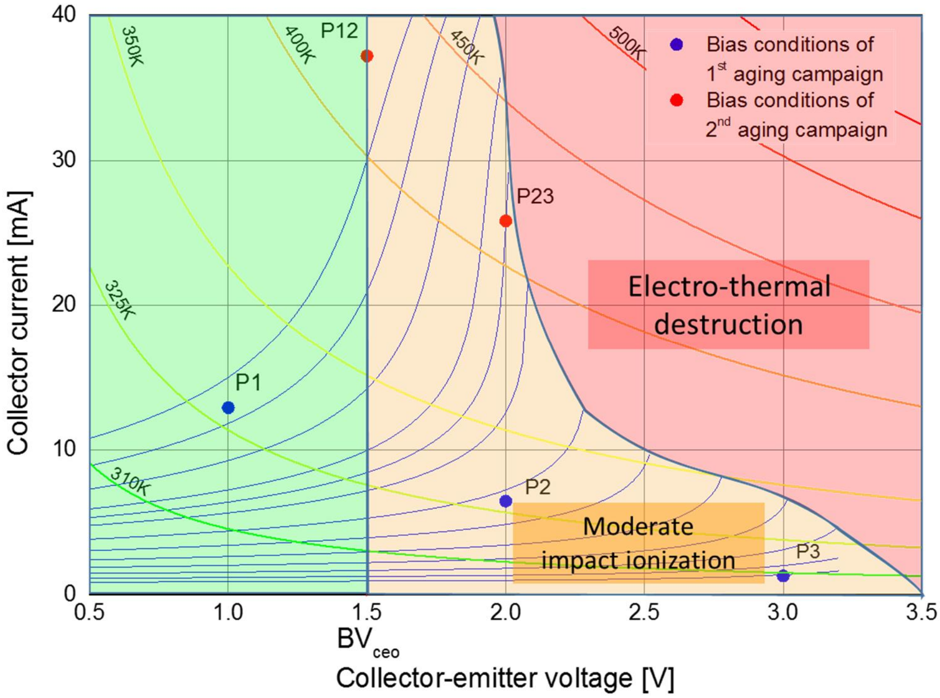


Figure 19: Output characteristics simulated using HICUM level 2 at V_{be} constant between 0.82V and 0.91V (Step of 0.01V) and junction temperature contours for an ambient temperature of 300K. Bias conditions of first (P1, P2 and P3) and second (P12 and P23) aging campaign are reported in the figure with the estimate SOA.

For the first aging campaign, the reliability investigation is focused on the impact of the collector-emitter voltage. Therefore, a second aging campaign has been performed with new bias conditions. The bias conditions of the second aging campaign, red dot in Figure 19, have been chosen to characterize the impact of higher values of collector current density on HBT reliability. The collector-emitter voltage of bias condition P23 is fixed at 2V, as for the P2 bias condition. A higher collector current density is chosen at J_c= 20mA/µm² (I_c= 25.82mA for size 3 HBT). The second bias condition P12 is fixed at V_{ce}=1.5V, between P1 and P2 bias conditions, at the limit of the BV_{ceo}. The collector current density of P12 is fixed at 30mA/µm² (I_c= 37.2mA for size 3 HBT), at the limit of the electro-thermal destruction.

Bias conditions	**V_{ce}**	**I_c**	**T_j**
P1	1V	12.91mA	328,4K
P2	2V	6.45mA	328,4K
P3	3V	1.29mA	308,5K
P23	2V	25.82mA	413,6K
P12	1.5V	37.2mA	422,7K

Table 3: Bias conditions and junction temperature

2.3.4. Aging test campaign configuration

2.3.4.1. First Aging test campaign

The first aging test campaign has been performed on a dedicated test bench. This test bench is composed of 3 identical test supports. Each support hosts 6 devices in the same slot, for a maximum of 18 HBTs on the test bench. Each device can be biased independently in a common-emitter configuration. A photo of the test bench is presented Figure 20.

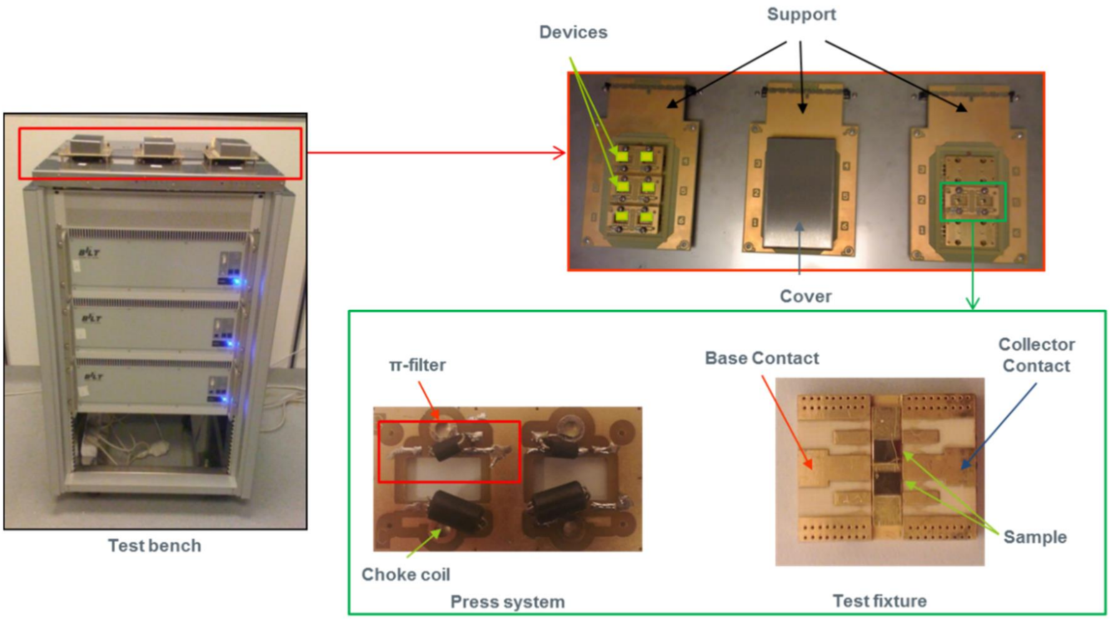


Figure 20: Photography of the dedicated test bench

To apply bias conditions, samples are reported on a specific test fixture. Two samples are reported on one test fixture to optimize the space. The base contact of one device is bonded to one contact of the test fixture, Figure 21. The same process is repeated on the collector side with the other contact of the test fixture.

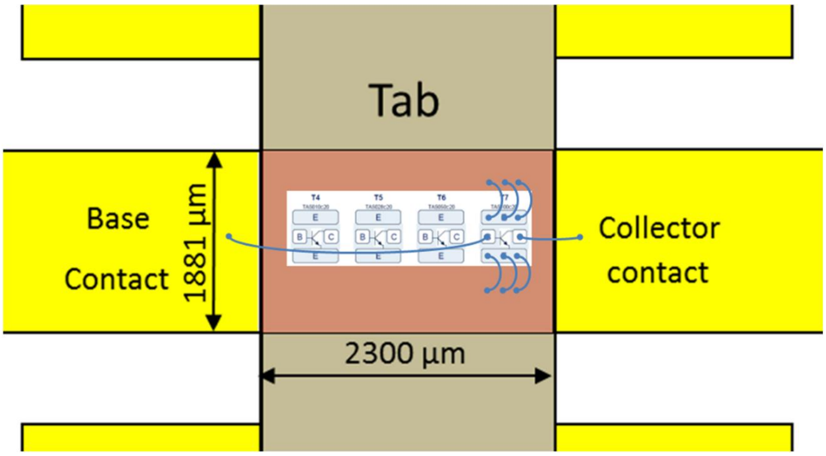


Figure 21 Illustration of test fixture with bounded samples

The emitter has to be grounded. Therefore, the emitter is connected with multiple ball bonding to the test fixture to reduce associated bonding resistance. The report and bonding of die on test fixture have been realized at the IMS lab. During aging test, only one sample is bonded to the test fixture to perform the aging test.

The first measurement performed before the aging test shows parasitic oscillations observed on the forward Gummel plot and the reverse Gummel plot. To avoid these parasitic oscillations, a π-type low-pass filter to the base and a choke coil to the collector have been added in the press system.

A system to perform the aging test at constant collector current and constant collector-emitter voltage is included in the test bench. The collector-emitter voltage is directly applied to the device. The collector current is controlled by adjusting the base current or voltage. Indeed, the test bench includes a feedback loop to control the collector current by adjusting the base current or voltage. The schematic of the whole system is represented Figure 22. This feedback loop is used to the keep the collector current constant during the aging test. It is possible to define a compliance of the base and the collector currents or voltage to avoid the destruction of the device. All these parameters and the aging time are controlled using a computer connected by USB link on the Easy stress software. For the measurement during aging tests a dedicated software, Easy report, is used.

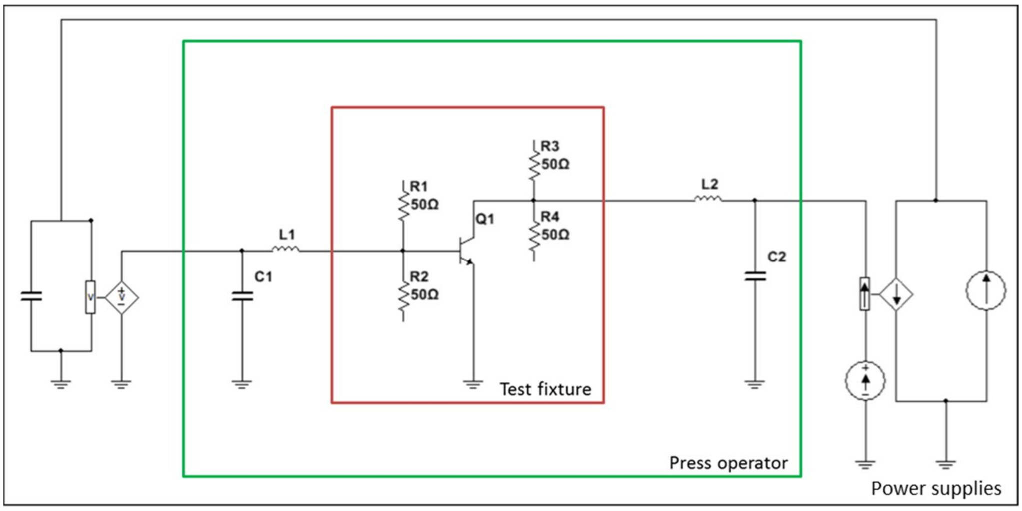


Figure 22: Electrical equivalent circuit of the stress test bench

2.3.4.2. Second aging test campaign

The second aging test campaign has been performed with another measurement setup. For this campaign, the device under test have been aged and measured using a probe station. With this test setup, low-frequency noise measurement could be performed at each step. The measurement setup is used to perform aging test and measurements between each stress time. All the setup is controlled using the IC-CAP software.

To avoid any problem with contacts between each stress test, the aging of the device and measurements have been performed on the same setup without removing the probes. A routine on IC-CAP software has been developed to maintain the collector current constant during the aging test. Every minutes, the collector current has been measured and the base-emitter voltage adapted to keep I_c according to the aging bias conditions.

To characterize the degradation mechanisms, three different measurements have been performed during the aging test. The forward Gummel plot and the reverse Gummel plot have been measured between each stress steps with the methodology described in section 2.3.2.

Thanks to the new measurement setup, the low-frequency noise measurement has been added (which is not possible with the first test setup). Low-frequency noise measurements have been performed at a collector-emitter voltage (V_{ce}) equal to 1V for different base current (I_b) values equal to 0.1µA, 1µA and 10µA.

2.4. The aging test results

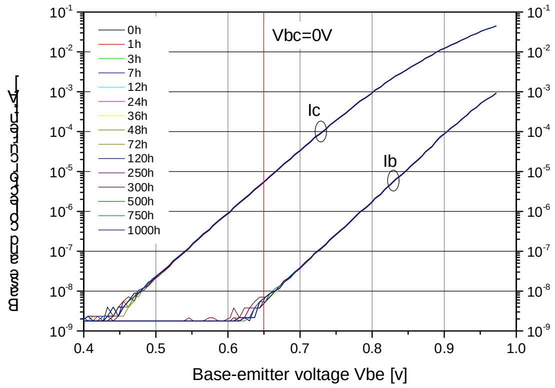
In this part, the evolution of the DC electrical characteristics of the device under test at different aging conditions are reported. Only the forward Gummel plot and reverse Gummel plot results for the first and the second aging campaign are reported. The low-frequency noise evolution during aging test is reported in the chapter 3.

2.4.1. First aging campaign results

For each bias conditions (P1, P2 and P3), 6 devices have been aged at the same time at a controlled ambient temperature equal to 300K. The forward Gummel plot and the reverse Gummel plot are measured at each aging time for each bias conditions.

2.4.1.1. Measurement results under P1 bias conditions

The forward Gummel plot of one device aged under P1 bias conditions is represented Figure 23. For a base-emitter voltage higher than 0.7V, no significant variation of the base current has been reported during the aging stress test. The slight variation of the base current at V_{be}<0.7V has the same order of magnitude as the resolution of the test bench. Therefore, the base current for the forward Gummel plot is almost constant during the aging test. The collector current is also almost constant during the aging test. Also, the base current and the emitter-substrate current of the reverse Gummel plot, Figure 24, are almost constant during the aging test.



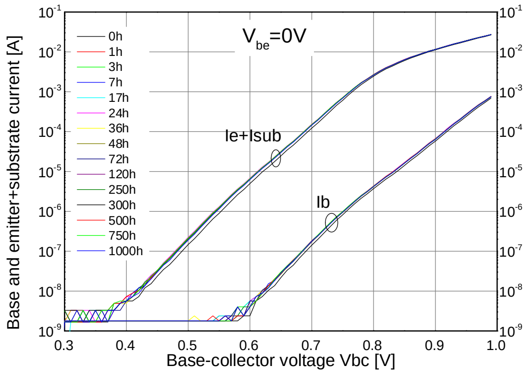


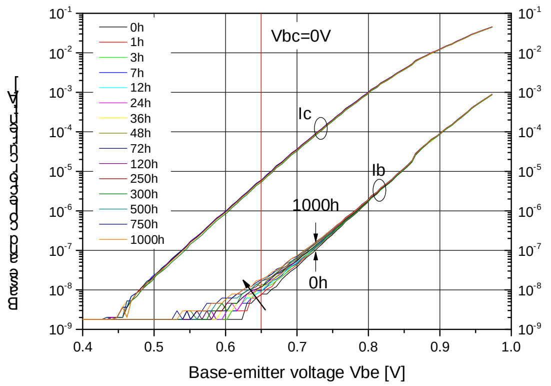
Figure 23: Forward Gummel plot at V_{bc}=0V at different aging times for one device aged under P1 bias conditions

Figure 24: Reverse Gummel plot at V_{be}=0V at different aging times for one device aged under P1 bias conditions

The SiGe:C HBTs aged under P1 bias conditions do not depict any significant variation of their DC electrical characteristics during the aging test. The SiGe:C structure seems not being affected by P1 stress bias conditions.

2.4.1.2. Measurement results under P2 bias conditions

For devices aged under the P2 bias conditions the forward and reverse Gummel plot at different aging times are reported in Figure 25 and Figure 26, respectively. The emitter+substrate current of the reverse Gummel plot, Figure 26, remains almost constant during the aging time. Likewise, the base current is constant or the variation of the base current has the same order of magnitude as the resolution of the test bench.



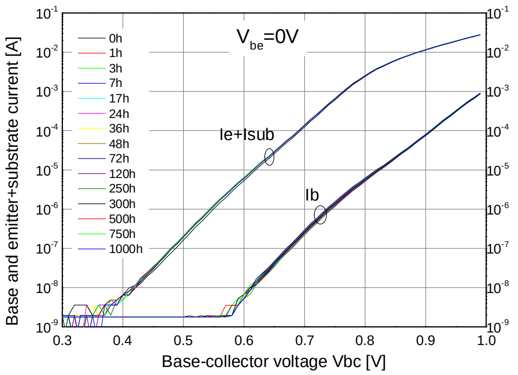


Figure 25: Forward Gummel plot at V_{bc}=0V for different aging times of one device aged under P2 bias conditions

Figure 26: Reverse Gummel plot at V_{be}=0V for different aging times of one device aged under P2 bias conditions

The collector current of the forward Gummel plot, Figure 25, is almost constant during the aging time. Likewise, the base current at V_{be} higher than 0.75V is constant during the aging test. On the contrary, the base current for V_{be} lower than 0.75V tends to increase with the stress time. To characterize the evolution of base current of the forward Gummel plot, the relative variation of the base current $\Delta I_b(t)$, as defined in equation 2.3, is extracted at V_{be}=0.65V.

$$\Delta I_b(t) = \frac{I_b(t) - I_b(0)}{I_b(0)} \tag{2.3}$$

The evolution of the base current as a function of the stress test, for all devices aged under P2 bias conditions, is shown in Figure 27. The ΔI_b of each device aged under P2 present the same evolution as a function of the aging time. The base current increase during the first hours of the stress test seems to reach a saturation value. However, we can note a relative variation of the final constant value of the base current for each device.

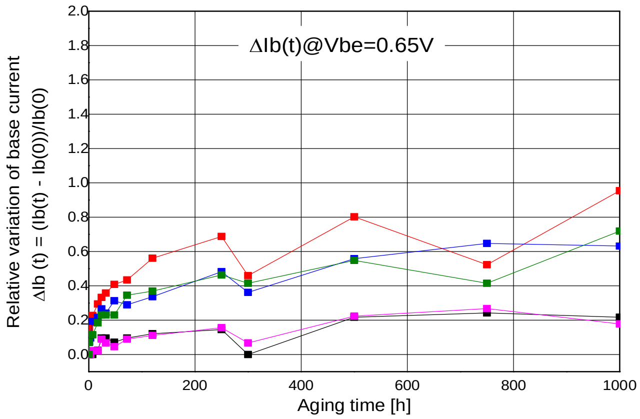


Figure 27: Relative variation of the base current during aging test for device aged under P2 bias conditions at V_{be}=0.65V.

For each device, a systematic decrease of the base current at 300h is observed, Figure 27. For this stress test cycle a delay of 50h has occurred between the end of the stress application and the measurement time. Therefore, the decrease of the base current can be ascribed to natural recovery phenomena. Natural recovery has also been observed for a comparable technology [Sass2_2014] aged under very high-reverse EB stress.

2.4.1.3. Measurement results under P3 bias conditions

Figure 28 represents the forward Gummel plot at V_{bc}=0V for the device aged under P3 bias conditions. The collector current is almost constant or its variation is below the resolution of the test bench during the aging test. For V_{be} higher than 0.7V, the base current does not significantly change. On the contrary, for V_{be} lower than 0.7V, the base current tends to increase with the aging time.

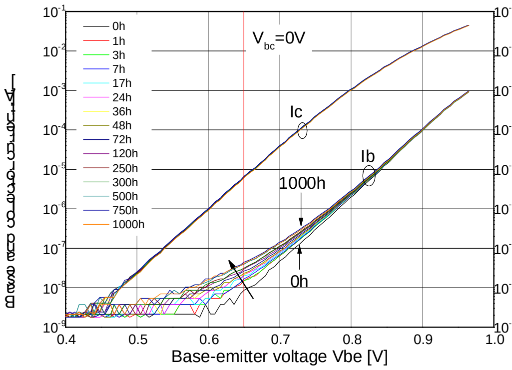


Figure 28: Forward Gummel plot at V_{bc}=0V for one device aged under P3 bias conditions for different aging times

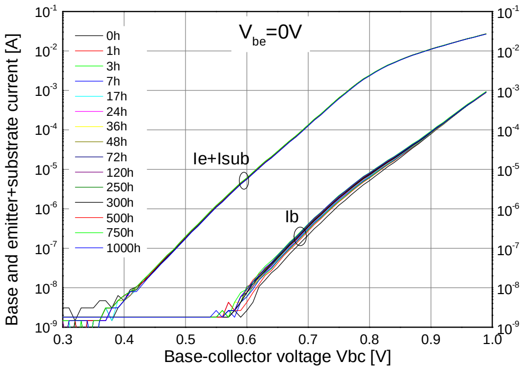


Figure 29: Reverse Gummel plot at V_{be}=0V for one device aged under P3 bias conditions for different aging times

The relative evolution of the base current at V_{be}=0.65V has been reported in Figure 30. The evolution of the base current increase under P3 bias conditions has the same evolution as the base current increase under P2 bias conditions: the base current increases during the first hours of the stress and reaches a saturation value after 700h.

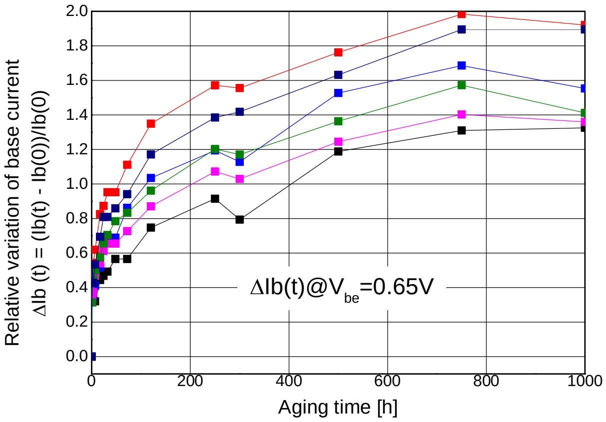


Figure 30: Relative Increased of the base current for devices aged under P3 bias conditions under V_{be}=0.65V as a function of the aging time

The relative variation of the base current at 300h due to natural recovery occurring for the device under P2 bias conditions also occurs for the device aged under P3 bias conditions. For the reverse Gummel plot, Figure 29, the base current and the emitter+substrate current is almost constant during the aging test.

2.4.1.4. Conclusion of the first aging test campaign

During the first aging campaign, 6 devices size 3 per bias conditions have been aged during 1000h. For each device, the forward Gummel plot and the reverse Gummel plot have been measured during the aging test.

The base current and collector currents of the reverse Gummel plot are almost constant for P1, P2 and P3 bias conditions during the aging test. At P1 bias conditions, the electrical characteristics of the device are almost constant during the aging test. Therefore, the reliability of the devices is not impacted by a low collector-emitter voltage and moderate collector current density.

The base current of forward Gummel plot of device aged under P2 and P3 bias conditions tends to increase with the stress time for V_{be} lower than 0.75V. For both bias conditions, the increase of the base current ΔI_b has the same evolution as a function of the aging time. The ΔI_b increases rapidly during the first hours of the aging test eventually reaching a constant value. However, the increase of the base current ΔI_b presents a rate different between device aged under P2 and device aged under P3 bias conditions. Also, the final constant value of the base current relative increase is higher for P3 compared to P2. This difference is probably the result of the higher V_{ce} of P3 bias conditions, V_{ce}=3V compared to V_{ce} of P2 bias conditions, V_{ce}=2V. To conclude, the higher the collector-emitter voltage is, the more rapid is the increase of the base current. The constant value reached by the variation of the base current also increases for higher V_{ce}.

2.4.2. Second aging test campaign

The second aging test campaign has been performed on a different measurement setup. However, the DC characteristics measured during the aging test is the same as the first aging test campaign, forward and reverse Gummel plot.

2.4.2.1. Measurement results under P23 bias conditions

The evolution of the forward Gummel plot of the device aged under P23 bias conditions is depicted in Figure 31. The collector current remains almost constant during the aging test. For V_{be} higher than 0.7V, the base current is constant while the base current tends to increase for V_{be} lower than 0.7V. The variation of the base current at V_{be}=0.65V is compared to the variation of the base current under P2 bias conditions, Figure 32. Since P2 and P23 bias conditions have the same collector-emitter voltage (V_{ce}= 2V) but with a collector current density 4 times higher under P23 compared to P2 bias conditions. The variation of the base current of the forward Gummel plot under P23 bias conditions has the same evolution as the base current under P2 bias conditions. This behavior confirms the impact on reliability of the collector-emitter voltage: a larger V_{ce} yields higher base current evolution.

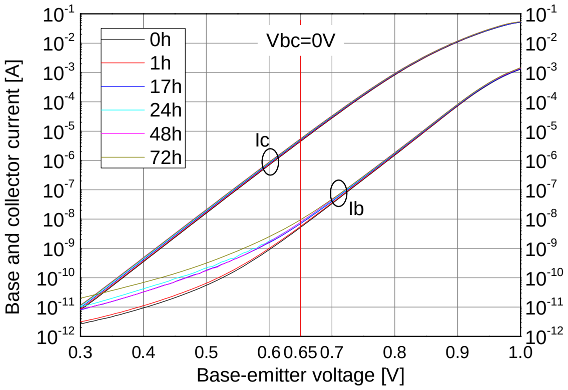


Figure 31: Forward Gummel plot at V_{bc}=0V for a device aging under P23 bias conditions for different aging times

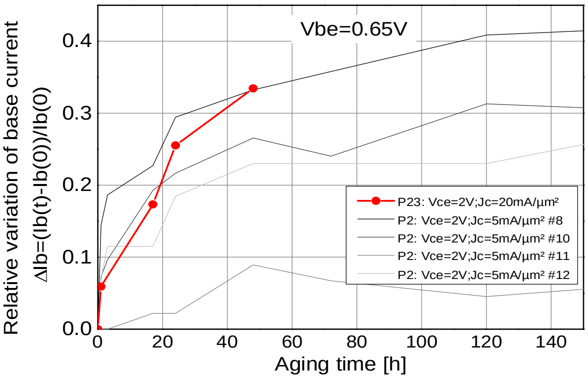


Figure 32: Relative variation of the forward Gummel base current of devices aging under P23 and P2 bias conditions

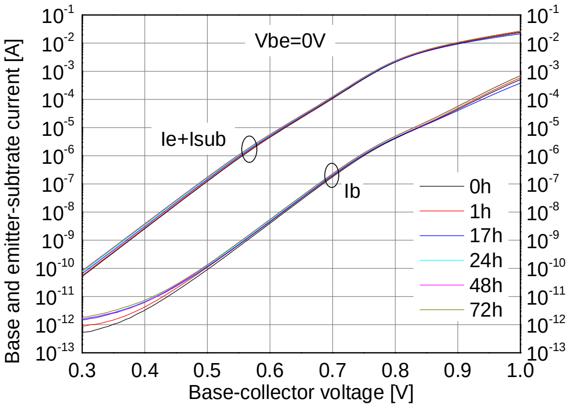


Figure 33: Reverse Gummel plot for a device aging under P23 bias conditions for different aging times

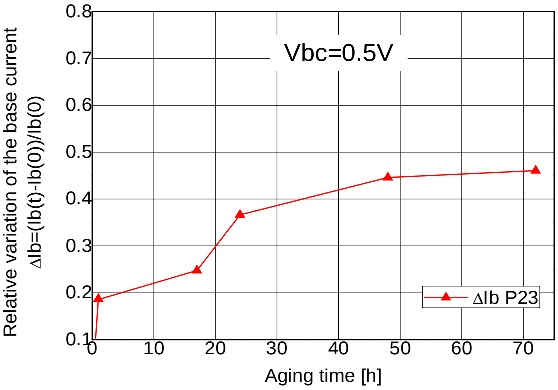


Figure 34: Relative variation of the base current for a device aging under P23 bias conditions for different aging times

The reverse Gummel plot of the device aged under P23 at different aging times is represented in Figure 33. The emitter-substrate current is almost constant during the aging test. The base current at V_{bc} higher than 0.7V is almost constant during the aging test. For V_{bc} lower than 0.7V, the base current tends to increase during the aging test. To analyze this behavior, the relative variation of the base current at V_{bc}=0.5V has been reported in Figure 34. The base current increases during the first 48h of aging to reach a constant value. We can note that the evolution of the reverse Gummel base current is similar to the evolution of forward Gummel plot.

2.4.2.2. Measurement results under P12 bias conditions

One device has been aged under P12 bias conditions, V_{ce}=1.5V and J_c=30mA/µm². During this aging test, the forward Gummel plot and the reverse Gummel plot have been measured and presented in Figure 35 and Figure 37, respectively.

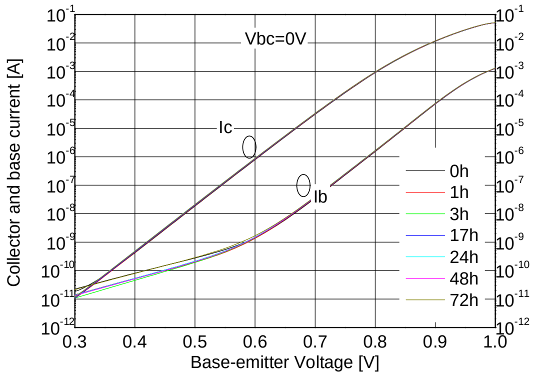


Figure 35: Forward Gummel plot at V_{bc}=0V for a device aged under P12 bias conditions

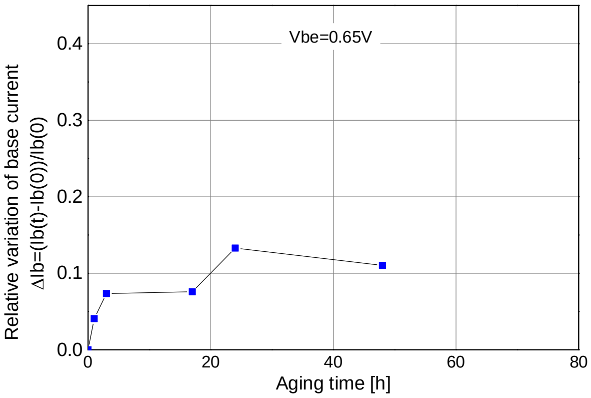


Figure 36 Relative variation of the base current of forward Gummel plot of a device aged under P12 bias conditions

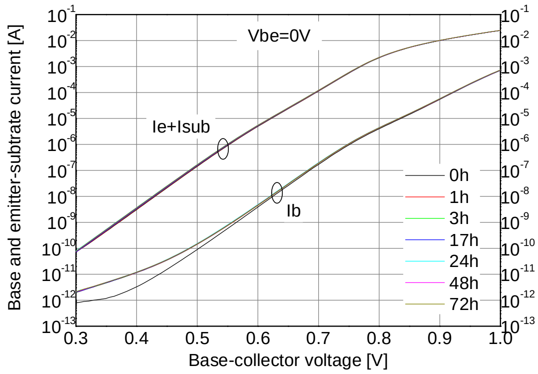


Figure 37: Reverse Gummel plot at V_{be}=0V for a device aged under P12 bias conditions

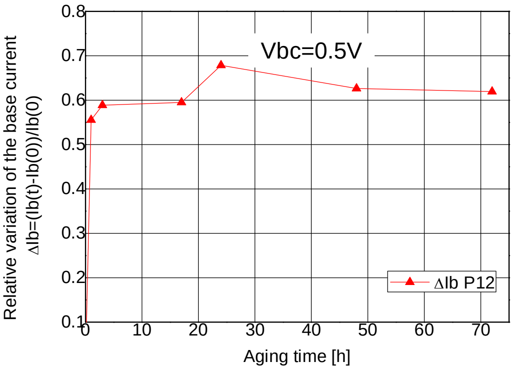


Figure 38: Relative variation of the base current of reverse Gummel plot of a device aged under P12 bias conditions

The collector current and the base current of the forward Gummel plot at V_{bc}=0V are almost constant during the aging test under P12 bias conditions. This slight variation of the base current, Figure 36, could be explained by the low V_{ce} of P12 bias conditions (lower than BV_{ceo}).

The reverse Gummel plot in Figure 37, shows that the emitter+substrate current is almost constant during the aging test. The base current at V_{bc} higher than 0.7V is almost the same during the aging test. Moreover, for V_{bc} lower than 0.7V, the base current increases rapidly after 1h, Figure 38. Subsequently, after 3h, the base current reaches a constant value.

2.4.2.3. Conclusion of the second aging test campaign

An aging test campaign has been performed under P23 and P12 bias conditions during 72h. For the device aged under P23 bias conditions, the base current of the forward Gummel plot increases during the aging test. The variation of the base current has the same evolution as the variation of the one under P2 bias conditions, subject to the same collector-emitter voltage equal to 2V. Indeed, the variation of the base current of the forward Gummel plot is mainly affected by V_{ce} rather than the collector current density.

The base current of the reverse Gummel plot increases during the aging time for both aging tests performed under P23 and P12 bias conditions. The evolution of the base current at low injection seems to be more activated by a high collector current density rather than a high emitter-collector voltage.

2.5. Conclusion

Two aging campaigns have been performed on SiGe:C HBTs manufactured by Infineon Technology AG. Aging tests have been performed on a common-emitter configuration with bias conditions within and without the limits of the Safe Operating Area. The first aging test campaign has been performed under P1, P2 and P3 bias conditions on a dedicated test bench. 6 devices, placed on a support, have been aged for each bias conditions. The forward and reverse Gummel plots are measured during the aging test at defined aging time. The aging stress test and DC measurements have been performed on a dedicated test bench, without moving the samples.

A second aging test has been performed using a probe station. Compared to the first aging stress campaign, only one device is aged at the same time. This aging campaign is performed at two bias conditions P23 and P2. The same DC characteristics as the first aging test have been measured.

The base current of the forward Gummel plot increases with increasing stress time for P2, P3 during the first aging campaign and for P23 bias conditions during the second aging campaign. For these bias conditions, the collector emitter voltage is above the BV_{ceo}. Furthermore, the base current of device aged under P2 and P23 bias conditions, with the same V_{ce}=0.65V, shows the same behavior during the aging test. The base current increases during the first hours of the aging stress test to reach a constant value. The degradation rate and the final constant value depend on the bias conditions, more precisely on the collector-emitter voltage.

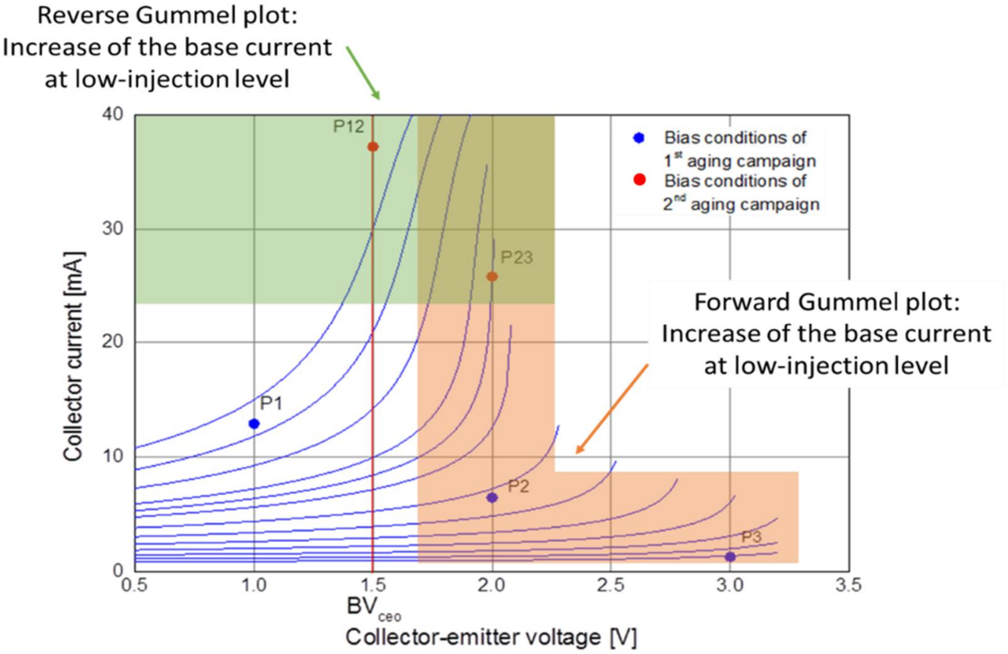


Figure 39 Summary of forward and reverse Gummel plot variation for different bias conditions

Contrary to the first aging campaign, the base current of the reverse Gummel plot increases under P12 and P23 bias conditions. The base current increases under P12 bias conditions and reaches a constant value after 1h. For the device aged under P23 bias conditions, we note a similar relative evolution of the reverse Gummel base current as the forward Gummel base current. The increase of base current of the reverse Gummel plot seems to be activated by the large collector current density.

The aging stress test show an impact on DC characteristics of bias conditions, Figure 39. Large V_{ce} values tend to increase the base current of the forward Gummel plot while the base current of the reverse Gummel plot tends to increase if the device is stressed with a large collector current density.

Chapter 3 Low-frequency noise

Characterization and evolution

3.1. Introduction

The low-frequency noise can be used to characterize the quality and reliability of transistors [Moha_2000]. As described in [Laba_2011], low-frequency noise is sensitive to surface degradation in the device structure and to resistance variation during aging time. With an accurate identification of low-frequency noise sources, it is possible to identify the interface behavior during the aging tests. LF-noise is more sensitive to variations of interface states compared to DC electrical characteristics, and can be used to evaluate trap activity associated with defects in the device.

Different noise sources have been reported in electronics devices. Flicker (*1/f*) noise and thermal noise are fundamental noise sources and are always present in electronic devices. Other noise can be added depending on the quality of the manufactured device and of the type of the device. Unlike the silicon Bipolar Junction Transistor, the noise of SiGe:C HBTs has been dominated by flicker noise and generation-recombination noise originated mostly in the device external surface and periphery [tutt_1995] [cost_1992]. Therefore, this chapter is focused on these two different noise sources.

To use low-frequency noise for reliability characterization, the study of its components and location is mandatory. The different noise sources of SiGe:C HBT will be presented in section 3.2. The low-frequency noise has been measured on HBTs with different size and at different bias conditions. Based on this analysis, the different noise components have been evaluated as a function of the device size and of the bias conditions.

The low-frequency noise during the aging tests is then measured for devices aged under P23 and P12 bias conditions in section 3.3. The evolution of low-frequency noise for these devices during the aging test has been studied. The variation of some low-frequency noise components has been used to determine the damage mechanism origin and the corresponding location.

3.2. Low-frequency noise of SiGe:C HBT

3.2.1. Main noise sources

The noise of SiGe:C HBT has mainly two different noise source, flicker noise and generation-recombination noise (Figure 40). The origin of these low-frequency noise components is detailed below.

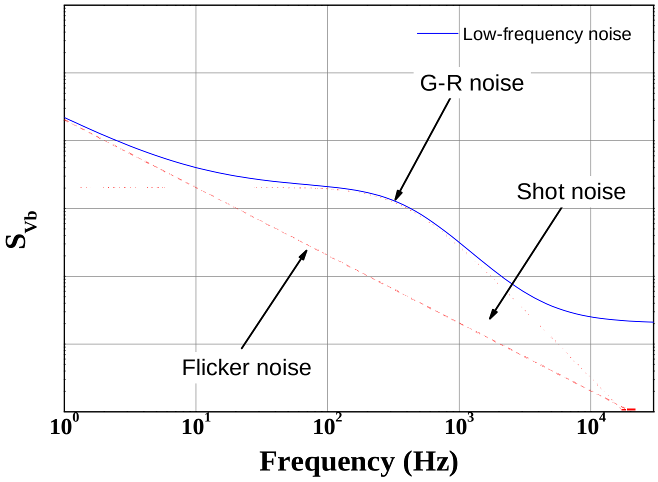


Figure 40: LF noise with main noise source contribution

3.2.1.1. Flicker noise

Flicker noise dominates the low-frequency noise spectrum. The flicker noise is observed in almost every electronic device. The name flicker noise comes from anomalous flicker that was seen in the plate current. It is also called *1/f* noise since the variation of noise spectrum varies as a *1/f* function.

The physical explanation of the *1/f* noise is still debated. One of the possible origin of the flicker noise is the fluctuation in the carrier mobility [Hoog_1969]. Another possible noise source of the *1/f* noise is the imperfection in the device structure [Whor_1955]. Therefore, the flicker noise is still an open topic. This is partly because low-frequency noise can be attributed to a wide range of sources in bipolar transistors and partly because the noise response depends on the spatial location of the source.

3.2.1.2. Generation-recombination noise

Depending on the manufacturing process quality, carriers can be trapped between the valence band and the conduction band, in energy states within the energy band gap.

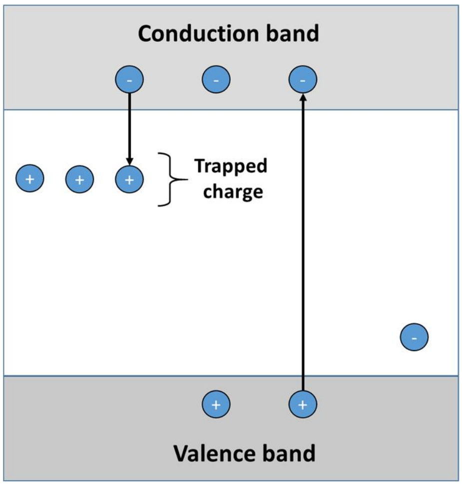


Figure 41: Fluctuation of charge, source of G-R noise

With these extra energy levels, the fluctuation in the number of carriers increases and is associated with random transitions of charges between states in different energy levels, Figure 41. The generation-recombination noise or G-R noise is the result of these transitions between two or more energy levels [sanc_2003]. The generation-recombination noise is enhanced by the presence of trapped charges in the energy band gap at the interfaces of the structure.

3.2.2. Low-frequency noise measurement of the SiGe:C HBT

3.2.2.1. Noise measurement setup

To measure the low-frequency noise, a specific measurement setup (Figure 42) has been used. The setup includes a semiconductor parameter analyzer, a dynamic signal analyzer and a low-noise voltage amplifier. The semiconductor parameter analyzer is used for providing DC bias to the structure. The dynamic signal analyzer measures the voltage noise spectral density of the base and the collector contact. The low-noise voltage amplifier has a gain up to 100dB with a bandwidth of 100KHz and a 1TΩ input impedance. The entire measurement setup is connected through a GPIB interface and controlled with ICCAP software.

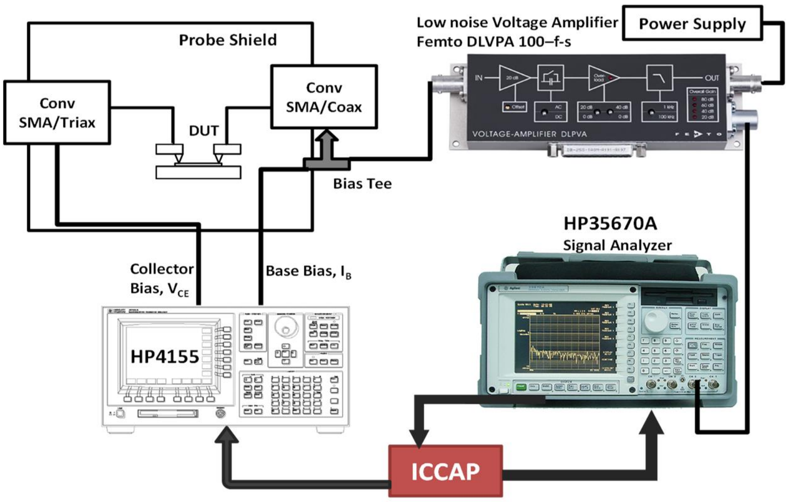


Figure 42 Low-frequency noise setup

3.2.2.2. Low-frequency noise model of SiGe:C HBTs

The low-frequency noise equivalent circuit of the bipolar transistor with noise sources, in the common-emitter configuration is represented in Figure 43 [Jarr_1997] [Bruc_1999]. $V_{Rbn}(t)$, $V_{Ren}(t)$ and $V_{Rcn}(t)$ are the noise voltage sources associated with the base, the emitter and the collector, respectively. $I_{bn}(t)$ and $I_{cn}(t)$ are the noise currents associated with noise fluctuations of the base and collector currents, respectively. LF-Noise is measured with an input base bias resistance R_s in front of the base resistance. For the measurement purpose, the R_s and R_L are the inputs of the DC biasing unit.

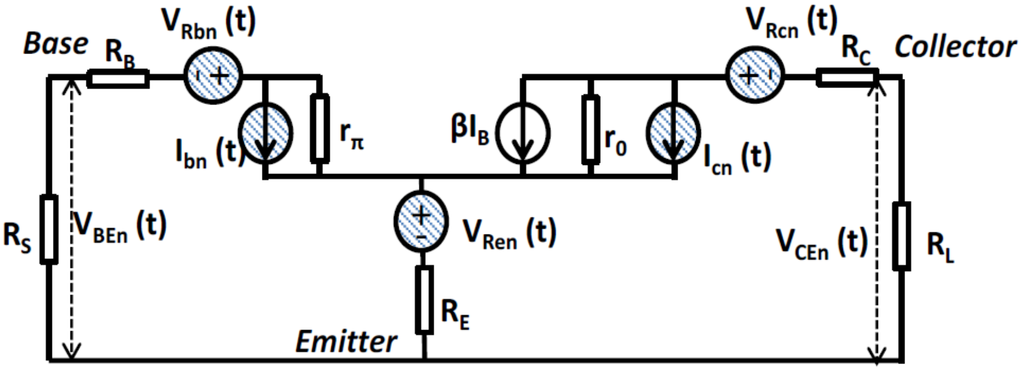


Figure 43 Equivalent circuit of the transistor with noise sources

Besides white noise, noise sources $V_{Rbn}(t)$, $V_{Ren}(t)$, $V_{Rcn}(t)$, $I_{bn}(t)$ and $I_{cn}(t)$ can include excess noise composed of *1/f* and occasionally G-R components. The noise voltage on the base and on the collector can be written as

$$\square_{\square\square\square}\square\square\square = \frac{\square_{\square}}{\square_{\square} + \square_{\square} + \square_{\square} + \square_{\square}\square 1 + \square\square}\square\begin{matrix}\square\dfrac{\square_{\square} + \square_{\square} + \square_{\square}\square 1 + \square\square}{\square_{\square}}\square\,\square_{\square\square\square}\square\square\square + \square_{\square\square\square}\square\square\square - \square_{\square\square\square}(\square)\\ - \square_{\square\square}\square\square\square\square_{\square} + \square_{\square}\square\square + \square_{\square}\square_{\square\square}(\square)\end{matrix}\square \tag{3.1}$$

$$\square_{\square\square\square}\square\square\square = \square_{\square\square\square}\square\square\square - \frac{\square_{\square}}{\square_{\square} + \square_{\square} + \square_{\square} + \square_{\square}\square 1 + \square\square}\square\,\square\square^{\begin{matrix}\square_{\square\square\square}\square\square\square - \square_{\square\square\square}\square\square\square + \square_{\square\square\square}(\square)\\ - \square_{\square\square}(\square)\square\square_{\square} + \square_{\square} + \square_{\square}\square\\ \square\square_{\square} + \square_{\square} + \square_{\square} + \square_{\square}\square\square_{\square\square}(\square)\end{matrix}\square}\square \tag{3.2}$$

The equation 3.3 and 3.4 of the current noise power spectral density (PSDs) S_{Ib} and S_{Ic} are obtained by derivate equation 3.1 and 3.2. These equations are obtaining by converting to frequency domain and considering R_s with a very high value due to the current source.

$$\square_{\square\square} \approx \square\frac{1}{\square_{\square}{}^{2}}\square\,\square\square_{\square\square} + \square\frac{\square_{\square}}{\square_{\square}}\square^{\square}\,\square_{\square\square} + \square_{\square\square\square} + \square_{\square\square\square} + \square\frac{\square_{\square}}{\square_{\square}}\square^{\square}\,\square_{\square\square\square}\square \tag{3.3}$$

$$\square_{\square\square} \approx \square\frac{1}{\square_{\square}{}^{2}}\square\,\square\square^{\square}\square_{\square\square} + \square\frac{\square_{\square} + \square\square_{\square}}{\square_{\square}}\square^{\square}\,\square_{\square\square} + \square^{\square}\,\square\square_{\square\square\square} + \square_{\square\square\square}\square + \square\frac{\square_{\square} + \square\square_{\square}}{\square_{\square}}\square^{\square}\,\square_{\square\square\square}\square \tag{3.4}$$

3.2.2.3. Low-frequency noise measurement

To deeply analyze the low-frequency noise location in the HBT structure, different size and configuration of transistors have been used. The size and configuration of the devices are reported in Figure 44, which includes the device used to perform aging stress tests (grey color).

The low-frequency noise measurement is performed at constant collector-emitter voltage equal to 1V for transistors with different sizes. The low-frequency noise has been measured on different sizes from several dies with the same setup to minimize the process dispersion impact and to locate the noise sources in the structure.

No.	Configuration	Effective Emitter Area [μm^2] $A_{E,eff}=(W_E x l_E)$
1	CBEBC	$0.11x9.93\mu m^2$
2	CBEBC	$0.13x9.93\mu m^2$
3	BEC	$0.13x2.71\mu m^2$
4	BEBC	$0.13x4.91\mu m^2$
5	BEBC	$0.13x9.91\mu m^2$
6	BEBC	$0.17x9.91\mu m^2$
7	BEBC	$0.25x9.91\mu m^2$
8	BEBC	$0.61x9.91\mu m^2$
9	BEBC	$1.11x9.91\mu m^2$
10	BEBC	$1.61x9.91\mu m^2$

Figure 44: Configuration and size of transistor used to investigate LF noise location

An average of 20 voltage noise spectra of the base (S_{vb}) and of the collector (S_{vc}) are measured (in V^2/Hz) for frequency range between 1Hz and 10KHz with the base current ranging between 100nA-10µA. S_{vb} and S_{vc} are converted to base current noise (S_{ib}) and collector current noise (S_{ic}) following equations 3.3 and 3.4.

To compare the noise contributions in different geometries, the noise measurements were carried out at the same base current density for all geometries. The low-frequency noise measurement for the smallest size ($0.13x2.71\mu m^2$) and the largest size ($1.61x9.91\mu m^2$) are reported Figure 45 and Figure 46, respectively.

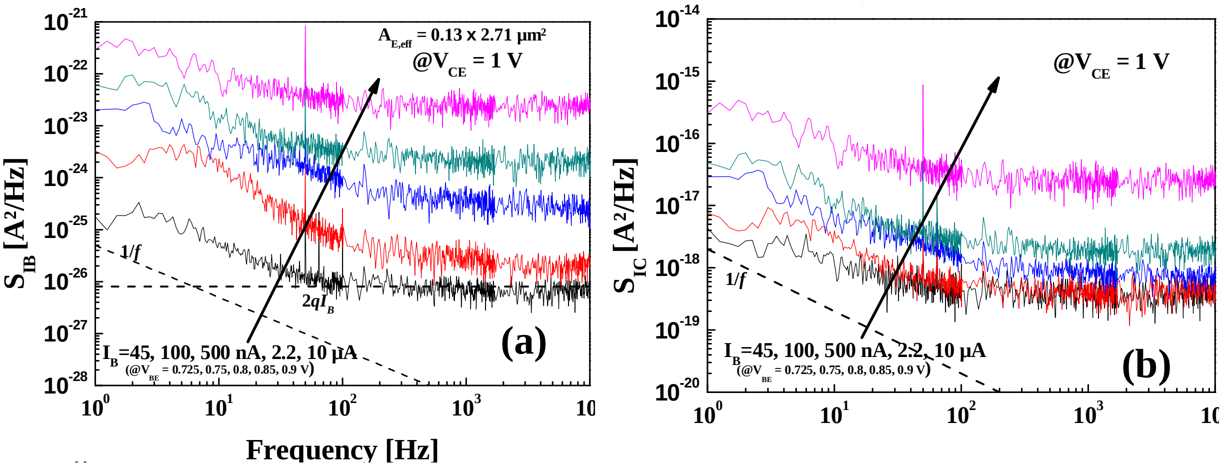


Figure 45: S_{IB} (a) and S_{IC} (b) extracted from the low-frequency measurement of the smallest device size (A_E= 0.13x2.71µm²)

Figure 45 (a) shows the S_{IB} for different V_{be} between 0.725V and 0.9V. The S_{IB} is affected by G-R noise at low base currents although the G-R magnitude diminishes at higher bias. This behavior has already been reported in [sanc_2003]. The low-frequency G-R also affects the S_{IC}, Figure 45 (b). The presence of the G-R noise in both, S_{IC} and S_{IB}, indicates that the source of this noise has probably the same origin, although the G-R noise is less prominent in S_{IC}.

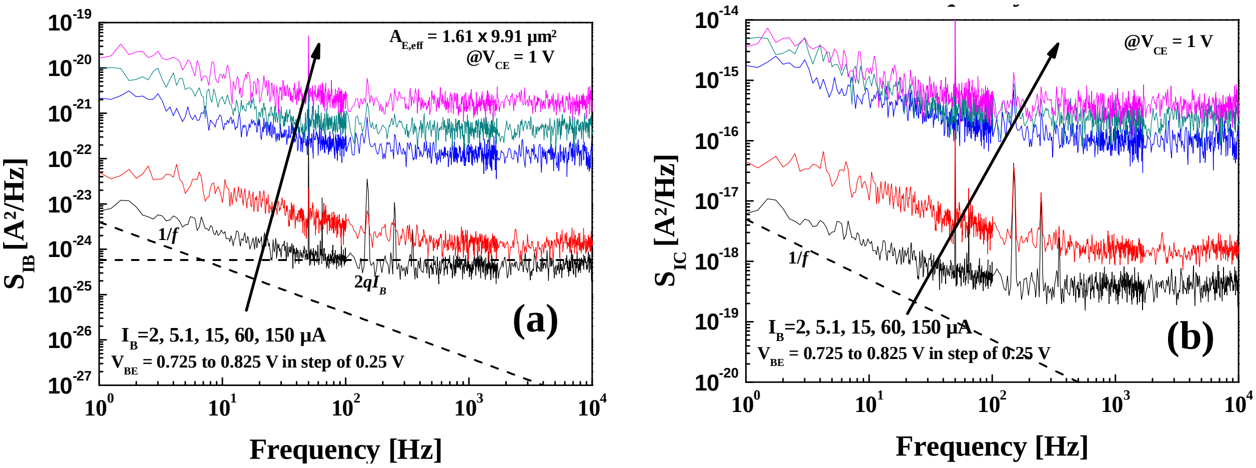


Figure 46 S_{IB} (a) and S_{IC} (b) extracted from the low-frequency measurement of the biggest device size (A_E= 1.61x9.91µm²)

Figure 46 present similar results for the largest device. Contrary to the S_{IB} of the smaller device, the S_{IB} doesn't show any G-R mechanism over the *1/f* noise in the low-frequency range. This indicates that the emitter perimeter/area ($P_{E,eff}/A_{E,eff}$) ratio plays an important role in the noise response. Device with higher $P_{E,eff}/A_{E,eff}$ ratios are more susceptible to the G-R mechanisms activity. The S_{IC} and S_{IB} show similar noise response in Figure 46, (a) and (b). Also, the high-frequency part of S_{IB} shows a higher noise level at higher bias condition compared to $2qI_B$, even though at lower bias we observe a noise level equal to $2qI_B$.

3.2.2.4. Low-frequency noise analysis

To characterize the low-frequency noise, the noise parameters of the conventional SPICE model of S_{IB} have been extracted. The base current noise PSD consists of the *1/f*, G-R and the shot noise components that can be written as

$$\square_{\square\square} = 2\square\square_{\square} + \square_{\square_{\square}}^{\square/\square} + \underset{\square\square\ \square}{\overset{\square}{\square}} \frac{\square_{\square\square,\square}(\square_{\square})}{1 + \square\frac{\square}{\square_{\square,\square}(\square_{\square})}\square^{\square}} \qquad 3.5$$

with

$$\square_{\square_{\square}}^{\frac{\square}{\square}} = \square_{\square}\frac{\square^{\square\,\square}_{\square}}{\square^{\square}} \quad \square$$
$$\square_{\square} = \square_{\square}\square_{\square,\square\square\square} \qquad 3.6$$

Equation 3.5 highlights the different noise sources that will be analyzed in this part. To evaluate the different components of S_{IB}, the SPICE model equation 3.5 is compared with measurements, Figure 47. These results, for one transistor, highlight the individual G-R, shot noise ($2qI_B$) and *1/f* components at low and high bias current.

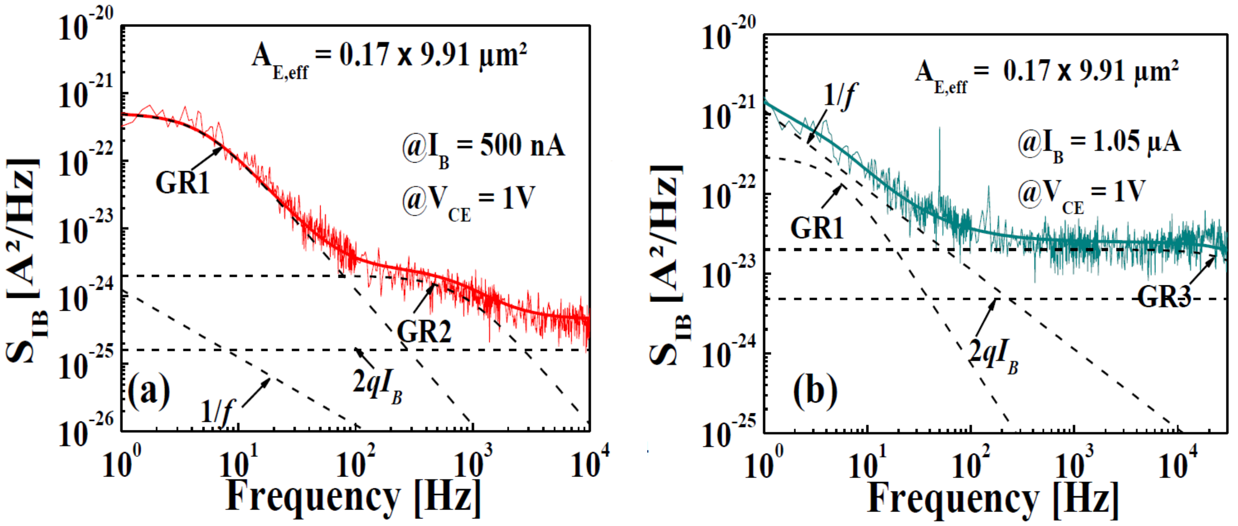


Figure 47 S_{ib} at 500nA (a) and 1.05µA (b) for transistor size 0.17x9.91µm² in comparison with the SPICE model

As clearly observed in Figure 47(a), at 500nA, the *1/f* noise is completely masked by the first G-R component (GR1) visible at low frequency (around 5Hz). There is a second G-R (GR2) component around 500Hz which is less significant compared to GR1. At 1.05µA (Figure 47(b)), the *1/f* noise magnitude becomes larger than GR1 and becomes the dominant noise source. GR2 is not visible at this bias, although a high-frequency G-R (GR3) can be assumed with a cut off frequency around 50kHz. This analysis demonstrates that it is essential to extract the *1/f* noise parameters at a higher bias rather than at low bias where the extraction might lead to erroneous values due to the presence of a dominant G-R, namely GR1.

The individual contributions from the periphery and the intrinsic device can be written as

$$\frac{S_{IB}^{1/f}}{A_{E,eff}} = S_{IA,f}^{1/f} + \left(\frac{P_{E,eff}}{A_{E,eff}}\right) S_{IP,f}^{1/f} \qquad 3.7$$

Here $S_{IA,f}^{1/f}$ and $S_{IP,f}^{1/f}$ are the noise components due to the intrinsic device and the emitter periphery, respectively. $A_{E,eff}$ (=*we·le*) and $P_{E,eff}$ (=*2x(we+le)*) are the effective emitter area and perimeter, respectively. From equation 3.7; it is clear that the intercept and the slope in a plot of $S_{IB,f}^{1/f}/A_{E,eff}$ versus $P_{E,eff}/A_{E,eff}$ provides an estimation of $S_{IA,f}^{1/f}$ and $S_{IP,f}^{1/f}$, respectively.

In Figure 48, the extracted *1/f* component of S_{IB} (normalized with the effective emitter area) is plotted as a function of the perimeter-area ratio at different current densities for the available transistor geometries. At each current density, V_{be} is kept the same value for all transistors. From the linear fit of equation 3.7 in Figure 48, the area and peripheral components are extracted. The component due to the periphery does not evolve with bias, whereas the area component increases with bias and at a higher bias the contribution of the periphery becomes significantly higher. The normalized S_{IB} does not evolve with $P_{E,eff}/A_{E,eff}$ at higher bias and the fit shows almost negligible slope (Figure 48). Hence, the *1/f* noise is dominated by the intrinsic device contribution.

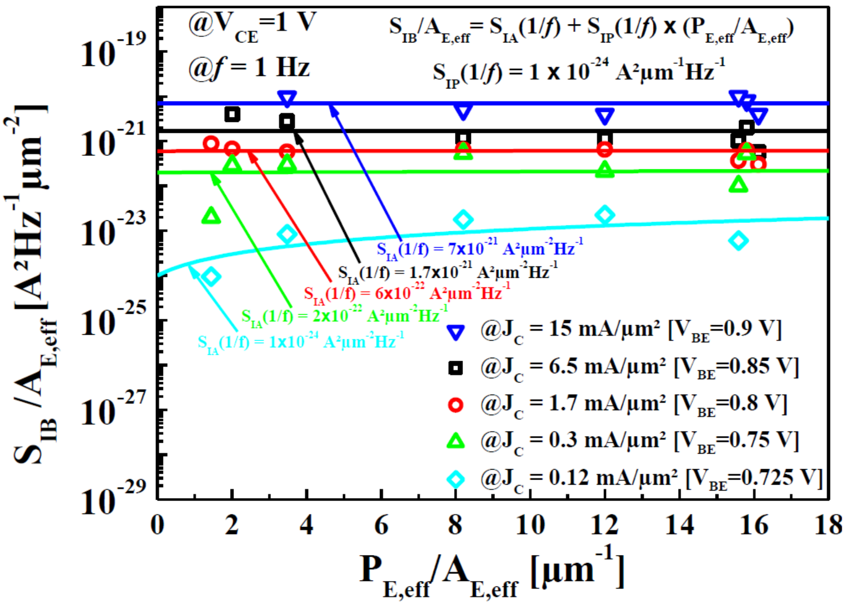


Figure 48 $S_{IB}^{1/f}$ normalized with $A_{E,eff}$ as a function of the perimeter-area ration at different current densities for the available transistor geometries

The same method is used to extract the magnitude of the most significant G-R contribution (GR1). Its normalized magnitude is plotted in Figure 49 as a function of the $P_{E,eff}/A_{E,eff}$ ratio at different current densities, and shows a gradual increase in the magnitude with the ratio. Figure 50 shows the peripheral component for the normalized K_{GR1} at different bias, extracted from Figure 49. The contribution of the periphery remains almost constant with bias. It is obvious from the figure that the periphery component always dominates in case of the peripheral G-R.

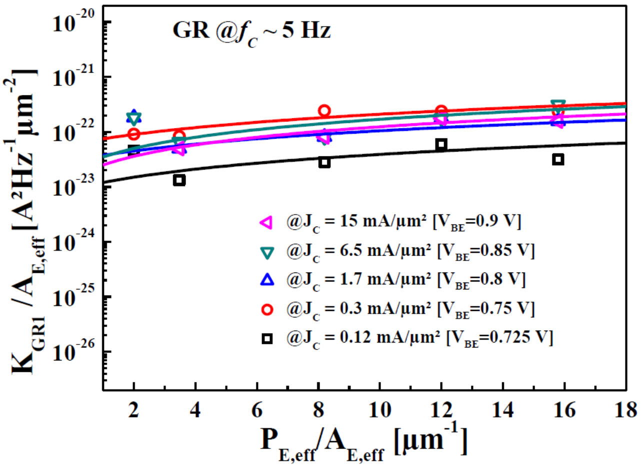


Figure 49 K_{GR1} normalized with $A_{E,eff}$ as a function of the perimeter-area ratio at different current densities for the available transistor geometries

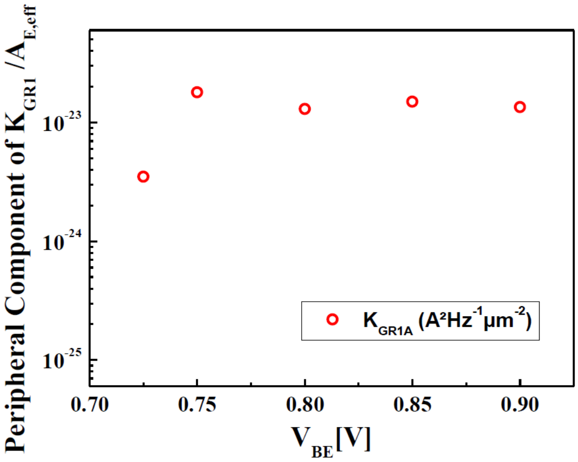


Figure 50 Peripheral component of normalized K_{GR1} at different bias

In Figure 51 (a), the magnitude of the peripheral G-R (GR1) is plotted as a function of I_b. It does not show any significant variation with the current, indicating that the origin of this G-R is from the imperfections in the emitter periphery [Dels_1997]. The magnitudes as well as the cut-off frequencies do not evolve significantly with the bias and the G-R is observed in almost all geometries. At higher bias, the *1/f* component becomes dominant over the G-R magnitude. This is also in line with the findings of Figure 48 where the noise response of the intrinsic device becomes dominant over the peripheral component at higher bias.

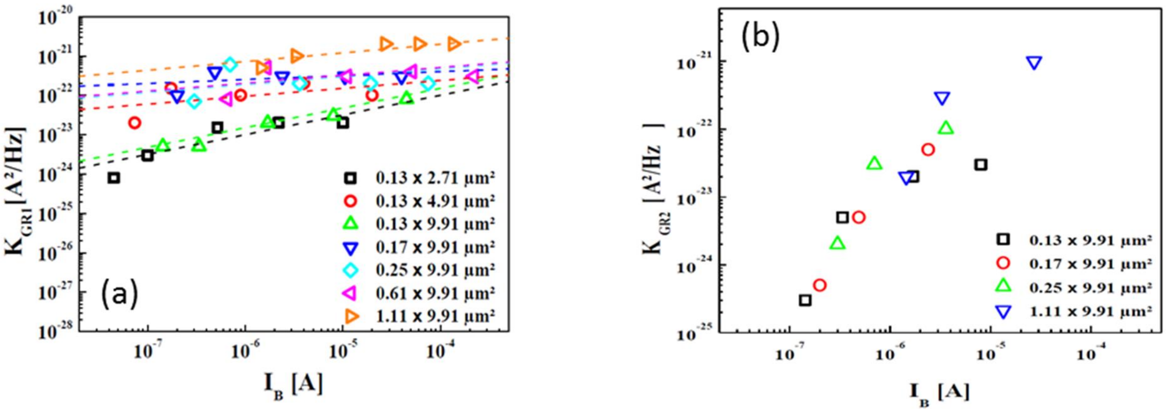


Figure 51: K_{GR1} (a) and K_{GR2} (b) parameter as function of the base current for different device size

The second G-R magnitude (GR2) has been analyzed in the same way, Figure 51 (b). The G-R magnitude evolves as a function of the base current contrary to the peripheral G-R mechanism (GR1). The magnitude of GR2 has possibly originated from the traps in the space charge regions and is not located at the emitter periphery.

3.2.2.5. Coherence function and correlation

Using the low-frequency small-signal equivalent circuit and the extraction methodology, the base $\square\square_{\square}\square$ and collector $\square\square_{\square}\square$ noise power spectral densities (PSD) have been extracted for the available transistor geometries. In addition to the noise current PSDs, the coherent function for different geometries at different bias conditions could be extracted. To extract the coherence, one needs to extract the cross spectral density $\square\square_{\square_{\square}}\square$first. If the base and collector noise current sources, $I_{bn}(t)$ and $I_{cn}(t)$ are partially correlated, they have a non-zero $\square_{\square_{\square}}$ which can be derived following the method presented in [Jarr_1997], using 3.3 and 3.4 as

$$\Gamma_{\square\square} \square \frac{\square\left[\square\square_{\square\square\square} \square \square_{\square\square\square}\square\square \frac{\square_{\square}\square\square_{\square} \square \square\square_{\square}\square}{\square_{\square}^{\square}}\square_{\square\square\square}\right]^{\square} \square \square\square_{\square\square} \square \frac{\square_{\square}\square\square_{\square} \square \square\square_{\square}\square}{\square_{\square}^{\square}}\square_{\square\square}\square}{\square\left[\square_{\square\square} \square \square\frac{\square_{\square}}{\square_{\square}}\square^{\square} \square_{\square\square} \square \square\square_{\square\square\square} \square \square_{\square\square\square} \square \square\frac{\square_{\square}}{\square_{\square}}\square^{\square} \square_{\square\square\square}\right]\square\cdot\square\left[\square^{\square}\square_{\square\square} \square \square\frac{\square_{\square} \square \square\square_{\square}}{\square_{\square}}\square^{\square} \square_{\square\square} \square \square^{\square}\square\square_{\square\square\square} \square \square_{\square\square\square}\square\square \square\frac{\square_{\square} \square \square\square_{\square}}{\square_{\square}}\square^{\square} \square_{\square\square\square}\right]} \qquad 3.8$$

To investigate the contribution of the *1/f* noise component of the base noise at the collector side, an approach is presented here. The component $\square^{2}\square_{\square}^{\square/\square}$ is compared with the S_{IC} in the range of I_b=200nA-10µA in Figure 52. At low bias conditions, S_{IC} is higher in magnitude compared to the contribution of the base noise at the collector, and therefore the measured S_{IC} shows excess noise over the contribution from the base noise at the collector side. This further indicates the existence of an excess noise source at the collector side.

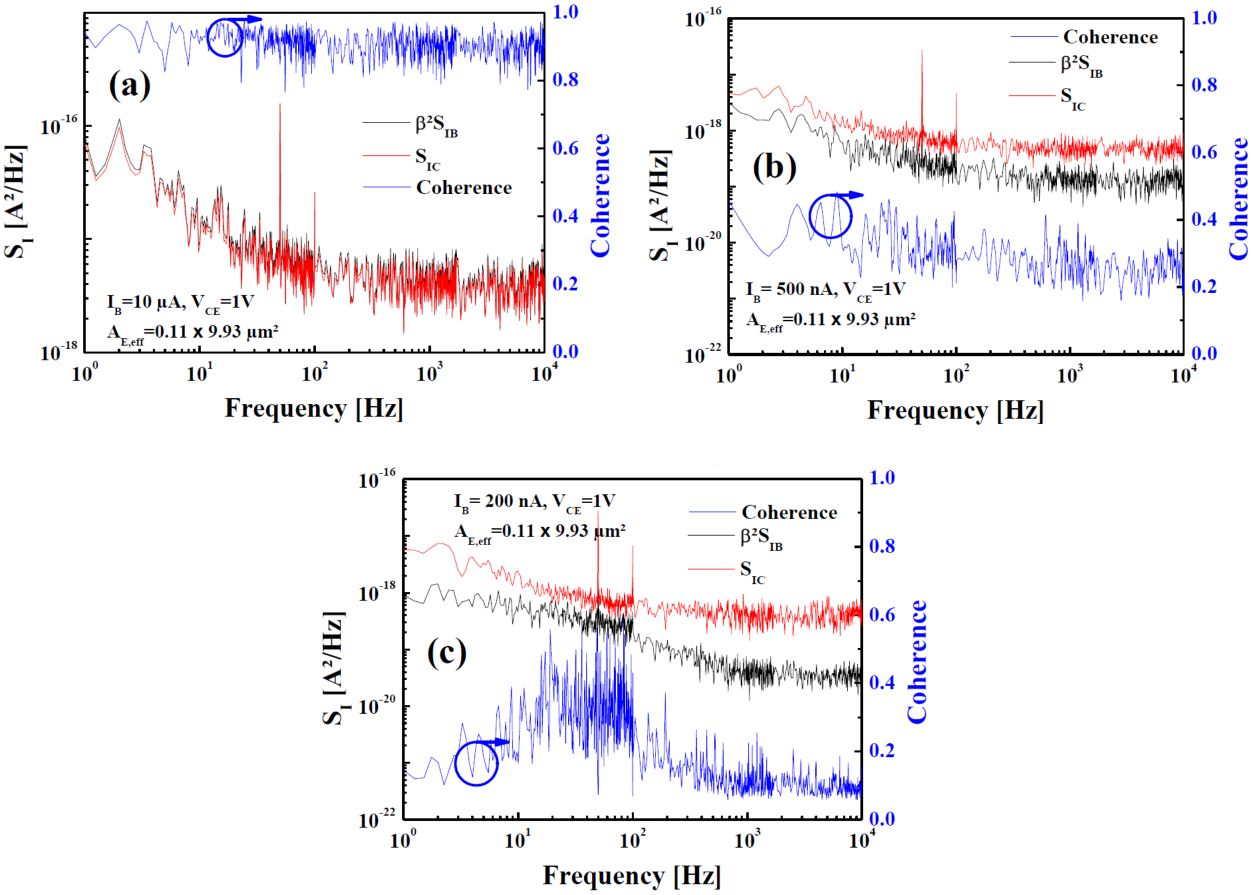


Figure 52 Comparison of S_{IC} and $\beta^2 S_{I_B}$ for different values of I_b, I_b=10µA(a), I_b=500nA(b) and I_b=200nA (c). The corresponding coherence function is also shown in blue at each bias.

The evolution of the base and collector noise correlation at different biases is studied using the coherence function. Using equation 3.8, the coherence between the base and the collector noise sources is extracted for one device size 0.11x9.91µm² and is shown Figure 52. As I_b increases, the coherence starts to approach unity which signifies complete correlation between the base and collector noise sources. At low bias, the coherence is low indicating a partial correlation between the base and the collector noise sources. Therefore, at the collector side, there exists an additional noise source, not correlated with the base noise source, and it is responsible for the higher S_{I_C} over the base contribution at low bias. An increase of the coherence function with I_B is also reported for partially-correlated base and collector noise sources in [Dels_1997].

Figure 53, the coherence function of the transistor device sizes 0.13x2.71µm² and 0.61x9.91µm² are obtained for the same range of V_{be} where the current density remains the same for all transistor geometries. It is interesting to note that the coherence is higher in transistor size 0.61x9.91µm² that has a larger area compared to transistor size 0.13x2.71µm² at the same current density. Also, there is a frequency dependence of the coherence at lower bias, whereas at higher bias, the coherence remains almost independent of frequency.

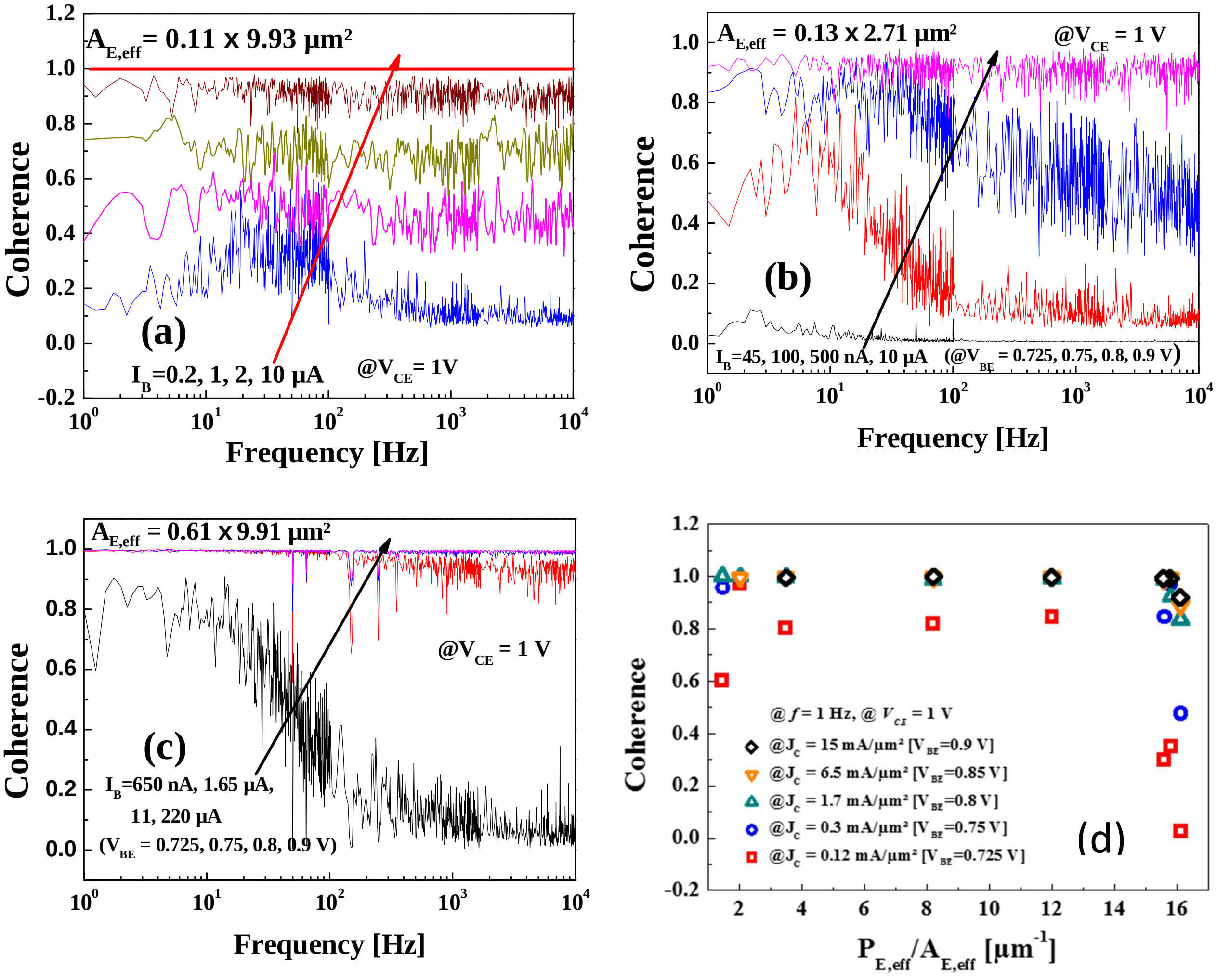


Figure 53 Coherence at different I_B for different device size (a), (b), (c) and function of the perimeter-area ratio (d), for different transistor geometries.

The average value of coherence extracted at a frequency at 1Hz is shown in Figure 53 (d) as a function of the perimeter-area ratio ($P_{E,eff}/A_{E,eff}$). Clearly the coherence is very close to unity at higher bias for all geometries, whereas at lower bias the coherence is less than 1 in smaller geometries (higher $P_{E,eff}/A_{E,eff}$ ratio) compared to the larger ones. Hence, the dominant G-R mechanism is identified as a peripheral mechanism whereas, according to the partial correlation of 1/*f* noise, the 1/*f* noise source is originates in the intrinsic device. This studied of the low-frequency noise has been publish in [muk1_2016] and [muk2_2016].

3.3. Evolution of low-frequency noise during aging tests

In chapter 2, the evolution of base current for the forward and reverse Gummel plot are reported for the device aged under P23 bias condition. For device aged under P12 bias condition, only an increase of the base current of reverse Gummel plot is reported.

An evolution of low-frequency noise occurring during aging test can be the result of device interface degradation, according to [Laba_2011]. Therefore, he evolution of the low-frequency noise during aging stress test is presented in this section.

3.3.1. Measurement conditions

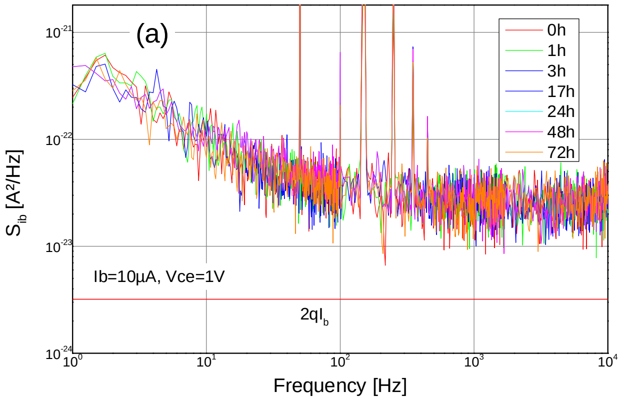
The low-frequency noise has been measured at different aging times during the aging tests performed under P23 and P12 bias conditions. The S_{ib} and S_{ic} have been evaluated for base current equal to 0.1µA, 1µA and 10µA and V_{ce} equal to 1V. The low-bias condition of the device aged under P12 bias condition is almost constant during the aging test for the different base currents.

The low-bias conditions of device aged under P12 bias condition provide no significant evolution of the low-frequency noise during the aging test for the different base currents. Therefore, the study of the low-frequency noise is focused on the evolution of the low-frequency of device aged under P23 bias condition.

3.3.2. Low-frequency noise under P23 bias condition

3.3.2.1. Measurements results

For the SiGe:C HBT submitted to P23 bias conditions, the low-frequency noise is represented Figure 54. At I_b equal to 10µA and 1µA, Figure 54 (a)(b), the low-frequency noise is almost constant during the aging time. On the contrary, the LF-noise at I_b=0.1µA, Figure 54 (c), presents variations during the aging time. To understand this behavior, an analysis of LF-noise at I_b=0.1µA has been performed.



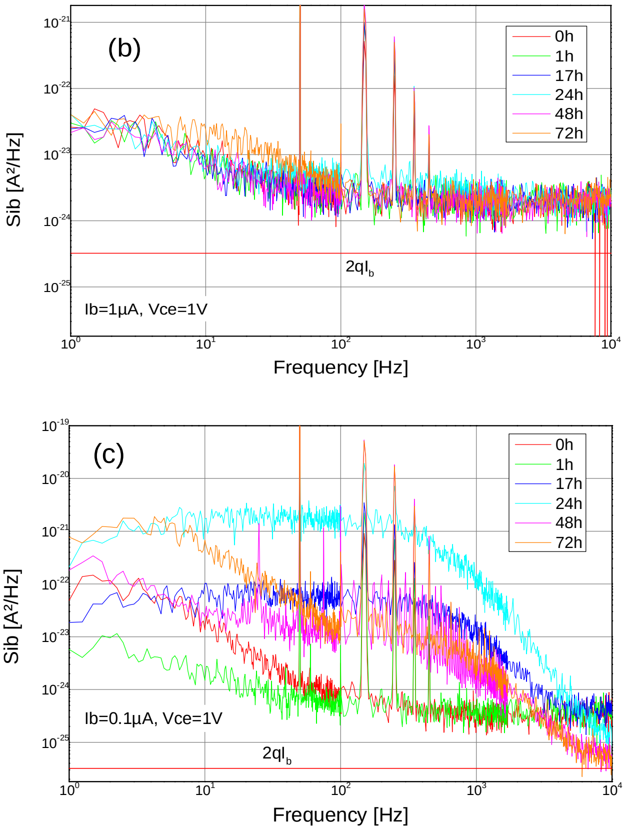


Figure 54 Evolution of the low-frequency noise for base current at base current equal to 10µA (a), 1µA (b) and 0.1µA (c).

3.3.2.2. Characterization of the low-frequency noise at I_b=0.1µA

The characterization the low-frequency noise is realized on the noise voltage PSD using equation 3.9 with $K_{GR,i}$, the amplitude and the $f_{c,i}$, the cut-off frequency of the G-R noises. This equation is based on equation 3.5 used to analyze the noise current PSD in the previous section. To evaluate the evolution of the noise during the aging tests, the parameters of G-R noise have been extracted at each stress test time.

$$S_{Vb} = K_{t_k}^{1/f} + \sum_{i=1}^{n} \frac{K_{GR,i}(t_k)}{1 + \left(\frac{f}{f_{c,i}(t_k)}\right)^2} \qquad 3.9$$

Figure 55 represents the LF-noise at I_b=0.1µA measured at different aging times together with the evaluated LF-noise resulting from equation 3.9. At the initial time (0h), S_{Vb} is dominated by GR1 noise with an amplitude K_{GR1} of 3×10^{-13} V²/Hz and a cut-off frequency f_{c1} of 5Hz. After 1h, the K_{GR1} falls to 2×10^{-13} V²/Hz. This decrease of K_{GR1} parameter could be explained as follows:

- At the initial step of the aging tests, the activity of the traps associated with defects is observed through the K_{GR1} parameter high value.

- Then, an annealing of the corresponding defects due to the structure biasing, natural recovery and/or temperature recovery in the device during the aging tests, could explain the decrease of K_{GR1}.

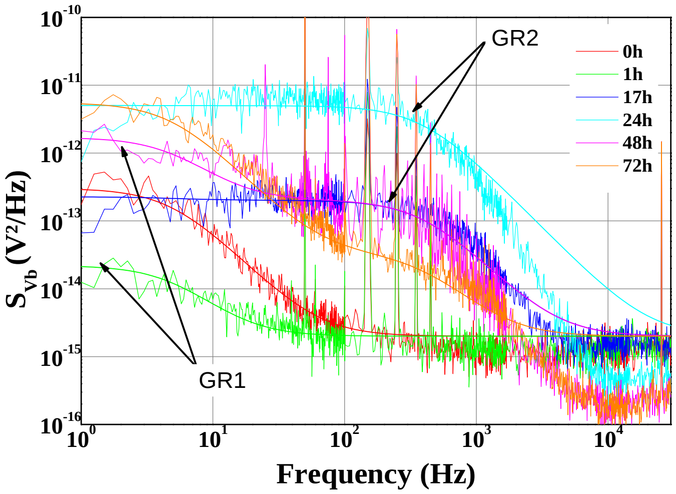


Figure 55: Low-noise measurement at V_{ce}=1V; I_b=0.1µA at different aging times

After 17h and 24h, the GR2 noise dominates the LF-noise, therefore, it's not possible to extract the GR1 noise parameter. The K_{GR2} parameter increases to 2×10^{-13} V²/Hz after 17h and reaches 5×10^{-13} V²/Hz after 24h. After 48h, the K_{GR2} parameter of GR2 noise goes down to 2×10^{-13} V²/Hz when the GR1 amplitude is equal to 1.5×10^{-12} V²/Hz. At 72h, GR1 continues to increase whereas GR2 decreased to 3×10^{-14} V²/Hz. The evolution of the K_{GR1} parameter of GR1 with a cut off frequency at 5Hz and K_{GR2} parameter of GR2 with a cut-off frequency at 500Hz are reported as a function of the aging time Figure 56 (a) and (b), respectively.

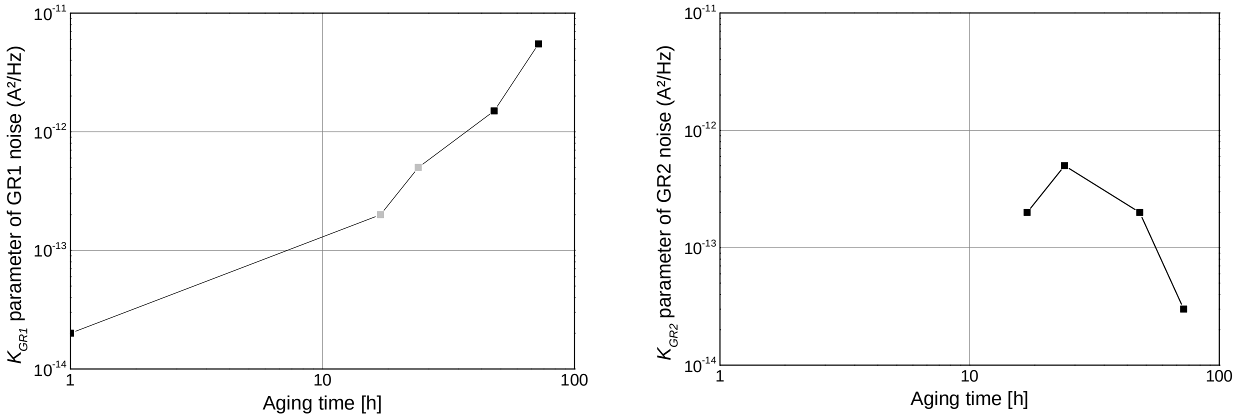


Figure 56 Evolution of GR1 noise (a) and GR2 noise (b) amplitude as a function of the aging time

The K_{GR1} parameter of GR1 tends to increase with the aging time. The amplitude of the GR2 noise K_{GR2} increases rapidly until 24h before decreasing with the aging time. At 17h and 24h, K_{GR2} dominate the LF noise. Therefore, the value of K_{GR1} is arbitrarily fixed at the K_{GR2} value, corresponding to the maximum possible value for K_{GR1} represented by grey points in Figure 56 (a). These variations of K_{GR1} parameter of GR1 and K_{GR2} parameter of GR2 could be the result of the degradation in the device. More precisely, the G-R components of the noise are attributed to trap activity at device interface (see section 3.2).

3.3.2.3. Device damage mechanisms

The variation of the forward Gummel plot seems to be correlated to LF noise variation. Indeed, the forward Gummel plot of device aged under P12 bias conditions is almost unchanged during the aging test time. The low-frequency noise evolution is also no significant during aging time.

To further analyze the evolution of low-frequency noise for the device aged at P23 bias condition, the Figure 57(a) has been elaborated. Figure 57(a) shows the forward Gummel plot at different V_{bc} values corresponding to the low-frequency noise bias conditions. Additionally, this figure points out the base current associated with the low-frequency noise according to DC bias conditions. Comparing Figure 57(a) and the evolution of the base current for the forward Gummel plot, Figure 57(b), during aging tests:

- the base current for mid and high injection level remains almost constant Figure 57 (b). Equally the LF noise measured at these level of injection, V_{ce}=1V;I_b=1µA and V_{ce}=1V;I_b=10µA, remains constant during the aging tests (Figure 54(a)(b)).
- an increase of the base current for the forward Gummel plot is observed at low-injection level (I_b=0.1µA), Figure 57 (b). For the LF noise evolution evaluated at I_b=0.1µA, Figure54(c), an evolution is also reported.

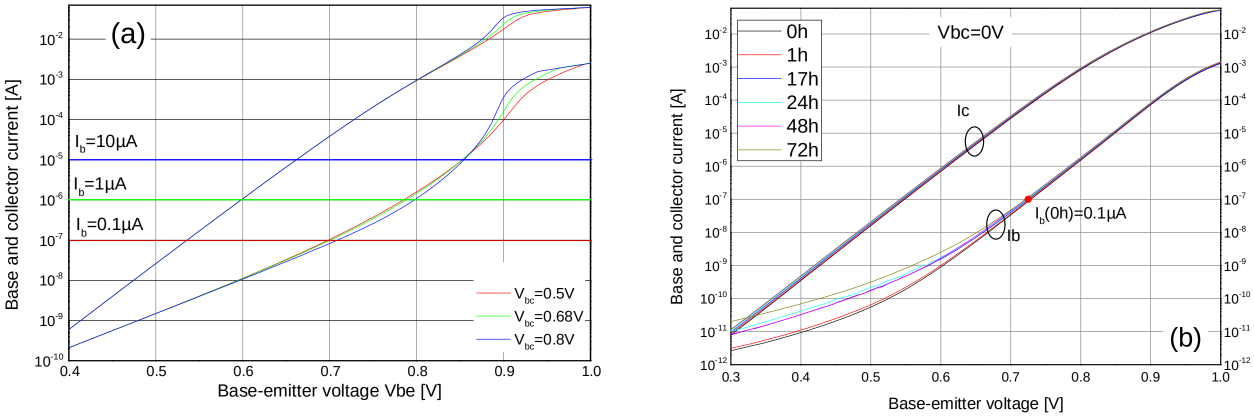


Figure 57 Forward Gummel plot with LF noise bias condition (a) and for device aged under P23 bias condition (b)

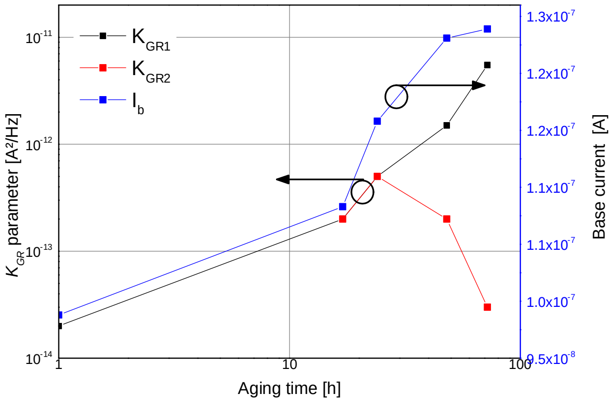


Figure 58: Comparison of the evolution of GR parameters and the base current function of the aging time

Figure 58 represents the evolution of the GR1 and GR2 amplitude together with the base current as a function of the aging time for V_{be} constant chosen to obtain I_b=0.1µA at initial time (0h). The evolution of the variation of the base current corresponds to the evolution of the sum of the equivalent variation of K_{GR1} plus K_{GR2} parameter.

This similar evolution of low frequency noise and of the forward Gummel base current confirms that the forward Gummel base current variation at a low-injection level is the result of trap activity in the structure. However, the exact location of trap density cannot be determined using these results.

3.4. Conclusion

The low-frequency noise of SiGe:C HBTs has been analyzed and the physical origin and location of noise sources have been identified. Based on this study, a noise law in HiCuM model has been proposed in [muk1_2016] [muk2_2016]. In the framework of this thesis, we have demonstrated that the low-frequency noise measurement could also be used as a reliability characterization mean.

Indeed, the low-frequency noise has been measured for devices aged under two different bias conditions until 72h at I_b equal to 0.1µA, 1µA and 10µA. The low frequency noise of the device biased under the P12 bias condition is shown to present no significant evolution during aging test time, as well as the DC characteristics. For the device aged under the P23 bias condition, the LF noise at I_b equal to 1µA and 10µA is shown to present no significant evolution, whereas a variation is reported for LF-noise measured at I_b=0.1µA. Hence the variation of the G-R component of the LF noise has the same source as the evolution of the forward Gummel base current.

This correlation between variation of forward Gummel base current and low frequency noise can be explained by the creation of trap density in the device. The increase of trap density in the device has an impact on the G-R component as well as on the low injection base current observed on the Gummel plot. The exact location of degraded interface and the damage mechanism origin are difficult to extract from these results. To get a deeper insight into this origin a physical simulation of the device has been performed and is detailed Chapter 4.

Chapter 4 Physical simulation

damage mechanism origins

4.1. Introduction

4.1.1. Hydrodynamic model for SiGe:C structure

To better understand the damage caused by damage mechanism activation, physical TCAD simulations of the SiGe:C HBTs under test have been undertaken. To perform these simulations, the hydrodynamic model developed during the DOTSEVEN project, with optimized parameters reported in [Sass_2010], has been used. As described in [Sass_2010], the density of states (DOS), carrier saturation velocity and high-field mobility for energy transport/hydrodynamic (ET/HD) simulations models have been improved to accurately describe SiGe:C HBT specificity, based on experiment results and Monte Carlo results [Jung_2000].

4.1.1.1. Density of states model

The effective density of states model (Nc: associated with conduction band, Nv: associated with valence band) plays an important role in collector current computation. The effective DOS for silicon-germanium and silicon is simplified by [Huet_1996] to obtain equation 4.1.

$$(N_C N_V)_{SiGe}/(N_C N_V)_{Si} \approx 0.4 \qquad 4.1$$

However, this constant ratio does not take into account a different critical dependence. A more accurate model for holes effective DOS, equation 4.2 has been proposed in [Sass_2010]. This model of holes effective DOS, takes into account the Ge mole fraction and lattice temperature dependences,

$$\square_{\square\_\square\square_{\square\square\square}\square\square_{\square}}(\square\square_{\square},\square\square) = \square_{\square\_\square\square}(\square\square_{\square})\cdot\frac{\square_{\square\square}+\square_{\square\square}\cdot\square\square\square\left(\frac{\Delta\square_{\square}\cdot\square}{\square_{\square}\cdot\square_{\square}}\right)}{\square_{\square\square}+\square_{\square\square}} \quad 4.2$$

Based on equation 4.2 and the splitting schematic view in [Prin_1989], the electron effective DOS equation proposed is

$$\square_{\square\_\square\square_{\square\square\square}\square\square_{\square}}(\square\square_{\square},\square\square) = \square_{\square\_\square\square}(\square\square_{\square})\cdot\frac{\square_{\square\square}+\square_{\square\square}\cdot\square\square\square\left(\frac{\Delta\square_{\square\square}\cdot\square}{\square_{\square}\cdot\square_{\square}}\right)+\square_{\square\square}\cdot\square\square\square\left(\frac{\Delta\square_{\square\square}\cdot\square}{\square_{\square}\cdot\square_{\square}}\right)}{\square_{\square\square}+\square_{\square\square}+\square_{\square\square}\cdot\square\square\square\left(\frac{\Delta\square_{\square\square}}{\square_{\square}\cdot\square_{\square}}\right)} \quad 4.3$$

Parameters of equation 4.2 and 4.3 have been calibrated to match the SiGe:C HBT studied in this thesis.

4.1.1.2. Carrier saturation velocity model

Carrier saturation velocity generally plays a significant role at high injection level. Carrier saturation velocity has been described by [Ersh_1994] as a function of the Ge mole fraction. With [Quay_2000], the lattice temperature influence could be added to the model. These models neglect the dependence upon the doping level. The model developed during DOTSEVEN project, presented in [Sass_2010], accounts for this effect. The model equations 4.4, 4.5 include the dependency of the carrier saturation velocity upon lattice temperature, Ge mole fraction and doping (N).

$$\square\square\square,\square_{\square}\square = \frac{\square_{\square\square\square}\square\square\,\square}{1-\square\cdot\square 1-\square\square_{\square}/\square_{\square}\square^{\square}\square} \quad 4.4$$

$$\square_{\square\square\square}\square\square\,\square = \square_{\square}\cdot\square\square/\square_{\square\square\square}\square^{\square} \quad 4.5$$

The dependence upon Ge mole fraction is given by

$$\square_{\square\square\square\square} = \square_{\square\square}\cdot\square 1-\square_{\square}\square+\square_{\square\square_{\square.\square}\square\square_{\square.\square}}\cdot\square_{\square}+\square 1-\square_{\square}^{\square}\square\cdot\square_{\square}^{\square}\cdot\square_{\square} \quad 4.6$$

where C_V is a bowing factor.

4.1.1.3. High-field mobility model

The use of energy-transport and hydrodynamic (HD) models is mandatory, in order to capture nonlocal effects due to downscaling of the device. In the presence of a strong electric field, the electrons gain energy and their temperature is highly increased [Gras_2003]. The carrier temperature gradient introduces an additional driving force and in TCAD HD simulations the electric field is replaced by an effective driving force, [TCAD_manual]. [Sass_2010] proposed a model taking into account the specificity of modern SiGe:C devices. This model offers a new analytical high-field formulation accounting for lattice temperature, carrier temperature, doping values and mole fraction. The complete model is described by equations 4.7 to 4.11.

$$\square = \sqrt{\max(\square_{\square}-\square_{\square},0)/(\square_{\square}\cdot\square\cdot\square_{\square\square\square})} \quad 4.7$$

$$\square_{\square\,\square\square\,\square} = \square_{\square\square\,\square} / \square\square 1 + \square\square/\square_{\square}\square^{\square}\square \cdot \square 1 + \square\square\square \cdot \square_{\square\square\,\square} / \square_{\square\square\square}\square\square^{\square}\square^{\square/\square}\square \qquad 4.8$$

$$\square = \square_{\square} + \square_{\square} \cdot \log_{\square\square}\square 1 + \square_{\square}\square + \square\square_{\square} \cdot \log_{\square\square}\square\square/\square_{\square\square\square}\square\square^{\square_{\square}} \qquad 4.9$$

$$\propto = \propto_{\square} - \propto_{\square} \cdot \log_{\square\square}(1 + \square_{\square}) \qquad 4.10$$

$$\square_{\square} = \frac{\square_{\square}}{\square_{\square}} \cdot \square\square\square\square\square_{\square\square} - \square_{\square\square} \cdot \log_{\square\square}(\square/\square_{\square\square\square})\square \qquad 4.11$$

4.1.2. Physical simulation purpose

The variation of SiGe:C HBT electrical characteristics and low-frequency noise have been reported and analyzed for devices aged at different bias conditions in chapter 2 and chapter 3, respectively. The evolution of device electrical characteristics indicates damage mechanism activation. The evolution of low-frequency noise of device aged under P23 bias condition tends to indicates degradation due to some trap density in the device. In this chapter, physical simulation results are used to understand the damage mechanisms and the damage resulting from its activation.

To investigate the origin of damage mechanisms, physical simulations are focused on the forward and reverse Gummel plot evolution. Trap density distributions have been added in SiGe:C structure to evaluate the DC electrical characteristic variation. To perform this simulation, a good agreement between measurements performed before the aging test, and the simulated DC characteristics is requested. Hence the calibration of TCAD simulation for a fresh device is described in section 4.2.

Based on this calibrated simulation, an additional trap density has been added in the SiGe:C HBT. Depending on trap location, the evolution (or not) of device electrical characteristics are observed. Based on these results, the variation of DC electrical characteristics has been attributed to a specific degradation effect in the structure and characterized in section 4.3.

4.2. Calibration of TCAD simulation

4.2.1. HD model

Simulations were performed using a calibrated hydrodynamic model and calibrated transport parameters for Sentaurus TCAD as described in section 4.1.1. The calibrated hydrodynamic model parameters are chosen according to the scaling level and no additional fitting was considered. Calibrated transport models for Sentaurus TCAD were developed during the *DOTFIVE* project for SiGe:C based on different results, i.e. experimental results and Monte Carlo simulation.

In addition to these models, equations included in Sentaurus TCAD have been activated to account for the specificity of measurement context. These models description and calibration are detailed below.

4.2.2. 2D structure

Physical simulations can be performed on a 2D or 3D structure. For the aging simulation, the thermal behavior is not taken account. Indeed, only DC electrical characteristics of the device have been simulated. For this measurement, junction temperature is estimated constant and reasonably low (see value of chapter 1). Therefore, a 2D structure is used for our simulation.

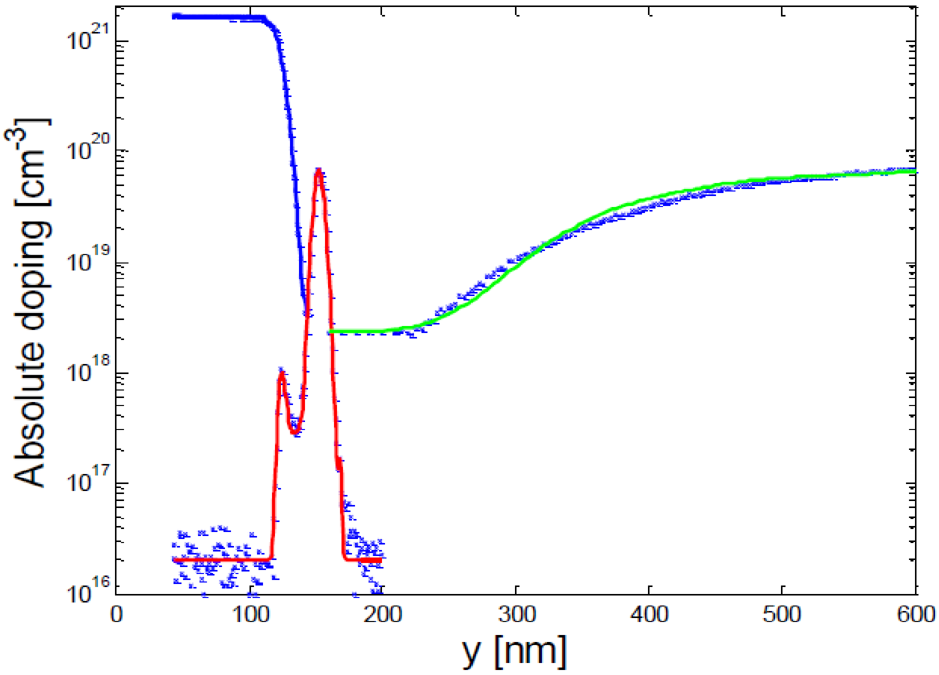


Figure 59 Doping profile from SIMS (blue cross) and doping profile of TCAD structure for arsenic emitter region (blue line), boron base region (red line) and arsenic collector region (green line).

To draw the 2D structure, dimension and doping profile information, from Secondary Ion Mass Spectrometry (SIMS) measurement, have been provided by Infineon technology AG for a BEC structure of the same technology node, Figure 59. Based on these information, a half device structure is draw, Figure 60. Only a half structure is chosen due to the symmetry of the CBEBC configuration of the device. The doping profile has been adjusted, Figure 59, according to the sensitivity of SIMS measurement. The simulated forward Gummel plot is depicted in Figure 61.

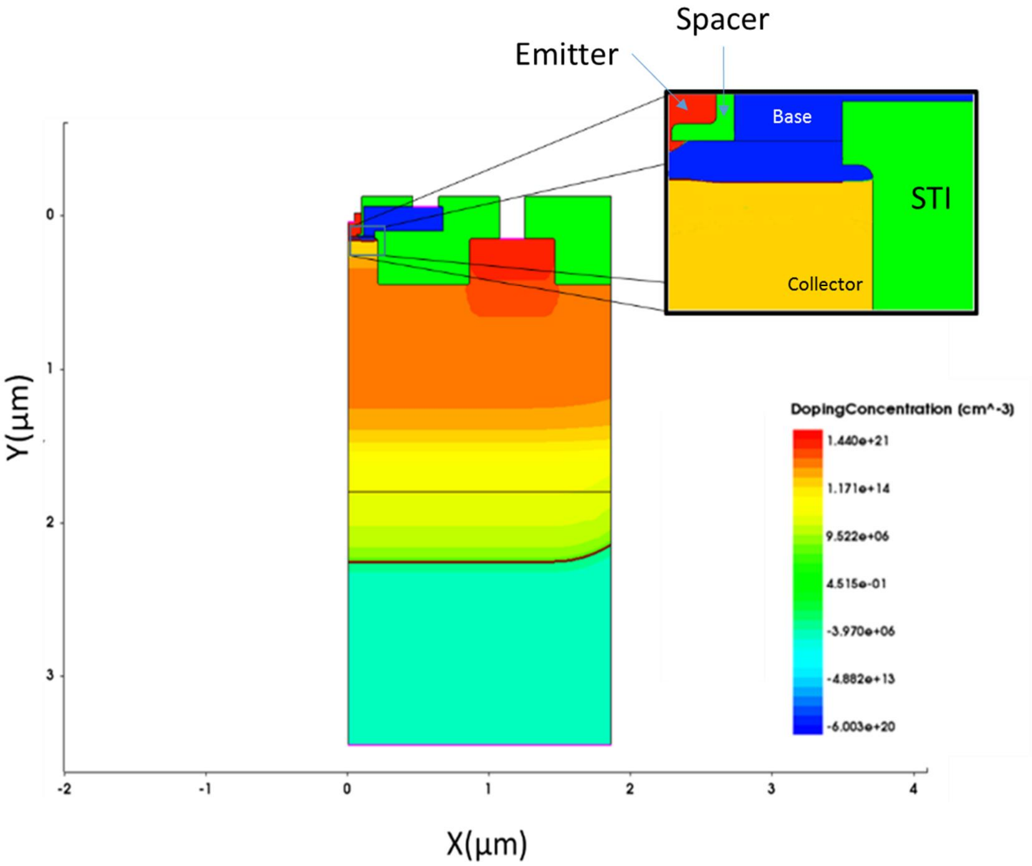


Figure 60: Representation of the half structure

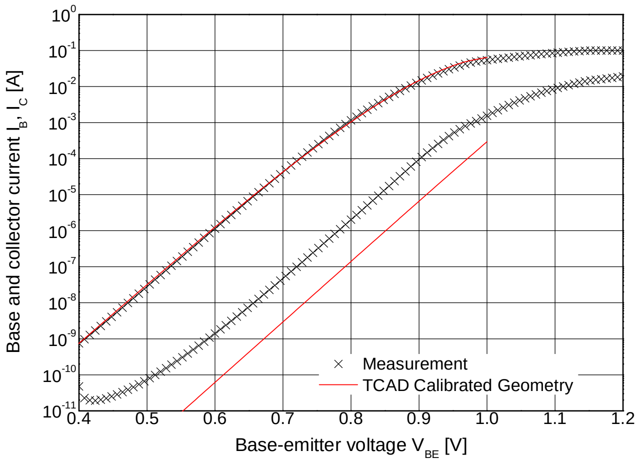


Figure 61: Gummel plot @ V_{cb}=0V. Comparison between measurement and simulation result with calibrated structure

Figure 61 shows a good agreement between measurement and simulation for the collector current of the forward Gummel plot. The simulated forward Gummel base current is lower than the measured one. To achieve a better agreement of the base current, some additional models of Sentaurus TCAD have been activated and calibrated.

4.2.3. Model calibration

4.2.3.1. TCAD model enable

A good agreement of the simulated and measured base current of the forward Gummel plot can be obtained by activating default Sentaurus TCAD models. According to [Paas1_2001], Auger recombination has a very significant role in highly doped base. The Auger recombination model has been activated and a calibration of parameters has been performed.

A second model in Sentaurus software has been activated, Shockley Read Hall (SRH) recombination. The SRH recombination plays also an important role in highly doped SiGe:C HBT. Like Auger recombination, SRH recombination has been calibrated for the SiGe:C structure.

4.2.3.2. Auger recombination: mid-injection level

The Auger recombination affects the mid-injection level of the base current. According to [TCAD_manual], Auger recombination is defined by equation 4.12 and 4.13. To calibrate the base current, equation 4.2 is used; more precisely parameter $A_{A,n}$ associated with the temperature independency.

$$R_{net}^{A} = (C_n n + C_p p)(np - n_{i,eff}^{2}) \quad 4.12$$

$$C_n(T) = \left(A_{A,n} + B_{A,n}\left(\frac{T}{T_0}\right) + C_{A,n}\left(\frac{T}{T_0}\right)^{2}\right)\left[1 + H_n \exp\left(-\frac{n}{N_{0,n}}\right)\right] \quad 4.13$$

Hence the $A_{A,n}$ coefficient of the equation 4.13 has been change according to the literature [Laks_1990], [Niu_1998]. The $A_{A,n}$ coefficient has been set to 1.5x10^{-29} cm^{6}s^{-1} for electrons and to 7.0x10^{-32} cm^{6}s^{-1} for holes Figure 62.

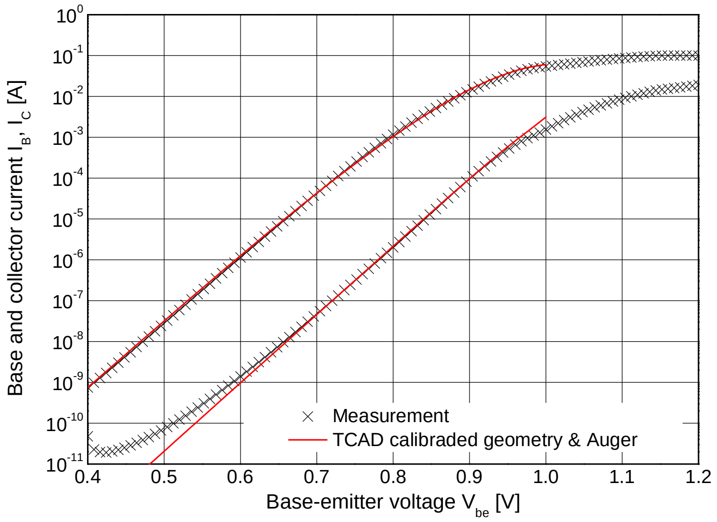


Figure 62: Gummel plot @ V_{cb}=0V. Comparison between measurements and simulation including Auger recombination model.

Between V_{be} equal to 0.65V and 0.95V, the simulated base current fits well with measurements. We can note that the collector current is not impacted by the modification of the Auger recombination parameter.

4.2.3.3. SRH recombination: Base current at low injection level

The base current at low injection levels is dominated by Shockley Read Hall (SRH) recombination. Different SRH models are available in the TCAD software. Only the SRH recombination models with high-field enhancement and doping dependence have been activated, which are non-local models. Default parameters of the high-field enhancement models are kept. The SRH doping dependence model, equation 4.14, has been calibrated.

$$\tau_{dop}\left(N_{A,0}+N_{D,0}\right)=\tau_{min}+\frac{\tau_{max}-\tau_{min}}{1+\left(\frac{N_{A,0}+N_{D,0}}{N_{ref}}\right)^{\gamma}} \qquad 4.14$$

The calibration of the SRH doping dependence is obtained by changing the N_{ref} parameter of equation 4.14. The default value of N_{ref} parameter is adjusted for Si bipolar transistor [Foss_1983] and depends on the device type. The N_{ref} parameter has been increased to $1.0 \cdot 10^{18}$ cm^{-3} instead of $1.0 \cdot 10^{16}$ cm^{-3} (default value) to fit the base current at low injection level.

To take into account resistive effects at very high-injection levels, a base contact resistance of R_{BS}=3.295 KΩ (2.55 KΩ/sq.) has been added. This resistance has the same order of magnitude as the contact resistance of a *DOTFIVE* device, estimate at 2.7 KΩ/sq. [Chev_2011]. The simulated forward and reverse Gummel plots are compared with on-wafer measurements in Figure 63 (a) and (b), respectively.

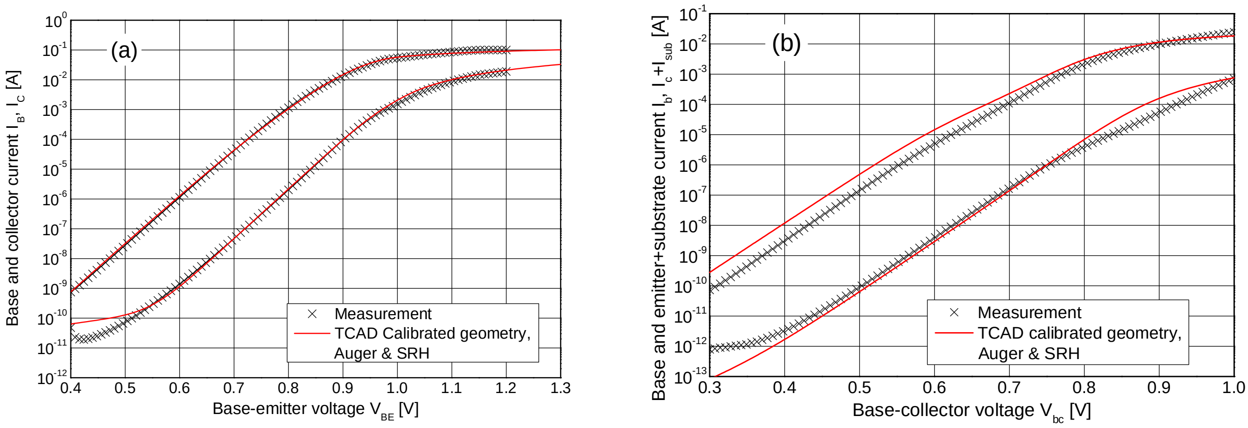


Figure 63: Forward Gummel plot @ V_{bc}=0V (a) and reverse Gummel plot @ V_{be}=0V (b). Comparison between measurements and simulation with Auger recombination model and SRH with high-field and doping dependence activated.

For the forward Gummel plot Figure 63 (a), the collector current and the base current fit very well with the measurement. However, for very low V_{be}, the simulated base current is larger than measurement data. This difference does not impact the analysis of device aging associated with the leakage current of the measurement setup, see paragraph 2.3.5.

For the reverse Gummel plot Figure 63 (b), the simulated emitter+substrate current depicts a discrepancy between the measured one, while the base current fits measurement data. Hence, to improve the accuracy of the reverse Gummel plot focus has been put on the emitter+substrate current.

4.2.3.4. Substrate contact

The emitter+substrate current has to be reduced to fit the measurement without having an impact on the forward Gummel plot. The emitter+substrate current is the sum of two currents, the emitter current and the substrate one. The emitter current has been adjusted with the forward Gummel plot. Therefore, the emitter+substrate current enhancement has been performed through the substrate current modification.

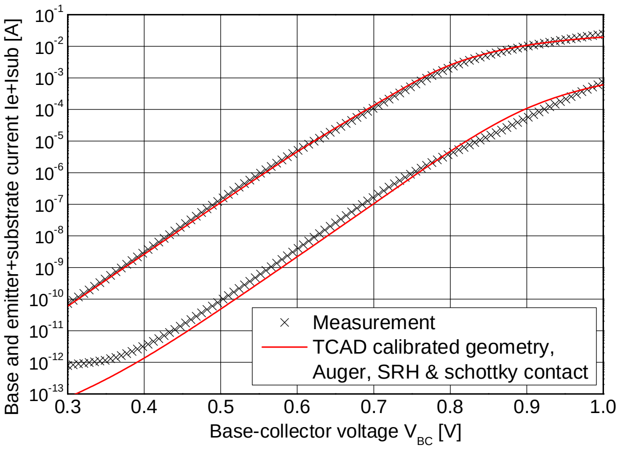


Figure 64 Reverse Gummel plot @ V_{be}=0V. Comparison between measurement and simulation result with calibrated geometry, Auger and SRH recombination with a substrate Schottky contact

The substrate contact is not designed to be biased in direct regime. Therefore, the interface between the metallic contact and the substrate is not optimized (i.e. ohmic contact). To simulate this effect, the substrate contact has been defined as a Schottky contact, [TCAD_manual]. The simulation result and measurements are compared Figure 64, with a Schottky barrier parameter defined at 0.05eV for the substrate contact.

4.2.3.5. Leakage current

In chapter 2, we have explained that the first aging campaign has been performed using a dedicated test bench with packaged devices. For this first aging campaign, a significant leakage current has been reported for low injection levels, Figure 65. This leakage current is associated with the test bench and to the device test support. For the second aging campaign, a leakage current is also reported for the reverse Gummel plot, but at a very low injection level.

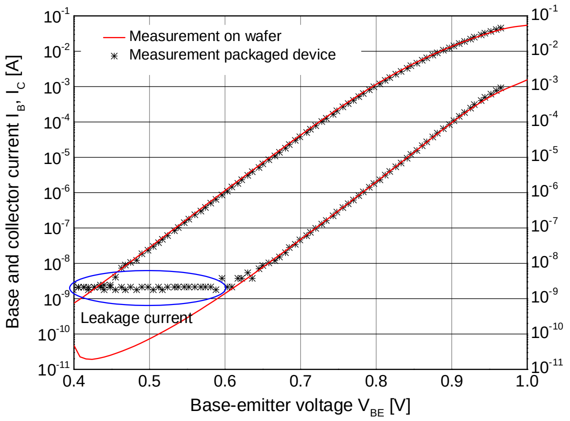


Figure 65: Forward Gummel plot @ V_{cb}=0V. Comparison between on wafer and packaged device measurements of the first aging campaign.

To simulate this leakage current, according to [Mart_2003], lumped resistors have been added between base and emitter R_{BE}, base and collector, R_{BC} and collector and emitter, R_{CE}. Then Mixed-mode simulations have been performed, including the 2D HBT structure together with lumped resistors. Values of lumped resistors have been defined to fit results for both aging test campaigns, Table 4.

Lumped resistor	First aging campaign	Second aging campaign
R_{BE}	200MΩ	700MΩ
R_{BC}	200MΩ	700MΩ
R_{CE}	200MΩ	700MΩ

Table 4: Fitted leakage current for the first and the second aging campaign

4.2.4. Conclusion

Before performing simulations of degradation effects, a calibration of the structure and physical models has been necessary. Based on a BEC device structure, a half 2D structure of the device has been drawn in Sentaurus TCAD. Conventional models and models developed for SiGe devices have been used and calibrated to simulate the structure before the aging tests. Also, we have taken into account the specificity of the measurement environment, through lumped resistances and mixed-mode simulation. Calibrated parameter values and lumped resistances are summarized in Table 5.

Model	Parameter	Value
Auger recombination	$A_{A,n}$ for electron	1.5×10^{-29} cm^{6}s^{-1}
	$A_{A,n}$ for holes	7.0×10^{-32} cm^{6}s^{-1}
SRH recombination	N_{ref}	1.0×10^{18} cm^{-3}
Base contact resistance	R_{BS}	3.295 KΩ
Schottky contact	Schottky barrier	0.05 eV
Lumped resistor	First aging campaign	200 MΩ
	Second aging campaign	700 MΩ

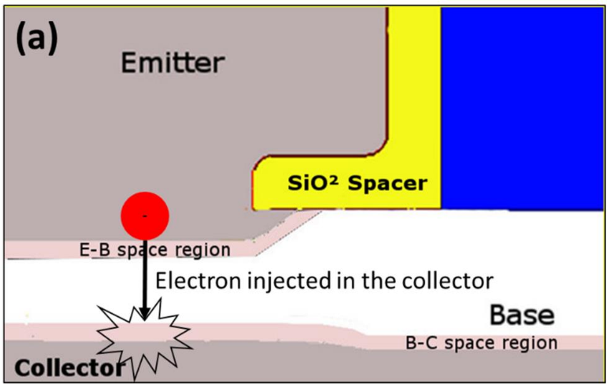
Table 5 Calibrated parameters and lumped resistances

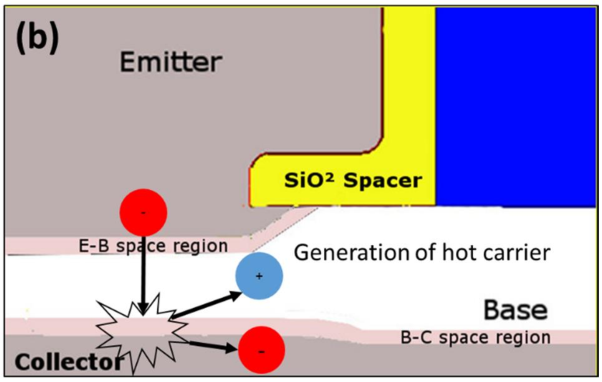
4.3. Investigation of physical origin of the degradation

4.3.1. Damage mechanism

4.3.1.1. Damage mechanisms

One major damage mechanism in SiGe:C HBT is associated to hot carriers, i-e electrons and holes with high energy. This appearance of hot carriers is the result of specific bias conditions, Figure 66 (a). Electrons are injected in the collector where they gain enough energy to generate new hot carrier pairs, Figure 66 (b). The appearance of hot carriers is the result of two physical mechanisms, either impact ionization [Cress_2004], [Neug_1997] or Auger recombination [Wach_1988], [Wier_2015]. These hot carriers may be subsequently injected at the interface of the device, Figure 66 (c). If the carrier energy is high enough, dangling bonds can be broken at this interface, increasing trap density, Figure 66 (d).





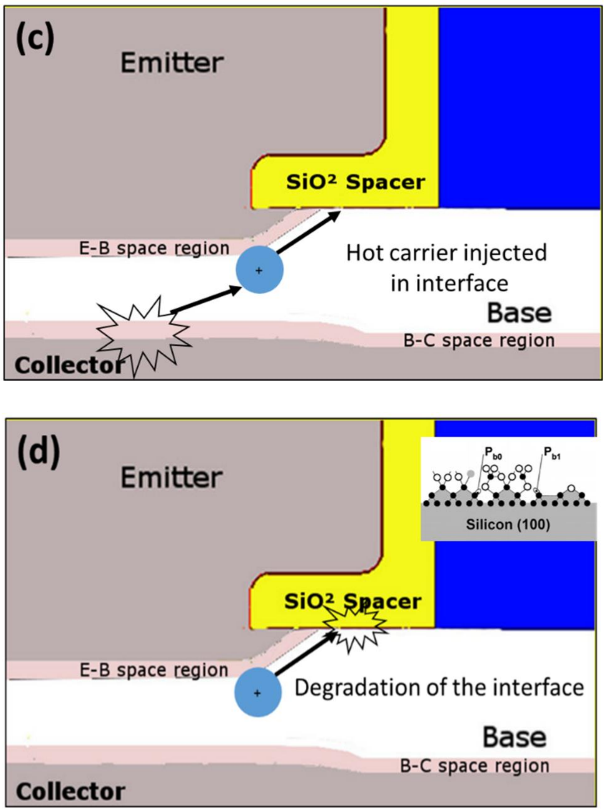


Figure 66 Damage mechanism description: Electron is injected in the collector (a). New hot carrier pair is created (b) These hot carriers are injected in the Si/SiO^2 interface (c) with enough energy to degrade the interface (d).

4.3.1.2. Location and nature of the degradation

According to [Kone_2013] and [Zhan_2002], three different interfaces of the device could be impacted by hot carriers. The first one is the interface between the emitter-base and the spacer (EB-spacer). The STI/Si interface may also be impacted by hot carrier degradation. The other interface affected by hot carrier is located in the emitter along the spacer. Damages at these interfaces can be simulated by defining additional trap density along these interfaces.

The energy level and spatial distribution of a trap density corresponds to the location and distribution of the traps in the energy band gap. However, the localization of the traps in the energy band gap is unknown and it is not possible to extract this information from measurement results. Therefore, trap density is defined at energy level E_T with a uniform distribution. The energy level E_T is chosen in the middle of the energy band gap corresponding to the maximum efficiency of the trap activity.

The trap density could be of two types, acceptor or donor depending on the carrier trapped. If hot holes degrade an interface, acceptor trap are created while a donor trap is the result of electron trapped. The type of the trap depends on the physical origin of damage mechanism and on the carrier injected at the interface.

From the literature and simulation results, two interfaces can be damaged with a significant impact on the electrical characteristics of the device:

- A Trap density at the EB-spacer interface has an impact on base current of the forward Gummel plot. An acceptor trap density has a more important impact on the forward Gummel plot than donor trap density. Therefore, we assume degradation by hot holes at this interface [Cress_2004].
- The base current of reverse Gummel plot is impacted by trap density along the STI/Si interface. Acceptor and donor trap density have exactly the same impact on reverse Gummel plot. The STI/Si interface degradation has been described in [Moen_2012].

4.3.2. Forward Gummel plot

4.3.2.1. Damage mechanisms

During aging time, an increase of the base current of the forward Gummel plot has been reported for device aged under P2 and P3 bias conditions. This behavior is also reported for the device aged under P23 bias conditions. According to 3.1.2, this evolution of the base current observed on the forward Gummel plot is the result of evolution of trap density at the EB-spacer interface, Figure 67.

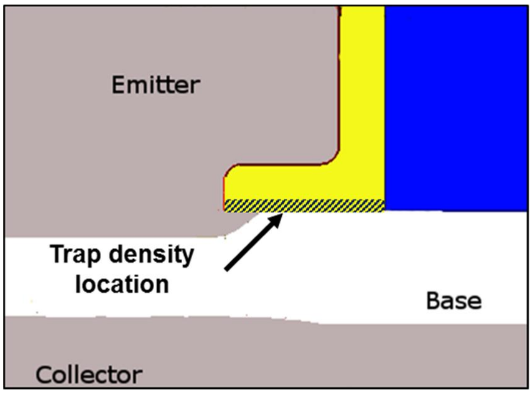


Figure 67 Trap location impacting the forward Gummel plot

The EB-spacer interface is affected by acceptor trap density, caused by hot carrier damages. The damage mechanism is attributed to impact-ionization effect [Neug_1997]. Indeed, evolution of forward Gummel plot is only reported for V_{ce} above BV_{ceo}, the activation threshold of the impact ionization. The impact ionization generates hot carriers. Generated hot holes are injected in the base-emitter region [Kamr_2016], creating an additional trap density at the EB-spacer interface.

4.3.2.2. Stress results at P2 bias condition

For each stress time, an additional acceptor trap density is assumed with energy level fixed at E_T with a uniform distribution. The trap density N_T was extracted for each stress time to fit the forward Gummel plot measurement.

Under measured P2 bias conditions, the forward Gummel plot measurement depicts an increase of the base current. To fit the measured increase of the base current, different values of trap density N_T are introduced. This process is repeated at each stress time as depicted in Figure 68 after 7h (a) and 750h (b).

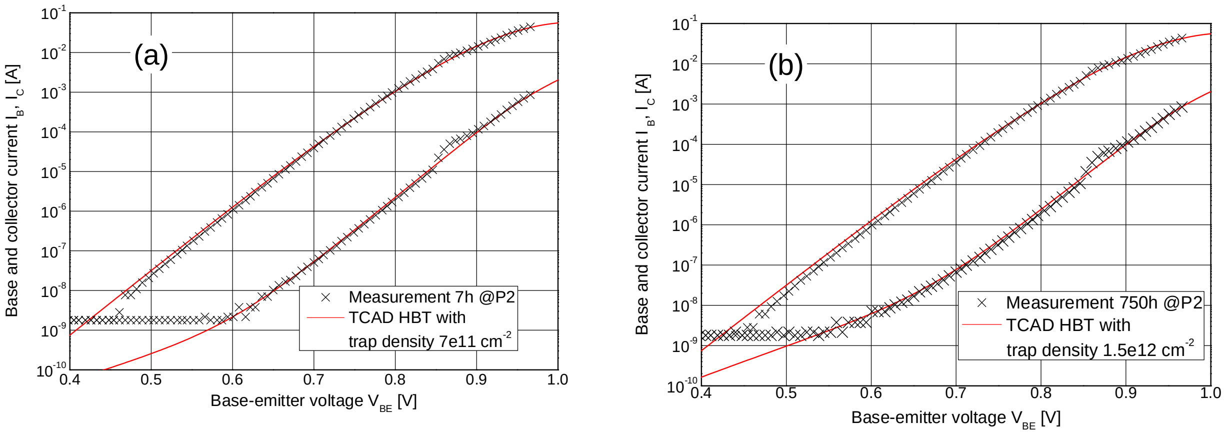


Figure 68 Forward Gummel plot @ V_{bc}=0V. Comparison between measurements after 7h (a) and 750h (b) under P2 bias conditions and simulation results with fitted trap density

The trap density for each stress time of the EB-spacer interface has been extracted for 3 different HBTs subjected to P2 bias conditions, as summarized Table 6. A mean value of the trap density for a device aged under P2 bias conditions is calculated and reported in Figure 69 as a function of the aging time.

Aging time [h]	**1**	**3**	**7**	**17**	**24**	**36**	**48**	**72**	**120**	**250**	**500**	**750**	**1000**
Trap density for device 1 [$\cdot 10^{12}$cm-2]	0.3	0.7	0.8	1	1.2	1.2	1.3	1.2	1.4	1.5	1.6	1.85	1.7
Trap density for device 2 [$\cdot 10^{12}$cm-2]	0.5	0.7	0.7	0.8	1	1	1.2	1.2	1.4	1.4	1.5	1.5	1.6
Trap density for device 3 [$\cdot 10^{12}$cm-2]	0.3	0.3	0.3	0.7	0.7	0.5	0.5	0.7	0.9	1.0	1.2	1.2	1.2

Table 6: Value of trap density for device aged at P2 bias condition

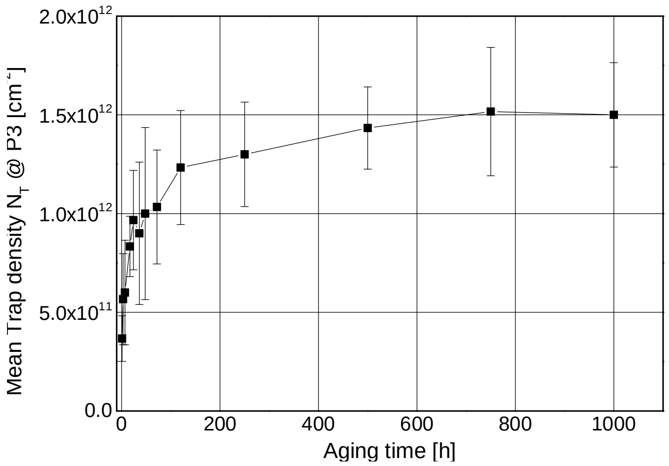


Figure 69 Mean trap density for device aged under P2 bias condition function of the aging time

The mean value of trap density as a function of the aging time shows an increase until 500h. The trap density tends to a constant value after 700h. This constant value is explained by the interface trap density saturation, due to the limited number of dangling bonds. The trap density presents the same evolution as the increase of the base current, confirming the relationship between the base current increase and the degradation of the EB-spacer interface caused by the hot carrier damage.

4.3.2.3. Stress device at P3 bias condition

The forward Gummel plot for devices subjected to P3 bias conditions shows an increase of the base current at low-injection level. Therefore, the same procedure as the device aged under P2 bias conditions is used. The trap density N_T is extracted for each stress time to fit the measurements (Figure 70) under P3 bias condition.

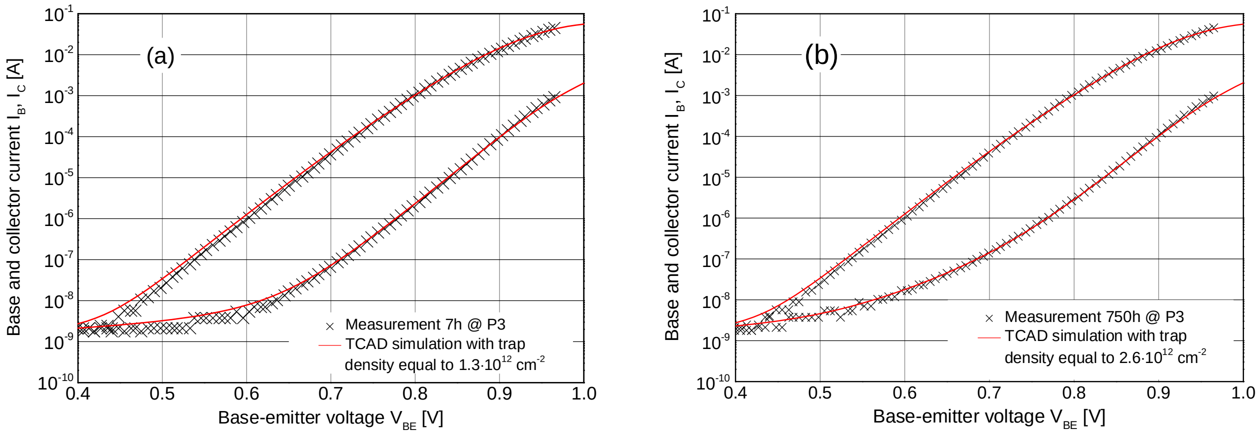


Figure 70 Forward Gummel plot @ V_{bc}=0V. Measurement results after 7h (a) and after 750h (b) under P3 bias conditions and associated simulation results

This extraction process is performed on 3 different devices aged under P3 bias conditions (Table 7). A mean value of the trap density at each stress time has been extracted (Figure 71). The mean trap density under P3 bias conditions has the same evolution as the trap density evolution under P2 bias conditions. However, the saturation value at large stress times is larger for P3 than for P2 bias conditions.

Aging time [h]	**1**	**3**	**7**	**17**	**24**	**36**	**48**	**72**	**120**	**250**	**500**	**750**	**1000**
Trap density for device 1 [$\cdot 10^{12}$cm^{-2}]	1.20	1.20	1.30	1.50	1.50	1.55	1.35	1.65	2.00	2.10	2.50	2.60	2.80
Trap density for device 2 [$\cdot 10^{12}$cm^{-2}]	1.00	1.20	1.30	1.50	1.60	1.70	1.75	2.00	2.00	2.10	2.40	2.50	2.50
Trap density for device 3 [$\cdot 10^{12}$cm^{-2}]	0.8	0.7	0.7	1.00	1.00	1.10	1.2	1.25	1.40	1.50	2.0	2.10	2.10

Table 7: Value of trap density for device aged under P3 bias conditions

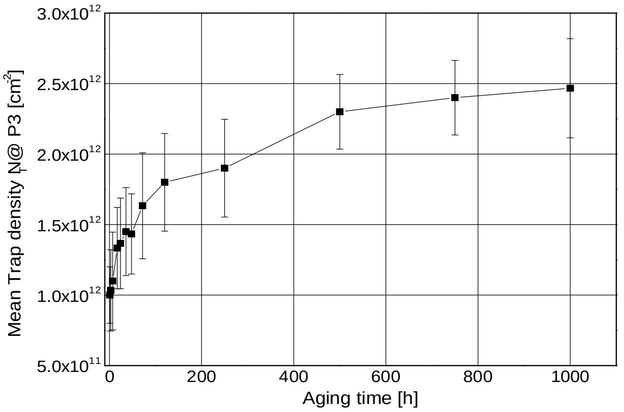


Figure 71: Mean trap density at the EB-spacer interface as a function of the aging time for devices submitted to P3 bias conditions

4.3.2.4. Conclusion

The increase of trap density at EB-spacer interface during the aging tests is reported for P2 and P3 bias conditions, Figure 72. The trap density generation in the base-collector space charge can be explained by the impact ionization effect. Impact ionization generates hot carriers. Hot holes are injected in the base whereas the hot electrons are injected towards the collector. Accelerated by electric field, hot holes gain enough energy to break the dangling bonds at the EB-spacer interface. This increase of the trap density, impacts the base current of the forward Gummel plot at low-injection levels.

The trap density at the EB-spacer interface, increasing the forward Gummel base current, is the result of a large collector-emitter voltage, above the BV_{ceo}. The higher the V_{ce} increase, the higher is the final value of the trap density at EB-spacer interface.

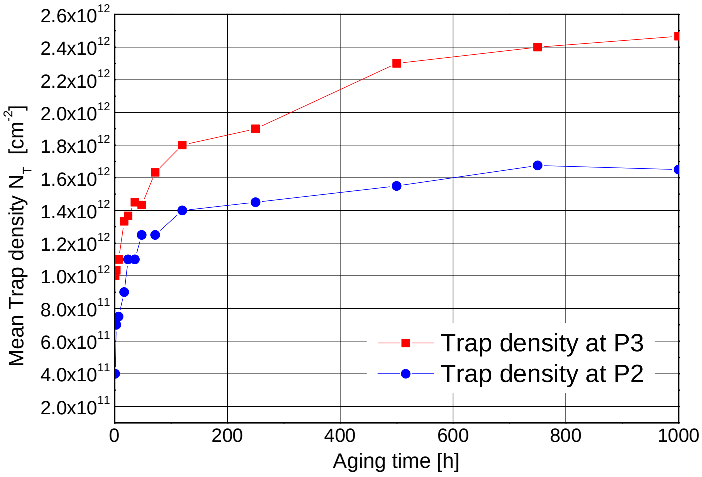


Figure 72: Trap density evolution as a function of aging time at P2 and P3 bias condition

4.3.3. Reverse Gummel plot

4.3.3.1. Damage mechanisms

The increase of reverse Gummel base current is only observed for device subjected to a high collector current density, higher than 10mA/µm². According to [Moen_2012], the damage at the STI/Si interface may be associated to hot holes and hot electrons. The upper region of the STI/Si interface is more affected by hot holes whereas the lower region is affected by hot electrons, Figure 73.

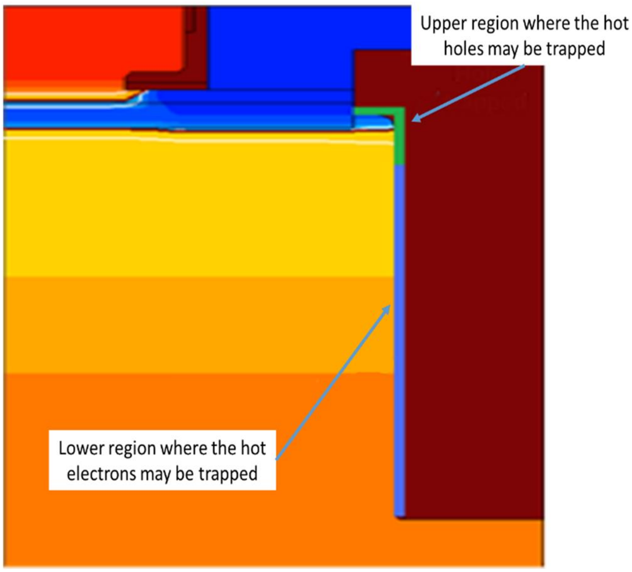


Figure 73: Location of the acceptor and donor trap densities that may be damaged by hot carriers along the STI interface

Simulation results performed with acceptor or donor trap density show that both have the same impact on the base current of the reverse Gummel plot. Therefore, it is not possible to choose the nature of trap density. To get a deeper information, a simulation of the electric field for the P23 bias condition is plotted, Figure 74.

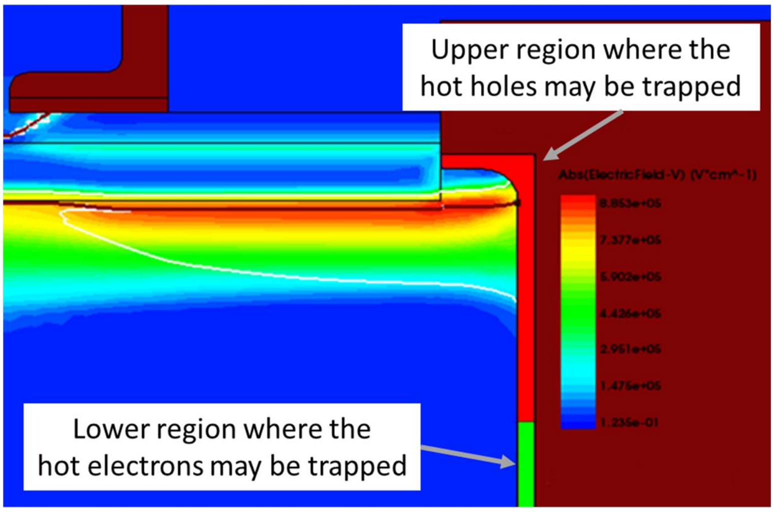


Figure 74 Electric field in the structure at the P23 bias conditions

Figure 74 shows that the electric field is more important in the upper region of the STI/Si interface than in the lower region. Therefore, the degradation of the STI/Si interface may likely be attributed to hot holes damage.

At each stress time, a trap density is defined so as to fit measurement results. The energy level and spatial distribution of trap density is defined as a uniform distribution in the middle of the energy gap, similarly to section 4.3.2.

Due to high electric field values, hot holes may damage the STI/Si interface [Zhu_2005]. As explained in 3.2, the EB-spacer interface is impacted by hot carriers generated by impact-ionization. However, for stress conditions associated with V_{ce} values lower than BV_{ceo} (P12) an increase of the reverse Gummel base current is also observed. Therefore, impact ionization may not be the only origin of degradation of the STI/Si interface.

The other possible cause of hot carrier is Auger recombination. Due to the important collector current density, Auger recombination could also be considered as an important source of hot carriers [Wier_2015]. Electric field in the structure redirect hot carrier in the STI/Si interface with enough energy to degrade the interface, same than impact ionization effect.

4.3.3.2. Trap density at P23 bias condition

Since the excess base current of the HBT aged under P12 bias condition is almost constant after 1h, it is not meaningful to extract the evolution of the trap density at that bias condition. Therefore, the trap density evolution at the STI/Si interface is only extracted under P23 bias conditions. The hole trap density is extracted at each stress time so as to fit the reverse Gummel plot measurement. An example is given in Figure 75 after 1h (a) and 48h (b) under P23 bias conditions.

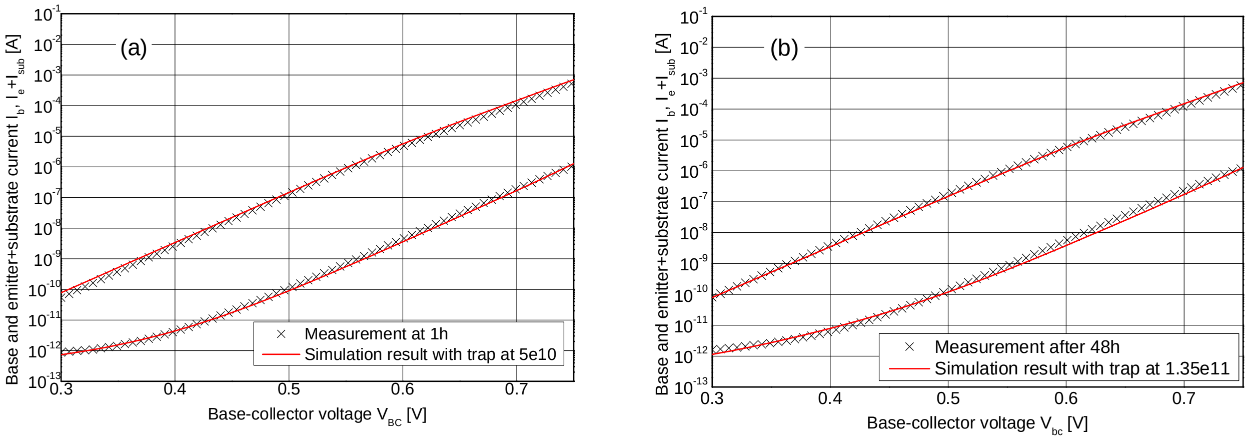


Figure 75 Reverse Gummel plot @ V_{be}=0V. Comparison between measurement and simulation results after 1h (a) and 48h (b) under P23 bias conditions

The trap density at the STI/Si interface has been extracted at each stress test, Figure 76. The trap density increases until 24h to reach a constant trap density.

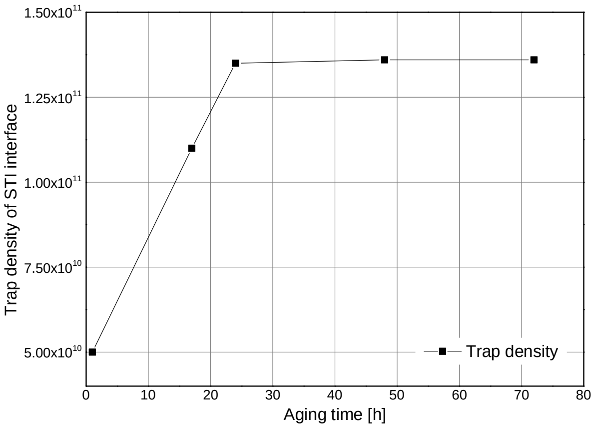


Figure 76 Evolution of trap density at STI interface for devices aged at P23 bias conditions

4.3.3.3. Conclusion

The evolution of the base current of the reverse Gummel plot corresponds to degradations of the STI/Si interface. STI/Si interface could be attributed to degraded by hot holes, in the upper region and/or by hot electrons, in the lower region. In our case, the degradation of the STI/Si interface is more likely attributed at hot hole degradations since the electric field values are much higher in that region.

The cause of the STI/Si interface damaged can have two different origins depending on the bias conditions:

- For stress conditions associated with V_{ce} values higher than BV_{ceo}, the impact ionization may be the dominant cause of hot carrier degradation.
- For stress conditions associated with V_{ce} values lower than BV_{ceo}, the Auger recombination may be the dominant cause of hot carrier degradation.

4.4. Conclusion

In chapter 2, the evolution of the base current of the forward and reverse Gummel plots have been reported during the aging stress tests. To get a deeper insight into the damage mechanism physical origin, 2D TCAD simulations have been performed. The hydrodynamic model with optimized transport parameters for Sentaurus TCAD has been used. After a calibration of the doping profile and of the model parameters, simulations have been performed to confirm the hypothesis of the degradation occurring during aging tests under different bias conditions.

For devices subjected to V_{ce} higher than BV_{ceo}, P2, P3 and P23 bias conditions, a base current variation of the forward Gummel plots have been observed. Due to the large value of V_{ce} (above BV_{ceo}), hot carriers are generated by impact ionization. These hot carriers are injected in the EB-spacer interface with enough energy to break dangling bond at this interface, increasing trap density. This increase of the trap density at the EB-spacer interface causes an increase of the base current of the forward Gummel plot at low-injection levels.

For devices subjected to P23 and P12 bias conditions, a base current variation of the reverse Gummel plot have been observed. This increase of the base current is attributed to generation of traps at the STI/Si interface caused by hot carrier damage. The degradation of the STI/Si interface can be attributed at two different damage mechanisms:

- For stress conditions associated with V_{ce} values higher than BV_{ceo}, the impact ionization may be the dominant cause of hot carrier degradation.
- For stress conditions associated with V_{ce} values lower than BV_{ceo}, the Auger recombination may be the dominant cause of hot carrier degradation.

Chapter 5 Compact model

5.1. Introduction

Technology selection for IC fabrication is mainly driven by both performance and reliability criteria. Lifetime is one of the most crucial factors for determining the performance of integrated circuits. To evaluate lifetime, the aging behavior of a specific degradation effect is studied with TCAD simulations focusing mostly on bias-temperature instability and hot carrier injection in MOSFETs, and on mixed mode degradation in bipolar transistors. TCAD simulations can provide some in-depth information on the physical mechanisms. However, these simulations can be done at the expense of very long simulation times thus making it less practical for circuit design.

Hence, it is necessary to develop a more practical circuit simulation platform using electrical compact model at the transistor level that will efficiently capture the physics of the degradation through aging laws and subsequently reflects its at circuit level.

The majority of the circuit reliability simulations has been performed on CMOS technologies. Most of these methods follow the reliability simulation flow proposed in [Hu_1992] where an electrical simulator uses standard transistors models to simulate the circuit, Figure 77. The “aging manager” computes the evolutions of transistor parameters due to degradation and performs the next simulation taking into account the new parameter value after this aging step. These tools are focused on the estimate of the overall lifetime in terms of a catastrophic failure using a figure-of-merit, the mean-time to failure (MTTF).

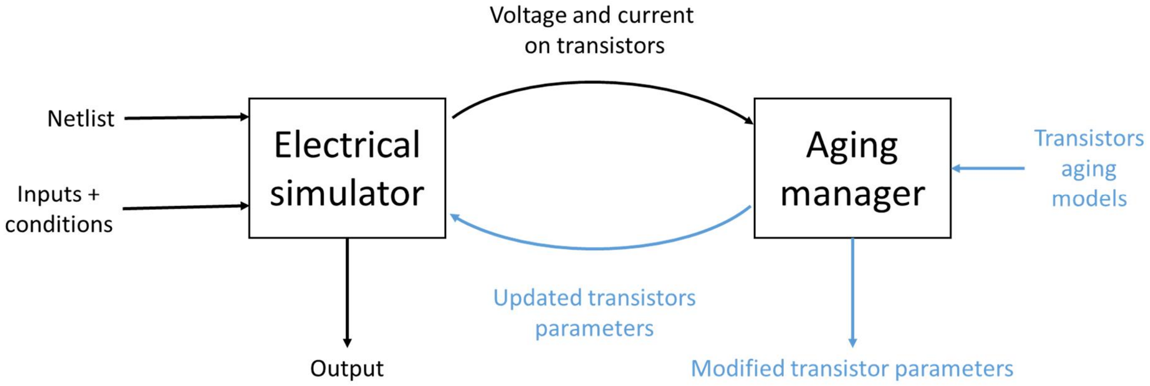


Figure 77 Conventional methodology for circuit-level reliability analysis

There are some initiatives such as [Morv_online] and [Cler_onlive] mainly focused on the modeling of the degradation at a behavioral level. A few other works on reliability simulations of analog CMOS circuits mainly addressed bias temperature instability or hot carrier injection in MOSFETs. Therefore, these aging simulation methods are mainly limited to CMOS circuits and lack the accuracy of physics based simulation.

There are only a handful of reliability studies that address the reliability of bipolar transistors, like [Ighi_2012]. [Ighi_2012] analyzes the reliability of SiGe:C HBT-based circuits based on aging law which are not implemented into the electrical compact model, and the methodology is quite similar to the conventional methodology described in [Hu_1992]. However, physics based compact modeling approaches have been proposed. One detailed and physics-based methodology has been reported in [Ardo_2012] that illustrates an accurate electrical compact model incorporating physics based aging laws, which has been extended to the circuit level for rigorous aging simulation of a complex transimpedance amplifier circuits based on InP HBT technologies, Figure 78. Compared to the conventional methodology, this methodology is based on a single simulator that optimizes the resources and integrates the aging law in the model code source to simulate circuit degradation dynamically. The same approach has been used to implement the aging laws of SiGe:C HBTs based on the studies of this thesis work.

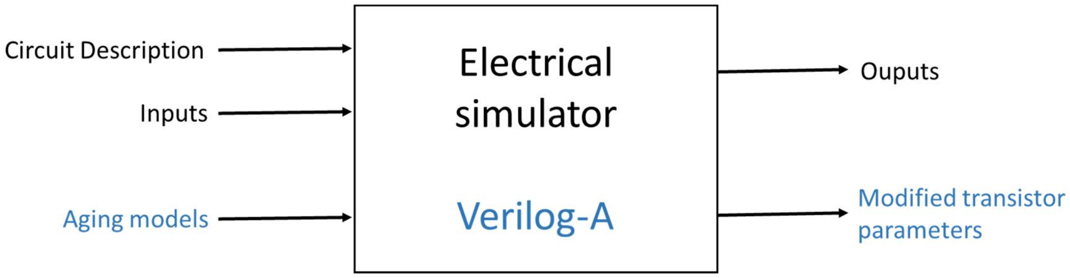


Figure 78 Single simulator-based approach for circuit-level reliability analysis

The methodology used here follows a reliability improvement short loop rather than the conventional methodology which is intended to reduce the circuit design time and costs (Figure 79). It involves a process-design kit which incorporates the electrical compact model with the aging laws implemented in it. This methodology provides an accurate description of device reliability by computing degradation laws directly in the compact models. A “virtual degradation acceleration mechanism” is taken into account for the aging model implementation to simulate years of circuit aging time translated down to seconds of electrical evolution.

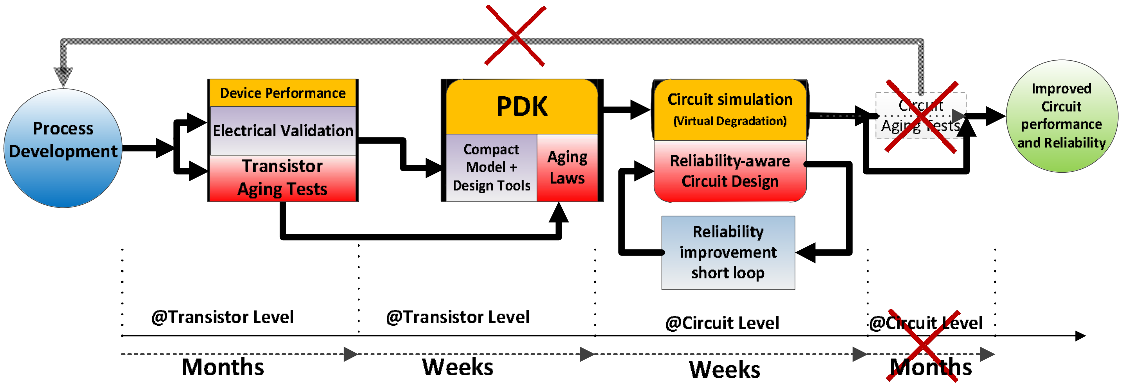


Figure 79 Methodology flow illustrating the reliability improvement loop.

The damage mechanisms affecting SiGe:C HBTs are studied in the chapter 2 during long-term aging tests. Two different damage mechanisms have been reported in chapter 4, hot carrier degradation of the EB-Spacer interface and hot carrier degradation of the STI/Si interface. In this chapter, the HICUM compact model and the implementation of the aging law are described in section 5.2. In section 5.3, a circuit reliability analysis is performed on a complex circuit (4 stages LNA) with the modified HICUM taking into account the HBT aging laws.

5.2. Aging laws implementation within HICUM compact model

5.2.1. Description of HICUM

A compact model is a physical-based and/or behavioral mathematic description of electrical and thermal characteristics of a device used to perform a simulation of complex circuits. A compact model describes many physical carrier transport mechanisms. Different compact models are used to develop mm-wave applications. The VBIC [Murt_2002] and MEXTRAM [Paas2_2001] compact models are used to model the bipolar junction transistor (BJT) and HBT. The VBIC compact model is based on the SPICE Gummel-Poon bipolar transistor model as well as the MEXTRAM model, which has been extended to SiGe HBTs. One of the most commonly used for modeling SiGe:C HBT is the HIgh CUrrent compact Model (HICUM) [Schr_2010].

HICUM is a compact model selected by the Compact Modeling Council (CMC) as one of the standard bipolar transistor compact models for the electronic industry. The first version of the model was introduced in 1987 by H.M Rein and M. Schröter and released to public domain in 1999. The HICUM compact model is based on the General Integral Charge-Control Relation (GICCR) [Schr_1993]. HICUM features a physics-based equivalent circuit containing all relevant physical effects for advanced bipolar process technologies, like distributed external base-collector region and weak avalanche breakdown.

HICUM model equations describe numerous physical effects like charge storage, bias dependence of the internal base resistance, temperature dependence of all elements (associated with its equivalent circuit) and energy-band related effects occurring in hetero-junction transistors. Due to these features, the HICUM model has been chosen in the DOTSEVEN project to simulate SiGe:C HBTs.

Presently three hierarchy (levels) of HICUM models (Level0, Level2 and Level4) exist differing by model complexity and each targeting a different design purpose. HICUM level2 contains a representation of all know relevant physical effects. A simplified HICUM compact model, level0, has been formulated to provide a model with similar simplicity as the SPICE Gummel-Poon model. HICUM Level4 has been developed for distributed electrical and thermal effects simulation.

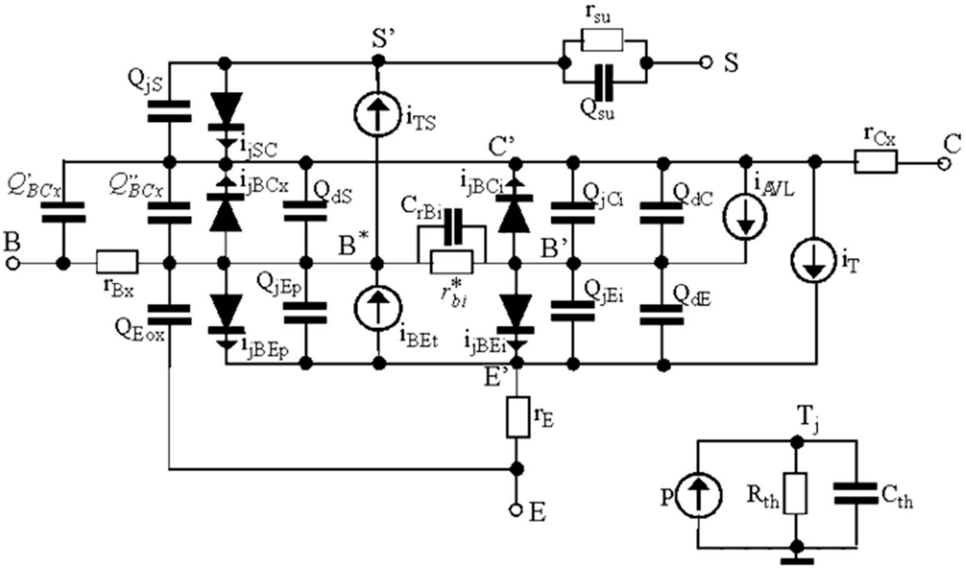


Figure 80 Equivalent schematic of HICUM level2

To implement aging laws, the HICUM level2 compact model is used (Figure 80). The physical effects, being described in the HICUM level2 model, have been used to implement the aging laws, based on the hot carrier degradation analysis described in chapter 4.

5.2.2. Peripheral base-emitter junction

According to TCAD simulation results, hot carrier damage occurs at two different interfaces during aging tests. The base-emitter spacer interface is damaged by hot holes, leading to an additional trap density. The second damaged interface is located along the STI/Si interface, and is also impacted by hot holes. The same method has been used to implement both interface degradation effects into the HICUM model.

5.2.2.1. Peripheral base current

In the HICUM compact model, the base current in normal forward regime is composed with different components [Schr_2010] as described in Figure 81. The main base current is injected in the intrinsic part of the emitter. This intrinsic base current is named I_{jBEi}. Another part of the base current is the peripheral current I_{jBEp}. This peripheral base current corresponds to the base current along the spacer (see associated description in chapter 4).

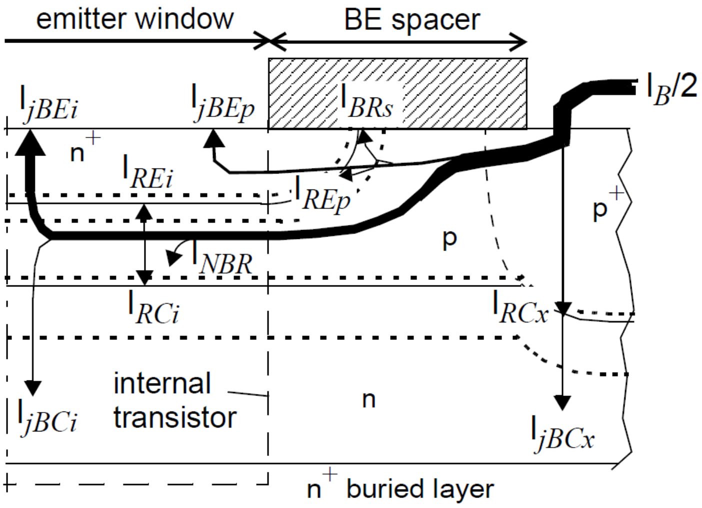


Figure 81 Repartition of the base current of HICUM model. Figure from [Schr_2010]

The peripheral base current I_{jBEp}, equation 5.1, is composed of two components, the back-injection across the emitter perimeter junction and the carrier recombination in the perimeter part of the base-emitter space-charge region.

$$I_{jBEp} = I_{BEpS}\left(\exp\left(\frac{V_{B^*E^*}}{m_{BEp}V_T}\right) - 1\right) + I_{REpS}\left(\exp\left(\frac{V_{B^*E^*}}{m_{REp}V_T}\right) - 1\right) \qquad 5.1$$

with I_{BEpS} and I_{REpS} representing the saturation currents and m_{REp} and m_{BEp} the ideal coefficients, respectively.

5.2.2.2. Carrier recombination current

During aging tests, an increase of the base current of the forward Gummel plot as a function of the aging time and bias conditions is observed. This increase of the base current is attributed to an increase of trap density at the base-emitter spacer interface (Chapter 4). In HICUM, this base current corresponds to the peripheral base current I_{jBEp}. More precisely, trap density impacts the carrier recombination current (I_{REp}), equation 5.2, of the peripheral base current.

$$I_{REp} = I_{REpS}\left(\exp\left(\frac{V_{B^*E^*}}{m_{REp}V_T}\right) - 1\right) \qquad 5.2$$

This equation has been used to simulate the increase of the base current observed during aging tests campaign.

5.2.3. Aging law

5.2.3.1. Trap density increase during aging test.

For each stress time, a value of the trap density N_T was extracted (see Chapter 4). Figure 82 presents the extracted values of the trap density at the base-emitter/spacer interface as a function of time for HBTs aged under P3 and P2 (or P23) bias conditions.

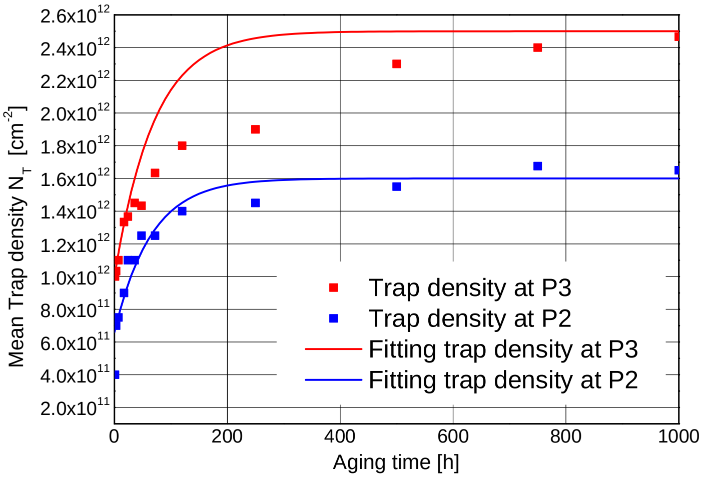


Figure 82 Trap density evolution at P2 and P3 bias conditions and the associated fitting function

For P3 and P2 bias conditions, the trap density increases drastically during the first aging hours; afterward, the trap density stabilizes to reach a constant value. Note that the trap density saturation value for P3 is higher than for P2. This higher trap density is due to a more important impact ionization effect due to the higher collector voltage in the case of P3 compared with P2.

As in [Ghos_2010] and [Ghos_2011], an exponential equation 5.3 is used to describe the evolution of the trap density as function of the aging time.

$$N_T(t) = N_{T,final}\left(1 - \left(1 - \frac{N_{T,initial}}{N_{T,final}}\right)\exp\left(-\frac{t}{\tau}\right)\right) \tag{5.3}$$

Equation parameters were extracted; with $N_{T,final}$, $N_{T,inital}$ and τ equal to 1.6x10^{12}cm^{-2}, 6.6x10^{11}cm^{-2}, and 65h for P2 and 2.5x10^{12}cm^{-2}, 1x10^{12}cm^{-2}, 70h for P3, respectively, and results depicted in Figure 82 were obtained. The time constant τ is roughly the same for both bias conditions, while for P3 the parameters $N_{T,final}$ and $N_{T,initial}$ are higher than for P2.

5.2.3.2. Fitting of peripheral base current

The evolutions of electrical characteristics during aging tests are attributed to trap activity at the emitter-base junction periphery. In the HICUM model, the base current in this region is modeled by equation 5.1. Parameters I_{BEpS} and m_{BEp} are extracted at initial time and kept constant during aging tests while recombination parameters, I_{REpS} and m_{REp}, are extracted from the measurement at the different stress times. The parameter mainly involved in the base current increase is I_{REpS}, while m_{REp} remains almost constant. The increase of I_{REpS} as a function of the aging time at P2 and P3 bias conditions is reported in Figure 83.

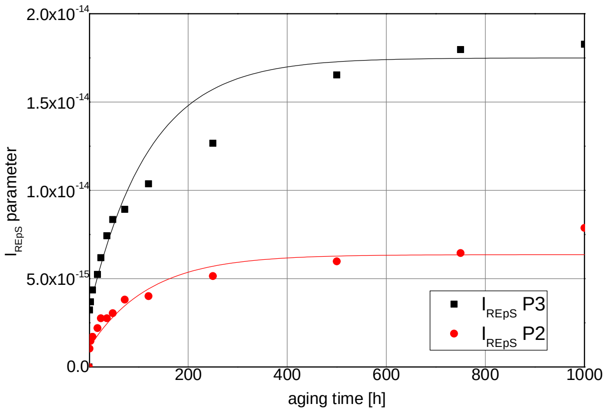


Figure 83 Evolution of I_{REpS} parameter vs. aging time for devices aged at P2 and P3 bias conditions

According to [Ghos_2010], the evolution of the parameter I_{REpS} is proportional to the trap density evolution. Finally, equation 5.4, based on equation 5.3, is used to describe the I_{REpS} evolution as a function of the aging time.

$$I_{REpS} = I_{REpS,final} + \left(I_{REpS,initial} - I_{REpS,final}\right) \cdot \exp\left(-\frac{t}{\tau}\right) \qquad 5.4$$

with $I_{REpS,final}$, $I_{REpS,initial}$ and τ equal to $1.75\text{x}10^{-14}$A, $3.2\text{x}10^{-15}$A and 120h for P2 and $6.36\text{x}10^{-15}$A, $1.08\text{x}10^{-15}$A and 120h for P3 bias conditions, respectively. The result is depicted in Figure 83.

5.2.4. Implementation of the aging law

5.2.4.1. Aging law

To implement this aging law in Verilog A, a differential equation 5.5 is used.

$$\frac{dI_{REpS}}{dt} = G - R \cdot I_{REpS} \qquad 5.5$$

with a generation rate of trap G and the rate of trap annihilation R. Equation 5.4 is the solution of the equation 5.5 with the generation rate of trap $G=I_{REpS,final}/\tau$ and the probability of traps annihilation $R=1/\tau$. A value of $2.57\text{x}10^{-20}$ A·s^{-1}, $3.7\text{x}10^{-6}$ s^{-1} for P2 and $6.66\text{x}10^{-20}$ A·s^{-1}, $3.7\text{x}10^{-6}$ s^{-1} for P3 are extracted for G and R, respectively. The annihilation ratio R is the same for the both bias conditions while the generation ratio increases with the collector-emitter voltage.

In order to include the aging law in HICUM model, we need to implement three additional parameters, namely *G*, *R* and *ATSF*:

- The *G* parameter is proportional to the impact ionization effect, occurring at high collector voltage. The impact ionization effect is modeled in HICUM through the avalanche current, I_{avl} [Schr_2010]. Equation 5.6 defines the generation rate G, according to bias conditions

$$G\left(I_{avl}\right) = A \cdot I_{avl} + G_0 \qquad 5.6$$

with $A=7.575\text{x}10^{-21}\text{s}^{-1}$ and $G_0= 0.75\text{x}10^{-20}$A·s^{-1}.

- The recombination rate *R* parameter is a constant, fixed at 3.7x10^{-6} s^{-1}.
- Aging effect takes several hours before a variation arises. To reduce the simulation time within a reasonable time, we introduce the Aging Time Scale Factor (ATSF), as

[illegible] 5.7

This parameter accelerates the aging effect so as to reduce the simulation time to few seconds.

5.2.4.2. Alternative aging law

With the first aging law, the evolution of the trap density with the aging time is described by an exponential behavior, equation 5.3. This formulation is easy to implement in a compact model environment and provides an accurate saturation behavior at large stress times. However, it does not follow the power law experimentally observed in all reported Mixed-mode experiments.

Hence, the first aging law can be improved following the approach proposed in [Huan_1993] for reverse emitter-base stress:

$$\frac{dN_T}{dt} = G N_T^{-h} - R N_T \quad 5.8$$

Here the term N_T^{-h} takes into account the effect on the generation rate of already created traps. At small stress times, the recombination term is negligible such that:

$$\frac{dN_T}{dt} \simeq G N_T^{-h} \quad 5.9$$

With G includes the effect of stress parameters. At large stress times, the aging law saturates to

[illegible] 5.10

The complete aging law is

[illegible] 5.11

Equation 5.11 could be implemented in the HICUM compact model. However, compared to equation 5.7, equation 5.11 features a power law with one more parameter and therefore yields a significant increase in the calculation time. Moreover, this equation mainly improves the aging law at small stress time, Figure 84. Therefore, to limit the impact on simulation time of the aging law, equation 5.7 is preferred to equation 5.11.

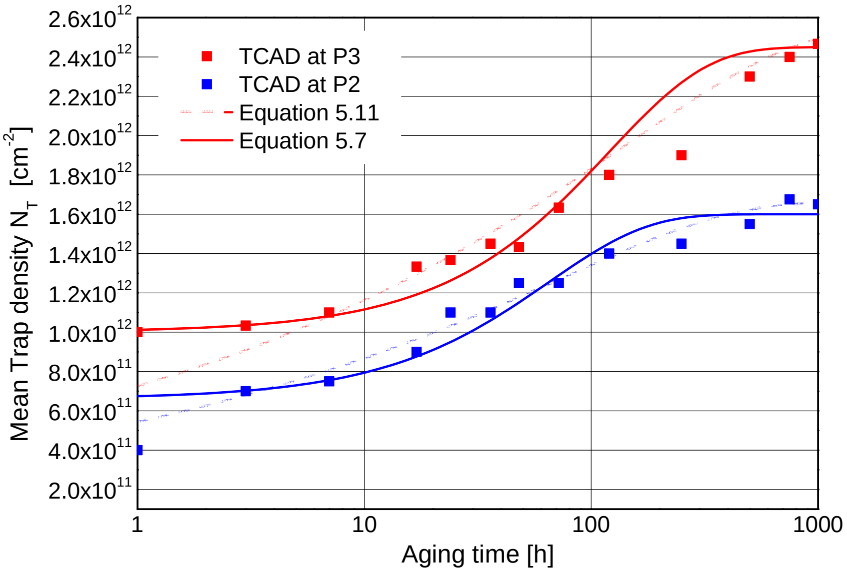


Figure 84: Mean trap density function of the aging time with associated equation 5.7 and equation 5.11

5.2.4.1. HICUM level 2 version 2.33 implementation

To implement equation 5.7 in the Verilog-A code of HICUM model level 2, we have to define a fictitious transistor node, similarly to the self-heating implementation. This new node is represented in Figure 85 and its voltage evolution follows equation 5.7, with *G* and *R* being equation parameters. The parameter *ATSF* is fixed at 3.6x10^6 to simulate 1000h (aging time) in 1s (simulated time).

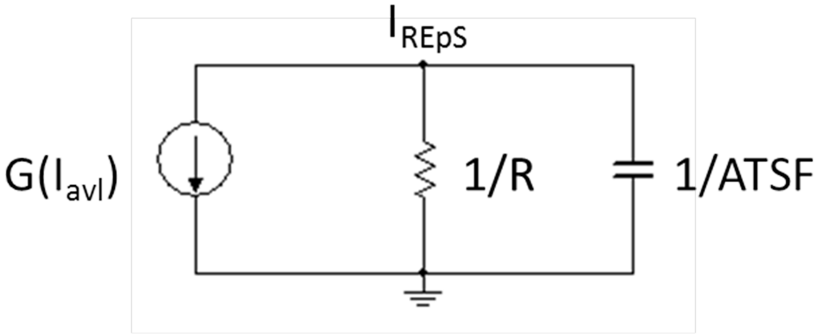


Figure 85 New transistor node used for aging law implementation in HICUM

Implementation of the aging equation and parameters in Verilog-A code of HICUM model level 2 version 2.33 are given in the box below.

```
module hic2_full_aging (c,b,e,s,tnode,age);

branch   (age ) br_age;

// Aging model parameter initialization
parameter integer  flag_age    = 1           from [0:1]  `ATTR(info="Flag for turning on and off aging effect");
parameter real       ATSF         = 3.6e6                          `ATTR(info="Accelerating Time Scale Factor");
parameter real       tau_age      = 270000                        `ATTR(info="Characteristic time" unit="s");

//Declaration of variable
real   ireps_new;
real   ga;

//Introducing Aging model
ireps_new=V(br_age)+ireps_t;

//Load source
if (flag_age == 1) begin
    if (analysis("tran")) begin
        if (analysis("ic")) begin
           V(br_age) <+ 0.0;
        end else begin
//Generation rate equation
           ga = 4.6621e-21+iavl*21.05e-21;
//Aging equation
           I(br_age) <+ ATSF*(ireps_new/tau_age-ga);
           I(br_age) <+ ddt(V(br_age));
        end
    end
end else begin
    V(br_age) <+ 0.0;
end
```

5.2.4.2. Validation of the compact model

The aging law has been implemented in HICUM Verilog-A code. To validate this aging law, simulations are performed with this model under P3 bias conditions. The model card of HICUM model has been used to fit the SiGe:C HBT characteristics for the fresh device.

Figure 86 is the schematic, based on description of the test bench, used to simulate the aging tests of one transistor. The test bench regulation loop is simplified with a comparator and an integrator is used to control the collector current with the base voltage. The collector current is compared to the bias collector current controlled by the comparator. If relevant, the difference between the desired collector current and the applied one is injected to the integrator and the result applied to the base of the SiGe:C HBT.

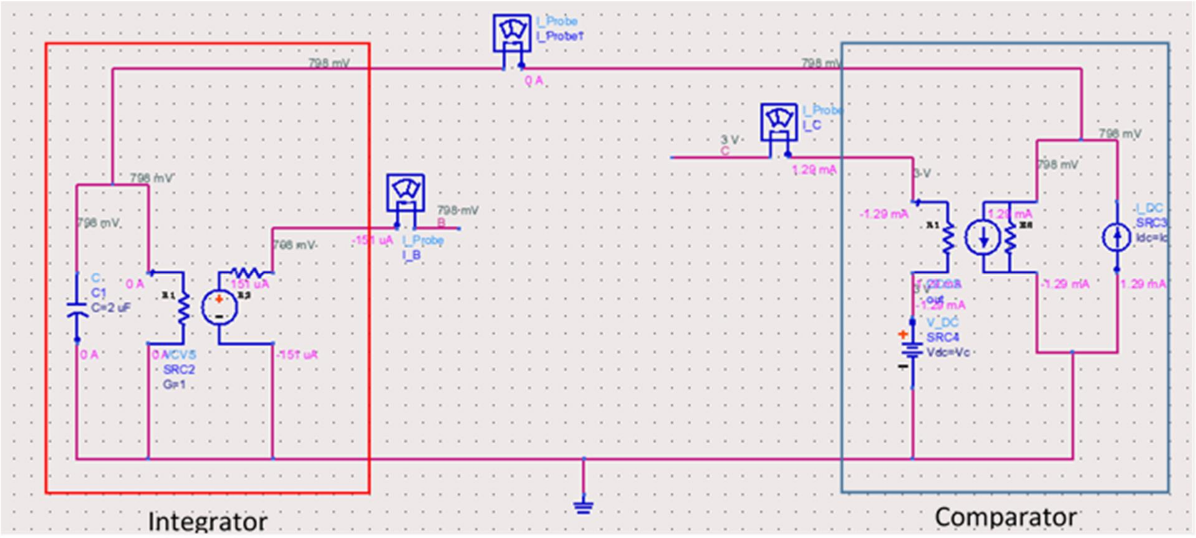


Figure 86 Schematic used to simulate the test bench

The HICUM model incorporating the aging law is used to simulate the aging of the device during 1000h. To simulate this 1000h in 1s, the ATSF parameter has been fixed at 3.6x10^{6}. To estimate the impact of the aging law implementation on simulation time, the simulation is performed with the aging law activated and disabled. The simulation time increase is lower than 1% with the aging law activated. This value demonstrates the reduced penalty of the aging law activation on the over whole circuit simulation time.

The forward Gummel plot is simulated at initial time and after 1000h under P3 bias conditions, and compared to measurement results, Figure 87 (b). The evolution of the I_{REpS} parameter is also reported as a function of the aging time, Figure 87 (a).

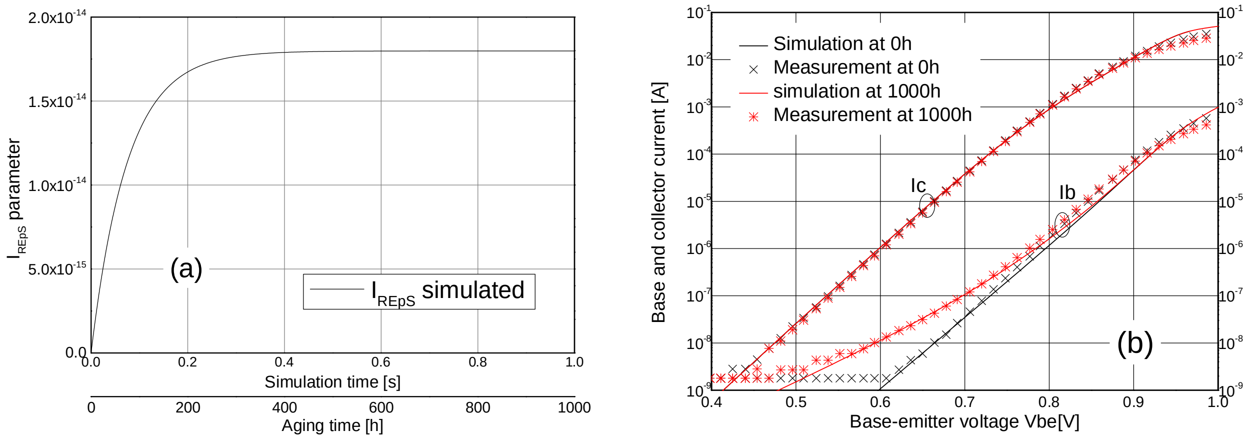


Figure 87: Evolution of the I_{REpS} parameter of one device simulated under P3 bias conditions (a) and comparison of forward Gummel plot simulated and measured at 0h and 1000h (b)

I_{REpS} presents the expected evolution as a function of the time, i.e. a rapid increase eventually reaching a constant value. The forward Gummel plot at initial time and after 1000h fit very well the measurement.

5.2.5. Conclusion on the enhanced compact model

To help designers to develop more reliable circuits, a compact model incorporating the device aging law has been developed. This compact model is based on HICUM level 2 version 2.33.

Only the damage mechanism associated with EB-spacer interface has been implemented since a more important impact on DC characteristics is expected compared to the degradation mechanism associated to the STI/Si interface. The I_{REpS} parameter of HICUM model is modified to follow the evolution of the associated EB-spacer trap density with device aging.

To validate this compact model, simulations have been performed in the same conditions as the aging tests. The evolution of the forward Gummel plot follows the base current increase as a function of the aging time. Hence, this compact model can be used to assess the reliability of a complex circuit schemes with a low impact on simulation time.

5.3. Reliability assessment of a complex circuit

The compact model with aging law has been developed to simulate evolution of complex circuit during time. The same methodology has been used in [Muk3_2016] to study the reliability of a transimpedance amplifier. Results presented in [Muk3_2016] confirm the feasibility of this methodology to study reliability of a complex circuit and the possibility to optimize the circuit to increase reliability of a whole system. Based on this, the compact model with aging law presented below could be used to perform reliability simulation of a complex circuit realized with studied SiGe:C HBTs.

5.3.1. Low-Noise Amplifier

Mm-wave circuits based on SiGe:C HBTs are mainly low-noise amplifier, oscillator and mixer circuits to realize RF front-ends [Ojef_2012]. A low-noise amplifier (LNA), designed by Ulrich PFEIFFER from the university of Wuppertal within the DOTSEVEN project, has been used to study the circuit reliability using enhanced HICUM model. The LNA is designed to operates at 220GHz. The architecture of the LNA is described below.

5.3.1.1. Structure of the full LNA

The schematic of low-noise amplifier is described in Figure 88. The LNA presents 4 amplifier stages featuring the same design plus two baluns.

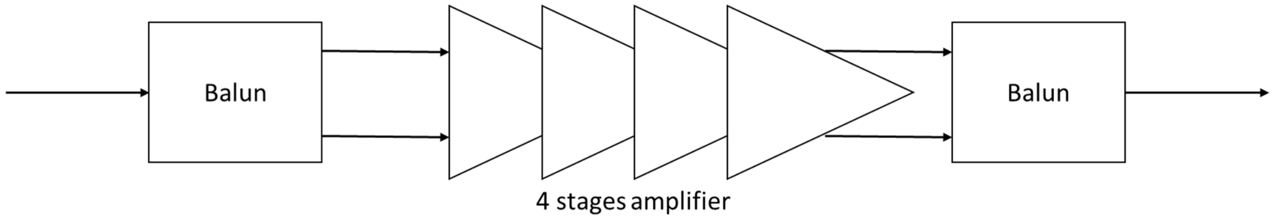


Figure 88 Schematic of the LNA

The input signal is applied to the input balun, to convert single ended signal into a differential signal. This differential signal is amplified by 4 differential cascode structures in series. The output signal of the last stage is applied to a balun to obtain a single ended signal.

The interconnection between each amplifier stage and balun is taken into account by adding extra circuits, as reported in Figure 89.

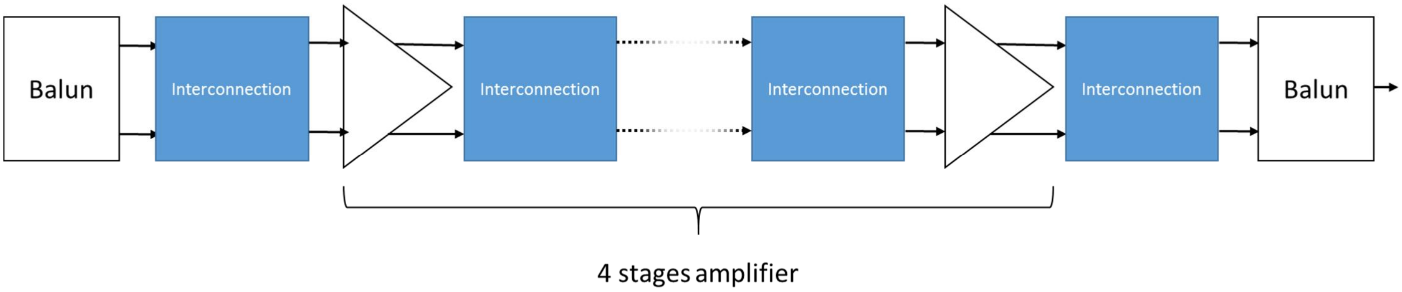


Figure 89: Schematic of the LNA

5.3.1.2. Details of one amplifier stage structure

Each amplifier stage of the LNA presents exactly the same differential cascode structure, reported Figure 90. The cascode structure is symmetric, transistors Q1 and Q2 operate as a common-emitter structure whereas Q3 and Q4 transistors are connected in a common-base configuration. A current mirror is realized with transistors Q5-Q3 and Q5-Q4.

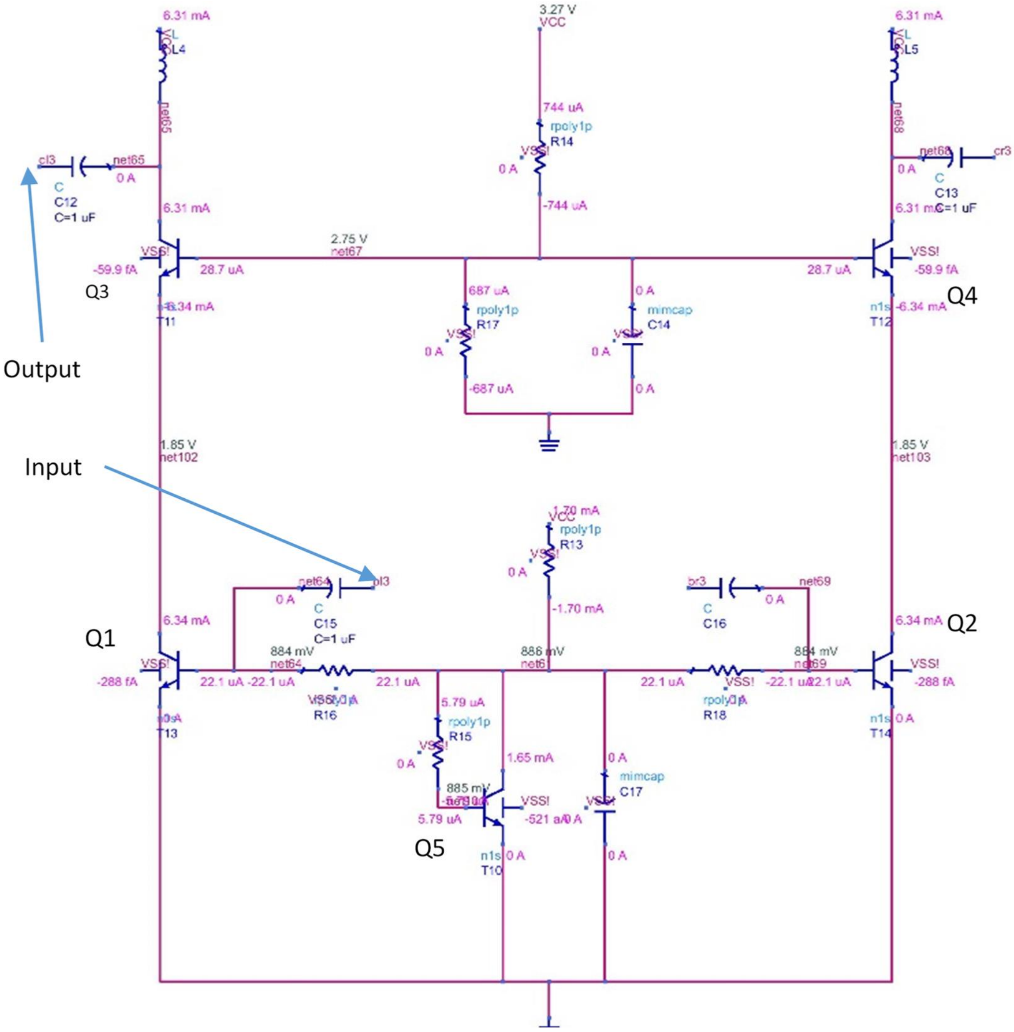


Figure 90 schematic of one amplifier stage

Transistors with common-base configuration, Q3 and Q4, presents an important voltage nominal gain. However, since the input resistance is very low, it limits the performance of the structure in terms of output power. To increase the input resistance, a common-emitter configuration, Q1 and Q2, is placed before the common-base structure. The common-emitter configuration is also used to bias the common-base configuration. To do that, a current mirror is realized with Q1 (or Q2) and Q5.

5.3.2. Simulation results

5.3.2.1. Initial characteristics of LNA

A simulation of the whole LNA circuit is performed using Advanced Design System (ADS) software. The LNA circuit is designed to operate at 220GHz with a DC power of 3.3V. The DC nominal bias conditions of each transistor is reported in the schematic Figure 90. Q4 and Q3 transistor are biased with a V_{ce}=1.42V at the limit of the BV_{ceo}=1.5V whereas Q1 and Q2 are biased with a V_{ce}=1.85V above the BV_{ceo}. The bias collector current of these transistors is fixed at 6.34mA. The transistor Q5 is biased at low V_{ce} (V_{ce}=0.886V) and low collector current (I_c=1.65mA).

The gain of the whole circuit is reported Figure 91. The maximum gain is close to 3.8 at 210GHz and falls to 3.2 at 220GHz. The simulated results include interconnection losses. These interconnection effects move the gain peak closer to 210 GHz than the intended 220-GHz center frequency. The same behavior is explained in [Ojef_2012] for the same LNA design with another SiGe:C technology node.

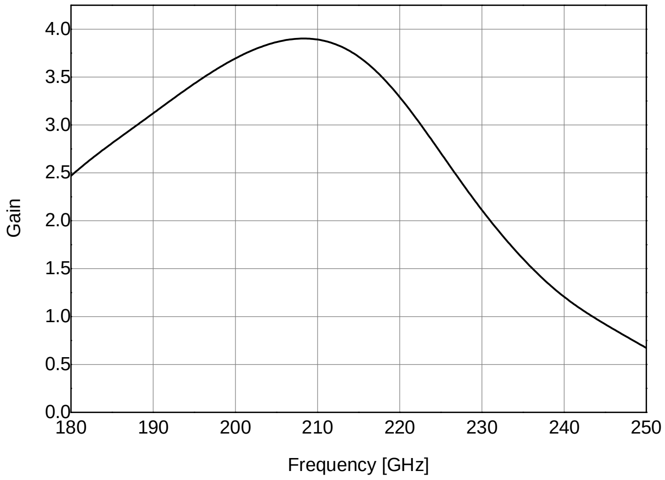


Figure 91: Gain of the LNA as a function of input frequency

5.3.2.2. Circuit reliability simulation

To study the reliability of LNA circuit, simulations are performed with the compact model taking account the degradation laws of the HBT. This modified compact model is used for all HBT's of the circuit. The $ATSF$ parameter is set at $3.6\text{x}10^{15}$ to simulate 1000h (aging time) in 10ns (simulated time). The impact on simulation time activating the aging laws is negligible, with an increase lower than 1%. The gain of the LNA has been compared at initial time and after 1000h in Figure 92. The gain of the whole circuit doesn't show significant variation after 1000h.

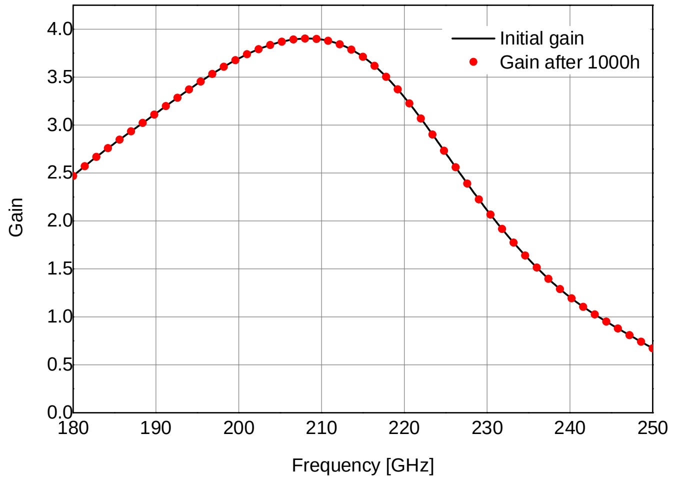


Figure 92: Gain of the LNA function of input signal frequency at 0h and after 1000h

To get a deeper insight in circuit reliability, the I_{REpS} parameter evolution is analyzed for every transistor and every stage of the LNA, Figure 93. We note a similar evolution for Q1 and Q2 transistors and Q3 and Q4 transistors. This similar evolution of I_{REpS} is explained by the symmetry of the differential cascode structure. Therefore, in the following, only half part of the differential cascode structure is studied.

The I_{REpS} parameter of the transistor Q5 is almost constant. The absence of Q5 degradation is explained by the operation of this transistor, only used to bias the circuit, no AC signal applied to the device, and its bias is lower than BV_{ceo}.

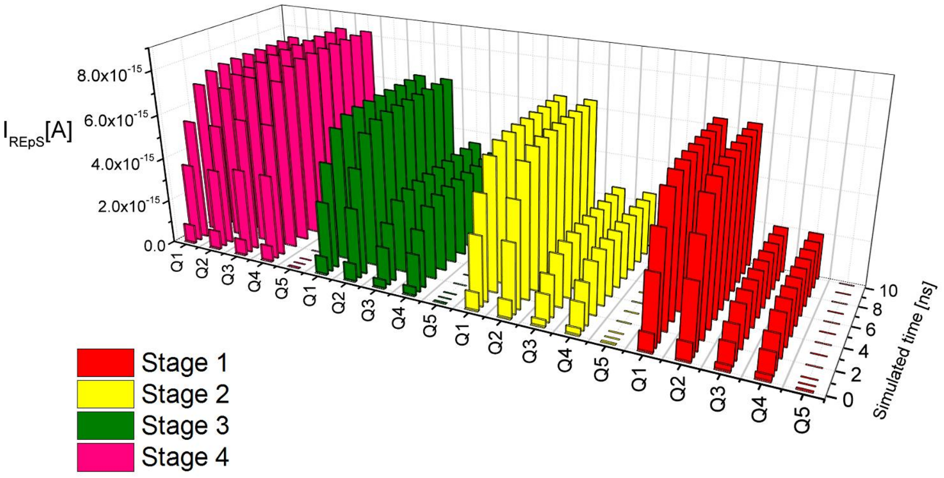


Figure 93: I_{REpS} parameter evolution for each transistor of the LNA

Figure 94 shows that the I_{REpS} parameter of Q4 increases with aging time. Moreover, depending on the stage number, it gradually increases from the first to the last LNA stage (I_{REpS} of stage 4 > I_{REpS} of stage 3 > I_{REpS} of stage

2 > I_{REpS} of stage 1). This evolution can be explained by an increase of the input signal amplitude from one stage to another.

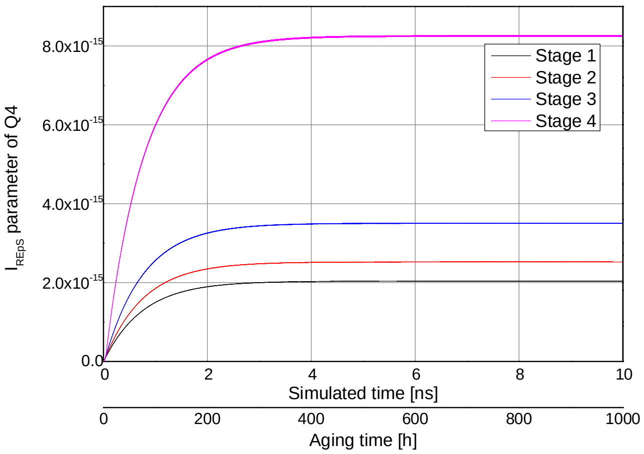


Figure 94 Evolution of the I_{REpS} parameter for Q4 for the different stages of the LNA

This evolution of the I_{REpS} parameter of Q4 is the result of the degradation of the EB-Spacer interface. However, Q4 is connected in a common-base configuration, therefore its low base current level has a low impact on its bias conditions. Therefore, the reliability of the LNA is not impacted by this evolution of Q4.

The second transistor with an evolution of the I_{REpS} parameter is Q2. The evolution of the corresponding I_{REpS} is reported in Figure 95. For stage 1 to 3, the I_{REpS} parameter presents the same evolution, whereas the I_{REpS} parameter of stage 4 is more important. The evolution of the I_{REpS} parameter of Q2 has the same order of magnitude as the I_{REpS} parameter of Q4.

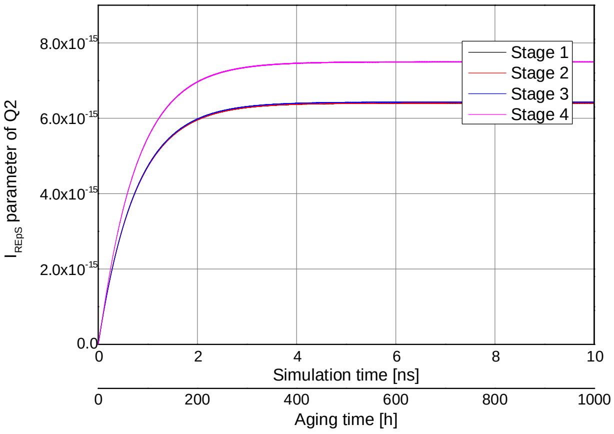


Figure 95 Evolution of the I_{REpS} parameter for Q2 for the different stage of the LNA

Differently from Q4, the degradation of transistor Q2 could have an impact on the circuit reliability. Indeed, an increase of the low base current of Q2 could change the current mirror (Q2, Q5) ratio. A changing of bias Q4 condition, defined by the current mirror, could reduce the gain of the common-base configuration and therefore of the whole LNA bias. However, the variation of the I_{REpS} parameter and therefore of the low base current, is too low to impact the LNA biases.

To conclude, HICUM model including the aging laws has been used to assess the reliability of a complex circuit: the 4 stages low-noise amplifier designed by the university of Wuppertal within DOTSEVEN project. The aging simulations using the HICUM model with the aging laws have detailed the evolution of the DC characteristics of different transistors. However, since the degradation effects reach saturation with the aging/operating time, this degradation does not have a significant impact on the whole LNA characteristics.

5.4. Conclusion

Based on the degradation mechanisms occurring during SiGe:C HBT operation, reported in previous chapters, an aging law has been proposed which take into account stress conditions. This aging laws depicts the evolution of the degradation of the EB-spacer interface, as a function of the bias conditions and the aging time. To implement this aging law in Verilog-A language, the derivative of this aging law has been calculated.

The HICUM compact model level2 version 2.33 has been chosen due to its features including numerous physical effects description. Moreover, the DOTSEVEN project has also chosen the HICUM compact model to simulate SiGe:C HBT. To implement the aging law, the I_{REpS} parameter has been used. This parameter corresponds to the base current of the EB-spacer interface impacted by hot carrier degradation. I_{REpS} has been adapted as a variable following the aging law.

A reliability simulation has been performed with this model on a complex-circuit, a 4-stage low-noise amplifier (LNA). The simulation time is not significantly affected by the activation of the aging law, since the increase of simulation CPU time is lower than 1%. The compact model with aging law has been used for every SiGe:C HBT operating in the LNA. Although the degradation of EB-spacer is taken account as a function of bias conditions for each device, the output signal of the LNA does not show a significant variation during the aging time. Hence, the operation of this LNA is weakly impacted by the degradation of the EB-spacer interface.

These results show the robustness of this LNA design subject to some degradation of EB-spacer interface. From a reliability methodology point of view, the possibility to individually study the evolution of each transistor electrical characteristics has been demonstrated with a low impact on simulation CPU time and confirms the consistency of the whole DOTSEVEN reliability methodology at circuit level.

Chapter 6 Conclusion

The reliability of modern SiGe:C HBT is an important criterion to develop future mm-wave applications. Conventional stress tests are useful to characterized SiGe:C technology reliability but it's difficult to predict the evolution of HBT characteristics under dynamic operating conditions. This difficulty can cause an over-estimation of SiGe:C HBT degradation, in circuit performance/efficiency. To predict the evolution of DC characteristics in circuit applications, a compact model taking into account damage mechanism activation has been proposed.

To characterize hot-carrier degradation mechanisms, a long-term reliability methodology has been proposed. This process consists to polarized the SiGe:C HBT in a common emitter configuration at bias conditions near the safe operating area border. This aging test has been performed on a 130nm SiGe:C HBT technology manufactured by Infineon technology, with an F_T/F_{max} equal to 240/380GHz at J_c=10mA/µm². Samples have a double collector and double emitter configuration with ground-signal-ground pads. Aging test are performed on 0.13x9.93µm² effective area devices.

To characterize the impact of degradation mechanisms on DC device characteristics, the forward and reverse Gummel plots have been measured at defined times during the aging tests. The results of aging campaigns can be summarized as:

- Increase of base current of forward Gummel plot for important collector-emitter voltage
- Increase of base current of reverse Gummel plot for important collector current density

Moreover, the low-frequency noise has been measured during the second aging campaign. The low-frequency noise is used like a reliability characterization means, more sensitive to variations of interface states compared to DC electrical characteristics. The low-frequency noise measurement depicts a variation of the base voltage PSD during the aging test. The variation of base current of forward/reverse Gummel plot and low-frequency noise can be explained by the creation of trap density at the interface of the device.

To better understand the creation of trap density by the damage mechanism activation, physical TCAD simulations have been undertaken. TCAD simulations are performed on a half device structure with the hydrodynamic model, adapted to the SiGe:C HBT. Hydrodynamic, Auger recombination and SRH recombination models are activated and calibrated to have a good agreement between simulated and measured Gummel plots before aging test.

Major degradation mechanisms in SiGe:C HBTs are associated to hot carrier degradations. Due to specific bias conditions, electrons are injected in the collector. These electrons gain enough energy to generate new hot carriers by impact ionization. Another physicals phenomenon can cause the generation of hot carriers Auger recombination in the neutral base region. These hot carriers may be subsequently injected at the interface of the device. If the carrier energy is high enough, it breaks dangling bonds at this interface, increasing trap density. Two interfaces have been identified to be impacted by hot carriers, the emitter-base/spacer and the STI/Si interface.

Based on these considerations and TCAD simulation results, the increase of the forward Gummel plot base current is attributed to the increase of trap density at the EB/spacer interface, whereas the increase of the reverse Gummel base current is attributed to an increase of trap density at the STI/Si interface. The trap density at these two interfaces have the same evolution during aging time: an increase during the first hours of the stress test gradually reaching a constant value. The degradation rate and the constant value are bias conditions dependent.

One degradation mechanism has been identified: for stress conditions associated with V_{ce} higher than BV_{ceo}, the impact ionization may be the cause of hot carries degraded the EB/spacer and STI/Si interfaces.

Additionally, for stress conditions associated with high collector current density, the Auger recombination may be the cause of hot carriers impacted STI/Si interface.

To implement the aging laws in a compact model, the HICUM compact model is chosen. This model is the choice within the DOTSEVEN project to simulate SiGe:C HBT. The HICUM compact model well describes different physical phenomena occurring in SiGe:C HBTs. For this thesis work, only the degradation of the EB/spacer interface has been implemented. However, the same process could be repeated for the STI/Si interface.

To implement degradation effects for the EB/spacer interface, the I_{REpS} parameter of HICUM compact model is used. This parameter corresponds to the base current part impacted by trap density at the EB/spacer interface. According to TCAD results, the evolution of trap density is caused by hot carriers generated by impact ionization. Impact ionization is a physical phenomenon implemented in HICUM, and represented by the avalanche current I_{avl}. To implement aging laws in HICUM, the I_{REpS} parameter has been converted in a variable following the evolution of trap density function of the avalanche current and therefore, impact ionization.

To validate the HICUM compact model taking into account the evolution of the EB/spacer interface, a simulation has been performed to age the SiGe:C HBTs in same conditions as aging test. The simulation result follow very well the measured forward Gummel plot after 1000h at P3 bias conditions.

To confirm the possibility of compact model to predict reliability issues of complex circuits, a reliability analysis has been performed on a low-noise amplifier designed with studied SiGe:C HBTs. For every SiGe:C HBT of the LNA, the compact model taking into account damage mechanism has been used. The CPU simulation time is not significantly affected by the activation of the aging law, with a variation lower than 1%. Despite the degradation of the EB/spacer interface, the output signal of the LNA does not show a significant variation during aging time.

The first compact model taking into account damage mechanism activation for SiGe:C HBT has been presented in this thesis work and published in [Jacq_2015]. An aging test methodology has been proposed to characterize the evolution of HBT characteristics during a long time at bias conditions near the safe operating area border. Damage mechanisms has been identified from these measurement results and implemented in the HICUM compact model.

This compact model can be used to design more reliable circuit by simulated reliability analysis. This process facilitates the reliability study of the circuit, reducing the development time of the mm-wave applications. The same procedure has been used in [Wier_2016] to develop a compact model taking into account the mixed-mode degradation.

References

[Akyi_2014] Akyildiz I. F., Jornet J. M., et Han Chong. Terahertz band: Next frontier for wireless communications. 2014, Physical Communication, vol. 12, p. 16-32.

[Ales_2010] dôAlessandro, V., Marano, I., Russo, S., Céli, D., Chantre, A., Chevalier, P., Pourchon F. & Rinaldi, N. Impact of layout and technology parameters on the thermal resistance of SiGe: C HBTs. 2010, Proc. IEEE BCTM (pp. 137-140).

[Ardo_2012] Ardouin B., Dupuy J.-Y., Godin J., Nodjiadjim V., Riet M., Marc F., Koné G. A. Ghosh S. Grandchamp B. & Maneux C. Advancements on reliability-aware analog circuit design. ESSCIRC (ESSCIRC), 2012 Proceedings of the, 2012, p. 46-52.

[Bock_2015] Böck J., Aufinger K., Boguth S., Dahl C., Knapp H., Liebl W., Manger D., Meister T.F. Pribil A., Wursthorn J., Lachner R., Heinemann B., Rucker H., Fox A., Barth R., Fischer G., Marschmeyer S., Schmidt, Trusch A. & Wipf C. SiGe HBT and BiCMOS process integration optimization within the DOTSEVEN project. 2015, Bipolar/BiCMOS Circuits and Technology Meeting-BCTM, pp. 121-124.

[Bruc_1999] Bruce S. P. O., Vandamme L. K. J., & Rydberg A. Measurement of Low-Frequency Base and Collector Current Noise and Coherence in SiGe Heterojunction Bipolar Transistors Using Trans-impedance Amplifiers, 1999 IEEE Trans. Electron Dev. vol. 46, no. 5, pp. 993-1000.

[Chev_2011] Chevalier P., Meister T. F., Heinemann B., Van Huylenbroeck S., Liebl W., Fox A., Sibaja-Hernandez A. & Chantre A. Towards THz SiGe HBTs. 2011, IEEE Bipolar/BiCMOS Circuits and Technology Meeting.

[Chev_2012] Chevalier P., Lacave T., Canderle E., Pottrain A., Carminati Y., Rosa J., Pourchon F., Derrier N., Avenier G., Montagne A., Balteanu A., Dacquay E., Sarkas I., Celi D., Gloria D. Gaquiere C., Voinigescu S. P., & Chantre A. Scaling of SiGe BiCMOS Technologies for Applications above 100 GHz. 2012, IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), pp. 1ï 4.

[Cism_2010] Cismaru C., Banbrook H., & Zampardi P. J.. High volume test methodology for HBT device ruggedness characterization. 2010, CS Mantech Conference, Paper (Vol. 5).

[Cler_online] Clerevo project http://www.clerevo.eu/publications

[Cost_1992] Costa D., & Harris J. S. Low-frequency noise properties of Npn AlGaAs/GaAs heterojunction bipolar transistors. 1992, IEEE transactions on Electron Devices, 39(10), 2383-2394.

[Cress_2004] Cressler, J. D. Emerging SiGe HBT reliability issues for mixed-signal circuit applications. IEEE Transactions on Device and Materials Reliability,4(2), 222-236, 2004.

[Dels_1997] C. Delseny, F. Pascal, S. Jarrix, and G. Lecoy, "Noise correlation measurements in bipolar transistors. II. Correlation between base and collector currents", J. Appl. Phys. vol. 81, no. 6, pp. 2658-2664, 1997.

[Dotfive_online] DOTFIVE, Towards 0.5 THz Silicon/Germanium Heterojunction Bipolar Technology. EUFP7 funded IP, number 216110, http://www.dotfive.eu/.

[Dotseven_online] DOTSEVEN, Towards 0.7 THz Silicon/Germanium Heterojunction Bipolar Technology. EUFP7 funded IP, number 316755, http://www.dotseven.eu/.

[Ersh_1994] Ershov M., & Ryzhii V. High-field electron transport in SiGe alloy. 1994, Jpn. J. Appl. Phys., vol 33, p. 1365-1371

[Fede_2005] Federici, J. F., Schulkin, B., Huang, F., Gary, D., Barat, R., Oliveira, F., & Zimdars, D. THz imaging and sensing for security applicationsð explosives, weapons and drugs. 2005, Semiconductor Science and Technology,20(7), S266.

[Fisc_2014] Fischer, G. G., Reliability of SiGe HBTs in Long-Term Operation. 2014, ECS Transactions, 64(6), 39-51.

[Fisc_2015] Fischer G.G., & Sasso G., Ageing and thermal recovery of advanced SiGe heterojunction bipolar transistors under long-term mixed-mode and reverse stress conditions, 2015, Microelectronics Reliability, vol. 55, no. 3ï 4, p. 498-507.

[Foss_1983] Fossum J. G., Mertens R. P., Lee D. S. & Nijs J. F. Carrier recombination and lifetime in highly doped silicon. 1983, Solid-State Electronics,26(6), 569-576.

[Fuka_2015] Fukasawa, R. Terahertz Imaging: Widespread Industrial Application in Non-destructive Inspection and Chemical Analysis. 2015, IEEE Transactions on Terahertz Science and Technology, vol. 5, no 6, p. 1121-1127.

[Ghos_2010] Ghosh S., Marc F., Maneux C., Grandchamp B., Koné G. A., & Zimmer T. Thermal aging model of inp/ingaas/inp dhbt. 2010, Microelectronics Reliability,50(9), 1554-1558.

[Ghos_2011] Ghosh S., Grandchamp B., Koné G. A., Marc F., Maneux C., Zimmer T., Nodjiadjim V., Riet M., Dupu, J-Y & Godi, J. Investigation of the degradation mechanisms of InP/InGaAs DHBT under bias stress conditions to achieve electrical aging model for circuit design. 2011, Microelectronics Reliability, 51(9), 1736-1741.

[Gogi_2000] Gogineni, U., Cressler J. D., Niu, G., & Harame, D. L.. Hot electron and hot hole degradation of UHV/CVD SiGe HBT's. IEEE Transactions on electron devices, 47(7), 1440-1448, 2000.

[Gran_2007] Grandchamp B. Etude des mécanisme de degradation dans les transistors bipolaires à hétérojonction InP/GaAsSb/InP utilizes dans les circuits de commande des systèmes de communication optique 40-80 Gbits/s. Thesis université de Bordeaux 1, 2007

[Gras_2003] Grasser T., Tang T.-W., Kosina H. & Selberherr S., A review of hydrodynamic and energy-transport models for semiconductor device simulation. 2003, Proc. IEEE, vol. 91, no. 2, pp. 251-274.

[Gumm_1969] Gummel H. K., On the definition of the cutoff frequency fT, Proceedings of the IEEE, vol. 57, no. 12, pp. 2159ï 2159, 1969.

[Hein_2010] Heinemann B., Barth R., Bolze D., Drews J., Fischer G. G., Fox A., Fursenko O., Grabolla T., Haak U., Knoll D., Kurps R., Lisker M., Marschmeyer S., Rucker H., Schmidt D., Schmidt J., Schubert M. A., Tillack B., Wipf C., Wolansky D., & Yamamoto Y. SiGe HBT technology with fT/fmax of 300GHz/500GHz and 2.0 ps CML gate delay, 2010 IEEE IEDM International, pp. 30.5.1ï 30.5.4.

[Hoog_1969] Hooge F. N. 1/ä noise is no surface effect. 1969, Physics letters A, 29(3), 139-140.

[Hout_2004] Houtsma V. E., Chen J., Frackoviak J., Hu T., Kopf R. F., Reyes R. R., Tate A., Yang Y., Weimann N. G. & Chen Y. K. Self-heating of submicrometer InP-InGaAs DHBTs. 2004 IEEE Electron Device Letters, 25(6), 357-359.

[Hu_1992] Hu C. 1ʉ Reliability Simulation. 1992, IEEE Journal of Solid-State Circuits,27(3).

[Huan_1993] Huang C. J., Grotjohn T. A., Sun C. J., Reinhard D. K., & Yu C. C. Temperature dependence of hot-electron degradation in bipolar transistors. 1993, *IEEE Transactions on Electron Devices*, *40*(9), 1669-1674.

[Huet_1996] Hueting R. J., Slotboom J. W., Pruijmboom A., de Boer W. B., Timmering C. E. & Cowern N. E. On the optimization of SiGe-base bipolar transistors. 1996, IEEE Transactions on Electron Devices, 43(9), 1518-1524.

[Ighi_2012] Ighilahriz S., Cacho F., Moquillon L., Razafimandimby S., Blanchet F., Morelle J., Corrao N., Huard V., Garcia P., Arnaud C., Fournier, J. M. & Benech P. Reliability study under DC stress on mmW LNA, Mixer and VCO. 2012 Reliability Physics Symposium (IRPS)

[Jacq_2015] Jacquet T., Sasso G., Chakravorty A., Rinaldi N., Aufinger K., Zimmer T., Dôalessandro V. & Maneux, C. Reliability of high-speed SiGe: C HBT under electrical stress close to the SOA limit. 2015, Microelectronics Reliability, 55(9), 1433-1437.

[Jarr_1997] Jarrix S., Delseny C., Pascal F. & Lecoy G. Noise correlation measurements in bipolar transistors. I. Theoretical expressions and extracted current spectral densities. 1997, Journal of applied physics, 81(6), 2651-2657.

[Jose_2001] Joseph A., Coolbaugh D., Zierak M., Wuthrich R., Geiss P., He Z., Liu X., Orner B., Johnson J., Freeman G., Ahlgren D., Jagannathan B., Lanzerotti L., Ramachandran V., Malinowski J., Chen H., Chu J., Gray P., Johnson R., Dunn J., Subbanna S., Schonenberg K., Harame D., Groves R. Watson K., Jadus D., Meghelli M.& Rylyakoc A. A 0.18 εm BiCMOS technology featuring 120/100 GHz (f T/f MAX) HBT and ASIC-compatible CMOS using copper interconnect. 2001, Bipolar/BiCMOS Circuits and Technology Meeting, pp. 143-146.

[Josh_1987] Joshi S. P., Lahri R., & Lage C.. Poly emitter bipolar hot carrier effects in an advanced BiCMOS technology. IEDM Tech. Dig, 182-185, 1987

[Jung_2000] Jungemann C., Keith S., & Meinerzhagen B. Full-band Monte Carlo device simulation of a Si/SiGe-HBT with a realistic Ge profile. 2000, IEICE Trans. Electron., vol. E83-C, no. 8, pp. 1228-1234.

[Kamr_2016] Kamrani H., Jabs D., dôAlessandro V., Rinaldi N. & Jungemann C. Physics-Based Hot-Carrier Degradation Model for SiGe HBTs0 2016, Sispad.

[Kim_2007] Kim J., Sadovnikov A., Chen T., & Babcock J. Safe operating area from self-heating, impact ionization, and hot carrier reliability for a SiGe HBT on SOI. In 2007 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (pp. 230-233). IEEE.

[Knap_2010] Knapp H., Meister T. F., Liebl W., Claeys D., Popp T., Aufinger K., Schafer H., Bock J., Boguth S. & Lachner R. Static frequency dividers up to 133GHz in SiGe: C bipolar technology. 2010, IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) (pp. 29-32). IEEE.

[Knap_2012] Knapp H., Treml M., Schinko A., Kolmhofer E., Matzinger S., Strasser G., Lachner R., Maurer L. & Minichshofer J. Three-channel 77 GHz automotive radar transmitter in plastic package. 2012, IEEE Radio Frequency Integrated Circuits Symposium (pp. 119-122).

[Kone_2011] Kone G. A. Caractérisation des effets thermiques et des mécanismes de défaillance spécifiques aux transistors bipolaires submicroniques sur substrat InP dédiés aux transmissions optiques Ethernet à 112 Gb/s. Thesis of Université de Bordeaux, 2011

[Kone_2013] Koné G. A., Grandchamp B., Hainaut C., Marc F., Labat N., Zimmer T., Nodjiadjim V., Riet M., Dupuy J.-Y., Godin J., & Maneux C. Submicrometer InP/InGaAs DHBT Architecture Enhancements Targeting Reliability Improvements. 2013, IEEE Transaction on Electron Devices, vol. 60, n. 3, pp. 1068-1074.

[Kraf_2005] Kraft J., Kraft D., Loffler B., Jauk H., & Wachmann E. Usage of HBTs beyond BVCEO. In Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting, 2005. pp. 33-36.

[Laba_2004] Labat N., Malbert N., Maneux C., & Touboul A. Low frequency noise as a reliability diagnostic tool in compound semiconductor transistors. 2004, Microelectronics Reliability, 44(9-11), 1361-1368.

[Laba_2011] Labat N., Malbert N., Maneux C., Curutchet A., & Grandchamp B., Link between low frequency noise and reliability of compound semiconductor HEMTs and HBTs. In Noise and Fluctuations (ICNF), 2011 21st International Conference on (pp. 458-463). IEEE.

[Lai_2007] Lai R., Mei X. B., Deal W. R., Yoshida W., Kim Y. M., Liu P. H., Lee J., Uyeda J., Radisic V., Lange M., Gaier T., Samoska L., & Fung A., ñSub 50 nm InP HEMT Device with Fmax Greater than 1 THz,ò in Electron Devices Meeting, 2007. IEDM 2007. IEEE International, 2007, pp. 609ï 611.

[Laks_1990] Laks D.B., Neumark G. F., & Pantelides S. T., Accurate interband-Auger-recombination rates in silicon, 1990, Physical Review B 42 (8), pp. 5176-5185.

[Lee_2006] Lee C. P., Chau F. H., Ma W., & Wang N. L. The safe operating area of GaAs-based heterojunction bipolar transistors. 2006, IEEE Transactions on Electron Devices.

[Liou_1994] Liou L. L., & Bayraktaroglu B. Thermal stability analysis of AlGaAs/GaAs heterojunction bipolar transistors with multiple emitter fingers. 1994, IEEE Transactions on Electron Devices, 41(5), 629-636.

[Lu_1989] Lu P. F. & Chen T. C. Collector-base junction avalanche effects in advanced double-poly self-aligned bipolar transistors. 1989, IEEE Transactions on Electron Devices, 36(6), 1182-1188.

[Lyer_1987] Iyer S. S., Patton G. L., Delage S. S., Tiwari S. & Stork J. M. C. Silicon-germanium base heterojunction bipolar transistors by molecular beam epitaxy. In Electron Devices Meeting, 1987 International (Vol. 33, pp. 874-876). IEEE.

[Mane_2004] Jacob-Maneux C. Etude des mechanismes de degradation des transistors bipolaire à Hétérojonction sur substrat GaAs, 1998, university of Bordeaux 1.

[Mart_2003] Martin J. C., Maneux C., Labat N., Touboul A., Riet M., Blayac S., Kahn M., & Godin J., Extrinsic leakage current on InP/InGaAs DHBTs. 2003, IEEE International Conference on Indium Phosphide and Related Materials, pp. 12-15.

[Meno_2005] Menozzi R., Barrett J. & Ersland P. A new method to extract HBT thermal resistance and its temperature and power dependence. 2005, IEEE Transactions on Device and Materials Reliability, vol.5, n°. 3, p 595-601.

[Mile_2007] Miles R., Zhang X. C., Eisele H., & Krotkus A. Terahertz frequency detection and identification of materials and objects. 2007, Springer Science & Business Media.

[Moen_2012]. Moen K. A, Chakraborty P. S., Raghunathan U. S., Cressler J. D. & Yasuda H., Predictive physics-based TCAD modeling of the mixed-mode degradation mechanism in SiGe HBTs. 2012, IEEE Trans. Electron Devices, vol. 59, no. 11, pp. 2895-2901.

[Moha_2000] Mohammadi S., Pavlidis D., & Bayraktaroglu B. Relation between low-frequency noise and long-term reliability of single AlGaAs/GaAs power HBTs. 2000, IEEE Trans. Electron Devices, vol. 47, no. 4, pp. 677ï 686.

[Moor_1975] Moore G. E.. Progress in digital integrated electronics. 1975, Electron Devices Meeting. p. 11-13.

[Morv_online] MORV project https://morv-project.eu/wordpress/

[Muk1_2016] Mukherjee C., Jacquet T., Chakravorty A., Zimmer T., Boeck J., Aufinger K. & Maneux C., Low-Frequency Noise in Advanced SiGe:C HBTs Part I: Analysis. 2016, IEEE Transaction on Electron Dev, vol. 63, n.9, pp. 3649-3656.

[Muk2_2016] Mukherjee C., Jacquet T., Chakravorty A., Zimmer T., Boeck J., Aufinger K. & Maneux C. Investigation of Low-Frequency Noise in Advanced SiGe:C HBTs Part II: Correlation and Modeling. 2016, IEEE Transaction on Electron Dev, vol. 63, n.9, pp 3657-3662.

[Muk3_2016] Mukherjee C., Ardouin B., Dupuy J.Y., Nodjiadjim V., Riet M., Zimmer T., Marc F. & Maneux C. Reliabillity-aware circuit design for terahertz communication. 2016, IEEE Transactions on Device and Materials Reliability, under publication.

[Murt_2002] Murty M. R., Newton K. M., Sweeney S. L., Sheridan D. C., & Harame D. L. Implementation of a scalable and statistical VBIC model for large-signal and intermodulation distortion analysis of SiGe HBTs. 2002 IEEE MTT-S International.

[Neug_1997] Neugroschel A., Sah C. T., Carroll M. S., & Pfaff K. G. Base current relaxation transient in reverse emitter-base bias stressed silicon bipolar junction transistors. 1997, IEEE Transactions on Electron Devices, 44(5), 792-800.

[Niu_1998] Niu G., Cressler J. D., & Joseph A. J., Quantifying Neutral Base Recombination and the Effects of Collectorï Base Junction Traps in UHV/CVD SiGe HBT. 1998, IEEE Transaction on Electron Devices, vol. 45, n. 12, pp. 2499-2504.

[Nodj_2009] Nodjiadjim V. Transistor bipolaire à double hétérojonction submicronique InP/InGaAs pour circuits neméiques ou mixtes ultra-rapides. 2009, Thesis université de Lille 1.

[Ojef_2010] Ojefors E. & Pfeiffer U. R. A 650GHz SiGe receiver front-end for terahertz imaging arrays. 2010, IEEE International Solid-State Circuits Conference-(ISSCC).

[Ojef_2012] Ojefors E., Heinemann B., & Pfeiffer U. R. Subharmonic 220-and 320-GHz SiGe HBT receiver front-ends. 2012, IEEE Transactions on Microwave Theory and Techniques, vol. 60, no 5, p. 1397-1404.

[Paas1_2001] Paasschens J. C. J., Kloosterman W. J., & Havens R. J., Modeling two SiGe HBTs specific features for circuit simulation. 2001, IEEE BCMT, pp. 38-41.

[Paas2_2001] Paasschens J. C. J., vd Toorn R., & Kloosterman W. J. The Mextram bipolar transistor model. 2001, Small.

[Prin_1989] Prinz E. J., Garone P. M., Schwartz P. V., Xiao X., & Sturm J. C. The effect of base-emitter spacers and strain-dependent densities of states in Si/Si1-xGex/Si heterojunction bipolar transistors. 1989, Proc. IEDM, pp. 639-642,.

[Quay_2000] Quay R., Moglestue C., Palankovski V., & Selberherr S. A temperature dependent model for the saturation velocity in semiconductor materials. 2000, Mat. Sci. Semic. Proc. vol. 3, pp. 149-155;

[Rick_2001] Rickelt M., Rein H. M., & Rose E. Influence of impact-ionization-induced instabilities on the maximum usable output voltage of Si-bipolar transistors. 2001, IEEE Transactions on Electron Devices, 48(4), 774-783.

[Rieh_2009] Rieh J. S., & Kim D. H. An overview of semiconductor technologies and circuits for terahertz communication applications. 2009, IEEE Globecom Workshops, p. 1-6.

[Rina_2005] Rinaldi N., & d'Alessandro V. Theory of electrothermal behavior of bipolar transistors: Part I-single-finger devices. 2005, IEEE Transactions on Electron Devices, 52(9).

[Rina_2006] Rinaldi N., & d'Alessandro V. Theory of electrothermal behavior of bipolar transistors: Part III-Impact ionization. 2006, IEEE Transactions on Electron Devices, 53(7), 1683-1697.

[Ruck_2010] Rucker H., Heinemann B., Winkler W., Barth R., Borngraber, J., Drews, J., Fischer G. G., Fox A., Grabolla T., Haak U., Knoll D., Korndorfer F., Mai A., Marschmeyer S., Schley P., Schmidt D., Schmidt J., Schubert M. A., Schulz K., Tillack B., Wolansky D. & Yamamoto Y. A 0.13 SiGe BiCMOS Technology Featuring f/f of 240/330 GHz and Gate Delays Below 3 ps. 2010, IEEE Journal of Solid-State Circuits, 45(9), 1678-1686.

[Ruck_2012] H. Rucker, B. Heinemann, and A. Fox, SiGe BiCMOS Technologies for Applications above 100 GHz. 2012, IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), pp. 1ï 4. [45] P.

[Sanc_2003] Sanchez J. E., Bosman G., & Law M. E. Two-dimensional semiconductor device simulation of trap-assisted generation-recombination noise under periodic large-signal conditions and its use for developing cyclostationary circuit simulation models. 2003, IEEE Transactions on Electron Devices, 50(5), 1353-1362.

[Sank_2005] Sankaran, S. Schottky barrier diodes for millimeter wave detection in a foundry CMOS process. 2005, IEEE Electron Device Letters, 26(7), 492-494.

[Sass_2010] Sasso G., Matz G., Jungemann C. & Rinaldi N., Analytical Models of Effective Dos, Saturation Velocity and High-Field Mobility for SiGe HBTs Numerical Simulation. 2010, International Conference on Simulation of Semiconductor Processes and Devices, SISPAD pp. 279-282.

[Sass1_2014] Sasso G., Maneux C., Boeck J., dôAlessandro V., Aufinger K., Zimmer T. & Rinaldi N. Evaluation and Modeling of Voltage Stress-Induced Hot Carrier Effects in High-Speed SiGe HBTs. 2014, IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), p. 1-4.

[Sass2_2014] Sasso G., Rinaldi N., Fischer G. G., & Heinemann B. Degradation and recovery of high-speed SiGe HBTs under very high reverse EB stress conditions. 2014, IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM).

[Schr_1993] Schroter M., Friedrich M. & Rein H.-M. A generalized integral charge-control relation and its application to compact models for silicon-based HBT's. 1993, IEEE Transactions on electron devices, vol. 40, no 11, p. 2036-2046.

[Schr_2010] Schroter M. & Chakravorty A. Compact hierarchical bipolar transistor modeling with HICUM. 2010, World Scientific, Singapore, ISBN 978-981-4273-21-3.

[Schr1_2011] Schroter M., Wedel G., Heinemann B., Jungemann C., Krause J., Chevalier P., & Chantre A. Physical and electrical performance limits of high-speed SiGeC HBTsð Part I: Vertical scaling. 2011, IEEE Transactions on Electron Devices, 58(11), 3687-3696.

[Schr2_2011] Schroter M., Krause J., Rinaldi N., Wedel G., Heinemann B., Chevalier P., & Chantre A. Physical and electrical performance limits of high-speed Si GeC HBTsð Part II: Lateral scaling. 2011, IEEE Transactions on Electron Devices, 58(11), 3697-3706,

[Song_2011] Song H. J., & Nagatsuma T. . Present and future of terahertz communications. 2011, IEEE Transactions on Terahertz Science and Technology.

[Suli_2005] Sulima P.-Y. Contribution à la modélisation analytique tridimentionnelle de lâauto-échauffement dans les transistors bipolaire à hétérojonction de type Si/SiGe. 2005, Thesis université de Bordeaux 1.

[Taba_2015] Tabata H. Application of Terahertz Wave Technology in the Biomedical Field. 2015, IEEE Transactions on Terahertz Science and Technology, vol. 5, no 6, p. 1146-1153.

[TCAD_manual] Synopsys TCAD Software, Release 2011.09.

[Tutt_1995] Tutt M. N., Pavlidis D., Khatibzadeh A. & Bayraktaroglu B. Low frequency noise characteristics of self-aligned AlGaAs/GaAs power heterojunction bipolar transistors. 1995, IEEE Transactions on Electron Devices, 42(2), 219-230.

[Urte_2010] Urteaga, M., Seo, M., Hacker, J., Griffith, Z., Young, A., Pierson, R., Rowell P., Skalare A. & Rodwell, M. J. W. InP HBT integrated circuit technology for terahertz frequencies. *2010 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*

[Wach_1988] Wachnik R. A., Bucelot T. J., & Li G. P. Degradation of bipolar transistors under high current stress at 300 K. 1988, Journal of applied physics,63(9), 4734-4740.

[Whor_1955] McWhorter A. L., 1/f noise and related surface effects in germanium. 1955, Thesis of Massachusetts Institute of Technology.

[Wier_2015] Wier B. R., Raghunathan U. S., Chakraborty P. S., Yasuda H., Menz P., & Cressler J. D.. A Comparison of Field and Current-Driven Hot-Carrier Reliability in NPN SiGe HBTs. 2015, IEEE Transactions on Electron Devices, 62(7), 2244-2250.

[Wier_2016] Wier B. R., Green K., Kim J., Zweidinger D. T., & Cressler J. D. A Physics-Based Circuit Aging Model for Mixed-Mode Degradation in SiGe HBTs, 2015, IEEE Transactions on Electron Devices, Vol 63, n°8, pp. 2987 ï 2993

[Zhan_2002] Zhang G., Cressler J. D., Niu G., & Joseph A. J. A new" mixed-mode" reliability degradation mechanism in advanced Si and SiGe bipolar transistors. 2002, IEEE Transactions on Electron Devices, 49(12), 2151-2156.

[Zhen_2009] Zheng R., Velamala J., Reddy V., Balakrishnan V., Mintarno E., Mitra S., Krishnan S. & Cao Y. Circuit aging prediction for low-power operation. 2009, IEEE Custom Integrated Circuits Conference, p. 427-430.

[Zhu_2005] Zhu C., Liang Q., Al-Huq R. A., Cressler J. D., Lu Y., Chen T., Joseph A. J. & Niu G. Damage mechanisms in impact-ionization-induced mixed-mode reliability degradation of SiGe HBTs. 2005, IEEE Trans. Electron Dev., vol. 5, no. 1, pp. 142-149.