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# Design characterization and implementation of an integrated CMOS driver circuit for GaN components

Van-Sang Nguyen

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## THÈSE

Pour obtenir le grade de

### **DOCTEUR DE LA COMMUNAUTÉ UNIVERSITÉ GRENOBLE ALPES**

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Présentée par

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Co-encadrant par **Pierre LEFRANC**

préparée au sein du **Laboratoire de Génie Electrique de Grenoble (G2ELab)**

dans l'**École Doctorale Electronique, Electrotechnique, Automatique et Traitement du Signal (EEATS)**

## **Conception, caractérisation et mise en œuvre d'un circuit intégré type driver en CMOS pour composants GaN**

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Prepared at **Grenoble Electrical Engineering Laboratory (G2ELab)**

Under the **Doctoral School of Electronics, Electrical Engineering, Automatics and Signal Treatment (EEATS)**

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To All

“Our life amounts to no more than one drop in a limitless ocean.

Yet what is any ocean, but a multitude of drops?”

- David Mitchell

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## List of Acronyms

Si	Silicon
WBG	Wide Band Gap
GaN	Gallium Nitride
GaN HEMT	Gallium Nitride High-Electron-Mobility Transistor
SiC	Silicon Carbide
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
BJT	Bipolar Junction Transistor
SCR	Silicon Controlled Rectifier
GTO	Gate Turn-Off Transistor
IEGT	Injection Enhanced Gate Transistor
UPS	Uninterruptible Power Supply
HVDC	High-Voltage Direct Current
FACT	Flexible Alternating Current Transmission
SMPS	Switching Mode Power Supply
EMI	Electro-Magnetic Interference
EMC	Electro-Magnetic Compatibility
CMTI	Common Mode Transient Immunity
LS	Low Side
HS	High Side
HT	High Temperature
HF	High Frequency
HEV / EV	Hybrid Electric Vehicle / Electric Vehicle
EMRC	Electro Magnetic Resonance Coupler

## List of Acronyms

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DAB	Dual Active Bridge
SAB	Single Active Bridge
MMC	Modular Multi-Level Converter
PDK	Process Design Kit
LTH	Low-to-High (delay)
HTL	High-to-Low (delay)
I2C	Inter-Integrated Circuit (communication protocol)
TX	Transmitter
RX	Receiver
C+RX	Coreless Transformer+ Receiver
Ext	External Isolator (of the power supply)
COM	Communication
PWM	Pulse Width Modulation
AZS	Auto-Zero-Skew
MEGaN	Module Electronique GaN (Project)

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## General Introduction

Recently, the 21<sup>st</sup> yearly session of Conference of the Parties (COP 21, December 2015, in Paris) have made a decision on the limiting of the global warming less than 2 degree Celsius (2<sup>o</sup>C) compared to pre-industrial level. Eventually, the parties will also effort to limit the increase to 1.5 °C. The 1.5 °C goal will require zero emissions sometime between 2030 and 2050 [1], [2]. In this context, many researchers have been engaged to pursue the efficient energy use; the low-carbon energy and the renewable energy are the key points on this transition.

In the renewable energy systems, the power electronics systems are considered critical elements. Similarly, the aeronautic applications, more electric aircrafts are intended to reduce on board weight and increase the efficiency to actuators, saving important quantities of energy. Also, in the automotive applications, the introduction of electrical appliance must be balanced by extremely efficient operations. In general, the power electronics systems are always required to be faster, more robust and more compact, operating in harsh environments, EMI and/or temperature dependent. Several researches are deployed to achieve these requirements which deal with design, control, integration and semiconductor materials.

Today, the conventional power electronics semiconductor counter parts based on Si reach their theoretical limitations. Working on the new generation of the semiconductor materials is more essential than ever. The novel components based on GaN, SiC and even coming up Diamond materials are becoming the key factor for the future of the power electronics breakthrough. Because, these semiconductor devices are faster, can perform at higher temperatures and under a better surface  $R_{DSon}$  tradeoff ratio, because there are a lot of improvements of these WBG components during last decade which make them more and more implemented in advanced power electronics systems.

However, high speed power components introduce fast  $dv/dt$  and high  $di/dt$  voltage and current transients when these devices switch. These are the origins of most of the EMI perturbations in the upper frequency range, from several MHz up to ten and even hundreds of MHz.

As a part of MEGaN project, this research focuses on the gate driver design and optimization for the WBG components, especially for implementation in a low side high side GaN power components configuration in order to optimize the EMI management in harsh environment. In Chapter I, the negative effects of the high  $dv/dt$  through the gate driver circuit as the conducted EMI perturbations are detailed and then the potential solutions are described. In this chapter, we understand that the problems of the gate driver circuit are not only located at the system level but also at the component level. Hereby, the proposed solutions are stretched out from the conceptual requirements of the gate driver system to the requirements of the new components of the gate driver. In the next chapters, the solutions are detailed with the validations to overcome the problems of the gate driver side-by-side.

Chapter II shows how the conducted EMI propagation paths are redefined by working on the system level. In this chapter, a novel architecture is depicted for optimizing the conducted EMI perturbation flowing from the power parts to the gate driver circuit when high  $dv/dt$  occurs. This chapter pushes also to the extreme optimization of the system by improving the interconnections of the circuit. Moreover, to minimize the negative impacts of the parasitic elements between the gate driver and the component to drive, the devices of the gate driver must be brought close to the WBG power

components where the temperature is critical and to be taken into account; the recommendations talk about which devices should be interconnected close to the power devices and “where”.

Also, in this chapter, the driver circuitry conducted EMI problems in more complex systems as the power electronics system with power transistors in series connection or MMC systems are investigated. In order to validate the solution at the system level, simulations and experiments are implemented, results are reported and analyzed.

To tackle the recommendations of Chapter II, the works of Chapter III at the components’ level are presented in order to minimize the conducted EMI propagation paths at their sources by optimizing the parasitic capacitances of the devices. The temperature becomes critical when the gate driver is implemented as close as possible to the WBG power devices to minimize the parasitic elements. This is an important motivation to design new components for the proposed gate driver circuit implementation, adapted to the constraints of GaN components.

In this thesis, the high temperature integrated power supply of the gate driver is designed after the studies of several power supply techniques and DC/DC converter topologies. At G2ELab, three techniques of the signal transfer units from the low side to the high side of the gate driver are also developed by our team in order to fulfill the requirements of the CMTI and the high temperature operation constraint. The high temperature integrated technology XFAB XT018 PDK is made available by MEGaN project for designing these elements.

Finally, Chapter IV shows a panorama of the proposed gate driver architecture with the high temperature components. In this chapter, WP3 partners (Work Package 3) introduce a dedicated work on the gate driver circuitry adapted to answer new constraints of GaN components implementations. The final ambition of WP3 is to implement the final version of a “fully” integrated gate driver and associated circuitry allowing to perform and to drive in the best manner advanced power device under strong  $dv/dt$  (50V/ns for instance) and under high temperature (up to 250°C at best). Chapter IV describes the specifications and depicts the schematic for implementation of the gate driver.

## **Chapter I**

### **Gate driver circuit for high speed power devices with improved EMI management in harsh environment:**

#### **Introduction and motivations**

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## Abstract

*In order to present a gate driver circuit for the high speed power devices with EMI management in harsh environment, the beginning point of this research is to present the problems of the high speed power devices – the conducted perturbations on the driver circuit.*

*In this chapter, a general introduction on EMI (Electro-Magnetic Interference) is presented. Hence this thesis focuses is on a specific gate driver for a high side – low side switching cell implementation. The gate driver circuit is dedicated for high speed power devices as wide band-gap components. The harsh environment issue is considered as the high temperature and the common mode transient immunity for strong  $dv/dt$ .*

*The sequence of the works is from the conceptual requirements of the system to the component specifications. Finally, the ending point is to show a fully integrated power module in order to overcome the conducted EMI problems which are presented as the orientations of this work.*

## I.1 The state-of-art of the wide-band gap power components and the challenges for the gate drivers

### I.1.a New specifications of the wide-band gap devices

Today, the power electronics system takes one of the most important roles in the renewable energy systems. The power electronics conversion circuits are the main pathways for the renewable energies to reach the loads, they are so-called the power electronics energy transfer systems.

Power semiconductor devices are used widely in power electronics energy transfer systems, especially in the renewable energy systems. An impressive development has been made on the technology of power semiconductors since the 1970s [3],[4], [5].

Fig.I.1 shows the application areas of classical Si power semiconductor devices. MOSFETs (Metal-Oxide Semiconductor Field-Effect Transistor) are used for high-frequency applications up to 1 MHz but at low power, less than 10kW. IGBTs (Insulated Gate Bipolar Transistor) are operated at lower switching frequencies but higher power, up to 1MW. And SCRs (Silicon Controlled Rectifier) and GTOs (Gate Turn-Off Thyristor) are mainly used for high-power applications up to 100MW. For medium-power applications such as uninterruptible power supply (UPS), automotive, and robots, IGBT or MOSFET power modules, are constructed with series and parallel connection of power devices inside a package.

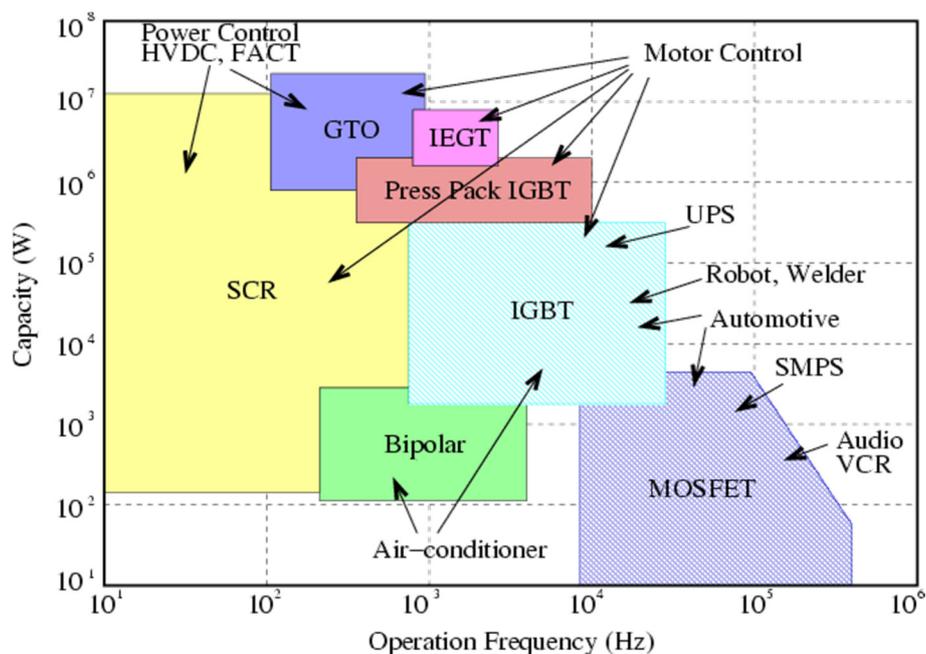


Fig.I.1 Application areas of classical discrete power semiconductors [6]

Concurrently, the classic silicon (Si) power components have reached their theoretical physical limitations, especially in terms of  $R_{DS(on)}/cm^2$  and temperature [7]. The wide band-gap (WBG) semiconductors such as the Gallium Nitride (GaN), the Silicon Carbide (SiC), and the Diamond are excellent candidates to replace the Si-based counterparts in the coming years.

"Wide-band-gap" refers to "high-different-energy-level" which makes the electrons of the semiconductor switch between the two energy levels as in Fig.I.2. There are two bands: the conduction band and the valence band. Between these two bands, the electrons do not exist, it is called the forbidden band.

In the valence band, the electrons have low energy of  $E_v$  and are not able to participate to current conduction. If they are excited externally, they can move to the conduction band, where the electrons are able to participate to current conduction. For an electron to move to the conduction band, it needs an amount of energy  $E_g = E_c - E_v$ , where  $E_g$  is so-called the band-gap.

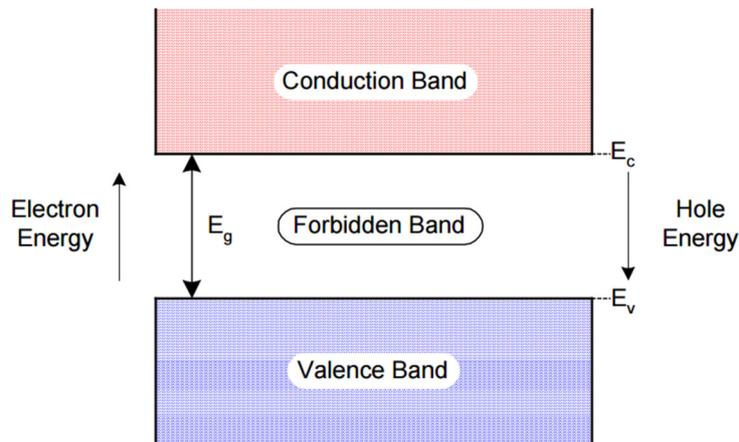


Fig.I.2 Simplified energy band of the semiconductor [8]

Silicon has a band-gap of  $E_{g,Si} = 1.12$  eV, this amount of energy is fairly small which is interesting to lower the energy needs to make the material conductive, but can also occur naturally when the material is heated up or heats up for example. This limit for Si-based devices is the reason why the operational maximum temperature is between 125°C and 250°C, depending mainly on material doping levels. Above this temperature, the electrons will switch between the energy levels without any controlled action. WBG materials typically have band-gaps on the order of 3 to 5.5 eV ( $E_{g,SiC} = 3.26$  eV,  $E_{g,GaN} = 3.45$  eV,  $E_{g,SiC} = 5.45$  eV ), allowing them to operate at higher temperatures typical above 300°C [9], [10], [11], [12]. In addition, most of them also have a much higher critical electrical field, in the order of ten times of silicon material (even 30 times for the Diamond), with comparable electron mobility. These very attractive properties enable to size down the drift region of the devices while increasing the doping levels which in turn decreases drastically the  $R_{DSon}/cm^2$  of the components. Nowadays, researchers are trying to combine these properties in order to produce devices able to operate at higher voltage and current ratings, making them highly suitable for high power, high power density applications such as portable electrical system, electrical mobility (EV, Train, buses and others), and more electrical aircraft.

Table.I.1 shows the main physical characteristics of Si and WBG materials [8], [13], [14], [15].

Table.I.1 Comparison between Si and WBG

Property	Si	4H - SiC	GaN	Diamond
Ban-gap, $E_g$ (eV)	1.12	3.26	3.45	5.45
Dielectric constant	11.9	10.1	9	5.5
Electric breakdown field (kV/cm)	300	2200	2000	10000
Electron mobility ( $cm^2/V.s$ )	1500	1000	1250	2200
Hole mobility ( $cm^2/V.s$ )	600	115	850	850
Thermal conductivity (W/cm.K)	1.5	4.9	1.3	22
Saturated electron drift velocity, $v_{sat}$ ( $\times 10^7$ cm/s)	1	2	2.2	2.7

Some of the advantages of WBG are:

- With the same breakdown voltage, the drift region thickness of WBG can be smaller, its doping level higher, which lead to have a lower on-resistance per  $\text{cm}^2$  means lower conduction losses per  $\text{cm}^2$  or lower surface at constant on-resistance.
- WBG semiconductor-based power devices can operate at high temperatures
- Because WBG devices can be unipolar with outstanding characteristics, they can operate at higher switching frequencies (from several 100kHz up to several MHz)

In Fig.I.3, if some materials and devices are still at a primitive development stage, the GaN and SiC devices are evaluated as the excellent WBG devices of today by YOLE development in 2015 [16].

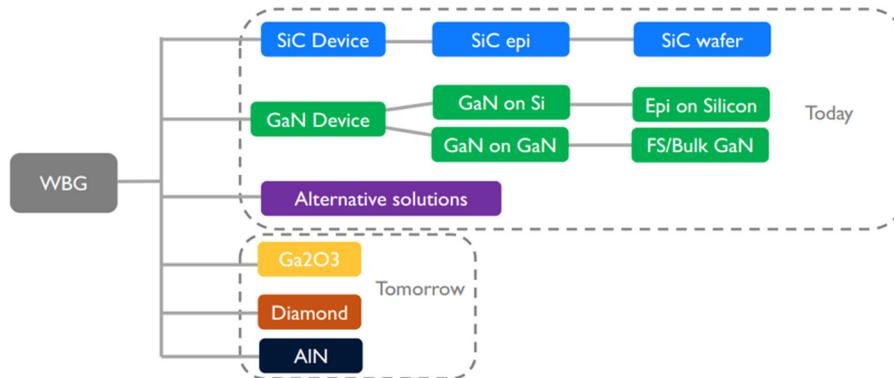


Fig.I.3 Overview of WBG devices in 2015 [16]

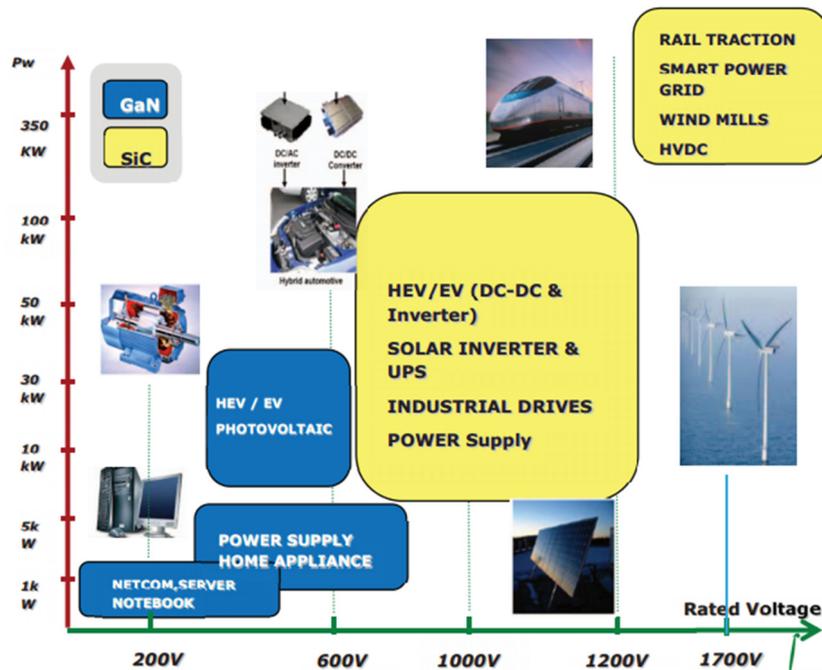


Fig.I.4 Market positioning of SiC and GaN Power devices [17]

Fig.I.4 shows the market positioning of GaN and SiC components presented by ST-Microelectronics in 2015 [17]. According to this article, SiC devices dominate applications at high power, high temperature and high voltage for applications such as the railway traction, the smart power grid, and the wind turbines. GaN power devices play a larger role in the low and medium voltage ratings.



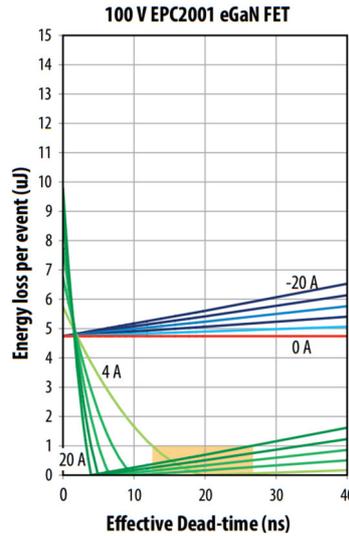


Fig.I.6 Critical dead-time management of GaN EPC – 100V EPC2001 eGaN FET [20]

The other hot topic for the gate driver is related to the EMI management, the  $dv/dt$  immunity, and then the parasitic inductances loops of the gate drivers that need to be reduced. The conducted EMI problem, the parasitic capacitances need to be minimized or the propagation pathways need to be routed in a way that the high noisy currents do not pass through the driver circuit when strong  $dv/dt$  occurs.

A half bridge with high side and low side GaN transistors (GaN transistors from GaN-System Company) which are driven by two gate drivers, a high side and a low side gate driver. Study the drain-source voltage of the transistor, Fig.I.7 shows the measured 10 ns of rise time for turn-on and 6ns of the fall time at 30 A. These figures present also  $dv/dt$  amplitude ranging from of 40 V/ns during the rise time to 70 V/ns during the fall time. The spike voltages on the Gate to Source signal are 0.8 V and 2 V during turn-on and turn-off, respectively, which demonstrates the extreme sensitivity of the gate signal with respect to the power side, even with a very nice packaging and interconnections of the switching cell. If these ripple voltages exceed the threshold voltage, the short circuit may occur within the half-bridge [21].

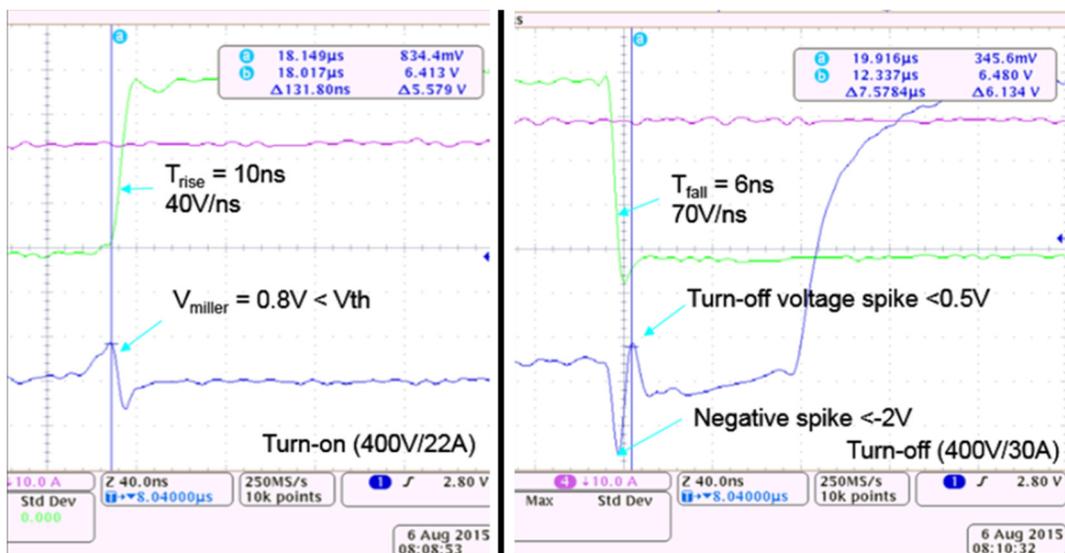


Fig.I.7 Pulse test switching waveforms turn-on and turn-off of GaN-System evaluation board [21]

Another GaN 600V normally-off device in [22] has commuted with the maximum slew rate of 240V/ns in Fig.I.8. An extreme  $dv/dt$  of 450V/ns of GaN device has been measured in [23]: Fig.I.9.

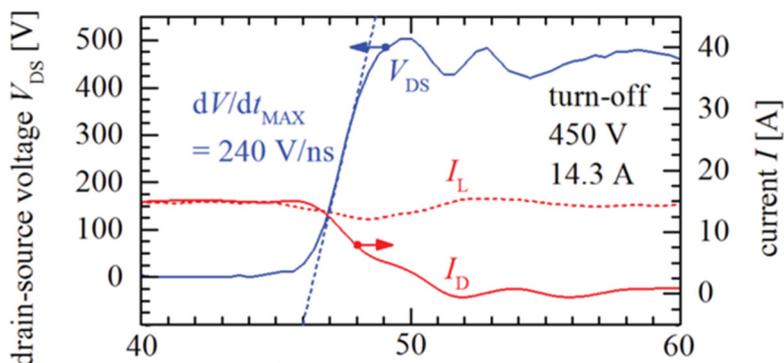


Fig.I.8 Inductive-load turn-off transition at 450 V, 14.3 A [22]

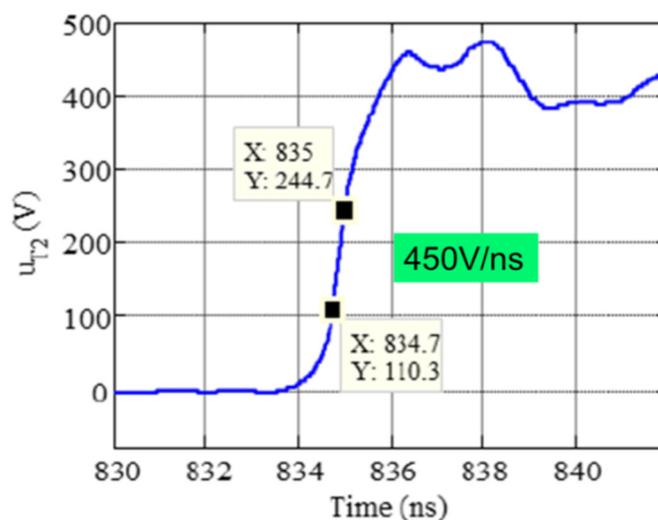


Fig.I.9 600V IFX Normally-Off GaN GIT with  $dv/dt$  up to 450V/ns [23]

The negative impact of  $dv/dt$  on the driver circuit is theoretically investigated in the next section. In these research and experimental implementations, many efforts are carried out on layout and device implementation to switch these extreme high speed devices. EMI optimization in the gate driver circuit of GaN power devices is a huge issue.

In this chapter, the driver circuit's problems are studied, evaluated and solutions are proposed.

### I.1.c MEGaN (Module Electronique GaN) Project

In France, WBG devices became a hot research trend over the last decade. This PhD dissertation is about the gate driver circuits in the context of GaN device H-bridges and GaN transistor to GaN transistor commutations. MEGaN (Module Electronique GaN) project involves industrial partners and also academic partners:

RENAULT, SCHNEIDER, SAFRAN, VALEO, STMicroelectronics, GRISET, LOUPOT, TRONICO, SERMA, ID-MOS, PRIMES Tarbes, LETI, ARMINES, G2ELAB, AMPERE, IFSTTAR, SATIE.

The aim is to achieve industrially demonstrated GaN based advanced converters in three application areas: *the automotive, the aeronautics and the energy management*

## I.2 The need of EMI management on the driver circuitry with the evolution of high speed power components

Fig.I.10 shows the overview of the MEGaN project, the principal applications and the main interests of the project leaders:

- SAFRAN: reverse acting actuators
- VALEO and RENAULT: inverters for power train and battery management
- SCHNEIDER: inverters for photovoltaic systems

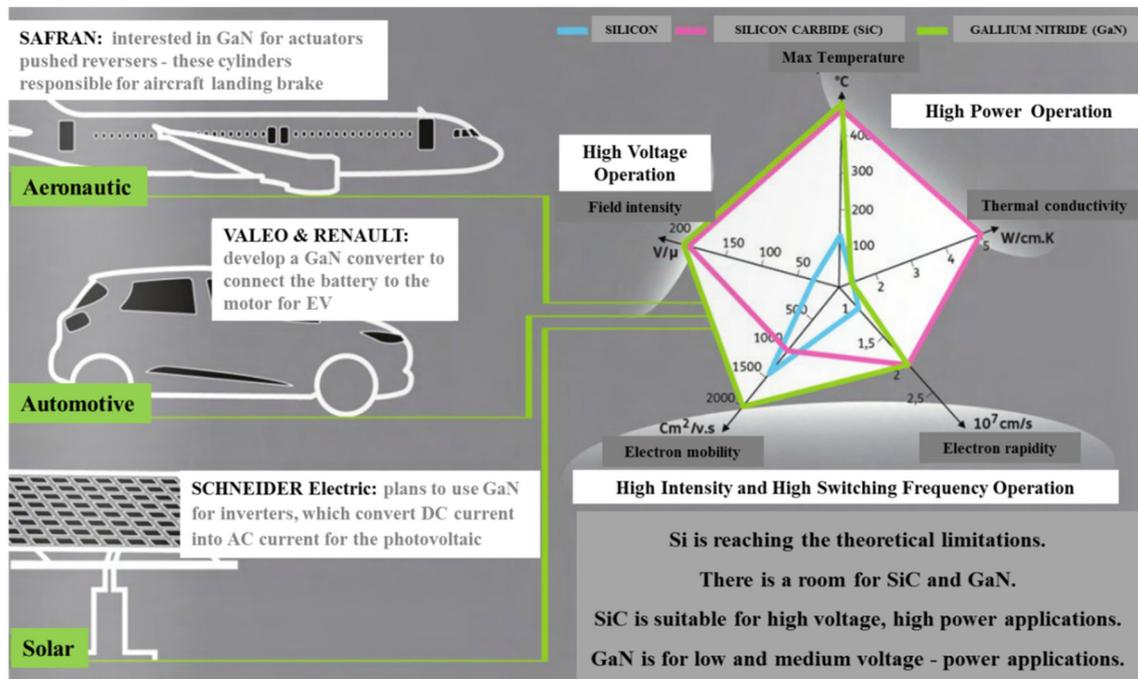


Fig.I.10 Initial context of MEGaN project, 2012 [24]

## I.2 The need of EMI management on the driver circuitry with the evolution of high speed power components

### I.2.a The EMI problems on the driver circuit

#### I.2.a-i EMI in general: source, propagation and reception

Nowadays, in aeronautic and automotive applications and in energy management systems for example, proper power electronics conversion systems require always higher efficiency, reduced system size and improved reliability. Therefore, the switching frequency of the power electronics systems is increasing constantly. High switching frequency (in MHz frequency range) and high switching speed (high voltage and current slew rates) with the parasitic elements of the circuit are the main reasons of increased EMI emissions. EMI are unwanted phenomena in the electrical systems due to electromagnetic radiations and electromagnetic conductions.

In one hand, the conducted EMI is carried out by the conductors, in another hand; the radiated EMI are produced by fields which propagate without physical contact with the conductors. As mentioned in many literatures, EMI phenomena deforms the electromagnetic field around the conductors by several effect as the skin and/or proximity effects, hysteresis losses, transients, voltage drops, electromagnetic disturbances, eddy current losses, harmonic distortion, and reduction in the permeability of the material [25],[26],[27].

EMI generation phenomena and mechanisms must be investigated in order to forecast, minimize and reduce it. Moreover, it is unavoidable to pay attention of EMI performances before making any high frequency power electronics circuit. EMI forecast and evaluation should be made during design process. Understanding electromagnetic capability of the modern devices is very important for power electronics design, where traditional viewpoints and the approximations of electrical circuit theory start to be inapplicable. The new approaches and tools are needed to understand the origin of the problems then the way to reduce or even eliminate them [28]. In Fig.I.11, the electromagnetic disturbances can be described in three steps:

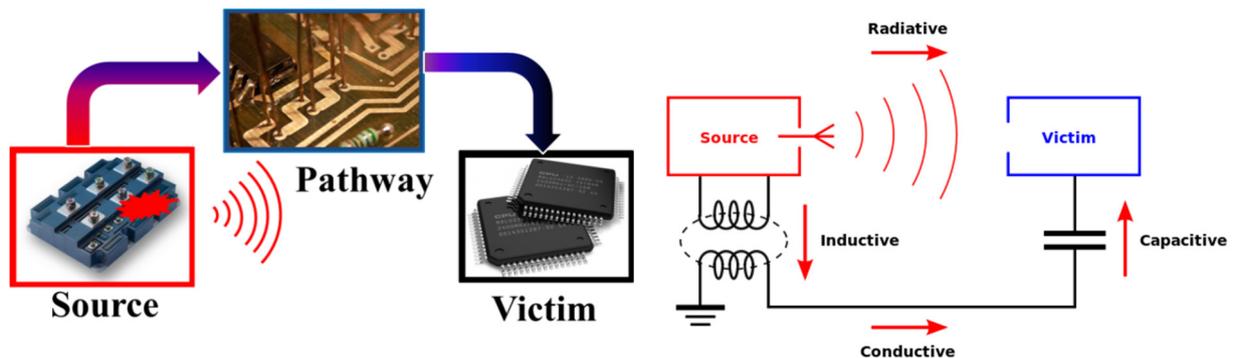


Fig.I.11 EMI from source through pathway to victim [28]

- **The source:** this is the device or equipment where the noise or disturbance is generated. The reason for this source can be a fast signal, fast rise and fall time as high voltage slew rate  $dv/dt$  and/or high current slew rate  $di/dt$ , resonance, antenna structures, wrong termination...
- **The reception unit** or so-called **the victim:** the electrical circuit which becomes influenced by the perturbations coming from the source.
- **The pathway:** the paths or medium where the disturbance is propagated from the source to the victim. The pathway could be the radiated or conductive ways as show in Fig I.11.

Several researches have been done on the conducted EMI and the radiated EMI [29] [30] [31] in a system point of view. In term of EMI conducted propagation modes, there are the common mode and the differential mode. The differential-mode noise involves the normal operation of the circuit, the noisy currents is flowing through the “usual” propagation path. While the common-mode noise does not relate to the normal operation of the circuit, this noise involves parasitic capacitors and circulates through the mechanical ground.

Fig.I.12 shows an example of the differential mode interference current and the common mode interference current in a power converter. The differential mode currents in Fig.I.12a circulate from V1 through the load then go back to V2, they do not go to the mechanical ground.

In the case of the common mode current in Fig.I.12b, it flows from the converter to the ground of the system (involving the parasitic capacitances). In high frequency systems, due to the parasitic inductance, the antenna phenomena may ruin out the proper performance of the system if the cables are not well grounded [32].

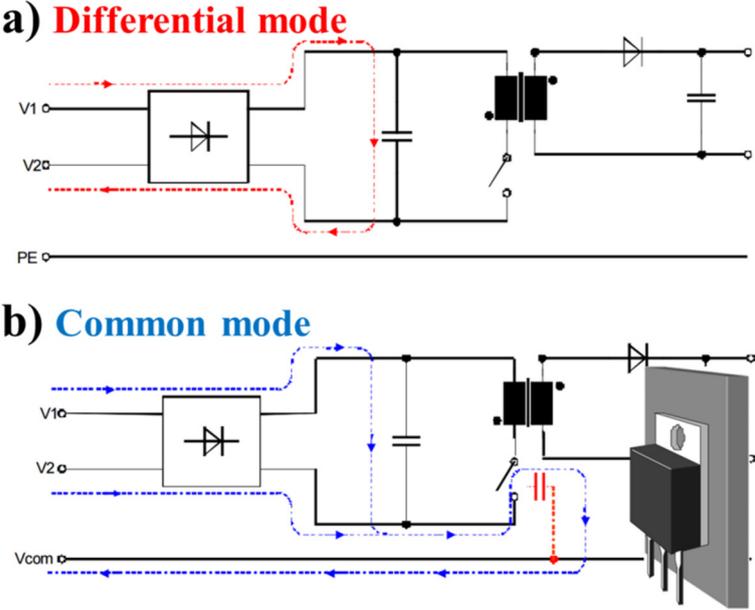


Fig.I.12 Example of the interference currents, a) Differential mode current b) Common mode current [32]

The noise sources and current paths must be first visualized and understood before determine any solutions. This research focuses on the conducted common mode current within the source and the power circuit, especially, the perturbation on the driver circuit.

As we can see in Fig.I.13, in a power electronics system, there are three loops for the common-mode current. The overall loop circulates from the source to the load through the power supply and the ground ; the output loop from the power supply to the load through the ground ; finally, the input loop from the source to the power supply through the ground [33].

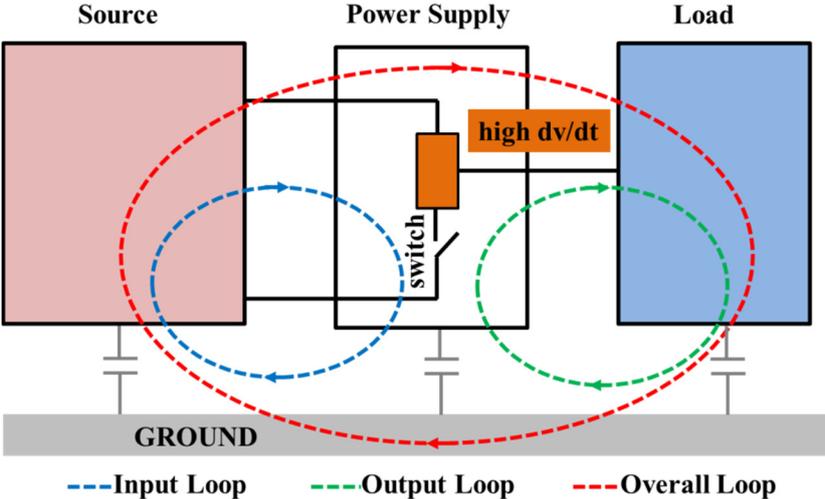


Fig.I.13 Three common mode current loops [33]

Fig.I.14 shows an example for three loops of the common mode current in an adjustable speed AC (alternative current) motor drive. In this figure, the main transformer, the AC drive, the AC motor represent the power supply, the power converter and the load respectively [34]. As in the Fig.I.13,

## I.2 The need of EMI management on the driver circuitry with the evolution of high speed power components

there are the input loop, the output loop and the overall loop. The parasitic capacitances between the devices and between the devices and the ground get involved into these loops.

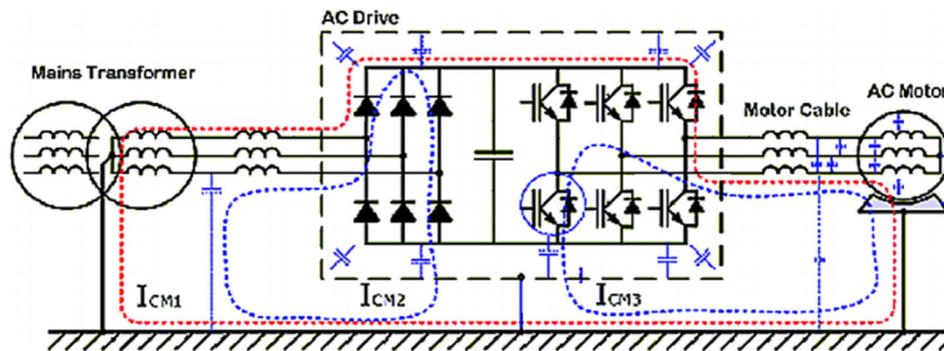


Fig.I.14 Example for common mode current paths in an adjustable speed AC motor drive application [34]

In a power electronics system, as mentioned before, increasing the switching frequency is a target. However, higher frequency or higher switching speed of power devices can cause many serious problems. The most difficult issues that we need to deal with are the conducted EMI perturbations on the driver circuit due to the high level of  $dv/dt$ . The inner loop shows the conducted EMI perturbations on the driver circuit.

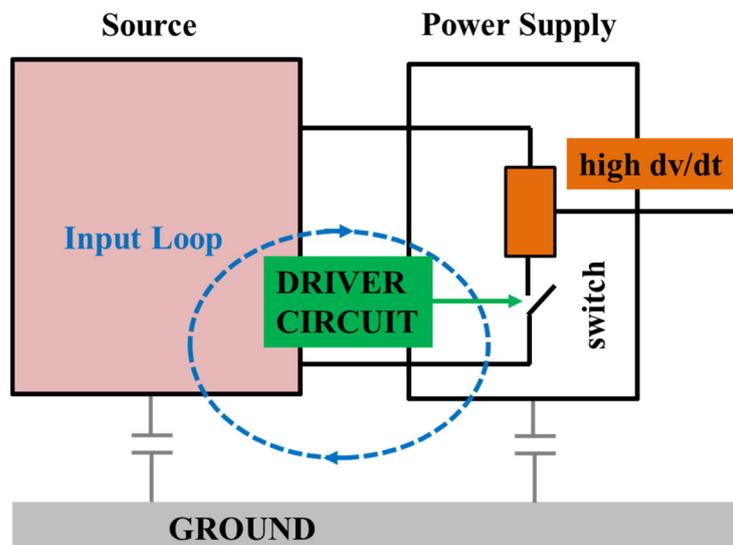


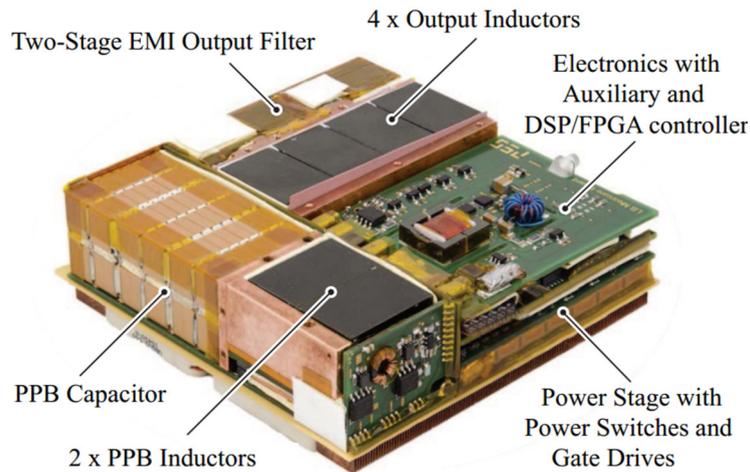
Fig.I.15 Driver within the input loop

Inside the input loop, there are the power electronics devices and its driver circuit. The driver circuit provides the control signal to the gate of the power component as shown in Fig.I.15. Once large  $dv/dt$  at the floating point are generated, large current noise via the parasitic capacitors of the driver circuit occurs inside of the driver circuit.

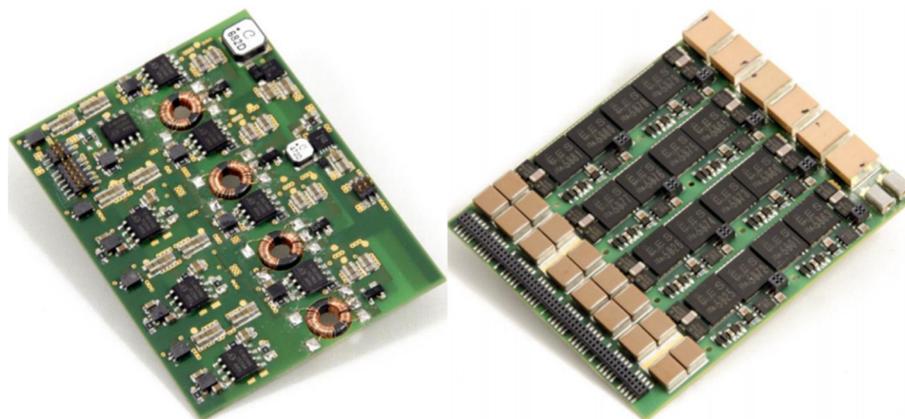
In the next part, the effects of the conducted EMI in common-mode on the driver circuit will be explained.

***1.2.a-ii How does the conducted EMI in common-mode impact on the driver circuit?***

As shown in the DC-DC power converter example in Fig.I.16, a power converter may include many switching cells, the passive devices, the filters, the cooling system and of course the driver circuits. Fig.I.17 shows the power switching cells and the driver circuit of in a power converter.



*Fig.I.16 Power converter all-in-one of 2kW with the power density of 200W/in<sup>3</sup> [35]*



*Fig.I.17 Left, gate driver circuit. Right, the switching cells of the power converter in Fig.I.6 [23]*

The control signals are generated by a pulse-width modulation by an external controller. These signals are transmitted to the power switches through the gate drivers as we can see in Fig.I.18 [36]. This figure shows the essential function blocks of a gate driver circuit in a high side – low side switching cell configuration. This gate driver circuit includes a primary side and a secondary side. Between two sides, a strong isolation is built up by the control signal isolators, and DC-DC isolated power supplies.

I.2 The need of EMI management on the driver circuitry with the evolution of high speed power components

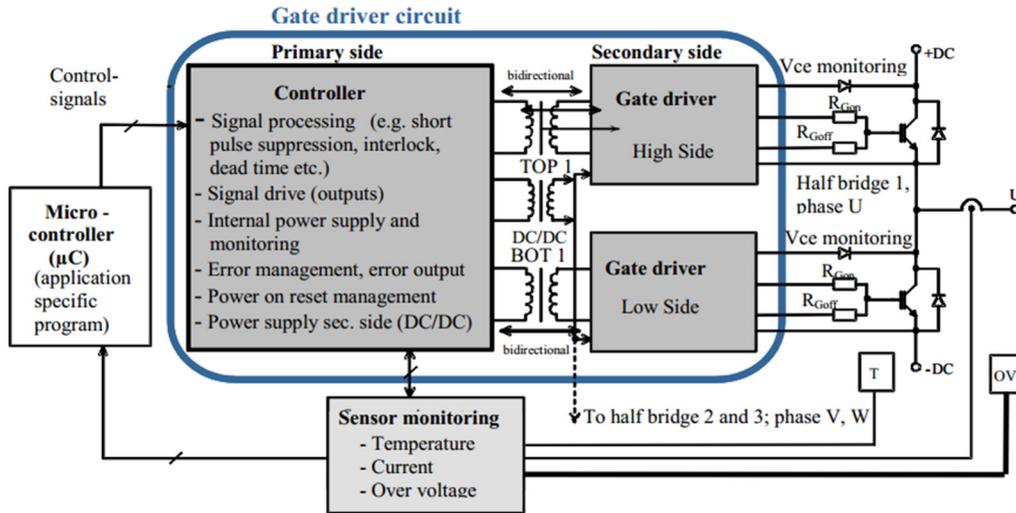


Fig.I.18 Principle driver circuit in power electronics system, adapted in a half-bridge [36]

The driver circuit is simplified into a block schema Fig.I.19. In this schema, the primary-secondary capacitances and the pathway of the noisy current are depicted. Since the switching cells commutates periodically,  $dv/dt$  appears at the middle point of the switching cell.

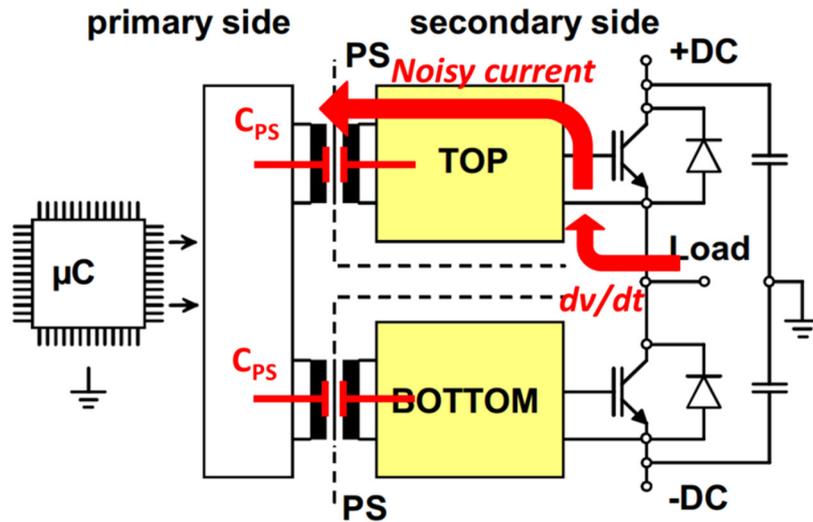


Fig.I.19 Conventional architecture of a gate driver circuit for a high side – low side devices [37]

This  $dv/dt$  generates a noisy current between the power part and the remote control part that can be estimated by Equation I.1.

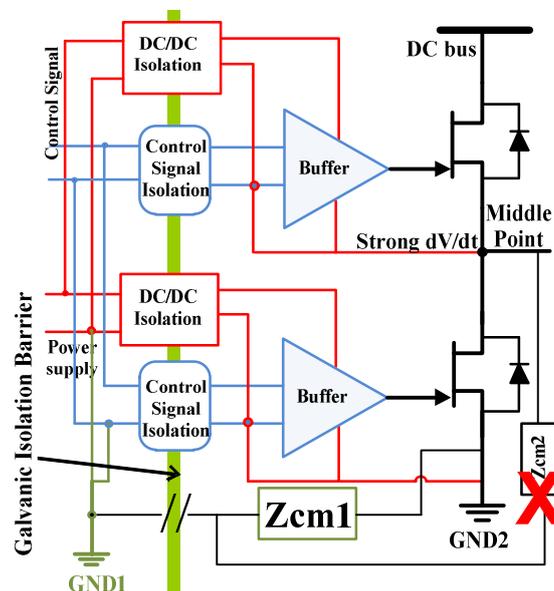
$$I_{NOISE}(t) = C_{PARASITIC} \times \frac{dv(t)}{dt} \tag{I.1}$$

The current flows through the parasitics capacitors and come back through the ground(s) of the system. The remote control part becomes the victim of the conducted EMI current in common-mode where the conducted EMI perturbations pass finally through the ground of the remote control part.

***I.2.a-iii Conducted EMI problems with high speed power devices***

A typical low side/high side gate driver circuit architecture with essential blocks, including isolation stages for power supplies and control units, is shown in Fig.I.20. In this conventional architecture [36] [37] [38] there are two “grounds”, one for the remote control circuit GND1 and one for the power circuit GND2. These grounds are insulated from each other by the isolated converters which are implemented in order to enable the isolation dedicated to the power supply parts, and the control signal isolators are used to isolate the control signals.

In Fig.I.20, two important impedances are presented. The common mode impedance  $Z_{cm1}$  represents the isolation between the grounds and shows the sum of the parasitic impedances between them.  $Z_{cm2}$  show the parasitic impedance between the middle point of the inverter leg and the ground of the remote control system. Several researches have been done on the effect of  $Z_{cm2}$  in the power electronics system [39] [40] [41]. The conducted EMI perturbations are investigated in this research as the perturbations on the driver circuitry through impedance  $Z_{cm1}$ .



*Fig. I. 20. Gate driver circuit with power devices and common mode impedances*

The power converters may operate by driving the low side and the high side power transistors with complementary signals.

In the conventional architectures, the gate driver and the associated supplies increase the conducted EMI pathways and the coupling capacitances across the insulation barrier. In a driver circuit, the parasitic capacitors and the parasitic inductors determine the EMI perturbation propagation paths from the power parts to the signal parts. To ease the explanation of the noisy current, the isolated power supplies and the control signal isolators are considered as a parasitic capacitor across the primary-secondary  $C_{PS}$  of each blocks into Fig.I.21. The interconnections of the low side and the high side power supplies represent as  $L_{WIRING\_LS}$  and  $L_{WIRING\_HS}$ . And the connection from GND1 to the input of the low side power supply is  $L_{WIRING}$ .

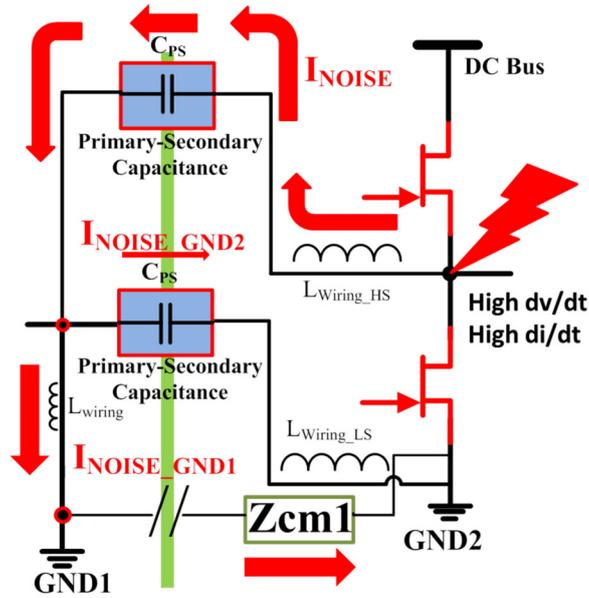


Fig.I.21. Simplified gate driver circuit with the primary-secondary capacitance of the conventional architecture

The detailed high frequency equivalent circuit of the architecture will be detailed in Chapter II. GND1 and GND2 are the electric reference potentials of the remote control circuit and the power part, respectively.

Since  $dv/dt$  are generated at the floating-middle point of the half-bridge (see Fig.I.21), the noisy current appears through  $C_{PS}$  as expressed in Equation I.1. Then this current is divided by two paths:

$$I_{NOISE} = I_{NOISE\_GND1} + I_{NOISE\_GND2} \quad I.2$$

A part circulates to GND1 on the impedance of the interconnection  $L_{WIRING}$  ( $I_{NOISE\_GND1}$ ); the second part goes to GND2 through the impedance of the low side power supply to the power part and the low side interconnection  $L_{WIRING\_LS}$  ( $I_{NOISE\_GND2}$ ).

The impedance in common mode between GND1 and GND2 ( $Z_{CM1}$ ) can be represented by a large capacitance  $C_{GND1-GND2}$  (from hundreds of pF to several nF) by two isolated power supplies which means a small impedance in the upper frequency range. For example, the power supply of the control circuit grounds to the earth by connecting directly to the grid, meanwhile the high voltage power supply of the power part connects to the grid by a 50 Hz transformer, the capacitance of this transformer is in the range of 10 nF – 100 nF [42]. In this context and in the upper frequency range, compared to the voltage appearing on the parasitic elements of the driver circuit at each switching transition, the potential difference between GND1 and GND2 can be neglected.

As a function of the impedance ratio, without the added measured impedance  $Z_M$  and considering a First Harmonic Approximation, the relation of the current can be written as:

$$\frac{I_{NOISE\_GND2}}{I_{NOISE\_GND1}} = \frac{2\pi f_{transient} L_{wiring}}{\frac{1}{2\pi f_{transient} C_{PS}} + 2\pi f_{transient} L_{LS1} + 2\pi f_{transient} L_{LS2} + 2\pi f_{transient} L_{wiring\_LS}} \quad I.3$$

## I.2 The need of EMI management on the driver circuitry with the evolution of high speed power components

Where,

- $f_{\text{transient}}$ : the transient frequency, is approximately equal to  $0.35/T_{\text{RISE-TIME}}$  where the rising time  $T_{\text{rise-time}}$  is about 20ns. So, the estimated transient frequency is equal to 17.5 MHz [43], [44].
- $L_{\text{WIRING}}$ : the parasitic inductance of the wiring connection from the ground of the remote control circuit to the input of the low-side power supply, is equal to several 10nH, see section Chapter II for the parasitic characterizations
- $L_{\text{WIRING\_LS}}$ : the parasitic inductance of the wiring connection from the output of the low-side power supply to the ground of the power parts, is equal to several 10nH, see section Chapter II for the parasitic characterizations
- $L_{\text{LS1}}$  and  $L_{\text{LS2}}$  primary and secondary parasitic inductor of low side power supply are estimated to 50nH in total, see Chapter II for the parasitic characterizations
- $C_{\text{PS}}$ : the parasitic capacitance of the power supply of the gate driver circuit, varies between 10pF to 100pF, see section Chapter II for the parasitic characterizations

The impedance between the low side power supply and the connection  $L_{\text{WIRING\_LS}}$  can be expressed as:

$$Z_{\text{PS}} = \frac{1}{2\pi f_{\text{TRANSIENT}} C_{\text{PS}}} + 2\pi f_{\text{transient}} L_{\text{LS1}} + 2\pi f_{\text{transient}} L_{\text{LS2}} + 2\pi f_{\text{TRANSIENT}} L_{\text{wiring\_LS}} \quad \text{I.4}$$

And the impedance of the connection is given by:

$$Z_{\text{Connection}} = 2\pi f_{\text{TRANSIENT}} L_{\text{wiring}} \quad \text{I.5}$$

The impedance plots in Fig.I.22 show the ratio between the  $Z_{\text{PS}}$  and  $Z_{\text{CONNECTION}}$ . As we can see, in the low frequency range of the plot which is around the transient frequency 17.5 MHz,  $Z_{\text{PS}}$  is much larger than  $Z_{\text{CONNECTION}}$ . This ratio is smallest at 190 MHz frequency which is far above the transient equivalent frequency considered of this research. Above that frequency, the capacitive impedance becomes small and the current ratio represents by the parasitic inductance ratio.

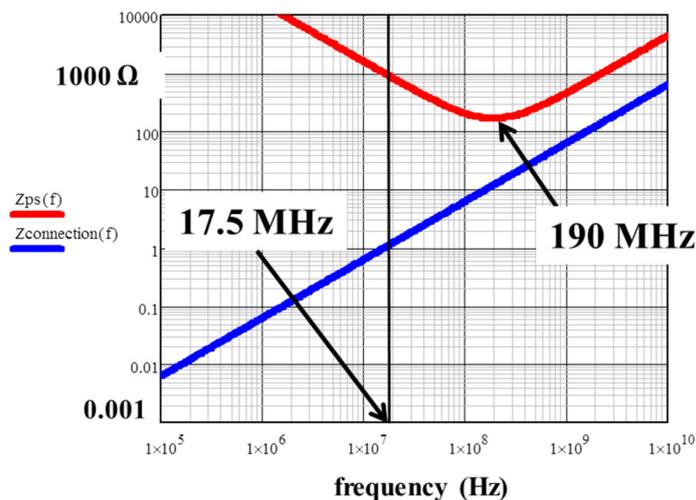


Fig.I.22. Impedances  $Z_{\text{PS}}$  and  $Z_{\text{CONNECTION}}$  versus transient frequency

According to the rise time of the power device, we can estimate the impedance contribution at the transient frequency of the primary-secondary path for parasitics for the low side power supply:

$$\frac{1}{2\pi f_{\text{transient}} C_{\text{PS}}} \approx \frac{20 \times 10^{-9}}{2\pi \times 0.35 \times 10 \times 10^{-12}} \approx 900 \Omega \quad \text{I.6}$$

And

$$2\pi f_{\text{transient}} L_{\text{wiring}} \approx 2\pi \times \frac{0.35}{20 \times 10^{-9}} \times 10 \times 10^{-9} \approx 1 \Omega \quad \text{I.7}$$

Now, the estimation of the current ratio becomes:

$$\frac{I_{\text{NOISE}_{\text{GND2}}}}{I_{\text{NOISE}_{\text{GND1}}}} = \frac{2\pi f_{\text{transient}} L_{\text{wiring}}}{\frac{1}{2\pi f_{\text{transient}} C_{\text{PS}}} + 2\pi f_{\text{transient}} L_{\text{LS1}} + 2\pi f_{\text{transient}} L_{\text{LS2}} + 2\pi f_{\text{transient}} L_{\text{wiring}_{\text{LS}}}} \quad \text{I.8}$$

$$\approx 10^{-3} \ll 1$$

As the estimated result of Equation I.8,  $I_{\text{NOISE}_{\text{GND2}}}$  is much smaller than  $I_{\text{NOISE}_{\text{GND1}}}$ , almost all the noisy current  $I_{\text{NOISE}}$  in Fig.I.21 goes through the ground of the primary side of the remote control part GND1.

The high speed power devices generate  $dv/dt$  from 10V/ns to 100V/ns. Then this perturbation generates, through the parasitic capacitors of the power supply of the gate driver circuit, a noisy current that can be in the range of several Amps.

An estimation of the noisy current magnitude is based on the average value of the generated  $dv/dt$ ; then we can estimate the noisy current as the conducted EMI perturbation in the equation I.9.

$$I_{\text{NOISE}} = 50 \text{ pF} \times \frac{50 \text{ V}}{\text{nsec}} = 2.5 \text{ A} \quad \text{I.9}$$

This estimated noisy current circulates to the ground of the micro-controller of the remote control circuit, and passes through the high side power supply of the gate driver where its nominal current is less than 100mA. This noisy current will be the disaster for the control circuit if the extreme  $dv/dt$  as in Fig.I.8 and Fig.I.9 occur in this situation: hereby the conducted EMI becomes a major problem in a real system.

These EMI disturbances, combined with non-adapted design of the gate driver and the supplies, limit designers in gaining a maximal benefit from the outstanding characteristics of the new generation of the high speed power devices.

### **I.2.b Solutions for the conducted EMI problems on the gate driver circuit**

There are no doubts that we have to overcome the conducted EMI problem for the proper performance of the system. The parasitic capacitances need to be reduced in order to minimize the value of the noisy current; or the propagation pathways need to be re-routed in a way that the high noisy currents do not pass through the ground of the remote driver circuit: Fig.I.23.

I.2 The need of EMI management on the driver circuitry with the evolution of high speed power components

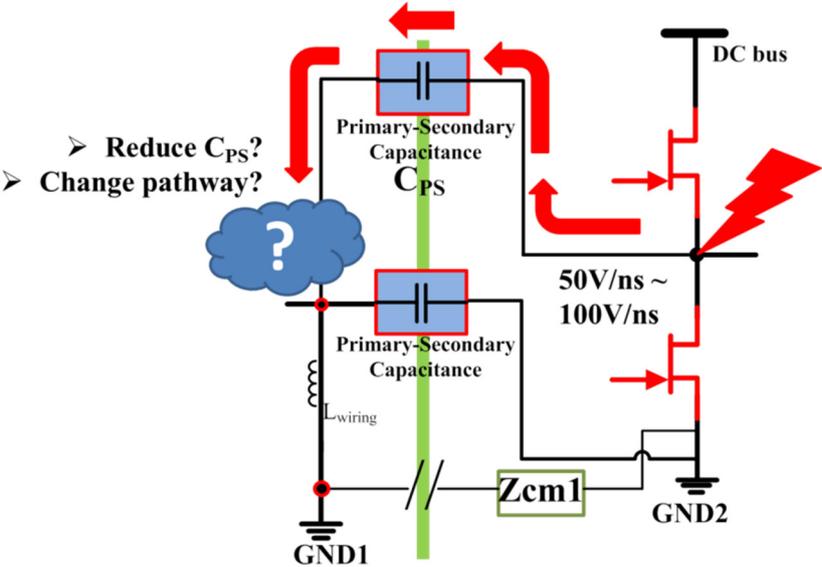


Fig.I.23. Which ways to reduce the conducted EMI perturbation?!

In this research, firstly, we work on the architecture of the driver circuit at the system level to find out the best way to minimize the impact of the conducted EMI current. Then, in the next step, the elements of the driver circuit are studied in order to reduce the parasitic capacitance; hereby the noisy current could be minimized even with an extreme value of  $dv/dt$ .

**I.2.b-i At system level for a low side – high side configuration**

At the system level point of view, this work proposes a novel architecture in order to modify the noisy current propagation pathways: Fig.I.24.

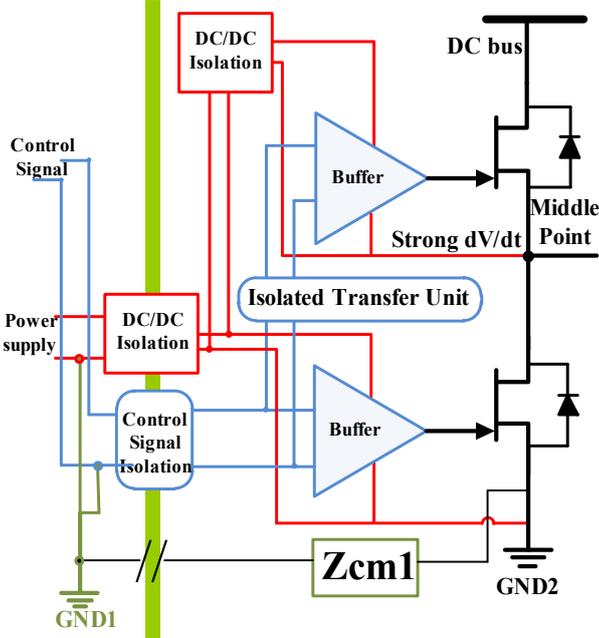


Fig.I.24. Proposed gate driver architecture solution at the system level

## I.2 The need of EMI management on the driver circuitry with the evolution of high speed power components

As we have seen in a power electronics system, the source of perturbations due to high switching speed always exists, and there are not interests to get it slower. The main idea of this architecture is to modify the pathway of the noisy current (as close as possible to the switches) and also to reduce it.

To explain qualitatively the amount of noisy current on the remote control circuit in the proposed architecture, as well as in the conventional architecture, the gate driver circuit is modeled with a parasitic capacitor for the isolators and parasitic inductors for the wiring connections as described in Fig.I.25.

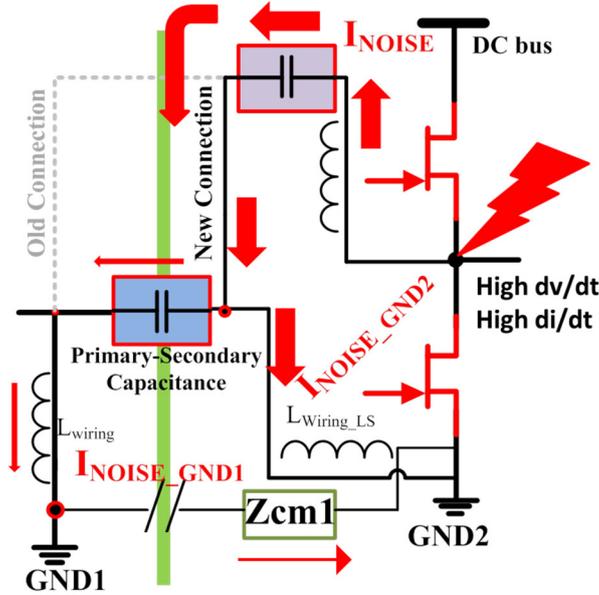


Fig.I.25. Simplified gate driver circuit with the primary-secondary capacitance of the proposed architecture

In this simplified circuit, the first part of perturbation goes to GND1 through the parasitic capacitor (primary/secondary capacitor of the insulated DC/DC converter) of the low side power supply to the power part as  $I_{NOISE\_GND1}$ . The second part turns back to the power part to GND2 through the impedance of the low side interconnection  $L_{WIRING\_LS}$ . Due to the large capacitance between GND1 and GND2, in the upper frequency range, the corresponding impedance can be neglected compared to the other parasitics:

$$I_{NOISE\_GND1} \times \left( \frac{1}{2\pi f_{transient} C_{PS}} + 2\pi f_{transient} L_{LS1} + 2\pi f_{transient} L_{LS2} + 2\pi f_{transient} L_{wiring} \right) = I_{NOISE\_GND2} \times 2\pi f_{TRANSIENT} L_{wiring\_LS} \quad I.10$$

According to the derivations of the equations I.4 – I.7, we can estimate the ratio of the currents in the proposed architecture as:

$$\frac{I_{NOISE\_GND1}}{I_{NOISE\_GND2}} = \frac{2\pi f_{transient} L_{wiring\_LS}}{\frac{1}{2\pi f_{transient} C_{PS}} + 2\pi f_{transient} L_{LS1} + 2\pi f_{transient} L_{LS2} + 2\pi f_{transient} L_{wiring}} \quad I.11$$

$$\approx 10^{-3} \ll 1$$

The result of Equation I.11 is opposite to Equation I.8 which means that the noisy current circulates mainly directly back to power part into GND2.

Nevertheless, due to the parasitic inductance of the wiring interconnections, there is a small amount of the noisy current that goes through the ground of the remote control circuit. In this proposed architecture, even an extreme  $dv/dt$  (see Fig.I.9) occurs, the remote control circuit is always safe. The optimized routing and the circuit improvement are critical points: the detailed validations are provided in Chapter II to prove the advantages of the proposed architecture on the conducted EMI.

However, the noisy current should be originally reduced by decreasing the parasitic capacitance of the elements in the circuit.

### ***I.2.b-ii At component level***

The value of the noisy current depends on the value of  $dv/dt$  and the parasitic capacitor value of the driver circuit's elements as shown in Equation I.12.

$$I_{NOISE} = \sum C_{PARASITIC\_DRIVER} \times \frac{dv}{dt} = (C_{POWER\_SUPPLY} + C_{CONTROL\_ISOLATOR}) \times \frac{dv}{dt} \quad I.12$$

Where,

- $C_{POWER\_SUPPLY}$ : the primary-secondary parasitic capacitance of the gate driver power supply
- $C_{CONTROL\_SIGNAL}$ : the primary-secondary parasitic capacitance of the signal control isolator such as the opto-coupler, the coreless transformer...

To minimize the noisy current, a special work must be engaged to minimize the parasitic capacitor value; decreasing the switching frequency or optimizing the circuit architecture and the IC (Integrated Circuit) designed by acting on the propagation pathways and IC susceptibility. The objective is to decrease the parasitic influences on the proper operation of the power converter, especially between the high side and the low side control modules of the gate driver.

On the other side, the parasitic inductances that cause propagation delays and magnetic couplings between the power devices and the gate drivers need to be reduced. This can be obtained by working at packaging level and designing a specific gate driver which can be placed very close to the power transistors.

In this work, Chapter III intends to deal with the conducted EMI problems at the component level for a high side – low side implementation.

### ***I.2.b-iii Perspective for the complex configurations***

The effects of this work at system level will be investigated for the gate driver circuitry for different configurations. As we have seen,  $dv/dt$  and the primary-secondary parasitic capacitance are the reason of the conducted EMI perturbation. The whole approach can be transposed to complex power converters, multi-cell, multi-level or even series connection of power devices. In these converters, many driver circuits are required and implemented and the proposed architecture can be derived to serve at best these complex driving configurations. In such converters, there are several  $dv/dt$  sources of the floating points and several parasitic capacitances of the gate driver isolated power supplies, the conducted EMI perturbation from the power part to the control part could be worse. The detail problems and solutions for the power devices in series connection configuration will be briefly discussed in Chapter II.

From this point-of-view, many challenges appear to the researchers. These issues must be taken into account and overcome for making an improved EMI management for gate drivers.

### I.2.c Side issues

#### I.2.c-i Thermal considerations of the proposed architecture

Fig.I.26 presents the parasitic elements of the gate driver circuit and the power part for a high side – low side configuration. Across the galvanic isolation barrier (green color) there are the primary-secondary parasitic capacitance of the high side and low side isolations (power supplies and the signal isolators), these parasitic values are critical for the noisy current. Then around the power devices which is considered as a hot device, there are the parasitic capacitances of the power devices and the element of the gate driver circuit, the parasitic inductances of the interconnections around the power devices and around the elements of the gate driver circuit.

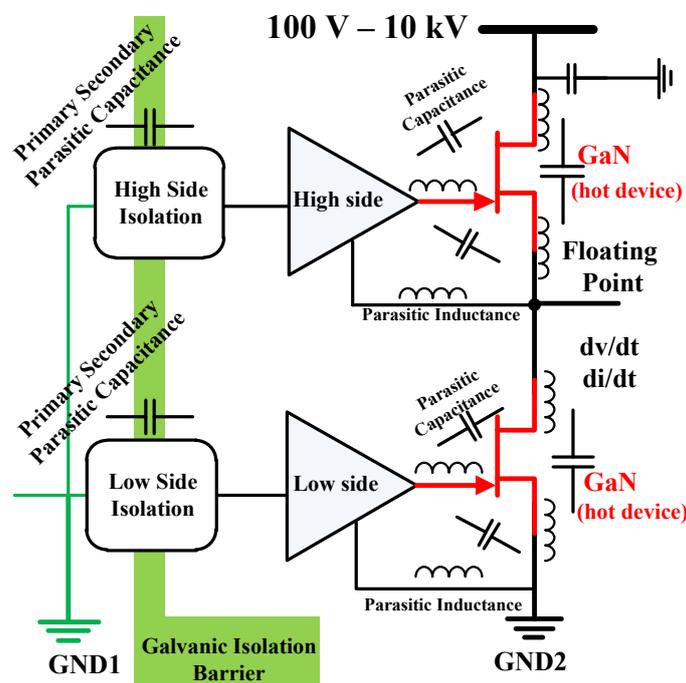


Fig.I.26 Parasitic elements of the conventional gate driver circuit and power devices

The reduction of these parasitic elements is necessary for  $dv/dt$  and  $di/dt$  immunity from the floating point. In the power part, the parasitic impedance should be minimized by using the advanced packaging technology flip-chip, 3D packaging or other solutions. In the closed control part of gate driver, the primary-secondary parasitic capacitance and the gate driver loop should be also reduced.

The aim of this work is to bring the driver circuit closer or as close as possible to the power component, even inside the WBG power module in order to minimize all the parasitic inductances as depicted in Fig.I.27 [45]; however, in this extreme case, the driver circuit must share the same thermal environment as the power devices. In a near future, the case temperature of WBG power module is expected to reach  $200^{\circ}\text{C}$  for high speed power devices. The driver circuit temperature operation and heat removal become a key challenge for the new generation of gate driver circuit for high speed power devices.



Fig.I.27 “Hot box” with the power devices and the driver circuit, all-in-one [45]

Therefore, another challenge to redesign the gate driver’s element at the component level in order to minimize the parasitic capacitances and resist in high temperature is necessary more than ever.

### ***1.2.c-ii The need of redesign the elements of the new architecture gate driver for high speed power devices***

Very high speed power devices and especially WBG devices are very constraining components. To maximize WBG devices operations, several researches [46], [47], [48], [49] show that advanced dedicated gate drivers circuitry must be designed.

The innovative solutions for low side - high side control signal transfer and the high side power supply of the gate driver under harsh operating conditions, especially at high temperature need to be investigated and finally implemented in the new gate driver.

### **APPROACH OF INTEGRATED CIRCUITS TOWARDS MONOLITHIC INTEGRATION**

Bring the gate driver as close as possible to the power device make the classical gate driver elements unsuitable according to the temperature and the electrical harsh environment issues: power supplies, signal transfer units and buffers.

The power supply and the buffers of the gate driver are brought close to the power part, and then a classical components are no more suitable, a high temperature technology must be considered for these parts.

There are the techniques of the signal transfer unit of the gate driver such as the well-known and classical current source level shifter, the high frequency magnetic coupler and the opto-coupler derived technique. For each technic of the level shifter, there are always the positive and drawback attributes for a specific application. Depending on the requirements of the system; the most suitable gate driver technique with its level shifter can be selected.

In Chapter III, solutions are studied and prototyped for the power supply and the signal transfer units using high temperature qualified technology SOI-CMOS from an industrial foundry. Eventually, an approach of a monolithic integrated gate driver would be the solution.

### I.3 Gate driver for high speed power devices with improved EMI management in harsh environments

Today, several commercial gate drivers are available for WBG devices as GaN and SiC. For a specific high side – low side driver, the gate driver system has usually two pathways for the power supplies as well as the control signal as depicted in Fig.I.28.

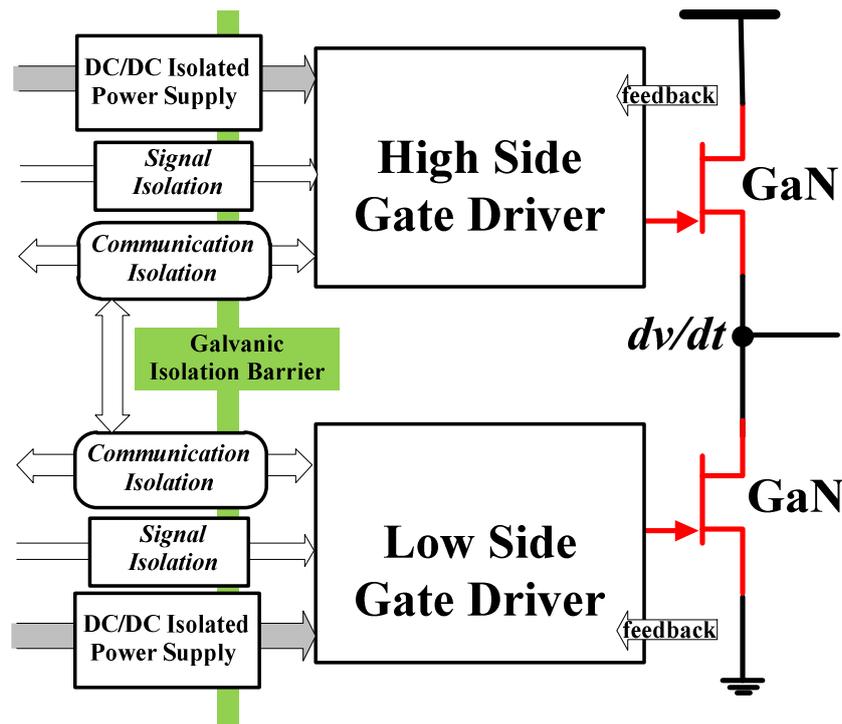


Fig.I.28 Conventional gate driver circuitry of the half-bridge system overview

As we mentioned before, high speed WBG devices generate strong  $dv/dt$  when they switch. In one hand, strong  $dv/dt$  could perturb gravely or even ruin out the remote control parts. On another hand, strong  $dv/dt$  effect distorts the control signals of the power devices then the behavior of the power devices may change negatively, even the noisy control signals could be induced to generate a short-circuit in an inverter leg.

#### I.3.a Today solutions of the gate driver for WBG devices

Commercial gate driver deals with CMTI (common-mode transient immunity), the propagation delay as well as the high temperature issue.

In the commercial solutions, the conventional gate driver architecture is used widely. There are two pathways for the control signal and the power supply independently. In the following part, low temperature and high temperature gate driver circuitries are shown.

#### Low temperature gate driver circuit

Fig.I.29 shows a gate driver circuit schematic which drives GaN devices from GaN Systems. In this schematic, there are two independent pathways for both the signal control and the power supply.

Fig.I.30 shows the evaluation board in the low temperature. The CMTI is 50V/ns in this gate driver circuit [21].

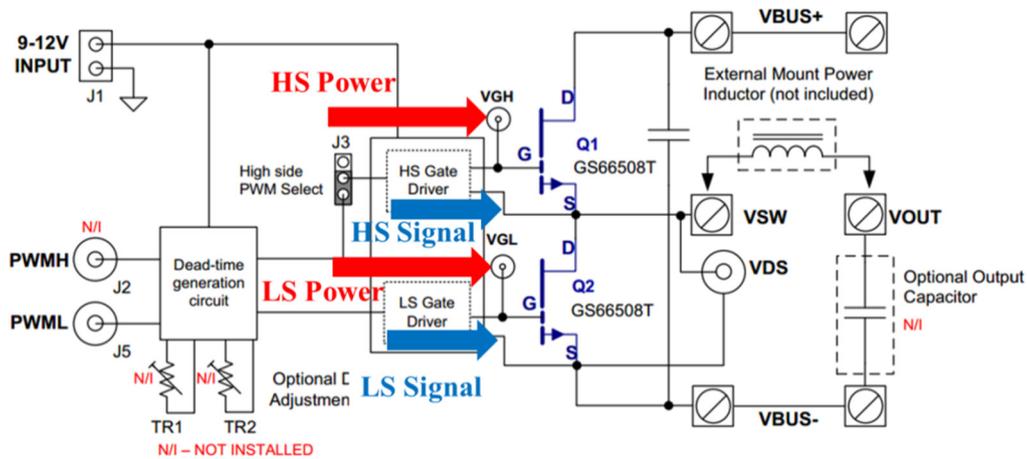


Fig.I.29 GS66508T-EVBHB Evaluation Board Block Diagram from GaN-System with the conventional gate driver architecture

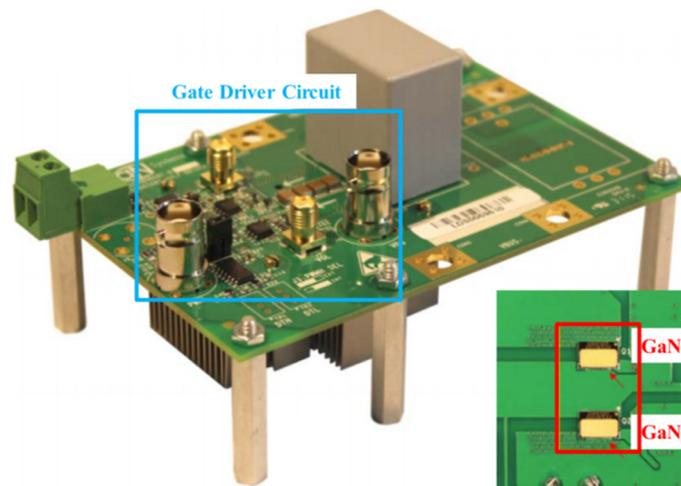


Fig.I.30 GaN E-HEMT Half Bridge Evaluation Board using SI8261BAC-C-IS driver

For 1200V SiC power devices, Fig.I.31 shows a gate driver schematic with the conventional architecture. The driver circuit is shown in Fig.I.32 for a low temperature application. The CMTI is up to 100V/ns in this gate driver circuit [50].

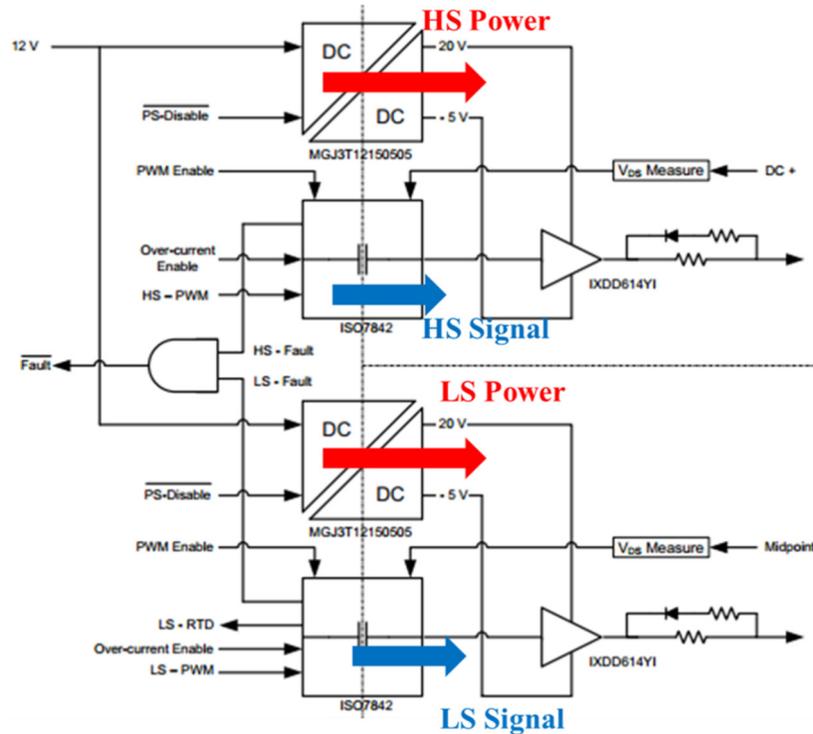


Fig.I.31 CREE CGD15HB62LP schematic circuit with the conventional gate driver architecture

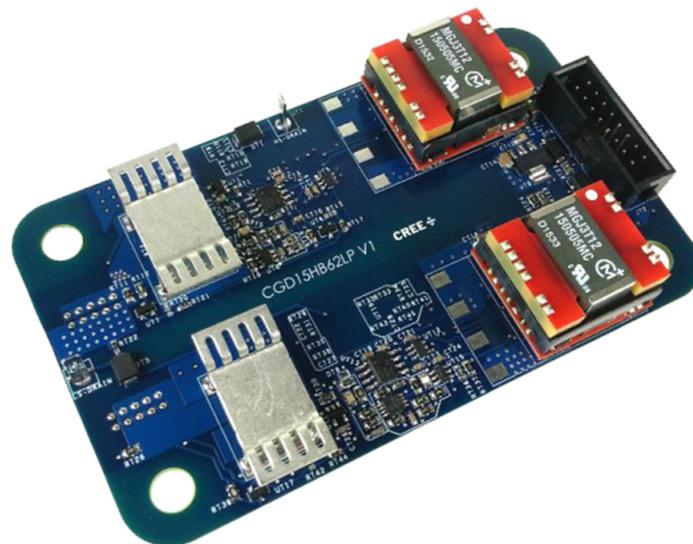


Fig.I.32 CREE CGD15HB62LP circuit with IXD614 gate driver

**High temperature gate driver circuit**

Fig.I.33 shows a complete gate driver circuit for high temperature applications. In this schematic, the conventional gate driver architecture is used to implement the power supplies and the signal isolators for a high side – low side configuration. Fig.I.34 shows a gate driver circuit on a 200°C polyimide PCB. However the maximum temperature of the active component is up to 225°C. The CMTI is about 50V/ns [51].

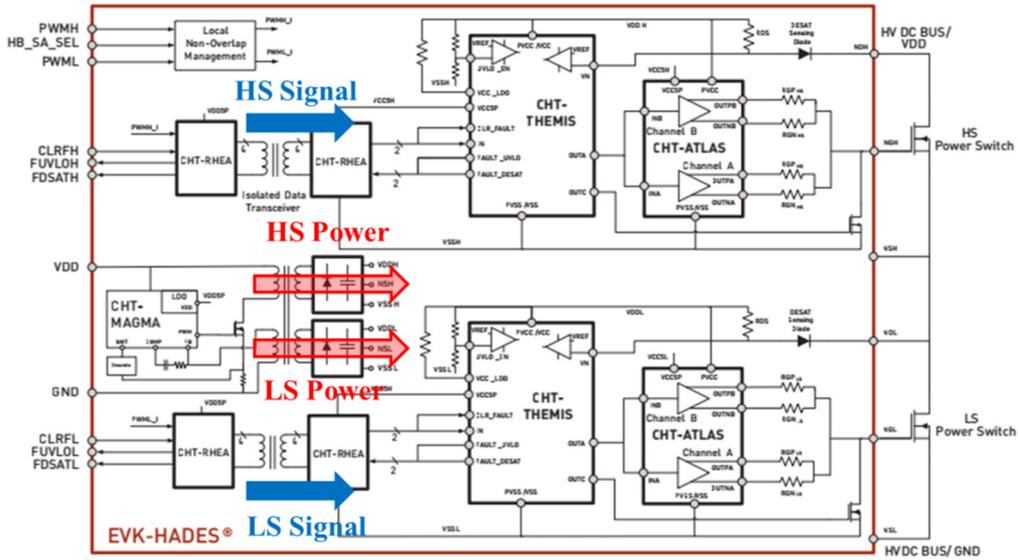


Fig.I.33 High temperature gate driver RHEA of CISSOID Company schematic

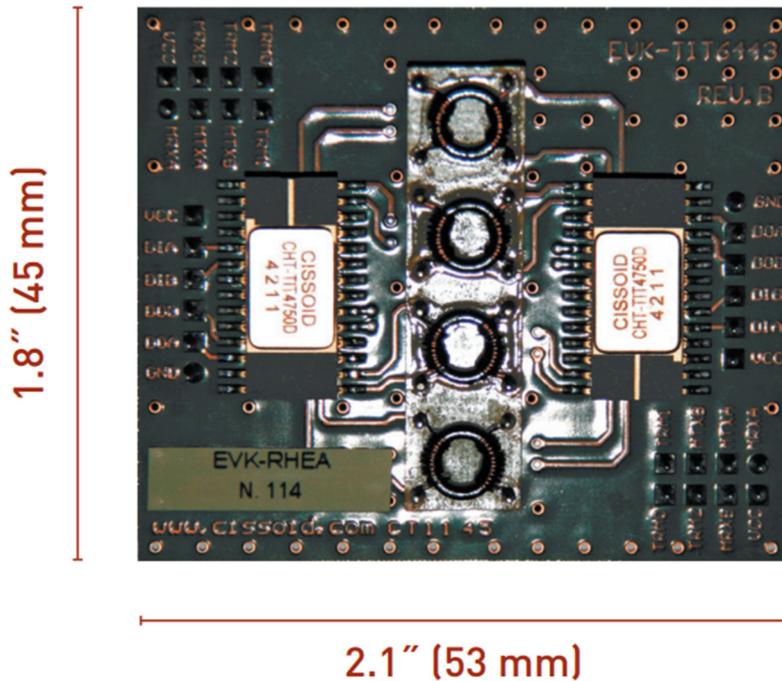


Fig.I.34 High temperature gate driver RHEA board overview

Table.I.2 shows the comparison of three commercial gate driver circuits. The propagation delay is considered as the delay of the whole system, including the delay on the primary gate driver circuit and the isolation barrier. The maximum temperature is the qualified junction temperature of the active component nearby the power devices.

Table.I.2 Comparison of the commercial gate drivers

Gate Driver Component	Company	Propagation delay of gate driver	CMTI	Max Temperature of active component
SI8261BAC-C-IS	 SILICON LABS	60ns	50V/ns	125 °C
IXD614	 IXYS INTEGRATED CIRCUITS DIVISION	75ns	100V/ns	125 °C
RHEA TIT4750D	 CISSOID	120ns	50V/ns	225 °C

The propagation delay of the gate driver is still high which causes difficulties in the precise dead-time management: Fig.I.6. For the temperature issue, the third solution is shown as the best; however, the propagation delay is the worst case. The CMTIs are quite impressive but all the gate drivers are using the conventional gate driver architecture, then, a large amount of the conducted EMI perturbation from strong  $dv/dt$  of the middle point of the half-bridge exists always on the primary side of the control circuit. This perturbation is able to disturb the remote control circuit including the micro-controller when the  $dv/dt$  is extremely high as we mentioned previously: Fig.I.8 and Fig.I.9.

For high speed power devices, there is no doubt that this perturbation must be redirected to another pathway, in the same time this perturbation needs to be reduced as small as possible. Reduce the delay propagation and improve simultaneously the temperature issue are also key issues.

**High temperature transformer for isolations**

In the high temperature gate driver circuit as we can see in Fig.I.34, there are the most challenge elements: the high temperature transformers for power and control signal.

Many researches have been engaged on this issue in order to increase the working temperature, decrease the primary-secondary parasitic capacitance meanwhile maintain the high galvanic isolation.

Fig.I.35 shows a coreless transformer by [52] for the power supply of the gate driver. The transformer can be used at the temperature high temperature; some specific materials has been mentioned in this work which can be used at temperature higher than 500 °C [53] [54]. This coreless transformer promises a low secondary-primary parasitic capacitance, this is crucial for minimizing the conducted EMI perturbation.

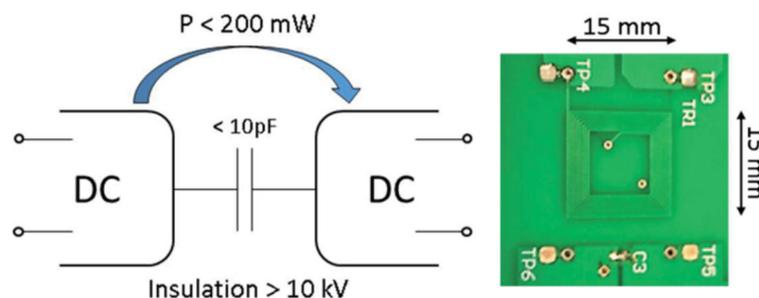


Fig.I.35 Left, gate driver power supply basic specification. Right, PCB coreless transformer of [52]

Another work [55] has been implemented for the control signal isolation based on an existing process, its capability at 200°C is tested. This design has a CMTI up to 75 V/ns.

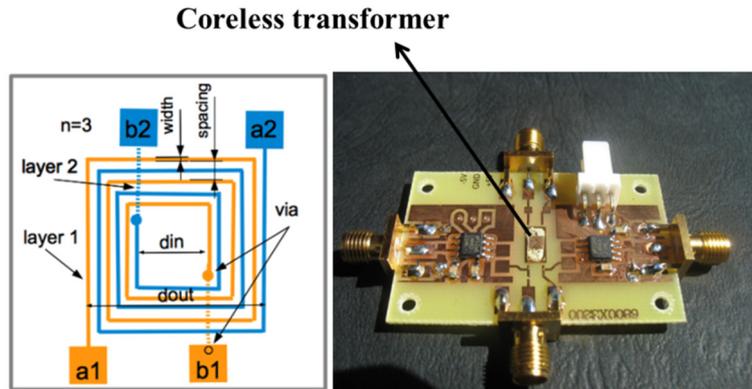


Fig.I.36 Left, Simplified top view of the coreless transformer for the control signal isolation. Right, the tests boards developed for the coreless transformers chips [55]

Within the gate driver’s task, the high temperature transformer is studied and developed by a partner of MEGaN project – Laboratory AMPERE.

In another hand, the control signal isolator is studied, developed and characterized by our integrated team in the power electronics group of G2ELab. The detailed works will be presented in Chapter III.

### I.3.b Driver circuit elements of a novel gate driver for high speed devices

Fig.I.37 illustrates the two regions of operational temperature and also the cascaded architecture to be implemented for proper EMI common mode path reduction: the low temperature zone under 100°C and the high temperature zone up to 200°C.

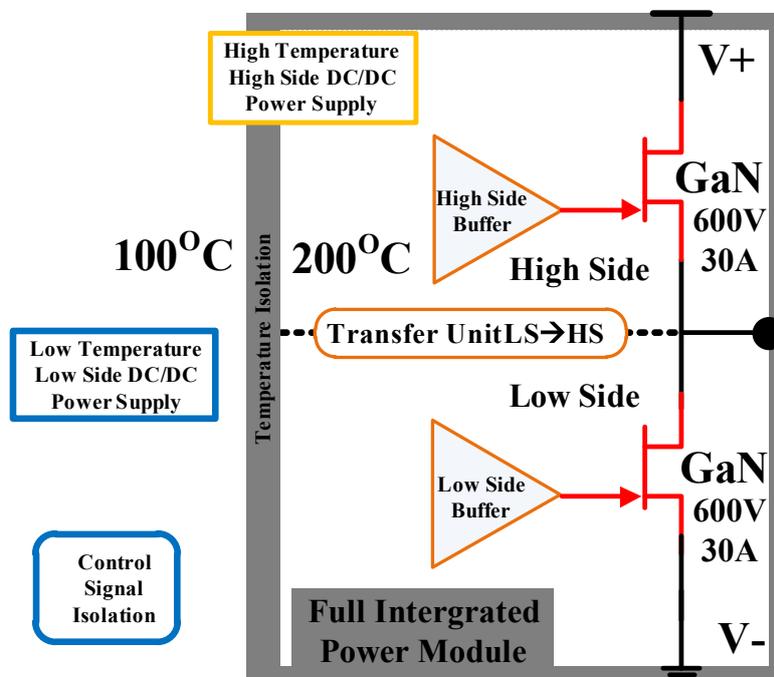


Fig.I.37 Gate driver with 2 temperature zones for thermal and EMI managements

According to several works [56], [57], [58] it is critical to care about how gate drivers are implemented close to the power devices in order to minimize parasitic inductances. The parasitic inductances in the gate driver circuit limit the speed of the gate charge and present an obstacle for  $dv/dt$  immunity purposes.

Conventional architectures of the power supplies with external gate driver circuits seem to be no more adapted to an effective implementation of very high speed power devices. The best solution would be to integrate the gate drivers within the power modules [59], [60].

In this work, the best positions of the essential elements are investigated: the low side - high side isolated control signal transfer unit, the low side - high side gate driver isolated power supplies. The answer is about which devices must be close to the power transistors. These locations are studied and justified in Chapter II.

The integration of CMOS IC of gate driver promises a short propagation delay, less than 20ns; and can be performed in the thermal environment of the thermal ratings of the WBG power devices up to 200°C. High temperature integrated technology is the solution for the elements in the high temperature zone.

Furthermore, the packaging technology of the integrated parts plays a very important role in order to minimize all the parasitic inductances of the interconnections. The classical wire-bonding imposes usually 1 nH/mm of the interconnection and it is limit at the working temperature [61] [62], [63] see Fig.I.38.

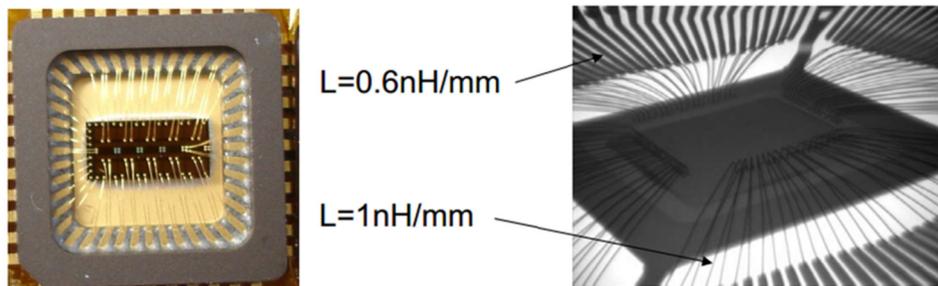
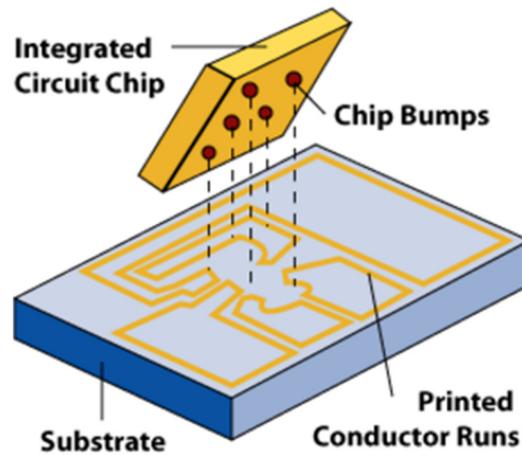


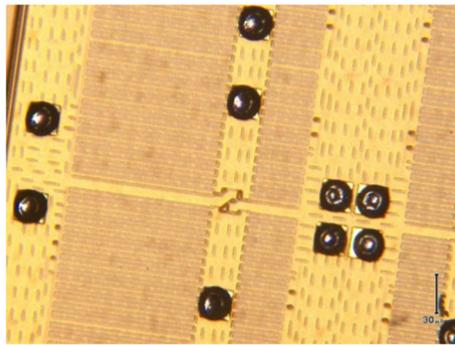
Fig.I.38 Left, photo of CQFP 44 packaging. Right, the estimation of the parasitic inductances [62], [63]

Meanwhile, the flip-chip technology [62] [64] brings several advantages for the packaging such as: reduce size, increase performance and working temperature of the circuit. In addition, it can nearly remove the packaging parasitic inductances between the devices and the carried circuit. The pictures in Fig.I.39, Fig.I.40 and Fig.I.41 present a brief introduction of the flip-chip process.

For optimizing the EMI perturbation, the flip-chip technology must be considered as an important factor.



*Fig.I.39 A flip chip and substrate, shown with the bumped active face of the die to be placed face down upon the matching substrate [64]*



*Fig.I.40 Solder bumps on the pads of the CMOS circuit [62]*

## **I.4 General research orientation – Thesis overview**

The conducted EMI problems related to driver circuit and architecture for high speed power devices as the WBG devices in high temperature and high CMTI have been presented.

Fig.I.42 shows the overview of this Ph.D work on the gate driver for WBG high speed devices, in this specification, the high side – low side power devices are GaN power devices (600V/30A). On this proposed orientation, we will overcome not only high CMTI but also reduce mostly the perturbation on the remote control, limit the propagation delay as well as the thermal problem.

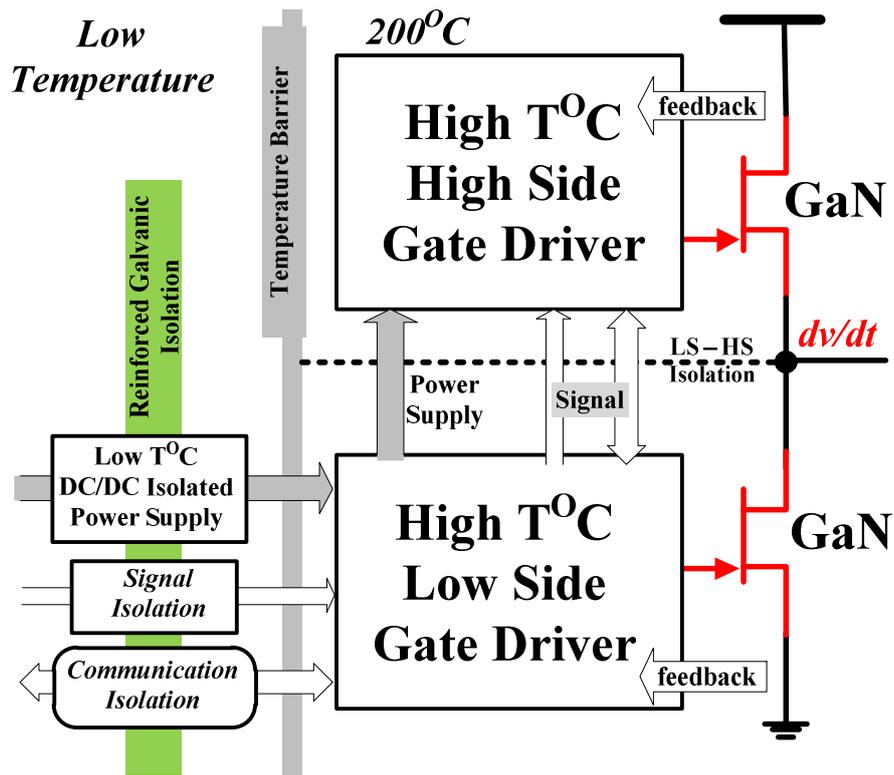


Fig.I.41 Proposed high temperature gate driver overview

In the next chapters, the proposed architecture is investigated in details with its advantages in Chapter II. Then, in Chapter III, the elements of the gate driver circuitry are redesigned, characterized and implemented in a high temperature qualified technology from a SOIC foundry, technology XFAB XT018.

Finally, a full integrated gate driver circuit in MEGaN project is depicted in Chapter IV.



# **Chapter II**

## **Gate Driver Architectures**

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## Abstract

*An innovative gate driver architecture for high speed power devices with high  $dv/dt$  in a low side – high side implementation is shown in this chapter. An EMI optimization is done by modifying the parasitic capacitance propagation paths between the power and the control sides thanks to a specific design of the circuit. Moreover, to reduce the impact of parasitic inductances, this chapter studies which elements of the drivers' circuitry must be brought as close as possible to the power parts and how/where they should be connected. This is an important issue for the gate driver's elements when the ambient temperature of the power devices becomes critical.*

*For a more complex configuration with multi floating points and several parasitic capacitances, the conducted EMI perturbations might become even more critical. We study and propose also in this chapter several gate driver architectures for the power devices in series connection. GaN devices in series connection configuration can benefit the high speed of GaN devices and at the same time, make a higher voltage ( $> 1kV$ ) system with EMI optimization.*

*Simulation and experimental results confirm the advantages of the innovative gate driver and the proposed power supplies architectures.*

## II.1 Introduction to gate driver architectures

### II.1.a Gate driver architecture for a high side – low side configuration: a reminder

The conventional gate driver architecture for a high side – low side specific configuration is depicted in Fig.II.1. As a reminder, Chapter I explained the perturbations of the power circuit on the control of the drivers flowing through the impedance of the gate driver circuit once the  $dv/dt$  occur. With the high speed advanced power devices, higher constraints are applied to the gate driver circuitry in order to minimize the negative impact of the conducted EMI.

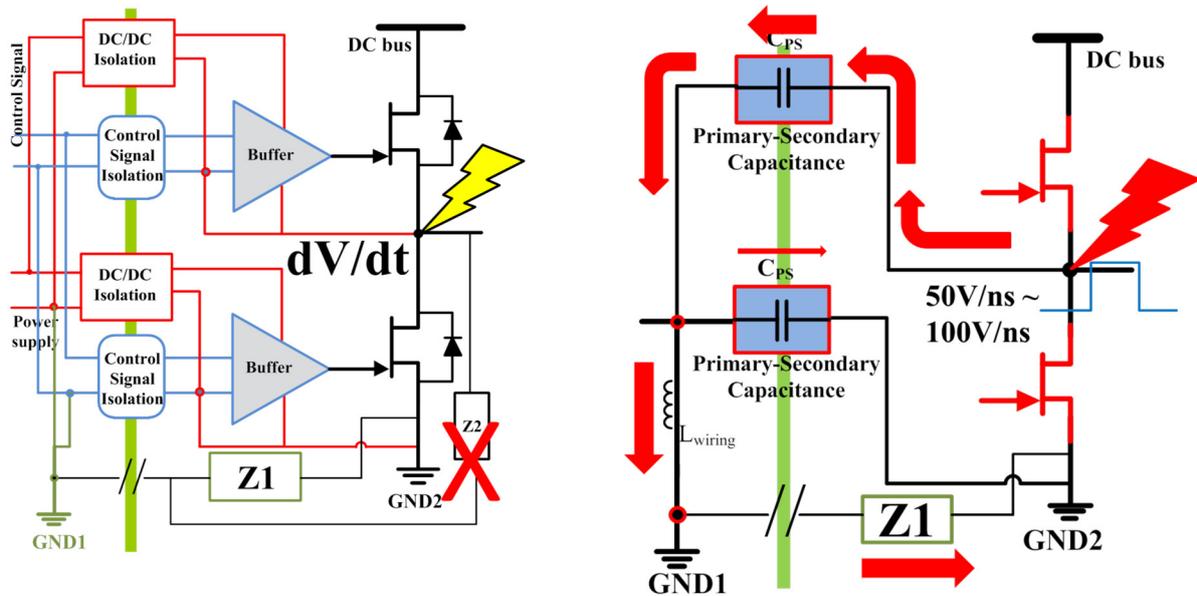


Fig.II.1. Gate driver circuit with conventional architecture. Left, schematic bloc diagram. Right, pathways for the conducted EMI perturbations

Until nowadays, this architecture has been used widely even for high speed power devices such as GaN and SiC power devices [36] [37] [38].

Within a gate driver circuit, the parasitic inductances that cause propagation delays and magnetic couplings between the power devices and the gate drivers need to be reduced. Nevertheless, parasitic propagation paths remain between the gate driver and the control parts through the gate driver supplies and gate signal isolators [21] [50] [51].

To overcome the conducted EMI problems on the gate driver circuit, as we mentioned in Chapter I, there are two solutions:

- Reduce the parasitic capacitances of the isolated stages of the gate driver
- Modify the propagation in a way that the high noisy currents do not flow in the common mode through the ground potentials when strong  $dv/dt$  occurs

In this chapter, the redirection of the propagation pathways by changing the gate driver architecture is studied. Then the analysis, the simulations and the experiments are detailed showing the advantages of the proposed gate driver architecture for a high side – low side configuration.

**II.1.b Power devices in series connection: expectation on the gate driver circuitry with EMI management**

The research for the gate driver of a low side – high side switching cells configuration leads to the investigation of the gate driver circuit of a complex configuration such as the power devices in series connection, multilevel converters such as flying capacitor architecture or modular multilevel converters [65] [66]:

- In chapter I, GaN power devices have been nominated as the power devices candidates for the new generation of the aeronautics, automotive and renewable energy management applications for instance. The specifications of the applications are in the range of several hundred volts and up to 100A (<1kV/<100A) [67], [68]. In order to make a higher voltage meanwhile keeping high the switching speed of the cells, the series connection is a solution for this specification. Therefore, works on the driver circuitry must be engaged.
- A complex configuration with power devices in series connection has multi floating points which mean multi  $dv/dt$  sources. Several isolated power supplies in the driver circuit means several parasitic capacitors. The conducted EMI perturbations might be much larger than a single high side – low side configuration. These perturbations must be investigated within the work on gate driver architecture.

As the same explanation for a high side – low side configuration, the noisy currents appear when high  $dv/dt$  sources are applied between the switching cells of the branch. In Fig.II.2, these noisy currents circulate at first in the driver(s) through the wired devices and the parasitic elements on the upper side devices. Then these currents go down to lower devices.

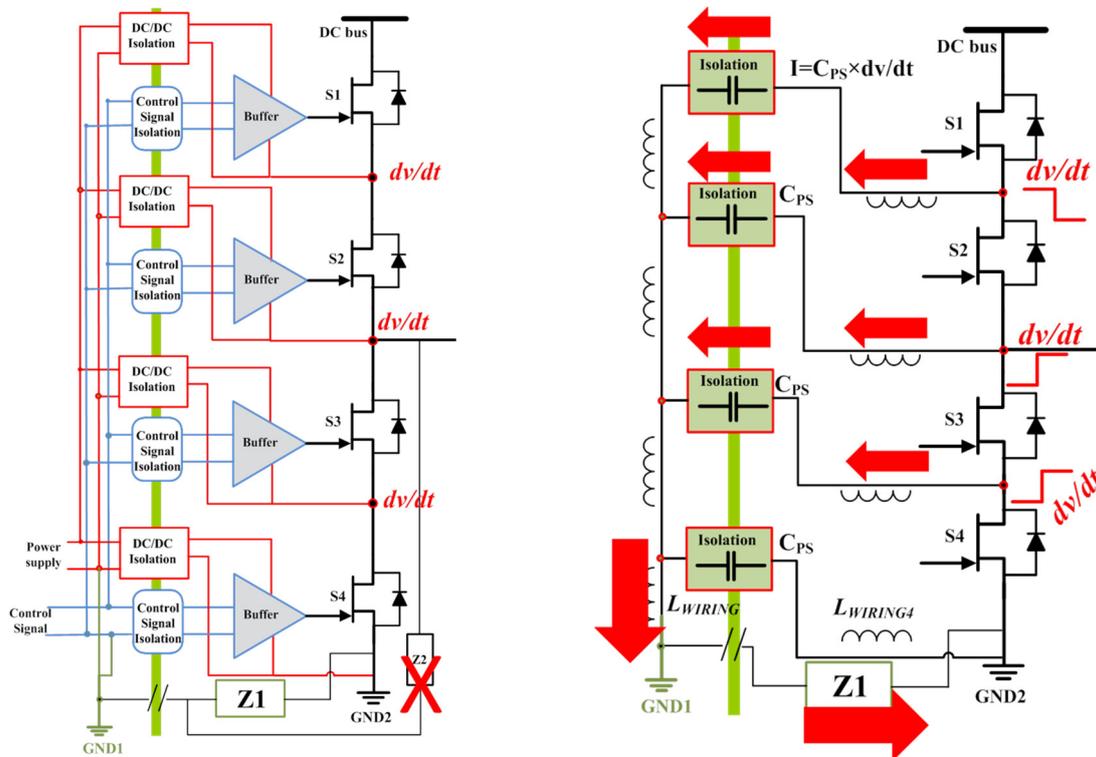


Fig.II.2. Left, conventional gate driver architecture of a series-connection of transistor. Right, the conducted EMI perturbations pathways in common mode

Each current is divided into two parts: the first component circulates back to the power part at the ground point through the lower parasitic element of “lower side” gate drivers and the second part circulates through the ground of the control circuit through the parasitic impedance of the interconnection. As a function of the impedance ratio, a large amount of noisy current goes through the ground of the control circuit.

In the simple case of two power devices in series connections as shown in Fig.II.2, there are already 3 sources of the perturbations with  $dv/dt$  as 3 floating points. Each  $dv/dt$  source will produce its own perturbations that may sum up and propagate to the control parts.

Three architectures are proposed and tested with experimental results in this chapter as one of the perspectives of the initial researches based on classical low-side / high-side architectures.

## II.2 Design and analysis of an innovative gate driver architecture

### II.2.a Proposed gate driver architecture from the conducted EMI point-of-view

As we mentioned in the first chapter, to overcome the EMI issue at high switching frequencies and especially under high  $dv/dt$ , this research proposes a new gate driver circuitry architecture for high switching speed components in Fig.II.3.

Changing the EMI current paths can limit the interactions between the converter modules. The proposed approach implements the high rating isolation stages only on the low side devices. In such a way, most disturbances circulate within the power side, especially if most of the driver elements can be integrated within the same package as the power devices. In this proposed architecture, the control signal is transferred to the high side through the low side gate driver components. In the same way, the input of the supply of the high side gate driver is directly connected to the output of the supply of the low side gate driver.

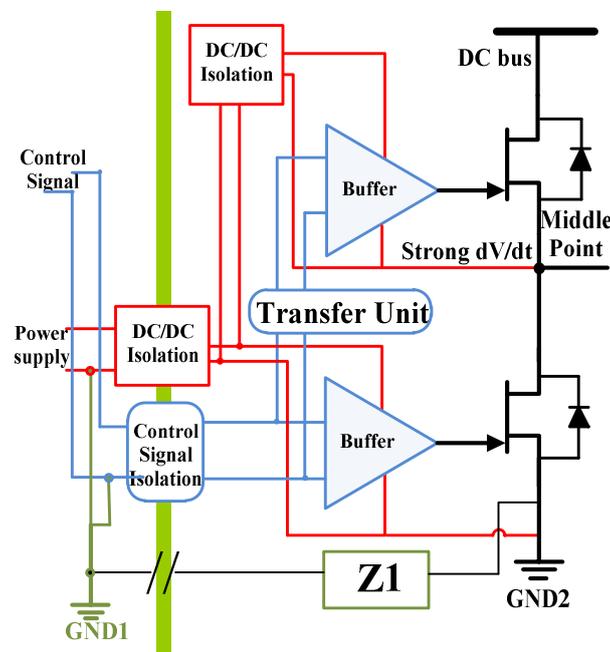


Fig.II.3. Proposed architecture of the gate driver circuitry

In Chapter I, the theoretical explanations are presented with the simplified circuits. In this chapter, the detailed validations with the simulations and the experiments are shown.

**II.2.b High frequency equivalent circuit of gate driver architectures**

High frequency equivalent circuit of the architectures are first analyzed and detailed in order to highlight the advantages of the proposed architecture and the effects of high  $dv/dt$  in the conventional architecture.

Fig.II.4 shows the parasitic elements of the power supplies (TRACO TMA1515S as the experiment's component) [69] and the isolations of the control signals (Optocoupler HPCL2211 as the experiment's component) [70] in a conventional gate driver architecture.

Each power supply has two parasitic inductances on the primary side and two parasitic inductances on the secondary side. There are also input and output decoupling capacitors, and two parasitic capacitors between the primary and the secondary sides.

The optocouplers have a similar set of parasitic inductances as the power supply. They have also parasitic capacitances between each primary side and secondary side.

In Fig.II.4, the parasitic inductances between the power supplies and the source terminals of the power transistors are also considered. Furthermore, parasitic inductances have been added between the power supplies, the optocouplers and the ground of the remote control circuitry.

Using the same way, the parasitic elements are added into the proposed gate driver architecture as depicted in Fig.II.5. In the experimental set-up, where the power supplies are identical but the signal transfer unit from the low side to the high side and the control signal isolator in Fig.II.5 is a level shifter which is different as an opto-coupler in the conventional architecture.

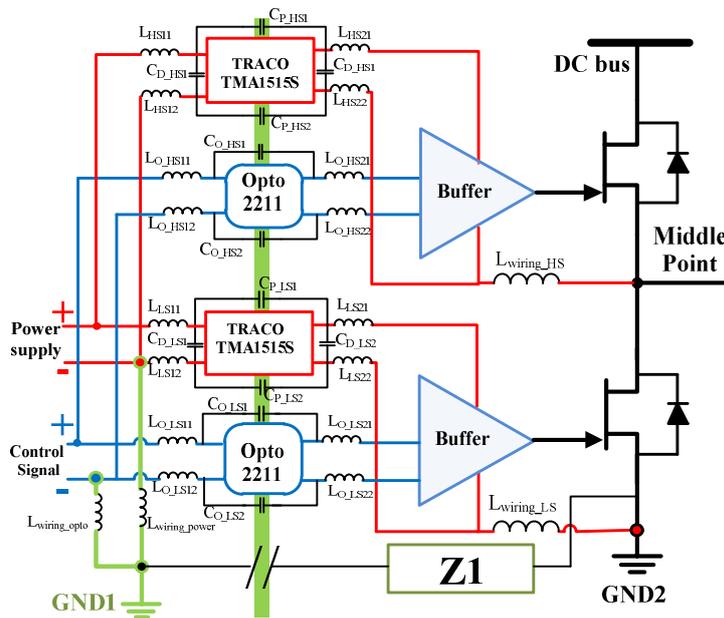


Fig.II.4. Parasitic elements around the power supplies and the control signal insulators in a conventional architecture

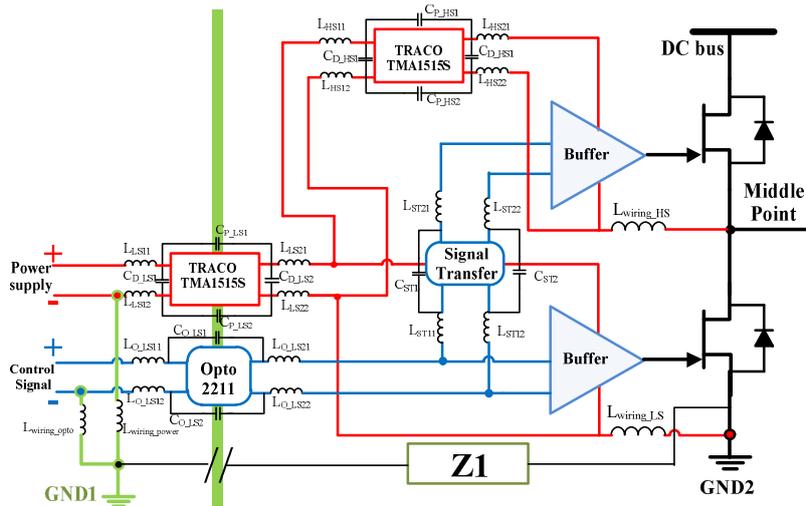


Fig.II.5. Parasitic elements around the power supplies and the control signal insulators in the proposed architecture

Table.II.1 shows all the elements of the equivalent circuits in Fig.II.4 and Fig.II.5

Table.II.1 The elements of the high frequency equivalent circuits in Fig.II.4 and Fig.II.5

$L_{HS11}, L_{HS12}, L_{HS21}, L_{HS22}$	Parasitic inductance on the primary and the secondary sides of high side power supply
$C_{D\_HS1}, C_{D\_HS2}, C_{D\_LS1}, C_{D\_LS2}$	Decoupling capacitor on the primary and the secondary side of high side and low side power supplies
$L_{wiring\_HS}, L_{wiring\_LS}$	Low side and high side from gate driver circuit to power device parasitic inductors
$L_{LS11}, L_{LS12}, L_{LS21}, L_{LS22}, L_{HS11}, L_{HS12}, L_{HS21}, L_{HS22}$	Primary and secondary parasitic inductor of the low side and the high side power supplies
$L_{O\_LS11}, L_{O\_LS12}, L_{O\_LS21}, L_{O\_LS22}, L_{O\_HS11}, L_{O\_HS12}, L_{O\_HS21}, L_{O\_HS22}$	Primary and secondary parasitic inductor of the low side and the high side Op-couplers
$C_{P\_HS1}, C_{P\_HS2}, C_{P\_LS1}, C_{P\_LS2}$	Parasitic capacitors between the primary and the secondary sides of the high side and the low side power supplies
$C_{O\_LS1}, C_{O\_LS2}, C_{O\_HS1}, C_{O\_HS2}$	Parasitic capacitor between the primary and the secondary sides of the low side and the high side Op-to-couplers
$C_{ST1}, C_{ST2}$	Parasitic capacitor between the primary and the secondary sides of the signal transfer unit from the low side to the high side
$L_{ST11}, L_{ST12}, L_{ST21}, L_{ST22}$	Primary and secondary parasitic inductor of the signal transfer unit
$Z_1$	Parasitic impedance between GND1 and GND2, represents totally the parasitic capacitor and the parasitics of the interconnections between GND1 and GND2
$L_{wiring\_opto}, L_{wiring\_power}$	Parasitic inductance from GND1 to devices.

In the high frequency range, the input and the output capacitors of the power supplies and the optocouplers can be shorted. Therefore, the high frequency equivalent model for each isolated device can be compacted as shown on Fig.II.6.

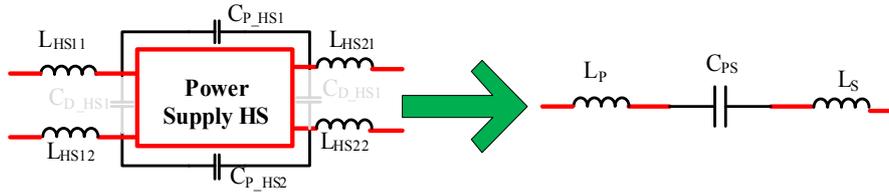


Fig.II.6. High frequency equivalent circuit of an isolated DC – DC power supply

In this equivalent circuit,  $L_P$  and  $L_S$  are the parasitic inductances on the primary side and secondary side, while  $C_{PS}$  is the equivalent parasitic capacitance across the primary side and the secondary side of the power supply.

In Fig.II.7, a simplified high frequency equivalent circuit of the conventional architecture is presented where only two power supplies are taken into account. This simplification is based on the fact that at high frequencies, the gate signal isolation stage and the gate driver supplies are in parallel and that the parasitics of the gate driver supplies are significantly larger than those of the gate signal isolation stage. In the experiment, the datasheets of the elements show that the parasitic capacitance of the power supply is in the range of 60pF – 100 pF. Meanwhile the input-output capacitance of the control signal isolator is about 0.5 pF [69] [70].

To represent the  $dv/dt$  generated at the middle point of the power transistors, a trapezoidal wave voltage source is inserted between the middle point of the equivalent circuit and GND2. The impedance  $Z_I$  in Fig.II.7 represents the common mode impedance between GND1 and GND2. In simulations and experiments, an impedance  $Z_M$  (capacitor in parallel with a resistor) is used to concentrate and to measure the noisy current which circulates in the driver circuit once  $dv/dt$  is applied at the middle point of the power transistors. In brief,  $Z_M$  is an added impedance for the measurement which shorts out  $Z_I$  to ease conducted EMI measurements.

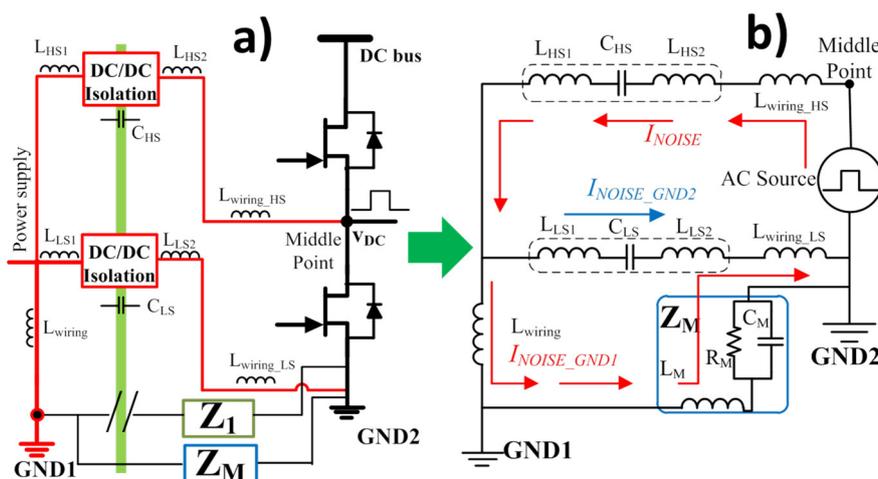


Fig.II.7. Left, high frequency equivalent circuit of the conventional architecture. Right, driver circuit only with the power supplies

The elements of the simplified high frequency equivalent circuit in Fig.II.6 and Fig.II.7 are shown in Table.II.2.

Table.II.2 Elements of the simplified high frequency equivalent circuit in, Fig.II.6, Fig.II.7

$L_{HS1}, L_{HS2}$ $L_{LS1}, L_{LS2}$	Simplified parasitic inductance on the primary and the secondary sides of the high side and the low side power supplies
$L_{wiring\_HS}$ , $L_{wiring\_LS}$	Low side and high side from gate driver circuit to power device parasitic inductors
$C_{HS}, C_{LS}$	Simplified parasitic capacitors between the primary and the secondary sides of the high side and the low side power supplies
$Z_M$	A small impedance is added to measure the noisy current simulations and experiments
$C_M, R_M, L_M$	Parasitic capacitance, resistance and inductance of the measured impedance $Z_M$
$L_{wiring}$	Parasitic inductance from GND2 to devices.

$L_{HS1}$  and  $L_{HS2}$  are the primary and the secondary parasitic inductances of the high side power supply. The parasitic capacitance between the input and the output of the power supply on the high side is represented by  $C_{P\_HS}$ .  $L_{wiring\_HS}$  is the parasitic inductance of the wiring of the high side pathway. On the low side, the same parasitics are given for the power supply and the wiring:  $L_{LS1}$ ,  $L_{LS2}$ ,  $C_{P\_LS}$ ,  $L_{wiring\_LS}$ . On the inputs of the power supplies, a parasitic inductance  $L_{wiring}$  is added.

The noisy currents appear when high  $dv/dt$  is applied at the middle point of the half-bridge, see Fig.II.8b. It circulates at first in the high side driver circuit through the wired devices and then through the parasitic elements. Then,  $I_{NOISE}$  is divided into two parts; the first component  $I_{NOISE\_GND1}$  circulates to GND1 through the wires and their parasitic inductance of the connection  $L_{wiring}$  and the second part  $I_{NOISE\_GND2}$  turns back to GND2 of the power part through the parasitic elements of the low side power supply. We have the estimation of the current ratio as (I.8) is:

$$\begin{aligned}
 \frac{I_{NOISE\_GND2}}{I_{NOISE\_GND1}} &= \\
 &= \frac{2\pi f_{transient} L_{wiring}}{\frac{1}{2\pi f_{transient} C_{PS}} + 2\pi f_{transient} L_{LS1} + 2\pi f_{transient} L_{LS2} + 2\pi f_{transient} L_{wiring\_LS}} \quad \text{II.1} \\
 &\approx 10^{-3} \ll 1
 \end{aligned}$$

As the estimated result of Equation II.1,  $I_{NOISE\_GND2}$  is much smaller than  $I_{NOISE\_GND1}$ , which means that almost all the noisy current  $I_{NOISE}$  in Fig.II.8 goes through the ground of the primary side of the remote control part GND1 as  $I_{NOISE\_GND1}$ .

In these driver circuits, the most important elements that have effects on the noisy current are the parasitic capacitances between the primary side and the secondary side of the isolated DC – DC power supplies.

Based on the method presented above, the high frequency equivalent circuit of the proposed gate driver architecture is shown in Fig.II.8. The wiring of the power supplies in the proposed architecture is presented in Fig.II.8a. Its high frequency equivalent circuit is presented in Fig.II.8b.

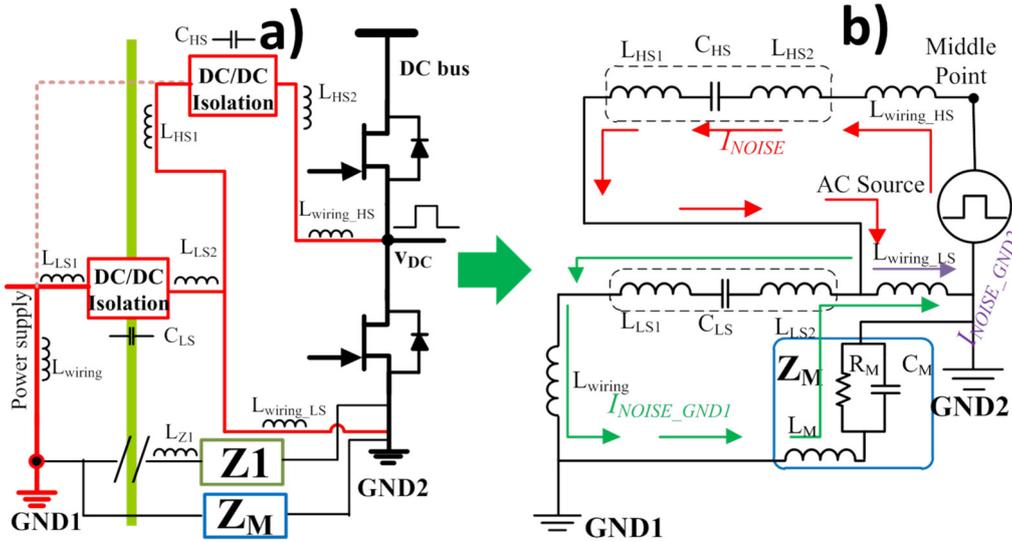


Fig.II.8. Left, high frequency equivalent circuit of the proposed architecture. Right, driver circuit with only power supplies

A noisy current appears when the voltage source generates high  $dv/dt$ , see Fig.II.8b. At first, the noisy current flows through the parasitic elements on the high side supply ( $L_{HS1}$ ,  $L_{HS2}$ ,  $C_{HS}$ ,  $L_{wiring\_HS}$ ) as  $I_{NOISE}$ . Then, this current split in two parts: the first part flows to the GND2 through the parasitic inductance of the wiring  $L_{wiring\_LS}$  as  $I_{NOISE\_GND2}$  while the second part circulates first through the parasitic elements of the low side supply ( $L_{LS1}$ ,  $L_{LS2}$ ,  $C_{LS}$ ) and the parasitic inductance  $L_{wiring}$  toward GND1 as  $I_{NOISE\_GND1}$ . According to equation (I.11), the relation between the currents in this architecture can be shown as:

$$\frac{I_{NOISE\_GND1}}{I_{NOISE\_GND2}} = \frac{2\pi f_{transient} L_{wiring\_LS}}{\frac{1}{2\pi f_{transient} C_{PS}} + 2\pi f_{transient} L_{LS1} + 2\pi f_{transient} L_{LS2} + 2\pi f_{transient} L_{wiring}} \quad II.2$$

$$\approx 10^{-3} \ll 1$$

In this case, a very small amount of the noisy current circulates from the power module to the ground of the primary side of the remote control circuit GND1 as  $I_{NOISE\_GND1}$ .

As a matter of fact, the current which goes to the ground of the primary side of the control circuit could be reduced even more by minimizing the parasitic inductance  $L_{wiring\_LS}$ . In Fig.II.9, an equivalent circuit without the  $L_{wiring\_LS}$  is depicted and the total amount of noisy current circulates in the loop of the DC source, no more current goes through GND1. The value of  $L_{wiring\_LS}$  could be reduced if the gate driver and the power supply of the high side are designed to be connected as close as possible to the GND2 of the power part. The most important issue is to limit the common traces between the low side supply and the high side supply to the GND2.

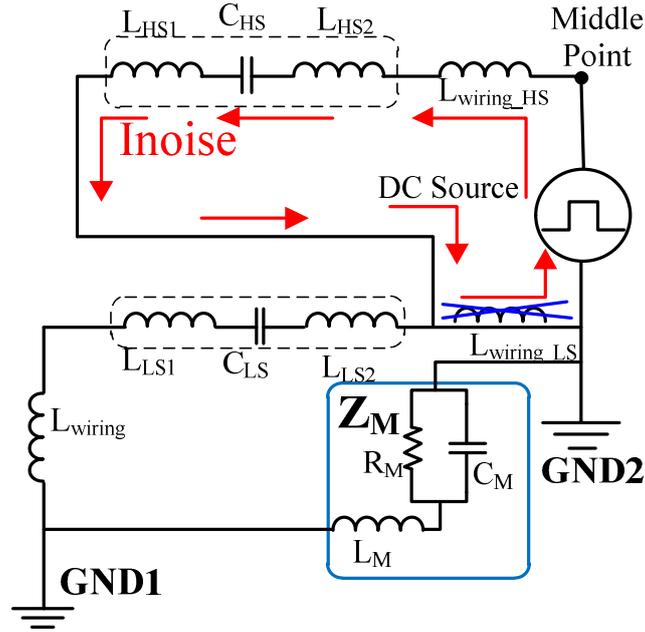


Fig.II.9. High frequency equivalent circuit of the proposed architecture with improvement

To validate the presented analysis, three simulations are presented in the next section. In the first and second cases, the equivalent circuits of the conventional and the proposed architectures are simulated. Then, the value of  $L_{wiring\_LS}$  is reduced in the last simulation to evaluate the decrease of the noisy current which circulates in the remote control circuit.

### II.2.c Simulation comparisons of the conventional and the proposed architectures

To carry out electrical time domain simulations, a value for each element of the equivalent circuit is needed. The values used in the simulations are derived from the experiments.

The primary to secondary equivalent impedance of the power supply TRACO TMA1515s which will be used in the experiments to supply the low side and the high side of the gate driver is characterized in Fig.II.10. At 66 kHz, the impedance plot shows a capacitive impedance of 28 k $\Omega$ . Based on these values, the capacitor can be calculated:

$$C_{traco} = \frac{1}{2 \times \pi \times 66 \text{ kHz} \times 28 \text{ k}\Omega} = 86 \text{ pF} \quad (\text{II.3})$$

In this plot, the resonant point is at 75 MHz, therefore the inductance of the power supply TMA1515s can be determined as follows:

$$L_{traco} = \frac{1}{(2 \times \pi \times 75 \text{ MHz})^2 \times 86 \text{ pF}} = 55 \text{ nH} \quad (\text{II.4})$$

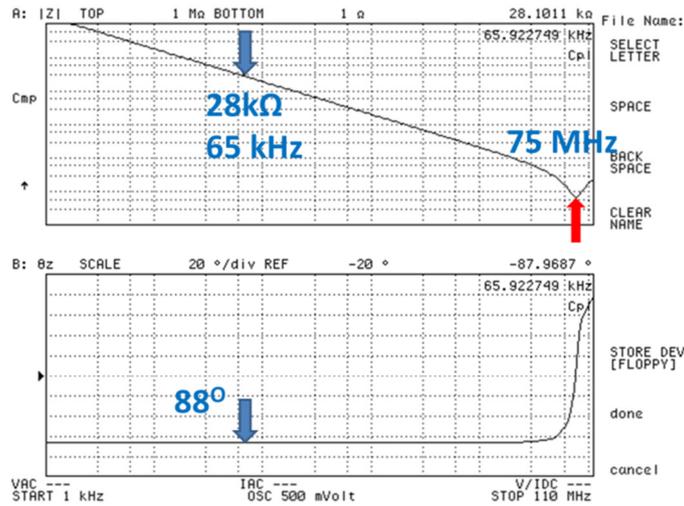


Fig.II.10. Primary – secondary impedance of the power supply TRACO TMA1515S.

A simulation tool InCa3D™ is used to estimate the parasitic inductance of the printed circuit board with the same geometry and the thickness of the conductor. InCa3D™ [71] (developed by CEDRAT and G2ELab) allows us to estimate the conductor impedance and near field of the electrical connections. The PCB layout of the experimental circuit has been imported into InCa3D™ to evaluate the parasitic inductance  $L_{wiring\_LS}$ , introduced in Fig.II.8.

The complete PCB layout of the power transistors and the conventional gate driver architecture is depicted in Fig.II.11. The layout into the black square is not considered into the simulations and is replaced by an equivalent disturbance source.

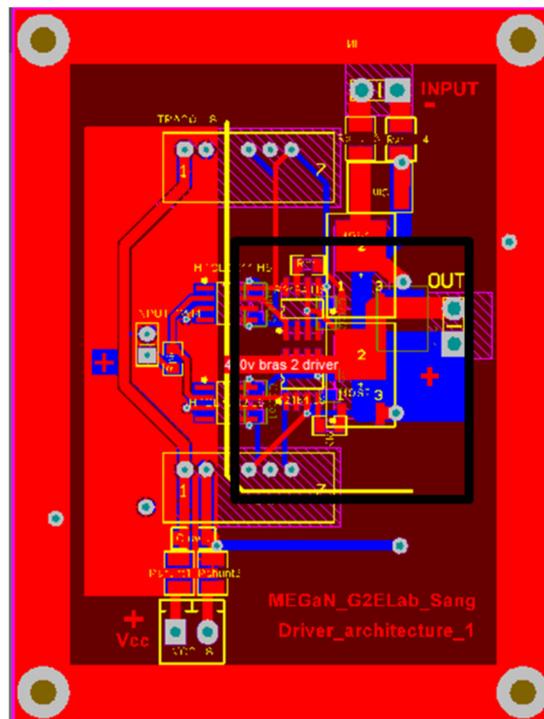


Fig.II.11. PCB layout of the conventional gate driver architecture

Fig.II.12 represents the simplified PCB traces between the output of the low side power supply and GND2 – the ground of the power part.

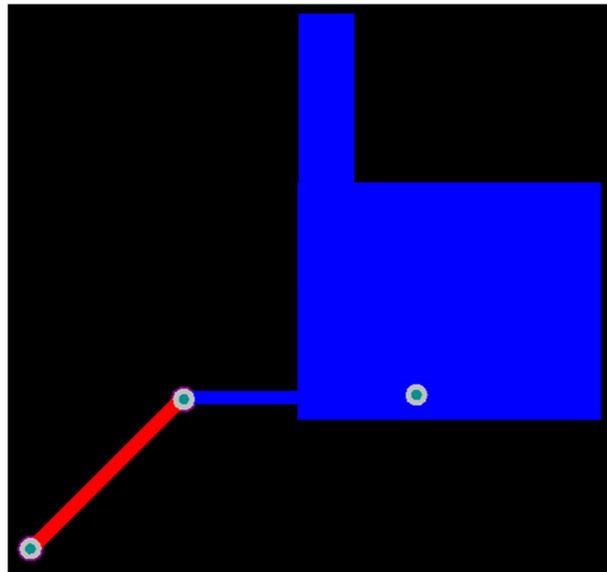


Fig.II.12. Simplified conductors between the GND2 and output of the low side power supply

Then, Fig.II.13 shows the modeled geometry in InCa3D of a sector of a standard 2 layers PCB with a copper thickness of  $35\mu\text{m}$ . The parasitic inductance  $L_{\text{wiring}_{LS}}$  of 16 nH has been extracted at 100 kHz in InCa3D for 18 mm of the length distance between two terminals.

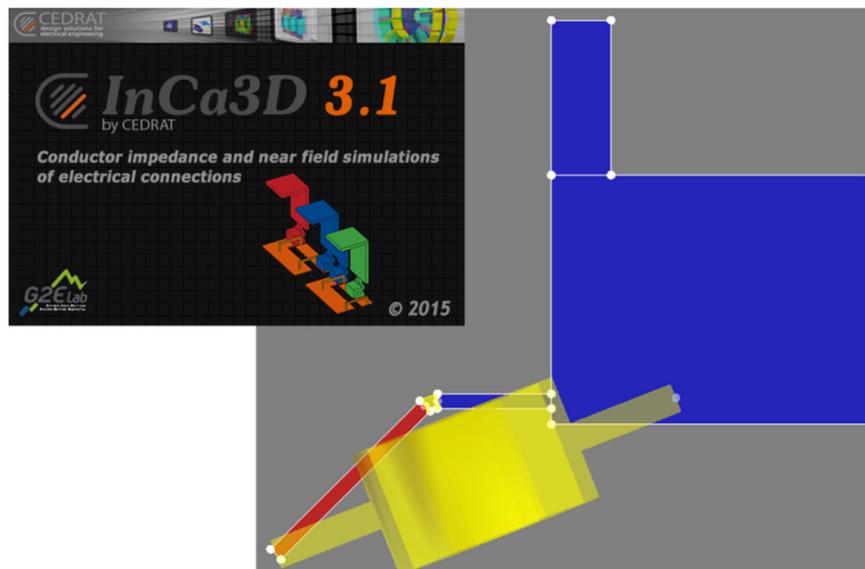


Fig.II.13. Modeled geometry in InCa3D

All parasitic inductance values have been estimated by using the length distance of the PCB traces. Since we do not consider the coupling between tracks which is completely equivalent and to simplify the value extraction in InCa3D, we decided to simulate a partial circuit. The other values are estimated through the length distance between two terminals.

For other parasitic inductances, the wiring parasitics  $L_{\text{wiring}_{HS}}$  and  $L_{\text{wiring}}$  are estimated based on the length distance of the trace between the terminals. The estimated values of the parasitic inductances are shown in Table.II.3.

Table.II.3 Estimate parasitic inductances of the connections

	Length distance of the PCB trace	Estimated value
$L_{\text{wiring\_HS}}$	25 mm	20 nH
$L_{\text{wiring}}$	15 mm	10 nH

Fig.II.14 shows the rising edge of the waveform of the single ramp voltage source used in the experiments. The amplitude is 250 V and the rising time is 15 ns which gives an average  $dv/dt$  of 16V/ns that will be considered in the simulations.

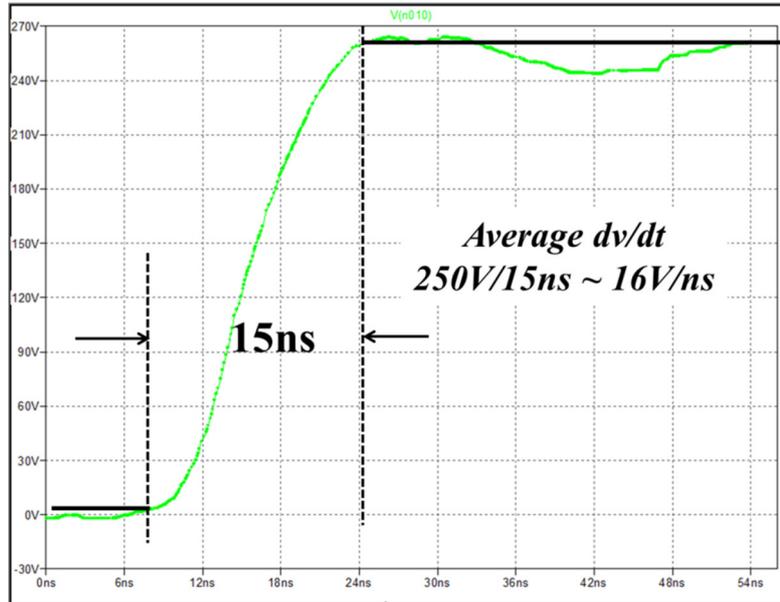


Fig.II.14. Screen shot of the power side middle point voltage rising.

Fig.II.15 shows the schematic used in the software SIMPLORER™ to simulate and to analyze the transient waveforms of the conventional architecture. The values of the parasitic elements of the high side and the low side power supplies are considered identical. The parasitic capacitances of the isolation  $C_{HS}$  and  $C_{LS}$  are 86 pF; the parasitic inductances  $L_{HS1}$ ,  $L_{HS2}$ ,  $L_{LS1}$  and  $L_{LS2}$  on the primary side and the secondary sides of the power supplies are 27.5 nH. Thus, the total parasitic inductance is 55 nH.

The fictive impedance  $Z_M$  has a parasitic inductance of 10 nH and a capacitance of 1 nF connected in parallel with a resistance of 10 MΩ. In fact, the parasitic impedance between the middle point of the power transistors and the ground of the remote control GND2 cannot be accessed by the current probe. Therefore, in both simulation and experiments, this impedance  $Z_M$  has been externally added to the circuit in order to measure the noisy current. The parasitic capacitance of the low side and the high side power supplies is expected to be less than 100 pF, thus a capacitor of 1 nF has been implemented between  $GND1$  and  $GND2$  to measure more than 90% of the noisy current. The resistor of 10 MΩ is a parasitic resistor between two grounds; the inductor of 10 nH represents 10 mm length of interconnections.

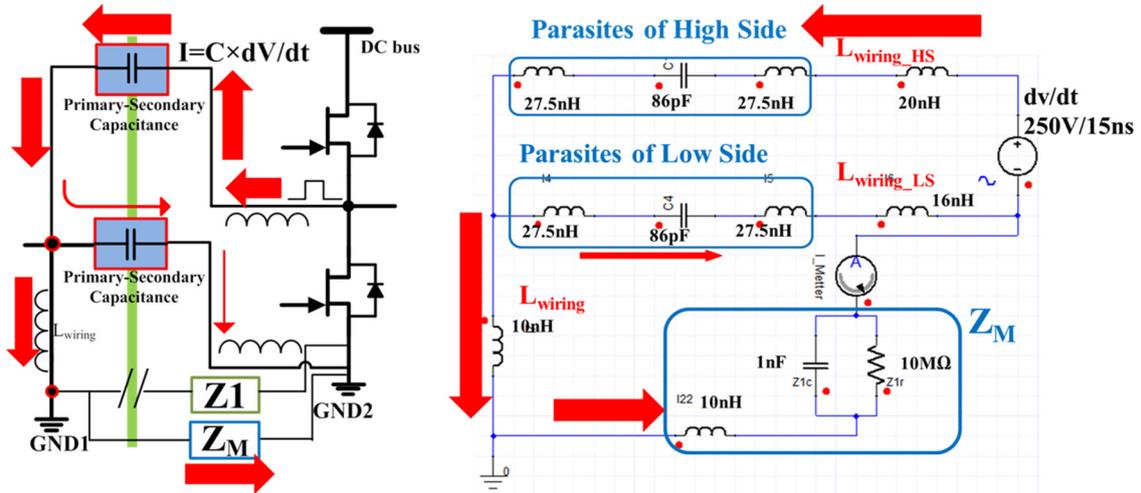


Fig.II.15. Conventional architecture: Left, schematic circuit. Right, SIMPLORER circuit

Fig.II.16 shows the simulation schematic of the proposed architecture. A large amount of parasitic inductances is still present since the output of the power supply on the low side is directly connected to the input of the power supply on the high side. The parasitic inductance on the low side power supply is 16 nH which corresponds to the wirings of the real circuit.

The above schematics are used in simulations to validate the analysis presented in the previous section, and to quantify the differences between the different cases. Fig.II.17 and Fig.II.18 show respectively simulation results of the conventional architecture and the proposed architecture.

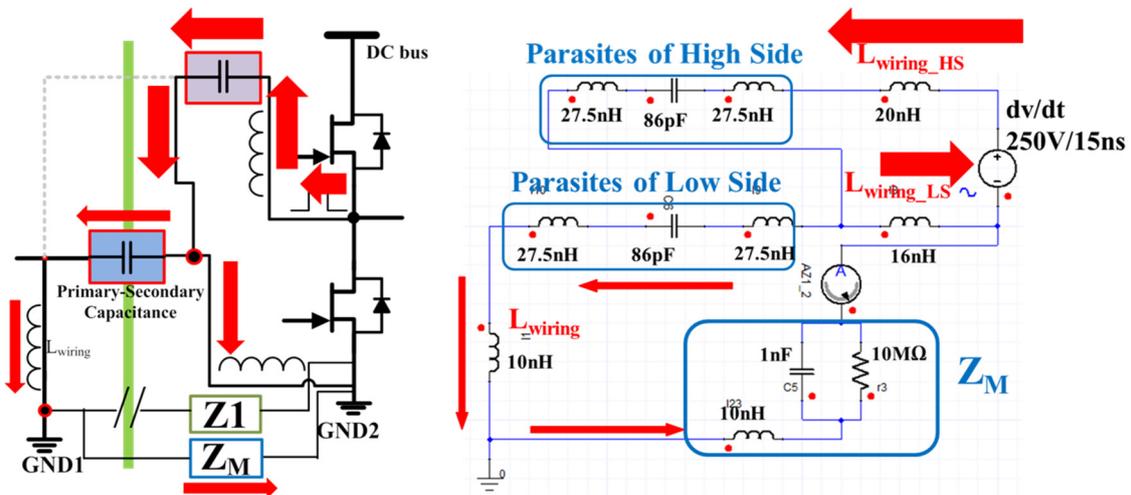


Fig.II.16. Proposed architecture: Left, schematic circuit. Right, SIMPLORER circuit

In these simulations, at the moment  $t = 0 \text{ sec}$ , the voltage source is 0 V and there is no  $dv/dt$ . At  $t = t_0$ , the single ramp voltage source produces a  $dv/dt = 16 \text{ V/ns}$  up to 250V.

As we can see in Fig.II.17, in the conventional architecture, a noisy current with 3.3 A peak to peak amplitude is circulating through  $Z_M$ . This current is reduced significantly to 0.41 A peak to peak in the proposed architecture as shown in Fig.II.18.

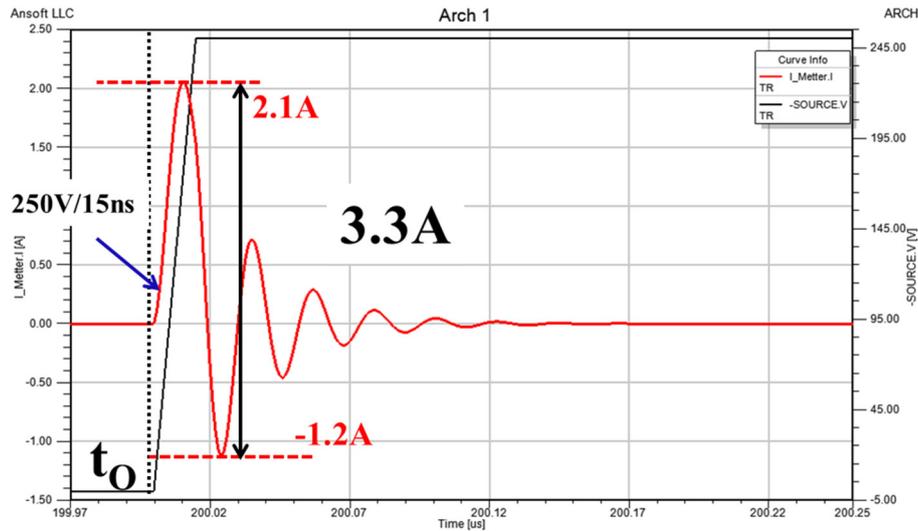


Fig.II.17. Noisy current in  $Z_M$  for the conventional architecture, simulation results

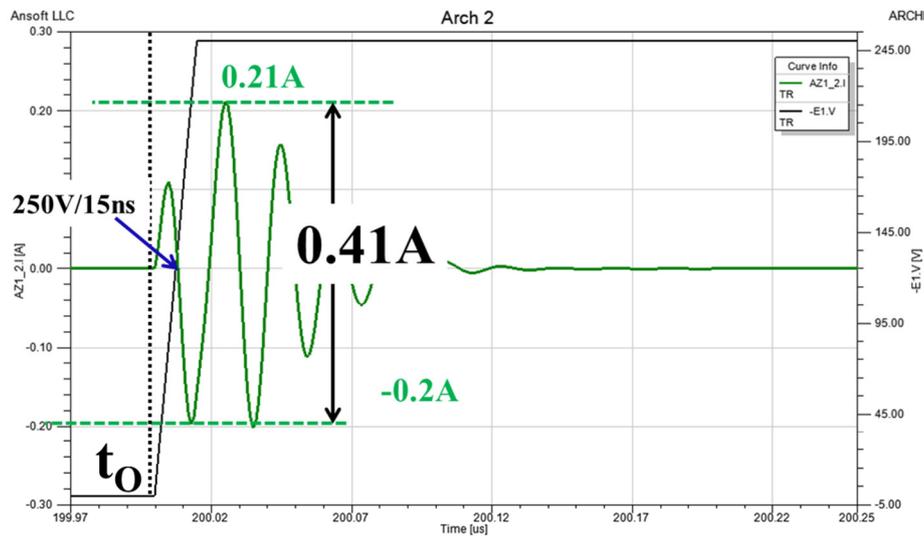


Fig.II.18. Noisy current in  $Z_M$  for the proposed architecture, simulation results

These simulation results indicate the advantage of the proposed architecture in terms of common mode noisy current reduction and as a consequence of conducted EMI.

Nevertheless, the location of the high side power supply will be now investigated to improve even more the conducted EMI perturbation in the gate driver circuit in the next section.

#### II.2.d Improved proposed gate driver architecture for the EMI management

As mentioned before, in the gate driver circuitry, the connection point of the output of the low side power supply and the input of the high side power supply should be as close as possible to the ground of the power part in order to minimize the parasitic of the interconnections.

In Fig.II.19, the parasitic inductance due to the wiring on the low side has been reduced to 8 nH thanks to an improved wire routing.

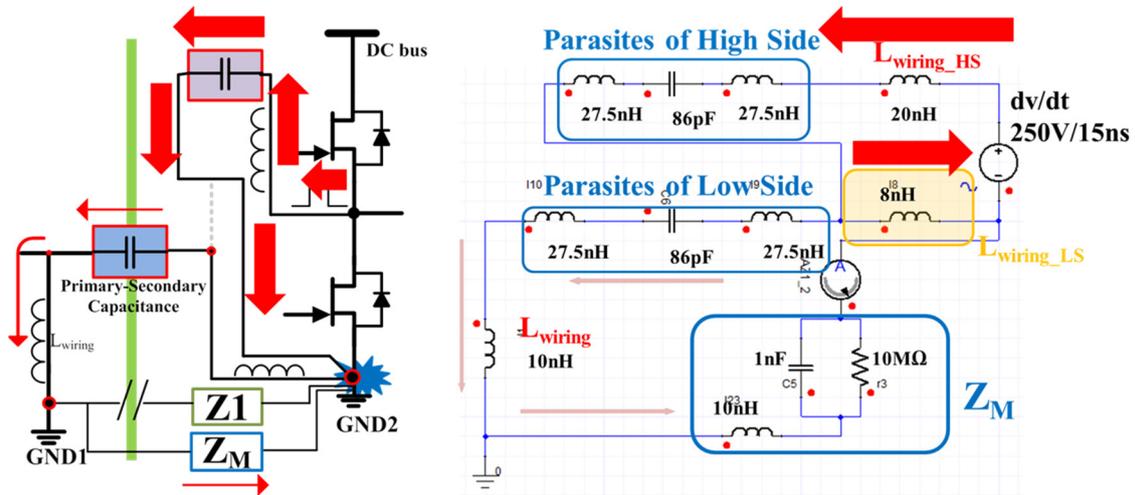


Fig.II.19. Proposed architecture with the improved routing: Left, schematic circuit. Right, SIMPLORER circuit

The simulation result is shown in Fig.II.20 for a proposed gate driver circuit with an improved wire routing. The noisy current is reduced down to 0.18A peak to peak. In reality, an amount of the noisy current to GND1 can be more reduced but always exists because the parasitic inductance of the interconnection cannot be eliminated.

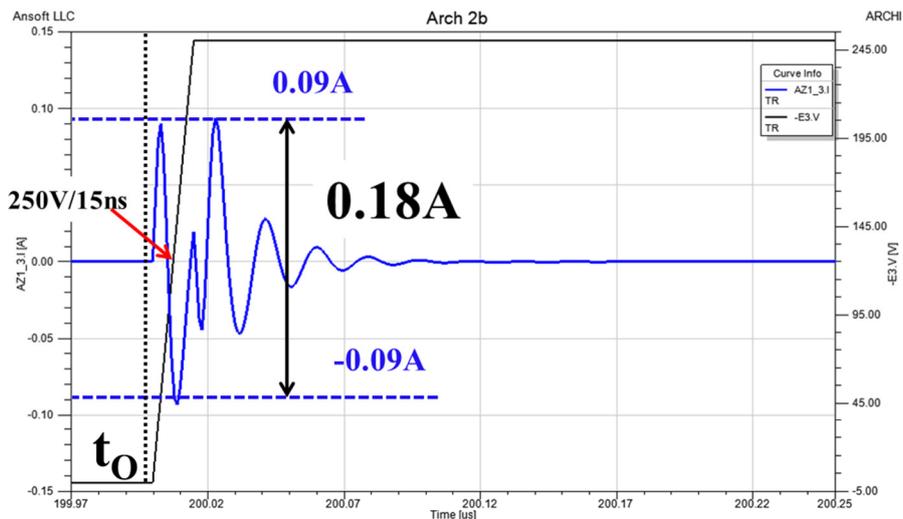


Fig.II.20. Noisy current in  $Z_M$  of the proposed architecture with improved wire routing, simulation results

In this case, the high side power supply must be close to the power parts for reducing the interconnections. The more parasitic inductances can be decreased, the less noisy current will circulate through the remote control part.

However, it is now important to evaluate if the high side power supply needs to be itself close to the power side or if only its interconnect needs to be well addressed.

With these reasons, another solution is presented in the next section as a compromised solution.

### II.2.e Compromised solution

The simulation circuit is shown in Fig.II.21. The parasitic inductance due to the wiring on the low side is always equal to 8 nH by maintaining the connection point identical but the high side power supply is brought out of the power part region. Simulation result in Fig.II.22 shows the noisy current in this

## II.3 Experimental validations of a high side – low side configuration’s gate driver

case. It increases slightly, up to 0.20 A peak to peak. The high side power supply can be connected away from this point of view, making possible to operate it at lower temperature.

In another hand, the negative consequence is to increase the parasitic inductances of for the high side power supply line. The antenna phenomena should be considered since the system is working in a high frequency range.

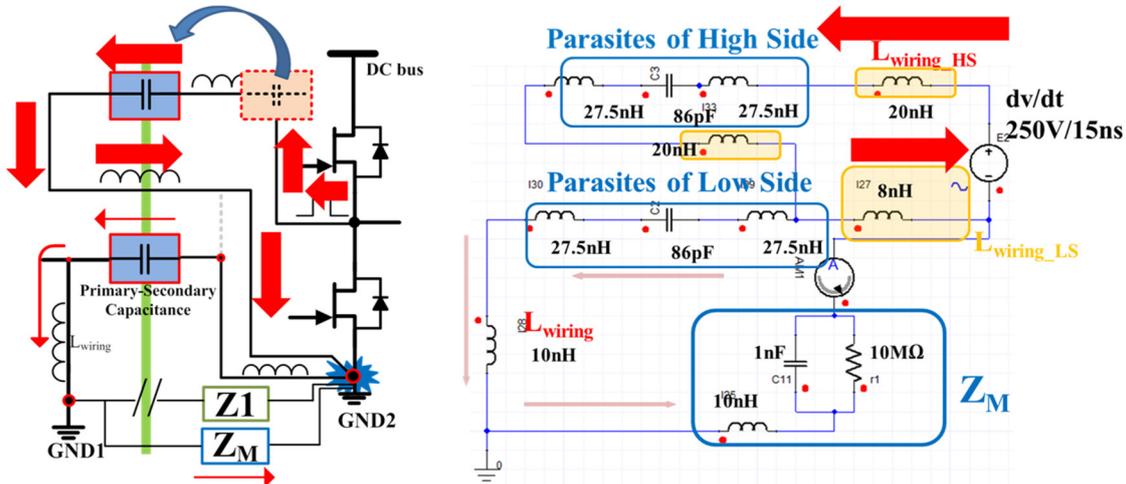


Fig.II.21. Left, schematic circuit. Right, SIMPLORER circuit of compromised solution of the proposed architecture

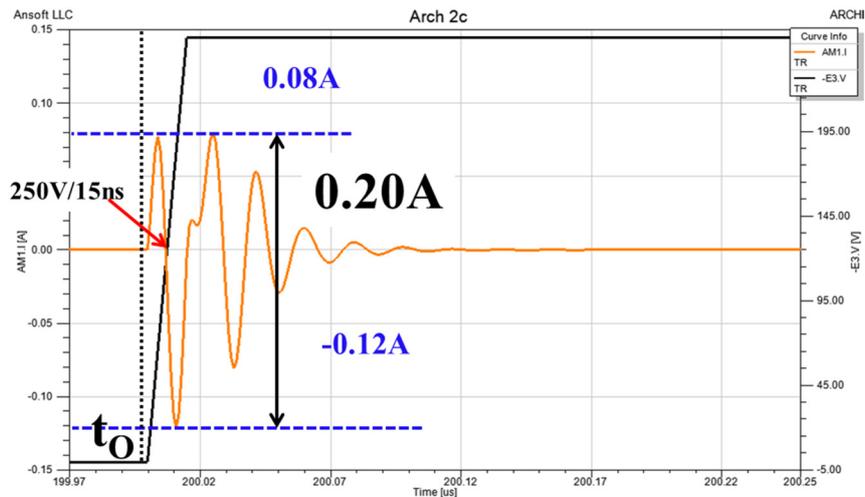


Fig.II.22. Noisy current in  $Z_M$  of compromised solution, simulation results

In the next section, the experimental validations will be demonstrated for 4 cases as investigated in the simulations.

## II.3 Experimental validations of a high side – low side configuration’s gate driver

### II.3.a Set-up for measuring the conducted EMI common mode current

The noisy currents between  $GND1$  and  $GND2$  are measured in the experimental setup depicted in Fig.II.23. High  $dv/dt$  can be produced by any device, not only WBG devices but also with classical Si power devices. In these robust experiments, transistors CoolMOS have been used.

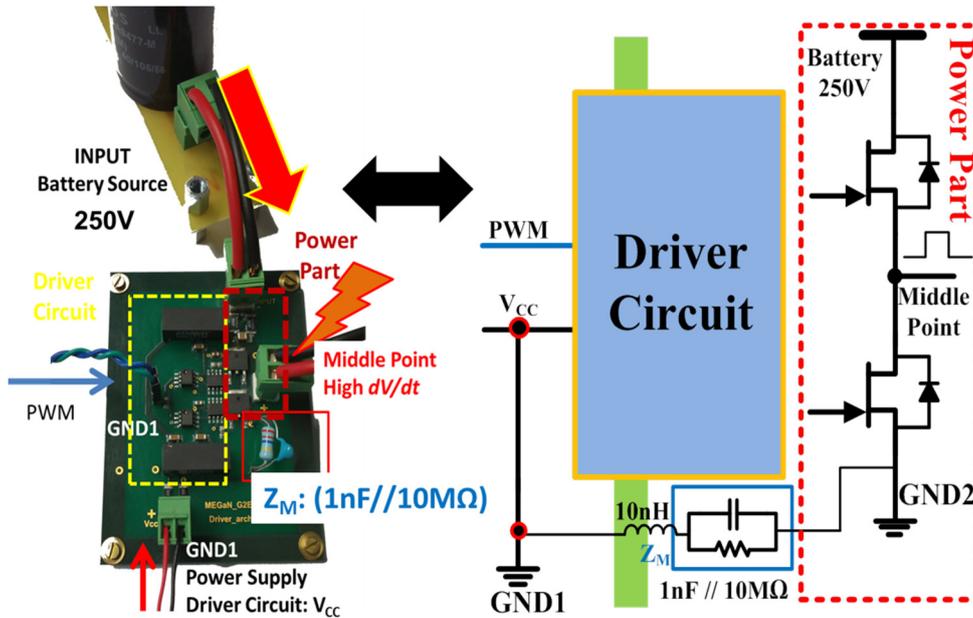


Fig.II.23. Experimental setup to separate physically GND1 and GND2

The DC-DC power supplies and the optocouplers make a strong isolation between the driver circuit and the power module. To physically separate *GND1* and *GND2*, a battery of 250 V has been used as input power for the power side.

An auxiliary 15 V power supply is used for powering the driver circuit; a function generator was used to generate the control signal of the remote control part. This 15V power supply and this function generator are powered by the grid.

The power side was supplied on batteries to ease measurements but also to simplify the use and implementation of a function generator to produce the driving signals. Most of all, the measurement devices could also be supplied directly on the means thanks to this choice. A control signal PWM with 50% duty cycle and 100 kHz frequency is used to drive the power transistors. Between the *GND1* and *GND2*, additional artificial impedance  $Z_M$  of 1 nF and 10 MΩ has been used to represent the impedance between *GND1* and *GND2*.

Table.II.3 shows the list of devices used in the test circuits.

Table.II.3 Elements of experiments

POWER PART (GND2)	Power Source	250 V battery bank
	Power transistors 400V	IRFR310PBF
DRIVER CIRCUIT (GND1)	DC- DC power supply	TRACO - TMA 1515S Nominal current 80 mA
	Control signal isolator	OPTO HPCL 2211
	Gate Driver	IR2184
MEASURE	Artificial Impedance $Z_M$ between GND1 and GND2	1 nF // 10 MΩ

**II.3.b Experimental Results**

Fig.II.24 shows the circuit with the conventional architecture of the driver circuit. In this circuit, an inverter leg is implemented with two independent control signals. Each driver is implemented with its own isolated power supply, optocoupler and gate driver. The schematic of this circuit is presented in Fig.II.1.

The noisy current through the driver circuit in the conventional architecture has been measured in Fig.II.25. It can be observed, the  $dv/dt$  of 16 V/ns at the middle point of the power inverter leg generates 4.2 A peak to peak noisy current.

This current circulates in the high side DC/DC power supply whose nominal current is 80 mA. A higher  $dv/dt$  would increase the noisy current and could alter not only the power supply but the other elements of the driver circuit as well.

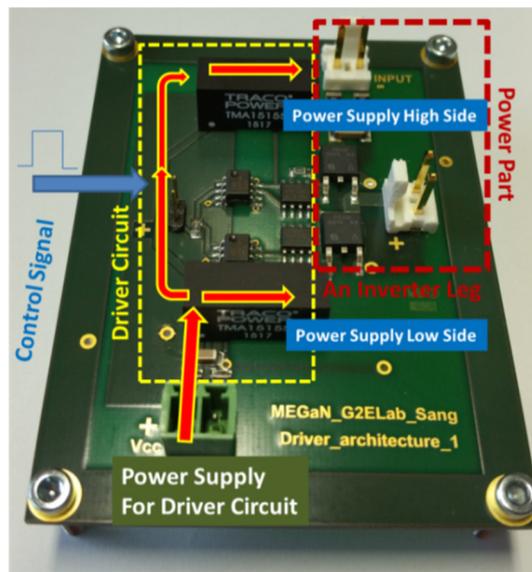


Fig.II.24. Experimental circuit with conventional gate driver architecture

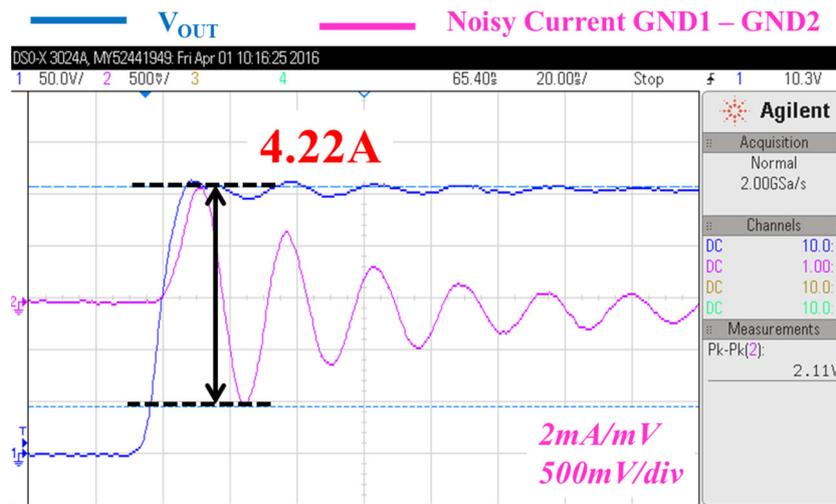


Fig.II.25. Noisy current between GND1 and GND2 in conventional architecture, test circuit and experimental results

Fig.II.26 shows a picture of the circuit of the proposed architecture. Two isolated power supplies, one optocoupler and one gate driver with integrated level shifter have been implemented to control both low side and high side of the power inverter leg. Fig.II.3 shows the schematic of this circuit.

In Fig.II.27, the measured noisy current is reduced by a factor 10 with 0.42 A peak to peak amplitude even though the wiring still causes a large parasitic inductance between the output of the low side power supply and between the high side power supply and  $GND2$ .

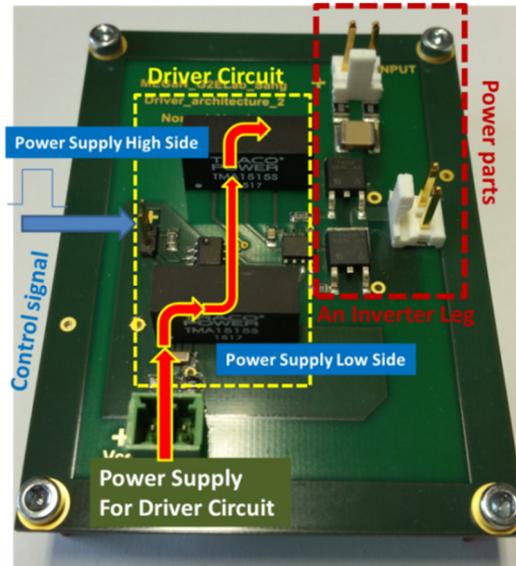


Fig.II.26. Circuit with proposed gate driver architecture

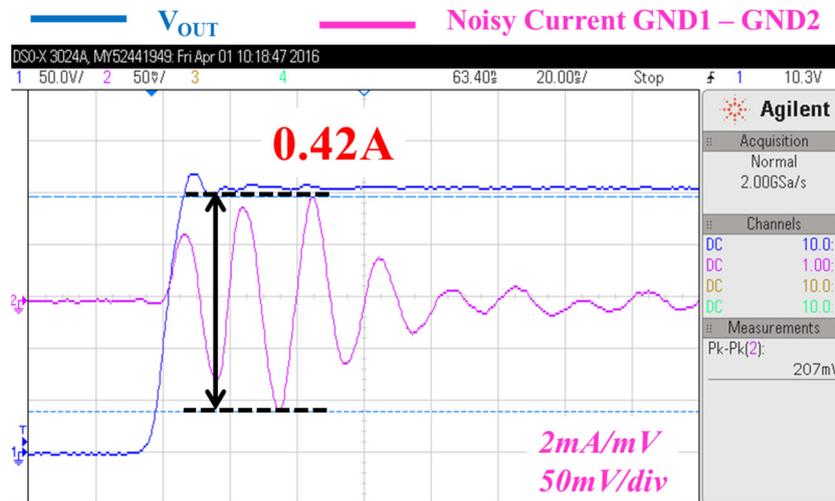


Fig.II.27. Noisy current between  $GND1$  and  $GND2$  in the proposed architecture

A second version of the PCB of the proposed architecture is designed with modified track routing to minimize the undesirable parasitic inductance of the wiring on the low side, see Fig.II.28. In this circuit, the high side power supply is placed on the bottom side right beneath the power part.

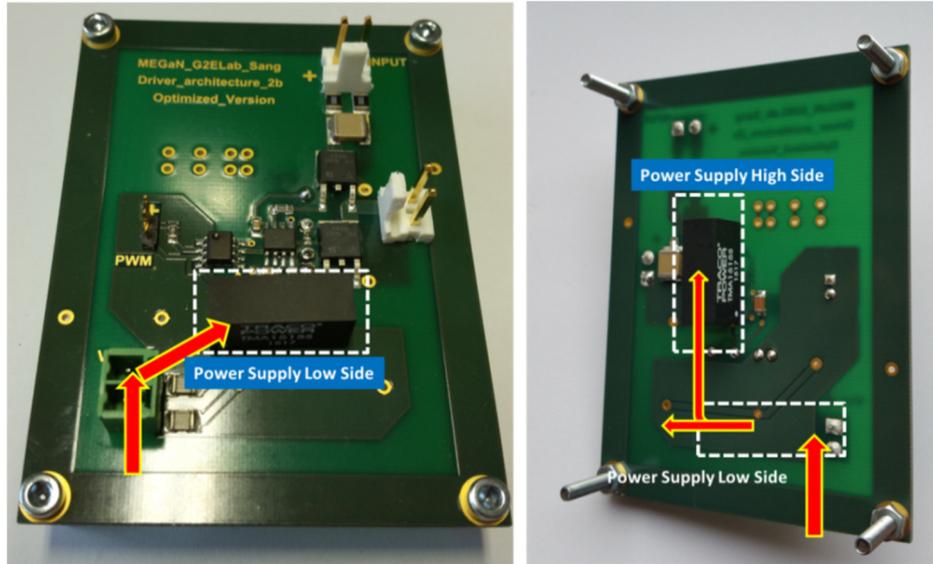


Fig.II.28. PCB circuit with top view and bottom view of the proposed architecture with improved wire routing,

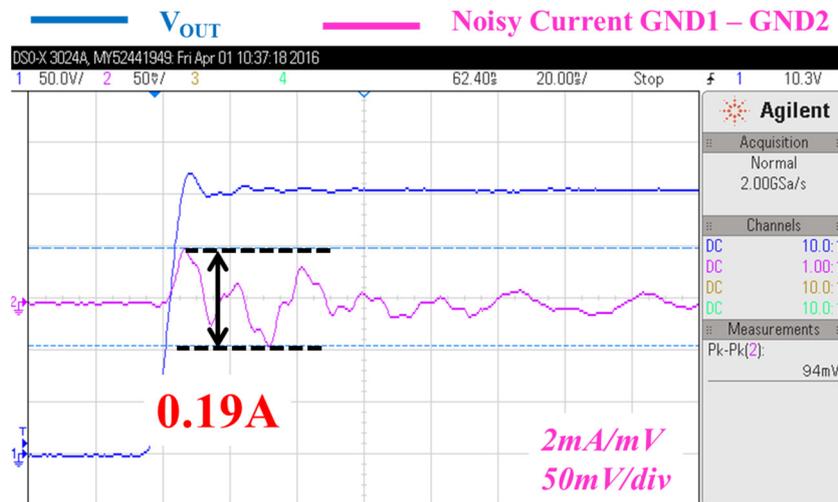


Fig.II.29. Experimental result of the noisy current between GND1 and GND2 in the proposed architecture with improved wire routing

On the PCB traces, the parasitic inductance of the wirings can be minimized but not completely eliminated. The optimization has a significant effect on the common mode noisy current. As it can be observed in Fig.II.29, the peak of the noisy current is drastically reduced by a factor 20 in comparison with the conventional architecture.

The last experiment corresponds to the “compromised” solution, the connection points between the output of the low side power supply and the input of the high side power supply are always close to the ground of the power part.

In this case, the footprints for the high side driver supply is reproduces outside of the power part to evaluate the impact of the location of the supply on common mode conducted EMI.

Fig.II.30 introduces the two physical locations for the high side gate driver power supply

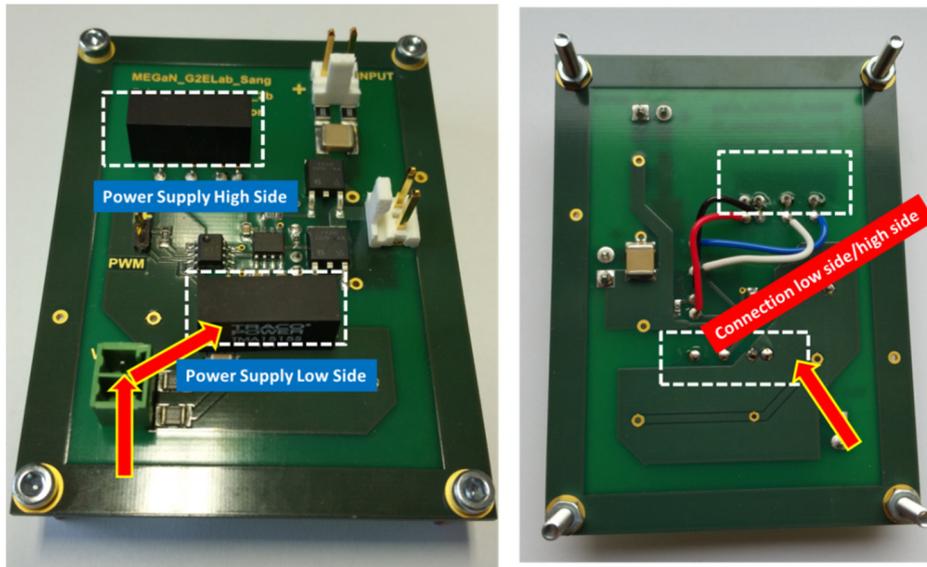


Fig.II.30. Compromised architecture circuit

Fig.II.31 shows the practical result for the “compromised” solution, where the noisy current between GND1 and GND2 is 0.21A.

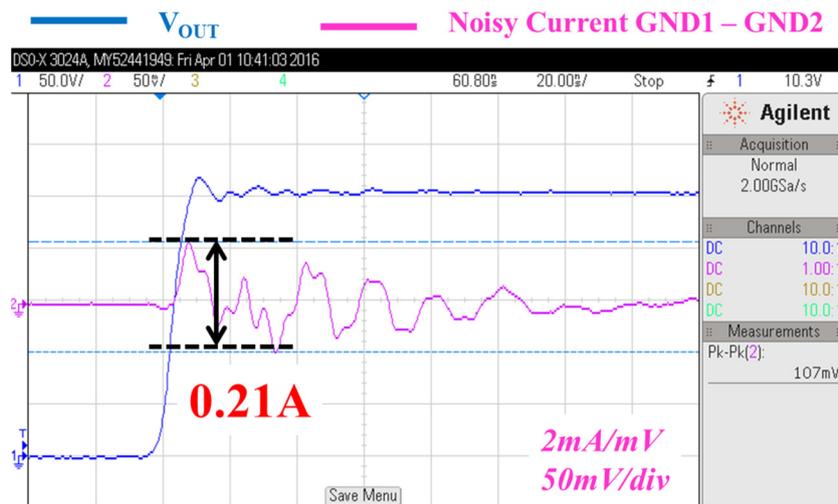


Fig.II.31. Noisy current between GND1 and GND2 in the compromised solution of the proposed architecture gate driver

In Fig.II.32, the experimental results of four circuits have been compared. As it can be observed, the noisy current as the conducted common mode EMI perturbation is decreased with a ratio of 10 from the conventional to the proposed gate driver architecture. In the third case, the proposed architecture has been optimized with a precise connection point for the driver supplies, and then the noisy current is reduced even more from 0.42 A to 0.19A peak to peak.

In the last case, the high side power supply has been brought away from the power part but the important connection point is unchanged. The noisy current as the conducted EMI perturbation increases slightly but great reduction can still be observed. Of course, one must keep in mind that there is a risk of adding the radiated EMI perturbation at the high frequency and this is left for future work.

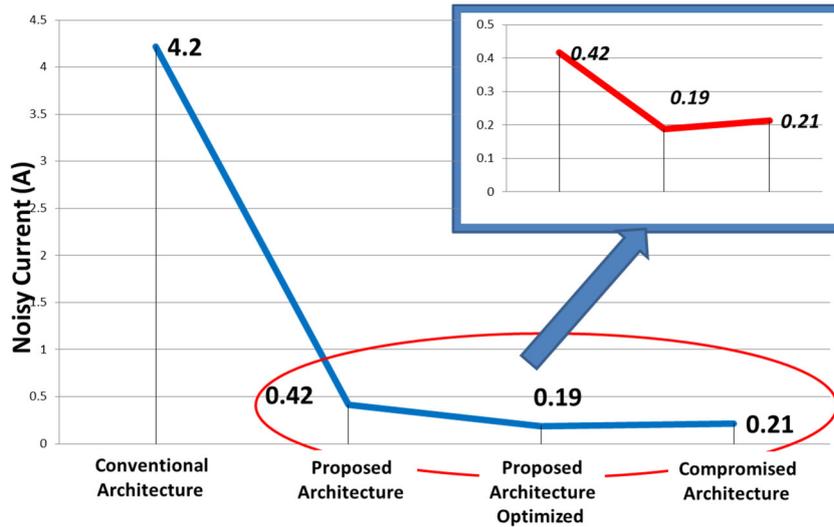


Fig.II.32. Noisy currents in the 4 different cases, experimental results

In both simulation and experimental results, the proposed architecture demonstrates significant reduction of the noisy current which is generated from the power part then may disturb the remote control signal.

With the proposed approach, almost all noisy current returns directly to the power module instead of circulating in the driver circuitry to the ground of the remote control circuit before coming back to the power module. In the next section, we present the recommendations and the notices for designing a gate driver circuitry for the high speed power devices.

### II.3.c Comparison of the switching speed of the power devices

The switching speed of the power devices has been slightly improved thanks to the modifications the gate driver architecture.

Fig.II.33 shows the speed  $dv/dt$  on the vertical axis and the horizon axis corresponds to the data point. As we can see in the results, the maximum  $dv/dt$  of the conventional architecture is 38.9 V/ns; the maximum switching speed of the proposed architecture is 40 V/ns.

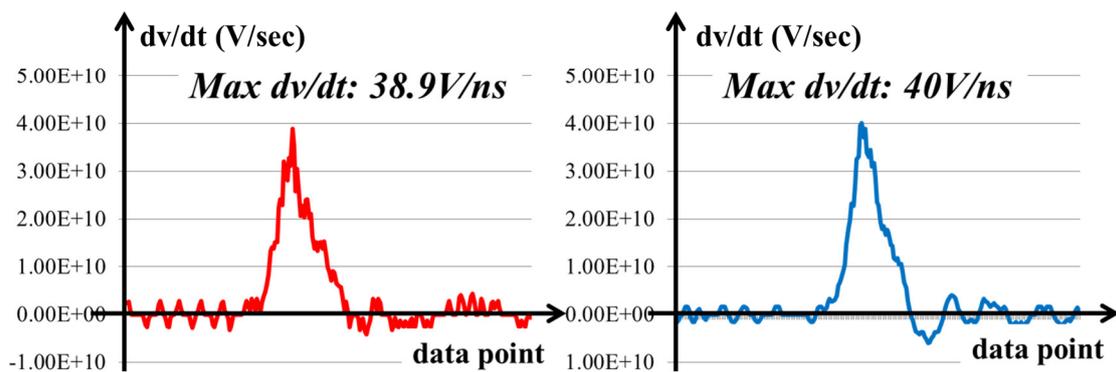


Fig.II.33  $dv/dt$  on each point of the rising voltage of the conventional architecture (left) and the proposed architecture (right)

The parasitic capacitance of the middle point to GND1, the noisy current and the parasitic values of the interconnection could have impact to the speed of the power devices.

Further works need to investigate the switching speed of the power devices in the different architectures of the gate driver circuit.

### **II.4 Recommendations for the design of HF power modules with high $dv/dt$ and in a harsh environment**

#### **II.4.a Recommendations for the locations of the elements of the gate driver circuitry**

These works focus on the improvement of the implementation of wide band gap devices in power modules with respect to the EMI management and especially to the conducted and radiated EMI perturbation in common mode. The system could be damaged by a large amount of the noisy current that may flow through the control parts if we do not pay high attention on the implementation of the control side of the power module.

Several works in the literature have pointed out the need to care about how gate drivers must be implemented close to the power devices [56] [57] [58]. By presenting in Chapter I and validating in Chapter II, it is clear that the gate drivers should be as close as possible to the power devices in order to minimize parasitic inductances limiting the speed of the gate charge and clamping for  $dv/dt$  immunity purposes.

Conventional power modules with external gate driver circuits seem to be no more adapted to an effective implementation of very high speed power devices. The best solution would be to integrate the gate drivers within the power modules [59] [60]. However, additional recommendations should be pointed out to really optimize their integration.

This work has clearly shown that it is important to supply the high side gate driver supply and to transfer the control signals through the low side gate driver circuitry. Cascaded circuitry with locally generated and isolated control signals and supplies would be the best solution.

The validations have also highlighted that this high side gate driver supply should be connected as close as possible to the reference potential of the power switching cell, i.e. named in this work *GND2*.

In this case of a low side – high side configuration, four essential elements should be implemented very close to the power transistors and/or connected in a very specific manner: two buffers of the gate driver and their associated decoupling capacitors to drive the low side - high side power devices. The high side gate driver power supply and the high side control signal transfer unit should be referenced to the ground of the power part, their location being less critical from the conducted common mode current point of view.

On the other side, the low side isolated gate driver supply as well as the low side isolation units for the gate signals do not have to be specifically integrated or close to the power module. And the isolation of the high side power supply and the isolation unit are less constrained.

This chapter has clearly underlined that efforts must be engaged not only toward the design, the qualification and the implementation of gate drivers but also toward the gate driver supplies and gate driver control signal transfer unit. Moreover, in what refers to the supplies, the cascaded architecture of the gate driver supplies and control signal isolation units should also be considered as an issue for advanced and high switching speed implementations.

Fig.II.34 illustrates the two regions of operational temperature and also the cascaded architectures to be implemented for proper EMI common mode path reduction.

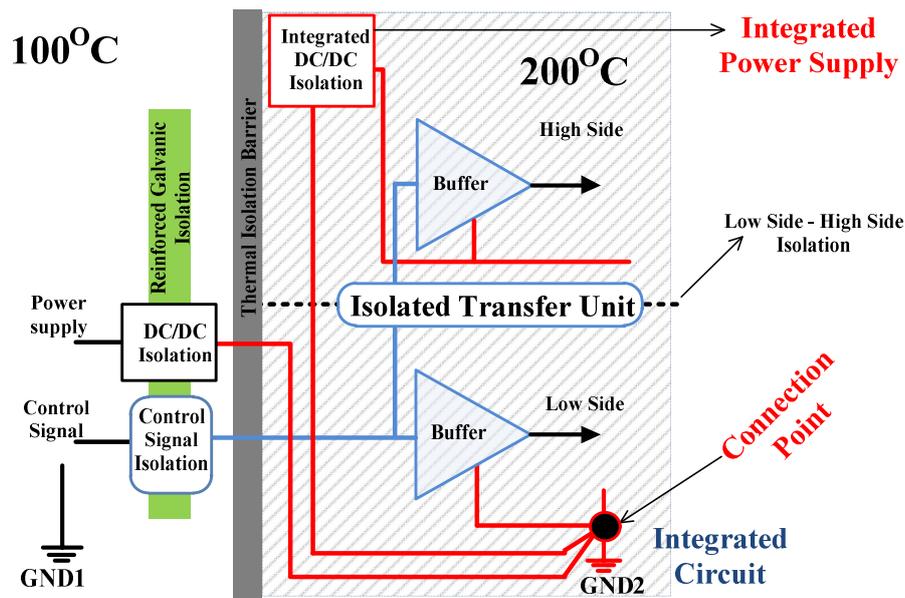


Fig.II.34. Circuit diagram of the gate driver for the proposed architecture

#### II.4.b Two options for the high side power supply of the gate driver circuit

The high side power supply should be cascaded after the low side power supply and connected to as close as possible to the reference potential of the power part GND2. The output decoupling capacitor of the low side gate driver supply should be connected as close as possible to GND2 as well in order to minimize high frequency common paths between low side and high side circuitries. The high side gate driver supply can be physically integrated within the power module but do not have to be placed very close to the switching cell since it is mainly its interconnection location which is critical.

The simulation and experimental results approved two possibilities for the high side power supply location: Fig.II.35.

- The first option is to bring the high side power supply inside the high level thermal zone in order to optimize the conducted EMI as well as to minimize the radiated EMI perturbations. This solution requires a high temperature technology for the high side isolated power supply.
- The second option is a compromised solution, the high side isolated power supply is brought to outside of the thermal zone, and however, the critical connection points are remained. Obviously, the high temperature power supply is no more needed. The disadvantages of this solution are to increase the conducted EMI perturbation and might generate more radiated EMI perturbations.

## II.5 Expectations on the gate driver architectures for the power devices in series connection configuration

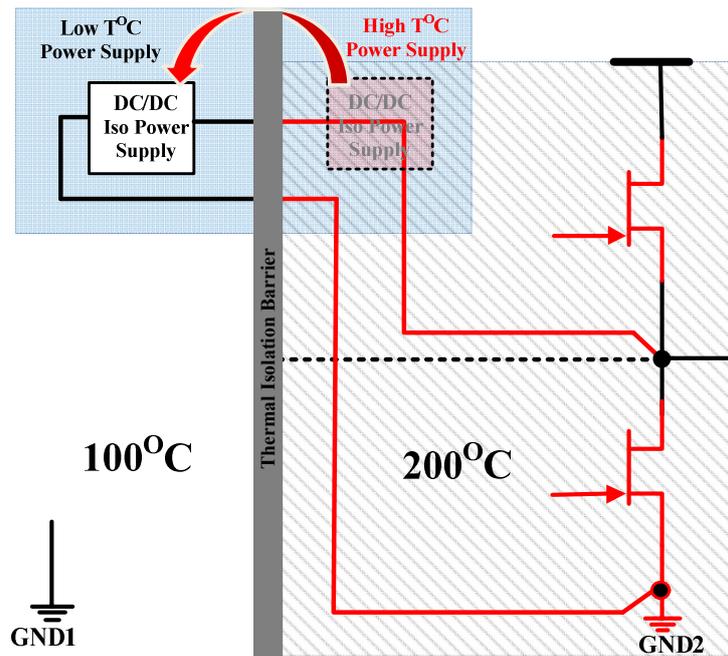


Fig.II.35. Two options for the high side DC-DC isolated power supply

Optimizing the implementation of gate driver circuitry, gives us the opportunity to minimize common mode currents. Nevertheless, it does not influence the level of parasitic currents circulating through the components. During the experiments, several supplies were destroyed due to excessive  $dv/dt$  leading to large parasitic currents able to damage the devices. As a result, if one is looking for operation at very high switching speed, improvement and optimization at component level is also required. Chapter III will present the design and the implementation of the high side power supply from the low side supply made available from a regular power supply. Then the works on the signal transfer units will be briefly addressed at the end of the Chapter III.

### II.5 Expectations on the gate driver architectures for the power devices in series connection configuration

#### II.5.a High voltage and high speed system with WBG devices in series

According to the advantages of the proposed gate driver architecture for a low side – high side configuration, the gate driver of the switching cells in series connection is investigated. The simulation results and the experimental validations are used to confirm the analysis.

Multilevel and series associations are expected to be applied in some critical applications when regular component ratings are not covering all specifications.

The implementation of GaN or SiC power devices in series connection is a solution for the power electronics conversion system [7, 17]. In a similar manner as previously carried out at the inverter leg level, work on the gate driver circuit can be carried out to improve the behavior of series connected power devices. We are going to investigate this based on a single inverter leg with each power device made out two components associated in series, including their own gate driver circuitry. Based on the previous analysis, several configurations can be considered are possible improvements for the management of conducted common mode currents from the gate driver circuitries. We are going to investigate this.

### **II.5.b The architectures of the gate driver (AS1 - AS2 - AS3 - AS4)**

#### ***II.5.b-i The conventional gate driver architecture of the power devices series connection (AS1)***

The conventional gate driver architecture considered for the study is named AS1 and is depicted in Fig.II.2. Identical power supplies and control signal isolators are used for each power device. In this architecture, it clearly appears that the noisy currents generated at each gate driver stage will all flow through the grounds of the system. The important question is not here to know if this will be worse than with single devices but it will be to know if we can apply and transpose our guidance to any power converter architecture with comparable benefits. In other words, the particular approach developed in the previous section can be generalized or not? If yes, which guidance can be generalized?

#### ***II.5.b-ii The proposed solutions of the gate driver architecture (AS2 – AS3 – AS4)***

To overcome the conducted EMI perturbations on the driver circuits of the conventional architecture, several architecture configurations can be considered. Among them, we propose three gate driver architectures for the power devices in series connection are investigated which seem to represent the most logical and the best options to be analyzed.

Changing the EMI current paths can limit the perturbations from the power parts to the remote control circuit. The advantages of the conducted EMI management and the complexity of the power supplies of the gate driver circuit are studied.

#### **Proposed architecture with pairs of low side and high side power supplies (AS2)**

This proposed architecture implements pairs of low side – high side power supplies, as it can be seen on Fig.II.36. This first proposed architecture is so-called AS2. The high rating isolation is located only on the low side power supplies. In each pair of the power supplies, most disturbances circulate within the power side, the rest of the currents go to the ground of the remote control circuit which remains still high. For the proposed gate driver architecture, the design of the power supplies must be carefully considered.

In this architecture, the configuration for each power supply is based on a pair of a low side and high side power supplies. The number of the power supply pairs is identical to the number of the power devices in series connection. There are two low side and two high side power supplies for the configuration of two power devices in series connection. The voltage ratings of the supplies between the low side and the high side gate driver correspond to the rating of the power parts, which must be higher than the power DC bus. Current rating for the low side supplies must take into account the high side gate driver to be supplied. In this configuration, cascaded supplies are generic and have comparable isolation ratings.

This first configuration clearly points out that the upper low side gate driver which is directly connected to GND1 will be affected by  $dv/dt(s)$  across the bottom switch. As a result, this architecture will probably reduce the amount of common mode currents but it will still provide a path for them to flow through the grounds.

## II.5 Expectations on the gate driver architectures for the power devices in series connection configuration

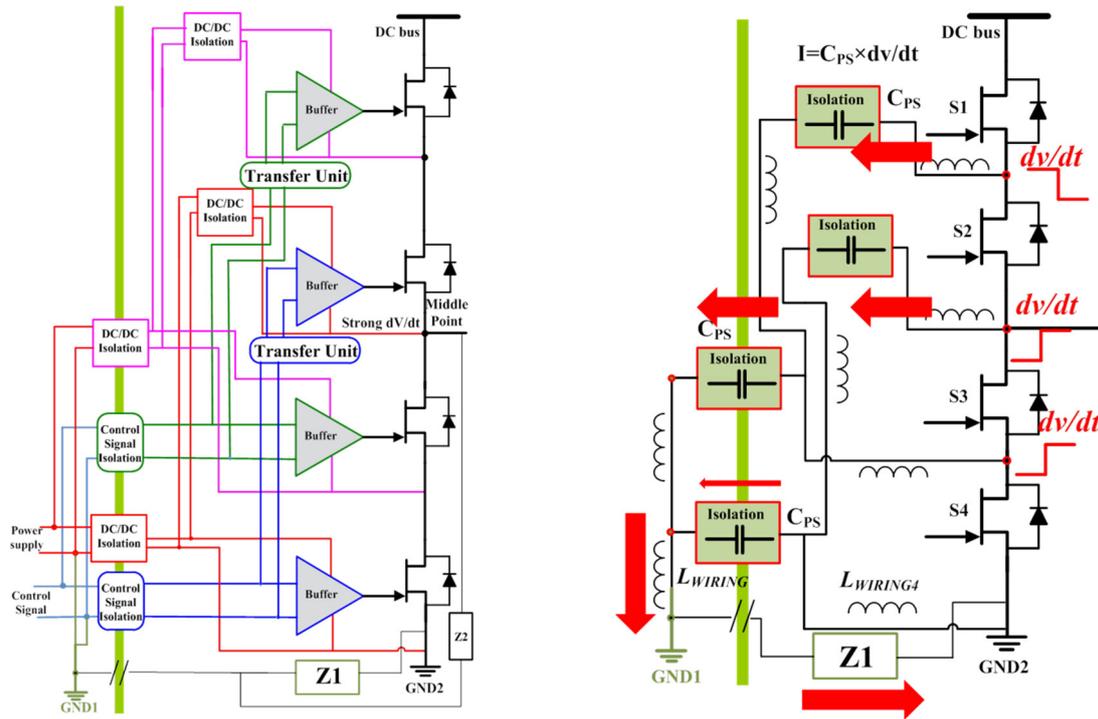


Fig.II.36. Left, first proposed gate driver architecture for series-connection of transistors, named AS2. Right, the conducted EMI perturbations in common mode

### **Proposed architecture with the high side power supplies in parallel (AS3)**

This second proposed architecture is shown in Fig.II.37, and is named AS3. In this configuration, only one supply, the bottom one is connected to GND1, all the other being cascaded from that first one and being all in parallel at their primary side. The high rating isolation locates only on one single low side power supply, and then all the high side power supplies are implemented in a parallel connection. Current rating for the first supply must consider the supply of the four gate drivers. To be generalized, the rating for this gate driver supply should be twice times the amount of power devices in series connections time the nominal rating for a gate driver supply. All other supplies are rated at their nominal gate driver current and must withstand isolation level greater than DC bus ratings.

In this architecture, the disturbances circulate within three high side power supplies. These currents will be divided by two pathways, almost all the current turns back to the ground of the power supply due to the impedance ratio between interconnection and the low side power supply, the rest of these noisy current circulates on the remote control part. From the conducted EMI perturbation point of view, this architecture looks better than AS2 since no gate driver circuitry connected to ground 1 is expected to be excited by large  $dv/dt$ .

For the design of the power supplies, all the high side power supplies are identical without a strong isolation. The isolation barrier now locates only on the low side power supply.

II.5 Expectations on the gate driver architectures for the power devices in series connection configuration

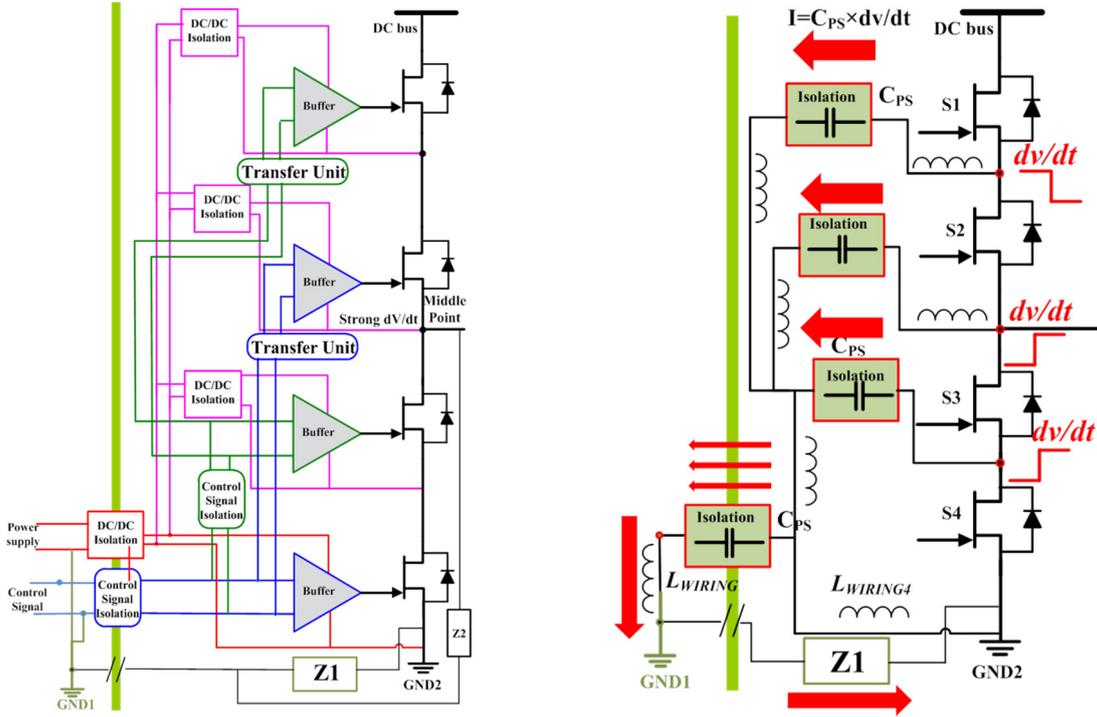


Fig.II.37. Left, second proposed gate driver architecture for a series-connection of transistors named AS3. Right, the conducted EMI perturbations in common mode

**Fully cascaded architecture (AS4)**

This last proposed gate driver architecture (AS4) for the power devices in series connection is introduced in Fig.II.38. The power supplies are fully cascaded, and then the perturbations are returned locally to the power parts once the *dv/dt* events occur through the parasitic capacitance of the power supplies. The final noisy current should be smallest one among the 4 architectures: AS1, AS2, AS3 and AS4.

## II.5 Expectations on the gate driver architectures for the power devices in series connection configuration

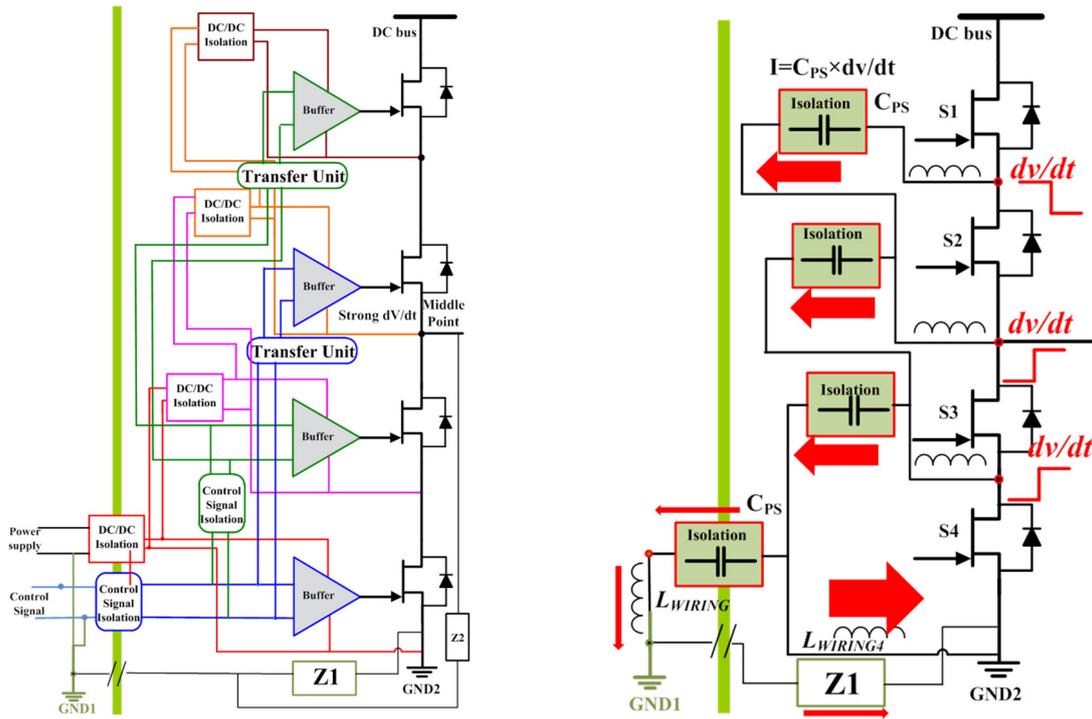


Fig.II.38. Left, conventional gate driver architecture for series-connection of transistors named AS4. Right, the conducted EMI perturbations in common mode

However, the cascaded power supplies must be designed carefully since their current ratings are changing from one to another. In addition, from the isolation voltage rating point of view, if small gain could be expected, in fact, the rating should be once more the one of the power side DC bus. This is especially the case for multilevel converters. The strong isolation barrier is still located on the low side power supply.

Of course, the way the gate driver supplies are cascaded could be investigated in more details. We did not have the time to look into the details of such aspects.

The simulation validations are presented for 4 architectures in the next section. One very important issue here is the way the  $dv/dt(s)$  are applied to each gate driver circuitry. Many aspects could be investigated here. Considering direct series connections of transistors, we could investigate perfect switching synchronization, small and large mismatches. Based on previous analysis [73], we know that all power devices en series connection do not switch at the same time and at the same speed. This could be investigated. In a different way, in multilevel converters, all power devices in the series association do not switch at the same time location within the switching period. This may influence the optimization of the gate driver circuitry. The lack of time, did not give us the opportunity to deeply address and investigate even a few of these possible configuration and most of them are left aside for future work. To complete a first set of analysis, we will consider here only direct series connections of transistors when all high side devices switch at the same time and all low side devices switch at the same time. Switching speed and location will be the same for each group of power devices.

### II.5.c Simulation comparison for 4 architectures (AS1 - AS2 - AS3 - AS4)

As it was made for the simulation parameters set up for the first section of this chapter, the values of the simulations for these power systems are extracted from the elements of the experimental circuits.

Fig.II.39 shows the rising edge of the waveform of the voltage source used in the experiments. The amplitude is 300 V and the rising time is 30 ns which gives a  $dv/dt$  of 10V/ns at the middle point of the inverter leg. The half of this voltage is applied on each transistor in the simulations as 5V/ns. In the experiment, the active gate controlled voltage balancing technique [72] has been used for the series connected power devices in order to make three identical floating points with  $dv/dt$  of 5V/ns.

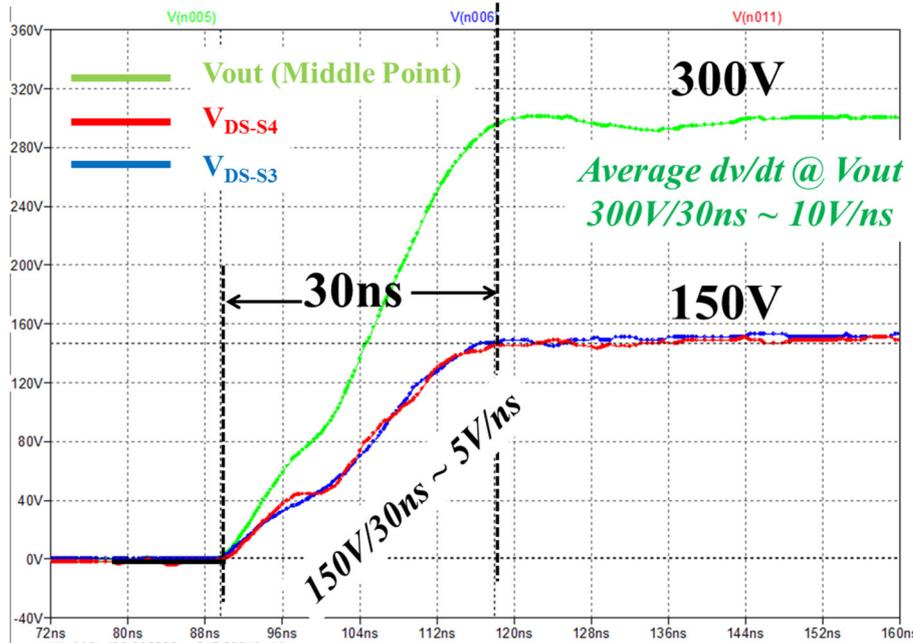


Fig.II.39. Experimental  $dv/dt$  captures across a pair of power devices in the experiment.

With the same method of simplification as it was presented in the first section of this chapter, the high frequency equivalent circuits have been built up for the series connection configuration of the power devices.

Fig.II.40 shows the schematic circuit used in the software SIMPLORER to simulate the transient waveforms of the conventional architecture with 2 power devices in series connection – AS1.

The values of the parasitic elements of the power supplies are identical. As introduced in Fig.II.10, the primary to secondary parasitic capacitances of power supplies  $C_{HS}$  and  $C_{LS}$  are 86 pF; the parasitic inductances  $L_{HS1}$ ,  $L_{HS2}$ ,  $L_{LS1}$  and  $L_{LS2}$  on the primary side and the secondary sides of the power supplies are 27.5 nH.

According to the length distance of the PCB trace of the realized circuits, the parasitic inductances  $L_{WIRING_1}$ ,  $L_{WIRING_2}$ ,  $L_{WIRING_3}$ ,  $L_{WIRING_4}$  are estimated to 30nH. The parasitic of the interconnection from GND1 is estimated to 50nH. The fictive impedance  $Z_M$  has a parasitic inductance of 50 nH and a capacitance of 10 nF connected in parallel with a resistance of 10 M $\Omega$  to measure approximately 95% of the noisy current.

As we can see in Fig.II.40, in the conventional architecture, a noisy current with 6.0 A amplitude is circulating through  $Z_M$  when a small  $dv/dt$  of 10V/ns occurs at the output of the inverter leg.

## II.5 Expectations on the gate driver architectures for the power devices in series connection configuration

Meanwhile a  $dv/dt$  of  $5V/ns$  appears at the highest source in the figure. Two sources at the low side are identical and complementary with the high side source.

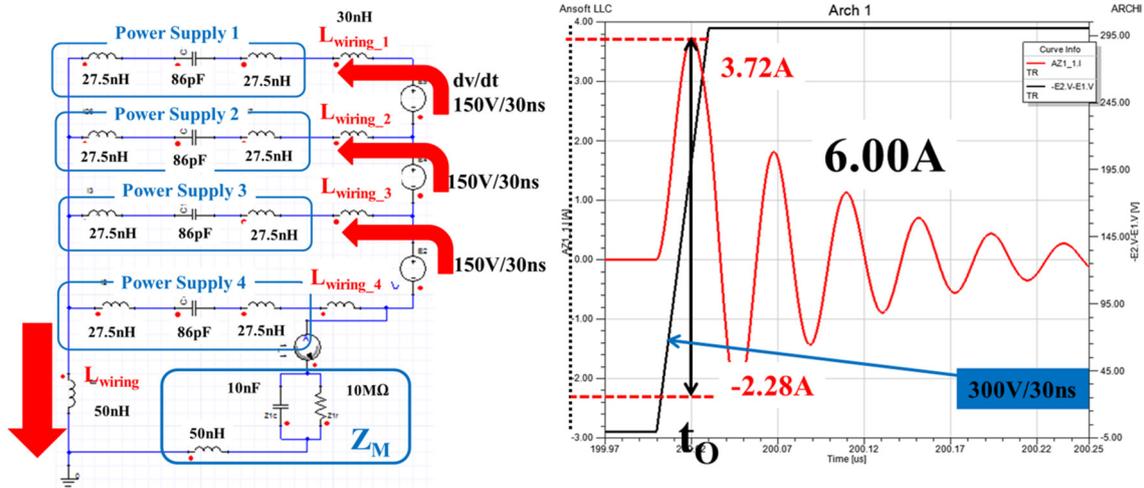


Fig.II.40. Simulation of the conventional architecture AS1: Left, schematic circuit. Right, simulation results

The simulation schematic of the first proposed architecture - AS2 with two pairs of cascaded gate drivers and the simulation results are figured out in Fig.II.41. A noisy current of 1.81 A circulates to the ground of the remote control part.

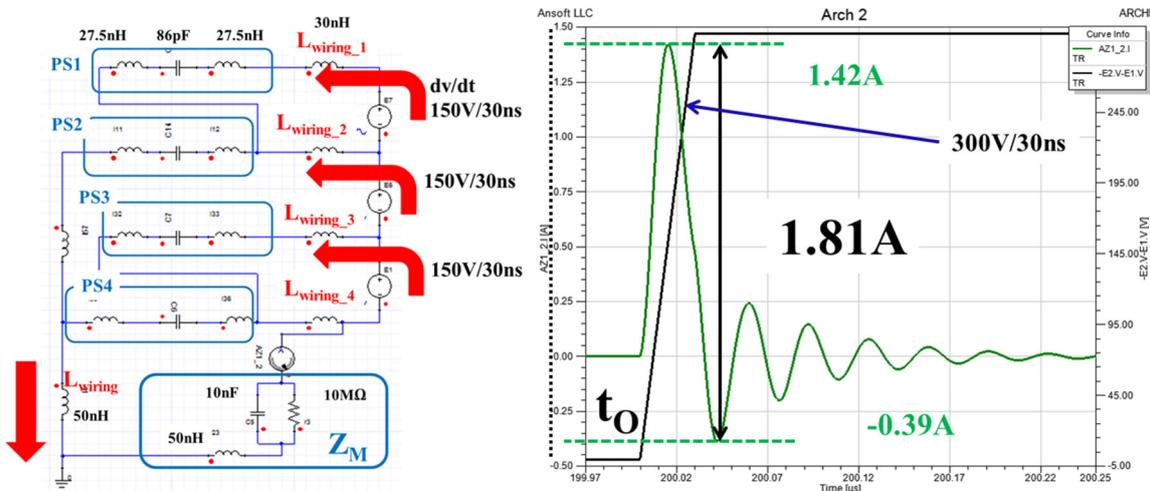


Fig.II.41. Simulation of the proposed architecture AS2: Left, schematic circuit AS2. Right, simulation result

Fig.II.42 shows the simulation schematic of the second proposed architecture – AS3 and the simulation result of the noisy current when a  $dv/dt$  of  $10V/ns$  occurs at the output. The noisy current is significantly decreased to 0.78 A.

## II.5 Expectations on the gate driver architectures for the power devices in series connection configuration

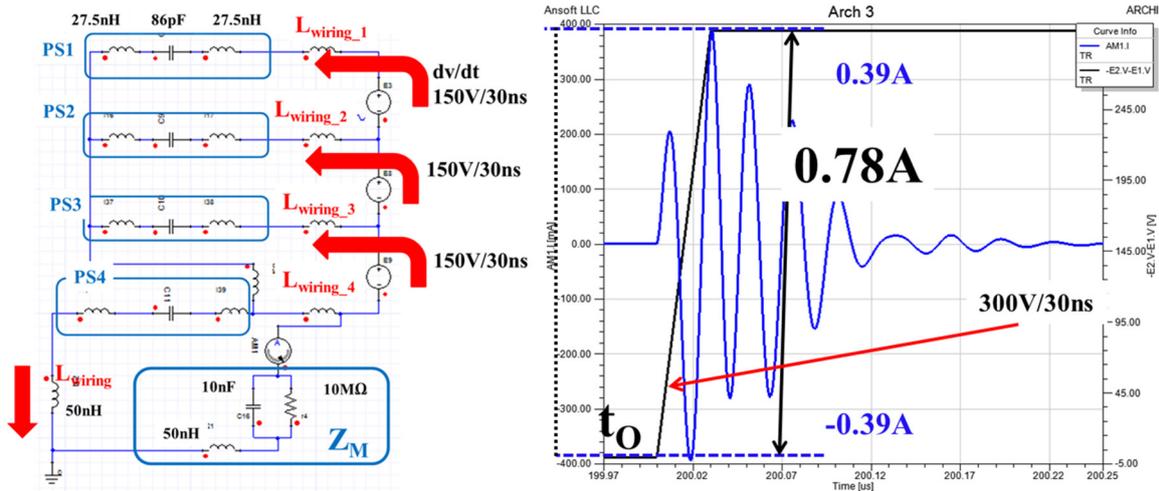


Fig.II.42. Simulation of the proposed architecture AS3: Left, schematic circuit AS3. Right, simulation result

As we can see in Fig.II.43, the best case for the reduction of the conducted EMI perturbations is presented, AS4. The noisy current is ultimately decreased to 0.17 A from 6.0 A for the conventional gate driver architecture.

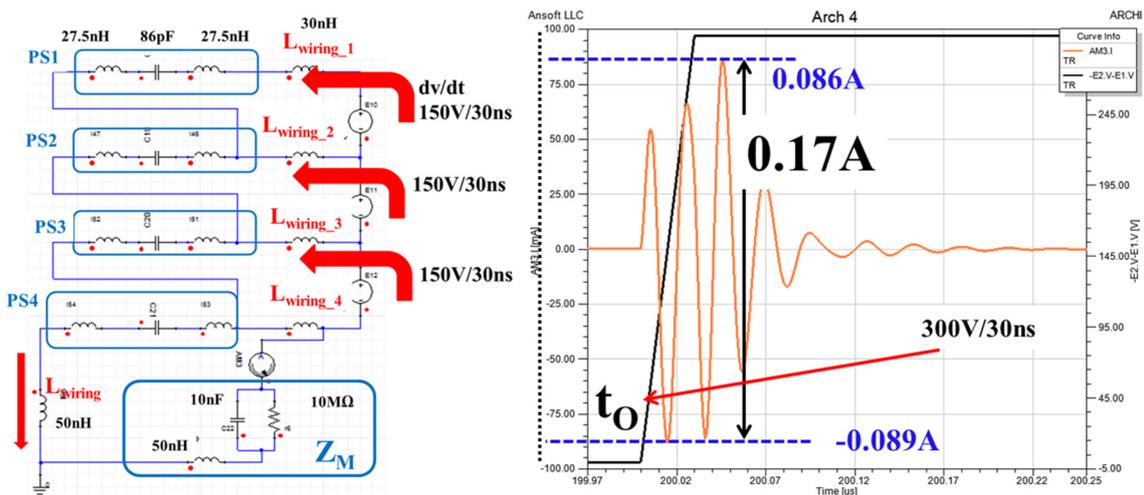


Fig.II.43. Simulation of the proposed architecture AS4: Left, schematic circuit AS4. Right, simulation result

In Fig.II.44, the simulation results of four gate driver architectures have been compared. As it can be observed, the noisy common mode current is significantly decreased from the conventional to the proposed gate driver architectures. In the 4<sup>th</sup> case, the proposed architecture has the smallest noisy current; however, this architecture of the power supplies requires them to be oversized to operate in full cascade configuration.

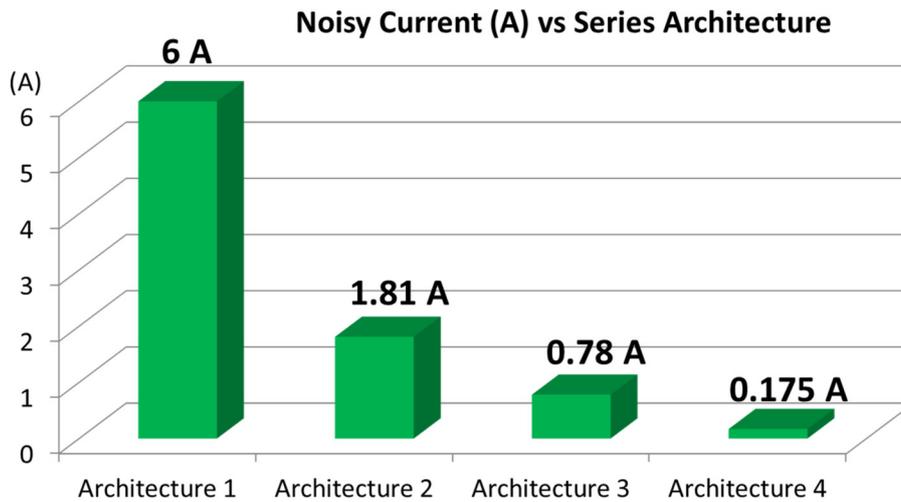


Fig.II.44. Noisy currents peak to peak maximum amplitude for the 4 different gate driver supplies architectures, simulation results

#### II.5.d Experimental results for 2 extreme architectures: AS1 and AS4

Based on the experiments developed in the previous works and on the simulation results analysis, the noisy currents between  $GND1$  and  $GND2$  are measured in the experimental setup for the series connection configurations for two extreme architectures: AS1 and AS4. Classical power MOSFET devices have been used.

To physically separate the  $GND1$  and  $GND2$ , a battery of 300 V has been used as input power for the power side. An auxiliary 15 V power supply is used for powering the driver circuit; a function generator was used to generate the control signal of the remote control part. This 15V power supply and this function generator are powered by the grid. A control signal PWM with 50% duty cycle and 100 kHz frequency is used to drive the power transistors.

Additional artificial impedance  $Z_M$  of 10 nF and 10 M $\Omega$  has been used to emulate the impedance between  $GND1$  and  $GND2$ . The experimental setup is demonstrated in Fig.II.45.

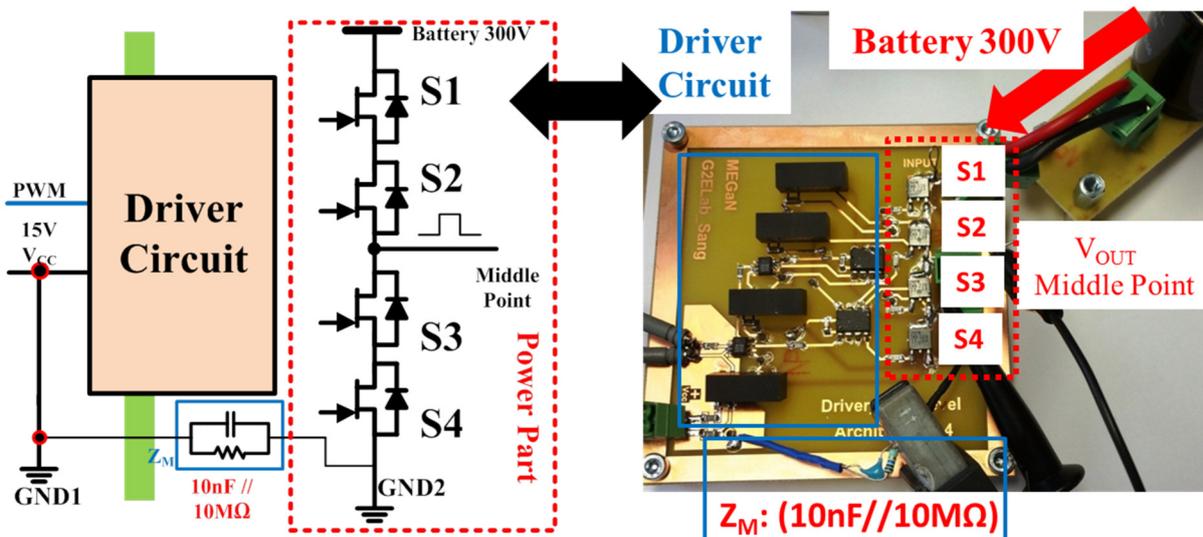


Fig.II.45. Experimental setup with physically separated  $GND1$  and  $GND2$

II.5 Expectations on the gate driver architectures for the power devices in series connection configuration

Fig.II.46 shows the circuit with conventional architecture of the driver circuit. In this circuit, an inverter leg has been implemented with two MOSFETs in series connection. The balancing technique of the voltages of the power devices is implemented as the active gate controlled voltage balancing technique [72]. There are 4 isolated DC-DC power supplies and 4 opto-couplers in this experiment.

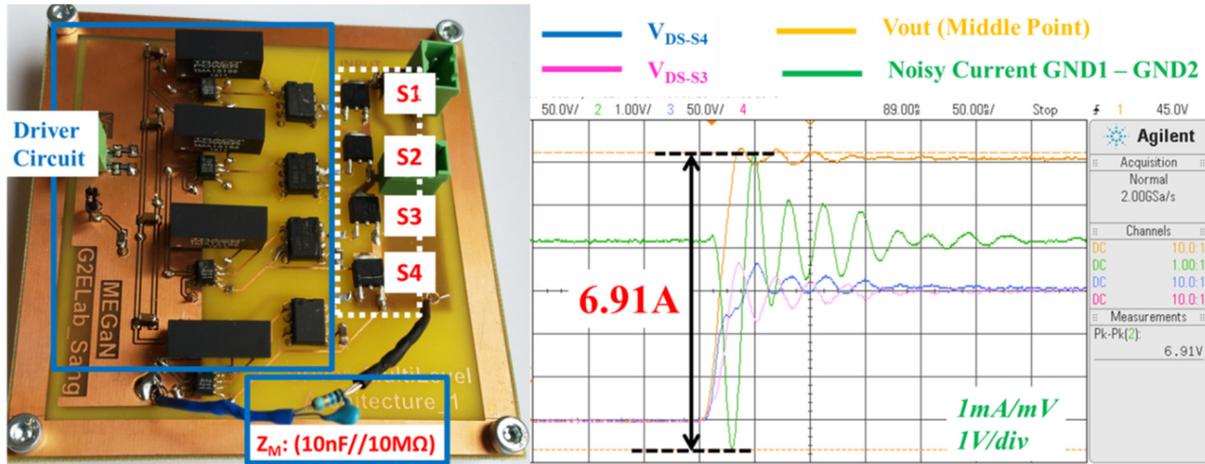


Fig.II.46. Conventional gate driver architecture (AS1) with 2 power devices in series connection: Right, Picture of the PCB circuit. Left, experimental results

The noisy current through the driver circuit in the conventional architecture has been measured. As it can be observed, the  $dv/dt$  of 10 V/ns appears at the middle point of the power inverter leg as  $V_{OUT}$ , which means  $dv/dt$  of 5V/ns on each power device is generated as  $V_{DS-S3}$  and  $V_{DS-S4}$ . A noisy current of 6.91 A peak to peak maximum amplitude is measured. This current circulates to the ground of the remote control circuit and goes back to the power through GND2 through  $Z_M$ .

Fig.II.47 shows a picture of the circuit of the 4<sup>th</sup> proposed architecture AS4 in the left side.

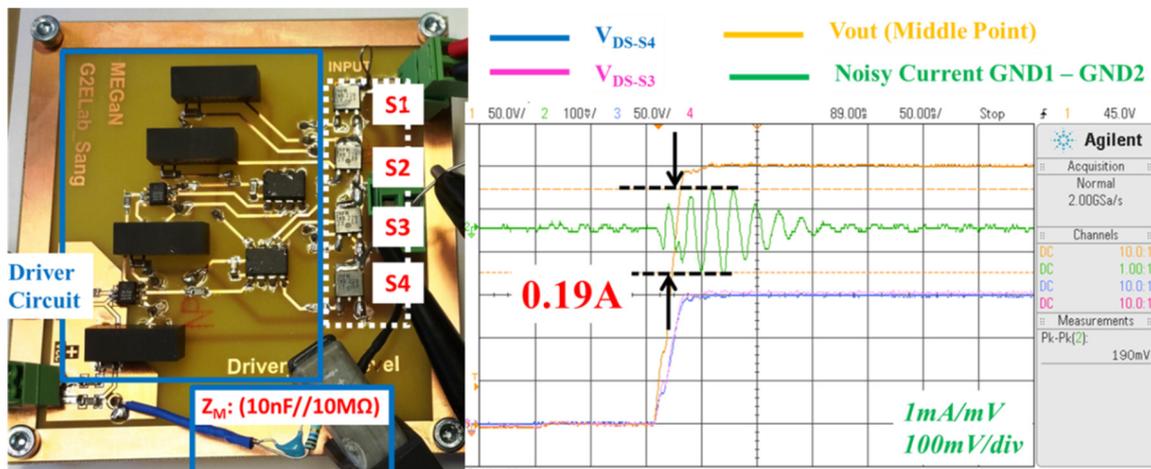


Fig.II.47. Proposed gate driver architecture (AS4 – fourth case): Right, Picture of the PCB circuit. Left, experimental results

Four isolated power supplies, two optocouplers and two gate drivers with integrated level shifter have been implemented to control the 4 power devices of the inverter leg. The power supplies are cascaded from the bottom device up to the upper one.

## II.5 Expectations on the gate driver architectures for the power devices in series connection configuration

On the right side of Fig.II.47, the measured noisy current is reduced from 6.91A to 0.19A peak to peak maximum amplitude. The voltage at the output of the inverter leg  $V_{OUT}$  and the voltage across the drain-source of the power devices ( $V_{DS-S3}$  and  $V_{DS-S4}$ ) are less bouncing than in the conventional architecture thanks to a non-polluted system.

In this experiment of AS4, the power supplies have been carefully selected to make sure the expected output voltages of the 4 stages corresponds to the specifications and are very close to those in the conventional architecture.

### II.5.e Comparison the switching speeds of the power devices in AS1 and AS4.

In order to compare the switching speed of the power devices in AS1 and AS4, we did a second experiment. In this experiment, all the gate resistors are reduce to zero for maximizing the switching speed of power devices. As we can see, Fig.II.48 shows the voltage waveform on the output voltage at the middle point of the inverter leg and also the noisy current between GND1 and GND2. In this experiment, the rising voltages are focused on for comparing the switching speeds.

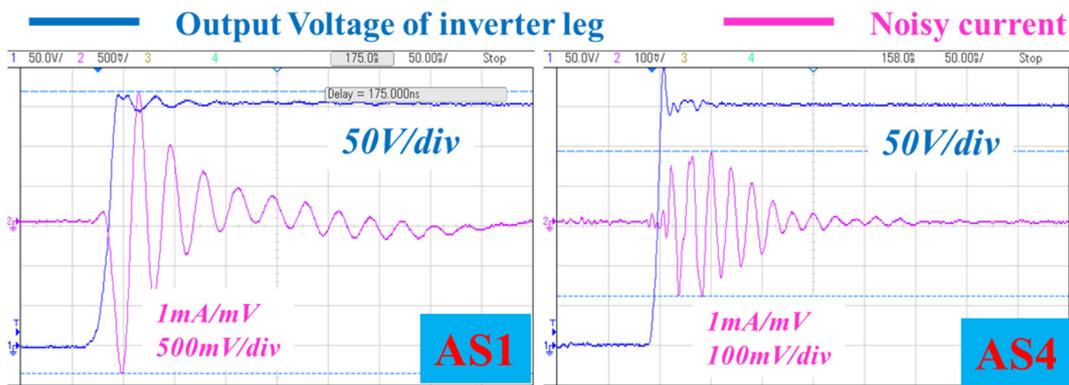


Fig.II.48 Rising voltages of AS1 and AS4 without the gate resistors of transistors

By calculating the speed of each data points of the experimental results, the switching speeds of power devices are depicted in Fig.II.49. The vertical axis is the speed  $dv/dt$  and the horizon axis corresponds to the data point. As we can see the maximum  $dv/dt$  of AS4 is much higher than  $dv/dt$  of SA1, 42.9 V/ns and 26.8 V/ns. Moreover, the inclination of the slope of AS1 is higher than the inclination of AS4 which means the rising time of AS4 is shorter than AS1.

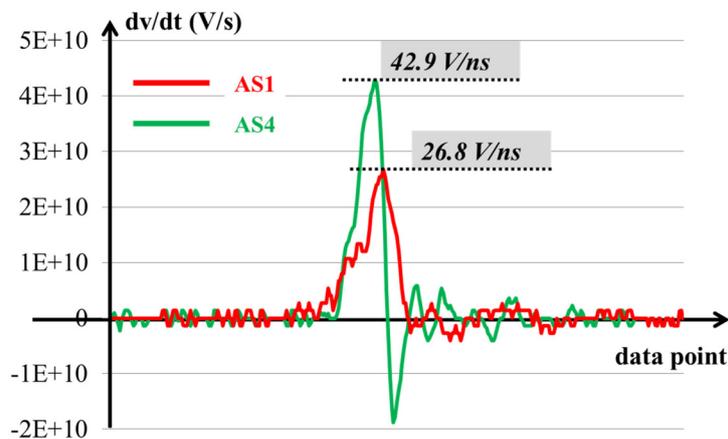


Fig.II.49 Switching speeds of AS1 and AS4, the  $dv/dt$

To explain this phenomenon, two simplified circuits of AS1 and AS4 are shown in Fig.II.50

In AS1 and AS4, two parasitic capacitances  $C_{S3}$ ,  $C_{S4}$  are illustrated, existing between the two power devices S3, S4 and the ground of the driver circuit. Due to the connection of the power supply of the gate driver, two parasitic capacitances of AS1 are in parallel meanwhile the capacitances of SA4 are in series. During switching transient, the voltage  $V_{DS}$  of each device changes rapidly, thus there are currents passing through these capacitances. The total capacitance of AS1 is equal to two capacitors in parallel,  $2C$ . In another side, the total capacitance of two capacitors in series is  $C/2$ . The difference of these parasitic capacitances between the output of the inverter leg and the ground of the gate driver explains the gain of the switching speed.

To obtain the advantage of the EMI issues and the gain of the switching speed of the power devices, more efforts must be engaged.

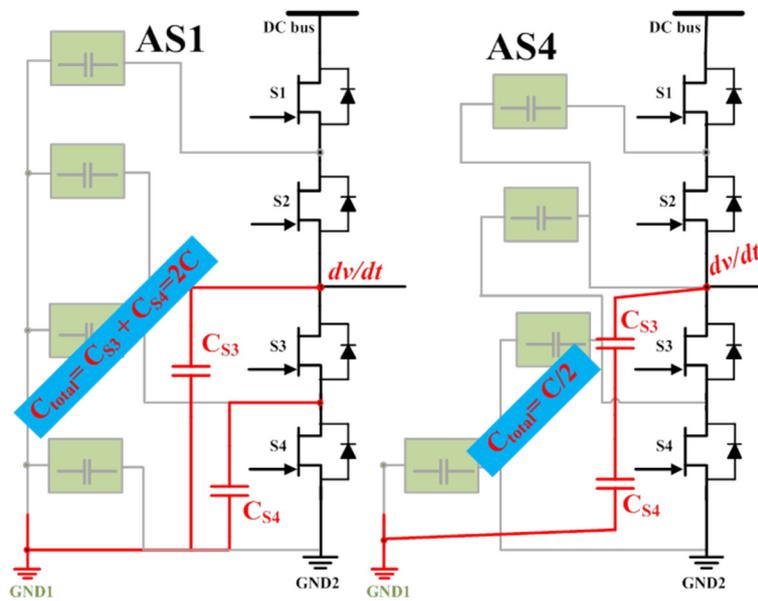


Fig.II.50 Parasitic capacitances in power circuit of 2 architectures: AS1 and AS4

To summarize the investigation carried out in this second section, it appears that the proposed gate driver circuitry architecture, based on cascaded driver supplies and signal isolation can be generalized to complex switching cells and converters. It appears that significant common mode current reduction can be reached based on the guidance proposed in the first section of this chapter. Nevertheless, we did not have the time to investigate deeply all the aspects involved in such more complex converters such as multilevel or even modular multi-level converters. A lot of work is still required to analyze precisely the advantage and the drawbacks of the cases of such applications since we have identified for example that the multi transistors cascaded configuration requires to oversize the gate driver power supply ratings with respect to the number of gate driver to supply. For high level converters, this may become a significant counterpart for problems of oversize but also additional losses due to cascaded supplies. On the other side, and this has also been left for future works, significant isolation level reduction for the gate driver supplies and signal isolators may be possible. To conclude on this section, the approach seems to offer interesting behavior and should be further investigated on specific cases.

### **II.6 Conclusions and perspectives**

In this chapter, a proposed architecture of gate driver circuitry for HF, very high switching speed power devices is presented in order to optimize the EMI propagation pathways from the power module and especially through the control units of a low side – high side switching cells configuration.

The experimental results proved its advantages regarding to the optimization of the EMI disturbances under very high  $dv/dt$ . The analysis of the work highlighted that cascaded supply architectures as well as the integration of part of the gate drivers' circuitry as close as possible to the power transistors are required to achieve effective high switching speed power module implementations for WBG power devices.

This chapter also confirms that the approach can be applied to the conducted EMI optimization on the gate driver architecture of the power devices in series connection configuration. The simulation results and the experimental results validate the interest of the cascaded gate driver supply architecture. There are the compromise between the redesign of the power supplies and the conducted EMI perturbation. Depending on the specifications of the application, a suitable gate driver architecture could be selected.

Further works need to be engaged on the configuration of the gate driver circuitries for power devices in series connection and the modular multilevel converter to clearly state on the advantage and drawbacks of the approach.

The next chapters will tackle the recommendations of the works in this chapter. In Chapter III, the high side gate driver power supply will be analyzed and characterized with the objective to reduce as much as possible the parasitics responsible for large common mode currents. And then a similar effort will be presented for the signal transfer units, based on the comparison of several technics developed within the research team.

**Chapter III**

**Redesign The Elements**

**Of Gate Driver Circuitry:**

**High Temperature ASICs For High  $dv/dt$**

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## Abstract

*In the previous works, the problems at system level are studied, Chapter II has been presented an innovative gate driver architecture with the conducted EMI optimization for high speed power devices with high  $dv/dt$  in a low side – high side switching cells configuration. In addition, the recommendations for the design of the gate driver introduced in Chapter II as well as in the research orientation in Chapter I, point out the EMI problems to be solved also at the component level for an improved EMI system.*

*In this chapter, the need for designing a specific isolated high side power supply for the gate driver circuits is firstly recalled. A review of the supplied techniques is considered: comparisons of the converter topologies are presented in order to select the most suitable candidate.*

*Secondly, the efforts to invest on the isolated control signal transfer unit evolutions are studied. In particular, the conducted EMI immunity is an important issue when strong  $dv/dt$  occurs. Three techniques of the gate driver circuit for the control signal transfer unit are presented: signal transfer unit with coreless transformer, with current source level-shifter and with optical transmission.*

*To overcome the temperature issue for both the isolated high side power supply and the isolated control signal unit, the designs of ASICs (Application-Specific Integrated Circuit) are carried out with the XFAB XT018 PDK, this integrated technology being well suited to operate at high temperatures.*

### III.1 Introduction of the high side power supply of the gate driver

#### III.1.a Solutions for the high side power supply of the gate driver

According to the conclusion of Chapter I, a new adaptive gate driver circuit is required. Chapter II proposed specific gate driver architecture to solve the problems at the system level; works are needed to deal with these problems also at the component level. This work describes a contribution in designing small isolated floating powers supply, providing a sufficient power, with a high CMTI and suitable for high temperature environment. There are several techniques to supply the high side switching cell. Advantages and drawbacks over alternative methods are presented to choose the suitable technique under these conditions.

In the medium-voltage power electronics systems, robust galvanic isolations are required in order to drive high-voltage switching devices. In the gate driver supplies of a low side – high side implementation, we report six techniques that have been implemented and mentioned in many literatures [74] [75] [76]:

- The widespread power supply technique that offers the most flexibility is that of DC-DC isolated converter such as flyback converters [77] [78] [79] in Fig.III.1. The output power is about 1W and the input power supply voltage level ranges from 3V to 24V.

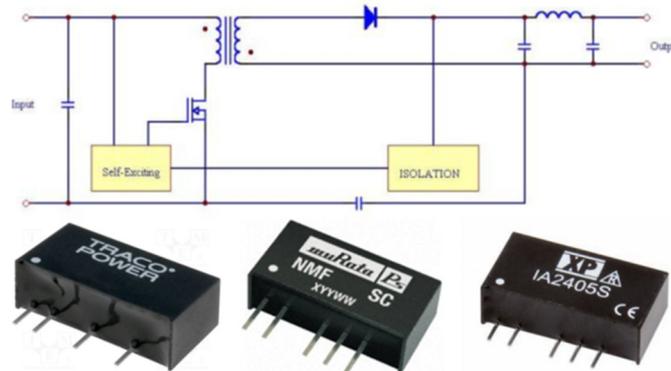


Fig.III.1 Commercial power supplies based on the flyback topology [77] [78] [79]

The main disadvantages of this technique are the volume, the generated EMI and the difficulty to be integrated monolithically due to an imposing transformer.

- The second widespread technique is the bootstrap supply [80] [81]. This simple technique consists of only a high-voltage diode between the power supply of the low-side control circuit and a bootstrap capacitor -  $C_{BS}$ , see Fig.III.2. The galvanic insulation is not provided in this technique. When low side transistor is closed, the middle point is virtually grounded and the bootstrap capacitor is charged to the voltage of the low-side power supply. This feeding technique is not compatible with a static operation, or a too low switching frequency.

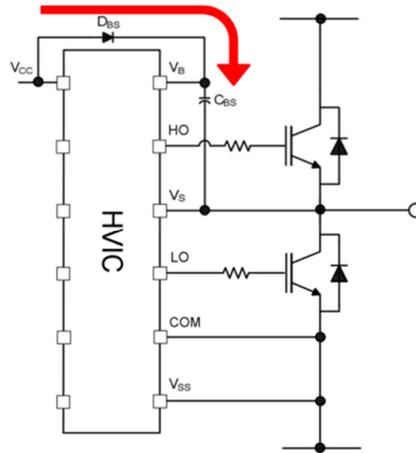


Fig.III.2 Bootstrap supply in IRS2330 gate driver[80] [81]

- The self-powering technique presented in [59] can be compared in its operation as a pulsed linear regulator connected between the source of the high side power transistor and its drain. When the high side transistor opens, the voltage source across the drain and the source is used to charge  $C_s$  [59] to a low voltage, typically less than ten volts as we can see in Fig.III.3. Then the energy of capacitor  $C_s$  serves as a floating supply. This solution allows a static OFF state of the two transistors where the bootstrap technique is not accurate. However, the permanent ON state operation is forbidden. The self-powering circuit is directly connected to the power supply and the source of the high-side transistor. There is no physical link with the low side circuit or the logic circuit; the galvanic isolation is naturally presented and this technique is suitable for high CMTI.

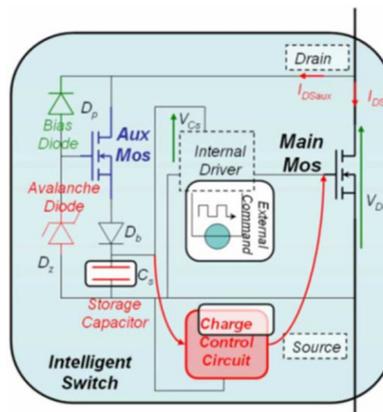


Fig.III.3 Self-powering circuit for high side transistor [59]

- The radio frequency power wave [82] is to recover the energy of a radio frequency coupler. The energy recovered by this technique is very low with a limited efficiency but it is already used to control a small GaN HEMT between 2V and -1V. To isolate the primary side and secondary side of the driver circuit, this technique is using an Electro Magnetic Resonance Coupler (EMRC) with a butterfly shape. The radio module is easily integrated to the driver circuitry. Fig.III.4 shows a specific application for this technique for power supply solution.

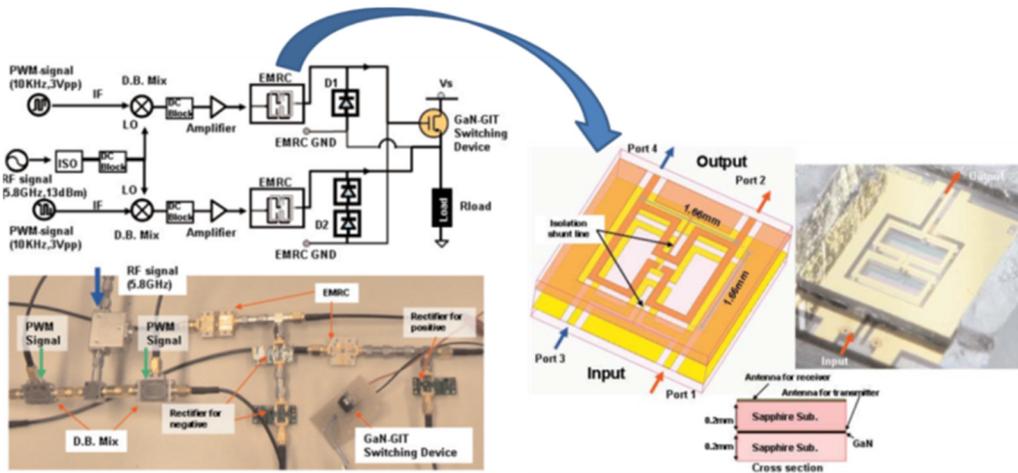


Fig.III.4 Direct gate driver supply using Electro Magnetic Resonance Coupler [82]

- The fifth technique is a piezoelectric transformer based DC/DC converter [83], [84], [85].

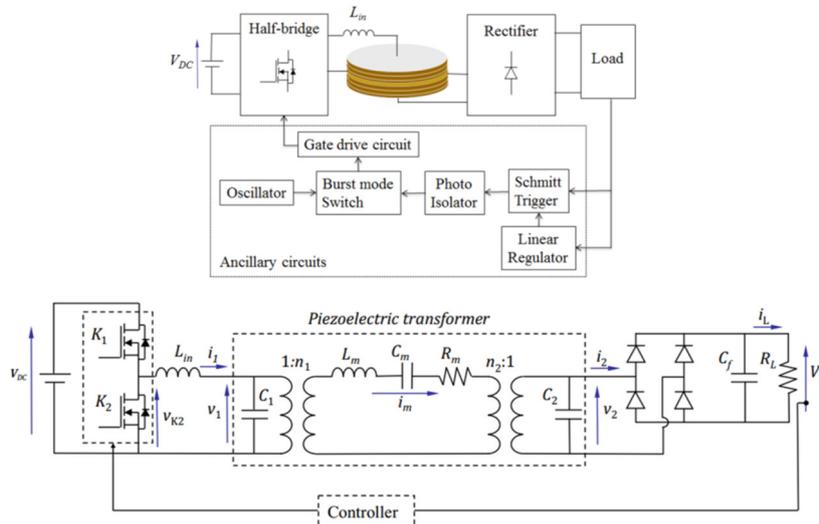


Fig.III.5 System block diagram and circuit topology of piezoelectric transformer based DC/DC converter with burst-mode control [83]

A piezoelectric transformer exchanges electric potential with mechanical force. In reality, the piezoelectric transformer cannot stop instantly to vibrate. By using a piezoelectric transformer, the DC/DC converter can be implemented with a resonant-mode operation [85] or a burst-mode control is adopted [83] to achieve a high efficiency at light load condition, see Fig.III.5. Working on the primary-secondary parasitic capacitance of piezoelectric transformer can improve the CMTI; however to perform the piezoelectric transformer at high temperature is a big issue due to the mechanical system.

- The sixth technique is using the optical source to supply the driver circuit of the high side transistor. Recently, the power electronics group of G2Elab proposed an optical sensor working in Photo-Voltaic Mode which can locally generate power for the gate driver; the schematic of the optical supply chain is shown in Fig.III.6 [86]. The prototype has also proved that this technique is suitable for high temperature environment. This approach then proposes to associate one or more optical detectors connected to an integrated DC-DC converter, to generate the power of all the functions of the gate driver. However, it presents some disadvantages: low efficiency and complex implementation.

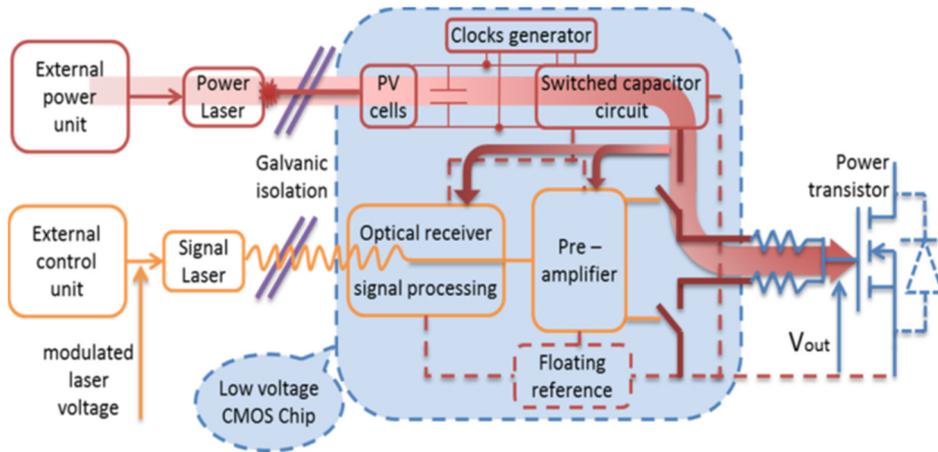


Fig.III.6 Optical supply chain [86]

These six techniques are synthesized in the Table.III.1 for their advantages and drawbacks.

Table.III.1. Supplied techniques of the high side switching cell

Type of Supply	Advantages	Drawbacks
DC-DC isolated converter (flyback converter by Traco, Murata or XP power) [77] [78] [79]	<ul style="list-style-type: none"> <li>- High functional voltage (~kV)</li> <li>- Flexible output voltage (3-24V)</li> <li>- Strong galvanic isolation (~kV)</li> <li>- High efficiency</li> <li>- High output power (~W)</li> <li>- active parts easy to integrate</li> <li>- Can be optimized for CMTI</li> </ul>	<ul style="list-style-type: none"> <li>- Magnetic core : difficult to integrate at high operating temperature</li> <li>- EMI issues (even more with coreless transformers)</li> </ul>
Bootstrap [80] [81]	<ul style="list-style-type: none"> <li>- High functional voltage (~1.2 kV)</li> <li>- Flexible output voltage (10-20V)</li> <li>- High efficiency</li> <li>- Hybrid integration</li> </ul>	<ul style="list-style-type: none"> <li>- No galvanic isolation</li> <li>- Low output power</li> <li>- Depends on the duty cycle of the power devices</li> <li>- Impossible OFF static state of 2 transistors</li> <li>- Operating temperature limited by max temp of bootstrap diode</li> <li>Driver voltage with ripple</li> </ul>
Self-powered supply [59]	<ul style="list-style-type: none"> <li>- Galvanic isolation (no link to control parts)</li> <li>- High integration level except for the capacitor</li> <li>- High temperature (if implemented with WBG devices)</li> <li>- highly suitable for CMTI</li> </ul>	<ul style="list-style-type: none"> <li>- Low output power</li> <li>- Low efficiency</li> <li>- Permanent ON state operation is forbidden</li> <li>Driver voltage with ripple</li> </ul>
Coupling radiofrequency [82]	<ul style="list-style-type: none"> <li>- Strong galvanic isolation (~5kV)</li> <li>- High possibility of integration</li> <li>- Can be optimized for CMTI</li> </ul>	<ul style="list-style-type: none"> <li>- Low functional voltage (~200V)</li> <li>- Inflexible output voltage (+2V/-1V)</li> <li>- Low output power</li> <li>- Low efficiency</li> <li>Large size</li> </ul>

Piezoelectric Transformer based DC-DC converter [83], [84], [85]	<ul style="list-style-type: none"> <li>- Galvanic isolation</li> <li>- Can be optimized for CMTI</li> <li>- High efficiency</li> </ul>	<ul style="list-style-type: none"> <li>- Difficult to integrate the piezoelectric transformer</li> <li>- Difficult to work at high temperature</li> <li>- Operating-mode is complex</li> </ul>
Optical supply chain [86]	<ul style="list-style-type: none"> <li>- High functional voltage (~kV)</li> <li>- Strong galvanic isolation (~limitless)</li> <li>- High possibility of integration</li> <li>- Suitable for CMTI (~limitless)</li> </ul>	<ul style="list-style-type: none"> <li>- Complex implementation</li> <li>- Very low efficiency</li> </ul>

The next sections present the requirements of the isolated high side power supply for driving WBG power devices.

Based on the specifications of the power supply and according to the advantages and drawbacks of the six supplied techniques, the selection of the most suitable technique is shown in the next section.

#### III.1.b Specifications of the isolated high side power supply of the gate driver

The specifications of the power supply are directly induced by the specifications of the HEMT transistors and its operating conditions (frequency, current, voltage, etc). Beside these specifications, the EMI problem and the high temperature issue are considered for the design of the isolated high side power supply.

Based on the datasheet, the key values of the GaN power devices in the MEGaN project can be extracted. The gate-source voltage is from -9 V to 9V. The typical drain-source voltage is 600V with the nominal current of 30A. In addition, the junction temperature of this GaN device is up to 250°C [Confidential documents of MEGaN project].

According to the specifications of the power devices, the voltage levels of the isolated power supply are decided to be 9V for the input and 9V for the output. The galvanic isolation voltage is set at 1kV for 600V power devices. To design the power supply, we need to calculate the average power needed to drive the power devices themselves but also the consumption of the associated parts of the gate driver circuit.

The gate charging consumption can be calculated by the specifications of the power device and its operating conditions. We have:

$$P_{MEGaN} = Q_g \times V_{GS-nominal} \times f_{switching} \quad (III.1)$$

Where,

- $P_{MEGaN}$ : the gate charging consumption of the GaN device in MEGaN project
- $Q_g$ : the total gate charge of the power device, is equal to 45 nC
- $V_{GS-nominal}$ : the nominal gate-source voltage of the power device, is considered to be 5 V
- $f_{switching}$ : the switching frequency of the power device, assigned to 1 MHz

The gate charging power consumption is:

$$P_{MEGaN} = 45 \text{ nC} \times 5 \text{ V} \times 1 \text{ MHz} = 0.225 \text{ W} \quad (III.2)$$

### III.1 Introduction of the high side power supply of the gate driver

The power consumption of the gate driver buffer is estimated according to commercial gate drivers which are widely used to drive GaN devices such as LM5113 and EL7158 [87], [88]. Following up the parameter in their datasheets, the maximum operating current is up to 3 mA for a driving voltage of 6V. The consumption of the gate driver can be estimated by the following equation:

$$P_{Driver} = 3 \text{ mA} \times 6 \text{ V} = 0.018 \text{ W} \quad (\text{III.3})$$

Hence, the total power that must be supplied by the isolated high side power supply is:

$$P_{HS-PS-Consumption} = P_{MEGaN} + P_{Driver} = 0.225 \text{ W} + 0.018 \text{ W} = 0.243 \text{ W} \quad (\text{III.4})$$

In order to compensate the losses in the system and guaranty the sufficient energy for the gate driver circuit, the isolated high side power supply is 2 times over-designed. Then the average power of the power supply is estimated to 500 mW.

Table.II.2 describes the specifications of the high side power supply of the gate driver circuit.

*Table.III.2. Specifications of the isolated high side power supply*

Parameters	Value	Notes
Input Voltage	9 V	Magnetic part: difficult integration for a high power and high temperature challenge
Output Voltage	9 V	
Power consumption	500 mW	With 2 times overdesign
Galvanic Isolation	1 kV	For 600V power device
CMTI	50 V/ns	Perspective of 100V/ns
Temperature	200°C	Efforts of works on the magnetic part
Other requirements	<ul style="list-style-type: none"> <li>• Open-loop design. The control signals for the active elements are generated by the logic block of ASIC</li> <li>• Output voltage stable versus driver consumption</li> <li>• Suitable for an integrated solution (with the external isolation part)</li> </ul>	

The transient immunity purpose is pushed to 50 V/ns at this moment, expecting 100 V/ns. Moreover, the temperature issue is strictly taken into account in order to bring the driver circuit close to the power device for the EMI optimization goal.

#### III.1.c DC-DC isolated converter as the most suitable technique

According to the comparison of the power supply techniques in Table.III.1, we can see that self-powered circuit is not suitable for this level of power supply because it would induce to much extra losses, for the same reasons, the RF and optical solutions are left aside. The piezoelectric transformer based converter is complex to implement due to the mechanical system and is not suitable for an integrated solution in the high operating temperature. The bootstrap technique, with a regular silicon diode, is not compatible with the thermal constraints. It could be implemented if we can use a WBG component but this has not been considered in this work although. The architecture of the bootstrap technique meets most of the constraints developed in the two first chapters.

According to the comparisons of the latest techniques and based on the specifications of the high side power supply, the DC-DC isolated converter seems to remain the most suitable technique for the power supply of the MEGaN gate driver.

In the next sections, the suitable DC-DC isolated converter topologies are compared to select the best candidate.

### III.2 DC-DC isolated converter topologies for the high side power supply

#### III.2.a Criteria for the topology's selection

Since the introduction of switch mode power supplies, many literatures have been published relating to studies of various topologies for specific applications [89] [90] [91] [92].

To select a topology to design the isolated high side power supply, several criteria need to be considered for effective comparison of the topologies:

➤ ***Conducted EMI***

One of the most important criteria is the consideration on the EMI; the power supply being entirely inside an optimized system. More specifically, we are not speaking about the EMI generated by the converter itself but by the EMI that may go through the supply, EMI generated by the power parts for example. In the context of the research, we have seen that high  $dv/dt$  applied at the middle point of the inverter leg generates noisy current through the power supply and it is important to minimize this propagation path acting directly on the parasitic of the gate driver power supply.

➤ ***Low power level***

In the previous section, the power level in the range of 500 mW has been figured out. Obviously, the topology should be optimized for low power levels.

➤ ***High efficiency***

This isolated high side power supply will be a part of the integrated gate driver circuit, for an optimized system, the efficiency of the power supply must be as high as possible.

➤ ***Galvanic isolation***

In the context of a low side – high side switching cell implementation, the nominal voltage of the power device is 600V. To guaranty the galvanic isolation between the low side and the high side of the driver circuit, an isolation of 1 kV is assigned as the galvanic isolation level.

➤ ***High switching frequency***

The power supply must also be integrated into the ASIC. Increasing the switching frequency is important for the optimization of the size of the passive components. Eventually, small size is an advantage when the gate driver circuit is brought close to the power devices for the improvements on EMI issues.

➤ ***Simplicity***

In order to make the system work, each element must be reliable, and then a complex system with complex control algorithms is not a smart choice. In this research, the DC-DC isolated converters will be presented; the selected topology will be as simple as possible.

If possible, close loop control will be avoided to limit communications wires and additional propagation paths between the primary and the secondary sides of the power supply.

➤ ***To be easily integrated***

The integration of each topology will be considered, based on either monolithic or hybrid solutions. The integration of the passive components might be a big challenge for this high temperature power supply.

### ➤ *Stable output characteristics*

The control of the power supply being fully independent and autonomous, directly integrated in the ASIC, the dispersion in the manufacturing process can lead to dispersion in the switching frequency generated by the logical block. The design of the power supply must ensure this dispersion does not ruin out the system. The stable output characteristics versus the load and the frequency are important. This is especially the case if we consider as an option to operate the converter in open loop mode, considering that the input voltage is stable and regulated.

In the next sections, the isolated DC-DC converter topologies will be compared and the design of the elements of the circuit will be detailed.

### III.2.b A brief comparison of the isolated topologies

#### III.2.b-i Isolated flyback converter

Among the conventional isolated DC-DC converter topologies, the flyback converter may be the most commonly used for power supplies up to 150W. Its basic topology is reminded in Fig.III.7 [93], [94]. This topology is generally a low cost solution, simple to implement and well suited for the low power applications.

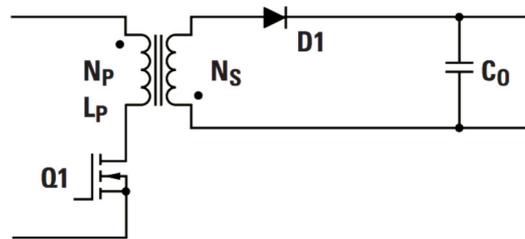


Fig.III.7 Conventional flyback converter topology [93]

The voltage gain of the flyback converter in continuous conduction mode can be calculated as:

$$\frac{V_{OUT}}{V_{IN}} = \frac{N_S}{N_P} \times \frac{D}{1 - D} \quad (III.5)$$

Where,

- $N_P$  and  $N_S$ : the primary and secondary winding turns of the transformer (considering that the leakage inductance value is neglected)
- $D$ : Duty cycle of the PWM control signal

The conventional flyback topology requires only a single active switch and an additional inductor with two windings for the periodic energy storage. The utilization of a transformer for both the isolation and the energy storage makes the topology easy to use and simple to be implemented.

The main disadvantage of the flyback topology is clearly the size of the transformer. And, due to the high input and output ripple current, extra capacitors are required [95]. The most critical issue remains the rating of the power devices the transistor and the output diode. These devices must be rated at twice the operating voltage which it not compatible with a monolithic integration with the considered technology where only 10V devices are available. Even the series connection of component is possible

in this technology, then, the implementation becomes more complex and this topology loses its advantages.

Considering the coupled inductors, huge magnetizing inductance values are required to operate the converter leading to larger windings and larger parasitic capacitive values between the windings. Large leakage inductance and primary to secondary capacitance have a significant impact on propagated EMI and self-generated EMI although this last issue is not considered in this work.

The Half-Bridge and Full-Bridge topologies are investigated for these reasons.

#### III.2.b-ii Half Bridge and Full Bridge converters

The conventional half-bridge and full- bridge converters with or without double ended rectification stage are depicted in Fig.III.8. These topologies are normally used for power applications up to 500W [95].

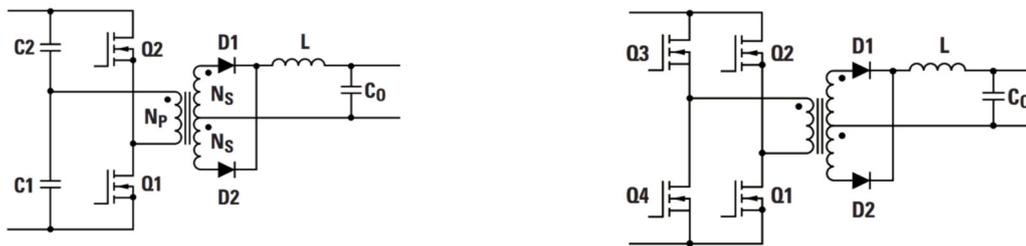


Fig.III.8 Left, Half-Bridge converter. Right, Full-Bridge converter [93]

These topologies have been widely studied in several literatures [93] [95] [96]. The voltage gain of the Half-Bridge converter can be calculated as [93]:

$$\text{Half Bridge: } \frac{V_{OUT}}{V_{IN}} = \frac{N_S}{N_P} \times D \quad (\text{III.6})$$

And the voltage gain of the Full-Bridge [93]:

$$\text{Full Bridge: } \frac{V_{OUT}}{V_{IN}} = 2 \times \frac{N_S}{N_P} \times D \quad (\text{III.7})$$

Where,

- $N_P$  and  $N_S$ : the primary and secondary winding turns of the transformer
- $D$ : duty cycle of the control signal PWM

The advantage of the Half-Bridge converter and Full-Bridge converter over the flyback converter is the primary switch voltage stress that does not exceed the input voltage which means a full technological compatibility. For the half bridge, the transformer must implement a transformation ratio of 2 which is not optimized. On the other side, the integration of 2 or 4 switches is not an issue for the full bridge. Half bridges are not recommended here.

The main issue for this topology is clearly related to the need to implement an inductive output filter. The extra magnetic component will enlarge the volume of hybrid components which is not satisfactory.

To further improve the use of switches in the high frequency domain and optimize the size of the passive elements, resonant topologies could be good candidates.

**III.2.b-iii LLC resonant half bridge converter**

In order to remove the output inductive tank, the LLC resonant topology has been studied and is introduced in Fig.III.9.

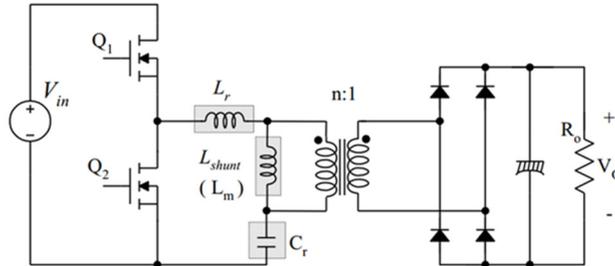


Fig.III.9 LLC resonant converter [97]

While Half-Bridge converter has commonly been used for isolated medium-power applications, this topology is often designed with resonant switching to achieve higher efficiency, an improvement that comes with added complexity but that nevertheless offers several performance benefits. A resonant half-bridge converter uses two inductors (LL) and a capacitor (C), known as an LLC configuration. Thanks to a high working frequency, the size of the passive components can be reduced [97] [98] and magnetic components can all be integrated into one device. The main time domain waveforms of the converter are depicted in Fig.III.10 for the voltages across the switches, the input voltage of the resonant tank, the resonant current and the secondary current at the resonant frequency point.

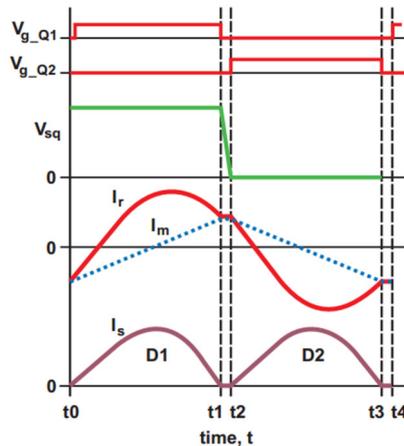


Fig.III.10 Operation of LLC at fo [97]

The resonant frequency [97] can be calculated as:

$$f_0 = \frac{1}{2\pi\sqrt{L_r \times C_r}} \tag{III.8}$$

And the voltage gain of this LLC resonant converter [98] when it operates at the resonant frequency is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{2} \times \frac{N_s}{N_p} \times M \tag{III.9}$$

Where,

- $N_P$  and  $N_S$ : the primary and secondary winding turns of the transformer
- $M$ : transfer ratio of the resonant circuit, working at resonant frequency  $M=1$

The control signal must be designed correctly at the ZVS (zero-voltage switching) point, otherwise the characteristics of the converter is out of the desirable values. This frequency issue becomes very critical for an integrated power supply where the control signal is locally generated by the logical block. After discussion with experts in designing precise clock generators, it has been decided to avoid the implementation of converters sensitive to the switching frequency precision like the resonant topologies do.

To overcome many of the drawbacks depicted in the previous topologies, the single-active bridge (SAB) converter and the dual-active bridge (DAB) converter are proposed in the next section.

**III.2.b-iv Dual Active Bridge converter (DAB)**

Many researches [89], [99], [100], [101], [102] have been engaged on the DAB converters for power levels from several watts to several kilo watts up to hundreds of kW. Its topology is depicted in Fig.III.11.

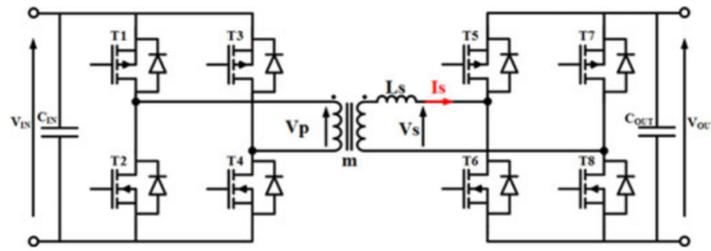


Fig.III.11 DAB topology [102]

Fig.III.12 shows the current waveforms in the leakage inductance of the transformer and the voltages applied on its primary and secondary sides  $V_P$  and  $V_S$ , respectively.

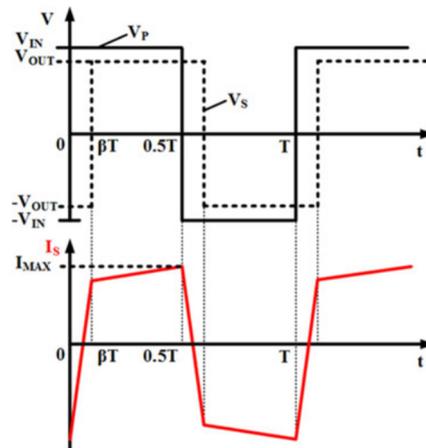


Fig.III.12 Current and voltage waveforms of DAB converter [102]

The voltage gain of a DAB converter [102] can be calculated as:

$$\frac{V_{OUT}}{V_{IN}} = \frac{(1 - 2\beta) \times \frac{N_S}{N_P} \times R}{f \times L_S} \quad (III.10)$$

Where,

- $N_P$  and  $N_S$ : the primary and secondary winding turns of the transformer
- $L_S$ : leakage inductance of the transformer
- $\beta$ : phase-shift of the control signal between the primary side and secondary side
- $R$ : resistive load at the output
- $f$ : switching frequency of the converter

Without the output inductor, a dual active-bridge topology contains only a transformer between the H-bridges of the primary side and secondary side. This converter is considered as a good candidate to reduce the number and sizes of passive elements.

The design of an integrated inverter leg and their closed driver circuits is carried out in order to benefit from the high level of integration and to reduce the amount of active components; finally the volume of the converter can be minimized. In [102], works demonstrated that, at low-power and low-voltage levels, the integrated DAB converter is a good candidate for high efficiency, high power density, and outstanding EMI and reliability performances.

The disadvantage of DAB is its control complexity; this topology needs a control signal for both sides with a controlled phase-shift between the secondary side and the primary side. That would imply an insulated communication between primary side and secondary side. In addition, its transfer function is very sensitive to the load levels, making open loop operation very critical.

### III.2.b-v Single Active Bridge converter (SAB)

In order to benefit the advantage of the integrated DAB converter and eliminate the complexity on the control of the secondary side of DAB converter, the single active bridge topology (SAB) is considered at last.

Several works [103], [104], [105] have been done on the SAB converter in a high level of power up to 1.2 kW. The SAB converter operates at very high frequency and high power and this topology is normally used where unidirectional power is needed. As we can see in Fig.III.13, the secondary side of the SAB converter is made of a simple full bridge diode rectifier.

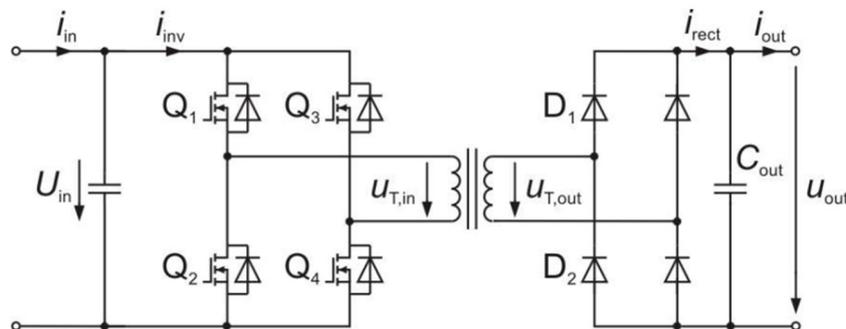


Fig.III.13 Topology of SAB converter[103]

Fig.III.14 shows the input and output voltages of the transformer and the corresponding input current (red dash line).

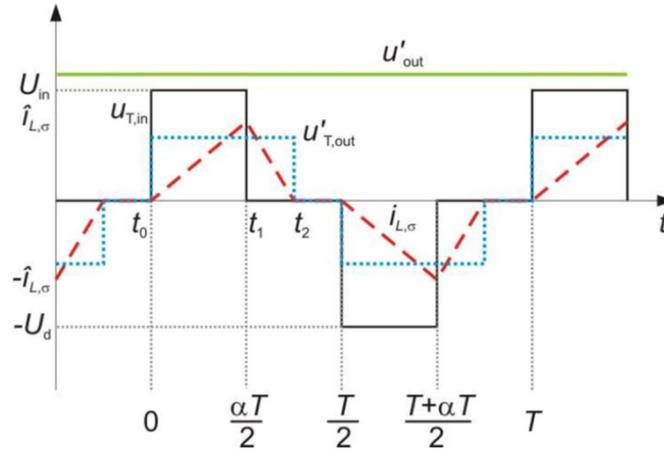


Fig.III.14 Transformer input voltage and the input current of SAB converter[103]

According to [103], the output voltage of the SAB converter can be expressed as:

$$V_{OUT} = \frac{N_p}{N_s} \frac{\alpha^2 \times V_{IN}^2}{\alpha^2 \times V_{IN} + 4 \times f \times \frac{N_s}{N_p} \times I_{OUT} \times L_{leakage}} \quad (III.11)$$

Where,

- $N_p$  and  $N_s$ : the primary and secondary winding turns of the transformer
- $L_{leakage}$ : leakage inductance of the transformer
- $\alpha$ : phase-shift of the control signal between the inverter legs
- $V_{IN}$  and  $I_{OUT}$ : are respectively the input voltage and the output current
- $f$ : switching frequency of the converter

In this static transfer function, the current in the magnetizing inductance of the transformer in [103] has been neglected due to the large size of the transformer for this specific application. If the SAB converter is considered as the converter for the low-power application as the power supply of the gate driver, the equation of the SAB converter must be re-derived.

However, Equation III.11 expresses that with a small output current and a low leakage inductance, the output voltage is quite stable when the frequency varies around the designed value. This argument is detailed in Section III.2.c and III.2.d. As a result, if the input voltage is considered stable, the output voltage may also remain quite stable at light loads.

Without any control on the secondary side, with a limited amount of passive components, especially a small HF transformer, with a limited dependence of the switching frequency and with active devices compatible with the technology, this converter looks like a good candidate for our purpose.

As we can see in these comparisons:

- ❖ Flyback converter has a high blocking voltage on the input switch (normally is double) then the implementation on our selected technology is complex where only the 10V devices are available. Moreover, due to the presence of the large leakage inductance and primary-secondary parasitic capacitance of the transformer, the propagated EMI from the power part and self-generated EMI are critical.

- ❖ The half-bridge and the full-bridge converters do not have the high blocking voltage on the input switch as flyback converter but require an inductive output filter, which enlarge the volume of hybrid components that is not satisfactory for our power supply design.
- ❖ The resonant topology seems like the best choice under the propagated EMI and self-generated EMI thanks to its compact transformer. But the resonant topology is sensitive to the precision of the frequency. In our integrated power supply, the control signal is locally generated by the logical block. We decided to avoid the implementation of the resonant converter after discussion with experts in designing precise clock generators.
- ❖ The DAB converter and the SAB converter seem like the most suitable candidates for such a special power supply for gate driver circuits. The DAB converter needs control signals for both primary side and secondary side which complicates the insulator for the signal. The open-load implantation is critical due to the sensitive transfer function of the DAB converter on the load levels
- ❖ Meanwhile the SAB converter does not need the control signal for the secondary side; only a small HF transformer is used as the passive component. The SAB converter has limited dependence of the switching frequency and the active devices are compatible with the selected integrated technology, this converter looks like a good candidate for our purpose.

According to these analyses, the SAB converter is selected for an isolated high side power supply for gate driver circuits. In the next section, the derivations of the SAB converter are presented step-by-step and then the validations are demonstrated to ensure further design of the SAB converter. The designs of the primary and secondary circuits are described, considering their monolithic integration in the high temperature integrated technology context (CMOS SOI XFAB XT018 technology).

#### III.2.c The selected topology: the SAB converter (SAB)

##### III.2.c-i Operating principle of SAB

To understand its functioning, the basic circuit of SAB is depicted in Fig.III.15; the transformer is represented by the leakage inductance –  $L_{in}$ , the magnetizing inductance –  $L_m$  and the transformer ratio  $N_p/N_s$ .

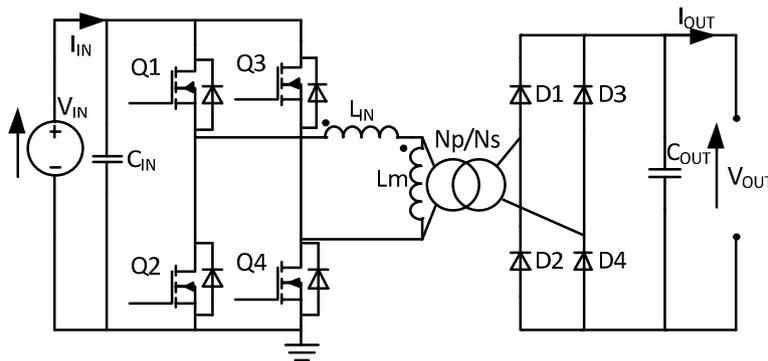


Fig.III.15 Equivalent circuit of SAB

A simplified circuit of SAB is shown in Fig.III.16 where the transformer ratio is removed in order to ease formula derivations.

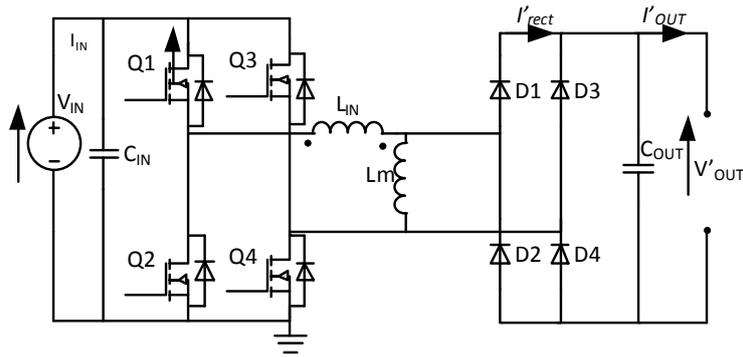


Fig.III.16 SAB topology without the idealized transformation ratio

Through the transformer, the modeling output voltage and current in the simple equivalent circuit can be rewritten as:

$$v'_{OUT} = v_{OUT} \times \frac{N_P}{N_S} = \frac{v_{OUT}}{N} \tag{III.12}$$

And,

$$i'_{OUT} = i_{OUT} \times \frac{N_S}{N_P} = i_{OUT} \times N \tag{III.13}$$

Where,

- $v_{OUT}$  and  $i_{OUT}$ : the output voltage and output current of the SAB
- $v'_{OUT}$  and  $i'_{OUT}$ : the output voltage and output current with the idealized transformer ratio
- $N_P, N_S$ : the primary and secondary winding turns of the transformer
- $N = N_S/N_P$ : winding turns ratio

Fig.III.17 shows the control signal sequence of the SAB converter where the pair of the control signals of Q1-Q2 and the pair of Q3-Q4 are complementary. The phase-shift between these control signal pairs changes the duty-cycle of the imposed voltage on the primary side of the transformer ( $V_{H-Bridge}$ ).

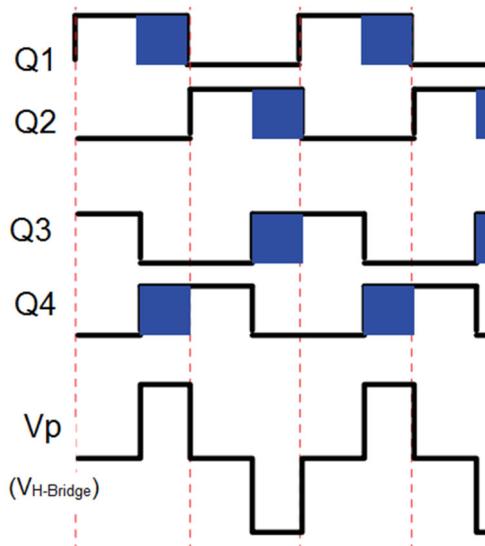


Fig.III.17 PWM wave forms of the H-bridge

Based on the waveform of the primary voltage of the transformer with the leakage inductance and the magnetizing inductance and the works on the SAB converter [103], [104], [105], the theoretical waveforms of the current can be depicted in Fig.III.18:

- $V_p$ : primary voltage of the transformer (blue)
- $i_p$ : primary current or current on the leakage inductance (yellow)
- $i_M$ : current on the magnetizing inductance (black)
- $i_s$ : secondary current (red)
- $i'_{out}$ : output current without the idealized transformer ratio (red, dash line)
- $I_{Lin-max}$ : maximum current on the leakage inductance
- $I_{Lm-max}$ : maximum current on the magnetizing inductance
- $\alpha$ : phase-shift of the control signals of the H-Bridge (between Q1-Q3 and Q2-Q4)

The evolutions of the current  $i_p$ ,  $i_M$  depend on the value of the inductances where the leakage inductance is much smaller than the magnetizing inductance in reality.

For more details, three different modes are analyzed from  $t_0$  to  $t_3$ :

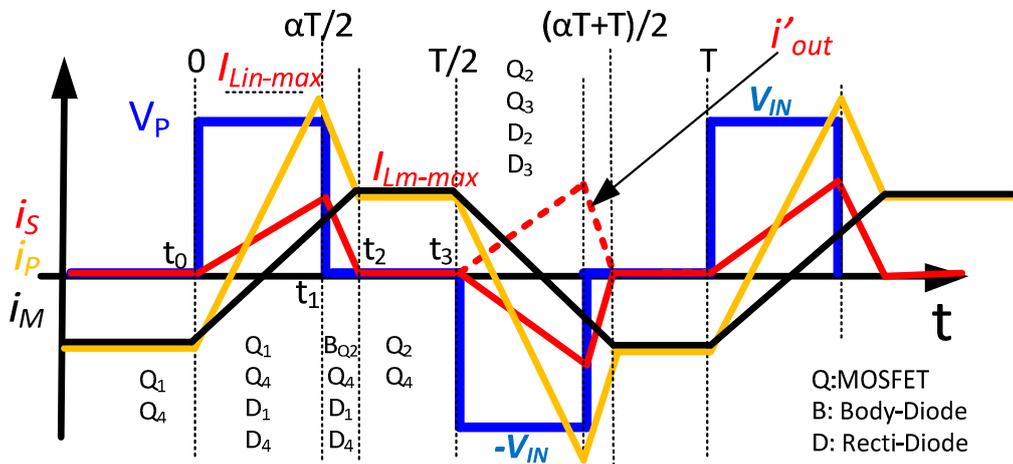


Fig.III.18 Waveforms of SAB converter: the input voltage of the transformer and the output voltage of SAB

As the Fig.III.18, before  $t_0$ , the output current is equal to zero; the output diodes are not polarized. From  $t_0$  to  $t_1$ , Q1 and Q4 are conducting, the currents evolves on the leakage inductance and the magnetizing inductance, the secondary current begins to increase, the diodes D1 and D4 are polarized, the energy is transferred from the primary side to secondary side. The current on the leakage inductance and the secondary current reach the maximum values in the end of this energy delivery mode.

From  $t_1$  to  $t_2$ , Q2 begins to conduct, the current on the leakage inductance decreases due to the absence of the input voltage. The secondary current decreases but always positive, D1 and D4 are still polarized, and then the current on the magnetizing inductance continues to increase thanks to the output voltage.

When the current on the leakage inductance is equal to the current on the magnetizing inductance, the secondary current disappears from  $t_2$  to  $t_3$ . D1 and D4 are not polarized during this interval.

The output current increases when the energy delivery mode is activated once again after  $t_3$  by the conduction of Q2 and Q3.

For more details, we derive the relations between the currents and the voltage from  $t_0$  to  $t_3$  in order to build up a voltage transfer function of the SAB converter.

**III.2.c-ii Design calculations**

**MODE 1: power delivery mode:  $t_0 < t < t_1$**

The mode 1 begins when the switches Q1 and Q4 are in conduction mode meanwhile Q2 and Q3 are open, see Fig.III.19.

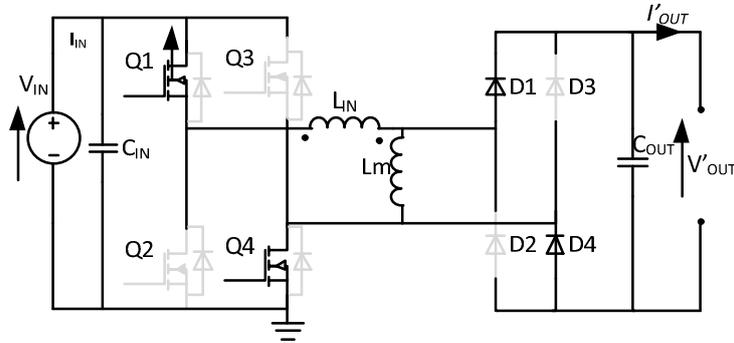


Fig.III.19 Simple equivalent circuit of SAB during MODE 1

Before  $t_0$ , the output current is equal to zero; the output diodes of the rectifier are not polarized.

At  $t=t_0$ , the current through the leakage inductance and the magnetizing inductance increase, the secondary current raises up, thereby diodes D1 and D4 conduct.

An equivalent circuit in MODE 1 is given in Fig.III.20.

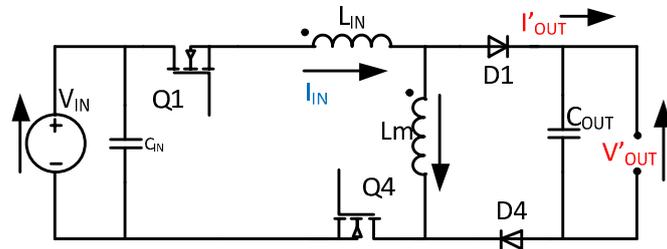


Fig.III.20 Simplified circuit during MODE 1

The currents through the inductances can be calculated as:

$$i_{L_{IN}}(t) = i_{L_{IN}}(t_0) + \frac{v_{Lin}(t)}{L_{IN}} \times t = i_{L_{IN}}(t_0) + \frac{V_{IN}}{L_{IN}} \frac{v'_{OUT}}{2} \times t \tag{III.14}$$

$$i_{L_M}(t) = i_{L_M}(t_0) + \frac{v_{LM}(t)}{L_M} \times t = i_{L_M}(t_0) + \frac{v'_{OUT}}{L_M} \times t \tag{III.15}$$

At  $t=t_1$ , we have:

$$i_{L_{IN}}(t_1) = I_{L_M-MAX} + \frac{V_{IN}}{L_{IN}} \frac{v'_{OUT}}{2} \times \frac{\alpha T}{2} \tag{III.16}$$

$$i_{L_M}(t_1) = I_{L_M-MAX} + \frac{v'_{OUT}}{L_M} \times \frac{\alpha T}{2} \quad (III.17)$$

**MODE 2: Q2 in the switch mode  $t_1 < t < t_2$  where  $t_1 = \alpha T/2$**

The mode 2 begins when Q1 opens, Q2 begins to switch. At this moment, the voltage of the primary side of the transformer is equal to zero, the energy delivery mode finishes. The current on the leakage inductance begin to reduce and then the output current decreases. The current in the magnetizing inductance keeps increasing thanks to the presence of the output voltage. D1 and D4 are polarized until the secondary current disappears (see Fig.III.17, Fig.III.18).

The equivalent circuit during this interval, MODE 2, can be depicted in Fig.III.21.

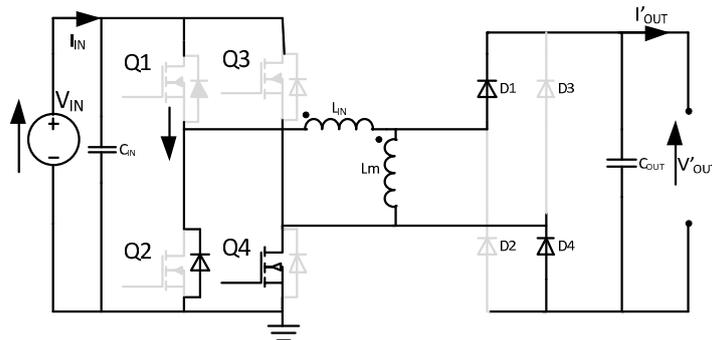


Fig.III.21 Simple equivalent circuit of SAB during MODE 2

MODE 2 ends when these two currents are equal, then the secondary current is zero until the end of the half period: see the waveforms in Fig.III.18.

The simple circuit of the MODE 2 is redrawn in Fig.III.22.

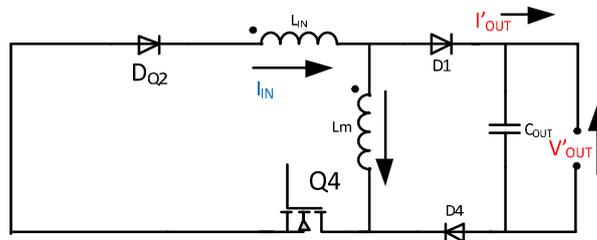


Fig.III.22 Simplified circuit during MODE 2

The currents through the inductances can be calculated as:

$$i_{L_{IN}}(t) = i_{L_{IN}}(t_1) + \frac{v_{L_{IN}}(t)}{L_{IN}} \times t = i_{L_{IN}}(t_1) + \frac{v'_{OUT}}{L_{IN}} \times t \quad (III.18)$$

$$i_{L_M}(t) = i_{L_M}(t_1) + \frac{v_{L_M}(t)}{L_M} \times t = i_{L_{IN}}(t_1) + \frac{v'_{OUT}}{L_M} \times t \quad (III.19)$$

At  $t=t_2$ , we have:

$$i_{L_{IN}}(t_2) = i_{L_{IN}}(t_1) + \frac{v'_{OUT}}{L_{IN}} \times (t_2 - t_1) = I_{L_M-MAX} \quad (III.20)$$

$$i_{L_M}(t_2) = i_{L_{IN}}(t_0) + \frac{v'_{OUT}}{L_M} \times t_2 = I_{L_M-MAX} \quad (III.21)$$

In the next stage, the output current is equal to zero as the end of MODE 2.

**MODE 3: Free-Wheeling mode,  $t_2 < t < t_3$  where  $t_3 = T/2$**

The mode 3 begins when Q2 switches to the conduction mode, Q4 still conducts; meanwhile Q1 and Q3 are open. During the MODE 3, the input voltage does not appear on the primary side of the transformer; the current on the leakage inductance and the current on the magnetizing inductance are the same. Hereby the secondary current is equal to zero, and the diodes of the rectifier are not polarized as depicted in Fig.III.23.

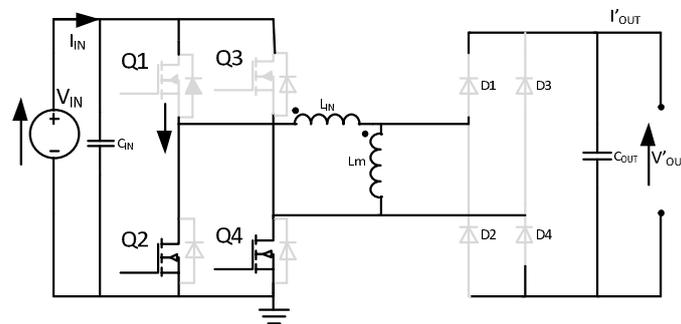


Fig.III.23 Simple equivalent circuit of SAB during MODE 3

The simple circuit of the MODE 3 is given in Fig.III.24.

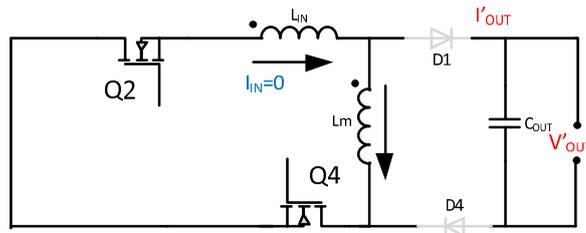


Fig.III.24 Simplified circuit during MODE 3

During this interval, the currents on the leakage inductance and the magnetizing inductance are constant. We have:

$$i_{L_M}(t) = I_{L_M-MAX} \text{ with } t_2 < t < t_3 \quad (III.22)$$

$$i_{L_{IN}}(t) = I_{L_M-MAX} \text{ with } t_2 < t < t_3 \quad (III.23)$$

During these three intervals (MODE1, MODE2 and MODE 3) from  $t_0$  to  $t_3$ , the average currents through the input inductance and the magnetic inductance can be calculated. And then the difference of these two currents is equal to the equivalent average output current.

From  $t_0$  to  $t_3$ , we have the equivalent output current under the turn ratio:

$$I'_{OUT} = \frac{1}{T/2} \times \int_{t_0}^{t_3} [i_{L_{IN}}(t) \quad i_{L_M}(t)] \times dt \quad (III.24)$$

During the interval  $t_2$  to  $t_3$ , the currents in the inductances  $L_{in}$  and  $L_m$  are equal which means the output current is equal to zero; the average output current is calculated by using the equivalent output current and can be expressed as:

$$I_{OUT} = \frac{I'_{OUT}}{N} = \frac{2}{T \times N} \times \int_{t_0}^{t_2} [i_{L_{IN}}(t) \quad i_{L_M}(t)] \times dt \quad (III.25)$$

Using the equations of the currents in three intervals for MODE 1, MODE 2 and MODE 3, the output current can be calculated as:

$$I_{OUT} = \frac{V_{IN} \times \alpha^2 \times \left[ N \times V_{IN} \times \frac{L_M}{L_{IN}} \quad V_{OUT} \times \left( 1 + \frac{L_M}{L_{IN}} \right) \right]}{4 \times f \times V_{IN} \times L_{IN} \times \left( 1 + \frac{L_M}{L_{IN}} \right)} \quad (III.26)$$

In the primary side of the transformer, the maximum input current can be written as:

$$I_{L_M-MAX} = \frac{V_{IN} \times \alpha}{4 \times f \times (L_{IN} + L_M)} \quad (III.27)$$

And the maximum current through the input inductance is:

$$I_{L_{IN}-MAX} = \frac{\alpha \times \left[ V_{IN} \times N \times \left( 1 + 2 \times \frac{L_M}{L_{IN}} \right) \quad 2 \times V_{OUT} \times \left( 1 + \frac{L_M}{L_{IN}} \right) \right]}{4 \times f \times V_{IN} \times (L_{IN} + L_M)} \quad (III.28)$$

Also, we can derive the relation between the output voltage of the SAB converter and the output current and the switching frequency.

$$v_{OUT}(f, i_{OUT}) = \frac{V_{IN}^2 \times \alpha^2 \times N \times \left( \frac{L_M}{L_{IN}} \right)^2}{(4 \times N \times f \times i_{OUT} \times L_{IN} + V_{IN} \alpha^2) \times \left( 1 + \frac{L_M}{L_{IN}} \right)} \quad (III.29)$$

Equation III.29 expresses the frequency and the output current as the variables of the output voltage in order to study the stability of the output voltage of the SAB converter.

In the design of the SAB converter, with the specification of Table.III.2, the input voltage and output voltage, as well as the output power are defined; the values of the transformer can be calculated and optimized accordingly.

As we mentioned in the beginning, the SAB converter has an advantage towards the objective of monolithic integration. The simulation results and the calculated results give the output voltage of SAB converter as the function of the switching frequency and the output load. In the simulation, the phase-shift between two inverter legs varies between  $180^\circ$  ( $\alpha = 0.5$ ) and  $360^\circ$  ( $\alpha = 1$ ).

**III.2.d Validation of SAB converter**

**III.2.d-i Simulations**

To validate the calculation of the SAB converter, an idealized PSIM simulation is proposed that can be seen in Fig.III.25. We consider idealized components for these validations.

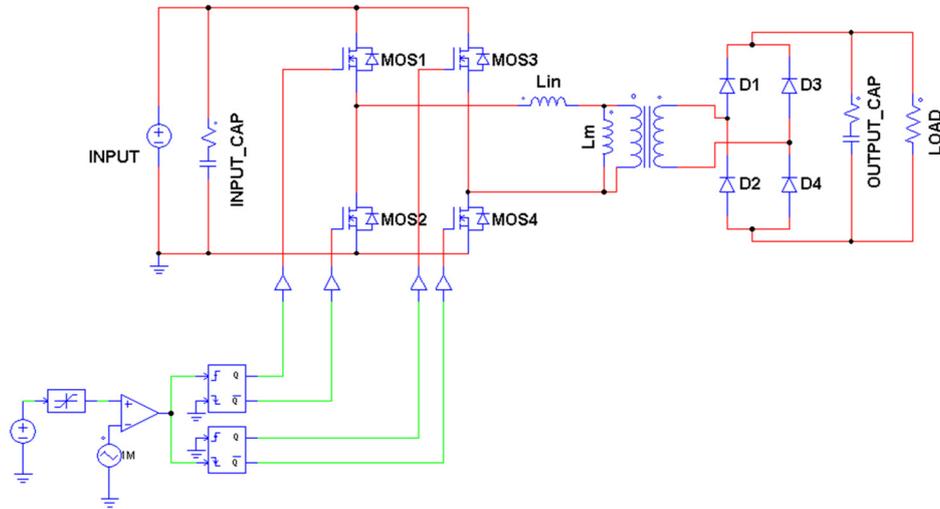


Fig.III.25 An idealized PSIM simulation of a SAB converter

The parameters are calculated by using the Equations III.26, III.27 and III.28 and then assigned to the components of PSIM simulation.

The parameters of the elements are shown in Table.III.3.

Table.III.3 Parameters of idealized PSIM simulations

Parameter	Value
$L_{in}$	2 $\mu$ H
$L_m$	72.8 $\mu$ H
Idealized transformer ratio	30/23 ( $N_p=23, N_s=30$ )
Phase-shift	180 <sup>0</sup> ( $\alpha = 0.5$ )

In Fig.III.26, the idealized transient simulation of the SAB converter gives the waveforms of the input current  $i_{IN}$ , magnetizing current  $i_M$  and the secondary current as  $i_{SEC}$ , the output voltage of the H-bridge and output voltage of the SAB converter as  $V_{H\_Bridge}$  and  $V_{OUT}$ .

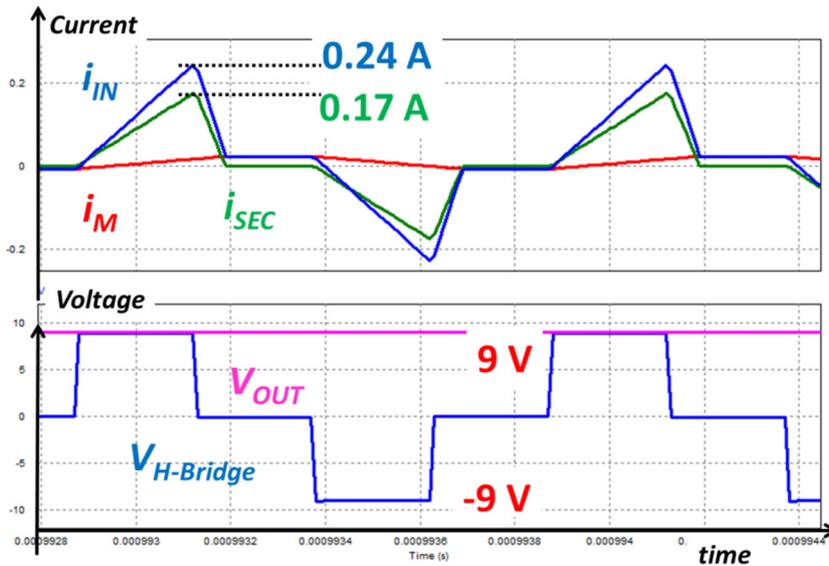


Fig.III.26 SAB waveforms of the idealized simulation with  $L_{in} = 2\mu H$ ,  $L_m=72.8\mu H$ ,  $f = 1\text{ MHz}$  and  $\alpha = 0.5$

Based on Equation III.29 and the PSIM simulations, simulation and analytical results are shown in Fig.III.27. As we have seen, the output load may vary from 5 mA (50 mW) up to 60 mA (680 mW), and the output voltage decreases from 10.8 V to 8.8 V. The specifications in the MEGaN project for the XFAB technology indicate a nominal voltage of 9V for 500mW with a maximum voltage of 12V [106] to guarantee that the CMOS driver die does not go into voltage breakdown of the XFAB transistor. At the designed point, current is equal to 56 mA meanwhile the value of the voltage is 9 V.

The relation between output voltage of the SAB converter and the output current can be expressed as:

$$v_{OUT}(i_{OUT}) = \frac{V_{IN}^2 \times \alpha^2 \times N \times \left(\frac{L_M}{L_{IN}}\right)^2}{(4 \times N \times f \times i_{OUT} \times L_{IN} + V_{IN}\alpha^2) \times \left(1 + \frac{L_M}{L_{IN}}\right)} \quad (III.30)$$

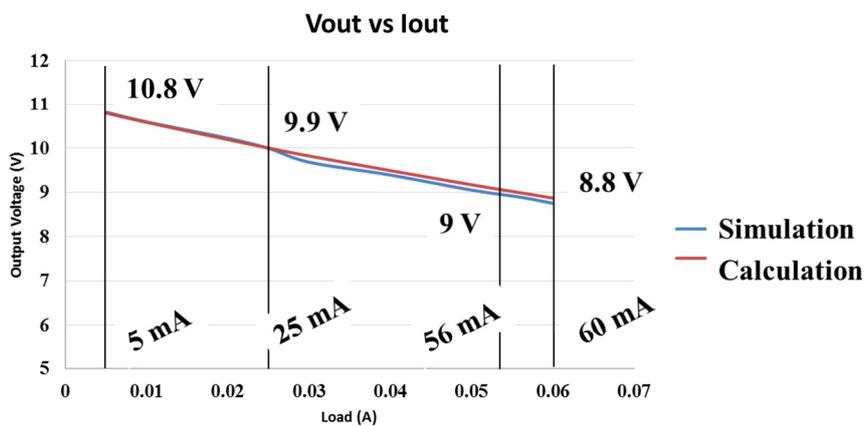


Fig.III.27 Comparison of the output voltage versus the output load between the idealized analytical calculation and the idealized PSIM simulation,  $L_{in} = 2\mu H$ ,  $L_m=72.8\mu H$ ,  $f=1\text{ MHz}$  and  $\alpha = 0.5$

The evolution of the output voltage of the SAB converter when the frequency varies from 500 kHz to 1.5 MHz is calculated: Fig III.28.

From Equation III.29, the relation between output voltage of the SAB converter and the frequency is:

$$v_{OUT}(f) = \frac{V_{IN}^2 \times \alpha^2 \times N \times \left(\frac{L_M}{L_{IN}}\right)^2}{(4 \times N \times f \times i_{OUT} \times L_{IN} + V_{IN} \alpha^2) \times \left(1 + \frac{L_M}{L_{IN}}\right)} \quad (III.31)$$

Around the designed frequency of 1 MHz, the output voltage of the SAB varies between 8.3 V (1.5MHz) and 9.7 V (0.5MHz) that is satisfying according to the requirements of the gate driver circuit.

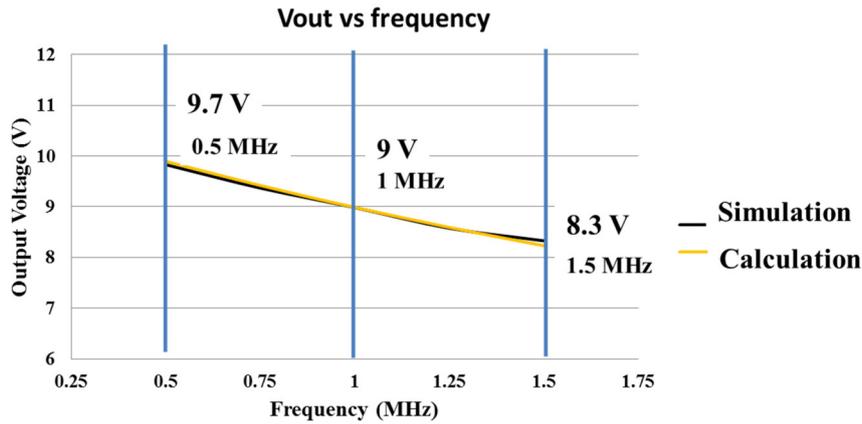


Fig.III.28 Comparison of output voltage versus frequency from 0.5 MHz to 1.5 MHz with  $L_{in} = 2\mu H$ ,  $L_m = 72.8\mu H$ , the resistive load  $R_{out} = 162 \Omega$  and  $\alpha = 0.5$

In the extreme case, where this scenario happens:

- the load is minimum in the design range as 5 mA
- the switching frequency is minimum as 500 kHz

The output voltage in the simulation is 11.1 V and the calculated value is 10.9V. In order to avoid the failure of the gate driver circuit due to over voltage of the power supply, a protection must be implemented. The simplest way to clamp the output voltage of the SAB converter under 10V is a 10V Zener diode.

### III.2.d-ii Experiments

To verify the characteristics of the SAB converter, we used a series-series resonant full bridge converter developed in G2ELab [107]. The resonant tank has been removed; the H-bridge and the diode rectifier were kept. Finally, a transformer with a cylindrical magnetic-core was placed in the middle of the circuit for the 1kV of galvanic isolation: see Fig.III.29.

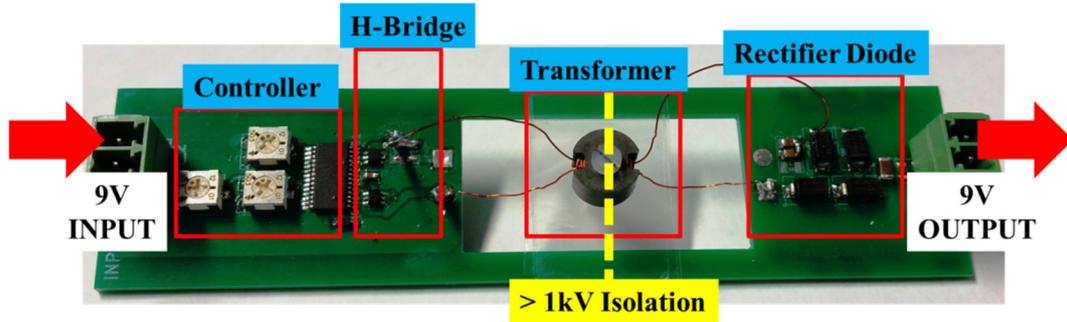


Fig.III.29 SAB converter prototype on a PCB implemented with discrete components

Fig.III.30 shows the experimental waveforms of the SAB converter. In this setup, the input voltage is 9V, the switching frequency is 1 MHz, and the output voltage is 9V with 500mW of the output power. The transformer of the SAB converter has been made for adapting the output voltage and the input voltage. By characterizing the transformer, the leakage inductance is equal to  $8.8\mu\text{H}$ , the magnetizing inductance of  $133\mu\text{H}$  is obtained, the turn ratio of the transformer is  $N_p/N_s=22/30$ .

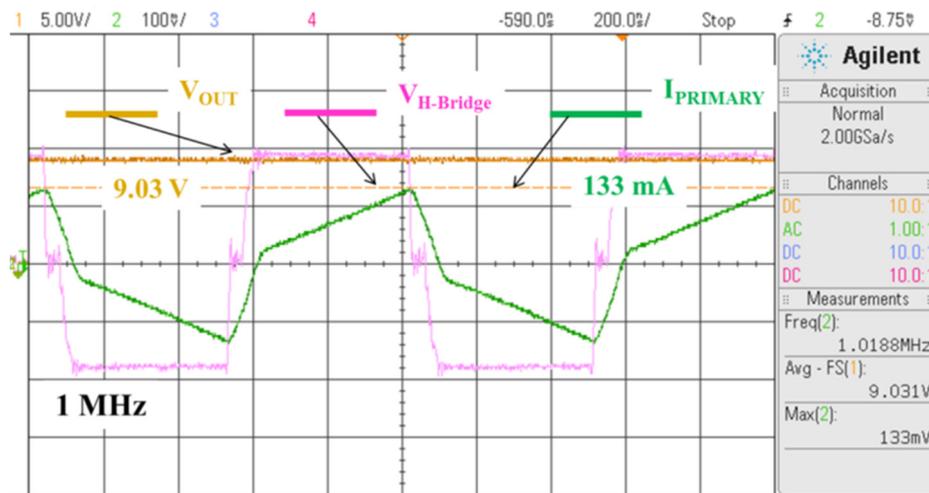


Fig.III.30 Waveforms of the SAB converter, experimental results: output voltage, H-Bridge voltage and primary current with  $L_{in}=8.8\mu\text{H}$ ,  $L_m=133\mu\text{H}$ ,  $N_p/N_s=22/30$ ,  $\alpha=0.95$  and  $R_{out}=162\Omega$

The parameters of the transformer have been modified to adapt the values in the PSIM simulations. To compare the experimental results and the simulation results, Table III.4 show the new parameters of the simulations including the parasitic resistance of the transformer, the On-resistance of the transistor and the drop voltage on the diode.

Table.III.4 Parameters of realistic PSIM simulations

Parameter	Value
$L_{in}$	$4.2 \mu\text{H}$
$L_m$	$60 \mu\text{H}$
transformer ratio	12/16 ( $N_p=12$ , $N_s=16$ )
parasitic resistance of transformer	$4 \Omega$
drop voltage on diode	$0.2 \text{ V}$
Phase-shift $\alpha$	$\alpha = 0.95$

With these parameters, Fig.III.31 shows the simulation results of the output voltage, the H-Bridge voltage and the primary current of the SAB converter with the realistic values of Table.III.4.

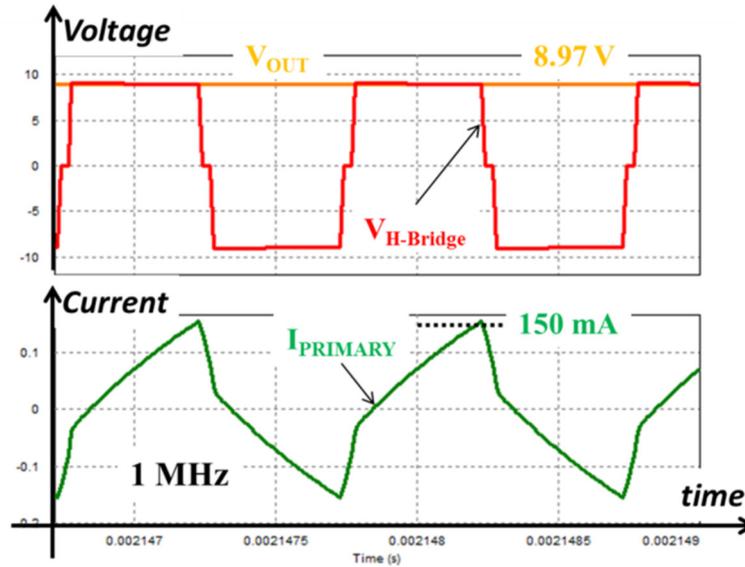


Fig.III.31 Waveforms of the SAB converter, simulation results with realistic parameters

In this setup, the phase-shift  $\alpha$  of the control signals of the inverter is equal to 0.95. This is an open-loop SAB converter; however the frequency can be adapted between 0.5 MHz and 1.5 MHz. In Fig.III.32 and Fig.III.33, we propose comparisons between transient PSIM simulations and experimental results on the output voltages as the function of the output load and the switching frequency.

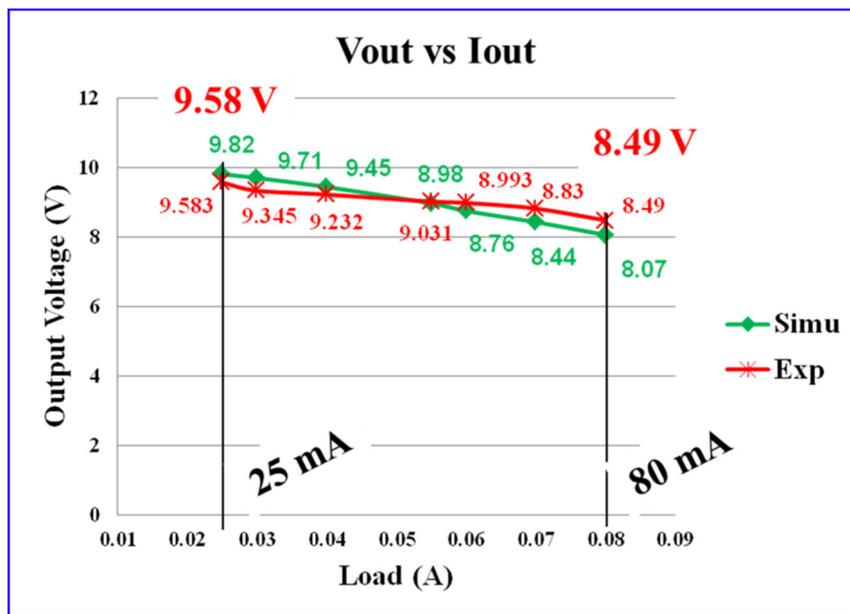


Fig.III.32 Output voltage as a function of the output load from 25mA to 80mA with the frequency of 1MHz, simulation and experimental results

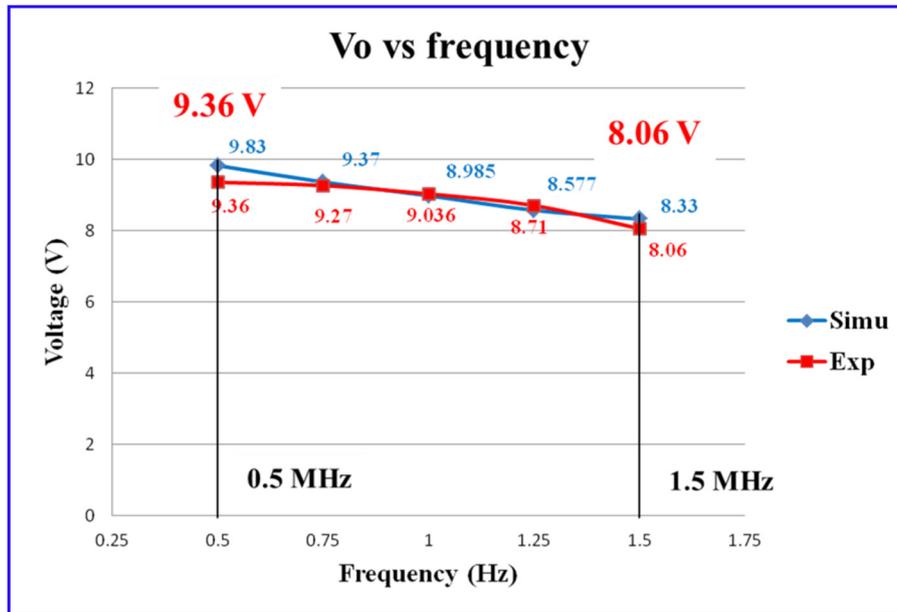


Fig.III.33 Output voltage as a function of the switching frequency from 0.5 MHz to 1.5 MHz with an output resistive load of 165  $\Omega$ , simulation and experimental results

As we have seen in Fig.III.32, the output load may vary from 25 mA up to 80 mA, and the output voltage decreases from 9.58 V to 8.49 V. This comparison also confirms that, with 50% deviation of the designed frequency, the output voltage varies of about 10%. So we can assume that the SAB converter proposes a suitable robustness of the switching frequency dispersion induced by the manufacturing process tolerances.

The protection circuit is recommended to keep the output voltage of the gate driver circuit staying in the safe zone in the worst case scenario such as the minimum load and lowest frequency.

In the next section, the designs of the active elements of the SAB converter in the XT0.18 XFAB high temperature integrated technology are presented in details: H-Bridge inverter and rectifier of the SAB converter.

G2Elab focused his efforts on the design of the active parts, and only this part will be reported in the design issues addressed here. As we mentioned in Chapter I, the design and manufacture of the high temperature transformer is carried out by AMPERE Laboratory, an academic partner of MEGaN project that is not presented in this work.

### III.3 Integrated high side power supply for high temperature

The low side - high side power supply is a part of the “fully” integrated gate driver circuit. Fig.III.34 shows the high temperature power supply as a part of the integrated high temperature gate driver circuitry.

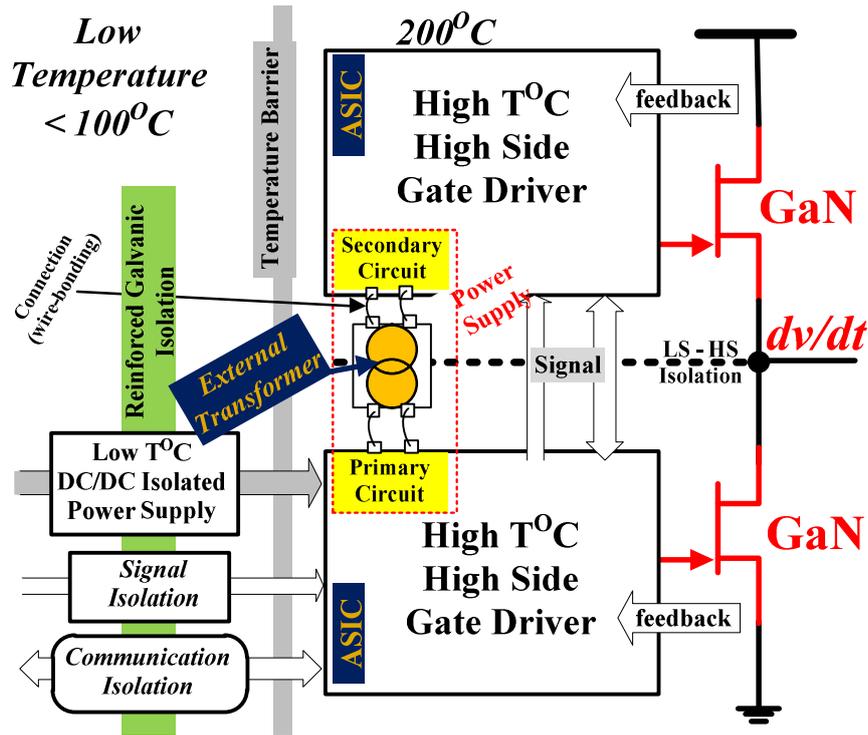


Fig.III.34 Gate driver architecture with the high temperature power supply

In this gate driver circuitry, the same ASICs (Application-Specific Integrated Circuit) are used for the low side gate driver and the high side gate driver. In this ASIC, there are the logical functions, the isolated control signal unit from low side to high side, the buffers and the power supply functions.

The primary circuit of the SAB converter is in the low side ASIC and the secondary circuit of the SAB converter is located in the high side ASIC. Between the low side ASIC and the high side ASIC, a high temperature transformer is used for the low side – high side galvanic isolation (designed by AMPERE Lab).

In this work, the active circuits of the power supply are designed and implemented.

### III.3.a High temperature technology for the active elements of the power supply: XFAB XT018

The XFAB XT018 (CMOS SOI technology) was made available through the project MEGaN. This integrated technology was chosen over several criteria: high temperature operation, high current capability, wide voltage range with multiple components at different voltages levels and the oxide boxes to isolate the parts of the overall circuit.

It is an SOI (Silicon-On-Insulator) partially depleted with 6 available metal levels (MET1, MET2, MET3, MET4, METTP, METHK). Furthermore, this technology implements oxide boxes which limit the crosstalk between the circuits and the substrate; it means that the leakage currents and parasitic capacitances are minimized. A low leakage current remains a critical factor, especially at high temperatures (the temperature range for this technology is from  $-40^{\circ}\text{C}$  to  $175^{\circ}\text{C}$  [106]).

A cross section of the XFAB XT018 technology with the layers of metal is depicted in Fig.III.35 where we can see that the layer DTI (Deep-Trench-Isolation) isolates the devices from the substrate.

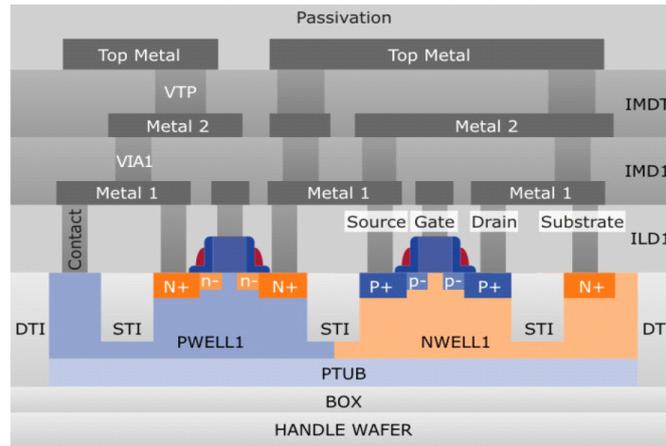


Fig.III.35 Devices schematic cross section of XFAB XT018[106]

III.3.b Design of the integrated H-bridge of the SAB converter

There are two active circuits into a SAB converter: the primary circuit is an H-Bridge inverter and the secondary circuit is an H-bridge rectifier. Fig.III.36 shows the schematic of the primary circuit.

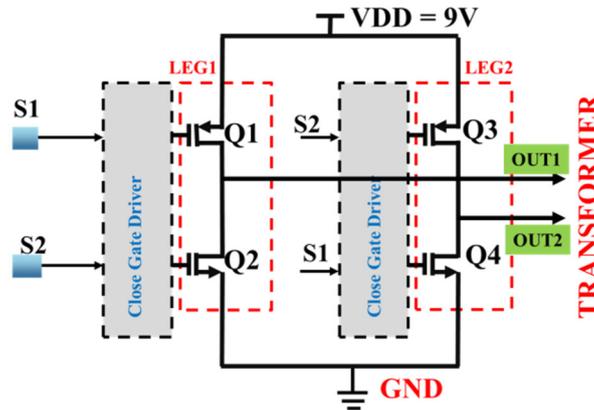


Fig.III.36 H-Bridge of the SAB converter

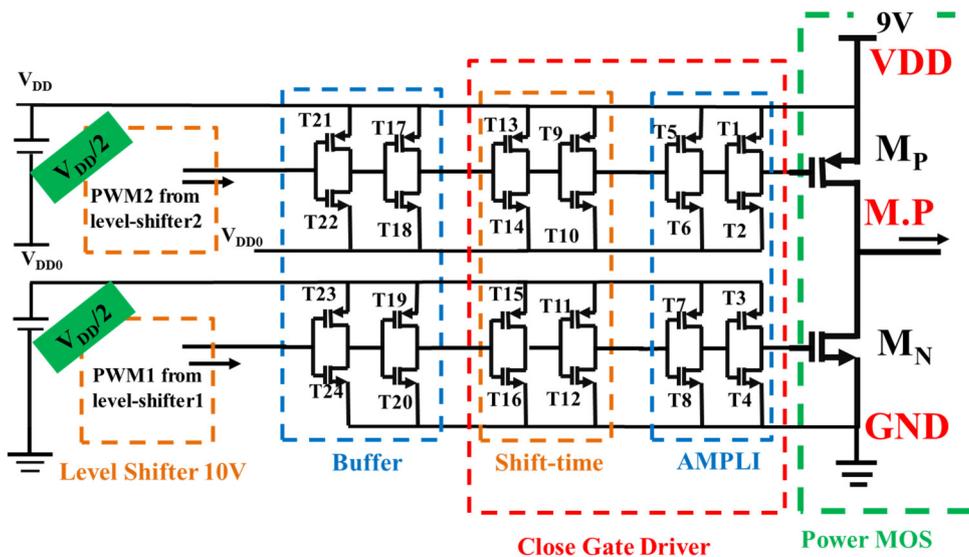


Fig.III.37 Schematic of the inverter leg with level shifters and buffers [89], [108], [109]

Inside of the primary circuit of the SAB converter, there are two inverter legs: LEG1 and LEG2. The schematic of an inverter leg including the power devices and their associated gate drivers is shown in Fig.III.37.

The validations in the experiments in Fig.III.29 show the input average current of 75 mA, the peak value of the input current is 143mA for the designed output current of 56mA (500mW). Hereby the current rating of the inverter leg design in the integrated technology is over-estimated to 100 mA for 10V power transistors.

The power transistors of the inverter leg are a PMOS at the high side named  $M_P$  and a NMOS at the low side named  $M_N$ . An analytical calculation is carried out to optimize the efficiency of the power structure, where the conduction, switching and charging losses are estimated by Equations III.30 and III.31 [14], [34]:

$$P_{Conduction} = \frac{1}{2}(R_{DSon\_N} + R_{DSon\_P})I^2 \quad (III.30)$$

$$P_{Switching} = \frac{1}{2}(C_{DS\_N} + C_{DS\_P})V_{DD}^2 f \quad (III.31)$$

$$P_{Charging} = \frac{1}{2}(C_{ISS\_N} + C_{ISS\_P})V_{DD}^2 f \quad (III.32)$$

Where,

- $I$ ,  $V_{DD}$  and  $f$ : the designed current, voltage and frequency of inverter leg
- NMOS parameters:  $R_{DSon\_N} = K_{R\_N}/W_N$ ,  $C_{ISS\_N} = K_{ISS} * W_N$ ,  $C_{DS\_N} = K_{SD} * W_N$
- PMOS parameters:  $R_{DSon\_P} = K_{R\_P}/W_P$ ,  $C_{ISS\_P} = K_{ISS} * W_P$ ,  $C_{DS\_P} = K_{SD} * W_P$

The PMOS and NMOS parameters are taken from the datasheet of the technology XT018 [106].

Fig.III.38 shows the evolution of the conduction loss, the switching loss, the charging loss and the total losses as a function of the N-channel width. As we can see, the total losses are optimal when the N-channel width is between 7 mm and 13 mm.

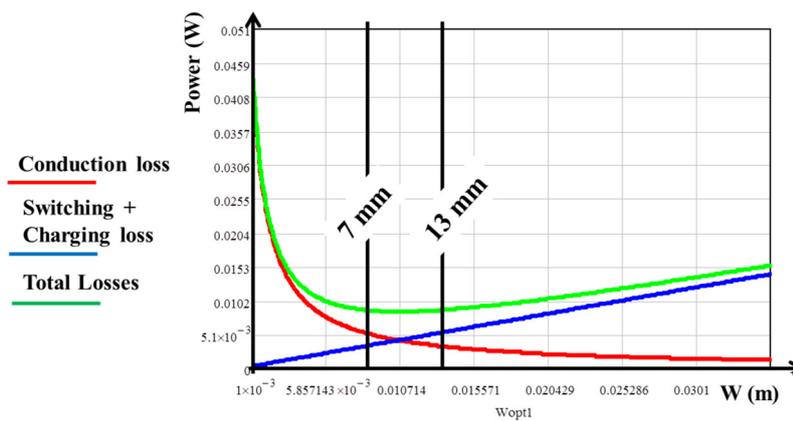


Fig.III.38 Losses and the N-channel width (Technology XFAB XT018,  $V_{DD}=10 V$ ,  $I = 0.1 A$ )

In fact, there is another loss which impacts to the calculation; this is the loss of the driver circuit. For selecting an optimal N-channel width, we need to calculate this loss of the gate driver. Due to the dependence of the loss of the gate driver on the channel widths of the power transistors, this loss is estimated.

Fig.III.39 shows the conduction loss, the charging loss, the switching loss, the estimated loss of the gate driver, the total losses and a theoretical efficiency in the calculation.

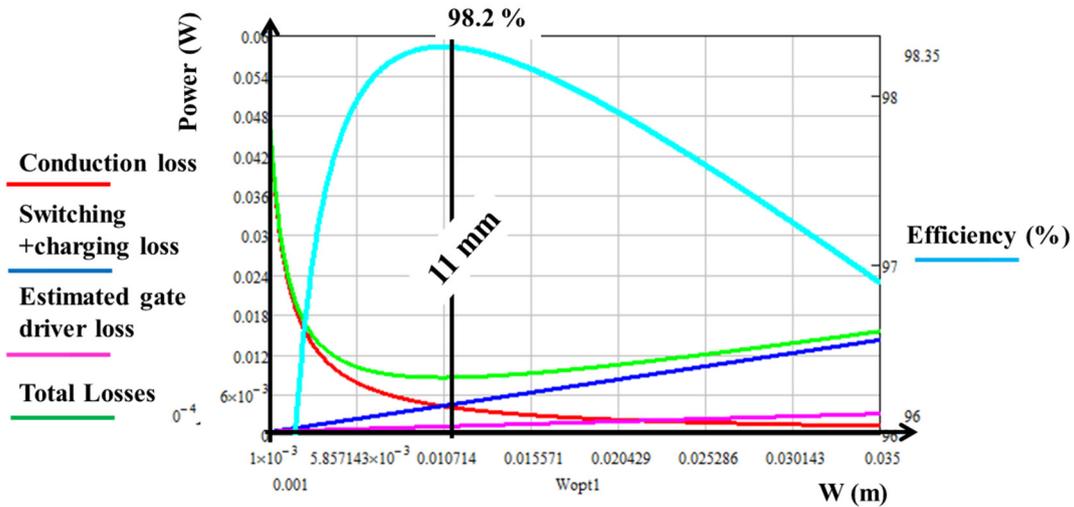


Fig.III.39 Theoretical efficiency with the estimated charging loss and the optimal N-channel width

The acceptable level of losses chosen involves the choice of the technology and the switching frequency of our structure. In theory, an efficiency of 98% for the inverter leg can be reached considering a nominal voltage and a current respectively equal to 10V and 100 mA.

The derivative of total losses expression gives the optimal gate width which depends on the technology characteristics and the specifications [34] that can be calculated as:

$$W_{N\_Optimal} = \sqrt{\frac{I^2(K_{R\_P} + 3K_{R\_N})}{12V_{DD}^2 f(K_{GS} + K_{DS})}} \tag{III.33}$$

Fig.III.40 presents the optimal channel width of the first amplification stage transistors, which achieves the best compromise between size and losses. As a result at the efficiency of 98.2%, we obtain the following values for the channel widths:

$$W_N = 11 \text{ mm and } W_P = 33 \text{ mm}$$

The parameters of the power transistors are shown in the table below:

Table.III.5 Parameters of the power transistors

	Power NMOS	Power PMOS
ON resistance	487 mΩ	337 mΩ
Drain Source Capacitance	7.45 pF	2.24 pF
Input Capacitance	1.49 pF	4.47 pF

At the optimal channel widths, the losses in the inverter leg can be presented as Table.III.6.

Table.III.6 Losses in the inverter leg

Conduction loss	Charging + Switching loss	Estimated loss of gate driver
≈ 4.5 mW	≈ 4.3 mW	≈ 1.25 mW

As we can see in the schematic of the inverter leg (Fig.III.38) we have to calculate the control circuit of these power devices  $M_N$  and  $M_P$ . In the inverter leg, if the charge time of the gate capacitance of the power transistor is too important, the switching losses would be too high. To enhance the drive of the power transistors and to ensure the best switching performances, several amplification stages have been designed [109], [110], [111] as stage AMPLI. Moreover, CMOS inverters, driven with the same gate signals for the N and P transistors, go through a short-circuit mode for a short amount of time during each switching transitions, that's why two gate drivers are designed one for each power device and a dead time between the power NMOS and PMOS.

The design of each stage starts from the largest stage: T1, T2, T3 to end with the design of T4. Indeed, this first stage is critical with respect to converter global switching losses. Oversize first amplification and driving stage would generate unnecessary additional driving losses, but if this stage is under-designed, the power transistors will switch slowly. Each next stage is designed regarding the input and output dynamics of the previous stage: T5, T6, T7 and T8.

To control the phase shift time between power NMOS and PMOS to avoid the short circuit within each inverter leg, a stage which creates a dead time between power transistors is designed. These stages with T9-T16 are not identical in order to introduce different delays for the power transistors  $M_N$  and  $M_P$ . This has been carried out realizing inverting stage with different on-state resistances for the transistors T14 and T15.

In our design of the layout, the amplification stage has been physically divided into 4 circuits to optimize for metal layer parasites and propagation delays for the gate drivers to the integrated power transistors. The buffer stage of T17-T24 ensures a sufficient current charge for the long distance of the metal connection.

Moreover, the level-shifter blocks are built up to generate the signal control for the low side channel  $0V$  to  $V_{DD}/2$  ( $0V/4.5V$ ) and the high side channel  $V_{DD}/2$  to  $V_{DD}$  ( $4.5V/9V$ ). An auxiliary power supply generates the voltage  $V_{DD}/2$  and is embedded in the H-Bridge (developed by CEA-LETI).

The details of the designs are shown in the APPENDIX A.

Fig.III.40 shows the complete layout of the H-Bridge of the SAB converter where all the parts of the amplification stages are highlighted.

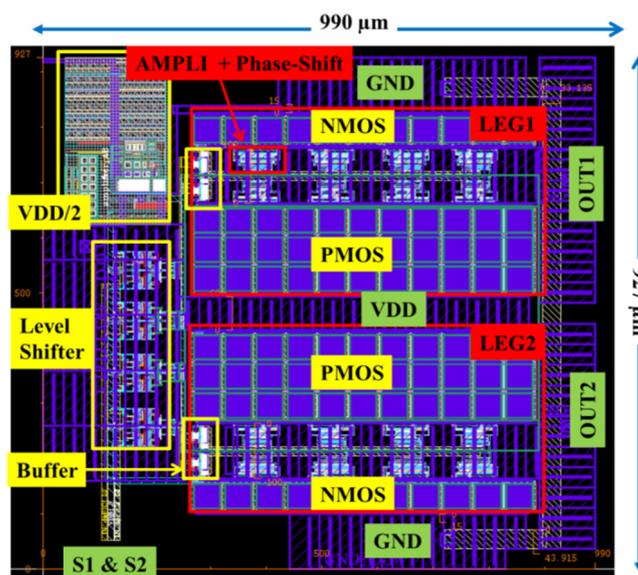


Fig.III.40 Layout of the H-bridge with gate driver  $990 \mu\text{m} \times 927 \mu\text{m}$

Fig.III.41 shows the layout of one of the 4 amplification stage for driving the NMOS device.

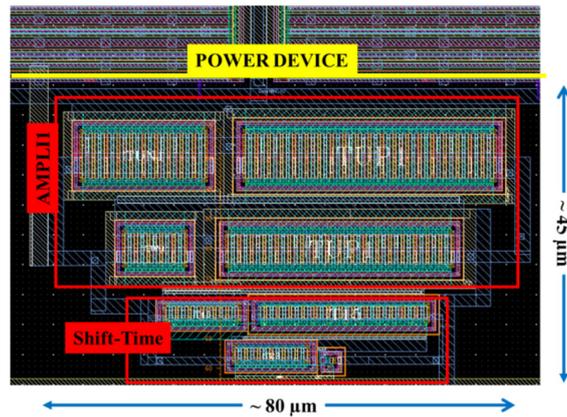


Fig.III.41 Layout of the amplification stage circuit with AMPL11 and Shift-Time blocs

### III.3.c Design the integrated rectifier

#### III.3.c-i The intrinsic-diode rectifier

In order to design the secondary side power circuit of the SAB converter, the first solution is a diode rectifier as shown in Fig.III.42. This rectifier is simple, easy to design without any control circuit.

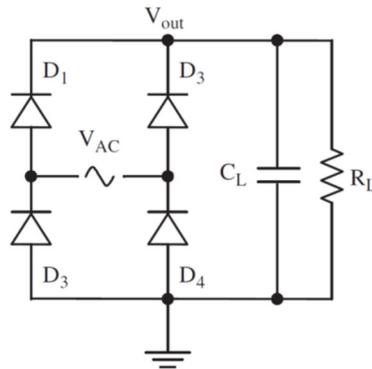


Fig.III.42 Schematic of a diode rectifier

However, a diode rectifier of 10V is not available in the selected technology XFAB XT018 technology. Using a diode of 40V with the drop-voltage of 0.667V is the solution for this diode rectifier, see Fig.III.43.

XT018 RECTIFIER DIODES					
Device	Name	Available with module	Vforward [V]	BV  [V]	Max  VCC  [V]
5V rectifier p+ /n	dfwdpa	DTI+PSUB+HVN+DNC	0.77	> 7.1	5.5
6V rectifier n+ /p	dfwdn5	DTI+PSUB	0.706	> 8	6
40V rectifier	dfwdnt	DTI+PSUB+NHVA	0.667	> 50	40
60V rectifier	dfwdnu	DTI+PSUB+NHVA	0.665	> 65	60

Fig.III.43 Options of the rectifier diodes in technology XFAB XT018

Instead of using the 40V diode rectifier of XFAB XT018, we use the 10V power transistors as the intrinsic diode (body diode) [112] by connecting the gates to the sources: Fig.III.44. This rectifier is called the intrinsic-diode rectifier.

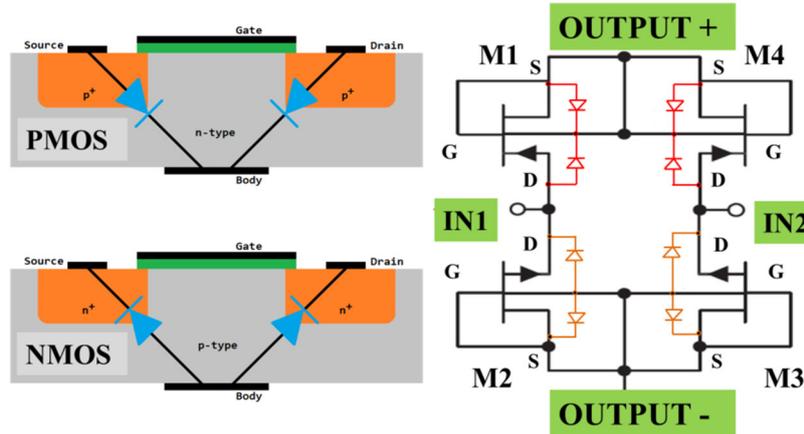


Fig.III.44 Schematic [112] [113] of the intrinsic body -diodes rectifier by connecting the gates and the sources

By using the layout of the primary circuit, removing the control and amplification stages and connecting all the gate terminals to the DC bus for PMOS and to the ground for NMOS, we have the layout of the intrinsic-diode rectifier as we can see in Fig.III.45.

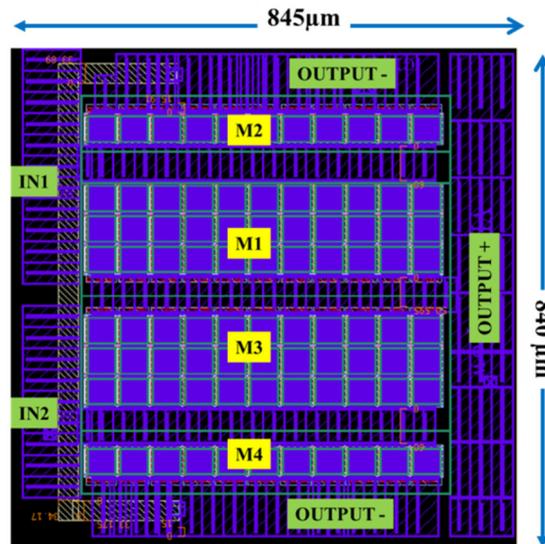


Fig.III.45 Layout of the intrinsic-body diodes rectifier in XFAB XT018, 845  $\mu\text{m}$  x 840  $\mu\text{m}$

Using an intrinsic-body diode rectifier remains an important drop-voltage on the secondary side of the SAB converter (typical 500 mV – 600 mV of a P-N diode [114]) which increases the losses in the secondary side. The synchronous rectifier is proposed as an optimized solution, known for its high efficiency; it reduces the voltage drop on the secondary circuit of the SAB converter.

Nevertheless, it is not a simple solution to be designed in this specific case since the signal coming from the secondary side of the transformer is not clear.

### III.3.c-ii The synchronous rectifier

Using a synchronous rectifier requires a control circuit for fast switching, use higher gate drive voltage conductivity (around 5V instead of 0.85V in the intrinsic-diode rectifier) for enhancing the switching speed, reduces losses thanks to almost negligible voltage drop (typically around 20 mV) in direct conduction. The synchronous rectifier uses either supplementary power supply for their active circuits.

Self-powered synchronous rectifier uses either a starting circuit or an auxiliary load path for the startup. The control circuit drives the gates of transistors to operate in synchronous rectifier mode.

In MEGaN project, the synchronous rectifiers are studied as a collaborative work with LE Thanh-Long. Several literatures [112], [115], [116], [40], [114] have been studied and reported on the different structures of the synchronous rectifier. We compared the solutions and the most suitable structure that has been selected thanks to the simplicity and reliability of the structure. This structure has two comparators driving the high side transistors and two other comparators for the low side transistors as described in [115].

In order to improve the reliability of the design, the structure is simplified for instance. The low side comparators are removed and replaced by the resistive-bridge to drive the gate-source voltages of the NMOS for the first prototype. Fig.III.46 shows the schematic of the synchronous rectifier with only two comparators for the high side transistors.

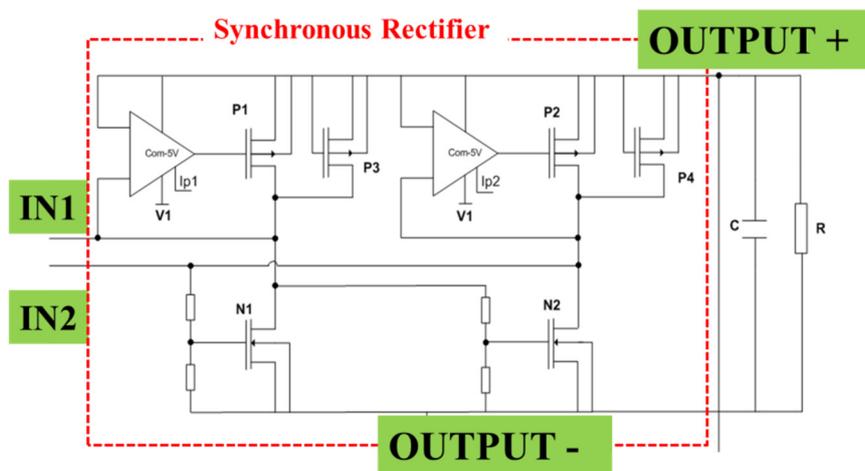


Fig.III.46 Schematic of the synchronous rectifier studied in this work

In this structure, the comparator has an important rule for the responding time of the system. When the input voltage of the synchronous rectifier is higher than its output voltage, the output signal of the comparator turns to positive and activates the power switch to enable the recharge of the output capacitor.

Conversely, when the input voltage of the synchronous rectifier is lower than the output voltage, the comparator output turns down, the switch is off and the direct conduction of the circuit is disconnected.

Two supplementary MOSFET P3 and P4 are added to aid the system during starting time. They charge the output capacitor in order to supply the comparators. Once the comparators work, transistor P1 and P2 are activated, consequently P3 and P4 are deactivated. The currents are now carried by the P1 and P2. In the design, P3 and P4 are implemented by using the parameter values of P1 and P2.

#### **PMOS (P1 & P2) and NMOS (N1 & N2)**

A synchronous rectifier is limited by the switching losses due to the associated parasitic element of the power transistors. They are usually implemented as the large transistors to achieve low conduction losses (low  $R_{ON}$ ) and deliver high output currents.

The synchronous rectifier is designed with the criteria:

- 1MHz switching frequency

### III.3 Integrated high side power supply for high temperature

- Consumption of the comparator is limited to 1mA, nominal supply voltage is 4.5V
- 200 mV voltage drop of power transistors

The voltage drop is defined due to the minimum different voltage of the comparator (200mV between V- and V+ of the comparator). This comparator is designed during the Ph.D work of LE Thanh-Long [75] and is used for design the synchronous rectifier.

Based on a desired voltage drop of 200mV and current of 55mA, we can calculate the  $R_{DS\_ON} \approx 4 \Omega$ .

When the gate voltage  $V_{GS}$  is superior to the threshold voltage  $V_{TH}$ , the transistor is in conduction. If the drop voltage on the transistor  $V_{DS}$  is inferior to the difference as  $V_{OV}$  between the VGS and VTH,  $V_{OV} = V_{GS} - V_{TH}$ , the transistor works in linear mode (resistive and unsaturated), the current  $I_{ds}$  can be calculated as:

$$I_{ds} = \frac{W}{L} \times \mu \times Cox \times \left( V_{ov} - \frac{V_{ds}}{2} \right) \times V_{ds} \quad (III.34)$$

L is the typical length of the transistor's channel - 500 $\mu$ m. Cox and  $\mu_p$  can be extracted from the datasheet of the XT018 technology.

$$Cox = 2.71 \times 10^{-3} \text{ F/m}^2 \text{ and } \mu_p = 97 \text{ cm}^2/\text{V.s}$$

Finally, the size of the PMOS is calculated to 2400 $\mu$ m.

Normally, the size of NMOS is designed 3 times smaller than PMOS due to much higher mobility of NMOS channels compared to PMOS channels. In this design, we chose identical transistor sizes  $W_{NMOS} = W_{PMOS}$  to reduce the ON-resistance of the NMOS transistor and then decrease the conduction load across the NMOS transistors of the synchronous rectifier.

Table.III.7 shows the parameters of the power transistors of the synchronous rectifier.

*Table.III.7 Parameters of the power transistors of the synchronous rectifier*

	P1, P2, P3 and P4	N1, N2
Channel Length	500 $\mu$ m	500 $\mu$ m
Channel Width	2400 $\mu$ m	2400 $\mu$ m
ON resistance	$\approx 4.5 \Omega$	$\approx 2.2 \Omega$

#### **Comparator:**

The power transistors PMOS (P1 & P2) and NMOS (N1 & N2) are 10V transistors,  $V_{DS} = 10V$ , but with the maximum gate voltage  $V_{GS\_MAX} = 5V$ . Furthermore, to limit consumption of the comparator, the 5V transistors are used to design the comparator.

A control circuit of the synchronous rectifier combines two parts: the comparator and the output buffer. An output buffer as an amplification stage is added to the output of the comparator for the gain of the signal.

A comparator combines 3 parts: pre-amplification stage, amplification stage and a buffer stage of the comparator. In fact, the pre-amplification stage and the amplification stage are built up by the differential comparison stages; the pre-amplification stage compares the V+ and V- at the input. To amplify and adapt the voltage level, an amplification stage is added.

The voltage applied at the negative terminal of the comparator comes from the transformer of the SAB converter with an amplitude ranging from -10V to 10V. In addition, the positive input is connected to  $V_{DD}$  (the rectifier output). This voltage is also the supply voltage of the comparator.

For instance, the comparator is designed with the current  $I_{DC} = 80 \mu A$  as a compromise between the responding time and the energy consumption of the comparator. A resistor is added in order to limit the current between the substrate of PMOS and  $V_{DD}$  ( $I_{BD}$ ). By the simulation in CADENCE, the value of the resistance is fixed at 100 k $\Omega$ .

Fig.III.47 shows a principal schematic of the comparator. The detail of the mirror current is presented in Appendix B.

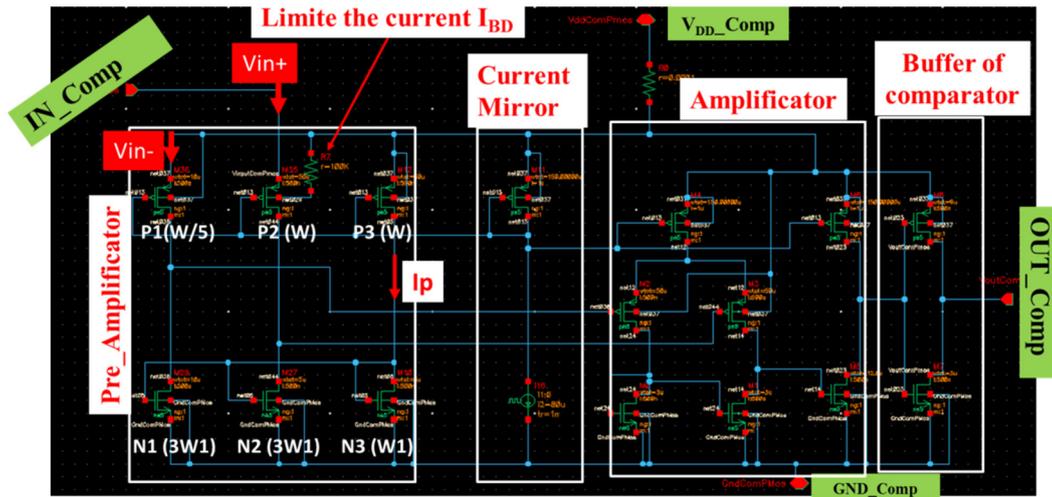


Fig.III.47 CADENCE schematic circuit of a PMOS comparator with its stages

In G2ELab, during his Ph.D, LE Thanh-Long [75] has developed a 5V comparator for his optical gate driver with the current mirror stage, amplification stage and buffer stage of the comparator. Moreover, the pre-amplification stage of high speed comparator was also studied and designed by Hynek Raisigel [118]. These designs are taken over to the design of the comparator of this synchronous rectifier.

The designs for our specific application are presented in the APPENDIX B.

**Layout of the synchronous rectifier**

Fig.II.48 depicts the layout of the synchronous rectifier in the XFAB XT018 technology.

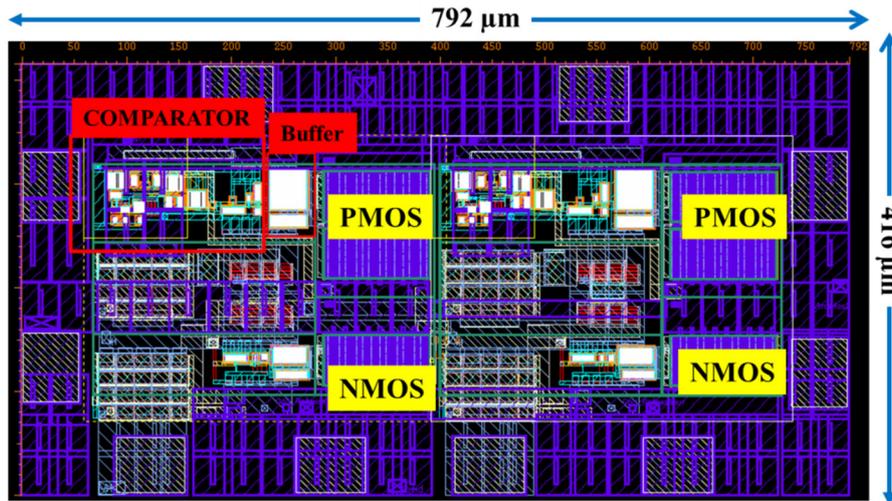


Fig.III.48 Layout of the synchronous rectifier, 792  $\mu\text{m}$  x 416 $\mu\text{m}$

The size of the synchronous rectifier (792  $\mu\text{m}$  x 416 $\mu\text{m}$ ) is smaller than the size of the intrinsic-diode rectifier (845  $\mu\text{m}$  x 840  $\mu\text{m}$ ) in Fig.III.44 due to the different size of the power transistors. Table III.8 shows the synthesis of the primary side and the secondary side of the SAB converter in the technology XFAB XT018.

Table.III.8 The sizes of the primary circuit (H-Bridge) and the secondary circuit (rectifier) of the SAB converter

H-Bridge	Intrinsic-diode rectifier	Synchronous rectifier
990 $\mu\text{m}$ x 927 $\mu\text{m}$ $\approx 0.92 \text{ mm}^2$	845 $\mu\text{m}$ x 840 $\mu\text{m}$ $\approx 0.71 \text{ mm}^2$	792 $\mu\text{m}$ x 416 $\mu\text{m}$ $\approx 0.33 \text{ mm}^2$

To compare the theoretical efficiency of the SAB converter with its rectifier, a schematic has been made by using a transformer equivalent model in CANDENCE with three different rectifier solutions:

- Synchronous rectifier as Fig.III.41
- Intrinsic-Diode Rectifier as Fig.III.39
- Intrinsic-Diode Rectifier with small size of the power transistor as the synchronous rectifier

The theoretical efficiencies of the three different cases are studied with a transformer model where the serial resistor of the transformer is estimated to 5 $\Omega$ .

Losses include those produced by the primary and secondary active circuits and those from the transformer. As we can see and as it could be expected, using a synchronous rectifier is the best choice for the efficiency of the SAB converter but its design is quite complex and its operation at high switching frequencies remains a challenge. Table.III.9 describes three rectifiers which are used in the studies of the theoretical efficiencies.

Table.III.9 Three cases of the efficiencies

Case 1	Small intrinsic-diode rectifier	WP = WN = 2.4mm
Case 2	Large intrinsic-diode rectifier	WP = 33mm, WN = 11mm
Case 3	Synchronous rectifier	WP = WN = 2.4mm

As expected, the use of the Intrinsic-Diode Rectifier with small transistors significantly reduces the power supply efficiency. The implementation of a larger intrinsic-diode rectifier improves the efficiency as the 2<sup>nd</sup> case in Fig.III.49 although; the larger transistor surface may induce extra costs.

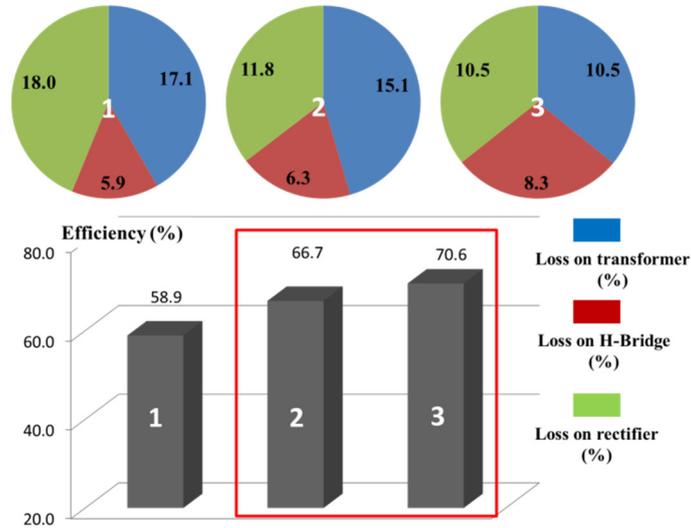


Fig.III.49 Comparison of the efficiencies and the losses' distributions of the SAB converter with three different rectifiers (case 1, case 2 and case 3)

In order to maximize successful operation within the MEGaN project, the two best solutions have been implemented in the integrated gate driver ICs.

#### III.3.d Characterization of the active part of the SAB converter

At the time of finishing this PhD dissertation, the designs of the active parts of the SAB converter are assembled in the gate driver IC by our partner IDMOS and the dedicated run is about to be launched for manufacturing (October 2016). In parallel, several test-chips have been designed in order to verify the function of the blocks and to investigate the maximum working temperature. In addition, a first MPW (Multi Project Wafer) prototype was manufactured to qualify components and functional blocs.

The first test-chip of the power supply has been designed and characterized in G2ELab; this is an inverter leg with its amplification stage circuitry. Fig.III.50 shows a set-up for tests with high temperature up to 175°C. The hot plat is used to heat the circuit; we stabilized the temperature around the circuit above the hot-plate by using a heating cover.

The test-chip prototype is tested on an IMS (Insulated Metal Substrates) for the high temperature purpose. The temperature increases from the ambient temperature from 25°C to 175°C.

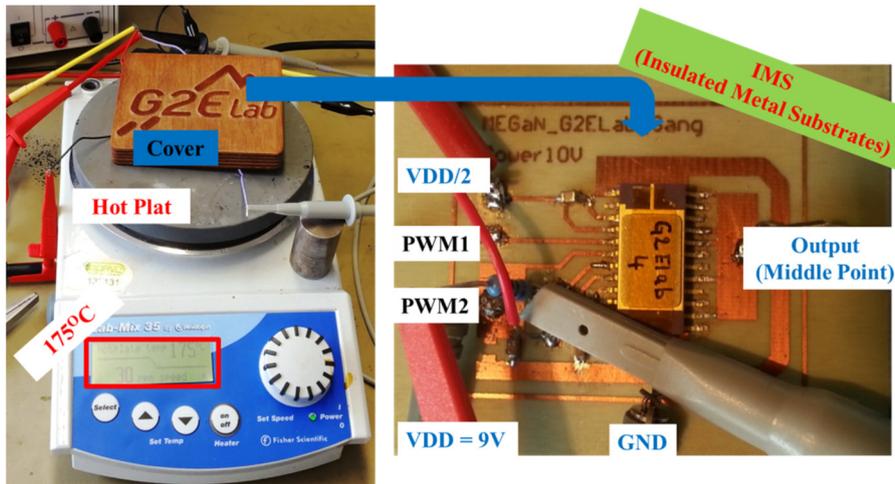


Fig.III.50 Test chip XFAB XT018 under high temperature tests

Fig.III.51 shows the schematic of the inverter leg and the picture of the integrated circuit with wire-bondings in the packaging SOIC-24.

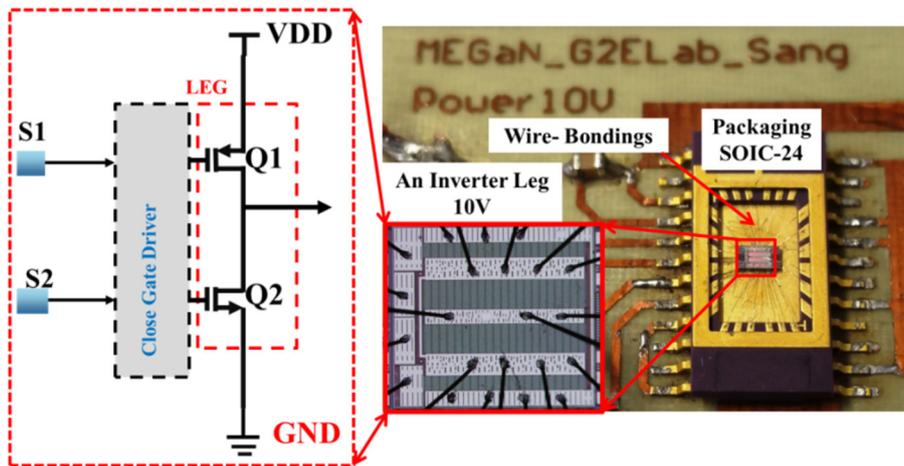


Fig.III.51 Test-chip - an inverter leg 10: schematic and pictures

The experimental results of the output voltage signal at 175°C are shown in the Fig.III.52. PWM1 and PWM2 are the control signals for the integrated level shifter of the inverter leg.

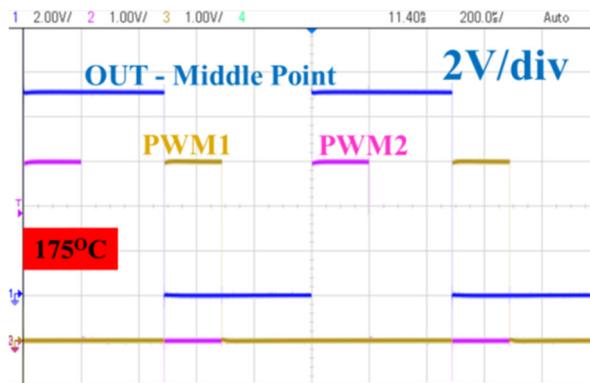


Fig.III.52 Output signal of the inverter leg with the control signals

III.3 Integrated high side power supply for high temperature

The delay times of 15ns are also observed during the rise time and the fall time of the output voltage: Fig.III.53. During the starting time, this delay time is important while the delay of the power supply is a part of the propagation delay of the gate driver circuit.

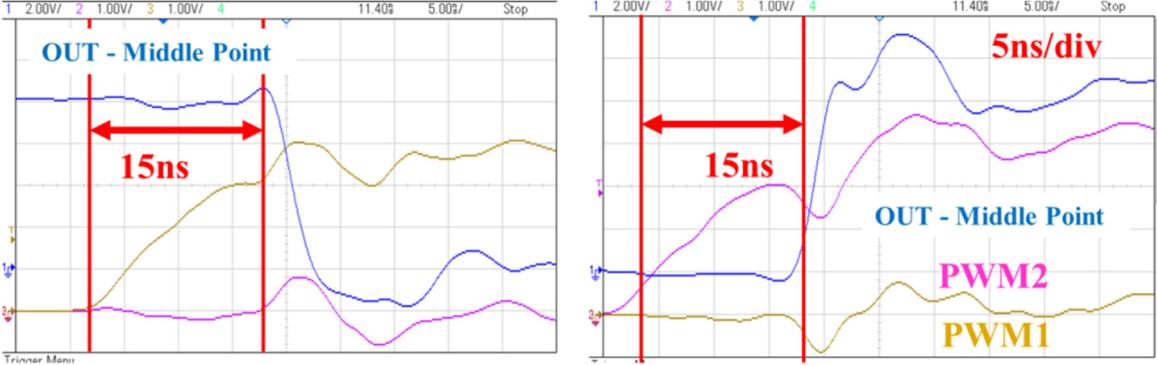


Fig.III.53 Delay times during rise time and fall time of the output voltage

The experiments confirm the high working temperature of the selected integrated technology XFAB. Using of the current set-up, the inverter leg is characterized at the maximum temperature of 175°C.

For a complete H-bridge, two identical inverter legs are used. Then the H-Bridge will be implemented with a HT-HF transformer and an integrated rectifier for the SAB converter of the gate driver circuit.

The characterizations of the H-Bridge, the rectifiers and the SAB converter will be deployed after the manufacturing of the ASICs (in 2017).

#### **III.4 Isolated signal transfer unit for very high switching speed and high temperature power devices**

This section presents developments and prototyping characterizations of a dedicated low side - high side isolated signal transfer unit based on the constraints introduced by WBG power device operating conditions. Designs take into account temperature, propagation delay deviation and high dv/dt susceptibility to deliver a generic solution able to comply with the constraints of new power devices implementations.

As we mentioned in the high side power supply of the gate driver, there are two identical ASICs for low side and high side of the gate driver circuit, both of them integrating a first stage and a secondary stage. It is important to separate the two parts on two different substrates in order to minimize capacitive coupling and to guaranty the isolation between the two parts. As a result, this integration gives us the opportunity to implement a bidirectional isolated signal transfer unit. This may be used to help in synchronizing inverter leg transistors signals.

- The primary circuit of the isolated signal transfer unit is on the low side ASIC
- The secondary circuit of the isolated signal transfer unit is located on the high side ASIC
- The isolator component of the signal transfer unit is an internal integrated circuit which is located either on the primary side or secondary side.

For the packaging, the wire-bonding could be used to interconnect the low side to the high side of the isolated control signal transfer unit.

##### **III.4.a Approach towards the integrated circuit complying with application constraints**

Three technologies are candidates for the high side gate driver signal transfer in harsh environment, integrated into a silicon chip:

- The current source level shifter [49], [48] is physically limited to the voltage ratings of the technology (200V in XFAB XT018). The maximum performing temperature of this level shifter will be investigated. Its pulsed operation is able to maintain a low power consumption, while keeping duty cycle deviation very low. However, this technique does not provide galvanic isolation.
- Coreless magnetic couplers [119], [120] integrated on silicon with modulator and demodulator are designed and optimized at best for high dv/dt immunity. They show suitable operation but introduce a more significant susceptibility to dv/dt due to its large capacitive coupling. In this signal transfer unit, the galvanic isolation is confirmed by the selected integrated technology up to 5.2kV.
- The last technique, via optical isolation [75], is promising for outstanding dv/dt immunity. Our approach is based on fiber optic light transmission to an optical receiver integrated directly into the gate driver CMOS chip. If the technique exhibits very promising performances, packaging issues remains relevant problems, especially when several power transistors are driven by light, each gate driver requiring one dedicated optical fiber. The spectral responsivity of different integrated detectors shows good photonic conversion, very high immunity and low duty cycle deviation.

Depending on the requirements of the system; the most suitable gate driver technique with its signal transfer technique can be selected. The coreless solution has been studied and prototyped using high temperature qualified SOI XT018 technology from XFAB within this Ph.D work for the MEGaN project.

Fig.III.54 shows the isolated signal transfer unit implementation as the parts of the gate driver with coreless transformer into the low side high side gate driver circuitry.

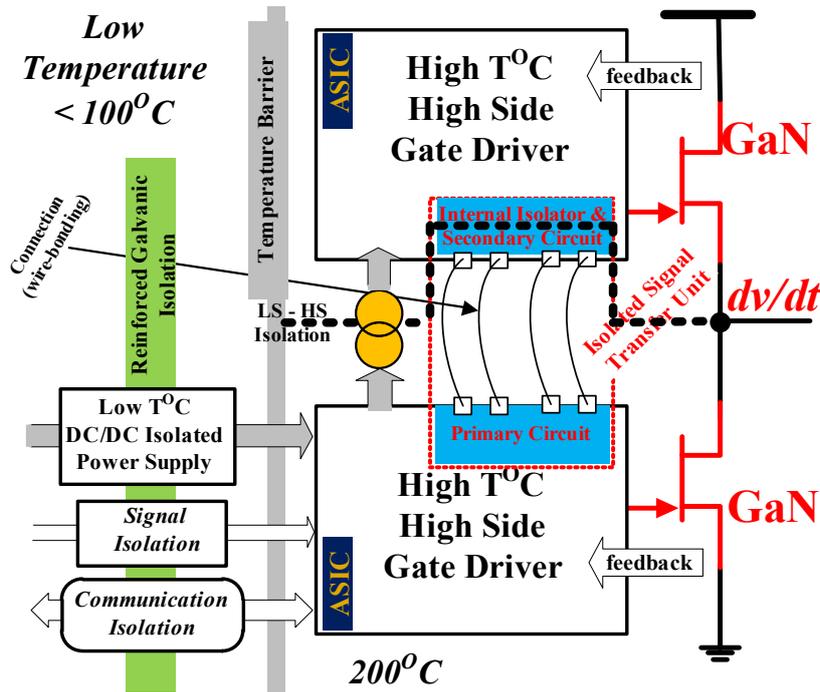


Fig.III.54 Gate driver architecture with the signal transfer unit as the gate driver by using coreless transformer

### III.4.b Integration approach of the isolated signal transfer unit

#### III.4.b-i Integrated coreless transformer

These characterizations continue the PhD work of TO Ngoc-Duc [49]:

- The designs in XFAB XT018 PDK have been completed during his thesis
- The prototypes of the driver with coreless transformers are packaged, characterized and used lately as a part of my work to isolate the signal transfer unit for the proposed gate driver circuitry.

Fig.III.55 shows a block diagram of the signal transmission function with the coreless transformer. This function consists of 4 parts: the control circuit in the primary side, coreless transformer, the demodulator and the output buffer in the secondary side.

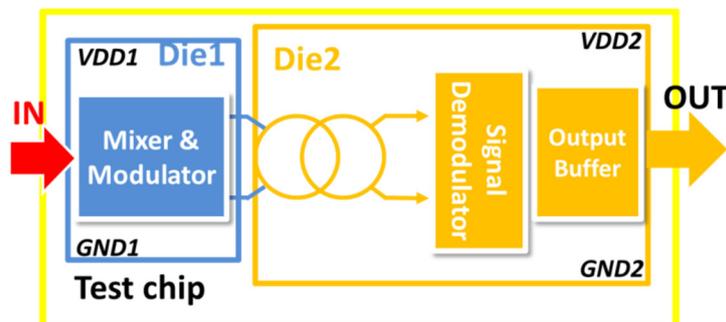


Fig.III.55. Schematic of the coreless gate driver signal transfer unit

The elements of each circuit are presented as follows: the primary circuit consists of a mixer and an integrated modulator. In a first test-chip, the primary driver is supplied by a square wave PWM ( $V_{DD1}$ ) modulated by a high frequency carrier by the modulation integrated circuit.

The integrated transformer provides galvanic isolation between the primary and the secondary. The secondary winding is beneath the primary winding: Fig.III.55.

The secondary circuit is integrated in a second chip to reduce the parasitic capacitances of the substrate, to hold the breakdown voltage between the two parts of the circuit.

The secondary circuit consists of a peak detector associated with a fast comparator and a current amplification stage which controls the power component. Both chips are interconnected via two wire-bonding as shown in Fig.III.56 (N.ROUGER2016). Two different reference potentials GND1 and GND2 correspond to two power supplies and they are isolated.

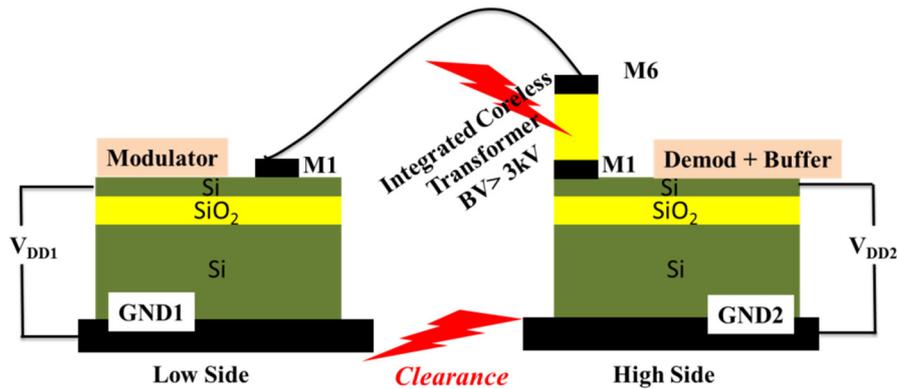


Fig.III.56. Low side – high side ICs [121]

The optical microscope photo of the XFAB XT018 chip is presented in Fig.III.57. For instance, the prototype on a single die has been implemented which means the primary side, the coreless transformer and the secondary side are on the same die.

The current works toward a prototype with two sides in two different dies are undergoing.

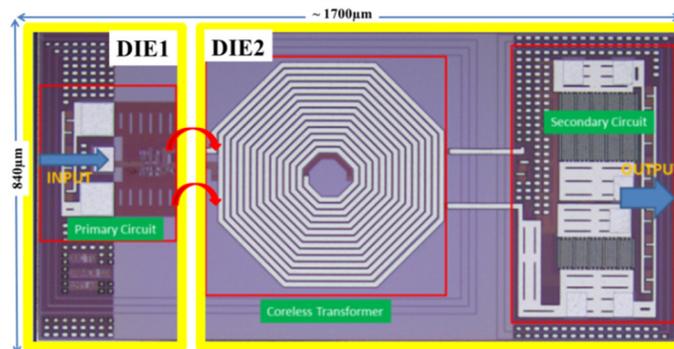


Fig.III.57 Microscope photo of XFAB XT018 gate signal transfer unit with coreless transformer

A high temperature set-up is shown in Fig.III.58, where the hot-plate and the heat-cover are used. The maximum temperature during the tests is 200°C. Fig.III.59 demonstrates the output voltage of the coreless transformer for the working frequency of 1 MHz, 1nF of charge is placed on the output of the gate driver.

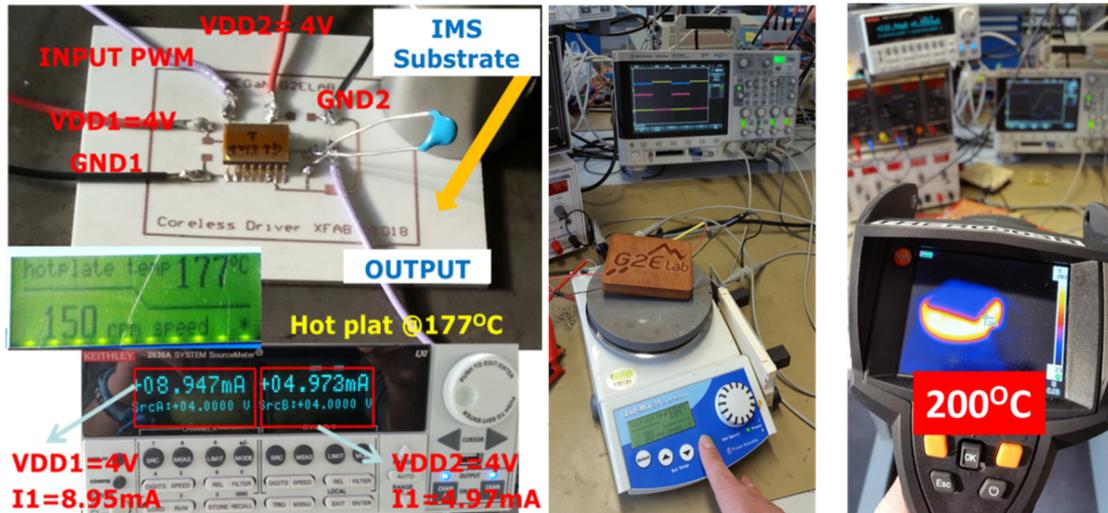


Fig.III.58 Set-up for tests at high temperatures

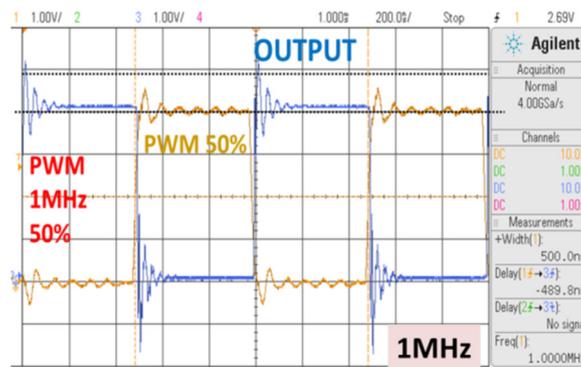


Fig.III.59 Input and output signals of the gate signal transfer unit with coreless transformer at 1 MHz under 175°C

Fig.III.60 shows the voltage waveforms applied on the primary side of the coreless transformer, where the modulated frequency is 323MHz.

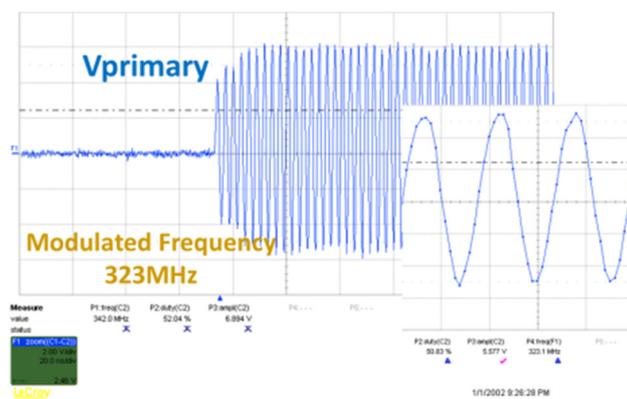


Fig.III.60 Primary voltage applied to the coreless transformer (+ Zoom of the waveform)

In Fig.III.61, the parasitic capacitance between primary side and secondary side of coreless transformer XFAB XT018 is characterized at 1.8pF at 1MHz. Primary to secondary breakdown voltage was not detected below 3kV (experimental setup limited to 3kV).

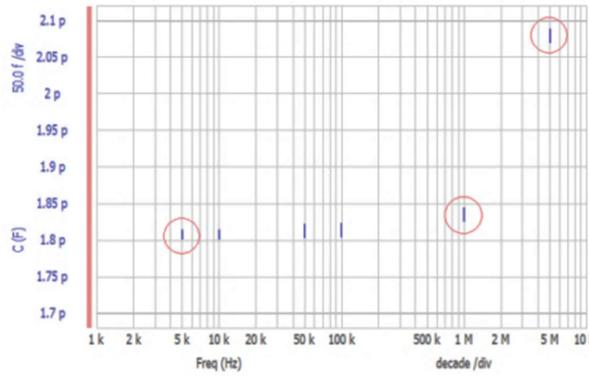


Fig.III.61 Primary-secondary windings parasitic capacitance with respect to frequency

In order to get a better characterization of the equivalent model of the elements of the integrated transformer, a characterization is performed at IMEP-LACH laboratory in Grenoble, where characterization platform are made available, allowing measurement in differential mode (GSSG) in the radio frequency range of 70MHz to 20GHz. Fig.III.61 shows a test transformer dedicated to the characterization under tips, and Fig.III.62 the value of S parameters measured at room temperature. Fig.III.63 demonstrates the proper operation of the transformer, especially a resonance in S21 at 650MHz.

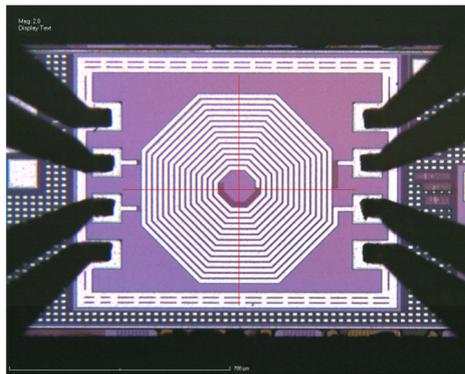


Fig.III.62 Microscope picture of the transformer under tips for the S-parameters characterisations (70MHz to 20GHz)

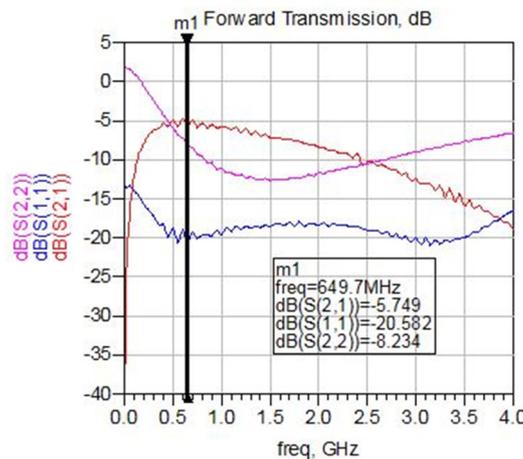


Fig.III.63. Measurement of S-parameters of the transformer

In Fig.III.64 is depicted the evolution of the propagation delays of the signal transmission function with respect to temperatures up to 200°C. This characterization confirmed that the maximum operating frequency is around 200°C. Due to the variations of the resistors inside the detection circuit with respect to temperature, the propagation delay high-to-low (H-T-L) increases significantly at high temperatures. It corresponds to the discharging period of the capacitor into the resistor of the detection circuit. Clearly, this limitation will have to be addressed in the future to raise the interest of this technique for very high switching frequencies where duty cycle is in the range of tens or hundreds nanoseconds.

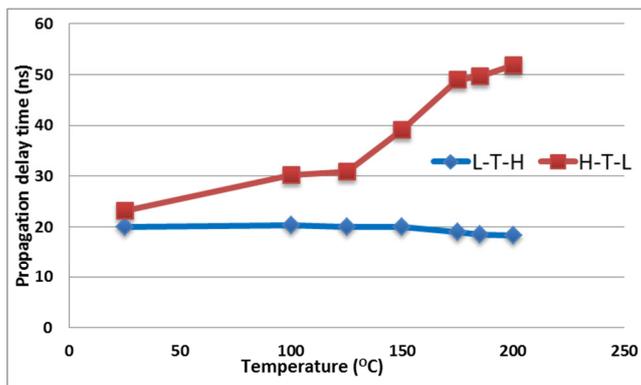


Fig.III.64 Propagation delay evolution of the coreless signal transmission unit as a function of the operating temperature

A 100V square wave disturbance source with a  $dv/dt$  of 25V/ns has been applied between the primary and the secondary side of the transfer signal unit. In Fig.III.65-a, the measured signal at the output of the coreless driver is presented. In the first figure, the driver is powered but without signal on its primary side. An important disturbance can be observed due to the circulating parasitic currents through the transformer. When the input signal is applied to the primary circuitry, the measured output signal is shown in Fig.III.65-b. Obviously, the disturbances produced by the external square wave are not removed but it can be seen that the integrity of the driver signal is remained as shown in Fig.III.65-b.

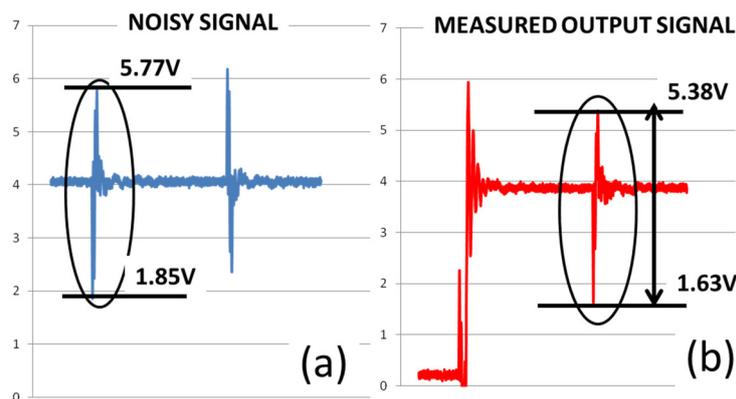


Fig.III.65 Output signals with  $dv/dt$ : a) No input signal, noisy signal at output; b) With input signal, measured output signal including the noise

In this transformer design, there is a large input-output parasitic capacitance because the modulator, the demodulator and the transformer are all located in a single die. As a result, there is a large parasitic capacitive coupling through the common substrate. Separate the primary and the secondary sides on different dies would reduce this parasitic capacitance. Fig.III.66 and Fig.III.67 show the microscope

### III.4 Isolated signal transfer unit for very high switching speed and high temperature power devices

pictures of two prototypes and their input-output parasitic capacitance. As we can see in Fig.III.67, the parasitic capacitance is reduced 10 times from 28.2 pF to 2.85 pF at 1 MHz.

With new prototype with two separated dies, the perturbation through the substrate is reduced then the  $dv/dt$  immunity is improved. Further characterizations will be provided up to 50V/ns.

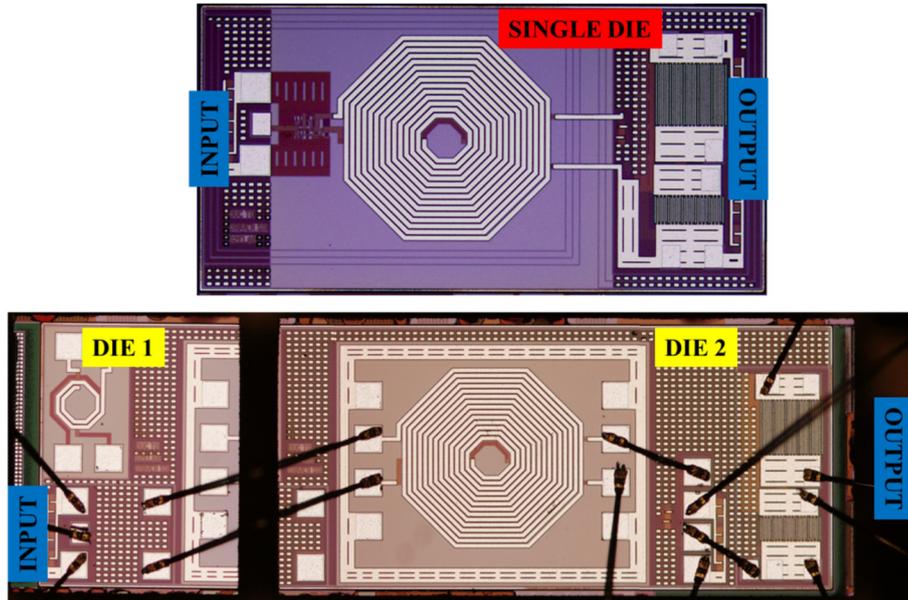


Fig.III.66 Microscope pictures of a single die prototype and a prototype with two separated dies

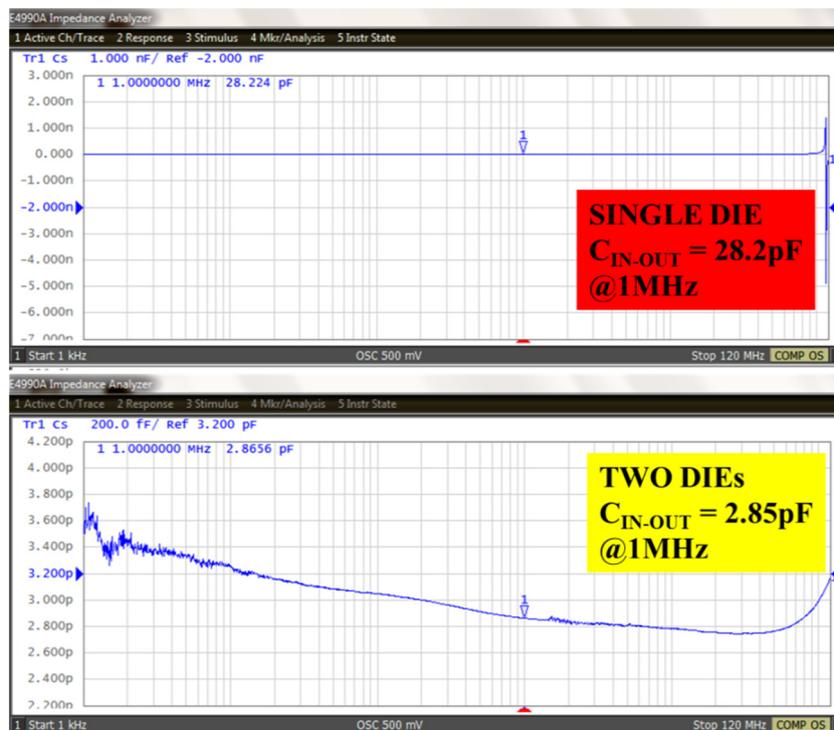


Fig.III.67 Input - output parasitic capacitance of two prototypes

**III.4.b-ii Current source level-shifter and optical transmissions**

As a part of the MEGaN project, the Power Electronics team of the G2Elab has developed two other techniques of the gate driver with a level-shifter and with an optical transmission.

- The Ph.D work of Farshid SARRAFIN was devoted in developing a gate driver with an integrated current source level shifter in XFAB XT018.

- In the thesis of LE Thanh-Long [75], an approach based on the integration of an optical gate driver is implemented in integrated technology XFAB XT018.

The detailed works are presented in APPENDIX 3.

**III.4.c Comparison between the three techniques**

According to our works [121], [122] (see APPENDIX C), the comparison results of the three different integrated techniques of the signal transfer units are shown in Table.III.10.

*Table.III.10 Comparison 3 integrated assessment of drivers*

	<b>Driver with coreless transformer</b>		<b>Driver with current source level-shifter</b>		<b>Driver with optical transmission</b>	
	25°C	200°C	25°C	200°C	25°C	175°C
<b><i>dV/dt max</i></b>	25 V/ns	-	5 V/ns	characterizing	characterizing	
<b><i>Delay LTH</i></b>	20ns	19ns	16.5ns	17.4ns	13.8ns	15ns
<b><i>Delay HTL</i></b>	22ns	51ns	16.6ns	18.1ns	18.5ns*	22ns*
<b><i>Consumption</i></b>	41.2 mW	46.9 mW	2 mW	3 mW	4mW (+5mW)**	characterizing

(\* not counting the additional propagation delay of the optical transmitter, \*\* the estimated consumption of optical transmitter)

For the consumption, the solution with the coreless transformer consumes more energy because of the high frequency modulation circuit (300 to 600MHz), 90% of the power is consumed by the high frequency modulator. The consumption of the driver with current source level shifter is the lowest. Meanwhile the consumption of the driver with integrated optical transmission is in the middle among three techniques with an estimation of the transmitter part.

The driver with the coreless transformer is tested with dv/dt up to 25V/ns which is the highest value we were able to apply. The driver with the current source level shifter has the lowest temperature dependence for the propagation delay time and for the dispersion of the control signal.

As the matter of fact, the gate driver with coreless transformer is selected as the solution of the gate driver because the optical solution is too complicated to be implemented within the gate driver circuitry and the gate driver with level-shifter does not offer satisfactory dv/dt immunity as well as satisfactory voltage operation levels (limited to 200V).

#### **III.5 Conclusions and perspectives**

At high temperature operating condition and under high  $dv/dt$  constraints, WBG devices are pushing hard efforts to develop the gate drive circuitry. This chapter has presented the design of two main elements of the gate driver circuitry: the isolated high side power supply and the isolated signal transfer unit.

The techniques of the power supply of the gate driver have been studied then an isolated DC-DC converter was selected as the most suitable topology in the context of our gate driver. The comparison of the isolated DC-DC converter topologies picked out the SAB converter as the power supply of the integrated gate driver. Then the design procedure of the active integrated circuits of the SAB converter has been presented.

This chapter also described practical characterizations of the isolated signal transfer unit. The experimental results showed for three different techniques their ability to operate at temperatures up to 200°C while offering fairly good propagation delays deviations and for some of them a good immunity to  $dv/dt$ . Mirror current pulsed level shifters have minimum propagation delays deviations but are limited in terms of  $dv/dt$  immunity as well as operating voltages. Coreless driver presents the best compromise with fairly good propagation delay deviation, correct  $dv/dt$  immunity and high operating voltage capabilities. Optical technique remains the technique expected to be the most immune to  $dv/dt$  with satisfactory power consumption but remains also more complex to be implemented.

In the next chapter, as a synthesis of MEGaN project, Work Package 3 on integrated drivers, an integrated gate driver will be introduced and depicted. Its design and implementation, partially based on the work presented in this PhD thesis, will be presented. Until now, the layout of the full integrated gate driver is prepared by our working group.



## **Chapter IV**

### **Implement An Integrated Gate Driver**

#### **Work Package 3 – MEGaN Project**

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## Abstract

*In this final chapter, the implementation of the proposed gate driver circuitry is presented. G2ELab team participates in MEGaN project where these works are conducted as WP3 (Work Package 3) dedicated to the design and the prototyping of an integrated gate driver adapted to new constraints of GaN components.*

*The general ambitions of WP3 are to improve the efficiency of system by driving optimally; while increasing the switching frequency of GaN based power devices in order to reduce the values and sizes of passive components; to operate at higher working temperature for reducing the cooling system and then to maximize the integration for gaining in terms of volume and performance.*

*Finally, the objective of WP3 is to implement an integrated gate driver circuit for a low side – high side configuration of MEGaN's power devices thus allowing this gate driver to perform with strong  $dv/dt$  under high temperature operation. As discussed in the previous chapters, focus is pointed toward the gate driver circuitry, its supplies, and its control signal units in the objective to handle the very strong  $dv/dt$  environment produced by GaN based switching cells.*

## IV.1 Generic Blocks of Gate Driver

### IV.1.a Gate Driver Tasks

Chapter I and II demonstrated that the conducted EMI perturbations related to driver circuit for the high speed power devices as the WBG devices may be significantly reduced acting on the architecture of the gate driver circuitry. Chapter III outlined another aspect working this time on the reduction of the propagation paths, reducing the parasitic capacitances in the gate driver circuitry. To overcome these problems, this Ph.D work proposed the improvements at the system level and at the component level.

By working at the system level, new gate driver architecture adapted to high CMTI is presented, reduces the perturbations on the remote control circuit.

Then at the component level of the gate driver circuitry, the new ASICs are suitable for high operating temperature which is made possible by the use of WBG power devices for the switching cells. Whereas, working at component level can decrease the parasitic values of the gate driver circuit.

These problems have been executed step-by-step and side-by-side by all four partners of WP3:

- ID-MOS: participates as the leader of WP3, an expert of numeric design and characterization of high temperature integrated technologies. ID-MOS implements the logical blocks of the gate driver and gathers all the function layouts of the partners to produce the final prototypes.
- CEA-LETI: Co-leader of WP3 is expert in industrial transfer, integrated circuit design and drivers for power components. CEA-LETI designs the functions for the programmable buffers, the monitoring blocks and the programmable regulators.
- AMPERE: an academic laboratory is expert in WBG power components and high temperature implementation. AMPERE laboratory participates in WP3 to characterize and implement a high temperature high frequency transformer as the isolator of the gate driver's power supply.
- G2ELab: an academic laboratory is expert in integrated and functional integration for the gate driver. Our group participates in the design effort at the system level for the concept of the gate driver architecture (Chapter II); and then designs, characterizes and implements the functions of the isolated power supply and the isolated signal transfer units (Chapter III).

All the functions are lastly gathered and assembled for a complete ASIC by ID-MOS.

This chapter shows firstly the specifications and the configuration of the gate driver for a low side high side implementation. Secondly, the layout of the ASIC gate driver is presented with the main features. Finally, the implementation of the proposed gate driver architecture with the ASICs is introduced.

### IV.1.b The specifications of the gate driver

Based on the design specifications of the power device (GaN power device of MEGaN project), and according to several discussions among the various end-users within the project, the specifications for the gate driver are defined for a low side – high side implementation. One objective was to develop a gate driver, taking into account new design and functional constraints and able to answer needs from several application field sharing main specifications.

Although the gate driver specifications are set according to the power devices considered in the project, the gate driver circuitry presented in this chapter is also suitable for other WBG devices.

The driver architecture is based on two ASIC, one for the high side switch and one for the low side switch. The two ASIC are the same and can be configured to operate in a low side position and a high

side position. All gate driver circuitry is integrated into the ASIC, leaving external passive components such as decoupling capacitors and the HF-HT transformer for the low side high side supply.

An external gate driver supplies the low side driver with reinforce isolation. The high side gate driver is supplied through the low side gate driver.

In a similar manner, the gate driver control signals for the low side and the high side drivers are sent to the low side gate driver.

In general, the most important specifications are:

#### **Input control signals of the gate driver (External to Low Side)**

- Reinforced isolation from the external circuit (remote control circuit) to the closed gate driver: 2.5 kVAC, with the low temperature technology. (High bandwidth digital communication I2C)
- Control input voltage level: 1.8V (compatible to 3.3 V and 5V)
- PWM control signal for gate driver is generated into the inverter leg gate driver unit. Its value is transferred through a numerical interface and refresh every 10 $\mu$ sec (Feedback status HS / LS and LS / external circuit in less than 10 $\mu$ sec)
- A synchronization signal is used to tackle the edges of the gate driver signal among inverter arms.
- Synchronization frequency: 1 kHz to 100 kHz ( $f_{\text{SYNC}}$ )

#### **Protection**

- Input control signals are well isolated
- Protection Under/Over-Voltage with active sink for low side and high side
- Short-circuit detection (desaturation observation)
- Active Miller clamping
- Reflex protection: sink active within 100nsec

#### **Power Supply**

- High side isolated power supply is based on a hybrid integration approach: primary and secondary active parts are integrated; the HF-HT transformer is implemented closely to the dies. The desirable primary-secondary parasitic capacitance of HF-HT transformer is about 5pF. (86pF of the commercial power supply in Chapter II is not suitable in this case)
- Isolation LS-HS: > 1kV (Isolation LS- Remote control: >2,5kV)
- Nominal input / output voltage of power supply: 9V / 9V

#### **Gate driver buffer:**

- Two separated outputs for source and sink independent operation and settings
- Variable and configurable gate signal output voltage: from -8 to +8V with a maximum voltage difference between  $V_{\text{GS-MIN}}$  and  $V_{\text{GS-MAX}}$  equal to 8V (from 4V to 8V)
- Source and Sink max current: 5A
- Internal resistances of source and sink (independently adjustable): 0,05  $\Omega$  to 20  $\Omega$
- Two different control signals one for the low side switch and one for the high side switch

#### **Switching frequency and duty cycle**

- Switching frequency:  $f_{\text{SYNC}}$  to 1 MHz

(Synchronization frequency: 1 kHz to 100 kHz)

- Adjustable duty cycle from 0% to 100% (complementary or active sink)

### **Packaging**

- Interconnection by wire-bonding technology for instance, flip-chip technology for the perspective
- Parasitic inductance for an IN/OUT: 2nH
- Consider to place the gate driver within the power module (high temperature environment)
- No consideration of either vibration or humidity aspects

### **Performance**

- Propagation delay ON/OFF: 10 - 30nsec
- Mismatch between LS – HS: 5nsec
- CMTI: 50V/ns (perspective in short-term 100V/ns)
- Working temperature: -40°C to 200°C

#### **IV.1.c Configuration of the generic integrated blocks**

To ease the implementations of the isolation between the low side and the high side gate driver units, two separate dies / ASICs must be used to avoid any coupling through a common substrate.

The low side ASIC includes the buffer, the monitoring circuit for the feedback from the low side power device, the level-shifter of the low side control signal, the logical blocks for generating locally the internal control signals (duty cycles), the regulators for various voltage levels sources and references and also the numerical communication interface from the remote control circuit to the closed control circuit. Obviously, the high side ASIC has also the buffer, the monitoring circuit, the regulator and the logical functions and blocks as the low side ASIC.

For the power supply from the low side to the high side, the low side ASIC contains the primary side of the SAB converter as the high side power supply. The high frequency transformer of the SAB converter is located outside of the ASICs. Therefore, the high side ASIC includes the secondary circuit of the SAB converter.

For the signal transfer units, there are the transfer lines for the PWM and the lines for communication. The receivers and the transmitters locate in the low side ASIC and the high side ASIC. The control signal insulator as the coreless transformer is integrated inside the ASICs.

There are two coreless transformers in each ASIC, one is for transferring the PWM signal from the low side to the high side, another carries the communication from the high side to the low side then to the remote control circuit. The isolation level of the coreless transformer is over 3 kV.

Fig.IV.1 shows the function blocks of the gate driver in a low side – high side implementation. In this figure, as we can see in the low temperature zone, the commercial power supply and the commercial communication insulator are used for isolating the remote control circuit and the closed control circuit.

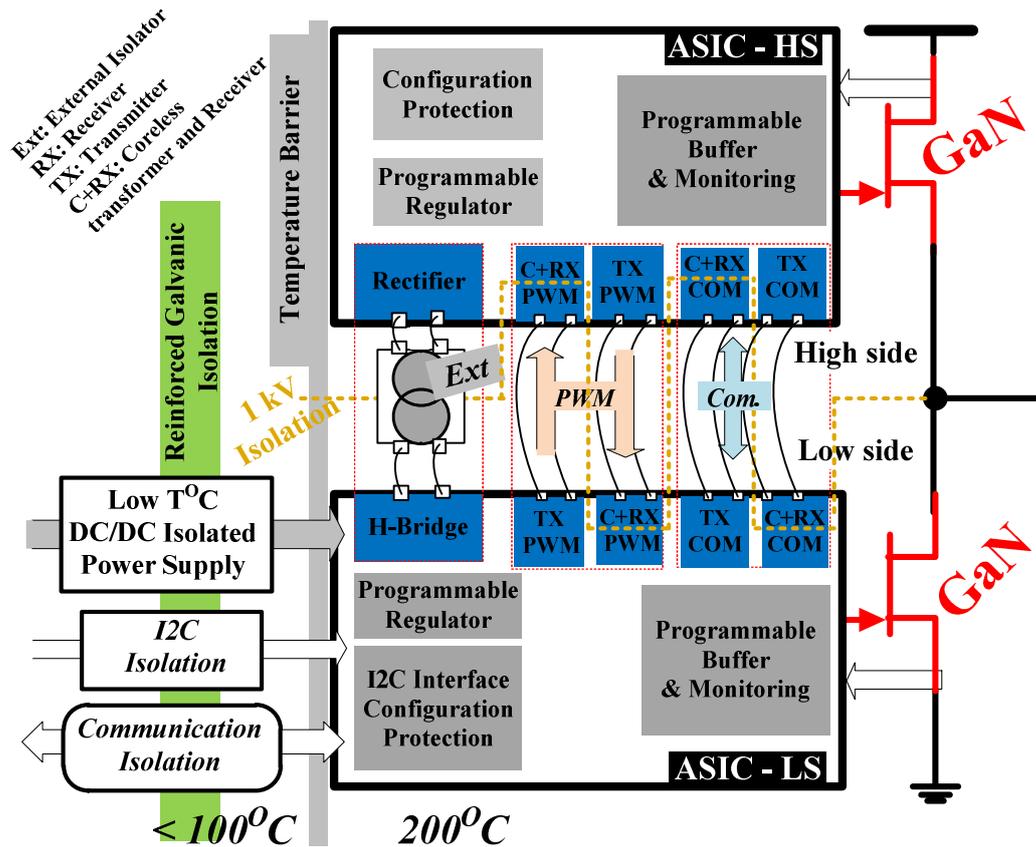


Fig.IV.1 Configuration of the block diagram for a low side-high side implementation

In this configuration, the blue function blocks are developed by G2ELab.

As we mentioned in Chapter III, the integrated gate driver is implemented very close to the WBG power devices where the temperature is critical. The ASICs are designed with a high temperature integrated technology. Therefore, the transformer of the SAB converter is expected to operate also at high temperature (HF-HT transformer).

## IV.2 Final ASIC

### IV.2.a Main features of the ASIC

The ASIC implemented in a high temperature integrated technology XFAB XT018 within the proposed gate driver architecture corresponds to the proposed final answer for the problems investigated on gate driver circuitry during the MEGaN project.

The main DC supplied voltage of the ASIC is 9V then the internal regulators step down the lower voltage (1 V to 8 V) to supply various functions.

The buffer of the gate driver is implemented with a Miller-clamp and min and max gate to source voltages can be programmed with two specific low drop regulators.

As usual, the protection functions implemented inside the ASIC are the under and over voltage of the power supply as well as the desaturation function.

The logical heart of the ASIC includes: I2C interface, PWM generator, auto-zero-skew (the final skew angle depends only on the feedback low side and feedback high side), registers for programmable blocks and the reflex protections. The propagation delay between the control signal of the remote

control circuit and the PWM signal generated by the low side ASIC is about 1 $\mu$ s. However, the propagation delay in the low side ASIC between the PWM signal generated by the logical block and the low side output signal of the gate driver is 20ns.

ID-MOS has confirmed the possible operating temperature of elementary semiconductor function in XFAB XT018 technology from -40 $^{\circ}$ C to +225 $^{\circ}$ C, allowing us to design the functions based on high temperature models.

An external transformer is required outside of the ASICs which is used for the isolator of the power supply from the low side to the high side which is defined as 1kV of the galvanic isolation in Chapter III. In another side, Chapter III confirmed that the minimum isolation of the coreless transformer of the signal transfer unit is 3kV.

If the isolation of the transformer of the power supply could be improved, the isolated level of the low side- high side power devices could also increase. As a perspective of this integrated gate driver, the WBG power devices of 3kV (SiC for example) could be implemented. In this situation, due to the existence of 3kV isolation of the coreless transformer, 3kV isolation of the HF-HT transformer of the power supply is required.

Table.IV.1 summarizes the main features of the ASIC.

*Table.IV.1 Main features of the ASIC (Source: ID-MOS)*

<b><i>Function mode</i></b>	Identical ASIC for low side and high side mode		
<b><i>Isolation signal</i></b>	2 Internal coreless transformers: <ul style="list-style-type: none"> <li>➤ 1 for PWM</li> <li>➤ 1 for communication</li> </ul>		
<b><i>Power DC-DC Isolation LS - HS</i></b>	External Power DC-DC Isolation		
<b><i>Power Supply</i></b>	Min: 9V	Nominal: 10V	Max: 11V
<b><i>Integrated regulator</i></b>	Integrated Regulators: 5V & 1.8V		
<b><i>Buffer</i></b>	Miller-Clamp & Programmable -8/+8		
<b><i>Protection</i></b>	<ul style="list-style-type: none"> <li>➤ Under-Voltage</li> <li>➤ Over-Voltage</li> <li>➤ Desaturation</li> </ul>		
<b><i>Propagation delay</i></b>	20ns (from PWM to OUT_LS)		
<b><i>Operating temperature</i></b>	Min : - 40 $^{\circ}$ C	Max : +225 $^{\circ}$ C	
<b><i>Digital Function</i></b>	<ul style="list-style-type: none"> <li>➤ I2C Control Interface</li> <li>➤ PWM Generator</li> <li>➤ Auto-zero-skew (AZS) <ul style="list-style-type: none"> <li>+/- 15ns AZS off</li> <li>+/- 5ns AZS on</li> </ul> </li> <li>➤ Fully programmable</li> <li>➤ Reflex Protections</li> </ul>		

Fig.IV.2 shows the positions of the function blocks inside an ASIC, assembled by ID-MOS:

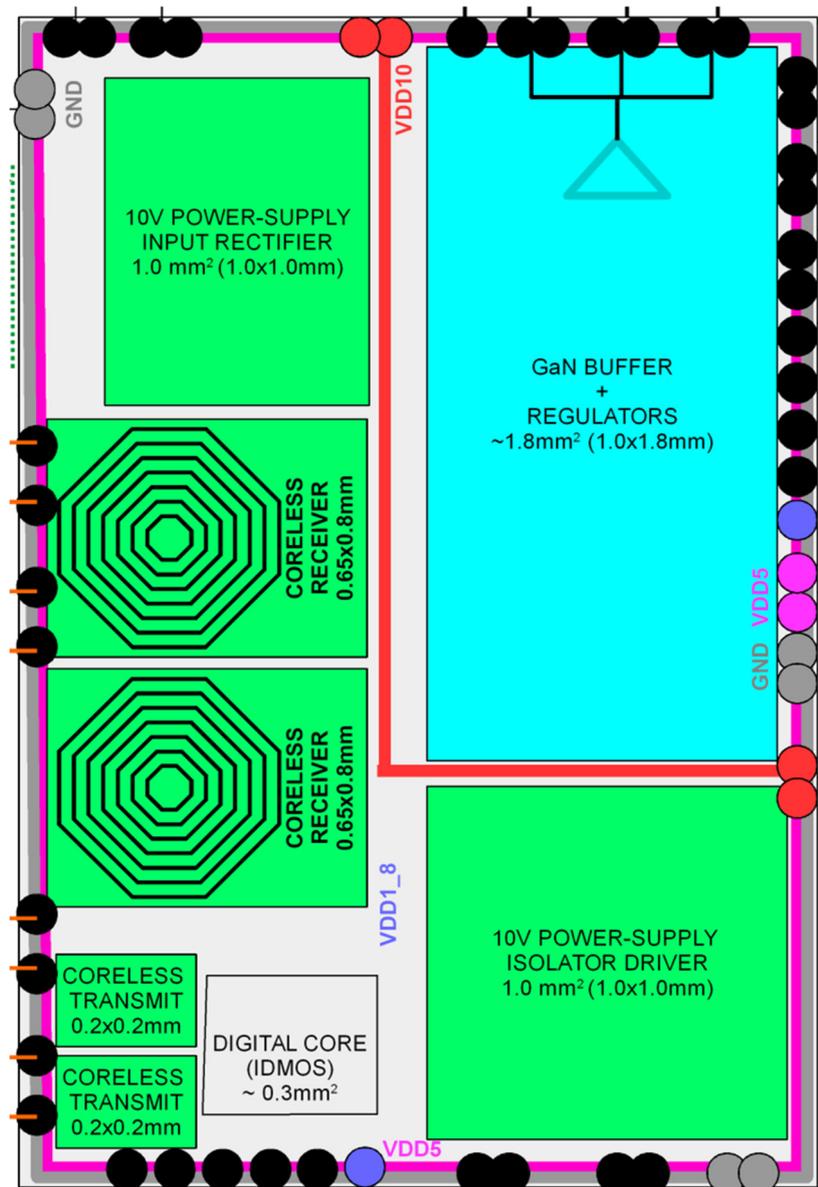


Fig.IV.2 Blocks and functions of a single ASIC (MEGaN©)

Finally, the XFAB XT018 layout of ASIC is shown in Fig.IV.3. The size of the complete integrated gate driver layout is about 2mm x 3mm (6mm<sup>2</sup>). This layout is being finalized and ready for manufacturing in the end of December 2016.

In the next section is proposed a schematic of the gate driver using two ASICs for an implementation with low side and high side GaN devices by using the proposed architecture of the gate driver.

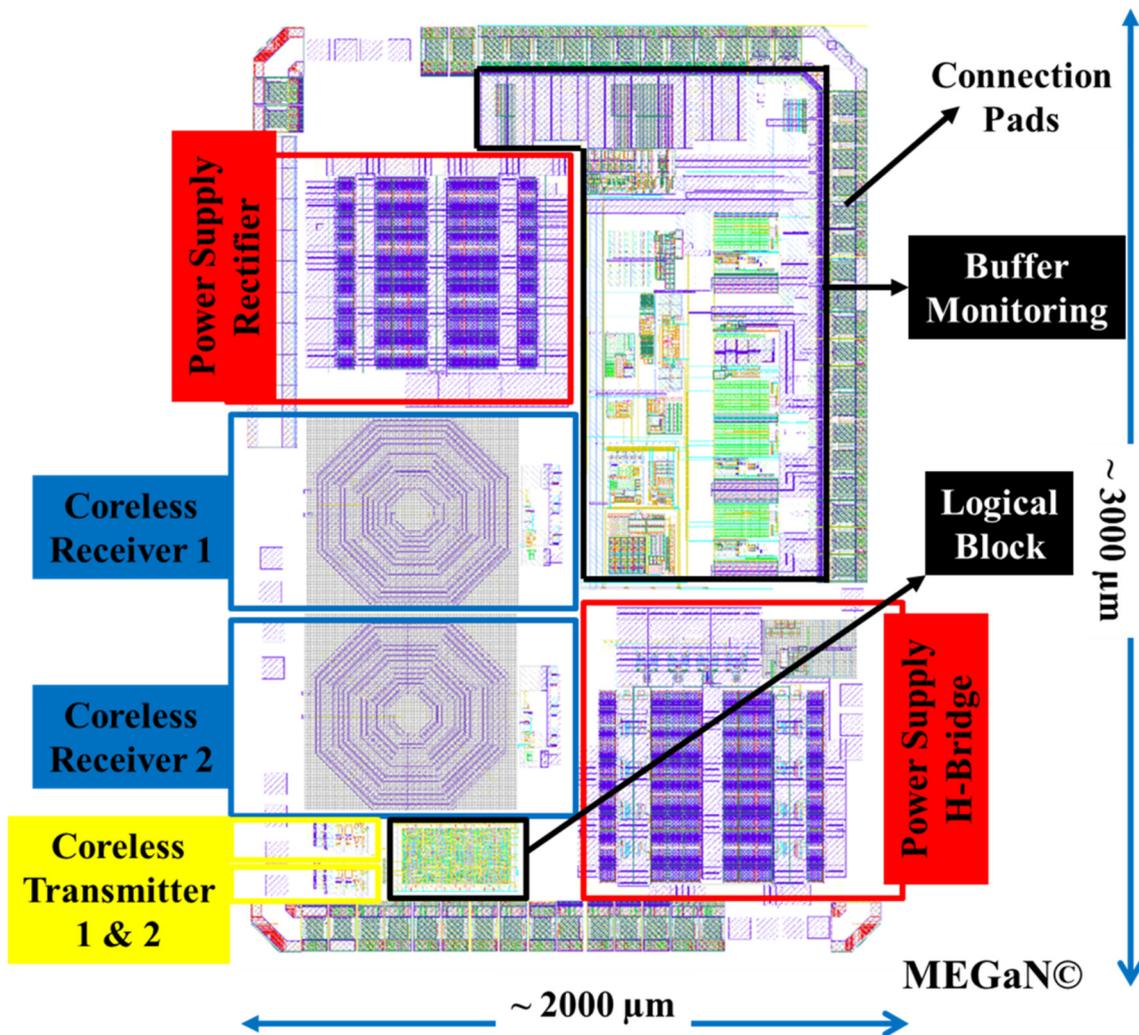


Fig.IV.3 ASIC layout in XFAB XT018,  $2 \times 3 \text{ mm}^2$  (MEGaN©)

#### IV.2.b Gate driver architecture with ASICs

In the proposed implementation of the gate driver for a low side high side power devices configuration, we need to use and implement an external high frequency and if possible high temperature transformer for the power supply of the high side gate driver, which is based on the SAB converter as developed in Chapter III. In addition, the low side ASIC and the high side ASIC are connected by using the wire-bonding technology as in Fig.IV.4. There are two inputs from the remote control circuit: an isolated power supply 10V with two terminals and an input for the entire control signal - the communication lines with 5 terminals including the I2C wires and the synchronization wire.

Several passive components are added in the implementation especially to filter and store energy at different voltage levels for the local driver supplies, the voltage reference and the programmable supplies of each gate driver buffer. High voltage desaturation diodes are also external devices since their voltage ratings were not compatible with the selected technology XFAB XT018. The gate driver output resistors can also be externally added in the case that the programmable buffers do not provide enough freedom.

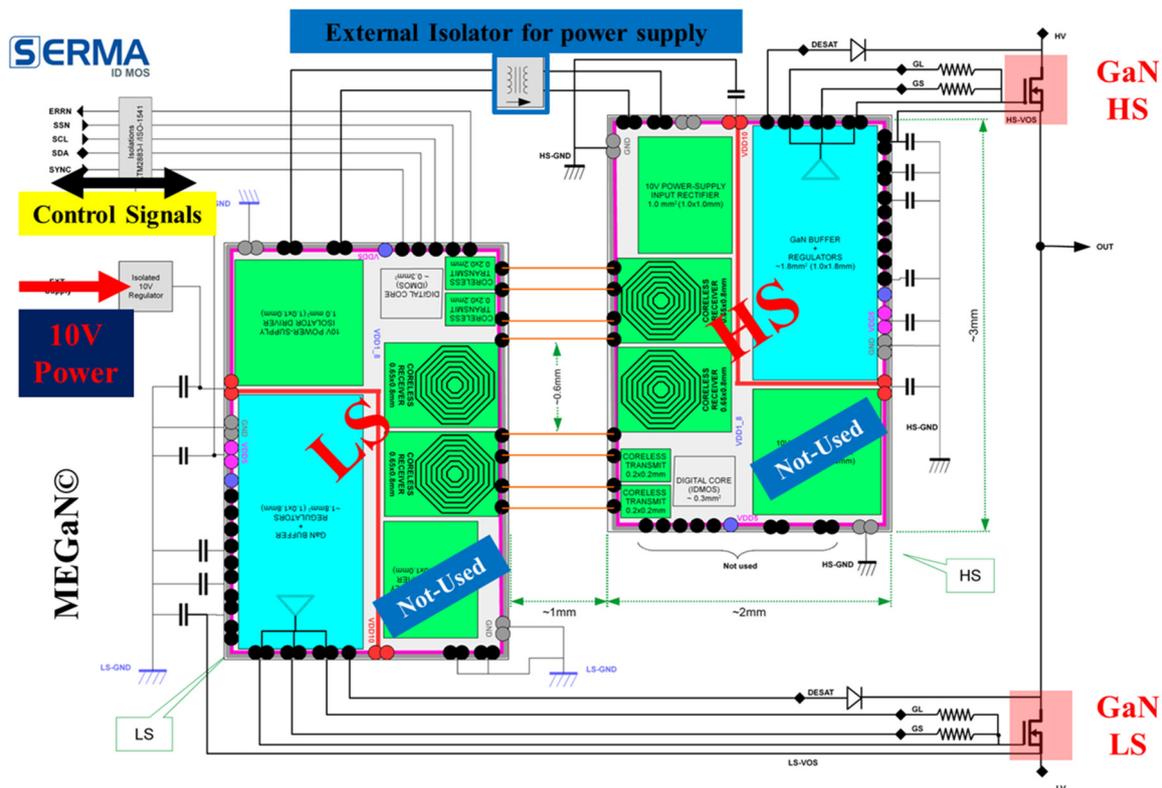


Fig.IV.4 Schematic of the proposed gate driver (MEGaN©)

### TOWARDS THE CHARACTERIZATIONS OF THE MEGaN GATE DRIVER

The characterizations of the integrated gate driver will be deployed after the ASICs are made out, in 2017.

- 1) Normally, each function will be tested separately meanwhile other functions will be deactivated for the first step of the characterizations.
- 2) Then a single ASIC will be implemented for driving one regular power device in order to verify the functions of the whole integrated circuit. Our efforts are pushing to minimize the risks of the failure.
- 3) The gate driver will be set-up with the passive devices as the configuration in Fig.IV.4 for a low side – high side power devices. This time, the gate driver circuitry and the power devices are separated.
- 4) Finally, the works will implement this gate driver inside the regular power switching cell before a final implementation into high temperature power module GaN-based component, considering the integration possibility of HF-HT transformer of the power supply. (GaN power modules will be delivered by the partner of MEGaN)

The performance of the driver will be studied to obtain the goals of WP3's specifications:

- The propagation delay
- The delay mismatch
- Conducted EMI perturbation on the remote control circuit
- CMTI
- Compare the impact of the interconnections
- Temperature endurance test

The experimental results will verify the advantage of the proposed gate driver on the conducted EMI perturbation ( $dv/dt$ ). By using the high temperature integrated circuit, this approach of the gate driver promises to eliminate maximally the parasitic elements in the gate driver circuit in order to improve the performance of the system.

### **IV.3 Conclusion and perspectives**

This chapter presents a panorama of the integrated gate driver circuit for high speed power devices in the context of high  $dv/dt$  and high temperature operating constraints developed within WP3 of MEGaN project, thanks to the collaboration between IDMOS, CEA LETI, Ampere lab and G2Elab.

Further works on the characterizations will verify the functions of the ASIC, and then it will be incorporated with the GaN based power device of MEGaN project. As we mentioned, the ASIC could implement up to 3kV of the low side high side isolation which allows using the SiC based power devices with the integrated gate driver or the GaN-based power devices in series connection.

Apparently, the wire-bonding technology will be used for these implementations. Moreover, flip-chip packaging technology must be considered in the next ASIC gate driver for optimizing extremely the EMI issues. Beside the gate driver circuit, the packaging of the power devices need to push to a highest degree for an optimized system, 3-D packaging or PCB embedded for example.

“Trời còn để có hôm nay,  
Tan sương đầu ngõ vén mây giữa trời.”

*“Heaven protects and saves you until today,  
Dispelling the fog and scattering the clouds.”*

Nguyen Du (1766 - 1820)



## General Conclusions and Perspectives

### Conclusions

In the beginning, this work has shown the EMI problems related to the gate driver architecture for the high speed GaN power components implemented in high temperature environments and producing high CMTI in a low side – high side configuration. We saw clearly that the conventional dual gate driver architecture with conventional circuitry implementations is not any more suitable of very high switching speed power devices.

Chapter I figured out from a theoretical point of view to optimize the propagation path for the conducted EMI perturbation elements flowing through the gate driver circuit.

Based on these ideas, the solutions were proposed in order to improve the conducted EMI perturbations from the power devices to the gate driver circuit; redirecting the parasitic disturbances currents “inside” the power module or switching cell before it propagates through control and ground(s). At the end of Chapter I, the configurations for the proposed gate driver circuit are depicted and analyzed. The main approach is based on cascading supplies and control signal transfer for the high side gate driver through the low side one. In such case, the high side gate driver supply is supplied from the low side supply, allowing to modifying the conducted EMI propagation paths, which turns, limits to common mode parasitic currents through the ground(s). If this architecture work does not actually reduce the parasitic currents through the components, it reduces significantly their propagation through the ground(s).

In chapter II were detailed and analyzed the proposed architecture thanks to simulations and experiments for the validations. The advantages on the conducted EMI optimization of the new gate driver architecture were detailed. In the recommendation section, we concluded that it is important to provide a path for the high side power supply and the control signal transfer unit through the low side elements of the gate driver, the cascaded circuitry for both high side supply and high side control signal is the best option. In this chapter, the locations of each device of the gate driver and associated circuitry were discussed. The buffers should be as close as possible to the power devices. The high side power supply and the signal transfer unit from the low side to the high side should be also close to the power devices. In these recommendations, the designs of the ASICs for gate driver circuit in a high temperature integrated technology are unavoidable.

In addition, more complex implementations of power devices were investigated, for example, two transistors in series. This section showed that the conducted EMI perturbation of series connected power devices is significantly more critical to study and to optimize than a simple low side high side implementation due to multi floating points and multi parasitic capacitances. Several architecture combinations are then possible. For time consideration, only a few analyses were carried out in this PhD work, leaving many options to be investigated later. Nevertheless, it has been concluded that, also in these more complex configurations, the management of conducted EMI propagation through the gate driver circuitries can be improved working at architecture level.

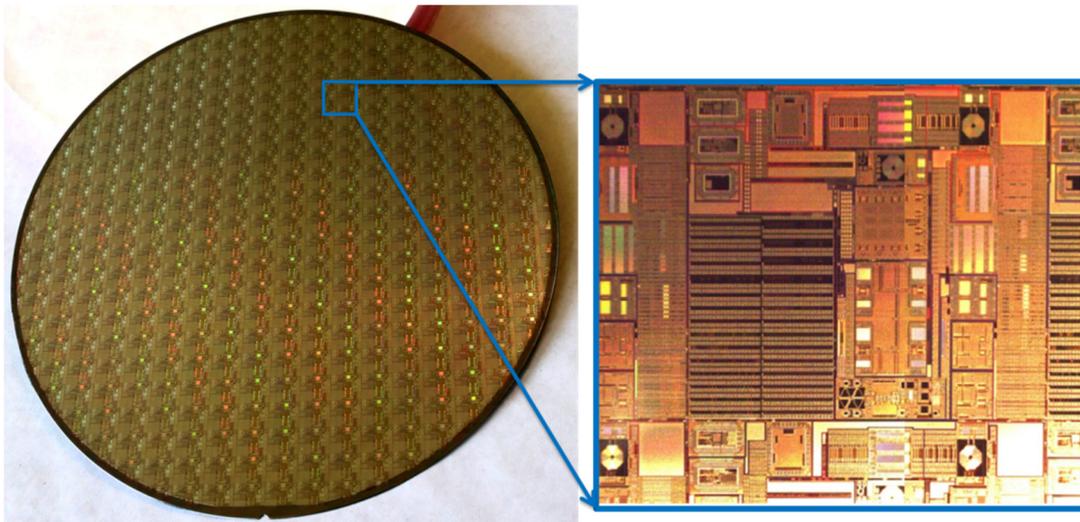
Working at architecture level showed nice reduction in conducted EMI level through the ground(s) of the converter but in fact, it had no effect on the parasitic currents flowing through the driver circuitry itself. Chapter III was dedicated on reporting efforts to answer the problems related to high

## *Design, characterization and implementation of an integrated CMOS gate driver circuit for GaN components*

### Conclusion and perspectives

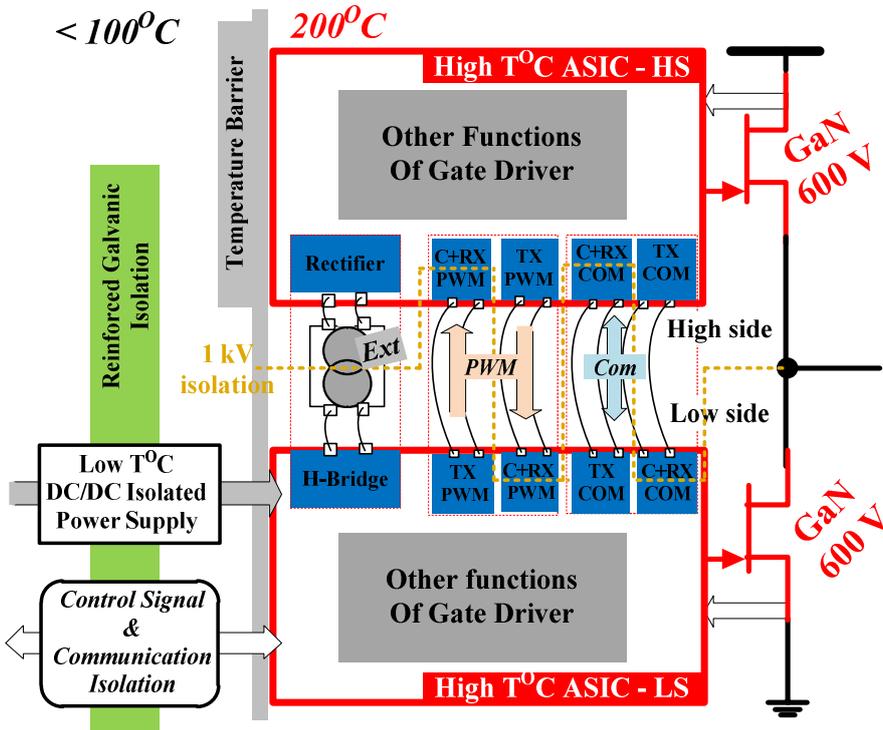
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temperature operation and parasitic component reduction, designing the elements of a new generation of gate driver circuits. The SAB converter was studied and selected for the high side power supply topology for its simple implementation, small number and size of passive magnetic components. The gate driver ASIC is integrating additional parts for implementing the active components and control circuitry of the SAB converter. This chapter described also the signal transfer unit based on a coreless transformer approach, well suited to high temperature and easy to integrate in the backend of CMOS technologies. Several test-chips were designed in the high temperature integrated technology XFAB XT018 to characterize and validate the opportunity to integrate the functions of each element. This was done, thanks to a multi-project wafer depicted in Fig.GCP.1, organized by IDMOS (MEGaN project partner) and founded by BPI France under MEGaN project. The test-chips were characterized at high temperature up to 250°C with respect to consumption, propagation delay, as well as with respect to parasitic elements. The control signal transfer unit based on coreless transformer approach showed fairly good propagation delay deviation (about 20ns), correct  $dv/dt$  immunity (25V/ns for instance due to the limitation of the experimental set-up) high operating voltage capabilities (at least 3 kV of the galvanic isolation), and fairly high operation temperature was validated, up to 200°C.



*Fig.GCP.1 Left, 8 inches wafer of the ASICs XFAB XT018. Right, the 1<sup>st</sup> version test-chips of the functions*

Finally, Chapter IV described a panorama of the integrated gate driver circuit within WP3 of MEGaN project thanks to the collaborative works between the partners: ID-MOS, CEA LETI, AMPERE Laboratory and G2ELab. Finally, the proposed gate driver architecture assuming a high temperature ASIC implementation is shown in Fig.GC.2.



*Fig.GCP.2 Configuration of the proposed gate driver architecture with the high temperature ASICs for 600V GaN components (Blue function blocks are designed by G2ELab)*

This implementation and the associated components are intended to answer high speed power devices new operating constraints in the context of high temperature and high dv/dt immunity requirements. Still, the final prototype needs to be produced and characterized and the time this thesis was reported.

## **Perspectives**

The perspectives are the future works at the system level of the gate driver and the implementations of the final ASICs with the proposed gate driver architecture.

### ***Gate driver architecture –Switching speed of power devices***

In these works, we have seen that the proposed gate driver architecture has reduced the conducted EMI perturbations on the ground of the control circuit for keeping the proper function of the gate driver circuit. And the proposed architectures improve the speed of the power devices:

- Improve slightly the switching speed of the power devices in a low side high side switching cells configuration
- Increase significantly this switching speed by the first validations in the circuit with the power transistors in series connection.

Hereby, the works on the architectures of the gate driver circuitries need to be continued to clearly state on the advantage and drawbacks of the approach. Especially, more experiments must be implemented to fully investigate the statements on the gain of the commutation speed of the power devices not only for a simple low side high side implementation but also for the complex system.

In that work, two phenomena should be studied simultaneously: work on the conducted EMI optimization on the gate driver circuit side and gain on the switching speed of power devices.

### ***High side power supply of gate driver***

It has been expected to be the most suitable candidate for the integrated high side power supply of the gate driver; the designs of the SAB converter are ended up without the characterizations of its HT-HF operation in the integrated implementation. In addition, characterization with a HF HT transformer will have to be carried out in collaboration with AMPERE laboratory. Work on this transformer optimization with respect to primary-secondary windings is essential to improve the CMTI of the gate driver.

Works are required to improve the synchronous rectifier since our structure of the first prototype has been simplified (comparators of the low-side NMOS transistors in order to ensure the reliability of the integrated circuit).

### ***Isolated control signal transfer unit***

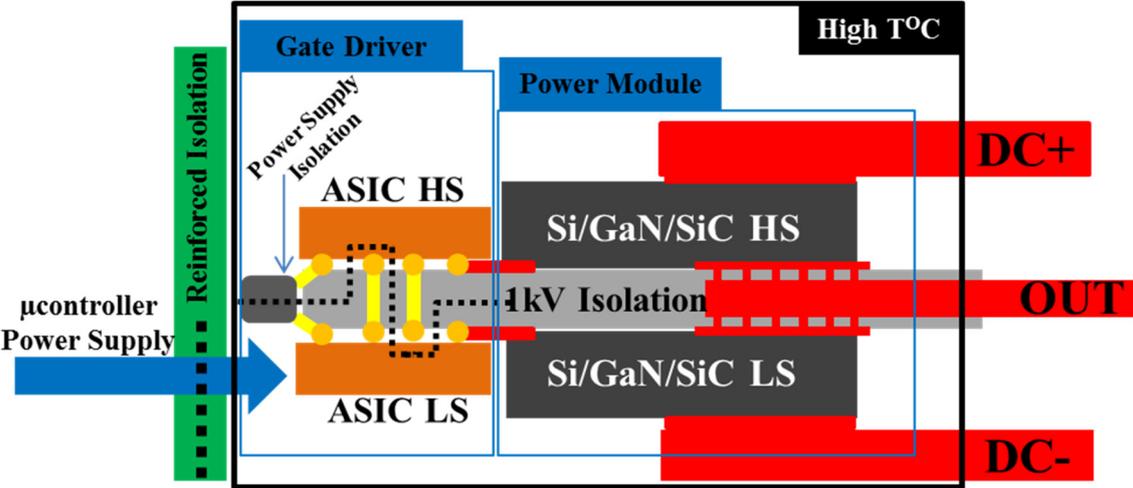
The CMTI of the control signal transfer unit based on an integrated coreless transformer approach was tested at 25V/ns due to the limitation of the set-up on a single die of ASIC. Nevertheless, the input-output parasitic capacitances for set-up with two separated dies should be improved. Thanks to an input-output parasitic capacitance for two separated dies prototype 10 times smaller, the perspective to operate under much higher CMTI is predicted at least 50V/ns and further works are engaged to improve the CMTI up to 100V/ns.

In this coreless signal transfer unit, due to the variations of the resistors inside the detection circuit with respect to temperature, the propagation delay high-to-low (H-T-L) increases significantly with respect to high temperatures. It corresponds to the discharging period of the capacitor into the resistor of the detection circuit. Using an active resistor could improve this delay time variation, making the delay of the signal transfer unit more stable, around 20ns.

Due to the limitation of the current experimental set-up, the maximum voltage was tested at 3kV without any breakdown. Meanwhile XFAB confirmed that the maximum value of the breakdown voltage of the metal layers is 5.2 kV. Hereby, another test on this voltage is required in order to confirm the possibility to implement the ASICs gate driver for the power modules with higher voltage range.

*Assembly a “fully” integrated gate driver with an innovative architecture into the power modules*

The final ASIC of the integrated gate driver is ready for manufacturing in the end of October 2016. The preparation toward the characterization in 2017 is described to obtain the specification of the MEGaN gate driver. In this preparation, the gate driver circuit will be performed with the power modules. However, the packaging of the ASICs and the packaging of the power modules need to be considered in order to decrease the parasitic elements of the circuits for the EMI optimization. For instance, the gate driver ASICs will be implemented with wire-bonding technology, the flip-chip would be the packaging of the next prototypes. The GaN power devices in 3D packaging technology or the power modules based on embedded die technology [123], [124], [125] would be the solution for the power parts of the final system: Fig.GCP.3.



*Fig.GCP.3 Cross-section of perspectives of gate driver circuit and 600V GaN power modules with advance packaging technology*

In this configuration, the high switching speed power modules could be GaN or other WBG components such as SiC based counter-parts where the low side – high side galvanic isolation of the ASICs is up to 5.2 kV which is confirmed by XFAB.

A lot of work remains here to be done to fully characterize the work carried out in this PhD dissertation.

*Design, characterization and implementation of an integrated CMOS gate driver circuit for GaN components*

Conclusion and perspectives

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## **Chapter V**

### **Résumé en français**

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### Résumé

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*Les travaux de la thèse sont intégralement focalisés sur la partie Driver intégré de composants GaN à base d'une technologie CMOS SOI XFAB XT018 pour favoriser l'utilisation des systèmes à haute fréquence et haute température. La thèse consiste à étudier des architectures des drivers et des fonctionnalités innovantes permettant de limiter les problèmes inhérents à la haute fréquence et la haute température (Compatibilité Électro Magnétique- CEM, pertes de commande par courant de fuites, limites fonctionnelles...). Suite à l'étude des architectures à l'échelle du bras d'onduleur à base de composants discrets, un circuit intégré est conçu en collaboration avec les partenaires du projet.*

*En particulier, des caractéristiques de réponses en fréquence et de tenue en température sont proposées. La mise en œuvre est conduite au sein même du module de puissance intégrant les composants de puissance en GaN, au plus près de ceux-ci pour favoriser les fonctionnements à haute fréquence. Le démonstrateur final peut servir plusieurs types d'applications grâce à sa versatilité. Le travail de thèse est alors plus spécifiquement orienté sur l'étude du comportement haute fréquence du driver et de l'ensemble interrupteurs avec de fortes vitesses de commutation / drivers d'un bras d'onduleur.*

## V.1 Introduction et motivations: circuit de pilotage pour les composants avec forte vitesse de commutation

### V.1.a Etat de l'art et objectifs du projet

Aujourd'hui, les composants classiques à base de silicium sont surpassés en termes de performances électriques et thermiques par les composants à grand gap avec des tenues en tension plus importantes mais la résistance à l'état passant plus petites. Donc, les pertes en commutation et en conduction sont diminuées. En plus, les composants à grand gap se présentent avec une vitesse de commutation élevée et une haute température opérationnelle.

Parmi la famille de composants à grand gap (Nitrure de Gallium (GaN) Carbure de Silicium (SiC) et Diamant), le GaN et le SiC existent de plus en plus dans les systèmes d'électronique de puissance modernes pour application à haute température et à fréquence élevée. Le GaN se positionne pour la basse tension mais avec des vitesses plus rapides comme le montre la figure de positionnement du marché des deux matériaux.

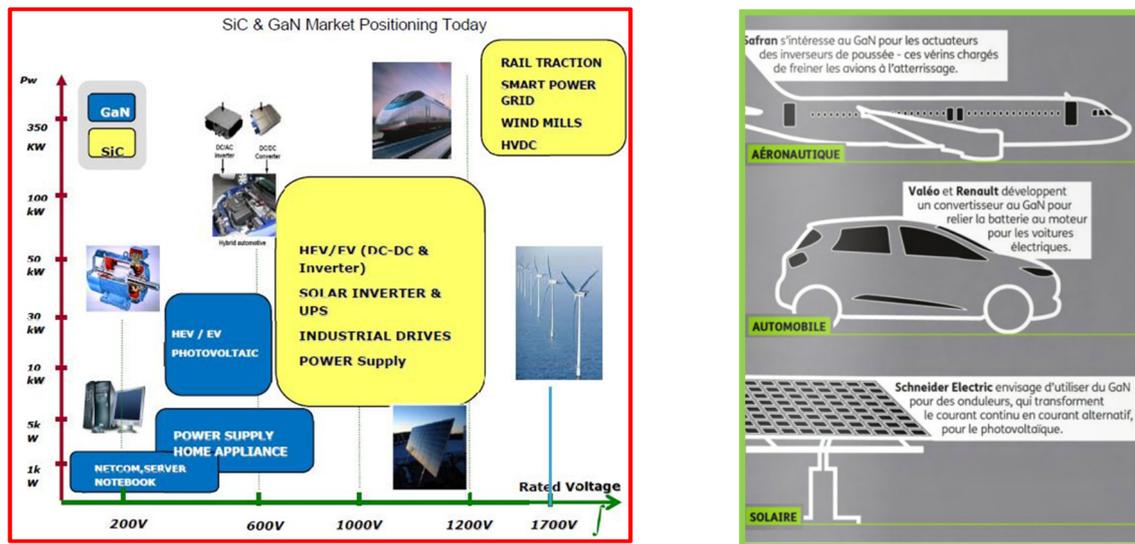


Fig.V.1 Gauche, positionnements du marché du composants GaN et SiC. Droite, contexte du projet MEGaN

Avec ces raisons, cette thèse s'inscrit dans le cadre d'un projet collaboratif (MEGaN – Module Electronique de GaN) avec de nombreux partenaires académiques et industrielles, les développements du projet sont autour de la technologie des composants GaN. Composants de puissance GaN: bon candidat pour les applications attendues par le marché (partenaires du projet), dans les domaines : aéronautique, automobile, management de l'énergie

Par contre, il y a deux barrières pour exploiter les avantages des composants GaN : le packaging et le gate driver (circuit de pilotage). C'est pourquoi, cette thèse est focalisé sur le gate driver pour composants GaN dans un bras d'onduleur.

En général, il y a des gros challenges pour les composants GaN comme la très forte vitesse ( $dv/dt$  et  $di/dt$ ). En plus, autour des composants de puissance et dans le circuit de pilotage, la température opérationnelle peut être élevée. Sur la Fig.V.2, on montre un bras d'onduleur avec les éléments parasites.

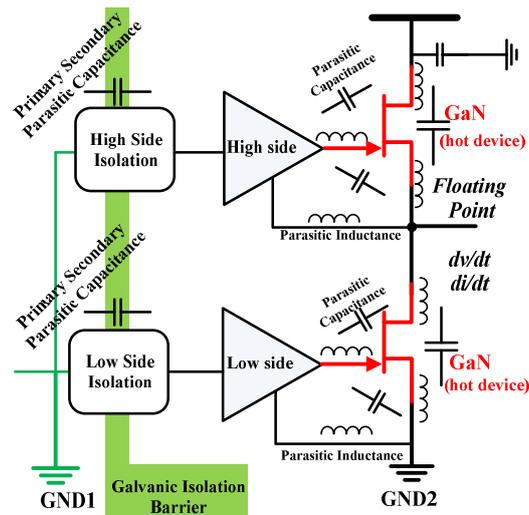


Fig.V.2 Défis du gate driver d'un bras d'onduleur

Pour améliorer la performance du système et exploiter les avantages des composants GaN, tout d'abord, il faut réduire les éléments de câblage en utilisant le packaging 3D ou le packaging Chip-on-Chip.

Dans le circuit de pilotage, il faut minimiser les inductances d'interconnexion, c'est-à-dire, mettre le driver à côté des composantes hautes températures. Les technologies intégrées hautes températures comme CMOS Si SOI ou CMOS SiC ou monolithique GaN sont alors considérées.

Le dernier point est sur l'immunité au  $dv/dt$  au niveau des composants, des travaux doivent être mis en œuvre pour optimiser les valeurs des capacités parasites des éléments du gate driver.

### V.1.b Deux approches proposées

La thèse propose des travaux sur deux approches complémentaires : système et composant.

Au niveau de système, une nouvelle architecture comme le montre la Fig.V.3 est proposée pour modifier les chemins de propagation des perturbations pour ne pas amener les perturbations vers le circuit de commande. Dans cette architecture, toutes les entrées du circuit de pilotage rentrent en bas pour piloter le transistor low-side, ensuite, elles transitent vers le haut en traversant les éléments cascades pour piloter le transistor high-side.

Au niveau des composants, le driver (ASIC) doit fonctionner à haute température et les capacités parasites de éléments du gate driver doivent être minimisées.

La technologie intégrée haute température utilisée est XFAB XT018. La température confirmée est  $175^{\circ}\text{C}$  avec 6 niveaux de tension des composants (1.8V, 5V, 10V, 40V, 100V, 200V).

La technologie de packaging flip-chip est considérée comme une perspective de la thèse pour améliorer la performance finale du système.

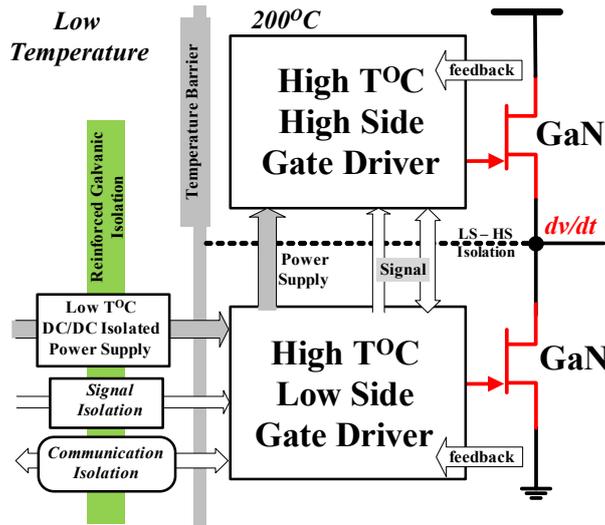


Fig.V.3 Proposition du gate driver au niveau système.

## V.2 Architectures du gate driver pour un bras d'onduleur

### V.2.a Architecture classique

Avant d'aller à notre architecture proposée, je présente le problème de l'architecture conventionnelle.

Dans cette architecture comme le montre la Fig.V.4, il y a deux alimentations isolées indépendantes, deux unités transferts d'ordre de commande isolées indépendantes. Il y a trois zones différentes avec trois tensions de référence: GND1, GND2 et point milieu.

Dans cette architecture, la perturbation de  $dv/dt$  est générée au point milieu par rapport à la masse GND2, elle fait apparaître un courant ( $C \cdot dV / dt$ ) en passant par l'alimentation high-side comme dans son circuit simplifié. Alors, ce courant est divisé en deux chemins, grâce au ratio entre les deux impédances vers GND1 et GND2, une petite partie retourne à la partie puissance, la plus grande partie attaque le circuit de commande d'entrée au niveau du primaire référencé par rapport à GND1.

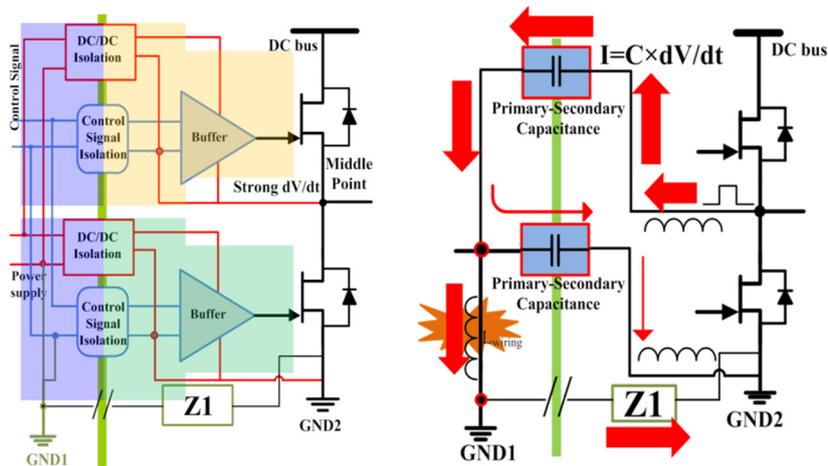


Fig.V.4 Architecture classique et son circuit simplifié

### V.2.b Architecture proposée

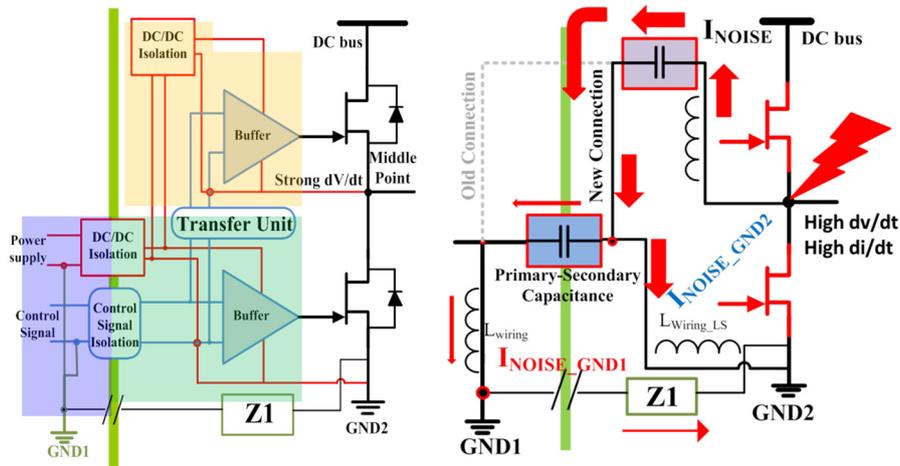


Fig.V.5 Architecture proposée et son circuit simplifié

La Fig.V.5 montre l'architecture proposée. Dans cette architecture, il n'y a qu'une voie d'entrée unique de l'alimentation et du transfert d'ordres. Les alimentations sont cascadées et les unités de transferts d'ordres de commandes sont également cascadées.

Dans cette architecture proposée, le courant de circulation ( $C * dV / dt$ ) est divisé en deux chemins, grâce au ratio modifié entre les deux impédances vers GND1 et GND2, plupart du courant retourne à la partie puissance. Finalement, il y a un confinement de la circulation du courant en mode commun.

### V.2.c Validations

Pour valider notre architecture proposée, les simulations des circuits simplifiés équivalents en haute-fréquence ont été mis-en-œuvre. Ensuite, les validations expérimentales sont présentées dans la Fig.V.6 comme les détails du chapitre II.

- A1 : architecture classique
- A2 : Architecture proposée sans l'optimisation de câblages d'interconnexion
- A3 : Architecture proposée avec l'optimisation de câblages d'interconnexion
- A2 : Architecture proposée comme un compromis entre l'optimisation de câblages et les positionnements des éléments du gate driver

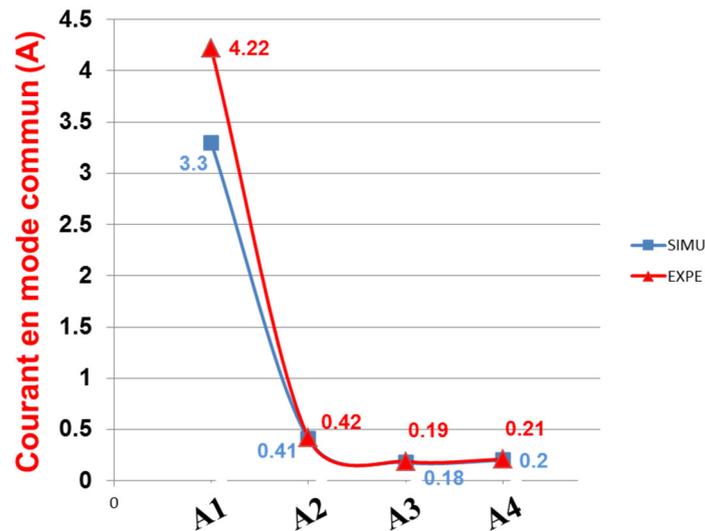


Fig.V.6 Validations des architectures sur le courant en mode commun. Résultats de simulation et résultats expérimentaux

### V.2.d Recommandations de la conception du gate driver pour composant GaN

Les recommandations de la conception du gate driver pour modules de puissance avec forte vitesse de la commutation sont présentées dans la Fig.V.7.

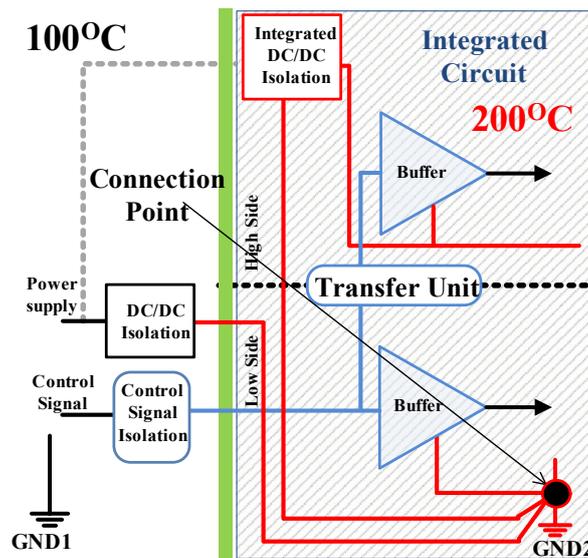


Fig.V.7. Recommandations de la conception du gate driver

Les buffers et l'unité de transfert d'ordres doivent être à proximité de dispositifs de puissance.

“Connection Point” est la sortie de l'alimentation low-side et l'entrée de l'alimentation high-side qui doit être connecté à GND2. Les alimentations sont bien cascadiées. Les capacités de découplage de l'alimentation high-side est au plus près de GND2. Les conclusions de la partie d'alimentation peuvent être transposées au transfert des ordres de commande.

Pour augmenter la température opérationnelle, les éléments haute température sont utilisés enfin de diminuer les capacités parasites de ces éléments : alimentation du high-side et unité de transfert d'ordre de low-side vers high-side.

### V.3 Dimensionnements des nouveaux circuits du gate driver

#### V.3.a Synoptique du gate driver MEGaN

La synoptique du gate driver MEGaN est montrée dans Fig.V.8.

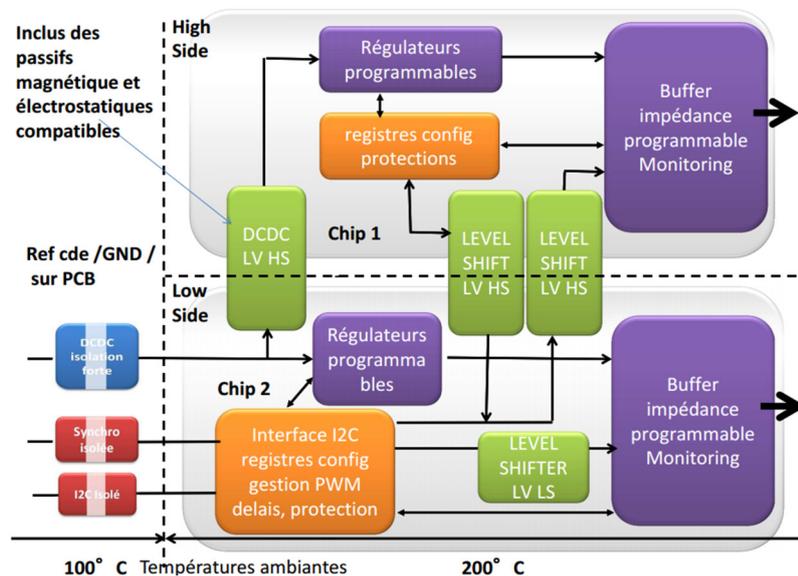


Fig.V.8 Synoptique du gate driver MEGaN

Deux ASICs identiques sont utilisés pour un bras d'onduleur low-side et high-side.

Dans chaque ASIC, il y a :

- Alimentation intégrée haute température (parties actives). L'isolateur magnétique de l'alimentation est localisé à l'extérieur de l'ASIC.
- Unité de transfert des ordres de commande du transistor
- Régulateurs programmables
- Buffers programmables
- Blocs logiques

Nos contributions sont sur les parties actives de l'alimentation intégrée haute température et l'unité de transfert des ordres de commande du transistor.

#### V.3.b Validations expérimentales des puces de test

Dans cette partie de dimensionnement, on a dimensionné l'alimentation et le transfert des ordres du gate driver, et on a validé expérimentalement les points développés.

Pour l'alimentation, après une étude des techniques d'alimentation du « High-Side» et les topologies isolées appropriées, le convertisseur SAB (Single Active Bridge) a été choisi comme une alimentation DC-DC isolée. Les circuits primaire et secondaire intégrés haute température XFAB XT018 ont été dimensionnés et validés.

Pour l'unité de transfert des ordres de commande, le driver avec le transformateur sans noyau intégré en XFAB XT018 a été choisi et validé.

### V.4 Mise en œuvre d'un gate driver intégré sous la forme d'un ASIC

Dans le projet MEGaN, le Work-Package 3 (WP3) est dédié à la conception et au prototypage du gate driver intégré. Il y a 4 partenaires de WP3 :

- ID-MOS : est pour la partie numérique
- CEA-LETI : est pour la partie buffer
- Laboratoire AMPERE : est pour le transformateur HT-HF pour l'alimentation
- G2ELab: est pour les parties actives de l'alimentation et unité de transfert des ordres

Un ASIC de 2mm x 3mm est en cours de finalisation comme dans Fig.V.9.

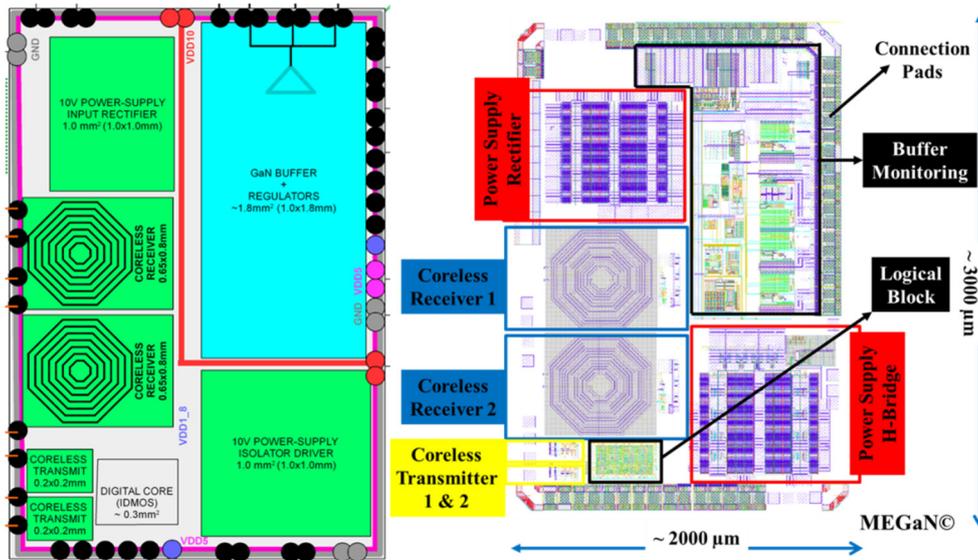


Fig.V.9 Gauche, fonctionnalités de l'ASIC. Droite, le layout final de l'ASIC

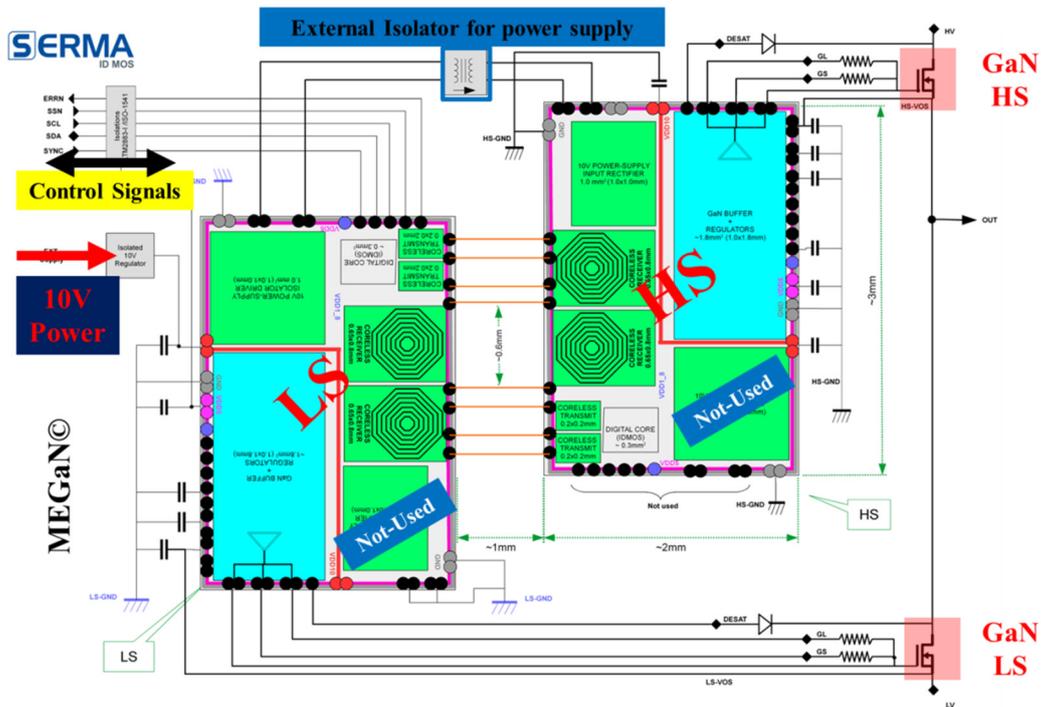


Fig.V.10 Schématique du gate driver pour les composants GaN

Le schéma du gate driver pour les composants GaN est montré dans Fig.V.10. Dans cette configuration, il y a deux ASICs identiques utilisés pour le mode de fonctionnement du low-side et du high-side. Un transformateur HF-HT est à l'extérieur pour l'alimentation du high-side du gate driver, c'est-à-dire, le convertisseur SAB. La technologie de packaging fils-bonding est utilisée pour les connexions dans cette étape de validation fonctionnelle.

## **V.5 Conclusions**

Dans ces travaux de thèse, une architecture du gate driver pour améliorer les perturbations CEM conduites des composants grand gap a été proposée pour résoudre le problème au niveau système & au niveau composant.

Les études approfondies des perturbations CEM conduites dans un driver avec très fort  $dv/dt$  pour un bras « high-side » et « low-side » ont été réalisées : caractérisation des différentes architectures, étude des effets des positions des éléments et des interconnexions. En plus, une extrapolation des architectures du gate driver avec les transistors mis en série a été présentée.

Dans ces travaux de thèse, l'alimentation du high-side et le transfert des ordres du gate driver ont été dimensionnés et validés expérimentalement sur les points développés.

A la fin de ces travaux, un gate driver complet sous la forme d'un ASIC a été présenté avec la préparation des caractérisations du gate driver final avec les composants grand gap en GaN.

## Publications

### International Journal

- V-S. NGUYEN, L. KERACHEV, P. LEFRANC and J-C. CREBIER” *Characterization and analysis of an innovative gate driver and power supplies architecture for HF power devices with high dv/dt*” IEEE Transactions on Power Electronics, .Volume: PP, Issue: 99, pp. 1-1, Oct. 2016 (early access).

### International conference

- NGUYEN Van-Sang, Lyubomir KERACHEV, Pierre LEFRANC and Jean-Christophe CREBIER ” *Characterization and analysis of an innovative gate driver and power supplies architecture for HF power devices in harsh environment*” 9th International Conference on Integrated Power Electronic Systems (CIPS 2016), March 2016. (*Oral*)
- V.-S. Nguyen, T.-L. Le, F. Sarrafin, N.-D. To, D. Colin, N. Rouger, P. Lefranc, Y. Lembeye, J.-D. Arnould, B. Allard, and J-C. CREBIER, “*Contributions to dedicated gate driver circuitry for very high switching speed high temperature power devices*” in 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2016, pp. 443–446. (*Oral*)
- NGUYEN Van-Sang, Pierre LEFRANC and Jean-Christophe CREBIER ” *Gate driver architectures for high speed power devices in series connection*” International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM 2017), May 2017. (*Oral-Accepted*)

### National conference

- V.-S. Nguyen, T.-L. Le, F. Sarrafin, N.-D. To, D. Colin, N. Rouger, P. Lefranc, Y. Lembeye, J.-D. Arnould, N. Corrao, B. Allard, and J-C. CREBIER, “*Contributions aux circuits de commande gate driver dédiés à la haute température et aux très fortes vitesses de commutation*” in SGE 2016 – Symposium de génie électrique, Grenoble, France, 2016. (*Poster*)



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**APPENDIX**

## Appendix A: Design the gate driver circuit of integrated H-Bridge of the SAB converter (XFAB XT018)

As we mentioned in Chapter III, we designed an H-Bridge for the SAB converter by using two identical inverter legs as in Fig.A.1. This structure allows providing a sufficient current for the power transistor  $M_P$  and  $M_N$  and managing the dead-time within the inverter leg.

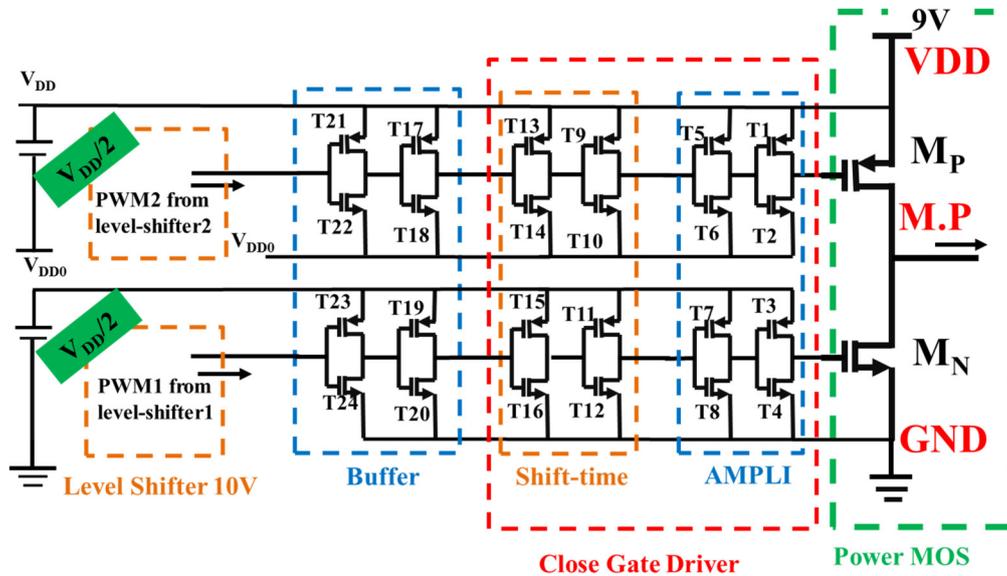


Fig.A.1 Schematic of the inverter leg with level shifters and buffers

The input parameters of the inverter leg calculation are (Datasheet XFAB XT018):

Table.A.1 Input parameter of the inverter leg and XFAB XT018 for calculations

Parameters	Symbol	Value	Unit
Current	I	$100 \times 10^{-3}$	A
Voltage	$V_{DD}$	10	V
Frequency	f	$10^6$	Hz
Maximum gate-source voltage of XFAB XT018 10 transistor	$V_{GS}$	5.5	V
Threshold voltage NMOS 10V (nmva)	$V_{th\_N}$	0.85	V
Threshold voltage PMOS 10V (pmva)	$V_{th\_P}$	-085	V
Number of finger (only in calculation)	N	1	
Channel length CMOS	$L_n$	$500 \times 10^{-9}$	m
Oxide Capacitance	$C_{OX}$	$2.71 \times 10^{-3}$	F/m <sup>2</sup>
Gain factor	$\beta$	$111 \times 10^{-6}$	A/V <sup>2</sup>
Effective Mobility NMOS 10V	$\mu_n$	400	cm <sup>2</sup> /Vs
Effective Mobility PMOS 10V	$\mu_p$	97	cm <sup>2</sup> /Vs

### A.1 First stage of AMPLI

In Chapter III, the 10V power transistors  $M_P$  and  $M_N$  are calculated with the value of the total channel width:  $W_P = 33 \text{ mm}$  and  $W_N = 11 \text{ mm}$ .

In several Ph.D researches of G2ELab (Olivier DELEAGE, Trung Hieu TRINH, Lyubomir KERACHEV [108], [89], [99]), an integrated inverter leg with its closed control circuit has been developed. With the same method, this work inherits their works for making an inverter leg with the closed control circuit in the integrated high temperature technology XFAB XT018. The AMPLI circuits locate between two power components of the inverter leg for distributing the control signal as described in Fig.A.2. The maximum gate-source voltage of a 10V transistor is 5.5V, thus all the elements of the control circuit are made by 5V transistors.

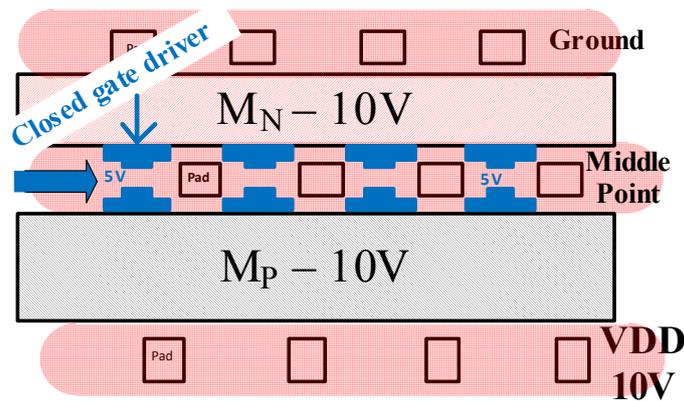


Fig.A.2 An inverter leg: the closed control circuit between two power components

The sizes of the transistors ( $T1 - T4$ ) of the AMPLLI first stage are critical because an undersized results in additional switching losses, since the transistors of this stage do not provide enough current for rapid switching power transistors. However, over-design would lead to over-size of the silicon.

In this stage, they will be provided more charges for switching. Finally, the transistors are driven by the same signal and therefore a short circuit appears. To limit the short circuit between them, the sizes of the components need to be decreased. The second stage will limit the short circuit in this stage.

Fig.A.3 shows the relation between the switching losses and the maximum current supplied by the MOS of the first stage.

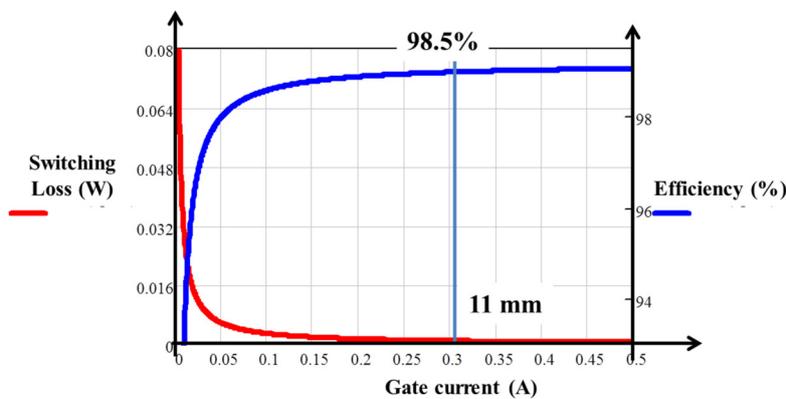


Fig.A.3 switching loss and efficiency of first stage of AMPLI

In this figure, the efficiency of 98.5% corresponds to 320 mA, below this value, the switching losses increase rapidly. It means that the power transistors are not controlled properly. For first stage, the transistors are designed so they can provide 320 mA. According to XFAB XT018 datasheet, the maximum drain-source saturation currents are 270  $\mu\text{A}/\mu\text{m}$  and 520  $\mu\text{A}/\mu\text{m}$  for the 5V PMOS and the 5V NMOS, respectively.

With this reasons, the size of the transistors have been selected as:

$$W_1 = W_3 = \frac{0.32}{I_{Sat\_Min\_P}} = \frac{0.32 \text{ A}}{270 \frac{\text{A}}{\text{m}}} = 1.18 \text{ mm}$$

$$W_2 = W_4 = \frac{0.32}{I_{Sat\_Min\_N}} = \frac{0.32}{520 \frac{\text{A}}{\text{m}}} = 0.62 \text{ mm}$$
(A.1)

A short circuit that may appear in this first stage, a second stage of AMPLI is necessary to limit the short circuit within the first stage.

### A.2 Second stage of AMPLI

The second stage is used to control the first stage transistors, the size of the transistors of the second stage relate directly to the short circuit current in the first stage. To identify the short-circuit current within the first stage of the closed control circuit, Fig.A.4 shows the input and output voltages of the first stage in three phases for two different scenarios. In the 1<sup>st</sup> case, the input and output voltage of the 1<sup>st</sup> stage have the equivalent dynamic. As we can see, at the end of phase 2, wherein the two transistors of the 1<sup>st</sup> stage are closed simultaneously, the output voltage of the 1<sup>st</sup> stage (VGN) takes time to reach relatively a high value, which is causing the short circuit. The second case shows a switch where the input is much more dynamic than the output voltage of 1<sup>st</sup> stage, thereby limiting the voltage as the origin of the short circuit because the transistor is completely closed which means the input voltage reaches zero before the output voltage begins voltage across the low side switch. If this output voltage is low in the scale of the switching cell, a small current will go through the low side transistor then limit the negative effects of short circuit.

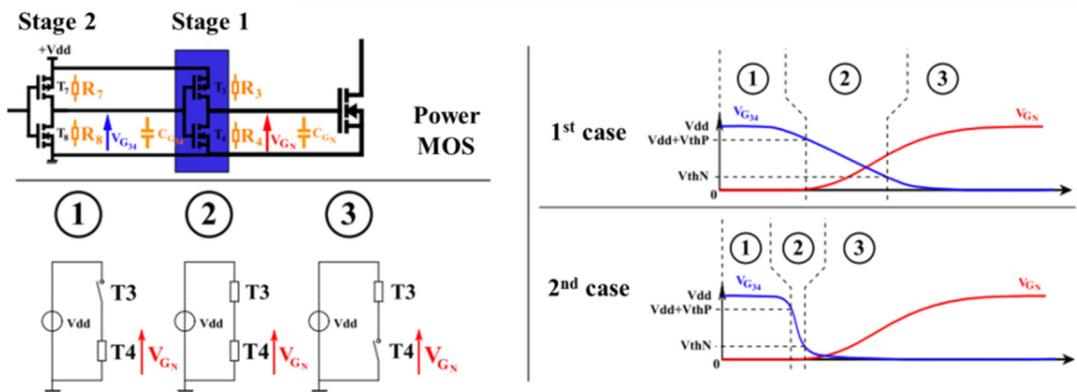


Fig.A.4 Input and output dynamic of second stage of the closed control circuit in the low side channel (for low side power transistor) [108]

To evaluate the speed of the input voltages and output voltage within the 1<sup>st</sup> stage, a value has been considered as the time constant between the input and the output. These time constants are defined by the on-resistance of transistors, since they get evolve during switching time as Equation A.2.

$$\alpha = \frac{R_3 \times C_{gN}}{R_8 \times C_{g34}} \quad (\text{A.2})$$

Based on the value " $\alpha$ ", the size of 2<sup>nd</sup> stage transistor can be defined. Therefore, as for 1<sup>st</sup> stage, there is a compromise between the losses and the size, this value  $\alpha$  is estimated to 5 as in Fig.A.5. This value allows us to design the 2<sup>nd</sup> stage of the closed control circuit.

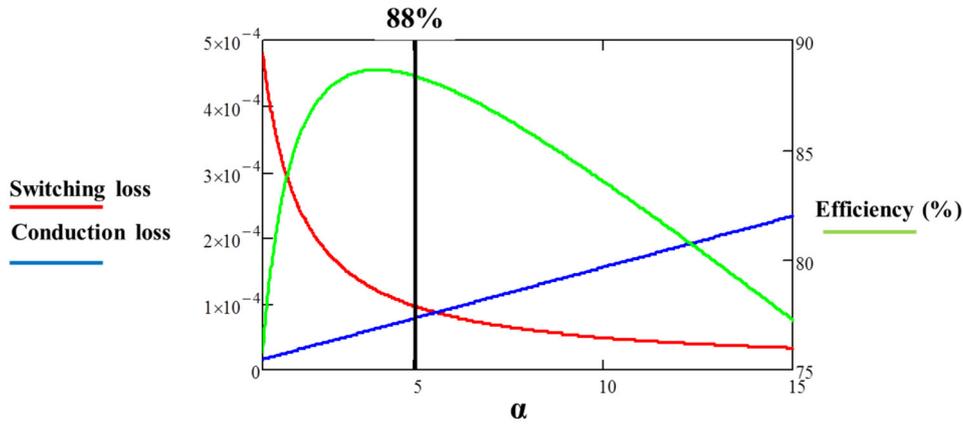


Fig.A.5 Design of the 2<sup>nd</sup> stage

The transistors of the 2<sup>nd</sup> stage are expressed in Equation A.3:

$$\begin{aligned} W_6 &= \frac{W_2}{\alpha} = 123 \mu\text{m} \\ W_8 &= \frac{W_3}{\alpha} = 237 \mu\text{m} \\ W_5 &= 3 \times W_6 = 369 \mu\text{m} \\ W_7 &= 3 \times W_8 = 711 \mu\text{m} \end{aligned} \quad (\text{A.3})$$

In fact, the sizes of the transistors in the 2<sup>nd</sup> stage are small enough to avoid the short circuit current within a switching cell. We can also design a 3<sup>rd</sup> stage in regarding the sizes of the transistors in 2<sup>nd</sup> stage in the context of the efficiency of the closed control circuit. A ratio of 20 between the 2<sup>nd</sup> stage and the 3<sup>rd</sup> stage is usually used in the reality to ensure the compromise size/loss.

As described in Fig.A.2, the 1<sup>st</sup> stage and the 2<sup>nd</sup> stage are divided into to 4 parts for contributing the control signal to the power component, due to these small divided sizes the 3<sup>rd</sup> stage is not needed in our specific layout design.

After the 2<sup>nd</sup> stage, a shift-time stage is placed in order to create the dead-time within the inverter leg.

### A.3 Shift-time stage

To limit the short circuit current within the inverter leg of the power transistors which may take place, it is necessary to design for the distinct periods of conduction of the NMOS and PMOS power transistors. For this, we opted for a simple analog circuit. Another solution could be directly developed as the dead-time management in the digital circuit. However, to ensure the reliability, we implemented a shift-time stage in the closed control circuit as depicted in Fig.A.6.

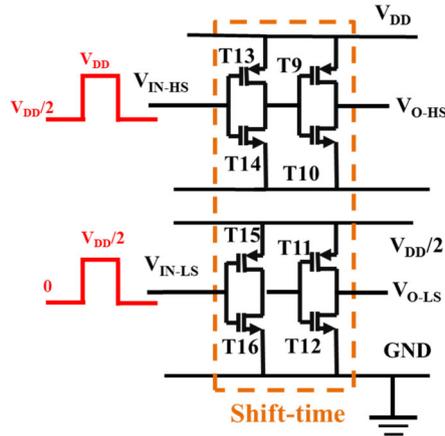


Fig.A.6 Shift-time circuit to manage the dead-time

The purpose of this circuit is to generate two signals  $V_{O\_LS}$  and  $V_{O\_HS}$  from two signals  $V_{IN\_LS}$  and  $V_{IN\_HS}$ . These signals  $V_{O\_LS}$  and  $V_{O\_HS}$  respectively will control the amplification stages of the NMOS and power PMOS.

The principle of the shift-time circuit is to delay the switching time of the power transistors. The output current of T9-T10 charges the gate capacitance of the PMOS power transistor. And the output current of T11-T12 is for the NMOS power transistor.

The ON resistances of transistors T15 and T15 are much more important than the other transistors of these stages. Therefore, when a negative switching of the input signal (high to low) occurs, T9 and T10 charge much faster than T11 and T12, it makes the delay of the high side signal  $V_{O\_LS}$  over the low side signal  $V_{O\_HS}$ . And, when a positive switching of the input signal (low to high) occurs, T11 and T12 discharge much faster than T9-T10, which can make a delay  $V_{O\_HS}$  over  $V_{O\_LS}$  (see Fig.A.10).

According to [108], a suitable set of the shift-time stage is designed as:

$$\begin{aligned}
 W_9 &= W_{11} = 35 \mu m \\
 W_{10} &= W_{12} = 15 \mu m \\
 W_{13} &= 35 \mu m \\
 W_{14} &= 0.5 \mu m \\
 W_{15} &= 1.35 \mu m \\
 W_{16} &= 15 \mu m
 \end{aligned} \tag{A.4}$$

In the simulation results, a suitable dead-time of 3ns has been created for the low side and the high side control signal (see Fig.A.10).

Due to our specific layout of the inverter leg, the supplementary buffers are inserted in order to ensure the sufficient current to the closed control circuit: one for the low side and another for the high side of closed control circuit as in Fig.A.7

The sizes of these buffers are adapted to the gap between two power components.

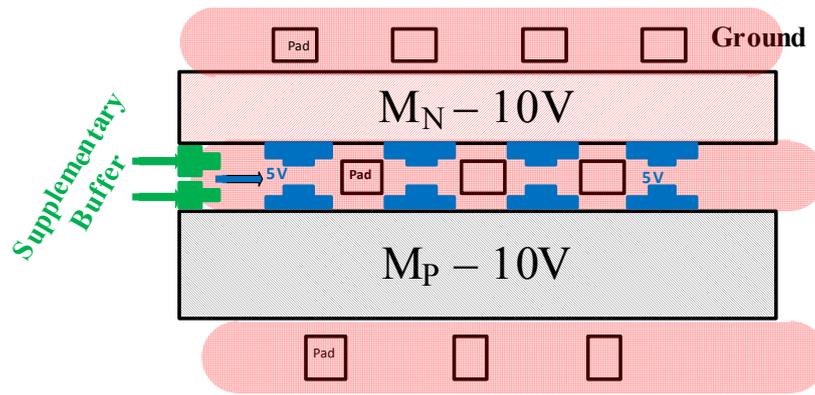


Fig.A.7 Supplementary buffer between two power components (green), layout of the inverter leg

#### A.4 Level-shifter for low side and high side control signals

The inverter leg with 10V power transistors but the maximum gate voltage is equal to 5V. Therefore the control circuit uses 5V transistor for its design.

In order to shift the voltage level for the high side as in Fig.A.8, the current-source level-shifter is implemented; see Appendix C for the details of the implementation of the level-shifter.

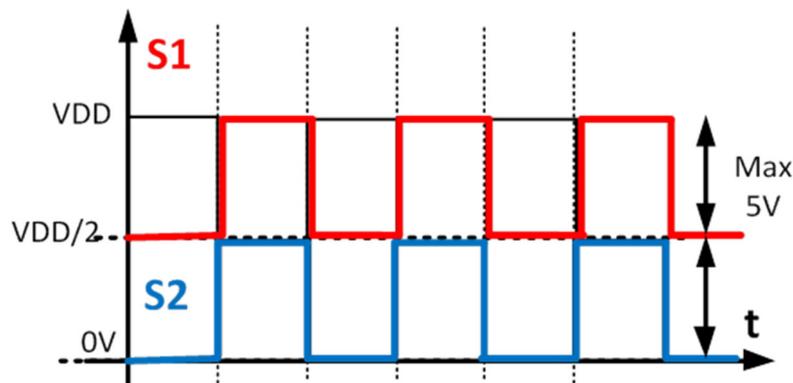


Fig.A.8 S1 is the control signal for the high side, S2 is the control signal for the low side

In MEGaN project, an integrated voltage regulator from CEA-LETI is used in order to step down the voltage  $V_{DD}$  to  $V_{DD}/2$ . The voltage  $V_{DD}/2$  is used for the current source level-shifter to generate the low side and the high side signal as in Fig.A.8.

Fig.A.9 and Fig.A.10 shows the simulation results of the low side and the high side control signals after the phase-shift stage and the dead-time of 3 ns between two signals.

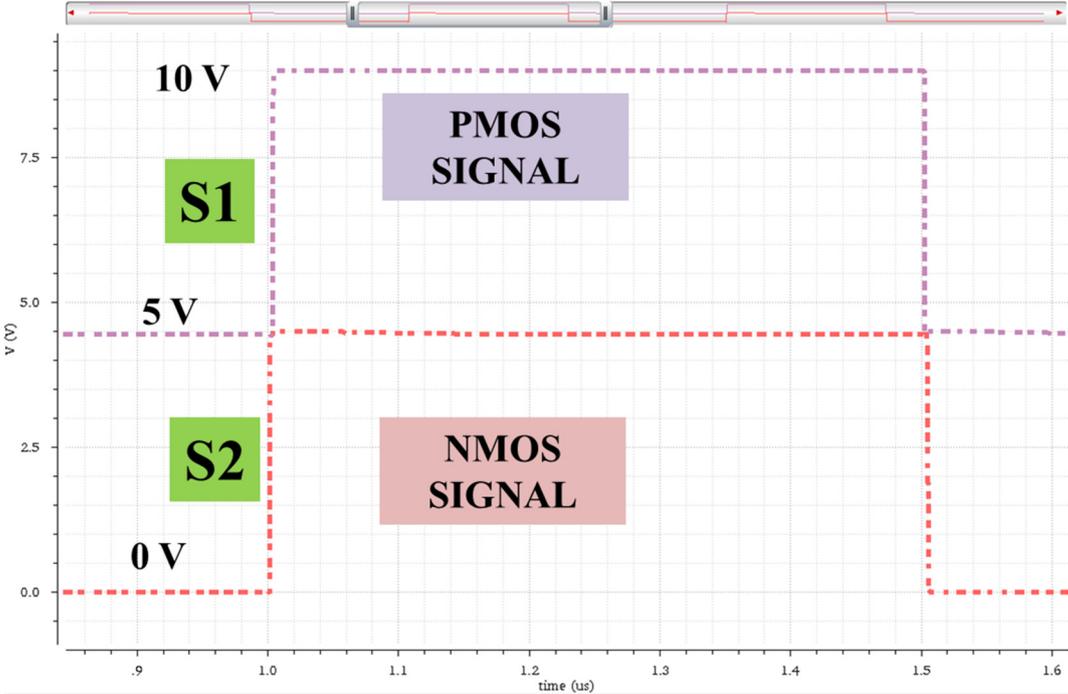


Fig.A.9 Low side and high side control signal after the dead-time stage, CADENCE simulation results

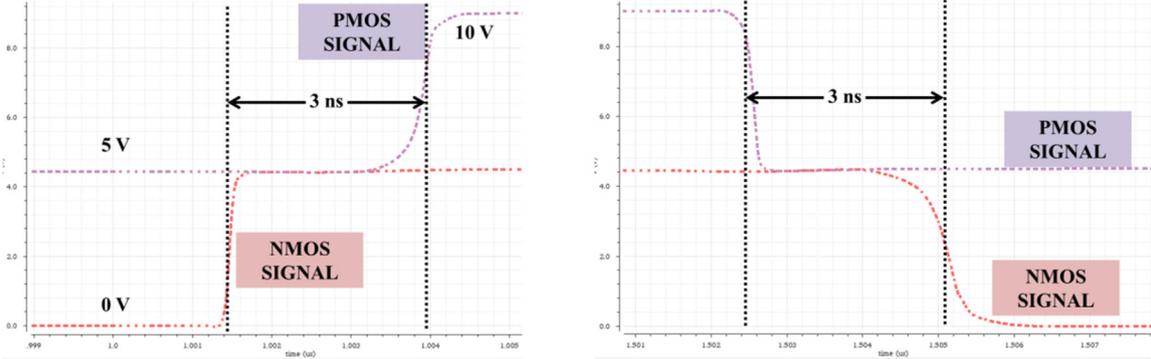


Fig.A.10 3ns of the dead-time between the low side and the high side control signals, CADENCE simulation results (zoom-in)

## Appendix B: The calculations of synchronous rectifier of the SAB converter

To continue the designs of the synchronous rectifier, this appendix details the design of the comparator circuit.

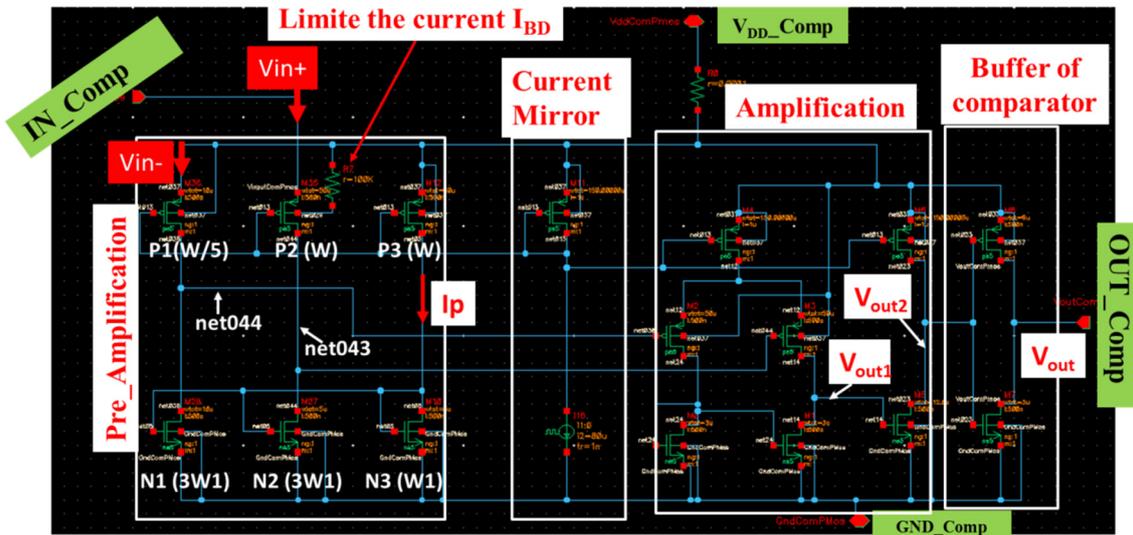


Fig.B.1 Schematic of the comparator of the synchronous rectifier

In this appendix, the pre-amplification stage, the current mirror stage, the amplification stage and the buffer stage of the comparator are detailed.

### B.1 Pre-amplification stage circuit:

The power devices are designed in Chapter III: P1-P3, P2-P4 and N1-N2.

In this design, the comparator is designed with the current  $I_{DC} = 80 \mu\text{A}$  as a compromise between the responding time and the energy consumption of the comparator. In the simulation, the output current of the mirror current  $I_p$  ( $I_{p1}$  and  $I_{p2}$ ) is  $100\mu\text{A}$  as the input signal of the pre-amplification stage (see Fig.B.3 for the outputs current of the mirror current  $I_{p1}$  and  $I_{p2}$ )

The transistors P1 and P3 are identical and to be polarized with the same way, they operate as a current source  $I_{\text{Sat}}$ . Where the polarized current of the transistor N1 and N2 is  $I_{\text{Sat}} = 3 \cdot I_p$  due to the different sizes of the NMOS and PMOS.

According to the works of Hynek Raisigel [118], the current  $I_{\text{DS}}$  on the transistors P1 and N1 is defined as  $I_{\text{Sat}_P1} \approx I_p/5 = 20 \mu\text{A}$  and  $I_{\text{DSat}_N1} = 3 \cdot I_{\text{DSat}_N3}$ . This makes the transistor N1 operating in the ohmic region instead of the saturated region.

The voltage on the transistor N1 –  $V_{\text{DS}_N1}$  is about 24 mV. For  $V_{\text{IN}_-} = V_{\text{IN}_+} = V_{\text{DDA}}$  the voltages  $V_{\text{DS}_N1}$  and  $V_{\text{DS}_N2}$  are the same.

Fig.B.2 shows the simulation results of the state of the pre-amplification stage with:

$$V_{\text{DD\_Comp}} = 10\text{V} \text{ and } V_{\text{GND}} = 5\text{V}$$

We found that  $\text{Net04} = 5.024$  and  $V_{\text{dsN1}} = 24\text{mV}$ .

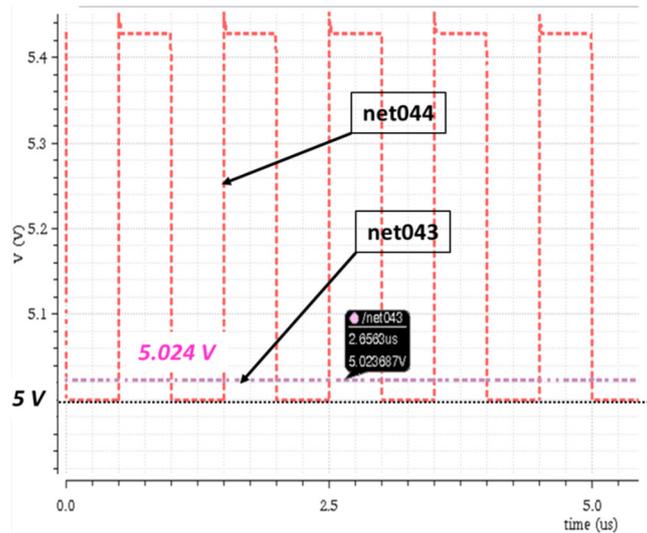


Fig.B.2 Voltage on the transistor of the pre-amplification stage:  $V_{DS\_P1}$  (net 44) and  $V_{DS\_N1}$  (net 43)

The sizes of the transistors in the pre-amplification stage are defined as the value of  $W$  and  $W_1$ . In our design,  $W = 50 \mu\text{m}$  and  $W_1 = 5 \mu\text{m}$  with the typical channel length of  $0.5 \mu\text{m}$

**B.2 Current mirror of the comparator**

The principal schematic of the current mirror is detailed in Fig.B.3. This current mirror supplies the activated currents to two comparators of PMOS transistors,  $I_{P1}$  and  $I_{P2}$ .

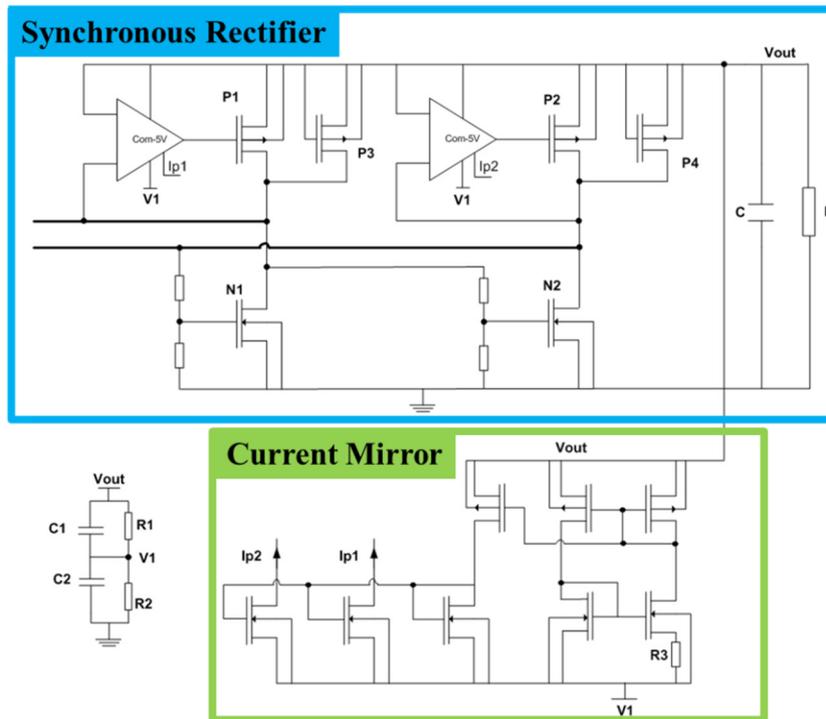


Fig.B.3 Mirror current of the synchronous rectifier

As we mentioned in Chapter III, the comparator is designed with the polarized current  $I_{DC}$  of  $80 \mu\text{A}$  as a compromise between the responding time, slew rate and the energy consumption of the comparator.

In the beginning, the output voltage  $V_{out}$  is equal to zero; the mirror current is not activated. The current  $I_{p1} = I_{p2} = 0$ . Then, the diode of the MOSFETs P3 and P4 are charged by the output capacitor of the SAB converter, supplied for the mirror current. When the mirror current is activated, the PMOS transistors (P1 and P2) of the synchronous rectifier are activated which make P3 and P4 short-circuited. The charging currents now are carried by the MOS.

To activate the mirror current, the applied voltage needs to be at least 2V. The simulation from the ambient temperature to 175°C with different  $V_{DC}$  of the mirror current is shown in Fig.B.4.

When the mirror current is activated, P1 and P2 are activated by the comparator, P3 and P4 are short-circuited.

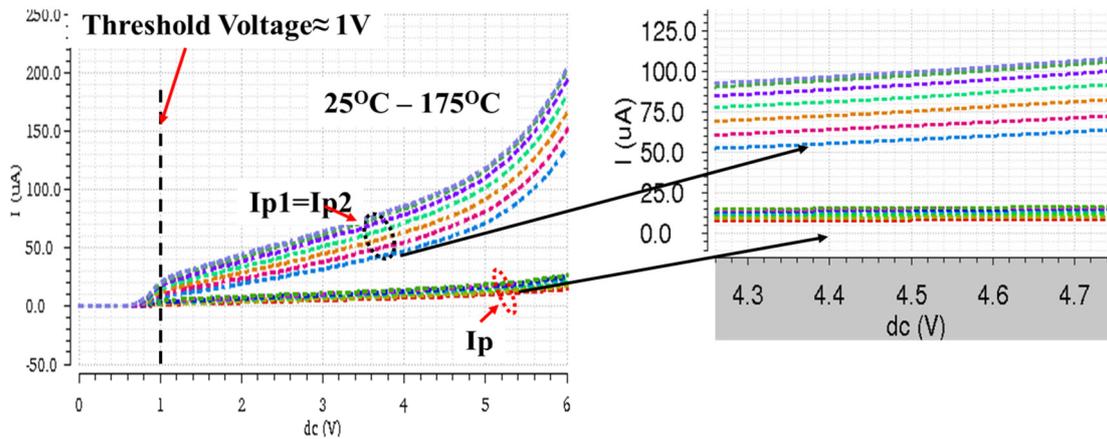


Fig.B.4 Current of the mirror current and current  $I_p$  of the pre-amplification stage with different supplied voltage  $V_{DC}$  (in the complete circuit,  $V_{DC}$  is  $V_{out}$  and GND is  $V_{out}/2$ )

### B.3 Amplification stage

Table.B.1 shows the parameters for implementing the amplification stage in the comparator.

Table B.1 Specification of the comparator

Parameters	Symbol	Specifications
Supply Voltage	$V_{DD}$	3V - 5V
DC Gain	$A_0$	> 50dB
Pass-Band	$f_{3dB}$	> 25 MHz
Slew rate of $V_{out2}$	SR	1000V/ $\mu$ s
Functional point of 1 <sup>st</sup> stage	$V_p$	$V_{in+} = V_{in-} = V_{DD}/2V$
Load	$C_c$	500fF

Fig.B.5 shows the amplification stage of the comparator, in this figure the transistors are named from M1 to M7.

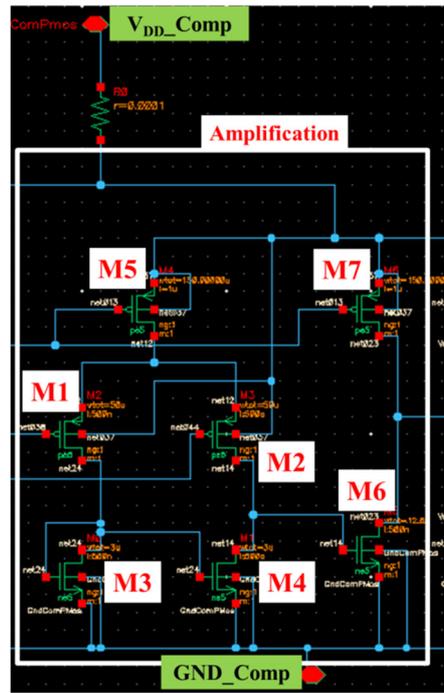


Fig.B.5 Amplification stage with its transistors

In the Fig.B.6, the simulation results present the gain of the different stages of the comparator. The gain of the first stage and the second stage are equal to 30 dB and 24 dB, respectively. Hereby, the total gain of 54 dB of the comparator is obtained which is satisfactory for the design constraints.

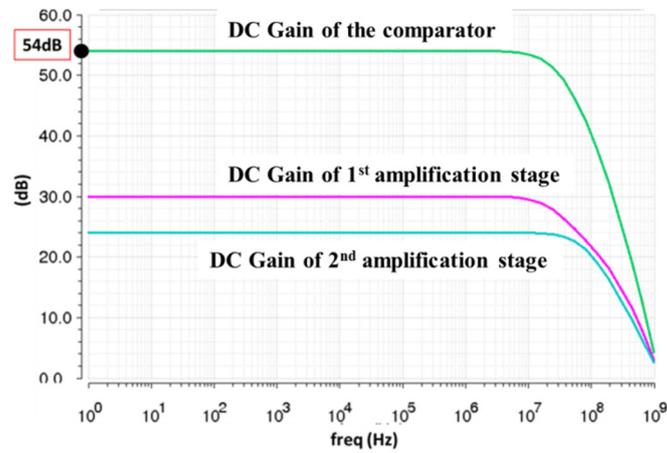


Fig.B.6 Gain of the different stages of the amplification stage, AC simulation results

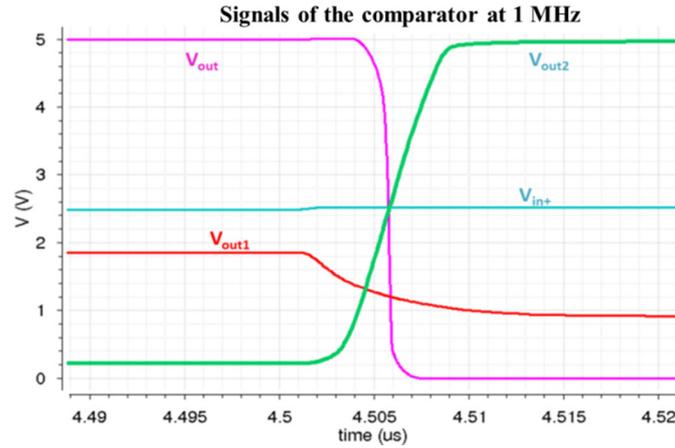


Fig.B.7 Signals of the comparator at 1 MHz, transient simulations results:  $V_{in+}$  of the pre-amplification stage,  $V_{out1}$  and  $V_{out2}$  of the amplification stage and  $V_{out}$  of the comparator

The simulation result of the comparator at 1MHz with an input voltage  $V_{ind} = 15\text{mV}$  is shown in Fig.B.7. The slew rate of the output voltage of the comparator  $V_{out2}$  is estimated of about  $1250\text{V}/\mu\text{s}$ .

Table.B.2 shows the designs of the transistors in the amplification stage according to the and the simulation results in CADENCE Virtuoso.

Table.B.2 The designs of the amplification stage by the estimations in simulation and the simulation results.

Design parameters		Simulation results	
$(W/L)_{1,2}$	$(50\mu\text{m}/0,5\mu\text{m})$	$V_{\text{SUPPLY}}$	5V
$(W/L)_{3,4}$	$(3\mu\text{m}/0,5\mu\text{m})$	$A_0$	54dB
$(W/L)_5$	$(150\mu\text{m}/1\mu\text{m})$	$f_{-3\text{dB}}$	25,87Mhz
$(W/L)_6$	$(12\mu\text{m}/0,5\mu\text{m})$	SR ( $V_{out2}$ )	$1250\text{ V}/\mu\text{s}$
$(W/L)_7$	$(150\mu\text{m}/0,5\mu\text{m})$	Consummation	$834\mu\text{A}$

The simulation is performed with  $V_{IN+} = 9.9\text{V}$  where  $V_{IN-}$  varies from 0 V to 10V with the duty cycle of 50% at 1 MHz; the voltage drop on the power transistor of the synchronous rectifier is estimated of about 100 mV, see Fig.B.8.

After this amplification stage, a small buffer is used to amplify the signal where  $W_p = 9\mu\text{m}$ ,  $W_N = 3\mu\text{m}$ .

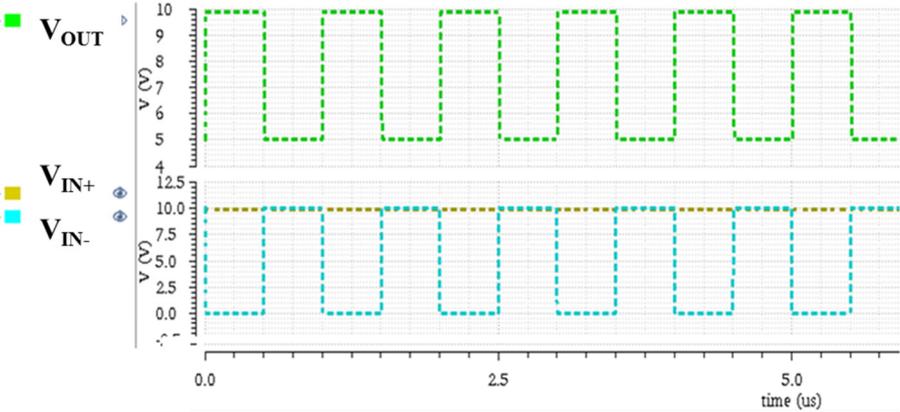


Fig.B.8 Input signals of the pre-amplification stage and the output signal of the comparator (for PMOS transistor)

## Appendix C: Signal transfer units: current source level-shifter and optical transmission

### C.1 An introduction of the Control Signal Unit (CSU) in the high voltage current source level shifter

Farshid SARRAFIN has developed a gate driver with the level shifter in his Ph.D work as a part of the industrial MEGaN project. This level shifter topology is composed of two pulsed Control Signal Units (CSU) as shown in Fig.C.1.

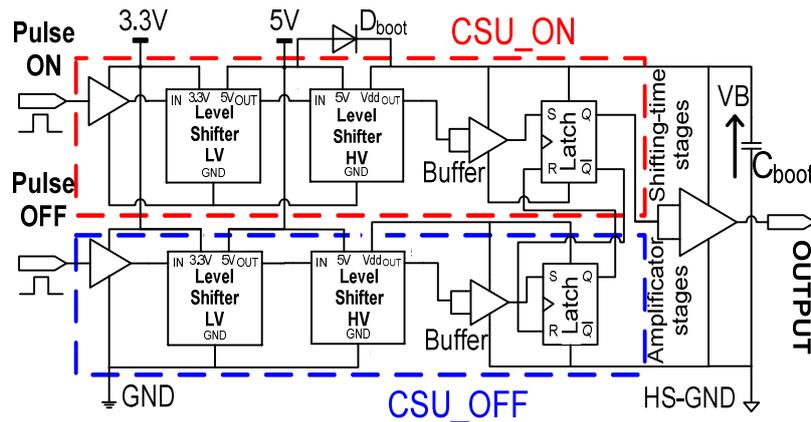


Fig.C.1 High voltage level shifter with CSUs

This CSU structure is made out of two channels, each carrying in a similar manner a pulse signal for optimizing the time location of each switching transition of each device. Time shifting between the two pulses is set accordingly to the duty cycle. An RS latch produces the duty cycle from the pulsed signals, with identical rise and fall time propagation delays, guarantying the duration of the duty cycle. This topology is also very well suited to optimize transistor to transistor switching because each CSU is designed to produce a reduced and very stable propagation delay. The opportunity to integrate all level shifters in one die, raise the possibility to keep all of them identical from a technological point of view and operated in similar operating conditions. In additional pulsed signal transmissions enable to design the mirror current level shifter with fairly large current ratings to improve their  $dv/dt$  immunity while maintaining its power consumption reasonably low ( $<10\text{mW}$ ). In this case, the voltage level of HS-GND can be shifted with respect to GND as much as the maximum drain to source voltage of  $T_{CM1}$  and  $T_{CM2}$  transistors in mirror current. Furthermore output parasitic capacitors value of transistor  $T_{CM2}$  in mirror current ( $C_{OSS2}$ ) is critical in order to limit EMI in high voltage Level-Shifter.

$C_{CM}$  is the common-mode parasitic capacitor and  $C_{OSS2}$  is the output parasitic capacitor of  $T_{CM2}$  in Fig.C.2. Once the slew rate in common-mode  $dv/dt$  appears, the noisy current is generated.

The IC was designed to exhibit high immunity to noise, low propagation delay, low power consumption due to the pulsed current control in mirror current and reliable signal transfer to a high voltage floating potential.

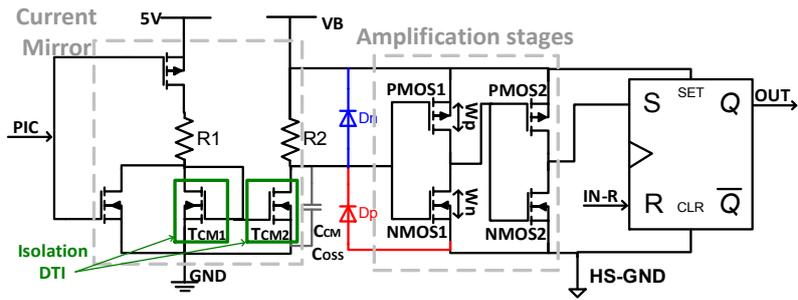


Fig.C.2 High Voltage Level Shifter topology proposed

As shown in Fig.C.3, a dedicated layout has been carried out to develop a first test chip as our collaborative work in MEGaN project. In order to match the mirror current values in both bridges of the mirror currents, the temperature of their transistors should be similar in each operating condition. Hence, these transistors must be placed side by side in the layout process to make their temperature as similar as possible.

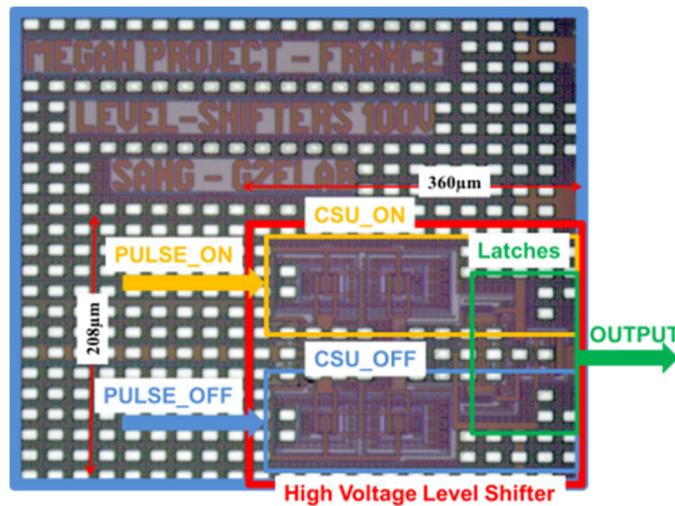


Fig.C.3 Microscope photo of XFAB XT018 level shifter

Fig.C.4 shows the output signals of the level shifter driver for a low side – high side implementation with its control signal.

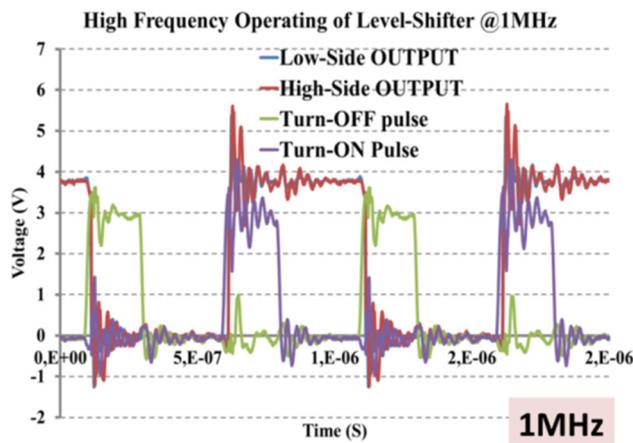


Fig.C.4 Pulsed signals for control and the output of the level shifter for a low side – high side implementation

In order to verify the operation and analysis of the proposed high voltage Level-Shifter as a function of temperature, a full set of characterization has been done. This section concerns the turn-on and turn-off signal propagation delays (Fig.C.5). In this case, input pulses width (turn-on and turn-off) is  $2\mu\text{s}$  for a 100 kHz operating frequency. As a matter of fact, propagation delay of turn-on signal increases of 0.9 ns (5.5%) for a temperature increase from 25 °C to 200 °C. In a similar way; the propagation delay of turn-off signal increases of 1.5 ns (9%).

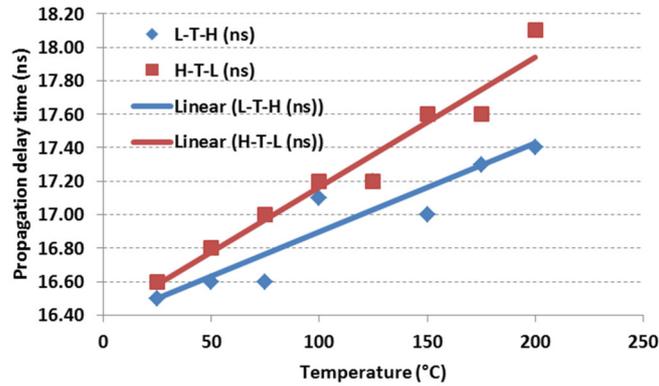


Fig.C.5 Propagation delay of turn-on and turn-off signals at differences temperatures

Concerning the immunity to  $dv/dt$ , the level shifter ended to be significantly sensitive even at reasonable low  $dv/dt$  of 5V/ns in Fig.C.6. As seen in the coreless driver, the  $dv/dt$  introduces large perturbation currents produce large disturbances greatly above expected levels. Transmission of gate signal is satisfactory but the gated signal is too much disturbed. Further work should be carried out here for a higher value of  $dv/dt$ .

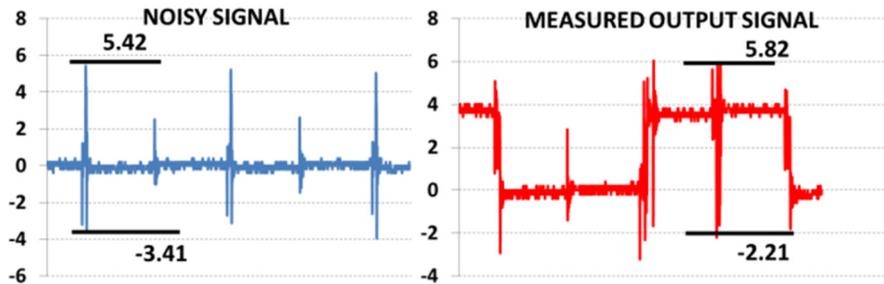


Fig.C.6 Output signals of the pulsed level shifter with  $dv/dt$ : a) No input signal, noisy signal at output; b) With input signal, measured output signal including the noise

## C.2 An introduction of integrated optical gate driver

An approach based on the integration of an optical gate driver is presented in Fig.C.7 by LE Thanh-Long during his PhD work. The control signal is transmitted by light via the external light emitter. As a function of its implementation approach, this allows very high levels of galvanic isolation and EMI immunity of the external gate control unit while being able to operate with transmitted optical power in the range of micro watts.

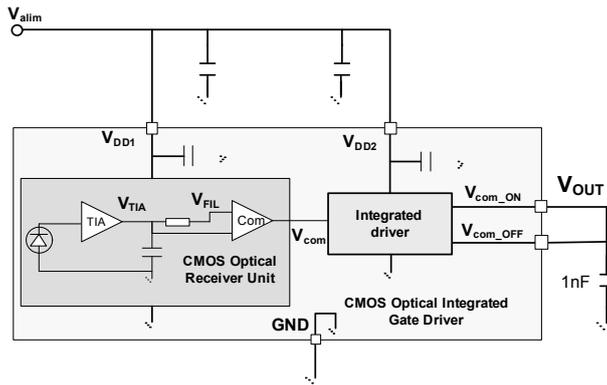


Fig.C.7 IC optical gate driver structure (Integrated photo-detector + signal process circuit + a gate driver)

In this work, a CMOS optical receiver, including a light-sensitive detector with its Signal Processing Circuit (SPC) and the output stage buffer of the gate driver are all integrated in one chip without special steps in the fabrication process while consuming less than 1mm<sup>2</sup> silicon area. A prototype is shown in Fig.C.8 with the output signal at 1 MHz in Fig.C.9.

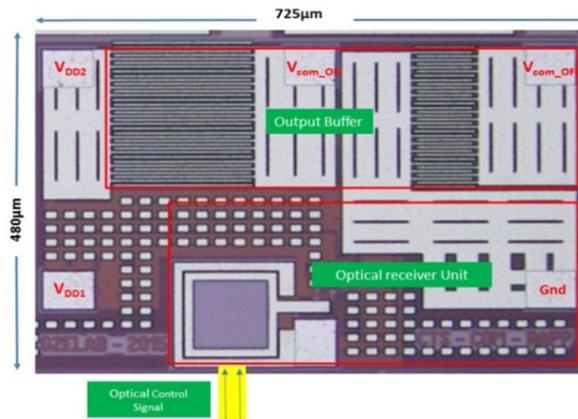


Fig.C.8 Optical microscope picture of the fabricated chip XFAB XT018

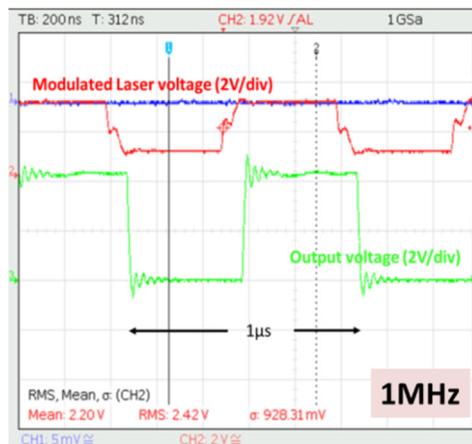


Fig.C.9 Optical microscope picture of the fabricated chip XFAB XT018

The photo-detector based on vertical *Nwell/Psubstrate* is integrated with its SPC without any specific processes (no anti-reflective coating, neither oxides nor passivation layer etching). The responsivity

and measured QE (Quantum Efficiency) of the integrated detector are measured as a function of the incident wavelength at 1V reverse bias and shown in Fig.C.10.

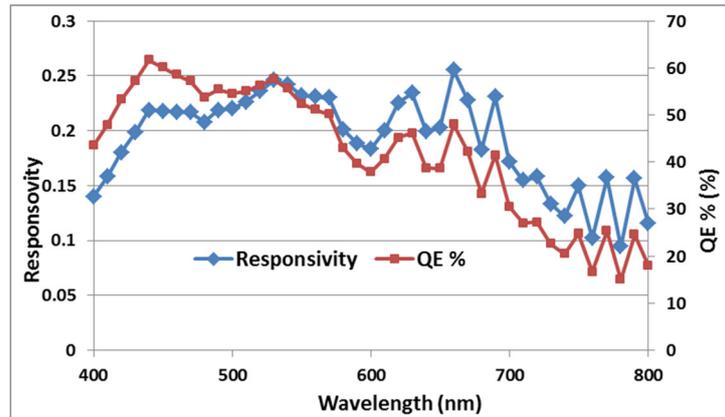


Fig.C.10 Measured spectral responsivity and QE%

The CMOS optical receiver consumes about 4mW at 4V at 25°C. The impact of the temperature on the switching specifications is studied experimentally. The results with different temperature (from 25°C to 175°C) are presented in Fig.C.11. The propagation delay between the input signal and output voltage waveforms with the output changing from low-to-high ( $t_{LTH}$ ) and the pulse-width distortion (the time difference between  $t_{LTH}$  and the propagation delay between the input signal and output voltage waveforms (of the output stage buffer) with the output changing from high-to-low ( $t_{HTL}$ ) are measured. The propagation delay between the input signal and output signal  $t_{LTH}$  is measured from 10% of the level of the input signal on the integrated photodiode to 10% of variation of the output signal  $V_{out}$  (see Fig.C.7).

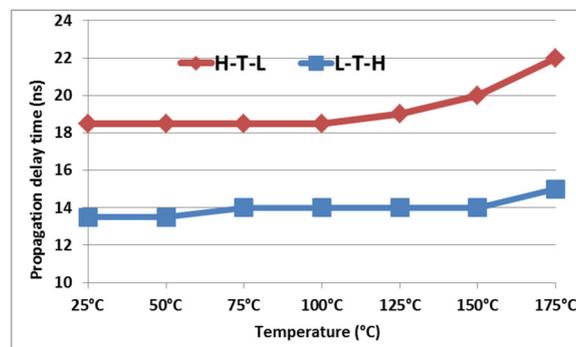


Fig.C.11 Measured turn-on and turn-off propagation delay times as a function of temperature

A fixed propagation delay of 72ns created by the chosen laser system is not included in the analysis of the gate driver. The switching frequency is fixed at 150 kHz.

The results show an increase of the propagation delay of about 4ns and a variation of the pulse width distortion of 3ns as function of the temperature. The results show the possibility, for this circuit, to drive a power component at high temperature. If this technic is expected to be the most immune to  $dv/dt$ , however, the results will be presented lately.

**Résumé:** Le projet de thèse s'inscrit dans le consortium industriel académique MEGAN (More Electric Gallium Nitride) réunissant de nombreux industriels français, grands groupes et PME (Renault, Schneider Electric, Safran, IDMOS, Valeo...) et académiques (G2Elab, Ampère, SATIE...) et le CEA. Le projet consiste à introduire de nouvelles technologies de composants de puissance à base de matériaux en GaN afin d'augmenter les performances des convertisseurs statiques pour divers types d'applications. La thèse est intégralement focalisée sur la partie Driver intégré de composants GaN à base d'une technologie CMOS SOI XFAB XT018 pour favoriser l'utilisation des systèmes à haute fréquence et haute température. La thèse consiste à étudier des architectures des drivers et des fonctionnalités innovantes permettant de limiter les problèmes inhérents à la haute fréquence et la haute température (Compatibilité Électro Magnétique - CEM, pertes de commande par courant de fuites, limites fonctionnelles...). Suite à l'étude des architectures à l'échelle du bras d'onduleur à base de composants discrets, un circuit intégré est conçu en collaboration avec les partenaires du projet. Le circuit intégré est alors réalisé avant d'être caractérisé puis mis en œuvre dans des démonstrateurs dans le cadre du projet.

En particulier, des caractéristiques de réponses en fréquence et de tenue en température sont proposées. La mise en œuvre est conduite au sein même du module de puissance intégrant les composants de puissance en GaN, au plus près de ceux-ci pour favoriser les fonctionnements à haute fréquence. Le démonstrateur final peut servir plusieurs types d'applications de part sa versatilité. Le travail de thèse est alors plus spécifiquement orienté sur l'étude du comportement haute fréquence du driver et de l'ensemble interrupteurs avec fortes vitesses de commutation / drivers d'un bras d'onduleur.

**Mots-clés:** CEM, GaN, Gate driver intégré, CMOS, XFAB XT018, Architecture de gate driver

**Abstract:** This Ph.D work is part of the industrial academic project MEGaN (More Electric Gallium Nitride) involving many French companies (Renault, Schneider Electric, Safran, ID MOS, Valeo, ...), academic institutions (G2Elab, Ampere, SATIE ...) and CEA. MEGaN project aims are to introduce a new technology of the power components based on GaN materials, to increase the performance of the static converters for various applications. This research is highly focused on the integrated driver and other power device peripheral units for GaN-based components. This is done in SOI CMOS XFAB XT018 technology to promote performing in high-frequency and high temperature applications. It involves examining driver's architectures and features, innovative methods to limit problems inherent in high frequency and high temperature (conducted EMI perturbation, delay mismatch, functional limitations ...). After studying the architecture at the scale of the discrete circuits, the integrated circuits are designed in collaboration with the project partners. The integrated circuit is manufactured by foundry XFAB before being characterized and implemented.

In particular, the characteristics at high frequency response and high temperature compliance are proposed. The final implementation is conducted in the hybrid power module power with the power components GaN, as close as possible to those for operation at high frequency which is presented in the end of this thesis. The final demonstrator serves several kinds of applications because of its versatility. The thesis is specifically focused on the study of high frequency behavior of the driver and power switches with high switching speed / the driver's components of an inverter leg.

**Keywords:** EMI/EMC, GaN, Integrated gate driver, CMOS, XFAB XT018, Gate driver architecture