Millimeter-wave phase shifters based on tunable transmission lines in MEMS technology post-CMOS process

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Déphaseurs en bande millimétrique basés sur des lignes à ondes lentes accordables en technologie MEMS dans un process post-CMOS.

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A mes parents,

A mes sœurs,

A mes frères,

A ma grande mère "Zaynab".

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Introduction

The wireless sensor networks for present consumer applications requires improved capabilities of wireless systems, including extremely high data rate, increased security, reduced electromagnetic interference, extreme miniaturization and low power consumption but with low cost. These applications include wireless personal area networks (WPAN), wireless high-definition video distribution, point-to-point links, automotive radars, backhauling. Due to congested aspect of the low frequency bands, these applications are moving to a significantly higher region of the frequency spectrum, at the millimeter-wave range.

To achieve well distributed point-to-point communication, most Wi-Fi applications at mm-wave require phased arrays. Phased arrays allow long communication range and minimize power consumption. A phased array is composed of an array of antennas in which the relative phases of the respective signals feeding the antennas are set to reinforce the radiation pattern in a desired direction and suppressed in other. In that context, phase shifters constitute the main challenge. Several technologies have been used to develop phase shifters at mm-wave for the consumer market, including CMOS, BiCMOS, BST, Liquid Cristal and MEMS. The present state-of-the-art shows that the phase shifters either consume high amount of power or occupy large surfaces and with significant insertion loss.

Due to the poor quality factor of varactors above 30 GHz frequency range it does not constitute a well-suited tunable element. MEMS technology is preferable in terms of electrical performance, but lead to large foot-print areas. In that context, tunable integrated slow-wave coplanar waveguides (S-CPWs) offer many advantages since (i) the floating shield of S-CPWs offers an additional degree of freedom for design purpose, (ii) S-CPWs exhibit inherently good quality factor, above 40, due to their strong slow-wave effect, and (iii) they present a high miniaturization factor (about 3 compared to classical non-slow-wave transmission lines).

The aim of the present thesis is to develop a distributed-MEMS phase shifter based on tunable slow wave CPW in BiCMOS technology. The phase tunability of the S-CPW can be achieved by etching the material between the floating shield and the CWP strips of the S-CPW. According to the voltage difference applied between floating shield and CPW strips, the shield can move, likely as in a NEMS. Note that tunability has already been demonstrated with such etched components by replacing the removed part with liquid crystals. In this thesis, a post-CMOS etching process has been applied to demonstrate good tunability without liquid crystals, thanks to the electromechanical effect.

In the first chapter, after explaining the principle of phase shifters and their applications, we will describe the existing technologies before presenting the background of tunable phase-shifters based on Slow-wave CPW. We will justify with a brief discussion the use of MEMS technology with a post-CMOS process (0.25 µm BiCMOS technology from IHP, Germany) and we will introduce the main objectives of this thesis.

In the second chapter, a brief review about RF-MEMS switches (i.e. ohmic switches and capacitive switches) and the electrostatic actuator will be carried out. Then, the simulated electrical performance of S-CPW in 0.25 µm BiCMOS technology will be presented. A new design topology of tunable S-CPW (TS-CPW) will be proposed. This proposed topology will be optimized in order to get good performance in terms of quality factor and insertion loss.

In the third chapter, the proposed TS-CPW will be used to design a distributed-MEMS phase shifter. A 1-bit phase shifter is first proposed by regrouping the floating ribbons of the TS-CPW, followed by the presentation of the design methodology used to design a digital phase shifter with N-bit of resolution and N-commands. The proposed methodology is then used to design a 3-bit phase shifter working at 60 GHz.

In the last chapter, the first measurement results of the distributed-MEMS phase shifter will be presented, and compared to the state-of-the art. Finally, a brief study about the parasitic effect of the substrate is made, followed by a solution in order to solve this issue.

Chapter 1

Mm-wave phase shifters: overview and state-of-the-art

Among the large number of integrated circuits in millimeter waves (mm-waves), phase shifter (PS) is a fundamental device of front-end transceivers. It is also the most important component in phased arrays for adjusting the phase on each antenna in order to achieve adaptive beam-steering.

Phase shifter can be passive or active with digital or analog tuning. It can be controlled electrically, magnetically or mechanically, and can be realized in various technologies with different topologies. Only passive phase shifters are considered in this thesis. The term “passive” will not be precised each time alongside the manuscript.

In this chapter, we present first an overview about several topologies of phase shifters and their recent applications in mm-waves. Then, a state-of-the-art on tunable phase shifters is carried out, classified according to the various technologies that can be used for tunability. In particular, a tunable phase shifter based on slow wave transmission lines is described. This technique is called distributed MEMS. Finally the description of the former and actual technologies in which the distributed MEMS approach has been developed at IMEP-LaHC is proposed, with a specific focus on IHP technology that was particularly studied and used during this PhD thesis.

1.1.Overview

1.1.1. Principle

The difference in phase angle between the input and the output signals of a 2-port device is expressed by the insertion phase angle φ, as illustrated in Figure 1-1. The S-parameters of the transmission mode can be given by eq. (1-1) when perfect matching and lossless network are considered.

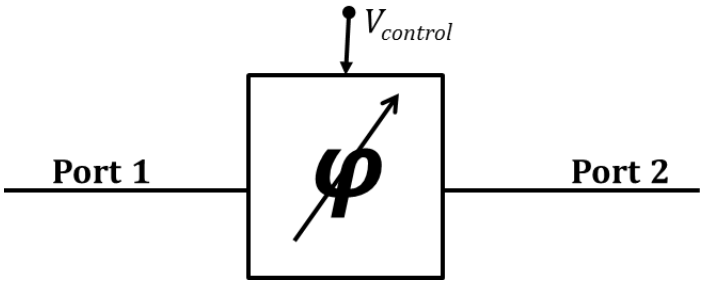


Figure 1-1: Phase shifter (transmission mode).

$$[S] = \begin{bmatrix} 0 & e^{j\varphi} \\ e^{j\varphi} & 0 \end{bmatrix} \quad \textbf{(1-1)}$$

The difference between two insertion phase angles (when an array of phase shifters is considered) or between an insertion phase angle and a reference phase angle (when making the insertion phase angle to vary) defines the relative phase shift that is expressed by eq. (1-2).

$$\Delta\varphi = \varphi_2 - \varphi_1 \quad \textbf{(1-2)}$$

An important parameter is the figure of merit (FoM in °/dB), defined as the maximum phase shift ($\Delta\varphi_{max}$) divided by the maximum insertion loss (IL_{max} in dB) (See eq. (1-3) and (1-4)).

$$IL = -20log_{10}S_{21} \quad \textbf{(1-3)}$$

$$FoM = \frac{\Delta\varphi_{max}}{IL_{max}} \quad \textbf{(1-4)}$$

Phase shifters may have analog or digital tuning. Analog phase shifters generate a continuous phase shift like the voltage-controlled phase shifter, which is controlled by varactor diodes. Digital phase shifters provide a discrete set of phase shifts. It discretizes the absolute phase into predetermined phase states, and the different phase states can be changing by digitally controlling each phase-shifter bit. It is an important issue to switch to different states of the digital phase shifter precisely. They are many methods to carry out a digital phase shifters, in this thesis; we are interested for digital phase shifter using the microelectromechanical systems (MEMS) to realize its switch.

1.1.2. Applications

Phase shifters are used in several applications. At mm-wave frequencies, the most important application is within a phased array antenna and reconfigurable antenna architecture for consumer applications such as wireless personal area networks (WPAN), wireless high-

definition video distribution, point-to point links, automotive radars and wireless sensor networks in general. Other applications of phase shifters include RF and microwave measurement instrumentation, PA linearizers, voltage controlled oscillator (VCO) and small-shift frequency translators [1] [2] [3]. Three main applications are presented herein: the tunable antenna phased array, the Butler matrix and the VCO.

A phased array is composed of an array of antennas in which the relative phases of the respective signals feeding the antennas are set in such a way that the effective radiation pattern of the array is reinforced in a desired direction and suppressed in all undesired ones. The phase relationships among the antennas can be fixed or adjustable by using tunable phase shifters, as for beam steering. Adding a phase shift to the signal received by each antenna in an array of antennas permits the common signal of these individual antennas to act as the signal of a single antenna with performance greatly different from the individual antennas in the array. In Figure 1-2, tunable phase shifters are integrated in an optimized design of a low-cost phased array antenna.

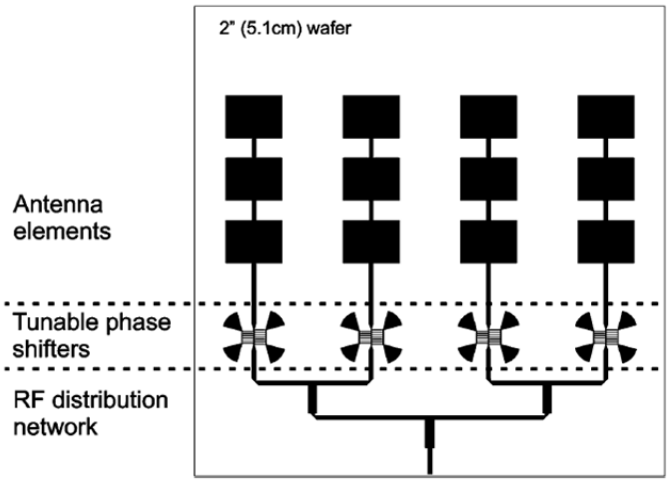


Figure 1-2: Phased array antenna using tunable phase shifters [4].

One application for phase shifters is the Butler matrix, offering beam forming and scanning network capabilities. The Butler matrix is a microwave network, constituted of couplers and phase shifters. Figure 1-3 illustrates the block diagram of a 4x4 Butler matrix. Thanks to a switching network upstream, the input signal enters one of the four input ports. Depending on the input port, the Butler matrix produces a different phase taper among the output ports. The phase shifts at the output ports can be determined by combination of the phase shifts of all the signal paths. A Butler matrix may feed an antenna array for beam steering capabilities, as on Figure 1-3

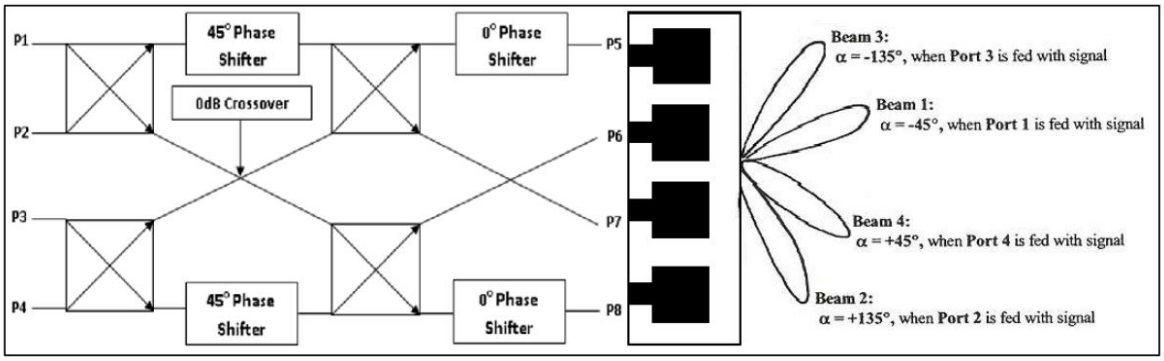


Figure 1-3: Block diagram of a 4x4 Butler matrix [5] using phase shifters.

A voltage controlled oscillator (VCO) is one of the most important circuits in wireless communication systems as a part of frequency synthesizers. A classical VCO is implemented by using a $LC\nearrow$ tank to generate signals at a particular frequency. Frequency control is traditionally achieved through a varactor diode or a variable MOS capacitance, etc., but power consumption is a special concern for portable devices using VCOs. This is the reason why some researches started a few years ago to implement PSs (mostly passive PSs) in VCOs due to their low power consumption to replace the conventional $LC\nearrow$ resonator. For example, Figure 1-4 shows a common collector Colpitts VCO using a tunable phase shifter as the frequency tuning component. This is a non-conventional use for phase-shifters. Here, to realize a tunable VCO, a voltage controlled analog phase shifter (tunable phase shifter) is placed between the input of the common collector Colpitts oscillator and ground.

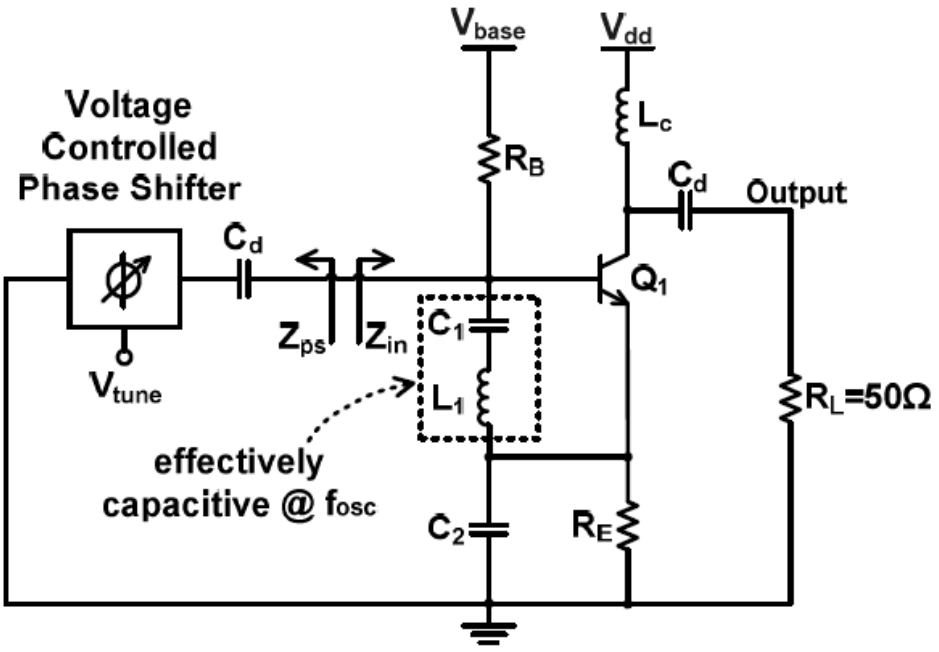


Figure 1-4: Common collector Colpitts VCO using tunable phase shifter [6].

1.1.3. Topologies

In this sub-section, we present three topologies to perform phase shifting:

- Reflection type phase shifter (RTPS),
- Loaded-line phase shifter,
- Switched-line phase shifter,

The first kind of phase shifter is the reflection type phase shifter (RTPS), which was proposed for the first time in 1960 by [8]. Figure 1-5(b) presents a RTPS that is composed of a branch-line coupler (Figure 1-5 (a)) loaded by two varactors Z_L.

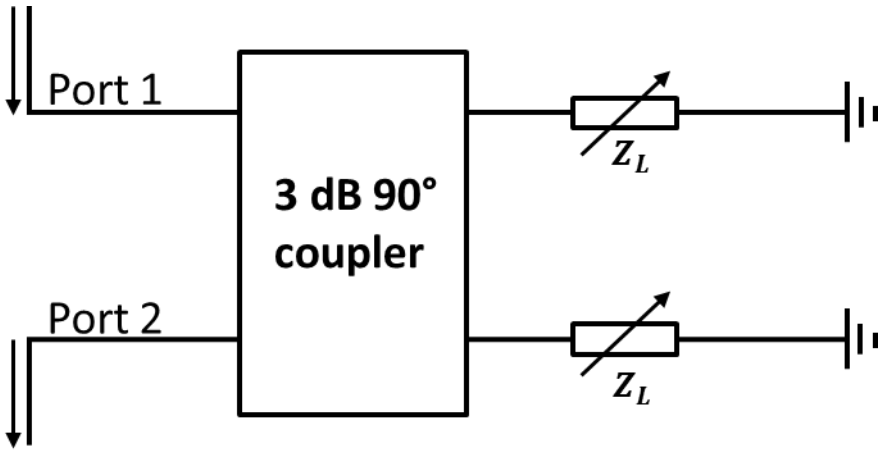


Figure 1-5: RTPS loaded by varactors.

An ideal reflection load (here a reactance $Z_L = 1/jc\omega$) can be considered as a single-port circuit with a reflection coefficient of magnitude unity and a relative phase shift. The phase angle of the transmission coefficient between ports 1 and 2 is expressed in eq. (1-5).

$$\varphi = \pi - 2\text{atan}(\frac{Z_L}{Z_0}) \quad \textbf{(1-5)}$$

where Z_0 is the port impedance.

The relative phase shift obtained from the tunable reactance (z_{Lmin}, z_{Lmax}), is given by eq. (1-6).

$$\varphi = 2[\text{atan}\left(\frac{Z_{Lmin}}{Z_0}\right) - \text{atan}\left(\frac{Z_{Lmax}}{Z_0}\right) \quad \textbf{(1-6)}$$

The second type of phase shifters is based on a loaded-line topology, which is used to tune the characteristics of a transmission line. The basic form for the loaded-line phase shifter is a transmission line possessing characteristic impedance (Z_T) and electrical length (θ), periodically loaded with reactive loads (shunt or series). The relative phase shift is obtained when the impedance of loads is changed, as shown in Figure 1-6.

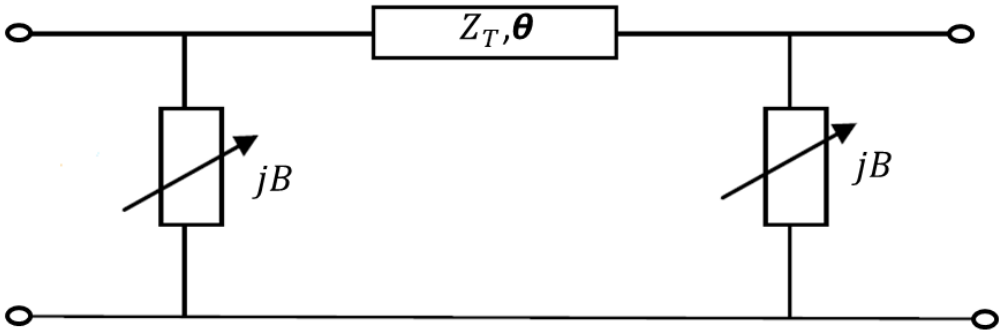


Figure 1-6: Loaded-line phase shifter with a shunt-coupled load.

Switched-line phase shifter (or switched delay-line phase shifter) is another kind of phase shifter, which consists of n delay lines, connected each side by a single-pole-n-throw (SPnT) switch. A switched-line phase shifter using two single-pole double throw (SPDT) switches is illustrated in Figure 1-7.

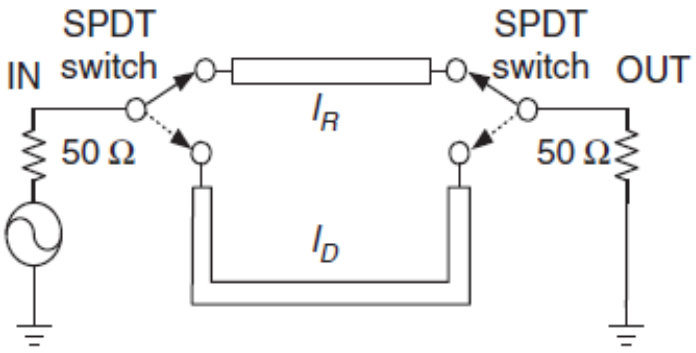


Figure 1-7: Switched-line type phase shifter [9].

This type of phase shifter has one disadvantage that is the interruption of the signal during the transmission, and this may be a problem in some communication applications, where protocols do not devote time for this interruption.

1.2.State-of-the-art

In this section, we present the state-of-the-art of passive phase shifters at mm-waves. Four technologies available at mm-waves are described:

- Ferroelectrics,
- Liquid crystals,
- Silicon (CMOS/BiCMOS),
- MEMS.

1.2.1. Ferroelectrics

Ferroelectrics are non-linear materials, but their main characteristic is the high and tunable relative permittivity. Several materials are available: Barium-Strontium-Titanate (BST), Potassium-Niobium-Titanate (KTN) or Lead-Zirconium-Titanate (PZT). The BST is the most popular ferroelectric material used in various microwave devices, such as phase shifters, filters, etc., because it has low dielectric losses, high tunability and low coercive field, thus reducing the hysteresis effect and simplifying the electric command [19].

A 360° phase shifter in the Ka-band with a moderate bias voltage using BST material was proposed in [20]. The phase shifter consists of a CPW for (CoPlanar Waveguide) periodically loaded by interdigitates BST capacitors (Figure 1-8). This design is also used by [21].

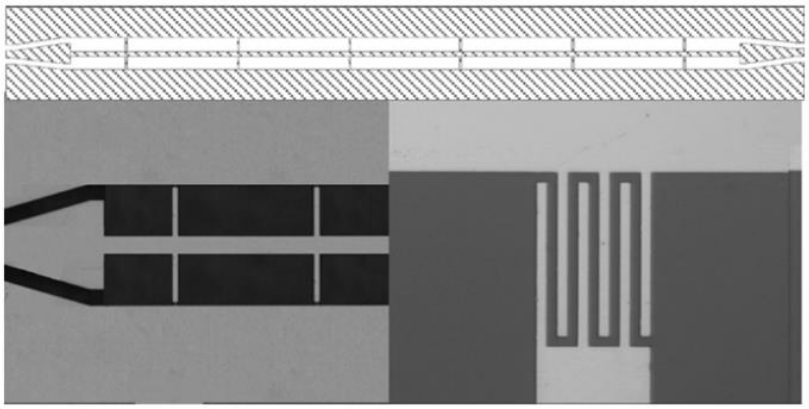


Figure 1-8: Schematic and optical views of the phase shifter proposed in [20].

The measured insertion loss of the proposed phase shifter is around 0.8 dB at low frequencies (1 to 5 GHz) and 3.6 dB at 30 GHz. The return loss is better than 12 dB in the entire frequency range which shows a good matching of this circuit. The maximum value of phase shift is 310° with a DC voltage of 35 V, leading to a figure of merit of 85°/dB.

The phase shifter proposed in [22], based on [23] and [24], is based on a high impedance CPW loaded with 12 identical MIM capacitors. It represents the first tunable phase shifter based on BST MIM capacitors working at 60 GHz. The schematic of the phase shifter and the design of a MIM capacitor are given in Figure 1-9.

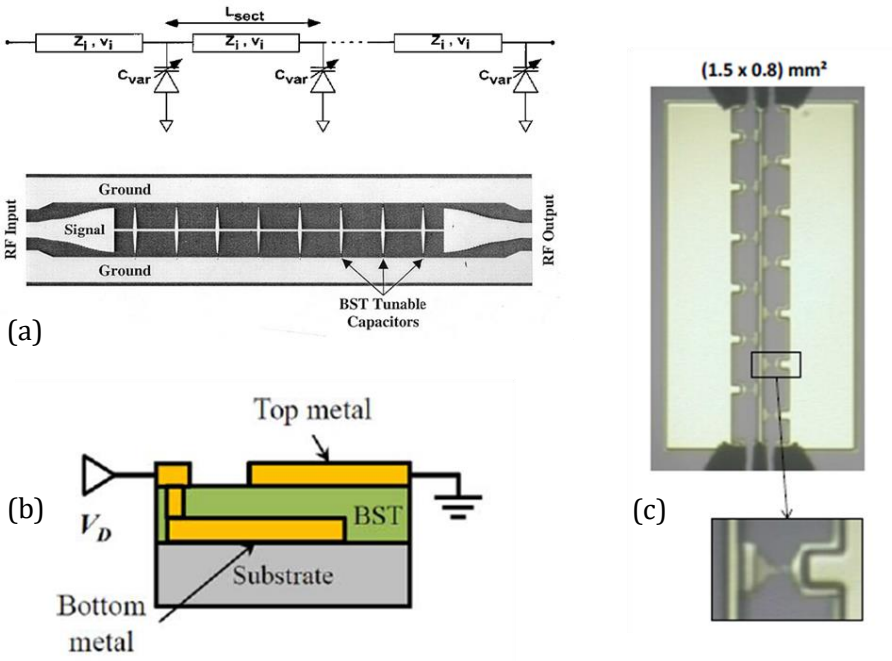


Figure 1-9: (a) Circuit schematic photograph of the fabricated phase shifter [24], (b) example of MIM capacitor [22] and (c) photograph of the BST tunable phase shifter, and of the MIM capacitor [23].

The measured electrical characteristics of the phase shifter are 12 dB and 5.9 dB for return loss and insertion loss, respectively. When varying the applied voltage from 0 to 90 V, the maximum value of phase shift is 150° at 60 GHz, which gives a FoM of 25°/dB.

Few instances of phase shifter based on BST MIM capacitor working at 60 GHz are available in the literature. Table 1-1 presents the state-of-the-art of passive phase shifters in BST technology working at 30 GHz and 60 GHz.

Table 1-1: State-of-the-art of passive phase shifters based on ferroelectrics.

Ref	Frequency (GHz)	Area (mm^2)	Max. IL. (dB)	Return Loss (dB)	Phase shift (°)	FoM (°/dB)	FoM/Area (°/mm^2)
[20]	30	7	3.6	12	310	85	44
[22]	60	1.2	5.9	12	150	25	125
[24]	30	NA	5.8	12	157	27.1	NA
[25]	60	33	10	5.5	220	22	6.6

Due to the high dielectric losses (in literature tan δ is 0.07, 0.13 and 0.2 in [27], [28] and [23], respectively) in the mm-waves, the FoM remains quite low at 60 GHz.

1.2.2. Liquid crystal

Liquid crystal (LC) is an anisotropic material, which exhibits two different permittivities depending on molecule direction. In between their solid and liquid states it has, depending on the LC mixture used, different mesophases such as the smectic and the nematic phase [26]. The nematic liquid crystal (LC) can be employed as a tunable dielectric in the microwave devices.

In [29], two LC-based phase shifters working in the 60 GHz band were presented. The first one is a meandered line phase shifter (MLPS) and is illustrated in Figure 1-10(a). It is based on a microstrip line with CPW transitions, as detailed in [30]. These transitions are proposed in order to provide low reflection as well as DC connectivity to the conductor pattern exposed to LC.

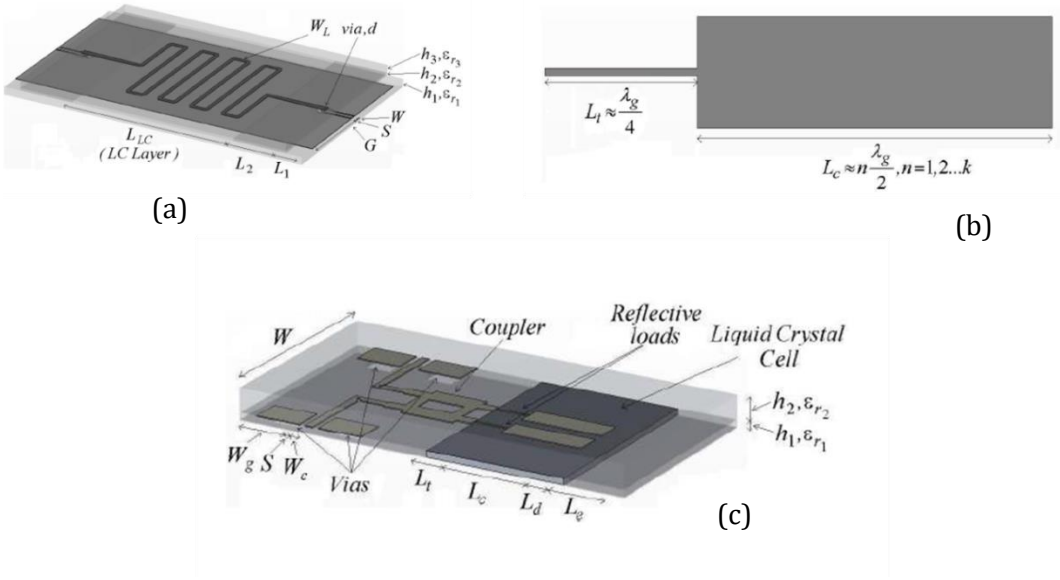


Figure 1-10: Structure of (a) LC-based MLPS for 60 GHz band, (b) reflection load and (c) LC-based RTPS for 60 GHz band [29].

The second phase shifter is a RTPS (Figure 1-10(c)) composed of a 3 dB hybrid coupler and two reflective loads (Figure 1-10(b)) exposed to the LC layer. When a bias voltage is applied through the probe pads to the conductor, the LC molecules change direction beneath the electrode. This changes the effective dielectric constant, and hence a variation of the reactance of the reflective loads and a differential phase shift occur.

The measured phase shift of the MLPS and the RTPS for an applied bias voltage of 11 V is 240° and 150°, with a return loss of 14 dB and 10 dB, respectively. The figure of merit is 20°/dB for the MLPS and 11°/dB for the RTPS. However, the advantage of the RTPS is its size. It occupies an area nearly 4 times lower than the MLPS.

Another phase shifter based on liquid crystal was proposed in [31]. The topology of a two layers microstrip meander line LC-based phase shifter is shown in Figure 1-11. This phase shifter is interesting owing to its planar structure and compact design. The total length of the phase shifter exposed to the LC is around 7 mm. Three phase shifters in series are implemented to design the four-element array.

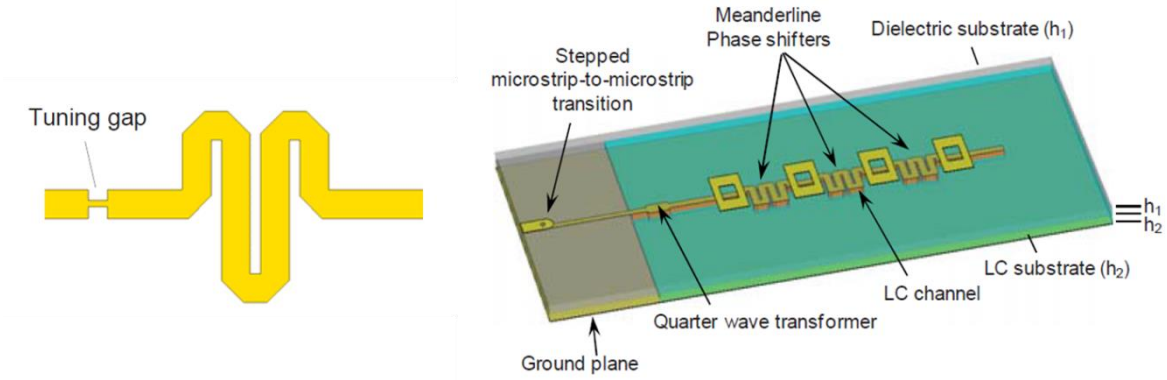


Figure 1-11: (a) Meander line phase shifter and (b) four-elements array including meander line phase shifter [31].

An insertion loss of 11 dB and a return loss of 12 dB were observed. The maximum value of phase shift was 47°, leading to a figure of merit around 4°/dB.

In [32], a LC phase shifter with a stripline configuration is integrated in a LTCC technology (for low temperature cofired ceramic), a low loss multilayer technology. The LC is an available commercial solution, as compared to the special LC solution used by the same team in [33], together with a standard inverted microstrip in a TMM3 technology (a low permittivity composite ceramic substrate). In [32][33], the figure of merit at 24 GHz was as high as 110°/dB, but the used LC solution might suffer from badly aging which does not seem the case in [32]. What's more, the topology suffered from large response time, which was in the order of minutes depending on the LC material and layer thickness. These are the two reasons why this work has not been referred to in Table 1-2.

Figure 1-12(a) describes the stripline topology used in [32], where the ground plane has the same width as the signal line. A photograph and 3D-model of the LTCC based LC stripline phase shifter are shown in Figure 1-12(b) and Figure 1-12(c). Experimental results between 30 and 34 GHz give a return loss equal to 10 dB, and a worst insertion loss of 6 dB and 8 dB, at 30 GHz and 34 GHz, respectively. The phase shift is 61°, leading to a FoM of 10°/dB at 30 GHz. De-embedding of these results highlights that the FoM of the phase shifter increases to 13°/dB at 30 GHz.

In [34], the same team associates with IMEP-LaHC on a commercially available LC solution. The phase shift effect is high but conjugated with a distributed-MEMS effect which leads to a very interesting FoM of 51°/dB at 45 GHz. In [35], in 2005, the aim was to test a specific solution, with similar benefits and disadvantages than in [33]. The FoM is thus very interesting but the PS presents an *off-time* still superior to 10 s.

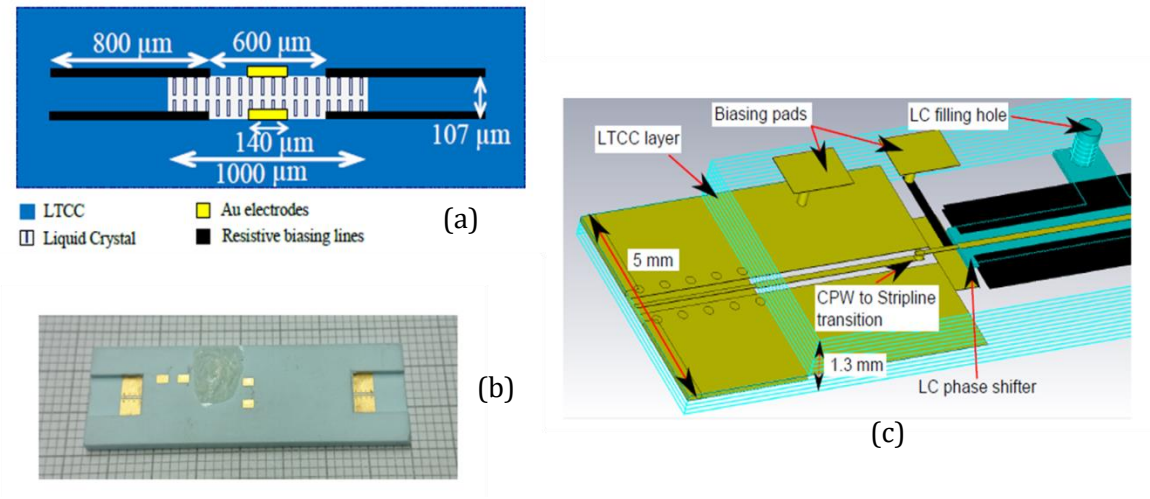


Figure 1-12: (a) Schematic cross section of the stripline LC phase shifter, (b) photograph of the LTCC-based LC phase shifter device and (c) 3D-model of the phase shifter realized in LTCC technology [32].

Main results for phase shifters using liquid crystal technology are presented and compared in Table 1-2.

Table 1-2: State-of-the-art of passive phase shifters based on liquid crystal.

Ref	Frequency (GHz)	Area (mm²)	Max. IL. (dB)	Return Loss (dB)	Phase shift (°)	FoM (°/dB)	FoM/Area (°/mm²)
[29]	60	128	11.6	14	243	20	1.89
[31]	60	NA	11	12	47	4	NA
[32]	30	>15	6	10	60	13	NA
[34]	45	0.38	5	NA	275	51	723
[35]	40	NA	4.8	10	303	63	NA

1.2.3. CMOS/BiCMOS

In recent years, devices based on silicon in CMOS/BiCMOS technologies have dominated the integrated circuits applications. Thus, in this sub-section we describe the main results carried out in these technologies.

In [36], three different passive and active phase shifters were designed and fabricated in a standard 1P7M 90 nm CMOS process. Here, we present only the passive phase shifter used in the

frequency range from 50 to 56 GHz for a passive quadrature generator. This phase shifter is of RTPS type. It consists in a coupled-line coupler loaded by shunts varactors. The schematic diagrams and the photographs of the phase shifter and the passive quadrature generator are shown in Figure 1-13 (a), Figure 1-13(b), Figure 1-13(c) and Figure 1-13(d), respectively.

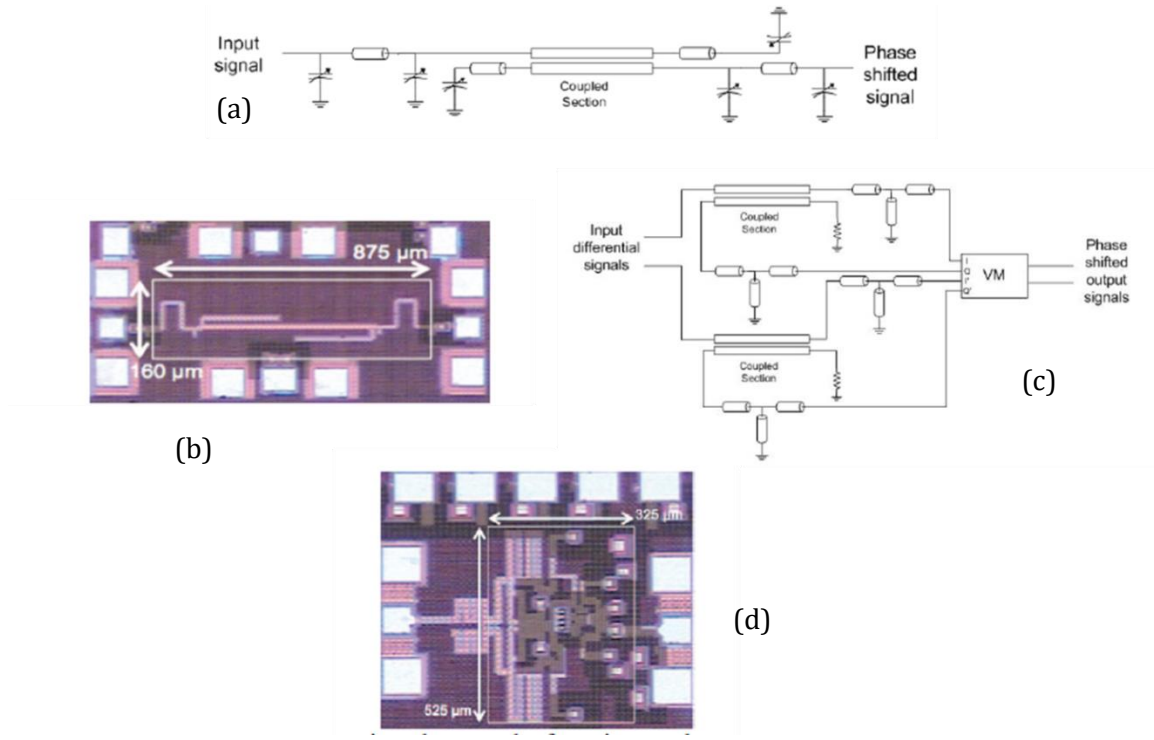


Figure 1-13: (a) Schematic of the phase shifter, (b) chip microphotograph of the passive phase shifter, (c) schematic of the quadrature generator with VM and (d) chip microphotograph of the quadrature generator based phase shifter [36].

Insertion loss of 16.75 dB and phase shift of 141° were obtained, leading to a FoM of 8.4°/dB.

A 4-bit passive phase shifter with phase resolution of 22.5° for automotive radar applications operating in the frequency range from 67 to 78 GHz was designed in a 0.12 µm BiCMOS process (IBM 8HP) in [37]. It consists of a low-pass π-network and CMOS passive switches. All inductors that form the low-pass π-network were implemented with a grounded CPW as shown in Figure 1-14 (a). Figure 1-14 (b) presents the schematic of the 4-bit digital phase shifter made of two 90° phase shifters tied together to form 180° phase shifting in series with 22.5°, 45° and 90° phase shifters.

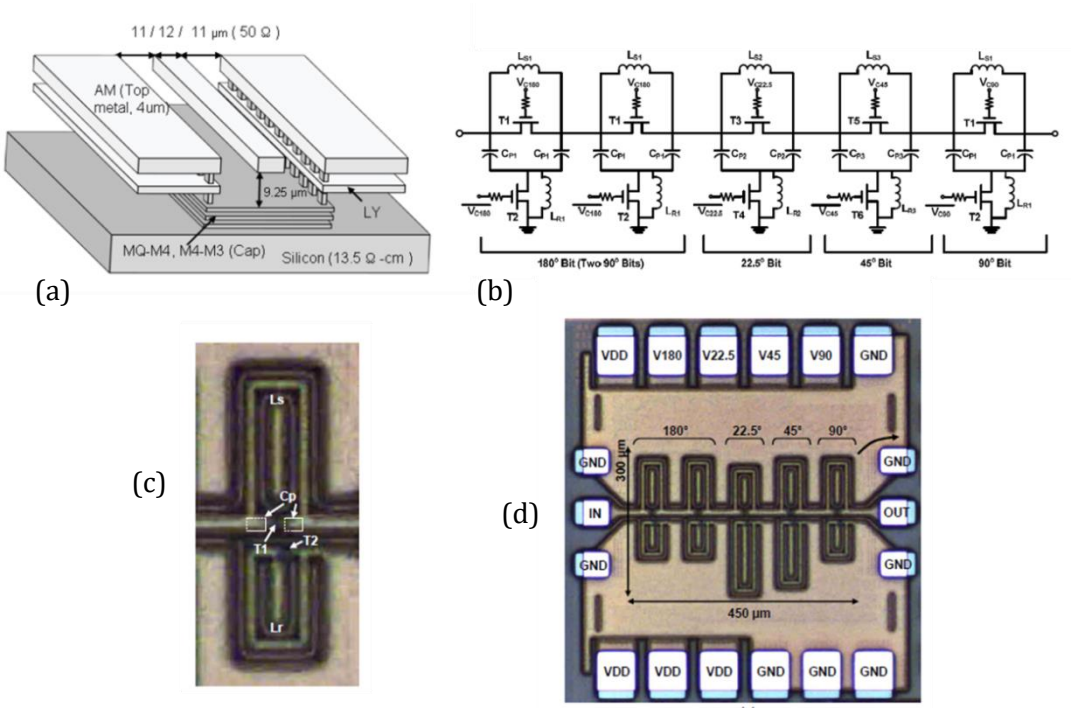


Figure 1-14: (a) The grounded-CPW, (b) schematic of the 4-bit digital phase shifter, (c) chip photograph of the 90°phase shifter cell and (d) chip photograph of the 4-bit digital phase shifter [37].

This digital phase shifter was measured up to 110 GHz with return loss of 10 dB for all 16 different phase states from 68 to 81 GHz. The highest value of phase shift was 337° with a maximum insertion loss of 19 dB, leading to a FoM equal to 17.7°/dB.

A summary of the main characteristics of phase shifters implemented in CMOS/BiCMOS technologies is carried out in Table 1-3.

Table 1-3: State-of-the-art of passive phase shifters in CMOS/BiCMOS technologies.

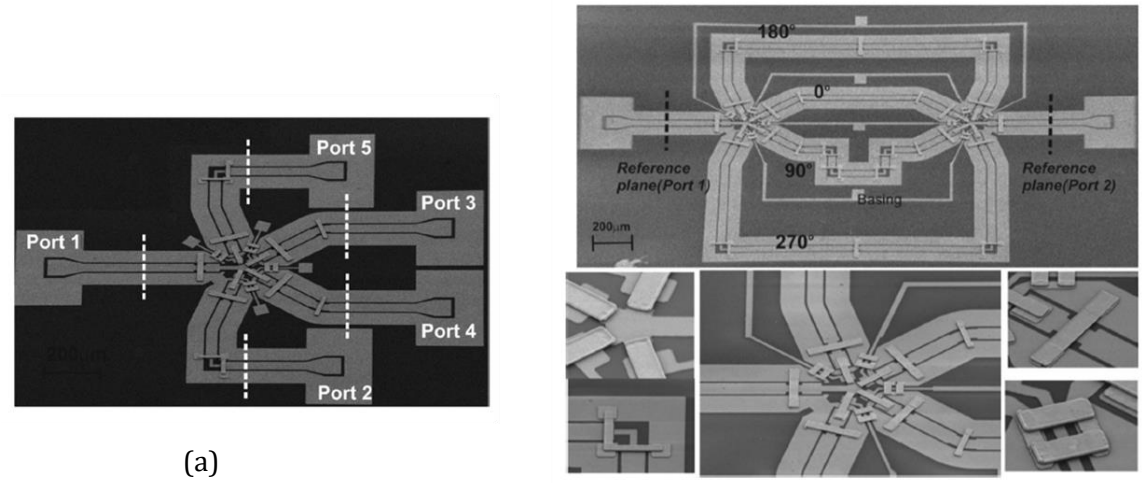
Ref/technology	Frequency (GHz)	Area (mm^2)	Max. IL. (dB)	Return Loss (dB)	Phase shift (°)	FoM (°/dB)	FoM/Area (°/mm^2)
[36]/CMOS	50-56	0.14	16.7	NA	141	11.1	1007
[37]/BiCMOS	67-78	0.13	19	10	337	17.7	2596
[38]/CMOS	50-65	0.075	8	12	90	11.25	120
[40]/CMOS	50-70	3.15	4	18	135	33.7	42.8

1.2.4. MEMS

The main advantages of MEMS phase shifters are: low loss, good linearity, broadband frequency operation, large tuning ratio and good power handling capability. In addition, in recent years, MEMS devices combined with CMOS/BiCMOS technologies have paved the way of a

great revolution for mm-wave systems. In this section, state-of-the-art of phase shifters in MEMS technology with pure MEMS or CMOS-MEMS technology is described.

The design, fabrication and characterization of a 2–bit switched line phase shifter using dc-contact single-pole-quadruple-throw (SP4T) RF-MEMS switches for 60 GHz applications were investigated in [41]. The SEM of the SP4T switches and the 2-bit phase shifter are shown in Figure 1-15(a) and Figure 1-15(b), respectively.



(a) (b)

Figure 1-15: (a) SEM of the fabricated SP4T RF-MEMS switch, (b) SEM images of the fabricated V-band 2-bit phase shifter [41].

An average insertion loss of 2.5 dB in the frequency range from 55 to 65 GHz was achieved for the 2–bit phase shifter, with a return loss better than 12 dB for all 4 states (0°, 90°, 180°and 270°), leading to a FoM equal to 108°/dB when considering the maximum phase shift of 270°.

A V-band CMOS-MEMS switchable phase shifter based on reflection-type topology was proposed in [42]. The schematic of the proposed phase shifter and its images of fabrication are shown in Figure 1-16(a) and Figure 1-16 (b, c), respectively.

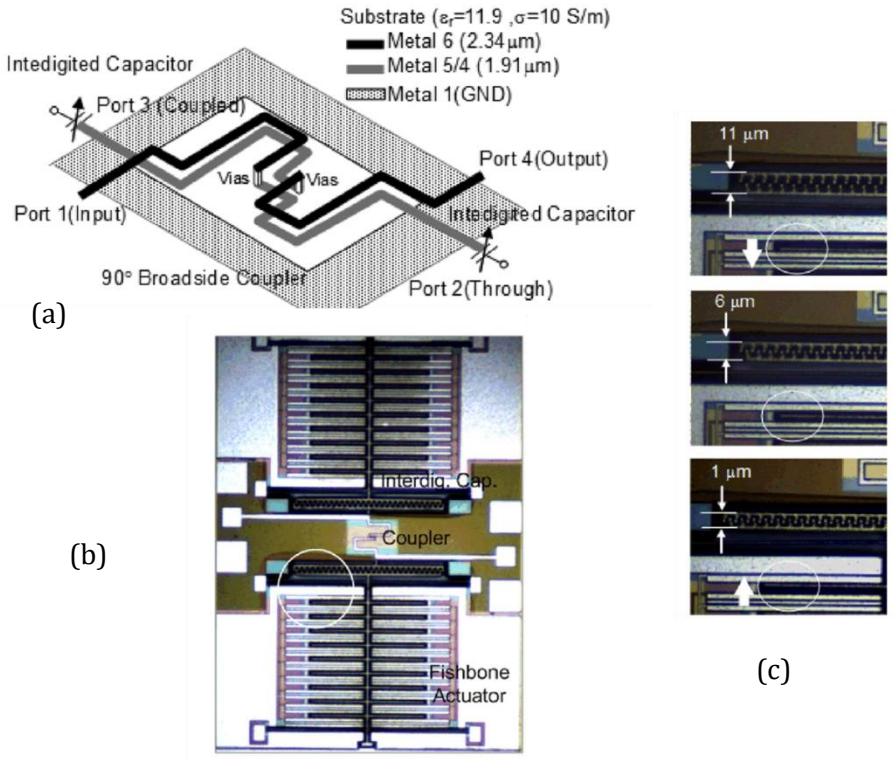


Figure 1-16: (a) Circuit schematic of the proposed reflection-type phase shifter and (b) and (c) images of the fabricated phase shifter [42].

After the fabrication of the phase shifter in a 0.18 µm CMOS technology, a post-CMOS process is necessary to release the MEMS structure. When an actuation voltage of 46 V is applied, three discrete phase states of 0°, 89° and 144° are achieved at 65 GHz. The measured return loss is better than 14 dB and the insertion loss is around 2.2 dB over the 55-65 GHz range. This performance is attributed to a specifically developed technology with an optimization of the design methodology.

Table 1-4 shows a comparison of the state-of-the-art for the phase shifters based on MEMS at mm-waves.

Table 1-4: State-of-the-art of passive phase shifters based on MEMS.

Ref	Frequency(GHz)	Area (mm^2)	Max. IL. (dB)	Return Loss (dB)	Phase shift (°)	FoM (°/dB)	FoM/Area (°/mm^2)
[41]	55-65	4	2.7	12	270	100	67.5
[42]	55-65	1	2.2	14	144	65.4	144
[43]	60	NA	2	10	118	60	NA
[44]	75-110	NA	2.7	NA	100	37	NA
[45]	50-57	3.15	4	11.7	135	33.75	42.8

1.2.5. Discussion

Table 1-5 The request for higher data rates and spectrum limitation makes 60 GHz the most promising frequency to return multi-gigabit high throughput wireless communication. This is due to its abundant multiple gigahertz license-exempt spectrum frequency and particularly for WPAN and WLAN implementation. Table 5 summarizes the main performance (FoM, insertion loss, return loss, phase shift and etc.) for 60-GHz phase shifters described in previous sections.

Table 1-5: Summary of state-of-the-art of passive phase shifters at 60 GHz.

Ref/Technology	Area (mm^2)	Max. I.L. (dB)	Return loss (dB)	Phase shift (°)	FoM (°/dB)	FoM/Area (°/ mm^2)
[22]/BST	1.2	5.9	12	150	25	125
[25]/BST	33	10	5.5	220	22	6.6
[29]/LC	128	11.6	14	243	20	1.89
[38]/CMOS	0.075	8	12	90	11.25	120
[40]/CMOS	3.15	4	18	135	33.7	42.8
[41]/MEMS	4	2.7	12	270	100	67.5
[42]/MEMS-CMOS	1	2.2	14	144	65.4	144

BST exhibits high loss tangent at mm-waves, which strongly affects the insertion loss. Liquid crystal material leads to lower insertion loss and usually a much higher FoM, but they require large areas. Very few references communicate on the area. On another hand, MEMS and CMOS phase shifters may present very high phase shift with a moderate to very low area on a chip. Due to the reasonable surface, MEMS and CMOS phase shifters exhibit a FoM (°/mm^2) two times higher than the other phase shifters implemented in other technologies. Anyway MEMS-based PS exhibit less insertion loss than CMOS-based PS but can be integrated in a CMOS process including a post-etching process. In addition, it is worth mentioning that advanced

CMOS/BiCMOS technologies are mandatory for the design of mm-wave phase shifters working at 60 GHz.

For all of these reasons, this PhD thesis will focus on a particular type of MEMS-based technologies, patented by the IMEP-LaHC laboratory, in the mm-wave frequency band. More precisely, a distributed MEMS slow wave coplanar waveguide (S-CPW) will be used as the basic element for tunability.

1.3. Solution based on slow wave transmission lines

There are several planar transmission lines such as microstrip and coplanar waveguide, which can be realized in different technologies as the printed circuit PCB and integrated CMOS/BiCMOS.

In the following sub-sections, we focus on the characteristic of a transmission line and how to make it tunable with two ways.

1.3.1. Transmission line characteristics

A transmission line (Tline) is characterized by different parameters. For a transmission line propagating a TEM mode, the telegraph model is used (Figure 1-17). R_l (Ω/m) is the linear resistance, which represents the resistive losses in the conductors, L_l (H/m) is the linear inductance, C_l (F/m) is the linear capacitance, and G_l (S/m) is the linear conductance related to the losses due to the leaks through the dielectric.

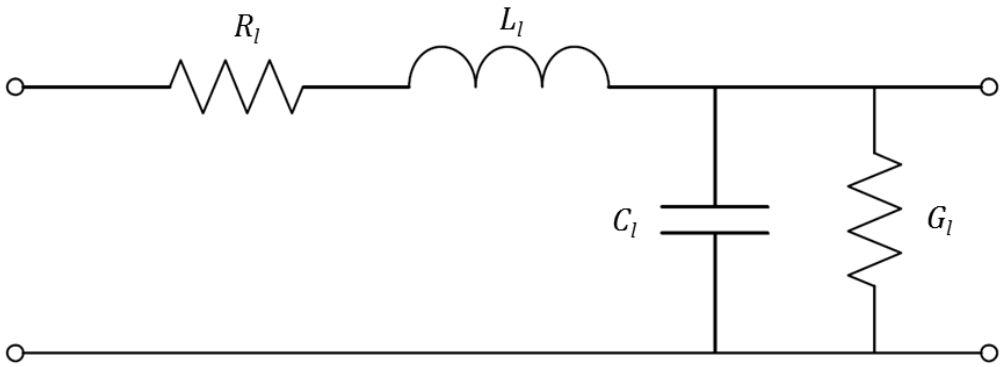


Figure 1-17: Telegrapher model (or RLCG model).

The behavior of transmission line can also be described by other parameters like the characteristic impedance Z_c and the propagation constant γ. These parameters are related to the elements of the RLCG model as expressed in eq. (1-7) and (1-8).

$$Z_c = \sqrt{\frac{R_l + jL_l\omega}{G_l + jC_l\omega}} \quad \textbf{(1-7)}$$

$$\gamma = \sqrt{(R_l + jL_l\omega)(G_l + jC_l\omega)} \quad \textbf{(1-8)}$$

The propagation constant γ is the sum of the attenuation constant α(dB/m) and the phase constant β(rad/m) as seen in eq. (1-9).

$$\gamma = \alpha + j\beta \quad \textbf{(1-9)}$$

When the Tline exhibits very low loss, R_l and G_l can be neglected, and the characteristic impedance can be considered as real, eq. (1-10).

$$Z_c = \sqrt{\frac{L_l}{C_l}} \quad \textbf{(1-10)}$$

In low-loss case, the attenuation constant α can be expressed by eq. (1-11). The phase constant β is linked to the phase velocity v_φ (m/s), eq. (1-12)(1-14).

$$\alpha = \frac{1}{2}\left(\frac{R_l}{Z_c} + G_l Z_c\right) \quad \textbf{(1-11)}$$

$$\beta = \frac{\omega}{v_\varphi} = \omega\sqrt{L_l C_l} \quad \textbf{(1-12)}$$

$$v_\varphi = \frac{\omega}{\beta} = \frac{c_0}{\sqrt{\varepsilon_{reff}}} = \frac{1}{\sqrt{L_l C_l}} \quad \textbf{(1-13)}$$

The phase shift φ (or electrical length) for a TLine is expressed by eq. (1-14).

$$\varphi = \beta . l \quad \textbf{(1-14)}$$

where l is the physical length of the TLine.

The efficiency of a Tline is defined by an important parameter called quality factor Q, given by eq. (1-15), [46] and [47].

$$Q = \frac{\beta}{2\alpha} \quad \textbf{(1-15)}$$

Eq. (1-16) can be obtained when the numerator and the denominator of eq. (1-15) are multiplied by the TLine's physical length; this gives a ratio between the phase shift and the attenuation constant.

$$Q = \frac{\beta . l}{2\alpha . l} = \frac{\varphi}{2\alpha . l} \quad \textbf{(1-16)}$$

1.3.2. Slow-wave coplanar waveguide concept

In integrated technologies, the performance of a Tline is limited by technology and price, which depends on the surface area. Some miniaturization methods have been developed in order to obtain good performances. In this section, we focus on the Slow-wave CoPlanar Waveguide called S-CPW, which is a topology that has been studied since more than ten years to reach higher quality factors than the microstrip line in integrated CMOS/BiCMOS technologies.

1.3.2.1. Concept

The classical CPW was invented in 1969 by Wen [48]. It is a planar Tline such as the microstrip, while the signal and the ground of CPW are formed on only one layer of metal. The structure of CPW is composed of the central strip for the signal and two strips for the grounds, deposited on a dielectric substrate. In order to improve the performance of the CPW, in particular the quality factor, we can reduce the losses or increase the phase constant in respect to eq. (1-15). Usually, α is imposed by the technology used for fabrication, so the solution is to increase β without changing the fabrication process. From eq. (1-13), with increase in β , the phase velocity decreases, and then the capacitance or the inductance increases. Thus, we can increase the capacitance by loading the CPW with shielding ribbons, also called fingers or sometimes shielding strips, without varying the inductance. This shielding layer is floating; it is made of metallic strips of width SL (for Shielding ribbons Length), which are separated by a gap SS (for Shielding ribbons Spacing). The spacing between the CPW strips' plane and the shielding layer plane is given by h. The topology of a S-CPW is shown in Figure 1-18.

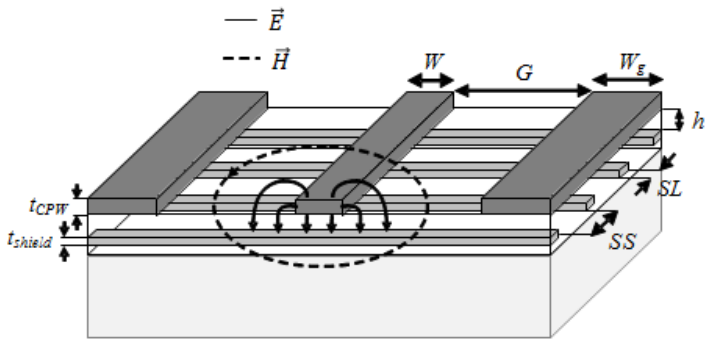


Figure 1-18: Topology of the slow-wave coplanar waveguide

As shown in Figure 1-18, the magnetic field passes through the spaces between the shielding strips. This leads to an inductance per length unchanged as compared to a classical CPW, whereas the electrical field lines end at the shielding strips; electrical field is concentrated between the CPW strips and the shielding strips. Thus, the capacitance per length is increased as compared to a classical CPW.

1.3.2.2. Electrical model

Eq. (1-17) describes the total capacitance ($Ctot$) of the S-CPW constituted of the capacitance between the CPW strips and the shielding layer, CW, in series with the capacitance between the CPW ground and the shielding layer, CWg. To model the conductive loss that occurs in the shielding strips, a resistance $Rstrips$ is added in series with$Ctot$. The total resistance $Rtot$ is given by eq. (1-18).

$$Ctot = \frac{2.CW.CWg}{CW + CWg} \quad \textbf{(1-17)}$$

$$Rtot = \frac{Rstrips}{2} \quad \textbf{(1-18)}$$

The RLCG model for CPW is not sufficient to evaluate the full behavior of S-CPW when losses are considered. Therefore, a new electrical model based on the physical behavior of the S-CPW was proposed in [49]. It is shown in Figure 1-19. The magnetic field has the same spatial distribution in a S-CPW and in a classical CPW; hence the modeled inductance L_l is similar for both topologies possessing the same geometrical dimensions.

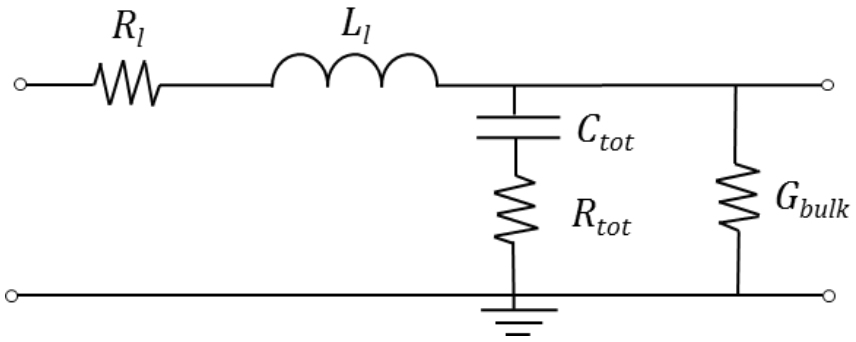


Figure 1-19: Proposed equivalent model for S-CPW.

In practice, the dielectric loss G_{bulk} due to the substrate is negligible because the electrical field is blocked by the shielding layer. Hence G_{bulk} is due to silicon oxide layers only that present low dielectric losses and can be avoided in the model. In order to fast compute the electrical performances of a slow-wave CPW, an analytical method was developed in [50] and [51].

1.4.Tunable slow-wave transmission lines

More than five years ago, several research projects have started at IMEP-LaHC based on a totally innovative technology of tunable S-CPW. Make this TLine tunable is proposed in two patents in 2011 [52] and 2012 [53]. This sub-section and section 1.4.3 focus on the description of how to make this S-CPW Tline tunable.

1.4.1. Principle

Per definition a tunable Tline is a Tline that has variable characteristic impedance. Then, according to equation (1-10), to change the characteristic impedance of a Tline, we have two possibilities: vary L_l or C_l . Changing L_l will not be the right way as we need to maintain a good quality factor. This is due to extra conductive losses that will be added when making L_l to increase whereas it is explicit that α should not be higher, according to equation (1-15). Hence, it is chosen to vary the capacitance C_l. Therefore, in order to make the S-CPW tunable (TS-CPW), $Ctot$ will change. The proposed equivalent model for TS-CPW is shown in Figure 1-20.

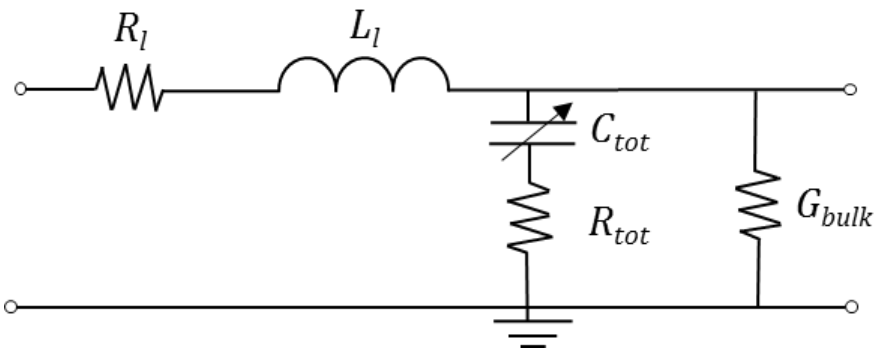


Figure 1-20: Proposed equivalent model for TS-CPW.

To vary the capacitance C_{tot} of the S-CPW, we have two methods: a) the first method is based on varactors (sub-section 1.4.2), b) the second method is based on distributed MEMS (section 1.4.3).

1.4.2. Varactor based

In that case, the topology of TS-CPW is based on varactors; its principle is to add varactors between the signal strip and the shielding plane as shown in Figure 1-21.

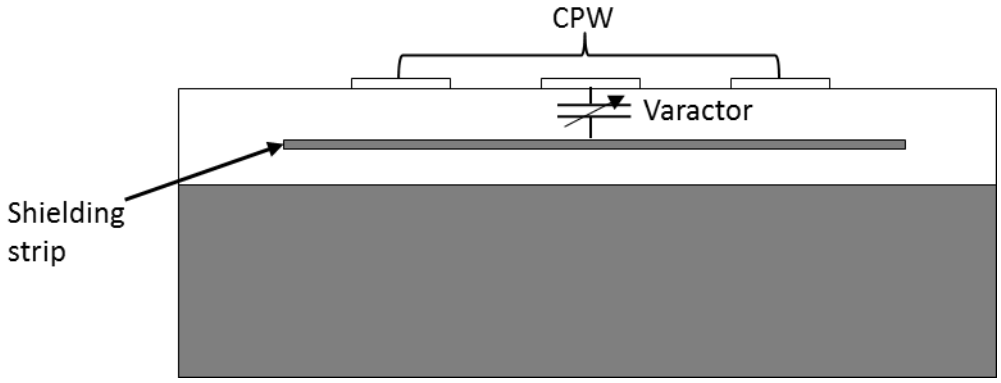


Figure 1-21: Cross view of S-CPW to form the tunable phase shifter with varactors.

The total capacitance that is controlled by the bias voltage applied to varactors (DC voltage is depending of the technology used) causes the variation of the phase and of the characteristic impedance.

[51] has proposed a phase shifter based on TS-CPW with varactors implemented in the 55 nm technology by STMicroelectronics. Figure 1-22(b) presents the phase shifter electrical model.

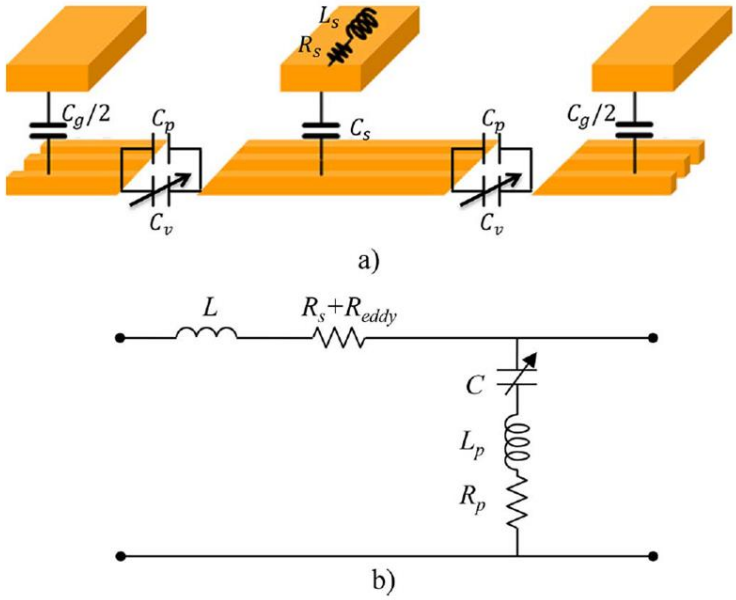


Figure 1-22: Phase shifter electrical model [51].

The shielding plan is broken in order to connect the varactors C_v in between as shown in Figure 1-22(a). The total TS-CPW's capacitance is variable and is given by equation (1-19).

$$C = \frac{2.Cs.Cg.(Cv+Cp)}{2.Cg.(Cv+Cp)+2.Cs.(Cv+Cp)+Cs.Cg} \quad \textbf{(1-19)}$$

C_p is the parasitic capacitance coming from the coupling between the two extremities of the broken floating shield. The phase constant of the Tline is varying due to the variation in the total capacitance C and then the absolute phase of S-CPW is changed. This phase shifter is working at 60 GHz and the varactors are chosen in order to obtain a maximum tuning rang (TR) and a maximum FoM.

Unfortunately, the parasitic capacitance and the varactor loss may degrade the performances of this kind of tunable S-CPW.

1.4.3. Distributed MEMS based

The second method to design a tunable Tline is with distributed MEMS. In this method, the phase tunability of the S-CPW can be achieved by controlling the distance between the CPW strips and the shielding layer, which gives the capacitance C_l. The idea is to apply a DC voltage between the shield and the CPW in order to vary the capacitance value, leading to a distributed MEMS effect.

In [55] a distributed MEMS phase shifter is implemented in CMOS a 0.35 µm technology by AMS. In this design, DC electrodes were added for electrostatic actuation to move the shielding plane. Figure 1-23 presents the cross views of the S-CPW with the DC electrodes and the tuning principle of the phase shifter.

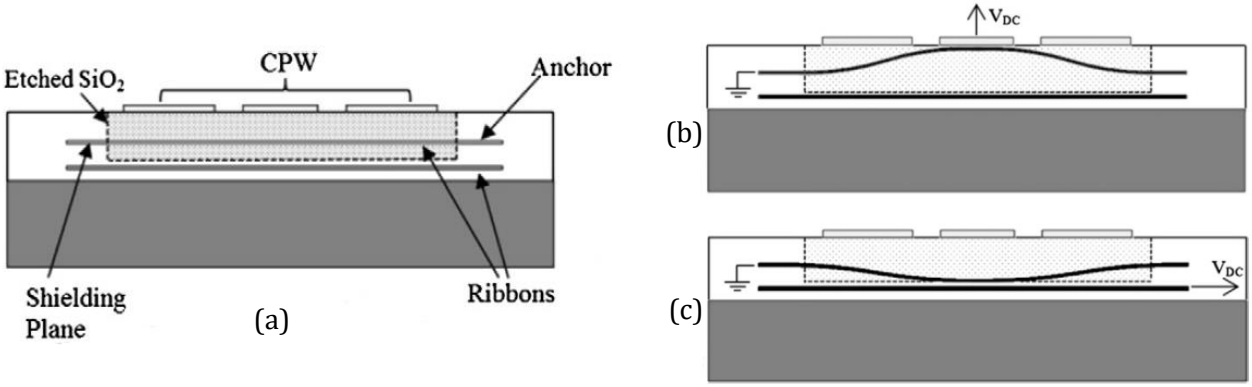


Figure 1-23:(a)Cross view of S-CPW to form the tunable phase shifter with distributed MEMS, (b) and (c) the tuning principle of the phase shifter [55].

A post-CMOS maskless etch step is necessary to make the shielding plane mobile. Then, the distance between the CPW strips and the shielding plane are controlled via the DC voltage. If the DC voltage is applied between the shielding plane and the CPW strips, the shielding strips move up to the CPW trips. Thus, the capacitance per unit length increases, leading to phase velocity decrease. If the DC voltage is applied between the shielding plane and the bottom electrodes, the shielding plane moves far away from the CPW strips. Thus, the capacitance per unit length decreases. At 60 GHz, the TS-CPW (for Tunable S-CPW) presents a variation of permittivity from 4.5 to 58 when the position of the shielding plane is varied from 0.08 to 2 µm, and the characteristic impedance varies from 26 to 95 Ω. The length of the proposed structure is 908 µm for area less than 0.14 mm^2. Finally, the return loss is better than 10 dB, and the insertion loss for a 360° phase shifter is 0.7 dB for a minimum quality factor (Q) of 40.

1.5. Integrated technologies description for distributed MEMS

An integrated circuit (IC) or monolithic integrated circuit is based on semiconductor material (silicon). An integrated technology consists of two parts: Front-end-of-line (FEOL) and back-end-of-line (BEOL) which consists in sandwiching metallic layers between isolating silicon oxide layers, on top of the silicon bulk.

In this section, only the CMOS, BiCMOS and MEMS technologies used by our laboratory to fabricate a tunable phase shifter at mm-wave is discussed. First, the technologies used in the previous designs by Marcus Peregrini [58] (PTA technology), Bruno Verona [59] (AMS technology) and Gustavo Rehder [59] (CEA and AMS technologies) are presented. The results were characterized during this PhD thesis. Second, the main technology, 0.25 µm BiCMOS by IHP, used in this thesis to design a new tunable phase shifter is described.

1.5.1. Previous work

1.5.1.1. PTA technology

PTA (for ‘‘Plateforme Technologique Amont’’) is a clean room installed in Grenoble where the process to fabricate the tunable phase shifter with a classical ‘‘bottom-up’’ MEMS technology approach was developed.

On a bare glass substrate, a deposit of 350 nm of aluminum is realized by e-beam, and then the CPW strips are defined by optical lithography, Figure 1-24(a). In order to avoid short circuits during MEMS actuation, a 50-nm layer of alumina is deposited by atomic layer deposition (ALD), Figure 1-24 (b). An oxide layer of 1.8 µm thickness is realized by plasma enhanced chemical vapor deposition (PECVD), Figure 1-24(c) followed by a chemical mechanical polishing (CMP), Figure 1-24(d). Finally, the floating strips of 350 nm thicknesses are formed by optical path above the CPW strips, Figure 1-24 (e), before releasing by HF vapor, Figure 1-24(f).

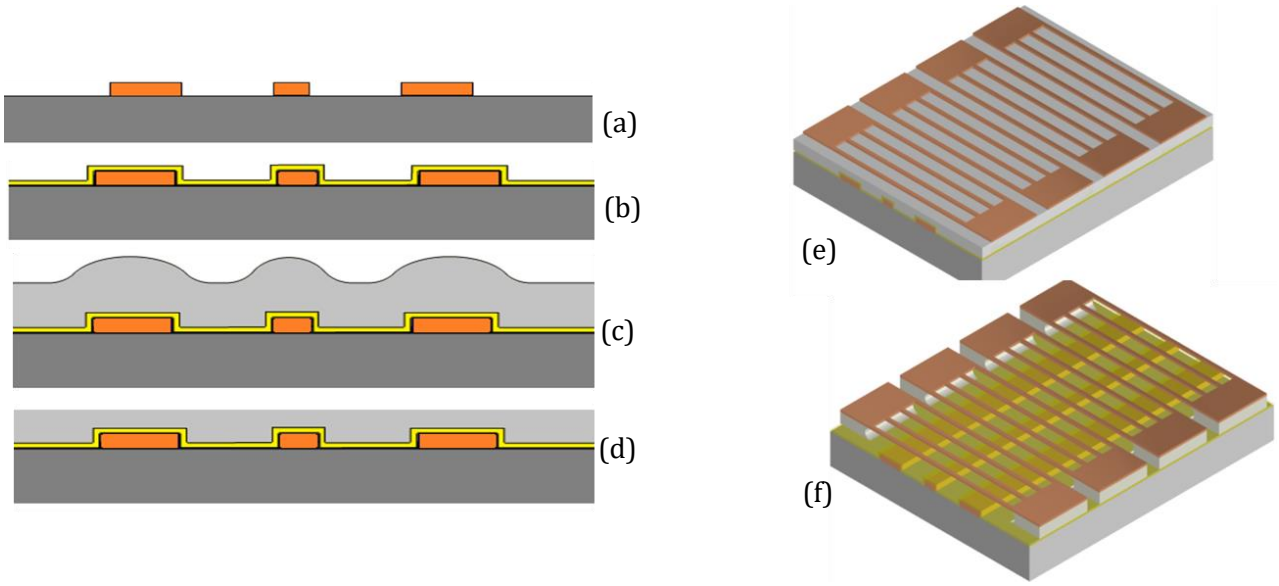


Figure 1-24: Fabrication process with PTA technology.

1.5.1.2. CEA technology

Thanks to the partnership between CEA-LETI and IMEP-LaHC, the classical MEMS technology of CEA was used to design a tunable phase shifter based on distributed MEMS. This technology is confidential, and thus we solely present the steps of fabrication for a MEMS structure without the thicknesses and types of materials that were used.

In the beginning, the cavity where the CPW strips are deposited is defined by photolithography and etching in a high resistivity substrate. Then, the etched substrate is covered with a silicon oxide, Figure 1-25(b). The metal layer of the CPW strips formed from Ti / Ni / Au is deposited by PVD (Physical Vapor Deposition) and is etched, Figure 1-25(c). A silicon sacrificial layer is deposited and planarized by CMP to fill in the cavity, Figure 1-25(d). Finally, the movable membrane is constituted of a SiN_x layer of 500 nm thickness, Figure 1-25(e). It is important to note that the interconnect pads of the membranes are set on a gold (Au) layer of 1 µm of thickness, Figure 1-25(f).

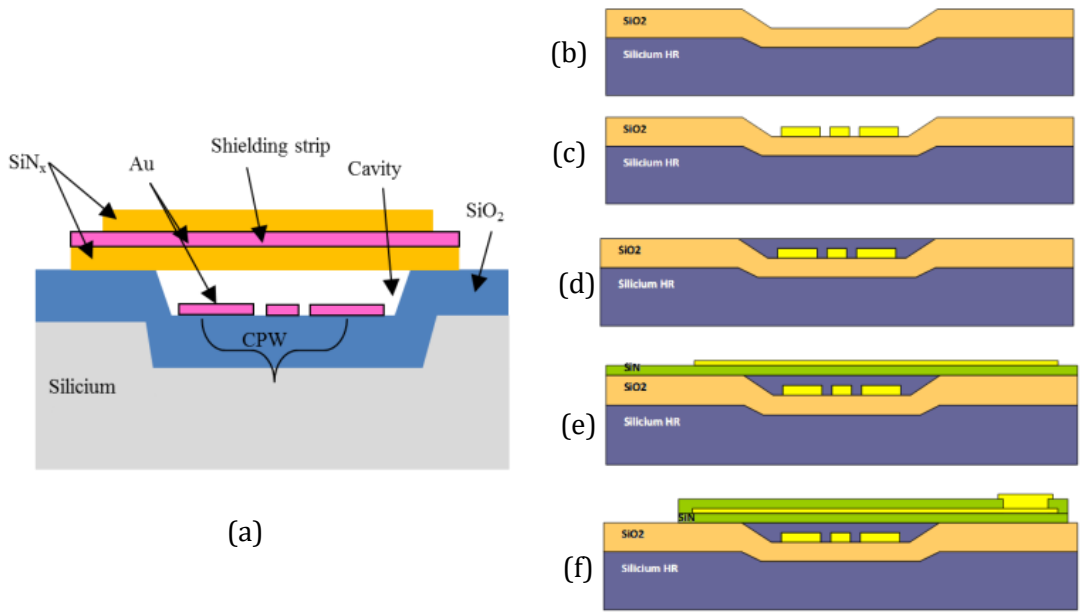


Figure 1-25: Fabrication process with CEA technology.

1.5.1.3. AMS 0.35 µm technology

The BEOL of the AustraMicroSystems AMS 0.35 µm technology is shown in Figure 1-26. It has four levels of aluminum metallization: the upper level is the 2.8 µm thick M4 in order to minimize the conductive loss, the other three metal levels possess a thickness of 0.64 µm and each layer of SiO_2 between two metal levels has a thickness of 1 µm. The stack is covered with a passivation layer (2 µm of silicon nitride Si_3N_4) to protect the devices from corrosion. The permittivity of silicon nitride is 7.4, which also serves to limit the leakage of the electric field lines in the air.

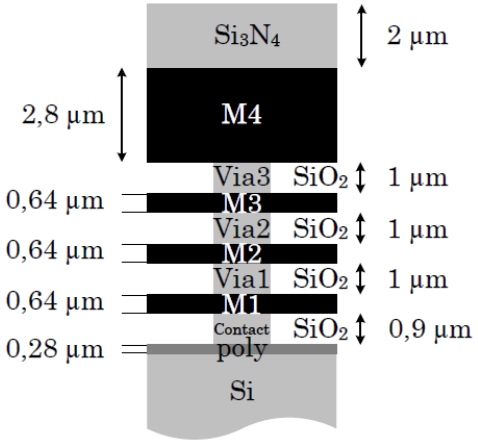


Figure 1-26: BEOL of the AMS 0.35 µm technology.

1.5.2. IHP technology

IHP (for Innovations for High Performance Microelectronics) is a research institute located in Frankfurt Oder, near Berlin, in Germany. Thanks to the partnership between IHP and IMEP-LaHC, IHP offers us access to powerful SiGe BiCMOS technologies. 0.25 µm and 0.13 µm BiCMOS technologies are available for chip fabrication at IHP Microelectronics. The IHP's 0.25 µm BiCMOS technology (SG25) is presented below, since this technology was used for the designs carried out in this thesis. Its BEOL is given in Figure 1-27.

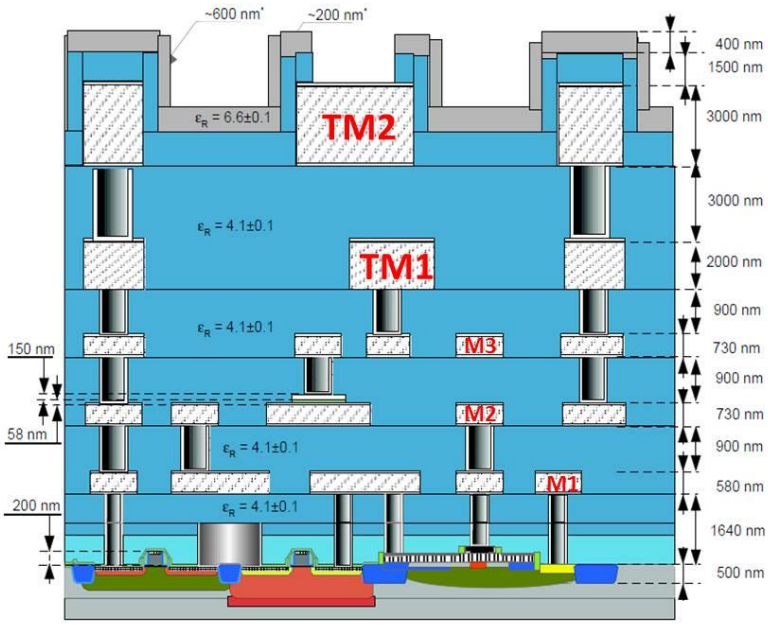


Figure 1-27: BEOL of the IHP's 0.25 µm BiCMOS technology.

The BEOL is constituted by five aluminum metallization levels, with two thick upper levels (TM1 and TM2) of 2 and 3 microns thickness, respectively. M2 and M3 levels are 0.73 µm thick, and the lower metal level M1 has a thickness of 0.58 µm. The gap between TM1 and TM2 is 3 µm thick, whereas the gap between the other layers is 0.9 µm thick.

In 2009, in reference [56], IHP presented the first BiCMOS embedded RF-MEMS switch for mm-wave applications. Figure 1-28 shows the 1st generation of IHP's RF-MEMS switch in 0.25 µm BiCMOS technology.

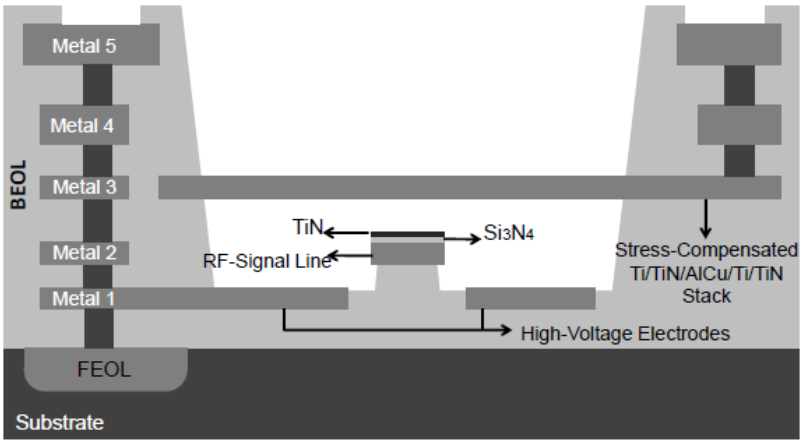


Figure 1-28: IHP's 1st generation RF-MEMS switch in 0.25 µm BiCMOS technology.

The M1 level was utilized to implement the high-voltage electrodes in order to move the MEMS membranes, while the capacitance switch was formed between M2 and M3 layers. M2 and M3 were used to RF signal line and membrane, respectively. On the M2 level, a thin layer stack of thin Si_3N_4/TiN was composed, which is a part of BiCMOS metal insulator-metal capacitor and forms the switch contact region. This configuration creates a height difference between the high-voltage electrodes and the signal line, which serves also as a stopping layer for the switch membrane. The MEMS membranes in M3 were realized using a stress compensated metallic layer Ti/TiN/AlCu/Ti/TiN.

There is also the 0.13 µm BiCMOS technology (SG13), utilized for example in [57], that is composed of two more metal layers than the SG25 technology to offer more opportunities for designing passives circuits.

In the following, we will use these abbreviations SG25 and SG13 for simplicity, instead of the full name 0.25 µm BiCMOS and 0.13 µm BiCMOS, respectively.

1.5.3. Discussion

A previous analysis in the state-of-the-art section has shown that the phase shifters based on MEMS and CMOS/BiCMOS technologies had good performances; MEMS circuits in terms of FoM and CMOS devices in terms of occupied area. Some other limitations for the original integrated approach (MEMS technology) for MEMS circuits exist: higher level of complexity for this integrated process lead to lower yields and the need of advanced packaging.

In addition, the fabrication process of a CMOS integrated circuit is much more simple and cost effective than a MEMS process.

For these reasons, a combination of these two technologies (MEMS and CMOS) can make a great revolution mostly for mm-wave applications and obtain reduction in term of size and cost. Recently, some researcher from institutes like IHP released MEMS structures which are fabricated directly on top of standard CMOS.

The challenge of this thesis is to design novel phase shifters based on distributed-MEMS technology in the 0.25 µm BiCMOS IHP's technology.

1.6. Conclusion

This chapter has presented an overview of phase shifters designed with different topologies and technologies, and some applications, followed by a state-of-the-art review for passive mm-wave phase shifters. With regards to the transmission lines based on slow-wave effect, characteristics and electrical model of tunable slow-wave transmission lines have been explained throughout the chapter.

In chapter 2, after an overview about the RF MEMS switches, previous designs of tunable transmission line using MEMS and CMOS technologies will be presented. Then, the proposed solution using MEMS technology with a post-CMOS process will be detailed.

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Chapter 2

Design of tunable slow-wave coplanar waveguides (TS-CPWs) based on distributed MEMS

Various topologies and applications of tunable phase-shifters have been described in chapter 1. An innovative solution, based on tunable slow-wave transmission lines with distributed MEMS, in integrated technologies, has been proposed. It should enable to further design a tunable N-bits phase shifter whose design and topology will be considered in chapter3.

This chapter 2 is devoted to deeper detail the design of TS-CPWs in a CMOS technology. First, a brief presentation of RF-MEMS switches theory including their types and operating principle is performed. This theoretical study is necessary to establish the preliminary basis for designing the TS-CPWs. Next, previous TS-CPWs topologies at IMEP-LaHC in MEMS technologies are presented. Then, the optimization of the tunable transmission lines through an electromagnetic simulation step is described. The impact of each physical dimension is studied.

2.1.RF-MEMS switches: types and operating principle

2.1.1. Overview

MEMS for “Micro-Electro-Mechanical System” refers to the deformable electrical micrometric systems which uses a mechanical movement to perform an electrical function. The idea was validated in 1967 [1] by producing the first MOS transistor with mechanically moving gate. This gate was like a suspended electrode whose movement could modulate the current.

A few years later, this coupling between electrical and mechanical components was demonstrated in the microwave field. In 1979 [2], the first MEMS component for communication applications has emerged and thus a new technology “Radio Frequency Micro-Electro-Mechanical Systems” (RF-MEMS) was developed.

There are two main types of RF-MEMS switches: capacitive switches (metal-dielectric contact) and ohmic switches (metal-metal contact). In both types, there is a movable structure where a force is applied to move the MEMS membrane in order to achieve the electrical function.

This applied force can be magnetic [3], thermal [4] or electrostatic. In the latter case, it is derived from the electric potential difference applied between the movable membrane and the activation electrode.

2.1.2. RF-MEMS ohmic switches

The behavior of RF-MEMS ohmic switches is similar to that of an interrupter (switch); it has a metal contact between the input and the output of the component in the actuated state. Figure 2-1 illustrates the operating principle.

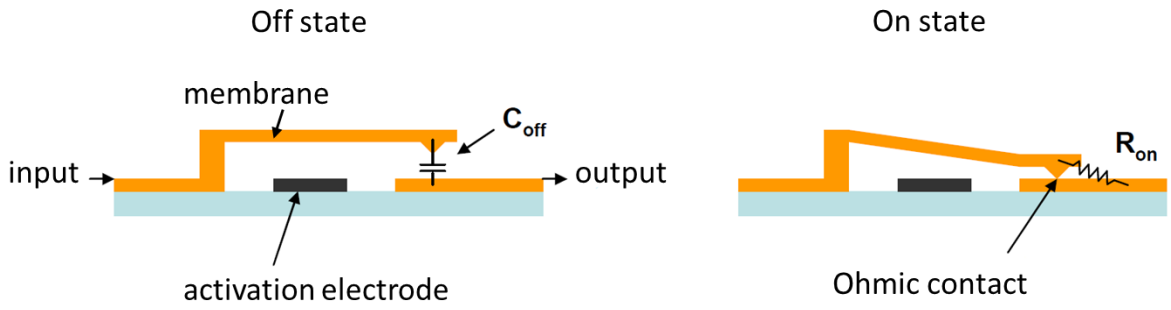

Figure 2-1: Operating principle of a RF-MEMS switch with an ohmic contact.

In the off state, the membrane does not contact the output, hence no transmission of the RF signal can be observed. However, a capacitance C_{off} is considered between the membrane and the output. When the voltage is applied to the activation electrode, an electrostatic field is created, which enables the membrane to move down (on-state). The metal-metal contact connects the input to the output and the signal is transmitted via a contact resistor (R_{on}) of a few ohms. A classical figure-of-merit to characterize an ohmic switch is the product $R_{on}C_{off}$ (in seconds).

2.1.3. RF-MEMS capacitive switches

RF-MEMS capacitive switches use a thin dielectric layer to create a component that will be a variable capacitor that can take two possible values between the input and the output (see Figure 2-2).

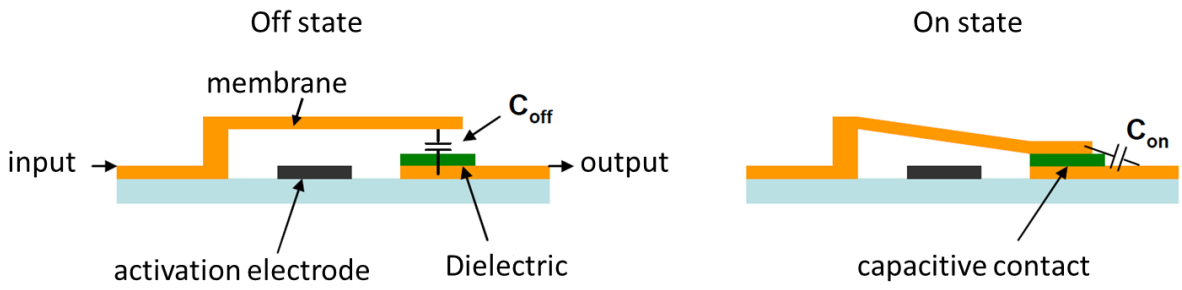

Figure 2-2: Operating principle of a RF-MEMS switch with a capacitive contact.

As for ohmic contacts, in the off-state, the membrane does not contact the output. The capacitance C_{off} has a low value that does not enable the transmission of the RF signal. This capacitance is increased in the on-state, the signal is transmitted via a capacitive contact metal-dielectric-metal (C_{on} with C_{on}>>C_{off}). A classical figure of merit to compare various capacitive switches is given by the ratio C_{on}/C_{off}.

As it will be explained later in this chapter, the solution with distributed MEMS is based on a capacitive contact to avoid shunting the RF signal to ground.

2.1.4. Electrostatic actuator

2.1.4.1. Introduction

RF-MEMS switches are generally composed of a movable metallic membrane. Hence the most prevalent method for applying forces to deformable elements in microsystems is seemingly the electrostatic actuation.

2.1.4.2. Operating principle

The electrostatic actuation of RF-MEMS is generally comparable to that of a simple mechanical system of plate-ressort. The movable membrane is similar to a mass/spring system located on top of a fixed metal electrode. This electrode enables to generate an electrostatic field due to an electric potential difference between both, which creates an attractive force on the membrane enabling to change its position [5]. In order to approximate this force, the electrode is modeled as a parallel plate capacitance. The model of the electrostatic actuator is shown in Figure 2-3.

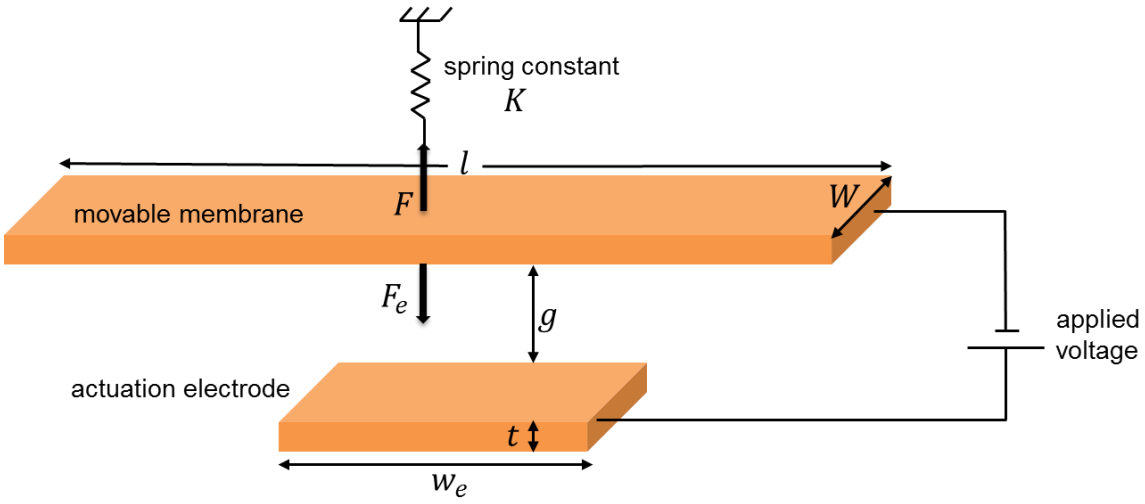

Figure 2-3: Modeling of the electromechanical operating principle of RF-MEMS electrostatically actuated.

Given that the length of the actuation electrode is w_e and the width of the pull-down electrode is W, the parallel plate capacitance is given in eq. (1-19).

$$C = \frac{\varepsilon_0 . A}{g} = \frac{\varepsilon_0 . W . w_e}{g} \quad \textbf{(2-1)}$$

where g is the gap between the membrane and the electrode and ε_0 the vacuum permittivity. The electrostatic force (F_e) applied to the membrane is found by considering the power delivered to the capacitance and is given by eq. (2-2) [5].

$$F_e = \frac{1}{2} V^2 \frac{dC(g)}{dg} = -\frac{1}{2} \frac{\varepsilon_0 . W . w_e . V^2}{g^2} \quad \textbf{(2-2)}$$

where V is the applied voltage between the membrane and the electrode. In the capacitive MEMS case, a dielectric layer is located above the actuation electrode; such layer is not considered in Figure 2-3. Thus its effect is neglected in eq. (2-2). In addition, it is considered that the electrostatic force is evenly distributed across the section of membrane above the electrode.

The mechanical restoring force (F) due to the stiffness of the membrane depends on the displacement of the membrane during the actuation and the spring constant associated with the membrane material and dimensions, see eq. (2-3).

$$F = K . (g - g_0), \quad \textbf{(2-3)}$$

where g_0 is the zero-bias bridge gap. Weighting force is totally negligible with respect to restoring force. Hence, when the system is well-balanced, the electrostatic force (F_e) and the mechanical restoring force (F) are equal, leading to eq. (2-4) and (2-5) [5].

$$\frac{1}{2}\frac{\varepsilon_0.W.w_e.V^2}{g^2} = K.(g_0 - g) \quad \textbf{(2-4)}$$

$$V = \sqrt{\frac{2.K}{\varepsilon_0.W.w_e}g^2(g_0 - g)} \quad \textbf{(2-5)}$$

The restoring force varies linearly with the gap while the electrostatic force varies nonlinearly with gap and bias voltage. Both forces are getting higher when g reduces. There is no compensating phenomenon. From eq. (2-5) it can be seen that the relationship between V and g is non-linear. Figure 2-4 shows the evolution of the gap with the applied voltage, and identifies the region of instability when a third of the gap height ($g = \frac{2}{3}g_0$) is achieved [5]. This value can be determined very easily firstly by calculating dg/dV and then identifying the position for which this derivative becomes infinite, hence leading to instability. This derivation is performed from eq. (2-6) to (2-10), as mentioned below.

$$\frac{1}{2}.\varepsilon_0.W.w_e.V^2 = 2.K.(g_0 - g).g^2 \quad \textbf{(2-6)}$$

$$\frac{1}{2}.\varepsilon_0.W.w_e.V^2 = K.g^2 g_0 - K.g^3 \quad \textbf{(2-7)}$$

By taking the derivative of eq. (2-7) versus V , eq.(2-8)is achieved.

$$\frac{1}{2}.\varepsilon_0.W.w_e.2\mathrm{V} = K.g_0.2g.\frac{dg}{dV} - K.3g^2.\frac{dg}{dV} \quad \textbf{(2-8)}$$

$$\frac{dg}{dV} = \frac{\varepsilon_0.W.w_e.V^2}{K.g.(2g_0 - 3g)} \quad \textbf{(2-9)}$$

$$\frac{dg}{dV} \to \infty, for\, g = \frac{2}{3}g_0 \quad \textbf{(2-10)}$$

So the minimum applied voltage V_p needed to move down the membrane and achieve contact is given by eq. (2-11).

$$V_p = V\left(^2/_3\, g_0\right) = \sqrt{\frac{8.K}{27.\varepsilon_0.W.w_e}{g_0}^3} \quad \textbf{(2-11)}$$

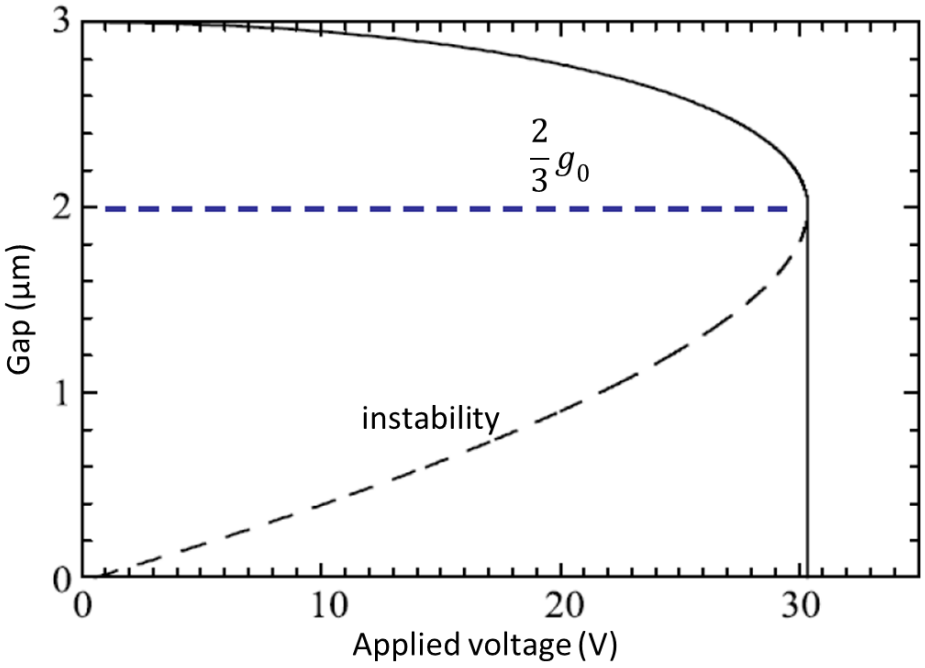

Figure 2-4: Gap height versus applied voltage with a spring constant of 10 N/m and 100*100 µm² of area [5].

The pull-in instability produces some difficulties in some special design (i.e. comb-drives, charge actuation [6]) and operation modes, but it is used in other applications to achieve a fast transition between two states of an electromechanical switch [6].

2.1.5. Reliability issues

An RF-MEMS component actuated with an electrostatic force can be exposed to several types of failure. First type is electrical such as the dielectric failure (breakdown due to ESD: Electro Static Discharge or EOD: Electrical Overstress), [8], and failure due to injection and charge trapping, which causes the deterioration of capacitive RF-MEMS due to the electronic conduction mechanism in the dielectric [9]. Second type is mechanical, and can be due to deformation with the apparition of a mechanical stress after the actuation step; it can be due as well to plots deterioration in the case of ohmic RF-MEMS. Another kind of mechanical failure is the creep phenomenon that can be accelerated with temperature. It is present probably in all RF-MEMS structures. There are also failures due to high microwave power [12], thermal effects [13], and external environment [14].

2.2.Tunable Slow Wave CoPlanar Waveguide (TS-CPW) with distributed MEMS in IHP 0.25 µm BiCMOS technology

2.2.1. S-CPW in the 0.25 µm BiCMOS technology

Before designing TS-CPWs based on distributed MEMS in IHP's 0.25 µm BiCMOS technology (SG25), a study was necessary in order to find the best design for the classical S-CPW in SG25 that will be used to perform high-performance TS-CPW. The S-CPW concept was already detailed in chapter 1. We just remind here that loading a conventional CPW with shielding ribbons leads to the increase of the capacitance, enabling slow-wave effect. This shielding layer can be realized above or below the strips of the conventional CPW.

Figure 2-5 is a reminder of the SG25 BEOL, the design of IHP's already available capacitive RF-MEMS switch, [56], and the topology of an S-CPW.

The SG25 BEOL has five metal layers with different gaps (Figure 2-5 (a)). From Figure 2-5 (b) and [56], we note that M3 uses a stress compensated Ti/TiN/AlCu/Ti/TiN in order to realize the movable membrane of the capacitive RF-MEMS switch. Adding this stress compensation, as compared with SG25 without MEMS, does not lead to a destruction of the original M3 process specifications (IHP certification process, [56]).

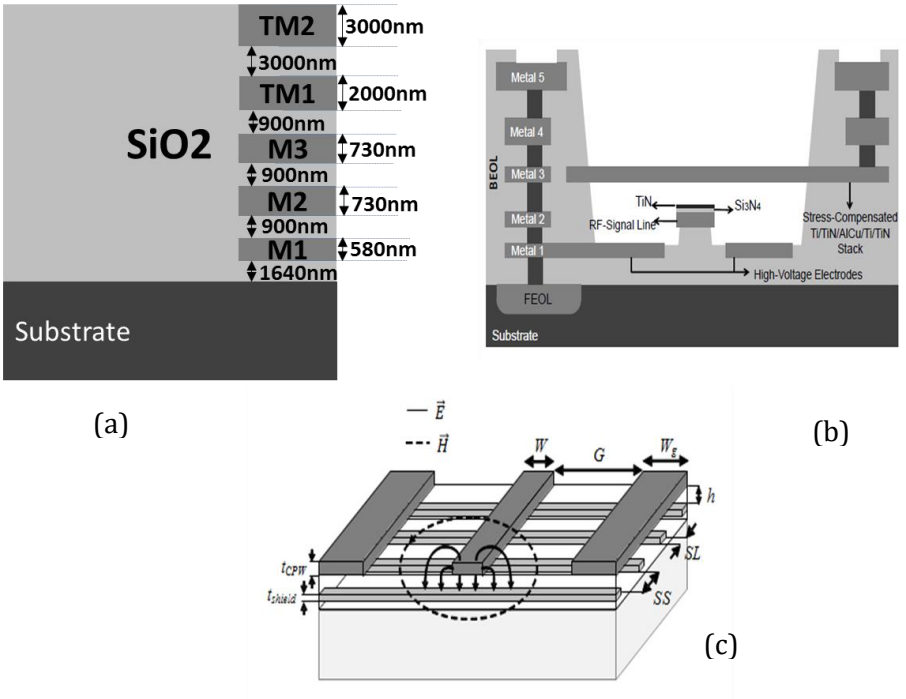

Figure 2-5: (a) BEOL of IHP's SG25 technology, (b) cross section embedded of IHP's RF-MEMS switch integration [56], (c) S-CPW topology.

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By comparing the topologies of the S-CPW and the RF-MEMS switch, M3 can be chosen to realize the tunable shielding layer in the TS-CPW [55], such as the movable membrane in the RF-MEMS switch.

There are many possibilities to choose the appropriate metallic layer for the CPW strips. M1 has the lowest thickness with respect to the others layers, and would lead to high metallic losses. The suitable layer must be chosen among M2, TM1 and TM2.

The geometrical parameters of a classical S-CPW are:

- Parameters linked with CPW
  - W: width of signal strip
  - W_g: width of ground strip
  - G: gap between signal and ground strips
  - t_{cpw}: metal thickness of CPW strips
- Parameters linked with shielding layer
  - SS: floating strips space
  - SL: floating strips length
  - t_{shield}: metal thickness of floating strips
  - h: dielectric thickness between floating strips and CPW strips

Figure 2-6 (a) shows the only possibility where the shielding layer is over the CPW strips. Figure 2-6 (b), Figure 2-6 (c) and Figure 2-6 (d) present the other cases where the shielding layer is below the CPW strips (TM1, TM2 and TM1-TM2 stack).

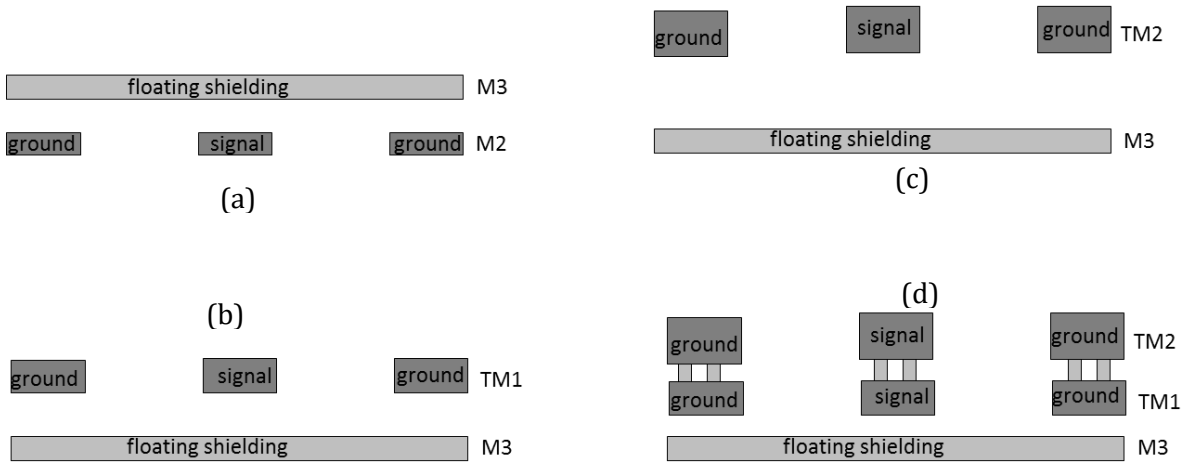


Figure 2-6: Cross section of different topologies of S-CPWs in IHP's SG25.

From equations (1-4) and (1-7), we can see that the characteristic impedance Z_C depends on the capacitance per length C_l, which depends on the signal width W. Thanks to HFSS™ simulation tool, a parametric simulation of all S-CPWs presented in Figure 2-6 was carried out in order to select the 50 Ω S-CPW in the different stack configurations. Table 2-1 gives the physical parameters and performances of different 50 Ω S-CPWs at 60 GHz.

Table 2-1: Characteristics and performances of the simulated 50 Ω S-CPWs in IHP's SG25 technology at 60 GHz.

$Z_c(\Omega)$	CPW layer	Floatting strips layer	Dimensions				Performances		
			W (µm)	W_g (µm)	G (µm)	SL(µm) SS(µm)	α (dB/mm)	Q	ε_{eff}
50	M2	M3	10	10	40	1	1.33	21.6	28
50	TM1	M3	10	5	40	1	1.24	20.4	21.8
50	TM2	M3	25	25	40	1	0.47	35	9.2
50	TM1-TM2	M3	5	5	70	1	0.86	27.8	19.3

Usually SS and SL are given by the minimum width allowed by the DRM (Design Rule Manuel), 0.5 µm for each. Here, the floating shield will be actuated. For precaution, we preferred fixing SS=SL $= 1$ µm .

The dimensions of the CPW (W, W_g, G) allow to determine the characteristic impedance. ε_{eff} depends on the capacitance per unit length C_l, which is not the same in the four cases. Figure 2-7 presents the maximum and minimum quality factor and maximum attenuation constant versus the CPW strips stacks, for a large range of characteristic impedances (15 Ω to 88 Ω).

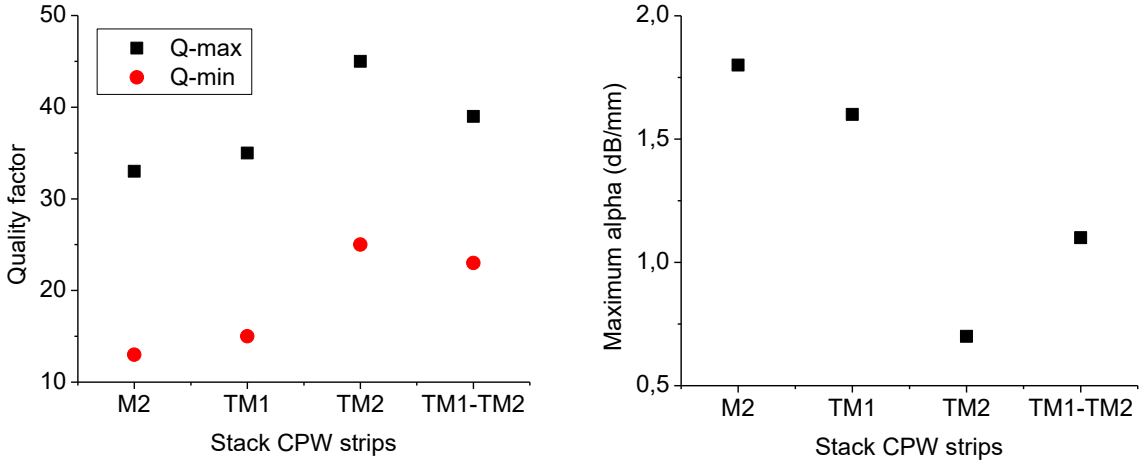


Figure 2-7: **Quality factor and maximum of linear loss versus CPW strips stacks.**

M2 has the smaller thickness layer among M2, TM1, TM2 and TM1-TM2 stack. This small thickness of M2 which is also the closer layer to the lossy doped silicon substrate, leads to higher dielectric losses and decreases the quality factor of the S-CPWs built in this layer.

The gaps between the substrate and TM1 and TM2 are 9.38 µm and 12.3 µm, respectively. As shown in Figure 2-7, whatever the stack is, a good quality factor can be obtained with an optimal value of Z_C. The maximum attenuation constant in TM2 is less than 1 dB, which gives a minimum quality factor better than the quality factor of the other lower layers due its high thickness and its distance from the lossy substrate.

When comparing TM1 and TM1-TM2 stack, losses are in favor of TM1-TM2. This is due to the stack higher thickness. Meanwhile the effective permittivities are quite similar, which leads to a better quality factor for TM1-TM2. A comparison between TM1 and TM2 alone imply a compromise between lower losses for TM2 (less proximity effect and higher thickness) but higher effective permittivity for TM1 (nearer to M3). The compromise leads to a better quality factor for TM2. Finally, even if the effective permittivity is higher for TM1-TM2 stack than for TM2 alone, due to the proximity with M3, the quality factor is highest for TM2 alone.

2.2.2. Design topology of TS-CPW

2.2.2.1. Fabrication priorities and specifications

Two priorities should be followed in practice for fabrication purposes:

- Etching release until M2, M2 included,

- Dimensions of the released floating strips not exceeding 200 µm; over length has to be a fixed part encapsulated with dielectric.

The previous study demonstrates that best performances for S-CPWs are obtained for CPW strips in the TM2. However, to release the TS-CPW structure a post etching process of the dielectric is necessary. When the CPW strips are on top of the membranes, the risk is high to have them movable too after etching, even with periodic pillar to support them. Therefore, the configuration in Figure 2-6 (a) has been chosen even if less promising in terms of quality factor.

Finally, the TS-CPW topology is presented in Figure 2-8. The structure is composed of CPW strips realized in M2. The floating shield (or floating membrane) takes place above the CPW strips in M3.

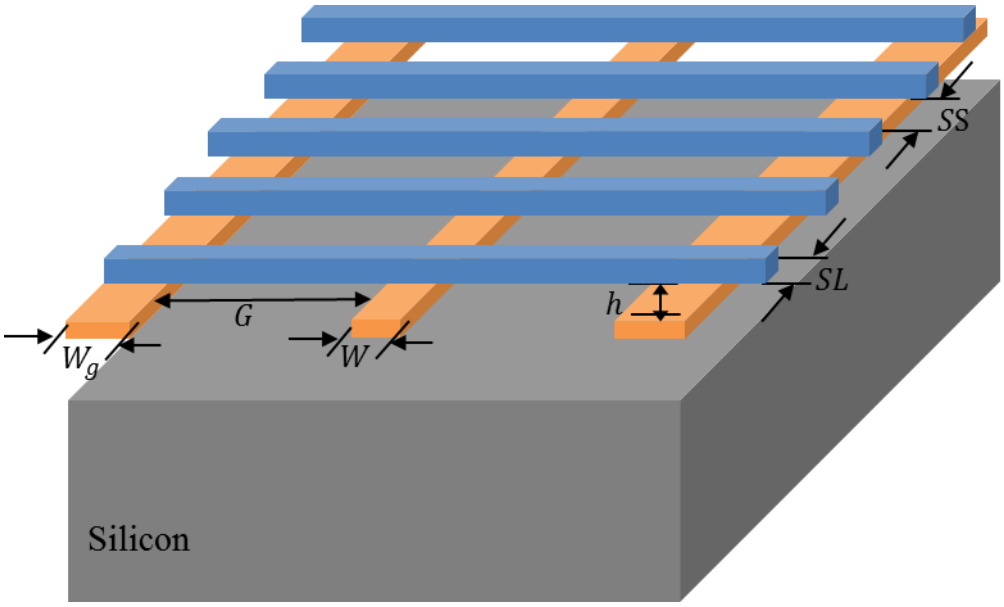


Figure 2-8: TS-CPW topology.

The high voltage electrode is realized in M1 below the CPW strips, as for IHP's capacitive switch [56], in order to have the floating membrane moving after applying a voltage. The minimum voltage needed to move the membrane depend on its size and the size of electrodes, as for RF-MEMS switches.

Figure 2-9 shows the cross sectional view of TS-CPW before actuation (off-state). The etching of the dielectric (SiO_2) is processed up to Metal 2. Hence the central part of the movable membrane of length (l) has been kept in air in order to allow capacitance variation, while the ground strips and the electrodes are totally embedded in dielectric. Embedding the ground strips and the floating membrane part over ground strips enable to reduce the released membrane length as recommended (see priorities). A longer release would be convenient for a

higher on/off capacitance ratio with a strong signal strip capacitance in series with two strong ground strips capacitances, but the risk would be high to get a weak spring effect and no tunability at all. On the contrary, the movable membrane is fixed on each side with SiO_2.

The supplementary parameters used in Figure 2-9 as compared to Figure 2-5 (c) are listed below:

- l: length of movable membranecorresponding to the etched zone
- G_1: air gap between signal and oxide
- G_2: oxide gap between air and ground strip
- $G = G_1 + G_2$: gap between signal and ground strips
- g: gap between membrane and actuation electrode
- w_e: width of actuation electrode

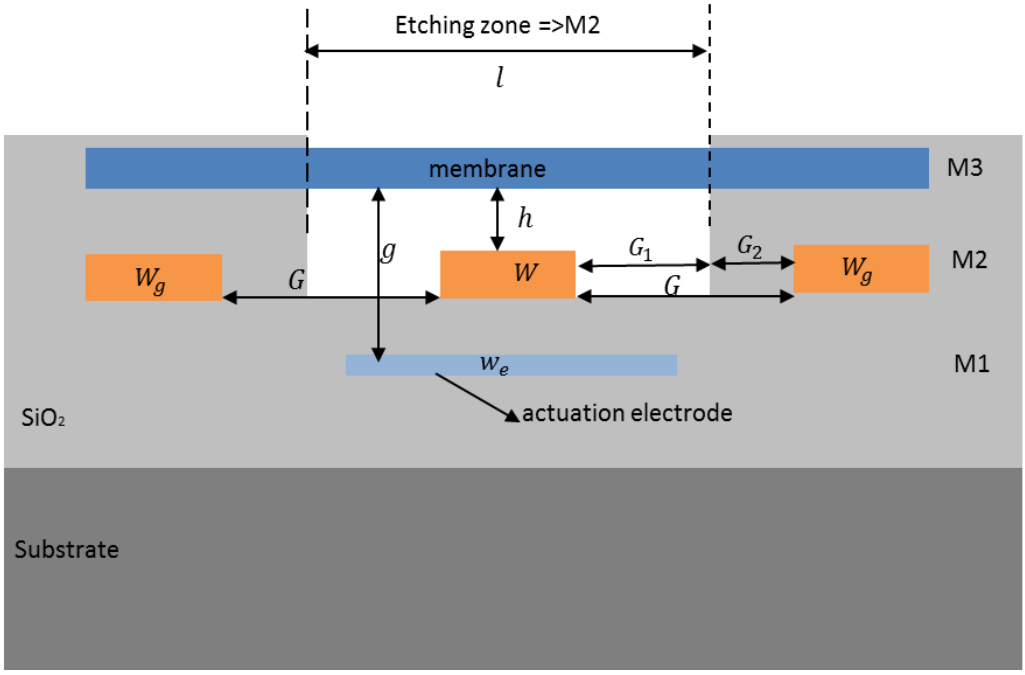


Figure 2-9: Cross sectional view of TS-CPW in IHP's SG25 technology before actuation (off-state).

A thin layer of TiN, with dielectric specification, takes place above the aluminum of the CPW strips in order to prevent the metal-metal contact (short circuit) that would lead to the destruction of the component during actuation. It is not shown in Figure 2-9.

Figure 2-10 shows the cross sectional view of the same TS-CPW after actuation (on-state). The application of a DC bias voltage between the membrane and the electrode leads to moving the membrane in the etching zone near to the central strip of the CPW thanks to the electrostatic force. Therefore, the gap between the membrane and the signal decreases and creates a

variation in the capacitance formed between membrane and signal strip. The gap after actuation is equal to of few nm of air [56].

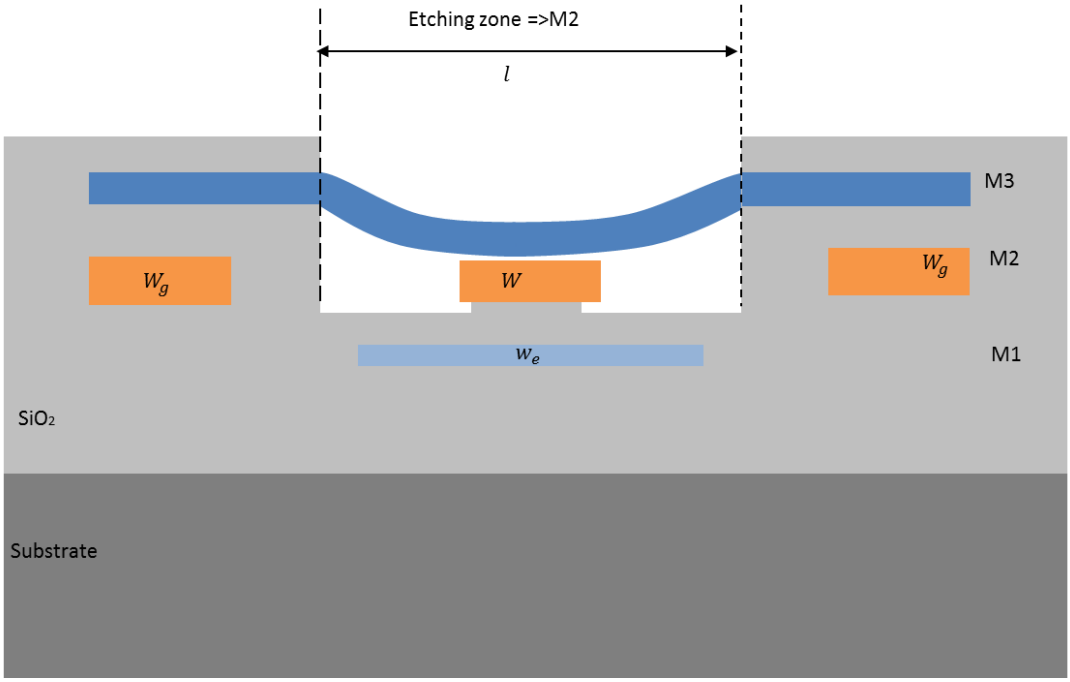


Figure 2-10: Cross sectional view of TS-CPW in SG25 technology after actuation (on-state).

2.2.2.2. Capacitances overview

For better understanding, Figure 2-11 presents a simple model of the capacitances formed between membrane and CPW strips. Capacitance C_g is formed between CPW ground strips and membrane, all embedded in dioxide. C_g does not vary with actuation. The variable capacitance is C_S, which is formed between CPW signal strip and the movable part of the membrane. Dielectric is air after etching. The expression of this variable parallel plate capacitance C_S is given in eq. (2-12).

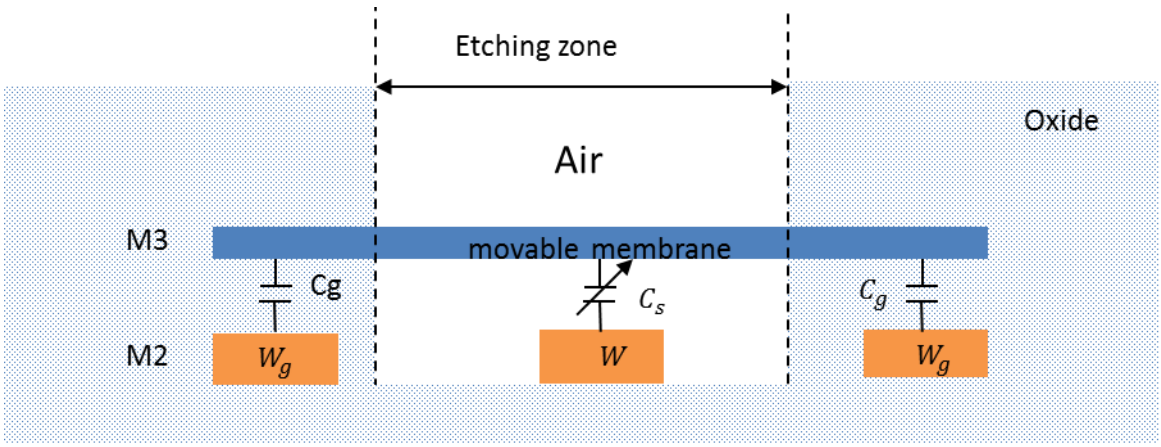


Figure 2-11: Simple model of the capacitances between the membrane and CPW strips.

$$C_s = \frac{\varepsilon_0 . \varepsilon_r . A}{h} \quad \textbf{(2-12)}$$

where A is the area ($A = W.SL$) and h is the variable gap between movable membrane and signal strip. h is changed from 900 nm for off-state to a few nm (≈11 nm) for on-state.

In practical cases, the electrical model for capacitance is composed of the parallel plate capacitances and fringing capacitances which are around 30 % of the global capacitance. The parasitic capacitances can be calculated and determined using electromagnetic software like HFSS. This will be detailed in chapter 3 dedicated to phase shifters.

2.2.3. Pull-in voltage calculation

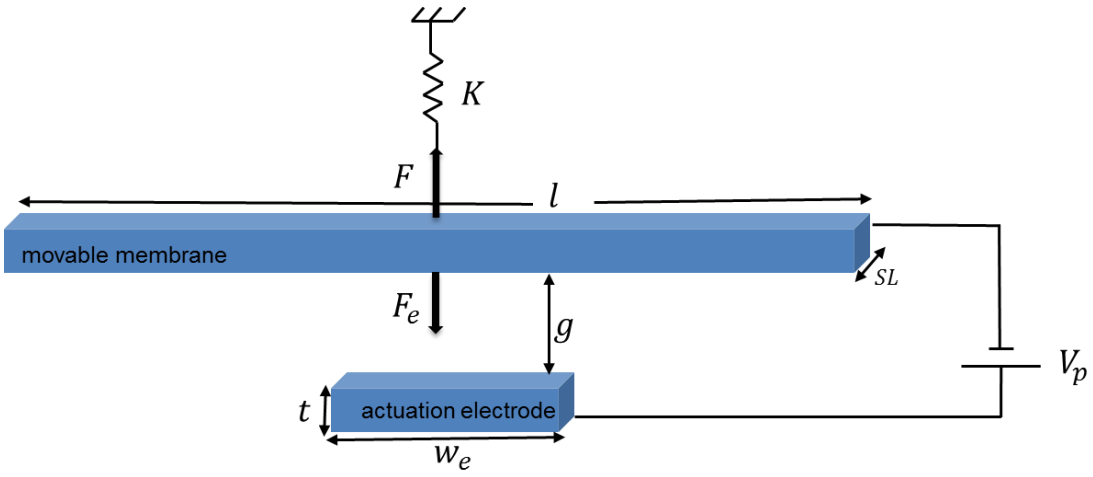


Figure 2-12: Electrostatic actuator of TS-CPWs.

As for RF-MEMS previously presented in section 2.1, an electrostatic actuator is used to actuate the TS-CPW. Figure 2-12 shows the model of the electrostatic actuator for TS-CPW.

The minimum applied voltage (V_p) to actuate the movable membrane of TS-CPW is given by eq. (2-13). The force must be evenly distributed over the center portion of the movable membrane fixed at both ends in the oxide. For this case the spring constant can be calculated by eq. (2-14).

$$V_p = \sqrt{\frac{8.K}{27.\varepsilon_0.SL.w_e} {g_0}^3} \quad \textbf{(2-13)}$$

$$K = \frac{192.E.I}{l^3} \quad \textbf{(2-14)}$$

where SL is the width of the movable membrane, l is the moving part of the membrane placed in the etching zone, as shown in Figure 2-12, E is the Young's modulus (elastic modulus) of the

metal used in this technology (here, for aluminum $E = 70\ GPa$, I is the inertia coefficient, which describes the motion of the membrane (see eq. (2-15)).

$$I = \frac{{t_{shield}}^3 . SL}{12} \quad \textbf{(2-15)}$$

When I is replaced in eq. (2-13) the new expressions of K and V_p are given by eq. (2-16) and (2-17), respectively.

$$K = \frac{2^4 . SL . {t_{shield}}^3 . E}{l^3} \quad \textbf{(2-16)}$$

$$V_p = \sqrt{\frac{8 . 2^4 . {t_{shield}}^3 . E}{27 . \varepsilon_0 . l^3 . w_e} {g_0}^3} \quad \textbf{(2-17)}$$

The dimensions of the movable portion of membrane and the actuation electrode are briefly studied in this section. From eq. (2-17), it is possible to observe that the minimum actuation voltage is modified with the initial gap between the actuation electrode and the movable membrane equal to 2.53 µm, the length of the movable portion of the membrane, the width of the actuation electrode and the thickness of the membrane metal layer which is imposed by the technology; here t_{shield} is fixed to 0.73 µm for M3. Calculations corresponding to different sizes of the movable portion of membrane and the actuation electrode are shown in Table 2-2.

Table 2-2: V_p for different dimensions.

Initial Gap g_0(µm)	w_e (µm)	l (µm)	V_p(V)
2.53	35	100	82
		150	49
		200	29
	70	100	59
		150	32
		200	21

From Table 2-2, we observe that the length of the movable membrane and the width of the actuation electrode are very important parameters to play with in order to reduce V_p. In practical cases, we cannot increase greatly l in order to avoid mechanical failures. From the electromagnetic point of view, the electrode is placed below the signal strip, so it is possible to strongly disturb the propagation by increasing greatly w_e. We can note that the SiO_2 between the

electrodes and the signal strip is not taken into account the sio2 so, we overestimate the actuation voltage.

2.2.4. TS-CPW simulations

For a proof concept, a simulation was made for a TS-CPW based on IHP's 0.25 µm BiCMOS technology, which BEOL has been detailed in chapter 1 and remembered in Figure 2-5**.** Figure 2-13 presents the cross views of half a TS-CPW structure, simulated with HFSS, for off- and on-states.

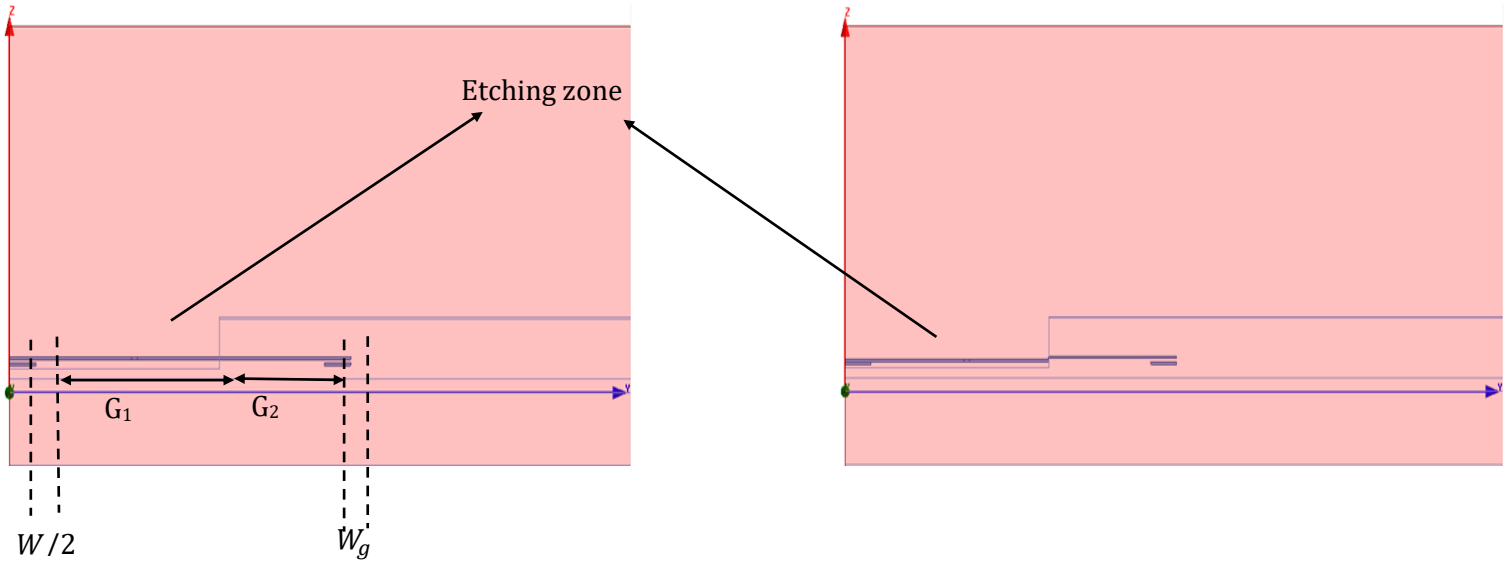


Figure 2-13: Cross view of TS-CPW (a) off-state and (b) on-state.

The gap between signal strip and membrane is about 900 nm of air in the off-state and 11 nm of air in the on-state. In counterpart, the gap between the ground strip and the membrane is the same (900 nm of oxide) in both cases.

HFSS simulation gives the scattering parameters. Then, these S-parameters are converted to ABCD parameters in HFSS or in MATLAB by writing the expressions of the output variables in order to determine the electrical characteristics of the TS-CPW. The diagram procedure is shown in Figure 2-14.

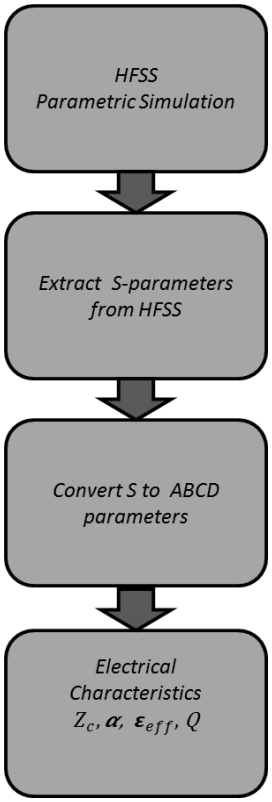


Figure 2-14: Diagram procedure to determine the TS-CPW electrical characteristics.

In section 2.2.3, we already saw that the length of the membrane is a very important parameter to consider in order to decrease the minimum applied voltage needed to make the membrane movable but with the priority of not exceeding 200 µm long. Two studies were carried out with respect to 160 µm of l corresponding to the etched zone, at various frequencies and for various signal widths. The other parameters were let fixed. In this section devoted to theoretical simulations only, we explain the dependency of the electrical parameters in two ways:

- versus the signal width W when l = 160 µm, at 60 GHz; other geometrical parameters are fixed
- versus frequency when l = 160 µm; all the geometrical parameters are fixed.

2.2.4.1. Simulation set 1 with l = 160 µm; signal width varies

The fixed dimensions of the simulated TS-CPW are presented in Table 2-3. Here, l was fixed to 160 µm. The signal width W and the gap G and $G1$ are variable.

Table 2-3: Dimensions of the simulated TS-CPW

Design parameters	
W_g	12 µm
G_1	70 µm
$SS = SL$	1 µm
w_e	70 µm

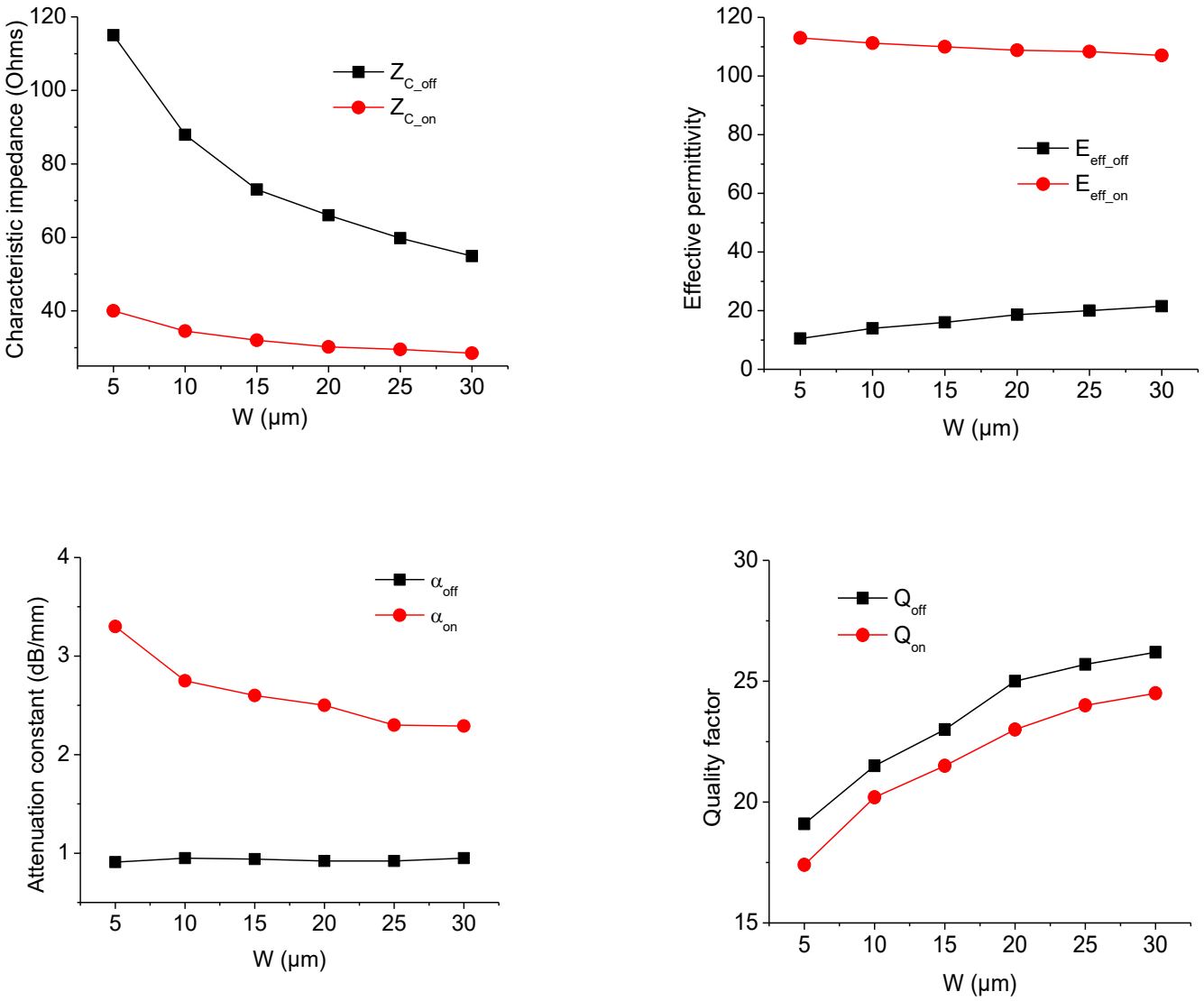


Figure 2-15: Electrical characteristics. (a) Characteristic impedance, (b) effective permittivity, (c) attenuation constant and (d) quality factor, versus width of CPW signal strip.

As expected, the characteristic impedance decreases with the width of the CPW signal strip. The capacitance is higher in the on-state than in the off-state. Consequently, as shown in Figure 2-15 (a), the characteristic impedance is lower in the on-state. For the same reason, the effective permittivity is five to six times higher in the on-state. Unfortunately, due to proximity effect, the

attenuation constant is higher in the on-state, about three times higher. Therefore, the quality factor is slightly lower for the on-state than for the off-state. For strip widths above 10 µm, both quality factors are superior to 20, which is a value near the state-of-the-art for integrated transmission lines in CMOS BEOL. The highest Q are reached with 30 µm of width (the maximum allowed by the technology) but they correspond to low characteristic impedances. Therefore, we choose a configuration for W equal to 20 µm to present the electrical characteristics versus frequency in the next section.

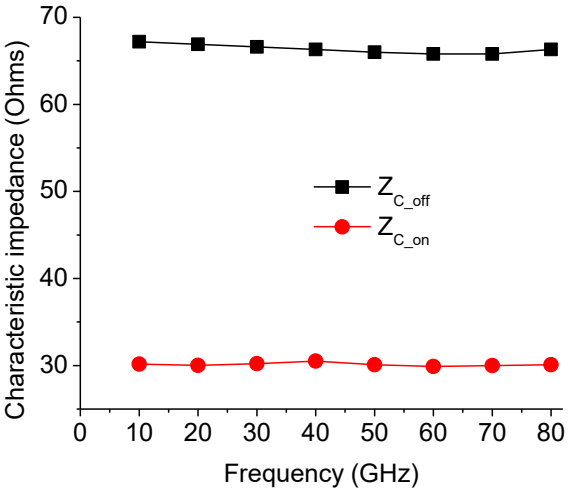
2.2.4.2. Simulation set 2 with l = 160 µm, frequency varies

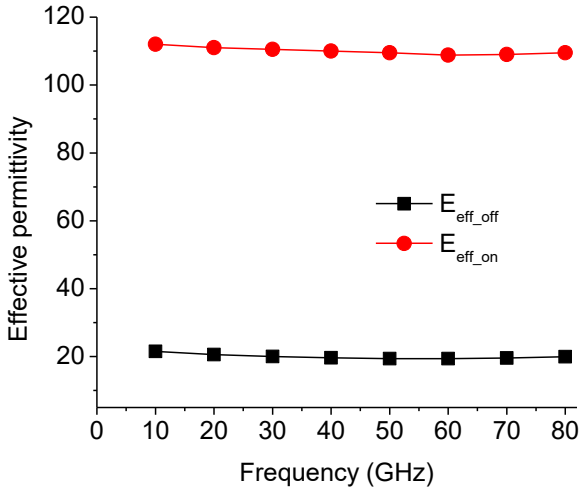
After the parametric study of the previous section, another example of simulation is shown. The fixed dimensions of the simulated TS-CPW are presented in Table 2-4. One can check that $+2 * G1 = 160\ \mu m$.

Table 2-4: Dimensions of the simulated TS-CPW.

Design parametrs	
W	20 µm
W_g	12 µm
G	110 µm
G_1	70 µm
G_2	40 µm
$SS = SL$	1 µm
w_e	70 µm

Figure 2-16 presents the electrical characteristics (characteristic impedance, effective permittivity, linear loss and quality factor) of the TS-CPW with the dimensions presented in Table 2-4.





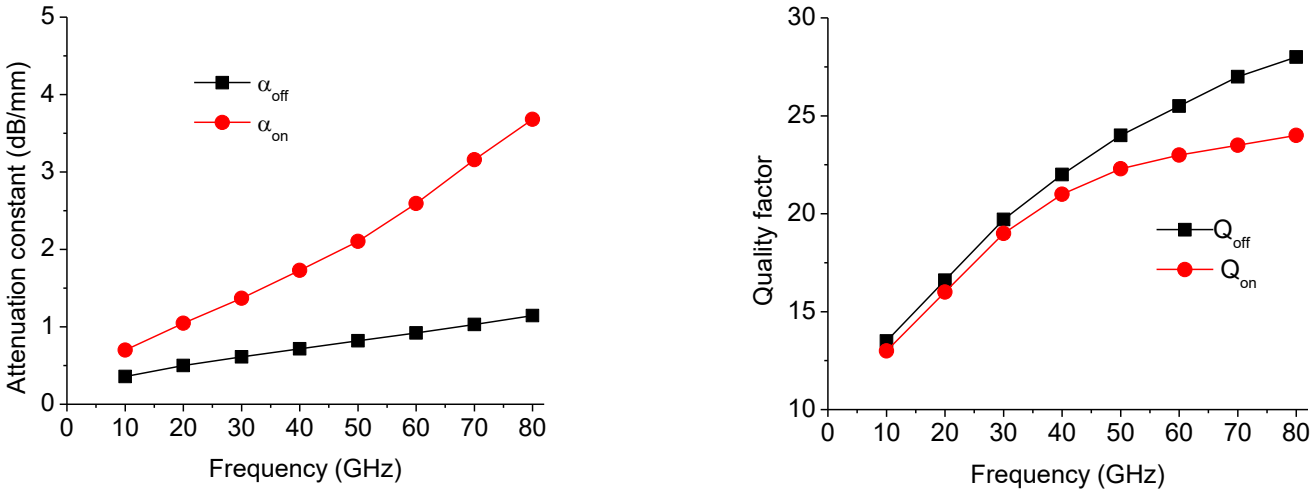


Figure 2-16: Electrical characteristics. (a) Characteristic impedance, (b) effective permittivity, (c) linear loss and (d) quality factor versus frequency.

From Figure 2-16 (a), the values of the characteristic impedances from ≈68 Ω in the off-state to ≈30 Ω in the on-state guaranty a return loss better than 10 dB in the whole frequency range. The average impedance of TS-CPW, defined as $\sqrt{Z_{c\_on}.Z_{c\_off}}$, is around 45 Ω. The effective permittivity is 4.5 times greater in the on-state than in the off-state, so that we can expect an on/off ratio a little higher than 2. The quality factor is varying between 13 at 10 GHz and 23 at 80 GHz in the on-state and from 12 at 10 GHz to 27 at 80 GHz in the off-state. It is better than 20 at 60 GHz.

As a consequence of the high variation of the effective permittivity between the off- and on-states, the electrical length of the TS-CPW will change as well. For this example, the electrical length is changed from 110° in off-state to 240° in on-state with 345 µm of physical length. This variation of the electrical length is named phase shift which can lead to design a phase shifter. Various phase shifters were designed and fabricated in IHP's SG25. They will be presented in chapter 3.

2.3.Previous works

In this section, three topologies of TS-CPWs based on distributed MEMS in classical MEMS technologies and a standard CMOS technology with post-process are described. These TS-CPWs were designed in our laboratory (IMEP-LaHC) and the LME laboratory of the University of Sao Paulo in Brazil. The first design was realized before my first year of PhD in the clean rooms. The second design was realized at the CEA by using their classical MEMS technology before the

beginning of my thesis. The third design on a standard AMS CMOS technology was performed independently from IMEP-LaHC, in the LME, during my first year of PhD. I participated by characterizing these TS-CPWs, up to 110 GHz, at IMEP-LaHC or on IHP's RF measurements platform. The measurement results will be presented in chapter 3 where the TS-CPWs are used to design tunable phase shifters.

2.3.1. Clean room technology: TS-CPW topology

Figure 2-17 presents the cross sectional view of the TS-CPW. The operating principle of TS-CPW in this technology is identical to the operating principle of TS-CPW in IHP technology. Here the substrate is glass due to its low cost and extremely low dielectric loss. To avoid the metal to metal contact (short circuit) between membrane and signal strip during actuation, a thin alumina layer of 50 nm is covering the CPW strips.

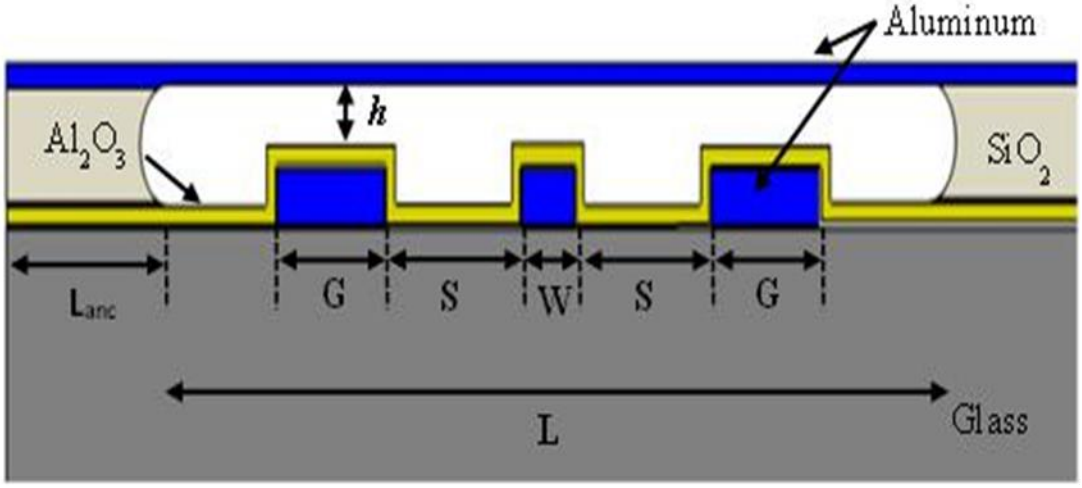


Figure 2-17: Cross sectional view of TS-CPW with the clean room MEMS technology.

The minimum actuation voltage needed in this topology to move the membrane is around 13 V. The parameters of the simulated and fabricated TS-CPW are: W = 29 µm, W_g = 20.5 µm, G = 40 µm, SS = 2 µm and SL = 2 µm.

2.3.2. CEA technology: TS-CPW topology

The tunable transmission line presented here is formed by a classical S-CPW as presented in [17], where the metallic ribbons that form the floating shielding are supported by another membrane that allows motion when a bias voltage is applied. The application of a DC voltage between the CPW strips and the shielding strips causes the membrane with shielding plane to move towards the CPW strips, due to the electrostatic force. Thus, the capacitance per unit length increases, reducing phase velocity, as explained in [18]. This TS-CPW was designed on a high resistivity silicon substrate.

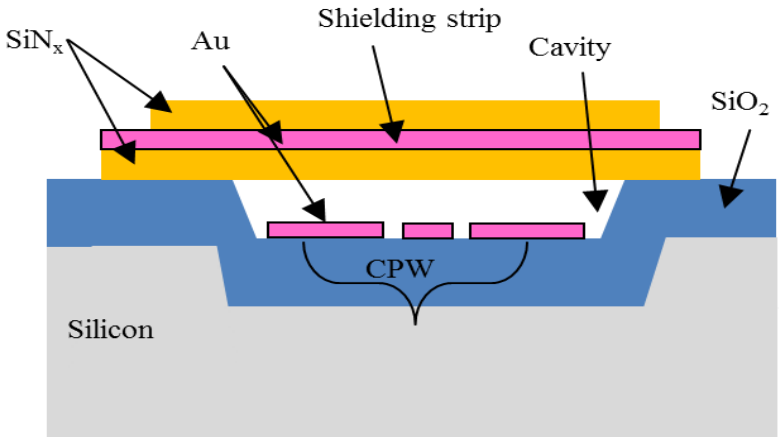


Figure 2-18: Cross sectional section of TS-CPW in the CEA MEMS technology.

In this topology, we do not need an electrode to activate the shielding strips because the strips of the CPW are used as electrodes. Then when this TS-CPW is measured, DC ground is connected to RF ground and the high voltage is applied onto the membrane.

2.3.3. AMS standard CMOS technology with post-process

As in the previous technologies, this proposed TS-CPW was fabricated within a commercial CMOS technology: the standard AMS 0.35 µm, and it is also based on classical S-CPW, with a little difference in topology anyway. Here, the CPW strips are over the shielding layer which is released and rendered mobile by removing the silicon oxide layers of the BEOL. They periodically rely on pillar made of SiO_2 in order to hold them in place (refers Figure 2-19).

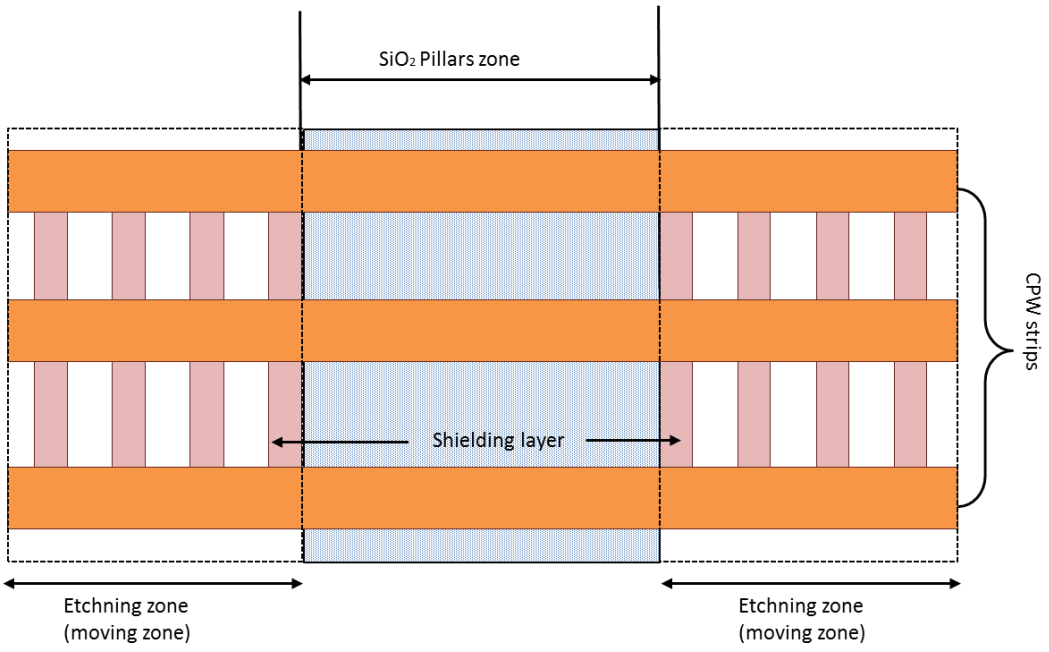


Figure 2-19: Top view of the TS-CPW with the Si O_2 pillars zone.

The actuation of the shielding layer is done via a DC voltage applied to the CPW strips while this shielding layer is DC grounded. In addition, mechanical stoppers are used to prevent a short circuit between the actuated membranes and the CPW strips. Figure 2-20 shows the cross sectional view of the proposed TS-CPW. The CPW strips where realized on the top metal layer (M4), the shielding layer on M2 and the stoppers on M3. The stoppers were anchored to the silicon substrate using vias.

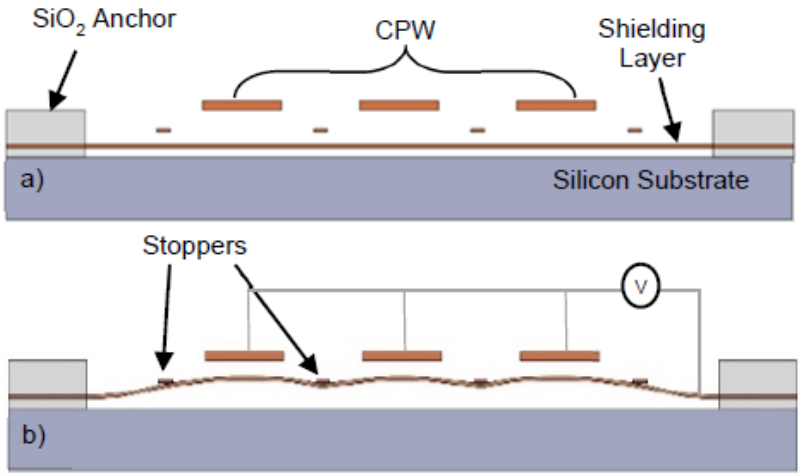


Figure 2-20: Cross sectional section of TS-CPW in the AMS technology. (a) Shielding layer at rest and (b) shielding layer actuated.

2.4.Conclusion

Table 2-5 gathers the physical parameters and performances of the simulated and sent to fabrication TS-CPWs in the 0.25 µm BiCMOS technology of IHP at 60 GHz. Note that the minimum activation voltage is around 32 V for this configuration.

Table 2-5: Geometry and performances of the simulated and sent to fabrication TS-CPWs in the IHP's SG25 at 60 GHz.

States	CPW layer	Floatting membrane layer	Dimensions						Performances			
			W (µm)	W_g (µm)	G (µm)	w_e (µm)	SS (µm)	SL (µm)	α (dB/mm)	Q	ε_{eff}	Z_c (Ω)
Off-state	**M2**	**M3**	20	12	180	70	1	1	1.5	28	20	68
On-state	**M2**	**-**	20	12	180	70	1	1	2.1	22	114	30

In this chapter, a new concept of integrated tunable CPW for mm-wave applications compatible with BiCMOS technology has been proposed. The concept is based on TS-CPWs where the slow-wave effect leads to very interesting characteristics in terms of quality factor and longitudinal length reduction. The TS-CPW is based on distributed MEMS. Electromagnetic simulations were done in order to extract the electrical characteristics and follow their evolution with the variation of the geometrical dimensions and frequency. Besides, the design methodology of the TS-CPW in IHP's BiCMOS technology was described in details. The transmission line measurements, either at off-state or on-state, will be detailed in the last chapter.

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Chapter 3

Design of digital phase shifters

In chapter 1, a review of the existing technologies for tunability, i.e. ferroelectrics [20], liquid crystal [2], MOS [36] and MEMS [4], was presented. It was concluded that MEMS and CMOS technologies lead to the highest Figure of Merit and the lowest surface area, respectively.

Also, several topologies of passive phase shifters are available, i.e. reflection type [5], switched line [6] and loaded line [51]. A new topology of tunable coplanar waveguide [52]-[53] based on distributed MEMS was presented in chapter 1 and chapter 2. In this chapter, a loaded line phase shifter is studied. It is based on MEMS-based TS-CPWs.

First, earlier N-bit phase shifters in MEMS technology, designed at IMEP-LaHC in collaboration with other institutes, and tested during my PhD, are presented. Then several phase shifters designed by myself are studied, with different degrees of maturity. First, a 1-bit phase shifter is studied, which uses the TS-CPWs designed in chapter 2. Then, the design methodology of an N-bit phase shifter with N commands is described in sections 3.3 and 3.4.

3.1.Previous Work

This thesis work is based on two patents [52], [53] and some previous work, i.e. clean room technology (PTA), CEA technology and AMS technology. These technologies have been described in chapter 1 (section 1.5). In previous works, phase shifters were developed in several technologies and were based on distributed MEMS S-CPWs. In this section, a brief description of previous phase shifter designs is presented in order to understand the improvements that were carried out during my thesis. The measurement results of these phase shifters are presented in chapter 4 dedicated to measurement results.

3.1.1. Clean room phase shifter design: PTA

A digital phase shifter was designed and fabricated [10]. The structure of this phase shifter is shown in Figure 3-1. This phase shifter is constituted of only 4 groups. All groups have the same length and each group is connected to one pad. So, there are 4 digital commands, which lead

theoretically to 16 states of phase. However there are 11 redundant states due to the symmetry of the structure. For instance, states 0001 and 1000 give exactly the same phase shift, and states 0001, 0010, 0100 and 1000 give almost the same phase shift (small differences are due to standing wave effect that differ from one state to another). Finally, this phase shifter has only 5 different states: at rest (state 0000); when only the first group is actuated (state 0001); when first and second groups are actuated (state 0011); when the three groups are actuated (state 0111) and when all groups are actuated (state 1111). It behaves like a thermometer. This phase shifter was designed to achieve 135° of phase shift at 60 GHz

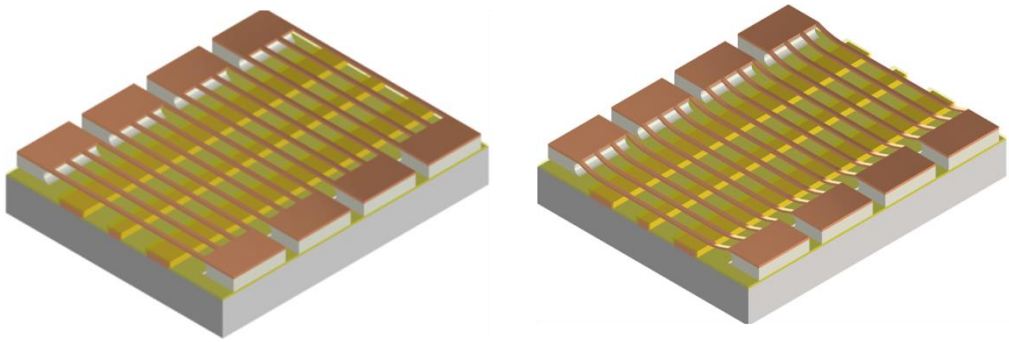


Figure 3-1: Structure of the realized phase shifter with PTA technology. (a) Off-state (b) on-state (all groups actuated).

3.1.2. CEA phase shifter design

Figure 3-2 presents the structure of a distributed MEMS phase sifter using the CEA MEMS technology [11]. The shielding ribbons of the S-CPW were divided in groups that can be actuated independently. Ideally, to obtain n-bits of resolution the shielding ribbons should be distributed into 2^n groups. However, the phase shift is not linear with respect to the length of each group, because of the different characteristic impedances shown between actuated and unactuated sections leading to standing waves formation and hence a non-linear phase variation. Therefore, in this first design, even if 128 phase shift positions were obtained with the use of 7 groups, corresponding to 7 commands, this phase-shifter is only a 3-bit one enabling to achieve 8 very precise phase shift steps given by the number of bits. Anyway, many phase shift steps occur between the latter's, and can be used in practice.

The Bragg effect must be considered when designing the phase shifter, since a periodic-like high-low characteristic impedance structure may appear for certain states. In order to minimize the Bragg effect, the groups were subdivided in eight interlaced sections, as exemplified in Figure 3-2.

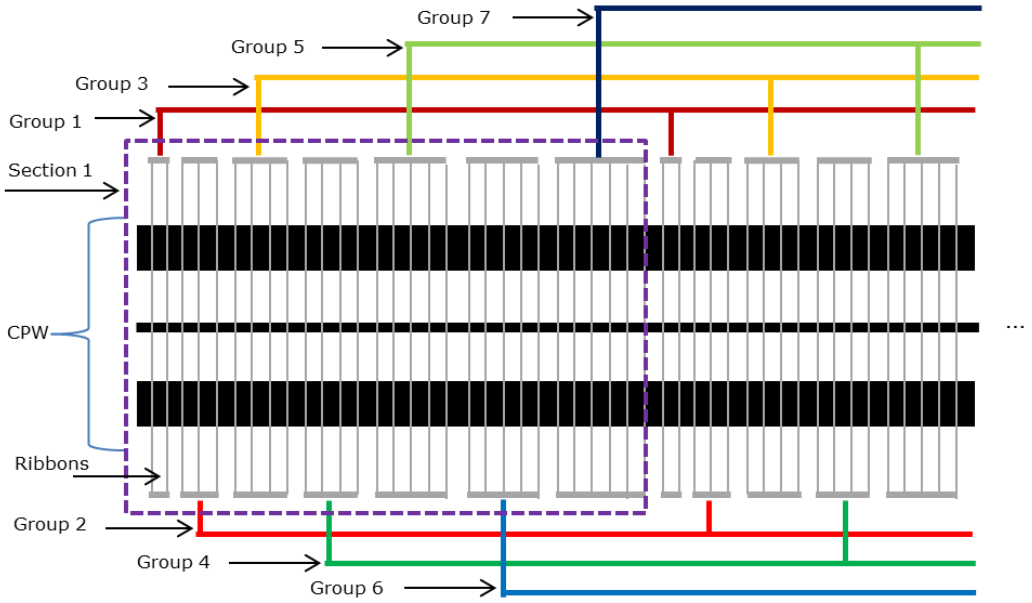


Figure 3-2: the distributed MEMS phase shifter in CEA technology.

This phase shifter was designed to achieve a maximum phase shift of 152°. The phase shift resolution between two successive states is around 21°.

3.1.3. AMS phase shifter design

In this technology, a 2-bit phase shifter was designed [12]. The proposed phase shifter is constituted of 3 groups of membranes in order to achieve 2 bits of resolution. Normally, 2-bit phase shifter has 4 states of phase. In this phase shifter, we have 8 states of phase with 4 linear states to obtain 2-bit resolution. The other 4 states are not linear due to asymmetry of the structure. Figure 3-3 shows the structure of the 2-bit phase shifter designed and fabricated in AMS technology.

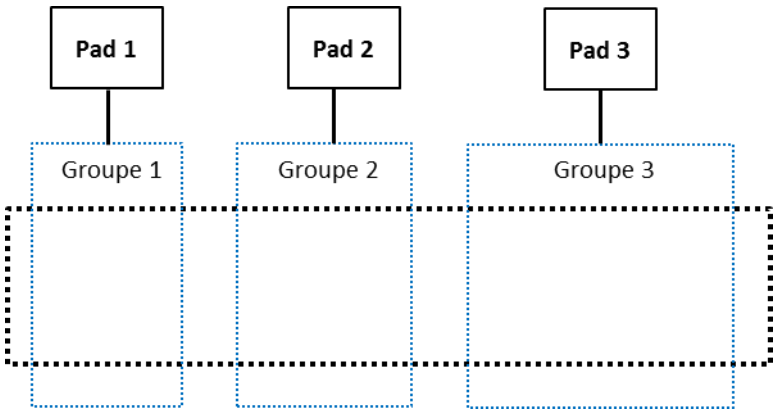


Figure 3-3: Top of the 2 bit phase shifter in AMS technology.

This phase shifter was designed to have a maximum phase shift of 45° at 60 GHz. It has 4 different states: at rest (state 00); a smallest phase shift is achieved with the actuation of only one group (Group1: state 01); the next phase state is obtained with the actuation of two groups (Group 1 and Group 2: state 10) and the maximum phase state is obtained with all three groups actuated (Group 1, Group 2 and Group 3: state 11).

3.2.TS-CPW as a 1-bit phase shifter

3.1.4. Principle

As explained in previous chapters, the use of a slow-wave approach allows shrinking the transmission line size by increasing the effective dielectric constant, which finally enhances its quality factor.

As discussed in chapter 2 also, the TS-CPW is composed of a conventional CPW loaded by a patterned shield, which is electrically controlled via a bias voltage in order to change the characteristics of the TS-CPW. In IHP's SG25 this shield is implemented over the CPW strips. Figure 3-4 reminds the topology and the parameters of a TS-CPW designed in IHP's SG25.

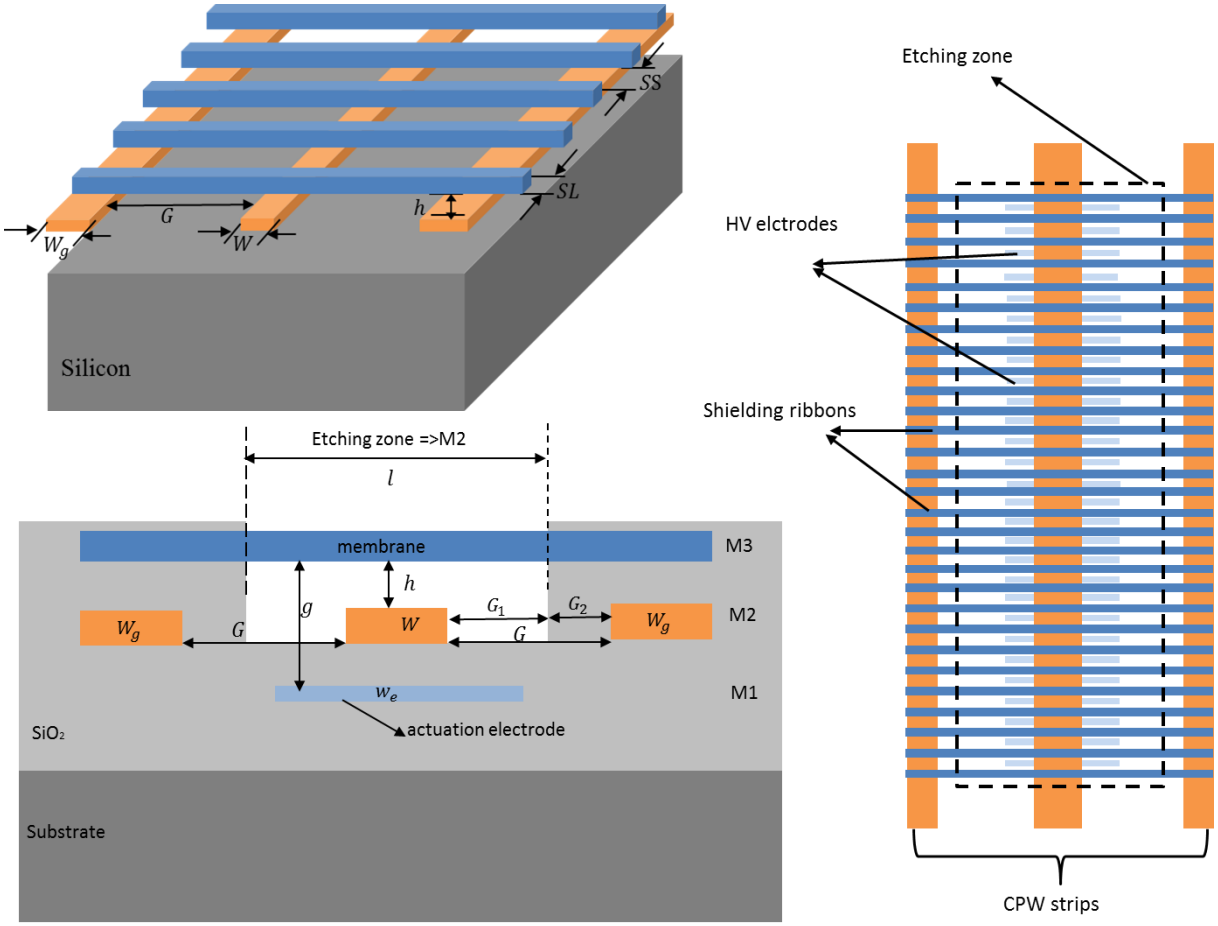


Figure 3-4: TS-CPW. (a) Topology, (b) Cross sectional view and (c) Top view.

When moving from *off*-state to *on*-state by applying a bias, the electrical length of the TS-CPW is changing as well. We can define a phase for each state: φ_{off} and φ_{on} (see eq. (3-1) and (3-2)). The difference between these two phases is called phase shift ($\Delta\varphi$) (see eq. (3-3) to (3-6)). Therefore, the TS-CPW is working as a 1-bit phase shifter because it has only two states, i.e. *off*- and *on*-.

$$\varphi_{off} = \beta_{off}.l \quad \textbf{(3-1)}$$

$$\varphi_{on} = \beta_{on}.l \quad \textbf{(3-2)}$$

$$\varphi_{off} - \varphi_{on} = (\beta_{off} - \beta_{on}).l \quad \textbf{(3-3)}$$

$$\Delta\varphi = \varphi_{off} - \varphi_{on} \quad \textbf{(3-4)}$$

$$\Delta\beta = (\beta_{off} - \beta_{on}) \quad \textbf{(3-5)}$$

$$\Delta\varphi = \Delta\beta.l \quad \textbf{(3-6)}$$

3.1.5. Need to combine the moveable ribbons

DC pads are necessary to apply the bias voltage. It is not possible to bias each ribbon individually; hence all ribbons of a group were connected together, with only one DC command, as shown in Figure 3-5. The connections also permit to "rigidify" the moveable ribbons.

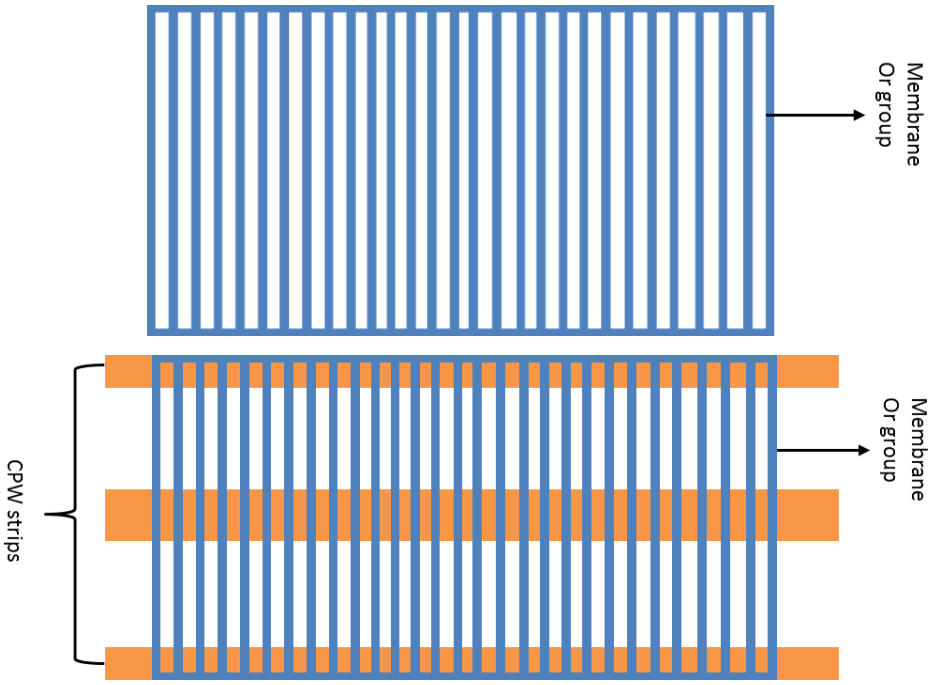


Figure 3-5: Top view. (a) Group of 1-bit phase shifter and (b) TS-CPW.

3.3.Phase shifter (N bit/N commands): design1

3.1.6. Principle

The idea, as for the CEA based phase shifter, consists in combining the ribbons in several groups as shown in Figure 3-6, and to develop in main time a design methodology that permits to reduce the number of commands to the number of bits, i.e. an N-bit phase shifter with only N commands.

For this purpose, the design procedure consists in optimizing the number of ribbons in each group. As an example, Figure 3-6 shows the TS-CPW as a succession of n similar groups. The distance between two successive groups is equal to *SS* to maintain the same slow-wave effect along the entire length of the TS-CPW.

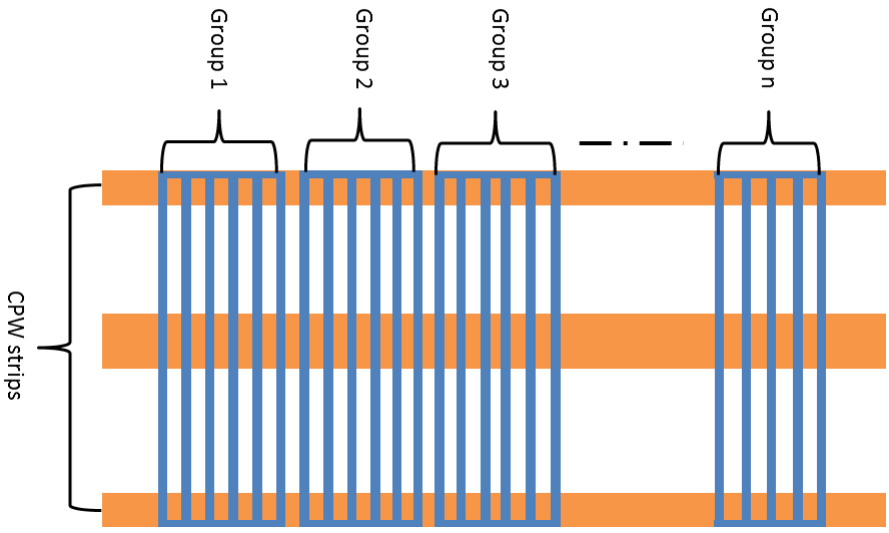


Figure 3-6: Top view of TS-CPW with a repetition of n similar groups.

The way to optimize the number and the size of groups is described in section 3.1.7.

Before describing the design methodology, it is important to clearly define **group** and **segment** definitions.

3.3.1.1. Group definition

As discussed above, the ribbons will be combined in several groups. A small study in this sub-section is presented to find the right shape forming the groups.

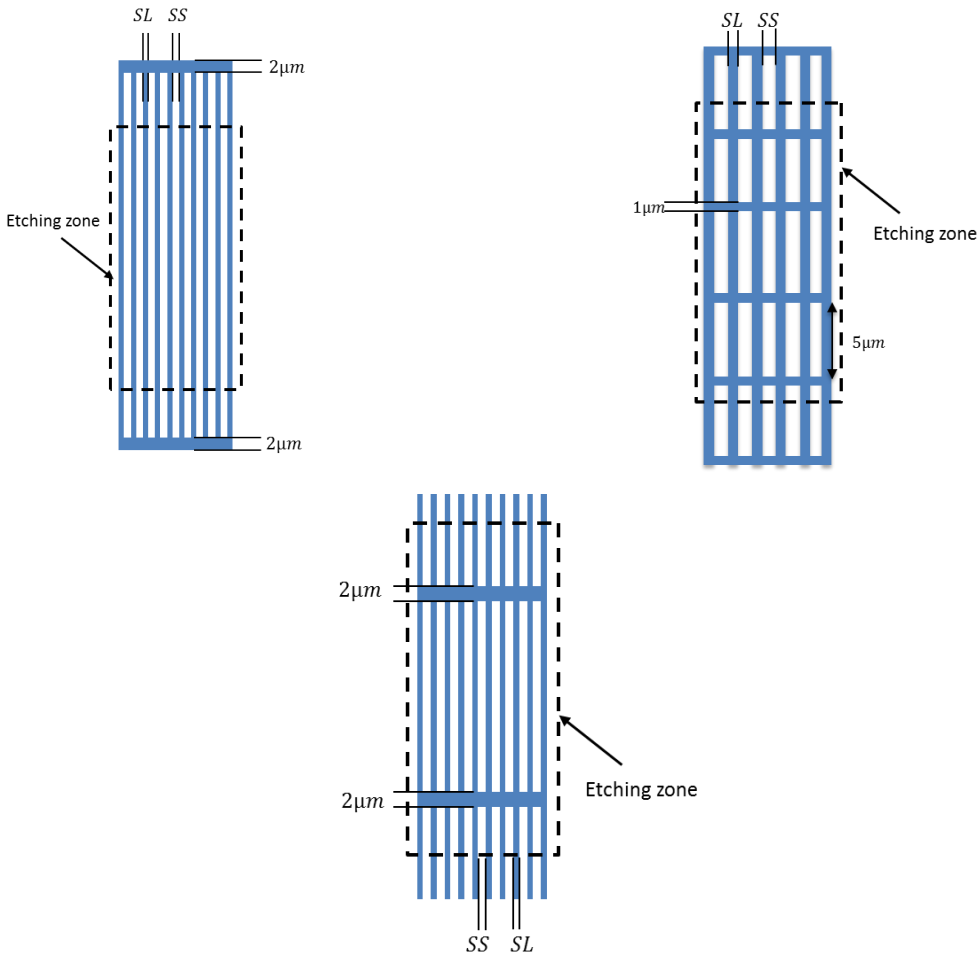


Figure 3-7: Group. (a) Shape 1, (b) shape 2 and (c) shape 3.

In first shape (Figure 3-7 (a)), the two strips of width 2 µm, the ones that force a same potential for all the ribbons of a same group, are fixed in the oxide, letting a long moveable part of ribbons. Hence the group of ribbons lacks rigidity. The second shape is shown in Figure 3-7 (b). Here, we force the ribbons to a unique potential with many strips of width 1 µm, which also enable to stiffen the structure. The electrical characteristics of the simulated TS-CPW for the two shapes in off-state are given in Table 3-1.

Table 3-1: Comparison of the electrical characteristics of the TS-CPW versus the shapes of group.

Shapes	Z_c (Ω)	Q	ε_{reff}
Shape 1	65	25.2	19
Shape 2	58	10.5	16
Shape 3	65	25	18.6

From calculated values of inductance and capacitance per unit length, we can determine the characteristic impedance ($Z_c = \sqrt{L/C}$) and effective permittivity ($\varepsilon_{reff} = C_0^2 \cdot L \cdot C$), given in Table 3-1. The inductance per unit length is a little bit smaller in shape 2 as compared to

shape 1, as the stiffening strips slightly prevent the magnetic field from circulating. Consequently the corresponding characteristic impedance and effective permittivity are lower. What's more, shape 2 offers much possibilities for eddy current losses, hence leading to a much lower quality factor as compared to shape 1.

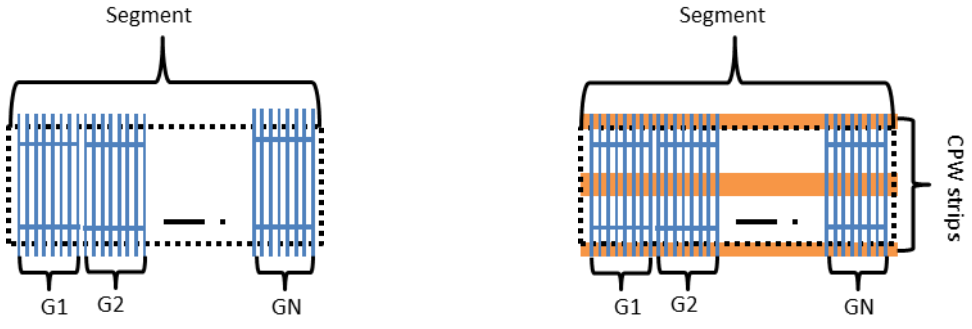
Shape 3 (Figure 3-7(c)) was proposed to overcome the problem of high eddy currents of shape 2 and low rigidity of shape 1. The electrical performance is almost the same as shape 1. However, shape 3 is more rigid in the etching zone as compared to shape 1.

So, the final definition for group is: **a set of ribbons spaced 1 µm from each other. These ribbons are connected by two metal strips of width 2 µm placed in the moveable part of group. Its size is variable and depends on the number of ribbons. Note that the length of the group will always be equal to an odd value or it can be null.**

3.3.1.2. Segment definition

The segment is constituted of a set of groups, as shown in Figure 3-8(a). The number of bits of the phase shifter determines the maximum number of groups per segment, for example a 3-bit phase shifter corresponds to a maximum of 3 groups per segment. But the number of segments is variable, it is determined during the optimization procedure. The segment of an N-bit phase shifter with the CPW strips and p segments of an N-bit phase shifter are plotted in Figure 3-8(b) and Figure 3-8(c), respectively.

Finally the definition of segment is: **set of groups spaced of 1 µm from each other. Its size depends on the size of group which is variable and the number of group per segment. The maximum number of groups per segment corresponds to the number of bit resolution of the designed phase shifter.**



(a) (b)

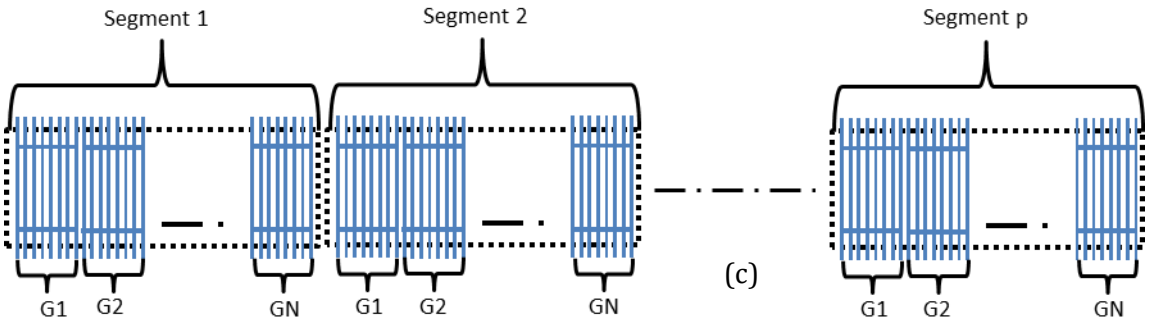


Figure 3-8: Top view of, (a) 1 segment of N groups, (b) 1 segment of N groups with the CPW strips drawn on the picture and (c) p segment of N groups.

It is important to note that all first groups of each segment are connected to the same DC command. In other words, first group of segment 1 is connected to first group of segment 2 up to segment p. That does not mean that group 1 of segment 1 has the same number of ribbons than group 1 of segment 2 or segment p. This is just a question of DC command. On the contrary, each length of each group is optimized for the best final linearity between phase shift states.

3.1.7. Design methodology: 3-bit phase shifter design 1

Figure 3-9 describes the flow diagram of the design methodology of the phase shifter (N bit/N commands).

In step 1, the dimensions of the TS-CPW and their respective metal layers are fixed. This step was described in chapter 2. The electrodes, the CPW strips and the moveable ribbons were implemented in Metal 1, Metal 2 and Metal 3, respectively, as described in section 2.2 chapter 2. Table 3-2 summarizes the dimensions of the used TS-CPW.

Table 3-2: Dimensions of the TS-CPWs used for design 1.

Dimensions	
W	20 µm
W_g	12 µm
G	110 µm
G_1	70 µm
G_2	40 µm
$SS = SL$	1 µm

In step 2, β_{off} and β_{on} are extracted for a particular frequency, from HFSS simulations of *off*- and o*n*- states of small sections of TS-CPW (for example 150 µm of length). Also, the difference $\Delta\beta$ between β_{off} and β_{on} is calculated in this step in order to determine the physical length of the phase shifter corresponding to the desired phase shift. For example, a 60 GHz phase

shifter with a total phase shift of $\Delta\varphi$ =157.5° leads to $\Delta\beta = 7963{,}7$ rad/mm, leading to a physical length equal to 345 µm.

In step 3, the parameters of the phase shifter are defined: number of segments (p), number of bits (N) and number of individual ribbons for each group that is to say the length of each group, to be chosen among a certain number of possible lengths (m in total). For example: p=5 segments were used to design a 3-bit phase shifter. This means N=3 groups maximum in a segment (N-bits / N-commands). Eventually one group may have no ribbon at all (length of 0 µm). As a matter of fact, the number of groups in the corresponding segment will be less than 3. As a general rule for optimization, a group length can only show odd values varying from 9 µm to 39 µm with a step of 2 µm. Thus, the number of possible lengths for each group is m=17 i.e. 0, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39).

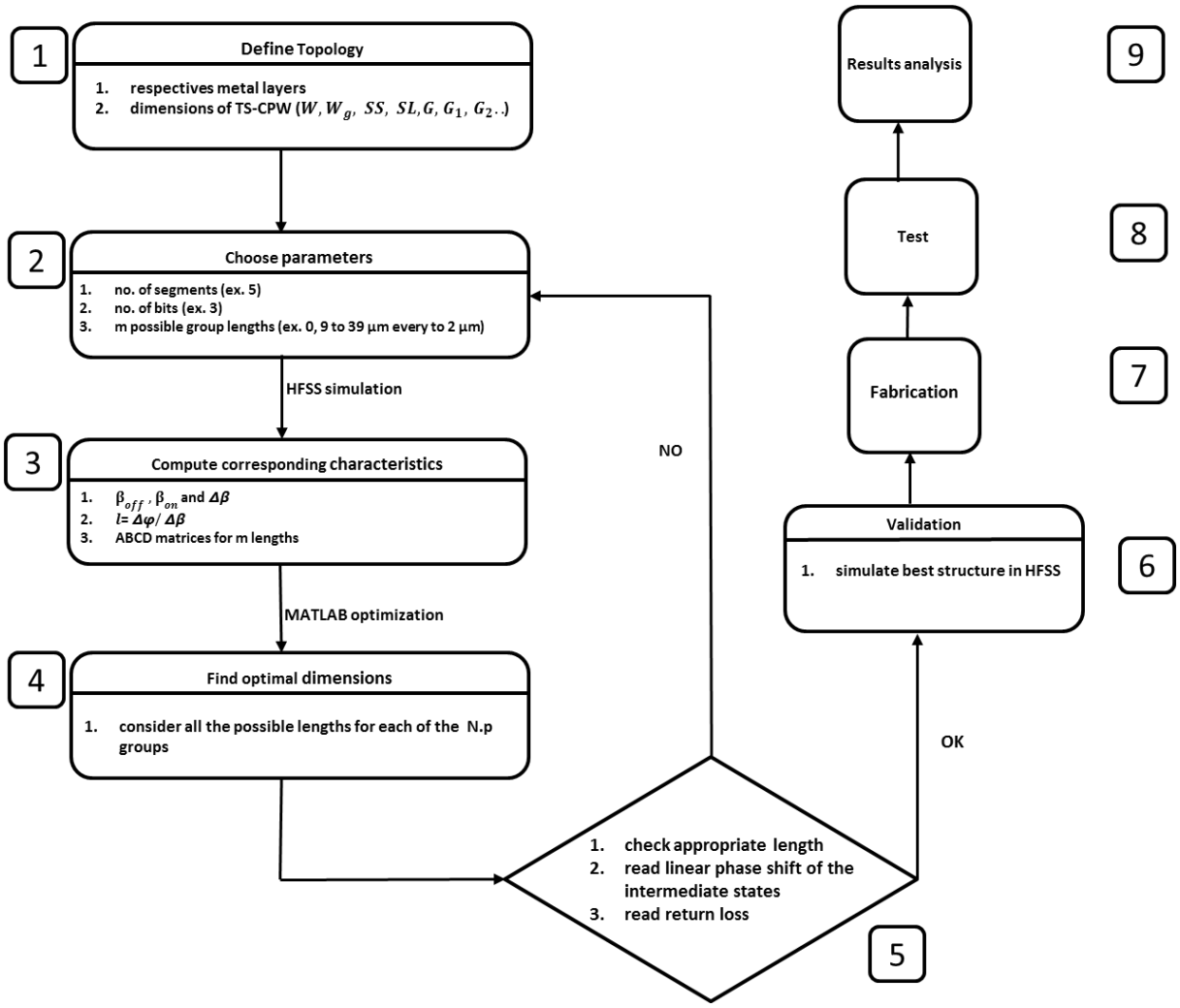


Figure 3-9: Flow diagram of the design methodology.

In step 4, the optimal dimension of each group in each segment is determined. Figure 3-10 shows the sub-steps of step 4. Firstly, one segment is generated with all possibilities of groups

lengths (m^N combinations available). For example, for a 3-bit phase shifter: 17 possible lengths for a group and 3 possible groups in a segment lead to 17^3combinations for one segment. Then, the combination of one segment is repeated p times to generate all segments (remember that the number of segments p is fixed by the designer). So there are $(m^N)^p$ segments possible, hence $(17^3)^5$ possibilities. Next, in order to find the maximum of possibilities we classify the total segments according the total length of phase shifter calculate in step 3 with condition $l_{min} < l < l_{max}$. l_{min} and l_{max} are chosen close to the exact value of l (with error value of 3%) . For example, for the length 345 µm , we put condition 335 µ$m < l <$ 355 µm. After this sub-step, the possibilities (solutions) leading to physical lengths close to l are known. Also, the corresponding lengths for each group per segment are known.

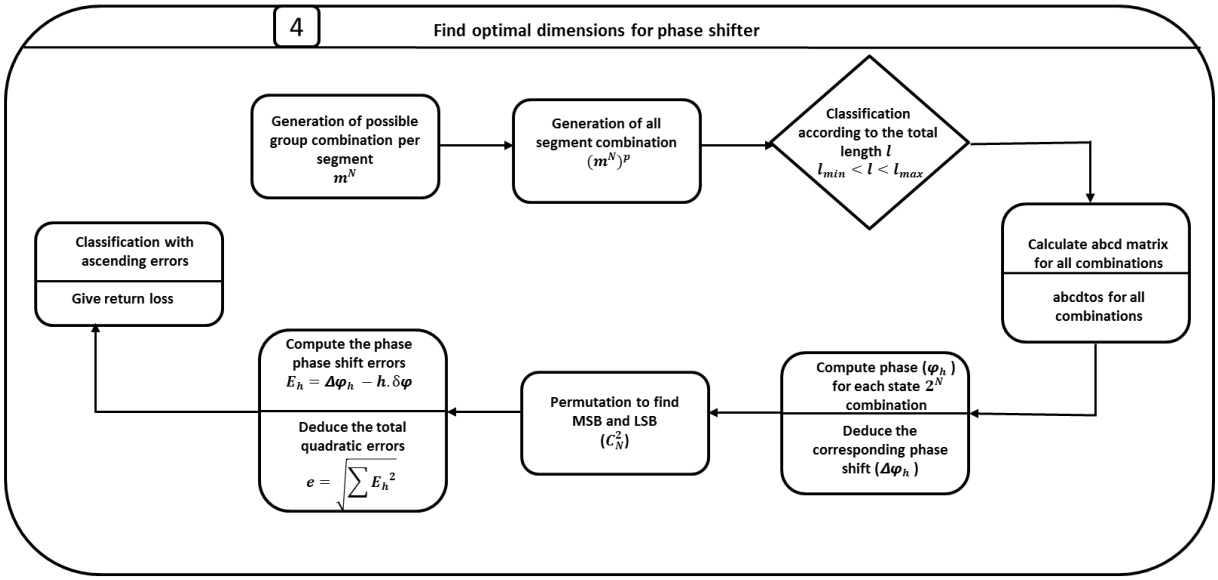


Figure 3-10: Detail of step 4 from flow diagram of the design methodology.

Then, the ABCD matrix for all valuable combinations is calculated by cascading the ABCD matrix of each group already calculated during HFSS process, as shown in Figure 3-9 and eq.(3-7). Eq (3-7) corresponds to the case of 5 segments of 3 groups maximum each. Then the corresponding S parameters are calculated, followed by the calculation of phase φ_h of the hth state of the N-bit phase shifter for all combinations. Then the overall phase shifts $\Delta\varphi_h$ between the first state φ_0, which is the *off*-state, and the last state φ_{2^N-1} (see eq. (3-9)) are calculated. Note that h varies from zero to $2^N - 1$. The input return loss is calculated as well as it can also make good criteria of discrimination.

$$[ABCD]_{ijk} = [ABCD\ segment\ 1]_{ijk} * [ABCD\ segment\ 2]_{ijk} * [ABCD\ segment\ 3]_{ijk} * [ABCD\ segment\ 4]_{ijk} * [ABCD\ segment\ 5]_{ijk} \quad \textbf{(3-7)}$$

with **(3-8)**

$$[ABCD\ segment\ s]_{ijk} = [ABCD\ group\ 1\ of\ segment\ s]_i * [ABCD\ group\ 2\ of\ segment\ s]_j * [ABCD\ group\ 3\ of\ segment\ s]_k$$

with i=0 or 1 / j=0 or 1 and k=0 or 1, 0 is for *off-state* and 1 for *on-state.*

Also, the phase shift of the eight states of a 3-bit phase shifter is,

$$\Delta\varphi_h = \Delta\varphi_{ijk} = \varphi_{ijk} - \varphi_{000} = \varphi_h - \varphi_0 \quad \textbf{(3-9)}$$

$$\Delta\varphi_{000} = 0$$
$$\Delta\varphi_{001} = \varphi_{001} - \varphi_{000}$$
$$\Delta\varphi_{010} = \varphi_{010} - \varphi_{000}$$
$$\Delta\varphi_{011} = \varphi_{011} - \varphi_{000}$$
$$\Delta\varphi_{100} = \varphi_{100} - \varphi_{000}$$
$$\Delta\varphi_{101} = \varphi_{101} - \varphi_{000}$$
$$\Delta\varphi_{110} = \varphi_{110} - \varphi_{000}$$
$$\Delta\varphi_{111} = \varphi_{111} - \varphi_{000}$$

where, φ_{000} and φ_{111} are the phases when no group is actuated and all groups are actuated, respectively. The rest of the intermediate states are expected to vary linearly.

Then, from eq. (3-10) we can calculate the phase shift errors E_h for each state in all possibilities and we deduce the total quadratic errors e with eq. (3-12):

$$E_h = \Delta\varphi_h - (h.\delta\varphi) \quad \textbf{(3-10)}$$

$$\text{where } \delta\varphi = \frac{\Delta\varphi}{2^N - 1} \quad \textbf{(3-11)}$$

$$e = \sqrt{\sum {E_h}^2} \quad \textbf{(3-12)}$$

where $\delta\varphi$ given in eq. (3-11) is the phase shift step to reach linear intermediate phases. For example for 3-bit phase shifter with 157.5°of maximum phase shift, $\delta\varphi$ is equal to 22.5°. Then, the errors for each state are calculated as follows:

$$E_{000} = \Delta\varphi_{000} - 0° \quad \textbf{(3-13)}$$
$$E_{001} = \Delta\varphi_{001} - 22.5°$$
$$E_{010} = \Delta\varphi_{010} - 45°$$
$$E_{011} = \Delta\varphi_{011} - 67.5°$$
$$E_{100} = \Delta\varphi_{100} - 90°$$

$$E_{101} = \Delta\varphi_{101} - 112.5°$$
$$E_{110} = \Delta\varphi_{110} - 135°$$
$$E_{111} = \Delta\varphi_{111} - 157.5°$$

The final sub-step in step 4 is the selection of the best combination: the one that fits the total targeted length and that gives the minimum error for the 3-bit phase shifter. With 5 segments for a 3-bit phase shifter, the best combination is shown in Figure 3-11.

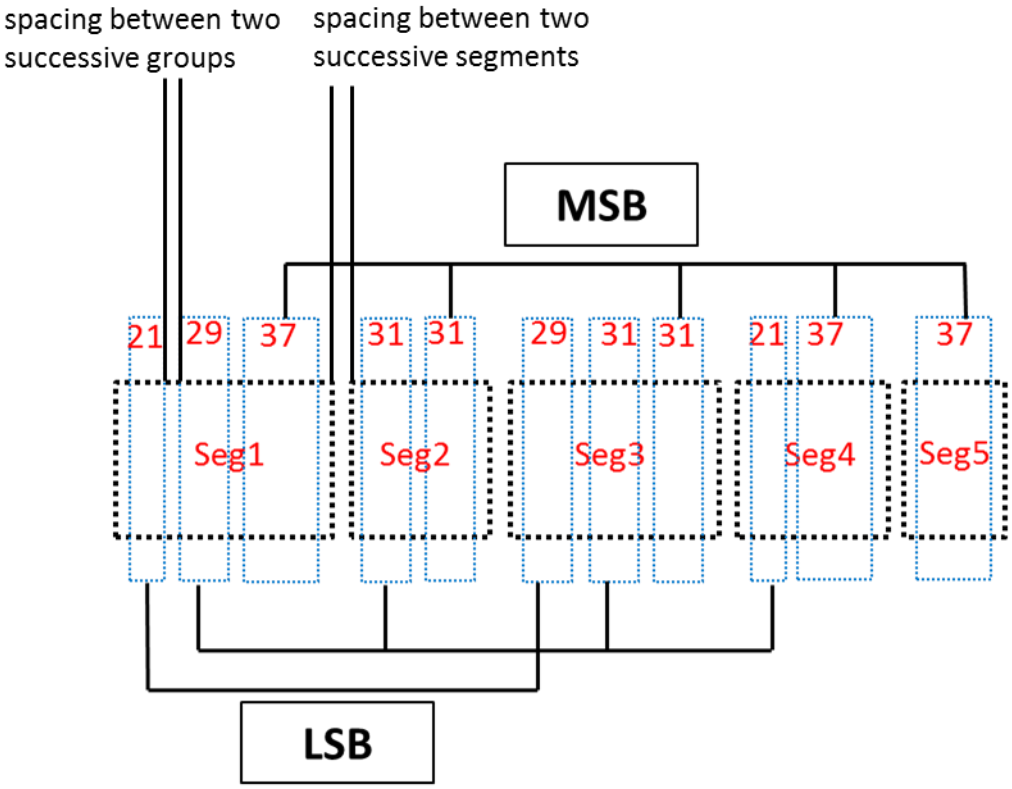


Figure 3-11: Structure of the 3-bit phase shifter with minimum average phase shift error.

From Figure 3-11, it can be seen that the second and fourth segments have only two groups, whereas the fifth segment has only one group. This was obtained by the optimization procedure described above. The first segment has 90 µm of length (3 groups: 21 µm +1 µm of space, 29+1 µm and 37+1 µm). The second segment has 64 µm of length with 2 groups of 31+1 µm. The third segment has 94 µm of length (1 group of 29+1 µm, 2 groups of 31+1 µm). The fourth segment has 60 µm of length (1 group of 21+1 µm and 37+1 µm and 1 space). The last segment has a length of 37 µm, leading to a total physical length of 345 µm. Note that we performed some mistakes in this first design by forgetting the space length between groups in MATLAB computation (for MATLAB, the total length was 335 µm). The phase shift for the 8 states of this combination and their corresponding errors are given in Table 3-3.

Table 3-3: Phase shift for the 8 states of the proposed structure and their corresponding errors.

	Phase shift	Phase shift errors
$\Delta\varphi_{000}$	0°	-
$\Delta\varphi_{001}$	22.6°	0.1
$\Delta\varphi_{010}$	46.4°	1.4
$\Delta\varphi_{011}$	67.4°	0.1
$\Delta\varphi_{100}$	87°	0.7
$\Delta\varphi_{101}$	116.5°	4
$\Delta\varphi_{110}$	140°	5
$\Delta\varphi_{111}$	155°	2.5

From Table 3-3, it can be seen that the maximum phase shift error is 5° for state 110.

In step 5, the best combination determined in step 4 is simulated in HFSS. The validation step is presented in section 3.1.9.

3.1.8. 315° phase shifter (3 bits/ 3 commands)

Before the validation step, a 315° 3-bit phase shifter was designed, with a simple idea of cascading two 157.5° 3-bit phase shifters. Note that combining two 157.5° 3-bit phase shifters leads to twice the phase shift error, leading to a -10° of error for state 110. Figure 3-12(a) shows the 315° phase shifter obtained by this simple way. To reduce the phase shift errors of states 101 and 110, an additional segment containing only one group of 21 µm was added, as shown in Figure 3-12(b). The latter is actuated only with states 101 and 110.

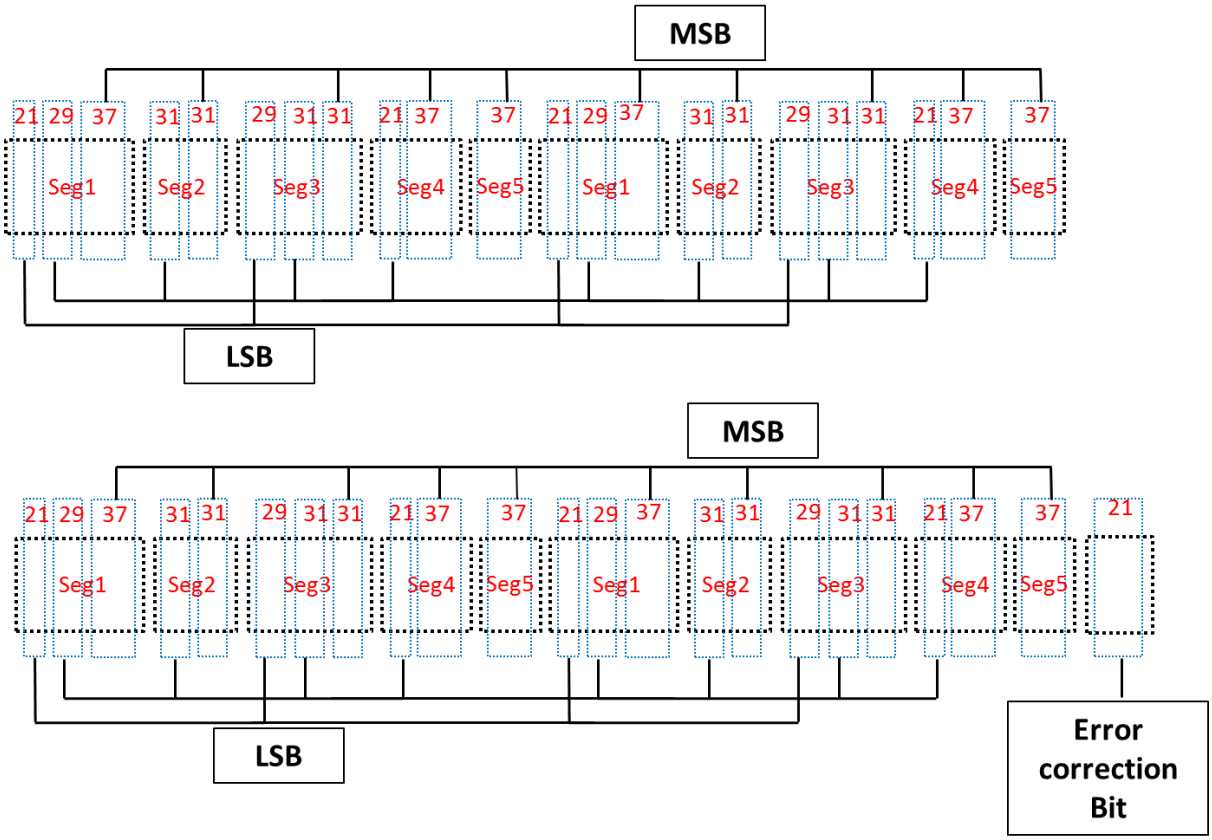
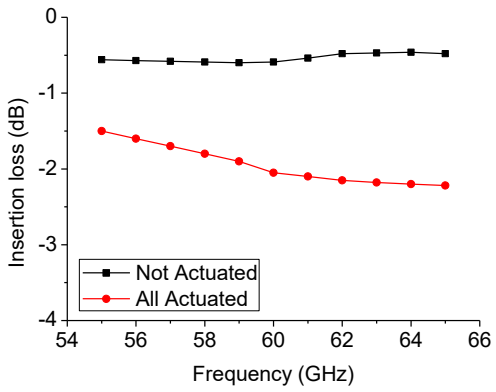


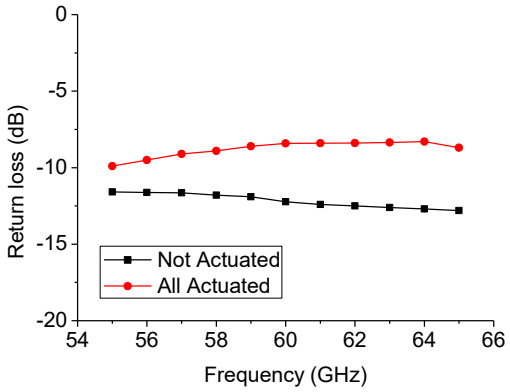
Figure 3-12: Structure combination of 360° phase shifter, (a) with 3 commands and (b) with additional bit for error correction.

3.1.9. HFSS simulation

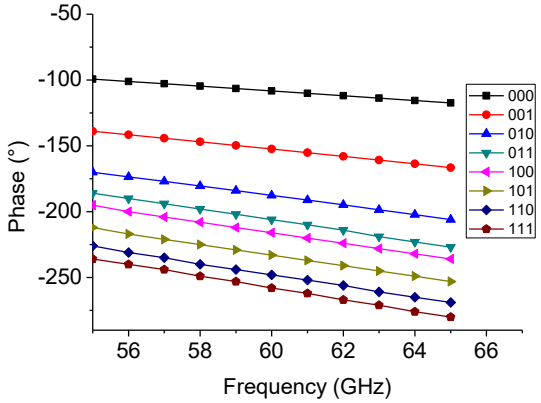
To proceed with step 5 of the design methodology in section 3.1.7, the 157.5° 3-bit phase shifter was simulated up to 65 GHz using HFSS. The insertion loss and the return loss of the off- and on-states (000 and 111) of the distributed MEMS phase shifter are given in Figure 3-13 (a) and (b). Figure 3-13(c) presents the phase of the 8 states.



(a)



(b)



(c)

Phase shift @60 GHz (°)	HFSS	MATLAB
$\Delta\varphi_{000}$	0	0
$\Delta\varphi_{001}$	47	22.6
$\Delta\varphi_{010}$	82	46.4
$\Delta\varphi_{011}$	101	67.4
$\Delta\varphi_{100}$	114	87
$\Delta\varphi_{101}$	131	116.5
$\Delta\varphi_{110}$	145	140
$\Delta\varphi_{111}$	151	155

(d)

Figure 3-13: HFSS simulation results of the157.5° phase shifter. (a) Insertion loss (b) return loss, (c) phase, and (d) phase shift

As shown in Figure 3-13 (a), an insertion loss of 2 dB is obtained at 60 GHz for 151° of phase shift. The insertion loss has a maximum variation of only 1.6 dB. The return loss is better than 8 dB for off- and on-states. By comparing the phase shift obtained by HFSS simulation with MATLAB algorithm in Figure 3-13(d), it can be seen that the total phase shift $\boldsymbol{\Delta\varphi_{111}}$ is in a good agreement (151° for HFSS and 155° for MATLAB). But this is not the case for the other states, i.e. $\boldsymbol{\Delta\varphi_{001}}$ to $\boldsymbol{\Delta\varphi_{110}}$. This difference in HFSS simulation is due to the fact that there exist geometric discontinuities when cascading on- and off- groups consecutively. This discontinuity is taken into account by HFSS simulator in all states but not in MATLAB algorithm. We note that the characteristic impedances vary from ≈68 Ω in the *off*-state to ≈30 Ω in the *on*-state. This is the guaranty for a return loss better than 10 dB in the whole frequency range. The average impedance for the phase shifter, defined as $\sqrt{\boldsymbol{Z_{c\_on}}.\boldsymbol{Z_{c\_off}}}$, is around 45 Ω.

Same analysis can be carried out for the 315° 3-bit phase shifter. As mentioned in section 3.1.8, this phase shifter is designed by cascading two 157.5° phase shifters, so the mismatch between HFSS and MATLAB algorithm is even higher for states 001 to 110. In Figure 3-14, the insertion loss, return loss and phase of *off*- and *on*-states are presented.

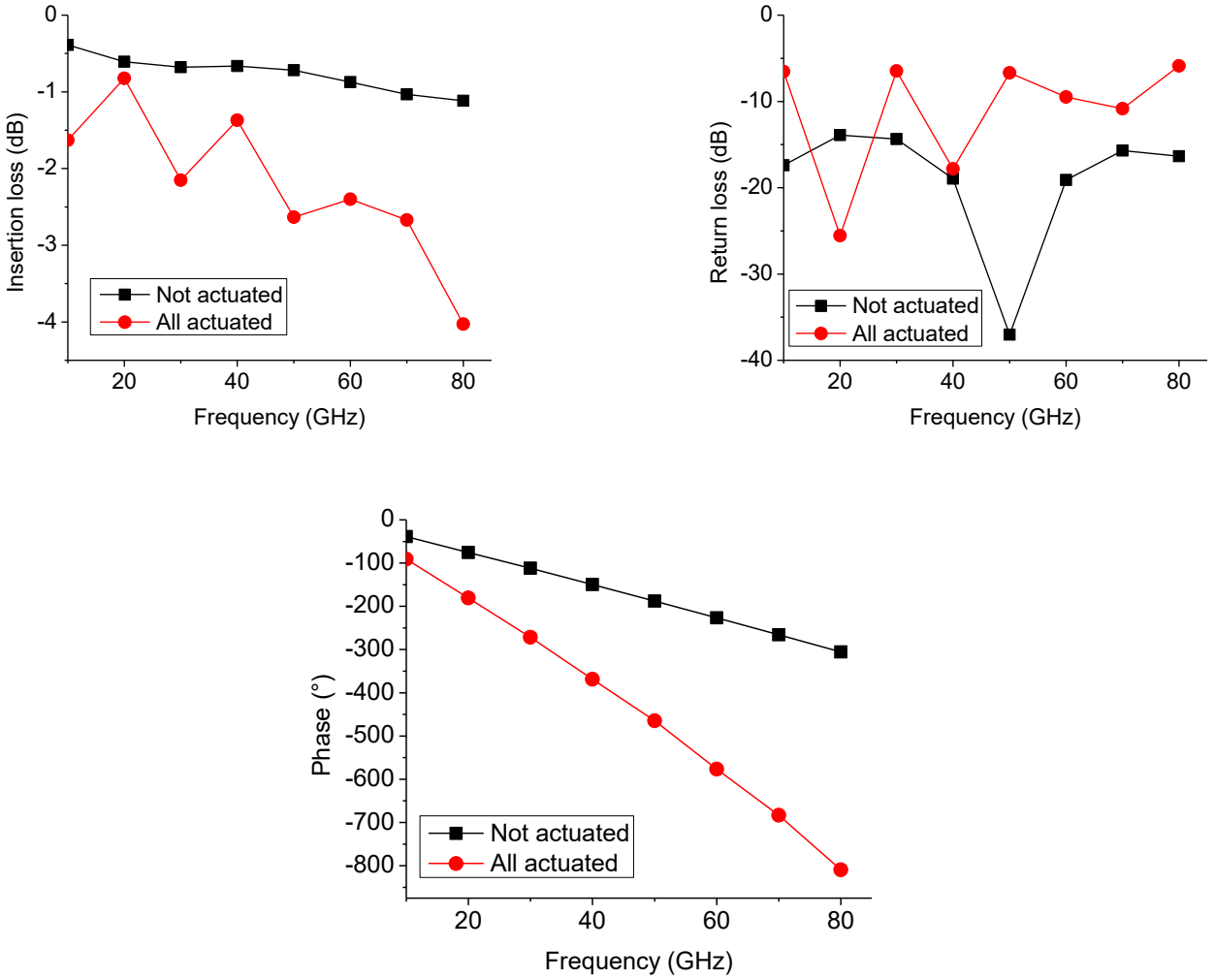


Figure 3-14: HFSS simulation results of the distributed MEMS 315°phase shifter. (a) Insertion loss, (b) return loss and (c) phase.

As shown in Figure 3-14, the insertion loss is 0.7 dB and 2.2 dB at 60 GHz for off- and on-states, respectively. The return loss is as low as 7 dB for the worst case. This is an issue that was addressed in an optimized design described in the next section, whereas the total phase shift at 60 GHz is approximately the same for MATLAB algorithm and HFSS simulation.

This phase shifter with and without the additional bit for error correction was sent to fabrication in March 2014 before the validation in HFSS.

3.4.Optimized Phase shifter: design 2

3.1.10. Proposed solution

In step 4 in the design methodology in section 3.1.7, we did not consider the space (1 µm) between two groups, neither the transition effect when we cascaded the ABCD matrices. This transition between two successive groups does not have a high effect when the phase shifter has

the same state throughout the transmission line, i.e. *off*-state (all groups not actuated) and *on*-state (all groups actuated). Never-the-less this transition or discontinuity has a great effect when successive groups do not have the same state (i.e. the consecutive groups are *on* and *off*). We can deduce that we have four transitions possible: *off-off*, *off-on*, *on-off* and *on-on* transitions. The problem occurs in the *off-on* and *on-off* transitions. The ABCD matrices of these transitions were taken into account in the new calculation in the developed MATLAB algorithm.

After simulating the four possible transition states in HFSS, S parameters of each transition were extracted. Then, the ABCD matrices were calculated. So, a new equation (eq. (3-15)) is derived from eq. (3-7) considering the ABCD matrices of transition states $[ABCD\ T]_{l\to n}$ where $[ABCD\ T]_{l\to n}$ describes the transition, materialized by the space between the group in the l -state (l stands for *on*- or *off*-) and the following group in the n-state (n stands for *on*- or *off*-).

$$[ABCD]_{ijk} = [ABCD\ segment\ 1]_{ijk} * [ABCD\ segment\ 2]_{ijk} * [ABCD\ segment\ 3]_{ijk} * [ABCD\ segment\ 4]_{ijk} * [ABCD\ segment\ 5]_{ijk} \quad \textbf{(3-14)}$$

with

$$[ABCD\ segment\ s]_{ijk} = [ABCD\ group\ 1\ of\ segment\ s]_i * [ABCD\ T]_{i\to j} * [ABCD\ group\ 2\ of\ segment\ s]_j * [ABCD\ T]_{j\to k} * [ABCD\ group\ 3\ of\ segment\ s]_k\ **\ [ABCD\ T]_{k\ segment\ s\to i\ segment\ s+1} \quad \textbf{(3-15)}$$

with i=0 or 1 / j=0 or 1 and k=0 or 1, 0 is for *off*-state and 1 for *on*-state. When s=5, there is no final transition.

3.1.1. Design issues

Before starting the design and optimization of this 'second round' 3 bit phase shifter, an important issue to be considered was the rigidity of the distributed MEMS which is presented in chapter 4, as any mechanical or electrical characterization. With 'first round' of measurement, we remarked that, within a segment, if the adjacent groups were not in the same *on*- or *off*-position, for example in state 010 the actuated second group disturbs the adjacent first and third groups in *off*-position. This problem exists for all intermediate states, i.e. from 001 to 110. Due to this reason 'first round' measurements could only be performed for states 000 and 111. To make this design more rigid, the side walls of each membrane (i.e. the inner and outer ribbons for each group) were made wider as compared to other ribbons within the group, as shown in Figure 3-15.

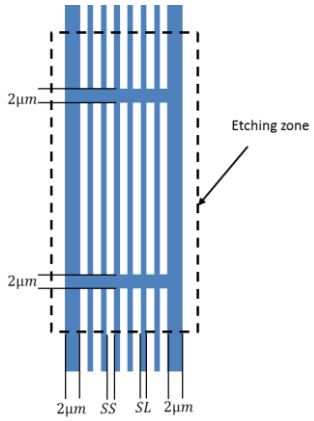


Figure 3-15: New structure for a group.

The second modification that was carried out to avoid this problem of shorting between adjacent groups is the increase of the distance between the groups. In order to find the optimum gap between the groups, S_g, we calculated the pull-in voltage vertically and horizontally. The vertical pull-in voltage refers to the minimum voltage applied between the electrodes and membranes (eq. 3-13) to move the groups vertically, whereas the horizontal pull-in voltage refers to the minimum computed voltage between two adjacent groups that makes them to attract (eq. 3-14).

$$V_{p\_vertical} = \sqrt{\frac{8.K}{27.\varepsilon_0.A}{g_0}^3} \quad \textbf{(3-16)}$$

$$V_{p\_horizontal} = \sqrt{\frac{8.K}{27.\varepsilon_0.A}{S_g}^3} \quad \textbf{(3-17)}$$

To move the membranes vertically and not horizontally, $V_{p\_horizontal} > V_{p\_vertical}$. This condition leads to $S_g > g_0$. Then, for an initial gap $g_0$of 2.53 µm (gap between Metal 1 where membranes are placed and Metal 3 where electrodes are placed), the space between two successive groups must be more than 2.53 µm. So, for this new design, two cases will be tested: the space between groups, S_g ,will be fixed to 3 µm in one case and to 2 µm in the other case as 3 µm sounded too large to prevent electric field from leaking to silicon substrate.

3.1.2. Validation of the solution

As for design 1, process flow starts at step 1 of the design methodology. The metal layers are the same as design 1, but the dimensions of the TS-CPW were modified (see Table 3-4).

Table 3-4: Dimensions of the TS-CPWs used for design 2.

Dimensions	
W	28 µm
W_g	16 µm
G	110 µm
G_1	70 µm
G_2	40 µm
$SS = SL$	1 µm
Side wall SL	2 µm
S_g	2.5 µm
w_e	70 µm

The new TS-CPW was simulated with HFSS. The characteristic impedance varies from 57 Ω for *off*-state to 19 Ω for *on*-state, leading to an average characteristic impedance of 33 Ω. The quality factor is more than 20 for both *off*- and *on*-states.

As mentioned in section 3.1.7, the number of segments must be fixed by the designer. So to increase the number of possibilities, the number of segments was fixed to p=11. Then, the number of group lengths was reduced to 0, 25, 27, 37 µm (m=4) in order to reduce the MATLAB computation time necessary to evaluate all the possibilities which total number equals $(m^N)^p = (4^3)^{11}$. The lengths are still odd values. The gap between two adjacent groups is considered in the transition. The same design algorithm than that of step 4 (section 3.1.7) was followed but with optimized ABCD matrices as defined in section 3.1.10. The structure of the new 3-bit phase shifter with 157.5° of phase shift is shown in Figure 3-16.

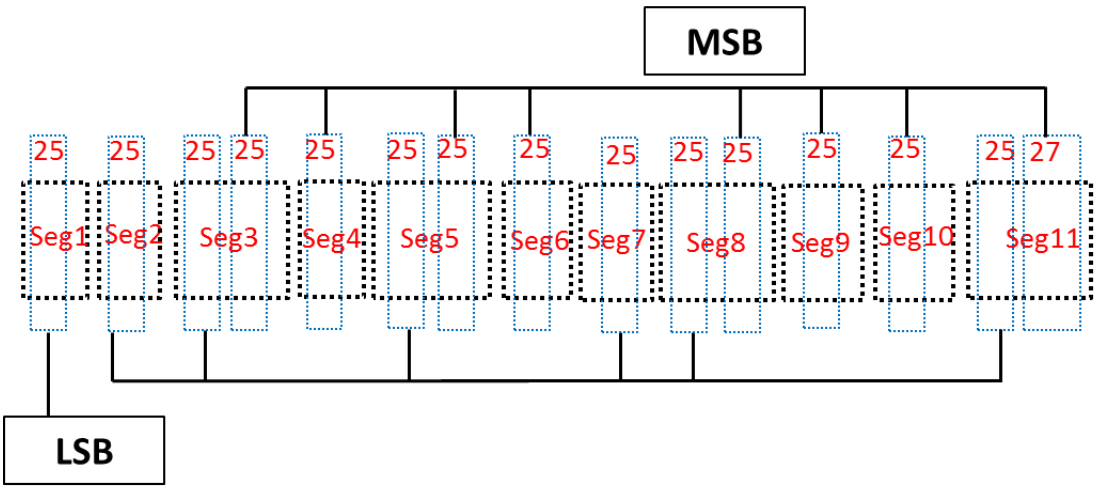
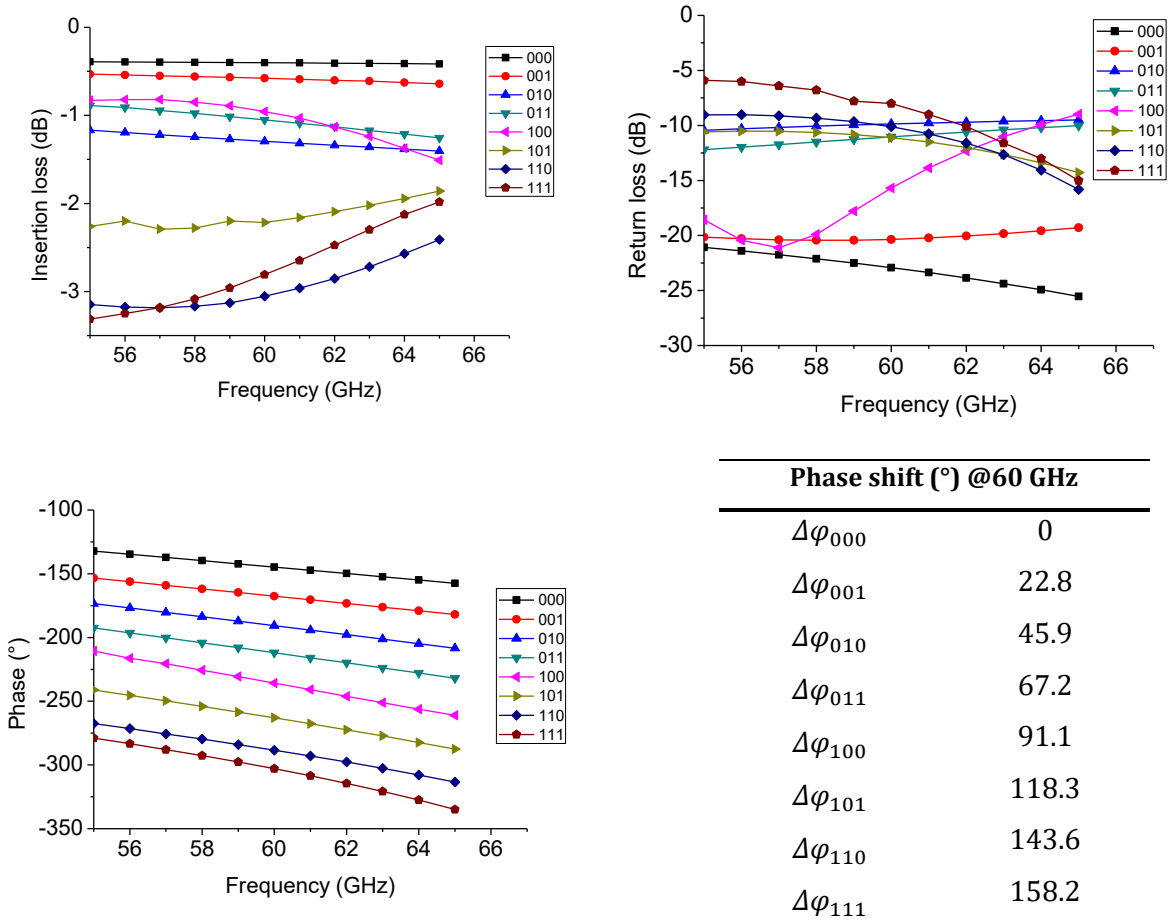


Figure 3-16: Structure of the optimized 3 bit phase shifter with minimum phase shift error.

As shown in Figure 3-16, the structure of the phase shifter is made of 14 groups of 25 µm and 1 group of 27 µm. The total physical length of the phase shifter is thus 407 µm (407.8 µm more precisely) including the distance between groups. The simulated performance of the optimized 157.5° 3 bit phase shifter is given in Figure 3-17.



Phase shift (°) @60 GHz	
$\Delta\varphi_{000}$	0
$\Delta\varphi_{001}$	22.8
$\Delta\varphi_{010}$	45.9
$\Delta\varphi_{011}$	67.2
$\Delta\varphi_{100}$	91.1
$\Delta\varphi_{101}$	118.3
$\Delta\varphi_{110}$	143.6
$\Delta\varphi_{111}$	158.2

Figure 3-17: HFSS simulation results of the optimized distributed MEMS phase shifter in IHP SG25 technology. (a) Insertion loss (b) return loss, (c) phase and (d) phase shift.

The maximum simulated insertion loss is 0.5 dB for *off*-state and 2.8 dB for *on*-state at 60 GHz. whereas the simulated return loss is better than 7 dB for all the states from 58 to 65 GHz frequency range. The phase shift in consecutive states is quite linear. The states 101 and 110 present the maximum of phase errors, i.e. 5.8° and 8.6° for 101 and 110, respectively. This simulated performance in HFSS is approximately matching with MATLAB algorithm (10% of error). We note that the characteristic impedances vary from ≈56 Ω in the *off*-state to ≈21 Ω in the *on*-state guaranty a return loss better than 7 dB in the whole frequency range. The average impedance for this phase shifter is around 34 Ω.

3.5.Conclusion

In this chapter a new concept of integrated distributed MEMS phase shifters based on TS-CPW for mm-waves applications was proposed. The use of the shielding layer as a moveable layer leads to a great design flexibility. A design methodology for an N bit phase shifter with N commands was developed. For a proof-of-concept, a 3 bit phase shifter with 158° of total phase shift was designed with eight linear states of phase at 60 GHz. The second generation of this 3 bit phase shifter was sent to fabrication in October 2015.

The layout and measurements of the fabricated TS-CPW and phase shifter are presented in Chapter 4. To explain discrepancies between simulated and measured phase shifts, an electrical model is also derived in Chapter 4 in order to study the evolution of the capacitance ratio between *off*- and *on*-states when varying the geometrical dimensions.

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Chapter 4

TS-CPWs and phase shifters measurements

In chapter 1, a review on various tunable phase shifting techniques is carried out. Then, our solution, based on tunable slow-wave coplanar waveguides (TS-CPW) with a distributed MEMS approach, including the description of the BiCMOS 0.25-µm IHP technology used for realization, is outlined. Also the technologies used for three other previous works, anterior to my PhD and performed at IMEP-LaHC in collaboration with the University of Sao Paulo and the CEA, are presented. In chapter 2, the TS-CPWs based on distributed MEMS are described in depth. A focus is made on their design, depending on the four technologies enfaced, mine and the three others. The millimeter wave N-bit phase shifters designs and their simulation results are explained in chapter 3. A specific focus is performed on the design methodology I developed to match the number of command to the number of bits of my phase shifters.

In this chapter, the measurement results of the various phase shifters are presented: first, the measurements of the previous phase shifters, next, the IHP phase shifters (optical, electrical, and RF measurements). Then, a discussion about substrate parasitic effect is done. And finally, a comparison with state-of-the art is made.

4.1.Previous Work measurements

The measurements of the previous millimeter wave phase shifters (PTA, CEA and AMS) previously presented in section 3.1 (chapter 3) are shown in this section. All phase shifters are measured in IMEP-LaHC platform.

4.1.1. Clean room (PTA) phase shifter

The PTA phase shifter was fabricated and measured from 10 to 70 GHz by Marcus Pelegrini [1] in 2013 before the beginning of my PhD. Figure 4-1 shows a MEB view of the fabricated phase shifter. These measurement results are given in Figure 4-2.

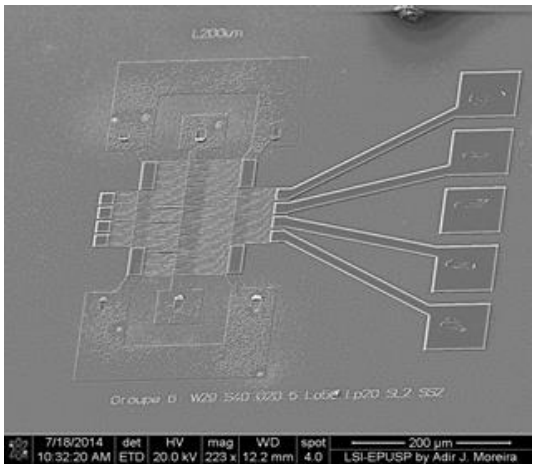


Figure 4-1: MEB view of the PTA phase shifter measured at 60 GHz.

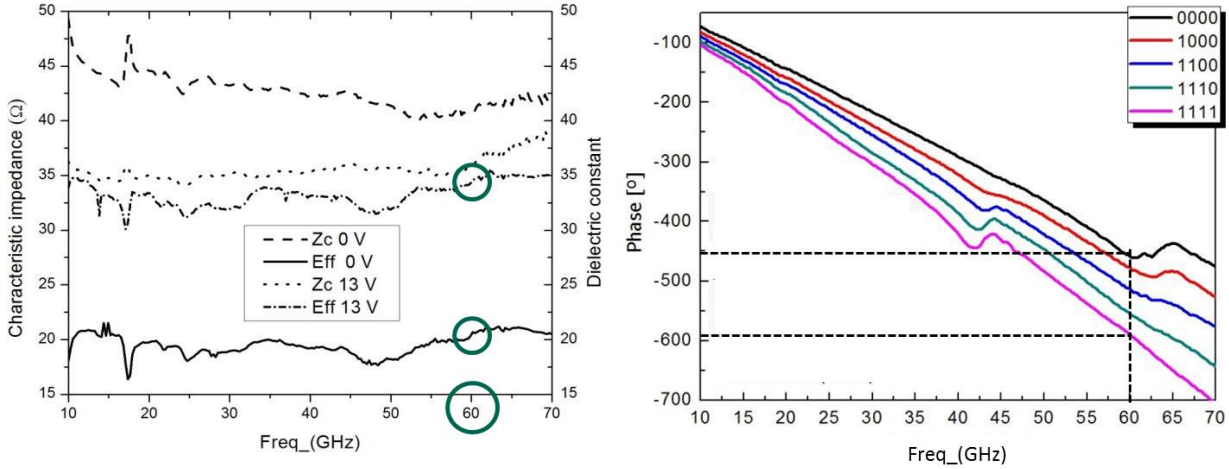


Figure 4-2: Measurement results of the PTA phase shifter. (a) Characteristic impedance and dielectric constant and (b) phase.

The *off*- and *on*-states of phase shifter were measured between 10 and 70 GHz. Then, the electrical parameters of the TS-CPW, shown in Figure 4-2, were extracted using Mangan method [2] for de-embedding. The characteristic impedance and the effective dielectric permittivity are shown in Figure 4-2(a). At 60 GHz, Z_c varies from 41 Ω for 0 V (*off*-state) to 36 Ω for 13 V (*on*-state), which leads to 38 Ω as an average impedance. Meanwhile, at 60 GHz ε_{eff} grows from 20.5 at 0 V, to 34.5 at 13 V. Figure 4-2(b) shows the measured phase of the five states of phase shifter. The total phase shift measured at 60 GHz is 131°. We can observe due to the standing waves effect an undulation of phase. The attenuation constants at 60 GHz are 1.7 dB/mm and 2.5 dB/mm for 0 V and 13 V, respectively. Then we can deduce some figures-of-merit of 93°/mm and 52°/dB. It is important to note that due to the van der Waals attraction forces the membranes are sticking with the RF strips after actuation. They are not rigid enough to compensate for this attraction. Hence these phase shifters cannot be measured again.

4.1.2. CEA phase shifter

The Figure 4-3 shows an optical microscope image of the fabricated 3-bit phase shifter in CEA-MEMS technology. This phase shifter was designed by Gustavo REHDER [11] and measured by myself at the IMEP-LaHC platform from 0 to 70 GHz. The phase shifter is 1.375 mm long and 340 µm wide, excluding RF and DC pads, leading to a total area of 0.47 mm^2. Large DC pads were used in this structure for wire bonding interconnection of the segments of each group.

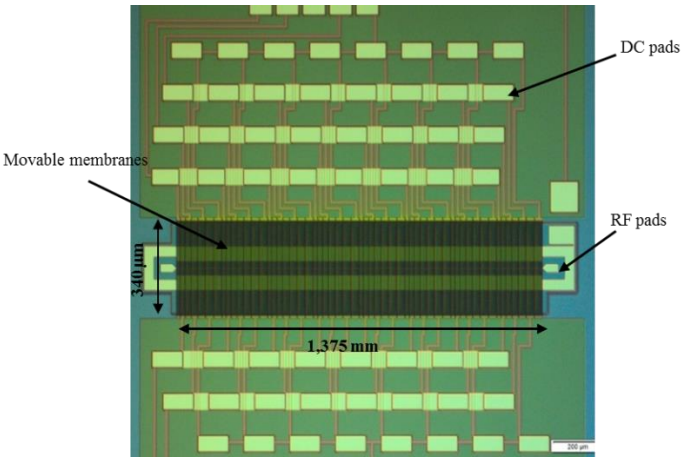


Figure 4-3: Optical microscope image in CEA-MEMS technology.

By applying DC voltage to the RF pads (RF ground and signal), and connecting the DC ground to the shielding layer (movable membrane), some pull-in and pull-out voltages of 17 V and 10 V were measured, respectively. The voltage was swept from -40 V to +40 V as shown by the capacitance versus voltage C(V) curve in Figure 4-4. A small shift in the pull-in/pull-out was observed as the voltage was cycled several times. This indicates that the dielectric is charging, which is a well-known failure mechanism for capacitive MEMS switches.

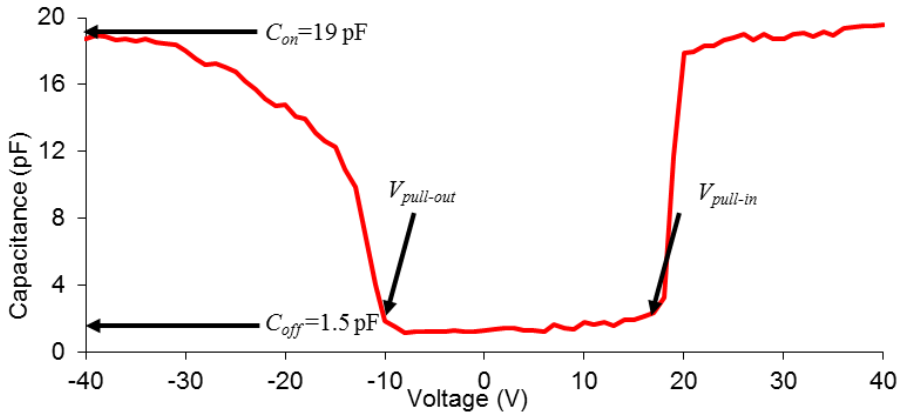


Figure 4-4: Measurement of the pull-in and pull-out voltages of the distributed MEMS phase shifter with CEA technology.

We can see from Figure 4-4 that the C_{off} and C_{on} are 1.5 pF and 19 pF, respectively. Hence the capacitance ratio C_{on}/C_{off} is around 12.6 that allows obtaining a strong phase shift per unit length.

This phase shifter was measured in weak signal (S-parameters) using a vector network analyzer from DC to 67 GHz. The RF measurement results are presented in Figure 4-5.

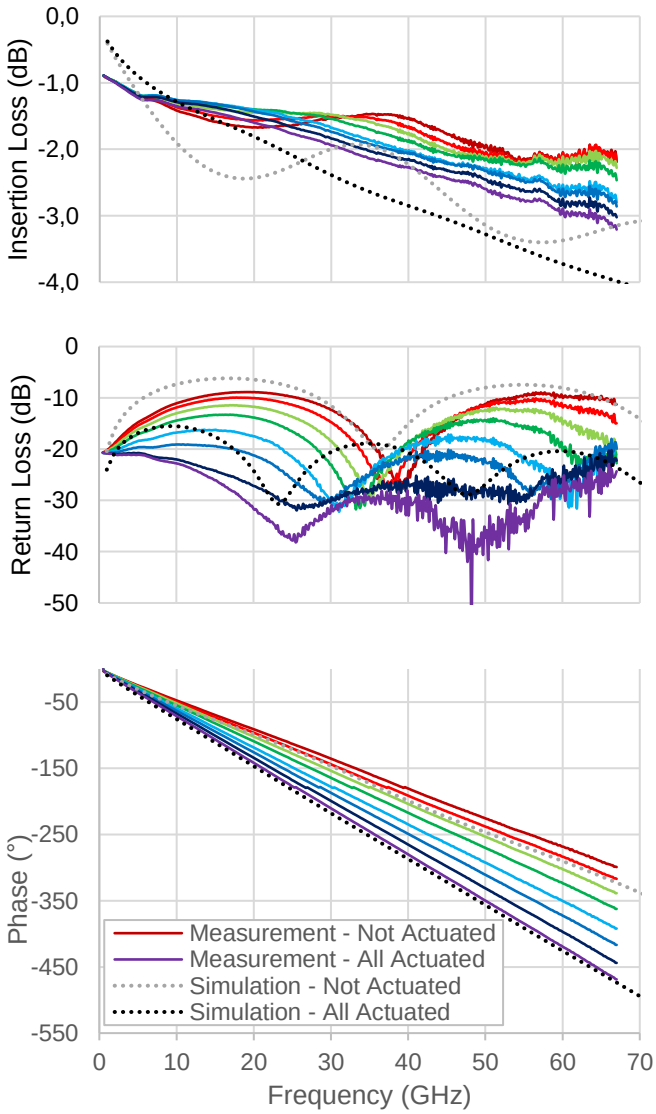


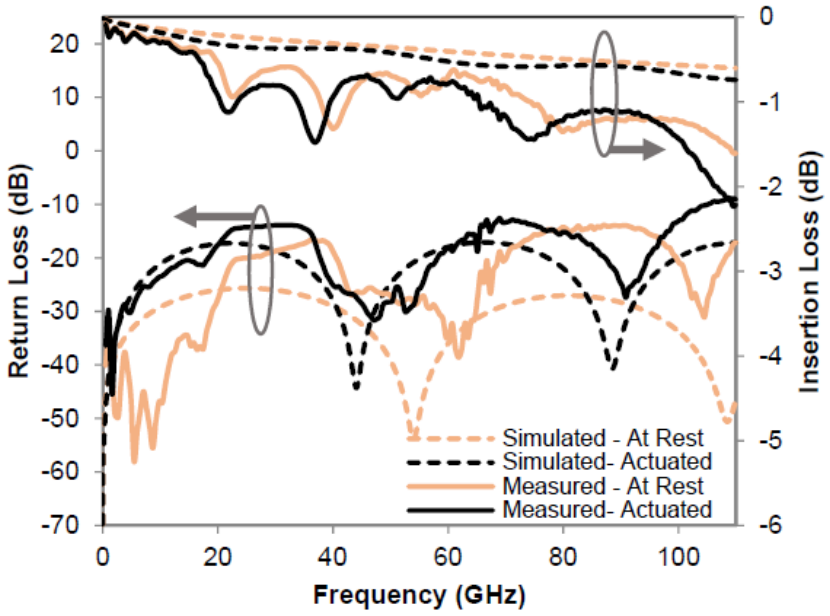
Figure 4-5: Measured and simulated insertion loss, return loss and phase shift of the distributed MEMS phase shift with CEA technology.

Figure 4-5(a), Figure 4-5(b) and Figure 4-5(c) compare the measured and simulated insertion loss, return loss and phase, respectively. The measurements showed maximum insertion loss of 2.9 dB at 60 GHz for 152° of phase shift. The insertion loss has a maximum variation of only 0.85 dB between *off*- and *on*-states. The measured return loss is better than 9.8 dB for all phase states. A good agreement was obtained between measurements and simulations, even if the simulation shows an overestimation of the insertion loss of almost 1 dB.

The FoM which is defined as the ratio between the maximum phase shift and the maximum insertion loss is around 50°/dB at 60 GHz. The simulated FoM is slightly different than measured FoM due to the overestimated insertion loss. Another FoM which is defined as the ratio between the maximum phase shift and the length of the phase shifter is around 110.5°/mm. A better optimization of the commands and phase shifter design could increase these two FoMs without increment in surface area.

4.1.3. AMS phase shifter

This phase shifter was designed by Bruno VERONA [4] and implemented in AMS technology. Bruno measured this phase shifter in 2013 at IMEP-LaHC laboratory from 0 to 100 GHz. Figure 4-6 shows the measured and simulated performances of the AMS phase shifter.



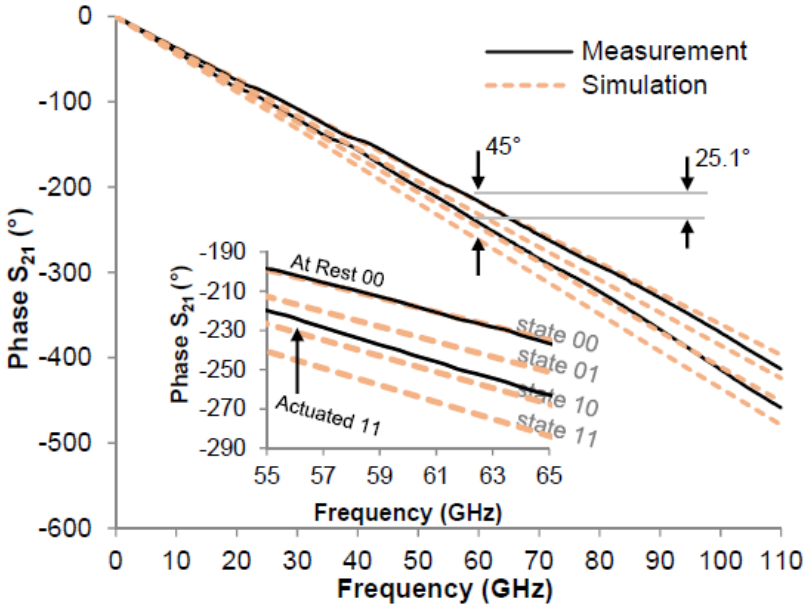


Figure 4-6: Measured and simulated AMS phase shifter. (a) Insertion and return loss and (b) phase.

Figure 4-6(a) presents the measured and simulated return and insertion losses for *off*- and *on*-states, respectively. The measured and simulated return losses are better than 10 dB in the frequency range from 0 to 100 GHz for both states. At 60 GHz, the insertion loss for *off*-state is around 0.7 dB for a 1120-µm long phase shifter. It does not change significantly in *on*-state, leading to a small insertion loss variation. Further, there exists good agreement between simulated and measured values, except for some oscillations in the insertion loss that could be due to de-embedding issues. In this phase shifter the shielding layer start to move at 20 V and gives the higher phase shift of 25° at 60 V which leads to a FoM of approximately 36°/dB. This phase shift is 20° smaller than expected. The most probable cause is the presence of an unknown material above the shielding layer. This materiel can prevent the displacement of the shielding layer, thus, reducing the phase shift. The need for a completely known technology is mandatory for the etching post-process steps.

4.2.IHP phase shifter design 1 measurements

In this section three measurements are presented in detail, i.e. optical and electrical (DC) for geometrical and mechanical observations and RF for design characterization. Before presenting these measurements, we will first refer to the layout of the phase shifter fabricated in the SG25 technology of IHP in Figure 4-7.

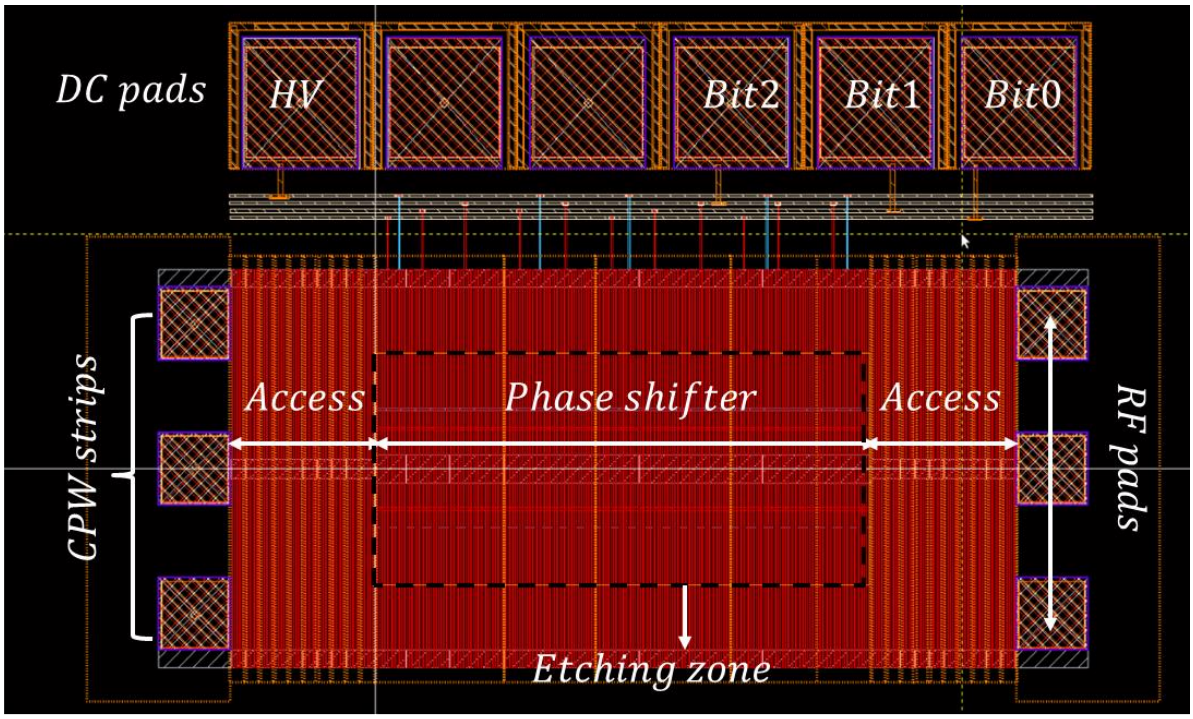


Figure 4-7: IHP phase shifter layout.

As shown in Figure 4-7, the layout has 4 parts: phase shifter (etching zone), access (without etching), RF pads and DC pads. This layout corresponds to a 3-bit phase shifter with expected total phase shift of 157.5°. The phase shifter is 340 µm long. Each access has 100 µm of length. It occupies a surface area of 340 µm × 252 µm excluding RF pads, RF access and DC commands which may vary depending on circuit' design.

In this section, we use the following abbreviations for phase shifters:

- PS1: for 3-bit phase shifter 315° with 3 commands (occupies 680 µm × 252 µm)
- PS2: for 3-bit phase shifter 315° with 4 commands (occupies 700 µm × 252 µm)
- PS3: for 3-bit phase shifter 157.5° with 3 commands (occupies 340 µm × 252 µm)

4.2.1. Optical and electrical characterization

The first set of measurements was performed in IHP platform on July 2015 except white light interferometry. This white light interferometry was performed in Grenoble on March 2016. Also, the RF measurements were re-performed at IMEP-LaHC on October 2016.

4.2.1.1. Optical measurements: laser Doppler velocimetry

First of all, we performed LDV (for laser Doppler velocimetry) measurements to check the placement of the membranes before and after actuation. Figure 4-8 shows the placement of

membranes (the gap between membranes and the signal strip) vs the applied voltage. These measurements were done at IHP platform in Germany.

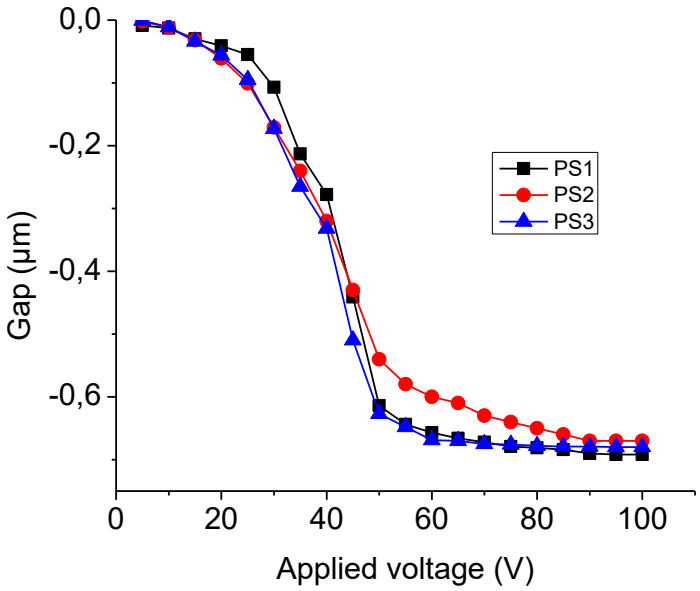


Figure 4-8: Gap variation.

From Figure 4-8, we can see that the membranes start to move at 25 V for the three phase shifters. The maximum displacement is obtained after 60 V for PS1 and PS3 and after 80 V for PS2. From this LDV measurement (for all the phase shifters) we can remark that the gap between membranes and signal strip is 700 nm only, as shown in Figure 4-8 while it was expected to be 900 nm, as specified in the SG25 BEOL description. Two reasons can be brought, (i) the membranes are wearing down at *off*-state, reducing the gap before actuation and/or (ii) the etching is less than expected in depth, letting about 200-300 nm of oxide on top of M2. This last hypothesis is not compatible with a standardized process as at IHP.

Note that these measurements are made at only one point of the device, i.e. in the middle of the membrane above the signal strip with some light reflected by the metallic ribbons of the membrane and some by the layer seen through the interstices of the membrane.

4.2.1.2. Optical measurements: white light interferometry

To understand a little more the LDV results in sub section 4.2.1.1, IHP sent the wafer to IMEP-LaHC on October 2015. And then, a new measurement in white light interferometry was performed the 24th of March 2016. Only two devices were measured: Device 1 was placed in the center of the wafer, Device 2 was placed on the edge of wafer. Table 4-1 presents the measurement results for Device 1.

Table 4-1: White light interferometry for Device 1.

Applied voltage (V)	Gap (µm)
0	10.95
70	10.95
110	11.2
150	11.7

From Table 4-1, we can see that the displacement of the membranes is 0.75 µm after applying a voltage of 150 V (a little bit more than the 0.7-µm value obtained in LDV for a 60 V voltage but this sounds consistent with the hypothesis of a wearing down of the membrane). For 0 V again, the membranes come back to 10.9 µm. This measurement was repeated 10 times from 0 to 100 V without any problem. The device was burnt after the repetition of this measurement 3 times from 0 to 150 V.

Table 4-2 presents the measurement results of the white light interferometry for Device 2.

Table 4-2: White light interferometry for Device 2.

Applied voltage (V)	Gap (µm)
0	10.7
30	10.9
50	11
75	11.15
85	11.32
100	11.8

From Table 4-2, we can see that after 100 V the displacement is 1.1 µm and it is 0.2 µm more than specified by the technology (i.e. 0.9 µm). Figure 4-9 shows a 3-D view and the gaps of Device 2 measured in white light interferometry.

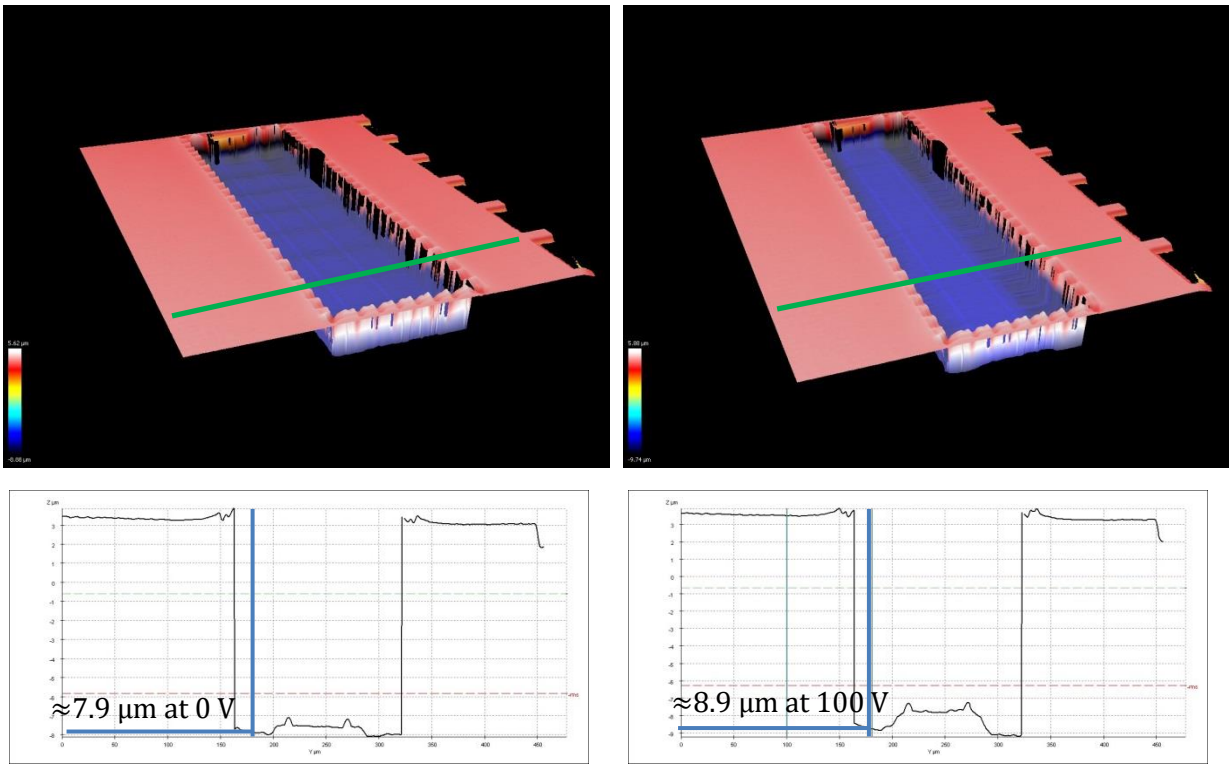


Figure 4-9: (a) 3-D view of Device 2 at 0 V, (b) 3-D view of Device 2 at 100 V, (c) gap at 0 V and (d) gap at 100 V.

The green lines in Figure 4-9 (a) and Figure 4-9 (b) are the cut lines for the measurements presented in Figure 4-9 (c) and Figure 4-9 (d). In those latter, we can note that the difference between displacements at 0 and 100 V is around 1 µm (> 900 nm) so we can confirm that complete etching has been performed, as expected. By comparing the results between Device 1 and Device 2, we can observe an inhomogeneity of etching on the wafer. More precisely, there can be an extra etch in some parts of the wafer. This extra etch cannot be estimated carefully as both effects (wearing down and extra etch) may superpose. Extra etch is not an issue. On the contrary, this guarantees a maximum of capacitance between the signal line and the membrane.

Concerning calibration, in white light interferometry as in LDV, the height absolute values do not make sense. In fact some light is reflected by the metallic membrane while some light, going through the interstices of the membrane, is reflected by the layer below; as a consequence, a mean height is calculated that is not the real position of the membrane. Never-the-less, the 7.9-µm in *off*-state, which has been measured with white light calibration, is not so far than the expected design kit values. On the contrary, difference is valuable, as long as no variation in the laser spot position between *off*- and *on*-states occurs. This is guaranteed in white light interferometry.

In conclusion, by assuming that difference between *off*- and *on*-states make sense, we could conclude to i) an extra etch of at least 200 nm on the edge of the wafer which seems meaningful

considering a total etch of around 9 µm and ii) a slight wearing down of the membrane of about 200 nm in some of the devices even if no actuation is performed. A wearing-up of the membrane ribbons could be enfaced as well. Statistical measurements correlated to the position on wafer should be done to confirm those assumptions. MEB observation could also be a good solution. Meanwhile, capacitance measurements can already help to better analyze the geometry and the mechanical behavior.

4.2.1.1. Electrical measurements: capacitances

Figure 4-10 shows the capacitance variation at 3 GHz. This measurement of capacitances was done at IHP platform in July 2015. Figure 4-10 compares the capacitances of PS1, PS2 and PS3.

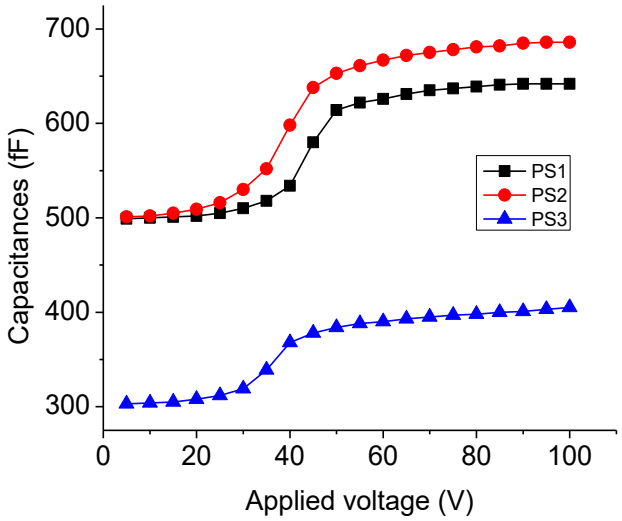


Figure 4-10: Capacitance variation.

From Figure 4-10, we can see that the capacitance at 0 V is almost the same for PS1 and PS2 (500 fF). At 95 V, the capacitance of PS2 is bigger than the capacitance of PS1 (650 fF for PS1 and 680 fF for PS2) because PS2 is 20 µm longer than PS1 which does not have a big effect in *off*-state. As compared to PS1 and PS2, PS3 is smaller. Hence the capacitance of PS3 is around 305 fF at 0 V and 405 fF at 95 V. The capacitance ratio Con/Coff is: 1.3 for PS1, 1.36 for PS2 and 1.33 for PS3.

Theoretically, we should observe a Con/Coff ratio of 2 by considering a 900 nm gap in *off*-state, with fringing effect, but no parasitic effect, as calculated in section 4.4.1.1. In practice, referring to the capacitance measurement a smaller capacitance ratio is observed. Thus, at first, this capacitance measurement can help us to understand the equivalent circuit of the phase shifter, and may be in second, to correlate it to geometrical observations.

4.2.2. RF measurements: S-parameters

The S parameter measurements of the three phase shifters, i.e. one 157.5° and two 315° phase shifters are presented in this section. These measurements were done at IHP platform in July 2015 up to 67 GHz. The measurements are raw measurements without pad or 50-Ω access de-embedding, which may deteriorate the losses but do not influence the phase difference.

4.2.2.1. 157.5° phase shifter/ 3 commands

Figure 4-11(a) shows the return loss (S11) measurement of the 157.5° phase shifter, from DC to 67 GHz. The insertion loss (S21) measurement of 157.5° phase shifter is shown in Figure 4-11 (b). The phase shift is shown in Figure 4-11(c).

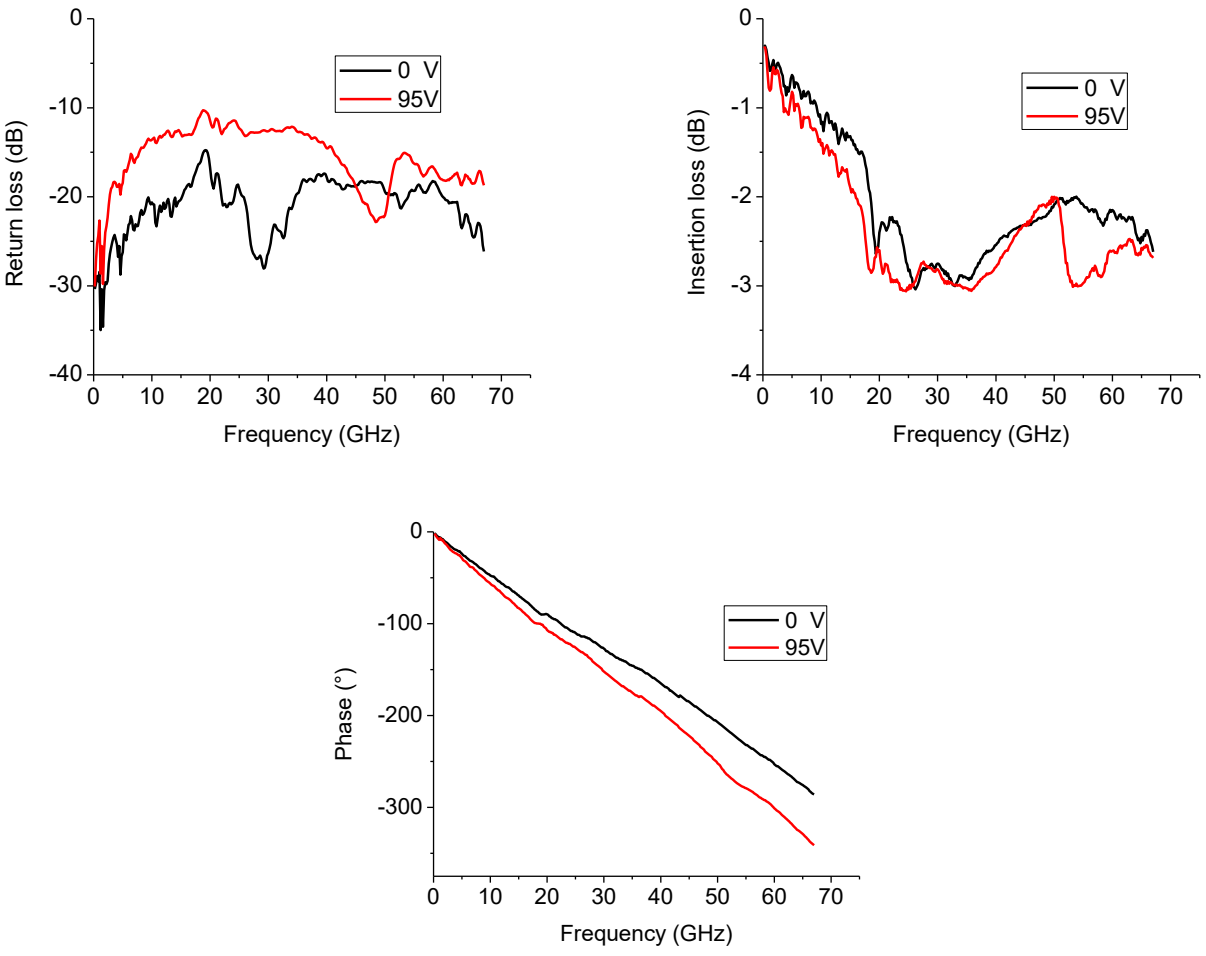


Figure 4-11: Measurement results of the 157.5° phase shifter. (a) Return loss, (b) insertion loss and (c) phase.

As shown in Figure 4-11(a), the return loss is better than 10 dB for *off*- and *on*-states over the whole bandwidth (200 MHz to 67 GHz). The measured insertion loss is 2.2 dB for 0 V and 2.8 dB for 95 V. The value of insertion loss is quite high due to the small thickness of metal M2

(730 nm only). A maximum phase shift of 55° was obtained for this 157.5° phase shifter, leading to ~20°/dB of FoM (no de-embedding). The other FoM defined as the ratio between the maximum phase shift and the length of the phase shifter is around 162°/mm.

4.2.2.2. 315° phase shifter/3 commands

Figure 4-12 (a) and Figure 4-12 (b) give the measured return and insertion losses, respectively, for the 315° phase shifter with 3 commands. The measured phase of this phase shifter is shown in Figure 4-12 (c).

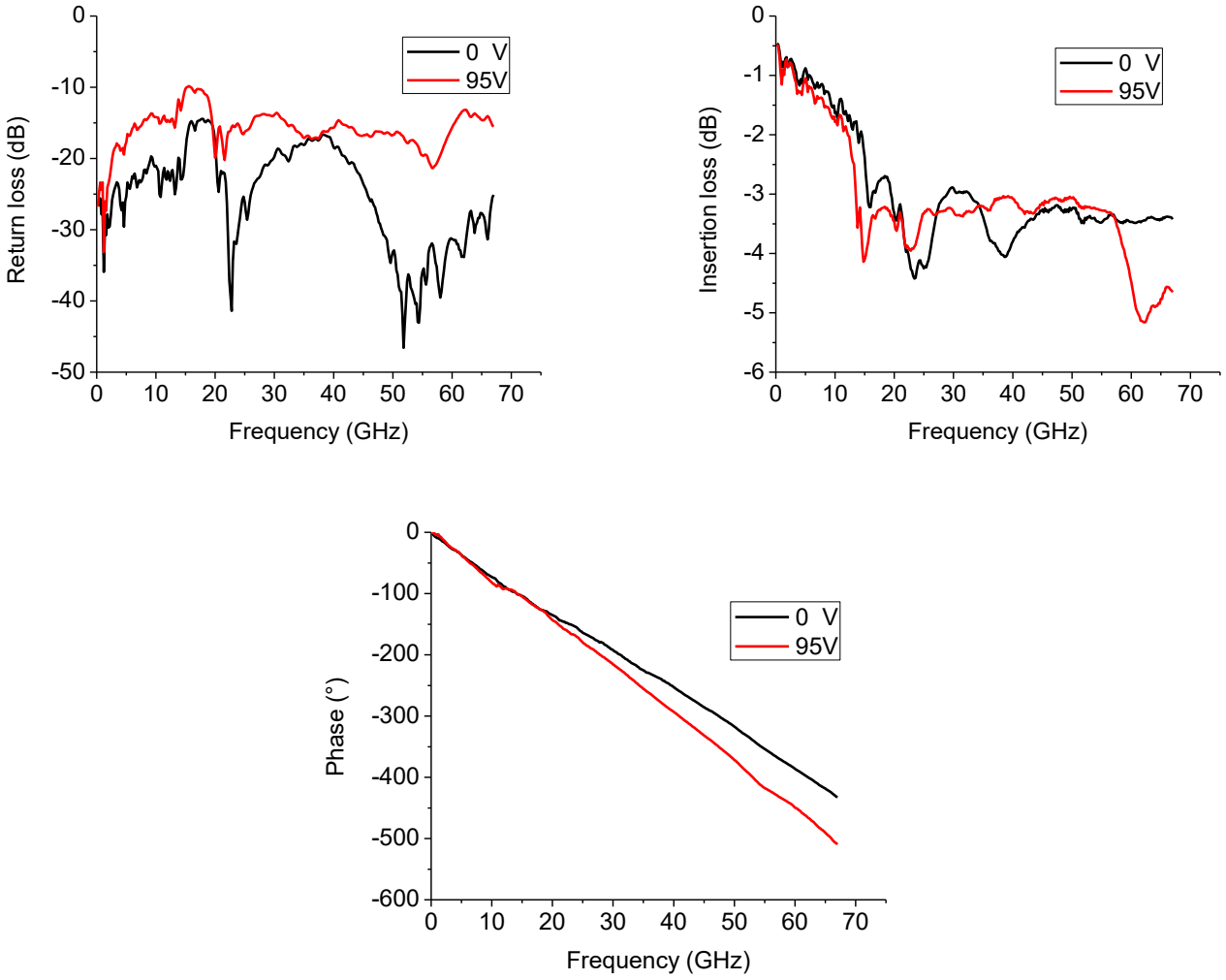


Figure 4-12: Measurement results of the 315° phase shifter with 3 commands. (a) Return loss, (b) insertion loss and (c) phase.

As shown in Figure 4-12 (a) the return loss is better than 10 dB at 0 and 95 V over the whole bandwidth (200 MHz to 67 GHz). For this 315° phase shifter, the insertion loss varies from 3.5 dB at 0 V to 4.4 dB at 95 V, as shown in Figure 4-12 (b). As this phase shifter is twice the length of 157.5° phase shifter, the losses in this phase shifter should be twice of the insertion loss (i.e. 5.6 dB) obtained for the 157.5° phase shifter. Variation is due to standing wave effect

that can be observed on Figure 4-12. The measured phase shift for this phase shifter is around 82° between 0 V and 95 V. The FoMs in this case are equal to ~19°/dB (no de-embedding) and 120°/mm. This phase shifter also showed the same issue of displacements as the 157.5° phase shifter.

4.2.2.3. 315° phase shifter/4 commands

Figure 4-13 presents the measured return loss, insertion loss and phase of the 315° phase shifter with 4 commands from 200 MHz up to 67 GHz.

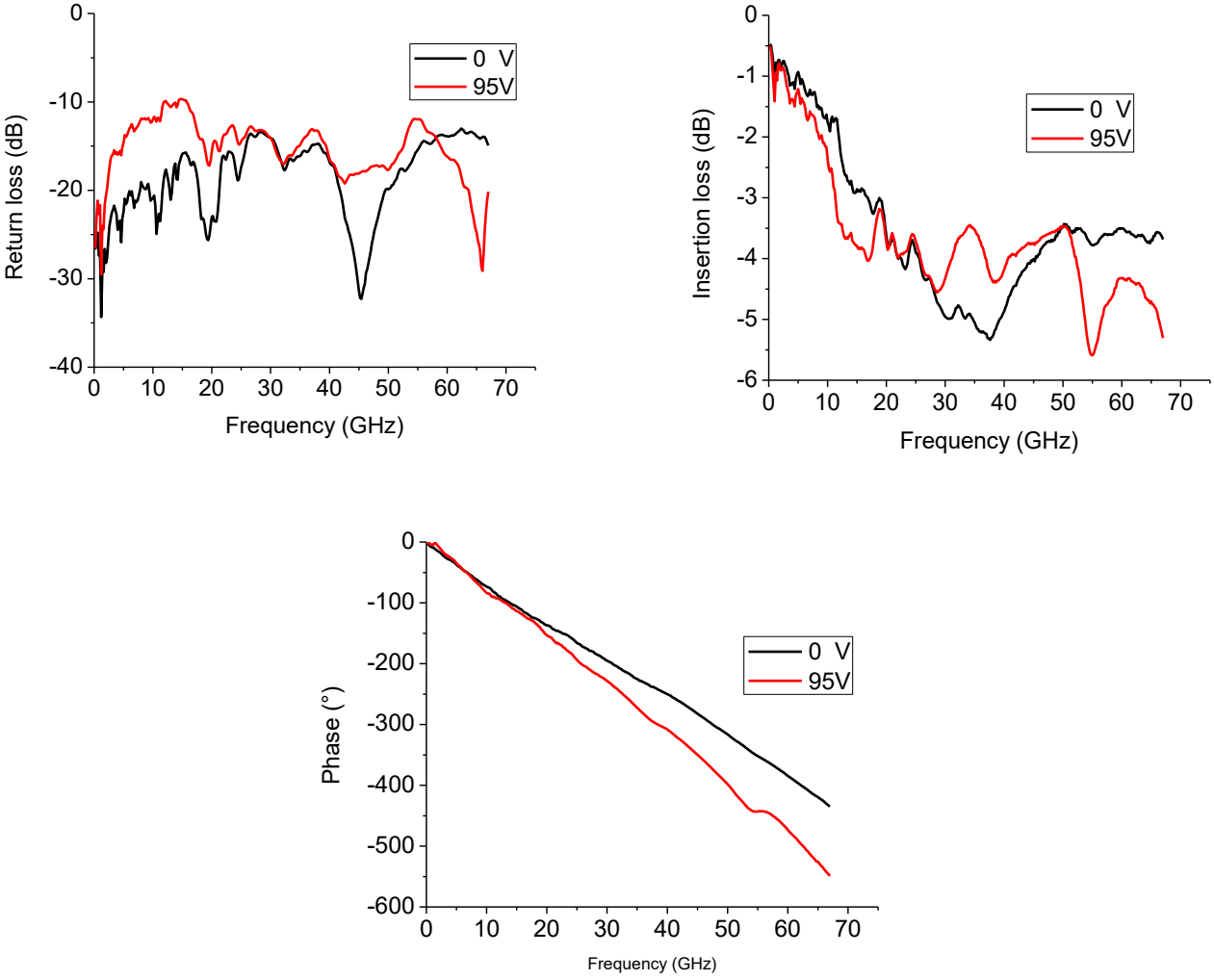


Figure 4-13: Measurement results of 315° phase shifter with 4 commands. (a) Return loss, (b) insertion loss and (c) phase.

As shown in Figure 4-13 (a) the return loss is better than -10 dB at 0 and 95 V over the whole bandwidth (200 MHz to 67 GHz). For this 315° phase shifter with 4 commands, the insertion loss varies from 3.6 dB @ 0 V to 4.5 dB @ 95 V, as shown in Figure 4-13 (b). The measured phase shift for this phase shifter is around 100° between 0 V to 95 V leading to FoMs of ~22°/dB (no de-embedding) and 142°/mm.

4.2.3. Observed limitations

In this section, we present a comparison between measurement and simulation results from 55 to 65 GHz. Figure 4-14 shows the return loss, insertion loss and phase comparison for the 157.5° phase shifter.

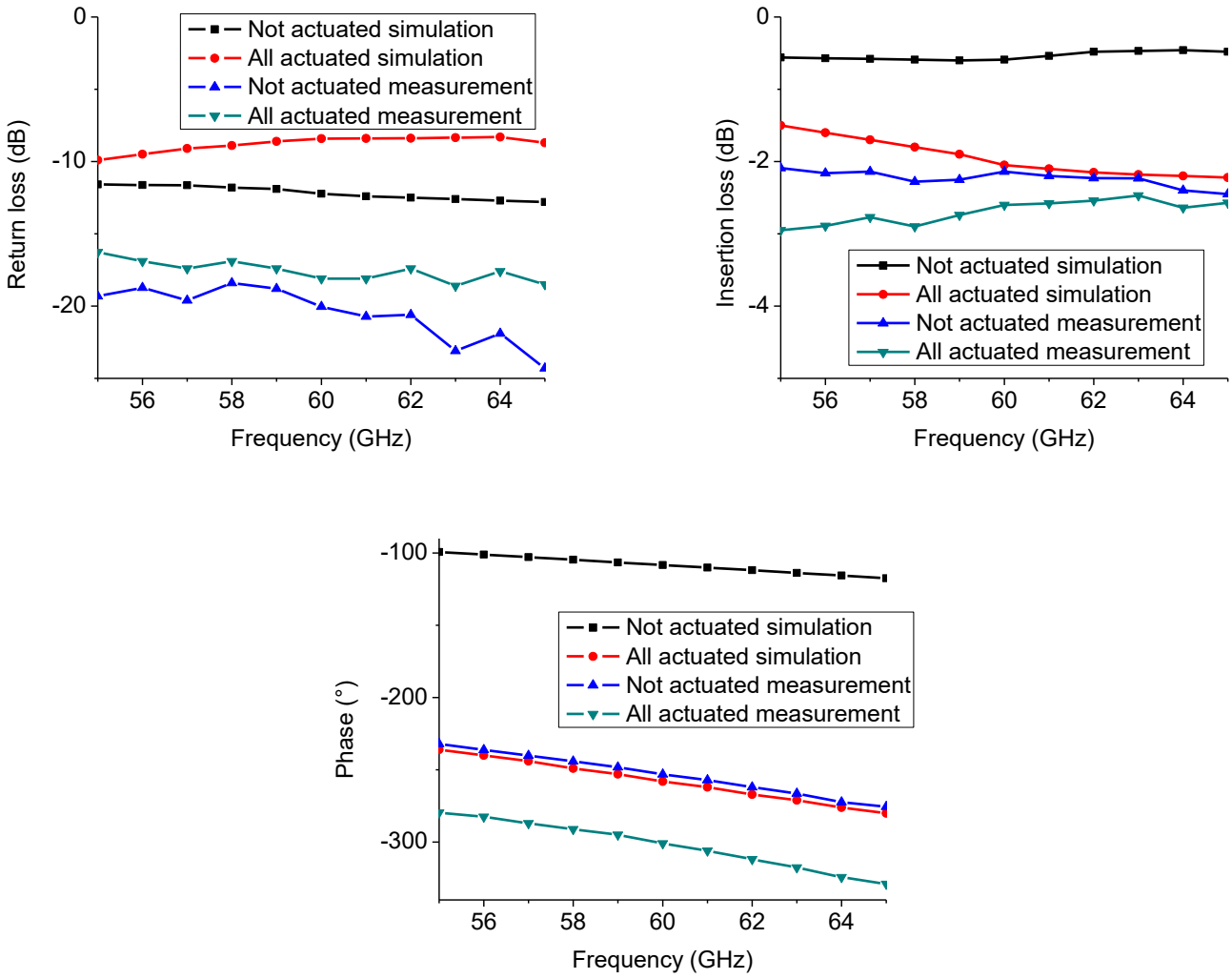


Figure 4-14: Measurement and simulation results of the 157.5° phase shifter. (a) Return loss, (b) insertion loss and (c) phase.

From Figure 4-14, we can remark that the simulation and measurement are not matched. The simulation shows an overestimation of the return loss for both cases *off*- and *on*-states of more than 7 dB in the whole frequency range (55 GHz to 65 GHz). The difference between simulated and measured insertion loss is almost 1.5 dB for *off*- and *on*-states. Also, we can observe in Figure 4-14 (c) that the total phase shift is 155° and 55° for simulation and measurement, respectively. This discrepancy between simulated and measured phase shift can be partly due to a smaller displacement than expected (700 nm instead of 900 nm) as explained in section 4.2.1.2. But this does not sound enough as a reason. Another aspect of this topology

may cause this difference: it could be due to the parasitic effect of the substrate which has not been considered during the simulation. To understand more the substrate effect, we made a calculation of the parasite capacitances in section 4.4.1.

4.3.IHP phase shifter design 2 measurements

Up to now, all the previous sections of chapter 4 considered the measurements of the first design in IHP SG25 technology. The measurements results of the optimized phase shifter of the second design (chapter 3, section 3.4) will be presented the day of my defense, the 15th of December 2016.

4.4.Discussion on the parasitic effect of the substrate

4.4.1. Analytical calculation of capacitances

As presented in Figure 4-7, the phase shifter has 3 parts: phase shifter, access and RF pads. In this section dedicated to the observation of the parasitic effect of the substrate, we calculate all the capacitances that exist for each part of the 157.5°phase shifter in IHP SG25 technology.

4.4.1.1. Equivalent capacitances: phase shifter movable part

Figure 4-15 shows the equivalent capacitances of the movable part of phase shifter. The structure has the same dimensions as those of the TS-CPW presented in chapter 2 ($W = 20\ \mu m, W_g = 12\ \mu m,\ h = 0.9\ \mu m,\ h_s = 2.91\ \mu m, h_1 = 0.9\ \mu m, h_2 = 1.64\ \mu m, l = 340\ \mu m$) . See Figure 4-15 for a reminding of the geometry. The capacitances that exist between the CPW strips and the membranes are shown in Figure 4-15(a) and their expressions are given in eq. (2-12) and (4-2).

$$C_{splate} = \frac{\varepsilon_0 . \varepsilon_r . W . l}{h} \quad \textbf{(4-1)}$$

$$C_{gplate} = \frac{\varepsilon_0 . \varepsilon_r . W_g . l}{h} \quad \textbf{(4-2)}$$

Parasitic capacitances also exist between the CPW strips and the substrate; they are shown in Figure 4-15(b) and their expressions are given in eq. (4-3), (4-4) and (4-5).

$$C_{1plate} = \frac{\varepsilon_0 . \varepsilon_r . W_g . l}{h_s} \quad \textbf{(4-3)}$$

$$C_{2plate} = \frac{\varepsilon_0 . \varepsilon_r . W . l}{h_1} \quad \textbf{(4-4)}$$

$$C_{3plate} = \frac{\varepsilon_0 . \varepsilon_r . W . l}{h_2} \quad \textbf{(4-5)}$$

Also, we add the fringing capacitance to all capacitances. $C_{fringing}$ is represented in red in Figure 4-15(a). Then, the new expressions calculated in eq.(2-12) to eq. (4-5) are now given by eq. (4-6) to eq. (4-10).

$$C_s = C_{splate} + 2.C_{sfringing} \quad \textbf{(4-6)}$$

$$C_g = C_{gplate} + 2.C_{gfringing} \quad \textbf{(4-7)}$$

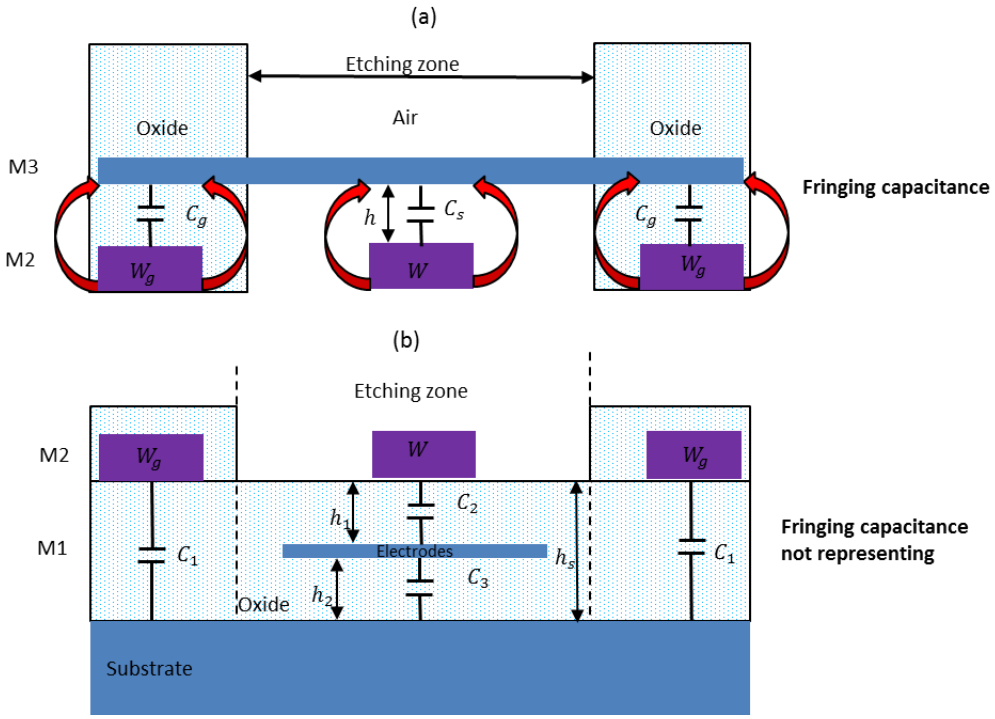
$$C_1 = C_{1plate} + 2.C_{1fringing} \quad \textbf{(4-8)}$$

$$C_2 = C_{2plate} + 2.C_{2fringing} \quad \textbf{(4-9)}$$

$$C_3 = C_{3plate} + 2.C_{3fringing} \quad \textbf{(4-10)}$$

The calculation of the fringing capacitance is given into details in [51]. Only the angle capacitance (see [51]) has been considered here and roughly calculated in an analytical way. The total capacitance is given by eq.(4-11):

$$C_{PS} = \frac{2C_sC_g}{C_s + 2C_g} + \frac{2C_1C_2C_3}{C_2C_3 + 2C_1C_2 + 2C_1C_3} \quad \textbf{(4-11)}$$



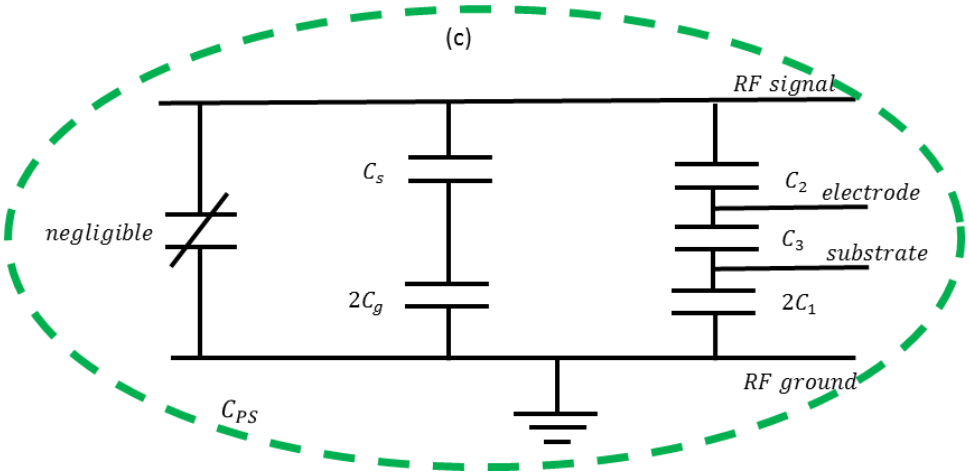


Figure 4-15: Equivalent capacitances for phase shifter. (a) Between CPW strips and membranes, (b) between CPW strips and substrate and (c) equivalent phase shifter capacitances.

As C_s is a capacitance that varies with the applied voltage between membrane and electrode, it is more appropriate to refer to it as C_{s-off} in the *off*-state and as C_{s-on} in the *on*-state. All other capacitances are fixed ones. C_g,C_1, C_2, and $C_3$are equal to 182 fF, 70 fF, 288 fF and 536 fF, respectively.

In *off*-state, C_{s-off} is equal to 75 fF. Using eq.(4-11), the equivalent capacitance C_{PSoff} (Figure 4-15(c)) is equal to 142 fF.

For *on*-state, only the capacitance of the movable part of the phase shifter is changed after etching and applying voltage, that is to say the capacitance C_{s_on} considering the parallel plate *on*-signal capacitance and a negligible *on*-signal fringing capacitance. C_{s_on} is extremely high; in series with $2C_g$, then only $2C_g$ has to be considered. Using eq. (4-12), the equivalent capacitance C_{PSon} (Figure 4-15(c)) is equal to 444 fF.

$$C_{PS} = 2C_g + \frac{2C_1C_2C_3}{C_2C_3 + 2C_1C_2 + 2C_1C_3} \quad \textbf{(4-12)}$$

4.4.1.2. Equivalent capacitances: access

Figure 4-16 shows the equivalent capacitances of the access part of the phase shifter. This access consists in an S-CPW transmission line without etching. Its dimensions are $W = 10\ \mu m, W_g = 12\ \mu m,\ h = 0.9\ \mu m,\ h_s = 2.91\ \mu m, l_{access} = 100\ \mu m$. The capacitances that exist between the CPW strips and the membranes are shown in Figure 4-16 (a). Also, the parasitic capacitances that exist between the CPW strips and the substrate are shown in Figure 4-16(b). The equivalent capacitance C_{access} (Figure 4-16(c)) of one access is around 45 fF (refers eq. (4-13)) taking into account the fringing effect. Then for both access (100 µm long on each sides) the equivalent capacitance is double (90 fF).

$$C_{access} = \frac{2C_sC_g}{C_s + 2C_g} + \frac{2C_1C_2}{2C_1 + C_2} \quad \textbf{(4-13)}$$

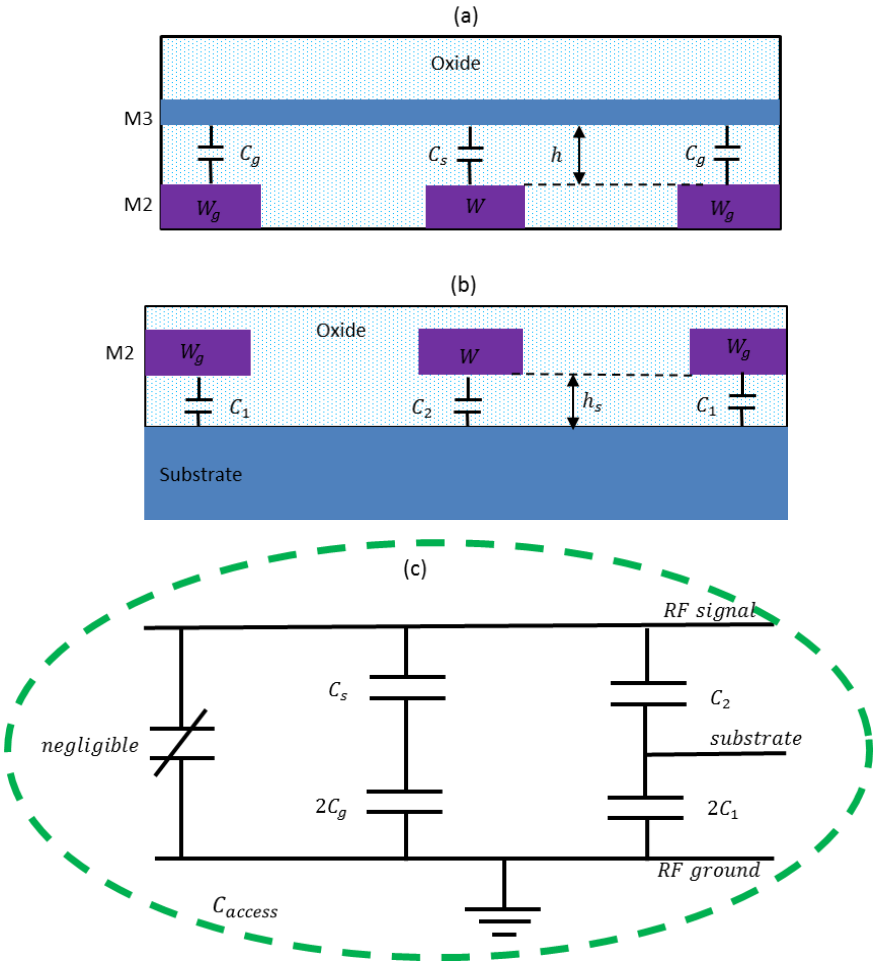


Figure 4-16: Equivalent capacitances for access. (a) Between CPW strips and membranes, (b) between CPW strips and substrate and (c) equivalent access capacitances.

4.4.1.3. Equivalent capacitances: RF pads

Figure 4-17 shows the equivalent capacitances of the RF pad part of the phase shifter. The dimensions of one pad are $W_{pad} = 60\ \mu m$, $h_s = 2.91\ \mu m, l_{pad} = 50\ \mu m$. The equivalent capacitance due to pad, C_{pad}, on one side of the circuit, is around 32 fF taking into account the fringing effect. Then, for both sides the equivalent capacitance is double (64 fF).

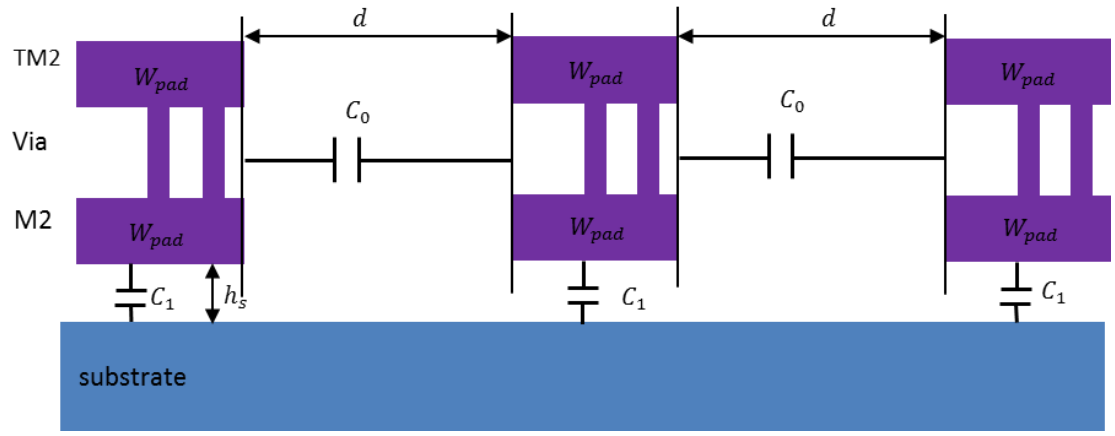


Figure 4-17: Equivalent capacitances for RF pads.

4.4.1.4. Discussion and final calculation

Figure 4-18 illustrates the equivalent capacitance for the fabricated phase shifter including the access and the RF pads for *off*- or *on*-state.

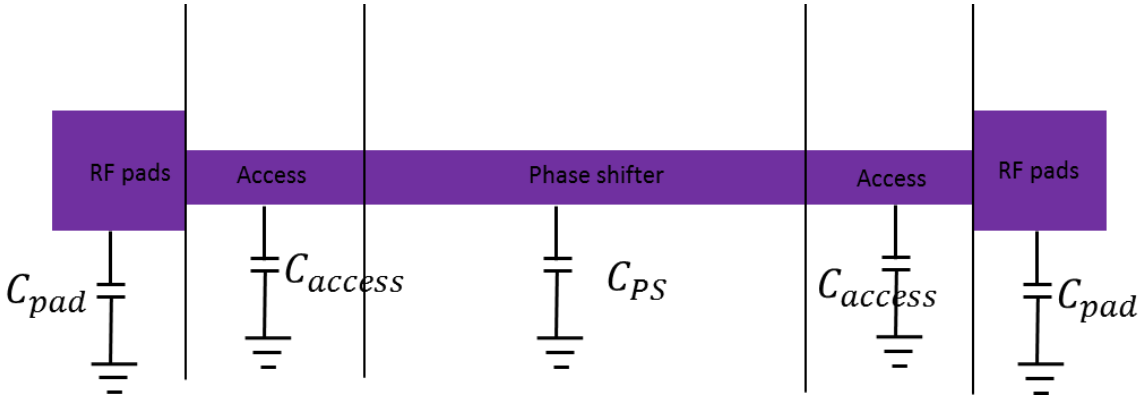


Figure 4-18: Equivalent capacitance.

Finally, the total capacitance of the phase shifter for *off*-state, C_{off}, is equal to the addition of $C_{PSoff} + 2.C_{access} + 2.C_{pad} = 142 + 90 + 64 = 296\,fF$. This value of calculated C_{off} is matching quite well the measurement value of 305 fF for *off*-state. For *on*-state, the equivalent capacitance is $C_{on} = C_{PSon} + 2.C_{access} + 2.C_{pad} = 444 + 90 + 64 = 598\,fF$. This calculated C_{on} is not matched with the measurement (405 fF). This mismatch between calculated and measured C_{on} is due to the fact that we estimate in calculation C_{s_on} higher than the actual existing capacitance in the phase shifter. Also this mismatch can be due to the fact that the capacitance between CPW strips and substrate has not been well estimated.

4.4.2. Solution to improve Con/Coff

The solution to reduce the parasitic capacitance due to the substrate is to place the membranes under the CPW strips in order to design the TS-CPW. In this proposition, we put the membranes in Metal 2, the CPW in Metal 3 and Top Metal 1 (TM1). Also, we place two high

electrodes voltage in TM1, 15 µm far from the signal strip ($d_e = 15\ \mu m$, on Figure 4-19), leading to a minimum applied voltage of 68 V. Figure 4-19 shows the new proposed topology of TS-CPW based on distributed MEMS in IHP SG25 technology.

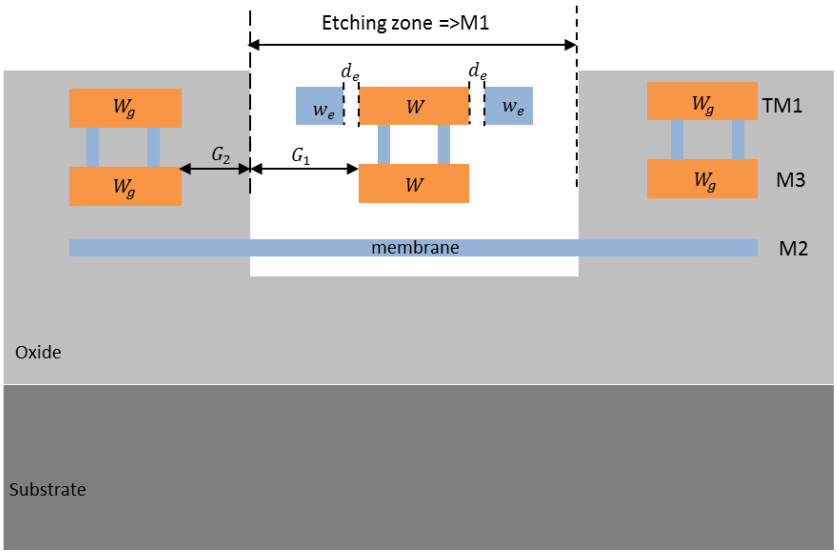


Figure 4-19: New topology of TS-CPW used for phase shifting in IHP SG25 BiCMOS technology.

In this structure, the signal strip and the electrodes are fixed by pillars of oxide every 50 ribbons of the membrane. The dimensions of the TS-CPW are $W = 10\ \mu m, W_g = 24\ \mu m,\ w_e = 15\ \mu m, h = 0.9\ \mu m, S = 60\ \mu m$. The presence of the ribbons below the CPW strips prevents the electricals field from passing to the substrate. This is a major point, and an undeniable advantage. Hence the parasitic capacitances caused by the substrate will be negligible. For this structure $C_{off} = (C_s .2C_g)/(C_s + 2C_g)$ and $C_{on} = 2. C_g$.

4.5.Comparison with state-of-the art

In Table 4-3, the performance of our MEMS-based phase shifter in IHP SG25 technology has been compared with state-of-the art of millimeter-wave passive phase shifters.

Table 4-3: State of-the art comparison at mm-wave frequencies.

Ref	Tuning element	Frequency (GHz)	Resolution	Area (mm^2)	IL (dB)	FoM1 (°/dB)	FoM2 °/Length (°/mm)	FoM3 °/Area (°/mm^2)
CMOS 90 nm/[6]	Varactor	60	Analog	0.075	6.25(±1.8)	11	-	916
CMOS 65 nm/[7]	Varactor	60	3-bit	0.2	9.4(±3.1)	12.5	-	587
SiGe 0.13 µm/[8]	Transistor	77	4-bit	0.135	19(±3.7)	15	-	2111
Quartz/[9]	MEMS	60	2-bit	4	3	90	-	67.5
Quartz/[10]	MEMS	65	4-bit	11.85	2.8(±0.8)	93	-	21.9
Glass/[44]	MEMS	78	3-bit	9.6	3.2	99	-	63
CMOS/[42]	MEMS	55-65	-	1.04	2.2(±1)	65.4	-	144
Glass/PTA[1]	MEMS	60	3-bit	0.35	3.5	52	58	93
HR Si /CEA[11]	MEMS	60	3-bit	0.47	2.9	50	111	107
0.35 µmAMS/[4]	MEMS	60	2-bit	0.58	0.7(±0.1)	36	94	43.5
SiGe	MEMS	60	3-bit PS2	0.176	4.5	19	143	568
0.25 µm/This	MEMS	60	3-bit PS1	0.171	4.4	22	121	480
work	MEMS	60	3-bit PS3	0.086	2.8	20	161	640

First, let us notice that the miniaturized phase shifter based on TS-CPW, and among them the IHP PS1, PS2 and PS3, present the lowest occupied area as compared to other MEMS based technologies, leading to a higher FoM3 (°/mm^2). However PS1, PS2 and PS3 showed higher insertion loss than their other MEMS counterpart, distributed or not. This can be improved by using the thick metal level in SG25 instead of M3, as proposed in the new solution to enhance Con/Coff. Then, the FoM1 will be improved. Never-the-less, even if PS1, PS2 and PS3 results were not de-embedded they still show much better insertion loss than varactor or transistor based phase shifters. So, if both FoM1 and area are taken into account, our device is a very good trade-off. Also our phase shifters show a 3-bit resolution with 3 commands, which had never been done before with previous works at IMEP-LaHC.

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Conclusion

The present thesis concerned the development of phase shifters based on Tunable Slow-wave CoPlanar Waveguides (TS-CPW) on MEMS technology with post-CMOS process for mm-wave frequencies. The objective was to answer new challenges for integrated circuit design, such as mm-wave front-end transceivers, for which a phased array can be required, thus needing the development of tunable phase shifters as presented in chapter 1. Thanks to the slow–wave effect, the TS-CPW exhibits a high miniaturization and high quality factor, thus leading to high electrical performance along with small foot-print. TS-CPW has been employed in this thesis work for designing a phase shifter with distributed MEMS in IHP 0.25 µm BiCMOS technology, IHP in Germany.

In chapter 2, an overview about RF-MEMS was presented with two types of switches (ohmic and capacitive) and their electrostatic actuator. Various types of failures due to the electrostatic force are also exposed. Also, before proceeding to TS-CPW design, the characteristics of the S-CPW on a 0.25 µm BiCMOS technology were studied. These characteristics gave us insight to choose the first design elements, as metal layer for TS-CPW strips or electrodes or movable membrane. The design topology of TS-CPW was defined taking into account the fabrication priorities. Also, the structure of the TS-CPW was simulated in HFSS in order to extract its electrical characteristics and optimized. These simulated and optimized TS-CPW structures have been utilized to design the phase shifters presented in the next chapter.

In chapter 3, a detailed design methodology to implement a digital phase shifter based on TS-CPW was presented. First, how to use a TS-CPW as a 1-bit phase shifter was explained after the presentation of previous designs of phase shifter carried out at IMEP-LaHC. Next, thanks to the movable membrane of the TS-CPW, ribbons are combined in groups and segments in order to design an N-bit phase shifter with N-commands. Then, the design methodology was proposed and used to implement at 60 GHz, one 157.5° and two 315° phase shifters with 3 commands in MATLAB. The three phase shifters were fabricated and received by the end of July 2015. Their simulated performance in HFSS clearly showed a problem in the MATLAB design methodology for the intermediate states of phase shift. This issue was then resolved by adding a transition for successive *off*- and *on*- states which was not taken into account before. Then, an optimized design for 157.5° phase shifter based on distributed MEMS with 3 commands was proposed with a good agreement between MATLAB and HFSS simulation. This optimized phase shifter was sent to fabrication on October 2015 and the measurement will be presented the day of my defense.

In chapter 4, the set of measurements for the phase shifters early designed in chapter 3 has been presented. Optical measurement (laser Doppler velocimetry and white light interferometry) of phase shifters showed that we need around 100 V of applied voltage to move the membrane. They enabled us to make some assumptions concerning the mechanical aspects of the membranes and the etching process. The electrical measurements showed the capacitance variation between *off*- and *on*- states. The capacitance ratio (Con/Coff) for the three measured phase shifters was 1.3. Also, RF measurements were performed in order to determine phase shift for each states and figures-of-merit (FoM). Thanks to the miniaturization of the TS-CPW caused by the slow wave effect, the FoM defined as the ratio between the maximum phase shift and the area of phase shifter is very high as compared to the other MEMS phase shifters existing in literature. This work demonstrates that a miniaturized phase shifter based on slow-wave CPW and MEMS may occupy a surface as low as 0.086 mm^2, with 2.8 dB of insertion loss, resulting in 21.5°/dB·and 639°/mm^2, which is the best FoM in terms of °/Area reported in the literature for MEMS-based phase shifter, to our knowledge.

However, the phase shifter design based on a new topology of TS-CPW, recently developed in this thesis, has several points to be improved among which:

- A lack of linearity in phase states. The second design of phase shifter up-coming in October 2016 in the 0.25 µm BiCMOS technology at the working frequency of 60 GHz should confirm the solving of this issue with good linearity performances.
- Insertion losses due to the thin metal thickness for the CPW strips. The third design proposed in chapter 4 should enable to overcome this issue.
- Substrate parasitic effects that decrease the Con/Coff ratio and also bring much loss. The third design proposed in chapter 4 should enable to overcome this issue.

As a short term prospective, this phase shifter can be also re-optimized in order to build a Voltage Controlled Oscillator (VCO) with phase shifter as resonator.

The long-term prospects will concern integrating the proposed phase shifter in a millimeter-wave beam-steering system. Finally, the demonstrations should be carried out at frequencies higher than 60 GHz in order to explore the potentialities of this topology to address millimeter-wave imaging systems above 100 GHz.

Publications

During PhD:

- **Victoria Nasserddine**, Gustavo Rehder, Florence Podevin, Bruno Reig, Vincent Puyal Cederic Dehos, Philippe Ferrari, "Déphaseur en technologie MEMS pour application en bande millimétrique", JNM Bordeaux 2015.

- Marcus Pelegrini, Florence Podevin, Gustavo Rehder, **Victoria Nasserddine**, Thu Trang Vo, Philippe Ferrari, "Déphaseur accordables à 60GHz basés sur des lignes à ondes lentes à MEMS distribués", JNM Bordeaux 2015.

- **Victoria Nasserddine**, Gustavo Rehder, Florence Podevin, Bruno Reig, Vincent Puyal, Cederic Dehos, Philippe Ferrari, "Déphaseur à base de MEMS pour application en bande millimétrique", JDR Lyon 2015.

Before PhD:

- Alejandro Niembro-Martín, **Victoria Nasserddine**, Emmanuel Pistono, Hamza Issa, Anne-Laure Franc, Tan-Phu Vuong, Philippe Ferrari, "Slow Wave Substrate Waveguide," IEEE Trans. Microw. Theory Tech., vol. 68, pp. 1625 - 1633, 2014.

Resumé

L'objectif de ces travaux de recherche est la conception en technologie intégrée d'une nouvelle topologie de ligne de transmission accordable afin de réaliser des déphaseurs en bande millimétrique. Cette topologie nommée TS-CPW (pour « Tunable Slow wave CoPlanar Waveguide ») utilise d'une part le phénomène d'ondes lentes qui permet de miniaturiser longitudinalement la ligne de transmission et offre un facteur de qualité plus élevé qu'en technologie microruban intégrée, et d'autre part une approche de type MEMS (Micro Electro Mechanical system) afin obtenir l'accordabilité de la ligne avec une figure de mérite élevée comparativement à une approche de type varactor. Dans un premier temps, la topologie et la conception d'une ligne TS-CPW basée sur des simulations électromagnétiques sont présentées en technologie BiCMOS. Dans un second temps, toujours sur la base de TS-CPWs, des déphaseurs présentant 3-bit de résolution, avec différentes valeurs de déphasage total (de 157.5° et 315°), ont été développés à une fréquence de fonctionnement égale à 60 GHz. Les TS-CPWs et les déphaseurs ont été réalisés avec la technologie BiCMOS 0.25 µm de l'institut IHP en Allemagne, puis mesurés à l'aide d'un analyseur de réseau à IHP et à l'IMEP-LaHc.

Mots-clés : Lignes de transmission S-CPW, ondes lentes, lignes accordables TS-CPW, déphaseurs, figure de mérite, MEMS, bande millimétrique, technologie 0.25 µm BiCMOS.

Abstract

This work focuses on the design of millimeter-wave phase shifters based on a new topology of tunable transmission lines named Tunable Slow wave CoPlanar Waveguide (TS-CPW). TS-CPW uses, on one side, the slow wave phenomenon in order to miniaturize longitudinally the transmission line and to show a better quality factor than its integrated microstrip transmission line counterpart and, on the other side, the MEMS approach to achieve tunability of the transmission line with a good figure-of-merit. First, the topology, the design and the electromagnetic simulations of the TS-CPW based on MEMS (Micro Electro Mechanical system) are presented in a BiCMOS technology. Next, phase shifters with 3-bit of resolution based on TS-CPWs are developed at 60 GHz with two different values of total phase shift (157.5° and 315°). These TS-CPWs and phase shifters were fabricated in IHP's 0.25 µm BiCMOS technology and measured on the vector network analyzers of IHP and IMEP-LaHC.

Key words: Transmission line S-CPW, slow wave, tunable transmission line TS-CPW, phase shifters, figure-of-merit, MEMS, millimeter wave band, 0.25 µm BiCMOS technology.