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THÈSE

présentée à

L'UNIVERSITÉ DE BORDEAUX

Ecole doctorale des Sciences Physique et de l'Ingénieur

Par **Nassim BOUASSIDA**

POUR OBTENIR LE GRADE DE

DOCTEUR

SPÉCIALITÉ : ÉLECTRONIQUE

**DESIGN OF A FULL SOFTWARE TRANSMITTER
BASED ON WALSH SEQUENCES**

Soutenue le 6 Décembre 2016

Devant la commission d'examen formée de

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*“If you can not explain it simply,
you do not understand it well enough”*

Albert Einstein

DESIGN OF A FULL SOFTWARE TRANSMITTER BASED ON WALSH SEQUENCES

Abstract: The use of electromagnetic waves, as a medium for transmitting information between the mobile terminals, has quickly lead to a congestion of the frequency spectrum. To improve the data traffic flow between users, the authorities regulate the access to the frequency bands by imposing stringent standards to the mobile telecommunication. Thus, and in order to increase their data exchange capabilities, the next generations of mobile terminals have to dynamically use the spectral resources. These constraints affect the design of mobile transceivers. They must transmit high data rates by using multiple carriers and various modulation schemes, while consuming as less energy as possible, in order to save their battery life. The Walsh transmitter tries to answer these challenges.

Keywords: Software Radio, Future Standard, Concurrent Transmission, Walsh Sequences, Digital-to-Analog Conversion

CONCEPTION D'UN ÉMETTEUR RADIO-LOGICIELLE A BASE DE SÉQUENCES DE WALSH

Résumé: L'utilisation des ondes électromagnétiques, en tant que moyen de transmission d'informations entre les terminaux mobiles, a rapidement conduit à une congestion du spectre fréquentiel. Pour améliorer le flux de données entre utilisateurs, les autorités réglementent l'accès aux bandes de fréquences en imposant des normes strictes aux télécommunications mobiles. Ainsi, et afin d'accroître leurs capacités d'échange de données, les prochaines générations de terminaux mobiles doivent utiliser dynamiquement les ressources spectrales. Ces contraintes affectent la conception des émetteurs-récepteurs mobiles. Ils doivent transmettre des débits de données élevés en utilisant plusieurs porteuses ayant différentes modulations, tout en consommant le moins d'énergie possible, afin d'économiser l'autonomie de leurs batteries. L'émetteur Walsh tente de répondre à ces défis

Mots-clés: Radio-Logicielle, Futur Standards, Emission Concurrente, Séquences de Walsh, Conversion Numérique/Analogique

RÉSUMÉ

L'utilisation des ondes électromagnétiques comme média de transmission d'information entre les terminaux mobiles ont rapidement mené à une congestion du spectre fréquentiel. Ainsi afin d'améliorer le flux de données entre les usagers, les autorités régulent l'accès aux ressources spectrales en imposant en permanence de nouveaux standards qui évoluent au rythme d'une demande incessante. De ce fait, les prochaines générations de terminaux mobiles devront utiliser dynamiquement ces ressources afin d'améliorer leurs capacités à échanger d'importants volumes de données relativement à de nouveaux services que les usagers veulent utiliser dans des situations extrêmes telles que lorsqu'ils se déplacent à grande vitesse.

L'ensemble de ces contraintes affectent le design des terminaux mobiles. Ils doivent transmettre d'important flux de données en utilisant plusieurs fréquences porteuses ayant différentes modulations tout en consommant le moins d'énergie possible pour assumer une autonomie raisonnable de leurs batteries.

Le chapitre 1 présente donc l'architecture classique de l'émetteur radiofréquence classique tout en exposant ses limites à la résolution de ces contraintes. Pour relever ces challenges, un état de l'art expose les évolutions de cette architecture vers des solutions plus numériques telles qu'elles le sont préconisée le principe de radio-logicielle. En effet dans la littérature il existe une multitude d'articles traitant des émetteurs radiofréquence qu'il est possible de regrouper en quatre catégories. L'objectif commun est de déplacer la limite entre le domaine en bande de bande (BB) et le domaine des radiofréquences de façon à réduire le front-end analogique (FEA)

et à rapprocher l'antenne au plus près du noyau numérique. Ainsi les émetteurs gagnent en flexibilité, en bande passante (BP) et en efficacité. On distingue donc :

- Les émetteurs reconfigurables dont le FEA est reconfigurable grâce à des commandes numériques. Ils sont basés sur une conversion numérique/analogique (N/A) en BB ou en fréquence intermédiaire (FI). La transposition aux hautes fréquences se fait dans le domaine analogique et elle est réalisée par différents FEA selon la BP ciblée. Ce type d'émetteur est donc capable d'adresser plusieurs standards de communication mais, la BP du canal reste limitée et la surface de silicium nécessaire reste importante.
- Les émetteurs à modulation digitale directe essaient de fusionner le DAC et le mixer. Ils utilisent dans la plupart des cas des modulateurs numérique large bande de type sigma-delta pour remplacer la dynamique importante des circuits analogiques par des circuits numériques rapides. Ainsi de par l'augmentation du nombre de commandes numériques ils sont plus flexibles et offrent une solution qui intègre également l'amplificateur de puissance (PA). Pourtant leurs performances (consommation énergétique importante et la BP limitée) ne permettent pas d'adresser les futurs standards
- Les émetteurs numériques sont des solutions implémentées sur FPGA qui permettent d'éliminer entièrement le FEA. Mais leurs BP sont limitées et ils sont assez rigides car la transposition se fait à une fréquence dépendante de la fréquence de BB ou de la FI. Ils sont donc inadéquats pour réaliser de l'émission concurrente.
- Les émetteurs basés sur des convertisseurs N/A radiofréquence offrent la possibilité de convertir des signaux large bande ayant à la fois différentes fréquences porteuses et différentes modulations tout en réduisant au maximum le FEA. Cette solution est la plus élégante mais malheureusement elle reste énergivore en présentant une efficacité de conversion de l'ordre de quelques pJ/bit.

Cette dernière solution ne permet donc toujours pas d'intégrer un émetteur radio-logiciel intégral dans un terminal mobile qui se doit : d'être une solution bon marché (pour adresser le marché de masse), d'avoir une faible consommation d'énergie (pour une durée de vie raisonnable de la batterie) et d'adresser une large BP (pour permettre d'importants flux de données).

Le chapitre 2 propose une nouvelle approche pour encoder le signal à transmettre à partir de son spectre fréquentiel. Elle est basée sur la théorie de la série de Walsh qui est la décomposition du signal dans une base de signaux carrés. Le processus de la conversion de données utilise le contenu spectral de ces signaux carrés pour en pondérer et sommer les harmoniques. La reconstruction du signal est réalisée grâce à l'émetteur de Walsh qui consiste en un synthétiseur des séquences de Walsh et un convertisseur numérique/analogique. Le dimensionnement du système est alors défini à l'aide de simulations Matlab pour permettre la synthèse de signaux à émission concurrente. Ainsi, en utilisant 64 séquences de Walsh pondérées par 64 coefficients de Walsh codés sur 6 bits, le système permet de synthétiser des signaux composés de plusieurs porteuses allant jusqu'à 4GHz et ayant des modulations différentes (jusqu'à 64-QAM) sur 100MHz de bande avec un SQNR de 40dB et des EVM <1%. L'approche de Walsh permet donc de générer numériquement n'importe quel signal à partir de signaux carrés, ce qui constitue un atout majeur pour proposer une architecture émettrice quasiment digitale et à faible consommation d'énergie.

Le chapitre 3 décrit le design de l'émetteur de Walsh en technologie CMOS 28 FDSOI de STMicroelectronics. Le design de chaque bloc est détaillé en utilisant une approche top/down depuis la topologie jusqu'au niveau transistor. L'émetteur de Walsh est constitué de 3 blocs : le synthétiseur de séquences de Walsh, le DAC et l'interface de conversion des coefficients de Walsh. Pour chacun des blocs et des sous-blocs, le comportement est vérifié à l'aide de simulations le plus souvent de type transitoire sous Cadence spectre RF.

Le synthétiseur de séquences de Walsh permet de générer les 64 séquences de Walsh à partir d'une horloge de 8GHz. Il est constitué de portes numériques logiques qui forment le diviseur de fréquences synchrone qui divise successivement l'horloge jusqu'à obtenir un signal carré périodique de 250MHz, et le générateur de Walsh qui combine alors les 6 horloges précédentes en 64 séquences de Walsh.

Le DAC permet de synthétiser la série de Walsh du signal à émettre au travers d'une charge résistive différentielle de 100Ω . Il est composé de 64 cellules utilisant une architecture différentielle de type current-steering formée de 6 DACs 1-bit. Le DAC unitaire est empilé sous 1V et il est formé d'une source de courant unitaire de $3.2\mu\text{A}$ cascodée et surmontée par une paire de switch différentiel cascodée. Ainsi, selon le bit de poids du coefficient de Walsh concerné, les dimensions du DAC 1-bit est augmenter du facteur en puissance de deux correspondant en augmentant la multiplicité des transistors. La consommation des 64×6 -bit DAC est de $13,6\text{mW}$ pour une surface de silicium estimée à $0,2\text{mm}^2$.

L'interface de conversion des coefficients de Walsh a pour rôle d'adresser au DAC les 64 coefficients de Walsh codés sur 6-bit issus du calcul algorithmique Matlab sous PC. Elle permettra de tester la puce en réduisant le nombre de pads (512 à défaut) en les acquérant sous une forme série depuis l'extérieur. Les coefficients de Walsh sont alors parallélisés et sauvegardés dans des mémoires SRAM pour être adressés en temps voulu au DAC.

Le cœur de l'émetteur de Walsh (synthétiseur et DAC) a été simulé, puis comparé au résultats comportementaux issus de l'algorithme Matlab. Le spectre relevé, et correspondant à la synthèse d'un sinus de 2.5GHz de fréquence, présente une réjection de 40dB des spurs sur plus de 4GHz de bande. Ce design démontre donc la capacité de l'émetteur de Walsh à gérer des vitesses de switching allant jusqu'à 16GSps en consommant uniquement 25mW . Le DAC présente alors de meilleures performances que l'état de l'art des RF-DACs en ne consommant que 0.26pJ/bit transmis.

Ces résultats montrent que l'émetteur de Walsh est une solution compétitive par rapport aux architectures conventionnelles qui échouent à réduire leurs prix énergétiques. Son intégration dans un émetteur radio-logicielle permettra donc de satisfaire plus aisément les attentes des futurs standards de communication.

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Contents

List of Figures	xv
List of Tables	xix
List of Abbreviations	xxi
List of Notations	xxv
Introduction	1
Chapter 1: Wideband Transmitters	3
1.1 Wireless Communication And Architecture:.....	5
1.1.1 Wireless Communication.....	5
1.1.2 Radio Frequency Architecture:.....	7
1.2 Transmitter Architecture for New Standards:.....	9
1.2.1 The Limits of the Classical Architectures:.....	9
1.2.2 The Software Radio Architecture:.....	10
1.2.3 The Future 5G Standard:.....	11
1.2.4 The Carrier Aggregation:.....	12
1.3 Direction of Research Toward Flexible Transmitters:.....	14
1.3.1 The Reconfigurable Transmitters:.....	15
1.3.2 The Direct Digital Modulation Transmitters:.....	17
1.3.3 The All-Digital Transmitters:.....	19
1.3.4 The RF-DACs:.....	21
1.4 Conclusion:.....	23

Chapter 2: The Walsh Transmitter	25
2.1 The Walsh Algorithm:.....	27
2.1.1 Dynamic Frequency Reconstruction:.....	28
2.1.2 The Walsh Mathematical Approach:.....	30
2.1.2.1 Background on Walsh Transforms:.....	31
2.1.2.2 The Walsh Series:.....	31
2.1.3 The Walsh Sequences Synthesis:.....	33
2.2 System Simulation Flow:.....	36
2.2.1 System Overview:.....	37
2.2.2 Walsh Series Generation Process:.....	38
2.2.3 Determination of the Optimum Order (M):.....	40
2.2.3.1 Time-Domain Investigation:.....	41
2.2.3.2 Frequency-Domain Investigation:.....	42
2.2.3.3 Determination of f_{ref} :.....	43
2.2.4 Determination of the Optimum Resolution (N):.....	45
2.2.4.1 D/A Conversion:.....	45
2.2.4.2 Quantization Noise:.....	45
2.2.4.3 SQNR Calculation:.....	46
2.3 Concurrent Transmission:.....	50
2.3.1 Three CC Signal Synthesis:.....	50
2.3.2 Error Vector Magnitude (EVM) Calculation:.....	52
2.4 Conclusion:.....	54

Chapter 3: Circuit Design	55
3.1 Technological Considerations and Design Flow:.....	57
3.1.1 The Cmos 28nm FDSOI Technology:.....	57
3.1.2 Design Flow:.....	59
3.2 The Walsh Sequences Synthesizer:.....	60
3.2.1 The Frequency Divider:.....	61
3.2.1.1 The Voltage Limiter:.....	61
3.2.1.2 The Synchronous Counter:.....	63
3.2.2 The Walsh Generator:.....	65
3.3 The DAC:.....	67
3.3.1 The Driver:.....	68
3.3.2 The Current Sources (CSs):.....	70
3.3.3 The DAC Design:.....	71
3.3.3.1 The DAC Unit Cell:.....	71
3.3.3.2 The 6-Bit DAC:.....	72
3.3.3.3 The Whole DAC:.....	74
3.4 The Walsh Coefficients Conversion Unit:.....	76
3.4.1 The SRAM:.....	78
3.4.2 The SPI:.....	78
3.4.3 The Walsh Coefficients Addressing:.....	80
3.4 Conclusion:.....	81
Conclusion	83

Bibliography	85
Annex A	89
Annex B	92

List of Figure

Figure 1-1: Global handset data traffic evolution [2]..... 6

Figure 1-2: Transceiver architecture..... 7

Figure 1-3: Classical direct up-conversion RF transmitter architecture..... 7

Figure 1-4: Classical direct down-conversion RF receiver architecture..... 8

Figure 1-5: Ideal software radio transmitter architecture..... 10

Figure 1-6: Radar diagram of 5G disruptive capabilities [4]..... 11

Figure 1-7: Intra-band and inter-band CA configurations [5]..... 13

Figure 1-8: Software Defined Radio transmitter architecture..... 15

Figure 1-9: Reconfigurable transmitters’ architecture..... 15

Figure 1-10: Direct digital transmitters’ architecture..... 17

Figure 1-11: All-Digital transmitters’ architecture..... 19

Figure 1-12: Radio evolution over the spaces of programmability and functionality [28]..... 23

Figure 2-1: Signal generation illustrating its decomposition in Fourier domain..... 28

Figure 2-2: Harmonic population given by PLL square waves..... 29

Figure 2-3: Dynamic frequency reconstruction scenario..... 30

Figure 2-4: The sixteen first Walsh sequences..... 32

Figure 2-5: Generation of $Wal(9,t)$ starting from Rademacher functions..... 34

Figure 2-6: The Walsh transmitter synopsis..... 37

Figure 2-8: Time-domain representation of the Walsh series for different orders..... 41

Figure 2-9: Frequency-domain representation of the Walsh series expansion for different orders
..... 42

Figure 2-10: Frequency-domain representation of the Walsh series for different orders..... 44

Figure 2-11: Discrete time-domain representation of the approximation error..... 46

Figure 2-12: Spectral representation of quantized sine wave at frequency f_{in} 49

Figure 2-13: SQNR of the Walsh conversion versus N..... 49

Figure 2-14: a- Spectrum obtained with 3 CC aggregation, b- zoom on the QAMs.....51

Figure 2-15: Eye and constellation diagrams resulting of 3 CC aggregation.....52

Figure 3-1: FDSOI NMOS and PMOS cutting view [43].....58

Figure 3-2: The Walsh transmitter block diagram (M=64/N=6).....59

Figure 3-3: The Walsh sequences synthesizer.....60

Figure 3-4: The frequency divider.....61

Figure 3-5: The voltage limiter.....62

Figure 3-6: Output of the voltage limiter for different input voltage values.....62

Figure 3-7: Frequency divider schematic.....63

Figure 3-8: Full frequency divider simulation results.....64

Figure 3-9: The Walsh generator architecture.....65

Figure 3-10: Architecture of the order 8 Walsh generator.....66

Figure 3-11: Some sequences at the output of the sequence synthesizer.....66

Figure 3-12: The DAC architecture.....67

Figure 3-13: The driver architecture.....68

Figure 3-14: Driver control signals.....69

Figure 3-15: DAC unit cell.....71

Figure 3-16: a- 6-bit DAC differential output voltage, b- zoom between 2.2ps and 2.7ps.....73

Figure 3-17: DAC output signal in 100Ω differential.....74

Figure 3-18: Spectra of a single tone RF signal of 2.50 GHz before, after coefficient quantization and at Walsh DAC output.....75

Figure 3-19: Walsh 6 bit coded coefficients distribution.....77

Figure 3-20: SPI's symbol.....78

Figure 3-21: SPI's digital design flow.....79

Figure 3-22: The link between SPI and SRAM.....80

Y

Figure A-1: The Walsh sequences from $Wal(16, t)$ to $Wal(31, t)$ 89

Figure A-2: The Walsh sequences from $Wal(32, t)$ to $Wal(47, t)$	90
Figure A-3: The Walsh sequences from $Wal(48, t)$ to $Wal(63, t)$	91

List of Table

Table 1-1: Evolution of technology generation in terms of services and performances [1].....6

Table 1-2: Performances of the reconfigurable transmitters.....17

Table 1-3: Performances of the direct digital modulation transmitters.....19

Table 1-4: Performances of all-digital transmitters.....20

Table 1-5: Performances of RF-DACs.....22

Table 2-1: Walsh sequence expressions as functions of the primary Walsh sequences.....35

Table 2-2: SFDR calculation results for different order.....43

Table 2-3: EVM calculation results for different modulation schemes (M=64 / N=6).....53

Table 3-1: Evolution of the time duration of the logical values at the output of the Voltage limiter in function of the input magnitude.....63

Table 3-2: Driver truth table.....68

Table 3-3: DAC unit cell MOSFET sizing.....72

Table 3-4: Currents spent in the bleeder branches.....72

Y

Table B-1: The Walsh sequence expressions from $Wal(0,t)$ to $Wal(31,t)$ in function of the primary sequences.....93

Table B- 2: The Walsh sequence expressions from $Wal(32,t)$ to $Wal(63,t)$ in function of the primary sequences.....94

List of Abbreviations

5G PPP	5G infrastructure Public Private Partnership
ADC	Analog-to-Digital Converter
BB	Base Band
BOX	Buried Oxide
BP	Back Plane
BW	Bandwidth
CA	Carrier Aggregation
CC	Component Carrier
CMOS	Complementary Metal Oxide Semiconductor
DA	Digital-to-Analog
DAC	Digital-to-Analog Converter
DCO	Digital Controlled Oscillator
DFT	Discrete Fourier Transform
DK	Design Kit
DPA	Digital Power Amplifier
DPLL	Digital Phase Locked Loop
DR	Data Rate
DRFC	Direct Radio Frequency Converter
EVM	Error Vector Magnitude
FBB	Forward Back Biasing

FDSOI	Full-Depleted Silicon On Insulator
FE	Front-End
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
I/Q	In-phase and Quadrature
IC	Integrated Circuit
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Less Significant Bit
LUT	Lock Up Table
LVT	Low Voltage Threshold
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most Significant Bit
PA	Power Amplifier
PLL	Phase Locked Loop
PWL	Piece Wise Linear
QAM	Quadrature Amplitude Modulation
RBB	Reverse Back Biasing
RF	Radio Frequency
RVT	Regular Voltage Threshold
SDR	Software Defined Radio
SFDR	Spurious-Free Dynamic Range
SNR	Signal to Noise Ratio
SPI	Serial to Parallel Interface

SQNR	Signal Quantization Noise Ratio
SR	Software Radio
SRAM	Static Random Access Memory
VCO	Voltage Controlled Oscillator
xG	x th Generation

List of Notations

f_{bin}	Frequency bin
(a_0, a_p, b_q)	Walsh coefficients
M_{cycle}	Number of used cycle involved in DFT
N_s	Number of samples involved in DFT
P_i	Power of the input signal
P_n	Power of the noise
P_{spur}	Power of the undesirable spurs
V_i	Magnitude of the input signal
$X_w \left[\frac{k}{f_0} \right]$	Walsh approximated signal samples in frequency domain
f_i	Frequency of the input signal
f_{max}	Frequency band of interest
f_{ref}	Walsh coefficients frequency refresh
f_s	Sampling frequency
f_0	Clock frequency
$x_w \left[\frac{n}{f_0} \right]$	Walsh approximated signal samples in time domain

$\frac{\delta I}{I}$	Current standard deviation
$Cal(i, t)$	i^{th} even Walsh sequence
L	Transistor length
M	Walsh series order
N	Number of bits involved in DA conversion
$Sal(i, t)N$	i^{th} odd Walsh sequence
W	Transistor width
$Wal(i, t)$	i^{th} Walsh sequence
j	Number of primary Walsh sequences
$rad(j, t)$	j^{th} Rademacher sequence
$x \left[\frac{n}{f_0} \right]$	Input signal samples in time domain
μ	Carrier mobilities

Introduction

The use of electromagnetic waves as a medium for transmitting information between the mobile terminals has quickly lead to a congestion of the frequency spectrum. To improve the data traffic flow between users, the authorities regulate the access to the frequency bands by imposing stringent standards to the mobile telecommunication. Thus, and in order to increase their data exchange capabilities the next generations of mobile terminals have to dynamically use the spectral resources.

These constraints affect the design of mobile transceivers. They must transmit high data rates by using multiple carriers and various modulation schemes, while consuming as less energy as possible, in order to save their battery life.

Chapter 1 presents the transmitter classical architecture and its limits to meet these requirements. To overcome these challenges, several ongoing evolutions toward more digital architectures as advocated by the Software Radio principle are exposed. Despite a gain in flexibility, it results in an important power consumption mainly due to the digital to analog conversion.

Chapter 2 proposes a new way to encode the signal to be transmitted by looking at it spectrum and coding it differently than usual. It borrows the principle of the Walsh series expansion to project the signal in a basis of square waves. The data conversion process deals with their spectral content through the digital coding of their magnitudes. The signal reconstruction is performed thanks to a custom sequence synthesizer and digital-to-analog converter. The whole system is named the Walsh transmitter. The sizing of the system is assessed toward multi-carrier and multi-modulated radio frequency signal generation using Matlab simulations.

Chapter 3 describes the design of the Walsh transmitter in ST-Microelectronics CMOS 28nm FDSOI. The design of every functional block is detailed using a top/down approach from the architecture to the transistor level implementation. At each step, simulations are presented to validate each block behavior. Then the complete system (i.e. the Walsh transmitter) is simulated and the results are compared with the Matlab data. It brings a proof of concept that the Walsh transmitter is a very promising architecture for targeting multiple carrier aggregation. Finally, a custom designed digital interface is proposed for a forthcoming test of the integrated version of the Walsh transmitter.



1st transmitters

1.

Contents

1.1 Wireless Communication and Architectures

1.1.1 Wireless Communication

1.1.2 Radio Frequency Architectures

1.2 Transmitter Architecture for New Standards

1.2.1 The Classical Transmitter Architecture Limits

1.2.2 The Software Radio Architecture

1.2.3 The Future 5G Standard

1.2.4 The Carrier Aggregation

1.3 Direction of Research Toward Flexible Transmitters

1.3.1 The Reconfigurable Transmitters

1.3.2 The Direct Digital Modulation Transmitter

1.3.3 The All-Digital Transmitters

1.3.4 The RF-DACs

1.4 Conclusion

Chapter 1 presents an introduction to wireless Radio Frequency (RF) transmitters. It shows the limits of the classical architecture when facing the future standard specifications in terms of bandwidth, power consumption and cost. The Carrier Aggregation technique (CA) is presented as a solution for further data rate increases. However, for power budget reasons it requires the help of a new kind of architecture. A state-of-the-art is presented to describe the transmitter evolution toward the Software Radio (SR) architecture. It highlights the digitalization of the transmitter architecture which is mainly based on the use of a RF Digital to Analog Converter (RF-DAC). Even if their use broadens the bandwidth, they are still too power greedy to be implementable in a handset.

Keywords: RF, CA, SR, 5G, RF-DAC, bandwidth, power consumption, cost,

1.1 Wireless Communication and Architecture:

1.1.1 Wireless Communication

After the demonstration of the existence of radio waves by H. Hertz, the first radio transmission was born in 1906. This feat was achieved by R. Fessenden owing to the equipment built by Marconi five years earlier. It was a long distance analog radio transmission carrying voice and music encoded by amplitude modulation. Because of the limitation of the equipment (size, cost, reliability ...) and the transmission quality, the radio transmission still had limited use. The development of the remote communication started flourishing with the invention of the transistor in 1948 and came into practical use by early 1950s. Involving Nyquist sampling theory, the communication system became digital using mostly twisted pair wire media for civil applications. The wireless systems were reserved for military application and it was only in 1981 that radio frequency analog systems first became a household commodity with the apparition of the First *Generation* (1G) of mobile phones.

Since then, the mobile RF communication evolved in an unparalleled way. Beginning from phone calls, each generation of mobile technology has been motivated by offering the user new services with a better quality experience.

Table 1-1: Evolution of technology generation in terms of services and performances [1]

Generation	Primary services	Key differentiator
1G	Analog phone calls	Mobility
2G	Digital phone calls Messaging	Secure, mass adoption
3G	Phone calls Messaging Data	Better internet experience
3,5G	Phone calls Messaging Broadband data	Broadband internet Applications
4G	All IP services	Faster broadband internet Lower latency

This evolution and emergence of smart phones brought to common people the access to use the internet in a very different way. The internet is more and more nomadic and as a result, the global amount of data exchanged by handsets is permanently growing as depicted in Fig 1.1.

Figure 1-1: Global handset data traffic evolution [2]

1.1.2 Radio Frequency Architecture:

The transceiver is the element which connects the wireless terminal to the network using radio-frequency electromagnetic waves. It is mainly composed of a transmitter and a receiver that exchange information through the communication medium (the air) as shown in Fig. 1.2.



Figure 1-2: Transceiver architecture

At the extremity of the transmitter/receiver there is an antenna that radiates/captures the electromagnetic waves to/from the air. To avoid the attenuation of those electromagnetic waves during their propagation in the air, their wavelength should be small. Thus, their frequency is high. That is why the digital data (which are of lower frequency) are conditioned by frequency transposition process. They are up-converted to be carried at radio frequency as illustrated in

Fig. 1.3. before transmission. After reception, they are down-converted to be processed at *Base Band* (BB) frequency (shown in Fig. 1.4). The information is then exchanged between the transmitter and the receiver at high frequencies with respect to various standards which set the traffic rules.

Transmitter:

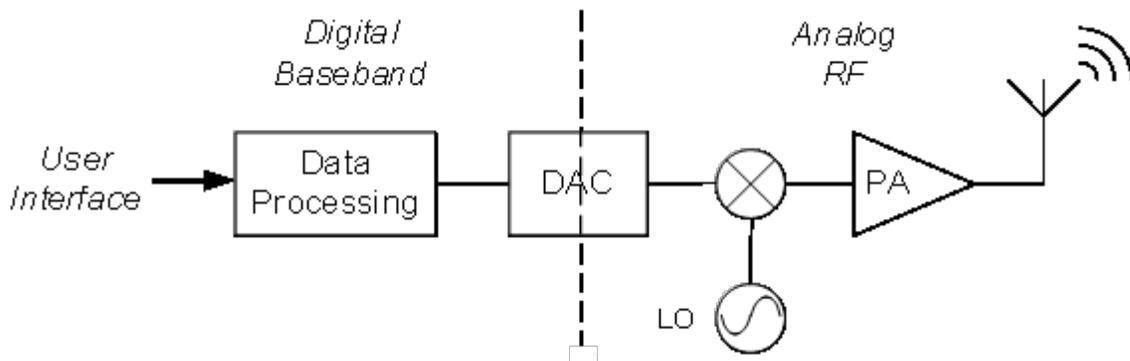


Figure 1-3: Classical direct up-conversion RF transmitter architecture

The transmitter is composed of:

- A BB processor
- A DAC
- A mixer + a *Local Oscillator* (LO) to up-convert the signal to the carrier frequency
- A *Power Amplifier* (PA)

The BB processor synthesizes and encodes the user actions in digital information that are of low frequency. The DAC turns those into analog signals that are up-converted to analog RF by mixing with a frequency carrier delivered by the LO. Then the resulting analog signal is amplified by the PA before sending through the antenna.

Receiver:

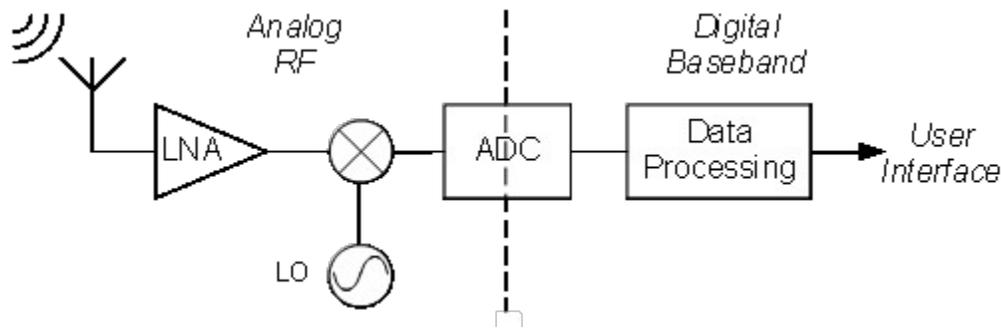


Figure 1-4: Classical direct down-conversion RF receiver architecture

The receiver is composed of:

- A Low Noise Amplifier (LNA)
- A mixer + LO → to down-convert the signal to baseband
- An Analog-to-Digital Converter (ADC)
- A BB processor

The incoming electromagnetic signal is captured by the antenna that converts it into an analog signal. This low power signal is then amplified by the LNA in order to obtain the cleanest possible low frequency analog signal after down conversion. Therefore, the ADC allows recovering the BB transmitted data. Note that the transmitter and the receiver can share the same processor, antenna and the same local oscillator.

1.2 Transmitter Architecture for New Standards:

1.2.1 The Limits of the Classical Architectures:

The classical architectures described previously suffer from their rigid analog *Front-End* (FE). All the analog FE blocks are designed to be operational at a specific given frequency. Even though the LO can generate carriers with a tuning range of the order of *Gigahertz* (GHz), the other parts will degrade the whole transceiver performance. This kind of architecture can only process a *Component Carrier* (CC) signal. Besides, they can only address one standard corresponding to a narrow frequency band.

However, the congestion of the frequency spectrum and the increasing user's data demand force the need of more bandwidth access. Hence, new standards are introduced to reach larger

and even unlicensed bands. The use of a particular standard is based on the service requested by the user. If the service requests to pass a lot of data, then a large bandwidth standard is used. On the other hand, there is no point to attribute and waste tens of *Megahertz* (MHz) of bandwidth for lower *Data Rate* (DR) services. That is why each standard has its own specificities: frequency carrier, bandwidth and so on.

Therefore, versatile handsets have to embed multiple transceivers to address the user's data demand while avoiding congestion issues. Of course it is possible to embed multiple analog FE to address 2 or 3 frequency bands. However, because of technological constraints, this is no longer enough to face the permanent generation of new standards. Increasing the number of chipsets in a mobile terminal makes the integration processes more problematic. Integrating multiple chips in a small volume of a handset terminal will:

- increase the total price of the device because of the cumulated die area
- augment the whole handset energy consumption thereby reducing the battery life
- deteriorate the performances because of the disturbance between the transceivers

For these reasons, new kinds of transceiver architectures are required. They should address several standard in the same time or alternatively while using only one analog FE. This will ensure a dynamic multi wide band access to the spectrum so that they can reach several CC of different bands at the same time. These are the SR architectures.

1.2.2 The Software Radio Architecture:

J. Mitola proposed a new radio paradigm to satisfy the new wireless communication perspectives [3]. The idea is to move the limit between the baseband domain and the analog RF domain, approaching the digital processing to the antenna. It avoids the frequency transposition process by reducing the number of analog front-ends in the PA, hence making the whole transmitter much more flexible. The ideal architecture is depicted in Fig. 1.5. It is composed of 3 blocks:

- A BB/RF processor
- A wideband DAC
- A wideband PA

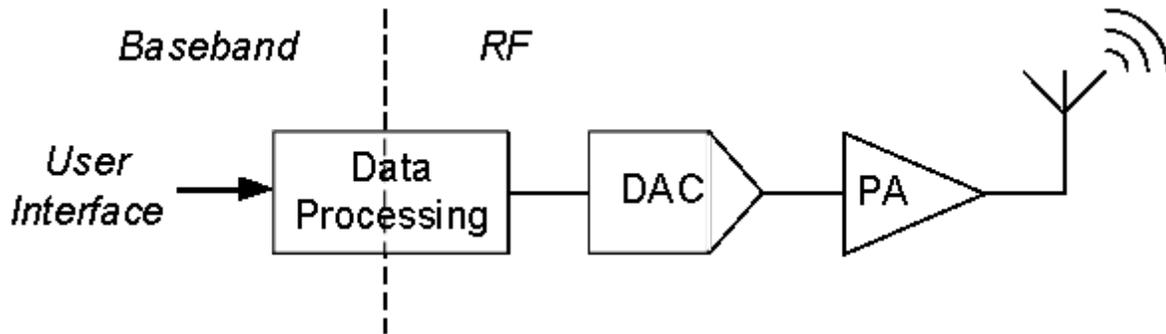


Figure 1-5: Ideal software radio transmitter architecture

This ideal architecture directly computes the modulated signal within the digital processor. The particularity is that the data processing is made at very high frequency. Thus it allows concurrent transmission directly and digitally synthesizing multi-carrier, multi-modulated signal. The wideband DAC converts the whole transmitting band of several GHz to the analog domain. Then, the PA amplifies the signal before transmission through the antenna.

Owing to its reconfigurable characteristics this ideal architecture can address multiple CC in the same time or alternatively while using only one analog FE. It offers a full compatibility with all the existing standards. It can even support future standards like the 5G, by simple software update.

1.2.3 The Future 5G Standard:

The 5G standard supports automotive, healthcare, home monitoring, media and entertainment. It is clear that 5G is defined by its ability to handle enough bandwidth for more than the 7.5 billion expected smartphone subscriptions. This brings the *5G Infrastructure Public Private Partnership* (5G PPP) to define the performance parameters for the future 5G (Fig. 1.6). The target is to ensure continuity of user experience in challenging situations such as high mobility or very dense or sparsely populated areas, while providing all kind of services such as teleworking. Moreover, all these need to be done with a very high reliability, in a secure way and consuming less power as possible.

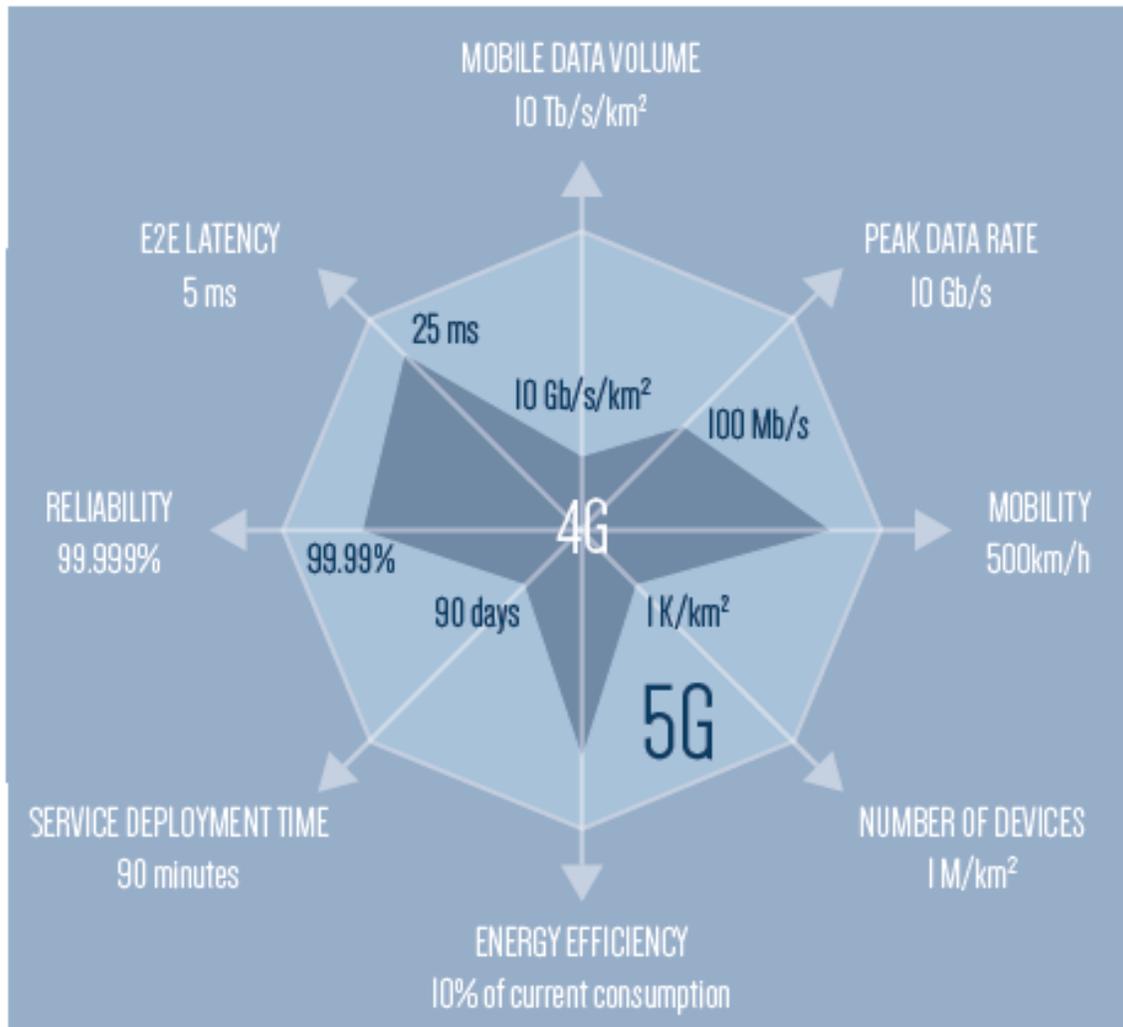


Figure 1-6: Radar diagram of 5G disruptive capabilities [4]

Thus comparing 5G with the previous generation Fig 1.6, the network and the mobile terminal should be able to address the following specifications:

- 1000 × in mobile data volume per geographical area reaching a target of 0.75 Tbps for a stadium
- 1000 × in number of connected devices reaching a density ≥ 1 M terminals/km²
- 100 × in user data rate reaching a peak terminal data rate ≥ 1 Gbps for cloud applications inside offices
- 1/10 × in energy consumption compared to 2010 while traffic is increasing dramatically at the same time
- 1/5 × in end-to-end latency reaching delay ≤ 5 ms

- $1/1000 \times$ in service deployment time reaching a complete deployment in ≤ 90 minutes
- Guaranteed user data rate ≥ 50 Mbps
- Capable of IoT terminals ≥ 1 trillion
- Service reliability $\geq 99.999\%$ for specific critical services
- Mobility support at speed ≥ 500 km/h for ground transportation
- Accuracy of outdoor terminal location ≤ 1 m

With regard to the previous specifications, it is definitely impossible to keep going with the transmitter architecture depicted in Fig 1.3. Next generation of handsets should involve at least the possibility to use 10 CCs at the same time. The SR transmitter architecture depicted in Fig. 1.5 can win this challenge by performing *Carrier Aggregation (CA)*.

1.2.4 The Carrier Aggregation:

The CA principle:

CA is a processing which consists of aggregating multiple CC signals in only one signal. The resulting signal spectrum is composed of many lobes that form an extended bandwidth signal. The spectral spreading of these lobes is divided into different ways that determine the configuration of the CA as shown in Fig. 1.7:

- **The intra-band contiguous CA** configuration refers to contiguous carriers aggregated in the same operating band.
- **The intra-band non-contiguous CA** configuration refers to non-contiguous carriers aggregated in the same operating band.
- **The inter-band CA** configuration refers to non-contiguous carriers aggregated in different operating bands, where the carriers aggregated in each band can be contiguous or non-contiguous.

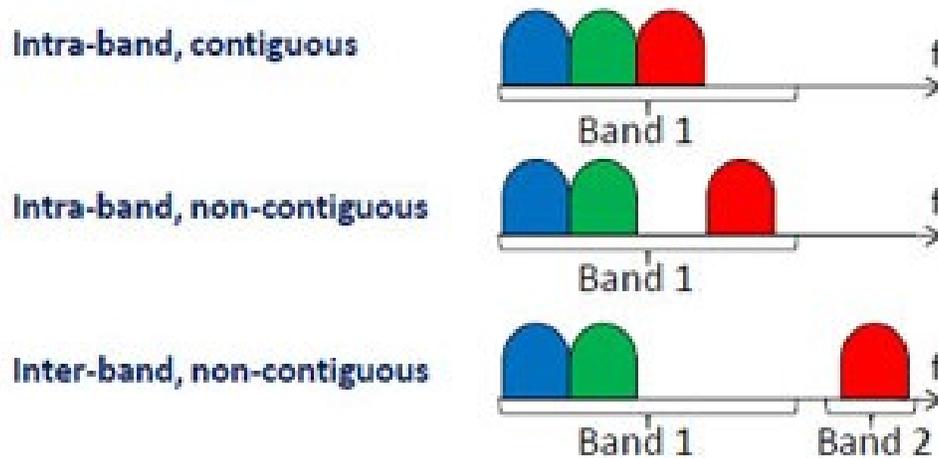


Figure 1-7: Intra-band and inter-band CA configurations [5]

The benefits of CA:

Thus, CA is an efficient technique that gives the operators a powerful tool to get the most out of their licensed spectrum resources as well unlicensed carrier spectrum. They are typically spread out on multiple sub bands of the frequency spectrum and mostly addressed by different CCs which are limited to a few MHz of bandwidth. Due to CA, the operators get more capacity and coverage capabilities:

- **Higher speeds:** CA increases the spectrum resources which provide higher speeds across the cell coverage.
- **Capacity gain:** aggregating multiple CC increases the spectrum but also allows a dynamic traffic scheduling across the entire spectrum. It increases the DR while improving the network efficiency. Hence, it provides all the users with a better experience: a user that was facing congestion previously on one carrier can be scheduled to a carrier with more capacity, thereby maintaining a consistent high-quality experience for all the users.
- **Bandwidth extension:** most of the operators have fragmented spectrum covering different bands and bandwidth. CA helps to combine these into more valuable frequency resources. Moreover, it offers the possibility to reach the unlicensed parts of the spectrum to supplement their resources.

The CA is the technique to resolve the spectrum congestion issue and to take on the challenges imposed by future standards. It allows exchanging of a huge amount of data fragmented on various frequency bands. It requires the use of SR architectures which cover several GHz of bandwidth with high resolution while working at low power to improve handset battery life.

The next section describes the transmitter's evolution that tends to meet the requirements of tomorrow. This state-of-the-art shows the progression of the transmitter architecture digitalization toward SR architectures. It demonstrates the feasibility of a full direct digital synthesized multi-carrier wideband transmitter.

1.3 Direction of Research Toward Flexible Transmitters:

In the literature there is a plethora of publications on RF transmitters that enable changing radio parameters such as carrier frequency, channel bandwidth, transmitter's spectral purity and power consumption (Fig. 1.8).

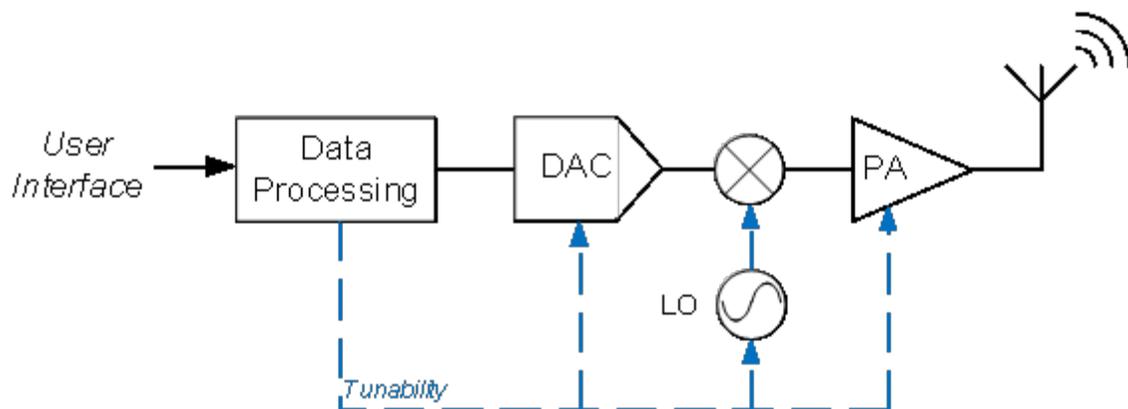


Figure 1-8: Software Defined Radio transmitter architecture

It exhibits a certain evolution that tends to the ideal RF transmitter architecture, moving the processor closer to the antenna:

- Analog front-end reconfiguration according to a targeted standard

- Mustering Analog functionalities
- Analog functionalities replaced by digital ones
- Wideband high speed DAC insertion

1.3.1 The Reconfigurable Transmitters:

The first step toward the previously described ideal architecture is to reconfigure the RF analog front-end of the direct conversion architecture [6] as per digital commands Fig. 1.9.

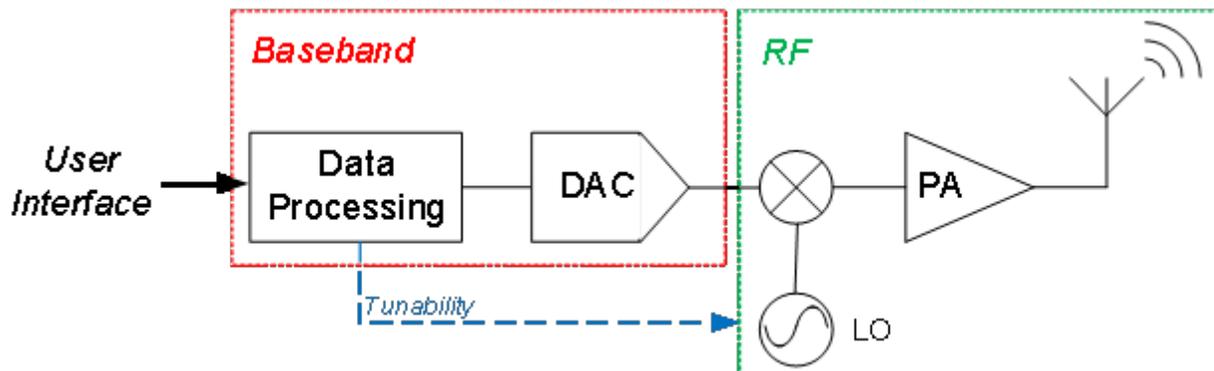


Figure 1-9: Reconfigurable transmitters' architecture

The purpose is to digitally select one of 2 or 3 transmission chains (selecting a frequency band) and to tune more or less the carrier frequency (selecting one of the frequency band sub-bands). Then, it becomes a narrow band transmitter targeting only one sub band of one frequency band at a time. Several kinds of reconfigurable transmitters are reported in the literature. Here are a few of them:

[7] presents a transceiver based on direct conversion and that provides extensive programmability of the LO generator, mixers and *Pre-PA* (PPA). The asset of this architecture is a low phase-noise *Voltage Controlled Oscillator* (VCO) with a large tuning range (3 to 6 GHz). An additional circuit called divide and multiply in quadrature is used to extend this frequency range to 100 MHz and up to 6GHz. It can assume 20 MHz channel bandwidth.

[8] presents a multiband multimode transmitter dedicated to the 2G, 3G and 4G communication standards but only one standard is active at any given time. It is also based on direct conversion but it implements multiple RF paths (each one designed to meet the requirement of previously enounced standards).

[9] proposes a reconfigurable transmitter architecture functioning from 50 MHz to 6 GHz frequency band. It uses a particular conversion scheme based on splitting the conversion process according to the synthesized signal frequency range. Then in order to filter LO harmonics, a two-step up conversion is employed for lower RF range and a direct up conversion for higher ones.

[10] offers a transmitter supporting intra-band CA owing to only one I-Q baseband path (while the others are using 2) including compensation techniques to minimize the power of the wideband analog baseband. This architecture, with a 100 MHz bandwidth, allows the aggregation of two non-contiguous carriers located in the same frequency band.

Table 1-2: Performances of the reconfigurable transmitters

	Bandwidth [MHz]	RF range [GHz]	Consumption [mW]	CMOS node [nm]
[7]	20	0,1 - 6	84	130
[8]	20	0,7 - 2,7	200	90
[9]	40	0,05 - 6	900	130
[10]	100	0,1 - 6	103	65

1.3.2 The Direct Digital Modulation Transmitters:

This kind of transmitter focuses on reducing the number of analog blocks. Therefore, multiple analog operations can be done by only one block. Mainly it is the digital-to-analog conversion and the mixing that are merged together (Fig. 1.10).

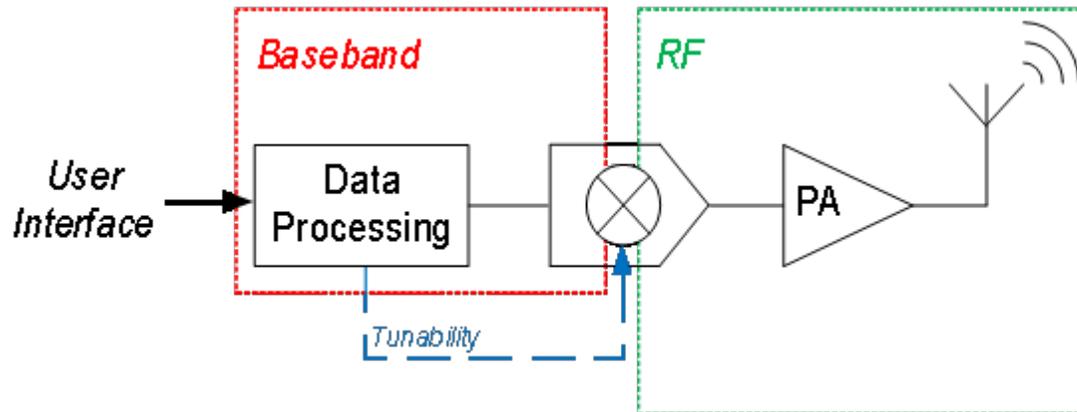


Figure 1-10: Direct digital transmitters' architecture

This architecture makes the RF front-end more tunable by the use of an increased number of digital signals. Hence the transmitter is more flexible and easier to integrate. Following are some of the achievements demonstrated by researchers:

[11] presents a circuit consisting in a digital delta-sigma modulator and a digital mixer with a RF band-pass reconstruction filter. This architecture replaces the analog circuits in the baseband signal path with high speed digital circuits, thereby taking advantage of digital *Complementary Metal Oxide Semiconductor* (CMOS) scaling.

[12] exhibits an all-digital RF signal generator using delta-sigma modulation and digital mixing. It employs specific techniques such as redundant logic and non-exact quantization providing a 50 MHz bandwidth at a 1 GHz frequency bandwidth.

[13] proposes a fully digital multimode polar transmitter. Here, the digital data are converted from the *In-phase and Quadrature* (I/Q) domain to polar. The resulting phase signal drives a *Digital Controlled Oscillator* (DCO) via a *Digital Phase Locked Loop* (DPLL). This modulated DCO clock drives the RF-DAC which is dynamically biased by the magnitude signal from the

coordinate conversion after gain controlling. Then the RF-DAC which acts as a current-mode mixer, synthesizes the analog output RF signal.

[14] exposes an all-digital quadrature architecture where the I/Q bit streams are directly fed to the input of a *Digital-PA* (DPA). Here, instead of employing a *Phase-Locked Loop* (PLL) to up-sample the BB signal, a configurable frequency divider is used. It derives the RF carrier frequency directly with an 800 MHz clock that runs a *Look-Up Table* (LUT) to drive the DPA.

[15] describes a RF I/Q power DAC transmitter with an embedded mixed-domain *Finite Impulse Response* (FIR) filter to suppress the off-band quantization noise. Thus, it allows full duplex operations

[16] presents a wideband 2×13 bit I/Q RF DAC based all digital modulator. The BB digital signals are digitally mixed and converted into the analog domain with the help of digital to RF amplitude converters.

[17] proposes an IQ digital Doherty transmitter that offers better output power performances. It uses 4 direct digital RF modulators organized in a Doherty-like configuration through two different transformers.

Table 1-3: Performances of the direct digital modulation transmitters

	Bandwidth [MHz]	RF range [GHz]	Consumption [mW]	CMOS node [nm]
[10]	200	5,25	187	130
[12]	50	0,01 - 1	120	90
[13]	4	0,9 & 1,9	250	-
[14]	80	2,2	510	40
[15]	20	2,4	515	65
[16]	150	0,06 - 3,5	560	65
[17]	10	2,15	500	90

1.3.3 The All-Digital Transmitters:

This type of architecture is designed to have almost a complete absence of the analog functionalities except the RF power amplification and the filtering, while using a *Direct Radio Frequency Converter* (DRFC) Fig. 1.11.

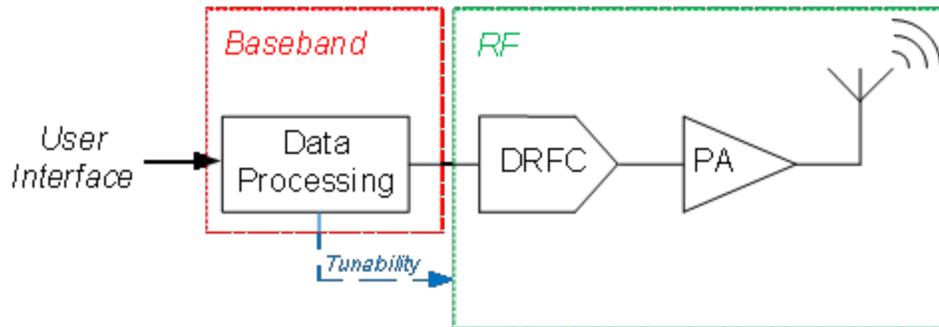


Figure 1-11: All-Digital transmitters' architecture

The development of the *Field Programmable Gate Arrays* (FPGA), which are very reconfigurable and programmable, motivated a lot of works on digital architectures [18]. They are mainly used to implement digital BB and *Intermediate Frequency* (IF) functionalities. This brings the whole transmitter architecture more programmable with capabilities to digitally combine signals from multiple channels while consuming less power.

[19] exhibits an all-digital transmitter that directly synthesizes RF signals in real time in the digital domain, thanks to a *Quadrature Amplitude Modulation* (QAM) modulator and one RF pulse width modulator implemented into an FPGA.

[20] presents an original architecture, that uses a LUT loaded with all the possible symbol transition given by a particular modulation implying that the signal is representable by a *Finite State Machine* (FSM). Next, the bit stream generation is based on replacing the RF analog samples labeling the FSM edges with the corresponding list-coded bit streams. These are then filtered and radiated directly by the antenna.

[21] proposes an FPGA based all digital transmitters capable of encoding multi-bit baseband signals into a single bit RF signal, enabling the use of switching mode PA. Multi-rate filters are used to achieve high interpolation rates, followed by a low pass delta-sigma modulator. The up conversion is then performed using direct digital frequency synthesis based on a DCO.

[22] exhibits also a transmitter but it uses 2 first order sigma-delta modulators implemented in parallel. The binary signal is then passed through high-speed multiplexing circuits running at 10 GHz thereby converting the signal to 2.5 GHz.

Table 1-4: Performances of all-digital transmitters

	Bandwidth [MHz]	RF range [GHz]	Architecture	Implementation
[19]	20	0,8	PWM	FPGA
[20]	-	1 - 13	DSM-LUT	Instrumentation
[21]	2	0,8	DSM	FPGA
[22]	2	2,5	DSM	FPGA+intrumentation

All the previous references on all-digital transmitters use *Digital-to-RF Converters* (DRFC) which is in charge of up-converting the BB signal into a RF. It requires to up-sample the digital data at a particular rate that should be an integer fraction of the LO frequency. Hence, the flexibility is reduced especially in the case of multi-band concurrent transmission.

To face these problems and to improve quantization filtering (until it is filtered by the RF matching circuitry), [23] proposes a highly configurable architecture where the number and order of the blocks are optimized for a wide range of interpolation factor using a Lagrange interpolator cascaded with an integrator. The flexibility in the position of the digital images as well as the total available bandwidth are enhanced by a programmable clock divider that derives the all the clocks from the LO signal.

Despite their merits, all these digital transmitters still have limited bandwidth of the order of several tens of MHz's and their implementation on FPGA makes them power hungry systems.

1.3.4 The RF-DACs:

The all-digital transmitter is a real step toward ideal SR architecture but, as previously mentioned, they cannot deal with direct digital carrier aggregated signal targeting multi-wideband frequencies using multiple modulation schemes. The main problem to achieve the architecture of Fig. 1.7 is to perform high-speed digital to analog conversion capable of converting the whole band of the synthesizable RF signals independent of their nature (bandwidth, modulation, carrier frequencies ...). Moreover, it should present a high-resolution to ensure the high spectral quality of the transmitted signal.

[24] proposes a 12-bits segmented 6 binary/6 unary current steering DAC using bleeder branches to maintain a permanent current flow in the cascoded differential switching pair. It results in a perfect matching of the loads, independent of the switching activity, thereby reducing the non-linearities under *Less Significant Bit* (LSB) level.

[25] presents a 13-bits segmented 6 binary/ 7 thermometer current steering DAC operating at 9GS/s. It implements (independent of the bit weight) the same design for all the currents sources using dummy current unit cells, thus reducing the dependency of the output capacitance to the coding.

[26] exposes a 28GS/s, 6-bits pseudo segmented current steering DAC that employs time-interleaving technique. It consists of two 14GS/s DACs that works in return-to-zero mode and outputs their current on the two clock edges. The clock frequency is thus reduced to the half of the sampling frequency.

[27] describes a current steering DAC with 14-bits and that operates at 6 GS/s. It implements quad-switching technique that improves current consumption and eliminates distortion by maintaining a constant switching activity.

The following table compares the performances of the previously inventoried RF-DACs using the efficiency as figure of merit. The figure of merit is defined as the ratio of the consumption over the data rate – resolution product.

Table 1-5: Performances of RF-DACs

	Data Rate [GSps]	Number of quantization bit	Consumption [mW]	Efficiency [pJ/bit]	CMOS node [nm]
[24]	2,9	12	188	5,4	65
[25]	9	13	360	3,1	28
[26]	28	6	2250	13,4	90
[27]	6	14	600	7,1	180

All the proposed DACs present a current steering topology. Most of them are segmented. This kind of architecture is a predominant choice for high-speed, high-resolution DACs. In spite of the continued scaling of CMOS technologies, they are hard to integrate in handset terminals. They are still power greedy. They present an average conversion efficiency of several mJ/Gbits while offering 12 bits of coding.

1.4 Conclusion:

Transmitters' architecture implementations are moving from the analog hardware forms toward digital software ones (Fig. 1.12). The digital-RF and the All-Digital architectures are classified as *Software Defined Radios* (SDR). They are multiband and multimode radios which already address present standards. However, they cover only few hundreds of bandwidth and do not support concurrent transmission systematically. That is why they are only paving the way toward ideal SR.

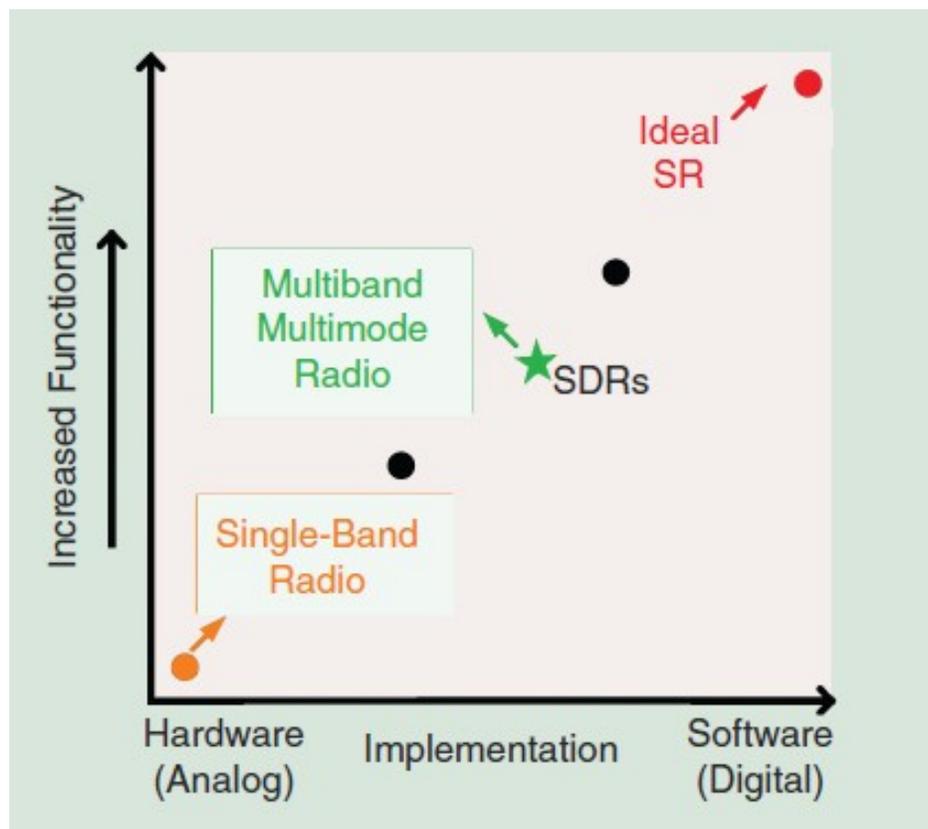


Figure 1-12: Radio evolution over the spaces of programmability and functionality [28]

On the contrary, SR will provide access to a bandwidth of the order of 10 GHz. They will bring more flexibility to the radio while consuming less power. Thus, they will be well suited for future standards subjected to a fast data processing and conversion. Unfortunately, the actual RF-DACs are too power greedy to allow the implementation of a full SR transmitter in a handset terminal.

Innovative solutions to improve the digital to analog conversion are needed to realize suitable transmitter. They have to satisfy the following requirements to integrate a handset terminal:

- Low cost (to address mass market)
- Low power consumption (to ensure a rational battery life)
- High bandwidth (to enable high DR)

We propose to explore a disruptive approach of digital to analog conversion, involving both the coding scheme and the DAC topology.



Ish Transmitter

2.

Contents

2.1 The Walsh Algorithm

2.1.1 Dynamic Frequency Reconstruction

2.1.2 The Walsh Mathematical Approach

2.1.2.1 Background on the Use of Walsh Transform

2.1.2.2 The Walsh Series

2.1.3 The Walsh Sequences Synthesis

2.2 System Simulation Flow

2.2.1 System Overview

2.2.2 Walsh Series Generation Process

2.2.3 Determination of the Optimum Order

2.2.3.1 Time-Domain Investigations

2.2.3.2 Frequency-Domain Investigations

2.2.3.3 Determination of f_{ref}

2.2.4 Determination of the Optimum Resolution (N)

2.2.4.1 D/A Conversion

2.2.4.2 Quantization Noise

2.2.4.3 SQNR Prospection

2.3 Concurrent Transmission

2.3.1 Three CC Signal Synthesis

2.3.2 *Error Vector Magnitude (EVM)* Calculation

2.4 Conclusion

Chapter 2 presents the Walsh mathematical approach based on the generation of the Walsh sequences. From theoretical features of the Walsh series and the data conversion, it highlights the tradeoff between the resolution of the digital data to be converted and the number of sequences used to expand the wanted signal. SQNR equations are extracted. They help to size the Walsh transmitter which is composed of a Walsh series generator and a DAC which weighs and sums the Walsh sequences to recover the wanted analog signal. Simulations using Matlab model of the behavior of the Walsh transmitter are presented as a proof of concept for the Walsh theory. They demonstrate the feasibility of the generation of a concurrent transmission from a few MHz's up to 4GHz.

Key words: DA conversion, Quantization noise, SQNR, EVM, Walsh sequences, Concurrent transmission, PLL.

2.1 The Walsh Algorithm:

The previous chapter introduced the need of more and more bandwidth to meet the increasing user demand for data. This goes on with the development of new transmitter architectures that tend to move from complex analog FE toward more digital solutions. These solutions can provide the bandwidth and the agility needed to deal with the future standards. However, these systems are based on high speed data processing coupled to the use of RF-DACs. Unfortunately, their power consumption still remains too high to allow their implementation in a handset

device. New ways to synthesize and encode signals are then required to lower the power consumption.

2.1.1 Dynamic Frequency Reconstruction:

The idea behind frequency reconstruction is to synthesize a signal from its spectral contents (Fig. 2.1). This can be done by summing its harmonics, f_n provided by a set of VCOs whose magnitudes (V_n) are determined by the coefficients of the signal decomposition in Fourier domain.

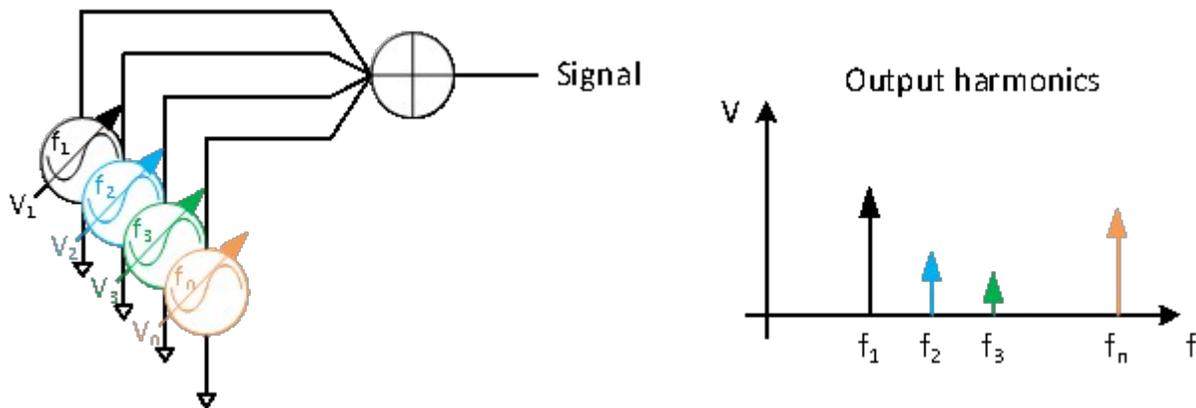


Figure 2-13: Signal generation illustrating its decomposition in Fourier domain

However, since the VCO is a sinewave source, it provides only one harmonic. Hence, several oscillators are needed to properly reconstruct the signal. Implementing them on a single die is difficult to realize because of coupling issues between the different VCO paths. It can lead to a shifting of the oscillation frequency and thus leads to an incorrect harmonic recombination. Even disregarding this problem, the concern remains that a single VCO still consumes a lot of power and silicon area. Thus integrating a number of VCOs to get enough harmonics is not power efficient. A better alternative would be to replace these VCOs by a single source signal. This source should generate enough harmonics to reconstruct the spectral contents of the wanted signal.

As square wave signal contains several harmonics. Using only a few square wave signals will cover as much frequency band as a multiple sine wave signals generated using VCOs. We can

obtain these square waves from a PLL as shown in Fig. 2.2. Its main function is to generate an output signal of frequency f_0 whose phase is related to the phase of an input reference signal of frequency f_r .

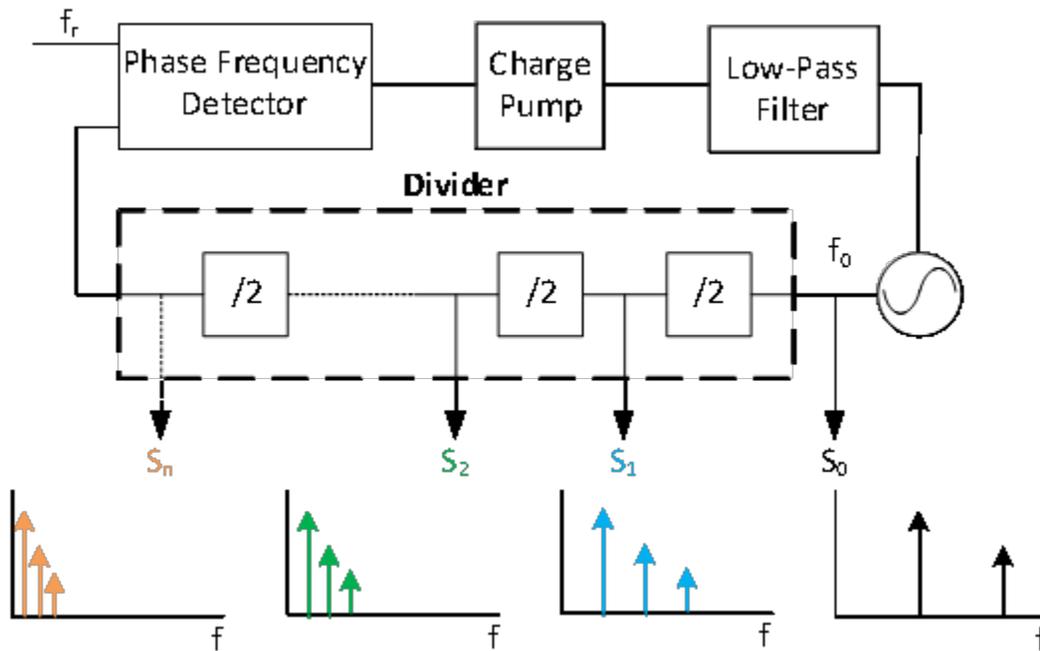


Figure 2-14: Harmonic population given by PLL square waves

Most of the time, this scheme uses a divider to feed the error signal back which is generated as a result of phase comparison. This divider can be wisely used to generate a family of square waves at lower power consumption since most of the circuit is digital. Next, by collecting the square wave signals, S_n , at the divider outputs, we can obtain enough harmonics to have the opportunity to reconstruct the spectral contents of a signal.

But, the question remains whether a recombination of those square wave harmonics can generate an arbitrary signal. More importantly, we need to find out whether there exists a

transform that can digitally and instantaneously process wideband, multi-modulated signals from the harmonics of a family of square waves.

Fourier decomposition is not well suited for square waves as the number of harmonics required is too large. New algebraic operations on these harmonics have to be investigated to synthesize a dynamic frequency reconstruction of any given signal as illustrated in Fig. 2.3.

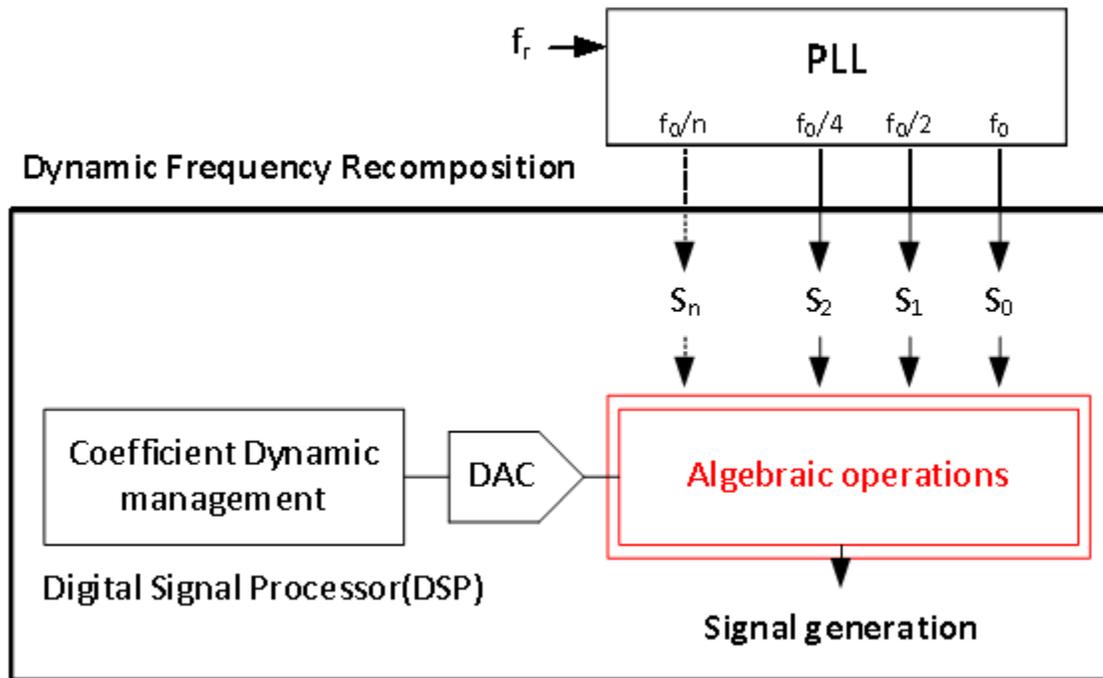


Figure 2-15: Dynamic frequency reconstruction scenario

2.1.2 The Walsh Mathematical Approach:

The previous section showed the interest in using square waves from a PLL for dynamic frequency reconstruction that would ensure:

- less power consumption
- wideband due to the large spectral density of square wave harmonics
- ease of integration (small die area and pressure shifted to digital processing)
- low cost (can be integrated in CMOS technology)

Algebraic manipulations can be used to take advantage of all these assets and to synthesize any kind of signal from a set of square-like waves. A study of the state-of-the-art of digital signal processing suggests the applicability of Walsh transforms, which can generate arbitrary waveforms digitally from square-wave sequences.

2.1.2.1 Background on Walsh Transforms:

The original paper [27], written by J.L. Walsh in 1923 describes the theory of Walsh functions. However, it was not until the article of H.F. Harmuth's [28] in 1968 that significant work on Walsh functions started to appear in the literature. After that, Walsh functions started finding applications in image enhancement, speech processing, pattern recognition, multiplexing [31]–[40] as a new concept of generalized spectral analysis and signal representation. The original goal was to use a transformation to process data faster, while being fairly simple to implement. Such a system which can build up any waveform out of a sum of square waves of some kind would be ideal for use in digital logic. The Walsh transform has emerged as a good candidate to replace the Fourier transform since intuitively the Walsh sequences have wide harmonic content as opposed to Fourier transform. Binary in nature, Walsh transform can be processed by Boolean algorithms and implemented in digital logic, using less storage and processing.

2.1.2.2 The Walsh Series:

The Walsh mathematical approach has demonstrated that from a combination of square-like wave signals as depicted in Fig. 2.4 (more sequences are depicted in Annex A), it is possible to generate any kind of arbitrary waveform. These sequences take values of +1 or -1 on a normalized time interval [0, 1] depending on the range of the desired signal. They are called Walsh sequences and are denoted as $Wal(i, t)$, where i is an integer corresponding to the sequence number and t is a real number representing the time. Some of them have the particularity to be periodic (grey circled curves). They are called the *Primary Walsh Sequences*

and correspond to the Walsh sequences with $i=2^k-1$ and where k is an integer. Note that the frequency of those sequences double each time k is incremented, except for $Wal(0,t)$, which has a value of +1 over the entire time interval. The other sequences result from a recombination of the primary sequences. Note that all the Walsh sequences take +1 as their first values.

All the sequences depicted in Fig. 2.4 have an interesting particularity:

- The blue curves (*withi an odd integer*) are odd, they are called sine Walsh and they are denoted as *Sal*
- The red curves (*withi an even integer*) are even, they are cosine Walsh and are denoted as *Cal*

Sal and *Cal* sequences form an orthonormal basis in \mathcal{R}^2 . Similar to the way a Fourier transform utilizes sine and cosine functions, a Walsh sequence expands a series that allows one to write any signal $x(t)$ as a sum of square-like functions (the Walsh sequences) weighted by the coefficients (a_0, a_p, b_q) which are called the Walsh coefficients.

$$x(t) = a_0 \text{Wal}(0, t) + \sum_{\square}^{M-1} b_q \text{Sal}(m, t) + a_p \text{Cal}(p, t) \quad (2.1)$$

where, $\text{order} = q + p + 1$, with $m, p \in \mathcal{N}$

Depending on the order (M) used to expand the series, there are two cases:

- If the order is even ($q = p$) then the same number of *Cal* and *Sal* function is used
- If the order is odd ($q = p + 1$) then one more *Sal* function is used

Therefore, one can represent any waveform using a family of square-like waves by using its Walsh series decomposition. The accuracy of the Walsh series decomposition depends on:

- **the order (M) used to develop the series i.e. the number n of used Walsh sequences.**
- **the precision on the Walsh coefficients (a_0, a_p, b_q) .**

2.1.3 The Walsh Sequences Synthesis:

There are several methods to build the Walsh sequences. The most efficient approach is to use the Rademacher functions. They are noted $rad(j, t)$, where $j \in \mathcal{N}$. As the *Primary Walsh Sequences*, they are periodic functions that take values of +1 or -1 on a normalized time interval $[0, 1]$. Their frequencies are of the form of:

$$f_n = 2^n \times f_0 \tag{2.2}$$

where, f_0 is the reference frequency and $n \in \mathcal{N}$

Walsh functions can be generated from the Rademacher functions by:

$$Wal(i, t) = \prod_j rad(j, t)^{g_j} \tag{2.3}$$

where, g_j designates a digit getting from the Gray coding of i

As an example, the next steps show how to get the ninth Walsh sequence $Wal(9, t)$:

- Conversion of $(9)_{10}$ to binary $(9)_2 = '1001'$ then to Gray $(9)_g = '1101'$
- Apply the formula of Equation 2.3

$$Wal(9, t) = \prod_j rad(k, t)^{g_j}$$

$$Wal(9, t) = rad(4, t)^1 \times rad(3, t)^1 \times rad(2, t)^0 \times rad(1, t)^1$$

- Draw the sequence (Fig. 2.5)

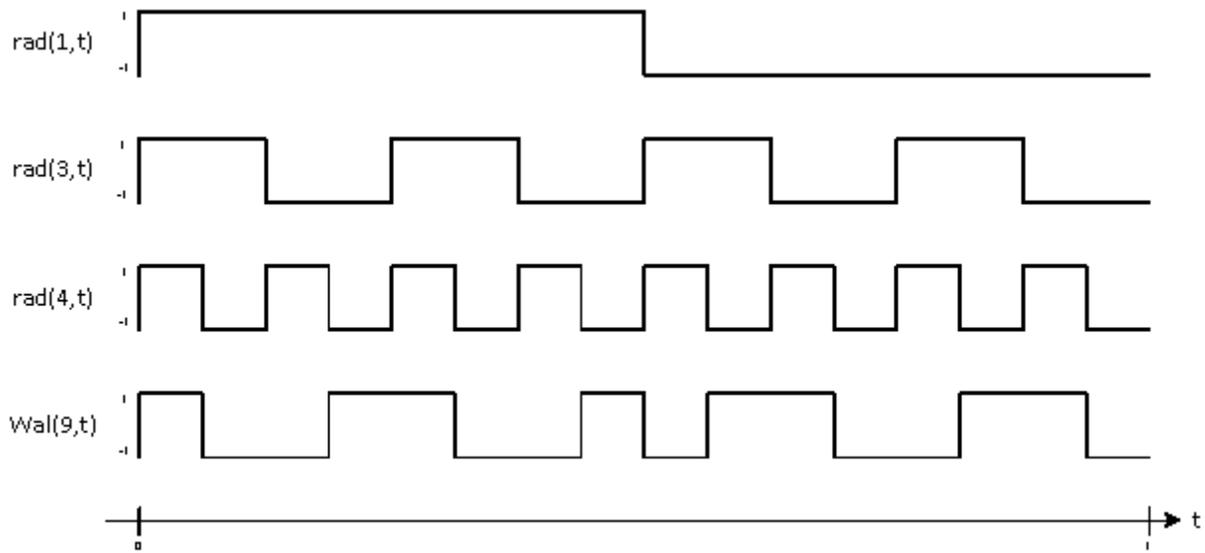


Figure 2-17: Generation of Wal(9,t) starting from Rademacher functions

Moreover, the rules of binary multiplication operation are the same as the XOR operation (whose symbol is \oplus). Therefore, starting from the primary Walsh sequences, it is possible to build the remaining sequences as shown in Table 2.1 (for more sequences building expressions see Annex B).

As all the Walsh sequences take +1 as a first value by definition, the sequences resulting from a combination of an odd number of XOR operations are complemented.

- Thereby, each new XOR combination between the next Walsh primary sequence and the last scheme gives twice more Walsh sequences and increases the order of the Walsh basis by two as well.

This last observation shows how to get a lot of sequences from a few square waves. It predicts that the Walsh transform implementation complexity could be small. Its strong algebraic properties previously announced make it a good candidate to construct any kind of arbitrary waveform from only a few square waves.

To ensure an optimal choice on the order (M) and the resolution of the Walsh coefficients (a_0, a_p, b_q) , the next section comes back to DA conversion theory. It highlights the tradeoff between the resolution and the sampling rate of the Walsh coefficient conversion. This has been described in detail in the next section to determine the system design specification of the Walsh transmitter.

2.2 System Simulation Flow:

In the next section, the system view of the Walsh transmitter is presented. The system simulation flow is described followed by the signal generation process. The simulation results are then compared with the theoretical expectations. Finally, the ability to address concurrent transmission will be assessed through the calculation of the Error Vector Magnitude of a multi-carrier multi-modulated signal.

2.2.1 System Overview:

The previous mathematical approach showed that the Walsh transform can synthesize an arbitrary waveform from only a few square waves. To demonstrate the concept of The Walsh transmitter, a behavioral model of the system was implemented in Matlab. The system is depicted in fig. 2.6., it consists of 3 main blocks:

- a frequency divider that provides j square waves which successively divides the frequency f_0 by 2. These are the Walsh primary sequences
- a Walsh sequence synthesizer builds a $M \cdot 2^j$ order Walsh basis using a combination of the previous j Walsh primary sequences
- a DAC that sums and weighs each Walsh sequence by its associated Walsh coefficient. The construction of the Walsh series is now complete.

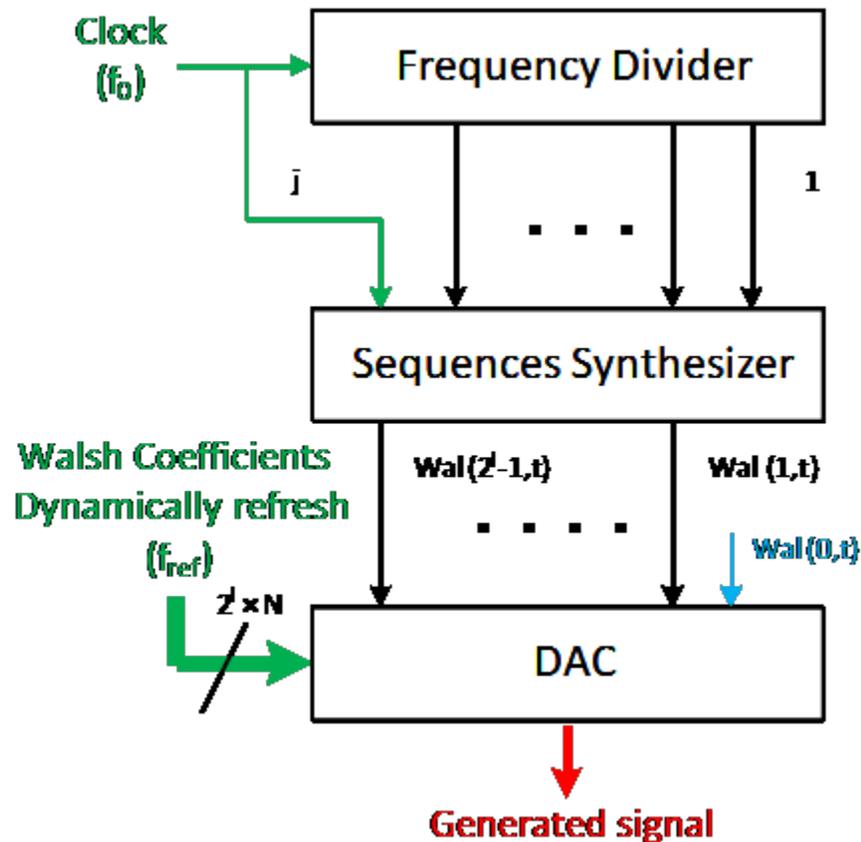


Figure 2-18: The Walsh transmitter synopsis

Many variables are setting the system's performance:

- N is the number of bits used to code the Walsh coefficients

- $f_{ref} = 1/T_{ref}$ is the refresh frequency of the Walsh coefficients with T_{ref} being the size of the time intervals that are defined successively for the Walsh sequences to expand the Walsh series.
- j is the number of primary sequences
- f_0 is the frequency clock. It is also the frequency of the primary Walsh sequence of the highest frequency. Its value should be at least twice the frequency of the synthesized signal. It is correlated to f_{ref} and to the order M as:

$$f_0 = 2^{j-1} \times f_{ref} = \frac{M}{2} \times f_{ref} \quad (2.4)$$

The above parameters help to size and determine the performances of the Walsh transmitter. Following sections illustrate how they can be used in the generation process of the Walsh series approximation. Simulation results are used to match the theoretical expectation. Lastly, trade-offs are made to determine optimized values.

2.2.2 Walsh Series Generation Process:

The system simulations are performed with the aid of digital calculations performed using Matlab software. The signal generation flow consists of four steps described by Fig.2.7.

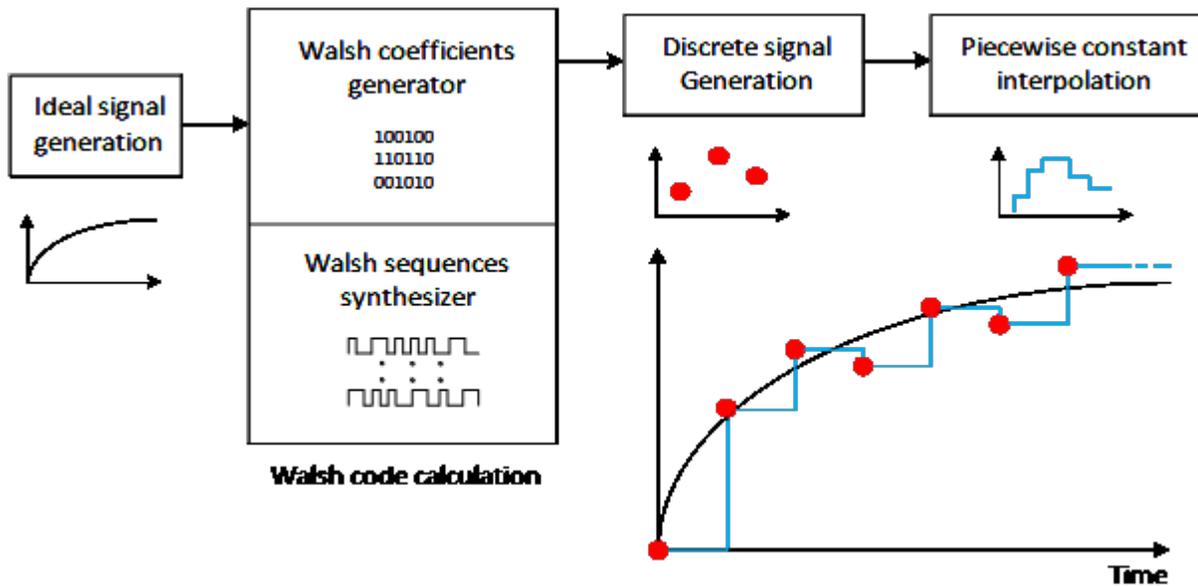


Figure 2-19 : Matlab signal generation

- **Ideal signal generation:** the wanted signal is generated with both a high digital resolution and a short time step. It can be considered as an ideal analog signal.
- **Walsh code calculation:** the Walsh series of the wanted signal is calculated. This block is composed of two sub-blocks. The Walsh coefficients generator generates the Walsh coefficients with a resolution of N bits at the working frequency f_s . While, the Walsh sequences synthesizer, synthesizes the ideal Walsh sequences.
- **Discrete signal generation:** the discrete Walsh series is expanded. It corresponds to the expansion of the individual members of the Walsh series by addition. Each member is the sum of the multiplications of each N -bit coefficients coded by their associated Walsh sequence.
- **Piecewise constant approximation:** it represents the corresponding voltage steps obtained across, say, an output resistive load (in other words, voltage steps are due to ideal current steps similarly to a current steering DAC with a resistor as output load).

This signal generation process allows one to investigate the Walsh transmitter sizing during the construction of the Walsh series. The dimensioning is mainly based on two key parameters: the order M and the number of quantization bit N . The selection of the order is the primary

target of this work since, the order determines the system power consumption as well as the chip size.

Hence, choosing the order before choosing N is advantageous from the system design point of view. In fact, equation (2.1), which governs the signal generation of the Walsh series, can be solely determined by the optimized order using only real values of the coefficients (a_0, a_p, b_q) without having to quantize them. Besides, choosing N before the order limits one from maximizing its value as the Walsh order is not fixed. Moreover, as the formula (2.13) indicates, other parameters are linked to the order value M such as, f_{ref} , f_0 and j (the number of primary Walsh sequences).

2.2.3 Determination of the Optimum Order (M):

The first step is to generate an ideal signal $x\left[\frac{n}{f_s}\right]$. The generated signal is a sinewave sampled at $f_s = 128\text{GHz}$ which is high enough in comparison to the band of interest which is determined by $f_{max} = 4\text{GHz}$. Its frequency f_i is selected such that it is a coherent frequency:

$$\frac{f_i}{f_s} = \frac{M_{cycle}}{N_s} \tag{2.5}$$

Where, N_s is the number of samples and M_{cycle} is the number of cycles in the sampled set. Note that M is required to be a prime number. The value of f_i is chosen using equation (2.5) to be 2.46875GHz. Then the samples of the ideal signal can be written as:

$$x\left[\frac{n}{f_s}\right] = \sin\left(2\pi f_c \frac{n}{f_s}\right) \tag{2.6}$$

After the ideal signal generation, the Walsh sequence synthesis yields a discrete Walsh series (equation 2.7) with the real values of the Walsh coefficients (a_0, a_p, b_q) .

$$x_w\left[\frac{n}{f_s}\right] = a_0 Wal\left(0, \frac{n}{f_s}\right) + \sum_{q=0}^{order-1} b_q Sal\left(q, \frac{n}{f_s}\right) + a_p Cal\left(p, \frac{n}{f_s}\right) \tag{2.7}$$

2.2.3.1 Time-Domain Investigation:

The results depicted in fig. 2.8 illustrate the comparison between the generated ideal signal (in red) and its Walsh series expansion for different values of M

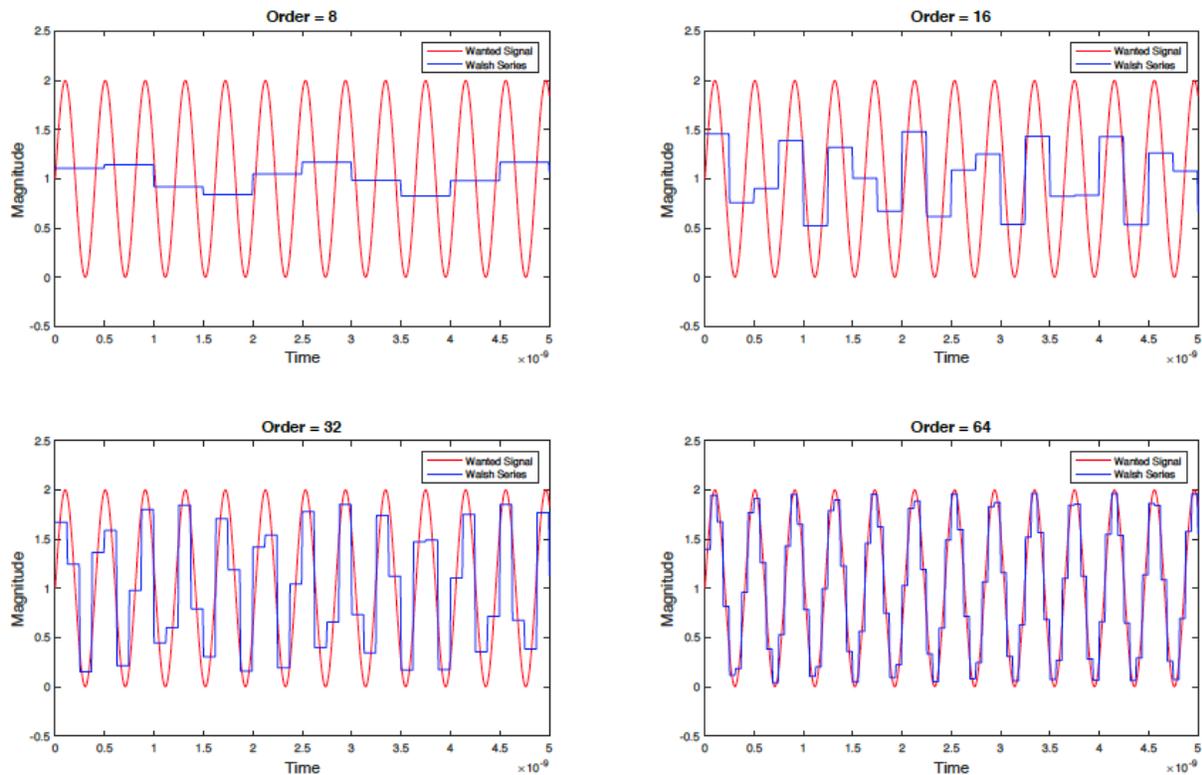
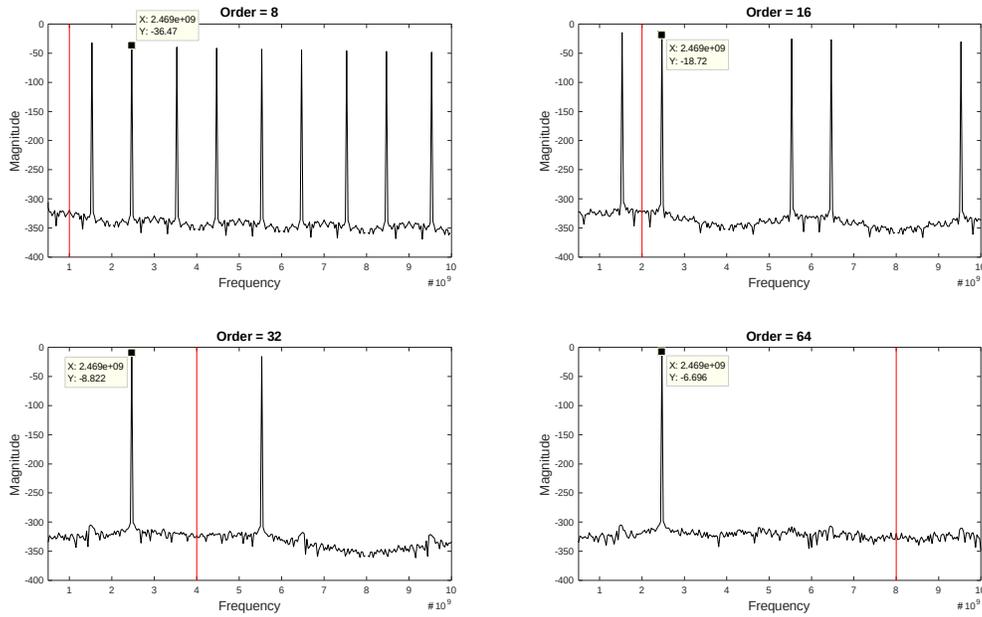


Figure 2-20: Time-domain representation of the Walsh series for different orders

The results highlight how increasing the order can improve the accuracy of Walsh series as the generated signal increasingly resembles the ideal signal and at order 64 it adequately matches the ideal signal since the full signal swing is approximately reached by the series. However, one needs to remember to utilize the minimum possible value M due to the restriction posed by the chip area and the power consumption. On the other hand, for all practical purposes, the signal with $M=32$ seems to provide reasonable accuracy and thus can be considered for an optimized design (see Table 2.2 in the next section). However, the choice between the orders 32 and 64 requires further investigation of the spectra.

2.2.3.2 Frequency-Domain Investigation:

The Fig. 2.9 shows the spectral representation of the Walsh series expansion for different M values. The spectra are obtained for a number of samples $N_s = 4096$. It results in a frequency bin of $f_{bin} = f_s / N_s = 31.25 \text{ MHz}$. The power of the expanded signal is extracted at the frequency 2.46875GHz.



Fig

ure 2-21: Frequency-domain representation of the Walsh series expansion for different orders

The red line represents the highest frequency of the generated *Primary Walsh Sequences* for each of the orders. The highest frequency, which is represented by f_0 in equation (2.13) is analogous to the Nyquist frequency which needs to follow $f_0 \geq 2 \times f_i$ in order to avoid aliasing. As mentioned before, orders 8 and 16 are not relevant for describing an accurate reconstruction of the ideal generated signal. This can also be observed in fig. 2.17 that shows several aliasing harmonics at the frequencies $\pm K f_0 \pm f_i$. Although, the harmonics can be removed using specific filters, the selection of the order can be further narrowed down using *Spurious-Free Dynamic Range* (SFDR) criteria. The SFDR is expressed by the following equation:

$$SFDR_{dBc} = P_s - \max(P_{spur}) \tag{2.8}$$

Where P_s is the power of the input signal and $\max(P_{spur})$ is the power of the highest spur level without considering the power of the aliasing harmonics. Using the above equation, the

SFDRs for all the orders under consideration have been calculated which are summarized in the following table:

Table 2-2: SFDR calculation results for different order

M	8	16	32	64
P_s	-36.5dB	-18.7	-8.8dB	-6.7
$\max(P_{spur})$	-310dB	-310dB	-304dB	-304dB
$SFDR_{dBc}$	273.5dB	291.3dB	295.2dB	297.3db

Based on the calculated figures of the SFDR, one can see that the order 64 provides a better figure of merit. From both the time and frequency domain analyses it seems to be a better choice, but requires greater chip area.

2.2.3.3 Determination of f_{ref} :

Furthermore, one needs to remember that the order value is selected with a particular of f_{ref} governed by equation (2.5). In the following discussion, it has been shown how the value of f_{ref} can impact the Walsh series expansion for a particular order value. To select the order 64 we have used a value of f_{ref} of 250MHz. Now, we will highlight the specific cases for choosing different values of f_{ref} :

- if the f_{ref} is chosen to be 125MHz, to achieve the same performance, i.e., $f_{max} = 4\text{GHz}$, an order $M=128$ can provide the same accuracy of the signal reconstruction. On the downside, selecting an order value as high as 128 will result in a larger circuit size (chip area) and higher power consumption.
- if the f_{ref} is chosen to be 500MHz, to achieve the same performance, an order of 32 will be sufficient. Although it will reduce the circuit size, it will increase the refresh

rate of the Walsh coefficients due to a higher f_{ref} , thereby, causing a drastic increase in power consumption. Besides, selecting an order $M=32$ and f_{ref} of 500MHz will sacrifice the accuracy of the spectral reconstruction of the signal. This is illustrated in fig. 2.10 where we can observe that a higher f_{ref} will result in an increased separation, Δf , between the targeted frequency (f_i) and the synthesized harmonics ($K \times f_{ref}$) as expressed by the following equation:

$$f_i = K \times f_{ref} + \Delta f \tag{2.9}$$

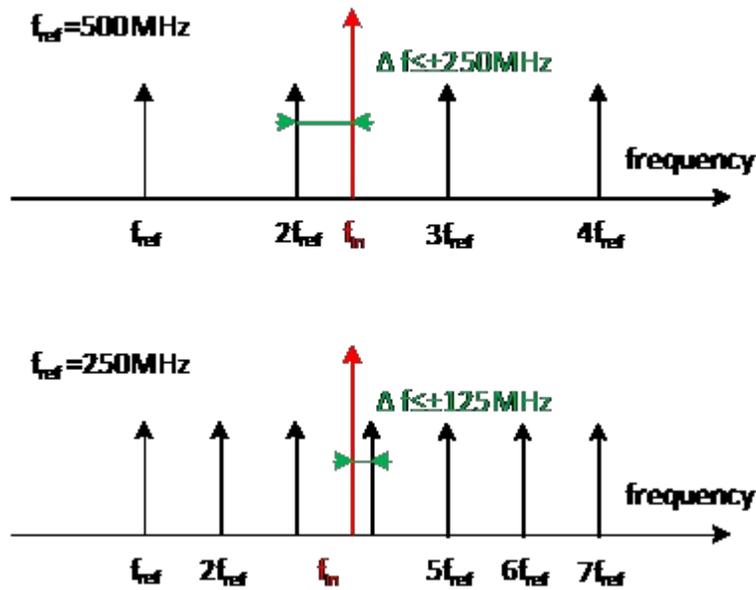


Figure 2-22: Frequency-domain representation of the Walsh series for different orders. Consequently, as Δf increases, the Walsh coefficients have larger amplitude variation, thereby making it more difficult to reconstruct the targeted frequency.

To summarize, we have demonstrated that using an order M of 64 and a f_{ref} of 250MHz provides a reasonable trade-off between the power consumption and the chip area yet preserving the accuracy of the signal reconstruction. This selection will require a value of $j=6$ (number of Walsh primary sequences) following equation (2.5) which leads to a frequency divider size of 5 (5 times division by 2 operations) that starts from a f_0 of 8GHz. This parameter selection can enable signal reconstruction up to a frequency of almost 4GHz.

2.2.4 Determination of the Optimum Resolution (N):

Once the optimum order has been chosen, the optimum resolution needs to be chosen as well.

To determine the resolution of the Walsh coefficients (a_0, a_p, b_q) , first we will discuss the principles of the DA conversion and the theory of quantization noise in the following sections, in order to extract the optimum value of the resolution.

2.2.4.1 D/A Conversion:

The principle of DA conversion relies on representing the magnitude of an analog signal V_{out} as a unique combination of N binary digits which can be represented mathematically as:

$$V_{out} = (V_{FS} - V_0) \times \left(b_1 2^{-1} + b_2 2^{-2} + \dots + b_N 2^{-N} \right) \quad (2.10)$$

Where V_{FS} is the full-scale voltage and V_0 is the reference voltage.

Equation (2.10) highlights that an analog signal can be represented by an infinite number of bits (N). The accuracy of the quantized signal depends on the resolution N, i.e. as N increases, the accuracy of the quantized signal increases, which comes at the cost of bit word size that represents the analog signal. Hence, the next section discusses the required quantization level that determines the accuracy of the DA conversion.

2.2.4.2 Quantization Noise:

Although an ideal DA conversion will have the highest accuracy for an infinite number of bits, from a practical point of view it is not feasible to design a system having a very high order of N since it complicates the design of the DAC significantly. Not only it will consume more power, but it will also require a higher chip area. Therefore, a trade-off needs to be made between accuracy of the D/A conversion and the number of quantization bits. However, this trade-off will cause an error between the actual value of the analog signal and its corresponding encoded value. This quantization error can be modeled as additive noise to an ideal analog signal out of the DA. The typical figure of merit of this error is the *Signal Quantization Noise Ratio* (SQNR) which represents the quality of the signal coming out of the DA. It is expressed as the ratio between the power of the useful signal P_s and the integrated power of the quantization noise P_n . For sine wave signal, it is equal to:

$$SQNR_{dB} = 10 \log_{10} \left(\frac{P_s}{P_n} \right) = 6.02 \times N + 1.76 \quad (2.11)$$

2.2.4.3 SQNR Calculation:

Time-Domain:

From a temporal point of view Fig. 2.11, the SQNR represents the quantization noise derived from the Walsh coefficient binary coding. It reflects the cumulated error between the temporal representation of the wanted signal x and the Walsh approximated signal x_w .

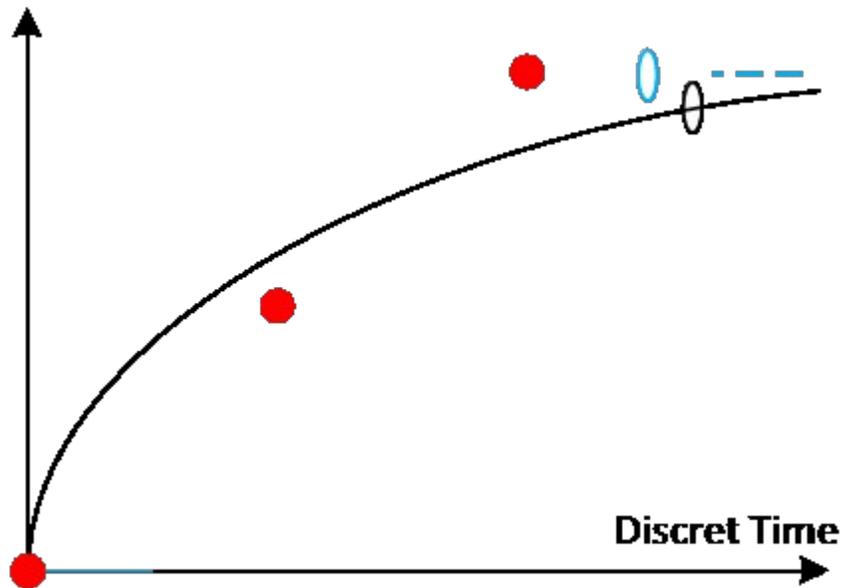


Figure 2-23: Discrete time-domain representation of the approximation error

Since, the Walsh coefficients are weighing the Walsh sequences, their quantization is made at the same frequency as the highest frequency of the Walsh sequences (f_0). Therefore, only

the $x\left[\frac{n}{f_0}\right]$ samples of the ideal signal are taken into account to determine the error between

the discrete Walsh series representation (equation 2.12) and the ideal signal (equation 2.13):

$$x_w\left[\frac{n}{f_0}\right] = a_0 Wal\left(0, \frac{n}{f_0}\right) + \sum_{q=1}^{M-1} b_q Sal\left(q, \frac{n}{f_0}\right) + a_p Cal\left(p, \frac{n}{f_0}\right) \quad (2.12)$$

$$x\left[\frac{n}{f_0}\right] = \sin\left(2\pi f_i \frac{n}{f_0}\right) \quad (2.13)$$

Then the power of the noise is expressed as the sum of the samples $e[n]$ which is the difference between the samples of the ideal signal and its Walsh approximation.

$$P_n = \frac{1}{n} \sum_n e \left[\frac{n}{f_0} \right] = \frac{1}{n} \sum_n \left(x \left[\frac{n}{f_0} \right] - x_w \left[\frac{n}{f_0} \right] \right)^2 \quad (2.14)$$

This leads to the following equation of the SQNR:

$$SQNR_{dB} = 10 \log_{10} \left(\frac{P_i}{P_n} \right) = 10 \log_{10} \left(\frac{\sum_n \left(x \left[\frac{n}{f_0} \right] \right)^2}{\sum_k \left(x \left[\frac{n}{f_0} \right] - x_w \left[\frac{n}{f_0} \right] \right)^2} \right) \quad (2.15)$$

The above equation allows one to calculate the noise over the entire spectrum. But it does not provide information about the amount of noise in the working band $f_{max} = 4GHz$. Only the SQNR calculations in the frequency-domain allow us to get rid of the noise from the outside of the band of interest.

Frequency-Domain:

To calculate the SQNR in the frequency domain, it is necessary to go from the temporal form of the Walsh approximation to its frequency form using the Fourier transform. The Walsh

approximation $x_w \left[\frac{n}{f_0} \right]$, being in sample time, a *Discrete Fourier Transform* (DFT) must be applied to obtain frequency samples which will have the form:

$$X_w \left[\frac{k}{f_0} \right] = DFT \left(x_w \left[\frac{n}{f_0} \right] \right) = \sum_{k=0}^{N_s-1} x_w \left[\frac{n}{f_0} \right] e^{\frac{-2j\pi nk}{N_s}} \quad (2.16)$$

The SQNR can be calculated from the samples using the Parseval theorem which states that the energy of a signal does not depend on its representative form (in time or frequency):

$$\sum_{n=1}^{N_s-1} \left| x_w \left[\frac{n}{f_0} \right] \right|^2 = \sum_{n=1}^{N_s-1} \left| X_w \left[\frac{k}{f_0} \right] \right|^2 \quad (2.17)$$

The SQNR of the Walsh approximated signal can thus be calculated as the Signal to Noise Ratio (there is not additive noise to the quantization noise) which is the PSD at the fundamental frequency P_i divided by the PSD at all the other frequencies which is the total noise power P_n :

$$SQNR_{dB} = SNR_{dB} = 10 \log_{10} \left(\frac{P_i}{P_n} \right) = 10 \log_{10} \left(\frac{\left| X_w \left[\frac{k}{f_0} \right] / f_i \right|^2}{\sum_{k/f_i} \left| X_w \left[\frac{k}{f_0} \right] \right|^2} \right) \quad (2.18)$$

The calculation of SQNR in its frequency form provides insight into the quantization noise of the DA conversion coefficients of the Walsh series within the useful band of the signal (Fig. 2.12).

Therefore, for a frequency fin carrying data over the bandwidth BW_{ch} , the contribution of the noise coming from the D/A conversion errors can be calculated by summing the samples of the

$$\text{interval} \left[f_i - \frac{1}{2} BW_{ch}, f_i + \frac{1}{2} BW_{ch} \right]$$

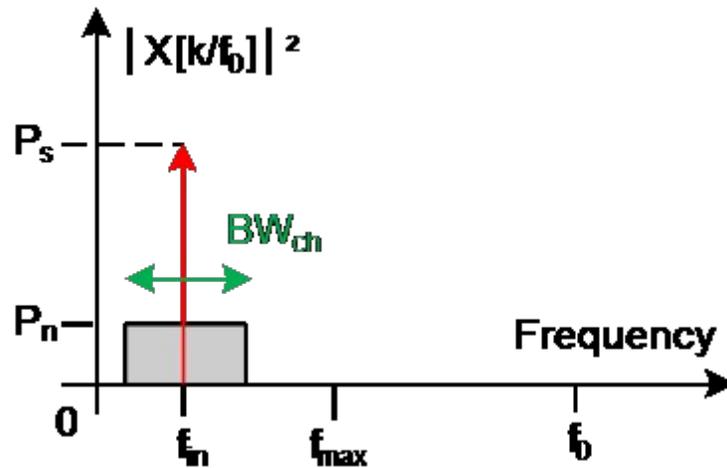


Figure 2-24: Spectral representation of quantized sine wave at frequency f_i

As can be noticed from the figure above, only the quantization noise, in the useful signal band

BW_{ch} , is likely to alter the information in the interval $\left[f_i - \frac{1}{2} BW_{ch}, f_i + \frac{1}{2} BW_{ch} \right]$.

In this work, the value of this working band BW_{ch} has been set at 100MHz and the SQNR was calculated by simulation. The results for different order of quantification (N) are presented in the following figure:

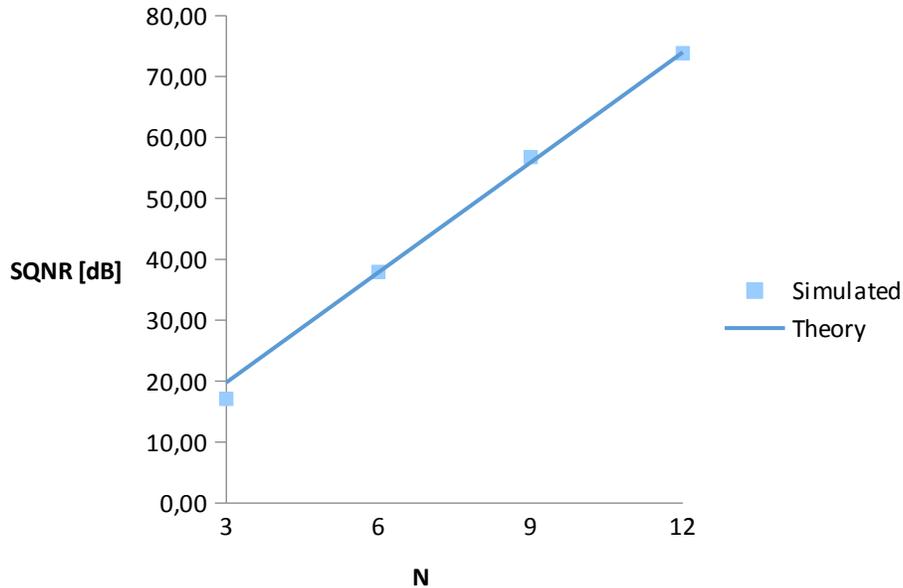


Figure 2-25: SQNR of the Walsh conversion versus N

In the figure above, simulation results are shown using symbols while the theoretical value expressed by the equation (2.11) appears as the blue straight line. As observed from the results, we note that the SQNR increases by 6.02 dB whenever the DA conversion resolution (N) of the Walsh coefficients increases by one bit. This behavior is similar to the behavior of a Nyquist DAC sampled at a frequency $f_0 = 8\text{GHz}$. In this work, the number of quantization bits has been fixed at 6. This ensures an optimum quantization level with the fundamental SQNR being 40dB above the quantization noise floor yet consuming less power for silicon based circuits.

The Walsh transmitter can generate a signal with a frequency not exceeding 4GHz that can operate in a frequency band of 100MHz. This can be done using a Walsh series with 64 Walsh sequences and by encoding the Walsh coefficients with 6 bit of quantization. Furthermore, to show that this algorithm can generate signals with multiple modulated carriers, the next section will present the results for a concurrent transmission signal.

2.3 Concurrent Transmission:

To demonstrate the feasibility of a concurrent signal transmission, an approach is proposed to generate a signal having 3 CC using the Walsh algorithm.

2.3.1 Three CC Signal Synthesis:

The ideal signal generated using Matlab is a multi-modulated signal where the modulation process consists of 3 schemes with random bit stream at different speeds:

- a *Quadrature Phase-Shift Keying* (QPSK) modulation scheme with a DR of 25MBps at a CC frequency of 3.58GHz
- a 16 *Quadrature Amplitude Modulation* (QAM) with a DR of 10MBps at a CC frequency of 2.31GHz
- a 64-QAM modulation with a DR of 10MBps at a CC frequency of 2.33GHz

The signal obtained by following the generation steps using the Walsh algorithm (with $order=64$ and $N=6$) is represented by the spectrum in the following figure:

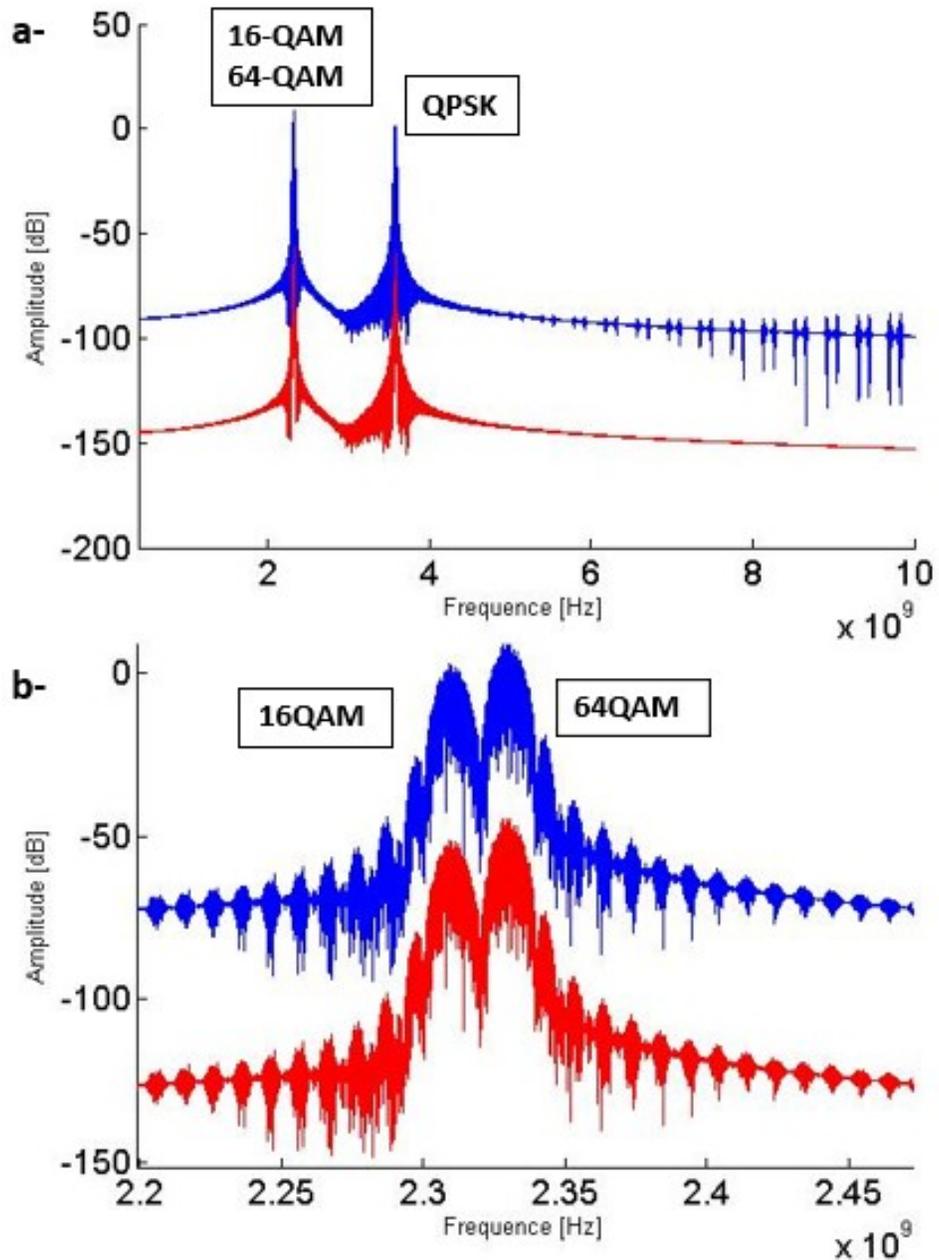


Figure 2-26: a- Spectrum obtained with 3 CC aggregation, b- zoom on the QAMs

In the Fig. 2.14-a, we observe the three CC carrier signals which have the right carrier frequencies (Fig. 2.14-b). But the signal have different powers. This is due to the fact that the DR and modulation levels are different which results in different bandwidths for each Carrier Component (i.e. carrier BW = BW/ (modulation order)).

From the above, we concluded that the modulated carriers had the correct center frequencies. We will next verify that the information is carried accurately as well.

2.3.2 Error Vector Magnitude (EVM) Calculation:

To calculate the EVM, the ideal signal generated using Matlab, which includes 300 16QAM, 200 64QAM and 900 QPSK symbols, is implemented in this simulation tool. At the end of the Walsh generation process, the Walsh approximation is demodulated in the bit streams that are represented in the following figure:

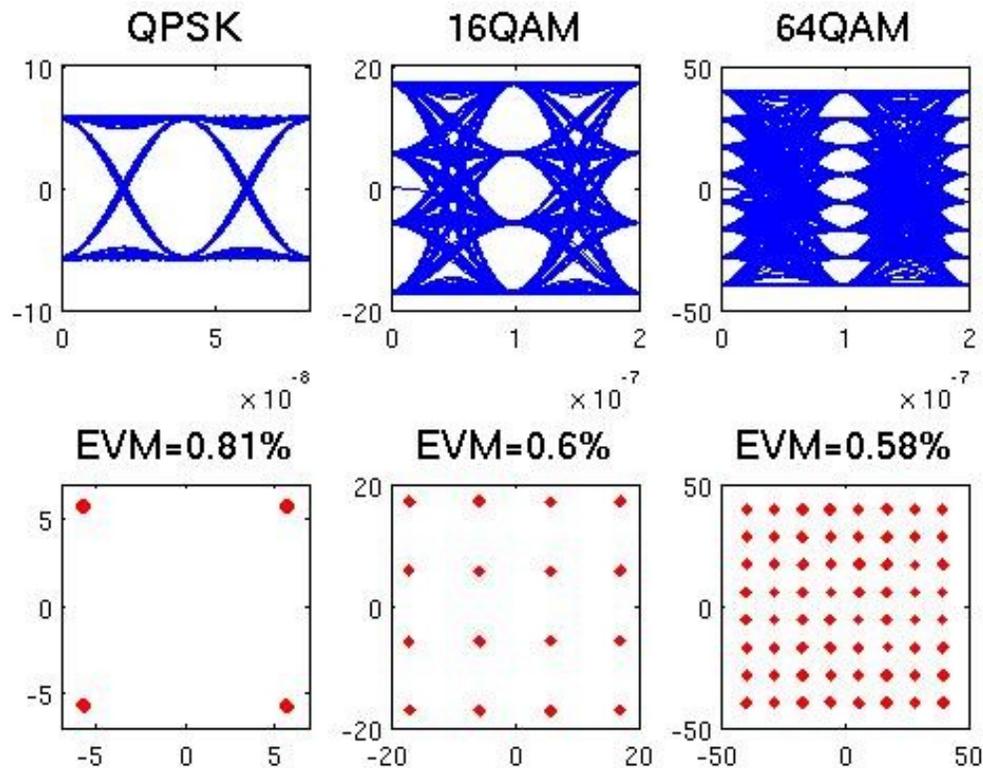


Figure 2-27: Eye and constellation diagrams resulting of 3 CC aggregation

The bit stream bit shows a large eye opening for each of the modulations. Besides, distinct constellations are observed and their corresponding EVMs [42] are calculated according to

equation 2.19, where P_{ref} is defined as the average reference power of the constellation and

P_{error} is the *Root Mean Square* (RMS) error in the power.

$$EVM = \sqrt{\frac{P_{error}}{P_{ref}}} \times 100 \quad (2.19)$$

EVMs for each of the modulation schemes are less than 1%. The calculated values are reported in the following table:

Table 2-3: EVM calculation results for different modulation schemes (M=64 / N=6)

Modulation scheme	QPSK	16-QAM	64-QAM
f_{cc}	2.5 GHZ	2.7 GHz	2.9 GHz
DR	25 MBps	10 MBps	10 MBps
EVM	0.81 %	0.6 %	0.58 %

Thus, the validity of the behavioral architecture of the Walsh transmitter has been demonstrated. It can digitally generate multi-carrier multi-modulated signal up to a bandwidth of almost 4GHz.

2.4 Conclusion:

The theory of Walsh algorithm can be used to develop a series that allows one to represent any type of signal as a combination of square-wave signals. A Walsh based transmitter was Matlab coded. The system simulation results demonstrated that this algorithm can synthesize signals with several modulated carriers. The proposed system has been optimized for input signals approaching a frequency of 4GHz and having a bandwidth of 100MHz. An EVM of less than 1% and a SQNR of 40dB have been obtained for the following values of the key parameters:

- the number of primary sequence is $j=6$
- the coefficients refresh rate $f_{ref}=250\text{ MHz}$
- the frequency clock is $f_0=8\text{ GHz}$
- the number of quantization bits is $N=6$



Design

3.

Contents

3.1 Technological Considerations and Design Flow

3.1.1 The CMOS 28nm FDSOI Technology

3.1.2 The Design Flow

3.2 The Walsh Sequences Synthesizer

3.2.1 The Frequency Divider

3.2.2 The Walsh Generator

3.3 The DAC

3.3.1 The Driver

3.3.2 The Current Sources

3.3.3 The DAC Design

3.3.3.1 The DAC Unit Cell

3.3.3.2 The 6-bit DAC

3.3.3.3 The Whole DAC

3.4 The Walsh Coefficient Conversion Interface

3.4.1 The SRAM

3.4.2 The SPI

3.4.3 The Walsh Coefficients Addressing

3.5 Conclusion

Chapter 3 presents the design of the Walsh transmitter in the 28 nm FDSOI CMOS technology from ST-Microelectronics. The design of the Walsh transmitter is described starting from the architecture to the transistor level implementation. Top level schematic simulation results are checked to assess the performances in terms of area and power consumption.

Keywords: Circuit design, FDSOI, RF-DAC, SPI, SRAM

3.1 Technological Considerations and Design Flow:

In comparison with other technologies, the integration of the Walsh transmitter in 28 nm FDSOI CMOS technology, takes advantage of using both small and fast transistors. Thus, in front of the stringent specifications imposed on our system, this technology is an asset to design an architecture presenting both low power consumption and small chip area.

3.1.1 The CMOS 28nm FDSOI Technology:

In FDSOI technology the transistor is controlled through its gate and its substrate polarization. It integrates a special transistor architecture (Fig. 3.1), which provides a much more efficient substrate biasing technique than the other technologies.

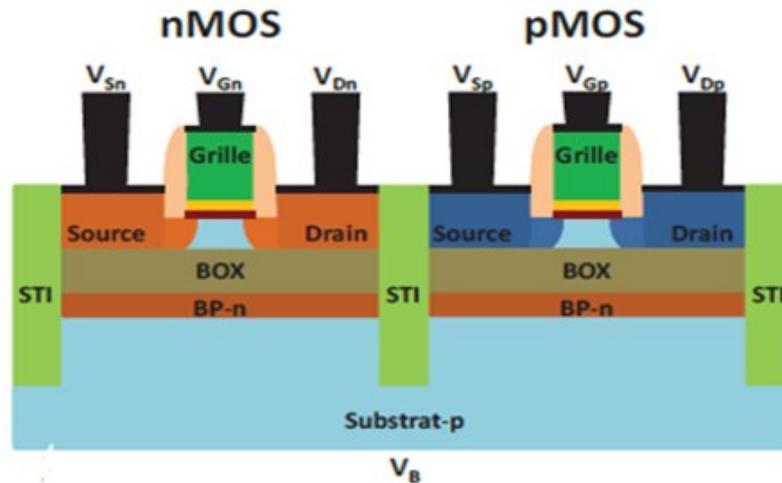


Figure 3-28: FDSOI NMOS and PMOS cutting view [43]

Indeed, as shown in the figure above, an additional fine layer of doping called *Back Plane* (BP) is buried under the *Buried OXide* (BOX) layer. It is doped complementarily to the doping of the source and the drain allowing then a better control of the electrostatic fields generated in the transistor channel. It is therefore possible with this technology to adjust the threshold voltage (V_{th}) of the transistor. This feature is the key point of the FDSOI technology. It offers both the opportunity to control with more flexibility the leakage currents and the possibility to increase the transistor speed.

The BP integration under the BOX can be used as a second gate which V_{bp} polarization acts on the electrical characteristics of the transistor. By applying a V_{bs} voltage between the BP and the transistor source, it is possible to:

- reduce the leakage current I_{off} while increasing V_{th} by applying $V_{bs} < 0$ for NMOS and $V_{bs} > 0$ for PMOS. It is the *Reverse Back Biasing* (RBB).
- increase the speed of the transistor by increasing the drain / source current. This is made possible by placing the transistor in strong inversion regime by applying $V_{bs} > 0$ for a NMOS and $V_{bs} < 0$ for a PMOS. It is the *Forward Back Biasing* (FBB).

The FDSOI technology achieves at a low voltage ($\sim 0.2V_{ds}$) higher performance (high speed and high drain / source current) while assuming greater energy efficiency than the CMOS Bulk technology.

3.1.2 Design Flow:

The architecture of the Walsh transmitter was built using 28nm FDSOI CMOS of ST-Microelectronics. The sizing of the system has been optimized according to the performance of this technology for the following parameters:

- the number N of N-bits coded Walsh coefficients is 6,
- the frequency f_{ref} of the Walsh coefficients refresh is 250MHz,
- the frequency f_0 of the samples is 8GHz,
- the number M of Walsh sequences is 64.

The key parameters in the design are highlighted in Fig. 3.2. It represents the top level features of the proposed Walsh transmitter for an input RF signal with frequency f_0 of 8GHz and a serial data input corresponding to bits of 64 encoded Walsh coefficients following the generation process of the Walsh series mentioned in chapter 2.

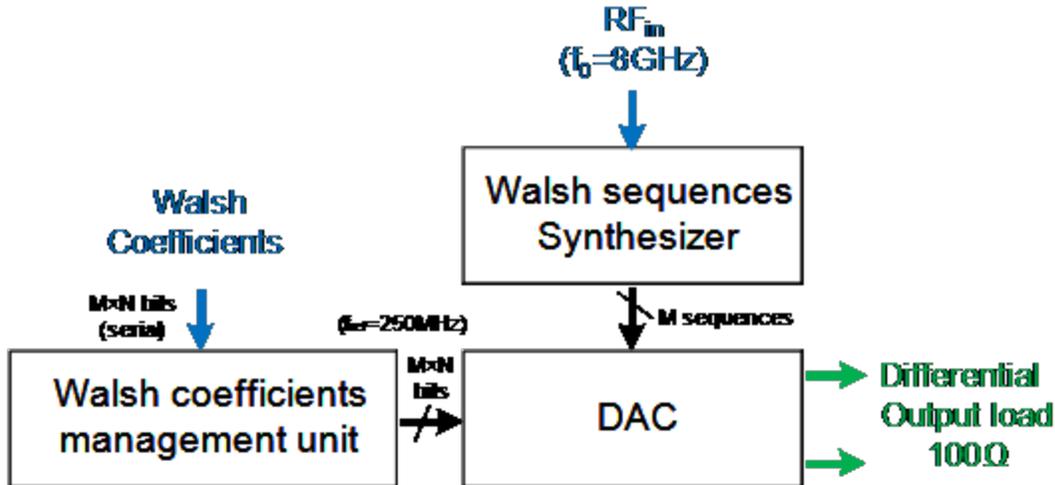


Figure 3-29: The Walsh transmitter block diagram ($M=64/N=6$)

This architecture consists of three main blocks:

- The Walsh coefficients management unit allows to parallelize the 6-bit coded Walsh coefficients produced in serial form by the synthesis of the Walsh series using the Matlab generation process,
- The synthesizer of Walsh sequences allows to synthesize 64 Walsh sequences from the input sinewave signal, necessary for the expansion of the Walsh series corresponding to the desired signal to order 64,
- The DAC will reconstruct the Walsh series weighting in the first 64 sequences from the synthesizer using 64 Walsh coefficients with 6-bits followed by summing each member of the product thus obtained.

The design of the Walsh transmitter is presented using a top-down approach ranging from the functional level to the logic level and ultimately to the transistor level. For each block the design has been optimized based on simulations using Spectre RF from Cadence. The results show the expected behavior for each of the features related to each of the blocks. Finally, the overall architecture of the Walsh transmitter was simulated to demonstrate its feasibility.

3.2 The Walsh Sequences Synthesizer:

The Walsh sequences synthesizer (Fig. 3.3) allows from a sinusoidal RF signal to generate the Walsh sequences necessary for the reconstruction of the Walsh series of order 64.

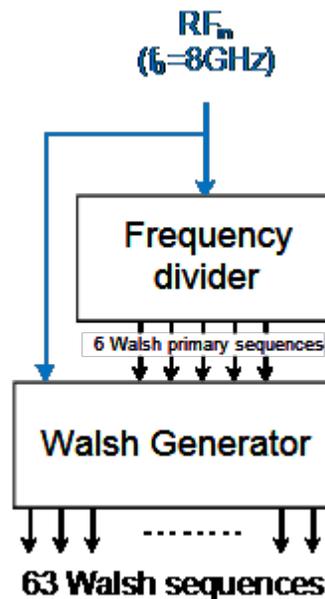


Figure 3-30: The Walsh sequences synthesizer

As can be observed in the figure above, this block is composed of two subsystems:

- a frequency divider that delivers 6 primary sequences (including the input frequency) from an input signal of 8GHz
- a logic block that synthesizes from these 6 primary sequences 2^6 i.e. 64 sequences necessary for the development of the Walsh series of order 64.

3.2.1 The Frequency Divider:

The frequency divider (Fig. 3.4) is one of the most critical parts of the sequence synthesizer. The accuracy of the Walsh sequences as well as the signal reconstruction by the series will depend on it.

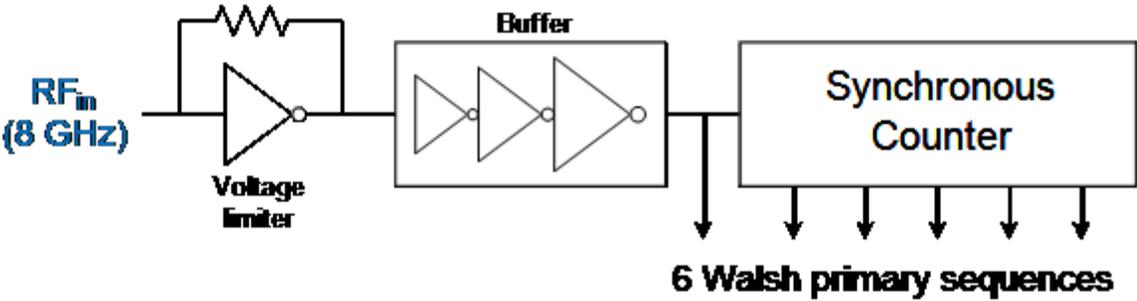


Figure 3-31: The frequency divider

Since the frequency divider is the part of the circuit that will be first given an external signal to the chip, it is necessary to take precautions in order to protect the circuit from potential voltage overshoots.

3.2.1.1 The Voltage Limiter:

To make sure that the input signal has a constant magnitude $V_i=1V$, a voltage limiter followed by a buffer (Fig. 3.5) has been integrated before the input of the frequency divider.

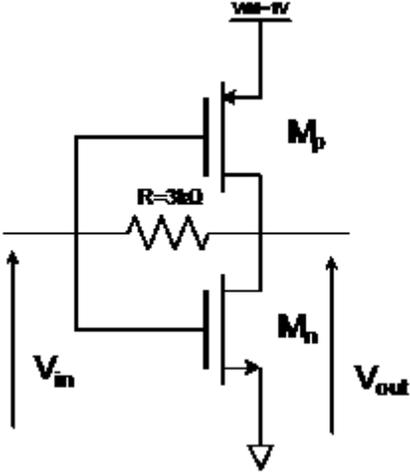


Figure 3-32: The voltage limiter

The voltage limiter of the above figure is composed of an inverter repowered through a resistance R of $3k\Omega$. The transistors M_n and M_p were sized so as to ensure the same rise and fall times to the output of the inverter and, in accordance with the following equation:

$$\frac{W_p}{L_p} = \frac{\mu_n}{\mu_p} \times \frac{W_n}{L_n} \tag{3.1}$$

where, μ_n and μ_p are respectively the mobility of the electrons and the holes

For ensuring a minimum gate length of the transistors ($L_n = L_p = 45nm$), the gate dimensions were thus cut to ($W_n = 0.57\mu m$ and $W_p = 1.2\mu m$). The circuit of Fig. 3.6 was simulated for different values of the amplitude (1V, 1.2V and 1.5V) of a sinusoidal input signal

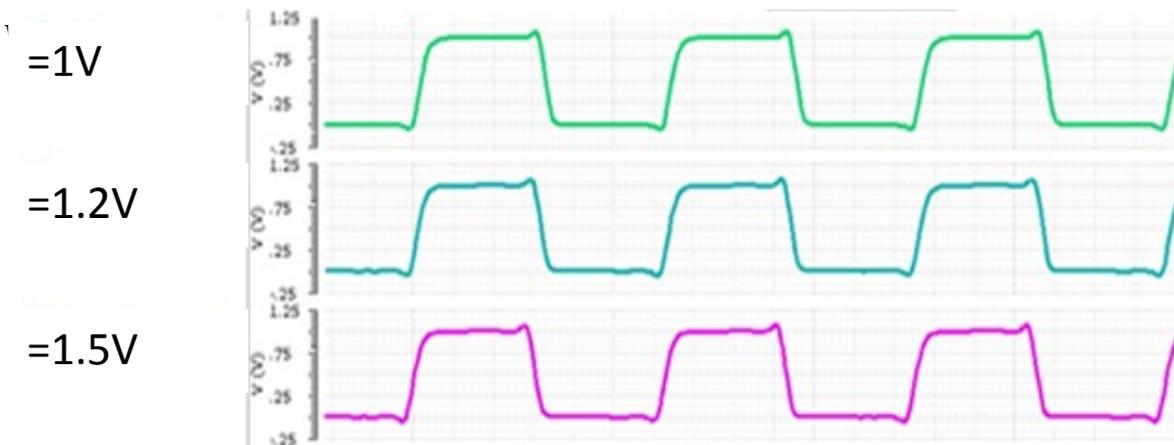


Figure 3-33: Output of the voltage limiter for different input voltage values
 For each of the input amplitudes, the output voltage is 1V and the rise and fall times do not exceed 12ps (representing less than 10% of the value of the period of the input signal 125ps).
 The time durations at logic level '1' and '0' are presented in the following table:

Table 3-1: Evolution of the time duration of the logical values at the output of the Voltage limiter in function of the input magnitude

V_i magnitude	Time duration of a logical '1'	Time duration of a logical '0'
1v	62.45ps	62.55ps

1.2V	61.13ps	63.87ps
1.5V	60.32ps	64.68ps

In light of these results, it appears that for voltage levels exceeding 1V of the input voltage, the output signal does not have the same slew rates at the rising/falling edges. A buffer has been added to relay the signal, while giving it enough slew rate to be applied to the frequency divider.

3.2.1.2 The Synchronous Counter:

The frequency divider generates the 6 primary Walsh sequences (which are periodic square waves whose frequency values are shown in Fig. 3.7) starting from the outgoing signal of the square-wave voltage limiter.

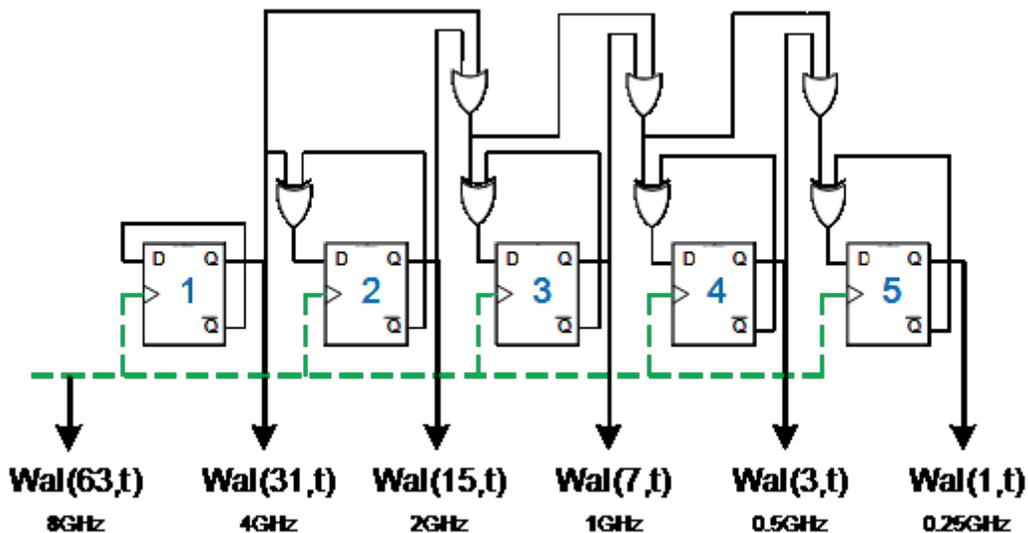


Figure 3-34: Frequency divider schematic

Since the input frequency is 8GHz, the chosen architecture is a synchronous counter. It will limit the time offsets between primary Walsh sequences that are available at the output of the divider.

The divider has been implemented using standard D flip-flop cells of the bookstore *Design Kit* (DK) from the CMOS 28nm FDSOI inventory of STMicroelectronics. Simulations were conducted on the entire set: voltage limiter, buffer and frequency divider, applying a sinusoidal signal

V_i of 2V / 8GHz at the voltage limiter input. The choice of these cells was optimized with capacitive loads of 10fF for each divider. The outputs are shown in the following figure:

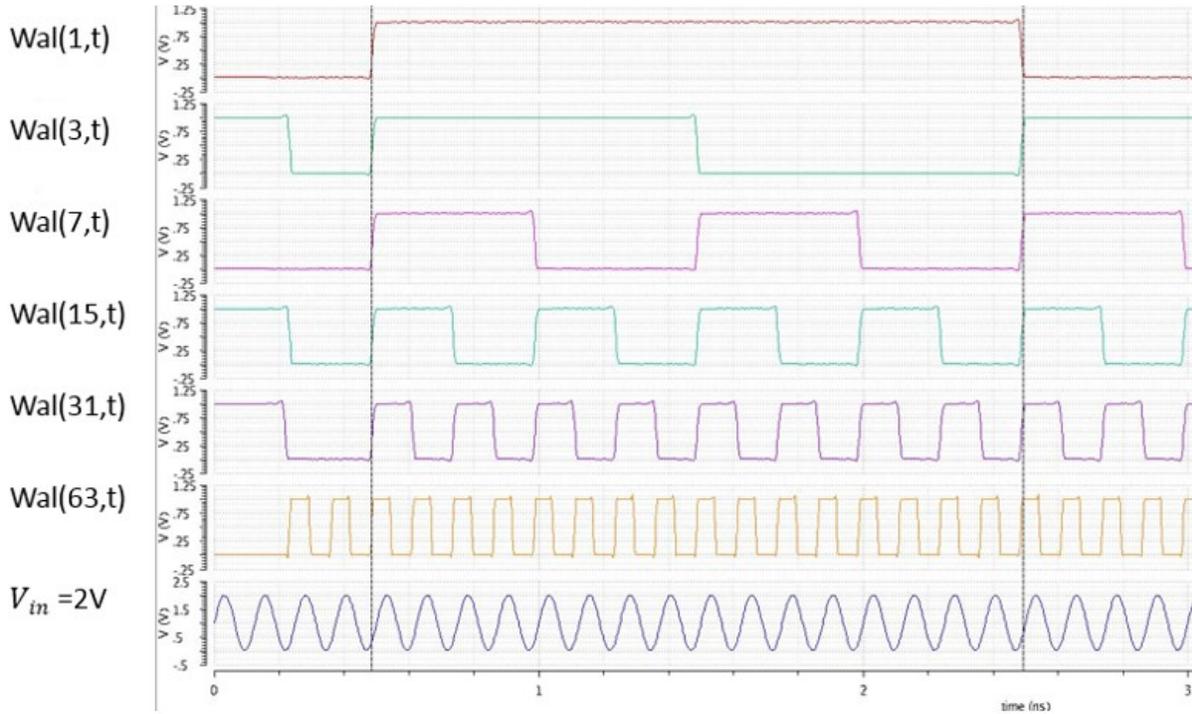


Figure 3-35: Full frequency divider simulation results

In Fig. 3.8, the 6 primary Walsh sequences are sorted from top to bottom in increasing order of their frequencies. The first curve represents the Walsh sequence and the lower frequency (250MHz) is the refresh rate of the coefficients f_{ref} . The penultimate waveform is the Walsh sequence of the fastest frequency which is the system clock, f_0 . The bottom blue curve represents the input signal applied to the chip. All the sequences show a rise / fall time of 13ps and are synchronous.

From these 6 sequences described in Fig. 3.3, one needs to generate the primary Walsh sequences of the order 64, i.e., to synthesize $2^6 = 64$ Walsh sequences. This is where the logic of constructing Walsh sequences mentioned in Table 2.1 of the previous chapter comes into play.

3.2.2 The Walsh Generator:

The Walsh generator (Fig. 3.8) synthesizes 64 sequences, apart from the zero order sequence ($Wal(0,t)$), which is directly taken from the power supply rail.

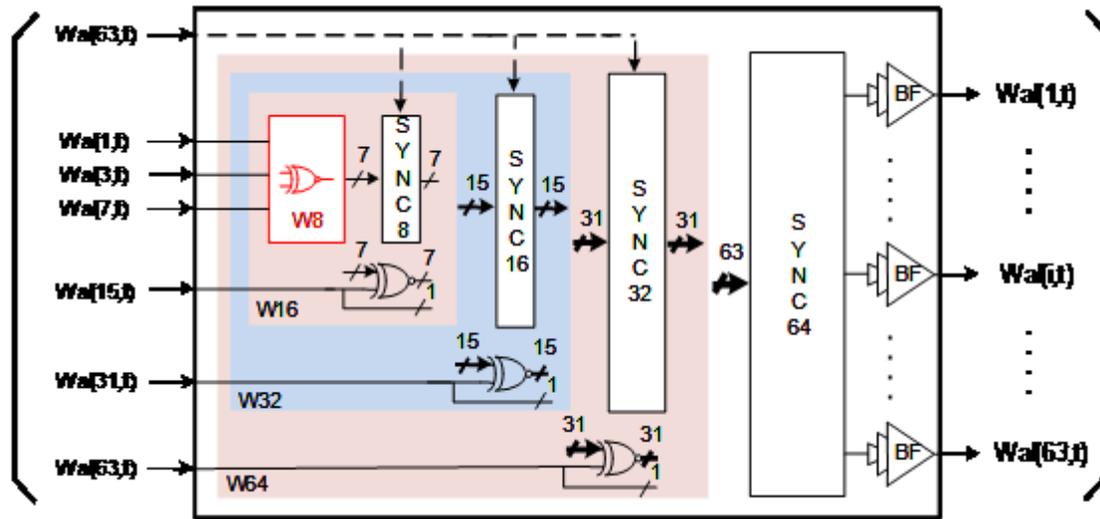


Figure 3-36: The Walsh generator architecture

The Fig. 3.9, shows the recursive nature of the instantiation of the Walsh generator:

- beginning from the architecture of the order 8 Walsh generator (Fig. 3,10), we have 7 sequences ($Wal(1,t)$ to $Wal(7,t)$),
- then, a D-latch array is added to synchronize these sequences with the sequence $Wal(63,t)$, which is the sequence of highest frequency,
- thus, these 7 outgoing synchronized sequences are combined with the primary Walsh sequence which has the next highest frequency $Wal(15,t)$,
- so, we get 15 sequences ($Wal(1,t)$ to $Wal(15,t)$),

- again, an another D-latch array is added to synchronize these sequences with the sequence $Wal(63, t)$,
- and so on, we get 64 sequences,

Finally, at the output, buffers are required to ensure a slew rate of 12.5ps, which is 10% of the value of the period of the fastest Walsh sequence.

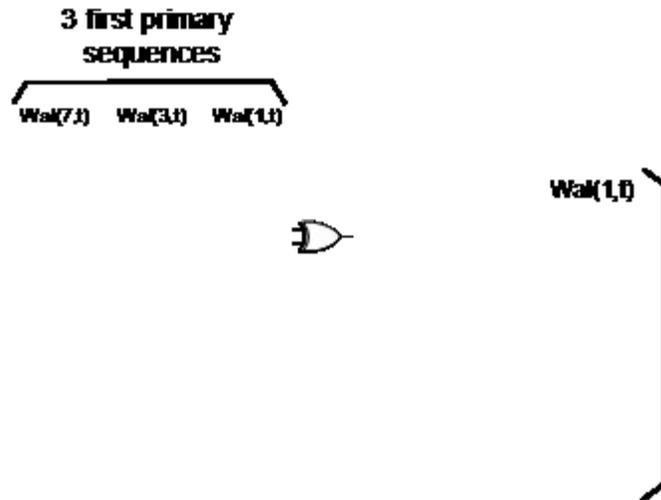


Figure 3-37: Architecture of the order 8 Walsh generator

The waveforms have been obtained after simulating the sequence synthesizer. Some of these sequences $(Wal(6,19,33,49,63, t))$ are shown from top to bottom in the curves of Fig 3.11.

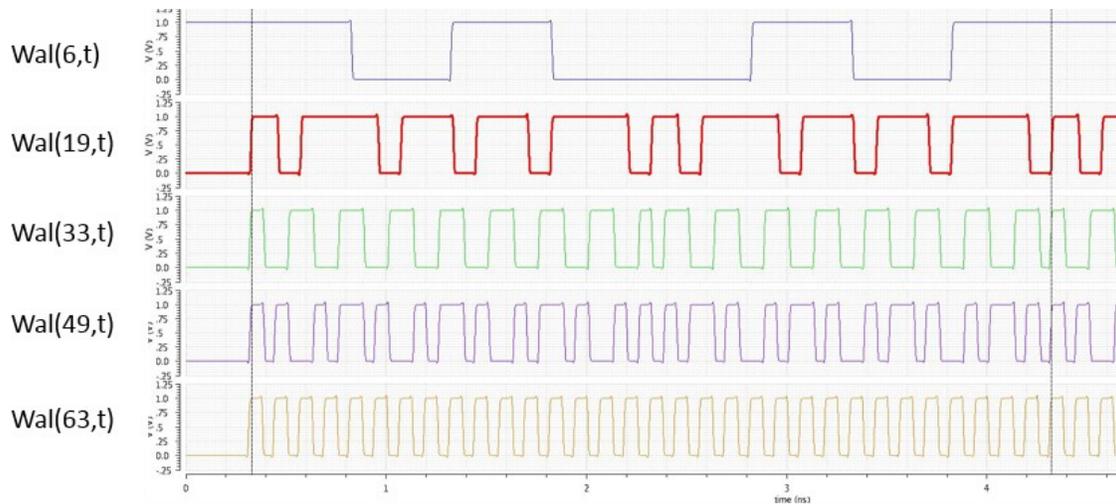


Figure 3-38: Some sequences at the output of the sequence synthesizer

Each output has been charged with a capacitor of 10 fF. At its input, the circuit had 6 primary sequences obtained previously and with rise / fall times of 13ps. The sequences obtained are synchronous and have a rise / fall time of ≈ 15 ps.

As mentioned in the Walsh algorithm (Equation 2.1), the next step is to reconstruct the desired signal by developing a Walsh series form of order 64. Thus, the sequences are weighted and summed to current levels corresponding to discrete values of 64 Walsh coefficients with 6-bits coding. Their passage into a 100Ω differential load will deliver an analog signal which is the Walsh approximation of the signal to be reconstructed.

3.3 The DAC:

The DAC is a differential structure and is composed of 64 cells of 6-bits DAC controlled by the previously generated Walsh sequences by the drivers. It supplies current steps into a differential load (Fig. 3.12).

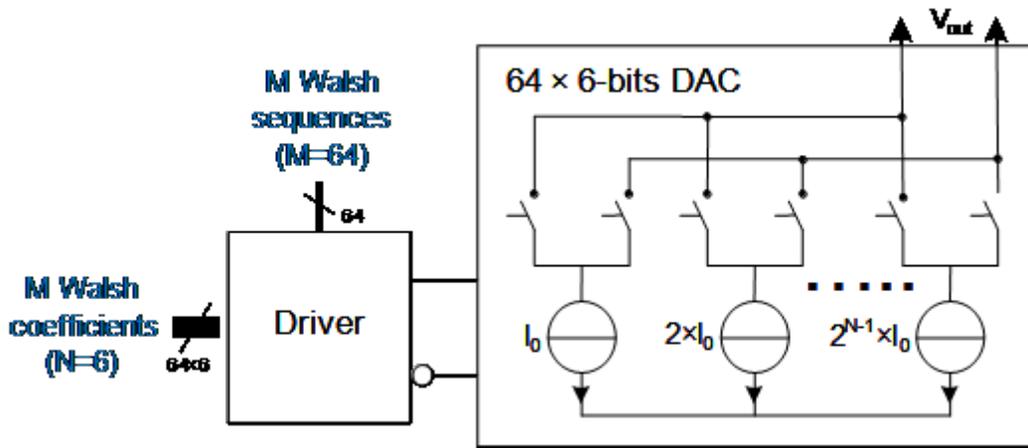


Figure 3-39: The DAC architecture

The DAC has to convert the members of the Walsh series quickly ($f_0=8\text{GHz}$) with a number N of quantization bits. The values of this two parameters specify the DAC architecture sizing beginning with the driver.

3.3.1 The Driver:

The driver is the circuit that masters the DAC switches. Since the DAC has is a differential, 2 outgoing signals (cmd, cmd') are required to drive the DAC switches. They are generated by the logical circuit of the following figure:

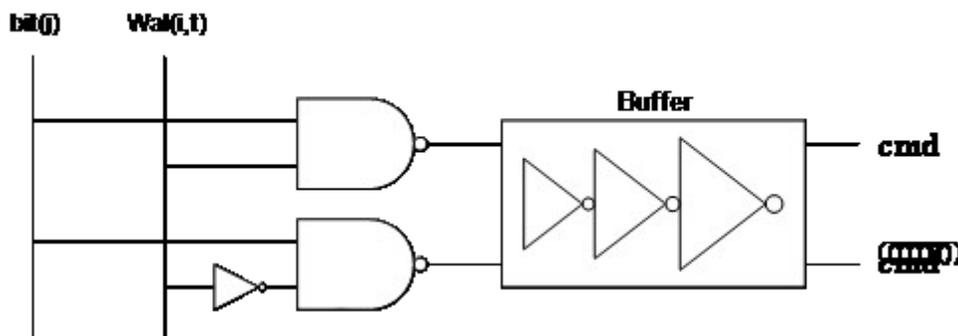


Figure 3-40: The driver architecture

For each bit j of the 6-bit word, encoding the coefficient i corresponding to the i^{th} Walsh sequence requires to leave or not pass current through the N or P branches to the differential load, depending on the value of $Wal(j,t)$. The truth table establishing the behavior of the switching is as follows:

Table 3-2: Driver truth table

$bit(j)$	$Wal(i,t)$	$Wal'(i,t)$	cmd	cmd'
0	0	1	0	0
0	1	0	0	0
1	0	1	0	1
1	1	0	1	0

Then, if the current bit weight (i) is not zero, depending on the value of the Walsh sequence, all the current passes into the branch P if it zero or into branch N if it is not zero.

The current is oriented in each of the branches every time the DA conversion takes place at a frequency f_0 of $8GHz$. The control signals (cmd, cmd') thus vary at the same frequency. They master switches that have variable size, depending on the current weight to drain.

Then, buffers are required to ensure a fast switching frequency of all the switches. Under these conditions, the architecture of Fig. 3.13 was thus sized to give the results shown in Fig. 3.14.

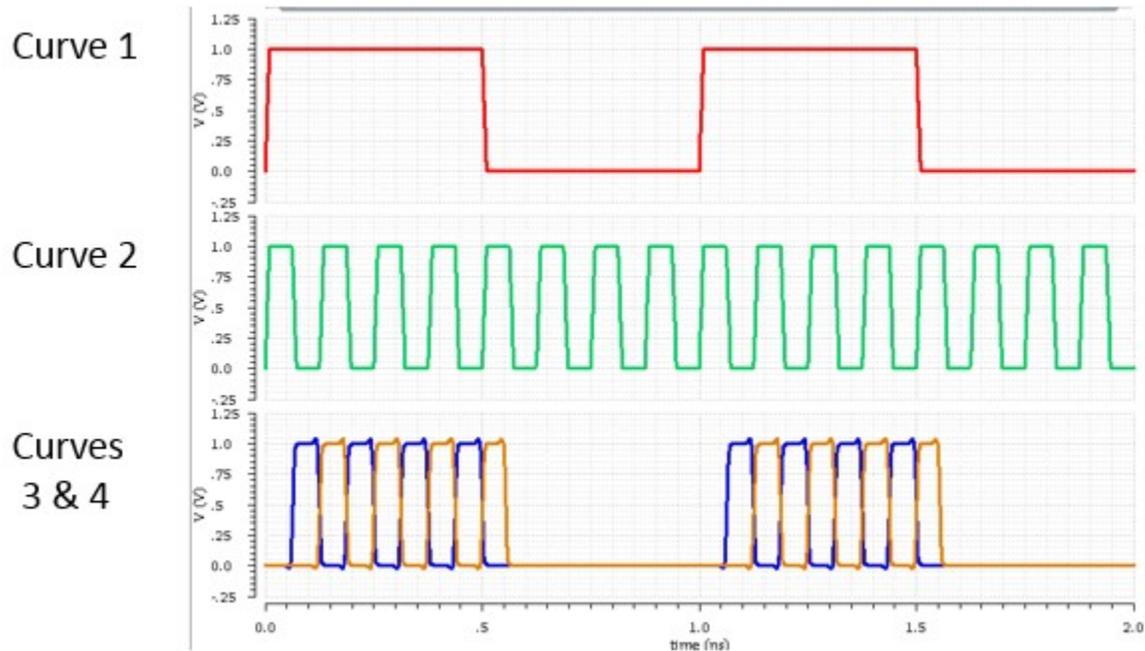


Figure 3-41: Driver control signals

The curve number 1 shows the variation of a Walsh coefficient bit at a frequency of 250MHz while the curve number 2 represents change in the fastest Walsh sequence. The curves 3 and 4 correspond to signals that will control the switches of the DAC. They are complementary and cross perfectly during the entire time interval.

The next parts depict the architecture of the DAC. First, we explain how the current sources are dimensioned to ensure their consistency despite the process manufacturing variability. Then, we explain how the switches are instantiated to ensure a continuity of the current in the differential load. After that, the performances of the 6-bit DAC and the entire DAC is showed.

3.3.2 The *Current Sources (CSs)*:

Technological considerations must be taken into account during integration on silicon of $64 \times 6 = 512$ unit CS. Dispersion on the uniformity of doping is expected. The CS sizing is therefore required to eliminate mismatch due to technology and the gate overdrive voltage.

This sizing starts by determining the unit current I_0 . It is determined especially according to the number of quantization bit $N=6$ and the number of Walsh sequences $M=64$ and following the next equation:

$$I_0 = \frac{1}{M \cdot 2^N} \sqrt{2} \times \sqrt{\frac{P_{out}}{R_{load}}} \quad (3.2)$$

The value of the differential load R_{load} is set at 100Ω and output power P_{out} at 0dBm.

After calculating using the above equation, the unit current is $I_0 = 3.2 \mu A$.

The *Integral Non Linearity* (INL) specification based on the random fluctuation in the nominal value of the CS is set to be 0.5 LSB. This results in a relative standard deviation $\frac{\delta I}{I}$ of 8.84%, according to equation (3.3):

$$INL \cong \sqrt{2^{N-1}} \frac{\delta I}{I} LSB = 0.5 LSB \quad (3.3)$$

One can then calculate the minimum gate area of the CS unit transistors [44] based on the parameter mismatch statistical model (for confidentiality reasons their values will not be provided here) following the next equation:

$$(W \times L)_{min} = \frac{1}{2} \left[A_{\beta}^2 + \frac{4 A_{Vt}^2}{(V_{GS} - Vt)^2} \right] I \left(\frac{\delta I}{I} \right)^2 \quad (3.4)$$

$(W \times L)_{min}$ has been calculated to be $0.1024 \mu m^2$ and so the CS transistor M_{CS} has a gate length of $0.15 \mu m$ and a width of $0.7 \mu m$. The CS unit has been implemented using *Regular Threshold Voltage* (RVT) MOS biasing voltage $V_{bias1} = 0.52 V$.

To limit variations in the unit current, the CS is cascoded by a *Low Threshold Voltage* (LVT) transistor M_{CAS1} operating in saturation condition that maintains a constant voltage to the input of the switch. It is sized minimally: $W_{CAS1} = 0.15 \mu m$ and $L_{CAS1} = 0.10 \mu m$.

3.3.3 The DAC Design:

3.3.3.1 The DAC Unit Cell:

As specified in the previous section, the cascaded current source will be connected to the load through a differential pair of switches. Fig. 2.15 shows the unit cell of the DAC.

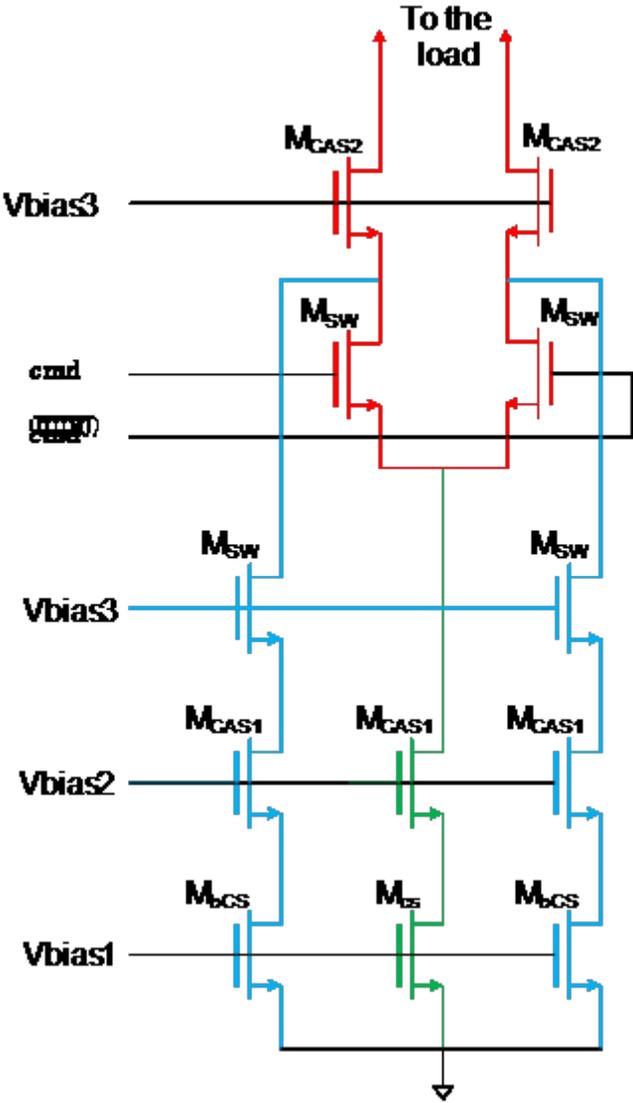


Figure 3-42: DAC unit cell

All transistors in the above figure are stacked under a 1V power supply and are biased from outside the chip using DC voltage sources. The cascaded current source (M_{cs}, M_{CAS1}) , that

was previously dimensioned, its output is connected to a differential switching pair (M_{sw} , M_{CAS2}).

Precautions have been taken to size M_{CAS2} : their r_{ds} has to be wide enough to isolate the cell and their C_{gs} values should be small enough to avoid the signal-dependent output impedance from the switching activity. That is why they are always kept on, ensuring a permanent current through the two extra branches drawn in blue (M_{bcs} , M_{CAS1} , M_{sw}). They are minimally sized (see table 3.3) to permanently drive only a small amount of current into the load (whenever or not switches are open).

Table 3-3: DAC unit cell MOSFET sizing

MOS	Type	W [nm]	L [nm]	Biasing [V]
M_{cs}	RVT	700	150	$V_{bias1}=0.52$
M_{bcs}	RVT	175	150	$V_{bias1}=0.52$
M_{cas1}	LVT	150	100	$V_{bias2}=0.9$
M_{sw}	LVT	90	35	0/1
M_{cas2}	LVT	160	100	$V_{bias3}=1$

3.3.3.2 The 6-bit DAC:

To get the 6-bit DAC, the transistor of the DAC unit cell has been parallelized as many times as needed to achieve each binary weight. Only the size of the bleeder branch transistors has changed. The transistor corresponding to the 3 LSB are sized as described by the previous table while the others are sized differently. The reason is to reduce the power consumption of these extra branches. Then, the M_{bcs} transistor drain currents of Table 3.4 are observed bringing only 12% of extra power consumption.

Table 3-4: Currents spent in the bleeder branches

	3LSB			3MSB		
Branch Weight	1	2	4	8	16	32
Bleeding current	0.79 μ A	1.6 μ A	3.19 μ A	3.21 μ A	6.41 μ A	12.48 μ A

To check the behavior of the 6-bit DAC, a transient simulation covering all the 2^6 binary codes have been processed. The first inputs $Wal(i,t)$ of the drivers were set to 1V. The second input was excited by *Piece Wise Linear* (PWL) sources oscillating at a frequency of 8GHz while taking 1V or 0V value according to the binary code. A differential voltage V_{diff} was taken at the inputs of a differential load of 100Ω and is depicted by the following figure:

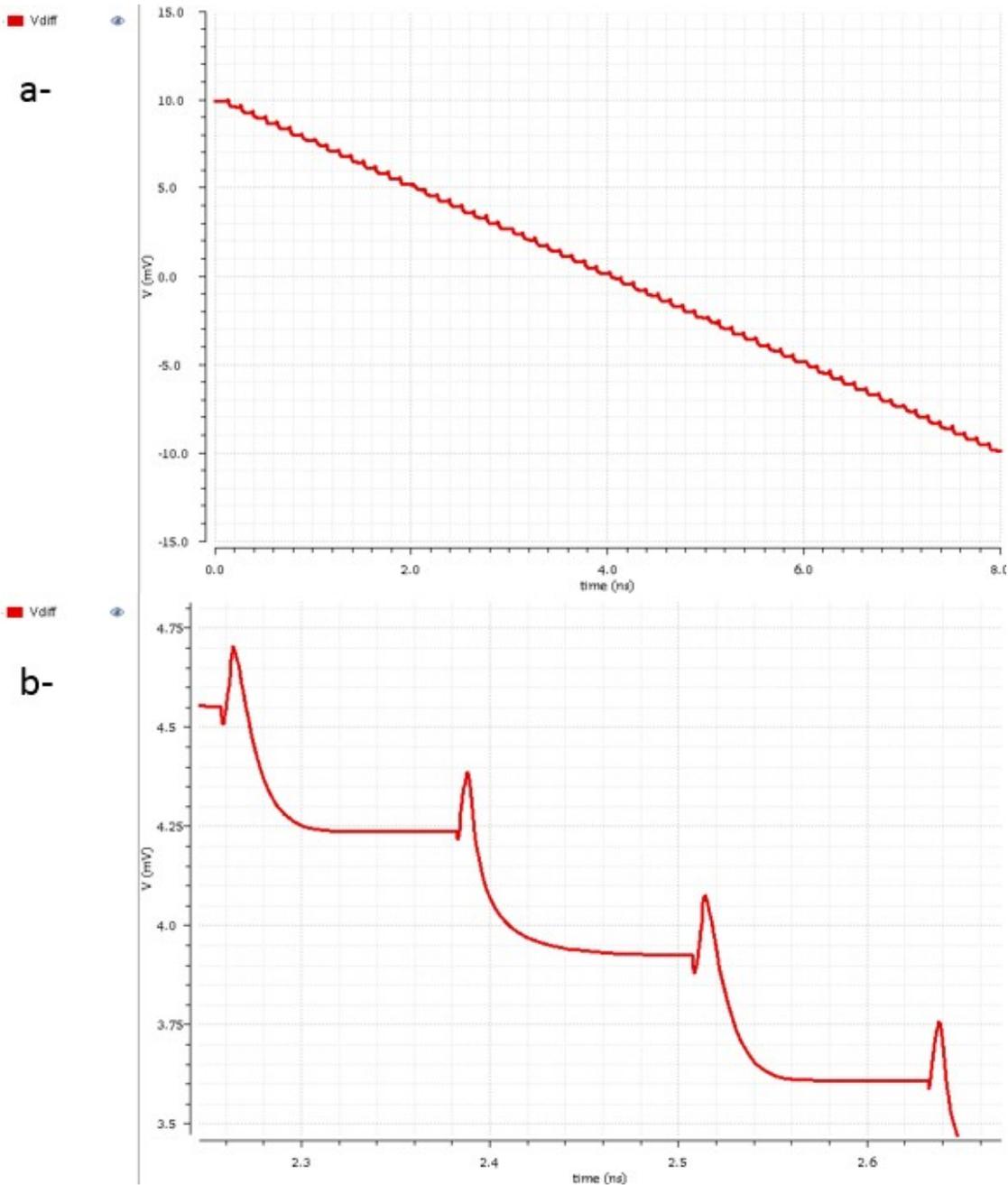


Figure 3-43: a- 6-bit DAC differential output voltage, b- zoom between 2.2ps and 2.7ps

The Fig. 3.16-a, shows that all the codes are recovered. The full scale differential voltage is 20mV. It corresponds to a full scale differential current of $200\mu\text{A}$ (into a differential load of $100\ \Omega$) and, as showed by the Fig. 3.16-b, the current steps have a regular value independently to the code. This value of $3.175\mu\text{A}$ is close to theoretical current unit value: $I_0=3.2\mu\text{A}$. It

confirms that the 6-bit DAC architecture is able to convert the 6-bit coded Walsh coefficients at a frequency of 8GHz.

3.3.3.3 The Whole DAC:

To check that the whole DAC is operational, all the blocks of the Walsh transmitter apart the Walsh coefficient conversion interface have been assembled. A 2.5GHz sinewave of 1V magnitude was processed under Matlab. The 64 coded Walsh coefficients have been extracted and loaded in 64×6 PWL sources. The resulting differential output is represented by the following figure:

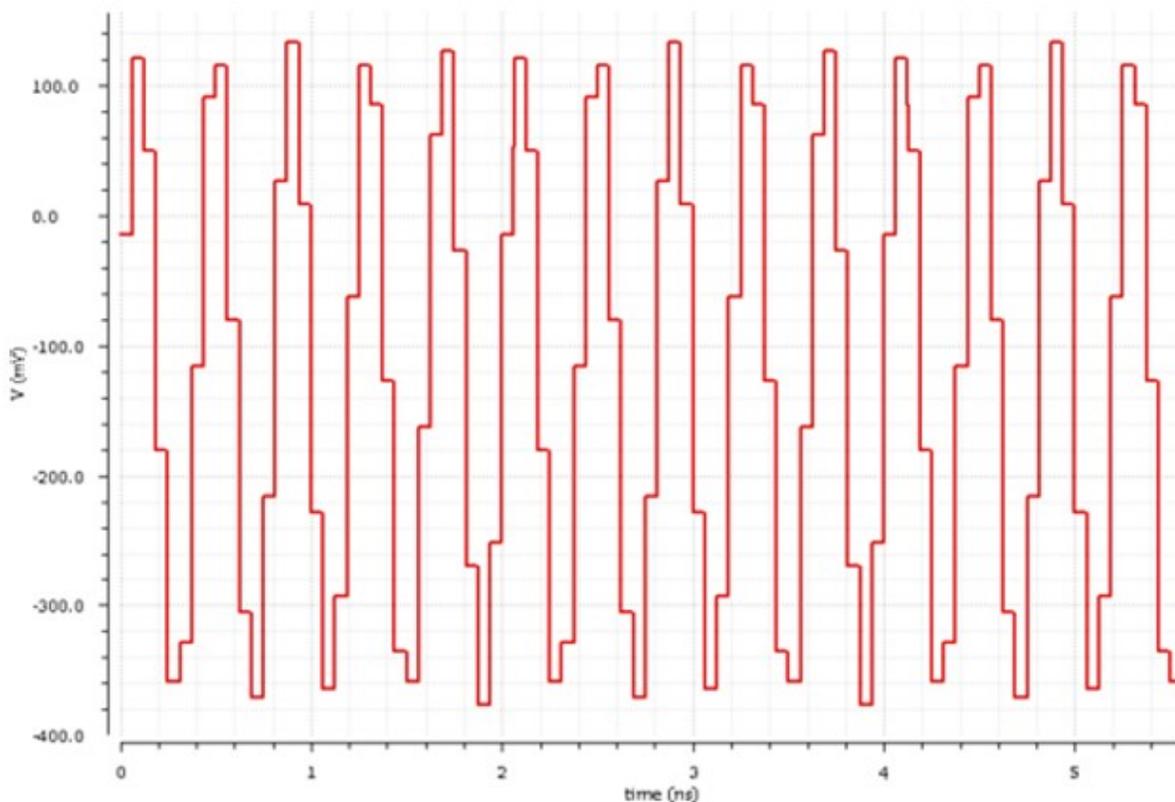


Figure 3-44: DAC output signal in 100Ω differential

In order to analyze the spectrum, the transistor level DAC simulated output signal is exported from Spectre RF to Matlab. Then, its DFT was calculated and compared with the spectrum of the ideal signal evolution through the generation process (Fig 3.18).

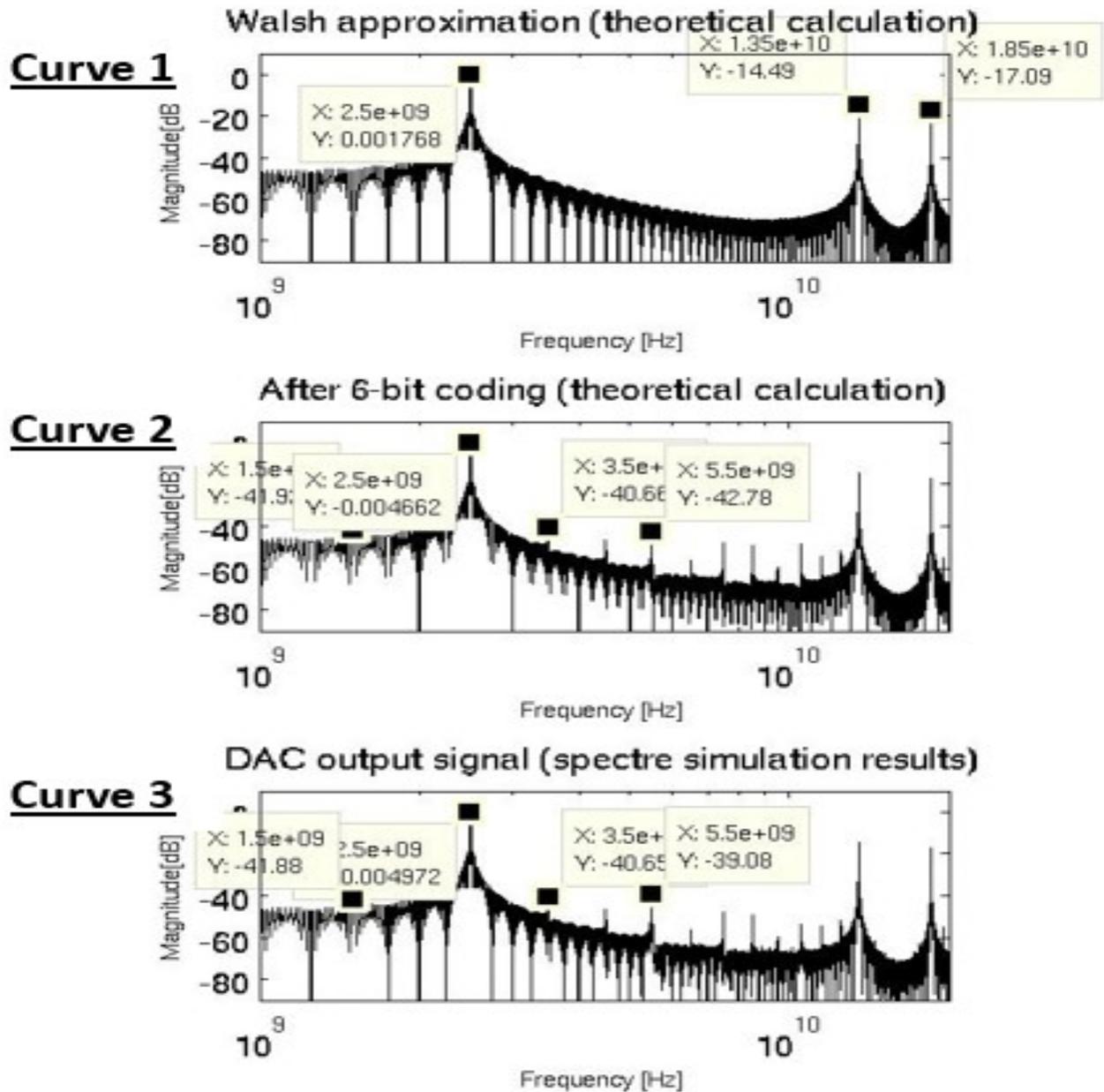


Figure 3-45: Spectra of a single tone RF signal of 2.50 GHz before, after coefficient quantization and at Walsh DAC output

The above figure describes the evolution of this single tone RF signal:

- Curve 1 is the spectrum of the piecewise linear interpolation of the Walsh series expansion at order 64 given by Matlab, while using real values of the coefficients. It presents spurs that are unavoidable with the sampled Walsh approach.

- Curve 2 is the spectrum of the same previous approximation but using 6-bits coded Walsh coefficients and always processed under Matlab. Here the noise floor increases revealing new spurs which are the consequence of the quantization error.
- Curve 3 is the spectrum of the signal processed by the Walsh transmitter which is imported from Spectre RF. There is no significant difference in results between the implementation of the Walsh transmitter and the Matlab Walsh series generation process.

The resulting spectra clearly show a 40 dB harmonic rejection over 4 GHz bandwidth.

After the Walsh transmitter integration in 28nm FDSOI, the system is characterized thanks to the Walsh coefficients calculated out of the chip. It is then required to address the chip by the

64×6 -bit coded Walsh coefficients. But, it is not possible to place so many pads on one chip.

It is then necessary to use an additional circuit to reduce this number of pads.

3.4 The Walsh Coefficients Conversion Unit:

The Walsh coefficient management unit role is to parallelize the incoming serial data which have been calculated thanks to a laptop (Fig 3.19). The aim of this block is to reduce the number of pads on the chip.

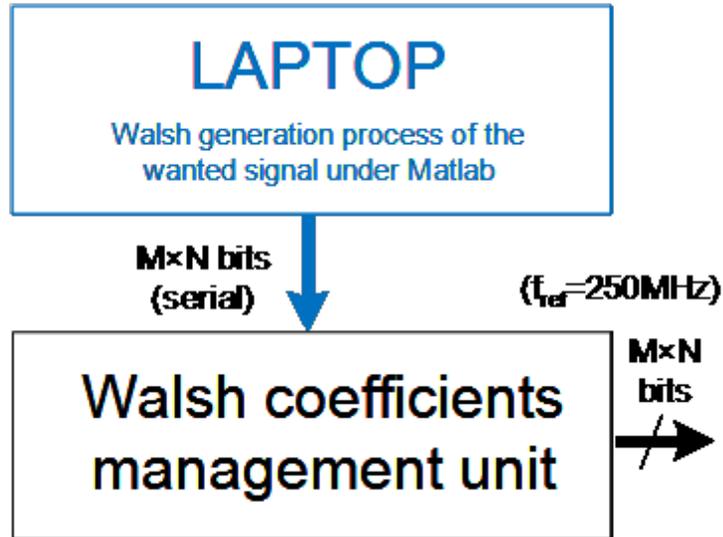


Figure 3-46: Walsh 6 bit coded coefficients distribution

As described in the Fig. 3.19, this bloc parallelizes the $M=64$ Walsh coefficients processed following the Matlab generation process of chapter 2. At that point, the Walsh coefficient are $N=6$ - bit coded and are provided by the laptop output in a serial form. Then, it is necessary to parallelize these data in order to properly address the switches of the 64×6 bits coding DAC. In order to avoid the use of a complex communication protocol between the chip and the laptop, this addressing is made in two steps:

- The first one is to parallelize the serial Walsh coded coefficients coming from the laptop with a *Serial Parallel Interface (SPI)* and store them by writing on a *Static Random Access Memory (SRAM)*
- The second one is to read the parallelized Walsh coefficients from the SRAM while switching off the SPI.

Thus, one should take in consideration the keys parameter of the system to link and size the SPI and the SRAM. The sizing begins with the SRAM because its size depends of which kind of signal

we need to reconstruct. The design is realized using a digital design flow from STMicroelectronics.

3.4.1 The SRAM:

To size the SRAM, the signal type is reconstructed and approximated by the generation process under Matlab. The number of symbols arising from a precise modulation scheme can be expressed as the following equation:

$$NoSymbol = SRAMsize \times \frac{1}{order \times N} \times \frac{1}{f_{ref}} \times DR \quad (3.3)$$

Thus, to simulate more than 120 symbols of a QPSK modulation signal running at 100Mbps and using ($M=64$ / $N=6$ / $f_{ref} = 250\text{MHz}$), the SRAM size should be more than 154kB. Then taking 2 SRAMs of 128kB will provide enough 16 QAM symbols to test the reconstructed signal.

The SRAMs have been generated to be of the size of 512 words and 256 bits. Their *GDS* files are automatically generated by a specific tool of STMicroelectronics. Each of the delivered SRAMs [45] have a size of 0.06mm² and consume 3.75mW in write mode while 0.3mW in read mode.

They are supplied under 1V voltage and their access time is of 618ps (which is less than $\frac{1}{f_{ref}}$).

3.4.2 The SPI:

The SPI writes the 6 bits coded Walsh coefficients on the SRAMs. As there are 2 SRAMs, 2 identical SPIs (Fig. 3.20) are used to address each of them.

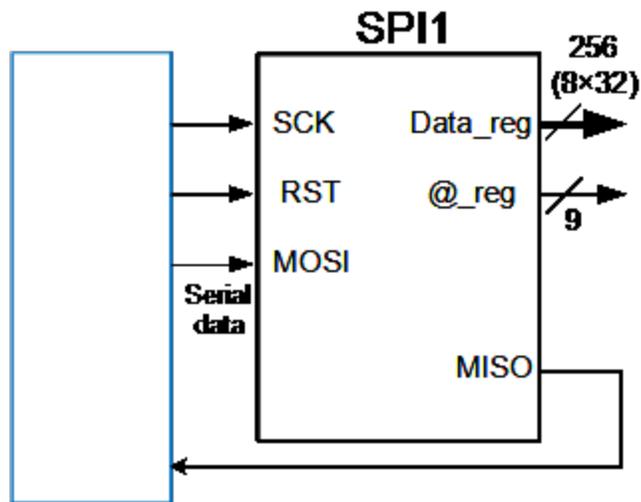


Figure 3-47: SPI's symbol

As depicted by the above figure, the SPI is mastered by the laptop which activate it through the RST and clock it through the SCK . The pin *Master Out Slave In* (MOSI) transmits data packet of 256 bits from the laptop to the SPI. The data correspond to 32 Walsh coefficients coded on 6 bit but encapsulated in an 8-bit word by the addition of 2 bits having a zero value. The corresponding parallel data are found in the data registers. They are transmitted to the SRAM at a frequency of 10MHz thanks to 256 wires. Depending on the address pointed by the address register ($@_reg$), the right SRAM line is loaded. The last pin *Master In Slave Out* (MISO) allows to check from the laptop the values of the 2 previously announced registers.

The SPI design is based on Verilog code that is processed in a *GDS* file thanks to the digital design flow represented in the following figure:

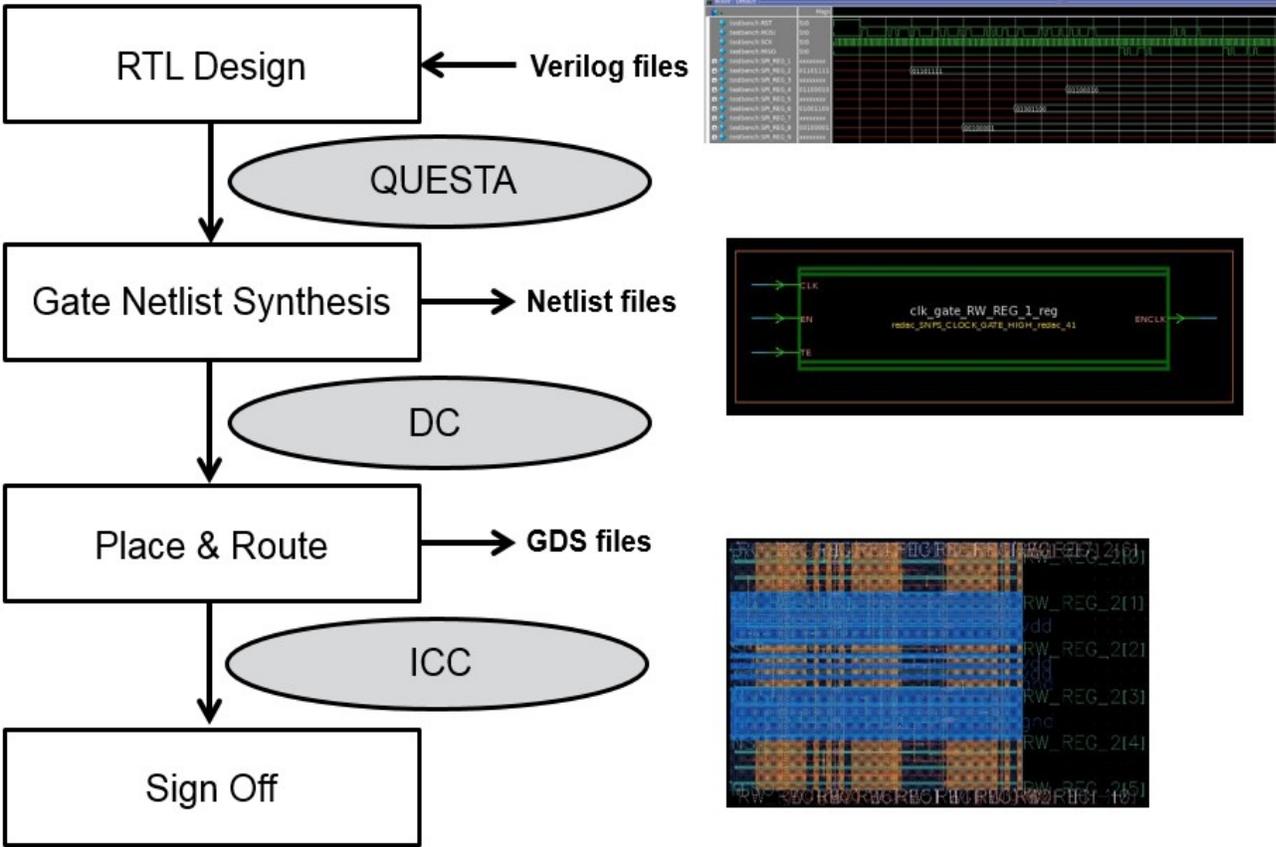


Figure 3-48: SPI’s digital design flow

3.4.3 The Walsh Coefficients Addressing:

From the netlists of the SPI and SRAM, the architecture of the Walsh coefficients conversion interface can be designed. To connect the SPI and the SRAM, a multiplexer is needed in order to select the working frequency of the memory. As announced before the writing is made at 10MHz but it should be read at the Walsh coefficients $f_{ref}=250\text{ MHz}$. Thus, a multiplexer (2:1) and a 9-bit counter has been designed to properly read the SRAMs values (Fig 3.22).

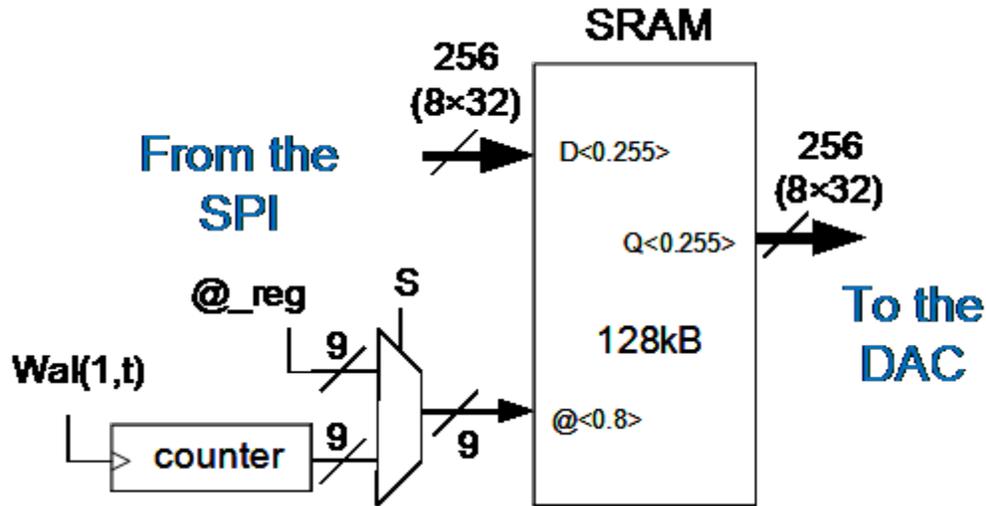


Figure 3-49: The link between SPI and SRAM

As depicted by the above figure, the SRAM reading is controlled by SPI. The bit S of an internal register of the SPI selects the multiplexer input to be read. Then when loading, the SRAM address registers receive at 10MHz the data coming from the $@_reg$ of the SPI, while reading the outputs of the 9-bit counter are read at 250MHz. to scroll all the addresses of the SRAM.

The whole circuit has been assembled twice to get the 256kB data corresponding to 512 sets of 64×6 Walsh coded coefficients. The whole area is 0.15mm^2 and an average power consumption of 8mW was estimated.

3.4 Conclusion:

System simulations of chapter 2 have shown that the Walsh approach allows direct digital modulated carrier aggregation. The simulations presented in this chapter show that the Walsh DAC can generate a carrier of 2.5 GHz. It presents 40 dB on 4 GHz of bandwidth, a power consumption of 13.62mW with an efficiency of 0.26pJ/bit and a size of 0.2mm² while running at 16GSps. Transistor level simulation results align very well with behavior model simulations. That confirms that the Walsh generator is a very promising architecture for targeting multiple carrier aggregation. The Walsh coefficient management unit with the core system can be integrated at the cost of 0.35mm² silicon area while dissipating only a power of 25mW. It is therefore possible to integrate this chip on a *System on Chip* (SoC) of almost 32 pins while using a total area of 1mm².

Conclusion

Converting digital data into an analog signal is a key point of the development of the wireless technologies. The state-of-the-art suggests multiple solutions which still struggle to meet the stringent power consumption constraints imposed by the future standards.

This thesis propose a new transmitter architecture named the Walsh transmitter. It is based on a spectral synthesis of the signal to transmit through its Walsh series expansion. The digital-to-analog conversion takes benefit from the number of Walsh sequences (order) and the resolution of the Walsh coefficients (N-bit quantization) used to develop the series in order to improve respectively the SFDR and the SNR.

The design of the Walsh transmitter in 28nm silicon technology from STMicroelectronics demonstrates its capability to deal with high speed switching of 16Gbps while consuming 25mW. The designed circuit presents a better energy cost than the state of the art FR-DACs, with a value of 0.26J per Gbit of transmitted data.

These results highlight the competitiveness of the Walsh transmitter when compared to the conventional architectures that fail to reduce the cost of information in terms of energy. That purpose is key when looking at the expected specifications for the next generation of wireless communication standards.

This thesis detailed an approach to the design by mathematics, while presenting a demonstrator of the Walsh transmitter design which can be adjusted to reach the forthcoming standard specifications.

Bibliography

- [1] "Understanding-5G_Perspectives on future technological advancements in mobile".
- [2] "Strategy Analytics, P. Nitesh, 'Handset Data Traffic.'"
- [3] J. Mitola, "The software radio architecture," *IEEE Commun. Mag.*, vol. 33, no. 5, pp. 26–38, May 1995.
- [4] 5GPPP, "The 5G Infrastructure Public Private Partnership: the next generation of communication networks and services." Feb-2015.
- [5] 4G Americas, "LTE Carrier Aggregation Technology Development and Deployment Worldwide." Oct-2014.
- [6] H. Darabi, A. Mirzaei, and M. Mikhemar, "Highly Integrated and Tunable RF Front Ends for Reconfigurable Multiband Transceivers: A Tutorial," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 58, no. 9, pp. 2038–2050, Sep. 2011.
- [7] M. Ingels, C. Soens, J. Craninckx, V. Giannini, T. Kim, B. Debaillie, M. Libois, M. Goffioul, and J. V. Driessche, "A CMOS 100 MHz to 6 GHz software defined radio analog front-end with integrated pre-power amplifier," in *Solid State Circuits Conference, 2007. ESSCIRC 2007. 33rd European, 2007*, pp. 436–439.
- [8] O. Oliaei, M. Kirschenmann, D. Newman, K. Hausmann, H. Xie, P. Rakers, M. Rahman, M. Gomez, C. Yu, B. Gilsdorf, and K. Sakamoto, "A multiband multimode transmitter without driver amplifier," in *2012 IEEE International Solid-State Circuits Conference, 2012*, pp. 164–166.
- [9] B. Analui, T. Mercer, S. Mandegaran, A. Goel, and H. Hashemi, "A 50 MHz-6 GHz, 2 × 2 MIMO, reconfigurable architecture, software-defined radio in 130nm CMOS," in *2014 IEEE Radio Frequency Integrated Circuits Symposium, 2014*, pp. 329–332.
- [10] Y. Yin, B. Chi, Z. Sun, X. Zhang, and Z. Wang, "A 0.1-6.0-GHz Dual-Path SDR Transmitter Supporting Inband Carrier Aggregation in 65-nm CMOS," *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 23, no. 5, pp. 944–957, May 2015.

- [11] A. Jerng and C. G. Sodini, "A Wideband $\Delta\Sigma$ Digital-RF Modulator for High Data Rate Transmitters," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1710–1722, Aug. 2007.
- [12] A. Frappe, A. Flament, B. Stefanelli, A. Kaiser, and A. Cathelin, "An All-Digital RF Signal Generator Using High-Speed Modulators," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2722–2732, Oct. 2009.
- [13] Z. Boos, A. Menkhoff, F. Kuttner, M. Schimper, J. Moreira, H. Geltinger, T. Gossmann, P. Pfann, A. Belitzer, and T. Bauernfeind, "A fully digital multimode polar transmitter employing 17b RF DAC in 3G mode," in *2011 IEEE International Solid-State Circuits Conference*, 2011, pp. 376–378.
- [14] C. Lu, H. Wang, C. Peng, A. Goel, S. Son, P. Liang, A. Niknejad, H. Hwang, and G. Chien, "A 24.7dBm all-digital RF transmitter for multimode broadband applications in 40nm CMOS," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 332–333.
- [15] R. Bhat and H. Krishnaswamy, "A watt-level 2.4 GHz RF I/Q power DAC transmitter with integrated mixed-domain FIR filtering of quantization noise in 65 nm CMOS," in *2014 IEEE Radio Frequency Integrated Circuits Symposium*, 2014, pp. 413–416.
- [16] M. S. Alavi, R. B. Staszewski, L. C. N. de Vreede, and J. R. Long, "A Wideband 2 13-bit All-Digital I/Q RF-DAC," *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 4, pp. 732–752, Apr. 2014.
- [17] W. M. Gaber, P. Wambacq, J. Craninckx, and M. Ingels, "A CMOS IQ Digital Doherty Transmitter using modulated tuning capacitors," in *ESSCIRC (ESSCIRC), 2012 Proceedings of the*, 2012, pp. 341–344.
- [18] P. Liang, H. Wang, C. H. Peng, A. Peng, H. C. Hwang, G. Chien, C. L. Tsai, Mediatek, and A. Niknejad, "Digital transmitter design for mobile devices," *IEEE Commun. Mag.*, vol. 51, no. 10, pp. 114–123, Oct. 2013.
- [19] Z. Ye, J. Grosspietsch, and G. Memik, "An FPGA Based All-Digital Transmitter with Radio Frequency Output for Software Defined Radio," in *Automation Test in Europe Conference Exhibition 2007 Design*, 2007, pp. 1–6.
- [20] J. Venkataraman and O. Collins, "An All-Digital Transmitter with a 1-Bit DAC," *IEEE Trans. Commun.*, vol. 55, no. 10, pp. 1951–1962, Oct. 2007.
- [21] K. A. Shehata, M. A. Aboul-Dahab, S. H. E. Ramly, and K. A. Hamouda, "An FPGA based 1-bit all digital transmitter employing Delta-Sigma Modulation with RF output for SDR," in *2nd International Conference on Signals, Circuits and Systems, 2008. SCS 2008*, 2008, pp. 1–6.

- [22] A. B. Arfi, M. Helaoui, and F. M. Ghannouchi, "All-digital sigma-delta RF modulator for software defined radio applications," in *2015 IEEE 28th Canadian Conference on Electrical and Computer Engineering (CCECE)*, 2015, pp. 1379–1382.
- [23] E. Roverato, M. Kosunen, J. Lemberg, T. Nieminen, K. Stadius, J. Ryyänen, P. Eloranta, R. Kaunisto, and A. Pärssinen, "A configurable sampling rate converter for all-digital 4G transmitters," in *2013 European Conference on Circuit Theory and Design (ECCTD)*, 2013, pp. 1–4.
- [24] C. H. Lin, F. van der Goes, J. Westra, J. Mulder, Y. Lin, E. Arslan, E. Ayranci, X. Liu, and K. Bult, "A 12b 2.9GS/s DAC with IM3<-60dBc beyond 1GHz in 65nm CMOS," in *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, 2009, p. 74–75,75a.
- [25] J. Xiao, B. Chen, T. Y. Kim, N. Y. Wang, X. Chen, T. H. Chih, K. Raviprakash, H. F. Chen, R. Gomez, and J. Y. C. Chang, "A 13-Bit 9GS/s RF DAC-based broadband transmitter in 28nm CMOS," in *2013 Symposium on VLSI Circuits*, 2013, pp. C262–C263.
- [26] T. Alpert, F. Lang, D. Ferenci, M. Grözing, and M. Berroth, "A 28GS/s 6b pseudo segmented current steering DAC in 90nm CMOS," in *Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International*, 2011, pp. 1–4.
- [27] G. Engel, S. Kuo, and S. Rose, "A 14b 3/6GHz current-steering RF DAC in 0.18 μ m CMOS with 66dB ACLR at 2.9GHz," in *2012 IEEE International Solid-State Circuits Conference*, 2012, pp. 458–460.
- [28] S. Balasubramanian, S. Boumaiza, H. Sarbishaei, T. Quach, P. Orlando, J. Volakis, G. Creech, J. Wilson, and W. Khalil, "Ultimate Transmission," *IEEE Microw. Mag.*, vol. 13, no. 1, pp. 64–82, Jan. 2012.
- [29] J. Walsh, "A Closed Set of Normal Orthogonal Functions," *Am. J. Math. Vol 45 No 1 Jan 1923 Pp 5-24*.
- [30] H. Harmuth, "A generalized concept of frequency and some applications," *IEEE Trans. Inf. Theory*, vol. 14, no. 3, pp. 375–382, May 1968.
- [31] H. E. Jones, "An adaptative digital voice multiplexer using Walsh functions," *1972 Proc. Appl. Walsh Funct. AD-744 650*.
- [32] P. J. Milne, N. Ahmed, R. R. Callagher, and S. G. Harris, "An application of Walsh functions to the monitoring of electrocardiograph signals," *1972 Proc. Appl. Walsh Funct. AD-744 650*.

- [33] H. F. Harmuth, "Applications of Walsh functions in communications," *IEEE Spectr.*, vol. 6, no. 11, pp. 82–91, Nov. 1969.
- [34] F. Furrer, A. Shah, and M. Maurer, "A Walsh-Function power-cable monitoring system," *1972 Proc. Appl. Walsh Funct. AD-744 650*.
- [35] C. W. Thomas and A. J. Welch, "Heart rate representation using Walsh functions," *1972 Proc. Appl. Walsh Funct. AD-744 650*.
- [36] D. I. Durst, "Results of Multiplexing experiments using Walsh functions."
- [37] H. F. Harmuth, "Sequency Filters Based on Walsh Functions," *IEEE Trans. Electromagn. Compat*, vol. EMC-10, no. 2, pp. 293–295, Jun. 1968.
- [38] A. M. Despain, "Walsh functions in Grille Spectroscopy," *1972 Proc. Appl. Walsh Funct. AD-744 650*.
- [39] W. L. Pratt, "Walsh Functions in Image Processin- and Two-Dimensional Filtering," *1972 Proc. Appl. Walsh Funct. AD-744 650*.
- [40] M. Bath and S. Burman, "Walsh Spectroscopy of Rayleigh waves caused by underground detonations," *1972 Proc. Appl. Walsh Funct. AD-744 650*.
- [41] J. Liferman, "Les méthodes rapides de transformation du signal: Fourier, Walsh, Hadamard, Haar," MASSON., pp. 145–166.
- [42] M. D. McKinley, K. A. Remley, M. Myslinski, J. S. Kenney, D. Scheurs, and B. Nauweaers, "EVM Calculation for Broadband Modulated Signals," *64th ARFTG Conf.*, 2004.
- [43] C. Al Khatib, "Conception de dispositifs de contrôle asynchrone et distribués pour la gestion de l'énergie."
- [44] J. Bastos, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 12-Bit Intrinsic Accuracy High-Speed CMOS DAC," *IEEE J. Solid-State Circuits*, 1998.
- [45] "C28SOI_MEM_SRAM_Data_Sheet".

Annex A

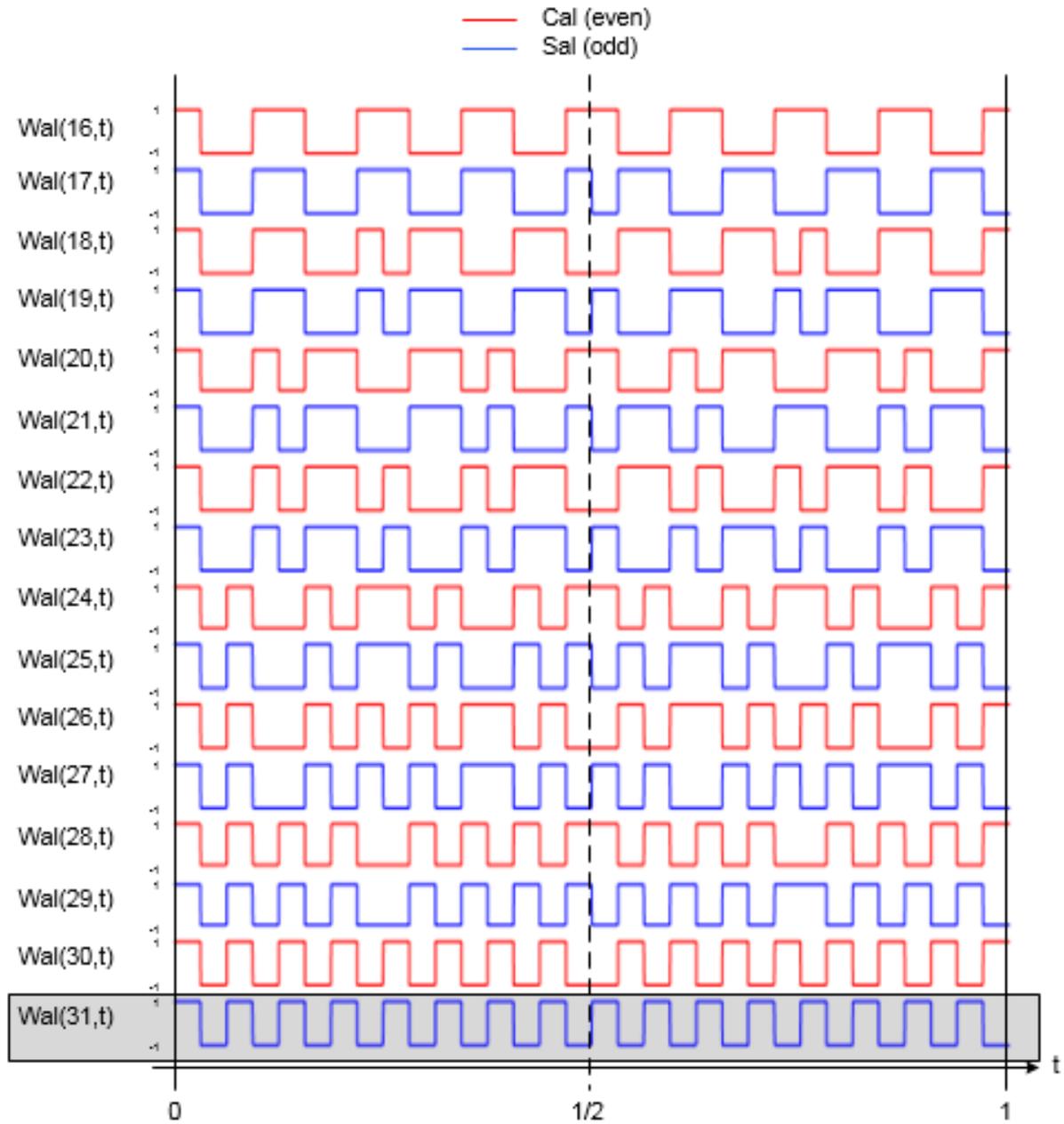


Figure A-1: The Walsh sequences from $Wal(16,t)$ to $Wal(31,t)$

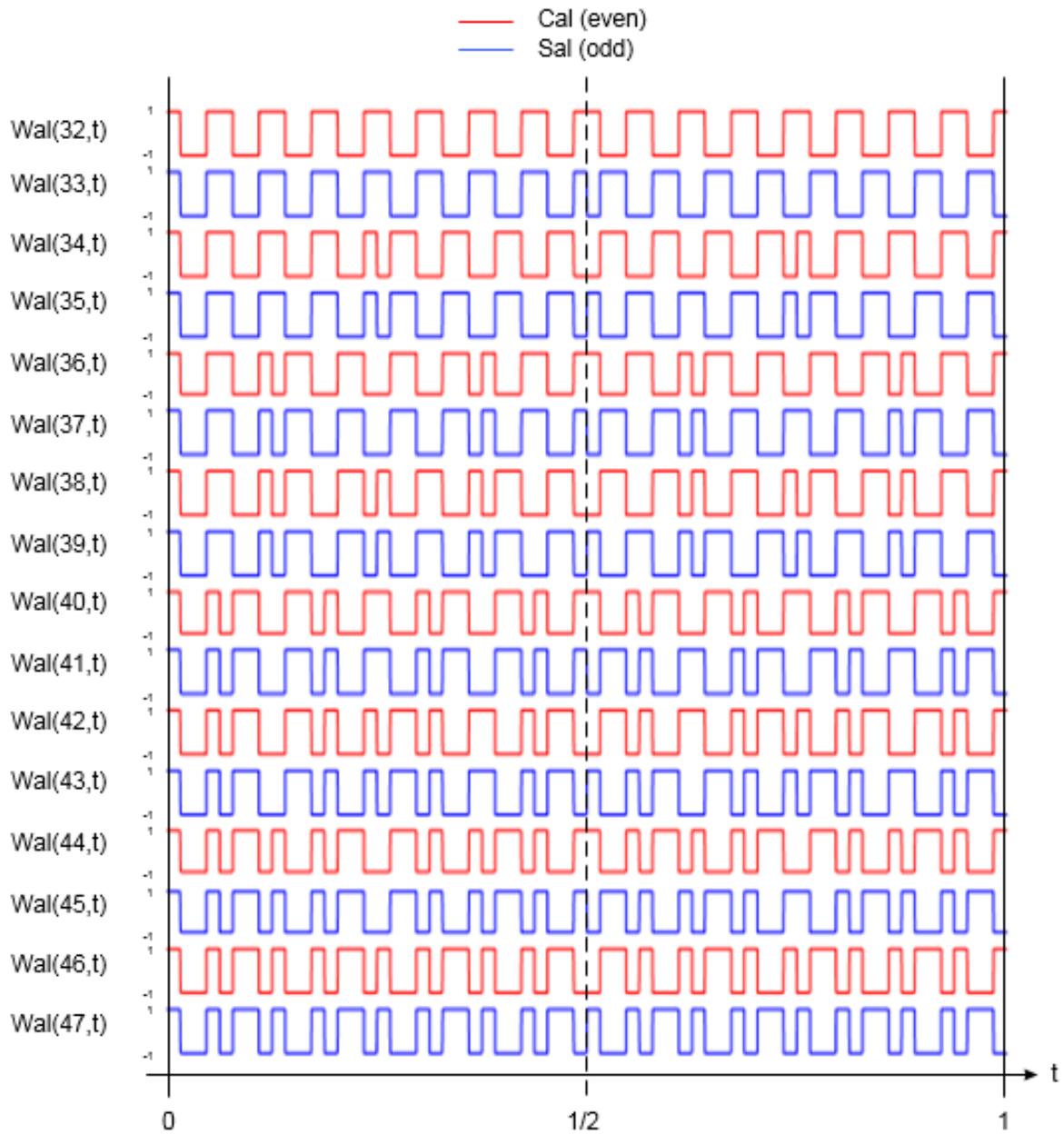


Figure A-2: The Walsh sequences from $Wal(32,t)$ to $Wal(47,t)$

Annex B

Table B-1: The Walsh sequence expressions from $Wal(0,t)$ to $Wal(31,t)$ in function of the primary sequences

	$rad(6,t)=$ $Wal(63,t)$	$rad(5,t)=$ $Wal(31,t)$	$rad(4,t)=$ $Wal(15,t)$	$rad(3,t)=$ $Wal(7,t)$	$rad(2,t)=$ $Wal(3,t)$	$rad(1,t)=$ $Wal(1,t)$	Walsh sequence expressed in function of the primary Walsh sequences
Bit of the Gray code	E_6	E_5	E_4	E_3	E_2	E_1	
$Wal(0,t)$	0	0	0	0	0	0	$Wal(0,t)$
$Wal(1,t)$	0	0	0	0	0	1	$Wal(1,t)$
$Wal(2,t)$	0	0	0	0	1	1	$Wal(1,t) \oplus Wal(3,t)$
$Wal(3,t)$	0	0	0	0	1	0	$Wal(3,t)$
$Wal(4,t)$	0	0	0	1	1	0	$Wal(3,t) \oplus Wal(7,t)$
$Wal(5,t)$	0	0	0	1	1	1	$Wal(1,t) \oplus Wal(3,t) \oplus Wal(7,t)$
$Wal(6,t)$	0	0	0	1	0	1	$Wal(1,t) \oplus Wal(7,t)$
$Wal(7,t)$	0	0	0	1	0	0	$Wal(7,t)$
$Wal(8,t)$	0	0	1	1	0	0	$Wal(7,t) \oplus Wal(15,t)$
$Wal(9,t)$	0	0	1	1	0	1	$Wal(1,t) \oplus Wal(7,t) \oplus Wal(15,t)$
$Wal(10,t)$	0	0	1	1	1	1	$Wal(1,t) \oplus Wal(3,t) \oplus Wal(7,t) \oplus Wal(15,t)$
$Wal(11,t)$	0	0	1	1	1	0	$Wal(3,t) \oplus Wal(7,t) \oplus Wal(15,t)$
$Wal(12,t)$	0	0	1	0	1	0	$Wal(3,t) \oplus Wal(15,t)$
$Wal(13,t)$	0	0	1	0	1	1	$Wal(1,t) \oplus Wal(3,t) \oplus Wal(15,t)$
$Wal(14,t)$	0	0	1	0	0	1	$Wal(1,t) \oplus Wal(15,t)$
$Wal(15,t)$	0	0	1	0	0	0	$Wal(15,t)$
$Wal(16,t)$	0	1	1	0	0	0	$Wal(15,t) \oplus Wal(31,t)$
$Wal(17,t)$	0	1	1	0	0	1	$Wal(1,t) \oplus Wal(15,t) \oplus Wal(31,t)$
$Wal(18,t)$	0	1	1	0	1	1	$Wal(1,t) \oplus Wal(3,t) \oplus Wal(15,t) \oplus Wal(31,t)$
$Wal(19,t)$	0	1	1	0	1	0	$Wal(3,t) \oplus Wal(15,t) \oplus Wal(31,t)$
$Wal(20,t)$	0	1	1	1	1	0	$Wal(3,t) \oplus Wal(7,t) \oplus Wal(15,t) \oplus Wal(31,t)$
$Wal(21,t)$	0	1	1	1	1	1	$Wal(1,t) \oplus Wal(3,t) \oplus Wal(7,t) \oplus Wal(15,t) \oplus Wal(31,t)$
$Wal(22,t)$	0	1	1	1	0	1	$Wal(1,t) \oplus Wal(7,t) \oplus Wal(15,t) \oplus Wal(31,t)$
$Wal(23,t)$	0	1	1	1	0	0	$Wal(7,t) \oplus Wal(15,t) \oplus Wal(31,t)$
$Wal(24,t)$	0	1	0	1	0	0	$Wal(7,t) \oplus Wal(31,t)$
$Wal(25,t)$	0	1	0	1	0	1	$Wal(1,t) \oplus Wal(7,t) \oplus Wal(31,t)$
$Wal(26,t)$	0	1	0	1	1	1	$Wal(1,t) \oplus Wal(3,t) \oplus Wal(7,t) \oplus Wal(31,t)$
$Wal(27,t)$	0	1	0	1	1	0	$Wal(3,t) \oplus Wal(7,t) \oplus Wal(31,t)$
$Wal(28,t)$	0	1	0	0	1	0	$Wal(3,t) \oplus Wal(31,t)$
$Wal(29,t)$	0	1	0	0	1	1	$Wal(1,t) \oplus Wal(3,t) \oplus Wal(31,t)$
$Wal(30,t)$	0	1	0	0	0	1	$Wal(1,t) \oplus Wal(31,t)$
$Wal(31,t)$	0	1	0	0	0	0	$Wal(31,t)$

Table B- 2: The Walsh sequence expressions from $Wal(32,t)$ to $Wal(63,t)$ in function of the primary sequences

	$rad(6,t)=Wal(63,t)$	$rad(5,t)=Wal(31,t)$	$rad(4,t)=Wal(15,t)$	$rad(3,t)=Wal(7,t)$	$rad(2,t)=Wal(3,t)$	$rad(1,t)=Wal(1,t)$	Walsh sequence expressed in function of the primary Walsh sequences
Bit of the Gray code	g_6	g_5	g_4	g_3	g_2	g_1	
$Wal(32,t)$	1	1	0	0	0	0	$Wal(31,t) \oplus Wal(63,t)$
$Wal(33,t)$	1	1	0	0	0	1	$Wal(1,t) \oplus Wal(31,t) \oplus Wal(63,t)$
$Wal(34,t)$	1	1	0	0	1	1	$Wal(1,t) \oplus Wal(3,t)Wal(31,t) \oplus Wal(63,t)$
$Wal(35,t)$	1	1	0	0	1	0	$Wal(3,t) \oplus Wal(31,t) \oplus Wal(63,t)$
$Wal(36,t)$	1	1	0	1	1	0	$Wal(3,t) \oplus Wal(7,t)Wal(31,t) \oplus Wal(63,t)$
$Wal(37,t)$	1	1	0	1	1	1	$Wal(1,t) \oplus Wal(3,t) \oplus Wal(7,t) \oplus Wal(31,t) \oplus Wal(63,t)$
$Wal(38,t)$	1	1	0	1	0	1	$Wal(1,t) \oplus Wal(7,t) \oplus Wal(31,t) \oplus Wal(63,t)$
$Wal(39,t)$	1	1	0	1	0	0	$\oplus Wal(7,t) \oplus Wal(31,t) \oplus Wal(63,t)$
$Wal(40,t)$	1	1	1	1	0	0	$Wal(7,t) \oplus Wal(15,t) \oplus Wal(31,t) \oplus Wal(63,t)$
$Wal(41,t)$	1	1	1	1	0	1	$Wal(1,t) \oplus Wal(7,t) \oplus Wal(15,t) \oplus Wal(31,t) \oplus Wal(63,t)$
$Wal(42,t)$	1	1	1	1	1	1	$Wal(1,t) \oplus Wal(3,t) \oplus Wal(7,t) \oplus Wal(15,t) \oplus Wal(31,t) \oplus Wal(63,t)$
$Wal(43,t)$	1	1	1	1	1	0	$Wal(3,t) \oplus Wal(7,t) \oplus Wal(15,t) \oplus Wal(31,t) \oplus Wal(63,t)$
$Wal(44,t)$	1	1	1	0	1	0	$Wal(3,t) \oplus Wal(15,t) \oplus Wal(31,t) \oplus Wal(63,t)$
$Wal(45,t)$	1	1	1	0	1	1	$Wal(1,t) \oplus Wal(3,t) \oplus Wal(15,t) \oplus Wal(31,t) \oplus Wal(63,t)$
$Wal(46,t)$	1	1	1	0	0	1	$Wal(1,t) \oplus Wal(15,t) \oplus Wal(31,t) \oplus Wal(63,t)$
$Wal(47,t)$	1	1	1	0	0	0	$Wal(15,t) \oplus Wal(31,t) \oplus Wal(63,t)$
$Wal(48,t)$	1	0	1	0	0	0	$Wal(15,t) \oplus Wal(63,t)$
$Wal(49,t)$	1	0	1	0	0	1	$Wal(1,t) \oplus Wal(15,t) \oplus Wal(63,t)$
$Wal(50,t)$	1	0	1	0	1	1	$Wal(1,t) \oplus Wal(3,t) \oplus Wal(15,t) \oplus Wal(63,t)$
$Wal(51,t)$	1	0	1	0	1	0	$Wal(3,t) \oplus Wal(15,t) \oplus Wal(63,t)$
$Wal(52,t)$	1	0	1	1	1	0	$Wal(3,t) \oplus Wal(7,t) \oplus Wal(15,t) \oplus Wal(63,t)$
$Wal(53,t)$	1	0	1	1	1	1	$Wal(1,t) \oplus Wal(3,t) \oplus Wal(7,t) \oplus Wal(15,t) \oplus Wal(63,t)$
$Wal(54,t)$	1	0	1	1	0	1	$Wal(1,t) \oplus Wal(7,t) \oplus Wal(15,t) \oplus Wal(63,t)$
$Wal(55,t)$	1	0	1	1	0	0	$Wal(7,t) \oplus Wal(15,t) \oplus Wal(63,t)$
$Wal(56,t)$	1	0	0	1	0	0	$Wal(7,t) \oplus Wal(63,t)$
$Wal(57,t)$	1	0	0	1	0	1	$Wal(1,t) \oplus Wal(7,t) \oplus Wal(63,t)$
$Wal(58,t)$	1	0	0	1	1	1	$Wal(1,t) \oplus Wal(3,t) \oplus Wal(7,t) \oplus Wal(63,t)$
$Wal(59,t)$	1	0	0	1	1	0	$Wal(3,t) \oplus Wal(7,t) \oplus Wal(63,t)$
$Wal(60,t)$	1	0	0	0	1	0	$Wal(3,t) \oplus Wal(63,t)$
$Wal(61,t)$	1	0	0	0	1	1	$Wal(1,t) \oplus Wal(3,t)Wal(63,t)$
$Wal(62,t)$	1	0	0	0	0	1	$Wal(1,t) \oplus Wal(63,t)$
$Wal(63,t)$	1	0	0	0	0	0	$Wal(63,t)$

