Performance prediction of a future silicon-germanium heterojunction bipolar transistor technology using a heterogeneous set of simulation tools and approaches

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From **Tommy ROSENBAUM**

Performance prediction of a future silicon-germanium heterojunction bipolar transistor technology using a heterogeneous set of simulation tools and approaches

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猿も木から落ちる。

Abstract

Bipolar complementary metal-oxide-semiconductor (BiCMOS) processes can be considered as the most general solution for RF products, as they combine the mature manufacturing tools of CMOS with the speed and drive capabilities of silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs). HBTs in turn are major contenders for partially filling the terahertz gap, which describes the range in which the frequencies generated by transistors and lasers do not overlap (approximately 0.3 THz to 30 THz). To evaluate the capabilities of such future devices, a reliable prediction methodology is desirable. Using a heterogeneous set of simulation tools and approaches allows to achieve this goal successively and is beneficial for troubleshooting. Various scientific fields are combined, such as technology computer-aided design (TCAD), compact modeling and parameter extraction.

To create a foundation for the simulation environment and to ensure reproducibility, the used material models of the hydrodynamic and drift-diffusion approaches are introduced in the beginning of this thesis. The physical models are mainly based on literature data of Monte Carlo (MC) or deterministic simulations of the Boltzmann transport equation (BTE). However, the TCAD deck must be calibrated on measurement data too for a reliable performance prediction of HBTs. The corresponding calibration approach is based on measurements of an advanced SiGe HBT technology for which a technology-specific parameter set of the HICUM/L2 compact model is extracted for the high-speed, medium-voltage and high-voltage transistor versions. With the help of the results, one-dimensional transistor characteristics are generated that serve as reference for the doping profile and model calibration. By performing elaborate comparisons between measurement-based reference data and simulations, the thesis advances the state-of-the-art of TCAD-based predictions and proofs the feasibility of the approach.

Finally, the performance of a future technology in 28 nm is predicted by applying the heterogeneous methodology. On the basis of the TCAD results, bottlenecks of the technology are identified.

Zusammenfassung

Bipolare komplementäre Metall-Oxid-Halbleiter (BiCMOS) Prozesse bieten hervorragende Rahmenbedingungen um Hochfrequenzanwendungen zu realisieren, da sie die fortschrittliche Fertigungstechnik von CMOS mit der Geschwindigkeit und Treiberleistung von Silizium-Germanium (SiGe) Heterostruktur-Bipolartransistoren (HBTs) verknüpfen. Zudem sind HBTs bedeutende Wettbewerber für die teilweise Überbrückung der Terahertz-Lücke, der Frequenzbereich zwischen Transistoren ($< 0.3\,\mathrm{THz}$) und Lasern ($> 30\,\mathrm{THz}$). Um die Leistungsfähigkeit solcher zukünftigen Bauelemente zu bewerten, ist eine zuverlässige Methodologie zur Vorhersage notwendig. Die Verwendung einer heterogenen Zusammenstellung von Simulationstools und Lösungsansätzen erlaubt es dieses Ziel schrittweise zu erreichen und erleichtert die Fehlerfindung. Verschiedene wissenschaftliche Bereiche werden kombiniert, wie zum Beispiel der rechnergestützte Entwurf für Technologie (TCAD), die Kompaktmodellierung und Parameterextraktion.

Die verwendeten Modelle des hydrodynamischen Simulationsansatzes werden zu Beginn der Arbeit vorgestellt, um die Simulationseinstellung zu erläutern und somit die Nachvollziehbarkeit für den Leser zu verbessern. Die physikalischen Modelle basieren hauptsächlich auf Literaturdaten von Monte Carlo (MC) oder deterministischen Simulationen der Boltzmann-Transportgleichung (BTE). Für eine zuverlässige Vorhersage der Eigenschaften von HBTs muss die TCAD Konfiguration jedoch zusätzlich auf der Grundlage von Messdaten kalibriert werden. Der zugehörige Ansatz zur Kalibrierung beruht auf Messungen einer fortschrittlichen SiGe HBT Technologie, für welche ein technologiespezifischer HICUM/L2 Parametersatz für die high-speed, medium-voltage und high-voltage Transistoren extrahiert wird. Mit diesen Ergebnissen werden eindimensionale Transistorcharakteristiken generiert, die als Referenzdaten für die Kalibrierung von Dotierungsprofilen und physikalischer Modelle genutzt werden. Der ausführliche Vergleich dieser Referenz- und Messdaten mit Simulationen geht über den Stand der Technik TCAD-basierender Vorhersagen hinaus und weist die Machbarkeit des heterogenen Ansatzes nach.

Schließlich wird die Leistungsfähigkeit einer zukünftigen Technologie in 28 nm unter Anwendung der heterogenen Methodik vorhergesagt. Anhand der TCAD Ergebnisse wird auf Engpässe der Technologie hingewiesen.

Résumé

Les procédés bipolaires semi-conducteurs complémentaires à oxyde de métal (BiCMOS) peuvent être considérés comme étant la solution la plus générale pour les produits RF car ils combinent la fabrication sophistiquée du CMOS avec la vitesse et les capacités de conduction des transistors bipolaires silicium-germanium (SiGe) à hétérojonction (HBT). Les HBTs, réciproquement, sont les principaux concurrents pour combler partiellement l'écart de térahertz qui décrit la plage dans laquelle les fréquences générées par les transistors et les lasers ne se chevauchent pas (environ 0.3 THz à 30 THz). Afin d'évaluer les capacités de ces dispositifs futurs, une méthodologie de prévision fiable est souhaitable. L'utilisation d'un ensemble hétérogène d'outils et de méthodes de simulations permet d'atteindre successivement cet objectif et est avantageuse pour la résolution des problèmes. Plusieurs domaines scientifiques sont combinés, tel que la technologie de conception assistée par ordinateur (TCAO), la modélisation compacte et l'extraction des paramètres.

Afin de créer une base pour l'environnement de simulation et d'améliorer la confirmabilité pour les lecteurs, les modèles de matériaux utilisés pour les approches hydrodynamiques et de diffusion par conduction sont introduits dès le début de la thèse. Les modèles physiques sont principalement fondés sur des données de la littérature basées sur simulations Monte Carlo (MC) ou des simulations déterministes de l'équation de transport de Boltzmann (BTE). Néanmoins, le module de TCAO doit être aussi étalonné sur les données de mesure pour une prévision fiable des performances des HBTs. L'approche correspondante d'étalonnage est basée sur les mesures d'une technologie de pointe de HBT SiGe pour laquelle un ensemble de paramètres spécifiques à la technologie du modèle compact HICUM/L2 est extrait pour les versions du transistor à haute vitesse, moyenne et haute tension. En s'aidant de ces résultats, les caractéristiques du transistor unidimensionnel qui sont générées servent de référence pour le profil de dopage et l'étalonnage du modèle. En élaborant des comparaisons entre les données de références basées sur les mesures et les simulations, la thèse fait progresser l'état actuel des prévisions basées sur la technologie CAO et démontre la faisabilité de l'approche.

Enfin, une technologie future de 28 nm performante est prédite en appliquant la méthodologie hétérogène. Sur la base des résultats de TCAO, les limites de la technologie sont soulignées.

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List of Symbols

Abbreviations

1D	One-dimensional
2D	Two-dimensional
3D	Three-dimensional
AMS	Analog mixed signal
BGN	Band gap narrowing
BiCMOS	Bipolar CMOS
BJT	Bipolar junction transistor
BTE	Boltzmann transport equation
CEDIC	Chair for Electron Devices and Integrated Circuits
CMOS	Complementary metal-oxide-semiconductor
DD	Drift-diffusion
DoS	Density of states
EBL	Electron beam lithography
EDX	Electron dispersive X-ray spectroscopy
FoM	Figure of merit
FRA	Full regional approach
GICCR	Generalized integral charge control relation
HBT	Heterojunction bipolar transistor
HD	Hydrodynamic
HEMT	High-electron-mobility transistor
HS	High speed
HV	High voltage

IC	Integrated circuit
II	Impact ionization
III/V	Material composition of the third and fifth group of the periodic table
InP	Indium phosphide
ITRS	International technology roadmap of semiconductors
MC	Monte Carlo
MOSFET	Metal-oxide-semiconductor field-effect transistor
MV	Medium voltage
NBR	Neutral base recombination
PoA	Perimeter over area
RF	Radio frequency
SCR	Space charge region
SH	Self-heating
SIC	Selectively implanted collector
SiGe	Silicon-germanium
SIMS	Secondary ion mass spectrometry
SRH	Shockley-Reed-Hall, the inventors of the corresponding recombination model
STI	Shallow trench isolation
TCAD	Technology computer-aided design
TEM	Transmission electron microscopy
TUD	Technische Universität Dresden
WPE	Well proximity effect

Variables

δ_{C}	Collector current spreading angle
$\overline{C}_{\mathrm{jCi}}$	Internal base collector junction capacitance
$\overline{C}_{\mathrm{jEi}}$	Internal base emitter junction capacitance
τ_{f0}	Low-bias forward transit time
τ_{f}	Forward transit time
ε_0	Permittivity in vacuum
ε_{r}	Relative permittivity

A_{E0}	Actual emitter area
b_{E0}	Actual emitter width
b_{E}	Emitter width
B_{f}	Forward DC current gain: $I_{\mathrm{C}}/I_{\mathrm{B}}$
BV_{CBO}	Open emitter breakdown voltage for HBTs
BV_{CEO}	Open base breakdown voltage for HBTs
BV_{DSS}	Leakage related breakdown voltage for MOSFETs
C'_{jCx}	External base collector junction capacitance
C'_{jEp}	Peripheral base emitter junction capacitance
C_{jS}	Collector substrate junction capacitance
f_{ext}	Extraction frequency
f_{meas}	Measurement frequency
f_{max}	Maximum oscillation frequency
f_{t}	Transit frequency
g_{m}	Internal transconductance
I_{avl}	Avalanche current
I_{B}	Base current
I_{CK}	Critical current
I_{C}	Collector current
k_{B}	Boltzmann constant
l_{E0}	Actual emitter length
l_{G}	Gate length
q	Elementary charge
Q_{jCi}	Base collector depletion charge
Q_{jEi}	Base emitter depletion charge
Q_{p0}	Zero-bias hole charge
Q_{p}	Hole charge
R_{Bi}	Internal base resistance
R_{Bx}	External base resistance
R_{Cx}	External collector resistance
R_{E}	Emitter resistance
R_{th}	Thermal resistance
T_0	Reference temperature

T_{amb}	Ambient temperature
V_{BC}	Base collector voltage
V_{BE}	Base emitter voltage
V_{CE}	Collector emitter voltage
w_{char}	Characteristic size

CHAPTER 1

Introduction

1.1 Motivation

The demand for increased functionality and speed of modern communication systems drives the evolution of RF technologies, such as RF-CMOS, III/V HBT, III/V HEMT or SiGe BiCMOS technologies (featuring both CMOS and SiGe HBTs). Within the publicly released RF/AMS tables, the ITRS [1] estimates the performance of all these technologies 15 years ahead of the current point in time. Each of the technologies has particular characteristics in comparison to the rest of the group:

- RF-CMOS technologies usually feature a state-of-the-art lithography node. Inherently, a reduced device size for large functional densities, a large number of metal layers and digital CMOS are available. However, typically the device speed is at the lower end of the competitors for a fixed feature size and the performance drop caused by interconnects becomes increasingly larger compared to the other technologies [2].
- III/V HBT and HEMT technologies currently offer the fastest devices available with maximum oscillation frequencies in the THz range for prototype devices [3,4]. The HEMT devices require electron beam lithogra-

phy (EBL) for achieving these speeds. In case of non-EBL systems, the node size is typically much larger than for current RF-CMOS lithography and thus, limits the functional density and device speed. As III/V technologies are not silicon based, they cannot be easily combined with CMOS for improving the feature size.

- BiCMOS technologies provide access to both high-density digital CMOS and the superior RF capabilities of SiGe HBTs. Although the performance does not reach the speed of for III/V technologies, BiCMOS processes can be considered as the most general solution for RF products, as they combine the mature manufacturing of CMOS with the speed and drive capabilities of SiGe HBTs.

The consideration of which option is most suitable for a given application is not trivial and depends on various factors; such as cost, design specifications (performance) and circuit volume. For speed limited circuit applications, e.g. in data communication or radar applications, device performance is becoming more important than other factors. Useful device metrics in this field are the transit frequency f_t and maximum oscillation frequency f_max for which a literature study is presented in figures 1.1 and 1.2 for RF-CMOS, SiGe HBTs and InP HBTs as an example for a fast III/V technology.

The mentioned figures of merit (FoMs) depend on the characteristic size of the respective device w_char. For RF-CMOS w_char is the gate length l_G, whereas for HBTs an appropriate selection is more difficult. HBT-relevant information about layer thickness is usually confidential and therefore inaccessible in publications. Consequently, the emitter width b_E was selected for the literature study in this introduction, as it is the most important lateral dimension that corresponds to the feature size and can be accessed.

Two factors influence the significance of these data: *(i)* Occasionally, w_char is not accurately specified in the publications. For example, instead of the actual emitter width[1] the drawn dimension is listed. *(ii)* Of course, other factors than the characteristic width can change performance. For example,

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[1] The actual emitter width b_E0 corresponds to the drawn emitter width b_drawn of the integrated circuit (IC) mask layout reduced by the width of the inside base emitter spacers.

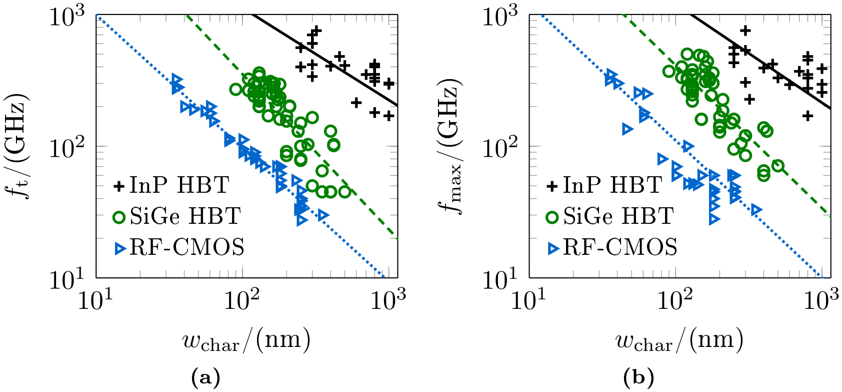


Figure 1.1: Results of a literature study covering a variety of publications for InP-HBTs, SiGe-HBTs and RF-CMOS [5–72]. **(a)** f_t vs. w_{char} and **(b)** $f_{\max}$ vs. w_{char} for the three different types of technologies.

for HBTs the vertical profile influences transistor speed and gain. *(i)* and *(ii)* lead to a data spread that can become significant, especially for HBTs. Nevertheless, the data are separated in three distinct areas corresponding to the respective technologies and are aligned fairly well. The extrapolated lines show the trend for all three technologies and were obtained by a robust fitting procedure to minimize the influence of outliers. Note the slightly different slopes indicating a somewhat more optimistic forecast for SiGe HBTs.

Judging from the data in fig. 1.1, the characteristic width required for a transistor with $f_t = 1\,\mathrm{THz}$ can be determined from the extrapolated lines as 10 nm, 41 nm and 120 nm for RF-CMOS, SiGe HBTs and InP HBTs, respectively. Similarly, the procedure is repeated for $f_{\max} = 1\,\mathrm{THz}$ leading to 12 nm, 44 nm and 130 nm. For InP HBTs the 1 THz barrier has been reached already at an emitter width of about 130 nm [4] aligning well with the studied data.

At a first glance, fig. 1.2 would be interpreted as a stalemate between SiGe HBTs and RF-CMOS in terms of f_t (contrary to fig. 1.1). However, when taking into account that the underlying characteristic width is more than three node steps ahead for RF-CMOS, it becomes clear that the performance can only be achieved with advanced manufacturing. Note that the diversity of the processes included in this study yields a strong data spread against time

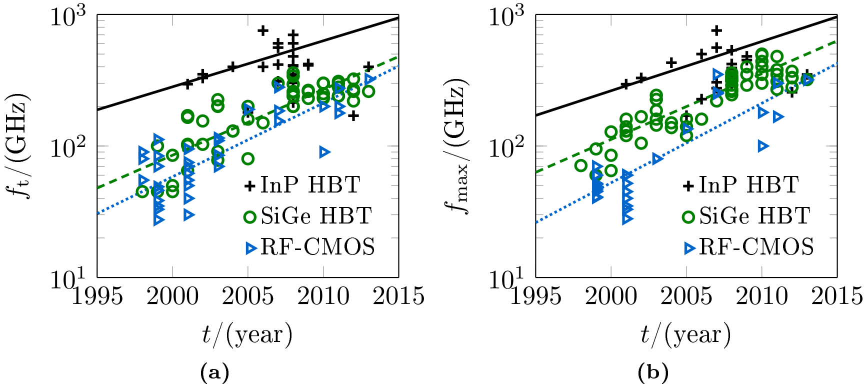


Figure 1.2: Results of a literature study covering a variety of publications for InP-HBTs, SiGe-HBTs and RF-CMOS [5–72]. **(a)** f_t vs. time and **(b)** f_max vs. time for the three different types of technologies.

reducing the significance of the extrapolations. A simple extrapolation was performed on the figure data: $f_\mathrm{t} = 1\,\mathrm{THz}$ is reached in 2022, 2021 and 2016 for RF-CMOS, SiGe HBTs and InP HBTs, respectively. Similarly, $f_\mathrm{max} = 1\,\mathrm{THz}$ is reached in 2022, 2019 and 2015.

These numbers could turn out to be somewhat too optimistic, as there might not be sufficient demand for circuits in this operating region, which would be necessary to keep production costs low for non-prototyping processes and to trigger the development of such processes. Furthermore, transistor development is expected to run into physical limitations for small dimensions.

In addition to the small signal behavior, the permissible voltage rating is important in circuit design for meeting DC and RF power delivery constraints, as well as reliability requirements. Suitable FoMs for the assessment of these circuit requirements are the breakdown voltages BV_CEO and BV_CBO for HBTs and BV_DSS for MOSFETs. Note that for CMOS a breakdown voltage like BV_CEO cannot be defined, as the Gate current under typical DC bias conditions (i.e. negligible gate tunneling and leakage) is zero. Therefore, only BV_CBO and BV_DSS are comparable FoMs, as they are measured in the same hierarchical way. Unfortunately, the amount of data for BV_DSS in the analyzed papers is small and therefore, no results can be presented here. Fig. 1.3

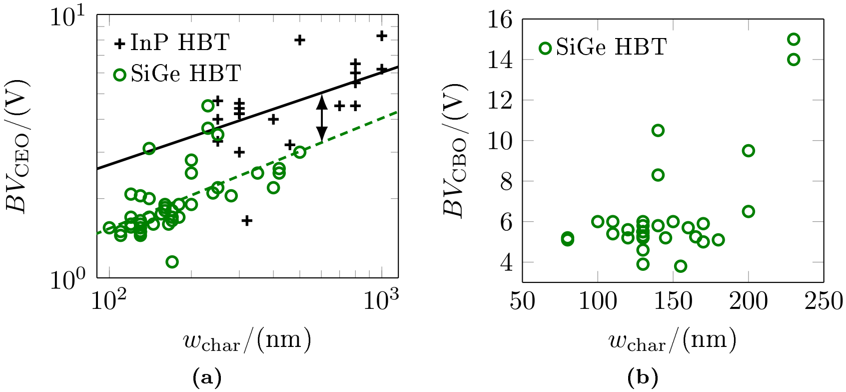
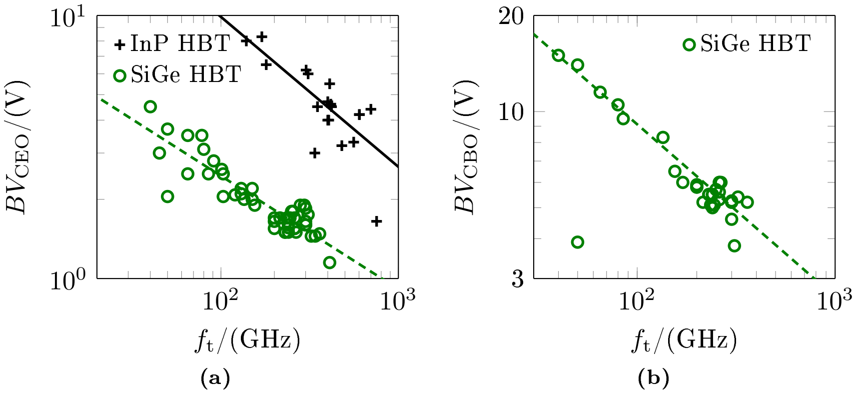


Figure 1.3: Results of a literature study covering a variety of publications for InP-HBTs and SiGe-HBTs [5–72]. **(a)** BV_{CEO} vs. w_{char} and **(b)** BV_{CBO} vs. w_{char} for SiGe HBTs only, due to the limited amount of data for InP HBTs.

shows the results of the literature study for the breakdown voltages BV_{CEO} and BV_{CBO}.

Even if the data for BV_{CEO} in fig. 1.3 are trending relatively well, it needs to be noted that there is no direct physical relation between breakdown mechanisms and the characteristic width. Instead, the reasons for the good alignment are an increasing current gain B_{f} for mature processes and the increasing collector doping required for speed improvements over the past years. Newer – and therefore smaller – high speed (HS) transistors typically have a smaller base current and a larger collector doping leading to a lower breakdown voltage. Contrary to BV_{CEO}, BV_{CBO} does not depend on the base current behavior, but on the breakdown behavior of the reverse biased BC diode making BV_{CBO} a true measure for the transistor voltage limit. A negative base current is tolerable for some applications and therefore BV_{CEO} can be exceeded to improve device performance [73].

Typically, the current gain of InP HBTs is more than a decade smaller than the current gain of SiGe HBTs. This leads to an increase of BV_{CEO} and the gap indicated in fig. 1.3. Also, it clearly demonstrates that BV_{CEO} is less significant for the voltage limit of a transistor because it makes break-



(a) **(b)**

Figure 1.4: Results of a literature study covering a variety of publications for InP-HBTs and SiGe-HBTs [5–72]. **(a)** BV_{CEO} vs. f_{t} and **(b)** BV_{CBO} vs. f_{t} for SiGe HBTs only, due to the limited amount of data for InP HBTs.

down depend on the base current – i.e. a transistor with a negligible base current would have a breakdown voltage close to zero. Consequently, the gap between BV_{CEO} and BV_{CBO} is much smaller for InP HBTs as illustrated by the standard text book equation [74]

$$BV_{\mathrm{CEO}} = BV_{\mathrm{CBO}} \left(\frac{1}{1 + B_{\mathrm{f}}} \right)^{\frac{1}{k}} , \tag{1.1}$$

with the material and doping dependent factor k. The larger the current gain, the larger the discrepancy between the two breakdown voltages.

Fig. 1.4 shows the trend of the breakdown voltages against transit frequency as obtained from the literature study. The data for BV_{CBO} are trending very well because the base current does not influence this FoM. Conversely, the uncertainty for BV_{CEO} is somewhat larger. As the electric field increases with increasing collector doping, f_{t} improves but the breakdown voltage reduces: For a transistor with $f_{\mathrm{t}} = 1\,\mathrm{THz}$, BV_{CEO} decreases to 0.9 V and 2.7 V for SiGe and InP HBTs, respectively. Similarly, $f_{\mathrm{t}} = 1\,\mathrm{THz}$ can be reached at $BV_{\mathrm{CBO}} = 2.6\,\mathrm{V}$ for SiGe HBTs. The values indicate a reasonable voltage rating even for very fast transistors.

In summary, SiGe HBTs are one of the major contenders for high speed analog circuits with additional potential for development. The high transit frequency and maximum oscillation frequency at a relaxed feature size allow a cheap fabrication of fast circuits.

1.2 Overview

The main goal of this thesis is to establish a reliable methodology for the performance prediction of SiGe HBTs using a heterogeneous set of simulation tools and approaches. To accomplish this task, various scientific fields have to be combined: technology computer-aided design (TCAD), compact modeling, parameter extraction and device physics. The employed TCAD simulations are based on the numerical evaluation of transport and electrostatics in semiconductor devices and allow to predict the performance of one-dimensional (1D) and two-dimensional (2D) structures. Using such tools bears the risk of generating incorrect results after long simulation times and consuming many resources, which is why this first step of the prediction needs to be kept as simple as possible without compromising accuracy. Consequently, the considered 1D evaluations are based on complex simulation schemes (like the Boltzmann transport equation (BTE) or hydrodynamic (HD) transport), whereas the prediction of 2D components is based on drift-diffusion (DD) simulations.

The biggest disadvantage of a prediction, which is solely based on TCAD, is that circuit simulations (but also simulations of the complete 3D transistor structure) are not feasible. The structures would be too complex and time consuming for efficient circuit design. As a result, the chosen prediction approach uses a suitable compact model for describing the TCAD results analytically. This makes the prediction depend on accurate and robust extraction methods but allows to proceed with a compact model. A large portion of the thesis is therefore dedicated to the extraction of parameters for the compact model; the feasibility of the approach depends on it.

After the extraction of the technology specific parameters for the internal transistor region, external transistor elements – such as the spacer capacitances and external resistances – are added to the modelcard. This is realized with the help of additional TCAD tools and methods, but some of the elements cannot be predicted by the approaches employed in the work and need to be assumed (e.g. contact resistances).

For a meaningful prediction, it is necessary to assess the significance of the TCAD simulations. Therefore, a prediction dry run is performed for an existing bipolar technology. The calibration of the tools mainly focuses on the adjustment of doping profiles, as they have turned out to be the decisive factor for obtaining reliable results [75]. Nevertheless, the used material models of the simulations are important too and thus, are summarized in the beginning of the thesis. At the end of the dry run, a comparison with measurement data reveals the accuracy that can be expected from the method.

Finally, the thesis is concluded with the evaluation of a novel SiGe HBT architecture, which can serve as the next generation of bipolar transistors. The technology is demonstrated to exhibit promising RF performances in comparison to existing industry processes [76].

The thesis is structured as follows: Chapter 2 examines the used material models for the DD and HD based simulations. The extraction methodology, which is applicable to simulations, is presented in chapter 3 for measurement data of an advanced SiGe HBT technology. In chapter 4, the TCAD calibration is performed by matching doping profile and physical models to the extracted reference data and parameters. Finally, the prediction is performed for the mentioned process and a future architecture in chapter 5 before giving a conclusion and outlook in chapter 6.

CHAPTER 2

Simulation setup for advanced SiGe HBTs

2.1 Overview on device simulators

The final goal of the thesis is to predict the performance of future SiGe HBT technologies. To achieve this goal, a TCAD based approach is chosen using a heterogeneous set of simulation tools. Using a set of simulations instead of a single simulation run – which would have to cover all physical aspects at the same time – splits up the task and hence, simplifies prediction. This is especially useful for the calibration process because it helps to assign measured/extracted technology parameters to easy-to-comprehend simulation setups. The following list gives a short overview of the used simulation tools.

Chief is an in-house hydrodynamic (HD) simulator developed by the Chair for Electron Devices and Integrated Circuits (CEDIC) at Technische Universität Dresden (TUD) featuring 1D simulation capability at 300 K [77]. Doping profile descriptions and physical model parameters are fully accessible and can be manipulated easily.

DEVICE is an in-house mixed-mode drift-diffusion (DD) simulator of CEDIC featuring 3D simulation capability at arbitrary temperatures [78] with full access to the tool and source code. Therefore, new physical models and analytical profile definitions can be implemented.

POICAPS is an in-house Laplace simulator of CEDIC featuring 3D simulation capability used for the determination of parasitic capacitances [79]. Due to the relatively low complexity of the Laplace equation, larger systems with complex geometries can be simulated within a small time frame.

DEBOTS is an in-house deterministic Boltzmann transport equation (BTE) solver of CEDIC. It solves the BTE with the help of the box-integration method and the WENO approach [80]. Although the BTE offers a more physical approach for device simulations, it needs to be noted that a conformity between HD-based commercial simulators and a BTE tool cannot be established for arbitrary doping profiles and a single physical parameter set. Additionally, the runtime is about three decades longer (in comparison to HD simulations), which makes the tool unsuitable for intensive usage, e.g. for calibration purposes. Therefore, BTE solvers are mainly used for predictions, in which physical limitations play an increased role.

A single tool is not capable of meeting all requirements for the performance prediction of SiGe HBTs. Each tool has an unique area of application making it necessary to combine the results for a unified prediction. The details of this approach are shown in chapter 5.

2.2 Physical models

Ultimately, for a meaningful assessment of the performance of SiGe HBTs, calibrated physical models are required. As a starting point for the final goal of a calibrated TCAD deck, the parameters used for the models in the simulation tools are adjusted to match literature data. The calibration needs to cover all models used in the simulations: Models for mobility and energy relaxation times are adjusted to the Monte Carlo (MC) based reference of [81]. Next, parameters for the density of states (DoS) and saturation velocity are tuned according to [82]. Finally, the remaining device models, like the band gap and recombination, are illustrated.

2.2.1 Mobility as a function of doping

Mobility in silicon devices is a function of doping, germanium content, carbon content, strain, field and direction. It also depends on the carrier type (electrons/holes) and their type of abundance (majorities/minorities). For most approaches in literature, the model core consists of the standard Caughey-Thomas equation [83] for describing the low-field mobility

$$\mu_{\mathrm{lF}} = \mu_{\mathrm{min}} + \frac{\mu_{\mathrm{max}} - \mu_{\mathrm{min}}}{1 + \left(G/G_{\mathrm{ref}}\right)^{\alpha}}, \tag{2.1}$$

with the total doping $G = N_{\mathrm{A}}^{-} + N_{\mathrm{D}}^{+}$ and the model parameters μ_{min}, μ_{max}, G_{ref} and α. For low doping concentrations G/G_{ref} approaches zero and μ_{lF} tends to μ_{max}. Likewise, for large doping concentrations G/G_{ref} approaches infinity and μ_{lF} tends to μ_{min}. The slope of the transition depends on the parameter α. A schematic illustration of the equation is shown in fig. 2.1 for a single parameter combination.

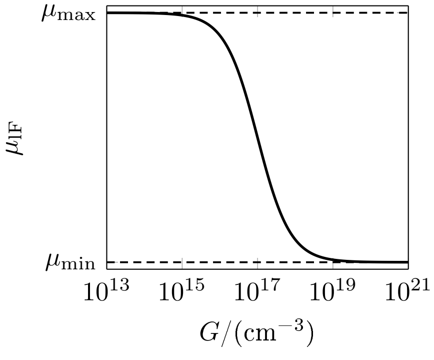


Figure 2.1: Schematic dependence of the mobility vs. doping for $\alpha = 1$ and $G_{\mathrm{ref}} = 10^{17}\,\mathrm{cm}^{-3}$ according to (2.1).

Mobility models implemented into device simulators use extended descriptions that also account for the type of abundance. An obvious approach is to use additional parameters to model abundance leading to a distinction of cases in the mobility description, as provided by Chief. For the reference model (Reggiani) and DEVICE, the abundance differentiation is taken into

Chief [77]

$$\mu_{\mathrm{lF}} = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left(G/G_{\mathrm{ref}}\right)^{\alpha}} \tag{2.2}$$

parameters: $\mu_{\max}$, G_{ref}, α and $\mu_{\min}$ for both majorities and minorities

DEVICE [78]

$$\begin{aligned}
\mu_{\mathrm{lF}} &= \mu_{\mathrm{f1,min}} + \frac{\mu_{\max} - \mu_{\mathrm{f1,min}}}{1 + \left(G/G_{\mathrm{ref}}\right)^{\alpha}} \\
\mu_{\mathrm{f1,min}} &= \mu_{\min}\left[1 + (r-1)\frac{N}{N+c}\right] \\
N &= \begin{cases} N_{\mathrm{A}}^{-} & \text{for electrons} \\ N_{\mathrm{D}}^{+} & \text{for holes} \end{cases} \\
c &= \begin{cases} n & \text{for electrons} \\ p & \text{for holes} \end{cases}
\end{aligned} \tag{2.3}$$

parameters: $\mu_{\max}$, G_{ref}, α, $\mu_{\min}$ and r

input: n as electron and p as hole density

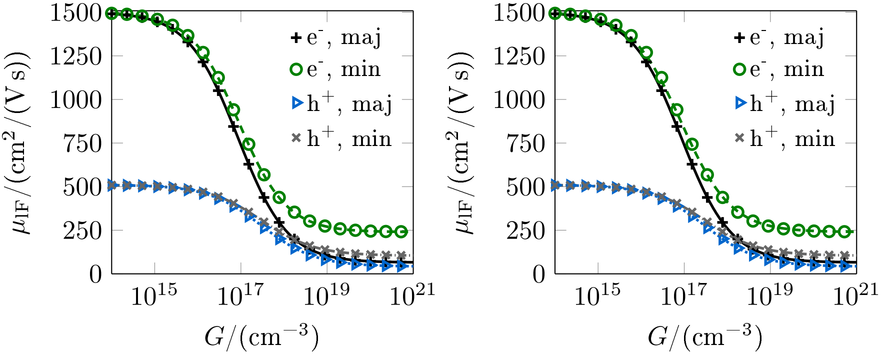
Reggiani [81, 84]

$$\begin{aligned}
\mu_{\mathrm{lF}} &= \mu_{\mathrm{f2,min}} + \frac{\mu_{\max} - \mu_{\mathrm{f2,min}}}{1 + \left(N_{\mathrm{A}}^{-}/N_{\mathrm{A,ref}}\right)^{\alpha_{\mathrm{A}}} + \left(N_{\mathrm{D}}^{+}/N_{\mathrm{D,ref}}\right)^{\alpha_{\mathrm{D}}}} \\
\mu_{\mathrm{f2,min}} &= \frac{\mu_{\mathrm{min,A}}N_{\mathrm{A}}^{-} + \mu_{\mathrm{min,D}}N_{\mathrm{D}}^{+}}{N_{\mathrm{A}}^{-} + N_{\mathrm{D}}^{+}}
\end{aligned} \tag{2.4}$$

parameters: $\mu_{\max}$, $N_{\mathrm{A,ref}}$, $N_{\mathrm{D,ref}}$, α_{A}, α_{D}, $\mu_{\mathrm{min,A}}$ and $\mu_{\mathrm{min,D}}$

account by additional analytical terms within the minimum mobility and the doping transition leading to a smooth description. The model equations are shown in (2.2), (2.3) and (2.4).

The mobility data presented in [81] are based on MC simulations and modeled with the Reggiani description. Most of the parameters can be transfered to Chief and DEVICE for ensuring a consistent model representation between the used simulators, while the parameter r does not exist in Chief and is used in DEVICE to represent the ratio between minority and majority mobility at very large doping concentrations. The mobility comparison for the out-of-plane case (transport in vertical/growth direction) and the corresponding parameters are shown in fig. 2.2 and tables 2.1 and 2.2, respectively.



(a) **(b)**

Figure 2.2: Low-field mobility of electrons and holes in silicon for both minority and majority carriers. Model comparison of μ_{lF} vs. $G = N_{\mathrm{A}}^{-} + N_{\mathrm{D}}^{+}$ for **(a)** Chief (lines) vs. [81] (markers) and **(b)** DEVICE (lines) vs. [81] (markers).

parameter (unit)	μ_{min} $(\mathrm{cm}^2/(\mathrm{V\,s}))$	μ_{max} $(\mathrm{cm}^2/(\mathrm{V\,s}))$	G_{ref} (cm^{-3})	α (1)	r (1)
Reggiani and Chief	65 (maj.) 240 (min.)	1500	$8.5 \cdot 10^{16}$ $9 \cdot 10^{16}$	0.75 0.78	-
DEVICE	65	1500	$8.5 \cdot 10^{16}$	0.75	3.69

Table 2.1: Consistent parameter set used for the out-of-plane mobility model for electrons in doped silicon based on reference [81].

parameter (unit)	μ_{min} $(\mathrm{cm}^2/(\mathrm{V\,s}))$	μ_{max} $(\mathrm{cm}^2/(\mathrm{V\,s}))$	G_{ref} (cm^{-3})	α (1)	r (1)
Reggiani and Chief	42 (maj.) 104 (min.)	510	$3 \cdot 10^{17}$ $3 \cdot 10^{17}$	0.7 0.7	-
DEVICE	42	510	$3 \cdot 10^{17}$	0.7	2.48

Table 2.2: Consistent parameter set used for the out-of-plane mobility model for holes in doped silicon based on reference [81].

2.2.2 Mobility as a function of germanium

When combining silicon with different materials to form an alloy, the mobility is altered. To calculate the resulting mobility, the rule of Matthiessen can be applied treating different mobilities like the concept of a parallel connection of several resistors. Additionally, nonlinear behavior can be introduced for covering different physical effects accurately, e.g. from various scattering mechanisms. (2.5) lists a simplified model from [81] for the SiGe composition system.

$$\frac{1}{\mu_{\mathrm{SiGe}}} = \underbrace{\frac{1-x_{\mathrm{mol}}}{\mu_{\mathrm{Si}}} + \frac{x_{\mathrm{mol}}}{\mu_{\mathrm{Ge}}}}_{1^{\mathrm{st}}\ \mathrm{term}} + \underbrace{\frac{x_{\mathrm{mol}}\left(1-x_{\mathrm{mol}}\right)}{C_0 + x_{\mathrm{mol}}C_1 + x_{\mathrm{mol}}^2 C_2}}_{2^{\mathrm{nd}}\ \mathrm{term}} \underbrace{\frac{1}{C_{\mathrm{z}}\left(z_{\mathrm{st}}\right)}}_{3^{\mathrm{rd}}\ \mathrm{term}}$$

$$C_{\mathrm{z}}\left(z_{\mathrm{st}}\right) = \chi_{\mathrm{st}} - \left(\chi_{\mathrm{st}} - 1\right)\exp\left(-\frac{z_{\mathrm{st}}}{z_1}\right) \quad \text{and} \quad z_{\mathrm{st}} = -0.1071 x_{\mathrm{mol}} - 0.0163 x_{\mathrm{mol}}^2 \tag{2.5}$$

The model consists of three main components:

- The standard Matthiessen rule (first term).
- The nonlinear extension to include the effect of alloy scattering for relaxed SiGe alloys (second term).
- The model to incorporate the impact of strain on mobility (third term).

In addition to this main description, the mobility at low doping concentrations is altered due to phonon interactions according to (2.6), which can be described by a change of μ_{max} that is taken into account for μ_{Si}.

$$\begin{aligned} &\overset{\text{for electrons}}{\boxed{\mu_{\mathrm{max}}\left(z\right)}} = \mu_{\mathrm{max,M1}} + \frac{\mu_{\mathrm{max,M2}} - \mu_{\mathrm{max,M1}}}{1 + \exp\left[\left(z_{\mathrm{st}} - z_0\right)\beta\right]} \\ &\overset{\text{for holes}}{\boxed{\mu_{\mathrm{max}}\left(z\right)}} = \mu_{\mathrm{max,M3}} + \left(\frac{z_{\mathrm{st}}}{z_0}\right)^2 \end{aligned} \tag{2.6}$$

Even if the description seems fairly complex, there is only a single quantity that serves as input to the model: x_{mol} is the germanium mole fraction within

parameter (unit)	C_0 ($\mathrm{cm^2/(V\,s)}$)	C_1 ($\mathrm{cm^2/(V\,s)}$)	C_2 ($\mathrm{cm^2/(V\,s)}$)	χ_{st} (1)
value	120	0	0	2.2
parameter (unit)	z_0 (1)	z_1 (1)	$\mu_{\mathrm{max,M1}}$ ($\mathrm{cm^2/(V\,s)}$)	$\mu_{\mathrm{max,M2}}$ ($\mathrm{cm^2/(V\,s)}$)
value	0	0.01	700	2300

Table 2.3: Parameters from the reference [81] for the out-of-plane mobility model for electrons in biaxially strained SiGe.

parameter (unit)	C_0 ($\mathrm{cm^2/(V\,s)}$)	C_1 ($\mathrm{cm^2/(V\,s)}$)	C_2 ($\mathrm{cm^2/(V\,s)}$)	χ_{st} (1)
value	60	70	170	2.1
parameter (unit)	z_0 (1)	z_1 (1)	$\mu_{\mathrm{max,M3}}$ ($\mathrm{cm^2/(V\,s)}$)	
value	0.0015	0.05	510	

Table 2.4: Parameters from the reference [81] for the out-of-plane mobility model for holes in biaxially strained SiGe.

the limits $0 \leq x_{\mathrm{mol}} \leq 1$ and C_0, C_1, C_2, χ_{st}, z_1, z_0, β, $\mu_{\mathrm{max,M1}}$, $\mu_{\mathrm{max,M2}}$ and $\mu_{\mathrm{max,M3}}$ are material parameters. The limits

$$\lim_{x_{\mathrm{mol}}\to 0} \mu_{\mathrm{SiGe}} = \mu_{\mathrm{Si}} \qquad \text{and} \qquad \lim_{x_{\mathrm{mol}}\to 1} \mu_{\mathrm{SiGe}} = \mu_{\mathrm{Ge}} \tag{2.7}$$

show that the additional terms do not affect the result for pure silicon or germanium. All related parameters of the model are listed in tables 2.3 and 2.4.

The model description is a comprehensive and successive approach that captures physical effects separately. Chief and DEVICE do not offer such a in-depth mobility description, but their simplified method still allows to model the SiGe composition system. In DEVICE, the model parameters μ_{max} and μ_{min} of (2.3) are replaced by generic quadratic functions of the mole fraction x_{mol} as shown in (2.8).

DEVICE [78]

$$\begin{aligned}\mu_{\text{max,f}}\left(x_{\text{mol}}\right) &= \mu_{\text{max}} + a_{\text{max}} x_{\text{mol}} + b_{\text{max}} x_{\text{mol}}^2 \\ \mu_{\text{min,f}}\left(x_{\text{mol}}\right) &= \mu_{\text{min}} + a_{\text{min}} x_{\text{mol}} + b_{\text{min}} x_{\text{mol}}^2\end{aligned} \tag{2.8}$$

parameters: μ_{max}, a_{max}, b_{max}, μ_{min}, a_{min} and b_{min} (abundance independent)

The model for Chief, like the one in [81], is based on BTE simulation results and therefore, uses an exponential description, see (2.9).

Chief [77]

$$\begin{aligned}\mu_{\text{max,f}}\left(x_{\text{mol}}\right) &= \mu_{\text{max}} + c_{\text{max}}\left[1 - \exp\left(-\frac{x_{\text{mol}}}{x_{\text{max}}}\right)\right] + a_{\text{max}} x_{\text{mol}} \\ \mu_{\text{min,f}}\left(x_{\text{mol}}\right) &= \mu_{\text{min}} + c_{\text{min}}\left[1 - \exp\left(-\frac{x_{\text{mol}}}{x_{\text{min}}}\right)\right] + a_{\text{min}} x_{\text{mol}} \\ \log_{10}\left(\frac{G_{\text{ref}}}{\text{cm}^{-3}}\right) &= a_G x_{\text{mol}} + b_G x_{\text{mol}}^2 + c_G x_{\text{mol}}^3 + d_G\end{aligned} \tag{2.9}$$

parameters: μ_{max}, a_{max}, c_{max}, x_{max}, μ_{min}, a_{min}, c_{min}, x_{min}, a_G, b_G, c_G and d_G for both majorities and minorities

Both models were adjusted to the reference (2.5) by means of optimization, with the corresponding comparisons shown in figures 2.3 and 2.4. Note that μ_{max} is identical for both types of abundance and hence, no distinction is made in the figures.

For the optimization, the following steps were carried out resulting in the parameters of tables 2.5 and 2.6:

(i) The parameters for the μ_{max} and μ_{min} descriptions were tuned for both Chief and DEVICE minimizing the least-square error with respect to (2.5) and therefore, the behavior for very low and very high doping vs. mole fraction is fixed.

(ii) For Chief, the model for G_{ref} is adjusted for the best overall fit in the relevant doping region of $10^{14}\ \text{cm}^{-3} \leq G \leq 10^{21}\ \text{cm}^{-3}$ and the considered mole fraction region of $0 \leq x_{\text{mol}} \leq 0.4$ while keeping the result of the previous step.

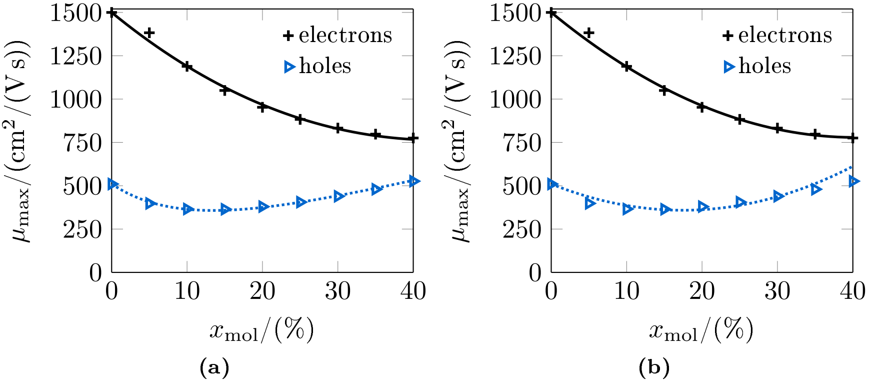


Figure 2.3: Out-of-plane mobility of biaxially strained SiGe for electrons and holes at low doping concentrations. Model comparison of $\mu_{\max}$ vs. x_{mol} for **(a)** Chief (lines) vs. [81] (markers) and **(b)** DEVICE (lines) vs. [81] (markers).

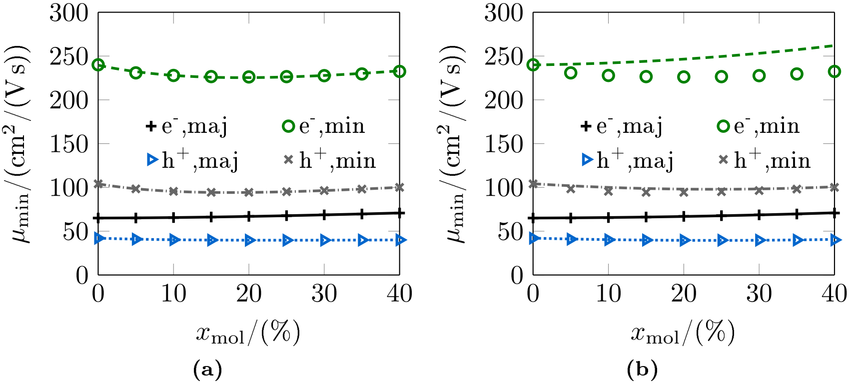


Figure 2.4: Out-of-plane mobility of biaxially strained SiGe for electrons and holes at very high doping concentrations. Model comparison of $\mu_{\min}$ vs. x_{mol} for **(a)** Chief (lines) vs. [81] (markers) and **(b)** DEVICE (lines) vs. [81] (markers).

parameter (Chief)	μ_{max}	a_{max}	c_{max}
(unit)	$(\mathrm{cm}^2/(\mathrm{V\,s}))$	$(\mathrm{cm}^2/(\mathrm{V\,s}))$	$(\mathrm{cm}^2/(\mathrm{V\,s}))$
value (maj.)	1500	10652	-21359
value (min.)			
parameter (Chief)	x_{max}	μ_{min}	a_{min}
(unit)	(1)	$(\mathrm{cm}^2/(\mathrm{V\,s}))$	$(\mathrm{cm}^2/(\mathrm{V\,s}))$
value (maj.)	1.502	65	30.99
value (min.)		239.5	87.42
parameter (Chief)	c_{min}	x_{min}	a_G
(unit)	$(\mathrm{cm}^2/(\mathrm{V\,s}))$	(1)	(1)
value (maj.)	-8.98	0.298	5.07
value (min.)	-45.7	0.170	4.72
parameter (Chief)	b_G	c_G	d_G
(unit)	(1)	(1)	(1)
value (maj.)	-15.5	16.12	16.93
value (min.)	-14.75	16.03	16.95
parameter (DEV.)	μ_{max}	a_{max}	b_{max}
(unit)	$(\mathrm{cm}^2/(\mathrm{V\,s}))$	$(\mathrm{cm}^2/(\mathrm{V\,s}))$	$(\mathrm{cm}^2/(\mathrm{V\,s}))$
value (maj.)	1500	-3579	4442
value (min.)			
parameter (DEV.)	μ_{min}	a_{min}	b_{min}
(unit)	$(\mathrm{cm}^2/(\mathrm{V\,s}))$	$(\mathrm{cm}^2/(\mathrm{V\,s}))$	$(\mathrm{cm}^2/(\mathrm{V\,s}))$
value (maj.)	65	2.97	30
value (min.)	$65 \cdot 3.69$		

Table 2.5: Consistent parameter set used for the out-of-plane mobility model of electrons for biaxially strained SiGe in DEVICE and Chief based on reference [81].

parameter (Chief)	μ_{max}	a_{max}	c_{max}
(unit)	(cm^2/(V s))	(cm^2/(V s))	(cm^2/(V s))
value (maj.)	510	1001	-386.1
value (min.)			
parameter (Chief)	x_{max}	μ_{min}	a_{min}
(unit)	(1)	(cm^2/(V s))	(cm^2/(V s))
value (maj.)	0.0986	42	4.37
value (min.)		104	49.13
parameter (Chief)	c_{min}	x_{min}	a_G
(unit)	(cm^2/(V s))	(1)	(1)
value (maj.)	-4.00	0.120	3.48
value (min.)	-24.77	0.127	3.02
parameter (Chief)	b_G	c_G	d_G
(unit)	(1)	(1)	(1)
value (maj.)	-8.85	7.03	17.48
value (min.)	-7.54	6.43	
parameter (DEV.)	μ_{max}	a_{max}	b_{max}
(unit)	(cm^2/(V s))	(cm^2/(V s))	(cm^2/(V s))
value (maj.)	510	-1738	4983
value (min.)			
parameter (DEV.)	μ_{min}	a_{min}	b_{min}
(unit)	(cm^2/(V s))	(cm^2/(V s))	(cm^2/(V s))
value (maj.)	42	-21.2	44.1
value (min.)	$42 \cdot 2.48$		

Table 2.6: Consistent parameter set used for the out-of-plane mobility model of holes for biaxially strained SiGe in DEVICE and Chief based on reference [81].

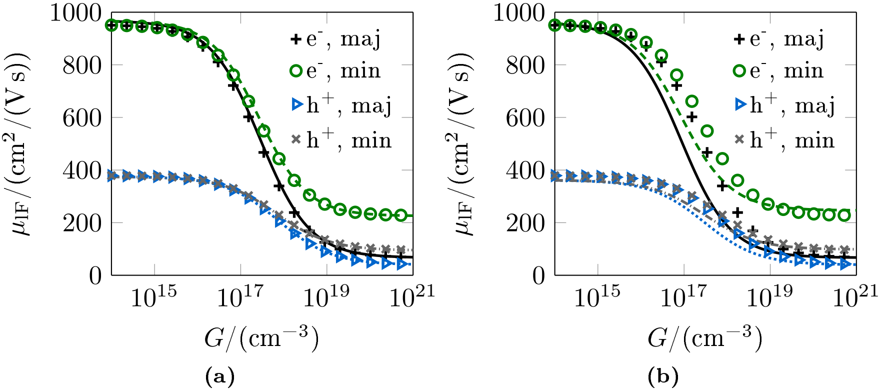


Figure 2.5: Out-of-plane mobility of biaxially strained SiGe for electrons and holes at a germanium concentration of $x_{\mathrm{mol}} = 20\,\%$. Model comparison of μ_{lF} vs. $G = N_{\mathrm{A}}^- + N_{\mathrm{D}}^+$ for **(a)** Chief (lines) vs. [81] (markers) and **(b)** DEVICE (lines) vs. [81] (markers).

Although the previous figures indicate a good agreement of DEVICE with the reference, the transition from low to high doping concentrations is not sufficiently well captured for some germanium concentrations, as shown in fig. 2.5. To improve the consistency between the used simulators, the full mobility description of Chief was implemented in DEVICE, including the G_{ref} model.

2.2.3 Energy relaxation times

The energy relaxation time τ_{e} is a material characteristic that describes the time required for thermally stimulated carriers to return to their steady state. As τ_{e} is used within the energy balance equation, only HD simulations require a respective model. The used reference description [81] reads

$$\tau_{\mathrm{e}} = (\tau_0 + \tau_1 x_{\mathrm{mol}}) \left[1 - \exp\left(-C_{\mathrm{ert}} \frac{T_{\mathrm{c}}}{T_{\mathrm{L}}}\right) + \left(\frac{T_{\mathrm{L}}}{T_{\mathrm{c}}}\right)\right], \tag{2.10}$$

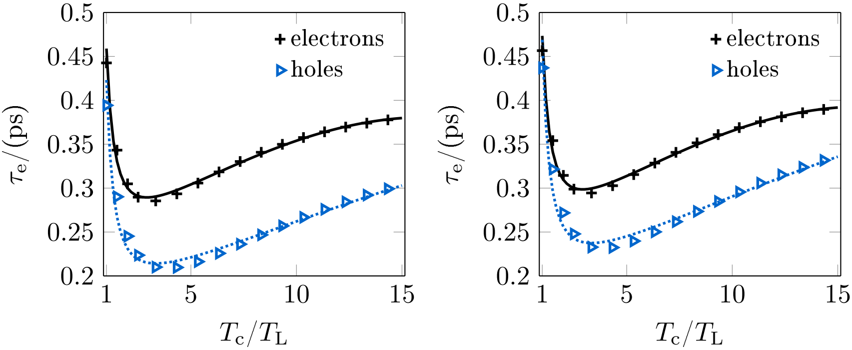
with the lattice temperature T_{L}, the carrier temperature T_{c} and the material parameters τ_0, τ_1 and C_{ert}. Chief provides a similar model to the user that was based on BTE simulations, see (2.11). For a consistent representation,

Chief [77]
$$\tau_\mathrm{e} = (\tau_\mathrm{a} + \tau_\mathrm{b} x_\mathrm{mol}) \exp\left[-C_\mathrm{t1}\left(\frac{T_\mathrm{c}}{T_\mathrm{L}} - C_\mathrm{o}\right)^2 + C_\mathrm{t2}\left(\frac{T_\mathrm{L}}{T_\mathrm{c}}\right)^2\right] \tag{2.11}$$

parameters: τ_a, τ_b, C_t1, C_t2 and C_o

parameter (ref.) (unit)	τ_0 (ps)	τ_1 (ps)	C_ert (1)		
electrons	0.38	0.04	0.18		
holes	0.36	0.13	0.10		
parameter (Chief) (unit)	τ_a (ps)	τ_b (ps)	C_t1 (1)	C_t2 (1)	C_o (1)
electrons	0.38	0.04	$1.93 \cdot 10^{-3}$	16.33	0.643
holes	0.36	0.13	$9.16 \cdot 10^{-4}$	28.87	0.873

Table 2.7: Parameters for the energy relaxation time models for electrons and holes in the reference [81] and Chief.



(a) **(b)**

Figure 2.6: Model comparison between Chief (lines) and [81] (markers) for the energy relaxation time of electrons and holes. τ_e vs. $T_\mathrm{c}/T_\mathrm{L}$ at a mole fraction of **(a)** $x_\mathrm{mol} = 0\,\%$ and **(b)** $x_\mathrm{mol} = 30\,\%$.

the model parameters were adjusted to the reference, with the corresponding values given in table 2.7 and a comparison for two different germanium mole fractions shown in fig. 2.6.

2.2.4 Effective density of states

The DoS is a material quantity that describes the amount states within an infinitesimally small energy span per unit volume available to be occupied by carriers, which does not necessarily mean that carriers filled these spots. Together with the distribution function that describes the probability to occupy a state, the number of free carriers per unit volume can be calculated for a bulk semiconductor:

$$\begin{aligned} n &= \int_{E_\mathrm{C}}^{\infty} \underbrace{\frac{8\pi m_\mathrm{e}}{h^3}\sqrt{2m_\mathrm{e,eff}\left(E-E_\mathrm{C}\right)}}_{\text{density of states}} \quad \underbrace{\exp\left(-\frac{E-E_\mathrm{F}}{k_\mathrm{B}T_\mathrm{L}}\right)}_{\text{Boltzmann distribution function}} \quad \mathrm{d}E \\ &= \quad \underbrace{2\left[\frac{2\pi m_\mathrm{e,eff}k_\mathrm{B}T_\mathrm{L}}{h^2}\right]^{3/2}}_{\text{effective density of states } (N_\mathrm{SiGe,n})} \quad \exp\left(-\frac{E_\mathrm{C}-E_\mathrm{F}}{k_\mathrm{B}T_\mathrm{L}}\right). \end{aligned} \tag{2.12}$$

E, E_C, E_F, $m_\mathrm{e,eff}$, h and T_L are the energy, conduction band edge, Fermi energy, effective electron mass, Planck constant and lattice temperature, respectively. Since $m_\mathrm{e,eff}$ (and the effective mass for holes $m_\mathrm{h,eff}$) depends on the germanium content, this must be taken into account for the device simulations. Using [82] as reference, the effective DoS for the SiGe composition system is described by

$$N_\mathrm{SiGe} = N_\mathrm{Si}\frac{M_1 + M_2\exp\left(\frac{\Delta E_1 x_\mathrm{mol}}{k_\mathrm{B}T_\mathrm{L}}\right) + M_3\exp\left(\frac{\Delta E_2 x_\mathrm{mol}}{k_\mathrm{B}T_\mathrm{L}}\right)}{M_1 + M_2 + M_3\exp\left(\frac{\Delta E_3}{k_\mathrm{B}T_\mathrm{L}}\right)}, \tag{2.13}$$

with the Boltzmann constant k_B and the material parameters M_1, M_2, M_3, ΔE_1, ΔE_2, ΔE_3 and N_Si for both electrons and holes. Corresponding parameter values are listed in table 2.8. Contrary to [82], the mole fraction dependent DoS models in DEVICE and Chief are based on the effective electron mass: DEVICE and Chief employ a generic quadratic and an exponential description, respectively. (2.14) and (2.15) list the corresponding models.

parameter (ref.) (unit)	ΔE_1 (eV)	ΔE_2 (eV)	ΔE_3 (eV)	N_{Si} (cm^{-3})
conduction band	-0.6	0	0	$2.94 \cdot 10^{19}$
valence band	-0.31	-0.315	-0.044	$2.24 \cdot 10^{19}$
parameter (ref.) (unit)	M_1 (1)	M_2 (1)	M_3 (1)	
conduction band	4	2	0	
valence band	1	1	1	

Table 2.8: Reference parameters [82] for the effective density of states model of electrons and holes.

DEVICE [78]

$$N_{\mathrm{SiGe}} = N_{\mathrm{z}} \left[m_{\mathrm{e,r}} + a_{\mathrm{e,r}} x_{\mathrm{mol}} + b_{\mathrm{e,r}} x_{\mathrm{mol}}^2 \right]^{3/2} \tag{2.14}$$

parameters: $m_{\mathrm{e,r}}$, $a_{\mathrm{e,r}}$ and $b_{\mathrm{e,r}}$

Chief [77]

$$\begin{aligned} N_{\mathrm{z}} &= 2 \left[\frac{2\pi m_{\mathrm{e}} k_{\mathrm{B}} T_{\mathrm{L}}}{h^2} \right]^{3/2} \\ N_{\mathrm{SiGe}} &= N_{\mathrm{z}} m_{\mathrm{e,r}}^{3/2} \left[(1 - c_{\mathrm{dos}}) + c_{\mathrm{dos}} \exp\left(-\frac{x_{\mathrm{mol}}}{x_{\mathrm{dos}}} \right) \right] \end{aligned} \tag{2.15}$$

parameters: $m_{\mathrm{e,r}}$, c_{dos} and x_{dos}

The parameters of DEVICE and Chief were tuned for agreement with the reference: $m_{\mathrm{e,r}}$ was calculated according to $m_{\mathrm{e,r}} = (N_{\mathrm{Si}}/N_{\mathrm{z}})^{2/3}$ and the other parameters were determined by least-square optimization. The results are shown in fig. 2.7 with the corresponding parameter listing in table 2.9. As can be observed in the figure, the generic quadratic description of DEVICE is not sufficient for a consistent model approach and therefore, the DoS model used in Chief has been implemented in DEVICE.

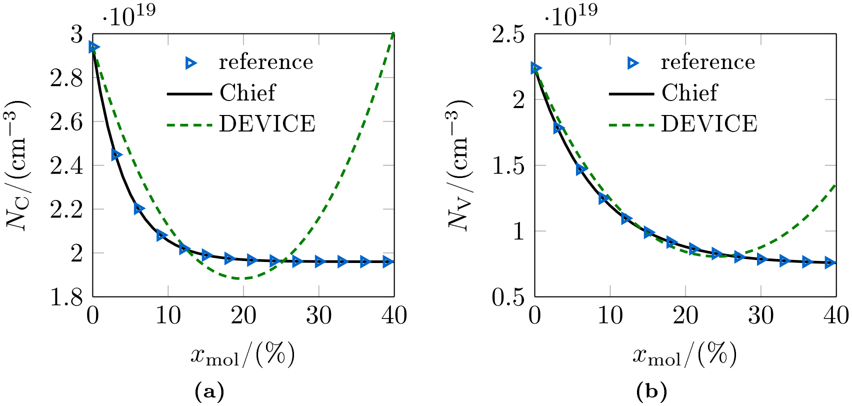


Figure 2.7: Model comparison between Chief, DEVICE and [82] for the effective density of states vs. germanium mole fraction for **(a)** the conduction and **(b)** valance band.

parameter (Chief) (unit)	$m_{\mathrm{e,r}}$ (1)	c_{dos} (1)	x_{dos} (1)
electrons	1.112	0.333	0.0431
holes	0.927	0.667	0.0827
parameter (DEV.) (unit)	$m_{\mathrm{e,r}}$ (1)	$a_{\mathrm{e,r}}$ (1)	$b_{\mathrm{e,r}}$ (1)
electrons	1.112	-2.91	7.39
holes	0.927	-3.79	7.84

Table 2.9: Parameters of the model description in Chief and DEVICE for the effective density of states model of electrons and holes.

2.2.5 Energy band diagram

The band model of a semiconductor – as used in classical DD and HD simulations – can be described by the energy band gap and electron affinity. Both quantities are composition dependent and additionally, the band gap is a function of doping concentration, caused by the so-called band gap narrowing (BGN) effect. It describes the band gap reduction due to the insertion of ionization energy levels close to the band edges.

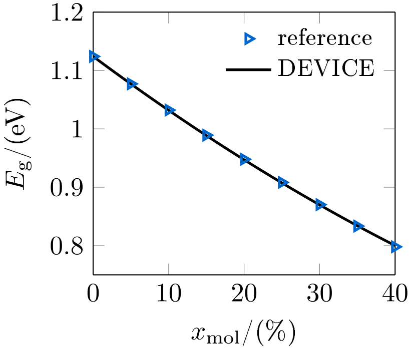


Figure 2.8: Band gap of biaxially strained SiGe vs. germanium mole fraction. Comparison of [85] (markers) and DEVICE/Chief (lines).

The band gap model reads

$$\begin{aligned} E_\mathrm{g}(x_\mathrm{mol}, G) &= \overset{\text{band gap at reference temperature}}{E_\mathrm{g0}} + \underbrace{a_\mathrm{g} x_\mathrm{mol} + b_\mathrm{g} x_\mathrm{mol}^2 + c_\mathrm{g} x_\mathrm{mol}^3}_{\text{SiGe composition}} - \underbrace{E_\mathrm{BGN}}_{\text{band gap narrowing}} \\ E_\mathrm{BGN} &= E_\mathrm{hd}\left[\ln\left(\frac{G}{G_\mathrm{hd}}\right) + \sqrt{\left[\ln\left(\frac{G}{G_\mathrm{hd}}\right)\right]^2 + c_\mathrm{hd}}\right], \end{aligned} \tag{2.16}$$

with the material parameters E_g0, a_g, b_g, E_hd, G_hd, γ_hd and c_hd. Corresponding parameter values are listed in table 2.10 and are taken from [85,86]. The implemented band gap models of DEVICE and Chief do not feature the cubic parameter c_g, as it only becomes relevant for large values of x_mol. For the relevant range of $x_\mathrm{mol} < 0.4$, c_g can be incorporated in b_g. A comparison is shown in fig. 2.8 and the additional parameter combination is listed in table 2.10.

The electron affinity χ is the energy required by an electron to reach the vacuum level E_vac starting from the conduction band edge E_C. The corresponding model is a generic quadratic function of x_mol

$$\chi\left(x_\mathrm{mol}\right) = \chi_0 + a_\chi x_\mathrm{mol} + b_\chi x_\mathrm{mol}^2 + \gamma_\mathrm{hd} E_\mathrm{BGN}, \tag{2.17}$$

with the material parameters χ_0, a_χ and b_χ. Values for the electron affinity

parameter (reference) (unit)	E_{g0} (eV)	a_g (eV)	b_g (eV)	c_g (eV)
value	1.1241	-0.96	0.43	-0.17
parameter (DEV./Chief) (unit)	E_{g0} (eV)	a_g (eV)	b_g (eV)	c_g (eV)
value	1.1241	-0.96	0.375	0
parameter (BGN) (unit)	E_{hd} (meV)	G_{hd} (cm^{-3})	c_{hd} (1)	γ_{hd} (1)
value	6.92	1.3e17	0.5	0.5

Table 2.10: Parameters of the references [85, 86] for the band gap model of biaxially strained SiGe.

parameter (ref.) (unit)	χ_0 (eV)	a_χ (eV)	b_χ (eV)
value	4.05	-0.05	0

Table 2.11: Assumed parameters for the electron affinity of SiGe.

of silicon and germanium can be found in literature [87], but a measurement based analysis of the functional dependence does not exist yet [88]. As χ_{Si} and χ_{Ge} do not differ significantly (4.05 eV vs. 4.0 eV), a linear behavior – with the corresponding parameter values listed in table 2.11 – is assumed. DEVICE and Chief provide the same description and therefore, no parameter adjustment is necessary.

To illustrate the effects of a changing band gap and affinity consider the exemplary structure in fig. 2.9. The left hand side part consists of a constantly doped region with variable germanium mole fraction, whereas on the right hand side the germanium content is fixed and the doping level increases. For the thermal equilibrium and without interaction of the Poisson equation with the band edges (i.e. the electrostatic potential ψ is zero), E_C and the valence band edge E_V can be calculated with the previously described models by applying

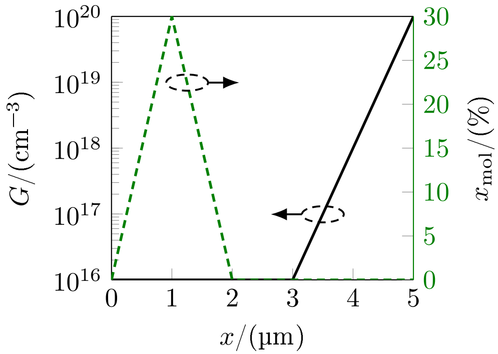


Figure 2.9: Exemplary structure to visualize a band gap change due to material composition and BGN.

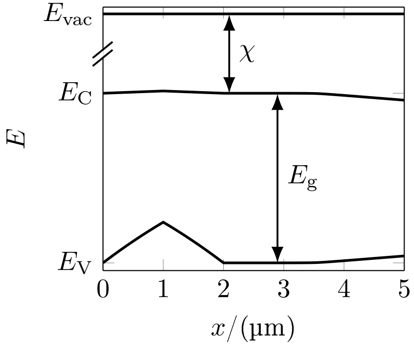


Figure 2.10: Band diagram of the exemplary structure (see fig. 2.9) illustrating the influence of alloying and BGN.

$$\begin{aligned} E_{\mathrm{C}} &= E_{\mathrm{vac}} - \chi \\ E_{\mathrm{V}} &= E_{\mathrm{C}} - E_{\mathrm{g}}. \end{aligned} \tag{2.18}$$

With increasing germanium content, both E_{g} and the electron affinity are reduced and both E_{C} and E_{V} of the left hand side of fig. 2.10 are changing accordingly. Due to BGN, the electron affinity is increased and the band gap reduced, as can be observed on the right hand side of the figure.

2.2.6 High-field mobility

The generic model for the high-field mobility μ_{hF} according to [89] reads

$$\begin{aligned} \mu_{\mathrm{hF}}\left(E_{\mathrm{eff}}\right) &= \frac{\mu_{\mathrm{lF}}}{\left[1+\left(\frac{E_{\mathrm{eff}}\mu_{\mathrm{lF}}}{v_{\mathrm{sat}}}\right)^{\beta_{\mathrm{hF}}}\right]^{1/\beta_{\mathrm{hF}}}} , \\ v_{\mathrm{sat}}\left(x_{\mathrm{mol}}\right) &= v_{\mathrm{Si}} + a_{\mathrm{sat}}x_{\mathrm{mol}} + b_{\mathrm{sat}}x_{\mathrm{mol}}^{2} + c_{\mathrm{sat}}x_{\mathrm{mol}}^{3} \end{aligned} \tag{2.19}$$

with E_{eff} as the driving field in HD simulations (E_{dF}) or the gradient of the quasi-Fermi potential in DD simulations ($|\mathrm{grad}\,(\varphi)|$) and the model parameters a_{sat}, b_{sat}, c_{sat} and β_{hF}. The model parameters of electrons were adjusted to MC simulation data [89] for a consistent model representation within the used simulators, see fig. 2.11. In DEVICE, a third order coefficient does not exist and therefore, c_{sat} is set to zero.

For holes, standard parameters are assumed, based on [83]. The complete parameter set is listed in table 2.12. Note that the value of β_{hF} used for DEVICE is different to Chief, as the driving force in HD simulations differs and an additional carrier temperature dependent portion is added to E_{eff} (see [89]).

2.2.7 Relative permittivity

The relative permittivity $\varepsilon_{\mathrm{r,AB}}$ of an arbitrary alloy consisting of the materials A and B may be calculated according to [90]

$$\varepsilon_{\mathrm{r,AB}}\left(x_{\mathrm{mol}}\right) = \left(1-x_{\mathrm{mol}}\right)\varepsilon_{\mathrm{r,A}} + x_{\mathrm{mol}}\varepsilon_{\mathrm{r,B}} + x_{\mathrm{mol}}\left(1-x_{\mathrm{mol}}\right)C_{\varepsilon}, \tag{2.20}$$

with the material parameters $\varepsilon_{\mathrm{r,A}}$, $\varepsilon_{\mathrm{r,B}}$ and C_{ε}. The parameters for the SiGe composition system are listed in table 2.13. The descriptions matches the implementations in DEVICE and Chief and therefore, a parameter adjustment was not necessary.

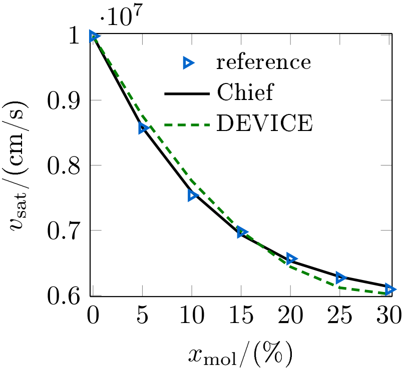


Figure 2.11: Saturation velocity of electrons in biaxially strained SiGe vs. germanium mole fraction. Comparison of [89] (markers) and DEVICE/Chief (lines).

parameter (Chief) (unit)	v_{Si} (cm/s)	a_{sat} (cm/s)	b_{sat} (cm/s)
electrons	$9.984 \cdot 10^6$	$-3.278 \cdot 10^7$	$9.949 \cdot 10^7$
holes	$9.5 \cdot 10^6$	0	0
parameter (Chief) (unit)	c_{sat} (cm/s)	β_{hF} (1)	
electrons	$-1.100 \cdot 10^8$	1.382 [89]	
holes	0	1	
parameter (DEV.) (unit)	v_{Si} (cm/s)	a_{sat} (cm/s)	b_{sat} (cm/s)
electrons	$9.984 \cdot 10^6$	$-2.675 \cdot 10^7$	$4.515 \cdot 10^7$
holes	$9.5 \cdot 10^6$	0	0
parameter (DEV.) (unit)	c_{sat} (cm/s)	β_{hF} (1)	
electrons	0	1.28 [89]	
holes	0	1	

Table 2.12: Parameter set for the high-field mobility model of SiGe alloys.

parameter (unit)	$\varepsilon_{\mathrm{r,Si}}$ (1)	$\varepsilon_{\mathrm{r,Ge}}$ (1)	C_{ε} (1)
value	11.7	16	0

Table 2.13: Parameter set for the permittivity of SiGe alloys.

parameter (unit)	τ_{min} (s)	τ_{max} (s)	G_{rec} (cm^{-3})	β_{rec} (1)
electrons	0	$9 \cdot 10^{-6}$	$2.5 \cdot 10^{15}$	0.5
holes	0	$3 \cdot 10^{-6}$	$2.5 \cdot 10^{15}$	0.5

Table 2.14: Parameter set for the SRH recombination of carriers in silicon based on [78, 91].

2.2.8 Recombination

Two recombination models are considered in the simulations: Shockley-Read-Hall (SRH) and Auger recombination. Other mechanisms – like surface or interface recombination – are not included, as their specific description is strongly process dependent and cannot be quantified with the used simulation approaches. The model for the SRH recombination rate R_{SRH} – including a doping dependence – reads

$$R_{\mathrm{SRH}} = \frac{pn - n_{\mathrm{ie}}^2}{\tau_n \left(n_{\mathrm{ie}} + p\right) + \tau_p \left(n_{\mathrm{ie}} + n\right)},$$

$$\tau_n = \tau_{n,\mathrm{min}} + \frac{\tau_{n,\mathrm{max}} - \tau_{n,\mathrm{min}}}{1 + \left(G/G_{n,\mathrm{rec}}\right)^{\beta_{n,\mathrm{rec}}}} \quad \text{and} \quad \tau_p = \tau_{p,\mathrm{min}} + \frac{\tau_{p,\mathrm{max}} - \tau_{p,\mathrm{min}}}{1 + \left(G/G_{p,\mathrm{rec}}\right)^{\beta_{p,\mathrm{rec}}}}, \tag{2.21}$$

with the carrier densities p and n, the effective intrinsic carrier density n_{ie} and the model parameters τ_{min}, τ_{max}, β_{rec} and G_{rec} for both holes and electrons. The respective parameter values for electrons and holes are listed in table 2.14 and are based on [78, 91].

The Auger recombination model is described by

$$R_{\mathrm{Aug}} = \left(c_{n,\mathrm{Aug}} n + c_{p,\mathrm{Aug}} p\right) \overset{\substack{\text{deviation from equilibrium} \\ |}}{\left(pn - n_{\mathrm{ie}}^2\right)}, \tag{2.22}$$

with the model parameters $c_{n,\mathrm{Aug}}$ and $c_{p,\mathrm{Aug}}$. The corresponding parameter values are listed in table 2.15 and are based on [92]. Both recombination processes are linked to the state of equilibrium indicated by the marked term in (2.22). For the thermal equilibrium there is no net recombination and the total recombination equals the generation rate.

parameter (unit)	$c_{n,\mathrm{Aug}}$ (cm^6/s)	$c_{p,\mathrm{Aug}}$ (cm^6/s)
value	$2.8 \cdot 10^{-31}$	$0.99 \cdot 10^{-31}$

Table 2.15: Parameter set for the Auger recombination of carriers in silicon based on [92].

2.2.9 Hydrodynamic transport parameters

The HD transport parameters f_{td}, f_{tc} and f_{ec} are – more or less – empirical model parameters within the energy flux and transport equation of the HD description. The HD transport equation for electrons in the 1D case is

$$\begin{aligned} J_{n,x} = &- qn\mu_n \operatorname{grad}(\psi + V_n) + \mu_n k_{\mathrm{B}} T_n \operatorname{grad}(n) \\ &+ \mu_n k_{\mathrm{B}} n \operatorname{grad}(T_n) \left[f_{\mathrm{td}} + \ln\left(\frac{N_{\mathrm{C}}}{n_{\mathrm{ir}}}\right)\right], \end{aligned} \tag{2.23}$$

with the elementary charge q, the electron mobility μ_n, the electrostatic potential ψ, the band potential of electrons V_n, the effective DoS in the conduction band N_{C} and the intrinsic carrier density n_{ir}. The energy flux density

$$\begin{aligned} S_{n,x} = &- \left(\frac{5}{2} + f_{\mathrm{tc}}\right)\left(\frac{k_{\mathrm{B}}}{q}\right)^2 q\mu_n n T_n \operatorname{grad} T_n \\ &- \left(\frac{5}{2} + f_{\mathrm{ec}}\right)\frac{k_{\mathrm{B}} T_n}{q} J_{n,x} \end{aligned} \tag{2.24}$$

includes the remaining HD transport parameters. A typical approach for adjusting them is to perform an optimization with the goal to match the terminal quantities of BTE simulations with the HD result. Assuming all other models are sufficiently matched with the BTE description, it is a valid approach to calibrate them. However, performing this adjustment step for various doping profiles and technology generations results in different sets of parameters [77] and shows that hydrodynamic simulations are just a simplified replacement for the BTE and that their predictive capabilities for future process generations is limited. Therefore, a suitable parameter set for current advanced SiGe HBTs is used [77] with the parameters listed in table 2.16.

parameter (unit)	f_{td} (1)	f_{tc} (1)	f_{ec} (1)
value	1.0	-1.7624	0.0

Table 2.16: Parameter set for the HD transport parameters of electrons based on [77].

Note that for holes only DD transport is assumed, which is a valid approach for npn HBTs. Since the hole current of npn transistors is mainly a recombination current and corresponding models are identical for both HD and DD transport, this simplification is justified. As already mentioned in section 2.2.8 – the considered recombination mechanisms are only a rough estimation.

CHAPTER 3

Scalable extraction procedure for an advanced SiGe HBT technology

Without a fast and reliable extraction procedure, the task of an heterogeneous TCAD approach would not be feasible. The procedure must be suitable for the device simulators DEVICE, Chief and DEBOTS – previously described in section 2.1. Since it is necessary to prove that the TCAD approach is applicable to advanced SiGe HBTs, the extraction procedure must also work for measurement data to generate a reference parameter set. Without a meaningful technology parameter set corresponding to measured devices, a thorough TCAD calibration is not possible. Consequently, the reliability and significance of the TCAD prediction would be reduced greatly. It is also very important to apply identical extraction procedures to measurement and simulation data for consistency.

HICUM [74] is the compact model that is employed here, as it is a comprehensive up-to-date framework that includes relevant physical effects and is applicable to advanced SiGe HBTs [93]. Its simplified equivalent circuit for a transistor in forward operation – including all elements relevant for the upcoming extraction tasks – is shown in fig. 3.1. As illustrated by the dotted and dashed boxes, HICUM contains elements for both modeling the 1D and internal 2D transistor regions (see also fig. 5.1 for the correspondence to the actual transistor structure) and consequently, is suitable for the heterogeneous prediction approach of section 5.1.

Some model parts of HICUM are mutually interdependent and therefore, the extraction should follow a certain sequence for consistency, see fig. 3.2. Few model parameters cannot be determined reliably from extraction and are estimated by other means:

- The spacer capacitances cannot be separated from the peripheral junction capacitance. However, as the spacer capacitance is related to its geometry, the value can be estimated by a Laplace solver, like POICAPS.
- With the help of special test structures, sheet resistance values can be determined for the corresponding collector and base regions. Feeding these values into quasi-3D device simulations [94] allows to determine the resistances required for further extraction steps.
- To the author's knowledge, there is no extraction method to determine the split-up of the high current transit time between the collector and base portion. Hence, $f_{\tau\mathrm{hc}} = 0.5$ is assumed.
- The scaling of the distributed substrate network is unclear. Only the capacitance of the CS junction is scaled for the model. The remaining parameters are extracted for each device and remain unscaled.

The extraction is performed for an advanced BiCMOS technology in a 55 nm lithography node of STMicroelectronics [76]. To limit the extraction effort, only long transistor structures with an emitter length larger than 4.5 µm are considered.

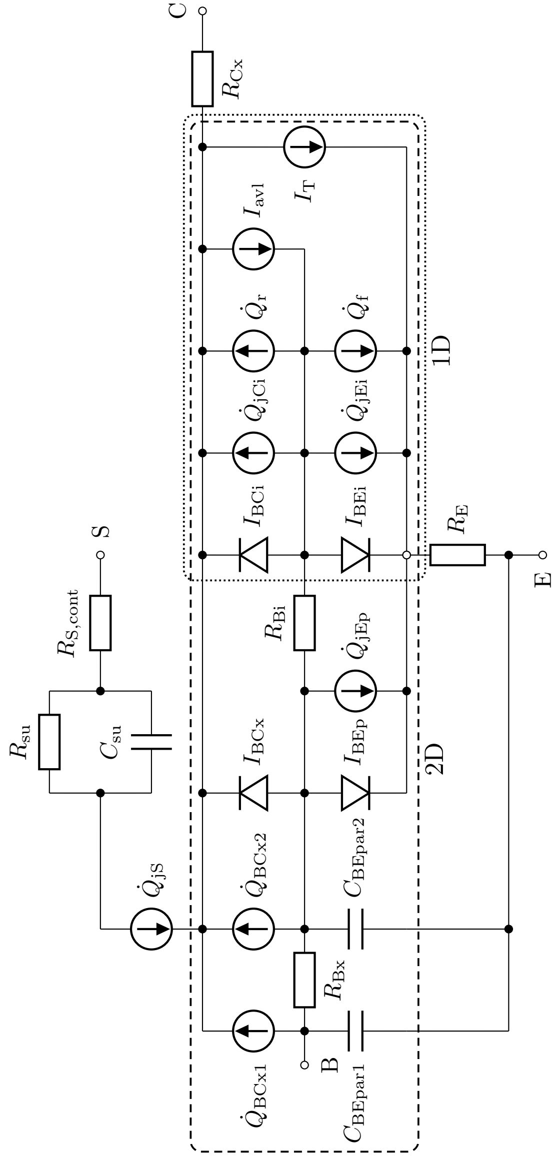


Figure 3.1: Simplified HICUM equivalent circuit for forward transistor operation. The dotted and dashed boxes enclose components required for modeling the 1D and internal 2D transistor regions, respectively.

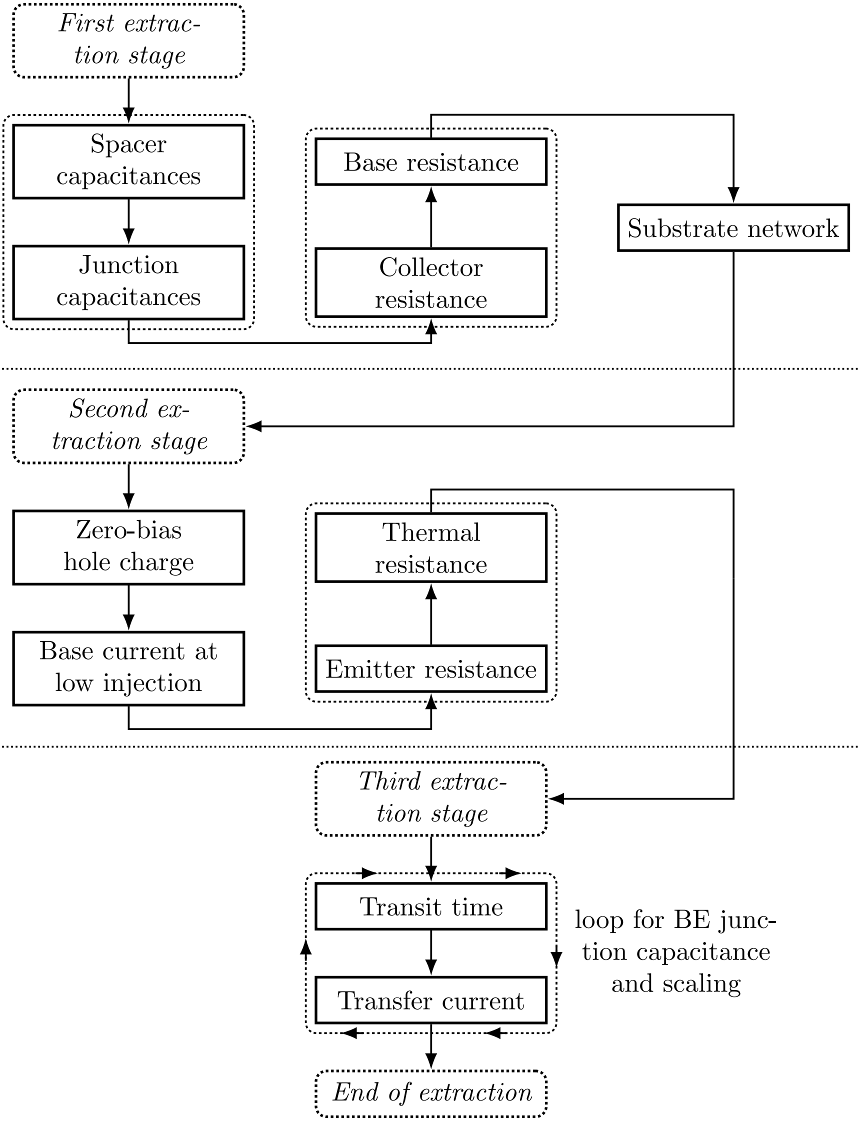


Figure 3.2: Proposed HICUM extraction workflow.

3.1 Perimeter over area separation

For the upcoming extraction tasks it will be necessary to apply geometry scaling based on the concept of the perimeter over area (PoA) separation. The general idea of the PoA separation is based on the transistor partitioning of fig. 3.3. By using the area and peripheral transistor portions, the electrical behavior of the full transistor can be calculated for all compact model parameters that require scaling. For example, the total BE junction capacitance

$$C_{\mathrm{jE,tot}} = \underbrace{\overline{C}_{\mathrm{jEi}} A_{\mathrm{E0}}}_{C_{\mathrm{jEi}}} + \underbrace{C'_{\mathrm{jEp}} P_{\mathrm{E0}}}_{C_{\mathrm{jEp}}}\,, \tag{3.1}$$

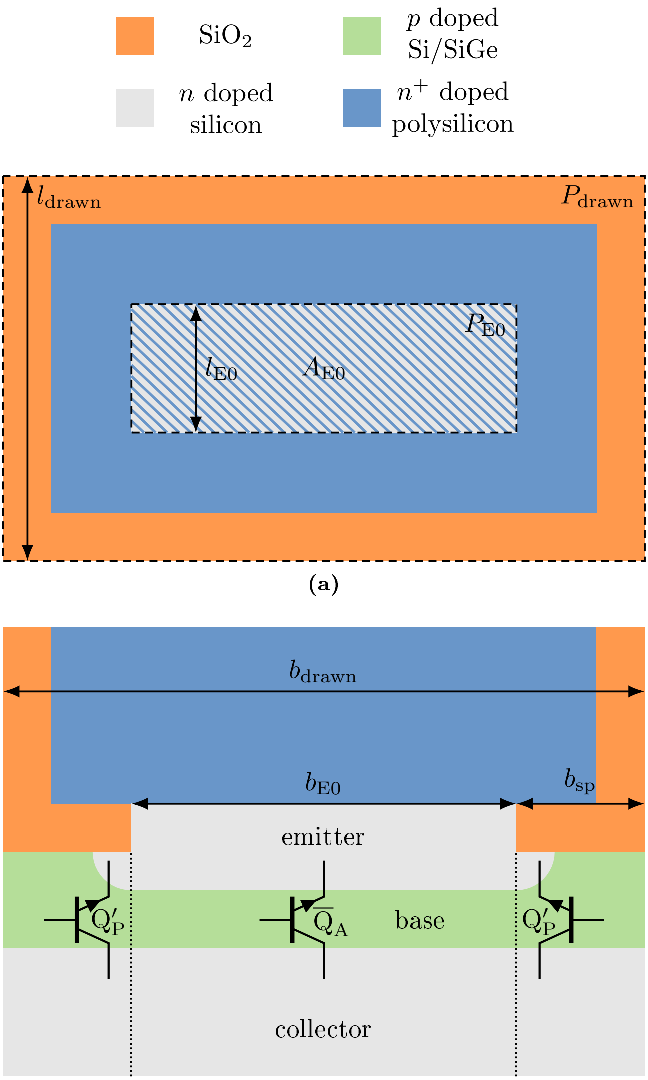
is described by the internal (area normalized) and the perimeter normalized components $\overline{C}_{\mathrm{jEi}}$ and C'_{jEp}, respectively. $P_{\mathrm{E0}} = 2\,(b_{\mathrm{E0}} + l_{\mathrm{E0}})$, $A_{\mathrm{E0}} = b_{\mathrm{E0}} l_{\mathrm{E0}}$, b_{E0} and l_{E0} denote the actual emitter window perimeter, area, width and length, respectively. The actual emitter size relates to the drawn size by

$$\begin{aligned} b_{\mathrm{E0}} &= b_{\mathrm{drawn}} - b_{\mathrm{sp}} \\ l_{\mathrm{E0}} &= l_{\mathrm{drawn}} - b_{\mathrm{sp}}, \end{aligned} \tag{3.2}$$

as illustrated in fig. 3.3. In the example, the capacitance components are unknowns and need to be determined from the known total capacitance $C_{\mathrm{jE,tot}}$. By normalizing (3.1) to A_{E0},

$$\frac{C_{\mathrm{jE,tot}}}{A_{\mathrm{E0}}} = \overline{C}_{\mathrm{jEi}} + C'_{\mathrm{jEp}} \frac{P_{\mathrm{E0}}}{A_{\mathrm{E0}}} \tag{3.3}$$

is obtained, which can be used to perform the PoA separation. (3.3) is a linear equation with the axis intercept $\overline{C}_{\mathrm{jEi}}$ and the slope C'_{jEp}. Using different transistor sizes allows to plot a reference dataset (e.g. measurements) of $C_{\mathrm{jE,tot}}/A_{\mathrm{E0}}$ vs. $P_{\mathrm{E0}}/A_{\mathrm{E0}}$ for fitting with a straight line and obtaining the required unknowns. Repeating the procedure for different bias points allows to capture the relevant range of $\overline{C}_{\mathrm{jEi}}$ and C'_{jEp}. The PoA separation is a common method in HBT modeling and was already applied to standard bipolar junction transistors (BJTs) in [95]. It has received additional development effort for advanced HBTs and their increased scaling complexity, e.g. in [96].



(a)

(b)

Figure 3.3: Transistor geometry partitioning concept for **(a)** the top view, defining major transistor dimensions and **(b)** the cross section, which divides the transistor into the area- $(\overline{\mathrm{Q}}_\mathrm{A})$ and perimeter-normalized (Q'_P) sub-transistors.

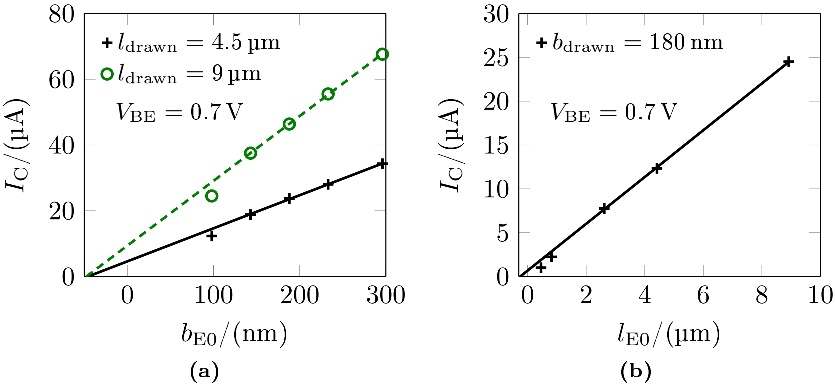


Figure 3.4: Scalability assessment for the measured collector current at $V_{BC} = 0\,V$ and $V_{BE} = 0.7\,V$ (HS transistors of [76]). **(a)** I_C vs. b_{E0} (markers) and linear fit (lines) for two fixed lengths. **(b)** I_C vs. l_{E0} (markers) and linear fit (line) for a fixed width.

Generally, the actual emitter window size does not necessarily correspond to the electrical dimensions that determine the behavior of the transistor, due to, e.g., laterally recessed or extended emitter doping diffusion. Also, with shrinking dimensions, the determination error for b_{E0} and l_{E0} increases. For compact modeling, it is therefore advised to use the electrical dimensions $b_E = b_{E0} - \Delta b_E$ and $l_E = l_{E0} - \Delta l_E$ instead of the actual emitter dimensions for forcing the collector current to be zero for $b_E = 0$ or $l_E = 0$. If $\Delta b_E \neq \Delta l_E$, a spatial dependence for the peripheral components is implied – actually requiring 3D simulations. For long devices however, Δl_E plays a minor role and the extraction in this work can follow the standard PoA approach.

The generic scalability of a process cannot be assessed by the quality of the PoA separation, as wrong actual dimensions can have a severe impact on the PoA scaling [96]. Instead, scalability should be assessed by plotting relevant quantities – like the collector current I_C – vs. b_{E0} and l_{E0}; if a linear fit can be applied to the data, the process is scalable. As can be observed in fig. 3.4, the HS transistors are only scalable to a limited extent because the smallest emitter width and the smallest lengths do not scale well. The behavior is confirmed by selecting other bias points within the low injection

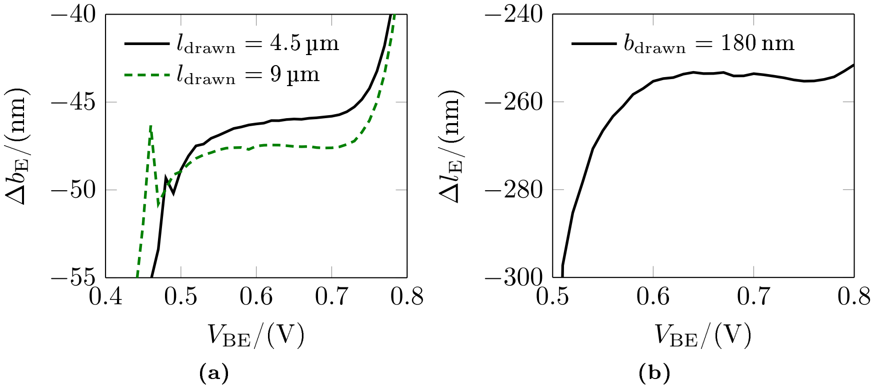
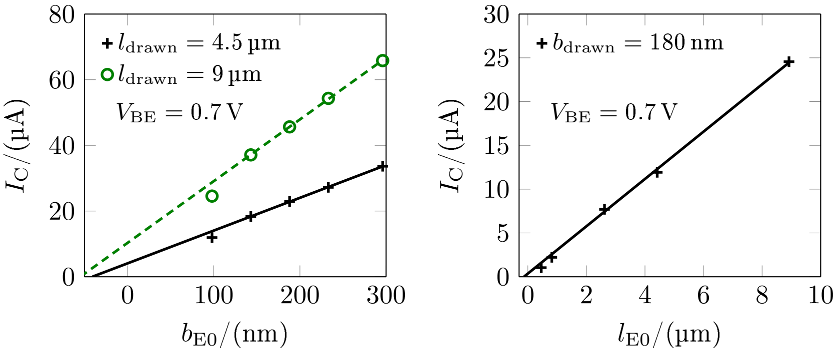


Figure 3.5: Voltage dependence of the dimension offset required for obtaining the effective electrical dimensions of the collector current at $V_{BC} = 0\,\mathrm{V}$ (HS transistors of [76]). **(a)** Δb_E vs. V_{BE} for two fixed lengths and **(b)** Δl_E vs. V_{BE} for a fixed width.

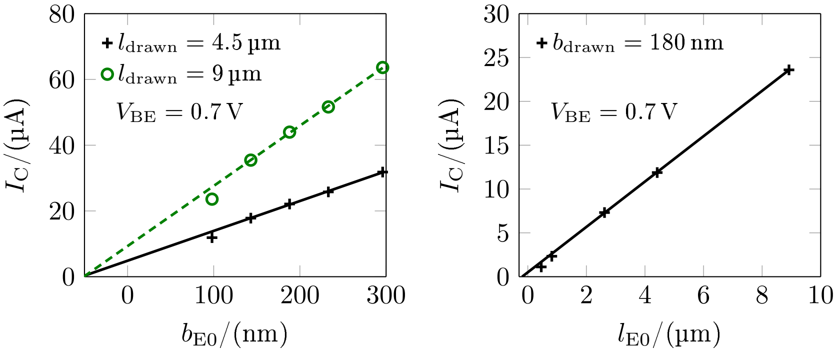
region. As depicted in [97], there is a variety of concrete reasons that can cause a process not to scale, but typically they are related to emitter width or length dependent doping profiles or e.g. an additional lithography dependence for small sizes. For the medium voltage (MV) and high voltage (HV) transistor versions the results are similar, see figures 3.6 and 3.7. Likewise, smallest transistor sizes do not scale well.

Fig. 3.5 shows the intercepts of the fits of fig. 3.4 with the x axis that correspond to the dimension offsets Δb_E and Δl_E required for obtaining the electrical dimensions. As Δb_E and Δl_E are smaller than zero, a laterally extended emitter doping is indicated. Consequently, for small transistors the peripheral component contains a large portion of the total collector current. Note that both the absolute value and the bias dependence of Δl_E and Δb_E are different. As $|\Delta l_E|$ is about four to five times larger than $|\Delta b_E|$, the emitter profile extends even further in z direction or the actual dimensions in z direction are different (caused by a directional lithography behavior). Taking the mean for the relevant bias region for HS, MV and HV devices leads to the technology parameters $\Delta b_E = -50.1\,\mathrm{nm}$ and $\Delta l_E = -194.3\,\mathrm{nm}$.



(a) **(b)**

Figure 3.6: Scalability assessment for the measured collector current at $V_{BC} = 0\,V$ and $V_{BE} = 0.7\,V$ (MV transistors of [76]). **(a)** I_C vs. b_{E0} (markers) and linear fit (lines) for two fixed lengths. **(b)** I_C vs. l_{E0} (markers) and linear fit (line) for a fixed width.



(a) **(b)**

Figure 3.7: Scalability assessment for the measured collector current at $V_{BC} = 0\,V$ and $V_{BE} = 0.7\,V$ (HV transistors of [76]). **(a)** I_C vs. b_{E0} (markers) and linear fit (lines) for two fixed lengths. **(b)** I_C vs. l_{E0} (markers) and linear fit (line) for a fixed width.

3.2 Spacer capacitances

The approach for determining the spacer capacitances is based on the Poisson equation

$$\mathrm{div}\left(-\varepsilon_0\varepsilon_\mathrm{r}\,\mathrm{grad}\left(\psi\right)\right) = \rho, \tag{3.4}$$

with the space charge density ρ and the permittivity in vacuum ε_0. Setting $\rho = 0$ is identical to assuming neutrality, which is a valid simplification for the passive spacer regions. Following this method, the capacitance determination reduces to a geometrical problem that can be analyzed with POICAPS. The charge of a contact within a two dimensional simulation is then calculated by the Gauss theorem

$$Q'_\mathrm{contact} = \oint \vec{D} \cdot \mathrm{d}\vec{s}, \tag{3.5}$$

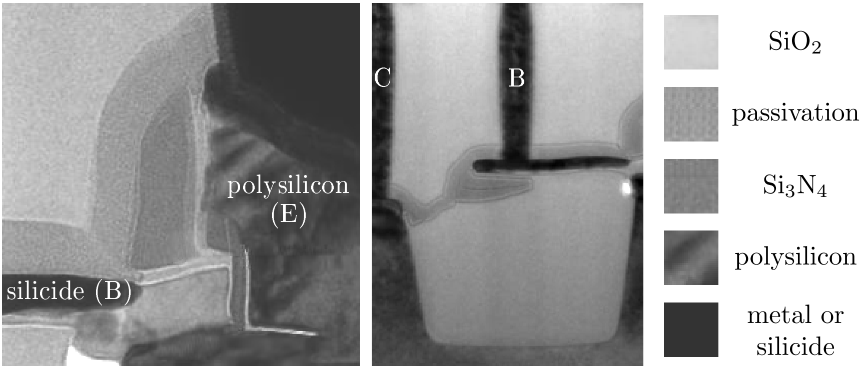
with Q'_contact as the length normalized contact charge, $\vec{D}$ as the electric displacement field and $\vec{s}$ as the normal vector of an arbitrary curve enclosing the contact. Assuming a linear relationship between $\vec{D}$ and the electric field $\vec{E}$

$$\vec{D} = \varepsilon_0\varepsilon_\mathrm{r}\vec{E} \tag{3.6}$$

and choosing the curve that directly encloses the contact leads to (3.7), the simplified form of Q'_contact. In order to obtain the relationship, the boundary condition of a contact (i.e. the electric field E_contact must be parallel to the normal vector of the contact surface) was applied.

$$Q'_\mathrm{contact} = \varepsilon_0 \oint \varepsilon_\mathrm{r} E_\mathrm{contact} \mathrm{d}s_\mathrm{contact} \tag{3.7}$$

Up to this point, these analyses are performed automatically inside of POICAPS [79]. Subsequently, (3.8) is applied by the user to calculate the length specific capacitance C'_AB between the contacts A and B using the charge of contact A Q'_A. The capacitance directly corresponds to the calculated charge of the simulator output by setting the voltage difference between the two contacts to $V_\mathrm{A,B} = 1\,\mathrm{V}$.



(a) **(b)**

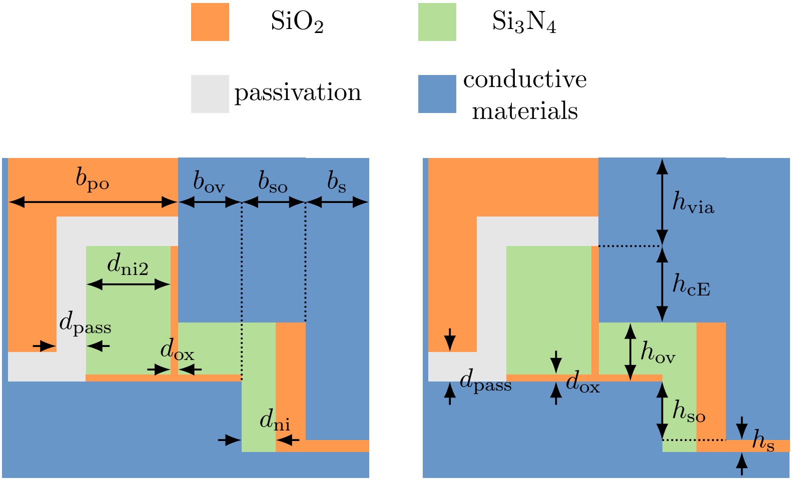
Figure 3.8: TEM pictures of an advanced SiGe HBT process [76] for **(a)** the BE spacer (zoom-in) and **(b)** the BC spacer.

$$C'_{\mathrm{AB}} = \frac{|Q'_{\mathrm{A}}|}{|V_{\mathrm{A,B}}|} \tag{3.8}$$

Using transmission electron microscopy (TEM) pictures of the transistor cross section, the BE and BC spacer geometry and materials can be determined. As passing electrons are increasingly diffracted by atoms with larger atomic number, the corresponding materials appear darker within the TEM picture (i.e. bright regions correspond to materials with low atomic number). Based on fig. 3.8, the POICAPS compatible schematics have been generated with the dimension definitions in figures 3.9 and 3.10 for the BE and BC spacer, respectively. The process matched dimensions are listed in tables 3.2 and 3.3. To verify the suitability of the proposed schematic, the resulting structures are compared as a transparent overlay to the TEM pictures in fig. 3.11. The assumed relative permittivities, used in the simulations for the spacer materials, are listed in table 3.1.

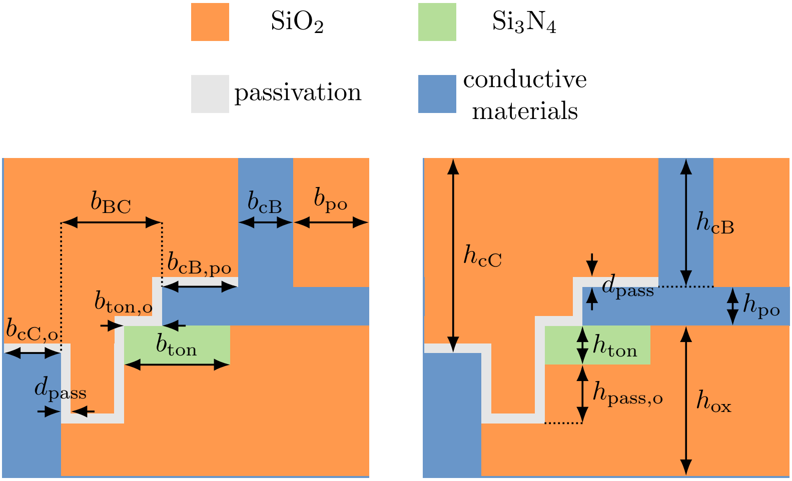
	SiO$_2$	Si$_3$N$_4$	Passivation (nitride)
ε_{r}	3.9	7.5	7.0

Table 3.1: Assumed relative permittivity used in the electrostatic simulations for the spacer materials.



(a) **(b)**

Figure 3.9: BE spacer geometry schematic with **(a)** vertical and **(b)** lateral dimensions.



(a) **(b)**

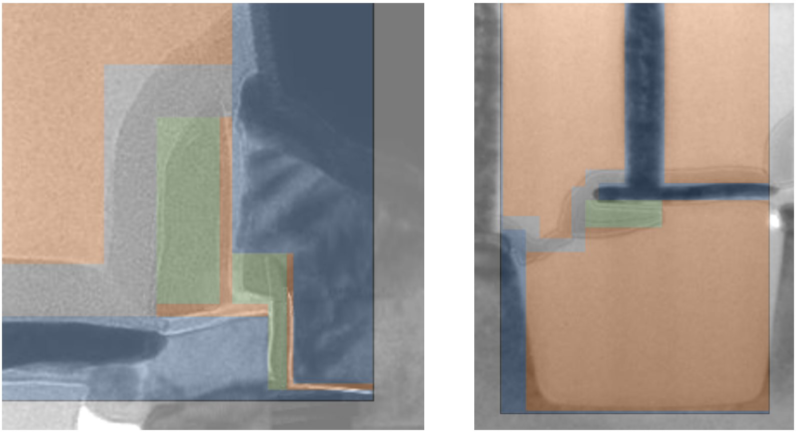
Figure 3.10: BC spacer geometry schematic with **(a)** vertical and **(b)** lateral dimensions.

dimension (unit)	b_{po} (nm)	b_{ov} (nm)	b_{so} (nm)	b_{s} (nm)	d_{ni} (nm)	d_{ni2} (nm)	d_{ox} (nm)
value	230	13	12	42	9	30	6
dimension (unit)	h_{via} (nm)	h_{cE} (nm)	h_{ov} (nm)	h_{so} (nm)	h_{s} (nm)	d_{pass} (nm)	
value	235	65	30	31	3	25	

Table 3.2: Process matched dimensions used for the BE schematic of fig. 3.9 to conduct Laplace simulations.

dimension (unit)	b_{po} (nm)	b_{cB} (nm)	$b_{\text{cB,po}}$ (nm)	b_{ton} (nm)	$b_{\text{ton,o}}$ (nm)	b_{BC} (nm)	$b_{\text{cC,o}}$ (nm)
value	191	73	47	50	25	133	42
dimension (unit)	h_{cB} (nm)	h_{po} (nm)	h_{ox} (nm)	h_{ton} (nm)	$h_{\text{pass,o}}$ (nm)	h_{cC} (nm)	d_{pass} (nm)
value	330	31	385	50	45	415	25

Table 3.3: Process matched dimensions used for the BC schematic of fig. 3.10 to conduct Laplace simulations.



(a) **(b)**

Figure 3.11: TEM picture and simulation input comparison of an advanced SiGe HBT process [76] for **(a)** the BE spacer (zoom-in) and **(b)** the BC spacer.

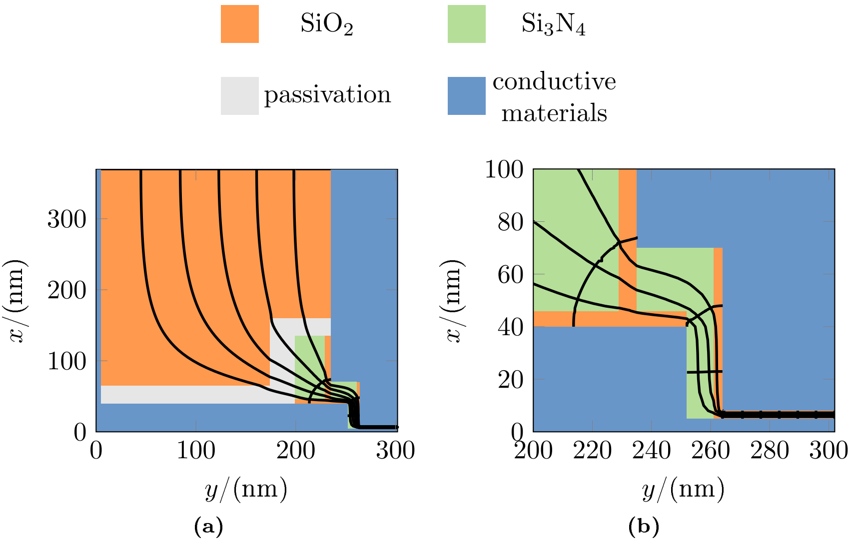


Figure 3.12: Field lines and equipotentials for **(a)** the BE spacer and **(b)** a corresponding zoom-in to the region with the largest capacitance contribution using a smaller number of equipotential lines.

The conducted simulations for the BE and BC spacer lead to the capacitances $C'_{\mathrm{BE,par}} = 0.796\,\mathrm{fF/\mu m}$ and $C'_{\mathrm{BC,par}} = 0.126\,\mathrm{fF/\mu m}$, respectively. Assessing the field lines in fig. 3.12 reveals the origin for the large BE spacer capacitance: In total, eleven field lines were drawn to divide the structure into ten segments. 90 % of the capacitance is attributed to the region shown by the zoom-in and the largest contribution is caused by the distance h_{s} between the polysilicon emitter and the lateral base. Either increasing h_{s} or decreasing b_{s} would significantly decrease the BE spacer capacitance.

As observed in fig. 3.13, there is some field line clustering at the closest distance between the base and collector contact. Therefore, decreasing $b_{\mathrm{cB,po}}$ would help to reduce the capacitance. Nevertheless, most streamlines are distributed fairly uniform and hence, the BC spacer structure is already optimized.

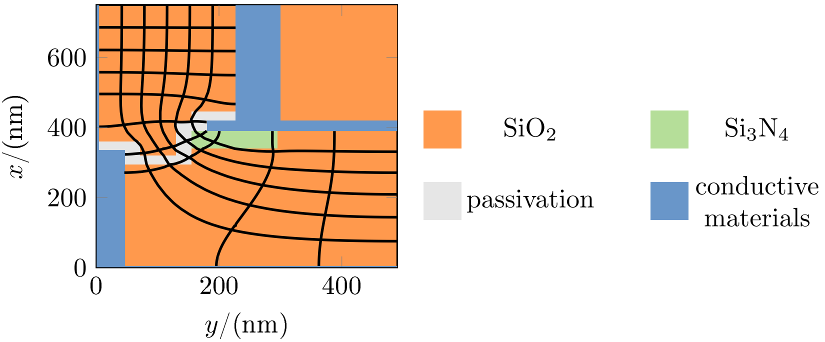


Figure 3.13: Field lines and equipotentials for the BC spacer.

For calculating the final capacitance required for the complete three dimensional transistor structure, the transistor layout needs to be taken into consideration. The full top view of an exemplary transistor in CBEBC configuration is shown in fig. 3.14. The figure illustrates that the previously examined cross section (cut A1) is the main contribution to the capacitances. Nevertheless, the top view depicts additional effects that may influence the total three dimensional parasitic capacitances: *(i)* The base and collector vias are checkered, *(ii)* the cross section differs in direction of cut A2 and *(iii)* the corner portions may influence the result.

To assess the impact of *(i)*, the contact vias of the BE and BC regions are simulated using the structures shown in fig. 3.15. The results are compared with the standard parallel plate capacitor (i.e. without checkering)

$$C'_{\mathrm{pp}} = \varepsilon_0 \varepsilon_{\mathrm{r}} \frac{b_{\mathrm{pp}}}{d_{\mathrm{pp}}}, \tag{3.9}$$

which is defined by the plate width b_{pp} and the distance between the two parallel plates d_{pp}. Table 3.4 concludes that it is not necessary to incorporate the influence of the checkered vias for long transistors by comparing the simulation result C_{sim} with C_{pp}. This is the case not only due to the small error, but also because the via capacitance is only a part of the total spacer capacitance. As the distance between the checkered vias is not much larger than the via size, most of the field lines are ending at the facing edges and hence, the simulation result is close to the parallel plate capacitance.

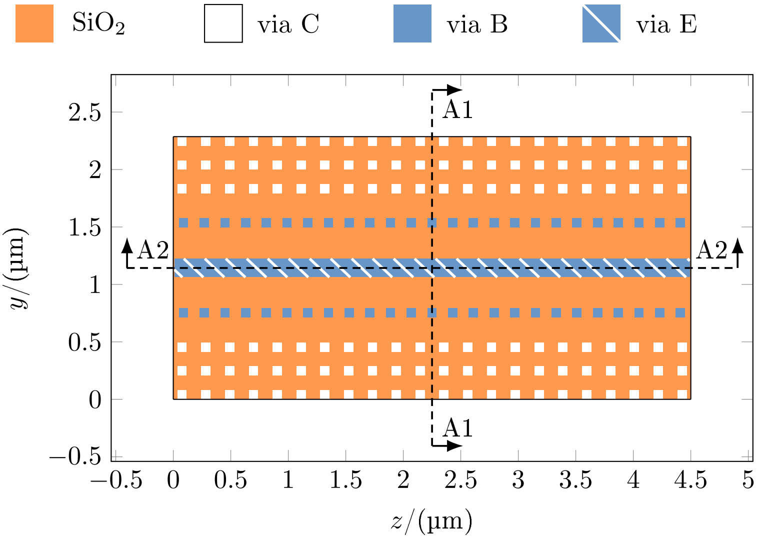
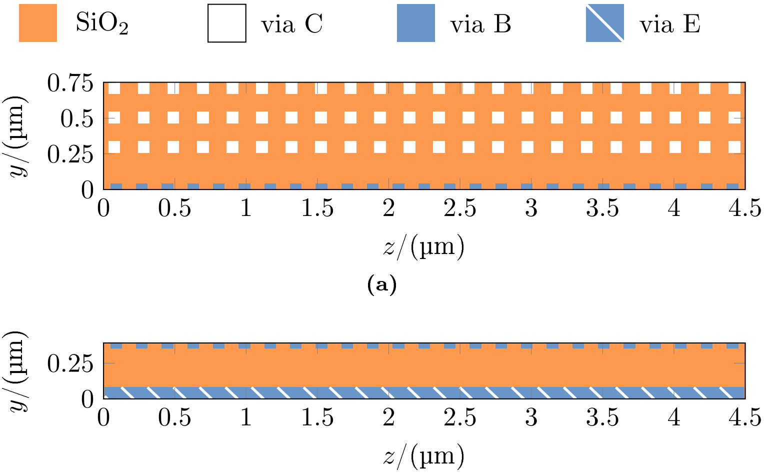


Figure 3.14: Contact via top view for a device in CBEBC configuration with a drawn emitter length of 4.5 µm.



(b)

Figure 3.15: Top view for a device with a drawn emitter length of 4.5 µm for **(a)** the BC and **(b)** the BC contact vias used for the capacitance simulations.

BC via array (unit)	C'_{sim} (fF/µm)	C'_{pp} (fF/µm)	error (%)
value	0.652	0.719	10.3
BE via array (unit)	**C'_{sim} (fF/µm)**	**C'_{pp} (fF/µm)**	**error (%)**
value	0.555	0.576	3.6

Table 3.4: Comparison for assessing the impact of checkered vias on the parasitic capacitances.

(ii): The cross section for the BE spacer structure obtained by cut A2 is identical to cut plane A1, except for the missing base via. As has been already pointed out for fig. 3.12, nearly no field lines end at the base contact via and therefore, the previous result for $C'_{\mathrm{BE,par}}$ is also applicable in direction of cut A2. This was also verified by simulations leading to an error of only 2 % for this assumption. For the BC spacer an additional component between the base polysilicon and the buried layer (h_{ox}) is taken into account for the lateral extension $l_{\mathrm{ex}} = 270\,\mathrm{nm}$ in z direction (starting from the shallow trench isolation (STI) up to the deep trench) by applying (3.9) leading to $C'_{\mathrm{BC,par,z}} = 0.024\,\mathrm{fF/µm}$.

Finally, the total parasitic capacitances can be determined for every device geometry by

$$\begin{aligned} C_{\mathrm{BE,par}} &= C'_{\mathrm{BE,par}} P_{\mathrm{E0}} \\ C_{\mathrm{BC,par}} &= 2C'_{\mathrm{BC,par}} l_{\mathrm{E0}} + 2C'_{\mathrm{BC,par},z} \left(b_{\mathrm{E0}} + 2b_{\mathrm{ex}}\right), \end{aligned} \tag{3.10}$$

with

$$\begin{aligned} b_{\mathrm{ex}} &= b_{\mathrm{s,tot}} + b_{\mathrm{po}} + b_{\mathrm{cB}} + b_{\mathrm{cB,po}} \\ b_{\mathrm{s,tot}} &= b_{\mathrm{s}} + b_{\mathrm{so}} + b_{\mathrm{ov}}. \end{aligned} \tag{3.11}$$

Unfortunately, the value determined for the total spacer capacitance $C'_{\mathrm{BE,par}}$ does not correspond to its effective portion required for the model, as the observed laterally extended emitter doping in fig. 3.5 will short part of the total capacitance. Additionally, the region underneath the spacer is – in part – undoped and would rather act as an insulator than a conductor and thus, decreases the capacitance additionally. For the extraction, no final evaluation can be performed and assumptions have to be made. As a rough estimation, the dimension b_s is set to 5 nm for including the effect of a laterally extended emitter doping and the undoped region, leading to an effective capacitance of $C'_\mathrm{BE,par,eff} = 0.416\,\mathrm{fF/\mu m}$ that replaces $C'_\mathrm{BE,par}$.

3.3 BE and BC junction capacitances

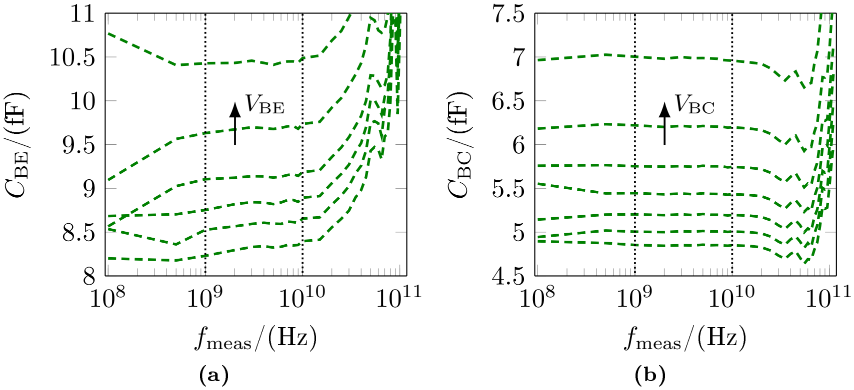
After determining the total capacitances C_BE and C_BC based on cold S-parameter measurements according to (3.12), an appropriate extraction frequency (f_ext) needs to be selected. f_ext needs to be in a certain range of the measurement frequency f_meas to maximize the accuracy of the measurement and the deembedding. Based on the data shown in fig. 3.16, $f_\mathrm{ext} = 5\,\mathrm{GHz}$ is selected.

$$\begin{aligned} C_\mathrm{BE} &= \frac{\Im\left(y_{11}+y_{21}\right)}{2\pi f_\mathrm{meas}} \\ C_\mathrm{BC} &= \frac{-\Im\left(y_{12}\right)}{2\pi f_\mathrm{meas}} \end{aligned} \tag{3.12}$$

Subtracting the spacer capacitance portion from the total capacitances by applying (3.13), the junction capacitance extraction can be performed using PoA separation. As fig. 3.17 shows, the BC capacitance scales well for all device sizes. Contrary to that, the BE capacitance does not scale for the smallest device width, as was expected from the scalability exercise for the collector current in section 3.1. However, additionally the BE capacitance of the largest device width does not align well with the rest of the data.

$$\begin{aligned} C_\mathrm{jE,tot} &= C_\mathrm{BE} - C_\mathrm{BE,par} \\ C_\mathrm{jC,tot} &= C_\mathrm{BC} - C_\mathrm{BC,par} \end{aligned} \tag{3.13}$$

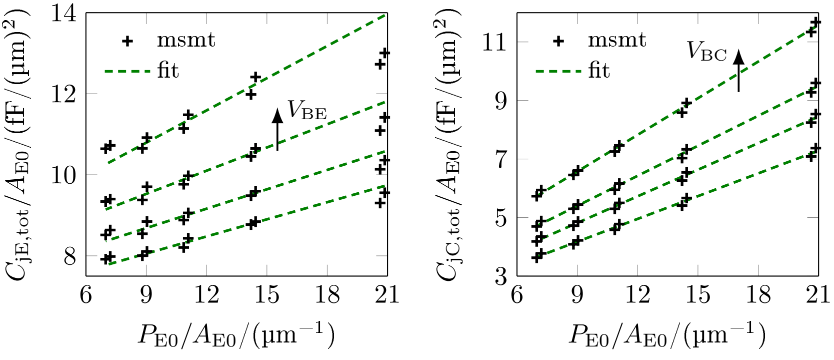
As the base and emitter doping for the HS, MV and HV transistors can be assumed to be identical within the process tolerances, the BE capacitances need to be identical as well. This is the case, as can be observed in figures 3.19 and 3.20. Conversely, due to the different collector doping of the three transistor flavors, the BC capacitances must be different, too.



(a) **(b)**

Figure 3.16: Total measured capacitance vs. frequency and different voltages of a HS transistor with an emitter area of $A_{\mathrm{drawn}} = 0.18\,\mu\mathrm{m} \times 4.5\,\mu\mathrm{m}$ (process of [76]) for **(a)** the base emitter capacitance and **(b)** the base collector capacitance. The region between the dotted lines indicates a reasonable frequency range suitable for extraction.

Also, a large noise level is observed for the measured BE capacitance in all corresponding plots. This behavior can be explained with fig. 3.18: During the deembedding of the structure, the capacitances of the “Open” are subtracted from the total capacitances measured for the transistor to account for the external influence of the pad and metal layers. As the capacitances attached to the substrate node ($C_{\mathrm{SE,o}}$, $C_{\mathrm{SB,o}}$, $C_{\mathrm{SC,o}}$) can be up to ten times larger than $C_{\mathrm{BE,o}}$, $C_{\mathrm{BC,o}}$ and $C_{\mathrm{CE,o}}$, they become a dominant factor. $C_{\mathrm{SE,o}}$, $C_{\mathrm{SB,o}}$ and $C_{\mathrm{SC,o}}$ assume a value of about 25 fF for modern process technologies regardless of the transistor size. Typically, the substrate node is shorted with the emitter at metal layer 1 in the S-parameter transistor test structures. Consequently, $C_{\mathrm{SB,o}}$ and $C_{\mathrm{SC,o}}$ are added to $C_{\mathrm{BE,o}}$ and $C_{\mathrm{CE,o}}$, respectively and need to be deembedded by $C_{\mathrm{BE}} = C_{\mathrm{BE,tot}} - C_{\mathrm{BE,o}} - C_{\mathrm{SB,o}}$. Since $C_{\mathrm{SB,o}}$ is very large, C_{BE} can become a residual, especially for small transistors. Note that C_{BC} is not affected because the large substrate capacitances were added to the emitter node. An effective workaround for the problem is to fabricate transistors also in common collector configuration for HF-measurements.



(a) **(b)**

Figure 3.17: Perimeter over area separation of HS transistors with l_{drawn} = (4.5 and 9) µm and b_{drawn} = (180 to 378) nm (process of [76]) for different voltages. Capacitance data (markers) and linear fit (lines) for **(a)** the base emitter capacitance and **(b)** the base collector capacitance.

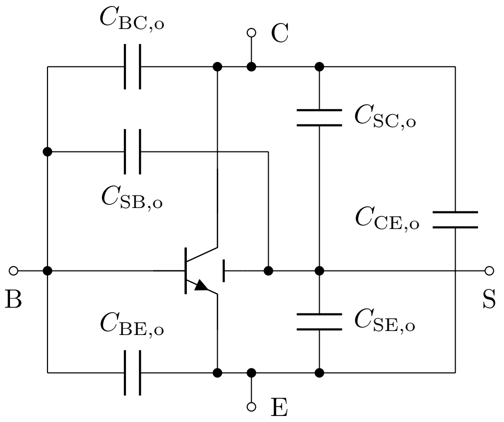
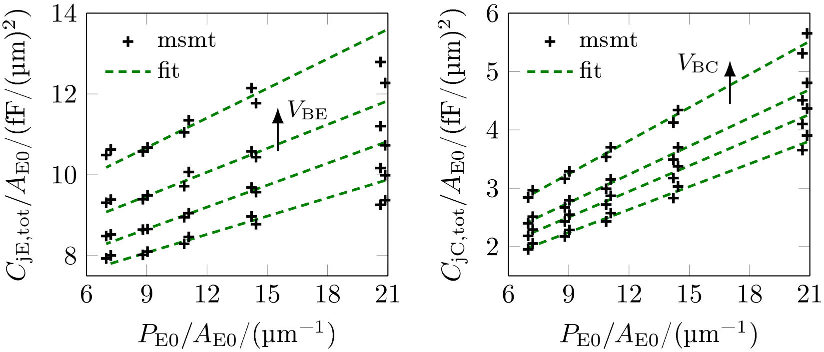
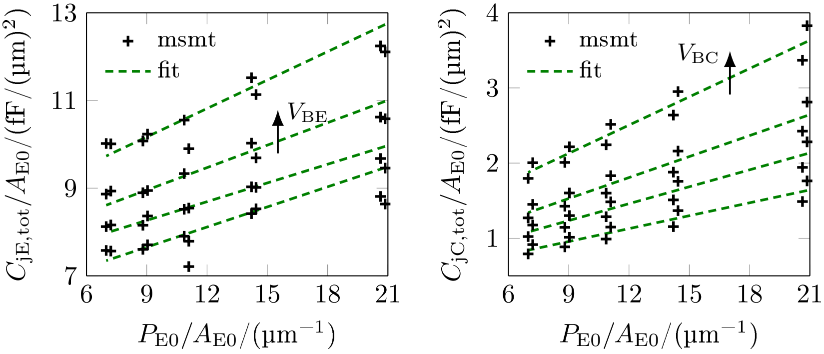


Figure 3.18: Transistor setup to illustrate the impact of pad and metal capacitances – represented by $C_{SE,o}$, $C_{SB,o}$, $C_{SC,o}$, $C_{BE,o}$, $C_{BC,o}$ and $C_{CE,o}$ – on transistor characterization.



(a) **(b)**

Figure 3.19: Perimeter over area separation of MV transistors with $l_{\mathrm{drawn}} = (4.5 \text{ and } 9)\,\mathrm{µm}$ and $b_{\mathrm{drawn}} = (180 \text{ to } 378)\,\mathrm{nm}$ (process of [76]) for different voltages. Capacitance data (markers) and linear fit (lines) for **(a)** the base emitter capacitance and **(b)** the base collector capacitance.



(a) **(b)**

Figure 3.20: Perimeter over area separation of HV transistors with $l_{\mathrm{drawn}} = (4.5 \text{ and } 9)\,\mathrm{µm}$ and $b_{\mathrm{drawn}} = (180 \text{ to } 378)\,\mathrm{nm}$ (process of [76]) for different voltages. Capacitance data (markers) and linear fit (lines) for **(a)** the base emitter capacitance and **(b)** the base collector capacitance.

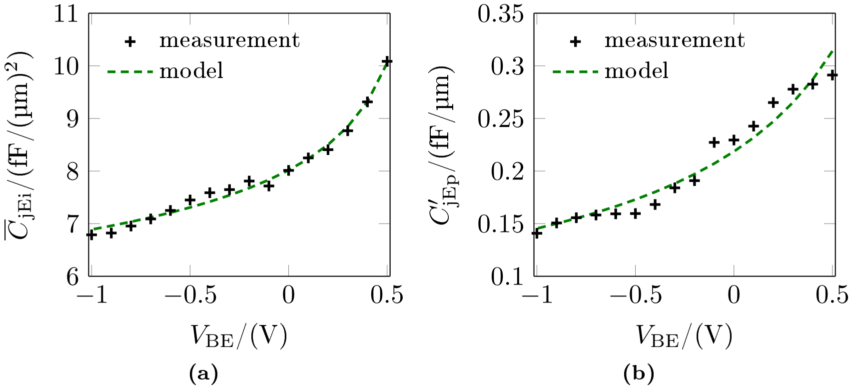
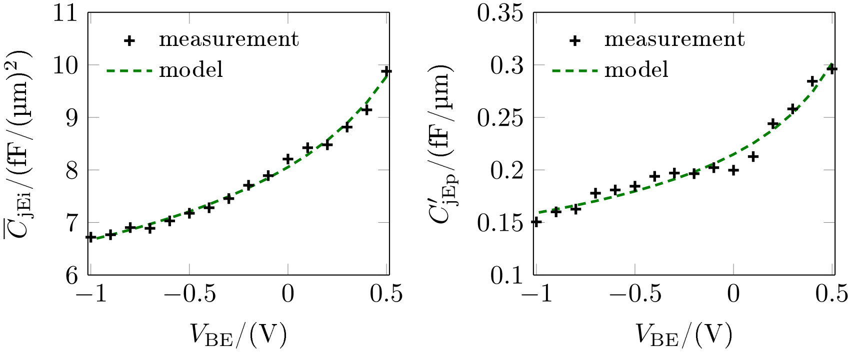


Figure 3.21: Comparison of the BE junction capacitance data obtained by the perimeter over area separation with the HICUM model description (HS transistors, process of [76]). Capacitance data (markers) and fit (lines) for **(a)** the internal BE capacitance $\overline{C}_{\mathrm{jEi}}$ and **(b)** the peripheral BE capacitance C'_{jEp}.

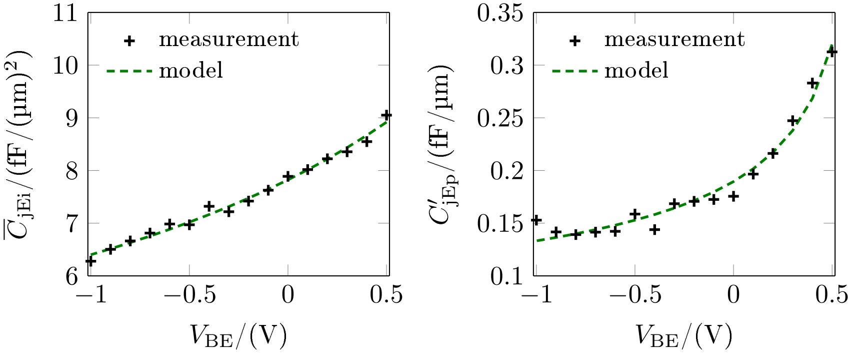
Based on the PoA separation, data for $\overline{C}_{\mathrm{jEi}}$ and C'_{jEp} were obtained and fitted with the capacitance description of HICUM, see fig. 3.21. The noise level for $\overline{C}_{\mathrm{jEi}}$ and C'_{jEp} is too large to determine reliable parameters for describing the shape vs. V_{BE}. This is confirmed by the results for the MV and HV transistors in figures 3.22 and 3.23, respectively. Especially the result for the HV flavor seems to be different: As the common emitter configuration of the measured transistors leads to an inaccuracy for C_{BE}, errors of up to 20 % are expected. The current S-parameter transistor test structure setup is a decisive factor and should be improved for reliable BE capacitance determination by including common collector setups. The quality for the MV fit is best and hence, corresponding parameters are used for all three transistor flavors and can be found in table 3.5.

The extraction for the parameters of the BC capacitances runs much smoother, as is shown in figures 3.24, 3.25 and 3.26 for the HS, MV and HV transistors, respectively. The corresponding parameters of the capacitance extraction can be found in table 3.6. The punch through voltages V_{PTCi} and V_{PTCx} were set to a sufficiently large value (100 V), as no punch through can



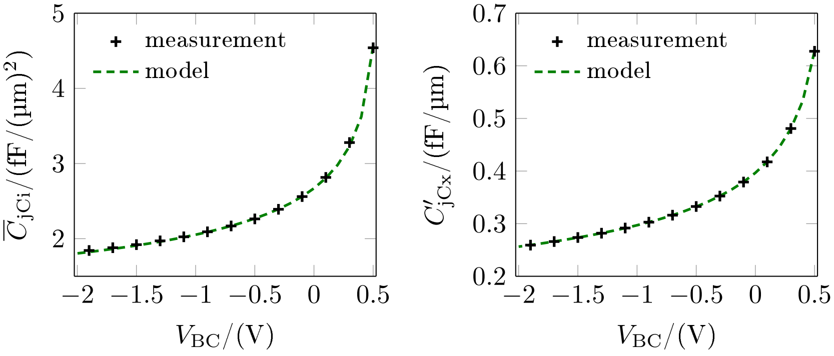
(a) **(b)**

Figure 3.22: Comparison of the BE junction capacitance data obtained by the perimeter over area separation with the HICUM model description (MV transistors, process of [76]). Capacitance data (markers) and fit (lines) for **(a)** the internal BE capacitance $\overline{C}_{\mathrm{jEi}}$ and **(b)** the peripheral BE capacitance C'_{jEp}.



(a) **(b)**

Figure 3.23: Comparison of the BE junction capacitance data obtained by the perimeter over area separation with the HICUM model description (HV transistors, process of [76]). Capacitance data (markers) and fit (lines) for **(a)** the internal BE capacitance $\overline{C}_{\mathrm{jEi}}$ and **(b)** the peripheral BE capacitance C'_{jEp}.



(a) **(b)**

Figure 3.24: Comparison of the BC junction capacitance data obtained by the perimeter over area separation with the HICUM model description (HS transistors, process of [76]). Capacitance data (markers) and fit (lines) for **(a)** the internal BC capacitance $\overline{C}_{\mathrm{jCi}}$ and **(b)** the external BC capacitance C'_{jCx}.

parameter ($\overline{C}_{\mathrm{jEi}}$) (unit)	$\overline{C}_{\mathrm{jEi0}}$ (fF/µm^2)	z_{Ei} (1)	V_{dEi} (V)
value	8.05	0.265	0.964
parameter (C'_{jEp}) (unit)	C'_{jEp0} (fF/µm)	z_{Ep} (1)	V_{dEp} (V)
value	0.215	0.390	0.862

Table 3.5: Extracted parameters for $\overline{C}_{\mathrm{jEi}}$ and C'_{jEp} of the capacitance description of HICUM.

be observed in the capacitance data. This assumption is reasonable for the HS and MV transistors because the collector doping is continuously changing and no abrupt change is present. Therefore, no precise punch through condition can be defined. Conversely, punch through exists for the HV transistors, but the available measurement range in the provided data is too limited to see the effect on the capacitance behavior.

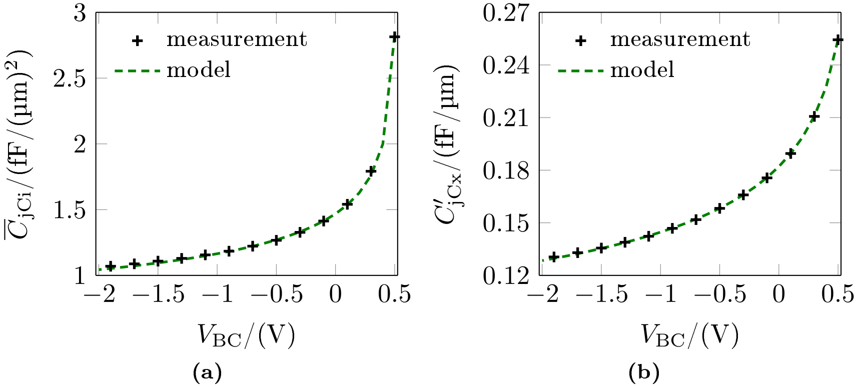


Figure 3.25: Comparison of the BC junction capacitance data obtained by the perimeter over area separation with the HICUM model description (MV transistors, process of [76]). Capacitance data (markers) and fit (lines) for **(a)** the internal BC capacitance $\overline{C}_{\mathrm{jCi}}$ and **(b)** the external BC capacitance C'_{jCx}.

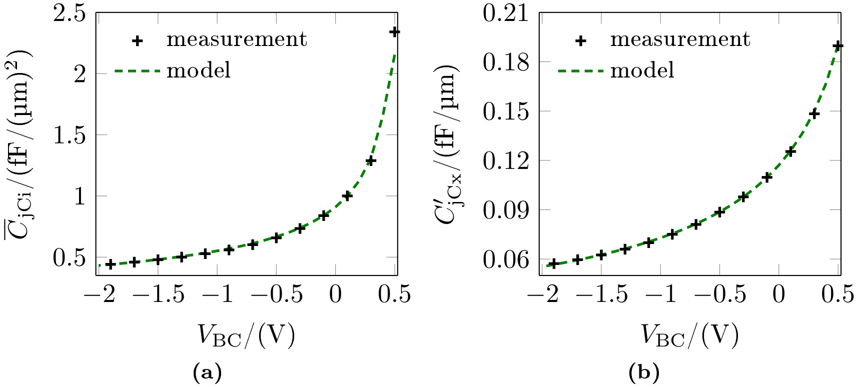


Figure 3.26: Comparison of the BC junction capacitance data obtained by the perimeter over area separation with the HICUM model description (HV transistors, process of [76]). Capacitance data (markers) and fit (lines) for **(a)** the internal BC capacitance $\overline{C}_{\mathrm{jCi}}$ and **(b)** the external BC capacitance C'_{jCx}.

parameter (HS) (unit)	$\overline{C}_{\mathrm{jCi0}}$ (fF/µm^2)	z_{Ci} (1)	V_{dCi} (V)
value	2.67	0.264	0.586
parameter (HS) (unit)	C'_{jCx0} (fF/µm)	z_{Cx} (1)	V_{dCx} (V)
value	0.343	0.311	0.652
parameter (MV) (unit)	$\overline{C}_{\mathrm{jCi0}}$ (fF/µm^2)	z_{Ci} (1)	V_{dCi} (V)
value	1.47	0.219	0.534
parameter (MV) (unit)	C'_{jCx0} (fF/µm)	z_{Cx} (1)	V_{dCx} (V)
value	0.182	0.256	0.687
parameter (HV) (unit)	$\overline{C}_{\mathrm{jCi0}}$ (fF/µm^2)	z_{Ci} (1)	V_{dCi} (V)
value	0.909	0.498	0.578
parameter (HV) (unit)	C'_{jCx0} (fF/µm)	z_{Cx} (1)	V_{dCx} (V)
value	0.117	0.670	0.971

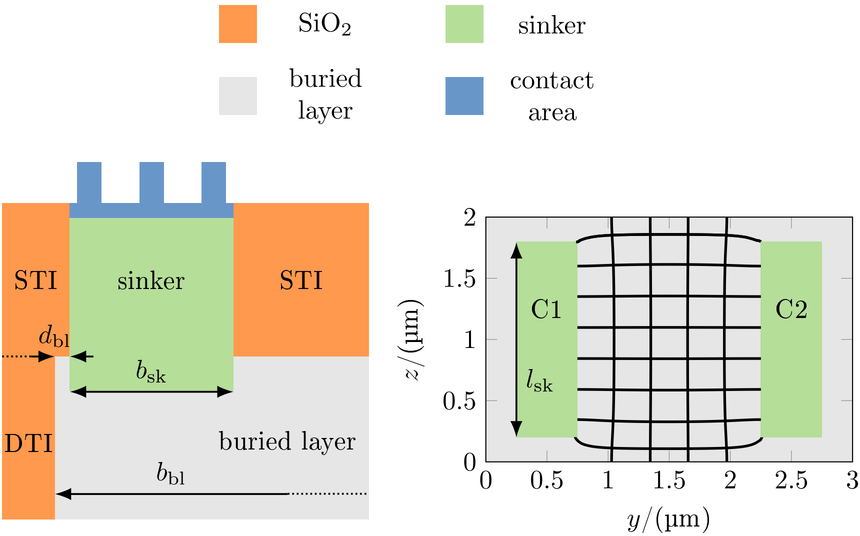
Table 3.6: Extracted parameters for $\overline{C}_{\mathrm{jCi}}$ and C'_{jCx} of the capacitance description of HICUM.

3.4 External collector resistance

The extraction of the external collector resistance R_{Cx} is based on the approach presented in [98, 99], using transistor structures in CBEBC configuration with varying buried layer length b_{bl}. As illustrated in fig. 3.27, both collector contacts are accessible for applying a voltage drop to the buried layer region. The measured resistance

$$\begin{aligned} R_{\mathrm{C1C2}} &= R_{\mathrm{bl}} + 2R_{\mathrm{sk}} \\ &\approx R_{\mathrm{s,bl}}\frac{d_{\mathrm{sk}}}{l_{\mathrm{sk}}} + 2\frac{\rho_{\mathrm{sk}}}{b_{\mathrm{sk}}l_{\mathrm{sk}}} \end{aligned} \tag{3.14}$$

between the contacts C1 and C2 includes the resistances associated to the



(a) **(b)**

Figure 3.27: **(a)** Schematic of the cross section with important dimensions for the collector resistance test structure. **(b)** Field lines and equipotentials of the corresponding top view for an exemplary test structure with realistic dimensions.

sinker and buried layer R_{bl} and R_{sk}, respectively. To obtain reliable results for the corresponding technology parameters $R_{s,bl}$ and ρ_{sk}, it is important to use four terminal sensing structures and to take into account current fringing. Following [98], the electrical correction offset $\Delta l_{sk,off}$ can be determined to map the fringing portion to an homogeneous resistor with the length $l_{sk,eff} = l_{sk} + \Delta l_{sk,off}$, replacing l_{sk}. Inherently, the fringing current of all device lengths is assumed to be identical, which is a valid assumption as long as the structures are not too short. By varying the buried layer width b_{bl} and plotting $R_{C1C2} l_{sk,eff}$ vs. $d_{sk} = b_{bl} - 2b_{sk} - 2d_{bl}$, the separation of $R_{s,bl}$ and ρ_{sk} is performed: The slope and y-axis intercept correspond to the buried layer sheet resistance $R_{s,bl}$ and $2\rho_{sk}/b_{sk}$, respectively.

Another option is to use the method described in [100], which generalized the approach of [101] by compensating the impact of fringing using resistances instead of currents. Although originally developed for the base resistance,

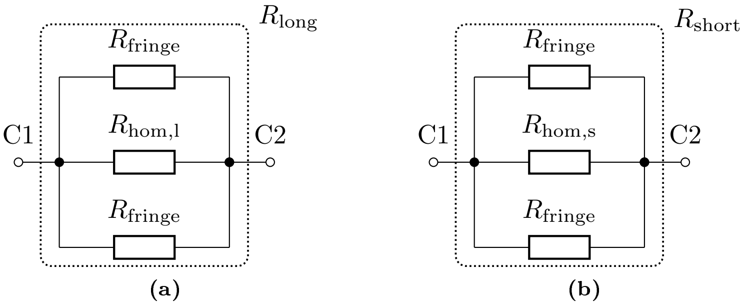


Figure 3.28: Equivalent circuit of the proposed method adapted from [100]: Resistance components for a long **(a)** and a short collector resistance test structure **(b)**.

the method is also applicable to the external collector resistance. Here, the resistance R_{fringe} caused by the fringing current is assumed to be identical for two different device lengths, as illustrated in fig. 3.28. The main advantage over [98] is that no fitting procedure is required for determining $\Delta l_{\text{sk,off}}$. By performing a simple subtraction, the fringing components cancel each other and a part of the total resistance remains. This homogeneous resistance

$$\begin{aligned} R_{\text{hom}} &= \frac{1}{1/R_{\text{long}} - 1/R_{\text{short}}} \\ &= \frac{1}{1/R_{\text{hom,l}} - 1/R_{\text{hom,s}}} \end{aligned} \tag{3.15}$$

does not contain R_{fringe} and can be calculated for different buried layer widths. Consequently, a slightly modified form of (3.14) is applied to the data:

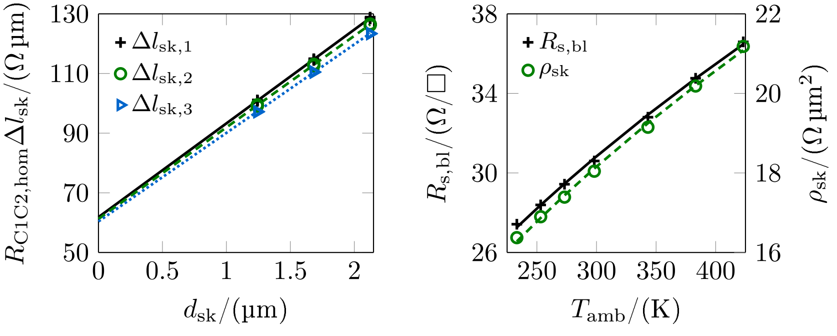
$$\begin{aligned} R_{\text{C1C2,hom}} &= R_{\text{bl,hom}} + 2R_{\text{sk,hom}} \\ &= R_{\text{s,bl}}\frac{d_{\text{sk}}}{\Delta l_{\text{sk}}} + 2\frac{\rho_{\text{sk}}}{b_{\text{sk}}\Delta l_{\text{sk}}}, \end{aligned} \tag{3.16}$$

with the difference between the long and short resistance structure length $\Delta l_{\text{sk}} = l_{\text{sk,long}} - l_{\text{sk,short}}$. Applying the approach to measurement data of [76] leads to fig. 3.29 for the HS transistors. Note that the shortest available length ($l_{\text{sk}} = 405\,\text{nm}$) was excluded for the extraction. By repeating the strategy for different ambient temperatures T_{amb} and assuming $T = T_{\text{amb}}$, additional data is generated. The temperature dependence implemented in HICUM for a resistance (mainly capturing the temperature dependent mobility) is modeled by the simple exponential dependence listed in (3.17) using the parameter ζ_{r} and the reference temperature T_0. For $R_{\mathrm{s,bl}}$ and ρ_{sk}, (3.17) is applied and the corresponding parameters ζ_{rbl} and ζ_{rsk} are extracted by a least square fit. The results for the MV and HV transistor versions are shown in fig. 3.30 along with the summarized parameter values in table 3.7. The parameters of the HS and MV transistor flavors differ within the process tolerances, as they feature identical doping for the buried layer and sinker. There is no influence of the selectively implanted collector (SIC) on the results as d_{sk} is not varied by changing the emitter width, but the width of the buried layer under the STI.

$$R(T) = R(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{\mathrm{r}}} \tag{3.17}$$

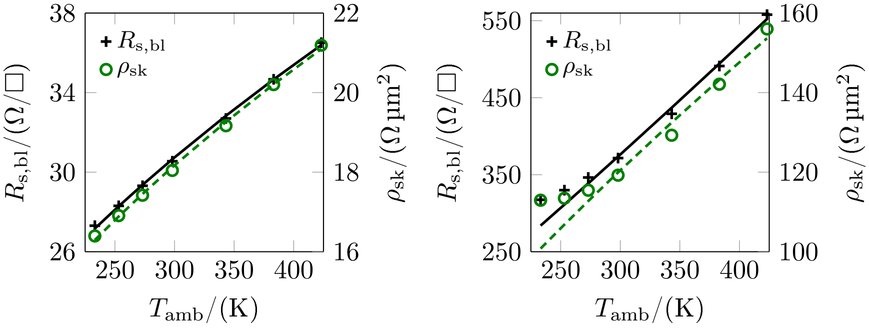
For the extraction, an identical voltage drop should be applied for different structure lengths to obtain similar conditions for the electric field within the buried layer. The provided measurements are forced current measurements and therefore, appropriate bias points had to be selected manually. It is advised to apply identical voltages for future measurements instead. An additional uncertainty is caused by the checkered contact configuration and the inconsistent contact areas of the test structure layout: The contact resistance ρ_{sk} consists of the vertical via resistance, the interface resistances (via/silicide/poly/mono stack), the sinker resistance itself and a part of the vertical buried layer resistance, which all feature a slightly different area. Ultimately, the resistance can only be normalized to a single area: $A_{\mathrm{sk}} = b_{\mathrm{sk}}\Delta l_{\mathrm{sk}}$. If the ratios between corresponding contact areas differ for different device lengths, an error for the determination of $R_{\mathrm{C1C2,hom}}$ is caused.

The value of R_{Cx} required for the HICUM modelcard of the actual device can be determined by means of device simulations using the previous extraction results. Actually, this requires 3D analyses, but viewing the buried layer as a resistive sheet with the sheet resistance $R_{\mathrm{s,bl}}$, the task can be reduced to a two dimensional problem without a considerable loss of accuracy. During forward active transistor operation, the collector current is injected into the



(a) **(b)**

Figure 3.29: Results of the external collector resistance extraction using an adapted method of [100] for three different Δl_{sk} and various bias (HS transistors, process of [76]). **(a)** Resistance data (markers) and linear extrapolation (lines) for $\Delta l_{\mathrm{sk,1}} = 4.5\,\mu\mathrm{m}$, $\Delta l_{\mathrm{sk,2}} = 7.65\,\mu\mathrm{m}$ and $\Delta l_{\mathrm{sk,3}} = 3.15\,\mu\mathrm{m}$ at $T_{\mathrm{amb}} = 25\,°\mathrm{C}$. **(b)** Comparison of measurements (markers) and model (lines) for the average values of $R_{\mathrm{s,bl}}$ and ρ_{sk} vs. temperature ($b_{\mathrm{sk}} = 590\,\mathrm{nm}$).



(a) **(b)**

Figure 3.30: Results of the external collector resistance extraction using an adapted method of [100] for three different Δl_{sk} and various bias (process of [76]). Comparison of measurements (markers) and model (lines) for the average values of $R_{\mathrm{s,bl}}$ and ρ_{sk} vs. temperature ($b_{\mathrm{sk}} = 590\,\mathrm{nm}$) for **(a)** the MV transistor and **(b)** the HV transistor versions. As the HV flavors do not feature a buried layer, the specific resistances increase significantly.

parameter (HS) (unit)	$R_{\mathrm{s,bl}}$ $(\Omega/\square)$	ρ_{sk} $(\Omega\,\mu\mathrm{m}^2)$	ζ_{rbl} (1)	ζ_{rsk} (1)
value	30.74	18.11	0.488	0.434
parameter (MV) (unit)	$R_{\mathrm{s,bl}}$ $(\Omega/\square)$	ρ_{sk} $(\Omega\,\mu\mathrm{m}^2)$	ζ_{rbl} (1)	ζ_{rsk} (1)
value	30.65	18.13	0.491	0.433
parameter (HV) (unit)	$R_{\mathrm{s,bl}}$ $(\Omega/\square)$	ρ_{sk} $(\Omega\,\mu\mathrm{m}^2)$	ζ_{rbl} (1)	ζ_{rsk} (1)
value	373.6	119.9	1.12	0.707

Table 3.7: Parameters of the external collector resistance description ($R_{\mathrm{s,bl}}$ and ρ_{sk}) for all three transistor flavors.

internal collector region along the buried layer and consequently, the current "disappears" from the resistive sheet. This behavior can be described by a constant recombination current density distributed over the internal collector region. Basically, the procedure is identical with the quasi-3D simulations in [94] for the base, except for the effect of current crowding. Therefore, only simulations at sufficiently small bias will lead to valid results. Fig. 3.31 shows an exemplary simulation result: In comparison to the collector test structure field distribution, the current flow is directed to the internal collector and therefore, the field lines are much more inhomogeneously distributed.

Note that the sinker resistance cannot be included in the 2D simulations and needs to be added analytically because the current flow direction at the sinker is perpendicular to the simulated current sheet. Hence, the boundary of the sinker to the buried layer is assumed to be an equipotential surface represented by an ideal contact within the simulations. After determining the geometry-dependent buried layer resistance $R_{\mathrm{bl,sim}}$ by means of device simulation, the sinker portion is added to R_{Cx} using (3.18). The final parameter values for R_{Cx} obtained by the method are listed in appendix A.1 for all relevant device geometries.

$$R_{\mathrm{Cx}}\left(T_0\right) = \frac{\rho_{\mathrm{sk}}}{2b_{\mathrm{sk}}l_{\mathrm{sk}}} + R_{\mathrm{bl,sim}} \tag{3.18}$$

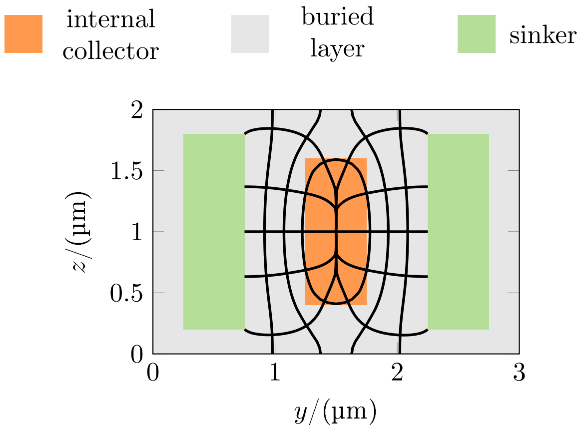


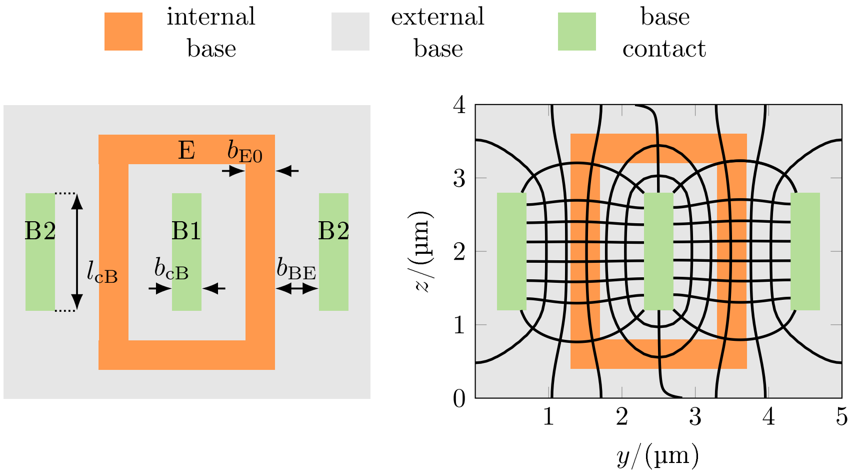
Figure 3.31: Simulated field lines and equipotentials of the buried layer for an exemplary device in forward active operation.

3.5 Base resistance

The base resistance $R_B = R_{Bi} + R_{Bx}$ is one of the elements with the largest impact on the maximum oscillation frequency f_{max}. Also, it is an important quantity to draw conclusions for the base doping. To extract the internal base resistance R_{Bi} and external component R_{Bx}, tetrode structures can be used for applying the approach of [100]. A tetrode consists of a ring emitter structure – with the internal base underneath – to electrically separate two external (polysilicon) base regions, which are connected with the contacts B1 and B2, as illustrated in fig. 3.32. Neglecting the contact resistance ($\rho_{B,cont} \approx 0.2\,\Omega\,\mu m^2$), the corresponding equivalent circuit of the tetrode is easily drawn (see fig. 3.33). Hence, the total resistance R_{B1B2} between the contacts evaluates to

$$R_{B1B2} = \frac{R_{Bi}}{2} + R_{Bx}. \tag{3.19}$$

As already pointed out for the external collector resistance, also for the base resistance four terminal sensing structures need to be used for reasonable accuracy. To take into account the apparent current spreading, the idea of fig. 3.28 and (3.15) are applied to the tetrode structure: By subtracting the



(a) **(b)**

Figure 3.32: (a) Schematic for the base resistance test structure illustrating important dimensions (top view). **(b)** Field lines and equipotentials of an exemplary 2D simulation.

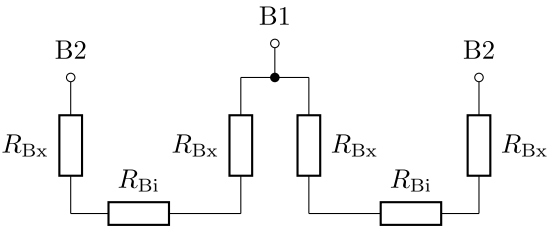
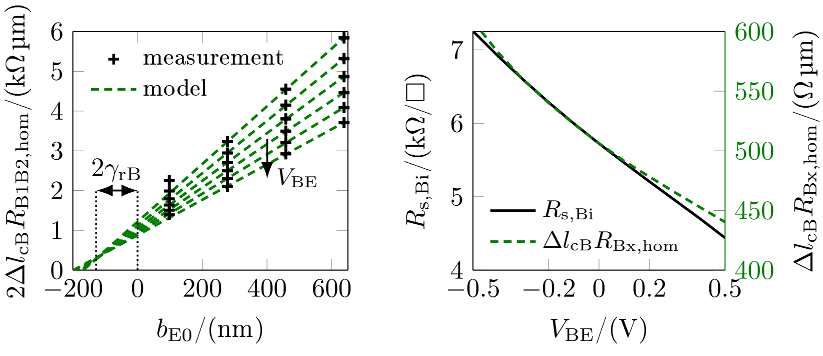


Figure 3.33: Equivalent circuit of a tetrode structure neglecting the contact resistance of the base.

conductance of two different tetrode lengths, the inhomogeneous resistance components cancel each other and a part of the homogeneous resistance remains (only valid for long structures). Neglecting the contact resistance, the corresponding resistance portion

$$\begin{aligned} R_{\mathrm{B1B2,hom}} &= \frac{R_{\mathrm{Bi,hom}}}{2} + R_{\mathrm{Bx,hom}} \\ &= R_{\mathrm{s,Bi}} \frac{b_{\mathrm{E0}}}{2\Delta l_{\mathrm{cB}}} + R_{\mathrm{Bx,hom}} \end{aligned} \tag{3.20}$$



(a) **(b)**

Figure 3.34: Results of the resistance extraction using the method of [100] for $\Delta l_B = 9\,\mu m$, $V_{BE} = (-0.5 \text{ to } 0.5)\,V$ and $V_{CE} = 0\,V$ (HS transistors, process of [76], $T_{amb} = 25\,°C$). **(a)** Resistance data (markers) and linear extrapolation (lines). **(b)** $R_{s,Bi}$ and $\Delta l_{cB} R_{Bx,hom}$ vs. V_{BE} ($V_{CE} = 0\,V$).

consists of the sheet resistance of the internal base $R_{s,Bi}$ and the homogeneous external base resistance $R_{Bx,hom}$. $\Delta l_{cB} = l_{cB,long} - l_{cB,short}$ represents the difference between the long and short tetrode structure length. To proceed with the extraction, (3.20) is multiplied with $2\Delta l_{cB}$ leading to

$$2\Delta l_{cB} R_{B1B2,hom} = R_{s,Bi} b_{E0} + 2\Delta l_{cB} R_{Bx,hom}. \tag{3.21}$$

By varying the emitter width and plotting $2\Delta l_{cB} R_{B1B2,hom}$ vs. b_{E0}, the separation of $R_{s,Bi}$ and $R_{Bx,hom}$ is performed: The slope and y-axis intercept correspond to the internal base sheet resistance $R_{s,Bi}$ and $2\Delta l_{cB} R_{Bx,hom}$, respectively. Fig. 3.34 illustrates the extraction result for the HS transistor version of the process of [76]. The electrical dimension offset $2\gamma_{rB}$ describes the width required to obtain a bias independent axis intercept $2\Delta l_{cB} R_{Bx,hom}$.

To process the result for $R_{Bx,hom}$ further, the resistance components of R_B are illustrated in fig. 3.35: As can be observed, the external base resistance

$$R_{Bx,hom} = R_{link,hom} + \underbrace{R_{s,po}\frac{b_{pm}}{\Delta l_{cB}}}_{R_{po}} + \underbrace{R_{s,sil}\frac{b_{sil}}{\Delta l_{cB}}}_{R_{sil}} \tag{3.22}$$

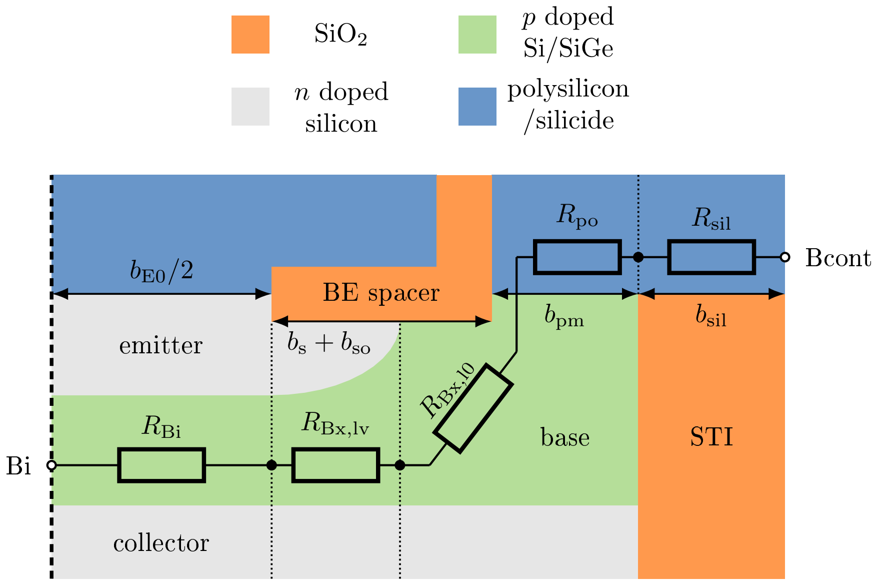


Figure 3.35: Schematic transistor cross section with important dimensions to illustrate the base resistance components.

consists of the sheet resistances of the base polysilicon $R_{s,po}$ and silicide $R_{s,sil}$, as well as the base link $R_{link,hom}$. $R_{link,hom}$ in turn consists of the bias dependent portion $R_{Bx,lv}$ – caused by the modulation of the peripheral space charge region (SCR) – and the bias independent portion $R_{Bx,l0}$, which is linked to the interface resistance of the base poly- to monosilicon, the vertical resistance contribution underneath and the sheet resistance further away from the BE junction. Rearranging (3.22),

$$\Delta l_{cB} R_{link,hom} = \Delta l_{cB} R_{Bx,hom} - R_{s,po} b_{pm} - R_{s,sil} b_{sil} \tag{3.23}$$

can be used to calculate $\Delta l_{cB} R_{link,hom}$ applying technology data for $R_{s,po}$ and $R_{s,sil}$. Subsequently, the result for $\Delta l_{cB} R_{link,hom}$ needs to be assigned to the respective base regions. To do so, assumptions have to be made because the information about the base link is limited:

(i) The bias dependent portion of the base link resistance ($R_{Bx,lv}$) is assumed to be linked with the electrical dimension offset Δb_E (see

section 3.1), meaning that $R_{\mathrm{Bx,lv,hom}} = R_{\mathrm{s,Bx,lv}} \frac{|\Delta b_{\mathrm{E}}|/2}{\Delta l_{\mathrm{cB}}}$. $|\Delta b_{\mathrm{E}}|/2$ is a measure to describe the extended emitter doping diffusion and consequently, corresponds to the width relevant for the bias dependent portion of R_{Bx}.

(ii) Unfortunately, the measurements were conducted at $V_{\mathrm{CE}} = 0\,\mathrm{V}$: This setting leads to $V_{\mathrm{BE}} = V_{\mathrm{BC}}$ and therefore, the base collector SCR is modulated as well, causing an additional change of the base resistance vs. bias. This in turn leads to a very large value for γ_{rB} in case of the the HS transistor version with high SIC doping. Hence, γ_{rB} does no longer correspond to the effective width required to reproduce $R_{\mathrm{Bx,lv}}$ (assuming $R_{\mathrm{s,Bx,lv}} = R_{\mathrm{s,Bi}}$). To circumvent this issue, γ_{rB} of the MV or HV transistors can be used because the reduced collector doping prevents a change of the BC SCR width inside the base.

(iii) The bias independent portion $R_{\mathrm{Bx,l0}}$ consists of a vertical and horizontal component. Therefore, it can be viewed as a contact and sheet resistance, meaning that $R_{\mathrm{Bx,l0,hom}} = R_{\mathrm{s,Bx,l0}} \frac{b_{\mathrm{s}}+b_{\mathrm{so}}-|\Delta b_{\mathrm{E}}|/2}{\Delta l_{\mathrm{cB}}} + \frac{\rho_{\mathrm{Bx,l0}}}{\Delta l_{\mathrm{cB}} b_{\mathrm{pm}}}$ holds. Assuming a negligible contact resistance, $R_{\mathrm{s,Bx,l0}} \approx 2R_{\mathrm{s,Bi}}$ is obtained for the process of [76]: Typically, $R_{\mathrm{s,Bx,l0}}$ must be smaller than $R_{\mathrm{s,Bx,lv}}$ and $R_{\mathrm{s,Bi}}$, as the diffusion from the poly-base region increases the conductivity of the region. Since $R_{\mathrm{s,Bx,l0}} > R_{\mathrm{s,Bi}}$, the result would be unphysical and indicates that a relatively large vertical component must be present. Assuming $R_{\mathrm{s,Bx,l0}} = R_{\mathrm{s,Bi0}}$ leads to the lower estimate for $\rho_{\mathrm{Bx,l0}}$ and $R_{\mathrm{Bx,l0,hom}} = R_{\mathrm{s,Bi0}} \frac{b_{\mathrm{s}}+b_{\mathrm{so}}-|\Delta b_{\mathrm{E}}|/2}{\Delta l_{\mathrm{cB}}} + \frac{\rho_{\mathrm{Bx,l0}}}{\Delta l_{\mathrm{cB}} b_{\mathrm{pm}}}$ is used.

Finally, $R_{\mathrm{s,Bx,lv}}$ and $\rho_{\mathrm{Bx,l0}}$ can be calculated using

$$\begin{aligned} R_{\mathrm{s,Bx,lv}} &= R_{\mathrm{s,Bi}} \frac{\gamma_{\mathrm{rB}}}{|\Delta b_{\mathrm{E}}|/2} \\ \rho_{\mathrm{Bx,l0}} &= \left(R_{\mathrm{link,hom}} \Delta l_{\mathrm{cB}} - R_{\mathrm{s,Bx,lv}} \frac{|\Delta b_{\mathrm{E}}|}{2} - R_{\mathrm{s,Bi0}} \left[b_{\mathrm{s}} + b_{\mathrm{so}} - \frac{|\Delta b_{\mathrm{E}}|}{2} \right] \right) b_{\mathrm{pm}}. \end{aligned} \tag{3.24}$$

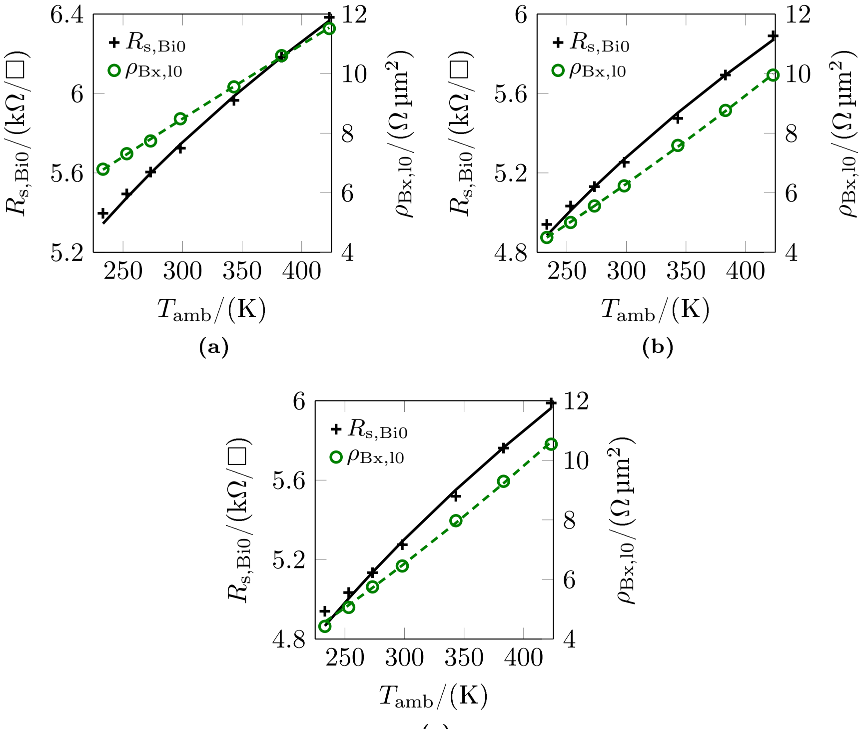
parameter (HS) (unit)	$R_{\mathrm{s,Bi0}}$ ($\Omega/\square$)	$R_{\mathrm{s,Bx,lv0}}$ ($\Omega/\square$)	$\rho_{\mathrm{Bx,l0}}$ ($\Omega\,\mu\mathrm{m}^2$)	ζ_{rBi} (1)	ζ_{rBx} (1)
value	5745	5873	8.44	0.294	0.894
parameter (MV) (unit)	$R_{\mathrm{s,Bi0}}$ ($\Omega/\square$)	$R_{\mathrm{s,Bx,lv0}}$ ($\Omega/\square$)	$\rho_{\mathrm{Bx,l0}}$ ($\Omega\,\mu\mathrm{m}^2$)	ζ_{rBi} (1)	ζ_{rBx} (1)
value	5270	5387	6.25	0.308	1.34
parameter (HV) (unit)	$R_{\mathrm{s,Bi0}}$ ($\Omega/\square$)	$R_{\mathrm{s,Bx,lv0}}$ ($\Omega/\square$)	$\rho_{\mathrm{Bx,l0}}$ ($\Omega\,\mu\mathrm{m}^2$)	ζ_{rBi} (1)	ζ_{rBx} (1)
value	5292	5410	6.48	0.341	1.41
parameter (generic) (unit)	γ_{rB} (nm)	$R_{\mathrm{s,po}}$ ($\Omega/\square$)	$R_{\mathrm{s,sil}}$ ($\Omega/\square$)	b_{pm} (nm)	b_{sil} (nm)
value	25.6	710	15	47	200

Table 3.8: Technology parameters of the base resistance description ($R_{\mathrm{s,Bi}}$, $R_{\mathrm{s,Bx,lv}}$ and $\rho_{\mathrm{Bx,l0}}$) for all three transistor flavors.

Using the temperature dependence of (3.17), the technology parameters are extracted and presented in table 3.8. The corresponding extraction is shown in fig. 3.36 for the HS, MV and HV transistor flavors.

Although HICUM does not offer a bias dependent external base resistance, the bias dependent portion of the external base-link resistance $R_{\mathrm{Bx,lv}}$ can be added to R_{Bi}. The value of R_{Bi0} and R_{Bx} required for the modelcard of the actual device can be determined by means of device simulations using the previous extraction results (similar to the determination of R_{Cx}). Again, quasi-3D simulations are performed, viewing the base region as a resistive sheet with several sheet resistances to model $R_{\mathrm{s,Bi0}}$, $R_{\mathrm{s,Bx,lv0}}$, $R_{\mathrm{s,Bx,l0}}$, $R_{\mathrm{s,po}}$ and $R_{\mathrm{s,sil}}$. During forward active transistor operation, the base current is injected into the emitter region along $b_{\mathrm{E0}} - \Delta b_{\mathrm{E}}$ and consequently, the current "disappears" from the resistive sheet. Similar to the treatment of the collector in section 3.4, this behavior is described by a recombination current density distributed over the emitter region.

Fig. 3.37 shows an exemplary simulation result. As the sheet resistance of the silicide is very low, the equipotential lines concentrate within the emitter and spacer region. $R_{\mathrm{B0}} = R_{\mathrm{Bi0}} + R_{\mathrm{Bx,sim}}$ is obtained by the simulation and



(a)

(b)

(c)

Figure 3.36: Results of the base resistance extraction using the method of [100] for $\Delta l_{\mathrm{B}} = 9\,\mu\mathrm{m}$, $V_{\mathrm{BE}} = 0\,\mathrm{V}$ and $V_{\mathrm{CE}} = 0\,\mathrm{V}$ (process of [76]). Comparison of measurements (markers) and model (lines) for $R_{\mathrm{s,Bi0}}$ and $\rho_{\mathrm{Bx,l0}}$ vs. temperature for the HS **(a)**, the MV **(b)** and the HV transistor versions **(c)**.

the resistance components have yet to be separated from each other. Thus, a second simulation is performed that only includes the internal and bias dependent spacer base region ($R_{\mathrm{s,Bi0}}$ and $R_{\mathrm{s,Bx,lv0}}$). The result corresponds to R_{Bi0} and can be subtracted from R_{B0} to calculate $R_{\mathrm{Bx,sim}}$.

Note that the vertical resistance component $\rho_{\mathrm{Bx,l0}}$ cannot be included in the simulations and needs to be added analytically afterwards using (3.25). The final parameter values for R_{Bi} and R_{Bx} obtained by the method are listed in appendix A.2 for all relevant device geometries.

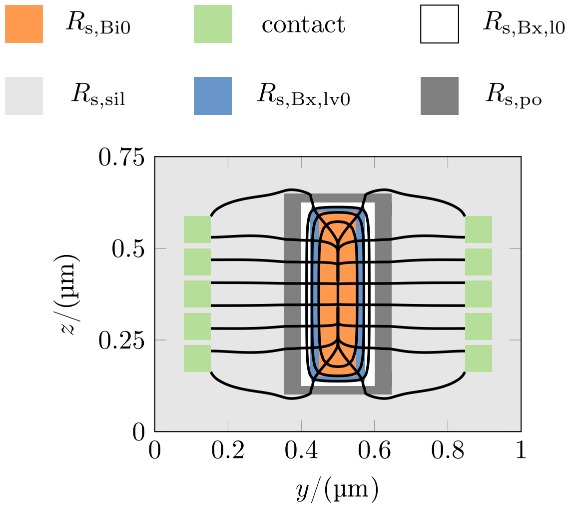


Figure 3.37: Simulated field lines and equipotentials of the base region for an exemplary device in forward active operation. The equipotential lines concentrate within the regions of high resistivity ($R_{\mathrm{s,Bi0}}$, $R_{\mathrm{s,Bx,lv0}}$ and $R_{\mathrm{s,Bx,l0}}$) and since the polysilicon and silicide sheet resistances are much lower, only a relatively small voltage drop is observed here.

$$R_{\mathrm{Bx}}\left(T_0\right) = \frac{\rho_{\mathrm{Bx,l0}}}{2 l_{\mathrm{pm}} b_{\mathrm{pm}}} + R_{\mathrm{Bx,sim}} \tag{3.25}$$

3.6 Substrate network

With the newest HICUM/L2 version (2.34), the substrate network has been extended to account for the peripheral isolation capacitance C_{SCp}, which is either caused by a bias dependent p-n junction or a bias independent isolation (DTI). The equivalent circuit is shown in fig 3.38 and can be used to calculate the impedance between the nodes C and S as a function of angular frequency $\omega = 2\pi f$:

$$Z_{\mathrm{CS,HICUM}}(\omega) = \frac{\frac{1}{\mathrm{j}\omega C_{\mathrm{SCp}}} \overset{Z_{\mathrm{CS,sim}}(\omega)}{\boxed{\left[\frac{1}{\mathrm{j}\omega C_{\mathrm{jS}}} + \frac{R_{\mathrm{su}}/(\mathrm{j}\omega C_{\mathrm{su}})}{R_{\mathrm{su}} + 1/(\mathrm{j}\omega C_{\mathrm{su}})}\right]}}}{\frac{1}{\mathrm{j}\omega C_{\mathrm{SCp}}} + \frac{1}{\mathrm{j}\omega C_{\mathrm{jS}}} + \frac{R_{\mathrm{su}}/(\mathrm{j}\omega C_{\mathrm{su}})}{R_{\mathrm{su}}+1/(\mathrm{j}\omega C_{\mathrm{su}})}} \tag{3.26}$$

(3.26) also contains the collector substrate junction capacitance C_{jS} and the intra-device substrate network (C_{su} and R_{su}). From measurements, the substrate impedance Z_{CS} can be determined by

$$Z_{\mathrm{CS}}(\omega) = 1/(y_{21} + y_{22}), \tag{3.27}$$

using the measured Y-parameters y_{21} and y_{22} of the respective device. Z_{CS} in turn consists of the frequency dependent substrate capacitance and resistance, C_{CS} and R_{CS}:

$$\begin{aligned} R_{\mathrm{CS}} &= \Re(Z_{\mathrm{CS}}) \\ C_{\mathrm{CS}} &= \Im(1/Z_{\mathrm{CS}})/\omega. \end{aligned} \tag{3.28}$$

To proceed with the extraction, the simplified substrate impedance $Z_{\mathrm{CS,sim}}$ is analyzed. For low frequencies, the limits

$$\begin{aligned} \lim_{\omega\to 0} R_{\mathrm{CS,sim}} &= R_{\mathrm{su}} \\ \lim_{\omega\to 0} C_{\mathrm{CS,sim}} &= C_{\mathrm{jS}} \end{aligned} \tag{3.29}$$

already give information on how to extract the parameters: C_{jS} and R_{su}

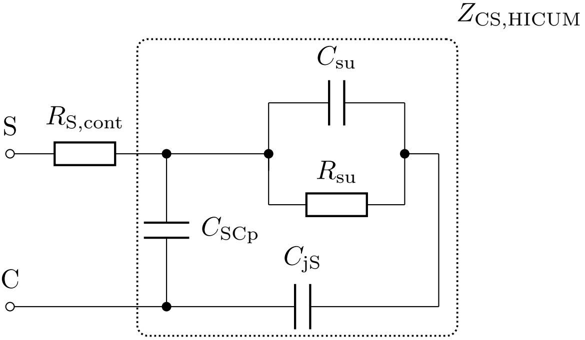


Figure 3.38: Substrate network of HICUM/L2 2.34 suitable for modeling both a junction and deep trench isolation with the corresponding impedance $Z_{\mathrm{CS,HICUM}}$ and a possible extension for high frequencies by adding $R_{\mathrm{S,cont}}$.

directly correspond to measurement data at low frequencies using (3.29). For high frequencies, the limits evaluate to

$$\begin{aligned} \lim_{\omega\to\infty} R_{\mathrm{CS,sim}} &= 0 \\ \lim_{\omega\to\infty} C_{\mathrm{CS,sim}} &= C_{\mathrm{CS,inf}} = \frac{C_{\mathrm{jS}}C_{\mathrm{su}}}{C_{\mathrm{jS}}+C_{\mathrm{su}}}. \end{aligned} \tag{3.30}$$

With the previous result for C_{jS}, (3.30) can be rearranged to calculate C_{su}. Applying the strategy to measurement data of [76] and using $C_{\mathrm{CS,inf}} = C_{\mathrm{CS}}$ at $f_{\mathrm{meas}} = 15\,\mathrm{GHz}$ leads to the result shown in fig. 3.39. As can be observed in the figures, the model shows good agreement for low to medium frequencies, but fails to capture the behavior at high frequencies. Nevertheless, as pointed out in [102, 103], the additional resistance $R_{\mathrm{S,cont}}$ (illustrated in fig. 3.38) can be added to the network to capture the high frequency behavior. The corresponding result is shown in fig. 3.40. Note though that the substrate is a strongly distributed network and therefore, the additional frequency range captured by a single discrete element is limited. Another downside is the increasing simulation runtime, as the node count of the compact model increases.

After the parameters have been determined for all relevant device geometries, a PoA separation can be performed to separate the area and peripheral

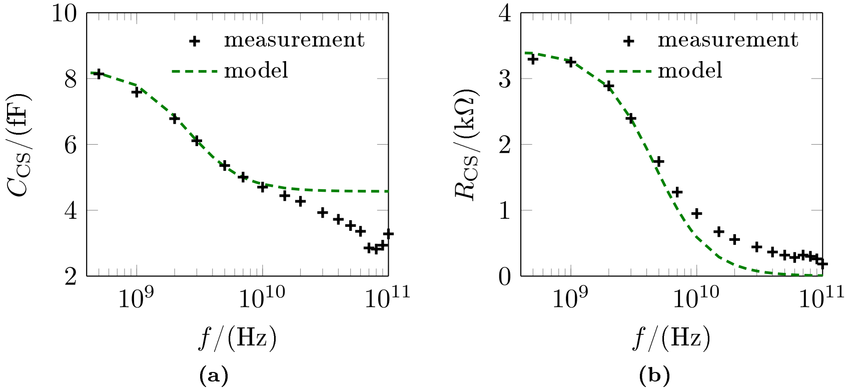


Figure 3.39: Results of the direct extraction of the substrate network for a device with $l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$ and $l_{\mathrm{drawn}} = 180\,\mathrm{nm}$ at $V_{\mathrm{CS}} = 0\,\mathrm{V}$ (HS transistor, process of [76], $T_{\mathrm{amb}} = 25\,°\mathrm{C}$). Comparison of measurements (markers) and model (lines) for **(a)** the substrate capacitance C_{CS} and **(b)** the substrate resistance R_{CS}.

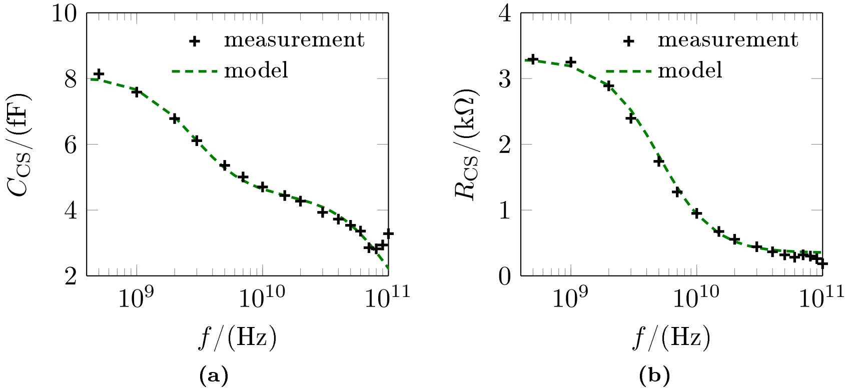
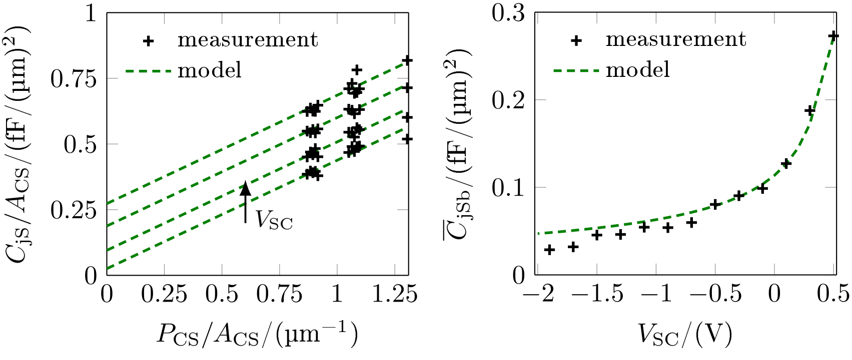


Figure 3.40: Results of the extended substrate network extraction (including $R_{\mathrm{S,cont}}$) for a device with $l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$ and $l_{\mathrm{drawn}} = 180\,\mathrm{nm}$ at $V_{\mathrm{CS}} = 0\,\mathrm{V}$ (HS transistor, process of [76], $T_{\mathrm{amb}} = 25\,°\mathrm{C}$). Comparison of measurements (markers) and model (lines) for **(a)** the substrate capacitance C_{CS} and **(b)** the substrate resistance R_{CS}.



(a) **(b)**

Figure 3.41: CS junction capacitance extraction for the HS transistors of [76]. Comparison of measurements (markers) and model (lines) for **(a)** the perimeter over area separation (devices with $l_{\mathrm{drawn}} = (3 \text{ to } 9)\,\mathrm{\mu m}$ and $b_{\mathrm{drawn}} = (180 \text{ to } 378)\,\mathrm{nm}$) for different voltages and **(b)** the bottom component $\overline{C}_{\mathrm{jSb}}$.

component of the junction capacitance from each other. Contrary to the example for the PoA shown in section 3.1, C_{jS} needs to be scaled with the collector substrate area A_{CS} and perimeter P_{CS}:

$$\begin{aligned} C_{\mathrm{jS}} &= \overline{C}_{\mathrm{jSb}} A_{\mathrm{CS}} + C'_{\mathrm{jSp}} P_{\mathrm{CS}} \\ A_{\mathrm{CS}} &= b_{\mathrm{bl}} \left(l_{\mathrm{sk}} + 2 d_{\mathrm{bl}} \right) \\ P_{\mathrm{CS}} &= 2 \left(b_{\mathrm{bl}} + l_{\mathrm{sk}} + 2 d_{\mathrm{bl}} \right) . \end{aligned} \tag{3.31}$$

Based on the result for the bottom component $\overline{C}_{\mathrm{jSb}}$ from the PoA separation (assuming a constant value $C'_{\mathrm{jSp}}(V_{\mathrm{CS}}) = \mathrm{const}$), data were fitted with the capacitance description of HICUM, see fig. 3.41. As C_{jS} corresponds to the capacitance at low frequencies, the noise level of the measurements is increased making the extraction somewhat difficult. Nevertheless, the agreement is adequate, as is also observed for the MV and HV transistor versions in fig. 3.42. Parameter values for all three transistor flavors can be found in table 3.9.

Contrary to C_{jS}, the elements for the intra-device coupling network cannot be scaled easily based on measurement data. Additionally, either complex three dimensional device simulations [104] or a Schwarz-Christoffel mapping

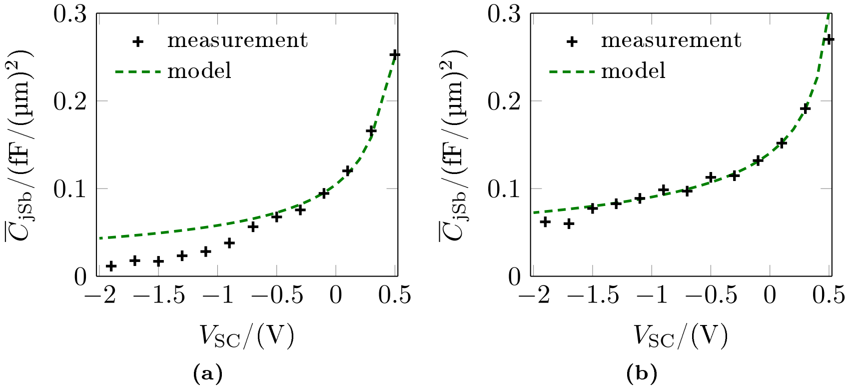


Figure 3.42: Comparison of measurements (markers) and model (lines) for the bottom component $\overline{C}_{\rm jSb}$ of the CS junction capacitance (process of [76]). Results for the MV transistor flavor **(a)** and HV transistors **(b)**.

parameter (HS) (unit)	$\overline{C}_{\rm jSb0}$ (fF/µm^2)	$z_{\rm Sb}$ (1)	$V_{\rm DSb}$ (V)	$C'_{\rm jSp}$ (fF/µm)
value	0.114	0.60	0.60	0.413
parameter (MV) (unit)	$\overline{C}_{\rm jSb0}$ (fF/µm^2)	$z_{\rm Sb}$ (1)	$V_{\rm DSb}$ (V)	$C'_{\rm jSp}$ (fF/µm)
value	0.104	0.60	0.60	0.423
parameter (HV) (unit)	$\overline{C}_{\rm jSb0}$ (fF/µm^2)	$z_{\rm Sb}$ (1)	$V_{\rm DSb}$ (V)	$C'_{\rm jSp}$ (fF/µm)
value	0.140	0.46	0.62	0.365

Table 3.9: Extracted parameters for $\overline{C}_{\rm jSb}$ of the capacitance description of HICUM and the bias independent component $C'_{\rm jSp}$ for all three transistor flavors.

approach in conjunction with physics-based equations [105] are required. As this would go beyond the scope of this thesis project, $C_{\rm su}$, $R_{\rm su}$ and $R_{\rm S,cont}$ are not scaled and remain associated to each individual transistor. Corresponding parameters for each individual device are listed in appendix A.3. Additionally, results for $C'_{\rm jSp}$ are illustrated.

3.7 Zero-bias hole charge

The hole charge Q_p describes the total charge related to the number of holes within the internal 1D transistor. Hence, the integration limits of

$$Q_\mathrm{p} = \underbrace{A_\mathrm{E,1D}}_{=1\,\mathrm{\mu m}^2} q \int_0^{L_x} p\mathrm{d}x \tag{3.32}$$

confine the region between the start of the mono emitter and the peak of the buried layer doping. The internal base sheet resistance $R_\mathrm{s,Bi}$ relates to Q_p by

$$1/R_\mathrm{s,Bi} = q \int_0^{L_x} p\mu_p \mathrm{d}x = Q_\mathrm{p}\overline{\mu}_p, \tag{3.33}$$

with the hole mobility μ_p and its average value $\overline{\mu}_p$ within the integration limits. Relating the sheet resistance of the base to its value at zero volt ($R_\mathrm{s,Bi0}$) leads to the ratio

$$r_\mathrm{zero} = \frac{R_\mathrm{s,Bi}}{R_\mathrm{s,Bi0}} = \frac{Q_\mathrm{p0}\overline{\mu}_{p0}}{Q_\mathrm{p}\overline{\mu}_p} \approx \frac{Q_\mathrm{p0}}{Q_\mathrm{p}}, \tag{3.34}$$

with the zero-bias hole charge Q_p0. Assuming $\overline{\mu}_p \approx \overline{\mu}_{p0}$, the terms cancel each other out and only the charges remain. Under low bias conditions, the hole charge only consists of the BE and BC depletion charges (Q_jEi and Q_jCi) and Q_p0. Hence, $Q_\mathrm{p} = Q_\mathrm{p0} + Q_\mathrm{jEi} + Q_\mathrm{jCi}$. Inserting this relation into (3.34) allows rearranging for Q_p0:

$$\begin{aligned} \frac{R_\mathrm{s,Bi}}{R_\mathrm{s,Bi0}} &\approx \frac{Q_\mathrm{p0}}{Q_\mathrm{p0} + Q_\mathrm{jEi} + Q_\mathrm{jCi}} \\ \Rightarrow Q_\mathrm{p0} &= \frac{Q_\mathrm{jEi} + Q_\mathrm{jCi}}{R_\mathrm{s,Bi0}/R_\mathrm{s,Bi} - 1}. \end{aligned} \tag{3.35}$$

Rewriting the equation using area normalized quantities leads to

$$\overline{Q}_\mathrm{p0} = \frac{\overline{Q}_\mathrm{jEi} + \overline{Q}_\mathrm{jCi}}{R_\mathrm{s,Bi0}/R_\mathrm{s,Bi} - 1}. \tag{3.36}$$

During the previous extraction steps (tetrode measurement evaluation and junction capacitance extraction), all required quantities to calculate $\overline{Q}_\mathrm{p0}$ have

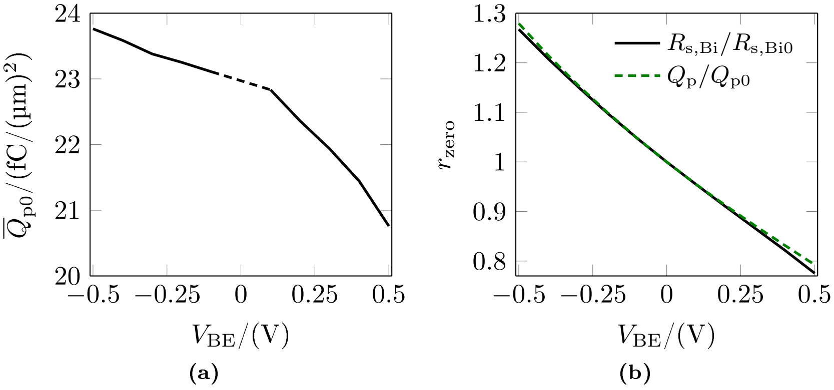


Figure 3.43: Results for the zero-bias hole charge determination for the HS transistors of [76] at $V_{\mathrm{CE}} = 0\,\mathrm{V}$. **(a)** $\overline{Q}_{\mathrm{p0}}$ obtained by (3.36) plotted vs. V_{BE}. The dashed line indicates the linear interpolation used to obtain the relevant zero-bias value. **(b)** Comparison between the charge and resistance ratio r_{zero} assuming the previously determined value for $\overline{Q}_{\mathrm{p0}}$ at zero bias.

been determined. Inserting them into (3.36) leads to the results shown in fig. 3.43. For $R_{\mathrm{s,Bi0}}/R_{\mathrm{s,Bi}} = 1$ the denominator approaches zero and hence, $\overline{Q}_{\mathrm{p0}}$ obtained by the method is undefined for $V_{\mathrm{BE}} = 0\,\mathrm{V}$. Therefore, the value for the zero-bias case needs to be calculated by interpolation.

With $\overline{Q}_{\mathrm{p0}}$ being known, it is possible to determine the average mobility of holes $\overline{\mu}_{p0}$ to get an idea if the physical model for the hole mobility is in line with the measured data:

$$\overline{\mu}_{p0} = \frac{1}{\overline{Q}_{\mathrm{p0}} R_{\mathrm{s,Bi0}}}. \tag{3.37}$$

All relevant values are listed in table 3.10 for all three transistor flavors. As can be observed from the data, $\overline{Q}_{\mathrm{p0}}$ is increasing for the MV and HV transistor versions. This is reasonable because the extension of the space charge region inside of the base reduces with decreasing collector doping and hence, the number of available holes increases. Note though that the accuracy of the determination method is about ±5 % (based on fig. 3.43).

parameter (HS) (unit)	$\overline{Q}_{\mathrm{p0}}$ (fC/µm^2)	$\overline{\mu}_{p0}$ (cm^2/(V s))
value	23.0	76.0
parameter (MV) (unit)	$\overline{Q}_{\mathrm{p0}}$ (fC/µm^2)	$\overline{\mu}_{p0}$ (cm^2/(V s))
value	24.0	79.2
parameter (HV) (unit)	$\overline{Q}_{\mathrm{p0}}$ (fC/µm^2)	$\overline{\mu}_{p0}$ (cm^2/(V s))
value	26.4	71.9

Table 3.10: Extracted parameters for $\overline{Q}_{\mathrm{p0}}$ and $\overline{\mu}_{p0}$ for all three transistor flavors.

3.8 Base current at low injection

Generally, the base current I_{B} is a recombination current: Holes are injected into the n doped transistor regions and recombine. These holes need to be supplied to fulfill continuity from the base terminal. The resulting current is physically independent from the transfer current and thus, should be modeled independently from I_{C}. The very simplified approach of describing a bipolar transistor via $I_{\mathrm{C}} = B_{\mathrm{f}} I_{\mathrm{B}}$ is therefore invalid.

In HICUM, there are several base current components to model the independent recombination regions of I_{B} [74]:

$$I_{\mathrm{B}} = I_{\mathrm{BE}} + I_{\mathrm{RE}} + I_{\mathrm{BC}}. \tag{3.38}$$

I_{BE} and I_{BC} represent the current injected into the neutral emitter and collector, respectively. Additionally, I_{RE} describes the recombination within the BE space charge region, which is relevant for low V_{BE}. Each of the components is modeled by the well-known current equation for pn-junctions:

$$I = I_{\mathrm{S}} \left[\exp\left(\frac{V_{\mathrm{j}}}{m V_{\mathrm{T}}} \right) - 1 \right]. \tag{3.39}$$

V_{T}, I_{S}, m and V_{j} denote the thermal voltage, the saturation current, the nonideality factor and the voltage applied across the junction, respectively. Each

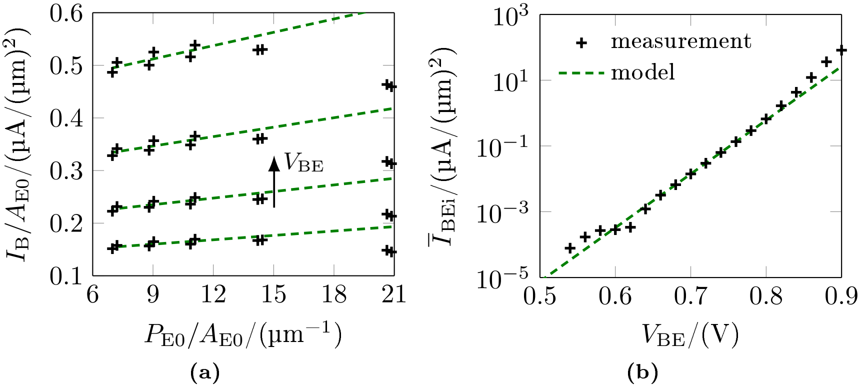


Figure 3.44: Base current extraction of the BE component for the HS transistors of [76]. Comparison of measurements (markers) and model (lines) for **(a)** the perimeter over area separation (devices with $l_{drawn} = (4.5 \text{ and } 9)\,\mu m$ and $b_{drawn} = (180 \text{ to } 378)\,nm$) for different V_{BE} and **(b)** the internal component $\overline{I}_{BEi}$.

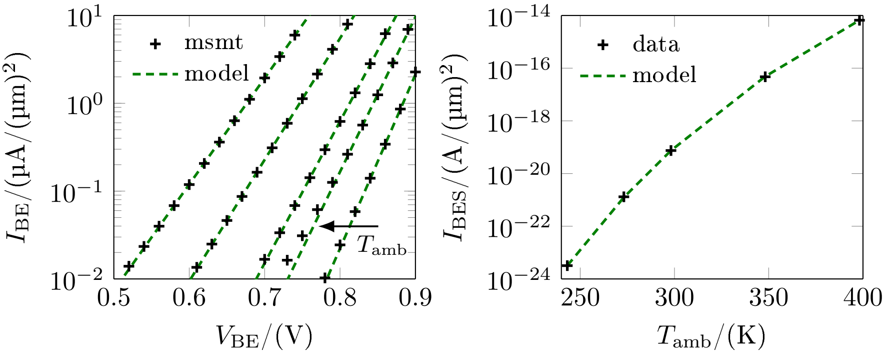
of the I_B components itself consists of an internal and a peripheral/external current component, which leads to twelve parameters dedicated to model I_B (I_S and m for each element).

To proceed with the extraction, a PoA separation is performed for the measured base current and the respective area and perimeter portions are then fitted with (3.39). The extraction results for the BE component of the base current are shown in fig. 3.44. As the measurements are too noisy below $V_{BE} = 0.6\,V$ to observe a recombination component in the PoA results, the extraction of I_{RE} was omitted.

In an additional step, the temperature dependence of I_B is extracted by fitting results for the saturation current measured at different ambient temperatures with the temperature dependent description of I_S:

$$I_S(T) = I_S(T_0)\left(\frac{T}{T_0}\right)^{\zeta_T} \exp\left[\frac{V_g}{V_T}\left(\frac{T}{T_0} - 1\right)\right]. \tag{3.40}$$

The parameters ζ_T and V_g are the temperature coefficient and the band gap of the injection region, respectively. As only a limited amount of temperature dependent measurement data was available, the results shown in fig. 3.45 do



(a) **(b)**

Figure 3.45: Extraction of the base current (BE component) for a single HS transistor of [76] ($l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$ and $b_{\mathrm{drawn}} = 180\,\mathrm{nm}$). Comparison of measurements (markers) and model (lines) for **(a)** I_{BE} vs. V_{BE} at different ambient temperatures and **(b)** I_{BES} vs. T_{amb}.

not correspond to the PoA components, but to the current of a single device (which is sufficient, as the temperature dependence of all devices of the same process is assumed to be identical). Tables 3.11 and 3.12 list the extracted parameter set corresponding to the base current for modeling the electrical and temperature behavior, respectively.

parameter (HS) (unit)	$\overline{I}_{\mathrm{BEiS}}$ (A/µm^2)	m_{BEi} (1)	I'_{BEpS} (A/µm)	m_{BEp} (1)
value	$4.99 \cdot 10^{-20}$	1.033	$3.74 \cdot 10^{-22}$	1.000
parameter (MV) (unit)	$\overline{I}_{\mathrm{BEiS}}$ (A/µm^2)	m_{BEi} (1)	I'_{BEpS} (A/µm)	m_{BEp} (1)
value	$2.94 \cdot 10^{-20}$	1.016	$3.00 \cdot 10^{-21}$	1.066
parameter (HV) (unit)	$\overline{I}_{\mathrm{BEiS}}$ (A/µm^2)	m_{BEi} (1)	I'_{BEpS} (A/µm)	m_{BEp} (1)
value	$2.72 \cdot 10^{-20}$	1.020	$2.50 \cdot 10^{-21}$	1.036
parameter (HS) (unit)	$\overline{I}_{\mathrm{BCiS}}$ (A/µm^2)	m_{BCi} (1)	I'_{BCxS} (A/µm)	m_{BCx} (1)
value	$3.14 \cdot 10^{-25}$	1	$3.01 \cdot 10^{-19}$	1
parameter (MV) (unit)	$\overline{I}_{\mathrm{BCiS}}$ (A/µm^2)	m_{BCi} (1)	I'_{BCxS} (A/µm)	m_{BCx} (1)
value	$2.50 \cdot 10^{-20}$	1	$2.20 \cdot 10^{-19}$	1
parameter (HV) (unit)	$\overline{I}_{\mathrm{BCiS}}$ (A/µm^2)	m_{BCi} (1)	I'_{BCxS} (A/µm)	m_{BCx} (1)
value	$1.26 \cdot 10^{-19}$	1	$2.44 \cdot 10^{-19}$	1

Table 3.11: Extracted electrical parameters for the base current for all three transistor flavors.

parameter (HS) (unit)	V_{gE} (V)	ζ_{BET} (1)	V_{gC} (V)
value	1.063	3.45	0.887
parameter (MV) (unit)	V_{gE} (V)	ζ_{BET} (1)	V_{gC} (V)
value	1.061	4.08	0.892
parameter (HV) (unit)	V_{gE} (V)	ζ_{BET} (1)	V_{gC} (V)
value	1.071	3.59	0.971

Table 3.12: Extracted temperature parameters for the base current for all three transistor flavors.

3.9 Emitter and thermal resistance

Both the emitter and thermal resistance are two critical components that determine transistor behavior at high injection and also have an impact on the transition frequency. The thermal resistance R_{th} of the transistor links the temperature increase ΔT by self-heating (SH) with the dissipated power P by

$$\Delta T = T - T_{\mathrm{amb}} = R_{\mathrm{th}} P, \tag{3.41}$$

with the ambient temperature T_{amb}. As R_{th} is a quantity with a complex 3D geometry dependence closely associated to the transistor structure, it is not practical (and possibly unfeasible) to develop a dedicated test structure for its extraction. Similarly, test structures for the emitter resistance R_{E} – like the one in [106] – cannot be fabricated anymore without significant effort, as they require a dedicated process step (and lithography mask) to form a n^+ doped region as replacement for the base. Older technologies used an additional process step to form such a region for the mono-silicon emitter making the approach feasible without any process changes. Consequently, for modern technologies that rely on the out diffusion of the n^+ doped polysilicon to form the n^+ doped mono-emitter (saving a mask), the approach has not been implemented anymore.

As a result, other determination methods need to be applied that use measured characteristics of single transistors for the determination of R_{E}, like the ones developed in [107–110]. As for all indirect extraction methods, the main goal is to find terminal characteristics in which the desired parameter dominates the behavior and can be extracted. This means, other yet unknown parameters (mainly for the internal transistor behavior) that have an impact on the respective procedure are either assumed or neglected. Since R_{E} is just one of the parameters that impacts the transistor behavior at high injection, these approaches can easily fail.

In this work, the approach of [110] is pursued, which is – from the author's perspective – one of the most consistent and direct approaches (as long as there is enough self-heating involved). For treating the base current (or the internal

BE voltage V_{BEi} in case of a forced I_{B} measurement) as a temperature sensor, the current equation for a pn-junction (see (3.39) and (3.40)) is rewritten and solved numerically for the device temperature T:

$$I_{\mathrm{B}} = I_{\mathrm{BES}}\left(T_0\right)\left(\frac{T}{T_0}\right)^{\zeta_{\mathrm{BET}}} \exp\left[\frac{\mathrm{V}_{\mathrm{gE}}}{\mathrm{V}_{\mathrm{T}}}\left(\frac{\mathrm{T}}{\mathrm{T}_0}-1\right)\right]\left(\exp\left(\frac{V_{\mathrm{BEi}}}{m_{\mathrm{BE}}V_{\mathrm{T}}}\right)-1\right). \tag{3.42}$$

Furthermore, it is assumed that the voltage drop caused by $I_{\mathrm{B}}R_{\mathrm{B}}$ is negligible. This is reasonable (the current gain of process [76] is very large) but also necessary, as the exact value of R_{Bi} at high currents is unknown at this point. This assumption leads to the internal voltages

$$\begin{aligned} V_{\mathrm{BEi}} &\approx V_{\mathrm{BE}} - \left(I_{\mathrm{C}} + I_{\mathrm{B}}\right) R_{\mathrm{E}} \\ V_{\mathrm{CEi}} &= V_{\mathrm{CE}} - \left(I_{\mathrm{C}} + I_{\mathrm{B}}\right) R_{\mathrm{E}} - I_{\mathrm{C}}R_{\mathrm{Cx}}. \end{aligned} \tag{3.43}$$

Neglecting the power dissipated in R_{B}, the pn-junctions and the power corresponding to impact ionization, (3.41) can be evaluated:

$$\Delta T \approx R_{\mathrm{th}}I_{\mathrm{C}}V_{\mathrm{CE}}. \tag{3.44}$$

Assuming then a constant collector current obtained by a forced I_{B} measurement, changing V_{CE} means changing device temperature in a linear way according to the previous equation and implies that the temperature increase must be zero for $V_{\mathrm{CE}} = 0\,\mathrm{V}$, which forms the condition to extract R_{E}: R_{E} is adjusted until ΔT obtained by (3.42) forces $\Delta T = 0\,\mathrm{K}$ at $V_{\mathrm{CE}} = 0\,\mathrm{V}$ for the forced I_{B} measurement. ΔT at $V_{\mathrm{CE}} = 0\,\mathrm{V}$ needs to be extrapolated within a reasonable voltage range because I_{C} cannot be assumed to be constant in the saturation regime (this would violate the assumption made for the extraction). Subsequently, the obtained data for R_{E} are scaled by

$$R_{\mathrm{E}} = R_{\mathrm{E,acc}} + \frac{\rho_{\mathrm{E}}}{A_{\mathrm{E0}}}, \tag{3.45}$$

with the access contribution $R_{\mathrm{E,acc}}$ caused by the on-chip metalization and probes. Since the measured resistances of the “Short” structure are taken into account by correcting the voltages applied to the actual transistor, $R_{\mathrm{E,acc}}$ should be negligible. Remaining error sources for $R_{\mathrm{E,acc}} \neq 0\,\Omega$ are an imperfect “Short” and the uncertainty of the extraction procedure.

Although the obtained value for R_{E} is physical and in line with the HICUM setting flsh = 2, the result is yet inconsistent with the typical model usage: For the HICUM setting flsh = 1 only the main contributions to the dissipated power are considered in the model for faster convergence of the positive self-heating feedback of BJTs. This means that (3.44) is rewritten to

$$\Delta T \approx R_{\mathrm{th}} I_{\mathrm{C}} V_{\mathrm{CEi}}, \tag{3.46}$$

now including the internal voltage V_{CEi} instead of V_{CE}. Subsequently, (3.43) is inserted into (3.46), which then finally leads to (3.47) and the description of the extraction method for flsh = 1.

$$\Delta T \approx R_{\mathrm{th}} I_{\mathrm{C}} \left(V_{\mathrm{CE}} - \underbrace{\left[\left(I_{\mathrm{C}} + I_{\mathrm{B}} \right) R_{\mathrm{E}} + I_{\mathrm{C}} R_{\mathrm{Cx}} \right]}_{V_{\mathrm{CE0}}} \right) \tag{3.47}$$

For $V_{\mathrm{CE}} = 0\,\mathrm{V}$, there is still a voltage drop over the series resistances (V_{CE0}) – assuming a constant collector current. However, this drop does not contribute to the temperature increase caused by self-heating for the setting flsh = 1. Consequently, the temperature increase must be zero for $V_{\mathrm{CE}} = V_{\mathrm{CE0}}$ – forming the updated condition to extract R_{E}. To force this condition, the data are extrapolated at a reasonable voltage range outside of saturation leading to the results shown in fig. 3.46 for the HS transistors of [76]. Fig. 3.47 illustrates the result for the MV and HV transistor versions.

As can be observed in the figures, the emitter resistance scales fairly well with emitter area. Nevertheless, due to the limited measurement data, the temperature parameters for I_{B} had to be extracted for the smallest device width (see section 3.8) and were assumed to be identical for other device geometries. This causes a certain extraction inaccuracy for R_{E}, which could be avoided by measuring relevant device geometries vs. temperature and applying a separate parameter combination for each geometry. Additionally, the available measurement resolution was only 1 mV for V_{BE}, which leads to

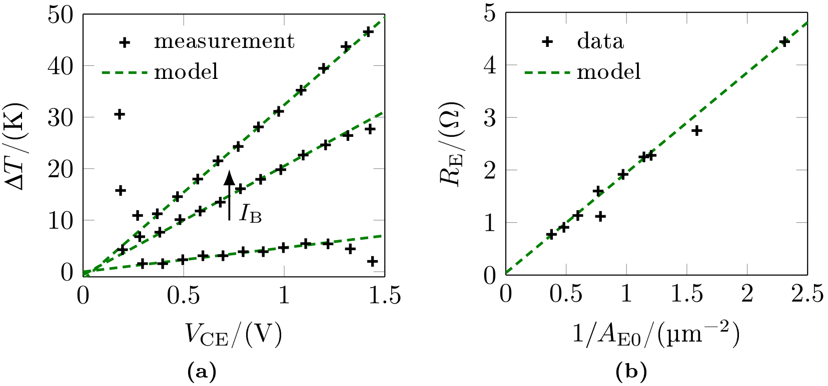


Figure 3.46: Emitter resistance extraction for the HS transistors of [76]. Comparison of measurements (markers) and model (lines) of **(a)** ΔT vs. V_{CE} for a device with a size of $A_{drawn} = 0.315\,\mu m \times 4.5\,\mu m$ at different forced I_B and **(b)** R_E vs. $1/A_{E0}$ for devices with $l_{drawn} = (4.5 \text{ and } 9)\,\mu m$ and $b_{drawn} = (180 \text{ to } 378)\,nm$.

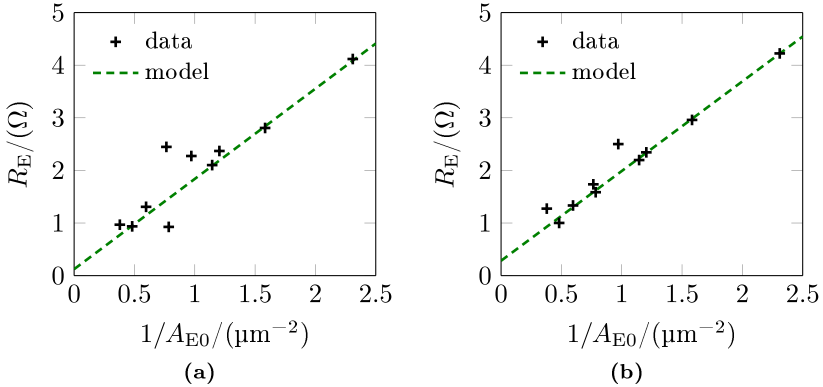


Figure 3.47: Emitter resistance extraction: Comparison of extracted data (markers) and model (lines) of R_E vs. $1/A_{E0}$ for devices with $l_{drawn} = (4.5 \text{ and } 9)\,\mu m$ and $b_{drawn} = (180 \text{ to } 378)\,nm$ for **(a)** the MV and **(b)** HV transistor versions of [76].

a behavior similar to several consecutive step-functions for ΔT and makes the method unreliable at low I_{B}.

After R_{E} has been extracted, R_{th} is obtained by rearranging (3.47):

$$R_{\mathrm{th}} = \frac{\Delta T}{I_{\mathrm{C}}\left(V_{\mathrm{CE}} - V_{\mathrm{CE0}}\right)}. \tag{3.48}$$

The scaling for R_{th} is based on a pyramidal heat flow – in analogy to the scaling of the internal collector resistance [74]:

$$R_{\mathrm{th}} = \rho_{\mathrm{th}} \underbrace{\frac{\ln\left(4l_{\mathrm{E}}/b_{\mathrm{E}}\right)}{l_{\mathrm{E}}}}_{f_{\mathrm{th}}}. \tag{3.49}$$

Normalizing R_{th} to f_{th} allows to extract the geometry independent value ρ_{th} by taking the mean for all considered transistor geometries. Respective results for all three transistor flavors are shown in fig. 3.48.

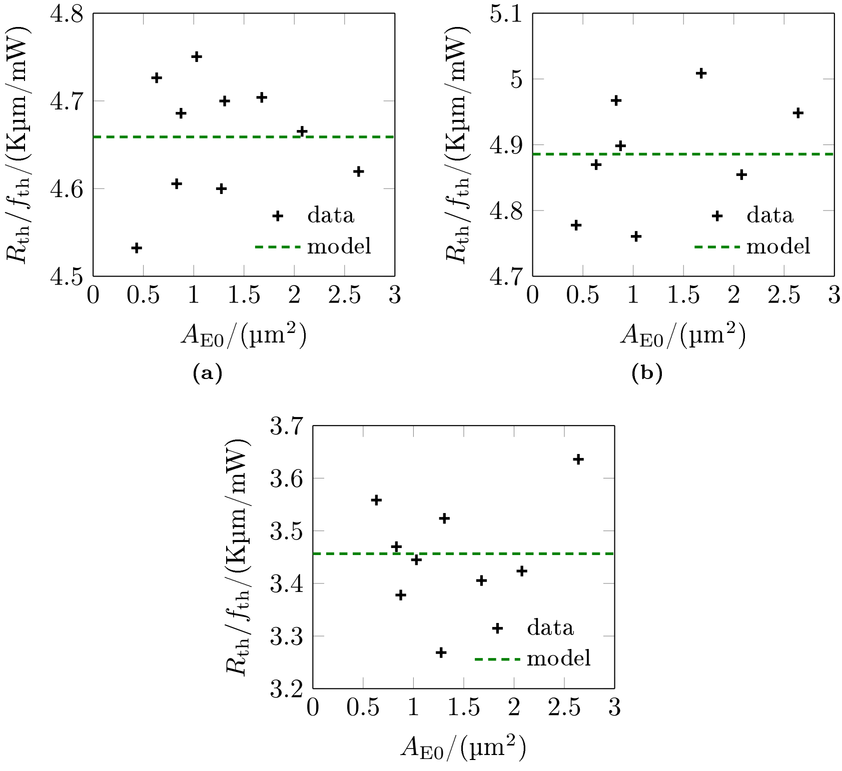
To evaluate the impact of self-heating on R_{E}, R_{th} and the extraction approach, the method is extended by including the temperature dependence of R_{Cx}, R_{E} and R_{th} via (3.17): The corresponding expressions – including the temperature coefficients ζ_{E}, ζ_{th} and ζ_{Cx} – are inserted in (3.43) and (3.47) leading to

$$\begin{aligned} V_{\mathrm{BEi}}(T) &\approx V_{\mathrm{BE}} - \left(I_{\mathrm{C}} + I_{\mathrm{B}}\right) R_{\mathrm{E}}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{\mathrm{E}}} \\ V_{\mathrm{CEi}}(T) &= V_{\mathrm{CE}} - \left(I_{\mathrm{C}} + I_{\mathrm{B}}\right) R_{\mathrm{E}}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{\mathrm{E}}} - I_{\mathrm{C}} R_{\mathrm{Cx}}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{\mathrm{Cx}}} \end{aligned} \tag{3.50}$$

and

$$\Delta T \approx R_{\mathrm{th}}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{\mathrm{th}}} I_{\mathrm{C}} V_{\mathrm{CEi}}(T). \tag{3.51}$$

The former linear relationship between the temperature increase and V_{CEi} is distorted by the temperature dependent coefficient $(T/T_0)^{\zeta_{\mathrm{th}}}$. However, the temperature independent prefactor can be restored by a proper normalization of (3.51):



(a) **(b)**

(c)

Figure 3.48: Results of the thermal resistance extraction using the method of [110] for devices with $l_{\mathrm{drawn}} = (4.5 \text{ and } 9)\,\mathrm{\mu m}$ and $b_{\mathrm{drawn}} = (180 \text{ to } 378)\,\mathrm{nm}$ (process of [76]). Comparison of extracted data (markers) and model (lines) for ρ_{th} vs. A_{E0} for the HS **(a)**, the MV **(b)** and the HV transistor versions **(c)**.

$$\Delta T \Big/ \left(\frac{T}{T_0}\right)^{\zeta_{\mathrm{th}}} \approx R_{\mathrm{th}}\left(T_0\right) I_{\mathrm{C}} V_{\mathrm{CEi}}\left(T\right). \tag{3.52}$$

Subsequently, the extraction approach can be applied to the data assuming initial starting values for ζ_{E} and ζ_{th}. By repeating the method for different ambient temperatures, the temperature coefficients can be determined and are then fed back for consistency: The method is repeated until a consistent

parameter (HS) (unit)	ρ_{E} ($\Omega\,\mu\mathrm{m}^2$)	ρ_{th} (Kμm/W)	ζ_{rE} (1)	ζ_{th} (1)
value	1.84	4269	-0.12	0.79
parameter (MV) (unit)	ρ_{E} ($\Omega\,\mu\mathrm{m}^2$)	ρ_{th} (Kμm/W)	ζ_{rE} (1)	ζ_{th} (1)
value	1.53	4190	0.13	0.65
parameter (HV) (unit)	ρ_{E} ($\Omega\,\mu\mathrm{m}^2$)	ρ_{th} (Kμm/W)	ζ_{rE} (1)	ζ_{th} (1)
value	1.56	3322	0^*	0.96

*Method failed for ζ_{rE} of the HV transistors.

Table 3.13: Parameter set for the emitter and thermal resistance for all three transistor flavors.

solution for the parameters has been found for the measurements of a single device at different ambient temperatures. While the initial method already requires a nested loop (optimizing for R_{E} while fitting a straight line to ΔT vs. V_{CEi}), the extension leads to an additional interleaving.

As can be observed in fig. 3.49, the temperature dependence of R_{E} is negligible and is lost within the extraction accuracy. Conversely, R_{th} follows a clear trend – close to a linear behavior. Naturally, the extension of the extraction method for the temperature dependence of the resistances can also be applied to geometry scaling – reducing R_{E} and R_{th} at reference temperature by about 5 % and 10 %, respectively. Table 3.13 summarizes the technology parameters (including the effect of SH on the resistances) for all three transistor flavors. It is assumed that the emitter resistance of the three flavors must be identical and hence, the mean value is used for the model ($\rho_{\mathrm{E}} = 1.64\,\Omega\,\mu\mathrm{m}^2$ and $\zeta_{\mathrm{rE}} = 0$).

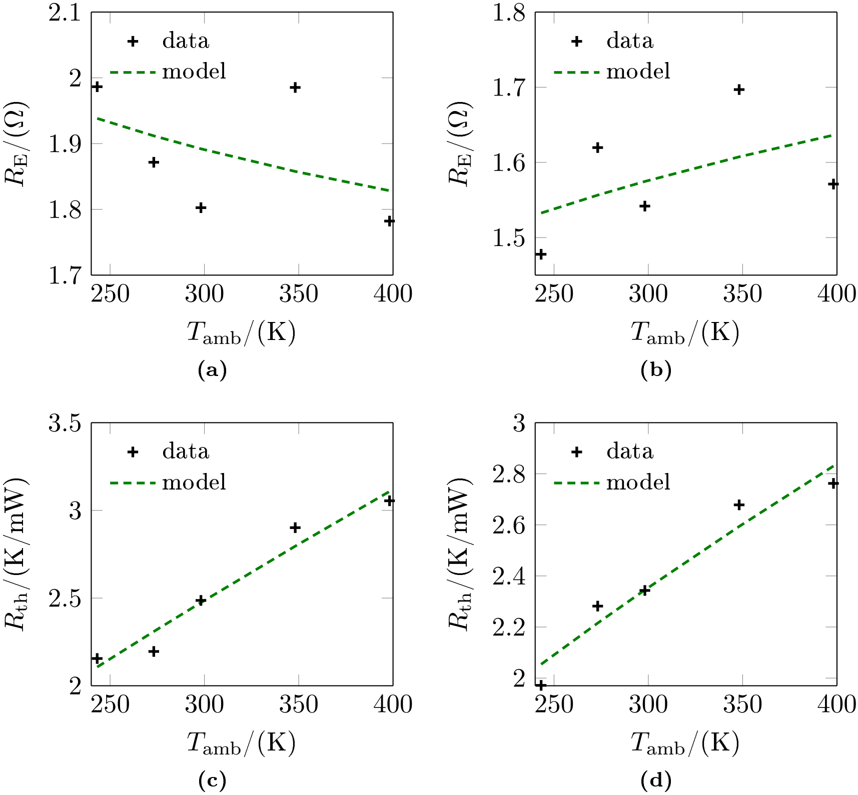


Figure 3.49: Extraction results for the temperature behavior of the emitter and thermal resistance for single transistors of [76] ($l_{drawn} = 9\,\mu m$ and $b_{drawn} = 180\,nm$). Comparison of extraction data (markers) and model (lines) of R_E vs. T_{amb} for **(a)** the HS and **(b)** the MV transistor versions. **(c)** and **(d)** illustrate R_{th} vs. T_{amb} for the HS and MV versions, respectively.

3.10 Transit time extraction

The extraction of most of the parameters of the external transistor elements is mandatory before starting the transit time extraction. Both the external capacitances and resistances can have a severe impact on the small signal behavior and need to be taken into account for the next extraction steps. All of the required parameters were determined previously, except for $f_{\mathrm{BE,par}}$ and $f_{\mathrm{BC,par}}$, which describe the partitioning of the parasitic BE and BC capacitances across the external base resistance. In section 3.5, it has been observed that the largest portion of R_{Bx} is associated to the interface of the poly- to mono-silicon base and the resistance of the spacer. Together with the extended emitter doping diffusion and the undoped region underneath the spacer (causing a greatly reduced capacitance underneath the spacer), this leads to the assumption that most of $C_{\mathrm{BE,par}}$ needs to be attached to the external base terminal and thus $f_{\mathrm{BE,par}} \approx 0.2$ based on the analysis of section 3.2. With this information, the partitioning for the BC capacitance is done according to

$$f_{\mathrm{BC,par}} = \frac{C_{\mathrm{jCx0}}}{C_{\mathrm{jCx0}} + C_{\mathrm{BC,par}}}, \tag{3.53}$$

which assumes that the bias independent portion $C_{\mathrm{BC,par}}$ is attached between the external base and collector terminals.

To proceed with the extraction of the transit time τ_{f}, the deembedding procedure described in [93] is applied. As a result, the fitting quantity τ_{fit} and the internal transconductance g_{m} are obtained, which will be used to conduct the extraction. The master equation consists of τ_{f}, C_{jEi} and the minor derivative for the low current transit time τ_{f0} with respect to the internal base collector voltage:

$$\tau_{\mathrm{fit}} = \tau_{\mathrm{f}} + \left(C_{\mathrm{jEi}} + I_{\mathrm{C}} \frac{\partial \tau_{\mathrm{f0}}}{\partial V_{\mathrm{BCi}}} \right) / g_{\mathrm{m}}. \tag{3.54}$$

τ_{f} in turn is composed of the high current transit time $\Delta\tau_{\mathrm{f}}$ and τ_{f0}. During the first extraction step the voltage dependence of the internal base emitter capacitance (described by the parameters V_{DEi} and z_{Ei}) are revised and a_{jEi}

– the ratio of the maximum to the zero-bias value of C_{jEi} – is extracted. To do so, the derivative of (3.54) w.r.t. $1/g_{\mathrm{m}}$ is calculated and simplified for low to medium current densities:

$$\frac{\partial \tau_{\mathrm{fit}}}{\partial\left(1/g_{\mathrm{m}}\right)} \approx C_{\mathrm{jEi}}. \tag{3.55}$$

Measurement data are typically too noisy to apply (3.55) for parameter extraction, but it can be used reliably to detect the relevant bias range without prior knowledge of the parameters for the transit time. Data up to the maximum value of C_{jEi} are included in the extraction process. As an alternative, (3.54) is rearranged to obtain

$$C_{\mathrm{jEi}} = \left(\tau_{\mathrm{fit}} - \tau_{\mathrm{f}}\right) g_{\mathrm{m}} - I_{\mathrm{C}} \frac{\partial \tau_{\mathrm{f0}}}{\partial V_{\mathrm{BCi}}} \tag{3.56}$$

and initially, τ_{f} is set to zero until it can be replaced by the HICUM model description during the next extraction steps. For the particular process analyzed in this thesis, the scaling for C_{jE} is unclear because there is a large measurement error caused by the deembedding of the “Open” (see section 3.3). To reassess the scaling, C_{jEp0} is set to zero during the deembedding process of [93] and hence, the total value of C_{jE} is obtained for C_{jEi} by the procedure. Consequently, parameters for the total junction capacitance can be extracted instead of C_{jEi}. After running the internal transistor extraction for all relevant geometries (the exact methodology to extract τ_{f} – which is required to obtain C_{jE} – is shown later in this section), the model description for C_{jE} can be scaled by performing a PoA separation on the MV transistor data – for which the scaling was working best. Contrary to section 3.3, all transistor widths were included in the separation process and thus, the extracted parameters are somewhat different – even at low bias. A change in C_{jEi} also requires updating Q_{p0} and therefore, the evaluations of section 3.7 are repeated. All results are summarized in fig. 3.50 with the corresponding parameter listing in table 3.14.

With the updated parameters, the actual transit time parameter extraction can be performed. As a first step, the internal device temperature is determined by solving

$$T = I_{\mathrm{C}} V_{\mathrm{CEi}}\left(T\right) R_{\mathrm{th}}\left(T\right) + T_{\mathrm{amb}} \tag{3.57}$$

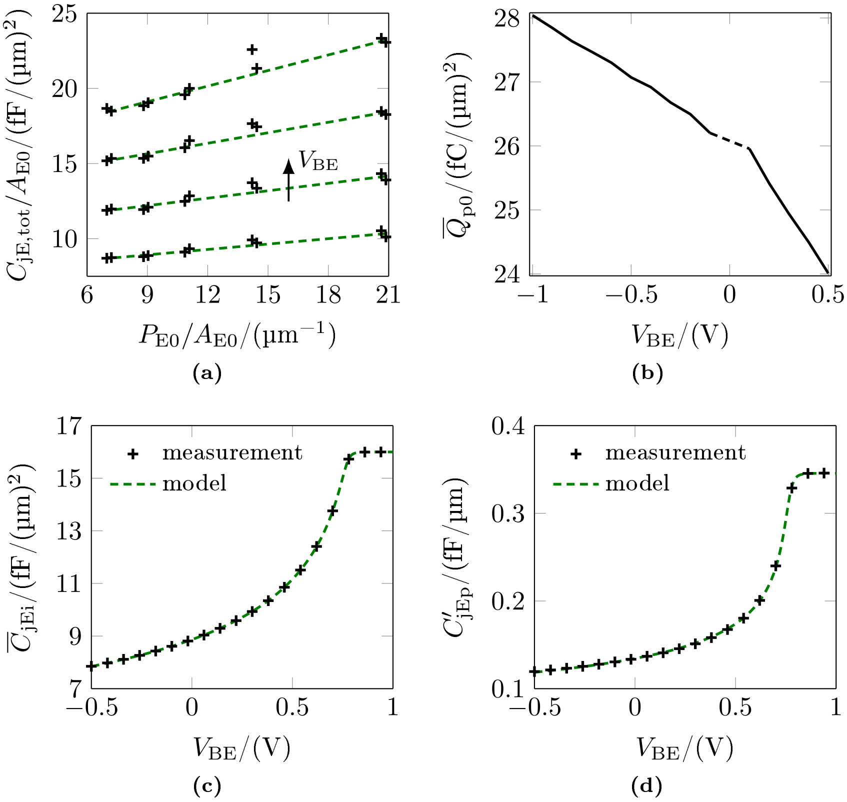


Figure 3.50: Extraction update for the base emitter junction capacitances and the zero-bias hole charge (MV transistors, process of [76]). Comparison of extraction data (markers) and fit (lines) for **(a)** the PoA separation, **(c)** the internal BE capacitance $\overline{C}_{\mathrm{jEi}}$ and **(d)** the peripheral BE capacitance C'_{jEp}. The update for $\overline{Q}_{\mathrm{p0}}$ is illustrated in **(b)**.

and

$$V_{\mathrm{CEi}}\,(T) = V_{\mathrm{CE}} - (I_{\mathrm{C}} + I_{\mathrm{B}})\,R_{\mathrm{E}}\,(T) - I_{\mathrm{C}}R_{\mathrm{Cx}}\,(T) \tag{3.58}$$

for the S-parameter measurements in forward bias – including the temperature dependence of the series resistances. Generally, it is important to include self-heating for the transit time extraction, as it already plays an important role for τ_{f0} for larger V_{CE}. Subsequently, (3.54) is rearranged for τ_{f0}:

parameter (unit)	$\overline{C}_{\mathrm{jEi0}}$ (fF/µm^2)	z_{Ei} (1)	V_{dEi} (V)	a_{jEi} (1)
value	8.86	0.269	0.872	1.80
parameter (unit)	C'_{jEp0} (fF/µm^2)	z_{Ep} (1)	V_{dEp} (V)	a_{jEp} (1)
value	0.134	0.253	0.787	2.57
parameter (unit)	$\overline{Q}_{\mathrm{p0}}$ (HS) (fC/µm^2)	$\overline{Q}_{\mathrm{p0}}$ (MV) (fC/µm^2)	$\overline{Q}_{\mathrm{p0}}$ (HV) (fC/µm^2)	
value	24.7	26.1	28.8	

Table 3.14: Updated parameter set for the base emitter junction capacitance and the zero-bias hole charge.

$$\tau_{\mathrm{f0}} = \tau_{\mathrm{fit}} - \left(C_{\mathrm{jEi}} + I_{\mathrm{C}} \frac{\partial \tau_{\mathrm{f0}}}{\partial V_{\mathrm{BCi}}} \right) / g_{\mathrm{m}} - \Delta\tau_{\mathrm{f}}. \tag{3.59}$$

Initially, $\Delta\tau_{\mathrm{f}}$ is unknown and hence, set to zero. During the course of the extraction, $\Delta\tau_{\mathrm{f}}$ will be determined and can be fed back to (3.59) for consistency. To proceed with the extraction of τ_{f0}, appropriate data need to be selected in a region where the low current transit time dominates τ_{fit}. It has been confirmed both by device simulations and measurement data that the appropriate region is just before the minimum of τ_{fit} ($\sim$ (10 to 30) mV before $V_{\mathrm{BE}}\left(\tau_{\mathrm{fit,min}}\right)$) and therefore $V_{\mathrm{BE}}\left(\tau_{\mathrm{fit,min}}\right)$ is an important reference (see fig. 3.51).

Using the selected data, τ_{f0} can be fitted with the description of HICUM, which relies on the normalized internal BC junction capacitance c [74]. Using c instead of V_{BCi} additional effort is avoided to treat numerical overflows, as $c > 0$. Fig. 3.52 illustrates the extraction result with and without self-heating for an exemplary transistor. Corresponding parameter values are listed in appendix A.4.

The initial result for τ_{f0} is used to conduct the extraction for $\Delta\tau_{\mathrm{f}}$: To apply the standard method [111], (3.54) is rearranged for $\Delta\tau_{\mathrm{f}}$:

$$\Delta\tau_{\mathrm{f}} = \tau_{\mathrm{fit}} - \left(C_{\mathrm{jEi}} + I_{\mathrm{C}} \frac{\partial \tau_{\mathrm{f0}}}{\partial V_{\mathrm{BCi}}} \right) / g_{\mathrm{m}} - \tau_{\mathrm{f0}}. \tag{3.60}$$

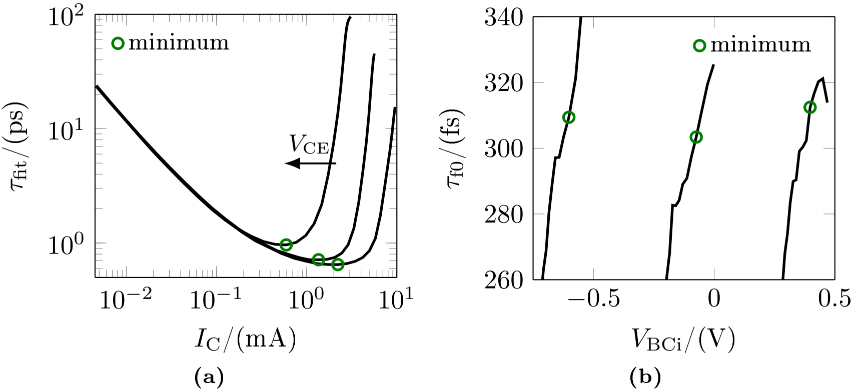


Figure 3.51: Exemplary data obtained from measurements (HS transistor, process of [76]) for **(a)** the fitting quantity τ_{fit} vs. I_{C} and **(b)** the low current transit time τ_{f0} vs. V_{BCi} for different V_{CE}. The minimum of τ_{fit} is indicated by markers in both plots for each V_{CE}. As can be observed in **(b)**, the appropriate selection range to extract τ_{f0} is just before the minimum of τ_{fit}, where bumps indicate a small constant region.

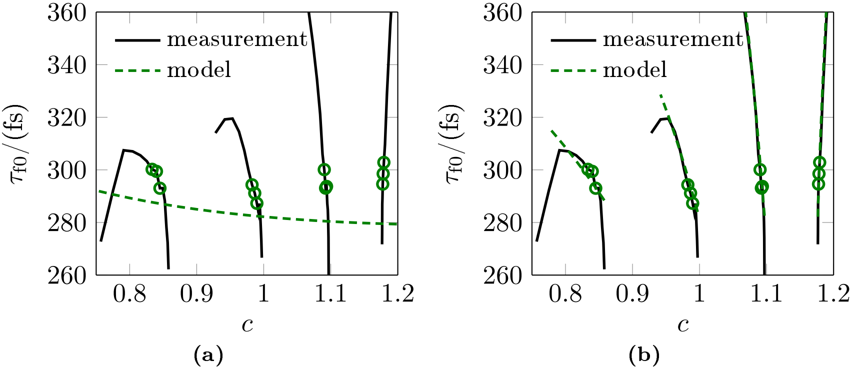
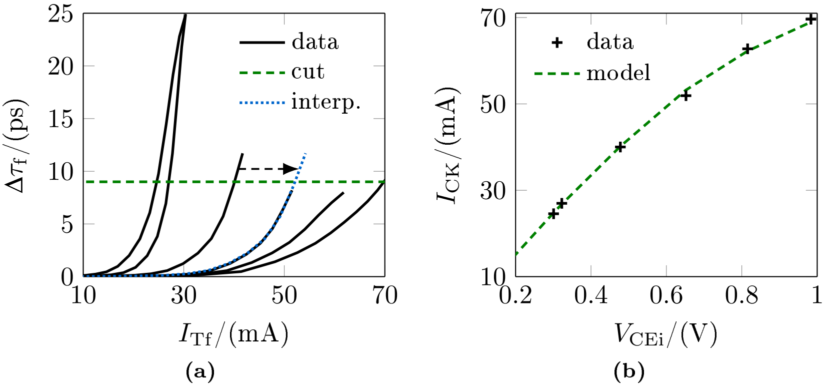


Figure 3.52: Extraction result for the low current transit time τ_{f0} of an exemplary transistor (HS transistor, process of [76]). Comparison of measurements and model of τ_{f0} vs. c without self-heating **(a)** and with self-heating **(b)** for four different V_{BC}. The data used to conduct the extraction were selected in the range of $\sim$ (10 to 30) mV before V_{BE} ($\tau_{\mathrm{fit,min}}$) and are indicated by markers. As can be observed, self-heating is a dominant factor for τ_{f0} and must be taken into account for reliable results.



(a) **(b)**

Figure 3.53: Illustration of the classical extraction method for the critical current I_{CK} based on measurement data (HS transistor, process of [76]). **(a)** Intercepts of $\Delta\tau_{\mathrm{f}}$ vs. I_{Tf} with the reference level $\Delta\tau_{\mathrm{f,ref}}$ are calculated for different bias conditions (constant V_{BC} and V_{CE}). If there is no intersection, an extrapolation is performed to determine $I_{\mathrm{CK,i}}$. **(b)** Fit of the HICUM description for I_{CK} with the obtained data.

The classical method determines the critical current I_{CK} based on calculating intercepts of $\Delta\tau_{\mathrm{f}}$ (I_{Tf}) with an arbitrary reference level $\Delta\tau_{\mathrm{f,ref}}$ (in forward operation and negligible breakdown, the forward transfer current I_{Tf} is assumed to be identical with I_{C}). Consequently, the data sets $I_{\mathrm{CK,i}}$, $V_{\mathrm{CEi,i}}$ and T_{i} at the intercept are obtained for different bias conditions (e.g. for measurements at different V_{BC}, V_{CE} and ambient temperatures) and are then used to extract the parameters for I_{CK}. The method is somewhat inaccurate because the condition to merge all different sweeps is only valid if self-heating for all bias sweeps is identical and in the end, the actual merging goal cannot be accomplished by a single reference level. Therefore, the classical method is only applied to determine starting values for the parameters of the critical current.

Applying the method to exemplary measurement data leads to the result shown in fig. 3.53. One of the problems here is that there might not be an intercept for certain V_{BC} if the maximum value of $\Delta\tau_{\mathrm{f}}$ is lower than the reference level. As a workaround, the missing values for $I_{\mathrm{CK,i}}$ can be extrapolated based on different V_{BC} or V_{CE} bias, as indicated in the figure. The biggest problem, however, is to select an appropriate reference level for the cut: The exact value is undefined (as there is no definition to select I_{CK}), but theoretically – as the HICUM description aims on merging $\Delta\tau_{\mathrm{f}}\left(I_{\mathrm{Tf}}\right)$ for different $V_{\mathrm{BC}}/V_{\mathrm{CE}}$ sweeps – all values should deliver a valid parameter set for I_{CK} (except for the internal collector resistance r_{Ci0}). In practice, the point of inflection of $\Delta\tau_{\mathrm{f}}\left(I_{\mathrm{Tf}}\right)$ at a single $V_{\mathrm{BC}}/V_{\mathrm{CE}}$ is used to determine $\Delta\tau_{\mathrm{f,ref}}$. Assuming a wrong reference level has been selected, the values obtained for $I_{\mathrm{CK,i}}$ will be altered by a constant factor (f_{Ick}), hence the extracted values will be $I_{\mathrm{CK,ex,i}} = f_{\mathrm{Ick}} I_{\mathrm{CK,i}}$. Consequently, the extracted value for the internal collector resistance will be $r_{\mathrm{Ci0,ex}} = r_{\mathrm{Ci0}}/f_{\mathrm{Ick}}$, whereas the other parameters are not affected (assuming identical self-heating for all bias sweeps). Therefore, it is not feasible to obtain an accurate value for r_{Ci0} with the classical method.

Based on the previous observations, the classical method was enhanced in [93,112]: Instead of a single reference level, the whole range of $\Delta\tau_{\mathrm{f}}\left(I_{\mathrm{Tf}}\right)$ is used for the merging process. As a result, the parameter balance is improved, but the issue for r_{Ci0} still remains. The improved method is applied subsequently, but does not lead to a significant gain in accuracy (depending on the reference level) – which is why this intermediate step is not shown here.

Before conducting the extraction of the transit time parameters at high injection, a similarity between the emitter transit time $\Delta\tau_{\mathrm{Ef}}$ and the Kirk-related transit time $\Delta\tau_{\mathrm{fh}}$ shall be pointed out for low-medium current densities. To do so, the exponential factor g_{tfe} of $\Delta\tau_{\mathrm{Ef}}$ needs to be isolated:

$$\begin{aligned} \Delta\tau_{\mathrm{Ef}} &= \tau_{\mathrm{Ef0}}\left(I_{\mathrm{Tf}}/I_{\mathrm{CK}}\right)^{g_{\mathrm{tfe}}} \\ \ln\left(\Delta\tau_{\mathrm{Ef}}/\tau_{\mathrm{Ef0}}\right) &= g_{\mathrm{tfe}}\ln\left(\underbrace{I_{\mathrm{Tf}}/I_{\mathrm{CK}}}_{f_{\mathrm{norm}}}\right). \end{aligned} \tag{3.61}$$

(3.61) describes g_{tfe} as the slope of the characteristics in a log-log plot. To directly force a linear relationship with f_{norm}, the variable $f_{\mathrm{norm,log}} = \ln\left(f_{\mathrm{norm}}\right)$ can be introduced, which then leads to

$$\ln\left(\Delta\tau_{\mathrm{Ef}}/\tau_{\mathrm{Ef0}}\right) = g_{\mathrm{tfe}}\ln\left(f_{\mathrm{norm}}\right) = g_{\mathrm{tfe}} f_{\mathrm{norm,log}}. \tag{3.62}$$

Calculating the derivative of the right hand side of (3.62) with respect to $f_{\mathrm{norm,log}}$ directly leads to g_{tfe}. Next, the same idea is applied to the description of $\Delta\tau_{\mathrm{fh}}$:

$$\Delta\tau_{\mathrm{fh}} = \tau_{\mathrm{hcs}} w_{\mathrm{in}}^2 \left[1 + \frac{2}{f_{\mathrm{norm}}\sqrt{i_{\mathrm{f}}^2 + a_{\mathrm{hc}}}}\right], \tag{3.63}$$

with the parameters τ_{hcs} and a_{hc}. The normalized injection width $w_{\mathrm{in,n}}$ and the additional variable i_{f} read

$$\begin{aligned} w_{\mathrm{in}} &= \frac{i_{\mathrm{f}} + \sqrt{i_{\mathrm{f}}^2 + a_{\mathrm{hc}}}}{1 + \sqrt{1 + a_{\mathrm{hc}}}} \\ i_{\mathrm{f}} &= 1 - 1/f_{\mathrm{norm}}. \end{aligned} \tag{3.64}$$

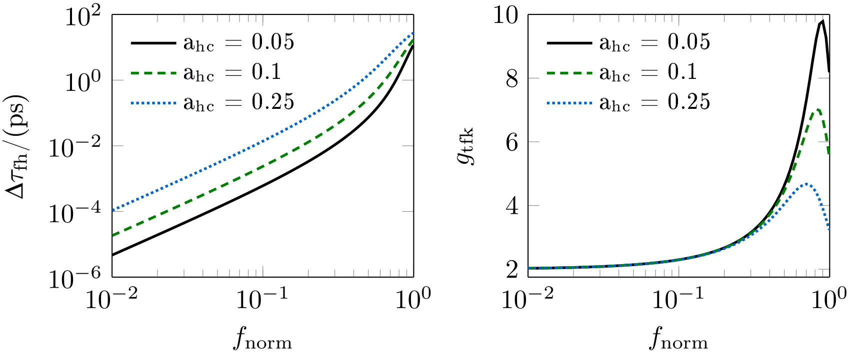
Consequently, the logarithm on both sides of (3.63) is taken and $f_{\mathrm{norm}} = \exp\left(f_{\mathrm{norm,log}}\right)$ is inserted into the equations. After that, the derivative with respect to $f_{\mathrm{norm,log}}$ is determined leading to the exponent of $\Delta\tau_{\mathrm{fh}}$:

$$g_{\mathrm{tfk}} = \frac{\partial \ln\left(\Delta\tau_{\mathrm{fh}}/\tau_{\mathrm{hcs}}\right)}{\partial f_{\mathrm{norm,log}}}. \tag{3.65}$$

The analytical result is too lengthy and not useful, but the limit $f_{\mathrm{norm,log}} \rightarrow -\infty$ ($f_{\mathrm{norm}} \rightarrow 0$) evaluates to

$$\lim_{f_{\mathrm{norm,log}} \rightarrow -\infty} g_{\mathrm{tfk}} = 2, \tag{3.66}$$

which does not depend on a_{hc} and means that $\Delta\tau_{\mathrm{fh}}$ behaves quadratically for small f_{norm}. The result can be troubling for the extraction process, considering that there are transistor technologies that have an emitter transit time exponent g_{tfe} close to 2. In that case, the extraction routine might not be able to distinguish between $\Delta\tau_{\mathrm{Ef}}$ and $\Delta\tau_{\mathrm{fh}}$. (3.63) and (3.66) are illustrated in fig. 3.54 for various parameter combinations of a_{hc}. In the relevant extraction range for $\Delta\tau_{\mathrm{Ef}}$ ($0.1 < f_{\mathrm{norm}} < 0.5$), $2.5 < g_{\mathrm{tfk}} < 4.5$, which still interferes with $\Delta\tau_{\mathrm{Ef}}$. As can be observed, the absolute value of $\Delta\tau_{\mathrm{fh}}$ at low currents decreases with decreasing a_{hc}. Consequently, the extraction of $\Delta\tau_{\mathrm{Ef}}$ should still be possible for low a_{hc}, even if g_{tfe} of the technology is close to g_{tfk} in the relevant extraction range. Note that the maximum of g_{tfk} – which represents the point of inflection – is before $f_{\mathrm{norm}} = 1$ and hence, before the critical current I_{CK}.



(a) **(b)**

Figure 3.54: Illustration of the behavior of the Kirk-related transit time $\Delta\tau_{\mathrm{fh}}$ for $\tau_{\mathrm{hcs}} = 100\,\mathrm{ps}$ and different values of a_{hc}. **(a)** $\Delta\tau_{\mathrm{fh}}$ vs. f_{norm} and **(b)** g_{tfk} vs. f_{norm}.

As has been pointed out before, $\Delta\tau_{\mathrm{Ef}}$ and $\Delta\tau_{\mathrm{fh}}$ are coupled and cannot be extracted separately from each other. Finally, the extraction of the parameters for $\Delta\tau_{\mathrm{f}}$ is conducted by optimization: The remaining parameters a_{hc}, τ_{hcs}, g_{tfe} and τ_{Ef0} are adjusted for the best fit with the reference data within $0.1 < f_{\mathrm{norm}} < 1.5$. Also, the value for r_{Ci0} needs to be included in this process, as it could not be determined accurately in the previous extraction steps. It is beneficial to take the logarithm for both the measured $\Delta\tau_{\mathrm{f}}$ and the model description before performing the fit. An exemplary result for this step is shown in fig. 3.55.

The previously described steps (extraction of τ_{f0}, I_{CK} and $\Delta\tau_{\mathrm{f}}$) describe the general idea of extracting the transit time for a single transistor geometry. The concrete sequence for the extraction flow is as follows:

(i) First, the temperature coefficients for the the transit time and the critical current need to be determined. Usually, only for selected devices measurements at different ambient temperatures exist (possibly from a different wafer) and hence, the method can only be applied as a single transistor approach. The transit time extraction is applied to these data and the obtained temperature coefficients are assumed to be identical for different geometries

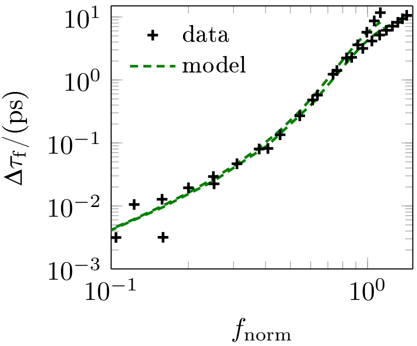


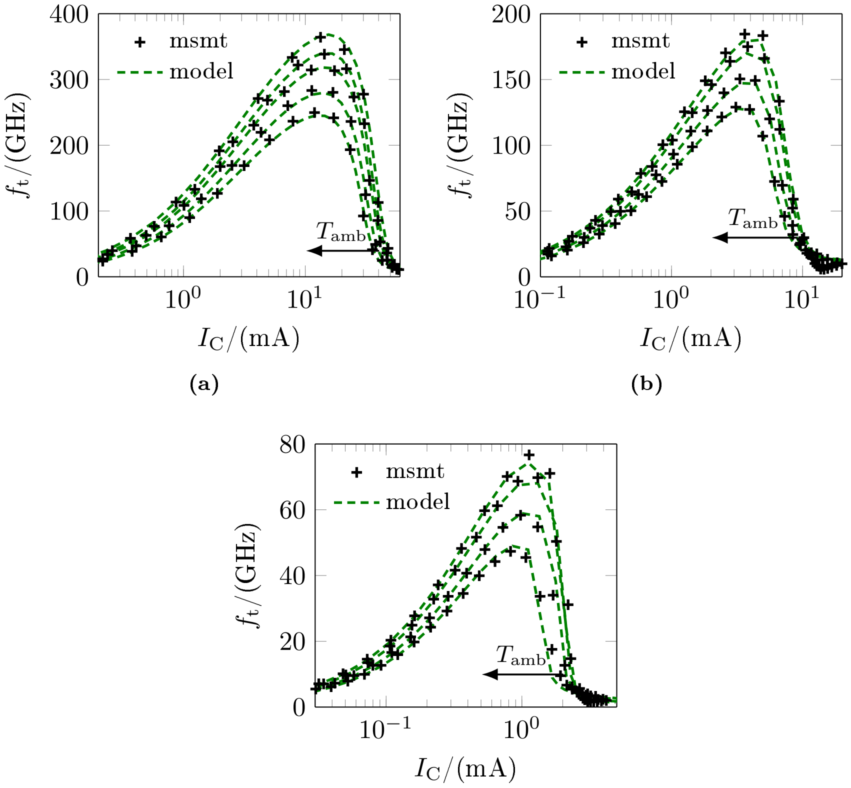
Figure 3.55: Extraction result for the high current transit time $\Delta\tau_f$ of an exemplary transistor (HS transistor, process of [76]). Comparison of measurements and model of $\Delta\tau_f$ vs. f_{norm} for two different V_{BC}. The split-up of the model for the two different sweeps is caused by self-heating.

(similar to the assumption in section 3.8).

(ii) The transit time extraction is performed for different geometries at room temperature using the previously determined temperature coefficients for taking self-heating into account. The obtained parameters are specific for each transistor. Extraction uncertainties are canceled out by taking the mean value for each of the geometry independent parameters.

(iii) The geometry dependent and independent parameters correlate with each other. Consequently, the transit time extraction needs to be repeated, but now fixing the geometry independent parameters during the extraction. As a result, the geometry dependent parameters τ_0 and r_{Ci0} can be scaled with a lower extraction error.

These three steps are very time-consuming and show how difficult a reliable transit time extraction for HBTs is. The author would like to point out that no manual adjustments were performed to the extracted parameters. All presented plots are as-is from the extraction output. The amount of data is too large to be presented in this section and therefore, only important results are shown on the following pages: Figures 3.56 and 3.57 show the agreement

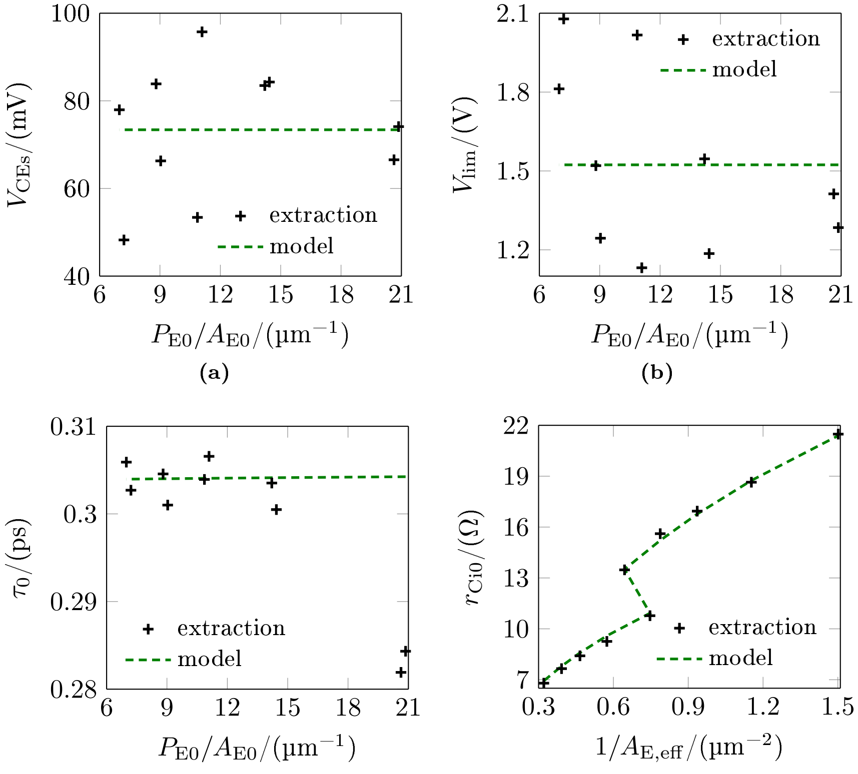


(a) **(b)**

(c)

Figure 3.56: Comparison of measurements and model for the transit frequency f_t vs. I_C at different ambient temperatures for devices with $l_\mathrm{drawn} = 9\,\mu\mathrm{m}$ and $b_\mathrm{drawn} = 180\,\mathrm{nm}$ at $V_\mathrm{BC} = 0\,\mathrm{V}$ (process of [76]). Results for **(a)** the HS ($T_\mathrm{amb} = (-30, 0, 25, 75$ and $125)\,°\mathrm{C}$), **(b)** the MV ($T_\mathrm{amb} = (0, 25, 75$ and $125)\,°\mathrm{C}$) and **(c)** the HV ($T_\mathrm{amb} = (0, 25, 75$ and $125)\,°\mathrm{C}$) transistor versions.

for the model with the measurement data at different temperatures and the behavior of some selected parameters, respectively. More comprehensive information can be found in appendix A.4.



(a) **(b)**

(c) **(d)**

Figure 3.57: Scaling behavior of selected transit time related parameters for the HS transistors of [76]: **(a)** V_{CEs} vs. $P_{\mathrm{E0}}/A_{\mathrm{E0}}$, **(b)** V_{lim} vs. $P_{\mathrm{E0}}/A_{\mathrm{E0}}$, **(c)** τ_0 vs. $P_{\mathrm{E0}}/A_{\mathrm{E0}}$ and **(d)** r_{Ci0} vs. $1/A_{\mathrm{E,eff}}$.

Even during extraction step *(iii)*, current spreading is assumed to be negligible (i.e. the current spreading parameters L_{B} and L_{L} are assumed to be zero), which might not be the case depending on the collector doping distribution. Therefore, the internal collector resistance r_{Ci0} is scaled by applying optimization to the reference data for different geometries. The current spreading angle δ_{C} is obtained and the model for $\Delta\tau_{\mathrm{fh}}$ needs to be adjusted for consistency with the current spreading description of HICUM. The general idea for this approach was already illustrated in [113]. Contrary to [113], the relevant range for I_{CK} is used for the adjustment instead of a single point.

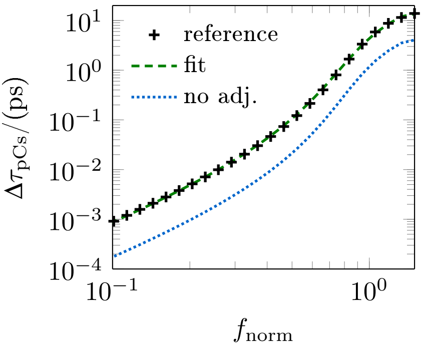


Figure 3.58: Illustration of the method for adjusting $\Delta\tau_{\mathrm{pCs}}$ to include current spreading in the model depending on the spreading angle δ_{C}. The reference corresponds to the extracted model without current spreading for a single transistor. Using the extracted model with current spreading leads to a large deviation, which can be compensated by adjusting τ_{pCs} and a_{hc} to the reference data.

By performing the correction for current spreading, the correct high current transit time, which corresponds to the 1D transport, is obtained. Adjusting the saturated collector transit time ($\tau_{\mathrm{pCs}} = f_{\tau\mathrm{hc}}\tau_{\mathrm{hcs}}$) and a_{hc} for fitting the current spreading description to the extracted model without current spreading for a single transistor leads to fig. 3.58. The transit time increase for τ_{pCs} ranges from 50 % for the MV transistors to 500 % for the HV version depending on δ_{C}. To the author's knowledge, there is no method to extract the partitioning factor $f_{\tau\mathrm{hc}}$ and thus, the base and collector portion of the high current transit time are assumed to be identical ($f_{\tau\mathrm{hc}} = 0.5$). The parameter change of a_{hc} is much smaller than for τ_{pCs} and therefore the approach of [113] – which only relies on changing τ_{pCs} – is confirmed (especially when only focusing on $f_{\mathrm{norm}} < 1$).

Besides the extracted transit time parameters that are relevant for TCAD calibration, the most important conclusion of this chapter is revealed by investigating the different current spreading angles (see table 3.15): δ_{C} is surprisingly large for the HS transistor flavor, which is in line with other previous observations, e.g. with the negligible area component of the BC diode current or the increased vertical resistance component of R_{Bx}. This implies

parameter (unit)	δ_C (HS) (°)	δ_C (MV) (°)	δ_C (HV) (°)
value	19.8	5.4	31.9
parameter (unit)	$f_{\tau\mathrm{pi}}$ (HS) (1)	$f_{\tau\mathrm{pi}}$ (MV) (1)	$f_{\tau\mathrm{pi}}$ (HV) (1)
value	1.00	1.23	1.25

Table 3.15: Extracted current spreading angle δ_C and the low current transit time ratio $f_{\tau\mathrm{pi}}$ for the three transistor flavors.

an increased collector doping towards the external BC junction, yet the exact location remains unknown. It is possible that the well proximity effect (WPE) [114] has an influence on the selectively implanted collector and may lead to an increased doping at the STI edge. The results are again confirmed by the extracted low current transit time ratio $f_{\tau\mathrm{pi}} = \tau_{0\mathrm{p}}/\tau_{0\mathrm{a}}$ obtained from the scaling of τ_0 (based on optimization) illustrated in fig. 3.57: $f_{\tau\mathrm{pi}}$ is typically larger than one because the transit time $\tau_{0\mathrm{p}}$ of the peripheral transistor is larger than the area related component $\tau_{0\mathrm{a}}$, i.e. the internal transistor should be faster since the profile in vertical direction is optimized for performance (especially the base doping and the germanium shape). $f_{\tau\mathrm{pi}} \approx 1$ indicates a significantly increased external collector doping of the HS transistors.

3.11 Transfer current

The extraction of the transfer current is the "discipline reine" of the HICUM parameter extraction, especially in the high injection regime. To understand how the transfer current is scaled, the γ_C approach shall be explained briefly. As was shown in fig. 3.3 on page 38, the internal transistor region consists of two components: the area and peripheral transistor. Hence, there are actually two different transfer currents, which need to be modeled for matching different device geometries. To save model runtime and extraction effort, the two components are merged into one, as described by the γ_C approach [115]:

$$\begin{aligned} I_\mathrm{T} &= \overline{I}_\mathrm{Ta} A_\mathrm{E0} + I'_\mathrm{Tp} P_\mathrm{E0} \\ &= \overline{I}_\mathrm{Ta} \left(A_\mathrm{E0} + \underbrace{\frac{I'_\mathrm{Tp}}{\overline{I}_\mathrm{Ta}}}_{\gamma_\mathrm{C}} P_\mathrm{E0} \right) \\ &= \overline{I}_\mathrm{Ta} A_\mathrm{E,eff} . \end{aligned} \tag{3.67}$$

γ_C has the dimension of a length and allows to relate the total transfer current to the area component $\overline{I}_\mathrm{Ta}$ and the effective emitter area $A_\mathrm{E,eff}$ without having to specify I'_Tp. Consequently, $A_\mathrm{E,eff}$ needs to be used to scale $\overline{I}_\mathrm{Ta}$. Applying the scaling to a simplified description of the transfer current of HICUM leads to

$$I_\mathrm{T} = \frac{\overline{c}_\mathrm{10a} A^2_\mathrm{E,eff}}{\overline{Q}_\mathrm{p0} A_\mathrm{E,eff} + h^*_\mathrm{jEi} \overline{Q}_\mathrm{jEi} A_\mathrm{E0}} \exp\left(\frac{V_\mathrm{BE}}{V_\mathrm{T}}\right) , \tag{3.68}$$

with the GICCR constant c_{10} and the effective weight factor h^*_jEi as parameters. (3.68) already reveals a first inconsistency: As the BE junction charge $\overline{Q}_\mathrm{jEi}$ needs to be scaled with A_E0 (for consistency with the AC behavior), I_T is not a sole function of $A_\mathrm{E,eff}$ anymore. To restore the required behavior, the effective weight factor relates to the actual h_jEi by $h^*_\mathrm{jEi} = h_\mathrm{jEi} A_\mathrm{E,eff} / A_\mathrm{E0}$. Similarly, the effective weight factor for the BC junction charge $\overline{Q}_\mathrm{jCi}$ is defined: $h^*_\mathrm{jCi} = h_\mathrm{jCi} A_\mathrm{E,eff} / A_\mathrm{E0}$.

γ_C was bias independent for former processes, but for modern SiGe technologies this is not the case anymore, making the scaling procedure more complex. In [116], a method has been developed to model the bias dependence by performing a scaling for h_{jEi}. The derivation of the approach was originally based on the reverse Early voltage but was rewritten for h_{jEi} in [117]. In [118], the scaling was extended to include the parameter a_{hjEi}, which models the bias dependence of h_{jEi}. Introducing the saturation current $\overline{I}_{\mathrm{Sa}} = \overline{c}_{\mathrm{10a}}/\overline{Q}_{\mathrm{p0}}$[1] allows to rewrite (3.68):

$$I_{\mathrm{T}} = \frac{\overline{I}_{\mathrm{Sa}} A_{\mathrm{E,eff}}}{1 + h_{\mathrm{jEi}} \overline{Q}_{\mathrm{jEi}}/\overline{Q}_{\mathrm{p0}}} \exp\left(\frac{V_{\mathrm{BE}}}{V_{\mathrm{T}}}\right). \tag{3.69}$$

Further, combining (3.69) with (3.67) and inserting the respective descriptions for $\overline{I}_{\mathrm{Ta}}$ and I'_{Tp} leads to

$$\frac{\overline{I}_{\mathrm{Sa}} A_{\mathrm{E,eff}}}{1 + h_{\mathrm{jEi}} \overline{Q}_{\mathrm{jEi}}/\overline{Q}_{\mathrm{p0}}} = \frac{\overline{I}_{\mathrm{Sa}} A_{\mathrm{E0}}}{1 + h_{\mathrm{jEia}} \overline{Q}_{\mathrm{jEi}}/\overline{Q}_{\mathrm{p0}}} + \frac{I'_{\mathrm{Sp}} P_{\mathrm{E0}}}{1 + h_{\mathrm{jEip}} \overline{Q}_{\mathrm{jEi}}/\overline{Q}_{\mathrm{p0}}}. \tag{3.70}$$

For low V_{BE}, $h_{\mathrm{jEi}} \overline{Q}_{\mathrm{jEi}}/\overline{Q}_{\mathrm{p0}} \ll 1$ and hence (3.70) can be simplified (note that $I'_{\mathrm{Sp}} = \gamma_{\mathrm{C0}} \overline{I}_{\mathrm{Sa}}$ and $\gamma_{\mathrm{C0}} = \gamma_{\mathrm{C}}\,(V_{\mathrm{BE}} = 0\,\mathrm{V})$):

$$A_{\mathrm{E,eff}} \left(1 - h_{\mathrm{jEi}} \frac{\overline{Q}_{\mathrm{jEi}}}{\overline{Q}_{\mathrm{p0}}}\right) \cong A_{\mathrm{E0}} \left(1 - h_{\mathrm{jEia}} \frac{\overline{Q}_{\mathrm{jEi}}}{\overline{Q}_{\mathrm{p0}}}\right) + \gamma_{\mathrm{C0}} P_{\mathrm{E0}} \left(1 - h_{\mathrm{jEip}} \frac{\overline{Q}_{\mathrm{jEi}}}{\overline{Q}_{\mathrm{p0}}}\right). \tag{3.71}$$

Around $V_{\mathrm{BE}} = 0\,\mathrm{V}$, a Taylor expansion leads to $\overline{Q}_{\mathrm{jEi}} = \overline{C}_{\mathrm{jEi0}} V_{\mathrm{BE}}$ and therefore the derivative of (3.71) with respect to V_{BE} is

$$\begin{aligned} h_{\mathrm{jEi}} A_{\mathrm{E,eff}} &= h_{\mathrm{jEia}} A_{\mathrm{E0}} + h_{\mathrm{jEip}} \gamma_{\mathrm{C0}} P_{\mathrm{E0}} \\ h_{\mathrm{jEi}} &= h_{\mathrm{jEia}} \frac{A_{\mathrm{E0}}}{A_{\mathrm{E,eff}}} + h_{\mathrm{jEip}} \gamma_{\mathrm{C0}} \frac{P_{\mathrm{E0}}}{A_{\mathrm{E,eff}}}. \end{aligned} \tag{3.72}$$

As the final modelcard needs to use h^*_{jEi}, it is convenient to reintroduce it to (3.72):

---

[1] Note that $\overline{Q}_{\mathrm{p0}}$ was determined from tetrode measurements and cannot be extracted from the transfer current characteristics at medium to high injection for modern SiGe technologies, as the influence of the weight factors is not negligible anymore.

$$h_{\mathrm{jEi}}^{*}=h_{\mathrm{jEia}}+h_{\mathrm{jEip}}\gamma_{\mathrm{C0}}\frac{P_{\mathrm{E0}}}{A_{\mathrm{E0}}},\tag{3.73}$$

which reveals a linear relationship. From [118],

$$\lim_{V_{\mathrm{BE}}\to 0}\frac{\partial h_{\mathrm{jEi}}}{\partial V_{\mathrm{BE}}}=a_{\mathrm{hjEi}}\frac{z_{\mathrm{Ei}}}{V_{\mathrm{dEi}}}\tag{3.74}$$

and hence, by calculating the derivative of (3.73) w.r.t. V_{BE}, the scaling for a_{hjEi} is obtained:

$$a_{\mathrm{hjEi}}^{*}=a_{\mathrm{hjEia}}+a_{\mathrm{hjEip}}\gamma_{\mathrm{C0}}\frac{P_{\mathrm{E0}}}{A_{\mathrm{E0}}}.\tag{3.75}$$

Note that for the final modelcard $a_{\mathrm{hjEi}}=a_{\mathrm{hjEi}}^{*}A_{\mathrm{E0}}/A_{\mathrm{E,eff}}$ – instead of a_{hjEi}^{*} – needs to be used.

To apply the strategy to measurement data, a PoA separation for the transfer current needs to be performed first. The parameters for the transfer current components are extracted using the method described in [117] and the model can then be compared with measurements[2]. The quality of the extraction can be assessed best by plotting the normalized transfer current $I_{\mathrm{T,norm}}=I_{\mathrm{T}}/\left[I_{\mathrm{S}}\exp\left(V_{\mathrm{BE}}/V_{\mathrm{T}}\right)\right]$ (see fig. 3.59). To verify the validity of the scalable model, a PoA separation is performed on simulated characteristics of the low-bias model for I_{T}: γ_{C} is calculated and compared with measurements in fig. 3.60. As can be observed in the figures, the model works reliably for the analyzed process. However, the extracted parameters of I'_{Tp} strongly depend on the selected extraction range, as the measurement accuracy is limited for small V_{BE}.

The extraction of the transfer current at large forward bias is a complex task: The impact of the external resistances, self-heating and all charges need to be taken into account for a reliable extraction. This is why the temperature coefficients need to be determined first for a single transistor, which is done by applying the procedure outlined hereafter to measurements at different ambient temperatures. Figures 3.61 and 3.62 show the agreement

---

[2] It is important to extract the parameters $\overline{I}_{\mathrm{Sa}}$ and I'_{Sp} and to determine γ_{C0} based on $\gamma_{\mathrm{C0}}=I'_{\mathrm{Sp}}/\overline{I}_{\mathrm{Sa}}$. Extrapolating linearly for γ_{C0} based on γ_{C} vs. V_{BE} will lead to incorrect results.

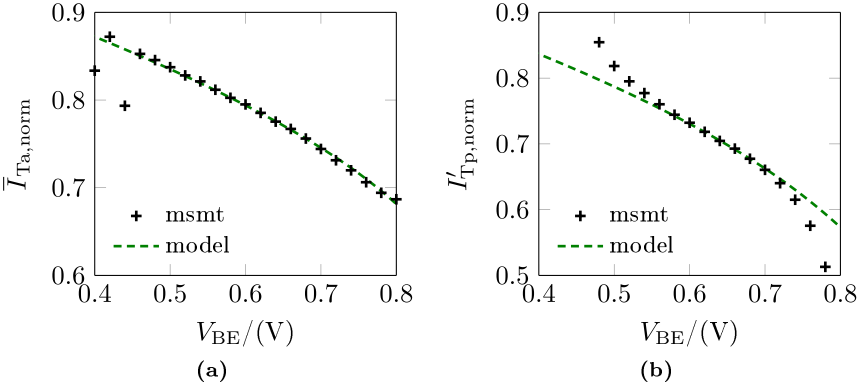


Figure 3.59: Result for the normalized transfer current after extracting the parameters c_{10}, h_{jEi} and a_{hjEi} (MV transistors of [76]). Comparison of measurements (markers) and model (lines) for **(a)** $\overline{I}_{\mathrm{Ta,norm}}$ vs. V_{BE} and **(b)** $I'_{\mathrm{Tp,norm}}$ vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$.

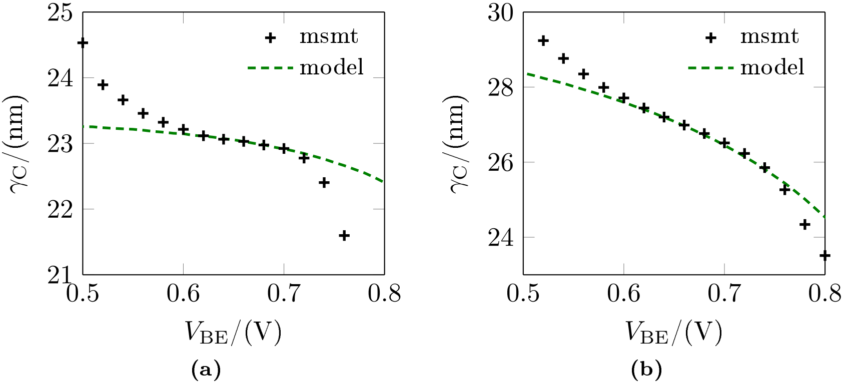
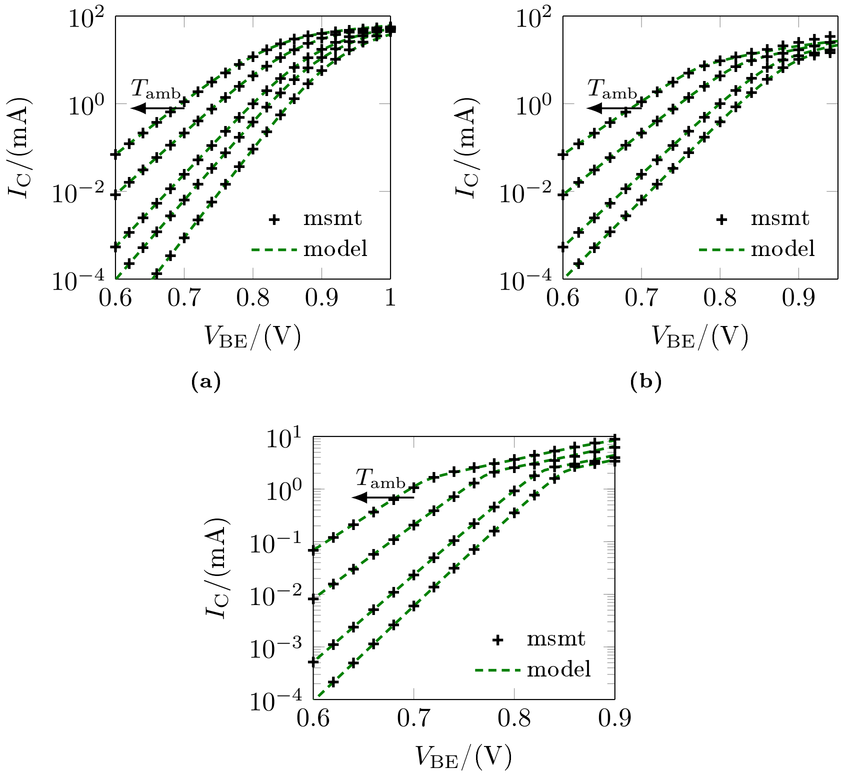


Figure 3.60: Result for γ_{C} obtained by a PoA separation (process of [76]) at $V_{\mathrm{BC}} = 0\,\mathrm{V}$. Comparison of measurements and model for **(a)** the HS and **(b)** the HV transistor versions.



(a) (b)

(c)

Figure 3.61: Comparison of measurements and model for the collector current I_C vs. V_{BE} at different ambient temperatures for devices with $l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$ and $b_{\mathrm{drawn}} = 180\,\mathrm{nm}$ at $V_{BC} = 0\,\mathrm{V}$ (process of [76]). Results for **(a)** the HS ($T_{\mathrm{amb}} = (-30, 0, 25, 75 \text{ and } 125)\,°\mathrm{C}$), **(b)** the MV ($T_{\mathrm{amb}} = (0, 25, 75 \text{ and } 125)\,°\mathrm{C}$) and **(c)** the HV ($T_{\mathrm{amb}} = (0, 25, 75 \text{ and } 125)\,°\mathrm{C}$) transistor versions.

for the model with the measurement data at different temperatures. More comprehensive information can be found in appendix A.5.

For other extraction methods – e.g. [112] – it is assumed that the transfer current of the final model, which “causes” the high current transit time charge ΔQ_f, is identical with the measured I_{Tf}, which is not necessarily the case at high injection. Applying this assumption, it is possible to calculate ΔQ_f

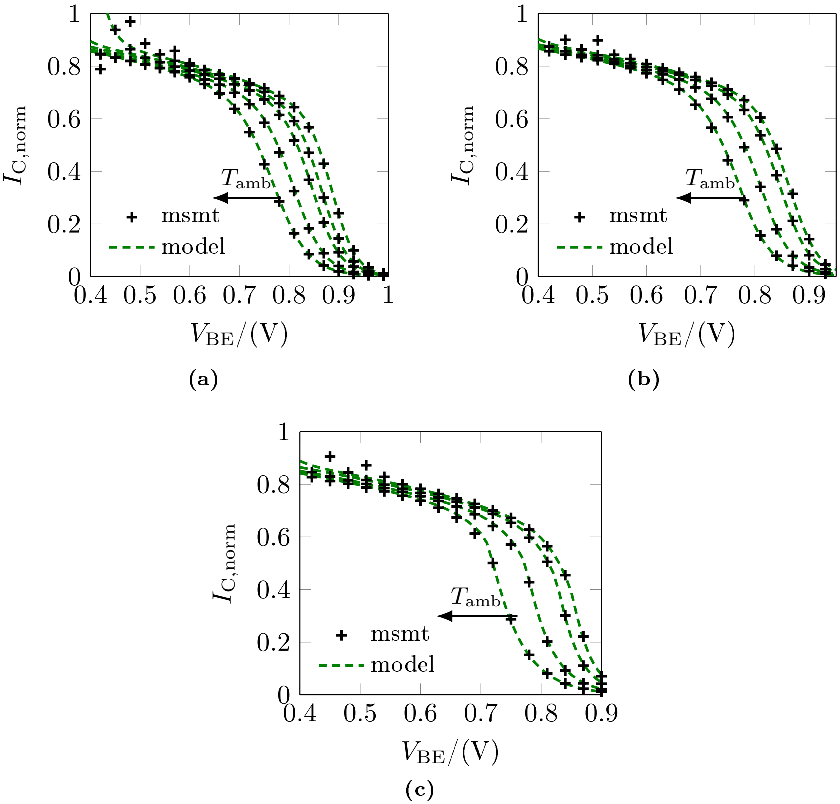


Figure 3.62: Comparison of measurements and model for the normalized collector current $I_{\mathrm{C,norm}}$ vs. V_{BE} at different ambient temperatures for devices with $l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$ and $b_{\mathrm{drawn}} = 180\,\mathrm{nm}$ at $V_{\mathrm{BC}} = 0\,\mathrm{V}$ (process of [76]). Results for **(a)** the HS ($T_{\mathrm{amb}} = (-30, 0, 25, 75$ and $125)\,°\mathrm{C}$), **(b)** the MV ($T_{\mathrm{amb}} = (0, 25, 75$ and $125)\,°\mathrm{C}$) and **(c)** the HV ($T_{\mathrm{amb}} = (0, 25, 75$ and $125)\,°\mathrm{C}$) transistor versions.

from the measured I_{Tf}. However, the previously extracted parameters are usually somewhat defective; especially ΔQ_{f} at high injection could not be matched for the process analyzed here due to the BC barrier effect [74] and the model shortcomings for this region [119]. Hence, the final model for I_{Tf} might not be fully accurate. Accepting this limitation complicates the extraction procedure a lot, as the internal voltages and ΔQ_{f} will be inconsistent with I_{Tf}.

This is the reason why the weight factors h_{fE} and h_{fC} are typically extracted by running circuit simulations for achieving the best fit. Note though that there is no issue for extracting the parameters r_{hjEi} and h_{f0}, as the model is sufficiently accurate in the corresponding region. For these parameters, the method described in [118] can be applied.

Running simulations needs to be avoided for extracting parameters quickly and hence, a simpler idea is required to solve the problem. The approach chosen here still assumes that the internal voltages are known (defined by the measured I_{Tf}), but the transit time charge and I_{Tf} are forced to be consistent by solving the transfer current equation of HICUM during each iteration step of the optimization. Optimizing h_{fE} and h_{fC} to fit I_{Tf} for $f_{\mathrm{norm}} > 0.3$ at large forward bias concludes the transfer current extraction. The external resistances, self-heating, h_{fE} and h_{fC} are coupled and thus, possible extraction errors in previous extraction steps are partially compensated by the error made for the weight factors.

The extraction for the process of [76] is concluded at this point. The extracted parameters and more information can be found in appendix A.

3.12 Process improvements

For the MV transistors, an alarming behavior for the transfer current is observed: After reaching the high injection region, the current increases again rapidly for large V_{CE} as illustrated in fig. 3.63. Such a behavior cannot be reproduced by the model. Taking a look at the internal device temperature reveals a process issue: Thermal breakdown. Due to the relatively large R_{th} and the increased V_{CE} in comparison to the HS transistors, the temperature increases up to more than 700 K according to the model. Therefore, the region of impurity exhaustion is left and additional carriers are generated leading to an additional positive feedback. Thus, the actual temperature of the device is even larger than predicted by the model, as the actual dissipated power is greater. The onset of thermal breakdown occurs at a temperature of about 500 K, which is somewhat lower than the limit of impurity exhaustion according to standard literature [87]. Note that the model temperature is an effective quantity for matching the device characteristics, i.e. the local temperature inside of the device is somewhat larger. Also, the main problem is not only caused by the large temperature itself, but by the huge temperature increase for small increase of the dissipated power.

To improve the behavior, it is possible to reduce the depth of the DTI – which is currently at 5 µm. A conclusive way to do so would be to estimate the heat flow angle with 45° and to extrapolate to the ideal DTI depth starting from the internal BC junction. That way, the thermal resistance is reduced, but the substrate resistance reduces too – leading to a trade-off. A DTI depth of about 3 µm is obtained. Reducing the STI depth will probably not help much, as the depth already is in line with the simplified 45° rule.

Section 3.5 revealed the main contribution to the external base resistance to be the interface or vertical resistance of the poly- to monosilicon region. Consequently, R_{Bx} can be reduced significantly by increasing the interface area. A possible way to do so – instead of doing a direct process change –, is to use a checkered emitter by changing the transistor layout. It is questionable if such a layout can improve performance because the capacitances will increase too – leading to a trade-off. To evaluate if such a device is useful, the extracted

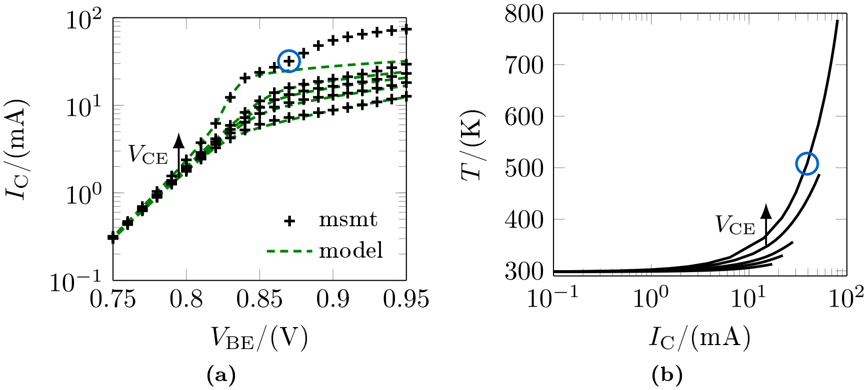
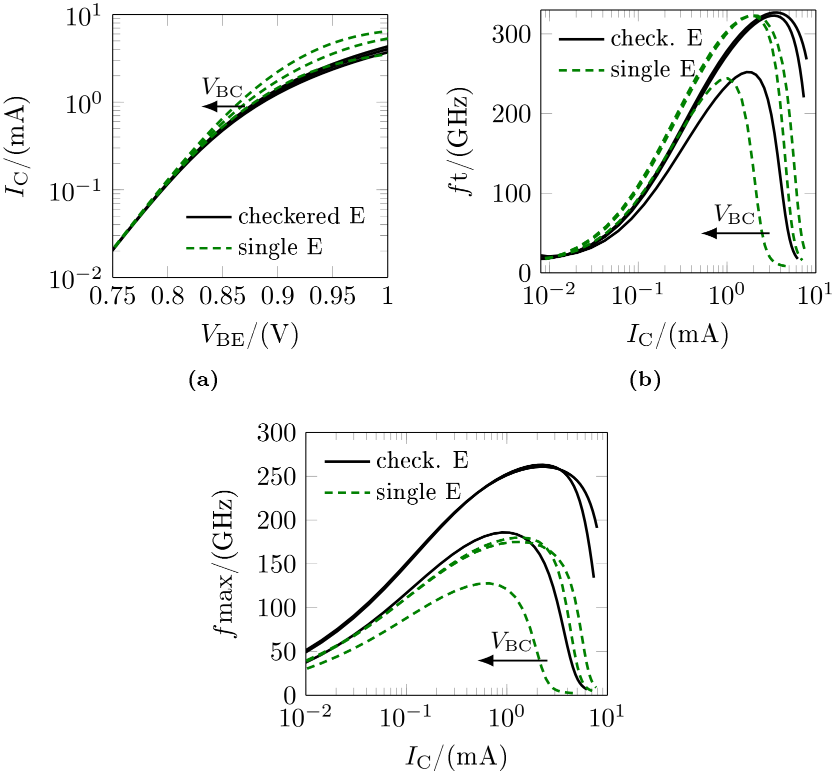


Figure 3.63: Observed thermal breakdown for a device with $l_{\text{drawn}} = 9\,\mu\text{m}$ and $b_{\text{drawn}} = 270\,\text{nm}$ (MV transistor of [76]): **(a)** Comparison of measurements and model for I_C vs. V_{BE} and **(b)** corresponding internal device temperature based on the model. The onset of thermal breakdown is indicated by an additional marker.

model is used to predict its performance. For the comparison, a single emitter device with a drawn emitter area of $180\,\text{nm} \cdot 954\,\text{nm}$ and a multi finger emitter device with a drawn size of $7 \times 180\,\text{nm} \cdot 180\,\text{nm}$ are analyzed. Between each of the fingers the minimum size for silicidation is used, leading to a total drawn length of $3.132\,\mu\text{m}$. Designing the transistors with these dimensions leads to identical collector currents at low injection according to the model. The difference in size demonstrates that the integration density is reduced drastically for the checkered device.

The scaling for the checkered emitter device is relatively straightforward. Most of the parameters are scaled according to the PoA results and the external base and collector resistance are determined by device simulation. However, the scaling for R_{th} is not obvious and therefore the worst case scenario is assumed: The value for R_{th} is assumed to be identical to a single emitter device with a drawn size of $180\,\text{nm} \cdot 3.132\,\mu\text{m}$ (leading to an overestimation). The internal collector resistance and current spreading is taken into account by calculating the corresponding parameters for a single emitter ($180\,\text{nm} \cdot 180\,\text{nm}$) and dividing the result for R_{Ci0} by seven. Plotting



(a) **(b)**

(c)

Figure 3.64: Study for improving the external base resistance. Comparison of simulations for a single emitter ($l_{\mathrm{drawn}} = 954\,\mathrm{nm}$ and $b_{\mathrm{drawn}} = 180\,\mathrm{nm}$) and a checkered emitter device ($7 \times l_{\mathrm{drawn}} = 180\,\mathrm{nm}$ and $b_{\mathrm{drawn}} = 180\,\mathrm{nm}$) for the HS technology of [76]. Results for **(a)** I_{C} vs. V_{BE}, **(b)** f_{t} vs. I_{C} and **(c)** f_{max} vs. I_{C} for $V_{\mathrm{BC}} = (-0.5, 0 \text{ and } 0.5)\,\mathrm{V}$.

the most important characteristics leads to fig. 3.64: As the capacitances of the checkered device increase, the transit frequency at low currents decreases considerably. Nevertheless, as R_{Ci0} decreases (current spreading for each of the emitter fingers is larger, reducing the resistance), the peak of f_{t} for both devices is quite similar. Although the gain for f_{max} is very promising, it is unclear if a fabricated device would behave similarly. With shrinking emitter dimensions, both the doping profiles of the vertical transistor and the interface properties (e.g. of the emitter) can differ and change the performance. Future trials with specific test structures of checkered devices should therefore also vary the emitter finger length.

CHAPTER 4

TCAD calibration for SiGe HBTs

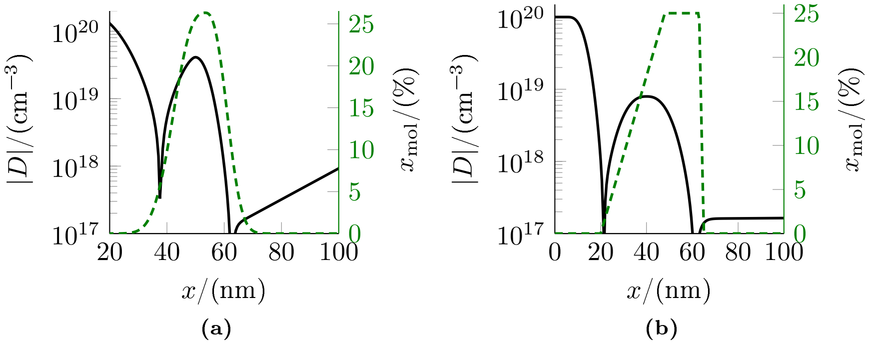
By completing the scalable extraction for the process of [76] (chapter 3) and setting initial physical models (chapter 2), the TCAD calibration can be performed. Although a lot of physical model development has been performed during the past years (e.g. [81,82,89]), these developments mainly focused on deriving physical models for DD/HD simulations from more complex physical approaches like the BTE. Major measurement based physical model development (e.g. [83,85]) started already in the 50ies and lasted until the beginning of the 90ies. Corresponding results still serve as reference today. Model development for scattering mechanisms – required for the BTE simulations – also took place during this period and hence, most physical models still relate to the respective equipment of that time. Even worse, for some underlying physics no measurements exist at all – e.g. electron affinity vs. composition (SiGeC system) – and hence, physical models must partially rely on theoretical evaluations or extrapolation. Also, cross correlations are not well known and are complex to measure – e.g. mobility depends on composition, doping, strain and field (a five dimensional system) – and thus, each influence is superimposed linearly (without cross correlations) within the used physical models.

Additional uncertainties stem from secondary ion mass spectrometry (SIMS) measurements or process simulations for obtaining doping profiles. As has been shown in [120], profile measurements of large transistor boxes of 100 µm × 100 µm size – which are required to apply SIMS – do not agree with other profile measurements for smaller devices that have practical relevance. The issue can be avoided for the detection of alloy concentrations (e.g. germanium content) by using electron dispersive X-ray spectroscopy (EDX) measurements, which can be applied to smaller TEM samples. Nevertheless, the sensitivity of EDX is too low to detect doping concentrations reliably and hence, SIMS is mandatory. Employing SIMS, different doping species require different primary ions for the bombardment and therefore, two different measurements need to be aligned for the full doping profile view. This leads to an uncertainty of about (4 to 5) nm for the position of the base doping and composition profile, which is significant if compared to the total base width. SIMS measurements inherently involve the sputtering of an imperfect cavity, as the sputtering angle is not exactly perpendicular to the probe surface. This means that the ion beam cannot focus on a single depth and the obtained doping concentrations flatten in comparison to the probe.

Accepting that there is an uncertainty for the physical models and doping profiles means that they may be tuned (in a reasonable range) for better agreement with the measurements. In a first step, the doping profile will be adjusted for agreement with the measured capacitances according to some of the approaches of [75]. If the obtained profile result is not feasible (e.g. if there is a large deviation for the germanium profile obtained by the method and the EDX measurement), the physical models and the transport model itself can be questioned and adjusted.

4.1 1D profile calibration – method description

The idea behind the profile adjustment is a (limited) one-to-one correspondence between electrical reference data and simulated profiles [75]. Some quantities, like the zero-bias hole charge or the internal junction capacitances



(a) **(b)**

Figure 4.1: **(a)** Zoom of the reference doping profile ($D = N_\mathrm{A}^- - N_\mathrm{D}^+$ and x_mol vs. vertical depth x) used to generate synthetic reference data. **(b)** Zoom of the initial doping profile serving as a starting point for the profile adjustment.

are only affected by electrostatics and hence, allow to reconstruct doping profiles without a large impact from the chosen transport model and the physical models. Other characteristics – like the collector current and the transit frequency – depend on carrier transport and therefore might require known material models for a profile reconstruction. For illustrating the method, the issue is circumvented in this section by using synthetic reference data generated from HD simulations (and therefore known material models).

The doping profile shown in fig. 4.1 (a) is used for generating a set of reference characteristics. $\overline{C}_\mathrm{jEi}$, $\overline{C}_\mathrm{jCi}$, f_t, $\overline{I}_\mathrm{T}$, $R_\mathrm{s,Bi}$, $\overline{Q}_\mathrm{p0}$, the output conductance g_o and the normalized transconductance $g_\mathrm{m,norm} = \overline{g}_\mathrm{m}/\overline{I}_\mathrm{T} \cdot V_\mathrm{T}$ serve as target quantities for tuning the initial doping profile in fig. 4.1 (b). For a fair evaluation, the profiles are assumed to be very different initially. Note that the reference and initial profiles use an exponential and trapezoidal germanium description, respectively. The employed initial doping profile is also very generic: As the one-to-one correspondence between electrical data and profile is limited, the profile information that can be recovered is limited and thus, only a reduced amount of profile descriptions is used. Profiles based on an exponential function

$$N_{\mathrm{exp}}(x) = N_0 \exp\left(\left|\frac{x - x_0}{a_{\mathrm{x}}}\right|\right)^{b_{\mathrm{x}}} \tag{4.1}$$

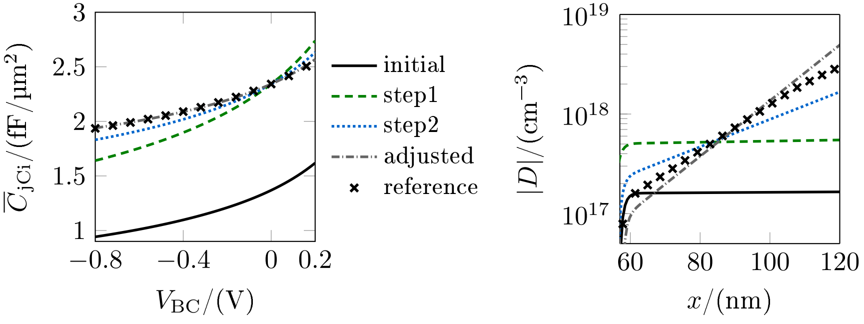
are used to model the base and internal collector profile (parameters N_0, a_{x}, b_{x} and x_0). A profile based on a complementary error function

$$\begin{aligned} N_{\mathrm{erfc}}(x) &= N_0 \,\mathrm{erfc}\left(\frac{x - x_0}{a_{\mathrm{x}}}\right) \\ \mathrm{erfc}(x) &= 1 - \frac{2}{\sqrt{\pi}} \int_0^x \exp\left(-t^2\right) \mathrm{d}t, \end{aligned} \tag{4.2}$$

is used for the emitter (parameters N_0, a_{x} and x_0). For the buried layer an additional complementary error function is used, which will remain fixed. At the end of the adjustment procedure, the reference profile will be restored if the electrical results are in agreement with the target characteristics and if there is a unique solution, i.e. if there is a one-to-one correspondence between electrical characteristics and doping profile.

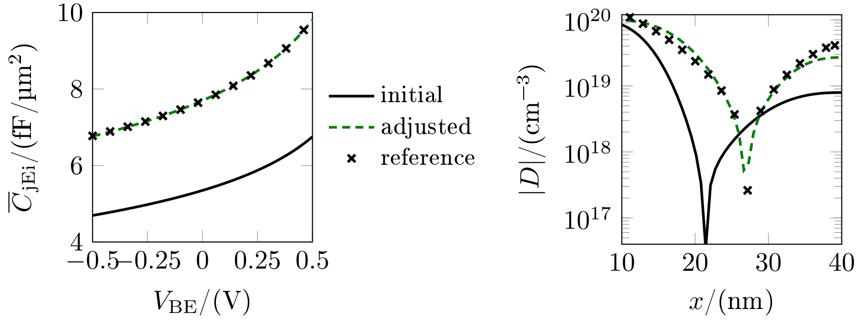
The first adjustment steps focus on matching the junction capacitances of the reference. $\overline{C}_{\mathrm{jEi}}$ and $\overline{C}_{\mathrm{jCi}}$ are directly related to the extension of the respective space charge regions of the 1D transistor. As the base doping N_{B} is much greater than the doping of the internal collector N_{Ci}, N_{Ci} determines the SCR width and hence, $\overline{C}_{\mathrm{jCi}}$. The slope and curvature of the collector doping determine the bias dependence of the capacitance. Adjusting the parameters $N_{0\mathrm{C}}$, a_{xC} of the collector profile (and assuming $b_{\mathrm{xC}} = 1$) for matching the reference data leads to fig. 4.2. As can be observed in the figure, the adjusted doping profile does not correspond to the reference even though the capacitance is matched. The reason for the discrepancy is the germanium profile that has not been adjusted yet, causing a different permittivity of the BC-SCR.

The same procedure is repeated for $\overline{C}_{\mathrm{jEi}}$ – this time by changing the parameters $x_{0\mathrm{E}}$, a_{xE} and a_{xB} of the emitter/base profile (keeping the initial value for b_{xB}). Simultaneously, the maximum doping of the base $N_{0\mathrm{B}}$ is tuned for forcing $\overline{Q}_{\mathrm{p0}}$. As is depicted in fig. 4.3, there is still a large deviation between the adjusted profile and the reference. However, the result is still inconsistent as other electrical characteristics have not been matched yet. Consequently, it is necessary to couple all relevant electrical quantities – allowing for profile



(a) **(b)**

Figure 4.2: Results for the profile adjustment procedure of the BC space charge region. **(a)** $\overline{C}_{\mathrm{jCi}}$ vs. V_{BC}: Comparison of different optimization steps with the reference. **(b)** Zoom of the corresponding doping profile region ($D = N_{\mathrm{A}}^{-} - N_{\mathrm{D}}^{+}$ vs. vertical depth x).



(a) **(b)**

Figure 4.3: Results for the profile adjustment procedure of the BE space charge region and total base doping. **(a)** $\overline{C}_{\mathrm{jEi}}$ vs. V_{BE}: Comparison between results of the initial, adjusted and the reference doping profile. **(b)** Zoom of the corresponding doping profile region ($D = N_{\mathrm{A}}^{-} - N_{\mathrm{D}}^{+}$ vs. vertical depth x).

interaction and consistent electrical results – for a final profile agreement.

The next step exploits the sensitivity of the collector current to the band gap in the base. Aside from band gap narrowing, which certainly plays a role, the main contributor to the band gap reduction is alloying. Hence, by changing the germanium peak concentration, it is possible to match the

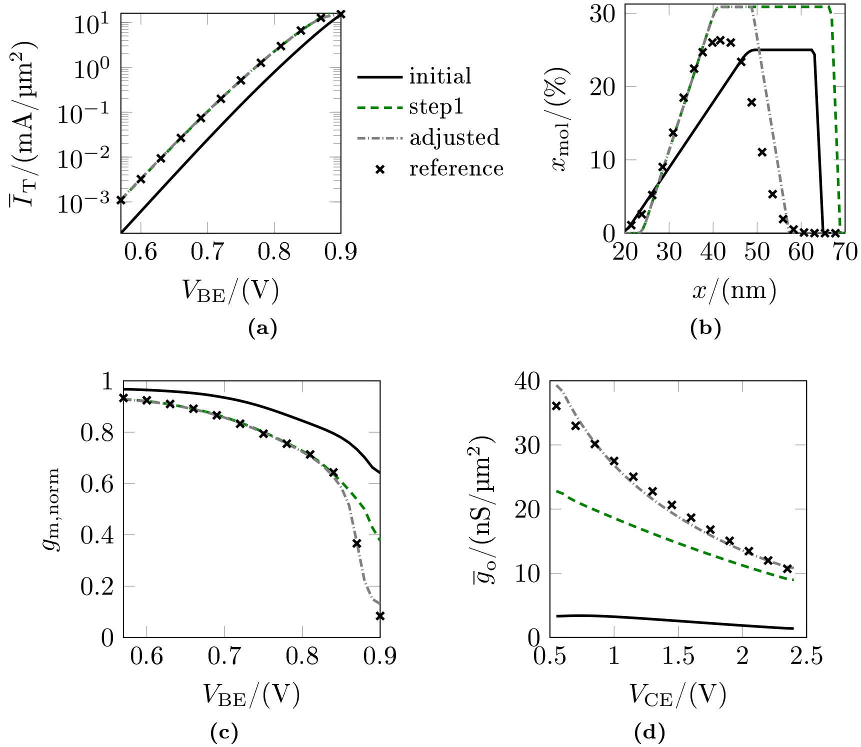
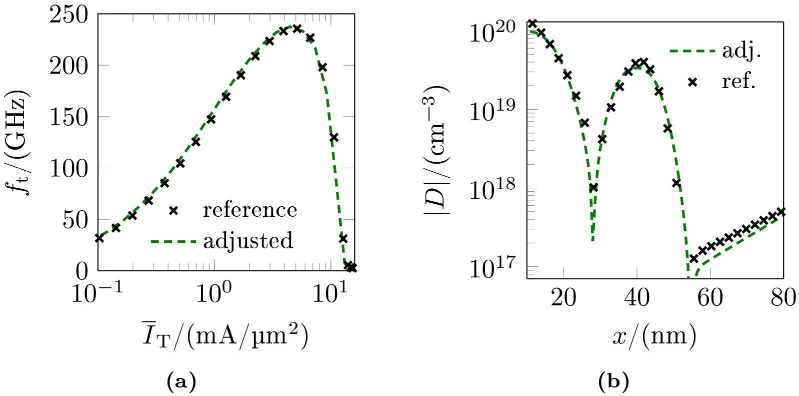


Figure 4.4: Results for the profile adjustment procedure of the germanium description. Comparison of different optimization steps with the reference for **(a)** $\overline{I}_T$ vs. V_{BE} at $V_{BC} = 0\,\mathrm{V}$, **(c)** $g_{m,norm}$ vs. V_{BE} at $V_{BC} = 0\,\mathrm{V}$ and **(d)** $\overline{g}_o$ vs. V_{CE} at $V_{BE} = 0.6\,\mathrm{V}$. **(b)** Zoom of the corresponding doping profile region ($D = N_A^- - N_D^+$ vs. vertical depth x).

collector current. Additionally, the rising and falling slope of the germanium profile will determine the reverse Early voltage and g_o, respectively [121]. Applying the strategy to the example leads to fig. 4.4. The method allows to capture the rising and falling slopes of the germanium profile well, even if the base width is not yet consistent with the reference. The position of the edges and the maximum germanium concentration, however, are not accurate and need to be refined for consistency later.

To complete a first calibration run, the base width and the maximum



(a) **(b)**

Figure 4.5: Results for the profile adjustment procedure neutral base region. **(a)** f_t vs. $\overline{I}_\mathrm{T}$ at $V_\mathrm{BC} = 0\,\mathrm{V}$: Comparison between results of the adjusted and the reference doping profile. **(b)** Zoom of the corresponding doping profile region ($D = N_\mathrm{A}^- - N_\mathrm{D}^+$ vs. vertical depth x).

doping of the base N_0B are tuned again to match the characteristics of f_t (changing a_xB while keeping the initial value for b_xB) and $\overline{Q}_\mathrm{p0}$, respectively. After this step, the doping profile is already – more or less – in agreement with the reference (see fig. 4.5).

For better consistency the described steps are repeated once, leading to the characteristics illustrated in fig. 4.6. In total, six doping profile parameters and five parameters of the germanium description were adjusted. By including a greater bias range for the reference data, the number of tunable parameters for a one-to-one correspondence can be increased. For example, the space charge region extension increases at larger negative bias, which is represented by a capacitance change. Therefore (as has been found by additional trials), eleven to thirteen profile parameters can be reconstructed by the method depending on the quality of the reference data, which in turn leads to a very important hypothesis: Eleven to thirteen degrees of freedom are enough to reproduce an arbitrary (but consistent) combination of electrical results by means of device simulation. Note though that the form of the result depends on the initially assumed profile shape.

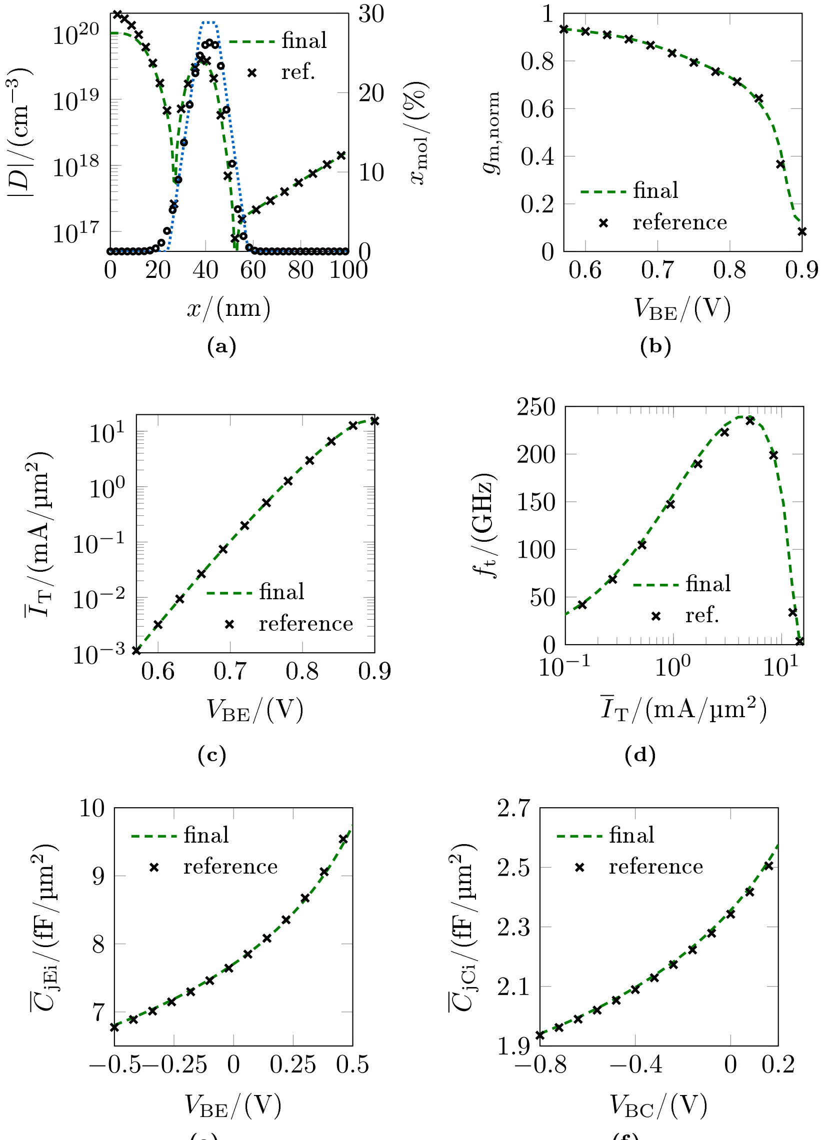


Figure 4.6: Final results of the profile adjustment procedure. Comparison between the final profile and the reference for **(b)** $g_{\mathrm{m,norm}}$ vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$, **(c)** $\overline{I}_{\mathrm{T}}$ vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$, **(d)** f_{t} vs. $\overline{I}_{\mathrm{T}}$ at $V_{\mathrm{BC}} = 0\,\mathrm{V}$, **(e)** $\overline{C}_{\mathrm{jEi}}$ vs. V_{BE} and **(f)** $\overline{C}_{\mathrm{jCi}}$ vs. V_{BC}. **(a)** Zoom of the corresponding doping profile region ($D = N_{\mathrm{A}}^{-} - N_{\mathrm{D}}^{+}$).

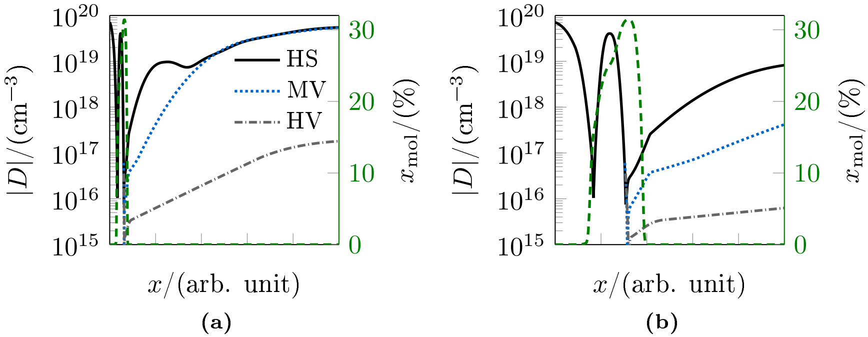


Figure 4.7: 1D doping profiles obtained from process simulations for the HS, MV and HV transistor versions of process [76]. **(a)** Profile overview: $D = N_\mathrm{A}^- - N_\mathrm{D}^+$ vs. vertical depth x and **(b)** zoom of the internal doping profile region.

4.2 1D profile calibration – application to measurement data

To generate the reference data used for the calibration, the previously extracted compact model is reduced to its 1D part in accordance with the 1D simulation approach. That means that the following settings are applied:

- All resistances and external capacitances are set to zero.
- All peripheral capacitances and currents are set to zero – that also means $\gamma_\mathrm{C} = 0\,\mathrm{nm}$.
- δ_C is set to zero (The reference data need to be free from current spreading).
- The reference data need to be free from self-heating.

Using these settings, the 1D modelcard ($A_\mathrm{E0} = 1\,\mathrm{\mu m}^2$) is generated, simulations at 300 K are performed for various bias conditions and reference data for the profile calibration are obtained. Subsequently, process simulations are executed to obtain initial doping profiles for the calibration. As displayed in fig. 4.7, the corresponding profiles for the HS, MV and HV transistor versions only differ for the collector doping.

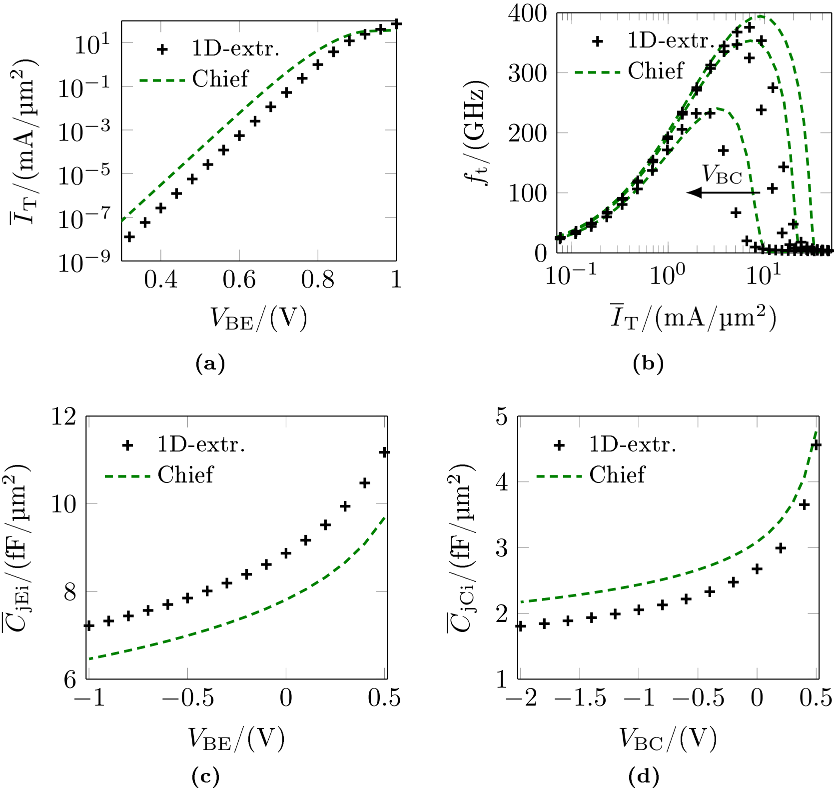


Figure 4.8: Initial comparison of the extracted 1D reference with HD simulations using the 1D profiles of process simulations (HS transistors of [76]). Results for **(a)** $\overline{I}_\mathrm{T}$ vs. V_BE at $V_\mathrm{BC} = 0\,\mathrm{V}$, **(b)** f_t vs. $\overline{I}_\mathrm{T}$ for $V_\mathrm{BC} = (-0.5, 0 \text{ and } 0.5)\,\mathrm{V}$, **(c)** $\overline{C}_\mathrm{jEi}$ vs. V_BE and **(d)** $\overline{C}_\mathrm{jCi}$ vs. V_BC.

For an initial comparison, device simulations are performed using the process TCAD profiles. The results are shown in fig. 4.8 for the HS transistor flavor (the corresponding plots for the MV and HV transistors can be found in appendix B.1). Additionally, a zero-bias hole charge of $\overline{Q}_\mathrm{p0} = 24.7\,\mathrm{fC}/\mu\mathrm{m}^2$ is obtained from the simulations, which aligns well with the extracted value. Nevertheless, the initial comparison is somewhat discouraging for the simulated transfer current with a factor ten discrepancy. The deviation can be explained by comparing the effective band gap in the base extracted for the

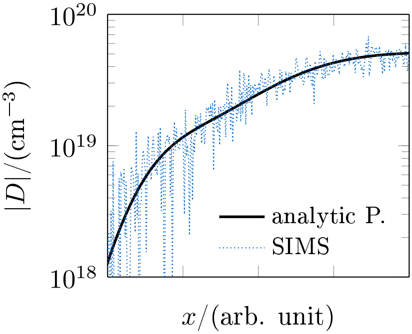


Figure 4.9: Adjusted collector doping profile according to SIMS measurements for the HS transistor version of process [76]. $D = N_\mathrm{A}^- - N_\mathrm{D}^+$ vs. vertical depth x.

compact model (required for matching the temperature dependence of the collector current) with the average band gap of the base in the simulations: $V_\mathrm{gB} = 1.01\,\mathrm{V}$ vs. $V_\mathrm{gB,avg,0K} = 0.93\,\mathrm{V}$. As the germanium profile is known well from EDX measurements for relevant transistor dimensions (with which the process simulations align well), adjusting it does not make sense. Only its position w.r.t. the base doping may be tuned or – more importantly – the material models for the band gap can be changed for an agreement with the transfer current. It is unknown if the cause for the discrepancy is by a model uncertainty of band gap narrowing or alloying. Therefore, the relative change applied to the model parameters a_g (band gap composition) and E_hd (band gap narrowing) – for matching the transfer current – is assumed to be identical, leading to $a_\mathrm{g} = -0.77\,\mathrm{eV}$, $E_\mathrm{hd} = 5.55\,\mathrm{meV}$ and hence, $V_\mathrm{gB,avg,0K} = 0.99\,\mathrm{V}$ for the simulations. Amongst others, the result for the transfer current is shown later in fig. 4.10.

During the next step, the doping profile (HS transistors) of the collector is adjusted to be in line with SIMS measurements for the buried layer as shown in fig. 4.9 (a region for which profile measurements can be trusted, as the doping level is large enough to be detected accurately and the doping change is small enough not to be affected by the effects mentioned in the beginning of chapter 4). As a result, the questionable "doping-hole" in the collector region disappeared (see fig. 4.7 as comparison). Note that the SIMS measurements for the region with $N_\mathrm{D}^+ < 1 \cdot 10^{19}\,\mathrm{cm}^{-3}$ in the collector are too noisy and inaccurate because of the low doping level and the large doping change. Consequently, there is room for a profile adjustment in that region: The internal collector profile is shifted into the base and also its steepness is slightly increased for improving the agreement with the measured internal BC junction capacitance. The modification is an expected outcome because SIMS measurements are too inertial to capture profile changes fast enough.

As explained in section 3.3, the base emitter junction capacitance is not well known from extraction and thus, it is rather advised to tune the emitter profile for f_t at low currents. Comparing the extracted value for $\overline{C}_\mathrm{jEi0}$ of [75] (which is the same process) with the value extracted in table 3.14 reveals an uncertainty of more than 20 %. Even the collector capacitance $\overline{C}_\mathrm{jCi0}$ changed about 10 %. The process TCAD result for the emitter profile is already in the range of uncertainty with the reference and thus, it is not changed. The same applies to the base profile, as the result for the zero-bias hole charge is within the extraction accuracy ($\overline{Q}_\mathrm{p0} = 24.0\,\mathrm{fC}$). To match the extracted value for $\overline{\mu}_{p0}$, the parameter G_ref is slightly increased to $3.5 \cdot 10^{17}\,\mathrm{cm}^{-3}$ for holes (majorities). The result for relevant characteristics, as well as the corresponding doping profile, is illustrated in fig 4.10 for the HS transistors.

The discrepancy for f_t at large currents can be explained with an uncertainty for the internal collector profile (resulting from an inaccuracy of the extracted internal BC capacitance), which changes ρ_Ci0 and the onset of high-current effects. During the extraction, the link between $\overline{C}_\mathrm{jCi0}$ and ρ_Ci0 may not be noticed (as the compact model decouples $\overline{C}_\mathrm{jCi0}$ from the onset of high current effects), but for TCAD simulations an inconsistency/inaccuracy between the two parameters is fatal. If – in such a case – $\overline{C}_\mathrm{jCi0}$ is used to restore profile information of the BC-SCR, the high-current onset of f_t will not be captured accurately. Comparing f_t of the extracted 1D model of this work with [75] leads to the result shown in fig. 4.11. Major deviations at low currents are observed, which stem from the inaccuracy for $\overline{C}_\mathrm{jEi}$. At medium to high injection the data do not differ significantly, but as $\overline{C}_\mathrm{jCi0}$ changed about 10 %, the doping profiles for the collector (which were tuned for matching $\overline{C}_\mathrm{jCi}$) are different. Using the doping profile of [75] allows to capture the high

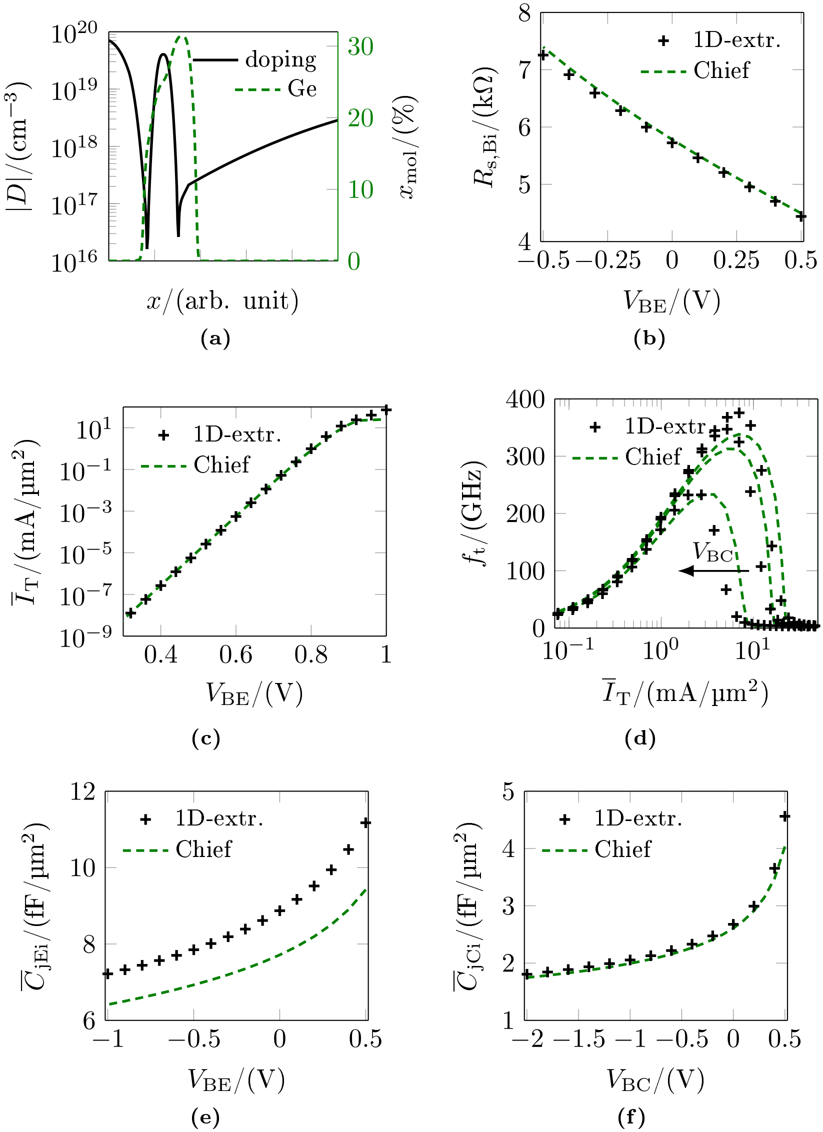


Figure 4.10: Final comparison of the extracted 1D reference with HD simulations for the HS transistors of [76]. The doping profile – incorporating a collector doping change – is illustrated in **(a)**. Results for **(b)** $R_{\mathrm{s,Bi}}$ vs. V_{BE} at $V_{\mathrm{CE}} = 0\,\mathrm{V}$, **(c)** $\overline{I}_{\mathrm{T}}$ vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$, **(d)** f_{t} vs. $\overline{I}_{\mathrm{T}}$ for $V_{\mathrm{BC}} = (-0.5, 0 \text{ and } 0.5)\,\mathrm{V}$, **(e)** $\overline{C}_{\mathrm{jEi}}$ vs. V_{BE} and **(f)** $\overline{C}_{\mathrm{jCi}}$ vs. V_{BC}.

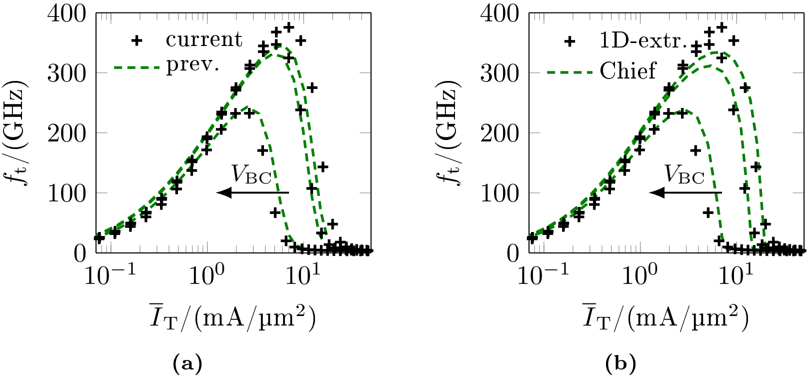
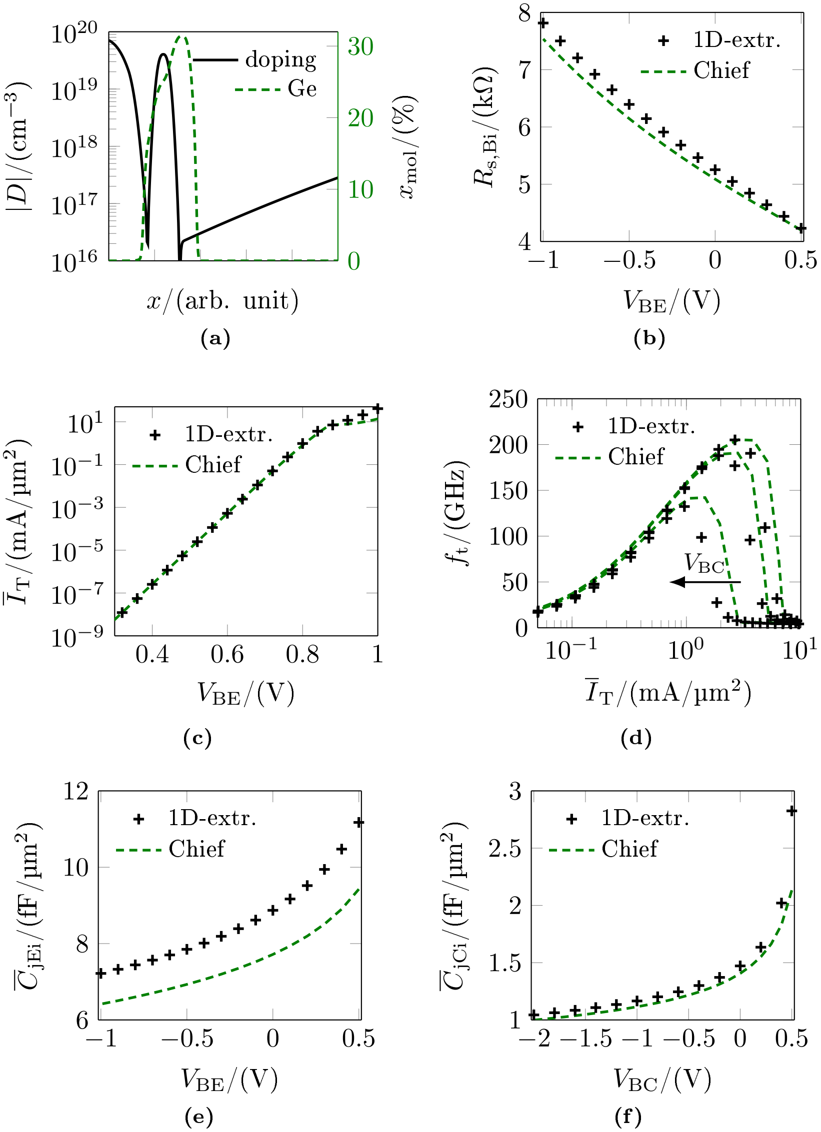


Figure 4.11: **(a)** Comparison of the current and previous 1D reference data obtained for the same process [75]. f_t vs. $\overline{I}_T$ for $V_{BC} = (-0.5, 0 \text{ and } 0.5)\,\text{V}$. **(b)** Comparison of simulations using the previous profile calibration result [75] with current 1D reference data. f_t vs. $\overline{I}_T$ for $V_{BC} = (-0.5, 0 \text{ and } 0.5)\,\text{V}$.

current region of the current reference data accurately (but not $\overline{C}_{jCi}$). All in all, it can be concluded that the remaining deviations are within the uncertainty for the measurements and the extraction approach and that an accurate TCAD calibration is difficult due to the limited measurement accuracy and process tolerances.

The next step focuses on tuning the doping profile for the MV transistors. All parts of the profile can be assumed to be identical with the HS transistors, except for the internal collector, which is adjusted for a trade-off between matching $\overline{C}_{jCi}$ and f_t. The corresponding profile and simulation results are shown in fig. 4.12. $\overline{Q}_{p0} = 25.6\,\text{fF}$ is obtained from the simulations, aligning well with the extracted value of $\overline{Q}_{p0} = 26.1\,\text{fF}$. Note that no physical model changes were applied.

Finally, the HV transistor profile is adjusted. This time, all parts of the profile can be assumed to be identical with the other transistor flavors, except for the collector region (including the implanted buried layer). The doping of the implanted collector region is too low to be measured accurately by SIMS measurements and hence, other measures need to be applied. As can



(a) **(b)** **(c)** **(d)** **(e)** **(f)**

Figure 4.12: Final comparison of the extracted 1D reference with HD simulations for the MV transistors of [76]. The doping profile – incorporating a collector doping change – is illustrated in **(a)**. Results for **(b)** $R_{\mathrm{s,Bi}}$ vs. V_{BE} at $V_{\mathrm{CE}} = 0\,\mathrm{V}$, **(c)** $\overline{I}_{\mathrm{T}}$ vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$, **(d)** f_{t} vs. $\overline{I}_{\mathrm{T}}$ for $V_{\mathrm{BC}} = (-0.5, 0 \text{ and } 0.5)\,\mathrm{V}$, **(e)** $\overline{C}_{\mathrm{jEi}}$ vs. V_{BE} and **(f)** $\overline{C}_{\mathrm{jCi}}$ vs. V_{BC}.

be observed for the initial simulations in appendix B.1 (using the process simulation result), the peak value for f_t is matched relatively well. However, $\overline{C}_\mathrm{jCi}$ is greatly underestimated: This is due to the well proximity effect that has not been taken into account in the process simulations. The WPE [114] affects implantation process steps depending on the thickness and characteristics of the photoresist, but also the wafer tilt. During the implantation step, ions are both reflected from and scattered inside the photoresist. As a result, regions close to the photoresist well will absorb a larger dose, resulting in a larger doping. Consequently, there is some room for profile modifications: The measured $\overline{C}_\mathrm{jCi}$ is used to adjust the internal collector, while the doping of the HV implant is adjusted to match f_t. A constant collector doping profile for the internal collector seems to match the capacitance best. As a result, the characteristics in fig. 4.13 are obtained. $\overline{Q}_\mathrm{p0} = 25.9\,\mathrm{fF}$ is obtained from the simulations, which is somewhat lower than the extracted value ($\overline{Q}_\mathrm{p0} = 28.8\,\mathrm{fF}$), but within the extraction accuracy. Note that no physical model changes were applied.

For all three transistor flavors, the onset of high-current effects is not taken into account correctly. As has been explained earlier, the link between $\overline{C}_\mathrm{jCi0}$ and ρ_Ci0 is one of the major complications for TCAD calibration and strongly depends on process variations and measurement accuracy. Even if the fall-off of f_t is captured (by compromising $\overline{C}_\mathrm{jCi}$), peak f_t cannot be matched very accurately. There is a variety of reasons to explain the discrepancy: *(i)* The physical models are not fully accurate (especially the HD parameters are not well known). *(ii)* The HD transport model itself is a simplification. *(iii)* There is a certain process variation or a measurement/extraction inaccuracy at peak f_t, as can be observed in fig. 4.11 (a). However, it would be unreasonable to tune physical parameters, as the direct cause for the discrepancy cannot be identified. Without evidence, a model change may degrade the predictive capabilities of the simulation setup and therefore, the physical models should not be tuned.

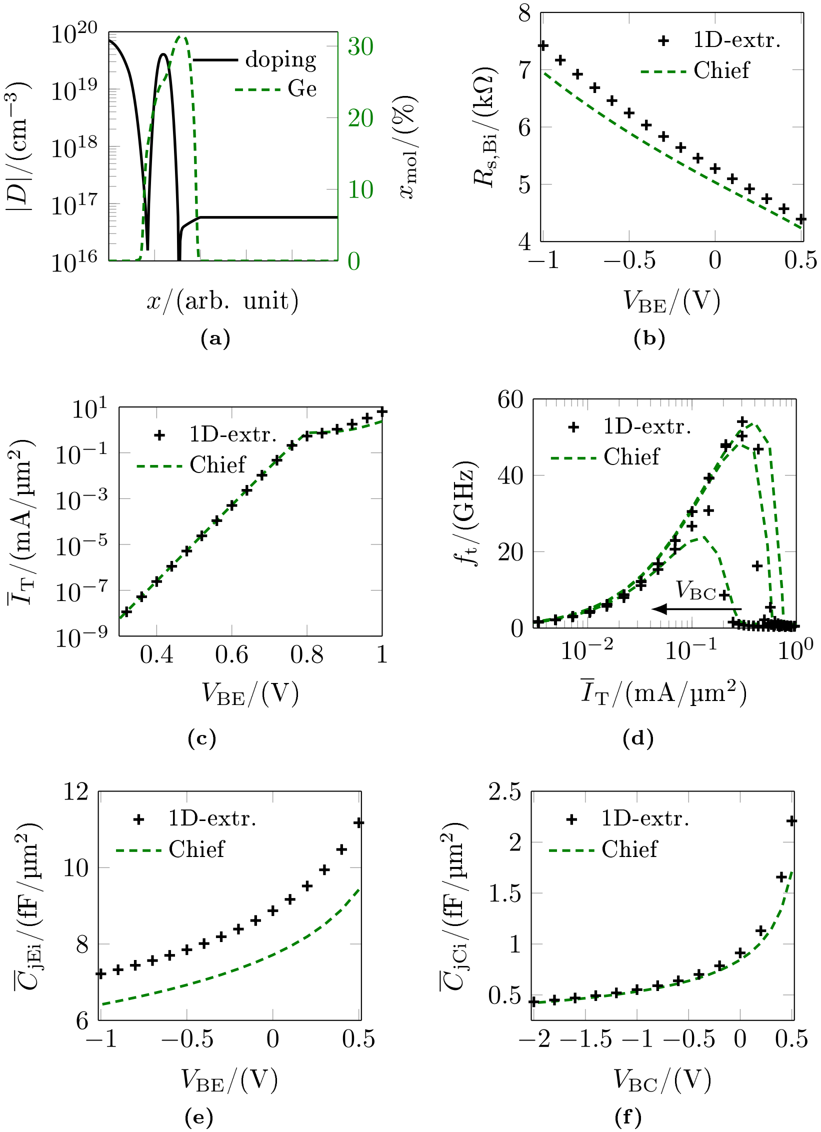


Figure 4.13: Final comparison of the extracted 1D reference with HD simulations for the HV transistors of [76]. The doping profile – incorporating a collector doping change – is illustrated in **(a)**. Results for **(b)** $R_{\mathrm{s,Bi}}$ vs. V_{BE} at $V_{\mathrm{CE}} = 0\,\mathrm{V}$, **(c)** $\overline{I}_{\mathrm{T}}$ vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$, **(d)** f_{t} vs. $\overline{I}_{\mathrm{T}}$ for $V_{\mathrm{BC}} = (-0.5, 0 \text{ and } 0.5)\,\mathrm{V}$, **(e)** $\overline{C}_{\mathrm{jEi}}$ vs. V_{BE} and **(f)** $\overline{C}_{\mathrm{jCi}}$ vs. V_{BC}.

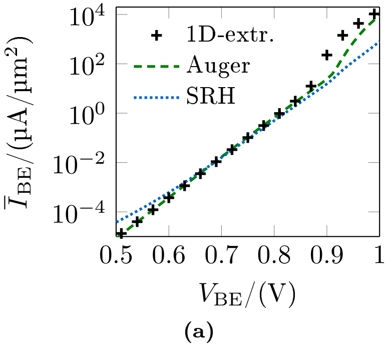
4.3 Base current calibration

The prediction of the base current is difficult because recombination processes strongly depend on the maturity of the process. During early process stages, the amount of traps in the transistor may be increased and the interface conditions may not be fully matured. Consequently, TCAD cannot predict I_B reliably. Nevertheless, to have an idea of how the base current could look like for similar processes, it can be useful to tune the physical models to match the extracted base current behavior of the analyzed process. Note that doing so is a fitting approach and hence, the result will only be applicable to similar processes. Also, a model for the recombination lifetimes for different alloy concentrations is missing and unfortunately, no reference data are available for model development.

The area component of the extracted base current from measurements for the HS transistors is about three times larger than $\overline{I}_\mathrm{BE}$ obtained from device simulations using the initial models. Consequently, it does not make sense to change the recombination velocity at the poly- to monosilicon interface, as adjusting it would only decrease the base current. By performing a parameter variation for the Auger and SRH recombination models, it is revealed that the SRH recombination plays an important role for the non-ideality factor of the current. To find out which parameter set to use, the Auger recombination parameters are adjusted for matching the base current at $V_\mathrm{BE} = 0.7\,\mathrm{V}$ while keeping the standard SRH parameters and vice versa (the relative change applied to the hole and electron parameters is assumed to be identical). As can be observed in fig. 4.14 (a), it is advised to tune the Auger coefficients for matching the slope of the base current. The corresponding parameters are listed in table 4.1.

parameter (unit)	$c_{n,\mathrm{Aug}}$ (cm^6/s)	$c_{p,\mathrm{Aug}}$ (cm^6/s)
value	$3.5 \cdot 10^{-29}$	$1.24 \cdot 10^{-29}$

Table 4.1: Parameter set of the Auger recombination adjusted for matching the base current $\overline{I}_\mathrm{BE}$ of the HS transistors (process of [76]).



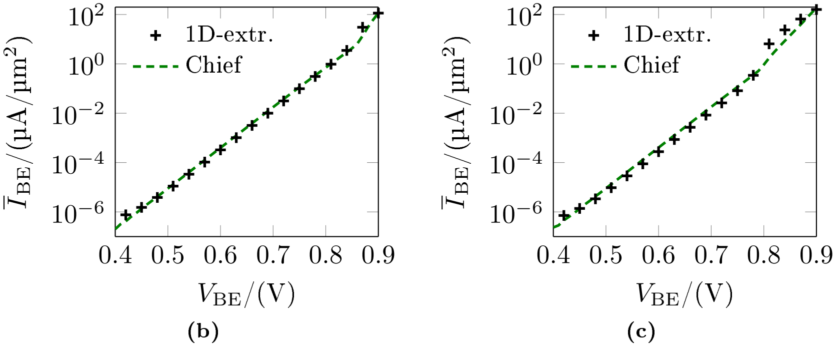
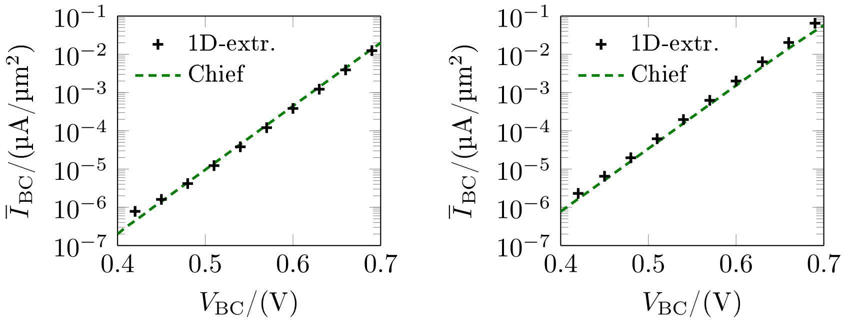


Figure 4.14: Comparison of the 1D reference data for $\overline{I}_{\mathrm{BE}}$ with HD simulations using different recombination models (HS transistors of [76]). **(a)** Plot of $\overline{I}_{\mathrm{BE}}$ vs. V_{BE} using either adjusted Auger or SRH recombination models. **(b)** and **(c)** compare reference and simulation of $\overline{I}_{\mathrm{BE}}$ vs. V_{BE} – using the adjusted Auger recombination model – for the MV and HV transistor versions, respectively.

Using the adjusted Auger recombination model, simulations for the MV and HV transistors are performed and compared with the 1D reference data for $\overline{I}_{\mathrm{BE}}$ and $\overline{I}_{\mathrm{BC}}$ (see figures 4.14 and 4.15). The adjusted model is also able to capture these characteristics accurately. Note that the extraction for the HS transistors lead to a negligible area component for I_{BC} and hence, no comparison is shown here.



(a) **(b)**

Figure 4.15: Comparison of the 1D reference data for $\overline{I}_{\mathrm{BC}}$ with HD simulations using the adjusted Auger recombination model (process of [76]). $\overline{I}_{\mathrm{BC}}$ vs. V_{BC} for **(a)** the MV and **(b)** the HV transistor flavor.

4.4 Impact ionization model calibration

Before starting the calibration of the avalanche parameters, reference data for all three transistor flavors need to be obtained. First, the avalanche current I_{avl} is separated from I_{B} based on forced V_{BE} measurements of different transistor geometries. To do so, I_{B} is plotted against V_{BC} for a fixed V_{BE} and the current close to $V_{\mathrm{BC}} = 0\,\mathrm{V}$ is fitted linearly to take neutral base recombination (NBR) into account (see fig. 4.16). The avalanche current is then calculated by

$$I_{\mathrm{avl}} = I_{\mathrm{B0}}\left[1 + m_{\mathrm{NBR}} V_{\mathrm{BC}}\right] - I_{\mathrm{B}}, \tag{4.3}$$

with the base current I_{B0} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$ and the slope of the linear interpolation m_{NBR}. Subsequently, the transfer current can be calculated according to

$$I_{\mathrm{T}} = I_{\mathrm{C}} - I_{\mathrm{avl}}. \tag{4.4}$$

By performing a PoA separation, the area related avalanche current $\overline{I}_{\mathrm{avla}}$ and transfer current $\overline{I}_{\mathrm{Ta}}$ can be determined and are then used to calculate the multiplication factor M_{a}:

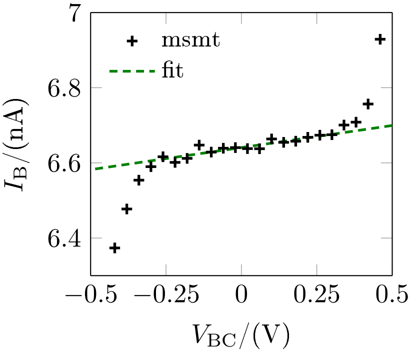


Figure 4.16: Separation of the base current from the impact ionization component based on measurements. I_B vs. V_BC at $V_\mathrm{BE} = 0.7\,\mathrm{V}$ for an exemplary HS transistor (process of [76]).

$$M_\mathrm{a} = 1 + \frac{\overline{I}_\mathrm{avla}}{\overline{I}_\mathrm{Ta}}. \tag{4.5}$$

The impact ionization (II) model for the HD transport (electrons) is based on an additional generation rate, mainly depending on the carrier temperature T_n and the amount of electrons:

$$G_{\mathrm{II},n} = \alpha_{\mathrm{II},n} n \exp\left(-\beta_{\mathrm{II},n} \frac{E_\mathrm{g}}{k_\mathrm{B} T_n}\right), \tag{4.6}$$

with the model parameters $\alpha_{\mathrm{II},n}$ and $\beta_{\mathrm{II},n}$. For holes, a corresponding DD model is used, which is based on the quasi-Fermi potential of holes φ_p and the amount of holes:

$$G_{\mathrm{II},p} = \alpha_{\mathrm{II},p} v_{\mathrm{sat},p} p \exp\left(-\frac{\beta_{\mathrm{II},p}}{\mathrm{grad}\left(\varphi_p\right)}\right), \tag{4.7}$$

with the model parameters $\alpha_{\mathrm{II},p}$ and $\beta_{\mathrm{II},p}$.

As has been observed in [122,123], the generation of holes plays an important role for breakdown, even in npn transistors: Due to the electron-hole pair generation caused by II, the amount of electrons and holes increases equally. When $I_\mathrm{avl} = I_\mathrm{T}$, the current caused by avalanche starts to dominate the transport and hence, the amount of holes has increased significantly. Conversely,

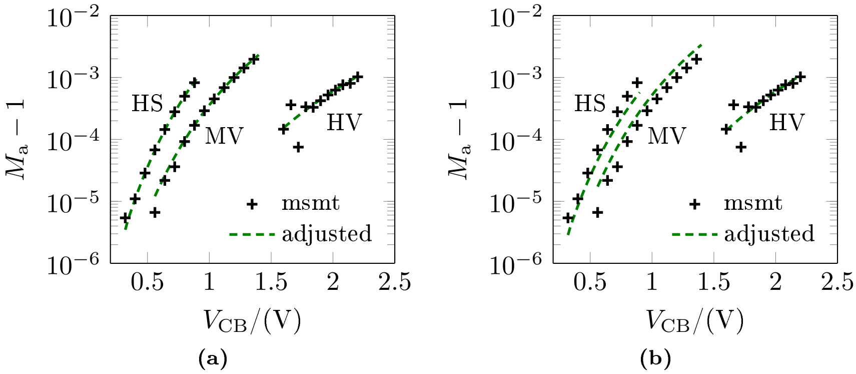
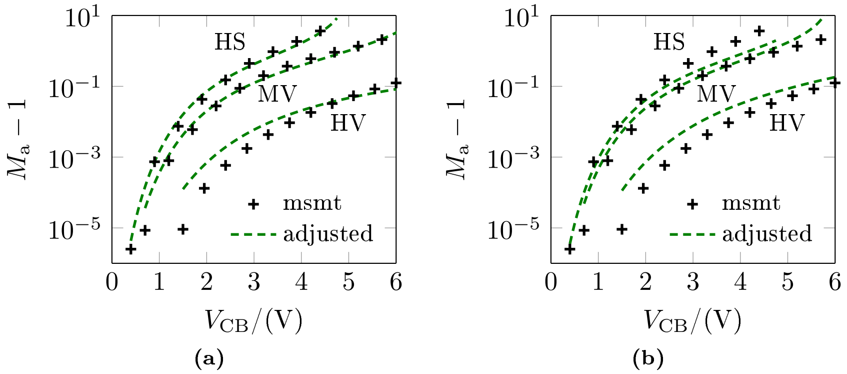


Figure 4.17: Comparison of the 1D reference data for $M_a - 1$ with HD simulations using adjusted impact ionization models for electrons (process of [76]). $M_a - 1$ vs. V_{CB} at $V_{BE} = 0.7\,V$ for all three transistor flavors using a separate parameter set for each transistor flavor **(a)** and a unified parameter set **(b)**.

for $M_a \approx 1$ the minority carrier transport in the base dominates and holes do not contribute as much as electrons.

Using the known 1D doping profiles, the parameters for the II model of electrons are tuned to match the data for $M_a - 1$ of all three transistor flavors. The result is illustrated in fig. 4.17 (a). For each flavor a separate set of parameters is obtained, which aligns well with the reference. It is known that the used avalanche generation models are a simplified approach for describing the actual physics behind II. As was shown by using MC simulations in [122], a "dead-space" inside the BC-SCR is forming, in which no II occurs. Such an effect is not taken into account by the considered models because they only rely on the carrier temperature inside of the device. Consequently, for a a unified parameter set, accuracy is compromised (see fig. 4.17 (b)). Also note that the measurement accuracy for the HV transistors was reduced, leading to bad scaling and noisy reference data.

Finally, the II parameters for holes are adjusted for measurement data with an extended V_{CB} range while keeping the previous adjustment for electrons. Unfortunately, these extended measurements are only available for a single device geometry and consequently, identical scaling – obtained from



(a) **(b)**

Figure 4.18: Comparison of the 1D reference data for $M_\mathrm{a} - 1$ with HD simulations using adjusted impact ionization models for both electrons and holes (process of [76]). $M_\mathrm{a} - 1$ vs. V_CB at $V_\mathrm{BE} = 0.6\,\mathrm{V}$ for all three transistor flavors using a separate parameter set for each transistor flavor **(a)** and a unified parameter set **(b)**.

parameter (unit)	$\alpha_{\mathrm{II},n}$ (1/ps)	$\beta_{\mathrm{II},n}$ (1)
value	65.9	3.49
parameter (unit)	$\alpha_{\mathrm{II},p}$ (1/cm)	$\beta_{\mathrm{II},p}$ (V/cm)
value	$8.84 \cdot 10^5$	$9.17 \cdot 10^5$

Table 4.2: Unified parameter set of the II models for electrons and holes, adjusted for matching the multiplication factor M_a of the HS, MV and HV transistors (process of [76]).

the previous PoA separation applied to the limited data range – had to be assumed. The result for $M_\mathrm{a} - 1$ using the adjusted parameters is displayed in fig. 4.18 and the parameters for the unified II model are listed in table 4.2. The obtained accuracy is acceptable although the predictive capabilities are limited due to the simple II model.

4.5 Attempting 2D doping profile calibration

Based on process simulations and the calibrated 1D doping profiles, analytical input profiles for DEVICE were created and are used to determine additional 2D parameters required for modeling the respective devices. In comparison to the 1D results, the following characteristics and parameters are added to the transistor:

- The peripheral BE junction capacitance and base current.
- The external BC junction capacitance and base current.
- The transfer current scaling modeled by the parameters γ_{C}, h_{jEip} and a_{hjEip}.
- Collector current spreading modeled by the current spreading angle δ_{C}.
- The transit time ratio $f_{\tau\mathrm{pi}}$, which describes the transit time scaling at low currents.

Also the internal and parts of the external base resistance are included by running 2D simulations. Nevertheless, it has been found in section 3.5 that a large portion of R_{Bx} is associated to the vertical resistance $\rho_{\mathrm{Bx,l0}}$ including the poly- to monosilicon interface, which cannot be predicted without atomistic simulations. Consequently, with the TCAD simulations employed in this work it is not possible to predict R_{Bx} without making assumptions. Although the exact value of $\rho_{\mathrm{Bx,l0}}$ is unknown (certain assumptions had to be made in section 3.5), adding it externally will be a reasonable estimation. Under these circumstances, tuning the diffusion of the polysilicon base for matching f_{max} would be a fit. The resulting doping profile would not correspond to actual fabricated silicon. Not only the base resistance but also the exact value of the peripheral BE junction capacitance is unknown. Both the measurement accuracy is low (see section 3.3) and the separation of the spacer capacitance and C_{jEp} is not exact, as the under-spacer doping is unknown. Consequently, for the 2D calibration only an attempt for adjusting the external BC junction doping to the measured characteristics is feasible. To match the measured γ_{C0}, the emitter doping diffusion may be tuned. Other doping profile regions need to remain at their initial process simulation result.

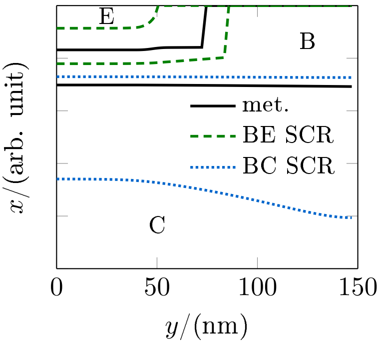


Figure 4.19: Metallurgical junctions and space charge region extensions at zero bias as obtained from the FRA for a HS transistor with an emitter width of $b_{\mathrm{E0}} = 98\,\mathrm{nm}$ (process of [76]). Only one half of the internal transistor (right hand side) is shown. The letters E, B and C indicate the respective transistor regions.

A possible – but cumbersome and time-consuming – way to extract the 2D parameters is to apply the methods described in chapter 3. Consequently, device simulations for different emitter widths can be conducted and the parameters are then obtained by PoA separation and scaling. Another option is to develop dedicated methods to determine the parameters based on single device simulations. The idea for doing so is based on [124], using the full regional approach (FRA). Applying the FRA to 2D simulation data is as simple as applying it to a 1D transistor slice repeatedly [125]. Exemplary for a FRA result, the zero-bias space charge region extensions are illustrated in fig. 4.19 for a HS transistor with an emitter width of $b_{\mathrm{E0}} = 98\,\mathrm{nm}$.

To determine the peripheral/external components from single device simulations is straightforward: The symmetry line at the middle of the emitter is used to determine the current and charges of the area component – corresponding to the 1D transistor. Multiplying them with the actual emitter width leads to area related (but now length specific) components, which are then subtracted from the total simulated quantities. For example, the area related transfer current density $\overline{I}_{\mathrm{Ta}}$ corresponds to the electron current density $\overline{I}_n$ at the end of the BC SCR $x_{\mathrm{jC,e}}$ in the collector at the symmetry line (where recombination and current spreading are negligible):

$$\overline{I}_{\mathrm{Ta}} = \overline{I}_{n}\left(x = x_{\mathrm{jC,e}}, y = 0\right). \tag{4.8}$$

The peripheral current I'_{Tp} is then obtained based on the total current:

$$I'_{\mathrm{Tp}} = \left(I'_{\mathrm{T}} - \overline{I}_{\mathrm{Ta}} b_{\mathrm{E0}}\right)/2. \tag{4.9}$$

Similarly, the idea can be applied to the BE and BC capacitances [125]. To assess if the method is working accurately, the results are compared with extraction on 2D simulations of different emitter widths and 1D simulations (see fig. 4.20). As can be observed, the accuracy is sufficient for waiving the time-consuming extraction step.

To determine $f_{\tau\mathrm{pi}}$ and δ_{C} from single 2D simulations is less straightforward. $f_{\tau\mathrm{pi}}$ describes the transit time ratio between the peripheral and area related τ_{f} components at low currents. Its meaning can be better understood by relating the transit frequency to quasi-static quantities for a simulated 2D internal HBT based on [74]:

$$\begin{aligned}\frac{1}{2\pi f_{\mathrm{t}}} &= \left.\frac{\partial Q'_{\mathrm{p}}}{\partial I'_{\mathrm{C}}}\right|_{V_{\mathrm{CE}}} \\ &= \left.\frac{\partial Q'_{\mathrm{p}}}{\partial V_{\mathrm{BE}}}\right|_{V_{\mathrm{CE}}} \underbrace{\left.\frac{\partial V_{\mathrm{BE}}}{\partial I'_{\mathrm{C}}}\right|_{V_{\mathrm{CE}}}}_{1/g'_{\mathrm{m}}} \\ &= \frac{1}{g'_{\mathrm{m}}} \int\!\!\int q \left.\frac{\partial p}{\partial V_{\mathrm{BE}}}\right|_{V_{\mathrm{CE}}} \mathrm{d}x\mathrm{d}y = \frac{C'_{\mathrm{p}}}{g'_{\mathrm{m}}}.\end{aligned} \tag{4.10}$$

Next, the total response of the charge C'_{p} caused by a voltage change and the transconductance g'_{m} are split up into their area and peripheral components according to transistor scaling:

$$\frac{1}{2\pi f_{\mathrm{t}}} = \frac{\overline{C}_{\mathrm{pa}} b_{\mathrm{E0}} + C'_{\mathrm{pp}}}{\overline{g}_{\mathrm{ma}} b_{\mathrm{E0}} + g'_{\mathrm{mp}}}. \tag{4.11}$$

The subscripts “a” and “p” indicate the area and peripheral components, respectively. Subsequently, the components of $\overline{C}_{\mathrm{pa}}$ and C'_{pp} are introduced to (4.11):

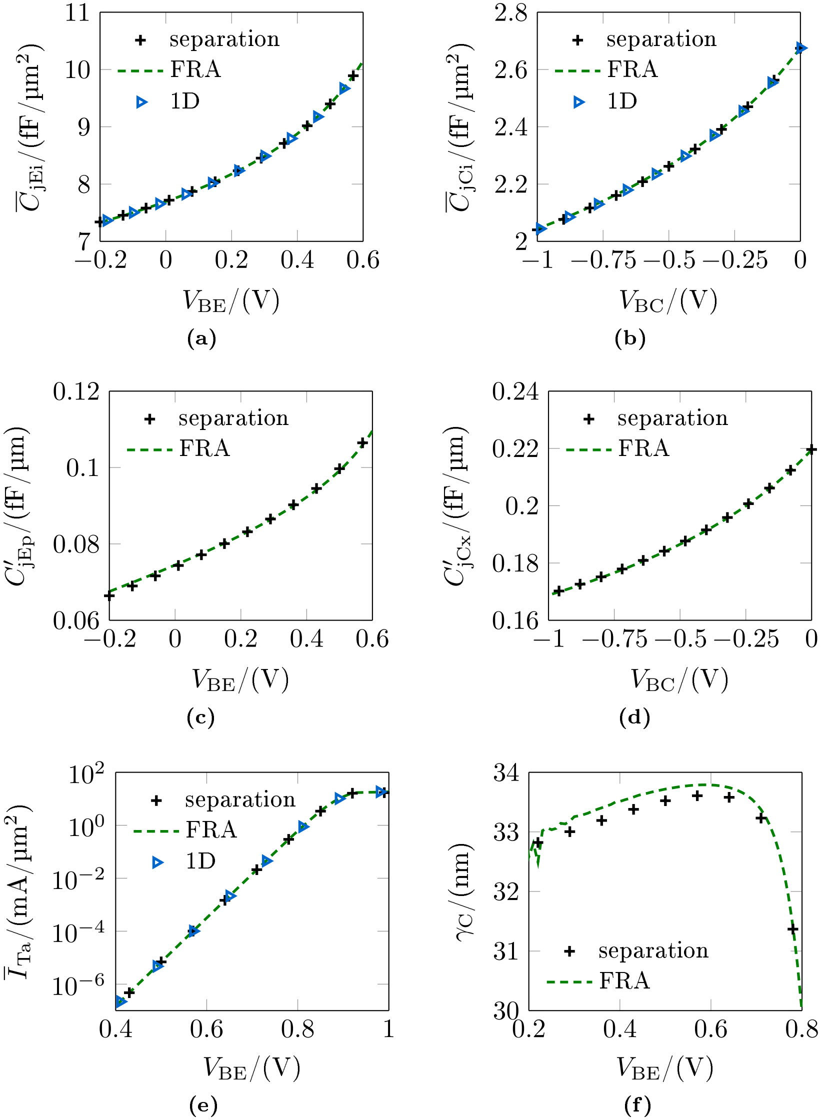


Figure 4.20: Comparison of methods for determining important 2D characteristics by means of PoA separation and single 2D simulation evaluations based on the FRA for an exemplary HS transistor with $b_{\mathrm{E0}} = 178\,\mathrm{nm}$ (process of [76]). Results for **(a)** $\overline{C}_{\mathrm{jEi}}$ vs. V_{BE}, **(b)** $\overline{C}_{\mathrm{jCi}}$ vs. V_{BC}, **(c)** C'_{jEp} vs. V_{BE}, **(d)** C'_{jCx} vs. V_{BC}, **(e)** $\overline{I}_{\mathrm{Ta}}$ vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$ and **(f)** γ_{C} vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$.

$$\frac{1}{2\pi f_{\mathrm{t}}} = \frac{\left(\overline{C}_{\mathrm{jEi}} + \overline{C}_{\mathrm{jCi}} + \tau_{\mathrm{fa}}\overline{g}_{\mathrm{ma}}\right) b_{\mathrm{E0}} + C'_{\mathrm{jEp}} + C'_{\mathrm{jCx}} + \tau_{\mathrm{fp}} g'_{\mathrm{mp}}}{\overline{g}_{\mathrm{ma}} b_{\mathrm{E0}} + g'_{\mathrm{mp}}}. \tag{4.12}$$

At low currents, the transit time consists of its bias independent portion only and hence, $\tau_{\mathrm{f}} \approx \tau_{\mathrm{f0}}$. Consequently, $f_{\tau\mathrm{pi}}$ is linked to f_t by

$$\frac{1}{2\pi f_{\mathrm{t}}} \approx \frac{\left(\overline{C}_{\mathrm{jEi}} + \overline{C}_{\mathrm{jCi}} + \tau_{\mathrm{f0a}}\,\overline{g}_{\mathrm{ma}}\right) b_{\mathrm{E0}} + C'_{\mathrm{jEp}} + C'_{\mathrm{jCx}} + f_{\tau\mathrm{pi}}\tau_{\mathrm{f0a}}\, g'_{\mathrm{mp}}}{\overline{g}_{\mathrm{ma}} b_{\mathrm{E0}} + g'_{\mathrm{mp}}}. \tag{4.13}$$

Even though τ_{f} and the minority transit time τ_{m} are known from the FRA, it is complicated to determine $f_{\tau\mathrm{pi}}$ without performing parameter extraction. This is because parts of τ_{f} behave like $C_{\mathrm{jE}}/g_{\mathrm{m}}$ and therefore need to be added to the junction capacitance. Consequently, the bias independent parts of τ_{f} at low injection – which are relevant for $f_{\tau\mathrm{pi}}$ – cannot be directly accessed from the FRA. Hence, the following equation for $f_{\tau\mathrm{pi}}$ is only an approximation:

$$f_{\tau\mathrm{pi}} \approx \frac{\tau_{\mathrm{mp}}}{\tau_{\mathrm{ma}}}. \tag{4.14}$$

Following the simple approach, fig. 4.21 is obtained. $f_{\tau\mathrm{pi}}$ can be read off the chart as the maximum value close before the peak of f_{t}. A deviation of about 6 % is achieved in comparison with the reference obtained by extraction on simulation data, which is within the limits of the extraction accuracy.

To assess the amount of collector current spreading, the collector current stream lines beginning from the emitter contact are plotted for low injection in fig. 4.22 and the current spreading angle δ_{C} is read off the plot by connecting the intersect of the dotted flow line with the metallurgical collector junction to the end of the internal collector (where there is no more current flow bending). For the example, $\delta_{\mathrm{C}} = 4.9\,^{\circ}$ is obtained, which is somewhat inaccurate in comparison with the reference value obtained from extraction on simulation data $\delta_{\mathrm{C}} = 1.3\,^{\circ}$. However, both the accuracy of the FRA-based approach and the standard extraction method are relatively low for δ_{C} (especially when there is nearly no current spreading) and hence, the accuracy of the FRA-

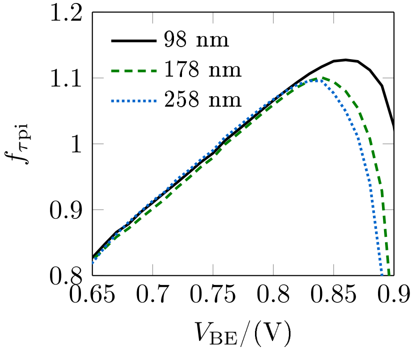


Figure 4.21: Result for determining $f_{\tau\mathrm{pi}}$ by means of single 2D simulation evaluations based on the FRA for exemplary HS transistors with $b_{\mathrm{E0}} = (98, 178 \text{ and } 258)\,\mathrm{nm}$ (process of [76]). Result for $f_{\tau\mathrm{pi}}$ vs. V_{BE}. The reference value obtained from extraction on simulation data is about 6 % larger.

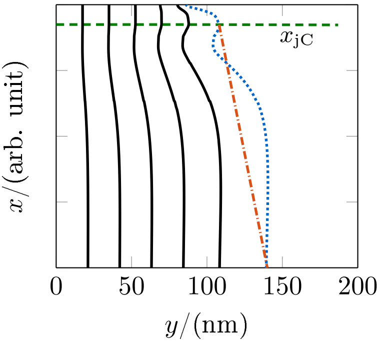


Figure 4.22: Result for the current stream lines of an exemplary HS transistor with $b_{\mathrm{E0}} = 178\,\mathrm{nm}$ at $V_{\mathrm{BE}} = 0.7\,\mathrm{V}$ and $V_{\mathrm{BC}} = 0\,\mathrm{V}$ (process of [76]). Only one half of the internal transistor (right hand side) is shown. The dotted current flow line can be used to determine the current spreading angle δ_{C} by connecting the intersect of the flow line with the metallurgical collector junction to the end of the internal collector – as illustrated by the dash-dotted line.

based method is sufficient for a fast profile adjustment approach.

Comparing the results for the 2D parameters of simulation and measurements for the HS transistors reveals that most parameters do not align well, as is shown in table 4.3. The same applies to the MV and HV transistor results in tables 4.4 and 4.5. This is due to several reasons: *(i)* The used process simulations were adjusted to match f_{max} by tuning the diffusion at the poly- to monosilicon interface (see [126]). As has been explained earlier, this can lead to a wrong peripheral base profile, which in turn can cause additional discrepancies. *(ii)* The lateral diffusion of the emitter doping profile is inaccurate, leading to a deviation for δ_{C} and C'_{jEp0}. *(iii)* As has been found in chapter 3, there are several indications for an increased external collector doping – again confirmed by the results for C'_{jCx0}, δ_{C} and $f_{\tau\mathrm{pi}}$.

For the profile calibration, the process simulation adjustments of [126] for the diffusion at the poly- to monosilicon interface of the base are undone. Next, the lateral diffusion of the emitter doping profile is adjusted to match γ_{C0}. In a final step, an additional collector doping is added to the internal BC periphery of the HS transistors for a better agreement with the measured external BC capacitance, $f_{\tau\mathrm{pi}}$ and current spreading. As detailed lateral doping profile information are unavailable, assumptions had to be made for the profile placement:

- The peak concentration of the profile is placed at the edge of the SIC implant window to account for the WPE.
- The falloff of the doping concentration in lateral direction is set not to influence the area related collector profile part.
- The peak concentration is optimized for agreement with C'_{jCx0}.

The SCR extension of the corresponding doping profile is compared to the initial version in fig. 4.23. As can be observed, the SCR extension of the periphery decreased to increase the corresponding capacitances. For the MV transistors, the lateral profile fall-off of the internal collector was changed to better match the reference for $f_{\tau\mathrm{pi}}$ and δ_{C}. Note that an adjustment for the HV transistors turned out to be unfeasible and not useful, as only insufficient information about the neutral collector is available. Subsequently, simulations

parameter (unit)	γ_{C0} (nm)	δ_{C} (°)	I'_{BEpS} (A/µm)	I'_{BCxS} (A/µm)
value (msmt)	23.3	19.8	$3.74 \cdot 10^{-22}$	$3.01 \cdot 10^{-19}$
value (sim.)	33.3	1.3 (4.9)	$1.86 \cdot 10^{-21}$	$8.93 \cdot 10^{-21}$
parameter (unit)	C'_{jEp0} (fF/µm)	C'_{jCx0} (fF/µm)	$f_{\tau\mathrm{pi}}$ (1)	
value (msmt)	0.215	0.343	1.00	
value (sim.)	0.074	0.220	1.18 (1.11)	

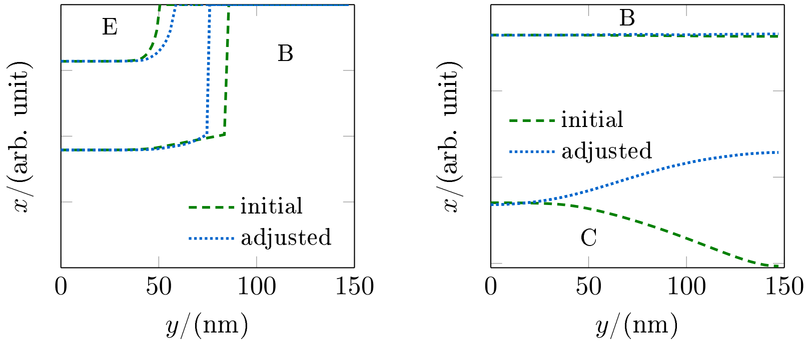
Table 4.3: Initial results for important 2D parameters obtained by extraction on simulations and measurements for the HS transistors of [76]. Values in brackets list results of the FRA-based methods.

parameter (unit)	γ_{C0} (nm)	δ_{C} (°)	I'_{BEpS} (A/µm)	I'_{BCxS} (A/µm)
value (msmt)	26.9	5.4	$3.00 \cdot 10^{-21}$	$2.20 \cdot 10^{-19}$
value (sim.)	33.5	8.2 (8.7)	$1.91 \cdot 10^{-21}$	$9.02 \cdot 10^{-21}$
parameter (unit)	C'_{jEp0} (fF/µm)	C'_{jCx0} (fF/µm)	$f_{\tau\mathrm{pi}}$ (1)	
value (msmt)	0.215	0.182	1.23	
value (sim.)	0.074	0.138	1.02 (1.04)	

Table 4.4: Initial results for important 2D parameters obtained by extraction on simulations and measurements for the MV transistors of [76]. Values in brackets list results of the FRA-based methods.

parameter (unit)	γ_{C0} (nm)	δ_{C} (°)	I'_{BEpS} (A/µm)	I'_{BCxS} (A/µm)
value (msmt)	30.3	31.9	$2.50 \cdot 10^{-21}$	$2.44 \cdot 10^{-19}$
value (sim.)	33.3	10.3 (9.9)	$1.92 \cdot 10^{-21}$	$2.36 \cdot 10^{-20}$
parameter (unit)	C'_{jEp0} (fF/µm)	C'_{jCx0} (fF/µm)	$f_{\tau\mathrm{pi}}$ (1)	
value (msmt)	0.215	0.117	1.25	
value (sim.)	0.074	0.083	0.96 (1.02)	

Table 4.5: Initial results for important 2D parameters obtained by extraction on simulations and measurements for the HV transistors of [76]. Values in brackets list results of the FRA-based methods.



(a) **(b)**

Figure 4.23: Comparison of the initial and adjusted 2D doping profile. **(a)** BE and **(b)** BC space charge region extensions at zero bias as obtained from the FRA for a HS transistor with an emitter width of $b_{\mathrm{E0}} = 98\,\mathrm{nm}$ (process of [76]). Only one half of the internal transistor (right hand side) is shown. The letters E, B and C indicate the respective transistor regions.

are performed and the extraction is redone for an updated comparison with the reference. Tables 4.6, 4.7 and 4.8 summarize the results for the HS, MV and HV transistor versions, respectively.

As is illustrated by the results, the agreement with the reference is reasonable and demonstrates again that TCAD can reproduce measured characteristics of actual devices. Nevertheless, the accuracy strongly depends on the used lateral profiles and unfortunately, there are only few methods that allow their determination [127]. Even worse, their accuracy is too low for relevant doping concentrations and hence, they are only applicable to alloy concentrations (for example the germanium concentration of the base). This means that 2D TCAD has to rely on process simulations and additional manual profile adjustments.

parameter (unit)	γ_{C0} (nm)	δ_{C} (°)	I'_{BEpS} (A/µm)	I'_{BCxS} (A/µm)
value (msmt)	23.3	19.8	$3.74 \cdot 10^{-22}$	$3.01 \cdot 10^{-19}$
value (sim.)	26.9	8.2	$1.43 \cdot 10^{-21}$	$9.77 \cdot 10^{-21}$
parameter (unit)	C'_{jEp0} (fF/µm)	C'_{jCx0} (fF/µm)	$f_{\tau\mathrm{pi}}$ (1)	
value (msmt)	0.215	0.343	1.00	
value (sim.)	0.134	0.344	0.95	

Table 4.6: Final results for important 2D parameters obtained by extraction on simulations and measurements for the HS transistors of [76].

parameter (unit)	γ_{C0} (nm)	δ_{C} (°)	I'_{BEpS} (A/µm)	I'_{BCxS} (A/µm)
value (msmt)	26.9	5.4	$3.00 \cdot 10^{-21}$	$2.20 \cdot 10^{-19}$
value (sim.)	26.9	4.3	$1.50 \cdot 10^{-21}$	$9.45 \cdot 10^{-21}$
parameter (unit)	C'_{jEp0} (fF/µm)	C'_{jCx0} (fF/µm)	$f_{\tau\mathrm{pi}}$ (1)	
value (msmt)	0.215	0.182	1.23	
value (sim.)	0.134	0.114	1.16	

Table 4.7: Final results for important 2D parameters obtained by extraction on simulations and measurements for the MV transistors of [76].

parameter (unit)	γ_{C0} (nm)	δ_{C} (°)	I'_{BEpS} (A/µm)	I'_{BCxS} (A/µm)
value (msmt)	30.3	31.9	$2.50 \cdot 10^{-21}$	$2.44 \cdot 10^{-19}$
value (sim.)	26.8	10.3	$1.50 \cdot 10^{-21}$	$2.35 \cdot 10^{-20}$
parameter (unit)	C'_{jEp0} (fF/µm)	C'_{jCx0} (fF/µm)	$f_{\tau\mathrm{pi}}$ (1)	
value (msmt)	0.215	0.117	1.25	
value (sim.)	0.134	0.083	0.88	

Table 4.8: Final results for important 2D parameters obtained by extraction on simulations and measurements for the HV transistors of [76].

4.6 TCAD calibration outlook

As has been observed in the previous sections of chapter 4, doping profiles play a very important role for a successful TCAD setup. It turned out that process simulations are not reliable and hence, additional methods were applied for retrieving profile information. On the other hand, it needs to be pointed out that without process TCAD, no quantitative link to the actual process implementation is possible. Fixing the process simulation setup is beyond the scope of this work and would require an additional thesis project. In addition to this important and time-consuming task, there is room for improvement by implementing the following enhancements:

- Due to the large noise level for the measured base emitter capacitance (see fig. 3.16), the methods of section 4.1 for optimizing the doping of the BE space charge region could not be applied. The reason for the noise was identified to be linked with the measured common emitter configuration transistors (see fig. 3.18). By fabricating common collector test structures, reliable data for C_{jEi} could be obtained for creating a more comprehensive doping profile view.

- Although the predictions will be carried out at room temperature, an attempt to calibrate the temperature behavior should be performed based on the extracted compact model for taking the impact of self-heating on the characteristics into account correctly.

- The base resistance model was built on tetrode measurements of an earlier process stage. It is recommended to revise the model for R_{B} based on updated data and to also apply other extraction methods for verification. Doing so would help to improve the agreement for the transfer current at medium-high injection and the f_{max} characteristic before its peak value (especially for the HS transistors).

CHAPTER 5

Performance prediction of SiGe HBTs

The previous methods and approaches of chapter 4 – in conjunction with some extensions – can be applied for predicting the performance of SiGe HBTs. After explaining the fundamentals of the prediction approach in the beginning of the chapter, the expected accuracy of the heterogeneous method is demonstrated by comparing the results with actual measurement data of different device sizes for the technology of [76]. Subsequently, the scheme is also applied to a fictitious technology in 28 nm for which no reference data exist yet. Based on the results, the approximate performance of the future technology is summarized.

5.1 A heterogeneous prediction approach

The goal of the prediction approach is to obtain specific model parameters for HICUM that describe the process under investigation sufficiently accurate to replace the TCAD-based simulations. A major advantage is that circuit simulations can be conducted by using the respective modelcards aiding early circuit designs for the technology. In the beginning of the considerations, the 1D transistor – which describes the main transport of a SiGe HBT – is characterized. By performing simulations, data are obtained for all rele-

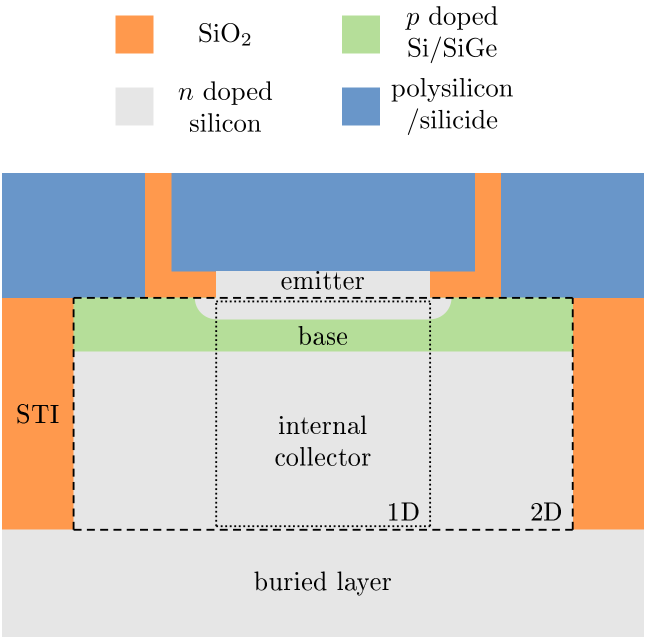


Figure 5.1: Cross section to illustrate the transistor regions covered by 1D and 2D simulations. External regions outside the 2D box are taken into account with additional dedicated simulations and approaches of the heterogeneous methodology.

vant characteristics of the 1D structure. Subsequently, extraction is applied to the data and the respective compact model parameters are added to the modelcard. Applying the same approach to the full intrinsic transistor region allows to obtain the parameters for the 2D characterization. The transistor cross section containing the respective regions is illustrated in fig. 5.1. Finally, external components are added to the parameter set of the technology:

- The BE and BC spacer capacitances are determined with the help of Laplace simulations assuming the geometry and materials of the technology under investigation.
- The external base and collector resistance are calculated based on quasi-3D simulations (see section 3.4) using sheet resistances from device simulation and assumed process specific values for regions that cannot be

sufficiently described with the simulation tools (e.g. contact resistances).

- For the substrate network only the isolation capacitance (either trench or junction isolation) is taken into account. The corresponding model is obtained by 1D simulation and calculations.
- The thermal resistance is calculated by means of 3D thermal simulations for which the geometry and materials of the structure need to be known.

The approach allows for combining different TCAD tools and their unique features employing extraction (see chapter 3 for corresponding methods), an accurate compact model (e.g. HICUM [74]) and scaling. At the end of the procedure, a modelcard is available for conducting simulations with an arbitrary circuit simulator and the FoMs of the technology can be determined. The determination sequence for the extraction is illustrated in fig. 5.2.

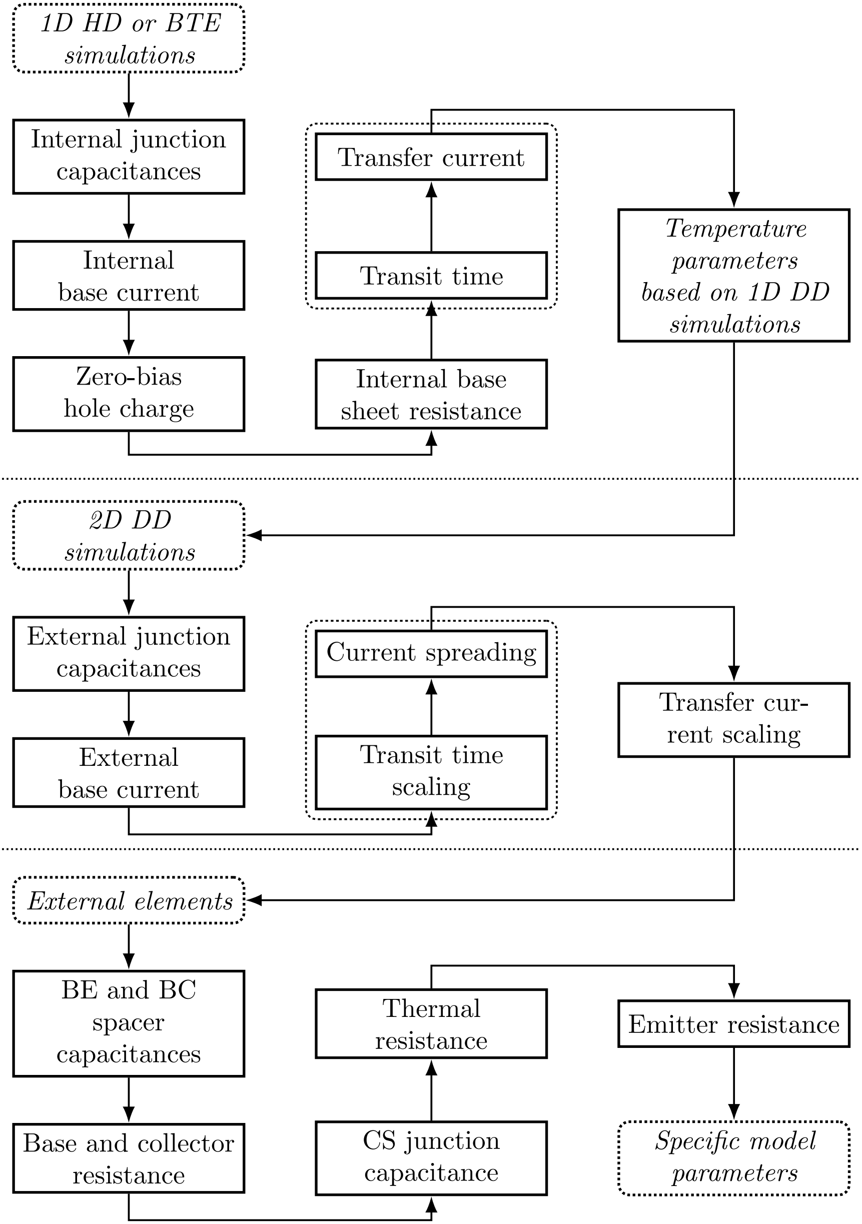


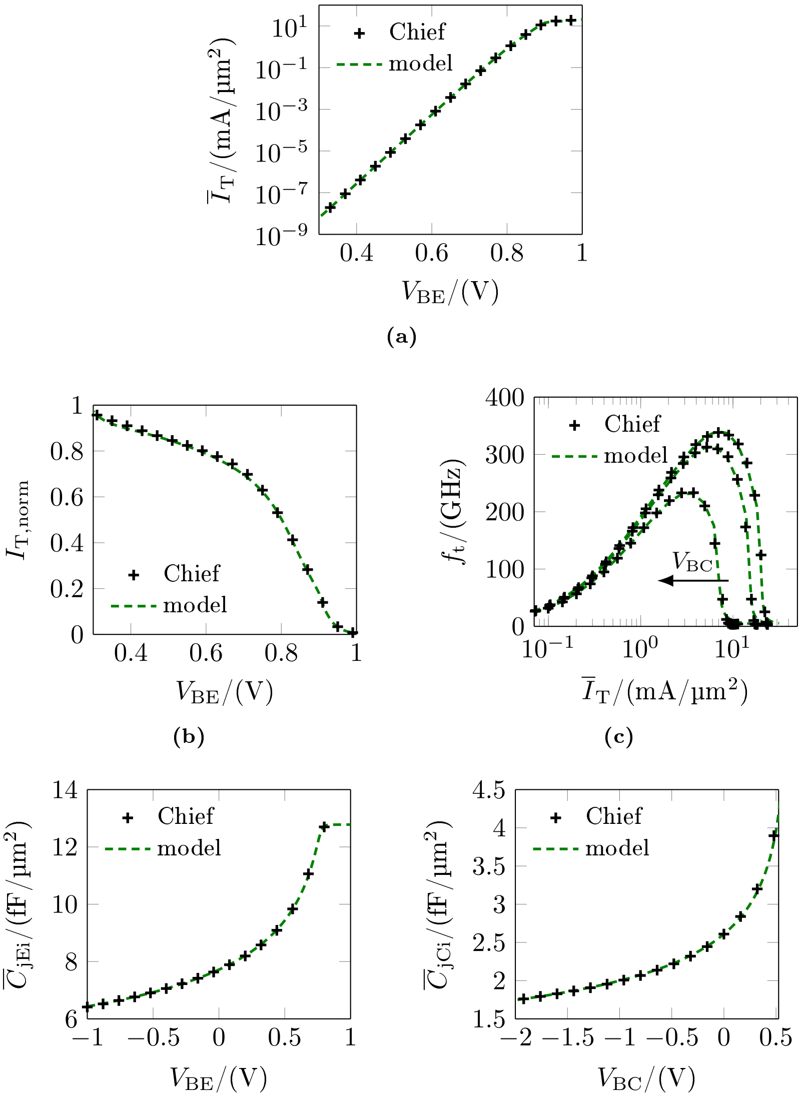
Figure 5.2: Proposed workflow of the extraction on TCAD data. Solid boxes illustrate a single extraction step of the strategy. An additional frame (dotted) depicts a coupling between two subsequent sections.

5.2 Case study for an advanced SiGe HBT technology

To demonstrate the prediction flow in detail and to get a picture of the accuracy that can be expected from a TCAD based prediction, the strategy in fig. 5.2 is exercised for the technology of [76]. At first, the parameters for the internal junction capacitances and the base current are extracted based on the simulation data and the corresponding HICUM model equations. Subsequently, the zero-bias hole charge and base sheet resistance are calculated according to (3.32) and (3.33), respectively. Finally, the transit time and transfer current extraction is conducted based on the extraction methods of sections 3.10 and 3.11. The 1D model is then compared to the simulation results: As can be observed in fig. 5.3, the accuracy of the compact model is sufficient to capture the presented figures of merit correctly. That means, instead of conducting device simulations, it suffices to run circuit simulations with the compact model.

The next step focuses on extracting the temperature parameters. As Chief does not permit to run simulations for different lattice temperatures, all simulations are performed using DEVICE. Consequently, the full extraction needs to be run again for the DD data – although only the temperature parameters are added to the modelcard of the prediction approach, whereas the electrical description is discarded. Performing simulations at various lattice temperatures allows for the extraction of the temperature parameters. Finally, the model is compared to the simulation results of the HS transistor flavor in fig. 5.4. The comparison for the MV and HV transistors can be found in appendix C.1 together with the extracted parameters for all three transistor flavors.

Most of the parameters of the final modelcard relate to 1D transport: Of the total 61 parameters required for modeling the internal transistor, only 15 are required to characterize the 2D impact. The additional prediction steps for the external/peripheral transistor were already carried out in section 4.5 and the required parameters are added from tables 4.6, 4.7 and 4.8 to the respective modelcards.



(a)

(b) **(c)**

(d) **(e)**

Figure 5.3: Comparison of HD simulations for the 1D profile with the corresponding extracted model based on HICUM for the HS transistors of [76]. Results for **(a)** $\overline{I}_{\mathrm{T}}$ vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$, **(b)** $I_{\mathrm{T,norm}}$ vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$, **(c)** f_{t} vs. $\overline{I}_{\mathrm{T}}$ for $V_{\mathrm{BC}} = (-0.5, 0 \text{ and } 0.5)\,\mathrm{V}$, **(d)** $\overline{C}_{\mathrm{jEi}}$ vs. V_{BE} and **(e)** $\overline{C}_{\mathrm{jCi}}$ vs. V_{BC}.

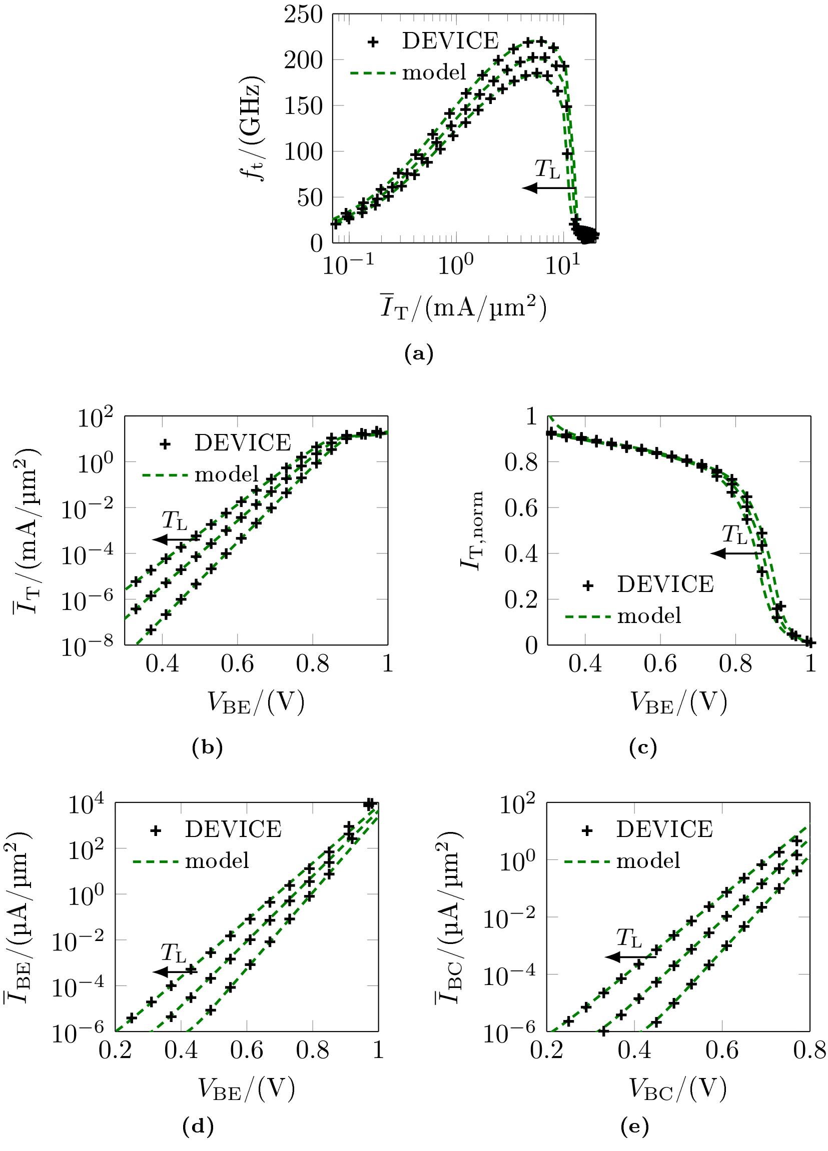


Figure 5.4: Comparison of DD simulations for the 1D profile with the corresponding extracted model based on HICUM for the HS transistors of [76] at $V_{BC} = 0\,\mathrm{V}$. Results for **(a)** f_t vs. $\overline{I}_T$, **(b)** $\overline{I}_T$ vs. V_{BE}, **(c)** $I_{T,norm}$ vs. V_{BE}, **(d)** $\overline{I}_{BE}$ vs. V_{BE} and **(e)** $\overline{I}_{BC}$ vs. V_{BC} for different lattice temperatures ($T_L = (300, 350 \text{ and } 400)\,\mathrm{K}$).

Following section 5.1, the BE and BC spacer capacitances need to be determined next based on Laplace simulations. The spacer results must be identical with the evaluations of section 3.2 and the respective values for $C'_{\mathrm{BE,par}}$ and $C'_{\mathrm{BC,par}}$ are added to the modelcard.

5.2.1 External resistances

The buried layer sheet resistance $R_{\mathrm{s,bl}}$ – which is required for determining the external collector resistance R_{Cx} – can be calculated based on the buried layer doping N_{bl} and electron mobility within the vertical limits $x_{\mathrm{bl,s}}$ and $x_{\mathrm{bl,e}}$ of the layer:

$$1/R_{\mathrm{s,bl}} = q \int_{x_{\mathrm{bl,s}}}^{x_{\mathrm{bl,e}}} N_{\mathrm{bl}}(x)\, \mu_n(x)\, \mathrm{d}x. \tag{5.1}$$

The approach leads to $R_{\mathrm{s,bl}} = 26.6\,\Omega/\square$ for the HS and MV transistors – aligning well with the extracted reference of $R_{\mathrm{s,bl}} = 30.7\,\Omega/\square$. For the HV flavor, $R_{\mathrm{s,bl}} = 434\,\Omega/\square$ is obtained.

The sheet resistance equation is not applicable to the sinker stack, as the current flow is perpendicular to the resistive layer (the sinker resistance is a contact resistance). Starting from the conductivity definition

$$\kappa = qn\mu_n \tag{5.2}$$

and the infinitesimal resistance of a cuboid with the cross-section area A and length $\mathrm{d}x$

$$\mathrm{d}R = \frac{1}{\kappa}\frac{\mathrm{d}x}{A}, \tag{5.3}$$

the monosilicon portion of the sinker resistance $R_{\mathrm{sk,mono}}$ can be calculated. Integrating $\mathrm{d}R$ over the sinker depth x and inserting the sinker doping $N_{\mathrm{sk}}(x)$ leads to

$$R_{\mathrm{sk,mono}} = \frac{1}{qA} \int_0^{l_{\mathrm{sk}}} \frac{1}{N_{\mathrm{sk}}(x)\, \mu_n(x)} \mathrm{d}x. \tag{5.4}$$

Note that the contact resistance $\rho_{\mathrm{sk,mono}} = R_{\mathrm{sk,mono}}A$ does not depend on the cross-section area. The approach leads to $\rho_{\mathrm{sk,mono}} = 10.6\,\Omega\,\mu\mathrm{m}^2$ for the HS and MV transistors. For the HV flavor, $\rho_{\mathrm{sk,mono}} = 88.0\,\Omega\,\mu\mathrm{m}^2$ is obtained. The values are somewhat lower than the extracted contact resistance of the test structures because the via portion and the interface resistances are not included in the result. As has been mentioned in the beginning of section 4.5, polysilicon, contact and interface resistances cannot be predicted and hence, need to be estimated. As a result, the remaining portion of the sinker stack is calculated by

$$\rho_{\mathrm{sk,int}} = \rho_{\mathrm{sk,meas,HS}} - \rho_{\mathrm{sk,mono}} = 7.5\,\Omega\,\mu\mathrm{m}^2, \tag{5.5}$$

which then also compensates for doping and model uncertainties. To obtain the final value for R_{Cx} required for each individual modelcard, quasi-3D simulations are run for the relevant transistor geometries assuming $\rho_{\mathrm{sk}} = \rho_{\mathrm{sk,mono}} + \rho_{\mathrm{sk,int}}$. The results are added to the existing table in appendix A.1, which originally focused on the measurement based evaluations only.

A reliable base resistance determination is complex, as the assumed model relies on certain assumptions (see section 3.5). For the TCAD approach, tetrode-like structures are simulated to determine the monosilicon contribution $R_{\mathrm{Bx,mono}}$: By applying the voltage $\mathit{\Delta} V_{\mathrm{BB}}$ between the base contacts of the CBEBC transistor, the interjacent resistance R_{B1B2} is calculated using the current I_{B} of one of the base contacts. R_{B1B2} consists of the internal and external monosilicon portion according to

$$\begin{aligned} R_{\mathrm{B1B2}} &= \frac{\mathit{\Delta} V_{\mathrm{BB}}}{I_{\mathrm{B}}} \\ R_{\mathrm{B1B2}} &= R_{\mathrm{Bi}} + 2R_{\mathrm{Bx,mono}} \\ &= R_{\mathrm{s,Bi}} \frac{b_{\mathrm{E0}}}{\Delta l_{\mathrm{z}}} + 2R_{\mathrm{Bx,mono}}, \end{aligned} \tag{5.6}$$

with the simulation dimension in z direction $\Delta l_{\mathrm{z}} = 1\,\mu\mathrm{m}$. Rearranging the equation allows for determining $R_{\mathrm{Bx,mono}}$, which is also defined by

$$\Delta l_{\mathrm{z}} R_{\mathrm{Bx,mono}} = R_{\mathrm{s,Bx,lv}} \gamma_{\mathrm{C0}} + R_{\mathrm{s,Bx,l0}} \left(b_{\mathrm{s}} + b_{\mathrm{so}} - \gamma_{\mathrm{C0}}\right) + \frac{\rho_{\mathrm{Bx,l0,mono}}}{b_{\mathrm{pm}}}. \tag{5.7}$$

parameter (HS) (unit)	$R_{\mathrm{s,Bx,lv0}}$ ($\Omega/\square$)	$R_{\mathrm{s,Bx,l0}}$ ($\Omega/\square$)	$\rho_{\mathrm{Bx,l0,mono}}$ ($\Omega\,\mu\mathrm{m}^2$)
value	5073	1339	1.55
parameter (MV) (unit)	$R_{\mathrm{s,Bx,lv0}}$ ($\Omega/\square$)	$R_{\mathrm{s,Bx,l0}}$ ($\Omega/\square$)	$\rho_{\mathrm{Bx,l0,mono}}$ ($\Omega\,\mu\mathrm{m}^2$)
value	4253	1243	1.24
parameter (HV) (unit)	$R_{\mathrm{s,Bx,lv0}}$ ($\Omega/\square$)	$R_{\mathrm{s,Bx,l0}}$ ($\Omega/\square$)	$\rho_{\mathrm{Bx,l0,mono}}$ ($\Omega\,\mu\mathrm{m}^2$)
value	4161	1201	1.44
parameter (generic) (unit)	$R_{\mathrm{s,po}}{}^*$ ($\Omega/\square$)	$R_{\mathrm{s,sil}}{}^*$ ($\Omega/\square$)	
value	710	15	

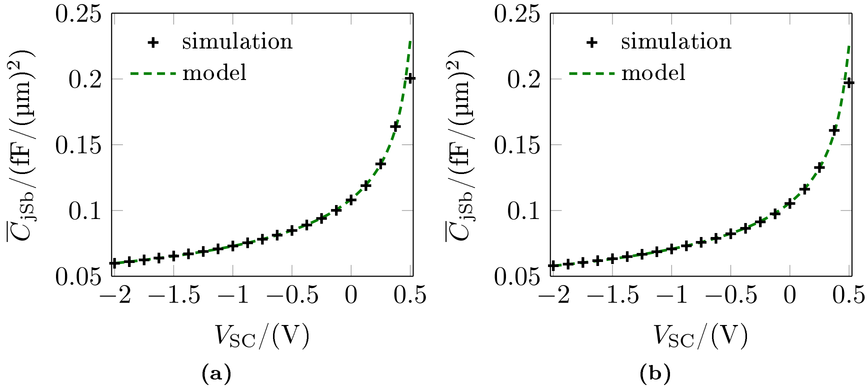
*Assumed values based on process information.

Table 5.1: Technology parameters of the base resistance description based on TCAD simulations for all three transistor flavors.

$R_{\mathrm{s,Bx,lv}}$ and $R_{\mathrm{s,Bx,l0}}$ are determined by calculating the spatial average of the sheet resistance for the respective regions beneath the BE spacer (adapting (5.1)). The vertical mono resistance $\rho_{\mathrm{Bx,l0,mono}}$ is then obtained by rearranging (5.7). The results in table 5.1 illustrate that $\rho_{\mathrm{Bx,l0,mono}}$ only covers a small part of the total value for $\rho_{\mathrm{Bx,l0}}$ obtained from measurements and consequently, the remaining interface portion is estimated:

$$\rho_{\mathrm{Bx,l0,int}} = \rho_{\mathrm{Bx,l0}} - \rho_{\mathrm{Bx,l0,mono}} = 6.89\,\Omega\,\mu\mathrm{m}^2. \tag{5.8}$$

To obtain the final value for R_{Bx} required for each individual modelcard, quasi-3D simulations are run for the relevant transistor geometries assuming $\rho_{\mathrm{Bx,l0}} = \rho_{\mathrm{Bx,l0,mono}} + \rho_{\mathrm{Bx,l0,int}}$. The results are added to the existing tables in appendix A.2, which originally focused on the measurement based evaluations only.



(a)

(b)

Figure 5.5: Comparison of 1D device simulations (markers) and model (lines) for the bottom component $\overline{C}_{\mathrm{jSb}}$ of the CS junction capacitance (process of [76]). Results for the HS/MV transistor flavors **(a)** and HV transistors **(b)**.

5.2.2 Collector substrate junction capacitance

To take the CS junction capacitance into account for the prediction approach, the bottom component $\overline{C}_{\mathrm{jSb}}$ is calculated based on 1D simulations using the full regional approach. Assuming a substrate doping of $N_{\mathrm{sub}} = 1 \cdot 10^{-15}\,\mathrm{cm}^{-3}$ and the buried layer doping profile of process TCAD leads to $\overline{C}_{\mathrm{jSb0}} = 0.089\,\mathrm{fF}/\mu\mathrm{m}^2$ for the HS/MV transistors, which is somewhat lower than the extracted value. As the substrate doping is much lower than the doping of the buried layer, the capacitance is determined by the substrate doping level mainly. Increasing N_{sub} to $1.5 \cdot 10^{-15}\,\mathrm{cm}^{-3}$ allows to reproduce the measurement based value for $\overline{C}_{\mathrm{jSb0}}$ accurately. The simulation result and the corresponding extracted model are shown in fig. 5.5 for different bias.

The DTI portion C'_{jSp} of the capacitance is calculated according to the simple parallel plate capacitance equation. Applying (3.9) to the DTI geometry and assuming the permittivity of silicon oxide leads to $C'_{\mathrm{jSp}} = 0.384\,\mathrm{fF}/\mu\mathrm{m}$. The relevant model parameters are summarized in table 5.2.

parameter (HS/MV) (unit)	$\overline{C}_{\mathrm{jSb0}}$ (fF/µm^2)	z_{Sb} (1)	V_{DSb} (V)
value	0.109	0.41	0.60
parameter (HV) (unit)	**$\overline{C}_{\mathrm{jSb0}}$ (fF/µm^2)**	**z_{Sb} (1)**	**V_{DSb} (V)**
value	0.106	0.41	0.60

Table 5.2: Extracted parameters for $\overline{C}_{\mathrm{jSb}}$ of the capacitance description of HICUM based on 1D device simulation data for the HS/MV and HV transistor flavors.

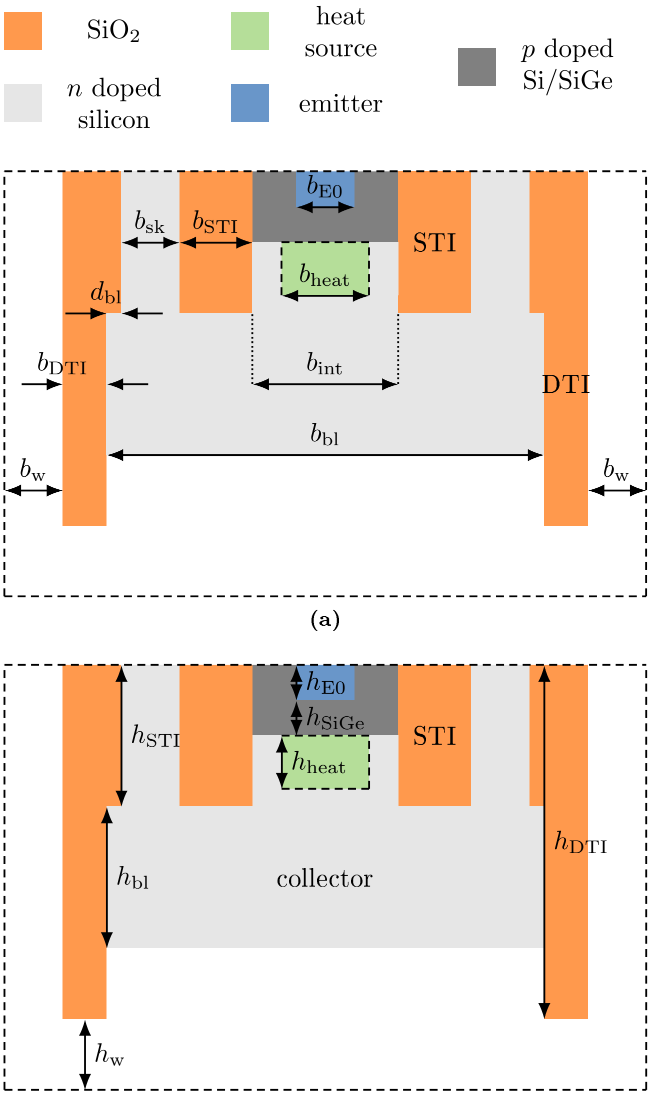
5.2.3 Thermal resistance

The thermal resistance R_{th} can be calculated with the help of the heat flow equation solver THERMO [128]. For the calculation, the transistor cross section of fig. 5.6 is used to build up an appropriate input file for conducting the simulations. The largest portion of heat is dissipated within the active BC SCR and hence, the heat source is placed accordingly after the metallurgical collector junction at the symmetry line of the transistor. Its width can be estimated by

$$b_{\mathrm{heat}} = b_{\mathrm{E0}} + 2\gamma_{\mathrm{C0}}, \tag{5.9}$$

whereas the height directly corresponds to the vertical SCR extension into the collector region, which can be determined by device simulations (see e.g. fig. 4.23). All other dimensions can be obtained by TEM pictures or process simulations in case of a fictitious technology. As the impact of thermal spreading is important, it is necessary to run full 3D simulations with the additional lateral dimensions from the respective transistor layout. For each part of the transistor, a material and doping dependent – but temperature independent – thermal conductivity is specified based on [129] (see table 5.3).

For the correct determination of R_{th}, the environment of the chip/wafer needs to be taken into account (heat sink, flip chip, etc.). During the measurements of the transistor characterization, the wafer is placed on a thermo chuck, which regulates the wafer temperature. Consequently, the heat drain



(a)

(b)

Figure 5.6: Cross section of the structure used to conduct thermal simulations. Geometry schematic with **(a)** lateral and **(b)** vertical dimensions. The dashed enclosure illustrates the considered simulation region.

$\kappa_{\mathrm{th}}/\,(\mathrm{W}/(\mathrm{m\,K}))$	internal C (HS)	internal C (MV)	internal C (HV)	oxide
value	118	129	147	1.4
$\kappa_{\mathrm{th}}/\,(\mathrm{W}/(\mathrm{m\,K}))$	buried layer (HS/MV)	buried layer (HV)	base	
value	82	146	102	
$\kappa_{\mathrm{th}}/\,(\mathrm{W}/(\mathrm{m\,K}))$	substrate	sinker	SiGe layer	emitter
value	148	75.5	13.6	93.9

Table 5.3: Thermal conductivity based on [129] used in the heat flow simulations (process of [76]).

of the simulations must be placed at the bottom of the wafer. The other heat path through the metalization up to the pads/air interface only adds a small (parallel) contribution to the thermal resistance because stationary air is a very bad heat conductor ($\kappa_{\mathrm{Si}} \approx 5000\kappa_{\mathrm{air}}$).

As the wafer thickness ($h_{\mathrm{w}} = 775\,\mu\mathrm{m}$) is by far the largest vertical dimension in the simulation, the discretization needs to be set up carefully. A weak exponential increase of the discretization step size is employed for the wafer part to keep the memory consumption of the simulations low while still delivering accurate results. Additionally, the wafer width b_{w} must be chosen sufficiently large to capture the spreading heat flow and hence, the dimension is repetitively increased until there is no impact on the simulation result anymore.

Fig. 5.7 illustrates the temperature distribution for an exemplary transistor and demonstrates that the DTI confines the heat flow. To assess its impact on the thermal resistance, the DTI depth is aligned with the collector substrate junction and the simulations are repeated. While this allows to reduce ρ_{th} by 20 %, it would also decrease the substrate resistance – leading to a trade-off.

Running the simulations for different emitter widths and lengths allows to extract the technology specific thermal resistance according to the scaling approach of (3.49). The results of the extraction are shown in fig. 5.8 for the

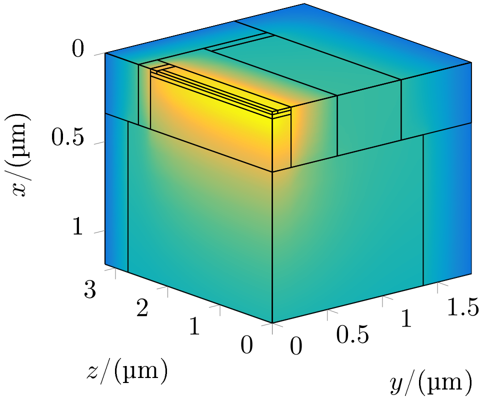
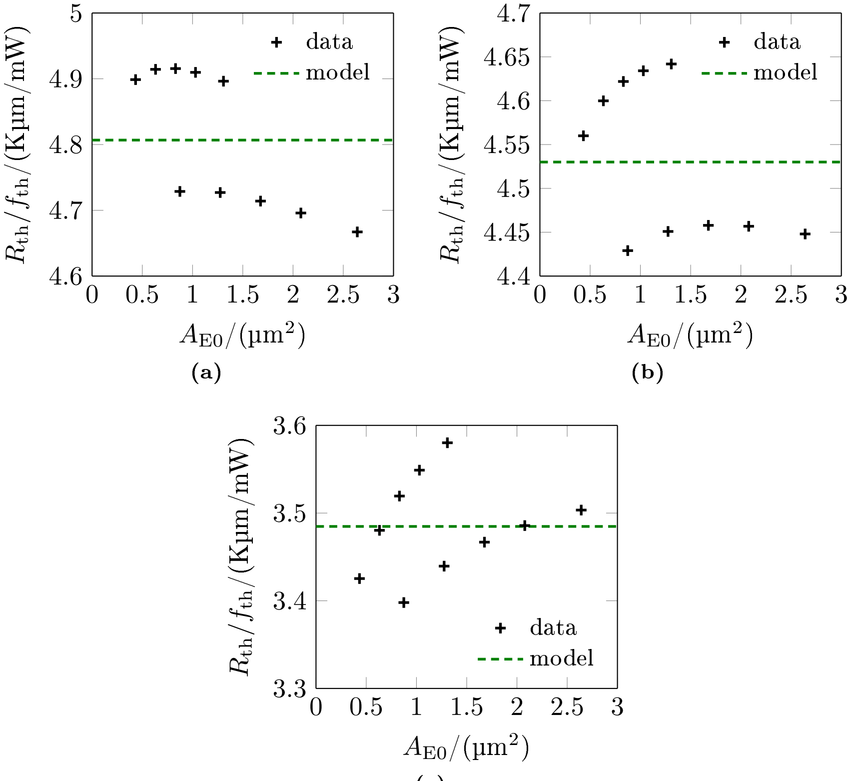


Figure 5.7: Simulation example for a transistor with a size of $l_{\mathrm{drawn}} = 4.5\,\mu m$ and $b_{\mathrm{drawn}} = 180\,\mathrm{nm}$ (process of [76]). Material boundaries and temperature distribution within one quarter of the actual device (zoom to relevant region). Brighter areas correspond to higher temperatures.

three transistor flavors. As can be observed by the summarized technology specific parameters in table 5.4, the accuracy is excellent. The different thermal conductivities for the internal collector and buried layer regions allow to capture the extracted variation of the HS, MV and HV transistor versions. For modeling the thermal simulation setup accurately, the heat source volume was adjusted for the respective flavors based on the SCR extensions of device simulations.



(a) **(b)**

(c)

Figure 5.8: Results for the thermal resistance obtained from thermal simulations for devices with $l_{\mathrm{drawn}} = (4.5 \text{ and } 9)\,\mathrm{\mu m}$ and $b_{\mathrm{drawn}} = (180 \text{ to } 378)\,\mathrm{nm}$ (process of [76]). Comparison of simulation data (markers) and model (lines) for ρ_{th} vs. A_{E0} for the HS **(a)**, the MV **(b)** and the HV transistor versions **(c)**.

$\rho_{\mathrm{th}}/\,(\mathrm{K\mu m/W})$	HS	MV	HV
reference (msmt)	4269	4190	3322
simulation	4807	4530	3485

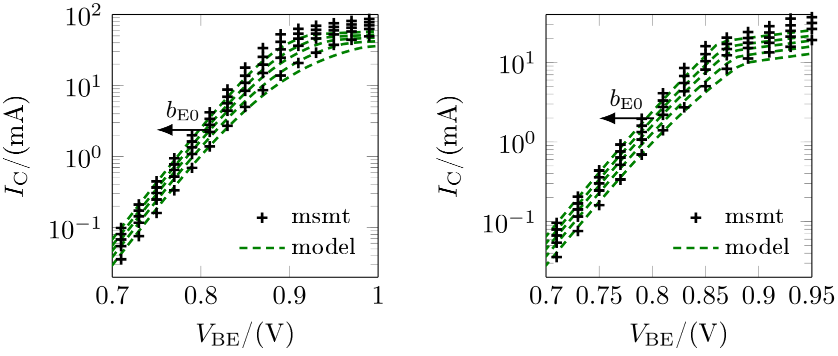
Table 5.4: Comparison of results for the simulated thermal resistance and the reference obtained by extraction on measurement data.

5.2.4 Full transistor results for selected transistor sizes

Assembling all previous simulation based extraction results allows to predict the performance of SiGe HBT devices. The technology specific parameters of the modelcard are scaled according to the approaches of chapter 3 and an individual modelcard for each device is obtained. Subsequently, circuit simulations can be performed and are then compared with measurements of the respective device.

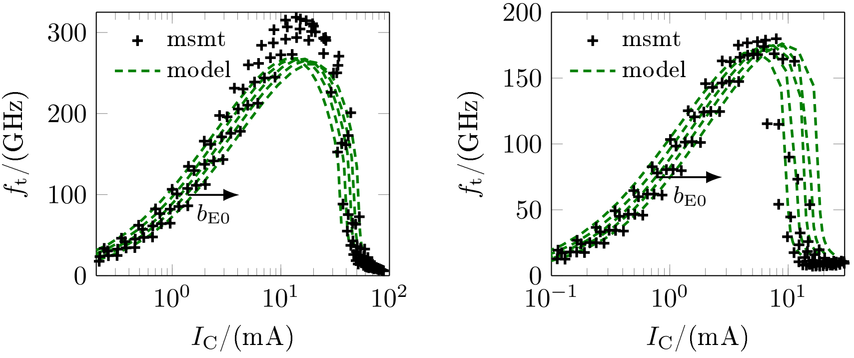
The results for the collector current and the transit frequency of the HS and MV flavors are shown in fig. 5.9 and fig. 5.10. It can be observed that the accuracy is acceptable and that the geometry trends are captured well. The difference between the weight factors of the reference and the TCAD approach was identified to be the cause for the discrepancy of I_{C} at high injection. Consequently, both the HD transport (and the chosen HD parameters), as well as the extraction uncertainty for the weight factors of the reference (caused by an extraction uncertainty for the composition of R_{th}, R_{E}, R_{Cx} and the weight factors) attribute to the weight factor inconsistency. Furthermore, the maximum of f_{t} is underestimated by the model for the HS transistor version, which was already the case for the 1D comparison in section 4.2.

Contrary to the adequate HS and MV results, the outcome for the HV transistors underestimates f_{t} greatly (see fig. 5.11). This is because current spreading is not taken into account correctly with the simulated 2D profiles; the current spreading angle is far too low in comparison with the reference. Adjusting δ_{C} to the reference value decreases the gap to the measurements significantly – as can be observed on the right hand side of fig. 5.11. The situation is identical for the collector current, as demonstrated in fig. 5.12. A plausible explanation for the deviation of δ_{C} is that the 2D doping profile of the periphery for the HV flavor is incorrect. Another additional error source is the DD transport limitation for the extraction of the 2D model description. According to (4.14), the model for the low-current transit time scaling relies on the area (1D) and peripheral minority transit time τ_{ma} and τ_{mp}. Reformulating the equation for HD transport reads



(a) **(b)**

Figure 5.9: Comparison of measurements and TCAD-based model for different emitter widths ($b_{\mathrm{drawn}} = (180 \text{ to } 378)\,\mathrm{nm}$, $l_{\mathrm{drawn}} = 9\,\mathrm{\mu m}$) at $T_{\mathrm{amb}} = 25\,°\mathrm{C}$ (including self-heating) and $V_{\mathrm{BC}} = 0\,\mathrm{V}$ (process of [76]). Results for the collector current I_C of the HS **(a)** and MV transistors **(b)**.



(a) **(b)**

Figure 5.10: Comparison of measurements and TCAD-based model for different emitter widths ($b_{\mathrm{drawn}} = (180 \text{ to } 378)\,\mathrm{nm}$, $l_{\mathrm{drawn}} = 9\,\mathrm{\mu m}$) at $T_{\mathrm{amb}} = 25\,°\mathrm{C}$ (including self-heating) and $V_{\mathrm{BC}} = 0\,\mathrm{V}$ (process of [76]). Results for the transit frequency f_t (5 GHz extrapolation frequency) of the HS **(a)** and MV transistors **(b)**.

$$f_{\tau\mathrm{pi,HD}} \approx \frac{\tau_{\mathrm{mp,HD}}}{\tau_{\mathrm{ma,HD}}}. \tag{5.10}$$

Additionally, the transit time ratios between DD and HD transport can be introduced for the area and periphery:

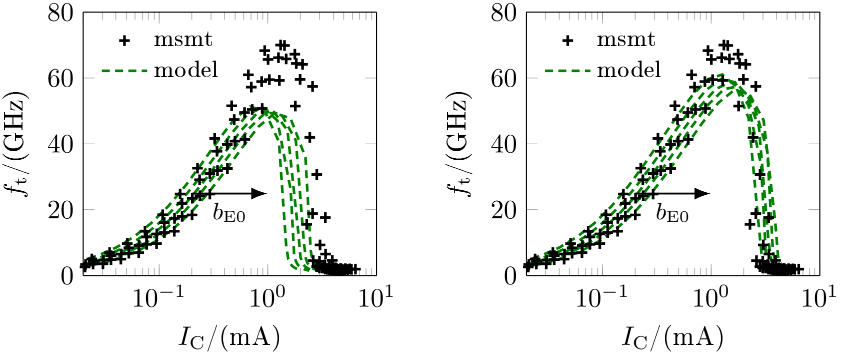
$$\begin{aligned} f_{\mathrm{trans,a}} &= \frac{\tau_{\mathrm{ma,HD}}}{\tau_{\mathrm{ma,DD}}} \\ f_{\mathrm{trans,p}} &= \frac{\tau_{\mathrm{mp,HD}}}{\tau_{\mathrm{mp,DD}}}. \end{aligned} \tag{5.11}$$

Combining (5.10) and (5.11) leads to

$$f_{\tau\mathrm{pi,HD}} \approx \frac{f_{\mathrm{trans,p}}}{f_{\mathrm{trans,a}}} \frac{\tau_{\mathrm{mp,DD}}}{\tau_{\mathrm{ma,DD}}} \tag{5.12}$$

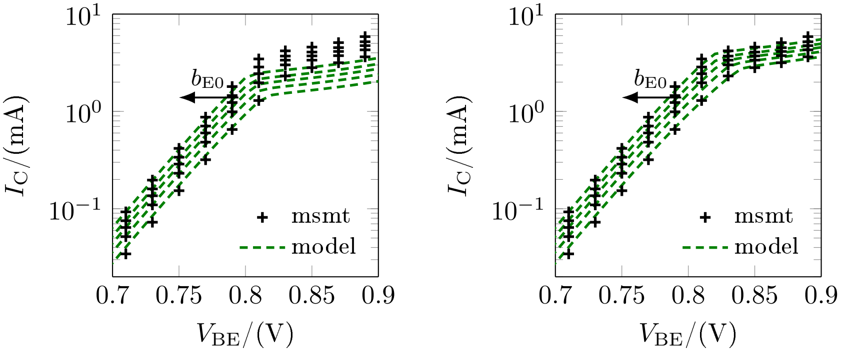
and illustrates that no HD transport is necessary to extract $f_{\tau\mathrm{pi,HD}}$ if the transport ratios are identical. As it can be assumed that the capacitances do not depend on the transport model, (5.11) basically results in $f_{\mathrm{trans}} = f_{\mathrm{t,DD}}/f_{\mathrm{t,HD}}$ – neglecting the difference for the transconductance between DD and HD transport. Even though the evaluations support that the 2D compact model parameters are mainly geometry dependent, the assumption of identical transport ratios involves an inconsistency for the prediction.

Finally, the predicted maximum oscillation frequency is presented in figures 5.13 and 5.14. A meaningful prediction of $f_{\max}$ strongly depends on the assumed interface resistances of the base link, for which a lower estimate has been done during the evaluation of tetrode measurements in section 3.5. Consequently, the prediction tends to result in a somewhat optimistic figure for $f_{\max}$.



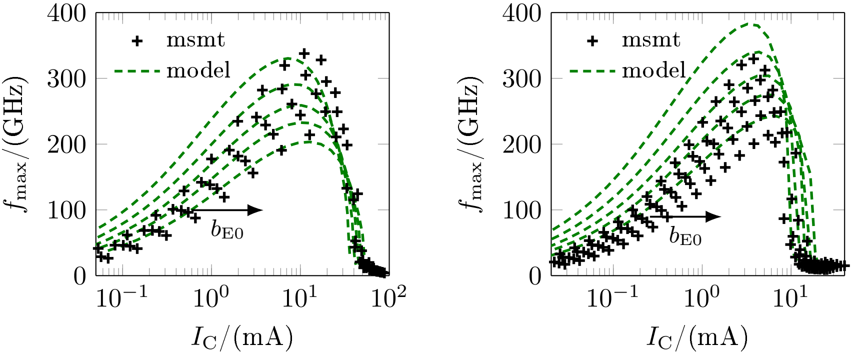
(a) **(b)**

Figure 5.11: Comparison of measurements and TCAD-based model for different emitter widths ($b_{\mathrm{drawn}} = (180 \text{ to } 378)\,\mathrm{nm}$, $l_{\mathrm{drawn}} = 9\,\mathrm{\mu m}$) at $T_{\mathrm{amb}} = 25\,°\mathrm{C}$ (including self-heating) and $V_{\mathrm{BC}} = 0\,\mathrm{V}$ (process of [76]). Results for the transit frequency f_t (5 GHz extrapolation frequency) of the HV transistors using **(a)** δ_C extracted from 2D TCAD and **(b)** the current spreading angle from measurements for the model evaluations.



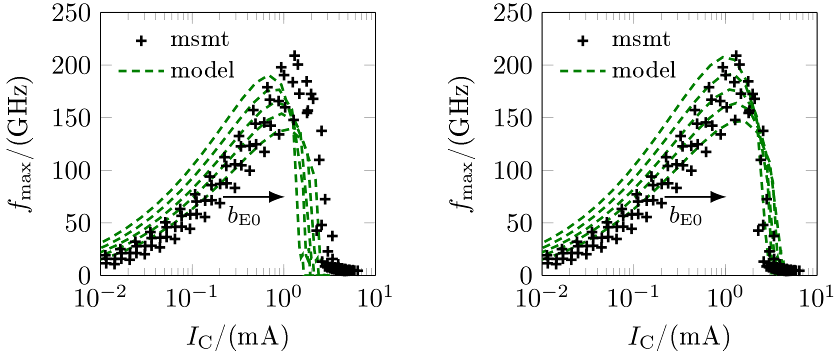
(a) **(b)**

Figure 5.12: Comparison of measurements and TCAD-based model for different emitter widths ($b_{\mathrm{drawn}} = (180 \text{ to } 378)\,\mathrm{nm}$, $l_{\mathrm{drawn}} = 9\,\mathrm{\mu m}$) at $T_{\mathrm{amb}} = 25\,°\mathrm{C}$ (including self-heating) and $V_{\mathrm{BC}} = 0\,\mathrm{V}$ (process of [76]). Results for the collector current I_C of the HV transistors using **(a)** δ_C extracted from 2D TCAD and **(b)** the current spreading angle from measurements for the model evaluations.



(a) **(b)**

Figure 5.13: Comparison of measurements and TCAD-based model for different emitter widths (b_{drawn} = (180 to 378) nm, l_{drawn} = 9 µm) at T_{amb} = 25 °C (including self-heating) and V_{BC} = 0 V (process of [76]). Results for the maximum oscillation frequency $f_{\max}$ (20 GHz extrapolation frequency) of the HS **(a)** and MV transistors **(b)**.



(a) **(b)**

Figure 5.14: Comparison of measurements and TCAD-based model for different emitter widths (b_{drawn} = (180 to 378) nm, l_{drawn} = 9 µm) at T_{amb} = 25 °C (including self-heating) and V_{BC} = 0 V (process of [76]). Results for the maximum oscillation frequency $f_{\max}$ (20 GHz extrapolation frequency) of the HV transistors using **(a)** δ_C extracted from 2D TCAD and **(b)** the current spreading angle from measurements for the model evaluations.

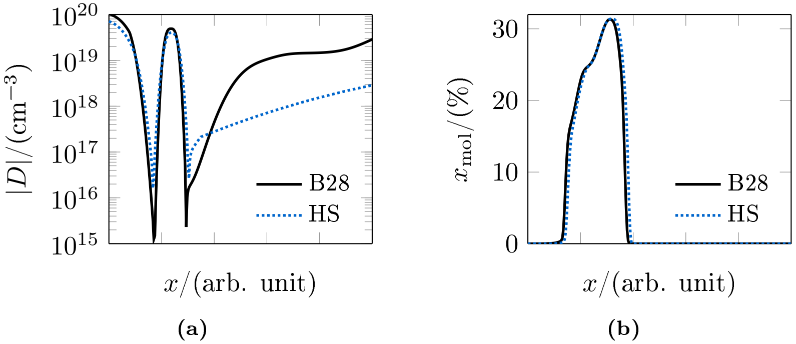


Figure 5.15: 1D doping profile comparison between the HS flavor of [76] (calibration result) and the process simulation based result for the future technology [130]. **(a)** Doping profile $D = N_{\mathrm{A}}^{-} - N_{\mathrm{D}}^{+}$ and **(b)** germanium mole fraction x_{mol} vs. vertical depth x.

5.3 Prediction of a future technology for a 28 nm lithography node

In [130] a fictitious BiCMOS technology has been designed for which the performance prediction is performed. The – in comparison to other advanced BiCMOS processes – very small feature size allows for sophisticated designs. In comparison to [76], the internal collector doping was increased (see fig. 5.15) to delay the onset of the Kirk effect by reducing the internal collector resistance. Conversely, other parts of the profile were only impacted by the slightly different thermal budget of the future process. A cross section of the process is shown in fig. 5.16 for an exemplary transistor. To counter self-heating at very high current densities, the thermal resistance is reduced by replacing the deep trench with a junction isolation and by decreasing the substrate thickness. Other core features of the architecture are a selectively grown base and an oxide-isolated internal collector – minimizing the external BC junction area. Note that the connection of the internal monosilicon base is realized from underneath.

All steps of section 5.2 need to be repeated for the new architecture. In the first step, 1D simulations are performed for determining the area related

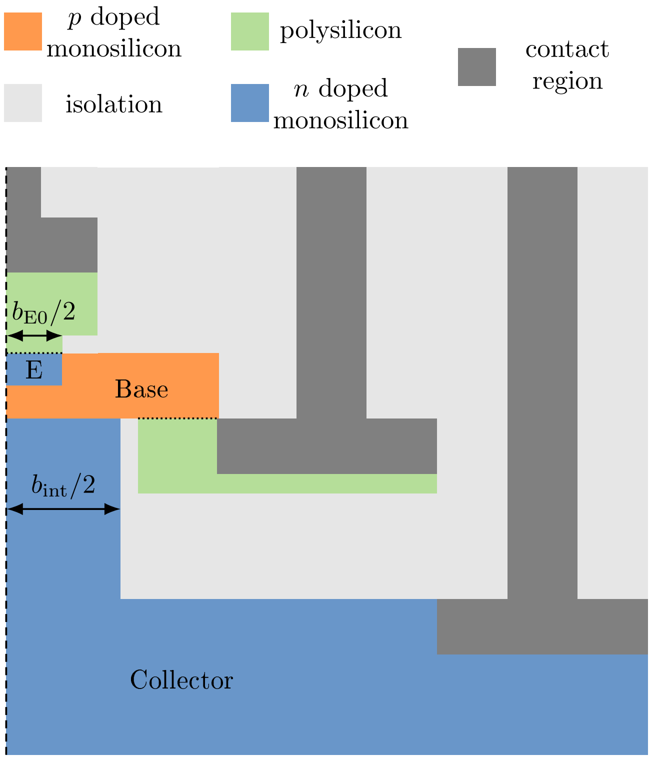


Figure 5.16: Cross section of the technology under investigation (right hand side of the structure). Exemplary transistor with an emitter width of $b_{E0} = 64\,\text{nm}$ and an internal collector width of $b_{int} = 130\,\text{nm}$. The dashed and dotted lines illustrate the symmetry line and mono- to polysilicon interfaces, respectively.

model components. Corresponding results are shown in fig. 5.18. The peak value for f_t is close to 650 GHz at $V_{BC} = -0.5\,\text{V}$ – a promising result for the full transistor structure. In comparison to the TCAD-based roadmap of [131], this result is a bit lower than the performance of node 2, which in turn would forecast a performance slightly below 400 GHz at peak f_t for the full 3D structure – depending on the external architecture. It also indicates that there is enough room for additional improvement of the 1D profile. By employing a profile similar to nodes 3 or 4, the 1D performance could be increased significantly. Moreover, the internal base sheet resistance of $R_{s,Bi0} =$

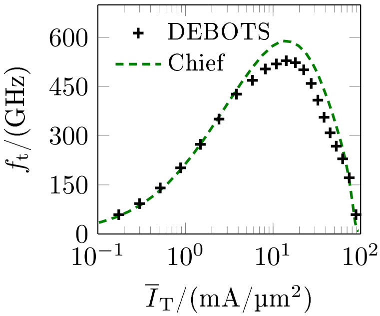
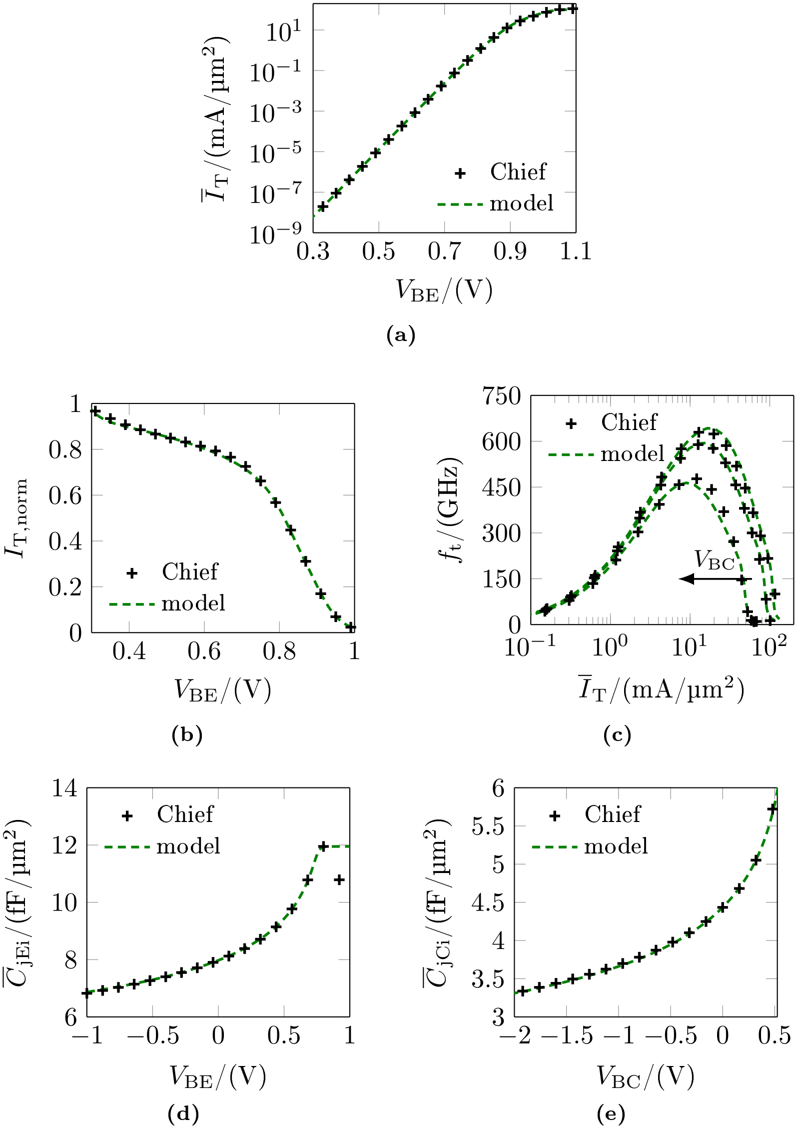


Figure 5.17: Comparison of BTE and HD simulation for the transit frequency using the 1D profile for the technology of [130] at $V_{CE} = 0.9\,\mathrm{V}$.

$5650\,\Omega/\square$ could be reduced by increasing the peak base doping, which in turn would help to keep the internal base resistance low.

To assess the impact of the chosen transport model on the transit frequency, additional BTE simulations are conducted with DEBOTS for a constant V_{CE}, which saves simulation runtime in comparison to forcing V_{BC}: As the calculation of f_t is based on a constant V_{CE}, the additional simulation run for the quasi-static excursion can be waived. The comparison is displayed in fig. 5.17 and demonstrates that the chosen HD approach is calibrated sufficiently. As the discrepancy is only slightly above 10 % at peak f_t (a difference of about 60 GHz), further BTE-based investigations are not performed. Other uncertainties, like contact resistances (see section 5.3.2 for a sensitivity study) or doping profiles have a similar impact.

Next, the temperature parameters are determined by extraction on DD simulation data of different lattice temperatures. Fig. 5.19 presents the corresponding comparison between compact model and device simulations. After the 1D model preparations, extraction on 2D DD simulations are performed and the geometry scalable model of the internal transistor is completed. The full parameter set is listed in appendix C.2: The obtained parameters demonstrate that the external collector junction capacitance has been reduced by about 60 % in comparison to the process of [76]. On the other hand, nearly no collector current spreading is observed for the analyzed technology – increasing the internal collector resistance of small devices. Both outcomes are a result of the isolated collector architecture.

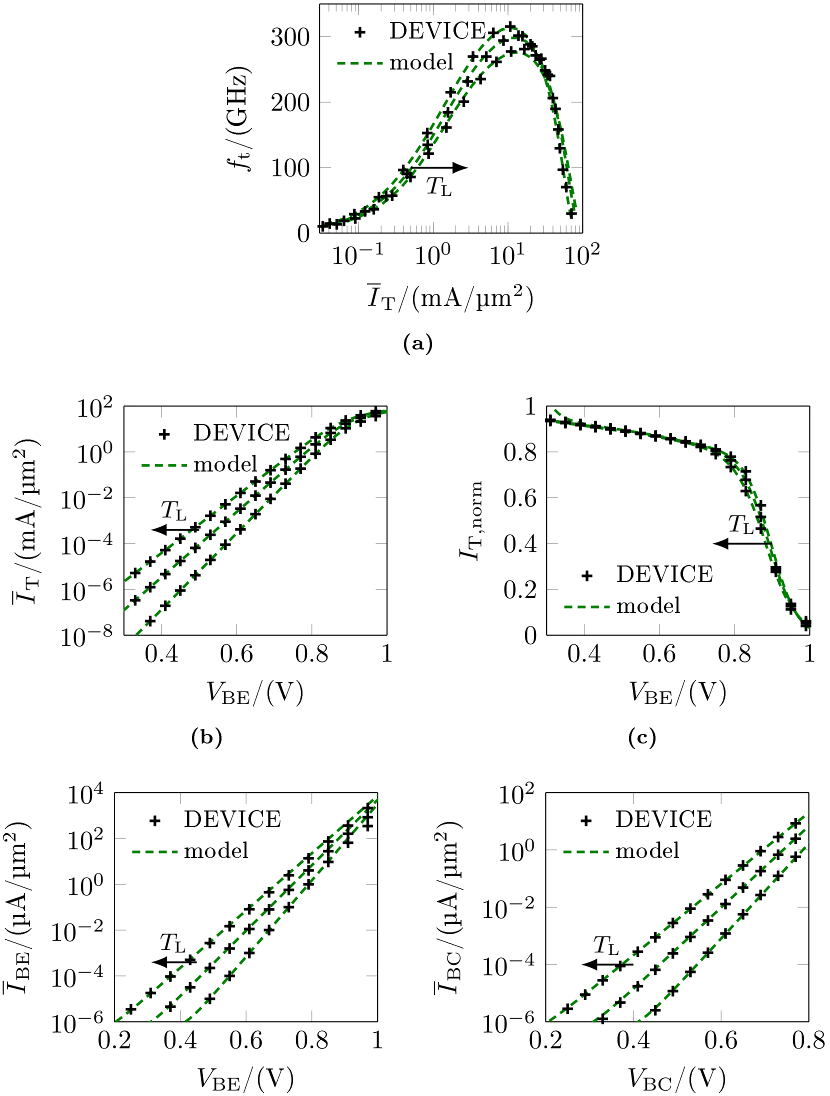


(a)

(b) **(c)**

(d) **(e)**

Figure 5.18: Comparison of HD simulations for the 1D profile with the corresponding extracted model based on HICUM for the technology of [130]. Results for **(a)** $\overline{I}_\mathrm{T}$ vs. V_BE at $V_\mathrm{BC} = 0\,\mathrm{V}$, **(b)** $I_\mathrm{T,norm}$ vs. V_BE at $V_\mathrm{BC} = 0\,\mathrm{V}$, **(c)** f_t vs. $\overline{I}_\mathrm{T}$ for $V_\mathrm{BC} = (-0.5, 0 \text{ and } 0.5)\,\mathrm{V}$, **(d)** $\overline{C}_\mathrm{jEi}$ vs. V_BE and **(e)** $\overline{C}_\mathrm{jCi}$ vs. V_BC.



(a)

(b) **(c)**

(d) **(e)**

Figure 5.19: Comparison of DD simulations for the 1D profile with the corresponding extracted model based on HICUM for the technology of [130] at $V_{BC} = 0\,\mathrm{V}$. Results for **(a)** f_t vs. $\overline{I}_T$, **(b)** $\overline{I}_T$ vs. V_{BE}, **(c)** $I_{T,norm}$ vs. V_{BE}, **(d)** $\overline{I}_{BE}$ vs. V_{BE} and **(e)** $\overline{I}_{BC}$ vs. V_{BC} for different lattice temperatures ($T_L = (300, 350 \text{ and } 400)\,\mathrm{K}$).

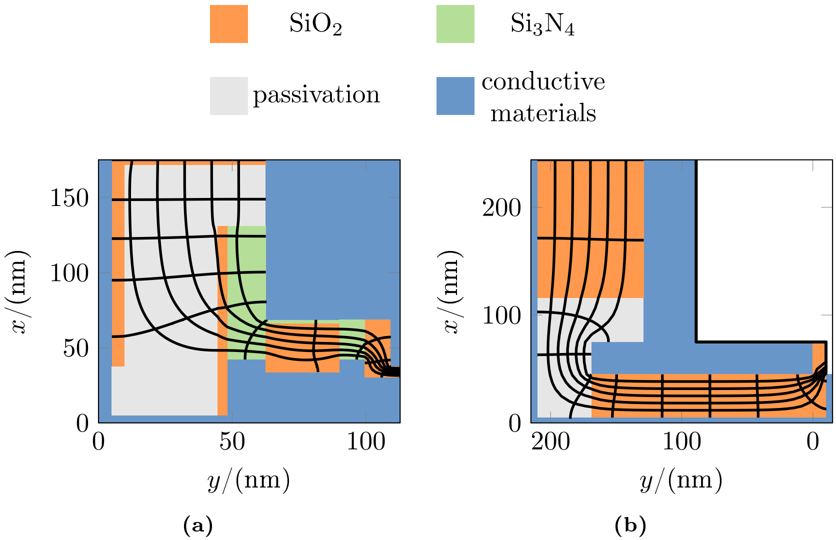


Figure 5.20: Field line and potential distribution for **(a)** the BE and **(b)** the BC spacer.

5.3.1 External elements

As the spacer structure has been modified in comparison to [76] (see section 3.2), Laplace simulations for the parasitic capacitances are performed. The geometry and material information of the process TCAD simulations are used to set up the simulation input and the capacitances $C'_{\mathrm{BE,par}} = 0.286\,\mathrm{fF/\mu m}$ and $C'_{\mathrm{BC,par}} = 0.373\,\mathrm{fF/\mu m}$ are obtained from the simulation output. Due to the comparably small spacer dimensions, the BC spacer capacitance increased. However, as all of the field lines end on the polysilicon side of the poly-to-mono interface of the base (see fig. 5.20), most of $C'_{\mathrm{BC,par}}$ connects the internal collector with the base via. That means that $f_{\mathrm{BC,par}}$ is very small, which is beneficial for f_{max}.

The determination of external resistances for the prediction approach is based on the methods and equations of section 5.2.1. Applying (5.1) and (5.4) leads to $R_{\mathrm{s,bl}} = 138\,\Omega/\square$ and $\rho_{\mathrm{sk,mono}} = 0.48\,\Omega\,\mathrm{\mu m}^2$, respectively. By conducting quasi-3D device simulations and including the interface resistance of (5.5) manually, the results for the external collector resistance are obtained

parameter (unit)	$R_{\mathrm{s,Bx,lv0}}$ ($\Omega/\square$)	$R_{\mathrm{s,Bx,l0}}$ ($\Omega/\square$)
value	4386	1068
parameter (unit)	$R_{\mathrm{s,po}}{}^{*}$ ($\Omega/\square$)	$R_{\mathrm{s,sil}}{}^{*}$ ($\Omega/\square$)
value	710	15

*Assumed values based on process information.

Table 5.5: Technology parameters of the base resistance description based on TCAD simulations.

parameter (unit)	$\overline{C}_{\mathrm{jSb0}}$ (fF/µm^2)	z_{Sb} (1)	V_{DSb} (V)
value	0.232	0.44	0.72

Table 5.6: Extracted parameters for $\overline{C}_{\mathrm{jSb}}$ of the capacitance description of HICUM based on 1D device simulation data for the future architecture of [130].

(see appendix C.2).

(5.6) and (5.7) lead to the parameters of table 5.5. The vertical resistance of the monosilicon does not play a role for the process because the link of the mono- on polysilicon region to the internal base is realized laterally and hence, $\rho_{\mathrm{Bx,l0,mono}} = 0\,\Omega\,\mu\mathrm{m}^2$. Nevertheless, the result for the generic interface property (see (5.8)) was taken into account for the quasi-3D simulation results of R_{Bx} presented in appendix C.2.

Repeating the approach of section 5.2.2 to determine the substrate capacitance leads to the results of table 5.6. It is observed that the substrate capacitance is increased due to the increased substrate doping close to the CS junction – caused by the different processing. Note that the peripheral portion of the CS junction capacitance could not be taken into account because no doping profile was available from process TCAD. Likewise, the remaining components of the substrate network (C_{su}, R_{su} and $R_{\mathrm{S,cont}}$) cannot be determined and are set to zero.

Finally, the thermal resistance model is updated by thermal simulations of the full 3D structure using updated dimensions and materials. Due to the reduced wafer thickness and the CS junction isolation (i.e. the DTI isolation is waived), the technology specific value for the thermal resistance is reduced to $\rho_{\mathrm{th}} = 3229\,\mathrm{K\mu m/W}$. The technology specific model generation is concluded by adding the emitter contact resistance to the modelcard. It is assumed that ρ_{E} remains at the previously extracted value of $1.64\,\Omega\,\mathrm{\mu m}^2$ (see section 3.9).

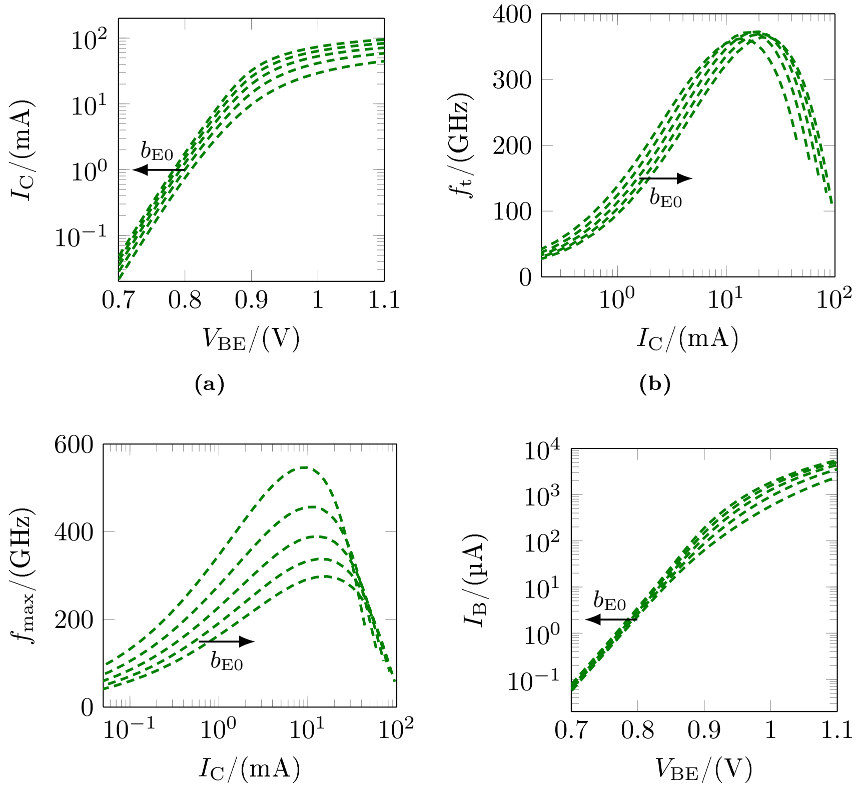
5.3.2 Full transistor results for selected transistor sizes

By collecting the previous model results, the technology specific modelcard for the architecture of [130] is created. After scaling the parameters according to the approaches of chapter 3 for selected device geometries, circuit simulations are performed and the typical performance of the technology is evaluated. Fig. 5.21 presents the corresponding results.

As was expected by the increased collector doping, both f_{t} and f_{max} increase significantly in comparison with the TCAD results of section 5.2.4. The low internal collector resistance delays the onset of the high current transit time and allows for higher collector current densities at peak f_{t}, which in turn decreases the impact of the capacitances. The current density at peak f_{t} is $J_{\mathrm{T,peak}} = 16.5\,\mathrm{mA/\mu m^2}$, which is about 2.5 times larger than $J_{\mathrm{T,peak}}$ of [76]. The peak values are $f_{\mathrm{t}} = 362\,\mathrm{GHz}$ and $f_{\mathrm{max}} = 546\,\mathrm{GHz}$ at $V_{\mathrm{BC}} = 0\,\mathrm{V}$ for the smallest transistor width. At $V_{\mathrm{BC}} = -0.5\,\mathrm{V}$, the performance can be increased to $f_{\mathrm{t}} = 375\,\mathrm{GHz}$ and $f_{\mathrm{max}} = 587\,\mathrm{GHz}$. Note though that the peak value for f_{max} strongly depends on the assumed interface resistance of the base link; increasing the interface area by a factor of two increases f_{max} by 50 GHz. Doing the opposite leads to a drop of nearly 90 GHz.

To identify performance bottlenecks of the transistor architecture, each external component is reduced by 50 % while keeping the remaining parameters at their initial value and the absolute increase of peak f_{t} and f_{max} is recorded at $V_{\mathrm{BC}} = 0\,\mathrm{V}$. As can be observed in table 5.7, the largest restraint is caused by R_{Bx}, R_{Cx} and $C_{\mathrm{BC,par}}$. Consequently, increasing the respective interface areas and the internal collector length are suitable options for a performance improvement.

To waive the trench isolation in favor of a junction isolation helped to keep the thermal resistance low. Even though the transistors operate at higher current densities, the temperature increase caused by self-heating at peak f_{t} of the smallest device is only 25 K, which is somewhat lower than the predicted temperature increase of technology [76]: 31 K. The external collector resistance, which is about 2 times larger than in [76], limits I_{C} and in turn the temperature increase caused by self-heating is restricted additionally.



(a) **(b)**

(c) **(d)**

Figure 5.21: TCAD-based model for different emitter widths ($b_{E0} = (64 \text{ to } 192)\,\mathrm{nm}$, $l_{E0} = 9\,\mu\mathrm{m}$) at $T_{amb} = 25\,°\mathrm{C}$ (including self-heating) and $V_{BC} = 0\,\mathrm{V}$ (future technology of [130]). Results for **(a)** I_C vs. V_{BE}, **(b)** f_t vs. I_C (20 GHz extrapolation frequency), **(c)** f_{max} vs. I_C (50 GHz extrapolation frequency) and **(d)** I_B vs. V_{BE}.

An increased collector doping comes at the cost of a decreased breakdown voltage. For the future architecture under investigation, $BV_{CEO} = 1.7\,\mathrm{V}$ has been determined for a DC current gain of $B_f \approx 1550$ at $V_{BE} = 0.7\,\mathrm{V}$. This outcome seems to be too optimistic considering that the breakdown voltage of other advanced SiGe HBTs with lower collector doping is in the same range, e.g. [76]. The uncertainty of the base current prediction causes a margin

parameter	R_{Bx}	R_{E}	R_{Cx}
impact on f_{max}	85 GHz	21 GHz	64 GHz
impact on f_{t}	0 GHz	22 GHz	30 GHz
parameter	$C_{\mathrm{BE,par}}$	$C_{\mathrm{BC,par}}$	C_{jCx0}
impact on f_{max}	4 GHz	49 GHz	19 GHz
impact on f_{t}	13 GHz	34 GHz	13 GHz

Table 5.7: Sensitivity study for assessing the impact of external elements on device performance. The respective parameter values are reduced by 50 % and the absolute increase of peak f_{t} and f_{max} is recorded for a transistor with a size of $b_{\mathrm{E0}} = 64\,\mathrm{nm}$ and $l_{\mathrm{E0}} = 9\,\mu\mathrm{m}$ at $V_{\mathrm{BC}} = 0\,\mathrm{V}$.

for BV_{CEO}: The base current could turn out to be smaller than predicted, which would reduce BV_{CEO}. To reduce the impact of the base current on the predicted breakdown voltage, the definition of the DC forward current gain is written down:

$$B_{\mathrm{f}} = \frac{I_{\mathrm{Tf}}}{I_{\mathrm{B}}}. \tag{5.13}$$

When BV_{CEO} is reached, the base current is zero and hence, the avalanche generated current I_{avl} equals I_{B}, which in turn leads to

$$B_{\mathrm{f}} = \left.\frac{I_{\mathrm{Tf}}}{I_{\mathrm{avl}}}\right|_{BV_{\mathrm{CEO}}}. \tag{5.14}$$

I_{avl} is determined from device simulations for different V_{CE} at a fixed V_{BE}. Subsequently, BV_{CEO} is plotted against B_{f}, which was calculated according to (5.14). The result is illustrated in fig. (5.22) and shows that the breakdown voltage varies between $1.51\,\mathrm{V} \leq BV_{\mathrm{CEO}} \leq 1.78\,\mathrm{V}$ within the relevant range. In addition to the uncertainty of the base current, an error is involved in comparison with more reliable avalanche models based on MC simulations (see [122]). For the prediction, a simplified impact ionization model is used, which is based on carrier temperature (see (4.6)).

All in all, the analyzed technology brings together all necessary features for great RF performance. Implementing an even faster 1D profile is possible for additional performance gains. The technology not only offers good perfor-

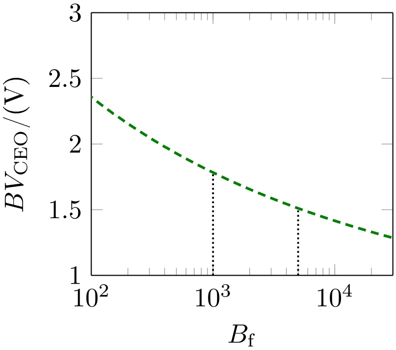


Figure 5.22: Breakdown voltage BV_{CEO} vs. forward current gain B_f obtained by 1D HD simulations for the future technology of [130]. The dotted lines indicate the relevant region for B_f.

mance, but also cost efficiency: The 28 nm lithography and the 300 mm wafer processing allow for a very small transistor footprint and high volumes.

CHAPTER 6

Conclusion and outlook

This thesis exploited the capabilities of TCAD tools and approaches for the performance prediction of SiGe HBTs. At the beginning the work, SiGe material models were calibrated to literature for the upcoming drift-diffusion and hydrodynamic simulation tasks. The models include all relevant physical effects of HD transport – like mobility, energy relaxation times or density of states. Additionally, the models for the band gap of the SiGe layer and band gap narrowing were adjusted to the measured reference during the course of the work. This step was mandatory for a reliable determination of the transfer current at low injection from TCAD simulations.

A large part of the thesis focused on the calibration of doping profiles and the assessment of the significance of TCAD simulations for the prediction approach. The relevant reference data were obtained for an advanced SiGe HBT technology [76] by extraction of compact model parameters on measurement data. Since the extraction methods assume the largest portion of the evaluations for the prediction, it was necessary to establish a sophisticated methodology for parameter determination.

Based on technology specific parameters for the analyzed architecture, 1D data can be generated that are free from the impact of external elements and thus, shortcomings of the 1D simulation approach are identified readily. The comparison between the data and 1D simulations revealed that the internal collector doping is the most important bottleneck for a reliable prediction. Overall, the agreement of simulations and measurements is very good if 2D doping profile information can be acquired. However, this is usually not the case because secondary ion mass spectrometry only allows to obtain vertical profile data and electron dispersive X-ray spectroscopy is not sensitive enough to capture the relevant doping levels (only alloy concentrations may be detected by EDX). In conjunction with the uncertainty on carrier transport and the assumed contact resistances, an inaccuracy arises for the prediction. Interface resistances will play an important role for the prediction: in particular the poly- to monosilicon interface resistances of the base link and the emitter stack. The former has become the dominant portion of the external base resistance and decides whether or not the predicted maximum oscillation frequency can be achieved with the analyzed technology.

Finally, the prediction methodology is applied to a future process architecture [130] in a 28 nm lithography node, which is demonstrated to exhibit excellent RF capabilities: The peak values of $f_\mathrm{t} = 362\,\mathrm{GHz}$ and $f_\mathrm{max} = 546\,\mathrm{GHz}$ at $V_\mathrm{BC} = 0\,\mathrm{V}$ exceed typical performances of current SiGe HBTs technologies in industry. The future architecture comprises several necessary process changes for the realization of sophisticated RF products: a junction isolation of the collector substrate area for reducing the thermal resistance, an isolated collector to reduce the external base collector junction capacitance and a lateral link of the external to internal monosilicon base for a low base resistance.

The prediction results for [130] align well with the high aims of the international technology roadmap for semiconductors of SiGe HBTs. The future process is positioned close to node 2 of the TCAD based roadmap of [131], which is based on a very similar methodology for the prediction. Yet, the 1D doping profiles are far from the ultimate transistor limits (represented by node 5 of the roadmap), which leaves additional room for improvements of the architecture; for example by implementing the 1D doping profiles of node 3 or 4 into [130]. Additionally, a different trade-off between external resistances and capacitances is feasible to improve f_max.

APPENDIX A

Supplementary extraction data and results

A.1 External collector resistance

The parameter values for R_{Cx} obtained by device simulation based on the buried layer sheet resistance and sinker contact resistance are listed in table A.1.

(HS) R_{Cx}/Ω	$l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$		$l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$	
	msmt	TCAD	msmt	TCAD
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	4.78	4.57	2.47	2.36
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	4.81	4.59	2.49	2.37
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	4.83	4.61	2.50	2.38
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	4.85	4.63	2.51	2.39
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	4.88	4.65	2.53	2.41
(MV) R_{Cx}/Ω	$l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$		$l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$	
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	4.78	4.57	2.47	2.36
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	4.80	4.59	2.49	2.37
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	4.83	4.61	2.50	2.38
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	4.85	4.63	2.51	2.39
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	4.88	4.65	2.53	2.41
(HV) R_{Cx}/Ω	$l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$		$l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$	
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	40.3	39.0	20.9	20.3
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	40.5	39.3	21.0	20.4
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	40.8	39.6	21.2	20.6
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	41.0	39.9	21.3	20.7
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	41.4	40.3	21.5	21.0

Table A.1: Quasi-3D simulation results for the external collector resistance R_{Cx} for all three transistor flavors. The as "msmt" and "TCAD" declared results either use technology specific resistances of measured collector resistance test structures or the TCAD based calculations of section 5.2.1.

A.2 Base resistance

The parameter values for R_{Bx} and R_{Bi0} obtained by device simulation based on the base sheet resistances are listed in tables A.2 and A.3, respectively.

(HS) R_{Bx}/Ω	$l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$		$l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$	
	msmt	TCAD	msmt	TCAD
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	37.2	25.3	19.0	13.0
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	36.8	25.1	18.8	12.9
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	36.5	24.9	18.8	12.9
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	36.2	24.5	18.7	12.7
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	35.8	24.2	18.6	12.7
(MV) R_{Bx}/Ω	$l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$		$l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$	
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	31.2	24.5	15.9	12.6
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	30.8	24.3	15.8	12.5
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	30.6	24.1	15.7	12.5
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	30.4	23.8	15.6	12.4
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	30.1	23.5	15.5	12.3
(HV) R_{Bx}/Ω	$l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$		$l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$	
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	31.8	24.8	16.2	12.8
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	31.4	24.6	16.0	12.7
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	31.1	24.4	16.0	12.6
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	30.9	24.1	15.9	12.5
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	30.6	23.8	15.8	12.5

Table A.2: Quasi-3D simulation results for the external base resistance R_{Bx} for all three transistor flavors. The as “msmt” and “TCAD” declared results either use technology specific resistances of measured tetrode structures or the TCAD based calculations of section 5.2.1.

(HS) R_{Bi0}/Ω	$l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$ msmt | TCAD	$l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$ msmt | TCAD
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	15.8 | 14.5	7.94 | 7.31
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	20.3 | 18.9	10.3 | 9.56
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	24.8 | 23.3	12.6 | 11.8
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	29.2 | 27.6	14.9 | 14.1
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	35.2 | 33.5	18.0 | 17.2
(MV) R_{Bi0}/Ω	$l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$	$l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	14.5 | 12.2	7.28 | 6.16
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	18.7 | 16.0	9.43 | 8.09
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	22.8 | 19.7	11.5 | 10.0
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	26.8 | 23.4	13.6 | 11.9
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	32.3 | 28.5	16.5 | 14.6
(HV) R_{Bi0}/Ω	$l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$	$l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	14.5 | 11.9	7.31 | 6.01
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	18.7 | 15.6	9.47 | 7.88
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	22.9 | 19.2	11.6 | 9.75
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	26.9 | 22.8	13.7 | 11.6
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	32.5 | 27.7	16.6 | 14.2

Table A.3: Quasi-3D simulation results for the internal zero-bias base resistance R_{Bi0} for all three transistor flavors. The as "msmt" and "TCAD" declared results either use technology specific resistances of measured tetrode structures or the TCAD based calculations of section 5.2.1.

A.3 Substrate network

The parameter values for C_{su}, R_{su} and $R_{\mathrm{S,cont}}$ obtained by extraction are listed in tables A.4, A.5 and A.6, respectively. Additionally, the behavior of the peripheral component C'_{jSp} of the CS junction capacitance is displayed in fig. A.1. As can be observed, the capacitance is nearly constant over bias – as is expected from the DTI isolation.

(HS) C_{su}/fF	$l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$	$l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	10.8	16.1
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	9.63	13.9
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	10.9	14.7
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	10.3	13.0
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	9.78	13.3
(MV) C_{su}/fF	$l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$	$l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	10.9	14.3
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	10.1	13.6
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	10.1	15.7
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	10.7	15.2
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	10.1	13.9
(HV) C_{su}/fF	$l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$	$l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	12.4	13.9
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	12.2	15.3
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	12.4	14.0
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	11.5	15.5
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	11.4	15.1

Table A.4: Extraction results for the substrate capacitance C_{su} for all three transistor flavors.

(HS) $R_{\mathrm{su}}/\mathrm{k\Omega}$	$l_{\mathrm{drawn}} = 4.5\,\mathrm{\mu m}$	$l_{\mathrm{drawn}} = 9\,\mathrm{\mu m}$
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	2.96	2.80
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	3.52	2.71
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	2.87	2.91
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	3.16	2.70
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	3.26	2.96
(MV) $R_{\mathrm{su}}/\mathrm{k\Omega}$	$l_{\mathrm{drawn}} = 4.5\,\mathrm{\mu m}$	$l_{\mathrm{drawn}} = 9\,\mathrm{\mu m}$
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	3.01	2.81
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	3.08	2.61
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	3.16	2.77
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	3.44	2.67
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	3.47	2.55
(HV) $R_{\mathrm{su}}/\mathrm{k\Omega}$	$l_{\mathrm{drawn}} = 4.5\,\mathrm{\mu m}$	$l_{\mathrm{drawn}} = 9\,\mathrm{\mu m}$
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	2.39	2.37
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	2.43	2.22
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	1.70	2.43
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	2.50	2.25
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	2.66	2.35

Table A.5: Extraction results for the substrate resistance R_{su} for all three transistor flavors.

(HS) $R_{\mathrm{S,cont}}/\Omega$	$l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$	$l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	349	265
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	341	214
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	291	222
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	250	171
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	202	121
(MV) $R_{\mathrm{S,cont}}/\Omega$	$l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$	$l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	420	300
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	418	260
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	409	237
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	325	197
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	313	169
(HV) $R_{\mathrm{S,cont}}/\Omega$	$l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$	$l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$
$b_{\mathrm{drawn}} = 180\,\mathrm{nm}$	419	292
$b_{\mathrm{drawn}} = 225\,\mathrm{nm}$	356	252
$b_{\mathrm{drawn}} = 270\,\mathrm{nm}$	412	256
$b_{\mathrm{drawn}} = 315\,\mathrm{nm}$	405	235
$b_{\mathrm{drawn}} = 378\,\mathrm{nm}$	338	224

Table A.6: Extraction results for the substrate contact resistance $R_{\mathrm{S,cont}}$ for all three transistor flavors.

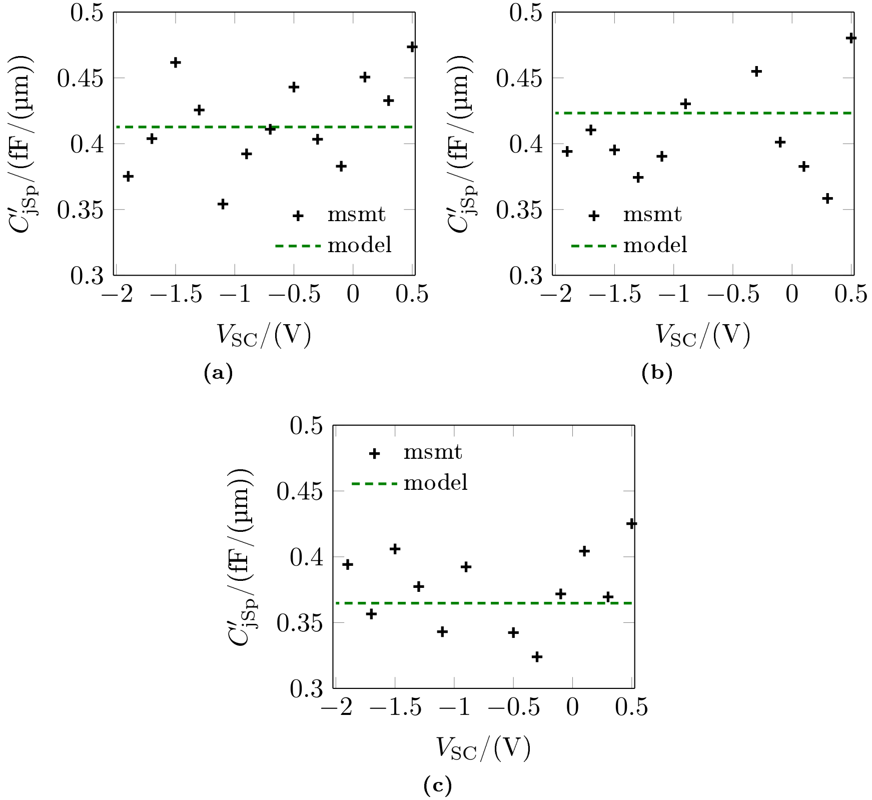


Figure A.1: Comparison of measurements (markers) and fit (lines) for the peripheral component C'_{jSp} of the CS junction capacitance (process of [76]). Results for **(a)** the HS, **(b)** the MV and **(c)** the HV transistor flavors.

A.4 Transit time

The extracted parameters for the transit time are listed in tables A.7, A.8 and A.9 for all three transistor flavors. Using the model, a comparison for the transit time and maximum oscillation frequency with measurements was performed, as illustrated in figures A.2, A.3 and A.4.

parameter (HS)	$\tau_{0\mathrm{a}}$	$\alpha_{\tau0}$	$k_{\tau0}$	τ_{bvl}	$\Delta\tau_{0\mathrm{h}}$
(unit)	(fs)	(1/kK)	(1/MK^2)	(fs)	(fs)
value	303.7	2.56	4.85	48.8	38.2
parameter (HS)	ρ_{Ci0}	ζ_{Ci}	V_{CEs}	α_{CEs}	V_{pt}
(unit)	($\Omega\,\mu\mathrm{m}^2$)	(1)	(mV)	(1/kK)	(V)
value	41.2	0.376	73.4	3.26	100
parameter (HS)	V_{lim}	α_{vs}			
(unit)	(V)	(1/kK)			
value	1.52	2.89			
parameter (HS)	τ_{hcs}	a_{hc}	τ_{Ef0}	g_{tfe}	
(unit)	(ps)	(1)	(ps)	(1)	
value	49.5	0.128	0	1	

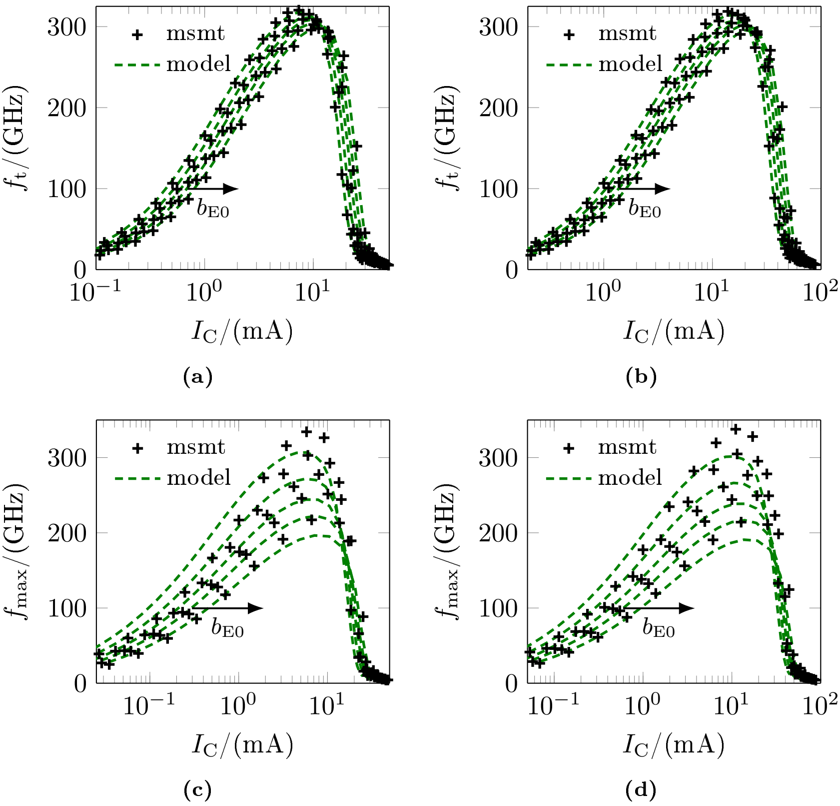
Table A.7: Extracted parameters of the transit time description of HICUM for the HS transistors of [76].

parameter (MV)	$\tau_{0\mathrm{a}}$	$\alpha_{\tau 0}$	$k_{\tau 0}$	τ_{bvl}	$\Delta\tau_{0\mathrm{h}}$
(unit)	(fs)	(1/kK)	(1/MK^2)	(fs)	(fs)
value	525.2	2.64	6.16	9.32	24.5
parameter (MV)	ρ_{Ci0}	ζ_{Ci}	V_{CEs}	α_{CEs}	V_{pt}
(unit)	($\Omega\,\mu\mathrm{m}^2$)	(1)	(mV)	(1/kK)	(V)
value	156	0.116	16.0	33.1	100
parameter (MV)	V_{lim}	α_{vs}			
(unit)	(V)	(1/kK)			
value	1.55	0.944			
parameter (MV)	τ_{hcs}	a_{hc}	τ_{Ef0}	g_{tfe}	
(unit)	(ps)	(1)	(fs)	(1)	
value	40.1	0.0866	23.4	1.25	

Table A.8: Extracted parameters of the transit time description of HICUM for the MV transistors of [76].

parameter (HV)	$\tau_{0\mathrm{a}}$	$\alpha_{\tau 0}$	$k_{\tau 0}$	τ_{bvl}	$\Delta\tau_{0\mathrm{h}}$
(unit)	(fs)	(1/kK)	(1/MK^2)	(fs)	(fs)
value	946.4	3.91	−10.7	213	440
parameter (HV)	ρ_{Ci0}	ζ_{Ci}	V_{CEs}	α_{CEs}	V_{pt}
(unit)	($\Omega\,\mu\mathrm{m}^2$)	(1)	(mV)	(1/kK)	(V)
value	627	−2.37	87.3	142	2.45
parameter (HV)	V_{lim}	α_{vs}			
(unit)	(V)	(1/kK)			
value	0.268	2.03			
parameter (HV)	τ_{hcs}	a_{hc}	τ_{Ef0}	g_{tfe}	
(unit)	(ps)	(1)	(ps)	(1)	
value	498	0.0147	1.16	1.85	

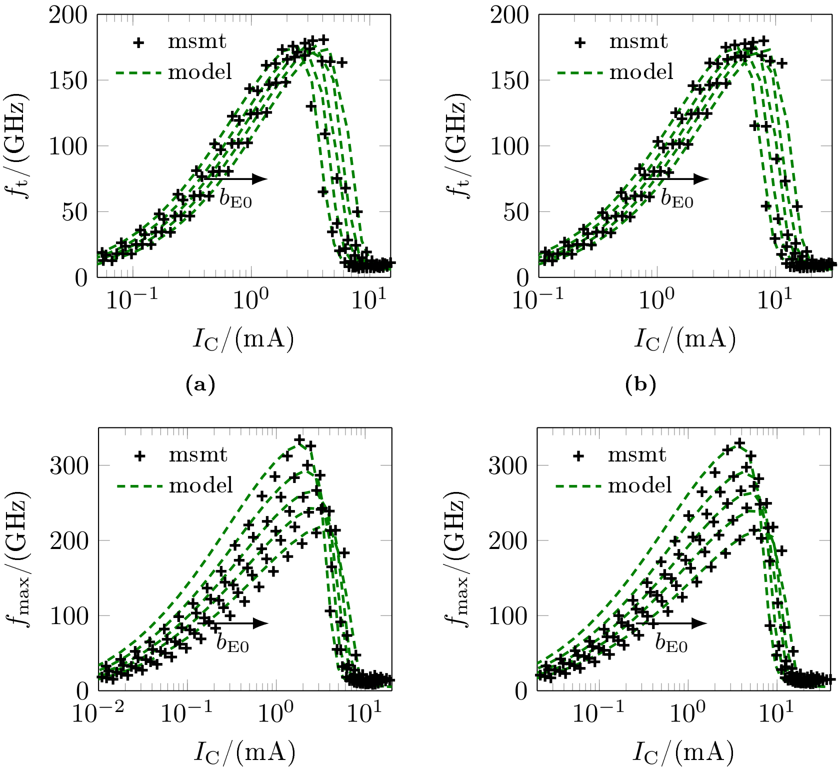
Table A.9: Extracted parameters of the transit time description of HICUM for the HV transistors of [76].



(a) **(b)**

(c) **(d)**

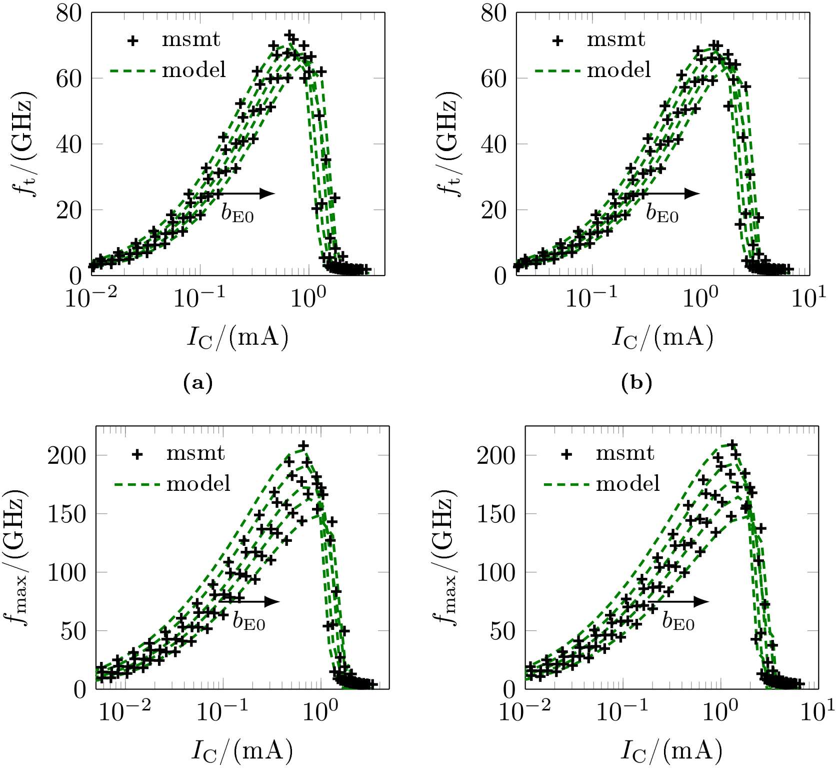
Figure A.2: Comparison of measurements and model for the transit frequency f_t (5 GHz extrapolation frequency) and the maximum oscillation frequency f_{max} (20 GHz extrapolation frequency) for different widths ($b_{drawn} = (180 \text{ to } 378)\,\mathrm{nm}$) at $T_{amb} = 25\,°\mathrm{C}$ and $V_{BC} = 0\,\mathrm{V}$ (HS transistors of [76]). **(a)** f_t vs. I_C for $l_{drawn} = 4.5\,\mu\mathrm{m}$. **(b)** f_t vs. I_C for $l_{drawn} = 9\,\mu\mathrm{m}$. **(c)** f_{max} vs. I_C for $l_{drawn} = 4.5\,\mu\mathrm{m}$. **(d)** f_{max} vs. I_C for $l_{drawn} = 9\,\mu\mathrm{m}$.



(a) **(b)**

(c) **(d)**

Figure A.3: Comparison of measurements and model for the transit frequency f_t (5 GHz extrapolation frequency) and the maximum oscillation frequency f_{max} (20 GHz extrapolation frequency) for different widths (b_{drawn} = (180 to 378) nm) at T_{amb} = 25 °C and V_{BC} = 0 V (MV transistors of [76]). **(a)** f_t vs. I_C for l_{drawn} = 4.5 µm. **(b)** f_t vs. I_C for l_{drawn} = 9 µm. **(c)** f_{max} vs. I_C for l_{drawn} = 4.5 µm. **(d)** f_{max} vs. I_C for l_{drawn} = 9 µm.



(a) **(b)**

(c) **(d)**

Figure A.4: Comparison of measurements and model for the transit frequency f_t (5 GHz extrapolation frequency) and the maximum oscillation frequency f_{max} (20 GHz extrapolation frequency) for different widths ($b_{drawn} = (180 \text{ to } 378)\,nm$) at $T_{amb} = 25\,°C$ and $V_{BC} = 0\,V$ (HV transistors of [76]). **(a)** f_t vs. I_C for $l_{drawn} = 4.5\,µm$. **(b)** f_t vs. I_C for $l_{drawn} = 9\,µm$. **(c)** f_{max} vs. I_C for $l_{drawn} = 4.5\,µm$. **(d)** f_{max} vs. I_C for $l_{drawn} = 9\,µm$.

A.5 Transfer current

The extracted parameters for the transfer current are listed in tables A.10, A.11, A.12 and A.13 for all three transistor flavors. Using the model, a comparison for the transfer current and normalized transfer current with measurements was performed, as illustrated in figures A.5, A.6 and A.7.

parameter (unit)	γ_{C0} (HS) (nm)	γ_{C0} (MV) (nm)	γ_{C0} (HV) (nm)
value	23.3	26.9	30.3

Table A.10: Extracted zero-bias values of γ_{C} for the HS, MV and HV transistors of [76].

parameter (HS) (unit)	$\bar{c}_{10}$ (fA fC/µm^2)	h_{jEi} (1)	h_{jEp} (1)	a_{hjEi} (1)	a_{hjEp} (1)
value	1.089	0.634	0.592	3.09	3.71
parameter (HS) (unit)	h_{jCi} (1)	r_{hjEi} (1)	h_{f0} (1)	h_{fE} (1)	h_{fC} (1)
value	0.109	2.55	7.6	0	0
parameter (HS) (unit)	ζ_{hjEi} (1)	ΔV_{gBE} (mV)	ζ_{VgBE} (1)	V_{gB} (V)	ζ_{CT} (1)
value	−1.53	−46.7	−0.360	1.011	3.08

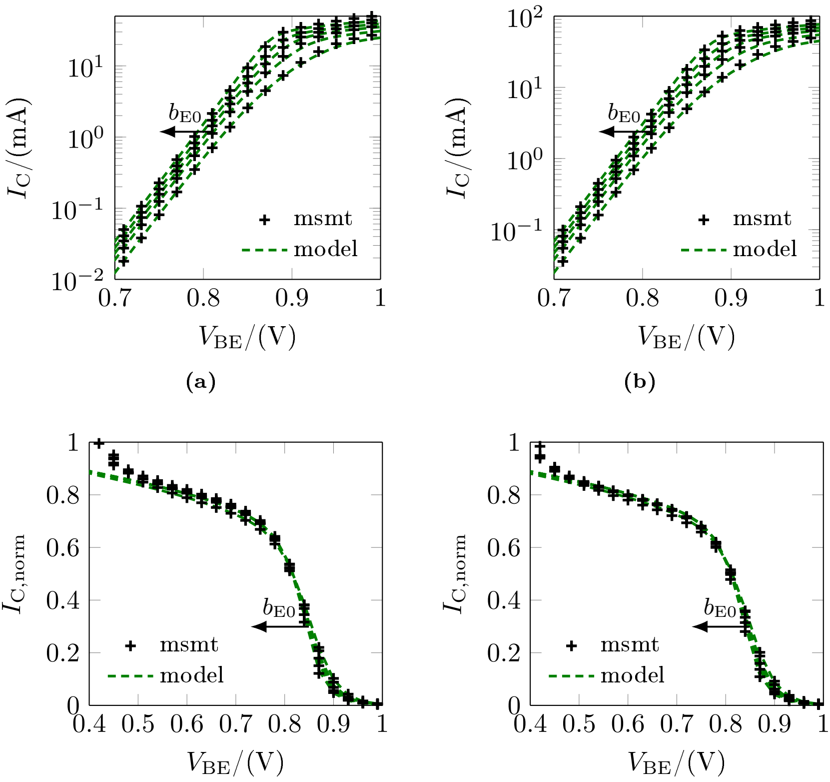
Table A.11: Extracted parameters of the transfer current description of HICUM for the HS transistors of [76].

parameter (MV) (unit)	$\bar{c}_{10}$ (fA fC/µm^2)	h_{jEi} (1)	h_{jEp} (1)	a_{hjEi} (1)	a_{hjEp} (1)
value	1.117	0.860	1.063	1.86	2.82
parameter (MV) (unit)	h_{jCi} (1)	r_{hjEi} (1)	h_{f0} (1)	h_{fE} (1)	h_{fC} (1)
value	0.159	1.07	5.74	0	2.25
parameter (MV) (unit)	ζ_{hjEi} (1)	ΔV_{gBE} (mV)	ζ_{VgBE} (1)	V_{gB} (V)	ζ_{CT} (1)
value	−1.30	−92.1	−0.206	0.998	3.53

Table A.12: Extracted parameters of the transfer current description of HICUM for the MV transistors of [76].

parameter (HV) (unit)	$\bar{c}_{10}$ (fA fC/µm^2)	h_{jEi} (1)	h_{jEp} (1)	a_{hjEi} (1)	a_{hjEp} (1)
value	1.123	0.567	0.812	3.87	4.42
parameter (HV) (unit)	h_{jCi} (1)	r_{hjEi} (1)	h_{f0} (1)	h_{fE} (1)	h_{fC} (1)
value	0.211	2.65	2.01	7.12	8.80
parameter (HV) (unit)	ζ_{hjEi} (1)	ΔV_{gBE} (mV)	ζ_{VgBE} (1)	V_{gB} (V)	ζ_{CT} (1)
value	−1.97	−98.7	−0.291	0.990	3.94

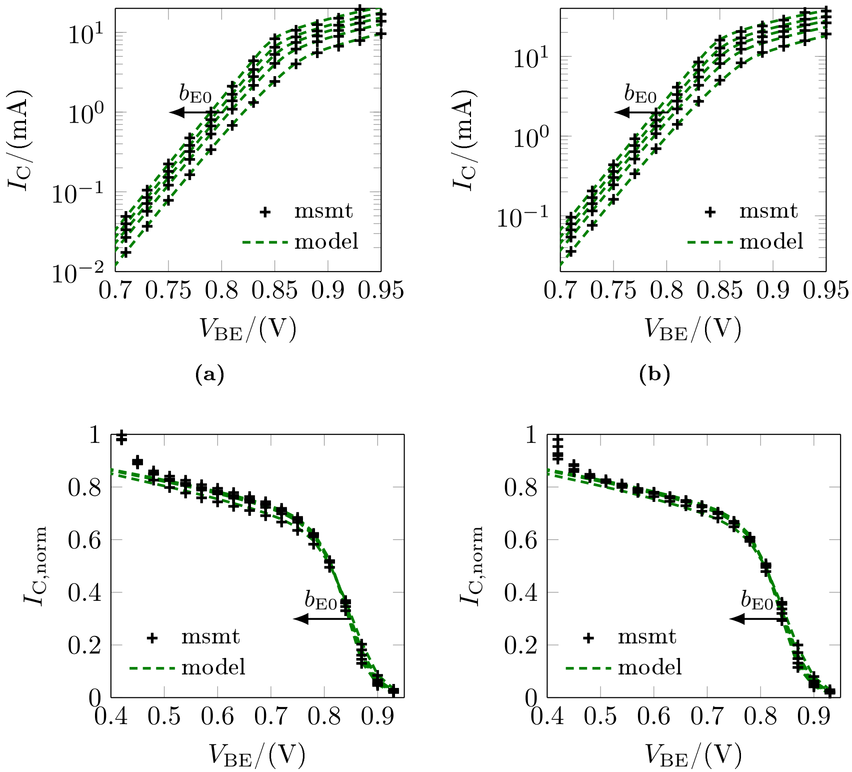
Table A.13: Extracted parameters of the transfer current description of HICUM for the HV transistors of [76].



(a) **(b)**

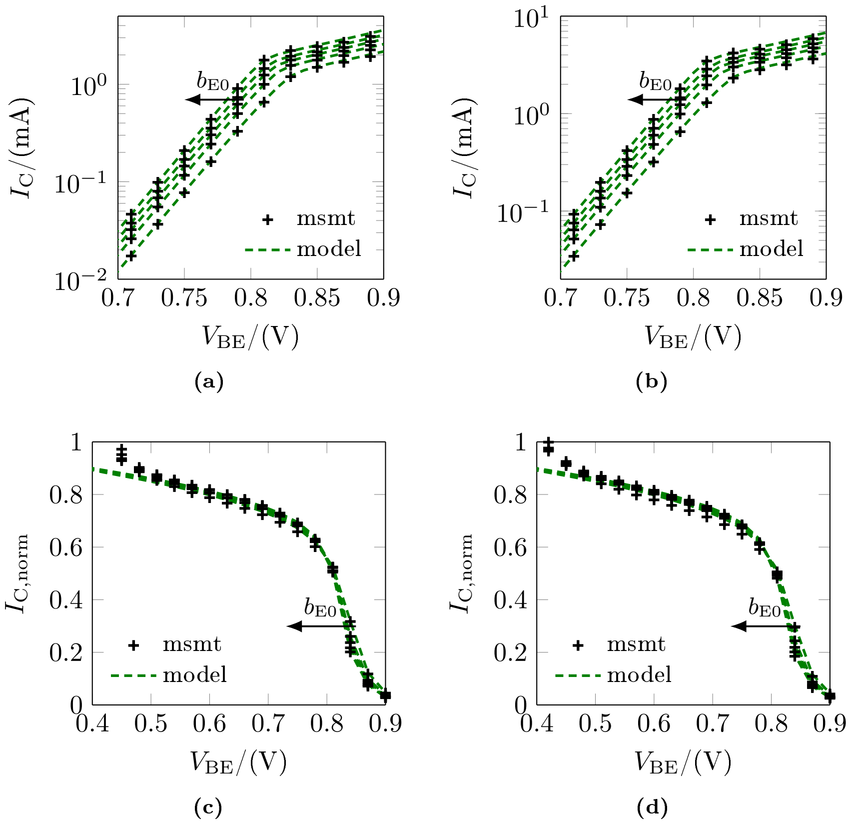
(c) **(d)**

Figure A.5: Comparison of measurements and model for the collector current I_C and the normalized collector current $I_{C,\mathrm{norm}}$ for different widths ($b_{\mathrm{drawn}} = (180 \text{ to } 378)\,\mathrm{nm}$) at $T_{\mathrm{amb}} = 25\,°\mathrm{C}$ and $V_{BC} = 0\,\mathrm{V}$ (HS transistors of [76]). **(a)** I_C vs. V_{BE} for $l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$. **(b)** I_C vs. V_{BE} for $l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$. **(c)** $I_{C,\mathrm{norm}}$ vs. V_{BE} for $l_{\mathrm{drawn}} = 4.5\,\mu\mathrm{m}$. **(d)** $I_{C,\mathrm{norm}}$ vs. V_{BE} for $l_{\mathrm{drawn}} = 9\,\mu\mathrm{m}$.



(a) **(b)** **(c)** **(d)**

Figure A.6: Comparison of measurements and model for the collector current I_C and the normalized collector current $I_{C,norm}$ for different widths (b_{drawn} = (180 to 378) nm) at T_{amb} = 25 °C and V_{BC} = 0 V (MV transistors of [76]). **(a)** I_C vs. V_{BE} for l_{drawn} = 4.5 µm. **(b)** I_C vs. V_{BE} for l_{drawn} = 9 µm. **(c)** $I_{C,norm}$ vs. V_{BE} for l_{drawn} = 4.5 µm. **(d)** $I_{C,norm}$ vs. V_{BE} for l_{drawn} = 9 µm.



(a) **(b)**

(c) **(d)**

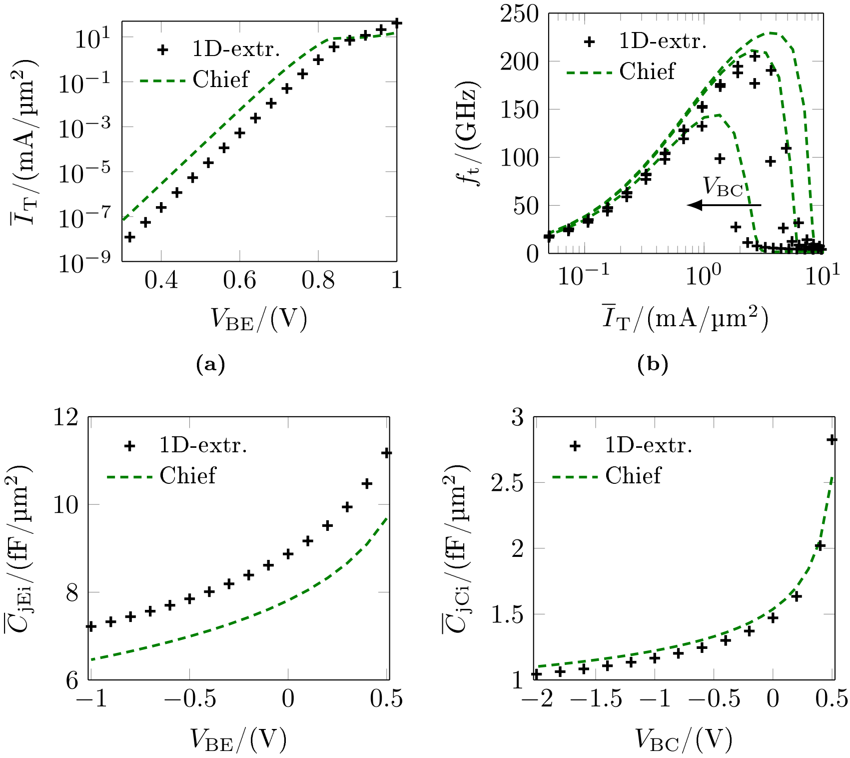
Figure A.7: Comparison of measurements and model for the collector current I_C and the normalized collector current $I_{C,norm}$ for different widths (b_{drawn} = (180 to 378) nm) at T_{amb} = 25 °C and V_{BC} = 0 V (HV transistors of [76]). **(a)** I_C vs. V_{BE} for l_{drawn} = 4.5 µm. **(b)** I_C vs. V_{BE} for l_{drawn} = 9 µm. **(c)** $I_{C,norm}$ vs. V_{BE} for l_{drawn} = 4.5 µm. **(d)** $I_{C,norm}$ vs. V_{BE} for l_{drawn} = 9 µm.

APPENDIX B

Supplementary profile calibration information

B.1 1D doping profile calibration

Figures B.1 and B.2 illustrate the initial comparison between the extracted 1D reference and device simulation using the process TCAD profiles for the MV and HV transistor versions, respectively.



(a) **(b)**

(c) **(d)**

Figure B.1: Initial comparison of the extracted 1D reference with HD simulations using the 1D profiles of process simulations (MV transistors of [76]). Results for **(a)** $\overline{I}_{\mathrm{T}}$ vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$, **(b)** f_{t} vs. $\overline{I}_{\mathrm{T}}$ for $V_{\mathrm{BC}} = (-0.5, 0 \text{ and } 0.5)\,\mathrm{V}$, **(c)** $\overline{C}_{\mathrm{jEi}}$ vs. V_{BE} and **(d)** $\overline{C}_{\mathrm{jCi}}$ vs. V_{BC}.

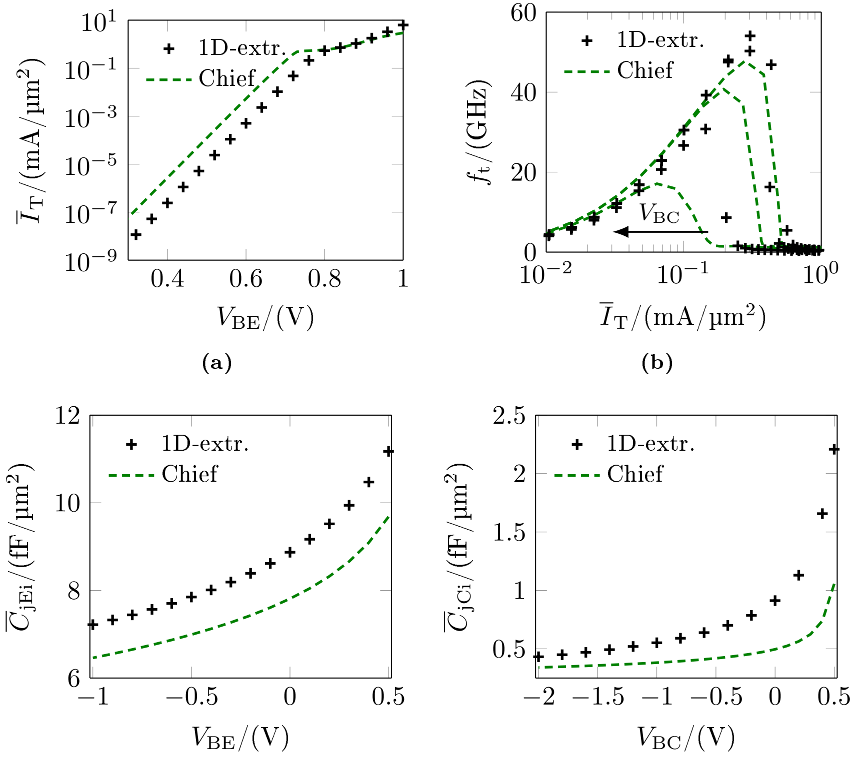


Figure B.2: Initial comparison of the extracted 1D reference with HD simulations using the 1D profiles of process simulations (HV transistors of [76]). Results for **(a)** $\overline{I}_{\mathrm{T}}$ vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$, **(b)** f_{t} vs. $\overline{I}_{\mathrm{T}}$ for $V_{\mathrm{BC}} = (-0.5, 0 \text{ and } 0.5)\,\mathrm{V}$, **(c)** $\overline{C}_{\mathrm{jEi}}$ vs. V_{BE} and **(d)** $\overline{C}_{\mathrm{jCi}}$ vs. V_{BC}.

APPENDIX C

Supplementary TCAD prediction information

C.1 1D simulation and extraction results (B55)

The extracted parameters of the HICUM description for the 1D simulations are listed in tables C.1, C.2 and C.3 for all three transistor flavors. Electrical and temperature related parameters were determined by HD and DD simulations, respectively. Using the compact model, a comparison for relevant characteristics with HD simulations was performed, as illustrated in figures C.1 and C.2 for the MV and HV versions. A comparison for different lattice temperatures is shown in figures C.3 and C.4.

parameter	$\overline{I}_{\mathrm{BEiS}}$	m_{BEi}	$\overline{I}_{\mathrm{BCiS}}$	m_{BCi}	ζ_{BET}
(unit)	(A/µm^2)	(1)	(A/µm^2)	(1)	(1)
value	$4.87 \cdot 10^{-20}$	1.019	$4.75 \cdot 10^{-20}$	1.011	4.0
parameter	$\overline{C}_{\mathrm{jEi0}}$	z_{Ei}	V_{dEi}	a_{jEi}	V_{gE}
(unit)	(fF/µm^2)	(1)	(V)	(1)	(V)
value	7.72	0.222	0.842	1.66	0.98
parameter	$\overline{C}_{\mathrm{jCi0}}$	z_{Ci}	V_{dCi}	$R_{\mathrm{s,Bi0}}$	V_{gC}
(unit)	(fF/µm^2)	(1)	(V)	(Ω/□)	(V)
value	2.61	0.288	0.656	5781	0.82
parameter	$\bar{c}_{10}$	$\overline{Q}_{\mathrm{p0}}$	h_{jEi}	a_{hjEi}	r_{hjEi}
(unit)	(fA fC/µm^2)	(fC/µm^2)	(1)	(1)	(1)
value	1.408	24.0	0.535	5.82	1.38
parameter	h_{jCi}	h_{f0}	h_{fE}	h_{fC}	
(unit)	(1)	(1)	(1)	(1)	
value	0.194	8.55	5.85	224	
parameter	τ_{0a}	τ_{bvl}	$\Delta\tau_{\mathrm{0h}}$	ρ_{Ci0}	V_{CEs}
(unit)	(fs)	(fs)	(fs)	(Ω µm^2)	(mV)
value	378.2	121.8	35.3	50.2	10.0
parameter	V_{pt}	V_{lim}	$f_{\tau\mathrm{hc}}$		
(unit)	(V)	(V)	(1)		
value	100	1.47	0.5		
parameter	τ_{hcs}	a_{hc}	τ_{Ef0}	g_{tfe}	
(unit)	(ps)	(1)	(ps)	(1)	
value	51.2	0.0030	0.45	2.85	
parameter	$\alpha_{\tau 0}$	$k_{\tau 0}$	ζ_{Ci}	α_{CEs}	α_{vs}
(unit)	(1/kK)	(1/MK^2)	(1)	(1/kK)	(1/kK)
value	1.80	1.38	−2.54	299	3.62
parameter	ζ_{hjEi}	ΔV_{gBE}	ζ_{VgBE}	V_{gB}	ζ_{CT}
(unit)	(1)	(mV)	(1)	(V)	(1)
value	−2.45	−48.9	−0.437	0.96	1.23

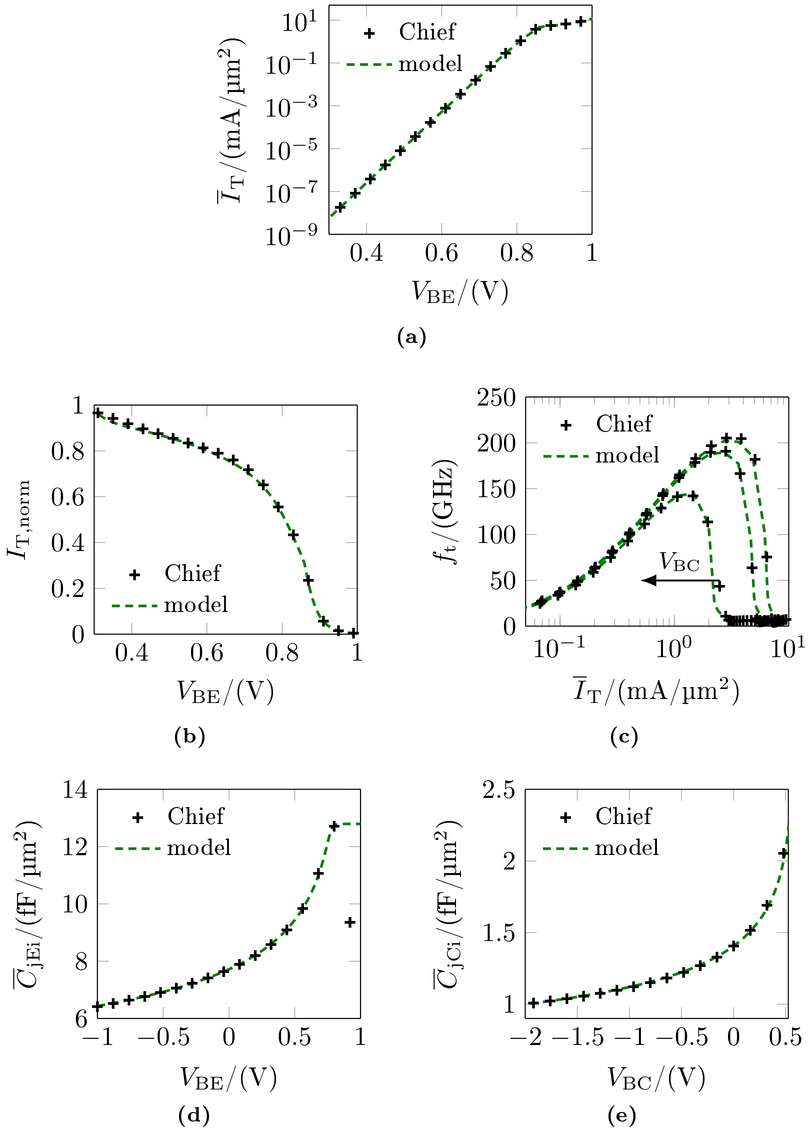
Table C.1: Extracted parameters of the HICUM description for the 1D simulations of the HS transistors (process of [76]).

parameter	$\overline{I}_{\mathrm{BEiS}}$	m_{BEi}	$\overline{I}_{\mathrm{BCiS}}$	m_{BCi}	ζ_{BET}
(unit)	(A/µm^2)	(1)	(A/µm^2)	(1)	(1)
value	$5.11 \cdot 10^{-20}$	1.019	$4.60 \cdot 10^{-20}$	1.009	4.0
parameter	$\overline{C}_{\mathrm{jEi0}}$	z_{Ei}	V_{dEi}	a_{jEi}	V_{gE}
(unit)	(fF/µm^2)	(1)	(V)	(1)	(V)
value	7.72	0.224	0.844	1.58	0.97
parameter	$\overline{C}_{\mathrm{jCi0}}$	z_{Ci}	V_{dCi}	$R_{\mathrm{s,Bi0}}$	V_{gC}
(unit)	(fF/µm^2)	(1)	(V)	(Ω/□)	(V)
value	1.41	0.238	0.624	5089	0.79
parameter	$\overline{c}_{10}$	$\overline{Q}_{\mathrm{p0}}$	h_{jEi}	a_{hjEi}	r_{hjEi}
(unit)	(fA fC/µm^2)	(fC/µm^2)	(1)	(1)	(1)
value	1.395	25.6	0.533	5.71	1.42
parameter	h_{jCi}	h_{f0}	h_{fE}	h_{fC}	
(unit)	(1)	(1)	(1)	(1)	
value	0.197	7.01	0	105	
parameter	τ_{0a}	τ_{bvl}	$\Delta\tau_{\mathrm{0h}}$	ρ_{Ci0}	V_{CEs}
(unit)	(fs)	(fs)	(fs)	(Ω µm^2)	(mV)
value	594.0	123.1	68.8	152.2	10.0
parameter	V_{pt}	V_{lim}	$f_{\tau\mathrm{hc}}$		
(unit)	(V)	(V)	(1)		
value	100	1.30	0.5		
parameter	τ_{hcs}	a_{hc}	τ_{Ef0}	g_{tfe}	
(unit)	(ps)	(1)	(ps)	(1)	
value	40.7	0.0023	0.37	3.00	
parameter	$\alpha_{\tau 0}$	$k_{\tau 0}$	ζ_{Ci}	α_{CEs}	α_{vs}
(unit)	(1/kK)	(1/MK^2)	(1)	(1/kK)	(1/kK)
value	1.68	-1.49	-3.77	583	0.552
parameter	ζ_{hjEi}	ΔV_{gBE}	ζ_{VgBE}	V_{gB}	ζ_{CT}
(unit)	(1)	(mV)	(1)	(V)	(1)
value	-1.54	-223	-0.040	0.96	1.23

Table C.2: Extracted parameters of the HICUM description for the 1D simulations of the MV transistors (process of [76]).

parameter	$\overline{I}_{\mathrm{BEiS}}$	m_{BEi}	$\overline{I}_{\mathrm{BCiS}}$	m_{BCi}	ζ_{BET}
(unit)	$(\mathrm{A}/\mu\mathrm{m}^2)$	(1)	$(\mathrm{A}/\mu\mathrm{m}^2)$	(1)	(1)
value	$5.25 \cdot 10^{-20}$	1.019	$2.24 \cdot 10^{-19}$	1.025	4.0
parameter	$\overline{C}_{\mathrm{jCi0}}$	z_{Ci}	V_{dCi}	a_{jEi}	V_{gE}
(unit)	$(\mathrm{fF}/\mu\mathrm{m}^2)$	(1)	(V)	(1)	(V)
value	0.845	0.501	0.666	1.45	0.97
parameter	$\overline{C}_{\mathrm{jEi0}}$	z_{Ei}	V_{dEi}	$R_{\mathrm{s,Bi0}}$	V_{gC}
(unit)	$(\mathrm{fF}/\mu\mathrm{m}^2)$	(1)	(V)	$(\Omega/\square)$	(V)
value	7.71	0.226	0.851	5034	0.94
parameter	$\bar{c}_{10}$	$\overline{Q}_{\mathrm{p0}}$	h_{jEi}	a_{hjEi}	r_{hjEi}
(unit)	$(\mathrm{fA\,fC}/\mu\mathrm{m}^2)$	$(\mathrm{fC}/\mu\mathrm{m}^2)$	(1)	(1)	(1)
value	1.359	25.9	0.485	6.10	3.5
parameter	h_{jCi}	h_{f0}	h_{fE}	h_{fC}	
(unit)	(1)	(1)	(1)	(1)	
value	0.522	6.70	0	178	
parameter	τ_{0a}	τ_{bvl}	$\Delta\tau_{\mathrm{0h}}$	ρ_{Ci0}	V_{CEs}
(unit)	(ps)	(ps)	(ps)	$(\Omega\,\mu\mathrm{m}^2)$	(mV)
value	1.633	1.153	0.802	1127	10.0
parameter	V_{pt}	V_{lim}	$f_{\tau\mathrm{hc}}$		
(unit)	(V)	(V)	(1)		
value	100	0.927	0.5		
parameter	τ_{hcs}	a_{hc}	τ_{Ef0}	g_{tfe}	
(unit)	(ps)	(1)	(ps)	(1)	
value	241	0.0025	2.09	2.90	
parameter	$\alpha_{\tau 0}$	$k_{\tau 0}$	ζ_{Ci}	α_{CEs}	α_{vs}
(unit)	(1/kK)	$(1/\mathrm{MK}^2)$	(1)	(1/kK)	(1/kK)
value	3.50	5.08	−2.89	148	7.03
parameter	ζ_{hjEi}	ΔV_{gBE}	ζ_{VgBE}	V_{gB}	ζ_{CT}
(unit)	(1)	(mV)	(1)	(V)	(1)
value	−1.26	−140	−0.034	0.96	1.22

Table C.3: Extracted parameters of the HICUM description for the 1D simulations of the HV transistors (process of [76]).

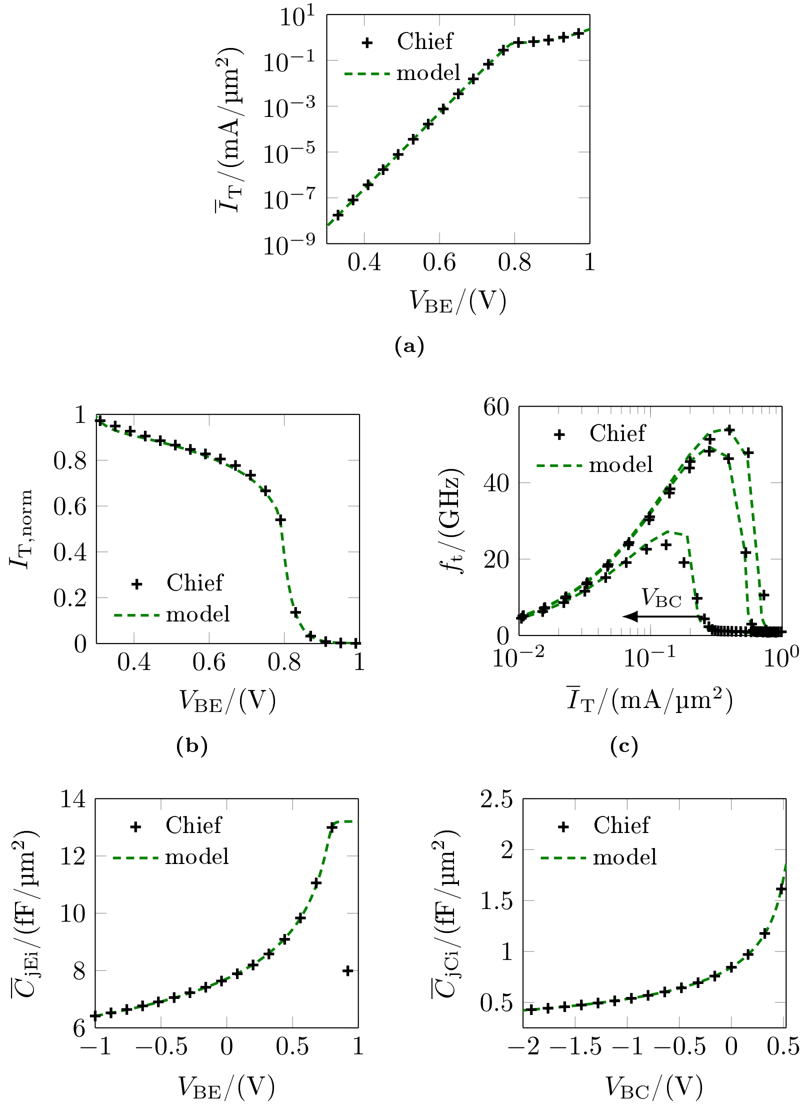


(a)

(b) **(c)**

(d) **(e)**

Figure C.1: Comparison of HD simulations for the 1D profile with the extracted model based on HICUM for the MV transistors of [76]. Results for **(a)** $\overline{I}_{\mathrm{T}}$ vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$, **(b)** $I_{\mathrm{T,norm}}$ vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$, **(c)** f_{t} vs. $\overline{I}_{\mathrm{T}}$ for $V_{\mathrm{BC}} = (-0.5, 0 \text{ and } 0.5)\,\mathrm{V}$, **(d)** $\overline{C}_{\mathrm{jEi}}$ vs. V_{BE} and **(e)** $\overline{C}_{\mathrm{jCi}}$ vs. V_{BC}.



(a)

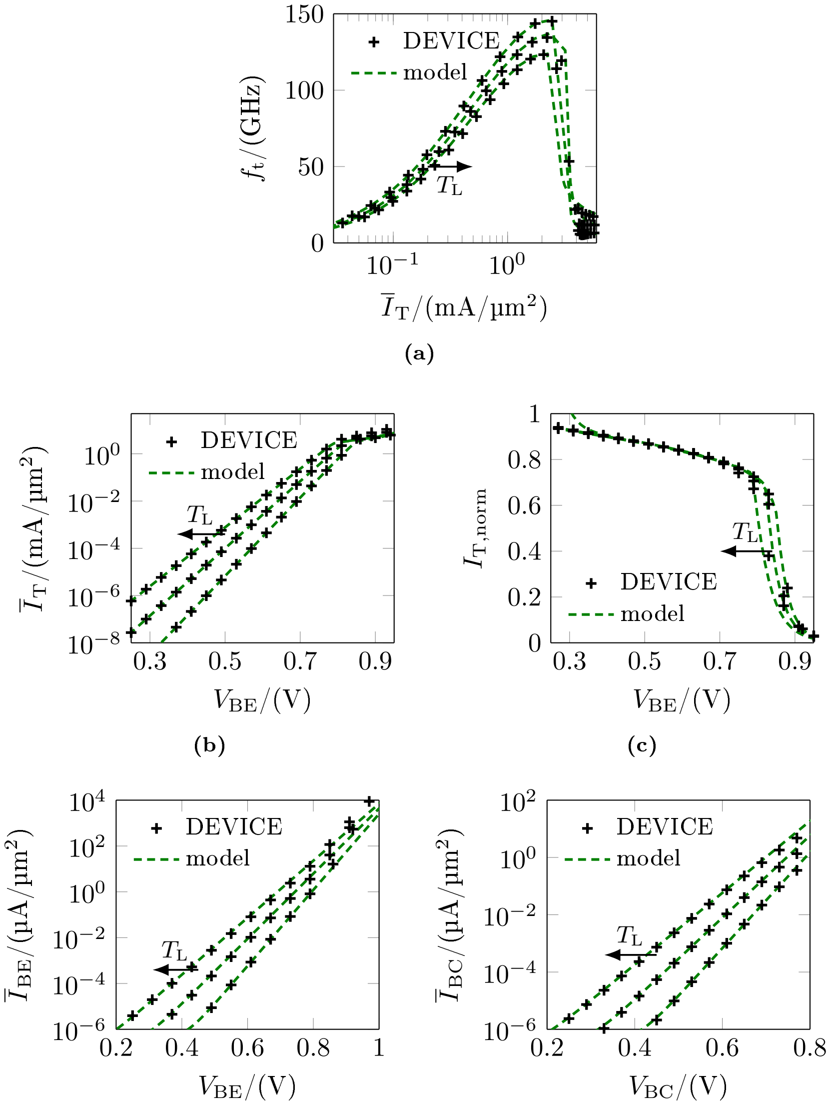
(b)

(c)

(d)

(e)

Figure C.2: Comparison of HD simulations for the 1D profile with the extracted model based on HICUM for the HV transistors of [76]. Results for **(a)** $\overline{I}_{\mathrm{T}}$ vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$, **(b)** $I_{\mathrm{T,norm}}$ vs. V_{BE} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$, **(c)** f_{t} vs. $\overline{I}_{\mathrm{T}}$ for $V_{\mathrm{BC}} = (-0.5, 0 \text{ and } 0.5)\,\mathrm{V}$, **(d)** $\overline{C}_{\mathrm{jEi}}$ vs. V_{BE} and **(e)** $\overline{C}_{\mathrm{jCi}}$ vs. V_{BC}.

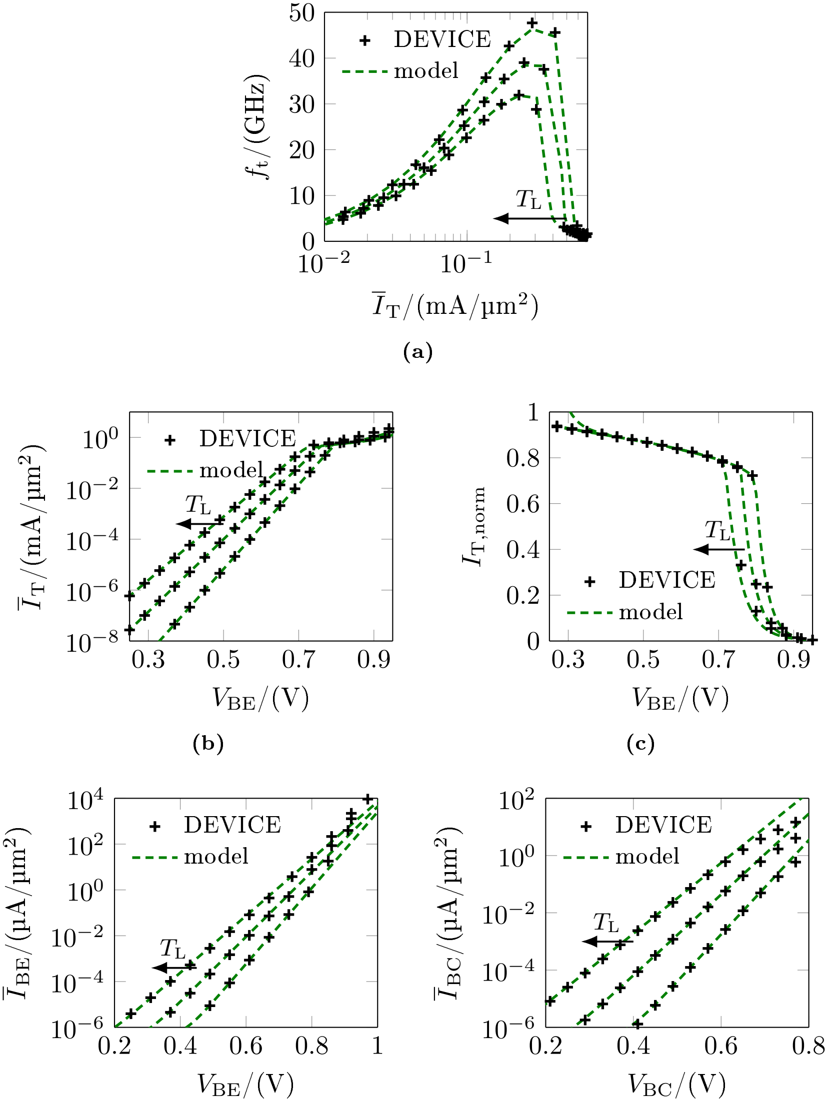


(a)

(b) **(c)**

(d) **(e)**

Figure C.3: Comparison of DD simulations for the 1D profile with the corresponding extracted model based on HICUM for the MV transistors of [76]. Results for **(a)** f_t vs. $\overline{I}_T$, **(b)** $\overline{I}_T$ vs. V_{BE}, **(c)** $I_{T,norm}$ vs. V_{BE}, **(d)** $\overline{I}_{BE}$ vs. V_{BE} and **(e)** $\overline{I}_{BC}$ vs. V_{BC} for different lattice temperatures ($T_L = (300, 350 \text{ and } 400)\,\mathrm{K}$).



(a)

(b) **(c)**

(d) **(e)**

Figure C.4: Comparison of DD simulations for the 1D profile with the corresponding extracted model based on HICUM for the HV transistors of [76]. Results for **(a)** f_t vs. $\overline{I}_T$, **(b)** $\overline{I}_T$ vs. V_{BE}, **(c)** $I_{T,norm}$ vs. V_{BE}, **(d)** $\overline{I}_{BE}$ vs. V_{BE} and **(e)** $\overline{I}_{BC}$ vs. V_{BC} for different lattice temperatures ($T_L = (300, 350 \text{ and } 400)\,\mathrm{K}$).

C.2 Model parameters and additional information of the prediction approach (B28)

The extracted parameters of the HICUM description for the 1D simulations are listed in table C.5. Electrical and temperature related parameters were determined by HD and DD simulations, respectively. The 2D model results are presented in table C.4.

The parameter values for R_{Cx}, R_{Bx} and R_{Bi0} obtained by device simulation based on technology-specific sheet and contact resistances are listed in tables C.6, C.7 and C.8, respectively.

parameter (unit)	γ_{C0} (nm)	δ_{C} (°)	I'_{BEpS} (A/µm)	I'_{BCxS} (A/µm)
value (sim.)	19.8	1.6	$1.36 \cdot 10^{-20}$	$4.74 \cdot 10^{-20}$
parameter (unit)	C'_{jEp0} (fF/µm)	C'_{jCx0} (fF/µm)	$f_{\tau\mathrm{pi}}$ (1)	
value (sim.)	0.064	0.140	1.28	

Table C.4: Results for important 2D parameters obtained by extraction on DD simulations for the future process technology of [130].

parameter	$\overline{I}_{\mathrm{BEiS}}$	m_{BEi}	$\overline{I}_{\mathrm{BCiS}}$	m_{BCi}	ζ_{BET}
(unit)	(A/µm^2)	(1)	(A/µm^2)	(1)	(1)
value	$4.94 \cdot 10^{-20}$	1.013	$5.49 \cdot 10^{-20}$	1.009	4.0
parameter	$\overline{C}_{\mathrm{jEi0}}$	z_{Ei}	V_{dEi}	a_{jEi}	V_{gE}
(unit)	(fF/µm^2)	(1)	(V)	(1)	(V)
value	7.97	0.180	0.825	1.85	0.96
parameter	$\overline{C}_{\mathrm{jCi0}}$	z_{Ci}	V_{dCi}	$R_{\mathrm{s,Bi0}}$	V_{gC}
(unit)	(fF/µm^2)	(1)	(V)	(Ω/□)	(V)
value	4.43	0.218	0.710	5650	1.00
parameter	$\bar{c}_{10}$	$\overline{Q}_{\mathrm{p0}}$	h_{jEi}	a_{hjEi}	r_{hjEi}
(unit)	(fA fC/µm^2)	(fC/µm^2)	(1)	(1)	(1)
value	1.582	26.8	0.617	5.61	1.26
parameter	h_{jCi}	h_{f0}	h_{fE}	h_{fC}	
(unit)	(1)	(1)	(1)	(1)	
value	0.241	14.7	120	664	
parameter	τ_{0a}	τ_{bvl}	$\Delta\tau_{\mathrm{0h}}$	ρ_{Ci0}	V_{CEs}
(unit)	(fs)	(fs)	(fs)	(Ω µm^2)	(mV)
value	193.1	73.1	16.1	9.45	10.0
parameter	V_{pt}	V_{lim}	$f_{\tau\mathrm{hc}}$		
(unit)	(V)	(V)	(1)		
value	100	1.37	0.5		
parameter	τ_{hcs}	a_{hc}	τ_{Ef0}	g_{tfe}	
(unit)	(ps)	(1)	(ps)	(1)	
value	25.8	0.0032	0.63	2.14	
parameter	$\alpha_{\tau 0}$	$k_{\tau 0}$	ζ_{Ci}	α_{CEs}	α_{vs}
(unit)	(1/kK)	(1/MK^2)	(1)	(1/K)	(1/kK)
value	1.14	6.49	3.50	-1.53	-0.28
parameter	ζ_{hjEi}	ΔV_{gBE}	ζ_{VgBE}	V_{gB}	ζ_{CT}
(unit)	(1)	(mV)	(1)	(V)	(1)
value	-2.37	-82.1	-0.192	0.95	1.30

Table C.5: Extracted parameters of the HICUM description for the 1D simulations of the future process technology [130].

R_{Cx}/Ω	$l_{\mathrm{E0}} = 4.5\,\mu\mathrm{m}$	$l_{\mathrm{E0}} = 9\,\mu\mathrm{m}$
$b_{\mathrm{E0}} = 64\,\mathrm{nm}$	9.79	4.98
$b_{\mathrm{E0}} = 96\,\mathrm{nm}$	9.87	5.02
$b_{\mathrm{E0}} = 128\,\mathrm{nm}$	9.94	5.06
$b_{\mathrm{E0}} = 160\,\mathrm{nm}$	10.0	5.10
$b_{\mathrm{E0}} = 192\,\mathrm{nm}$	10.1	5.14

Table C.6: Simulation results for the external collector resistance R_{Cx} for the future process technology of [130]. The results use technology specific resistances of the TCAD based calculations of section 5.3.1.

R_{Bx}/Ω	$l_{\mathrm{E0}} = 4.5\,\mu\mathrm{m}$	$l_{\mathrm{E0}} = 9\,\mu\mathrm{m}$
$b_{\mathrm{E0}} = 64\,\mathrm{nm}$	20.8	10.6
$b_{\mathrm{E0}} = 96\,\mathrm{nm}$	20.6	10.6
$b_{\mathrm{E0}} = 128\,\mathrm{nm}$	20.5	10.5
$b_{\mathrm{E0}} = 160\,\mathrm{nm}$	20.4	10.5
$b_{\mathrm{E0}} = 192\,\mathrm{nm}$	20.2	10.4

Table C.7: Quasi-3D simulation results for the external base resistance R_{Bx} for the future process technology of [130]. The results use technology specific resistances of the TCAD based calculations of section 5.3.1.

R_{Bi0}/Ω	$l_{\mathrm{E0}} = 4.5\,\mu\mathrm{m}$	$l_{\mathrm{E0}} = 9\,\mu\mathrm{m}$
$b_{\mathrm{E0}} = 64\,\mathrm{nm}$	8.92	4.47
$b_{\mathrm{E0}} = 96\,\mathrm{nm}$	12.0	6.02
$b_{\mathrm{E0}} = 128\,\mathrm{nm}$	15.1	7.59
$b_{\mathrm{E0}} = 160\,\mathrm{nm}$	18.2	9.17
$b_{\mathrm{E0}} = 192\,\mathrm{nm}$	21.2	10.7

Table C.8: Quasi-3D simulation results for the internal zero-bias base resistance R_{Bi0} for the future process technology of [130]. The results use technology specific resistances of the TCAD based calculations of section 5.3.1.

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