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Methodology for Substrate Parasitic Modeling in HV/HT Smart Power Technology - Application to Automotive Industry

Hao Zou

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THÈSE DE DOCTORAT DE L'UNIVERSITÉ PIERRE ET MARIE CURIE

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Présentée par

Hao ZOU

Pour obtenir le grade de

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Devant le jury composé de

| | | |
|---------------------------|-------------------------------|-----------------------|
| PR. Bruno ALLARD | INSA Lyon | Rapporteur |
| PR. Pascal NOUET | Université Montpellier, LIRMM | Rapporteur |
| PR. Etienne SICARD | INSA Toulouse | Examineur |
| M. Ehrenfried SEEBACHER | ams AG | Examineur |
| Dr. Pierre TISSERAND | Valeo | Examineur |
| PR. Habib MEHREZ | UPMC, LIP6 | Examineur |
| Dr. Marie-Minerve LOUËRAT | CNRS, LIP6 | Directrice de Thèse |
| Dr. Ramy ISKANDER | UPMC, LIP6 | Co-directeur de Thèse |
| Dr. Thomas GNEITING | AdMOS | Invited |



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Doctoral School of Computer Science, Telecommunications and Electronics

Presented by

Hao ZOU

To obtain the degree of

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Thesis title

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Smart Power Technology - Application to Automotive Industry**

Defended in **December 12th 2016**

In front of jury composed of

| | | |
|---------------------------|-------------------------------|---------------|
| PR. Bruno ALLARD | INSA Lyon | Reviewer |
| PR. Pascal NOUET | Université Montpellier, LIRMM | Reviewer |
| PR. Etienne SICARD | INSA Toulouse | Examinator |
| M. Ehrenfried SEEBACHER | ams AG | Examinator |
| Dr. Pierre TISSERAND | Valeo | Examinator |
| PR. Habib MEHREZ | UPMC, LIP6 | Examinator |
| Dr. Marie-Minerve LOUËRAT | CNRS, LIP6 | Supervisor |
| Dr. Ramy ISKANDER | UPMC, LIP6 | Co-Supervisor |
| Dr. Thomas GNEITING | AdMOS | Invited |

Every day is a new day. It is better to be lucky. But I would rather be exact. Then when luck comes you are ready.

- Ernest Hemingway, The old man and the sea

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*Hao ZOU
Paris, France
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Abstract

Smart Power Integrated Circuits (ICs) are intensively used in automotive embedded systems due to their unique capabilities to merge low power and high voltage (HV) devices on the same chip. In such systems, induced electrical coupling noise due to switching of the power stages is a big issue. During switching, parasitic voltages and currents, lead to a local shift of substrate potential that can reach hundreds of millivolts, and can severely disturb low voltage circuits. Such parasitic signals are known to represent the major cause of failure and costly circuit redesign in power ICs. Most solutions are layout dependent and are thus difficult to optimize using available electrical simulator. The lack for a model strategy prohibits an efficient design strategy and fails at giving clear predictions of perturbations in HV ICs.

In this thesis, we present a post-layout extraction and simulation methodology for substrate parasitic modeling. We have developed a Computer-Aided-Design (CAD) tool for substrate extraction from layout patterns. The extraction employs a meshing algorithm for substrate model generation. The behavior of the substrate currents can be taken into account in post-layout simulation, and enables an exhaustive failure analysis due to substrate coupling. Several industrial test cases are considered to validate this work, the interference of substrate currents in a current mirror configuration, and a standard automotive test in *ams AG* technology. This methodology is also applied to a HV BCD technology of *STMicroelectronics*. Eventually, by using the proposed CAD tool, it becomes possible to simulate the behaviors of substrate noises before fabrication.

Key words: substrate parasitic, modeling, simulation, noise coupling, meshing, high voltage CMOS

Résumé

Les circuits intégrés (CI) de puissance sont utilisés dans les systèmes embarqués automobiles en raison de leur capacité à réunir sur la même puce des dispositifs basse tension et haute tension (HV). Dans de tels systèmes, le bruit de couplage électrique induit par la commutation des étages de puissance est un problème majeur. Pendant la commutation, les tensions et les courants parasites produisent un décalage local de la tension de substrat allant jusqu'à une centaine de millivolt, perturbant ainsi le circuit basse tension. Ces signaux parasites entraînent des dysfonctionnements. Les solutions existantes reposent sur le dessin de masque et sont difficiles à optimiser par simulation électrique. L'absence d'une stratégie de modélisation interdit de fait une stratégie de conception s'appuyant sur la prédiction de ces perturbations.

Nous présentons ici une méthode d'extraction et de simulation post-layout pour la modélisation des parasites de substrats. Nous avons développé un logiciel (CAO) pour l'extraction du substrat fondé sur la génération du modèle du substrat. Les courants de substrat peuvent être pris en compte lors de la simulation post-layout, autorisant l'analyse des dysfonctionnements éventuels induits par les couplages à travers le substrat. Ce travail a été validé par plusieurs cas d'études industriels, une configuration en mirror de courant, et un test automobile standard en technologie *ams AG*. Cette méthodologie est aussi appliquée à une technologie HV BCD de *STMicroelectronics*. Ainsi, en utilisant notre approche, il devient possible de simuler des bruits de substrat avant fabrication.

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List of Abbreviations

| Abbreviation | Description |
|--------------|--|
| ADC | Analog-to-Digital Converter |
| API | Application Programming Interface |
| ASIC | Application Specific IC |
| BCD | Bipolar-CMOS-DMOS |
| CAD | Computer-Aided Design |
| CMOS | Complementary MOS |
| DAC | Digital-to-Analog Converter |
| DC | Direct current |
| DMOS | Double diffused MOS |
| EDA | Electronic Design Automation |
| EMI | Electromagnetic Interference |
| EEPROM | Electrically Erasable Programmable ROM |
| EPROM | Erasable Programmable ROM |
| ESD | Electrostatic discharges |
| FEM | Finit Element Method |
| FET | Field-Effect Transistor |
| FEV | Fully Electrical Vehicle |
| HV | High Voltage |
| HT | High Temperature |
| IC | Integrated Circuit |
| IGBT | Insulated Gate Bipolar Transistor |
| I/O | Input/Output |
| IoT | Internet of Things |
| IP | Intellectual Property |
| LDMOS | Lateral Diffused MOS |
| LIP6 | Laboratoire d'Informatique de Paris 6 |
| LV | Low Voltage |

| Abbreviation | Description |
|--------------|---|
| MOSFET | Metal-Oxide-Semiconductor Field Effect Transistor |
| NMOS | N-type MOS |
| PMOS | P-type MOS |
| PWM | Pulse Width Modulation |
| RAM | Random-Access Memory |
| RT | Room Temperature |
| ROM | Random-Access Memory |
| RF | Radio Frequency |
| SCR | Semiconductor-Controlled Rectifier |
| SoC | System-on-Chip |
| SOI | Silicon On Insulator |
| SW | SoftWare |
| TCAD | Technology Computer-Aided-Design |
| VDMOS | Vertical Diffused MOS |

Résumé Étendu en Français

Ce chapitre est un résumé étendu de la thèse, en français. Le lecteur intéressé par plus de détails pourra commencer directement la lecture au chapitre suivant.

Le couplage électronique à travers le substrat est l'une des principales causes de panne des circuits intégrés Haute-Tension (HV) et Haute-Température (HT) qui force à répéter à plusieurs reprises les étapes de conception et fabrication de ces circuits et augmente le coût global du produit réalisé. Cette situation fait apparaître le besoin d'analyse des causes de défaillance des circuits HV-HT pour identifier celles qui sont dues au couplage par le substrat. Dans cette thèse, nous présentons une méthodologie de modélisation des parasites du substrat fondée sur une extraction post-layout, en vue de la simulation électrique au niveau transistor et de l'analyse de la robustesse du circuit au couplage par le substrat. Sur la base de cette méthodologie, nous avons développé un outil de CAO dédié qui est utilisé pour l'extraction du substrat à partir du dessin des masques (layout). L'extraction repose sur un algorithme de maillage pour la génération des parasites du substrat. Pour valider le modèle du substrat, nous avons utilisé un processus de calibration qui s'appuie sur des circuits intégrés en technologie HV CMOS $0.35\mu\text{m}$. Pour illustrer la pertinence de notre approche, nous présenterons deux cas test en simulation transitoire. Le premier est un miroir de courant. Nous verrons que notre outil d'extraction couplé à un simulateur électrique au niveau transistor (type SPICE) permet d'estimer l'impact des courants de substrat sur le circuit initial avant la fabrication. Le second cas test est un circuit intégré industriel où le couplage par les parasites de substrat apparaît lors d'un test automobile standard. Ainsi nous montrons qu'en utilisant l'outil de CAO proposé, il devient possible de simuler l'impact du couplage de substrat sur la robustesse du circuit avant sa fabrication.

Introduction

La tendance actuelle de la microélectronique est d'intégrer plus de fonctionnalités sur une seule puce, ce qui réduit le coût et le nombre total de composants externes. Cette intégration augmente la fiabilité et réduit les interférences électromagnétiques (EMI) de l'ensemble du système. On trouve également cette approche dans le cas des circuits intégrés (IC) HV, où les dispositifs de puissance (HV), les dispositifs analogiques sous basse tension (LV) et les sous-systèmes numériques (LV)

coexistent sur le même substrat de silicium.

Dans un circuit HV typique, l'étage de puissance est couramment utilisé pour piloter des charges inductives, par exemple un moteur. Lors de la commutation de l'étage de puissance, la tension de drain des transistors passe en dessous de la tension d'alimentation négative ou au-dessus de la tension d'alimentation positive, ce qui induit des sources de courants parasites dans le substrat. Les courants de substrat ainsi créés conduisent à un changement local de potentiel de substrat pouvant atteindre des centaines de millivolts. Ces variations de potentiel de substrat induisent à leur tour le couplage entre les nombreuses diodes de jonctions PN présentes et rendent possible l'activation du transistor à jonction bipolaire (BJT) NPN distribué entre les puits et le substrat (Nwell/substrat-P/Nwell). Les trajets des courants de substrat induits dépendent du layout et atteignent des longueurs considérables.

Contrairement aux circuits intégrés (IC) basse tension (LV) en technologie CMOS standard, les circuits intégrés de puissance doivent résister à des conditions environnementales difficiles comme des températures de fonctionnement très élevées. Dans de telles conditions, le couplage par les bruits de substrat devient pire encore. Conformément aux tendances des technologies d'intégration sur silicium, les dispositifs HV voient leurs dimensions augmenter pour offrir plus de puissance, alors que les dispositifs numériques LV voient leurs dimensions diminuer pour offrir une fréquence de fonctionnement plus élevée et réduire la consommation d'énergie. Par conséquent, il devient de plus en plus difficile d'assurer l'immunité des blocs LV contre les couplages parasites issus des blocs HV. Le bruit de couplage détériore les fonctionnalités normales du système et compromet ses performances. De plus, l'activation éventuelle de transistors BJT parasites peut entraîner des effets destructeurs tels que le déclenchement du latch-up.

Les défaillances dues à un couplage du substrat par les transistors bipolaires NPN latéraux forcent à répéter plusieurs fois les étapes du cycle de conception et fabrication du circuit complet HV/LV. Comme on voit toujours des pannes se reproduire lors d'essais après fabrication, il devient crucial d'aborder l'analyse fine de ces problèmes sur un circuit complet. Il est très difficile de réaliser actuellement cette analyse du fait que d'une part, la conception d'IC conventionnelle ignore les effets des porteurs minoritaires dans le substrat, alors que les effets dus à l'injection et à la propagation dans le substrat des porteurs (majoritaires et minoritaires) sont significatifs dans les IC HV/LV. D'autre part, l'impact des porteurs minoritaires ne peut pas être modélisé par un modèle compact, puisque la modélisation compacte standard ne peut pas prendre en compte la propagation des porteurs minoritaires entre deux jonctions P/N.

Les outils de simulation fine de dispositif technologique (Technologie Computer-Aided-Design - TCAD) [5] sont considérés comme la seule façon d'analyser les effets induits par la propagation des porteurs minoritaires. Un tel simulateur de dispositif physique résout les systèmes d'équations 2D ou 3D par la méthode des éléments finis (FEM). Il produit des résultats fiables, mais exige un

temps de calcul considérable. Des études précédentes ont porté sur la modélisation des transistors latéraux parasites du substrat (BJT NPN) en utilisant des simulations TCAD. Elles donnent des résultats en accord avec les mesures. Cependant, la méthode n'est pas applicable pour un circuit complet car le temps de calcul est trop important (plusieurs heures sont nécessaires pour un seul dispositif), et elle nécessite une réduction ad hoc du layout.

En 2010, les collègues de l'EPFL dans [18] ont introduit une nouvelle méthodologie de modélisation des parasites du substrat. Leur approche consiste à modéliser le substrat par un réseau de dispositifs parasites particuliers. Les modèles des dispositifs parasites sont enrichis par rapport aux modèles compact traditionnels pour prendre en compte les effets liés aux porteurs minoritaires, qui ne sont pas modélisés par les modèles compacts standard. Soulignons qu'en plus de l'existence des modèles, la prise en compte de la géométrie du layout est un facteur clé pour modéliser correctement le comportement du bruit de substrat. En nous appuyant sur ces modèles de dispositifs parasites, nous proposons une méthode pour développer un outil automatique d'extraction du layout et de modélisation des bruits issus du substrat qui impactent le circuit principal.

Ce résumé est organisé ainsi : Dans la première section, nous rappelons la méthodologie de modélisation des parasites de substrat en technologie HV. La section suivante présente notre flot de conception. Pour valider notre modèle de substrat, nous proposons ensuite une analyse comparative, entre simulation et mesure, des diodes parasites et transistors bipolaires. Nous appliquons notre méthode à deux cas d'étude et terminons par une conclusion.

Méthodologie de modélisation

Dans le cadre du projet européen AUTOMICS intitulé "Solution Pragmatique pour la Conception Immune aux Parasites pour l'automobile", notre but est de proposer une nouvelle solution pour modéliser les couplages parasites qui se produisent au sein des systèmes intégrés utilisés dans les automobiles.

Notre idée repose sur la construction automatique d'un réseau 3D qui prend en compte à la fois la propagation des porteurs majoritaires et celle des porteurs minoritaires dans le substrat. Ce réseau est composé d'une interconnexion d'instances de modèles de dispositifs parasites (comme les diodes, résistances et homojonctions proposées par l'EPFL) avec des caractéristiques géométriques extraites du layout. Ces modèles enrichis sont des modèles compacts de type SPICE (écrits en Verilog-A), qui possèdent deux terminaux supplémentaires pour donner la concentration et le gradient de concentration des porteurs minoritaires. Les concentrations des porteurs minoritaires sont représentées par une tension et leur gradient par un courant [19]. Par conséquent, les effets bipolaires (NPN) ou (PNP) peuvent être respectivement modélisés simplement par deux diodes en série (NP-PN, respectivement PN-NP). Les transistors NPN latéraux issus du substrat peuvent alors être extraits et simulés par un simulateur électrique de type SPICE [17]. Soulignons

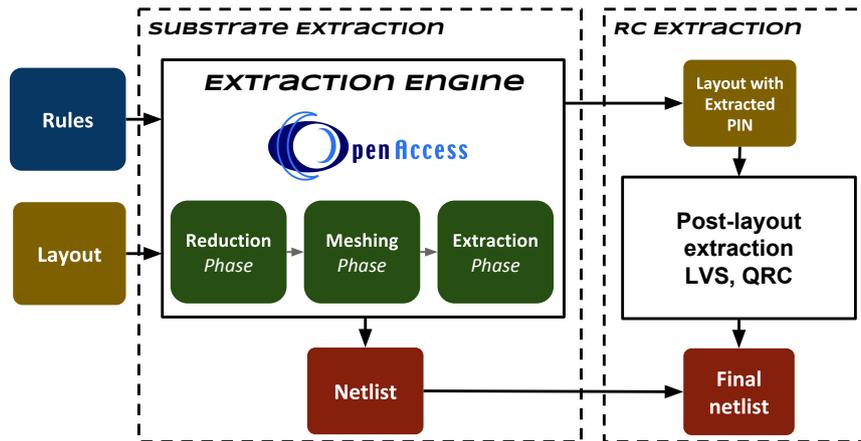


Figure 1: Flot global d'extraction post-layout.

que ce réseau modélisant le substrat peut être rétro-annoté dans la netlist du circuit principal, ce qui est impossible à réaliser avec un logiciel TCAD. Notre approche permet donc d'estimer les comportements des courants de substrat et leur impact sur le fonctionnement du système, par des simulations au niveau transistor, lors de la phase de conception avant la fabrication du premier prototype [49, 48, 26].

Méthodologie d'extraction et modélisation du substrat

Dans ce qui suit, nous détaillons notre approche pour l'extraction post-layout incluant les parasites du substrat. Le flot de la figure 1 décrit l'idée générale.

Notre flot d'extraction se compose de 2 parties :

- Extraction du réseau représentant le comportement du substrat. Nous avons développé un moteur d'extraction en nous appuyant sur la base de données Open Access. Nous avons intégré l'extracteur dans l'environnement de conception Cadence, paramétré suivant la technologie ams AG (en complétant le Process Design Kit –PDK– de cette technologie). L'approche que nous suivons pour modéliser le substrat est illustrée par la figure 2, et sera expliquée dans les paragraphes suivants.
- Extraction des résistances et capacités (RC) et rétro-annotation de la netlist. Pour rétro-annoter la netlist post-layout standard du circuit principal avec le réseau modélisant le substrat, nous avons défini des terminaux supplémentaires à l'interface entre le substrat et le circuit principal dont les masques sont "au-dessus" du substrat. On utilise ces terminaux pour relier automatiquement, par des courts-circuits, les fils métalliques du circuit principal au réseau de composants parasites représentant le substrat.

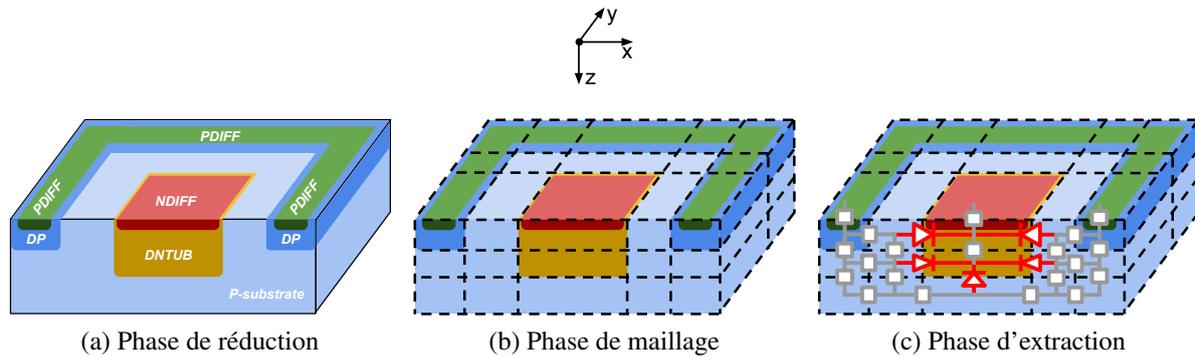


Figure 2: Modélisation d'une diode simple : approche pour l'extraction des parasites du substrat.

Notre méthodologie suit 3 phases pour extraire le réseau de composants parasites représentant le substrat :

Phase de réduction

La région que nous considérons pour l'extraction particulière du substrat se situe en dessous des zones de diffusion des transistors. Nous considérons d'une part les puits de diffusion : par exemple le puits profond N (DNTUB) et le puits profond P (DPTUB) du procédé technologique AMS AG 0.35 μm HV-CMOS, et les implants : par exemple l'implant N (NDIFF) et l'implant P (PDIFF). D'autre part, nous considérons que tous les autres matériaux, comme les couches métalliques et les vias, ne produisent pas de composant parasite de substrat et nous les ignorons dans cette phase d'extraction. Nous utilisons des règles spécifiques pour définir les masques impliqués pour un processus technologique cible. Les règles sont exprimées en langage XML (Extensible Markup Language –XML–). Par conséquent, dans notre approche, nous commençons notre processus d'extraction des composants parasites du substrat par une phase de définition d'un jeu réduit de masques, et la production d'une version réduite du layout par rapport à sa version issue directement de la conception, sur laquelle nous procédons aux étapes suivantes :

Phase de maillage

Le maillage en volume du substrat s'appuie sur des éléments localisés en 3-D (i.e. cubes). Chaque élément représente une région différente du substrat et peut avoir une taille différente. Pour construire le maillage en 3D, nous procédons en trois étapes: 1). définition des différents niveaux suivants l'axe vertical; 2). maillage en surface 2D; 3). optimisation du maillage 2D.

Niveaux suivants l'axe vertical : Pour effectuer le maillage, le substrat est divisé en plusieurs couches, ou tranches, empilées selon la verticale. Le nombre total de tranches est calculé à partir de l'épaisseur des puits suivant la profondeur des jonctions. Par exemple, si l'on considère une région de substrat d'épaisseur de 20 μm , les couches considérées dans

ce cas sont DNTUB et DPTUB (Figure 2(b)). Finalement, dans ce cas, le maillage vertical conduit à considérer 3 tranches. La “coupe” à travers la jonction PN (DNTUB vers substrat-P) et la “coupe” DPTUB vers le substrat de type P conduisent aux trois tranches suivantes : la tranche “haute” comprend les puits DPTUB et DNTUB et le substrat de type P (Figure 3b); la tranche “milieu” ne comprend que DNTUB et le substrat de type P (Figure 3c); puis la tranche “basse” est composée uniquement du substrat de type P (figure 3d). Le tableau 2 présente les informations pertinentes pour le maillage, telles que l’épaisseur (deuxième colonne) des puits ou des implants (troisième colonne) à chaque tranche considérée (indice dans la première colonne). En outre, les zones de diffusion de type N et de type P sont considérées comme des contacts sur la surface de la tranche “haute” tranche (Figure 3a).

Table 2: Tableau des couches à considérer dans chaque tranche.

| <i>Indice</i> | <i>Épaisseur (μm)</i> | <i>Puits et/ou Implants</i> |
|---------------|---|-----------------------------------|
| 0 | d_{DP} | <i>NDIFF, PDIFF, DNTUB, DPTUB</i> |
| 1 | $d_{DN} - d_{DP}$ | <i>DNTUB</i> |
| 2 | $20 - d_{DN}$ | <i>N/A</i> |

Maillage 2D en surface : une fois que le substrat est divisé en tranches, on construit un maillage 2D sur la surface (axes x-y) au niveau de chaque tranche. Comme les puits ont différentes profondeurs de jonction, les maillages 2D sont différents d’une tranche à l’autre (Cf. Figure 3). Dans notre méthodologie, le maillage le 2-D est basé sur des points et non pas sur des formes prédéfinies (par exemple un rectangle ou un polygone est représenté par une combinaison de points ordonnés). Le coût pour le calcul et la mémoire utilisée augmentent à mesure que le layout devient plus complexe. Avant de commencer à construire le maillage, nous recueillons les sommets que nous sauvegardons comme :

$$S = \{v_1, v_2, \dots, v_n\}$$

où n est le nombre total de sommets reliés, chacun représentant un point, à savoir $v_j = (x_j, y_j)$. Si un point 2-D peut décrire un emplacement sur la surface, alors deux points 2-D décrivent un segment correspondant à une limite de jonction. L’extension de ce segment jusqu’aux extrémités des bords devient une ligne du maillage (ligne noire sur la figure). L’ensemble des projections de ces sommets sur l’axe x est appelé *Xarray*, et celui des projections sur l’axe y, *Yarray*. Dans notre cas, ils sont exprimés par :

$$Xarray = \{a_1, a_2, a_3, \dots, a_p\}$$

$$Yarray = \{b_1, b_2, b_3, \dots, b_q\}$$

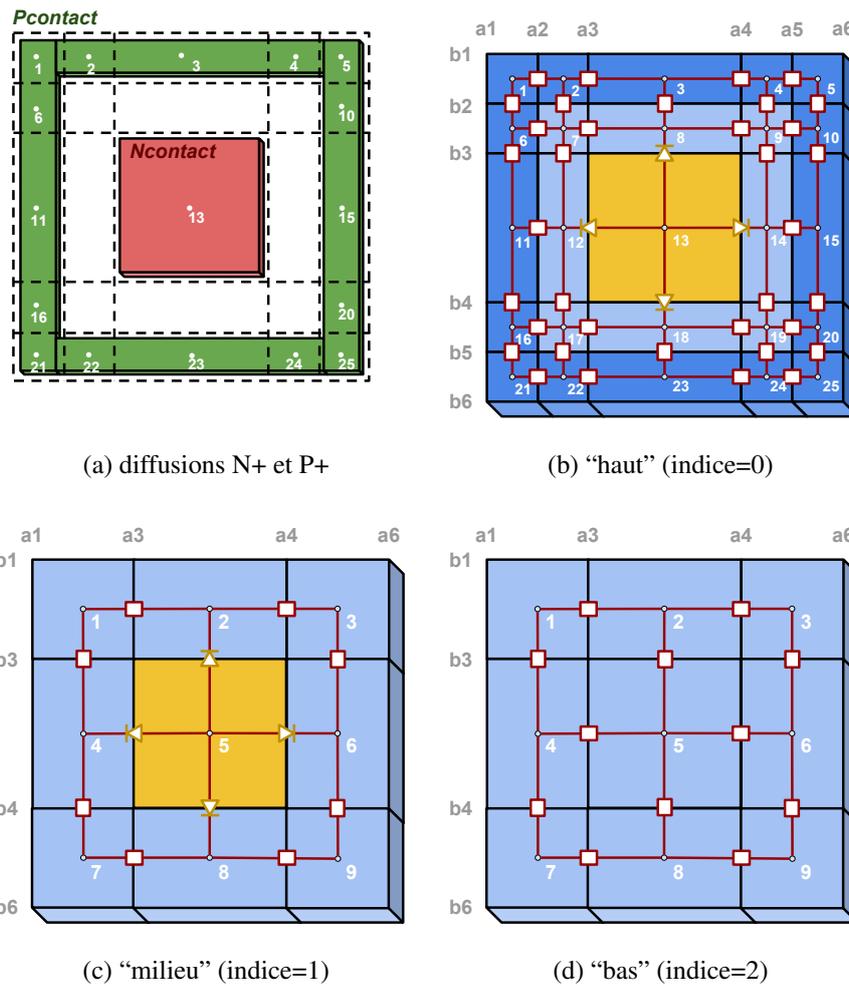


Figure 3: Maillage 2D pour chaque tranche: (b) "haute", (c) "milieu", (d) "basse", et (a) Diffusion N+/P+ sur la surface du "haut". $\{a_1, a_2, \dots\}$ sont les coordonnées sur l'axe x, et $\{b_1, b_2, \dots\}$ sont les coordonnées sur l'axe y. Les lignes en noir représentent les lignes de maillage. Les lignes en rouge sont les fils métalliques dans la netlist. Les symboles en jaune et rouge représentent respectivement des diodes DN-PS et des résistances dans le substrat-P.

où p est le nombre total de coordonnées sur l'axe x, et q celui sur l'axe y. Ces deux ensembles de points servent à construire le système de coordonnées du maillage résultant. Pour chaque élément de maillage, sa profondeur est égale à l'épaisseur de la tranche (Cf. Tableau 2) et sa surface est définie par les coins opposés, soit par le coin inférieur gauche (LL) et le coin supérieur droit (UR). Finalement, la géométrie de l'élément peut être exprimée sous la forme :

$$Length = UR.x - LL.x$$

$$Width = UR.y - LL.y$$

$$Depth = d_{couche}$$

Outre la géométrie, un élément de maillage possède un type de matériau. Les types de

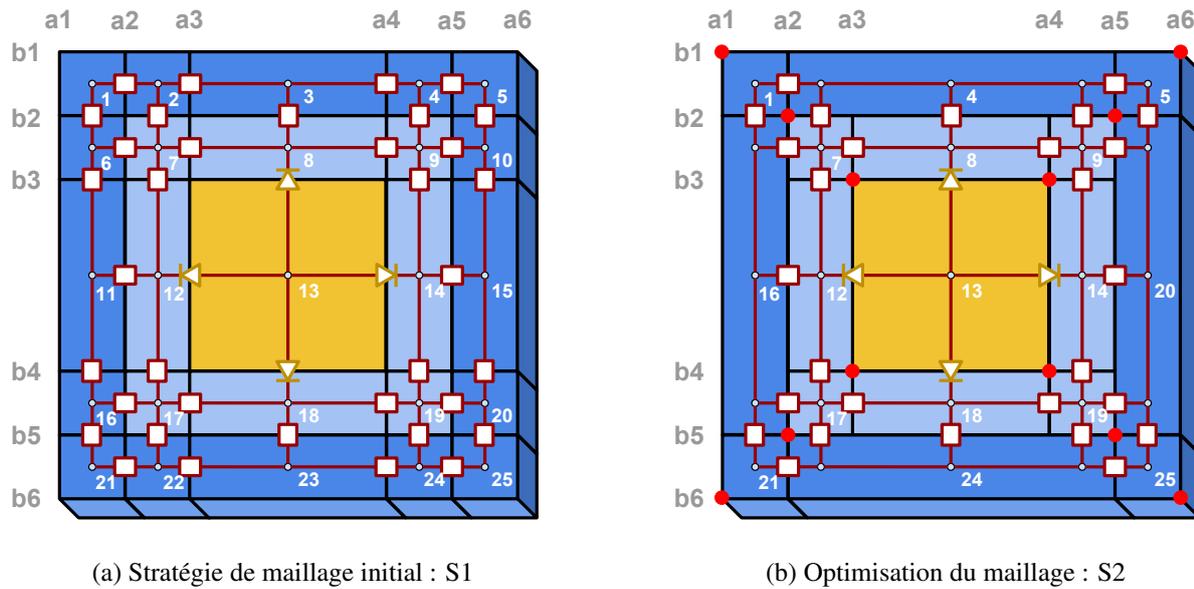


Figure 4: Principe pour optimiser la tranche “haute”. Les points rouges dans la figure (b) représentent les sommets des formes géométriques (la couche DPTUB est un polygone et la couche DNTUB est un rectangle).

matériaux disponibles sont : Nwell, Pwell, Nimplant, Pimplant, Psub.

Optimisation du maillage : Nous venons d’introduire une méthodologie pour mailler le substrat. Cette méthode repose sur un maillage 2D rectiligne du substrat. Nous avons présenté dans l’article [47], une stratégie de maillage optimisé, qui contribue à réduire de façon significative la taille du réseau maillé, et ainsi accélérer la simulation. Dans cette section, nous présentons cette stratégie d’optimisation du maillage sur la tranche ”haute” de la structure, en ayant en tête que cette stratégie peut être appliquée à chacune des tranches du maillage 3-D.

La stratégie initiale de maillage (S1) est représentée sur la figure 4a. Dans notre approche, le maillage est construit par des cubes 3-D dont la hauteur est définie par la profondeur de la tranche, et la surface (dans le plan x-y) est définie par les coins opposés suivant la diagonale. Pour trouver ces coins, nous avons conçu un système de coordonnées en 2-D. Les coins des cubes sont les intersections ses lignes de maillage perpendiculaires. Par exemple, le maillage de la figure 4a possède les coordonnées sur l’axe X- $Xarray = \{a1, a2, a3, a4, a5, a6\}$ et les coordonnées sur l’axe Y $Yarray = \{b1, b2, b3, b4, b5, b6\}$. Ces coordonnées sont la projection sur les axes X et Y des sommets des masques DNTUB, et DPTUB. A titre d’exemple, les sommets de DNTUB produisent les coordonnées $\{a3, a4\}$ pour l’ensemble $Xarray$ et $\{b3, b4\}$ pour l’ensemble $Yarray$.

La stratégie de maillage optimisée (S2) est représentée sur la figure 4b. A partir du maillage initial, on applique la technique d’optimisation de maillage pour réduire le nombre

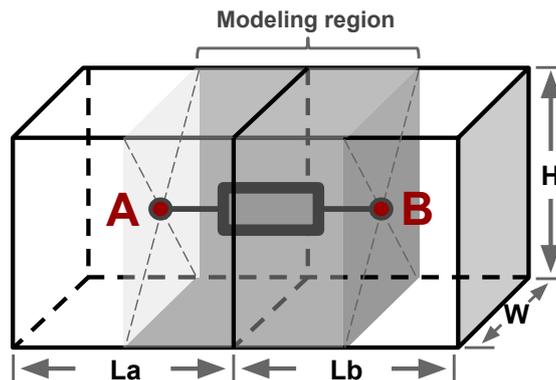


Figure 5: Principe pour extraire un composant parasite. Les ronds rouges au centre des cubes deviendront les noeuds de la netlist résultante.

d'éléments en combinant plusieurs éléments. Pour pouvoir fusionner des petits éléments, on doit respecter les 3 conditions suivantes: 1) même type de matériau; 2) l'élément fusionné réalise une forme rectangulaire; 3) la forme résultante ne chevauche pas des sommets (rouges sur la figure). Par exemple, un groupe d'éléments initiaux 1, 2, 3, 4, 5 (Cf. Figure 4a) recouvre les sommets (a2, b2) et (a5, b5), donc ils ne peuvent pas être fusionnés, même si ils sont composés du même type de matériau. Au contraire, le groupe d'éléments initiaux 2, 3 (Cf. Figure 4a) peut être fusionné avec l'élément 4 sur la figure 4b. Cette technique de fusion reconstitue une structure unique de maillage composée de nouveaux éléments de maillage de tailles distinctes.

Phase d'extraction

L'extraction des composants parasites du maillage produit une netlist. Cette netlist se compose de composants parasites avec des paramètres géométriques. L'extraction d'un composant est effectuée entre deux éléments adjacents dans le maillage. Considérons deux éléments adjacents du maillage, comme illustré sur la figure 5, un composant parasite est extrait entre leurs deux centres. En fonction des types de matériaux, le composant obtenu peut être soit une diode (si les matériaux sont de types différents), soit une résistance (même matériau), soit une homojonction (même matériau mais avec des concentrations de dopages différents). Les paramètres géométriques extraits sont la longueur, surface, etc (Cf. tableau 3).

Outre la géométrie, on extrait également le matériau. Par exemple, la résistance extraite du puits DNTUB diffère de celle extraite du puits DPTUB du fait de la nature du dopage du silicium, qui diffère également de la résistance extraite du substrat-P. Ceci entraîne des résistances extraites différenciées selon :

Table 3: Liste des paramètres pour l'extraction des composants parasites.

| <i>Composant parasite</i> | <i>Profil de dopage</i> | Paramètres géométriques | |
|---------------------------|-------------------------|--------------------------------|--------------------------------|
| | | <i>Longueur [m]</i> | <i>Surface [m²]</i> |
| Diode | n | $L_a/2$ | $w \times h$ |
| | p | $L_b/2$ | |
| Résistance | n or p | $L_a/2 + L_b/2$ | |
| Homo-junction | n or p | $L_a/2$ | |
| | n+ or p+ | $L_b/2$ | |

Table 4: Les combinaisons possibles et les composants parasites disponibles.

| | PSUB | DNTUB | DPTUB | NDIFF | PDIFF |
|-------|-------------|-------------|-------------|-------|-------|
| PDIFF | H_{PD-PS} | D_{PD-DN} | H_{PD-DP} | N/A | N/A |
| NDIFF | D_{ND-PS} | H_{ND-DN} | D_{ND-DP} | N/A | |
| DPTUB | H_{DP-PS} | D_{DP-DN} | R_{DP} | | |
| DNTUB | D_{DN-PS} | R_{DN} | | | |
| PSUB | R_{PS} | | | | |

- R_{DP} : à l'intérieur du puits DPTUB;
- R_{DN} : à l'intérieur du puits DNTUB;
- R_{PS} : à l'intérieur du substrat de type P.

Ce même principe est utilisé dans le cas des composants parasites diodes et homojonctions. Le tableau 4 énumère toutes les combinaisons possibles des masques et les composants parasites résultants.

Validation

La calibration des paramètres technologiques, tels que le profil de dopage et la durée de vie des porteurs, a été effectuée en utilisant des structures de référence fabriquées par le fondeur amsAG. L'entreprise amsAG a fourni plusieurs structures de référence pour les diodes, de diverses tailles (surface, périmètre). Ces structures de référence ont été extraites en utilisant notre approche et notre outil CAO et les paramètres de la technologie ont été calibrés en utilisant un algorithme d'identification pour adapter les résultats de la simulation aux données mesurées. Nous ne détaillons pas ici le processus de calibration lui-même, mais nous montrons les résultats issus de ce processus.

Modélisation de la diode

Notre première étude de cas est la structure de référence de la diode DNPS. Cette structure est une diode de dimensions $800\mu\text{m} \times 800\mu\text{m}$. Les paramètres de sortie provenant de l'extraction et de la simulation sont résumés dans le tableau 5. Les résultats des comportements DC, y compris en polarisation directe et inverse sont présentés à la figure 6. Les résultats respectifs des simulations sont dessinés avec des lignes droites et les mesures avec des points. Dans la même figure, les courbes en couleurs montrent les comportements en fonction de la température : 27°C (bleu), 75°C (noir) et 125°C (rouge).

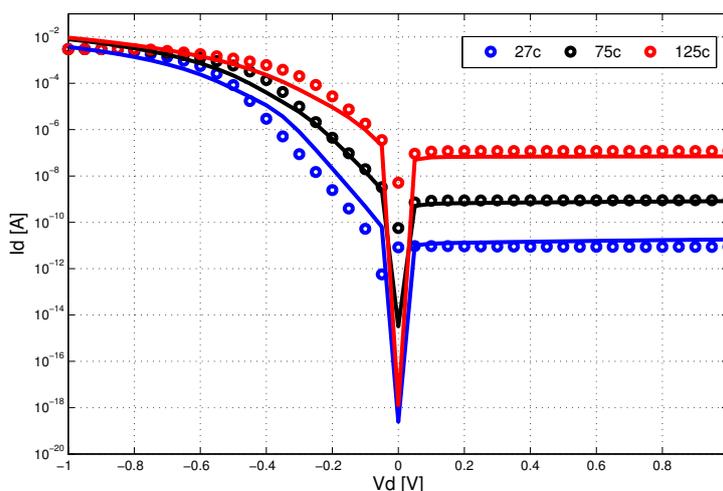


Figure 6: Comportements de la diode en fonction de la température en polarisation directe et inverse, à 27°C (bleu), 75°C (noir) et 125°C (rouge).

Modélisation du transistor NPN latéral

La modélisation du transistor parasite NPN latéral parasite est une tâche difficile. Dans la technologie CMOS HV, l'émetteur du transistor NPN est causé par l'injection, dans un caisson (puits)

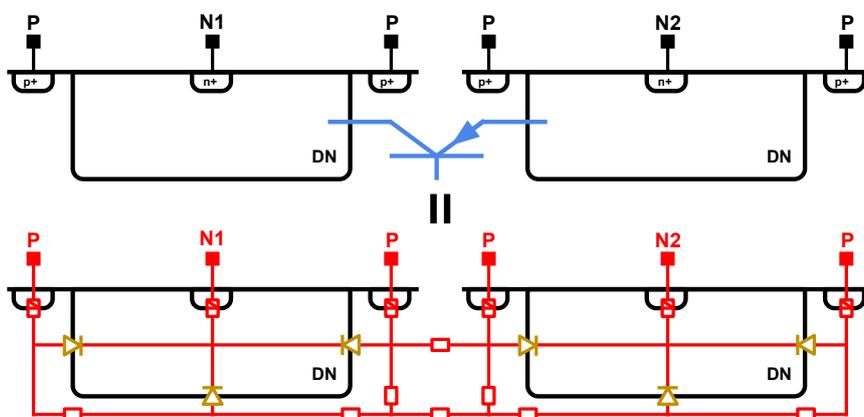
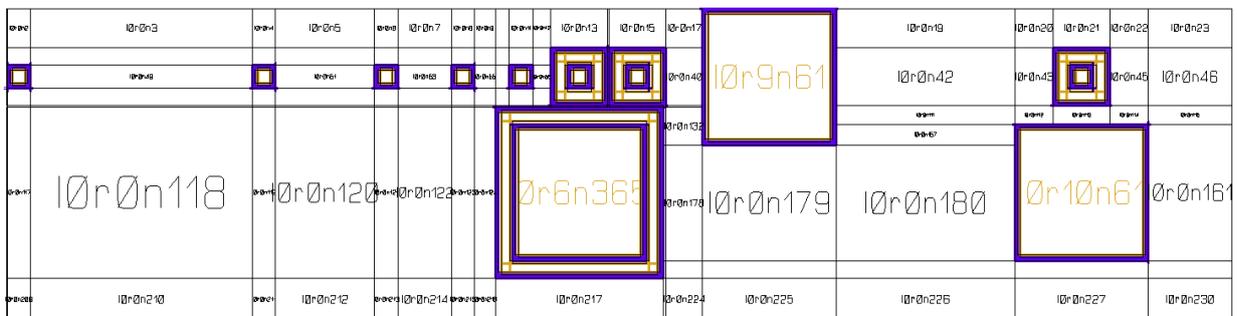


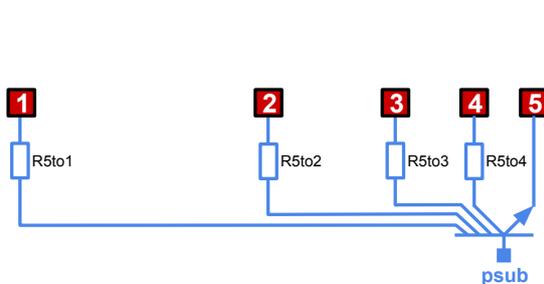
Figure 7: Illustration du transistor BJT NPN latéral parasite et son circuit équivalent.

N-well, d'un courant de substrat (généralement issu d'un dispositif de puissance), les collecteurs sont les puits N-well environnants tandis que la base est la totalité du substrat de type P. Par conséquent, l'extraction de ces dispositifs parasites suivant la géométrie du layout devient impossible en utilisant le modèle BJT standard. Dans notre approche, la modélisation du transistor parasite NPN latéral s'appuie sur le maillage du substrat (Cf. Figure 7). Le maillage du substrat conduit à modéliser le transistor parasite latéral NPN avec plusieurs diodes en fonction de la géométrie du layout. L'effet bipolaire parasite NPN est ensuite ajouté à la netlist (post-layout) du circuit initial.

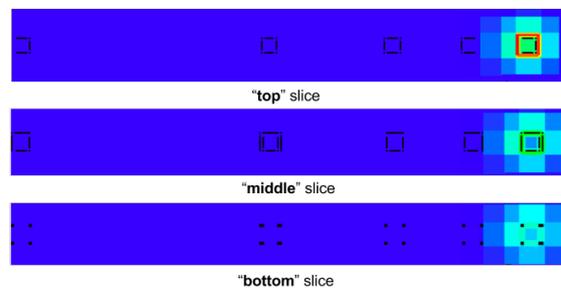
La deuxième structure de test et validation est un circuit fabriqué par amsAG. Ce circuit de test contient 15 diodes DN-PS partageant le même substrat. Il dispose de plots d'entrées-sorties. Les 15 premiers d'entre eux (PAD 1 à 15) sont chacun connectés à un des 15 puits N-well, et le dernier (PAD16) est connecté à un anneau de P-well qui est le contact de substrat autour des 15 puits N-well. L'ensemble du circuit de test est extrait à l'aide de notre méthode (Cf. tableau 5). L'extraction de la totalité du circuit est réalisée en deux étapes: 1) l'extraction des dispositifs parasites (chaque diode DN-PS); 2) l'extraction du substrat en dehors des zones occupées par les dispositifs. La structure du maillage est représentée à la figure 8. Avant de procéder à la simulation, il faut s'assurer que les 15 diodes DN-PS ne sont pas comptabilisées 2 fois (par l'extracteur du substrat et par l'extraction standard fondée sur le Process Design Kit du fondeur).



(a) Maillage



(b) Cas de test



(c) Carte en couleur

Figure 8: (a) Capture d'écran de maillage de l'ensemble de la puce test; (b) la configuration des cas de test. (c) la carte en couleur de la chute de tension due à l'injection de porteurs minoritaires.

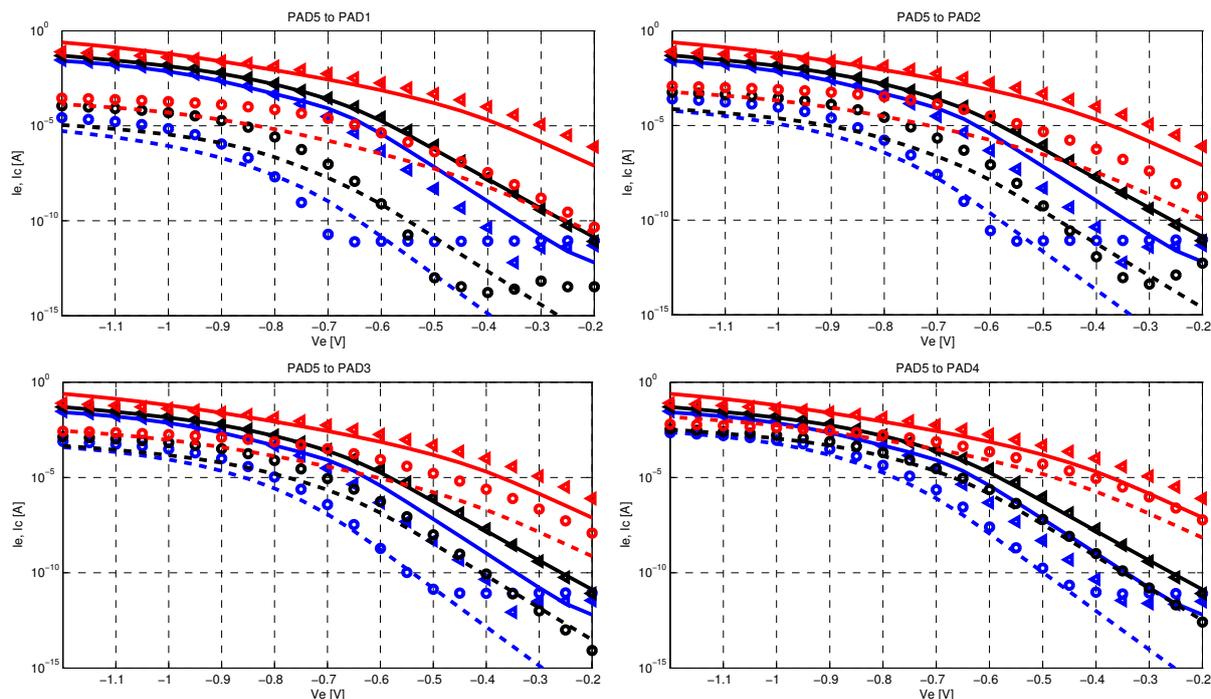


Figure 9: Caractéristiques courant-tension du transistor parasite NPN latéral en fonction de la température : -25°C (bleu), 27°C (noir) et 125°C (rouge) et en fonction de la distance à l'émetteur PAD5 (collecteur PAD1 au collecteur PAD4). Les courants à l'émetteur (I_e) et au collecteur (I_c) sont présentés pour la simulation (lignes) et les mesures (symboles).

Dans le test que nous effectuons, présenté à la figure 9, nous considérons en particulier les plots PAD1 à PAD5. Nous nous intéressons principalement à l'analyse des transistors parasites NPN latéraux et nous cherchons à estimer l'effet de la distance. Chaque puits Nwell a la même dimension ($20\mu\text{m} \times 20\mu\text{m}$), et est situé à une distance différente de PAD 5. Pour la simulation, le plot PAD5 est la zone de substrat émettant et le collecteur est un des 4 autres plots, tandis que les 3 autres sont flottants. La comparaison avec les mesures montre un bon accord entre résultats de simulation et mesures (Cf. Figure 9), y compris avec la variation de température, ce qui confirme la validité de notre approche.

Modélisation des transistors parasites verticaux NPN et PNP

Dans la technologie CMOS HV, un caisson N profond isole les transistors du substrat de type P. Cette structure présente intrinsèquement un transistor parasite vertical à jonction bipolaire NPN (cas d'un transistor N-MOS) ou PNP (cas d'un transistor P-MOS). Le drain du transistor P-MOS correspond à l'émetteur du transistor parasite PNP vertical, qui est habituellement relié à la charge. Les conditions de fonctionnement sont telles que le potentiel de ce drain peut être inférieur à la tension la plus négative ou supérieur à la tension d'alimentation, au risque d'activer le transistor bipolaire vertical qui injecte alors du courant dans le substrat. Ce type de configuration se retrouve souvent dans les applications automobiles HV. En règle générale, le transistor vertical parasite peut

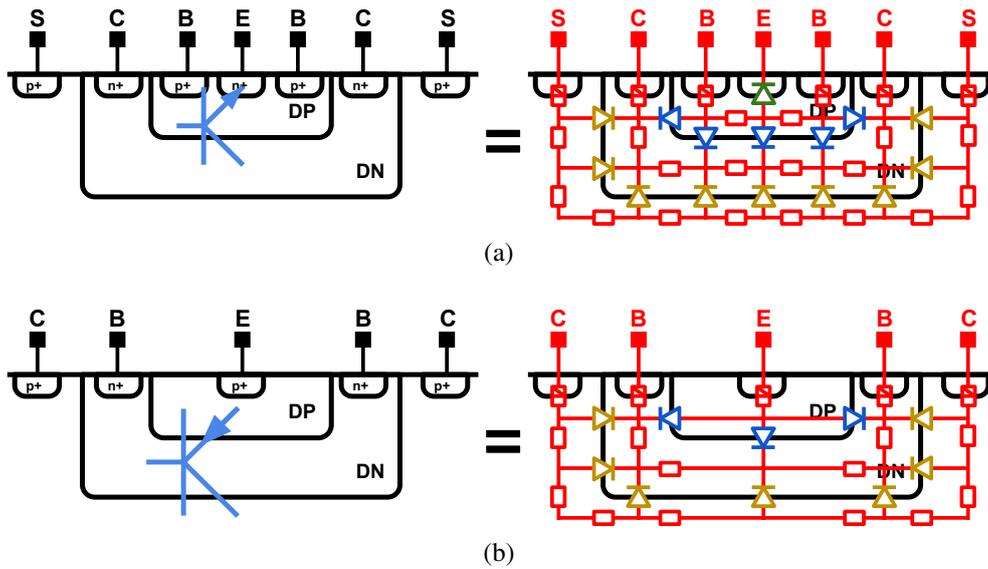


Figure 10: Structure des transistors verticaux NPN (VERTN1, a), et PNP (VERTPH, b), et leurs équivalents en circuits modélisés suivant notre approche.

être ajouté au modèle compact du modèle SPICE standard, cependant la propagation des courants de substrat est impossible à modéliser avec cette approche, qui ne prend pas en compte l'ensemble du layout. Par conséquent, dans notre approche, nous modélisons également les transistors parasites verticaux par des combinaisons de diodes à modèle enrichi.

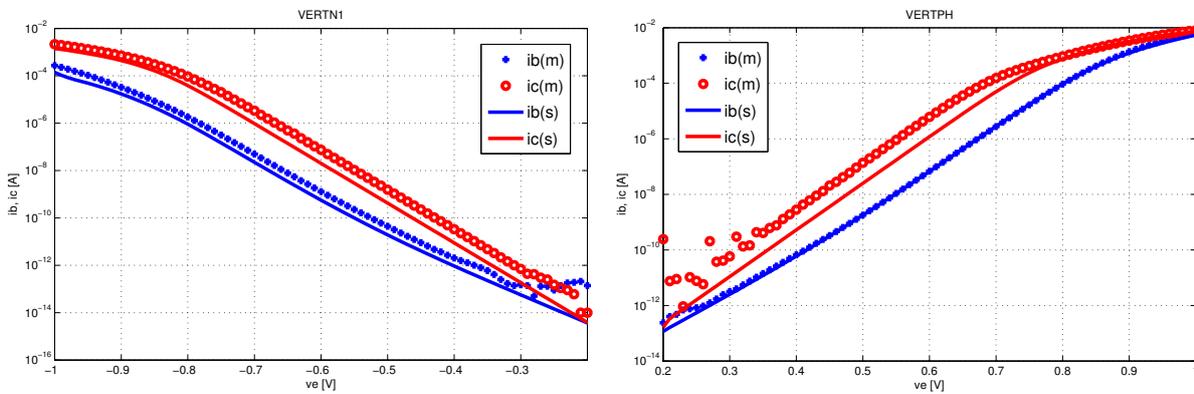


Figure 11: Courants DC des transistors verticaux NPN (VERTN1, a) et PNP (VERTPH, b) BJT. Comparaison des résultats de simulation (lignes) aux données mesurées (symboles).

Dans la structure de test que nous avons étudiée précédemment, l'effet du transistor parasite NPN latéral était produit en connectant des diodes latérales, entre des puits N-well, par leurs anodes. L'extraction des transistors parasites verticaux s'appuie, elle, sur différents puits N-well et P-well présents dans le substrat. Il faut donc prendre en compte divers types de diodes parasites en fonction de la jonction PN du puits considéré. La connexion entre les anodes de ces diodes propage des porteurs minoritaires permettant de simuler le comportement d'un transistor NPN parasite. D'une façon analogue, la connexion de ces diodes par les cathodes permet de simuler le

comportement d'un transistor PNP parasite.

Outre la diode DN-PS (jaune), on rencontre la diode DP-DN (bleu) et la diode ND-DP (verte) au cours de l'extraction du substrat (comme indiqué au tableau III). La calibration de ces diodes est réalisée en utilisant les dispositifs bipolaires classiques de la bibliothèque standard du fondeur qui définit précisément la géométrie de la structure BJT verticale (Cf. Figure 10). Les résultats concernant l'extraction et la simulation de deux transistors bipolaires sont présentés par le tableau IV. Il faut veiller à ne pas prendre en compte 2 fois ces transistors verticaux (via la bibliothèque de modèles du fondeur et via notre extraction du substrat). Les caractéristiques courant-tension en DC obtenues par simulation sont représentées sur la figure 11 et validées par comparaison avec les mesures.

Cas d'études

Test 1 : Miroir de current

Le miroir de courant est un circuit simple qui est régulièrement utilisé dans les IC analogiques. Ce circuit est conçu pour reproduire un courant (courant de référence) d'une branche du circuit à une autre branche, et permet donc de conserver le courant de sortie constant quel que soit la charge. Dans notre étude, nous nous intéressons à l'influence des courants de substrat sur ce circuit analogique de base. Le circuit test est présenté sur la figure 12.

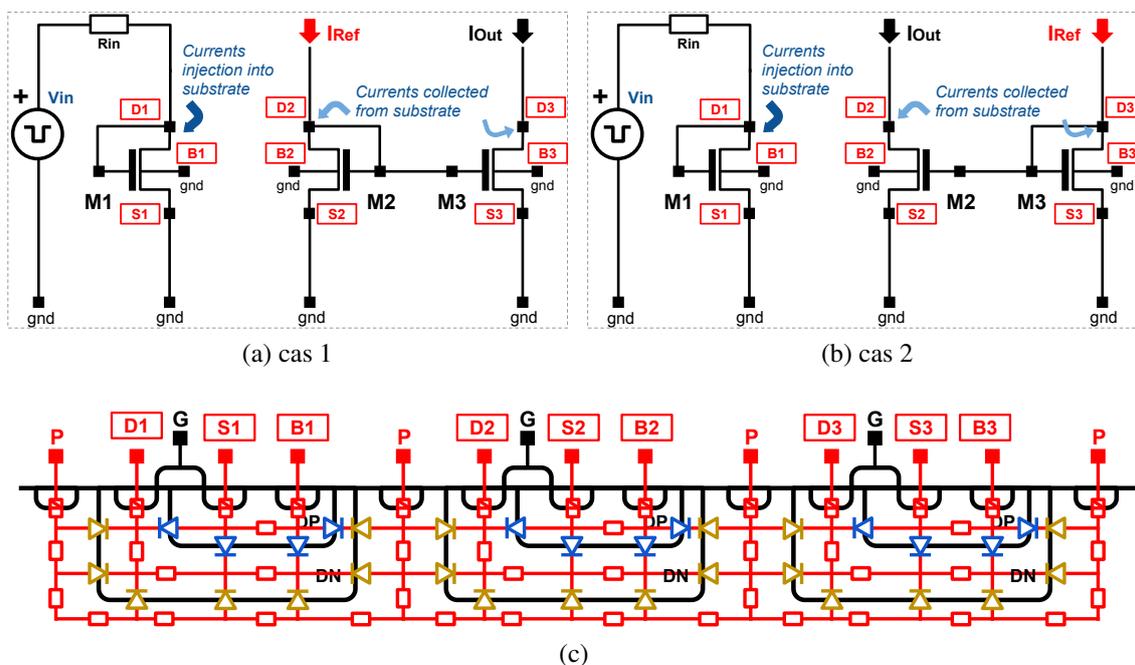


Figure 12: (a, b) Un circuit de test dans 2 configurations miroir de current, et (c) le réseau modélisant le substrat.

Le transistor M1 est un LDMOS à canal N auto-polarisé qui injecte des courants dans le substrat à partir d'une source de tension d'alimentation négative (V_{in} dans la figure 12). Les transistors M2 et M3 sont également des transistors LDMOS à canal N et ont la même taille (i.e. W et L) que le transistor M1. Le transistor M2 est plus proche de M1 que le transistor M3 au point de vue layout. Les transistors sont utilisés comme puits dans deux configurations différentes:

- cas 1: le transistor M2 est la source de courant du miroir de courant, il est proche de l'agresseur M1;
- cas 2: le transistor M3 est la source de courant du miroir de courant, alors il est plus éloigné de l'agresseur M1;

Les réseaux de substrat extraits dans les deux cas sont les mêmes, car ils représentent la même géométrie du substrat (Cf. Figure 12c). Le circuit principal est rétro-annoté avec la netlist extraite du substrat. Un signal transitoire sous forme d'impulsion négative ($1V$, $2\mu s$) est appliqué comme source de tension d'entrée (Cf. figure 13). Le potentiel négatif du drain du transistor M1 provoque l'injection de courant dans le substrat. Puis la polarisation, dans le sens direct, de la diode DN-PS parasite du transistor M1 déclenche le transistor NPN latéral. Par conséquent, les courants des 3 transistors M1, M2 et M3 se trouvent couplés par les puits DNTUB des transistors M2 et M3. Les courants de couplage dépendent de la distance entre les dispositifs : $I_{subM2} > I_{subM3}$, parce que $d_{M1-M2} < d_{M1-M3}$. En conséquence, la chute de tension au niveau du puits DNTUB du transistor M2 est supérieure à celle du transistor M3.

- Dans le cas 1, le transistor M2 est la source du miroir de courant qui convertit le courant en tension. La chute de tension au drain de M2 (D2) provoque une baisse de tension à la grille de M2. Du fait de cette chute de tension grille-source du miroir de courant, le courant de drain du transistor M3 diminue. Cette chute du courant recopié par le miroir n'est pas compensée par l'augmentation des courants de couplage à travers le substrat, et donc le courant total du transistor M3 (I_{out}) diminue. Au contraire, le courant total du transistor M2 (I_{ref}) augmente car les courants dus à la propagation à travers le substrat y sont plus importants.
- Dans le cas 2, le transistor M3 est la source du miroir de courant. Comme M3 est plus loin que M2 de l'agresseur, l'effet de couplage, à travers le substrat, sur le miroir de courant est moindre que dans le cas précédent et la diminution du courant recopié par le miroir, est moins importante que l'effet de couplage des courants à travers le substrat. Les courants de M2 (I_{out}) et M3 (I_{ref}) augmentent selon leur distance par rapport à M1.

Sur la figure 13, les résultats de la simulation confirment la validité du comportement du transistor de substrat parasite NPN dans des conditions du test. L'impact des bruits de substrat sur le

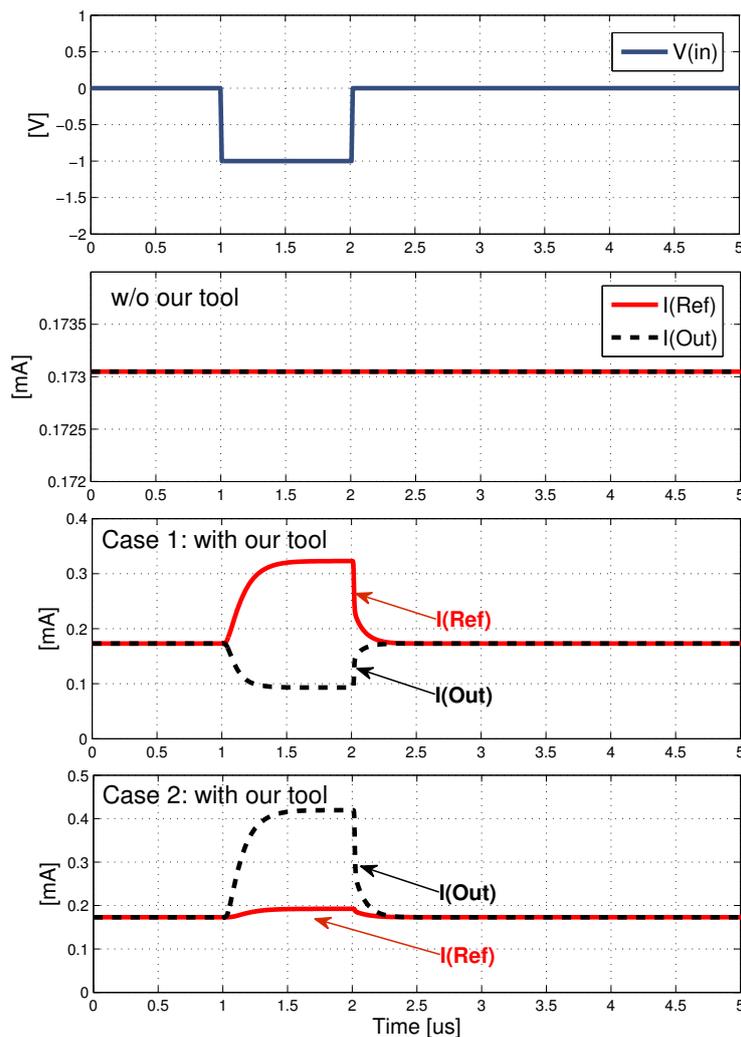


Figure 13: Comportements transitoires avec injection de courant substrat.

miroir de courant apparaît clairement à l'aide de notre outil. Soulignons que cet effet ne peut pas être simulé de façon classique.

Test 2 : standard pour l'automobile

Le second cas de test est un circuit industriel fabriqué par amsAG [41]. Son principe est présenté sur la figure 14. L'entrée est un plot d'entrée-sortie (IO) qui se compose de deux diodes connectées en série entre VDD et la masse. La source de l'agression se situe entre les deux diodes (Cf. " V_{in} " Figure 14). Deux puits N-well de taille $d4 \times d6$ chacune, sont placés pour collecter les charges injectées. La distance à l'émetteur est différente dans les deux cas et vaut respectivement $d5$ pour le plus proche et $d5 + d6 + d7$ pour l'autre. La sortie " V_{out} " est implémentée par un plot. On utilise une option de découpage au laser pour connecter ou déconnecter les différents puits N-well sur le plot " V_{out} ".

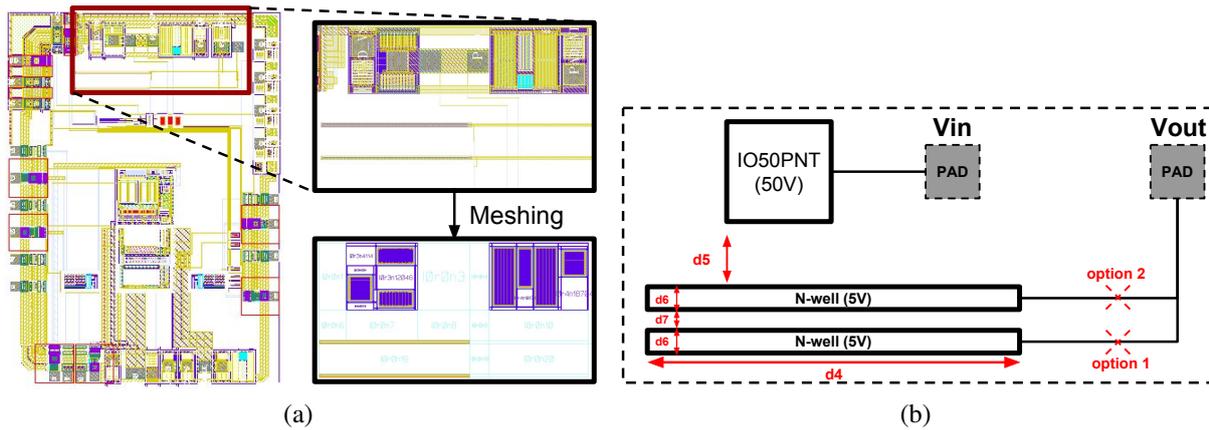


Figure 14: (a) Vue du layout du test 2; (b) la structure simplifiée du cas test.

Afin d'atteindre la phase de production, tous les produits destinés aux applications embarquées dans l'automobile doivent passer des tests de qualification. Certains de ces tests peuvent causer des courants parasites de substrat. Dans notre cas, un signal de test automobile standard (ISO 7637-2 Pulse 1) est appliqué comme signal sur le plot "Vin". Ce signal d'entrée est un exemple de signal de test sévère qui requiert que le produit reste entièrement fonctionnel tandis que les bornes de sortie sont soumises à une tension négative.

Le comportement de ce signal de test (bleu) est représenté figure 15. Il simule une impulsion transitoire de polarité négative provoquée par la coupure de l'alimentation en courant continu à travers une charge inductive. La tension de crête " V_s " prend les valeurs 6V, 12V et 20V pour différents tests. Le temps de récupération est 2ms et le taux de répétition est de 500ms. Enfin,

Table 5: Les paramètres de sortie pour la simulation.

| Structures de test | | Diode DN-PS | NPN latéral | NPN vertical | PNP vertical | Test 1 : Miroir | Test 2 : automobile |
|------------------------|---------------|-------------|-------------|--------------|--------------|-----------------|---------------------|
| Noeuds | | 154 | 1958 | 238 | 313 | 871 | 6561 |
| Composants | | 262 | 3419 | 440 | 601 | 1619 | 12291 |
| Substrat | diode* | 17 | 487 | 71 | 54 | 304 | 2766 |
| | homojunction* | 68 | 163 | 76 | 147 | 261 | 807 |
| | resistance* | 177 | 2676 | 280 | 392 | 1007 | 8193 |
| Temps d'extraction (s) | | 1.96 | 19.71 | 2.23 | 2.57 | 16 | 20.82 |
| RC | diodes | 1 | 15 | 0 | 0 | 0 | 11 |
| | capacitance | 0 | 47 | 9 | 3 | 8 | 104 |
| | resistance | 0 | 31 | 4 | 5 | 27 | 286 |
| | bjt | 0 | 0 | 0 | 0 | 4 | 62 |
| | jfet | 0 | 0 | 0 | 0 | 8 | 62 |
| Temp de simulation (s) | | 2.5 | 12.6 | 1.1 | 1.23 | 14.2 | 295 |

Les composants signalés par * sont les parasites à modèle enrichi.

Le travail est effectué avec une machine Intel Core i5-3470S munie d'un Processeur à 2.9GHz

l'alimentation en tension VDD est 14V.

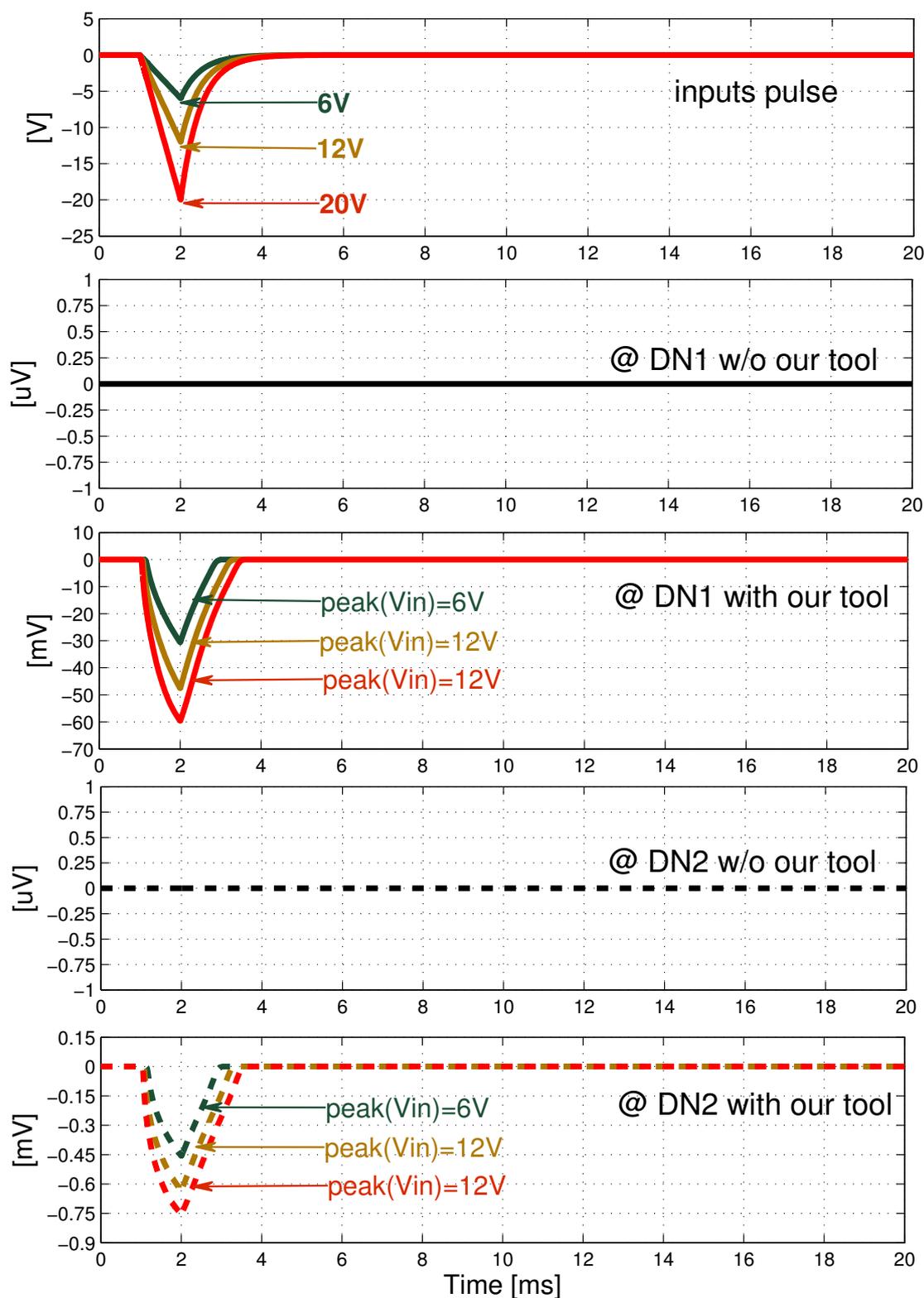


Figure 15: Résultat de la simulation transitoire avec test impulsionnel pour l'automobile: de tension de crête 6V, 12V ou 20V. Les tensions simulées en sortie sur 50Ω avec ou sans notre outil. L'option de découpe au laser permet de choisir le Nwell : DN1 ou DN2.

Les résultats de cet essai sont présentés figure 15 lorsque la tension à la sortie " V_{out} " est mesurée sur 50Ω . Les courbes sont affichées en fonction des différentes valeurs des tensions de crête: 6V, 12V et 20V. Les signaux provoqués par le couplage à travers le substrat ne peuvent pas être simulés de manière classique. En utilisant notre outil, nous pouvons observer des signaux impulsionnels sur le puits correspondant (DN1 et DN2). Comme prévu, le signal simulé est plus élevé pour le signal d'entrée de plus grande amplitude. Une distance plus courte à la source de courant dans le substrat produit, comme prévu, un signal d'amplitude plus élevée.

Conclusion

La modélisation des bruits de substrat est critique pour les circuits intégrés de puissance. Les bruits de couplage dans le substrat sont dus à l'injection et à la propagation des porteurs, particulièrement en provenance des dispositifs haute tension. Les effets de ces porteurs sont amplifiés à haute température. De tels bruits de couplage par le substrat ne sont pas prévisibles à l'aide d'une simulation SPICE standard qui ne propose pas de modèle compact du transistor parasite NPN latéral dans le substrat. Dans cette thèse, nous avons présenté une méthode d'extraction et simulation post-layout des parasites du substrat. Cette méthode repose sur un outil de maillage du layout et de génération de netlist de composants parasites pour représenter le comportement du substrat. L'utilisation de notre outil complète le flot existant de vérification après le layout. Le comportement des courants de substrat peuvent alors être pris en compte dans la simulation post-layout. Nous avons extrait les paramètres technologiques du modèle de substrat pour diverses structures de référence en technologie ams AG HV-CMOS $0.35\mu m$. Nous avons étudié dans ce travail l'effet du transistor bipolaire parasite NPN latéral dans deux cas de test : les perturbations par les courants de substrat d'un miroir de courant dans un premier cas, puis un cas de test standard pour une application automobile. L'approche proposée donne aux concepteurs la possibilité de simuler le comportement du substrat. La vérification précoce du système, avant fabrication, permet de protéger le circuit conçu des effets du couplage par le substrat. Finalement, elle contribue à réduire le cycle de conception et augmente ainsi la fiabilité et la sécurité des circuits intégrés intelligents de puissance.

Chapter 1

Introduction

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1.1 Overview

The modern trend of microelectronics is to integrate more functionalities on a single chip, along with reducing the total number of external components, as well as space, weight and the overall costs. Thus, it increases the reliability of electronic component and reduces electromagnetic interference (EMI) of the entire system. One possible implementation is the Smart Power integrated circuit (IC) [8] which comprises power control, computational functionalities, sensing and diagnostic capabilities.

This kind of integrated circuit is a very common choice that is increasingly required by today's market, especially the automotive industry. Besides, it becomes more attractive recently since more and more electronic applications will be connected together, for the sake of Internet of Things (IoT). The IoT allows more physical objects to be sensed and controlled remotely across the existing network infrastructure, such as "smart car" and "smart home". Today, a typical fully electrical vehicle contains up to 300 Smart Power ICs.

In the Smart Power technology [7, 8, 20], high voltage (HV) devices and low voltage (LV) analog and digital devices are both integrated on the same silicon substrate. This kind of integration may cause unwanted parasitic coupling in the substrate. Besides the voltage level, it has to withstand harsh environment conditions like high operating temperature (HT). Under such conditions, the impact of substrate parasitic coupling becomes even worse, thereby it is quite challenging to ensure immunity against substrate parasitic. Unlike the traditional ICs in LV technology with

mixed-signal, where the noises come from fast switching of digital circuit or radio frequency (RF) circuits or supply line perturbations, the noises in the Smart Power ICs is caused by large voltage swings arising from power domains.

In Smart Power IC, the power transistors are usually used in HV driver for power switching. In such devices, the drain connects out to an inductive load, as shown in figure 1.1. The injection of carriers (electrons and holes) in a p-type substrate occurs when inductive loads are switched off. During switching, the voltage drop will lead to the well-known current recirculation phenomena [8, 15]. The potential at drain of power transistor instantly goes below ground, leading to the forward biasing of the drain-substrate junction. The induced substrate current consisting of electrons leads to a local shift of substrate potential that can reach hundreds of millivolts.

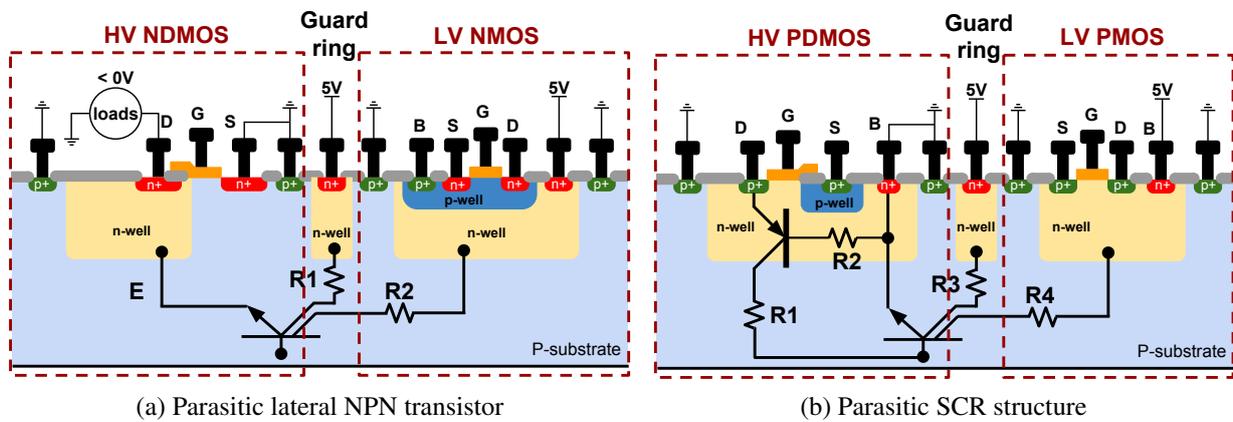


Figure 1.1: Substrate noise coupling due to possible activation of (a) parasitic lateral NPN transistor, and (b) parasitic silicon controlled rectifiers (SCR) structure.

As a consequence, this voltage drop can disturb the normal system operation and deteriorate system performances. Since substrate currents due to minority carriers' injection are significant, inherent parasitic components cannot be neglected by simulation. The minority carriers, in 3-D substrate, propagate and may be collected by nearby noise-sensitive devices. With the presence of multi-collector parasitic lateral NPN bipolar junction transistor (BJT), the path of parasitic coupling can be severely long and layout dependent. This parasitic coupling may cause destructive effects such as triggering the substrate thyristor. As technology improves, HV devices are getting larger to deliver more power, at the same time LV devices are shrinking to provide higher frequency and less power consumption, which implies that the substrate parasitic coupling will cause more and more failures.

Addressing failures due to minority carriers is becoming of interest, since these failures are still reported in tests after fabrications. On the one hand, designers adopt the conventional IC design flow to design Smart Power IC. However, the conventional IC design flow, of the LV mixed-signal, ignores the minority carriers related effects which are in our case significant. On the other hand, modeling of this multi-collector parasitic lateral NPN BJT is still the missing part in the

standard IC-CAD because of the following reasons. First, standard compact models consider a full recombination of minority carriers at the device terminals, hence they cannot simulate the continuity of minority carriers in the substrate. Second, the impacts of minority carriers in the substrate are hard to model since they are layout dependent.

Facing these problems, it is essential to enhance the existing IC-CAD (Computer-Aided-Design) environment for designing a Smart Power IC, where the immunity against substrate parasitic is one of the keys leading to successful design. The emergence of design methodology for this kind of failure analysis will definitely favor the development of this research direction.

1.2 Contribution

The main objective of this thesis is to model the minority carriers' propagation in the substrate and enhance existing design methodologies to design efficiently Smart Power IC. The following points summarize the main contributions realized in this work.

Methodology for Substrate Parasitic Extraction: We have introduced a new methodology to model the parasitic coupling in the substrate of Smart Power IC. The model consists of a netlist of components which can handle the minority carriers' propagation in the substrate. This netlist is extracted from layout and can be simulated with a spice-like simulator. To construct this netlist, we have developed a substrate meshing strategy in 3-D that allows the construction of meshes based on the layout geometry. This substrate equivalent netlist consists of many lumped parasitic components. These components are the EPFL enhanced models of diode, resistor and homojunction [37]. Based on the describing methodology, we have developed a complete IC-CAD framework at post-layout.

Optimization of 3-D Substrate Meshing and Parasitic Extraction: One of the key factors in high quality layout extraction is the resolution, known as grid size or dimensions. The smaller the grid, the more lumped elements will be extracted. Thus simulation results could be more accurate yet much more time consuming. However, a massive number of simulated components may disturb the simulator due to inconvenient convergence issue. The accuracy of parasitic noise analysis is not as important as simulation time, because the parasitic substrate model basically gives an insight of parasitic noises and should not slow down the entire system simulation. A good trade off between accuracy and efficiency is significant for a full-chip size analysis. We have introduced a new mesh structure for silicon substrate modeling. The idea of meshing optimization is first developed in 2-D surface layout and then extended to 3-D volume layout. The enhanced mesh structure leads to reduction in the number of extracted components and speed up in simulation time.

Methodology Validation: The process design kit (PDK) integration is one of the major tasks in the work, because it eases the design process of Smart Power IC and evaluates our methodology in different technology processes. However, such integration is a hard task, because the silicon fabrication processes differ from one to another. They have different layer systems, doping strategies and shielding structures, etc. To validate our modeling methodology, we are involved into 2 different Smart Power Technologies. First, we have integrated our IC-CAD tool into hitkit of *ams AG* for the 350nm HV-CMOS technology process. Thanks to this integration, we are able to investigate the impact of minority carriers in the substrate from the simply benchmark structures to complex industrial test chips used in automotive applications. Second, we have also installed our CAD tool into design environment of *STMicroelectronics*, it enables us to investigate the influences of minority carriers in BCD technology (including deep trench isolation).

1.3 Outline

This part gives a brief overview of the overall organization of the thesis:

After a brief introduction in this chapter, chapter 2 defines the main problem that we are dealing with in this thesis, where the substrate parasitic coupling due to minority carriers' injection and propagation in substrate are the major issues that cause circuit redesign in smart power technology.

Chapter 3 is the state-of-the-art work related to parasitic noise analysis due to minority carriers where the physical device simulation based methodology and the state-of-the-art parasitic compact model based methodology are reviewed.

Chapter 4 presents in detail the proposed methodology for parasitic substrate extraction. A layout-to-netlist extraction engine including 3-D meshing strategy is added to a standard CAD framework. As an example under study, we demonstrate the idea on a simple structure, and compare results of circuit simulations to the one from physical based device simulation.

Chapter 5 introduces an optimized mesh structure. The proposed optimization strategy is performed in three steps: 2-D surface layout optimization, 3-D volume layout optimization and meshing strategy of sub-regions. Case study including two n-wells in substrate is performed by investigating the parasitic lateral NPN bipolar transistor.

Chapter 6 presents experimental results. First benchmark structures used to calibrate the technology parameters for substrate PN junctions are discussed. Then several test cases in transient simulation are considered. One case is a common used current mirror circuit. The interference of substrate currents to this basic circuit is predicted by our tool. Another case is an industrial design test chip where parasitic coupling is investigated in a standard automotive test.

Chapter 7 concludes this research work with some guidelines for future work.

Chapter 2

Motivation and Problem Definition

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2.1 Introduction

The invention of Smart Power technology contributes to miniaturize the electronic systems and hence integrate more functionalities all together on a single chip. The automotive application is a growing market for Smart Power ICs, especially Fully Electrical Vehicle (FEV).

In section 2.2, a brief introduction about Smart Power IC is given. The Smart Power IC incorporates high voltage and low voltage devices together on the same chip. As a feature, it provides both decision making, sensing and diagnostic and power control capabilities.

In section 2.3, the failures due to substrate noise coupling of Smart Power IC are discussed. The sources of this coupling noise are the injection of the majority and minority carriers in the substrate. The majority carriers propagation is well modeled, however, the minority carriers propagation cannot be correctly modeled by standard compact models.

In section 2.4, we point out that the increasing needs in automotive drive the motivation for increasing the immunity against substrate coupling of HV/HT electronic automotive circuits, which also motivate the European Project AUTOMICS. A brief introduction of this project is included.

In section 2.5, we conclude this chapter.

2.2 Smart Power IC

2.2.1 Background

The traditional approach to develop an application was to combine a number of chips implementing different functions on the same circuit board. Each chip has a distinct function that is realized in a specific process technology, for instance CMOS for digital logic and bipolar for analog functions.

When the modern system demands more and more functionalities, such as electronic compass and navigation system, auto distance cruise control, and even autopilot system in the Fully Electrical Vehicle (FEV) as shown in figure 2.1, the development of system in the traditional way has a limit in terms of size and weight, as well as the overall cost.

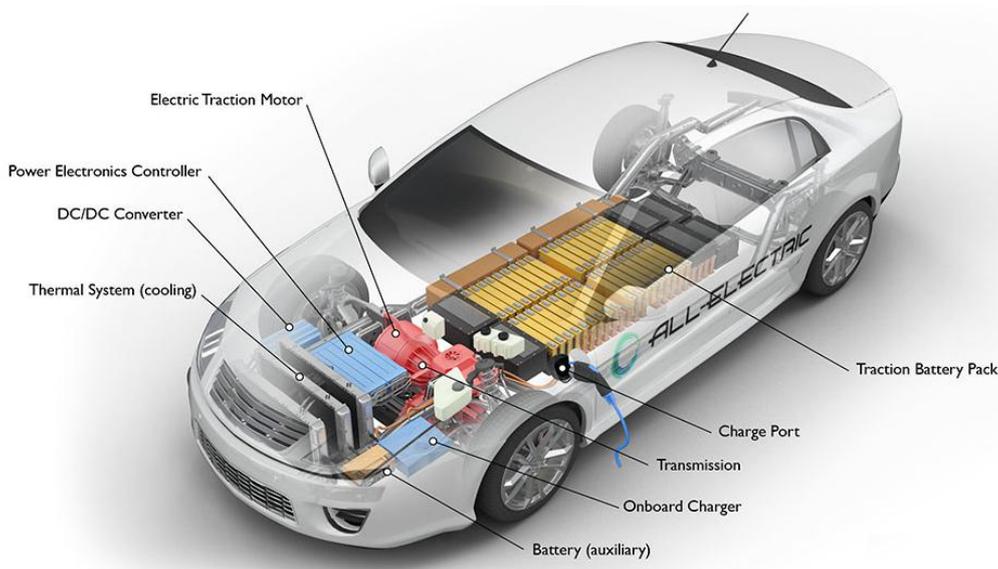


Figure 2.1: A fully electrical vehicle (FEV). Photo: U.S. AFDC [6]

As a consequence, today's market requires the combination of different functions on the same ASIC (Application-Specific Integrated Circuit). The system integration brings several advantages:

- reducing the size and weight of overall system;
- saving the silicon area, thus save the cost of overall system;
- reducing the total number of external components;
- reducing the electromagnetic interference (EMI);
- increasing the reliability and safety of electronic components;

and meanwhile the disadvantages:

- increasing parasitic interferences between different systems;
- prolonging the design and verification processes;
- increasing the cycle of time-to-market;

2.2.2 Description

In the power electronics industry, a new family of integrated circuit was invented in the year of 80s, called “Smart Power IC” [8]. It has received increasing attention due to its unique capabilities to merge sensing, computational and power functions in the same chip, as shown in figure 2.2. In order to combine these functions together, low voltage (LV) logic circuitry is integrated in the high voltage (HV) and high temperature (HT) power IC.

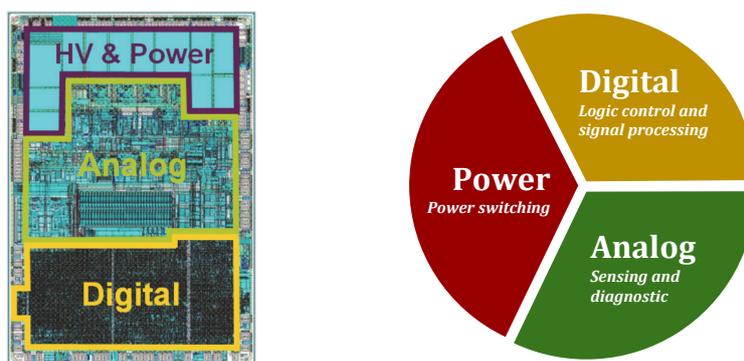


Figure 2.2: Smart Power IC (left, photo: *cmp* [2]), and its main function blocks (right).

Inside a chip of Smart Power technology, a part comprises HV domain, and the other part comprises LV domain consisting of analog and digital circuits. The HV section intends to offer power distribution and power conversion (e.g. motor control and DC-DC convertor); the LV analog blocks intend to interface the external world to digital systems (e.g. sensing and diagnostic); and the LV digital core is used for logic control and signal processing. As a consequence, the power devices (e.g. DMOS), analog (e.g. bipolar) and digital circuit (e.g. CMOS) are all integrated on the same silicon substrate.

Smart power ICs have evolved over the last few decades due to the need for more advanced electronics, from a simple driver circuit of power switching, to a complex System-on-Chip (SoC) including both power, analog and digital devices. A typical application using this kind of technology is motor control where power switches, power driver, electronic protection and control logic are required in a fully integrated IC.

The integration of functions leads to the development of very complex manufacturing process compared to the traditional LV CMOS technology. For instance, the HV-CMOS technology and BCD technology:

- *High-Voltage CMOS (HVCMOS)* Technology is an extension of standard CMOS technology where additional steps are added in the process flow to create high-voltage and high-power transistors. It targets to HV applications with complex analog and mixed signal circuits involved. In addition to the standard CMOS transistors, this technology provides also high

voltage transistors, such as HV-NMOS, HV-PMOS, HV-DMOS transistors etc. Within this technology, high voltage and standard devices can be combined into the same chip.

- *Bipolar-CMOS-DMOS* (BCD) technology has been invented around the mid-eighties [7, 20]. This process technology allows to mix on the same chip different structures, such as Bipolars for precise analog functions, CMOS for digital design and DMOS structures for power and high voltage elements. By integrating three distinct types of components on a single die, this technology helps to reduce the number of components, area required on the board, thus driving down costs. The technology BCDs8AUTO of STMicroelectronics-Italy is investigated in this work.

To implement such power applications, different aspects have to be taken into account in order to meet automotive industry standard. The design of robust applications have to consider high operating temperature, high voltage, high electromagnetic fields, hard transient disturbance and reverse polarity capability [11]. To protect circuit against over-current, over-temperature and short-circuit, circuits for detection as well as corresponding protection are required.

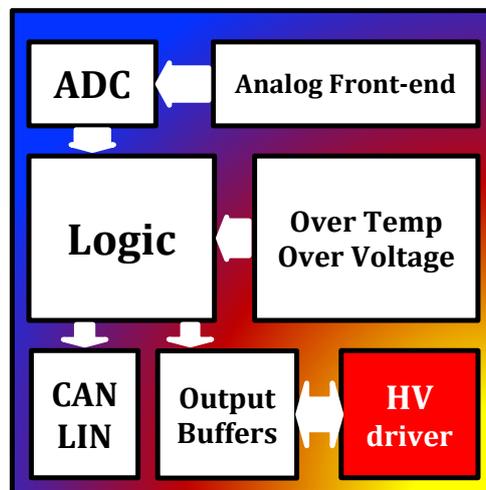


Figure 2.3: Typical automotive block diagram of Smart Power IC.

Power devices are used in HV output stage to control power loads. They consist of power driver that translates the logic level signal (e.g. command) received from central processing units to a power switching signal (e.g. PWM). The analog front-end receives inputs from different transducers which convert the continuous quantities to be measured into continuous electrical signals. These analog signals are filtered, amplified and then converted into digital domain by Analog-to-Digital Converter (ADC). The logic unit is a central processing unit, which performs the logic level controlling and signal processing. It manipulates the inputs, then, based on these inputs it responds with the convenient outputs.

2.3 Substrate Parasitic Interference

2.3.1 Basic physics

A thermal process is used extensively in IC fabrication [28]. This process is used to modify the conductivity of semiconductors by introducing impurities into the silicon material. Therefore, the semiconductor with higher concentration of impurities has more conductivity. The amount of impurity, or dopant, added to an intrinsic (pure) silicon material varies its level of conductivity so that PN junctions can be formed. The formed PN junction is a basic block of semiconductor devices. The process of adding controlled impurities to a semiconductor is known as “doping”.

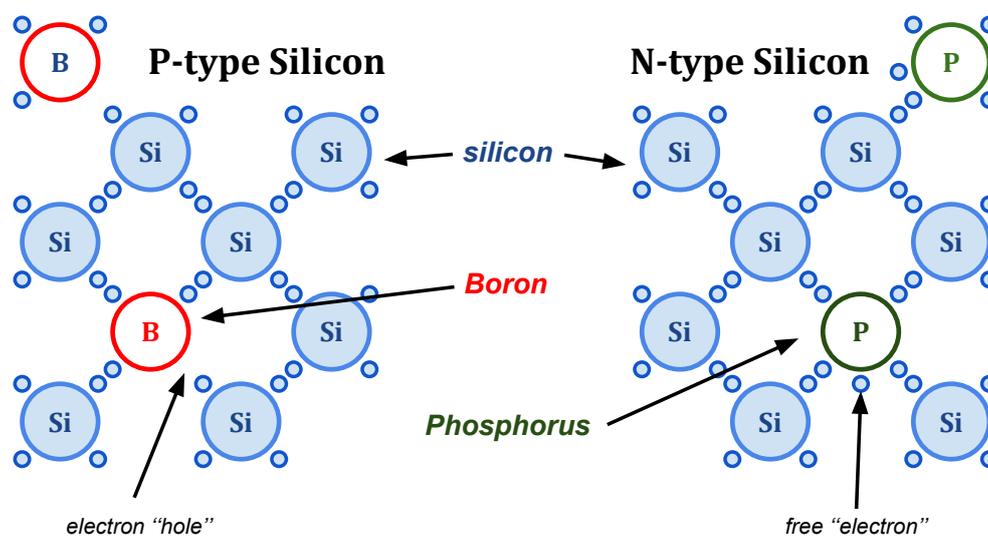


Figure 2.4: Doping of p-type (left) and n-type (right) silicon.

The materials chosen as dopants depend on the properties of both the dopant and the material to be doped. In general, dopants are classified as either electron acceptors or donors, and the most common dopants are “Boron” and “Phosphorus”, as shown in figure 2.4.

“Boron” contains three valence electrons that makes it to function as electron acceptor when used to dope silicon. Hence, it will attract one silicon electron to complete its valence band, thus creating an electron “hole” so that a p-type silicon is created. In this case holes are majority carriers and electrons are minority carriers.

“Phosphorus” have five valence electrons, which causes free “electrons” when used to dope silicon. This type of silicon with excess of electrons is called n-type silicon, while electrons are majority carriers and holes are minority carriers.

In general, the current can be carried by electrons or holes, and the displacement of these carriers in silicon generates the currents.

2.3.2 The Origin of Substrate Noise

In LV analog and mixed-signal IC, the noises originate from fast switching of digital circuits, or RF circuits or disturbances on the supply lines. Most of these noise currents flow in metal connections or near the surface of the substrate. Such noise is due to majority carriers and can be modeled by R-C network from conventional modeling methodologies [23, 46, 30, 25, 40, 22].

In HV power IC, the HV devices are used in a circuit in switching mode, normally at output stage that connect to inductive load, e.g. the electrical motor. Wide system application fields in automotive need high voltage and/or high current capabilities, typically from 5 to 200 volts and from micro to several tenth of amperes. Hence, the noises originate from switching of power stages or high chip temperatures arising from power domains. Switching of power stages are the reason for carrier injection into the substrate.

2.3.2.1 H-bridge operation

To illustrate the issues, an H-bridge circuit, as depicted in figure 2.5, is discussed in this section. The H-bridge is an electronic circuit that is commonly used in automotive applications. This circuit is designed for controlling the applied voltage across a load in two directions: i.e. forward or reverse the motor.

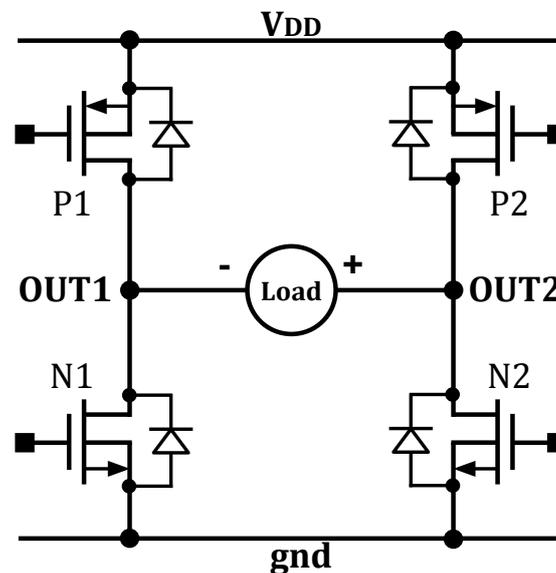


Figure 2.5: Classical H-bridge circuit configuration for motor control.

Four switching elements are used in a typical H-bridge configuration, each one is a HV power transistor (e.g. LDMOS). Two HV p-channel LDMOS transistors ($P1$ and $P2$) are on the high side connected to a power supply V_{DD} , and the other two are HV n-channel LDMOS transistors ($N1$ and $N2$) that are on the low side connected to the ground. The output is connected between “OUT1” and “OUT2”.

To control the motor, we need to switch on or off both the diagonal opposed transistors. For example, in reverse direction, transistor $P1$ and $N2$ are both turn on while the other two transistors are switched off. Under such condition, the current flows from power supply, through transistor $P1$, the load and transistor $N2$ then to the ground, as illustrated in figure 2.6a.

It has to be noticed that two transistors at one side cannot be both switched on at the same time, because it may directly short circuit the power supply to ground. Before switching to forward direction (figure 2.6c), the four transistors of H-bridge should be switched off during a fixed period of time, called the dead time, to prevent the circuit from damage.

At this moment (figure 2.6b), the inductive load tries to keep a continuous current flow, because the electrical motor cannot be stopped instantly and the only possible current path is through the free-wheeling diodes (red) of transistors $N1$ and $P2$. This current flows through the free-wheeling diodes, thus it generates a potential at the drain of $P2$ (i.e. $OUT2$) above power supply and at the drain of $N1$ (i.e. $OUT1$) below ground. This above supply and below ground condition leads to carriers injection due to majority carriers and minority carriers.

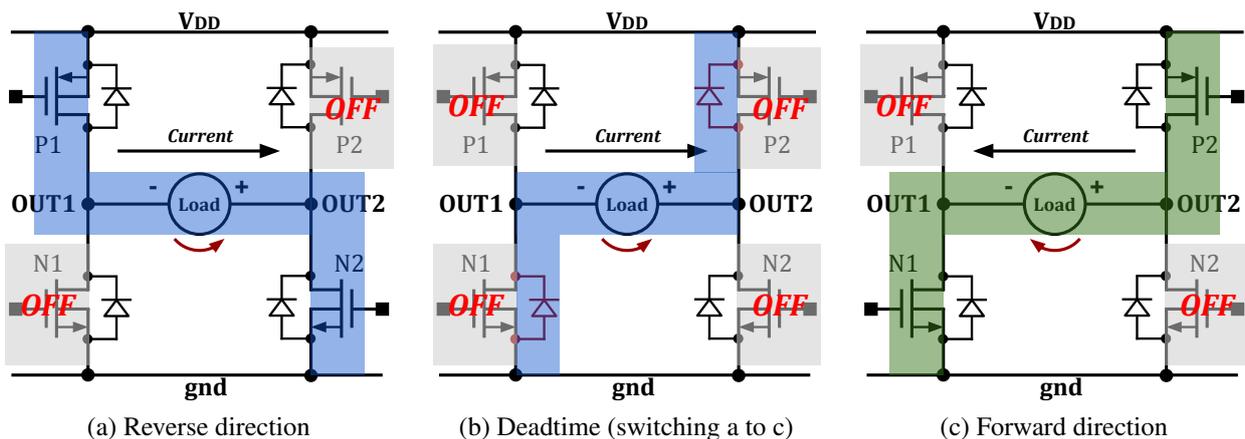


Figure 2.6: H-bridge operation and switching from reverse to forward direction.

2.3.2.2 Carriers Injection Due to Majority Carriers

At the right side of figure 2.6b, transistors $P2$ and $N2$ are involved. Figure 2.7 draws the layout cross-sectional view of these two transistors.

At the above supply condition, a forward biased drain-bulk PN junction in transistor $P2$ triggers the inherent parasitic vertical PNP (i.e. $Q1$ in figure 2.7) BJT. The drain of transistor $P2$ is the emitter, the n-well is the base while the whole substrate is the collector.

As a consequence, the currents consisting of holes are injected into the substrate and flowed to the substrate contacts. The excess of electron holes in substrate causes a positive shift of local

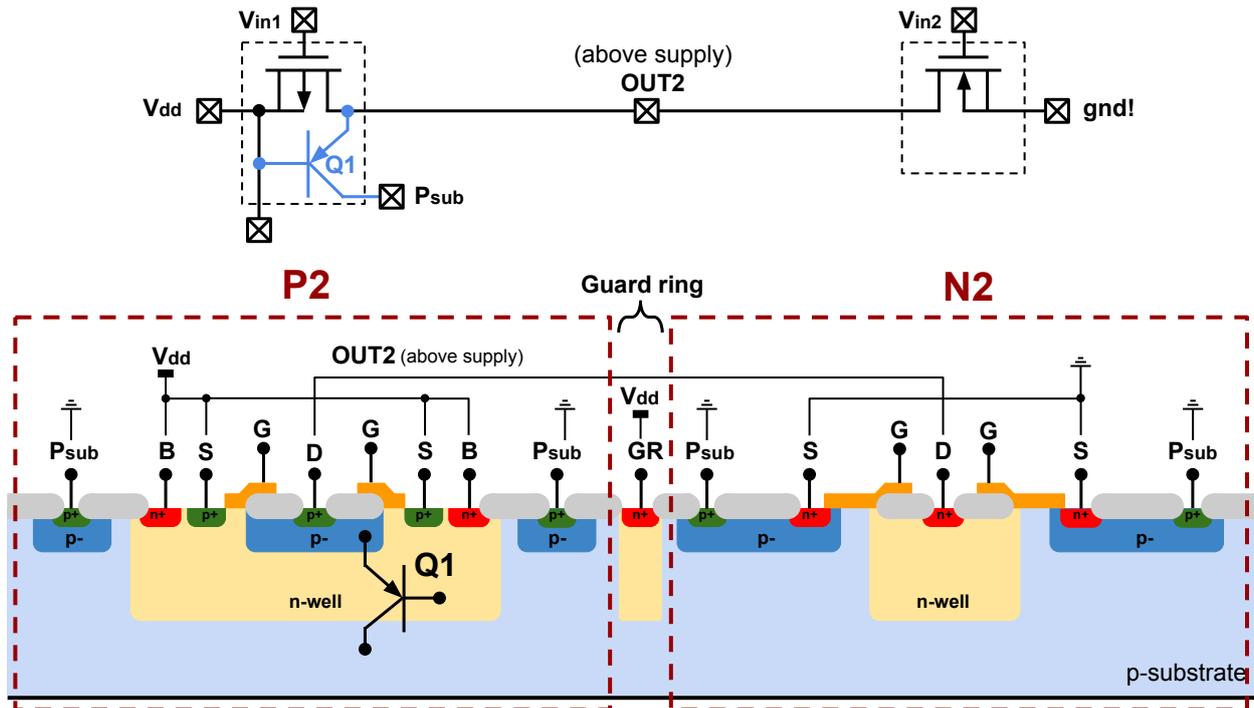


Figure 2.7: Schematic and layout cross-section view of half H-bridge at above supply condition.

substrate potential. This positive potential shift can lead to junction isolation failures, especially at n-wells on low potential.

In this case, we have to face the problems of:

- the risk of forward-biased isolation junction at different grounding configuration;
- this parasitic vertical PNP transistor has well-defined emitter and base, however the collector is the whole substrate. In some process/models, the modeling of such BJT use standard compact model which takes into account this majority carrier injection.

2.3.2.3 Carriers Injection and Propagation Due to Minority Carriers

At the left side of figure 2.6b, transistor $P1$ and $N1$ are involved. Figure 2.8 draws the layout cross-sectional view of these two transistors.

At the below ground condition, the potential at drain of transistor $N1$ goes below the substrate potential. It results in a forward biased substrate-drain PN junction in transistor $N1$ that triggers the parasitic lateral NPN BJT, as $Q2$ shown in figure 2.8. Clearly, the drain of transistor $N1$ is the emitter, the whole substrate is the base and the other N-wells in the substrate are the collectors, e.g. n-type guard ring and the N-well of transistor $P1$.

As a consequence, the currents consisting of electrons are injected into the substrate by the forward biased substrate PN junction at transistor $N1$. Electrons flow to the rest of the substrate

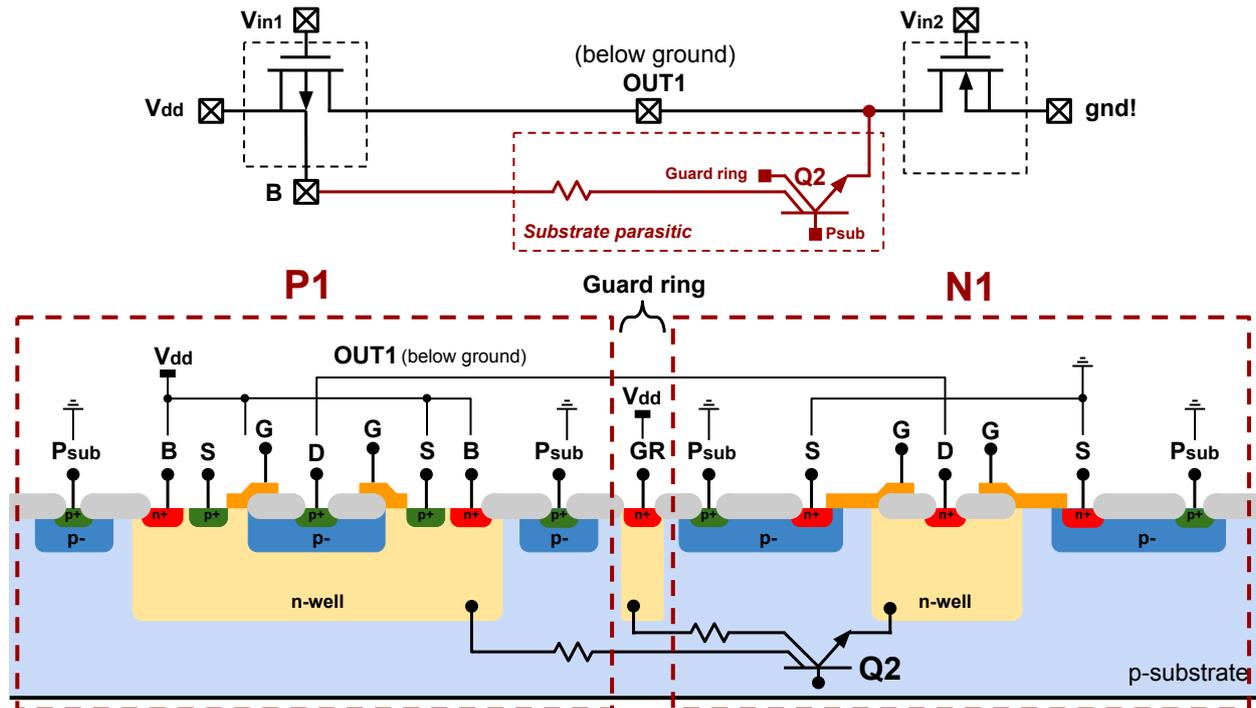


Figure 2.8: Schematic and layout cross-section view of half H-bridge at below ground conditions.

thanks to their long carrier lifetime. This minority carrier injection leads to a negative potential shift in substrate which is not harmful to the HV transistor *N1* itself, because it supports the reverse bias of the isolation junction structure.

However, the injected electrons can be collected by any other N-wells in the substrate even at a long distance. The electrons collected by N-well can disturb the normal function of LV devices and compromise the system performance. For instance, the current mirror circuits depend directly on the ratio of the collector currents of the two transistors used. Thus, “current mirrors can easily be disturbed by substrate currents” as quoted in [34].

In this case, we have to face the problems of:

- the risk of triggering the parasitic lateral NPN transistors, which has the whole substrate as base and collectors located anywhere in the chip;
- the risk of triggering the destructive effect due to the structure of parasitic thyristor;
- the modeling of such lateral NPN BJT due to minority carriers is difficult, because such parasitic BJTs cannot be modeled by using compact BJT model and they are layout dependent.

2.4 Motivations and European Project

2.4.1 Motivations

In the previous section, the problem of substrate parasitic due to carriers injection and propagation are clearly stated. So the question is why are we interested in such problem, especially for HV/HT Smart Power ICs ?

To answer this question, we have to point out the following three points:

- Unlike the traditional IC in LV technology, the Smart Power ICs have to withstand harsh environmental conditions like high operating temperatures. Due to high chip temperature arising from power domains, the substrate noise increases and the impact of substrate coupling becomes even worse.
- As technology improves, HV devices continue to get larger to deliver more power, in the meantime LV digital devices are shrinking to provide higher frequency and less power consumption. Therefore, substrate noise from power domains can be more important and at the same time the LV blocks become more sensitive, hence it can be quite challenging to ensure immunity against parasitic coupling.
- Failures due to coupling of substrate lateral NPN BJTs cause several circuit redesigns. Addressing such failures is becoming of interest since these failures are still reported in tests after fabrication.

2.4.2 EU project: AUTOMICS

The AUTOMICS project aims at solving such problem, and proposing a new pragmatic, focused and well-structured solution for modeling and fast simulation for HV/HT automotive ICs. European Commission founded the AUTOMICS project within the 7th framework (2012-2015). The motivation of AUTOMICS project were mentioned in [27] and summarized as follows.

“In the automotive industry, one of Smart Power ICs applications is motor management IC that comprises four power transistors in H-bridge configuration with their drivers and protection circuitry. In such safety critical applications, substrate current effects lead to serious quality and reliability problems if they are not detected before delivery of the system.”

“In terms of reliability issues, it has been observed that the number of chip defects in junction isolation technologies due to EMI, ESD and substrate parasitics have increased from 20% (2000-2010) to 40% (2010-2015) and remained 20% for trench isolation technology (2010-2015). Another concern, related to risk assessment, is the fixing a bug due to a substrate parasitic is never

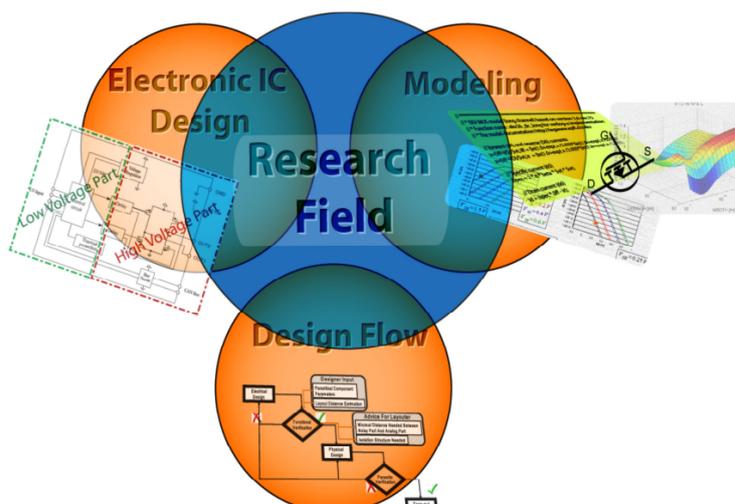


Figure 2.9: Illustration of the fields of research involved in the project [27].

fully under control by the designer since it cannot be simulated. It is always dealt with after fabrication through chip measurements.”

At the start of the project, “the lack of design methodology prohibited an efficient design strategy and failed at giving clear predictions of electrical perturbations in high voltage integrated circuits. Industry reports that for 10-15 years lifetime product chips, these have globally more than 10 versions of the chips during development and fabrication. Therefore, the time to market is increased. Therefore, AUTOMICS project significantly contributes to reduce the cost of automotive ICs, ensures fail-safe operation of electronic components and ameliorates the safety in fully electrical vehicle. With the new developed design methods and tools, cost reduction is achieved by reducing IC die size due to the optimization of guard rings to protect against parasitic effects.”

“With this proposed technique, 3% to 6% die size reduction is feasible, leading to 2% to 6% savings in component cost. In a typical business of 5M€ per year and per IC, this represents 100k€ to 300k€ savings per year and per IC. Moreover, considering an average number of 3 full mask and 2 metal mask steps for such complex IC development, then for a realistic saving of 1 full mask with the new methods and tools, the development cost will be decreased by 10% to 20%. For a typical development cost of 20M€ (system supplier and semiconductor foundry), the saving on R&D budget is expected to range from 2M€ to 4M€.”

This project has involved three main domains, namely *Electronic IC’s design*, *Design flow* and *Modeling*. All these research areas collaborated in AUTOMICS as shown in figure 2.9.

- *Modeling development*. EPFL* was responsible for developing the enhanced parasitic model that extend existing model from state of the art.

*École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, CH-1015, Switzerland.

- *CAD development.* UPMC[†] was responsible for developing the CAD framework for parasitic substrate extraction and to integrate different process technologies.
- *Electronic IC design.* Two foundries (*ams AG*[‡] and *STMicroelectronics-Italy*[§]) were responsible for design and measure the benchmark chip and industrial validation. *AdMOS*[¶] was responsible for extracting and calibrate the technology parameters. *Valeo*^{||} and *Continental*^{**} were responsible for industrial chip benchmark and validation.

2.5 Conclusion

In this chapter, the motivation and problem that we are facing with are clearly stated.

The Smart Power technology has been invented in the year of 80s after the demand of function integration. This “hybrid” technology merges low voltage control logic functions into high voltage and high temperature power IC that share the same silicon substrate. This invention contributes to reduce die size and the cost of entire system.

Such integration in the same substrate leads to unpredictable substrate parasitic. The substrate parasitic becomes significant in HV technology due to the carriers injection and propagation in the substrate. The failures due to parasitic coupling cause several circuit redesigns and prolong the cycle of time-to-market, because such failures are still reported in tests after fabrication.

The lack of modeling of such parasitic is the major problem in the conventional IC-CAD environment. First, because the standard compact model ignores the effect of minority carriers between devices. Second, substrate parasitic are highly layout dependent. Therefore, the above points motivate the European Project AUTOMICS as well as this thesis.

[†]Université Pierre et Marie Curie Paris 6, 4 Place Jussieu, 75005 Paris, France

[‡]ams AG, Tobelbader Strasse 30, 8141 Unterpremstaetten, Austria

[§]STMicroelectronics, Milan, Italy Tobelbader Strasse 30, 8141 Unterpremstaetten, Austria

[¶]Advanced Modeling Solutions, In den Gernaeckern 8, 72636 Frikenhausen, Germany

^{||}Valeo, 43 Rue Bayen, 75017 Paris, France

^{**}Continental Automotive France SA, 1 Avenue Paul Ourliac, 31100 Toulouse, France

Chapter 3

State of the Art in Substrate Parasitic Modeling

Contents

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3.1 Introduction

In the previous chapter, the problem of minority carriers in substrate, responsible for substrate parasitic coupling is clearly stated. Smart power ICs are employed in the automotive industry since they incorporate the high-voltage (HV) and low-voltage (LV) circuits on the same die [8]. This feature allows us to miniaturize the electronic systems and implement more functionality in the vehicles. However, the substrate noise coupling in the Smart Power ICs becomes a severe issue. Failures due to the substrate noise coupling are still reported in tests after fabrication. Most of these failures are caused by the minority carriers' propagation since their behavior cannot be predicted by the current commercial tools. Therefore, we need to investigate the minority carriers propagation in the substrate and their modeling techniques to validate the capability of simulation for such complicated behavior.

In Smart Power ICs, the HV circuits commonly drive inductive loads. The presence of such loads stimulates parasitic components and injects minority carriers in the substrate. The noise due to minority carriers injection is a function of the operating voltages and currents. This noise becomes non negligible and can cause significant effects, such as latch-up. Therefore, techniques were investigated to study the substrate coupling due to the minority carriers propagation.

This chapter introduces the state of the art in substrate parasitic modeling. The remaining of this chapter is organized as follows: In section 3.2, we present the parasitic extraction and simulation approach in the conventional way. We introduce several approaches related to modeling techniques or design methodology to deal with this kind of issue with or without minority carriers involved. In section 3.3, we present the EPFL modeling methodology. This method relies on the substrate parasitic models which take into account the minority carriers in circuit-level simulation. And finally, we conclude the chapter in section 3.4.

3.2 State of the Art in Parasitic Modeling

In a typical analog and mixed-signal IC, the parasitic noise mainly originates from fast switching of digital circuits. This kind of parasitic noise takes only the majority carriers into account. Most of the noise currents operate at high frequency and are distributed through either metal wires or inside substrate. This kind of parasitic can be modeled using passive components. These components can be capacitances, inductances or resistances. In fact, the cross-talk between two metal lines will lead to an equivalent coupling capacitance. Similarly, parasitic serial resistances can be attributed to the resistivity of metal wires. An equivalent schematic modeling the propagation of parasitic currents can be built using these passive components. This schematic containing all extra components is then added to the original schematic to model the possible coupling occurring in the chip.

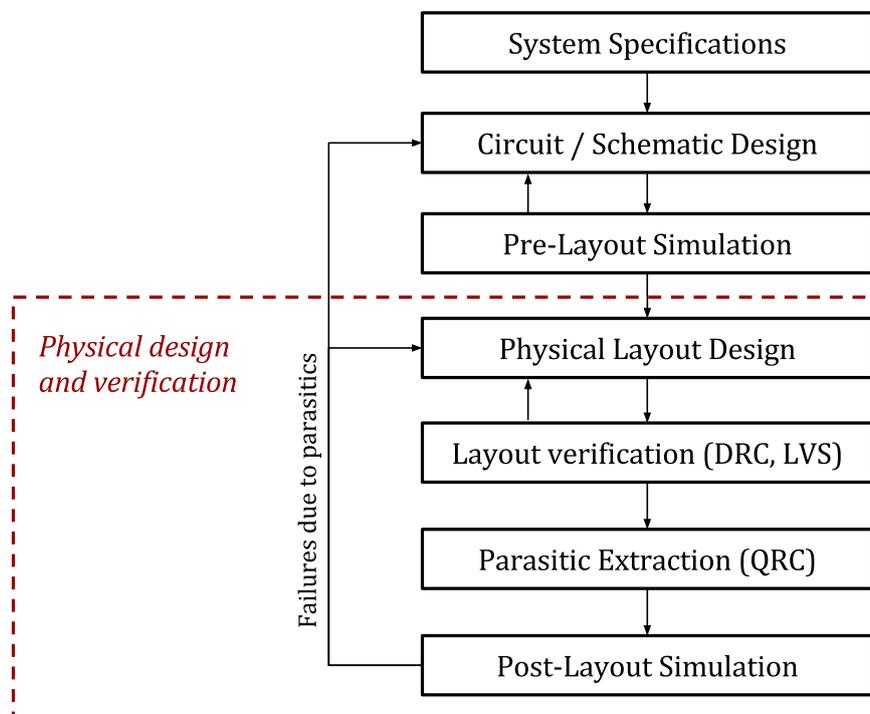


Figure 3.1: Illustration of the conventional IC design flow including post-layout verification.

In order to validate the physical design, layout has to be verified by post-layout simulation. The

final netlist including parasitic can be simulated using the same testbench used during the design phase. Post-layout simulation is performed in order to be sure that the system specifications are still met when including parasitic interconnections.

In the conventional approach (Figure 3.1), verification software, like Assura^{*}, Calibre[†], and StarRC[‡] are the major EDA tools available in the market. They are able to extract from the layout the describing parasitic components, responsible for cross-coupling between transistors. However, this approach is mainly used to model metallic interconnections coupling between transistors.

3.2.1 Methodologies Using Substrate Parasitic R-C

Several design methodologies have been developed for the reduction of substrate noise couplings in mixed-signal integrated circuits. Guard rings and different substrate grounding schemes are the most common solutions employed to reduce substrate noise. These solutions when implemented in a complex mixed-signal IC design, can be evaluated through post-layout simulations of the extracted R-C substrate parasitic model.

The parasitic coupling from metal interconnection are represented by R-C network. Based on the same idea, EDA tools developed in [45] and [12] are focusing on the parasitic extraction in the substrate. They model the cross-coupling occurring inside the substrate, thus both take only the majority carriers into account.

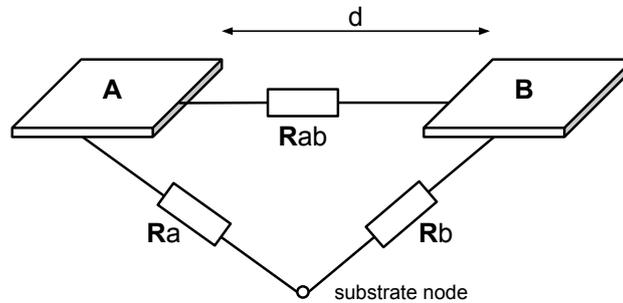


Figure 3.2: Model for a configuration with two substrate terminals [45].

In [45], the impact of substrate parasitic coupling was verified by computing the substrate resistances between: 1) the parts of circuit that inject noise into the substrate; 2) and the parts that are sensitive to it. A representation of the substrate network is shown in Figure 3.2. They describe two different methods for substrate resistance calculation and the methods have been implemented in a practical layout-to-circuit extraction program called “SPACE”. One method is an accurate 3-D boundary-element technique that can be used for circuits containing up to few hundreds of substrate terminals. The other method is a fast interpolation technique that can be used for VLSI.

^{*}Cadence Assura Physical Verification tools [1]

[†]Mentor Graphics IC verification and Signoff [3]

[‡]Synopsys Parasitic Extraction tool [4]

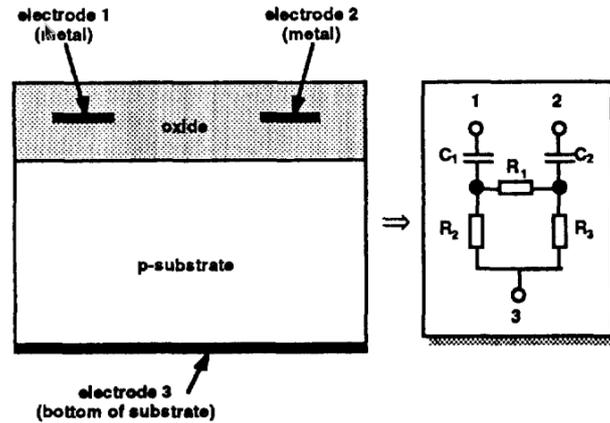


Figure 3.3: Structure simulated with “LAYIN” in [12].

In [12], the authors present a CAD tool, named “LAYIN”, dedicated to substrate parasitic coupling modeling and visualization. A representation of the layout and a specific technology description are used to extract a simple substrate parasitic coupling model. This model consists of resistors and capacitors only. The output is spice compatible and includes a geometrical information that is used to show on the layout the distribution of the equipotential lines produced by a perturbing source.

Another tool, like SILENCER! from [9], is dealing with the same issue, but for RF circuit design. Another modeling approach such as [24], proposes a global methodology that includes an early verification in the design flow as well as post-layout iterative optimization to deal with substrate noise, and helps designers to achieve a first silicon-success of their chip.

In the above studies, modeling of substrate parasitic in mixed-signal IC is mainly based on R-C network that is extracted from circuit layout. In these cases, they take only the majority carriers into account. The law governing the current carried by majority carriers are well known. In fact it corresponds to the classical electronics governed by the Ohm’s law. It is obvious that in low voltage technology, the substrate currents are relatively small and since the parasitic PN junctions are reversed biased, the effect of minority carriers can be ignored without prejudice. However, in high voltage technology, related effects due to minority carriers injection and propagation in substrate become significant.

3.2.2 Methodologies Using Substrate Parasitic BJT

In HV technology, the minority carriers are injected in substrate when a PN junction, instead of being reversed biased, becomes direct biased. Under such condition, electrons are injected into the substrate from some unwanted direct biasing of substrate diodes. This normally triggers the parasitic lateral NPN bipolar junction transistor (BJT), where the emitter is the injecting point and the collectors are the sensitive low voltage analog or digital devices.

In the conventional way, the simulation of parasitic coupling effects can be done by adding bipolar transistors or thyristors that account for minority carriers. These components are identified by experienced designer.

Negative voltages in power stages of junction-isolated Smart Power ICs turn on parasitic bipolar transistors and inject minority carriers into the substrate, which can affect the functionality of the chip. In order to indicate unacceptable substrate currents and to evaluate protection measures, these parasitic transistors have to be included into a post-layout simulation. In [29], a methodology has been developed for automatically generating Verilog-A models for these parasitics from layout data. These models account for an inhomogeneous current flow and high electron densities in the substrate.

The extraction of the bipolar transistor parameters is a difficult task due to the interactions in between various components. Due to the complexity of the system, restrictive assumptions are then made on the relative placement of injecting and collecting junctions. This is a strong limitation. An H-bridge for example has two drain junctions injecting charges in the substrate at the same time.

Nowadays, the state of the art in substrate parasitic modeling considers the minority carrier related effects by identifying the parasitic components such as the lateral parasitic bipolar transistor or the thyristor-like circuit.

However, parasitic identification is a difficult task due to the complexity of layout geometry. On one hand, the propagation of minority carriers are of 3D nature through long diffusion paths, and the multi-collectors bipolar transistor effect can not be modeled with existing components. On the other hand, the extraction of these parasitic related parameters is difficult due to the interactions between various components.

3.2.3 Methodology Using Finite Element Device Simulation

Nevertheless, the coupled noises due to carriers injection and propagation in the substrate can only be accurately modeled at that time through physical simulator, such as TCAD simulation[§]. Therefore, it is claimed in [34] that “simulations have to be carried out with a device simulator because a circuit simulator neglects minority carriers”.

In general, this physical based simulation refers to using computer simulations to develop and optimize semiconductor processing technology and devices. The tools solve fundamental, physical, partial differential equations, such as diffusion and transport equations for discretized geometries, representing the complete silicon wafer or layer system in a semiconductor device. That is why this deep physical approach gives TCAD simulation predictive accuracy.

[§]Synopsys Sentaurus Technology Computer-Aided-Design (TCAD) simulators

The TCAD consists of two branches: “process” simulation and “device simulation”. The former refers to developing and characterizing a new semiconductor process, which is complicated and not so widely used for standard IC design outside semiconductor foundries. On the other hand, the latter is more widely used, in both semiconductor industry and academic researches, for a new developed device or structure optimization.

In 2000, a methodology based on TCAD for substrate parasitic investigations was introduced. First, investigations on a Smart Power test chip (Figure 3.4a) were initially presented in [32]. The test chip consists of four high-voltage LDMOS transistors, in H-bridge configuration, as shown in figure 3.4b. In this work, authors constructed a simplified 3-D structure similar to the existing test chip using TCAD, but only two n-regions are constructed in the modeling structure: one for low-side transistor that is biased down to $-1V$ and the other one for high-side transistor that connects to power supply $+14V$ (Figure 3.5a). As we know from chapter 2, the negative biased n-region is responsible for injecting minority carriers into the substrate, hence shifting the substrate potential. A DC simulation of such structure was performed in this work, thus simulation costed 800MB RAM memory and lasted about 6 hours on a server with 3.6GHz processors in parallel.

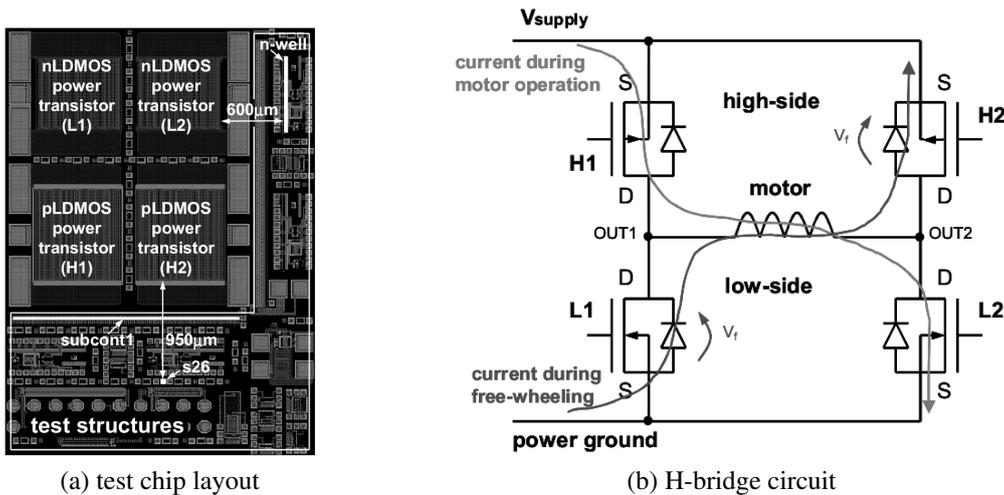


Figure 3.4: (a) Layout of test chip and (b) related H-bridge circuit in [33].

As a continuation of this work, transient simulations were performed as well. In [31], device simulations were performed first in 2-D structure. Investigations on different substrate contact placement strategies as well as the biased conditions were discussed. Result showed an acceptable error compared to measurement, hence accuracy was sufficient to make important decisions for failure analysis. Then, a TCAD guided methodology was later introduced in [33] based on the previous works. In addition, a full-chip 3-D device simulation were presented in this work. The structure in figure 3.5b consists of the four LDMOS transistors and one additional substrate contact that collects substrate current. Different biased conditions were considered in this work.

To summarize, this TCAD based methodology provides a possible solution at that time to

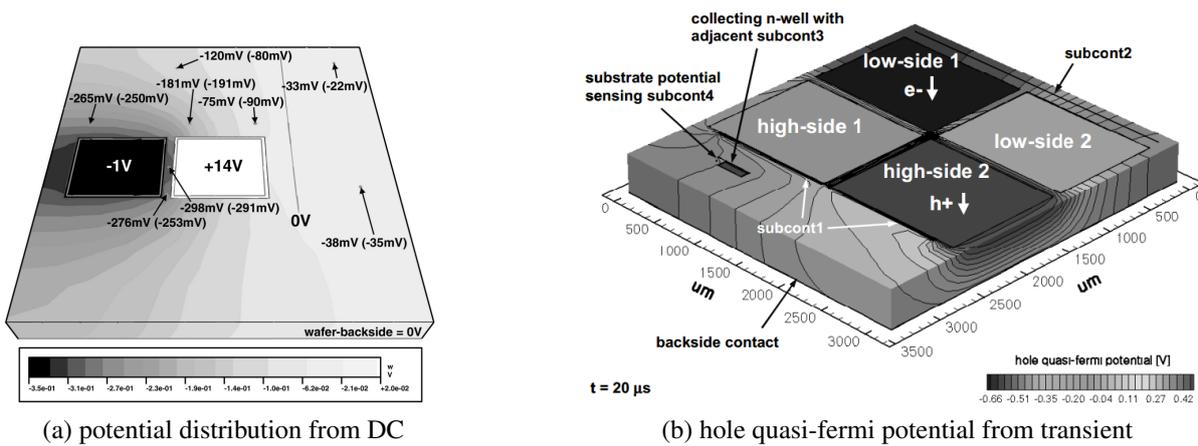


Figure 3.5: Potential distributed substrate from a DC device simulation in [32], Simulation structure and hole quasi-fermi potential at chip surface calculated by means of full-chip 3-D device simulation, as in [33].

model the substrate coupling effects related to carriers' propagation in the substrate of Smart Power IC. In this method, the important technology parameters were extracted by means of measured data from simple structures [32]. Results of this work showed a good agreement between device simulation and measurement. The drawback of this method is the demanding time, even for a simple structure with two n-regions. Hence, the presented method is indeed not suitable for a more complex chip while huge simulation time is needed. This kind of purely physical modeling methodology is limited to simple structures.

3.3 EPFL Modeling Methodology

In classical circuit-level simulation, compact models are connected by metal wires between each other. This implies that the excess of minority carriers at the terminals of these models equals zero, and the modeling of minority carriers' propagation between two devices was impossible in circuit-level simulation. This is however not the case in physics, the minority carriers in p-type substrate (electrons) can propagate through the entire substrate, even at a long distances due to their long carriers' lifetime.

In 2009, a new modeling approach was introduced in EPFL[¶] [17]. This approach relies on a new developed models accounting for minority carriers propagation. To do that, the authors extend the traditional diode models by introducing an additional terminal (Figure 3.6c). This additional terminal represents the status of minority carriers at the boundaries of lumped substrate PN junction. At this terminal, the minority carriers' concentration is represented by a voltage, on the other hand, its gradient is represented as a current.

[¶]École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, CH-1015, Switzerland.

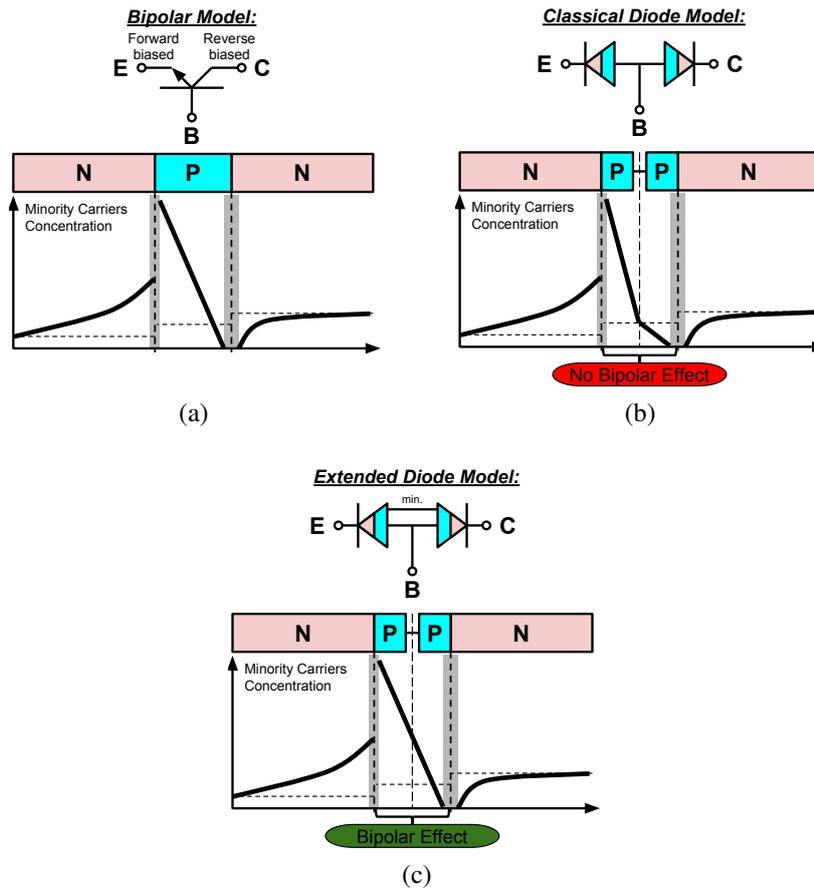


Figure 3.6: (a) Planar bipolar layout and minority carriers density, (b) equivalent bipolar modeled with classical diode, (c) equivalent bipolar modeled with the extended diode, as in [17].

By using this new diode model, they can maintain the continuity of minority carriers concentration between two models, and the propagation between devices becomes possible in this way. Therefore, two back-to-back diodes can eventually model the bipolar effect which is impossible by using the traditional compact diodes, as shown in figure 3.6. As a consequence, a netlist consisting of these model can be simulated by spice-like simulator.

The authors present several test cases consisting of N-wells over P-substrate, as in [17, 18, 13, 19]. An equivalent substrate schematic has been extracted manually, as discussed in [16]. In these works, modeling of parasitic lateral NPN bipolar junction transistor (BJT) with multi-collectors have been presented. Result shows a good agreement with TCAD device simulation, thus simulation time (0.6s) was much faster than TCAD (3016s), as reported in [19].

This modeling approach has been used in [16, 14], for the substrate noise investigations on an integrated H-bridge (Figure 3.7) in Smart Power technology. The equivalent schematic was manually extracted as depicted in figure 3.7c. It shows an impressive results by using such method which reduces significant the simulation time from 9 hours (TCAD) to 10 second (spice simulation), and

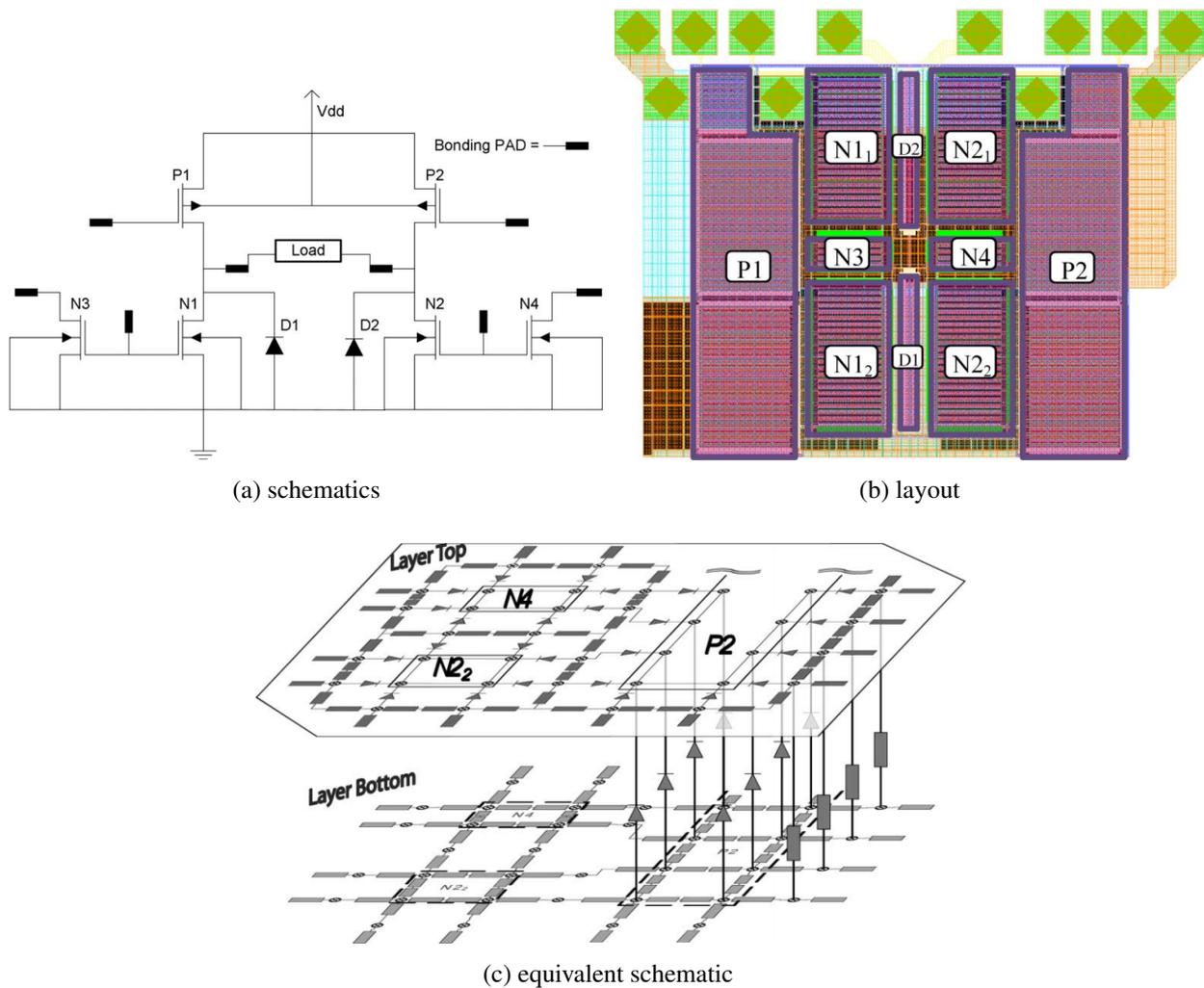


Figure 3.7: Integrated H-bridge and investigations for substrate noise, as in [16, 14].

memory use for computation from 2.2GB (TCAD) to 30MB (spice simulation).

However, the introduced models take only low current injection into account. The injected currents in simulation are much smaller than the realistic condition where substrate potential may reach up to several hundreds of millivolts. In these works, the simulations were only performed in DC, but substrate noise coupling in the Smart Power IC often occurs in transient when switching the power stage. On the other hand, the equivalent schematic were manually extracted by the authors. However, this will not be convenient for designer and even becomes impossible for a very large scale IC design, because the effects of substrate noise coupling, in particular the latch-up, are very sensitive and layout dependent.

3.4 Conclusion

In this chapter, we presented the state of the art efforts done to address the modeling of substrate parasitic. To begin with, we described the modeling of parasitic in the conventional design flow where metal interconnections were addressed. In the second part, modeling of parasitic in substrate considered.

The state of the art showed that, the modeling of such parasitic coupling is a hard task, because “most of the solutions are layout dependent and are thus difficult to optimize using available electrical simulator software” [19]. Several EDA tools dedicated to substrate parasitic modeling are based on R-C network which considers only the majority carriers. However, the physical based finite element simulations are the only way to simulate minority carriers’ related effects, whereas such device modeling methodology mainly focused on the transistor scale and not applicable for large scale IC design.

The EPFL modeling methodology was presented. This method relies on a substrate network consisting of parasitic models. These parasitic models have additional terminals to model the propagation of minority carriers between devices. Hence, the effect of minority carriers involved can be done in circuit-level simulation. However, this model can only simulate in circuit operating low current injection regime and substrate network has to be improved.

In the following chapters, we will introduce enhanced parasitic components developed in the framework of the AUTOMICS project and our approach to extract automatically the substrate parasitic model in 3-D and back annotation the circuit netlist.

Chapter 4

Methodology for Substrate Parasitic Extraction

Contents

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4.1 Introduction

In the following, a methodology of post-layout substrate parasitic extraction is introduced. This method takes circuit layout as input and generates a substrate parasitic equivalent netlist as the result.

Layout-based extraction is the translation of topological layout back into the electrical circuit it is intended to represent. Before talking about the layout extraction, we have to make a distinction between two definitions: *design devices*, which are the devices that are deliberately created by the designer; and the *parasitic devices*, which are not explicitly intended by the designer but are inherent in the layout.

In the conventional way, the layout extraction takes into account the extraction of design devices, the interconnection (e.g. metal layers and vias) and parasitic devices. The parasitic device extraction in the conventional way considers parasitic ohmic devices (resistance), parasitic cross-coupled devices (capacitance and inductance), parasitic diodes or vertical PNP bipolar junction

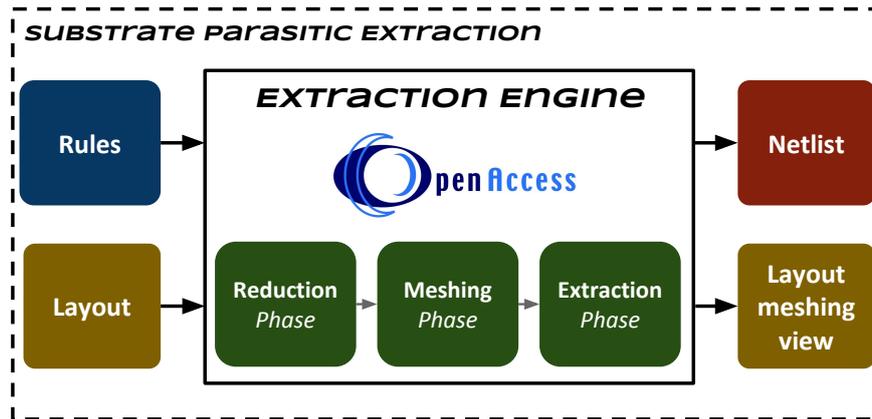


Figure 4.1: Overall flow of post-layout substrate parasitic extraction.

transistors (BJT). However, the substrate current propagation in substrate can not be modeled due to the lack of extraction of parasitic lateral NPN BJTs.

In our methodology, we extract the whole substrate as an equivalent netlist of enhanced parasitic components with extracted geometrical features from layout. Those enhanced parasitic components (i.e. EPFL diodes, resistor and homojunction) are compact spice models (written in Verilog-A) [36, 37, 35, 38, 39, 10], which have two additional terminals introducing minority carriers concentration and gradient (presented in Chapter 3). As for the RC network above substrate, they will be extracted use existing popular CAD/EDA tools, such as Quantus QRC of Cadence. In this chapter, we are only discussing about extraction of substrate parasitics, the extraction of RC network and the substrate parasitic back-annotation will be discussed in Chapter 6.

The flow in figure 4.1 illustrates the overall idea about our substrate parasitic extraction methodology. The extraction engine is operating in three phases, and encapsulated in a CAD framework. The “Reduction” phase reduces the complexity of layout hence select the region of interest for substrate parasitic extraction. The “Meshing” phase divides the remaining reduced layout into small sized cuboids. The “Extraction” phase extracts lumped parasitic components from those cuboids, and eventually generate a substrate parasitics equivalent netlist. The entire CAD framework is developed based on the “OpenAccess” programming library. We take circuit layout “OA” database and a specific set of rules as inputs. As for outputs, we generate a substrate parasitic equivalent netlist and a “OA” based cell view relating to layout meshing.

The remaining of this chapter is organized as follows: In section 4.2, the extraction flow associated with a CAD framework is introduced. The “OpenAccess” programming library that relates to our work is discussed. In section 4.3, our methodology of layout extraction is introduced. The methodology employs a 3-D extraction engine and has been encapsulated in a dedicated IC-CAD tool. In section 4.4, as a case study, a simple diode structure is extracted and simulated. Finally, we conclude the chapter in section 4.5.

4.2 Computer-Aided-Design Framework

We have just given a short introduction about our methodology. The extraction engine is driving in three phases, and encapsulated in a Computer-Aided-Design framework, as illustrated in figure 4.2. The framework development is based on the *OpenAccess* programming library, which provides an open source API (Application Programming Interface) to an IC design database. The most important feature of *OpenAccess* is the interoperability across different design platforms and EDA tools. The major CAD/EDA tool vendors such as *Cadence*, *Synopsys*, *Mentor Graphics* support the *OpenAccess* API. In the meantime, technology providers like *STMicroelectronics*, *ams AG*, etc., are also distributing process design kits (PDK) as “OA” database.

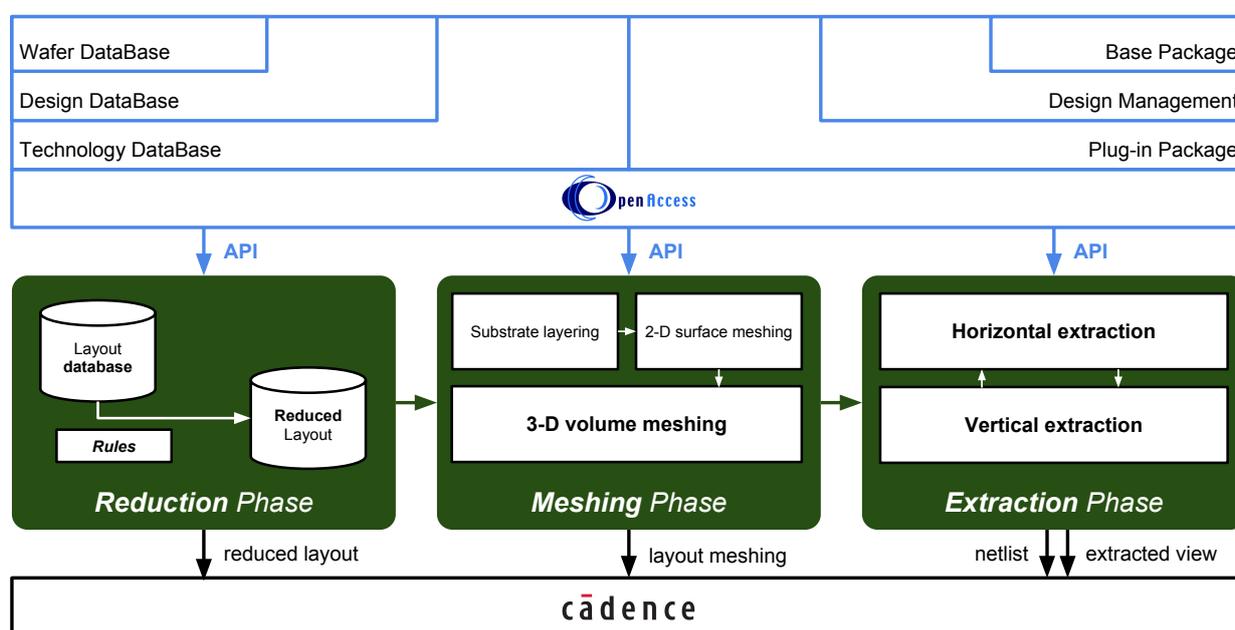


Figure 4.2: Computer-Aided-Design framework of substrate parasitic extraction.

By using “OA” public APIs, we are able to access the design database, and at the same time, we are capable to add our representations produced by substrate parasitic extraction to the design database. Therefore, layout entry, reduced layout, layout meshing, netlist and extracted view are all represented as “OA” database, as illustrated in figure 4.2. At the end of each phase, corresponding representation is generated and saved as a Cell View. The implementation of these Cell Views and the netlist back-annotation can be done in most of the major IC design environments, as long as they support “OA” based API. In our case, they are integrated in *Cadence* design environment.

The “OA” API is organized as a set of packages. Each package provides a part of the functionality. They are a total of six packages, as depicted in figure 4.2. Three database packages and three additional general purpose packages. “Design”, “Technology” and “Wafer” are the three database packages. “Design Management”, “Base” and “Plug-in” are the three additional packages.

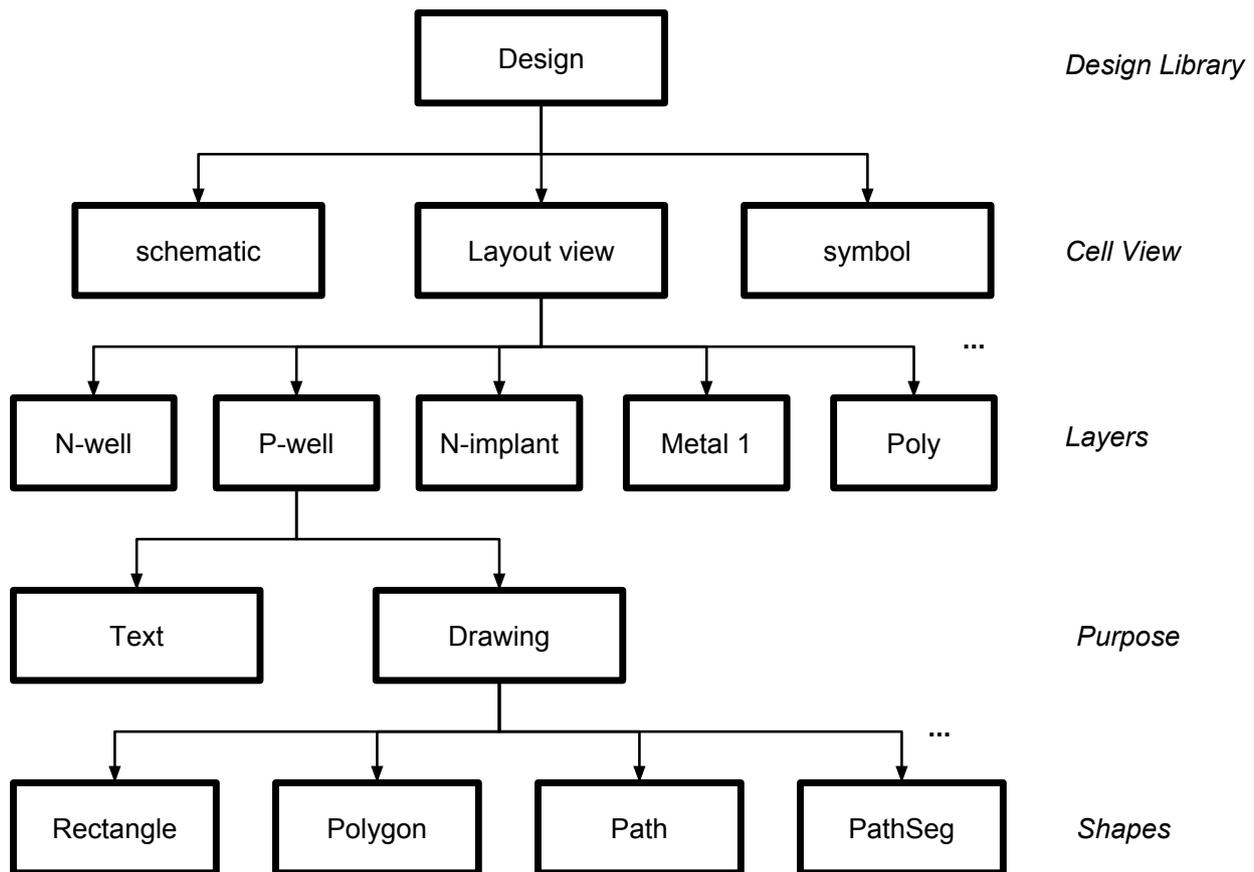


Figure 4.3: Contents of design object in *OpenAccess* database.

The API for “Design Management” consists of functions necessary to keep the design libraries, cells and views organized. The “Base” one provides common functions like error handling, namespaces, strings, extensions, etc. The “Plug-in” one contains a set of specific API interface classes to enable dynamic loading of third party software to integrate with “OA” model. The “Wafer” database holds the manufacturing information like semiconductor mask layers, frames, etc. This is particularly helpful in yield analysis. Since our work focuses on layout extraction, discussion of this database is out of the scope. In the following, we mainly focus on the “design” and “technology” databases.

The “Technology” database manages the technology data like mask layer definitions, routing and foundry constraints, etc. The technology data may not be limited to a particular design but across all the designs made with a given technology. The “*oaTech*” class is the main class associated with “Technology” database, and “OA” organizes each technology database as a “Technology Library”.

The “Design” database manages everything related to a design such as its hierarchy, schematic, layout, floor planning, etc. The “*oaDesign*” class is the main class associated with this database. The design’s cell views such as schematic, symbol, layout are stored as *oaDesign* in “OA”. *Ope-*

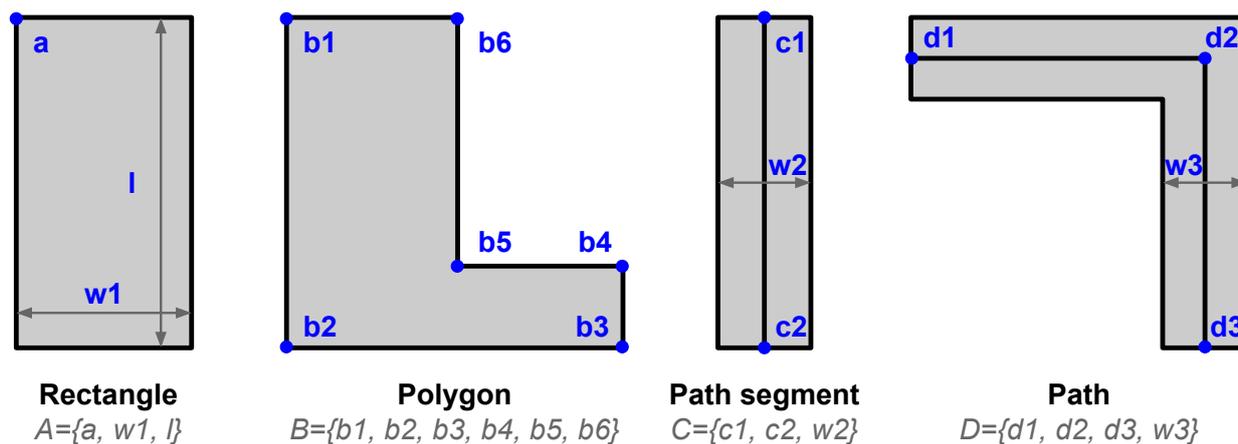


Figure 4.4: Frequently used shapes in IC layout design and their definitions.

nAccess organizes each design as a “Design Library” (different from “Technology Library”), Cell and Cell View, as illustrated in figure 4.3.

Since we are discussing about layout extraction, the “Layout View” of the “Cell” is of main interest. The “Layout View” basically contains information of different layers (e.g. wells, implants, metals and polys). As illustrated in figure 4.3, one layer, or mask layer, has different purposes (i.e. text, drawing), and different shapes. The “OA” API supports different shapes associated with mask layers such as rectangle, polygon, path, etc., as shown in figure 4.4. We can understand that each kind of shape has its own attributes and definition, for example, a rectangle will have a bounding box that forms the rectangle shape, and it is defined by the upper left corner and its length and width; on the other hand, a polygon will have an array of ordered points in a bounding box. The substrate parasitics in the layout involve different layers like wells and implants. Hence, they are represented by geometric shapes, having different set of attributes and doping characteristics. To extract the geometry of relevant layers, the coordinates of all the required shapes associated with each layer need to be extracted from the layout “OA” database.

In the “OA” database, a “Layer Purpose Header” (LPPHeader) is automatically created whenever a particular layer and purpose number is created. If a shape with same layer and purpose number is drawn then it shares the same LPPHeader. All these shapes are created using one of the subclass of *oaShape* base class in “OA”. A function called “*getShapes*” returns a collection of shapes associated to a given LPP Header. Up to now, we have explained how to use “*OpenAccess*” provided public API to extract the geometry from layout “OA” database. In the next section, the three phases of substrate parasitic extraction are presented.

4.3 Layout-Based Extraction Methodology

In the following, our approach of post-layout substrate parasitic extraction in three phases will be introduced. Figure 4.5 depicts the representations of Cell View created at the end of each phase (Figure 4.2), thus the main concept of our extraction methodology can be simply illustrated: figure 4.5a is showing the layout cross section of reduced layout; figure 4.5b indicates the mesh lines describe the 3-D structure; figure 4.5c shows the extracted parasitic components that we consider in our methodology. Details will be explained in the following paragraphs.

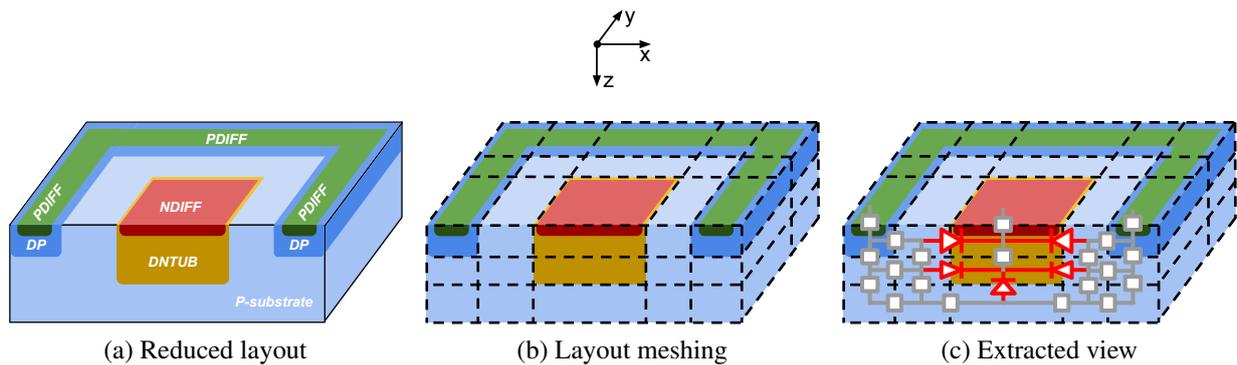


Figure 4.5: Modeling approach of substrate parasitic extraction in case of a simple diode in $0.35\mu\text{m}$ HV-CMOS technology of *ams AG*.

4.3.1 Reduction Phase

The region of interest that we consider in our methodology is underneath transistor diffusion areas. In the one hand, we consider wells and implants. On the other hand, all the others, e.g. METAL layers, CONTACT and VIA, are ignored in our methodology. Hence, specific rules are used to define the masks involved in a target technology process, e.g. H35, or H18 process nodes of *ams AG* HV-CMOS technology. The rules are formed in Extensible Markup Language (XML), thus written in XML file. The file describes two kinds of information: 1). The list of masks of interest in our methodology, these masks are semiconductor layers having material types of: N-well, P-well, N-implant, P-implant, diffusion or poly-silicon; 2). the thickness of substrate region and the junction depths of relevant masks. It is important to note that “*OA*” API doesn’t provide any function or class to store the height or thickness of a layer, yet these kind of additional informations should be considered as well.

An example of rules for *ams AG* $0.35\mu\text{m}$ HV-CMOS technology process node is shown in listing 4.1. Rule line 2 defines thickness of substrate region to be extracted; rule line 3 declares the mask name of diffusion; rule line 4 declares the mask name of poly-silicon; rules lines 5 and 6 declare the mask name and junction depths of p-type and n-type implants respectively; rule line 7 declares the mask name and junction depth of N-well; eventually, rule at line 8 declares the mask

name and junction depth of P-well.

```

1 <LAYERS>
2   <SUBSTRATE thickness="dPS" />
3   <LAYER name="DIFF" />
4   <LAYER name="POLY1" />
5   <LAYER name="PPLUS" thickness="dPD" />
6   <LAYER name="NPLUS" thickness="dND" />
7   <LAYER name="DNTUB" thickness="dDN" />
8   <LAYER name="DPTUB" thickness="dDP" />
9 </LAYERS>

```

Listing 4.1: Rules for ams AG 0.35 μm HV-CMOS technology process node.

Therefore, in our approach, we start by selecting a set of layers, and deriving a reduced version of the original layout (Figure 4.5a) that is used for further extraction. The technique of reduction is performed by checking if the layer purpose pair (LPP) number is of interest. For example, we are looking for the layers that are defined in rule file and with purpose “drawing”. Thus, the remaining data that do not contribute to substrate parasitic extraction should be ignored.

4.3.2 Meshing Phase

This phase consists in dividing the substrate into small volumes, that will be further represented by a lumped electrical element. From a geometrical point of view, the substrate may be divided into cuboids that have a different size: length, width and height, but, sharing the same surface with the adjacent ones. Besides geometry, the element in meshing is parameterized by material type. The available material types are: N-well, P-well, N-implant, P-implant and P-substrate. In our methodology, the meshing in 3-D is constructed in three steps: 1) the vertical meshing along z-axis, which we call “*substrate layering*”; 2) the horizontal meshing along x-y plane, which we called “*2-D surface meshing*”; and 3) the combination of both for the final meshing in 3-D.

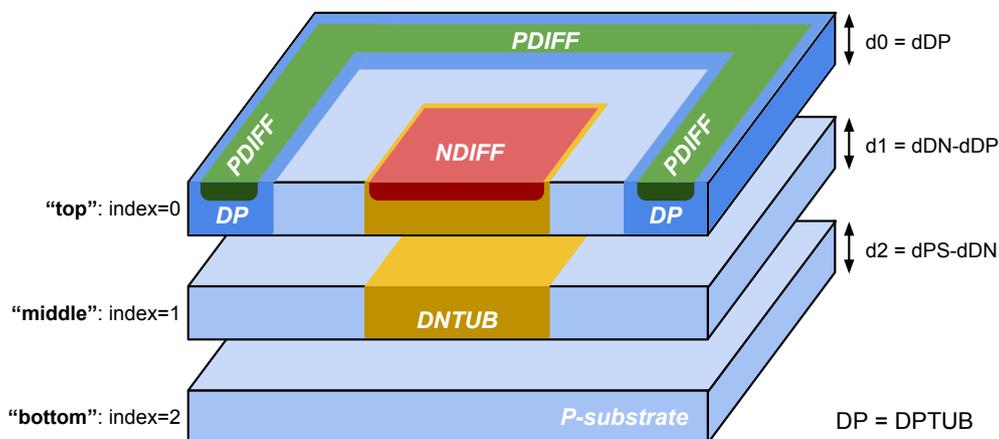


Figure 4.6: Process of substrate layering, in HV-CMOS technology process.

Table 4.1: Layer Relation Table.

| Index | Thickness (μm) | Wells and/or Implants |
|-------|-----------------------------|-----------------------------------|
| 0 | d_{DP} | <i>DNTUB, DPTUB, NDIFF, PDIFF</i> |
| 1 | $d_{DN} - d_{DP}$ | <i>DNTUB</i> |
| 2 | $d_{PS} - d_{DN}$ | <i>N/A</i> |

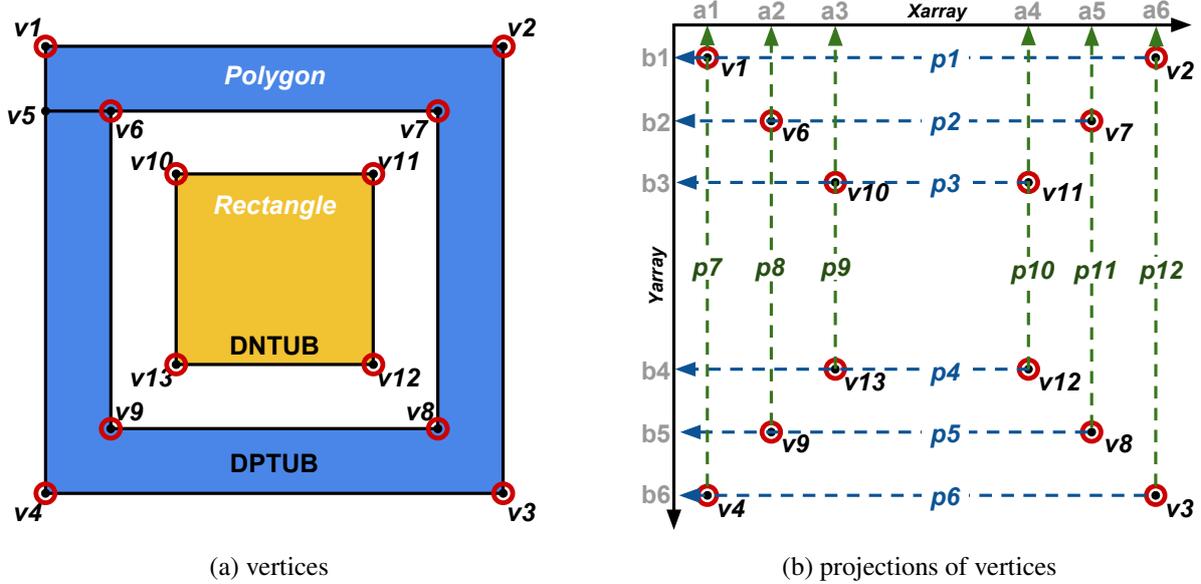


Figure 4.7: (a) Representation of geometrical shapes (rectangle and polygon) by points, the points marked in red are vertices; (b) projection of vertices on x- and y-axis.

These three steps will be explained in detail in the following sections:

4.3.2.1 Substrate Layering

For vertical meshing along z-axis, the substrate will be divided into several stacked layers, or slices (Figure 4.6). The total number of slices is derived from the wells, and their thicknesses are derived from the junction depths. For example, if we consider in our case the deep N-well (DNTUB) and the deep P-well (DPTUB) over P-substrate, the substrate will be divided into 3 slices. The “cut” through highly to lightly doped junction (DPTUB and P-substrate) results in two slices “top” and “middle”, and the “cut” through PN junction (DNTUB to P-substrate) results in two slices “middle” and “bottom”. Eventually 3 slices are derived from vertical meshing: the slice on “top” includes DNTUB and DPTUB wells; the slice in the “middle” includes only DNTUB; and then the slice at “bottom” is P-substrate region only. In addition, N-implants (NDIFF) and P-implants (PDIFF) serve as the contacts on the surface of the “top” slice. Table 4.1 records the relevant informations for meshing for each slice (row with index), such as thickness (second column) and involved wells or implants (third column).

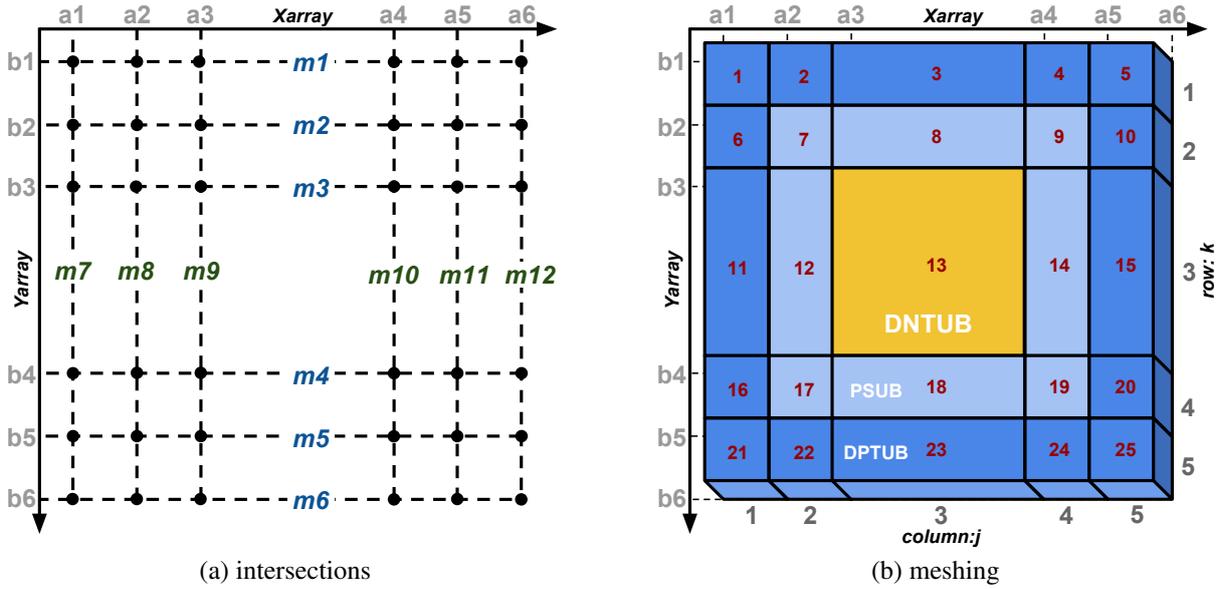


Figure 4.8: Representation of geometrical shapes by vertices.

4.3.2.2 2-D Surface Meshing

Once the substrate is layered, a meshing working on a 2-D surface (x-y axis) is developed at each slice. In general, it begins from the top (index=0) and ends up with the bottom (index=last). In our methodology, the 2-D meshing is based on points instead of shapes. The rectangle or polygon shapes are commonly used in IC layout design. For instance, the rectangle (yellow) in figure 4.7 represents a deep N-well over the P-substrate, and the polygon (blue) represents a surrounding deep P-well ring. These shapes can be described as a set of ordered points. For example, the polygon can be described by ordered points in clockwise:

$$S_{poly} = \{v_1, v_2, v_3, v_4, v_5, v_6, v_9, v_8, v_7, v_6, v_5\}$$

in the same way, the rectangle can be described as 4 ordered points:

$$S_{rect} = \{v_{10}, v_{11}, v_{12}, v_{13}\}$$

Among these points, we start to collect the vertices. The vertices are the corner points of a given shape where the direction of the edge changes. They are marked as red points in figure 4.7. Therefore, the intersection point v_5 is then removed from initial list, since it is on the edge of polygon. The final list of vertices describing the 2-D surface of figure 4.7 is saved as:

$$S = \{v_1, v_2, v_3, v_4, v_6, v_7, v_8, v_9, v_{10}, v_{11}, v_{12}, v_{13}\}$$

The projections of these vertices on the x-axis is called “Xarray”, and the ones on the y-axis

is called “*Yarray*”. In our case, see figure 4.7b, they can be expressed as:

$$Xarray = \{a_1, a_2, a_3, \dots, a_6\}$$

$$Yarray = \{b_1, b_2, b_3, \dots, b_6\}$$

where a are coordinates in “*Xarray*” and arranged by value from left to right; and b are coordinates in “*Yarray*” and arranged by value from top to bottom. These two arrays build the coordinate system of the resulting meshing. Lines at coordinates b_1, b_2, \dots, b_6 result in horizontal mesh lines m_1, m_2, \dots, m_6 ; in the same way, lines at coordinates a_1, a_2, \dots, a_6 result in mesh lines m_7, m_8, \dots, m_{12} , illustrated in figure 4.8a. The intersections of two perpendicular mesh lines are mesh points, marked as black points in figure, called “*intersections*”. As one intersection describes a location on surface, then two can indicate an edge of one element in meshing, and the four rectangle-like points form an element. For each element, its size on 2-D is defined by the diagonal opposed “*intersections*”, i.e. the lower left (LL) and the upper right (UR) points. And its height equals to the slice thickness (in table 4.1). To summarize, the geometry of one element in meshing can be expressed as:

$$Length = UR.x - LL.x$$

$$Width = UR.y - LL.y$$

$$Height = d_{slice}$$

Besides geometry, each element is parameterized by its index (red) and material type, as illustrated in figure 4.8b. The index number refers to the node of final netlist, called index of connection G_{id} , it is defined as:

$$G_{id} = m(k - 1) + j$$

where m is total number of columns, k and j are row and column of target element.

4.3.2.3 3-D Volume Meshing

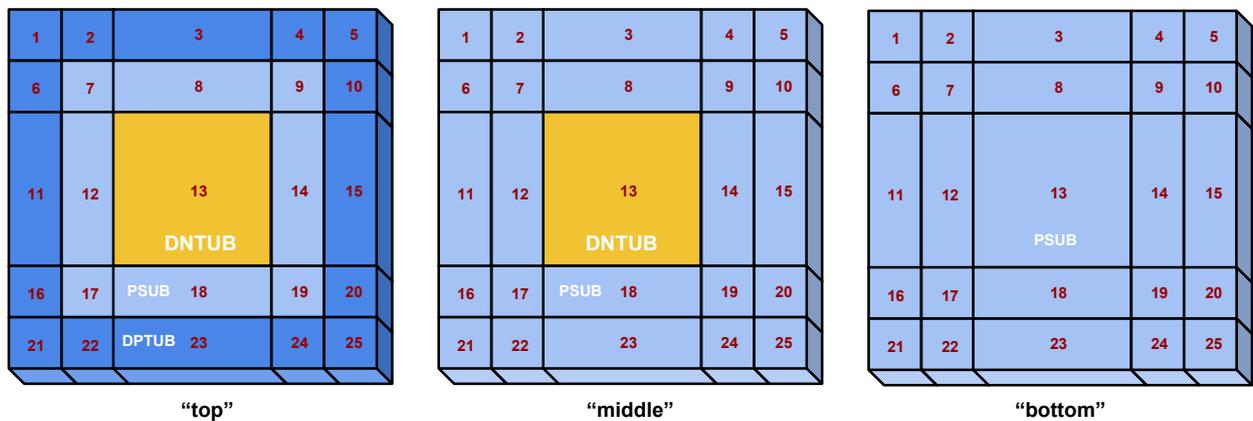


Figure 4.9: Process of substrate meshing in 3-D for each slice: “*top*”, “*middle*” and “*bottom*”.

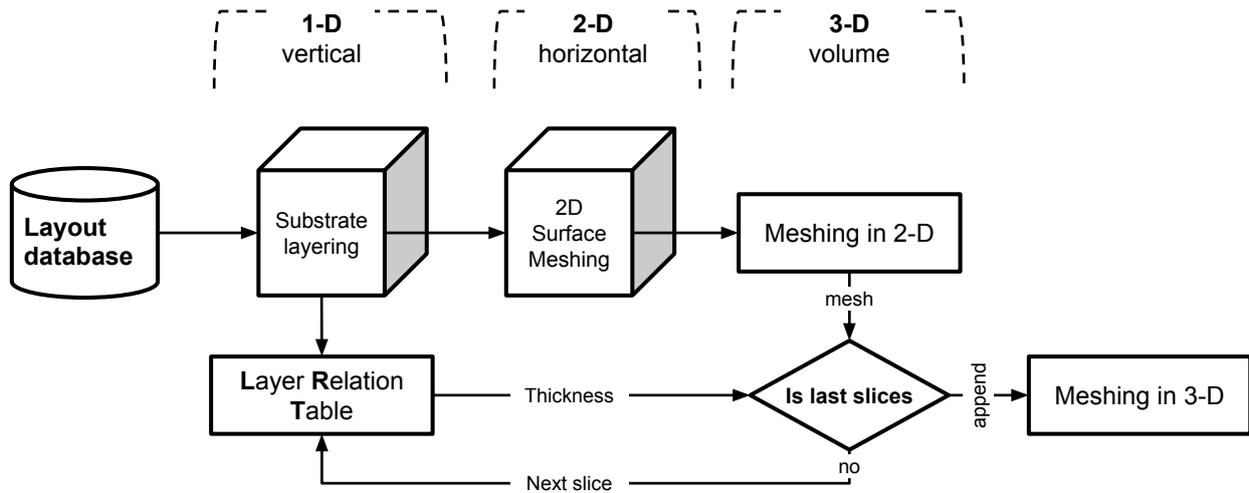


Figure 4.10: Meshing Algorithm in 3-D

In this section, an algorithm to mesh the substrate in 3-D is presented. This includes meshing along z-axis (substrate layering) and along x-y plane (2-D surface meshing) at each slice in the substrate. The flow chart in figure 4.10 shows an algorithm to implement a meshing technique in 3-D. The algorithm can be divided into three parts. The first two parts were discussed in the previous sections, and the third part is the combination of the two. The resulting meshes at each slice are the same in terms of geometry but differ in doping properties. For example, mesh of “middle” in figure 4.9 has the same dimensions as the one of “bottom”, hence element “13” is N-type material in “middle” but P-type material in “bottom”. To visualize the meshing at different slices, we redraw the cell view with meshing and saved them in the design database. “OA” provides the possibility to create a new physical layer with a specified purpose, e.g. drawing. In our case, we use a user defined layer with a purpose “drawing” to draw the meshing inside cell view.

4.3.3 Extraction Phase

In the following, we study the extraction of parasitic components from the meshed substrate as an equivalent netlist. This netlist consists of extracted parasitic components together with geometrical patterns. The extraction happens where two adjacent elements intersect. Assuming two adjacent elements: A and B intersect, with dimensions shown in figure 4.11a, a parasitic component will be extracted between their centers. Depending on the material types of both elements, the extracted parasitic component can be either:

- an enhanced “**diode**”, if they have different material types; or
- an enhanced “**resistor**”, if they have the same material type with same doping concentration; or
- a “**homojunction**”, if they have the same material type but different doping concentrations.

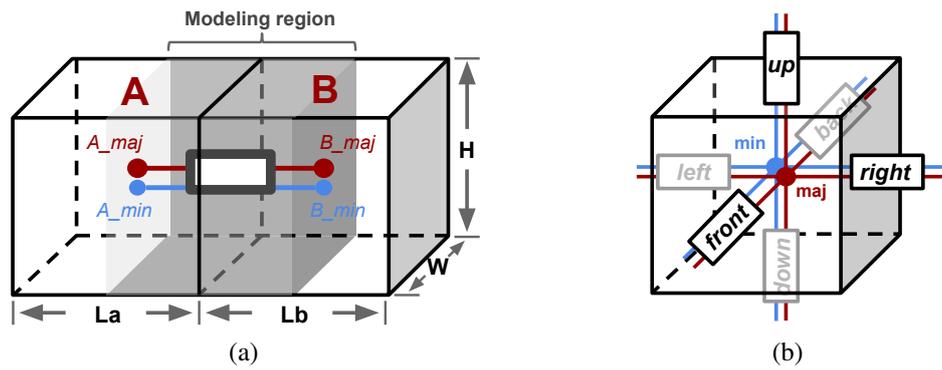


Figure 4.11: Basis of parasitic components extraction: (a) extract a component from two adjacent cuboids, the extracted component can be either an enhanced diode or an enhanced resistor or a homojunction; (b) connection in 3-D of one cuboid in the mesh.

Table 4.2: List of parameters to extract for enhanced parasitic components.

| <i>Parasitic model</i> | <i>Doping profile</i> | Geometrical parameters | |
|------------------------|-----------------------|--|--|
| | | Length [μm] | Area [μm^2] |
| Diode | n | $L_a/2$ | $w \times h$ |
| | p | $L_b/2$ | |
| Resistor | n or p | $L_a/2 + L_b/2$ | |
| Homo-junction | n or p | $L_a/2$ | |
| | n+ or p+ | $L_b/2$ | |

At the center of one element, we define two separate nodes: one terminal for majority carriers (“*maj*”) and the other for minority’s (“*min*”). Hence, terminals of surrounding components to this node are separated between majority’s (red) and minority’s (blue), see figure 4.11b. Depending on the position in the mesh, a cubic element may have different numbers of adjacent elements. Among all the possibilities, they are mainly 4 cases: 1) the one in the middle of meshing has six adjacent elements, typically in six directions (front, back, left, right, up and down); 2) the one on the boundary side of the mesh has five adjacent elements; 3) the one at the edge of the mesh has four adjacent elements; and 4) the one at corner of the mesh has only three adjacent elements.

For each parasitic component, the additional parameters that should be extracted from geometry are the length, the area, etc (in table 4.2). Besides geometry, doping characteristics are extracted as well. For instance, resistor extracted from deep N-well differs from the one extracted from deep P-well in terms of material types. Resistor extracted from deep P-well differs from the same material type resistor extracted from P-substrate in terms of levels of doping. Therefore, resulting resistors to extract are:

Table 4.3: Possible combinations and the corresponding parasitic components.

| | PSUB | DNTUB | DPTUB | NDIFF | PDIFF |
|-------|-------------|-------------|-------------|-------|-------|
| PDIFF | H_{PD-PS} | D_{PD-DN} | H_{PD-DP} | N/A | N/A |
| NDIFF | D_{ND-PS} | H_{ND-DN} | D_{ND-DP} | N/A | |
| DPTUB | H_{DP-PS} | D_{DP-DN} | R_{DP} | | |
| DNTUB | D_{DN-PS} | R_{DN} | | | |
| PSUB | R_{PS} | | | | |

- R_{DP} : inside deep P-well (DPTUB);
- R_{DN} : inside deep N-well (DNTUB);
- R_{PS} : inside P-substrate.

The same idea stands for enhanced parasitic model of diode and homojunction. Table 4.3 lists all the possible combinations of parasitic component. Component with $D_$ stands for enhanced diode, component with $R_$ stands for enhanced resistor, and component with $H_$ stands for homojunctions.

Based on the above idea, extraction of parasitic components is performed over the entire meshing. In general, extraction of netlist in 3-D takes two steps: 1) extraction at each slice, the resulting netlist is called “*horizontal network*”, and 2) extraction between two slices, the resulting netlist is called “*vertical network*”:

- *Horizontal* networks are generated at each slice, for instance, networks at “*top*”, “*middle*” and “*bottom*” of figure 4.12. They consist of netlist of different parasitic models though having the same geometries. The extracted components are interconnected to the node, named by G_{id} ;
- *Vertical* networks are generated between two slices, for instance, networks at “*top to middle*” and “*middle to bottom*” of figure 4.12. The network connects the netlist at above slice with below slice according to the G_{id} nodes, e.g. node of the “*top*” slice is connected to node of the “*middle*” slice. In addition, network at “*contacts*” is extracted on the surface of “*top*” slice. The vertical homojunction are extracted where N-implants (red) or P-implants (green) are located, as depicted in figure 4.12a. Therefore, these homojunctions connect out to the contacts of original design netlist: i.e. “*Pcontact*” and “*Ncontact*” via terminals of majority carriers, while terminals of minority carriers are grounded as boundary condition.

The describing networks are described as an equivalent netlist, and saved as “*netlist.scs*”.

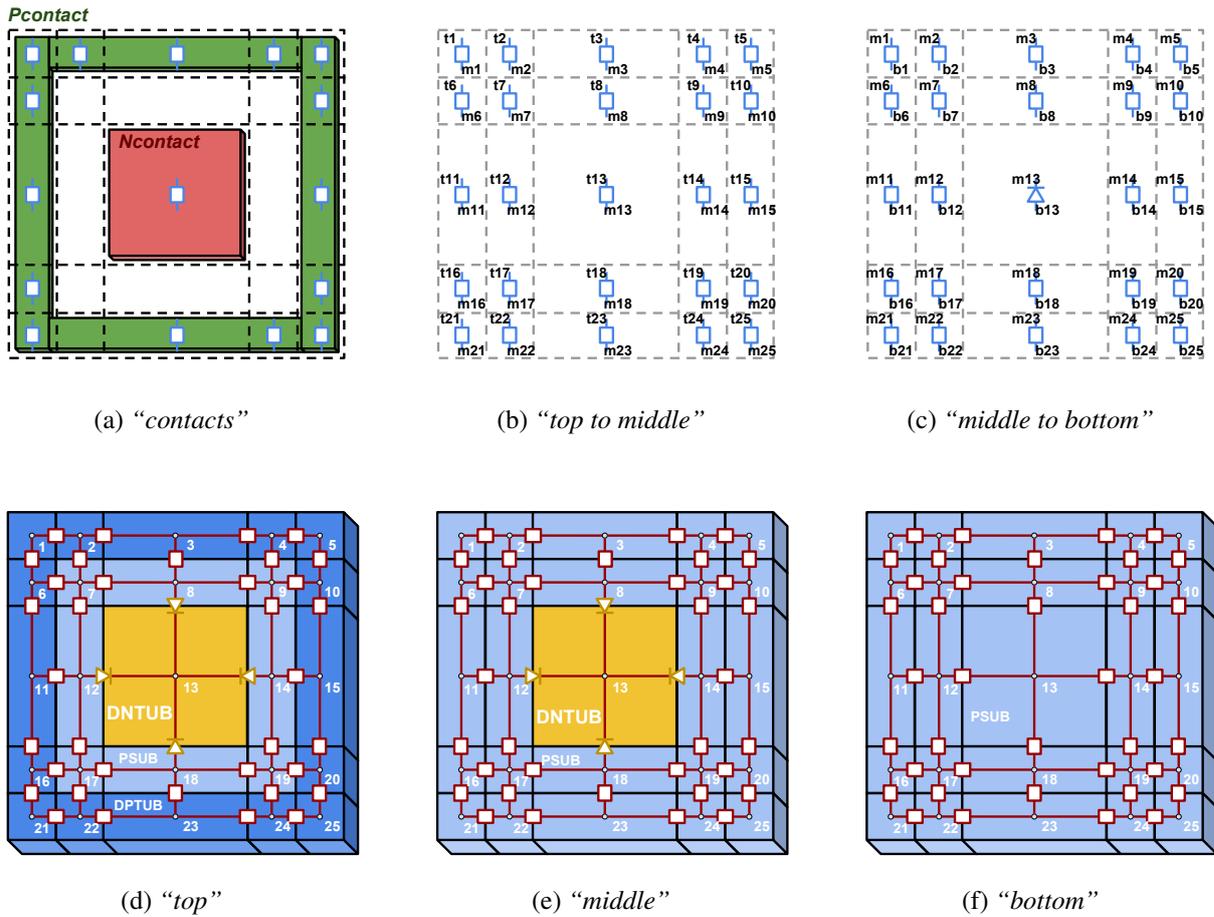


Figure 4.12: Substrate parasitic network in 3-D.

4.4 Simulation and Evaluation

In the conventional way, device simulation based on TCAD and complex models are obtained to simulate coupling caused by substrate parasitic BJTs. However, device structure needs to be simplified in order to construct its 3-D model in TCAD environment. Although this approach is commonly used for process modeling of a newly developed structure, it is not applicable for a whole circuit design. Moreover it is still impossible to attach this substrate model with circuit schematic.

On the other hand, our modeling methodology provides a layout-to-netlist extraction approach. Substrate model is described as a netlist that is extracted directly from IC layout. It consists of interconnected parasitic components with geometrical patterns from layout. These parasitic components can maintains carriers propagation in substrate for both majority and minority. In this way, the effects of substrate coupling between components can be simulated in fast circuit simulation.

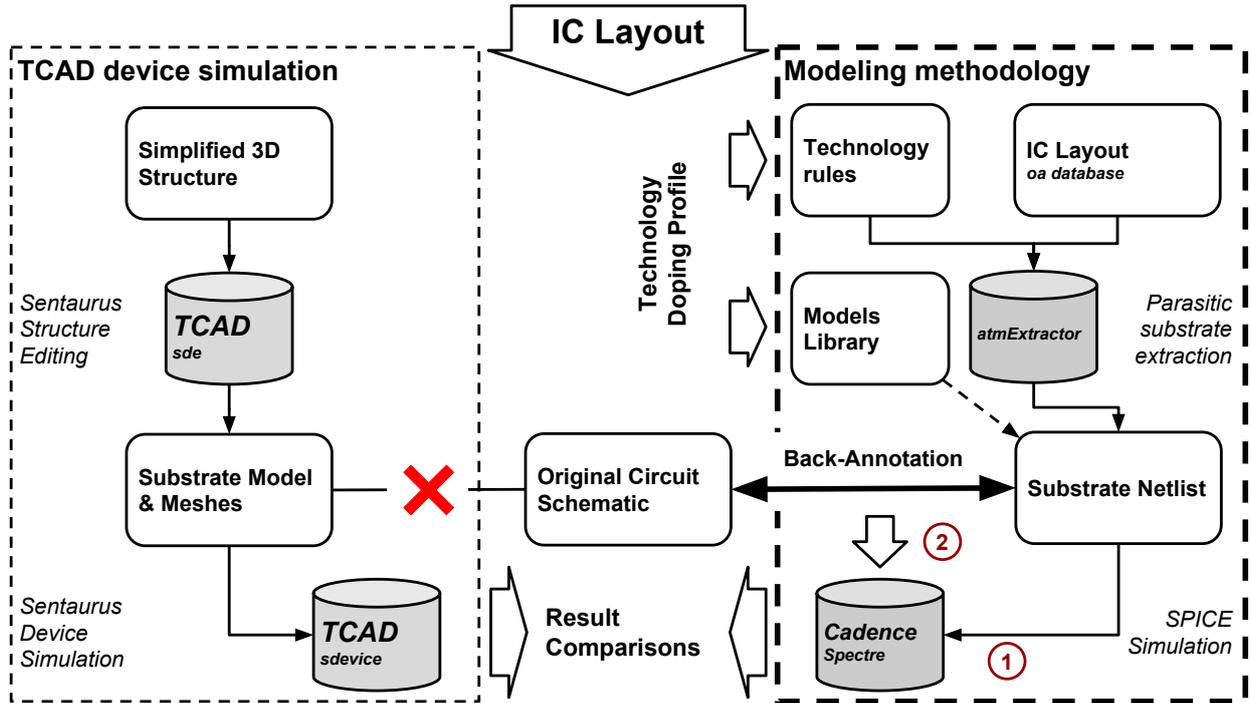


Figure 4.13: Concept of evaluating the proposed modeling methodology to physical based TCAD. Left side: conventional approach based on TCAD device simulation for substrate parasitic BJTs. Right side: proposed approach of layout-to-netlist parasitic substrate extraction. Substrate model can be back-annotated into the original circuit and used by standard spice-like simulator.

As a first case study, the simple diode structure shown in figure 4.5a has been investigated in both approaches. The objective of this investigation is to see the basic diode behaviors, as well as the temperature effects in both forward and reversed biased condition. Eventually, the results of circuit simulation are compared to the ones obtained from TCAD simulations.

Table 4.4: DC simulation setup with temperature conditions.

| Simulation setup | Emitter [V] | | | Collector [V] | Temperature [°C] |
|----------------------------|-------------|-----|------|---------------|------------------|
| | Start | End | Step | | |
| DC Forward/Reverse biasing | -1.0 | 8.0 | 50m | 0 | -25, 27, 75, 125 |

The 3-D structure with same dimensions are implemented in Sentaurus TCAD tools, i.e. *sde* (Sentaurus Device Editor) in figure 4.15a. The doping density profiles are assumed constant and equal to $4.5 \cdot 10^{15} \text{cm}^{-3}$ for the p-substrate and to $2 \cdot 10^{17} \text{cm}^{-3}$ for the n-well. The p+ and n+ doped diffusion regions were assumed to be Gaussian with peak doping density of $5.0 \cdot 10^{19} \text{cm}^{-3}$. DC analysis are performed, i.e. *sdevice* (Sentaurus Device Simulator) in figure 4.15c, by sweeping the emitter (i.e. V_N) from -0.1V to 8.0V with step of 50mV while the collector (i.e. V_P) is grounded.

Table 4.4 reports the simulation setups for a DC analysis. The voltage source is connected to the emitter (N-well of diode), and the collector (P-substrate) is grounded. Since temperature

behaviors are very important in Smart Power technology, we have also performed the simulations with same setup at different temperature conditions: the temperatures considered in our case are -25°C , 27°C , 75°C and 125°C .

Curves in figure 4.14 show results of DC analysis as function of junction voltage: from -1V to 8V at x-axis that covers the forward and reverse biased regimes. Results from TCAD (points) are compared to the ones from our work (lines). It can be seen that both, the forward behavior (current increases exponentially as applied voltage increases) between $[-1\text{V}, 0\text{V}]$ and reversed behavior (a small constant negative current regardless of applied voltage) between $[0\text{V}, 8\text{V}]$ are clearly observed as expected. Results show a good agreement between TCAD and our work.

In the same figure, curves in colors show the results at different temperature conditions. The temperature behaviors are clearly observed: in reverse biased condition $[0\text{V}, 8\text{V}]$, the reverse saturation current increases as the temperature rises; on the other hand, the forward diode current increases as temperature rises, thus diode forward-voltage drops (more free electrons in higher temperature condition, less voltage is required).

Results from both TCAD and our work confirm the correct diode behaviors, in forward and reverse biased condition. When comparing the two approaches, as reported in table 4.5, the simulation time cost using our approach was 242 times less than the one from TCAD simulation.

Table 4.5: Simulations output parameters of TCAD and spice.

| | Meshes elements | DC points | Simulation Time [s] |
|---|-----------------|-----------|---------------------|
| TCAD | 341788 | 21 | 1204 |
| This work | 178 | 21 | 4.96 |
| Simulation were performed with Intel Core i5-3470S Processor (2.9GHz) | | | |

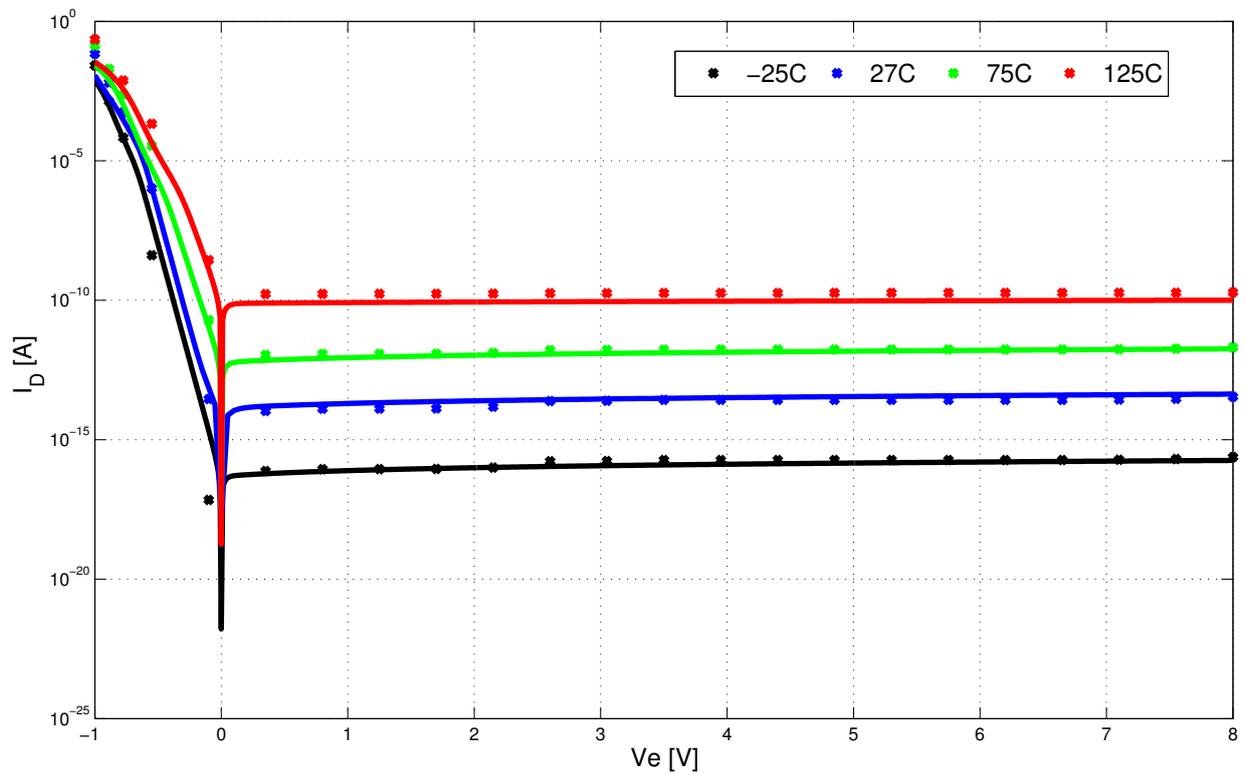


Figure 4.14: IV characteristics and temperature behaviors in both forward and reverse biased conditions of single diode structure. Points for TCAD and solid lines for our work.

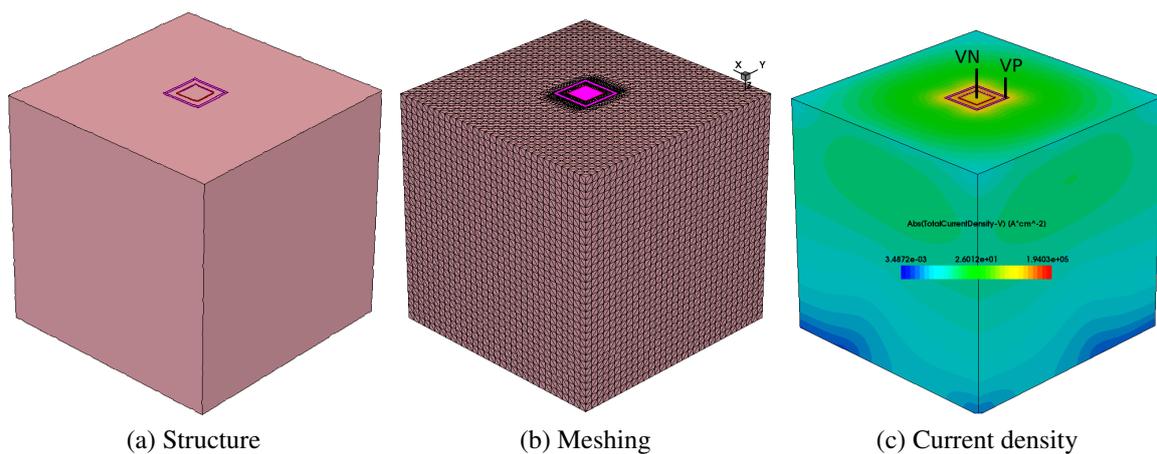


Figure 4.15: 3-D structures in Sentaurus TCAD tools: (a) 3-D structure of stand alone diode in p-substrate; (b) meshed structure; and (c) total current density after simulations at $V_N = -1V$ and $V_P = 0V$ at room temperature.

4.5 Conclusion

In this chapter, a methodology of substrate parasitic extraction is introduced. Beginning with layout entry, this method performs a substrate meshing in 3-D that models the entire substrate with small sized cuboids. These cuboids contain the geometrical properties as well as the technological ones. Thus, we are able to model the substrate by lumped parasitic components extracted from the meshing in 3-D. This layout-based extraction methodology has been developed based on *OpenAccess* database, and encapsulated in a dedicated CAD framework.

A simple structure including a stand-alone diode over P-substrate is considered as the first case under study. Two approaches for substrate parasitic modeling including our work are compared in this case. On the one hand, the conventional time-cost physical based TCAD simulations were performed. The proposed layout-extraction methodology was performed on the other hand. DC Simulations were performed to investigate the basic diode behaviors, hence temperature effects were also considered. Results show a good agreement between our work and TCAD simulation, though our work has a gain factor in time of 242.

Chapter 5

Mesh Refinement Strategy for Substrate Parasitic Extraction

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5.1 Introduction

In the previous chapter, a methodology for substrate parasitic extraction was introduced. This method relies on a strategic meshing in layout, where the parasitic components are extracted. These parasitic components are enhanced EPFL models (i.e. diodes, resistors and homojunctions) that are parameterized with geometric and technological data. Additional terminals at each of the lumped models are reserved for minority carriers. The parasitic effects due to carriers (electrons and holes) injection and propagation in the substrate can be eventually predicted in circuit-level simulation.

Generally speaking, a complete model for substrate parasitics relies on three features: 1) compact and fitted parasitic models, i.e. EPFL models; 2) parameter calibration for a target technology; and 3) meshing strategy dedicated to layout extraction. The first one requires the modeling of three basic lumped elements, and they are extracted between two cubic elements to model two basic lumped elements. However, simulator could suffer from convergence issues when addressing a massive number of extracted components, and it slows down the overall simulation time. The second one relies on parameters fitting hence contributes to improve the accuracy. Finally, the third one converts topological layout back into the electrical netlist using adaptive rectilinear meshing algorithm, and it consequently plays the role to balance the time-efficiency and accuracy.

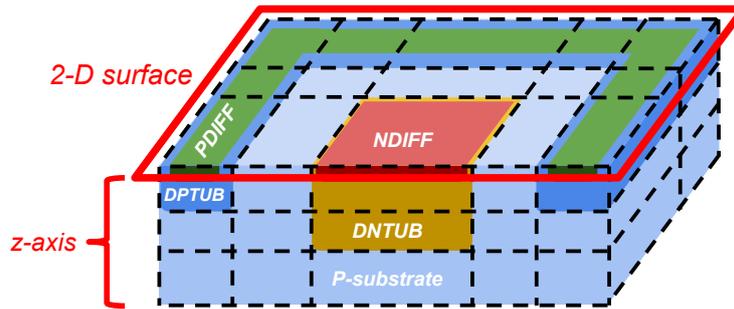


Figure 5.1: Representation of layout meshing in 3-D.

Since analog integrated circuit layout is a combination of art and science [21], the modeling of substrate parasitics becomes even harder. Yet, substrate parasitics modeling should give the designer an insight of substrate behaviors associated with parasitics location, and it should not slow down too much the overall system simulation. This step is followed by deeper investigations. The combination of overall fast simulation and accurate local extraction is more interesting in terms of time saving. Therefore, the trade off between time-efficiency and accuracy is considered as the key to this kind of failure analysis.

In this chapter, we mainly focus on the optimization strategies dedicated to meshing that has been introduced in the previous chapter. Figure 5.1 redraws the same example of one simple diode. Strategies of mesh refinement are considered in two ways: 1) the optimization on 2-D surface meshing; and 2) the optimization in z -axis, as shown in figure 5.1. Then, we will discuss a meshing strategy considering subregions that takes into account many devices. Extraction of a simple structure including two N-wells over P-substrate is demonstrated, where parasitic lateral NPN BJT is then investigated.

The remaining of this chapter is organized as follows: In section 5.2, a strategy for device meshing is discussed. In section 5.3, strategy of region meshing is explained. Finally, we conclude the chapter in section 5.4

5.2 Mesh Refinement Strategy in Device

In this section, strategies of meshing optimization in 3-D are explained. As our example under study, we take the same structure that has been discussed in the previous chapter: a diode over P-substrate. In this structure, the N-well is covered by the $n+$ diffusion which connects out to terminal “Ncontact”, and the $p+$ diffusion covers the P-well which surrounds the N-well region and connects out to terminal “Pcontact”. We explain in the following our strategy of mesh refinement in two parts: 1) the optimization on 2-D surface; 2) the optimization in z – axis direction.

5.2.1 Mesh Refinement on 2-D Surface

In the following, we recall the meshing strategy that we have introduced in the previous chapter. To recall the idea, we use the same figures shown before, Figure 5.2. Moreover, red circles in figures represent the vertices. These vertices are formerly collected at the beginning of the substrate model extraction (Figure 4.1 in Chapter 4). They indicate the points of shapes where a direction of the edge changes, e.g. 8 for polygon (dark blue) and 4 for rectangle (yellow).

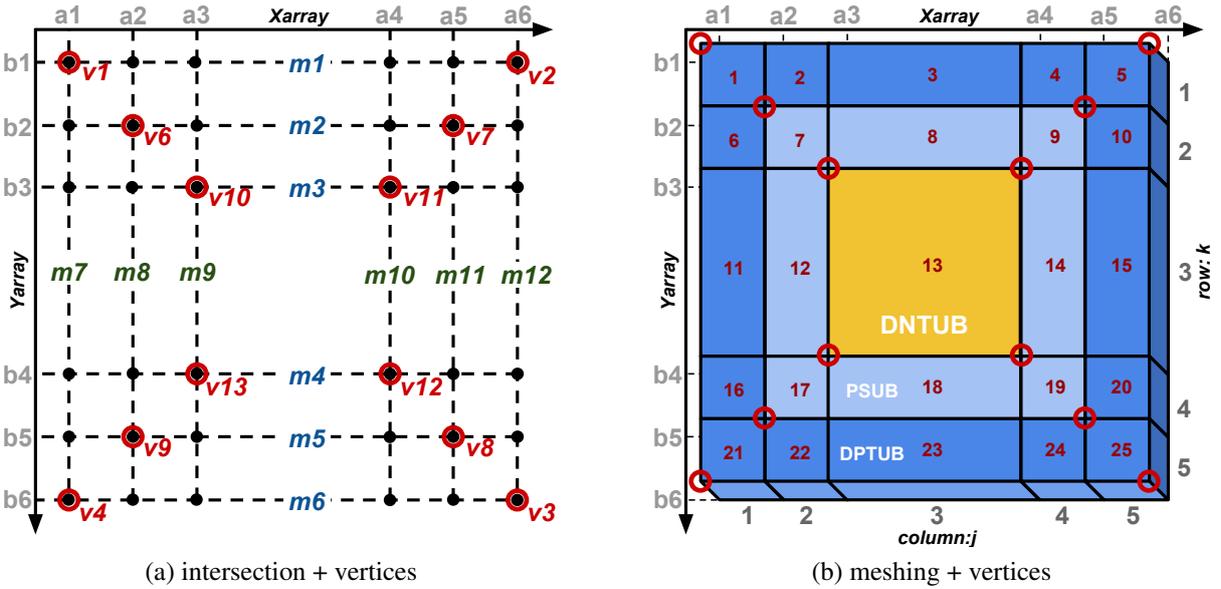


Figure 5.2: Representation of meshing by “intersection”, and vertices (red).

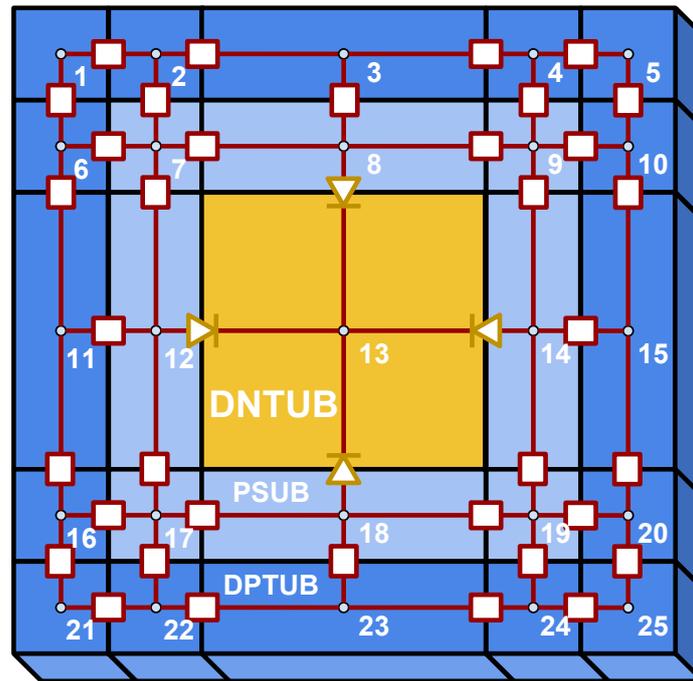
The initial mesh that has been introduced in the previous chapter is shown in figure 5.2b. The entire mesh consists of 25 elements, corresponding to 5 columns and 5 rows. Each element is a cuboid characterized by diagonal opposed “intersections” (black points in figure 5.2a). These “intersections” are found based on the “coordinate system”: i.e.

$$Xarray = \{a1, a2, a3, a4, a5, a6\}$$

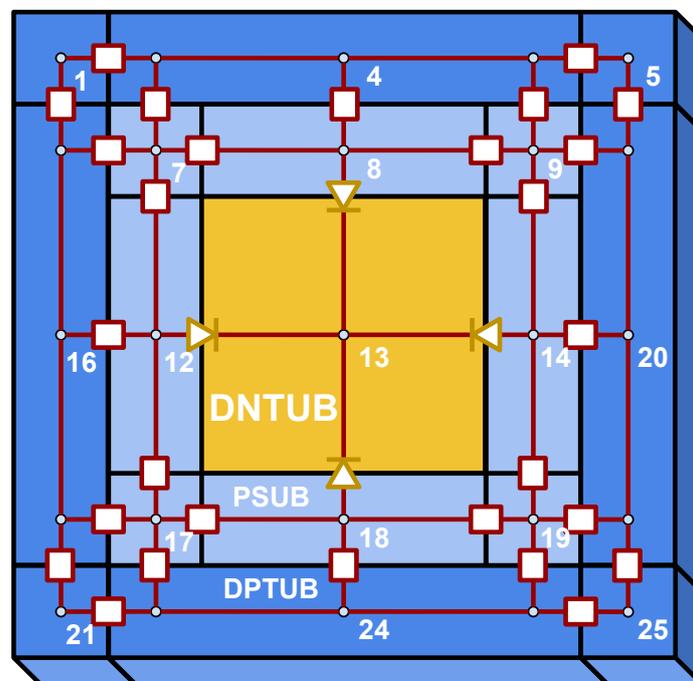
$$Yarray = \{b1, b2, b3, b4, b5, b6\}$$

Hence, the “coordinate system” is the projection of vertices on both x- and y-axis. This meshing strategy, called “S1”, introduces an initial mesh where the elements are entirely aligned to each other, as illustrated in figure 5.3a. Further extraction of parasitic component is based the principle that only one parasitic component will be extracted per side. Following this rule, one element can have no more than one adjacent element at each side. Eventually, 40 parasitic components are extracted between 25 nodes, consisting of 4 enhanced diodes and 36 enhanced resistors.

Then, the remaining question is how can we optimize this meshing? If we go back to figure 5.2b where we are showing the initial mesh together with vertices, the vertices (red circle) always



(a) initial meshing: M1



(b) enhanced meshing: M2

Figure 5.3: (a) initial mesh, and (b) enhanced mesh.

indicate the turning points of edges. Furthermore, two aligned vertices form an edge segment. The edges combined with the vertices provide the required information to merge adjacent elements. Hence, we introduce a technique for mesh refinement, called “merging”. This technique is applied to reduce the total number of meshed elements. The idea is to combine many small sized elements to a larger element. For those small sized elements that can be merged, they have to meet the following three conditions:

1. same material characteristics;
2. the resulting merged element form a rectangular shape;
3. the edge of resulting shape does NOT overlap any of the vertices.

For example:

- the group of initial elements $\{1, 2, 6, 7\}$ in figure 5.3a can form a rectangular shape, but the elements do not have the same material characteristics. This group of elements can not be merged.
- the group $\{1, 2, 3, 4, 5\}$ in figure 5.3a, consists of initial elements having the same material characteristics, and they form a rectangular shape. However, they can not be merged because the bottom edge of the union overlaps the vertices v_6 and v_7 .
- the group $\{2, 3, 4\}$ in figure 5.3a can be merged since they satisfy the three conditions above. The merged element regroupes the three initial elements: its size is the union of the three, and its index is the number of the last merged element, i.e. the merged element is indexed as “4” in the optimized mesh, as shown in figure 5.3b.

Figure 5.3b depicts the final mesh after optimization, where 12 elements have been merged to 4. We have eventually achieved an element reduction up to 32% (i.e. 8 out of 25 on one slice) by using the strategy of mesh refinement.

Further extraction of parasitic component is based on the new topology M2. In the previous cases M1, we have mentioned that there should be no more than one parasitic component extracted at one side of each element. Since the topology has changed, this rule has to be completed

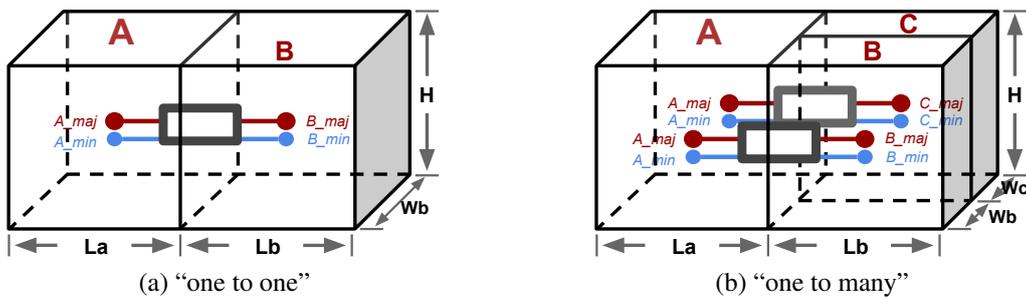


Figure 5.4: Component extraction in two different topologies.

Table 5.1: Report of extracted parasitic components.

| Slice | initial meshing: M1 | | enhanced meshing: M2 | |
|----------|---------------------|----------|----------------------|----------|
| | horizontal | vertical | horizontal | vertical |
| “top” | 40 | 16 | 32 | 9 |
| “middle” | 40 | 25 | 32 | 17 |
| “bottom” | 40 | 25 | 32 | 17 |
| In total | 186 | | 139 | |

accordingly.

It can be noticed from figure 5.3b that, the resized element in mesh could possibly have more than one adjacent elements per side, e.g. element 4 intersects elements 7, 8, 9 at bottom side. Figure 5.4 illustrates the idea for parasitic component extraction, from the topologies of “one to one” and of “one to many”. In case of “one to one”, the idea remains the same as for M1 topology. In case of “one to many”, the parasitic components are extracted between each two of them. Hence the two extracted components share the same nodes at the larger element: i.e. one for majority and the other for minority. For each component, the area equals to intersection and the length equals to distance between two centers.

In figure 5.3, extracted netlist is shown on the mesh of “top” slice. Comparing to the initial one (M1), the enhanced one (M2) has saved 8 parasitic components over 40 in total. The component reduction is achieved up to 20% (i.e. 8 out of 40 on one slice). Applying the optimized strategy over the entire mesh, this number increases up to 25% (i.e. 47 out of 186), see reports on extraction in Table 5.1.

5.2.2 Mesh Refinement in z-axis Direction

In the following, strategy of mesh refinement in z – axis direction is introduced. The idea of this optimization technique is to consider each substrate slice as an individual 2-D region for meshing, which means that the topology of meshing at each slice could be different from one another.

For our example, the “top” slice includes DNTUB and DPTUB wells, the “middle” slice includes DNTUB well, and the “bottom” slice is P-substrate only. The parasitic component used to model the substrate depends on the wells involved. Therefore, for meshing the substrate, we consider the involved wells at each slice rather than the entire substrate, as illustrated in figure 5.5. In addition, the construction of mesh at each slice relates to the above slice. For example, “bottom” slice is P-substrate without any wells or implants. If we assume this region as only one single cuboid, it is therefore impossible to model the horizontal propagation of substrate current

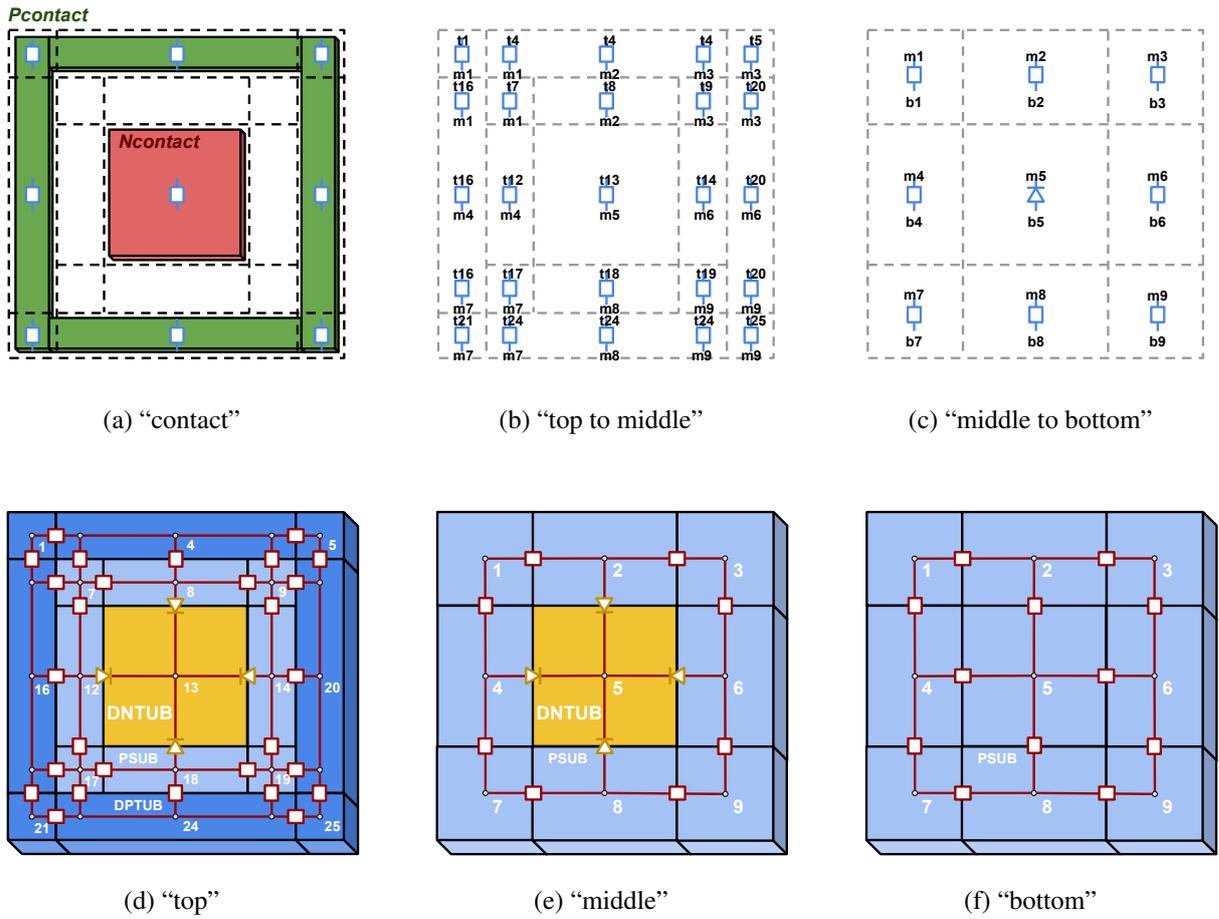


Figure 5.5: Meshing and parasitic component extraction at each slice.

inside this region only. On the contrary, if we divide this region into small-sized cuboids as the “top” slice, the number of components to extract from this region will increase. However, the increased number of parasitic components will not help to improve simulation accuracy, because the P-substrate under wells is more like an ohmic region. Therefore, the meshing of P-substrate region remains the same as the “middle”, as shown in figure 5.5f.

Now consider extraction in z-axis. In between 2 adjacent 2D-slices, parasitic components in the z-axis should be extracted, considering that the two slices can have different topologies from one another. The idea remains the same like in the horizontal intersect case. For example, element 1 from “middle” slice intersects four elements from “top” slice: 1, 4, 16 and 7. At each intersection, we extract a vertical parasitic component, as shown in figure 5.5b. The four components share the same nodes at the “middle” slice: one for majority carriers and one for minority carriers, and have separate nodes at each of the destination nodes (in the “top” slice).

5.3 Mesh Refinement Strategy for Region

The modeling of substrate currents caused by the possible activation of parasitic lateral NPN BJT is a hard task. This parasitic bipolar is a multi-collector NPN (N-well to P-substrate to many N-wells). The emitter is the injecting N-well of substrate currents (usually power device), the collectors are the surrounding N-wells and the base is the whole substrate. Modeling of such parasitic lateral NPN is therefore impossible using compact BJT models, since the victims of substrate noise coupling can be anywhere in the chip and the geometrical patterns of layout substrate can never be correctly extracted. The lack of modeling for this parasitic bipolar is still the missing part in the conventional design flow, thus studies of this parasitic models are of our interest and are the main topic in this section.

In the previous section, we have introduced a substrate meshing strategy in 3-D. This strategy is well-developed for a device, which means the strategy considers the whole structure as one device regardless of its size or shape, or the number of fingers. Assuming a circuit consisting of 4 HV devices and 8 LV devices, the HV devices are in H-bridge configuration to control the motor while the LV devices are the controlling circuit of the H-bridge. The 4 HV devices may have the same size that is much larger than the sizes of 8 LV devices in total. To prevent and protect the design against parasitics, we usually put the LV circuits away from HV devices, or add guard rings around the suspicious aggressor (HV devices) or the noise sensitive part (LV circuit). If we mesh the layout of this design, the results are possibly similar to the one in figure 5.6. It is obvious that the meshing from LV part is much thinner than the meshing from HV part, this thinner mesh lines introduce over developed meshing in HV part, as marked in figure 5.6.

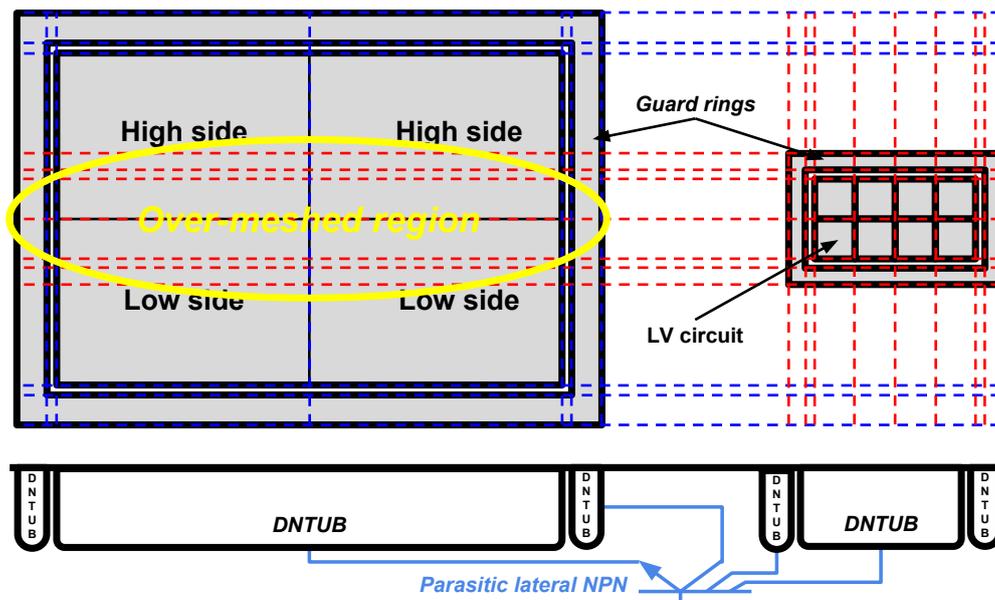


Figure 5.6: Issue for meshing strategy when considering several different sized devices. Blue dash lines represent the meshing from HV devices, and the ones in red are from LV devices.

The resulting mesh results in a massive number of components to extract, which is not helping to improve the accuracy while slowing down the overall time of simulation. To overcome this issue, we have developed a methodology that will be explained in the following. To illustrate the idea, we take a simple structure including two N-wells over P-substrate as the second example under study.

5.3.1 Descriptions of Design Structure

Figure 5.7 depicts the structure of our example under study. The simple structure includes two N-wells with spacing d over P-substrate. In this structure, a parasitic lateral NPN BJT is inherently created after layout. If we suppose the N-well at left side is the emitter of substrate currents and the other one is the collector, then the whole substrate is the base of NPN BJT, as shown in figure 5.7.

To investigate the effect of substrate currents depending on distance, we consider the test structure with same dimensions but different spacing d : i.e. $d = 20\mu\text{m}$ in case 1 and $d = 60\mu\text{m}$ in case 2. The layout is designed in ams AG $0.35\mu\text{m}$ HV-CMOS technology process node.

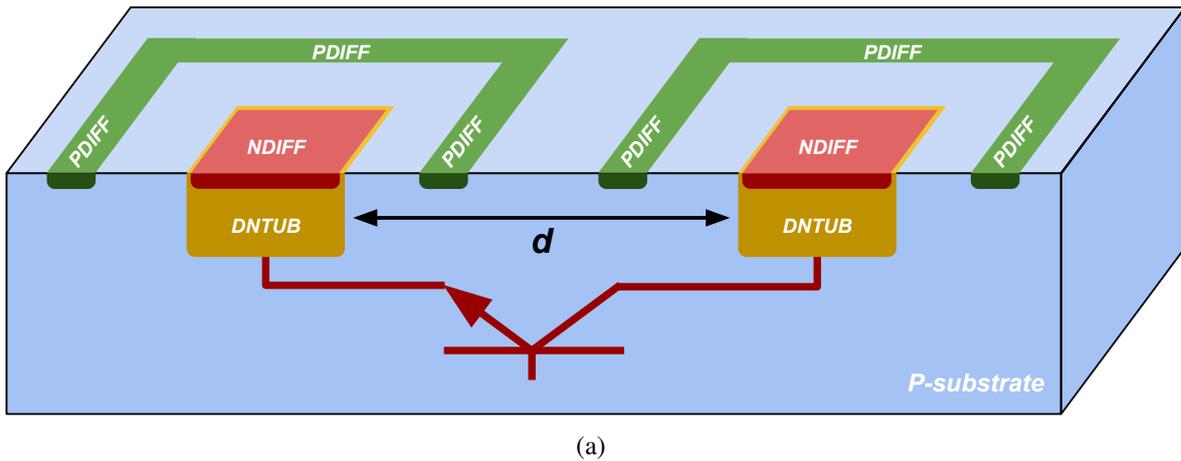


Figure 5.7: Structure in 3-D of two distant N-wells, in HV-CMOS technology.

The common p-type substrate is a cube with dimensions $L = 200\mu\text{m}$ by $W = 200\mu\text{m}$ by $H = 200\mu\text{m}$. The two n-type wells share the same dimensions $L = 20\mu\text{m}$ by $W = 20\mu\text{m}$ and their depths are equal to thickness of N-well. Each N-well is covered by a n-type diffusion region, and connected out to terminals named $N1$ (left) and $N2$ (right) respectively. They are both surrounded by a p-type diffusion regions, and connected out to P-substrate contacts named $Psub$.

5.3.2 Applying Meshing Strategy for Regions

To take into account different devices while meshing, the extraction engine has to understand the layout floor planning. This step usually takes place at the beginning of the substrate model extraction when collecting shapes from layout “OA” database.

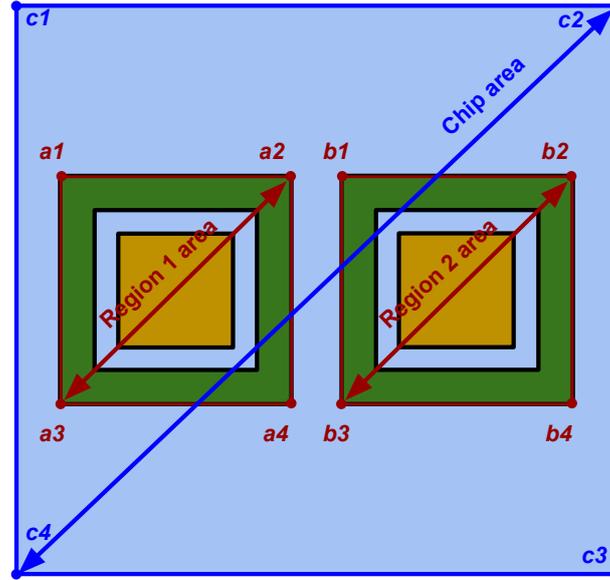


Figure 5.8: Layout pattern matching for substrate parasitic extraction.

In our methodology, we have developed a pattern matching technique to identify device regions. Following a pattern matching approach, this technique is searching for the bounding boxes from a set of given shapes. Hence, the outermost bounding boxes (red in figure 5.8) indicate regions of interest, and they can be described as:

$$\begin{aligned} region_1 &\leftarrow \{a1, a2, a3, a4\} \\ region_2 &\leftarrow \{b1, b2, b3, b4\} \end{aligned}$$

where a_x and b_x are vertices of red bounding boxes.

In the same way, the chip region can be described as:

$$chip \leftarrow \{c1, c2, c3, c4\}$$

where c_x are vertices of the blue bounding box.

Once we have defined the chip and regions in our methodology, the meshing of layout can be developed “inside” and “outside” regions separately, such as:

- The meshing “inside” regions takes place inside each region. For example, the meshing of device at left hand side considers only the shapes included in $region_1$, and the same idea holds for the device at right hand side. This results in two meshes separated as shown in figure 5.9a.
- The meshing “outside” regions takes place inside chip area while ignoring the contents inside regions. Hence, the construction of meshing takes the bounding boxes as input. The technique of meshing is similar to the one that we formerly introduced. This results in an optimized mesh “outside” regions as shown in figure 5.9b.

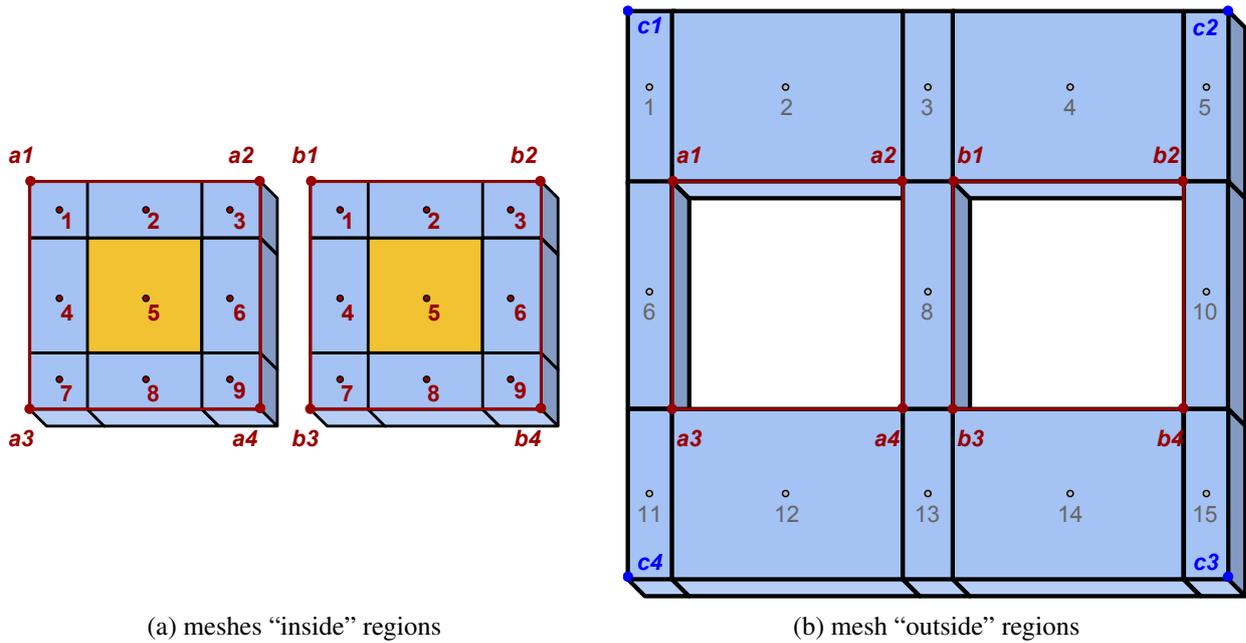
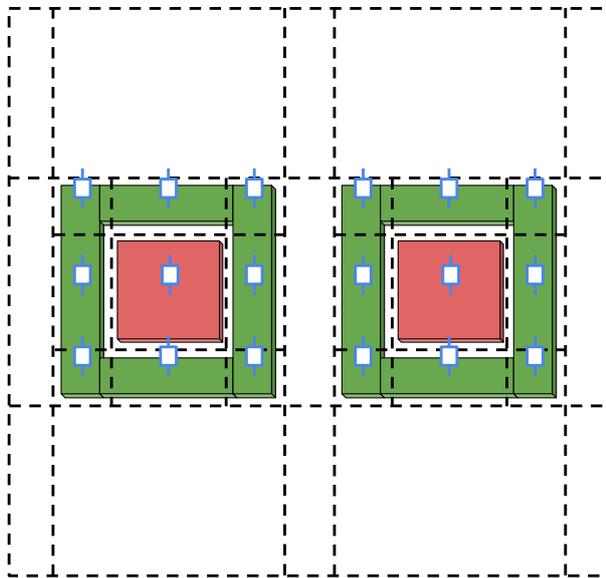


Figure 5.9: (a) meshes of devices, and (b) mesh of region outside devices, showing N-well and P-substrate in the “top” slice.

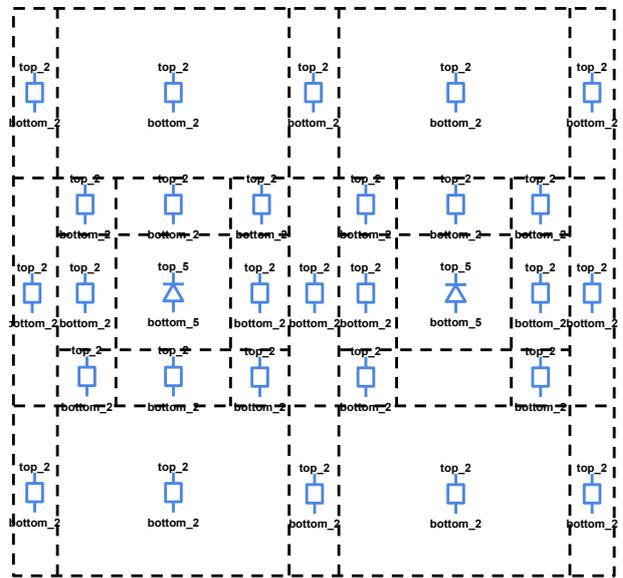
Figure 5.9 depicts side by side the meshes “inside” regions and the mesh “outside” regions. In general, these meshes are arranged in a list, and are labeled by index. The one “outside” regions is indexed by 0, and the ones “inside” regions are indexed by numbers starting from 1. The order of region is defined from upper left one to lower right one.

To summarize, the entire mesh has 2 slices: the “cut” through PN junction (DNTUB to P-substrate) results in two slices “top” and “bottom”. The “top” one has depth of N-well thickness, and the “bottom” one considers the rest of the P-substrate, as shown in figure 5.10. Extraction of parasitic component in such mesh (shown by black lines in figure 5.10) becomes more complicated than the previous cases. There will be three cases depending on their locations: “inside”, or “outside” regions, or “at the boundaries” of regions. For these ones:

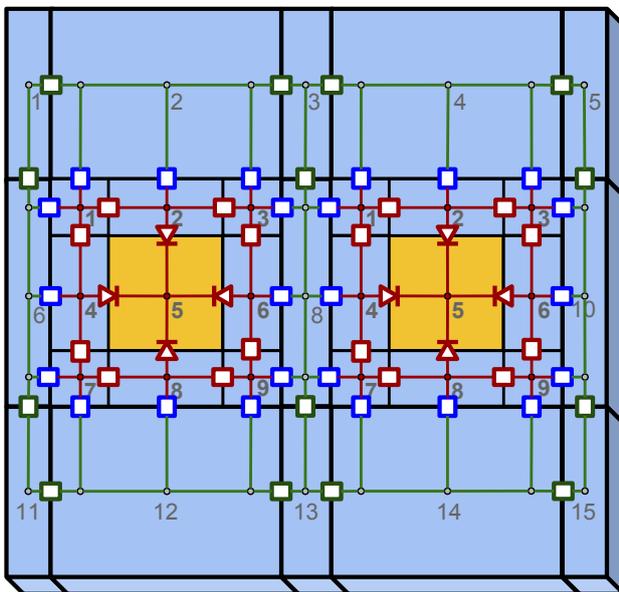
- “inside” regions (red components in figure 5.10), they are extracted in mesh from one region, like the mesh in figure 5.9a. The idea of extraction for parasitic components remains the same as we discussed in the previous section.
- “outside” regions (green components in figure 5.10), the parasitic components are extracted in mesh outside regions, like the mesh in figure 5.9b. The components are extracted between two adjacent elements, hence not every element in mesh has its adjacent elements in the outside region.
- “at the boundaries” of regions (blue components in figure 5.10), the parasitic components are extracted between two meshes: one from an inside region (figure 5.9a) and the other one from outside region (figure 5.9b). Extraction takes place at the boundaries of two meshes,



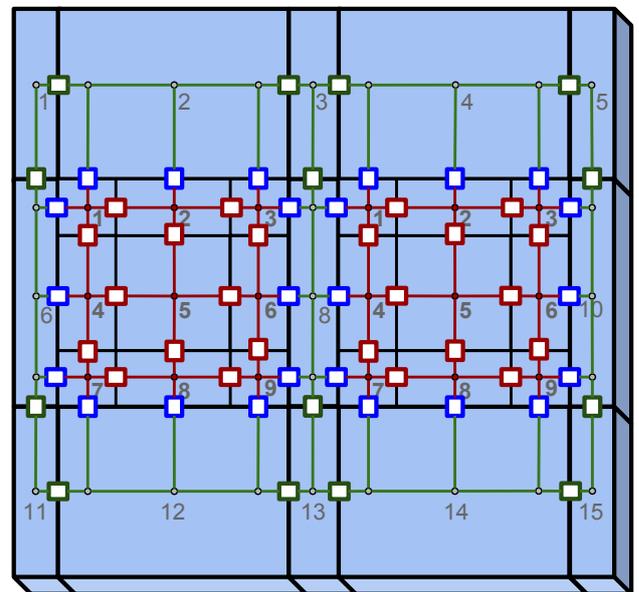
(a) "contacts"



(b) "top to bottom"



(c) "top"



(d) "bottom"

Figure 5.10: Decomposition of substrate parasitics following our modeling methodology: the mesh and the extracted parasitic netlist are shown in 3-D.

while two elements intersect.

Based on the idea above, the meshing strategy considering subregions is applied to the example in figure 5.6. The dash lines represent the mesh lines of resulting mesh in 2-D. The blue ones represent the meshing “inside” HV devices, the red ones represent the meshing “inside” LV devices, and the green ones represent the meshing “outside” regions. Thereby, the enhanced meshing strategy results in an optimized mesh. Such idea of mesh refinement targets to reduce the complexity of overall mesh, hence it saves the overall of system simulation time.

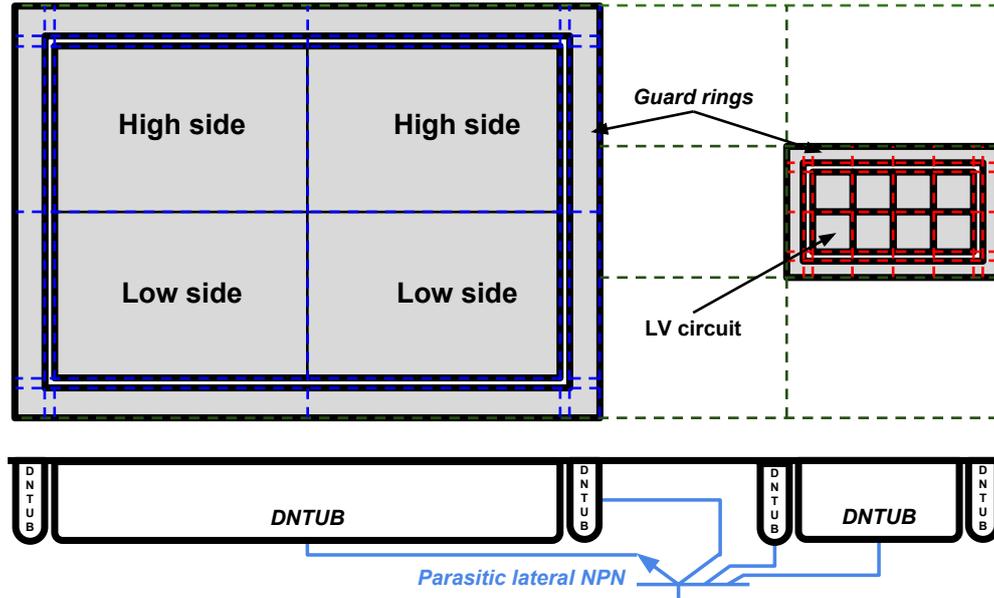


Figure 5.11: Meshing after optimization, considering device regions.

5.3.3 Simulation Results

Both structures $S1$ ($20\mu m$) and $S2$ ($60\mu m$), are implemented in Sentaurus TCAD simulations. The P-substrate doping density profiles were assumed constant and equal to $N_a=4.5 \cdot 10^{15} cm^{-3}$. The N-wells doping density profiles were assumed to be Gaussian with peak doping density of $2 \cdot 10^{17} cm^{-3}$. In the same way, doping density profiles of p+ and n+ doped diffusions were assumed to be Gaussian with peak doping density of $5 \cdot 10^{19} cm^{-3}$.

Table 5.2: DC simulation setup with voltage conditions.

| Simulation setup | Emitter [V] | | | Collector [V] | Base [V] | Temperature [$^{\circ}C$] |
|--------------------|-------------|------|------|---------------|----------|-----------------------------|
| | Start | End | Step | | | |
| DC Forward biasing | -1.0 | -0.2 | 50m | 5 | 0 | 27 |

Table 5.2 gives the setup of the proposed simulations at room temperature ($27^{\circ}C$): DC swept analysis were performed by sweeping the emitter (i.e. V_{N1} left) from $-1.0V$ to $-0.2V$ with step of

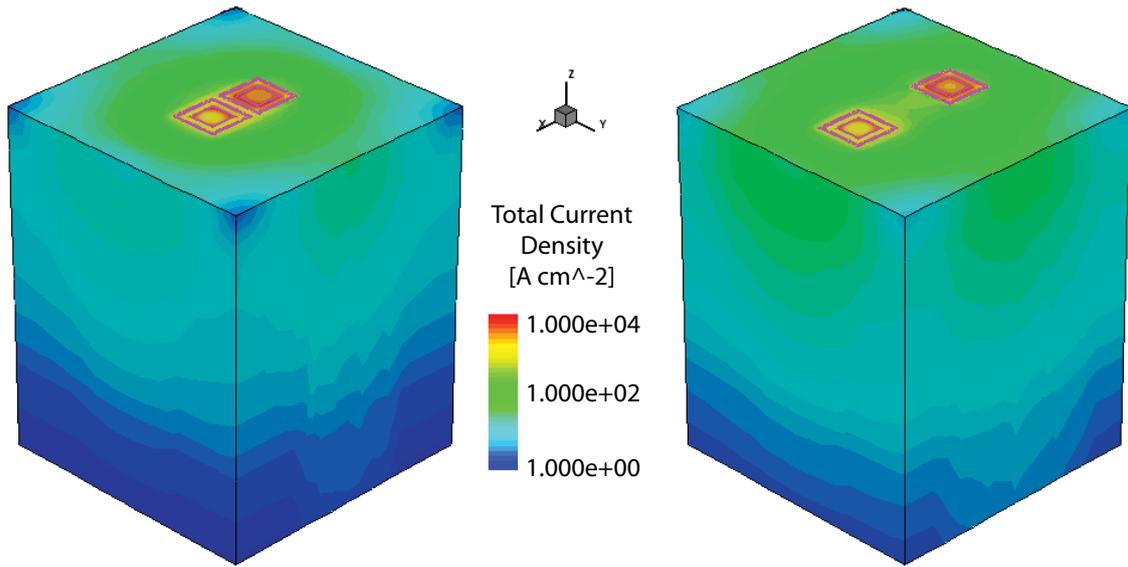
50mV while collector (i.e. V_{N2} right) is biased at 5V, and base (i.e. V_S) is grounded.

By forward biasing the base-emitter PN junction, substrate current is injected into substrate. At the same time, the diffused substrate current is collected at collecting well while the base-collector PN junction is reversed biased. This parasitic structure is formed as a parasitic lateral NPN bipolar transistor, as shown in Figure 5.7.

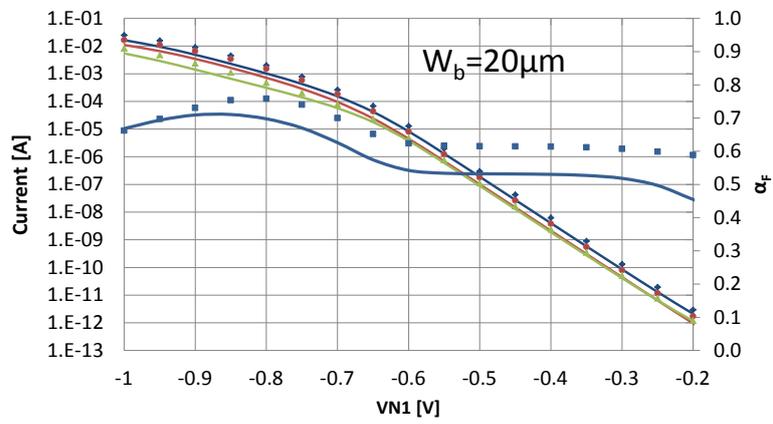
Table 5.3: Simulations output parameters of TCAD and SPICE simulations.

| DC swept simulation | | Meshes elements | DC points | Simulation Time [s] |
|---|-----------|-----------------|-----------|---------------------|
| $d = 20\mu m$ | TCAD | 325000 | 21 | 2 hours |
| | This work | 510 | 101 | 5 sec. |
| $d = 60\mu m$ | TCAD | 320000 | 21 | 2 hours |
| | This work | 510 | 101 | 5 sec. |
| Simulation were performed with Intel Core i5-3470S Processor (2.9GHz) | | | | |

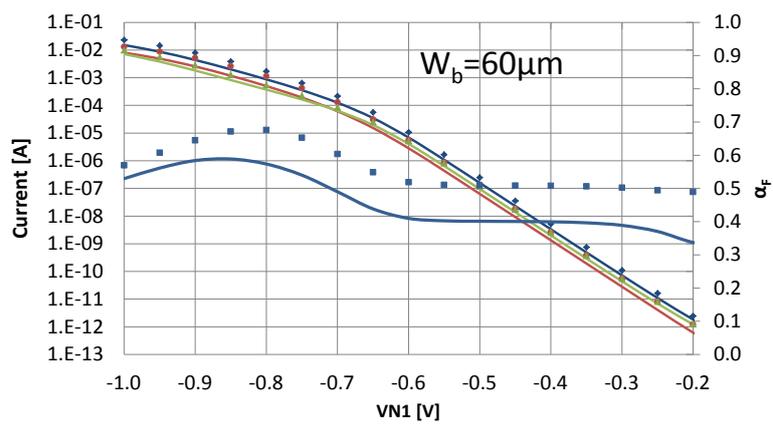
The curves in figure 5.12 show the IV characteristics and current gain parameter $\alpha_F = I_C/I_E$ for both structure $S1$ and $S2$. Results of both, TCAD simulations (points) and our work (lines) show the substrate currents and current gain α_F depending on the distance d . The distance effects are clearly observed. Moreover our work gives accurate and reliable results on parasitic currents to investigate the parasitic lateral BJT while reducing the simulation time considerably with respect to TCAD (see Table 5.3).



(a)



• IE_TCAD — IE_Spice • IC_TCAD — IC_Spice
 ▲ IB_TCAD — IB_Spice ■ α_F _TCAD — α_F _Spice



• IE_TCAD — IE_Spice • IC_TCAD — IC_Spice
 ▲ IB_TCAD — IB_Spice ■ α_F _TCAD — α_F _Spice

Figure 5.12: (a) TCAD simulations of two n-type well with distance of $20\mu m$ (left) and $60\mu m$ (right). (b) behavior of IV curve and α_F for $d=[20, 60]\mu m$, $V_C = 5V$.

5.4 Conclusion

In this chapter, we presented our approach to optimize the substrate meshing.

In the first part, we focused on device meshing optimization. The enhanced mesh resulted in less extracted parasitic components and less simulation time. The example of the diode was considered as an example showing a reduction up to 32% in the number of extracted components.

In the second part, the concept of regions (inside devices and outside devices) was introduced. The meshing algorithm is enhanced by defining the connection between the meshed regions. The example of a simple structure consisting of two N-wells was presented. DC simulations were performed to illustrate the impact of distance between the wells on the parasitic lateral NPN BJT. Comparison with TCAD simulations shown the effectiveness of the approach in terms of accuracy and speed.

Up to now a complete methodology for substrate parasitic extraction was introduced. It will be used in the next chapter for large circuits in two different high-voltage Smart Power technologies: 0.35 μm HV-CMOS technology of *ams AG* and BCD8sAUTO of *STMicroelectronics*.

Chapter 6

Experimental Validation

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6.1 Introduction

In the previous chapters, a methodology for post-layout substrate parasitic extraction was introduced. This approach aims at extracting the substrate parasitic considering also parasitic lateral NPN BJT in HV technology. Eventually, we extract the substrate as a model that can be simulated with a circuit-level simulator.

It is important that this newly extracted substrate model is back-annotated to the original circuit netlist. To do so, we consider the contacts of the substrate. The contacts are N-type or P-type implants square on the top slice. We associate a pin to a set of same physical contacts, the pin is the interface between the conventional post layout netlist of the circuit and the substrate parasitic network.

The process of model calibration is a necessary step for a newly developed substrate model. In order to fit the correct behaviors to measurements, technology parameters should be extracted according to a target technology. Thereby, several benchmark structures need to be defined for

the purpose of extracting these parameters. Hence, the project partners *ams AG* and *STMicroelectronics* provide us the benchmark chip of their technologies: *350nm HV-CMOS* for *ams AG*, and *BCD8sAUTO* for *STMicroelectronics*. In addition, another project partner from the German company *AdMOS* has developed parameter extraction and calibration methodology, in order to extract the technology parameters for *ams AG* technology.

The remaining of this chapter is organized as follows: In section 6.2, integration of CAD tool into *ams AG* hitkit is explained. In section 6.3, a process of model calibration and benchmarking is explained. Simulation results compared to measurements are reported. In section 6.4, we show the impact of the substrate model in circuit behavior. In section 6.5, we present our industrial test evaluation. In section 6.6, we present the process integration of our modeling approach for *BCD* technology. In section 6.7, investigations of substrate noise in *BCD* technology considering different isolation structures are discussed. Finally, we conclude the chapter in section 6.8.

6.2 PDK Integration for HV-CMOS Technology

In the phase of physical design (i.e. layout), designers have different approaches to try to minimize the parasitic. Nevertheless, post-layout verification is still needed in order to ensure the proper functionalities of the final design. To simulate the corresponding physical behaviors including parasitic, several tools and models have been implemented in the PDK of target technology.

In the conventional way, the extraction of parasitic consists in R-C (Resistive and Capacitive) extraction of metal connections, and possibly completed with R-C substrate network. In addition, substrate diode or bipolar effects have been considered as well. To do so, corresponding parasitic components should be extracted during post-layout extraction or they can be included as well in device compact models themselves. Since these parasitic components are layout dependent, only a few of them are correctly modeled in the design kit.

To complete the existing design flow of smart power technology, our approach has been integrated into *ams AG* hitkit for process node of $0.35\mu\text{m}$ HV-CMOS. The process of PDK integration mainly takes two steps:

- *Identification of the substrate PN junction;*
- *Netlist back-annotation.*

In the following subsections, these two steps are explained in detail.

6.2.1 Identification of the Substrate PN Junction

In the 350nm process node of *ams AG* HV-CMOS technology, there are 6 substrate masks in use. Each one represents a mask of a doped semiconductor layer, thus different material types and

doping concentrations. These 6 substrate masks are as follows:

- *DNTUB*: deep N-well;
- *DPTUB*: deep P-well;
- *SNTUB*: shallow N-well;
- *SPTUB*: shallow P-well;
- *NDIFF*: N-type implant;
- *PDIFF*: P-type implant.

They result in different combinations of substrate PN junction. In the *ams AG* hitkit, 8 substrate PN junctions are mentioned which can be extracted at post-layout. They are modeled by using the standard diode instantiating with geometry from the layout.

In our approach, we only take into account 4 of the substrate masks that are introduced above, and we ignore the “SNTUB” and “SPTUB” masks because of the following reasons. In the purpose of simplifying the models, we are concentrating on the masks which define the substrate PN junctions. Since the above two masks represent the wells implanted inside “DNTUB” and “DPTUB” wells thus having higher doping concentration, they do not contribute to define another substrate PN junction.

Since we consider 4 different masks in the substrate, then there will be 5 different materials (including P-substrate) in our case. Table 6.1 lists all the possible combinations of the 5 materials. The combination of two materials (one in row, and the other in column) results in one possible parasitic model: an enhanced diode is created between PN junction and marked as “D₋”; an enhanced resistor is created between two nodes of the same material and marked as “R₋”; a homojunction is created between junction with different doping concentrations and marked as “H₋”.

Table 6.1: Possible combinations of the 5 different materials and the corresponding parasitic models created for 350nm HV-CMOS technology of *ams AG*.

| | <i>PSUB</i> | <i>DNTUB</i> | <i>DPTUB</i> | <i>NDIFF</i> | <i>PDIFF</i> |
|--------------|-------------|--------------|--------------|--------------|--------------|
| <i>PDIFF</i> | H_{PDPS} | D_{PDDN} | H_{PDDP} | N/A | N/A |
| <i>NDIFF</i> | D_{NDPS} | H_{NDDN} | D_{NDDP} | N/A | |
| <i>DPTUB</i> | H_{DPPS} | D_{DPDN} | R_{DP} | | |
| <i>DNTUB</i> | D_{DNPS} | R_{DN} | | | |
| <i>PSUB</i> | R_{PS} | | | | |

Besides the material types and doping profiles, parasitic models are differentiated by spatial orientations. For example, DNPS diodes are extracted when finding deep N-well inside P-substrate. We define the sub-models of DNPS diode, namely: $DNPS_{vertical}$ and $DNPS_{horizontal}$. The former is used to represent the vertical components from P-substrate to the deep N-well, the latter is used

to represent the horizontal components surrounding the deep N-well. These models should be parametrized differently during model calibration and saved in the model library.

6.2.2 Netlist Back Annotation

In the conventional way, several steps are necessary in order to pass the post-layout verification. LVS* checks if the physical design corresponds to circuit schematic. QRC† extracts the circuit schematic and possible parasitic from the layout. Then, the post-layout simulation should be performed by using the same testbench during circuit design.

To complete the existing design flow, the proposed flow of post-layout extraction with PDK integration is implemented in *ams AG* hitkit, as shown in figure 6.1. The described flow at post-layout takes 2 steps, as follows:

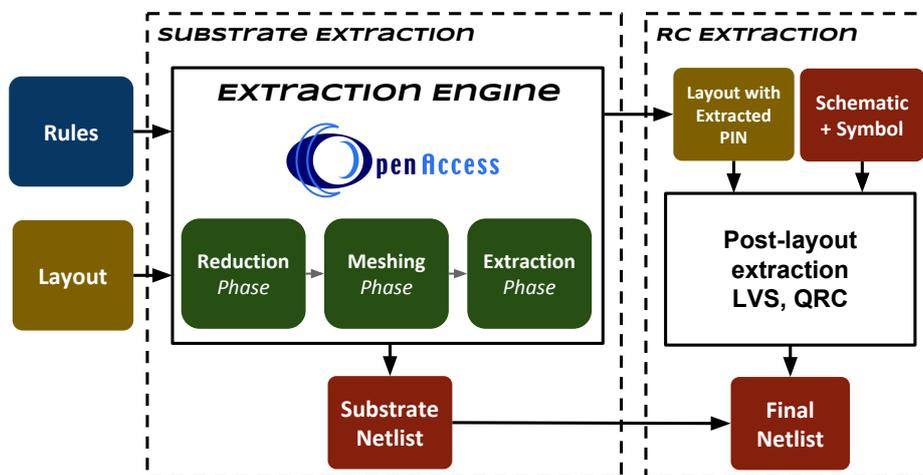


Figure 6.1: Design flow of post-layout extraction with PDK integration.

1. *Substrate parasitic extraction.* In our approach, we extract the substrate parasitic as an equivalent netlist. The interface of such netlist is realized by the components modeling vertical homojunctions. These homojunctions are extracted from N-implants or P-implants on the surface of the “top” slice. To back annotate our substrate model with the standard post-layout schematic, we extract the pins where the vertical homojunctions are extracted. In the meantime, an extended version of the original layout including these pins is created. This newly created layout is the one used in the next step.
2. *Standard extraction at post-layout including pins.* As in the conventional way, the new layout including the pins should pass LVS verification before launching the standard post-layout extraction. Once this layout has been approved, the QRC extraction is then performed. The

*Layout Versus Schematic, design verification tool.

†Cadence Quantus QRC Extraction Solution is the sign-off parasitic extraction tool.

QRC extraction takes into account the original circuit schematic, the R-C metal interconnections, and the substrate pins as well. Thereby, additions rules for these substrate pins was specified in hitkit of *ams AG*. As a consequence, short vias are extracted between metal wires and our substrate model.

6.3 Model Benchmarking for HV-CMOS Technology

Substrate parasitic modeling, in our approach, is based on a network of many lumped parasitic components. These components are handled by the enhanced models of EPFL diode, resistor, and homojunction [37]. Basically, modeling of such enhanced models need two kinds of parameters:

1. the geometrical parameters, such as length, area, etc., that are extracted from layout patterns in 3-D. The extracted components are instantiated with these parameters and saved in netlist;
2. the technology dependent parameters, such as doping concentrations and carriers' lifetime, etc., that represent the internal recipe of foundries. These parameters are unknown but should be extracted. Basic models of substrate PN junction (Table 6.1) are instantiated with these parameters, and saved in a model library.

The former is handled by our 3-D substrate extraction tool, and the latter should be considered afterward. In a target HV technology, the process of parameter extraction and model calibration is a necessary step for a newly developed substrate model.

In general, the process of model calibration could be done as well through TCAD[‡]. However, TCAD simulations need a detailed description of doping concentrations, and it may not fit the actual process conditions used for manufacturing. Therefore, in the framework of AUTOMICS project, a new strategy is developed for extracting those technology parameters done by *AdMOS*, and applied to *ams AG* technology. Figure 6.2 depicts the describing flow of parameter extraction and model calibration process.

To extract the parameters, a special algorithm is used to fit simulations with measurements. The layout of benchmark structures has been studied, and netlist is extracted by using the 3-D extraction tool. A preliminary model library containing basic models with initial parameters are used for the first time. A control code is added automatically to perform the simulations with the same condition as in the measurements of the test devices. The simulations are compared to measurements and used by an optimization algorithm to tune the available model parameters. After calibration is done, a set of calibrated model parameters is added to the final model library that is used for parasitic simulation.

[‡]Synopsys Sentaurus Technology Computer-Aided-Design tools.

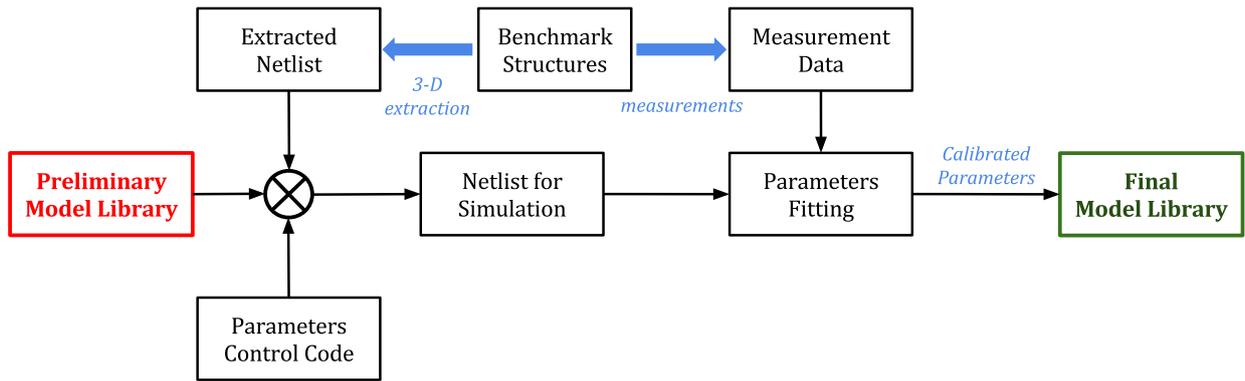


Figure 6.2: *AdMOS* parameter extraction and model calibration process, for *ams AG* technology.

In this work, we are not going to detail the strategy of parameter extraction, but we illustrate the work of model calibration. The model calibration is performed by using industrial benchmark structures. Test chips for benchmarking are provided by *ams AG* for 350nm process node of HV-CMOS technology. The test chips include various benchmark structures, from basic diodes to combinations of implanted wells, in order to measure and characterize the different substrate PN junction behaviors as well as the interaction between different wells and/or implants.

In this work, we mainly focus on 3 types of substrate PN junctions, as illustrated in figure 6.3. These PN junctions in substrate possibly result in 3 kinds of parasitic components, as follows:

- vertical PNP transistor includes DPDN and DNPS junctions;
- vertical NPN transistor includes NDDP and DPDN junctions;
- lateral NPN transistor includes 2 DNPS junctions over P-substrate.

A process of model benchmarking is detailed in the following subsections. To begin with, we model the basic stand alone DNPS diode in the section 6.3.1; then the parasitic lateral NPN transistor is studied in the section 6.3.2, and the investigations of substrate current are also discussed in this section; finally, the parasitic vertical BJT (NPN and PNP) are modeled in the section 6.3.3.

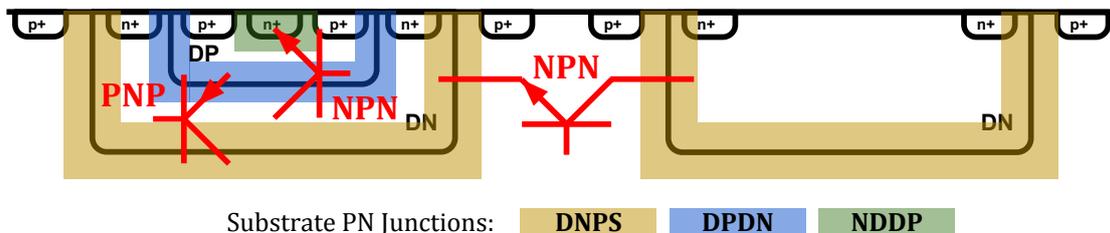


Figure 6.3: Illustration of 3 kinds of substrate PN Junctions existing in HV-CMOS technology. The combination of these PN Junctions results in 3 types of parasitic bipolar transistors: vertical NPN, PNP and lateral NPN.

6.3.1 DNPS diode modeling

As the first case study, a benchmark structure of DNPS diode has been investigated 6.4. The structure under study is an area diode with dimension $800\mu \times 800\mu$. The output parameters from extraction and simulation are summarized in Table 6.5.

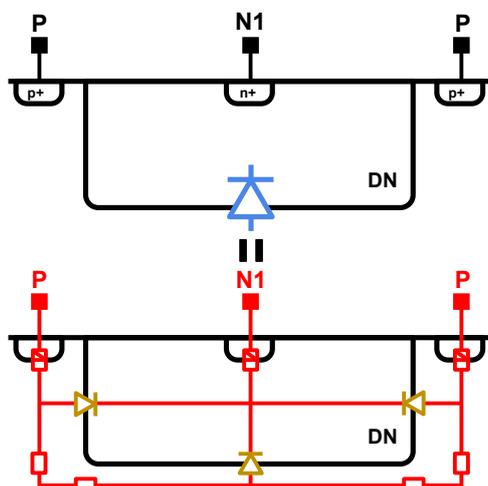


Figure 6.4: Illustration of parasitic diode DNPS and its equivalent circuit.

Results of DC behaviors including forward and reversed biased conditions are reported in Figure 6.5. Results from simulations are drawn with straight lines and measurement with dots. In the same figure, curves in colors show the temperature behaviors at: 27°C (blue), 75°C (black) and 125°C (red).

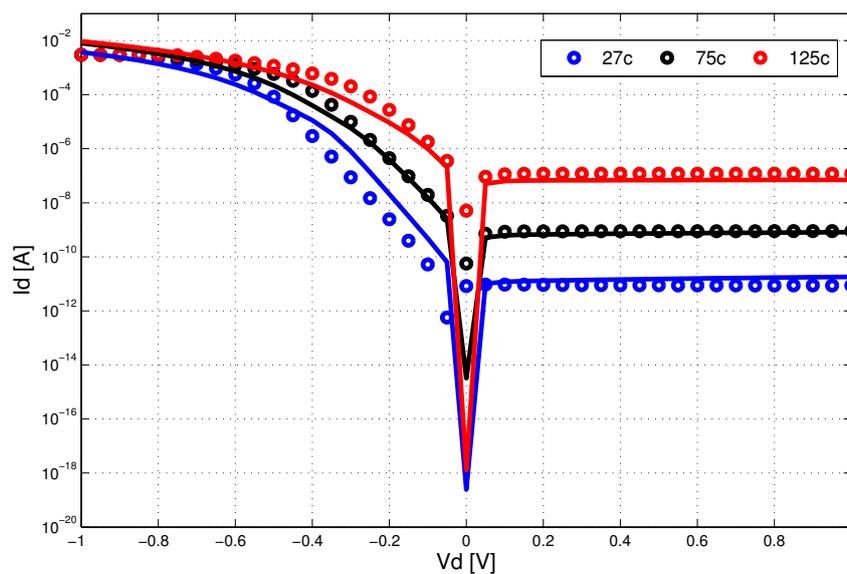


Figure 6.5: Diode DC current behavior as function of bias voltage and temperature. Comparisons between measurement (symbols) and simulation (lines).

6.3.2 Parasitic lateral NPN modeling with DNPS diodes

The modeling of parasitic lateral NPN BJT in HV-CMOS technology is a hard task. The emitter is the injecting N-well of substrate currents (usually power devices), the collectors are the surrounding N-wells and the base is the whole substrate. Modeling of such parasitic lateral NPN is therefore impossible using compact BJT models, since the victims of substrate noise coupling can be anywhere in the substrate and the geometrical patterns of layout substrate can never be correctly extracted.

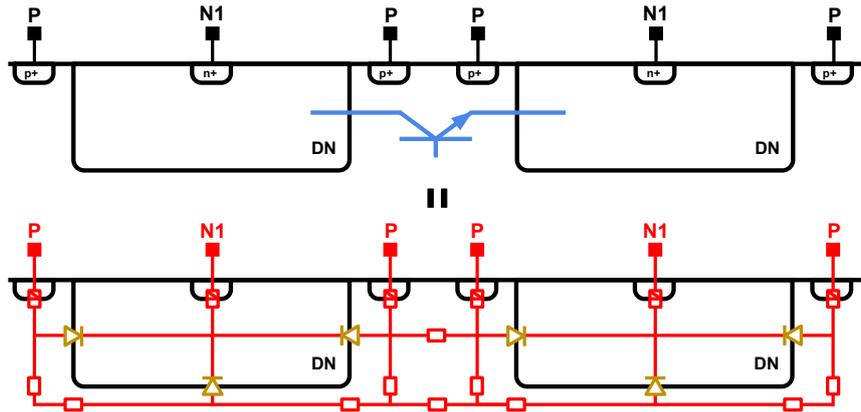


Figure 6.6: Illustration of parasitic lateral NPN BJT and its equivalent circuit.

In our methodology, modeling of such parasitic lateral NPN BJT is realized by constructing a substrate parasitic equivalent model, as shown in figure 6.6. This substrate model includes DNPS diode (yellow) that models the PN junction behavior between DNTUB well and P-substrate. Thereby, the bipolar effects of parasitic lateral NPN BJT is handled by two back-to-back DNPS diodes [37].

Such DNPS diodes should be calibrated in order to fit the correct physical behaviors. The model calibration is performed by fitting the simulation to measurement with various of benchmark structures. One of the benchmark chips designed and fabricated by *ams AG*, in 350nm HV-CMOS technology process, is illustrated in figure 6.7.

We mainly focus on the investigation of geometrical floor-planing of layout, where the distance effect is under study, as well as the influence of shielding structure to protect the sensitive area from parasitic substrate current. In addition, influence of temperature as well as voltage supplied are under investigation.

This test chip includes 15 DNPS diodes sharing the same substrate. The test chip has 16 I/O PADs: the first 15 PADs (*PAD1* to *PAD15*) connect to the N-wells of 15 DNPS diodes individually, and the *PAD16* connects to 15 P-wells where each one surrounds a DNPS diode.

The extraction of this test chip is taken in two steps: 1) the extraction of each DNPS devices;

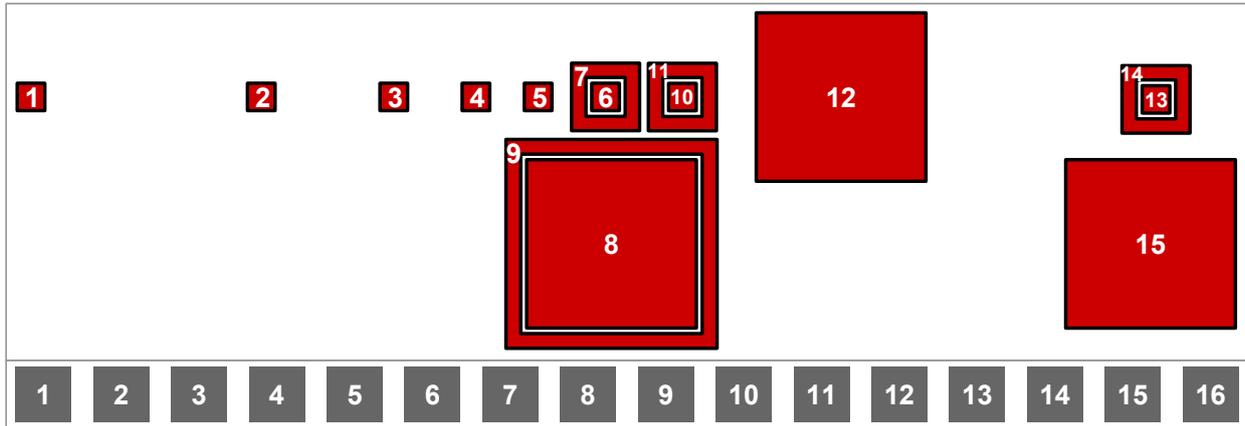


Figure 6.7: Simplified layout view of benchmark chip.

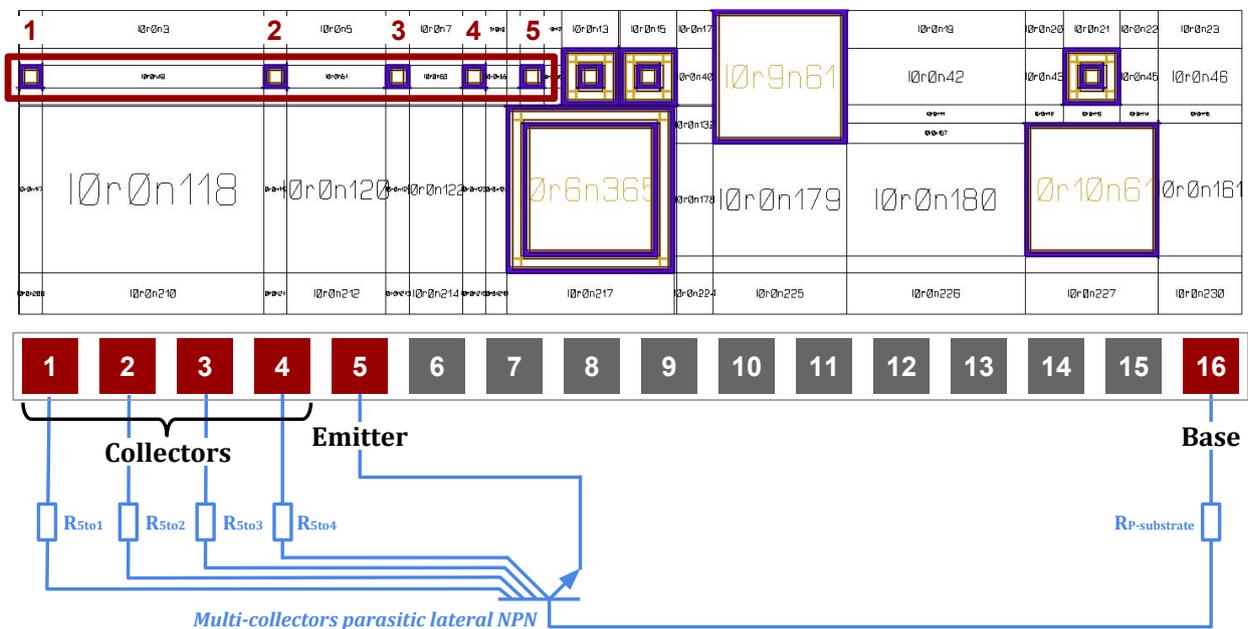


Figure 6.8: Benchmark 1: PAD1 to PAD5 are involved (enclosed by red rectangle). Substrate parasitic equivalent component is drawn in blue.

2) the extraction of the whole chip outside DNPS diodes. The combination of the two is the final result of extraction as reported in table 6.5. It is important to notice that, the 15 DNPS diodes that are extracted from standard layout extraction should be switched off, because our substrate model already take them into account.

6.3.2.1 Benchmark 1: impact of distance

In the first test case, 5 DNPS diodes are involved, as shown in figure 6.8. In this case, we mainly focus on the investigation of parasitic lateral NPN BJTs as function of distance while injecting electrons into substrate from *PAD5* and collecting them at each *PAD* respectively.

The 5 DNPS diodes have the same size. Each one includes a DNTUB well $20\mu\text{m} \times 20\mu\text{m}$ and a surrounding DPTUB well. The first 4 DNPS diodes (“1”, “2”, “3” and “4”) have different distance to the last one “5”, and they are connected to I/O PADs (“PAD1”, “PAD2”, “PAD3”, “PAD4” and “PAD5”) respectively.

Setups for measurement and simulations are listed in Table 6.2. *PAD5* is the emitting point of substrate current that is connected to an input voltage source. The emitting voltage (*PAD5*) is swept from -0.2V to -1.0V to cover the whole range from low current up to high current injection regimes. The collector is one of the 4 other PADs at a time, while all the others are left open (connected to resistors with high impedance $1e^{18}\Omega$ for simulation). The base is the substrate thus *PAD16* is grounded in all cases.

For the four test cases in table 6.2, results of simulation and measurements are compared as shown in figure 6.9. The curves with straight lines represent simulation results and while the dots are measurements. The sub-figures in figure 6.9 from top to bottom represent the collected current at *PAD1*, *PAD2*, *PAD3* and *PAD1*, respectively. A good agreement with measurements shows reliable results from simulation.

Same setup with different temperature conditions were performed as well. In the same figure 6.9, curves in colors illustrate the results at -25°C (blue), 27°C (black) and 125°C (red). Both measurements and simulations confirm the temperature effect as expected: current at both emitter and collector are increased as temperature arises.

6.3.2.2 Benchmark 2: impact of guard ring

The second test case includes 4 DNPS diodes, as shown in figure 6.10. They are connected to *PAD4*, *PAD5*, *PAD6* and *PAD7*. The objective of this test case is to investigate the influence of guard ring to protect the sensitive target. *PAD4* and *PAD6* are victims of substrate current injected from *PAD5*, however, *PAD6* is under protection of guard ring *PAD7*, and *PAD4* has no protection.

The DNPS diodes 4, 5 and 6 have the same dimensions $20\mu\text{m}$ by $20\mu\text{m}$, and the diode 7 is

Table 6.2: Measurement and simulation setups for benchmark 1, “nc” stands for “not connected”.

| Tests | <i>Emitting PADs</i> [V] | <i>Collecting PADs</i> [V] | | | | <i>Base</i> [V] | <i>Temperature</i> [$^\circ\text{C}$] |
|-------|--------------------------|----------------------------|----|----|----|-----------------|---|
| | 5 | 1 | 2 | 3 | 4 | 16 | |
| 1 | -0.2→-1.2 | nc | nc | nc | 0 | 0 | -25, 27, 125 |
| 2 | | nc | nc | 0 | nc | | |
| 3 | | nc | 0 | nc | nc | | |
| 4 | | 0 | nc | nc | nc | | |

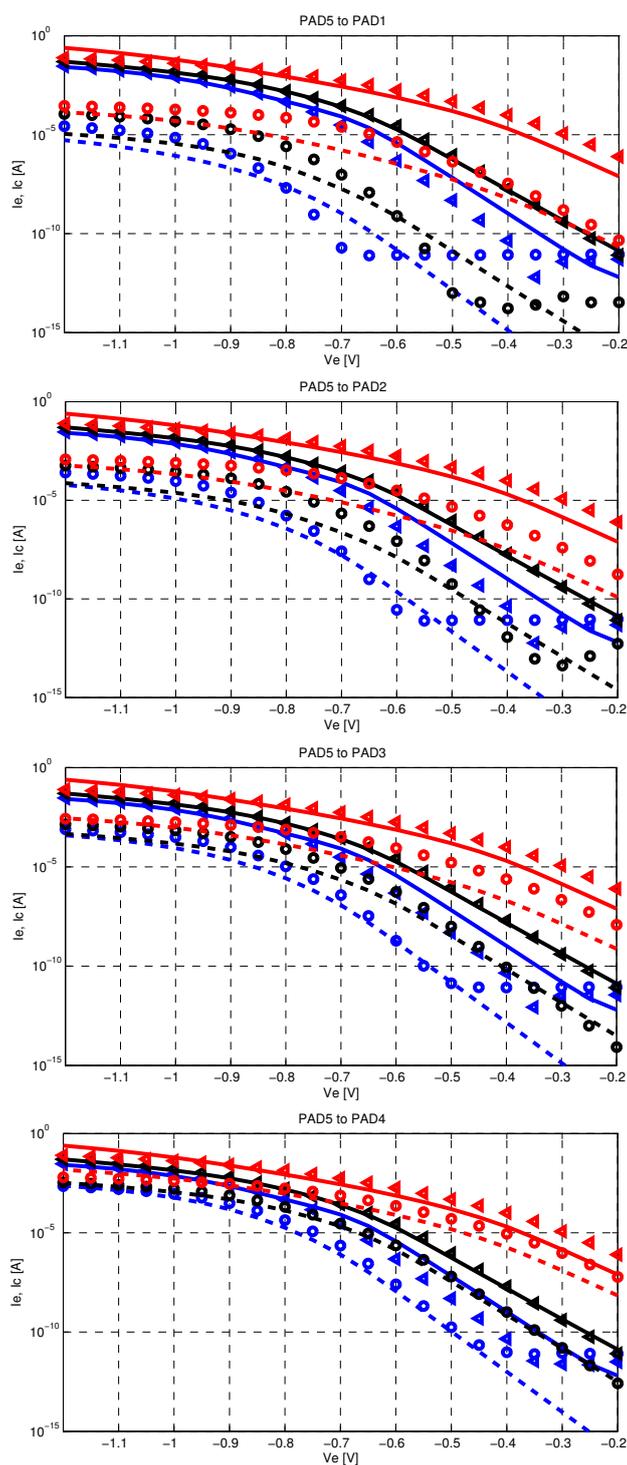


Figure 6.9: Current-voltage characteristics and temperature behaviors: -25°C (blue), 27°C (black) and 125°C (red) of parasitic lateral NPN BJTs. The currents at emitter I_e (triangle or solid line) and collector I_c (circle or dash line) are shown in figure while simulation (lines) are compared to measured one (symbols). The distance effect is observed also from the 4 test cases where collector is PAD1 to PAD4 respectively (from top to bottom).

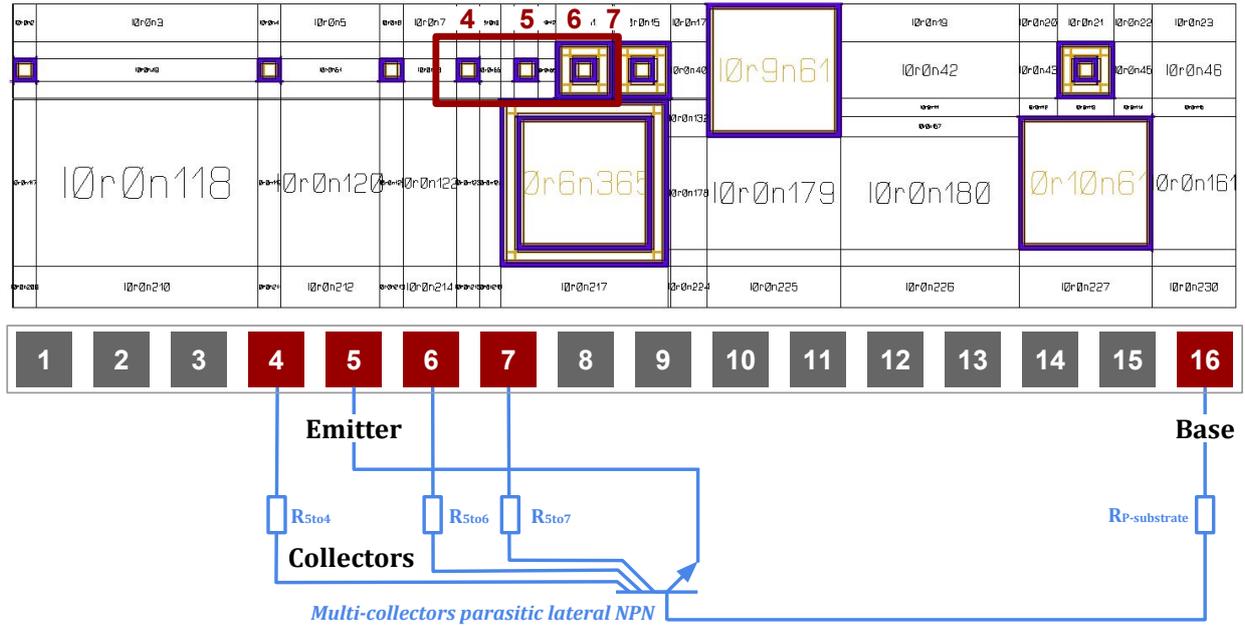


Figure 6.10: Benchmark 2: *PAD4* to *PAD7* are involved (enclosed by red rectangle). Substrate parasitic equivalent component is drawn in blue.

the guard ring to diode 6 surrounding. In this test case, the diode 5 is the aggressor of substrate currents while the diodes 4 and 6 are victims located at left side and at right side, respectively. The diodes 4 and 6 have the same distance to diode 5, thus the distance dependency is discarded here. Schematic (blue) in figure 6.10 shows the parasitic lateral NPN BJT of interest.

Emitter voltage is swept from $-0.2V$ to $-1.0V$ while the base (p-substrate) and two collectors are both grounded. Different setups for biasing the guard ring, either connected to power source (50V) or grounded or even left open, are summarized at Table 6.3.

Parasitic substrate network has been extracted and then simulated for both guard ring biasing cases at room temperature. Results from spice simulations (lines) are compared to measured data (symbols), and drawn in graphs in figure 6.11. Current path driven by electrons and holes are created with activation of a multi-collectors lateral parasitic BJT, thus electrons are injected into substrate from *PAD5* (red), then collected by *PAD4* (blue), *PAD7* (cyan) and *PAD6* (black).

Table 6.3: Measurement and simulation setups for benchmark 2, “nc” stands for “not connected”.

| Tests | <i>Emitting PADS</i> [V] | <i>Collecting PADS</i> [V] | | | <i>Base</i> [V] |
|-------|--------------------------|----------------------------|---|----|-----------------|
| | | 5 | 4 | 6 | 7 |
| 1 | 0.2 → 1.2 | 0 | 0 | 0 | 0 |
| 2 | | | | 50 | |
| 3 | | | | nc | |

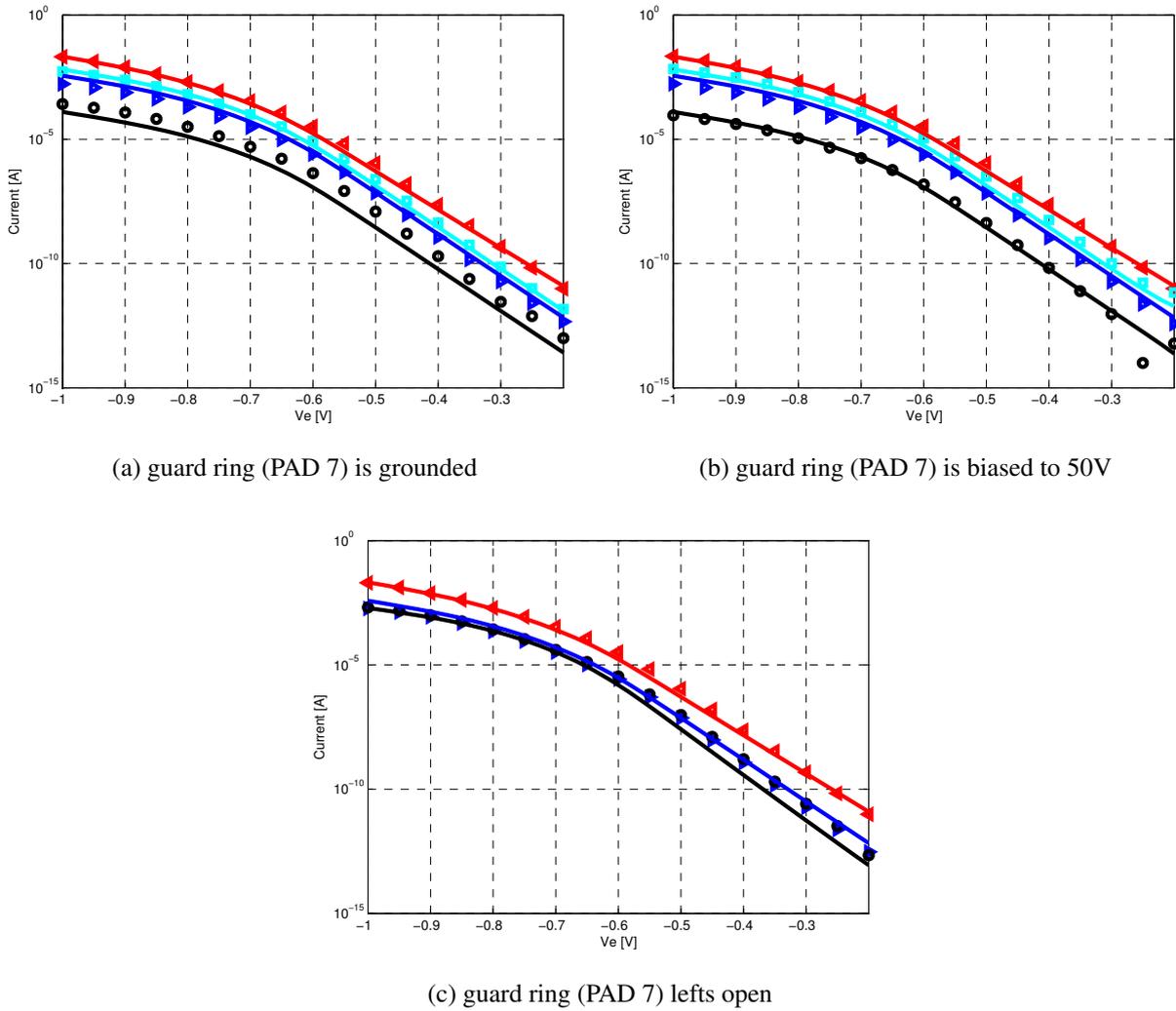


Figure 6.11: IV characteristics for benchmark 2 with comparison between simulation (lines) and measured data (symbol): currents at emitter (red), at collector without protection (blue), at collector with protection (black) and at guard ring (cyan).

Both measurement and simulation show the impact of guard ring that protects the victim (*PAD6*, black) from parasitic coupling noises. Majority of electrons on current path (*PAD5* to *PAD6*) are collected by guard ring (*PAD7*, cyan). However, victim will suffer from parasitic noises either without protection (*PAD4*, blue) or when guard ring is not biased.

6.3.2.3 Benchmark 3: impact of guard ring biasing

The third test case includes four DNPS diodes: 6, 7, 10 and 11, as shown in figure 6.12. They are connected to *PAD6*, *PAD7*, *PAD10* and *PAD11*, respectively. In this case, we are interested to investigate the influence of guard ring not only on the collector side but also on the emitter side.

The diodes 6 and 10 have the same size $20\mu\text{m}$ by $20\mu\text{m}$. The diode 6 acts as the aggressor of

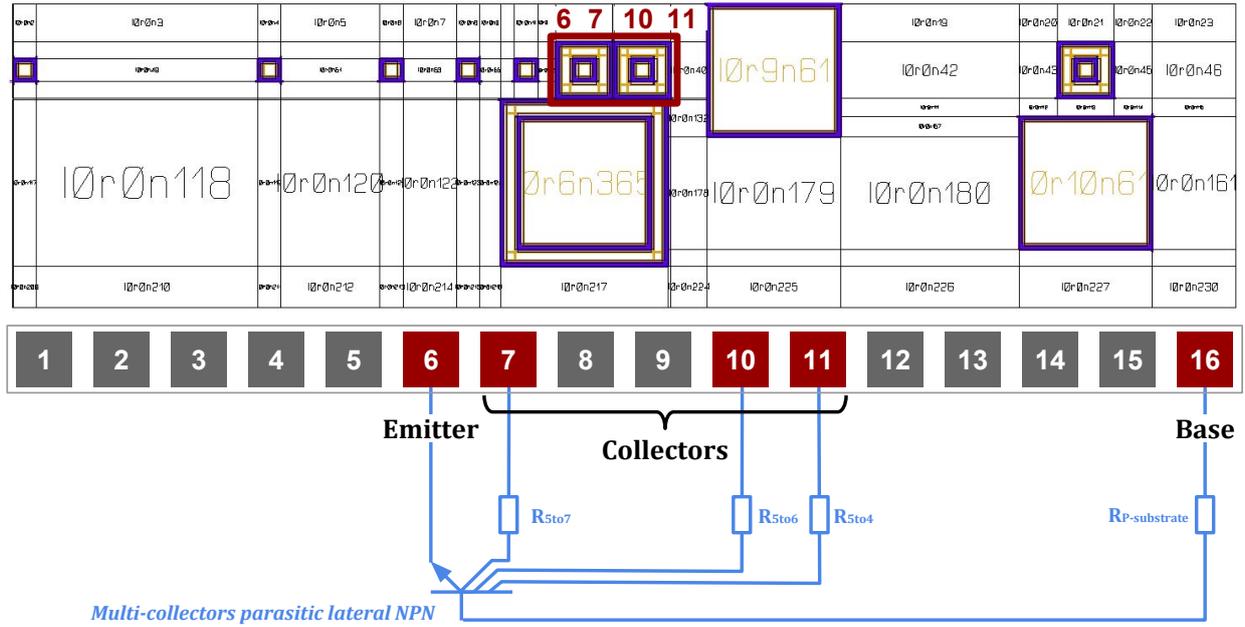


Figure 6.12: Benchmark 3: *PAD6*, *PAD7*, *PAD10* and *PAD11* are involved (enclosed by red rectangle). Substrate parasitic equivalent component is drawn in blue.

substrate parasitic, and diode 10 is target victim, as shown in figure 6.12. In addition, 7 and 11 are the shielding structures to diodes 6 and 10, respectively. Schematic in blue represents the parasitic BJTs of interest.

The *PAD6* is the emitting point and is connected to the input voltage source. The emitting voltage is swept from $-0.2V$ to $-1.0V$. The *PAD10* is the collector and it is grounded. Setup of measurements and simulations are reported in table 6.4. In this test case, guard ring *PAD7* and *PAD11* have different biasing: either they are both grounded, or one of them left open, or both left open.

Results of simulations (lines) are compared to measurements (symbols), as shown in Figure 6.13. Curves represent the emitting current (red), collecting currents at collector (black), at

Table 6.4: Simulation and measurement setups for benchmark 3, “nc” stands for “not connected”.

| Tests | Emitting PADs [V] | | Collecting PADs [V] | | Base [V] |
|-------|-------------------------|----|---------------------|----|----------|
| | 6 | 7 | 10 | 11 | 16 |
| 1 | -0.2 \rightarrow -1.2 | 0 | 0 | 0 | 0 |
| 2 | | 0 | | nc | |
| 3 | | nc | | 0 | |
| 4 | | nc | | nc | |

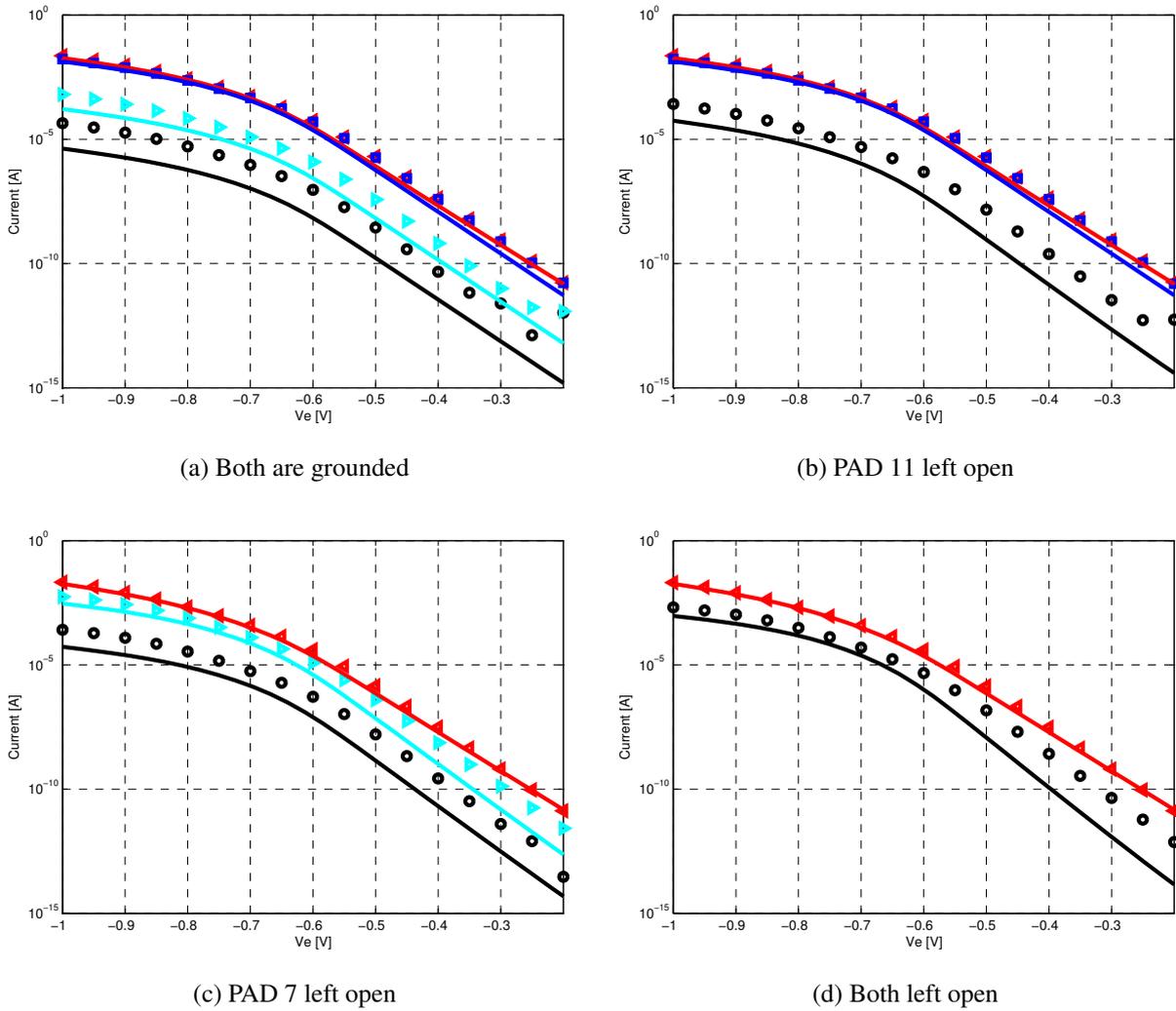


Figure 6.13: IV characteristics for benchmark case SUBC12T3 with comparison between simulation (lines) and measured data (symbol): currents at emitter (red), at collector (black), at guard ring of emitter (blue) and guard ring of collector (cyan).

guard ring of emitter (blue) and at guard ring of collector (cyan). The curves (Figure 6.13) show that: when both guard rings are left open, victim (PAD 10, black) collects most of the substrate current (worst case). In the contrary, victim has been protected from substrate current if both guard rings are grounded (best case). Otherwise, if only one guard ring is biased, victim can be protected as well, though less efficiently. Moreover guard ring at emitter (PAD 7, blue) has more efficiency when compared to the other one (PAD 11, cyan).

6.3.3 Parasitic vertical BJT modeling with enhanced diodes

In HV-CMOS technology, a deep N-well isolates the transistors from the substrate. Inherently this structure introduces a parasitic vertical bipolar junction transistors (BJTs). For a N-channel (or P-channel) LDMOS transistor, the drain of N-MOS (or P-MOS) transistor corresponds to the emitter of vertical NPN (or PNP) BJT, which is usually connected to the load. During power stage switching, the below ground (or above supply) condition at drain of LDMOS transistor may activate the possible vertical BJT that injects carriers (electrons and holes) into substrate.

This kind of parasitic structure is often seen in HV-CMOS technology, where the vertical parasitic BJTs can be added in compact model of standard spice model. However, the parasitic lateral components are hard to be modeled using standard compact model, as we have explained in chapter 3. To study these vertical BJTs, we select the benchmark structures as the existing BJT of the process, namely the NPN (VERTN1) and PNP (VERTPH), as shown in figure 6.14.

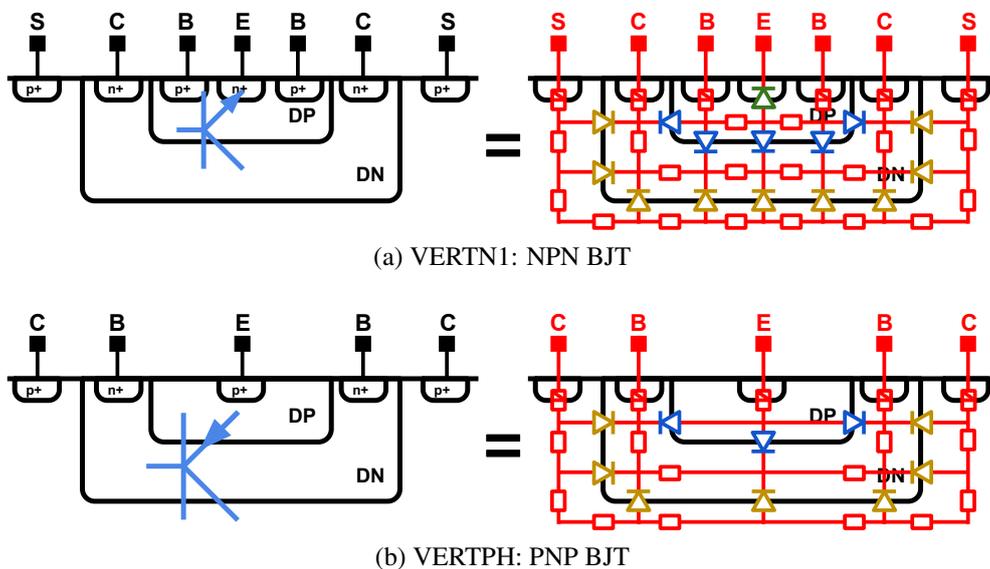
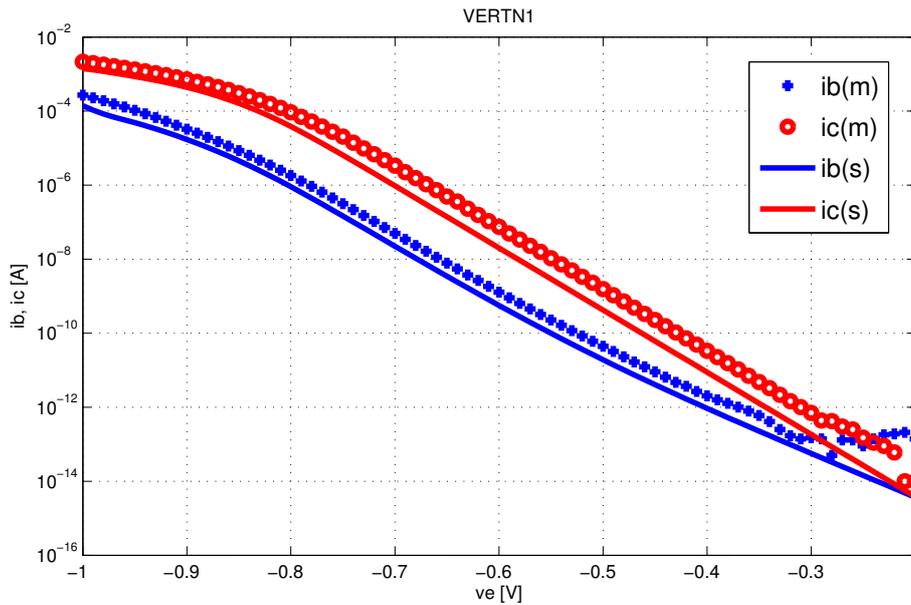


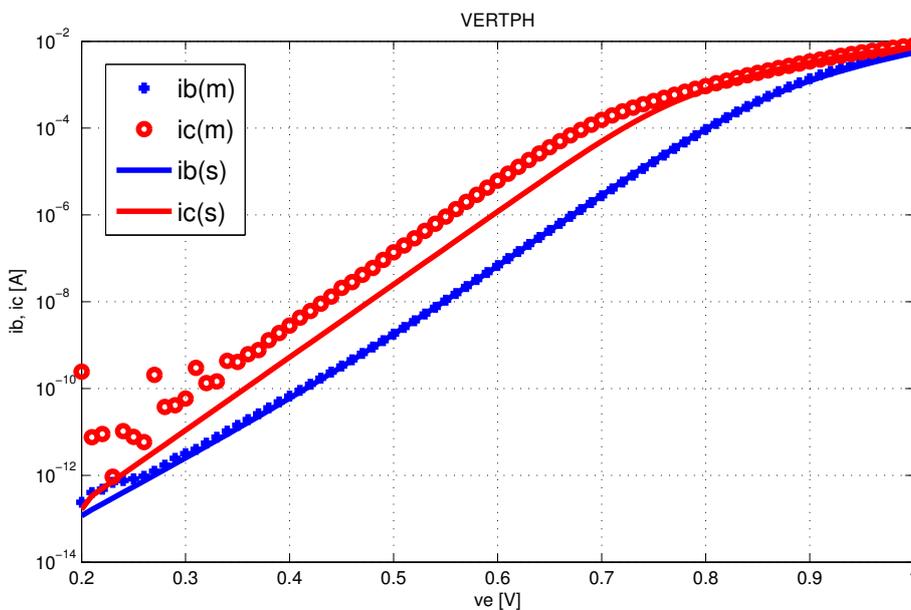
Figure 6.14: Structure of bipolar transistors and their equivalent circuits.

In our methodology, the modeling of these parasitic BJTs is done by extracting vertical connected back-to-back or front-to-front enhanced diodes to the netlist, as shown in figure 6.14. The back-to-back connection of these enhanced diodes propagates minority carriers allowing NPN BJT simulations. In the same way, the front-to-front connection of enhanced diodes can simulate parasitic PNP BJT. Extracted netlists (red) from these structures are equivalent to devices themselves: NPN in figure 6.14a and PNP in figure 6.14b.

Moreover, the model of vertical BJTs consists of enhanced diodes with different technology parameters setting. For example, the structure of NPN BJT (Figure 6.14a) is a N-P-N-P configuration including DNPS (yellow), DPDN (blue) and NDDP (green) diodes; and the structure of PNP BJT (Figure 6.14b) includes DNPS (yellow) and DPDN (blue) diodes only.



(a) VERTN1: NPN BJT



(b) VERTPH: PNP BJT

Figure 6.15: DC behaviors of NPN (VERTN1, a) and PNP (VERTPH, b) BJT. Results of simulation (lines) are compared to measured data (symbols).

Calibration of these diodes are performed by using the standard bipolar cells from library which has well defined structure of vertical BJT. Report on extraction and simulation of two BJTs is summarized in Table 6.5. Since post-layout extraction of BJT includes compact model itself, a “flag” inside model can switch on or off the model depending on whether the 3-D extraction tool is used or not. Curves depicted in figure 6.15 shows the measurements (dots) and simulation (lines) after parameters calibration. Bipolar effects for both NPN and PNP in DC are confirmed.

Table 6.5: Results of proposed post-layout extraction and simulation.

| Test structures | | DNPS | SUBC1 | VERTN1 | VERTPH |
|---|---------------|------|-------|--------|--------|
| Total number of nodes | | 154 | 1958 | 238 | 313 |
| Total number of components | | 262 | 3419 | 440 | 601 |
| Substrate extraction | diode* | 17 | 487 | 71 | 54 |
| | homojunction* | 68 | 163 | 76 | 147 |
| | resistor* | 177 | 2676 | 280 | 392 |
| Extraction time (s) | | 1.96 | 19.71 | 2.23 | 2.57 |
| QRC extraction | diodes | 1 | 15 | 0 | 0 |
| | capacitor | 0 | 47 | 9 | 3 |
| | resistor | 0 | 31 | 4 | 5 |
| | bjt | 0 | 0 | 0 | 0 |
| | jfet | 0 | 0 | 0 | 0 |
| Simulation time (s) | | 2.5 | 12.6 | 1.1 | 1.23 |
| Components with * are enhanced EPFL parasitic components | | | | | |
| Work is performed with Intel Core i5-3470S Processor (2.9GHz) | | | | | |

6.4 Impact of Substrate Parasitic in HV-CMOS Technology

Current mirror is a simple circuit that is widely used in analog IC design. This circuit is designed to replicate a current through one active current branch I_{ref} to another active current branch of circuit, therefore keeping the output current I_{out} constant regardless of loading, as circuits shown in figure 6.16.

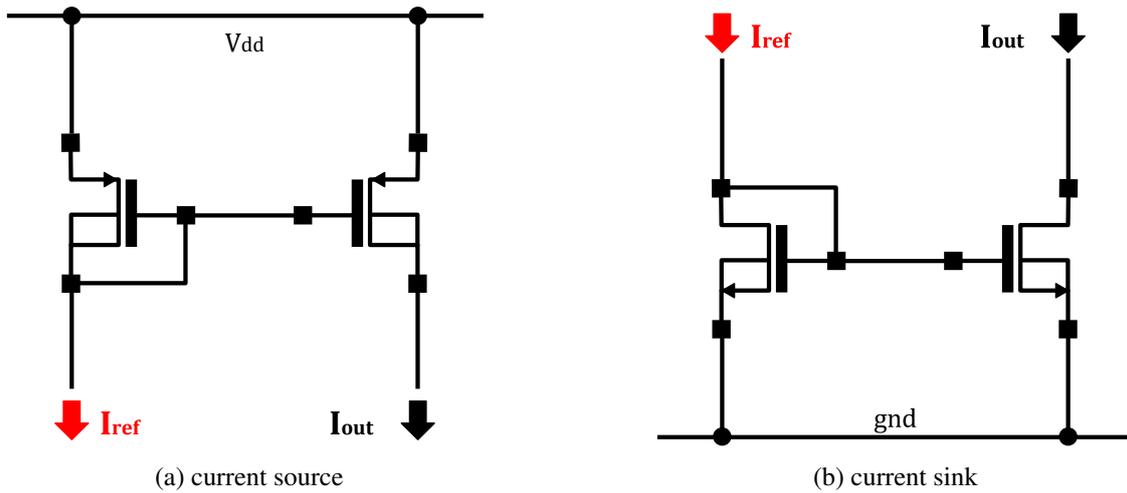


Figure 6.16: Circuit configuration of current mirror. Depending on the circuit, it can be either a current source (a) or a current sink (b).

In this example illustrated in figure 6.17, we are interested in the impact of substrate currents to this basic analog circuit. The circuit of example consists of three N-channel LDMOS transistors. Transistor $M1$ is a self biasing HV N-MOS transistor that injects substrate current from a negative supply voltage source marked as “ V_{in} ” in figure 6.17. Transistors $M2$ and $M3$ are in current mirror configuration and have the same size (i.e. W and L) as transistor $M1$, but transistor $M2$ is closer to $M1$ than transistor $M3$ in layout point of view. Besides, we consider the circuit in two cases:

- case 1: transistor $M2$ is the source of current mirror, it is closer to aggressor $M1$;
- case 2: transistor $M3$ is the source of current mirror, and it is farther from aggressor $M1$.

From geometrical point of view, the substrate parasitic models in both cases are similar to each other, as depicted in figure 6.17c. The extracted netlists of substrate parasitic are back-annotated to circuit schematic via the extracted PIN layers.

A transient signal with a negative pulse ($-1V$, $2\mu s$) is applied to input voltage source, as depicted in figure 6.18. Between $1\mu s$ and $2\mu s$, the voltage at drain of transistor $M1$ goes below ground ($-1V$) thus causes the forward biasing of substrate DNPS diodes (yellow) at $M1$. Under such condition, electrons and holes are injected into the substrate, and create currents that propagate to the rest of the substrate.

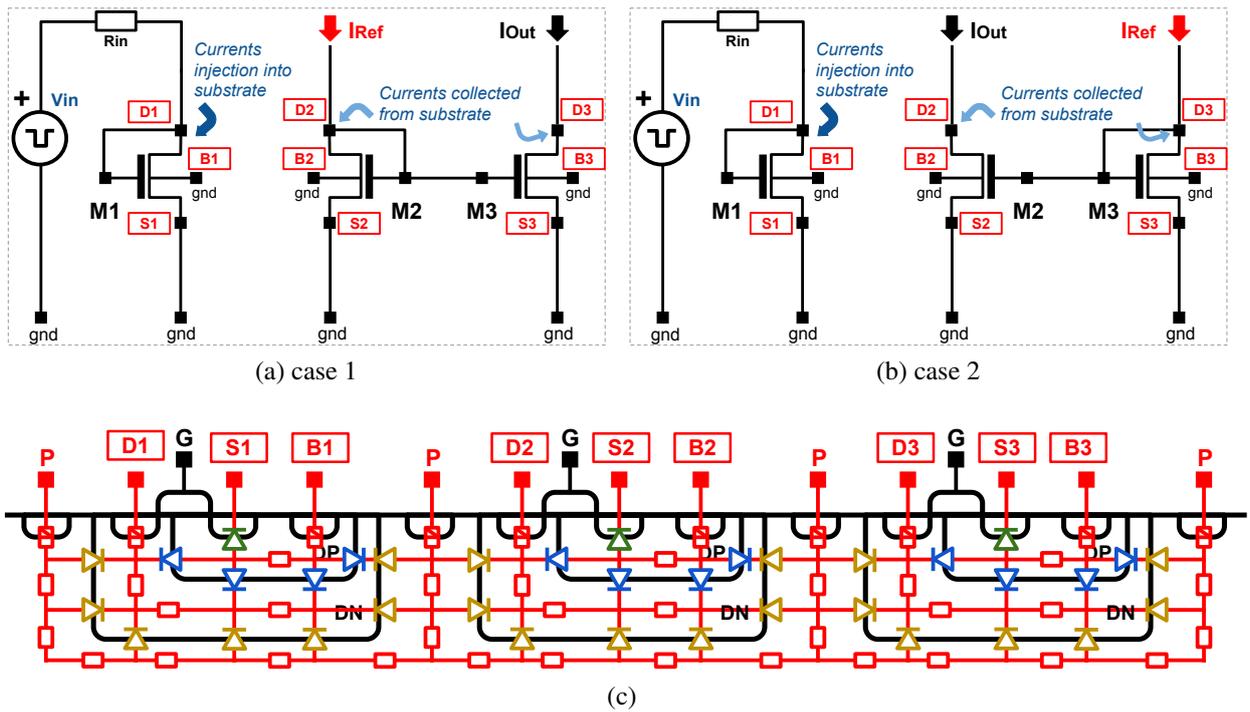


Figure 6.17: (a, b) Test circuit of 2 current mirror configurations, and (c) the equivalent substrate network.

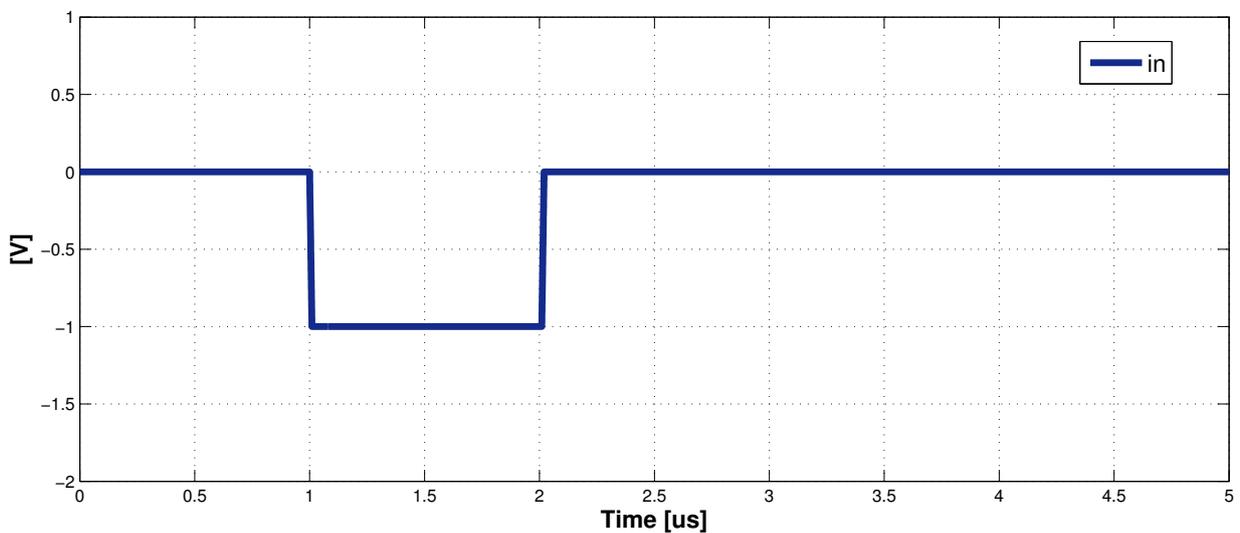


Figure 6.18: Transient signal at input voltage source “ V_{in} ”.

The forward biasing of DNPS diodes at $M1$ triggers the parasitic lateral NPN BJT's between $M1$ and $M2$ and between $M1$ to $M3$. As a consequence of activating parasitic lateral NPN BJT's, the excess currents in substrate may be possibly coupled to the N-wells of transistor $M2$ and $M3$. The collected substrate currents (electrons) at N-well of a N-MOS transistor will lead to voltage drop of drain potential. Depending on their distances to aggressor ($M1$), the coupled currents at $M2$ and

M3 are different as well: $I_{sub_{M2}} < I_{sub_{M3}}$, since $d_{M1-M2} < d_{M1-M3}$. Thereby, the voltage drop at drain of transistor M2 is higher than of transistor M3. Such parasitic noises can cause several malfunctions of normal circuit operation, thus, the related effects should be predicted at the phase of post-layout simulation.

However, such effects of substrate parasitic can not be simulated in the conventional way. Simulation results in figure 6.19 show the sensed currents at the two branches of current mirror circuit. The results show the expected current mirror function, but not the correct behaviors in physical point of view. The missing part from simulation in the conventional way is due to the lack of modeling of parasitic lateral NPN BJTs.

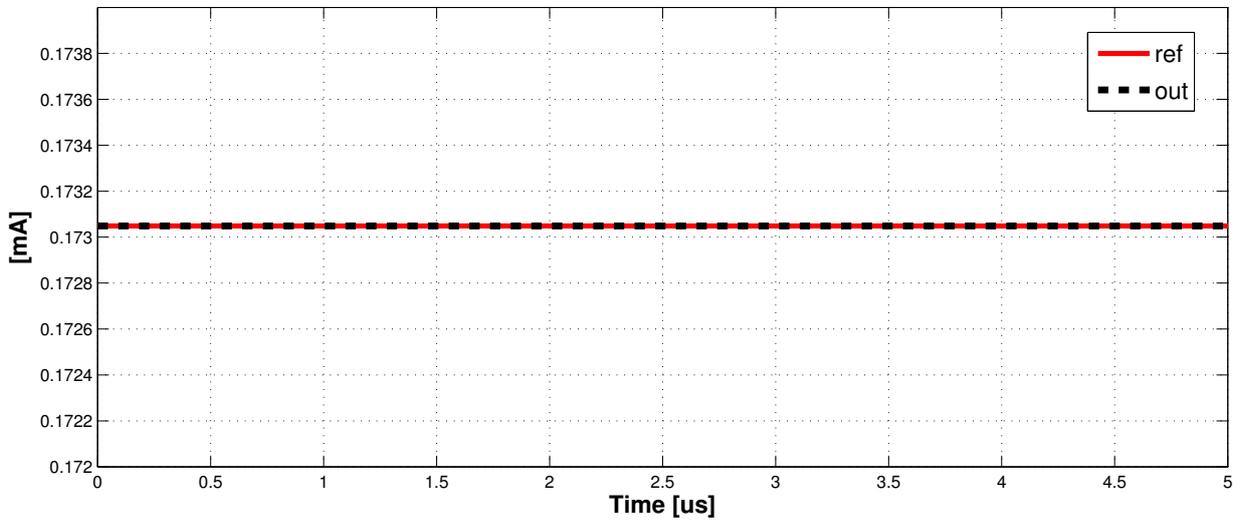


Figure 6.19: Sensed currents at current mirror circuit without substrate parasitic model.

In the following, we consider the same testbench, but with substrate parasitic model:

- In case 1 (figure 6.17a), transistor M2 is the source of current mirror who converts current into voltage. The voltage drop at drain of M2 (D2) causes the drop of controlling voltage at the gate of M2. Because the controlling voltage drops, the mirrored current at transistor M3 decreases. When voltage shifts, we have the currents changing at both branches of current mirror circuit, from the increase of coupled substrate current and the decrease of mirrored current at each branch. However, at transistor M3, the drop of mirrored current can not be compensated by the increase of coupled substrate currents, then the total current (I_{out} , black) decreases. On the contrary, at transistor M2, the total current (I_{Ref} , red) increases since the coupled substrate currents are more significant, as the curves shown in figure 6.20.
- In case 2 (figure 6.17b), transistor M3 is the source of current mirror. Since M3 is farther than M2 from the aggressor, the interference of substrate coupling to mirrored current is less important than in the case 1. As a consequence, the decrease of mirrored current caused by voltage drop at the drain of transistor M3 is less important than the coupled substrate

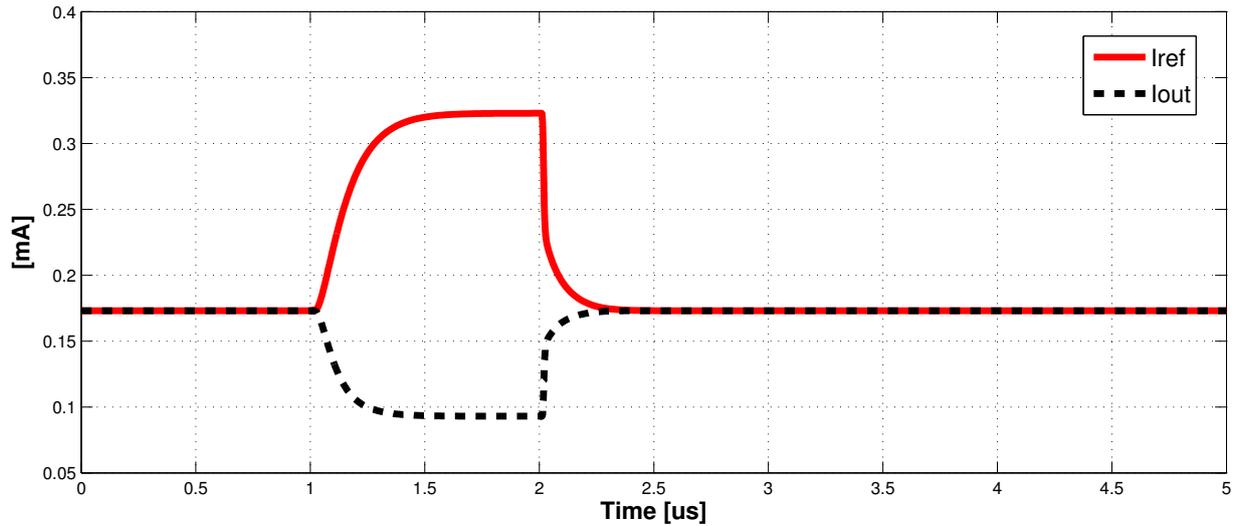


Figure 6.20: Sensed currents with substrate parasitic model in case 1 of figure 6.17a.

currents in both branches. As you can see in the figure 6.21, the total currents at M2 (I_{out} , black) and at M3 (I_{Ref} , red) are both increased, the differences are caused by the distances to M1.

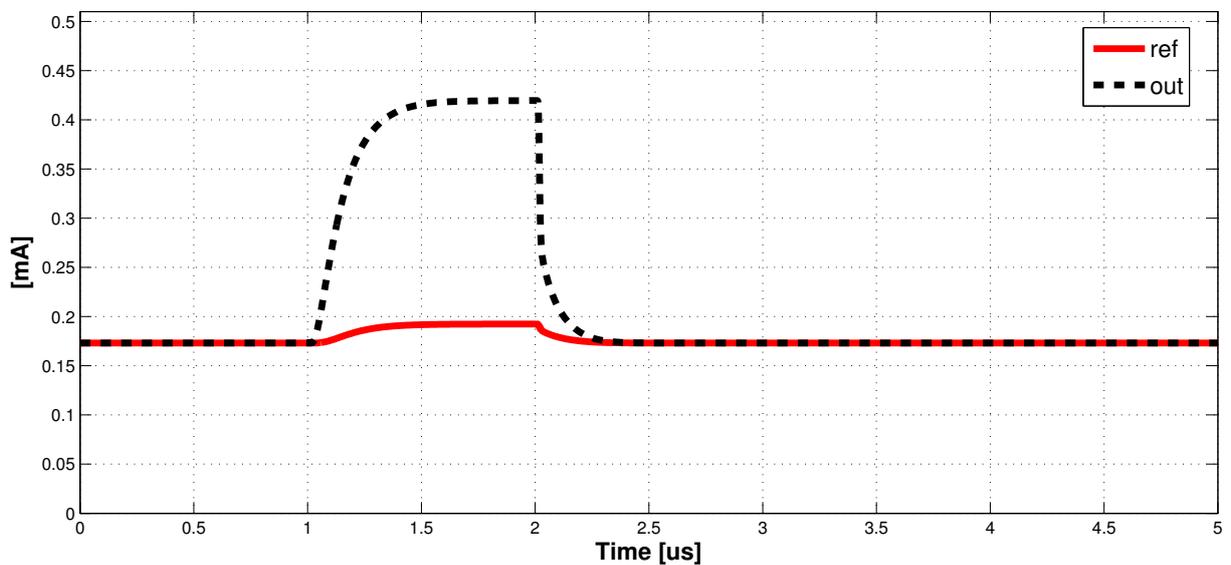


Figure 6.21: Sensed currents with substrate parasitic model in case 2 of figure 6.17b.

As conclusion of this test example, results of fast transient simulation confirm the correct behaviors of substrate currents as we expected. The interferences of substrate noises are caused by the activation of substrate parasitic lateral NPN BJTs. The impact on a basic current mirror circuit are clearly observed by using our 3-D substrate extraction tool. The lack of modeling for parasitic NPN BJTs in the conventional way is considered the missing part for this kind of failure analysis.

6.5 Industrial Test Evaluation in HV-CMOS Technology

We now present an industrial test evaluation using an industrial design and fabricated test chip [44, 43, 41, 42]. In this section, an industrial automotive test case is considered as an example. A standard automotive ISO test signal is applied to the chip PAD where the investigation of substrate current injection through IO PAD is presented.



Figure 6.22: Test chip fabricated by *ams AG* ($0.35\mu\text{m}$ HV-CMOS), and the chosen test case

In figure 6.22, the principle structure under study is chosen from the layout, and has been extracted using our 3-D extraction tool. The resulting meshing of selected region is also depicted. Consequently, extraction of the whole region takes less than half a minute, the total number of nodes, the total number of extracted components and others information are reported in table 6.6. In figure 6.23, we illustrate the simplified structure related to our test example. The structure includes three important parts: one is the injection point of aggressor, it is an IO device with ESD (electrostatic discharge) projection that can sustain over-voltage up to 50V, and the other two are the N-type wells that have different distances to the aggressor.

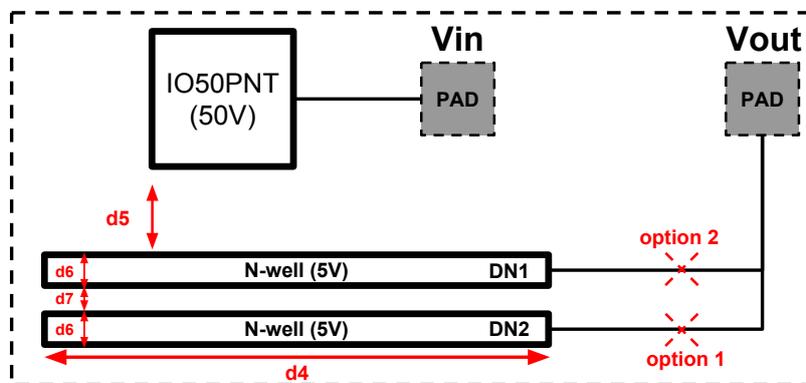


Figure 6.23: Illustration of a simplified structure of our test example.

The IO device consists of two series connected diodes supplied between the power supply (14V) and the ground. The injection PAD is between two diodes marked as “Vin” in figure 6.23. The two N-type wells with geometry $d4 \times d6$ each, are placed to collect the injected charges. The distance to the emitter is different as $d5$ for the closer placed one (DN1) and $d5 + d6 + d7$ for the second one (DN2). The output “Vout” is implemented as a PAD. In the layout, the two N-type wells are both connected to the “Vout” PAD. Laser cut options are used to connect or disconnect the different N-wells.

For the testbench, a standard automotive test signal (ISO 7637-2 Pulse 1) is applied to the PAD “Vin”, the behavior of this test signal is shown in figure 6.24. This test signal is an example of severe test signal requiring that the product remains fully functional while the output terminals are stressed with negative voltage. It simulates a negative polarity transient pulse caused by the disconnection of the DC supply through an inductive load. The peak voltage is varied as 6V, 12V and 20V for three different test cases. The recovery time is 2ms and the repetition rate is 500ms (not shown in figure 6.24).

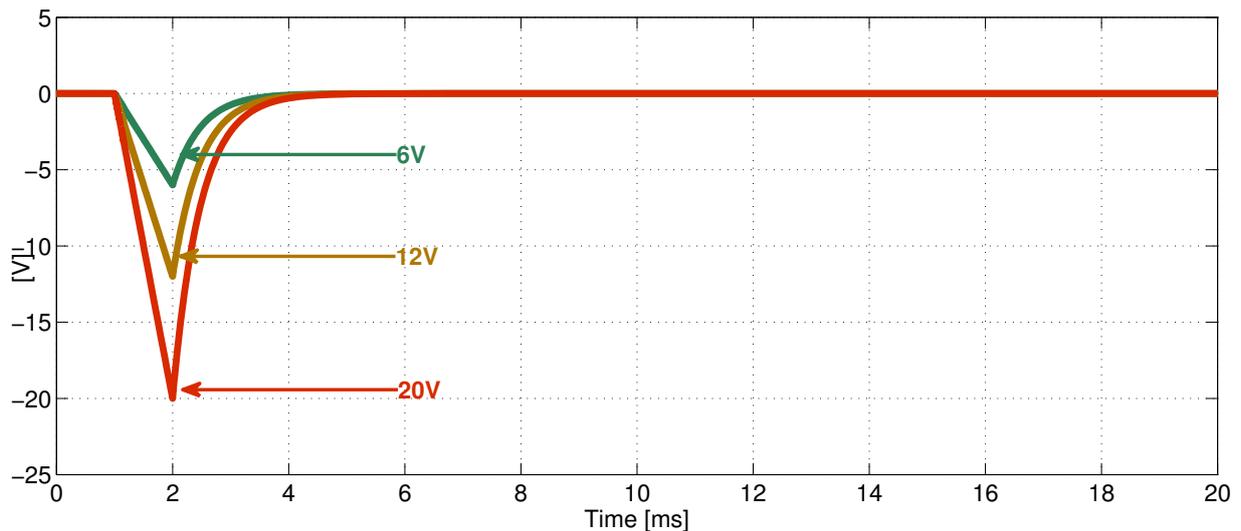
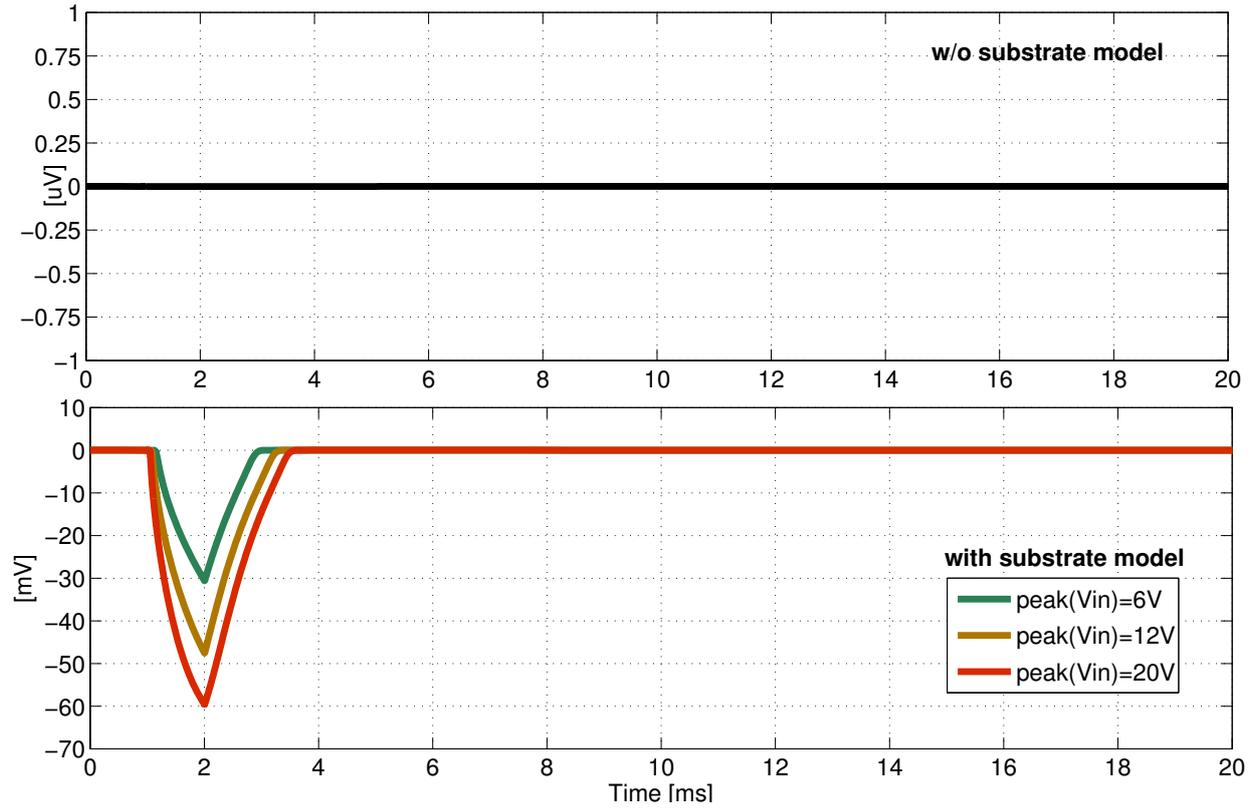


Figure 6.24: Inputs of automotive test signals, 3 pulse signals are applied in this case: as 6V, 12V and 20V peak voltage, respectively.

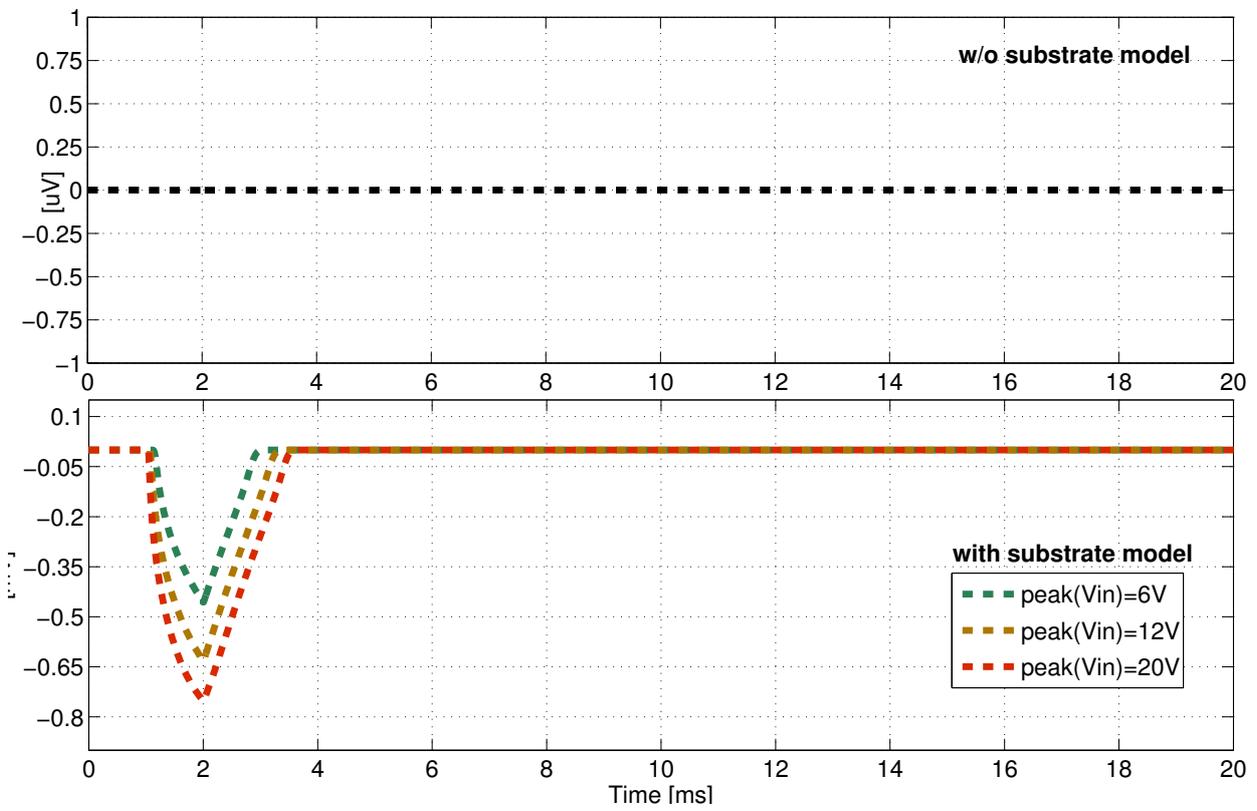
In this test example, spice-like simulations are performed. As for different input test signals, simulation will take less than 5 minutes for each, as reported in table 6.6. The voltage is sensed at the output measured on 50Ω .

On one hand, we consider this example as in the conventional way which our substrate model is not included in the circuit simulation. Black curves in figure 6.25 represent the sensed voltages at the “DN1” well (straight line) and the “DN2” well (dashed line). Without our substrate model, the effect of substrate noise injected from the IO PAD cannot be observed from simulation.

On the other hand, we consider our substrate model within circuit simulation. The colored



(a) Signals sensed at "DN1"



(b) Signals sensed at "DN2"

Figure 6.25: Sensed voltages at different N-type wells in case of different test signals.

Table 6.6: Results of proposed post-layout extraction and simulation.

| Test structures | | Current mirror | Test-chip 2 |
|---|---------------|----------------|-------------|
| Total number of nodes | | 871 | 6561 |
| Total number of components | | 1619 | 12291 |
| Substrate extraction | diode* | 304 | 2766 |
| | homojunction* | 261 | 807 |
| | resistor* | 1007 | 8193 |
| Extraction time (s) | | 16 | 20.82 |
| QRC extraction | diodes | 0 | 11 |
| | capacitor | 8 | 104 |
| | resistor | 27 | 286 |
| | BJT | 4 | 62 |
| | JFET | 8 | 62 |
| Simulation time (s) | | 14.2 | 295 |
| Components with * are enhanced parasitic models | | | |
| Work is performed with Intel Core i5-3470S Processor (2.9GHz) | | | |

curved in figure 6.25 represent the sensed voltages at the two different N-type wells: straight lines for the closed one, and the dashed lines for the other one. The colors of the curves are according to the different peak voltages at the input. As we expected, the simulation with our substrate model shows the correct behaviors of substrate noise coupling in the substrate. The collected noise due to minority carriers' propagation in the substrate leads to a local shift of substrate potential. This voltage drop at "DN1" can reach up to $-60mV$ which can be dangerous for automotive application. However, the conventional IC-CAD tool is not able to simulate the same behavior as we observed in real case.

To summarize, an industrial automotive test example was performed in this section. This example takes an industrial design and fabricated test chip of Smart Power technology. To investigate the substrate current injection in case of IO PAD with ESD protection, a standard automotive ISO test signal was applied in his example. The simulations are performed in two ways: with or without our substrate model. Results of simulation confirm that the behaviors can only be observed by using our substrate model. However, in the conventional way, the target design may still pass the automotive qualification tests even with this serious issue.

6.6 Process Integration for BCD Technology

High-voltage BCD technology has been invented in the year of 80s. This technology is a considerable complex silicon process, combining together the “Bipolar”, “CMOS” and “DMOS” technologies all in a same silicon die. In *STMicroelectronics*, this high-voltage technology continue to be developed from the first invention at 1984 (BCD1 at $4.0\mu\text{m}$ process node) to today’s technology (BCD10 at $0.09\mu\text{m}$ process node).

6.6.1 Silicon Structures Against Substrate Parasitic

To ensure the correct behavior of each individual device, transistor in high-voltage BCD technology should be electrically isolated to the others. Thereby, several isolation structures have been developed along with the development of BCD technologies, such as “junction isolation”, “shallow trench isolation” (STI), “deep trench isolation” (DTI), etc.

The DTI structure has been developed on the bulk substrate to minimize the leakage and reduce the amount of silicon defects. In figure 6.26, structure demonstrates the layout cross sectional view including DTI structure. The body of transistors are implanted in a heavy doped N+ buried layer that protect the device by junction isolation structure. Substrate noise coupling reduces to minimum between devices thanks to the described DTI structure.

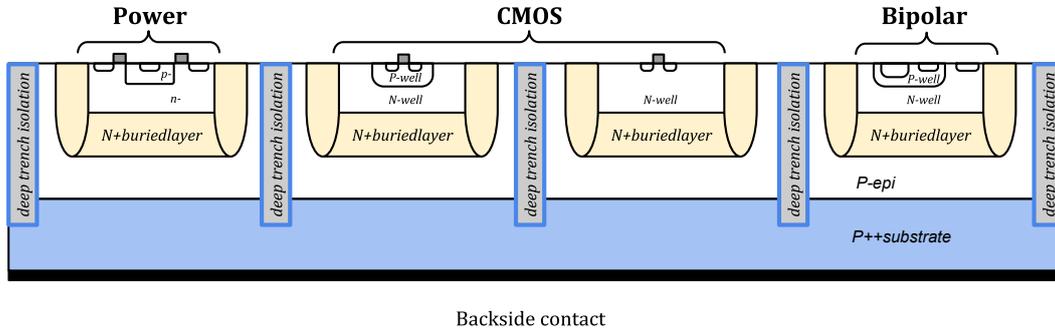


Figure 6.26: Illustration of simplified layout cross sectional view in BCD technology.

Besides deep trench isolation, designer may use N-type shielding structure in between the substrate current path, which wastes more silicon area but uses less expensive fabrication process. Moreover, it is less efficient to substrate parasitic immunity compared to DTI and increase the risk to silicon defects. Hence, the trade off between the cost and reliability is one of the factors to successes design in high-voltage BCD technology.

6.6.2 Our Modeling Approach in BCD Technology

In the following, we discuss the process integration of our modeling approach to the high-voltage BCD technology. In the framework of AUTOMICS project, we used the BCD8sAUTO ($0.16\mu\text{m}$

process node) of *STMicroelectronics* technology.

In such BCD technology, the possible substrate noise from HV device can be efficiently limited thanks to DTI structure. Because minority carriers' propagation in substrate are in 3-D, current injection into the substrate is still possible in vertical direction with forward biased substrate PN junction. Hence, the only possible way for minority carriers is through heavily doped P++ substrate region. This leakage current in substrate can be collected by backside contact or the other N-type buried layer structures, as illustrated in figure 6.27.

The above physical phenomena can be modeled in our modeling approach by adding a substrate equivalent parasitic model. To do so, we consider in BCD technology the N+ buried layer, the P-type epi layer, the heavily doped P++ region and the DTI structure. Figure 6.27 represent the equivalent substrate network in our modeling approach. Inside such substrate network, we suppose the N+ buried layer is the interface of our substrate model that should be connected to circuit devices. In addition, we define also the backside contact which is at the bottom slice of substrate network. As for the DTI, we consider it as an open circuit in our case.

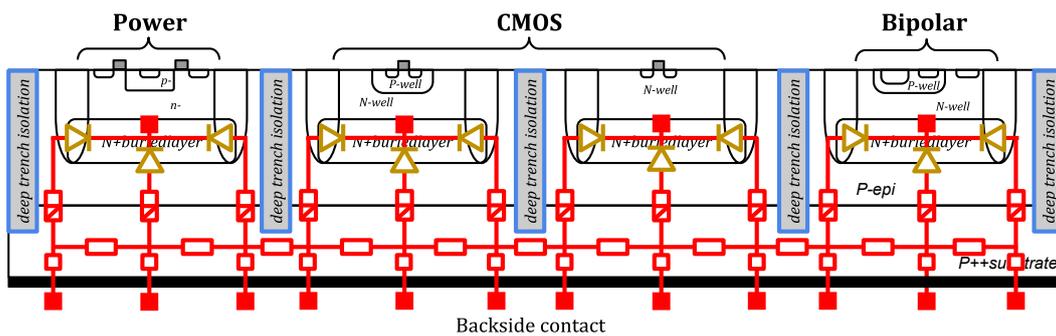


Figure 6.27: Substrate parasitic equivalent network that modeled by using our 3-D extraction tool.

Table 6.7: Possible combinations of the 3 materials and the corresponding parasitic models created for BCD8sAUTO technology of *STMicroelectronics*.

| | N+ buried layer | epi-substrate | P++substrate |
|-----------------|-----------------|---------------|--------------|
| P++substrate | N/A | H_{PP-PS} | R_{PP} |
| epi-substrate | D_{BU-PS} | R_{PS} | |
| N+ buried layer | R_{BU} | | |

Based on the describing structure, there are 3 kinds of materials contributing to create the parasitic component. Thereby, the possible parasitic models that can be extracted from our 3-D extraction tool are the following, as listed in table 6.7.

6.7 Model Benchmarking for BCD Technology

The objective in this section is to benchmark the substrate model for BCD technology, and the investigations of minority carriers propagation in such technology. In this work, we present the results of our investigations including deep trench isolation and/or N-type shielding structure. After the results of our investigation, we will see the advantages of adding more DTI structure to prevent the device from substrate noise, as well as the influence of N-type shielding structure compared to DTI structure.

To benchmark our substrate model, a test chip that designed and fabricated in BCD8sAUTO technology is provided by *STMicroelectronics-Italy*, as shown in figure 6.28.

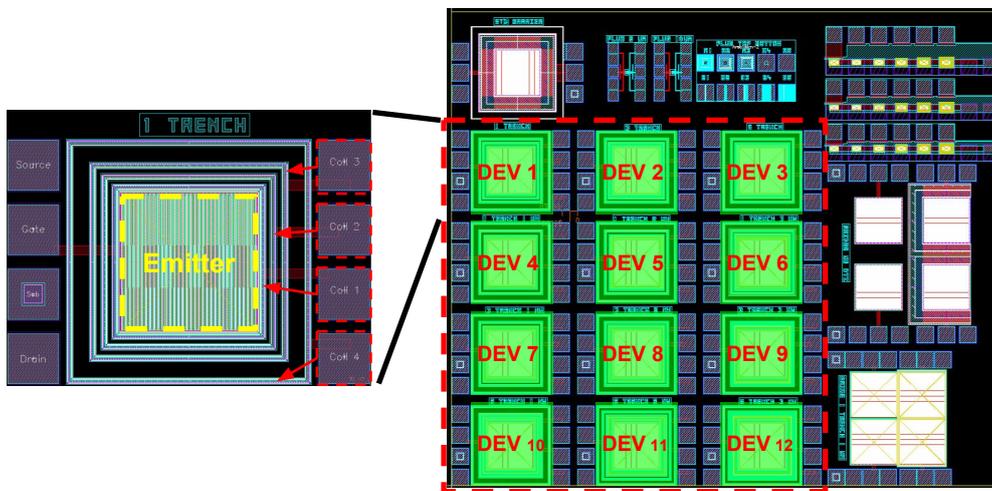


Figure 6.28: Test chip of benchmark structure in BCD8sAUTO technology of *STMicroelectronics-Italy*.

In this test chip, we have 12 benchmark devices, as shown in figure 6.28. Each one is an individual test structure consisting of one emitter and several collectors. The emitter is the rectangle device in the middle and the collectors are the surrounding N-type rings. The difference of each case is the isolation structure that are used in between the emitter and the closest collector. The proposed isolation structures are either DTI or N-type shielding well (floating structure).

In devices 1, 2 and 3, only DTI structure are used, to see the influence of substrate noise coupling by adding more DTI structures. Thereby, device 1 has only one “trench”, device 2 has 3 “trenches” and device 3 has 5 “trenches”. The “trench” is constructed by adding two “DTI” implants deep inside heavily doped P++ substrate. Moreover, adding “trenches” is done by inserting more “DTI” implants, as illustrated in figure 6.29.

In devices 4, 7 and 10, both DTI structure and N-type shielding well (NW) are used. These 3 devices have only one “trench” thus different “NWs”. In addition, device 4 has one “NW”, device 7 has 2 “NWs” and device 10 has 3 “NWs”. The “NW” is constructed in between two “DTI”

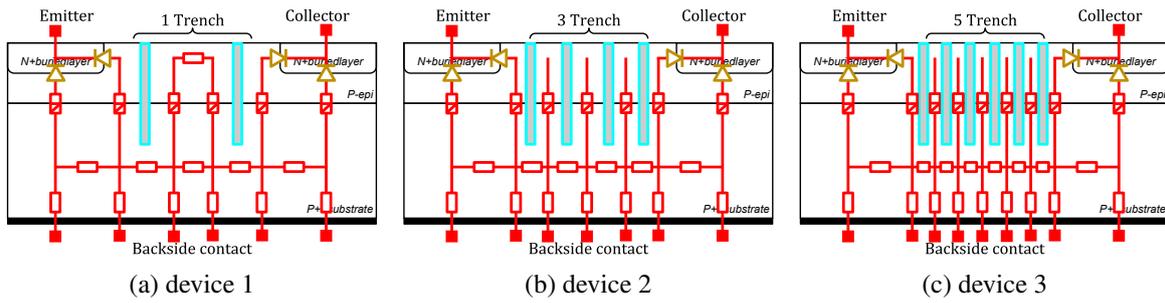


Figure 6.29: Illustration of layout cross sectional view of benchmark devices 1, 2, and 3 including deep trench isolation (DTI) structures, and their substrate equivalent networks.

implants, as illustrated in figure 6.30.

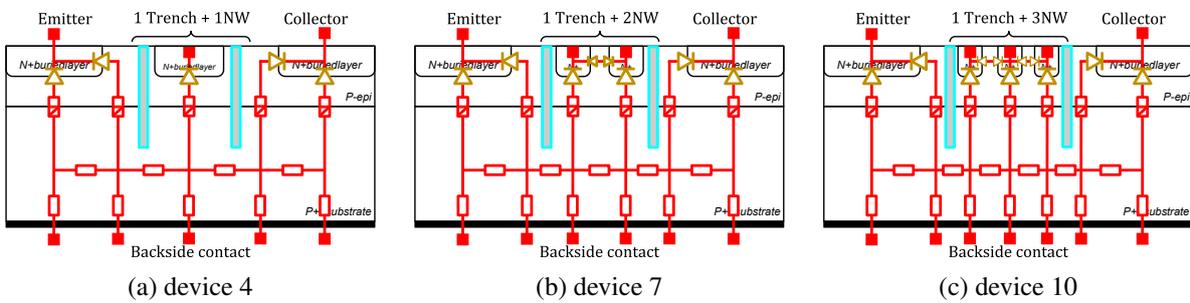


Figure 6.30: Illustration of layout cross sectional view of benchmark devices 4, 7, and 10 including one “trench” and different number of “NWs” structures, and their substrate equivalent networks.

As for the other devices in figure 6.28: devices in the same column have the same number of “trenches”, and devices in the same row have the same number of “NWs”. In the following subsections, investigations are done in two test cases:

- the first test case includes the first 3 devices having only “trenches”;
- the second test case includes the other 9 devices having both “trenches” and “NWs”.

Benchmark structures are extracted in our approach, as reported in table 6.8. Simulation for each benchmark device is performed by using spice-like simulator. Result of simulation is compared to measurement, and conclusions are drawn in the end of this section.

6.7.1 Benchmark 1: impact of the number of trenches

The first benchmark case includes 3 devices: “1”, “2” and “3”. To remind these structures, only “trenches” are involved in these devices with different number. The injecting point of substrate current is at the emitter, while the sensed point is the closed collector.

A DC current source is connected to emitter that is responsible for injecting minority carriers

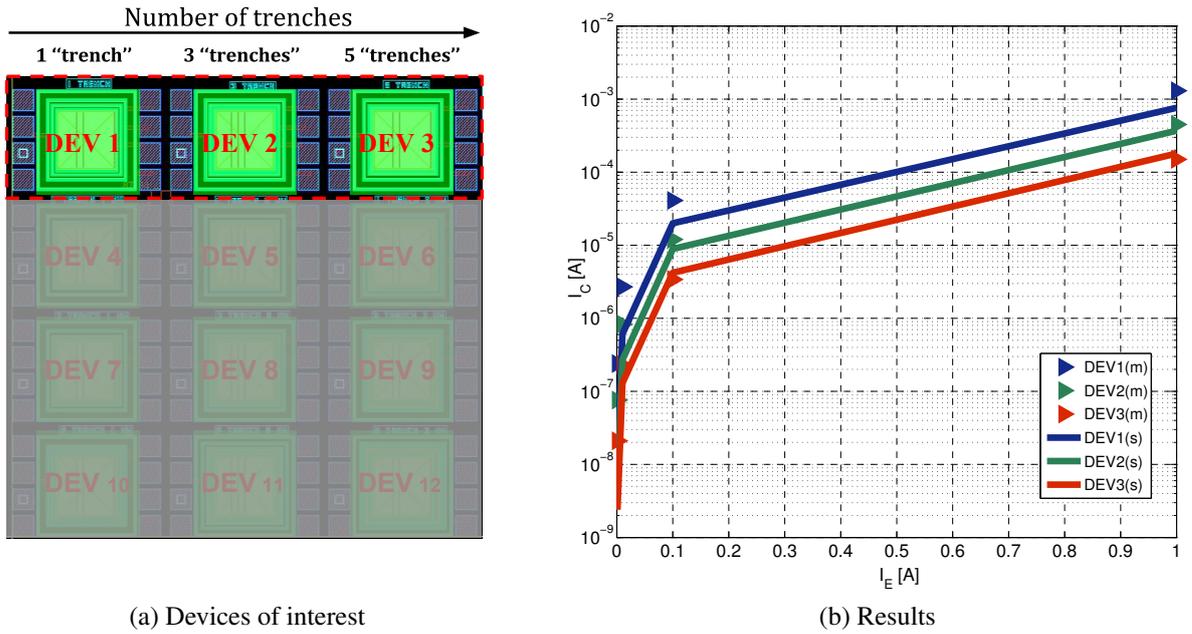


Figure 6.31: IV characteristics comparing the measured and simulated results.

into the substrate. To see the influence of substrate noise coupling, DC current source is applied to emitter at 1mA , 10mA , 100mA and 1A at room temperature. Result of measurement at the first collector of these devices are shown in figure 6.31, and represented by triangle symbol.

In our approach, the spice simulations with the same setup as the measurement are performed. Time cost for simulation is reported in table 6.8. Straight lines in figure 6.31 represent the one from simulations.

Results in figure 6.31 show that: On one hand, substrate noise can be efficiently limited by introducing the deep trench isolation structure. However it can still be significantly high (more than 1mA) with high current injection (1A), which may be dangerous for the sensitive low-voltage circuit. On the other hand, the induced noise due to minority carriers propagation in the substrate can be reduced by adding more DTI structure in between the possible substrate current path. Result of simulation and measurement both confirm this point, where the blue ones are with one “trench”, the green ones are with 3 “trenches” and the red ones are with 5 “trenches”.

6.7.2 Benchmark 2: impact of shielding structures and trenches

The second benchmark case includes 9 devices: from “4” to “12”. These devices have both “trenches” and “NWs” in between the emitter and the closed collector. We use in this test case the same testbench as the previous one, where the emitter is connected to a current source biased at different currents: 1mA , 10mA , 100mA and 1A .

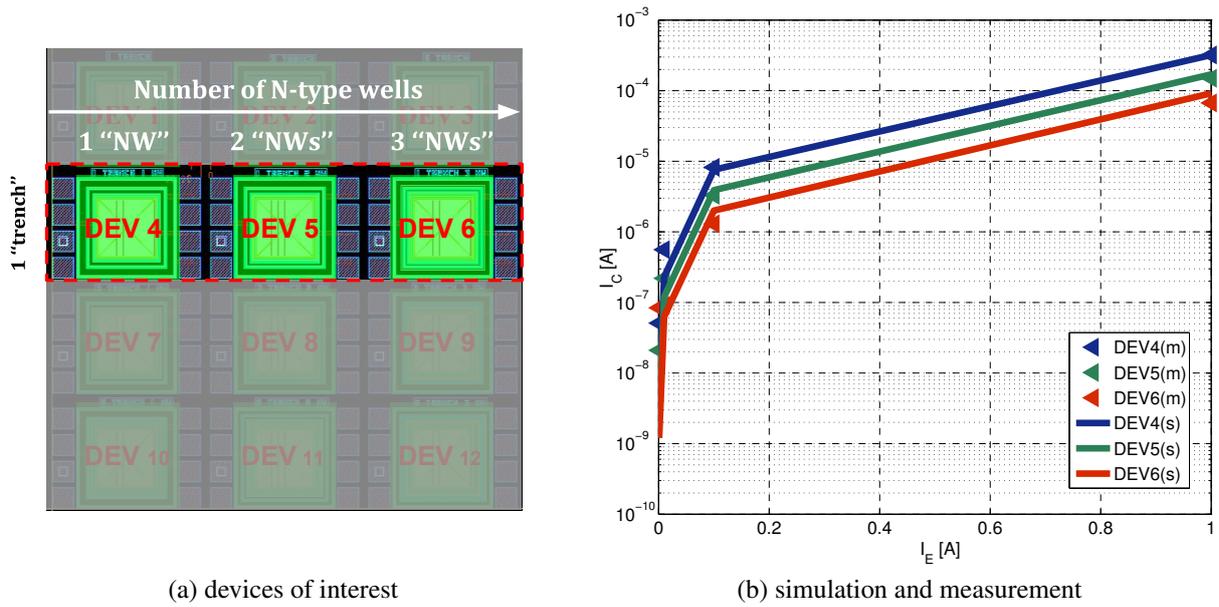


Figure 6.32: (a) Benchmark structures of interest: devices 4, 5 and 6, and (b) the results of simulation (straight lines) and measurement (triangle symbols) on DC current analysis.

On one hand, we consider only devices “4”, “5” and “6”, which have only one “trench” but increased number of “NWs”, as shown in figure 6.32a. As we expected, result of simulation (straight line) and measurement (triangle symbol) in figure 6.32b confirms that adding the N-type shielding wells can also decrease the substrate noise in BCD technology.

On the other hand, we consider only devices “4”, “7” and “10”, which have only one “NW” but increased number of “trenches”, as shown in figure 6.33a. As we have already observed in figure 6.31, “trenches” structures contribute to reduce the substrate noise and the impact will increase by adding more “trenches”. In addition, the induced substrate noise can be removed also by adding N-type shielding structure (comparing figure 6.31 with figure 6.33b).

From the results, both the simulation and measurement confirm the impact of substrate noise in the substrate of BCD technology, and the effects of silicon structures against substrate parasitic coupling. Hence, the N-type shielding structure has less efficiency than the deep trench isolation structure to protect the devices from substrate noise coupling.

To summarize, we have investigated in this test case the influence of minority carriers propagation in the substrate in BCD technology, where the deep trench isolation and the N-type shielding structure are applied. From the result of benchmarking, we have observed the correct behavior in simulation with respect to measurement with an acceptable error. The error comes from the simplification of modeling region where we only consider the buried layer and substrate underneath the body of transistors.

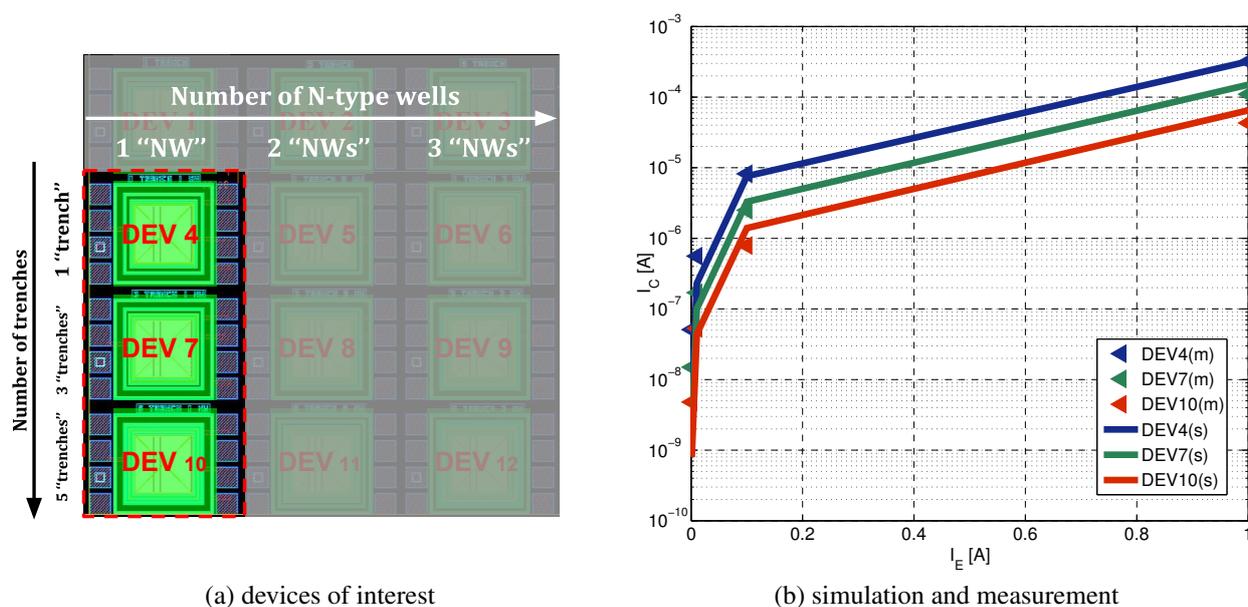


Figure 6.33: (a) Benchmark structures of interest: devices 4, 7 and 10, and (b) the results of simulation (straight lines) and measurement (triangle symbols) on DC current analysis.

Table 6.8: Results of substrate parasitic extraction and simulation for test chip in BCD8sAUTO technology of *STMicroelectronics-Italy*.

| | <i>nodes</i> | <i>diode*</i> | <i>homojunction*</i> | <i>resistor*</i> | Extraction time (s) | Simulation time (s) |
|-------|--------------|---------------|----------------------|------------------|---------------------|---------------------|
| DEV1 | 972 | 133 | 170 | 1197 | 1.88 | 31.3 |
| DEV2 | 1100 | 133 | 186 | 1357 | 2.66 | 23.6 |
| DEV3 | 1003 | 101 | 162 | 1237 | 2.25 | 20.2 |
| DEV4 | 972 | 133 | 170 | 1197 | 2.04 | 23.9 |
| DEV5 | 1132 | 165 | 202 | 1397 | 2.36 | 30.5 |
| DEV6 | 1292 | 197 | 234 | 1597 | 2.97 | 39.5 |
| DEV7 | 1100 | 133 | 186 | 1357 | 2.31 | 26.9 |
| DEV8 | 1260 | 165 | 218 | 1557 | 3.04 | 64.7 |
| DEV9 | 1420 | 197 | 250 | 1757 | 3.74 | 57.0 |
| DEV10 | 1228 | 133 | 202 | 1517 | 2.85 | 27.6 |
| DEV11 | 1388 | 165 | 234 | 1717 | 3.89 | 42.9 |
| DEV12 | 1549 | 197 | 266 | 1917 | 4.63 | 44.7 |

Components with * are enhanced EPFL parasitic components

Work is performed with Intel Core i5-3470S Processor (2.9GHz)

6.8 Conclusion

In this chapter, we explained how the proposed modeling approach applies for different technology processes: HV-CMOS technology of *ams AG* and BCD technology of *STMicroelectronics*. As of today, post-layout extraction from traditional low-voltage IC design tools can not model the parasitic lateral NPN BJT which cannot be neglected in HV and HT ICs of smart power technology. The induced electrons in substrate due to minority carrier propagation often disturb the functionality of circuit operation, may be destructive. The missing part from existing IC-CAD design flow has been illustrated in this chapter.

Parameter calibration ensures a good fitting between circuit simulation to real world behavior. In both, HV-CMOS technology and BCD technology, proposed modeling methodology provides an efficient solution to predict the parasitic substrate coupling in circuit simulation with an acceptable error. Investigations of parasitic coupling based on layout geometry have been done in HV-CMOS technology, key factors (distance, area, guard ring) influence parasitic coupling noises are found. Impact of deep trench isolation as well as shielding well in BCD technology have been modeled by our proposed approach.

Chapter 7

Conclusion

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7.1 Conclusion

The Smart Power ICs are extensively used in automotive embedded systems due to their unique capabilities to merge the low-voltage logic functions into high-voltage power ICs. On one hand, this integration leads to the reliability enhancement, chip size reduction and the overall cost saving. On the other hand, such integration brings up unwanted substrate parasitic coupling and causes circuit redesign. Yet, minority carriers' injection and propagation in the substrate can be significantly high in Smart Power IC, and become even worse at high operating temperature.

The lack of modeling for substrate parasitics is the major cause of failures, because this kind of noise is never fully under control by the designer since it cannot be simulated. First, designers adopt the conventional IC design flow to design Smart Power IC, however, the such design flow ignores the minority carriers related effects in the substrate. Second, minority carriers' propagation in the substrate cannot be modeled by using the standard compact models. Third, the impacts of minority carriers in the substrate are hard to model since they are layout dependent.

Facing these challenges, this Ph.D. thesis described the author's contributions to the development of dedicated methodology for substrate parasitics extraction and the investigation of minority carriers' propagation in Smart Power IC, as summarized in the following.

We have developed a methodology dedicated to substrate parasitics extraction. This methodology relies on a substrate meshing strategy in 3-D, which considers the layout and extract the substrate as a netlist in 3 phases. This netlist consists of many lumped components that extracted

from meshed substrate. The components are EPFL enhanced models which can handle minority carriers' propagation in the substrate. We extract the substrate parasitic components based on layout geometry. Besides geometry, components take technology parameters such as doping profiles as the required parameters.

We have proposed an enhanced mesh suitable for modeling substrate parasitics Firstly, optimization was done in 2-D surface. Secondly, strategy of meshing optimization was extended to 3-D. Thirdly, strategy of meshing considering subregions was provided. The optimization contributes to reduce the total number of elements, as well as extracted parasitic components. By using the proposed meshing technique, it is feasible to deal with more complex design in Smart Power technology.

The use of our tool completes the existing post-layout verification flow. The behaviors of substrate current can be also taken into account in simulation. In $0.35\mu\text{m}$ process node of *ams AG* HV-CMOS technology, we extracted the technology parameters of substrate model from various benchmark structures. We have investigated in this work the effect of parasitic lateral NPN BJTs in two different test cases: the interferences of substrate currents to a current mirror configuration was studied at first. Then, an automotive test case was included. This methodology was also applied to a HV BCD technology of *STMicroelectronics*. Investigations on deep trench isolation as well as shielding structures was discussed.

The proposed approach at post-layout stage gives the designers the possibility to simulate the substrate parasitic behaviors. The verification at early phase before fabrication enables the optimization of design against substrate coupling. Eventually, it contributes to reduce the design cycle thus increases the reliability and safety of smart power ICs.

7.2 Future Works

In this thesis, we have developed a CAD tool targeting to investigate the minority carriers related effects in substrate of Smart Power IC. As for the future works, the following points seem interesting to investigate:

- **Industrialization of CAD tool:** The development of substrate extraction tool should continue in order to meet the industrial standards. On the one hand, benchmarking of CAD tool requires more challenging test cases from industry. On the other hand, PDK integration should consider more advanced technology process, for instance, the $0.18\mu\text{m}$ process node.
- **Optimization of 3-D substrate network:** For a real Smart Power IC design consisting of more than hundred of devices, the meshing of such design may still need tenth thousand of components in the substrate. Optimization of meshing should take advices from designer. For instance, meshing should be optimized by focusing on the region where the power devices are located.

Appendices

Appendix A

List of publication:

Journal papers

Hao Zou, Yasser Moursy, Ramy Iskander, Alexander Steinmair, Heimo Gensinger, Ehrenfried Seebacher, Jean-Paul Chaput and Marie-Minerve Louërat, “Using CAD Tool for Substrate Parasitic Modeling in Smart Power Technology”, IEEE Transactions on Circuits and Systems I regular papers, December 2016.

Yasser Moursy, **Hao Zou**, Raouf Khalil, Ramy Iskander, Pierre Tisserand, Dieu-My Ton, Giuseppe Pasetti and Marie-Minerve Louërat, “Efficient Substrate Noise Coupling Verification and Failure Analysis Methodology for Smart Power ICs in Automotive Applications”, IEEE Transactions on Power Electronics, 2016.

Pietro Buccella, Camillo Stefanucci, **Hao Zou**, Yasser Moursy, Ramy Iskander, Jean-Michel Sallese and Maher Kayal, “Methodology for 3-D Substrate Network Extraction for Spice Simulation of Parasitic Currents in Smart Power ICs”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 29 December 2015.

International conferences

Hao, Zou, Yasser Moursy, Ramy Iskander, Jean-Paul Chaput and Marie-Minerve Louërat, “An Adaptive Mesh Refinement Strategy of Substrate Modeling for Smart Power ICs”, IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, Canada, May 2016.

Yasser Moursy, **Hao, Zou**, Ramy Iskander, Pierre Tisserand, Dieu-My Ton, Giuseppe Pasetti, Ehrenfried Seebacher, Alexander Steinmair, Thomas Gneiting and Heidrun Alius, “Towards Automatic Diagnosis of Minority Carriers Propagation Problems in HV/HT Automotive Smart Power ICs”, Design, Automation and Test in Europe Conference and Exhibition (DATE) conference, Dresde, Germany, 2016.

Hao, Zou, Yasser Moursy, Ramy Iskander, Camillo Stefanucci, Pietro Buccella, Maher Kayal and Jean-Michel Sallese, “Substrate Noise Modeling with Dedicated CAD Framework for Smart Power ICs”, IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, Portugal, May 2015.

Hao, Zou, Yasser Moursy, Ramy Iskander, Jean-Paul Chaput and Marie-Minerve Loueërat, “A Novel CAD Framework for Substrate Modeling”, 10th Conference on Ph.D Research in Microelectronics and electronics, Grenoble, France, 2014.

International workshops

Hao Zou, Yasser Moursy, Ramy Iskander, Jean-Paul Chaput, Marie-Minerve Loueërat, Camillo Stefanucci, Pietro Buccella, Maher Kayal, Jean-Michel Sallese, Thomas Gneiting, Heidrun Alius, Alexander Steinmair and Ehrenfried Seebacher, “A CAD Integrated Solution of Substrate Modeling for Industrial IC Design”, 20th International Mixed-Signal Testing Workshop (IMSTW), Paris, France, May 2015.

Camillo Stefanucci, Pietro Buccella, Yasser Moursy, **Hao Zou**, Ramy Iskander, Maher Kayal and Jean-Michel Sallese, “Substrate Modeling to Improve Reliability of High Voltage Technologies”, 20th International Mixed-Signal Testing Workshop (IMSTW), Paris, France, May 2015.

Book chapters

Yao Li, **Hao Zou**, Yasser Moursy, Ramy Iskander, Robert Sobot and Marie-Minerve Louërat, “Optimization and Co-Simulation of an Implantable Telemetry System by Linking System Models to Nonlinear Circuits”, accepted at Springer Book: “Computational Intelligence in Electronic Design” edited by Dr. Mourad Fakhfakh, Prof. Esteban Tlelo-Cuautle, and Prof. Patrick Siarry. The book is available in the 1st quarter of 2015.

Patent

Title: *Method for generating an electronic circuit modeling substrate coupling effects in an integrated circuit*, European patent application No. 15306016.5-1954, date of filing: 26 June 2015.

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