

### Recherche et évaluation d'une nouvelle architecture de transistor bipolaire à hétérojonction Si/SiGe pour la prochaine génération de technologie BiCMOS

van Tuan Vu

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SPÉCIALITÉ: ÉLECTRONIQUE

Par Van Tuan VU

## Recherche et Evaluation d'une Nouvelle Architecture de Transistor Bipolaire à Hétérojonction Si/SiGe pour la Prochaine Génération de Technologie BiCMOS

Soutenue le : 29 Novembre 2016

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#### DISSERTATION

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## THE DEGREE DOCTOR OF PHILOSOPHY AT UNIVERSITY OF BORDEAUX

#### DOCTORAL SCHOOL OF PHYSICAL SCIENCE AND ENGINEERING

SPECIALTY: ELECTRONICS

By Van Tuan VU

## Exploration and Evaluation of a Novel Si/SiGe Heterojunction Bipolar Transistor Architecture for Next BiCMOS Generation

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## Abstract

The ultimate objective of this thesis is to propose and evaluate a novel SiGe HBT architecture overcoming the limitation of the conventional Double-Polysilicon Self-Aligned (DPSA) architecture using Selective Epitaxial Growth (SEG). This architecture is designed to be compatible with the 28-nm Fully Depleted (FD) Silicon On Insulator (SOI) CMOS with a purpose to reach the objective of 400 GHz  $f_{\rm T}$  and 600 GHz  $f_{\rm MAX}$  performance in this node. In order to achieve this ambitious objective, several studies, including the exploration and comparison of different SiGe HBT architectures, 55-nm Si/SiGe BiCMOS TCAD calibration, Si/SiGe BiCMOS thermal budget study, investigating a novel architecture and its optimization, have been carried out. Both, the fabrication process and physical device models (incl. band gap narrowing, saturation velocity, high-field mobility, SRH recombination, impact ionization, distributed emitter resistance, self-heating and trap-assisted tunneling, as well as band-to-band tunneling), have been calibrated in the 55-nm Si/SiGe BiCMOS technology. Furthermore, investigations done on process thermal budget reduction show that a 370 GHz  $f_{\rm T}$  SiGe HBT can be achieved in 55nm assuming the modification of few process steps and the tuning of the bipolar vertical profile. Finally, the Fully Self-Aligned (FSA) SiGe HBT architecture using Selective Epitaxial Growth (SEG) and featuring an Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC) is chosen as the most promising candidate for the 28-nm FD-SOI BiCMOS generation. The optimization of this architecture results in interesting electrical performances such as 470 GHz  $f_{\rm T}$  and 870 GHz  $f_{\rm MAX}$  in this technology node.

**Keywords**: Hetero-junction bipolar transistors (HBTs), TCAD calibration, Thermal budget, 55-nm BiCMOS (BiCMOS055), 28-nm FD-SOI BiCMOS (BiCMOS028), Novel SiGe HBT architecture,

## Résumé

L'objectif principal de cette thèse est de proposer et d'évaluer une nouvelle architecture de Transistor Bipolaire à Héterojonction (TBH) Si/SiGe s'affranchissant des limitations de l'architecture conventionnelle DPSA-SEG (Double-Polysilicium Self-Aligned, Selective Epitaxial Growth) utilisée dans la technologie 55 nm Si/SiGe BiCMOS (BiCMOS055) de STMicroelectronics. Cette nouvelle architecture est conçue pour être compatible avec la technologie 28-nm FD-SOI (Fully Depleted Silicon On Insulator), avec pour objectif d'atteindre la performance de 400 GHz de  $f_T$  et 600 GHz de f<sub>MAX</sub> dans ce nœud. Pour atteindre cet objectif ambitieux, plusieurs études complémentaires ont été menées: 1/ l'exploration et la comparaison de différentes architectures de TBH SiGe, 2/ l'étalonnage TCAD en BiCMOS055, 3/ l'étude du budget thermique induit par la fabrication des technologies BiCMOS, et finalement 4/ l'étude d'une architecture innovante et son optimisation. Les procédés de fabrication ainsi que les modèles physiques (comprenant le rétrécissement de la bande interdite, la vitesse de saturation, la mobilité à fort champ, la recombinaison SRH, l'ionisation par impact, la résistance distribuée de l'émetteur, l'auto-échauffement ainsi que l'effet tunnel induit par piégeage des électrons), ont été étalonnés dans la technologie BiCMOS055. L'étude de l'impact du budget thermique sur les performances des TBH SiGe dans des nœuds CMOS avancés (jusqu'au 14 nm) montre que le  $f_{\rm T}$  maximum peut atteindre 370 GHz dans une prochaine génération où les profils verticaux du BiCMOS055 seraient 'simplement' adaptés à l'optimisation du budget thermique total. Enfin, l'architecture TBH SiGe EXBIC, prenant son nom d'une base extrinsèque épitaxiale isolée du collecteur, est choisie comme la candidate la plus prometteuse pour la prochaine génération de TBH dans une technologie BiCMOS FD-SOI dans un nœud 28 nm. L'optimisation en TCAD de cette architecture résulte en des performances électriques remarquables telles que 470 GHz f<sub>T</sub> et 870 GHz f<sub>MAX</sub> dans ce nœud technologique.

**Mots-clés**: Transistor bipolaire à hétérojonction (TBH), SiGe, TCAD, budget thermique, 55-nm BiC-MOS (BiCMOS055), 28-nm FD-SOI BiCMOS (BiCMOS028), terahertz.

## Abbreviations

B2B	Band-to-band tunneling
BGN	Band-gap narrowing
BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
BiCMOS028 or B28	STMicroelectronics 28-nm FD-SOI SiGe BiCMOS (under study)
BiCMOS055 or B55	STMicroelectronics 55-nm SiGe BiCMOS (in production)
BiCMOS8HP or 8HP	IBM/GF 30-nm SiGe BiCMOS
BiCMOS9HP or 9HP	IBM/GF 90-nm SiGe BiCMOS
BiCMOS9MW	STMicroelectronics 130-nm SiGe BiCMOS (in production)
BOX	Buried Oxide
$BV_{\rm CBO}$	A breakdown voltage in common base connection with the emitter in an
	open circuit configuration
BVCEO	A breakdown voltage in common emitter connection with the base in an
	open circuit configuration
$C_{\rm BC}$	Base-Collector Capacitance
$C_{\mathrm{EB}}$	Emitter-Base capacitance
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chemical Mechanical Polishing
DPSA-SEG	Double-Poly-Silicon Self-Aligned (DPSA) architecture using a Selective
	Epitaxial Growth (SEG)
DTI	Deep Trench Isolation
EBL	A SiGe HBT architecture featuring the selective Epitaxial Base-Link in
	conjunction with selective base epitaxy
EDX	Energy-Dispersive X-ray spectroscopy
EEB	A SiGe HBT architecture featuring the epitaxial Elevated External Base-
	contact with a non-selective base epitaxy
EXBIC	A novel fully self-aligned Si/SiGe HBT architecture using selective epi-
	taxial Growth and featuring an Epitaxial eXtrinsic Base Isolated from the
	Collector
FD-SOI	Fully Depleted Silicon on Insulator
$f_{MAX}$	Maximum oscillation frequency (Mason gain)
$f_{ m T}$	Transit frequency (H <sub>21</sub> gain)
FSA	Fully Self-Aligned
G1G	A fully self-aligned SiGe:C HBT architecture featuring a single-step epi-
	taxial collector-base process, that is simply called 'Growth in One Go',
	was designed in an IMEC-NXP cooperation
GHz	Gigahertz
HD	Hydrodynamic
$I_{\rm B}$	Base current
Ic	Collector current
	Emitter current
IFX	Infineon
ITRS	International Technology Roadmap for Semiconductors
HBT	Heterojunction Bipolar Transistor
LSA	Laser Spike Annealing
LE	Transistor length
MBE	Molecular Beam Epitaxy
mmwave	Millimeter Wave
NB	Neutral base
Polyreox	Poly-gate re-oxidation

QSA	Quasi Self-Aligned
R <sub>B</sub>	Base resistance
$R_{\rm BX}$	Extrinsic base resistance
R <sub>C</sub>	Collector resistance
$R_{\rm E}$	Emitter resistance
$R_{ m sBi}$	Intrinsic base sheet resistance
RF	Radio frequency
SA	Spike Annealing
SCR	Space Charge Regions
SEM	Scanning Electron Microscope
SIBL	A novel Sub-Isolation Buried Layer collector structure employed under
	the shallow trench isolation is used at Freescale
SIC	Selectively Implanted Collector
SiGe(:C)	Silicon Germanium Carbon
SIMS	Secondary Ion Mass Spectrometry
SOI	Silicon On Insulator
SSOFIT	The implementation of the Secondary Shallow Oxide Filled Isolation
	Trenches at IBM
ST	STMicroelectronics
STI	Shallow Trench Isolation
TAT	Trap-assisted tunneling
TEM	Transmission Electron Microscope
TEOS	Tetra Ethyl Ortho Silicate oxide
THz	Terahertz
W <sub>Bm</sub>	The metallurgical base width
$W_{\rm E}$	Emitter (finger) width

## **General introduction**

Since the first manufacturable 0.5  $\mu$ m SiGe HBT demonstrated on 200-mm wafer in 1994 [1], Si/SiGe BiCMOS technologies have gone through an impressive journey for more than 20 years. Several Si/SiGe BiCMOS technologies have been introduced [2] [3] [4] [5] [6]. The most advanced technologies in volume production today offer 0.18  $\mu$ m and 0.13  $\mu$ m CMOS nodes in which the 0.13  $\mu$ m technologies keep a strong foundation to address successfully several optical, wireless and wireline applications such as automotive radars, high bandwidth analog to digital converters, optical network and high-precision analog circuits. However, such applications incorporate more and more control circuits, digital signal processing and built-in test functions. Those require denser and faster CMOS transistors. Therefore, GLOBALFOUNDRIES (IBM) announced a 90-nm Si/SiGe BiCMOS (or BiCMOS9HP) technology in 2014 [7] and a 55-nm Si/SiGe BiCMOS (or BiCMOS055) technology [8] was introduced by STMicroelectronics (ST) in the same year. This technology was developed in ST's 300 mm wafer line offering a gate density more than 5 times larger than in 0.13  $\mu$ m technology and 2.5 to 3 times larger compared to 90-nm technology [9]. The integration of the SiGe HBT into the 55-nm CMOS node comes obviously with a higher complexity and big challenges have been overcome by Si/SiGe BiCMOS developers at ST.

Beside the Si/SiGe BiCMOS development, the SiGe HBT has also been studied and investigated in several publications in literature. On top of those, IHP announced the Elevated Extrinsic Base (EEB) architecture in 2010 [10] and Epitaxial Base Link (EBL) architecture in 2011 [11] both reaching 300 GHz  $f_T$  and 500 GHz  $f_{MAX}$  performances. Recently, the EEB architecture was optimized to catch the performance of 570 GHz  $f_{MAX}$  [6] in DOTSEVEN project\*. This architecture exhibits today the-state-of-the art of SiGe HBT performance. Obviously, the work done by IHP plays an important role in the Si/SiGe BiCMOS technology development.

Coming back to the Si/SiGe BiCMOS technology at ST, the introduction of BiCMOS055 exhibited the state-of-the-art of 320 GHz  $f_T$  and 370 GHz  $f_{MAX}$  by the integration of the conventional Double-Poly-Silicon Self-Aligned (DPSA) architecture using a Selective Epitaxial Growth (SEG) into the 55-nm CMOS node. The 370 GHz  $f_{MAX}$  reaches the BiCMOS055's objective but is not as high as the one aforementioned. This is primary due to a large extrinsic base resistance ( $R_{BX}$ ) [9] that is the main limitation of this architecture. Therefore, we decided to investigate a novel architecture in this thesis to keep ST at the forefront in the international competition when introducing the next Si/SiGe BiCMOS technology node.

This thesis, which embraces both, the advanced features of the 55-nm Si/SiGe BiCMOS technology and its transition to the 28-nm Fully Depleted (FD) Silicon-On-Insulator (SOI) BiCMOS technology, covers all the topics such as investigating new SiGe HBT architectures, TCAD calibration, investigating the impact of thermal budget during the fabrication process and the architecture as well as vertical profiles optimizations. The main content of this thesis is presented below.

The fundamental theory of the SiGe HBT is shortly summarized in chapter 1. Next, the review of existing Si/SiGe BiCMOS technologies is carried out. Finally, the advantages and limitations of each SiGe HBT architectures are clarified.

In chapter 2, we deepen the understanding of the SiGe HBT's physical models and give solutions to calibrate the TCAD tools for the simulation of the DPSA-SEG architecture in the 55-nm Si/SiGe BiCMOS [8]. The critical fabrication process steps including the SiGe:C epitaxy growth and the in-situ As doped emitter are calibrated in TCAD simulation to match vertical profiles with those obtained from secondary ion mass spectrometry (SIMS) (for As, Ge and B) and energy-dispersive X-ray spectroscopy (EDX) (for As and Ge) measurements. Moreover, a sensitivity analysis approach is employed to adjust some model parameters (including band-gap narrowing, saturation velocity, high-field mobility, SRH recombination, impact ionization, distributed emitter resistance, self-heating and trap-assisted tunneling as well as band-to-band tunneling) to figure out how physical models and related parameters impact the different electrical performances. Finally, an effective way to calibrate physical device models for SiGe HBT is illustrated and discussed in detail in this chapter.

In chapter 3, we focus on the thermal budgets and investigate how the different process steps impact the vertical doping profile. In the first part, a study of B55's thermal budget partitioning is carried out. The evolution of dopants' diffusion is investigated after each main process steps (incl.  $n^+$  buried layer, STI, DTI,  $n^+$  sinker, base epitaxy, poly-gate re-oxidation, CMOS's spacer formation and spike annealing) to clarify their respective impacts. Particularly, the poly-gate re-oxidation (Polyreox) and spike annealing thermal budgets are inspected. Finally, a roadmap, running parallel to the ITRS one [12], presents the performance of SiGe HBTs considering the impact of the thermal budget coming from advanced CMOS nodes (incl. 40-nm CMOS, 28-nm CMOS, 28-nm FD-SOI CMOS and 14-nm FD-SOI CMOS) is exhibited in this chapter.

In the final chapter, we propose a new type of SiGe HBT architecture classification and investigate a novel SiGe HBT architecture overcoming the limitations of the DPSA-SEG one. The novel fully self-aligned Si/SiGe HBT architecture using selective epitaxial growth and featuring an Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC) is chosen as the promising candidate for the next Si/SiGe BiCMOS generation. This architecture is designed to be compatible with the 28-nm FD-SOI CMOS (C28FD) technology available at ST and 400 GHz  $f_{T}$  and 600 GHz  $f_{MAX}$  are targeted in this technology node. In order to achieve this goal, the architecture is firstly evaluated and optimized by TCAD simulation before launching the fabrication process trials.

# Chapter 1 Silicon-Germanium het tion bipolar transistor

## heterojunc-

#### **1.1** History, the state-of-the-art and applications

Over decades, SiGe BiCMOS technologies have played an important role in semiconductor history and demonstrated usefulness and expediency in numerous high-speed applications including radio frequency (RF) transceivers, analog-to-digital converters, optical networking (amplifiers, clock data recovery, etc.), telecommunications networking (wireless backhaul), instrumentation and automotive radar (77-79 GHz) [13]. Today the technologies are gradually moving into the terahertz (THz) domain where a variety of new applications in biology and medical sciences (tumor recognition), security (drug and explosive detection), THz imaging, non-destructive control or high-speed communication (5G and beyond) are envisioned [14] (see Figure 1-1).



Figure 1-1. SiGe HBT applications

The invention of heterojunction bipolar transistor (HBT) in 1951 [15] was a significant milestone in the development of the SiGe HBT technology in which W. Shockley presented the theory of the combination of the wide bandgap Si emitter and the narrow bandgap germanium base to form the first SiGe HBT. Then the theoretical foundation of modern SiGe HBT was later refined by H. Kroemer in [16]- [17]. However, it had taken more than thirty years to bring the SiGe HBT from laboratory environment into commercial productions. The reason for this long delay was the inability to grow device quality epitaxial SiGe layers due to the lattice mismatch of 4.2% between Si and Ge. The first functional SiGe HBT was announced by IBM in 1987 [18]. The devices were fabricated by using Molecular Beam Epitaxy (MBE) with low-temperature processing and different Ge contents. Since then there have been a number of significant milestones in the measured performance of SiGe HBTs including the graded base SiGe HBT design with the first 75 GHz silicon bipolar transistor [19] and the first SiGe HBT technology entered commercial production on the 200-mm wafer in 1994 [1]. Since that time, IBM emerged as a pioneer in SiGe BiCMOS technology in the 2 later decades (see Figure 1-2 and Figure 1-3). The first 200 GHz  $f_{\rm T}$  and 280 GHz  $f_{\rm MAX}$  were achieved at IBM by integrating SiGe HBT module into the 0.13 µm CMOS node in 2003 [3], then IBM reached a new record of 300 GHz  $f_T$  and 350 GHz  $f_{MAX}$  in 2004 [20]. IBM's 90nm SiGe BiCMOS (9HP), which was announced in 2014, is the world's first 90-nm SiGe BiCMOS technology featuring 300 GHz  $f_T$  and 360 GHz  $f_{MAX}$  [7]. However, the leading SiGe HBTs performance has recently moved into Europe. This movement, which is clearly shown in the evolution of  $f_T$  and  $f_{MAX}$  performances in SiGe BiCMOS technologies (see Figure 1-2 and Figure 1-3), is primary due to an enormous effort and contribution from European SiGe HBTs community.

To establish a leadership position for the European semiconductor industry in the area of SiGe HBTs, they received a strong support from the European Commission through the 3 ambitious research projects including DOTFIVE [21], DOSEVEN [22] and RF2THZ SiSoC [23] to get SiGe HBTs reaching cutting-edge transit frequency ( $f_T$ ) and maximum oscillation frequency ( $f_{MAX}$ ). The target of 500 GHz  $f_{MAX}$  in the DOTFIVE was achieved by IHP in 2010 [10] and in 2011 [11]. The high  $f_{MAX}$  performance is primarily driven by the low extrinsic resistance ( $R_{BX}$ ) provided by the Elevated Extrinsic Base (EEB) and Epitaxial Base Link (EBL) architectures. Particularly, the 570 GHz  $f_{MAX}$  demonstrated in DOTSEVEN [6] by EEB architecture optimization is the state-of-the-art of SiGe HBTs performance at the moment. In the RF2THZ SiSoC project, a conventional Double-Poly-Silicon Self-Aligned (DPSA) architecture using a Selective Epitaxial Growth (SEG) of the base featuring 320 GHz  $f_T$  was successfully integrated into a 55-nm CMOS node [8] benefiting from both a reduced process thermal budget and the advanced patterning capability of a 300-mm wafer line [9].



Figure 1-2. Evolution of transit frequency  $(f_T)$  in SiGe BiCMOS technologies



Figure 1-3. Evolution of maximum oscillation frequency ( $f_{MAX}$ ) in SiGe BiCMOS technologies

Nowadays, SiGe HBTs technology is moving into the nanoscale era that is defined for technologies featuring CMOS nodes below 100 nm in which 28-nm Fully Depleted (FD) Silicon-On-Insulator (SOI) CMOS node is positively evaluated as a potential candidate to integrate the SiGe HBT module for the next generation [9].  $f_{T}$  and  $f_{MAX}$  performances are targeted to achieve 400 GHz and 600 GHz respectively, in this technology node at STMicroelectronics (ST) [24].

#### **1.2 Principle of the SiGe HBT**

Basically, bipolar junction transistor (BJT) and SiGe heterojunction bipolar transistor (HBT) employ two closely spaced *pn* junctions. It is an *npn* transistor if these junctions have a common p-type region, otherwise, it is a *pnp* transistor (see Figure 1-4. a and b). The three regions are known as an emitter, base and collector of the transistor in which the base terminal serves as a control electrode. The schematic diagram of 2D and 1D transistor as well as vertical doping profiles are illustrated in Figure 1-4 (*npn* transistor). The theoretical foundation of SiGe HBTs was initially presented in [16] and [17] by Kroemer, is well summarized in several books [25]- [26].



Figure 1-4. a) npn and pnp transistors, b) DPSA-SEG architecture is an example of the 2D SiGe HBT architecture,

c) 1D doping profile, d) Schematic diagram of 1D transistor including current distribution

To overcome the trade-off between current gain and base transit time [25], the Silicon homojunction was replaced by Si/SiGe heterojunction. In the one hand, we know that the Ge-induced band offsets (see Figure 1-5) at the emitter-base (EB) junction will exponentially enhance the collector current density resulting in the  $\beta$  improvement of a SiGe HBT compared to a comparably constructed Si BJT (see eq. 1-1 and 1-2).

$$J_{C,SiGe} = \frac{qD_{nb}n_{io}^2}{N_{\overline{ab}}W_b} \left( e^{\Delta E_{gb}^{app}/kT} e^{qV_{BE}/kT} - 1 \right) \left\{ \tilde{\gamma} \tilde{\eta} \frac{\Delta E_{g,Ge}(grade)}{kT} \frac{e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \right\},\tag{1-1}$$

$$\frac{\beta_{siGe}}{\beta_{si}}\Big|_{V_{BE}} = \frac{\tilde{\gamma}\tilde{\eta}\frac{\Delta E_{g,Ge}(grade)}{kT}e^{\Delta E_{g,Ge}(0)/kT}}{(1 - e^{-\Delta E_{g,Ge}(grade)/kT})}, [27]$$
(1-2)

Where  $J_{C,SiGe}$  is the collector current density,  $V_{BE}$  is the base-emitter voltage,  $\Delta E_{gb}^{app}$  is the apparent bandgap narrowing induced by heavy doping,  $\Delta E_{g,Ge}(x)$  is the Ge-induced bandgap offset at position x inside the base, and  $\Delta E_{g,Ge}(\text{grade}) = \Delta E_{g,Ge}(w_B) - \Delta E_{g,Ge}(0)$ .  $D_{nb}$  is the minority carrier diffusion constant in the base,  $\tilde{\gamma}$  is the effective density of states ratio between SiGe and Si, and  $\tilde{\eta}$  is the minority carrier diffusion ratio between SiGe and Si. To ensure a fair comparison, the  $\beta_{SiGe}/\beta_{Si}|_{V_{BE}}$  ratio is considered by a constructed SiGe HBT and Si BJT with identical emitter contact. It is further assumed that the Ge profile on the EB side of the neutral base does not extend into the emitter in order to assure the same base current density as well as the base current  $(J_B)$  should be comparable between the two devices.

From a technological point of view, we have introduced a new degree of freedom. In fact, in order to decrease the base transit time, the standard approach is to decrease the neutral base width. Doing so, we are increasing the base resistance resulting in a decrease of  $f_{MAX}$ . The base resistance can be controlled by the doping, but increasing the doping in order to avoid the increase of  $R_B$  results in a decrease of the current gain. Thus, all these parameters are linked together in a vicious circle. This circle has been broken by the introduction of the heterojunction because the current gain is controlled mainly by the ratio of the Ge content at the BE-junction and not only by the ratio of emitter doping / base doping. We can now decrease the base width to gain speed, increase the base doping in order to control  $f_{MAX}$  without losing the current gain.



Figure 1-5. Schematic base bandgap in a linearly graded SiGe HBT [27]

In addition, the introduction of a graded Ge profile into the base creates a built-in electric field that will accelerate the injected electrons across the base. The base transit time is reduced (see in detail in section 1.3.1), hence an improved transit frequency ( $f_T$ ) is obtained.



Figure 1-6. Energy band diagram for a Si BJT and a graded-base SiGe HBT, both biased in forward active mode at low injection [27]

Furthermore, the presence of Ge content in the CB junction will impact positively the output conductance of the transistor, yielding higher Early voltage ( $V_A$ ). The ratio between a SiGe HBT and a Si BJT is an exponential function of Ge-induced bandgap grading across the neutral base (see eq. 1-3).

$$\frac{V_{A,SiGe}}{V_A}\Big|_{V_{BE}} \approx e^{\Delta E_{g,Ge}(grade)/kT} \left[\frac{1 - e^{\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT}\right] [27]$$
(1-3)

#### **1.3 Figures-of-Merit**

For high-frequency AC operation, SiGe HBTs are often assessed according to three figuresof-merits. The first is well known as the unity gain cut-off frequency  $f_T$ . The second is the maximum oscillation frequency  $f_{MAX}$ . The collector-emitter break-down voltage ( $BV_{CEO}$ ) and  $f_T$  trade-off (or the Johnson limit) is known as the final one.

#### **1.3.1** Transit frequency $(f_T)$

 $f_{\rm T}$  is one of the most important high-frequency parameters for a bipolar transistor and is defined as a frequency at which the gain of the bipolar transistor drops to unity [25]. The  $f_{\rm T}$  represents an important figure-of-merit and gives information about the quality of the vertical doping profile of the transistor. The  $f_{\rm T}$  is expressed as a function of the emitter-to-collector transit time ( $\tau_{EC}$ ) (see eq. 1-4) which physically relates to the total delay time for the minority carriers traveling from emitter to collector.

$$f_T = \frac{1}{2\pi\tau_{EC}},\tag{1-4}$$

$$\tau_{EC} = \tau_F + \tau_j + \mathcal{C}_{BC}(R_E + R_C) = \tau_E + \tau_{EB} + \tau_B + \tau_{BC} + \frac{kT}{qI_C}(\mathcal{C}_{BE} + \mathcal{C}_{BC}) + \mathcal{C}_{BC}(R_E + R_C), (1-5)$$

$$\tau_F = \tau_E + \tau_{EB} + \tau_B + \tau_{BC}, \tau_j = \frac{kT}{qI_C} (C_{BE} + C_{BC})$$
(1-6)

Where the forward transit time  $(\tau_F)$  is the sum of the individual delay times in the various region of the transistor, including the transit time related to the excess minority carrier charge in the neutral emitter ( $\tau_E$ ), the emitter / base depletion region ( $\tau_{EB}$ ), the base ( $\tau_B$ ) and the collector / base ( $\tau_{BC}$ ) depletion region.  $C_{BC}$ ,  $C_{BE}$ ,  $R_E$  and  $R_C$  are respectively base-collector and base-emitter capacitances, emitter and collector resistances. The most significant delay time contributor is the base transit time ( $\tau_B$ ) which depends on the square of the neutral base width as well as reciprocally on the amount of Ge-induced bandgap grading across the neutral base (see eq. 1-7).

$$\tau_{B,SIGe} = \frac{W_b^2}{\overline{D_{nb}}} \frac{kT}{\Delta E_{g,Ge}(grade)} \left\{ 1 - \frac{kT}{\Delta E_{g,Ge}(grade)} \left[ 1 - e^{-\Delta E_{g,Ge}(grade)/kT} \right] \right\} [28], \tag{1-7}$$

By combining (1-4) and (1-5), the  $f_{\rm T}$  can be formulated as

$$f_T = \frac{1}{2\pi(\tau_F + \frac{kT}{ql_C}(C_{BE} + C_{BC}) + C_{BC}(R_E + R_C))}$$
(1-8)

From equation (1-6),  $\tau_j$  depends reciprocally to the collector current and being a dominant term at the low collector current ( $I_C$ ), hence  $f_T$  tends to increase with an increase in  $I_C$ . However, the influence of  $\tau_j$  reduces drastically when the  $I_C$  moves into the range of high current, the dominant terms are replaced by  $\tau_B$  and  $\tau_{BC}$  at peak  $f_T$ .

#### **1.3.2** Maximum oscillation frequency (*f*<sub>MAX</sub>)

Another important high-frequency parameter for a bipolar transistor is the maximum oscillation frequency ( $f_{MAX}$ ). This is defined as the frequency at which the unilateral power gain of a bipolar transistor drops to unity [25].  $f_{MAX}$  is expressed as an approximation of the function of  $f_T$  and total components of  $C_{BC}$  and  $R_B$  in which parasitic components are included, and given by

$$f_{MAX} \approx \sqrt{\frac{f_T}{8\pi R_B C_{BC}}} \tag{1-9}$$

Obviously,  $f_{MAX}$  represents a figure-of-merit that depends not only on the intrinsic transistor but also the parasitic components related to the SiGe HBT architecture.

#### 1.3.3 Breakdown voltages and Johnson limit

In bipolar transistors, the breakdown voltage depends on how the bipolar transistor is connected in the circuit.  $BV_{CBO}$  is a breakdown voltage in common base connection with the emitter open while  $BV_{CEO}$  is known as a breakdown voltage in common emitter connection with the base in an open circuit configuration (see Figure 1-7). The  $BV_{CEO}$  determines the maximum supply voltage that can be applied between the collector and emitter. The value is limited by two different reverse bias junction breakdown mechanisms including Zener and avalanche. The former occurs when both sides of a junction have high dopant concentrations. The latter is recognized when a large electric field appears across the depletion region causing an impact ionization and generation of electron-hole pairs. The value of  $BV_{CEO}$  can be determined when the breakdown occurs (see eq. 1-10).

$$\frac{\alpha}{1 - \left(\frac{BV_{CEO}}{BV_{CBO}}\right)^n} = 1 \iff BV_{CEO} = BV_{CBO}(1 - \alpha)^{1/n} = \frac{BV_{CBO}}{\beta^{1/n}}, [25]$$
(1-10)

Where  $\alpha$  is the common base current gain,  $\beta$  is the comment emitter current gain and *n* takes a value between 3 and 6.



Figure 1-7. Breakdown voltage  $BV_{\text{CEO}}$  and saturation  $I_{\text{CEO}}$  for common-emitter open-base configuration, and breakdown voltage  $BV_{\text{CBO}}$  and current  $I_{\text{CBO}}$  for common-base open-emitter configuration

From the standpoint of circuit design, breakdown voltages and transit time frequency ( $f_{\rm T}$ ) performance are recognized as significant characteristics. When breakdown voltage is considered, the well-known trade-off relationship known as the Johnson limit comes into play. This trade-off can be basically understood that a high  $f_{\rm T}$  requires a large transfer current density and therefore a high collector doping with the consequence of a strongly reduced  $BV_{\rm CEO}$ . Although the Johnson limit has been defeated by the modern technology but the existence of such a trade-off is still a challenge for technology developer. In fact, advanced device structures raise  $f_{\rm T} \times BV_{\rm CEO}$  product from 200 GHzV to more than 500 GHzV. However,  $BV_{\rm CEO}$  is dropped to less than 1.7 V for  $f_{\rm T}$  of greater than 300 GHz (see Figure 1-8).



Figure 1-8. Dependence of cut-off frequency  $f_{\rm T}$  on the collector-emitter breakdown voltage  $BV_{\rm CE0}$ 

#### **1.4** Review of SiGe HBT architectures on bulk substrate

#### 1.4.1 FREESCALE-NXP

Freescale has developed its SiGe HBT technology for 15 years. The  $f_T$  and  $f_{MAX}$  performances have been continuously improved through the BiCMOS generations as shown in Figure 1-9. The starting point for the SiGe HBT technology at Freescale was an established 0.18-µm BiCMOS platform, designed for wireless radio frequency (RF) application in 2001 [29]. A quasi-self-aligned architecture was used with a non-selective Si/SiGe:C/Si epitaxial base layer (see Figure 1-10. a). This architecture was known as a very simple structure but has a very large parasitic capacitance and resistance due to the non-self-alignment of the emitter and the extrinsic base. Therefore, a self-aligned structure featuring selective Si/SiGe:C epitaxial base were designed at Freescale in 2006 [30].



Figure 1-9. Evolution of  $f_T$  and  $f_{MAX}$  performances in Freescale SiGe BiCMOS technologies

Figure 1-10. b illustrates the self-aligned structure for "xHBT" device which was integrated into 0.18-µm CMOS node. A novel sub-isolation buried layer (SIBL) collector structure employed under the shallow trench isolation was introduced into the architecture. High dose  $n^+$  is implanted into the bottom of the etched shallow trenches before completion of a conventional STI module [31]. The fabrication process of the SIBL is illustrated in Figure 1-11. The SIBL enables to reduce the collector resistance while avoiding the more expensive buried layer / epitaxy plus deep trench isolation (DTI). The implementation of the SIBL module allows for a 60% reduction in collector resistance ( $R_C$ ) compared to a high-energy (deep) n-well, leading to improve 20% of RF performance [31].



Figure 1-10. Illustration of a) Quasi-self-aligned structure, b) Fully-self-aligned structure



Figure 1-11. SIBL collector structure implementation

In order to enhance  $f_T$  and  $f_{MAX}$  performances, more aggressive layout rules aided by advanced photolithography has enabled a shrink of the SiGe HBT emitter / base structure to improve layout parasitic for high  $f_{MAX}$  in "xHBT2" [32]. Moreover the optimization of the SiGe:C base and the collector doping was applied to increase the intrinsic device performance for higher  $f_T$ . Therefore,  $f_T$  and  $f_{MAX}$  achieved 260 GHz and 350 GHz respectively. By employing the significant scaling of the SiGe HBT, more aggressive layout rules and advanced photolithography, NXP introduced a 90nm BiCMOS technology with a SiGe:C HBT archiving 230 GHz  $f_T$  and 400 GHz  $f_{MAX}$  in 2016 [33] (see TABLE 1-1).

SiGe HBT	Units	HBT	eHBT	<b>xHBT</b> [31]	<b>xHBT2</b> [32]	HBT [33]
$W_{\rm E}$	nm	250	250	150	125	100
Current gain $(\beta)$	-	120	360	550	1500	700
R <sub>BI</sub>	kΩ/sq	1.8	4.8	3.1	3.4	3.1
BVCEO	V	3.3	1.8	1.9	1.5	1.7
$f_{ m T}$	GHz	50	120	200	260	230
<i>f</i> <sub>MAX</sub>	GHz	110	120	280	350	400

TABLE 1-1. Comparison of SiGe BiCMOS electrical performances at Freescale

#### **1.4.2 HITACHI**

A conventional DPSA-SEG architecture has been developed for more than 15 years at Hitachi. The transistor featuring a BEC layout with the STI between the internal base and the collector contact areas is shown in Figure 1-12. In general, the DPSA-SEG architecture is well known. It is the most popular and simplest fully self-aligned structure with advanced features such as the STI separating between the base and the collector is used to reduce the parasitic base-collector capacitance ( $C_{BC}$ ), the DTI feature is not only utilized for bipolar collector-substrate capacitance ( $C_{CS}$ ) reduction, but, also under the passive elements to reduce the substrate coupling. However, the large  $R_{BX}$  and the  $R_{BX}-C_{BC}$  trade-off are easily recognized as the disadvantages of this architecture. It is different from the DPSA-SEG architecture demonstrated at ST (see in detail in section 3.2), the pedestal formation at Hitachi includes  $SiO_2/Si_3N_4$  stacked layers (see Figure 1-13. b), while the only  $SiO_2$  layer is deposited at ST. Another difference is the in-situ phosphorus doped poly-silicon emitter (the in-situ arsenic doped emitter is used at Infineon (IFX) and ST).

In order to enhance the electrical performances, several techniques were applied at Hitachi [34]. It is noted that the separation length of the STI dividing the collector plug and the intrinsic base region ( $L_{CB}$ ) (see Figure 1-13. a) was shrunk to reduce the collector resistance ( $R_C$ ), hence  $f_T$  increase was obtained. As a consequence, the best 253 GHz  $f_T$  and 325 GHz  $f_{MAX}$  were achieved at Hitachi in 2014 [34]. The evolution of the SiGe HBTs performances is shown in Figure 1-14.



Figure 1-12. SEM cross-sectional view of 0.18 µm based SiGe HBT [35]



Figure 1-13. a) Schematic cross section of SiGe HBT b) Process flow for making SiGe base region and emitter-base separation wall as self-aligned structure [34]



Figure 1-14. Evolution of  $f_{\rm T}$  and  $f_{\rm MAX}$  performances in Hitachi SiGe BiCMOS technologies

#### 1.4.3 IBM-GLOBALFOUNDRIES

From the first SiGe HBT technology entered commercial in production on 200-mm wafers in 1994 [36], IBM was always a pioneer in SiGe BiCMOS technology in two last decades. IBM was the first company achieving 200 GHz  $f_T$  and 280 GHz  $f_{MAX}$  that was successfully integrated with 0.13 µm foundry-compatible CMOS node in BiCMOS8HP [3], and reached 300 GHz  $f_T$  and 350 GHz  $f_{MAX}$ in 2004 [20]. Actually, the SiGe HBT architecture using the non-selective growth (NSEG) of the base featuring an advanced concept of raised extrinsic base (see Figure 1-16) is a central element for these achievements. In 2014, a novel fully self-aligned architecture using the NSEG and featuring a silicon link region between the intrinsic base and extrinsic base was integrated into the 90-nm CMOS node.  $f_T$  and  $f_{MAX}$  reached 300 GHz and 360 GHz respectively. The evolution of performances in IBM SiGe BiCMOS technologies is illustrated in Figure 1-15.



Figure 1-15. Evolution of f<sub>T</sub> and f<sub>MAX</sub> performances in IBM SiGe BiCMOS technologies

#### 1.4.3.1 BiCMOS8HP

Figure 1-16 depicts the SiGe HBT architecture used in BiCMOS8HP. This architecture is well known with FSA structure using the NSEG of the base and featuring a raised  $p^+$  doped extrinsic base. The process integration begins with a conventional collector module (N buried / epitaxy / DTI) formation. A significant structural improvement is the implementation of the raised  $p^+$  doped extrinsic base self-aligned to the emitter, which allows the reduction of parasitic base resistance ( $R_B$ ). Extrinsic base resistance ( $R_{BX}$ ) can be further improved by reducing the spacing between the raised extrinsic base silicide and the emitter. However, when the high boron-doped extrinsic base is close to the emitter, boron diffusion from the extrinsic base into the intrinsic collector (see Figure 1-17. a) driven by the emitter formation and CMOS thermal budgets is the main reason that accounts for the  $C_{BC}$  degradation.



Figure 1-16. a) Cross-section of a raised extrinsic base SiGe HBT, b) SEM photo [37]

In an effort to maximize SiGe HBT performances, the scaling strategy (lateral and vertical scaling) was employed at IBM. Typically, the millisecond anneal (MSA) and low temperature NiSi contact techniques show an effective way in reducing the base resistance to yield a 40 GHz improvement in  $f_{MAX}$ , without a significant degradation in  $f_T$ . In addition, the implementation of the secondary shallow oxide filled isolation trenches (SSOFIT) in the active device periphery (see Figure 1-17. b), which can reduce the  $C_{BC}$  while maintaining the low  $R_B$  due to the high doped-boron extrinsic base, results in 20 GHz improvement in  $f_{MAX}$ . As a consequence,  $f_T$  and  $f_{MAX}$  can achieve 300 GHz and 420 GHz respectively [38]. By taking full advantage of the MSA technique, the modified trenches (incl. SSOFIT) and low thermal budgets of the 90nm CMOS node, IBM introduced the 90 nm BiCMOS technology which achieved 285 GHz  $f_T$  and 475 GHz  $f_{MAX}$  [39]. However, the introduction of the SSOFIT, which is not self-aligned with the emitter, leads to a modification of the existing fabrication process and implements more masks in the production line. Therefore a novel architecture was introduced in BiCMOS9HP [7].



Figure 1-17. a) Simulated nominal NPN device b) Schematic cross-section of SiGe NPN device with the implementation of the SSOFIT [38]

#### 1.4.3.2 BiCMOS9HP

Figure 1-18 is a cross-section of the 9HP HBT architecture which is the FSA structure using the NSEG of the base and is integrated into a 90-nm CMOS node. After non-selective epitaxial growth of the intrinsic base, an oxide / p+ poly-silicon / dielectric stack is formed. The emitter opening is patterned and following formation of an inner sidewall the base is undercut and an epitaxial growth forms the link between the intrinsic and extrinsic base. The fabrication process continues with the emitter formation. A significant structural improvement is the link between extrinsic and intrinsic base. The extrinsic base can be doped as large as possible to reduce parasitic base resistance while boron diffusion from extrinsic base into intrinsic collector is controlled by the width of the undercut oxide layer (see Figure 1-18. b). The formation of extrinsic base after and before the in-situ doped

emitter presents a main difference between 8HP and 9HP respectively.  $f_T$  and  $f_{MAX}$  performances reached 300 GHz and 360 GHz respectively, in this node.



Figure 1-18. a) Cross-section of the BiCMOS9HP architecture, b) TEM photo [7]

#### 1.4.4 Infineon (IFX)

The development of IFX SiGe BiCMOS technology can be divided into two time periods: before DOTSEVEN and during DOTSEVEN projects. Only the DPSA-SEG architecture was developed and optimized for a long-term before the DOTSEVEN project.  $f_T$  and  $f_{MAX}$  achieved 230 GHz and 350 GHz respectively, in 2010 [40]. But during the DOTSEVEN project, on the one hand, this architecture was continuously optimized to reach 250 GHz  $f_T$  and 370 GHz  $f_{MAX}$  in B11HFC [6]. On the other hand, IFX has a cooperation with IHP in DOTSEVEN, the epitaxial base link (EBL) architecture from IHP was integrated into 130-nm CMOS node at IFX. Benefiting from the low base link resistance of EBL architecture,  $f_{MAX}$  performance has recently achieved 500 GHz in this cooperation [41]. The evolution of  $f_T$  and  $f_{MAX}$  performances in IFX SiGe HBTs is shown in Figure 1-19.



Figure 1-19. Evolution of  $f_{\rm T}$  and  $f_{\rm MAX}$  performances in IFX SiGe HBTs

#### 1.4.4.1 B7HF200-B11HFC

The DPSA-SEG architecture, which was designed at IFX since 2000 [42], was originally coming from Siemens AG [43]. The fabrication process flow of the one is close to BiCMOS055 developed at ST (see in detail in section 3.2). However the fabrication process exhibits some differences between them. The SIC is completed by one mask right after the bipolar area patterning in ST, while the inner nitride spacers formed after the emitter window opening are applied in IFX to reduce the width of the window before implantation. Another difference concerns the nitride sidewalls protecting the poly-base from base epitaxy that are also removed after the epitaxy in IFX but still kept in

ST process and become therefore part of the emitter-base inside spacer's formation. The best  $f_T$  and  $f_{MAX}$  performances achieved 250 GHz  $f_T$  and 370 GHz  $f_{MAX}$  in 2015 [6].



Figure 1-20. a) Cross-section of DPSA-SEG architecture at IFX, b) TEM photo [44]

#### 1.4.4.2 IFX-IHP

In the DOTSEVEN project, the epitaxial base link (EBL) architecture (see Figure 1-21) has demonstrated the performance potential under industrial conditions realized through a cooperation between IFX and IHP. This SiGe HBT module was implemented in IFX's 0.13µm BiCMOS environment. In contrast to the EBL process described in [45] using the implanted collector module, this fabrication process was begun in IFX with a conventional collector module including the buried layer, the DTI and the STI. Then the EBL module (see section 1.4.5.2) was fabricated at IHP. Finally the backend process was completed at IFX using the standard 6 layer Cu metallization including Al pads as well as passives like TaN meal resistor and MIM capacitors. This architecture is known with advanced features such as low  $C_{BC}$ , low  $R_{BX}$  (monocrystalline base link). The best performances achieved 300 GHz  $f_{T}$  and 500 GHz  $f_{MAX}$  in 2015 [41].



Figure 1-21. a) Cross-section of EBL architecture, b) TEM photo [41]

#### 1.4.5 IHP

IHP has emerged as a leading  $f_{MAX}$  performance in SiGe BiCMOS technology since 2010. They achieved 500 GHz  $f_{MAX}$  in DOTFIVE [10] and even 570 GHz in DOTSEVEN [6] by optimizing the elevated extrinsic base (EEB) architecture. Simultaneously, IHP is also well known for developing the EBL architecture that achieved 300 GHz  $f_T$  and 500 GHz  $f_{MAX}$  too [44] and is ongoing to optimize the architecture in a cooperation with IFX. The evolution of  $f_T$  and  $f_{MAX}$  performances in IHP SiGe HBTs is shown in Figure 1-22.



Figure 1-22. Evolution of  $f_{T}$  and  $f_{MAX}$  performances in IHP SiGe HBTs

#### 1.4.5.1 Elevated extrinsic base (EEB) architecture

The self-aligned emitter-base architecture using the NSEG of the base and featuring the elevated extrinsic base (EEB) is shown in Figure 1-23. Key features are listed as following:

- The formation of EEB regions is self-aligned to the emitter. The low  $R_{\rm BX}$  compared to the conventional DPSA-SEG architecture is obtained. It is primary due to a mono-crystalline base link formation (Figure 1-23. b)
- The formation of the high-speed HBT device in a single active area without shallow trench isolation (STI) between emitter and collector contacting regions resulting in low  $R_{\rm C}$  and small collector-substrate junction areas. However, normalized  $C_{\rm BC}$  and  $R_{\rm C}$  of this architecture are still 1.2 and 2.7 times greater than those obtained from the conventional DPSA-SEG at ST [44].

Based on these advanced features, this architecture exhibited the state-of-the-art of 570 GHz  $f_{MAX}$  performance in 2015 [6].



Figure 1-23. a) Cross-section of EEB architecture at IHP, b) TEM photo [46]

#### 1.4.5.2 Lateral base link (EBL) architecture

Figure 1-24 shows two types of the lateral base link architectures that were developed at IHP. The key feature of these HBT modules is a connection of the extrinsic and intrinsic base regions by lateral epitaxial overgrowth.

- Type 1 : Lateral base link is formed before the in-situ As doped emitter (see Figure 1-24. a)
- Type 2 : Epitaxial base link is formed after the in-situ As doped emitter (see Figure 1-24. b)

In type 1, the HBT fabrication requires three lithographic steps defining the collector well, emitter window and emitter patterning (see Figure 1-24. a). The fabrication starts with the implanted collector formation. Pedestal oxide / poly-base (in-situ boron doped extrinsic base) / nitride stack layers are deposited. Then the emitter window is opened by etching through these stacks. Subsequently, nitride sidewalls are deposited to protect the poly-base while the pedestal oxide layer is removed by wet etching. Then, a Si buffer layer is grown selectively followed by a self-aligned collector implantation (SIC). To create a link between the extrinsic base and intrinsic base, the nitride sidewalls are partially removed. The B-doped SiGe:C base layer is grown selectively and the intrinsic and extrinsic base are connected during the process. Next, the sacrificial nitride layer is etched back laterally to produce the overlap of the T-shaped emitter (see Figure 1-24. a-3). After that, the spacers and the deposition of the in-situ As-doped emitter layer are formed, a CMP step is used to remove this layer outside of the HBT regions. As a conclusion, the architecture opens an interesting idea whose uses the lateral base link between extrinsic base. But the architecture encounters some limitations in the fabrication.

- To open the lateral link areas between poly-bases and the intrinsic collector, the protected nitrides are partially removed. This critical step is controlled by etching time, hence this step is limited under the industrial fabrication condition.
- The complexity of base link formation during the B-doped SiGe:C layer results in faceting at the base link (see Figure 1-24. a). Large  $R_B$  is obtained. Even if the architecture was optimized in [47], the normalized  $R_B$  of this architecture was not better than a conventional DPSA-SEG architecture.



- Using of CMP after the emitter formation results in the complexity of the fabrication process.

Figure 1-24. a) Base link formation before the in-situ As doped emitter [45], b) base link formation after the in-situ As doped emitter [11]

In order to overcome these limitations, IHP developed the EBL architecture in 2011 [11]. The poly-base layer is replaced by a sacrificial layer in the EBL structure (see Figure 1-24. b). Hence the formation of B-doped SiGe:C epitaxy and emitter module are simplified. The extrinsic base is formed by the in-situ B-doped epitaxy. The base link allows combining a very low  $R_B$  with a lower  $C_{BC}$  compared to the conventional DPSA-SEG architectures [11].  $f_T$  and  $f_{MAX}$  performances achieved 310 and 480 GHz respectively. The optimization of this architecture is ongoing in the cooperation between IHP and IFX.



Figure 1-25. TEM photo of lateral base link architectures a) type 1, b) type 2 [47]

#### 1.4.6 IMEC

A low complexity single poly quasi-self-aligned (QSA) structure with the non-selective epitaxial growth (NSEG) was developed for a long time at IMEC [48] [49]. The main limitation of this architecture is the lack of scalability, high parasitic values and the difficulty to minimize simultaneously the external  $C_{BC}$  and the  $R_{B}$ . In order to further improve the  $f_{MAX}$ , the fabrication process and layout rules were modified to aim at a reduction of the device parasitic resistance and capacitance values. These modifications have gathered considerable interests. In the one hand, airgap deep trenches were introduced in 2006, the conventional oxide / polysilicon trench filling was replaced by airgap encapsulated in an oxide plug (see Figure 1-26. a). By this way, the peripheral collector-substrate capacitance ( $C_{cs, p}$ ) was reduced by 82% [50]. In the other hand, the  $C_{BC}$  and  $R_B$  tradeoff were handled by implementing lateral oxide filled cavities (see Figure 1-26. b) to decouple between the extrinsic base and the collector. As a consequence, this implementation did not impact the  $R_{\rm B}$ , while  $C_{\rm BC}$  was reduced by 15% [51]. In order to introduce these lateral oxide layers, the fabrication process is modified as in Figure 1-27. After processing the heavily doped arsenic sub-collector, a lowly-doped collector epitaxial region is grown, in which a 15 nm thick Si<sub>0.75</sub>Ge<sub>0.25</sub> layer is integrated. The shallow trenches are etched through this layer and the lateral cavities are created (see Figure 1-26. b). After a filling of STI, these cavities are completely filled by oxide [51].



Figure 1-26. a) QSA-NSEG with air gaps DTI [50], b) QSA-NSEG with oxide filled cavities [51]



Figure 1-27. Overview of the cavity processing: a) after STI etch, b) after cavity etch and c) after shallow trench filling and polishing [51]

Both the air gaps deep trenches and lateral oxide filled cavities were integrated into the QSA-NSEG structure, but the best  $f_{\rm T}$  and  $f_{\rm MAX}$  performances of 210/290 GHz were only achieved [51] that were far away from 500 GHz (target of DOTFIVE). Therefore, a fully self-aligned SiGe:C HBT architecture featuring a single-step epitaxial collector-base process, that is simply called 'Growth in One Go' (G1G), was designed in an IMEC-NXP cooperation in 2007 [52]. The fabrication process is illustrated in Figure 1-28. The key concept of the architecture is based on the growth of the collectorbase region in one single epitaxial step. The removal of the external device regions using a sacrificial emitter pedestal and the self-aligned reconstruction of the base contacts using oxide/poly deposition and CMP planarization techniques enable the independent reduction of the  $R_{\rm B}$  and  $C_{\rm BC}$ . Figure 1-28. b shows the effective emitter width of 80 nm [53]; the lateral base link can also reduce the boron diffusion from the extrinsic base into the intrinsic collector resulting in low  $C_{\rm BC}$ . Since,  $f_{\rm T}$  and  $f_{\rm MAX}$ could achieve 245/460 GHz in [54]. Evolution of  $f_{\rm T}$  and  $f_{\rm MAX}$  performances in IMEC SiGe BiCMOS technologies is shown in Figure 1-29. However, the architecture involves some limitations in production:

- Self-aligned extrinsic base and emitter
- Using CMP planarization technique (see Figure 1-28. a-2) leads to an increased complexity of the fabrication process



- The total height of the device is also a concern for integration in CMOS.

Figure 1-28. a) Fabrication process steps of G1G architecture, b) TEM photo [55]



Figure 1-29. Evolution of  $f_T$  and  $f_{MAX}$  performances in IMEC SiGe BiCMOS technologies

#### 1.4.7 STMICROELECTRONICS (ST)

The DPSA-SEG architecture, which is well-known with the most popular and simplest fully self-aligned structure, has gathered glorious records of electrical performances obtained in different companies (ST, IFX and Hitachi). The first ST's SiGe BiCMOS technology using the DPSA-SEG, which was BiCMOS9MW [4] into a 0.13- $\mu$ m CMOS node, achieved very promising performances of 230 GHz  $f_T$  and 280 GHz  $f_{MAX}$ . The cross-section of a transistor featuring a standard CBEBC layout is shown in Figure 1-30. The record of 410 GHz  $f_T$  was held at ST [56], only overtaken recently [46]. Even more, the architecture exhibited the state-of-the-art performances of 320 GHz  $f_T$  and 370 GHz  $f_{MAX}$  in the 55-nm SiGe BiCMOS [8]. The evolution of  $f_T$  and  $f_{MAX}$  performances in ST SiGe BiCMOS technologies is shown in Figure 1-31.



Figure 1-30. TEM cross-section of an HBT in BiCMOS055 [57]

As the leading company in the integration of the SiGe HBT module into the nanoscale era of denser and faster CMOS nodes, syntheses of the SiGe HBT architectures presented in [44] and [57] were demonstrated by concentrating on the impact of the constraints of nanoscale CMOS technologies [9]. A DPSA-SEG architecture with the implanted collector and the removal of the STI between the base and the collector contact, which was integrated into 55-nm CMOS node, was thoroughly evaluated at ST [9]. The 330 GHz  $f_{T}$  was obtained but the exhibition of a 350 GHz  $f_{MAX}$  is not as high as targeted. It is primary due to a large  $R_{BX}$  [9] that is the main limitation of this architecture. Therefore, several novel Si/SiGe HBT architectures overcoming this limitation are proposed in this thesis (see in detail in section 4.4). One of the best proposals is the FSA-SEG architecture featuring an Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC) [24]. This architecture is intended
to be integrated into the 28-nm FDSOI CMOS technology available at ST and targeted to further achieve 400 GHz  $f_{T}$  and 600 GHz  $f_{MAX}$  in this node.



Figure 1-31. Evolution of  $f_{T}$  and  $f_{MAX}$  performances in ST SiGe BiCMOS technologies

#### 1.4.8 TOWERJAZZ

The FSA-NSEG architecture was designed at TowerJazz to be compatible with 180-nm CMOS node in 2001 [58] (see Figure 1-32). Key attributes include low buried layer resistance (high-dose implant and growth of an epitaxial layer), low collector-substrate capacitance (deep trench iso-lation), scalable emitter width with self-aligned base link implants and low-resistance in-situ doped emitter. One of the main limitation of this architecture is the use of the implanted extrinsic base. The boron can diffuse into the collector during this implantation, hence can degrade the electrical performances. Moreover, the boron diffusion can also lead to a transient enhanced diffusion (TED) of boron in the base.

The fabrication process flow starts with the formation of the buried layer including highdose implant and silicon epitaxy. Both an oxide filled shallow trench and a polysilicon filled deep trench are then formed. After the base of NPN region is opened, a non-selective SiGe deposition is performed to form both the intrinsic epitaxial base and the extrinsic polycrystalline base. A sacrificial emitter is used to self-align the extrinsic base and the emitter (see Figure 1-32. a). Next, the sacrificial one is removed and replaced by the in-situ As doped emitter. The final spike annealing and cobalt silicidation complete the front-end process flow. The best performances of the architecture achieved 240 GHz  $f_T$  and 280 GHz  $f_{MAX}$  in 2012 [59]. Evolution of  $f_T$  and  $f_{MAX}$  performances in Towerjazz SiGe BiCMOS technologies is shown in Figure 1-33.



Figure 1-32. a) Cross-section of the FSA-NSEG architecture at TowerJazz b) TEM photo [60]



Figure 1-33. Evolution of  $f_{T}$  and  $f_{MAX}$  performances in Towerjazz SiGe BiCMOS technologies

# **1.5** Review of SiGe HBT architectures on SOI substrate

SiGe HBTs on Silicon-On-Insulator (SOI) technology are attractive for mixed-signal radio frequency (RF) applications and have gathered numerous studies due to their compatibility with SOI. In practice, the use of SOI substrate is able to eliminate parasitic substrate transistors and associated latch-up and has the ability to reduce crosstalk, particularly when combined with buried ground planes (GP) [61]. The SiGe HBTs on SOI were maturely developed at IBM, IHP, ST and Towerjazz (built on thick SOI) where the architectures can be classified into 2 groups (see Figure 1-34):

- SiGe HBT module is designed to float on the BOX or the collector is on the top of the buried oxide (BOX) (incl. IBM [61], STMicroelectronics [62] and Towerjazz [63]),
- The collector is a high-dose implantation substrate below the BOX (IHP [64]).



Figure 1-34. The cross-section of SOI SiGe HBT architectures at a) IBM [65], b) STMicroelectronics [66], c) Towerjazz [63], d) IHP [64]

The concept of the fully-depleted-collector was used to construct a polysilicon-emitter SiGebase vertical profile bipolar transistor on SOI at IBM [67]. The sub-collector and DTI are not required in this architecture. The transistor operates on the principle that the charge carriers can travel laterally towards the collector reach-through and contact after traversing the intrinsic SiGe base. The architecture is designed to float on the BOX (see Figure 1-34. a).

Within the same category of building the SiGe HBT module floated on the SOI, a compact self-aligned emitter and base structure with the SEG of the base was designed at ST [62]. The STI was no longer used to isolate between the extrinsic base and the collector, and replaced by pedestal oxide layers (see Figure 1-34. b). The best performance was able to archive 86 GHz  $f_T$  and 149 GHz  $f_{MAX}$  in 2005 [62]. However, it is easily recognized that both ST and IBM encountered the significant challenge of large collector resistance ( $R_C$ ) resulting in low  $f_T$  due to the thin SOI, particularly when the thin silicon is less than 120 nm.

Building the SiGe HBT module floated on the SOI was also used at Towerjazz. Benefiting from the thick SOI, the FSA-NSEG architecture (see section 1.4.8) was fully integrated into this SOI substrate without any modifications [63] (see Figure 1-34. c). This device exhibited a small degradation of approximately 7 GHz in  $f_T$  as compared with the bulk device while  $f_{MAX}$  remains near 280 GHz. It is noticed that the integration of SiGe HBT module onto thick SOI is not different from the integration onto the bulk silicon.

In contrast to the previous approaches developed at IBM, ST and Towerjazz, the EEB architecture (see section 1.4.5.1) was integrated into the SOI substrate at IHP by a novel concept (see Figure 1-34. d). The HBT module starts with the formation of windows in the BOX. Then the windows are filled by selective Si epitaxy. The low collector resistance is obtained by high-dose implantation through two windows as performed in Figure 1-35. b. This approach opened a new way for BiCMOS technologies combining state-of-the-art SOI CMOS and bipolar performance. However, the opening of the BOX does not benefit from the low  $C_{CS}$  offered by the BOX isolation in the other architectures. The best performance that was achieved is 220 GHz  $f_T$  and 230 GHz  $f_{MAX}$  in [64].



Figure 1-35. Schematic cross sections illustrating the fabrication of HBT collector wells, (a) After dry etching BOX windows and inside spacer formation (b) After selective epitaxy and collector well implantation. The two windows in the BOX are used for the active HBT region and the collector contact [64]

# **1.6** Comparison of architectures and the choice of the best features for novel architectures at ST

In order to develop novel architectures for the next Si/SiGe BiCMOS technology, the deep understanding about the advantage as well as the limitation of current technologies is required to be clarified. In this section, a rough comparison of the main technological / electrical characteristics of the different HBTs (incl. IBM, IFX, IFX-IHP, IHP and ST) (see TABLE 1-2 and TABLE 1-3) is shown.

The collector module, which is the main difference between the architectures, is classified into 2 categories such as a conventional collector ( $n^+$  buried collector + collector epitaxy + DTI + STI + SIC) and an implanted collector (STI + implanted collector + SIC). Low  $C_{BC}$  (see TABLE 1-3) is recognized as a key advantage of the conventional collector module. This low  $C_{BC}$  is obtained due to a good isolation of STI between the base and the collector. But the ~350 nm thickness and ~100 nm minimum width of a conventional STI become a constraint for the integration of the conventional collector module into the advanced CMOS nodes (28-nm CMOS, 28-nm FD-SOI CMOS and 14-nm FD-SOI CMOS nodes). These thicknesses and widths are huge compared to the geometry dimension of the architecture intended to be integrated into 28-nm FD-SOI CMOS (the emitter width is intended to be much smaller than 100 nm in B55). In fact, the ~350 nm STI's thickness can entail the thick related selective collector epitaxy. Otherwise, MOS devices are built on the top of this selective collector epitaxy. But the height of the SiGe HBT is limited by the pre-metal dielectric (PMD) thickness which is less than 200 nm in the 28-nm FD-SOI CMOS, hence limits the SiGe HBT architecture and MOS devices integration. Therefore, the implanted collector is preferred in these nodes. In addition, a modification of the conventional STI to reduce the STI thickness (i.e. a Super Shallow Trench Isolation (SSTI)) and width would likely be required and can be an alternative choice.

Obviously, most of the architectures shown in the TABLE 1-3 are able to achieve 300 GHz in  $f_{\rm T}$ . It is due to the precise control of the base epitaxy growth, optimized vertical profiles (As, B, Ge and C) and low thermal budgets. But 500 GHz  $f_{\rm MAX}$  and beyond are only achieved by EEB and EBL architectures. These achievements are primary due to the feasibility of forming a silicon base link with a low-resistive connection to the internal base (see TABLE 1-3) as well as a simultaneously low  $C_{\rm BC}$ . In fact, normalized ( $R_{\rm B}+R_{\rm E}$ )× $L_{\rm E}$  of EBL and EEB architectures exhibit the reduction of 47% and 65% respectively, as compared to the conventional DPSA-SEG (from ST). Therefore, these advanced features will be considered and investigated in detail in the novel architectures (see section 4.3).

To handle completely the  $R_{BX}$ - $C_{BC}$  trade-off, the implementation of the secondary shallow oxide filled isolation trenches (SSOFIT) at IBM or the introduction of the lateral oxide filled cavity at IMEC are also evaluated. These core ideas of decoupling between extrinsic base and intrinsic collector will be thoroughly explored in novel architectures in section 4.3.

Based on these comparisons and the review of advanced features coming from different architectures in section 1.4 and 1.5, a series of novel architectures will be proposed in section 4.3 in which the EXBIC architecture emerges as the most promising candidate for the next SiGe BiCMOS technology at ST.

TABLE 1-2. Comparison of the main technological characteristics of the different HBTs architectures

	Unit	IFX	IFX-IHP	ST-B55	IBM9HP	IHP-EEB
Node	nm	130	130	55	90	130
Layout	-	BEC	BEBC	CBEBC	BEBC	BEC
Collector module	-	n+ b	uried layer -	+ DTI + STI +	-SIC	STI+implanted
		collector +SIC				collector +SIC
STI between collector active area and col-	-	Yes	Yes	Yes	Yes	No
lector contact						
B-C junction self-aligned onto E-B junc-	-		Y	es		No
tion						
Emitter self-aligned onto extrinsic base	-	Yes				
Extrinsic base link	-	Vertical	Lateral		Vertical	l
Base link property	-	Poly-	Silicon	Poly-si	ilicon	Silicon
		silicon				
Base epitaxy	-		SEG			NSEG
Ge mode fraction	-	max.=0.3	-	max.=0.32	-	-
Emitter width	nm	130	130	100	100	90
Emitter doping	-	As	As	As	Р	As
Emitter spacer	-	L-shape Straight			Straight shape	
Silicide	-	CoSi <sub>2</sub>	CoSi <sub>2</sub>	NiSi	NiSi	CoSi <sub>2</sub>
Spike annealing temperature	°C	1040	-	1050	-	1050

TABLE 1-3	3. Comparison	of the main	n electrical	characteristics	of the	different HBTs
	· · · · · · · · · · · · · · · · · · ·					

	Unit	IEV	IEV ILID	ST D 55	IDMOUD	ILID EED	IUD EED
	Unit	ΙΓΛ	ΙΓΛ-ΙΠΓ	51-655	ШИЭПГ	INF-EED-	INF-EED-
		[6], [41]	[41]	[8]	[7]	2011 [44]	2015 [6]
$W_{\rm E} \times L_{\rm E}$	$\mu m^2$	0.13×2.73	0.13×2.69	0.1×4.9	0.1×2.0	0.12×0.96	0.09×1.0
n <sub>E</sub>	-	3	3	1	-	8	8
$f_{\mathrm{T}}$	GHz	250	300	320	300	300	325
$f_{\rm MAX}$	GHz	370	500	370	360	500	570
Peak $\beta$	-	1300	1000	1900	470	700	-
$BV_{\rm CE0}$	V	1.5	1.5	1.5	1.7	1.6	-
$(R_{\rm B}+R_{\rm E})\times L_{\rm E}$	$\Omega \times \mu m$	86	46	132	-	70	-
$R_{\rm C} \times L_{\rm E}$	$\Omega \times \mu m$	25	55	24	-	37	-
$C_{\rm CB}/L_{\rm E}$	fF/µm	1.3	1.45	1.17	-	1.8	-
$C_{\mathrm{BE}}/L_{\mathrm{E}}$	fF/µm	2.1	2.1	1.62	-	2.6	-
$C_{\rm CS}/L_{\rm E}$	fF/µm	0.9	0.9	0.85	-	1.1	-
R <sub>sBi</sub>	k Ω/sq	2.6	3.0	5.7	-	2.6	-

# 1.7 Conclusion

In this first chapter, the historical evolution, as well as the state-of-the-art of Si/SiGe BiCMOS technologies have been presented. The electrical performances achieved by different companies were gathered and the evolution of  $f_T$  and  $f_{MAX}$  performances is shown. This chapter has also shortly described the fundamental theory and the figures-of-merit of SiGe HBTs that aim at understanding the device operation as well as the key characteristics. In addition, the development of Si/SiGe BiCMOS technologies within different companies has been figured out. The exploration of different architectures is summarized in a table form. The key advanced features of these current technological characteristics of different HBTs are clarified. It explains in detail how their electrical performances (see Figure 1-36) have been attained. The position of STMicroelectronics inside the map showing Si/SiGe BiCMOS electrical performances compared to other competitors is identified (see Figure 1-36). It is recognized that a novel SiGe HBT architecture is necessary to keep STMicroelectronics at the forefront in the international competition when introducing the next Si/SiGe BiCMOS node. Therefore, developing a novel architecture and related works (B55 TCAD calibration,

thermal budgets investigation and architecture optimization) become a mainstream flowing throughout this thesis.



Figure 1-36. Peak  $f_{\rm T}$  and  $f_{\rm MAX}$  values of high-speed SiGe HBT technologies

# Chapter 2 55-nm Si/SiGe BiCMOS TCAD calibration

## 2.1 Introduction

The integration of the SiGe HBT module into a CMOS process offers circuit designers a Si/SiGe BiCMOS technology. BiCMOS nodes follow the CMOS evolution but being 3 to 4 nodes late. The most advanced Si/SiGe BiCMOS technologies now are the 90-nm Si/SiGe BiCMOS [7], 55-nm SiG/SiGe BiCMOS [9]. Particularly, the evaluation of the SiGe HBT in 28-nm FD-SOI CMOS [24] is carrying out at ST. The HBT's transit frequency  $(f_T)$  and maximum oscillation frequency (f<sub>MAX</sub>) improvements have been driven by scaling strategies (lateral and vertical scaling). Typically, the aim of the vertical scaling is to reduce the emitter-to-collector transit time ( $\tau_{EC}$ ) in order to increase  $f_{\rm T}$ , while  $f_{\rm MAX}$  improvement is accomplished by the lateral scaling due to the decrease of parasitic components such as extrinsic base resistance ( $R_{BX}$ ) and base-collector capacitance ( $C_{BC}$ ). Furthermore, developing new architectures with low parasitic components is also a good choice to achieve higher  $f_{MAX}$  performance [44], [24]. These optimization processes are pushing SiGe HBT performances, but they are practically complicated and always raised the cost in the manufacturing because a large number of advanced process techniques, layouts and masks are required. Therefore, TCAD simulation has emerged as an effective tool to support the SiGe HBT development by providing a detailed understanding of the fabrication process and also the resulting electrical characteristics of a device. The first step in a chain of TCAD's works and supports is the TCAD calibration. Both the fabrication process and the physical device require being calibrated to attain these electrical performances as accurate as possible.

In this chapter, we deepen the understanding and give solutions to calibrate the TCAD tools for simulation of a high-speed Double-Polysilicon Self-Aligned (DPSA) architecture using a Selective Epitaxy Growth (SEG) of the Si/SiGe base in 55-nm BiCMOS [8]. The critical fabrication process steps including the SiGe:C epitaxy growth and in-situ As doped emitter are calibrated in TCAD simulation to match vertical profiles with those obtained from secondary ion mass spectrometry (SIMS) (for As, Ge and B) and energy-dispersive X-ray spectroscopy (EDX) (for As and Ge) measurements. Limitations of this fabrication process calibration are also presented in section 2.2.3. Moreover, the feasibility of capturing accurately electrical performance by physical models validated in previous studies [68], [69] and [70] is systematically evaluated in the chapter. An effective way to calibrate physical device models for SiGe HBT is illustrated and discussed in detail in section 2.4.

The first part of the chapter presents the calibration of the fabrication process with a focus on both the 1D-doping vertical profiles and polysilicon / silicon base link. In addition, the impact of SiGe:C epitaxy growth temperature on the base thickness is analyzed. The limitation of the TCAD deck is then clarified as well. In the second part, a sensitivity analysis approach has been used to adjust some model parameters (including band-gap narrowing, saturation velocity, high-field mobility, SRH recombination, impact ionization, distributed emitter resistance, self-heating and trap-assisted tunneling as well as band-to-band tunneling) to figure out how physical models and related parameters impact the different electrical performances. The resulting map of the impacts of the different physical models provides precious information for TCAD calibration of current and future SiGe HBTs technology at ST.

# 2.2 Fabrication process calibration

## 2.2.1 Regular process calibration

#### 2.2.1.1 Geometry and vertical profile calibration

A careful calibration of the fabrication process in 2D-TCAD is mandatory to simulate accurately the SiGe HBT performance. The Si substrate of 50µm, Deep Trench Isolations (DTI), Shallow Trench Isolations (STI) and CMOS fabrication processes are fully simulated in this TCAD simulation. The first step is to reproduce precisely the device geometry captured with Transmission Electron Microscope (TEM) pictures (see Figure 2-1). Secondly, the vertical doping profile is required to be calibrated from both SIMS (for As, Ge and B) and EDX (for As and Ge) measurements (see Figure 2-3 and Figure 2-4). However, SIMS measurement exhibits an inaccurate result at low doping and very steep profiles [71]- [72]. Particularly, the variation of 1D doping profiles with the emitter width is recognized as a critical step. It requires a specific treatment in the process TCAD simulation to get a good agreement with measurements. This effect is known as the "loading effect" and will be presented in detail in section 2.2.2.1. The inaccurate SIMS measurement and the loading effect lead to an uncertainty about the doping profile. Thus, the profiles from SIMS measurement and the calibrated one from Sprocess TCAD are compared and investigated in detail to gain credibility for the next steps of calibration: A reverse engineering approach based on electrical measurement is used to demonstrate the accuracy of the vertical profile. Obtained resistances and capacitances of the device, calculated from physical model parameters as presented in the initial part of section 2.3, show a good agreement with electrical measurements (see TABLE 2-1) enhancing the confidence in the doping profile obtained from TCAD simulation.



Figure 2-1. SiGe HBT emitter / base architecture: TEM photo (left) vs. implementation in TCAD (right) TABLE 2-1. Comparison of resistances and capacitances between TCAD simulation and measurement

Electrical	$C_{\mathrm{BC0}}(\mathrm{fF})$	С <sub>ВЕ0</sub> (fF)	$R_{\rm BX} \times L_{\rm E} (\Omega.\mu m)$	$R_{\rm sBi}$ ( $\Omega/{\rm sq}$ )	$R_{\rm E}(\Omega)$
Performances	$L_{\rm E} = 5 \; (\mu {\rm m})$	$L_{\rm E} = 5 \; (\mu {\rm m})$	$L_{\rm E} = 10 \; (\mu {\rm m})$	$L_{\rm E} = 10 \; (\mu {\rm m})$	$L_{\rm E} = 10 \; (\mu {\rm m})$
	$W_{\rm E_win} = 0.2 (\mu m)$	$W_{\rm E_win} = 0.2 (\mu m)$	$W_{\rm E_{win}} = 0.2 (\mu m)$	$W_{\text{E}_{win}}=0.2(\mu m)$	$W_{\text{E}_{win}}=0.42(\mu m)$
Measurement	5.62	8.13	510	5724	0.76
TCAD	5.7	8.16	505	5335	0.75

#### 2.2.1.2 Base link calibration

Even when vertical profiles are well calibrated, the simulation of  $f_{MAX}$ ,  $R_{BX}$  and  $C_{BC}$  for DPSA-SEG architecture is still challenging due to the complexity of the base link formation: it has to include the faceting at the edge of SiGe:C intrinsic base and the shallow trench isolation (STI), the boron diffusion through polycrystalline / monocrystalline interface as well as hidden defects. Therefore, the base link formation is simplified by skipping the faceting effect and the boron diffusion through the base link interface is analyzed through inspection of  $R_{BX}$ ,  $C_{BC}$  and  $f_{MAX}$  by a reverse engineering approach [72].

The total dopant flux at polycrystalline / monocrystalline interfaces between the grain boundary and the neighboring layer can be described by the following relationships [73]:

$$\boldsymbol{j}.\boldsymbol{n} = k_{Transfer} \left( C_{Boron}^{Other} - \frac{C_{Boron}^{gb}}{f_{gb} s_g k_{Segregation}^{gb}} \right)$$
(2-1)

$$k_{Transfer} = Prefactor. e^{A/(k_BT)}, \quad A = 2.481$$
(2-2)

Where  $C_{Boron}^{Other}$  is the concentration of boron dopant on the other side of the interface,  $C_{Boron}^{gb}$  is the gain boundary concentration,  $k_{Transfer}$  is the transfer rate,  $k_{Segregation}^{gb}$  is the segregation rate of boron dopant in the grain boundary, the coefficient  $s_g$  is the grain-grain boundary segregation coefficient, the Boltzmann constant ( $k_B$ ) and the temperature (T).

To fit  $R_{BX}$ ,  $C_{BC}$  and  $f_{MAX}$  from electrical measurements, the pre-factor (see eq. 2-2) is adjusted in *Sprocess* TCAD simulation (see TABLE 2-2). Obtained results show clearly the extrinsic base resistance ( $R_{BX}$ ) and base-collector capacitance ( $C_{BC}$ ) trade-off (see TABLE 2-2) when the pre-factor is adjusted. In fact, the pre-factor reduction from default (equal to 80.0 that is given by Sprocess) to 4 results in 265  $\Omega$ .µm increase of  $R_{BX} \times L_E$ , hence can reduce by 73 GHz the peak  $f_{MAX}$  to fit with the measurement. The  $R_{sBi}$  is seemingly unchanged. The absence of the faceting and hidden defects is then taken into account through the pre-factor reduction. The boron diffusion through polycrystalline / monocrystalline interface is not known actually, only the polybase doping is known by SIMS measurement. However, this assumption cannot fit totally the  $f_{MAX}$  for the large range of  $J_C$ . Particularly, the discrepancy on  $f_{MAX}$ , which is observed in Figure 2-2, can be one of the limitations of this TCAD simulation. In fact, this shift is sometime seen in the RF measurement which depends on the measurements method and frequency of extraction. Therefore more experiments and TCAD simulations require to carry out to get a better  $f_{MAX}$  comparison between them. The best calibrated  $f_{MAX}$  (see Figure 2-2) is obtained at the pre-factor value of 4.

Evaluated cases	Pre-factor	$R_{ m sBi}\left(\Omega/ m sq ight)$ $L_{ m E}=10~\mu m m$	$R_{\text{BX}} \times L_{\text{E}} (\Omega.\mu \text{m})$ $L_{\text{E}} = 10 \ \mu \text{m}$	С <sub>вс0</sub> (fF) L <sub>E</sub> =5 µm	f <sub>MAX</sub> (GHz) L <sub>E</sub> =10 μm
Measurement		5724	530	5.62	366
Investigated case 0	3	5329	550	5.67	339
Investigated case 1	4	5335	505	5.7	367
Investigated case 2	4.5	5330	450	5.72	369
Investigated case 3	5.0	5330	430	5.73	375
Investigated case 4	6.0	5328	420	5.76	390
Investigated case 5	80.0 (default)	5338	240	5.82	440

TABLE 2-2. Obtained parameters based on  $R_{\rm sBi}$ ,  $R_{\rm BX}$ ,  $C_{\rm BC}$  and  $f_{\rm MAX}$  measurement by reverse engineering approach



Figure 2-2. Simulated and measured  $f_{\rm T}$  and  $f_{\rm MAX}$  performance

#### 2.2.2 Specific effects

#### 2.2.2.1 Loading effect

A comparison of diffused Ge profile between a real device (HBT) and a process monitoring box (TBox) highlights the variation of Ge profiles with different emitter widths (see Figure 2-3). This effect indicates the injection of interstitial and vacancy defects during the SiGe:C epitaxy resulting in enhanced dopants diffusion. In fact, the defects injection depends on the silicon area exposed during the growth; hence it influences directly the Ge diffusion of the 2D doping profile. Ge diffusion in the TBox (very wide emitter window) is identified to be much larger compared to the real device. In order to reproduce this effect in TCAD simulation, the flux that takes into account the interstitial and vacancy injection during the SiGe:C epitaxy is varied by adjusting the multiply factor ( $\theta$ ) in the generation rate (G) component [73]. Calibrated  $\theta$  values for these injections are shown in TABLE 2-3. As a consequence, the variation of Ge profile with different emitter widths is perfectly captured as shown in Figure 2-3. In addition, the interstitial and vacancy injection during the steep As profile in the emitter (see TABLE 2-3). Calibrated As and B profiles obtained from the *Sprocess* simulation get a good agreement with measurement as shown in Figure 2-4.



Figure 2-3. Comparison of diffused Ge profiles between EDX and TCAD between a real device ( $W_{E_{HBT}_window} = 0.2 \mu m$ ) and a process monitoring box ( $W_{E_{TBox_window}} = 100 \mu m$ )

Obviously, the handling of the loading effect in *Sprocess TCAD* simulation takes a crucial role in the lateral scaling strategy. There is a direct correlation between the accurate doping profile obtained from TCAD simulation and accurate electrical performance predictions of the device.

TABLE 2-3. Calibrated multiply factor ( $\theta$ ) for the SiGe:C epitaxy and in-situ As doped emitter

Epitaxial process	$oldsymbol{ heta}$ Interstitial	$oldsymbol{ heta}_{ ext{Vacancy}}$
SiGe:C epitaxy	7E-7	8E-4
In-situ doped As emitter	0	3E-4





#### 2.2.2.2 Impact of SiGe:C epitaxy growth temperature variation

As mentioned in the previous section, accurate modeling of SiGe:C epitaxy growth is a vital step to get reasonable vertical profiles. The profile does not only depend on carbon and germanium contents incorporated in the silicon base and defects injection but also on temperature and the thermal ramp rate during the SiGe:C epitaxy growth. A series of short loop experiments to evaluate directly the impact of a small variation of the epitaxy temperature is conducted as shown in TABLE 2-4. The variation of  $\pm 2^{\circ}$ C does not make a huge difference on dopants diffusion but it can totally change the base layer thickness, hence it can modify the dopants profile in the base. As a consequence, the  $f_{T}$  and  $f_{MAX}$  drop by 21 GHz and 9 GHz respectively, when the temperature is increased by  $+2^{\circ}$ C. By contrast, the  $f_{T}$  and  $f_{MAX}$  increased by 17 GHz and 3 GHz respectively, when the temperature is decreased by  $-2^{\circ}$ C. This is primary due to the variation of intrinsic resistance and capacitance components. The variation of the base thickness and germanium profile plays also a role in the transit time.

TABLE 2-4. Measured value of normalized SiGe:C and Si-cap thickness corresponding to different epitaxy	growth tem-
peratures	

Temperature(T°C)	Normalized SiGe thickness	Normalized Si-cap thickness
T <sub>ref</sub>	a	b
T <sub>ref</sub> +2°C	1.05a	1.15b
$T_{ref}$ -2°C	0.97a	0.91b

TABLE 2-5. Electrical performance comparison between TCAD simulation and measurement

Measurement			TC	AD
Temperature	$f_{\mathrm{T}}$	fмах	$f_{\mathrm{T}}$	<i>f</i> мах
Tref	326	366	325	367
Tref+2°C	305	357	300	360
Tref-2°C	343	369	339	367

From these experiments, it is recognized that the SiGe:C and Si-cap thicknesses in *Sprocess* simulation are required to be investigated carefully to capture the real doping profile. These thicknesses can be obtained by indirect or direct approaches.

- Indirect approach: Temperature dependence of growth rate featuring the defects injection during the selective epitaxial growth of boron-doped SiGe:C is included in *Sprocess* simulation. The SiGe or Si-cap thickness will be specified through the growth rate, temperature and growth time.
- Direct approach: SiGe:C and Si-cap thicknesses taken by TEM photo are pre-defined in the base epitaxy step in *Sprocess* simulation.

The modeling of the "Indirect approach" is complex in TCAD simulation. Hence SiGe:C and Si-cap thicknesses are introduced using the "Direct approach" in this thesis. These pre-defined values are taken by TEM as shown in TABLE 2-4. Attainable performances show a good agreement comparing between TCAD and measurements (see TABLE 2-5). This demonstrates that reasonable vertical pro-files and calibrated physical models have been used. It is noticed that the physical models applied in this work are the ones fully calibrated in section 2.3.

# 2.2.3 A short summary and existing limitations

From a general and practical point of view, there are three main aspects to be considered to get a good process calibration.

- Capture a precise device geometry
- Capture a suitable vertical doping profile
- Capture an appropriate base link description between extrinsic and intrinsic transistor

Capturing the device geometry is the easiest one in the 3 aspects. The geometrical structure obtained from *Sprocess* simulation is systematically compared with a TEM photo. To ensure a precise geometry modeling at the end of the process flow, the comparison is also carried out after each main process step including the emitter window opening, the pedestal oxide etching, the base epitaxy, the emitter forming as well as the emitter and poly-base patterning.

A consistency of obtained device geometries at different sites on a wafer is also a difficult task. In practice, a difference in geometry is observed by Scanning Transmission Electron Microscope (STEM) combined with energy-dispersive X-ray (EDX) photos. Figure 2-5 shows the difference between devices fabricated at the center and at the edge of a wafer. The simulation of this non-uniformity is not included in this TCAD deck.

Accurate 1D doping profile becomes more difficult to be captured when the emitter width is scaled down to a dimension being smaller than 100 nm. The existence of specific effects described in section 2.2.2 starts showing significant impacts. Particularly, non-uniform Ge (green color) in the base is observed in Figure 2-5. Ge deposited in corners of cavities formed by etching the pedestal oxide is thinner than at the center of this device. This non-uniform Ge can lead to different lattice mismatch resulting in residual strain along lateral SiGe base, hence impacts physical properties of the SiGe base. Modeling of the non-uniform Ge is not included in this simulation. In addition, unexpected defects coming from fabrication processing are not modeled in this *Sprocess* TCAD deck, neither.

In practice, the formation of the base link during the selective epitaxial growth of borondoped SiGe:C base is always complicated. Simultaneously, mono-SiGe-base is grown on the Si substrate and poly-SiGe-base is formed under the overlapped poly-base. Interfaces between them create base links between the extrinsic and the intrinsic base. This formation happens in the corner of the cavity, thus unexpected defects can come into play. The faceting can be formed around the edge of STI. In addition, unclean silicon and polysilicon surfaces in corners can remain after the pedestal oxide wet etching. All of these issues degrade the base link property leading to a large base resistance. Although the base link is closely modeled by the assumption in the previous section, what happens in practice (incl. hidden defects, faceting, etc.) is still not fully described. The simulation of the base link is still a limitation in this work.



Figure 2-5. Non-uniform SiGe in the base and different device geometries obtained at a) the center and b) the edge of a wafer (the sloping device is due to an artifact in the analysis)

# 2.3 Physical device calibration

Considering now the electrical / physical device calibration, the following physical models are used in the B55 TCAD deck:

- Hydro Dynamic (HD) parameters [68]
- Bandgap (BG) of SiGe structure [74] and bandgap narrowing (BGN) [75]
- Energy and relaxation time, mobility [70]
- Intrinsic carrier densities, saturation velocity [69]
- Default Shockley-Read-Hall (SRH), surface SRH and Auger recombination models from Synopsys TCAD [76]
- Default Lackner model for impact ionization from Synopsys TCAD [76]
- Default Schenk model parameters for the trap-assisted tunneling from Synopsys TCAD [76]
- Default Schenk model parameters for the band-to-band tunneling from Synopsys TCAD [76]

These physical models are fed into *Sdevice* simulation to investigate the possibility of TCAD calibration in 55-nm Si/SiGe BiCMOS. The limitation of current models is thoroughly discussed as well. Therefore, a sensitivity analysis approach has been used to adjust some model parameters (incl. band-gap narrowing, saturation velocity, high-field mobility, SRH recombination, impact ionization, distributed emitter resistance, self-heating, trap-assisted tunneling and band-to-band tunneling) in order to figure out how these models impact the different electrical performances. To investigate separately the impact of each physical model, it is assumed that all other physical models are already calibrated and only model parameters for the model under test are adjusted.

#### 2.3.1 Bandgap narrowing (BGN)

Heavy-doping-included bandgap narrowing (BGN) is an important effect in the SiGe HBTs. It tends to increase the equilibrium minority carrier concentration and hence affects the base and collector currents as well as to the carrier transit time. The Slotboom BGN model [75] is applied in the study to describe the effective carrier concentration at heavy doping using a Boltzmann statistics equation without the presence of degeneracy effect (see eq. 2-3).

$$\Delta \boldsymbol{E}_{g,app} = \Delta \boldsymbol{E}_{g,0} \times \left[ ln \frac{N}{N_{ref}} + \sqrt{\left(n \frac{N}{N_{ref}}\right)^2 + C} \right], \tag{2-3}$$

where  $\Delta E_{g,app}$  is the *apparent* BGN and *N* is the impurity concentration. By default  $\Delta E_{g,0}$ =6.92 meV,  $N_{ref}$ =1.3×10<sup>17</sup> cm<sup>-3</sup> and *C*=0.5. The sensitivity analysis approach is carried out by adjusting  $N_{ref}$ . Obtained results show a high impact of this adjustment on  $I_B$ ,  $I_C$ ,  $f_T$  and  $f_{MAX}$ . As shown in Figure 2-6 and Figure 2-7, the  $N_{ref}$  increase is able to fit at medium currents,  $f_T$  and  $f_{MAX}$ . The physical origin for the artificial  $\Delta E_{g,app}$  reduction relies on a difference between *apparent* and *true* BGN [77] caused by carrier degeneracy that is not included in Boltzmann statistics. A consistent Fermi-Dirac statistic correction to the bandgap [78] can take into account the *apparent-true* BGN difference. However, adjusted  $N_{ref}$  of  $1.3 \times 10^{18}$  cm<sup>-3</sup> for Slotboom model can match moderately medium  $I_B$  and  $I_C$  with lower computation time. Thus, the calibrated Slotboom model is retained in this study.



Figure 2-6. Obtained Gummel plot by adjusting N<sub>ref</sub>



Figure 2-7. Obtained  $f_{\rm T}$  and  $f_{\rm MAX}$  performances by adjusting  $N_{\rm ref}$ 

N <sub>ref</sub> (cm <sup>-3</sup> )	Default (1.3×10 <sup>17</sup> )	5×10 <sup>17</sup>	1.3×10 <sup>18</sup>	5×10 <sup>18</sup>
$f_{\rm T}({\rm GHz})$	309	316	325	336
$f_{\rm MAX}  ({ m GHz})$	345	355	367	375
$C_{\rm BE0}({ m fF})$	8.18	8.18	8.16	8.16
$C_{\rm BC0}({ m fF})$	5.7	5.7	5.7	5.7
$R_{ m E0}\left(\Omega ight)$	1.45	1.45	1.44	1.44
$R_{\rm BX0} \left( \Omega. \mu m \right)$	505	505	505	505
$R_{\rm sBi0}$ ( $\Omega/{\rm sq}$ )	5316	5347	5367	5383
$BV_{CEO}(V)$	1.52	1.51	1.5	1.5

TABLE 2-6. Obtained electrical performance by Slotboom parameter variation

#### 2.3.2 Mobility and saturation velocity

The mobility plays a significant role for HD simulations as it influences directly the base and collector current, transit time, the base resistance and the leakage currents. Mobility models, which are validated for SiGe:C alloys with up to 2% of carbon content and 50% of Ge content featuring an ability to distinguish between the isotropic relaxed mobility, and the in-plane and out-ofplane components of the anisotropic mobility tensor relevant to SiGe:C alloys strained on bulk Si [70], are used for the low-field mobility ( $\mu_{Low}$ ). The high-field mobility ( $\mu_{High}$ ) model by *Caughey-Thomas* [79] is used in the study. It is a function of the  $\mu_{Low}$ , the saturation velocity ( $v_{sat}$ ), driving force (*F*) and a fitting parameter ( $\beta$ ) (see eq. 2-4). To investigate the impact of high-field mobility,  $v_{sat}$  component is switched from the default values from Synopsys to the validated one in [69]. However  $f_{T}$  and  $f_{MAX}$  are still underestimated (see TABLE 2-7) despite the fact that the Ge mole fraction dependence of  $v_{sat}$  and  $\beta$  is included. The  $\beta$  is the only parameter left that can be modified to fit the  $f_{T}$ and  $f_{MAX}$  performances. The Ge mole traction dependence of  $\beta$  is skipped. The value of  $\beta$  is varied in a range of 1 to 3 for both the minority and majority carrier. Obtained  $f_{T}$  and  $f_{MAX}$  performance get a good agreement with their measurements at the  $\beta$  of 2.8 as shown in Figure 2-8 and TABLE 2-7.

$$\mu_{High}(F) = \frac{\mu_{Low}}{\left[1 + \left(\frac{\mu_{Low}F}{v_{sat}}\right)^{\beta}\right]^{1/\beta}},$$
(2-4)



Figure 2-8. Obtained  $f_{\rm T}$  and  $f_{\rm MAX}$  frequencies by adjusting  $v_{\rm sat}$  and fitting parameter ( $\beta$ )

	Default model from Synopsis	<i>v</i> <sub>sat</sub> from G. Sasso [69] <i>B</i> =1.384 from G. Wedel [68]	<i>v</i> <sub>sat</sub> from G. Sasso [69] Adjusted exponent <i>B</i> =2.8
$f_{\rm T}$ (GHz)	270	284	325
f <sub>MAX</sub> (GHz)	325	336	367
$C_{\rm BE0}({ m fF})$	8.16	8.16	8.16
$C_{\rm BC0}({ m fF})$	5.7	5.7	5.7
$R_{\rm BX0} \times L_{\rm E} (\Omega.\mu m)$	497	510	505
$R_{\rm sBi0} (\Omega/{\rm sq})$	5378	5452	5366
$BV_{CEO}(V)$	1.39	1.45	1.5

TABLE 2-7. Obtained electrical performances from different saturation velocities and fitting parameter

#### 2.3.3 Recombination and life time

Auger recombination and Shockley-Read-Hall (SRH) models are used in the *Sdevice* simulation to account for the dominant recombination processes in the bulk Si and SiGe:C base. Default parameters for the temperature dependence of the SRH lifetime and Auger recombination models [76] are fed into *Sdevice*. The doping dependence of the SRH lifetime with the Scharfetter relation (see eq. 2-5) is applied and the corresponding parameters are adjusted to take into account the lifetime reduction due to the imperfections in the crystal lattice and the unavoidable introduction of impurities during the crystal growth and wafer processing.

$$\tau_{dop}(N_{A,0} + N_{D,0}) = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_{A,0} + N_{D,0}}{N_{ref}}\right)^{\gamma}},$$
(2-5)



Figure 2-9. Obtained Gummel plot at  $V_{BC}$ =0 (V) by adjusting Scharfetter relation parameters a)  $N_{ref}$  variation, b)  $\tau_{MAX}$  variation and c)  $\gamma$  variation

TABLE 2-8. Default parameters for doping-dependent SRH life time [76]

Symbol	Unit	Electrons	Holes
$ au_{min}$	S	0	0
$ au_{max}$	S	1×10 <sup>-5</sup>	3×10 <sup>-6</sup>
N <sub>ref</sub>	cm <sup>-3</sup>	1×10 <sup>16</sup>	1×10 <sup>16</sup>
γ	1	1	1

TABLE 2-9. Obtained electrical performances by adjusting  $\gamma$ 

γ	Default	1.4	1.6
$f_{\rm T}$ (GHz)	324	325	324
f <sub>MAX</sub> (GHz)	373	367	360
$C_{\mathrm{BE0}}\mathrm{(fF)}$	8.16	8.16	8.16
$C_{ m BC0}( m fF)$	5.7	5.7	5.7
$R_{\rm BX0} \times L_{\rm E} (\Omega.\mu m)$	504	505	505
$R_{\rm sBi0}$ ( $\Omega/{\rm sq}$ )	5383	5370	5375
$BV_{CEO}$ (V)	1.35	1.5	1.8

TABLE 2-8 shows their default parameters. The distinct variation of  $\tau_{\text{max}}$  (0.1×default-10×default s),  $N_{\text{ref}}$  (0.1×default - 10×default cm<sup>-3</sup>) and  $\gamma$ (1-1.6) indicates a high impact on  $I_{\text{B}}$  while a slight impact on  $I_{\text{C}}$  only (see Figure 2-9). Medium  $I_{\text{C}}$  current is moderately fitted with measurement using the  $\gamma$  value of 1.4 (see Figure 2-9. c and TABLE 2-9).

#### 2.3.4 Impact ionization

Impact ionization is one of the most common breakdown mechanisms in real SiGe HBTs. At high reverse voltages, when the electric field in a semiconductor exceeds a certain value, the carriers gains enough energy to excite electron-hole pairs by a process called impact ionization. This process and subsequent avalanche multiplication result in the generation of large numbers of carriers and hence to a larger current. In this thesis, the Lackner model [80] is applied to determine the ionization rate ( $\alpha_v$ ) in the form of a modification of the Chynoweth law by assuming stationary conditions.

$$\alpha_{\nu}(F_{a\nu a}) = \frac{\gamma a_{\nu}}{z} \exp(-\frac{\gamma b_{\nu}}{F_{a\nu a}}), \text{ where } \nu = n, p$$
(2-6)

$$Z = 1 + \frac{\gamma b_n}{F_{ava}} \exp\left(-\frac{\gamma b_n}{F_{ava}}\right) + \frac{\gamma b_p}{F_{ava}} \exp\left(-\frac{\gamma b_p}{F_{ava}}\right), \gamma = \frac{\tanh\left(\frac{\hbar\omega_0 p}{2kT_0}\right)}{\tanh\left(\frac{\hbar\omega_0 p}{2kT}\right)},$$
(2-7)

$$\boldsymbol{b}_{\boldsymbol{v}} \approx \frac{\beta \boldsymbol{E}_{\boldsymbol{g}}}{q\lambda} \tag{2-8}$$

where  $F_{ava}$  is a driving force;  $\gamma$  is the temperature-dependent factor;  $\hbar\omega_{0p}$ ,  $a_v$  and  $b_v$  are the Lackner coefficients in which the  $b_v$  (in eq. 2-7 and eq. 2-8) is specified as a function of bandgap ( $E_g$ ) with the optical-phonon mean free path ( $\lambda$ ) and proportionality constant ( $\beta$ ) (see eq. 2-8). Their default values are shown in TABLE 2-10. In order to ensure a reasonable adjustment, a small variation of  $\beta$  is carried out as shown in TABLE 2-11. The reduction of  $\beta$  results in the  $BV_{CEO}$  and  $f_{MAX}$  reductions (see Figure 2-10 and Figure 2-11), while  $f_T$ , capacitances and resistances are unchanged. Good agreement is obtained for both peak of  $f_{MAX}$  and  $BV_{CE0}$  by adjusting the  $\beta$  value from default down to 0.65 (see TABLE 2-11). Figure 2-11 shows an evolution of the  $I_B/I_{BO}$  vs  $V_{CB}$  relationship at  $V_{BE}$ =0.7 (V). This relationship obtained from *Sdevice* simulation is moderately close to measurement at the  $\beta$  of 0.65. However, considerable differences between simulation and measurement at positions being close to the  $I_{\rm B}/I_{\rm B0}$  ratio of 1 (in the dash-dot olive rectangle) are observed in Figure 2-11. Neutral base recombination (NBR) during electrical measurement [81] seems to be at the origin of this deviation at low  $V_{\rm CB}$ .

Symbol	Unit	Electrons	Holes
a	cm <sup>-1</sup>	$1.316 \times 10^{6}$	$1.818 \times 10^{6}$
$\hbar\omega_{0p}$	eV	0.063	0.063
λ	cm	62×10 <sup>-8</sup>	45×10 <sup>-8</sup>
β	1	0.812945	0.815009

TABLE 2-10. Default coefficients for Lackner model for silicon [76]

TABLE 2-11. Obtained electrical performances by adjusting the proportionality constant  $\beta$ 

$\beta_{\nu}$	Default	0.7	0.65	0.62
$f_{\rm T}({\rm GHz})$	325	325	325	325
$f_{\rm MAX}({ m GHz})$	387	381	367	362
$C_{\rm BE0}({ m fF})$	8.16	8.16	8.16	8.16
$C_{\rm BC0}({ m fF})$	5.7	5.7	5.7	5.7
$R_{\rm BX0} \times L_{\rm E} (\Omega.\mu m)$	505	505	505	505
$R_{ m sBi0} \left( \Omega/ m sq  ight)$	5369	5370	5367	5365
$BV_{\text{CEO}}(\mathbf{V})$	2.1	1.66	1.50	1.43



Figure 2-10. Obtained  $f_{MAX}$  by  $\beta$  adjustment



Figure 2-11. Obtained  $I_{\rm B}/I_{\rm B0}$  vs  $V_{\rm CB}$  by  $\beta$  adjustment at  $V_{\rm BE}$ =0.7 (V)

#### 2.3.5 Distributed emitter resistance and self-heating

In order to capture accurately high  $I_B$  and  $I_C$  currents with measurements, the thermal resistance for the substrate *thermode* ( $R_{\text{sTH}}$ ) and the distributed emitter contact resistance of the device [76] are required to be implemented properly in *Sdevice*. The position of thermodes is directly set on the contact of emitter, base, collector and the bottom of the substrate. Firstly, the variation of the distributed emitter resistance ( $R_{\text{DE}}$ ) (see TABLE 2-12) with an identical substrate thermal resistance of 0.0035 (cm<sup>2</sup>K/W) shows a significant impact at high currents. High  $I_B$  and  $I_C$  only match with their measurement at the  $R_{\text{DE}}$  of close to 0 (see Figure 2-12). Both  $I_B$  and  $I_C$  obtained from different emitter windows ( $W_{\text{E}\_window}=0.2 \ \mu\text{m}$  and  $W_{\text{E}\_window}=0.42 \ \mu\text{m}$ ) are well simulated.  $f_T$  and  $f_{\text{MAX}}$  increase respectively by 6 GHz and 5 GHz to reach measurements when  $R_{\text{DE}}$  is reduced from  $1.8 \times 10^{-8}$  ( $\Omega$ .cm<sup>2</sup>) to 0. While  $BV_{\text{CEO}}$ ,  $C_{\text{BC}}$ ,  $C_{\text{BE}}$  and  $R_{\text{B}}$  do not change (see TABLE 2-12). It means that the distributed emitter is very small in practice. Therefore, this value can be 0 ( $\Omega$ .cm<sup>2</sup>) in other investigations.



Figure 2-12. Obtained Gummel plot with the variation of the distributed emitter resistance a)  $W_{E_window}=0.2 \ \mu m$ , b)  $W_{E_window}=0.42 \ \mu m$ 

$R_{\rm DE} (\Omega. \rm cm^2)$	1.8×10 <sup>-8</sup>	1.0×10 <sup>-8</sup>	1.0×10 <sup>-9</sup>	0
$f_{\rm T}$ (GHz)	319	322	325	325
$f_{\rm MAX}$ (GHz)	362	364	366	367
$C_{\rm BE0}({ m fF})$	8.16	8.16	8.16	8.16
$C_{\rm BC0}({ m fF})$	5.7	5.7	5.7	5.7
$R_{ m B}\left(\Omega ight)$	235	235	235	235
$BV_{\rm CEO}$ (V)	1.5	1.5	1.5	1.5

TABLE 2-12. Obtained electrical performances by adjusting the distributed emitter resistance

Aggressive scaling intended for speed enhancement in B55 usually involves a considerable increase in operation current density. Particularly, a significant impact of the self-heating at high currents is recognized. To identify a precise substrate thermal resistance that will be used in the B55 TCAD deck, the variation of  $R_{sTH}$  is carried out in a range of 0.001 to 0.015 (cm<sup>2</sup>K/W). The  $R_{DE}$  is 0 ( $\Omega$ .cm<sup>2</sup>) in all investigated cases (see TABLE 2-13). High  $I_B$  is recognized to be more sensitive than high  $I_C$  with the variation of  $R_{DE}$  (see Figure 2-13). All electrical performances including  $I_B$ ,  $I_C$ ,  $f_T$ ,  $f_{MAX}$  and  $BV_{CE0}$  are well fitted at the  $R_{sTH}$  of 0.0035 (cm<sup>2</sup>K/W).

The distributed emitter contact resistance and substrate thermal resistance, which have an important impact at high  $I_B$ ,  $I_C$  and at the peak of  $f_T$  and  $f_{MAX}$  as well, depend greatly on the contact resistance during measurement, SiGe HBT architecture and CMOS substrate. Therefore, these values are required to be calibrated accurately for each technology node.



Figure 2-13. Obtained Gummel plot with the variation of thermal resistance

a)  $W_{E_window}=0.2 \ \mu m$ , b)  $W_{E_window}=0.42 \ \mu m$ 

TABLE 2-13. Obtained electrical performances by adjusting substrate thermal resistance in Sdevice

$R_{sTH}$ (cm <sup>2</sup> K/W)	0.015	0.005	0.0035	0.001
$f_{\rm T}({\rm GHz})$	319	323	325	328
$f_{\rm MAX}  ({ m GHz})$	363	366	367	370
$C_{\rm BE0}({ m fF})$	8.15	8.15	8.15	8.15
$C_{\rm BC0}({\rm fF})$	5.7	5.7	5.7	57
$R_{ m B}\left(\Omega ight)$	235	235	235	235
$BV_{CEO}(V)$	1.5	1.5	1.5	1.5

#### 2.3.6 Trap-assisted tunneling (TAT)

Trap-assisted tunneling (TAT) causes a significant increase of the base current at low forward emitter-base bias. This effect generally considered within the field-dependence of the SRH recombination model is caused by strong electric fields. Particularly, it must not be neglected if the electric field exceeds  $3 \times 10^5$  V/cm [76] in certain regions of the device. It should be noticed that the introduction of Ge mole fraction up to 0.32 affects the impact of the lattice mismatch and induces a biaxial tensile stress in the SiGe base layer. This stress results not only in a bandgap reduction but also in a reduction in the carrier's effective mass and the mid-gap trap level [82]. Therefore the increase of TAT current is observed.

Schenk's model [83] describing the TAT is applied. Carrier tunneling masses ( $m_{\theta}$ ) are only modified to reproduce the reduction of their masses due to the biaxial tensile stress (see corresponding tensile strain measured at ST by the NanoBeam Electron Diffraction (NBED) measurement in Figure 2-14). Other parameters kept their default values set in Synopsys [76]. The band-to-band (B2B) tunneling is not activated in this simulation. Obtained result shows that the  $m_{\theta}$  reduction describes accurately how the TAT impacts  $I_{\text{B}}$  at medium-low  $V_{\text{BE}}$  (see Figure 2-15).  $I_{\text{B}}$  from *Sdevice* TCAD simulation gets a good agreement with electrical measurement when the  $m_{\theta}$  is reduced by a factor of 0.31 (see Figure 2-15) that is consistent with the work presented in [82]. In addition, in Figure 2-15 we can recognize the dominant regime of the TAT in a  $V_{\text{BE}}$  range of 0.38 V to 0.65 V in this device.

It is noticed that the dominant regime of the TAT is very large in this experimental lots. This regime is going to be minimized in other lots at ST.



Figure 2-14. a) Tensile strain is measured along cutting line 1 b) Tensile strain along the cutting line 1 was measured at STMicroelectronics



Figure 2-15. Obtained base current by adjusting effective electron mass in Schenk's TAT model

#### 2.3.7 Band-to-Band-tunneling (B2B)

The onset of TAT starts at an electric field of about  $3 \times 10^5$  V/cm, independent of the value of the lattice energy, whereas a B2B tunneling rate of  $10^{14}$  cm<sup>-3</sup> s<sup>-1</sup> is reached at  $6.6 \times 10^5$  V/cm [84].

Thus, both TAT and B2B tunneling can come into play at low  $I_B$ . In fact, their dominant regimes can be divided as following. Going from large forward bias (low field strength) to zero voltage (higher field strength), the excess current due to the TAT comes first into play, then the  $I_B$  is governed by a superimposition of TAT and B2B tunneling. Finally, the current is determined by sole B2B tunneling. Therefore, the activation of the TAT is required in this simulation.

In order to take into account B2B tunneling, Schenk's model described in the expressions (eq. 2-9 and 2-10) is applied. Where the default values of *A* and *B* can be identified in TABLE 2-14.  $n_0$  and  $p_0$  are the electron and hole equilibrium concentrations. The  $\hbar\omega$  quantity denotes the energy of the effective phonon energy; the default energy value figures in TABLE 2-14.  $E_{g,eff}$  is the effective bandgap,  $E_g=E_g-E_{bgn}$ . *F* is electric field strength. The calibrated TAT (in section 2.3.6) is switched on. The B2B is also impacted by defects occurring during the fabrication process as well as the biaxial stress that existes in the SiGe base [82]. Therefore, *A* and *B* are alternatively adjusted to reproduce  $I_B$  at low  $V_{BE}$ . The adjustment of *A* value does not influence  $I_B$  (see Figure 2-16. a), while a large impact of the adjustment of *B* value on  $I_B$  (see Figure 2-16. b) is observed. In fact, the original expression of *B* in Schenk's model [84] is described by eq. 2-11 where  $\mu_{\parallel}^{\alpha}$  is a component including the electron tunneling masses for the three Cartesian directions of the crystal. Therefore, the reduction of  $0.53 \times B$  (see Figure 2-16. b) to match with electrical measurement can be interpreted as the electron tunneling mass reduction due to the impact of defects and stresses that exists in the SiGe:C base [82]. The dominant regime of B2B-tunneling is identified to be in a  $V_{BE}$  range of 0 V to 0.38 V in this device (see Figure 2-16).

$$R_{net}^{bb} = AF^{7/2} \frac{np - n_{i,eff}^2}{(n + n_{i,eff})(p + n_{i,eff})} \left[ \frac{\left(F_c^{\mp}\right)^{-3/2} exp\left(-\frac{F_c^{\pm}}{F}\right)}{exp\left(\frac{\hbar\omega}{kT}\right) - 1} + \frac{\left(F_c^{\pm}\right)^{-3/2} exp\left(-\frac{F_c^{\pm}}{F}\right)}{1 - exp\left(-\frac{\hbar\omega}{kT}\right)} \right]$$
(2-9)

$$F_{C}^{\pm} = B \left( E_{g,eff} \pm \hbar \omega \right)^{3/2}, n_{i,eff} = n_{0} p_{0}$$
(2-10)

TABLE 2-14. Coefficients of Schenk model for band-to-band tunneling [76]

Symbol	Unit	Default value
Α	cm <sup>-1</sup> s <sup>-1</sup> V <sup>-2</sup>	$8.977 \times 10^{20}$
В	Vcm <sup>-1</sup> eV <sup>-3/2</sup>	2.14667×10 <sup>7</sup>
ħω	MeV	18.6

$$B = \frac{4}{3} \frac{\sqrt{2\mu_{\parallel}^{\alpha}}}{e\hbar}$$
(2-11)



Figure 2-16. Obtained base current by adjusting parameters of Schenk's B2B tunneling model a) adjustment of the *A* value, b) adjustment of the *B* value

# 2.4 Discussion

mobility

SRH model

Impact

ionization R<sub>DE</sub>

Self-heating

ТАТ

**B2B** 

The Si/SiGe BiCMOS TCAD calibration is fully recognized as a significant and challenging works in the chain of supporting the SiGe HBT development. It is significant because of following reasons.

- It provides a detailed understanding of the fabrication process and also the resulting electrical characteristics of a device
- It permits the optimization of the geometrical dimensions, vertical doping profile and thermal budgets of the SiGe HBT architecture for electrical performances' enhancement
- It saves costs for the R&D and the manufacturing process

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- It provides good physical models to predict SiGe HBT performances of the next generation.

Ів **I**c Peak Peak BVCEO **Physical models** Low Medium High Low Medium High fт fmax BGN +++ +++  $^+$ +++++++ +**High-Field** *v*<sub>sat</sub> +++++++ +++ ++

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TABLE 2-15. The resulting map of the impacts of the different physical models (+++ indicates a high impact,	, - indi
cates no impact)	

At the beginning, the uncertainty concerning the correct vertical doping profile as well as
the non-calibrated physical model parameters cause enormous difficulties during the TCAD calibra-
tion. Therefore, a series of short loop experiments, physical and electrical measurements as well as
thousands of TCAD simulations are performed to figure out how the physical models impact the
different electrical characteristics. An analysis of the impact of the different physical models and their
corresponding parameters presented in previous sections is summarized in TABLE 2-15.

Obviously, the capability to control precisely the thicknesses and doping profiles is different in each technology due to the available tools and techniques. The loading effect and hidden defects remaining in the transistor result in a variation of physical model parameters which hence require being calibrated for every new technology node. From this point of view, an emerging question is "How/what is the best/fastest way to calibrate accurately physical models for every SiGe HBT technology node?"

To the best of the author's knowledge, there is no previous report / publication on the SiGe HBT calibration available in literature addressing the previous questions. Therefore, starting from the map of the impacts of the different physical models vs. electrical performances presented in TABLE 2-15 we can elaborate the TCAD calibration process as summarized in the following steps.

- Step 1: Capture reasonably the device geometry and the vertical doping profile
- Step 2: It is noticed that HD parameters highly impact the SiGe HBT performances. These parameters are required to be setup as described in [68] and [85]
- Step 3: Calibrate the bandgap of SiGe structures, BGN and effective density-of-states (DOS) to fit medium  $I_{\rm C}$
- Step 4: Calibrate SRH and Auger recombination to fit medium I<sub>B</sub>
- Step 5: Calibrate the distributed emitter resistance and self-heating to fit high  $I_{\rm C}$  and  $I_{\rm B}$  respectively
- Step 6: Calibrate the mobility and the saturation velocity to fit  $f_{\rm T}$
- Step 7: Calibrate the impact ionization to fit  $BV_{CE0}$  and  $f_{MAX}$
- Step 8: Activate TAT and B2B tunneling to calibrate low  $I_B$ . Both TAT and B2B models are only switched on when the investigation of low current is necessary. The activation of these models can take time and may lead to convergence problem in simulation.

# 2.5 Conclusion

Both, the fabrication process and physical device calibrations for the high-speed DPSA-SEG Si/SiGe HBTs in 55-nm BiCMOS have been presented in this chapter. Not only vertical profiles and extrinsic base link calibrations have been introduced, but also for the first time all the physical models (including bandgap narrowing, mobility, SRH recombination, impact ionization, distributed emitter resistance, self-heating, TAT and B2B tunneling) have been simultaneously worked out. The obtained 2D-TCAD electrical results fit well with the  $I_B$ ,  $I_C$ ,  $f_T$ ,  $f_{MAX}$  and  $BV_{CEO}$  measurements. The resulting map of the impacts of the different physical models on various electrical characteristics provides precious information for TCAD calibration of current and future SiGe HBTs technologies (see TA-BLE 2-15). This chapter concludes by showing up an effective way to calibrate physical models in any Si/SiGe BiCMOS technology node. The results obtained in this chapter are a strong foundation to ensure accurate predictions of the performances of the next SiGe HBT generation that will be presented in chapter 3 and chapter 4. Results presented in this chapter contributed to the publication at the ECS PRiME-2016 [86].

# Chapter 3 BiCMOS thermal budget study

# 3.1 Introduction

The performance of SiGe HBTs is driven by innovative architectures and scaling strategies including vertical and lateral scaling. Both these driving aspects are thoroughly investigated in this thesis to enhance Si/SiGe BiCMOS performances in the next generation at STMicroelectronics. Obviously, the transistor architecture is a central element for  $f_{MAX}$  performance enhancement. Thus, the advantages and limitations comparison of different SiGe HBT architectures were fully clarified in section 1.6. Furthermore, novel architectures with advanced features (low  $R_{BX}$  and low  $C_{BC}$ ) for the next SiGe HBT generation are going to be presented and discussed in detail in section 4.3. For scaling strategies, advanced photolithography is the key for the lateral scaling. Fortunately, a series of available 40-nm CMOS (C40), 28-nm CMOS (C28), 28-nm CMOS FD-SOI (C28FD) and 14-nm CMOS FD-SOI (C14FD) nodes featuring advanced photolithography and process techniques establish a strong starting point to move the current 55-nm Si/SiGe BiCMOS technology into the next generation at ST. Vertical scaling employed for improving  $f_{\rm T}$  performance is usually accomplished by a combination of following processing steps: (i) implementing carbon to SiGe epitaxy base, controlling Sicap thickness and reducing the processing thermal budget to minimize the boron diffusion (ii) optimizing germanium ramp to accelerate the electron movement through the neutral base and finally (iii) increasing the collector doping level. The introduction of carbon and optimization of Si-cap thickness for the base can handle efficiently the boron out-diffusion. In fact, the origin of boron out-diffusion and Ge ramp flattening comes from the processing thermal budget that challenges the vertical profile optimization. Therefore, the impact of the thermal budget is widely explored and thoroughly explained in this work.

In this chapter, we deepen the understanding how the thermal budgets of the different process steps impact the vertical doping profile. In the first part, a study of B55's thermal budget partitioning is carried out. The evolution of dopants' diffusion is investigated after each main process steps (incl.  $n^+$  buried layer, STI, DTI,  $n^+$  sinker, base epitaxy, poly-gate re-oxidation, CMOS's spacer formation and spike annealing) to clarify their respective impact. Particularly, the poly-gate re-oxidation (Polyreox) and spike annealing thermal budgets are inspected. Their thermal budgets have not only a huge impact on the base thickness but also represent a dominant factor for the extrinsic base resistance (see in detail in 3.4). Finally, a roadmap, running parallel to the ITRS one [12], to predict the performance of SiGe HBTs considering the impact of the thermal budget coming from advanced CMOS nodes is exhibited in this chapter.

The first part of this chapter presents in detail the BiCMOS055's fabrication process flow in order to clearly explain how the transistor is fabricated. The second part describes precisely the B55's thermal process steps and shows their impacts on the evolution of the vertical doping profiles. The thermal budgets coming from manufacturing processes after the SiGe and Si capping epitaxy are particularly investigated. Finally, the influence of the thermal processing of advanced CMOS nodes

on 1D profiles of SiGe HBTs is carried out by associating fabrication process and hydrodynamic (HD) [68] simulations in the following manner: Firstly, the calibrated 1D-TCAD deck is modified by splitting the fabrication process flow. The collector, base and emitter of SiGe HBTs module is kept identical while the CMOS process is alternately replaced by the one coming from C40, C28, C28FD and C14FD. For a fair comparison of the different technologies and for bringing the profiles as close as possible to a real fabrication, the SiGe:C thickness and Si capping have been tuned as detailed in section 3.6. These process modifications are simulated by the calibrated TCAD deck presented in chapter 2. Obtained vertical doping profiles are fed into Hydrodynamic (HD) simulator to predict the main electrical characteristics including the transit frequency  $f_{\rm T}$ , internal capacitances and pinched base sheet resistance for the HBT fabricated in the next CMOS nodes.

# 3.2 BiCMOS055 fabrication process flow

The fabrication process flow for the DPSA-SEG architecture at ST is presented in detail in [4]. The first part of this flow addresses the formation of the conventional collector including  $n^+$  buried collector (see Figure 3-1. a), collector epitaxy (see Figure 3-1. b) and DTI (see Figure 3-1. c). The STI is performed next and then the  $n^+$  sinker is implanted to reduce the extrinsic collector resistance (see Figure 3-1. c). Under the driving thermal budgets coming from the recrystallization annealing, DTI and STI formation, a number of arsenic atoms gradually diffuses from the high  $n^+$  buried layer into the collector epitaxy of the transistor. The CMOS process flows (incl. deep Nwell, Nwell, Pwell, PMOS, Well annealing, etc.) are fabricated after this step. Finally, the collector module is completed by the selectively implanted collector (SIC) by using one mask. This SIC is carried out after opening the SiGe HBT region being in the window of the polysilicon (see Figure 3-1. d).

The SiGe HBT emitter / base fabrication starts with the deposition of the extrinsic base stack composed of pedestal oxide / poly-base / oxide / nitride layers (see Figure 3-2. a). The emitter window opening (see Figure 3-2. b) is carried out by one mask and then, nitride sidewalls are formed to protect poly-base from the base epitaxy. The SEG is performed after the wet etching of a cavity in the pedestal oxide (see Figure 3-2. c). It is noticed that the cavity width is larger than the emitter window width to provide a vertical base link between extrinsic-intrinsic base forming during the selective epitaxial growth of boron-doped SiGe:C and the Si-cap. The in-situ As doped emitter is deposited after the formation of inside "L" spacers reducing the effective emitter width ( $W_E$ ) (see Figure 3-2. d). The HBT fabrication module ends by the patterning of the poly-emitter and the extrinsic poly-base (see Figure 3-2. e), the spike annealing, silicidation and contact formation (Figure 3-3).













d)

Figure 3-1. a)  $n^+$  buried collector, b) collector epitaxy, c)  $DTI + STI + n^+$  sinker and d) SIC







b)



c)



Figure 3-2. a) Pedestal oxide / Poly-base / Nitride stack b) emitter window c) pedestal oxide wet etching and SiGe-Si capping epitaxy, d) "L" spacer formation and in-situ As doped emitter and e) emitter, poly-base patterning and collector opening



Figure 3-3. Obtained architecture after spike annealing, silicidation and contact formation

# **3.3 BiCMOS055 thermal budget partitioning**

To fully understand the impact of thermal budgets during the manufacturing process, the evolution of vertical profiles is thoroughly investigated after each main process step including  $n^+$  buried layer, STI, DTI,  $n^+$  sinker, MOS well anneal, SIC, SiGe base epitaxy, in-situ As doped emitter deposition, poly-gate re-oxidation (Polyreox), CMOS spacers formation, spike annealing and silicidation as well as contacts formation. This investigation plays a crucial role not only in understanding how the thermal budget of the processing steps impacts the doping profiles but also in optimizing the thermal budgets for the vertical scaling strategy. In practice, process steps including thermal processing during the manufacturing process can be divided into two categories in B55:

- Process step before SiGe base epitaxy
- Process step after SiGe base epitaxy.



Figure 3-4. Evolution of As doping profile with the thermal budget in B55 before SiGe epitaxy

The thermal budgets in the first category mainly come from the bipolar collector module formation (n<sup>+</sup> buried layer anneal, collector epitaxy, deep trenches anneal), the shallow trenches, n<sup>+</sup> sinker and MOS well anneals. These thermal processing steps contribute largely to the As diffusion from the n<sup>+</sup> buried layer into the collector epitaxy (see Figure 3-4). Particularly, process steps conducted during and before the STI result in a large As diffusion while others have less impact. These thermal budgets play an important role on the resulting collector profile, influencing directly  $C_{BC}$  and the collector resistance ( $R_C$ ). Fortunately, their impacts can be controlled by tuning the buried layer implantation conditions and collector epitaxy thickness for example. The steepness of the collector profile can be adjusted by the selectively implanted collector (SIC).

For the second category, the main thermal process steps are from the base epitaxy itself, the poly-gate re-oxidation (Polyreox) performed after gate patterning, and the source / drain spike annealing. The evolution of dopants diffusion from the base epitaxy to the source / drain anneal is presented in Figure 3-6. The thermal budgets coming from silicidation and contacts formation is skipped because of a low treatment temperature (smaller than 400°C). Arsenic from the emitter is deeply driven into the base while the boron width determined at EB junction of  $1.6 \times 10^{16}$  cm<sup>-3</sup> in Figure 3-6. a is multiplied by a factor of ~3 between base deposition and the end of the process flow (see Figure 3-5). Particularly, it is recognized that the boron thickness is increased by a factor of approximately 2.5 after the Polyreox process (reaching 800°C). These results indicate a high impact of this thermal budget on both As and B profiles, while a small variation of Ge profile is observed. From the technical point of view, it is preferred to replace the Polyreox process by a lower treatment temperature process to avoid both As and B diffusion in order to obtain a thinner base width. However, the Polyreox thermal budget benefits to the reduction of the intrinsic-to-extrinsic base link resistance [87]. Finally, the spike annealing is shown as the one of key thermal budget influencing the diffusion of all dopants. It does not only expands As and B diffusions but also flattens the Ge ramp. To better understand the impact of spike annealing thermal budget, the investigation of peak spike annealing temperature is carried out in section 3.5.



Figure 3-5. Evolution of boron thickness at the EB junction doping of  $1.6 \times 10^{16}$  cm<sup>-3</sup>



Figure 3-6. Evolution of the vertical profile with the thermal budget in B55: AF1-after base epitaxy, AF2-after Polyreox, AF3-after CMOS spacers formation and AF4-after spike annealing for a) Arsenic, b) boron c) Germanium and d) As and B in AF2 and AF4

# **3.4** Replacement of the Polyreox by TEOS oxide deposition

The previous study of the thermal budget from the different process steps shows an important impact on the vertical doping profile during the Polyreox process. Though it does not change the germanium ramp, it increases the arsenic drive-in from the emitter into the Si-cap as well as the boron diffusion. In order to minimize the influence of the thermal budget, the Polyreox is replaced by the Tetra Ethyl Ortho Silicate (TEOS) oxide deposition having a maximum process temperature of  $625^{\circ}$ C. In fact, the replacement of Polyreox by TEOS deposition is done in advanced CMOS nodes (beyond 55 nm). The vertical doping profile obtained after this replacement is shown in Figure 3-7. The reduction of arsenic and boron diffusion observed in Figure 3-7 results in 6% and 18% decrease of  $R_{sBi}$  and  $C_{BE}$  respectively. However, the  $R_{BX}$  is increased by 27% because the number of boron diffusion from the extrinsic into the intrinsic is reduced by a lower thermal budget (see Figure 3-8. a and Figure 3-9. b). This large  $R_{BX}$  increase leads to a degradation of 71 GHz in  $f_{MAX}$  performance (see Figure 3-10). It highlights the importance of the base link resistance in the DPSA-SEG architecture.

To optimize the benefits of the thermal budget reduction, we reduce the Si-cap thickness by a factor from 1 down to 0.65. This is carried out to bring the arsenic profile in the emitter being closer to the boron profile in the base. The thinner Si-cap can reduce the transit time, hence improving  $f_T$  performance. In fact, the  $f_T$  increases from 309 GHz to 335 GHz and to 365 GHz in this TCAD simulation when the reduction factor of si-cap thickness is reduced from 1 to 0.8 and to 0.65, respec-

tively (see Figure 3-10). However, both  $C_{BE}$  and  $R_{sBi}$  are increased by a factor of 1.3 and 1.2 respectively (see Figure 3-8. a and Figure 3-9. b). The thinner Si-cap results in a thinner base link, hence the high boron doped extrinsic base is closer to the boron doped intrinsic base in the link region. In fact, the obtained  $R_{BX} \times L_E$  when the Polyreox is replaced by TEOS oxide deposition, is reduced by 70  $\Omega$ .µm when the Si-cap thickness is reduced by a factor from 1 to 0.65 (see Figure 3-8. b). But this value is still 65  $\Omega$ .µm greater than the one of using the Polyreox. Therefore, the poly-base doping is increased to decrease the extrinsic base resistance in the next investigation.

The maximum boron doping can be greater than  $1 \times 10^{21}$  cm<sup>-3</sup>, but active boron obtained from SIMS measurement is below few  $10^{20}$  cm<sup>-3</sup>. In this study, the poly-base doping is still investigated in a range of  $1 \times 10^{21}$  cm<sup>-3</sup> (in B55) to  $1 \times 10^{22}$  cm<sup>-3</sup>. The improvement of the boron diffusion from extrinsic into intrinsic base leads to the reduction of  $R_{BX}$ . As a consequence,  $R_{BX}$  is reduced by a factor of 1.14 (see Figure 3-11), hence pushing up 37 GHz in  $f_{MAX}$  (from 367 GHz to 404 GHz), while the  $f_T$  is unchanged at 365 GHz (see Figure 3-12).

As a short conclusion, the replacement of the Polyreox by the TEOS oxide deposition can reduce the thermal budget impacting on arsenic and boron doping profiles. We optimize the benefits of this reduction by adjusting the Si-cap thickness to decrease the intrinsic base width. The degradation of  $R_{BX}$  due to thermal budget reduction is handled by increasing the poly-base doping. 365 GHz  $f_{T}$  and 404 GHz  $f_{MAX}$  obtained from TCAD simulation are promising performances for a high-speed SiGe HBT device with the DPSA-SEG architecture. However, more experiments require to carry out to calibrate the boron diffusion from extrinsic base into intrinsic base to estimate the accuracy of this prediction.



Figure 3-7. Obtained vertical doping profile by replacing Polyreox by TEOS process



Figure 3-8. Obtained base resistance components by replacing Polyreox by TEOS process and adjusting the Si-cap thickness a)  $R_{\rm sBi}$  b)  $R_{\rm BX}$ 



a)



Figure 3-9. Obtained capacitances by replacing Polyreox by TEOS process and adjusting the Si-cap thickness a)  $C_{\text{BE}}/A_{\text{E}}$  b)  $C_{\text{BC}}/A_{\text{E}}$ 



Figure 3-10. Obtained  $f_{\rm T}$  and  $f_{\rm MAX}$  performances by replacing Polyreox by TEOS process and adjusting the Si-cap thickness



Figure 3-11. Obtained extrinsic base resistance by increasing the polybase doping



Figure 3-12. Obtained  $f_{T}$  and  $f_{MAX}$  performances by increasing the polybase doping

# **3.5** Spike annealing temperature variation

The reduction of the spike annealing (SA) temperature plays an important role in the vertical scaling strategy. It is noticed that the SA optimization has been carried out in several companies. For examples, the SA temperature was reduced from 1100°C (D51) to 1070°C (D52) and further to 1050°C (D53) at IHP to speed up ( $f_T$ ,  $f_{MAX}$ ) performances from (235 GHz, 300 GHz) to (250 GHz, 400 GHz) and (300 GHz, 500 GHz), respectively [10]. In fact, these performances were obtained by the combination of both SA temperature reduction and corresponding variations of effective emitter width ( $W_E$ ), SIC and base width. At ST, the SA temperature was also reduced from 1113°C (B9MW) down to 1080°C (B4T) and to 1050°C (B55). Benefiting from this reduction, and with the combination of variations in SIC,  $W_E$  and base width and the use of advanced layouts, the increasing ( $f_T$ ,  $f_{MAX}$ ) performances from (230 GHz, 280 GHz) [4] to (265 GHz, 400 GHz) [88] and to (320 GHz, 370 GHz) [8] have been achieved. Ultimately, the  $f_T$  of 410 GHz has been demonstrated in [56] by reducing the spike anneal temperature down to 1000°C.


Figure 3-13. Vertical doping profile corresponding to spike annealing temperature of 1113°C (B9MW), 1050 °C (B55) and 1000°C a) As-B vertical profiles and b) Ge %



Figure 3-14. Boron thickness at a BE junction doping of  $1.6 \times 10^{16}$  cm<sup>-3</sup> corresponding to the spike annealing temperature variation from 700°C to 1113°C

To deepen the understanding of the impact of the SA temperature, the former is varied in a large range of  $1113^{\circ}$ C down to 700°C in process TCAD simulation. This variation shows an enormous impact on vertical doping profiles (see Figure 3-13 and Figure 3-14). The boron thickness measured at a BE doping junction of  $1.6 \times 10^{16}$  cm<sup>-3</sup> is decreased by a factor of 2 when the SA temperature is reduced from  $1113^{\circ}$ C to 700°C. Particularly, it is important to note that the boron thickness is not expected to further reduce for an SA temperature below 1000°C since the boron diffusion is dominated by the thermal budget of base epitaxy itself and Polyreox processes.

#### **3.6** Impact of process thermal budget coming from different CMOS nodes

The 1D-profile shown in Figure 2-3 and Figure 2-4, corresponding to the B55 technology [8], is used as a reference for the following studies. The laser spike annealing (LSA) employed in the advanced CMOS nodes (C40, C28, C28FD and C14FD) allows reducing the thermal budget. Particularly, the maximum of the SA temperature is reduced and the Polyreox process step is no longer used beyond the 55-nm CMOS node. As a consequence, the thermal budget reduction results in the decrease of Arsenic's drive-in from the emitter and the SIC into the base and the reduction of boron diffusion into the Si capping, either (see Figure 3-15). By *Sprocess* TCAD simulation, it is recognized that the boron thickness (determined again at  $1.6 \times 10^{16}$  cm<sup>-3</sup>) is sharply reduced by ~40% in C40 and C14FD, and ~25% in C28 as well as ~20% in C28FD (see Figure 3-16).



Figure 3-15. Vertical profiles at the end process flow corresponding to B55, C40, C28, C28FD and C14FD a) As vertical profiles, b) B vertical profiles, c) Ge vertical profiles and d) As-B doping profiles of B55 and C14FD in the same plot

For a fair comparison of the different technologies and for bringing the vertical doping profiles as close as possible to a real fabrication, it is necessary to tune the thicknesses of the SiGe:C and the Si capping layers to account for the reduced diffusion (see Figure 3-17). In addition, keeping the distance between the rising and falling slopes of the Ge and the metallurgic junctions constant for all CMOS nodes is a prerequisite to perform comparable simulations for all process technologies. It ensures comparable reverse and forward Early voltages for all processes. The deposited SiGe:C layer is therefore modified by cutting the parts highlighted in Figure 3-17. The movement of Si/SiGe BiC-MOS from 55-nm node to advanced nodes can need a considerable modification of extrinsic transistor, even a new architecture is required as discussed in chapter 1. Therefore, only vertical profiles obtained by 1D-TCAD process simulations are fed into a 1D HD simulator [72] to determine relevant electrical characteristics. Two approaches are evaluated to predict the impact of the thermal budget on the device performance:

- Identical doping at BE and BC metallurgical junctions (equal to B55)
- Identical internal BE capacitance (equal to B55)



Figure 3-16. Boron thickness at a BE junction doping of  $1.6 \times 10^{16}$  cm<sup>-3</sup> with CMOS thermal budget variation from B55 to C14FD



Figure 3-17. Tuned parts of SiGe layer and Si capping thickness

#### 3.6.1 Approach 1: Identical doping at BE and BC metallurgical junctions

To fix the doping at BE and BC junctions at the respective level of  $1.6 \times 10^{16}$  cm<sup>-3</sup> and  $2.4 \times 10^{16}$  cm<sup>-3</sup>, it requires to make the following modifications: reduce the Si capping thickness, modify the SiGe:C thickness and shift the collector for each profile. Vertical profiles obtained by 1D-TCAD after tuning of the layers thicknesses are shown in Figure 3-18. The consequence of steeper doping profiles associated with a lower process thermal budgets is a thinner space charge regions (SCR) leading to an increase of both  $C_{jEi}$  and  $C_{jCi}$ . In addition, the neutral base thickness is also reduced as shown in Figure 3-20, causing a dramatic increase of the base sheet resistance ( $R_{Bi}$ ) as shown in Figure 3-19. c. Resulting electrical performances are summarized in TABLE 3-1. It is noted that 15.3 % difference between  $R_{sB0}$ (B55-1D) and  $R_{sB0}$ (B55-2D) comes from the physical models in 1D device simulation in [71] and [72] are not fully calibrated. The reference exhibits 330 GHz  $f_{T}$ , higher than the one of chapter 2 due to the use of only 1D simulation.



Figure 3-18. Vertical profiles after tuning the SiGe layer, the Si capping thicknesses and a collector shift to fix the doping at the BE and BC junctions for all nodes a) Arsenic, b) Boron, c) Germanium and d) Vertical profiles with related SRC at 0 V



Figure 3-19. Electrical performances obtained by 1D simulation for the case of the fixed doping at BE and BC junctions: a)  $C_{jCi}$ , vs  $V_{BC}$ , b)  $C_{jEi}$  vs  $V_{BE}$ , c)  $R_{sBi}$  vs  $V_{BE}$  and  $f_T$  vs  $J_C$ 

Nodes	B55-2D	B55-1D	C40-1D	C28-1D	C28FD-1D	C14FD-1D
$C_{jC0}$ (fF/ $\mu$ m <sup>2</sup> )	2.7	2.89	3.20	3.11	3.07	3.19
$C_{\rm jE0}~({\rm fF}/{\rm \mu m^2})$	7.21	7.06	10.49	9.38	8.91	11.05
$R_{\rm sB0}$ (k $\Omega$ /sq)	5.3	4.49	6.29	5.47	5.22	6.26
$f_{\rm T}$ (GHz)	325	330	356	369	370	360

TABLE 3-1. Obtained electrical performances for the assumption of identical base-emitter junction



Figure 3-20. Normalized neutral base thickness corresponding to different nodes by the assumption of identical EB and BC junctions

#### 3.6.2 Approach 2: Identical base-emitter capacitance

The strong increase of  $R_{\text{Bi}}$  and  $C_{\text{jEi}}$  will degrade both  $f_{\text{MAX}}$  and  $f_{\text{T}}$  at low current densities, respectively. To overcome these issues, the second assumption with a fixed identical  $C_{\text{jEi}}$  is performed, leading to the profiles shown in Figure 3-21. The Si capping thickness can be adjusted to fix a  $C_{\text{jE0}}$  equal to 7.06 fF/µm<sup>2</sup> for all nodes. Consequently, 1D-TCAD process simulations with the modified SiGe layer and Si capping thicknesses are carried out. It was not necessary to modify the collector region, as observed change in  $C_{\text{jCi}}$  of the previous section is negligible for the considered nodes. The internal base resistance considerably reduces as shown in Figure 3-22. c, because of the reduced extension of the SCR into the base. In fact, the neutral base thicknesses (in C40, C28, C28FD and C14FD) in approach 2 are increased compared to those in approach 1 (see Figure 3-20 and Figure 3-23). Additionally,  $f_{\text{T}}$  increases at low current densities, while maintaining the peak  $f_{\text{T}}$  values reported in the previous approach. The processes with two lowest thermal budgets C40 and C14FD reach 370 GHz and 365 GHz peak  $f_{\text{T}}$  respectively for a lower  $R_{\text{Bi0}}$  (TABLE 3-2).

TABLE 3-2. Obtained electrical performances for the assumption of identical base-emitter capacitance

Nodes	B55-2D	B55-1D	C40-1D	C28-1D	C28FD-1D	C14FD-1D
$C_{jC0}$ (fF/ $\mu$ m <sup>2</sup> )	2.7	2.89	3.20	3.11	3.07	3.19
$C_{\rm jE0}~({\rm fF}/{\rm \mu m^2})$	7.21	7.06	7.06	7.06	7.06	7.06
$R_{\rm sB0}$ (k $\Omega$ /sq)	5.3	4.49	5.18	4.85	4.76	5.02
$f_{\rm T}$ (GHz)	325	330	370	356	352	365



Figure 3-21. Vertical profiles after tuning the SiGe layer and Si capping thicknesses to fix identical  $C_{jEi}$  a) Arsenic, b) Boron, c) Germanium, d) As-B profiles of B55 and C14FD



Figure 3-22. Electrical performances obtained by 1D device simulation in the case of fixing identical  $C_{\rm jEi}$  to 7.06 (fF/ $\mu$ m<sup>2</sup>) for a)  $C_{\rm jCi}$ , vs  $C_{\rm BC}$ , b)  $C_{\rm jEi}$  vs  $V_{\rm BE}$ , c)  $R_{\rm sBi}$  and d)  $f_{\rm T}$  vs  $J_{\rm C}$ 



Figure 3-23. Normalized neutral base thickness corresponding to different nodes by the assumption of identical  $C_{iE0}$ 

#### **3.7** A roadmap running parallel to the ITRS one

Figure 3-24 presents a comparison of  $f_{\rm T}$  performance vs. the metallurgical base width ( $W_{\rm Bm}$ ) between the roadmaps coming from the ITRS [12], [89] and the approach 2 in section 3.6.2. Obviously, although obtained results in section 3.6.2 exhibits the  $f_{\rm T}$  increase of ~16% in C40, ~10% in C28 and C28FD as well as ~14% in C14FD compared to that in B55, these  $f_T$  values are still far away from the  $f_T$  performances obtained from N<sub>2</sub>, N<sub>3</sub>, N<sub>4</sub> and N<sub>5</sub>. In fact, this study only evaluated the impact of the thermal budget for an existing vertical profile obtained from the B55, and these modified profiles employed in C40, C28, C28FD and C14FD were sole optimized to take the benefit of the thermal budget reduction. Moreover, the thermal budget is not only an element playing a role in the  $f_{\rm T}$  performance evaluation of SiGe HBTs. The engineering base profile and the increase of the doping level, especially an increase of the collector doping, that usually goes along with the scaling from one note to the next will be required to investigate thoroughly in the next Si/SiGe BiCMOS generation. These As, B and Ge doping profiles require to follow the ones presented in the ITRS [12], [89]. Indeed, the big difference of the  $f_{\rm T}$  performance between ITRS (N<sub>2</sub>, N<sub>3</sub>, N<sub>4</sub> and N<sub>5</sub>) and the approach 2 is from the collector doping profile. Therefore, in order to enhance the  $f_{\rm T}$  performance greater than 400 GHz, the collector doping profile is increased in the 28-nm FD-SOI BiCMOS generation presented in chapter 4 and will be optimized in the section 4.4.7.



Figure 3-24. A comparison of  $f_T$  performance between the ITRS and the approach 2

## 3.8 Conclusion

The evolution of dopants diffusion after each main process steps through the study of the thermal budget partitioning has been investigated. From this study, we found a high impact of the thermal budget during the Polyreox process. This exploration opens a new door to make a thinner base to enhance the  $f_{\rm T}$  and  $f_{\rm MAX}$  performances by the following steps: (i) replacing the Polyreox by TEOS oxide deposition with lower process temperature, (ii) thinning the Si-cap to bring the As profile in the emitter closer to the boron profile, and (iii) increasing the poly-base doping to compensate the increase of  $R_{\rm BX}$  due to the lower thermal budget. The obtained results of 365 GHz  $f_{\rm T}$  and 404 GHz  $f_{\rm MAX}$  are a promising performance for the high-speed SiGe HBT device with the DPSA-SEG architecture.

In the second part of this chapter, an impact study of the process thermal budget of advanced CMOS nodes on the performance of SiGe HBT is presented. The results show that  $f_T$  of SiGe HBT will benefit from the reduction of the thermal budget. The best approach is to target identical  $C_{jEi}$  since it leads to an  $f_{T,peak}$  at lower  $J_C$  and lower  $R_{Bi}$  benefiting to  $f_{MAX}$ . It also exhibits that, for doping levels comparable to those in B55, the  $f_T$  increase is moderate ~16% in C40, ~10% in C28 and C28FD as well as ~14% in C14FD.

This chapter provided a useful complement to the ITRS roadmap with respect to the BiC-MOS integration by highlighting how process thermal budget may limit the engineering of the vertical profile. More especially, it is interesting to note that a reduction of the spike annealing temperature below 1000°C does not further reduce the base width. Indeed, boron diffusion is then dominated by the thermal budget of the base epitaxy itself, highlighting the need to reduce the thermal budget of this operation.

Nevertheless, lowering the process thermal budget also means a reduction of the boron diffusion from extrinsic-to-intrinsic base leading to an increase of the base link resistance (see section 3.4), hence the increase of poly-base doping is required. The choice of the transistor architecture presented in chapter 4 will, therefore, remain a key element for  $f_{MAX}$  enhancement in the next Si/SiGe BiCMOS generation.

Results presented in this chapter contributed to the publication at the BCTM-2015 [71].

## Chapter 4 SiGe HBT architecture for 28-nm FD-SOI BiCMOS

### 4.1 Introduction

Obviously, the SiGe HBT architecture is a central element for  $f_{MAX}$  performance improvement. Over the last decade, several companies have chosen the solution to develop a new SiGe HBT architecture for their electrical performances enhancement when moving to the next technology node. For examples: IBM moved from the raised extrinsic base architecture [3] to the silicon link region between the intrinsic base and extrinsic base architecture [7] in 2014. IMEC moved from the usage of the single poly quasi-self-aligned architecture [48], [49] to the "G1G" architecture [52] in 2007. Although IHP has gathered outstanding records of electrical performance (570 GHz  $f_{MAX}$  [6] and 720 GHz  $f_{MAX}$  in IEDM-2016) with the EEB architecture. They try to further improve the  $f_{MAX}$  performance using the EBL architecture as presented in 2011 [11]. In fact, this architecture performed an impressive performance of 500 GHz  $f_{MAX}$  in DOTSEVEN [6] and has been investigated at IFX in the IFX-IHP cooperation. At STMicroelectronics (ST), the double-polysilicon quasi-self-aligned architecture in BiCMOS9 [90] was replaced by the conventional DPSA-SEG in BiCMOS9MW [4]. Although this architecture exhibits state-of-the-art performances of 320 GHz  $f_{T}$  and 370 GHz  $f_{MAX}$  in the 55-nm BiCMOS node, the  $f_{MAX}$  performance is still far away from the 570 GHz  $f_{MAX}$  obtained at IHP. In fact, ST's 370 GHz f<sub>MAX</sub> achieves the objective of the BiCMOS055 project but is not as high as the ones aforementioned at IHP. This is primary due to a large extrinsic base resistance that is the main limitation of this architecture. Therefore, in order to ensure ST to be at the forefront in the international competition when introducing the next Si/SiGe BiCMOS node, we propose a series of novel SiGe HBT architectures overcoming the limitations of the conventional DPSA-SEG one. The most promising architecture will be chosen for the next Si/SiGe BiCMOS generation at ST.

In this chapter, we also propose a new type of SiGe HBT architecture classification and deepen the investigation of a novel SiGe HBT architecture overcoming the limitations of the DPSA-SEG one. This investigation starts from previous results presented in section 1.4 and focuses on the impact of the constraints of nanoscale CMOS technologies [9]. The key concepts of the architecture chosen for the next Si/SiGe BiCMOS generation will be presented in more detail in section 4.3.3. This architecture is designed to be compatible with the 28-nm FD-SOI CMOS (C28FD) technology available at ST and to satisfy 400 GHz  $f_{T}$  and 600 GHz  $f_{MAX}$  in this node (i.e. between the N2 and N3 nodes simulated in [12]). In order to achieve this goal, the architecture is firstly evaluated and optimized by TCAD simulation before launching the fabrication process trials.

The first part of this chapter presents a new type of the SiGe HBT architecture classification in which current SiGe HBT architectures are classified based on the fabrication process flow and the relative positon level between the intrinsic and extrinsic bases. In the second part, we propose several new architectures. A novel fully self-aligned Si/SiGe HBT architecture using selective epitaxial growth and featuring an Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC) is chosen as the promising candidate for the next Si/SiGe BiCMOS generation. In addition, the fabrication process flow is presented in detail in this section 4.3.3. In the third part, electrical performances of the EXBIC architecture integrated into the bulk area part (called "NOSO" for No SOI) of the C28FD node are systematically evaluated by TCAD simulations. All the technological parameters of the architecture such as the boron in-situ doped base link, the emitter width and height, the pedestal oxide and sidewall thicknesses as well as the arsenic collector doping profile are thoroughly investigated. The results are discussed in the last section, where we also draw the conclusion about the best performance achievable with the EXBIC architecture.

## 4.2 SiGe HBT architecture classification

In order to develop novel SiGe HBT architectures, the understanding of the advantages and limitations of current architectures is a key driver to bring brilliant ideas coming from the world of imagination into the reality of manufacturing. Thus, the extensive exploration of different SiGe HBTs technology presented in chapter 1 becomes a precious source of information to classify their architectures.



Figure 4-1. Fabrication process flow for the self-aligned transistor using a) inner spacers and b) outer spacers

In the past, SiGe bipolar transistor structures can be roughly divided into non-self-aligned (or quasi-self-aligned) and self-aligned structures [27]. Non-self-aligned structures employ more masks than self-aligned structure. Particularly, the active region width is larger to compensate the lithography tolerance, hence always degrades the electrical performance of a transistor. Thus, this type of architecture is no longer used in advanced Si/SiGe BiCMOS technologies. A self-aligned structure normally implies that the extrinsic base is self-aligned to the emitter and the intrinsic base

of the transistor. This self-alignment is accomplished by the formation of the inner spacer (see Figure 4-1 a), or the outer spacer (see Figure 4-1 b) or both inner as well as outer spacers (see Figure 4-2). The self-aligned structure featuring the inner spacer usually comes with selective SiGe epitaxy (for example the conventional DPSA-SEG one). This type of architectures allows reducing the effective emitter width compared to emitter window width. By contrast, the non-selective SiGe epitaxy is usually applied in the self-aligned structure featuring the outer spacer. The limitation of the outer spacer structure is lateral scaling (it is difficult to reduce the effective emitter width). Therefore, the inner spacer, which is formed after the extrinsic base, is constructed sometimes to compensate this limitation (see Figure 4-2). However, the combination of both inner and outer spacers within one architecture results in a more complex fabrication process.



Figure 4-2. Self-aligned transistor using both the inner and the outer spacers

In this chapter, we propose a new kind of architecture classification that is established from the fabrication process flow. Analyzing the complex table of structural processing features of different SiGe architectures (see TABLE 4-1), these current architectures can be divided into three groups following the fabrication flow of the collector, intrinsic base, extrinsic base and emitter (see Figure 4-4).

- Group 1: Collector (C)  $\rightarrow$  Intrinsic base (IB)  $\rightarrow$  Extrinsic base (EB)  $\rightarrow$  Emitter (E)
- Group 2: Collector (C)  $\rightarrow$  Intrinsic base (IB)  $\rightarrow$  Emitter (E)  $\rightarrow$  Extrinsic base (EB)
- Group 3: Collector (C)  $\rightarrow$  Extrinsic base (EB)  $\rightarrow$  Intrinsic base (IB)  $\rightarrow$  Emitter (E)



Figure 4-3. The example of the sacrificial emitter structure

For the group 1, we can consider 4 current architectures such as the raised extrinsic base architecture in BiCMOS8HP [37], the silicon buffer link between extrinsic-intrinsic base architecture in BiCMOS9HP [7], the Towerjazz's architecture [59] and "G1G" architecture in IMEC-NXP [55].

The common feature coming with them is the non-selective SiGe epitaxy. Furthermore, this type benefits from the flavor of the sacrificial emitter [91]; the usage of the outer spacer coming with the sacrificial emitter module can assure the self-alignment between the extrinsic base and the emitter (see Figure 4-3). The vertical base link is used in BiCMOS8HP, BiCMOS9HP and Towerjazz, while the "G1G" structure uses the lateral base link.

For the group 2, we consider 2 architectures developed at IHP. These are the EEB and EBL architectures that have a common feature of using the sacrificial extrinsic base. This sacrificial layer was presented in detail in section 1.4.5. It is interesting to note that these architectures exhibit the state-of-the-art of  $f_{MAX}$  performances in the Si/SiGe BiCMOS technology. Finally, the rest of the architectures presented in TABLE 4-1 is in the group 3 where the DPSA-SEG architecture is well-known as a key member featuring the selective SiGe base epitaxy.

Structural features	Freescale [32]	Hitachi [34]	8XP [37]	9XP [7]	IFX [6]	IHP EEB [46]	IHP IFX [46]	IMEC [55]	Tower- Jazz [59]	ST [8]
Layout	CBEBC	BEBC	BEBC	BEBC	BEC	BEC	BEBC	BEC	BEBC	CBEBC
BC junction self-aligned with BE junction			Yes			No		Y	es	
Emitter is self-aligned with extrinsic base				Yes				No	Y	es
SiGe epitaxy	Selectiv	re (S)	Non-selec	tive (N-S)	S	N-S	S	N-S	N-S	S
Base link	Vertical	Vertical	Vertical	Vertical	Vertical	Vertical	Lateral	Lateral	Vertical	Vertical
Base link property	Poly-Si	Poly-Si	Si	Poly-Si	Poly-Si	Si	Si	Poly-Si	Poly-Si	Poly-Si
Emitter doping	As	Р	Р	Р	As	As	As	As	As	As
Collector module	N+ buried	N+ buried	N+ buried	N+ buried	N+ buried	Im- planted collector	N+ buried	Im- planted collector	N+ buried	N+ buried
$C \rightarrow IB \rightarrow EB \rightarrow E$			Yes	Yes				Yes	Yes	
$C \rightarrow IB \rightarrow E \rightarrow EB$				Yes	Yes					
$C \rightarrow EB \rightarrow IB \rightarrow E$	Yes	Yes			Yes					Yes

 TABLE 4-1. Structural processing features of different SiGe HBT architectures



Figure 4-4. SiGe HBT architectures classification

From a geometrical connection point of view, we realize that the relative position between extrinsic base level (EBL) and intrinsic base level (IBL) can be classified into 3 categories: (i) EBL contacts with IBL by a lateral interface (ii) the bottom face of the EBL overlaps with the top face of the IBL and finally (iii) the top face of the EBL overlaps with the bottom face of the IBL. The combination of the classification by the fabrication process and the relative position between the EBL and IBL can easily be visualized as nine SiGe HBT architecture diagrams presented in Figure 4-5, Figure 4-6 and Figure 4-7.



Figure 4-5. Fabrication process following the flow of C-IB-EB-E a) lateral base-link, b) the bottom of the EBL overlaps the top of the IBL and c) the bottom of the IBL overlaps with the top of the EBL



Figure 4-6. Fabrication process following the flow of C-IB-E-EB a) lateral base-link, b) the bottom of the EBL overlaps the top of the IBL and c) the bottom of the IBL overlaps with the top of the EBL



Figure 4-7. Fabrication process following the flow of C-EB-IB-E a) lateral base-link, b) the bottom of the EBL overlaps the top of the IBL and c) the bottom of the IBL overlaps with the top of the IBL

Following these diagrams, the current SiGe HBT architectures can be sub-divided as shown in the classification table (see in TABLE 4-2) and presented in detail below.

- The diagram in Figure 4-5 a) implies the "G1G" architecture in IMEC-NXP [55]
- The diagram in Figure 4-5 b) implies to the raised extrinsic base architecture in BiCMOS8HP [37], the silicon buffer link between extrinsic-intrinsic base architecture in BiCMOS9HP [7], and the architecture in Towerjazz [59]
- There are no architectures that are indicated in the diagram in Figure 4-5 c
- The diagram in Figure 4-6 a) implies the EBL architecture from IHP. A new one will be presented in detail in section 4.3.1 of this thesis
- The diagram in Figure 4-6 b) implies the EEB architecture from IHP. A new one will be presented in detail in section 4.3.1 of this thesis
- There are no architectures that are indicated in the diagram in Figure 4-6 c
- The diagram in Figure 4-7 a) implies the lateral base link architecture developed at IHP in 2008 [45] presented in section 1.4.5.2

- The diagram in Figure 4-7 b) implies the conventional DPSA-SEG architecture at Freescale [32], Hitachi [34], IFX [6] and ST [8]
- The diagram in Figure 4-7 c) implies 2 novel architectures to be presented in section 4.3.2 and section 4.3.3.

In fact, the ideas of setting the lateral base link and the vertical contact between the bottom of the EBL and the top of the IBL are existing in current SiGe HBT architectures (incl. EBL, EEB and DPSA-SEG architectures). But the vertical contact between the top of the EBL and the bottom of the IBL has never been presented in any patents or publications. Therefore, this idea involves novel architectures which will be presented in detail in section 4.3.2.

TABLE 4-2. Architecture classification table (white color: existing architectures, purple color: Non-existing architectures, olive green color: new architectures will be presented in this chapter)

Fabrication process flow	Lateral contact	The bottom of EBL con- tacts to the top of IBL	The top of EBL contacts to the bottom of IBL
C→IB→EB→E	G1G [55]	8HP [37], 9HP [7] and Towerjazz [59]	
	EBL [11]	EEB [46]	
C→IB→E→EB	A new architecture will be presented in Section 4.3.1 The EXBIC architecture will be presented in Section 4.3.2	• A new architecture will be presented in Section 4.3.1	
C→EB→IB→E	Lateral base link architec- ture was developed at IHP in 2008 [45] A new architecture will be presented in Section 4.3.2	DPSA-SEG architectures at Freescale [32], Hitachi [34], IFX [6] and ST [8]	A new architecture will be presented in Section 4.3.2 The EXBIC architecture will be presented in Section 4.3.2

## 4.3 New Si/SiGe HBT architecture

In this section, we are going to present potential Si/SiGe architectures that are developed based on proceeding diagrams shown in Figure 4-5, Figure 4-6 and Figure 4-7. By following these diagrams, several architecture candidates can be proposed. However, only the best five architectures are presented and discussed in this thesis.

## 4.3.1 A series of architectures following the C-IB-E-EB flow

Obviously, the type of C-IB-E-EB architectures permits achieving the best  $f_{MAX}$  performance in Si/SiGe BiCMOS technologies at the moment. Therefore, we deepen the investigation of such types of architectures. There are two new architectures proposed in this section.

For the architecture 1, the fabrication process flow is similar to the conventional DPSA-SEG presented in section 3.2. Particularly, it has to be noted that the poly-base deposited after the pedestal oxide deposition in the DPSA-SEG architecture is replaced by a sacrificial nitride layer. This layer will be removed after the emitter patterning. Then the extrinsic base and base link are formed by the combination of the selective epitaxy silicon and the non-selective epitaxial growth of boron doped silicon. This extrinsic base formation is similar to the one applied in the EBL architecture [41] at IHP. The monocrystalline silicon base link obtained by the selective epitaxy silicon can reduce  $R_{BX}$ , hence

enhances the  $f_{MAX}$  performance. However, this type of extrinsic base formation comes with the complexity in the fabrication because we need more specific treatment to remove the p<sup>+</sup> polysilicon covering the emitter and STI regions that are formed during the non-selective epitaxial growth of boron doped silicon. Therefore, we investigate an architecture 2 that is resolving the complexity of extrinsic base formation.



Figure 4-8. Architecture 1: Fully self-aligned architecture featuring the top of IBL overlaps the bottom of EBL

For the architecture 2, the fabrication process starts with the formation of the standard module shown in section 3.2. Collector areas are protected by an oxide layer. The fabrication continues with the formation of a thin non-selective silicon epitaxy / sacrificial oxide / nitride layers stack. An emitter window is opened by etching the nitride layer. Then, the cavity is formed by wet etching of the sacrificial oxide. The SiGe:C / Si-cap stack is grown selectively in this cavity. The in-situ arsenic doped emitter is formed after the L-shaped spacers. Next, the emitter is patterned, then outer spacers are added to protect the emitter. The sacrificial oxide is removed by wet etching and the extrinsic base is formed by the selective epitaxial growth of boron doped silicon. Finally, the fabrication is completed by extrinsic base patterning, spike annealing, silicidation and contact formation (see Figure 4-9).

As a short conclusion, this architecture has a simple fabrication process flow. Low  $C_{BC}$  can be obtained due to the usage of the standard collector module presented in B55 [8]. The extrinsic base can be formed by one step of the selective epitaxial growth of boron doped silicon. The extrinsic base formation is simpler than the one presented in the previous architecture.



Figure 4-9. Architecture 2: Fully self-aligned structure featuring the lateral base link

#### 4.3.2 A series of architectures following the C-EB-IB-E flow

The conventional DPSA-SEG architecture is the most famous representative of the C-EB-IB-E structure. This one employs the vertical base link featuring the overlap of the top of IBL with the bottom of EBL (see diagram Figure 4-7 b). In this section, we present further architectures that employ vertical base link featuring the overlap of the top of EBL with the bottom of IBL (see diagram Figure 4-7 c) and architectures coming with the combination between vertical and lateral base links.

Figure 4-10 shows a fully self-aligned structure featuring the overlap of the bottom of the IBL with the top of the EBL. The fabrication process starts with the implanted collector module. It continues with the deposition of an oxide layer/  $p^+$  poly-base / sacrificial oxide / nitride layer stacks. An emitter window is etched through these layers, stopping on the silicon substrate. Nitride sidewalls are formed inside the emitter window to protect the  $p^+$  poly-base then the intrinsic collector is formed by selective silicon epitaxy and SIC or arsenic in-situ doped silicon collector. Next, the SiGe:C/Si-cap stack is grown selectively inside the cavity that is formed by specific steps including (i) removing the nitride sidewall and (ii) wet etching the oxide layer (see Figure 4-11). The rest of fabrication process is similar to those in DPSA-SEG architecture (see in detail in section 3.2).



Figure 4-10. Architecture 3: Fully self-aligned structure featuring the overlap of the bottom of IBL with the top of EBL





b)

Figure 4-11. Specific steps form a) the cavity and b) the SiGe:C / Si-cap epitaxy base

The complicated formation of the base link during the selective epitaxial growth of borondoped SiGe:C is the main limitation of this architecture. Polysilicon base link and hidden defects, which can come into play during this formation, lead up to degrading the base link resistance, hence reducing the  $f_{MAX}$  performance. Therefore, this architecture is not chosen for the next Si/SiGe BiC-MOS generation. However, this architecture exhibits an interesting feature that the collector is isolated from the extrinsic base by nitride sidewalls.

For the architecture 4, Figure 4-12 presents a fully self-aligned structure featuring a lateral silicon link between extrinsic and intrinsic bases. This structure is integrated into the SOI region to benefit from the SOI sole leading to a fully mono-crystalline extrinsic base.



Figure 4-12. Architecture 4: Fully self-aligned structure featuring the lateral silicon link between extrinsic and intrinsic base

The fabrication process flow starts with the implantation of the highly-doped collector between two STIs. Arsenic is implanted through the BOX layer. It continues with the non-selective epitaxial growth of boron doped silicon and the deposition of oxide / nitride / oxide layer stack. An emitter window is etched through these layers and stops on silicon substrate. Nitride sidewalls are formed to protect extrinsic bases. Then the intrinsic collector, SiGe:C base and L-shaped spacers as well as the emitter are formed inside this window.

An interesting idea employing the lateral silicon base link to connect between the extrinsic and intrinsic base is presented in Figure 4-13. In fact, the emitter is protected by oxide spacers after the emitter patterning (see Figure 4-13 a). Then, sacrificial nitride layers and sidewall nitrides are removed by wet etching. Next, the lateral silicon base link is formed by the selective silicon epitaxy (see Figure 4-13 b). The rest of fabrication process is the same than the previous architecture.







c)

Figure 4-13. Lateral silicon base link formation between extrinsic and intrinsic base: a) before the sacrificial nitride and nitride sidewalls are removed and c) the selective silicon epitaxy is employed to form a silicon link between extrinsic and intrinsic bases

Finally, we introduce a fully self-aligned architecture Si/SiGe HBT architecture using selective epitaxial growth and featuring an Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC) (see Figure 4-14). This architecture employs both lateral and vertical base link and is the most promising candidate for the next 28-nm Si/SiGe BiCMOS technology at ST. A detailed fabrication process flow of this architecture will be presented in the next section.



Figure 4-14. Architecture 5: Fully self-aligned Si/SiGe HBT architecture using selective epitaxial growth and featuring an epitaxial extrinsic base isolated from the collector

## 4.3.3 Detailed fabrication process flow of the EXBIC architecture for BiCMOS028

The EXBIC architecture has been designed based on two key concepts. The first one is the boron in-situ doped epitaxial lateral base link used to reduce the extrinsic base link resistance. The second one is the oxide sidewalls isolating the intrinsic collector from the extrinsic base and prohibiting boron diffusion from extrinsic base into intrinsic collector. Additionally, the standard collector module (N-buried / Epitaxy / Deep Trenches / Sinker / Selectively Implanted Collector (SIC)) is

replaced by an implanted collector module (implanted collector / SIC) to comply with C28FD [8]. Because the architecture optimization is still ongoing, some material layers in the following description could be changed in the final device.

A cross-section of the EXBIC architecture is depicted in Figure 4-14. The fabrication starts with the implantation of the highly-doped collector between two shallow trenches (STI). It continues with the deposition of a pedestal oxide / p<sup>+</sup> poly-base / sacrificial & isolation layer stack (see Figure 4-15). It is noted that the boron doped poly-base is not mandatory. An emitter window is etched through these layers, stopping on Si, at the bottom of the pedestal oxide layer. Oxide sidewalls are formed inside the emitter window in which the intrinsic collector is formed by selective silicon epitaxy and SIC (see Figure 4-16). The Si/SiGe:C base stack is also grown selectively in this cavity (see Figure 4-17). Arsenic in-situ doped emitter is deposited after the formation of L-shaped spacers. Next, the emitter is patterned and sealed (see Figure 4-18). There are 2 ways to create the base link: (i) the sacrificial nitride layers are removed and left cavities are filled with boron in-situ doped epitaxy. Then, the sacrificial oxide layers are removed and the selective silicon epitaxy is employed to connect between the poly-base and the selective epitaxial growth of the boron doped base link. (ii) Both the sacrificial oxide and nitride layers are removed as shown in Figure 4-19 a. Then, the base links are formed by the selective epitaxial growth of the boron doped silicon (see Figure 4-19 b). Finally, the fabrication is completed by the opening of the collector areas, spike annealing, silicidation and contact formation (see Figure 4-14).

Collector, base and emitter of the EXBIC architecture are self-aligned and mono-crystalline (including the lateral base link). Oxide sidewalls between the extrinsic base and the intrinsic collector aim to get rid of the  $R_{BX}$ - $C_{BC}$  trade-off limiting many architectures, including the conventional DPSA-SEG one. Moreover, an interesting feature of the EXBIC architecture lies in its ability to be integrated either on the SOI or the NOSO areas of C28FD. In the case when the architecture is built on SOI, the pedestal oxide is formed by the buried oxide (BOX), which is 25-nm thick in C28FD, and the SOI layer is used as the extrinsic base sole, leading to a fully mono-crystalline extrinsic base. By contrast, the external part of the extrinsic base is polycrystalline when the architecture is built on NOSO but the thicknesses of the pedestal oxide and extrinsic base sole layers are not fixed, which gives more flexibility for device optimization. In the thesis, the SiGe HBT module is integrated onto the NOSO area.

Following the classification table presented in section 4.2, the EXBIC architecture has two options (see Figure 4-14 left). One can follow the type of C-EB-IB-E architecture if the  $p^+$  poly-base layer is employed (see Figure 4-15). By contrast, the EXBIC architecture will be classified as a type of C-IB-E-EB architecture if the  $p^+$  poly-base is replaced by a sole polysilicon layer and the selective epitaxial growth of the boron doped base link is applied.



Figure 4-15. A deposition of oxide / poly-base / oxide / polysilicon / oxide / nitride layers stack









Figure 4-16 a) emitter window opening and b) intrinsic collector formation



Figure 4-17. SiGe:C / Si-cap epitaxy







Figure 4-18 a) L-shaped spacers formation and in-situ arsenic doped emitter and b) emitter patterning



b)



c)

Figure 4-19 a) sacrificial polysilicon and nitride sidewall removals b) the growth of boron doped extrinsic base c) extrinsic patterning

## 4.4 BiCMOS028 architecture optimization

Both the vertical and lateral scaling of the EXBIC architecture have to be considered for its integration into C28FD technology. The height of the SiGe HBT is limited by the pre-metal dielectric (PMD) thickness, which is less than 200 nm, while the emitter width is targeted to be smaller than 100 nm as it is already the case in B55 [8]. Optimizing all the dimensions of the transistor together with the doping profiles is therefore extremely important before starting the hardware based process developments. Boron-doped base link, emitter width and height, pedestal oxide thickness and isolation sidewall thickness are thoroughly evaluated by TCAD simulations. The physical models used in *Sdevice* module of Synopsys<sup>®</sup> come from the TCAD deck calibrated in BiCMOS055 (see in initial part of section 2.3). Simulation results obtained with the 28-nm BiCMOS (B28) technology are compared to the ones obtained in B55 for 8.9-µm long transistors. By default, the doping of the epitaxial base link, emitter width and height, pedestal oxide and sidewall thickness are  $6 \times 10^{20}$  cm<sup>-3</sup>,  $W_{E0}$ ,  $t_{E0}$ ,  $t_{p0}$  and  $t_{w0}$  respectively (see dimensions reported in Figure 4-20).



Figure 4-20. TCAD cross-section of the EXBIC architecture

The vertical doping profile (incl. As, B, Ge) employed in B28 is shown in Figure 4-21. This profile is close to the one that comes from the "approach 2" presented in section 3.6.2, where the recipes used in B55 are tuned with respect to their thicknesses to account for the process thermal budget reduction in 28-nm FD-SOI. The arsenic collector profile in the approach 2 was obtained by the conventional  $n^+$  buried layer module. It is noticed that the collector doping in the B28 is higher than the reference one in order to enhance  $f_T$  performance. The B28's arsenic collector profile is formed by the implanted collector. Indeed, this profile is not yet fully optimized for the best performance of the HBT integrated into C28FD.



Figure 4-21. Arsenic, boron and germanium vertical profiles

#### 4.4.1 Boron-doped base link variation

The boron in-situ doped epitaxial lateral base link and the oxide sidewall between the extrinsic base and the intrinsic collector are key features which are expected to permit overcoming the  $C_{BC}$ - $R_{BX}$  trade-off in this architecture. The emitter width, emitter height and pedestal oxide thickness are  $W_{E0}$ ,  $t_{E0}$  and  $t_{p0}$  respectively, shown in Figure 4-20, and the doping of the epitaxial base link is varied between  $1 \times 10^{19}$  cm<sup>-3</sup> and  $8 \times 10^{20}$  cm<sup>-3</sup>. TCAD simulation results of key figures of merit are presented in TABLE 4-3.

As expected, oxide sidewalls are successful to avoid boron diffusion from the extrinsic base into the intrinsic collector. Base resistance  $R_{B0}$  is reduced by ~18% when the doping is increased from  $1 \times 10^{19}$  cm<sup>-3</sup> to  $8 \times 10^{20}$  cm<sup>-3</sup> while  $C_{BC}$  is unchanged. While the pinched base sheet resistance ( $R_{sBi}$ ) is close to the B55 one, the base resistance ( $R_{B}$ ) is reduced by approximately 55% in B28 due to both a better lateral base link and lateral scaling. The reduction of the extrinsic base link resistance ( $R_{BL}$ ) is only limited by the number of active boron atoms in relation to the total boron doping in the lateral base link as shown in Figure 4-23. As a consequence,  $f_T$  remains constant at 380 GHz while  $f_{MAX}$  is increased by ~19%.

Detailed TCAD simulations, presented in Figure 4-23, reveal that the intrinsic doping profiles can be changed due to the undesired diffusion of boron from the extrinsic base into the intrinsic base. This effect shortens by 15% the internal transistor width leading to higher  $C_{BE}$  and  $R_E$ . As can be seen in Figure 4-22, this diffusion is larger in the Si capping of the base than in the intrinsic collector region thanks to the carbon doping in the intrinsic base. Current gain ( $\beta$ ) benefits from the increase of extrinsic base doping.  $I_B$  is reduced (see in Figure 4-24), while a small variation of  $I_C$  is obtained. In fact, a larger extrinsic base doping results in a thinner space charge region (SCR) and less recombination in the peripheral region of this device, hence to the reduction of peripheral  $I_B$ current.

Doping (cm <sup>-3</sup> )	1×10 <sup>19</sup>	4×10 <sup>20</sup>	6×10 <sup>20</sup>	8×10 <sup>20</sup>	B55
$C_{\mathrm{BE0}}\mathrm{(fF)}$	10.2	10.8	10.8	10.9	14.4
$C_{\rm BC0}({ m fF})$	12.9	13.0	13.0	13.0	10.3
$R_{ m E0}(\Omega)$	1.62	1.69	1.69	1.69	1.92
$R_{\rm B0}(\Omega) (V_{\rm BE}=0)$	70.7	59.3	58.7	58.3	130
$R_{\rm BX}(\Omega.\mu m) (V_{\rm BE}=0)$	230	170	160	158	510
$R_{\rm sBi0}(\Omega/{\rm sq}) (V_{\rm BE}=0)$	5445	5554	5560	5563	5324
$\beta(V_{\rm BE}=0.6~{\rm V})$	835	1060	1080	1085	1950
$f_{\rm T}$ (GHz) ( $V_{\rm CB}$ =0.5V)	381	380	380	380	321
$f_{\text{MAX}}(\text{GHz}) (V_{\text{CB}}=0.5\text{V})$	700	820	830	835	370

TABLE 4-3. Obtained results for different doping of the epitaxial lateral base link



Figure 4-22. Boron diffusion from the selective epitaxial growth of boron doped silicon into the internal transistor



Figure 4-23. Horizontal active doping profiles for different epitaxial base link doping levels are measured along cutting line shown in Figure 4-22



Figure 4-24. The  $I_{\rm B}$  reduction due to the increase of extrinsic base doping

#### 4.4.2 Emitter width variation

Results shown in TABLE 4-4 refer to a variation of the emitter width  $W_{E0}$  of  $\pm 18\%$ . As expected, reducing  $W_{E0}$  is beneficial to  $R_B$ ,  $C_{BE}$  and  $C_{BC}$  and consequently  $f_{MAX}$  while  $f_T$  is degraded by the increase of the emitter resistance  $R_E$ . In fact, the variation of emitter width from  $1.18W_{E0}$  to  $0.82W_{E0}$  causes 27% increase of an emitter thickness measured from the emitter/Si-cap to the silicide/emitter interfaces (see Figure 4-25). The combination of the thickness increase and the emitter width reduction result in 33% increase of  $R_E$ , only 13% reduction of  $C_{BE}$  and 19% reduction of  $C_{BC}$ . In addition, the increased thickness can also increase the emitter transit time. Therefore, a decrease of 35 GHz in  $f_T$  is obtained from the reduction of emitter width thickness. The  $f_{MAX}$  is increased by ~100 GHz between the wider and the narrower emitter. This is mainly due to  $R_B$  and  $C_{BC}$  reductions of 19% and 6%, respectively. The  $R_E$  increase when shrinking the emitter width remains a limitation to device scaling that calls for innovative solutions to reduce the specific emitter resistance.



Figure 4-25. The comparison of emitter thickness between architectures varied different emitter widths

Electrical performance	$W_{\rm E0} - 0.18 W_{\rm E0}$	WE0	$W_{\rm E0} + 0.18 W_{\rm E0}$
$C_{\rm BE0}({ m fF})$	10.1	10.8	11.6
$C_{\rm BC0}({\rm fF})$	12.6	13.0	13.4
$R_{ m E0}(\Omega)$	1.91	1.69	1.44
$R_{ m B0}(\Omega)$	52.4	58.7	64.8
$R_{ m sBi0}(\Omega/ m sq)$	5561	5560	5562
$\beta(V_{\rm BE}=0.6 \text{ V})$	1017	1080	1145
$f_{\rm T}$ (GHz) ( $V_{\rm CB}$ =0.5V)	360	380	395
$f_{\text{MAX}}$ (GHz) ( $V_{\text{CB}}$ =0.5V)	882	830	778

 TABLE 4-4 Obtained results for different emitter widths

## 4.4.3 Emitter height variation

As mentioned earlier, the height of the SiGe HBT in C28FD must fit in ~200nm, including the contacts. Since the emitter contributes substantially to the transistor height, its height is reduced from  $t_{E0}$ , which is already much lower than 200 nm, to  $0.57t_{E0}$ . In order to investigate only the impact of the emitter thickness, it is assumed that a similar doping profile at the emitter-base junction can be obtained for the different cases under study. Practically, the thickness of the deposited As-doped emitter is not changed in the simulations and the emitter is then thinned down by dry etching before silicidation. The doping of the base link is kept at  $6 \times 10^{20}$  cm<sup>-3</sup>.

Doing so,  $C_{BE}$ ,  $C_{BC}$  and  $R_B$  do not change with the emitter height (see TABLE 4-5).  $f_T$  and  $f_{MAX}$  are not noticeably changed, while the  $\beta$  is degraded because of  $I_B$  increase. Actually,  $I_B$  is dominated by the recombination at the emitter contact, the metal/silicon interface acting as a fast recombination surface with a shallow emitter [92]. The minor increase of  $R_E$  can be neglected due to the accuracy of  $R_E$  extraction methodology.

Electrical performance	t <sub>E0</sub>	0.86×tE0	$0.71 \times t_{\rm E0}$	0.57×tE0
$C_{\rm BE0}({ m fF})$	10.8	10.9	10.9	10.9
$C_{\rm BC0}({\rm fF})$	13.0	13.0	13.0	13.0
$R_{ m E0}(\Omega)$	1.69	1.71	1.76	1.84
$R_{ m B0}(\Omega)$	58.7	58.6	58.6	58.6
$\beta(V_{\rm BE}=0.6 \text{ V})$	1080	1012	948	881
$f_{\rm T}$ (GHz) ( $V_{\rm CB}$ =0.5V)	382	383	385	386
$f_{\text{MAX}}(\text{GHz}) (V_{\text{CB}}=0.5\text{V})$	830	826	821	816

TABLE 4-5 Obtained results for different emitter heights

#### 4.4.4 Pedestal oxide thickness variation

Pedestal oxide thickness is expected to have a major impact on  $f_{MAX}$  through  $C_{BC}$  due to the implanted collector architecture (no shallow trench to isolate the collector from the extrinsic base). Emitter height, emitter width and base link doping are kept at  $t_{E0}$ ,  $W_{E0}$  and  $6 \times 10^{20}$  cm<sup>-3</sup> respectively, while pedestal oxide thickness is varied between  $0.4t_{p0}$  to  $2t_{p0}$ . This range is defined to investigate thicknesses not too far from the BOX thickness (25 nm).

The process simulations show that the As profile in the collector is modified when the SIC is kept identical because of the scaling of the epitaxial silicon collector thickness with the pedestal oxide thickness. The consequence is illustrated in Figure 4-26.  $C_{BC0}$  decreases dramatically by 43% when the pedestal thickness increases from  $0.4t_{p0}$  to  $2t_{p0}$ , without compromising  $C_{BE}$ ,  $R_B$  and  $R_E$  (emitter-base profile is not impacted).  $f_T$  and  $f_{MAX}$  increase by ~13% (+46 GHz) and ~11% (+82 GHz) respectively (see TABLE 4-6). It is interesting to note that  $f_T$  increase saturates above  $1.6t_{p0}$ , which is explained by the degradation of the collector resistance. For a given SIC, the increase of the pedestal oxide thickness to reduce  $C_{BC}$  is limited by a  $R_C$ - $C_{BC}$  trade-off impacting  $f_T$ . Therefore, it is essential to optimize again the As profile in the collector together with the pedestal oxide thickness.



Figure 4-26. As profiles with different pedestal oxide thicknesses for a given SIC TABLE 4-6 Obtained results for different pedestal oxide thicknesses

Electrical performance	$0.4 \times t_{p0}$	t <sub>p0</sub>	$1.2 \times t_{p0}$	1.6×t <sub>p0</sub>	$2 \times t_{p0}$
$C_{\rm BE0}({ m fF})$	10.9	10.8	10.8	10.8	10.8
$C_{\rm BC0}({\rm fF})$	19.5	13.0	12.3	11.6	11.1
$R_{ m E0}(\Omega)$	1.7	1.69	1.69	1.7	1.7
$R_{ m B0}(\Omega)$	58.6	58.7	58.7	58.8	58.9
$\beta(V_{\rm BE}=0.6~{\rm V})$	1044	1080	1082	1085	1087
$f_{\rm T}$ (GHz) ( $V_{\rm CB}$ =0.5V)	345	382	385	390	391
$f_{\text{MAX}}(\text{GHz}) (V_{\text{CB}}=0.5\text{V})$	780	830	840	847	862

#### 4.4.5 Sidewall thickness variation

As mentioned in section 4.3.3, the oxide sidewall is an advanced feature which aims at isolating the intrinsic collector from the boron diffusion coming from the extrinsic base. Thus we evaluate here the impact of the sidewall thickness on electrical performance. In practice, when the deposited sidewalls thickness is modified, it changes the emitter width, which could lead to the "emitter plug" effect, and sidewalls are over-etched during wet cleaning (if recipes are not adapted). Obtained performance would, therefore, be a mixture of several variations and the impact of the sole sidewall thickness would not be captured. To investigate only the thickness impact, an artifice in TCAD simulation is carried out: the over-etching of the sidewall is skipped and the sidewall thickness is modified from  $0.5t_{w0}$  to  $1.5t_{w0}$  at the end of the process simulation without changing the emitter width. The comparison between the two cases (with and without over-etching of the sidewalls), illustrated in Figure 4-27, shows that  $C_{BC}$  is slightly reduced (see TABLE 4-7) while  $R_B$  and  $C_{BE}$  are increased when over-etching is accounted due to the filling of the over-etched gaps by the boron-doped epitaxy. The variation of the sidewall thickness from  $0.5t_{w0}$  to  $1.5 t_{w0}$  exhibits only a slight  $f_T$  increase of ~3% (+10 GHz) due to a 7% reduction of  $C_{BC}$ . Both  $C_{BE}$  and  $R_B$  (especially base link resistance) get an increase due to the lengthening of the base link. Current gain ( $\beta$ ) benefits from the increase of the sidewall thickness is widened from  $0.5t_{w0}$  to  $1.5t_{w0}$ . This increase results from the peripheral  $I_B$  reduction due to the increase of the base link resistance and thinner spacer charger region in the peripheral region of this device.



Figure 4-27. Base link without over-etched (WOE) sidewall and b) Base link with over-etched (OE) sidewall TABLE 4-7 Obtained results for different sidewall widths (a comparison between with over-etching (OE) and without over-etching (WOE) is provided)

Electrical performance	<b>OE_0.5</b> × <i>t</i> <sub>W0</sub>	WOE_0.5×two	WOE_two	WOE_1.5×two
$C_{\rm BE0}({ m fF})$	10.7	10.3	10.7	10.8
$C_{\rm BC0}({\rm fF})$	13.6	13.5	13.0	12.6
$C_{\rm BC0}/A_{\rm E}({\rm fF}/{\rm \mu m^2})$	4.5	4.5	4.5	4.5
$R_{ m E0}(\Omega)$	1.6	1.6	1.55	1.52
$R_{ m B0}(\Omega)$	64.1	64.4	64.9	65.3
$\beta(V_{\rm BE}=0.6 \text{ V})$	1108	1240	1345	1414
$f_{\rm T}$ (GHz) ( $V_{\rm CB}$ =0.5V)	390	392	399	402
$f_{\text{MAX}}(\text{GHz}) (V_{\text{CB}}=0.5\text{V})$	770	755	754	753

#### 4.4.6 The silicidation on both the poly-base and the epitaxial lateral base link

An interesting feature of the EXBIC architecture lies in its ability to deposit the silicidation on the epitaxial lateral base link shown in Figure 4-28. In order to form this lateral link, outer oxide sidewalls are removed before the silicidation. Then the silicidation is carried out on both the polybase and the epitaxial base link. Obtained electrical performances presented in TABLE 4-8 show that this modification does not impact the performances. Only a small variation of  $C_{BC}$  and  $R_B$  is observed because of a thinner length of the epitaxial base link resulting from the modification during the silicidation. However, from the technological point of view, electric charges can move laterally through the epitaxial base link to the silicidation without a resistance from an interface between the poly-base and the epitaxial base link. It is noticed that hidden defects coming from practical process fabrication can come into play during this interface formation, hence degrade the base link property. Therefore, the base link presented in Figure 4-28 b) is better than the one presented in Figure 4-28 a). The base link simulated in this Sprocess TCAD is ideal with the absence of these hidden defects.



Figure 4-28. Architectures featuring the silicidation of a) the poly-base and b) both the poly-base and the epitaxial lateral base link

Electrical performance	Vertical silicide link	Both vertical and lateral silicide link
$C_{\rm BE0}({ m fF})$	10.8	10.8
$C_{\rm BC0}({ m fF})$	13.0	12.3
$R_{ m E0}(\Omega)$	1.69	1.69
$R_{ m B0}(\Omega)$	58.7	58.2
$\beta(V_{\rm BE}=0.6 \text{ V})$	1080	1000
$f_{\rm T}$ (GHz) ( $V_{\rm CB}$ =0.5V)	382	382
$f_{\text{MAX}}(\text{GHz}) (V_{\text{CB}}=0.5\text{V})$	830	845

TABLE 4-8 A comparison between vertical silicide link and vertical-lateral silicide link architectures

#### 4.4.7 Arsenic collector doping profile variation

The arsenic collector doping profile plays an important role in the vertical scaling strategy. The high collector doping profile is required to enhance  $f_T$  performance and results in a strongly reduced  $BV_{CEO}$ . Therefore, the collector doping profile is thoroughly investigated in this section. We propose a replacement of the intrinsic collector formation (incl. the selective epitaxy silicon + SIC) by the selective epitaxial growth of arsenic doped silicon. This process aims at a better control of the stiffness of the arsenic profile in the collector; hence the  $f_T$ - $BV_{CEO}$  relation can be optimized straightforwardly. In order to investigate the  $f_T$ - $BV_{CEO}$  relation, the usage of fully calibrated physical models is required. The electrical performances obtained from fully and partly calibrated physical models are compared as shown in the next section.

# 4.4.7.1 The electrical performances comparison obtained from partly and fully calibrated physical models

It has to be noticed that the BiCMOS055 TCAD calibration and the 28-nm FD-SOI BiCMOS projects were conducted in parallel. The fully calibrated physical models in the BiCMOS055 TCAD calibration were completed when the investigation of "the silicidation on both the poly-base and the epitaxial base link" presented in the previous section have been done. Therefore, the fully calibrated physical models obtained from the BiCMOS055 TCAD calibration is now used in BiCMOS028 from this section. These physical models used in the investigations of section 4.4.1 to 4.4.6 are partly calibrated. These partly calibrated models were presented in the initial part of section 2.3 and are represented as bellows:

- Hydro Dynamic (HD) parameters [68]
- Bandgap (BG) of SiGe structure [74] and bandgap narrowing (BGN) [75]
- Energy and relaxation time, mobility [70]
- Intrinsic carrier densities, saturation velocity [69]

- Default Shockley-Read-Hall (SRH), surface SRH and Auger recombination models from Synopsys TCAD [76]
- Default Lackner model for impact ionization from Synopsys TCAD [76]
- Default Schenk model parameters for the trap-assisted tunneling from Synopsys TCAD [76]
- Default Schenk model parameters for the band-to-band tunneling from Synopsys TCAD [76].



Figure 4-29. The comparison of I<sub>B</sub> and I<sub>C</sub> obtains from partly and fully calibrated physical device parameters



Figure 4-30. The comparison of  $f_{T}$  and  $f_{MAX}$  obtains from partly and fully calibrated physical models in Sdevice TABLE 4-9. A comparison of obtained electrical performances between the partly calibrated models and fully calibrated models in Sdevice

Electrical performance	Partly calibrated physical models	Fully calibrated physical models
$C_{\rm BE0}({ m fF})$	10.8	10.8
$C_{\rm BC0}({\rm fF})$	13.0	13.0
$R_{ m E0}(\Omega)$	1.69	1.69
$R_{ m B0}(\Omega)$	58.7	58.2
$R_{\rm sBi}(\Omega/{ m sq})$	5560	5528
$\beta(V_{\rm BE}=0.6 \text{ V})$	1080	580
$f_{\rm T}$ (GHz) ( $V_{\rm CB}$ =0.5V)	382	440
$f_{\text{MAX}}(\text{GHz}) (V_{\text{CB}}=0.5\text{V})$	830	741
$BV_{\text{CEO}}(\mathbf{V})$	1.95	1.57

The comparison of obtained electrical performances between the partly calibrated models and fully calibrated models in Sdevice shows that the obtained capacitances and resistances are not changed (see in TABLE 4-9). The main differences of obtained electrical performances between these models are the peak  $f_T$  and  $f_{MAX}$ , current gain and  $BV_{CEO}$ . The peak  $f_T$  obtained by the fully calibrated models is greater than the one obtained by the partly calibrated models. This is mainly due to the increase of the fitting parameter ( $\beta$ ) in the expression of the high-field mobility model (see in detail in section 2.3.2). The peak  $f_{MAX}$  obtained by the fully calibrated model is less than the one obtained by the partly calibrated model that is because of the impact ionization at high current (see in the section 2.3.4). Moreover, the current gain ( $\beta$ ) is reduced from 1080 to 580 (see in TABLE 4-9). This large difference is explained by the reduction of the life time (the fitting parameter ( $\gamma$ )) when the SRH model is calibrated in the section 2.3.3. In fact, the *I*<sub>B</sub> obtained from the fully calibrated models is increased as presented in Figure 4-29, while *I*<sub>C</sub> is not changed. Finally, the calibrated impact ionization results in a reduction of *BV*<sub>CEO</sub> from 1.95 V to 1.57 V (see in TABLE 4-9). The impact ionization phenomenon was presented in detail in section 2.3.4.

#### 4.4.7.2 Arsenic collector profile optimization

Coming back to the arsenic collector optimization, the fully calibrated physical models are employed in this investigation. Figure 4-31 shows different arsenic collector profiles in which the arsenic doping is varied in a range of  $1 \times 10^{18}$  cm<sup>-3</sup> to  $1.5 \times 10^{19}$  cm<sup>-3</sup> during the selective epitaxial growth of arsenic doped silicon. The base-collector (BC) metallurgical junctions are identical to the reference one as presented in Figure 4-31. The variation of arsenic collector doping does not impact the boron and germanium profiles. The boron-doped base link, emitter width, emitter height, pedestal oxide thickness and sidewall thickness are  $6 \times 10^{20}$  cm<sup>-3</sup>,  $W_{E0}$ ,  $t_{H0}$ ,  $t_{p0}$  and  $t_{p0}$ , respectively. The silicidation on the epitaxial lateral base link is not used in this investigation.



Figure 4-31. Arsenic profiles in the collector with different doping levels

Electrical performance 1×10 <sup>18</sup> (cm <sup>-3</sup> )		$5 \times 10^{18} (\text{cm}^{-3})$	1.5×10 <sup>19</sup> (cm <sup>-3</sup> )	Reference	
$C_{\rm BE0}({ m fF})$	10.9	10.9	10.9	10.9	
$C_{\rm BC0}({ m fF})$	10.9	14.1	15.8	13.0	
$R_{ m B0}(\Omega)$	51.3	56.7	59.0	58.7	
$R_{\rm sBi}(\Omega/{ m sq})$	4723	5213	5555	5528	
$\beta(V_{\rm BE}=0.6 \text{ V})$	940	622	680	580	
$f_{\rm T}$ (GHz) ( $V_{\rm CB}$ =0.5V)	310	429	490	440	
$f_{\text{MAX}}(\text{GHz}) (V_{\text{CB}}=0.5\text{V})$	1170	565	440	741	
$BV_{\text{CEO}}(V)$	1.9	1.3	1.0	1.57	

Obtained results presented in TABLE 4-10 show that the variation of arsenic collector doping profile does not impact the  $C_{BE}$ . The higher and steeper collector profile results in a thinner space charge region (SCR), hence increases the C<sub>BC</sub>. In addition, the higher and steeper collector profile also results in the thinner neutral base (NB) leading to the increase of ~18%  $R_{sBi}$  when the arsenic doping is increased from  $1 \times 10^{18}$  cm<sup>-3</sup> to  $1.5 \times 10^{19}$  cm<sup>-3</sup>. The thinner SCR and NB cause a transit time reduction in these regions. Therefore,  $f_T$  performance benefits from 58% increase (corresponding to 180 GHz, from 310 GHz to 490 GHz). In contrast, the higher doping collector can reduce the  $BV_{CEO}$ performance. In fact, this value is dropped from 1.9 V to 1.3 V and to 1.0 V when the collector doping is increased from  $1 \times 10^{18}$  cm<sup>-3</sup> to  $5 \times 10^{18}$  cm<sup>-3</sup> and to  $1.5 \times 10^{19}$  cm<sup>-3</sup>, respectively. In order to improve both the  $f_{\rm T}$  and  $BV_{\rm CEO}$  performances, the arsenic collector doping profile is optimized in the next part.

In order to enhance the  $f_{\rm T}$  and not degrade  $BV_{\rm CEO}$ , the selective epitaxial growth of arsenic doped silicon is built by two-step doping layers. The first step is doped by very high arsenic doping  $(4 \times 10^{19} \text{ cm}^{-3})$  while the second step is doped by low arsenic doping  $(1 \times 10^{17} \text{ cm}^{-3})$  to ensure a good  $BV_{\rm CEO}$  performance. To choose the best  $BV_{\rm CEO}$  performance, the thicknesses of these steps are varied and presented as following investigations.

- Collector 1: The first arsenic doping step is  $4 \times 10^{19}$  cm<sup>-3</sup> with the thickness of  $t_1=2/5$   $t_0$  and the second arsenic doping step is  $1 \times 10^{17}$  cm<sup>-3</sup> with the thickness of  $t_2=3/5$   $t_0$
- Collector 2: The first arsenic doping step is  $4 \times 10^{19}$  cm<sup>-3</sup> with the thickness of  $t_1=3/5$  t<sub>0</sub> and the second arsenic doping step is  $1 \times 10^{17}$  cm<sup>-3</sup> with the thickness of  $t_2=2/5$  t<sub>0</sub>
- Collector 3: The first arsenic doping step is  $4 \times 10^{19}$  cm<sup>-3</sup> with the thickness of  $t_1=4/5$   $t_0$  and the second arsenic doping step is  $1 \times 10^{17}$  cm<sup>-3</sup> with the thickness of  $t_2=1/5$   $t_0$ .



Figure 4-32. The selective epitaxial growth of arsenic doped silicon with two doping steps



Figure 4-33. Obtained vertical doping profile from the collector 1, 2 and 3

Figure 4-33 shows the arsenic collector doping profiles in this investigation. The variation of arsenic collector doping does not impact the boron and germanium profiles. The  $C_{\text{BE}}$  is the same than the previous investigation and is not impacted by the variation of arsenic collector doping. By keeping the low  $1 \times 10^{17}$  cm<sup>-3</sup> arsenic doping profile at the BC metallurgical junction, we achieve 436 GHz and 473 GHz  $f_{\text{T}}$  in the collector 1 and collector 2 (see TABLE 4-12), respectively. These values are greater than the 395 GHz  $f_{\text{T}}$  obtained from N<sub>2</sub>, which was presented in ITRS roadmap [12], while  $BV_{\text{CEO}}$  still reaches 1.73 V and 1.65 V, respectively. In the case of collector 3, the  $f_{\text{T}}$  can reach 506

GHz  $f_T$  that is greater than the 502 GHz obtained from N<sub>3</sub> [12], but the  $BV_{CEO}$  drops to 1.16 V that is much less than 1.55 V obtained from N<sub>3</sub>. These obtained results show that the arsenic collector profile optimization only is impossible to catch the N<sub>3</sub>'s electrical performances. Therefore, the arsenic profile in the emitter and boron as well as germanium profiles in the base are required to be optimized to get a better ( $f_T$ ,  $BV_{CEO}$ ) trade-off.

Electrical performance	Collector 1	Collector 2	Collector 3	Reference	
$C_{\rm BE0}({ m fF})$	10.9	10.9	10.9	10.9	
$C_{\rm BC0}({ m fF})$	11.5	13.0	15.6	13.0	
$R_{ m B0}(\Omega)$	48.6	51.6	56.7	58.7	
$R_{\rm sBi}(\Omega/{ m sq})$	4417	4733	5297	5528	
$\beta(V_{\rm BE}=0.6~{\rm V})$	500	545	640	580	
$f_{\rm T}$ (GHz) ( $V_{\rm CB}$ =0.5V)	436	473	501	440	
$f_{\text{MAX}}(\text{GHz}) (V_{\text{CB}}=0.5\text{V})$	1043	868	506	741	
$BV_{\rm CEO}$ (V)	1.73	1.65	1.16	1.57	

TABLE 4-11. Obtained electrical performance with different investigated collectors

#### 4.5 Discussion on 400 GHz $f_{\rm T}$ and 600 GHz $f_{\rm MAX}$ feasibility in 28-nm FDSOI

The results obtained in the previous section represent a strong base to choose the best geometrical parameters to further maximize ( $f_T$ ,  $f_{MAX}$ ) performance towards a target of (400, 600) GHz. Based on this work, the emitter width and height, pedestal oxide thickness, sidewall thickness and the doping of base link chosen for the B28 architecture are  $W_{E0}$ ,  $t_{E0}$ ,  $t_{p0}$ ,  $t_{w0}$  and  $6 \times 10^{20}$  cm<sup>-3</sup>, respectively. Particularly, the preferred arsenic collector profile can be the "collector 2" presented in the previous section. The comparison to B55 presented in TABLE 4-12 exhibits ( $R_E + R_B$ ) and  $C_{BE}$  reductions of 43% and 25% respectively. 473 GHz  $f_T$  and 868 GHz  $f_{MAX}$  are obtained in B28. As shown in Figure 4-35, peak  $f_T$  and  $f_{MAX}$  values obtained in B28 are reached at a larger collector current density compared to the ones obtained in B55. The collector current density for a given  $V_{BE}$  is similar between B28 and B55, while a higher base current density in the B28 compared to the one in B55 is observed in Figure 4-34. The  $BV_{CEO}$  of 1.65 obtained in B28 is better than the one obtained in B55. The main reason comes from the better-optimized collector thanks to the given flexibility by the selective epitaxial growth of arsenic doped silicon (see in detail in the previous section) and from a low current gain.



Figure 4-34. (I<sub>B</sub>, I<sub>C</sub>) comparison between B28 and B55



Figure 4-35. ( $f_T$ ,  $f_{MAX}$ ) comparison between B28 and B55

TABLE 4-12. Comparison between B55 and B28 for the optimized architecture

	$C_{\rm BE0}/L_{\rm E}$	$C_{\rm BC0}/L_{\rm E}$	$(R_{\rm E}+R_{\rm B}) \times L_{\rm E}$ At peak $f_{\rm T}$	$R_{\rm BX} \!  imes \! L_{\rm E}$	<b>BV</b> CEO	$f_{ m T}$	fмах
Unit	fF/µm	fF/µm	Ω.µm	Ω.µm	V	GHz	GHz
B55	1.62	1.17	132	505	1.5	325	473
B28	1.22	1.5	75	160	1.65	473	868

Inevitably the performances (and more especially  $f_{MAX}$ ) reported in this study raise the question of the TCAD accuracy even if physical models were carefully calibrated in chapter 2. 473 GHz  $f_{T}$  is easily explained by the low parasitic capacitances and resistances featured by the EXBIC architecture combined with the reduced process thermal budget [71]. 868 GHz  $f_{MAX}$  may look very optimistic but is consistent with the 68% reduction of  $R_{BX}$  compared to B55. Moreover, normalized  $C_{BC}$  and ( $R_B+R_E$ ) of the EXBIC architecture are in agreement with those published in [13] for an architecture featuring an epitaxial base link too. On the other hand, the base link simulated in TCAD is ideal with the uniformity of the silicon link and the absence of defects coming from practical process fabrication. As a consequence, the calibration of the base link resistance on measured data will be required to refine  $f_{MAX}$  values. Simultaneously, the validity of the physical models used in *Sdevice* will require to be verified as it is required for every new technology node [85], [12]. However, these results give confidence in the feasibility of a 400 GHz  $f_T$  and 600 GHz  $f_{MAX}$  Si/SiGe HBT in a 28-nm FD-SOI BiCMOS.

### 4.6 Conclusion

In this final chapter, we have proposed a new SiGe HBT architecture classification based on the fabrication process flow. The combination of this classification and the relative position level between the intrinsic and extrinsic bases results in nine diagrams and an architecture classification table that enables the classification of current architectures and to develop new architectures. Four new architectures have been proposed in this chapter. It is noticed that the EXBIC architecture is the most promising candidate for the next Si/SiGe BiCMOS generation.

The EXBIC architecture has been studied and optimized by TCAD simulation in the 28-nm FD-SOI CMOS node. The key features of this EXBIC architecture are an epitaxial boron in-situ doped lateral base link and oxide sidewalls isolating the collector from the extrinsic base. Low  $R_{BX}$  and  $C_{BC}$  values are reported with no trade-off in between. In addition, the arsenic collector profile is optimized by employing the selective epitaxial growth of arsenic doped silicon. The low doping level at the metallurgical BC junction and a higher doping level close to the n<sup>+</sup> silicon layer aim at resolving

the  $f_{\rm T}$ - $BV_{\rm CEO}$  trade-off (see in detail in section 4.4.7). Peak  $f_{\rm T}$  and  $f_{\rm MAX}$  values of 473 GHz and 868 GHz respectively are forecasted in a 28-nm FD-SOI BiCMOS technology demonstrating the potential of the EXBIC architecture and giving confidence in the feasibility of a 400 GHz  $f_{\rm T}$  and 600 GHz  $f_{\rm MAX}$  Si/SiGe HBT.

Results presented in this chapter contributed to the publication at the BCTM-2016 [24].

## **General conclusion**

The main goal of this thesis was the exploration and evaluation of a novel architecture for the 28-nm Si/SiGe FD-SOI BiCMOS technology by TCAD simulation targeting to 400 GHz  $f_{T}$  and 600 GHz  $f_{MAX}$  in this technology node. On the road to reach this objective, several studies were carried out resulting in remarkable findings. These results are summarized below.

In chapter 1, the Si/SiGe BiCMOS technologies realized by different companies is presented. The comparison between the different SiGe HBT architectures is synthesized in a table form. Both the advantages and limitations are clarified for the different architectures. This synthesis is strong base to explore new SiGe HBT architectures.

Both the fabrication process and physical device calibration for the DPSA-SEG architecture in the 55-nm Si/SiGe BiCMOS are presented in chapter 2. Not only the vertical profiles and the base link calibration is mentioned, but also for the first time all physical models including the band-gap narrowing, mobility, SRH recombination, impact ionization, distributed emitter resistance, selfheating, TAT and B2B tunneling have been simultaneously worked out. In addition, this chapter also presents an effective way to calibrate physical models in any Si/SiGe BiCMOS technology nodes.

The impact of the process thermal budget is studied in chapter 3. The evolution of dopants diffusion after each main fabrication process steps is presented. The thermal budget during the STI formation results in the large arsenic diffusion from the  $n^+$  buried layer into the collector epitaxy. This thermal budget plays an important role on the collector profile, influencing directly the base-collector capacitance and the collector resistance. From the study of the thermal budget partitioning, we also found a high impact of the thermal budget during the Polyreox process. This exploration opens a new door to make a thinner base to enhance the  $f_T$  and  $f_{MAX}$  performances by the following steps: (i) replacing the Polyreox by TEOS (oxide) deposition with lower process temperature, (ii) thinning the Si-cap to bring the As profile in the emitter closer to the boron profile, and (iii) increasing the polybase doping to compensate the increase of  $R_{BX}$  due to the lower thermal budget. The obtained result of 365 GHz  $f_T$  and 404 GHz  $f_{MAX}$  is an interesting performance for the high-speed SiGe HBT device with the DPSA-SEG architecture.

More especially, it is interesting to note that a reduction of the spike annealing temperature below 1000°C does not further reduce the base width. Indeed, boron diffusion is then dominated by the thermal budget of the base epitaxy itself, highlighting the need to reduce the thermal budget of this operation.

In the second part of chapter 3, an impact study of the process thermal budget of advanced CMOS nodes on the performance of SiGe HBT is presented. The results show that  $f_T$  of SiGe HBT will benefit from the reduction of the thermal budget. The best approach is to target identical  $C_{jEi}$  since it leads to a  $f_T$  at lower  $J_C$  and lower  $R_{Bi}$  benefiting to  $f_{MAX}$ . It also exhibits that, for doping levels

comparable to those in B55, the  $f_T$  increase is moderate ~16% in C40, ~10% in C28 and C28FD as well as ~14% in C14FD.

Finally, this chapter provides a useful complement to the ITRS roadmap with respect to the BiCMOS integration by highlighting how process thermal budget may limit the engineering of the vertical profile. The comparison between two roadmaps shows that the  $f_T$  obtained from approach 2 (in section 3.6.2) is still far away from the  $f_T$  performances received from N<sub>2</sub>, N<sub>3</sub>, N<sub>4</sub> and N<sub>5</sub> in ITRS. The reason lies mainly in the collector doping which is much larger in the ITRS roadmap. In addition, the base profile is carefully optimized in this roadmap.

The final chapter can be considered as the heart-piece of this thesis. We have proposed a new SiGe HBT architecture classification that was established based on the fabrication process flow. The combination of this classification and the relative position level between the intrinsic and extrinsic bases presents nine diagrams and an architecture classification table that are a strong foundation to classify current architectures and develop new architectures. Five novel architectures were proposed in this chapter. It is noticed that the EXBIC architecture is a promising candidate for the next Si/SiGe BiCMOS generation.

The EXBIC architecture has been studied and optimized by TCAD simulation in the 28-nm FD-SOI CMOS node. The key features of this EXBIC architecture are an epitaxial boron in-situ doped lateral base link and oxide sidewalls isolating the collector from the extrinsic base. Low  $R_{BX}$  and  $C_{BC}$  values were reported with no trade-off in-between. In addition, the arsenic collector profile was optimized by employing the selective epitaxial growth of arsenic doped silicon. The low doping step at the metallurgical BC junction and a higher doping step being close to the silicon substrate aim at relaxing the  $f_{T}$ -BV<sub>CEO</sub> trade-off. Peak  $f_{T}$  and  $f_{MAX}$  values of 470 GHz and 870 GHz respectively are forecasted in a 28-nm FD-SOI BiCMOS technology and the BV<sub>CEO</sub> of 1.65 V is the same with the one obtained from N<sub>2</sub> in ITRS. These results demonstrate convincingly the potential of the EXBIC architecture and give confidence in the feasibility of a 400 GHz  $f_{T}$  and 600 GHz  $f_{MAX}$  the Si/SiGe HBT in the 28-nm FD-SOI BiCMOS.
## Perspectives

In order to enhance the  $f_{\rm T}$  performance, the vertical profiles can be optimized as suggested.

- To enhance the  $f_{\rm T}$  performance while not too much degrading  $BV_{\rm CEO}$ , the optimization of the arsenic profile in the emitter and boron, as well as germanium profiles in the base, are needed. These profiles can follow the vertical profiles presented in N<sub>3</sub> and N<sub>4</sub> from the ITRS roadmap [12].
- The combination of arsenic and phosphorous implantation in the implanted collector module can be a solution to reduce the extrinsic collector resistance; hence can improve the  $f_{\rm T}$  performance.
- In order to increase the extrinsic collector doping, a high doping of the implanted collector module can be carried out before the STI formation. This work is very similar to what we did for the conventional n+ buried module in the B55. It is noticed that the collector epitaxy formed after the high arsenic doping implantation in the conventional n+ buried module is not included in this collector formation.

In order to enhance the  $f_{MAX}$  performance, further EXBIC architecture optimization can be carried out as suggested below.

- The complexity of EXBIC architecture presented in this thesis is one of the limitations. Therefore, a simplification of the fabrication process flow is required. In fact, this simplification is actually ongoing by A. GAUTHIER who is a Ph.D student at ST.
- The link area between extrinsic and intrinsic bases should be thoroughly investigated to keep a low base link resistance; hence the  $f_{MAX}$  performance can be enhanced.
- The silicidation on both the poly-base and the epitaxial lateral base link can be employed for further resistance reduction.
- The EXBIC architecture can be integrated onto the SOI area to benefit from the fully monosilicon extrinsic base.
- Further investigations of the "architecture 2: Fully self-aligned structure featuring the lateral base link", which is presented in Figure 4-9, require to be carried out. This architecture is also a promising candidate for the next Si/SiGe BiCMOS technology at ST. However, the EXBIC architecture is still the first candidate for the BiCMOS028.

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## **Author's Publications**

- <u>V.T. Vu</u>; T. Rosenbaum; O. Saxod; D. Celi; T. Zimmer; S. Fregonese; P. Chevalier, "Impact study of the process thermal budget of advanced CMOS nodes on SiGe HBT performance", BCTM, 2015, pp. 76-79.
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- [5] <u>V.T. Vu</u>; D. Celi; T. Zimmer; S. Fregonese; P. Chevalier, "Advanced Si/SiGe HBT architecture for 28-nm FD-SOI BiCMOS", BCTM, 2016, pp. 64-67.

## **Publications in preparation**

- [6] <u>V.T. Vu</u>; D. Celi; T. Zimmer; S. Fregonese; P. Chevalier, "TCAD of high-speed Si/SiGe HBT- Part I: 55-nm BiCMOS calibration", IEEE TED, to be submitted.
- [7] <u>V.T. Vu</u>; D. Celi; T. Zimmer; S. Fregonese; P. Chevalier, "TCAD of high-speed Si/SiGe HBT- Part II: Toward 28-nm FD-SOI BiCMOS", IEEE TED, to be submitted.