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# Design of millimeter wave VCO based on slow-wave transmission lines

Ekta Sharma

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## **THÈSE**

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Préparée au sein du **Laboratoire IMEP-LAHC**  
dans **l'École Doctorale Electronique, Électrotechnique,  
Automatique et Traitement du Signal**

## **Conception de VCO millimétriques à basé de lignes de transmission à ondes lentes**

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## INTRODUCTION

The need of high-data-rate systems to answer the demand for big data exchanges has pushed the electronics systems to millimeter-wave (mm-wave) frequency bands. High-data-rate communications, radars, security, and medical applications are concerned by the development of millimeter-wave systems.

In the vicinity of 60 GHz, a 5 GHz band between 59 and 64 GHz was defined for unlicensed use in the countries where the consumer electronic market was the most developed. For very high data rate applications, i.e. wireless local area networks (WLANs) or wireless personal area networks (WPAN), this spectrum is an interesting option. Also, the millimeter-wave radiations are capable of penetrating clothes while being partially reflected by human skin. Millimeter-wave imagers are considered as a superior alternative as compared to traditional metal detectors, since the reflection pattern of metals, plastics, ceramics and liquids are detectable quickly for radiation at these frequencies. Hence, the security domain constitutes one of the major areas for millimeter-waves imaging systems. The frequencies better suited to this use are 35, 94, 140, and 220 GHz, which correspond to the atmospheric propagation windows, e.g. to the minima observed in terms of atmospheric attenuation. In the past, 94 GHz systems were usually adopted, but higher frequencies, leading to even better spatial resolutions, are under study.

Among millimeter-wave frequency band the 71-76 and 81-86 GHz bands (widely known as "E-band") are permitted worldwide for ultra-high capacity point-to-point communications. The 10 GHz of spectrum available represents by far the most ever allocated at any one time, enabling fiber-like gigabit per second (Gbps) and greater data rates that cannot be achieved at the bandwidth-limited lower microwave frequency bands. Also the E-band propagation characteristics are comparable to those at the widely used microwave bands, and with well characterized weather characteristics allowing rain fade to be understood, link distances of several miles can confidently be realized. For improving vehicle safety significant technological advances in the automotive industry have taken place as well. The radar system is capable of detecting and tracking objects, hence warning driver of an imminent collision. For long range radar there is a certain international consensus regarding the 76-77 GHz band whereas for short range such as anti-collision and handheld radars for parking assistance, pre-crash sensing, obstacle avoidance and blind spot detection the working frequency was fixed to 79 GHz. Here again, high spatial resolution is required and obviously the smallest antennas as possible.

All these millimeter-waves applications are commonly recognized to belong to and to lead to a smart society because they will facilitate the communications between people, inside or outside homes and offices, and from building to building (backhauling), avoiding heavy civil engineering infrastructure.

The rapid growth in global communications networks has driven the demand for high-performance communications systems that are faster and consume less power. The advanced CMOS-BiCMOS technologies are the preferred technologies to develop these future applications/systems. They offer relative low-cost, as compared to AsGa technologies, and high performance, with transistors  $f_{max} - f_t$  higher than 300 GHz.

Due to their crucial role in a wide variety of modern applications, PLL frequency synthesizers have been the subject of extensive research in recent years. In particular, the synthesizer requirements imposed by the targeted applications have been a key driver for PLL research. Specifically, stringent phase noise specifications provided considerable incentive for research solely focused on improving the voltage-controlled oscillator (VCO) performance, one of the most challenging aspects of PLL design. Power consumption, output power, frequency tuning range and chip area are also important subject of concern. As a result, there have been considerable advances in VCO and PLL design techniques and corresponding improvements in performance.

However, a predominant class of VCO utilizes lumped  $LC$ -tank that offers several disadvantages, i.e. high phase noise ( $PN$ ), reduced frequency tuning range ( $FTR$ ) and high power consumption ( $P_{DC}$ ), due to the low- $Q$  offered by lumped inductor and varactor. Thus, improvement in  $Q$ -factor of  $LC$ -tank or let's say in resonator of VCO is needed. Thanks to the high- $Q$  slow-wave transmission line (TL) that was proposed in 2003 by John Long<sup>1</sup>, the VCO design with improved performance can be obtained for targeted frequency band. A step by step procedure will be followed for designing the VCO based on slow-wave TL. Thanks to the recently developed equivalent electrical model by Alfredo Bautista in 2015<sup>2</sup>, the design and optimization of these slow-wave TL based resonator become faster and easier.

This thesis focuses on achieving wideband low-noise frequency synthesis, with a particular emphasis on wideband VCO design. In **chapter 1**, several applications available for mm-wave frequency band and the fundamentals to design the VCO are given. Also, a brief literature review is done to notice several design issues for implementing the VCO. A brief review of the utilized technology, i.e. BiCMOS 55 nm, is given as well, as this technology is being used for designing all the VCO of this thesis.

In **chapter 2** before starting up the oscillator design, a common VCO design methodology will be set down, which will be followed throughout the thesis. A conventional  $LC$ -tank VCO design will be presented. This VCO is designed to make a fair comparison with the proposed idea of using distributed elements (S-CPS) based oscillator. After this conventional  $LC$ -tank based VCO design, from next chapter 3 a step by step process will be followed to improve the VCO performance.

Then in **chapter 3**, the lumped inductor will be removed and instead a distributed inductor will be synthesized using S-CPS. For tuning the frequency same varactor set as used in chapter 2 VCO design will be utilized. This topology improves the VCO performance in terms of phase noise and power consumption. The obtained frequency tuning range is the same as VCO designed in chapter 2. This is due to the fact that the slow-wave effect also adds some capacitance to the resonator, hence not letting too much increment in frequency tuning range.

In **chapter 4** a new resonator topology will be utilized, i.e. an unsymmetric S-CPS based phase shifter, for designing the VCO. An unsymmetric S-CPS structure is proposed to reduce the added capacitance by slow-wave effect. The proposed topology is expected to show good performance in terms of phase noise and frequency tuning range as the loading effect of varactors is distributed along the length of S-CPS,

1. J. R. Long, "On-chip interconnect for mm-wave applications using an all-copper technology and wavelength reduction," in *IEEE Int. Solid-State Circuits Conf.*, San Francisco, 2003.

2. Bautista, A.; Franc A.-L.; Ferrari, P.; "An Accurate Parametric Electrical Model for Slow-wave CPW," in *Int. Microw. Symp.*, Phoenix, USA, 2015.

hence improved phase noise performance and frequency tuning range is expected. So in **chapter 5** the same unsymmetric resonator i.e. unsymmetric S-CPS based phase shifter will be considered, but with a distributed cross-coupled pair topology. This topology reduces the loading parasitic capacitance and hence improves the frequency tuning range. A new buffer-less mm-wave VCO design topology is proposed in chapter 5. Thanks to a careful choice of the output position any output impedance can be envisaged, thus avoiding the necessity of an output buffer, leading to wider tuning range and lower power consumption, small chip area and improved power efficiency.



# 1. VOLTAGE CONTROLLED OSCILLATOR FOR MM-WAVE APPLICATIONS

## 1.1 Mm-wave Applications

Mainstream commercial technologies are predominant at microwave frequencies, as they have reached into the mm-wave spectrum to take advantage of the looser regulations and the progressively faster and cost-effective silicon-based IC processes. There are many promising mm-wave commercial applications as described in Table 1.1.

Application	Description	Frequency band
Local Multipoint Distribution Service (LDMS) [1]	Terrestrial communications (1-4 miles)	20 – 40 GHz
Fiber-optic communications [2]	Long-haul terrestrial WAN communication networks (>40 Gbps)	20 – 40 GHz
Wireless HDMI [3]	Wireless high definition audio and video signals connectivity on consumer electronics products	57 – 64 GHz
60 GHz Radio [3]	WPANs: short haul high capacity traffic (> 1 Gbps)	57 – 64 GHz
Automotive radar [4]	Automotive cruise control (ACC)	76 – 77 GHz
Wireless backhaul application [5]	Ultra-high capacity point-to-point communication	71 – 76 GHz & 81 – 86 GHz
Imaging	Image scanning/detection systems	100 + GHz

Table 1.1: Millimeter-wave applications

Among all these applications the 71-76 and 81-86 GHz bands (widely known as “E-band”) are permitted worldwide for ultra-high capacity point-to-point communications. E-band wireless systems are available to offer full-duplex Gigabit Ethernet connectivity at data rates of 1 Gbps and higher in cost effective radio architectures, with carrier class availability at distances of a mile and beyond.

The significance of the e-band frequencies cannot be overstated. With 5 GHz of bandwidth available per channel, gigabit and greater data rates can be accommodated.

Let us notice that the characteristics of wireless propagation at E-band frequencies are only slightly different to those at the widely used lower frequency microwave bands that enables the transmission distances of many miles to be realized. The atmospheric attenuation of radio waves varies significantly with frequency, shown in Figure 1.1. At the microwave frequency bands of up to 38 GHz, the attenuation due to the atmosphere at sea level is low at 0.3 dB/km or less. A small peak is seen at 23 GHz, followed by a large peak at 60 GHz, corresponding to absorption by water vapor and oxygen molecules respectively. This effect at 60 GHz in particular, where absorption increases to 15 dB/km, significantly limits radio transmission distance at this frequency. Above 100 GHz, numerous other molecular absorption effects occur, limiting the effectiveness of radio transmissions. A clear atmospheric window can be seen in the spectrum from around 70 GHz to 100 GHz. In this area, low atmospheric attenuation around 0.5 dB/km occurs, close to that of the popular microwave frequencies, and

very favorable for radio transmission. For this reason, E-band wireless systems can transmit high data rate signal over many miles under clear conditions.

The more important parameter is free space path loss model, as it is used to predict received signal strength when transmitter and receiver have clear, unobstructed line of sight path between them. Free space path loss  $L_{dB}$  at distance  $d_{km}$  and frequency  $F_{GHz}$  can be calculated by eq. (1.1) [6]

$$L_{dB} = 92.4 + 20 \log (F_{GHz}) + 20 \log (d_{km}) \quad (1.1)$$

Under stable, well mixed atmospheric condition this free space attenuation is about  $\sim 130dB/km$  within 71 – 76 GHz band and  $\sim 131dB/km$  within 81 – 86 GHz band [6].

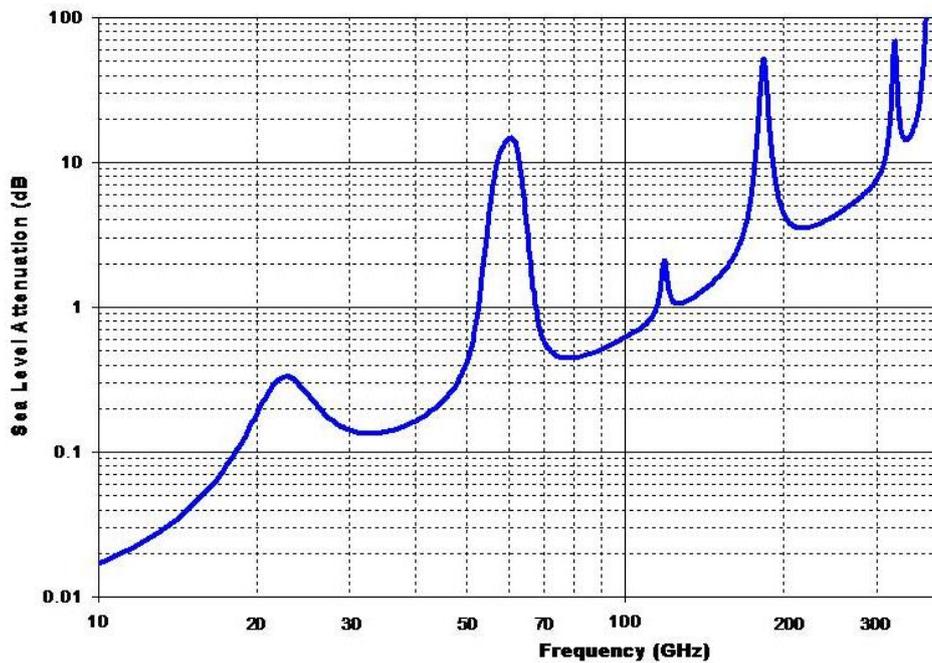


Figure 1.1: Atmospheric and molecular absorption [6]

Nearly all millimeter-wave applications (mentioned in Table 1.1) need an appropriate frequency reference to operate. The particular method used to synthesize such reference frequencies is determined by the specifications of the system. However PLL is the most popular system to synthesize frequencies since it allows tuning the operating frequency while achieving good noise performances. To make the PLL variable, a VCO is needed. It is the heart of the system. It is difficult to demonstrate explicit VCO specifications for each application as it strongly depends on the overall system design. Nonetheless, designers should expect stringent specifications on the VCO, which is a fundamental block in mm-wave wireless communication systems, Figure 1.2.

Based on current wireless communications systems, the 4 most important performance requirements of a mm-wave VCO in ultra-wideband radio systems are:

- Low VCO phase noise, which is often the most difficult and confounding property to optimize. A spectrally pure VCO is required for a dense channel spacing to efficiently utilize the available bandwidth.
- Sufficient output power to drive the mixer.

- Sufficiently wide tuning range to cover process variations, temperature variations, and frequency hopping schemes.

Power consumption is becoming more and more important parameter as mobile applications are targeted (for example with 5G).

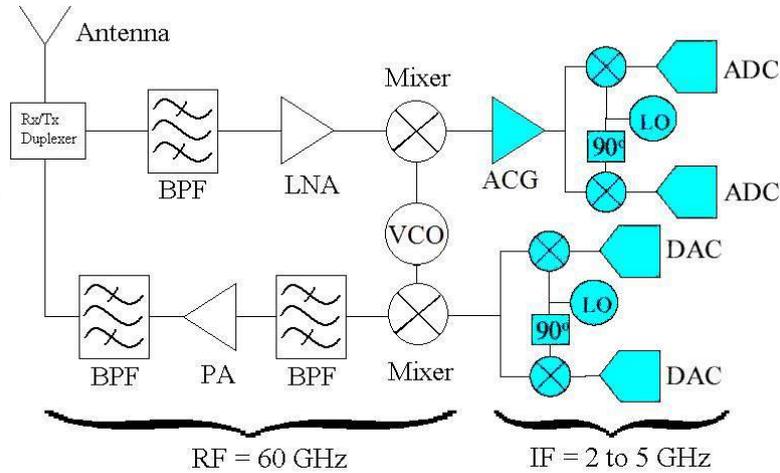


Figure 1.2: Block diagram of heterodyne RF front-end for 60 GHz radio.

Due to their crucial role in a wide variety of modern applications, VCO has been the subject of extensive research in recent years. The current trends clearly indicate a growing customer demand for faster data rates. Higher data rates are typically achieved by increasing the allocated channel bandwidth. Furthermore, cellular applications themselves are becoming multiband due to the growing number of standards that must be supported. While each frequency band is narrow, having a dedicated VCO covering each band can become very expensive as the number of bands increases. Instead, a single wideband VCO can be used to cover several bands. Hence, wideband tunable VCOs are becoming important in those applications. In light of the above trends, the main goal of this thesis is to develop new prototypes for wideband, i.e. wide enough to cover one entire band of E-band, low-noise frequency synthesis. In this thesis VCOs will be designed for frequency band of 81 – 86 GHz.

## 1.2 BiCMOS 55 nm Technology: An Overview

All the simulated and fabricated voltage controlled oscillators (VCO) in this thesis involve the Back End of Lines (BEOL) proposed by STMicroelectronics (STM) in the 55 nm BiCMOS technology, i.e. also called as B55. The B55 BEOL is specially addressed to mm-wave applications. A BEOL is adapted to mm-wave when it shows the minimum losses for 50Ω transmission lines [7]. Figure 1.3(a) compares different BEOL and Figure 1.3(b) is a SEM (scanning electron microscopy) picture of the 65 nm CMOS technology BEOL by STM.

The BEOLs in Figure 1.3(a) present at least three thick metal layers (M6, M7 and Alucap) in the upper levels. In the B55 technology, an eighth level (M8) of very thick metal is added before the aluminum cap. The thick layers in B55 (M6, M7 and M8) have the objective to reduce the resistive losses in the interconnections, which allows to realize low-loss passive structures. On the other hand, the dimensions of the lower layers (from M1 to M5) significantly decrease in terms of metal and dielectric thickness. Both lead to a decrease in the quality factor of the passive components built in these layers.

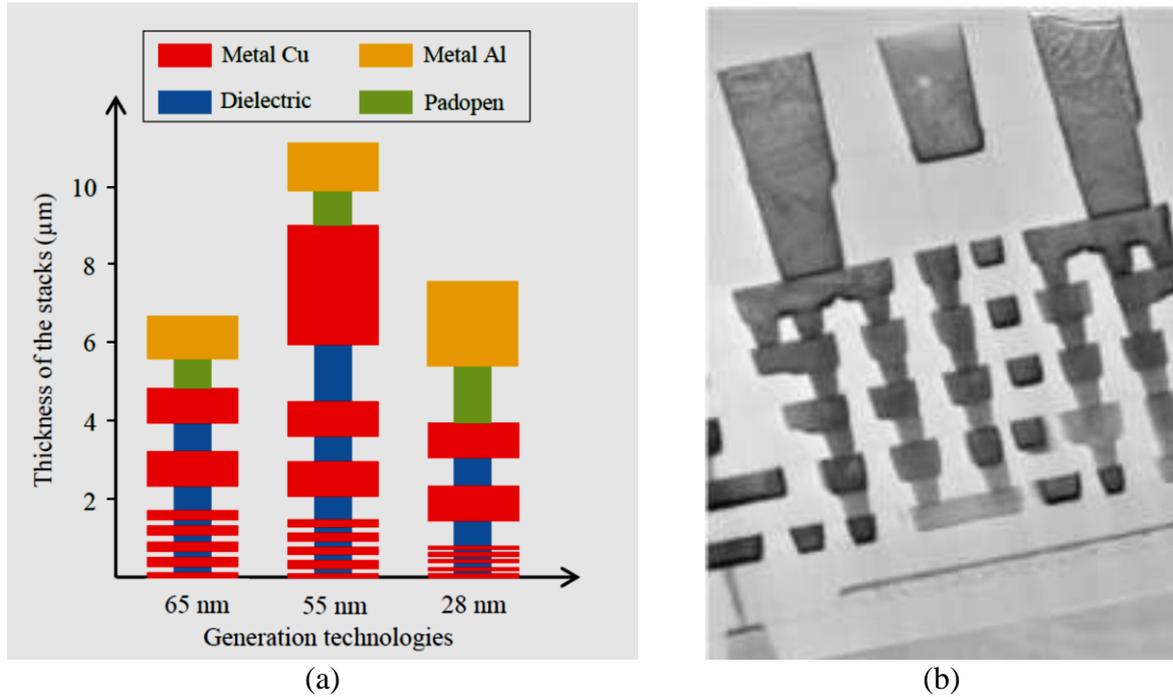


Figure 1.3: (a) Comparison of different STM BEOL stacks. (b) SEM picture of the 65 nm CMOS technology BEOL from STM [8]

Technological limitations are important and must be taken into account. Remarkably, BEOL metal layers density rules must be respected in order to guarantee flatness over the wafer when the mechanical operations are done as CMP (Chemical Mechanical Planarization). Besides, the evolution of the technologies leads to a reduction of the maximal allowed widths for metallic layers.

Based on this BEOL of 55 nm technology, the physical parameters and performances of simulated TLs in both topologies, microstrip and S-CPW (slow-wave coplanar waveguide), at 60 GHz in the 55 nm technology are summarized in Table 1.2 [9]. The maximal total length of the S-CPW was fixed to 124 μm, with 12 μm of ground strip width.

Topology	$Z_c$ (Ω)	Signal stack	Finger layer	Dimensions			Performance		
				$W$ (μm)	$G$ (μm)	$W_g$ (μm)	$\epsilon_{reff}$	$\alpha$ (dB/mm)	$Q$
S-CPW	23	M8-M3	M1	32	34	12	36.6	1.2	27.5
S-CPW	50	M8-M7	M1	26	37	12	10.4	0.46	38
S-CPW	83	M8	M5	6	47	12	8.5	0.5	31
μstrip	26	M8	-	26	Ground M1 plane		3.8	1.01	10.5
μstrip	49	M8	-	8			3.86	1	11.2
μstrip	72	M8	-	2			3.9	1.1	9.1

Table 1.2: Characteristic and performances of the simulated TLs in the 55 nm technology at 60 GHz [9]

For this analysis three characteristic impedances were targeted [9], i.e. 23 Ω, 50 Ω and 83 Ω (72 Ω for microstrip), for both S-CPW and microstrip. It could be possible to reduce the signal width of the 72 Ω microstrip TL in order to get higher characteristic impedance but the insertion loss would increase as well. Indeed  $W$  is really thin, equal to 2 μm. Lower values of  $W$  would lead to very high series resistance and high insertion loss in microstrip line. The effective relative permittivity of 23 Ω S-CPW is very high, i.e. 36.6, thanks to the stack M8-M3 of the CPW, as it leads to a strong capacitance per unit length. The drawback is the high

level of insertion loss, 1.2 dB/mm, but in spite of that, the quality factor is still 2.6 times higher as compared to the microstrip TL with the same characteristic impedance. The highest  $Q$  factor is still obtained for the 50  $\Omega$  TL.

Same BEOL will be utilized in this thesis in order to design low-loss passive/distributed structure. In [9] S-CPW has been utilized, whereas in this thesis a differential TL with slow-wave effect, i.e. S-CPS (slow-wave coplanar stripline) will be utilized. For designing VCO in this thesis S-CPS is chosen; firstly because S-CPS occupies less area, i.e. almost half of S-CPW for same inductance value, and secondly VCO design topology is differential, so the needed distributed inductor is differential as well.

### 1.3 Mm-wave VCO: An overview

A VCO is classically implemented by use of a LC tank but the LC tank/resonator does not oscillate indefinitely by itself because the energy stored within inductor and varactor gets dissipated in their equivalent resistive losses in every cycle. This resonator circuit must entail a self-sustaining mechanism that allows its own noise to grow and become a periodic signal and then maintain oscillations by compensating the losses in the tank. There exist two different ways of representing an oscillator circuit. The first representation is a feedback circuit, as shown in Figure 1.4.

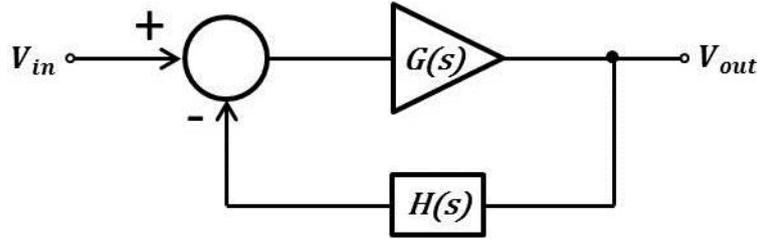


Figure 1.4: Negative feedback network

The overall transfer function of the feedback network is given by eq. (1.2). If the negative feedback amplifier itself experiences so much phase shift that the overall feedback becomes positive, then oscillation may occur.

In other words, if  $s = j\omega_o$ ,  $G(j\omega_o).H(j\omega_o) = -1$ , then the closed-loop gain approaches infinity at  $\omega_o$ . Under this condition,  $V_{out}(\omega_o)$  exist while  $V_{in} = 0$  which means that the system is unstable and oscillates.

$$\frac{V_{out}}{V_{in}}(s) = \frac{G(s)}{1 + G(s).H(s)} \quad (1.2)$$

Thus, for steady oscillations, two conditions must be met simultaneously at  $\omega_o$ :

- (a) the loop gain, i.e.  $|G(j\omega_o).H(j\omega_o)| = 1$
- (b) with total phase shift of  $180^\circ$ , i.e.  $\angle G(j\omega_o).H(j\omega_o) = (\frac{n}{2} + 1)\pi$ , where  $n$  is integer value.

Called Barkhausen criteria, these conditions imply that any feedback system can oscillate if its loop gain and phase shift are chosen properly. This criterion is necessary but not sufficient.

The above view of oscillator is called the “two-port” model in microwave theory because the feedback loop is closed around a two port network  $H(s)$ .

On the contrary to feedback system, the second representation of an oscillator is “one-port model”, as shown in Figure 1.5. It treats the oscillator as two one-port networks connected to each other. The idea in one-port model is that an active network generates impedance  $R_{negative}$  equal to negative of  $R_p$ , so that the equivalent parallel resistance seen by the resonator is infinite. Hence, the energy lost in  $R_p$  is replenished by the active circuit in every cycle, allowing steady oscillations.

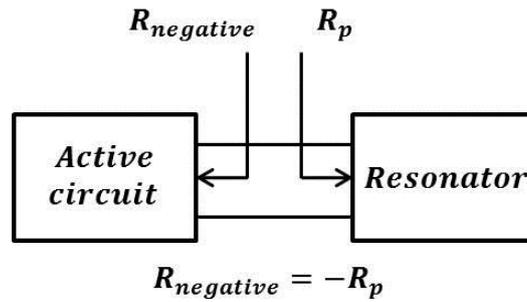


Figure 1.5: One-port model

As mentioned above, a LC resonator does not oscillate indefinitely. The oscillations are sustained by providing sufficient negative resistance ( $R_{negative}$ ) to cancel the losses of the resonator. An active network is needed to generate this negative resistance, so that the equivalent parallel resistance ( $R_p$ ) seen by lossless resonator is infinite

The 2-ports representation of a LC oscillator is shown in Figure 1.6(a) with a typical schematic realization of such VCO shown in Figure 1.6 (b), where nMOS transistor M1-M2 provides negative resistance to compensate the losses of the tank. As shown in Figure 1.6 (a), the open loop gain of active circuit is given by eq. (1.3),

$$G(j\omega_o).H(j\omega_o) = G_m.Z(j\omega_o) \quad (1.3)$$

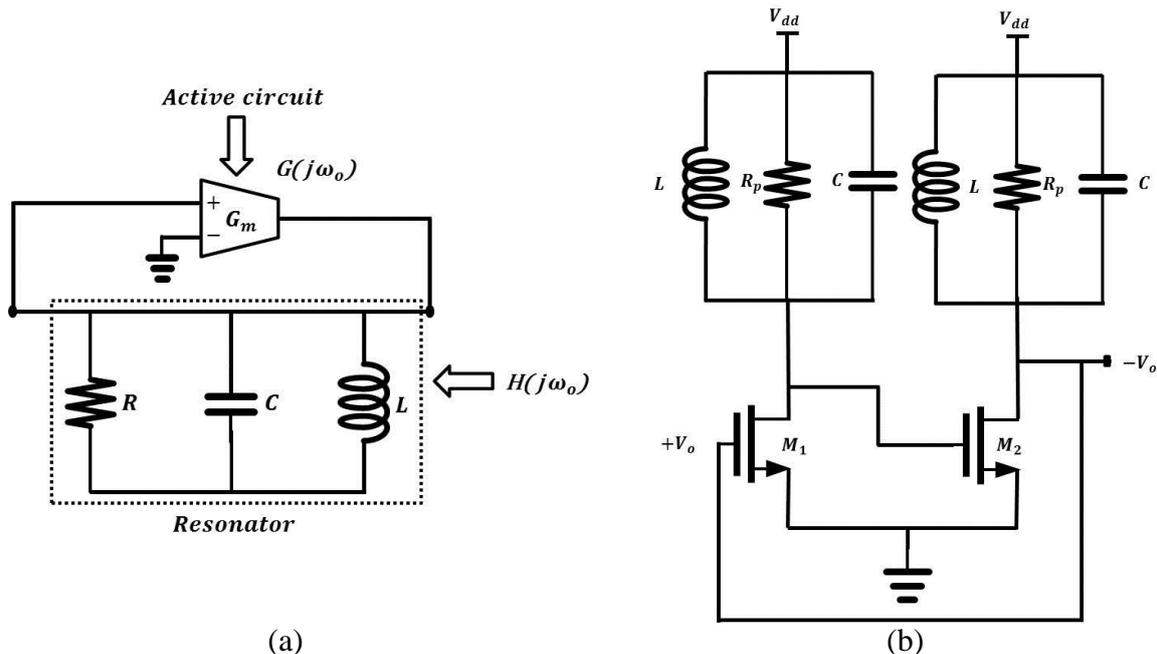


Figure 1.6: LC oscillator (a) General structure and (b) Schematic

So according to Barkhausen criteria  $|G_m \cdot Z(j\omega_0)| = G_m \cdot R > 1$  and phase shift around the loop is zero or integer multiple of  $2\pi$ , i.e.  $\angle G_m \cdot Z(j\omega_0) = 0^\circ \pm 2\pi n$ . As with single stage common source amplifier gives a phase shift of  $180^\circ$ , so it is not possible to attain oscillation. Hence, two stage of common source amplifier are connected in series in feedback loop, as shown in Figure 1.6 (b). So the condition of oscillation is as given by eq. (1.4).

$$|G_m \cdot Z(j\omega_0)|^2 = (G_m R_p)^2 \geq 1 \quad (1.4)$$

$$G_m R_p > 1$$

However, VCO implementation is still challenging, even if the advanced BiCMOS technologies have pushed the transistors cut-off and maximum frequencies  $f_t/f_{max}$  beyond 300 GHz [10]. This is due to the fact that high losses of the passive components leads to need of high transconductance ( $G_m$ ), which rather increases the parasitic capacitance and power consumption of the VCO. In order to overcome the limitations imposed on high frequency VCOs, various design schemes have been proposed in literature. So, before going towards mm-wave VCO design, it is important to notice the design issues and proposed techniques that will be presented in the state-of-the-art discussed in section 1.3.1.

### 1.3.1 Design issues and proposed topologies in state-of-the-art

A VCO is classically implemented by the use of a  $LC$ -tank. However the  $Q$ -factor of the varactor is dominantly low at mm-wave frequencies, refer eq. (1.5a), which dominates the  $Q$ -factor of the  $LC$ -tank, refer eq. (1.6). Hence, increasing the frequency tuning range (FTR) by increasing the varactor size would inevitably degrade the tank  $Q$ -factor and the VCO performance. This is due to the fact that the added loss compensation circuit adds more parasitic capacitance to the oscillator core, hence reducing the FTR. Also, the low- $Q$  lead to increased phase noise, refer eq. (1.7). So, the most challenging issue in mm-wave VCO design is to improve the  $Q$ -factor of the tank. In order to address this issue, several topologies were proposed in [11]-[32].

$$Q_{var} = \frac{1}{\omega R_s C} = \omega C R_p \quad (1.5a)$$

$$Q_{Ind} = \frac{\omega L_s}{R_s} = \frac{R_p}{\omega L_p} \quad (1.5b)$$

$$\frac{1}{Q_{Tank}} = \frac{1}{Q_{Ind}} + \frac{1}{Q_{Var\_min}} \quad (1.6)$$

$$L\{\Delta f\} = 10 \log \left\{ \frac{2FkT}{P_{sig}} \left[ 1 + \left( \frac{f_o}{2Q\Delta f} \right)^2 \right] \right\} \quad (1.7)$$

These proposed topologies can be classified into four main categories:

- (i) Conventional  $LC$ -tank oscillator: designer using lumped inductor and varactor [11] – [19],
- (ii) Hybrid oscillator: designed using both transmission line and lumped  $LC$  [20] – [29],
- (iii) Distributed oscillator: designed using transmission line as resonator [30] – [32]. A brief description of each of these categories will be given in section 1.3.1.1 to 1.3.1.3.



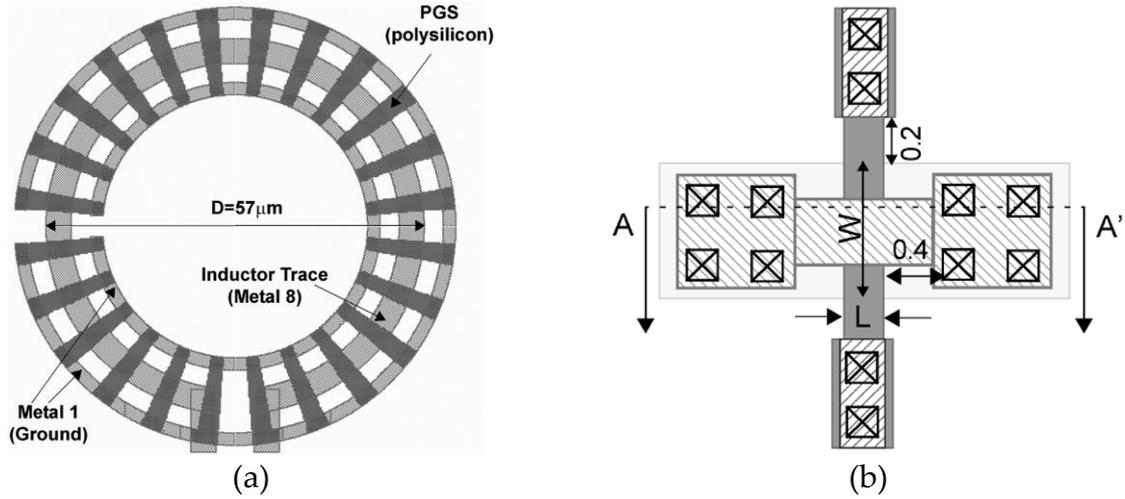


Figure 1.8: (a) Inductor layout (b) Top view of MOS varactor [11]

In [12] and [13] the design issue related to low- $Q$  of high frequency on-chip passive elements has been reported, as it restricts not only the operating frequency of the LC-tank VCO, but also it leads to difficult start-up conditions for sustained oscillation. To alleviate the frequency limitations due to presence of the varactors, admittance transformation technique was proposed in [12] and [13].

A conceptual illustration of this technique is shown in Figure 1.9 [12]. By inserting an inductive elements in series connection with the varactor, the equivalent shunt conductance of the tank was effectively reduced at higher frequencies, hence leading to a VCO design close to the  $F_{max}$  of the MOSFETs.

With a series connection of the varactor  $C_{var}$  and an additional inductor  $L_1$ , the input admittance  $Y_{in}$  can be expressed as,

$$Y_{in} = \frac{1}{j\omega L_1 + (G_{var} + j\omega C_{var})^{-1}} = G_T + (j\omega L_T)^{-1} \quad (1.8)$$

where,

$$G_T = \frac{G_{var}}{L_1^2 C_{var}^2 \omega^4 + (L_1^2 G_{var}^2 - 2L_1 C_{var}) \omega^2 + 1} \quad (1.9)$$

$$L_T = \left( 1 - \frac{L_1 C_{var} \omega^2 - 1}{L_1^2 C_{var}^2 \omega^4 + (L_1^2 G_{var}^2 - L_1 C_{var}) \omega^2} \right) L_1 \quad (1.10)$$

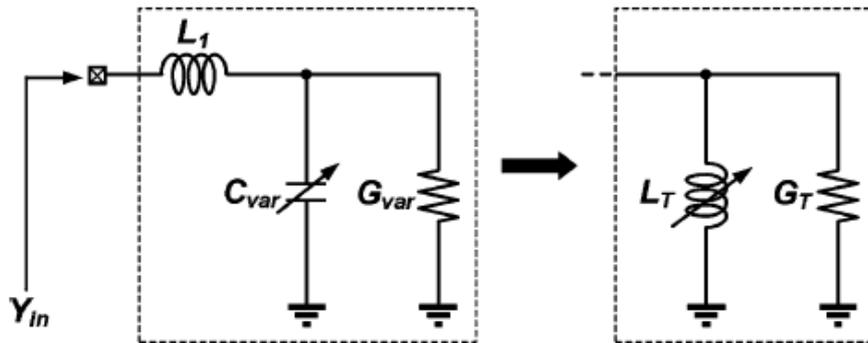


Figure 1.9: Equivalent circuits of the series LC-resonator for the admittance-transforming technique with lossless inductor  $L_1$  [12]

Referring to equation (1.9),  $G_T$  is smaller than  $G_{var}$  if,

$$\omega > \sqrt{\frac{2}{L_1 C_{var}} \frac{Q_{var}^2}{Q_{var}^2 + 1}} \approx \frac{\sqrt{2}}{\sqrt{L_1 C_{var}}} = \sqrt{2} \omega_r \quad (1.11)$$

where,  $Q_{var}$  is the quality factor of varactor, and  $\omega_r$  is the resonant frequency of  $L_1$  and  $C_{var}$ . Hence with proper choice of  $L_1$ , the high frequency losses of the varactor can be reduced and by varying the value of  $C_{var}$  the imaginary part of  $Y_{in}$  can be treated as tunable inductor  $L_T$  at a frequency higher than  $\omega_r$ . Figure 1.10 (a) shows the admittance transformation phenomenon, i.e. reduction in conductance of series ( $L_1 C$ ) resonator with frequency (for different values of  $L_1$ ). Figure 1.10 (b) shows the variation in equivalent inductance ( $L_T$ ) versus frequency (for different values of  $L_1$ ), representing the achievable tuning ratio.

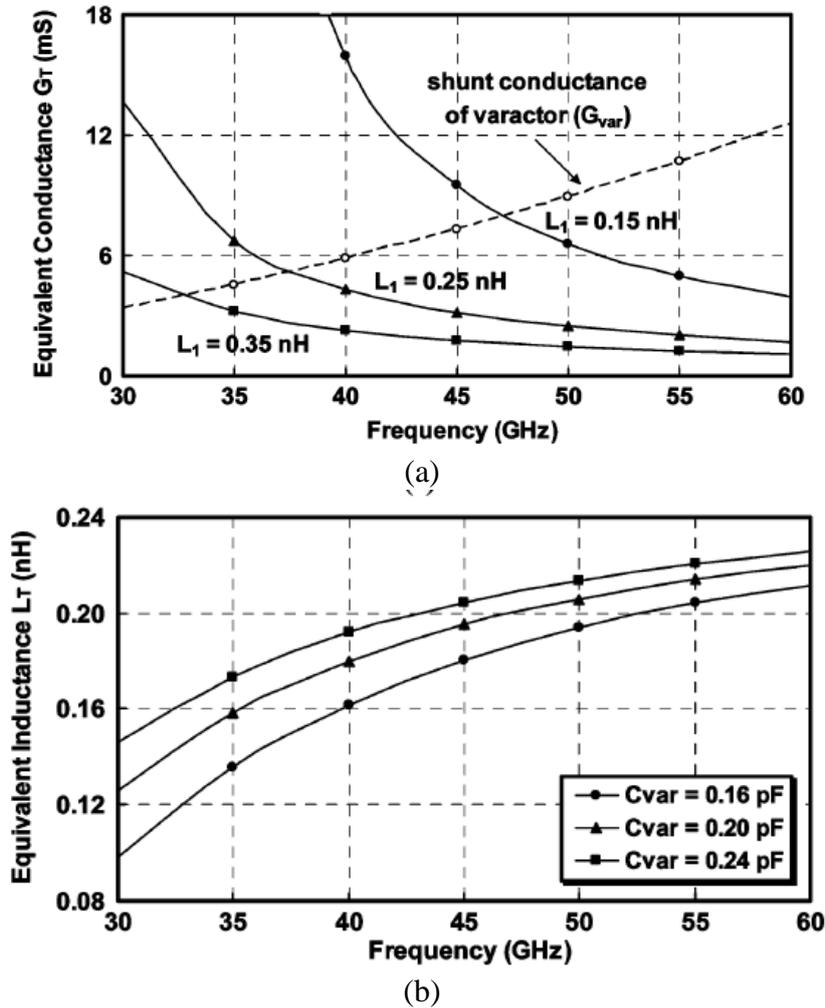


Figure 1.10: (a) Simulated equivalent conductance  $G_T$  for various values of  $L_1$  with  $C_{var} = 0.2$  pF, (b) Simulated equivalent inductance  $L_T$  for various values of  $C_{var}$  with  $L_1 = 0.25$  nH [12]

The VCO topology [12] is shown in Figure 1.11 and has been designed in 0.18  $\mu\text{m}$  CMOS technology. The designed oscillator topology for  $F_{osc}$  of 49 GHz achieved a tuning range of only 0.8 GHz, with phase noise of -101 dBc/Hz at 1MHz offset and the power consumed by VCO core was 45 mW.

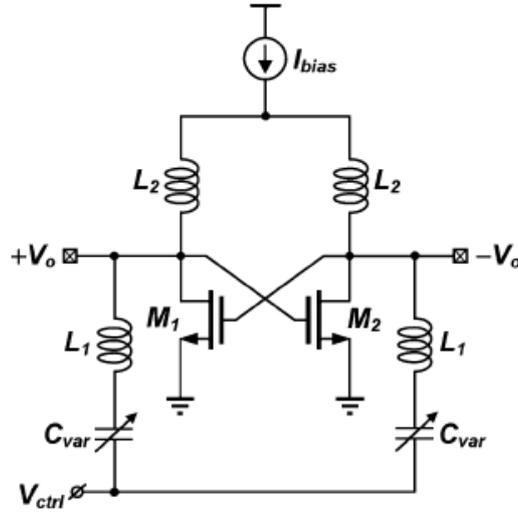


Figure 1.11: VCO topology proposed in [12]

Similar to [12], the admittance transformation technique has been proposed in [13]. However unlike [12] where the admittance transformation was applied on the LC tank, in [13] this technique has been applied to cross-coupled pair. So, in [13] the equivalent negative conductance of the cross-coupled pair has been enhanced through the on-chip transmission lines without increasing the transistor size, shown in Figure 1.12.

Figure 1.13 shows a conceptual illustration of the proposed admittance transformation technique. With a series connection of a cross-coupled pair and addition transmission line segments, the input admittance  $Y'_{in}$  is given by eq. (1.12).

$$Y'_{in} = \frac{1 - |\Gamma| \exp(-2j\beta_o l_o + j\varphi)}{1 + |\Gamma| \exp(-2j\beta_o l_o + j\varphi)} \cdot Y_o \quad (1.12)$$

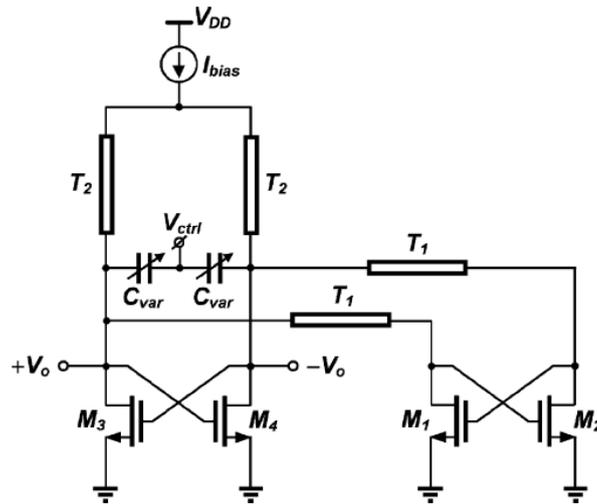


Figure 1.12: VCO topology proposed in [13]

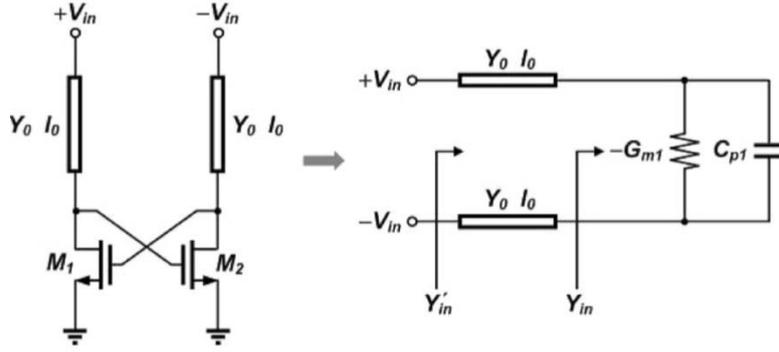


Figure 1.13: Proposed admittance transformation technique [13]

where,

$$|\Gamma| = \sqrt{\frac{(Y_o + G_{m1})^2 + (\omega C_{p1})^2}{(Y_o - G_{m1})^2 + (\omega C_{p1})^2}} \quad (1.13)$$

$$\varphi = -\tan^{-1}\left(\frac{\omega C_{p1}}{Y_o + G_{m1}}\right) - \tan^{-1}\left(\frac{\omega C_{p1}}{Y_o - G_{m1}}\right) \quad (1.14)$$

If the operating frequency  $\omega_o$  is chosen such that,

$$2\beta_o l_o - \varphi = 180^\circ \quad (1.15)$$

the input admittance in eq. (1.12) can be expressed as

$$Y'_{in}(\omega_o) = -\frac{|\Gamma| + 1}{|\Gamma| - 1} \cdot Y_o \quad (1.16)$$

As the length of the transmission line segments are properly chosen such that the condition in eq. (1.15) is satisfied at 60 GHz, the input admittance reaches a maximum value for the negative conductance while the imaginary part becomes zero. As a result, the cross-coupled pairs can be used to compensate for the losses from the  $LC$ -tank without introducing additional capacitive loadings.

The VCO topology presented in [13] has been designed in 0.18  $\mu\text{m}$  CMOS technology. The designed oscillator topology for  $F_{\text{osc}}$  of 63 GHz achieved a tuning range of only 0.67 GHz, with phase noise of -89 dBc/Hz at 1MHz offset and the power consumed by VCO core was 74 mW.

An inductive division technique was proposed in [14] to improve both phase noise and tuning range of VCO, especially under a low supply voltage. In general a VCO has three intrinsic noise contributors: the tank loss, the noise of the cross coupled pair and the noise of the tail current. The phase noise has two generation processes: one is captured by the physical interpretation of Leeson's noise factor, called direct phase noise generation process; the other is due to the tank indirect nonlinear AM-PM conversion processes.

So, in proposed VCO to achieve good phase noise performances two ways were proposed, i.e. by using a high- $Q$  tank, hence increasing the signal amplitude across the tank and the tail current was removed in the proposed oscillator structure shown in Figure 1.14 (a).

To improve the tuning range of VCO, two-turn inductor has been utilized with a varactor having double gate connection to reduce  $R_{poly}$ , shown in Figure 1.14 (b). Due to magnetic coupling between inductor lines, the inductor area is reduced. This inductor is octagon shaped to reduce the series losses without violating the design rules, and it uses top metal to reduce the substrate loss.

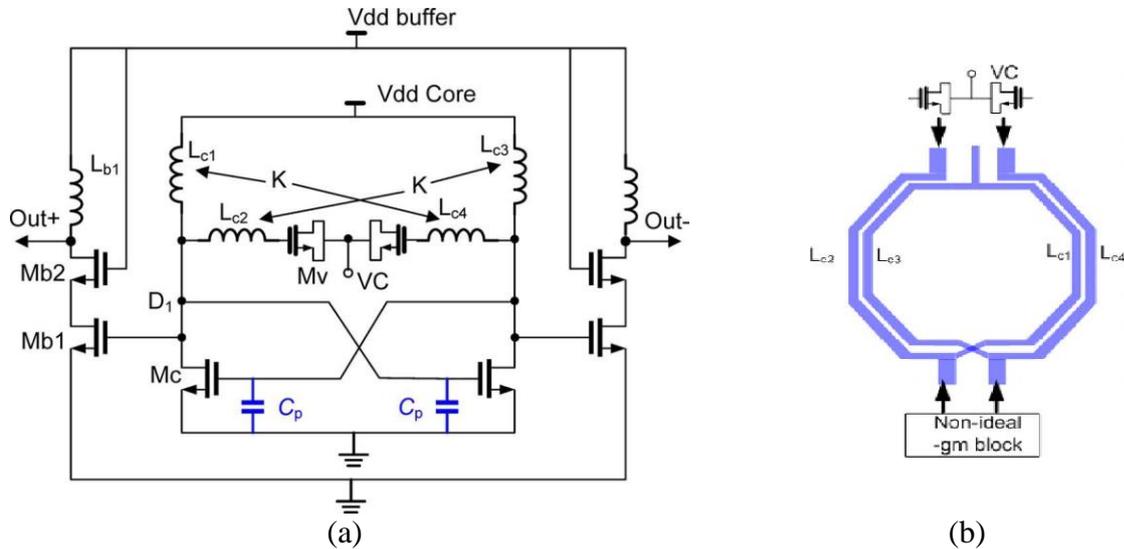


Figure 1.14: (a) Tail current biased cross-coupled pair oscillator, (b) Layout arrangement of oscillator tank [14]

The VCOs presented in [14] were designed in 90 nm CMOS technology. These VCOs designed under supply voltage of 0.7 V and 0.43 V for  $F_{osc}$  of 58.4 GHz and 61.7 GHz achieved tuning range of 5.2 GHz and 2.9 GHz, respectively. The achieved phase noise was -91 dBc/Hz and -90 dBc/Hz at 1 MHz offset, for power consumption of 8.1 mW and 1.2 mW, respectively.

The typical tuning range using varactor tuning scheme at mm-wave frequency is less than 10% [11] – [14]. Hence, a novel technique for coarse tuning was proposed in [15] to increase the tuning range of VCO without using large varactors. In this technique the coupling coefficient of a transformer tank (see Figure 1.15) was changed in order to increase the frequency tuning range. As shown in Figure 1.15, by exploiting the three states with different magnetic coupling coefficients created by the proposed switched-triple transformer, the continuous frequency tuning range was achieved.

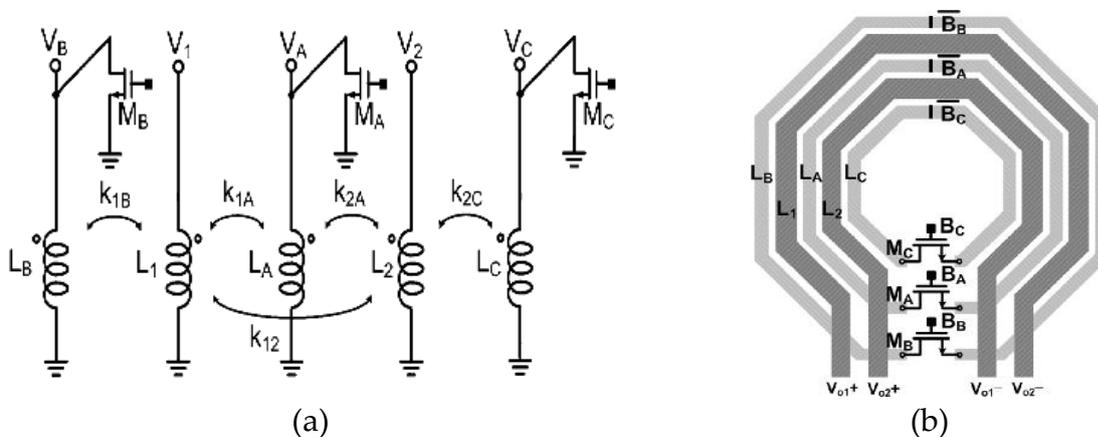


Figure 1.15: (a) Schematic and (b) Layout of proposed switched-triple-shielded transformer [15]

The schematic of proposed MT-VCO is shown in Figure 1.16, has been designed in 65 nm CMOS technology. With proposed magnetically tuned (MT) VCO, a frequency tuning range of 32 GHz was achieved for a center frequency of 73.8 GHz, while consuming 7 to 9 mA at 1.2 V supply with phase noise of -104 to -112 dBc/Hz at 10 MHz offset.

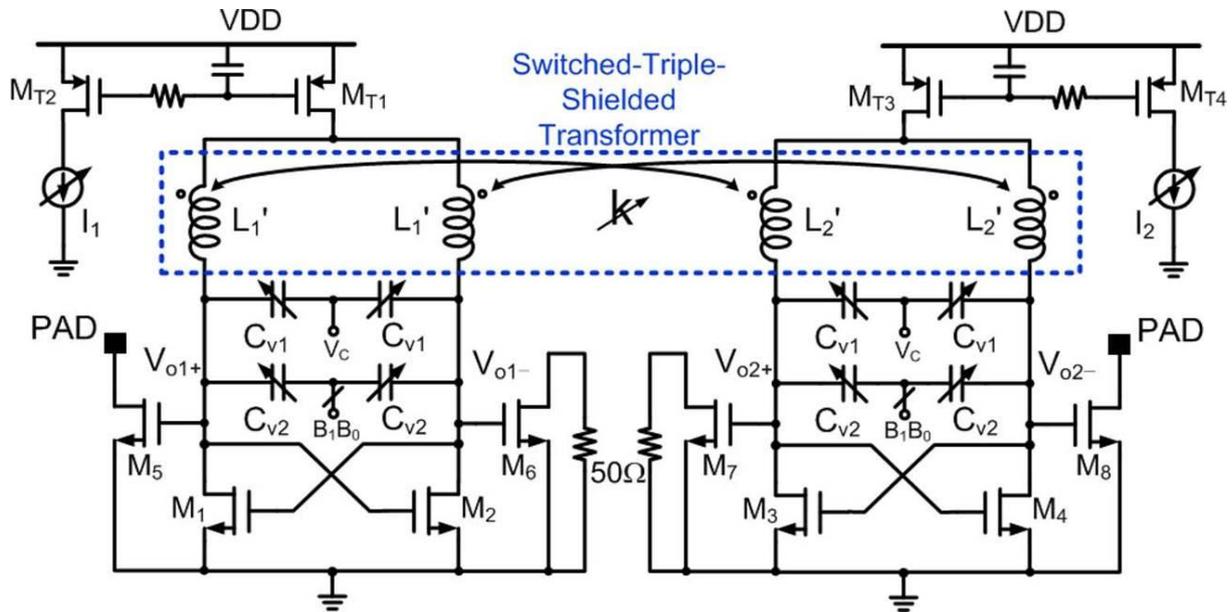


Figure 1.16: Schematic of proposed MT-VCO [15]

Even though the presented architecture in [15] is very performant, but the proposed design is thoroughly complex: firstly because for tuning inductors magnetically, switches have been employed, which changes the coupling factor 'k'. And secondly as the inductive tuning with switched inductors provide only coarse tuning with a large step size (e.g., 1 GHz/bit), so it must be augmented by switched-capacitors to form a VCO or DCO.

Unlike [15], in [16], [17] a constant single-turn inductor has been utilized with a digital controlled varactor bank. For designing the continuous tuning digitally controlled varactor bank a differential N+poly/Nwell varactor operating in accumulation mode has been utilized. An additional bank of digitally controlled differential varactors has been utilized to provide coarse tuning using three bits ( $b_2, b_1$  and  $b_0$ ). It has been implemented with seven equal differential varactors grouped in 4, 2, and 1 units that change the binary-scaled capacitance. The binary switched varactors have been made from same structure as the fine-tuning varactor. Figure 1.17 shows the VCO schematic and the digitally controlled varactor bank of proposed architecture.

The proposed VCO circuit in [16], [17] were implemented in 65 nm CMOS technology. For a center frequency of 56 GHz a frequency tuning range of 9.3 GHz was achieved, with a power consumption of 15 mW and a phase noise of -99.4 dBc/Hz at 1 MHz offset.

As per [16] the best compromise for FTR, PN and power consumption can be obtained using LC-Tank VCOs by optimally sizing the VCO transistors in order to minimize the parasitic capacitances and by maximizing the varactor capacitance range. However for broadband mm-wave applications a multi-band VCO is needed, but a conventional capacitive bank for multi-band operation cannot be used because the loading capacitance will be very large to be tolerable.

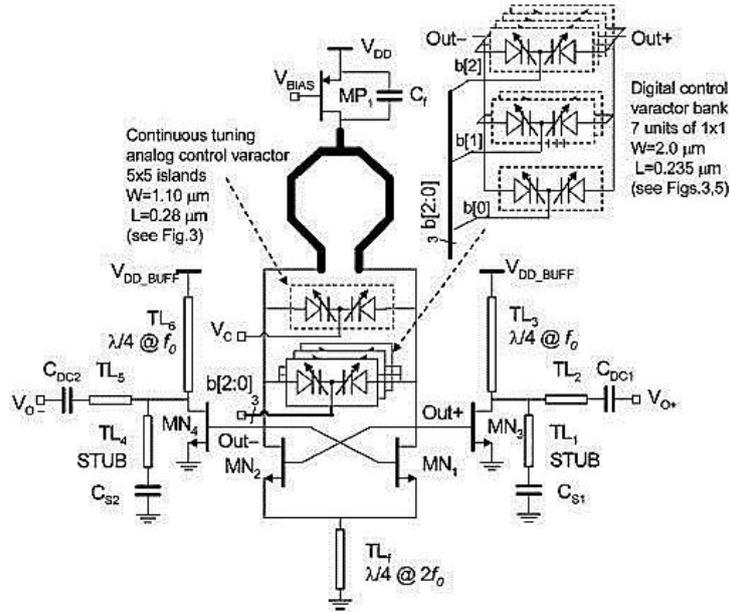


Figure 1.17: VCO schematic [16], [17]

Hence, varactor less VCO was proposed in [18], [19] for multi-band operation using a novel variable inductor (VID), shown in Figure 1.18. This VID employs the magnetic tuning scheme and achieved multiband as well as broadband operation without sacrificing the oscillation frequency. The VID implementation shown in Figure 1.18 (a) has been modified to multiband VID, shown in Figure 1.18 (b), by decomposing  $M_v$  into several smaller devices  $M_{v1} \dots M_{vn}$  in parallel. Each smaller device is separately controlled by voltages  $V_{b1} \dots V_{bn}$ .

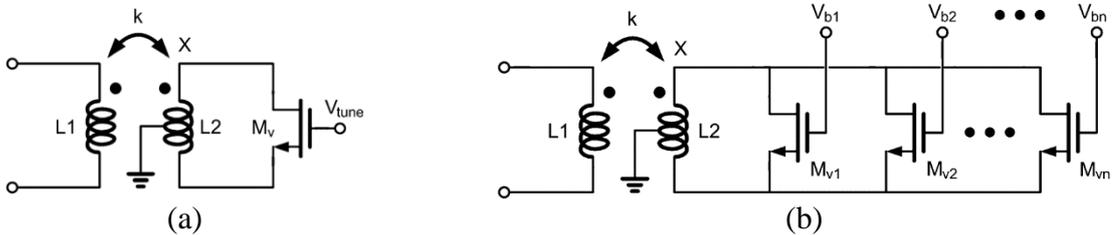


Figure 1.18: (a) VID implementation, (b) Multiband Variable inductor implementation [18], [19]

As the device size of  $M_v$  is equal to those of  $M_{v1} \dots M_{vn}$  in total, the parasitic capacitance at node X in Figure 1.18 (b) is almost the same as that in Figure 1.18 (a). Thus, multi-band operation can be achieved without severely affecting the inductance and the tuning percentage of the VID. This is a major advantage in contrast to conventional capacitor-bank structure, where the parasitic capacitor in general contributes significantly to the total capacitance at the oscillating node, and thus limits the tuning range. The VCO schematic of varactor less VCO is shown in Figure 1.19.

The proposed varactor less VCO was implemented in 90 nm CMOS technology. For a center frequency of 56.7 GHz the achieved frequency tuning range was 8.8 GHz, with power consumption of 8.7 mW and phase noise of -118 dBc/Hz at 10 MHz offset.





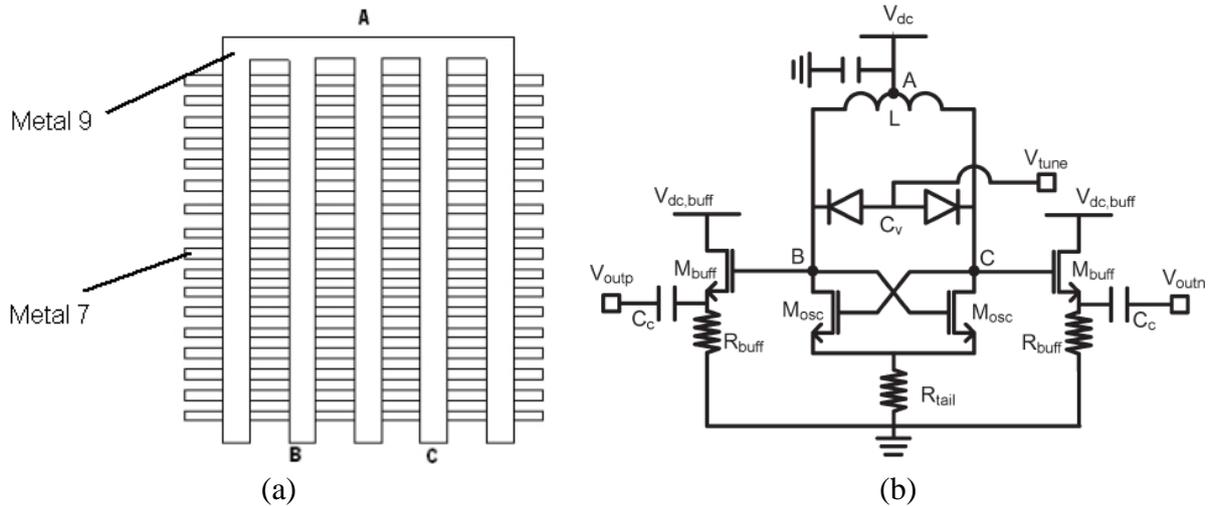


Figure 1.22: (a) Top view of shorted differential Slow-wave CPW (b) Simplified schematic of VCO [22], [23]

A digitally switchable Metal-Oxide-Metal capacitor design, shown in Figure 1.23, was proposed in [24] to achieve wide frequency tuning range. This VCO has been designed in 0.13- $\mu\text{m}$  CMOS technology. However the tuning range of only 2 GHz was obtained for  $F_{osc}$  of 45 GHz with phase noise of -97 dBc/Hz at 3MHz offset and power consumption of 4 mW.

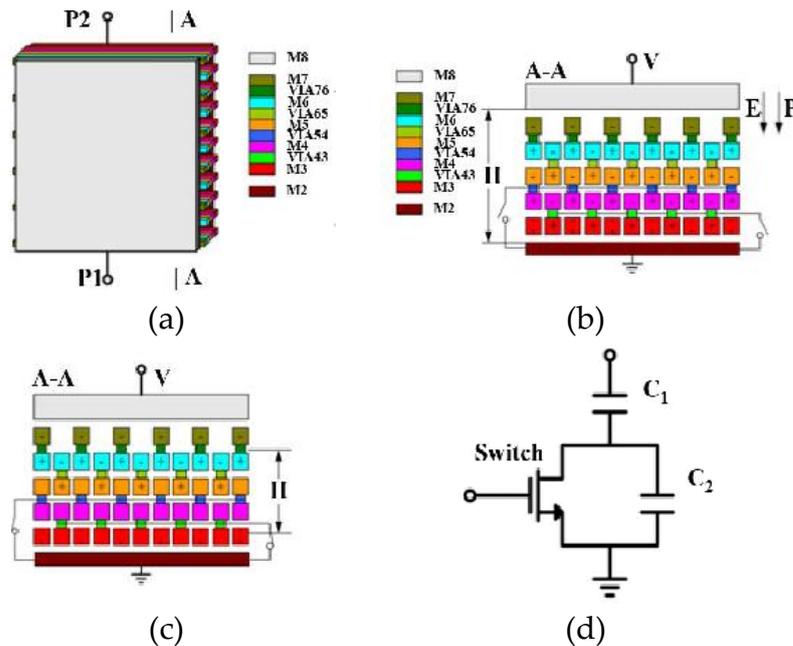


Figure 1.23: (a) Physical structure of the MOM capacitor (b) Cross section view with switches open (c) Cross section view with switches closed (d) Equivalent model of the MOM capacitor [24]

For the purpose of improving  $Q$ -factor of resonator, a switchable artificial grounded metal guard ring (SWAG-MGR) technique was proposed in [25]. With SWAG-MGR technique, planar inductors has been converted into switchable inductors and by turning the switch (SW) ‘on and off’, shown in Figure 1.24, the tuning range of mm-wave VCO has been extended.

In designed VCO, small MOS varactors were used for fine tuning within the band and the SWAG-MGR based switchable inductors were used for coarse tuning of 2.7 GHz. The designed VCO with switchable inductor attained tuning range of 9.43 GHz for  $F_{osc}$  of

55.7 GHz and the measured phase noise was -119 dBc/Hz at 10 MHz offset with power consumption of 10.2 mW.

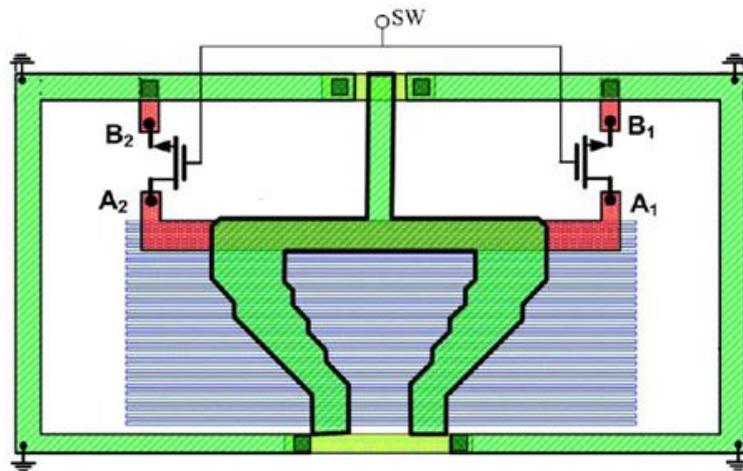


Figure 1.24: Proposed switched inductor [25]

Use of floating metal strip slow-wave structure underneath the transmission line leads to reduced length of on chip interconnects and oscillator. This approach was extended in [26] to the use of embedded 2-dimensional artificial dielectrics in order to shrink the resonator size, reduce substrate losses and enhance resonator  $Q$ -factor. Figure 1.25 (a) shows the quarter wavelength ( $\lambda/4$ ) resonator with underlying artificial dielectric. Although the VCO designed using the resonator with embedded artificial dielectric (Figure 1.25 (b)) showed very limited tuning range of 100 MHz for a  $F_{osc}$  of 60 GHz because of very small varactor variations, however the measured phase noise was -100 dBc/Hz at 1 MHz offset with power consumption of 1.9 mW. This VCO has been designed in 90 nm CMOS technology.

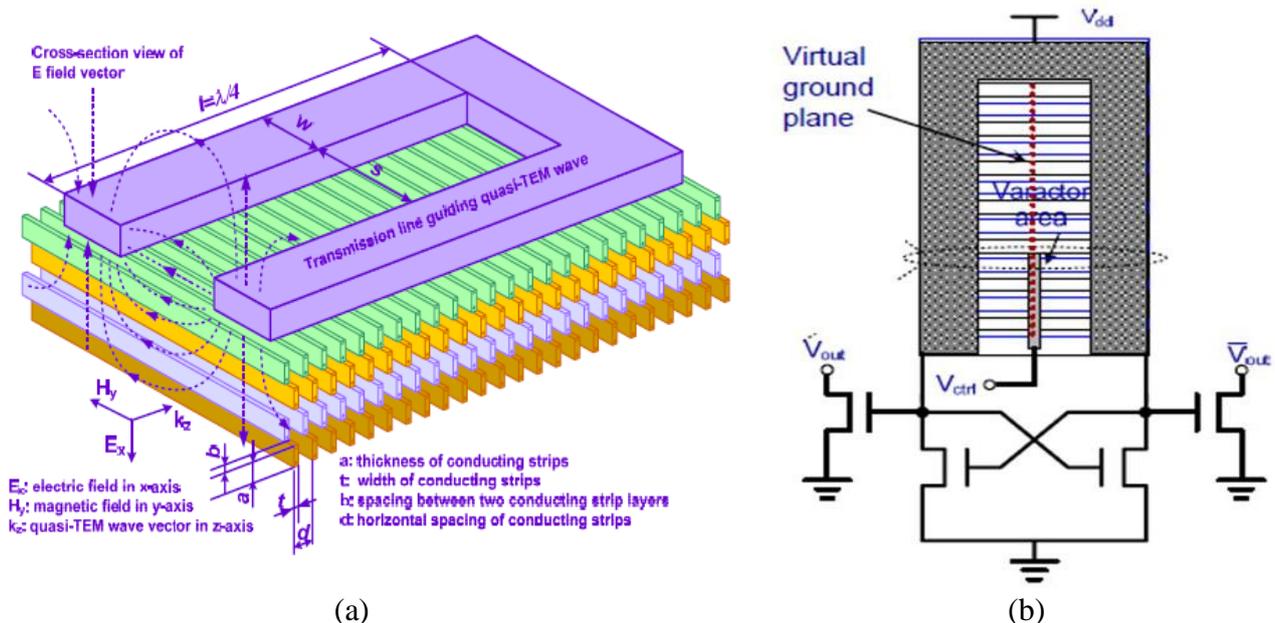


Figure 1.25: (a)  $\lambda/4$  standing wave resonator with underlying artificial dielectric, (b) VCO schematic [26]

As mentioned in introduction of this section 1.3.1.2, in [27] – [29] instead of varactors, switches have been utilized with distributed elements for tuning the frequency of oscillation and lumped inductors have utilized instead of lumped varactor/ capacitors.

In [27] an open circuited DiCAD stub has been presented as a tuning element. This open circuited DiCAD stub was utilized for designing a mm-wave digital controlled oscillator (DCO). This DiCAD differential transmission line (DTL) is a slow-wave structure, in which the effective permittivity was digitally controlled by nMOS  $\pi$ -switches when tuned on or off, shown in Figure 1.26, hence engaging or disengaging the floating strips and changing its average effective dielectric constant.

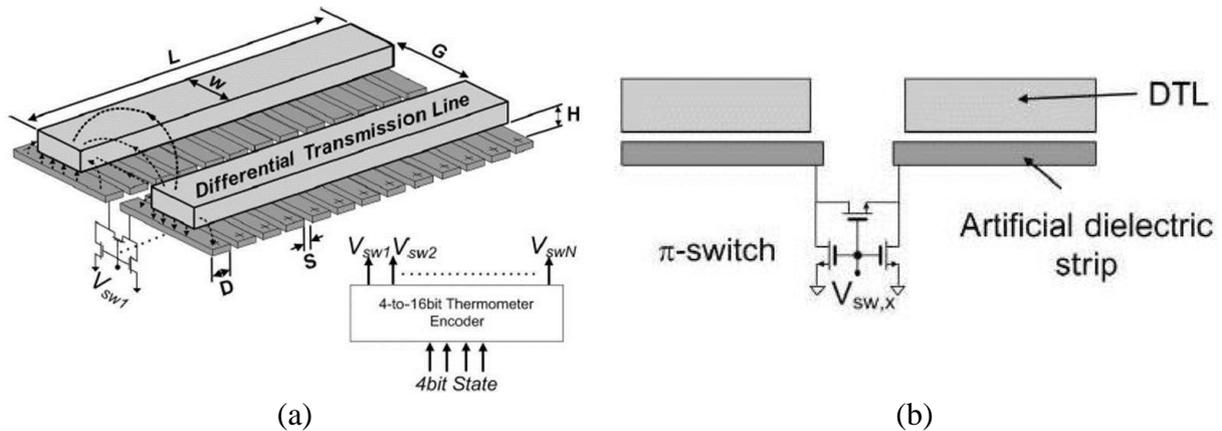


Figure 1.26: (a) DiCAD differential transmission line layout, (b) cross-sectional view of DiCAD DTL strip [27]

Figure 1.27 shows the DCO schematic and has been designed in 90 nm CMOS technology. The standard nMOS cross coupled pair has been loaded by single turn inductor and an open-circuited DiCAD stub. This DCO [27] achieved frequency tuning of 6 GHz for  $F_{osc}$  of 61 GHz. The phase noise was better than -90 dBc/Hz at 1 MHz offset with power consumption of 8.52 mW.

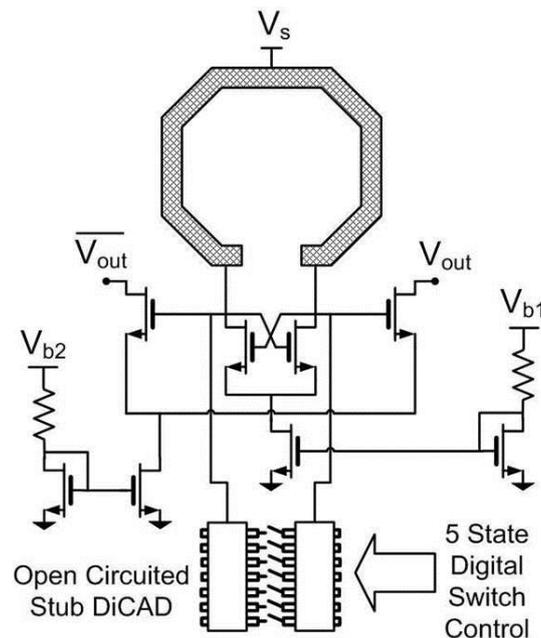


Figure 1.27: Proposed DCO schematic [27]

Based on the same technique of DiCAD resonator [27], two DCOs were proposed in [28] and [29], i.e. L-DCO and T-DCO. The frequency resolution was just 1.16 GHz for [27], whereas the proposed DCO in [28], [29] offer frequency resolution better than 1 MHz. The schematic of proposed L-DCO and T-DCO is shown in Figure 1.28.

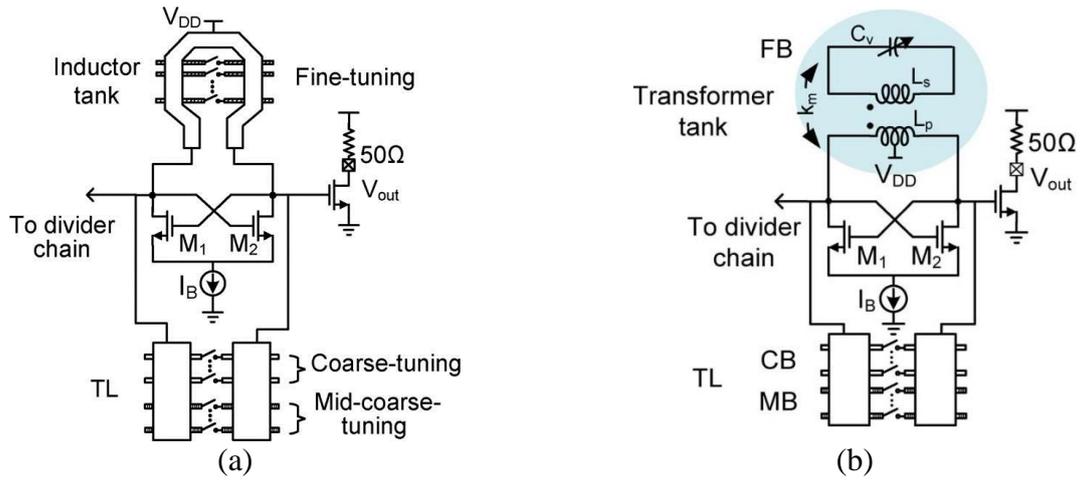


Figure 1.28: Schematic of 60 GHz (a) L-DCO, (b) T-DCO [28], [29]

The L-DCO was designed around an inductor based fine-tuning bank (Figure 1.29(a)), whereas the T-DCO employed a weakly coupled transformer (Figure 1.29(b)) to implement a unit-weighted fine-tuning bank. Both DCOs comprised of three-stage segmented tuning: a CB, an FB, and a MB that bridges the gap in step-size between CB and FB. The CB and FB for both DCOs was employed with a reconfigurable TL (transmission line), shown in Figure 1.29 (c).

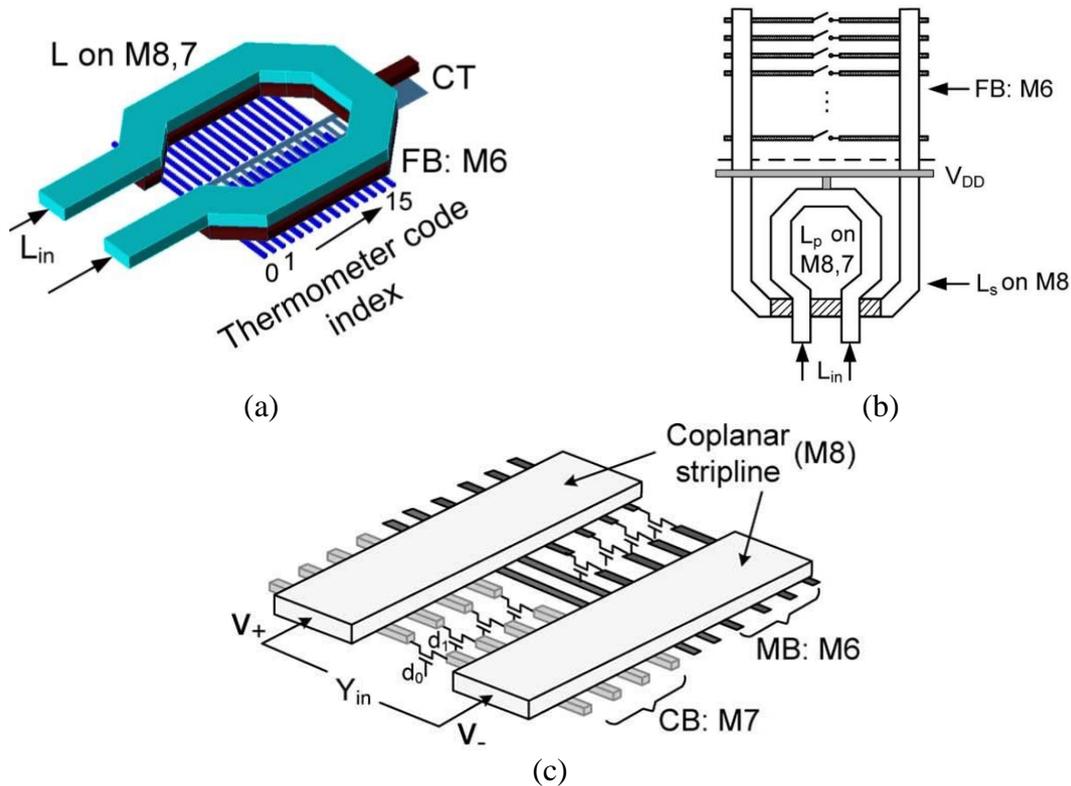


Figure 1.29: 3-D view of reconfigurable TL for (a) Fine tuning L-DCO, (b) Fine tuning T-DCO, (c) coarse- and mid-coarse tuning L- and T-[28], [29]

The inductor-based DCO, i.e. L-DCO achieved fine-tuning resolution better than 160 kHz. While, the transformer based DCO, i.e. T-DCO achieved fine-tuning step of 2.5 MHz. Both the proposed designs were designed in 90-nm CMOS technology. For both DCOs the obtained linear tuning range was 6 GHz for  $F_{osc}$  59 GHz and the obtained phase noise was

-93 dBc/Hz at 1 MHz offset. The L-DCO and T-DCO consumed 12 mW and 14.4 mW, respectively.

On comparing the topologies proposed in this section, it can be remarked that use of varactor in [20] – [24], [26] lead to reduction in tuning range, as the  $Q$ -factor of the tank is limited. Whereas in [25] tunable inductor (using nMOS switches) was utilized for switching the band and small varactors were utilized for fine tuning within the band, providing better performance as compared [20] – [24], [26]. In [27] – [29] no varactors were utilized. In fact the frequency tuning was performed by employing reconfigurable TLs. The TLs were made reconfigurable by employing switches. Although the proposed designs in this section achieved good performance in terms of phase noise and tuning range, but with these topologies [27] – [29] it is difficult to realize wide-band VCOs/SWOs. It is important to note that in all the proposed designs [20] – [29], as the losses are compensated on localized position (i.e. only at one position of resonator), it leads to addition of high parasitic capacitance as well. To solve these issues concerning wide-band oscillators, the concept of distributed SWO seems to be a good approach. This approach of distributed SWO is discussed in next section 1.3.1.3.

#### 1.3.1.3 Distributed standing wave oscillator

As seen in section 1.3.1.1, a prevalent class of oscillators relies on lumped  $LC$ -resonator. However due to the limitations on device parasitics most of the high frequency  $LC$ -tank VCOs suffer from an inadequate frequency tuning range. Wave-based oscillator is another category of oscillators that has emerged. The wave-based oscillators operating on wave behavior of transmission line forms a prominent category as well because it allows placing high- $Q$  resonator and hence improving VCO/ SWO performance (discussed in section 1.3.1.2). Nevertheless among the presented SWOs in section 1.3.1.2, the most improved performance were from the DCOs [27] – [29] employing reconfigurable TLs for improving the FTR.

In state-of-the-art there exists one more category of wave-based oscillators, i.e. called as distributed SWO. This category of wave-based oscillators fulfill certain design criteria, i.e. firstly the proper distribution of active gain elements along a wave propagation medium facilitates oscillation frequencies towards  $F_t$ . Secondly, this distributed architecture reduces the loading effect hence wave-based oscillators demonstrate great potential for wide-band applications at mm-wave frequencies. However this structure consumes high dc power because it includes several transconductance ( $g_m$ ) cells for compensating the losses of resonator periodically.

Position-dependent voltage-current amplitudes is very basic property of standing-wave resonators/ oscillators, shown in Figure 1.30. In [30] it is demonstrated that one can physically taper a transmission line such that it is adapted to the standing wave amplitude variations to reduce loss in the line, hence leading to improved- $Q$  and significant phase noise reduction in standing wave oscillators (SWO).

Since the CPS of Figure 1.30 has large voltage amplitude and negligible current amplitude near  $z = 0$ , the majority of loss is through shunt conductance  $G$  towards  $z = 0$ . Therefore,  $G$  must be minimized to reduce loss near  $z = 0$ , while the unavoidable increase in  $R$  due to the  $R$ - $G$  tradeoff is not detrimental because of the negligible current amplitude in this vicinity.

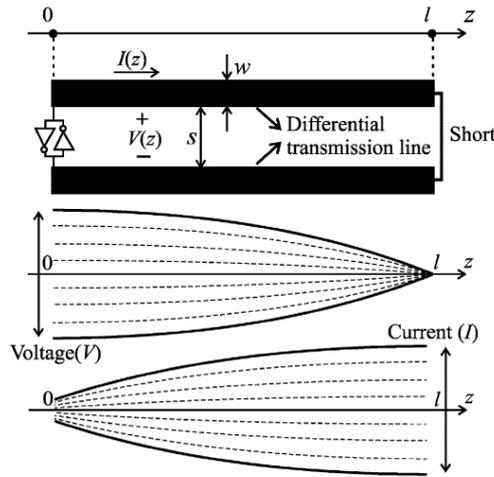


Figure 1.30:  $\lambda/4$  standing wave oscillator (SWO) and voltage-current standing wave amplitudes [30]

Similarly, since the  $\lambda/4$  CPS of Figure 1.30 has large current amplitude and insignificant voltage amplitude near  $z = l$ , most loss occurs in the series resistance  $R$  towards  $z = l$ . Therefore,  $R$  must be minimized to reduce loss near  $z = l$  while the inevitable increase in  $G$  due to the  $R$ - $G$  tradeoff is not harmful because of the locally negligible voltage. This variation of the loss parameters,  $R$  and  $G$ , with position,  $z$ , to reduce loss by circumventing the  $R$ - $G$  tradeoff yields a tapered transmission line.

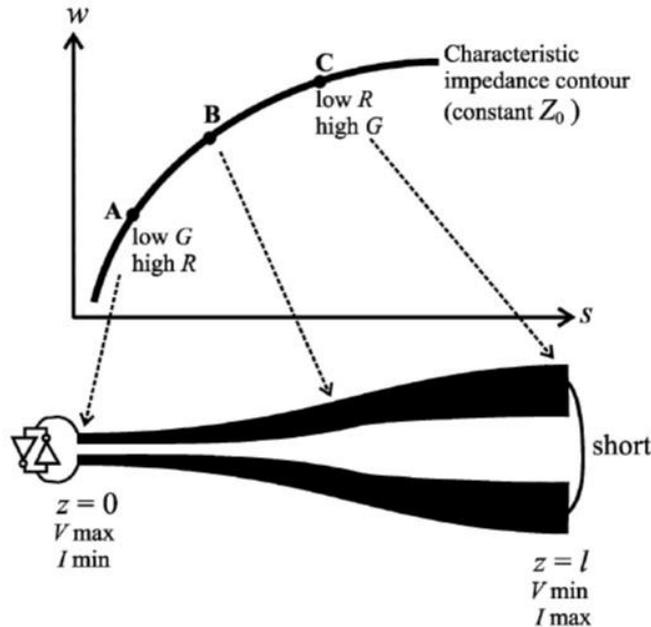


Figure 1.31: Simulation-based characteristic impedance contour and  $R$ - $G$  variations in  $w - s$  space. As one simultaneously increases metal width  $w$  and metal spacing  $s$  of a CPS along the characteristic impedance contour,  $Z_o$  remains constant while  $R$  decreases and  $G$  increases [30]

Figure 1.31 shows a simulation-based contour of characteristic impedance in  $w - s$  space in a standard CMOS technology. As one simultaneously moves apart (increasing) and widens (increasing) the CPS following this contour,  $Z_o$  remains constant while  $R$  decreases and  $G$  increases. In [30] two oscillator designs were proposed without any varactor, i.e. only to demonstrate the reduced losses in tapered transmission line over an un-tapered transmission line.

The same principle of operation has been utilized in [31], but instead of tapering the transmission line resonator the gain elements were tapered for compensating the losses. Also, to extend the tuning range of the proposed distributed SWO, MOS switches were employed as well, shown in Figure 1.32. By turning these switches ‘on and off’ the length of the resonator was changed and hence the frequency range/band was varied. The MOS switches in Figure 1.32 lead to band switching mechanism and the varactors were utilized to obtain a fine-tuning of the oscillator frequency within the frequency band. This technique [28] achieved a tuning range of 7.5 GHz for  $F_{osc}$  of 38 GHz, with a phase noise of -100.2 dBc/Hz at 1 MHz offset and for power consumption of 27 mW. This SWO has been designed in 0.18  $\mu\text{m}$  CMOS technology.

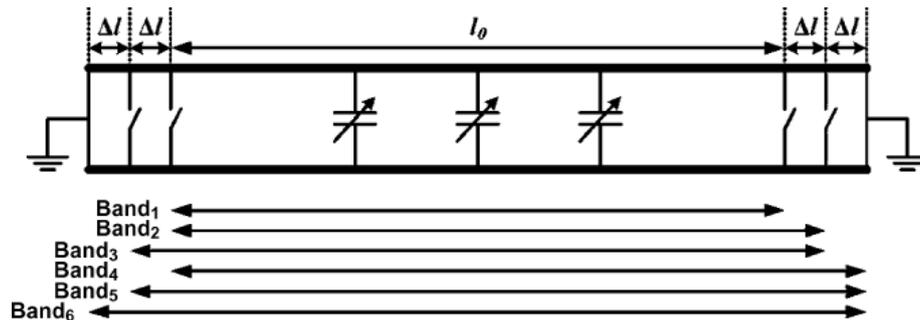


Figure 1.32: band switching mechanism [31]

Based on similar approach as [31] distributed SWO, a push-push SWO design for G-band application has been presented in [32]. The only difference between [31] and [32] is the way of embedding the varactors for frequency tuning, i.e. in [31] varactors were placed parallel with cross-coupled pairs while in [32] varactors were connected in the center of the resonator. And no band switching mechanism has been employed in [32]. With power consumption of 33 mW, [32] achieved tuning range of 23 GHz for  $F_{osc}$  of 162 GHz. The estimated phase noise based on measurement performed at fundamental frequency was -91.3 dBc/Hz at 1 MHz offset for power consumption of 33 mW. This SWO has been designed in 65 nm CMOS technology.

A detailed comparison of all the presented topologies in section 1.3.1 is tabulated in section 1.3.2.

### 1.3.2 Comparison of proposed techniques in state-of-the-art

On comparing the performance of various schemes, refer Table 1.3, it can be remarked that the VCO performance is very much dependent on utilized technology and it is difficult to establish a fair comparison without knowing the exact BEOL. However it is evident that the major design constraints are, firstly to achieve high  $Q$ -factor of the tank/resonator with a wide tuning range and secondly to improve the phase noise performance. For portable devices the power consumption is also one of the special concerns.

The conventional approach (i.e. with lumped inductor and varactor) proposed in [11] – [13] presents low  $Q$ -factor of the LC tank, which degrades VCO performance. This is due to the fact that low  $Q$ -factor of the varactors is difficult to improve in this frequency range. While, from [14] – [19] several optimization techniques have been applied with lumped-LC tank to improve the VCO performance. Among these the magnetically tuned multi-mode VCO design [15] showed exceptionally good performance in terms of frequency tuning range i.e. 40 % (approx.). The varactor less VCO designed by using variable inductors VID in [18],

[19] showed good performance, but its implementation is as difficult as the one presented in [15]. In [20] – [29] various topologies with combination of distributed and lumped elements and tunable/switched inductors were proposed. Among these proposed topologies, use of digitally switchable metal-oxide-metal (MOM) capacitors in [24] and use of on-chip resonator with embedded artificial dielectric in [26] resulted in very low tuning range. Instead, use of distributed tunable inductor in [20], [21], just slow-wave structure in [22], [23], switchable artificial grounded metal guard ring in [25], and DiCAD resonator in [27] – [29] resulted in promising mm-wave VCOs. Lastly, the distributed SWO topologies [30] – [32], showed very good performance with the highest targeted frequency (among the studied articles) in [32] and wide-band tuning [31], [32].

<i>Ref</i>	<i>Technology</i>	$F_{osc}$ (GHz)	$FTR$ (%)	$TR$ (GHz)	$PN$ (dBc/Hz)	$P_{out}$ (dBm)	$P_{DC}$ (mW)	$FOM$ (dBc/Hz)	$FOM_T$ (dBc/Hz)	
[11]	0.13- $\mu$ m CMOS	59	9.8	5.8	-89@1MHz	-18	9.8	-174.9	-174.4	
[12]	0.18- $\mu$ m CMOS	49	1.6	0.8 to 1.1	-101 @1MHz	-11	45	-178	-163	
[13]	0.18- $\mu$ m CMOS	63	1.07	0.67	-89@1MHz	-15	74	-166	-147	
[14]	90-nm CMOS	58.4	9.32	5.2	-91@1MHz	-9.7	8.1	-177.2	-176.6	
		61.7	4.81	2.9	-90@1MHz	-19	1.2	-185	-178.6	
[15]	65-nm CMOS	73.8	41.1	32	-105 to -112 @10MHz	-20	8.4 to 10.8	-172 to -180	-184.2 to -192.2	
[16], [17]	65-nm CMOS	56	17	9.3	-99.4 @1MHz	-9.8	15	-182.2	-186.8	
[18], [19]	90-nm CMOS	56.7	14	8.8	-118.7 @10MHz	-11	8.7	-184.3	-187.4	
[20]	65-nm CMOS	76.5	6.3	4.8	-109 @10MHz	--	14.3	-174.6	-170.6	
[21]	65-nm CMOS	76.5	16	10.6	-108.4 @10MHz	--	14.3	-184	-185.2	
[22]	90-nm CMOS	42	5	1.8	-102.7 @1MHz	--	11.1	-184.9	177.4	
[23]	90-nm CMOS	43	4.1	1.77	-102.7 @1MHz	--	11.1	-183	-177.1	
[24]	0.13- $\mu$ m CMOS	45	4.4	2	-103 @3MHz	--	4	-180.7	-173.5	
[25]	90-nm CMOS	55.7	17	9.4	-119 @10MHz	-7	10.2	-183.4	-188	
[26]	90-nm CMOS	60	0.17	0.1	-100 @1MHz	--	1.9	-193	-157.2	
[27]	90-nm CMOS	61	6	10	-90@1MHz	-5	8.52	-176.8	-176.3	
[28], [29]	90-nm CMOS	L-DCO	59.2	5.94	10	-93@1MHz	-3.4	12	-178.1	-177.9
		T-DCO	58.7	5.72	9.75	-94@1MHz	--	14	-178.3	-177.9
[31]	0.18- $\mu$ m CMOS	38	20	7.5	-100.2 @1MHz	-9.1	27	-177.9	-183.9	
[32]	65-nm CMOS	163	14	23	91.3 @1MHz	-14.5	33	-179.7	-182.6	

Table 1.3: State-of-the-art comparison

As mentioned before, due to different BEOL it is difficult to compare the performances of proposed VCO topology within a particular category. Hence different topologies are designed in same BEOL in order to recognize better the advantage offered by certain topology.

There are two possible solutions to improve the  $Q$ -factor of the resonator. The first solution could be the use of variable/switchable inductor instead of utilizing varactors. However the design and implementation of variable or switchable inductor is difficult. The second possible solution is to use very high- $Q$  inductor, which is difficult to implement with lumped inductor. Instead, using a distributed inductor, based on transmission lines, can be envisaged at mm-wave frequencies, since their physical length becomes more and more reasonable as the

working frequency increases. Therefore, in this thesis the later solution is employed; S-CPS VCOs are designed which is easy to implement and achieve high  $Q$ -factor. So, in this thesis differential slow-wave transmission line [33], i.e. S-CPS is employed in the resonator instead of lumped inductor.

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## 2. CONVENTIONAL LC TANK VCO FOR E-BAND APPLICATIONS

As discussed in chapter 1 several VCO design issues and solutions have been reported in literature [1] - [7]. Among the proposed solutions one of the major part deals with lumped *LC*-tank based topologies, i.e. having either a conventional *LC*-tank topology or involving concept of mutual coupling or switchable inductors and the second part deals with hybrid topologies, i.e. involving both lumped and high-*Q* distributed components. From this comparison of different topologies we can conclude that improving the VCO performance in terms of frequency tuning range, phase noise or power consumption is difficult to achieve with technology varactors as they have degrading *Q*-factor with increase in frequency specifically at mm-wave. The design and implementation of switchable inductors is difficult. So instead use of high-*Q* (33) distributed inductors is a better option to start with, as it is easy to design.

Before moving on to the VCO design with topologies based on distributed inductor, in this chapter we deal with a conventional *LC*-tank VCO. This VCO has been designed for comparing with the proposed topologies (based on slow-wave structures) presented in this thesis. In section 2.1 a common VCO design methodology has been defined for designing all the VCOs of the thesis. For designing *LC*-tank VCO the characteristic of technology inductor and varactors have been analyzed in section 2.2 along with the loss estimation technique of *LC* tank. Section 2.3 determines the CCP and output buffer design and its optimization in order to have less loading capacitance. And finally in section 2.4 the VCO design with *LC*-tank has been given.

### 2.1 VCO Design Methodology

Figure 2.1 shows the topology of a conventional *LC*-tank VCO. Due to its relatively good Phase Noise (PN) performance, the topology of cross-coupled differential CMOS *LC*-tank oscillator has been a common circuit structure in classical VCOs [1]. As shown in Figure 2.1, the *LC*-tank VCO consists of nMOS cross-coupled differential pair ( $M_1, M_2$ ). For tuning oscillator frequency, two varactors are employed. To minimize the load on the oscillator core and to obtain a 50  $\Omega$  output matching, output buffers are also considered. Hence, the transistors ( $M_3, M_4$ ) and transmission lines sizes are chosen such that the loading effect on VCO core is minimized while maintaining the sufficient output swing (explained in Section 2.3.2).

The nMOS cross-coupled pairs are employed to provide a negative resistance i.e.  $R_{negative} = 2/G_m$ , for compensating the losses added by *LC*-tank resonator. Figure 2.2 shows a simplified equivalent circuit for oscillation frequency and startup conditions derivation.

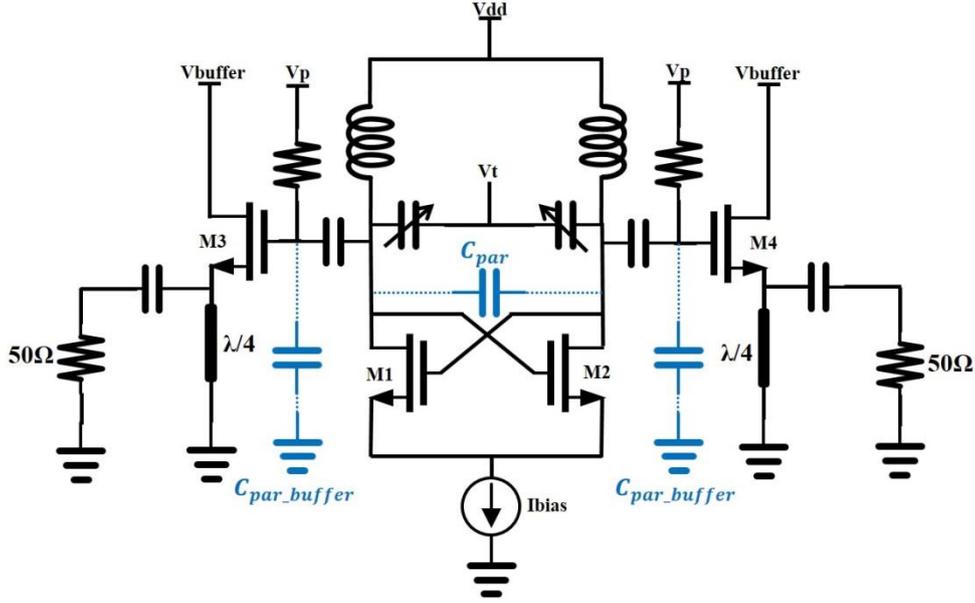


Figure 2.1: Schematic of LC tank VCO

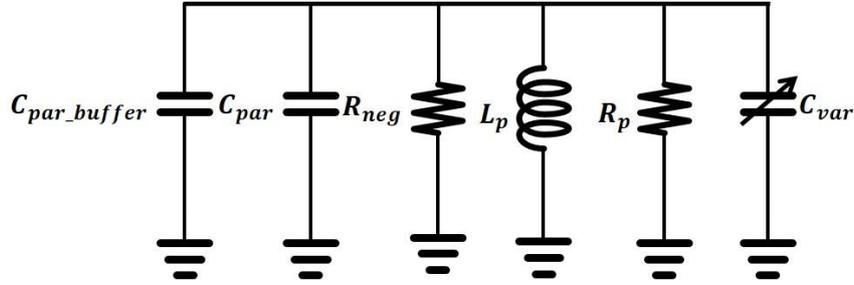


Figure 2.2: Simplified model for circuit analysis

According to narrowband approximation,  $L_p$ ,  $C_p$  and  $R_p$  can be estimated as,

$$L_p = L \quad (2.1)$$

$$C_p = C_{var} + C_{par} + (C_{par\_buffer} \times 2) \quad (2.2)$$

$$R_p = \frac{(R_{p\_var} \times R_{p\_ind})}{(R_{p\_var} + R_{p\_ind})} \quad (2.3)$$

where,  $L_p$  is the equivalent inductance,  $C_p$  is the equivalent capacitance,  $R_p$  is the equivalent parallel resistance of LC tank,  $C_{var}$  is the varactor capacitance,  $C_{par}$  is the parasitic capacitance added by the nMOS cross-coupled,  $C_{par\_buffer}$  is the parasitic capacitance added by each output buffer circuit,  $R_{p\_var}$  represents the equivalent parallel resistive losses of varactor and  $R_{p\_ind}$  represents the equivalent parallel resistive losses of inductor.

All the parasitic capacitances have been highlighted in Figure 2.1. As discussed in chapter 1, LC tank oscillator is considered as a two stage looped amplifier. So, the Barkhausen criteria states that the circuit will sustain steady-state oscillations only at frequencies for which,

- The loop gain is equal to unity in absolute magnitude, i.e.  $|G_m \cdot Z(j\omega_0)^2| > 1$ , and

- The phase shift around the loop is zero or integer multiple of  $2\pi$ , i.e.  $\angle G_m \cdot Z(j\omega_0) = 0$  or  $2\pi n$ . Thus,  $G_m > 1/R = 2/R_p$  and  $\omega_0 = 1/\sqrt{LC}$ .

The oscillation frequency ( $F_{osc}$ ) and the startup condition are given by eq. (2.4) and eq. (2.5), respectively.  $R_p$  in eq. (2.5) is incurred by the losses from the varactor and inductor of the LC-tank.

$$F_{osc} = \frac{1}{2\pi\sqrt{LC_p}} \quad (2.4)$$

$$G_m = LCF \times (2/R_p) \quad (2.5)$$

where,  $G_m$  is the trans-conductance of nMOS cross-coupled pair and  $LCF$  is the loss compensation factor needed to ensure that the oscillation starts ( $G_m > 1/R = 2/R_p$ ).

The above mentioned eq. (2.5) can also be explained in terms of  $R_{negative}$  and  $LCF$ , given by eq. (2.6).

$$R_{negative} = \frac{R_p}{LCF} \quad (2.6)$$

where  $R_{negative}$  is inverse of trans-conductance ( $G_m$ ).

The LCF of the VCOs presented in this thesis has been kept close to 3 and can be expressed by eq. (2.7).

$$LCF = \frac{R_p}{R_{negative}} \quad (2.7)$$

Hence, for designing VCO after determining the equivalent  $R_p$  of the LC-tank  $R_{negative}$  is chosen so that the ratio given in eq. (2.7) is equivalent to 3.

At mm-wave, it is difficult to provide sufficient negative resistance to cancel the losses of the resonator because the core transistors cannot be very large due to the parasitic capacitance they add to the tank, thus limiting the oscillation frequency. The conductance of nMOS transistor is given by eq. (2.8):

$$G_m = \sqrt{2K_n \frac{W}{L} I_d} \quad (2.8)$$

So, to achieve sufficient negative resistance ( $2/G_m$ ) with less parasitic capacitance, we altered firstly the size of the transistor ( $W/L$ ), secondly the tail or bias current ( $I_d$ ). In other words, smaller ( $W/L$ ) are chosen, for a given power budget, since it will reduce the parasitic capacitance. Hence the frequency tuning range will be less affected. The characteristics of nMOS cross-coupled pair in BiCMOS 55 nm technology is explained in Section 2.3.1, i.e. variation in ( $G_m$ ) and ( $C_{par}$ ) versus ( $W/L$ ) and ( $I_d$ ).

Therefore, a design methodology for designing the mm-wave (E-band in this thesis) VCO is needed in order to provide a good compromise between several performance parameters. As remarked in Chapter 1 also (Section 1.2), the  $Q$ -factor of the LC tank is the most critical

design parameter, as it leads to degradation of frequency tuning range and phase noise, with increment in power consumption of overall circuit. Thus, the design methodology can be briefly explained in four steps:

- (a) Firstly the tank capacitance and inductance are fixed according to desired oscillation frequency ( $\approx 81$  to  $86$  GHz in this thesis). The tank is optimized to maximize the Q factor.
- (b) The second step consists of determining  $R_p$ , which give the value of  $R_{negative}$  and  $C_{Par}$ .
- (c) The cross-coupled pair has been designed to achieve the minimum  $C_{Par}$  for the given  $R_{negative}$  and a chosen LCF.
- (d) Then the last step is to change the tank capacitance and inductance again according to the required oscillation frequency, given in eq. (2.4), because the  $F_{osc}$  shifts due to added  $C_{Par}$ .

To follow the above mentioned methodology, several parameters must be studied, i.e. the characteristics of inductor and varactor from the BiCMOS 55 nm technology.

## 2.2 Characteristics of inductor & varactor from BiCMOS 55nm technology

The minimum  $Q$ -factor of a LC tank is given by eq. (2.9),

$$\frac{1}{Q_{Tank}} = \frac{1}{Q_{Ind}} + \frac{1}{Q_{Var\_min}} \quad (2.9)$$

where,  $Q_{Ind}$  is the  $Q$ -factor of inductor and  $Q_{Var\_min}$  is the minimum  $Q$ -factor of varactor. These  $Q$ -factors are given by eq. (2.10) and eq. (2.11).

$$Q = X_s/R_s = R_p/X_p \quad (2.10)$$

$$R_s = R_p/(1 + Q^2) \quad (2.11a)$$

$$X_s = X_p \cdot Q^2/(1 + Q^2) \quad (2.11b)$$

Figure 2.3 shows the conversion between series/ parallel RL/ RC networks, where,  $R_s$  and  $R_p$  are the series and parallel resistive losses, respectively, while,  $X_s$  and  $X_p$  are the series and parallel reactance, respectively. From eq. (2.10) and eq. (2.11) inductance and capacitance values can be computed.

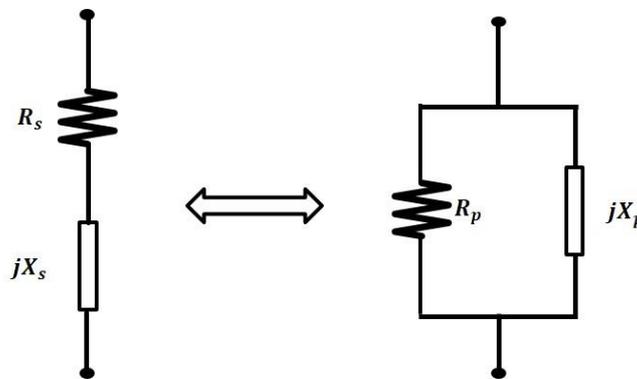


Figure 2.3: Interconversion between series/ parallel RL/ RC network

In this section the characteristics of inductor and varactor are studied, i.e. the  $Q$ -factor, losses ( $R_s$ ) and inductance/capacitance versus variation in dimension and control voltage, etc. Characteristics of inductor and varactor need to be studied before designing the VCO in order to choose a good  $Q$ -factor LC tank. All the simulation results presented in this section were performed at 83.5 GHz, as the targeted frequency of oscillation for VCO design is from 81 GHz to 86 GHz.

### 2.2.1 Characteristic of Inductor in BiCMOS 55 nm Technology:

Due to the chosen design topology of the oscillator i.e. cross-coupled differential CMOS LC-tank oscillator, we need to study the differential inductor provided in the technology. Figure 2.4 shows the layout of the differential inductor with its two variables, i.e. width of coil ( $W$ ) and diameter ( $D$ ).

Please note that the DC bias is kept 1.2 V as needed in VCO design (explained in detail in section 2.3 and 2.4).

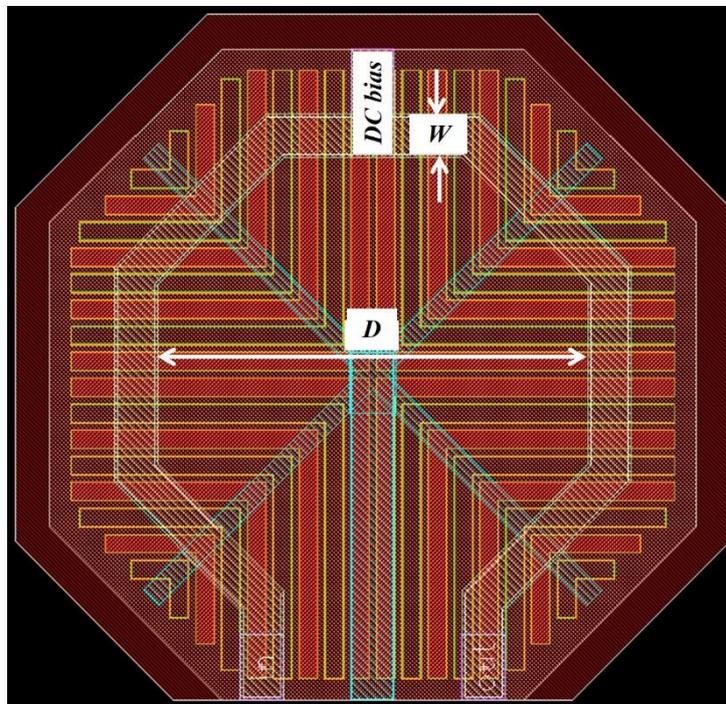


Figure 2.4: Layout view of differential inductor in BiCMOS 55 nm technology

The BiCMOS 55 nm process allows diameters from 44  $\mu\text{m}$  to 440  $\mu\text{m}$ , and coil width from 5.5  $\mu\text{m}$  to 33  $\mu\text{m}$ . Figure 2.5(a) shows the variation in inductance ( $L$ ) value with respect to change in diameter and width of the coil. As shown in Figure 2.5(a), the increase in Diameter of the coil leads to an augmentation of the inductance value because by increasing the diameter, the area of the coil is increasing, and the magnetic flux grows accordingly. Nevertheless when the width of the coil's strip is increased the inductance value is reduced because the increase in width (i) reduces the area of the coil and (ii) decreases the magnetic field in the loop (the current in the middle of the strips produces less magnetic field), hence reducing the overall magnetic flux. Similarly, Figure 2.5(b) shows the variation in equivalent series resistance with respect to change in diameter and width of the coil. As expected, the series resistance grows with the increase in diameter and reduction in width of the coil. This behavior is continuous only up to 60  $\mu\text{m}$  of the diameter of the coil. After that, the series

resistance increases with the width of the coil as well. Figure 2.5(c) shows the variation in the  $Q$ -factor of the inductor with respect to change in diameter and width of the coil. The  $Q$ -factor of the inductor decreases with increase in diameter and width of coil because of the reduction in inductance value and increment in series resistance in both the cases.

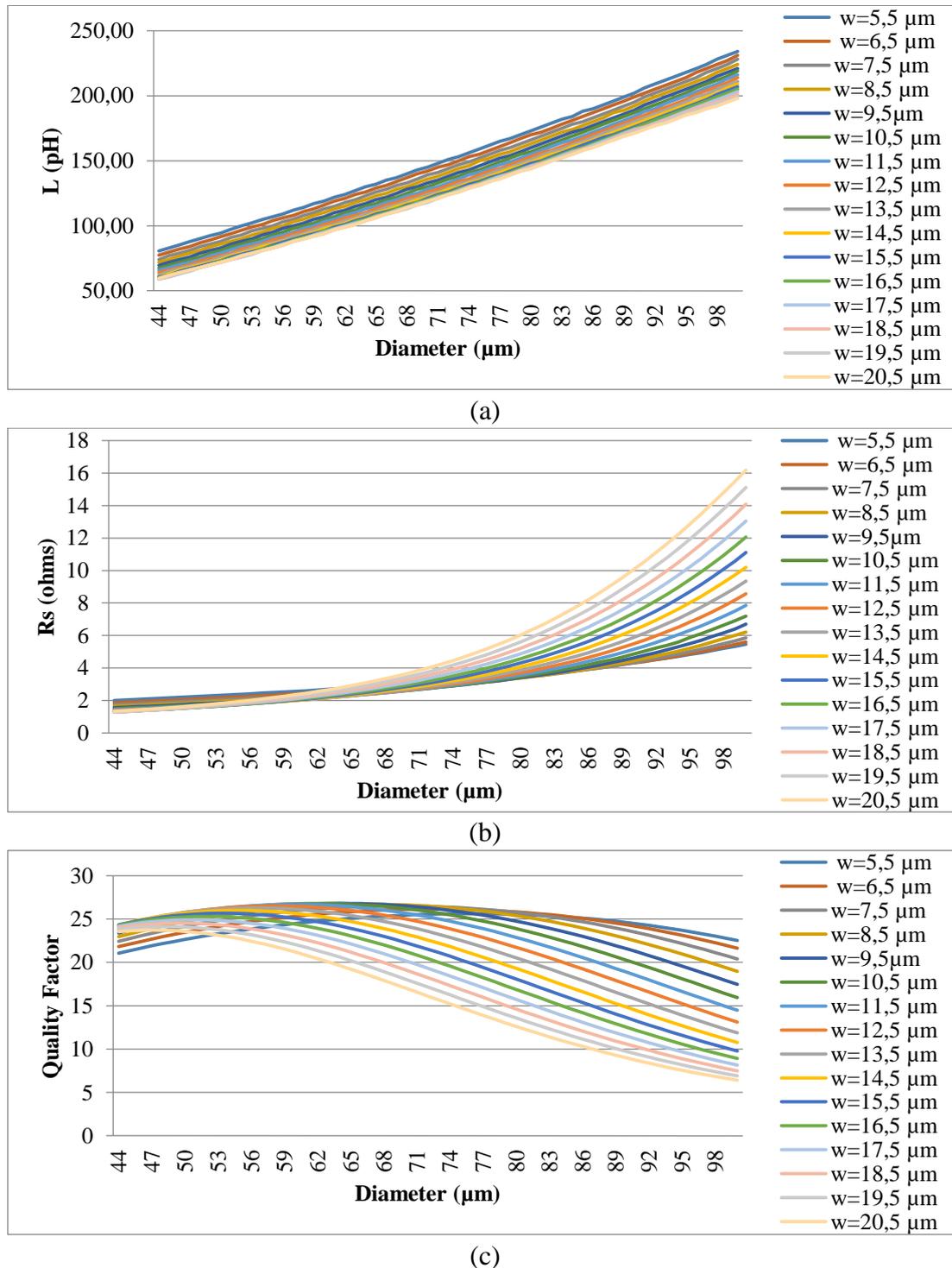


Figure 2.5: (a) Equivalent Inductance, (b) Series resistance, and (c)  $Q$ -factor variation versus variation in diameter and width of inductors coil

As observed in Figure 2.5(c) the resistive losses increases exponentially after 60  $\mu\text{m}$  diameter, hence reducing the  $Q$ -factor. So, the while choosing the inductor for VCO design, it has been kept within the limit of 60  $\mu\text{m}$  diameter.

### 2.2.1 Characteristic of Varactor in BiCMOS 55 nm Technology

In BiCMOS 55 nm technology MOS diode based varactors are available. Due to their performances at mm-wave frequencies, these devices are good candidates for LC tank design. To analyze the performance of varactor from the BiCMOS 55 nm technology, there are four design parameter effects to study i.e. number of fingers ( $N_f$ ), number of cells ( $N_{bcells}$ ), finger width ( $W$ ) and length ( $L$ ), as shown in the layout view of varactor in Figure 2.6. Apart from these three parameters, there is another parameter, i.e. the bias voltage which varies from 0 V to 2.4 V. This bias voltage must be applied to the varactor. To bias the varactor a control voltage is applied to either of the terminal and the other terminal must be connected with the constant bias voltage of 1.2 V.

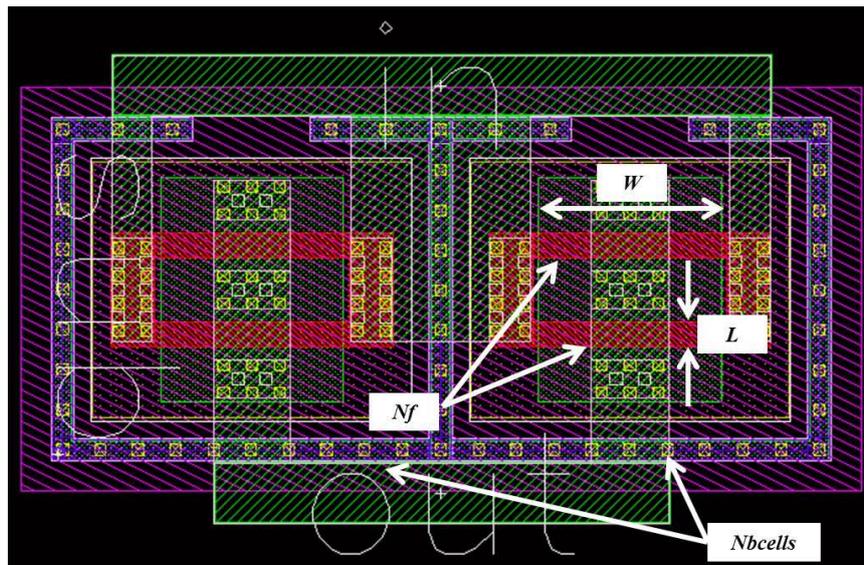


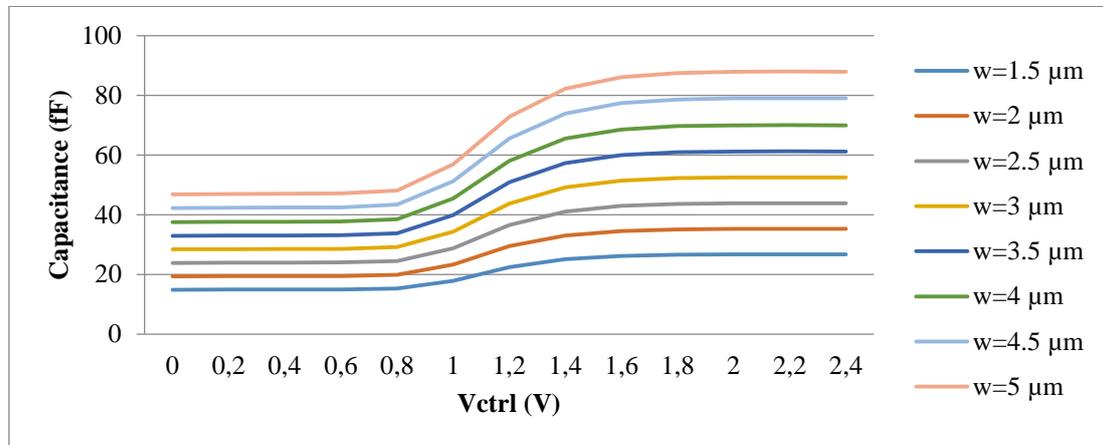
Figure 2.6: Layout view of varactor in BiCMOS 55 nm technology

Starting from the parameters “ $N_f$ ” and “ $N_{bcells}$ ” it must be noted that increasing these design parameters increases the number of devices in parallel and thus increases the capacitance value. But, increasing capacitance value will lead to  $Q$ -factor reduction. Hence while performing these preliminary simulations we chose  $N_f, N_{bcells} = 2$  (choosing these values of  $N_f$  and  $N_{bcells}$  is only a used case and is not a definite choice). For  $N_f, N_{bcells} = 2$  it is then possible to study the effect of the other design parameters, i.e. finger width ( $W$ ) and length ( $L$ ), with a voltage tuning from 0 to 2.4 V. Figure 2.7 (a) to (c) shows the variation of the capacitance, tuning ratio and  $Q$ -factor, for different values of finger width ( $W$ ) versus tuning voltage. For the first set of simulations the length of varactor was set to its minimum value, i.e.  $0.06 \mu\text{m}$ .

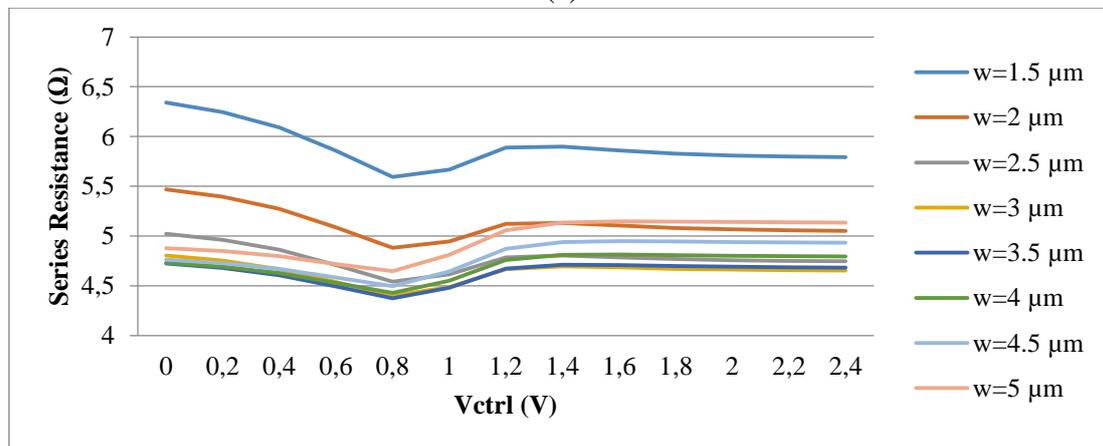
Increasing the finger width increases the capacitor, as observed in Figure 2.7(a). In Figure 2.7(b) it can be observed that series resistance does not vary a lot versus width, hence reduction of the  $Q$ -factor is expected, as observed in Figure 2.7(c). Figure 2.8 shows the tuning ratio variation versus finger width. The small variation (4.2 %) that is observed is due to the fact that the effective capacitance of MOS varactors is dependent on its effective length in saturation and non-saturation region. But in off state this effective capacitance is dependent on both effective width of the gate and length of the channel. Hence, as the length was constant for this set of simulations, the tuning range is also quite constant.

Figure 2.8 shows the tuning ratio variation versus finger width. The small variation (4.2 %) that is observed is due to the fact that the effective capacitance of MOS varactors is

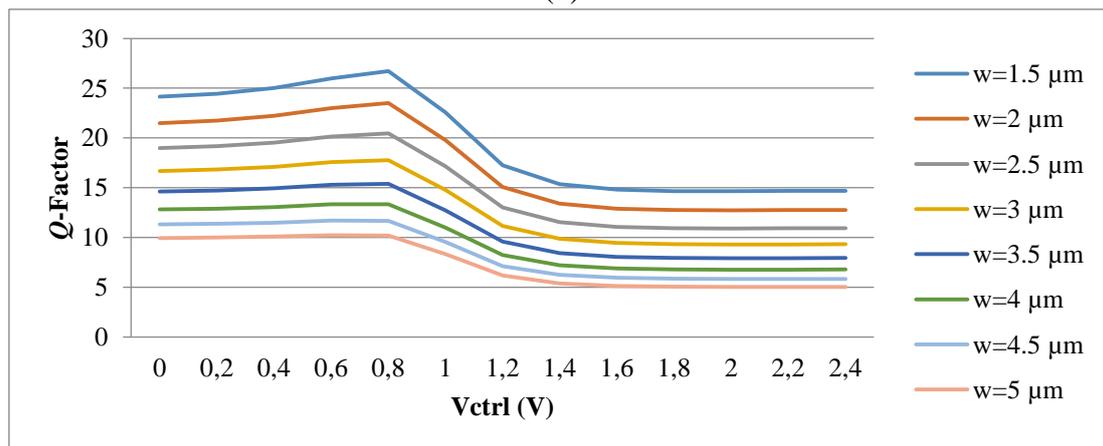
dependent on its effective length in saturation and non-saturation region. But in off state this effective capacitance is dependent on both effective width of the gate and length of the channel. Hence, as the length was constant for this set of simulations, the tuning range is also quite constant.



(a)



(b)



(c)

Figure 2.7: (a) Equivalent capacitance, (b) Series resistive losses, and (c)  $Q$ -factor versus variation in tuning voltage and Finger width (W)

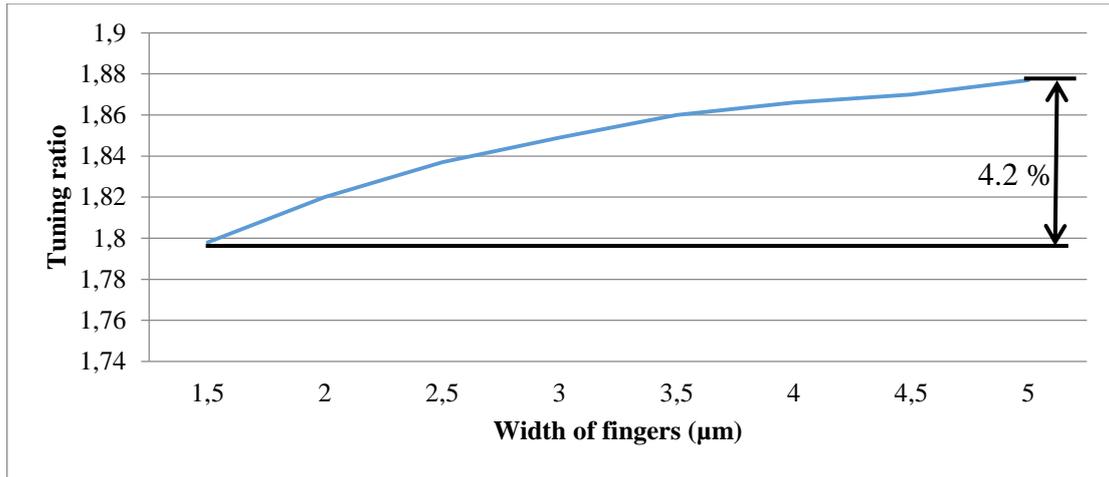
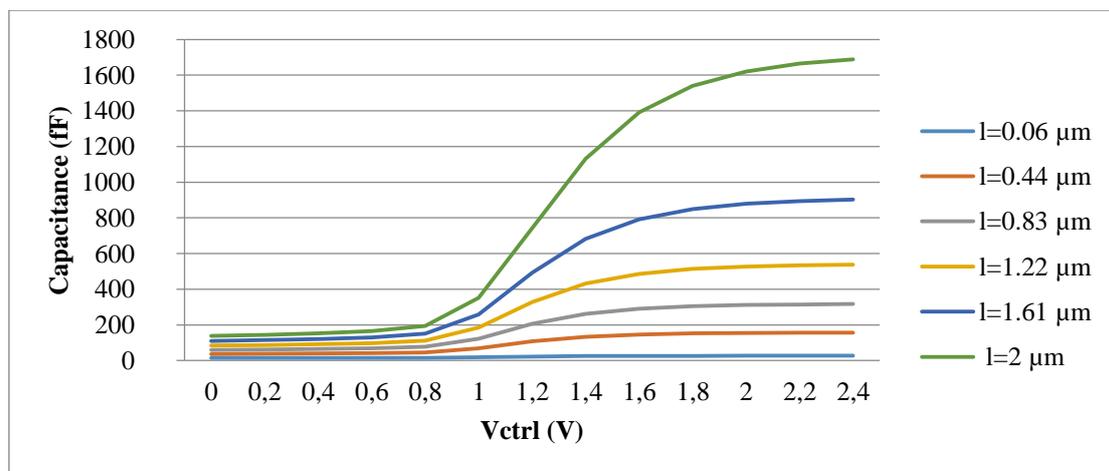


Figure 2.8: Tuning ratio variation versus Finger width

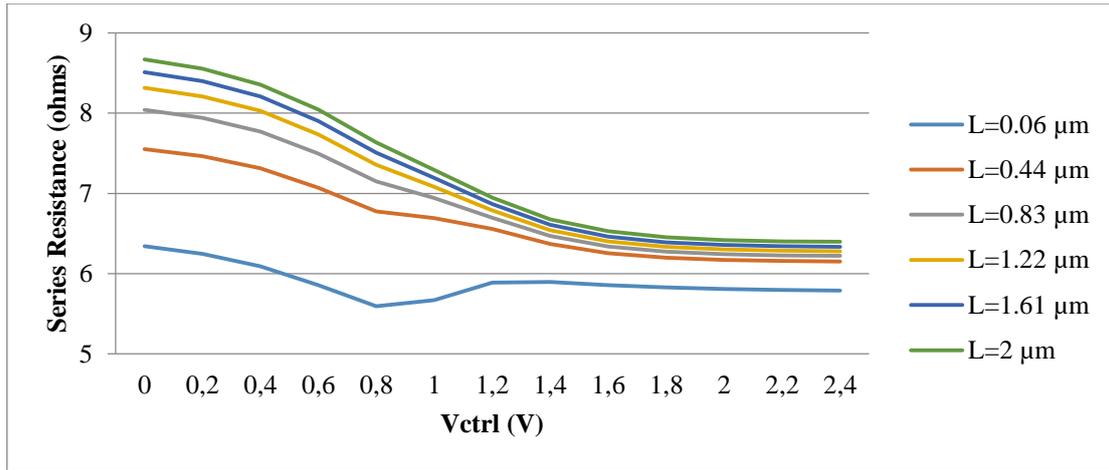
Figure 2.9 shows the characteristics of the varactor with respect to change in length. The width of fingers was kept  $1.5 \mu\text{m}$  for this set of simulations. As shown in Figure 2.9(a), the capacitance increases with the length, as the associated resistive losses increases, because the channel conductance is dependent on the channel length modulation parameter. Channel length modulation (CLM) is the shortening of the length of the inverted channel region which occurs for large drain bias voltages. The result of CLM is an increase in current with the drain bias and a reduction of the output resistance. Hence, as the resistive losses increase versus length,  $Q$ -factor reduces significantly, as shown in Figure 2.9 (b) & (c), respectively.

As mentioned before, the tuning ratio of the varactor is primarily depending on the length of the varactor. This point is evident from the plot shown in Figure 2.10, in which the tuning range changes from 1.8 to 12 as the length changes from  $0.06 \mu\text{m}$  to  $2 \mu\text{m}$ , respectively.

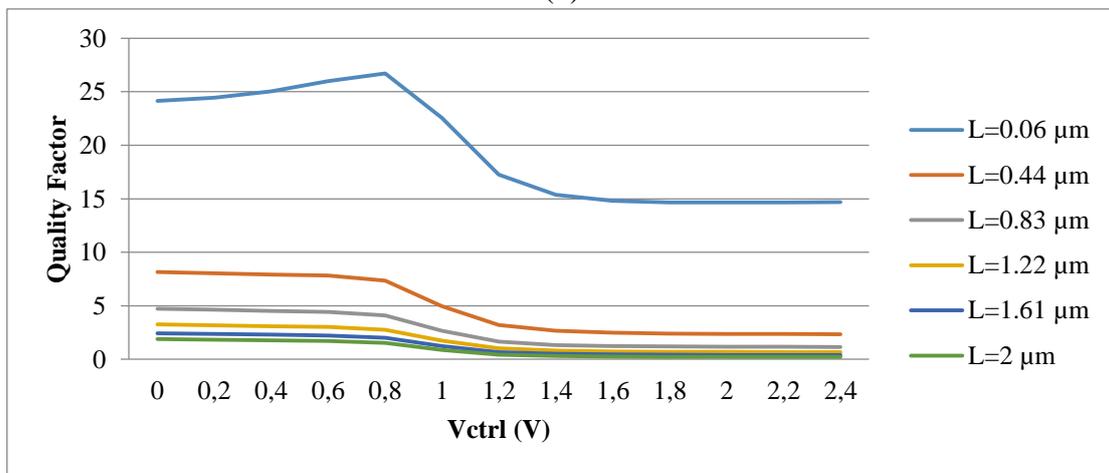
So, as observed in Figure 2.10 that increment in length leads to increment in tuning ratio of varactor, but at the same time it also leads to rigorous reduction in  $Q$ -factor due to increment in series resistive losses. So, high tuning ratio and high  $Q$ -factor are not possible to achieve from the same MOS varactor. Hence, for designing the LC tank, varactor with small tuning range (enough to cover the aimed frequency band) and high- $Q$  will be chosen.



(a)



(b)



(c)

Figure 2.9: (a) Equivalent capacitance, (b) Series resistive losses, and (c)  $Q$ -factor versus variation in tuning voltage and Length ( $L$ )

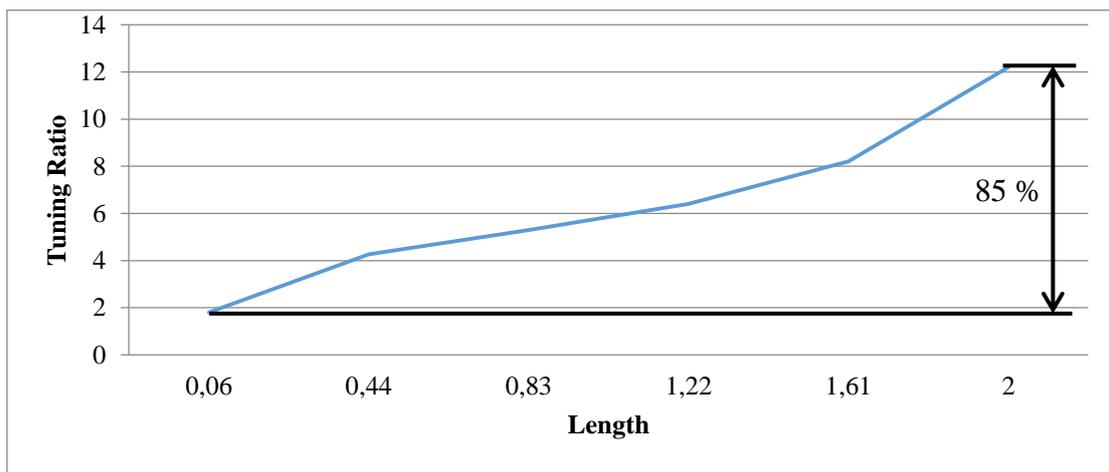


Figure 2.10: Tuning ratio variation versus Length

### 2.2.2 Loss estimation of LC tank: one-port method

The next step for designing the VCO is to determine the equivalent parallel resistive losses (i.e.  $R_p$ ) of the LC tank. For the same one-port method was used. The one-port method states that a high impedance/resistance port must be connected across the LC tank circuit, as shown

in Figure 2.11, (so that the equivalent  $R_p$  of the LC tank should not be altered) and the real part of the impedance seen from the port gives the value of equivalent parallel resistance ( $R_p$ ) of the LC tank. This same value of  $R_p$  can also be obtained by converting the series resistive losses of inductor and varactor individually.

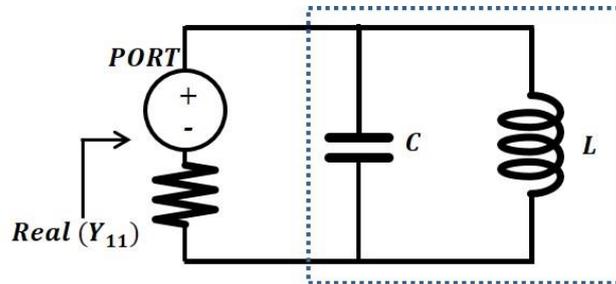


Figure 2.11: One-port Method

Thus eq. (2.12) gives equivalent impedance of the LC tank seen from the high impedance port and eq. (2.13) gives the equivalent parallel resistive losses of LC tank, which will be further used in next section to determine the needed negative resistance for loss compensation of LC tank.

$$Y_{11} = \frac{1}{R_p} + j \left( \omega C - \frac{1}{\omega L} \right) \quad (2.12)$$

$$\text{Real} (Y_{11})^{-1} = R_p \quad (2.13)$$

## 2.3 nMOS cross-coupled pair and optimum output buffer design

The loss compensation factor that has been mentioned in section 2.1 is actually modelled by a nMOS cross-coupled pair (CCP). Based on the LCF value the dimension of CCP is chosen, but the same CCP adds parasitic capacitance ( $C_{par}$ ), big enough to reduce the tuning range and shift the frequency of oscillation to a lower frequency band. So, in section 2.3.1 the negative resistance ( $R_{negative}$ ) and parasitic capacitance ( $C_{par}$ ) added by nMOS CCP has been modelled. Also a methodology to reduce  $C_{par}$  and the power consumption has been given in this section 2.3.1.

### 2.3.1 nMOS Cross-Coupled Pair: Negative Resistance & Capacitance modelling

The next step to design the VCO is to design nMOS Cross-Coupled Pair (CCP), in order to attain the needed loss compensation ( $LCF \approx 3$  in our design). In other words, we can say that the needed nMOS CCP must be designed to have  $R_{negative} = R_p/3$ . At the same time, the parasitic capacitance ( $C_{par}$ ) added by CCP must be determined also, as it will shift  $F_{osc}$  and reduce the frequency tuning range (FTR) as well. Figure 2.12(a) shows the schematic of nMOS CCP. Their common source has a constant voltage value because the circuit has a symmetrical structure and the output of CCP is differential. Hence, in differential mode this point is a virtual ground which leads to the small-signal model shown in Figure 2.12(b). Moreover, each transistor model considers five intrinsic capacitances, as shown in Figure 2.12(b),  $C_{gs}$ ,  $C_{db}$ ,  $C_{ds}$ ,  $C_{gb}$  and  $C_{gd}$ . As bulk and source voltages are at a virtual ground, the capacitances  $C_{sb}$  are short-circuited in the differential mode small-signal model. Since the transistors are considered identical and the gate of one transistor is connected to the drain of

the other, hence a simplified differential model is as shown in Figure 2.12(c). The schematic shown in Figure 2.12(a), with a high impedance port connected across drain, was used to determine the approximate value of  $R_{negative}$  and  $C_{par}$ , by using eq. (2.15)(2.15) and eq. (2.16), respectively.

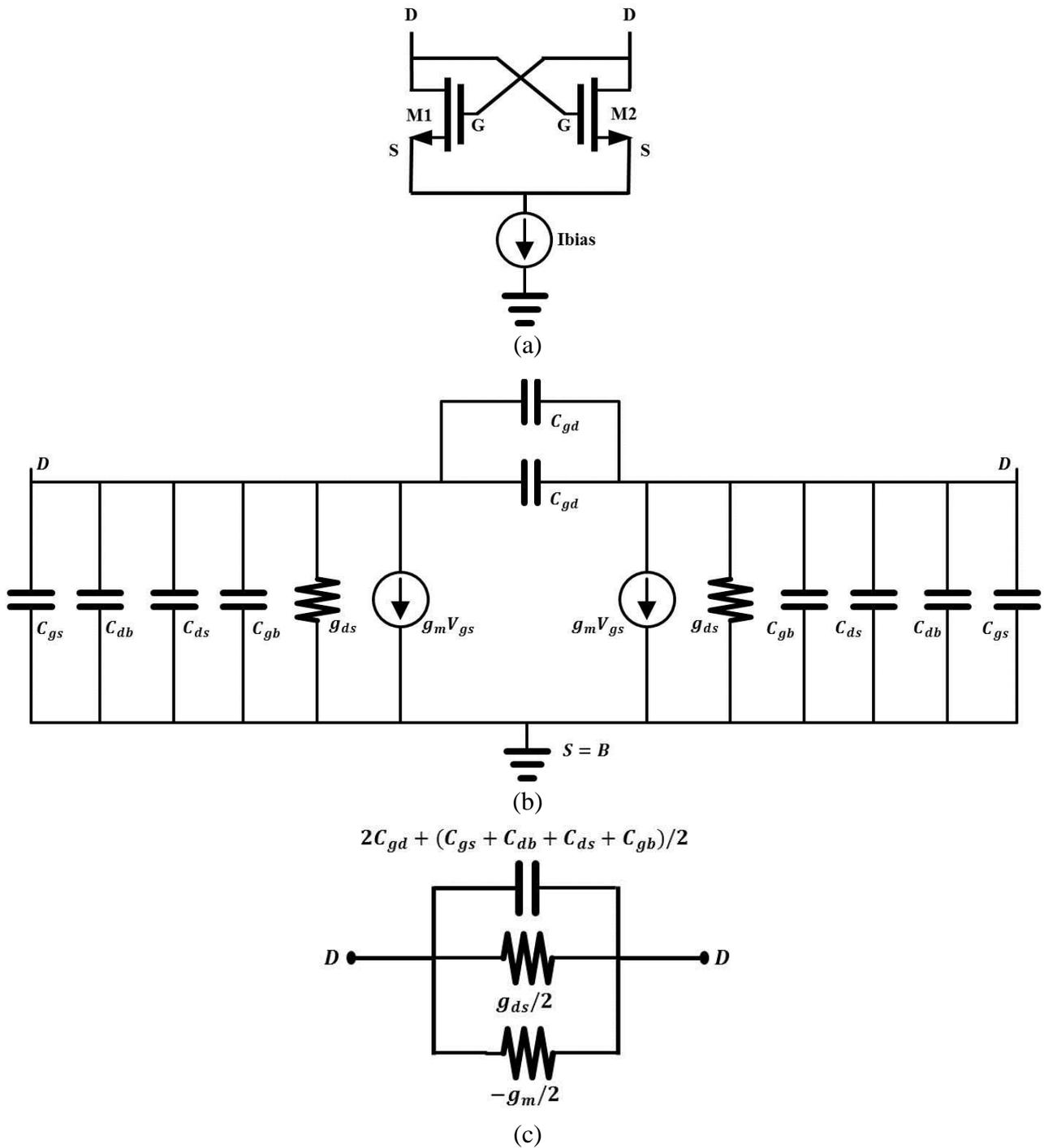


Figure 2.12: (a) nMOS Cross-Coupled pair, (b) Equivalent Small-Signal model, and (c) Simplified equivalent model

$$Y_{11} = \frac{1}{R_{negative}} + j\omega C_{par} \quad (2.14)$$

$$Real(Y_{11})^{-1} = R_{negative} \quad (2.15)$$

$$\frac{\text{Imag}(Y_{11})}{\omega} = C_{par} \quad (2.16)$$

The variation of both  $R_{negative}$  and  $C_{par}$  with bias current ( $I_d$ ) and size of transistor is shown in Figure 2.13. As shown in Figure 2.13(a),  $R_{negative}$  increases first linearly and then remains quite constant versus  $I_d$ .  $R_{negative}$  also increases with the transistor width ( $W$ ). Similarly,  $C_{par}$  increases with both  $I_d$  and  $W$  (Figure 2.13(b)).

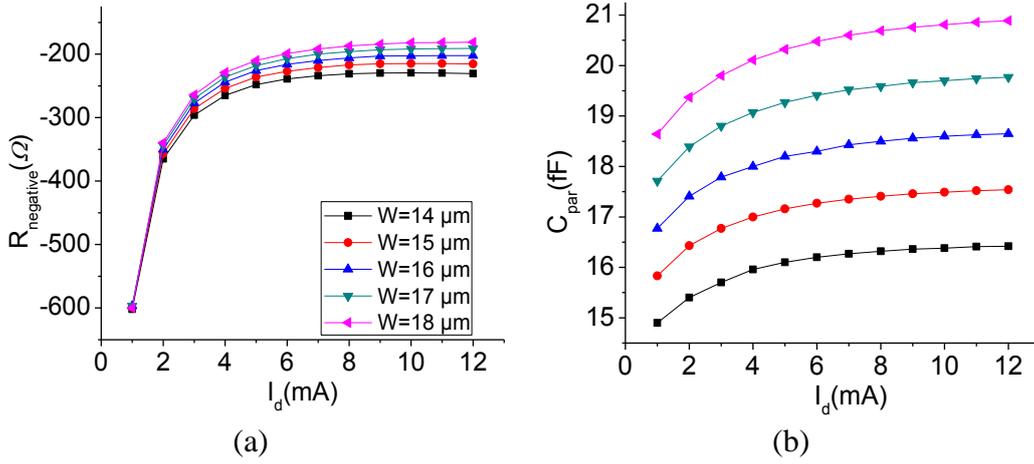


Figure 2.13: (a) Negative resistance ( $R_{negative}$ ); (b) Parasitic capacitance ( $C_{par}$ ) of nMOS cross-coupled pair

As per the design methodology described in introduction of section 2.1, there exist many possible combinations of ( $W/L$ ) and ( $I_d$ ) to attain a given value of  $R_{negative}$ . For example, referring to Figure 2.13,  $R_{negative} = -240 \Omega$  can be obtained for:

- (a)  $W = 18 \mu m$  and  $I_d = 3.8 mA$ , leading to  $C_{par} \approx 21 fF$ , or
- (b)  $W = 14 \mu m$  and  $I_d = 5.8 mA$ , leading to  $C_{par} \approx 16 fF$ .

This simple example clearly shows the trade-off between power consumption and parasitic capacitance. The CCP is sized to achieve the needed  $R_{negative}$  with the smallest  $W$  for a given  $I_d$  in order to minimize the parasitic capacitance. To do so, CCP is biased at the limit of the velocity saturation region which has been represented in the Figure 2.13(a) by the flat section of the curve.

### 2.3.2 Optimized output buffer for measurement

The main reason for designing the buffer is for the VCO measurement, i.e. to convert high output impedance of VCO core to a  $50 \Omega$  load matched to the measurement equipment. For output buffer design a source follower amplifier has been utilized, shown in Figure 2.14.

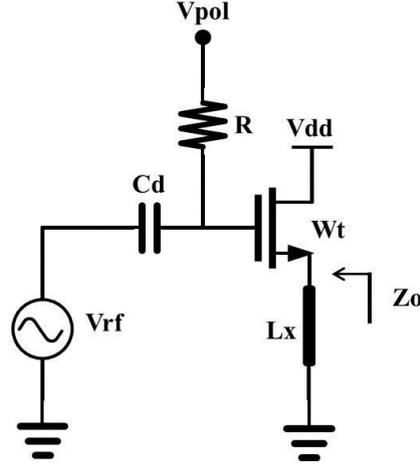


Figure 2.14: Source follower buffer circuit

The real part of output impedance is given by  $gm$  (i.e.  $Re(Z_0) = 1/gm$ ). The transmission line ( $L_x$ ) acts as a parallel stub that cancels the imaginary part of the output.

To design the buffer, following method has been considered. First, the width of the transistor is determined to achieve  $gm = 20\text{ mS}$ . The gate is biased at  $V_{dd}$  to simplify the biasing scheme and avoid the use of dc blocking capacitor  $C_d$ . In this step, to achieve simulation, the transmission line is sized to  $\lambda/4$  in order to add an open circuit at  $F_0$ . Once the size of the transistor is set,  $L_x$  (length of transmission line) is adjusted to cancel the imaginary part seen at the output. The final design parameters of this buffer design for the E-band VCO are given in Table 2.1.

$L_x$	196 $\mu\text{m}$
$W_x$	6.9 $\mu\text{m}$
$W_t$	13.5 $\mu\text{m}$
$V_{pol}$	1.2 V

Table 2.1: Design parameters of source follower buffer circuit

The output buffer design presented above adds  $17\text{ fF}$  of loading capacitance at the VCO output hence reducing dramatically the  $FTR$ . Hence, in order to reduce this loading capacitance added by output buffer (i.e. to reduce the width ( $W_t$ ) of the buffer) an impedance transformer with length ( $L_{x2}$ ) has been used at the output, as shown in Figure 2.15.  $L_{x2}$  can transform the real part of the output impedance of MOS to  $50\Omega$ . It allows synthesizing a larger real part of the MOS output impedance (i.e. a smaller  $gm$ ) which finally reduces  $W$  and hence the parasitic capacitance, refer Table 2.2. Finally, the resultant loading capacitance of the optimized buffer design is almost  $7\text{ fF}$ , i.e. the loading capacitance was reduced by  $60\%$  as compared to topology presented in Figure 2.14.

$L_{x2}$	247.2 $\mu\text{m}$
$W_{x2}$	4 $\mu\text{m}$
$L_x$	150 $\mu\text{m}$
$W_x$	6.9 $\mu\text{m}$
$W_t$	7 $\mu\text{m}$

Table 2.2: Design parameters of optimized source follower buffer circuit

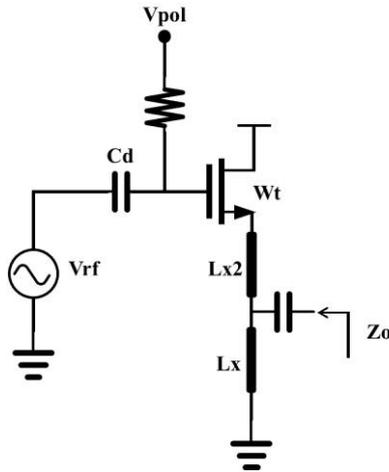


Figure 2.15: Optimized buffer design

## 2.4 LC tank VCO design

### 2.4.1 Summary of Methodology: Flow diagram

Figure 2.16 shows the design methodology flow diagram. Firstly, in step (a) we need to choose the inductor ( $L$ ) and varactor ( $C_{par}$ ) for a given frequency of oscillation. Then in step (b) the equivalent losses ( $R_p$ ) of chosen LC tank are determined. In step (c) the parasitic capacitance ( $C_{par}$ ) is determined as per needed negative resistance ( $R_{negative}$ ). And finally in step (d) the inductor or varactor is adjusted to shift the frequency of oscillation ( $F_{osc}$ ) to the expected value.

As mentioned in section 2.1, there exist one more set of parasitic capacitance that is added by the buffer circuit, needed for impedance transformation. As the designed VCO has a differential topology, this added parasitic capacitance from buffer ( $C_{par\_buffer}$ ) is twice its value. Hence it is necessary to consider these parasitics also, while designing VCO.

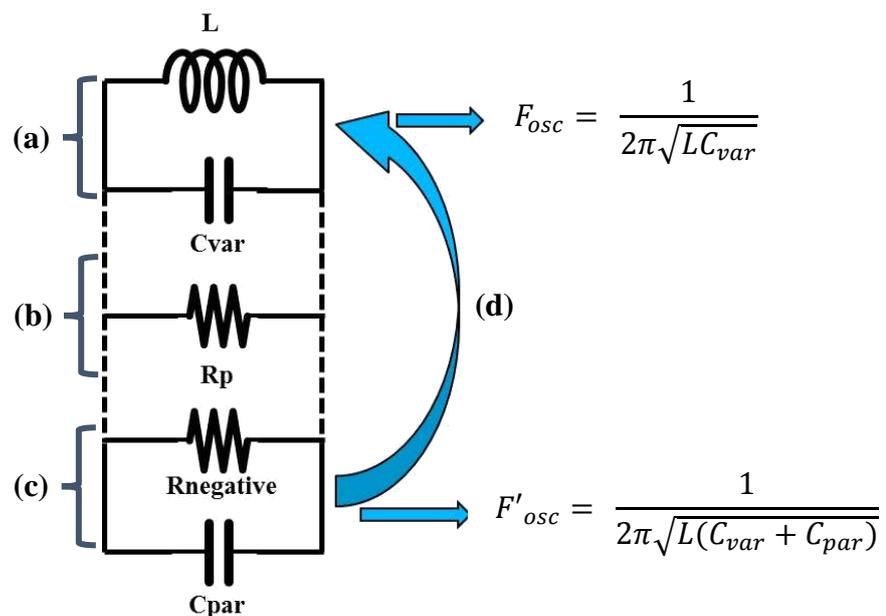


Figure 2.16: Design methodology flow diagram

### 2.4.1 Parametric simulation for $Q$ -factor vs LC tank

In this section, preliminary set of simulations are achieved for determining the variation in the  $Q$ -factor of the LC tank with variation in different set of inductors and varactors, i.e. variation from small inductors & large varactors to large inductors & small varactors. In this section the simulations are done for lower E-band, i.e. 71 - 76 GHz for the purpose of analysis, although the VCO designs presented in this thesis target a center frequency of 83.5 GHz. However, the methodology remains the same.

Figure 2.17 shows the different set of inductor and varactor combination (on x-axis) chosen to give same frequency of oscillation (i.e.  $\approx 71 - 76$  GHz) with  $Q$ -factor of each combination on y-axis. Also, the  $Q$ -factor of inductor and varactor are given individually in Figure 2.17.

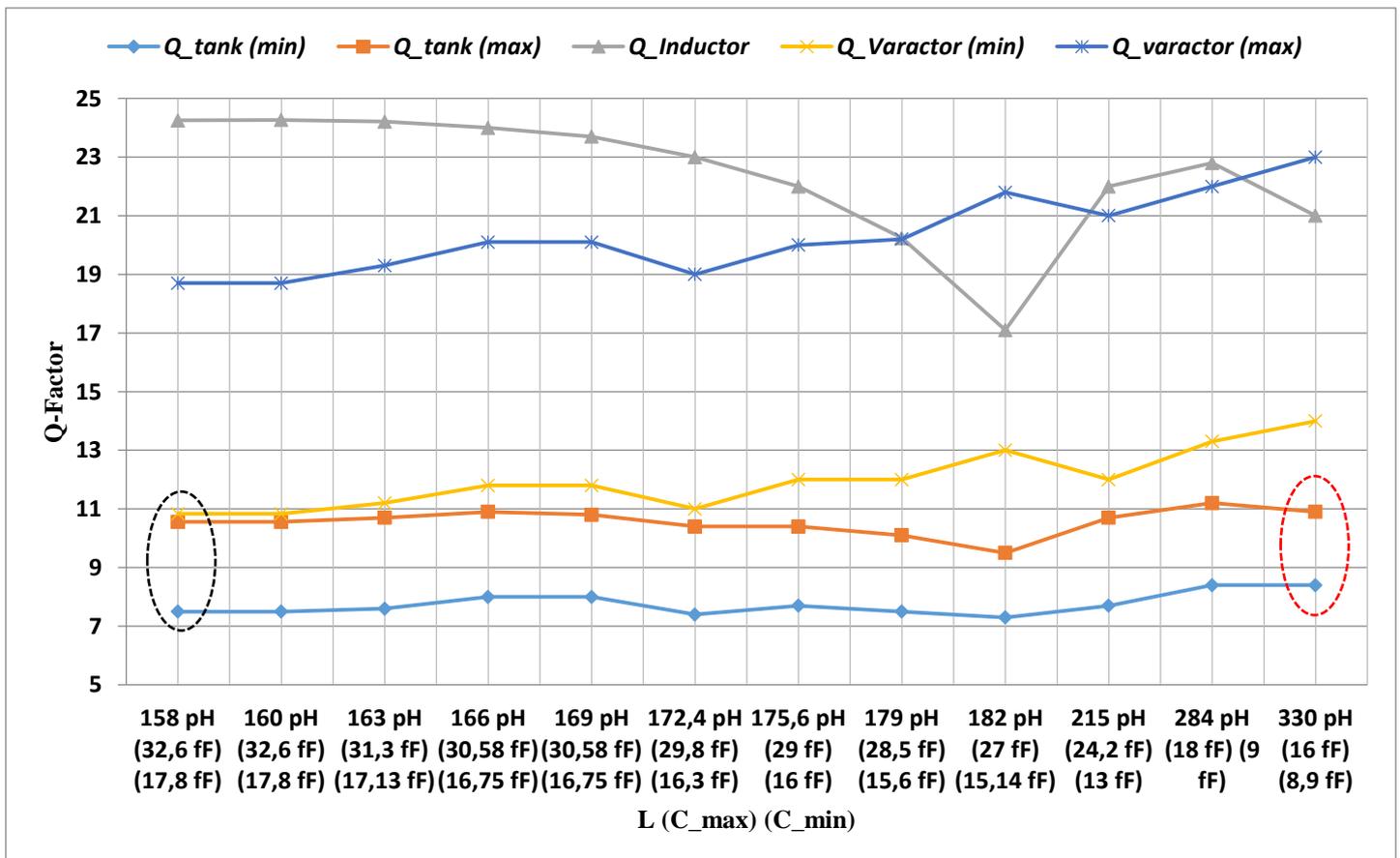


Figure 2.17:  $Q$ -factor vs. LC tank for 70 GHz

As shown in Figure 2.17, the  $Q$ -factor of inductor varies from 24 to 17 (approx.). For varactor the minimum  $Q$ -factor varies from 11 to 14 and maximum  $Q$ -factor varies from 19 to 23 (the most important parameter is minimum  $Q$ -factor of varactor). As expected, the low  $Q$ -factor of varactor dominates the LC tank  $Q$ -factor, as shown in Figure 2.17.

To resonate at a given frequency, several L-C combinations are possible. However, since the  $Q$ -factor of the LC tank is dominated by the varactor and remains quite constant it is recommended to use large inductor and small varactor, because the parallel resistor of a LC tank is given by  $R_p = Q/(\omega_0 C) = Q\omega_0 L$ . Such approach maximizes  $R_p$  and thus minimizes the size of CCP needed to cancel the losses.

Table 2.3 shows the comparison of three different set of LC tank i.e. first with big varactor & small inductor, second with intermediate values of varactor & inductor and third with small varactor & big inductor. The  $Q$ -factor of tank is quite the same in all three chosen combination. However, the other important parameter of concern is the equivalent  $R_p$  of the LC tank, since it will settle the value of parasitic capacitance to be added by cross-coupled pair, and hence impact the VCO frequency tuning range.

On comparing these three designs, least value of the parasitic capacitance is associated with design 3. So, while designing the conventional LC tank VCO (presented in Section 2.4.3) combination of smaller varactor and big inductor was considered.

Please note that the sets of LC tank given in Table 2.3 are only for demonstrating the effect of different LC combinations.

<i>Design</i>	<i>L (pH)</i>	<i>C (fF)</i>	<i>R<sub>p</sub> (Ω)</i>	<i>Q<sub>tank</sub></i>	<i>I<sub>o</sub> (mA)</i>	<i>W (μm)</i>	<i>R<sub>neg</sub> (Ω)</i>	<i>C<sub>par</sub> (fF)</i>
<b>1</b>	158	32.5 17.85	562 1.02k	8 11	12	16	202	18.7
<b>2</b>	237	21.57 12	924 1.66k	8.3 10.6	7	10	320	11.78
<b>3</b>	330	16 8.9	1.21k 2.02k	8.4 10.9	5.5	8	413	9.37

Table 2.3: Comparison of three different sets of LC tank

Apart from choosing a varactor with low loss, it is also important to notice interconnects between inductor and varactor, as it can add significant amount of losses to the LC tank. These losses vary for almost each metal layer and via interconnecting them. A brief study for resistance modelling of interconnecting metal layers is given in next Section 2.4.2.

#### 2.4.2 Resistive interconnect modelling

In BiCMOS 55 nm technology, the I/O pins in layout of inductor and varactor are on metal layer 8 and 4, respectively. It can also be viewed in Figure 2.4 and Figure 2.6, respectively. The estimation of losses is done by eq. (2.17).

$$R = \frac{l}{\sigma A} \quad (2.17)$$

where,  $l$  is the thickness of each metal layer,  $\sigma$  is the conductivity of respective metal layer and  $A$  is the area covered by metal layer. The thickness and conductivity of each metal layer (M) and via (V) connecting them are different, as given in Table 2.4. So, in accordance with the area of the stack utilized in layout (for making interconnection between two components), the equivalent resistance was computed for each metal layer and via. These resistance values of each metal layer and via are then added up to determine the total resistance.

<i>Layer</i>	$\sigma$ (MS)	<i>Thickness</i> ( $\mu\text{m}$ )
<i>M8</i>	46.3	3
<i>V7</i>	9.4	1.5
<i>M7</i>	38.1	0.9
<i>V6</i>	4.2	0.6
<i>M6</i>	38.1	0.9
<i>V5</i>	4.2	0.6
<i>M5</i>	26.8	0.2
<i>V4</i>	6.15	0.16
<i>M4</i>	26.8	0.2
<i>V3</i>	6.15	0.16
<i>M3</i>	26.8	0.2
<i>V2</i>	6.15	0.16
<i>M2</i>	26.8	0.2
<i>V1</i>	6.15	0.16
<i>M1</i>	25.5	0.16

Table 2.4: Conductivity and thickness of metal layers and vias

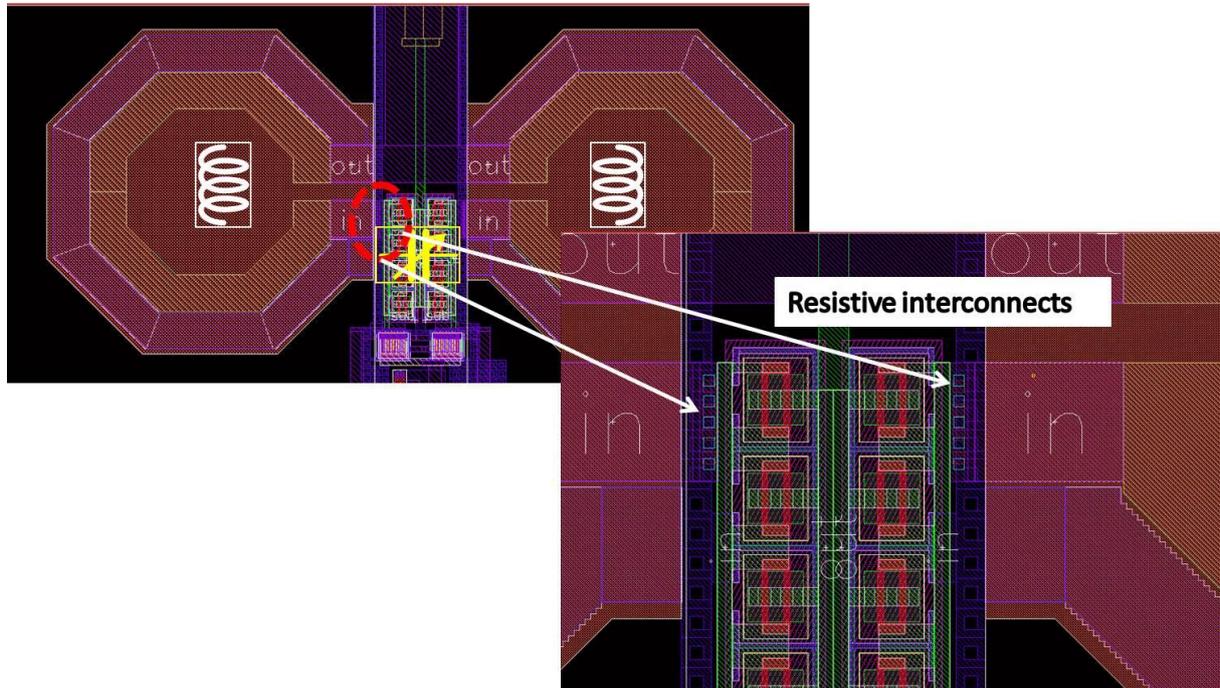


Figure 2.18: LC tank layout

For example, referring to the *LC*-tank layout shown in Figure 2.18 two interconnects are highlighted. As it is a symmetric structure, the resistance for one interconnection was computed and considered for other interconnects also. Depending on the area and utilized stack (in this case M4 to M8) the computed resistance for each metal layer and via is given in Table 2.5. Similarly the equivalent resistance to interconnect the varactor and cross-coupled pair shown in Figure 2.19 was computed ( $\approx 2.08 \Omega$ ). The schematic model of the *LC* tank and its equivalent parallel resistance ( $R_p$ ) with and without interconnect losses is as shown in Figure 2.20. As shown in Figure 2.20(b), due to the added resistive interconnects the equivalent  $R_p$  has been reduced by almost 50 %. This shows how the resistive interconnects could affect the  $Q$ -factor of the tank and by consequence  $FTR$  and power consumption.

<i>Metal (M) or via (V)</i>	<i>Equivalent Resistance (<math>\Omega</math>)</i>
<i>M4</i>	0.003
<i>V4</i>	0.05
<i>M5</i>	0.003
<i>V5</i>	0.2
<i>M6</i>	0.01
<i>V6</i>	0.2
<i>M7</i>	0.01
<i>V7</i>	0.25
<i>M8</i>	0.14
<i>R<sub>total</sub></i>	0.87

Table 2.5: Computed resistance for each metal layer shown in Figure 2.18

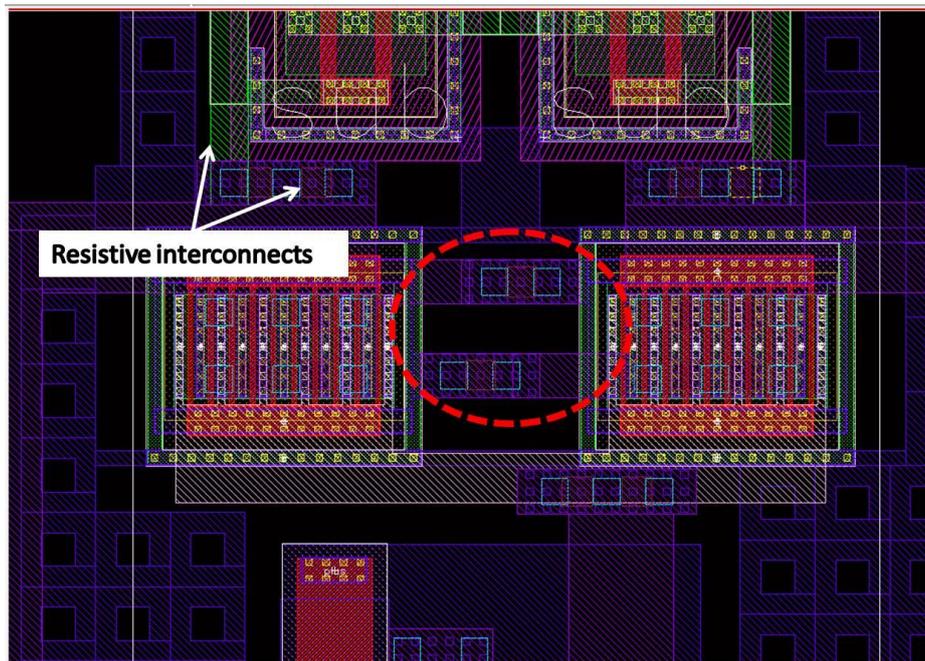
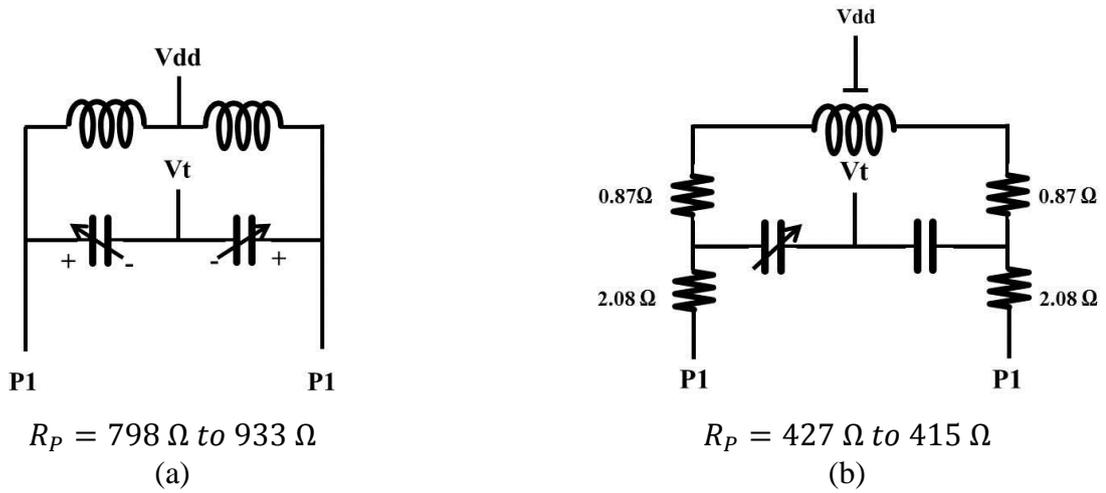


Figure 2.19: LC tank interconnection with cross-coupled pair

These hand calculated losses have been validated by RC extractions as well, i.e. on performing the RC extractions over the layouts shown in Figure 2.18 and Figure 2.19 the obtained value of equivalent  $R_p$  varies from 513  $\Omega$  to 540  $\Omega$ . On comparing the  $R_p$  computed in Figure 2.20(b) with RC extraction results, the value varies by 10 %.

As the hand calculated results, shown in Figure 2.20(b), demonstrates more pessimistic results as compared to RC extractions, so while designing the VCO hand calculations has been performed for determining the values of resistive interconnects. Hence, while designing the VCO these interconnections are considered as an accurate post layout simulations.

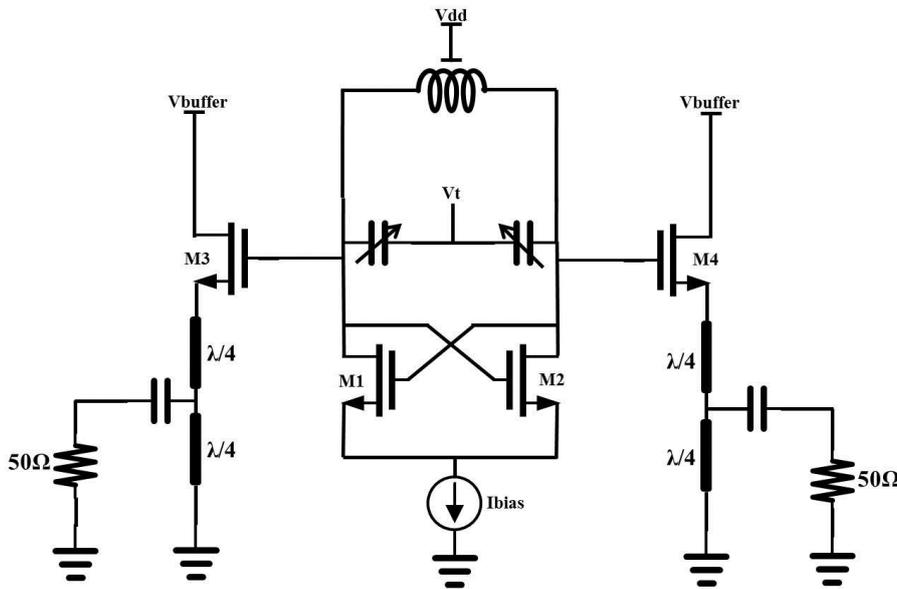


**\*RC extraction result:  $R_p = 513 \Omega \text{ to } 540 \Omega$**

**Figure 2.20: Loss estimation of LC tank (a) without resistive losses and (b) with added hand calculated resistive losses**

### 2.4.3 Design and simulated performance of conventional LC tank VCO

Finally, the schematic of the VCO is as shown in Figure 2.21. It has been finally designed at 83.5GHz (instead of 73.5GHz for comparison purpose with other presented work in this thesis). Due to the issue of mutual coupling between two single inductors and based on a state-of-the-art study [2]-[5] we utilized differential inductor in this design.



**Figure 2.21: Schematic of VCO**

In order to cover the targeted frequency band, i.e. 81 to 85 GHz, the varactor with 4 fF to 9 fF capacitances and inductor with 107 pH inductance were chosen. These values of LC were chosen after performing retro simulations including the parasitic capacitance added by CCP and output buffer circuits, as mentioned in the circuit design methodology (section 2.4.1). Also, as demonstrated in section 2.4.2 that resistive interconnects leads to increment in associated losses to LC tank. Figure 2.22 shows the interconnect value that has been computed and hence considered as well for determining the equivalent losses of LC tank. All the design parameters obtained after these steps are given in Table 2.6.

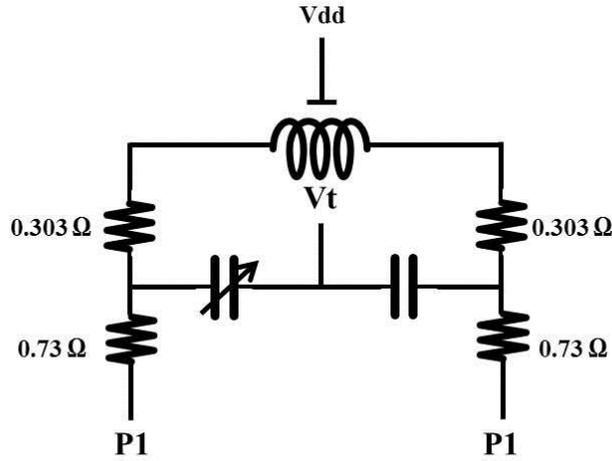


Figure 2.22: LC tank with resistive interconnects

	<i>Inductor</i>	<i>Varactor</i>
<i>Dimensions</i>	$W = 5.5 \mu\text{m}; D = 55 \mu\text{m}$	$W = 1.7 \mu\text{m}; Nf = 2; L = 0.2 \mu\text{m}$ $n\text{bcell} = 4$
<i>Equivalent value</i>	107 pH	$C_{\text{max}} = 8.94 \text{ fF}; C_{\text{min}} = 4.44 \text{ fF}$ $T.R. \approx 2$
<i>Quality factor</i>	23	$Q_{\text{min}} = 13.5$
<i>Tanks Q-factor</i>	8.5	
<i>Tanks Rp (Without resistive interconnects)</i>	872 Ω to 1096 Ω	
<i>Tanks Rp (With resistive interconnects)</i>	632 Ω to 692 Ω	
<i>Rnegative <math>\approx (Rp/3)</math></i>	210 Ω	
<i>Cross-coupled pair size</i>	$W = 17 \mu\text{m}; L = 0.06 \mu\text{m}; Nf = 17$	
<i>Id</i>	7 mA	
<i>Cpar (from CCP)</i>	19.7 fF	
<i>Cpar_buffer_total</i>	$7 \text{ fF} * 2 = 14 \text{ fF}$	

Table 2.6: Design parameters of LC-tank VCO

Also, the bias current can be varied from 3 mA to 12 mA by varying the bias voltage ( $V_b$ ) of current mirror from 0.78 V to 1.9 V, respectively. Hence, LCF is varied from 2 to 3.1 by varying  $V_b$  from 0.78 V to 1.9 V, respectively, as given in Table 2.7.

$V_b(\text{V})$	$I_d(\text{mA})$	$R_{\text{neg}}(\Omega)$	$C_{\text{par}}(\text{fF})$	$LCF = R_p / R_{\text{neg}}$
0.78	3	-306	18.96	2
1.2	7.36	-214	19.7	2.9
1.9	12.4	-205	20	3.1

Table 2.7: LCF variation with bias current

Table 2.8 the post layout simulation (PLS) of conventional LC-tank VCO. All the performances based on the S-parameter, transient and harmonic balance simulations are given in Table 2.8. The S-parameter simulation was performed to estimate approximately the oscillation frequency and tuning range. From S-parameter simulation the oscillation frequency is estimated by observing the point where  $Real(Z_{\text{port}})$  is negative and  $Imag(Z_{\text{port}})$  intersects zero.

With transient simulation the time response of the VCO was observed. In transient simulation we can only observe the output voltage of the VCO. So, the oscillation frequency and tuning range, given in Table 2.8(b), were hand calculated. Harmonic balance simulation was performed to observe the phase noise (PN) performance of the VCO. Hence, the slight variation between these three simulations is expected.

<i>Simulation</i>	$V_b(V)$	$V_t(V)$	$F_{osc}(GHz)$	$FTR (GHz)$
<i>S-parameter</i>	0.78	0	80.7	5.3
		2.4	86	
	1.2	0	79.9	5.1
		2.4	85	
	1.9	0	79.6	5.1
		2.4	84.7	

(a)

<i>Simulation</i>	$V_b(V)$	$V_t(V)$	$F_{osc}(GHz)$	$FTR (GHz/\%)$	$V_{out}(V)$
<i>Transient</i>	0.78	0	81.7	5.3/ 6.3	0.21
		2.4	87		0.22
	1.2	0	79.3	4.7/ 5.8	0.387
		2.4	84		0.4
	1.9	0	78.7	4.6/ 5.7	0.48
		2.4	83.3		0.49

(b)

<i>Simulation</i>	$V_b(V)$	$V_t(V)$	$F_{osc}(GHz)$	$FTR (GHz)$	$V_{out}(V)$	$PN (dBc/Hz)$	$FOM_T (dBc/Hz)$
<i>Harmonic balance</i>	0.78	0	81.7	5.3	0.21	-69.2 @ 1MHz	-159.7
		2.4	87		0.22	-89.4 @ 10 MHz	-159.9
	1.2	0	79.7	4.9	0.28	-72.7 @ 1MHz	-157.3
		2.4	84.6		0.29	-93.14 @ 10 MHz	-157.7
	1.9	0	78.7	4.6	0.48	-70.9 @ 1MHz	-152.5
		2.4	83.3		0.49	-93.7 @ 10 MHz	-155.3

(c)

Table 2.8: (a) S-parameter; (b) Transient and (c) Harmonic balance simulation

The bias voltage  $V_b$  of current source was modified to vary the LCF. With  $V_b = 0.78 V$ , the tuning range was slightly higher as compared to other bias conditions. This is due to fact that, with lower bias voltage, the associated value of  $R_{negative}$  is lower and hence the parasitic capacitance is lower too. But for  $V_b = 0.78 V$  the phase noise is higher because at this bias voltage the output power is low. By increasing this bias voltage to 1.2 V, the phase noise can be reduced, due to increment in output power, but at the expense of higher power consumption. As shown in Figure 2.13, with increase in power consumption the associated parasitic capacitance increases, hence leading to reduced  $FTR$ .

The figure of merit (FOM) of a VCO is defined as [6]:

$$FOM = L(\Delta f) - 20 \times \log \left( \frac{f_o}{\Delta f} \right) + 10 \times \log \left( \frac{P_{diss}}{1mW} \right) \quad (2.18)$$

where  $L(\Delta f)$  is the phase noise at the offset frequency  $\Delta f$  from oscillation frequency  $f_o$  in dBc/Hz.  $P_{diss}$  is the DC power consumption in mW. To take the frequency tuning range (FTR) into account, figure of merit with tuning range  $FOM_T$  is given in [7] as:

$$FOM_T = L(\Delta f) - 20 \times \log \left[ \left( \frac{f_o}{\Delta f} \right) \times \left( \frac{FTR}{10} \right) \right] + 10 \times \log \left( \frac{P_{diss}}{1mW} \right) \quad (2.19)$$

The resulting  $FOM_T$  is better for  $V_b = 0.78 V$ , as the tuning range is better and power consumption is lower, even though the phase noise is slightly higher.

The layout of SWO is shown in Figure 2.23. It occupies  $560 \mu m \times 747 \mu m$  including RF and DC pads.

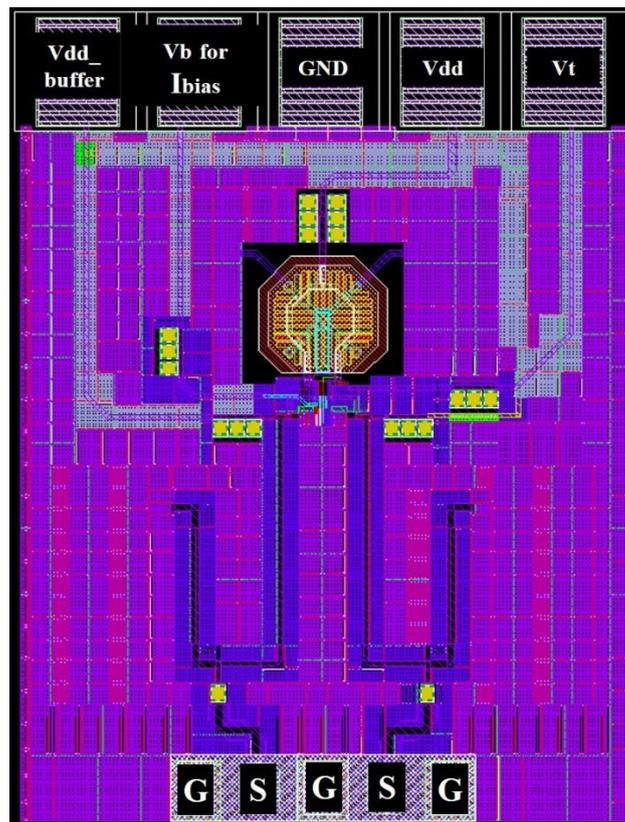


Figure 2.23: Layout of conventional LC-tank VCO (VCO 1)

## 2.5 Conclusion

In this chapter firstly, the VCO design methodology has been fixed/decided in order to achieve better frequency tuning range with low power consumption. Secondly, a brief study of “tank  $Q$ -factor versus various  $LC$  combinations” has been done for analyzing the circuit behavior. Although the tank  $Q$ -factor is dominated by low- $Q$  of varactor, but choosing a smaller varactor and bigger inductor leads to a better circuit performance in terms of FTR and power consumption. Also, an optimized output buffer for measurement has been proposed in this chapter, which allows having output impedance of  $50 \Omega$  but with reduced loading capacitance on VCO core. A brief study for determining the value of resistive interconnects has been done as well. This is also one of the crucial points to consider while designing the VCO as it contributes to increment in  $LC$ -tanks losses.

From the simulated performance of conventional  $LC$ -tank VCO, as expected the low- $Q$  conventional  $LC$ -tank VCO lead to many demerits. The very first demerit is the increased phase noise due to the lower  $Q$ -factor of  $LC$ -tank. Second demerit is reduced  $FTR$ , which is basically due to added parasitic from the cross-coupled pair. The reduction in  $FTR$  is related to the fact that lower  $Q$ -factor implies high series resistive losses hence bigger transconductance is needed to cancel these losses, leading to reduction in both  $F_{osc}$  and  $FTR$ . The third important demerit is increased power consumption. Hence obtained  $FOM_T$  is bad and not comparable to state-of-the-art.

So, the perspective followed in next chapters is to improve the  $Q$ -factor of  $LC$  tank in order to overcome the above mentioned shortcomings.

## 2.6 REFERENCES

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### 3. E-BAND VCO WITH S-CPS BASED DIFFERENTIAL INDUCTOR

As concluded in Chapter 2, there exist plenty of demerits of employing the inductors and varactors proposed by the design kit of a technology as conventional LC tank for mm-wave VCO design. This is particularly due to low- $Q$  of LC tank. In [1]-[11] various solutions to improve the  $Q$ -factor of VCO tank have been proposed.

Among the different solutions presented in the literature (chapter 1), improving the LC-tank  $Q$ -factor by different inductor orientation is interesting since it allows the use of varactors convenient for tuning the oscillation frequency of the VCO. The drawback of such approach is that the overall improvement of the tank  $Q$ -factor might be low since it is the varactor which is the most limiting component in term of  $Q$ -factor. However, recent studies on slow-wave transmission line [12] show very high  $Q$ -factor for such structures. Thanks to the improved- $Q$ , we can expect substantial improvement by synthesizing the tanks inductor with S-CPS lines. In this chapter we will explore different ways of improving the VCO performance. The results will be compared to the design presented in chapter 2 in order to understand the advantages and drawbacks of using a S-CPS based inductor.

The first step proposed in this chapter consists of using a differential slow-wave transmission line [12], i.e. S-CPS as inductor in the resonator instead of lumped inductor. To make a fair comparison with VCO design presented in Chapter 2, the same varactors have been employed and same inductance value has been synthesized with a slow-wave transmission line. The slow-wave concept has been briefly explained in Section 3.1, followed by design and optimization of differential slow-wave transmission line as inductor in Section 3.2. Finally the implementation of S-CPS inductor based VCO is presented in Section 3.3.

#### 3.1 Integrated slow-wave transmission lines

Transmission lines are the basic building blocks for typical mm-wave devices, e.g. matching network, power splitter, balun, coupler and filter. Due to the Back-End-Of-Line (BEOL) configuration (low dielectric and metallic layers thicknesses, and lossy silicon substrate proximity), low- $Q$  factors (lower than 20) are obtained for classical transmission lines such as microstrip and CPW, hence leading to lossy on-chip transmission line based passive components. So to overcome this problem of low- $Q$  factor the solution of slow-wave propagation was proposed in [13] and was implemented on an integrated technology in [14]. A brief explanation of slow-wave concept is given in Section 3.1.1

##### 3.1.1 Slow-wave Concept

A transmission line with reduced phase velocity is called as slow-wave transmission line. The phase velocity of a transmission line can be determined from eq. (3.1).

$$v_{\phi} = \frac{\omega}{\beta} = \frac{\omega \cdot \text{length}}{\theta} \quad (3.1)$$

For a fixed angular frequency ( $\omega$ ) and electrical length ( $\theta$ ), the reduced phase velocity leads to the reduction in the physical length of the transmission line.

Then, let us define now the essential factor of merit allowing defining the relevance of transmission lines. This factor of merit called  $Q$ -factor was proposed in [16]. It allows obtaining the insertion loss for a particular electrical length of the transmission line. The higher the quality factor, the most efficient the transmission lines for a given phase shift.

$$Q = \frac{\beta}{2\alpha} \quad (3.2)$$

Hence, from eq. (3.2) we can say that a higher  $Q$ -factor can be obtained either by reducing the losses or by increasing the phase constant, and therefore the dielectric constant. As per slow-wave concept given [17], a reduced phase velocity is obtained by periodically loading the CPW line with floating ribbons. Thus, allowing increase in phase constant while the attenuation remains the same. This solution consequently improves the quality factor without need of modifying the fabrication process.

In order to obtain the slow-wave structure, the methodology followed can be explained by considering the well-known Telegraphist model [18] of transmission lines, shown in Figure 3.1.  $R$  and  $L$  represent the per unit length series resistive losses in ( $\Omega/m$ ) and series inductance in ( $H/m$ ), respectively, while  $G$  and  $C$  represents per unit length conduction losses in ( $S/m$ ) and coupling capacitance between conductors in ( $F/m$ ), respectively.

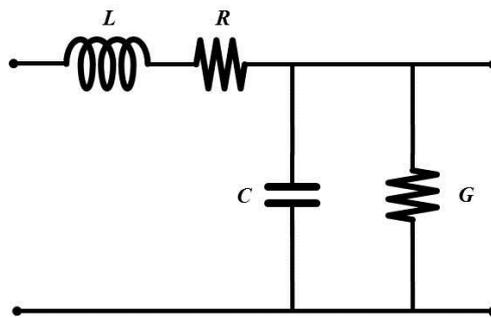


Figure 3.1: Telegraphist model - RLGC model of transmission line

The behavior of the transmission line can be determined from its electrical characteristics, i.e. characteristic impedance ( $Z_c$ ) and propagation constant ( $\gamma$ ), given for a lossless line in eq. (3.3) and eq. (3.4), respectively.

$$Z_c = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \approx \sqrt{\frac{L}{C}} \quad (3.3)$$

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta \quad (3.4)$$

From eq. (3.3) and eq. (3.4) the RLGC model parameters can be extracted using propagation parameters computed using EM simulators.

$$L = \frac{im(Z_c \cdot \gamma)}{\omega} \quad (3.5)$$

$$C = \frac{im(\gamma/Z_c)}{\omega} \quad (3.6)$$

$$R = \text{real}(Z_c \cdot \gamma) \quad (3.7)$$

$$G = \text{real}(\gamma/Z_c) \quad (3.8)$$

For a low-loss transmission line:

- The loss parameters i.e. R and G can be neglected, leading to simplified characteristic impedance
- The propagation constant can be determined in terms of real part, i.e. attenuation constant ( $\alpha$ ) which is generally expressed in (dB/m) and imaginary part, i.e. phase constant ( $\beta$ ) which is expressed in (rad/m). The phase velocity  $v_\phi$  is calculated by (3.9)

$$v_\phi = \frac{\omega}{\beta} = \frac{c_0}{\sqrt{\epsilon_{\text{reff}}}} = \frac{1}{\sqrt{L \cdot C}} \quad (3.9)$$

So low phase velocity i.e. slow-wave effect can be obtained by either increasing per unit lengths inductance or capacitance, refer eq. (3.9). The inductance can be increased by either reducing the width of the conductor, which will increase conductor loss or by increasing the gap between the signal and ground strip (refer Figure 3.2), which will increase the area of the chip. Also due to limitation in the technology, increment in inductance is not feasible beyond a limit. So the other solution, i.e. to increase capacitance, is employed to obtain a slow-wave transmission line.

In Section 3.1.2 two slow-wave transmission lines topologies will be proposed, and the choice of S-CPS (for VCO design) will be justified.

### 3.1.2 Need of S-CPS in VCO design

Among several transmission line topologies [19], slow-wave transmission lines are well suited for mm-wave, in order to achieve low attenuation and hence improved  $Q$ -factor [12]-[17]. Hence, with slow-wave concept two commonly used transmission lines are considered in standard silicon microelectronics technology (such as BiCMOS 55 nm technology) S-CPW and S-CPS, as shown in Figure 3.2.

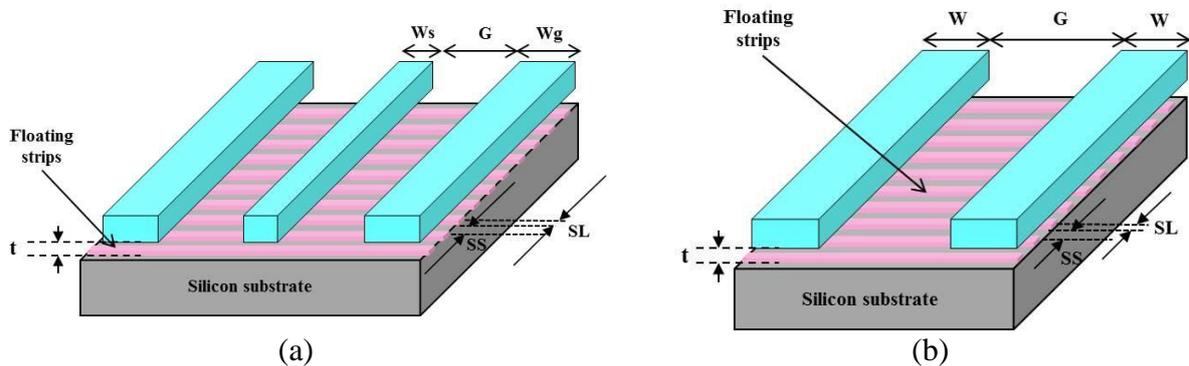


Figure 3.2: 3-D view of (a) S-CPW (slow-wave coplanar waveguide) and (b) S-CPS (slow-wave coplanar stripline)

As shown in Figure 3.2(a), a S-CPW consists of a conducting (signal) strip of width ( $W_s$ ) with a pair of ground conductors of width ( $W_g$ ) on Top Metal (M), say M8, one to either side of the signal strip separated by a gap ( $G$ ) and backed by an array of thinner floating strips on a lower metal layer of width ( $SL$ ) separated by spacing ( $SS$ ). Concerning the S-CPS, two signal strips are positioned on Top Metal (M), say M8, of width ( $W$ ), separated by gap ( $G$ )

and similar to S-CPW, backed by an array of thinner strips on a lower metal layer of width ( $SL$ ) separated by spacing ( $SS$ ), shown in Figure 3.2(b).

The difference between S-CPW and S-CPS is primarily that S-CPW structure consists of a single conducting strip with two grounds, while S-CPS has two signal strips leading to a differential transmission line. Hence the chip area occupied by S-CPS is less than half as compared to S-CPW, for the same inductance value. As the VCO design topology is differential, the needed distributed inductor is differential as well. Hence, unlike S-CPS with S-CPW we need to merge two S-CPWs [6], [7] to design a differential inductor.

Thus, utilizing differential S-CPW needs a larger chip area with longer interconnects to varactors and nMOS cross-coupled pair. With S-CPS these added interconnects will be smaller and hence for the VCO designed in this thesis, S-CPS have been employed. The electrical characteristics of S-CPS are given in Section 3.2, along with its equivalent  $RLRC$  model.

## 3.2 Structure of S-CPS based differential inductor

### 3.2.1 Electrical characteristics of S-CPS in BiCMOS 55 nm Technology

The use of a slow-wave approach allows shrinking the resonator size by increasing the effective dielectric constant which finally enhances the resonator  $Q$ -factor [14]-[15]. In [14] and [15] a slow-wave coplanar waveguide (S-CPW) was considered whereas, we consider the slow-wave coplanar stripline (S-CPS), shown in Figure 3.2(b). For the VCO design presented in this chapter, S-CPS with the following parameters was utilized: two metallic strips on Metal 8- Metal 7 and fingers on Metal 5. Several other combinations of Metal Layers were simulated also, i.e. (i) Metallic strips on Metal 8- Metal 7 and fingers on Metal 6: This stack offered high eddy current losses (ii) Metallic strips on Metal 8- Metal 7 and fingers on Metal 4: Low losses but reduced slow-wave effect as well. Hence, the chosen stack was Metal 8- Metal 7 and fingers on Metal 5, with a tradeoff between losses and slow-wave effect.

Figure 3.3 shows the electrical characteristics of the chosen S-CPS line, i.e. per unit length inductance ( $L$ ),  $Q$ -factor, characteristic impedance ( $Z_C$ ), effective permittivity ( $\epsilon_{eff}$ ) and attenuation constant ( $\alpha$ ) at 83.5 GHz (as the targeted  $F_{osc}$  for VCO is from 81 to 86 GHz), carried out with HFSS (3D-EM simulator). Various differential inductors have been simulated using HFSS with metallic strips width ( $W$ ) ranging from 10  $\mu\text{m}$  to 50  $\mu\text{m}$ , and gap ( $G$ ) ranging from 10  $\mu\text{m}$  to 30  $\mu\text{m}$ . Using ABCD parameters [19], the electrical characteristics ( $Z_C$ ,  $\epsilon_{eff}$ ,  $L$ ,  $Q$  and  $\alpha$ ) of S-CPS have been computed.

As we want to synthesize a high- $Q$  inductor with S-CPS, so focusing on the inductive characteristics in Figure 3.3(a) we see that per unit length inductance ( $L$ ) increases with  $G$  and decrease with  $W$ . And the  $Q$ -factor increases with both  $G$  and  $W$ . Hence, both  $Q$ -factor and inductance ( $L$ ) increases with  $G$ . Nevertheless, it is impractical to make  $G$  very large since the occupied area would be prohibitive. Also, the connection of the S-CPS based inductor to the rest of the circuit would add significant capacitive and parasitic effects. Although all the electrical characteristics are in synchronization with each other, but if we compare  $Z_C$  and  $\alpha$  in Figure 3.3(a) and Figure 3.3(e), respectively, we can say that for a higher  $Z_C$ ,  $\alpha$  is lower. This analysis can be explained by Matthaei model [21], even if this

model is rigorously valid for quarter- and half-wavelength only. This analysis has been explained in Section 3.2.2 and detailed design parameters of VCO are given in Section 3.3.

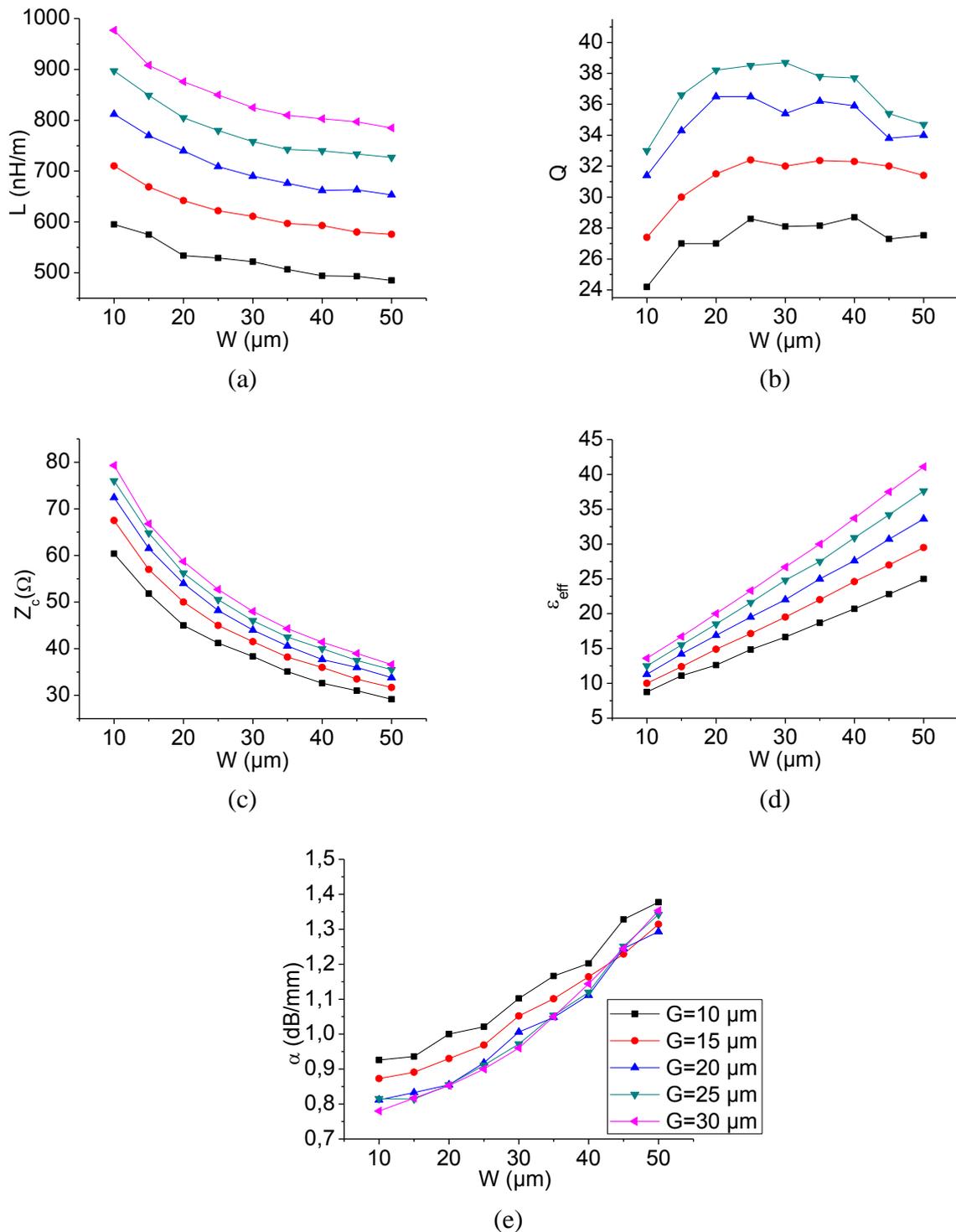


Figure 3.3: (a) Characteristic Impedance; (b) Effective permittivity; (c) Equivalent inductance (d)  $Q$ -factor, and (e) Attenuation constant of S-CPS

Please note that the Matthaei model [21] explained in next section 3.2.2 is only to justify the selection of chosen dimension of S-CPS and not the only criteria.

### 3.2.2 Effect of Characteristic Impedance of transmission line: Matthaei Model

A transmission line terminated either by an open-circuit or short-circuit is often used as a resonator. Figure 3.4 and Figure 3.5 show four resonators of this type along with their lumped-constant equivalent circuits. For both kinds of resonators in each case, their lumped constant equivalent circuits are dual of one another.

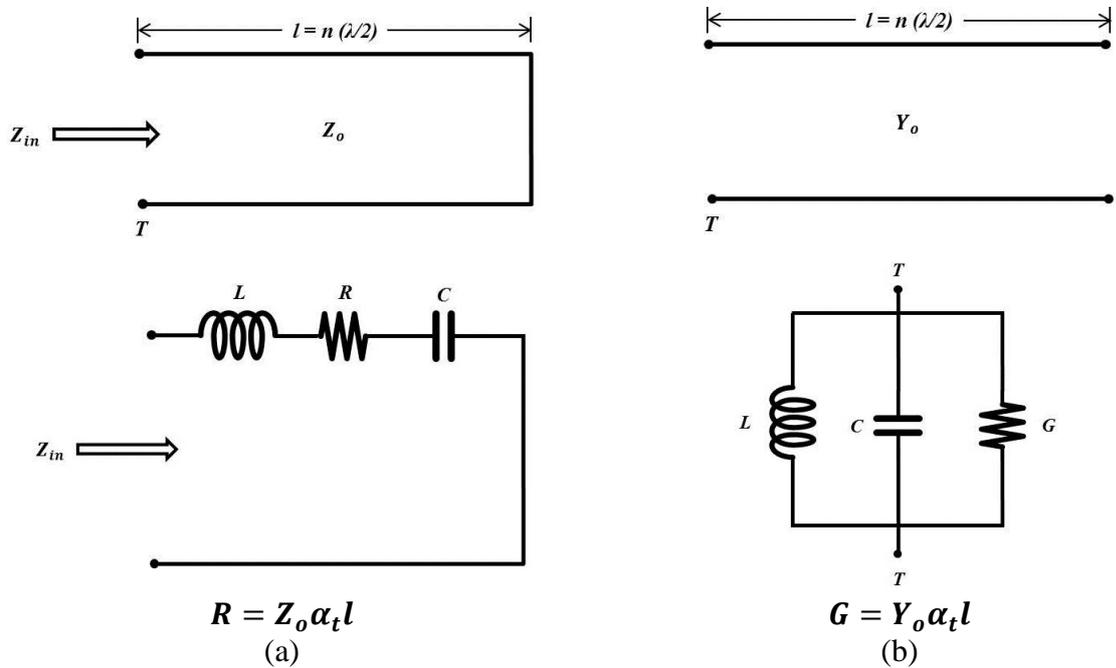


Figure 3.4: Transmission line resonators of one-half guide wavelength [21]

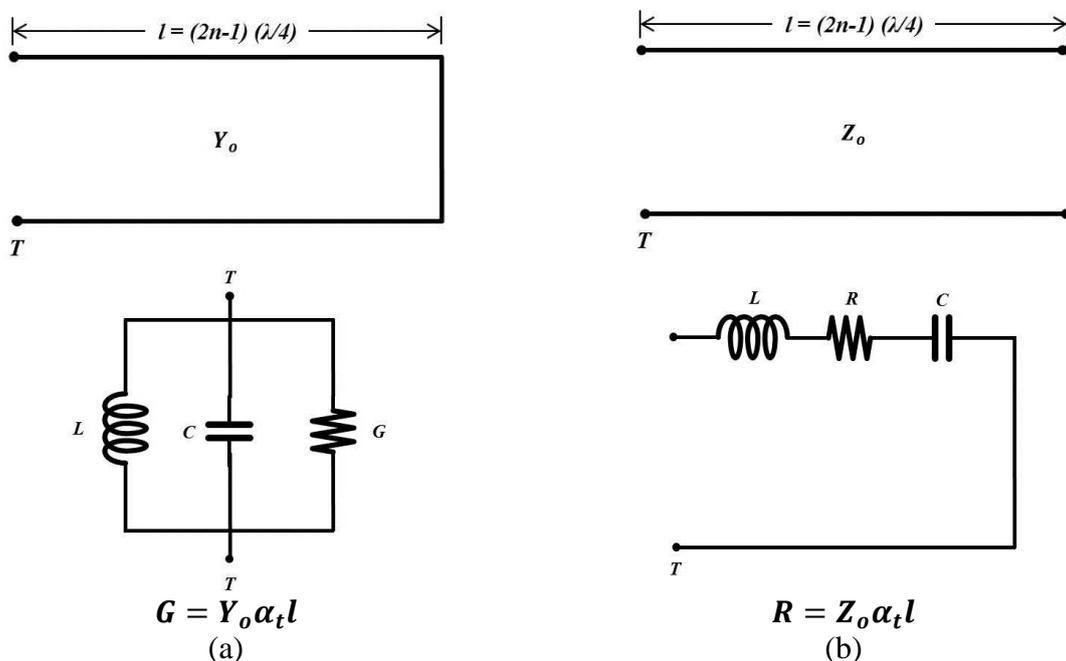


Figure 3.5: Transmission line resonators of one-quarter guide wavelength [21]

(where,  $\alpha_t$  is the attenuation constant of the transmission line,  $Z_o$  is characteristic impedance,  $Y_o$  is characteristic admittance,  $\lambda$  is the guide wavelength at resonant frequency and  $l$  is the physical length of resonator)

For designing VCOs, the short circuited quarter wavelength transmission line was employed, as the open circuited transmission line resonators need more chip area. This is due to nMOS cross-coupled topology of the VCO, as it needs to differential biasing.

If we see equation for each type of resonator in Figure 3.4 and Figure 3.5, the relation between characteristic impedance and resistive losses can be determined. For example Figure 3.4(a) shows a half wavelength short-circuited resonator and its equivalent lumped model, i.e. series combination of  $RLC$ . Here with higher  $Z_C$ , higher series resistive losses are expected. This observation is similar for quarter wavelength open-circuited resonator, shown in Figure 3.5(b).

But on the contrary, resonators shown in Figure 3.4(b) and Figure 3.5(a) are expected to have lower resistive losses with higher  $Z_C$ . So, in order to validate Matthaei's model we chose three different cases from the previous simulation of S-CPS line, as shown in Figure 3.6.

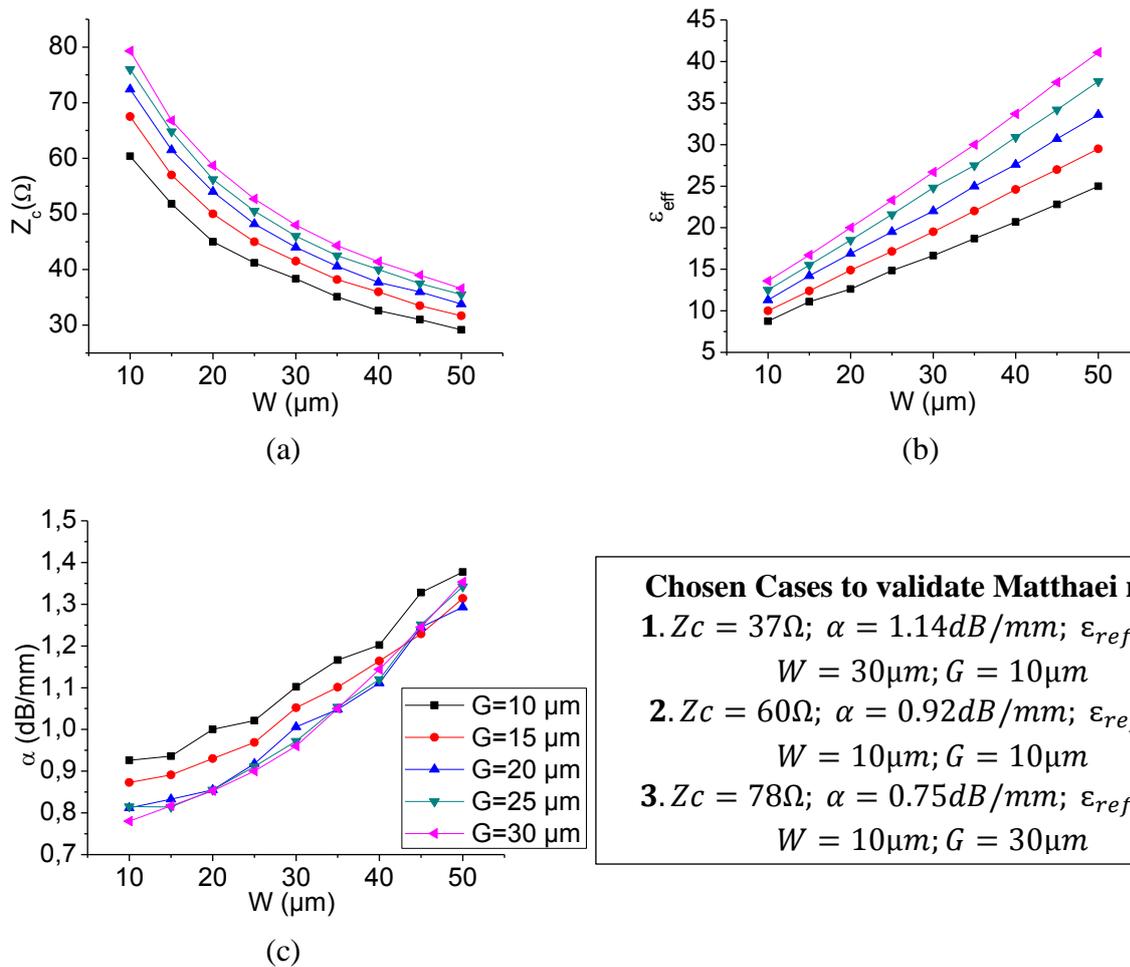


Figure 3.6: Chosen cases for validating Matthaei model

As shown in Figure 3.6 we chose three different impedances. By comparing these three cases of quarter wavelength S-CPS (see Table 3.1), as expected, by increasing  $Z_C$ ,  $G$  reduces, hence  $R_P$  increases. This  $R_P$  is directly proportional to  $Q$ -factor, leading to a smaller cross-coupled pair design, hence reduced parasitic and power consumption (refer to Section 2.1, Chapter 2). Thus, for a quarter wavelength transmission line the higher characteristic impedance the better resonator.

Similarly, these three cases were compared for half wavelength S-CPS also in Table 3.2. In this case if the  $Z_C$  of the line is increased, the equivalent  $R_S$  of the line also increases leading

to increment in losses, hence the  $Q$ -factor reduces. So, in case of a half wavelength transmission line lower impedance will result in a better resonator.

$Z_C$ ( $\Omega$ )	$\alpha$ (dB/mm)	$l = \lambda/4$ ( $\mu\text{m}$ )*	$G$ ( $\mu\text{S}$ )	$R_P = 1/G$ (k $\Omega$ )
37,25	1,1427	276	922	1.08
60,2	0,922	357,6	640	1.56
<b>78</b>	<b>0,754</b>	<b>297,6</b>	<b>326,5</b>	<b>3.06</b>

Table 3.1: Parameters for quarter wavelength S-CPS (\* Calculated done for 70 GHz)

$Z_C$ ( $\Omega$ )	$\alpha$ (dB/mm)	$l = \lambda/2$ ( $\mu\text{m}$ )*	$R_S$ ( $\Omega$ )
<b>37,25</b>	<b>1,22</b>	<b>552</b>	<b>2.63</b>
60,2	0,85	714	4.544
78	0,85	594	4.08

Table 3.2: Parameters for half wavelength S-CPS (\* Calculated done for 70 GHz)

As mentioned above that the quarter wavelength resonator has been utilized for VCO design, so S-CPS with  $Z_C \approx 78\Omega$  was chosen. The simulated  $Q$ -factor of the chosen dimension of S-CPS is about 33, refer Figure 3.3. Let us notice that due to the added capacitance by varactors and cross-coupled pair, the chosen electrical length of S-CPS is shorter than quarter wavelength when used as a resonator. The detailed explanation is given in Section 3.3 with all the design parameters of VCO.

### 3.2.3 Equivalent RLRC model of S-CPS

The above mentioned electrical characteristics of S-CPS are determined by HFSS simulations. Generally, from HFSS simulations the S-parameters are converted to ABCD parameters in MATLAB in order to determine the electrical characteristics of S-CPS. The flow diagram shown in Figure 3.7 represents the same procedure. But the first step of this procedure generally takes immense amount of time due to electromagnetic simulation in full-wave 3D-EM tool. The later steps are considerably faster as they are performed on MATLAB with set of interconversion equations between S and ABCD parameters.

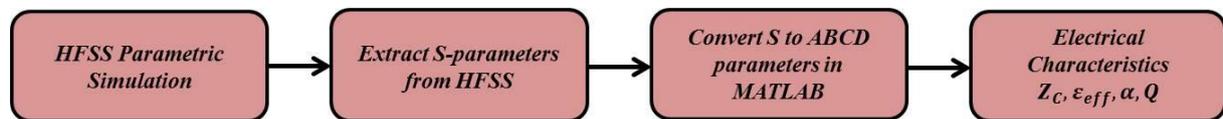


Figure 3.7: Flow diagram of conventional procedure to determine electrical characteristics of S-CPS

Following the above mentioned procedure leads to long development time, due to the uncertainty of getting optimum design. For the same purpose, an accurate electrical model based on geometric parameters of S-CPW with very fast circuit simulations has been presented in [22]. An accurate RLRC model has been proposed in [22] based on assumption of Quasi-TEM propagation mode, with wide band accuracy and without need of fitting factors. This proposed model has been developed by treating electric and magnetic field separately to process apart both inductor and capacitor.

The study presented in [22] is mainly made over the electric field. Indeed, the magnetic field is not perturbed by the presence of the floating shielding, which means that the equivalent inductance of slow-wave CPW is the same as the conventional CPW one. The inductance was therefore calculated with the formulation developed in [23]. In [22] S-CPW was considered, whereas in this thesis the model for S-CPS has been utilized based on same approach, as shown in Figure 3.8.

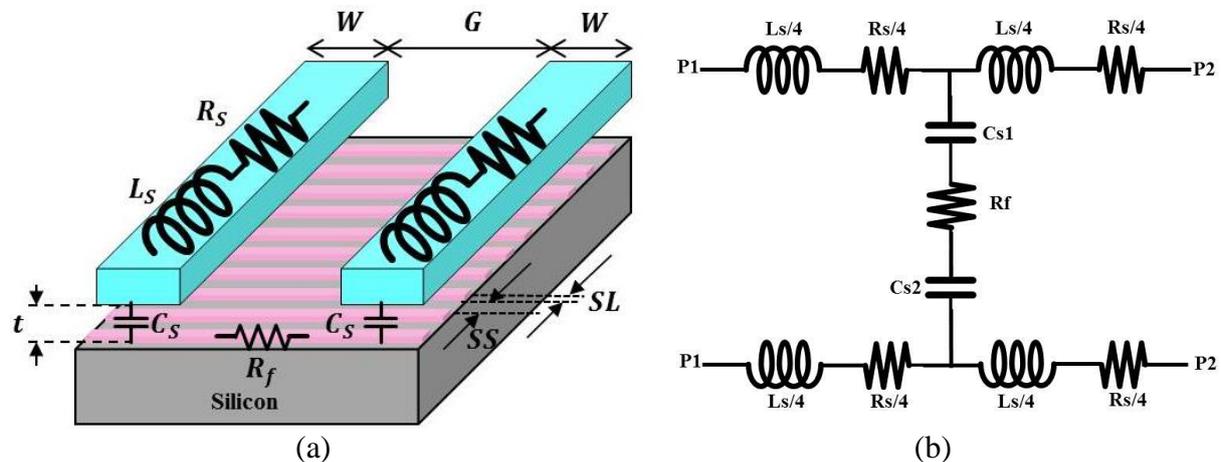


Figure 3.8: (a) A 3D schematic view of the S-CPS and (b) Symmetric electrical model

### 3.3 VCO design with S-CPS synthesized as inductor

#### 3.3.1 Loss Estimation and nMOS Cross-Coupled Pair design

Before starting to design the VCO based on S-CPS synthesized inductor, it is important to note that to make a fair comparison with VCO design presented in Chapter 2, i.e. lumped  $LC$ -tank VCO, the varactors with same value ( $4\text{ fF}$  to  $9\text{ fF}$ ) has been employed in the VCO design presented in this chapter and same inductance ( $\approx 107\text{ pH}$ ) value has been synthesized with a slow-wave transmission line.

For synthesizing the S-CPS based inductor, the dimension of S-CPS has been chosen based on the approach presented in Section 3.2.2 [21], i.e. the S-CPS with high impedance line has been chosen as it has lower losses, refer Table 3.1. So the S-CPS with width ( $W$ ) of  $10\text{ }\mu\text{m}$  and gap ( $G$ ) of  $30\text{ }\mu\text{m}$  has been utilized for synthesizing the inductor. To start, in order to synthesize the  $107\text{ pH}$  inductance, a length of  $120\text{ }\mu\text{m}$  was chosen for the S-CPS. Let us notice that unlike Section 3.2.2, this chosen length of S-CPS for VCO design is much smaller than quarter wavelength, by once connected to the varactor added capacitance and parasitic from cross-coupled pair & output buffer circuits, the equivalent electrical length of resonator is  $90^\circ$  at the oscillation frequency.

Based on the one-port method approach (presented in Chapter 2, Section 2.2.3), the equivalent  $R_p$  of the resonator is determined. To cancel these losses of tank cross-coupled pair of width  $8.2\text{ }\mu\text{m}$  were chosen.

Due to the added interconnects (shown in Figure 3.9) between “S-CPS & varactor” and between “varactor & cross-coupled pair”, the equivalent losses were slightly higher. So the size of cross-coupled pair was increased to  $9.8\text{ }\mu\text{m}$ . This arrangement led to reduced oscillation frequency, so the final chosen length of S-CPS was reduced to  $114\text{ }\mu\text{m}$ . Width of

cross-coupled pair was increased to  $11 \mu\text{m}$  to compensate the losses. All the design parameters are given in Table 3.3.

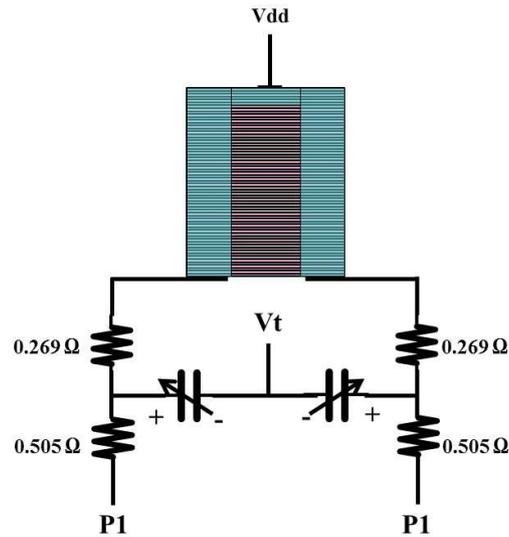


Figure 3.9: Tank circuit of VCO2 with interconnects

	<i>Inductor (S-CPS)</i>	<i>Varactor</i>
<i>Dimensions</i>	$W = 10 \mu\text{m}; G = 30 \mu\text{m};$ $l = 114 \mu\text{m}$	$W = 1.7 \mu\text{m}; Nf = 2;$ $L = 0.2 \mu\text{m}$ $nbcell = 4$
<i>Equivalent value</i>	108 pH	$C_{max} = 8.94 \text{ fF};$ $C_{min} = 4.44 \text{ fF}; T.R. \approx 2$
<i>Quality factor</i>	$\approx 35$	$Q_{min} = 13.5$
<i>Tanks Q-factor</i>	9.7	
<i>Tanks Rp (Without resistive interconnects)</i>	1186 $\Omega$ to 1654 $\Omega$	
<i>Tanks Rp (With resistive interconnects)</i>	967 $\Omega$ to 1179 $\Omega$	
<i>Rnegative <math>\approx (Rp/3)</math></i>	322 $\Omega$	
<i>Cross-coupled pair size</i>	$W = 11 \mu\text{m}; L = 0.06 \mu\text{m}; Nf = 11$	
<i>Id</i>	6 mA	
<i>Cpar (from CCP)</i>	13 fF	
<i>Cpar_buffer_total</i>	$7 \text{ fF} * 2 = 14 \text{ fF}$	

Table 3.3: Design parameters of VCO design with S-CPS based differential inductor

The current from current mirror can be varied from 1.9 mA to 6 mA by varying the bias voltage ( $V_b$ ) of current mirror from 0.7 V to 1.2 V, respectively. Hence, LCF can be varied from 2 to 3 by adjusting  $V_b$  from 0.7 V to 1.2 V, respectively, as given in Table 3.4.

$V_b(V)$	$I_d(mA)$	$R_{neg}(\Omega)$	$C_{par}(fF)$	$LCF = R_p / R_{neg}$
0.7	1.9	-466	12.3	2
1.2	6	-321	12.9	3

Table 3.4: LCF variation with bias current

### 3.3.2 Simulated performance

In Table 3.5, the post layout simulation (PLS) of VCO2 is given. In Table 3.5 the performance based on S-parameter, transient and harmonic balance simulations are given. The estimated oscillation frequency and tuning range from S-parameter simulation are given in Table 3.5(a), by observing the point where  $Real(Z_{port})$  is negative and  $Imag(Z_{port})$  intersects zero.

The time response of VCO was observed with transient simulation. As in transient simulation only output voltage of oscillator can be observed so, the oscillation frequency and tuning range, given in Table 3.5(b), is hand calculated.

The phase noise (PN) performance of the VCO is obtained by harmonic balance simulation given in Table 3.5(c). In Table 3.5(c), both worst and best possible PN is presented, i.e. from -83 dBc/Hz to -89.2 dBc/Hz at 1MHz offset and -104.4 dBc/Hz to -113.3 at 10 MHz offset, respectively.

As all the three simulations i.e. S-parameter, transient and harmonic balance are performed for different purpose, hence the slight variation between these three simulations is expected, i.e. FTR is a bit higher in S-parameter and harmonic balance simulation as compared to transient simulation. Similarly, there is slight variation in the output power obtained by transient and harmonic balance simulation.

Simulation	$V_b(V)$	$V_t(V)$	$F_{osc}(GHz)$	FTR (GHz)
S-parameter	0.7	0	81.9	5.7
		2.4	87.6	
	1.2	0	81.2	5.6
		2.4	86.8	

(a)

Simulation	$V_b(V)$	$V_t(V)$	$F_{osc}(GHz)$	FTR (GHz/%)	$V_{out}(V)$
Transient	0.7	0	83.3	4.9/ 5.7	0.15
		2.4	88.2		0.16
	1.2	0	80.8	5.3/ 6.4	0.36
		2.4	86.1		0.4

(b)

Simulation	$V_b(V)$	$V_t(V)$	$F_{osc}(GHz)$	FTR (GHz)	$V_{out}(V)$	PN (dBc/Hz)	$FOM_T$ (dBc/Hz)
Harmonic balance	0.7	0	82.6	5.8	0.13	-78.6 to -87 @ 1MHz	-178.7
		2.4	88.4		0.15	-99.5 to -109 @ 10MHz	-180.3
	1.2	0	81	5.3	0.31	-83 to -99.2 @ 1MHz	-175.1
		2.4	86.3		0.33	-104 to -113.3 @ 10MHz	-179.2

(c)

Table 3.5: (a) S-parameter; (b) Transient and (c) Harmonic balance simulation

As discussed in chapter 2, the bias voltage  $V_b$  was varied to adjust the current and hence to modify the LCF. With  $V_b = 0.7 V$ , the tuning range was slightly higher as compared to other bias condition. This is due to the fact that with lower bias voltage i.e.  $V_b = 0.7 V$ , the associated value of  $R_{neg}$  is lower and hence the parasitic capacitance is lower too. But for  $V_b = 0.7 V$  the phase noise is higher as the output power is low. By increasing the bias

voltage, i.e. to  $V_b = 1.2 V$ , the phase noise can be reduced, due to increment in output power, but at the expense of higher power consumption. It is to be noted that increasing the power consumption leads to an increased parasitic capacitance (as mentioned in Section 2.1.3), hence the obtained  $FTR$  is reduced.

For this VCO the resulting  $FOM_T$  is almost the same for both bias states, i.e.  $V_b = 0.7$  and  $1.2 V$ . It is due to the fact that in one case (i.e.  $V_b = 0.7 V$ )  $FTR$  was higher while in the other case (i.e.  $V_b = 1.2 V$ ) phase noise was lower, hence leading to almost same  $FOM_T$ . The best possible  $FOM_T$  obtained for this VCO design is  $-175.1$  dBc/Hz at 1MHz offset and  $-179.2$  at 10 MHz offset.

On comparing the simulated performance of the VCO topology presented in this chapter (say  $VCO2$ ) with VCO design presented in Chapter 1 (say  $VCO1$ ), we can say that  $VCO2$  has better performance primarily in terms of  $PN$ , power consumption and secondly in terms of frequency tuning range. The  $PN$  of  $VCO2$  has improved by 10 to 15 dB. Due to improved  $Q$ -factor the power consumption is lower in  $VCO2$  and output power is slightly better as well. But the tuning range increment was 0.5 GHz only. This is due to fact that S-CPS also adds some capacitance ( $\approx 7.3 fF$ ) due to slow-wave effect, hence leading to a negligible amount of increment in  $FTR$ . Hence in total due to use of high- $Q$ ,  $FOM_T$  is improved by 19 dBc/Hz. A detailed comparison between simulated performance of  $VCO1$  and  $VCO2$  is given in Table 3.6.

<i>Simulated performance parameters</i>	<i>VCO1: With lumped inductor</i>	<i>VCO2: With S-CPS synthesized inductor</i>
$F_o$ (GHz)	82.1	83.6
$TR$ (GHz)	4.9	5.3
$FTR$ (%)	6	6.3
$P_{out}$ (dBm)	-0.7	0.4
$P_{dc,core}$ (mW)	8.4	7.2
$PN$ at 10MHz offset (dBc/Hz)	-93.1	-113.3
$FOM_T$ (dBc/Hz)	-158	-179.2

Table 3.6: Simulated performance of  $VCO1$  and  $VCO2$

### 3.4 Comparison with state-of-the-art

In Table 3.7 the performance of VCO design with S-CPS synthesized inductor has been compared with state-of-the-art. First, let us notice that  $VCO2$  presents the lowest power consumption inducing at the same time a low  $FTR$  comparable only to [4], [5]. Second, even though the power consumption is minimal, the output power is the highest one compared to all previous designs. The  $PN$  performance of  $VCO2$  has been improved as well compared to  $VCO1$  due to better  $Q$ -factor and output power. Hence, the overall performance in terms of  $FOM_T$  has been improved as compared to the design presented in Chapter 2. But the improvement in  $FTR$  is needed in order to achieve higher  $FOM_T$ .

The layout of SWO is shown in Figure 3.10. It occupies  $560 \mu m \times 700 \mu m$  including RF and DC pads.

VCOs	$P_{dc\_core}$ (mW)	FTR (%)	$P_{out}$ (dBm)	$F_o$ (GHz)	PN (dBc/Hz) (Best PN)	$FOM_T$ (dBc/Hz)
[4]	15.81	6.3	---	76.5	-109 @ 10MHz	-170.6
[5]	14.3	6.3	-4.5	76.5	-109 @ 10 MHz	-171.1
[5] post fabrication	14.3	15.8	-4.5	76.5	-108.4 @ 10MHz	-178.5
[8]	8.4 to 10.8	41	---	73.8	-104.6	-184.2
[24]	15	17	-4.9	56	-89.8 @ 1MHz (worst) -99.4 @ 1MHz (best)	-177.4 -186.8
[25]	27	20	-4	40	-96 @ 1MHz (worst) -100.2 @ 1MHz (best)	-179.2 -183.9
[26]	33	14	-0.5	81.5	-97.3 @ 1MHz (best)	-182.6
<b>This work VCO2</b>	7.2	6.3	0.55	83	-89.2 @ 1MHz -113.3 @ 10MHz	-175 -179.2

Table 3.7: State-of-the-art comparison

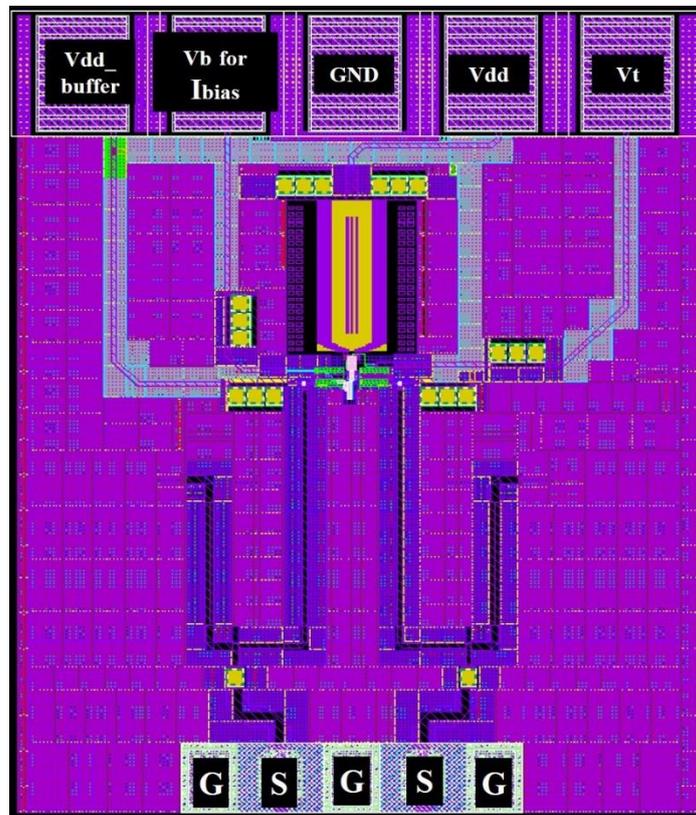


Figure 3.10: Layout of VCO with S-CPS synthesized inductor

### 3.5 Conclusion

Thanks to the high- $Q$  S-CPS, its utilization in VCO design lead to several advantages. First of all is reduced power consumption. This is due to the fact that lower losses are associated to the resonator hence leading to need of smaller cross-coupled pair with reduces current. Due to higher  $Q$ -factor, the output power is high and hence it leads to have improved  $PN$ .

Besides the fact that performance was improved in terms of power consumption and  $PN$ , the  $FTR$  is still lower and not comparable with state-of-the-art and hence need to be improved.

In next chapter this perspective of lower  $FTR$  has been considered as a part of study/ analysis. And a new resonator topology with concept of loaded line phase shifter has been proposed to overcome this issue of low  $FTR$ .

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## 4. E-BAND VCO WITH UNSYMMETRIC S-CPS BASED PHASE SHIFTER AS RESONATOR

On referring the VCO performance presented in Chapter 3, we can clearly observe that replacing a lumped inductor having low  $Q$ -factor with a distributed inductor having high  $Q$ -factor leads to very slight increment in the overall  $Q$ -factor of the resonator. This slight improvement leads to little improvement in  $FTR$  and  $PN$ . Hence the idea proposed in this chapter is to improve the  $Q$ -factor of the resonator by employing a loaded line phase shifter based on S-CPS transmission lines instead of a tunable resonator constituted of S-CPS inductor with a lumped varactor.

There exists several phase shifter topologies in literature [1] – [9], i.e. reflection type, loaded line and switched line. Preliminary studies have shown the good performances of S-CPW based phase shifter [5] – [7]. However, to be used in a VCO, the phase shifter must be differential. So, in this chapter S-CPS based phase shifter is proposed to be used as quarter-wavelength ( $\lambda/4$ ) resonator in order to design Standing Wave Oscillator (SWO). The proposed phase shifter in this chapter is based on the concept of new tunable S-CPS, i.e. the S-CPS is periodically loaded by varactors, leading to the concept of tunable  $\lambda/4$  resonator.

Firstly, a state-of-the-art review is done for various loaded line phase shifters in section 4.1.1 and then some phase shifter topologies are proposed in section 4.1.2. In section 4.2, the design methodology for phase shifters and SWO are given along with its simulated performance, followed by performance comparison with state-of-the-art.

### 4.1 Loaded line phase shifter

#### 4.1.1 State-of-the-art-review: mm-wave phase shifter

As mentioned in the introduction of this chapter, phase shifters is the key element for proposed resonator design for varying the phase and hence, the oscillation frequency of oscillator. Several types of phase shifters are demonstrated in the literature. They can be classified as passive or active, with digital or analog tuning. Reflection type [1], loaded-line [2] – [7] and switched-line [8] are examples of currently used phase shifters. However, for the proposed SWO design a loaded-line phase shifter is needed. Firstly, because reflection-type phase shifters use a 3-dB coupler, usually a hybrid coupler that occupies large area and has a high insertion loss at mm-wave frequencies. Secondly, switched-line phase shifters are based on SPDT switches that can be realized in a wide variety of ways, i.e. by using FET, diode, or MEMS (micro-electro-mechanical systems) switches. It is important to choose a switch technology appropriately for the frequency band of interest. As active phase shifter consume high DC power [9], so passive phase shifter for design the proposed SWO is preferred.

The Figure of Merit ( $FoM$ ) of a phase shifter ( $\Delta\phi$ ) is defined as the ratio of the maximum phase shift over the maximum insertion loss ( $\alpha_{max}$ ), expressed in  $^{\circ}/dB$ , eq. (4.1).

$$FOM = \Delta\phi/\alpha_{max} (^{\circ}/dB) \quad (4.1)$$

In [2] phase shifter design was proposed based on millimeter-wave coplanar strip (CPS) in 650  $\mu\text{m}$  GaAs substrate using 0.25  $\mu\text{m}$  MMIC process. Schottky varactor diodes were used

between the coplanar strip lines to control the line CPS capacitance as a phase shifter. Fabricated phase shifter showed maximum phase shift of  $110^\circ$  and insertion loss of 5.6 dB at 60 GHz. The distributed phase shifter, shown in Figure 4.1, comprises a high impedance CPS line ( $Z_C = 100 \Omega$ ) periodically loaded with voltage-controlled variable capacitors ( $C_{var}$ ). The capacitance of the varactor diodes changes (20 fF to 34.5 fF) with variation of the bias voltage between two strip lines. This has the effect of changing the phase velocity of the CPS line, which can be effectively used to control the electrical phase shift of the lines with the fixed physical length. In [2] the measured return losses and insertion loss was better than 15 dB and 3.2 dB, respectively, up to 70 GHz. The chip size of this phase shifter was  $1.46 \times 0.24 \text{ mm}^2$ .

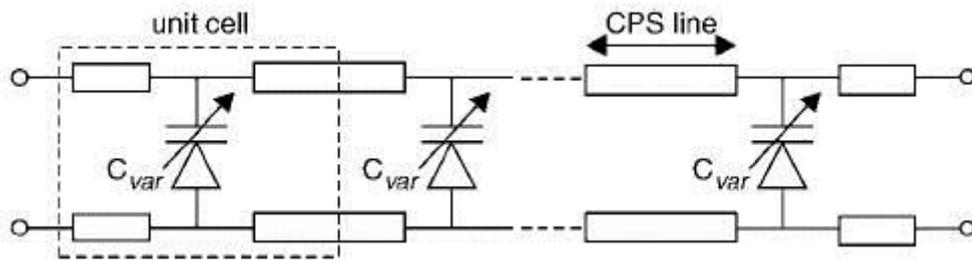


Figure 4.1: Distributed phase shifter [2]

In [3], [4] digital control of the effective dielectric constant of a differential mode transmission line has been presented up to 60GHz in IBM 90nm CMOS technology. The achieved variation in effective dielectric constant was from 5 to over 50 for the fixed artificial dielectric case. Unlike [1] and [2], in [3] MOS switches were used (Figure 4.2) to dynamically control the phase, i.e. to control digitally the phase variation. DiCAD achieves 50% of the physically available tuning range with effective dielectric constants varying between 7 and 28. The measured performance of a  $200 \mu\text{m}$  longer DiCAD showed phase variation of  $20^\circ$  corresponding to the effective dielectric constant varying from 7 to 28. In off state of switches loss of DiCAD line is  $-4 \text{ dB/mm}$ , while in on state the losses are beyond  $-14 \text{ dB/mm}$ . In [4] a DCO, i.e. digitally controlled oscillator, has been proposed based on the concept of DiCAD proposed in [4].

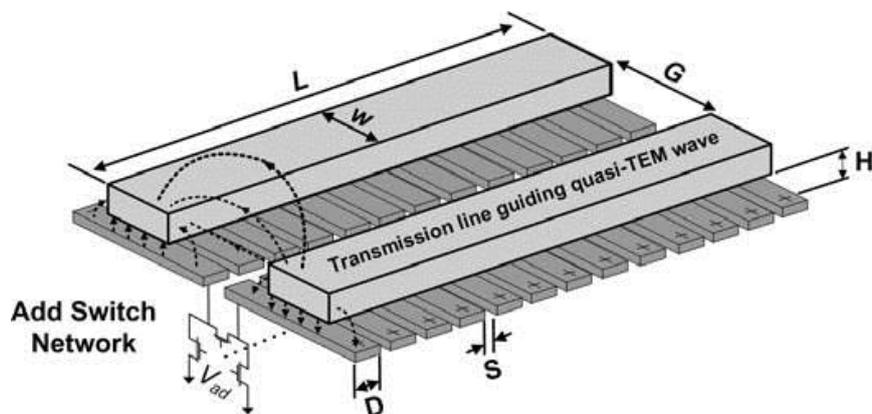


Figure 4.2: Digital controlled artificial dielectric (DiCAD) differential transmission line with NMOS switch network [3], [4]

The same concept of digitally controlling the effective dielectric constant of transmission line has been presented in [5] and [6] in order to change the phase and hence the frequency of

DCOs. A digitally controlled TL is used for both coarse tuning (CB) and mid-coarse tuning (MB) as shown in Figure 4.3.

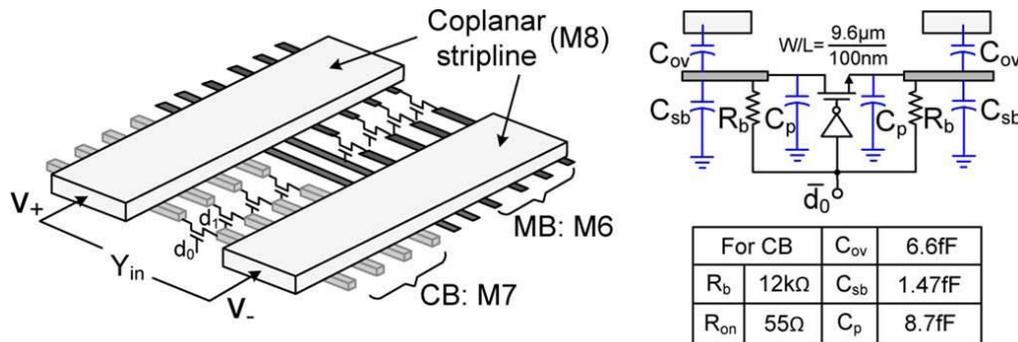


Figure 4.3: 3-D view of the reconfigurable TL for coarse- and mid-coarse tuning and detailed switch schematic, including parasitics [5], [6]

There is freedom in this design [5], [6] to dimension the metal strips and place them on different metal layers in order to obtain CB and MB with the desired frequency step ratio (e.g., 8). A 19-bit thermometer-coded CB and 8-bit MB are implemented as shown in Figure 4.4. Each bit in the CB (i.e., M7 strip) can introduce a  $\Delta C$  of 1.2 fF, which corresponds to a frequency change of 315 MHz at 60 GHz, whereas the MB located on the (lower) M6 achieves a  $\Delta C$  of 0.13 fF/bit (1/8 of the CB step-size). The switchable capacitance ratio ( $C_{max}/C_{min}$ ) of 1.6 provides over 6-GHz tuning range and a minimum tank Q-factor of 12 when all CB and MB switches are ON.

In [7] a 30° continuous tunable phase shifter at 60 GHz working frequency was designed based on the predictive electrical model of the slow-wave coplanar waveguide (S-CPW) structure. To design this phase shifter a slow-wave structure has been considered. Unlike [3] – [6], in [7] SCPW has been utilized to design the phase shifter. To design the phase shifter in [7] the floating shields were broken between the signal and the ground, to allow connecting varactors in between, shown in Figure 4.4. This 30° phase shifter was designed in BiCMOS 55nm technology.

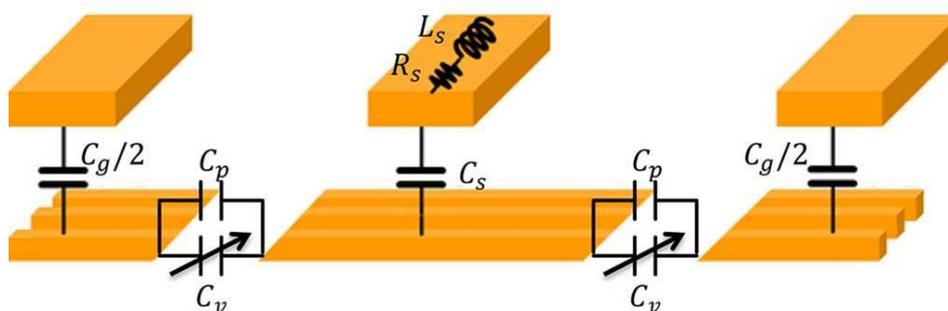


Figure 4.4: 3D Phase shifter model [7]

As mentioned in [7], for designing such tunable phase shifter, a 3D EM simulation tool is needed, together with a deep understanding of the S-CPW's physical behavior, and retro simulations between 3D-EM tools and CAD tool (Cadence for example) are necessary. This procedure drives to long developing times. The model proposed in [7] allows the designer to make a quick optimization by scripting it directly in any CAD tool.

To design the phase shifter, technique of adjusting the effective permittivity, and hence the electrical length (i.e. phase) has been applied in all the referred papers. As remarked above

there exists two ways of designing such phase shifters, i.e. either by discrete or digital control [3]- [6] by employing switches, or by adding varactors [2], [7] within the transmission line.

In [3] and [4] use of switches for phase shifter design lead to higher losses while, the one proposed in [5] and [6] resulted in good performance. However, utilizing switches and discrete control is a complex method to start with. As the targeted frequency band for SWO design is a continuous band, i.e. 81 GHz to 86 GHz, so the use of varactors for phase shifter design seems to be a better choice. Also, the method of utilizing equivalent RLRC model instead of 3D EM simulation proposed in [7] is a quick optimization technique for such circuits (phase shifter in our case). So, based on the concept of determining RLRC model [7], in following section 4.1.2 three S-CPS based phase shifter topologies are presented and compared.

#### 4.1.2 Phase shifter topologies

As remarked in Chapter 1 (Section 1.3), there exist several VCOs in state-of-the-art that utilize transmission lines based resonator [4] – [6], [10]- [18] due to the advantage it offers over lumped LC tank, as the most fundamental need is high- $Q$  resonator for VCO design. Due to the topology (geometry and metal layers) S-CPS based phase shifter can be implemented in different manners. Based on the study presented in Chapter 3 (Section 3.2.2), i.e. variation in  $Q$ -factor vs characteristic impedance ( $Z_C$ ) for a quarter wavelength transmission line, high- $Z_C$  has been targeted to achieve high- $Q$ . To design the phase shifter, varactors are distributed all along the resonator length, as it allows distributing the loading effect of varactors. Before proposing a specific phase shifter topology for high- $Z_C$ , several topologies are studied in this section, based on placing varactor within S-CPS.

As discussed in chapter 3 (section 3.2.3), the electromagnetic simulation (in full-wave 3D-EM tool) takes immense amount of time. So the design and analysis of S-CPS based phase shifter topologies is performed with the equivalent  $RLRC$  model of S-CPS based on [7]. Please note that in [7] S-CPW was considered, whereas in this thesis the model for S-CPS is utilized based on same approach.

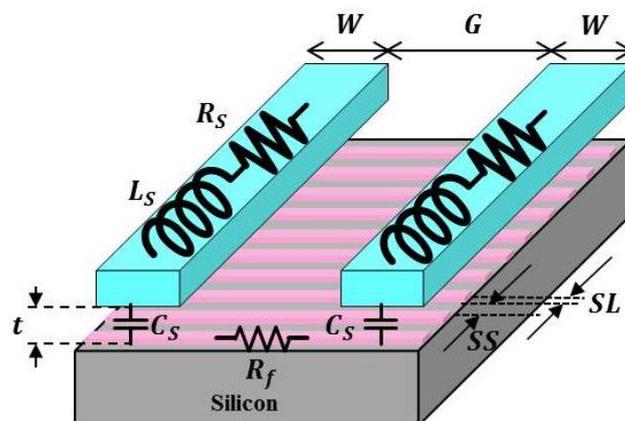


Figure 4.5: 3-D view of S-CPS

As explained in chapter 3 also, S-CPS is composed of a conventional CPS transmission line loaded by a patterned shield, which is electrically floating, shown in Figure 4.5. In CMOS/BiCMOS technologies, the periodic shield is implemented below the CPW strips. Therefore,

the electric field is trapped in between the CPS strips and the shield preventing conductive losses in the bulk silicon. In contrast, the magnetic field is not perturbed due to its conservative properties. The *RLRC* model proposed in [7] is shown in Figure 4.6.

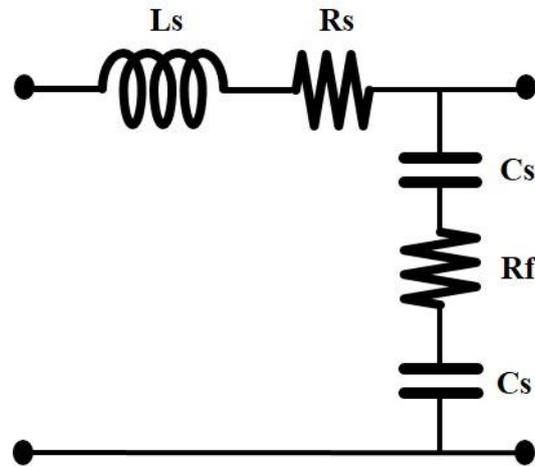


Figure 4.6: Equivalent electrical circuit

It consists of an inductance ( $L_S$ ) due to the current propagation in the CPS, a capacitance ( $C_S$ ) related to the capacitive effect between the CPS strips and the shield, resistances. The resistances reflect conductive losses in the CPS strips ( $R_S$ ) and the conductive losses in the shield ( $R_f$ ). To extract these component values, two simulations were performed [19], i.e. an electric and a magnetic simulation. The electric simulation allows  $C_S$  and  $R_f$  calculation, whereas the magnetic simulation gives  $L_S$  and  $R_S$ .

Based on the assumption of Quasi-TEM propagation mode inductive and capacitive elements were calculated independently in [7]. Similarly, conductive losses were splitted in the CPS strips and in the patterned shield.

The inductance was extracted from the measured S parameters by using the well-known relation [7], given by eq. (4.2)

$$L_S = \text{Imag} (Z_C \beta / \omega) \quad (4.2)$$

Conductive losses in the CPS, i.e.  $R_S$ , are modelled by the method proposed in [20], whereas conductive losses in the floating shield i.e.  $R_p$ , are simply modelled eq. (4.3) [7],

$$R_p = \frac{1}{4d} \left( \frac{D}{\sigma_{shield} t_{shield}} \right) \quad (4.3)$$

where,  $d$  is shield period ( $d = SS + SL$ ),  $D$  is the distance between two strips of S-CPS ( $D = G$ ), and  $\sigma_{shield}$  and  $t_{shield}$  is conductivity and thickness of shield field metal layer, respectively.

Lastly, the total capacitance at each region is computed by sum of electric field lines [7], given by eq. (4.4).

$$C = \frac{\epsilon_o \epsilon_r W l}{n} \left( \sum_{i=1}^n \frac{1}{h_i} \right) \quad (4.4)$$

where,  $\epsilon_0$  is the dielectric constant in vacuum,  $\epsilon_r$  is the relative dielectric constant,  $W$  is width of the conductor,  $l$  is its length and  $h_i$  is the height or distance between conductors.

Based on above mentioned equations, in subsections below, the possible S-CPS based phase shifter topologies are analyzed and then the reason to propose an unsymmetrical phase shifter for VCO design is given.

#### 4.1.2.1 Topology 1

One of the proposed topology is shown in Figure 4.7. The varactors, for tuning the phase of the resonator, are distributed along the transmission line. This is done by connecting varactors between floating shield and both ('+' and '-') signal strips. It is to be noted that width of each finger strip and space between fingers is small ( $0.6 \mu\text{m}$ ) [19]. Hence, varactors must be connected by grouping several fingers since a varactor is much larger than one finger. Grouping a number of fingers depends on the method used for designing the phase shifter (given in section 4.2.1). On reviewing Figure 4.13, this topology can be implemented in a VCO. Indeed, the voltage across the varactor can be varied if the tuning voltage (say  $V_t$ ) is connected to the fingers and the fixed voltage (say  $V_{dd}$ ) is connected to the shorted end of the resonator.

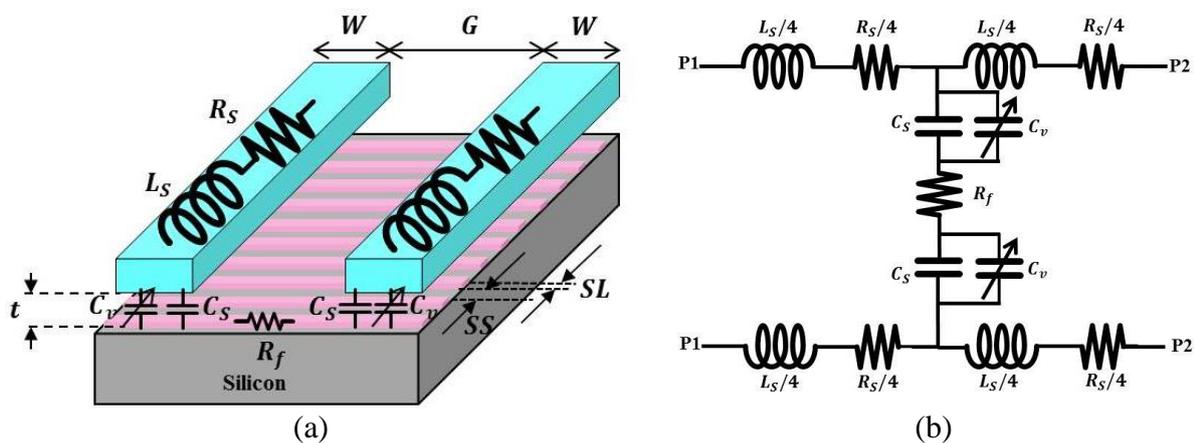


Figure 4.7: (a) 3-D view of proposed topology 1 and (b) equivalent electrical circuit

The simulated electrical characteristics of  $\lambda/4$  phase shifter (i.e. with phase shift around  $90^\circ$ ) with topology 1 are given in Table 4.1. As two varactors are placed in this topology, so a short length of  $66 \mu\text{m}$  is needed to design a  $\lambda/4$  phase shifter and by tuning the varactors the phase shift ( $S_{21}^\circ$ ) of  $17^\circ$  is achieved varying around  $90^\circ$ .

$V_t$	0	2.4
$S_{21}^\circ$	-102	-85
$Z_c (\Omega)$	17	22
$\alpha(Np/mm)$	5.9	3.4
$\alpha(dB/mm)$	51.2	29.5
$Q - factor$	2.5	3.5

Table 4.1: Electrical characteristics of topology 1

This topology offers very low- $Q$ , i.e. 2.5 to 3.5 (approx.). It is due to the fact that large varactors are employed in this phase shifter periodically. Large varactors are needed in this topology because the capacitance ( $C_S$ ) generated due to slow-wave effect adds parasitic

capacitance ( $\sim 0.9 \text{ fF}$ ) hence increasing the needed value of the variable capacitance. Hence, due to its low  $Q$ -factor this topology is not suited to VCOs.

#### 4.1.2.2 Topology 2

The second proposed topology is shown in Figure 4.8. The idea is to break the floating shield between both the signal strips to allow connecting varactors in between. Figure 4.8(b) shows the equivalent schematic model for one group of phase shifter. In this equivalent schematic, it is easy to bias both sides of varactor, i.e. fixed voltage ( $V_{dd}$ ) on one and the tunable voltage ( $V_t$ ) on the other terminal of varactor. Nevertheless if we focus on the layout of the phase shifter, shown in Figure 4.8(a), we can see that there is a parasitic capacitance ( $C_p$ ) parallel to  $C_{var}$ , due to the coupling effect. Even though this topology offers better  $Q$ -factor than topology 1 (presented in section 4.1.2.1) the high  $C_p$  leads large varactors and hence increases the losses.

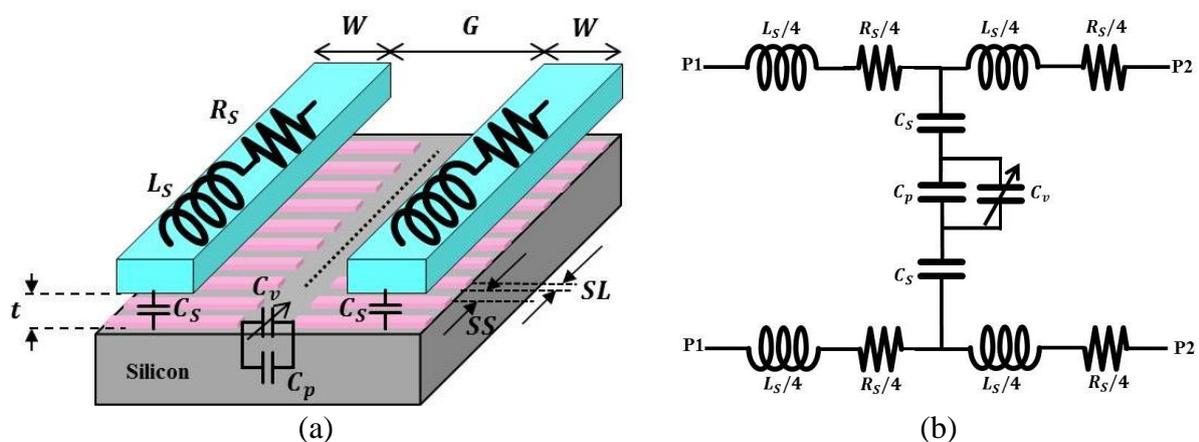


Figure 4.8: (a) 3-D view of proposed topology 2 and (b) equivalent electrical circuit

The simulated electrical characteristics of  $\lambda/4$  phase shifter (i.e. with phase shift around  $90^\circ$ ) with topology 2 are given in Table 4.2. As compared to topology 1 (refer section 4.1.2.1), this topology consists of only one varactor, so a longer length of  $180 \mu\text{m}$  is needed to design a  $\lambda/4$  phase shifter and by tuning the varactors the phase shift ( $S_{21}^\circ$ ) of  $7.5^\circ$  is achieved.

$V_t$	0	2.4
$S_{21}^\circ$	$-92.5$	$-85$
$Z_c (\Omega)$	47	52
$\alpha(Np/mm)$	0.24	0.21
$\alpha(dB/mm)$	2	1.8
$Q - factor$	19	19.5

Table 4.2: Electrical characteristics of topology 2

Since only one varactor is utilized in this topology so the achieved phase shift ( $\Delta\phi \approx 7.5^\circ$ ) is less than topology 1 ( $\Delta\phi \approx 17^\circ$ ). However the losses are very high in topology 1 as compared to topology 2, hence resulting  $Q$ -factor of latter is better. Please note that in topology 2, the achieved phase shift is very less due to the fact that a large coupling capacitor ( $C_p$ ) is connected parallel to varactor.

So, referring to both the topologies shown in Figure 4.7 and 4.8, we can say that topology 1 shows more losses due to need of two varactors with  $\Delta\phi \approx 17^\circ$ . Whereas, in topology 2 there is only one varactor, so the losses are lower as compared to topology 1 with  $\Delta\phi \approx$

7.5° only. Hence, a tradeoff between  $Q$ -factor and phase shift (that will determine the frequency tuning range of VCO) can be remarked on comparing both topologies. To increase the tuning range of topology 2 larger varactors are needed to overcome the coupling capacitance  $C_P$ , hence leading to high losses.

#### 4.1.2.3 Topology 3: Unsymmetric phase shifter: Proposed topology

So, in order to avoid this problem of high parasitic and losses, an unsymmetric phase shifter topology is proposed in this section, by involving one advantage of above presented topologies, i.e. advantage of ease of biasing varactor from topology 1 and using one capacitance from topology 2.

Figure 4.9 shows the topology of unsymmetric phase shifter. As per the proposed idea, only one varactor is used for tuning but to reduce the parallel connected capacitance the width of the strip ( $W_2$ ) is reduced (width where varactor is connected). Due to smaller width ( $W_2$ ) the capacitance ( $C_{S2}$ ) is 80% lower as compared to ( $C_{S1}$ ). So, this topology gives more flexibility for tuning the phase and hence the frequency.

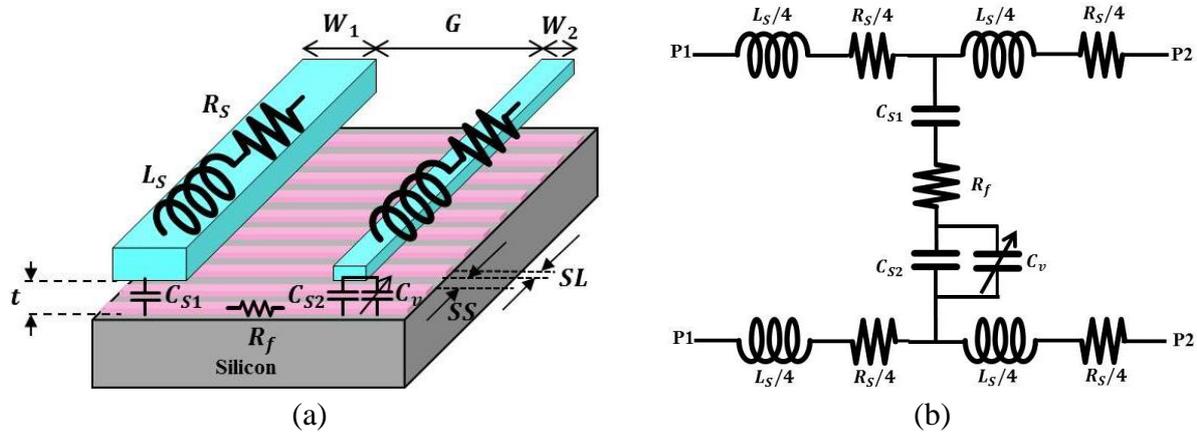


Figure 4.9: (a) 3-D view of proposed topology 3 and (b) equivalent electrical circuit

The simulated electrical characteristics of  $\lambda/4$  phase shifter (i.e. with phase shift around 90°) with topology 3 are given in Table 4.3. The achieved  $Q$ -factor is less as compared to topology 2, but the achieved phase shift is better. The length of 168  $\mu\text{m}$  is utilized to design  $\lambda/4$  phase shifter. A detailed comparison of three topologies is given in Table 4.4. With slight increment in losses the tuning range of 10° is achieved in topology 3, while in topology 2 the tuning range was 7.5°. Hence, topology 3 is chosen for designing the SWO in section 4.2.

$V_t$	0	2.4
$S_{21}^\circ$	-96	-86
$Z_C (\Omega)$	48	54
$\alpha(Np/mm)$	0.37	0.33
$\alpha(dB/mm)$	3.2	2.8
$Q - factor$	13.5	13.7

Table 4.3: Electrical characteristics of topology 3

Electrical characteristics	Topology 1	Topology 2	Topology 3
$\Delta\phi$	17°	7.5°	10°
$\alpha_{maximum}(dB/mm)$	51.2	2.1	3.2
$Q_{minimum}$	2.5	19	13.5

Table 4.4: Comparison of phase shifter topologies

Before starting the phase shifter and SWO design, a methodology is decided and followed in section 4.2.1 and 4.2.2, respectively.

## 4.2 Proposed VCO design with S-CPS based phase shifter as resonator

To analyze the proposed idea, a method has been followed for designing the phase shifter, as proposed in section 4.2.1. There exists several design parameters as shown in Figure 4.9. Depending on these parameters the varactor has to be chosen with a particular tuning range in order to estimate the tuning range of, firstly the phase shifter and then of VCO. The tuning range of the phase shifter has to be slightly higher for VCO design in order to consider the parasitic capacitance added by cross-coupled pair and output buffers.

### 4.2.1 Followed method for phase shifter design

Figure 4.10 shows the side view and top view of the phase shifter topology, where the S-CPS is periodically loaded (from 1 to  $n$  groups) with varactor capacitance. Figure 4.11 shows the equivalent lumped model for one group of the phase shifter (same as Figure 4.5).

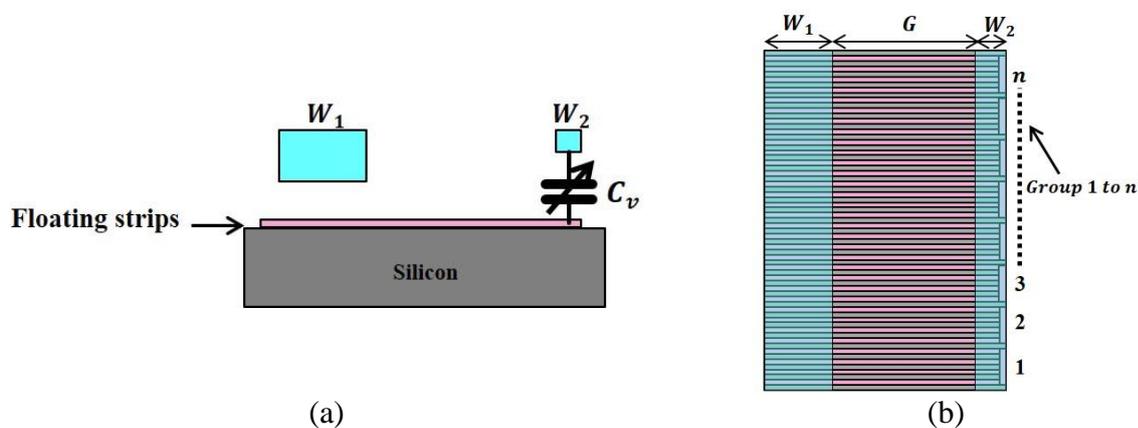


Figure 4.10: (a) Side view and (b) Top view of phase shifter topology

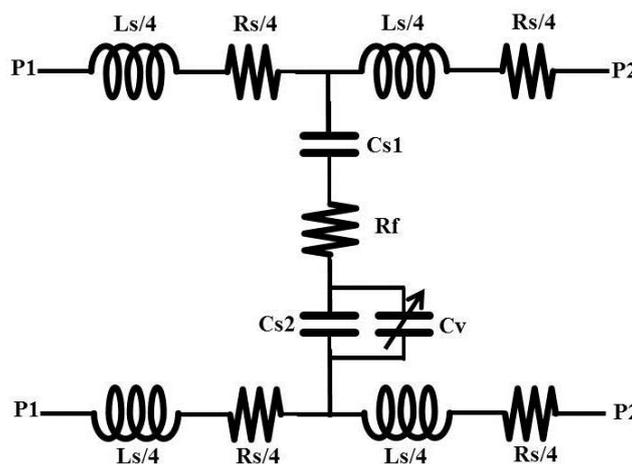


Figure 4.11: Equivalent lumped model for one group of phase shifter

The first step to design a phase shifter is to choose a varactor ( $C_v$ ) according to the needed *FTR* of VCO. But as shown in Figure 4.7, along with the varactor ( $C_v$ ) there are additional capacitances, i.e.  $C_{s1}$  and  $C_{s2}$  created under strips with  $W_1$  and  $W_2$ , respectively. Hence these added capacitances must be considered while evaluating the needed varactor capacitance. The phase velocity can be given by eq. (4.5),

$$V_\varphi = \frac{1}{\sqrt{LC_{eq}}} = \frac{C_o}{\sqrt{\varepsilon_{eff}}} \quad (4.5)$$

where,  $C_o$  is velocity of light and  $C_{eq}$  is the equivalent capacitance of the resonator.

$$\varepsilon_{eff} = C_o^2 LC_{eq} \quad (4.6)$$

We know that electrical length ( $\theta$ ) is given by,

$$\theta = \beta l = \frac{2\pi}{\lambda} l = \frac{\omega}{V_\varphi} l = \frac{\omega \sqrt{\varepsilon_{eff}}}{C_o} l \quad (4.7)$$

Using eq. (4.6) in eq. (4.7),

$$\theta = \frac{\pi}{2} = \frac{\omega l \sqrt{C_o^2 LC_{eq}}}{C_o} \quad (4.8)$$

Note that eq. (4.8) is valid only for quarter wavelength. Under this condition, eq. (4.8) can be rewritten as,

$$\frac{\pi}{2} = \omega l \sqrt{LC_{eq}} \quad (4.9)$$

$$C_{eq} = \frac{1}{L(4 \cdot f \cdot l)^2} \quad (4.10)$$

In eq. (4.6),  $L$  is the inductance in ( $H/m$ ), so the calculated  $C_{eq}$  will be in ( $F/m$ ). Hence for maximum and minimum frequency of oscillation, we have

$$C_{eq, min} = \frac{1}{L(4 \cdot f_{max} \cdot l)^2} \quad (F/m) \quad (4.11a)$$

$$C_{eq, max} = \frac{1}{L(4 \cdot f_{min} \cdot l)^2} \quad (F/m) \quad (4.11b)$$

The  $C_{eq}$  in eq. (4.10) and eq. (4.11) can also be written as (refer Figure 4.9 also),

$$C_{eq} = \frac{C_{S1} * (C_{S2} + C_v)}{C_{S1} + C_{S2} + C_v} \quad (4.12)$$

Hence the value of varactor capacitance ( $C_v$ ) can be determined from eq. (4.12),

$$C_v = \frac{C_{S1} * C_{eq} + C_{S2} * C_{eq} - C_{S1} * C_{S2}}{C_{S1} - C_{eq}} \quad (F/m) \quad (4.13)$$

where,  $C_{S1}$  and  $C_{S2}$  are determined in farads ( $F$ ). They have been converted in ( $F/m$ ) to compute  $C_v$  in ( $F/m$ ), in order to compute the needed  $C_{vmax}$  and  $C_{vmin}$  in ( $F$ ) per group. This can be done by multiplying  $C_v(F/m)$  with length of one group. Hence  $C_{vmax}$  and  $C_{vmin}$  can be determined in accordance with that of  $C_{eq, max}$  and  $C_{eq, min}$ , respectively. Also, in order to recheck the applied methodology, the phase shift ( $\theta = \omega l \sqrt{LC_{eq}}$ ) must be calculated again, which must be equal to  $90^\circ$ .

Figure 4.12 shows the flow diagram of the applied methodology. Before starting the phase shifter design, we fix the minimum and maximum frequency of oscillation.

In **Step 1**, we need to choose the dimension of S-CPS and their respective metal layers. Also, the number of fingers per group and number of groups in the phase shifter must be decided in this step.

In **Step 2**,  $C_{S1}$ ,  $C_{S2}$ ,  $L_S$ ,  $C_{eq,max}$  and  $C_{eq,min}$  are determined [7] in (unit/m). For determining these parameters no EM simulations are needed in this method since [7] gives an accurate model based on geometry.

In **Step 3**,  $C_{vmax}$  and  $C_{vmin}$  are computed for one group, refer eq. (4.13). Then the varactor is chosen from the design kit of BiCMOS 55 nm technology. The varactor is sized to achieve  $C_{min}$  and  $C_{max}$  with the maximum  $Q$ -factor.

In **Step 4** the equivalent RLRC model for one group of phase shifter is determined based on the same approach as [7], also presented in section 4.1.2.

In **Step 5** the  $S_{21}$  phase of cascaded groups is computed (for same number of groups as decided in Step 1), in order to recheck if the average phase shift is  $90^\circ$  or not (normally it is around  $90^\circ$ ).

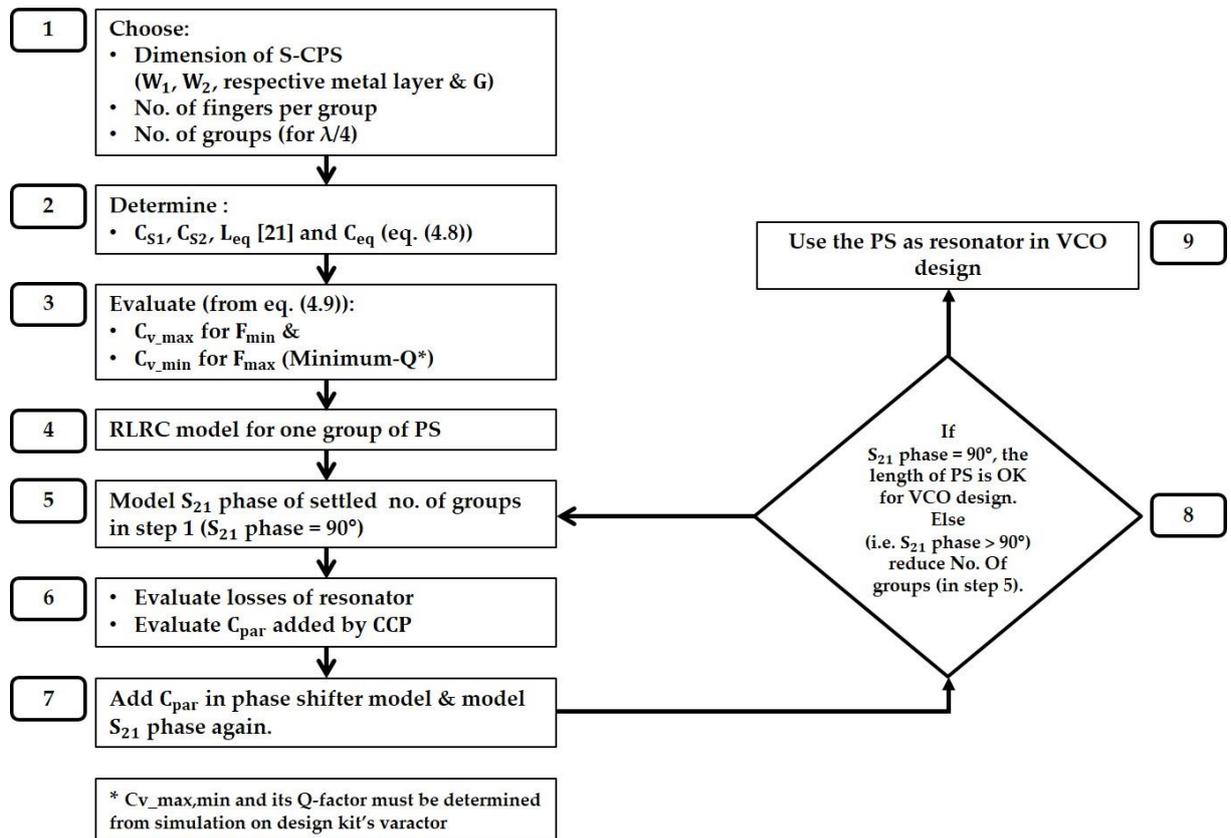


Figure 4.12: Flow diagram of applied methodology

In **Step 6** the equivalent  $R_p$  of the phase shifter is determined based on  $RLRC$  model using one-port method (refer chapter 2, section 2.2.3). From  $R_p$  the needed negative resistance for loss compensation and hence the added  $C_{par}$  are determined. This added  $C_{par}$  from nMOS cross-coupled pair and from buffer leads to increment in  $S_{21}$  phase, as expected from eq. (4.8).

In **Step 7**  $C_{par}$  is added to  $RLRC$  model of phase shifter and  $S_{21}$  phase is computed again.

The **Step 8** is a decision state/ step, i.e. if S21 phase (average value) is  $90^\circ$  (typically no in the first sequence of operation), then the phase shifter can be employed in VCO design (in **Step 9**), else the length of phase shifter has to be reduced in Step 5. This cycle continues till average phase shift of phase shifter is  $90^\circ$ . After this step we can employ the phase shifter (with reduced no of groups) in the SWO as a resonator.

#### 4.2.2 81 – 86 GHz VCO design with phase shifter as resonator

The flow diagram given in Figure 4.12 (section 4.2.1) gives the steps to design the phase shifter. But the SWO design process does not end on the step 9 of this flow diagram. As mentioned several times in previous chapters that to compensate losses the price to pay is addition of parasitic capacitance and hence, losing  $FTR$  of the oscillator. In this SWO design also, we need to know these parasitic capacitance value in order to redesign the phase shifter to fit the oscillation frequency of SWO from 81 to 86 GHz. In other words, initially as per needed  $FTR$  of 5 GHz and  $F_{osc}$  from 81 to 86 GHz, the tuning range of varactor must be 1.4. But added parasitic capacitance from cross-coupled pair and output buffer leads to a tuning range less than 3 GHz, and shift in oscillation frequency as well. Hence the tuning range of varactor has to be increased to 2.5 or higher to reach  $FTR$  of 5 GHz. This whole phenomenon is explained in this section. The architecture of this VCO is shown in Figure 4.13.

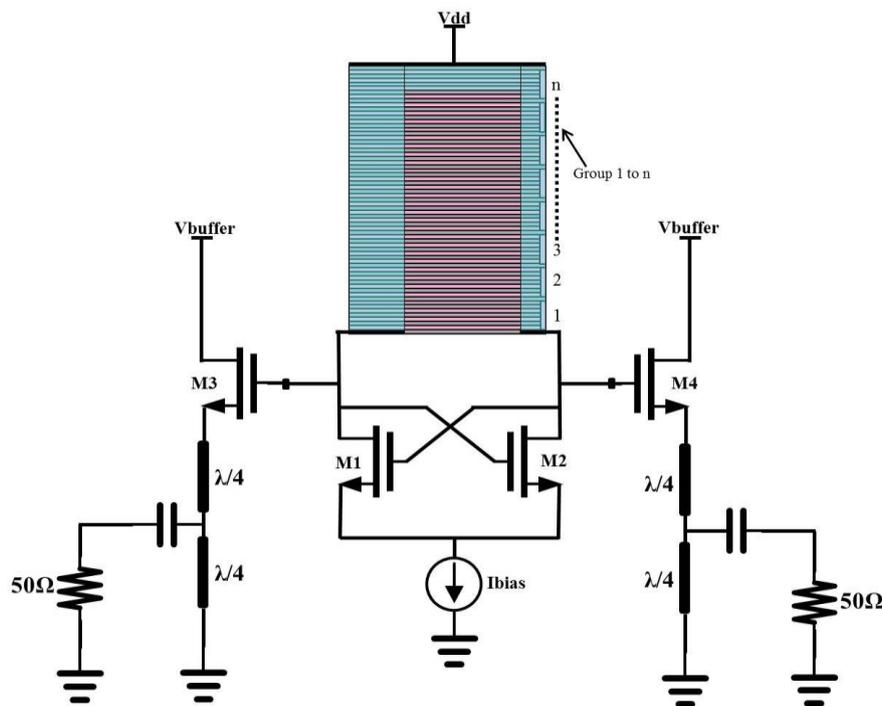


Figure 4.13: VCO architecture

The stepwise design process is as follows: Step 1: (a) the chosen dimension of unsymmetric S-CPS based phase shifter is given in Table 4.5.

Dimension of unsymmetric S-CPS		Metal layer
$W_1$	20 $\mu\text{m}$	M8 – M6
$W_2$	5 $\mu\text{m}$	M8
$G$	30 $\mu\text{m}$	
<b>Fingers (<math>SS = SL</math>)</b>	0.6 $\mu\text{m}$	M3

Table 4.5: Chosen dimension of unsymmetric S-CPS

(b) No. of fingers per group = 5; No. of groups = 25; Length of phase shifter = 150  $\mu\text{m}$ .

Step 2 & 3: As per evaluated inductance ( $L$ ), capacitances ( $C_{S1}$ ,  $C_{S2}$  and  $C_{eq}$ ) and for needed frequency tuning range of SWO the needed varactor capacitance specification is given in Table 4.6.

$C_{v\_min}$	3.9 fF
$C_{v\_max}$	5.4 fF
$T.R. = C_{v\_max}/C_{v\_min}$	1.4

Table 4.6: Evaluated capacitance

The needed capacitance and tuning range of varactor can be obtained by following specifications of varactor, given in Table 4.7.

Dimension of varactor		Electrical characteristics of Varactor	
Width	1.9 $\mu\text{m}$	$C_{vmax}$	5.4 fF
Length	0.08 $\mu\text{m}$	$C_{vmin}$	3.8 fF
No. of fingers	2	$T.R. = C_{vmax}/C_{vmin}$	1.4
nbcells	2	$Q_{min}$	17.8

Table 4.7: Varactor specifications and characteristics

Step 4: The RLRC model of phase shifter is given in Table 4.8.

$R_s$	0.14 $\Omega$
$L_s$	6.14 pH
$C_{S1}$	4.1 fF
$C_{S2}$	0.79 fF
$R_f$	0.38 $\Omega$

Table 4.8: Equivalent RLRC model

Step 5: The electrical characteristics of the phase shifter is given in Table 4.9, for a physical length of 144  $\mu\text{m}$ .

$Vt(V)$	0	2.4
$S_{21}^\circ$	-95.4	-90.7
$Z_c (\Omega)$	49.6	52.3
$\alpha (Np/m)$	376	375
$\alpha (dB/mm)$	3.2	3.3
$\epsilon_{reff}$	47.6	43.6
$Q_{ps\_min}$	13	

Table 4.9: Electrical characteristic of phase shifter

Step 6: Loss estimation of phase shifter by one-port method lead to equivalent losses of 391  $\Omega$  to 995  $\Omega$ . For LCF of 3 the needed  $R_{negative}$  for compensating the losses is -130  $\Omega$ . This value of negative resistance will add a parasitic capacitance of 32 fF (in addition to 14 fF of loading capacitance from output buffers) and with a high power consumption of (12 mA $\times$ 1.2 V).

Step 7: These values of added parasitic capacitance lead to increment in electrical length ( $S_{21}^\circ$ ) beyond 90 $^\circ$ , i.e.  $\approx$ 130 $^\circ$ .

Step 8: Hence the number of groups are reduced in order to reduce the electrical length to  $90^\circ$  (by taking added parasitic capacitance into account). So, with reduced number of groups, i.e. with 17 groups of phase shifter the loss estimation is performed again (step 6). The determined value of losses from one port method varies from  $841 \Omega$  to  $992 \Omega$ . With  $LCF$  of 3 the needed value of  $R_{negative}$  for compensating the losses is  $-280 \Omega$ . To achieve  $-280 \Omega$  of  $R_{negative}$  cross-coupled pair of  $12.5 \mu m$  width has been utilized. All design parameters are given in Table 4.10.

$R_p (\Omega)$	841 to 992
$R_{negative} (\Omega)$	-280
<b>nMOS cross-coupled pair</b>	$W = 12.5 \mu m; L = 0.06 \mu m; Nf = 13$
<b>Bias current (mA)</b>	7.8
$C_{par} (fF)$	14.6
$C_{par\_buffer} (fF)$	14

Table 4.10: Design parameters of cross-coupled pair

The current from current source can be varied from 2.3 mA to 7.8 mA by varying the bias voltage ( $V_b$ ) of current source from 0.5 V to 0.7 V, respectively. Hence,  $LCF$  is varied from 2 to 3 by varying  $V_b$  from 0.5 V to 0.7 V, respectively, as given in Table 4.11.

$V_b(V)$	$I_d(mA)$	$R_{neg}(\Omega)$	$C_{par}(fF)$	$LCF = R_p / R_{neg}$
0.5	2.3	-420	14	2
0.7	7.8	-280	14.6	3

Table 4.11: Variation in  $I_d$  (mA),  $R_{neg}$  ( $\Omega$ ) and  $LCF$  with  $V_b$  (V)

In Table 4.12 the performance based on S-parameter, transient and harmonic balance simulations are given. Similar to Chapter 2 and 3, the estimated oscillation frequency and tuning range from S-parameter simulation are given in Table 4.12 (a), by observing the point where  $Real(Z_{port})$  is negative and  $Imag(Z_{port})$  intersects zero.

The time response of SWO was observed with transient simulation. As in transient simulation only output voltage of oscillator can be observed so, the oscillation frequency and tuning range, given in Table 4.12 (b), is hand calculated.

In Table 4.12 (c) the performance of SWO based on harmonic balance simulation is given. With harmonic balance simulation the phase noise ( $PN$ ) performance of the SWO is obtained, given in Table 4.12. The phase noise is  $-88$  dBc/Hz to  $-90.1$  dBc/Hz at 1MHz and  $-109.6$  dBc/Hz to  $-112$  dBc/Hz at 10 MHz offset, respectively. As all the three simulations presented in Table 4.12 are performed with different simulators, so slight variation between these three simulations is expected.

<i>Simulation</i>	$V_b(V)$	$V_t(V)$	$F_{osc}(GHz)$	$FTR (GHz)$
<i>S-parameter</i>	0.5	0	84	3.3
		2.4	87.3	
	0.7	0	83.2	3.3
		2.4	86.5	

(a)

<i>Simulation</i>	$V_b(V)$	$V_t(V)$	$F_{osc}(GHz)$	$FTR (GHz/\%)$	$V_{out}(V)$
<i>Transient</i>	0.5	0	84.7	3.8/ 4.4	0.16
		2.4	88.5		0.18
	0.7	0	83.3	2.5/ 3	0.38
		2.4	85.8		0.4

(b)

<i>Simulation</i>	$V_b(V)$	$V_t(V)$	$F_{osc}(GHz)$	$FTR (GHz)$	$V_{out}(V)$	$PN (dBc/Hz)$	$FOM_T (dBc/Hz)$
<i>Harmonic balance</i>	0.5	0	84.6	3.5	0.13	-82.2 to -86.3 @ 1MHz	-173
		2.4	88.1		0.16	-104 to -107.2 @ 10MHz	-174
	0.7	0	83	3	0.32	-88 to -90.1 @ 1MHz	-170
		2.4	86		0.35	-110 to -112 @ 10MHz	-172

(c)

Table 4.12: (a) S-parameter; (b) Transient and (c) Harmonic balance simulation of VCO 3a

On comparing this simulation of SWO, say  $VCO3a$ , with  $VCO2$  presented in chapter 3, we can say that the phase noise performances are comparable. Specifically at 1MHz offset, the phase noise performance of presented  $VCO3a$  is better than  $VCO2$ . A detailed comparison of both designs is given in Table 4.13.

<i>Simulated performance parameters</i>	<i>VCO2: With S-CPS synthesized inductor</i>	<i>VCO3a: With S-CPS based phase shifter</i>
$F_o (GHz)$	83.6	84.5
$TR (GHz)$	5.3	3
$FTR (\%)$	6.3	3.6
$P_{out} (dBm)$	0.4	0.9
$P_{dc\_core} (mW)$	7.2	9.3
$PN$ at 1MHz offset (dBc/Hz)	-83 to -89	-88 to -90
$PN$ at 10MHz offset (dBc/Hz)	-104 to -113.3	-110 to -112
$FOM_T (dBc/Hz)$	-179.2	-172

Table 4.13: Performance comparison of VCO2 and VCO3a

Although  $FOM_T$  of  $VCO3a$  is less as compared to  $VCO2$ , but the phase noise performance has improved. The reduced  $FOM_T$  of  $VCO3a$  is due to the reduced  $FTR$ . While determining maximum to minimum value of needed varactors (in step 2 and 3) the effect of parasitic capacitance was not taken into account so, this performance (i.e. reduced  $FTR$ ) of  $VCO3a$  was anticipated.

To increase  $FTR$  of  $VCO3a$  larger varactors is added. It is important to note that these large varactors will also add losses to the phase shifter. Therefore increasing the overall loading effect and hence the increment in phase noise is expected. So, the losses of the phase shifter are modelled again and hence the cross-coupled pair is redesigned for loss compensation.

After performing retro simulations, the needed specification of varactor is given in Table 4.14 to cover the bandwidth of 5 GHz.

Dimension of varactor		Electrical characteristics of Varactor	
Width	1.7 $\mu\text{m}$	$C_{vmax}$	7.2 fF
Length	0.38 $\mu\text{m}$	$C_{vmin}$	2.9 fF
No. of fingers	1	$T.R. = C_{vmax}/C_{vmin}$	2.5
nbcells	2	$Q_{min}$	9.7

Table 4.14: Varactor specification for phase shifter design

The electrical characteristics of phase shifter for a physical length of 90  $\mu\text{m}$  are given in Table 4.15. This physical length is chosen after retro simulation and taking into account the parasitic capacitance.

$Vt(V)$	0	2.4
$S_{21}^\circ$	-59.8	-52
$Z_c(\Omega)$	47	53
$\alpha(Np/m)$	436	342
$\alpha(dB/mm)$	3.8	3
$\epsilon_{reff}$	43.6	33.6
$Q_{ps\_min}$	9	

Table 4.15: Electrical characteristics of phase shifter

The maximum estimated losses of the resonator determined using one-port method is 574  $\Omega$ . Hence the needed negative resistance is -191  $\Omega$  for LCF of 3. In order to compensate the losses, cross-coupled pair of 20 $\mu\text{m}$  width has been utilized. All design parameters are given in Table 4.16.

$R_p(\Omega)$ (Without resistive interconnects)	575 to 943
$R_p(\Omega)$ (With resistive interconnects)	552 to 847
$R_{negative}(\Omega)$	-190
nMOS cross-coupled pair	$W = 20 \mu\text{m}; L = 0.06 \mu\text{m}; Nf = 20$
Bias current (mA)	7.2
$C_{par}(fF)$	23
$C_{par\_buffer}(fF)$	14

Table 4.16: Design parameters of VCO

The current from current source can be varied from 2.6 mA to 8.6 mA by varying the bias voltage ( $V_b$ ) of current source from 0.5 V to 0.7 V, respectively. Hence, LCF is varied from 1.8 to 3 by varying  $V_b$  from 0.5 V to 0.7 V, respectively, as given in Table 4.17.

$V_b(V)$	$I_d(mA)$	$R_{neg}(\Omega)$	$C_{par}(fF)$	$LCF = R_p/R_{neg}$
0.5	2.6	-312	21.8	1.8
0.7	8.6	-181	23	3

Table 4.17: Variation in  $I_d$  (mA),  $R_{neg}$  ( $\Omega$ ) and LCF with  $V_b$  (V)

In Table 4.18 the post layout simulation (PLS) of SWO (VC03b) is given. In Table 4.18 the performance based on S-parameter, transient and harmonic balance simulations are given. The estimated oscillation frequency and tuning range from S-parameter simulation are given

in Table 4.18(a), by observing the point where  $Real(Z_{port})$  is negative and  $Imag(Z_{port})$  intersects zero.

The time response of this SWO, say  $VCO3b$ , was observed with transient simulation. As in transient simulation only output voltage of oscillator can be observed so, the oscillation frequency and tuning range, given in Table 4.18 (b), is hand calculated.

The phase noise ( $PN$ ) performance of  $VCO3b$  is obtained by harmonic balance simulation given in Table 4.18 (c). The  $PN$  varies from -85 dBc/Hz to -86 dBc/Hz at 1MHz and -108 dBc/Hz to -108 dBc/Hz at 10 MHz offset, respectively.

<i>Simulation</i>	$V_b(V)$	$V_t(V)$	$F_{osc}(GHz)$	$FTR (GHz)$
<i>S-parameter</i>	0.5	0	78.7	5.6
		2.4	84.3	
	0.7	0	77.5	5.4
		2.4	82.9	

(a)

<i>Simulation</i>	$V_b(V)$	$V_t(V)$	$F_{osc}(GHz)$	$FTR (GHz/ \%)$	$V_{out}(V)$
<i>Transient</i>	0.5	0	79.3	6.1/ 7.4	0.08
		2.4	85.4		0.15
	0.7	0	77.7	4.7/ 5.9	0.29
		2.4	82.4		0.35

(b)

<i>Simulation</i>	$V_b(V)$	$V_t(V)$	$F_{osc}(GHz)$	$FTR (GHz)$	$V_{out}(V)$	$PN (dBc/Hz)$	$FOM_T (dBc/Hz)$
<i>Harmonic balance</i>	0.6	0	79.3	6.2	0.08	-80.6 to -85.4 @ 1MHz	-176.3
		2.4	85.5		0.13	-102.4 to -106 @ 10MHz	-177
	0.7	0	77.4	4.8	0.3	-83 to -86 @ 1MHz	-170
		2.4	82.2		0.33	-105 to -108 @ 10MHz	-172

(c)

**Table 4.18: (a) S-parameter; (b) Transient and (c) Harmonic balance simulation**

Referring to Table 4.18, the bias voltage  $V_b$  was varied to vary the current and hence to vary the  $LCF$ . With  $V_b = 0.5 V$ , the tuning range was slightly higher as compared to other bias condition, because on lower bias voltage i.e.  $V_b = 0.5 V$ , the associated value of  $R_{neg}$  is lower and hence the parasitic capacitance is lower too. But for  $V_b = 0.5 V$  the phase noise is higher as the output power is low. On increasing the bias voltage to  $V_b = 0.7 V$ , the phase noise can be reduced, due to increment in output power, but the price to pay is higher power consumption. It must be noted that increasing the power consumption induces an increase of the associated parasitic capacitance as well (mentioned in Section 2.1.3), hence leading to another disadvantage of reduced  $FTR$ .

The resulting  $FOM_T$  for this  $VCO3b$  is higher for the bias states of  $V_b = 0.5$ , due to higher  $FTR$  and low power consumption. While in the other case (i.e.  $V_b = 0.7 V$ ) phase noise was lower, but due to high power consumption and reduced  $FTR$ ,  $FOM_T$  was low. The best possible  $FOM_T$  obtained for this  $VCO3b$  design is -176.3 dBc/Hz at 1MHz offset and -177 dBc/Hz at 10 MHz offset.

### 4.2.3 Comparison with state-of-the-art

Detailed comparison of proposed SWO (*VC03b*) with *VC02* and state-of-the-art is given in Table 4.19. On comparing the simulated performance of two presented SWOs (say *VC03a* and *VC03b*) with VCO design presented in Chapter 3 (say *VC02*), we can say that *VC03a* showed better performance in terms of phase noise, with a tuning range much lower than *VC02*. Whereas *VC03b* showed better performance in terms of FTR, with slightly bad phase noise. So phase noise is still an issue to solve concerning this proposed SWO design.

The FTR of the presented *VC03b* is comparable with state-of-the-art, as power consumption of presented design is lower than *VC02* and less than other compared references. The output power is low as compared to [10], [11], [15], [16], [21] and [22]. The needed improvement is in *PN* performance as it is higher than [10], [11], [16], and *VC02* presented in chapter3. Due to higher phase noise, the overall performance in terms of  $FOM_T$  is slightly better than *VC02*, however  $FOM_T$  of *VC03b* is much better as compared to only [10], [11]. So, phase noise is still an issue to solve with the proposed topology of phase shifter based oscillator, i.e. SWO.

<i>VCOs</i>	$P_{dc\_core}$ (mW)	<i>FTR</i> (%)	$P_{out}$ (dBm)	$F_o$ (GHz)	<i>PN</i> (dBc/Hz) (Best <i>PN</i> )	$FOM_T$ (dBc/Hz)
[10]	15.81	6.3		76.5	-109 @ 10MHz	-170.6
[11]	14.3	6.3	-4.5	76.5	-109 @ 10 MHz	-171.1
[11] post fabrication	14.3	15.8	-4.5	76.5	-108.4 @ 10MHz	-178.5
[15]	27	20	-4	40	-96 @ 1MHz (worst) -100.2 @ 1MHz (best)	-179.2 -183.9
[16]	33	14	-0.5	81.5	-97.3 @ 1MHz (best)	-182.6
[21]	8.4 to 10.8	41		73.8	-104.6	-184.2
[22]	15	17	-4.9	56	-89.8 @ 1MHz (worst) -99.4 @ 1MHz (best)	-177.4 -186.8
<i>VC02</i>	7.2	6.3	0.55	83	-89.2 @ 1MHz -113.3 @ 10MHz	-175 -179.2
<i>This Work</i> ( <i>VC03b</i> )	3.12	7.52	-7.7	82.4	-85.4 @ 1MHz -106 @ 10MHz	-176.3 -177

Table 4.19: State-of-the-art comparison

The layout of SWO is shown in Figure 4.14. It occupies  $560 \mu\text{m} \times 654 \mu\text{m}$  including RF and DC pads.

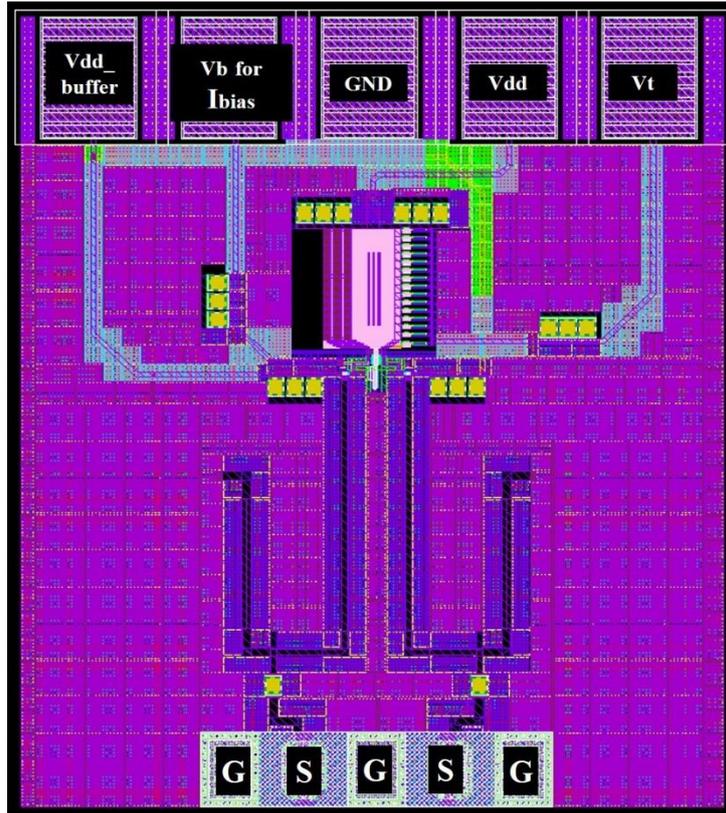


Figure 4.14: Layout of SWO with S-CPS based phase shifter as resonator (VCO 3)

### 4.3 Conclusion

With the new topology proposed in this chapter, i.e. SWO based on phase shifter as resonator, the performance has improved in terms of tuning range. This is due to the use of S-CPS as phase shifter for tuning the frequency of oscillator. But the major disadvantage is in terms of phase noise, as it can be improved only at the cost of smaller  $FTR$ .

Hence, even though with the improved design topology, i.e. distributing the losses throughout the resonator, we obtained a good performance SWO, but not an extraordinary one. So, a new design topology is studied and proposed to improve SWO performance in next chapter 5. It is based on periodically compensating the losses (distributed SWO) and improving all the performance parameter of SWO, i.e.  $FTR$ , Power consumption, output power.



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## 5. DISTRIBUTED STANDING WAVE OSCILLATOR FOR E-BAND APPLICATION

### 5.1 Introduction to Standing-wave oscillators (SWO)

As discussed in chapter 1 (section 1.3.1), among several VCO topologies proposed in literature a dominant class of mm-wave oscillators relies on lumped  $LC$  resonators. However due to the limitations on device parasitics most of the high frequency  $LC$ -tank VCOs suffer from an inadequate  $FTR$ . Although wave-based oscillator seems to be a good solution to fulfill certain design criteria [1], i.e. higher  $FTR$ ,  $F_{osc}$  and better phase noise performance, the proposed VCO design (also called Standing Wave Oscillator) in chapter 4, showed good performance in terms of phase noise when smaller varactors were employed to design the resonator (section 4.2.3, step 6 to 8), however the  $FTR$  was limited due to added parasitic capacitance from CCP and output buffer. So, in order to increase the  $FTR$  bigger varactors were employed, which rather lead to increment in overall losses of the resonator, hence resulting in higher phase noise.

So, the proposed architecture in [2]-[4] reduces the loading effect due to proper distribution of active gain ( $g_m$ ) elements for loss compensation and hence demonstrating great potential for wide-band applications at mm-wave frequencies. As this topology is based on the wave behavior of transmission line, it allows adding slow-wave effect, hence leads to improved  $Q$ -factor (as mentioned in chapter 3, section 3.1).

Hence, there exists a great motivation for utilizing wave-based oscillators as it provides wider  $FTR$  due to distributed loading effect, reduced phase noise due to improved  $Q$ -factor of resonator and also the alleviated  $F_{osc}$  towards cutoff frequency ( $F_t$ ) of the device. In section 5.2, a distributed standing wave oscillator (D-SWO) has been proposed with all these improved performance parameters. Nevertheless this structure consumes high DC power because it includes several  $g_m$  cells and the output power swing is low as well.

Moreover, in all the SWOs proposed in the last decade, as for VCOs based on other topologies, a buffer is needed to convert high output impedance of VCO core to  $50\ \Omega$ , most of the time for measurement purposes [1]-[7]. Many drawbacks are linked to the use of output buffers: (i) large costly area, (ii) increase of power consumption and decrease of output power, and, even the most important at mm-waves, (iii) decrease of the tuning range due to the effect of added parasitic capacitance, which cannot be de-embedded. So, to address these critical criteria, a new topology is proposed in section 5.3, providing low power consumption and higher output power swing, i.e. good power efficiency is targeted,  $P_{eff} = P_{out} / P_{dc\_total}$ . The operating principle and design of the proposed buffer less distributed SWO is explained in section 5.3.1 and 5.3.2, respectively.

Hence, in order to circumvent the drawbacks of current SWOs mentioned in literature, two main innovations are presented in this chapter (section 5.2 and 5.3). First, slow-wave coplanar striplines (S-CPS) are used instead of microstrip lines; S-CPS exhibit higher  $Q$ -factor and lead to reduced size, thanks the slow-wave effect [8]. Moreover, a new tunable S-CPS concept is used: the S-CPS is periodically loaded by varactors, leading to the concept of tunable quarter-wavelength resonator (also mentioned in chapter 4). Second, thanks to a

careful choice of the output position, output buffers are no longer needed, leading to wide tuning range and low power consumption.

Please note that the phase shifter utilized in this chapter for designing distributed SWOs (with and without buffer) are having same topology as utilized in chapter 4, i.e. unsymmetric S-CPS based phase shifter. Only the design parameters, i.e. width, gap, and respective metal layers are changed.

### 5.1.1 Design purpose & operating principle of distributed SWO

Among all the proposed topologies of VCOs, distributed SWO topology was proposed in the last decade in order to improve the frequency tuning range (*FTR*), output power and phase noise [2] – [5]. It is based on the concept of utilizing transmission line as a half- or quarter-wavelength resonator and periodically loaded by cross-coupled pairs (CCPs) and tunable components, e.g. varactors in CMOS/BiCMOS technologies. Based on microstrip line, the topologies proposed in [1] – [3] exhibit poor *Q*-factor. Moreover, low loss-compensation ability is achieved since varactors are positioned at the same position as the CCPs. Using slow-wave effect with distributed SWO topology allows improving the performance mainly in terms of *FTR* and phase noise.

**Operating Principle:** The distributed SWO is based on a tunable quarter-wavelength resonator, i.e. terminated by a short and open circuits at near and far-ends. Figure 5.1 shows the 3D topology of the tunable quarter-wavelength resonator exhibiting an electrical length of  $90^\circ$  at the center frequency  $f_0$ . As mentioned before in this chapter the considered transmission line is S-CPS demonstrating a high-quality factor (i.e.  $\sim 30$ ) as compared to classical  $\mu$ strip lines (less than 20). The resonance frequency, which corresponds to the VCO oscillating frequency, is tuned by changing the electrical length of the resonator, i.e. by tuning the varactors, as for a classical VCO tank.

In traditional implementation of distributed SWO, the varactors are placed in parallel with the CCPs [2] or at the center of the line [3]. The use of a phase shifter allows distributing the varactors all along the resonator length. Thus, the loading effect of the varactors is well distributed and its effect is well compensated. Moreover, small varactors are used which reduces parasitic effects allowing reduction in resonator losses and parasitic capacitances. In our implementation, varactors are distributed all along the resonator length, as shown in Figure 5.1.

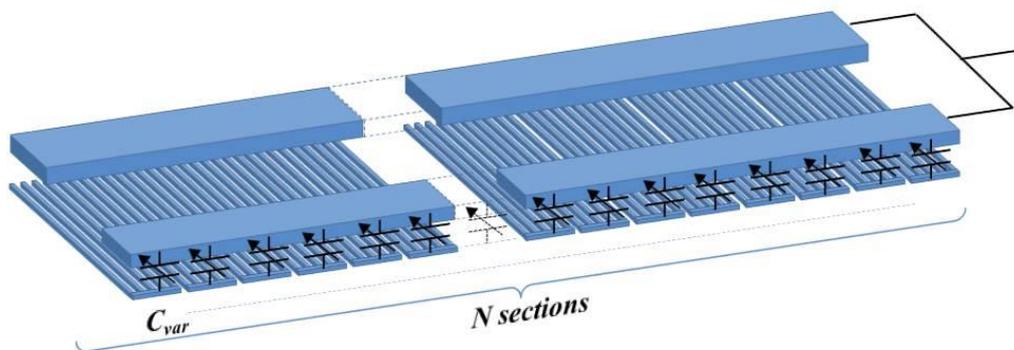


Figure 5.1: Tunable quarter-wavelength resonator based on S-CPS periodically loaded by varactors  $C_{var}$

The concept of distributed SWO says that the losses of the resonator must be compensated periodically, i.e. by distributing the CCPs all along the resonator.

As shown in Figure 5.2 the distributed SWO is obtained by distributing the CCPs all along the tunable resonator for compensating the losses locally (let us notice that the number of CCPs can be different from the number of varactors). The size of the CCPs depends on the compensation factor and the start-up condition which are derived in [2], also mentioned in section 5.1.2.

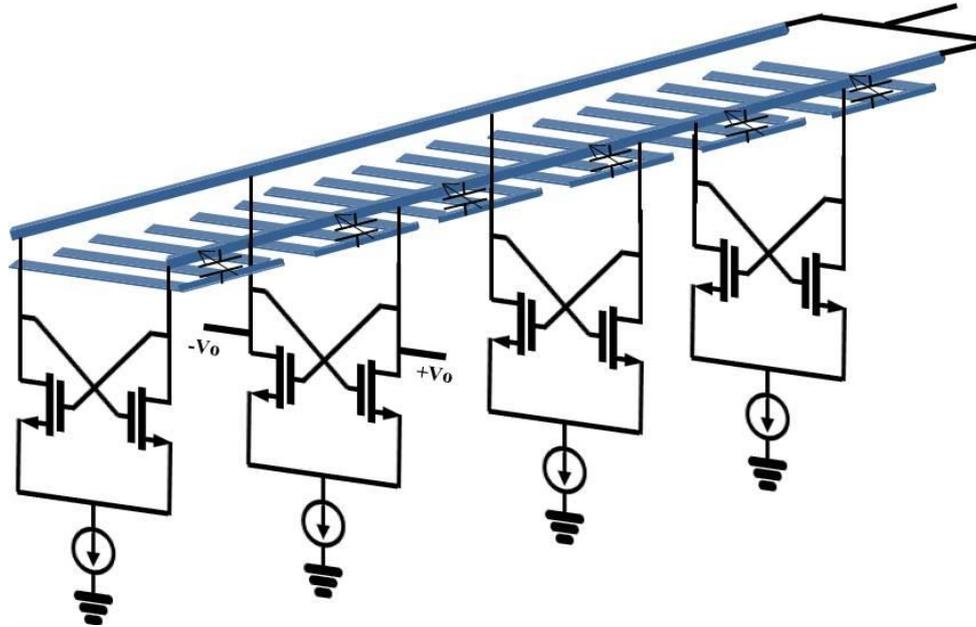


Figure 5.2: Circuit topology of distributed SWO based on the tunable S-CPS based resonator topology of Figure 5.1

### 5.1.2 Oscillation frequency, start up conditions and loss estimation

Figure 5.3 shows the lumped equivalent model of loaded transmission line.  $R$  and  $L$  represent the series resistive losses in ( $\Omega/m$ ) and series inductance in ( $H/m$ ), respectively, and  $G$  and  $C$  represents the conduction losses in ( $S/m$ ) and coupling capacitance between conductors in ( $F/m$ ), respectively.  $G_d$  and  $C_d$  correspond to the equivalent per unit length trans-conductance and capacitance contributed by cross-coupled inverters.

Hence, the characteristic impedance  $Z_0$  and propagation constant  $\gamma$  of loaded transmission lines are given by [2],

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega(C + C_d)}} \quad (5.1)$$

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C + j\omega C_d)} \quad (5.2)$$

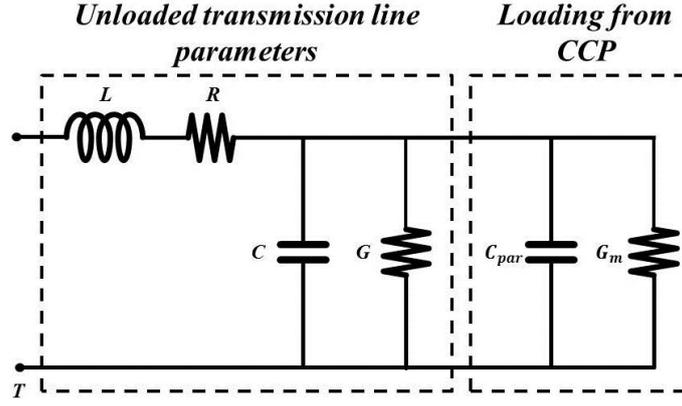


Figure 5.3: Lumped equivalent circuit of the loaded transmission line [2]

By applying the low-loss approximation [9]  $Z_0$  and  $\gamma$  can be expressed as,

$$Z_0 = \sqrt{\frac{L}{C + C_d}} \quad (5.3)$$

$$\gamma = \alpha + j\beta \approx \frac{1}{2} \left( \frac{R}{Z_0} + Z_0 G \right) + j\omega \sqrt{(C + C_d)} \quad (5.4)$$

In the distributed SWO, the several trans-conductance cells (i.e. cross-coupled inverters) are utilized to compensate for the losses of the transmission lines. To derive the start-up conditions for the oscillator, the attenuation constant  $\alpha$  in above equation (5.4) can be modified by introducing a negative conductance ( $-G_d$ ),

$$\alpha \approx \frac{R}{2Z_0} + \frac{(G - G_d)Z_0}{2} \approx \frac{R}{2Z_0} - \frac{G_d Z_0}{2} \quad (5.5)$$

Thus, for evaluation of the oscillation start-up, the compensation factor  $LCF$  can be defined in first approximation as,

$$LCF = \frac{G_d Z_0 / 2}{R / 2Z_0} = \frac{G_d Z_0^2}{R} \quad (5.6)$$

The line losses can be fully compensated to initiate the oscillation as long as  $LCF$  is larger than unity. For practical circuit designs,  $LCF$  is typically chosen between 3 and 5 to tolerate the process variation.

The oscillation frequency of the SWO is given by,

$$f_{osc} = \frac{v_p}{\lambda} \quad (5.7)$$

where,  $v_p$  is the phase velocity given by,

$$v_p = \frac{1}{\sqrt{L(C + C_d)}} \quad (5.8)$$

and  $\lambda$  is the equivalent wavelength depending on the physical length of resonator i.e. for half-wavelength resonator

$$l = \frac{\lambda}{2} \quad (5.9)$$

So, equation (5.7) allows obtaining the oscillation frequency for half-wavelength resonator

$$f_{osc} = \frac{v_p}{\lambda} = \frac{1}{2l\sqrt{L(C + C_d)}} \quad (5.10)$$

Similarly, for quarter-wavelength resonator,

$$l = \frac{\lambda}{4} \quad (5.11)$$

and the oscillation frequency for quarter-wavelength resonator is

$$f_{osc} = \frac{v_p}{\lambda} = \frac{1}{4l\sqrt{L(C + C_d)}} \quad (5.12)$$

Eq. (5.6) also provides useful design insights for the circuit optimization. The idea is to determine the needed transconductance per unit length (i.e.  $G_d$  ( $S/m$ )) based on the 2-port parameters of the transmission line (i.e.  $Z_0$  ( $\Omega$ ),  $R_S$  ( $k\Omega/m$ ) and  $LCF$  (compensation factor)), refer eq. (5.6). Based on the value of compensation factor ( $LCF$ ) transconductance per unit length is determined, i.e.  $G_d$  ( $S/m$ ), refer eq. (5.13).

$$G_d = \frac{\eta R}{Z_0^2} (S/m) \quad (5.13)$$

The number of CCPs is then chosen so as the distance between two CCPs is  $\leq \lambda / 10$  [2]. This length of each section is then multiplied with  $G_d$  ( $S/m$ ), to determine the needed transconductance  $G_D(S)$  of CCP for each section, refer eq. (5.14).

$$G_D = \frac{\eta R}{Z_0^2} \times l_{1-section}(S) \quad (5.13)$$

In section 5.1.2 a brief summary of above described methodology will be given.

### 5.1.3 Followed design methodology

The followed methodology for designing the SWO is given by flow diagram shown in Figure 5.4.

1. In the first step a phase shifter is designed based on the methodology decided in Chapter 4 (section 4.2.1).
2. Then in second step based on the resistive losses, characteristic impedance (obtained from transmission line parameters, i.e. ABCD parameters) of phase shifter and needed compensation factor, the per unit length transconductance  $G_d$  ( $S/m$ ) is determined
3. In this step, the number of SWO sections is determined based on the fact that length of each section of SWO must be  $\leq \lambda / 10$  [2].
4. Based on the length of each section of SWO, the required transconductance  $G_D(S)$  for each section is computed.

5. Parasitic capacitance added transconductance and buffers are modelled in this step.
6. This step is a decision state, i.e. due to added parasitic capacitance from cross-coupled pair the oscillation frequency of SWO gets shifted to lower frequency. Hence, in this step if the oscillation frequency of SWO is very much lower to the targeted frequency, then in step 6a the length of phase shifter has to be reduced. This step 6a is followed by repetition from step 2 to step 6 till the targeted oscillation frequency is obtained.

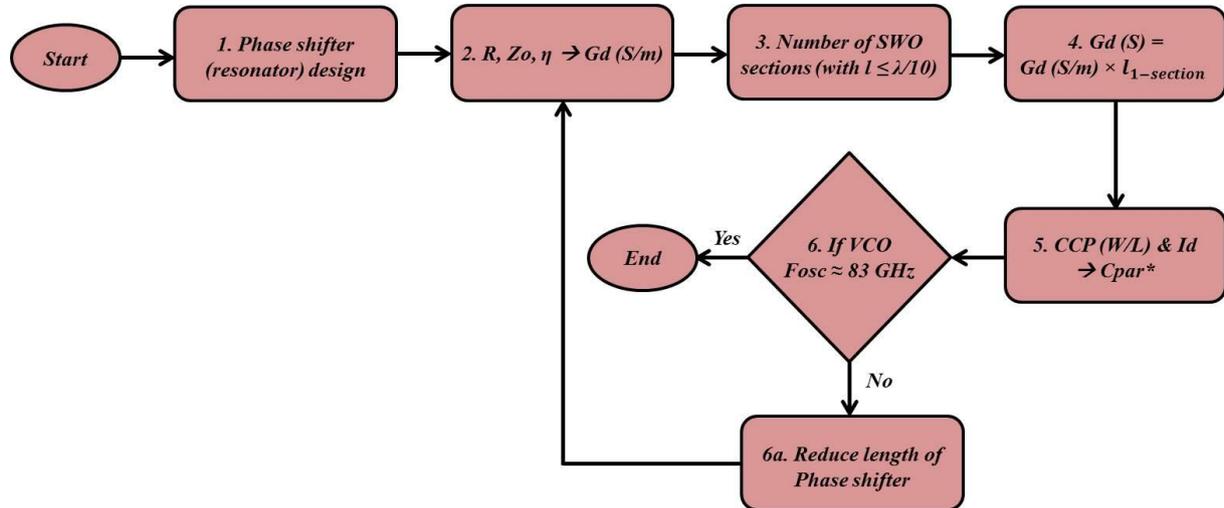


Figure 5.4: SWO design flow diagram  
 (\*Cpar of buffer has been included as well, refer chapter 2 (section 2.3.2))

Following the same methodology the distributed SWO design is presented in section 5.2.

## 5.2 Designed standing wave oscillators with phase shifter as resonator

In this section a distributed SWO design is presented, following the design methodology discussed in section 5.1.3.

### 5.2.1 Phase Shifter design and proposed distributed SWO

The stepwise process for designing phase shifter is as follows,

Step 1: The chosen dimension of unsymmetric S-CPS based phase shifter is given in Table 5.1.

Dimension of unsymmetric S-CPS		Metal layer
$W_1$	10 $\mu\text{m}$	M8 – M6
$W_2$	5 $\mu\text{m}$	M8
$G$	20 $\mu\text{m}$	
<b>Fingers (SS = SL)</b>	0.6 $\mu\text{m}$	M4

Table 5.1 : Chosen dimen of unsymmetric S-CPS

(b) No. of fingers per group = 5; No. of groups = 18; Length of phase shifter = 108  $\mu\text{m}$  (this design has been started with less number of groups, i.e. with a smaller electrical length, because as expected due to added parasitics from cross-coupled pairs and output buffer, the electrical length of the phase shifter will be increased. So, after retro simulations 18 groups were finalized for designing the SWO).

Step 2 & 3: As per evaluated inductance ( $L$ ), capacitances ( $C_{S1}$ ,  $C_{S2}$  and  $C_{eq}$ ) the evaluated/ needed varactor capacitance specification is given in Table 5.2.

$C_{v\_min}$	3.9 fF
$C_{v\_max}$	5.4 fF
$T.R. = C_{v\_max}/C_{v\_min}$	1.4

Table 5.2 : Evaluated varactor capacitance and tuning range

The evaluated tuning range of varactor in Table 5.2 is low, however increment in tuning range of varactor is needed as the added parasitic will lead to reduction in FTR of distributed SWO.

Please note that even though distributed loading effect is anticipated in distributed SWO topology, still we choose to have a bigger varactor. It is due to the fact that the fundamental of distributed SWO design proposed in this section is to increase FTR. Hence, following specifications of varactor (with higher tuning range) has been chosen from starting of the design, as referred in Table 5.3.

Dimension of varactor		Electrical characteristics of Varactor	
Width	1.7 $\mu\text{m}$	$C_{vmax}$	7.2 fF
Length	0.38 $\mu\text{m}$	$C_{vmin}$	2.9 fF
No. of fingers	1	$T.R. = C_{vmax}/C_{vmin}$	2.5
nbcells	2	$Q_{min}$	9.7

Table 5.3: Varactor specifications and electrical characteristics

Step 4: The RLRC model of phase shifter is given in Table 5.4

$R_S$	0.14 $\Omega$
$L_S$	5.63 pH
$C_{S1}$	3.33 fF
$C_{S2}$	0.83 fF
$R_f$	0.26 $\Omega$

Table 5.4: Equivalent RLRC model

Step 5: Hence, the electrical characteristics of the phase shifter are given in Table 5.5, for a physical length of 108  $\mu\text{m}$ .

$Vt(V)$	0	2.4
$S_{21}^\circ$	-63.5	-56.8
$Z_c (\Omega)$	50.8	57.9
$\alpha (Np/m)$	391	313
$\alpha (dB/mm)$	3.4	2.7
$\epsilon_{reff}$	34	25.8
$Q_{ps}$	12.5	13.6
$R_S (\Omega/mm)$	19.9	18.16

Table 5.5: Electrical characteristic of phase shifter

Step 6: As mentioned above, the flow to design phase shifter is same as the one given in chapter 4 (section 4.2.3) up to step 6. Then, from step 6 given in section 4.2.3, i.e. step for loss estimation, the design method of this phase shifter varies. Hence a new flow diagram is given in this section, as shown in Figure 5.5.

As shown in Figure 5.5, the losses are estimated in step 6 using eq. (5.13). Based on the chosen length of each section the number of CCPs is decided. Based on  $W/L$  of CCP the

added parasitic capacitance is computed in addition to the parasitics added by two output buffers.

Therefore, the estimated losses of phase shifter are given in Table 5.6, for  $LCF$  of 6. Please note that the considered  $LCF$  is higher for distributed SWO design because smaller  $LCF$  (say 3) leads to smaller  $G_d$  ( $S/m$ ) and hence size of CCPs will be smaller that does not allow to vary  $LCF$  beyond a fixed value. Hence in order to have flexibility to vary  $LCF$ , a higher value of  $LCF$  is chosen.

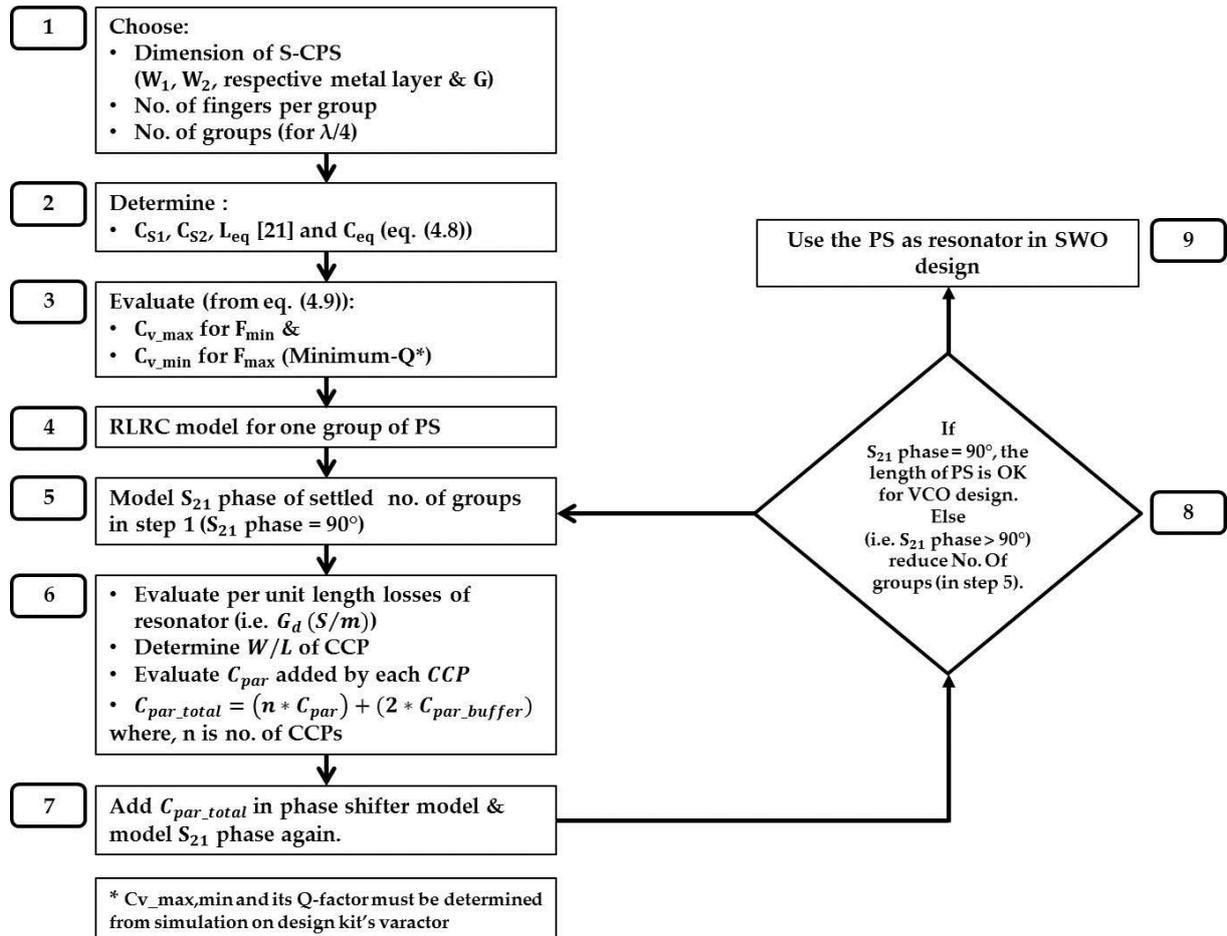


Figure 5.5: Flow diagram for phase shifter and SWO design

So referring to Table 5.6, the maximum needed transconductance is 46.3 S/m to compensate for the losses. As mentioned before in this chapter the number of CCPs is chosen so as the distance between two CCPs is lower than  $\lambda / 10$  [2]. Hence, 4 CCPs are employed in this design each with transistors width and current of 6.5  $\mu\text{m}$  and 2.8 mA, respectively, leading to a transconductance of 1.4 mS and a parasitic capacitance of ( $C_{par}$ ) 7.7 fF, also given in Table 5.7.

As mentioned in step 1 of this design flow, considering the loading capacitance added by CCPs and output buffers, the number of sections of the phase shifter is chosen equals 18 (after retro simulation) to achieve 90° phase-shifter electrical length at  $f_0$ , leading to a total physical length of 108  $\mu\text{m}$  for the resonator. However, the length of one section with 5 fingers is 6  $\mu\text{m}$  and it is not possible to position the CCPs on equal distance along the resonator. Hence, the CCPs are distributed as shown in Figure 5.6.

Please note that even though the length of alternate section varies with the other by 20%, refer Figure 5.6, still same CCPs are being used for compensating losses of all sections. This is due to the fact that for 24  $\mu\text{m}$  sections the needed transconductance is 1111  $\mu\text{S}$ , leading to need of  $R_{negative} = -900 \Omega$ , so the needed CCP will be smaller and hence, the LCF variation will be less flexible.

OFF ( $V_t = 0 \text{ V}$ )	ON ( $V_t = 2.4 \text{ V}$ )
$G_d = 46.3 \text{ S/m}$	$G_d = 32.4 \text{ S/m}$
$G_D = 1389 \mu\text{S}$	$G_D = 972 \mu\text{S}$
$R_p = \frac{1}{G_D} = 720 \Omega$	$R_p = \frac{1}{G_D} = 1028 \Omega$

Table 5.6: Loss estimation of the resonator

$R_{negative} (\Omega)$	-691 to -573
nMOS cross-coupled pair	$W = 6.5 \mu\text{m}; L = 0.06 \mu\text{m}; Nf = 5$
Bias current (mA)	1.7 to 2.8
$C_{par} (fF)$	7.5 to 7.8
$C_{par\_buffer} (fF)$	$7 * 2 = 14$

Table 5.7: Design parameters of CCP

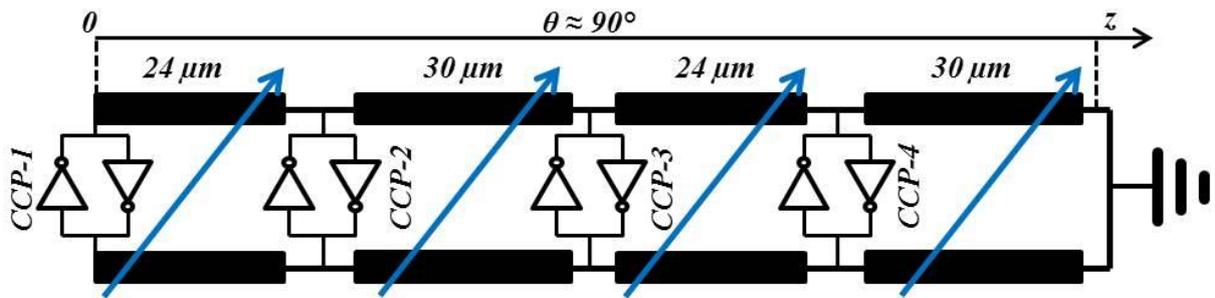


Figure 5.6: Circuit topology of distributed SWO

Step 7 & 8: In step 7 the modeled parasitics are added with the chosen length of the phase shifter (i.e. 108  $\mu\text{m}$ ) and then the S21 phase of resonator is modeled. In step 8 as the modeled S21 phase is about  $90^\circ$ , the number of groups in phase shifter is kept unchanged.

Step 9: Finally in this step the distributed SWO is simulated. Similar to previously designed oscillators, all three different simulations are done, i.e. S-parameter, transient and harmonic balance simulations.

In Table 5.8, the post layout simulation (PLS) of distributed SWO is given. On comparing all the three performed simulations, the performance is similar with a tuning range. Also, the output power is almost the same as obtained from transient and harmonic balance simulation. Hence, a tuning ratio varying from 10.4% to 9.5% is obtained for a current from each current source varying from 1.7 mA (at  $V_b = 0.6 \text{ V}$ ) to 2.8 mA (at  $V_b = 0.7 \text{ V}$ ), so the total power consumption varies from 8.2 mW to 13.4 mW, respectively. Hence, the maximum power consumption of SWO is 1 mW higher than VCO3 and 6 mW higher than VCO2. Let us remember that this increase of power consumption allows greatly improving the tuning ratio as compared to VCO2 and VCO3 exhibiting a FTR of only 6.3%. In Table 5.8(c) the both worst and best possible PN is presented, i.e. -85.7 to -91 dBc/Hz at 1MHz offset and -106 dBc/Hz to -112.2 at 10 MHz offset, respectively. Finally, the main improvement is in

terms of tuning ratio as expected from the topology. Hence, for distributed SWO the best possible  $FOM_T$  is -177.6 dBc/Hz at 1MHz offset and -178.5 dBc/Hz at 10 MHz offset.

<i>Simulation</i>	$V_b(V)$	$V_t(V)$	$F_{osc}(GHz)$	$FTR (GHz/\%)$
<i>S-parameter</i>	0.6	0	75.6	8.1/ 10.2
		2.4	83.7	
	0.7	0	75.4	7.9/ 10
		2.4	83.3	

(a)

<i>Simulation</i>	$V_b(V)$	$V_t(V)$	$F_{osc}(GHz)$	$FTR (GHz/\%)$	$V_{out}(V)$
<i>Transient</i>	0.6	0	75.7	8.3/ 10.4	0.1
		2.4	84		0.24
	0.7	0	75.7	7.6/ 9.6	0.2
		2.4	83.3		0.33

(b)

<i>Simulation</i>	$V_b(V)$	$V_t(V)$	$F_{osc}(GHz)$	$FTR (GHz)$	$V_{out}(V)$	$PN (dBc/Hz)$	$FOM_T (dBc/Hz)$
<i>Harmonic balance</i>	0.6	0	75.84	8.3	0.094	-83.4 to -88.4 @ 1MHz	-177.6
		2.4	84.14		0.227	-104.3 to -109 @ 10MHz	-178.2
	0.7	0	75.57	7.6	0.183	-85.7 to -91 @ 1MHz	-177.3
		2.4	83.13		0.316	-106.5 to -112 @ 10MHz	-178.5

(c)

Table 5.8: (a) S-parameter; (b) Transient and (c) Harmonic balance simulation

### 5.2.2 Comparison with state-of-the-art

Table 5.9 gives a brief comparison of proposed distributed SWO (D-SWO) with state-of-the-art.

On comparing with state-of-the-art, the proposed design can be compared to [3], [10]-[12], as they have oscillation frequency around 80 GHz. The FTR of proposed design is better than [10] and [11] and slightly lower than [3] and [12]. However the power consumption of proposed design is lower as compared to [3], [10] and [11] and slightly higher to [12]. Please note that even though the power consumption is minimal in proposed D-SWO design, the output power is higher as compared to [3], [10]-[12], i.e. the power efficiency of the proposed design is better as compared to state-of-the-art. Similarly,  $PN$  has improved as compared to [10]-[12] due to better  $Q$ -factor and output power, but higher as compared to [3]. Hence, the overall performance in terms of  $FOM_T$  has improved [10], [11] but did not go higher than [3] and [12]. The targeted improvement in terms of  $FTR$  has been achieved on comparing with previously designed/ proposed oscillator designs, i.e. VCO2 and VCO 3, in this thesis.

VCOs	$P_{dc\_core}$ (mW)	FTR (%)	$P_{out}$ (dBm)	$F_o$ (GHz)	PN (dBc/Hz) (Best PN)	$FOM_T$ (dBc/Hz)
[2]	27	20	-4	40	-96 @ 1MHz (worst) -100.2 @ 1MHz (best)	-179.2 -183.9
[3]	33	14	-0.5	81.5	-97.3 @ 1MHz (best)	-182.6
[10]	15.81	6.3		76.5	-109 @ 10MHz	-170.6
[11]	14.3	6.3	-4.5	76.5	-109 @ 10 MHz	-171.1
[11] post fabrication	14.3	15.8	-4.5	76.5	-108.4 @ 10MHz	-178.5
[12]	8.4 to 10.8	41		73.8	-104.6	-184.2
[13]	15	17	-4.9	56	-89.8 @ 1MHz (worst) -99.4 @ 1MHz (best)	-177.4 -186.8
VCO2	7.2	6.3	0.55	83	-89.2 @ 1MHz -113.3 @ 10MHz	-175 -179.2
VCO3	10.3	6.3	0.21	79.5	-86 @ 1MHz -108 @ 10MHz	-170 -172
<b>This work D-SWO</b>	13.4	9.6 to 10.4	0	79.4	-91 @ 1MHz -112.2 @ 10MHz	-177.3 -178.5

Table 5.9 : Comparison with state-of-the-art

## 5.3 Buffer less E-band SWO

### 5.3.1 Operating principle of distributed buffer less SWO

Essentially, the buffer is needed in an oscillator design for measurement purpose only i.e. to convert high output impedance of VCO core to  $50 \Omega$ . While utilizing the oscillator in a transmitter or receiver system, we only need a matching network. So, the idea is to overpass the limitation of tuning ratio, output power and excess power consumption added by buffer. Also, due to this flexibility in choosing the output impedance, we do not need a matching network in a system design. Thanks to the position dependent voltage and current amplitude variations of quarter-wavelength Standing Wave resonator [1], shown in Figure 5.7, the optimum output impedance can be chosen along the resonator length.

Hence, as mentioned in introduction of this chapter as well in order to overcome the drawbacks of distributed SWOs mentioned in literature, a buffer less D-SWO design is presented in this section with reduced power consumption and improved power efficiency. Please note that in proposed buffer less D-SWO design the targeted output impedance is  $50 \Omega$  due to the impedance of measurement probe. Moreover, the proposed buffer less D-SWO can be used in a fully integrated circuit, as it simplifies the design of the matching network needed for the connection with other parts, since any real output impedance can be realized. So, the innovation in this design is linked to the flexibility of choosing the output impedance of the oscillator core design.

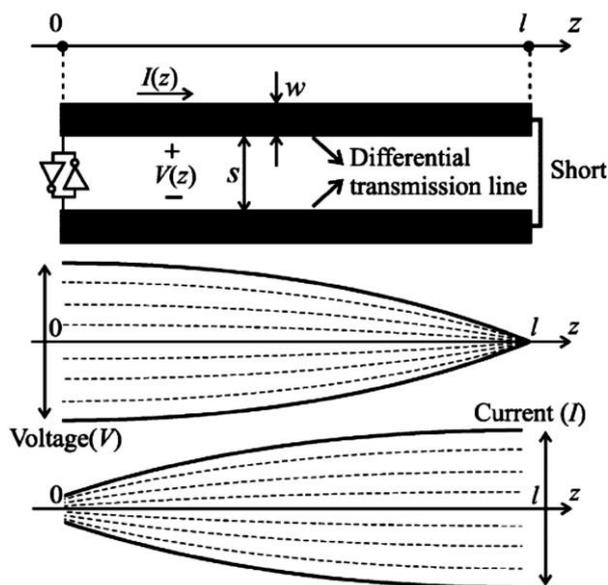


Figure 5.7:  $\lambda/4$  standing wave oscillator (SWO) and position dependent voltage-current standing wave amplitudes at the fundamental mode ( $l = \lambda/4$ ) [1]

The buffer less D-SWO is also based on same tunable quarter-wavelength resonator, as utilized in section 5.2.1. In fact the whole circuit is same as D-SWO presented in section 5.2.1. Such topology allows choosing the optimum output impedance because at open circuit the local impedance is very high (ideally infinite) and zero at short circuit [1]-[5].

In case of the buffer less oscillator design, regardless of CCPs position, the output can be taken from any position of the resonator as the losses are compensated periodically. The circuit topology of buffer less D-SWO is shown in Figure 5.8. As mentioned before, the choice of output position depends on the needed output impedance i.e.  $50 \Omega$  in our case. This output impedance variation along the length of D-SWO is determined by load pull simulation technique, explained in the next section 5.3.2. This taped-line coupling feeding is commonly used for bandpass filters I/O feeding [14].

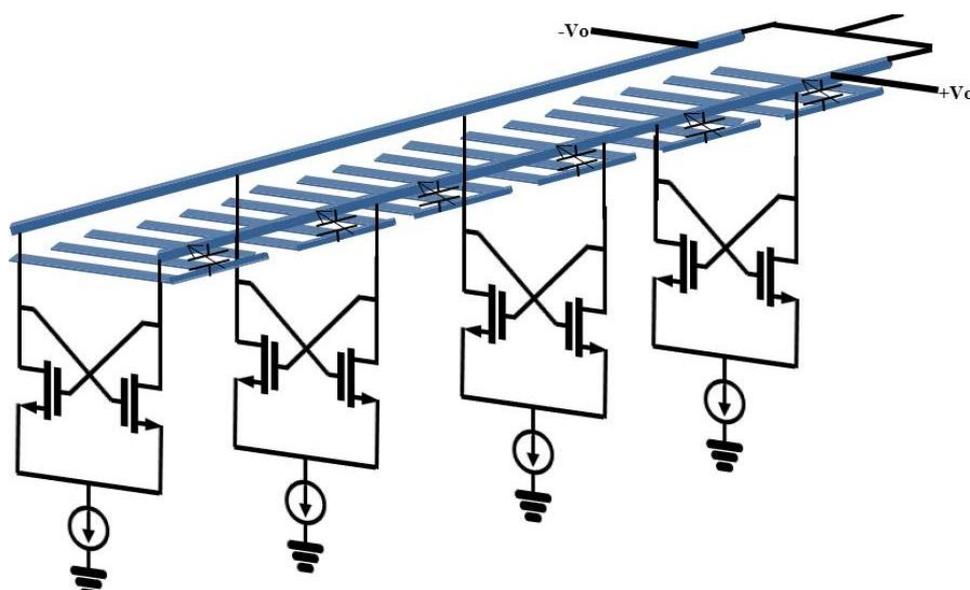


Figure 5.8: Circuit topology of buffer less D-SWO based on the tunable S-CPS based resonator topology of Figure 5.6 loaded by CCPs

### 5.3.2 Load pull simulation approach

In order to determine the optimal position along the length of SWO to match a 50- $\Omega$  load resistance, the load pull simulation has been done. It involves varying the load impedance presented to SWO and monitoring output power ( $P_{out}$ ), i.e. two steps are followed. First the load impedance across each section of the resonator was varied and second the  $P_{out}$  for each of the load impedance was determined; then, the best matching impedance was identified. The single port impedance variation from open to short circuit is from 600  $\Omega$  to 0  $\Omega$ , respectively. Figure 5.9 shows the voltage ( $V$ ), current ( $I$ ) and impedance ( $Z$ ) variation along the resonator, as determined by load pull simulations. This value of impedance ( $Z$ ) can also be obtained from the ratio of position dependent voltage ( $V$ ) and current ( $I$ ) obtained from the load pull simulation.

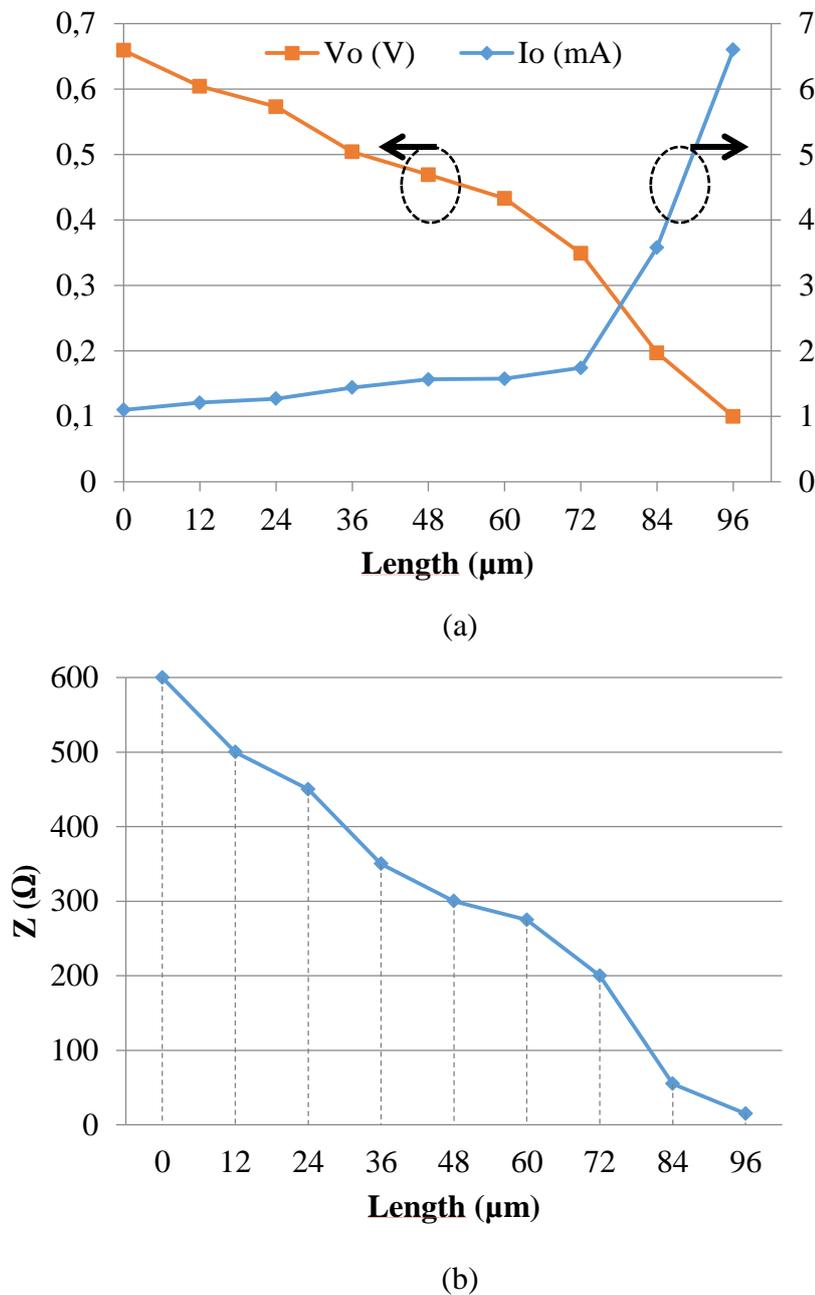


Figure 5.9: (a) Voltage ( $V$ ), Current ( $I$ ) & (b) Impedance ( $Z$ ) variation versus loaded resonator length

### 5.3.3 Simulated performance of Buffer-less Standing Wave Oscillator

In Table 5.10, the post layout simulation (PLS) of buffer less D-SWO is given. Hence, a tuning ratio varying of 11% is obtained for a current from each current source of 2.8 mA (at  $V_b = 0.7 V$ ), so the total power consumption is 13.4 mW. The buffer less D-SWO oscillates between 79.2 to 88.4 GHz. The maximum output power ( $P_{out}$ ) of 1.4 dBm can be achieved with total power consumption of 13.4 mW. In Table 5.10 both worst and best possible  $PN$  is presented, i.e. varying from -83.4 to -87.3 dBc/Hz at 1MHz offset and -104 to -110 dBc/Hz at 10 MHz offset, respectively. Hence, the best possible  $FOM_T$  for this buffer less D-SWO is -175.3 dBc/Hz at 1MHz offset and -178 dBc/Hz at 10 MHz offset.

<i>Simulation</i>	$V_b$ (V)	$V_t$ (V)	$F_{osc}$ (GHz)	$FTR$ (GHz/ %)	$V_{out}$ (V)	$PN$ (dBc/Hz)	$FOM_T$ (dBc/Hz)
<b>Harmonic balance</b>	0.7	0	79.2	9.2 (11%)	0.15	-83.4 to -87.3@ 1MHz	-175.3
		2.4	88.4		0.37	-104 to -110 @ 10MHz	-178

Table 5.10: Harmonic balance simulation

A brief comparison with state-of-the-art has been given Table 5.11, in addition to the comparison with other topologies presented in this thesis.

### 5.3.4 Comparison with state-of-the-art

In comparison with state-of-the-art (see Table 5.11), the achieved  $P_{out}$  is the highest one with the lowest power consumption, since no output buffer is needed. Hence the achieved power efficiency (i.e.  $P_{eff} = P_{out}/P_{dc\_total}$ ) of the proposed design is higher as well.

<i>Ref</i>	$F_o$ (GHz)	$TR$ (GHz)	$P_{out}$ (dBm)	$P_{dc\_total} = P_{dc\_core} + P_{dc\_buffer}$ (mW)	$PN@1MHz$ (dBc/Hz)	$P_{eff}$	<i>Area</i> (mm <sup>2</sup> )
[2]	40	7.5	-4	27 + 15	-100.2	0.01	0.62
[3]	81.5	11	-0.5	33 + 3	-97.3	0.02	0.34
[13]	56	9.3	-4.9	15 + 9.6	-99.4	0.01 3	0.98
[15]	60.8	10.3	-30	19.1 + 0	-93.5	5. 10 <sup>-5</sup>	0.34
<b>VCO2</b>	83	5.3	0.4	7.2 + 11	-89.2 @ 1MHz -113.3 @ 10MHz	0.06	0.39
<b>VCO3</b>	79.5	5	1.12	10.3 + 11	-86 @ 1MHz -108 @ 10MHz	0.06	0.37
<b>D-SWO</b>	79.4	7.6	0	13.4 + 11	-91 @ 1MHz -112.2 @ 10MHz	0.04	0.4
<b>This* work</b>	83.8	9.2	1.4	13.4 + 0	-87.3 @ 1MHz -110 @ 10MHz	0.10	0.18

Table 5.11 : Comparison with state-of-the-art

The achieved  $FTR$  of 9.2 GHz is comparable with [2], [3], [13] and [15]. The phase noise varies from -84 to -87 dBc/Hz at 1 MHz and from -104 to -110 dBc/Hz 10 MHz offset. The best simulated  $FOM_T$  is -176 at 1 MHz and -178 dBc/Hz at 10 MHz offset. The layout of

distributed SWO is shown in Figure 5.10, it occupies  $670 \mu\text{m} \times 600 \mu\text{m}$  including RF and DC pads. The layout of buffer-less distributed SWO is shown in Figure 5.11, it occupies  $450 \mu\text{m} \times 400 \mu\text{m}$  including RF and DC pads, which is the smallest one as compared to other proposed designs in state-of-the-art. Simulated results show high performance in power efficiency and overall area and good trade-off between tuning range & phase noise.

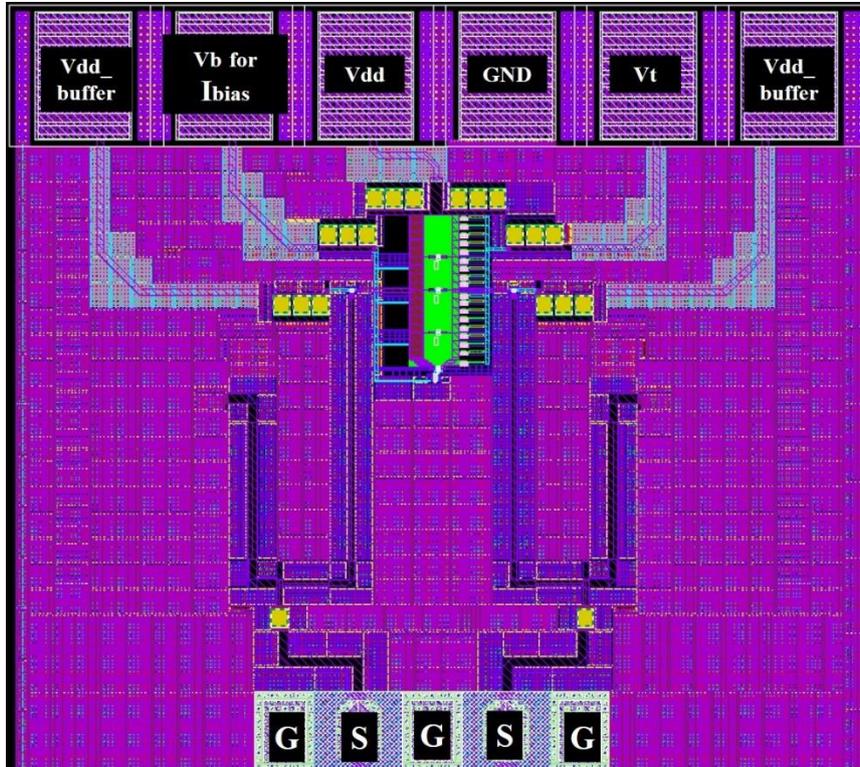


Figure 5.10: Layout of distributed SWO (VCO 4)

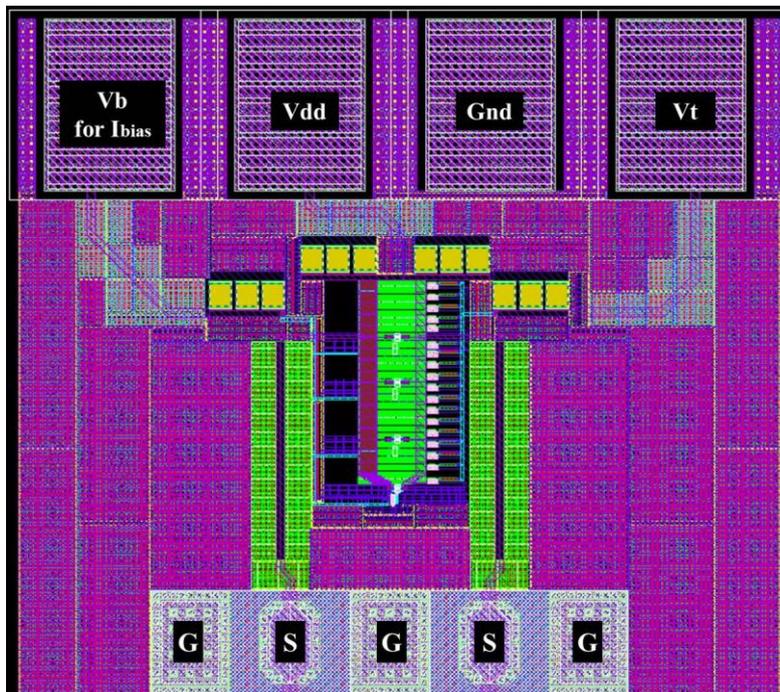


Figure 5.11: Layout of buffer less distributed SWO (VCO 5)

## 5.4 Conclusion

In this chapter, a VCO design based on the concept of distributed SWO was presented, with two major innovations. In the first part of this chapter, i.e. section 5.2, innovation is linked to the concept of utilizing a distributed loaded-line S-CPS phase shifter as a resonator to design the SWO. Indeed, by distributing the varactors uniformly over a high- $Q$  S-CPS, it offers low losses and hence improved performance of SWO has been achieved specifically in terms of frequency tuning range.

In the second part of this chapter, i.e. section 5.3, innovation is attributed to the fact that no output buffer is needed in the proposed design, due to the flexibility in choosing the output position along the length of SWO. This innovation leads to two merits: (a) a  $50\Omega$  output can be synthesized without any additional power consumption and (b) the size is reduced if a matching network is needed to connect the VCO to a mixer or another building block.

## 5.5 REFERENCES

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## GENERAL CONCLUSIONS

The demand for high performance circuits with low cost and better functionality keep increasing at millimeter-wave applications. This leads to new challenges for integrated circuit design, such as front-end transceiver, for several frequency bands and for several applications. For designing front-end transceiver a substantially good frequency synthesizer, i.e. PLL, is required. However for designing a variable PLL a voltage controlled oscillator is needed.

The work proposed in this thesis concerned the design and optimization of a key building block of front-end transceiver, i.e. voltage controlled oscillator (VCO), in BiCMOS 55 nm technology. The fundamental proposed in this thesis is to utilize high- $Q$  resonator in order to overcome the typical design issues of a VCO, i.e. reduced frequency tuning range ( $FTR$ ), high phase noise ( $PN$ ), high power consumption ( $P_{DC}$ ) and low output power ( $P_{out}$ ). Thanks to slow-wave effect, high- $Q$  resonator has been designed using slow-wave coplanar stripline (S-CPS). This high- $Q$  S-CPS based resonator has been then employed for designing VCO. A methodology was decided, which was kept common for all the presented VCO in this thesis.

In chapter 1, firstly a brief overview of the standard millimeter-wave application was given, followed by VCO design criteria. Secondly, the available VCO design topologies in literature were studied and compared. Finally, the reason for choosing the hybrid and distributed VCO topology i.e. standing wave oscillator (SWO), for this thesis was justified.

In chapter 2 the VCO design methodology was defined thoroughly, that has been followed throughout this thesis. Before proceeding for VCO design, the characteristics of the inductor, varactor, and nMOS transistor from the BiCMOS 55 nm technology were studied. These characteristics gave insight of choosing the design elements value as per needed oscillation frequency. Also a loss estimation method was discussed, that has been kept common for all VCO designs. For analyzing the circuit behavior the variation in tank  $Q$ -factor versus various  $LC$  combinations has been done as well. A resistive interconnect modelling has been discussed, that is needed while designing the layout of VCO. In order to make fair comparison with proposed hybrid and distributed VCO in later chapters, a conventional  $LC$ -tank VCO was designed and presented in this chapter. Finally from simulated performance of conventional VCO design the constraints concerned with lumped  $LC$ -tank VCO were explained.

To ameliorate the design issues of  $LC$ -tank VCO, in chapter 3 the lumped inductor was replaced by high- $Q$  differential slow-wave transmission line, i.e. S-CPS synthesized inductor. A differential transmission line was chosen, firstly due to the differential topology of VCO and secondly to make a compact design. To compare fairly with VCO design presented in chapter 2 (say VCO 1), same varactors were utilized and same inductor value was synthesized with S-CPS. Due to better  $Q$ -factor of S-CPS the equivalent losses of the resonator was less. So the designed VCO in this chapter 3 (say VCO 2) needed small cross-coupled pair to cancel the losses of resonator (or to start the oscillation). The simulated performance showed improvement in terms of  $PN$  and power consumption, i.e. both  $PN$  and power consumption reduced for VCO 2 due to use of high- $Q$  distributed inductor. However

the  $FTR$  did not show prominent increment as the slow-wave effect itself also adds some capacitance to the inductor value.

In chapter 4, to improve further the  $Q$ -factor of resonator, the S-CPS was periodically loaded by varactors, leading to the concept of tunable quarter-wavelength resonator (also called as phase shifter). As remarked in previous chapter 3, the slow-wave effects adds capacitance to the resonator, so to amend this issue an unsymmetric S-CPS topology has been proposed in chapter 4. Thanks to equivalent  $RLRC$  model, the design and optimization of unsymmetric S-CPS based phase shifter was faster. This unsymmetric structure allows to improve VCO performance especially in terms of  $PN$ . However the obtained  $FTR$  could not be improved as the varactor of small tuning range were utilized. By embedding larger varactors  $FTR$  of VCO was improved, but as expected due to higher losses the  $PN$  was higher. The VCO designed in this chapter (say VCO 4) is also called as standing wave oscillator (SWO), as a quarter wavelength resonator has been employed to design the oscillator. The simulated performance of VCO 4 showed clearly the tradeoff between  $PN$  and  $FTR$ . So, to overcome this tradeoff the concept of distributed SWO was employed in chapter 5.

In chapter 5 the issue of low  $FTR$  was resolved by employing distributed SWO topology. It allows distributing the cross-coupled pair for compensating losses of resonator periodically. Hence, an improved  $FTR$  was obtained. In all the VCO/SWO designs one of the major contributor of parasitic capacitance, power consumption and reduced output power is output buffer also. However being a necessary circuit for measurement it was difficult to cancel these effects of output buffer. Thanks to the careful choice of the output position, any output characteristic impedance can be envisaged due to the position dependent voltage and current of quarter wavelength resonator. Thus avoiding the necessity of an output buffer, leading to wider  $FTR$  and lower power consumption. Due to buffer-less distributed SWO the achieved power efficiency was higher as well.

## PUBLICATIONS

- E. Pistono, A. Bautista, E. Sharma, J. Lugo-Alvarez, Z. Iskandar, F. Podevin, S. Bourdel, P. Ferrari, “Recent advances of CMOS/BiCMOS tunable circuits for mm-wave applications,” en technologie BiCMOS 55nm. Application à l’orientation de faisceau en bande millimétrique,” in European Microwave Conference Workshop on Technologies Overview for mm-wave Tunable Circuits, **invited paper**, Paris, France, 2015.
- E. Sharma, A. Bautista, E. Pistono, P. Ferrari, S. Bourdel, “81–86 GHz VCO for Backhaul application with S-CPS based differential inductor in BiCMOS 55nm technology” in IEEE International NEW Circuits And Systems (NEWCAS) conference (NEWCAS), Grenoble, France, June 7 – 10, 2015.



## Résumé

Ce travail se concentre sur la conception de VCO en bande millimétrique et en technologie BiCMOS 55 nm pour les applications de Backhaul. Toutes les conceptions de VCO proposées sont comparées à l'oscillateur à résonateur LC conventionnel. La première solution proposée fonctionne entre 81-86 GHz. L'innovation réside dans l'utilisation d'une ligne coplanaire à ondes lentes (S-CPS) comme inducteur différentiel. Grâce au facteur de qualité élevé ( $\approx 33$ ) des lignes S-CPS, le bruit de phase a été amélioré de 20 dBc/Hz à 10 MHz d'offset et la consommation d'énergie a été réduite de 14%. La plage de réglage de fréquence (FTR) était de 5,3 GHz seulement. La seconde version du VCO est basé sur l'utilisation comme résonateur d'une ligne chargée (déphaseur). Le déphaseur a été conçu en utilisant une topologie dissymétrique de S-CPS afin de parvenir à une meilleure FTR. Cependant, les performances réalisées par ce VCO n'ont pas été beaucoup améliorées en raison de la capacité parasite en charge. Ainsi, avec le même déphaseur dissymétrique résonateur un oscillateur à onde progressive distribué a été conçu, ce qui a réduit l'effet de charge et a permis d'obtenir une FTR de 8 GHz. Enfin, un oscillateur en bande millimétrique sans buffer et à onde stationnaire a été conçu. Dans cet oscillateur, il a été montré que n'importe quelle impédance caractéristique de sortie peut être envisagée grâce à un choix judicieux de la position de sortie. Par conséquent, aucun buffer de sortie n'est nécessaire dans la conception proposée, en raison de la flexibilité dans le choix de la position de sortie le long du SWO. Cette innovation conduit à deux innovations. Tout d'abord une sortie 50 ohm peut-être synthétisé sans consommation d'énergie supplémentaire et d'autre part la taille est réduite si un réseau d'adaptation est nécessaire pour connecter le VCO à un mélangeur ou un autre bloc du système d'émetteur-récepteur.

**Mots-clés :** Ondes millimétriques, VCO, backhaul, BiCMOS 55 nm technologie, ondes lentes, ligne de bande coplanaires.

## Abstract

This work focuses on the design of millimetre-wave VCO for Backhaul applications in BiCMOS 55 nm technology. All the proposed VCO designs are compared to the conventional LC-tank oscillator. The first proposed oscillator design operates between 81-86 GHz. The innovation is linked to the use of a slow-wave coplanar strip (S-CPS) as a differential inductor. Thanks to high quality factor ( $\approx 33$ ) of S-CPS, the phase noise was improved by 20 dBc/Hz at 10 MHz offset and the power consumption was reduced by 14 % as well. The achieved frequency tuning range (FTR) was 5.3 GHz only. The second VCO design is based on loaded line phase shifter as a resonator. The phase shifter has been designed using an unsymmetric topology of S-CPS in order to achieve better FTR. The achieved VCO performance showed tradeoff between phase noise and FTR. So, with the same unsymmetric phase shifter based resonator a distributed standing wave oscillator was designed, which reduced the loading effect and lead to a FTR of 8 GHz. Finally, a buffer less mm-wave distributed standing wave oscillator was designed. In this proposed buffer less oscillator it is shown that any output characteristic impedance can be envisaged thanks to a careful choice of the output position. Hence, no output buffer is needed in the proposed design, due to the flexibility in choosing the output position along the SWO. This innovation leads to two merits. Firstly a 50 $\Omega$  output can be synthesized without any additional power consumption

and secondly the size is reduced if a matching network is needed to connect the VCO to a mixer or another building block of the transceiver system.

**Key words:** Millimetre-wave, VCO, backhaul, BiCMOS 55 nm technology, slow-wave, coplanar stripline.

