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# Caractérisation électrique des dispositifs FDSOI établie par mesures C-V

Blend Mohamad

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## THÈSE

Pour obtenir le grade de

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préparée au sein du **CEA-LETI** et de **l'IMEP-LAHC**  
dans **l'École Doctorale d'Électronique, Électrotechnique,  
Automatique et Traitement du Signal**

# Electrical characterization of fully depleted SOI devices based on C-V measurements

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# General context

The invention of the first transistor in 1947 allows John Bardeen, William Shockley and Walter Brattain to obtain the Nobel prize in Physics. This important event leads to a tremendous change in every aspects of life. Indeed after the first developments in 1954, the first general public application based on transistors appears with the radio. The field-effect transistor (MOSFET: Metal Oxide Semiconductor Field Effect Transistor) fabricated for the first time by Atalla and Kahng in 1960, became the key element for the semiconductor industry since 70's to nowadays becoming omnipresent (portable computer, mobile phone, cars, satellite . . .).

The operating principle of this device remains unchanged but its dimensions reduce continuously as predicted by Moore law. This phenomena well-known as "Downscale" from a generation to another (technological node) aims to gain in terms of electrical performance which substantially means to increasingly obtain faster transistors and therefore integrated circuit and high level electronic systems. The other main target of the downscale is to reduce the cost production of the transistor. Therefore, the semiconductor industry engages totally in downscale process with the objective of downscaling the density of transistors each two years as described by the ITRS (international Roadmap for Semiconductor). In this way between the economical considerations and the technological progress, the microelectronic evolution allows to obtain electronic devices (mobile phone, portable computer . . .) more and more fast and complex.

Nevertheless, since 2000's, the reduction of the dimensions is no longer sufficient in order to improve the electrical performance of the transistors which defines the end of the "straight Downscale Era". Indeed at nanometric scale, complex quantum phenomena are occurring, which deviates the standard operation principle of the transistor. Therefore in order to preserve the standard transistor operation, it is necessary to minimize these quantum parasitic effects. Straight downscale has to be accompanied with alternatives technological solutions which are:

- New device based on exotic architecture design: FDSOI (Fully depleted silicon on insulator transistor), Nanowires and Tri-Gate
- New channel material (III-V group) with higher charge mobility substituting the Silicon material.
- Mechanical stress induced during fabrication process which enhances the channel mobility.
- Gate stack process engineering which plays a fundamental role in defining the technological parameters (threshold voltage  $V_t$ , leakage current  $I_{off}$  and operation current  $I_{on}$ ).

Whereas the first solution overcome the limits of the conventional planar architecture on substrate (Bulk technology) from 32nm node technology authorizing downscale to lower technology node (12nm), the others three solutions are simply enhancing the electrical performance without decreasing the dimensions of the transistor. These solutions are widely used in the last decades and their effects on technological parameters of the transistors are more and more complicate to understand.

In this context, new electrical characterization methodologies are necessary to analyze the impact of these new technological solutions, in order to identify optimum solutions to improve the transistors electrical performance and diminish its cost production. This is called "Technology Optimization". Specifically, this work treats in detail the fully depleted FDSOI transistor on which new Gate stack process and different channel material (such as SiGe) including channel mechanical stress are carried out during the process fabrication.

Two parameters are representative of all the electrical performance aspects of a specific technology: the effective work function ( $WF_{eff}$ ) and the Equivalent Oxide Thickness (EOT). The aim of this work is to find new electrical characterization methodologies in order to analytically, rapidly and accurately extract EOT and  $WF_{eff}$  in case of thin film FDSOI transistors and to pursue the Technology Optimization.

The first chapter generally introduces the operation principles of a standard transistor MOSFET on bulk substrate. Specifically a detailed description of the traditional MOSFET operation during Capacitance-Voltage measurement, the typical extraction methodologies of EOT and  $WF_{eff}$  based on this C-V measurements and the flat band voltage  $V_{fb}$  identification are presented. Moreover a rigorous definition of EOT and  $WF_{eff}$  is given. The incompatibility

of this standard C-V measurement technique with innovative FDSOI transistors and a necessary need of new electrical characterization methodologies in order to extract EOT and  $WF_{\text{eff}}$  are evidenced.

The incompatibility of the classical C-V extraction methodologies is due to the missing flat band condition in the FDSOI Capacitance-Voltage characteristics. The necessity of a physical comprehension of the electrostatic behavior of the FDSOI during C-V measurement comes out naturally. The first half of the second chapter is devoted to electrostatic analysis of FDSOI transistor which means to find the fundamental relationships, in terms of Voltage and Capacitance, accounting of the complexity of the electrostatic FDSOI behavior during C-V measurements. The second half of the chapter is dedicated to the numerical simulation that can reproduce Capacitance-Voltage characteristics for a specific FDSOI transistor. Such simulations are fundamental to understand the electrostatic behavior of the FDSOI device under specific biases conditions (C-V measurement).

The third chapter presents an extraction methodology to extract EOT and  $WF_{\text{eff}}$  which is based on specific strategy (or procedure). This numerical extraction methodology identifies all the FDSOI stack layers thicknesses (Gate oxide, channel and buried oxide). This is carried out for each layer by fitting specific C-V measurements with the numerical simulations that are introduced in the second chapter. The FDSOI stack thicknesses are required in order to obtain the proper value of  $WF_{\text{eff}}$  for a specific FDSOI transistor Gate stack. Despite its extraction precision, the numerical methodology appears costly and complex highlighting the need of a faster and simpler analytical methodology.

Therefore in the fourth chapter, we will present an analytical extraction methodology which is faster than the numerical methodology (chapter 3). It is based on the linear regression which leads to the direct estimation of the FDSOI stack layers (Gate oxide, channel and buried oxide) thicknesses. Unfortunately, we will show that this methodology is incomplete since the fundamental identification of  $WF_{\text{eff}}$  cannot be carried out. Moreover, the extraction methodology requires a correction (quantum) on the estimated FDSOI stack layers thicknesses due to the quantum effects occurring in the channel and well layers.

Considering the cost of complexity of the numerical extraction presented in chapter 3 and the limit of the analytical method of chapter 4, the necessity of an alternative analytical methodology is evidenced. In the chapter 5, a complete extraction methodology is proposed which leads not only to estimate

EOT and  $W_{\text{eff}}$  but as well all the FDSOI stack layers thicknesses, the bulk substrate properties and the total electrostatic condition (channel, well and metal charges) of the the FDSOI transistor during C-V measurement. This extraction methodology is based on new capacitance measurements and an innovative extraction algorithm which allows to compare different technologies (e.g. Si and SiGe channel material). Moreover, this extraction is fast and precise since quantum effects are properly considered.

# Chapter 1

## Introduction to C-V measurements and operation of MOS

### 1.1 Introduction

Metrology, defined by international Bureau of Weights and Measures, as the science of measurements, embraces both theoretical and practical aspects of the measurement. The science of measurements plays a fundamental role in the technology optimization. Indeed electrical measurements and analysis, which are a fundamental part of device engineering, are carried out continuously in order to improve and design optimized transistors in the microelectronic industry. It is in this context that Capacitance-Voltage measurements have been and are one of the most widely used technique to electrically characterize MOSFET transistor and consequently extract the relevant parameters related to specific technologies (materials electrical properties) used in the transistor. These capacitance voltage measurement are carried out on the traditional MOS transistor whose acronym stands for Metal oxide semiconductor field effect transistor. Whereas the Capacitance-Voltage techniques, for traditional MOS transistors, are well known and mastered in the state of the art, new electrical methodologies are required for recent upcoming technologies such as the FDSOI MOSFET transistors, whose acronym, in this case, stands for fully depleted silicon on Insulator MOSFET transistor. Therefore in order to understand the problematics related to the new technologies, and especially the incompatibility of the standard C-V measurement technique with innovative FDSOI transistors, a detailed description of the traditional MOSFET operation during C-V measurement, the typical extraction methodologies based on this C-V measurement and a comparison with FDSOI architecture will be presented.

Moreover, we will present the fundamental technological parameters and their impact over the device electrical performances.

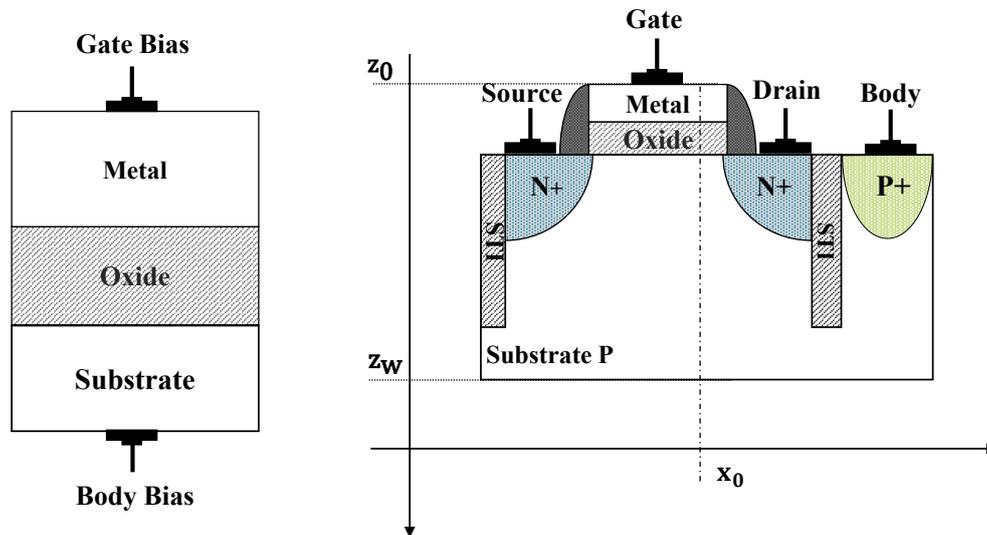


Figure 1.1: Schematic of a MOS capacitance.

## 1.2 MOS transistor and operation regime during C-V measurement

As shown in the right side of Fig. 1.1, the MOSFET is a four-terminal device: Gate (G), Source (S), Drain (D), and Body (B). The Gate stack is composed of a specific bilayer structure consisting of a metal on top of an oxide, whereas Source and Drain are simply ohmic contacts. The Source and Drain contacts feature highly doped semiconductor wells ( $10^{20}\text{cm}^{-3}$ ), specifically P or N-type for P or N-MOS devices. The Body contact, always ohmic, features as well a highly doped semiconductor well ( $10^{20}\text{cm}^{-3}$ ) whose doping type depends on the MOS type: N-type well for P-MOS and P-type well for N-MOS devices. Finally, the substrate (or channel semiconductor) is doped, with the same doping type as the Body well, but at a lower level (between  $10^{16}\text{cm}^{-3}$  and  $10^{18}\text{cm}^{-3}$ ). In general terms, this MOS transistor is a component which plays the role of an electrical switcher by passing or blocking the channel current between Source and Drain terminals. The basic principle of this technology is based on what is called the field effect, which will electrostatically modulate the density of free charge in the channel by applying a specific Gate Voltage ( $V_G$ ). The conductivity of the silicon channel, like any other semiconductor, will depend on the quantity of free carriers in the

conduction band (electrons) or the valence band (holes). The voltage applied to the Gate will modulate these quantities, at the semiconductor surface close to the dielectric, thus obtaining a MOS capacitance. The channel features a doping type, as previously said, opposite to the Source and the Drain wells. If no Gate voltage is applied, its resistivity is high and therefore the resistance between Source and Drain is large. This is called 'off-state'. By applying a proper Gate voltage, the channel is enriched by the minority carriers, coming from the Source and Drain wells. The resistivity of the channel decreases sharply and the transistor is said 'on-state'. Thus, in an n-channel transistor (N-MOS), the Source and Drain are source of electrons and the transistor will be on-state if the channel is enriched by minority carriers (electrons). The voltage  $V_G$  applied at the Gate will enable us to create the inversion charge in the channel and a different applied voltage at the Source and Drain terminals ( $V_{DS} = V_D - V_S = V_D$ ) will displace these charges, under the effect of an electrical field induced by  $V_{DS}$ , from Source to Drain terminal. The analysis of the band diagrams of the MOS capacitor of Fig. 1.1 (left side) will allow us to better understand the transistor regime operation depending on the applied  $V_G$  voltage.

### 1.2.1 Band diagram of the MOS capacitor

The heart of the MOS transistor is the MOS capacitor (Fig. 1.1), presented and indicated as "varactor" capacitance by Moll [1] and by Pfann and Garrett [2] in 1959. The term varactor was used at that time to indicate that the capacitance between a metal and a semiconductor varies with voltage. It was clear that the semiconductor, different from the metal, had a key role in the deformation of the expected measured capacitance between the metal and the semiconductor. Indeed Pfann, Garrett and Moll got to the conclusion that this variation was due to the behavior of the space-charge layer near the surface of oxide-semiconductor, and therefore the semiconductor electrical behavior or more properly the semiconductor operation regime (the electrostatic condition and the state of its charge). In Fig. 1.2 we report an example of Capacitance-Voltage characteristics of a simple MOS stack with a P-type substrate. The C-V curves of this stack is obtained with a Capacitance-meter, named 4284A, that allows to measure complex impedance thanks to the superimposition of an alternate small voltage signal and a main continuous voltage (High terminal) while induced current is measured on the other grounded terminal (Low terminal). The two terminals are connected to the

electrical contacts of MOS stack test structure, respectively the High terminal to the Gate and Low terminal to the Body, as reported in Fig. 1.3. The measurement has been carried out by varying the Gate voltage from 1V to -1.4V. For each step voltage (50mV), the small signal voltage induced current is read at the low terminal by the Capacitance Meter and the relative capacitance is calculated. These are reported with black triangle symbol in Fig. 1.2.

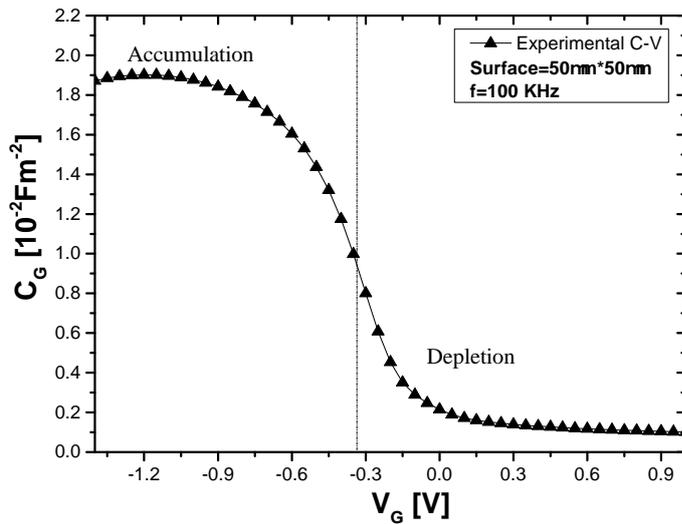


Figure 1.2: Capacitance-Voltage measurements of a MOS capacitor.

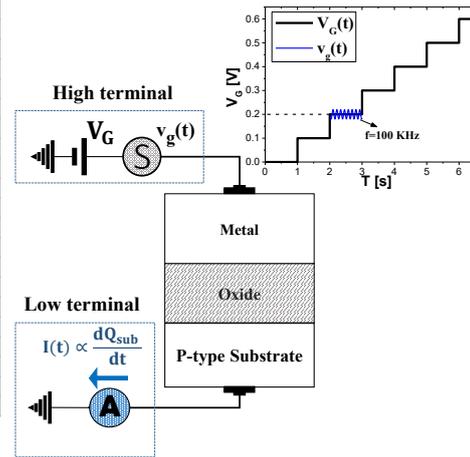


Figure 1.3: Experimental configuration for C-V measurement.

In order to understand the Capacitance variation, we propose hereafter a study of the MOS system through its band diagrams representation, by taking care of the semiconductor layer electrostatic behaviour. Each material of this capacitor is characterized by electrical macroscopic parameters that affect the behaviour of the channel charge induced by  $V_G$  voltage. In figure 1.4, we report the band diagrams as well as the relative technological parameters.  $WF_m$ , the metal work function, corresponds to the energy that has to be supplied ( $T = 0\text{K}$ ) to extract an electron from the metal to the vacuum whereas  $X_{\text{ox}}$  and  $X_{\text{sc}}$  are the electrical affinity of the oxide and semiconductor which represent the energies required to extract an electron from their relative conduction bands.  $WF_{\text{sc}}$  is the necessary energy to extract an electron from the semiconductor: this energy is lower compared to the oxide electrical affinity. By bringing these three materials into contact and applying a Gate voltage, a thermodynamic equilibrium is established among them. We remember that the Gate voltage is the applied voltage at the Gate terminal and corresponds to the difference between the metal and semiconductor Fermi energies. If  $V_G = 0\text{V}$  these Fermi energies are aligned. For any  $V_G$  bias a potential profile is induced along the  $z$  position, perpendicular to

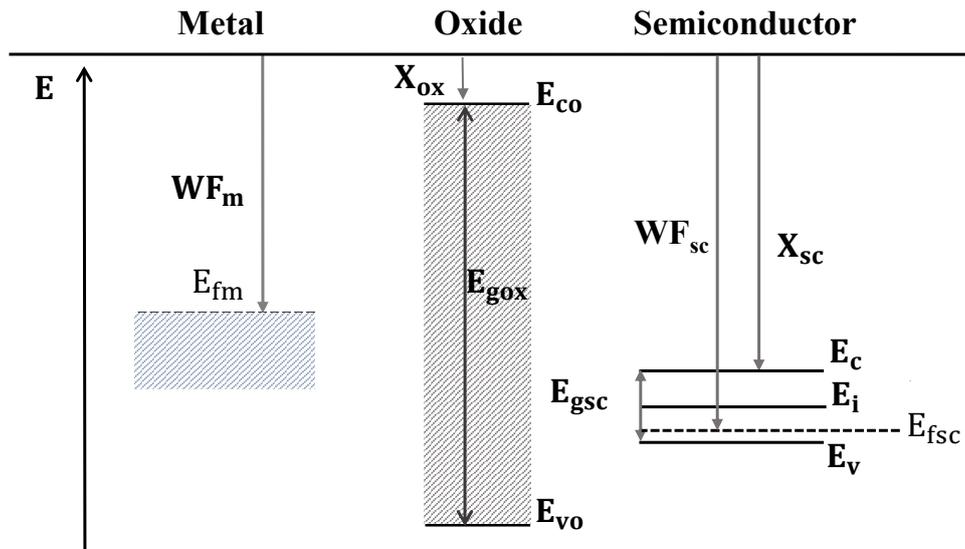


Figure 1.4: Band diagrams of the layers composing the MOS capacitor: Metal-Oxide-Semiconductor.

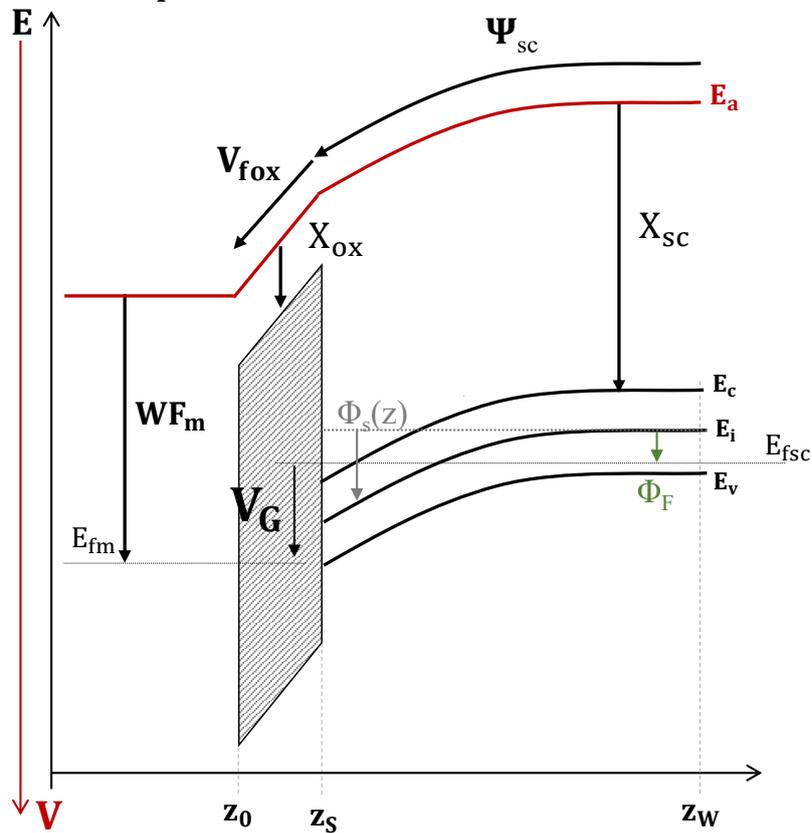


Figure 1.5: Band diagrams of the MOS capacitor at thermodynamic equilibrium.

oxide semiconductor interface. The type of charge induced at the interface will define the operation regime of the MOS capacitor during C-V measurement.

## 1.2.2 Operation Regime

Before introducing the operation regimes, we need to clarify a few things. As reported in Fig. 1.5, the semiconductor band bending represents the variation of potential energy of electrons, in terms of electron Volts (eV). This potential  $\phi_s(z)$  varies from 0, in the neutral region of the semiconductor ( $z_W$ ) to  $V=\phi_s$  at the interface oxide-semiconductor ( $z_S$ ).  $\phi_s$  is known as the potential surface. The operation regimes depend of the applied  $V_G$  voltage. Whereas a detail description of these regimes can be found in Shockley's book [3], here we propose a brief picture of these regimes, that are:

1. Accumulation Regime: The channel is enriched of majority carriers. For an N-MOS with a P-type substrate, the amount of holes (p) is therefore higher than the level of the holes induced intrinsically by the semiconductor, that is equal to the number of active acceptors ( $N_a$ ). This occurs when  $\phi_s < 0$ . The transistor is therefore off-state. In case of P-MOS with a N-type substrate, the amount of electrons (n) has to be bigger than  $N_d$ , where  $N_d$  is the donor concentration. This condition occurs when  $\phi_s > 0$ .
2. Depletion Regime: The surface of the semiconductor is depleted of the majority carriers. The amount of holes at the oxide-semiconductor interface is lower than the acceptor concentration. Nevertheless, the holes concentration, in the valence band, is still superior to the electrons concentration (n) in the conduction band which means  $0 < \phi_s < \phi_F$  where  $\phi_F$  is the Fermi potential related to the Fermi holes concentration in the neutral region from the doping concentration  $N_a$  ( $N_d$  in case of P-MOS transistor). Therefore we have  $n < p < N_a$  whereas for a P-MOS we have  $p < n < N_d$  ( $-\phi_F < \phi_s < 0$ ). The depletion region is the result of the displacement of the majority carriers across the semiconductor that are escaping through the semiconductor-electrode ohmic contact (Body contact).
3. Inversion Regime: In this operation regime, we have an inversion of free carriers ( $\phi_s > 0$ ). This condition occurs in case of transistors (1.1 right side) and as well simple MOS capacitors. Indeed the creation of inversion charge is related to two specific processes: the inversion supplied by the Source and Drain wells or the carrier generation phenomena [4] that occurs at a specific generation rate. Specifically we have a thermal generation type which is always present whenever the temperature of the semiconductor material is greater than zero kelvin. Once the inversion is generated, independently

by the Source and by Source-Drain diffusion or thermal generation, two sub-regimes are identified during the inversion operation regime:

- (a) weak inversion: This condition occurs while the inversion layer at oxide-semiconductor interface is equal or bigger with respect to the doping concentration of the semiconductor ( $N_a$ ). Therefore we have, in case of N-MOS transistor, that  $\phi_s > 0$  and  $\phi_F < \phi_s < 2\phi_F$  while for P-MOS transistor the condition is  $-2\phi_F < \phi_s < -\phi_F$ .
- (b) strong inversion: When  $\phi_s$  is larger than  $2\phi_F$  the minority carriers concentration is larger compared to the majority ones, that means  $n \gg p$  for a N-MOS.  $\phi_s = 2\phi_F$  represents the condition that defines the limit between weak and strong inversion. In case of P-MOS transistor we have  $\phi_s \leq -2\phi_F$ .

In case of MOS capacitor (Fig. 1.2), inversion characteristic is missing. This is related to the fact that for these measurements there is no Source and Drain diffusion which doping-type is opposite with respect to the substrate and would provide a sufficient amount of minority carriers, able to respond to the potential variations applied to the Gate terminal. The capacitive measurement is then only related to the response of the majority carriers. This is the capacitance measurement between the Gate and substrate (Body) terminals, commonly denoted as  $C_{gb}$ . In general the C-V characteristic associated to majority carriers is the easiest measurement result to obtain since only two terminals are necessary (Gate and substrate), which allows us to consider simplified test structures. There's no need of specific Source and Drain implantation since the  $V_{fb}$  and EOT can be extracted in the depletion-accumulation region and specifically the EOT at strong accumulation and the  $V_{fb}$  at the beginning (onset) of the accumulation [5, 6]. The missing  $C_{gc}$  characteristic is used in Bulk substrate for the study of the carrier mobility because it gives us access to the carrier concentration in the transistor during channel inversion, as demonstrated by F.Lime et al. [1].

The only phenomena leading to the semiconductor inversion, in this case, is the thermal generation. The inversion carriers are created at a specific rate which is  $f_{gr}$ . As previously said, during C-V measurement, two signals are applied at Gate contact: a constant voltage  $V_G$  ( $f_G=0$ ) and a small signal voltage  $v_g(t)$  characterized by a specific frequency  $f_g$ . The inversion charge, created by the thermal generation phenomena, can always respond to the constant voltage  $V_G$  since  $f_{gr} > f_G=0$ , but is not capable to respond to the variations of small signal voltage  $v_g(t)$  if  $f_{gr} < f_g$ . Since the C-V measurement of Fig. 1.2 (MOS capacitor)

is carried out at  $f_g = 100 \text{Kz} > f_{gr}$ , only depletion and accumulation regimes are observed on the C-V characteristic.

### 1.2.3 Total charge and C-V characteristics of a MOS capacitor

As previously seen, depending of the applied Voltage  $V_G$ , the semiconductor is characterized by a specific operation regime during C-V measurement. At this condition, we have a specific distribution of semiconductor charge ( $\rho(z) = p(z) - n(z) + N_d - N_a$ ) from which we can easily calculate the total charge by its simple integration, which leads to:

$$Q_{sc} = -Q_g = \int_{z_S}^{z_W} \rho(z) dz \quad (1.1)$$

In Figure 1.6 we report the dependence of a simulated total charge as a function

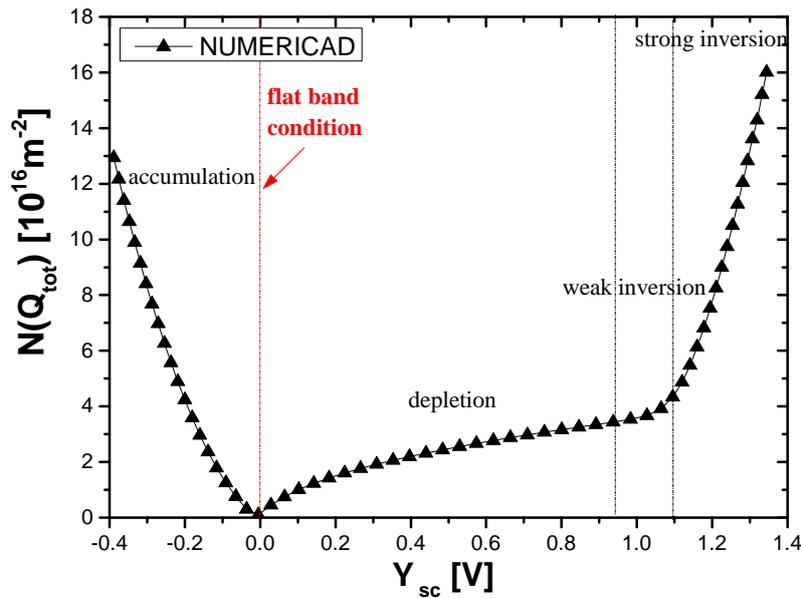


Figure 1.6: Variation of the total number of carriers of the semiconductor versus the semiconductor potential drop for a constant doping ( $N_a$ ) concentration level equal to  $10^{18} \text{cm}^{-3}$ .

of the semiconductor potential drop for P-type semiconductor, for a doping concentration  $N_a = 10^{18} \text{cm}^{-3}$ . As we previously said, the total charge varies with the Gate voltage at different operation regimes. Therefore the C-V characteristic will depend on electrostatic condition of the semiconductor (the charge and the potential drop). Indeed, during C-V measurement, for each specific  $V_G$  we have a different distribution of semiconductor charge whose relationship

with the relative surface potential  $\Psi_{sc}$  affects the expected dielectric capacitance between the two electrodes (metal and semiconductor). We remember that, at the opposite, in a metal electrode, independently of the metal charge, no potential drop occurs which leads to a very large metal capacitance  $C_m = dQ_m / d\Psi_m$  that can be neglected. Therefore the MOS stack capacitor is a system of two capacitances in series: the oxide capacitance and the semiconductor capacitance which is dependent of the Gate Voltage.

If we know the relation between the semiconductor charge  $Q_{sc}$  (Coulomb) and its potential drop  $\Psi_{sc}$  (Volts) we can calculate the associate semiconductor capacitance  $C_{sc} = -dQ_{sc} / d\Psi_{sc}$ , leading then to obtain the total capacitance  $C_g$  from a given specific charge  $Q_{sc}$ :

$$\frac{1}{C_g} = \frac{1}{C_{ox}} + \frac{1}{C_{sc}} \quad (1.2)$$

where  $C_{ox} = \epsilon_{SiO_2} / t_{ox}$  is the expected capacitance of the oxide between the two electrodes. This total capacitance is normalized by the device area and is measured in Farad/m<sup>2</sup>. When we increase the voltage  $V_G$  for a semiconductor of type P (respect. N), as reported in Fig. 1.2, the substrate evolves from the accumulation of holes (respect. inversion of holes) to the depletion and then to inversion of electrons (respect. accumulation of electrons). As previously explained, inversion cannot be measured in the case a MOS capacitor. From accumulation to depletion, there's a specific voltage condition for which the substrate charge is zero. This means  $Q_{sc} = 0$  that is well known as flat band condition ( $V_{fb}$ ) at the interface oxide-semiconductor. Once we have identified this voltage condition on the characteristic C-V of Fig. 1.2, we can calculate the semiconductor charge at any  $V_G$  voltage by integrating the total experimental capacitance from the flat band voltage  $V_{fb}$ :

$$Q_{sc} = -Q_m = - \int_{V_{fb}}^{V_G} C_g dV \quad (1.3)$$

The applied voltage  $V_G$ , during C-V measurement, is equivalent to the sum of the drop voltages across the dielectric oxide  $V_{ox}$ , the semiconductor  $\Psi_{sc}$  and the difference of Fermi levels between the metal and the semiconductors. From the analysis of Fig. 1.5, we can calculate

$$V_G = \frac{WF_m}{q} - \frac{WF_{sc}}{q} + \Psi_{sc} + V_{ox} \quad (1.4)$$

This equation takes into account the relation between the charge at the electrodes

and the oxide voltage drop  $V_{ox} = -Q_{sc}/C_{ox}$ .  $WF_m$  and  $WF_{sc}$  are technological parameters associated to the electrodes materials, their work function.  $WF_{sc}$  can be estimated from given doping level  $N_{sc}$  and temperature ( $T=300$  K) by simply solving the following equation

$$WF_{sc} = X_{sc} + E_{gap}/2 + LK_B T \ln \frac{N_{sc}}{n_i} \quad (1.5)$$

where  $n_i$  is the intrinsic doping level of silicon material ( $n_i=10^{10} \text{cm}^{-3}$  at 300 K) and  $K_B$  is the Boltzmann constant with  $L$  equal to 1 for a substrate of type P and -1 for a substrate of type N. This leads us finally to obtain:

$$V_G(Q_{sc}) = \frac{WF_m}{q} - \frac{WF_{sc}}{q} + \Psi_{sc}(Q_{sc}) - \frac{Q_{sc}}{C_{ox}} \quad (1.6)$$

Using equations 1.2, 1.5, 1.6 and knowing the relation  $\Psi_{sc}(Q_{sc})$  (as reported in Fig. 1.6), we can predict the experimental behavior of a Capacitance-Voltage characteristic of a specific Gate stack (Metal-Oxide-Semiconductor). This Capacitance-Voltage is unique for each specific MOS capacitor ( $WF_m$ ,  $C_{ox}$  and  $N_{sc}$ ). In Figures 1.7 and 1.8, we report the simulated total charge and capacitance as function of the applied voltage  $V_G$ . For this simulation, an oxide thickness ( $t_{ox}$ ) was 1 nm, the metal work function  $WF_m$  4.76eV and the semiconductor doping level equals  $N_a=10^{18} \text{cm}^{-3}$ . C-V characteristic of MOS capacitor is

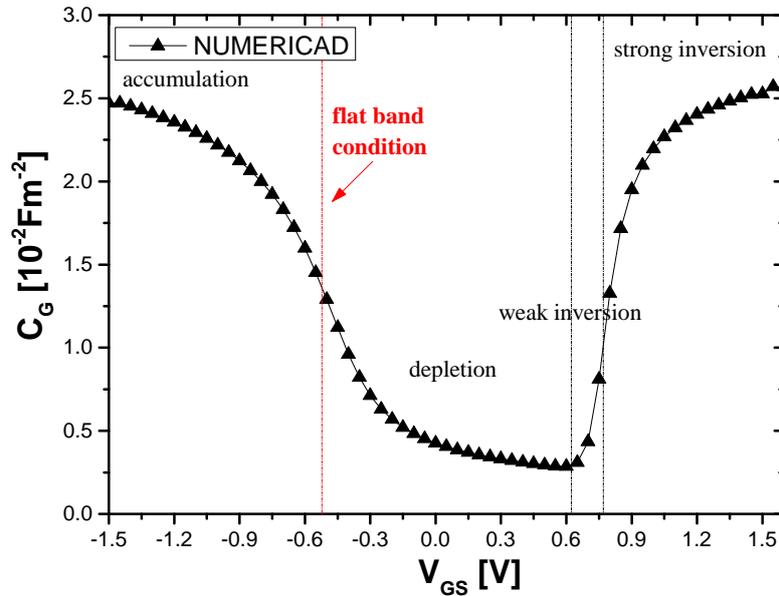


Figure 1.7: Total capacitance as function of the Gate voltage for a  $10^{18} \text{cm}^{-3}$  constant doping ( $N_a$ ) concentration level.

a fundamental source of information. Indeed, its dependence is related to

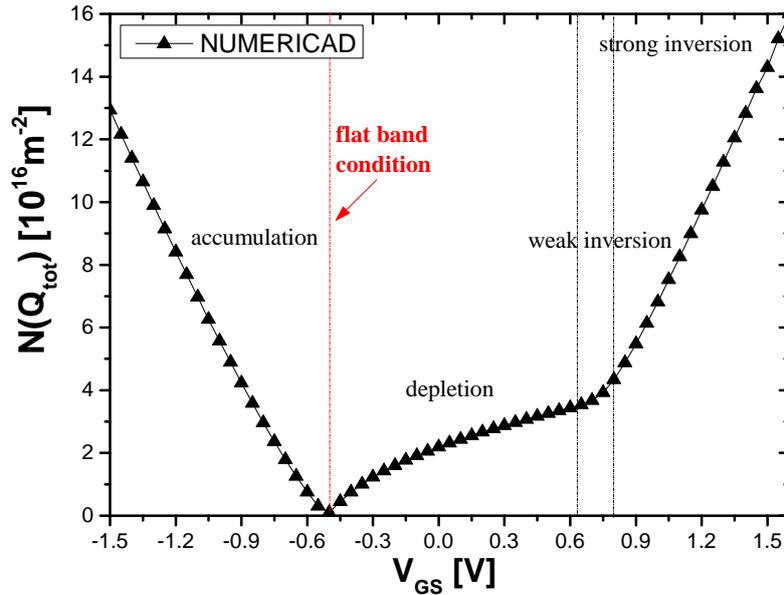


Figure 1.8: Variation of the total number of carriers of the semiconductor versus the Gate voltage for a  $10^{18} \text{ cm}^{-3}$  constant doping ( $N_a$ ) concentration level.

the dielectric oxide and the semiconductor electrostatic behavior (macroscopic electrical properties). In the state of the Art, the Capacitance-Voltage (C-V) measurement is used to determine the semiconductor and the dielectric technological parameters, particularly in MOSCAP and MOSFET structures. C-V measurements can reveal oxide thickness, oxide charges, contamination from mobile ions, and interface trap density in wafer processes. These measurements continue to be important after each process steps that has been performed, including lithography, etching, cleaning, dielectric and polysilicon depositions, and metallization processes. C-V characteristics are often used to characterize the flat band and threshold voltage ( $V_{th}$ ) and other parameters during reliability and basic device testing and to model device performance. It is in this context that we will introduce in the next section three important technological parameters that defines the performance of a MOS transistor.

### 1.3 $V_{fb}$ , EOT and $WF_{eff}$ definition

Based on the work of Troutman [7], the  $V_{fb}$  is defined as the Gate voltage for which the total semiconductor charge level is zero, as reported in Figures 1.7 and 1.8. By assuming constant doping concentration and classical formalism (Boltzmann), not only the semiconductor charge is zero but as well the semiconductor potential drop  $\Psi_{sc}=0$ . Unfortunately this condition rarely occurs in the real devices where substrates are characterized by a non-constant doping concentration and therefore  $\Psi_{sc} \neq 0$ . From the relation 1.6, we can define the flat band voltage  $V_{fb}$  as

$$V_G(Q_{sc} = 0) = V_{fb} = \frac{WF_m}{q} - \frac{WF_{sc}}{q} + \Psi_{sc}(V_{fb}) \quad (1.7)$$

This voltage, expressed in Volts (V), allows the  $WF_m$  extraction of the Gate stack expressed in electron-Volts (eV). The flat band voltage takes into account the reference potential of the semiconductor ( $WF_{sc}$ ). This depends only on the semiconductor and it is calculated in eV. Thus, assuming a certain doping level value, the relation between the metal work function and the flat band voltage is direct since no drop voltage occurs at this condition ( $\frac{Q_{sc}}{C_{ox}} = 0$  and  $\Psi_{sc}=0$ ) leading to the extraction of the metal work function. This calculation is for an ideal MOS capacitor, that means zero charge inside the oxide including its interface (metal-oxide and oxide-semiconductor). Unfortunately such condition

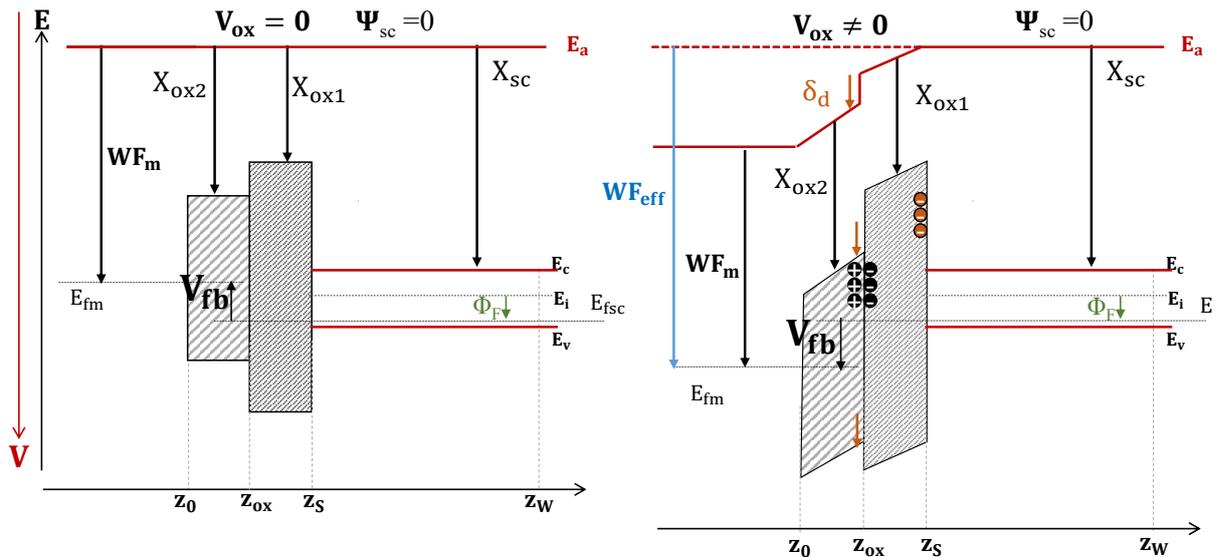


Figure 1.9: Energy band diagrams of a MOS structure at the flat band condition without any oxide charge (left figure) and with charges and dipole in the oxide (right figure).

doesn't occur in the real devices. From the first and simple MOS stack capacitors [1, 2] in the 50-60s, the progressive scaling-down and the necessity of higher electrical performance devices, pushed them to turn the standard MOS Capacitor into a more complex multilayer stack with multiple process steps that induce undesired (or desired) defects across the stack. Indeed the presence of fixed charges and dipole at specific interface location induce a drop voltage across the oxide even when the substrate charge is still zero. In Figure 1.9, in the left side, we show the band diagrams of the ideal MOS capacitor with two different oxides in series at flat band condition and, in the right side, the band diagrams of a non-ideal MOS capacitor characterized by the same dielectric stack, metal and semiconductor but with the presence of fixed charge at the interface between the first oxide and semiconductor and a dipole located at the interface between the two oxides, always at flat band condition. We notice that the presence of these oxide impurities changes the flat band condition with respect to the ideal MOS capacitor. The relation between the flat band and the metal work function has to take into account the voltage drop induced by the oxide charges and dipole. Therefore relation 1.7 becomes:

$$V_G(Q_{sc} = 0) = V_{fb} = \frac{WF_m}{q} - \frac{WF_{sc}}{q} - \frac{Q_{fi}}{C_{ox}} + \delta_d + \Psi_{sc}(V_{fb}) \quad (1.8)$$

where  $\delta_d$  is the impulsive drop voltage located at the interface between the two dielectrics due to the dipole,  $Q_{fi}$  is the fixed charge,  $C_{ox}$  is the equivalent capacitance of the Gate stack dielectric (series of the two oxide) and  $\Psi_{sc}(V_{fb})=0$  if classical formalism and constant doping are assumed. Moreover, the drop voltage induced by the fixed charges is  $\frac{Q_{fi}}{C_{ox}}$  since we assume that they are located at the interface oxide/semiconductor. Therefore, in terms of  $V_{fb}$ , equation 1.6 can be written as

$$V_G(Q_{sc}) = V_{fb} + \Psi_{sc}(Q_{sc}) - \frac{Q_{sc}}{C_{ox}} - \Psi_{sc}(V_{fb}) \quad (1.9)$$

The presence of these charges and dipole doesn't affect only the flat band voltage but also the threshold voltage  $V_{th}$  that is defined from equations 1.6 and 1.8 as

$$V_{th} = V_{fb} + 2\phi_f - \frac{\sqrt{2q\epsilon_{Si}N_a(2\phi_f)}}{C_{ox}} - \Psi_{sc}(V_{fb}) \quad (1.10)$$

The impact of the relative fixed charges and dipole is the same for any applied voltage  $V_G$  (accumulation, depletion and inversion). Therefore, since the simulated Capacitance-Voltage characteristics of the ideal MOS capacitor of Fig. 1.9 (left side), is reported in Fig.1.7, the C-V characteristics of the real MOS (Fig. 1.9

right side) will have the same trend of the ideal MOS C-V but shifted of a voltage  $\delta V_G = -\frac{Q_{fi}}{C_{ox}} + \delta_d$ . This means that we can tune and change the threshold voltage (and the flat band voltage) by inducing charges and dipole inside the oxide and therefore by playing with the fabrication process and not only by tuning the theoretical gate stack parameters (metal work function, oxide thickness and doping level of the semiconductor). The "tunable" shift on the C-V characteristic is interpreted by the process engineers as the result of a new C-V measurement on a different gate stack, with respect to the ideal MOS stack structure, which features a new metal characterized by an "effective work function"  $WF_{eff}$ . The effective work function is the sum of the metal work function and the shift induced by fixed charges and dipoles expressed in eV ( $q\delta V_G = -\frac{qQ_{fi}}{C_{ox}} + q\delta_d$ ). Indeed from equation 1.8 we define the effective work function as:

$$WF_{eff} = WF_m - \frac{qQ_{fi}}{C_{ox}} + q\delta_d + q\Psi_{sc}(V_{fb}) = WF_m - \frac{qQ_{fi}t_{ox}}{\epsilon_{ox}} + q\delta_d + q\Psi_{sc}(V_{fb}) \quad (1.11)$$

that, in terms of  $V_{fb}$ , is

$$WF_{eff} = qV_{fb} + WF_{sc} - q\Psi_{sc}(V_{fb}) \quad (1.12)$$

and therefore relation 1.6 becomes

$$V_G(Q_{sc}) = \frac{WF_{eff}}{q} - \frac{WF_{sc}}{q} + \Psi_{sc}(Q_{sc}) - \frac{Q_{sc}}{C_{ox}} - \Psi_{sc}(V_{fb}) \quad (1.13)$$

The effective work function value (eq. 1.11) depends strongly on the technology process through which the process engineers induce fixed charges and dipoles across the dielectric ( $q\delta V_G = -\frac{qQ_{fi}}{C_{ox}} + q\delta_d$ ). Moreover, this value depends on the dielectric constant and thickness, which are as well affected by the process, since they define the drop voltage induced by the fixed charges ( $-\frac{qQ_{fi}}{C_{ox}} = -\frac{qQ_{fi}t_{ox}}{\epsilon_{ox}}$ ). Therefore two Gate stacks (metal-oxide-semiconductor) that differ from the dielectric constant and thickness value ( $\epsilon_{ox1}, t_{ox1}$  and  $\epsilon_{ox2}, t_{ox2}$ ) with the same amount of dipole and fixed charges at the oxide-semiconductor interface, will have two different effective work function values ( $WF_{eff1}$  and  $WF_{eff2}$ ). Indeed the induced oxide voltage ( $\frac{qQ_{fi}}{C_{ox1}} \neq \frac{qQ_{fi}}{C_{ox2}}$ ), at the flat band condition, will be different for the two dielectrics supposing the same amount of fixed charge.

The choice of the dielectric type and thickness can be crucial for the electric performance of the MOS stack. Indeed, the reduction of the dielectric thickness (SiO<sub>2</sub>) in the subnanometric range produces dramatic gate leakage issues detrimental for the electrical performance. The process engineers try to replace

this standard dielectric oxide (SiO<sub>2</sub>) with the introduction of high-k materials (or high-dielectric permittivity material) which allows an increasing electrical performance without reducing the physical dielectric thickness. By convenience, the physical thickness has been replaced by an electrical thickness or Equivalent Oxide Thickness (EOT). This technological parameter is used in order to refer all the dielectric technologies to the reference SiO<sub>2</sub> dielectric technology. We can calculate the equivalent oxide thickness by simply using the following equation

$$EOT = \frac{t_{ox}\epsilon_{SiO_2}}{\epsilon_{ox}} \quad (1.14)$$

This relation requires the precise value of the Gate stack dielectric constant. Therefore in order to calculate the effective work function and the equivalent oxide thickness of a Gate stack, firstly we need to extract the amount of fixed charge and dipole inside the oxide and secondly the exact value of the dielectric constant. This extraction results tedious and almost impossible. The aim of the extraction is not to find the physical thickness of the dielectric and neither the effective metal work function values but to take into account properly of the electrical coupling between the two electrodes. It is for this reason that alternative approach have been proposed in order to extract  $WF_{eff}$  and EOT and this will be presented in the next section.

## 1.4 Impact of EOT and $WF_{\text{eff}}$ on the MOS Electrical performance

EOT and  $WF_{\text{eff}}$  extraction is fundamental due to their impact on the transistor electrical performance. In this paragraph we will define the most important transistor performance parameters, that are:

1. **Threshold Voltage:** As seen previously we define the threshold voltage as the Gate voltage for which the density of inversion charge becomes equal to the depletion charge. This condition leads to have  $\phi_s = 2\phi_f$ . In this case the inversion charge is the free carrier and the  $V_{\text{th}}$  corresponds to the on-set state of the channel. This parameter is fundamental because it corresponds to the on-state behavior of the transistor. In the case of the N-MOS, for negative  $V_G$ , the transistor will be off-state (accumulation regime). By progressively increasing the voltage, a depletion region forms until its maximum extension and the formation of the first inversion charge at the surface oxide-semiconductor. The threshold voltage is defined, in terms of EOT and  $WF_{\text{eff}}$ , as

$$V_{th} = V_{fb}(WF_{\text{eff}}) + 2\phi_f - \frac{\sqrt{2q\epsilon_{Si}N_a(2\phi_f)}\mathbf{EOT}}{\epsilon_{SiO_2}} - \Psi_{sc}(V_{fb}) \quad (1.15)$$

2. **Commutation time:** This parameter defines the time necessary to pass from offset to onset state. It's a fundamental parameter that describes, in terms of speed, the efficiency of a single transistor in digital circuits. The intrinsic commutation time is defined by the relation

$$\tau = \frac{C_{ox} \cdot V_{DD}}{I_{on}} = \frac{\epsilon_{SiO_2} \cdot V_{DD}}{I_{on}\mathbf{EOT}} \quad (1.16)$$

where  $V_{DD}$  is the supplied voltage applied at the Drain that defines the  $I_{on}$  current. The aim is to diminish this time as much as possible in order to reduce the commutation time. An optimization of the dielectric oxide is necessary (comparing different technologies with different EOT).

3. **Sub-threshold slope:** it is a typical parameter of the transistor during weak inversion regime.

$$S = \frac{\partial V_G}{\partial \log I_D} = \frac{KT}{q} \ln(10) \left( 1 - \frac{1}{C_{ox}} \frac{\partial Q_d}{\partial \phi_s} \right) = \frac{KT}{q} \ln(10) \left( 1 - \frac{\mathbf{EOT}}{\epsilon_{SiO_2}} \frac{\partial Q_d}{\partial \phi_s} \right) \quad (1.17)$$

with  $(1-dQ_d/\phi_s \times 1/C_{ox})=(1-C_d/C_{ox})$  where  $C_d=-dQ_d/\phi_s$ . It's given in Volts per decade and it corresponds to the variation of the potential barrier at the beginning of the channel (Source-channel) in function of the Gate voltage: It is a fundamental parameter for the optimization of the ratio between the saturation current and leakage current [8, 9]. The theoretical limit of this slope is fixed by the diffusion phenomena of the channel charge at  $\ln(10)KT/q=60\text{mV/Decade}$  at 300K.

4. Gate leakage current: the shrink of the gate oxide thickness have been a critical feature of the overall scaling of transistor dimensions for six decades, enabling a continuous speed improvement even as operating voltage decrease. Further scaling down is not possible due to the leakage currents in such thin oxides that reach such a high value as comparable to ON state current causing very high static power dissipation. The Gate leakage current depends on the macroscopic electrical properties of the Gate dielectric whose relation given by Yee-Chia Yeo [10], for the classical direct tunneling regime, is

$$J_G = b \exp(-\alpha f \cdot EOT) \quad (1.18)$$

where  $f = \epsilon_{SiO_2}(m_{eff}\phi_B)^{1/2}$ ,  $m_{eff}$  is the tunneling effective mass of the carriers,  $\phi_B$  is the tunneling barrier height and  $\alpha$  is a constant. Therefore new alternatives have been proposed in order to diminish this leakage current due to the tunneling phenomena through the oxide [11]. As previously said in modern devices, new oxide with higher dielectric constant, known as high-k dielectrics, are used, replacing the standard  $SiO_2$ . These high-k dielectrics allow us to keep the same Capacitance-Voltage characteristics (same  $V_{th}$ , S and commutation time) of  $SiO_2$  and at the same time reduce the Gate leakage current ( $J_G$ ).

## 1.5 State of the art

As previously described, for the microelectronic industry involved in the development of advanced CMOS technology for MOS (metal/Oxide/Semiconductor) transistors, the extraction of EOT (Equivalent oxide thickness) and  $WF_{\text{eff}}$  (effective work function) of the metal gate stack is important. These two parameters are fundamental in order to compare different technologies featuring specific architectures or process technology (fabrication procedure), that are significant for the technology engineers.

The EOT and  $WF_{\text{Eff}}$  extraction from the CV measurements is a well known technique in the state of the art. The book reference on MOS capacitance "MOS (Metal-Oxide-Semiconductor) Physics and Technology" [12] describes this technique in details. For a long time, they proposed analytical methods for the EOT and  $V_{\text{fb}}$  extraction, from the typical points of the CV characteristic (maximum and minimum) or from its derivative. We will find in the article of C. Leroux [13] a review of the different techniques of  $V_{\text{fb}}$  and  $WF_{\text{Eff}}$  extraction based on the analytical relation. In the analytical case, we obtain the oxide capacitance and therefore the equivalent oxide thickness ( $C_{\text{max}} = \epsilon_{\text{SiO}_2} / \text{EOT}$ ), from the maximum value of the experimental C-V characteristic.

This hypothesis is no longer valid for nanometric oxide thicknesses because the thickness, associated to quantum effects (depletion of the free carriers at the semiconductor surface) becomes at the same order of magnitude as the measured oxide thickness. This thickness is known as dark space, whose first appearance is associated with the work of Stern [14] where a study of the inversion charge in the semiconductor is carried out, demonstrating that its barycenter is not anymore close to the oxide-semiconductor surface. We remember that for a silicon oxide the relation between this capacitance ( $C_{\text{ox}}$ ) and the thickness ( $t_{\text{ox}}$ ) is given by the expression  $C_{\text{ox}} = \epsilon_{\text{SiO}_2} / t_{\text{ox}}$  where  $\epsilon_{\text{SiO}_2}$  is the dielectric constant ( $3,9 \cdot 8,85 \cdot 10^{-12}$  F/m).

Therefore, the analytical methods are too approximated for these nanometric oxide. We need to use an appropriate extraction method for the oxide extraction. This is based on comparison between experimental C-V characteristic (Fig. 1.2) and simulation of a MOS gate stack (Fig. 1.7) by tuning the gate stack theoretical parameters (metal work function and oxide thickness and doping level of the semiconductor) in order to reproduce the experimental characteristic. This simulation is taking properly into account the quantum phenomena occurring

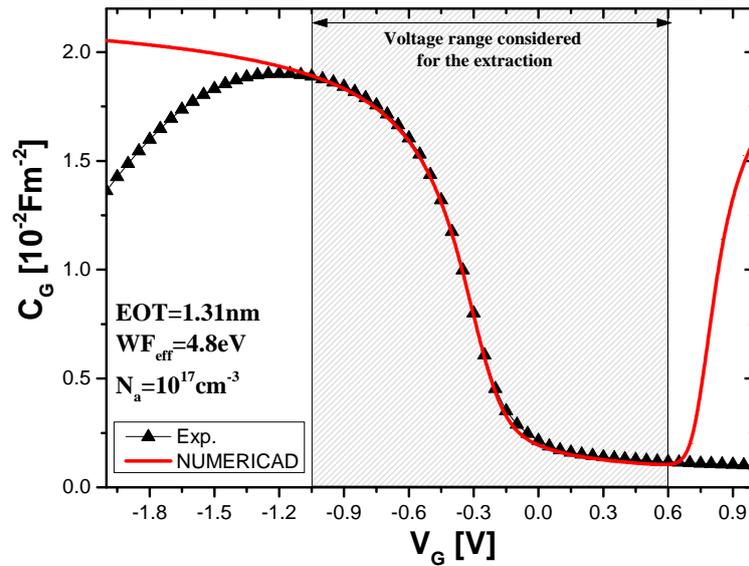


Figure 1.10: Matching between experimental and simulation (solid curve of the type in Figure 1.7) to extract EOT, metal effective work function and semiconductor doping. The voltage range (indicated in gray lines) over which the measurement is considered to be not affected by parasitic phenomena.

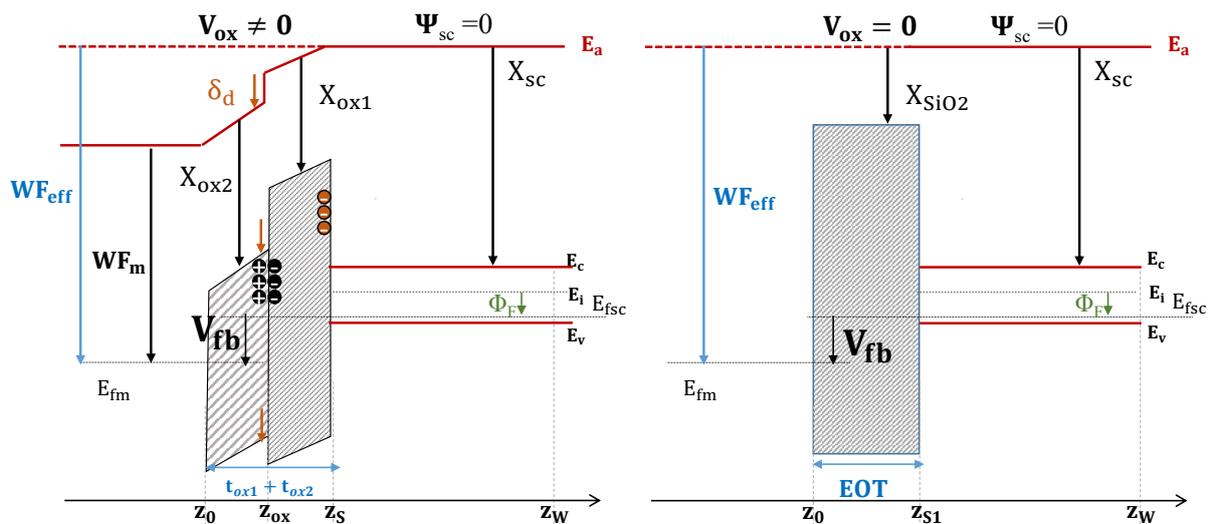


Figure 1.11: Energy band diagrams of a ideal MOS structure at the flat band condition without any oxide charge (right figure) and non-ideal with charges and dipole in the oxide (left figure) reproducing the same Capacitance-Voltage characteristic.

at the oxide/semiconductor interface. The aim is to obtain a matching over a meaningful voltage range and well known in the literature. We report in Figure 1.10 an example of adjustment between the experiment and simulation that allows us to identify the value of EOT ( $t_{ox}$ ) and  $WF_{eff}$ . We notice that for the experimental C-V characteristic we don't obtain the capacitance related to the

substrate inversion for positive voltages contrary to the numerical simulation. As previously said, this difference is related to the fact that for these measurements there is no Source and Drain diffusion which would provide a sufficient amount of minority carriers, able to respond to the AC potential variations applied to the Gate terminal. This new extraction technique needs to solve self-consistently the electrostatic equation (Poisson) and Schrodinger equation that calculates, for a specific potential distribution, the free carrier charge across the gate stack. This simulation leads to the calculation of the potential drop across the semiconductor for a given charge:  $Q_{sc}(\Psi_{sc})$ . Therefore C-V characteristic, for a specific oxide capacitance, can be reproduced by using equation 1.2 and setting the proper material (semiconductor) parameters values: Gate metal, oxide thickness and doping level of the semiconductor substrate without including any oxide dipole or fixed charges. The simulation assumes always an ideal MOS stack. Therefore, the value of the metal work function, used in the simulation, will take into account the oxide defects (fixed charges and dipole) and their electrostatic effect over the stack. In Fig. 1.11 we report the associate band diagrams, at the flat band condition, of the simulation (right side) and the experimental (left side) C-V characteristics reported in Fig 1.10.

These bands diagrams, representing two different stack, lead to the same Capacitance-Voltage characteristics which are respectively reported in Fig. 1.10 (black- triangles experimental and red simulation). Even if they look different, these two band diagrams have the same flat band condition, effective work function and EOT.

The EOT and effective work function  $WF_{eff}$  are defined as the equivalent oxide thickness, in terms of  $SiO_2$  dielectric constant, and metal work function of an ideal Gate stack that reproduces the same electrical Capacitance-Voltage characteristic of a real Gate stack, supposing the same semiconductor doping level and type.

Figure 1.12 reports some examples of gate stack simulations compared with experimental C-V characteristics. If we consider the electrical structure, that we want to simulate, it is composed of a metal, oxide and substrate that features a metal work function ( $WF_M$ , oxide thickness ( $t_{ox}$ ) and a semiconductor work function  $\phi_{sc}$ . As previously seen, it is composed by the series of two capacitances: the dielectric capacitance  $C_{ox}$  and the semiconductor capacitance  $C_{sc}$ . Therefore, if we know the relation between the semiconductor charge  $Q_{sc}$  (Coulomb) and its potential drop  $\Psi_{sc}$  (Volts) we can calculate the semiconductors capacitance

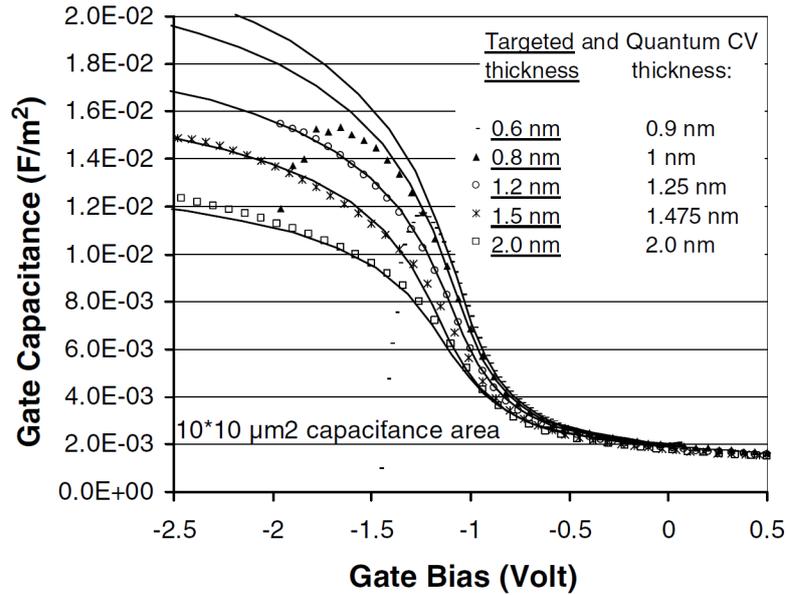


Figure 1.12: Comparison of CV measurements (symbols) and simulation (lines) allowing the extraction of EOT (Quantum CV thickness) and  $V_{fb}$  (not shown in the figure) by fitting the characteristics. It will be noted that according to the characteristics only certain parts of the measurement are reliable (degradation due to tunnel-type leakage currents), according to C.Leroux et al. [15].

$C_{sc} = dQ_{sc} / d\Psi_{sc}$  in order to obtain the total capacitance  $C_g$ .

The equations 1.2, 1.3 and 1.4 allows us to define in a unique way a C-V characteristic for a specific gate stack by setting the proper value of its technological parameters: type of metal ( $WF_m = WF_{eff}$ ), the oxide thickness ( $t_{ox}$  or EOT) and the type of semiconductor (its work function  $WF_{sc}$  and relation between charge and potential:  $\Psi_{sc}(Q_{sc})$ ).

If we use  $V_{fb}$  instead of  $WF_{sc}$ ,  $V_{fb}$ , EOT and  $\Psi_{sc}(Q_{sc})$  defines in a unique way the C-V characteristic from equations 1.2, 1.3 and 1.9. However we notice that the relationship between these equations is complicate and that is not anymore possible to extract independently EOT and  $V_{fb}$ , with respect to the analytical methods.

Let us remember that with analytical methods, EOT is extracted from the maximum capacitance value and then  $V_{fb}$  is extracted from an another relation. By setting these three parameters ( $V_{fb}$ , EOT and  $N_{sc}$ ), we obtain a unique C-V curve. Therefore it's possible to identify, from a given experimental C-V characteristic, by progressive adjustments, this "hat trick" ( $V_{fb}$ , EOT and  $N_{sc}$ ) that performs a simulation that better matches the experiment as reported in Figs.

**1.10 and 1.12.**

Indeed, the EOT plays a fundamental role on the amplitude of the maximum capacitance whereas the doping level  $N_{sc}$  on the minimum value and  $V_{fb}$  on the lateral shift of  $V_G$ . Therefore it's possible to identify  $V_{fb}$  and EOT by simply fitting the experiments with simulation results (Figs. 1.10 and 1.12). The procedure can result complicated and with an uncertainty since lowest time cost (rapidity) is demanded in order to perform statistical analysis over hundreds of devices. This is why, in CEA-LETI laboratory they proposed a new extraction methodology that allows to automatically extract  $V_{fb}$  and EOT from a measured C-V characteristic [16]. The only limitation of this methodology is to identify from the beginning the semiconductor doping, that we consider not variable over all the same set of measurements and to identify the voltage range of the accumulation of the majority carrier for which the measurement is considered reliable. This methodology starts from a quantum simulation of relation  $\Psi_{sc}(Q_{sc})$  for a given substrate and find the proper values of EOT and  $V_{fb}$  for which simulations fits the experimental C-V characteristic, given by the relations 1.2, 1.3 and 1.9. In order to take into account most of the semiconductors based on Silicon technology, C.Leroux proposed to simulate different bars of semiconductor of N and P-type with constant doping concentrations whose values are defined between  $10^{15}\text{cm}^{-3}$  and  $10^{20}\text{cm}^{-3}$  [13]. These hundreds of simulations are sufficient to take into account most of the situations of MOS capacitance with a Silicon substrate. Other works, with respect to C. Leroux and Charbonnier [13, 16, 17], have been proposed in order to extract EOT and  $V_{fb}$ . Despite these attempts, most propose simply to perform specific measurement, or design new specific test structures in order to minimize the parasitic effects on Capacitance-Voltage measurements, but very few on the extraction of EOT and  $V_{fb}$  for FDSOI transistor from the C-V experimental characteristic. For instance, the work of SHARP [18] proposed to add in series a capacitance in order to reduce the leakage current in case of really thin oxide. According to the present work [18], the insulator capacitance analyzer includes a capacitance whose dielectric thickness value can be configured in function of the specific measurement need. The aim is to reduce the leakage effect on the C-V characteristic of the tested transistor. Interesting is the work of AMD [19] who proposes an apparatus and method related to a new test structure for capacitance-voltage (C-V) measurements. This test structure is composed by two transistors in parallel with specific channel lengths. They propose to solve the degradation problems, tunneling of carriers from the inversion layer through

the gate oxide, by reducing the Gate length of each elementary transistor. In the same context, C.Leroux [20] proposed to work on two different test structures (capacitance) and to work on different measurements in order to get rid of the parasitic capacitances. The first test structure is characterized by two parallel transistors with respectively length  $L_1$  and width  $W_1$  for the first transistor  $T_1$  and length  $L_2$  and width  $W_2$  for the second transistors  $T_2$ . The second transistor is a similar test structure but having an inversion of Gate lengths. These are selected so that  $(L_1W_1+L_2W_2)_{T_1}-(L_2W_1+L_1W_2)_{T_1}=(L_1-L_2)(W_2-W_1)=(C_{T_1}-C_{T_2})$ , and so that the surface area difference  $S_{\text{equiv}}$  between the two devices is nonzero. The work defines a test structure which uses differences in dimensions of MOS transistors for cancelling by subtraction the various effects of the parasitic capacitances and of the imprecision in the surface areas of the transistors. The only work that really concerns the EOT and  $V_{\text{fb}}$  extraction, is presented by the SSM [21]. Indeed he proposed a analysis method based on numerical algorithm of capacitance-voltage that aims to automatically extract EOT and  $V_{\text{fb}}$  including quantum effects. This work seems too approximated since he tries to take into account quantum effects with analytical corrections and without using the relation  $\Psi_{\text{sc}}(Q_{\text{sc}})$  that is obtained by a Poisson Schrodinger simulation.

The aim of these works is not to extract the physical dielectric thickness and neither the metal work function but to take into account the dielectric coupling between the metal and semiconductor of a specific technology that we want to characterize as an ideal MOS stack composed by a metal, an dielectric  $\text{SiO}_2$  with a well known dielectric constant value of  $3,9 \cdot 8,85 \cdot 10^{-12} \text{ F/m}^2$  and a semiconductor. The silicon-oxide of this MOS Gate stack is considered as ideal without any fixed charge or dipole at its interface. For a given experimental C-V characteristic extraction of EOT and  $\text{WF}_{\text{eff}}$  means to respectively find the oxide thickness and metal work function of an ideal MOS that has the main electrical behavior of the tested structure. With EOT and  $\text{WF}_{\text{eff}}$ , therefore we define a common language in order to compare different technologies from the point of view of these two keys parameters, able to strongly influence the device electrical behavior. Therefore, these two parameters are considered more universal than the classical parameters as the threshold voltage  $V_{\text{th}}$  or the inversion capacitance at a given voltage (CET). Therefore with CET and  $V_{\text{th}}$  it's complicated to compare two different technologies, CET is dependent on  $V_{\text{th}}$  and  $V_{\text{th}}$  doesn't depend only on the Gate stack technology (dielectric and metal) but also on the substrate and even on its polarization. Moreover, comparing EOT and  $\text{WF}_{\text{eff}}$  of two different technologies allows us to highligh phenomena such

as dielectric growth or electrical shift with respect to the reference polarization (charge inside the dielectric, interface dipole, variation of metal work function, etc...).

## 1.6 EOT and $WF_{eff}$ extraction issues in case of FDSOI transistors

Despite the methodology proposed by C.Leroux et al. [13] is and has been used in a reliable way for standard bulk devices, this isn't anymore the case for the FDSOI technology whose typical structure is reported in Fig. 1.13. The challenge is related to the absence of the flat band voltage  $V_{fb}$  and the associated depletion-accumulation region. The only available C-V characteristic region is the inversion as reported in Figure 1.14. A solution has been proposed to adapt the standard extraction methodology to FDSOI device in order to be reliable and efficient over any region of the characteristic and therefore also in the inversion region [17]. The fitting between simulation and experiment allows to identify EOT and  $V_{fb}$ . From the given  $V_{fb}$  it is possible to calculate the effective work function of the Gate metal stack using equation 1.12.

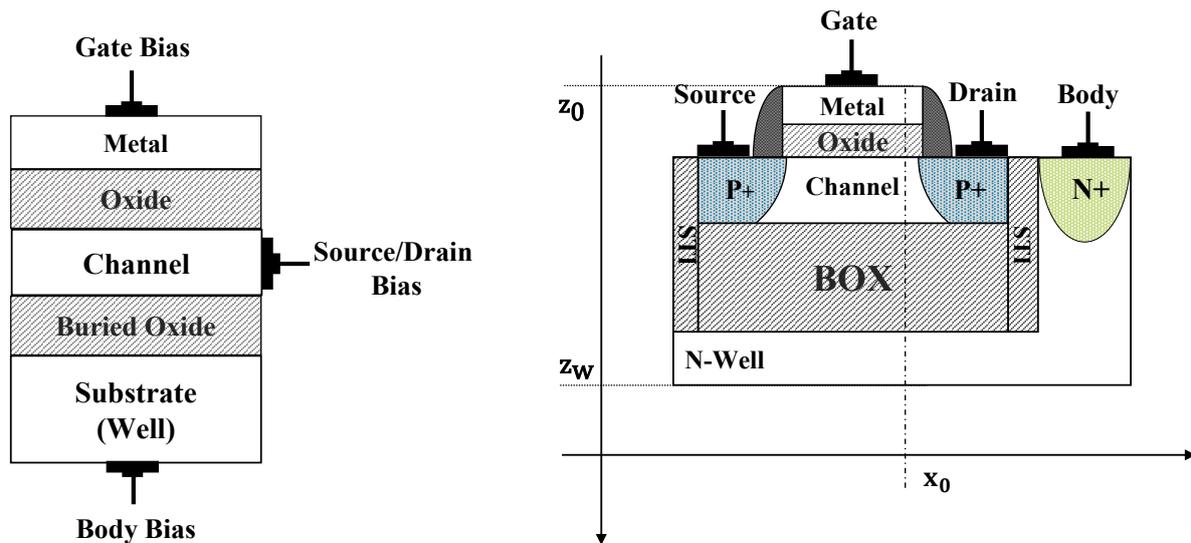


Figure 1.13: Schematic of a FDSOI capacitance.

However an hypothesis on the semiconductor doping level has to be made since a difference between the experimental threshold voltage  $V_{th}$ , that is fitted, and the  $V_{fb}$ , that we want to extract (eq. 1.10), is dependent of the depletion charge that varies with doping level. Therefore, in the work of Charbonnier [17] the doping level is considered negligible with a value of  $10^{15} \text{cm}^{-3}$ . This hypothesis is made for one reason. The FDSOI Gate-to-channel capacitance  $C_{gc}$  doesn't take into account the depletion charge. Indeed, with a standard bulk simulation (Figure 1.7), in case of minimum value of doping level

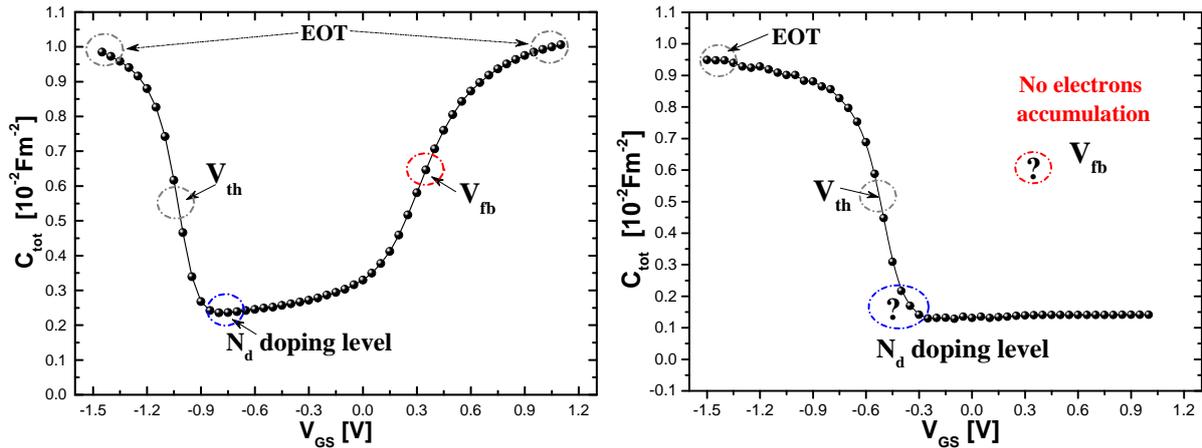


Figure 1.14: Comparison between MOS and FDSOI C-V characteristics.

( $10^{15} \text{cm}^{-3}$ ), the depletion capacitance disappears. Therefore, the only observed capacitance is the inversion and accumulation which looks as a typical FDSOI  $C_{gc}$  characteristic. Other works, with respect to C. Leroux and Charbonnier [17], have been proposed. Indeed, in the past, many studies have been dedicated to develop specific extraction methodologies in order to extract the most relevant parameters in FDSOI structures. In the FDSOI devices, the silicon channel thickness plays a fundamental role in the determination of the main electrical and transport properties of the carriers in the inversion layer. Thus its thickness extraction becomes more and more interesting for the process engineering such as the buried oxide thickness. One of the most representative work is presented by Lim et al. [22] with coupling charge model. In this model front (respectively back) threshold voltage ( $V_t$ ) characteristics as function of the back bias  $V_B$  (respectively  $V_G$ ) are analyzed in order to electrically characterize these structures. In fully depleted devices the width of the depletion region is greater than channel thickness, so that the film can be completely depleted from the front to the back interface. Depending of this thickness, the two interfaces are more or less coupled leading to the interdependence of the front and back threshold voltages [22]. This coupling between the two interfaces can be used to extract the channel thickness [23, 24]. In the work of Cassè et al. [25], the applicability of this methodology is presented for very thin film FDSOI transistors. Indeed in this work it has been proved that for really thin channel thickness the extraction methodology based on the couple charge model lead to a wrong estimation of the channel thickness. They demonstrate that this was due to the influence of the substrate capacitance.

Another main representative work, in the state of the art was presented by

Jian Chen et al. [26]. Indeed, he proposed a specific C-V measurements in order to extract the thicknesses FDSOI stack channel and EOT. This is the Gate-to-Drain-Source capacitance  $C_{GDS}$ , or Gate-to-channel  $C_{gc}$  in our case as previously reported in Fig. 2.16. The principle is to extract the EOT at really strong inversion ( $C_{max} = \epsilon_{fox}/t_{fox}$ ) by neglecting the quantum effects. Whereas the EOT was extracted at the maximum value of  $C_{GDS}$ , the channel thickness was extracted through the back biasing effect on the capacitance characteristics. At specific bias condition, he found that the inversion charge onset occurs at the interface channel-back-oxide. Therefore at this condition while almost all channel is depleted the capacitance seen during the measurement is the series of the front-oxide and channel capacitance that is  $C_{GDS} = C_{fox} // C_{ch}$  form which the extraction of the channel thickness is carried out. Unfortunately this analytical methodology doesn't take into account of the quantum phenomena. Indeed, in case of nanometric thicknesses the inversion layer at the back channel is no longer negligible compared to the depleted channel region. Afterwards other works, proposed for the same aim, were based on Capacitance-Voltage measurements: the split C-V technique in the work of BenAkkez et al. [27], split C-V with back bias modulation and the Gate-to-Body capacitance presented by Shin et al. [28] and MOS gated diode (PIN) based methods reported by Navarro et al. [29, 30]. The aim of all these works was to extract the thicknesses of the FDSOI and especially the channel thickness. Unfortunately these works are not able to extract the effective work function  $WF_{eff}$  of the FDSOI transistors.

Among these works, we previously mentioned a solution proposed by Charbonnier et al. [17] which fits the experimental capacitance  $C_{gc}$  (response of the free inversion carriers) with bulk numerical simulations. However, whereas this solution seems to allow us to identify EOT and  $WF_{eff}$ , this methodology hides difficulties related to the complexity of the FDSOI structure with respect of the standard bulk transistors. Whereas, for standard bulk transistors, the threshold voltage  $V_{th}$  depends only on the semiconductor doping level, metal work function and oxide thickness, for FDSOI transistors the relation between  $V_{th}$  and the FDSOI stack physical parameters is more complex. We remember that the SOI substrate is composed by channel materials stacked on a buried oxide and substrate well layers as reported in Fig. 1.13 which is more complex than the standard bulk substrate composed only by a semiconductor material. The physical parameters of each FDSOI stack layer will affect the threshold voltage.

In a recent work [31], we show, for FDSOI transistors, how can be tedious and difficult the extraction of  $WF_{eff}$  by only fitting the inversion capacitance  $C_{gc}$

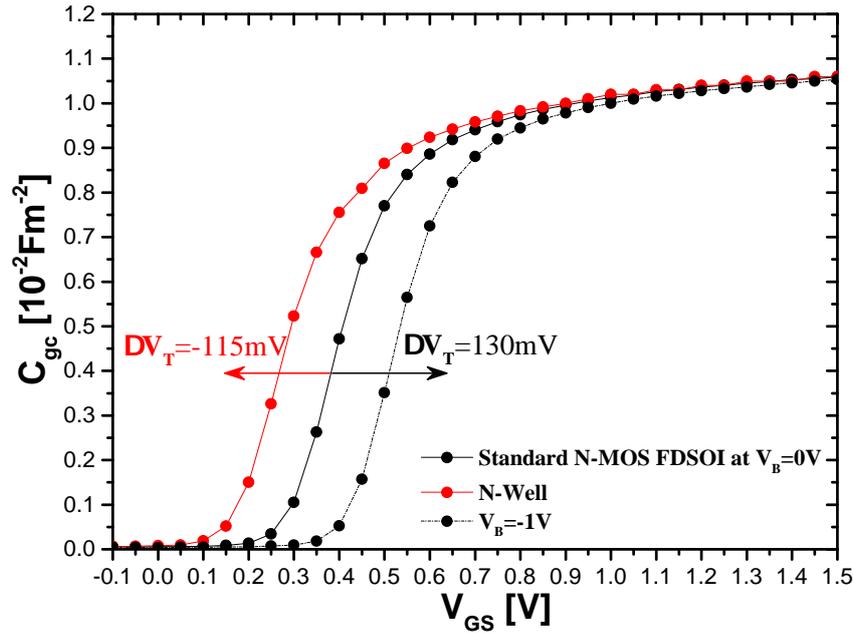


Figure 1.15:  $C_{gc}$  versus  $V_{GS}$  characteristics for two FDSOI devices with a N-well at  $V_B=0V$  (in red) and with a P-well at  $V_B=0V$  and  $-1V$  (in black with big and small circles).

and therefore the threshold voltage  $V_t$  with numerical simulation. Indeed, in Figure 1.15 we report the experimental characteristics for two N-MOS FDSOI transistors featuring the same Gate stack (same EOT and  $WF_{eff}$ ), same channel and buried oxide thicknesses but different substrate (well) types. The standard N-MOS transistor is characterized by a P-type well (in black-circles line) from which the variation of  $V_t$  are calculated. As we can observe, changing the Well doping type (in red) or applying a back  $V_B=-1V$  (in black dashed line) induces respectively a shift of the threshold voltage of  $-115mV$  and  $130mV$  with respect to the reference architecture (Standard N-MOS in black line). The solution proposed by Charbonnier et al. [17], will lead to 3 different effective work function which is not a good result since both transistors has the same Gate stack and therefore EOT and  $WF_{eff}$ . Therefore, the extraction of  $WF_{eff}$  should be independent of well-type or back bias. The proper identification of effective work function  $WF_{eff}$  needs the exact values of the different physical parameters of FDSOI stack. This is not possible with the standard bulk numerical simulation proposed by Charbonnier since the measured C-V characteristic doesn't seem unique for the same Gate stack.

The EOT and  $WF_{eff}$  extraction from the C-V curves faces different obstacles with SOI substrate that are threefold:

- The missing flat band condition and accumulation regime on the C-V characteristics.
- The complex dependence of  $V_{th}$  with the FDSOI stack parameters.
- The necessity to extract the proper physical parameter values of each FDSOI stack layer.

As explained in the previous section, the impact of EOT and  $WF_{eff}$  is fundamental for the bulk technology, in terms of electrical performance. Their extraction is important also for the FDSOI technology. Therefore, the aim of the thesis will be to find new electrical methodologies, based on C-V measurements, in order to extract in reliable and fast way the effective work function and the equivalent oxide thickness, including all the thicknesses of the stack, for thin film FDSOI technology.

Due the huge structural discrepancy between FDSOI and bulk, in next chapter we will introduce the FDSOI technology in terms of geometric structure, we will calculate the electrostatic relations and also the capacitance relations. Moreover, a part of the next chapter will be dedicated to numerical simulations. we will show how to calculate band diagrams, the charge distribution and the electrostatic profile of a specific FDSOI transistor under specific voltage conditions.

## 1.7 Conclusion

In conclusion, the basic principles of a MOS capacitor have been explored. Three main regimes (accumulation, depletion, and inversion) are evidenced and described during C-V measurements.

Impact of Dipole and fixed charges are seen as a possible mechanism in order to tune the electrical performance parameters of the MOS transistors ( $V_{th}$ ).

$WF_{eff}$  and EOT have been introduced as a common language in order to compare different technologies. Specifically,  $WF_{eff}$  takes into account the impact of dipoles and fixed charges induced by process and EOT the innovative technologies (high-k) replacing the reference SiO<sub>2</sub> dielectric.

Most of the FDSOI or bulk performance parameters are strongly influenced by the equivalent oxide thickness (EOT) and the effective work function ( $WF_{eff}$ ).

We have seen that traditional C-V characteristics techniques, in order to extract EOT and  $WF_{eff}$  are adequate for the standard bulk technology but are no longer fitted for FDSOI technology.

New extraction methodology are necessary for FDSOI technology in order to extract  $WF_{eff}$  and EOT.

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# Chapter 2

## FDSOI Electrostatic Modeling and Simulation

### 2.1 Introduction

We saw in the previous chapter that Capacitance-Voltage measurements are used in order to extract EOT and  $WF_{\text{eff}}$ . In case of standard bulk technology, the extraction of these technological parameters are carried out using two main equations which are taking into account the physical phenomena occurring across the transistor stack during C-V measurement. These are the Gate voltage relation,

$$V_G = \frac{WF_m}{q} - \frac{WF_{sc}}{q} + \Psi_{sc} + \frac{Q_{sc}}{C_{ox}} \quad (2.1)$$

and the Gate capacitance relation,

$$\frac{1}{C_g} = \left( -\frac{\partial V_G}{\partial Q_{sc}} \right)^{-1} = \frac{1}{C_{ox}} + \frac{1}{C_{sc}} = \frac{1}{C_{ox}} - \frac{\partial \Psi_{sc}}{\partial Q_{sc}} \quad (2.2)$$

Therefore the experimental C-V characteristic of a specific Gate stack transistor can be predicted using equations 2.1 and 2.2. This prediction is carried out through analytical estimation of the semiconductor electrostatic behavior which is identified as the relation between its charge  $Q_{sc}$  and surface potential  $\Psi_{sc}$ . Indeed, equation 2.1 represents the relationship between the experimental voltage applied at the Gate terminal ( $V_G$ ) and the physical parameters of the Gate stack layers which are defined in the analytical model. This relationship is fundamental in order to carry out the extraction of the transistor technological parameters which passes through the electrostatic modelling of the gate stack behavior.

The huge discrepancy, in terms of design structure, between FDSOI (Fig. 2.1) and the standard bulk technology puts in doubt the validity of the previous relationships (eqs. 2.1 and 2.2) for FDSOI transistors. Therefore in this chapter, Capacitance and Voltage relationships for the FDSOI technology are investigated and obtained through a band diagram analysis. The aim is to find the relations between the experimental Voltage and Capacitance and the relative physical parameters of the FDSOI stack.

Moreover, in the second part of this chapter, a numerical simulation, will be proposed in order to predict the FDSOI electrostatic behavior. This numerical simulation resolves Poisson and Schrodinger equations in a self-consistent way and should allow to better understand the electrostatics of FDSOI structure.

The analytical FDSOI Capacitance-Voltage relationships and the numerical predictive model will lead to understand the electrostatic behavior of the FDSOI transistor but also help to find new methodologies in order to extract the FDSOI technological parameters in the next Chapters. Before to face this analysis, an introduction of the FDSOI technology is proposed with special focus on the description of its structure.

## 2.2 Fully depleted FDSOI Capacitance and Voltage Relationships

### 2.2.1 Introduction to FDSOI technology

The Fully Depleted Silicon thin films technology On Insulator (FDSOI) [1] is one of the major candidates for the future applications. Indeed, its unique and compelling architecture, the SOI substrate, leads to a great improvement of electrostatic behavior and advantage compared to the standard bulk technology [2]. Historically, the SOI substrate has been introduced for spatial application [3], since it showed a higher resistance to the ionizing rays with respect to the silicon substrate. But afterwards the SOI substrate has been employed in different technology applications due to its clear advantages with respect to the substrate technology, that are:

1. BOX (buried oxide): the presence of BOX (Fig. 2.1) leads to a total isolation of the device. There's no current flow coming from the substrate related to other adjacent device whereas this is the case for bulk transistors. The phenomena such as the latch up, well explained in the work of Hargrove et al. [4], is completely absent in case of FDSOI.
2. Electrostatic control: Due to the steeper Source and Drain junctions [5, 6] and smaller depletion region is fixed by the presence of the buried oxide. Moreover the not-doped channel leads to less variability of the technological parameters such as  $V_{th}$ .
3. Fixed depletion region: a smaller depletion region leads as well to a smaller transversal electric field which means a better mobility of the free carriers in the channel and consequently an improvement of the current in saturation regime.

Fig. 2.1 reports on a typical structure of a fully depleted FDSOI MOSFET. As the traditional bulk devices, FDSOI is a four-terminal device: Gate, Source, Drain and Body. The Gate terminal is used to create an inversion charge whose carriers are supplied by Source and Drain wells whereas a drop voltage between the Source and Drain terminals induces a field-effect current. Finally, the Body terminal can be used, in parallel to the Gate terminal, in order to modulate and shift the channel charge and therefore affecting the Source-Drain current. The Body biasing is very limited when used in the bulk technology due to the parasitic

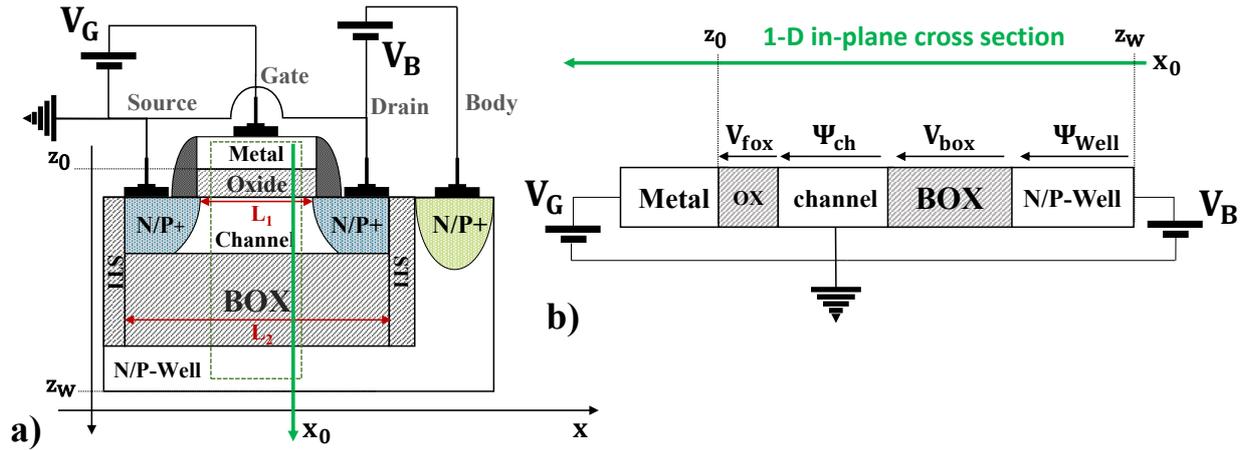


Figure 2.1: a) FDSOI device under biasing (field-effect); b) FDSOI stack under biasing.

current leakage coming from the substrate whereas the FDSOI technology is more efficient due to the presence of the Buried oxide. Moreover, as reported in Fig. 2.1 a (x direction) and b, the presence of a buried oxide (silicon on Insulator SOI) splits the standard bulk substrate in two independent systems (semiconductors): the channel, intentionally not doped and the well. The FDSOI structure is simply an evolution from the standard bulk CMOS process. The FDSOI Gate stack, like the normal bulk transistor, is always a multiple layer structure, composed by the metal, dielectric oxide and channel, whereas Source and Drain are simply ohmic contacts with strongly doped wells (n-type for N-MOS and p-type for P-MOS). The length of the Gate,  $L_1$  in Figure 2.1 a (z direction), is the distance between the Source and Drain terminals whereas the length of the box between the two shallow trench isolations (STI) is  $L_2$ . The width  $W$  is the extension of the transistor, in direction perpendicular to the cross section of Fig. 2.1 a.

### 2.2.2 $V_G$ and $V_B$ voltage relationship in fully depleted FDSOI

The standard Capacitance-Voltage measurements [7] are the main techniques used to determine the electrical properties of bulk and but also of the FDSOI transistors. During these measurements voltages are applied on these four-terminal devices. Four potentials are defined, depending on the terminals: the Gate voltage  $V_G$ , the Source and Drain voltages  $V_S$  and  $V_D$  and finally the Body voltage  $V_B$  (see Fig. 2.1 a). The relationship between these voltages and the physical FDSOI stack parameters will be investigated on the FDSOI transistor. We

remember that the C-V measurements, differently from the current-voltage (I-V) measurements are always performed with  $V_S$  and  $V_B$  at the same potential. Short channel effect (SCE) phenomena, typical of the Drain current measurements, such as Drain induced barrier lowering (DIBL), surface scattering, velocity saturation, impact ionization and hot electron effects [8] are not present during C-V measurements. This leads to consider the channel and the substrate charge uniformly distributed along  $L_1$ ,  $L_2$  and  $W$  (uniform in all the surface  $W*L$ ).

Therefore, for a complete electrostatic description of FDSOI device, a 1-D in-plane cross section, taken from the 2-D structure, as shown in fig. 2.1 a and b, is sufficient. In these configurations, the FDSOI Source and Drain contacts are grounded, the Gate terminal is biased at  $V_G$  potential and finally the Body terminal at  $V_B$  potential. The purpose is to find the relation between the  $V_G$  and  $V_B$  potentials and the relative potential drops across the FDSOI stack (Fig. 2.1.b), including the physical parameters.  $V_{fox}$ ,  $\Psi_{ch}$ ,  $V_{box}$  and  $\Psi_{Well}$  are respectively the potential drops across the front-oxide, channel, back-oxide (or buried oxide) and well substrate.

This relationship between  $V_G$  and  $V_B$  depends on the electrical interaction between the different layers composing the FDSOI stack. The energies bands of the different layers are reported in Fig. 2.2 respectively to the vacuum Energy level ( $E_a$ ).  $WF_m$  and  $E_{fm}$  are the metal work function and Fermi energy level of the metal.  $X_{fox}$ ,  $X_{ch}$ ,  $X_{box}$ ,  $X_{Well}$  are the electron affinities of the front-oxide, channel, back-oxide and Well layers and  $E_{gfox}$ ,  $E_{gch}$ ,  $E_{gbox}$ ,  $E_{gW}$  are the corresponding energy gaps. Finally,  $E_{fch}$  and  $E_{fW}$  are the Fermi energy levels of the channel and well layers.

In case of fully-depleted FDSOI, due to the low channel doping level and nanometric channel thickness ( $t_{ch}$ ), the channel is always fully depleted. This occurs when  $t_{ch} < 2x_{dep\ max}$ , as reported in the work of Hyung-Kyu Lim and J. G. Fossum [9], where  $x_{dep\ max}$  is the maximum depletion region in the channel. The condition comes out from possibility of a simultaneous appearance of this depletion region from the back and front interface oxide-channel due to the interaction between the metal-channel and the metal-well systems. Therefore direct and correlated interaction between metal and well system occurs. The electrical interaction between the layers causes a band bending of all the entire system as reported in Fig. 2.3. The applied voltages  $V_G$  and  $V_B$  induce respectively a difference of the Fermi energy levels between channel and metal systems and channel and well systems. Specifically, the relation between  $V_G$  and  $V_B$  and the

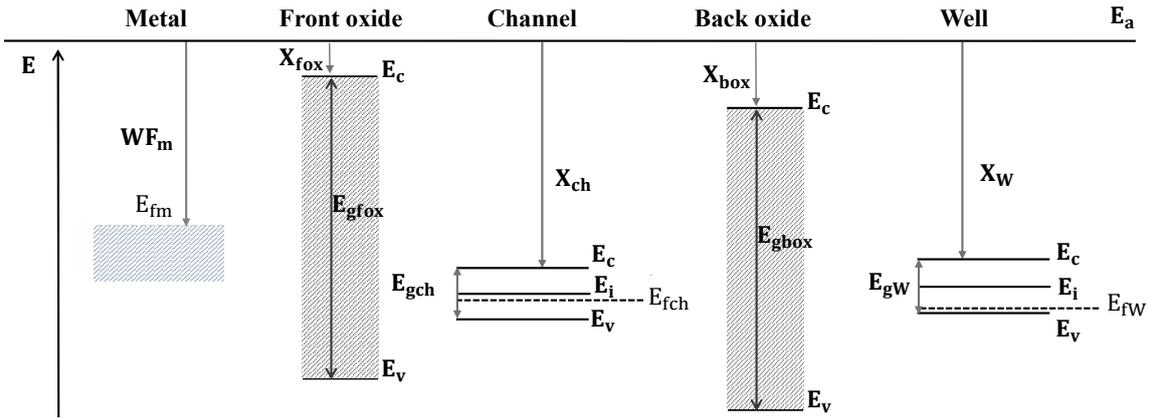


Figure 2.2: Energies band diagrams of the FDSOI stack layers before interaction: Metal, front oxide, back oxide and Well substrate.

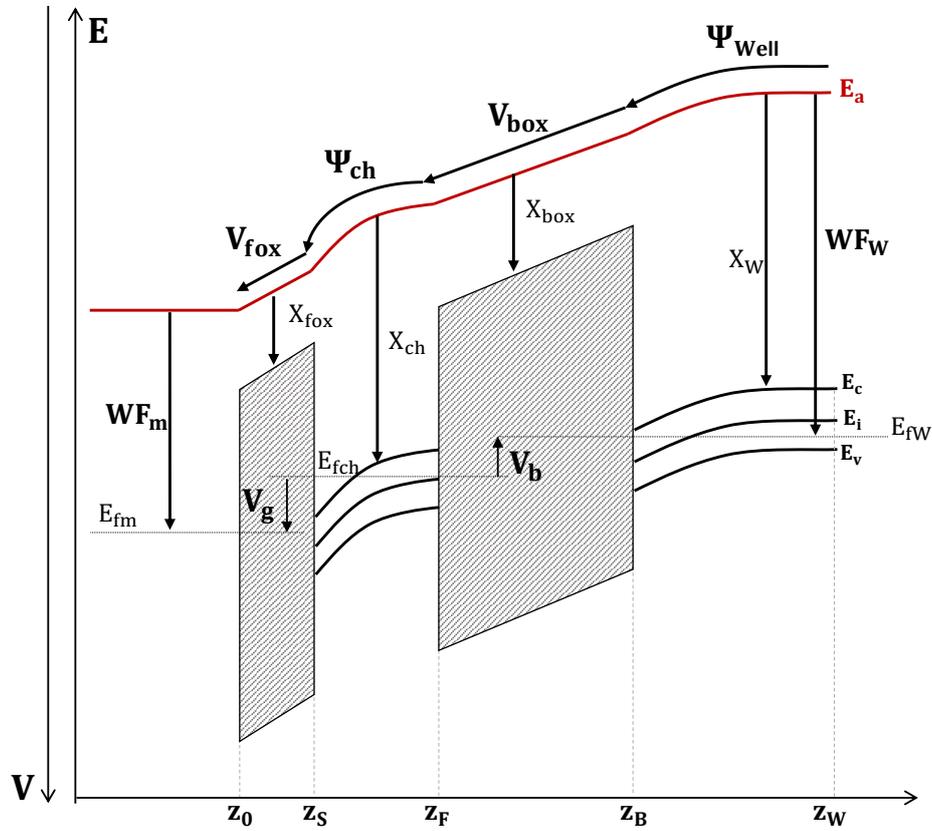


Figure 2.3: Band Energies after interaction.

Fermi energy of the metal, channel and well systems are

$$V_G = \frac{E_{fch} - E_{fm}}{q} \quad (2.3)$$

and

$$V_B = \frac{E_{fch} - E_{fw}}{q} \quad (2.4)$$

where  $q$  is the electron charge. The channel Fermi energy is fixed and it is the reference energy level of the electrons in the entire system. From the band diagrams of Fig. 2.3, we can easily determine the electrostatic relation between these potential differences and the potential drops across the FDSOI stack. Indeed, from equations 2.3 and 2.4, since we have

$$V_G - V_B = \frac{E_{fW} - E_m}{q} \quad (2.5)$$

we can find that

$$V_G - V_B = \frac{WF_{fm}}{q} + V_{fox} + \Psi_{ch} + V_{box} + \Psi_{well} - \left( \frac{X_W}{q} + \frac{E_{cW} - E_{fW}}{q} \right) \quad (2.6)$$

The last term in bracket, of the equation 2.6, is known as the well work function potential. It is defined in the neutral N-type well region ( $z_W$ ). It is reported in Fig. 2.3 and is defined as the difference between the vacuum energy  $E_a$  and well Fermi energy  $E_{fW}$ . It can also be related to well doping level  $N_W$  using Boltzmann law, leading to

$$\phi_W = \frac{WF_W}{q} = \frac{X_W}{q} + \frac{E_{cW} - E_{fW}}{q} = \frac{X_W}{q} - KT \lg \left( \frac{N_{dW}}{N_c} \right) \quad (2.7)$$

whereas for P-type well, it becomes

$$\phi_W = \frac{X_W}{q} + \frac{(E_{cW} - E_{vW}) + (E_{vW} - E_{fW})}{q} = \frac{X_W}{q} + \frac{E_{gW}}{q} + KT \lg \left( \frac{N_{aW}}{N_v} \right) \quad (2.8)$$

$N_{aW}$  and  $N_{dW}$  are the well doping concentration level for acceptor (P-type) and donor (N-type) and  $N_v$  and  $N_c$  are the 3-D effective densities of states for the conduction and valence bands. Finally  $K$  and  $T$  are the Boltzmann constant and the temperature expressed in Kelvin. By defining the difference between the metal and well work function potential as

$$\phi_{mW} = \frac{WF_{fm}}{q} - \phi_W \quad (2.9)$$

we obtain from equation 2.6:

$$V_G - V_B = \phi_{mW} + V_{fox} + \Psi_{ch} + V_{box} + \Psi_{well} \quad (2.10)$$

where the channel potential drop is

$$\Psi_{\text{ch}} = \Psi_{\text{ch}}(z_S) - \Psi_{\text{ch}}(z_F) \quad (2.11)$$

and the well potential drop

$$\Psi_W = \Psi_W(z_B) - \Psi_W(z_W). \quad (2.12)$$

As reported in Fig. 2.4, in the equation 2.10,  $V_{\text{fox}}$  and  $V_{\text{box}}$  can be related to the charges in the channel, well and metal ( $Q_{\text{ch}}$ ,  $Q_W$  and  $Q_m$ ) with:

$$Q_{\text{ch}} = \int_{z_S}^{z_F} \rho(z) dz \quad (2.13)$$

$$Q_W = \int_{z_B}^{z_W} \rho(z) dz \quad (2.14)$$

where  $\rho(z) = q(p(z) - n(z) + N_d(z) - N_a(z))$  is the carrier concentrations across the FDSOI stack.  $p(z)$  and  $n(z)$  are the free carriers densities and  $N_d(z)$  and  $N_a(z)$  are the doping concentrations along  $z$  direction.

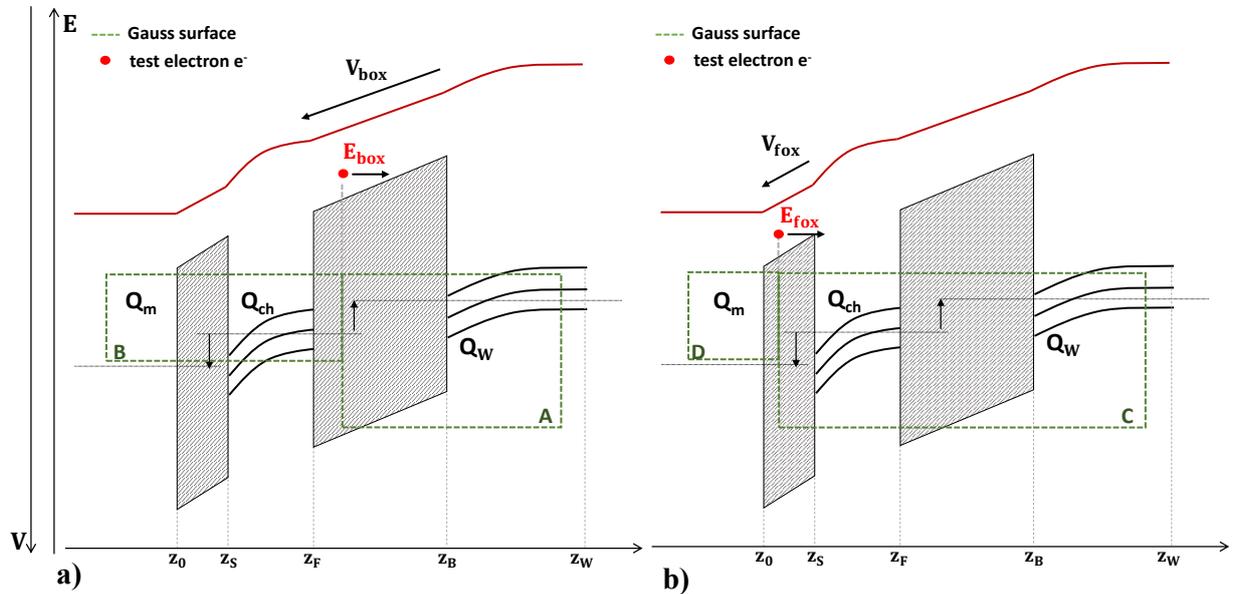


Figure 2.4: Band Energies with the relative charge across the FDSOI stack after interaction.

The total charge of FDSOI system is neutral, that means

$$Q_m + Q_{\text{ch}} + Q_W = 0 \quad (2.15)$$

The calculation of  $V_{\text{fox}}$  and  $V_{\text{box}}$  can be calculated through Gauss law since these potentials are related to the electric fields induced by the charges of the FDSOI system. Indeed we can calculate the electric field in the front-oxide and back-oxide using Gauss law. We remember that in case of an infinite plane sheet of charge, the field is independent of the distance from the sheet. This result is valid also for two infinite plane sheets of opposite charges separated by a distance  $d$ . It is the case of a parallel plate capacitor. The electric field between these two infinite plates is independent of the position between them ( $0 < x < d$ ) and perpendicular to the plate. An 'infinite' plate is an idealization. Indeed in real parallel plate capacitors, the plate has a finite dimension and Surface ( $S=L \cdot W$ ). However, the result of constant and perpendicular electric field holds as long as the distance between the two plates ( $d$ ) is lower with respect to the dimension of the plates itself ( $L$  and  $W$ ). These assumptions are valid also for the electric field of the front oxide ( $\vec{E}_{\text{fox}}$ ) and back-oxide ( $\vec{E}_{\text{box}}$ ) in  $z$  direction as reported in Fig. 2.4 a and b.

Indeed in the FDSOI transistor, the parallel plates are respectively the metal, channel and well material which are separated by a distance  $t_{\text{fox}}$  (between metal and channel) and  $t_{\text{box}}$  (between channel and well). The dimension of these surface "plates" ( $L_1$ ,  $L_2$  and  $W \simeq 10$  micrometers)) which are perpendicular to  $z$  direction are high compared to distance between them ( $t_{\text{fox}} \simeq 1-3$  nm and  $t_{\text{box}} \simeq 20$ nm) Therefore, the assumption of constant electric fields independent of  $z$  in the front and back oxide regions is valid. These front and back-oxide electric fields can be calculated by selecting appropriate Gauss surfaces (1<sup>st</sup> A and B in fig. 2.4 a and C and D in fig. 2<sup>nd</sup> b). An electron placed in the back-oxide, as reported in Fig. 2.4 a, will feel the effect of two main electric fields (A and B surfaces). Therefore the back-oxide electric field is sum of these two contributions, that are:

$$\vec{E}_{1\text{box}} = \frac{Q_{\text{W}}}{2\epsilon_{\text{box}}} \quad (2.16)$$

and

$$\vec{E}_{2\text{box}} = -\frac{Q_{\text{ch}} + Q_{\text{m}}}{2\epsilon_{\text{box}}} \quad (2.17)$$

Since  $Q_{\text{W}} = -Q_{\text{m}} - Q_{\text{ch}}$  (equation 2.15), from equations 2.16 and 2.17 we find that

$$\vec{E}_{\text{box}} = \vec{E}_{1\text{box}} + \vec{E}_{2\text{box}} = \frac{Q_{\text{W}}}{\epsilon_{\text{box}}} \quad (2.18)$$

An electron test charge placed in the front-oxide conduction band, as reported in Fig. 2.4 b, will feel as well the effect of two main electric fields (C and D surfaces)

that are:

$$\vec{E}_{1\text{fox}} = \frac{Q_{\text{W}} + Q_{\text{ch}}}{2\epsilon_{\text{fox}}} \quad (2.19)$$

and

$$\vec{E}_{2\text{fox}} = -\frac{Q_{\text{m}}}{2\epsilon_{\text{fox}}} \quad (2.20)$$

Since  $Q_{\text{m}} = -Q_{\text{W}} - Q_{\text{ch}}$ , we find that the total electric field, in this region, is given by

$$\vec{E}_{\text{fox}} = \vec{E}_{1\text{fox}} + \vec{E}_{2\text{fox}} = \frac{Q_{\text{W}} + Q_{\text{ch}}}{\epsilon_{\text{fox}}} \quad (2.21)$$

From these electric fields (equations 2.18 and 2.21), we can easily obtain the relative potential drops as

$$V_{\text{box}} = -\int_{z_{\text{F}}}^{z_{\text{B}}} E_{\text{box}} dz = -\int_{z_{\text{F}}}^{z_{\text{B}}} \frac{Q_{\text{W}}}{\epsilon_{\text{box}}} dz = -\frac{Q_{\text{W}}}{\epsilon_{\text{box}}} t_{\text{box}} = -\frac{Q_{\text{W}}}{C_{\text{box}}} \quad (2.22)$$

and

$$V_{\text{fox}} = -\int_{z_0}^{z_{\text{S}}} E_{\text{fox}} dz = -\int_{z_0}^{z_{\text{S}}} \frac{Q_{\text{W}} + Q_{\text{ch}}}{\epsilon_{\text{fox}}} dz = -\frac{Q_{\text{W}} + Q_{\text{ch}}}{\epsilon_{\text{fox}}} t_{\text{fox}} = -\frac{Q_{\text{W}} + Q_{\text{ch}}}{C_{\text{fox}}} \quad (2.23)$$

where  $t_{\text{box}}$  and  $t_{\text{fox}}$ ,  $C_{\text{box}} = \frac{\epsilon_{\text{box}}}{t_{\text{box}}}$  and  $C_{\text{fox}} = \frac{\epsilon_{\text{fox}}}{t_{\text{fox}}}$  are respectively the back and front-oxide thickness and capacitance. From equations 2.22, 2.23 and 2.10 we obtain the final relation for the front, that is

$$V_{\text{G}} - V_{\text{B}} = \phi_{\text{mW}} - \frac{Q_{\text{W}} + Q_{\text{ch}}}{C_{\text{fox}}} + \Psi_{\text{ch}} - \frac{Q_{\text{W}}}{C_{\text{box}}} + \Psi_{\text{Well}} \quad (2.24)$$

By simply changing the sign of equation 2.24 and replacing  $Q_{\text{W}}$  with  $-Q_{\text{m}} - Q_{\text{ch}}$  we obtain the relation for back side, that is

$$V_{\text{B}} - V_{\text{G}} = \phi_{\text{Wm}} - \frac{Q_{\text{m}}}{C_{\text{fox}}} - \Psi_{\text{ch}} - \frac{Q_{\text{m}} + Q_{\text{ch}}}{C_{\text{box}}} - \Psi_{\text{Well}} \quad (2.25)$$

where  $\phi_{\text{Wm}} = \phi_{\text{W}} - \phi_{\text{m}}$ .

The relations 2.24 and 2.25 are not totally different from the standard MOS relation. From these equations, by defining an equivalent potential substrate as

$$\Psi_{\text{sc}} = \Psi_{\text{ch}} - \frac{Q_{\text{W}}}{C_{\text{box}}} + \Psi_{\text{Well}} \quad (2.26)$$

and an equivalent substrate (or total) charge as

$$Q_{\text{sc}} = Q_{\text{W}} + Q_{\text{ch}} \quad (2.27)$$

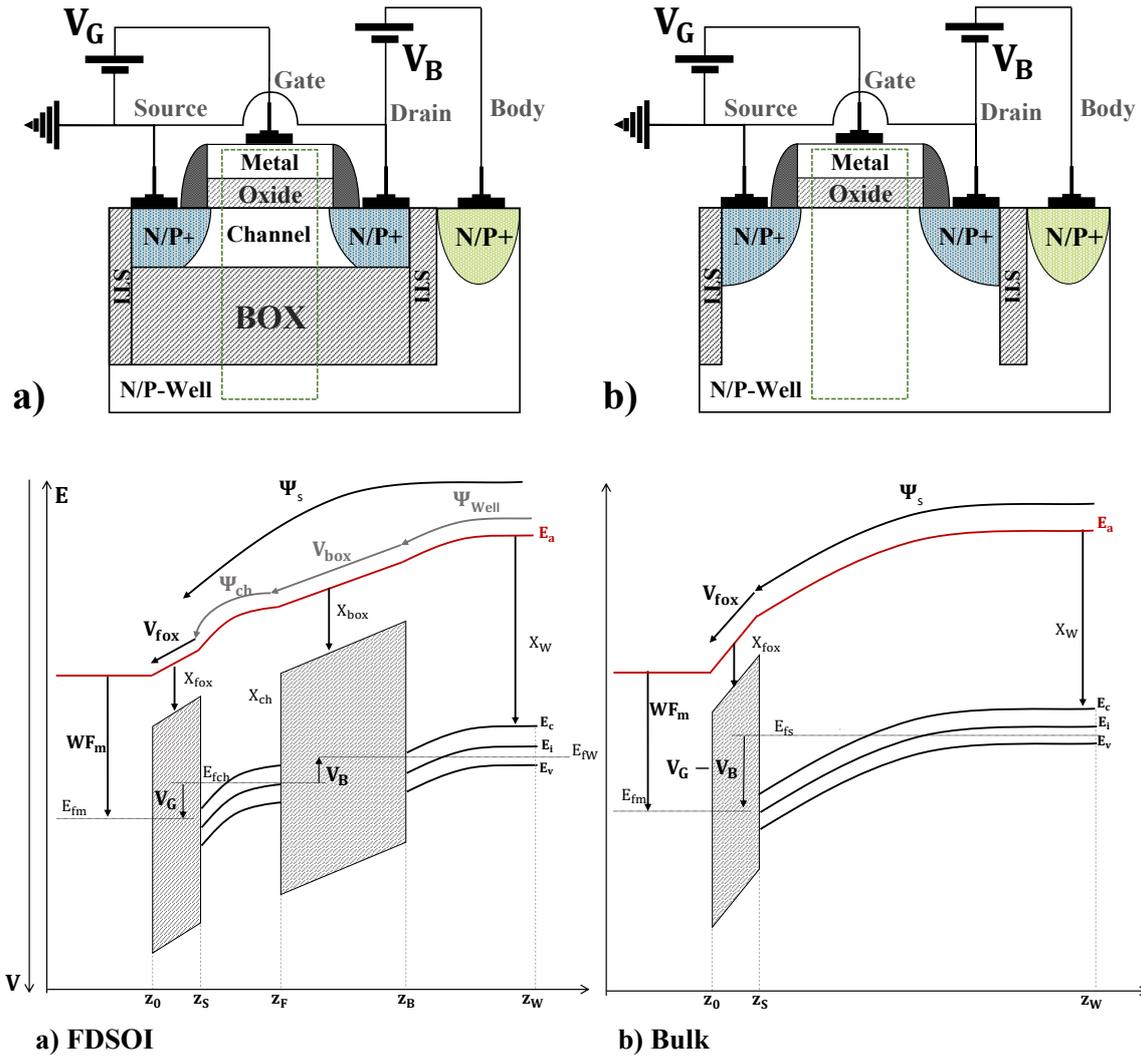


Figure 2.5: Band Energies after interaction for a MOS and FDSOI transistor.

we obtain that

$$V_G - V_B = \phi_{mW} - \frac{Q_{sc}}{C_{fox}} + \Psi_{sc} \quad (2.28)$$

This is the typical MOS electrostatic relation as reported in Fig. 2.5 b, where structure and band diagrams are shown with respect to the FDSOI device (Fig. 2.5 a). Despite this illusory similarity, significant differences are observed that are

- $\Psi_{sc}$  for standard MOS transistor is simply the semiconductor potential drop whereas for FDSOI transistors (eq. 2.26) represents the sum of the all potential drops across the FDSOI stack ( $\Psi_{ch} + V_{box} + \Psi_{Well}$ ).

- $Q_{sc}$  for standard MOS transistor is the total semiconductor charge whereas for FDSOI transistors (eq. 2.26) is the sum of the well and channel charges.
- The impact of  $V_B$  on the charge versus  $V_{GS}$  characteristic (Fig. 1.8) is different for bulk and FDSOI transistor: in case of bulk we have a simple shift  $Q_{sc}(V_{GS}, V_B) = Q_{sc}(V_{GS} - V_B)$  whereas in case of FDSOI transistor we have that  $Q_{sc}(V_{GS}, V_B) \neq Q_{sc}(V_{GS} - V_B)$ .

We can conclude that the relation between the experimental  $V_G$  and the physical parameters of the FDSOI transistor stack (eq. 2.24) is more complicated than the standard bulk relation (eq. 2.1). This is due to the dependence of  $V_G$  with multiple physical parameters associated to the channel, buried oxide and substrate well. Therefore the extraction of EOT and  $WF_{eff}$  has to take into account these dependencies and the proper physical parameters values of all the FDSOI stack layers.

### 2.2.3 FDSOI Capacitance relationship

From the voltages relations (eqs. 2.24 and 2.25) previously obtained we can easily calculate the capacitance relations and therefore find the dependence of the experimental capacitance with the physical parameters of the FDSOI stack. As previously observed, the capacitance relationship for a traditional MOS transistor is obtained through the definition of the total capacitance with respect to the Gate voltage and therefore the variation of the substrate charge with respect of the Gate Voltage ( $dV_G/Q_{sc}$ ). Compared to the standard MOS transistors, the presence of the buried oxide plays a fundamental role, not only on the relation  $\Psi_{sc}(Q_{sc})$ , but as well on the capacitance characteristics of the FDSOI devices since  $C_{sc}$  is affected. The presence of the buried oxide splits the substrate system in two systems, channel and well. Therefore, it is more interesting to define capacitances with respect to the channel and well charges than all the system charge ( $Q_{sc} = Q_{ch} + Q_{well}$ ). The aim of this chapter is to define from an analytical point of view, the expression of the different accessible capacitances of a FDSOI device without explaining how the associate experimental measurements are practically carried out.

We have seen that, for the traditional MOS transistors, the gate capacitance is defined as  $C_g = -\partial Q_{sc} / \partial V_G$ . From this definition and eq. 2.1 we obtain the bulk capacitance relation defined with respect to the Gate potential (eq. 2.2). Now,

in a MOS transistor, the electrostatic condition of  $V_G$  at specific potential and  $V_B=0V$  is the same of having  $V_G=0$  and  $V_B=-V_G$ . We remember that at this specific electrostatic condition we have  $Q_{sc}=-Q_m$  where  $Q_m$  is the metal charge. Therefore if we define the body capacitance  $C_b$  as  $-\partial Q_m/\partial V_B$  which is defined with respect to the Body potential, we can easily prove that the Body capacitance is identical to the Gate capacitance. Indeed we have

$$\frac{1}{C_b} = \left( -\frac{\partial V_B}{\partial Q_m} \right)^{-1} = \left( -\frac{\partial V_G}{\partial Q_{sc}} \right)^{-1} = \frac{1}{C_g} \quad (2.29)$$

Therefore, in the traditional MOS transistors, defining the capacitances with respect to the Gate and Body potentials leads to the same capacitance relation (eq. 2.2). Contrary to the bulk transistor, this is not longer true for FDSOI devices, whose structure is characterized by 3 electrodes (metal, channel and substrate) and 2 dielectrics (FOX and BOX), The effects of  $V_G$  and  $V_B$  on the FDSOI stack charges is different and depend on the stack technological parameters such as BOX and FOX thicknesses and therefore their capacitances. The FDSOI capacitances will depend, during the C-V measurement, on the applied voltage ( $V_G$  or  $V_B$ ).

From the relations 2.24 and 2.25, we can calculate different capacitances associated to the relative FDSOI stack charges related to the separated well and channel material layers. These capacitances are defined with respect to the variation of the Gate potential ( $V_G=V_{G\text{ static}}+v_g(t)$ ) or with respect to the variation of the back-Gate (or Body) potential ( $V_B=V_{B\text{ static}}+v_b(t)$ ). The capacitances defined with respect to the Gate voltage are called as "front" capacitances, whereas the capacitances defined with respect to the Body voltage are called as "back" capacitances. Two "front" capacitances can be identified. The first "front" capacitance is the Gate-to-channel capacitance, experimentally introduced by Yuan et al. [10]. It is defined as the variation of the channel charge with respect to the Gate voltage whose relation is

$$C_{gc}(V_G, V_B) = -\frac{\partial Q_{ch}(V_G, V_B)}{\partial V_G} \quad (2.30)$$

Another definable "front" capacitance is the Gate-to-Body capacitance, whose first appearance is reported in the work of Shin et al. [11]. It is defined as the variation of the well charge with respect of the Gate voltage, which can be

formulated in the following way:

$$C_{gb}(V_G, V_B) = -\frac{\partial Q_W(V_G, V_B)}{\partial V_G} \quad (2.31)$$

The relation between these "front" capacitances ( $C_{gc}$  and  $C_{gb}$ ) and the front-oxide, channel, back-oxide and Well capacitances can be easily derived by calculating the derivative of 2.24 with respect to  $Q_{ch}$  and  $Q_W$  charges.

From 2.24 we find that the derivative with respect to  $Q_{ch}$ , including multiplication by -1 of both side of the equation, is

$$-\frac{\partial V_G}{\partial Q_{ch}} = \frac{\partial Q_W}{\partial Q_{ch}} \frac{1}{C_{fox}} + \frac{\partial Q_{ch}}{\partial Q_{ch}} \frac{1}{C_{fox}} - \frac{\partial \Psi_{ch}}{\partial Q_{ch}} + \frac{\partial Q_W}{\partial Q_{ch}} \frac{1}{C_{box}} - \frac{\partial \Psi_{well}}{\partial Q_{ch}} \quad (2.32)$$

and by defining the channel capacitance as

$$\frac{1}{C_{ch}} = -\frac{\partial \Psi_{ch}}{\partial Q_{ch}} \quad (2.33)$$

, the well capacitance as

$$\frac{1}{C_{well}} = -\frac{\partial \Psi_{well}}{\partial Q_W} \quad (2.34)$$

and the new parameter  $\alpha$ , which relates the variation of the well charge with respect to the variation of channel charge, as

$$\alpha = \frac{\partial Q_W}{\partial V_G} \cdot \left( \frac{\partial Q_{ch}}{\partial V_G} \right)^{-1} = \frac{\partial Q_W}{\partial Q_{ch}} \quad (2.35)$$

equation 2.32 becomes

$$\frac{1}{C_{gc}} = \frac{1}{C_{fox}} + \frac{1}{C_{ch}} + \alpha \left( \frac{1}{C_{fox}} + \frac{1}{C_{box}} + \frac{1}{C_{well}} \right) \quad (2.36)$$

For what concerns the Gate-to-Body capacitance, we know that, from equations 2.30 and 2.31,  $C_{gb} = \alpha \cdot C_{gc}$ . Therefore from equation 2.36 we obtain

$$\frac{1}{C_{gb}} = \frac{1}{C_{cg} \cdot \alpha} = \frac{1}{C_{fox}} + \frac{1}{C_{box}} + \frac{1}{C_{well}} + \alpha^{-1} \left( \frac{1}{C_{fox}} + \frac{1}{C_{ch}} \right) \quad (2.37)$$

Due to the particular and compelling structure, in a FDSOI device, we can access to two others capacitances: the "back" capacitances which are defined with respect to the Body voltage ( $V_B = V_{B \text{ static}} + v_b(t)$ ). The first, the Back-Gate-to-Channel

capacitance, is defined as the variation of the channel charge with respect to the Body voltage, that is

$$C_{bc}(V_G, V_B) = -\frac{\partial Q_{ch}(V_G, V_B)}{\partial V_B} \quad (2.38)$$

and second, the Back-Gate-to-Gate (or Body-to-Gate) capacitance, is defined as the variation of the metal charge always with respect to the Body Voltage, that is

$$C_{bg}(V_G, V_B) = -\frac{\partial Q_m(V_G, V_B)}{\partial V_B} \quad (2.39)$$

As previously done, we can find the relation between these capacitances and the FDSOI stack capacitances, by calculating the derivative of the equation 2.25 with respect to the channel and metal charges and including multiplication by -1 of both side of the equation. Indeed, we find that

$$-\frac{\partial V_B}{\partial Q_{ch}} = \frac{\partial Q_m}{\partial Q_{ch}} \frac{1}{C_{fox}} + \frac{\partial \Psi_{ch}}{\partial Q_{ch}} + \frac{\partial Q_{ch}}{\partial Q_{ch}} \frac{1}{C_{box}} + \frac{\partial Q_m}{\partial Q_{ch}} \frac{1}{C_{box}} + \frac{\partial \Psi_{well}}{\partial Q_{ch}} \quad (2.40)$$

By defining the new parameter  $\beta$ , which relates the variation of the metal charge with respect to the variation of channel charge, as

$$\beta = \frac{\partial Q_m}{\partial V_B} \cdot \left( \frac{\partial Q_{ch}}{\partial V_B} \right)^{-1} = \frac{\partial Q_m}{\partial Q_{ch}} \quad (2.41)$$

and considering equations 2.34, 2.35) and that channel capacitance is defined as eq. 2.33 but with positive sign, we obtain

$$\frac{1}{C_{bc}} = \frac{1}{C_{ch}} + \frac{1}{C_{box}} + \beta \left( \frac{1}{C_{fox}} + \frac{1}{C_{box}} \right) + \frac{-\alpha}{C_{well}} \quad (2.42)$$

From 2.42, since  $C_{bg} = \beta \cdot C_{bc}$ , we can easily calculate the Back-Gate-to-Gate capacitance as

$$\frac{1}{C_{bg}} = \frac{1}{C_{bc}\beta} = \beta^{-1} \left( \frac{1}{C_{ch}} + \frac{1}{C_{box}} \right) + \frac{1}{C_{fox}} + \frac{1}{C_{box}} + \frac{-\alpha\beta^{-1}}{C_{well}} \quad (2.43)$$

These capacitance relations can be summarized in matrix form as

$$\begin{bmatrix} C_{gc}^{-1} \\ C_{gb}^{-1} \\ C_{bc}^{-1} \\ C_{bg}^{-1} \end{bmatrix} = \begin{bmatrix} 1 + \alpha & 1 & \alpha & \alpha \\ 1 + \alpha^{-1} & \alpha^{-1} & 1 & 1 \\ \beta & 1 & 1 + \beta & -\alpha \\ 1 & \beta^{-1} & 1 + \beta^{-1} & -\alpha\beta^{-1} \end{bmatrix} \cdot \begin{bmatrix} C_{fox}^{-1} \\ C_{ch}^{-1} \\ C_{box}^{-1} \\ C_{well}^{-1} \end{bmatrix} \quad (2.44)$$

We remember that  $C_{ch}$  is defined as  $-\partial Q_{ch}/\partial \Psi_{ch}$  for the "front" capacitances relationships whereas for the "back" capacitances relationships it is defined as  $+\partial Q_{ch}/\partial \Psi_{ch}$ . This difference in sign is related to the definition of the channel potential drop in equation 2.11. A positive variation of the Gate voltage will induce a positive variation of the channel potential whereas a positive variation of the Body voltage will induce a negative variation. In fig.2.6, we report the schemes of these capacitances. As we can notice we can relate the front ( $C_{gc}$  and

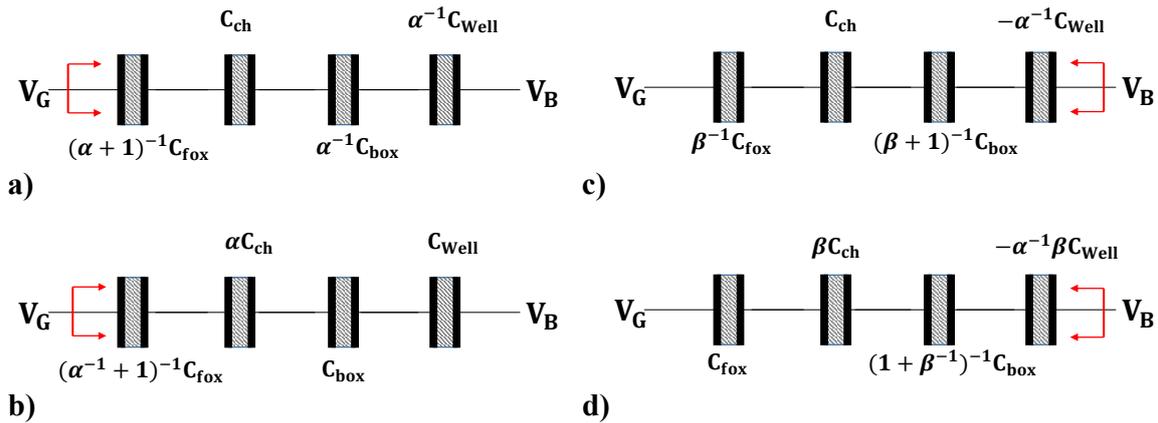


Figure 2.6: Schemes related to the FDSOI device stack capacitance, of  
a)  $C_{gc}$  b.)  $C_{gb}$  c)  $C_{bc}$  d)  $C_{bg}$

$C_{gb}$ ) and back capacitances ( $C_{bc}$  and  $C_{bg}$ ) with the FDSOI stack capacitance ( $C_{fox}$ ,  $C_{ch}$ ,  $C_{box}$ ,  $C_{well}$ ) with only two parameters that are  $\alpha$  and  $\beta$ . These parameters are new compared to the standard bulk transistor since the FDSOI transistors feature two separated material layer that are well and channel whose charge depends on the applied voltages  $V_G$  and  $V_B$ . Therefore,  $\alpha$  and  $\beta$  parameters are fundamentals in order to understand the behavior of the FDSOI charges (metal, channel and well) and therefore the electrostatic behavior of the FDSOI stack (operation regime) during Capacitance-Voltage measurement. These capacitance expressions are reported for the first time and they will be used in detail in the next chapters in order to propose new extraction methodology for FDSOI stack during C-V measurement. Moreover, these capacitance expressions are similar to the capacitance relationship of the standard bulk transistor capacitance (see eq. 2.2).

## 2.3 FDSOI numerical simulation

### 2.3.1 Introduction

The relations between the capacitances, calculated in 2.44, are complex and correlated. These are controlled by the variation of the metal, channel and well charges with respect to the variation of  $V_G$  and  $V_B$  voltages. The direct relations between  $Q_m$ ,  $Q_{ch}$  and  $Q_{well}$  with their relative potential drops  $\Psi_{ch}$  and  $\Psi_{well}$  are not known analytically and these are the solutions of more complex numerical simulations, based on Poisson-Schrodinger formalism (PS). These are performed by NUMERICAD simulator (UTOXPP [12]). The calculated well and channel charge with their relative potential drops will be used in order to calculate the associated FDSOI capacitances. Therefore in this paragraph we will describe how to perform these simulations and how the concentrations of the channel and well charge along z direction, with the associated  $C_{gc}$  and  $C_{gb}$  capacitances, are calculated at specific  $V_G$  and  $V_B$  potentials conditions, by showing some numerical results obtained in this work. These numerical simulation will allow to understand the electrostatic behavior of the FDSOI device during C-V measurement.

The intensive downscaling of CMOS transistor, aiming to improve device performance, cost of production and energy, leads to FDSOI channel ( $t_{ch}$ ), front-oxide ( $t_{fox}$ ) and back-oxide ( $t_{box}$ ) thicknesses of very few nanometers. Mechanisms such as Quantum confinement [13, 14] and wave function penetration [15], typical of the dual particle-wave nature of the electrons, become more and more important with the decrease of these thicknesses. The analytical model proposed by Hyung-Kyu Lim and J. G. Fossum [9] is not longer sufficient with such nanometric thicknesses, since the dark space (1.1nm in terms of Si dielectric) is in the range of channel and oxide thickness (6-10 nm and 1 nm). Moreover a distinction of two independent charges (front and back channel) is no longer possible with such nanometric channel thickness since the channel can be filled entirely by free carriers. Therefore quantum effect has to be taken into account in order to predict the real electrostatic behavior and distribution charge [16, 17]. A classical description of the carrier concentration, based on Boltzmann formalism, is not sufficient anymore to get a real distribution of the charge in the channel and well regions. For an accurate description of the electron behavior and therefore charge distribution, Schrodinger and Poisson

equations have to be solved self-consistently [18]. This means that from an ab initio electrostatic potential distribution, calculated within classical formalism, the Schrodinger equation calculates the charge distribution across the FDSOI stack. This charge distribution is given to Poisson equation that calculates the new potential electrostatic distribution. These are solved self-consistently, as formerly said, until convergence condition is satisfied. The scheme is reported in fig. 2.7.

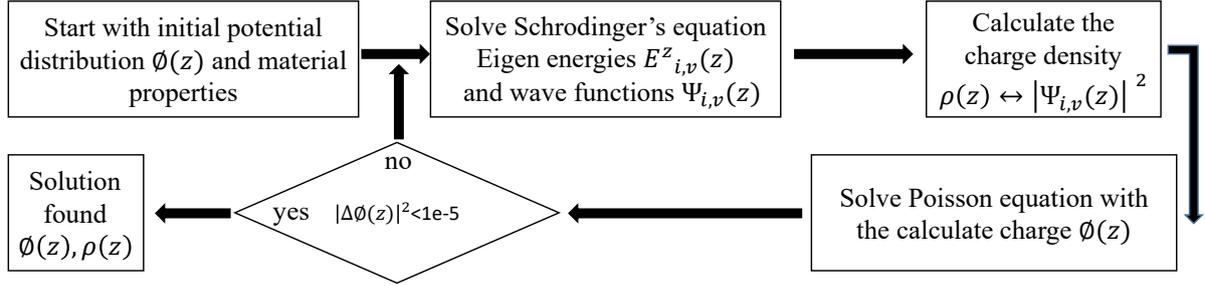


Figure 2.7: Flow chart of the Poisson-Schrodinger self-consistent solution.

### 2.3.2 1-D Poisson-Schrodinger Equation

As reported in Fig. 2.7, the Poisson law is a differential equation of the second order with two potential boundary conditions ( $V_{G \text{ static}}, V_{B \text{ static}}$ ). The FDSOI electrostatic potential distribution is the result of a typical Dirichlet problem, that can be formulated as

$$\begin{cases} \frac{\partial}{\partial z} \left( \epsilon(z) \frac{\partial}{\partial z} \right) \phi(z) = -\rho(z) \\ \phi(z_0) = V_{G \text{ static}} - \phi_{mW} \\ \phi(z_W) = V_{B \text{ static}} \end{cases} \quad (2.45)$$

The equations 2.24 and 2.25, previously found, and the Dirichlet problem in eq. 2.45 are relations obtained from Gauss law related to this Poisson equation. From the potential distribution calculated by equation system 2.45 and within the effective mass approximation, for a particle of mass  $m$  under a potential energy  $q\phi(z)$ , the charge distribution is obtained with the 1-D dimensional time

independent Schrodinger equation (fig.2.7), that is given by:

$$\begin{cases} -\frac{\hbar^2}{2} \frac{\partial}{\partial z} \left( \frac{1}{m_i(z)} \frac{\partial}{\partial z} \right) \psi_{i,v}(z) + q\phi(z)\psi_{i,v}(z) = E_{i,v}^z(z)\psi_{i,v}(z) \\ \psi_{i,v}(z_1) = 0 \\ \psi_{i,v}(z_2) = 0 \\ z_1 < (\psi_{i,v}(z), E_{i,v}(z), \phi(z)) < z_2 \end{cases} \quad (2.46)$$

where  $m$  is the effective mass,  $\hbar = \frac{h}{2\pi}$  is the Planck constant,  $\psi_{i,v}$  is the

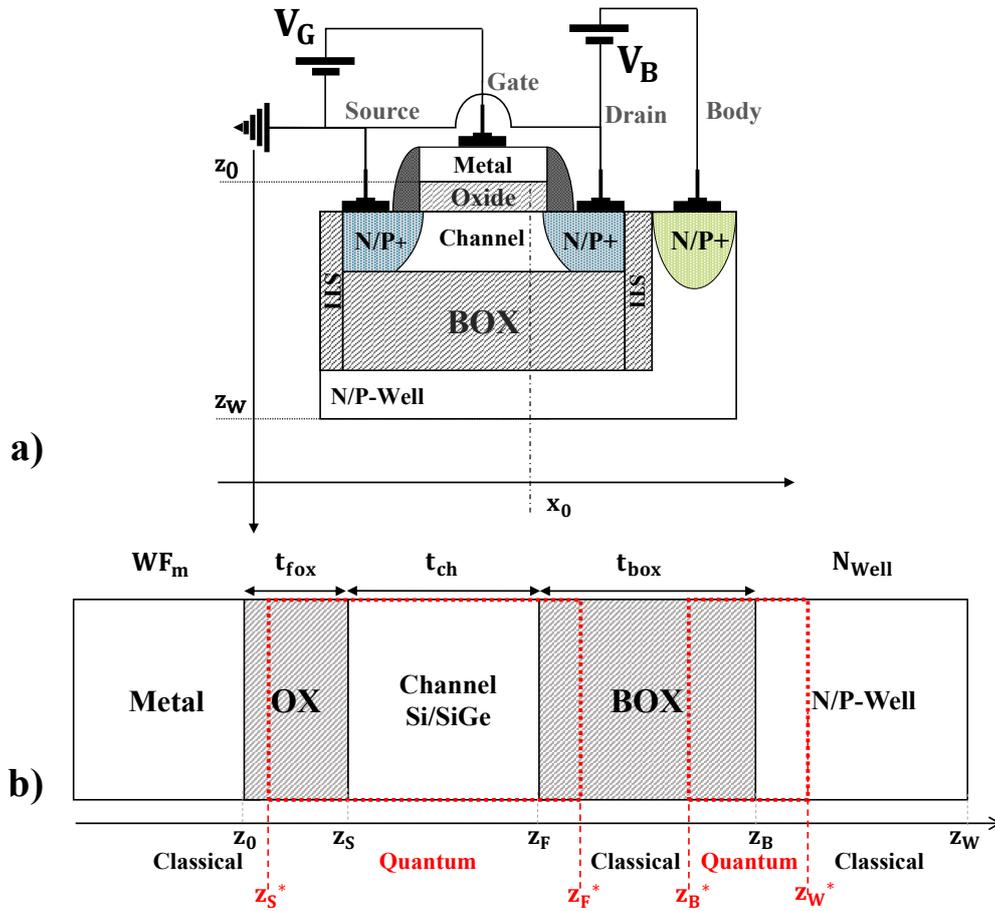


Figure 2.8: a) FDSOI device with in-plane cross section ( $x_0$ ) for 1-D numerical simulation. b) Cross section  $x_0$  with definition of the classical and quantum regions along  $z$  direction.

wave function of the  $v$ -th sub-band of  $i$ -th band of Silicon material. As we can observed, for the Schrodinger equation, as imposed by the boundary conditions, the particle wave-function has to be zero in two specific positions of the FDSOI stack, that means zero probability to find a particle in those positions. These conditions are dependent on the formalism, Boltzmann or Schrodinger, used in

order to calculate the charge in the FDSOI stack. As shown in fig. 2.8, the free carrier density is calculated using PS formalism just in specific regions of the FDSOI stack (the entire channel and part of the well substrate) which includes oxide/semiconductors interfaces. The complementary zones are within classical formalism based on Boltzmann law.

With the purpose of including electron and hole wave function penetration, the PS formalism is also solved in complementary zones as the front-oxide and back-oxide (Fig. 2.8). This means to have, for the first region (channel),

$$\begin{cases} \psi_{i,v}(z_S^*) = 0 \\ \psi_{i,v}(z_F^*) = 0 \end{cases} \quad (2.47)$$

and for the second region (well),

$$\begin{cases} \psi_{i,v}(z_B^*) = 0 \\ \psi_{i,v}(z_W^*) = 0 \end{cases} \quad (2.48)$$

The Poisson-Schrodinger equations are discretized along  $z$  direction using second order derivative discretization [19]. From the obtained discretized Schrodinger equation, we can calculate the energy eigenvalues ( $E_{i,v}$ ) and the wave function ( $\psi_{i,v}$ ) from which we can calculate the free density charge (fig.2.7), (of electrons in this case) as

$$n(z) = \sum_{i,v} \frac{m_{xy}^v}{\pi \hbar^2} g_v k_B T \ln \left( 1 + e^{\frac{E_F - E_{i,v}^z}{k_B T}} \right) |\psi_{i,v}(z)|^2 \quad (2.49)$$

where  $m_{xy}^v$  is the in-plane effective mass of the  $v$ -th band and  $g_v$  is the corresponding sub-band degeneracy for the Silicon conduction band (Table 2.1). The same can be calculated for holes  $p(z)$ ,

$$p(z) = \sum_{i,v} \frac{m_{hxy}^v}{\pi \hbar^2} g_{h,v} k_B T \ln \left( 1 + e^{\frac{-(E_F - E_{i,v}^z)}{k_B T}} \right) |\psi_{i,v}(z)|^2 \quad (2.50)$$

where  $m_{hxy}^v$  is the in-plane effective mass of the  $v$ -th band and  $g_{h,v}$  is the corresponding sub-band degeneracy for the Silicon valence band (Table 2.2).

From  $p(z)$  and  $n(z)$  therefore we can calculate the total charge distribution as

$$\rho(z) = q \cdot (p(z) - n(z) + N_d(z) - N_a(z)) \quad (2.51)$$

Table 2.1: Silicon masses for calculation of free density charge  $n(z)$ . A value of electron longitudinal and transverse mass of  $0.916m_0$  and  $0.190m_0$  are used [20].

Conduction Band Ellipsoid	Degeneracy	Effective masses $m_i^z$ [electron mass $m_0$ ]	In-plane effective masses $m_{xy}$ [electron mass $m_0$ ]
$k_X$	2	0.19	0.418
$k_Y$	2	0.19	0.418
$k_Z$	2	0.916	0.19

Table 2.2: Silicon masses for calculation of free density charge  $p(z)$ . A detailed description of the hole masses can be found in the book of Bhattacharya [20].

Valence Band	Degeneracy	Effective masses $m_i^z$ [electron mass $m_0$ ]	In-plane effective masses $m_{hxy}$ [electron mass $m_0$ ]
$HH$	1	0.277	2.5
$LH$	1	0.201	0.151
$SO$	1	0.233	0.233

where  $n(z)$  and  $p(z)$  are defined within quantum formalism (equations 2.49 and 2.50) for  $z_S^* \leq z \leq z_F^*$  and  $z_B^* \leq z \leq z_W^*$  and classically for the complementary regions

$$\begin{cases} n(z) = N_C \cdot e^{\frac{q\phi(z)}{k_B T}} \wedge p(z) = N_V \cdot e^{\frac{-E_{gW} - q\phi(z)}{k_B T}} & \text{for } z_W^* \leq z \leq z_W \\ n(z) = p(z) = 0 & \text{for } z_0 \leq z \leq z_S^* \cup z_F^* \leq z \leq z_B^* \end{cases} \quad (2.52)$$

$N_C$  and  $N_V$  are the 3-D effective density of state for the conduction and valence band of a Silicon semiconductor [21] in the well region. From the calculated total densities of charge (2.52) we can finally obtain the channel, well and metal charges using equations 2.13 and 2.14 with the only difference that the integrals are evaluated between  $z_S^*$  and  $z_F^*$  for the channel charge and  $z_B^*$  and  $z_W$  for the well charge (wave function penetration). From these charges, we can obtain the voltage drops across the front-oxide using equations 2.23 and 2.22 Using these relations, we assume that the penetrating charge is located at the interface front-oxide-channel (ideal case) but this is not true. However, the impact of the charge penetration is not important in the determination of the maximum capacitance and Gate voltage. Indeed, the total charge can be seen as the sum of the penetration charge and not penetrating one. We remember that the

penetrating charge is only inside the front-oxide whereas the not penetrating charge is the integral of the density of charge from the interface front-oxide to the well neutral region (across all the FDSOI stack in z direction). Indeed we find out that the voltage drop at the front-oxide can be affected since the penetrating charge see a dielectric thickness lower than the not penetrating charge. Indeed we find that

$$V_{fox} = -\frac{Q_{ch} + Q_w}{C_{fox}} - \frac{Q_{chp}}{C_{fox}^*} = -t_{fox} \frac{Q_{ch} + Q_w}{\epsilon_{fox}} - t_{fox}^* \frac{Q_{chp}}{\epsilon_{fox}} \quad (2.53)$$

where  $Q_{chp}$  is the channel charge penetrating in the oxide,  $Q_{ch}+Q_w$  is the total charge not penetrating and  $t_{fox}^* = t_{fox} - \Delta t_{fox}$ . Therefore at really strong inversion (and as well accumulation in case of standard bulk devices) a variation of the maximum capacitance and Voltage occurs with respect of the ideal case. The variation depends on the distribution of the penetrating charge in the oxide that will define  $\Delta t_{fox}$ . We report in Fig 2.10 a numerical simulation of both the charges (taking their absolute values). These are calculated by integrating density of charge of Fig. 2.9 where the distribution of these charge, close to the interface oxide-channel, are reported in function of the Gate voltage. As we observe the amount of charge penetrating (black triangles) into the oxide is at least 200 times lower than the total charge (black circles) for both the accumulation and inversion regimes. Consequently the drop voltages across the front oxide due to

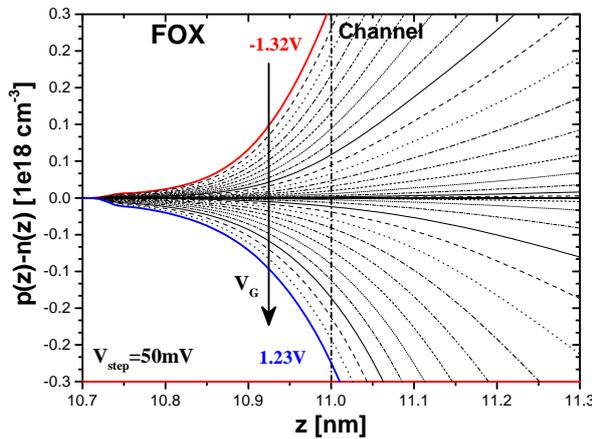


Figure 2.9: Free carriers distribution close at the interface front-oxide-channel, showing the penetration charge distribution from  $V_G = -1.32V$  to  $1.23V$  at  $V_B = 0V$ .

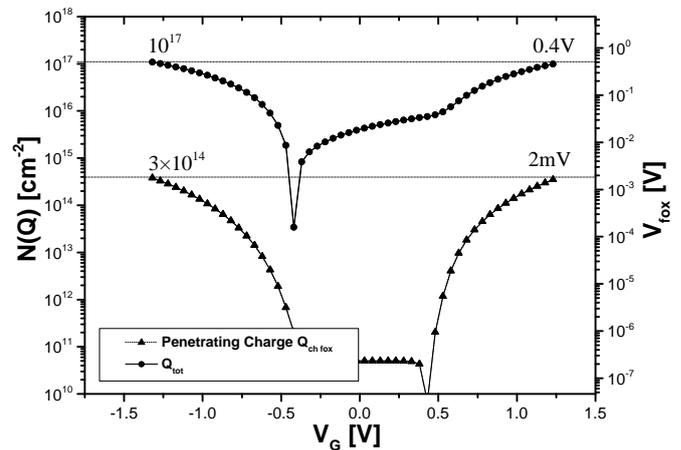


Figure 2.10: Simulated electrostatic potential of the FDSOI stack from  $V_G = -1.32V$  to  $1.23V$  at  $V_B = 0V$ .

the penetrating charge (less than 2mV) is much lower than drop voltage induced

by the total charge (less than 0.4V). The impact on the Gate voltage and therefore on the capacitance characteristic in case of SiO<sub>2</sub> is considered as negligible.

Always concerning the distribution charge across FDSOI stack, there's another critical point that has to be considered. Indeed whereas the channel charge is described within quantum formalism, the well charge is described within quantum and classical formalism. Indeed, its carrier density ( $\rho(z)$ ), is defined within Quantum formalism (2.49) between  $z_B^*$  and  $z_W^*$  and within Classical formalism between  $z_W^*$  and  $z_W$  (Fig.2.8). The adjustment of the two solutions is critical for the majority carriers, since the concentration of the minority carriers at 20 nm from the interface box-well is negligible. At the right edge of a well quantum box ( $z_W^*$ ), the wave functions of the carriers at the different energy levels is zero. Thus this boundary condition creates an artificially area without charge (about 5 nm.  $z_W^* - 5nm < z < z_W^*$ ). The conventional solution is thus to connect a few nanometers before this edge the classical solution, calculated until this new border, with the quantum mechanically solution, calculated always within the quantum region (until  $z < z_W^*$ ) to ensure a seamless transition. Therefore, accordance between classical and quantum mechanical solution in  $z_W^* - 5nm$  is necessary in order to obtain a continuous solution [12]. A good choice of the 3-D effective density of states mass, in the classical region is necessary in order to have this perfect matching between these two regions (classic and quantum). The values are reported in Table 2.3.

Table 2.3: Classical 3-D silicon masses for calculation of free density charges  $p(z)$  and  $n(z)$  in the classical region at T=300K

Band	3-D Effective density of states mass [electron mass $m_0$ ]	3-D Effective density of states [ $10^{19}cm^{-3}$ ]
Conduction Band	1.12	2.96
Valence Band	1.25	3.5

The value of the in-plane effective mass for the heavy hole (HH) valence band doesn't correspond to the standard value ( $0.513m_0$ ) used in the state of the Art. This value ( $m_{HHxy}$ ) of  $2.5m_0$ , with  $m_0$  for the electron mass, has been obtained from the calibration of the simulation, based on parabolic approximation, with a more complex and accurate 6-  $K \cdot P$  band self-consistent simulation, as reported in the work of S. Soussou et al. [22]. This value is used in order to modify the effective mass of the heavy hole ((CEMA) corrected effective mass) and fit the Capacitance-Voltage characteristic obtained with the 6-  $K \cdot P$  methods. This value,

obtained through the CEMA method, takes into account the real curvature of heavy hole band, that affects its effective mass. This leads to higher value of 3-D effective density of states ( $N_V = 3.5 \cdot 10^{19} \text{cm}^{-3}$ ) and 3-D DOS mass ( $1.25m_0$ ) for the valence band in the classical region with respect to the value ( $3 \cdot 10^{19} \text{cm}^{-3}$ ) used in the state of the art.

Until now, we just mention the technological parameters related to the Silicon material used in conventional transistors but in the last decades Silicon-Germanium (SiGe) has been proposed as a worthy prospect and legitimate candidate for P-MOS FDSOI devices [23, 24, 25, 26]. Indeed, in the FDSOI technology, channel material has a fundamental role in defining the electrical properties as mobility and transport [27]. Since the purpose of this work is to characterize, as well, devices with SiGe channel, a proper calibration of the technological parameters is necessary.

Table 2.4:  $\text{Si}_{1-\chi}\text{-Ge}_\chi$  masses for calculation of free density charge  $p(x)$  with  $\chi=0.25$

Valence Band	Degeneracy	Effective masses $m_i^z$ [electron mass $m_0$ ]	In-plane effective masses $m_{xy}$ [electron mass $m_0$ ]
<i>HH</i>	1	0.277	<b>1.5</b>
<i>LH</i>	1	0.201	0.151
<i>SO</i>	1	0.233	0.233

In the previous work of S.Soussou et al. [28], it has been demonstrated that during the Si-SiGe channel epitaxy, tensile stress is induced by the presence of the Germanium. This tensile stress causes a variation of the channel lattice constant. This leads to a SiGe channel film compressively strained. This induces a variation, in form of deformation, splitting and shift [29], of the channel valence bands. In order to take into account this deformation, a value of the in-plane effective mass of  $1.5m_0$  is necessary, as reported in Table 2.4. This value is set for an expected concentration level of 25% of Germanium. The value of in-plane effective mass for the heavy hole of the valence band has been obtained, as done previously for the strained Silicon, from the calibration of the CEMA simulation, based on parabolic approximation, with a more complex and accurate 6- $K \cdot P$  band self-consistent simulation [22]. Indeed the  $K \cdot P$  formalism is able to take into account of the mechanical stress, the presence of Germanium in the FDSOI channel and its effect over the curvature of the energy bands. As reported in the work of Yang et al. [29], the in-plane effective mass takes into account the

variation of the curvature whereas the proper values of the gap energy and electron affinity ( $E_{g\text{ SiGe}}$ ) of the valence band takes into account the shift and splitting of the bands energies. In this work, just the variation of the valence bands is taken into account since the only devices based on SiGe channel film are the P-MOS FDSOI ones. Once understood the evaluation of the electrostatic potential and charge distribution across the device stack and how to take into account the difference between Si and SiGe channel, we can finally evaluate the effect of the electrostatic potential ( $V_G, V_B$ ) and technological parameters ( $t_{\text{fox}}, t_{\text{ch}}, t_{\text{box}}$  and  $N_{\text{Well}}$ ) over the charges ( $Q_{\text{ch}}, Q_{\text{Well}}$  and  $Q_m$ ) and the relatives capacitance ( $C_{\text{gc}}, C_{\text{gb}}, C_{\text{bc}}$  and  $C_{\text{bg}}$ ).

### 2.3.3 Numerical simulation of Electrostatic Potential and C-V characteristic of FDSOI stack

The purpose of the numerical simulations is twofold:

- Understand the electrostatic behavior of a FDSOI stack: calculation of the potential profile and distribution of the charges ( $Q_{ch}$  and  $Q_{well}$ ).
- Simulate and predict the Capacitance-Voltage characteristic for a specific FDSOI stack which is defined by a specific set of physical parameters ( $t_{fox}=EOT$ ,  $WF_m=WF_{eff}$ ,  $t_{ch}$ ,  $t_{box}$ ,  $N_{Well}$  etc.).

For this purpose, in this paragraph we report two numerical simulation results obtained in this work. These are the "front" capacitances ( $C_{gc}$  and  $C_{gb}$ ) carried out at two specific back bias conditions ( $V_B=0V$  and  $V_B=5V$ ). These simulated charges, respectively channel and well, at different  $V_G$  biases, will lead us to obtain the Gate-to-channel and Gate-to-Body capacitances in case of NMOS-FDSOI device. The simulated device structure is shown in the scheme of Fig. 2.11. For

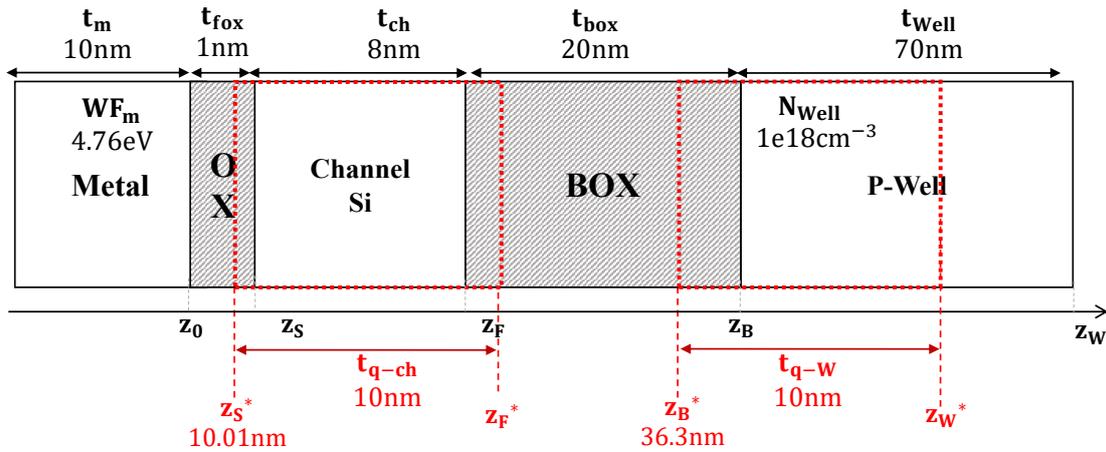


Figure 2.11: FDSOI device with in-plane cross section for 1-D numerical simulation with definition of the classical and quantum regions along  $z$  direction.

this specific simulation, a thickness of 1nm and 20nm for front-oxide and the back-oxide are considered. Moreover, a value of 4.76eV for  $WF_m$  and a well doping level of  $10^{18} \text{ cm}^{-3}$  (P-doped) are taken into account. Both the quantum box widths, for channel and well, are set 10nm thick. The electrostatics simulation is performed by varying the Gate voltage, from -1.32V to 1.27V with a step of 50mV, and by fixing the Body voltage, as said previously, at two specific values: 0V and 5V.

Table 2.5: SiO<sub>2</sub> masses for calculation of free density charge  $p(z)$  and  $n(z)$ .

Band	Degeneracy	Effective masses $m_i^z$ [electron mass $m_0$ ]	In-plane effective masses $m_{xy}$ [electron mass $m_0$ ]
<i>HH</i>	1	0.5	0.5
<i>LH</i>	1	0.5	0.5
<i>SO</i>	1	0.5	0.5
Conduction band	6	0.5	0.5

The front and back-oxide are SiO<sub>2</sub> material whose effective masses are reported in Table 2.5. These effective masses values are different with respect to the Si material and are used in PS equation in order to take into account the wave function penetration. The value of SiO<sub>2</sub> dielectric constant ( $\epsilon_{\text{SiO}_2}$ ) is  $3.9\epsilon_0$ , where  $\epsilon_0$  is the vacuum dielectric constant, while electron affinity ( $X_{\text{g SiO}_2}$ ) and energy gap ( $E_{\text{g SiO}_2}$ ) are respectively 1.1eV and 9eV. The channel and well are pure Silicon crystal oriented in <001> direction. They are characterized by a dielectric constant value ( $\epsilon_{\text{Si}}$ ) of  $11.7\epsilon_0$  and a  $E_{\text{g Si}}$  and  $X_{\text{g Si}}$  respectively of 1.12eV and 4.2eV. For each bias ( $V_G$ ), Poisson-Schrodinger is solved self consistently until convergence condition is reached.

Band diagrams and relative electrostatic potential profiles are reported in Figs. 2.12 and 2.13 for the case  $V_B=0V$ . Due to nanometric scale and a non-doped channel, we can observe that the variation of the Gate voltage, from  $V_G=1.23V$  (blue solid line) to  $V_G=-1.32V$  (red solid line), induces a variation of the potential and energy band profile across the whole FDSOI stack.

These variations of electrostatic potential distribution are occurring due to the simultaneous variation of FDSOI channel and well charges, as reported in Figs. 2.14 and 2.15. Specifically, we can observed that the trends of  $Q_{\text{ch}}$  and  $Q_{\text{w}}$ , with respect to Gate voltage variation, are similar. Indeed by increasing more and more the Gate voltage from negative to positive values, the channel and well charges become more and more negative. We remember that whereas the potential drop of the back oxide is only induced by the well charge (equation 2.22), the front-oxide potential drop is induced by both the well and channel charges (equation 2.23). The distribution of these two charges, as function of Gate voltage, is not the same. This is strongly dependent on the device technological parameters ( $t_{\text{ch}}$ ,  $t_{\text{box}}$ ,  $N_W$ , material channel,  $V_B$  back biasing etc..).

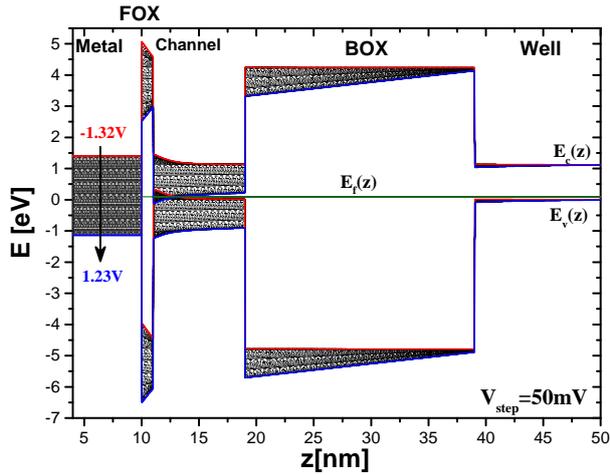


Figure 2.12: Simulated Energies band diagrams of the FDSOI stack from  $V_G = -1.32V$  to  $1.23V$  at  $V_B = 0V$ .

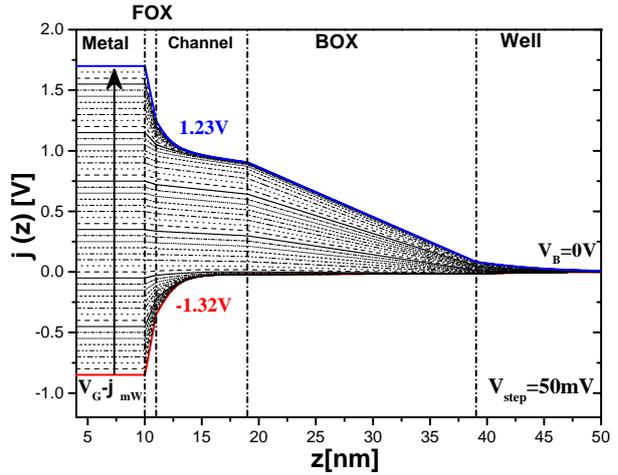


Figure 2.13: Simulated electrostatic potential of the FDSOI stack from  $V_G = -1.32V$  to  $1.23V$  at  $V_B = 0V$ .

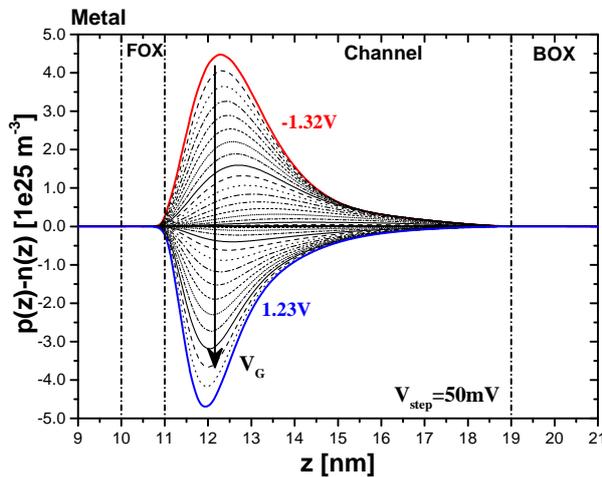


Figure 2.14: Free carriers distribution of the FDSOI stack channel from  $V_G = -1.32V$  to  $1.23V$  at  $V_B = 0V$ .

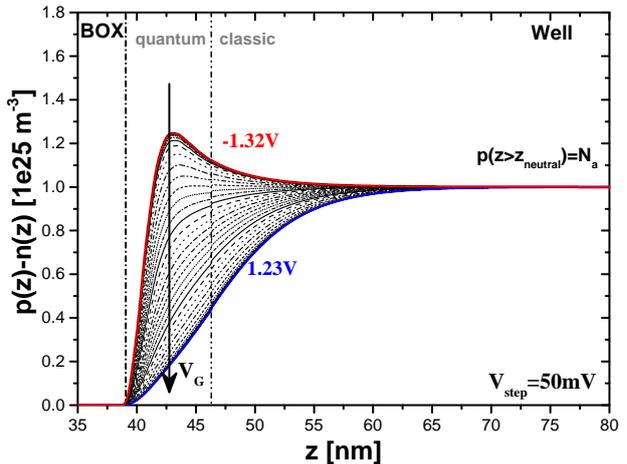


Figure 2.15: Free carriers distribution of the FDSOI stack well from  $V_G = -1.32V$  to  $1.23V$  at  $V_B = 0V$ .

From these simulated charges, NUMERICAD UTOXPP calculates directly the capacitance  $C_{gc}$  and  $C_{gb}$  by using equation 2.30 and 2.31.

The relations 2.30 and 2.31 are independent of the frequency and therefore of the reaction time of the free carriers (channel and well). Indeed, we assume that the free carriers charge in the channel and well instantly responds to the variation of the small signal voltage applied at the Gate terminal ( $v_g(t)$ ). This means, as previously said, that we don't have any frequency dependency with these simulated capacitance. Moreover, the simulator assumes that the charge inversion of electron and holes, occurs in the channel independently of the MOS

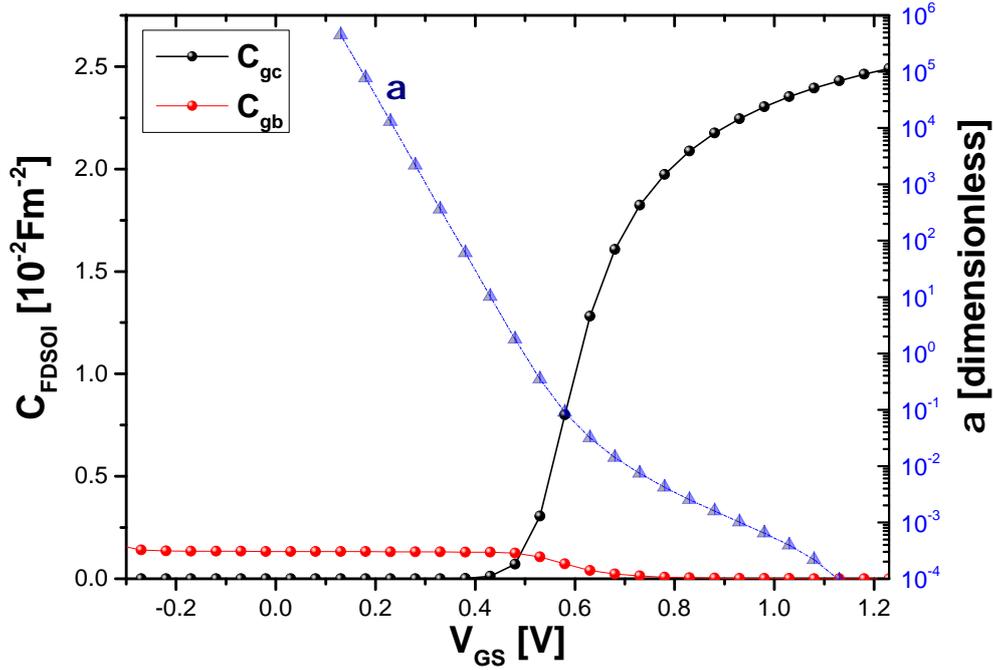


Figure 2.16: FDSOI capacitance characteristics ( $C_{gc}$  in black ,  $C_{gb}$  in red) and  $\alpha$  parameter versus the Gate-Source voltage.

type and layout. We will always have both inversion for positive (electron) and negative (negative) voltage. This means that in the channel or in the well, in terms of numerical simulation, we have a source for both type of the charges (n and p). We have seen that this is not true in case of a P-MOS or N-MOS FDSOI where the support of only one type of free carriers can occur. Indeed in Chapter 1, as reported in Fig. 1.14, we saw experimentally that in case of P-MOS devices, accumulation of electrons doesn't occur since Source and Drain are highly p-doped and channel is not doped at all. The Capacitance voltage characteristics,  $C_{gc}$  and  $C_{gb}$ , calculated from the charges of Figs. 2.14 and 2.15, are shown in figure 2.16. The  $C_{gc}$ , associated with electron inversion, is reported in black solid line whereas  $C_{gb}$  in red solid line.

From these capacitances, by simply calculating their ratio ( $C_{gb}/C_{gc}$ ), we can obtain the parameter  $\alpha = \partial Q_w / \partial Q_{ch}$ .  $\alpha$  has an important role in defining the FDSOI capacitances (eqs. 2.36, 2.37, 2.42 and 2.43). This parameter describes the electrostatic regime operation of a FDSOI device. Indeed in Fig. 2.16, we observe that for  $V_{GS} < 0.4V$ , and therefore a value of  $\alpha$  higher than  $10^1$ , the Gate-to-channel capacitance is zero since no channel charge is present. Only the Gate-to-Body capacitance is present and the well charge dominates the FDSOI electrostatics. On the contrary, for  $V_{GS} > 0.7V$  and therefore a value of  $\alpha$  lower than  $10^2$ , the Gate-to-Body capacitance is zero and the Gate-to-channel capacitance

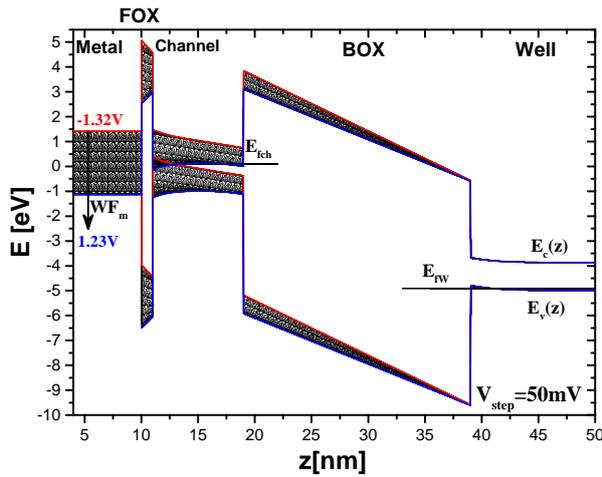


Figure 2.17: Simulated Energies band diagrams of the FDSOI stack from  $V_G = -1.32\text{V}$  to  $1.23\text{V}$  at  $V_B = 5\text{V}$ .

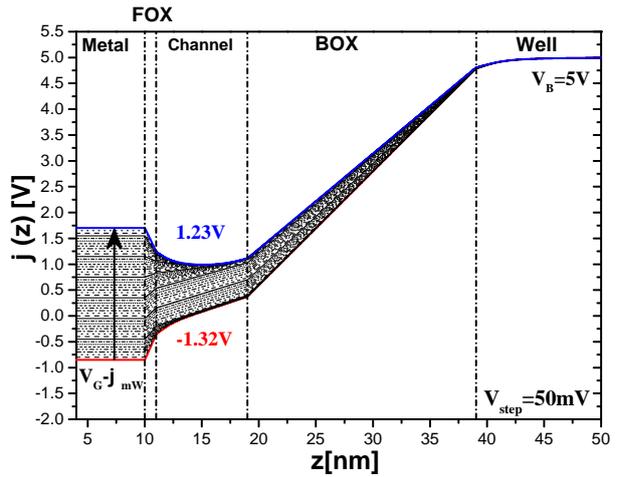


Figure 2.18: Simulated electrostatic potential of the FDSOI stack from  $V_G = -1.32\text{V}$  to  $1.23\text{V}$  at  $V_B = 5\text{V}$ .

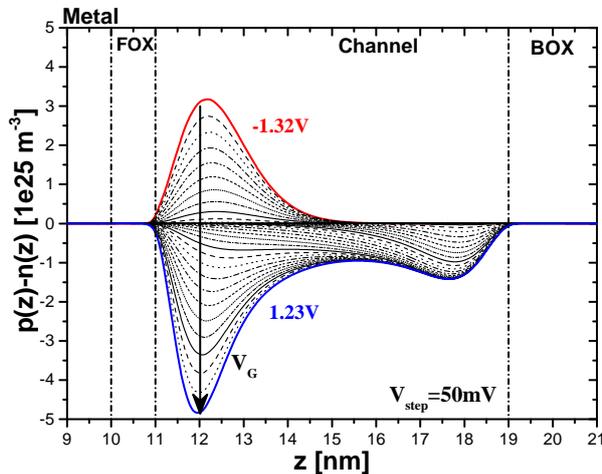


Figure 2.19: Free carriers distribution of the FDSOI stack channel from  $V_G = -1.32\text{V}$  to  $1.23\text{V}$  at  $V_B = 5\text{V}$ .

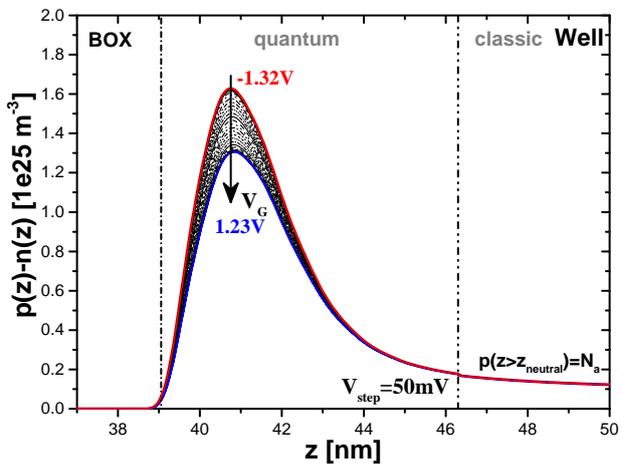


Figure 2.20: Free carriers distribution of the FDSOI stack well from  $V_G = -1.32\text{V}$  to  $1.23\text{V}$  at  $V_B = 5\text{V}$ .

increases since the channel charge, at strong inversion, get closer to the interface oxide-channel and screens the effect of the Gate voltage on the well charge. Therefore, the well charge is fixed and independent of the applied voltage for  $V_{GS} > 0.7\text{V}$ . This parameter can be obtained experimentally and will be used to identify the proper way to characterize the FDSOI stack, as will be shown in the next chapter.

These capacitances (Figure 2.16) can be affected by the back biasing  $V_B$  and the numerical simulation can predict the impact of Body potential on C-V previously calculated. We report in Figures 2.17 and 2.18 the bands diagrams and the electrostatic potential profile across the FDSOI for  $V_B = 5\text{V}$ . As observed, the

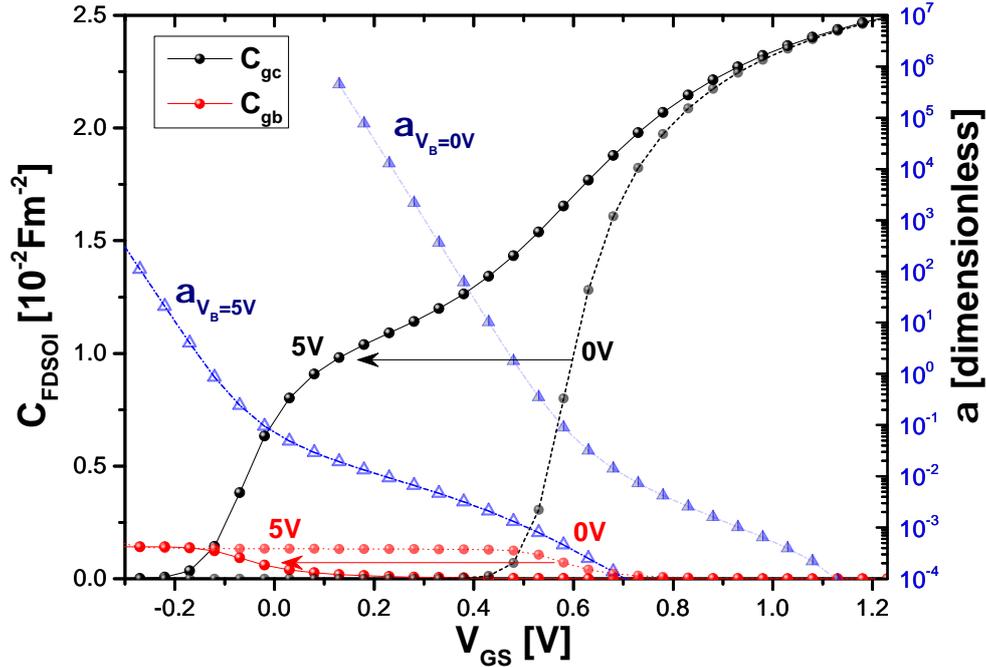


Figure 2.21: FDSOI capacitance characteristics ( $C_{gc}$  in black,  $C_{gb}$  in red) and  $\alpha$  parameter versus the Gate-Source voltage.

first remarkable difference with respect to  $V_B=0V$ , is the band diagrams. We remember that in the first part we introduced the relation between  $V_B$  and the channel and well Fermi energies (equation 2.4). Therefore, based on this relation, by applying such Body voltage value, a split of the Fermi energies occurs between the channel and well system (Fig. 2.17). The immediate consequence is a variation of the potential distribution as reported in Fig. 2.18. Indeed the potential drop across the back-oxide and well are shifted toward negative values by larger positive values of  $V_B$ . This potential variations are induced by the simultaneous variation of the channel and well charge, as reported in Figs. 2.19 and 2.20, with respect to the condition  $V_B=0V$  (Figs. 2.14 and 2.15). Moreover at  $V_B=5V$  (compared to  $V_B=0V$ ) the distribution of the channel charge radically changes. Indeed the onset of the inversion charge starts close the interface channel-back-oxide and not at the interface front-oxide-channel as for  $V_B=0V$ . By increasing the Gate voltage the channel is progressively filled with electrons until their appearance at the interface front-oxide-channel.

$V_B$  therefore affects the relations  $\Psi_{ch}(Q_{ch})$  and  $\Psi_{well}(Q_w)$ . As consequence, we will expect that the capacitance  $C_{gc}$  and  $C_{gb}$ , based on the relations 2.36 and 2.37 will change with respect to  $V_B=0V$ . Indeed, as shown in Fig. 2.21, the calculated  $C_{gc}$  and  $C_{gb}$  capacitances vary with back biasing. A remarkable deformation and shift of  $C_{gc}$  and  $C_{gb}$  are observable in this figure, if compared to the capacitance at  $V_B=0V$

reported in dashed line while the capacitances at  $V_B=5V$  are in solid lines. The same discussion can be done for two other capacitances,  $C_{bc}$  and  $C_{bg}$ , defined in eq.2.42 and 2.43 where  $\beta$  parameter plays the same role as  $\alpha$ .

Changing the box, channel thickness and doping level has a non-linear effect on the capacitance characteristic. Indeed as for  $V_B$ , deformation and shift are expected. We can conclude that this numerical simulator is capable to predict the C-V characteristics of a FDSOI stack from a specific set of physical parameters values of a FDSOI stack. This simulated capacitance can be compared with the experimental C-V characteristic of a real FDSOI transistor allowing the extraction of the technological parameters of the FDSOI. All these elements will be discussed in the next chapter where extraction of EOT and  $WF_{eff}$  of the FDSOI devices will be carried out by fitting the experimental C-V with such numerical simulations.

## 2.4 Conclusion

In this Chapter, FDSOI device technology has been presented by specifically focusing on the structure and its difference with respect to the bulk technology.

FDSOI Electrostatics has been introduced by analysing the interaction between the different band diagrams (all the layers composing the FDSOI stack).

From the band diagram, relationship between the experimental voltage and the physical parameters of the FDSOI stack have been obtained for the front and back Gate terminals. Specifically, these equations relate the respective biases,  $V_G$  and  $V_B$  to the respective potentials drops ( $\Psi_{ch}$ ,  $\Psi_{well}$ ) and metal, channel and well charges ( $Q_m$ ,  $Q_{ch}$  and  $Q_{well}$ ).

Capacitances ( $C_{gc}$ ,  $C_{gb}$ ,  $C_{bc}$  and  $C_{bg}$ ) have been defined with respect to  $V_G$  and  $V_B$  potentials which also are related to the FDSOI stack capacitances.

The obtained C-V relations will be used in order to characterize the FDSOI stack through simple strategy.

Due to the not-known analytical relationships,  $Q_{ch}(\Psi_{ch})$  and  $Q_w(\Psi_{well})$ , the previously defined capacitances cannot be directly calculated and compared with experimental results.

Numerical methods (UTOXPP), based on Poisson-Schrodinger formalism, has been presented in order to predict the electrostatic behavior (charges and profile potential) of a specific FDSOI stack under specific bias conditions.

The numerical prediction will be used, in the next chapter as important tool, in order to understand the physical phenomenon during field effects measurements and to extract the technological parameters ( $WF_{eff}$  and EOT) of the FDSOI devices.



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# Chapter 3

## Numerical Extraction of $WF_{\text{eff}}$ and EOT based on inversion C-V measurements

### 3.1 Introduction

As already seen in the chapter 1, the effective Work function ( $WF_{\text{eff}}$ ) and the Equivalent Oxide thickness (EOT) are key parameters for FDSOI device characterization.  $WF_{\text{eff}}$  and EOT are the values of Work Function and Thickness that an ideal Metal/SiO<sub>2</sub> gate stack should have to account for the measurements. They directly influence Capacitance Equivalent thickness (CET), Threshold voltage ( $V_{\text{th}}$ ) and therefore on-current. Both are strongly related to the process: dielectric thickness, metal gate work function and dielectric interface dipole [1].

We have also seen that the former methodologies [2, 3] for automatic and statistical extraction of  $WF_{\text{eff}}$  and EOT are compatible for bulk technology but no longer sufficient for FDSOI technology. Moreover, we remember that Capacitance–Voltage extraction of the flat band voltage ( $V_{\text{FB}}$ ) in the accumulation region has been traditionally the  $WF_{\text{eff}}$  extraction method for the bulk technology. The absence of CV signal in the accumulation and flat band regions compared to standard bulk capacitance pushes us to look for alternative solutions for  $WF_{\text{eff}}$  and EOT extraction. Indeed the inversion region ( $V_{\text{th}}$ ), including its modulation, as reported in Fig. 3.6, still available in FDSOI can be used to extract the  $WF_{\text{eff}}$  and EOT.

The extraction difficulties are due to the complexity of the FDSOI structure compared to the bulk technology (Fig. 3.1) and the strong influence of several

technological parameters (previously introduced) on  $V_{th}$  such as: channel thickness  $t_{ch}$ , buried oxide (BOX) thickness  $t_{box}$  and well doping level of substrate N-Well at BOX backside. All of them may impact the  $V_t$  of transistor with a certain Gate stack with its EOT and  $WF_{eff}$ .

In this chapter, we will present a methodology based on numerical simulation which allows a reliable extraction of  $WF_{eff}$  and EOT. This methodology has been validated on a wide set of transistors (15), all processed on a same wafer. Therefore, we will present first the process and the different splits among the transistors. For a reliable extraction, the classical  $C_{gc}$  measurement is no longer sufficient and an additional  $C_{bc}$  measurement is presented to allow the characterization of the buried oxide capacitance. Then the different characteristics are compared and the methodology to lead from them to a reliable extraction of EOT and  $WF_{eff}$  is presented. Finally, the extraction results are commented both to confirm the methodology and to analyze the impact of process module on FDSO stack thicknesses and metal Gate effective work function.

## 3.2 Technology and test structures

We will present in this paragraph, the reference FDSOI MOS architectures that have been used for this extended study. Various technology options, such as Gate stack process, Source-Drain well type, channel materials and back plane doping type, have been introduced and investigated as possible technological solutions in order to improve the electrostatic performance of the reference architectures. The two reference architectures are reported in Fig. 3.1 respectively: (a) FDSOI P-MOS device and (b) N-MOS device both featuring a gate stack characterized by a metal bilayer (Poly and TiN) on the top of oxide bilayer (High-k dielectric HfON and SiON).

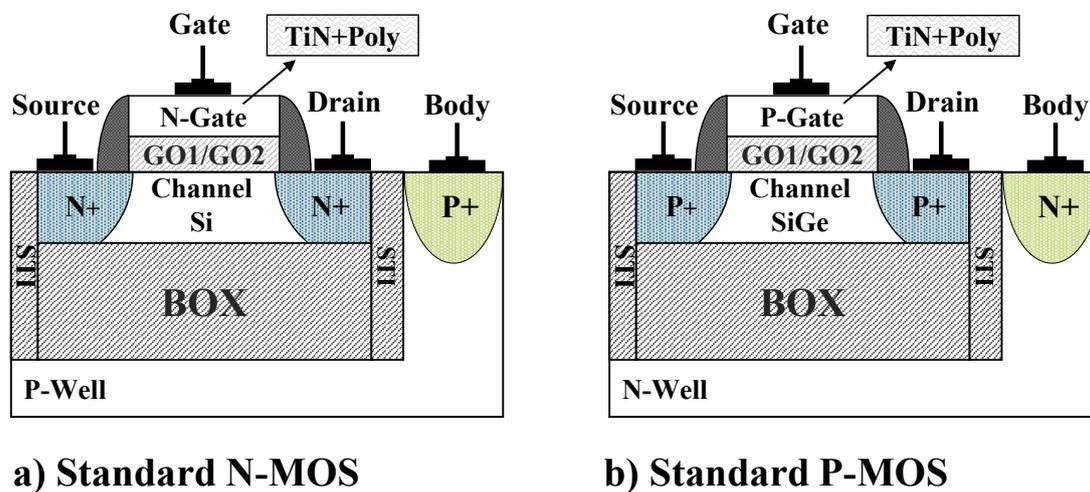


Figure 3.1: Standard (a) PMOS and (b) NMOS FDSOI devices: both feature a gate stack TiN+Poly on a bilayer oxide HfON+SiON but (a) with SiGe channel and N-Well substrate and (b) with Si channel and P-Well substrate.

To get these devices, the process starts from an ultra-thin silicon body over a buried oxide. The strained  $\text{Si}_{0.75}\text{Ge}_{0.25}$  channel (cSiGe) is selectively processed in PMOS areas by epitaxy process followed by a Ge condensation. This step is performed before shallow trench isolation (STI) regions are patterned and the back side wells are implanted. Thus, the channel thickness is around 6-8 nm of Si or  $\text{Si}_{0.75}\text{Ge}_{0.25}$  over a 20 nm BOX with a P or N-Well with a  $10^{18}\text{cm}^{-3}$  doping level at its backside. Two different interlayer (SiON) dielectrics, can be deposited corresponding to two different final oxide thicknesses: EOT=1 nm for GO1 and EOT=3 nm for GO2. The bilayer high-k HfON/SiON is deposited by Atomic Layer Deposition, Metal Organic Vapor deposition and decoupled plasma

nitridation. To obtain N and P gate types, a sacrificial gate is deposited before the final metal gate (TiN+Poly), specifically to each N or P gate type. Sacrificial gate includes specific additives which are diffused by thermal annealing in order to adjust dipole at oxide bilayer inner interface [1, 4]. The final metal gate bilayer (TiN+Poly) is the same for all the devices (N and P-MOS) and it is deposited right after the sacrificial gate etching. After final gate deposition, the Source-Drain implantations (specific to each FDSOI MOS type) are carried out, followed by final annealing. The process for the Gate stack deposition is reported in Fig. 3.2.

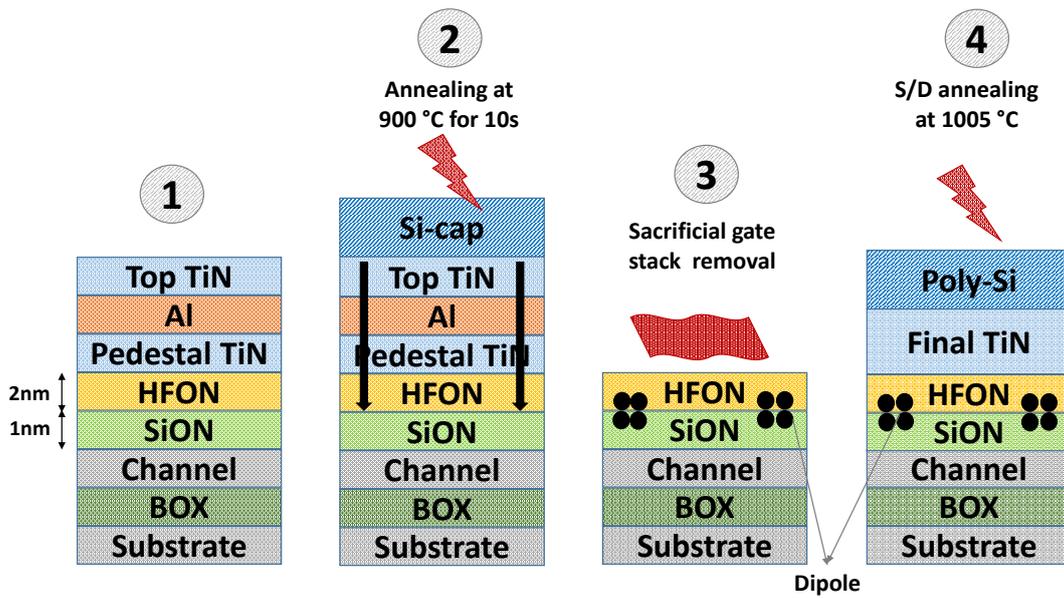


Figure 3.2: Sacrificial Gate first approach: 1) sacrificial Gate deposition, 2) annealing at 900 C for 10s, 3) Sacrificial Gate stack wet removal and 4) Final Gate deposition, Gate patterning and Source-Drain annealing.

Table 3.1: Set of different FDSOI devices featured by a combination of different process modules on metal gate, channel (Si and SiGe) and well (P and N doped) for GO1 and GO2 dielectrics.

Device	channel	Metal	Well substrate
N-MOS	Si	N-Gate	P
	Si	N-Gate	N
	Si	P-Gate	P
P-MOS	SiGe	P-Gate	N
	SiGe	N-Gate	P
	SiGe	N-Gate	N
	Si	P-Gate	N
	Si	N-Gate	N

From these standard FDSOI MOS (Fig. 3.1), a wide set of devices can be obtained by combining the process modules on metal gate, dielectric, channel and well type, as reported in Table 3.1. 13 extra architectures are obtained with respect to the two reference devices for a total of 15 different transistors reported in Table 3.1. For the N-MOS transistors for each dielectric type (2 dielectrics: GO1 and GO2) we have 3 different architectures: the reference N-MOS device (Fig. 3.1 a), N-MOS device featuring a N-type Well and an N-MOS with a P-Gate metal. Thus a total of  $(2 \times 3)$  6 N-MOS transistors are obtained. Same discussion can be done for the P-MOS devices. Indeed, for each dielectric type (2 dielectrics: GO1 and GO2) we have 5 different architectures: the reference P-MOS device (Fig. 3.1 b), P-MOS device featuring a N-type Gate and P-type Well respectively, a P-MOS device featuring N-type Gate, a P-MOS device featuring Si channel material and a P-MOS device featuring Si channel material and N-type Gate. The last architecture exists only for GO1 dielectric. Thus a total of  $((2 \times 5) - 1)$  9 P-MOS transistors are obtained. Therefore, the sum of the different N and P-MOS transistors is  $(6 + 9)$  15.

These multitude of devices will allow us to investigate the impact of the different process modules on the Gate stack technological parameters ( $EOT$  and  $WF_{eff}$ ) but also to validate the numerical methodology that we will propose in the next section. The originality of this work is the possibility to test several different structure characterized by different technological specificities.

### 3.3 Numerical methodology

#### 3.3.1 Experimental configurations and inversion C-V characteristics

As previously said, the numerical methodology is carried out using specific experimental Capacitance-Voltage characteristics. Two types of measurements are performed on this set of devices: the gate-to-channel capacitance ( $C_{gc}$ ) and the back-gate-to-channel capacitance ( $C_{bc}$ ) [5]. These have been already defined in the first chapter in equations 2.30 and 2.38. As explained in chapter 1, Capacitance meter has two main terminals: Low and High. Whereas the High terminal imposes a static voltage ( $V_{BIAS}$ ) with a superimposed small signal voltage ( $v(t)$ ), the Low terminal, consisting of an grounded Ampere-meter, reads the current ( $I(t)$ ) which is induced by the variation of the small signal voltage. For  $C_{gc}$  measurements (Fig.3.3), the small AC signal is applied on the Gate ( $V_G=V_{G\ static}+v_g(t)$ ) and the induced capacitive current is measured on Source and Drain ( $I(t)=dQ_{ch}(t)/dt$ ). For  $C_{bc}$  measurements (Fig.3.4), the small AC signal is applied on the back side contact ( $V_B=V_{B\ static}+v_b(t)$ ) and the induced capacitive current is still measured on Source and Drain ( $I(t)=dQ_{ch}(t)/dt$ ). In both experimental configurations the Source and Drain are grounded. The back (or front) contact is not necessary grounded but it can be biased at specific value during  $C_{gc}$  measurements (or  $C_{bc}$ ). This is well known as "Capacitance Modulation". Therefore in order to calculate these capacitances, since we know the imposed voltage and the induced current, the capacitance-meter uses the following relation

$$I(t) = C \frac{dv(t)}{dt} \quad (3.1)$$

that for  $C_{gc}$  becomes

$$C = I(t) \frac{\partial t}{\partial v(t)} = \frac{-\partial Q_{ch}(V_G, V_B)}{\partial t} \frac{\partial t}{\partial V_G(t)} = -\frac{-\partial Q_{ch}(V_G, V_B)}{\partial V_G(t)} \quad (3.2)$$

and for  $C_{bc}$

$$C = I(t) \frac{\partial t}{\partial v(t)} = \frac{-\partial Q_{ch}(V_G, V_B)}{\partial t} \frac{\partial t}{\partial V_B(t)} = -\frac{-\partial Q_{ch}(V_G, V_B)}{\partial V_B(t)} \quad (3.3)$$

that are exactly identical to the relations defined in chapter 2 (2.30 and 2.38). These measurements have been performed for all the devices.

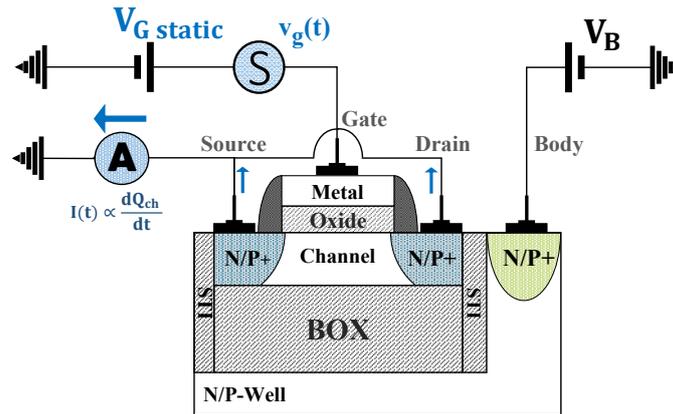
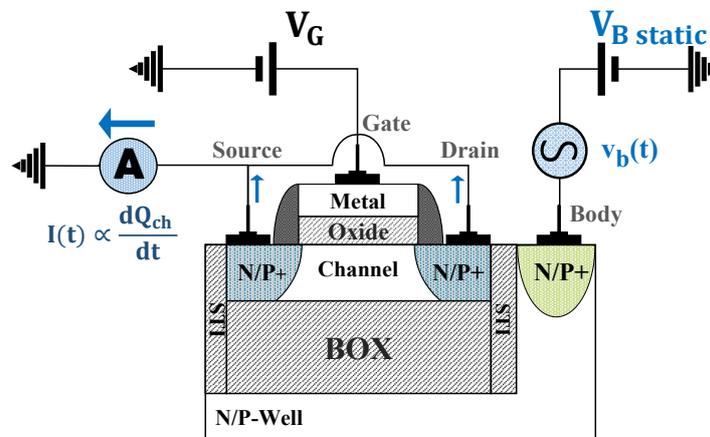
Figure 3.3: Experimental configuration for  $C_{gc}$  measurement.Figure 3.4: Experimental configuration for  $C_{bc}$  measurement.

Fig.3.5 shows the results of these experiments for the standard P-MOS GO2 device. The two measurements are respectively carried out with  $V_B=0V$  for  $C_{gc}$  (left figure) and with  $V_G=0V$  for  $C_{bc}$ . Whereas  $C_{gc}$  characteristic is well known in the literature [6, 7, 8, 9],  $C_{bc}$  characteristic is reported for the first time (right figure) [5]. The first remarkable difference is the maximum capacitance value between  $C_{gc}$  and  $C_{bc}$  capacitances. This is due to the difference of thickness between the front ( $t_{fox}$ ) and back-oxide ( $t_{box}$ ). Another remarkable difference is the voltage range for which the two characteristics varies. Indeed, whereas for  $C_{gc}$  characteristic a variation of  $\Delta V_{GS}=0.3V$  is sufficient in order to see the capacitance variation from the 10% to 90% of its maximum Capacitance value CET (weak inversion and strong inversion), for  $C_{bc}$  characteristic a variation of  $\Delta V_{BS}=1.5V$  is necessary. We remember that for  $C_{gc}$  characteristic the inversion charge is located at the front channel, close to the interface front-oxide/channel, whereas for  $C_{bc}$  characteristic the inversion charge is located at the back channel, therefore close to the interface channel/back-oxide.

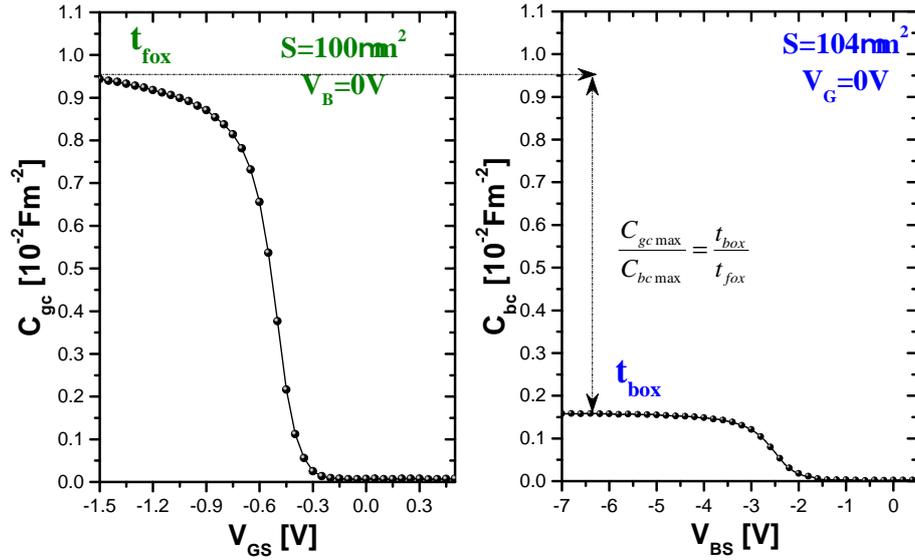


Figure 3.5: Experimental  $C_{gc}(V_{GS})$  (left figure) and  $C_{bc}(V_{BS})$  (right figure) capacitance characteristics for a standard P-MOS GO2 device.

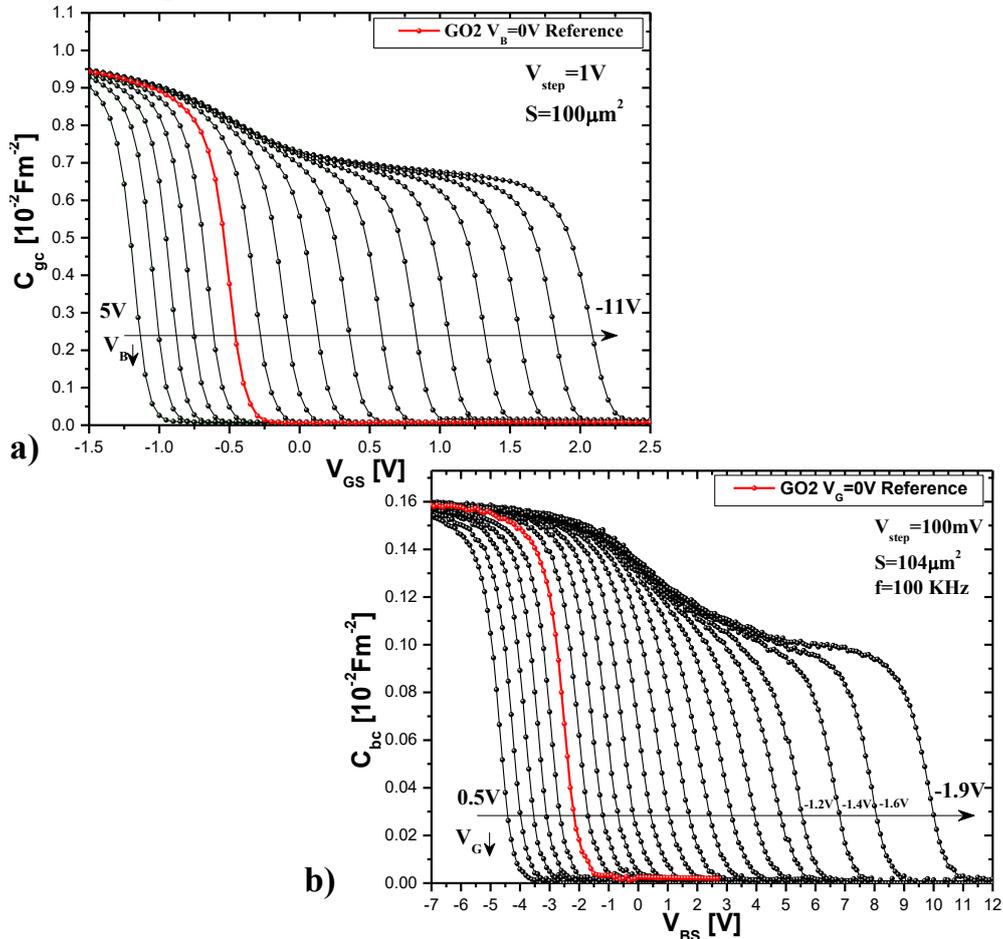


Figure 3.6: Experimental  $C_{gc}(V_{GS})$  (left top figure) and  $C_{bc}(V_{BS})$  (right bottom figure) capacitance characteristics with modulation.

As usual, the maximum capacitance of  $C_{gc}$ , during strong front-inversion, should be used for the front-oxide thickness (GO2) extraction. For the first time,  $C_{bc}$ , during strong back-inversion, can be used for the back-oxide thickness ( $t_{box}$ ) extraction. Fig.3.6 a (top-left) displays the modulation of the  $C_{gc}(V_{GS})$  curves with body bias  $V_B$  for P-MOS GO2 device, illustrating the onset of back channel inversion for negative  $V_B$ 's.  $V_B$  varies from -11V to 5V with a step of 1V.

Interestingly, with the back gate operation mode, Fig.3.6 b (bottom-right) shows that similar characteristics can be obtained for  $C_{bc}(V_{BS})$  curves with also clear formation of front channel inversion for negative  $V_G$ 's.  $V_G$  varies from -1.9V to 0.5V with a step of 0.1V. The maximum value of the capacitance for all the modulated  $C_{gc}$  and  $C_{bc}$  characteristics, reached respectively at  $V_{GS}=-1.5V$  and  $V_{BS}=-7V$ , is identical and therefore independent of the back (or front) bias voltage. These characteristics, including their modulation will be used to extract the effective work function and the equivalent oxide of all the devices previously presented.

Table 3.2: Set of different FDSOI devices featured by a combination of different process modules on metal gate, channel (Si and SiGe) and well (P and N doped) for GO1 and GO2 dielectrics. We also report on the  $V_{th}$  shifts that are observed for the different architectures.

Device	channel	Metal	Well substrate	$\Delta V_{th}$ GO1 [mV]	$\Delta V_{th}$ GO2 [mV]
N-MOS	Si	N-Gate	P	Reference	Reference
	Si	N-Gate	N	45	115
	Si	P-Gate	P	90	45
P-MOS	SiGe	P-Gate	N	Reference	Reference
	SiGe	N-Gate	P	60	90
	SiGe	N-Gate	N	100	45
	Si	P-Gate	N	320	250
	Si	N-Gate	N	X	295

As summarized in TABLE 3.1, we have the opportunity to test a significant number of devices, N-MOS and P-MOS, on which we can get various channel materials, Gate type and well type for ground plane. In order to carry out the parameter extraction of EOT and  $WF_{eff}$ , including the channel box thicknesses,  $C_{gc}$  and  $C_{bc}$  measurements, previously introduced, are performed on this set of devices.

The different  $C_{gc}$  characteristics versus  $V_{GS}$  at  $V_B=0V$  are reported for N-MOS GO1 (Fig. 3.7 right side) and GO2 (Fig. 3.8 right side) and P-MOS GO1 (Fig. 3.7 left side) and GO2 (Fig. 3.8 left side) devices.

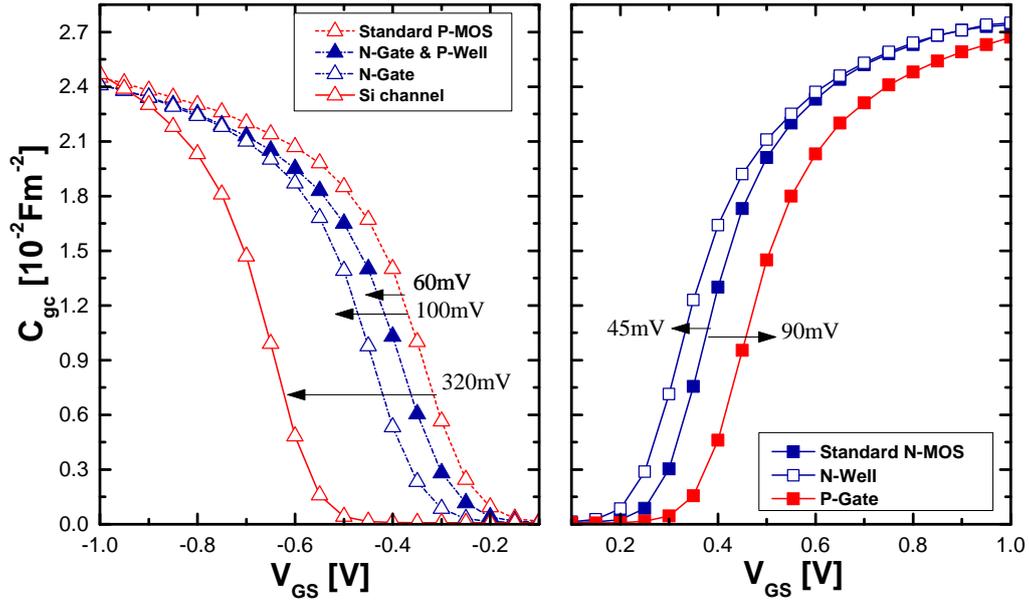


Figure 3.7: Gate-to-channel capacitance at back bias  $V_B=0V$  for P-MOS and N-MOS FDSOI GO1 with  $V_{th}$  shift with respect to the reference architecture.

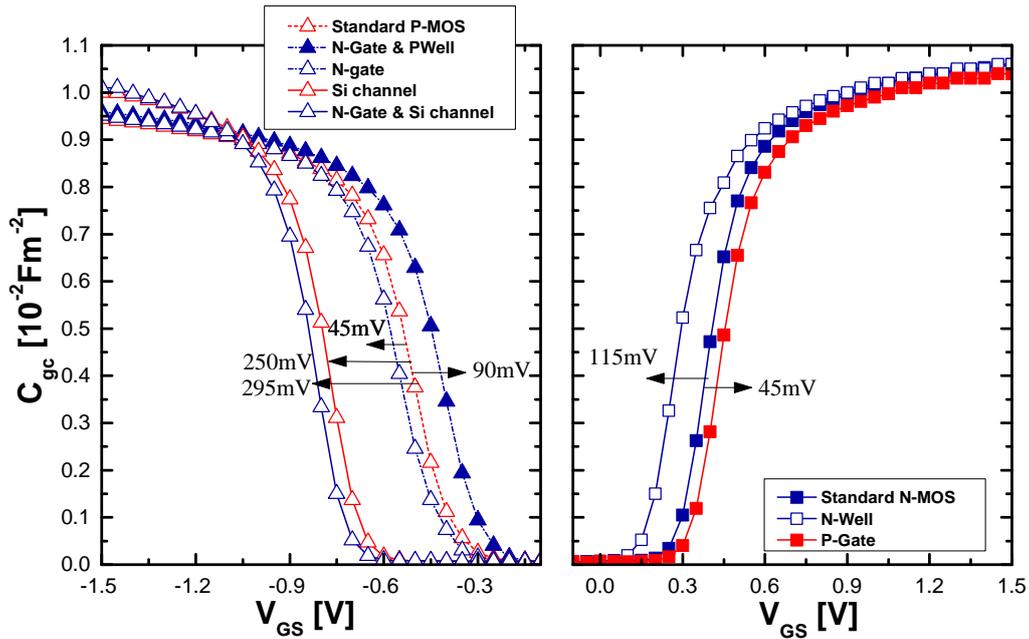


Figure 3.8: Gate-to-channel capacitance at back bias  $V_B=0V$  for P-MOS and N-MOS FDSOI GO2 with  $V_{th}$  shift with respect to the reference architecture.

The arrows in these figures identify the  $V_{th}$  shift from reference when we modify some process modules of the gate stack.  $V_{th}$  shifts are reported in TABLE 3.2. The references reported in these figures for each MOS type (N or P) correspond to the reference process given in Fig. 3.1. N-MOS reference transistor (Fig. 3.1 a) has a

N-Gate and P ground plane with a Si channel whereas P-MOS reference transistor (Fig. 3.1 b) has P-Gate and N ground plane with a SiGe channel. The  $V_{th}$  shifts are calculated at 50% of the maximum capacitance value of the reference transistors characteristics. A first observation of the impact of the process modules on  $V_{th}$  with respect to the reference Capacitance-Voltage characteristics leads to assert that

- The impact of P-Gate metal seems to be independent of the MOS type (P or N) and channel material. The only observed dependency is with dielectric type: for GO1 devices we have a  $\Delta V_{th}$  of 90-100mV and for GO2 devices we have a  $\Delta V_{th}$  of 45mV.
- The impact of the N-Well type seems to be dependent of the MOS type (P or N) and dielectric type (GO1 or GO2).
- The impact of the channel material (SiGe) seems to be dependent of the dielectric type: for GO1 devices we have a  $\Delta V_{th}$  of 320mV and for GO2 devices we have a  $\Delta V_{th}$  of 250mV.

It's obvious that these impacts are observed on the threshold voltage  $V_{th}$  but this doesn't necessary mean that the same impacts are observed on  $WF_{eff}$ . Indeed if we consider the standard N-MOS GO1 reference transistor (Fig. 3.7 blue-squares) and the same structure but with a N-Well type (Fig. 3.7 white-squares and blue line) we observe that they have a different threshold voltage ( $\Delta V_{th}=45mV$ ). Despite this different  $V_{th}$  we know that these two transistors have the same Gate stack which means same EOT and  $WF_{eff}$ . Therefore, in order to extract the proper value of  $WF_{eff}$ , we have to take into account the relationship between  $V_{th}$  and the well doping level. Unfortunately, this is not the only dependence. Indeed,  $V_{th}$  depends on other physical parameters such as buried oxide thickness, channel material and thickness and Gate metal which get tedious the correct extraction of  $WF_{eff}$ . The extraction of the correct physical FDSOI stack parameters is firstly required in order to extract then the correct  $WF_{eff}$  value.

### 3.3.2 Principles

The extraction of Gate stack parameters (EOT and  $WF_{\text{eff}}$ ) for these devices (TABLE 3.2) is obtained by fitting Quantum Simulation to experimental capacitance-voltage characteristics (C-V). Indeed, for a specific FDSOI stack device ( $WF_{\text{eff}}$ , EOT,  $t_{\text{ch}}$ ,  $t_{\text{box}}$ ,  $N_{\text{W}}$ ), we can simulate  $C_{\text{gc}}$  and  $C_{\text{bc}}$  characteristics and compare them to experimental measurements. We underline that such agreement is not a simple fitting, but we propose here a method based on a specific procedure that allows us to properly identify all the physical stack parameters including the technological parameters of the Gate stack (EOT and  $WF_{\text{eff}}$ ). This method has four main steps, that are:

1. Extraction of EOT by fitting  $C_{\text{gc}}$  characteristic at  $V_{\text{B}}=0\text{V}$ .
2. Extraction of  $t_{\text{box}}$  by fitting  $C_{\text{bc}}$  characteristic at  $V_{\text{G}}=0\text{V}$ .
3. Extraction of  $t_{\text{ch}}$  by fitting  $C_{\text{gc}}$  at large negative (or positive for N-MOS) back bias  $V_{\text{B}}$ .
4. Extraction of  $N_{\text{W}}$  by fitting  $C_{\text{gc}}$  from positive to large negative (or inversely for N-MOS) back bias  $V_{\text{B}}$

Each step of the proposed methodology requires a fitting procedure between the experimental C-V characteristic and numerical simulation in order to extract the relative physical parameter. These simulations, based on PS formalism are obtained through NUMERICAD Simulator previously introduced in chapter 2. Values of the physical parameters (such as effective masses, energy gap, dielectric constants etc..) are reported in the previous chapter. We remind only that for the Si and SiGe channel we have corrected in-plane effective masses for the heavy hole valence band (mDOS-HH xy) of  $2.5m_0$  for Si and  $1.5m_0$  for SiGe that are taken into account (2.1 and 2.2). If we write equations 2.28 and 2.36, reported in chapter 2, in terms of  $WF_{\text{eff}}$  and EOT, for  $V_{\text{G}}$  relation, we obtain

$$V_{\text{G}} = WF_{\text{eff}} - \phi_{\text{W}} - \frac{Q_{\text{sc}} \cdot EOT}{\epsilon_{\text{SiO}_2}} + \Psi_{\text{sc}} + V_{\text{B}} \quad (3.4)$$

and for  $C_{\text{gc}}$  relation

$$\frac{1}{C_{\text{gc}}} = \frac{\epsilon_{\text{SiO}_2}}{EOT} + \frac{1}{C_{\text{ch}}} + \alpha \left( \frac{\epsilon_{\text{SiO}_2}}{EOT} + \frac{1}{C_{\text{box}}} + \frac{1}{C_{\text{Well}}} \right) \quad (3.5)$$

These Relations suggest that it is not necessary to perform a simulation each time we change EOT or  $WF_{\text{eff}}$  if we keep the same channel, buried oxide thicknesses and well doping level. Once we perform a numerical simulation for a FDSOI transistor  $T_1$  ( $EOT_1$ ,  $WF_{\text{eff}1}$ ,  $t_{\text{ch}1}$ ,  $t_{\text{box}1}$  and  $N_{W1}$ ) we obtain its  $Q_{\text{sc}1}(\Psi_{\text{sc}1})$  information. We remember that  $Q_{\text{sc}}$  is the sum of the channel and well charges ( $Q_{\text{W}}+Q_{\text{ch}}$ ) and  $\Psi_{\text{sc}}$  is the sum of the potential drops across FDSOI stack ( $\Psi_{\text{ch}}+V_{\text{box}}+\Psi_{\text{well}}$ ) from which we can easily calculate  $C_{\text{ch}}$ ,  $C_{\text{box}}$ ,  $C_{\text{Well}}$  and  $\alpha$ . Therefore, we can predict analytically, without performing any other simulation, the C-V characteristic of a FDSOI transistor  $T_2$  that only differs with respect to  $T_1$  transistor for the Gate stack technological parameters ( $EOT_2$ ,  $WF_{\text{eff}2}$ ). This can be carried out with equations 3.4 and 3.5, using the previous numerical simulation  $Q_{\text{sc}1}(\Psi_{\text{sc}1})$  and the new values  $EOT_2$ ,  $WF_{\text{eff}2}$ . As previously seen in chapter 1, this is the same methodology used in the state of the Art for the standard bulk transistor in order to extract  $WF_{\text{eff}}$  and EOT.

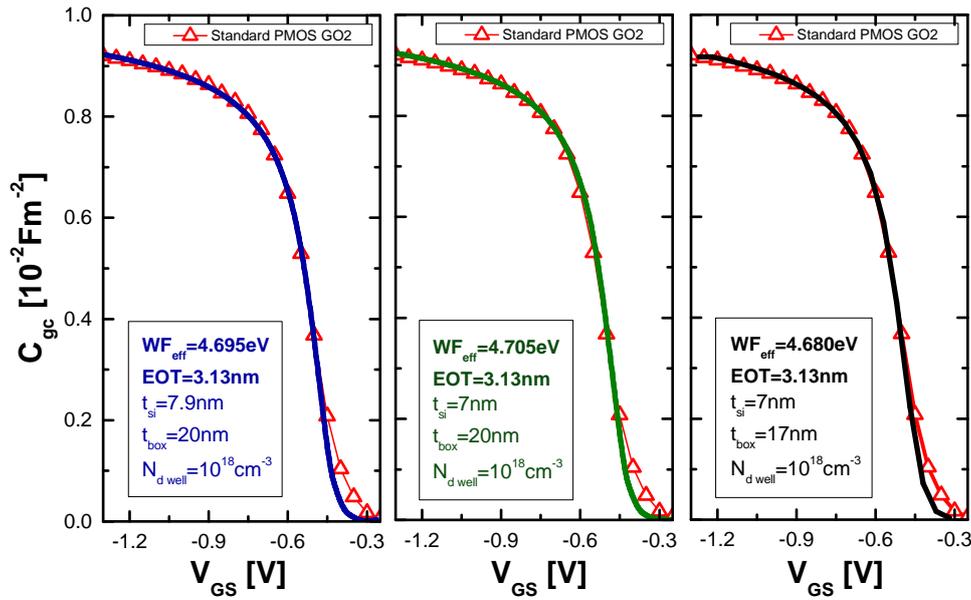


Figure 3.9: Standard PMOS GO2 Gate-to-channel capacitance compared with Simulation (NUMERICAD) with different channel and BOX thicknesses (each fit leads to a certain  $WF_{\text{eff}}$  and EOT extraction).

We can consider that  $WF_{\text{eff}}$  and EOT are correctly identified once we have found the correct values for the different FDSOI stack technological parameters ( $t_{\text{ch}}$ ,  $t_{\text{box}}$ ,  $N_{\text{W}}$ ). We can consider that it is the case if we account of the proper dependencies of the experimental capacitances with Gate and Body biases.

The first step is the identification of EOT, the equivalent thickness of the front oxide. In order to carry out this extraction, we need to fit the inversion

experimental Capacitance-Voltage characteristic  $C_{gc}(V_{GS})$  at  $V_B=0$ . In the 3 graphics of Fig. 3.9, we report  $C_{gc}(V_{GS})$  experimental characteristic for the same Standard P-MOS GO2 device (red triangles). And, for each figure, we report a numerical simulation which fits perfectly the experiment for a specific set of physical parameters ( $t_{ch}$ ,  $t_{box}$ ,  $N_W$ ). Therefore, a good fit of  $C_{gc}(V_{GS})$  can be obtained for three different set of parameters leading to three different values for EOT and  $WF_{eff}$ . These values are given with a precision of 0,01 nm and 3-4 meV. Whereas EOT is found to be independent of  $t_{box}$  and  $t_{ch}$  values (with precision below 0.01 nm), a 25meV  $WF_{eff}$  uncertainty is found.

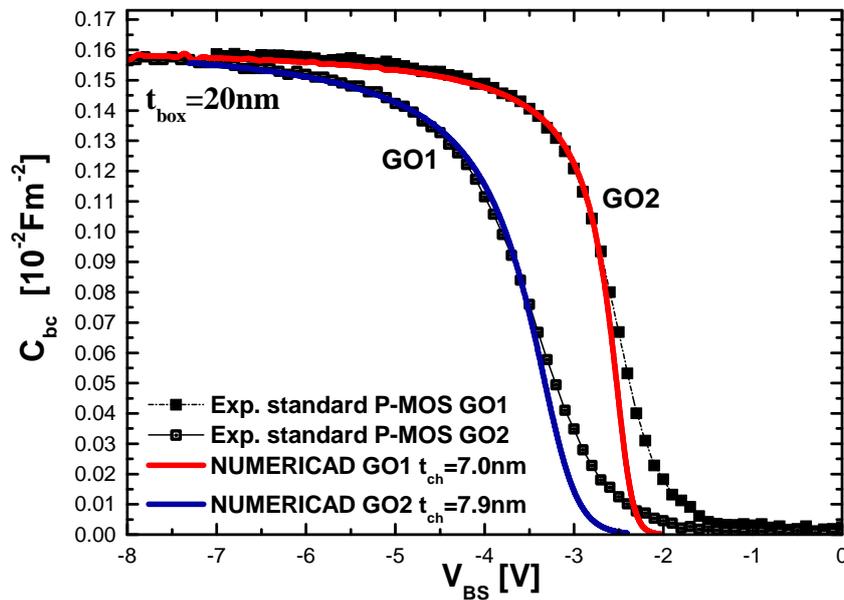


Figure 3.10: Experimental standard PMOS GO1 and GO2 back-Gate-to-channel capacitance compared to Simulation (NUMERICAD) leading to  $t_{box}$  extraction.

Such a result confirms the importance of a previous extraction on  $t_{box}$  and  $t_{ch}$  in order to accurately extract  $WF_{eff}$ . The only parameters that can be properly extracted is the equivalent oxide thickness EOT. The front oxide EOT can be extracted by applying the methodology proposed by Charbonnier et al. [10], whereas  $WF_{eff}$  remains still inaccessible.

Once the front oxide EOT is extracted, the following step is the extraction of the buried oxide thickness  $t_{box}$ . To extract  $t_{box}$ , we have recently proposed a new C-V measurement (Figs. 3.4, 3.6 and 3.5), the  $C_{bc}(V_{BS})$  earlier mentioned, with back side wafer (Body) contact as Gate. Fig. 3.10 shows back-gate-to-channel capacitance measurements results for a standard P-MOS GO1 and GO2. The corresponding CV curves for GO1 and GO2 (Fig. 3.10) shows characteristics

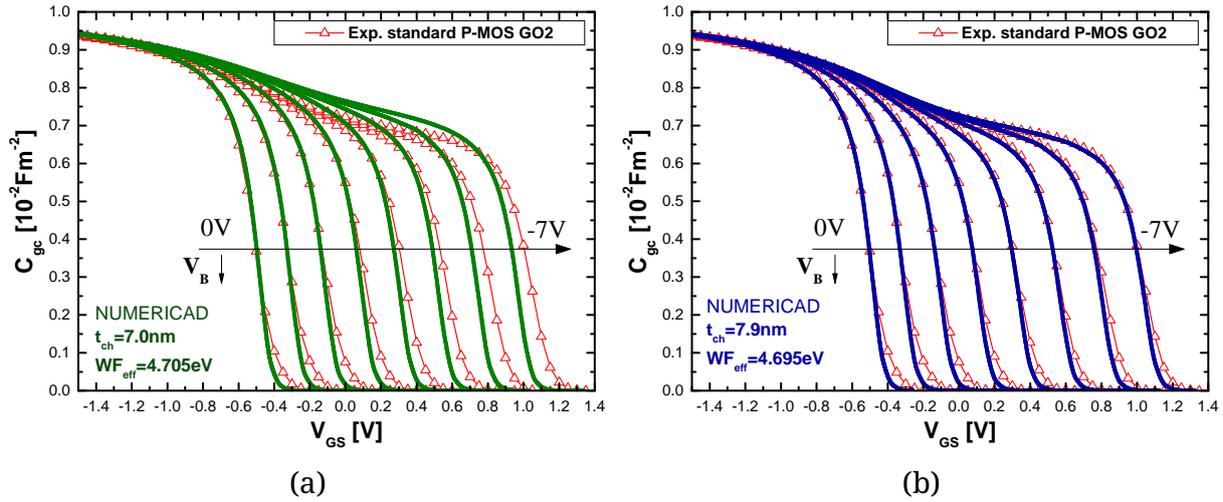


Figure 3.11: Standard PMOS GO2 Gate-to-channel capacitance vs Simulation (NUMERICAD) with two different channel thicknesses (7,9 nm  $t_{ch}$  is mandatory for fitting all CVs).

similar to the standard gate-to-channel capacitance but at a significantly lower level ( $0.16 \text{F/m}^2$  versus  $0.95 \text{F/m}^2$ ). Adjustment with quantum simulation allows a reliable extraction of the box thickness, independently of  $t_{ch}$  and EOT (or  $t_{fox}$ ) [5]. A 20 nm box thickness is necessary in order to fit  $C_{dc}(V_{BS})$  capacitance for both the standard PMOS (GO1 and GO2).

From the extraction of EOT and  $t_{box}$  found respectively at 2.85nm and 20nm for this standard P-MOS GO2 gate stack, we confirm that the hypothesis of 17nm for  $t_{box}$  is wrong. Therefore,  $WF_{eff}$  found for the third right figure in Fig. 3.9 is also not valid. Therefore, among the three first fitting solutions, only two are still a possible solution. These two simulations differs from their channel thickness value: 7.9nm for the first fitting simulation (blue line first figure of Fig. 3.9) and 7.0nm for the second fitting simulation (green line second figure of Fig. 3.9). It's obvious that in order to get the correct value of  $WF_{eff}$ , we need to extract the proper value of the channel thickness which is the last step of the methodology.  $t_{ch}$  can be obtained by comparison between simulations and experiments on a large set of CV characteristics for which back biases vary from 0V to large values leading to back interface inversion (Fig. 3.11). We can notice that there is only one channel thickness that  $V_{th}$  shift versus back biasing is varying with the channel thicknesses and only one thickness value account account for the experimental variation. It leads us to conclude that 7.9nm is the right channel thickness. Therefore the correct fitting solution is the first figure of Fig. 3.9 whose EOT,  $t_{box}$  and  $t_{ch}$  are respectively 2.85nm, 20nm and 7.9nm. this fitting result lead

to  $WF_{eff}$  value of 4.695eV for the Gate stack of the standard P-MOS GO2 transistor. This extraction is carried out by knowing the correct well doping concentration used in the numerical simulation ( $N_W=10^{18}cm^{-3}$ ).

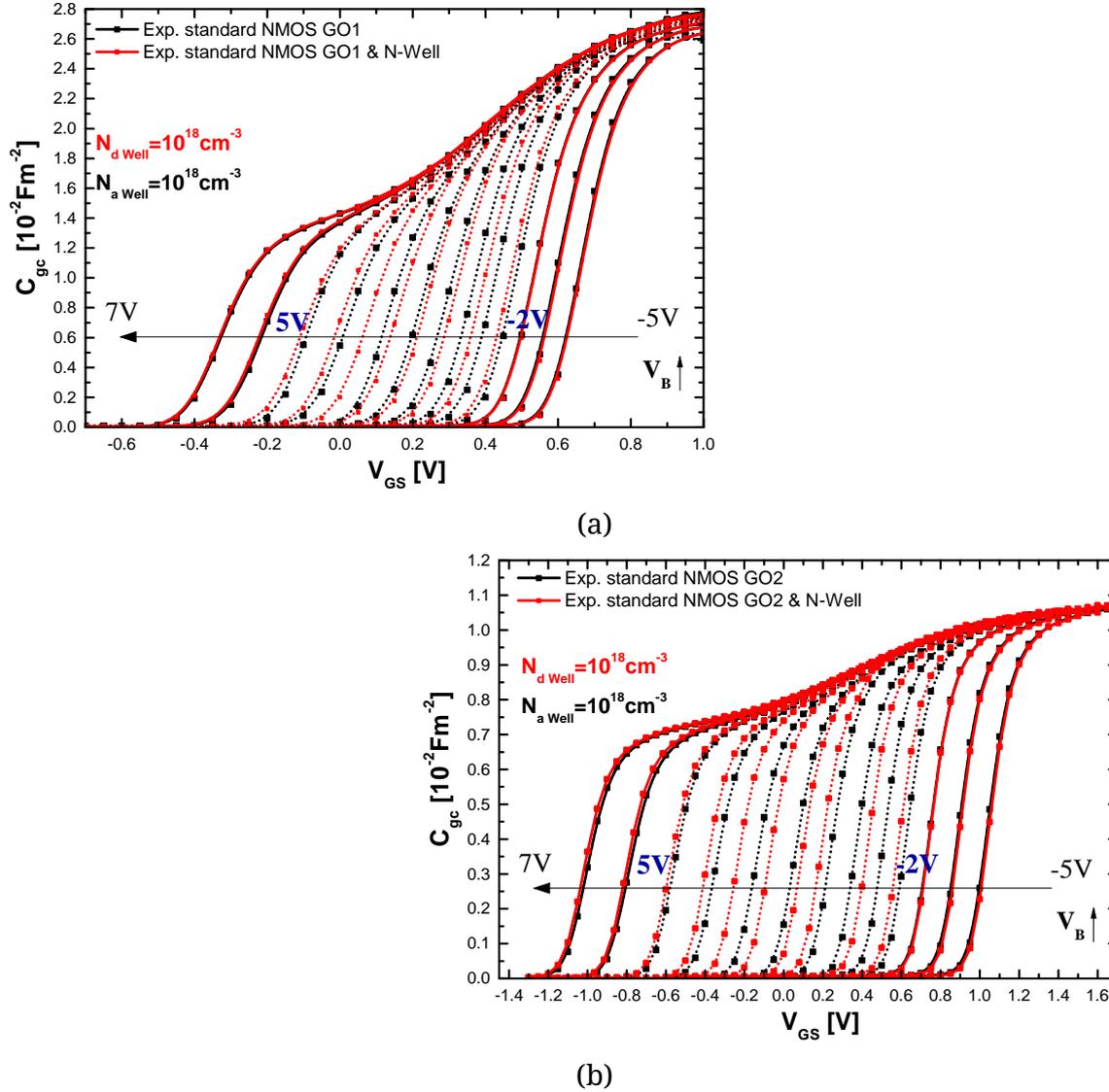


Figure 3.12: Impact of well doping on  $C_{gc}$  characteristics for GO1 and GO2.

If we choose a different doping level ( $\neq 10^{18}cm^{-3}$ ) and we impose the same value of effective work function (4.695eV) and channel thickness (7.9nm) for the numerical simulations, we will not be able to fit all the  $C_{gc}$  characteristics at different  $V_B$  of Fig. 3.11. Indeed  $V_{th}$  versus  $V_B$  depends also on the well doping level  $N_W$  for a specific  $V_B$  range.

In Fig. 3.12 a, we report the comparison of two experimental  $C_{gc}$  characteristics at different  $V_B$  of a standard GO1 N-MOS and N-MOS with N-type well (N-Well in

red and standard (P-Well) in black solid line). In Fig. 3.12 b, we report the same comparison but for a GO2 devices. As we can observe for both cases, GO1 and GO2 devices, the impact of well doping is observed just for the characteristics with a back bias that varies from -2V to 5V (characteristics in dotted-line). The impact is simply a shift among the different characteristics. The value of this shift depends firstly on the well doping concentration of the two devices and secondly on the applied Body voltage. The shift is negative as we go from P-Well to N-Well. Its amplitude varies from 5V to -2V with a maximum around 1-2 Volts. but for Body biases above 5V or -2V (solid lines in Fig. 3.12) the C-V characteristics superimpose. This observation is valid for GO1 and GO2 devices. Therefore, in order to extract  $WF_{\text{eff}}$  and EOT, we don't need to take into account the proper well doping level value in the numerical simulation since for high or really low value of  $V_B$  the characteristic  $C_{\text{gc}}$  is independent of the well concentration.

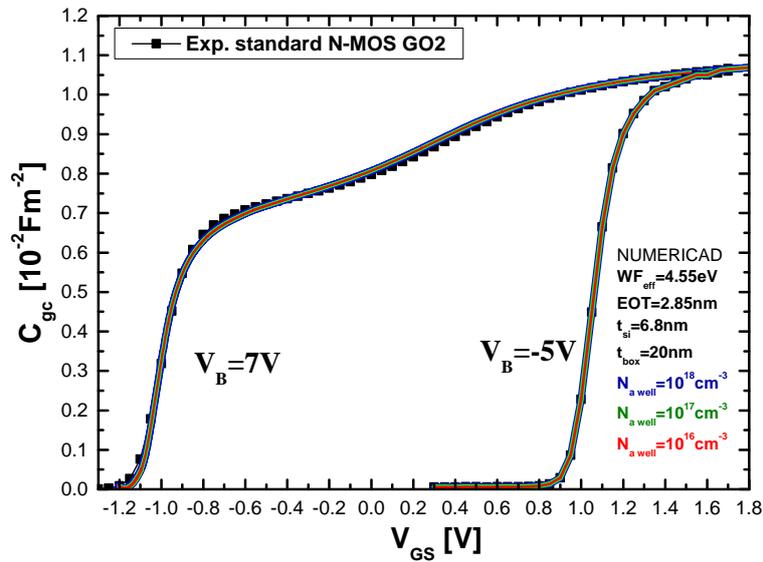


Figure 3.13: Numerical simulations with 3 different well doping level showing the independence of the extraction with the well doping level for  $C_{\text{gc}}$  at high Body voltage  $V_B=7\text{V}$  and  $-5\text{V}$ .

Since we showed, as reported in Fig. 3.12, the independence of  $C_{\text{gc}}$  characteristics at  $V_B=-7\text{V}$  and  $5\text{V}$  with the well doping level, the fitting of these two characteristics, once extracted EOT from  $C_{\text{gc}}$  characteristic and  $t_{\text{box}}$  from  $C_{\text{bc}}$  characteristic, is sufficient in order to extract  $t_{\text{ch}}$  and more importantly the proper  $WF_{\text{eff}}$  value independently of the well doping level used in the numerical simulation. This is also valid for our standard P-MOS GO2 device. This lead to obtain the technological parameters without fitting all the  $C_{\text{gc}}$  characteristics at different  $V_B$  as done in the third step of the methodology but just two

characteristics. Whereas the third step of the methodology requires the proper value of the doping level and channel thickness, the fitting of two  $C_{gc}$  characteristics at large positive and negative back biases requires only the proper value of the channel thickness.

In Fig. 3.13 we report simulations with respectively a well doping level of  $10^{16}\text{cm}^{-3}$ ,  $10^{17}\text{cm}^{-3}$  and  $10^{18}\text{cm}^{-3}$ . These simulation fitting lead to the same  $WF_{eff}$  value. The fitting of all the  $C_{gc}$  characteristics at different  $V_B$  will lead to extract the correct value of  $t_{ch}$  and  $N_W$ . By applying this methodology we can extract the technological parameters of the Gate stack of all the 15 devices.

## 3.4 Results

The numerical methodology, previously introduced, is applied on all the 15 devices in order to extract their Gate stack technological parameters (EOT,  $WF_{\text{eff}}$ ). The aim is twofold:

- to verify the coherence and robustness of the methodology on the extraction of Gate stack technological parameters (affecting EOT and  $WF_{\text{eff}}$ ).
- to investigate the impact of the different process modules on the physical parameters of the FDSOI stack.

The first target is important since it will validate the numerical extraction methodology. As previously observed, the extracted  $t_{\text{box}}$  and  $t_{\text{ch}}$  are expected to shift the threshold voltage  $V_{\text{th}}$  but not necessarily  $WF_{\text{eff}}$ . Indeed, the effective work function could also vary with channel material (Si versus SiGe) but it is obviously independent of the Source and Drain or Well type. Indeed, during the device fabrication, the implantation of the Source-Drain as well as the back substrate well is carried out without any influence on the MOS Gate stack, since carried out around the Gate stack deposition.

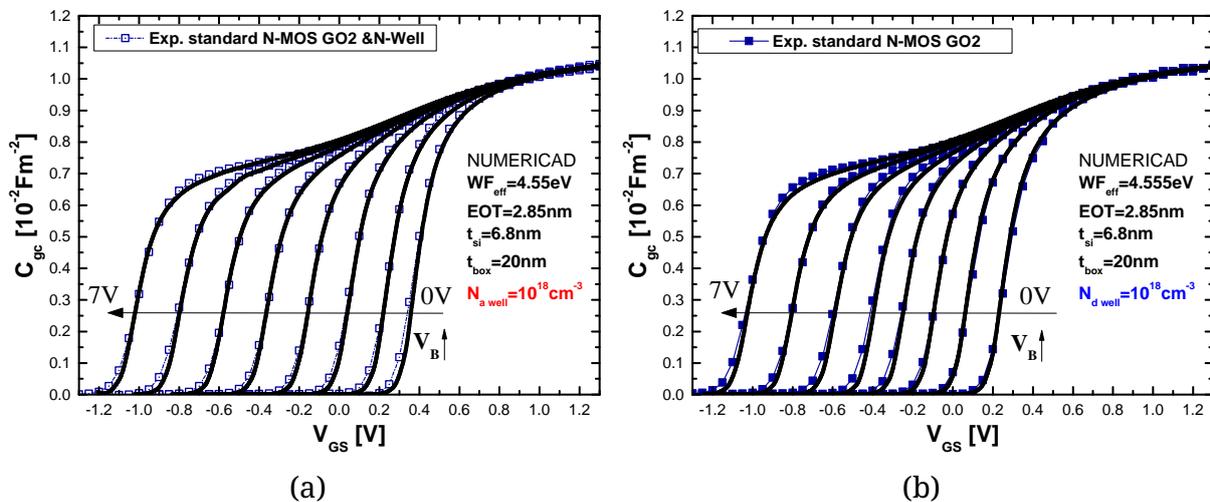


Figure 3.14: Fitting between simulations and experiments for two MOS devices having two different well types at back side of buried oxide.

The consequence is that a reliable parameter extraction must verify the independence of  $WF_{\text{eff}}$  and EOT with variations on types of Source and Drain (N or P diffusion) or Well implantation (N or P-type).

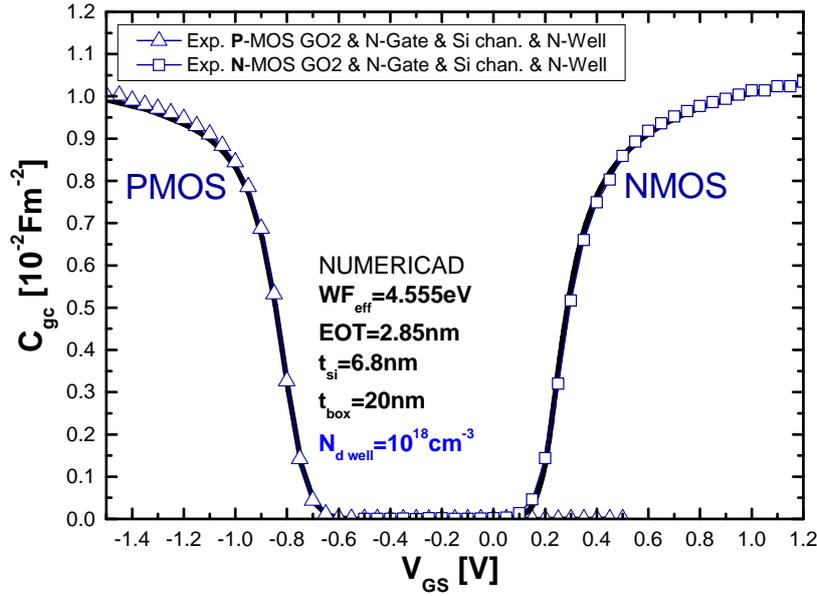


Figure 3.15: Fitting between simulation and experimental data for two different MOS devices having a same gate stack and two different Source and Drain implantation (GO2 NMOS with N-Well and GO2 PMOS with N-Well and N-Gate metal and Si channel).

The validity of the extraction methodology has been confirmed on three different MOS devices, corresponding to two different well types (Fig. 3.14) and two different MOS types as reported in Fig. 3.15. Moreover, the good fit of both the inversion characteristics in Fig. 3.15 validates the good choice of mDOS-HH of  $2.5m_0$  for Si channel [3]. Indeed, only a good value of mass, related to electrons (conduction band) and holes (valence band), can reproduce with a same  $WF_{eff}$  and EOT both capacitances in hole and electrons inversion.

$WF_{eff}$  and EOT extracted for all the fifteen tested FDSOI devices (TABLE 3.2) are reported in Fig. 3.16. The square identifies N-MOS devices whereas the triangles P-MOS devices. For what concerns the colors of these symbols, they identify the Gate metal type: red for P-Gate and blue for N-Gate. These symbols can also be solid and open which represent respectively architectures (N-MOS and P-MOS) with P-type and N-type wells. Finally, the channel type are indicated with specific circles: black for the Si channel and gray for the SiGe channel. The extraction results are reported in two graphs respectively for GO1 and GO2 architectures (Fig. 3.16). The agreement reported above on  $WF_{eff}$  and EOT for three different MOS structures (Figs. 3.15 and 3.14) is identified in Fig. 3.16 with a blue arrow. Among the fifteen different devices, other configurations correspond to same gate stack and channel material but different Source and Drain or back side well types. The extractions of their  $WF_{eff}$  and EOT lead to a good agreement which are

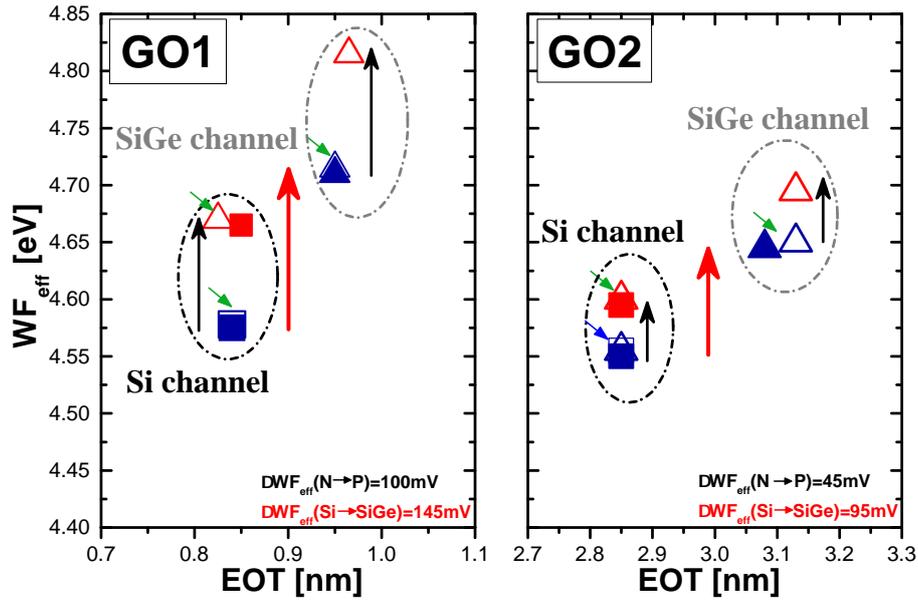


Figure 3.16:  $WF_{eff}$  versus EOT for different PMOS and NMOS FDSOI structures. Impact of Ge and sacrificial Metal gate and coherence of  $WF_{eff}$  and EOT extractions are shown.

identified with green arrows in Fig. 3.16.

This validate the proposed numerical methodology. Therefore, the accurate extraction of the physical parameters of all different devices can be used in order to investigate the impact of the different process modules over its physical parameters (thicknesses and effective work function).

Starting with the channel thickness if we report it in function of EOT for different P-MOS and N-MOS FDSOI structures we can investigate the impact of Ge material and the coherence of  $t_{ch}$  and EOT extractions. Indeed, as reported In Fig. 3.17, we can observe that the dependence of  $t_{ch}$  with EOT varies only with the channel material (Si and SiGe) and the oxide type (GO1 and GO2). Indeed, we observe in Fig. 3.17 that it is equal to 6.1 nm for Si material and 7 nm for SiGe material for all GO1 devices and 6.8 nm for Si material and 7.9 nm for SiGe material for all GO2 devices. Therefore, in case of SiGe channel devices, we found that the channel thickness is found to be 1 nm thicker than Si channel devices Moreover, the dielectric type (GO2 and GO1) plays a role in the final channel thickness value. Indeed we found that the GO2 process module leads to less channel consumption than GO1 process for both Si and SiGe channel material.

For what concerns the buried oxide thickness  $t_{box}$ , we report it as function of EOT on Fig. 3.18 and it is found at the same 20 nm value for all the different MOS devices, a value corresponding to the target of the SOI substrate. Therefore,

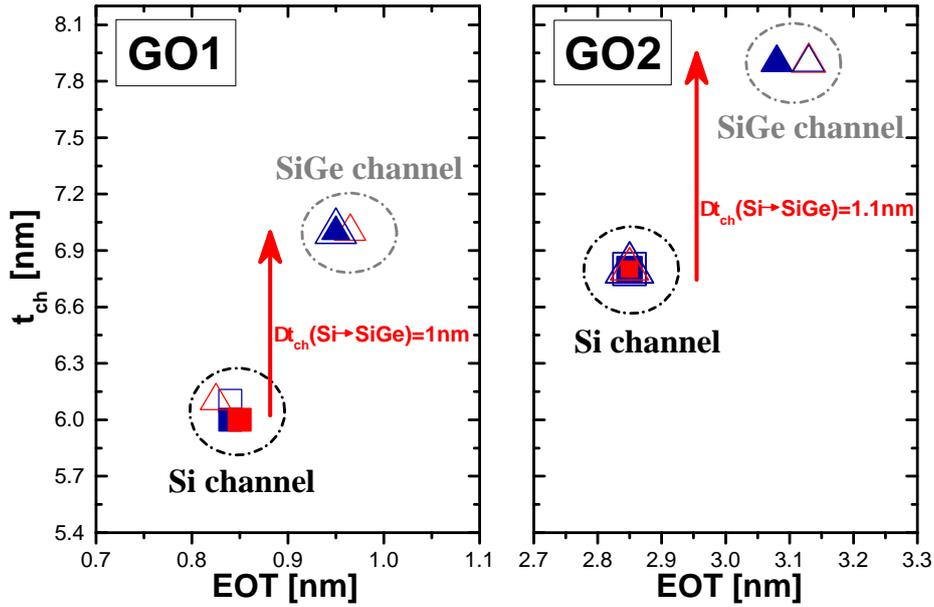


Figure 3.17:  $t_{ch}$  versus EOT for different PMOS and NMOS FDSOI structures.

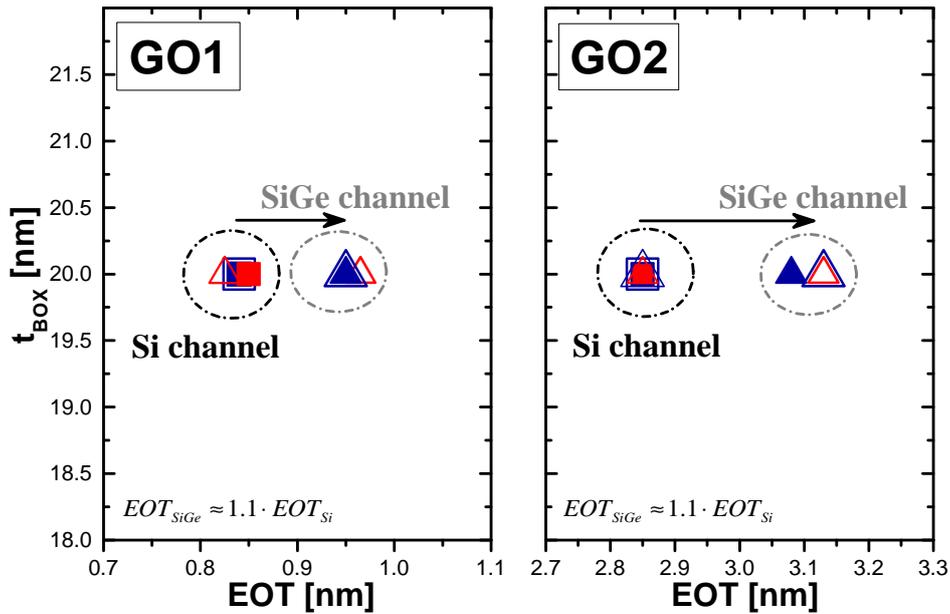


Figure 3.18:  $t_{box}$  versus EOT for different PMOS and NMOS FDSOI structures.

we can conclude that the different process modules don't affect the buried oxide thickness.

Different is the extraction result for the equivalent oxide thickness with respect to the buried oxide. Indeed, as reported in Figs. 3.16, 3.17 and 3.18 we observed that EOT depends on oxide type (GO1 and GO2) but also on channel material (Si and SiGe). As already evidenced in previous studies of Soussou et al. [11], the

gate oxide formation leads to a slight interlayer thickness increase in case of MOS transistors with SiGe substrate. We notice here an interlayer regrowth around 0.12 nm for all GO1 SiGe channel devices and 0.3 nm for all GO2 SiGe channel devices.

Finally, the last technological parameter, that we want to analyze, is the effective work function. As can be observed in Fig. 3.16,  $WF_{\text{eff}}$  depends on Gate type, channel material and oxide (GO1 and GO2). Considering first the GO1 devices, we notice an average shift of 100mV from N to P metal gate. It is the expected effect of Al dipole created at HfON/SiON interface by the sacrificial gate process proposed by Suarez Segovia et al. [1] (see Paragraph 3.2). Moreover, with SiGe channel material,  $WF_{\text{eff}}$  evidences an additional shift of 145 mV. In Fig. 3.7 we can observe that  $V_{\text{th}}$  shift with SiGe channel reaches 320 mV. It is partially explained by the shift of valence band for SiGe semiconductor and this is already take into account through PS simulation, but an additional  $WF_{\text{eff}}$  shift of 145 mV is required to account for the whole  $V_{\text{th}}$  shift. It has been attributed to an interface dipole at SiGe/SiON interface [11]. For GO2 devices the observe effect are similar but with smaller amplitude. Both dipoles at HfON/SiON and SiGe/SiON device interfaces decreases of 45 and 95 mV, respectively.

## 3.5 Conclusion

We can conclude that the validated numerical methodology allows us to extract in precise and coherent way all the physical parameters of a specific FDSOI stack. The numerical extraction is carried out on 15 different devices which makes this work original with respect to any previous work. It is based on 3 main steps that are: (1) identification of front oxide EOT, (2) identification of the buried oxide and (3) identification of the channel thickness. This extraction procedure is necessary in order to obtain the proper  $WF_{eff}$  value of the 15 different devices.

The obtained results from the numerical extraction allows us to observe the impacts of the different modules on the technological parameters which are the following:

- The sacrificial Gate induces a  $WF_{eff}$  shift of 100mV for GO1 devices and 45mV for GO2 devices. This is associated to the presence of an induced dipole at the interface HK/SiO<sub>2</sub> which is different for GO1 and GO2 dielectrics.
- The buried oxide thickness (20nm) is found to be independent of any process module. Therefore, no impact is observed with the different technological processes.
- The channel thickness is found to be 1nm thicker with GO2 devices compared to GO1 devices since GO2 deposition leads to less channel consumption. Moreover, the channel thickness is found to be 1nm thicker for devices with SiGe channel material compared to devices with Si channel material.
- An hypothesis of the presence of the dipole (150mV) with SiGe channel at the front-oxide/channel interface is made in order to account of observed experimental  $V_{th}$  shift (320mV) between the  $C_{gc}$  characteristics. This has to be proved in the next chapters.

Despite this precise extraction, that leads for the first time to  $WF_{eff}$  extraction, the numerical methodology defects in terms of time and computation cost (complicated numerical procedure) which are fundamental in order to carry fast statistical analysis. Therefore in order to extract the FDSOI technological parameters including  $WF_{eff}$  in a faster, less complicated and accurate (such as the methodology presented in this chapter) new analytical methodologies are necessary with respect to the numerical methodology.

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# Chapter 4

## Analytical characterization of FDSOI stack based on inversion C-V measurements and linear regression

### 4.1 Introduction

In the previous chapter, we have seen that the numerical methodology allows us to extract all the FDSOI thicknesses (EOT front oxide, channel and buried oxide) including  $WF_{\text{eff}}$ . Despite its precision and validity, it leads to very high computational and time costs which are fundamental for the statistical analysis. Indeed, we remind that in the numerical methodology each thickness has to be extracted through a fitting procedure between the experimental C-V characteristic and the numerical simulation based on PS formalism which makes it complicate and really expensive in terms of time. The numerical approach is not convenient to obtain fast results. Another approach that can overcome these issues related to the time and computational cost is the analytic procedure. Indeed, the major incentive for recent researches has been to attain simple analytical methods in order to extract the most important technological MOS stack parameters. The criterion are threefold:

- fast
- simple
- less expensive

The extraction of the different FDSOI stack thicknesses is the primary goal of this chapter. It is why that we will present an analytical method based on linear regression which allows us to extract specifically the EOT front oxide, buried oxide and channel thicknesses in a faster way than to the numerical approach. This methodology is based on C-V measurements such as the previous numerical methodology. These are the inversion C-V measurements ( $C_{gc}(V_{GS})$  and  $C_{bc}(V_{BS})$ ) which are already presented in chapter 3.

Therefore, in the first part of this chapter the principles of the analytical methodology, based on Boltzmann formalism, will be presented in order to extract the different FDSOI stack thicknesses. Instead, the second part of the chapter mainly will focus on the validity of the analytical extraction methodology. Indeed, Quantum numerical simulation will be compared to the extraction results which are obtained within Boltzmann formalism. Finally, in the last part of the chapter we will discuss about the limits and advantages of the analytical approach with respect to the previous numerical methodology.

## 4.2 Analytical extraction methodology based on linear regression

In the chapter 2 we have obtained, through FDSOI band diagram analysis, the complex analytical expressions of  $C_{gc}$  and  $C_{bc}$  capacitances depending on the parameters  $\alpha$  and  $\beta$ . These relations 2.36 and 2.42 can be simplified under specific electrostatic conditions, therefore at specific  $V_G$  and  $V_B$  voltages. Starting from  $C_{gc}$  characteristics, considering that we are at large front-inversion, we can assume that  $\alpha = dQ_{well}/dQ_{ch} = 0$ . Indeed no variation of the well charge is induced by  $V_G$  small signal variation due to the screening effect [2, 3] of the free channel carriers at the front channel. Therefore starting from the  $C_{gc}$  capacitance relation (eq.2.36), we obtain simply that

$$\frac{1}{C_{gc}} = \frac{1}{C_{fox}} + \frac{1}{C_{ch}} + \alpha \left( \frac{1}{C_{fox}} + \frac{1}{C_{box}} + \frac{1}{C_{well}} \right) \simeq \frac{1}{C_{fox}} + \frac{1}{C_{ch}} \quad (4.1)$$

The gate-to-channel capacitance depends only on the front-oxide and channel capacitance at strong front-inversion. A simple calculation of  $1/C_{ch}$  can be obtained in case of Boltzmann approximation. Indeed, by assuming that the inversion channel carrier is located exactly at the interface front-oxide-channel and using Boltzmann formalism [4] we know that the inversion charge  $Q_{ch\ inv}(z_S)$  is proportional to  $e^{B\phi(z_S)}$  where  $B = \frac{q}{k_B T}$ . Therefore,  $C_{ch}$  can be defined as  $BQ_{ch\ inv}$ . This leads us, as reported in the work of T. Poiroux [5] to reduce equation 4.1 to

$$\frac{1}{C_{gc}} \simeq \frac{1}{C_{fox}} + \frac{1}{C_{ch}} = \frac{1}{C_{fox}} + \frac{\partial\phi(z_S)}{\partial Q_{ch\ inv}} = \frac{1}{C_{fox}} + \frac{1}{BQ_{ch\ inv}} \quad (4.2)$$

where  $Q_{ch\ inv}$  is the integral of  $C_{gc}$  capacitance. This relation can be used, as proposed by Imed Ben Akkez [6], to extract the front-oxide thickness. Indeed a plotting of the reciprocal capacitance versus the reciprocal inversion charge leads to a straight line. With a linear regression [7], we can extract the reciprocal front-oxide capacitance (therefore its thickness) from the y-axis intercept and the value of B from the inverse of the slope as shown in Fig. 4.1 for a standard P-MOS GO2. This methodology can be approximate for two specific reasons. Firstly the linear characteristic (black line in in Fig. 4.1) is calculated with the linear regression over a small region ( $Q_{ch\ inv}^{-1}$ ) which means imprecision on B value. An imprecision of B value also impact the value of the oxide thickness obtained at y-axis interception. We remind that B here is considered as a pure

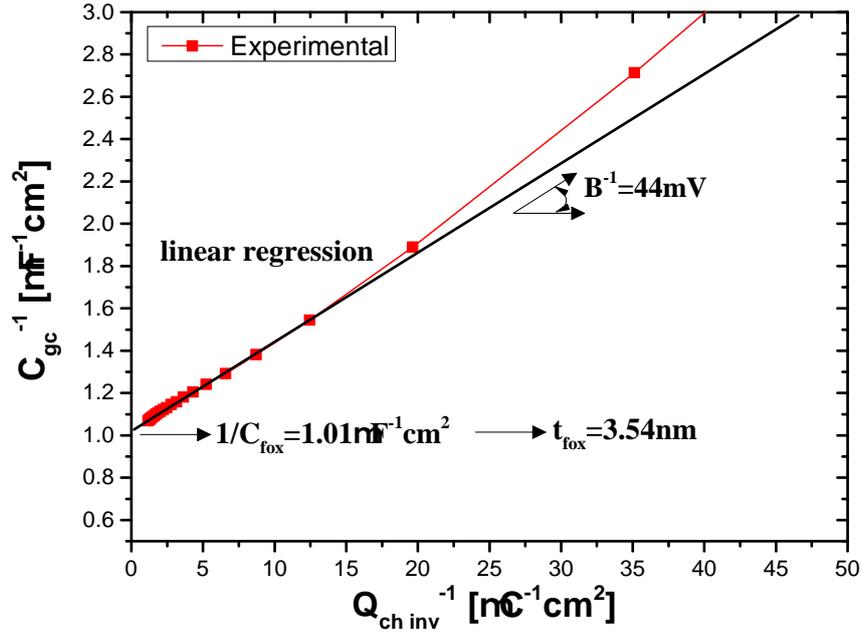


Figure 4.1: Linear plot of  $1/C_{gc}(V_{GS})$  versus  $1/Q_{ch\ inv}(V_{GS})$  allowing the extraction of the front-oxide thickness for a standard P-MOS GO2 device.

fitting parameter whose obtained value, from the inverse slope, ( $B^{-1}=44\text{mV}$ ) is really different from the expected theoretical and physical value at 300 Kelvin ( $B^{-1}=26\text{mV}$ ) [4].

Due to the limited region for which the linear regression is applied in the previous extraction methodology and consequently its incertitude on the oxide thickness value extraction, we propose for the first time an alternative approach. By multiplying both side of the equation 4.2 by  $Q_{ch\ inv}$  we obtain

$$\frac{Q_{ch\ inv}}{C_{gc}} = \frac{Q_{ch\ inv}}{C_{fox}} + \frac{1}{B} \quad (4.3)$$

This relation suggests that plotting  $Q_{ch\ inv}/C_{gc}$  should give straight lines versus  $Q_{ch\ inv}$ . As reported in Fig. 4.2 for  $V_B=0\text{V}$ , the relation is linear and from the slope ( $\eta_{fox}$ ) we can extract the classical reciprocal front-oxide capacitance and its corresponding thickness, it leads to a slightly different value with respect to the former methodology: 3.48nm (with our methodology) and 3.54nm [6] of  $t_{fox}$ . This difference can be explained by observing the two characteristics on which the extraction is carried out. Indeed, it's obvious that it's easier and more reliable to calculate the value of the oxide thickness from the large linear region of Fig. 4.2 than the small linear region of Fig. 4.1.

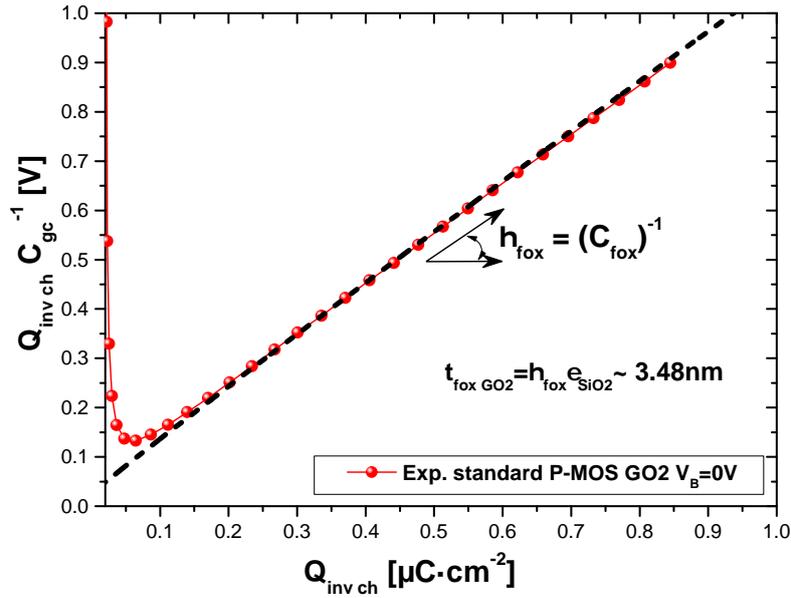


Figure 4.2: Linear plot of  $Q_{ch\ inv}/C_{gc}(V_{GS})$  versus  $Q_{ch\ inv}(V_{GS})$  allowing the extraction of the front-oxide thickness for a standard P-MOS GO2 device.

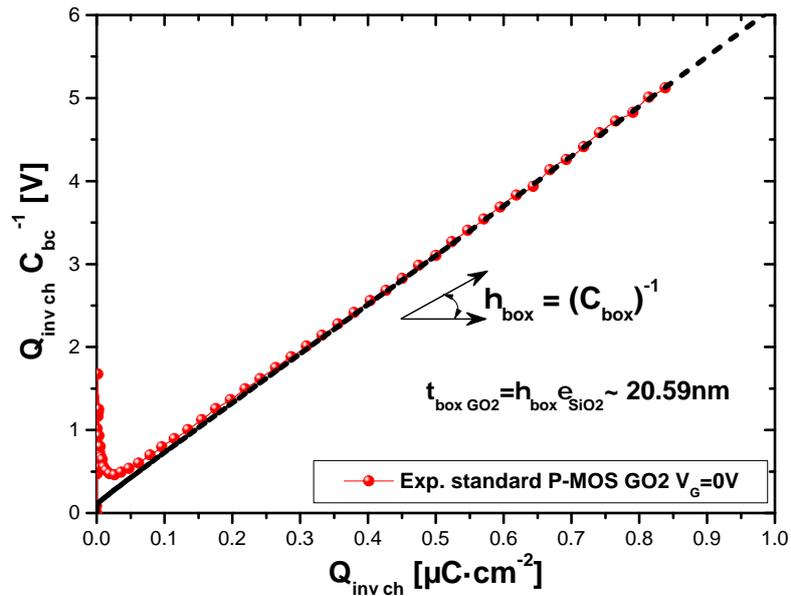


Figure 4.3: Linear plot of  $Q_{ch\ inv}/C_{bc}(V_{BS})$  versus  $Q_{ch\ inv}(V_{BS})$  allowing the extraction of the back-oxide thickness for a standard P-MOS GO2 device.

This methodology can be applied as well on  $C_{bc}$  characteristic [8, 9] in order to extract the box capacitance and its thickness. For large back-inversion condition (i.e. fig.3.5  $C_{bc}$  for  $V_{BS} > -4V$ ) we can assume that  $\beta = dQ_m/dQ_{ch} = 0$ . Indeed no variation of the metal charge is induced by  $V_B$  small signal variation due to the screening by channel layer of any back side modulation of inversion layer at the

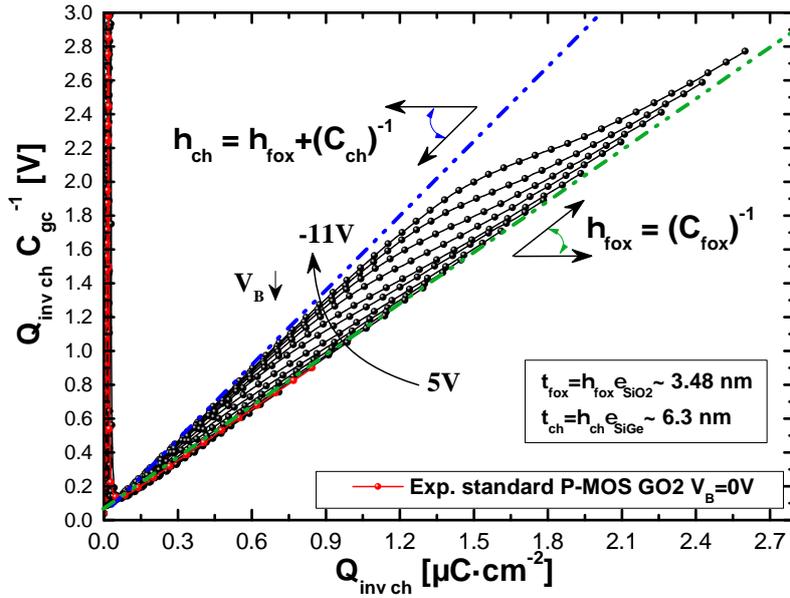


Figure 4.4: Linear plot of  $Q_{ch\ inv}/C_{gc}(V_{GS})$  versus  $Q_{ch\ inv}(V_{GS})$  from  $V_B=5V$  to  $V_B=-11V$  allowing the extraction of the front-oxide and channel thickness for a standard P-MOS GO2 device.

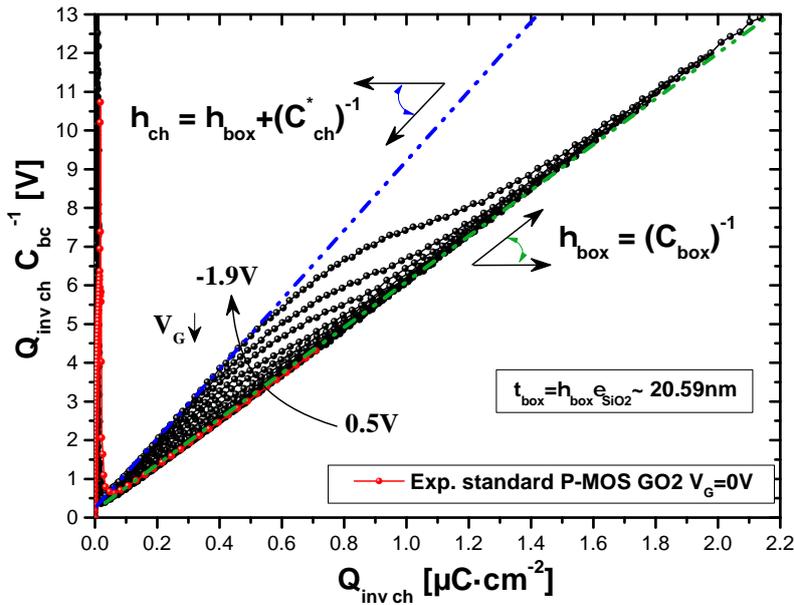


Figure 4.5: Linear plot of  $Q_{ch\ inv}/C_{bc}(V_{BS})$  versus  $Q_{ch\ inv}(V_{BS})$  from  $V_{GS}=0.5V$  to  $V_{GS}=-1.9V$  allowing the extraction of the back-oxide thickness for a standard P-MOS GO2 device.

back channel. As  $\beta$  is zero,  $\alpha=dQ_W/dQ_{ch}=-1$  since the variation of the channel and well charge is identically induced by  $V_B$ . Therefore from equation 2.42 we obtain

that

$$\frac{1}{C_{bc}} = \frac{1}{C_{ch}} + \frac{1}{C_{box}} + \beta \left( \frac{1}{C_{fox}} + \frac{1}{C_{box}} \right) + \frac{-\alpha}{C_{Well}} \simeq \frac{1}{C_{ch}} + \frac{1}{C_{box}} + \frac{1}{C_{Well}} \quad (4.4)$$

The back-Gate-to-channel capacitance depends only on the back-oxide, channel and well capacitance. We remind that during  $C_{bc}$  measurement, at large negative  $V_{BS}$  bias (P-MOS), the channel is in strong back inversion condition (holes) and the well substrate is in really strong accumulation condition (electrons). Moreover, the well capacitance is much larger than the buried oxide capacitance since in accumulation condition and it can be neglected. Therefore  $C_{bc}$  depends primarily on the channel and buried oxide capacitance at strong back channel inversion condition. By assuming that the inversion channel carrier is located exactly at the interface channel-back-oxide (where  $Q_{ch\ inv}(z_F)$  is proportional to  $e^{B\phi(z_F)}$ ) and the well capacitance is negligible, equation 4.4 reduces to

$$\frac{1}{C_{bc}} \simeq \frac{1}{C_{box}} + \frac{1}{C_{ch}} = \frac{1}{C_{box}} + \frac{1}{\partial Q_{ch\ inv}} = \frac{1}{C_{box}} + \frac{1}{BQ_{ch\ inv}} \quad (4.5)$$

where  $Q_{ch\ inv}$  is the integral of  $C_{bc}$ . By multiplying both side of the equation by  $Q_{ch\ inv}$  we obtain

$$\frac{Q_{ch\ inv}}{C_{bc}} = \frac{Q_{ch\ inv}}{C_{box}} + \frac{1}{B} \quad (4.6)$$

This relation, similar to  $C_{gc}$  case (eq. 4.3), suggests as well that plotting  $Q_{ch\ inv}/C_{bc}$  should give straight lines versus  $Q_{ch\ inv}$ . As reported in Fig. 4.3 for  $V_G=0V$ , the relation among them is linear and from the slope ( $\eta_{box}=1/C_{box}$ ) we can extract the classical reciprocal back-oxide capacitance and its corresponding thickness leading to 20.59nm for  $t_{box}$  value (classical back-oxide thickness).

By applying this methodology for all the  $C_{gc}$  curves at different  $V_B$  and all the  $C_{bc}$  curves at different  $V_G$  we should obtain again straight line at respectively strong front and back inversion channel conditions. Therefore equations 4.3 and 4.6 can be generalized in terms of  $V_B$  and  $V_G$  as follows

$$\frac{Q_{ch\ inv}(V_B)}{C_{gc}(V_B)} = \frac{Q_{ch\ inv}(V_B)}{C_{fox}} + \frac{1}{B} \quad (4.7)$$

$$\frac{Q_{ch\ inv}(V_G)}{C_{bc}(V_G)} = \frac{Q_{ch\ inv}(V_G)}{C_{box}} + \frac{1}{B} \quad (4.8)$$

In Figs. 4.4 and 4.5,  $Q_{ch\ inv}/C_{gc}$  and  $Q_{ch\ inv}/C_{bc}$  versus  $Q_{ch\ inv}$  curves for different  $V_G$  and  $V_B$  are reported. With  $Q_{ch\ inv}/C_{gc}(V_B)$  characteristics (Fig. 4.4), we

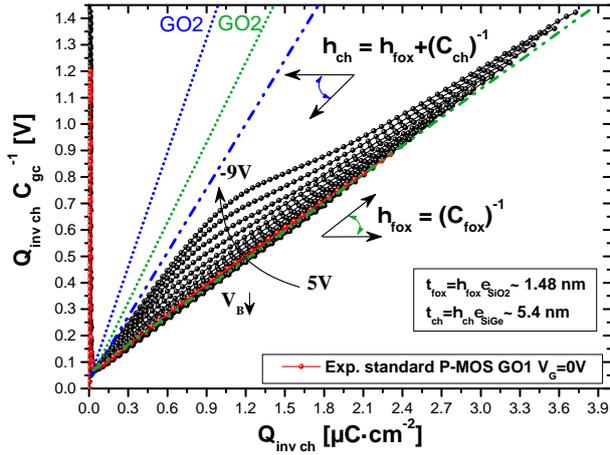


Figure 4.6: Linear plot of  $Q_{ch\ inv}/C_{gc}(V_{GS})$  versus  $Q_{ch\ inv}(V_{GS})$  allowing the extraction of the front-oxide and channel thickness for a standard P-MOS GO1 device.

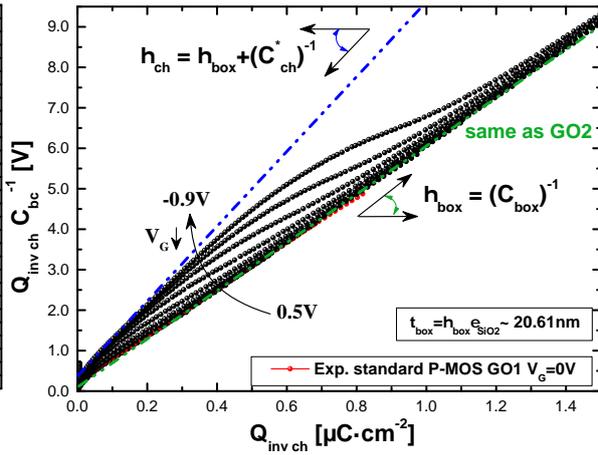


Figure 4.7: Linear plot of  $Q_{ch\ inv}/C_{bc}(V_{BS})$  versus  $Q_{ch\ inv}(V_{BS})$  allowing the extraction of the back-oxide and channel thickness for a standard P-MOS GO1 device.

notice the different impact of  $V_B$  bias with respect to the characteristic at  $V_B=0V$  (red line). Whereas for positive  $V_B$  voltages no effect is observed and therefore superimposition occurs, for negative  $V_B$  voltages the characteristics start to detach from the reference characteristic ( $V_B=0V$ ) and specifically at large negative voltage ( $V_B=-11V$ ) another linear region appears, for low  $Q_{ch\ inv}$  values, featuring a higher slope with respect to the reference curve. This region can be used in order to extract the channel thickness. Indeed as observed in chapter 2, at large negative  $V_B$  voltage the onset of the channel inversion is located at the interface channel/back-oxide while the channel is almost fully depleted. Therefore in this linear region, the experimental capacitance corresponds to oxide and channel capacitances in series. Equation 4.7 should be rewritten as

$$\frac{Q_{ch\ inv}}{C_{gc}(V_B)} = \left( \frac{1}{C_{fox}} + \frac{1}{C_{ch}} \right) Q_{ch\ inv} + \frac{1}{B} \quad (4.9)$$

Therefore Fig. 4.4 clearly exhibits two asymptotic lines with small slope value ( $\eta_{fox}=1/C_{fox}$  in green dashed-dotted line) equal to reciprocal front-oxide capacitance (same line in green of fig. 4.2) and large slope (blue line) value equal to reciprocal gate-through-silicon capacitance ( $1/C_{fox}+1/C_{ch}$  where  $C_{ch}=\epsilon_{ch}/t_{ch}$ ). Therefore, it allows the extraction of front-oxide and channel thickness. Whereas  $t_{fox}$ , with respect to fig. 4.2, can be obtained from positive to large negative  $V_B$ , the thickness channel is found only with characteristics at very large negative  $V_B$  whose slope is calculated at very low charge level. A value of 6.3nm for the

channel thickness is found for this standard GO2 P-MOS. The relation used for the thickness channel is justified by analyzing the distribution charge at large negative back biases, as previously said.

Similar discussion can be done for  $C_{bc}$  characteristics, as reported in Fig. 4.5. The impact of  $V_G$  front bias on  $C_{bc}$  characteristics is similar to the impact of  $V_B$  back bias on the  $C_{gc}$  characteristics. Whereas for positive  $V_G$  voltages no effect is observed and therefore superimposition occurs with the reference characteristic ( $V_G=0V$  red line), for negative  $V_G$  voltages the characteristics starts to detach from the reference characteristic ( $V_G=0V$ ) and specifically at large negative voltage ( $V_G=-1.9V$ ) another linear region appears, for low  $Q_{ch\ inv}$  values, featuring a higher slope with respect to the reference curve. In this region, the inversion onset occurs at the interface front-oxide-channel. Therefore the capacitance seen is the result of the series of the channel, back oxide and well capacitances and we have

$$\frac{Q_{ch\ inv}}{C_{bc}(V_G)} = \left( \frac{1}{C_{box}} + \frac{1}{C_{ch}} + \frac{1}{C_{Well}} \right) Q_{ch\ inv} + \frac{1}{B} \quad (4.10)$$

Two asymptotes are evidenced, such as for  $C_{gc}$ , with small slope value (green dash-dot line) equal to the classical reciprocal back-oxide capacitance (same line in green of Fig.4.3) and large slope (blue dash-dot line) value equal to reciprocal well-through-silicon capacitance ( $1/C_{box}+1/C_{ch}+1/C_{Well}$  where  $C_{ch}=\epsilon_{ch}/t_{ch}$  and  $C_{ch}^*=C_{well}/C_{ch}$ ). Therefore  $C_{Well}$  has to be known in order to extract the thickness channel.

Results for a standard P-MOS GO1 device are reported in figs. 4.6 and 4.7 where corresponding value of  $t_{fox}=1.28nm$ ,  $t_{box}=20.61nm$  and  $t_{ch}=5.4nm$  are obtained. In order to carry out these extractions for FDSOI SiGe and Si channel based devices, specific value of the channel dielectric constant  $\epsilon_{ch}$  are used for  $t_{ch}$  extraction. Indeed, for an expected 25% of germanium concentration for a standard P-MOS device, a value of  $12.875\epsilon_0$  is taken into account. This value is calculated from Schaffler relation [10]

$$\epsilon_{Si_xGe_{1-x}} = \epsilon_{Si} + 4.7x\epsilon_0 \quad (4.11)$$

where  $\epsilon_{Si}=11.7\epsilon_0$  and  $x$  is the percentage of Germanium present in the semiconductor.

### 4.3 Comparison with NUMERICAD simulation and quantum correction

The proposed methodology uses a Boltzmann formalism which doesn't take into account the quantum nature of the charge in the channel [11, 12, 13, 14, 15]. Using Boltzmann formalism implies to have an ideal charge located exactly at the interface between front-oxide and channel or channel and back-oxide during strong front inversion or back inversion respectively for  $C_{gc}$  and  $C_{bc}$  characteristics. This doesn't reflect the real distribution of the channel charge which needs a Schrodinger formalism as described in Chapter 2 where phenomenon such as dark space and wave function penetration [16] are occurring. Therefore, a discrepancy between the extracted values, obtained with Boltzmann formalism, of the different FDSOI stack layers and the effective ones is expected. NUMERICAD simulations (UTOXPP) including quantum effects can also accounts very accurately of experimental dependence of gate and body capacitance with  $Q_{ch\,inv}$ . Indeed, the fit authorizes an accurate evaluation of the different MOS layer thicknesses. Therefore, the accuracy of the experimental methodology can be validated.

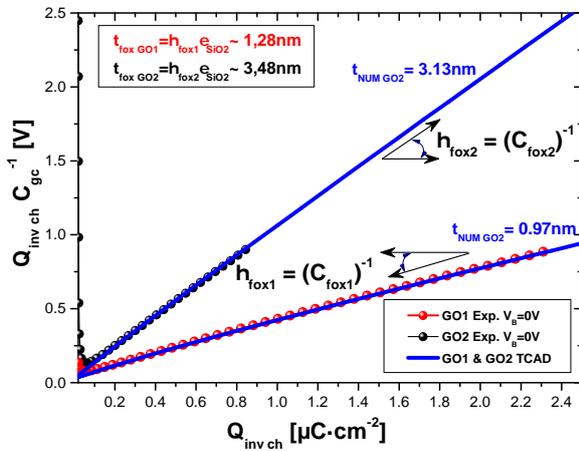


Figure 4.8: Linear plot of  $Q_{ch\,inv}/C_{gc}(V_{GS})$  versus  $Q_{ch\,inv}(V_{GS})$ . Comparison between NUMERICAD fit and experimental methodology for the standard P-MOS GO1 and GO2 devices.

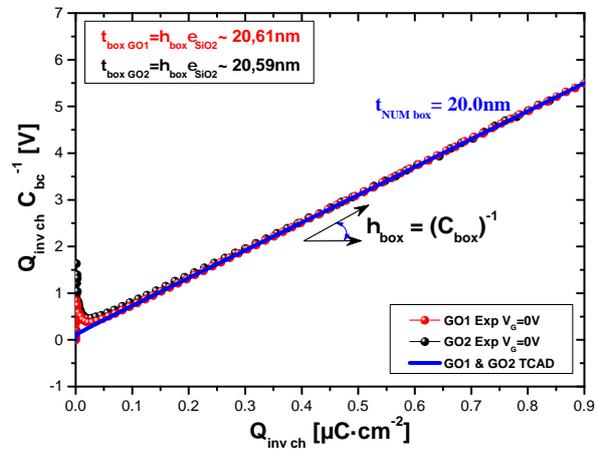


Figure 4.9: Linear plot of  $Q_{ch\,inv}/C_{bc}(V_{BS})$  versus  $Q_{ch\,inv}(V_{BS})$ . Comparison between NUMERICAD fit and experimental methodology for the standard P-MOS GO1 and GO2 devices.

Fig. 4.8 reports the comparison between the experimental methodology (circles) and NUMERICAD simulations (blue line) for  $t_{fox}$  extraction. For the same

characteristic, a small difference between the obtained values of  $t_{fox}$  is reported. Indeed a value of 0.97nm and 3.13nm for GO1 and GO2 devices is obtained by fitting the experiments to Quantum simulations whereas a value of 1.28nm and 3.48nm was been obtained by simply calculating the slopes of linear  $Q_{ch\ inv}/C_{gc}(V_{GS})$  versus  $Q_{ch\ inv}(V_{GS})$  characteristics. This error of 0.3nm is due to

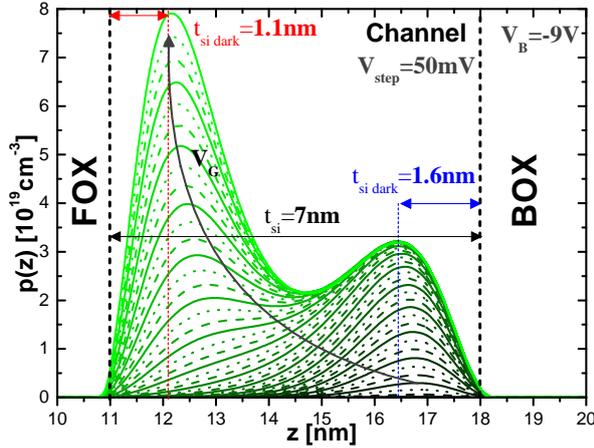


Figure 4.10: Hole carrier density versus channel position from NUMERICAD at different  $V_G$  and  $V_B=-9V$  for the standard P-MOS GO1 device. Evidence of the difference between the physical and electrical channel thickness.

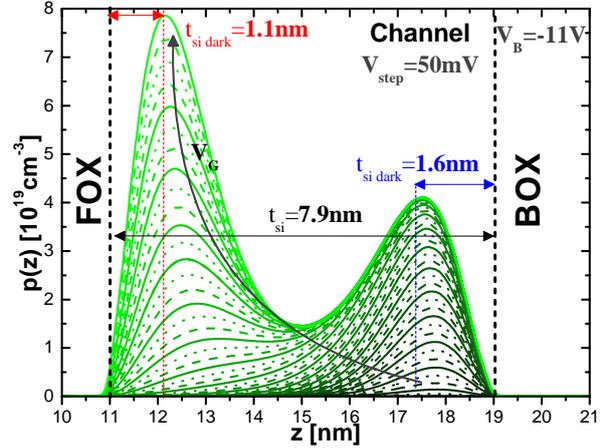


Figure 4.11: Hole carrier density versus channel position from NUMERICAD at different  $V_G$  and  $V_B=-11V$  for the standard P-MOS GO2 device. Evidence of the difference between the physical and electrical channel thickness.

the formalism applied within the experimental methodology as previously said (Boltzmann versus Schrodinger) which doesn't take into account the dark space (around 0.3nm in terms of equivalent SiO2 oxide thickness). Figs. 4.10 and 4.11 are numerical simulations of the channel charge within quantum formalism. They report the channel carrier density profiles (GO1 and GO2) obtained by NUMERICAD for various biases  $V_G$  at the minimum  $V_B$ . As we can observe, the barycenter of the charge, in strong front inversion, is located at 1.1nm from the interface oxide-channel (red arrows) that exactly corresponds to 0.3nm of dark space in terms of SiO2 equivalent thickness. Therefore, in order to get a precise thickness value, a correction has to be made on the previous extracted front-oxide thickness  $t_{fox}$  obtained within Boltzmann formalism which suppose that the charge barycenter is exactly located at the interface oxide-channel. The corrected front-oxide thickness is

$$t_{foxq} = t_{fox} + t_{dark} \tag{4.12}$$

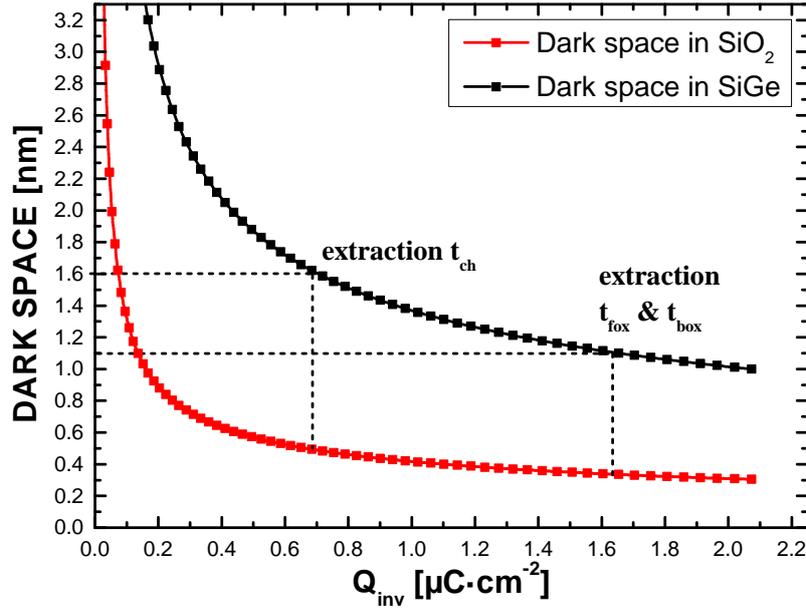


Figure 4.12: Numerical simulation (UTOXPP) of the dark space as a function of the inversion channel charge, in terms of SiO<sub>2</sub> and SiGe dielectric constant.

For what concerns back-oxide extraction, an error of 0.6nm is evidenced between the extracted thicknesses (Fig. 4.9). Indeed a value of 20nm for GO1 and GO2 devices is obtained by fitting the experiments to Quantum simulations whereas a value of 20.61nm and 20.58nm was been obtained by simply calculating the slopes of linear  $Q_{ch\ inv}/C_{bc}(V_{BS})$  versus  $Q_{ch\ inv}(V_{BS})$  characteristics. This is always due to the presence of two semiconductors (channel and well) located at the top and bottom sides of the buried oxide. We remind that whereas the channel is at strong back inversion, the well is in strong accumulation (neglected in the equation 4.5). This electrostatic condition corresponds to the presence of two dark spaces: one associated to the channel and the other to the well (the associated capacitances are  $\epsilon_{Si}/t_{dark}$ ). Therefore, in order to get a precise thickness value, a correction has to be made as well on the extracted classical back-oxide thickness ( $t_{box}$ ), including the double presence of the dark space, that is

$$t_{boxq} = t_{box} + 2t_{dark} \quad (4.13)$$

The front-oxide and back-oxide thicknesses are calculated in terms of SiO<sub>2</sub> equivalent thickness (EOT). Taking into account the correction of the channel and well quantum dark space (0.3 nm), we obtain:  $EOT_{GO1}=t_{foxq}=0.98$  nm,  $EOT_{GO2}=t_{foxq}=3.18$ nm,  $EOT_{BOX\ GO1}=t_{boxq}= 19.98$  nm and  $EOT_{BOX\ GO2}=t_{boxq}= 20.01$  nm in very good agreement with NUMERICAD values (Figs. 4.8 and 4.9).

The channel thickness extraction requires a larger dark space correction with respect to the front-oxide and back-oxide thicknesses extractions (Eqs. 4.12 and 4.13). We remind that Figs. 4.10 and 4.11, are numerical simulation results of the inversion channel charge versus the channel position ( $z$ ). The extraction of  $t_{ch}$  occurs at the onset of inversion at back interface between the channel and the buried oxide interface (overlapped region between the blue asymptote and experimental data in Figs.4.4 and 4.6). At this electrostatic condition (lower charge inversion level) an observed 1.6 nm thickness for the dark space at Si back interface is observed (blue arrow). It accounts for the difference between simulated and extracted SiGe channel thickness. Therefore the corrected channel thickness is

$$t_{chq} = t_{ch} + \frac{\epsilon_{ch}}{\epsilon_{SiO_2}} t_{dark} \quad (4.14)$$

We remind that in order to extract the channel thickness, a corrected value of the front-oxide thickness is necessary. The different values of dark space used for the channel thickness extraction (1.6nm) and front and back oxide thickness extraction (1.1nm) are justified by the fact that these extractions are occurring at different inversion channel charge levels. Indeed  $t_{ch}$  extraction is carried out at lower channel charge level compared to  $t_{fox}$  and  $t_{box}$  extraction. Unfortunately as reported in Fig. 4.12, the dark space is dependent of the channel charge level. For simplicity, two fixed values (Fig. 4.12) of the dark spaces are taken into account during the extraction which are exactly the errors found between the previous extraction results based on Boltzmann Formalism and the fitting numerical simulation results. In this chapter, only results for PMOS devices have been shown but similar results have also been obtained for NMOS devices. The results of the P-MOS devices are identical to the ones obtained in the previous chapter through numerical simulations which validated the analytical extraction methodology.

## 4.4 Conclusion

We can conclude that for the first time an analytical extraction methodology based on linear regression which exploits the linearity of  $Q_{\text{ch inv}}/C_{\text{gc}}$  and  $Q_{\text{ch inv}}/C_{\text{bc}}$  versus  $Q_{\text{ch inv}}$  characteristics has been presented. Moreover, the impacts of the modulation  $V_B$  and  $V_G$  on these characteristics have been investigated.

The analytical methodology leads us to directly and analytically extract all the FDSOI stack thicknesses ( $t_{\text{fox}}$ ,  $t_{\text{ch}}$  and  $t_{\text{box}}$ ). This is carried out by simply calculating the slopes of the linear region of  $Q_{\text{ch inv}}/C_{\text{gc}}$  and  $Q_{\text{ch inv}}/C_{\text{bc}}$  versus  $Q_{\text{ch inv}}$  characteristics.

The analytical methodology has been validated through comparison with the numerical simulations results obtained in the previous chapter.

The extraction methodology is faster and less complicated procedure compared to the previous numerical methodology which is expensive in terms of computational and time cost.

Despite the simplicity of this methodology compared to the numerical methodology,  $WF_{\text{eff}}$  and the well doping concentration cannot be extracted. Only a fitting between the experimental C-V and the numerical simulation which uses the FDSOI stack thicknesses extracted with the analytical methodology as inputs, allows us to properly identify  $WF_{\text{eff}}$  (previous chapter last step of the numerical methodology).

Moreover the analytical methodology needs to take into account a dark space correction due to the discrepancy between the Boltzmann formalism (used in the methodology) and the PS formalism (used in the numerical simulation). The values of these dark spaces are considered constant even if dependent of the channel charge level. This approximation can lead to imprecision of the extracted front, back oxide and channel thicknesses.

Therefore this fast and simple extraction technique is not sufficient and rigorous to evaluate the impact of the technology over all the electrical performance of the FDSOI transistors. This leads us to look for new analytical methodologies for a complete characterization of the FDSOI devices.

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# Chapter 5

## Analytical characterization of FDSOI stack based on universal curve $Q_{\text{tot}}(E_c - E_f)$

### 5.1 Introduction

In the previous chapters, we proposed two different extraction methodologies in order to extract the relevant parameters of the FDSOI transistors. The first, the numerical methodology, is based on fitting the experimental C-V capacitances with the PS numerical simulation [1, 2]. We remind that this methodology is not simply a fitting operation but an accurate procedure carried out by following a specific extraction strategy (see chapter 3 for details). The second methodology is the analytical extraction presented in Chapter 4. This methodology contrary to the numerical procedure, is based on simple linear regression and doesn't need any numerical simulation in order to extract the various FDSOI stack thicknesses (see chapter 4 for details).

We have seen that both methodologies have advantages and disadvantages in terms of computational cost and extraction rapidity. We briefly remind the most important ones:

- The numerical methodology allows us to extract all the the FDSOI stack thicknesses ( $t_{\text{fox}}$ ,  $t_{\text{ch}}$  and  $t_{\text{box}}$ ) and the effective work function  $WF_{\text{eff}}$ . Unfortunately, in terms of computation cost and extraction time is really expensive (days).
- The analytical methodology allows us to extract only the FDSOI stack thicknesses ( $t_{\text{fox}}$ ,  $t_{\text{ch}}$  and  $t_{\text{box}}$ ) but not the effective work function. It's a fast

and simple procedure that allows us to extract the different FDSOI stack thicknesses in few seconds.

Therefore, It's clear that the two methodologies are not adequate for a fast and complete characterization of the FDSOI transistors because either the extraction methodology is too slow and complicate (numerical) or is not complete (analytical).

The aim of this chapter is to present an innovative methodology which is fast, complete and accurate for the technological optimization of FDSOI transistors. The chapter is divided in 3 main parts.

The first part is focused on the calculation of the different charges of FDSOI stack (metal, channel and substrate). In order to calculate these charges, two other C-V measurement set-up are introduced and presented with respect to previous  $C_{gc}$  and  $C_{bc}$  inversion capacitances.

The second part is related to the presentation of the principles of the extraction methodology. The electrostatic information obtained in the first part and the innovative capacitance measurement methodologies will be used to carry out the extraction of the thickness of the different layers (gate oxide, substrate channel, buried oxide) in an innovative way compared to the previous works in the state of the art [3, 4, 5, 6] and as well as the effective work function  $WF_{eff}$  and the Well doping level for Si and SiGe FDSOI devices.

Finally, the third part is the conclusion of the chapter where an evaluation of the methodology and a comparison with the previous analytical and numerical methodologies are carried out.

## 5.2 Calculation of the FDSOI stack charges

### 5.2.1 Introduction to the different capacitances measurement set-up on FDSOI transistors

In order to calculate the well, channel and metal charges, we will introduce in this paragraph the different Capacitance-Voltage characteristics which can be measured on a FDSOI transistor. This will be carried out on a P-MOS FDSOI transistor featuring a GO2 dielectric, a Si channel, a P-type metal Gate and N-type Well as reported in the scheme of Fig. 5.1. We remind that this device is build with the same technology process introduced in chapter 3. As previously presented in chapter 2, we have analytically defined 4 different capacitances for a FDSOI transistor. Up to now, we have experimentally introduced only two different capacitances among the 4. These are the Gate-to-channel  $C_{gc}$  and Body-to-channel  $C_{bc}$  capacitances which are used in order to carry out the previous numerical (chapter 3) and analytical (Chapter 4) extractions. In this paragraph, we will present two other capacitances which are the Gate-to-Body  $C_{gb}$  and Body-to-Gate  $C_{bg}$  Capacitance. These are fundamental in order to calculate the different charges in the FDSOI stack as will be seen in the next sections.

Starting from  $C_{gb}$  measurement, the first experimental result was reported in the work of Shin et all [7]. In Fig. 5.1 we show the classical experimental configuration for the measurement of Gate-to-channel ( $C_{gc}$ ) and Gate-to-bulk ( $C_{gb}$ ) capacitances at  $V_B=0V$ . In order to carry out  $C_{gb}$  measurement (right side of Fig. 5.1), the small AC signal is applied on the Gate ( $V_G=V_{G\ static}+v_g(t)$ ) and the induced capacitive current is measured on Body terminal or Well ( $I(t)=dQ_{Well}(t)/dt$ ) which leads to obtain, with the Capacitance meter,

$$C = I(t) \frac{\partial t}{\partial v(t)} = \frac{-\partial Q_{Well}(V_G, V_B)}{\partial t} \frac{\partial t}{\partial V_G(t)} = -\frac{\partial Q_{Well}(V_G, V_B)}{\partial V_G(t)} \quad (5.1)$$

that is exactly identical to the relation 2.31 defined in chapter 2. The experimental results,  $C_{gc}$  in black line and  $C_{gb}$  in red line, are reported in Fig. 5.2.

For what concerns the last capacitance, the Body-to-Gate  $C_{bg}$ , in Fig. 5.3 we report its experimental configuration and the experimental configuration of the Body-to-channel capacitance measurement ( $C_{bc}$ ), already presented in Chapter 3, respectively at  $V_G=0V$ .

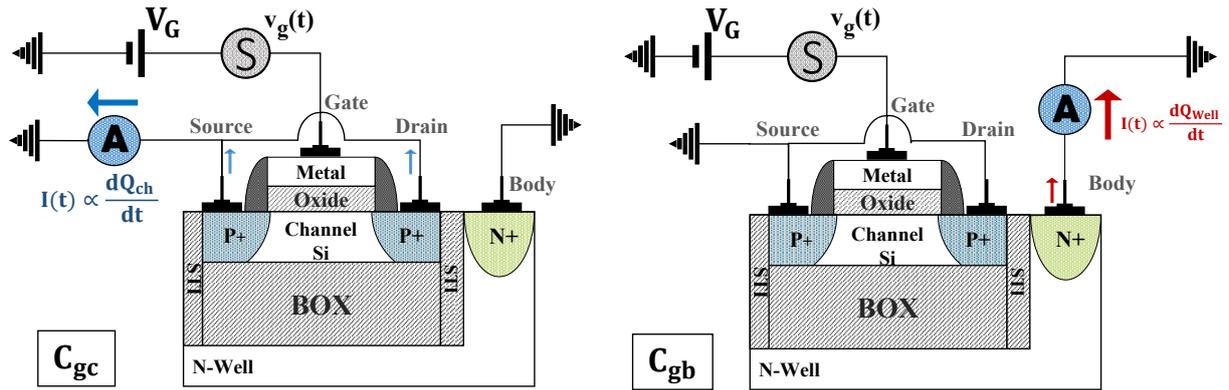


Figure 5.1: Scheme of the standard experimental configurations for Gate-to-channel ( $C_{gc}$ ) and Gate-to-Body ( $C_{gb}$ ) capacitances measurements in case of a FDSOI device.

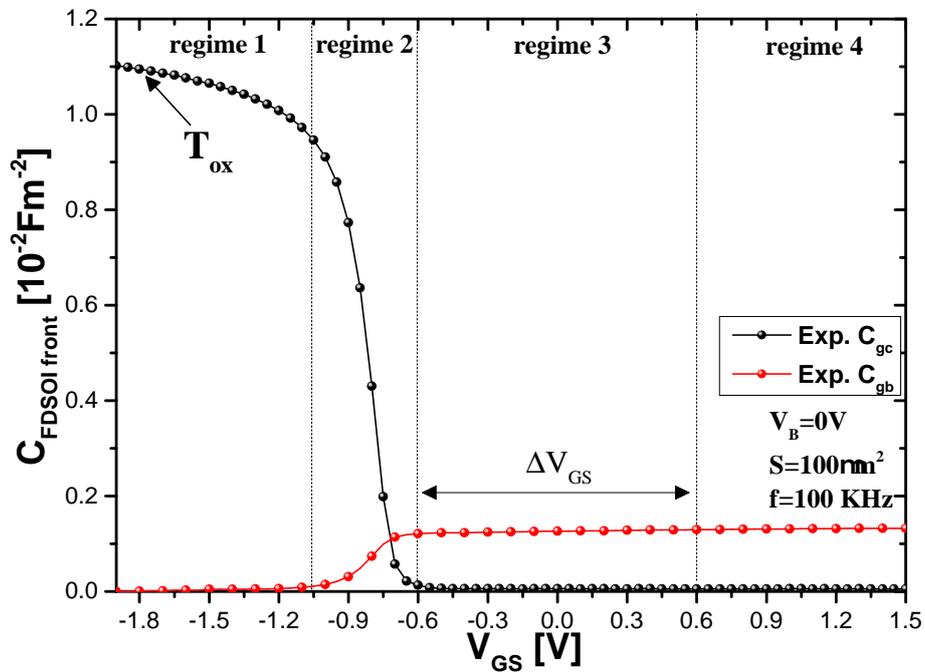


Figure 5.2: Gate-to-channel ( $C_{gc}$ ) and Gate-to-Body ( $C_{gb}$ ) capacitance characteristics versus Gate-to-Source voltage ( $V_{GS}$ ) for a P-MOS GO2 Si-channel device.

Whereas  $C_{gc}$  and  $C_{gb}$  are well known in the state of the art [7],  $C_{bg}$  is presented for the first time such as  $C_{bc}$  which is reported in the previous chapter 3 (see also the work of B.Mohamad et al. [8]). In order to carry out  $C_{bg}$  measurement (right side of Fig.5.3), the small AC signal is applied on the Body ( $V_B = V_{B\text{static}} + v_b(t)$ ) and the induced capacitive current is measured on Gate terminal ( $I(t) = dQ_m(t)/dt$ ) which

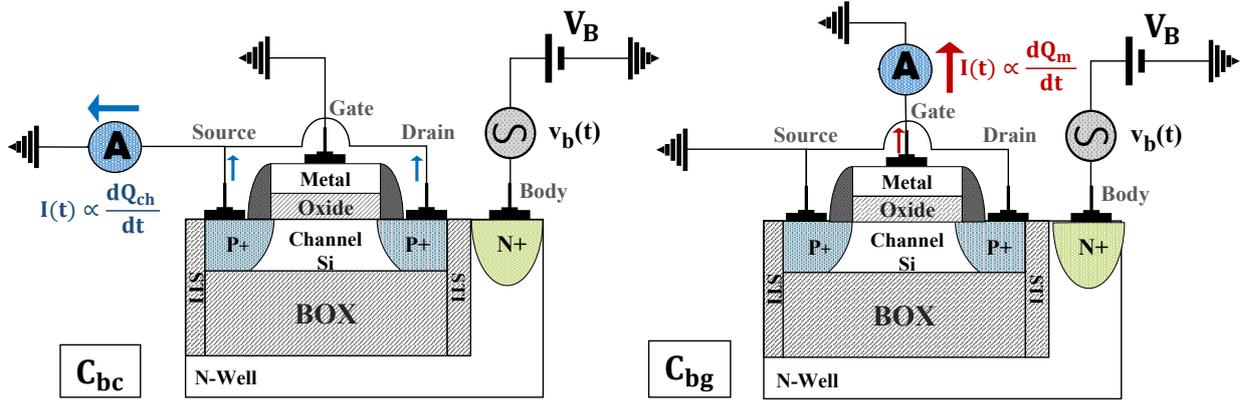


Figure 5.3: Scheme of the experimental configurations for Body-to-channel ( $C_{bc}$ ) and Body-to-Gate ( $C_{bg}$ ) capacitance measurements in case of a FDSOI device.

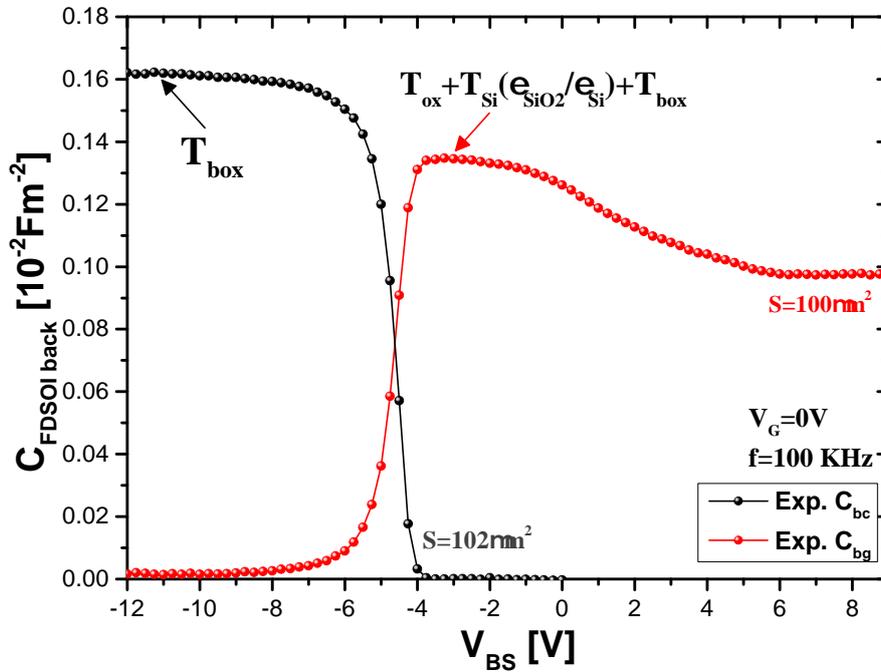


Figure 5.4: Body-to-channel ( $C_{bc}$ ) and Body-to-Gate ( $C_{bg}$ ) capacitance characteristics versus Body-to-Source voltage ( $V_{BS}$ ) for a P-MOS GO2 Si-channel device.

leads to obtain, with the Capacitance meter,

$$C = I(t) \frac{\partial t}{\partial v(t)} = \frac{-\partial Q_m(V_G, V_B)}{\partial t} \frac{\partial t}{\partial V_B(t)} = -\frac{\partial Q_m(V_G, V_B)}{\partial V_B(t)} \quad (5.2)$$

where  $Q_m$  is the metal charge. This relation is identical to equation 2.39 defined in chapter 2. We report the experimental results,  $C_{bc}$  in black line and  $C_{bg}$  in red line, in Fig. 5.4. All these 4 capacitance measurements lead to a complete back and

front split C-V measurements of the FDSOI transistor. Each measurement gives a different electrostatic information of FDSOI stack condition. We remind that in case of traditional bulk transistors, as presented in Chapter 1, an identification of the flat band condition with the classical state of the art methods [9] is necessary to calculate the total charge in the substrate. The identification of the flat band condition in a standard bulk transistor C-V characteristic is possible since all this capacitance is the result of the entire evolution of the substrate charge (Inversion, depletion and accumulation) [10]. It's obvious that an operation regime analysis of the FDSOI transistor during C-V measurement is necessary to understand how these capacitance characteristics are related to the evolution of the channel, metal and well charges of the FDSOI stack. Therefore, the aim of the next section will be to carry out an operation regime analysis of the FDSOI stack to find a possible flat band condition such as in the traditional bulk transistors and consequently access to the metal, channel and well charges which means the whole electrostatic condition of the FDSOI stack.

### 5.2.2 FDSOI transistor Operation regime during C-V measurement

We remind that in chapter 2 we have previously obtained the analytical expression of all the 4 Capacitances relations that are measurable on FDSOI transistors (the "front"  $C_{gc}$  and  $C_{gb}$  capacitances and the "back"  $C_{bc}$  and  $C_{bg}$  capacitances). These analytical expressions have been related to two important parameters that are  $\alpha = \partial Q_w / \partial Q_{ch}$  and  $\beta = \partial Q_m / \partial Q_{ch}$  which are strongly dependent of the operation regime condition of the FDSOI stack. Therefore, it is interesting to carry out an operation regime analysis starting from these capacitance expression and to see if there's a condition for which these capacitances relations are simplified and turned into the same capacitance relation of the traditional bulk where the calculation of the charge from the flat band condition is easily carried out.

Starting from  $C_{bg}$  and  $C_{bc}$  capacitances we report here the expressions obtained in chapter 2 that are respectively

$$\frac{1}{C_{bc}} = \frac{1}{C_{ch}} + \frac{1}{C_{box}} + \beta \left( \frac{1}{C_{fox}} + \frac{1}{C_{box}} \right) + \frac{-\alpha}{C_{Well}} \quad (5.3)$$

$$\frac{1}{C_{bg}} = \frac{1}{C_{bc}\beta} = \beta^{-1} \left( \frac{1}{C_{ch}} + \frac{1}{C_{box}} \right) + \frac{1}{C_{fox}} + \frac{1}{C_{box}} + \frac{-\alpha\beta^{-1}}{C_{Well}}. \quad (5.4)$$

As reported in Fig. 5.5, four main regions (or regimes) are evidenced that are:

- **regime1:** This first region ( $V_{BS} < -8V$  in Fig. 5.5) is characterized by the presence of the  $C_{bc}$  signal whereas  $C_{bg}$  is zero. We remember that  $C_{bc}$  and  $C_{bg}$  signal are related respectively to the variation of the channel and metal charge with respect to the Body potential ( $V_B$ ) variation as reported in Fig. 5.6 a. Therefore this regime, called "**strong back inversion**", is dominated only by the variation of the channel charge  $Q_{ch}$  whereas  $Q_m$  is fixed since the response of the channel carriers, that is related to the  $C_{bc}$  capacitance characteristic, screens the electrostatic fluctuations influence, applied on the Body, on the metal charge. Indeed the  $C_{bg}$  capacitance signal is absent. The variations of the channel charge are directly coupled with the variations of the well charge as reported in the scheme of Fig. 5.6 a. From this analysis we obtain that  $\beta = 0$  and consequently  $\alpha = -1$  which leads to

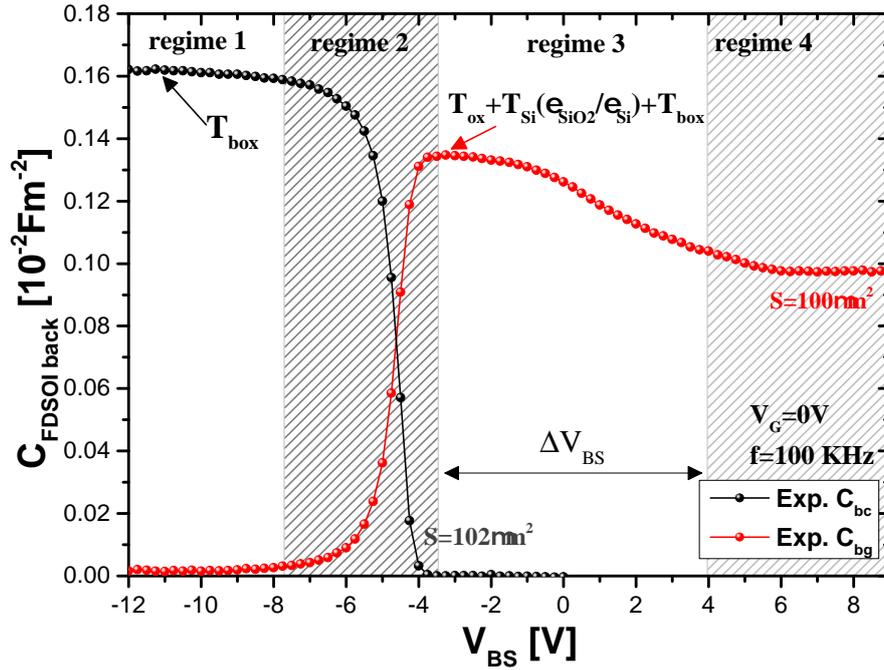


Figure 5.5: Different operation regimes on Body-to-channel ( $C_{bc}$ ) and Body-to-Gate ( $C_{bg}$ ) capacitances characteristics versus Body-to-Source voltage ( $V_{BS}$ ) for a P-MOS GO2 Si-channel device.

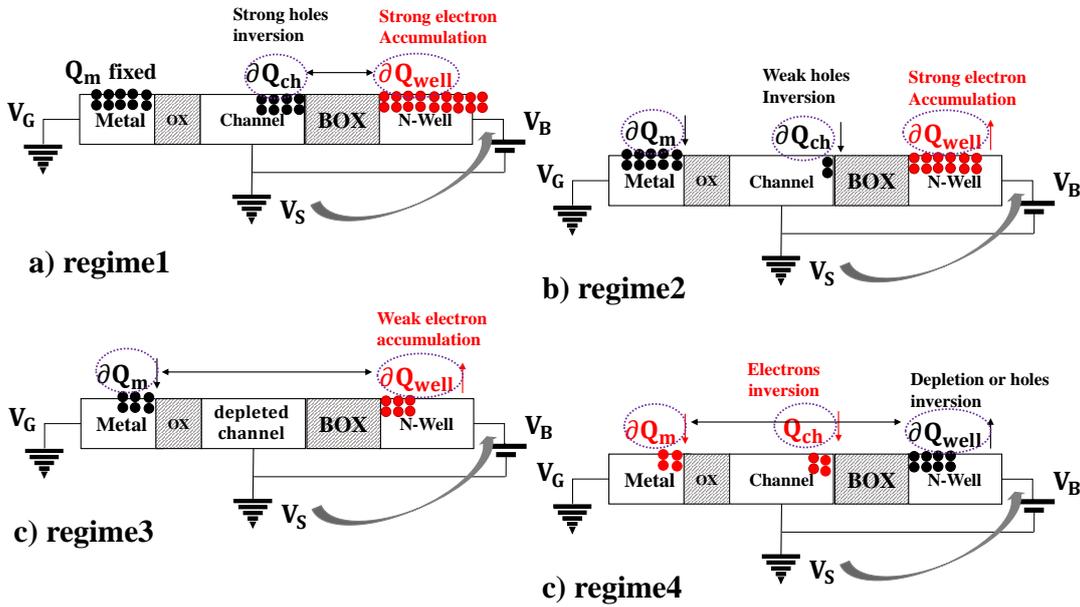


Figure 5.6: FDSOI Electrostatic condition at different operation regimes. The red spheres represent the negative charge whereas the black spheres the positive charges in the different layers of the FDSOI stack.

obtain from equation 5.3,

$$\frac{1}{C_{bc}} = \frac{1}{C_{ch}} + \frac{1}{C_{box}} + \frac{1}{C_{well}} \tag{5.5}$$

$$C_{bg} = 0 \quad (5.6)$$

- **regime2:** The second region ( $-8V < V_{BS} < -3.5V$  in Fig. 5.5) is characterized by the simultaneous presence of both the characteristics  $C_{bc}$  and  $C_{bg}$ . During this regime the  $C_{bc}$  capacitance decreases with his associate channel charge whereas  $C_{bg}$  starts to rise up strongly. Indeed the screening effect, dominating the first regime, decreases its effect on the metal charge since the channel is not anymore at strong back inversion. Therefore we have a simultaneous variation of  $Q_{ch}$  and  $Q_m$  with respect to the fluctuations induced by the Body potential (induced by the  $Q_{well}$  variations) as reported in Fig. 5.6 b. Therefore, all the charges are varying as function of  $V_B$  voltage, as reported in the scheme of Fig. 5.6 b. Equations 5.3 and 5.4 represent the relations of the  $C_{bc}$  and  $C_{bg}$  characteristics during this regime.
- **regime3:** The 3<sup>rd</sup> regime ( $-3.5V < V_{BS} < -4V$  in Fig. 5.5) is characterized by the only presence of  $C_{bg}$  signal since  $C_{bc}$  signal is absent. Indeed once the  $C_{bc}$  capacitance disappear, for large positive  $V_B$  voltage, the channel is not anymore in inversion condition which means no free carriers and a fully depleted channel as reported in Fig. 5.6 c. We know that the channel charge is the contribution of two main charges: the free inversion carrier and the fixed charge related to residual channel doping level ( $Q_{ch} = Q_{ch\ inv} + Q_{ch\ fix}$  where  $Q_{ch\ fix} = q t_{ch} N_{ch}$ ). Since  $Q_{ch\ inv} = 0$  and  $Q_{ch\ fix} = 0$ , due to low doping level in the channel, we know that the effective charge in the channel can be considered zero. Even if  $Q_{ch\ fix} \neq 0$ , the fixed charge  $Q_{ch\ fix}$  will simply shift the flat band condition and the total charge as a function of  $V_{GS}$  characteristic and no other impact on this characteristic trend will be observed. Therefore, when the channel is in fully depleted condition, the metal charge is directly coupled with well charge as reported in the scheme of Fig. 5.6 c. In this electrostatic condition, we have that

$$\alpha\beta^{-1} = \frac{\partial Q_w}{\partial Q_{ch}} \cdot \frac{\partial Q_{ch}}{\partial Q_m} = \frac{\partial Q_w}{\partial Q_m} = -1. \quad (5.7)$$

Relation 5.4 becomes

$$\frac{1}{C_{bg}} = \frac{1}{C_{fox}} + \frac{1}{C_{box}} + \frac{1}{C_{Well}} + \frac{\beta^{-1}}{C_{ch}} + \frac{\beta^{-1}}{C_{box}} \quad (5.8)$$

Whereas the last term of equation 5.8 can be neglected since  $\beta^{-1} = 0$ , the second last term  $\beta^{-1}/C_{ch} = 0/0$  is an indeterminate form that has to be solved.

Indeed we know that

$$\beta^{-1} \frac{1}{C_{ch}} = \frac{\partial Q_{ch}}{\partial Q_m} \cdot \frac{\partial \Psi_{ch}}{\partial Q_{ch}} = \frac{\partial \Psi_{ch}}{\partial Q_m} \quad (5.9)$$

Since the channel is fully depleted the potential induced by metal (or well) charge is simply

$$\Psi_{ch} = \frac{Q_m}{\epsilon_{ch}} \cdot t_{ch} = \frac{Q_m}{C_{Si}} = -\frac{Q_{Well}}{C_{Si}} \quad (5.10)$$

where  $C_{Si} = \epsilon_{ch}/t_{ch}$  is the channel capacitance. Therefore, the second last term of eq.5.8) becomes

$$\beta^{-1} \frac{1}{C_{ch}} = \frac{\partial \Psi_{ch}}{\partial Q_m} = \frac{1}{C_{Si}} \quad (5.11)$$

Finally from equations 5.8 and 5.10 we can obtain the simplified expression of  $C_{bg}$  during the third regime, that is

$$\frac{1}{C_{bg}} = \frac{1}{C_{fox}} + \frac{1}{C_{box}} + \frac{1}{C_{Si}} + \frac{1}{C_{Well}} \quad (5.12)$$

This last expression can be reformulated as

$$\frac{1}{C_{bg}} = \frac{t_{fox} + t_{box} + t_{ch}(\epsilon_{SiO2}/\epsilon_{ch})}{\epsilon_{SiO2}} + \frac{1}{C_{Well}} = \frac{EOT_{stack}}{\epsilon_{SiO2}} + \frac{1}{C_{Well}} \quad (5.13)$$

This is the typical capacitance of a bulk transistor featuring an  $EOT_{stack} = t_{fox} + t_{box} + t_{ch}(\epsilon_{SiO2}/\epsilon_{ch})$  which is the result of direct coupling between metal and well charges. This regime is defined in our work as the **FDSOI bulk regime** and represents the evolution, from depletion to accumulation, of the metal (or well) charge. The channel behaves as a dielectric since it has no free carriers.

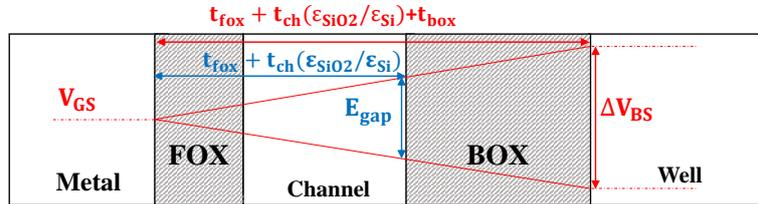


Figure 5.7: Scheme of FDSOI stack and application of Thales's theorem.

The value of the voltage range for which we have the FDSOI bulk regime is given in first approximation by

$$\Delta V_{BS} = E_g \frac{(t_{box} + t_{ch}(\epsilon_{SiO2}/\epsilon_{ch}) + t_{fox})}{(t_{ch}(\epsilon_{SiO2}/\epsilon_{ch}) + t_{fox})} \quad (5.14)$$

This expression is obtained with the Thales's theorem as reported in Fig. 5.7. Indeed for Thales's theorem we know that  $\Delta V_{BS}/E_{gap} = (t_{fox} + t_{ch} + t_{box}) / (E_{gap} + E_{gap}(\epsilon_{SiO2})/\epsilon_{ch})$  which leads to equation 5.14. This 3<sup>rd</sup> regime is the most important region and will be the key for the identification of the flat band condition and the calculation of the well charge as we will see in the next section.

- **regime4:** The last regime ( $V_{BS} > -4V$  in Fig.5.5) is defined by the onset of electrons channel inversion phenomena as reported in Fig. 5.6 d. The electrons inversion carrier are created through thermal generation at specific rate which is  $f_{gr}$ . During C-V measurement two signal are applied at the Body contact: a constant voltage  $V_B$  ( $f_B=0$ ) and a small signal voltage  $v_b(t)$  at specific rate  $f_b$ . The electrons inversion phenomena will always responds to the constant voltage since  $f_{gr} > f_B=0$  but it is not capable to respond to the variations of the small signal since  $f_b > f_{gr}$ . The channel charge will depends on the applied Body voltage  $V_B$ . Deformation of the bulk capacitance is expected and is dependent of the amount of channel charge created by the thermal generation phenomena. This regime is defined as **distorted FDSOI bulk regime**.

Among these 4 different regimes, we remind that the most important one is the FDSOI bulk regime (or 3<sup>rd</sup> regime) from which the identification of well flat band can be carried out.

Similar analysis can be carried out on the "front" FDSOI capacitances,  $C_{gc}$  and  $C_{gb}$ . Here we remind the expressions obtained in chapter 2 for these capacitances that are respectively:

$$\frac{1}{C_{gc}} = \frac{1}{C_{fox}} + \frac{1}{C_{ch}} + \alpha \left( \frac{1}{C_{fox}} + \frac{1}{C_{box}} + \frac{1}{C_{Well}} \right) \quad (5.15)$$

$$\frac{1}{C_{gb}} = \frac{1}{C_{cg} \cdot \alpha} = \frac{1}{C_{fox}} + \frac{1}{C_{box}} + \frac{1}{C_{Well}} + \alpha^{-1} \left( \frac{1}{C_{fox}} + \frac{1}{C_{ch}} \right) \quad (5.16)$$

We have reported in Fig. 5.2  $C_{gc}$  and  $C_{gb}$  capacitances and the 4 main operation regimes which are similar to the ones defined for the "back" capacitances:

- **regime1:** The first region ( $V_{GS} < -1.1V$  in Fig. 5.2) is characterized by  $C_{gb}=0$  and large  $C_{gc}$  signal. This is dominated by the channel charge, and is defined as **strong front inversion regime**. The well charge is constant and doesn't vary due to the screening effect of the channel charge on the potential variations induced by  $V_G$  voltage. Since  $\alpha = 0$ , from equation 5.15 we obtain that  $C_{gc}$  capacitance is

$$\frac{1}{C_{gc}} = \frac{1}{C_{fox}} + \frac{1}{C_{ch}} \quad (5.17)$$

- **regime2:** The second region ( $-1.1V < V_{GS} < -0.6V$  in Fig. 5.2) is characterized by the simultaneous presence of both  $C_{gc}$  and  $C_{gb}$  capacitances. This means, such as for  $C_{bc}$  and  $C_{bg}$  characteristic in the second regime, a variations of all the FDSOI charges ( $Q_{Well}$ ,  $Q_m$ ,  $Q_{ch}$ ). Therefore relations 5.15 and 5.16 define the  $C_{gc}$  and  $C_{gb}$  characteristics in this region.
- **regime3:** During 3<sup>rd</sup> regime ( $-0.6V < V_{GS} > 0.6V$  as reported in Fig. 5.2), we have only the presence of  $C_{gb}$  signal while  $C_{gc}$  is zero. As for  $C_{bc}$  and  $C_{bg}$  characteristic in the third regime, the channel is depleted ( $C_{bc}=0$ ) and the  $C_{gb}$  characteristic is the result of the direct coupling between metal and well charge. From equation 2.37, in this regime, since  $\alpha^{-1} \frac{1}{C_{ch}} = \frac{1}{C_{Si}}$  and  $\alpha^{-1} \frac{1}{C_{fox}} = 0$  we easily obtain:

$$\frac{1}{C_{gb}} = \frac{1}{C_{fox}} + \frac{1}{C_{box}} + \frac{1}{C_{Si}} + \frac{1}{C_{Well}}. \quad (5.18)$$

This equation is identical to the relation 5.12 and consequently 5.13. This regime is still defined as **FDSOI bulk regime** and it is the key for the calculation of the FDSOI stack charges. This capacitance relationship is the result of the direct coupling between the metal and well charges with an equivalent dielectric given by  $EOT_{stack} = t_{fox} + t_{box} + t_{ch}(\epsilon_{SiO2}/\epsilon_{ch})$ . The first time that  $C_{gb}$  measurement was reported [7], Shin et al believed that  $C_{gb}$  remains constant in depletion and does not reach its accumulation value due to the absence of AC response of holes in case of N-MOS devices. But as we will analytically and experimentally demonstrate in next sections, this is not true. This capacitance is the result of the direct coupling between the well charge and the metal charge which features and EOT given by the series of the front-oxide, channel and back-oxide capacitance (equation 5.13). The channel behaves as a dielectric oxide. The value of the voltage range for which we have the FDSOI bulk regime is found with an analysis similar to

the one for  $C_{gb}$  and it is given as in first approximation by

$$\Delta V_{GS} = E_g \frac{(t_{box} + t_{ch}(\epsilon_{SiO2}/\epsilon_{ch}) + t_{fox})}{(t_{ch}(\epsilon_{SiO2}/\epsilon_{ch}) + t_{box})} \quad (5.19)$$

- **regime4:** The last regime ( $V_{GS} > 0.6V$  as reported in Fig. 5.2) is defined by the onset of electrons channel inversion phenomena. The electrons inversion carrier are created through thermal generation at specific rate which is  $f_{gr}$ . As for the "back" capacitance, this regime is defined as **distorted FDSOI bulk regime**.

We have seen that both for  $C_{gb}$  and  $C_{bg}$  the 3<sup>rd</sup> regime or FDSOI bulk regime is fundamental since the FDSOI device works as typical bulk capacitance. This region can be used in order to extract the flat band condition of the well substrate thus allowing the calculation of the well charge. Since during the FDSOI bulk regime the capacitance relations are the same for  $C_{gb}$  and  $C_{bg}$ , in the next sections we will prove experimentally that  $C_{gb}$  and  $C_{bg}$  measurements will give the same result. This will be carried out through modulation of these capacitances by the bulk or Gate contact.

### 5.2.3 Effect of back and front biasing on the Gate-to-Body capacitance measurement

Modulation effect on  $C_{gc}$  by back biasing characteristics is well known in the state of the art [7] whereas modulation effect on  $C_{bc}$  by front biasing was reported for the first time in chapter 3 [8]. Here, we report corresponding results for  $C_{gc}$  (Fig. 5.8) and for  $C_{bc}$  (Fig. 5.8) with respect to the reference characteristics at  $V_B=0V$  and  $V_G=0V$  of Figs. 5.2 and 5.4.

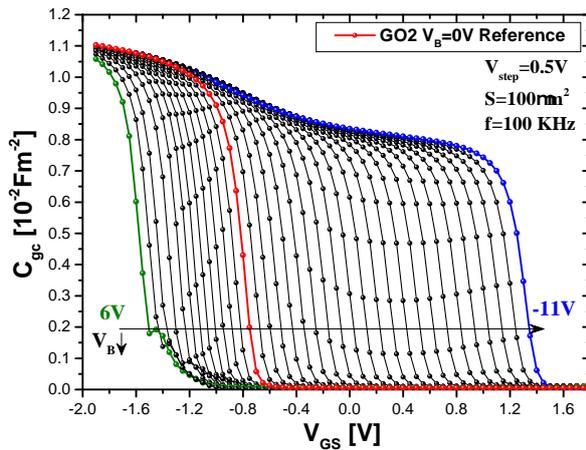


Figure 5.8: Gate-to-channel characteristics from large negative (-11V) to positive (6V) Body bias ( $V_B$ ) for a P-MOS GO2 Si channel device.

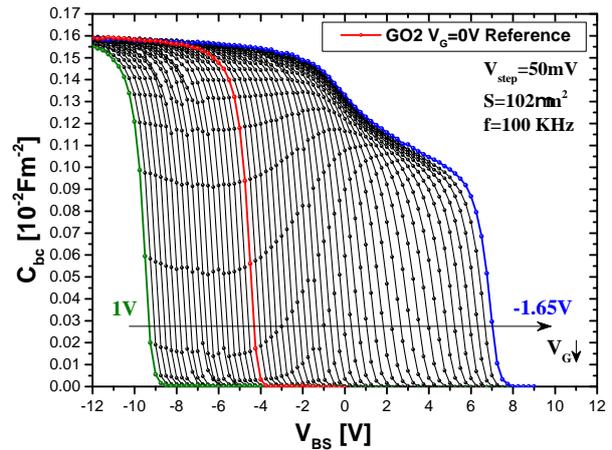


Figure 5.9: Body-to-channel characteristics from large negative (-1.65V) to positive (1V) Gate bias ( $V_G$ ) for a P-MOS GO2 Si channel device.

The effect of back-bias  $V_B$  on  $C_{gb}$  characteristics were firstly reported in the work of Shin [7] whereas the effect of front-bias  $V_G$  on  $C_{bg}$  characteristic are not known in the state of the art. In order to carry out  $C_{gb}$  measurement with back-biasing, a back bias voltage  $V_B$  has to be applied in series to the Ampere-meter (Low terminal connected to the Body) as reported in the first configuration in Fig. 5.10. But as explained in the work of Shin [7], it is not possible since the low terminal is forced at ground. Therefore, in order to carry out  $C_{gb}$  measurement, he proposed an alternative configuration (2nd configuration in Fig. 5.10). An reverse back bias  $V_B$  has to be simultaneously applied on Source-Drain and Gate terminals. Unfortunately, during  $C_{gb}$  measurement (2<sup>nd</sup> configuration of Fig. 5.10) at large back biasing, e.g.  $V_B=-11V$ , high potential drop between Gate and Source-Drain terminals can occur if the signal at the different contacts is not synchronized. Since the front-oxide features few nanometers of oxide thickness, a high voltage drop would lead to an oxide breakdown phenomena [11, 12]. In order to avoid

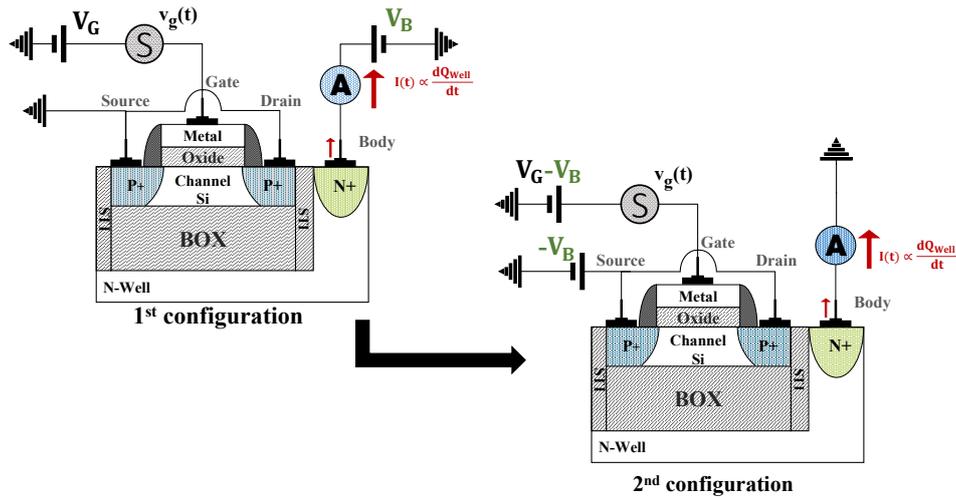


Figure 5.10: Alternative configuration for  $C_{gb}$  measurement with back biasing.

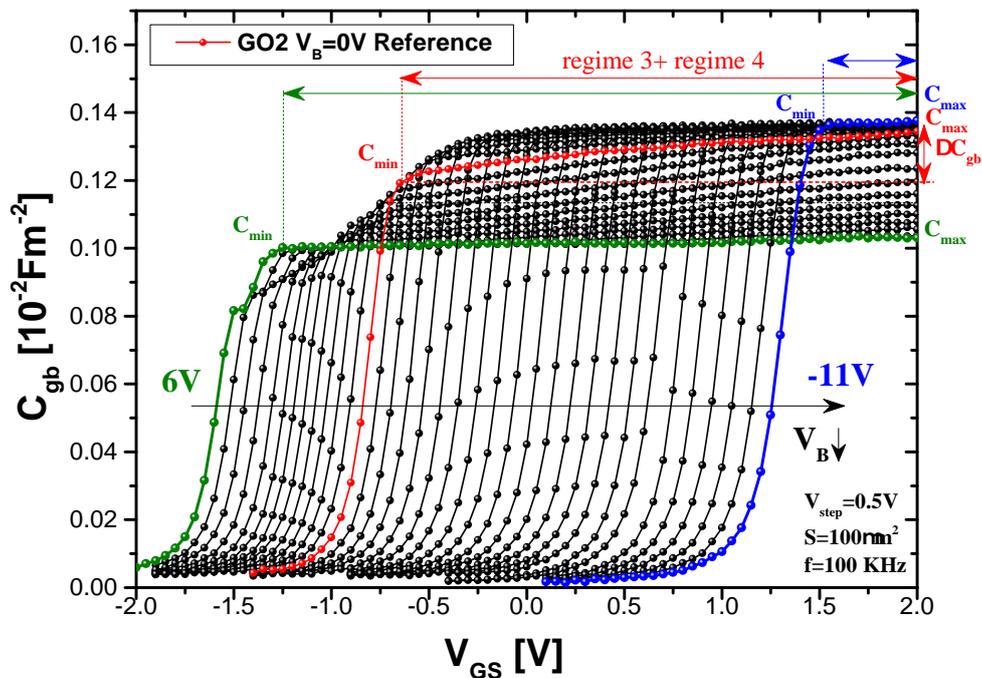


Figure 5.11:  $C_{gb}$  versus  $V_{GS}$  with back biasing  $V_B$  varying from 6V to -11V with a step of 0.5V for a P-MOS GO2 Si channel device.

this dielectric breakdown, we have proposed two significant adaptations of the experimental set-up:

- First, the voltage applied on the Gate terminal and Source-Drain ( $-V_B$ ) terminals (reported in the 2<sup>nd</sup> configuration of Fig. 5.12) are simultaneously increased to  $-V_B$  by progressive steps to avoid any significant bias drop on gate oxide. Then, the capacitance measurement is performed, meaning that

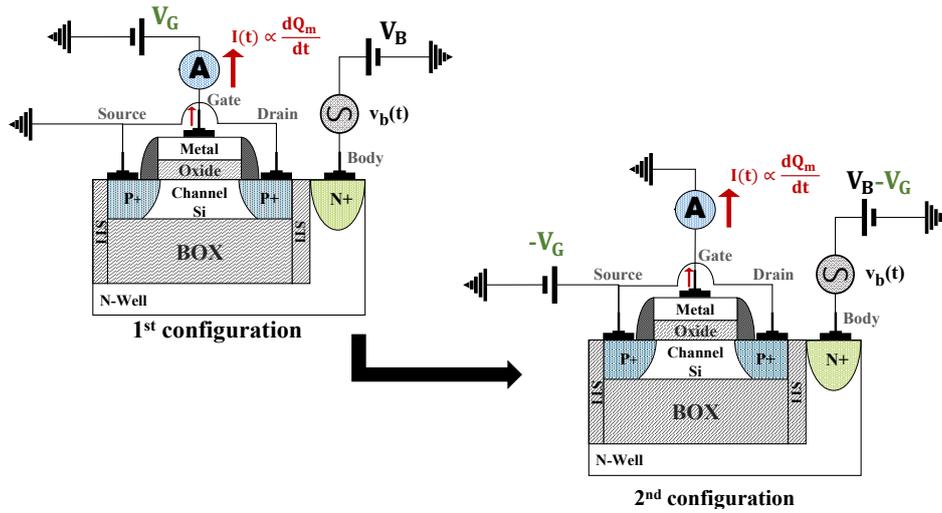


Figure 5.12: Alternative configuration for  $C_{bg}$  measurement with front biasing.

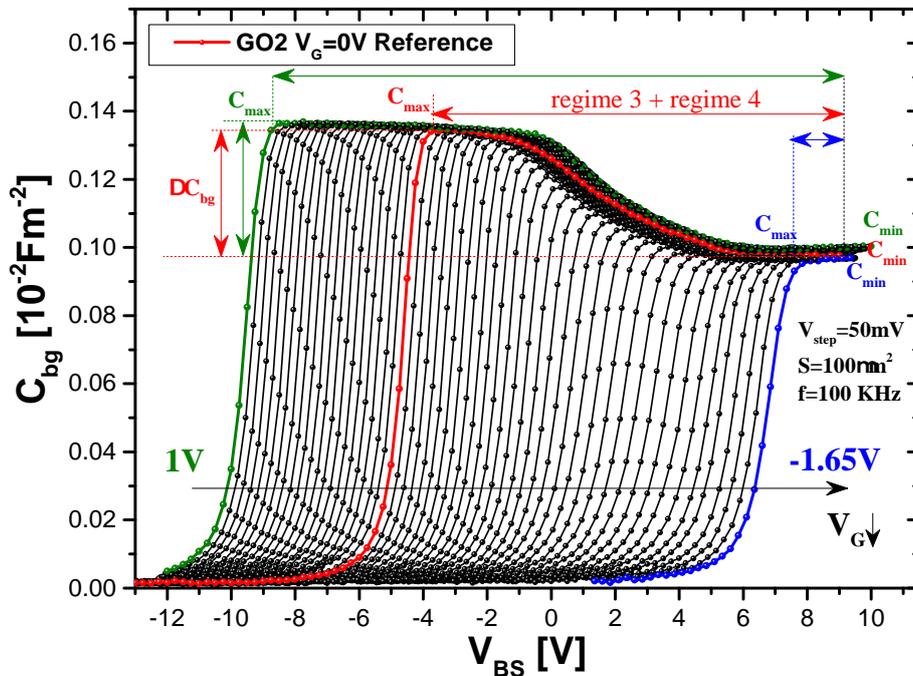


Figure 5.13:  $C_{bg}$  versus  $V_{BS}$  with front biasing  $V_G$  varying from 1V to -1.65V with a step of 50mV for a P-MOS GO2 Si channel device.

Gate bias evolves from  $-V_B+v_g(t)$  to  $V_G-V_B+v_g(t)$ .

- Second, the current limitation of the measurement unit at Source and Drain has been reduced to avoid any gate oxide breakdown but not too low to guarantee a reliable measurement of the induced current at the (Body) Low terminal (Fig. 5.12).

Once these actions are taken, a measurement of  $C_{gb}$  is possible. Results from

positive (6V in green) to large negative (-11V in blue) back bias  $V_B$  are reported in Fig. 5.11 with respect to the reference characteristic at  $V_B=0V$  (in red from Fig. 5.2). These characteristics are plotted in function of  $V_{GS}$ . Two important effects are observable due to the back bias voltage  $V_B$ . Firstly the range voltage  $\Delta V_{GS}$  for which we have the FDSOI bulk regime and the distorted FDSOI bulk regime (indicated by the horizontal double arrows) decreases from positive to large negative  $V_B$  voltage. Secondly, also the capacitance variation  $\Delta C_{gb}=C_{max}-C_{min}$  (indicated by the vertical double arrows) during this regime is dependent of the applied  $V_B$  voltage.

For what concerns  $C_{bg}$  measurement, the modulation is carried out through front-biasing  $V_G$ . Indeed, in order to perform this measurement, the front bias voltage  $V_G$  has to be applied in series to the Ampere-meter (Low terminal connected to the Gate) as reported in the first configuration in Fig. 5.12. Unfortunately, as seen for  $C_{gb}$  case, this is not possible since the low terminal is always forced at ground. Therefore, in order to carry out  $C_{bg}$  measurement, we have proposed for the first time an alternative configuration (2nd in Fig. 5.12). As clearly reported in this second configuration an inverse front bias  $V_G$  has to be simultaneously applied on Source-Drain and Body contacts. Contrary to the  $C_{gb}$  measurement, during  $C_{bg}$  measurement synchronization among Source-Drain and Body signal and limitation of the Body current are not necessary thanks to the thicker buried oxide with respect to the front-oxide which can not lead to any breakdown phenomena. Results from positive (1V in green) to large negative (-1.65V in blue) front bias  $V_G$  are reported in Fig. 5.13 with respect to the reference characteristic at  $V_G=0V$  (in red from Fig. 5.4). These characteristics are plotted in function of  $V_{BS}$ . Similar observation can be done for these capacitance measurements. Firstly, the range voltage  $\Delta V_{BS}$  for which we have the FDSOI bulk regime and the distorted FDSOI bulk regime (indicated by the horizontal double arrows) decreases from positive to large negative  $V_G$  voltage. Secondly, the capacitance variation  $\Delta C_{gb}=C_{max}-C_{min}$  (indicated by the vertical double arrows) during this regime also decrease from positive to large negative  $V_G$  voltage.

We have previously said that  $C_{gb}$  and  $C_{bg}$  during the FDSOI bulk regime (channel fully depleted with no minority carriers) should be the same capacitance since we analytically demonstrate that both are the result of the direct coupling between metal and well charge (eq. 5.12=eq. 5.18). Whereas  $C_{bg}$  shows a significantly variation as a function of  $V_{BS}$  voltage,  $C_{gb}$  shows a lower variation with  $V_{BS}$  voltage ( $\Delta C_{bg} \gg \Delta C_{gb}$ ) as reported in Figs. 5.11 and 5.13 for characteristics respectively at  $V_B=0V$  and  $V_G=0V$ . This is due to the large difference, in terms of

range, between  $V_{GS}$  and  $V_{BS}$  voltages during  $C_{gb}$  and  $C_{bg}$  measurements. But even if  $C_{bg}$  evidence at each  $V_G$  a larger well capacitance shift due to a larger range on  $V_{BS}$ , we must keep in mind that each characteristic only lead to a section of the Gate to well FDSOI capacitance. Indeed, we must keep the regime 3 with fully depleted channel to guarantee a reliable measurement. We remind our goal is to calculate the well charge and this can be carried out only through an identification of the well flat band condition. The flat band condition can be identified only if we can observe the entire evolution of the well charge and therefore the FDSOI bulk regime capacitance. Two questions are rising up. First how we can rebuild the entire FDSOI bulk regime capacitance starting from  $C_{gb}$  or  $C_{bg}$  characteristics? Second, how  $C_{bg}(V_{BS})$  and  $C_{gb}(V_{GS})$  can be the same when they appear significantly different in Figs. 5.11 and 5.13?

### 5.2.4 Reconstruction of $C_{gb}$ capacitance and comparison with $C_{bg}$ characteristic

We must notice that  $C_{gb}$  and  $C_{bg}$  are reported as a function of  $V_{GS}$  and  $V_{BS}$  in Figs. 5.11 and 5.13. It's well known in the state of the art and well described in chapter 1, that a standard MOS bulk capacitor is the result of the direct coupling between the metal and substrate charge. Its capacitance characteristic is usually reported as a function of the applied voltage between the metal and bulk contacts  $V_{GB}$ .

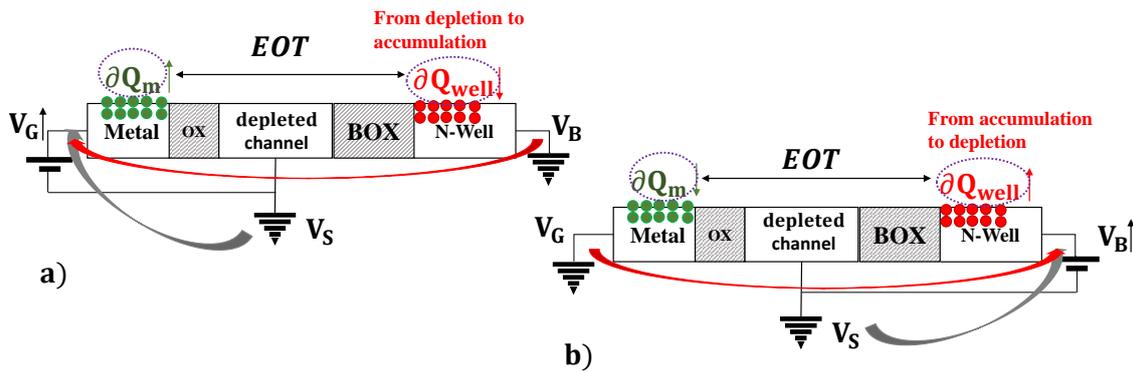


Figure 5.14:  $C_{gb}$  (a) and  $C_{bg}$  (b) measurement during FDSOI bulk regime.

We remind that during the FDSOI bulk regime,  $C_{gb}$  and  $C_{bg}$  measure the coupling between the metal and well charge while the channel is fully depleted. These electrostatic conditions are reported in Fig. 5.14 for  $C_{gb}$  and  $C_{bg}$  characteristics. This suggests, as carried out for the traditional MOS capacitor, to plot respectively  $C_{gb}$  and  $C_{bg}$  as a function of  $V_{GB}$  and  $V_{BG}$  (red arrows Figs. 5.14 a and b) and not as a function of  $V_{GS}$  and  $V_{BS}$  (black arrows Figs. 5.14 a and b). This means to plot these capacitance characteristics as a function of the potential difference between the metal and well electrodes.

Results for  $C_{gb}$  and  $C_{bg}$  are reported in Figs. 5.15 and 5.16. Starting with  $C_{gb}$  characteristics, we observe that by plotting them in function of  $V_{GB}$  voltage we obtain the full  $C_{gb}$  capacitance which is the result of the well charge evolution from depletion to strong accumulation condition.  $V_{GB}$  is defined as  $V_{GB} = V_{GS} + V_{SB}$  with  $V_{SB} = -V_{BS}$ . Each characteristic at a specific back bias  $V_B$  represents a portion of the entire capacitance. As reported in Fig. 5.15, the characteristic at  $V_B=6V$  (in green) features a capacitance for which the well ( $\Delta C_{Well1}$ ) is mostly in depletion regime while the characteristic at  $V_B=0V$  (in red) and finally the characteristics at  $V_B=-11V$  (in blue) features a capacitance for which the well is

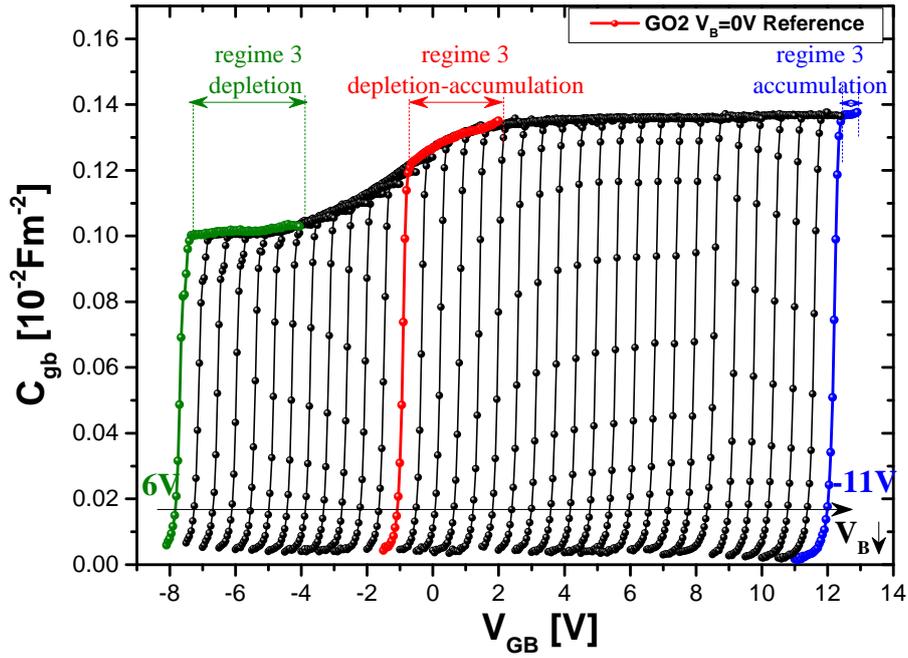


Figure 5.15:  $C_{gb}$  versus  $V_{GB}$  with back biasing  $V_B$  varying from 6V to -11V with a step of 0.5V.

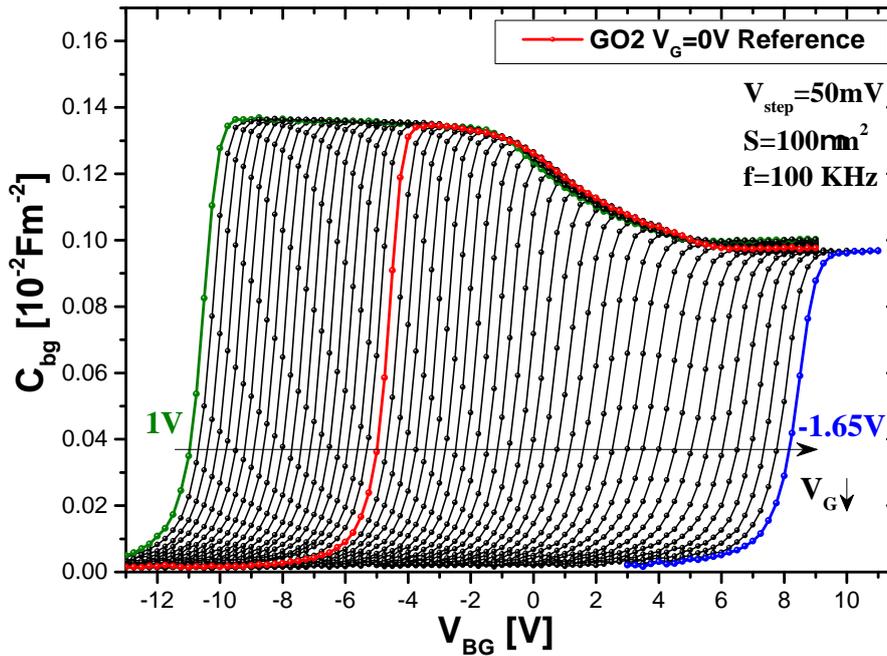


Figure 5.16:  $C_{bg}$  versus  $V_{BG}$  with front biasing  $V_G$  varying from 1V to -1.65V with a step of 50mV.

respectively in depletion-accumulation and strong accumulation regime. It rises up more clearly that only one  $C_{gb}$  measurement cannot figure the entire FDSOI bulk regime capacitance variation, but multiple characteristics at different  $V_B$  biases are necessary to rebuild it.

The reason are twofold:

- Front-oxide breakdown: We remember that for  $C_{gb}$  measurement we applied the High terminal ( $V_G - V_B$ ) on the Gate contact and Source and Drain are biased at  $-V_B$  (Fig. 5.10). It's obvious that  $V_G$  cannot largely varies since a high potential drop between the Gate and Source-Drain contacts could lead to the front-oxide breakdown.
- The voltage range of the FDSOI bulk regime: As we previously described the voltage range (eq. 5.19) for  $C_{gb}$  characteristics is not enough ( $\Delta V_{GS} \approx 1V$ ) to figure the entire evolution of the FDSOI bulk regime capacitance.

Therefore, by plotting the  $C_{gb}$  at different  $V_B$  biases as a function of  $V_{GB}$  we can rebuild the entire bulk regime capacitance. This is the answer at the first question of the previous section.

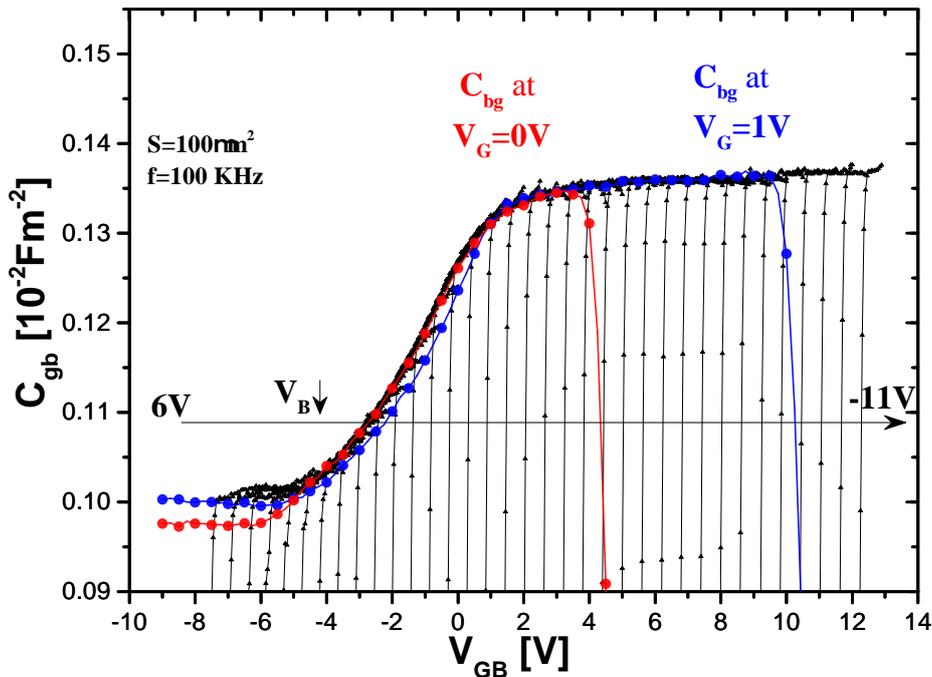


Figure 5.17:  $C_{gb}$  and  $C_{bg}$  versus  $V_{GB}$  measurement during the 3<sup>rd</sup> regime for a P-MOS GO2 Si channel device.

For what concerns  $C_{bg}$  versus  $V_{BS}$  characteristics, as previously put in evidence in Fig. 5.13, the set of characteristics looks more to a similar C-V characteristic.  $C_{bg}$  characteristics still need to be plotted as a function of  $V_{BG}$  voltage. Indeed as reported in Fig. 5.16, at first sight, we obtain a unique curve without any significant discrepancy among the characteristics at different front bias  $V_G$ . The characteristics at  $V_G=1V$  (in green),  $V_G=0V$  (in red) and  $V_G=-1.65V$

(in blue) are mostly superimposed. However these characteristics are not perfectly superimposed due to the distorted FDSOI bulk regime at which the FDSOI transistor undergoes. Indeed this regime deforms the FDSOI bulk regime capacitance since the channel electrons inversion occurs due to the thermal generation phenomena. The total  $C_{bg}$  capacitance can be obtained with only two characteristics in a valuable range (e.g.  $V_G=1V$  (in green) and  $V_G=0V$  (in red)) since the voltage range (eq. 5.14) of the FDSOI bulk regime for  $C_{bg}$  characteristic ( $\Delta V_{BS} \simeq 8V$ ) is higher compared to  $C_{gb}$  characteristic ( $\Delta V_{GS} \simeq 1V$ ).

The characteristics  $C_{gb}(V_{GB})$  and  $C_{dg}(V_{BG})$  should give the same exact capacitance. Indeed, by plotting  $C_{dg}$  as a function  $V_{GB}$  ( $=-V_{BG}$ ), and comparing it with  $C_{gb}(V_{GB})$  characteristic, we obtain the same characteristic, as reported in Fig. 5.17.  $V_{GB}$  is defined as ( $V_{GB} = V_{GS} + V_{SB}$  with  $V_{SB} = -V_{BS}$ ). This unique characteristic is the result of the direct coupling between metal and well whose charge progressively pass from depletion to accumulation region. This characteristic is the complete FDSOI bulk regime capacitance whose behavior is identical to a typical bulk capacitance characteristic (see Chapter 1). This answers to the second question of the previous section which clearly evidenced the apparent difference between  $C_{gb}$  and  $C_{dg}$  characteristics as a function of  $V_{GS}$  and  $V_{BS}$ . Such  $C_{dg}$  capacitance can be used in order to determine the condition of zero well charge or well flat band condition.

### 5.2.5 Identification of the well flat band condition ( $V_{fb\ w}$ ) and calculation of the total charge

The FDSOI bulk regime has a fundamental role to identify the electrostatic condition of the FDSOI transistor. Indeed, the well charge can be calculated from such experimental  $C_{bg}$  characteristic. Once the well flat band condition on the  $C_{bg}$  capacitance is determined, we can integrate  $C_{bg}$  capacitance from  $V_{fb}$  to any  $V_{GB}$  voltage, as carried out on the standard bulk transistor (chapter 1). Therefore, we have

$$Q_{Well} = \int_{V_{fb}}^{V_{GB}} C_{bg} dV_{GB} \quad (5.20)$$

This leads us to know the overall polarization state of the SOI well substrate at least during inversion or depletion conditions of the channel. The Gauss theorem tells us that the electric field at the channel surface will be the sum of the two components that are induced by the channel charge and substrate charge. Whereas the measurement of the channel inversion charge, which is calculated by simply integrating the capacitance  $C_{gc}$ , is well known in the state of the art, the measurement of the substrate charge is not common in MOS SOI technology since there's not a direct way to access to the substrate charge. Unlike the  $C_{gb}$  measurement of traditional MOS transistor whose entire depletion-accumulation regions are well known and thus their analysis of flat band condition and charge (Figs. 1.7 and 1.8 ) as a function of applied voltage, the  $C_{gb}$  measurement of FDSOI transistors is reported here for the first time (Fig. 5.17). We remind that this curve is a typical characteristic of a traditional MOS stack, where the gate is always the studied gate capacitance and its oxide corresponds to a stack composed of three dielectric layers (the Gate front-oxide, the depleted channel that behaves like a dielectric and finally the buried oxide or back-oxide) and the substrate is located at the backside of the buried oxide. The methodology, used in the state of the art in order to extract EOT and  $V_{fb}$  or  $WF_{eff}$  for a traditional MOS stack, can be used here to extract the  $V_{fb}$  and EOT for FDSOI transistors.

We report in Figure 5.18 the comparison of experimental with the C-V characteristic simulation that takes into account the quantum effects. With such fitting of experimental result with numerical simulation, a flat band voltage of 280mV and a dielectric equivalent thickness of 25.1 nm are obtained. This adjustment allows us to estimate the effective work function  $WF_{eff}$  of this stack (4.58 eV). The EOT is extracted as well in the accumulation region and it is equal

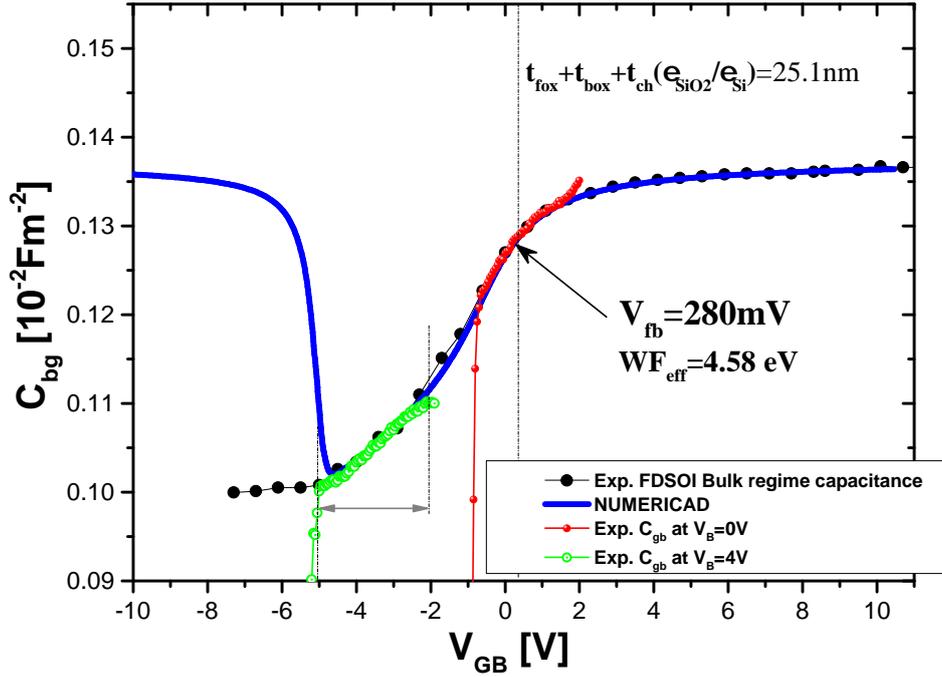


Figure 5.18: Extraction of  $V_{fb}$  from  $C_{bg}$  characteristic for a P-MOS Si channel N-type well transistor.

to

$$EOT = t_{fox} + t_{ch} \frac{\epsilon_{SiO2}}{\epsilon_{ch}} + t_{box} \quad (5.21)$$

The extracted effective work function is the  $WF_{eff}$  value of the metal Gate of the FDSOI stack and the EOT is the sum of 3 dielectrics thicknesses (front-oxide, channel and buried oxide) between the metal and well substrate. The value of the effective work function includes the cumulative impact of the different electrostatic effects (fixed charges and dipoles) across these 3 dielectrics.

The identified flat band voltage is independent of the Source and Drain voltage. Indeed, since the channel is fully depleted,  $V_s$  and  $V_D$  cannot control the electrostatics of the channel. The well flat band voltage can be identified on the classical  $C_{gb}$  characteristic at  $V_B=0V$  of Fig. 5.2 since we know that the flat band voltage of the substrate at the back of the buried oxide for which the total charge is zero. We are now able to calculate the channel and substrate charge for each  $V_{GS}$  voltage. In Figure 5.19 we report the superposition of the complete FDSOI bulk regime capacitance characteristic with  $C_{gb}$  characteristic at  $V_B=0V$ .

This charge calculation, performed for the different semiconductor layers (channel and substrate), is carried out and reported in Figure 5.20. The integral of these capacitances,  $C_{gc}$  and  $C_{gb}$  ( $F/m^2$ ), leads to the associated charges  $Q_{ch}$  and  $Q_{Well}$  ( $C/m^2$ ). We can also turn this charge into number of carriers  $N(Q_{tot})$  as

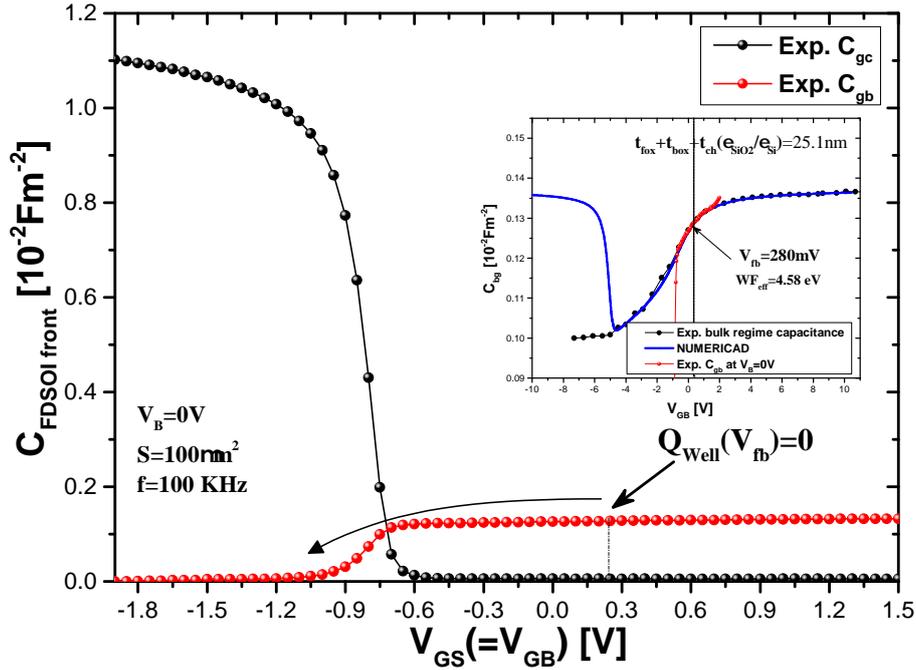


Figure 5.19: Identification of the flat band on front FDSOI capacitances.

reported in Figure 5.20 by considering the following relationship:

$$Q = q \cdot N(Q_{\text{tot}}) \quad (5.22)$$

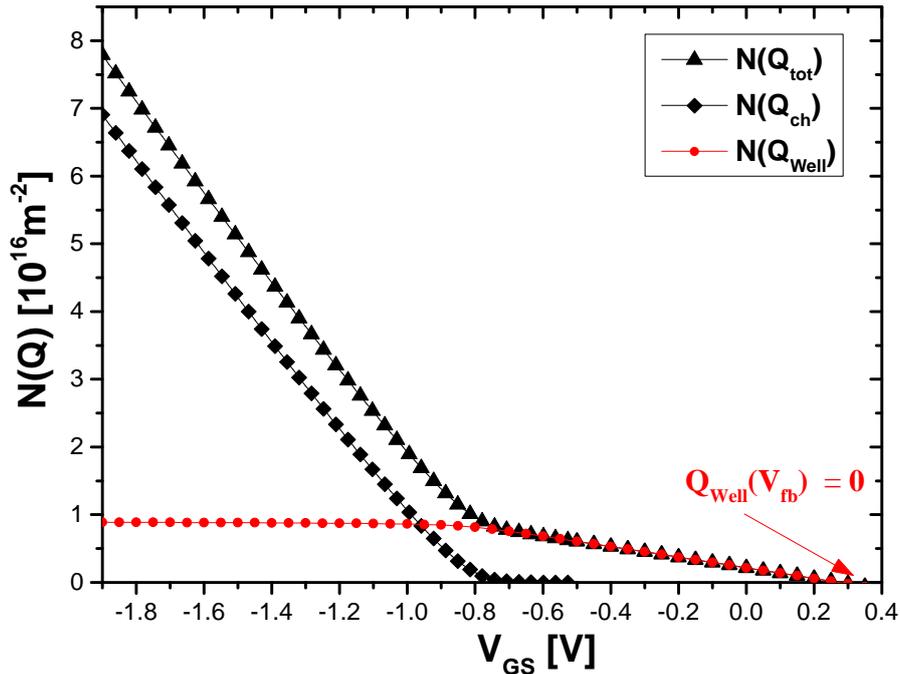
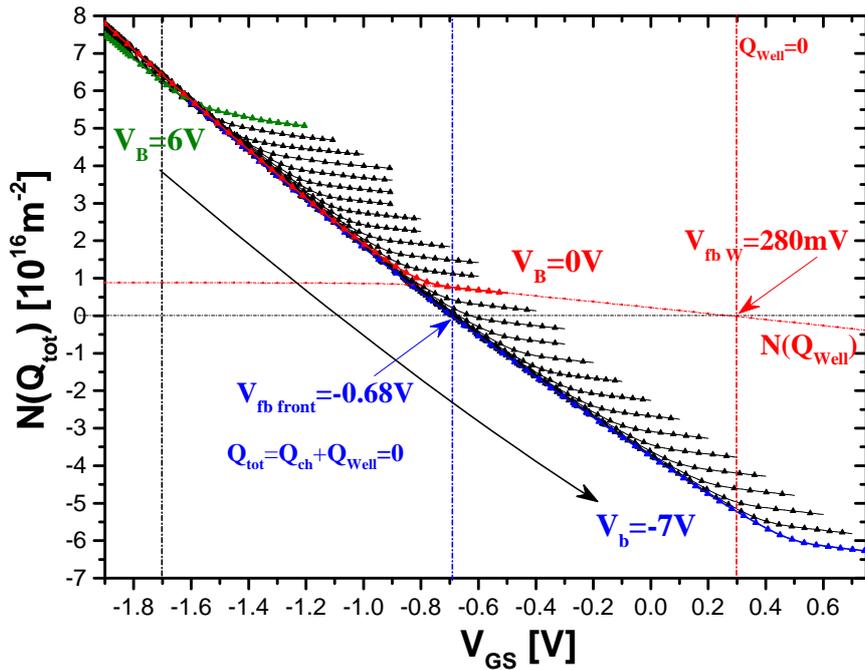
where  $q$  is the elementary charge. In Fig. 5.20, we report the trend for the two charges: the free carriers of the channel ( $Q_{\text{ch}}$ ) and the substrate charge ( $Q_{\text{well}}$ ). Strictly speaking, the total charge (seen at the front-oxide/channel interface) is the sum of the free charge and the fixed charge carriers:

$$Q_{\text{tot}} = Q_{\text{ch}} + Q_{\text{well}} + Q_{\text{ch fix}} + Q_{\text{box}} + Q_{\text{int}} \quad (5.23)$$

where  $Q_{\text{ch fix}}$  is the depleted charge ( $Q_{\text{ch fix}} = q t_{\text{ch}} N_{\text{ch}}$ ),  $Q_{\text{box}}$  is the sum of the fixed charges located within the buried oxide, including its front and back interface, and  $Q_{\text{int}}$  is the fixed charges located at the front-oxide/channel interface. Since we suppose a really low doping level in the channel and not significant presence of  $Q_{\text{int}}$  and  $Q_{\text{box}}$  charges, we simply propose:

$$Q_{\text{tot}} = Q_{\text{ch}} + Q_{\text{well}} \quad (5.24)$$

We can notice in Fig. 5.20 that once we have the onset of the inversion charge (square black) in the channel, the well charge (in red) saturates due to the

Figure 5.20:  $Q_{tot}$ ,  $Q_{ch}$  and  $Q_{Well}$  versus  $V_{GS}$  at  $V_B=0V$ .Figure 5.21:  $Q_{tot}$  versus  $V_{GS}$  at  $V_B$  from 6V to -7V with step of 0.5V.

screening effect. The value of well charge, during strong front channel inversion at  $V_{GS}=-1.8V$ , is important and not negligible. Indeed, its values is higher than 10% of the calculated channel charge at this voltage condition. As carried out for the reference characteristic at  $V_B=0V$ , the total charge at the front-oxide/channel interface can be calculated for all the characteristics at different  $V_B$ , since

we know the well flat band condition. Indeed, as reported in Fig. 5.18, the integral from the well flat band condition of the rebuilt FDSOI bulk regime C-V characteristic (black spheres) is sufficient to obtain the charge well at any  $V_{GB}$  voltage and for any  $C_{gb}$  characteristic (at any  $V_B$  voltage). For sake of clarity in Fig. 5.18, we report also the  $C_{gb}$  characteristic at  $V_B=4V$  (green circles). We remind that this characteristic is a part of the entire FDSOI bulk regime C-V characteristic (black spheres). It's obvious that the integral of FDSOI bulk regime C-V characteristic (black spheres) will give us the well charge values of the  $C_{gb}$  characteristic at  $V_B=4V$  (green circles). Once the well charge is known, the channel charge is obtained by integrating the  $C_{gc}$  at  $V_B=4V$  characteristic. The sum of the well and channel charges leads to the total charge for the characteristic at  $V_B=4V$ . In Fig. 5.21, we report the trends of the total number of carriers  $N(Q_{tot})$  as a function of  $V_{GS}$  voltage for all the back bias  $V_B$  varying from -7 (in blue) to +6 (in red) Volt from the reference characteristic  $V_B=0V$  (in red). Two regimes are observable for all the characteristics. The first is the channel depletion regime characterized by a lower slope and the second is the inversion channel regime whose slope is higher with respect to the channel depletion regime. It is noteworthy to observe that, apart from the depletion regime, as soon as we have the onset of inversion in the channel, all the different characteristics are superimposed. This seems to reflect a general behavior of the semiconductor, since it is a relationship between  $V_{GS}$  and  $N(Q_{tot})$  and appears to be independent of the applied  $V_B$  voltage. This general behavior will be investigated in the next section and will be the key for the proposition of an new extraction methodology of EOT and  $WF_{eff}$ . In Fig. 5.21 we also report the well flat band condition. This condition is identified during channel depletion regime and occurs for  $V_{GS}=V_{fb\ w}$  which is

$$\begin{cases} Q_{Well} = 0 \\ Q_{ch} = 0 \\ Q_{tot} = Q_{ch} + Q_{well} = 0 \end{cases} \quad (5.25)$$

Interesting is another electrostatic condition, which can be identified on Fig. 5.21 occurring during the channel inversion regime ( $Q_{ch} \neq 0$ ), that is

$$\begin{cases} Q_{ch} = -Q_{Well} \neq 0 \\ Q_{tot} = Q_{ch} + Q_{well} = 0 \end{cases} \quad (5.26)$$

This is the front flat band condition  $V_{fb\ front}$  for which the electric field on the front-oxide is zero assuming no fixed charges (see chapter 2). This condition (eq.

5.26), different from the well flat band condition (eq. 5.25), is identified for all the capacitance characteristics at  $V_B < 0$  (Fig. 5.21). In the next section, two main goals will be addressed. Firstly we will demonstrate why we have for a specific FDSOI stack a general trend. Secondly, we will see how this relationship  $N(Q_{tot})(V_{GS})$  can be used to carry out the extraction of  $WF_{eff}$  and EOT.

## 5.3 Analytical extraction based on universal curve $Q_{tot}(E_c-E_f)$

### 5.3.1 Universal Curve: $Q_{tot}(E_f-E_c)$

In the previous section, we have obtained the experimental characteristics of total charge  $N(Q_{tot})$ , seen at the front-oxide/channel interface, as a function of the applied voltage  $V_{GS}$  at different  $V_B$  back biases for a specific FDSOI transistor (P-MOS GO2 Si channel). We observed that a universal trend occurs once the channel is in inversion regime ( $Q_{ch} \neq 0$ ). Indeed, the characteristics are superimposed as reported in Fig. 5.21. This universal trend of the total charge as a function of the potential  $V_{GS}$  is investigated in this section. This universal behavior between  $N(Q_{tot})$  and  $V_{GS}$ , suggest us to investigate their relationship expressed in terms of FDSOI stack physical parameters which can be obtained from the analysis of the band diagram of Fig. 5.22

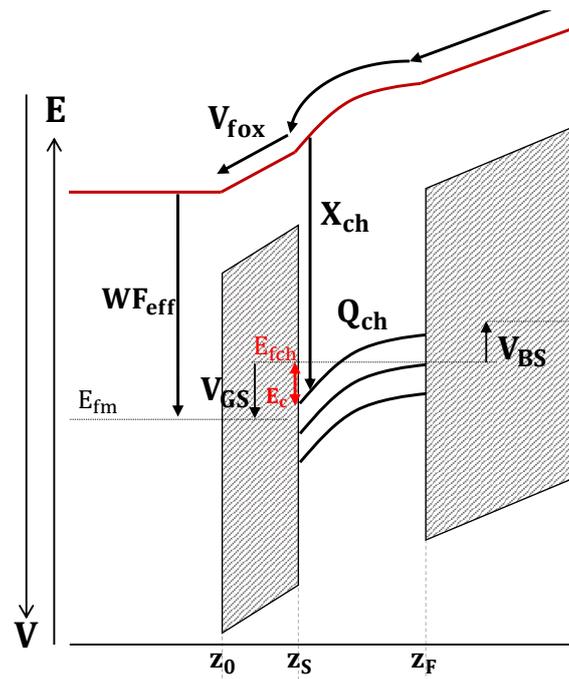


Figure 5.22: FDSOI band diagrams at the front oxide.

We can imagine that it is a relationship between the voltage drop in the semiconductor and the total charge seen at its interface. Indeed from the analysis

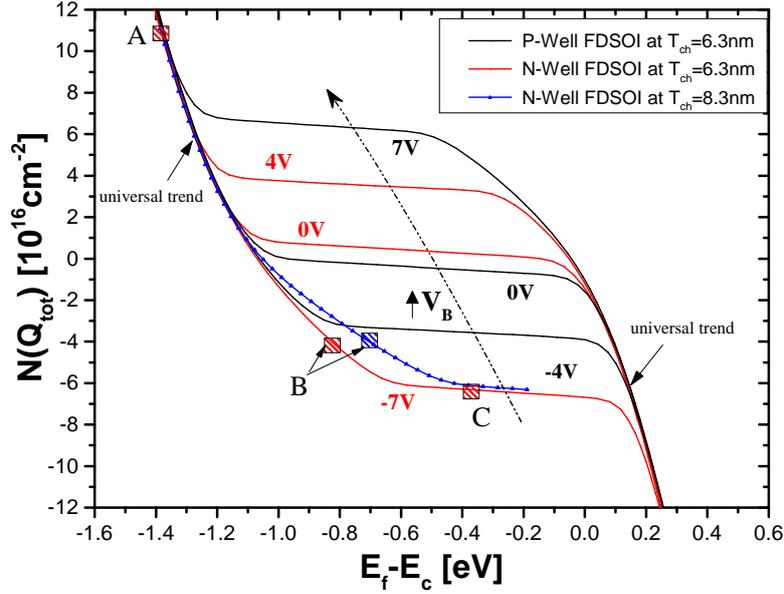


Figure 5.23:  $N(Q_{tot})(E_f - E_c)$  for different FDSOI and bulk transistors featuring different channel and doping type and level.

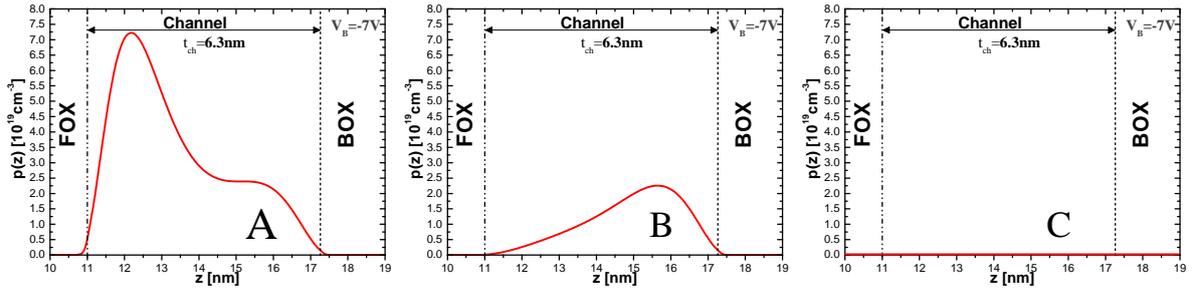


Figure 5.24: Distribution of the channel charge at 3 different conditions indicated in Fig. 5.23: (A) front channel inversion, (B) back channel inversion and (C) fully depleted channel.

of the band diagram of Fig. 5.22 we can easily obtain

$$V_{GS} = \frac{WF_{eff}}{q} + \frac{(E_{fch}(N(Q_{tot})) - E_c(N(Q_{tot})))}{q} - \frac{X_{ch}}{q} - \frac{qN(Q_{tot})EOT}{\epsilon_{SiO_2}} \quad (5.27)$$

where  $E_{fch}(N(Q_{tot})) - E_c(N(Q_{tot}))$  is the difference between the Fermi energy and the conduction band energy at the interface ( $z_S$ ) and  $-qN(Q_{tot})EOT/\epsilon_{SiO_2} = V_{fox}$ . Therefore, this relation 5.27 implies that if  $N(Q_{tot})(V_{GS})$  is universal then  $N(Q_{tot})(E_{fch} - E_c)$  must be also universal since  $WF_{eff}$ ,  $EOT$  and  $X_{ch}$  are constant parameters. Therefore, we carried out different simulations by coupling in a self-consistent way the Poisson and Schrodinger equations for different FDSOI devices and seeking each time to identify the relationship between the total charge  $Q_{tot} = Q_{ch} + Q_{well}$  located at the interface and the relative position of the Fermi level and the semiconductor conduction band always at the interface. This

study was made for transistors with SOI substrate featuring different channel material and different substrate type as well as back biases. In Figure 5.23, we report  $N(Q_{\text{tot}})$  as a function of  $(E_{f\text{ch}}-E_c)$  characteristics for two FDSOI transistors with the same Si channel thickness of 6.3 nm and a buried oxide of 20 nm and different well type (P in black and N in red at  $10^{18}\text{cm}^{-3}$ ) at  $V_B=7,4,0,-4$  and  $-7\text{V}$ . Two important observations can be done. Firstly, as we can see in Fig. 5.23 for the N-Well FDSOI simulations (red lines), a universal behavior is observed for electrons and holes independently of the applied back bias  $V_B$ . Secondly, a universal behavior is also observed independently of the Well-type of the devices. Indeed superimposition between simulations for the N-Well FDSOI (red lines) and P-Well FDSOI (black lines) occurs during electrons and holes channel inversion. In Fig. 5.23, we also report a simulation of a FDSOI at  $V_B=-7\text{V}$  which features the same front and back-oxide thicknesses of the previous N-Well FDSOI device (red lines) but different channel thickness  $t_{\text{ch}}=8.3\text{nm}$  (blue line). As reported in Fig. 5.23, the comparison of the characteristics at  $V_B=-7\text{V}$  for  $t_{\text{ch}}=6.3\text{nm}$  (red line) and  $t_{\text{ch}}=8.3\text{nm}$  (blue line) reveals still a universal trend of the  $N(Q_{\text{tot}})$  as a function of  $(E_{f\text{ch}}-E_c)$  characteristic but not for all the channel inversion regime. This can be explained by investigating the channel charge condition during the inversion regime. In Fig. 5.24, we report the channel charge distribution at three specific conditions indicated in Fig. 5.23 for the characteristic at  $V_B=-7\text{V}$  (red line), they are respectively the front channel inversion (A), the back channel inversion (B) and the fully depleted channel (C). Therefore, the characteristic  $N(Q_{\text{tot}})(E_{f\text{ch}}-E_c)$  at  $V_B=-7\text{V}$  (in red) has two different channel inversion conditions (front and back). We observe that whenever we are in the back channel inversion (Fig. 5.24 (B)), the two characteristics are not superimposed as indicated by the two boxes and arrows (red and blue stripes). This suggests us that a universal law can be observed once front channel inversion condition occurs. This is a necessary condition at the front-oxide channel interface.

Another aspect which needs to be investigated is the impact of the dimensions of the channel at really few nanometers (below 4 nm) on the universal characteristic during front channel inversion (holes and electrons). Indeed at this condition, the independence of the charge at the front-oxide/channel interface with respect to the potential at channel/back-oxide interface is investigated. In Fig. 5.25 (left figure), we report numerical simulation of the absolute value of  $N(Q_{\text{tot}})$  as a function of  $E_{\text{Ef}}-E_c$  for FDSOI devices featuring different channel thicknesses. These simulations have been carried out from

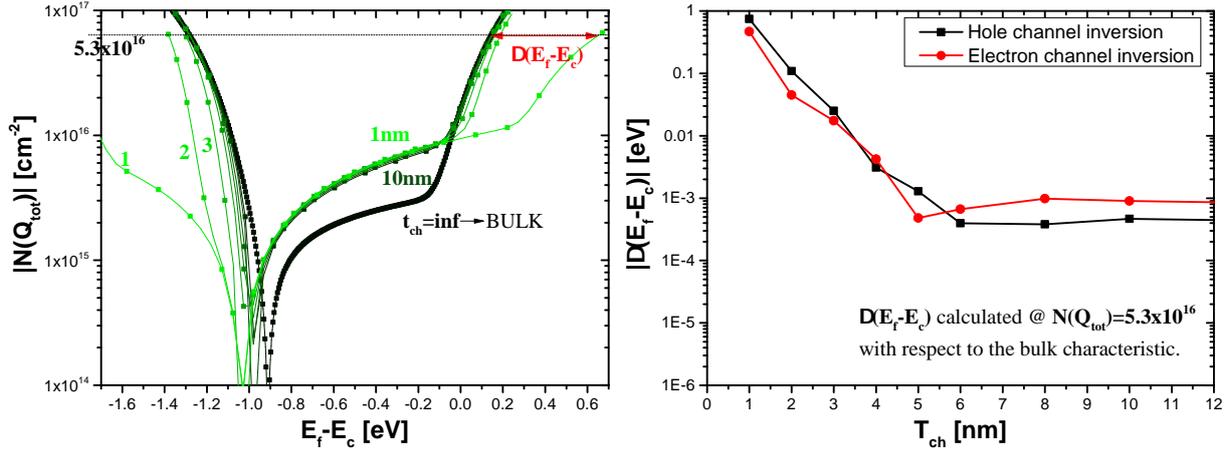


Figure 5.25: EMA numerical simulation of  $N(Q_{tot})$  as a function of  $(E_f-E_c)$  for FDSOI devices featuring different channel thicknesses (from 10nm to 1nm) and for bulk device featuring a 700nm substrate with  $10^{16}\text{cm}^{-3}$  doping level.

1nm to 10 nm channel thickness values and compared to a simulation of bulk transistor with  $10^{16}\text{cm}^{-3}$  doping level for which no back interface exist ( $t_{ch}=\infty$ ). Two important observations can be made:

1. The universal characteristic can be generalized to the case of bulk transistor (black line for  $N_a=10^{16}\text{cm}^{-3}$ ) since its characteristic during inversion or accumulation is superimposed with FDSOI numerical simulation characteristic as reported in Fig 5.25 (left figure).
2. The universal characteristic is valid for a channel thickness larger than 4nm since superimposition between the characteristics is no longer observed below this channel thickness limit. The associated shift  $\Delta(E_{EF}-E_c)$  calculated at  $N(Q_{tot})=5.3\times 10^{16}\text{cm}^{-3}$  with respect to the bulk characteristic at strong inversion and accumulation are reported in the right figure of Fig. 5.25.

In Fig. 5.25, we report the superimposition of the numerical FDSOI simulation with a single simulation of a P-type substrate bulk transistor with  $N_a=10^{16}\text{cm}^{-3}$ . This superimposition occurs independently of the doping level and type of the bulk transistor. In Fig. 5.26 we report numerical simulation (EMA approximation in red) of  $N(Q_{tot})$  as a function of  $E_{EF}-E_c$  characteristics for the previous P-type substrate bulk transistors with a doping level  $N_a$  of  $10^{16}$  and other two with an  $N_a$  of respectively  $10^{17}$ ,  $10^{18}\text{cm}^{-3}$ . As we can observe the universal trend occurs independently of the doping level and distribution.

It's worth to note that if a different formalism (classical Boltzmann formalism

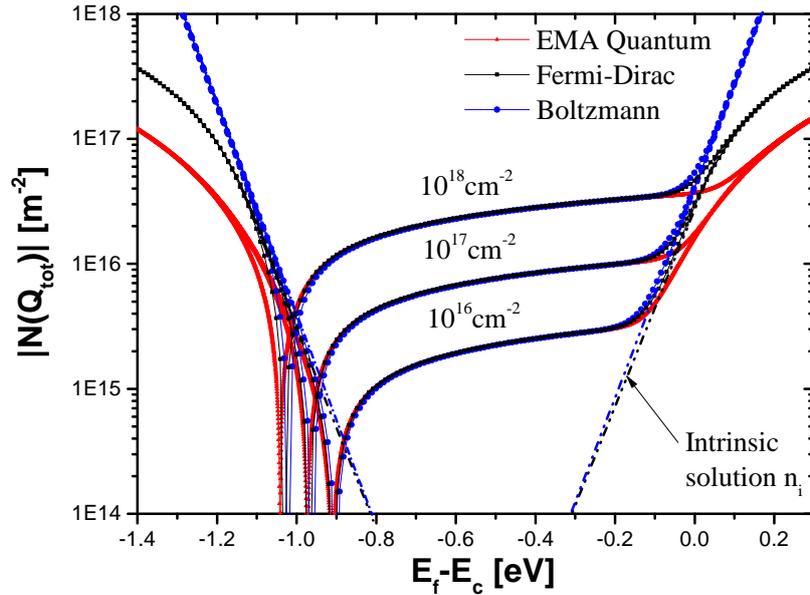


Figure 5.26:  $N(Q_{tot})(E_f-E_c)$  for different bulk transistors featuring different doping levels.

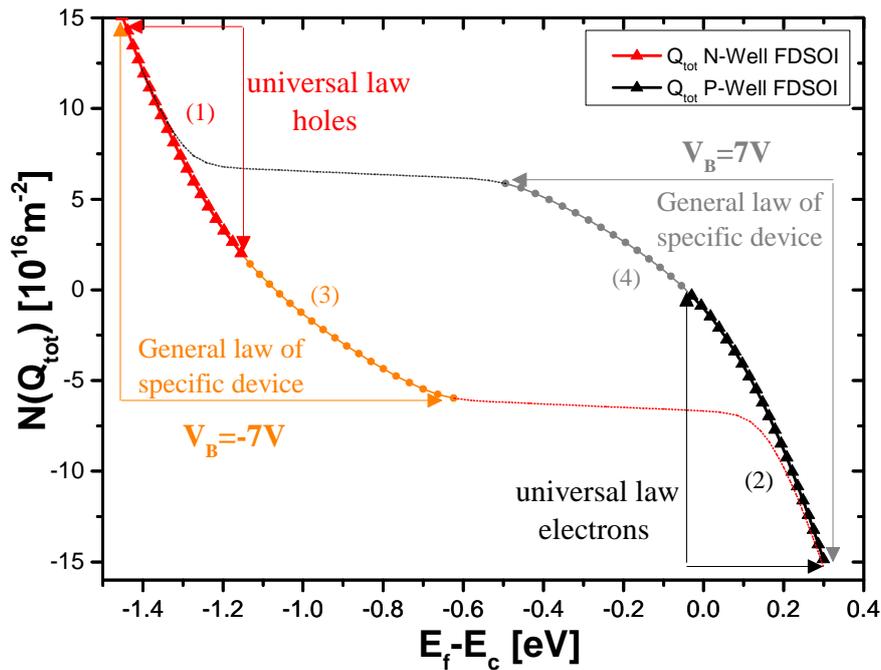


Figure 5.27:  $N(Q_{tot})(E_f-E_c)$  for two FDSOI featuring Si channel and two different doping type (N in red and P in black) at respectively  $V_B=-7V$  and  $V_B=7V$ .

(blue lines) and Fermi-Dirac formalism (black lines)) is used for the calculation of the total charge a different universal curve (for holes and electrons) is obtained as reported in Fig. 5.26. The independence of the universal curve with doping level can be easily proved in case of Boltzmann formalism by calculating the

intrinsic solution which is

$$Q_{sc} = \sqrt{2q\epsilon_{Si} \left[ \frac{n_i}{B} \left( e^{B\Psi_s} - 1 \right) + \frac{n_i}{B} \left( e^{-B\Psi_s} - 1 \right) \right]} \quad (5.28)$$

where  $B=1/k_B T$  and  $\Psi_s$  is the potential surface calculated in eV with respect to the intrinsic Fermi energy ( $E_i$ ). This characteristics which is a straight blue dashed line is reported in Fig. 5.26 as a function of  $E_f-E_c=\Psi_s-E_{gap}/2$ . More generally in case of a different doping concentration ( $N_a$  or  $N_d$ ) we can define the difference between the Fermi and conduction energies at the surface for a p-type substrate (blue lines in Fig. 5.26) as

$$E_f - E_c = \Psi_s - B \ln \left( \frac{N_a}{n_i} \right) - \frac{E_{gap}}{2} \quad (5.29)$$

This can be similarly obtained in case of n-type semiconductor ( $N_d$ ). The Boltzmann formalism doesn't take into account the quantum effects of the charge. Therefore, only numerical simulation results within EMA approximation are considered for a realistic description of the charge distribution. Therefore, the validity of the universal curve can be generalized for all possible FDSOI transistors featuring different channel ( $t_{ch}>4nm$ ) and buried oxide thicknesses and well and channel doping type and level. Moreover, as observed previously for the bulk simulation at  $10^{16}cm^{-3}$  doping level, this universal law can be validated on other bulk transistors featuring different doping level and distribution. We can conclude that once the onset of the inversion of free carriers in the channel (holes or electrons) occurs at the front-oxide/channel interface, we have a **universal law** for electrons or holes of total charge that depends only on the type of channel semiconductor that we simulate (Silicon, Germanium, GaN, etc...). These two universal laws for holes and electrons can be deduced for Silicon material from the characteristics of Fig.5.23 and are reported in red triangles for holes and black triangles for electrons in Fig. 5.27. These universal curves are reported for the first time (Fig. 5.27) and they will be used in order to extract EOT and  $WF_{eff}$  as we will show in the next section. The curves in orange circles and gray circles reported also in Fig. 5.27 represents the **general law of the specific FDSOI device** which is dependent of the buried oxide and channel thickness. These two curves can be also used in order to extract EOT and  $WF_{eff}$  since they include the back channel inversion regime (depends on the buried oxide and channel thickness) and the front channel inversion regime (universal law). These universal laws mean that once we are in accumulation or

inversion with free carrier becoming larger than any other source of charge, the dependence of potential at the interface reaches a universal behavior typical of the semiconductor that leads to unique dependence between the potential and its derivative. Such behavior disappears when we are no longer in a "one" interface situation: thin film before 4nm, nanowires, ect..

### 5.3.2 $WF_{eff}$ and EOT extraction based on $Q_{tot}(E_f-E_c)$ of MIS structure

The relation between  $N(Q_{tot})$  and  $V_{GS}$  suggest to rewrite equation 5.27 as follows

$$qV_{GS} + X_{ch} - (E_{fch}(Q_{tot}) - E_c(Q_{tot})) = WF_{eff} - \frac{q^2 N(Q_{tot}) EOT}{\epsilon_{SiO_2}} \quad (5.30)$$

where  $X_{ch}$  is the electronic affinity of the reference semiconductor (4.2 eV for Silicon) due to the value used in the PS simulator. Therefore, we expect that plotting  $qV_{GS} + X_{ch} - (E_f - E_c)$  as a function of  $N(Q_{tot})$  leads to a linear law whose slope is proportional to EOT and the ordinate at the origin is the effective work function. The linearity is maintained only during front channel inversion condition.

We remind that we have already obtained the experimental relationship between  $V_{GS}$  and  $N(Q_{tot})$  for a specific FDSOI transistor (in our case a P-MOS GO2 Si Channel device) as reported in Fig. 5.21. Therefore, we can use the general curve of the FDSOI device for holes inversion ( $E_{Ef} - E_{Ec}$ ), obtained numerically as reported in Fig. 5.27 (orange circles n. 3), in order to extract EOT and  $WF_{eff}$  for this specific FDSOI transistor. Indeed for each specific experimental  $N(Q_{tot})$  value we know the associated numerical value of  $E_{Ef} - E_{Ec}$ .  $WF_{eff}$  extraction is therefore obtained with an innovative methodology compared to the previous works in the state of the art [13, 14, 15].

This kind of plot, for the characteristics of the P-MOS GO2 Si channel device is reported in Figure 5.28. The EOT and  $WF_{eff}$  extraction has been carried out by using its experimental  $Q_{tot}(V_{GS})$  relationship reported in Figure 5.20. As we can observe, the characteristic is linear for most of the total charge range which represents the front channel inversion regime. Once the channel is in depletion regime, the  $qV_{GS} + X_{ch} - (E_f - E_c)$  versus  $N(Q_{tot})$  characteristic is no longer linear and the experimental curve (red line) starts to detach from the linear curve (black dotted line). The linear characteristic leads us to an estimation of  $WF_{eff}$  and EOT through the calculation of its slope ( $q^2 EOT / \epsilon_{SiO_2}$ ) and the interception of line with y axis (at  $Q_{tot}=0$ ) as reported in Fig. 5.28. In this case, we find 4.59 eV and 2.75nm for a P-MOS GO2 featuring Si channel and a N-type well which is in agreement with the simulation result obtained in chapter 3.

The same calculation can be carried out for all the capacitance characteristics at different  $V_B$  back biases as reported in Fig. 5.29. As we can observe, from positive (5V in green) to large negative voltage (-7V in blue), the function (eq.

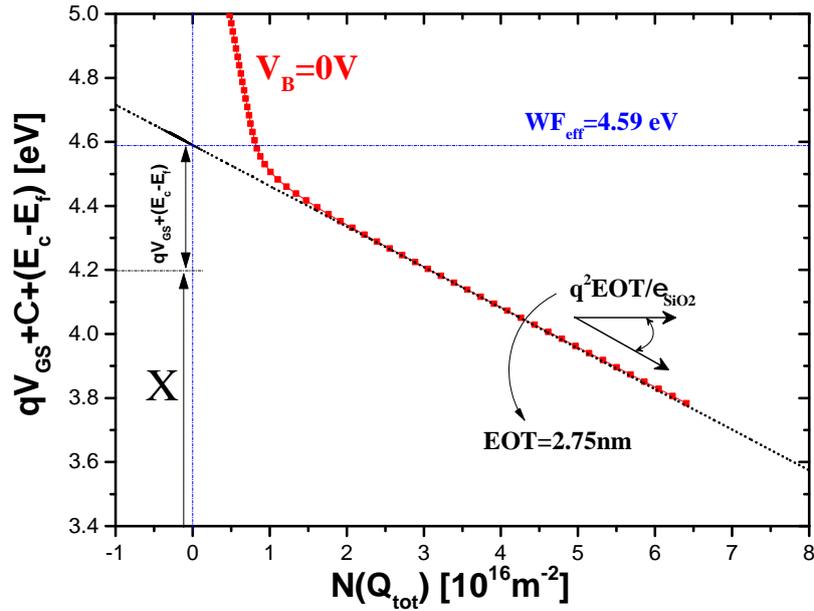


Figure 5.28:  $WF_{eff}$  and EOT extraction for a P-MOS GO2 device featuring a Si-channel and N-type well at  $V_B=0V$ .

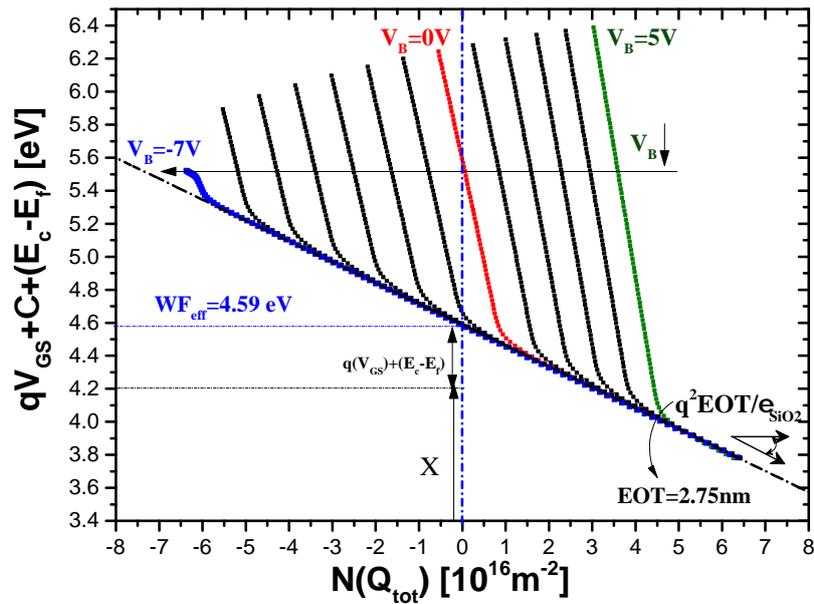


Figure 5.29:  $WF_{eff}$  and EOT extraction for a P-MOS GO2 device featuring a Si-channel and N-type well from  $V_B=5V$  to  $-7V$  with a step of  $1V$ .

5.30) has a linear trend for more extended  $N(Q_{tot})$  range. Indeed if we take into consideration the characteristic at  $V_B=-7V$  (in blue) we observe that its linear region is bigger with respect to all the other characteristics (e.g.  $V_B=0V$  in red Fig. 5.28). This extended region represent the back channel and front channel inversion conditions. We remind that in order to carry out the EOT and  $WF_{eff}$  extraction we are using here the law of the specific FDSOI for which the channel

thickness is 6.3nm (orange circles in Fig. 5.27 curve 4).

Therefore, the linearity is maintained with same slope during these two regimes since the channel thickness value used in the PS simulation (6.3nm in this case) in order to obtain  $E_f-E_c$  corresponds to the physical thickness of this specific P-MOS GO2 devices. The channel thickness value has a huge impact on the  $N(Q_{tot})(E_f-E_c)$  characteristic during back channel inversion regime (see Fig. 5.23). Indeed if the simulation  $E_f-E_c$  used for the extraction was obtained with a different channel thickness, a linear characteristic will be obtained only during front channel inversion condition and not back channel inversion regime as will be shown in case of GO1 device in Fig. 5.31.

Indeed this reduced linearity is observed on the extraction of EOT and  $WF_{eff}$  for a P-MOS GO1 (EOT=0.85nm) device Si-channel and N-type well which features a different channel thickness (5.7nm) compared to the previous GO2 device (6.3nm). The comparison of its  $N(Q_{tot})(V_{GS})$  characteristics with respect to our previous GO2 device characteristics is reported in Fig. 5.30. A general trend is also observed for GO1 device. Indeed once the channel inversion occurs the different characteristics (red lines) are superimposed. Another important observation is the higher slope of the  $N(Q_{tot})(V_{GS})$  for the GO1 device (red lines) with respect to GO2 device (black lines). Indeed, we remind that these characteristics depend on Gate stack technological parameters as EOT (GO2 in black and GO1 in red), channel material (both Si) and  $WF_{eff}$  during front channel inversion. Since GO1 device features a smaller dielectric than GO2 device, this explains the higher characteristic slope for GO1 device with respect to GO2 device. In Fig. 5.31, we report the extraction of EOT and  $WF_{eff}$  for the two devices when we use the same universal law obtained at  $t_{ch}=6.3nm$ . As we can observe, the straight line for GO1 device characteristic at  $V_B=-7V$  is not obtained for all the inversion regime range ( $6 \times 10^{16} cm^{-2} < N(Q_{tot}) < 8 \times 10^{16} cm^{-2}$ ). Indeed as we can observe this experimental curve (red line) is superimposed with a straight green line only for positive total charge values when front channel inversion occurs. A linear law is obtained which is sufficient to extract the technological parameter of the transistor. Indeed, a value of  $WF_{eff}$  and EOT of 4.65eV and 0.85nm is obtained for the GO1 as reported in Fig. 5.31. This result can be obtained by only using the characteristic at  $V_B=0V$ . We can resume the main important steps to perform an extraction of EOT ( $t_{fox}$ ) and  $WF_{eff}$  at the front Gate stack of a specific FDSOI transistor.

- 4 C-V measurements are firstly carried out on the FDSOI transistor which

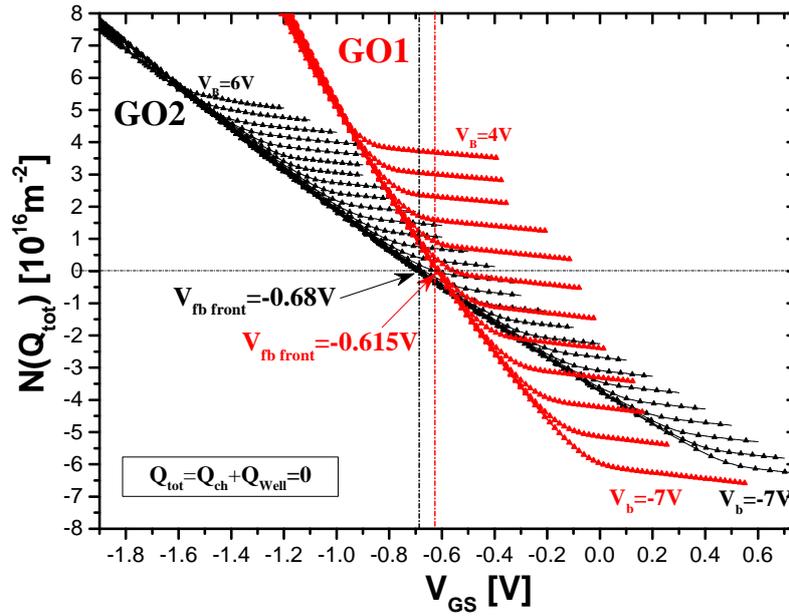


Figure 5.30:  $N(Q_{tot})$  versus  $V_{GS}$ : comparison between GO1 ( $t_{ch}=5.7\text{nm}$ ) and GO2 ( $t_{ch}=6.3\text{nm}$ ).

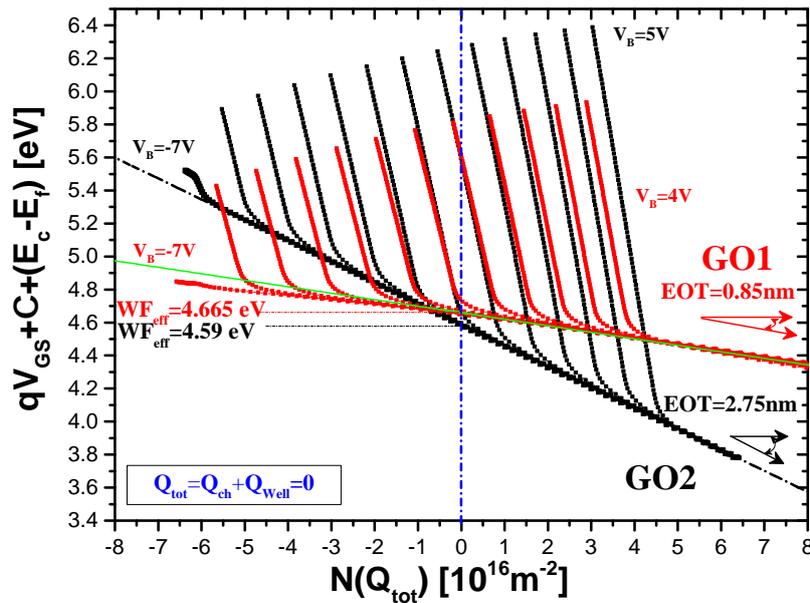


Figure 5.31: Extraction  $WF_{eff}$  and EOT for GO1 and GO2 devices.

are respectively the "front" capacitances ( $C_{gc}$  and  $C_{gb}$ ) and the "back" capacitances ( $C_{bc}$  and  $C_{bg}$ ) at different  $V_B$  and  $V_G$  biases.

- $C_{bg}(V_{GB})$  characteristics are used to rebuild the entire FDSOI bulk regime capacitance.
- This  $C_{bg}$  FDSOI bulk regime measurement is used to extract  $WF_{eff}$  from the well flat band condition and  $t_{box} + t_{ch}\epsilon_{SiO2}/\epsilon_{ch} + t_{fox}$  from the accumulation

region of the capacitance.  $t_{box}$ ,  $t_{ch}\epsilon_{SiO_2}/\epsilon_{ch}$  and  $t_{fox}$  are respectively the thicknesses of the buried oxide, silicon channel and the Gate front-oxide. This method turns the FDSOI problem into a typical MOS on bulk substrate extraction problem.

- The identification of the well flat band on  $C_{bg}(V_{GB})$  allows us to calculate the total charge using also "front" capacitances ( $C_{gc}$  and  $C_{gb}$ ) characteristics at  $V_B=0V$ . The well charge is obtained by integrating the  $C_{gb}$  characteristic from well flat band and the channel charge from the integration of  $C_{gc}$  characteristic. Relationship between the total charge  $N(Q_{tot})$  and  $V_{GS}$  voltage is obtained for the C-V characteristic at  $V_B=0V$ .
- The methodology also lies on, discovering under certain conditions (accumulation or inversion at the front channel interface), a universal relationship between the total charge  $N(Q_{tot})$  and  $E_f-E_c$  the position of which depends only on the semiconductor nature (Silicon in this work) when front channel inversion regime occurs.
- As suggested by equation 5.30, the extraction of EOT and  $WF_{eff}$  for a specific FDSOI stack can be carried by plotting  $qV_{GS}+X-(E_f-E_c)$  as a function of  $N(Q_{tot})$  using the general law of the FDSOI (orange (3) or gray (4) circles in Fig. 5.27)  $E_f-E_c$  which includes the universal law (red (1) or black (2) triangles in Fig. 5.27) and the experimental relationship  $N(Q_{tot})(V_{GS})$  at  $V_B=0V$ . From the slope of this plot and the interception at y axis EOT and  $WF_{eff}$  are extracted.

### 5.3.3 $X_{\text{eff}}$ and $t_{\text{box}}$ extraction using $Q_{\text{tot}}(E_f-E_c)$ of SIS structure

The front Gate stack is a typical metal-insulator-semiconductor (MIS) structure. The extraction methodology, previously proposed, is perfectly adequate for MIS structure since equation 5.30 relates the applied voltage  $V_{\text{GS}}$  between the channel and the metal to the total charge  $N(Q_{\text{tot}})$  seen at the front-oxide/channel interface. Therefore, the use of only one single universal curve (electrons or holes)  $N(Q_{\text{tot}})(E_f-E_c)$  is sufficient in order to extract EOT and  $WF_{\text{eff}}$  structure since only one semiconductor is present in such MIS structures. In some case polysilicon replaces the metal of MIS structure, leading to a stack composed by an insulator and two semiconductors which is known as SIS structure [16]. The semiconductor shows a different electrical behavior compared to the metal in terms of charge behavior. Typical phenomena of the semiconductor charge such as dark space, depletion and potential drop are not occurring in case of metal since the charge is ideally placed at the oxide interface. It is for this reason that the use of the relationship  $N(Q_{\text{tot}})(E_f-E_c)$  is necessary to take into account the nature of the semiconductor. Therefore, its obvious that contrary

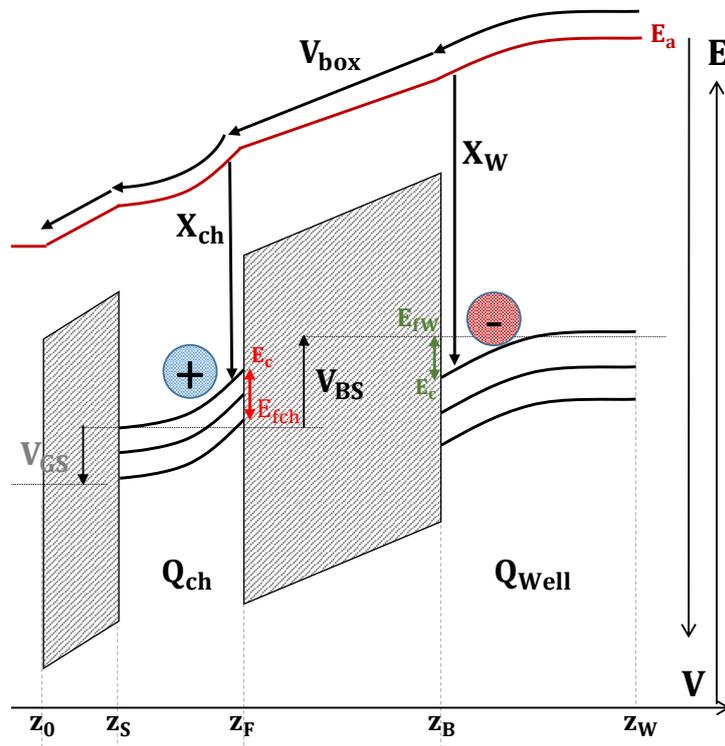


Figure 5.32: FDSOI band diagrams at the back oxide during  $C_{bc}$  measurement.

to the MIS structure, two universal curves are necessary in order to extract

the technological parameters of a semiconductor-insulator-semiconductor (SIS) structure stack due to the presence of two semiconductors. A typical SIS structure in a FDSOI transistor is the back Gate stack which features a buried oxide insulator between two semiconductors (the channel and the well) as reported in Fig. 5.32. During back Gate operation ( $C_{bc}$  and  $C_{bg}$  measurements) the total charge seen at channel/back-oxide interface is:

$$Q_{tot} = Q_{ch} + Q_m = -Q_{well} \quad (5.31)$$

The band diagram of Fig. 5.32 represents the back Gate stack at strong back channel inversion (holes,  $+Q_{tot}$ ) condition while the well is in accumulation (electrons,  $-Q_{tot}$ ). It comes out naturally that equation 5.30 is no longer adequate for SIS structure. From the band diagram of Fig. 5.32, we can easily obtain the correct relation for the back Gate stack which is:

$$V_{BS} = \frac{X_W - X_{ch}}{q} - \frac{E_{fW}(-Q_{tot}) - E_{cW}(-Q_{tot})}{q} + \frac{E_{fch}(Q_{tot}) - E_{cch}(Q_{tot})}{q} - \frac{qN(Q_{tot})t_{box}}{\epsilon_{SiO_2}} \quad (5.32)$$

We remind  $X_{ch}$  and  $X_W$  are the electron affinity of the channel and well. Relation 5.32 doesn't take into account the presence of dipoles and fixed charges across the buried oxide. Therefore, we feel essential to introduce a new parameter: the effective electron affinity  $X_{eff}$  which is defined as

$$X_{eff} = X_W - \frac{qQ_{fi}}{C_{box}} + q\delta_d \quad (5.33)$$

where  $qQ_{fi}/C_{box}$  is the shift induced by the fixed charges  $Q_{fi}$  and  $q\delta_d$  is shift induced by the dipole present at the channel/back-oxide interface. This technological parameter, equivalent to  $WF_{eff}$  for the front Gate stack, takes into account the eventual dipoles and fixed charge across the buried oxide. Therefore, equation 5.32 can be rewritten as

$$qV_{BS} + (E_{fW}(-Q_{tot}) - E_{cW}(-Q_{tot})) - (E_{fch}(Q_{tot}) - E_{cch}(Q_{tot})) + X_{ch} = X_{eff} - \frac{q^2N(Q_{tot})t_{box}}{\epsilon_{SiO_2}} \quad (5.34)$$

As equation 5.34 suggests, if we plot  $qV_{BS} + X_{ch} + (E_{fW}(-Q_{tot}) - E_{cW}(-Q_{tot})) - (E_{fch}(Q_{tot}) - E_{cch}(Q_{tot}))$  as a function of  $N(Q_{tot}) = N(Q_{ch} + Q_m)$ , a linear dependence can be observed with a slope proportional to  $t_{box}$  and an ordinate at the origin equalling the effective electron affinity of the well. In order to carry out this extraction we need two universal laws which are:

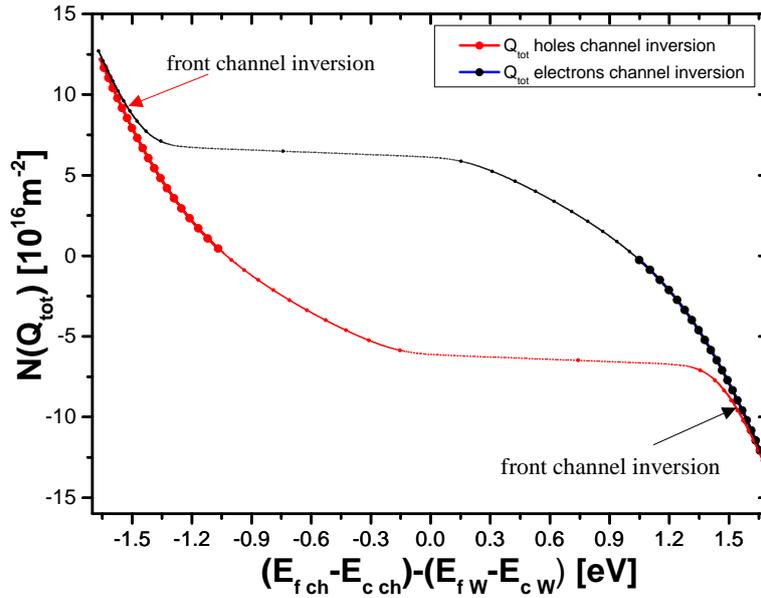


Figure 5.33:  $N(Q_{tot})(E_f-E_c)$  for two FDSOI featuring Si channel and two different doping type (N in red and P in black) at respectively  $V_B=-7V$  and  $V_B=7V$ .

- $(E_{fw}(-Q_{tot})-E_{cw}(-Q_{tot}))$  which is related to the well substrate (electrons curve).
- $(E_{fch}(+Q_{tot})-E_{cch}(+Q_{tot}))$  which is related to the channel (holes curve).

This differences  $(E_f-E_c)$  in terms of Energy are calculated for the well and channel charge at  $Q_{tot}$  and  $-Q_{tot}$  conditions. As we can notice from equation 5.34 what we need is the difference between two universal characteristics which can be easily calculated from the characteristics of Fig. 5.27. The results is reported in Fig. 5.33. The necessary step required to carry out the extraction is to calculate the back Gate stack  $N(Q_{tot})(V_{BS})$  experimental relationship as previously done for the front Gate stack  $(N(Q_{tot})(V_{GS}))$  Fig. 5.21). We remind that the total charge during back operation is  $Q_{tot}=Q_m+Q_{ch}$ . Therefore, in order to calculate the channel and the metal charge we need to integrate respectively the capacitance  $C_{bc}$  and  $C_{bg}$  of Fig. 5.4 from the well flat band condition ( $V_{fb_w}$ ) as previously carried out for  $C_{gc}$  and  $C_{gb}$  measurement (Figs. 5.19 and 5.20). The well flat band voltage is the same of Fig. 5.18 but with opposite sign. During the 3<sup>rd</sup> regime (or FDSOI bulk regime), we have

$$Q_m = -Q_w \quad (5.35)$$

This means that when we integrate  $C_{bg}$  from well flat band condition to any  $V_{BS}$  we obtain simultaneously both the well and metal charge since the depleted channel charge is negligible. In Fig. 5.34 we report the capacitance of Fig. 5.4 and the well flat band condition (or metal), from which we can calculate

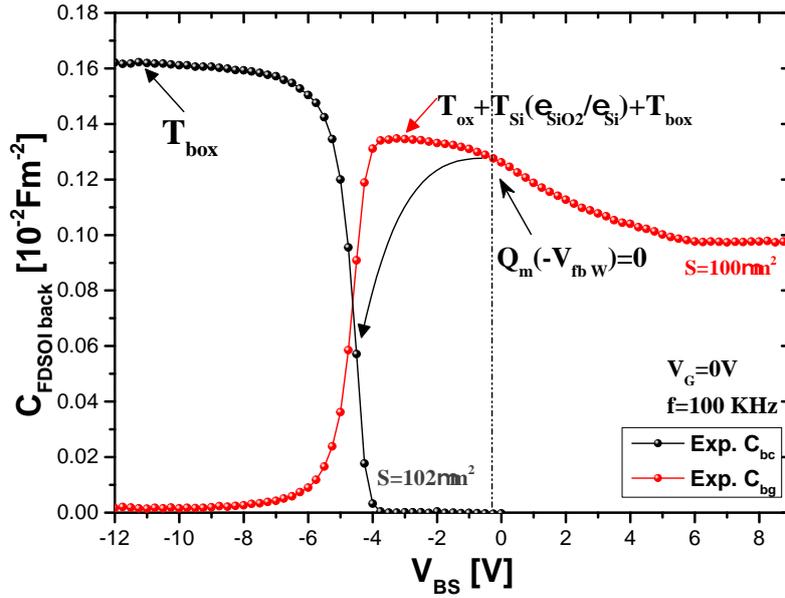
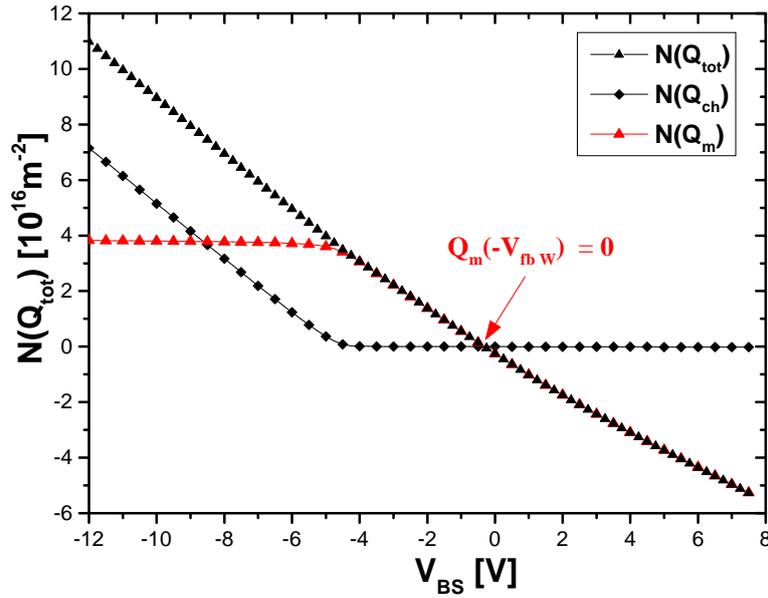
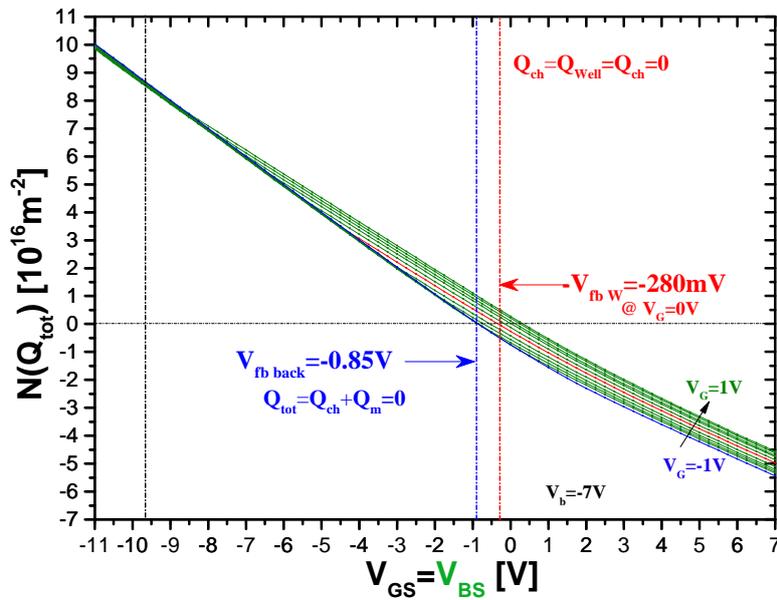


Figure 5.34:  $C_{bc}$  and  $C_{bg}$  versus  $V_{BS}$  characteristics at  $V_G=0V$ .

the total charge. The channel charge can be easily calculated by integrating the capacitance  $C_{bc}$  (black circled line Fig. 5.34). In Figure 5.35, we reported the trend of the two charges: the free carriers of the channel ( $Q_{ch}$ ) and the substrate charge ( $Q_{well}$ ). As we can notice in Fig. 5.35, once we have the onset of the inversion charge (square black) in the channel, the metal charge (in red) saturates due to the screening effect. The value of metal charge, during strong back channel inversion is fixed and not necessary equal to zero. Consequently  $C_{bg}$  signal is absent. On the contrary, when channel inversion doesn't occur, the metal charges varies as a function of  $V_{BS}$  from its flat band condition as in the standard MOS transistor (FDSOI bulk regime). As carried out for the reference characteristic at  $V_G=0V$ , the total charge can be calculated for all the characteristics at different  $V_G$  once we know the flat band condition. In Figure 5.36, we report the trends of the total number of carriers  $N(Q_{tot})$  for back bias  $V_G$  varying from -1 to 1 Volt (the reference characteristic  $V_G=0V$  is in red). It is noteworthy to observe that, apart from the depletion regime, as soon as we have the onset of inversion in the channel, the different curves are superimposed. This reflects the general behavior  $N(Q_{tot})(V_{BS})$  of the back Gate stack of the FDSOI device, such as for  $N(Q_{tot})(V_{GS})$  (black lines reported in Fig. 5.36 from Fig. 5.21) for the front Gate stack. Interesting is another condition for which the total charge is zero. Indeed as reported clearly in Fig. 5.21, we can observe that another flat band condition can be identified at  $V_{GS}=-0.85V$ , called back flat band voltage  $V_{fb\ back}$ . This condition occurs when the channel is in inversion regime contrary


 Figure 5.35:  $Q_{tot}$ ,  $Q_{ch}$  and  $Q_m$  versus  $V_{BS}$  at  $V_G$  at 0V.

 Figure 5.36:  $Q_{tot}$  versus  $V_{BS}$  at  $V_G$  from 1V to -1V with step of 0.2V.

to the well flat band condition, which is

$$\begin{cases} Q_{ch} = -Q_m \neq 0 \\ Q_{tot} = Q_{ch} + Q_m = 0 \end{cases} \quad (5.36)$$

The electric field at the back oxide (look chapter 2) induced by  $Q_{ch}$  and  $Q_m$  at  $V_{BS} = -0.85V$  for characteristic at  $V_G = -1V$  (blue line in Fig. 5.21) is zero. As previously said, these characteristics  $N(Q_{tot}(V_{GS}))$  can be used to carry out the

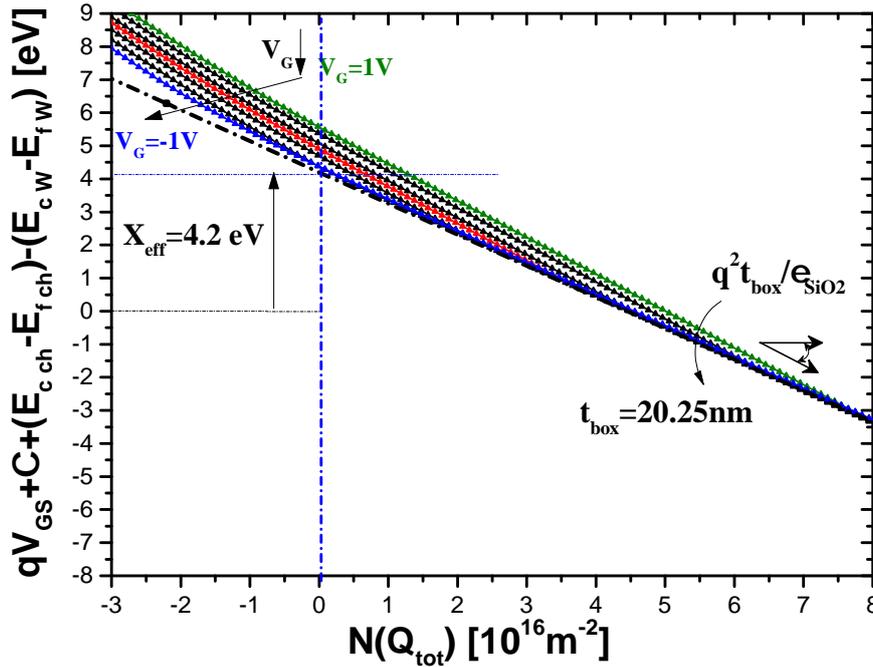


Figure 5.37:  $X_{\text{eff}}$  and  $t_{\text{box}}$  extraction for a P-MOS GO2 device featuring a Si-channel and N-type well from  $V_G=1\text{V}$  to  $-1\text{V}$ .

extraction of  $t_{\text{box}}$  and  $X_{\text{eff}}$  by using the two universal laws and relation 5.34. In Fig. 5.37 we report the result of the extraction of the technological parameters of the back Gate stack for the same P-MOS GO2 Si channel device. A buried oxide thickness and the effective electron affinity values of respectively 20.25nm and 4.2 eV are obtained. The extraction of the BOX thickness doesn't need any quantum correction since both the numerical universal curves, used for the channel and well, are taking into account the quantum phenomena occurring in these layers (dark space, wave function penetration).

### 5.3.4 Si versus SiGe channel

We have applied these innovative measurement methodologies to the characterization of the FDSOI gate stack, enabling an accurate evaluation of the thickness of the different layers ( $EOT$ ,  $t_{ch}$ ,  $t_{box}$ ) and the extraction of the effective work function  $WF_{eff}$  (using  $C_{bg}$  measurement Fig. 5.18 and using the total charge Fig. 5.29) or effective electron affinity  $X_{eff}$ . These innovative methodologies can be applied also to FDSOI transistor with SiGe channel [17, 18]. We remind that a  $V_{th}$  shift on  $C_{gc}$  characteristic is observed with SiGe channel devices with respect to the Si channel devices (see chapter 3). In Fig. 5.38, we report  $C_{gc}$  characteristics for two P-MOS FDSOI devices featuring the same GO1 front oxide, same buried oxide, N-type well but different channel material.  $Si_{0.75}Ge_{0.25}$  induces a  $V_{th}$  shift of 340mV. An hypothesis of the presence of the dipole (160mV) at the front-oxide/channel interface and valence energy shift (180mV) was made in chapter 3 in order to account of observed experimental  $V_{th}$  shift between the  $C_{gc}$  characteristics. This hypothesis was proposed by A. Soussou et al. [19] in order to justify the shift occurring in presence of SiGe channel material in bulk transistor. This hypothesis is fundamental since it

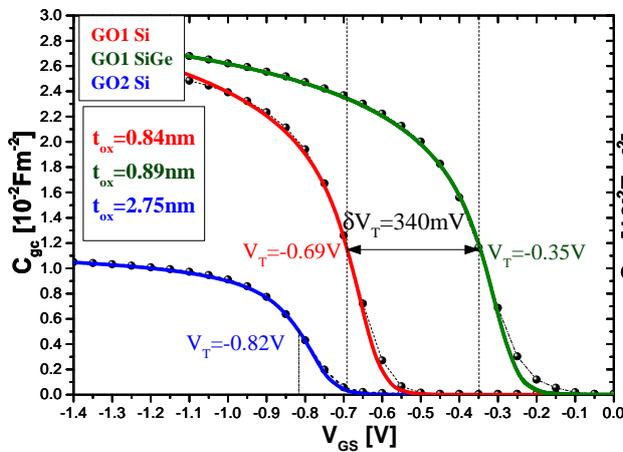


Figure 5.38:  $C_{gc}$  versus  $V_{GS}$  at  $V_B=0V$  for 3 PMOS devices: GO1 with Si (red) and SiGe (green) channel and GO2 with Si channel (blue).

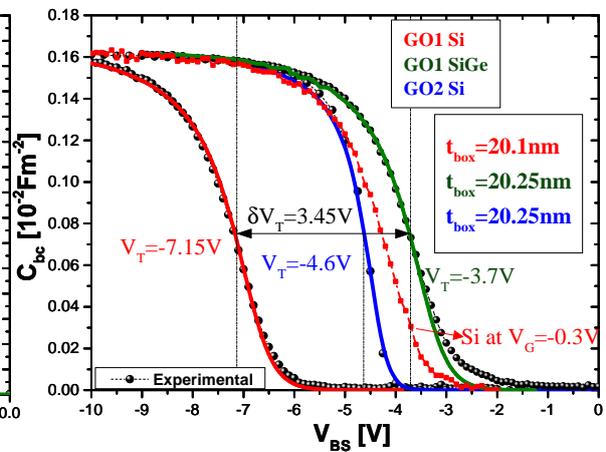


Figure 5.39:  $C_{bc}$  versus  $V_{BS}$  at  $V_G=0V$  for 3 PMOS devices: GO1 with Si (red) and SiGe (green) channel and GO2 with Si channel (blue).

defines the value of the effective work function for devices featuring a SiGe channel. Therefore, we feel essential to investigate and try to validate the hypothesis of the dipole presence at the dielectric-semiconductor interface. Moreover, the physical parameters values of SiGe material proposed by A. Soussou et al. [19] and used to carry out properly the EOT and  $WF_{eff}$  extraction

(see Chapter 2) are investigated. In order to validate this hypothesis, we will apply the previous methodologies of extraction on the P-MOS GO1 SiGe channel device and these are:

- $WF_{eff}$  and EOT extraction (Fig. 5.29) using  $N(Q_{tot})$  versus  $V_{GS}$  characteristic.
- $X_{eff}$  and  $t_{box}$  extraction (Fig. 5.37) using  $N(Q_{tot})$  versus  $V_{BS}$  characteristic.
- $EOT=t_{box}+t_{ch}+t_{fox}$  and  $WF_{eff}$  extraction using  $C_{bg}$  versus  $V_{GB}$  characteristic (Fig. 5.18).

The extraction methodology is based on the universal curve  $E_f(Q_{tot})-E_c(Q_{tot})$  previously introduced for the Silicon material. It's obvious that this curve is different in case of SiGe material (blue curve in Fig. 5.40 to be compared with red curve corresponding to Si material). This new curve (holes) will be used to carry out properly the extraction of the different technological parameters of the P-MOS GO1 SiGe channel device. As we previously confirmed such characteristic depends only on the semiconductor material (SiGe versus Si material). We remind that a proper value of the in-plane effective mass for SiGe material takes into account the variation of the valence band energy ( $\Delta E_v$ ) with respect to Si material.

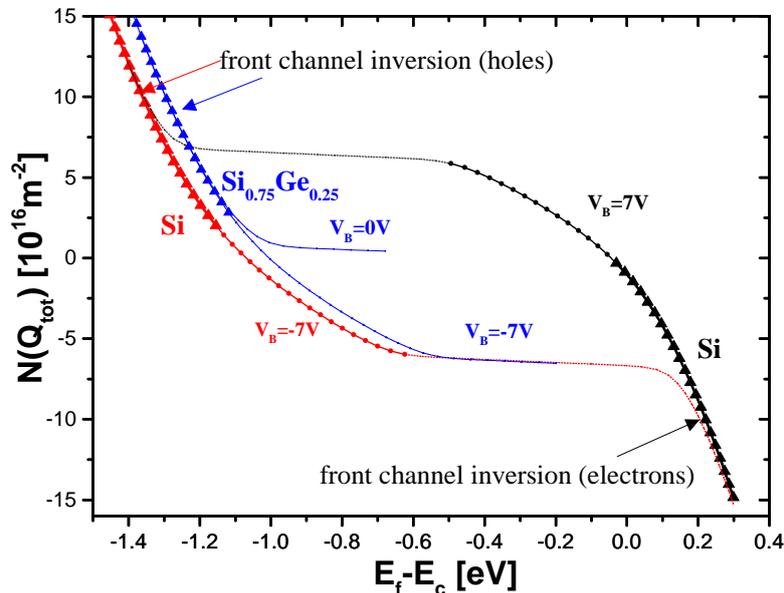


Figure 5.40:  $N(Q_{tot}(E_f-E_c))$  characteristics for Si and SiGe material.

Once we take into account the proper universal characteristics we can extract  $WF_{eff}$ , EOT,  $X_{eff}$  and  $t_{box}$  using equations 5.30 and 5.34, as carried out for the previous P-MOS GO2 Si channel device. As previously said the first extraction

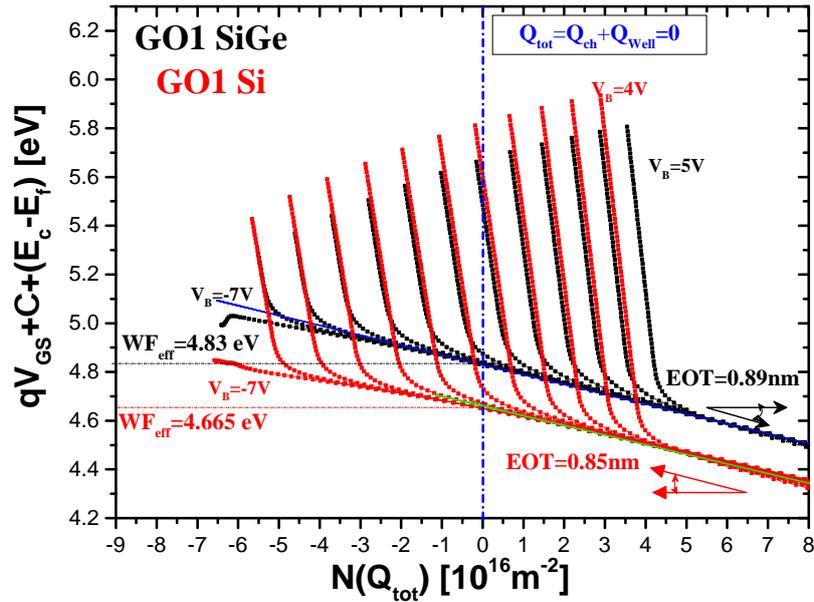


Figure 5.41:  $WF_{eff}$  and EOT extraction for two GO1 devices featuring a Si channel (in red) and SiGe channel (in black).

is carried out using  $N(Q_{tot})$  as a function of  $V_{GS}$  characteristics. In Fig. 5.41, we report the extraction of  $WF_{eff}$  and EOT for GO1 Si channel device (red lines) and GO1 SiGe channel device (black lines). A value of 4.665eV and 0.85nm is found for the GO1 Si channel device whereas for GO2 SiGe channel device a value of 4.83eV and 0.89nm are obtained. We remember that the electron affinities are respectively 4.2 eV for Si and 4.115eV for  $Si_{0.75}Ge_{0.25}$ . The results are similar to the ones obtained with the first numerical methodology (look chapter 3). The difference of 165mV between the two extracted  $WF_{eff}$  is primarily explained by the presence of the dipoles or fixed charges at the front interface between front-oxide/channel in case of SiGe channel device. This extraction is carried out on  $N(Q_{tot})$  as a function of  $V_{GS}$ . Therefore, only the impact on the front interface has been observed (Fig. 5.45). The second step is the extraction of the effective electron affinity during back operation. Indeed we respectively report in Figs. 5.42 and 5.43 results for the P-MOS G Si channel and P-MOS GO2 SiGe channel. We notice that the buried oxide thickness value of 20.25nm is the same for both the devices whereas the effective electron affinity is different. Indeed we have 4.2eV for Si channel device and 4.37eV for SiGe channel device. A difference of  $\Delta X_{eff}=170mV$  is found and it is similar to the previous shift  $\Delta WF_{eff}=165mV$  obtained during the extraction of the effective work function. This difference as for the front oxide can be deduced as impact of an equivalent dipole or fixed charges located at the channel/back-oxide interface. This extraction is carried out on  $N(Q_{tot})$  as a function of  $V_{BS}$  characteristics obtained from the characteristics of

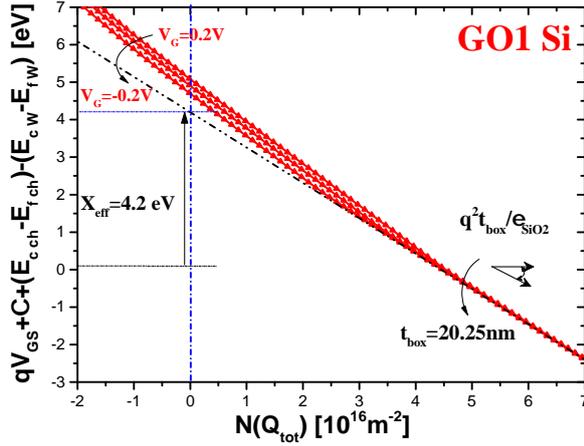


Figure 5.42:  $X_{\text{eff}}$  and  $t_{\text{box}}$  extraction for a P-MOS GO1 device featuring a Si-channel and N-type well from  $V_G=0.2\text{V}$  to  $-0.2\text{V}$ .

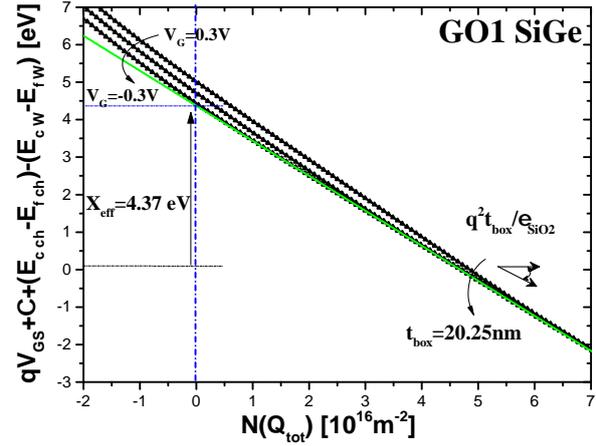


Figure 5.43:  $X_{\text{eff}}$  and  $t_{\text{box}}$  extraction for a P-MOS GO1 device featuring a SiGe-channel and N-type well from  $V_G=0.3\text{V}$  to  $-0.3\text{V}$ .

Fig. 5.18. Therefore only the impact of the back interface has to be observed (Fig. 5.45) on the extraction results. We find that the differences among the extracted effective work functions and electron affinities are mostly the same. Indeed we have:

$$WF_{\text{eff SiGe}} - WF_{\text{eff Si}} = X_{\text{eff SiGe}} - X_{\text{eff Si}} \sim 170\text{mV} \quad (5.37)$$

Until now we have found the same difference by comparing the extraction results between these two devices and we have related this shift to the possible presence of the same dipole or fixed charges at both the channel interfaces (back and front) due to the SiGe material. In order to understand which is the primary element (dipoles or fixed charges) that induces a shift on  $WF_{\text{eff}}$  and  $X_{\text{eff}}$  a last extraction has to be carried out using  $C_{\text{bg}}(V_{\text{GB}})$  characteristic. Indeed the measurement of the well flat band condition ( $WF_{\text{eff}}$ ) on the  $C_{\text{bg}}(V_{\text{GB}})$  characteristic for the two different Si and SiGe channel devices gives us a supplementary information compared to the previous extractions. We remind that the value of  $WF_{\text{eff}}$  extracted at well flat band condition includes all the effects induced by the presence of fixed charges and dipoles across the FDSOI stack dielectrics which are the front and back oxides and the channel (including the two channel interfaces). This extraction is carried out on  $C_{\text{bg}}$  versus of  $V_{\text{GB}}$  characteristics. Therefore, in case of a same dipole at the front and back interfaces, no impact of these dipoles has to be observed (Fig. 5.45) on the extracted value of  $WF_{\text{eff}}$  since their effects are opposite. But most importantly, this couldn't happen if we were supposing the same fixed charges, instead of dipoles, at the front and back channel interfaces induced by SiGe material their electrostatic effects would

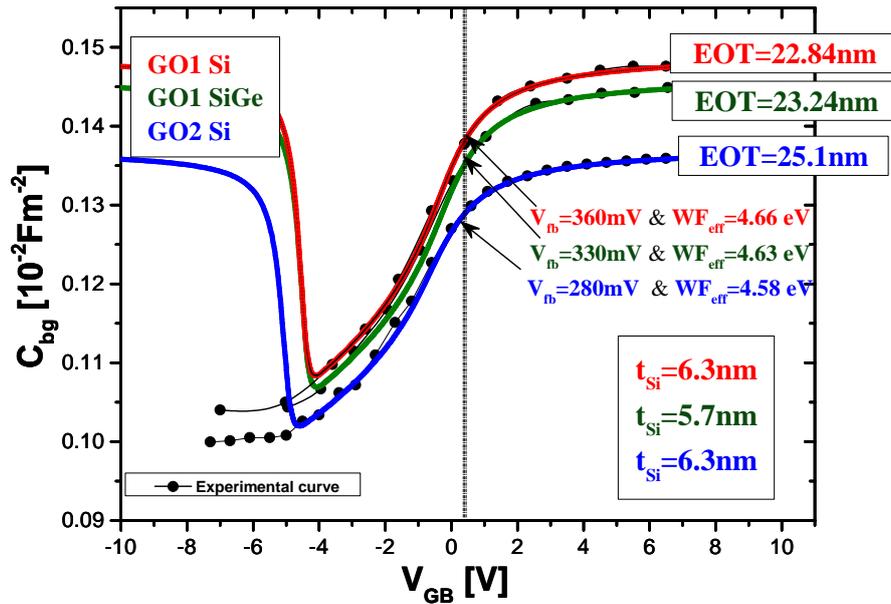


Figure 5.44:  $C_{bg}$  as a function of  $V_{GB}$  simulated and experimental characteristics for two GO1 devices featuring a Si and SiGe channel and one GO2 device with Si channel.

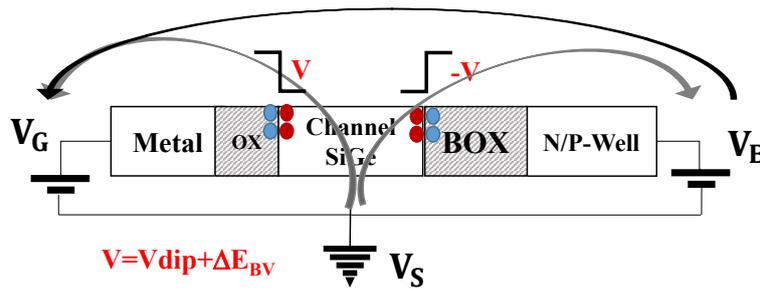


Figure 5.45: Scheme of FDSOI SiGe with dipoles and shift of valance band.

accumulate. Moreover, since the two compared devices have the same stack except for channel material (Si and SiGe), the effective work function extracted using  $C_{bg}$  versus of  $V_{GB}$  has to be similar. As reported in Fig. 5.44, where  $C_{bg}$  versus  $V_{GB}$  characteristics are shown, values of the effective work function of 4.66eV and 4.63eV are respectively obtained for the P-MOS GO1 Si channel (red) and P-MOS GO1 SiGe channel device (Green) which are really similar. Moreover, a direct extraction of the channel thickness is carried out for these two devices leading to a value of 6.3nm for SiGe channel device and 5.7nm for Si channel device.

The different extraction results are summarized in TABLE 5.1. These results leads us to validate the hypothesis of the presence of the dipole at the front and back channel interfaces with SiGe channel and to reject any influence of fixed charges at the interface. The reasons are twofold:

Table 5.1: Extraction result using the three previous methodologies.

DEVICE	1 <sup>st</sup> Methodology $WF_{eff}$	2 <sup>nd</sup> Methodology $X_{eff}$	3 <sup>rd</sup> Methodology $WF_{eff}$
P-MOS GO1 channel Si	4.665eV	4.2eV	4.66eV
P-MOS GO1 channel SiGe	4.83eV	4.37eV	4.63eV

- Firstly, the shifts  $\Delta WF_{eff}$  and  $\Delta X_{eff}$  are found to be the same at the front and back Gate stack. This confirms the effect at each SiGe/oxide interfaces.
- Secondly, the extraction of  $WF_{eff}$  at well flat band condition (3<sup>rd</sup> methodology) reveals that effects at the two interfaces counterbalance, meaning that the  $WF_{eff}$  shift is due to the dipole and not to charges.

The  $V_{th}$  shift of 340mV in case of  $C_{gc}$  characteristics in Fig. 5.38 has been justified by the presence of the dipole (165mV) and the energy valence band shift with respect to the Si material. More tedious is the relation between the dipole and valence energy shift with the  $V_{th}$  shift of 3.4V observed for the  $C_{bc}$  characteristics in Fig. 5.39. This larger shift is due to two specific reasons:

- The direct shift induced by the back channel interface dipole and valence band energy shift ( $\Delta V=340mV$ ).
- The effect of modulation induced by front channel interface dipole and valence band energy shift ( $\Delta V=340mV$ ). Indeed as reported in Fig. 5.39 a front bias  $V_G=-\Delta V$  applied at the  $C_{gc}$  characteristic of P-MOS Si channel device (red dashed line) reduces the  $V_{th}$  shift with respect to the P-MOS SiGe channel device up to 340mV which is directly related to the back channel interface  $\Delta V$ .

Therefore, the  $V_{th}$  shift seen on  $C_{gc}$  and  $C_{bc}$  can only be explained by two similar abrupt voltage drops at SiGe interface (Fig. 5.45). The Valence band shift related to SiGe band structure explains only one half of the  $V_{th}$  shift, implying the existence of an additional dipole at SiGe/SiO<sub>2</sub> interface.

## 5.4 Conclusion

In this chapter, we have presented for the first time a new extraction methodology for fully depleted FDSOI transistors which is fast and reliable. This methodology authorizes the extraction of the effective work function  $W_{\text{eff}}$  at the front interface, all the FDSOI stack thicknesses ( $t_{\text{fox}}$ ,  $t_{\text{ch}}$  and  $t_{\text{box}}$ ) and the effective electron affinity  $X_{\text{eff}}$  at back interface.

It has been demonstrated that this methodology overcomes the limits of the two previous methodologies since it is complete, fast with a minimal computational cost.

In order to carry out these extractions, a new capacitance measurement  $C_{\text{bg}}$  has been presented. The reconstruction of the entire FDSOI bulk regime capacitance has been successfully demonstrated from which an accurate identification of the well flat band has been achieved using standard extraction techniques used for the traditional bulk transistors.

The identification of well flat band condition on the  $C_{\text{bg}}(V_{\text{GB}})$  allows us to calculate for the first time the well charge in the FDSOI transistors and consequently the total charge seen at the front interface. Thus, the FDSOI electrostatic condition is perfectly known from these measurements.

Two universal behaviors which are respectively  $N(Q_{\text{tot}})(V_{\text{GS}})=N(Q_{\text{ch}}+Q_{\text{w}})(V_{\text{GS}})$  and  $N(Q_{\text{tot}})(V_{\text{BS}})=N(Q_{\text{ch}}+Q_{\text{m}})(V_{\text{BS}})$  are reported for the first time. These characteristics show a universal dependence between the total charge and the applied voltage and are used for the extraction of the technological parameters of the FDSOI stack. Moreover, two flat band conditions have been identified for the first time: the front flat band  $V_{\text{fb},f}$  and the back flat band  $V_{\text{fb},b}$  conditions.

Numerical simulations have been performed for different transistors. It has been demonstrated that a universal law  $E_{\text{f}}(N(Q_{\text{tot}}))-E_{\text{v}}(N(Q_{\text{tot}}))$  for electrons and holes is observed independently of the channel thickness (the only limit is :  $t_{\text{ch}}>3\text{nm}$ ), buried oxide thickness, channel and well doping level and type and transistor type (FDSOI or BULK). Therefore, the relationship between the total charge seen at the dielectric-semiconductor interface and the difference between the Fermi and conduction Energy levels depends only the physical parameters of the simulated semiconductor where inversions of electrons and holes occur.

We have shown that using these universal laws and the experimental relationship  $N(Q_{tot})(V_{GS})$  or  $N(Q_{tot})(V_{BS})$ , we can extract  $WF_{eff}$ , EOT (or  $t_{fox}$ ) and  $X_{eff}$  and  $t_{box}$ .

Finally, the hypothesis of the presence of the dipole (170mV) with SiGe channel at the back and front channel interface made to account of observed experimental  $V_{th}$  shift(340mV) between the  $C_{gc}$  characteristics has been validated. This has been achieved through the analysis of extraction results using the methodology presented in this chapter. Indeed whereas the same shift is found at the front gate ( $\Delta WF_{eff}=165mV$ ) and back gate ( $\Delta X_{eff}=165mV$ ) with respect to the Si channel device no shift is observed on the  $WF_{eff}$  extraction at the well flat band condition since the dipoles effects at the front and back channel interfaces is opposite. This validate the previous hypothesis proposed by A. Soussou et al [19].

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# Conclusion and Perspectives

As described in the previous Chapters, for the microelectronic industry involved in the development of advanced CMOS technology for MOS (metal/Oxide/Semiconductor) transistors, the extraction of EOT (Equivalent oxide thickness) and  $WF_{\text{eff}}$  (effective work function) of the metal gate stack is important. These two parameters are fundamental in order to compare different technologies featuring specific architectures or process technology (fabrication procedure). Moreover, EOT and  $WF_{\text{eff}}$  extraction is fundamental due to their impacts on the transistor electrical performances and still important in FDSOI technology. It is in this context that we felt essential to propose new electrical characterization methodologies, based on C-V measurements which can extract in reliable and fast way the effective work function and the equivalent oxide thickness for the fully depleted SOI technology.

Indeed as reported in chapter 1, we have reminded that EOT and  $WF_{\text{eff}}$  extraction from the C-V measurements is a well known technique in the state of the art for the standard bulk technology. For a long time, they proposed analytical methods for the EOT and  $V_{\text{fb}}$  extraction, from the typical points of the C-V characteristic (maximum and minimum) or from its derivative. Unfortunately, these methodologies are no longer adequate for the FDSOI technology. The issue is related to the absence of the flat band voltage  $V_{\text{fb}}$  and the associated depletion-accumulation region on its Capacitance characteristic. The only observed capacitance is the inversion or  $C_{\text{gc}}$  characteristic from which only the identification of  $V_{\text{th}}$  is possible. Despite the few attempts in the state of the art to extract EOT and  $WF_{\text{eff}}$  from  $C_{\text{gc}}$  characteristic ( $V_{\text{th}}$ ), the complex dependence of  $C_{\text{gc}}$  characteristic with the FDSOI stack parameters makes this extraction tedious and not reliable.

The huge structural and electrical capacitance behavior discrepancies between FDSOI and bulk transistors are evidenced in chapter 2. The extraction of EOT and  $WF_{\text{eff}}$  for bulk transistors has been carried out by using the typical capacitance and voltage relations. For this reason an introduction of the FDSOI technology in terms of geometric structure and calculation of the electrostatic relations and

the capacitance relationships have been carried out. These are fundamentals in order to carry out the extraction of the FDSOI technological parameters. Moreover, a part of the chapter has been dedicated to the numerical simulation of the FDSOI stack. These simulations are based on PS formalism within the effective mass approximation (EMA). Indeed, this part of the chapter shows specifically how to calculate the band diagrams, the charge distribution and the electrostatic profile of a specific FDSOI transistor under specific voltage conditions which are fundamental for the FDSOI electrostatic comprehension and for the analysis carried out in the chapters 3, 4 and 5.

In chapter 3, we have presented the first extraction methodology, the numerical methodology, based on a specific algorithm in order to extract accurately EOT and  $WF_{\text{eff}}$ . The numerical extraction was carried out on 15 different devices of same wafer which made the work original with respect to any previous work. We have seen that the numerical extraction methodology is based on 4 main steps that are: (1) identification of front oxide EOT, (2) identification of the buried oxide thickness, (3) identification of the channel thickness and (4) extraction of  $WF_{\text{eff}}$ . Each step of the proposed methodology required a fitting procedure between the experimental C-V characteristic and quantum numerical simulation in order to extract the relative physical parameter. Moreover, in order to carry out the extraction two specific capacitances measurements were used: the typical gate-to-channel  $C_{\text{gc}}$  characteristic and a new back-gate-to-channel  $C_{\text{bc}}$  capacitance. This new capacitance measurement results from the variations of the channel charge induced by the small signal applied on back gate contact potential.  $C_{\text{bc}}$  capacitance has been presented in this chapter for the first time. A first identification of the various FDSOI stack thicknesses was necessary in order to obtain the proper  $WF_{\text{eff}}$  value of these 15 different devices, N-MOS and P-MOS, on which we had various channel materials (Si or SiGe), Gate metal type (P with sacrificial gate process or N with standard process), gate dielectric (GO1  $\simeq$  1nm and GO2  $\simeq$  3nm) and well type (N or P) for ground plane. The results obtained with the numerical extraction allowed us to observe the impacts of the different modules on the technological parameters. A  $WF_{\text{eff}}$  shift of 100mV for GO1 devices and 45mV for GO2 devices due to the sacrificial Gate process (P metal gate) with respect to the standard process. The buried oxide thickness has been found independent of any process modules. The channel thickness has been found to be dependent of channel material (1 nm thicker in case of SiGe channel with respect to Si channel), on the dielectric type (1 nm thicker in case of GO2 ( $\simeq$  3nm) dielectric devices with respect to GO1 ( $\simeq$  1nm) dielectric devices).

Finally,  $WF_{\text{eff}}$  has been found to depend on the channel material. Indeed an observed shift of  $\Delta WF_{\text{eff}}=150\text{mV}$  between SiGe and Si GO1 channel devices due to a hypothesized dipole located at the front-oxide/channel interface induced by SiGe. Despite its precise and complete extraction, the numerical methodology lacks in terms of time and computation cost (complicated numerical procedure) which are fundamental in order to carry fast statistical analysis.

It is for this reason that an alternative approach has been proposed in Chapter 4 with respect to the numerical methodology: the analytical extraction methodology. This extraction methodology is based on linear regression which exploits the linearity of  $Q_{\text{ch inv}}/C_{\text{gc}}$  and  $Q_{\text{ch inv}}/C_{\text{bc}}$  versus  $Q_{\text{ch inv}}$  where  $Q_{\text{ch inv}}$  is the channel inversion charge calculated for the integral of  $C_{\text{gc}}$  and  $C_{\text{bc}}$  characteristics. This approach, presented for the first time, allowed us to directly and analytically extract all the FDSOI stack thicknesses ( $t_{\text{fox}}$ ,  $t_{\text{ch}}$  and  $t_{\text{box}}$ ). Indeed, this is carried out by simply calculating the slopes of the linear region of  $Q_{\text{ch inv}}/C_{\text{gc}}$  and  $Q_{\text{ch inv}}/C_{\text{bc}}$  versus  $Q_{\text{ch inv}}$  characteristics. The analytical methodology has been validated through comparison with the numerical simulations results obtained in chapter 3. We have evidenced the simplicity and rapidity of this analytical methodology compared to the numerical methodology but also that  $WF_{\text{eff}}$  cannot be extracted. Since the classical Boltzmann formalism has been used to carry out the extraction of the various FDSOI stack thicknesses and doesn't take into account quantum effects of the channel charge, a correction, in terms of dark space, on the extracted classical thickness values was necessary. For the correction of the FDSOI stack thicknesses two constant dark space values were respectively considered, in terms of equivalent  $\text{SiO}_2$  thickness, of 0.3 nm for the front and back oxide thicknesses and 0.5nm for the channel thickness. This assumption of a constant dark space thickness (independent of the channel charge) and the impossibility to extract  $WF_{\text{eff}}$  have pushed us to look for alternative solutions.

Indeed, in Chapter 5, we evidenced that the two previous methodologies are not adequate for a fast and complete characterization of the FDSOI transistors because either the extraction methodology is too slow and complicate (numerical of chapter 3) or it is not complete (analytical of chapter 4). In order to overcome both the limits of the previous methodologies, an innovative extraction methodology (which is fast and reliable) for fully depleted FDSOI transistors is presented in this chapter. We have seen that in order to carry out this extraction, all the capacitances had to be measured on the FDSOI transistor. These capacitances are the front capacitances, which are the previous gate-to-channel  $C_{\text{gc}}$  and the classical gate-to-bulk  $C_{\text{gb}}$  capacitance and the back capacitances which

are the previous back-gate-to-channel  $C_{bc}$  (presented in previous chapter) and the new bulk-to-gate  $C_{bg}$  capacitance which is presented for the first time in this chapter. We have also shown that from this particular  $C_{bg}$  capacitance characteristic, it's possible to identify the well flat band condition and thus the first effective work function ( $WF_{eff}$ ) which includes all the impacts of the fixed charges and dipoles across the whole FDSOI stack. Once the well flat band is extracted, we have shown that the well charge (also reported for the first time) can be easily calculated by integrating  $C_{bg}$  capacitance. Moreover, from the calculated well charge, we can easily obtain the total charge which leads to a perfect knowledge of the electrostatic condition of the FDSOI transistor since the channel charge is easily calculated from the integral of  $C_{gc}$  or  $C_{bc}$  capacitances. The experimental trend of the total charge as a function of  $V_{GS}$  characteristics at different  $V_B$  showed a general behavior for the specific FDSOI transistor during the front and back channel inversion condition. But more importantly, this general electrostatic behavior of the specific FDSOI led us to discovery for the first time a universal law  $E_f(N(Q_{tot})) - E_v(N(Q_{tot}))$  which occurs at strong front channel inversion (holes and electrons) and which is dependent only of the simulated semiconductor physical parameters. Moreover, we have shown that using these universal laws and the experimental relationships  $N(Q_{tot})(V_{GS})$  or  $N(Q_{tot})(V_{BS})$  we can extract  $WF_{eff}$ , EOT (or  $t_{fox}$ ) and  $X_{eff}$  and  $t_{box}$  which leads to a complete characterization of the FDSOI stack.  $WF_{eff}$ , EOT (or  $t_{fox}$ ) are respectively extracted from the intercept at y-axis and the slope of the  $qV_{GS} + X - (E_f - E_c)$  as a function of  $N(Q_{tot})$  characteristic.  $X_{eff}$  and  $t_{box}$  are also extracted from the intercept at y-axis and the slope of the  $qV_{BS} + X_{ch} + (E_{fW}(-Q_{tot}) - E_{cW}(-Q_{tot})) - (E_{fch}(Q_{tot}) - E_{cch}(Q_{tot}))$  as a function of  $N(Q_{tot}) = N(Q_{ch} + Q_m)$  characteristic. Finally, the precise and complete (front and back) extraction of the technological parameters of the FDSOI allows us to prove the existence of a same dipole ( $\Delta V \simeq 150-170mV$ ) at the front and back channel interfaces between SiGe and its oxide.

We can conclude that an accurate, robust, fast and complete extraction methodology has been successfully validate and develop in chapter 5 for the fully depleted FDSOI transistors which will be fundamental for the technological Optimization. Moreover, the discover of a universal law which depends only on the simulated semiconductor material will certainly have a drastic impact for the future research and specifically in the field of reliability and compact modelling.

## Future works and recommendations

Hereafter, we suggest some works that can be investigated in a near future:

- Investigation of the impact of the Germanium concentration on the universal curve.
- Investigation of the behaviour of the universal curve under the channel thickness limit ( $t_{\text{ch}} < 4\text{nm}$ ) within the K-P formalism which takes properly into account the effective mass variation and the variation of the distribution of the band energies for Silicon and SiGe materials. Comparison of the result within K-P formalism with the result obtained within EMA formalism.
- Development of an automatic tool for statistical extraction of  $WF_{\text{eff}}$ ,  $t_{\text{fox}}$ ,  $t_{\text{box}}$ ,  $t_{\text{ch}}$ ,  $N_{\text{Well}}$  and  $X_{\text{eff}}$ . based on the previous extraction methodology (chapter 5).
- Investigation of the extraction precision of well flat band condition on the FDSOI bulk regime capacitance characteristic ( $C_{\text{bg}}(V_{\text{GB}})$ ) and of the various FDSOI stack thicknesses ( $t_{\text{fox}}$ ,  $t_{\text{ch}}$  and  $t_{\text{box}}$ ) on the  $C_{\text{cg}}$ ,  $C_{\text{bc}}$  and  $C_{\text{bg}}$  capacitance characteristics. Moreover, analysis of the variability of the previous FDSOI stack thicknesses,  $WF_{\text{eff}}$  and  $X_{\text{eff}}$  extraction on all the capacitance characteristics at different front ( $V_{\text{G}}$ ) and back  $V_{\text{B}}$  biases.
- Adaption of the extraction methodology to new materials (III-V). This means, trying to identify the universal law by proper identification of the physical parameters (effective mass, gap energy ...) for the III-V group materials with respect to well-known Si and SiGe materials.
- Investigation of the use of the universal law in the compact modelling and reliability research fields.



## Résumé

Comme décrit dans les chapitres précédents, l'extraction de l'EOT (épaisseur équivalent d'oxyde) et  $WF_{\text{eff}}$  (travail de sortie effective) de la grille métallique est fondamental pour l'industrie de la micro-électronique impliqué dans le développement de la technologie CMOS avancée pour les transistors MOS (Métal / Oxyde / Semi-conducteur). Ces deux paramètres sont fondamentaux afin de comparer technologies caractérisé par différents architectures et différents procédures de fabrication. En outre, l'extraction de EOT et  $WF_{\text{eff}}$  est fondamentale en raison de leur impacts sur les performances électriques du transistor MOS et encore important pour la technologie FDSOI. Il est dans ce contexte que nous sentions essentielle de proposer de nouvelles méthodes de caractérisation électrique, à partir des mesures C-V pour extraire de manière fiable et rapide le travail de sortie effective et l'épaisseur équivalent d'oxyde pour la technologie FDSOI.

En effet, comme indiqué dans le chapitre 1, nous avons rappelé que l'extraction de l'EOT et  $WF_{\text{eff}}$  à partir des mesures C-V est une technique bien connue dans l'état de l'art pour la technologie bulk standard. Pendant longtemps, ils ont proposé d'analyse des procédés d'extraction de l'EOT et  $V_{\text{fb}}$ , à partir des points caractéristiques de la caractéristique C-V (maximum et minimum) ou de son dérivé. Malheureusement, ces méthodes ne suffisent plus pour la technologie FDSOI. Le problème est lié à l'absence de la tension de bande plate  $V_{\text{fb}}$  et la région associé de déplétion et accumulation sur la caractéristique capacitive. La seule mesure capacitive observée est l'inversion connu autre mode comme la caractéristique grille-canal ( $C_{\text{gc}}$ ) sur la quelle l'identification de la tension de seuil ( $V_{\text{th}}$ ) est possible. Malgré quelques tentatives dans l'état de l'art, l'extraction de l'EOT et  $WF_{\text{eff}}$  sur la caractéristique  $C_{\text{gc}}$  ( $V_{\text{th}}$ ) est complexe en raison de la dépendance aussi complexe entre la caractéristique  $C_{\text{gc}}$  et les paramètres électriques de l'empilement de transistor FDSOI que rend cette extraction fastidieux et surtout pas fiable.

Les énormes écarts structuraux et du comportement électrique capacitive entre FDSOI et le transistor bulk traditionnelle sont évidence au chapitre

2. En effet, l'extraction de EOT et  $WF_{\text{eff}}$  pour les transistors bulk a été toujours réalisé en utilisant les typique relations de capacité et tension non plus compatible avec la technologie FDSOI. Pour cette raison, une introduction de la technologie FDSOI en termes de structure géométrique et le calcul des relations capacitives et relations électrostatique sont effectuées. Ce sont fondamentaux afin d'effectuer l'extraction des paramètres technologiques de FDSOI. En outre, une partie du chapitre a été consacré à la simulation numérique de l'empilement FDSOI. Ces simulations sont basées sur le formalisme Poisson-Schrödinger dans l'approximation de masse effective (EMA). Cette partie du chapitre montre précisément comment calculer les diagrammes de bande, la répartition de charge et le profil électrostatique des transistor FDSOI dans des conditions de tension spécifiques qui sont fondamentales pour la compréhension électrostatique de transistor et aussi pour l'analyse réalisée dans les chapitres 3, 4 et 5.

Du coup dans le chapitre 3, nous avons présenté la première méthode d'extraction, la méthode numérique, basée sur un algorithme spécifique afin d'extraire EOT et  $WF_{\text{eff}}$  avec précision. L'extraction numérique a été réalisée sur 15 dispositifs différents ce que rend ce travail original pour rapport aux autres précédent travaux. Le méthode d'extraction numérique est basée sur quatre étapes principales qui sont: (1) identification de l'épaisseur d'oxyde de la grille face avant, (2) l'identification de l'épaisseur d'oxyde enterrée (de la grille face arrière) (3) l'identification de l'épaisseur de canal et (4) l'extraction de  $WF_{\text{eff}}$ . Chaque étape de la méthodologie proposée est basé sur des procédures d'ajustement entre la caractéristique C-V expérimentale et la simulation numérique quantique afin d'extraire le paramètre physique correspondant. Afin de réaliser l'extraction, deux spécifiques mesures capacitives ont été utilisées: la typique caractéristique capacitive grille-canal  $C_{\text{gc}}$  et une nouvelle capacité grille-arrière-canal  $C_{\text{bc}}$ . Cette nouvelle mesure capacitive est le résultat à partir des variations de la charge de canal provoquée par le petit signal de tension appliqué sur le contact de grille face arrière. Cette capacité  $C_{\text{bc}}$  a été présentée dans ce chapitre pour la première fois. Cette mesure et  $C_{\text{gc}}$  sont utilisé pour identifier les différentes épaisseurs de l'empilement de FDSOI qui sont nécessaire afin d'obtenir la valeur correcte de  $WF_{\text{eff}}$  de ce 15 différents dispositifs, N-MOS et P-MOS, sur lesquels on a différents matériaux de canaux (Si ou SiGe), type de métal de grille (P avec le processus de grille sacrificielle ou N avec le processus standard), type de diélectrique de grille ( $GO1=1\text{nm}$  et  $GO2=3\text{nm}$ ) et enfin le type de well (N ou P). Les résultats obtenus par l'extraction numérique nous

a permis d'observer les impacts des différents modules sur les paramètres technologiques. Un décalage de travail de sorti effective de 45mV et 100mV est observé pour les deux dispositifs GO1 et GO2 du processus de grille sacrificielle (métal P) par rapport au module standard. L'épaisseur d'oxyde enterrée est trouvée indépendante de tous les modules de processus. L'épaisseur du canal est trouvée être dépendante du matériau de canal (1 nm plus épaisse dans le cas du canal SiGe par rapport au canal Si), du type de diélectrique (1 nm plus épaisse en cas des dispositifs avec diélectriques GO2 (« 3 nm) par rapport à GO1 (« 1 nm)). Enfin,  $WF_{\text{eff}}$  a été trouvé dépendre du matériau du canal. En effet, un décalage observé de  $\Delta WF_{\text{eff}} = 150\text{mV}$  entre SiGe et Si canal pour les deux dispositifs GO1 est expliqué par la présence de un dipôle hypothétique situé à l'interface avant oxyde/canal induite par le module SiGe. En dépit de son extraction précise et complète, la méthodologie numérique manque de rapidité et facilite en termes de coûts de temps et de calcul (procédures numériques complexes) qui sont fondamentales pour mener une analyse statistique rapide.

Il est pour cette raison que on a proposé une autre approche d'extraction dans le chapitre 4 par rapport à la méthodologie numérique: la méthode d'extraction analytique. Cette méthode d'extraction est basée sur une simple régression linéaire qui exploite la linéarité de  $Q_{\text{ch inv}}/C_{\text{gc}}$  et  $Q_{\text{ch inv}}/C_{\text{bc}}$  en fonction de  $Q_{\text{ch inv}}$  où  $Q_{\text{ch inv}}$  est la charge de canal d'inversion calculée en intégrant les caractéristiques de  $C_{\text{gc}}$  et de  $C_{\text{bc}}$ . Cette approche, présentée pour le premier fois, nous a permis d'extraire directement et analytiquement toutes les épaisseurs de l'empilement FDSOI ( $t_{\text{fox}}$ ,  $t_{\text{ch}}$  et  $t_{\text{box}}$ ). Cela est fait simplement en calculant les pentes de la région linéaire de les caractéristiques  $Q_{\text{ch inv}}/C_{\text{gc}}$  et  $Q_{\text{ch inv}}/C_{\text{bc}}$  en fonction de de  $Q_{\text{ch inv}}$ . La méthode d'analyse a été validée par comparaison avec les résultats des simulations numériques obtenus dans le chapitre 3. Nous avons mis en évidence la simplicité et la rapidité de cette méthode d'analyse par rapport à la méthodologie numérique, mais aussi que  $WF_{\text{eff}}$  ne peut pas être extrait. En outre, depuis le formalisme de Boltzmann classique est utilisé pour faire l'extraction des différentes épaisseurs de l'empilement FDSOI, cette méthodologie analytique ne prend pas en compte des effets quantiques de la charge de canal, et comme conséquence une correction en termes de dark space, sur les valeurs d'épaisseur classique extraites est nécessaire. Pour la correction des épaisseurs de l'empilement FDSOI deux valeurs de dark space constants ont été respectivement considérée en termes d'épaisseur équivalente SiO<sub>2</sub> : 0.3 nm pour l'épaisseur d'oxyde face avant et arrière (enterrée) et 0.5 nm pour l'épaisseur du canal. Cette hypothèse des valeurs des dark space constant (charge

indépendante du canal) et l'impossibilité d'extraire  $WF_{\text{eff}}$  nous ont poussés à chercher des solutions alternatives.

Dans le chapitre 5, nous mettons en évidence que les deux méthodes précédentes ne sont pas suffisantes pour une caractérisation rapide et complète des transistors FDSOI parce que soit la méthode d'extraction est trop lent et compliqué (numérique du chapitre 3) soit ce n'est pas complète (analytique chapitre 4). Afin de surmonter les deux limites des méthodes précédentes, une méthode d'extraction innovante (qui est rapide, fiable et complet) pour le transistor FDSOI est présentée dans ce chapitre. Nous avons vu que pour réaliser cette extraction, toutes les capacités devaient être mesurées sur les transistors FDSOI. Ces capacités sont les capacitances face avant, la précédente capacité classique grille-canal  $C_{gc}$  (présentée dans le chapitre précédent) et la capacité grille-substrat  $C_{gb}$ , et les capacités face-arrière, la précédente capacité grille-arrière-canal  $C_{bc}$  (présentée dans le chapitre précédent pour la première fois) et la nouvelle capacité substrat-grille  $C_{bg}$  qui est présenté pour la première fois dans ce chapitre. Nous avons également montré que à partir de cette caractéristique capacitive particulière,  $C_{bg}$ , il est possible d'identifier la condition de bande plate de substrat et donc déterminer le travail de sorti effective ( $WF_{\text{eff}}$ ) qui prends en compte de tous les impacts des charges fixes et dipôles sur l'ensemble de l'empilement FDSOI.

Une fois que la bande plate est extraite, nous avons bien montré que la charge du substrat (également montre pour la première fois) peut être facilement calculée en intégrant la capacité  $C_{bg}$ . En autre, depuis la charge de substrat calculé, on peut facilement obtenir la charge totale qui conduit à une parfaite connaissance de l'état électrostatique des transistors FDSOI puisque la charge de canal est aisément calculable en intégrant les capacités  $C_{gc}$  ou  $C_{bc}$ . La caractéristique expérimentale de la charge totale en fonction des  $V_{GS}$  à différents  $V_B$  montre un comportement général pour un transistor FDSOI spécifique une fois que la condition d'inversion de canal face avant et face arrière est satisfait. Mais plus important encore, ce comportement électrostatique général nous a amenés à découvrir pour la première fois une loi universelle  $E_f(N(Q_{\text{tot}})) - E_v(N(Q_{\text{tot}}))$  qui se produit à forte inversion des canaux avant ou arrière (trous et électrons) et qui ne dépend que des paramètres physiques simulés de semi-conducteurs du canal. En autre, nous avons montré que en utilisant ces lois universelles (trous et électrons) et les relations expérimentales  $N(Q_{\text{tot}})(V_{GS})$  ou  $N(Q_{\text{tot}})(V_{BS})$ , nous pouvons extraire  $WF_{\text{eff}}$ , EOT (ou  $t_{\text{fox}}$ ) pour la grille face avant et  $X_{\text{eff}}$  et  $t_{\text{box}}$  pour la grille face arrière. Ce qui conduit à une caractérisation complète

de l'empilement FDSOI.  $WF_{\text{eff}}$ , EOT (ou  $t_{\text{fox}}$ ) respectivement sont extraits à partir de l'intersection à l'axe y et la pente de la caractéristique  $qV_{\text{GS}} + X - (E_f - E_c)$  en fonction de  $N(Q_{\text{tot}})$ . Equivalamment  $X_{\text{eff}}$  (affinité électronique effective) et  $t_{\text{box}}$  sont extraits de l'ordonnée à l'origine à l'axe y et la pente de la caractéristique  $qV_{\text{BS}} + X_{\text{ch}} + (E_{\text{fW}}(-Q_{\text{tot}}) - X_{\text{cW}}(-Q_{\text{tot}})) - (E_{\text{fch}}(Q_{\text{tot}}) - E_{\text{cch}}(Q_{\text{tot}}))$  en tant que fonction de  $N(Q_{\text{tot}}) = N(Q_{\text{ch}} + Q_{\text{m}})$ . Enfin, la précise et complète (avant et arrière) extraction des paramètres technologiques du FDSOI nous permet de mettre en évidence l'existence d'un même dipôle (150-170mV) à l'avant et les interfaces de canal arrière entre SiGe et son oxyde. Nous pouvons conclure qu'une méthode d'extraction précise, robuste, rapide et complet a été validée avec succès et développer au chapitre 5 pour les transistors FDSOI qui sera fondamentale pour son optimisation technologique. De plus, la découverte d'une loi universelle qui ne dépend que du matériau semi-conducteur simulé aura certainement un impact considérable pour la recherche future et plus particulièrement dans le domaine de la fiabilité et de la modélisation de model compact.

### Les travaux futurs et recommandations

Ci-après, nous vous proposons quelques œuvres qui peuvent être étudiés dans un avenir proche:

- Analyse de l'impact de la concentration de germanium dans le canal sur la courbe universelle
- Etude du comportement des courbes universelles dans la limite d'épaisseur de canal ( $t_{\text{ch}} < 4$  nm). Dans le KP formalisme qui prend correctement en compte la variation de la masse effective et la variation de la distribution des énergies de bande pour les matériaux silicium et SiGe. Comparaison du résultat dans le formalisme KP avec le résultat obtenu dans le formalisme de l'EMA.
- Développement d'un outil automatique pour l'extraction statistique des  $WF_{\text{eff}}$ ,  $t_{\text{fox}}$ ,  $t_{\text{box}}$ ,  $t_{\text{ch}}$ , et  $X_{\text{eff}}$  puits N. sur la base de la méthode d'extraction précédente (chapitre 5).
- Etude de la précision d'extraction de bande plate sur la caractéristique capacitive  $C_{\text{bg}}$  ( $V_{\text{GB}}$ ) pendant la condition de déplétion total du canal de FDSOI et des différentes épaisseurs pile FDSOI ( $t_{\text{fox}}$ ,  $t_{\text{ch}}$  et  $t_{\text{box}}$ ) sur les caractéristiques capacitives  $C_{\text{gc}}$ ,  $C_{\text{bc}}$  and  $C_{\text{bg}}$ . En outre, l'analyse de la variabilité de des tous les précédentes épaisseurs de l'empilement FDSOI

et l'extraction  $WF_{\text{eff}}$  et  $X_{\text{eff}}$  sur toutes les caractéristiques capacitive a différentes polarisation a face avant ( $V_G$ ) et polarisation a face arrière ( $V_B$ ).

- adaptation de la méthode d'extraction pour les matériaux nouveaux (III-V). Cela signifie, en essayant de déterminer la loi universelle en identifiant les correcte paramètres physiques (masse effective, ban d'énergie) pour les matériaux du groupe III-V par rapport à des matériaux Si et SiGe bien connus.
- Enquête sur l'utilisation de la loi universelle dans les domaines de recherche de modélisation et de fiabilité.

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**Abstract :** Thin film technologies appear as reliable solutions for Nano electronics to go beyond bulk silicon technology limits, allowing lower power bias and thus energy harvesting. Indeed, Metal Oxide Semiconductors transistors (MOSFETs) with fully depleted substrate (FDSOI for 'Fully Depleted Silicon On Insulator') allow low static off-currents and variability improvement that enable the use of power supply biases lower than with bulk silicon, especially for SRAMs. From 14nm nodes, FDSOI generations are including SiGe channel, high-k dielectric and metal gate. All these new process modules required for technology improvement also significantly increase the complexity of the MOS devices electrical analysis and meanwhile its correlation with technology. This PhD study propose different novel methodologies for automatic and statistical parameter extraction of advanced FDSOI MOS gate stack. These methodologies are all based on capacitance versus voltage (C-V) characteristics, obtained for the capacitive coupling between metal gate, channel and back side. With such C-V characteristics, reliable methodologies are proposed, leading to the extractions of the equivalent oxide thicknesses (EOT), the effective work function of the FDSOI metal gate ( $W_{eff}$ ), but also other parameters such as channel and buried oxide thicknesses ( $t_{ch}$ ,  $t_{box}$ ) and an effective electron affinity of the substrate well ( $X_{eff}$ ) that includes all electrostatic effects in the buried oxide and at its interfaces. Moreover, quantum simulations are considered in order to validate the different methodologies. For experimental analysis, the study has considered coherence and complementarity of different test structures as well as the impact of back substrate polarization.

**Keywords :** MOSFET; FDSOI; Effective work function; Equivalent oxide thickness; buried oxide thickness; channel thickness; effective electron affinity; well flat band condition; front flat band condition; back flat band condition; threshold voltage.

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**Résumé :** Les technologies de films minces sur isolant apparaissent comme des solutions fiables pour la nano électronique Nano. Elles permettent de dépasser les limites des technologies sur substrat silicium massif, en autorisant de faibles tensions d'utilisation et un gain en énergie significatif. En effet, les transistors à semi-conducteurs à grille métallique (MOSFET) avec un substrat totalement déplété (FDSOI) conduisent à des courants de fuites faible et améliorent la variabilité ce qui permet de diminuer les tensions d'alimentation en particulier pour les applications SRAM. A partir du nœud 14 nm, les transistors peuvent intégrer un canal SiGe, le diélectrique high-k et la grille métallique. Tous ces nouveaux modules de procédés technologiques rendent l'analyse électrique des transistors MOS ainsi que sa corrélation avec la technologie plus compliquées. Ce travail de thèse propose plusieurs nouvelles méthodologies d'extraction automatique et statistique de paramètres pour les empilements MOS FDSOI avancées. Ces méthodologies sont toutes basées sur des mesures de capacité par rapport à la tension (C-V) rendant compte du couplage capacitif entre grille métallique, canal et substrat face arrière. Avec de telles caractéristiques C-V, des méthodologies fiables sont proposées pour l'épaisseur d'oxyde de grille équivalente (EOT), le travail effectif de la grille métallique FDSOI ( $W_{eff}$ ), ainsi que d'autres paramètres comme les épaisseurs du canal ( $t_{ch}$ ) et de l'oxyde enterré ( $t_{box}$ ) ainsi que l'affinité électronique efficace ( $X_{eff}$ ) du substrat face arrière qui inclut les différents effets électrostatique sà l'œuvre dans l'oxyd eenterré et à ses interfaces. Ces différentes méthodologies ont été validées par des simulations quantiques. La force de l'analyse expérimentale a été de contrôler la cohérence des extractions obtenues sur tout un ensemble de transistors MOS obtenus à partir de variation sur les différentes briques de base et de contrôler la cohérence des paramètres extraits.

**Mots-clés:** MOSFET; FDSOI; travail de sortie effectif; épaisseur d'oxyde de grille équivalente; oxide enterré; épaisseur de canal; affinité électronique effective; condition de bande plate de substrat; condition de bande plate face avant; condition de bande face arrière; tension de seuil.

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