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Feasibility of solution processed organic field-effect transistors

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Wenlin Kuai. Feasibility of solution processed organic field-effect transistors. Micro and nanotechnologies/Microelectronics. Université de Rennes, 2017. English. NNT : 2017REN1S013 . tel-01620216

HAL Id: tel-01620216

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THÈSE / UNIVERSITÉ DE RENNES 1
sous le sceau de l'Université Bretagne Loire

pour le grade de
DOCTEUR DE L'UNIVERSITÉ DE RENNES

1 Mention : Electronique

Ecole doctorale MATISSE

présentée par

Wenlin KUAI

préparée à l'unité de recherche IETR- UMR CNRS 6164
Institut d'Electronique et de Télécommunication de Rennes
UFR Informatique – Electronique

Intitulé de la thèse :

**Faisabilité de
transistors organiques
à effet de champ
fabriqués entièrement
en solution.**

**Thèse soutenue à Rennes
le 23 janvier 2017**

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Thèse de l'Université de Rennes 1

Faisabilité de transistors organiques à effet de champ fabriqués
entièrement en solution

Feasibility of fully solution deposited OFETs

Présentée par **Wenlin KUAI**

Résumé

Ces dernières décennies, des efforts de recherches considérables ont été mis en œuvre afin de répondre aux nouveaux défis sociétaux (i.e., énergie durable, utilisation efficace de matières premières, santé, mobilité...) ainsi qu'aux nouveaux modes de consommation (i.e., objets connectés, écrans grande surface et/ou souples...). Ainsi, devraient voir le jour dans un future proche : i) des écrans souples transparents et couvrant de grandes surfaces, ii) des panneaux photovoltaïques souples iii) des capteurs connectés souples enregistrant des constantes physiologiques au plus près des patients... Les acteurs de l'électronique, multinationales et laboratoires de recherche, s'efforcent de proposer de nouvelles technologies permettant de satisfaire ces nouveaux besoins. L'une d'elle, développée depuis une décennie et communément appelée « électronique imprimée », est un sérieux candidat pouvant répondre aux problématiques actuelles citées précédemment.

L'électronique imprimée, met en œuvre des matériaux en solution (encres : polymériques, semiconductrices, à base de nano-objets...) en utilisant des équipements déjà éprouvés dans l'art graphique. Cependant, les savoir-faire acquis dans le domaine de l'impression doivent être transférés vers « le monde de l'électronique » où la réalisation de motifs miniatures et la qualité de transport électronique sont des paramètres importants. ***Cette problématique, constituant un enjeu majeur, a donné naissance à cette étude.*** En effet, la méthodologie de conception des dispositifs électroniques imprimés est différente de celle utilisée en « électronique conventionnelle ». Concrètement, un dispositif électronique

imprimé est réalisé de façon additive (chaque couche le constituant est déposée l'une après l'autre et ne nécessite aucune étape de gravure) contrairement à un dispositif réalisé par photolithographie où les couches sont déposées sur une grande surface puis gravées pour définir des motifs (procédé communément utilisé en microélectronique). De plus, l'électronique imprimée peut adresser d'autres challenges tels que : la réalisation à basse température d'électronique sur des substrats non-conventionnels et de grande surface (plastique, papier, biodégradable...). Des premiers transistors entièrement imprimés ont été réalisés en laboratoire, mais, à ce jour, aucun produit n'a été commercialisé en utilisant cette technologie. En effet, de nombreux verrous restent à lever tels que : la fiabilité, la reproductibilité de fabrication et de performance des dispositifs.

Le laboratoire a acquis par le passé une expérience solide sur la réalisation par lithographie de transistors sur substrat flexible et plus récemment de transistors organiques réalisés par évaporation. La technologie organique est un candidat de choix pour réaliser des transistors entièrement en solution. En effet, tous les matériaux constituant un transistor peuvent être « mis en solution ». Des encres à base de nanoparticules ou de polymères conducteurs, d'isolants polymériques et de semiconducteurs organiques solubles peuvent être utilisées respectivement comme électrodes de contact, isolant de grille et couche active. Par conséquent, ***Cette étude a pour but d'étudier la faisabilité de fabrication de transistors organiques entièrement en solution et à terme entièrement imprimés.*** La démarche scientifique suivie lors de cette étude consistera en :

- L'étude et l'optimisation des paramètres expérimentaux permettant de fabriquer des transistors organiques réalisés par photolithographie dont le semiconducteur solubilisé a été déposé en solution (par « drop casting »).
- L'étude de faisabilité de transistors organiques entièrement imprimés
- L'étude d'une nouvelle fonctionnalisation chimique de surface permettant d'améliorer les caractéristiques électriques des transistors.

Dans la première partie de ce travail, des structures « bottom gate-bottom contact » ont été réalisées par photolithographie. Ces structures dont la technologie est maîtrisée au laboratoire, ne sont pas réalisées entièrement en solution (cf figure 1). Cependant, elles

constituent une base solide permettant d'établir les paramètres expérimentaux optimums de la couche active de semiconducteur organique déposée en solution (drop-casting).

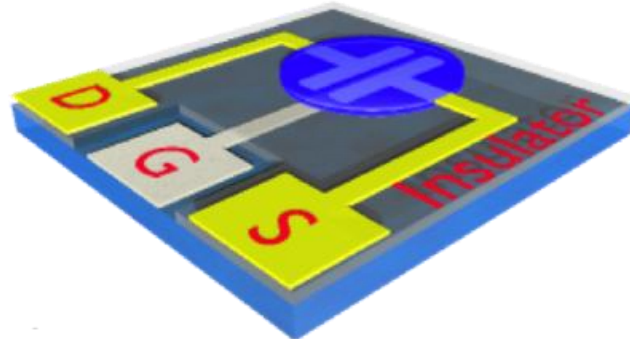


Figure 1 : Illustration d'un transistor organique (structure « bottom gate-bottom contact »).

Dans le cadre de notre étude les matériaux et les techniques de dépôt utilisés sont les suivants : contact de grille en aluminium déposé par évaporation thermique, contact drain et source en or déposé par évaporation thermique ; isolant de grille (Su8) déposé par « spin-coating » (en solution) ; semiconducteur déposé par « drop-casting » (en solution)

Le C_{60} de conduction de type n et le Tips-pentacene de conduction de type p, deux semiconducteurs organiques, ont été choisis comme couche active de transistors de type n et de type p aboutissant à une électronique CMOS entièrement en solution. Pour chaque type de semiconducteur, l'effet des paramètres expérimentaux (type de solvant, température de séchage et de recuit du semi-conducteur) sur la réponse électrique des transistors organiques a été étudié. Aussi, une analyse morphologique des semiconducteurs organiques a démontré que la nature des solvants à un impact drastique sur la morphologie des cristaux des semiconducteurs mais aussi sur la valeur du courant de fuite de grille I_{GS} .

Semiconducteur	Solvant	$\mu(\text{cm}^2/\text{Vs})$	$V_{\text{TH}} (\text{V})$	SS (V/dec)	$I_{\text{on}}/I_{\text{off}}$
C_{60}	Dichlorobenzene	0.018	31.5	12.64	10^5
Tips-pentacene	Chlorobenzene	0.094	-2.1	2.7	10^3

Tableau 1: Principaux paramètres, mobilité μ , tension de seuil V_{TH} , pente sous le seuil SS et rapport courant direct sur courant inverse $I_{\text{ON}}/I_{\text{OFF}}$, extraits des caractéristiques électriques de transistors organiques dont le semiconducteur C_{60} dissous dans du dichlorobenzene ou Tips-pentacene dissous dans du chlorobenzene, a été déposé par « drop casting » et dont les paramètres expérimentaux ont été optimisés.

D'autres, par une analyse du courant de grille I_{GS} a montré qu'il était dépendant du solvant solubilisant le semiconducteur (cf figure 2)

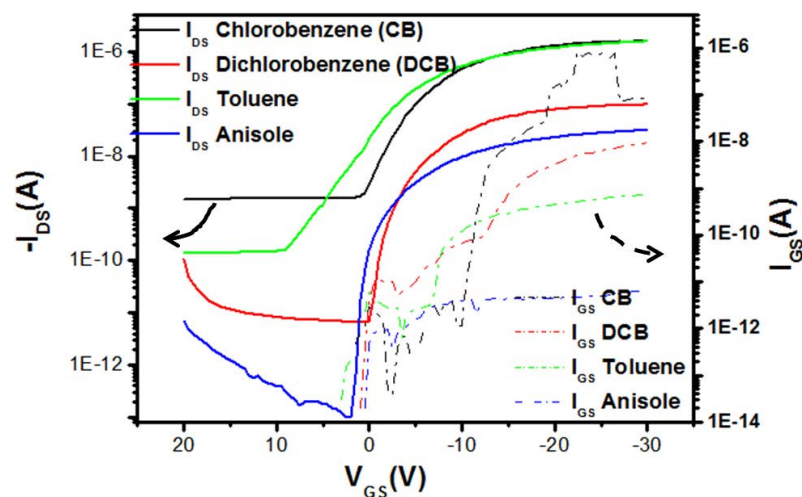


Figure 2 : Caractéristique de transfert courant drain-source I_{DS} en fonction de la tension grille-source V_{GS} et courant de fuite de grille I_{GS} des transistors organique en fonctions du type de solvant utilisé pour diluer le semiconducteur (Tips-pentacene).

Ce résultat a été confirmé par des mesures de capacités MIM (métal/isolant/métal) dont l'isolant a subi un traitement à base de solvant. Nous avons émis l'hypothèse que le solvant pouvait « endommager chimiquement » l'isolant polymérique. Cette première partie a permis de déterminer les paramètres expérimentaux optimaux concernant la dilution des semiconducteurs et de soulever le problème du fort courant de grille I_{GS} . Ce dernier étant

néfaste pour un fonctionnement optimal des transistors, une solution originale pour le réduire a été proposée et sera décrite par la suite.

La seconde partie de ce travail traite de l'impression jet d'encre. Cette technologie, nouvelle pour le laboratoire, a nécessité une étude portant sur le choix et la mise en œuvre des matériaux. Chaque matériau constituant le transistor organique a été caractérisé vis à vis de l'éjection, de l'imprimabilité, de sa morphologie et de ces propriétés électriques.

En ce qui concerne les électrodes de grille et de drain/source, une encre commerciale à base de nanoparticules d'argent a démontré la possibilité de réaliser : i) des pistes de résistivité comparable à la littérature ($2.5 \cdot 10^{-5}$ ohm.cm), ii) une largeur de piste minimum de $60\mu\text{m}$, iii) une distance reproductible entre deux pistes de $60\mu\text{m}$, iv) une température de recuit de 120°C compatible avec la température maximale acceptable d'un substrat plastique, type PEN.

Concernant l'isolant de grille, l'étude a permis de démontrer la versatilité d'une encre polymérique (Su-8) d'un point de vue de l'éjection (sur une large gamme de concentration en polymère (1 à 15cp) et de l'imprimabilité (après traitement chimique de surface par UV/ozone). De plus, plusieurs scripts d'impression (en activant une ou plusieurs buses d'impression simultanément) ont montré la possibilité de contrôler l'épaisseur de la couche isolante. Par conséquent, des structures « bottom gate-bottom contact » non-entièrement imprimées ont été réalisées (figure 3) et testées avec un semiconducteur évaporé afin de montrer la faisabilité de la structure (grille/isolant/drain-source) dans un premier temps. Un récapitulatif des paramètres (μ , V_{TH} , SS, $I_{\text{on}}/I_{\text{off}}$) extraits des caractéristiques électriques d'un transistor est montré en tableau 2.

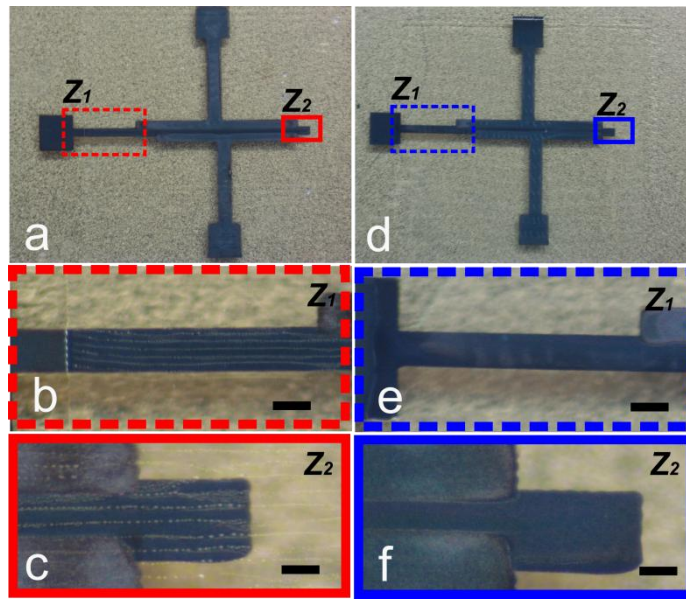


Figure 3: Images optiques des structures « bottom gate-bottom contact » non entièrement réalisées par impression (électrodes et isolant imprimés, semiconducteur évaporé) : (a) isolant réalisé en activant une buse d'impression; (b) Zoom sur les bords de l'isolant correspondant au transistor décrit en (a); (c) Zoom sur le canal du transistor décrit en (a); (d) isolant réalisé en activant plusieurs buses d'impression; (e) Zoom sur les bords de l'isolant correspondant au transistor décrit en (d); (f) Zoom sur le canal du transistor décrit en (d).

$\mu(\text{cm}^2/\text{Vs})$	$V_{\text{TH}} (\text{V})$	SS (V/dec)	$I_{\text{on}}/I_{\text{off}}$
0.0059	21.76	4.72	10^4

Tableau 2: Exemple de caractéristique électrique d'OFET imprimé en activant plusieurs buses d'impression et un isolant d'épaisseur $1\mu\text{m}$.

La structure étant validée, des tests de transistors entièrement en solution ont été réalisés mais un phénomène de démouillage du semiconducteur (déposé par drop casting) sur les électrodes drain/source a été observé. Par conséquent, la couche active de semiconducteur n'était pas continue entre les électrodes (cf figure 4a). Une méthode originale a été proposée pour résoudre ce problème. L'idée consiste à ajouter un polymère en faible quantité dans la solution semiconductrice afin de piéger la ligne de contact du semiconducteur liquide (cf figure 4b).

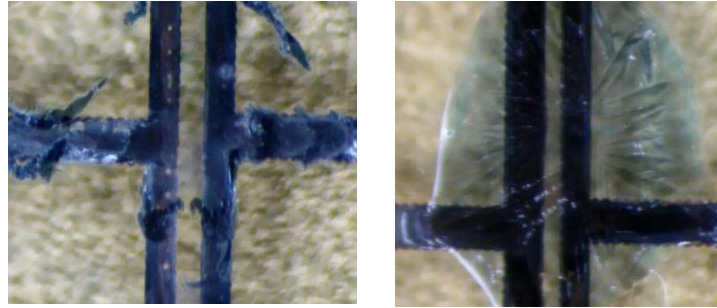


Figure 4: Images optiques du semiconducteur déposé par “drop casting” sur des électrodes imprimées: a) couche non continue de semiconducteur après séchage d’une goutte de tips-pentacène dilué dans son solvant; b) couche continue de semiconducteur après séchage d’une goutte de tips-pentacène dilué dans : i) son solvant et ii) une faible quantité de polymère (5% en volume de Su8).

Des transistors entièrement imprimés ont été réalisés mais leur comportement électrique, bien que prometteur, n’a pas montré un comportement électrique compatible avec la réalisation de circuit électronique de type inverseur, par exemple. Par conséquent, une étude plus approfondie de la dilution de polymères est indispensable et sera effectuée dans des travaux ultérieurs.

La troisième partie de ce travail a consisté en l’étude et la mise au point d’une nouvelle fonctionnalisation de surface de l’isolant polymérique dans le but de réduire le courant de fuite I_{GS} . Le greffage de l’1-aminoanthraquinone sur l’isolant a été étudié d’un point de vue : rugosité, énergie de surface et polarité. L’impact de la fonctionnalisation de surface sur les transistors a été estimé en réalisant des caractérisations électriques (caractéristique de transfert, de sortie et de stabilité électrique). Comme le montre la figure 5, la mobilité des transistors est considérablement augmentée (1 décade) lorsque les transistors sont fonctionnalisés. De plus, et ce qui est particulièrement important, le courant de fuite de grille a été largement réduit (Figure 6).

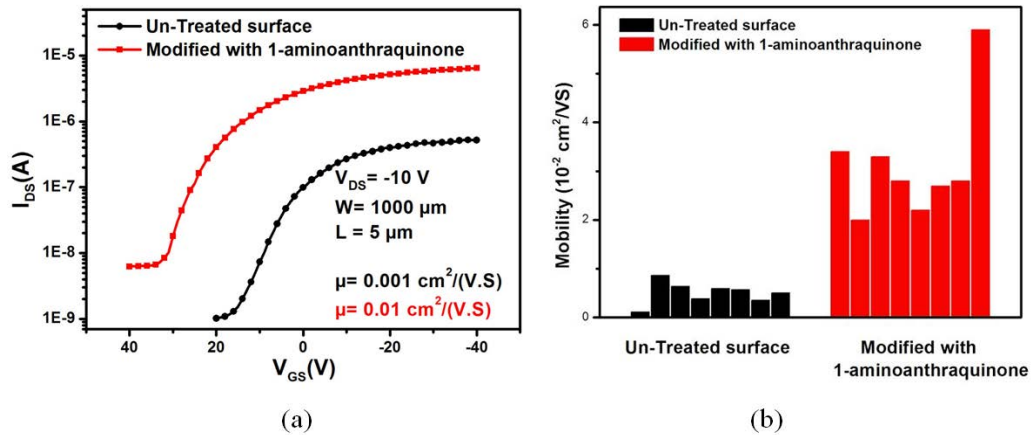


Figure 5: (a) Caractéristiques de transfert avec et sans fonctionnalisation (b) dispersion de la mobilité avec et sans modification de surface

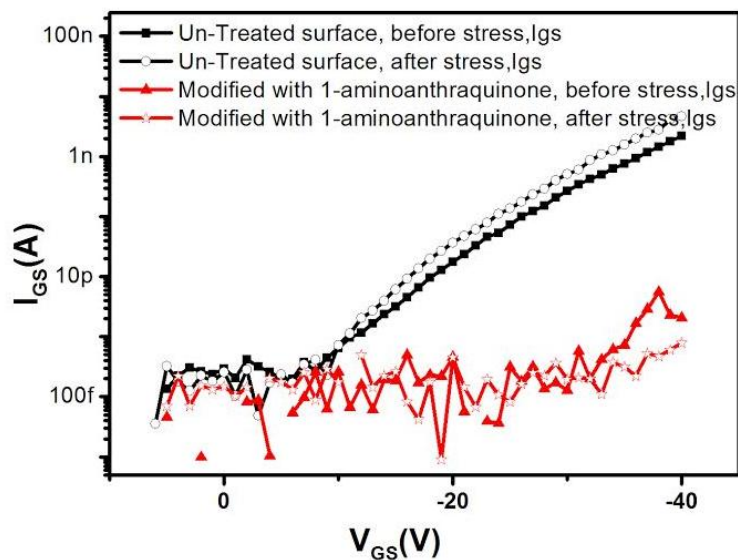


Figure 6: Courant de fuite de grille en fonction de la tension grille pour un transistor dont l'isolant de grille SU8 n'a pas été (courbe en noir) ou a été (courbe en rouge) fonctionnalisé avant le dépôt de la couche active semiconductrice.

En conclusion cette thèse constitue une très large revue de la problématique et des difficultés à surmonter dans la recherche d'un procédé fiable et reproductible de fabrication de transistors entièrement en matériaux organiques déposés par impression à jet d'encre. Des solutions ont été trouvées et de nouvelles idées proposées. Cependant beaucoup de travaux sont encore nécessaires.

Le plus important a été ici de montrer la faisabilité d'un tel procédé.

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Introduction

Flexible electronics becomes now a major research domain due to a fast growing market. The market of wearable technology was \$24 billion in 2015 and it is expected to grow over \$70 billion in 2025 ^[1]. Only the e-textiles market will grow by 68% rate reaching \$3 billion in 2026 ^[2]. These data cover in fact a lot of fields, technologies and materials. Robotics ^[3], health monitoring ^[4], epidermal electronics ^[5], e-textile ^[6], displays ^[7] are the main targeted fields.

Flexible or even stretchable devices need ultra-flexible materials. The first parameter indicating the flexibility of a material is its Young modulus. Young modulus is in the range of 0.1-10 GPa ^[8] for organic materials. It is higher than 100 GPa for inorganic oxide based semiconductors (130 GPa for the most used oxide IGZO ^[9]) and around 160 GPa for silicon. With their very low Young modulus, organic materials are considered fitting perfectly the need of flexibility.

This is why numerous studies on organic materials based electronic devices were made in the last 2 decades. Particularly the first element of any electronics that is the transistor was, since 1986, and continue to be the subject of major research in the world.

Field Effect Transistor, particularly in its thin film structure, is a stack of different thin films, mainly the semiconducting active layer, the gate insulator and the gate contact. Major works in the world on these Organic Thin-Film Transistors (OTFTs) focus only on the need to have organic semiconducting active layer; the other insulating and conducting films are made of inorganic materials. In the main idea to get highly flexible device, it is more important to focus on fully organic TFT where all the layers are made on organic materials in the purpose to benefit from the low Young modulus of these materials.

The present PhD thesis focuses on this main purpose, trying to determine the main parameters influencing the performance of fully organic TFT.

In this trying, the work considers the need to use the lowest cost but highest reproducibility techniques. Indeed, the main interest of flexible electronics is its use in lowest cost and large public products.

Deposition of thin films by solution techniques at ambient temperature, avoiding vacuum techniques, will lead to lowest cost devices.

Solution techniques are numerous. We can take as examples spin coating, drop casting, printing... From all these techniques, inkjet printing becomes more and more attractive thanks to the low used volume inducing low cost, the reproducibility that is the main issue of such techniques and the use of software design avoiding the need of hard mask. Most of studies on solution processed OTFTs are devoted on this technique.

The present work focuses on solution processed OTFTs fabricated by using drop casting and inkjet printing to achieve high electrical performance, electrical stability and reproducibility. Drop casting was used only as a first step in determining the main parameters influencing the process of solution deposited OTFTs.

The work benefited from the great experience of IETR in thin film electronics, particularly in silicon based devices. This experience was extended some years ago on organic TFTs using evaporated organic semiconducting active layer, organic insulator and inorganic metallic contacts ^[10]. The present work continues this trend towards low cost and low temperature processed electronics.

The thesis is organized in 4 chapters.

In the first chapter, the development of OTFTs will be introduced. The principle and deposition methods including vacuum deposition and solution processing of organic semiconductor will be described. Afterwards, a brief description of solution-processed OTFTs will be given. The basics, the structure, the characteristics and parameters extraction of OTFTs are detailed.

In the second chapter, drop casted OTFTs will be introduced. N-type OTFTs based on C₆₀ and p-type OTFTs based on Tips-pentacene will be detailed. Issues of solution processing, including solvent effect, drying and annealing temperature effect, and surface functionalization effect will be firstly presented. The processing of OTFTs will be introduced. Depending on the issues of solution processing, solvent effect, drying and annealing temperature effect, and surface functionalization effect will be presented in detail.

In the third chapter, inkjet printed OTFTs will be presented. This chapter consists of two major parts.

Part I is dealing about technique and methodology of inkjet printing. Printed electronics, including applications and printing techniques will be first detailed. Inkjet printing technology as well as printing key steps, printing system and characterization methods will be detailed in the second section.

Part II is dealing about inkjet print OTFTs. The printability of OTFT functional materials, including conductive ink, insulator ink, and semiconductor ink will be presented. The OTFT fabrication, as well as printing methodology for stacked layers structure, and electrical characterization will be presented in the second section.

In the fourth chapter, a method to improve the characteristics of solution processed OTFTs using surface modification of the Su8 gate insulator by 1-aminoanthraquinone before depositing the semiconducting active layer, will be introduced. Principle of surface modification at the interface between the active layer and the gate insulator in OTFTs process will be firstly introduced. Indeed, charge carrier transport between source and drain in OTFTs is restricted by the first several semiconductor monolayers next to semiconductor-insulator interface. Thus, the surface of insulator is critical for the electrical performance of the transistors. Main factors at the semiconductor-insulator interface, including surface roughness, surface energy, surface polarity and dielectric constant will be detailed. Then first trying to change the interface between the semiconductor and the insulator in present OTFTs is introduced by functionalizing the surface of Su8 gate insulator by 1-aminoanthraquinone.

Finally, the thesis is concluded by remembering the main results and presenting the way to continue this work leading to functional solution processed organic electronics.

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Chapter 1: OTFTs: General Points

I Introduction

As explained in the introduction of this thesis, the present work deals with the development of new organic electronics based on solution fabricated electronic circuits. It focuses on the first element of any electronics that is the transistor and particularly on the field effect transistor. Field effect transistor is a stack of different thin films when dealing with large-area electronics fabricated on any substrate and using different semiconductor materials as silicon, metal oxides or organics. In this case, the transistor is named Thin Film Transistor (TFT).

Thin Film Transistor is based on the modulation of the current flowing in a semiconductor material between 2 electrodes, named source and drain, by a bias applied on a third electrode, the gate, that is electrically insulated from the way between drain and source electrodes by an insulator (or dielectric) material. A structure of TFT in bottom gate, bottom contacts configuration is given in the scheme of Figure 1-1. Present work will focus on this configuration. However, other configurations are possible and will be presented in the next. The choice of the configuration of Figure 1-1 will be also explained.

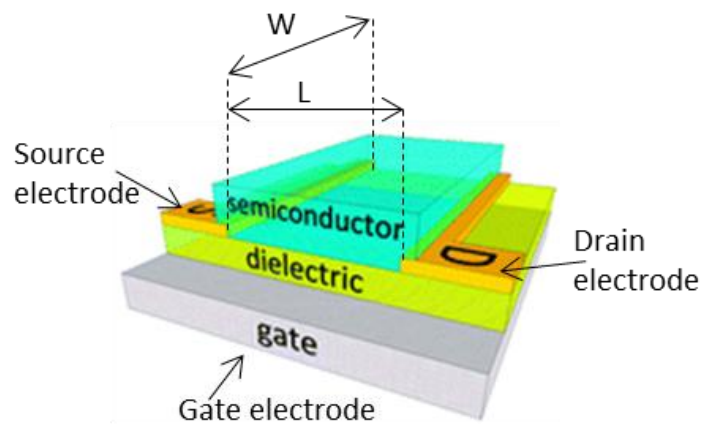


Figure 1-1: Structure of Thin Film Transistor presented here in the bottom gate, bottom contacts configuration.

In the ideal, under some gate voltage no current flows between source and drain contacts. In this case, the transistor is in its off-regime. Under other gate voltage the maximum current has to flow between source and drain contacts and the transistor is in its on-regime. In practical, low current I_{off} flows in off-regime and lower is this current best performance of TFT is expected.

In on-regime the performance is quantified by the maximum current I_{on} flowing between source and drain.

Hence, in high performance TFT, I_{off} has to be as low as possible and I_{on} as high as possible. The ratio I_{on}/I_{off} is a good factor to evaluate the quality of a TFT.

The value of the on-current I_{on} depends on:

- The external parameters: gate voltage, voltage between source and drain contacts.
- The physical parameters: charge transport parameters of the semiconducting material between source and drain, the electrical quality of the interface between the insulator and the semiconductor as the different films are very thin.
- The geometrical dimensions: the distance between source and drain contacts (named L for length) and the length of the drain and source electrodes (named W for width of the transistor).

Higher on-current is given by the best charge transport parameters of the semiconducting material (that means the highest charge carrier mobility) for the same geometrical dimensions and the same applied voltages.

After this brief introduction on the principle of a transistor, we have now to introduce the organic based TFT or OTFT

II Development of Organic Thin-film Transistors (OTFTs)

Compared to inorganic-semiconductor based transistors ^[1-3], the study of organic semiconductor based transistors ^[4] started more recently. Before the use of organic semiconductor as active layer for transistor, researchers have focused on material properties.

In 1832, Jacob Berzelius firstly used the polymer as organic material ^[5]. It is well-known that polymers have an insulator behavior. Consequently, experiments performed on polymer's conductivity improvement have been carried out since the end of the 18th. In 1862, Henry Letheby succeeded to fabricate a partly conductive "blue substance" ^[6]. Moreover, in 1906, Pochettino reported the photovoltaic effect in anthracene ^[7]. Such organic molecule was widely used in the following decades for the interpretation of physical properties. Until the second half of the 19th, Akamatu obtained a conductive organic material: the perylene ^[8]. It has a relatively good electrical conductivity (10^{-3} S/cm). Preliminary studies dealing with electrical and optical properties of polymer chains were performed around 1960s ^[9]. Some

work focused on the fabrication of new polymers with longer organic molecules and in order to improve electrical performance.

In the same period, another route of research on organic semiconductor materials was the investigation of π -conjugated materials. Hideki Shirakawa obtained a conductive transpolyacetylene, with conductivity of 30 S/cm^[10].

After 30 years of study on polymers^[11, 12] and small molecules^[13, 14], Richard Friend and Francis Garnier have fabricated organic transistors, in 1988^[15] and 1990^[16], respectively. They have contributed greatly on the development of Organic Field-Effect Transistors (OTFTs).

One of the most important electrical parameters of organic transistors is carrier mobility^[17]. The development of the field effect mobility of both p-type and n-type transistors based on small molecule and polymer is summarized in Figure 1-2^[17]. It can be observed that the motility has been improved continually for both p-type and n-type and both vacuum-processed and solution-processed during the past 30 years.

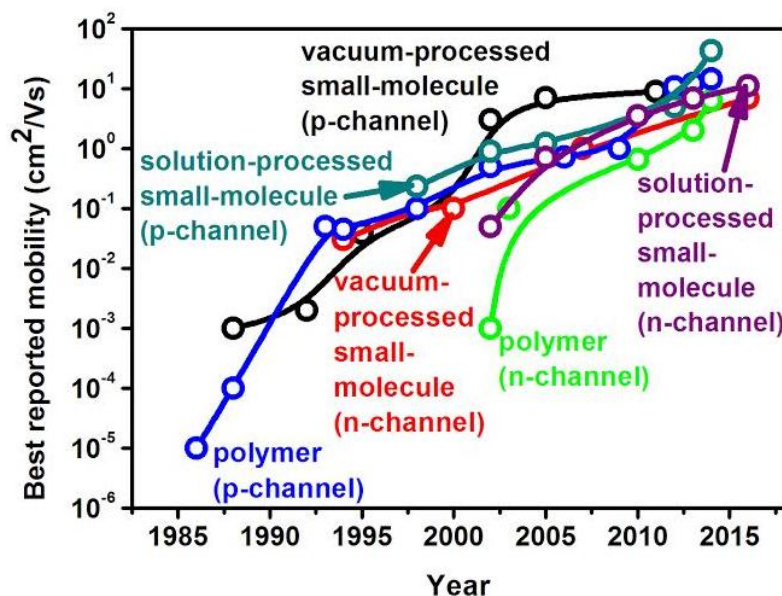


Figure 1-2: Development of the carrier field-effect mobility of p-channel and n-channel transistors based on small molecule and polymeric semiconductors.

Vacuum-processed technique and solution-processed technique are two main methods for depositing organic semiconductors^[18]. Table 1-1 lists the highest field-effect mobility (μ) values measured from OTFTs as reported in the literature, annually from

Year	Mobility (cm ² /Vs)	Material (deposition method) (v) = Vacuum deposition (s) = From solution	I _{on} /I _{off}	W/L	Ref
1983	Minimal, NR	Polyacetylene (s)	NR	200	[19]
1986	10 ⁻⁵	Polythiophene (s)	10 ³	NR	[20]
1988	10 ⁻⁴	Polyacetylene (s)	10 ⁵	750	[21]
	10 ⁻³	Phthalocyanine (v)	NR	3	[22]
	10 ⁻⁴	Poly (3-hexylthiophene) (s)	NR	NR	[23]
1989	10 ⁻³	Poly (3-alkylthiophene) (s)	NR	NR	[24]
	10 ⁻³	A-v-hexathiophene (v)	NR	NR	[25]
1992	0.027	A-v-hexathiophene (v)	NR	100	[26]
	2×10 ⁻³	Pentacene (v)	NR	NR	[43]
1993	0.05	A-v-dihexyl-hexathiophene (v)	NR	100-200	[30]
	0.22	Polythiylenevinylene (s)	NR	1000	[28]
1994	0.06	A-v-dihexyl-hexathiophene (v)	NR	50	[29]
	0.03	A-v-hexathiophene (v)	>10 ⁶	21	[30]
1995	0.038	Pentacene (v)	140	1000	[31]
	0.3	C ₆₀ (v)	NR	25	[32]
	0.02	Phthalocyanine (v)	2×10 ⁵	NR	[33]
1996	0.045	Poly (3-hexylthiophene) (s)	340	20.8	[34]
1997	0.13	A-v-dihexyl-hexathiophene (v)	>10 ⁴	7.3	[35]
	0.62	Pentacene (v)	10 ⁸	11	[36]
	1.5	Pentacene (v)	10 ⁸	2.5	[37]
	0.05	Bis(dithienothiophene) (v)	10 ⁸	500	[38]
1998	0.1	Poly (3-hexylthiophene) (s)	>10 ⁶	20	[39]
	0.23	A-v-dihexyl-quaterthiophene (v)	NR	1.5	[40]
	0.15	Dihexyl-anthradithiophene	NR	1.5	[41]
2000	0.1	N-decapentafluoroheptyl-methylnaphthalene-1,4,5,8-tetracarboxylic diimide (v)	10 ⁵	1.5	[42]
	0.1	A-v-dihexyl-quaterthiophene (s)	NR	NR	[42]
2002	0.89	Pentacene precursor (s)	4.4×10 ⁵	313	[43]
	0.66	BP2T (v)	2×10 ⁴	80-200	[44]
	3	Pentacene (v)	10 ⁵	1.3	[45]
2003	5.5	TES ADT Pentacene (s)	10 ⁶	NR	[46]
2004	1	Pentacene (v)	10 ⁸	NR	[47]
2005	7	Pentacene (v)	10 ⁶	NR	[48]
	0.7	Rubrene (s)	10 ⁶	NR	[49]
	1.2	Tips-pentacene (s)	10 ⁸	5.5	[50]
2006	0.72	Thieno-thiophene (s)	10 ⁶	NR	[51]
2007	3	Fluorinated F-TES ADT (s)	10 ⁷	NR	[52]
2009	3.8	Pentacene (v)	10 ²	10	[53]
2011	8.85	Pentacene (v)	10 ³	10	[54]
2012	10.5	DPP-DTT-based polymer (s)	10 ⁶	28	[55]
	5	PF-TAA (s)	10 ⁶	22	[56]
2013	3.5	NDI-DTYMI (s)	10 ⁸	28-280	[57]
	6.8	Tips-pentacene:o-Meo-DMBI (s)	10 ⁶	20	[58]
	12	P-29-DPPDTSE (s)	10 ⁶	NR	[59]

Year	Mobility (cm ² /Vs)	Material (deposition method) (v) = Vacuum deposition (s) = From solution	I _{on} /I _{off}	W/L	Ref
2014	1.7	FBDPPV-1 (s)	10 ⁶	20	[60]
	1.1	DNTT (s)	10 ⁷	5	[61]
	6.3	DBPy (s)	10 ³	33	[62]
	14.4	PTIIG-NP (s)	10 ⁵	50	[63]
	43	C8-BTBT (s)	10 ³	10	[64]
2015	6.7	diF-TES-ADT (s)	10 ⁵	12.5	[65]
2016	11.1	Tips-TAP (s)	10 ⁷	10	[66]
	6.8	Tips-TAP (v)	10 ⁷	10	[66]

Values for Ion/Ioff correspond to different gate voltage ranges and thus are not readily comparable to one another.

NR = Not reported

Table 1-1: Highest field-effect mobility (μ) values measured from OTFTs as reported in the literature annually from 1983 to 2016.

It can be observed that the mobility increased from 10⁻⁵ to 43 cm²/Vs. Moreover, lots of organic materials were used as active layer in transistors. Solution-processed OTFTs have attracted interests of scientific research and industry, because of its low cost, and low temperature fabrication process. Furthermore, solution-processed organic semiconductor is a serious candidate in order to achieve equivalent field effect mobility than vacuum-processed technique.

III Principle and deposition methods of organic semiconductor

In this section, the working principle of organic semiconductor will be introduced firstly. The deposition methods of organic semiconductor including vacuum deposition and solution process will be presented. Moreover, solution-processed deposition method will be presented in detail.

III.1 Principle of organic semiconductor

The energy scheme in Figure 1-3 (a) shows: the respective positions of the Fermi level of gold, the lowest unoccupied molecular orbital (LUMO) and the highest occupied molecular orbital (HOMO) of pentacene. As can be seen in Figure 1-3 (a), the LUMO level of pentacene is quite far away from the Fermi level of gold than the HOMO level. Consequently, there is a substantial energy barrier for electrons. When a positive voltage is applied to gate,

although negative charges will be induced at the source, barrier height is too high to inject electron. In contrast, when a negative voltage is applied to gate, holes are easily injected from HOMO to gold. Due to this fact, pentacene is said to be p-type.

On the contrary, an organic semiconductor is said to be n-type when electron injection is easier than hole injection, which occurs when the LUMO level is closer to the Fermi level than the HOMO level.

Organic semiconductors are conjugated π -electron systems with sp^2 hybridized carbon-carbon bonds. Figure 1-3 (b) shows the classic example of a benzene ring. π -electron cloud is formed between π -orbitals, allowing for the delocalization of electrons through bond resonance. The π -orbitals are out-of-plane with the atoms, meaning that the conjugated π -electron cloud can interact with π -electron clouds on neighboring molecules. Due to the interaction, periodicity of molecules can result in a split of the molecular orbitals into energy bands (i.e. HOMO energy band and LUMO energy band).

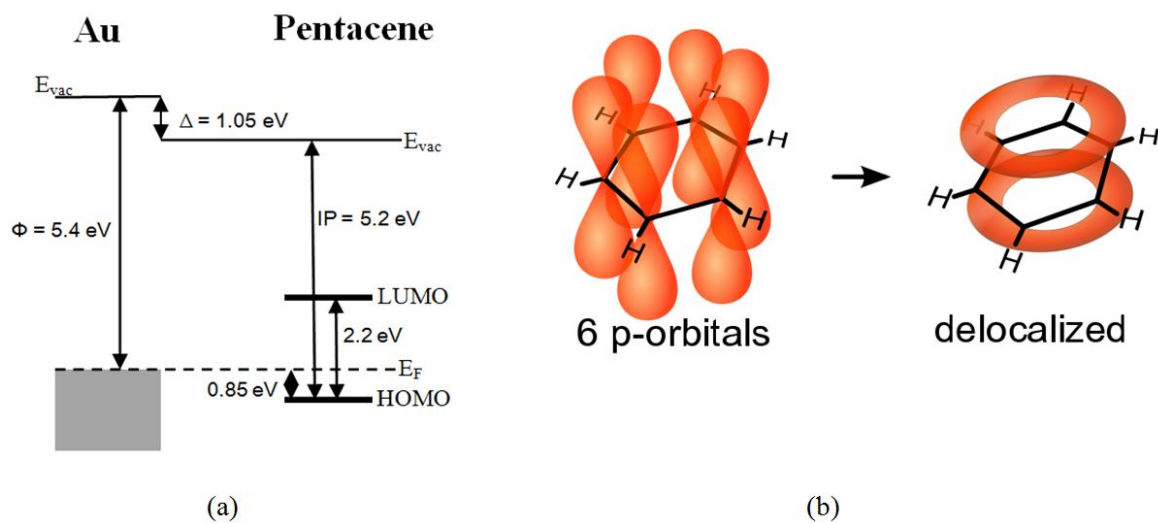


Figure 1-3: (a) Energy diagrams of Au/pentacene interface, (b) Schematic illustration of the orbital hybridization in a benzene ring^[67].

III.2 Deposition methods of organic semiconductor

There are many deposition methods in OTFT fabrication process. Each method has its own specific feature and application. Here, two different deposition methods will be presented: vacuum deposition and solution-processed deposition.

III.2.1 Vacuum deposition

Vacuum deposition is a well-known process. It is used to deposit layers of material atom-by-atom or molecule-by-molecule on a solid surface. This process operates at pressures well below atmospheric pressure. The deposited layers can range from a thickness of one atom up to several micrometers. Many organic materials can be thermally evaporated, and consequently can form a thin film layer. The schematic illustration of the vacuum deposition process is shown in Figure 1-4.

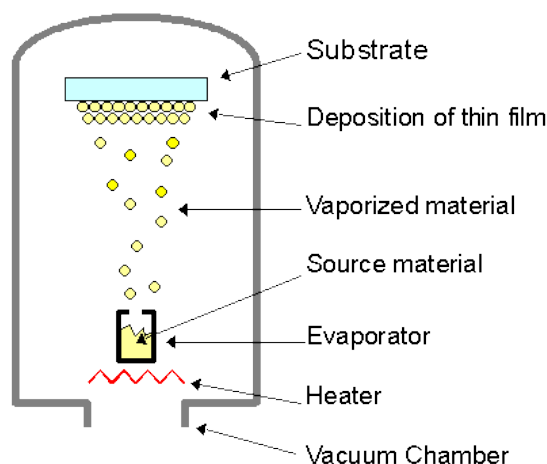


Figure1-4: Schematic illustration of the vacuum deposition process.

The advantages of vacuum deposition technique are listed as follows:

- Metal, semiconductor, insulator, and polymer can be deposited on metal, semiconductor, insulator, and even on plastic, paper...
- The crystals of deposited material are related to the deposition rate, substrate temperature and the deposition angle of thermally evaporated material.
- High purity films can be obtained.

III.2.2 Solution-processed deposition

Since 1990, researchers have proved that equivalent electrical performance can be obtained using solution-processed OTFTs and vacuum-processed OTFTs. Development of high performance p-type and n-type semiconductors is a key step in order to fabricate electronic devices (i.e. p-n junction devices, organic light-emitting diodes, photovoltaic, organic complementary metal-oxide-semiconductor (CMOS)). In this work, C₆₀ and Tips-pentacene were used as n-type and p-type organic semiconductor respectively, in order to

fabricate solution-processed OTFTs. The development of the field effect mobility of both C₆₀ and Tips-pentacene transistors based on solution-processed OTFTs were summarized in Figure 1-5. As can be observed, the motility has been improved for both C₆₀ and Tips-pentacene during the past years. Table 1-2 lists the field-effect mobility (μ) values measured from OTFTs as reported in the literature, annually from 2002 through 2015.

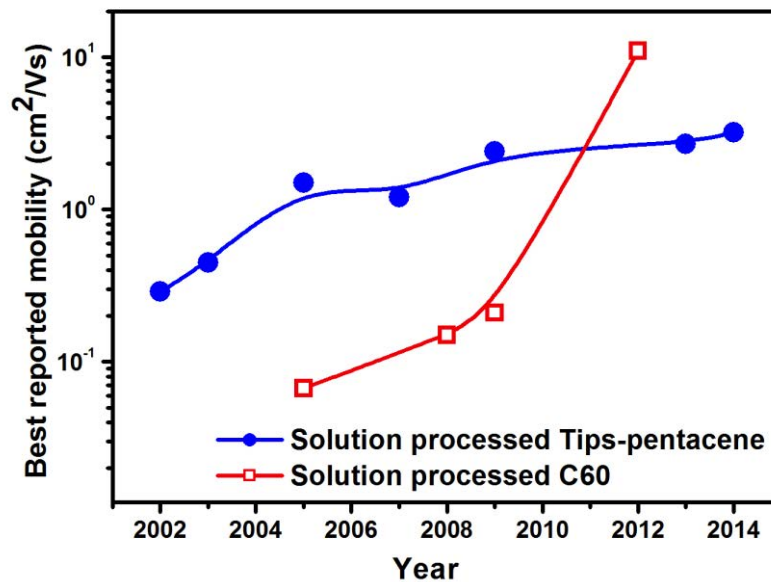


Figure 1-5: Development of the carrier field-effect mobility of p-channel and n-channel transistors based on solution-processed OTFTs. Note that, the reported mobilities are extracted from Table 1-2 (Only the best motilities are plotted for each year)

Year	Mobility (cm ² /Vs)	Material (solution-processed) (sc) = spin coat (dc) = drop cast (dp) = dip coat (ip) = inkjet print	Solvent	I _{on} /I _{off}	W/L	Ref
2002	0.29	Pentacene (sc)	Chloroform	2×10 ⁷	100	[68]
2005	>1.5	Tips-pentacene (dc)	Toluene	10 ⁶	4.4	[69]
	1.5	Tips-pentacene (sc)	Toluene	NR	5.5	[70]
	0.1	C ₆₀ derivative (sc)	Chlorobenze	<10 ⁴	4000	[71]
	0.45	Pentacene (dc)	Trichlorobenze	10 ⁵	10	[72]
	0.067	C ₆₀ derivative (sc)	Chloroform	1.6×10 ⁵	250	[73]
	0.023	C ₆₀ derivative (sc)	Chloroform	7×10 ⁴	250	[73]
2007	1.2	Tips-pentacene(dc)	Toluene	10 ⁸	8.8	[74]
	0.6	Tips-pentacene(dc)	Toluene	NR	NR	[74]
	0.2	Tips-pentacene(dp)	Toluene	NR	NR	[74]
	0.6	Tips-pentacene (dc)	Toluene	NR	10	[75]
	0.48	Tips-pentacene (dc)	Toluene	10 ⁶	2.48	[76]
	0.29	Tips-pentacene (ip)	NR	10 ⁷	12.5	[77]
2008	0.17	Tips-pentacene (dc)	Toluene	10 ⁵	2	[78]
	0.15	C ₆₀ derivative (sc)	Chlorobenze	>10 ⁶	2000	[79]
	0.24	Tips-pentacene (ip)	Dichlorobenze	10 ⁷	39.3	[80]
	0.214	Tips-pentacene (dc)	Toluene	10 ⁶	6.7	[81]
	0.101	Tips-pentacene (dc)	Chlorobenze	10 ⁵	6.7	[81]
	0.009	Tips-pentacene (dc)	Tetrahydrofuran	10 ⁴	6.7	[81]
	0.018	Tips-pentacene (dc)	Chloroform	10 ⁴	6.7	[81]
1	Tips-pentacene (dp)	Toluene	10 ⁶	12.5	[82]	
2009	1.2	Tips-pentacene (dc)	Toluene	>10 ⁷	6.29	[83]
	0.21	C ₆₀ derivative (sc)	Trichlorobenze	5×10 ⁵	NR	[84]
	0.001	Tips-pentacene (dc)	Chlorobenze	4.3×10 ³	25	[85]
	0.06	Tips-pentacene (ip)	Cyclohexanol	10 ⁵	39.3	[86]
	0.07	Tips-pentacene (sc)	Dichlorobenze	NR	30	[87]
	0.3	Tips-pentacene (sc)	Xylene	4×10 ⁸	31.4	[88]
2010	0.8	Tips-pentacene (ip)	Tetralin	NR	20	[89]
2011	0.02	Tips-pentacene (ip)	Toluene	10 ⁴	31.7	[90]
	0.72	Tips-pentacene (ip)	Tetralin	10 ⁹	NR	[91]
	0.06	Tips-pentacene (ip)	Dichlorobenze	10 ⁴	4.17	[92]
	0.0079	Tips-pentacene (dc)	Toluene	10 ⁴	390	[93]
2012	11	C ₆₀ (dc)	CCl ₄ & M-Xylene	2×10 ⁶	20	[94]
	0.21	Tips-pentacene (ip)	Anisole	4×10 ⁷	15.5	[95]
	1.7	Tips-pentacene (ip)	Chlorobenze & Dodecane	10 ⁶	4	[96]
	0.85	Tips-pentacene (ip)	Dichlorobenze	10 ⁵	16.7	[97]
	0.23	Tips-pentacene (ip)	Toluene	7×10 ⁵	20	[98]
	0.18	Tips-pentacene (ip)	NR	10 ⁷	33.3	[99]
2013	0.53	Tips-pentacene (ip)	Amorphous polycarbonate	1.6×10 ⁶	20	[100]
	0.31	Tips-pentacene (ip)	Anisole	4×10 ⁷	99	[101]

Year	Mobility (cm ² /Vs)	Material (solution-processed) (sc) = spin coat (dc) = drop cast (dp) = dip coat (ip) = inkjet print	Solvent	I _{on} /I _{off}	W/L	Ref
2015	0.073	Tips-pentacene (dc)	Anisole	5×10 ⁴	10	[102]
	0.198	Tips-pentacene (ip)	Dichlorobenze	8×10 ³	6820	[103]
	0.25	Tips-pentacene (ip)	Anisole	8×10 ⁷	NR	[104]

Values for I_{on}/I_{off} correspond to different gate voltage ranges and thus are not readily comparable to one another.

NR = Not reported

Table 1-2: Summary of field-effect mobility (μ) values measured from OTFTs based on solution-processed as reported in the literature annually from 2002 through 2015.

In this work, solution-processed deposition technique has been used to performed organic semiconductor layer. The solution-processed deposition techniques can be divided into two categories:

- **Fully substrate coating:** the organic semiconductor solution is deposited on the whole substrate;
- **Selective substrate coating:** the organic semiconductor solution is deposited only on specific areas.

Each technique has advantages and drawbacks that must be carefully studied in order to determine the most suitable method for this work.

- **Fully substrate coating**

- **Spin coating**

Spin coating has been used for depositing uniform thin film in the field of micro-fabrication for several decades. Briefly, a little amount of material is deposited on the the substrate center. Then, the substrate rotates at a high speed and centrifugal forces induce material spreading uniformly on the substrate. The schematic illustration of a spin coating process is shown in Figure 1-6.

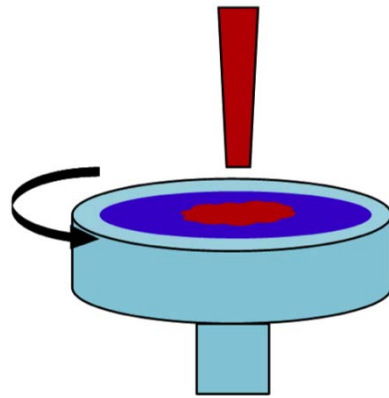


Figure 1-6: Schematic illustration of the spin coating process.

There are many factors which have a strong effect on the film morphology: the rotational velocity, the acceleration, the time, the viscosity, the concentration of the solution and the nature of the solvent (boiling point, surface tension...). Note that, in the case of organic semiconductor, it is well known that grain size is small because of a fast solvent evaporation ^[105].

➤ **Dip coating**

Dip coating has been widely used in industry. It allows the formation of uniform layer, especially on a flat or cylindrical substrate. A typical process involves immersing the substrate into coating material solution at a constant speed, after a while, pulling up the substrate from the solution with a constant speed. A thin film of solution remains on the substrate. Then, the solvent evaporates, and consequently, the thin film is deposited. The schematic illustration of a dip coating process is shown in Figure 1-7.

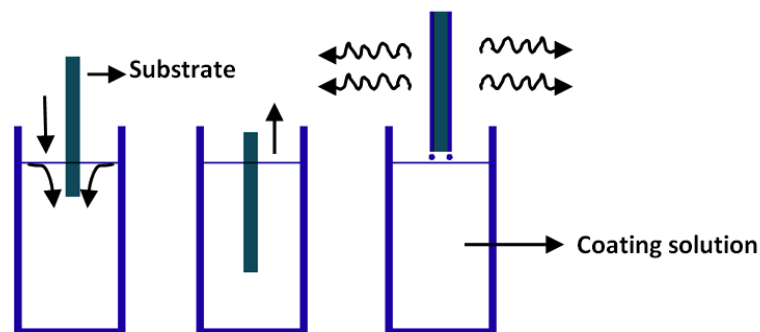


Figure 1-7: Schematic illustration of the dip coating process.

The immersion time, the speed of pulling, the solvent nature etc. have influence on the thickness and the morphology of the thin film.

➤ **Spray coating**

Spray coating has been used to fabricate organic semiconductor thin films for large-area devices. The material is mixed with a neutral gas and expelled from a nozzle to a substrate. Then, droplet spreads, the solvent evaporates, and the droplet dries. The schematic illustration of a spray coating process is shown in Figure 1-8.

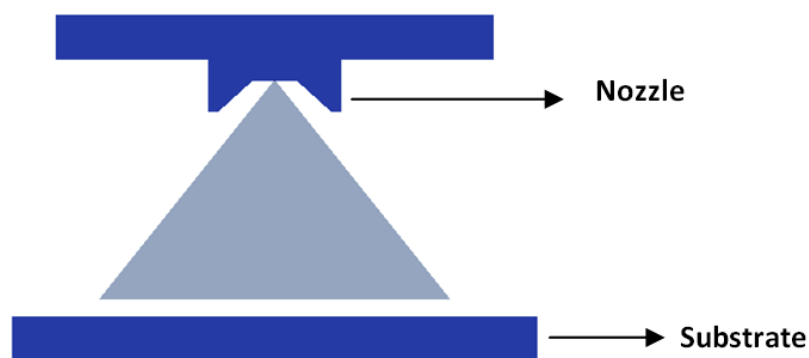


Figure 1-8: Schematic illustration of the spray coating process.

The thickness of the thin film is governed by the gas pressure, spray distance between nozzle and substrate, the solution concentration, the solvent material etc.

● **Selective substrate coating**

➤ **Drop casting**

A droplet of organic semiconductor solution is deposited on the substrate using micropipettes (manually or automatically). This deposition method allows more time for semiconductor drying than the techniques described previously. As a consequence higher degree of organic semiconductor crystallinity can be obtained, which has a great influence on its electrical behavior^[105].

The liquid volume ranging from 0.5 to 5 μl , depending on the requirement, consequently can cover several transistors at the same time as shown in Figure 1-9. This method is well adapted to a systematical study of organic semiconductor experimental parameters (solvents choice, drying and annealing temperature...) and consequently evaluates their impact on OTFT behavior. Moreover, as shown in Figure 1-9, it saves process time and

materials cost due to the fact that multiple experiments can be performed on the same substrate.

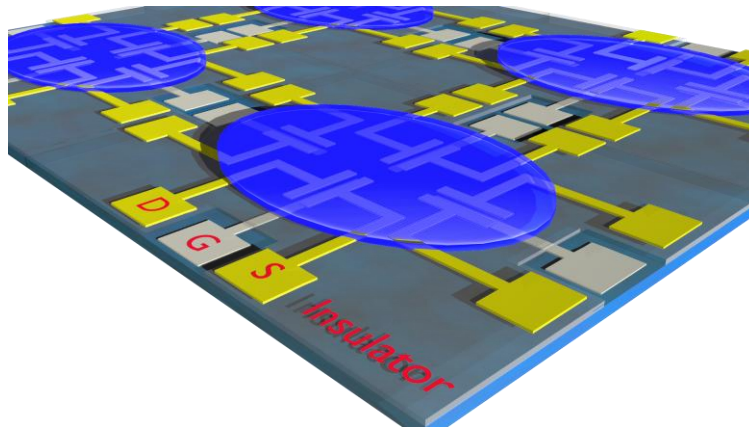


Figure 1-9: Schematic illustration of the drop casting process.

However, this deposition method suffers from a huge drawback: it is difficult to fabricate circuit due to the fact that the drop casted semiconductor covers a large surface (several mm²) and the accuracy is difficult to control.

➤ **Inkjet printing**

Inkjet printing process is similar to drop casting but the volume range is smaller (some pL). As a consequence, the droplet can be addressed only on one transistor as shown in Figure 1-10.

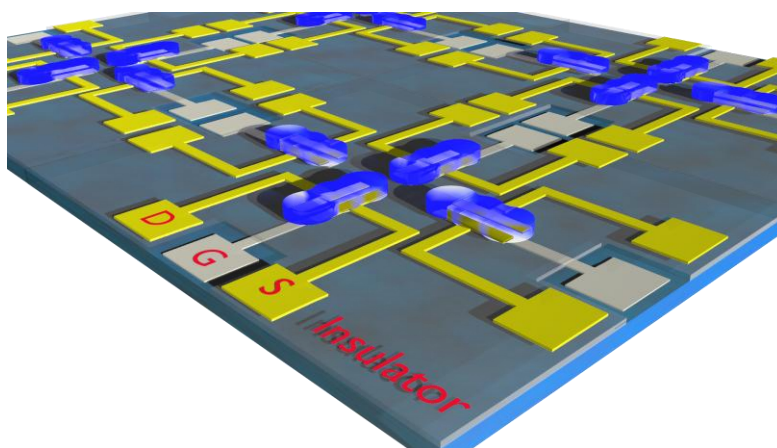


Figure 1-10: Schematic illustration of the inkjet printing process.

Note that, the working principle of inkjet printing will be discussed in more detailed in chapter 3.

IV Basics and structures of OTFTs

IV.1 Basics of OTFTs

Here a p-type organic semiconductor is used as an example in order to describe the basic operation and parameter extraction of OTFT.

OTFT working principle is similar to conventional field-effect transistors, where the channel carriers are induced in the channel by a gate bias.

Under a negative voltage on the gate (V_{GS}), holes are induced and gathered in the active layer close to the interface between insulator layer and active layer. Under a negative voltage between source and drain (V_{DS}), gathered holes in active layer are drifted, forming current (I_{DS}). Both V_{GS} and V_{DS} can control the current.

Grain boundary and impurity inside the organic semiconductor can trap electrons. A conducting channel can be formed between source and drain only when V_{GS} is larger than V_{TH} . Indeed, electrons traps filled and enough electrons gathered in active layer. Here, V_{TH} is defined as threshold voltage of OTFTs. As V_{DS} increases, I_{DS} subsequently increases linearly. This behavior is called: linear regime. In linear regime, electrons density distribution is not continuous; instead, it presents the staircase shape from source to drain. Taking V_{GS} , V_{DS} into account, the linear current can be approximated as equation (1.1):

$$I_{DS(lin)} = \frac{W}{L} \mu C_i (V_{GS} - V_{TH}) V_{DS} \quad (1.1)$$

where W and L are the channel width and length, μ is the mobility in linear regime, C_i is the insulator capacitance per unit area, V_{GS} is the gate voltage, and V_{TH} is the threshold voltage. μ is the most important parameter in OTFTs. In linear regime, μ can be calculated using equation (1.2):

$$\mu_{lin} = g_m \frac{W}{L} \frac{1}{C_{OX}} \frac{1}{V_{DS}} \quad (1.2)$$

here, g_m can be calculated as equation (1.3):

$$g_m = \left(\frac{\partial I_{DS}}{\partial V_G} \right)_{maximum} \quad (1.3)$$

where g_m is transconductance, represents the maximum value of modulation of V_{GS} to I_{DS} .

There are two important electrical parameters to describe the electrical properties of the transistors: the subthreshold slope SS and on/off current ratio I_{on}/I_{off} . Figure 1-11 shows a typical transfer characteristic of a p-type OTFT. The subthreshold slope corresponds to the difference of gate voltage values when the increase of drain current is equal to one decade. The I_{on}/I_{off} ratio presents the difference between off state and on state current.

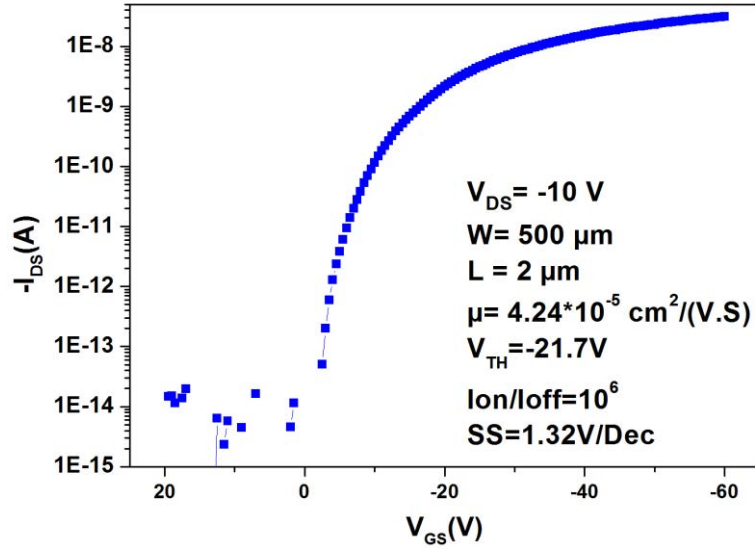


Figure 1-11: Typical transfer characteristics of a p-type OTFT.

As V_{DS} continues increasing, when $|V_{DS}| > |V_{GS} - V_{TH}|$, the voltage drop at drain decreases to a point which it falls to zero. At this point, which occurs the drain voltage approaches the gate voltage, holes close to the drain are depleted, leading to a pinch off in the conducting channel, and I_{DS} becomes independent of the drain bias. This regime is called saturation regime. The saturation current can be approximated as equation (1.4):

$$I_{DS(sat)} = \frac{W}{2L} \mu C_i (V_G - V_{TH})^2 \quad (1.4)$$

μ in saturation regime can be calculated as equation (1.5):

$$\mu_{sat} = \frac{2L}{WC_i} \left[\frac{\partial(\sqrt{I_{DS}})}{\partial V_G} \right]^2 \quad (1.5)$$

IV.2 Structures of OTFTs

At least four layers are required to fabricate for an OTFT. Such layers have specific properties that could be listed as follows:

- **Gate:** It is a conductor, and usually it's heavily doped silicon or metal material depending on the requirement. The heavily doped silicon is used as gate for processing convenience in many studies. However, the drawback of silicon gate will be explained in the following.
- **Insulator:** Thermally grown silicon dioxide is used as insulator in most cases. Recently organic materials such as polyvinylpyrrolidone (PVP), poly (methyl methacrylate) (PMMA), polystyrene (PS) used as insulator have also been reported ^[106].
- **Drain and Source:** They are also conductors, and metal is used as drain and source, normally. The main requirement for this layer is the “electrical affinity” with the semiconductor, as explained above. For instance gold is well adapted with pentacene. Moreover, this layer could be chemically modified in order to improve the properties of OTFT.
- **Organic semiconductor:** As listed in Table 1-1, many materials have been reported used as organic semiconductor.

Many combinations between those layers can be used to fabricate OTFT as shown in Figure 1-12. Each structure has advantages and drawbacks. In this section, four common structures will be described including their advantages and drawbacks. Structure specificity is necessary to define which one is the most convenient structure for the considered applications.

In order to classify the structures a well-known classification in “TFTs community” has been followed. For instance, if the gate is under dielectric and the drain/sources electrodes are under the semiconductor; the structure is called: bottom-gate and bottom contact.

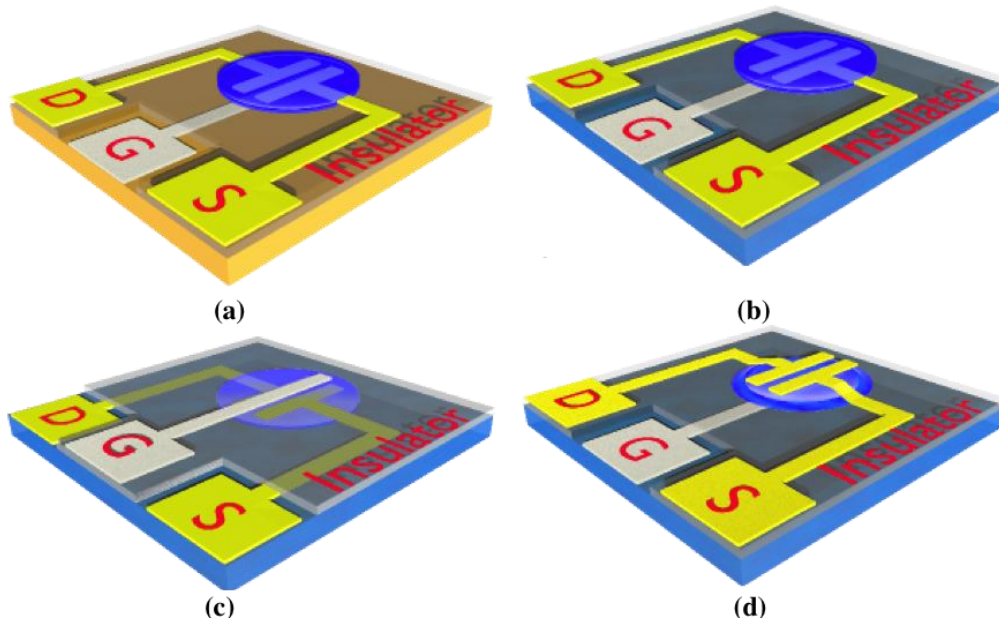


Figure 1-12: Common OTFTs structure. (a) Back-gate and bottom-contact, (b) Bottom-gate and bottom-contact, (c) Top-gate and bottom-contact, and (d) Bottom-gate and top-contact.

The most commonly used structure is the back-gate and bottom-contact type as illustrated in Figure 1-12(a). The heavily doped silicon substrate is used as gate due to the advantage that it is easily “processable” (less processing steps are required) and SiO_2 as insulator can be thermally grown. This well-known dielectric allows obtaining a good interface between the gate and the insulator. Indeed, a smooth interface between SiO_2 and the semiconductor is also performed. In contrary, drawbacks could also be listed. As the same gate voltage is applied to the overall substrate, circuits which requiring individually addressed transistors can't be achieved. Moreover, a huge overlap between gate and drain/source electrodes is obtained that negatively impact OTFT electrical behavior. As consequence, this structure is not suitable to optimize OTFT electrical behavior. This work will not deal with this structure.

A bottom-gate and bottom-contact type OTFT is shown in Figure 1-12 (b). Different from the previous one, this structure uses a patterned gate electrode, resulting in significant reduction of overlap capacitance. Besides, many substrates can be considered such as glass, plastics... Moreover, polymeric insulator can be used. Solvent compatibility among layers is the main concern for inkjet printed transistors, i.e. the deposited layers can be re-dissolved by subsequent printing if non-orthogonal solvent were used. Thus, this structure is favorable for printing process, as semiconductor is printed at last, avoiding solvent “attack” from other layers.

Structures shown in Figure 1-12 (c) and (d) are often used because it is reported that their electrical characteristics is improved compare to the other OTFT configurations ^[107]. However, because of processing conditions those structures have not been used in this work (i.e., inkjet printing). The structure of Figure 1-12 (c) is challenging in terms of process integration, as the semiconductor layer is deposited as the second layer. The subsequent printing and heating steps can potentially degrade the semiconductor.

Fig 1-12 (d) shows that drain and source electrodes are deposited at the last process step. Patterning such electrodes can be obtained using two techniques: lithography or shadow masking. Lithography techniques needs solvent that is not required for the reasons described previously. Using shadow masking does not offer the possibility to align source-drain and gate accurately.

In this work, the bottom-gate and bottom-contact structure is used to fabricate solution processed OTFTs. The following strategy should be adopted:

- Determining the best experimental parameters of organic semiconductor deposition. Drop casting method has been used to optimize experimental parameters due to the fact that it is the most convenient method to achieve systematic study. Lithographical structure has been used to optimize experimental parameters due to its reproducibility. As a consequence, “photo-patternable” but also printable polymeric insulator should be used.
- Optimizing bottom-gate and bottom-contact inkjet printing structure.
- Fabricating fully-inkjet-printed OTFTs.

V Characteristics and parameters extraction of OTFTs

V.1 Characteristics of OTFTs

V.1.1 Transfer characteristics

The transfer characteristics corresponds to the measurement of current I_{DS} as a function of the gate voltage V_{GS} for a constant drain voltage V_{DS} . Figure 1-13 presents a typical transfer characteristic of a p-type OTFT. From this curve, “3 operation zones” of OTFT can be defined.

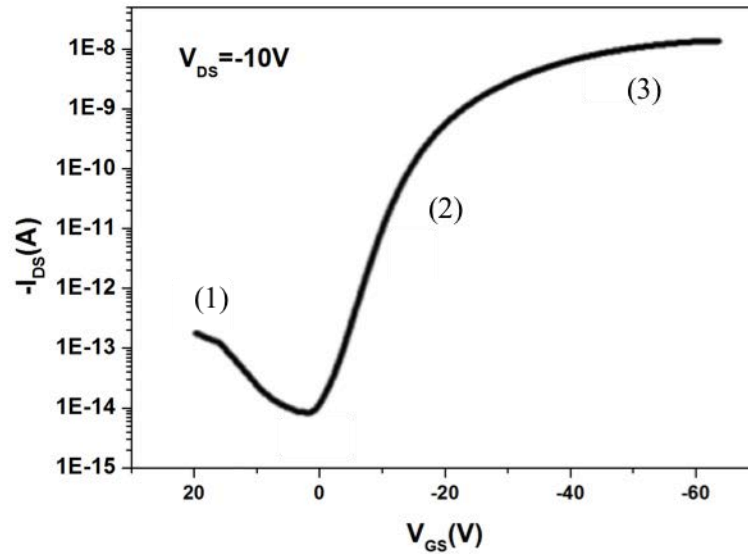


Figure1-13: Typical transfer characteristic of p-type OTFT on semi-logarithmic scale.

The first area shows the OTFT behavior in off state with a current ($I_{DS}=I_{OFF}$). The low value of current is primarily due to the electrical conductivity of the active layer, which should be as low as possible in order to decrease this current. An increase of this current under an inverse gate voltage (positive in the case of p-type transistor as shown in Figure 1-13) can be observed sometimes, is due to the activation of the carriers by the reverse electric field.

The second area shows that the formation of the channel and the drain current increases rapidly with the gate voltage.

The third area shows the on state of OTFT ($I_{DS} = I_{ON}$).

V.1.2 Output characteristics

The output characteristics corresponds to the measurement of current I_{DS} as a function of the drain voltage V_{DS} for a constant gate voltage V_{GS} . Figure 1-14 shows a typical output characteristic of a p-type OTFT. This figure shows clearly the linear regime under a weak drain voltage and the saturation regime occurs when V_{DS} becomes larger than $|V_{GS} - V_{TH}|$. This figure also shows the drain current variation with different gate voltages.

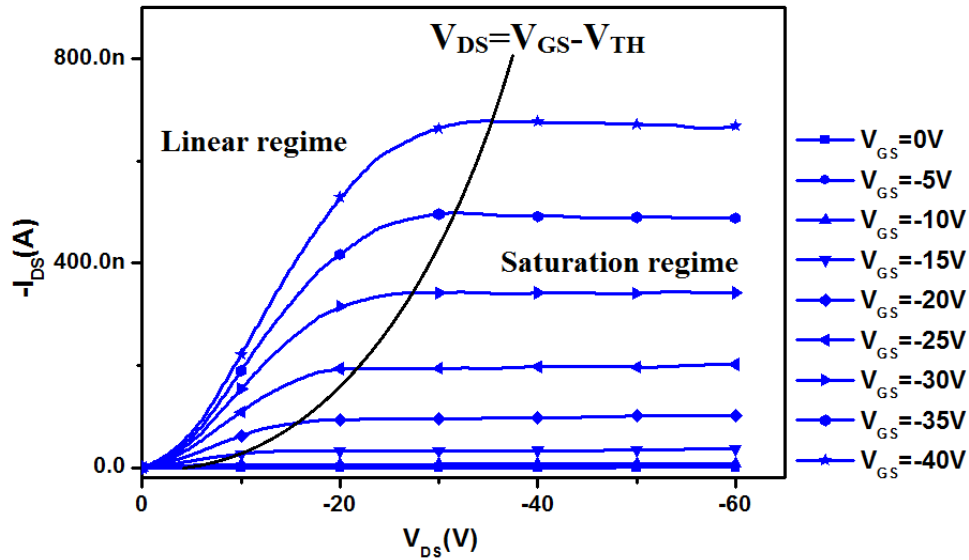


Figure 1-14: Output characteristic of a p-type OTFT.

V.1.3 Successive measurements of the transfer characteristics

The successive measurements of the transfer characteristics corresponds to the measurement of current I_{DS} as a function of the gate voltage V_{GS} for a constant drain voltage V_{DS} . The transfer curves are measured at least two times in succession. Figure 1-15 presents typical successive measurements of the transfer characteristic for two times of a p-type OTFT.

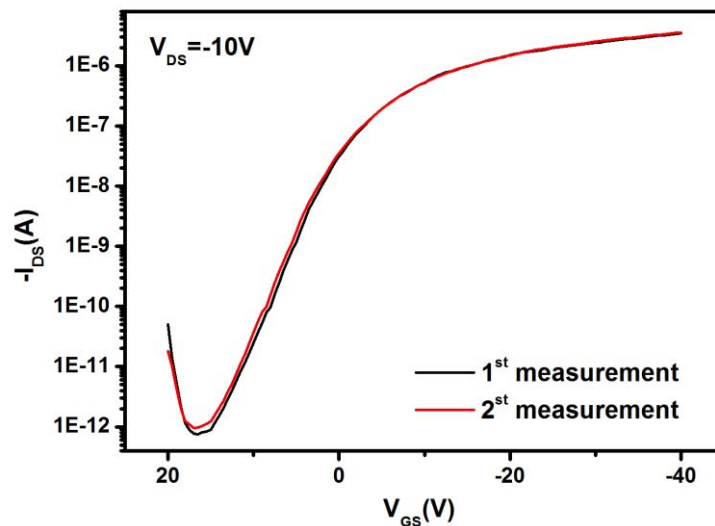


Figure 1-15: Successive measurements of the transfer characteristic of a p-type OTFT.

V.1.4 Hysteresis characteristics

The hysteresis characteristics corresponds to the measurement of current I_{DS} as a function of the gate voltage V_{GS} for a constant drain voltage V_{DS} . The measurement of the transfer characteristic is performed when gate voltages increases then when it decreases. The difference between these two curves is called hysteresis. Figure 1-16 shows a typical hysteresis characteristic of a p-type OTFT. A difference is observed between these two curves.

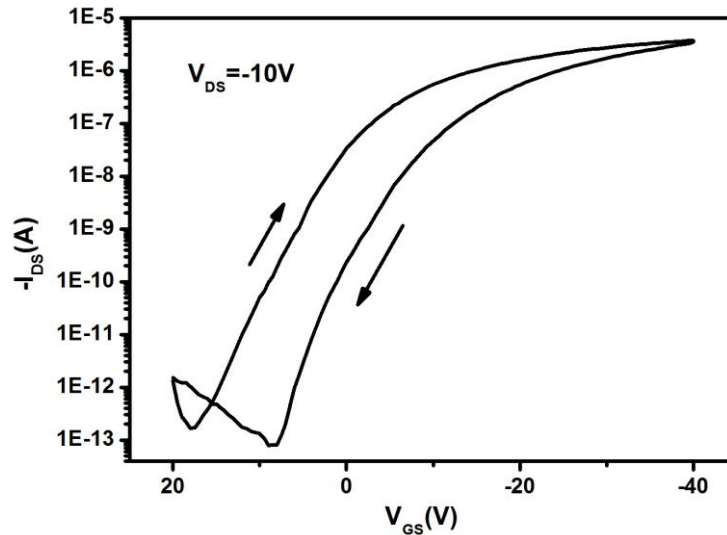


Figure 1-16: Hysteresis characteristic of a p-type OTFT.

The hysteresis may be related to the charge trapping and de-trapping at the interface between the active layer and the insulator layer, or in the insulator layer.

V.1.5 Bias stress characteristics

The bias stress characteristics corresponds to the measurement of current I_{DS} as a function of the gate voltage V_{GS} for a constant drain voltage V_{DS} . The transfer curves are measured under a bias stress. Applying a high gate voltage (negative voltage in a p-type OTFT as shown in Figure 1-17) during a long time can accelerate the test of reliability of OTFT. Figure 1-17 presents a typical successive bias-stress characteristic of a p-type OTFT.

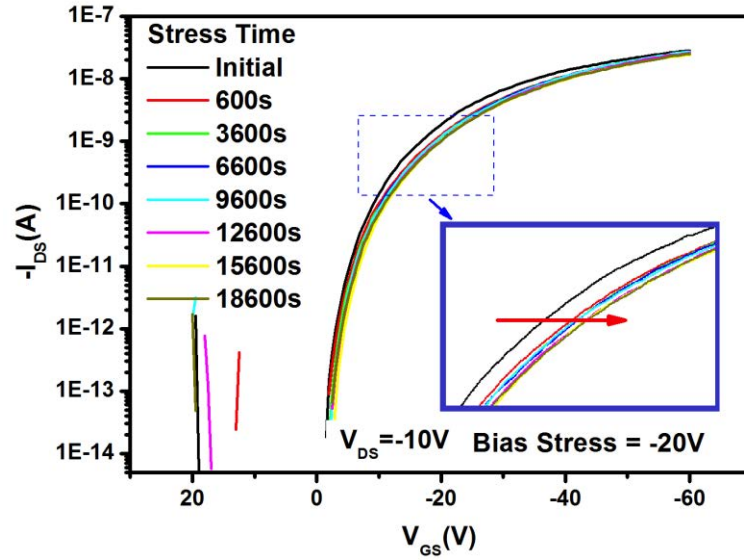


Figure 1-17: Bias stress characteristic of a p-type OTFT.

Gate bias-stress often induces threshold voltage shift mainly due to defect creation in semiconductor and charge trapping in insulator layer.

V.1.6 Gate leakage current characteristics

The gate leakage current characteristics corresponds to the measurement of current I_{GS} as a function of the gate voltage V_{GS} for a constant drain voltage V_{DS} . Figure 1-18 presents a typical gate leakage current characteristic of a p-type OTFT.

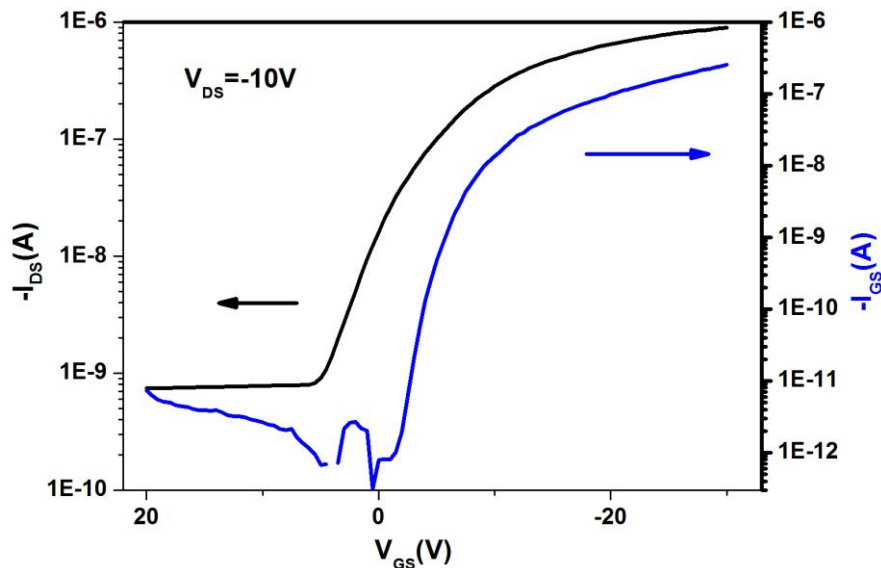


Figure 1-18: Gate leakage current characteristic of a p-type OTFT.

In conclusion, the stability of OTFT is related to the successive transfer characteristics, hysteresis, bias-stress and gate leakage current characteristics.

V.2 Parameters extraction of OTFTs

Threshold voltage V_{TH} , transconductance g_m , subthreshold slope SS and I_{on}/I_{off} ratio can be obtained using the transfer characteristics. As shown in Figure 1-19 (a), by plotting the drain current I_{DS} as a function of gate voltage V_{GS} in the linear coordinate, the threshold voltage V_{TH} is typically defined as the X-intercept of the tangent line extrapolated in linear regime of the I_{DS} - V_{GS} curve. The transconductance g_m is the maximum value of the slope of I_{DS} - V_{GS} curve (the extraction is shown in Figure 1-19 (b)). SS is defined as the maximum slope of the $\log(I_{DS})$ - V_{GS} curve, with the unit of volt-per-decade (V/Dec) (the extraction is shown in Figure 1-19 (c)). I_{on}/I_{off} is defined by the ratio of the maximum current divided by the minimum current observed in the transfer characteristics (the extraction is shown in Figure 1-19 (d)).

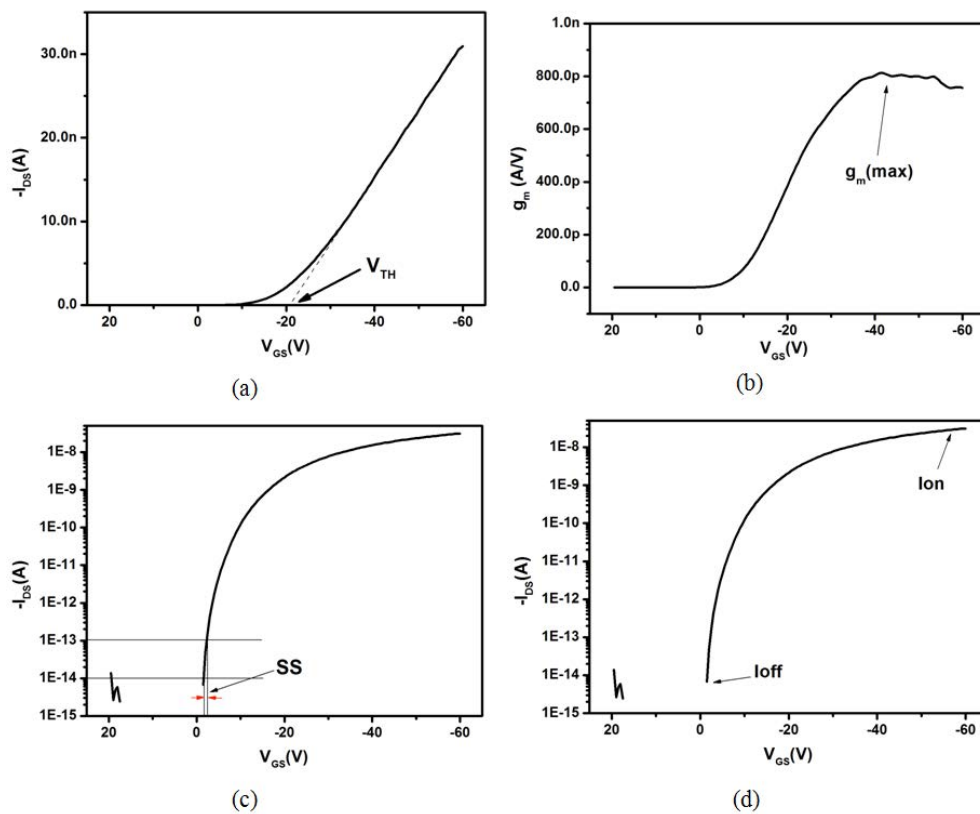


Figure 1-19: Parameters extraction from a p-type OTFT. (a) Extraction of V_{TH} , (b) Extraction of g_m , (c) Extraction of SS, and (d) Extraction of I_{on}/I_{off} .

VI Thesis organization

Solution-processed OTFTs are promising technique for the fabrication of electronic devices on a very low cost and large area substrate like paper. The focus of this thesis concerns using inkjet-printing in order to fabricate high electrical performance and better stability OTFTs on flexible substrates.

In the first chapter, the development of OTFT is introduced. The principle and deposition methods including vacuum deposition and solution processing of organic semiconductor are described. Afterwards, a brief description of solution-processed OTFTs is given: the basics, the structure, the characteristics and parameters extraction of OTFTs are detailed.

The second part of this thesis consists in optimizing inkjet-printing parameters of organic semiconductor materials deposition by using drop-casting method. First, issues of solution processing, including solvent effect, drying and annealing temperature effect, and SAMs effect are presented. N-type and p-type OTFTs will be discussed in detail. Depending on the issues of solution processing mentioned in the first chapter, solvent effect, drying and annealing temperature effect, and SAMs effect will be presented to optimize parameters.

Chapter 3 describes inkjet-printing technology in order to fabricate fully-solution-processed OTFTs. In this chapter, introduction of printed electronics is firstly presented, including inkjet print technique and methodology. Then the printability of OTFT functional materials is discussed. OTFTs are fabricated using inkjet printing, and electrical characteristics are presented.

Chapter 4 describes a method in order to improve the performance of solution-processed OTFTs. In this chapter, a polymeric gate insulator functionalized with 1-aminoanthraquinone is presented in order to achieve “a better interface”, and to improve the electrical performance, including OTFTs stability. Four main factors at the semiconductor-insulator interface are measured to confirm the improvement. Electrical characterization and bias stress measurement are extracted.

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**Chapter 2: N-type and p-type drop casted
organic semiconductors on OTFT: processing
and characterization**

I Introduction

As mentioned in the first chapter, thin film transistor is a stack of different films where not only the quality of each film but also the interface in-between determine the performance of the transistor. Then, processing TFTs by solution technique needs to determine the main deposition parameters influencing the physical and electrical quality of the films and the technological steps to improve the interface between these films.

Material constituting the films is deposited in solution. The used solvents can have some influence on the deposition.

Deposited films are in solution. The drying conditions reaching solid film can have some influence on the quality of the film.

Sometimes the films need to be annealed after the drying steps in order to improve their physical organization. The annealing conditions can have also some importance.

Finally, stacking a film on another one needs to adapt its surface to the material of this other film. The conditions of this adaptation have also to be studied carefully.

This chapter starts with an introduction on the influence of each of these parameters that is the same whatever the solution technique (spin coating, drop casting, inkjet printing, ...). Then, this influence is evaluated through the fabrication of bottom-gate/bottom-contact OTFT by drop casting. In this evaluation, C₆₀ and Tips-pentacene will be respectively used as n-type and p-type semiconductor.

Drop-casting technique is used firstly due to its easiness process compared to inkjet printing. Determining the influence of each parameter using drop casting will lead to prepare the conditions of the deposition by inkjet printing that is the final purpose.

II. Issues of solution processing

II.1 Effect of solvents

- **The case of C₆₀**

In this work, C₆₀ is used as n-type organic semiconductor material, because C₆₀ is a very promising material that provides high electron mobility (up to 1 cm²/Vs)^[1-3]. However, it is difficult to obtain uniform C₆₀ thin-film layers prepared by a solution process. The difficulty of producing a C₆₀ thin film layer by solution process is attributed to the low solubility of C₆₀

in organic solvents ^[4]. C₆₀ is essentially insoluble in polar and H-bonding solvents like acetone, ethanol. It is sparingly soluble in alkanes like pentane, hexane, and decane. Note that, the solubility increasing with the number of carbons. The solubility in chloroalkanes is generally higher than in alkanes. C₆₀ is appreciably soluble in aromatic solvents, while substitution with methyl and methoxy groups increases the solubility, with nitro and nitrile reduces it. Solubility increases in going from benzene to toluene. Substitution with chlorine increases solubility, and introduction of a second chlorine results in a substantial increase in solubility. Solubility of dichlorobenzene is better than that of chlorobenzene. However, third chlorine results in a sharp decrease in solubility. Table 2-1 presents the chemical structure, physical properties and reported solubilities of different solvents.

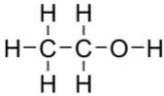
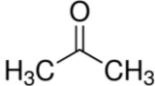
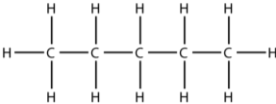
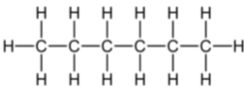
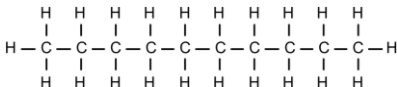

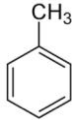
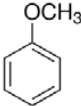
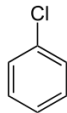
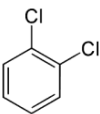
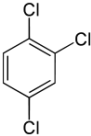
Solvent	Chemical Structure	Boiling Point (°C)	[C ₆₀], mg/mL
polars			
ethanol		78.4	0.001
acetone		56	0.001
alkanes			
n-pentane		36	0.005
n-hexane		68	0.043
n-decane		174	0.071
benzenes			
benzene		80	1.7
toluene		111	2.8
anisole		154	5.6
chlorobenzene		131	7
1,2-dichlorobenzene		180	27
1,2,4-trichlorobenzene		214	8.5

Table 2-1: Solubility of C₆₀ in various solvents.

Some groups have used functionalized C₆₀ derivatives to enhance the solubility [5-7]. However, the performance of FETs with C₆₀ derivatives was quite poor compared with that of OTFTs with vacuum-deposited layers of C₆₀. Thus, there have been only a few reports of C₆₀ OTFTs fabricated by solution process. The solvent nature used in order to dilute C₆₀ in solution-processed OTFTs is critical.

● **The case of Tips-pentacene**

Tips-pentacene is used as p-type organic semiconductor in this work. The thin-film morphology and crystal of Tips-pentacene were significantly depending on the solvent, which have a strong impact on electrical properties of OTFT.

Choi *et al* [8] investigated the solvent effect of Tips-pentacene OTFTs with four different solvents (chlorobenzene, p-xylene, toluene, and chloroform). The boiling points were 131°C, 138°C, 110°C, and 61°C, respectively. As can be seen in Figure 2-1, the grain size of pentacene layer is larger for solvents with higher boiling point. The Tips-pentacene film obtained using chlorobenzene solution showed the highest crystallinity and the film obtained using chloroform showed the lowest crystalline phase. Consequently, as shown in Figure 2-2, the best electrical performances can be obtained with devices fabricated using chlorobenzene as solvent.

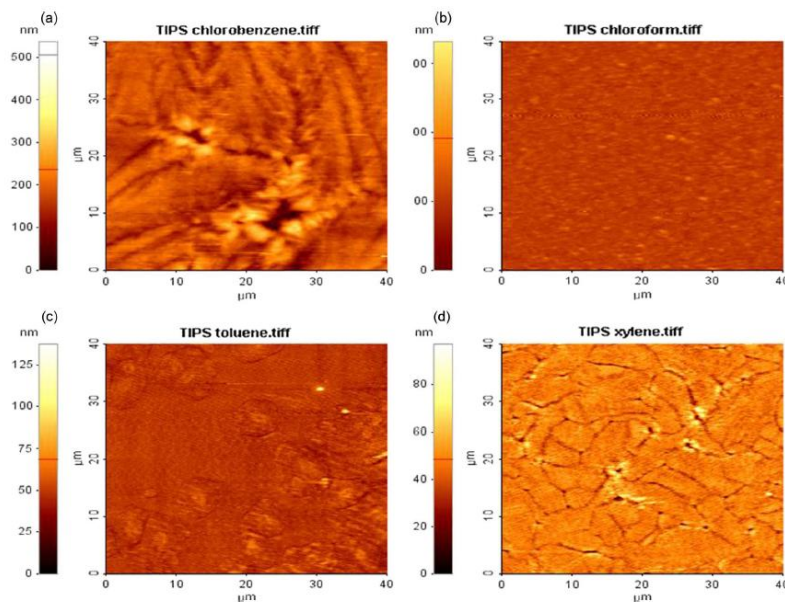


Figure 2-1: AFM images of pentacene layer spin coated from different solvents:
(a) Chlorobenzene, (b) Chloroform, (c) Toluene, (d) p-xylene [8].

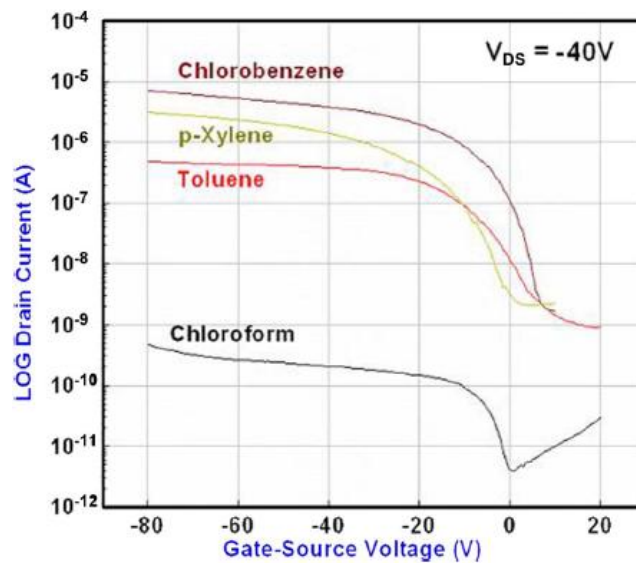


Figure 2-2: Transfer characteristics of Tips-pentacene OTFTs fabricated with different solvents [8].

Kim *et al* [9] have also investigated the solvent effect of Tips-pentacene OTFTs with four different solvents (toluene, chlorobenzene, tetrahydrofuran, and chloroform). The boiling points were 110°C, 131°C, 66°C, and 61°C, respectively. Solvent evaporation of high boiling point solvents was lower than lower boiling point solvents. A lower solvent evaporation allows more structural rearrangement prior to film solidification. Thus, Tips-pentacene allows obtaining larger and more crystalline grains.

Kim *et al* [10] have investigated the dependence of electrical properties of inkjet-printed Tips-pentacene OTFTs on the solvent boiling point used in the inkjet printing. Two kinds of organic solvents were employed in the device fabrication: chlorobenzene and anisole. The OTFT fabricated using anisole has shown higher field-effect mobility than using chlorobenzene. Tips-pentacene in high boiling point solvent exhibits a dendrite-like structure. In the contrary, Tips-pentacene in low boiling point solvent exhibits an amorphous structure.

Lee *et al* [11] have examined the effects of the solvent on the morphology and structure properties of Tips-pentacene deposits using solvents with different boiling points: toluene, chlorobenzene, dichlorobenzene, and trichlorobenzene. As the solvent boiling point increased, the field-effect mobility increased. Furthermore, a mixed solvent containing chlorobenzene and dichlorobenzene was also examined. Equal masses of chlorobenzene and dichlorobenzene produced large crystals with an optimal pattern size. Chlorobenzene induced contact line

pinning of the droplets, whereas dichlorobenzene provided a long evaporation time that permitted crystallization of the Tips-pentacene molecules.

In conclusion, the solvents have significant impact on the thin-film morphology and crystal of semiconductor. In this work, for the reasons described in this section, only high boiling point solvents have been used (i.e., boiling point > 110°C).

II.2 Effect of drying and annealing temperature

When the drying temperature is a lower, the growth of the semiconductor film should be slower and the ordering of the molecular should be better. Furthermore, the semiconductor layer is more uniform when the drying temperature is lower due to the coffee ring effect [12].

The coffee ring effect, also named coffee stain effect, was first explained by Deegan [13], stating that the non-uniform drying of the droplet can lead to an excess of solute at the edges. This is due to higher evaporation at the pinned contact lines than in the center. The coffee ring effect is detrimental to film formation, as thicker films are deposited at the edges relatively. Reducing substrate temperature can partially overcome the coffee ring. In such case, the cooled substrate can retard the rim evaporation of coffee ring formation. Figure 2-3 illustrates the principle of coffee ring effect.

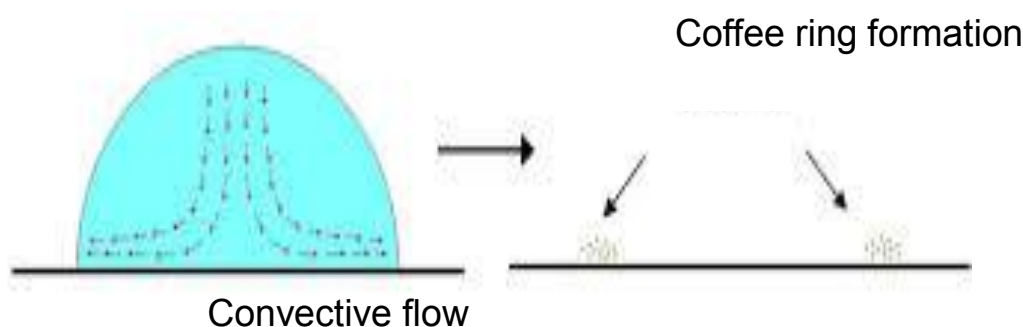


Figure 2-3: Schematic illustration of the coffee ring formation.

Annealing also plays an important role in achieving OTFTs with excellent performance. Figure 2-4 extracted from literature, shows the mobilities of the devices fabricated on glass and flexible substrate as a function of annealing temperature [14]. It has been reported that electrical characteristics of OTFTs based on C₆₀, were dependent on the annealing temperature. In this case, the mobility reached a maximum value at 90°C. The decrease in mobility at annealing temperature higher than 90°C might be due to a change in

the crystalline structure or an increase in grain size. Figure 2-5 shows the atomic force microscopy (AFM) images of the C₆₀ films annealed at temperature ranging from 50 to 150°C. The average grain size increased when increasing the annealing temperature.

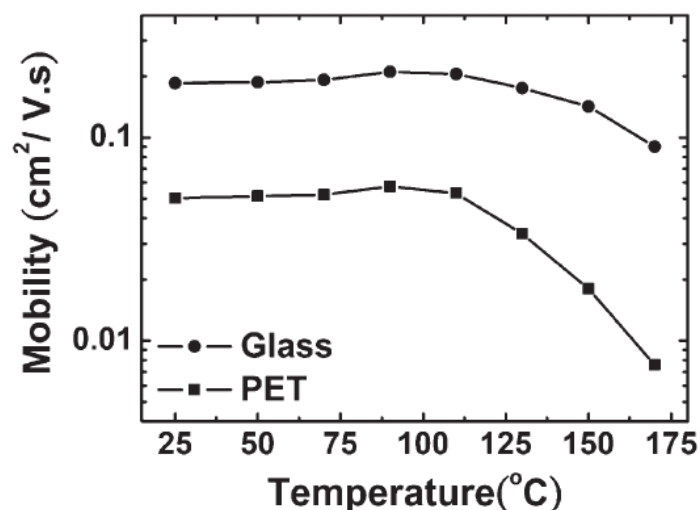


Figure 2-4: Mobilities of OTFTs featuring C₆₀ semiconductor films annealed at temperature between 25°C and 170°C [14].

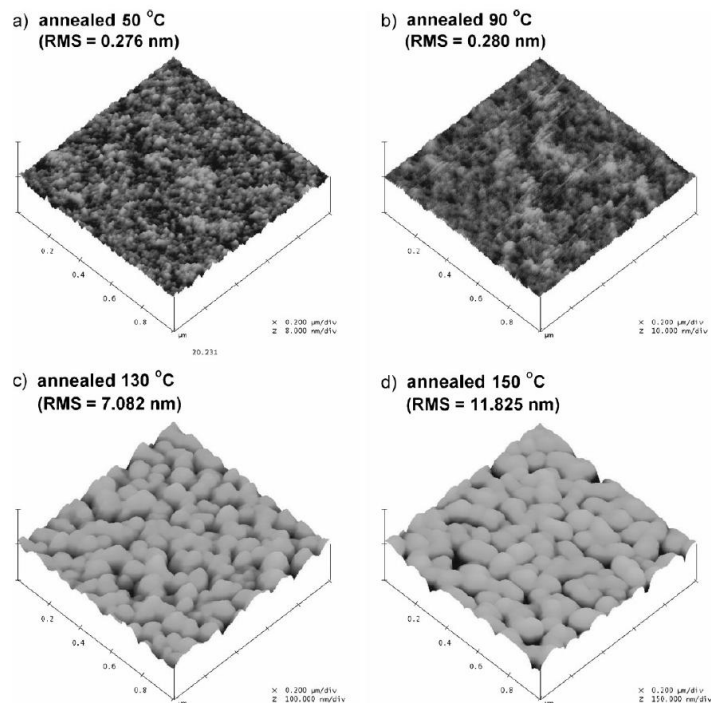


Figure 2-5: AFM images of C₆₀ thin films on ITO glass/PVP substrates annealed at 50°C, 90°C, 130°C and 150°C [14].

Bae *et al* ^[15] have reported the annealing effect of OTFTs based on Tips-pentacene. As shown in Figure 2-6, mobility decreases as annealing temperature exceeds 60°C, due to the fact that cracks were developed as shown in Figure 2-7.

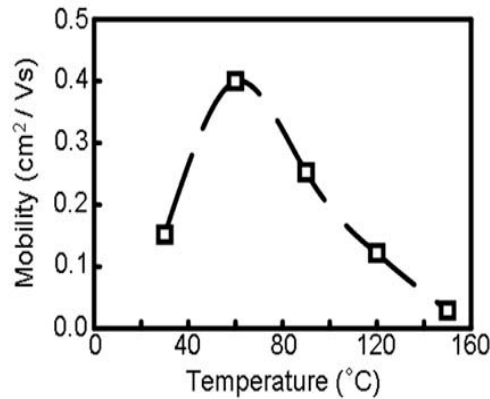


Figure 2-6: Mobility of Tips-pentacene as a function of annealing temperature ^[15].

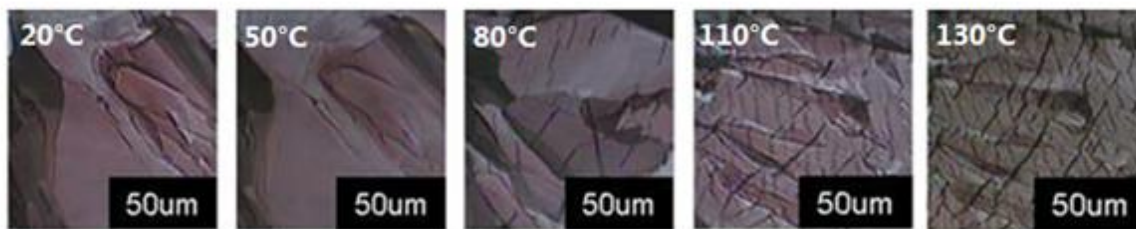


Figure 2-7: Images of X-ray diffraction peaks observed in the Tips-pentacene films annealed at various temperatures ^[15].

Note that these experiments will be also performed in this work in order to determine the optimum annealing temperature.

II.3 Effect of surface functionalization (SAMs)

Many researchers focus on OTFT performance improvement by modifying the gate dielectric ^[16-18]. Self-assembled monolayers (SAMs), due to its robust insulating properties, tunable thicknesses, and efficient solution processability, have gained significant attention.

Lin *et al* ^[19] firstly using SAM to modify the surface of the dielectric layer in order to improve the mobility of a pentacene transistor. After that, SAMs have been attracted to modify insulator surface ^[20]. The direct effect of SAMs is its impact on dielectric surface disorder, roughness of thin films ^[21-23] and on single crystals formation ^[24].

Bao *et al* [25] shown that the mobility is primarily depending on the crystalline structure of the first active monolayer at the vicinity of the dielectric interface. Thus, a SAM of hexamethyldisilazane (HMDS) was employed to modify the dielectric interface and a high mobility of $3.4 \text{ cm}^2/\text{Vs}$ was obtained.

Park *et al* [26] have reported the impact of SAMs on dielectric surface energy, which influences the morphology of the semiconductor thin film. Klauk *et al* [27] have obtained a high mobility of $3 \text{ cm}^2/\text{Vs}$ using SAMs.

SAMs also play an important role in single-crystal transistor. Takeya *et al* [28] have reported a high mobility of $40 \text{ cm}^2/\text{Vs}$ using SAM to reduce the number of interface states.

Besides, it was reported that SAMs has impact on the static charge and the trap states in the interface of dielectric, which relates to the threshold voltage and sub-threshold current [29].

III OTFTs processing

Bottom-gate/bottom-contact structure (see in Figure 2-8) was used to fabricate n-type and p-type OTFT, as described in chapter 1. Corning glass was used as substrate. The glass substrate was ultrasonically cleaned in acetone and alcohol baths during 10 minutes, respectively. 150 nm thick aluminum was thermally evaporated on glass substrate, and patterned by wet etching. 400 nm thick Su8 2000.5 was spin coated on glass substrate. Aluminum and Su8 were used as the gate electrode and insulator, respectively. Then, 50 nm thick gold was thermally evaporated and patterned by wet etching in order to define source and drain electrodes. Semiconductor (C_{60} and Tips-pentacene) was dissolved in solvents and drop casted on the active region with a volume of $2 \mu\text{L}$.

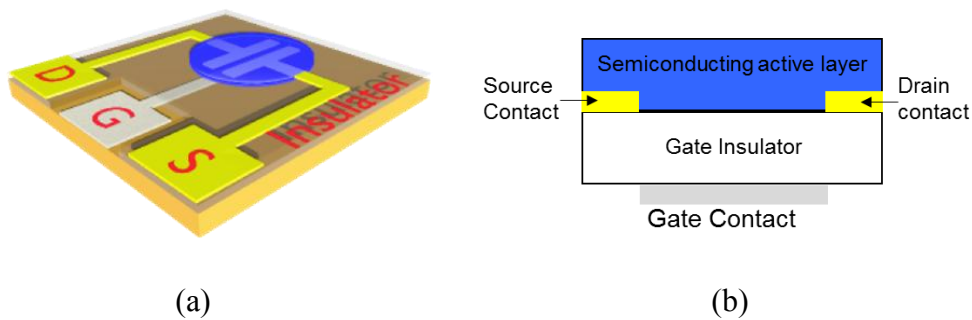


Figure 2-8: (a) Top-view and (b) cross-section of bottom-gate/bottom-contact structure of studied OTFTs.

Four identical cells are fabricated on the same substrates (5×5 cm squared glass). Each cell, as shown in Figure 2-9, contains sixteen transistors with various sizes. Five transistors have fixed channel width (i.e. 1000 μm) and various channel length (1 μm , 2 μm , 5 μm , 10 μm , and 20 μm). Three transistors have fixed channel length (i.e. 10 μm) and various channel width (250 μm , 500 μm and 1000 μm). Another transistor has channel length of 1 μm and channel width of 2000 μm .

The last step of the process is drop casting semiconductor. For all the experiments, 2 μL organic semiconductor drop is deposited on the active area as shown in Figure 2-9 (hatched area). A volume of 2 μL organic semiconductor drop allows covering all the transistors.

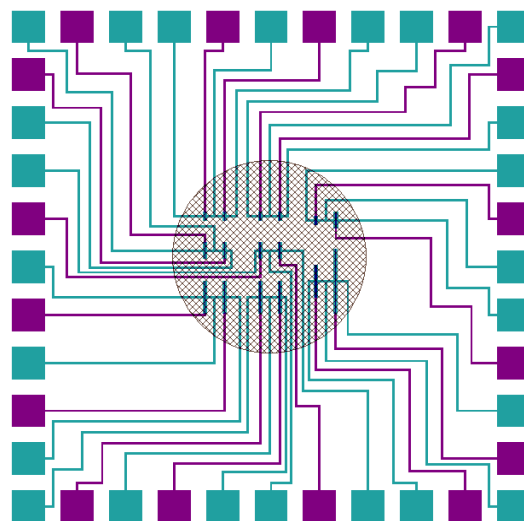


Figure 2-9: Schematic illustration of the lithograph mask with 16 transistors of various channel sizes. Hatched area is active region.

Note that, all the electrical measurements were carried on under N₂ environment. Electrical characterizations of both n-type and p-type OTFTs were performed using KEITHLEY 2636A equipment.

IV N-type solution processed OTFTs

IV.1 Effect of solvent of C₆₀ OTFTs

As described previously, the solubility of C₆₀ in organic solvents is poor^[4]. As listed in Table 2-1, dichlorobenzene is best choice of C₆₀ due to its molecular structure of benzene and two chlorine groups^[4]. In this work, dichlorobenzene was used as solvent in order to dilute C₆₀.

IV.2 Effect of drying and annealing temperature of C₆₀ OTFTs

IV.2.1 Drying temperature effect

As explained in last section, drying temperature is a well-known experimental parameter, which has a strong impact on semiconductor film formation^[30,31]. Consequently, organic semiconductor layer was deposited on OTFT at different substrate temperature: room temperature (25 °C), 45 °C, 65 °C and 85 °C in order to study drying temperature effect.

As shown in Figure 2-10 (a), (b), (c), and (d), in the center of the dried film, no evolution of C₆₀ grains size can be clearly distinguished even if drying temperature is different (from 25 °C to 85 °C). However, optical observations of drop edges clearly show that drying temperature have a strong impact on C₆₀ crystals size as shown in Figure 2-10 (e), (f), (g), and (h). Indeed, the more the temperature is, the less the crystal size is. Such observations are not possible in the center of C₆₀ film because it is less densely packed than in the edge.

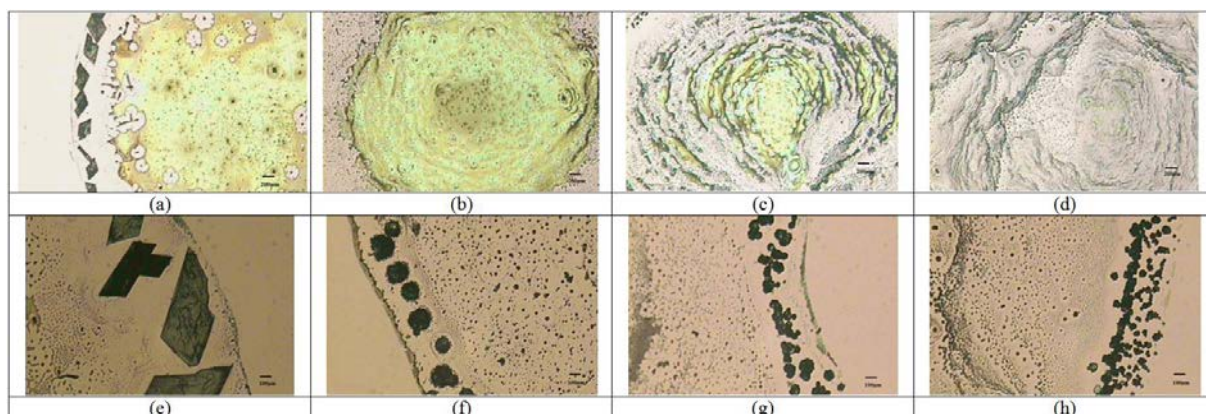


Figure 2-10: Optical picture of C_{60} film ((a), (b), (c) and (d)) and grain ((e), (f), (g) and (h)) obtained by different drying temperature: (a) (e) 25 °C, (b) (f) 45 °C, (c) (g) 65 °C, and (d) (h) 85 °C.

In more detailed level, the grain size decreases as drying temperature increases. When the C_{60} droplet is deposited on the insulator layer at room temperature (25 °C), it took about 10 minutes to complete the drying. However, when the droplet was deposited on a heated insulator layer (85°C). In this case, the drying is completed within 1 minute. Low drying temperature allows long time for solvent evaporation, which leads to big grain. Otherwise, high drying temperature allows short time for solvent evaporation and consequently small grains are obtained.

It is well-known that electrical performance of OTFT is impacted by semiconductor packing^[30]. It is also well-known that drying temperature has a strong impact on ordering of molecular^[31]. Such assertions can explain the OTFT electrical behavior of Figure 2-11.

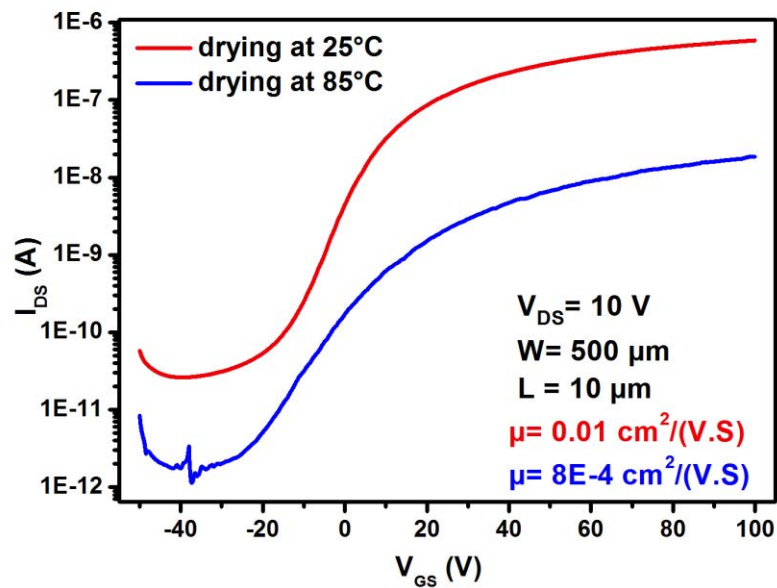


Figure 2-11: Transfer characteristics of C_{60} OTFTs dried at 25 °C and 85 °C.

As shown in Figure 2-11, device dried at 25°C shows the high mobility ($0.01 \text{ cm}^2/\text{Vs}$), $I_{\text{on}}/I_{\text{off}}$ ratio about 5 decades, and a threshold voltage of -3.8V. In contrast, dried at 85°C shows the low mobility ($8 \times 10^{-4} \text{ cm}^2/\text{Vs}$), $I_{\text{on}}/I_{\text{off}}$ ratio about 4 decades, and a threshold voltage of -20.3V. Such results proved that devices dried at low temperature exhibit better performance. Consequently, for the rest of the test of this work, drying temperature will be set at 25°C.

IV.2.2 Annealing temperature effect

Figure 2-12 shows transfer curves as a function of annealing temperatures.

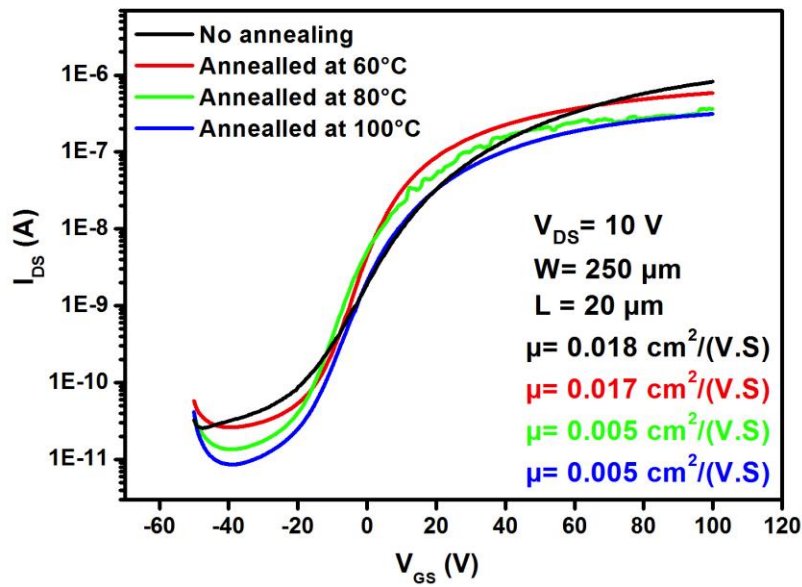


Figure 2-12: Transfer characteristics of C_{60} OTFTs as a function of annealing temperature.

Annealing temperature	μ (cm^2/Vs)	V_{TH} (V)	SS (V/dec)	$I_{\text{on}}/I_{\text{off}}$
25°C	0.018	31.5	12.64	10^5
60°C	0.017	7.57	10.15	10^4
80°C	0.005	9.38	8.53	10^4
100°C	0.005	14.23	10.29	10^4

Table 2-2: Summary of electrical characteristics of drop cast C_{60} OTFTs as a function of annealing temperature.

In Figure 2-12 and Table 2-2, the best electrical behavior is obtained for devices without annealing or annealed at 60°C. The device shows a higher mobility about 0.018 cm^2/Vs , $I_{\text{on}}/I_{\text{off}}$ ratio about 5 decades, a threshold voltage equal 31.5V. In contrast, annealed at 100°C shows a lower mobility about 0.005 cm^2/Vs , $I_{\text{on}}/I_{\text{off}}$ ratio about 4 decades, and a threshold voltage equal 14.23V. As summarized in Table 2-2, mobility decreases when annealing temperature exceeds 60°C. Consequently for the rest of this work, no annealing was performed for OTFT based on C_{60} .

V P-type solution processed OTFTs

V.1 Effect of Tips-pentacene solvent

Tips-pentacene is most popular p-type semiconductor used in the field of OTFT. This section focuses on the solvent impact on electrical performance of drop casted Tips-pentacene OTFT.

It is well-known that the morphology of the drop casted Tips-pentacene films is dependent on the solvent used to dissolve the semiconductor. For instance, as explained previously, high boiling point solvents exhibit larger crystals (several micrometers) than low boiling point solvents^[10].

Only high boiling point solvents were used in this work: chlorobenzene, dichlorobenzene, toluene, and anisole. The chemical structure and boiling point are presented in Table 2-3. Indeed, it has been judge no relevant to use low boiling point solvents such as chloroform that are not printable.

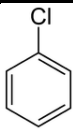
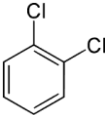
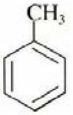
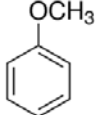
Solvent	Chemical structure	Formula	Boiling point (°C)
Chlorobenzene		C ₆ H ₅ Cl	131
Dichlorobenzene		C ₆ H ₄ Cl ₂	180
Toluene		C ₇ H ₈	110
Anisole		C ₇ H ₈ O	154

Table 2-3: Chemical structure and boiling point of four solvents.

Tips-pentacene (1.5% wt) was dissolved in such solvents and drop casted on Su8 in order to study their impact on semiconductor morphology. Figure 2-13 shows optical pictures obtained using polarized microscope.

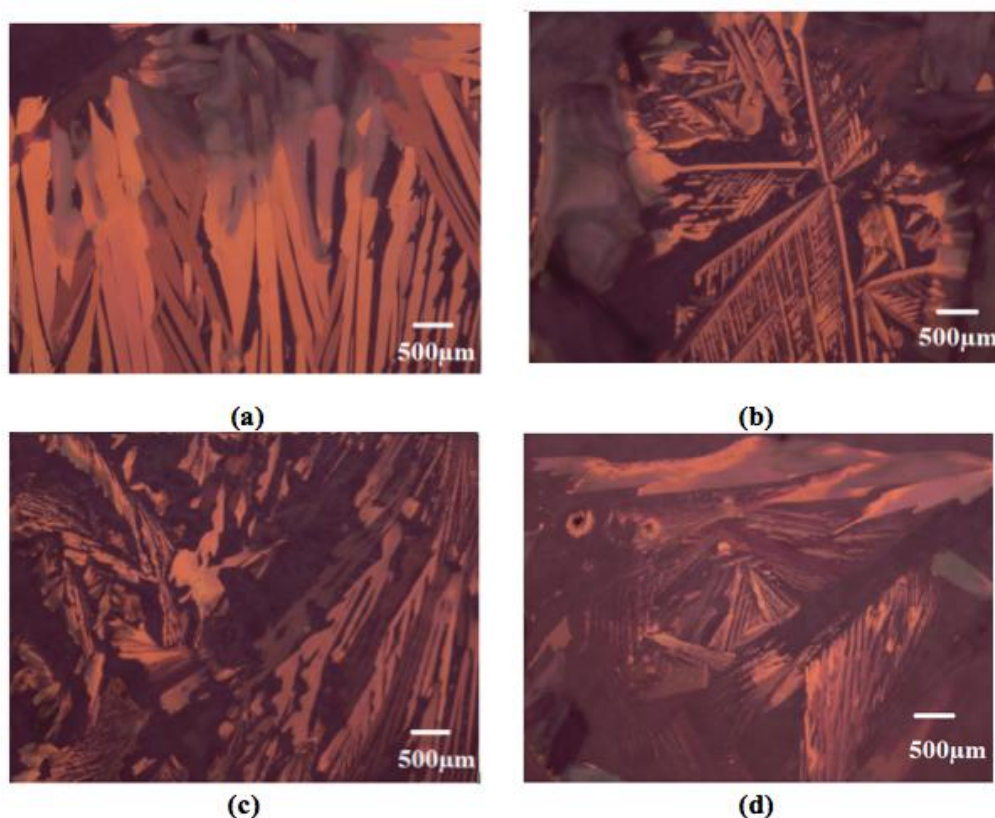


Figure 2-13: Polarized optical pictures of Tips-pentacene films drop casted using different solvents: (a) chlorobenzene, (b) dichlorobenzene, (c) toluene, and (d) anisole.

As shown in Figure 2-13, big crystals are observed from these four solvents due to the fact that high boiling point solvents allow long evaporation time. A low solvent evaporation allows more structural rearrangement before film solidification. Thus, Tips-pentacene allows to obtain larger and more crystalline grains. Note that, Tips-pentacene dissolved in chlorobenzene seems to exhibit more regular and uniform crystals than the other solvents.

1.5% wt Tips-pentacene dissolved in such solvents was drop casted on lithography structure as described previously, and dried at room temperature. Figure 2-14 shows the transfer characteristics of OTFTs as a function of solvents.

Both off-current and on-current are high when diluting in chlorobenzene and toluene. Their values are much lower when using anisole. The gate leakage current is very high when diluting in chlorobenzene and dichlorobenzene. Threshold voltages seem more or less similar. Subthreshold slope seems very low when using anisole.

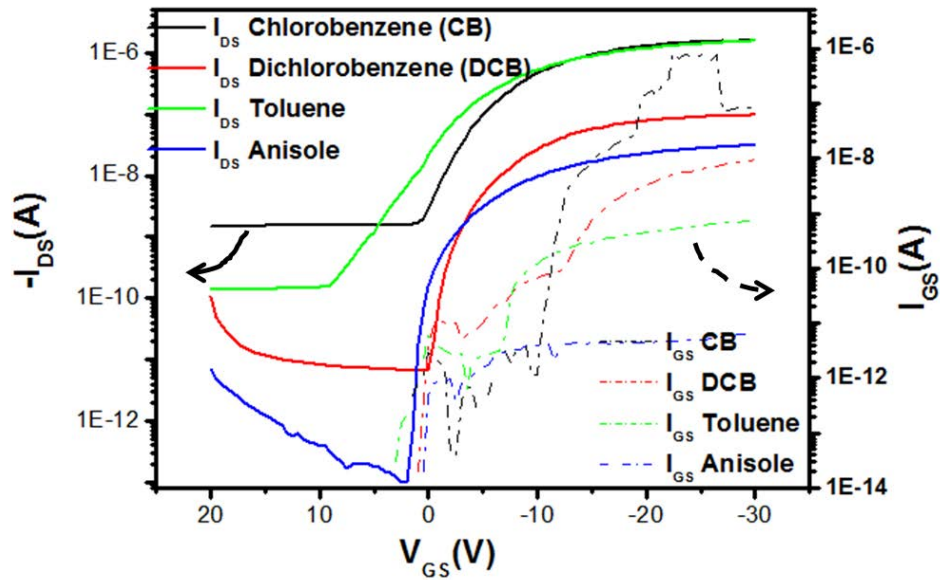


Figure 2-14: Transfer characteristics, Drain-Source current I_{DS} as a function of the Gate-Source bias V_{GS} , of same size Tips-pentacene OTFTs fabricated by diluting Tips-pentacene in different solvents and leakage Gate-Source current I_{GS} as a function of V_{GS} .

Solvent	Threshold voltage V_{TH} (V)	Subthreshold slope SS (V/dec)	Maximum Mobility (cm^2/Vs)
Chlorobenzene	-4.7	2.6	2.8×10^{-2}
Dichlorobenzene	-5.6	1	1.8×10^{-3}
Toluene	-2.8	3.7	2×10^{-2}
Anisole	-3.4	0.6	4×10^{-4}

Table 2-4: Electrical parameters of OTFTs fabricated by diluting Tips-pentacene in different solvents.

Table 2-4 summarizes the electrical parameters of these OTFTs. OTFTs fabricated with chlorobenzene present the highest mobility, however the other parameters are not so interesting. Anisole based OTFTs present the most interesting characteristics from V_{TH} and SS point of view. However the mobility is too low. The best compromise seems to be toluene based OTFTs. However the high SS indicates the presence of a lot of defects at the Su8/pentacene interface.

Before continuing the study, it seems more important now to focus on the gate leakage current and the off-drain current that are the key for understanding the performances. Figure

2-15 compares the on-current, the off-current and the gate leakage current of the transistors for the four solvents. The lowest on-current corresponds to the lowest off-current and to the lowest gate leakage current. From this current point of view, anisole solvent seems giving the best transistors with an on-current highest to the off current by 6×10^4 and to the leakage current by 5×10^3 . Transistors fabricated from chlorobenzene and dichlorobenzene have too much leakage current. These observations indicate a link between the performance in on-regime and the off-current and the gate leakage current.

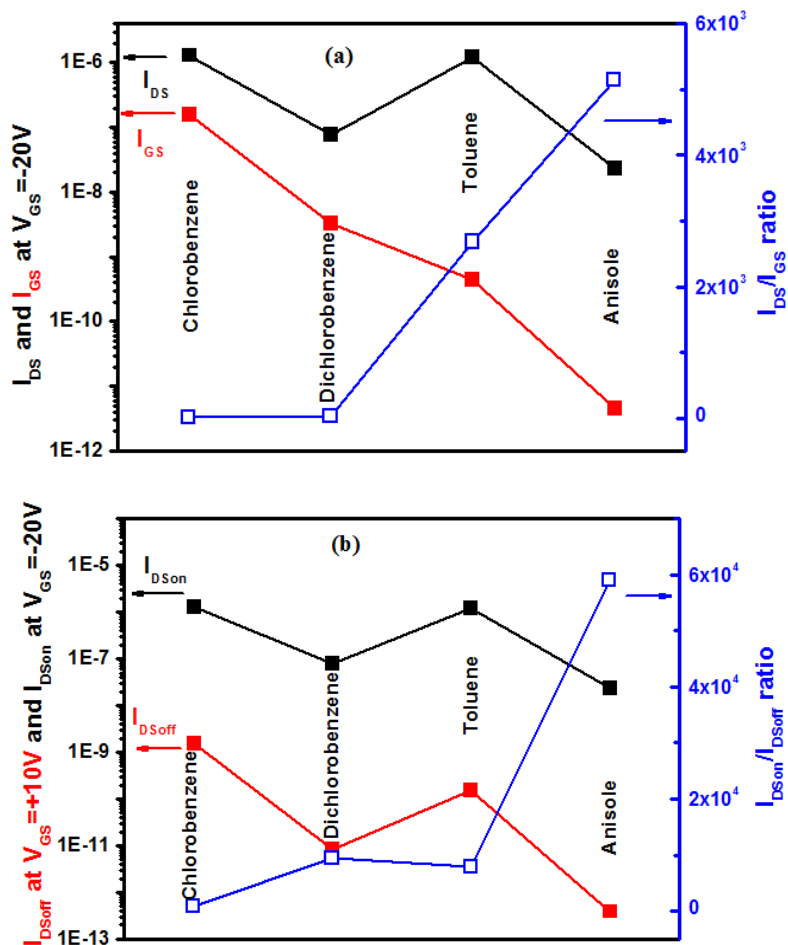


Figure 2-15: (a) On-current $I_{DS(on)}$ and gate leakage current I_{GS} in on-regime ($V_{GS} = -20V$), and their ratio for the four solvents. (b) On-current $I_{DS(on)}$ ($V_{GS} = -20V$) and off-current $I_{DS(off)}$ ($V_{GS} = +10V$), and their ratio for the four solvents.

Output characteristics of these four types of transistors are plotted in Figure 2-16. The characteristics saturate well and are well modulated by the gate voltage. Linear increase of the current at low V_{DS} is observed in all the characteristics even if the linearity is not so obvious when using chlorobenzene. Source contact can be considered as well injecting contact. When

using dichlorobenzene, the current starts positively at very low V_{DS} . It becomes negative at higher V_{DS} when increasing V_{GS} . In fact, this observation is true for the three other transistors as it can be seen in the zoom of the low V_{DS} region of the characteristics (Figure 2-17).

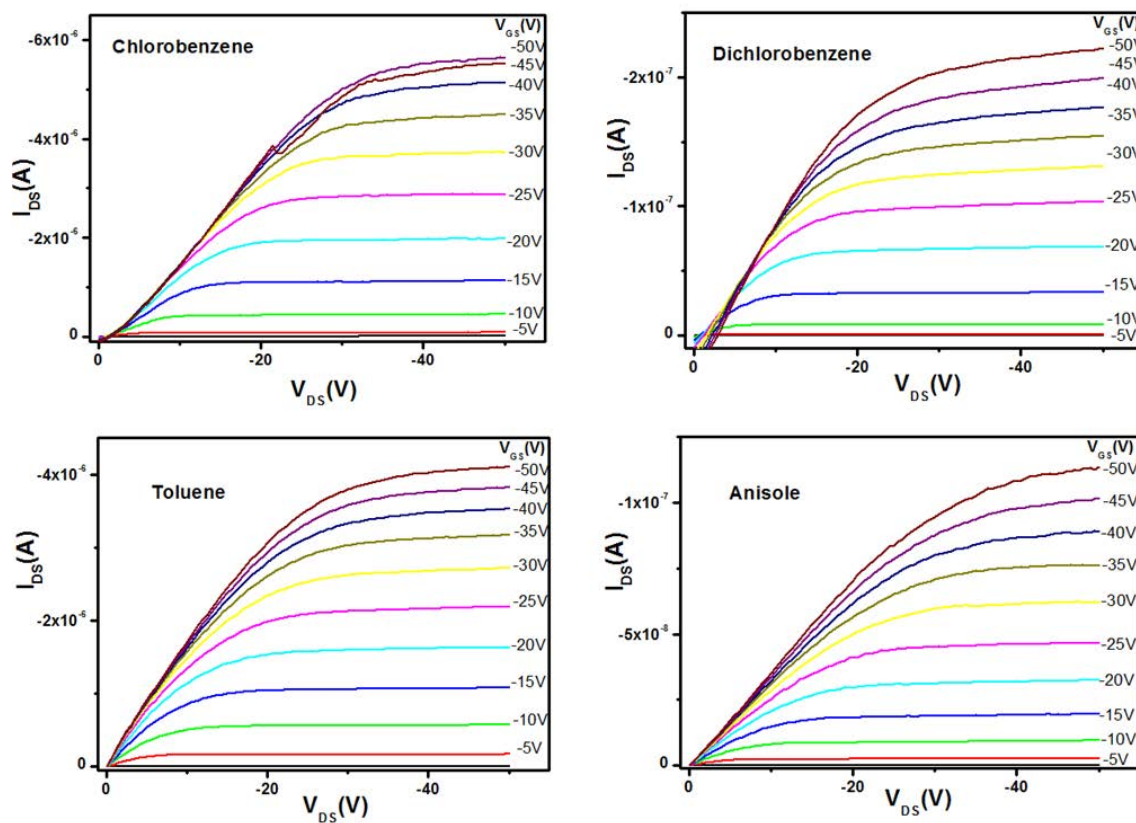


Figure 2-16: Output characteristics of same size Tips-pentacene OTFTs fabricated by diluting Tips-pentacene in chlorobenzene, dichlorobenzene, toluene and anisole solvents.

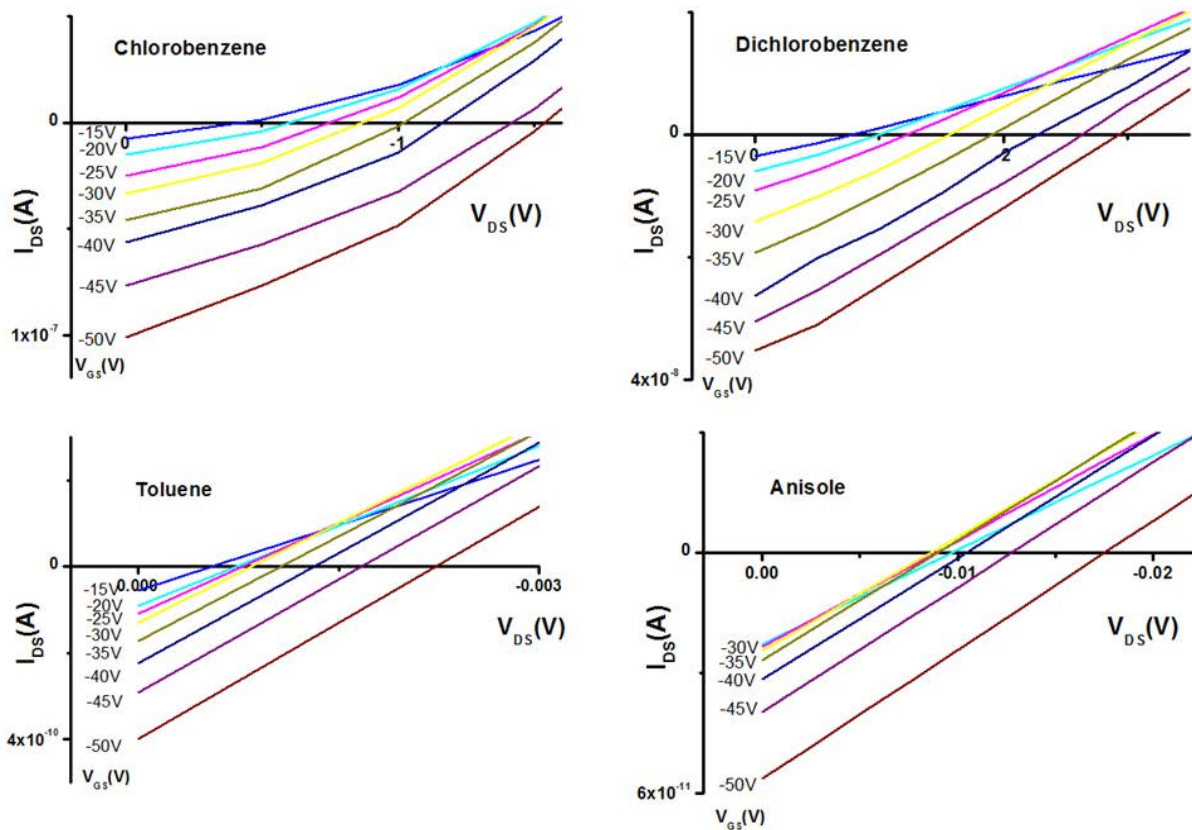


Figure 2-17: Zoom of the output characteristics of Figure 2-16 around very low values of the drain voltage. Drain current starts at positively increasing values when the gate voltage is more and more negative.

The starting positive values of I_{DS} are more important for the same gate voltage when moving from chlorobenzene, dichlorobenzene, toluene and anisole. This behavior follows that of the gate leakage current. Higher this starting positive value of I_{DS} is, more important is the gate leakage current I_{GS} .

The link between the starting positive values of I_{DS} and the gate leakage current can be explained through the scheme presented in Figure 2-18.

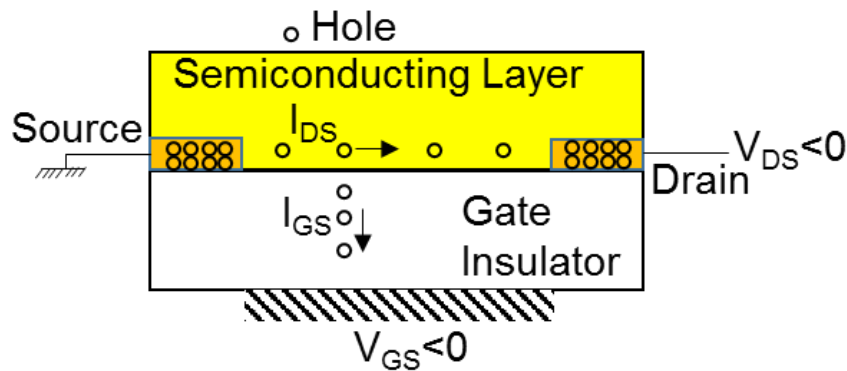


Figure 2-18: Scheme of the p-type OTFT showing the drain-source current I_{DS} and the gate-source current I_{GS} .

At very low value of V_{DS} , the gate field due to V_{GS} is more important than the Drain field due to V_{DS} . High number of holes flow in the direction of the negatively polarized gate. Due to this important flow, holes flow in the semiconductor to compensate the loss of holes in the channel, inducing positive drain-source current. When V_{DS} increases, drain field becomes more and more important inducing negative drain-source current.

Trying to understand the origin of the gate leakage current in the transistors fabricated from chlorobenzene higher than the leakage current in the transistors fabricated from anisole, it can be involved some reaction of the solvent of Tips-pentacene with the previously deposited Su8 gate insulator leading to an increase of the current flowing in this insulator. To confirm this hypothesis, Aluminum-Su8-Aluminum (Metal-Insulator-Metal) structures have been fabricated. Before depositing the top Aluminum electrode, a drop of chlorobenzene or of anisole have been deposited on previously spin-coated Su8 film. Figure 2-19 shows the current-voltage characteristics and the answer to a step of voltage of these MIM structures.

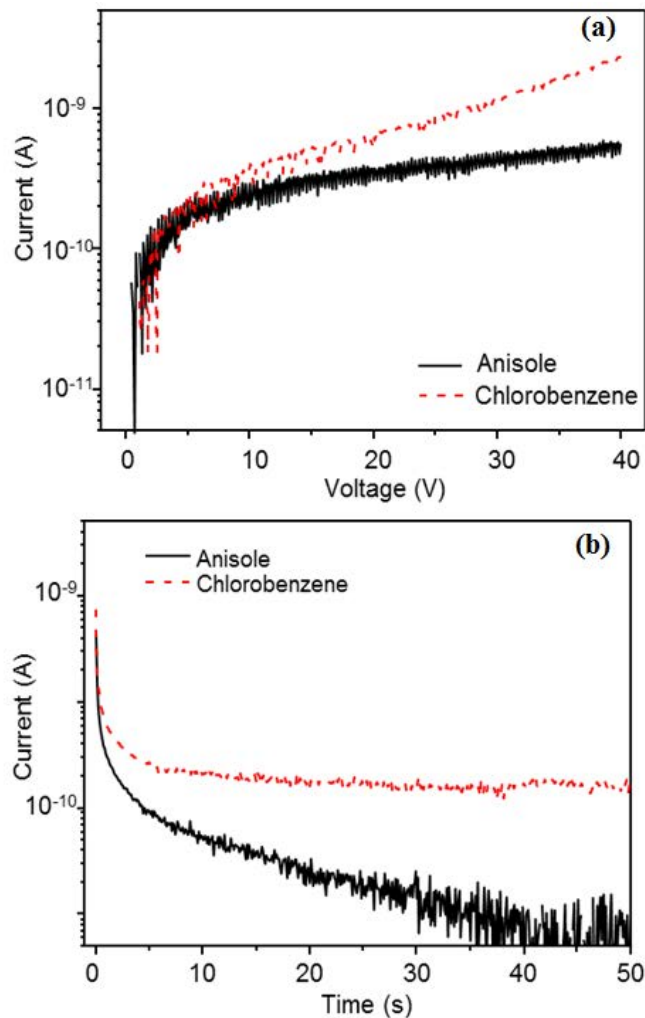


Figure 2-19: (a) Current-Voltage characteristics and (b) Answer to a step of voltage of Su8 on Aluminum after depositing drop of anisole or chlorobenzene on it.

When depositing anisole drop on Su8, the current as a function of the voltage saturates well as usual for an insulator. In the contrary, the current increases continuously with the voltage when using chlorobenzene drop, indicating a leakage in the insulator. Under a step of voltage, the current saturates very quickly at high value when using chlorobenzene. It decreases continuously in the first time when using anisole.

These measurements were confirmed by the plot of the capacitance-voltage characteristics. Figure 2-20 shows the C-V characteristics of three MIM samples: Aluminum-Su8-Aluminum, Aluminum-Su8-drop of Chlorobenzene-Aluminum, Aluminum-Su8-drop of Anisole-Aluminum. Depositing anisole or not on Su8 doesn't change the capacitance. However the drop of chlorobenzene decrease a lot the capacitance.

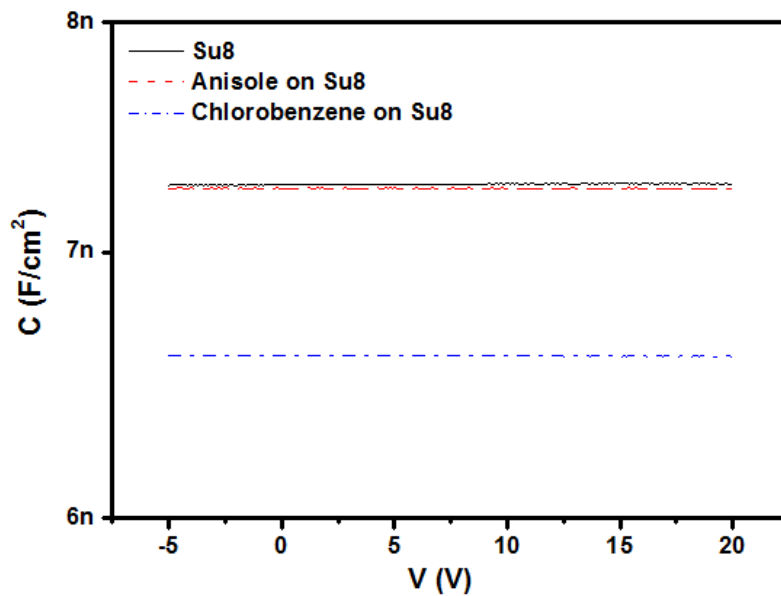


Figure 2-20: Capacitance-voltage characteristics of MIM structures: Aluminum-Su8-Aluminum, Aluminum-Su8-drop of Anisole-Aluminum, Aluminum-Su8-drop of Chlorobenzene-Aluminum.

The high gate leakage current of TFTs when depositing Tips-Pentacene diluted in chlorobenzene or dichlorobenzene can be explained then by the chemical reaction of these solvents with Su8 weakening its insulating character.

Finally the link between the performance in on-regime and the off-current and the gate leakage current can also be explained. The link can be well described by the scheme presented in Figure 2-21.

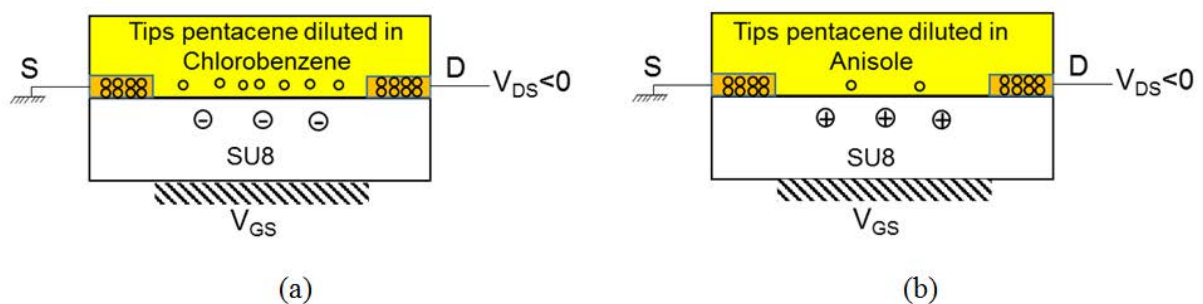


Figure 2-21: Scheme of OTFTs fabricated by using Tip-pentacene diluted in (a) Chlorobenzene, and (b) Anisole.

It can be assumed that negative fixed charge can appear in Su8 due to its reaction with chlorobenzene. This negative charge attracts holes towards the pentacene-Su8 interface in the pentacene, leading to existing channel whatever the gate voltage. In off regime off-current is high due to this existing channel. In on-regime, drain current is high and at the same time gate leakage current is high due to the negative gate voltage. When using anisole, no interaction between anisole and Su8 occurs. In this case, Su8 contains positively charged traps as concluded in a previous work^[32]. No hole accumulation occurs at the interface between Su8 and pentacene. The off-current is low. In on-regime the drain current is also low and due to the repulsion by positive fixed charge in Su8, the hole gate leakage current is low even if negative gate voltage is applied.

It can be seen in this study that solvent has a significant impact on the morphology of Tips-pentacene film and the electrical characteristics of OTFTs. The effect on the electrical characteristics is mainly due to the chemical reaction between the Tips-pentacene solution and the al-ready deposited Su8 gate insulator.

V.2 Effect of drying and annealing temperature of Tips-pentacene OTFTs

V.2.1 Drying temperature effect

Park *et al*^[31] have reported that drying temperature has a strong impact on device performance. They fabricated devices by drop casting of P3HT solution on the insulator layer at room temperature (25°C) and 70°C. The device fabricated at room temperature shows better performance compare to device fabricated at 70°C. In this work, OTFTs have been fabricated by drop casting 1.5% wt Tips-pentacene in chlorobenzene on lithography structure dried at room temperature (25°C) and 70°C. Figure 2-22 shows the transfer characteristics of Tips-pentacene OTFTs as a function of drying temperature.

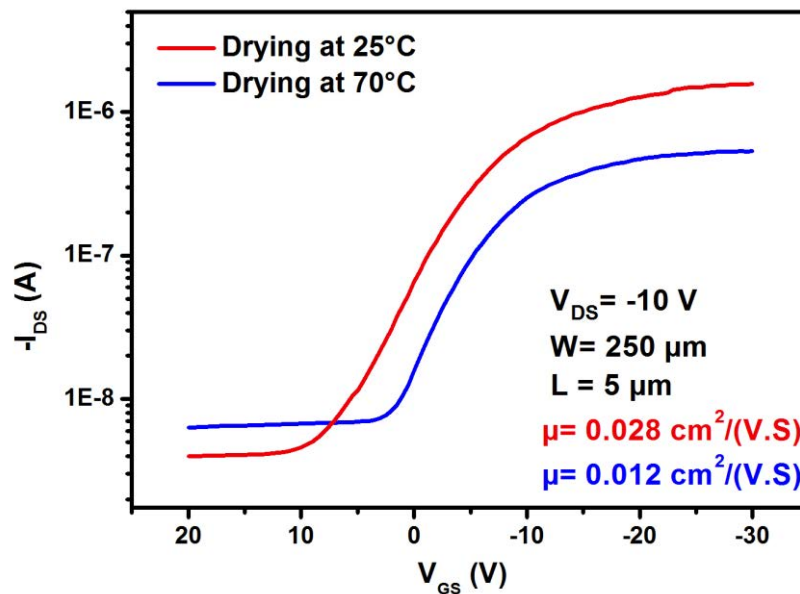


Figure 2-22: Transfer characteristics of Tips-pentacene OTFTs dried at room temperature (25°C) and 70°C.

As shown in Figure 2-22, Tips-pentacene dried at 25°C shows mobility about $0.028 \text{ cm}^2/\text{Vs}$, $I_{\text{on}}/I_{\text{off}}$ ratio of 3 decades, and threshold voltage of -1.32V. In contrast, Tips-pentacene dried at 70°C shows mobility about $0.012 \text{ cm}^2/\text{Vs}$, $I_{\text{on}}/I_{\text{off}}$ ratio of 2 decades, and threshold voltage of -2.32V.

It can clearly be seen that the Tips-pentacene OTFT dried at room temperature exhibits superior performance than OTFT dried at 70°C. As previously mentioned, when the drying temperature is lower, the formation rate of the semiconductor film is slower leading to better molecular packing.

V.2.2 Annealing temperature effect

As introduced previously, Bae *et al* ^[15] reported the annealing effect of OTFTs based on Tips-pentacene. Mobility decreases as annealing temperature exceeds 60°C, due to the fact that cracks are developed. In this work, OTFTs have been fabricated by drop casting 1.5% wt Tips-pentacene in chlorobenzene on lithography structure dried at room temperature, annealed at: 40°C, 60°C, 80°C, and 100°C. Figure 2-23 shows that mobility is dependent on annealing temperature.

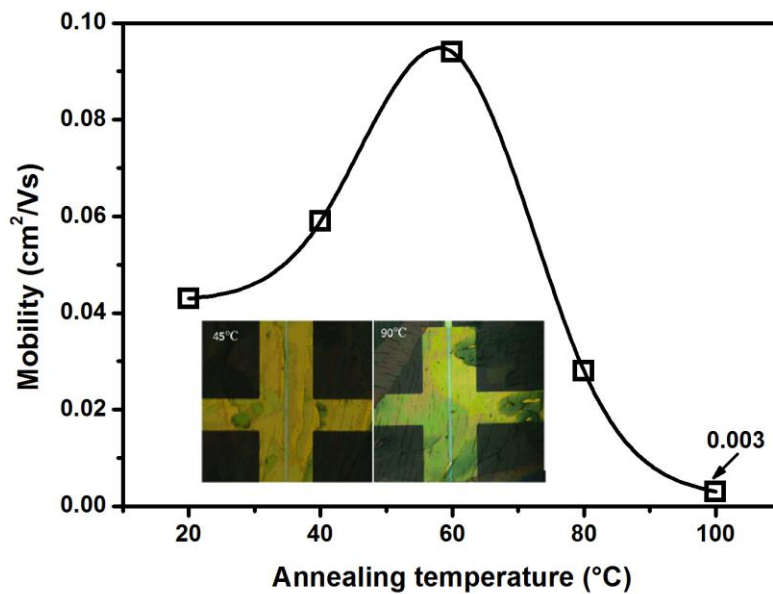


Figure 2-23: Mobility of Tips-pentacene OTFTs as a function of the annealing temperature. The inset shows the optical micrographs of cracks development.

When annealing temperature increases from 20°C to 60°C, the mobility is slightly improved. However, when annealing temperature exceeds 60°C, the mobility is drastically impacted (i.e. decreases from 0.094 to 0.003 cm²/Vs). Optical pictures of organic semiconductor deposited on drain and source shows that at high annealing temperature (>90°C) micro-cracks are observed. Such phenomenon, certainly due to the thermal mismatch between the polymeric insulator (Su8 in this case) and the organic semiconductor, can explain the decrease of mobility at high annealing temperature.

V.3 Effect of a functionalization of drain and source contacts on Tips-pentacene OTFTs

Finally, another expected improvement of the OTFT's characteristics can be given by a functionalization of the gold drain and source contacts to improve the charge injection.

A self-assembled monolayer of pentafluorobenzenethiol (PFBT) was formed on the Au source/drain electrodes to modify the interface between injection contacts and organic semiconductor.

As introduced in section II, a bottom-gate and bottom-contact geometry was used to study the effect of the functionalization of drain and source contacts on performance of OTFTs. Before fabrication of active layer, PFBT monolayers on gold were prepared at room

temperature by immersing the substrates into 10mM ethanol solution of the PFBT for two minutes. After removal from the solution, the substrates were carefully rinsed with pure ethanol and dried by N₂. Finally, 1.5% Tips-pentacene in chlorobenzene was drop casted on active region. Figure 2-24 shows the schematic picture of Tips-pentacene OTFT modified with PFBT. Figure 2-25 presents the transfer characteristics of similar OTFTs with no treatment and PFBT treatment.

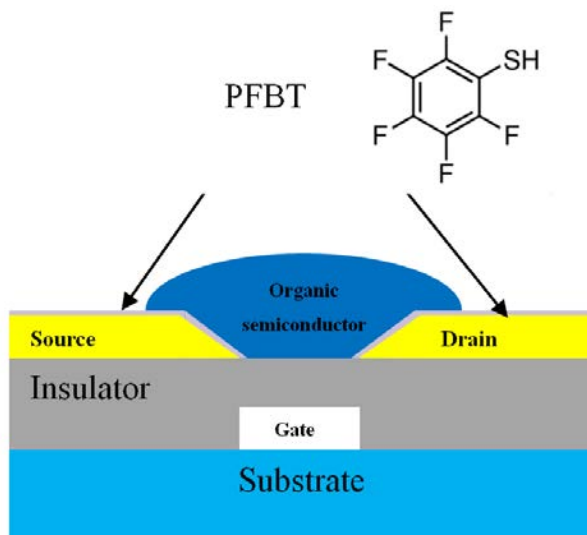


Figure 2-24: Cross sectional view of Tips-pentacene OTFT functionalized with PFBT.

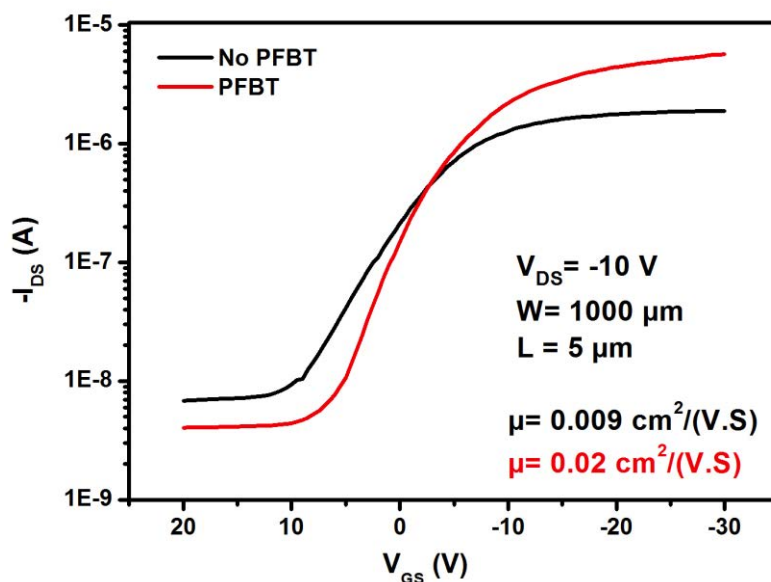


Figure 2-25: Transfer characteristics of OTFTs modified with PFBT.

As shown in Figure 2-25, functionalizing gold source and drain contacts with PFBT leads to better characteristics, particularly higher on-current and then higher mobility increasing from 0.009 to 0.02 cm^2/Vs . The source-drain voltage is -10V, and the channel length and width are 5 μm and 1000 μm , respectively.

V.4 Structure factors: Effect of channel length of Tips-pentacene OTFTs

Finally, to check the reliability of the process, a series of OTFTs, with a channel width of 1000 μm and different channel length, 1 μm , 2 μm , 5 μm , 10 μm and 20 μm , were employed. 1.5% Tips-pentacene in chlorobenzene was drop casted on photolithography structure. OTFTs was dried at room temperature and annealed at 60°C. Figure 2-26 shows the transfer curves of this series of OTFTs. As expected, for the same channel width, drain-source current decreases when the channel length increases. This decrease is more or less linear with the length inverse ($1/L$) as shown in Figure 2-27.

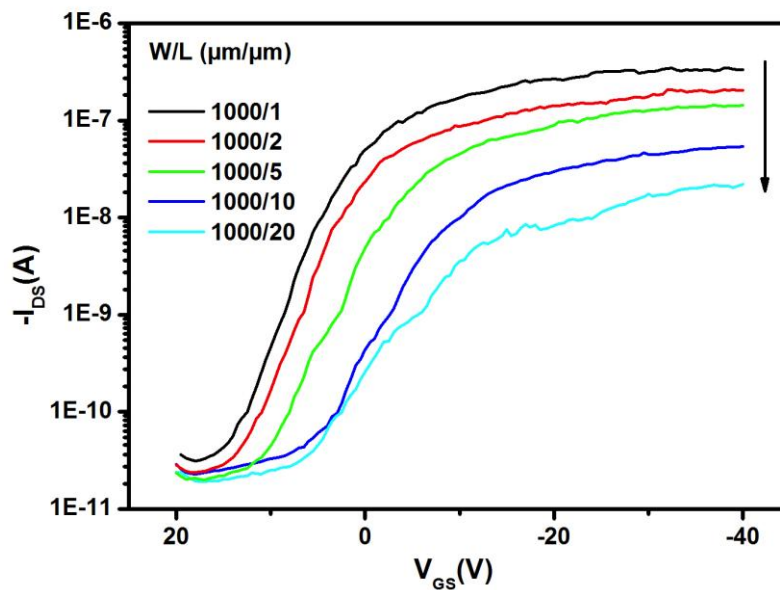


Figure 2-26: Transfer characteristics of a series of OTFTs with various channel lengths at the channel width of 1000 μm .

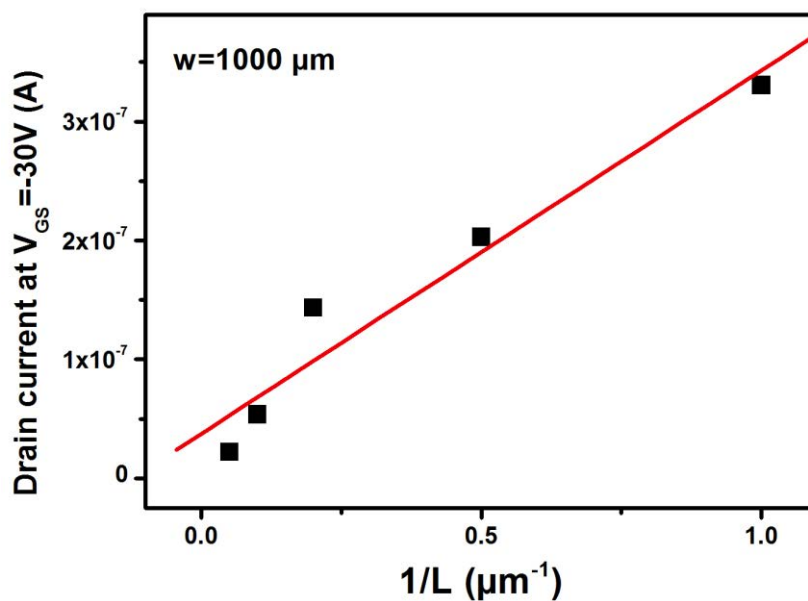


Figure 2-27: Linear increase of the drain-source current for a gate voltage of $-30V$ when the inverse ($1/L$) of the channel length L increases (or the channel length decreases).

Hence, the fabrication of OTFTs by drop casting is reliable inside the area of the drop. All the results presented in this chapter are reliable in the limit of the area of the drop.

Conclusion

In this first chapter, the performance of solution processed OTFTs as a function of the main parameters when depositing thin film in solution was carefully described. The influence of solvent, drying and annealing temperature were studied more particularly. For this work, simple drop-casting technique was used. It allowed quick answer on the main questions we had.

For this work both n-type OTFTs and p-type OTFTs were fabricated.

Process of n-type OTFT based on C₆₀ was unreliable, mainly due to the poor solubility of C₆₀ in organic solvent.

P-type OTFTs based on Tips-pentacene were more reliable. Great effect of the type of solvent was demonstrated. This effect is particularly more important when using bottom organic gate insulator as here. Solvent can react with the insulator weakening its insulating properties sometimes. The other influent technological parameter is the drying temperature. It was shown here that low drying temperature leads to better results. Low drying temperature allows long time for the formation the active film and better ordering of the molecules. Finally the last studied parameter is the post-annealing temperature. Annealing temperature has to be high but not so high as high temperature will lead to the appearance of cracks. Here 60°C was found as the optimum annealing temperature.

Finally this chapter led us to check the feasibility of solution processed fully organic OTFTs where both the gate insulator and the semiconducting active layer are organic. In this work we used very simple technique to deposit the semiconducting active layer. This technique, drop-casting, allowed to analyze the different technological parameters that influence the OTFTs characteristics. However, it is not reliable technique as the deposited active layer has no uniform thickness and its reproducibility is hard to reach. We will use present results to deposit the active layer by more powerful technique that is the inkjet printing. More reproducible process is expected when using this printing technique.

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Chapter 3: Inkjet-printing

After considering the possibility of solution fabricated OTFTs using very simple drop casting technique, it is now the moment to check the use of more complicated but more reliable and costly printing technique. Indeed, drop casting allowed determination of the different parameters influencing the electrical performance of OTFTs. However, it is very difficult to control the area of the deposition and the uniformity of the thickness of the deposited film when using drop casting. Printing technique through the very small volume of the droplets and the precise positioning can allow more reproducible films.

This chapter deals with the fabrication and the characterization of fully-printed OTFT using drop on demand technique. The chapter is divided in two parts.

The first one deals with the description of principle, main parameters, methodology of the printing technique:

- i) Inkjet printing techniques,
- ii) Key printing parameters such as: jetting, wetting and spreading,

- iii) Characterization method commonly used in the field of inkjet printing. Compare to conventional OTFT processing (OTFT fabricated using photolithography), drop on demand inkjet printing techniques require new processing methodology.
- iv)* Methodology.

The second part follows the methodology described in the first part in the purpose to process and characterize printed OTFTs. All the materials used in order to fabricate fully-printed OTFTs are deeply studied in terms of printability, and morphology. Then the electrical characterization of OTFT fabricated using inkjet printing is detailed and the electrical parameters of OTFTs are given and discussed.

Part I: Technique and methodology

I.1 Printed electronics

Printed electronics benefits from techniques already developed in the field of graphic arts last centuries. The past few years, a growing interest has gained for additive printing technologies. Such technologies offer an alternative to others based on conventional lithography processing using silicon derivative materials, for instance. Printing electronics offers many advantages such as ^[5]: i) unconventional substrates processing (flexible, stretchable, wearable...), ii) large area processing, iii) fast processing, iv), environmental friendly processing, v) low capital investment, vi) low time lapse from idea to the fabrication... Consequently, printed electronics has gained a growing interest throughout the past decades and many applications can be envisaged.

I.1.1 Applications

Printed electronic, benefits from previously mentioned advantages, has become the most suitable technology for realizing large area applications such as printed RFID tags, sensors and flexible display. Figure 3-1 shows the roadmap for organic and printed electronics applications published bi-yearly by the Organic Electronics Association (OE-A).

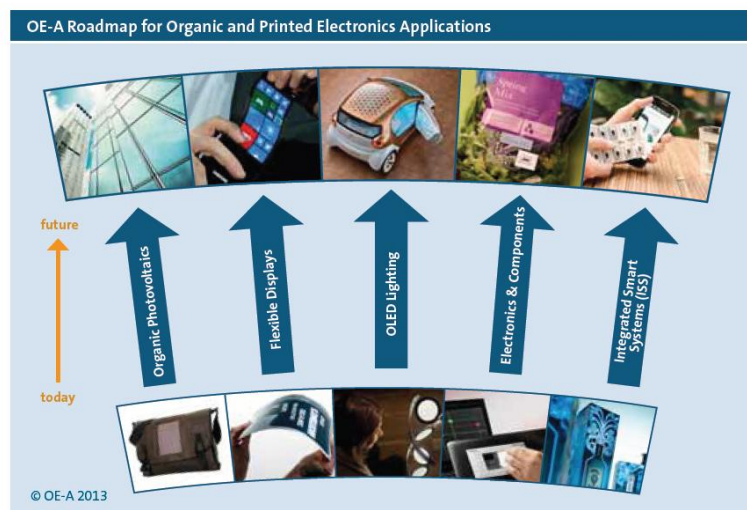


Figure 3-1: Roadmap for organic and printed electronics applications ^[6].

- **RFID tags**

RFID, radio frequency identification, is a wireless communication technology. RFID tags are frequently used in food industries, security, logistics, payment, and health...A typical RFID system is illustrated in Figure 3-2.

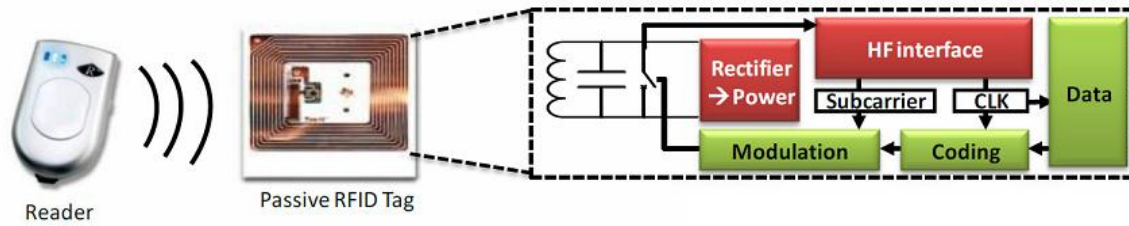


Figure 3-2: A basic RFID system comprises a reader, tag.

Reducing the price of RFID is a crucial step for its development. Most economic analysis suggests that the cost of each tag needs to be less than one cent to be economically viable, since the individual tagged product typically has a price floor in the range of few cents to few tens of cents [7]. Therefore, it is extremely challenging to deploy an RFID tag with a cost less than one cent. Printed RFID is a solution of choice for the achievement of low cost RF tags in high volume markets.

- **Displays**

An important potential commercial application of printed organic thin-film transistors is in backplanes fabrication for display. The large demand for portable electronic equipment, such as cell phones, laptop computers, personal digital assistants, and digital cameras, has advanced display technology rapidly and become an essential component of electronic devices, as many devices rely upon display to convey information and interact with users. Figure 3-3 shows the basic architecture and schematic diagram of the AMLCD.

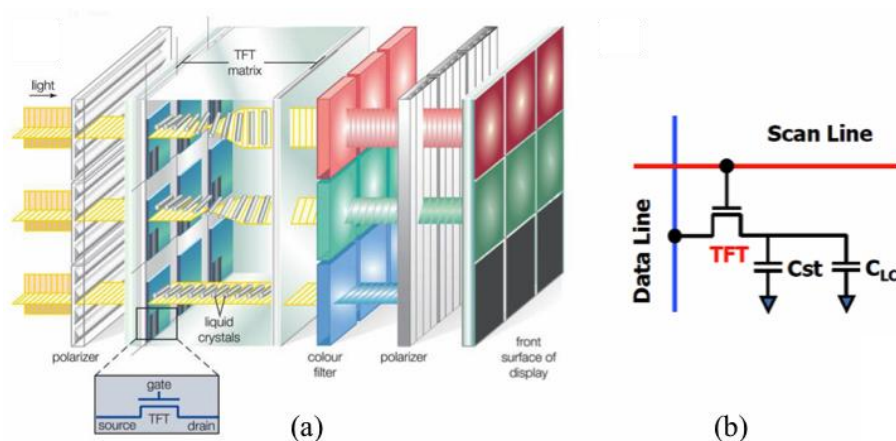


Figure 3-3: (a) Basic architecture of an AM-TFT-LCD [8], (b) Schematic diagram of an AM-LCD pixel.

- **Sensors**

Another promising application for organic transistors is large-area sensor. In this kind of application high speed is not required, consequently, organic transistors can be used. Moreover, printed OTFT offers other interesting advantages such as large-area processing, flexibility, and low-cost, are benefits. A large-area, flexible pressure sensor is shown in Figure 3-4.

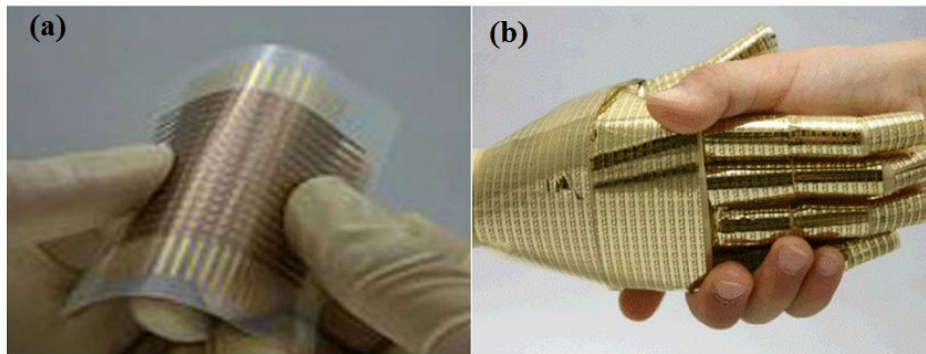


Figure 3-4: A flexible, large-area pressure sensor. (a) Organic transistor active matrix is formed on a plastic film and integrated with pressure-sensitive rubber; (b) an image of electronic artificial skin attached to the robot surface.

I.1.2 Printing techniques

A variety of techniques have been used in printing industry, including: screen-printing, offset printing, gravure printing, flexography, xerography, laser ablation, and inkjet printing ^[9]. Figure 3-5 classifies the techniques as a function of their main characteristics (minimum features size and throughput). Note that, the characteristics of photolithography technique are indicated onto the graphics. Compare to photolithography, printing techniques suffer from its low accuracy but benefits from high throughput.

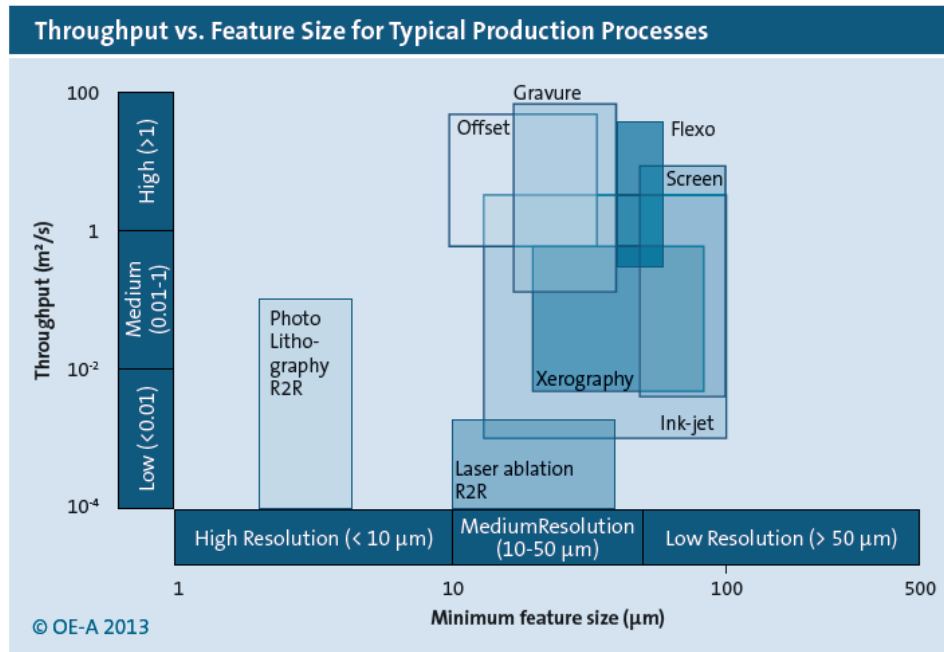


Figure 3-5: Throughput and resolution for a variety of processes ^[6].

● Screen printing

In screen-printing, ink is pushed through a fine mesh of plastic or metal fibers. The pattern is defined by filling apertures of a stencil. Screen printing has been largely used in printed circuit boards fabrication, in which a relatively thick ($> 1 \mu\text{m}$) and low resolution ($> 50 \mu\text{m}$) film is deposited. Indeed, the film thickness is determined by the thickness of the screen.

For OTFT fabrication, this technique is mainly used for deposition of thick layers such as dielectric or encapsulation. The first demonstration of printed organic TFT was made using screen-printing graphite source-drain (channel length $200 \mu\text{m}$, thickness $10 \mu\text{m}$) ^[10]. Screen printing has also been used in order to pattern source/drain electrodes (channel length $100 \mu\text{m}$, thickness $10 \mu\text{m}$) of bottom-gate FETs in both: top-contact ^[11] and bottom-contact configuration ^[12]. Moreover, such technique has been used in order to fabricate gate electrodes in top-gate FETs ^[13].

● Offset printing

Offset printing is the most widespread commercial printing technique where an “inked image” is transferred (or “offset”) from a plate cylinder to a blanket cylinder, then to the substrate. It is based on contrast between hydrophilic and hydrophobic areas which are created onto the plate cylinder. Hydrophobic area is coated with ink whereas hydrophilic is coated with water. Both areas are transfer onto the blanket cylinder then to the substrate.

It is a high-throughput printing technique, however, ink formulation is a challenging task in order to produce high-quality printed structures on a given substrate. Offset printing has been used to print source-drain structures of PEDOT/PSS for top-gate OTFTs with channel lengths of 30-200 μm , and lines widths of 100-200 μm ^[14].

- **Gravure printing**

A typical gravure system consists in a plate cylinder, a doctor blade, and an impression cylinder. The plate cylinder has a pre-defined pattern on the surface, which is used to transfer the ink onto a flexible substrate. The ink is coated on the cylinder as it turned through a reservoir. The ink excess on the cylinder surface is then wiped off by the doctor blade. The remaining ink filled inside the patterns is then transferred to the substrate as it turns and contacts the substrate.

It is a very high-throughput printing technique, which is more attractive for industrial high-speed manufacturing. Gravure printing has been used to print semiconductor ^[15], dielectric layer ^[16], and also fully-printed TFT ^[17].

- **Flexography**

Flexography is a form of printing process with a flexible relief plate. It is made by creating a positive mirrored master of the required image as a 3D relief in a rubber or polymer material. The image areas are raised above the non-image areas on the rubber or polymer plate. The ink is transferred from the ink roll, which is partially immersed in the ink tank. Then it transfers to the anilox roll, which can hold a specific amount of ink. A doctor blade is needed to wipe off the ink excess. The substrate is finally sandwiched between the plate cylinder and the impression cylinder to transfer the image.

The main application is in packaging where lower print quality can be tolerated. However, flexography has been used to print semiconductor layer, for instance ^[18].

- **Xerography**

Xerography, also known as electrophotography, is a printing and photocopying technique based on electrostatic charges. It has received substantial attention. However, with its low resolution and small throughput, it has not yet been used for OTFT fabrication.

- **Laser ablation**

Laser ablation is an innovative solution for flexible and high speed devices. Using laser wavelengths from UV to infrared and pulse lengths from femto-to-microseconds, organic and inorganic materials can be patterned by ablation. For instance, thin layer of conductor can be patterned in order to fabricate OTFT ^[19].

- **Inkjet printing**

Recently, inkjet printing has received growing interests as a way to deposit functional materials. It is a digital process. Nowadays, the development of the inkjet print-head, allows a resolution about few micrometers. Moreover, throughput has been improved with the development of multiply nozzles print-head.

I.2 Inkjet printing

Inkjet printing is a non-contact and additive printing technology. It is one of the most promising techniques in the field of organic electronics. It consists on small amount of functional ink jetted from a chamber through a hole, usually named: nozzle. The ink droplets fall and impact the substrate that can be heated. After this step, the droplet wets the substrate and evaporation takes place leaving a solid thin film. Adjacent droplets are cleverly adjusted in order to obtain the desired pattern used as active layers (conductor, insulator and semiconductor). Depending on drop ejection technique, inkjet-printing technology can be divided into two categories: continuous inkjet printing and Drop-on-Demand (DoD) inkjet printing. Focusing more on DoD, two main jetting methods can be distinguished including: thermoelectric or a piezoelectric transducer^[20]. Figure 3-6 sums the DoD technologies^[21-24]. Note that, all of printing techniques have ever been extensively described in the literature^[25-28] and will not be described in this document.

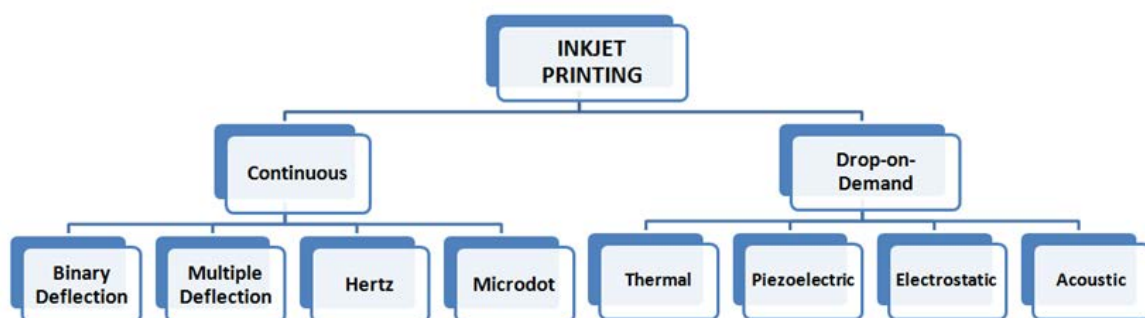


Figure 3-6: Schematic classifications of the inkjet-printing technologies.

As discussed previously, inkjet printing (i.e., DoD in our case) is considered as a promising manufacturing tool for the fabrication of organic electronics over flexible and large area substrate. Indeed, it allows the fabrication of micropatterns directly from a digital mask (devices are designed using a conventional CAD software and directly printed) using low functional ink amount as shown in Figure 3-7. Moreover, post-treatment processes such as: i) conventional thermal heating, ii) IR treatment, iii) UV curing can be performed online.

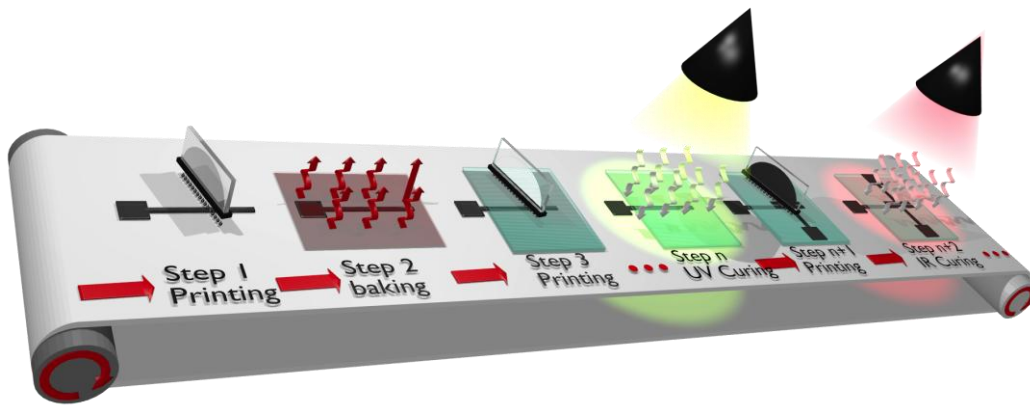


Figure 3-7: Schematic of inkjet printing process showing post-treatment processes which can be performed online.

Figure 3-8 shows the higher fabrication complexity of photolithography compare to printing process. Indeed, patterns fabrication using photolithography technique requires: i) hard mask, ii) photoresist spin coating, iii) UV exposure, iv) etching, and v) photoresist stripping.

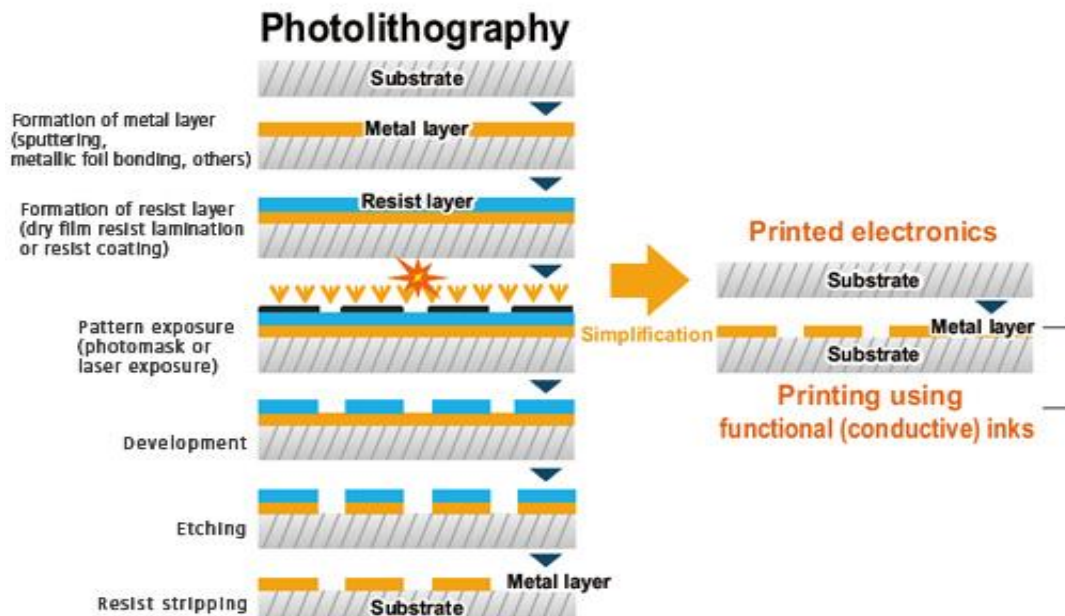


Figure 3-8: Comparison between printing techniques and photolithography process.

In conclusion, compared to conventional photolithography process, the inkjet printing technology suffers from a low minimum resolution (50 μm typically) but such technology offers an alternative to conventional process. Indeed it is a convenient way in order to drastically reduces the fabrication time from idea to proof of concept. Moreover, such

technology is a serious candidate for low cost organic electronic fabricated on flexible substrate over large area!

I.2.1 DoD Technology

● *Thermal DoD*

The working principle of thermal DoD inkjet-printing technology is as follows: when a pulse of current is applied to a heating resistor, its temperature increases rapidly as well as the ink at the vicinity of the heating resistor. The ink solvent starts to vaporize and a “vapor bubble” is generated. The bubble expands as the temperature increase. Due to bubble expanding, the pressure increases and pushes the ink out of the chamber through the nozzle. Then the current is cut off suddenly, the resistor temperature decreases and the vapor bubbles vanishes. Consequently ink is refilled. The formation of the ink by thermal DoD inkjet-printing process is shown in Figure 3-9.

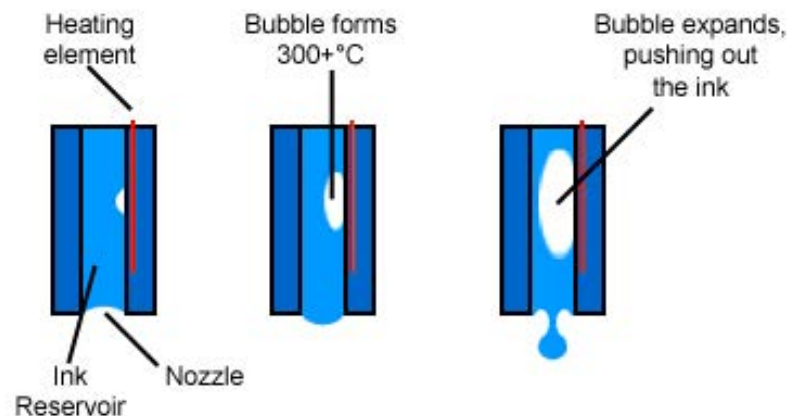


Figure 3-9: Schematic diagram of a thermal DoD inkjet-printing process ^[29].

● *Piezoelectric DoD*

The other most commonly used inkjet printing technology is piezoelectric DoD inkjet printing (i.e., technology used in this study) ^[30]. A piezoelectric membrane is used as actuator inside ink chamber. A high voltage (typically ranging from 50 to 120 Volts) pulse is applied to the piezoelectric membrane and consequently ink is pushed out through the nozzle. Droplets generation mechanism using piezoelectric DoD inkjet-printing process is shown in Figure 3-10.

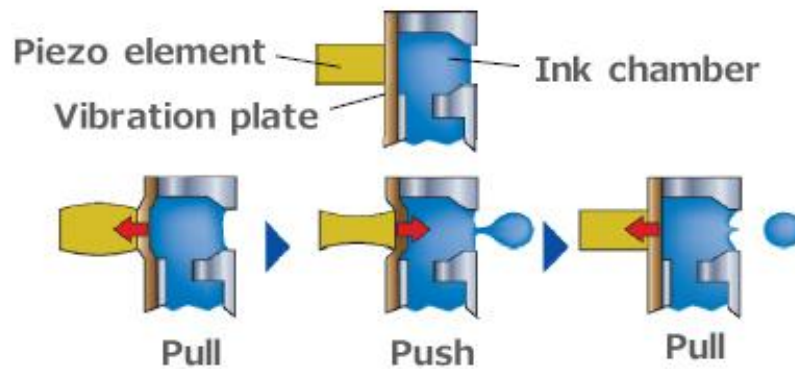


Figure 3-10: Schematic diagram of a piezoelectric DoD inkjet-printing process ^[31].

I.2.2 Inkjet printing key steps: Jetting, Spreading, Wetting and Drying.

Three main steps can be distinguished during inkjet printing process such as: i) droplets generation, ii) droplets interaction with substrate after their deposition at the desire location and iii) droplets drying. This sub-section describes why these steps are crucial and must be controlled in order to improve inkjet printing accuracy.

I.2.2.1 Droplet generation (jetting)

- Waveform

Droplet generation is monitored using a piezoelectric membrane actuates thanks to voltage applied to the piezo in function of time (i.e., the waveform). Depending on fluid properties (viscosity, molecular weight, amount of nanoparticles...), complex waveforms can be found in literature ^[32]. Note that, inks used in this study are versatile and consequently require only basic waveform as shown in Figure 3-11. This waveform can be divided into four steps.

Droplets are formed on positive firing voltage time (t_{dwell}) in step 1. Then, droplets are falling down with the firing voltage decreased from positive to negative (t_{fall}). Negative firing voltage time (t_{echo}) has been fixed at twice of t_{dwell} to avoid residual deformation waves after ejection of each drop (step 3). Then, negative firing voltage increases to positive firing voltage (t_{rise}) in order to assure the droplet formation (step 4). Note that, t_{fall} and t_{rise} should be as short as possible to not perturb droplet formation and to avoid a large volume of liquid jetting.

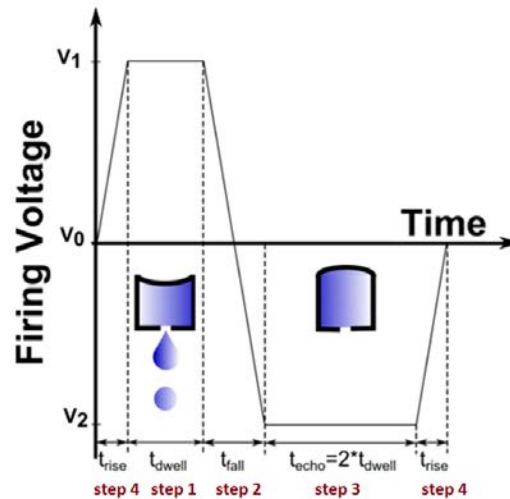


Figure 3-11: Typical waveform of inkjet-printed droplet formation.

These four steps can be controlled in terms of: i) duration and firing voltage for step 1 and step 3, ii) duration (slew rate) for step 2 and step 4. Moreover, jetting frequency, which must be as high as possible in order to optimize printing velocity, is also a crucial parameter in order to obtain stable jetting as shown in Figure 3-12 (a). When a parameter exceed a “correct value” unstable jetting dramatically occurs. Many unstable jetting configurations have already been reported such as: droplets misalignment during jetting, satellites droplets, spraying as shown in Figure 3-12 (b). Such configuration must be avoided in order to obtain accurate printing as shown in Figure 3-12 (c). Obviously, inappropriate jetting leads to inaccurate patterns as shown in Figure 3-12 (d).

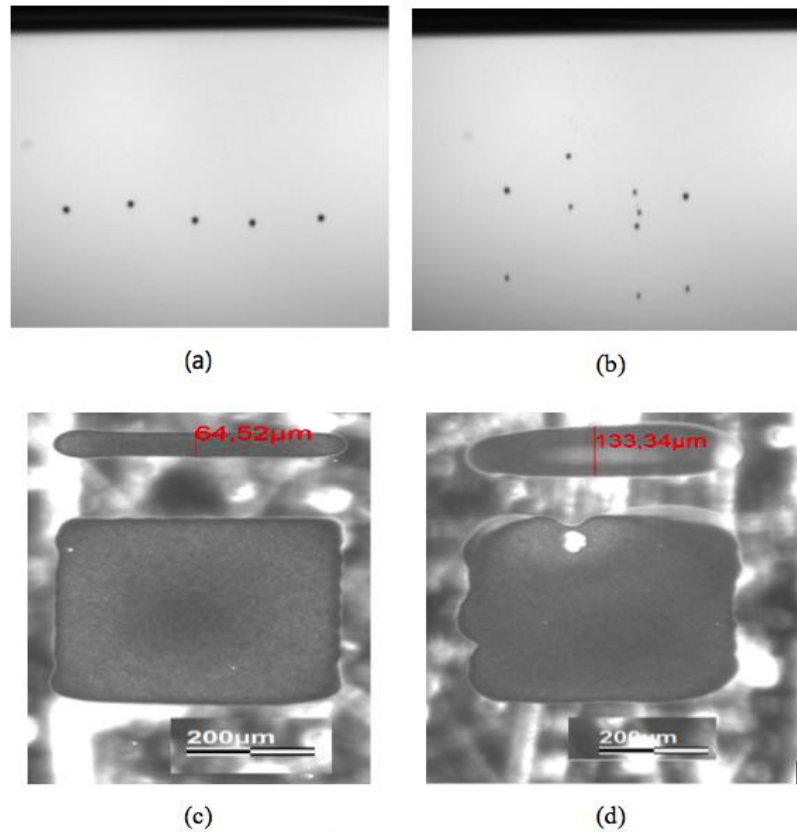


Figure 3-12: (a) stable jetting drops, (b) unstable jetting drops, (c) optimum jetting printed pattern, and (d) unstable drops effect on a printed pattern.

In addition, other cases during printing process can also affect patterns morphology. Inaccurate droplets jetting and their corresponding effects on printed patterns are shown in Figure 3-13.

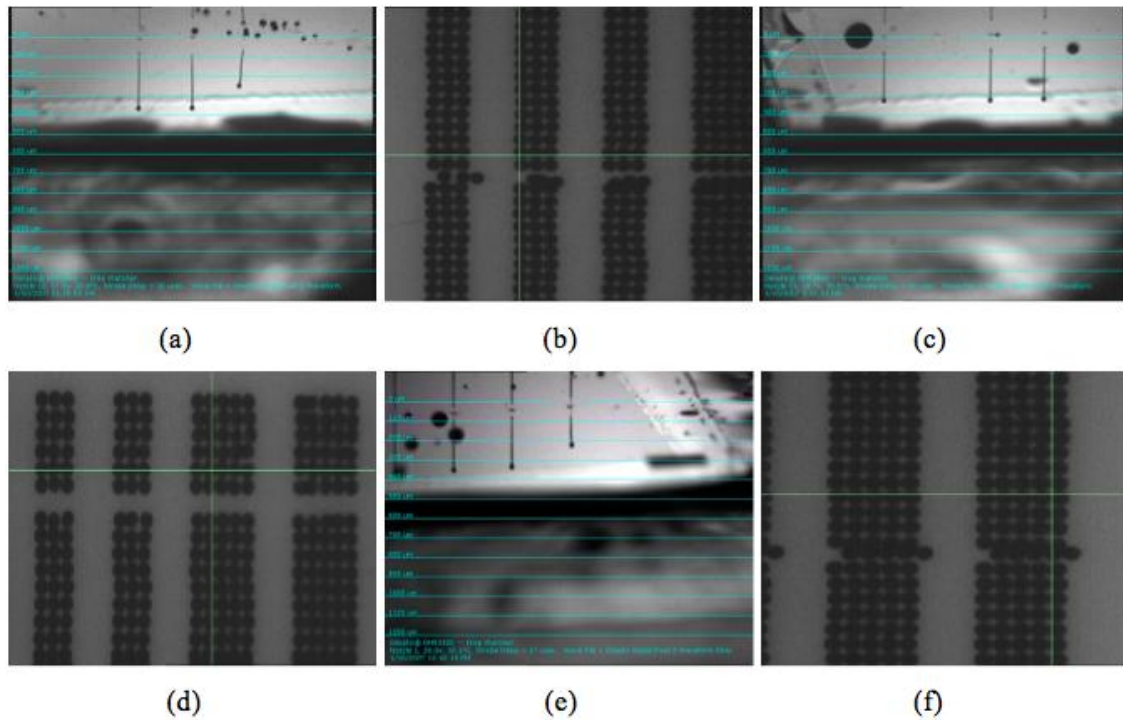


Figure 3-13: (a) Misdirected drops and (b) effect on printed pattern; (c) non-jetting nozzles and (d) effect on printed pattern; (e) non-matched velocities and (f) effect on printed pattern [33].

Misdirected nozzles refer to drop shift away from the original track as shown in Figure 3-13 (a). Consequently, inaccurate droplet location (one line) is observed on Figure 3-13 (b). Non-jetting nozzles do not eject drop as shown in Figure 3-13 (c) and (d), are usually due to the nozzle clogging. Consequently missing lines are observed as shown in Figure 3-13 (d). When one or several nozzles are jetting slower than the others, the vertical lines will have uneven edges, as can be observed in Figure 3-13 (e) and (f).

Importantly in this thesis, jetting is considered stable when the following jettability criteria are respected. The jettability criterion is the ability to obtain a droplet at a distance range (Δr) between 500 μm and 1 mm (acceptable working distance for the printer equipment: CERADROP© Xseries). Satellite droplets or tail must be reabsorbed by the nozzle and jettability must be stable for a long time with low droplet misalignment on the substrate ($\Delta x < 5 \mu\text{m}$).

In summary, particular attention must be paid on waveform before the printing step. Moreover, the jettability of each functional ink must be study. However, two kinds of inks can be distinguished as following:

i) Commercial ink (e.g., silver ink used in this study) which fit all the printing requirements (viscosity, surface tension...). Consequently, such ink doesn't need to be deeply study and only parameters described previously is adjusted (firing voltage, jetting frequency...)

ii) Home-made ink (e.g., epoxy-based ink used in this study) which must be deeply study. Indeed, a deeper investigation of jettability must be performed in order to evaluate its versatility. The following sub-section will describe the methodology explained for the first time in the work of Subramanian in order to qualify an ink from jettability point of view [34]. This universal approach has also been followed in this study concerning the jettability of epoxy-based ink.

- Fluid requirement

Following literature requirement, in order to obtain stable jetting, the following values are usually satisfied: droplet velocity, ink viscosity and surface tension equal 6-10 m/s, 10-12 cP and 28-33 mN/m, respectively. However, ink can be also printable if it doesn't respect the previous mentioned requirements. For instance, epoxy based ink used in this study doesn't respect all those criterions (viscosity is equal 2.5 cP) but, following Subramanian's rigorous methodology, a high printability behavior have been observed.

Indeed, jettability is governed by inertial, viscous, and surface tension forces. Dimensionless numbers including Reynolds (Re), Weber (We), Capillary (Ca), and Z number characterize the droplet formation process [35]. These four dimensionless numbers is defined as follows:

$$Re = \frac{\text{inertial force}}{\text{viscous force}} = \frac{\rho v^2 d^2}{\eta v d} = \frac{\rho v d}{\eta} \quad (4.1)$$

$$We = \frac{\text{inertial force}}{\text{surface tension}} = \frac{\rho v^2 d^2}{\sigma d} = \frac{\rho v^2 d}{\sigma} \quad (4.2)$$

$$Ca = \frac{\text{viscous force}}{\text{surface tension}} = \frac{\eta v d}{\sigma d} = \frac{\eta v}{\sigma} \quad (4.3)$$

$$Z = \frac{\sqrt{\text{inertial force} \times \text{surface tension}}}{\text{viscous force}} = \frac{\sqrt{\sigma \rho v^2 d^3}}{\eta v d} = \frac{\sqrt{\sigma \rho d}}{\eta} \quad (4.4)$$

where η , σ , ρ are the viscosity, the surface tension, and the density of the ink, respectively. v and d are the velocity and the nozzle diameter. The surface tension force σ does not vary significantly during the ink droplet formation. d is kept constant, and ρ varies negligibly. Thus,

the jettability of an ink system should be governed primarily by the viscous force and inertial force. Therefore, Ca-We parameter space is employed to investigate the impact of ink rheology on jettability. As discussed previously, ρ , σ , and d do not change drastically during droplet formation, thus, Ca and We are primarily determined by v and η . Here v is controlled by the pulse waveform. In each system, the viscosity η in Newtonian systems is constant across all shear tension, i.e. jetting velocities, thus Ca is proportional to v , and We is proportional to v^2 . When plotted on a log-log scale in Ca-We space, data could be always lie along a line with slope=1/2. The calculation can be detailed as follows:

$$We = \frac{\rho v^2 d}{\sigma} \quad Ca = \frac{\eta v}{\sigma} \quad (4.5)$$

σ does not vary significantly during the ink droplet formation, d is kept constant, and ρ varies negligibly, thus equation (4.5) can be simplified as follows:

$$We = Av^2 \quad Ca = B \eta v \quad (4.6)$$

$$Ca^2 = CWe \quad (4.7)$$

C is constant during the ink droplet formation in one ink system.

$$C = \frac{\eta^2}{\rho d}$$

Using log-log scale, equation (4.7) can be simplified as follows:

$$\log Ca = \frac{1}{2} \log \sqrt{C} We \quad (4.8)$$

In log-log scale, data of each ink could always lie along a line with slope=1/2. Each line represents an individual ink system operating at a velocity, and parallel lines represent different velocities. The length of the lines is governed by the velocity range for a given ink system.

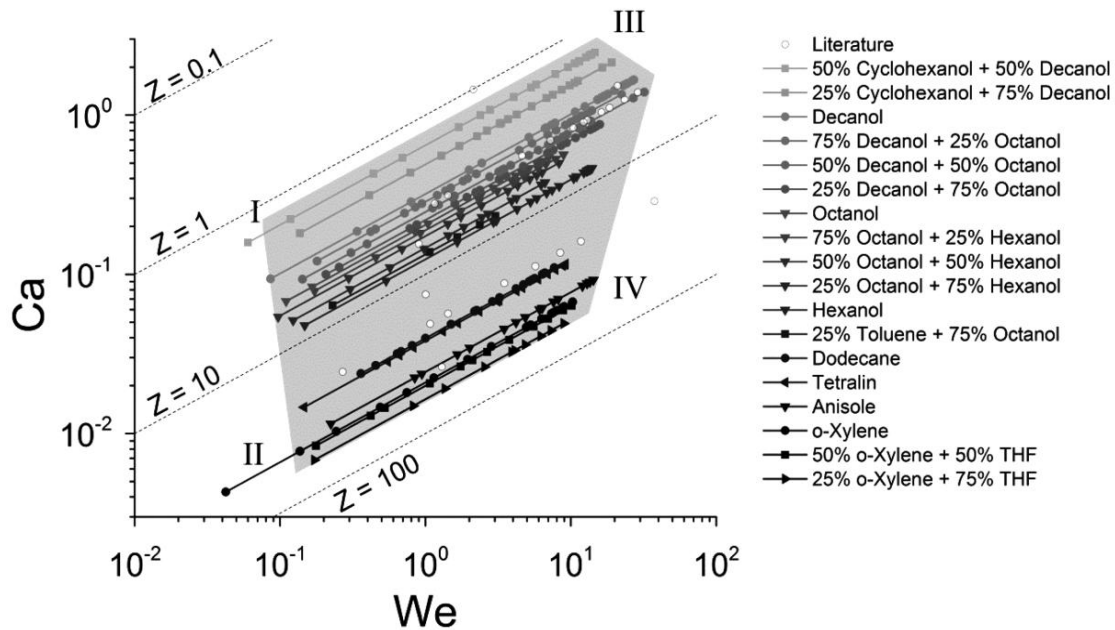


Figure 3-14: Jettable window within the Capillary number-Weber number parameter space.

Hatched area: The printable window defined by Subramanian ^[34].

More viscous ink systems occupy the lines with higher Ca value and less viscous ink systems occupy the lines with smaller Ca value. If a given ink system lies inside of the printable window, it is jettable in the range of velocity; otherwise, if a given ink system lies outside of the printable window, either above or below, it is unjettable for all the velocity. Thus, Subramanian defined a jettable window using systematical study of many solvents. The jettable window is shown in Figure 3-14.

I.2.2.2 Spreading, Wetting & Drying

As previously detailed, the droplet is jetted and: i) impacts on the surface (spreading phase), ii) minimizes its energy (wetting phase), iii) solidifies (drying phase). Such steps play crucial role in the accuracy of printed patterns and have to be detailed.

- Spreading

When a droplet, jetted at a relatively high velocity ($6-10\text{m.s}^{-1}$), impacts on a dry surface, several behaviors can be observed. Indeed, depending on substrates (hydrophobicity, roughness...) and/or fluid (viscosity, elasticity...) properties, different spreading behaviors can be observed as shown in Figure 3-15.

The first line of Figure 3-15 illustrates the best impact mechanism required for inkjet printing techniques (i.e, without splashing or rebound). The droplet deposition can be divide in two parts: i) Images 1, 2 and 3 of the first line show the spreading step (i.e., droplet impact and its diameter increased). This step is mainly affected by fluid viscosity. The lower is the viscosity, the larger is the impact diameter and consequently large printed patterns will be performed. ii) Images 4 and 5 of the first line show the relaxation phase where the droplet minimizes its energy and determines the equilibrium contact angle. Surface wetting properties strongly affect this phase.

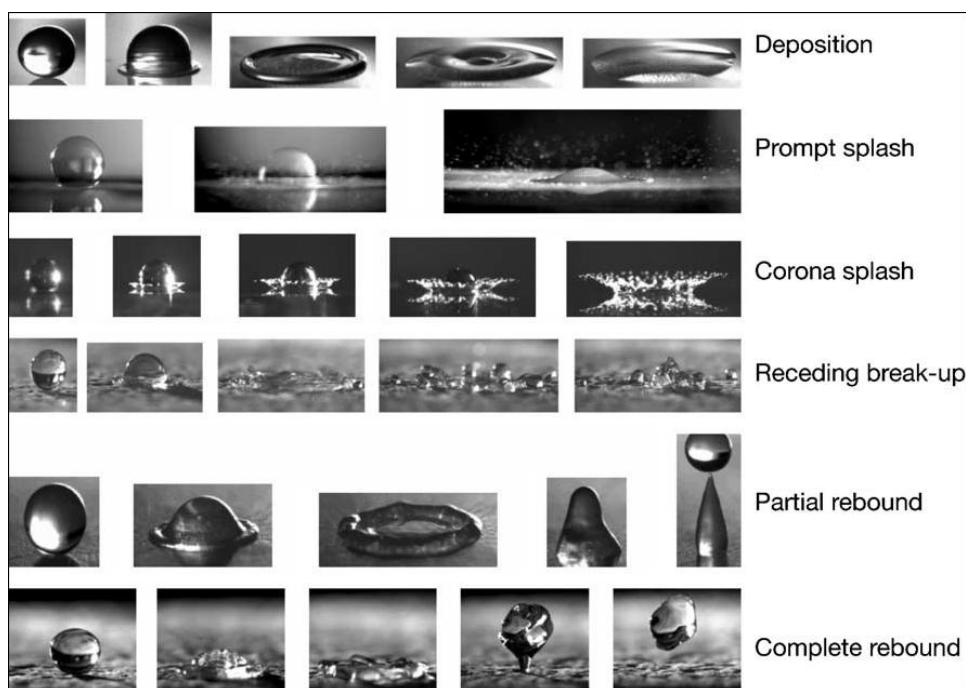


Figure 3-15: Behavior of drop impact on a dry surface ^[36].

The other lines of Figure 3-15 show unwanted spreading effects for inkjet printing technology. For instance, splashing showing in the second and third lines affects the printed pattern accuracy. This behavior can appear when: velocity is too high, surface tension and viscosity is too low or substrate is too rough ^[37]. The other lines of Figure 3-15 show unwanted phenomenon that can occurs on super-hydrophobic surfaces (i.e., in our case super-hydrophobic surface will be more adapted because liquid used for inkjet printing usually shows low surface tension values).

Unfortunately, impact mechanisms will be not studied in this thesis because imaging droplets impact need a high speed camera and the printer (CERADROP X-series) is not

equipped with such kind of camera. However, such experiments can be found in other works [38,39].

● Wetting

As described before, a droplet of liquid impinging upon a substrate minimize its interfacial energy forming a spherical caps (i.e., when substrates is flat). When droplet is at equilibrium, Young-Dupre law can be used in order to describe a system composed of substrate, air and liquid, as shown in equation (4.9). The fluid's surface tension γ is defined as follows:

$$\gamma \cos \theta_{eq} = \gamma_{SL} - \gamma_{SO} \quad (4.9)$$

where γ_{SL} and γ_{SO} represent the substrate-liquid and substrate-air interfacial tensions, respectively.

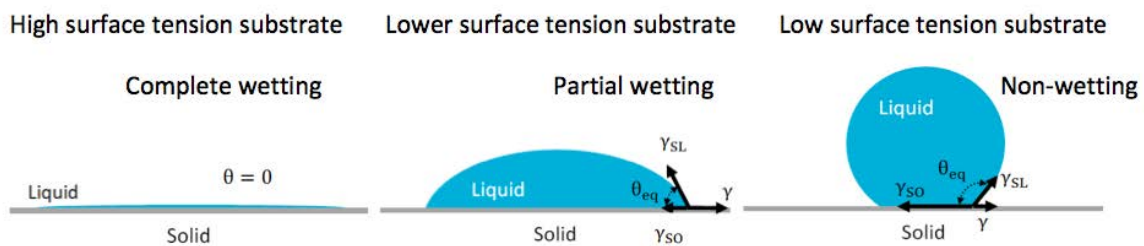


Figure 3-16: Droplet wetting behavior as a function of surface tension substrate.

Figure 3-16 described three wetting regimes: complete wetting, partial wetting, and non-wetting. As shown in Figure 3-16, wetting behavior will give information on final patterns size. Consequently, in this study, surface tension of each ink and substrate will be systematically measured. Such measurements will give crucial information on substrate printability. Indeed two different cases can be distinguished:

i) When the substrate shows high surface energy the droplet is highly pinned (high static contact angle hysteresis) and wets a lot the substrate. In this case the substrate is easily printable but patterns shows poor resolution. For instance, droplet diameter value after drying ranging from 70 to 110 μm for a volume about 15 pL. Any kind of patterns including lines or square shaped can be achieved.

ii) When the substrate shows low surface energy the droplet is less pinned than in the first case (static hysteresis contact angle is lower) and consequently wets less the substrate. In this case patterns shows higher resolution. For instance, droplet diameter value after drying ranging from 20 to 40 μm for a volume about 15 pL. However in most of cases line or

squared shaped can't be obtained because of "line stability" also named rivulet instability [40,41]. Work performed by Davis shows that if contact line is not pinned (low contact angle hysteresis) and the water contact angle is more than 90° , the printed line is not stable. Obviously, if the contact line is pinned and the water contact angle is less than 90° , the printed line is stable. For instance when a printed line is not stable, it can be split in macrodroplet as shown in Figure 3-17.

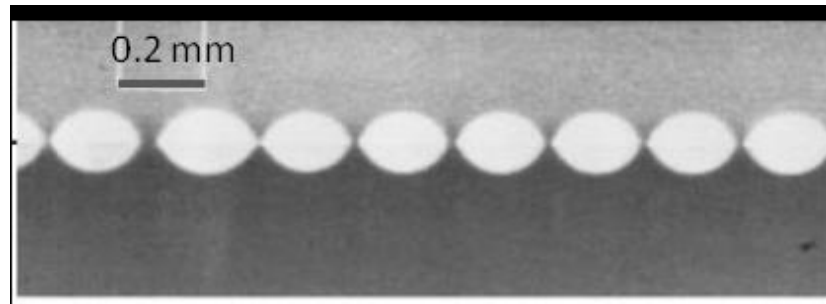


Figure 3-17: *Unstable inkjet printed line of water droplets on Plexiglas (without contact angle hysteresis), having dewetted into spherical cap macrodrops [42].*

Consequently, in this thesis substrates and surfaces has been classified in function of their wetting properties. Unstable wetting conditions, as described previously, have been observed when silver ink has been printed on polymer surface (Su8). Consequently surface treatment described in sub-section II.1.2 in part II of chapter 3 has been performed to solve this problem.

- Drying

When the droplet is deposited on the substrate, a phase change occurs that is usually induced by solvent evaporation. Solidification mechanism is governed by liquid/substrate interaction. Particular attention must be paid on solidification step because the resulting layers morphology depends on drying conditions. Such impacts can be observed on films thickness homogeneity (i.e., due to coffee ring effect) and films width uniformity (i.e., due to printing parameters such as overlap).

- **Coffee ring effect**

For instance, a well-known drying behavior, which is reported as a drawback, in most cases, is the coffee ring effect (i.e., also named coffee stain effect). Such drying behavior firstly described by Deegan [43] impact drastically printed layer morphology as shown in Figure 3-18 (a).

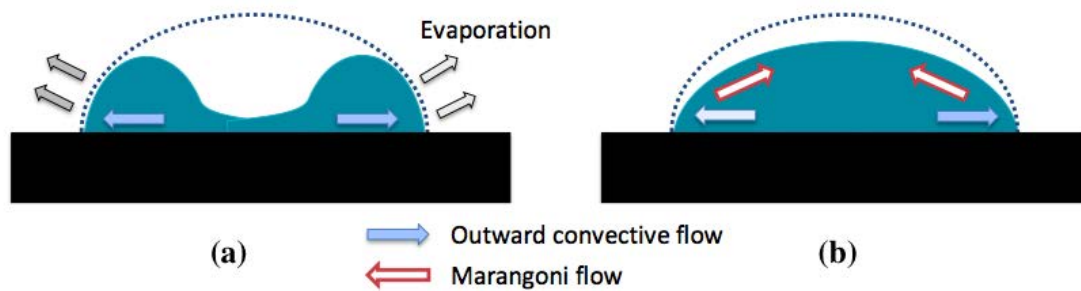


Figure 3-18: (a) Schematic illustration of the coffee ring formation; (b) schematic illustration of the coffee ring suppressed using Marangoni flow. Dotted lines represent the droplet shape before drying ^[44].

The coffee ring effect results from a greater solvent evaporation rate at the surrounding of the contact line than in the center of the droplet. When the contact line is pinned, the solute transport from the center to the edge is induced by replenish flow, leading to inhomogeneous films after complete evaporation. Many techniques, which mainly consist on introducing additional flow inside the droplet (opposite to evaporation flow) has been used in order to decrease such phenomena, as shown in Figure 3-18 (b). For instance, the use of higher substrate temperature during printing can improve the film homogeneity. Heating the substrate increases the surface tension gradient between the edge and the center of the droplet. Such surface tension gradient induces Marangoni flows that carry the solute inward ^[16]. Consequently, this effect competes with this one observed by Deegan leading to obtain a more uniform profile.

➤ **Printing parameters effect (overlap)**

Printing parameters should be adjusted before printing. In inkjet printing process, printing patterns are composed of several discrete pixels (isolated droplets). Droplets coalescence is governed by overlapping of adjacent droplets. When such droplets coalesce along X axis, a line is printed. Obviously, lines coalescence along Y axis form the film. The resolution of printed patterns depends on the drop size on substrate and the overlap between drops. In general, drop size is constant when the ink, the volume, the substrate kind, and the substrate temperature are fixed. The overlap has to be adjusted through repetitive experiments in order to avoid patterns morphology such as individual drops, scalloped line, and bulging ^[45]. Such behavior will be described more precisely in section named printing methodology.

Moreover, a special attention has to be paid during patterns design. Indeed, inkjet printing is a digital processing and consequently, printed patterns will not exactly respect the ideal design (especially for curved-shape) as shown in Figure 3-19.

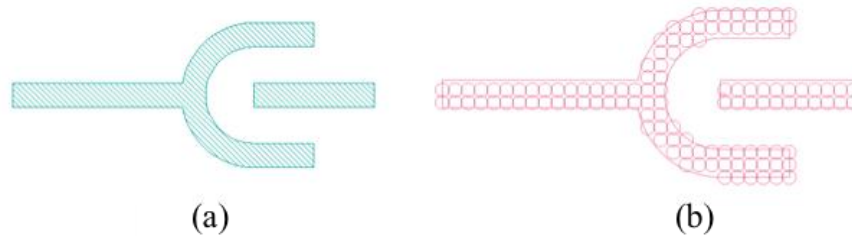


Figure 3-19: (a) Ideal design, (b) Digital design

I.2.3 Inkjet printing system and characterization methods

I.2.3.1 Inkjet printer

- Hardware

The inkjet printer used in this thesis is piezoelectric jet systems, named Ceraprinter X-series. It is an “all-in-one” advanced materials deposition inkjet tool for inkjet processes development in printed electronics and smart 3D printing. It offers the possibility to use different print-head manufacturers. Thanks to its embedded post-process and its innovative software package, Ceraprinter X-series brings new opportunities to a wide range of industrial fields. The optical picture of Ceraprinter X-series is shown in Figure 3-20.



Figure 3-20: Optical picture of Ceraprinter X-series.

The Ceraprinter X-series, used in this work, embeds two print-heads, one with 256 nozzles (256 nozzles Q-class print-head (Dimatix[®]) and the other with 16 nozzles cartridge (Dimatix[®]). In his study the first print-head is used to print silver ink and the second one is used to print polymeric insulator. The maximum printing velocity is 500 mm/s and X/Y stage accuracy is about 1.5 μm . Such characteristics allow the fabrication of fully-printed OTFT online onto maximum substrate size about 305×305 mm. Note that a wide range of substrates can be used (from paper sheet to 10 mm thick substrate). Moreover, substrate temperature can be heated up to 60°C and high accuracy positioning (substrate alignment < +/- 2 μm) allows printing multi-layers devices at high accuracy. A stroboscopic visualization system is used to characterize jetting step.

- Software

The software is composed of three modules: Ceraslice, Fab-analyser, and Drop-analyser.

Drop-analyser is an advanced droplets jetting analysis software.

Fab-analyser is used for analysis printed layers and substrate alignment.

Ceraslice is dedicated to the design (including: a gds files viewing, simulation step allowing the visualization of droplets overlapping).

1.2.3.2 Wettability characterization

- Contact angle and liquid surface tension

The wetting characteristics of ink-jetted drops on surfaces are crucial for controlling the formation of lines and patterns.

In 1805, Young has established a relationship between the interfacial tensions at the triple phase contact line, as shown in Figure 3-21 ^[46]. The relationship is shown in equation 4.10:

$$\gamma_{SG} = \gamma_{SL} + \gamma_{LG} \cos \theta \quad (4.10)$$

where γ_{SG} , γ_{SL} , γ_{LG} and θ are the interfacial tension between the solid and gas, the interfacial tension between solid and liquid, the interfacial tension between the liquid and gas, and the contact angle, respectively.

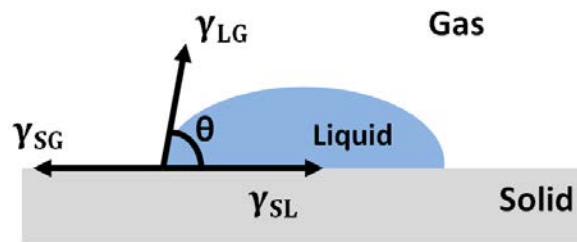


Figure 3-21: Schematics of the different interfacial tension at the triple phase contact line.

The contact angle θ , corresponding to the angle between vectors γ_{LG} and γ_{SL} , can be measured using a contact angle goniometer. In this work, KRUSS drop shape analyzer DSA30 is used to measure the contact angle. Usually, the surfaces with contact angle $\theta < 90^\circ$ are classified as hydrophilic, and those with contact angle $\theta > 90^\circ$ as hydrophobic. Note that, when $\theta > 110^\circ$, surfaces shows super-hydrophobic properties.

In order to measure the contact angle with DSA30, a drop is deposited on a surface.

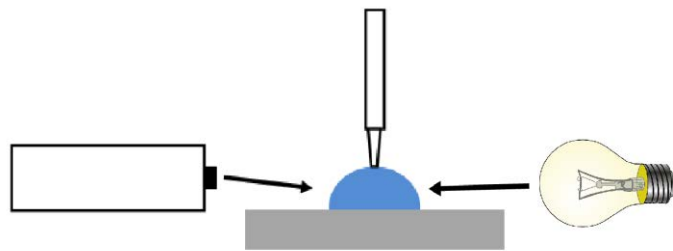


Figure 3-22: Schematic diagram of measuring principle of DSA30.

The drop is illuminated from one side and a camera at the opposite side records an image of the drop. The DSA30 software is used to calculate the contact angle. The schematic diagram of measuring principle of DSA30 is shown in Figure 3-22.

- Substrate surface energy characterization

Wu's method is used to calculate the surface energy of substrate using contact angle measurement with at least two liquids. The surface energy of the solid is the sum of polar and dispersive part.

At least two test liquids with known polar and dispersive parts are required for this method. Note that, at least, one of the liquids must have a polar part >0 . Water and diiodomethane are commonly used solvents.

Wu's initial equation for the interfacial tension between a liquid and a solid phase is as follows:

$$\gamma_{SL} = \gamma_{SG} + \gamma_{LG} - 4\left(\frac{\gamma_{LG}^D \times \gamma_{SG}^D}{\gamma_{LG}^D + \gamma_{SG}^D} + \frac{\gamma_{LG}^P \times \gamma_{SG}^P}{\gamma_{LG}^P + \gamma_{SG}^P}\right) \quad (4.11)$$

Equation (4.10) then is inserted in equation (4.11), and the following relationship is obtained:

$$\gamma_{LG} (\cos\theta + 1) - 4\left(\frac{\gamma_{LG}^D \times \gamma_{SG}^D}{\gamma_{LG}^D + \gamma_{SG}^D} + \frac{\gamma_{LG}^P \times \gamma_{SG}^P}{\gamma_{LG}^P + \gamma_{SG}^P}\right) = 0 \quad (4.12)$$

where γ_{LG}^D , γ_{LG}^P , γ_{SG}^D and γ_{SG}^P are the dispersive and polar parts of the surface tension of the tested liquid, the dispersive and polar parts of the surface energy of solid, respectively.

In order to determine γ_{SG}^D and γ_{SG}^P , the contact angles for two liquids on the solid surface are measured, and then using equation (4.12), for each liquid a system of equation is solved.

1.2.3.3 Rheological characterization

- Liquid surface tension characterization

The surface tension measurement is based on pendant drops. The pendant drop is a drop suspended from a needle in a bulk liquid or gaseous phase. The shape of the drop results from the relationship between the surface tension and gravity. In the pendant drop method, the surface tension is calculated from an optical image of a pendant drop using drop shape analysis.

An increased pressure is produced inside the drop as a result of the interfacial tension between inner and outer phase. The correlation between the pressure difference Δp , the radii of curvature of the surface r_1 and r_2 , and the surface tension is described by the Young-Laplace equation as follows:

$$\Delta p = \sigma \cdot \left(\frac{1}{r_1} + \frac{1}{r_2}\right) \quad (4.13)$$

This equation describes the difference between the pressure below and above a curved section of the surface of a drop with the principal radii of curvature r_1 and r_2 . The pressure difference Δp is the difference in pressure between the outside of the drop and its inside.

- Liquid viscosity characterization

The viscosity of a fluid is relative to resistance to gradual deformation by shear stress or tensile stress^[47]. Liquid is placed in between cone/plane geometry, which are adapted to

measure shear strain of small amount of liquid (100 μL). Equipment used in this works is a rheometer (Malvern kinexus lab+).

I.2.3.4 Printing Methodology

As described above, inkjet printing behavior is governed by numerous physical properties that can strongly impact final printing quality and consequently devices electrical characteristics in our case. Consequently, a rigorous printing methodology, as shown in Figure 3-23, must be followed in order to fabricate optimized devices. Indeed, performing all the steps of this methodology leads to avoid the drawbacks described in the previous subsections (i.e., jetting, wetting, drying).

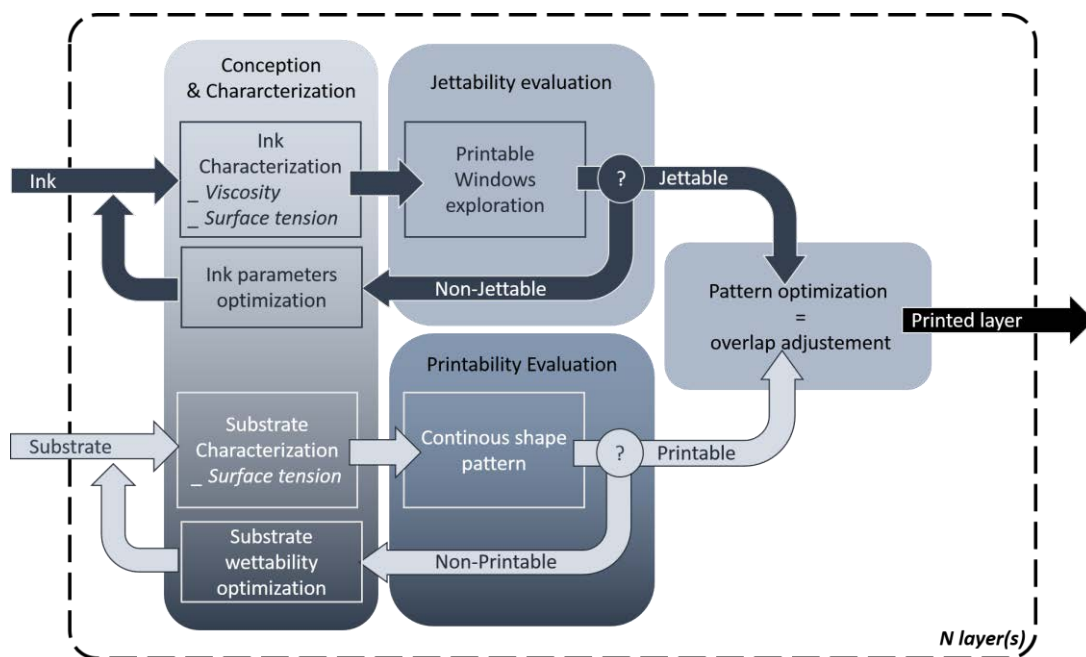


Figure 3-23: Printing methodology.

- **Printing methodology**

Before printing a layer, an extensive study of ink and substrate must be performed in order to obtain jettable and printable conditions, respectively. Note that, this methodology must be repeated for each layer that composed the desire device. For instance, OTFT is composed of 4 layers, as a consequence such methodology must be performed 4 times.

- **Ink jettability evaluation and optimization**

As described in sub-section I.2.2 “fluid requirement”, jettability is mainly governed by surface tension and viscosity. Consequently such physical properties must be determined prior to jetting. As described in sub-section I.2.2 “droplet generation (jetting)”, two kinds of inks

can be distinguished (i.e., home-made ink and commercial ink). Consequently, commercial ink is jettable and there is no need of material optimization. Only jetting waveform optimization such as firing voltage, jetting frequency is necessary. Concerning home-made ink, material optimization (e.g., adding solvents to adjust viscosity and/or surface tension...) is necessary in order to obtain a jettable ink. Moreover, the jettable windows exploration will lead to an extensive investigation on the versatility of such ink. For instance, in this thesis, epoxy based ink has been deeply investigated in order to obtain jettable ink with optimum physical characteristics. Indeed, adjusting ink viscosity allows the fabrication of insulator with thickness compatible with OTFT technology. In conclusion, home-made ink requires deeper investigation in order to fabricate jettable ink formulation but such ink is more versatile and can be easily adapted for many applications (tuning viscosity for instance)

- ***Surface wettability evaluation and optimization***

As described in sub-section I.2.2 “spreading, wetting & drying”, wettability is mainly governed by the energy of the surface that is not easily printable when it is hydrophobic because of contact line instability. Contact line instability can be observed by printing a line for instance. If the line splits in several macrodrops, the hydrophobicity must be carefully “decreased” until contact line is continuous. UV-ozone or O₂ plasma treatments are usually performed in order to control surface wettability and water contact angle measurement is a convenient way to measure surface energy.

- ***Patterns optimization***

The last step consists of patterns optimization using the well-adapted ink and surface. In general, printed structure is constituted of pixels (isolated droplets), vertical lines, horizontal lines, and rectangular patterns. A “vector test” pattern is designed to obtain the suitable printing parameters (essentially, overlap), as shown in Figure 3-24 (a) and (b).

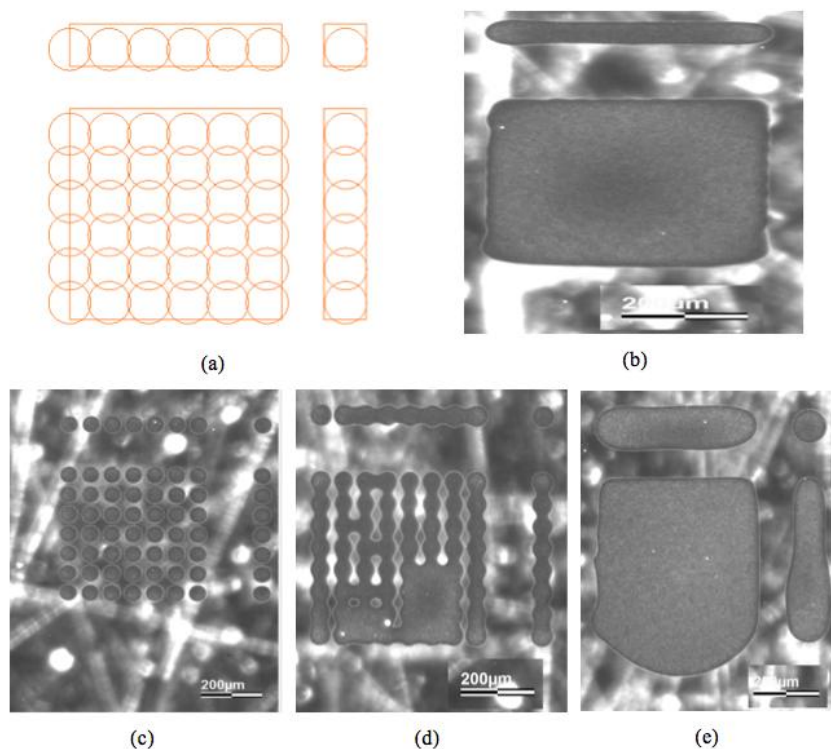


Figure 3-24: (a) “Vector test” design pattern; four basic morphology of printed line based on printing parameters: (b) Well printed pattern; (c) Isolated pattern; (d) Scalloped pattern; and (e) Bulging pattern. Silver ink was used for these experiments.

Printing “vector test” before printing the final desired patterns, is the best way to adjust overlap in order to avoid isolated droplets (c), scalloped line (d), bulging (e). The drop spacing increases from (c) to (e). Note that, “Vector test” patterns have to be printed on the same surface as the final device.

Part II: Inkjet printed OTFTs

After defining a methodology to study the printing of the layers constituting OTFTs and the whole OTFT's process, we will use it now to describe the fabrication and the characterization of OTFTs. The bottom-gate/bottom-contact structure of OTFTs will be used in this work (see in Figure 3-25).

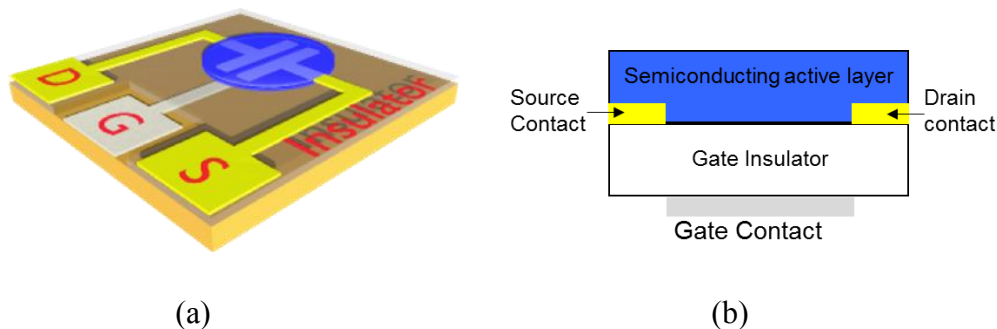


Figure 3-25: (a) Top-view and (b) cross-section of bottom-gate/bottom-contact structure of studied OTFTs.

The deposition steps of OTFTs follow this order:

- Gate contact,
- Gate insulator (Su8 photoresist used as gate insulator in this work),
- Source and drain contacts,
- Semiconducting active layer.

II.1 Printability of OTFT functional materials

Organic and printed electronics relies on electrically active materials that can be used as conductors, insulators and semiconductors. In this section, the printing methodology described previously is followed in order to qualify printing behavior of inks (silver ink, Su8 2000.5, and Tips-pentacene in solvent), which are used for OTFT fabrication.

II.1.1 Conductive ink

Silver nanoparticles based ink (Reference: Silver jet ANP40LT15C from Anapro) has been used in this study. Ink physical properties (Viscosity= 15 cPs, surface tension=35 mN/m, curing temperature ranging from 120°C to 150°C, nanoparticles diameter approximately equal to 50nm) allow the fabrication of conductive lines on glass or on plastic substrate such as PEN.

II.1.1.1 Jettability

This commercial ink is easily printable and doesn't require extensive jetting investigations. As consequence, only firing voltage and jetting frequency effects have been studied.

- ***Firing voltage***

Basically, firing voltage must be enough strong to push out the droplet, from the chamber, through the nozzle. But over a certain value the jetting behavior doesn't respect jettability criterions defined in subsection I.2.2 of chapter 3 part I. Moreover, higher firing voltages result in bigger and faster drops with longer tails; while, on contrary, lower firing voltages result in smaller and slower drops with reduced tails. This firing voltage is one of the most important parameter to set before printing.

More deeply, ink physical characteristics (i.e. viscosity, molecular weight...) have a strong impact on firing voltage value. For instance, on one hand, high-viscosity inks require higher firing voltages in order to prevent nozzles clogging. On the other hand, low-viscosity inks require lower voltages; otherwise drops are followed by long-lived filament satellites droplets or long tail. Consequently, particular attention must be paid to firing voltage adjustment step. Indeed, jettability criterions must be respected in order to fabricate highly accurate patterns (i.e., well defined source and drain in our case). Figure 3-26 shows silver ink droplet formation as a function of firing voltages. The formation of silver ink droplet varies from well-defined droplets to droplets followed by satellites droplets when the firing voltages increased from 50 to 70 V. Moreover droplet speed also increased drastically from (a) to (c). Stable droplets with volume of 13 pL, are obtained at firing voltage equal 50V and at jetting frequency equal 1 KHz.

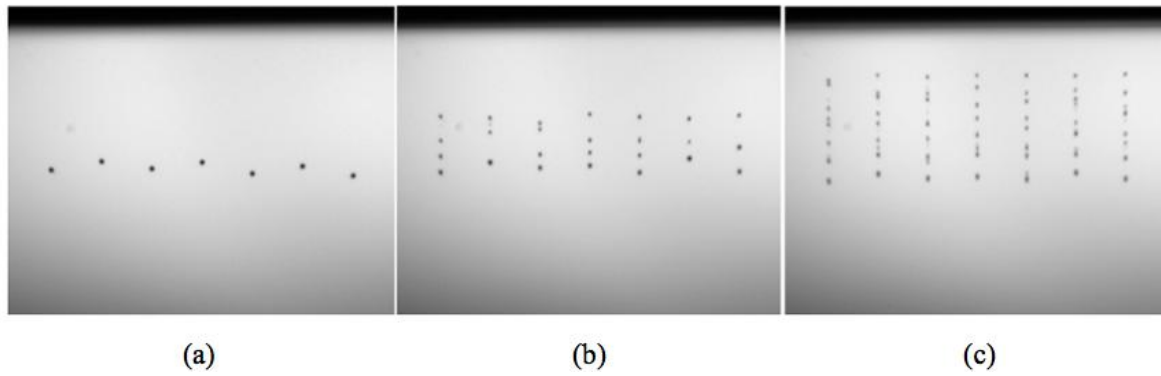


Figure 3-26: Optical pictures, acquired using stroboscopic camera of the printer, showing droplets formation of silver ink as a function of firing voltage: (a) 50 V, (b) 60 V, and (c) 70 V. Jetting frequency is fixed to 1KHz for all the experiments.

- **Jetting frequency**

Concretely, jetting frequency is correlated to the frequency of droplet deposition on the substrate. Consequently, the higher the jetting frequency is, the higher the printing velocity is. However, in general, printing at high frequency leads to unstable jetting behavior. Indeed, as shown in Figure 3-27 (a), (b), and (c), perfect jetting behavior is observed at 1 KHz (as shown in Figure 3-27 (a)). When jetting frequency increases more droplets are jetting for the same time laps (as shown in Figure 3-27 (c)) but importantly satellites droplets appears leading to unstable jetting (as shown in Figure 3-27 (b) and (c)).

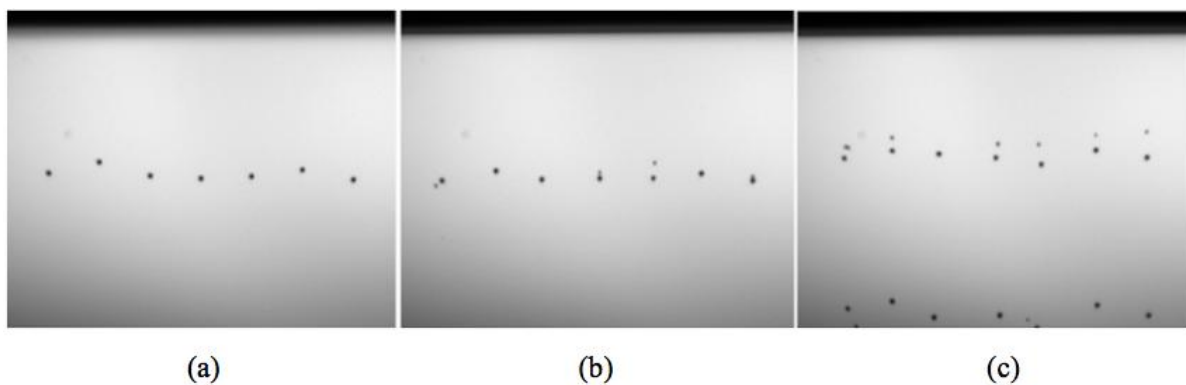


Figure 3-27: Droplet formation of silver ink in function of jetting frequency: (a) 1 KHz, (b) 3 KHz, and (c) 5 KHz.

In conclusion, concerning the jettability, optimum parameters have been determined. Firing voltage and jetting frequency will be fixed at 50 V and 1 KHz, respectively. These parameters will be kept constant for the rest of this work.

II.1.1.2 Morphology on hydrophilic substrate

In this thesis, most of experiments have been performed on glass substrate. Printed OTFT using bottom-gate and bottom-contact structure has been fabricated and consequently, gate has been directly printed on glass substrate. Consequently, following the printing methodology described above, the wetting properties of glass must be characterized before the pattern optimization step.

- **Wetting**

- **Basic characterization**

It is well-known that glass is hydrophilic but in order to follow rigorously the printing methodology, wetting properties of glass has been determined. As we expected, glass substrate shows low water contact angle (i.e., hydrophilic behavior) and high surface energy equal 67 mJ/m^2 , as shown in Figure 3-28 and Table 3-1.

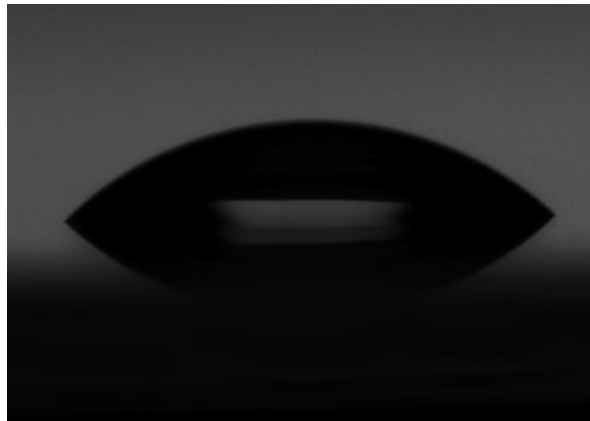


Figure 3-28: Water contact angle on glass substrate.

	Water	Diiodomethane
Surface tension (mJ/m ² @ 20°C)	72.8	50.8
Dispersion (mJ/m ² @ 20°C)	21.8	49
Polar (mJ/m ² @ 20°C)	51	1.8
Contact angle (°)	32	48
Surface energy (mJ/m ²)	67	

Average values were obtained from more than 10 measurements.

Table 3-1: Contact angle measurement of glass substrate for Wu's method.

➤ **Printability**

As shown in Figure 3-29 (a), the droplet diameter after drying also named “splat” is equal to 60 μm that is an expected value for a hydrophilic substrate. Such interestingly value gives important information: The minimum line width that can be fabricated will be approximately equal to 60 μm. Consequently, gate will have a poorer resolution on glass substrate compare to patterns achieved on more hydrophobic surface (dealing with printing on hydrophobic substrate in section II.1.1.3 in chapter 3 part II). However, it is not a drawback for the achievement of OTFT in bottom-gate and bottom-contact configuration where gate will have overlap with source and drain electrodes. Moreover, optical picture in Figure 3-29 (b) shows that a continuous line can be easily fabricated with line width equal 64μm. Indeed, as explained in subsection I.2.2.2 in chapter 3 part I, liquid contact line is stable (firmly pinned) on hydrophilic substrate. Such results clearly show that interactions between silver ink and glass substrate are well adapted and patterns optimization step can be performed.

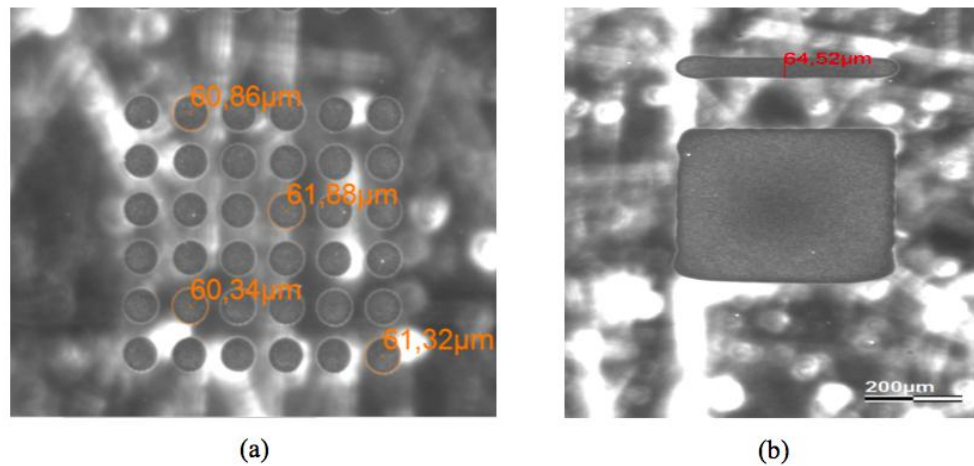


Figure 3-29: (a) Splat diameter of printed silver ink on glass, (b) Printed line.

- **Patterns optimization**

- **Gate requirement**

Gate is the first deposited layer of OTFT structure in bottom-gate and bottom-contact configuration. Obviously, it must be conductive that's why silver ink has been chosen. From morphological point of view, this layer must be continuous in the X-Y plane, but its thickness and its morphology are also important points as they can affect the deposition of layers on top of the gate. In general, the gate electrode of bottom-gate structure should be as thin as possible. When this condition is satisfied, source, drain and semiconductor can be deposited on a planar insulator in order to minimize the "complication of electric field" on a curve surface. Indeed, the role of thickness and morphology has already been reported ^[48]. In this relevant study, Tokito *et al* have shown that optimization of the electrodes profile (i.e., from convex to concave) strongly reduces OTFT leakage current (I_{GS}).

Consequently, in the following subsections: i) drop spacing has been investigated in order to define optimized parameter allowing continuous patterns fabrication, ii) experimental parameter (substrate temperature) has been studied in order to observe its impact on morphology.

- **Drop spacing impact (overlap impact)**

Drop spacing between centers of two adjacent droplets has been varied in order to obtain optimized patterns that must be continuous including no scalloping or bulging. Figure 3-30 shows optical images of the printed silver ink using "Vector Test" patterns with different

drop spacing. The drop spacing varies from 70 to 20 μm each 10 μm (Figure 3-30 from (a) to (f)).

When drop spacing is higher or equal to splat diameter, isolated droplets are observed and consequently patterns are not continuous (Figure 3-30 (a) and (b)). When drop spacing is lower than splat diameter, scalloped patterns are observed (Figure 3-30 (c)). When drop spacing decreased too much, too many materials are deposited and bulging effect are observed (Figure 3-30 (e) and (f)). Such phenomena are more and more exacerbated until patterns are totally unrecognizable (Figure 3-30 (d)).

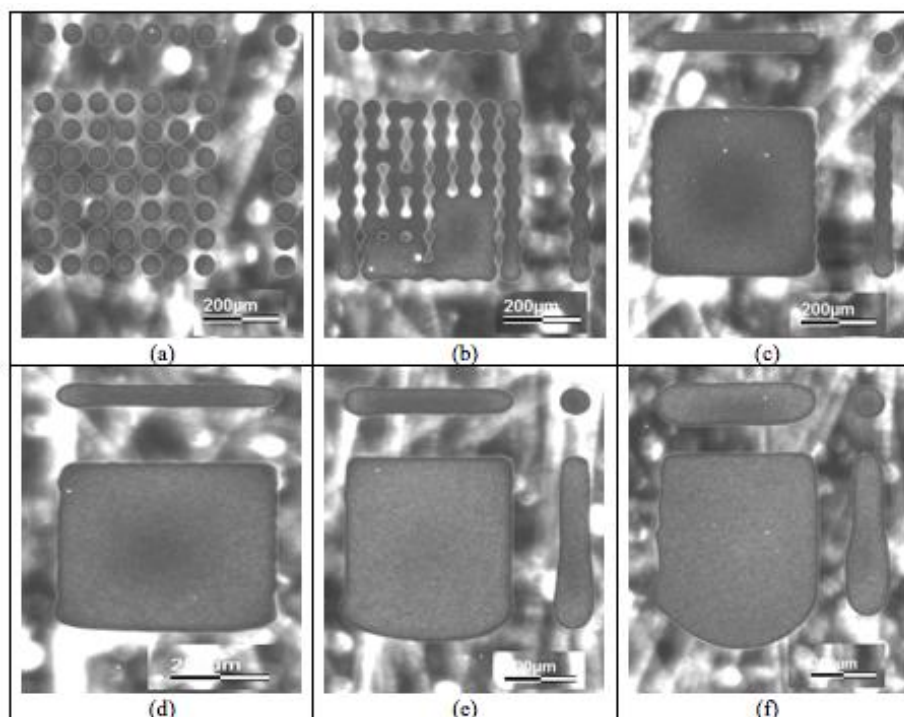


Figure 3-30: Optical images showing drop spacing effect. Drop spacing varies from 70 to 20 μm each 10 μm from (a) to (f).

As clearly, shown above, drop spacing has a strong impact on X-Y plan resolution (i.e., 2D resolution). Moreover, it has also be clearly shown that drop spacing has a strong impact on material amount deposited on the surface and consequently on the patterns thickness (3D resolution). Such assertion can also be observed in Figure 3-31.

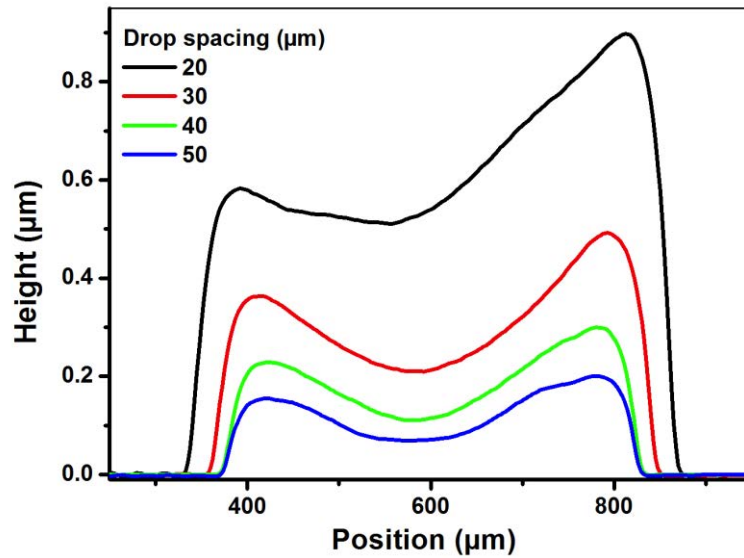


Figure 3-31: Cross-section view obtained with a profilometry measurements of the printed silver patterns showing patterns thickness evolution as a function of drop spacing.

Figure 3-31 shows that thickness is not constant along profile due to coffee stain effect. Indeed, the film thickness is higher at the edge than in the center. Consequently, for gate printing drop spacing value of 40 μm has been chosen. Indeed, such parameter allows the formation of continuous film as thin as possible. However, other investigations have been performed in order to decrease coffee ring effect.

➤ **Substrate temperature impact**

Coffee ring effect has been firstly observed using single droplet as shown in Figure 3-32. Indeed, it has been judged more convenient to observe the phenomenon using single droplet than square shape printed films.

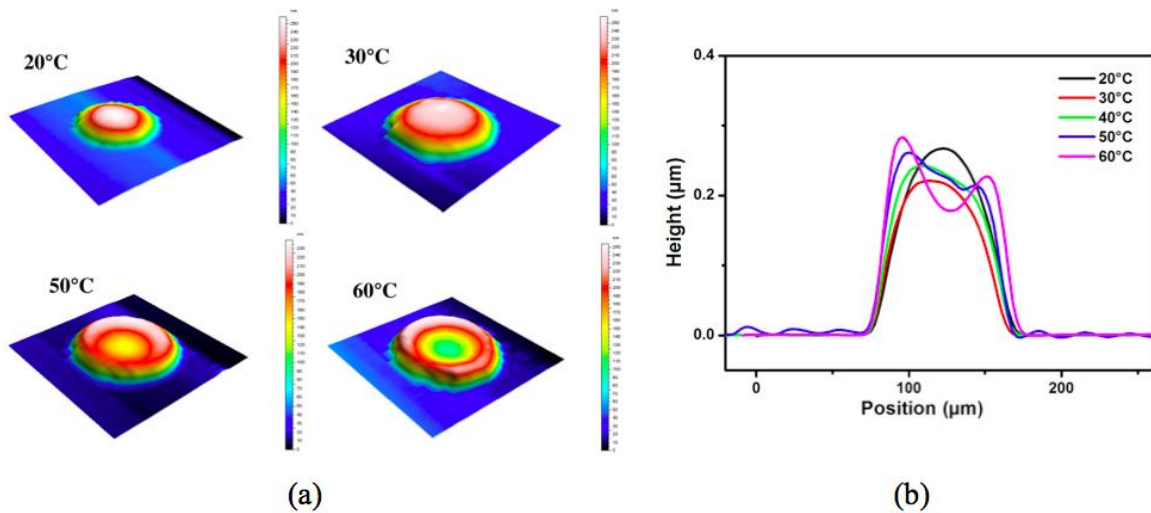


Figure 3-32: Morphological behavior of printed droplet on glass as a function of drying temperature. (a) 3D picture; (b) Cross-section profiles.

Figure 3-32 clearly shows that the increase of temperature exacerbates coffee ring effect. As expected, at low temperature (20°C) droplet have more time to dry. This phenomenon has ever been observed in literature ^[49]. Consequently, convex or concave droplets profile can be achieved by cleverly choosing drying temperature. However, concerning gate requirements large size patterns have to be fabricated. Consequently, same experiments have been performed on square shape profiles, as shown in Figure 3-33.

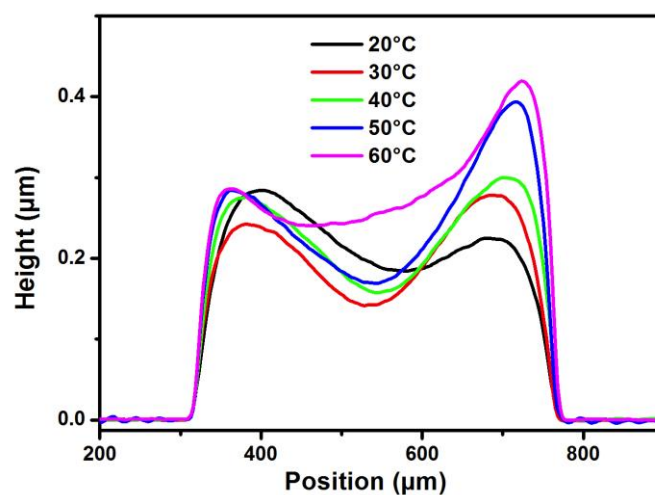


Figure 3-33: Morphological behavior of printed square shape pattern on glass as a function of drying temperature (cross section profiles). Drop spacing is equal to 40 μm.

Figure 3-33 confirms observations made previously. Increasing drying temperature leads to enhance coffee ring effect. However, in this case, coffee ring effect can't be totally suppressed. Unfortunately, using commercial silver ink, experiments can't be easily performed on ink composition (e.g. solvent). Consequently, drop spacing value of $40\mu\text{m}$ and substrate temperature value of 30°C has been chosen. Indeed, such values are the best ones to fit gate requirements.

➤ *Electrical characterization*

To optimize the conductivity of the electrodes, the sintering of the silver patterns is characterized. Resistivity was measured on the printed square-shaped pattern with a length of 5mm and printed parameters of drop spacing $40\mu\text{m}$, substrate temperature 30°C , using four-point probe method. Figure 3-34 shows the printed silver resistivity as a function of sintering temperature and time. For all the tested temperature optimum resistivity (typically $2.2 \times 10^{-5} \Omega \cdot \text{cm}$) is obtained after 35 minutes.

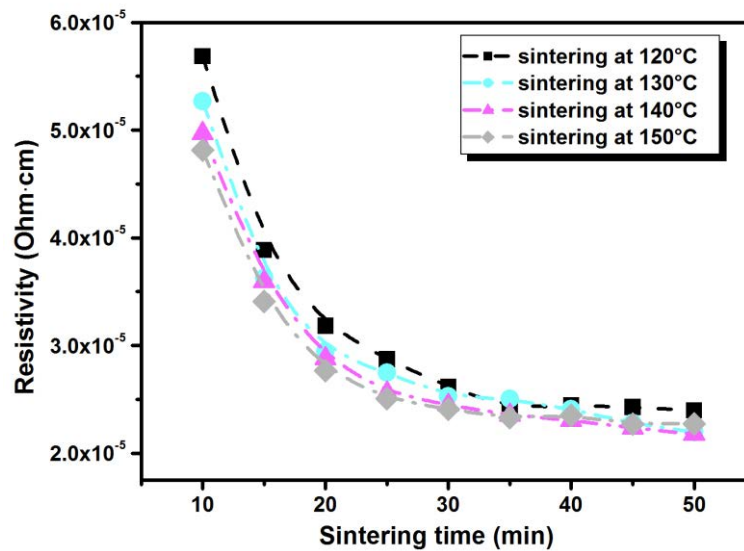


Figure 3-34: Printed silver resistivity as a function of sintering temperature and time.

Moreover, the printed silver resistivity as a function of drop spacing has also been characterized. Table 3-2 shows the resistivity when drop spacing varied from 10 to $40\mu\text{m}$. Resistivity is obtained after sintering at 120°C for 1 hour.

Drop spacing (μm)	Pattern thickness (μm)	Resistivity ($\times 10^{-5} \Omega \cdot \text{cm}$)
10	9	1.47
20	1.2	1.41
30	0.45	1.5
40	0.2	1.45

Table 3-2: Resistivity as a function of drop spacing.

In conclusion, the sintering temperature is compatible with Su8 maximum processing temperature (120°C), and drop spacing has no impact on resistivity.

➤ **Optimized parameter**

Optimized parameters are summed up in Table 3-3.

Parameter	Silver ink
Drop spacing	40 μm
Firing voltage	50 V
Maximum jetting frequency	1 KHz
Printing nozzles	1
Substrate temperature	30°C
Cartridge print height	700 μm
Number of layers	1

Table 3-3: Printing parameters for silver ink.

II.1.1.3 Morphology on hydrophobic substrate

● **Wetting**

➤ **Basic characterization**

In this work, silver ink is printed on Su8 as source and drain electrodes. Su8 surface is more hydrophobic than glass; consequently, wetting properties of Su8 surface have been determined in order to understand printing behavior. As expected, Su8 surface shows higher water contact angle than glass and lower surface energy, as shown in Figure 3-35 and Table 3-4.

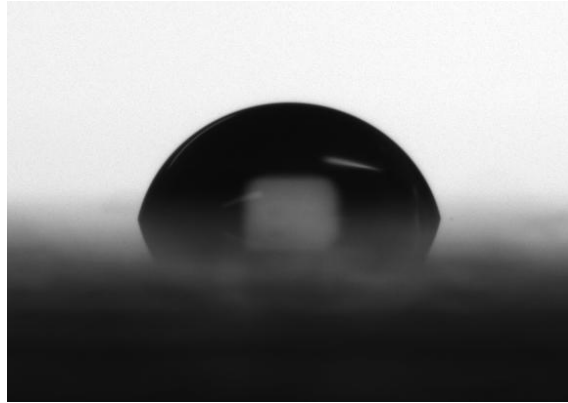


Figure 3-35: Water contact angle on Su8 surface.

	Water	Diiodomethane
Surface tension (mJ/m ² @ 20°C)	72.8	50.8
Dispersion (mJ/m ² @ 20°C)	19.9	49.5
Polar (mJ/m ² @ 20°C)	52.2	1.3
Contact angle (°)	86.5	48.79
Surface energy (mJ/m ²)	45.30	

Average values were obtained from more than 10 measurements.

Table 3-4: Contact angle measurement of Su8 for Wu's method.

➤ **Printability**

The silver droplet diameter after drying as shown in Figure 3-36 (a) equals 42 μm that is smaller than this one printed on glass.

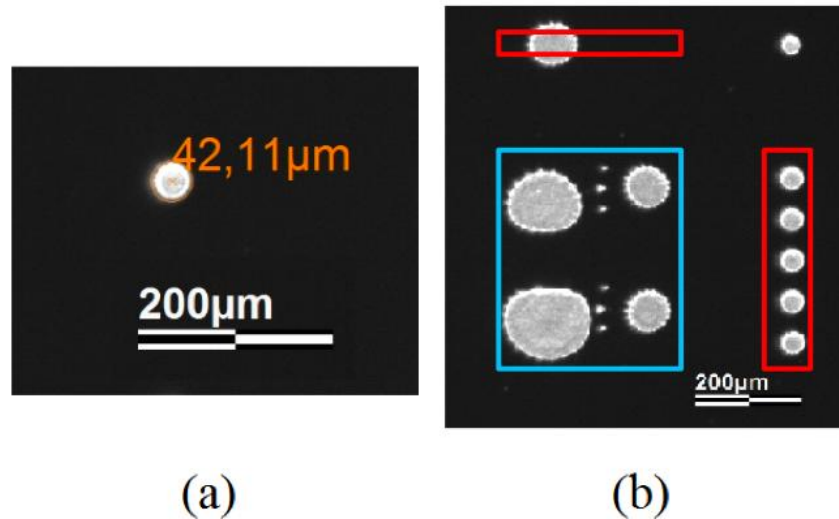


Figure 3-36: (a) Splat diameter of printed silver ink on Su8, (b) Printed “Vector Test” showing dewetting. Blue and red indicate the shape of the designed patterns.

Optical picture in Figure 3-36 (b) shows that “dewetting behavior” is observed when “Vector Test” is printed on Su8. Indeed, square-shaped patterns (blue area) and lines (red areas) can’t be printed accurately (ink split into several droplets). This phenomenon can be attributed to rivulet instability which is frequently observed when ink is printed on hydrophobic surfaces.

Consequently UV-ozone treatment has been performed in order to decrease the hydrophobicity until contact line will be more firmly pinned.

➤ *Impact of UV-ozone*

UV-ozone treatment is a well-known method in order to increase the polymer surface hydrophilicity. UV-ozone treatment is a gentle surface modification method compared to wet and dry pre-treatment methods. Wet pre-treatment methods usually utilize a chemical agent that reacts with hydroxyl and/or carboxyl groups generated by acid and/or alkali treatment [50-52]. Dry pre-treatments usually utilize oxygen or ammonia plasma. In both cases, surface roughness increases significantly. The roughness of Su8 surface is not affected by UV-ozone treatment [53]. Although, UV-ozone treatment doesn’t increase Su8 surface roughness, it creates polar groups at the polymer surface [54]. The impact of surface roughness on electrical characteristics will be discussed in next chapter. However, it is also well-known that UV-ozone treatment is not a permanent chemical modification. Indeed, this effect disappeared

after one hour approximately. As a consequence, UV-ozone is the method of choice in order to control the hydrophobicity of a polymer in the field of inkjet printed technology.

Contact angle and splat diameter on Su8 surface have been measured as a function of UV-ozone exposure time. Figure 3-37 (a) shows that the water contact angle can be significantly reduced by exposing Su8 to UV-ozone. Consequently, the increase of splat diameter shows that hydrophilicity of Su8 can be easily control using UV-ozone treatment.

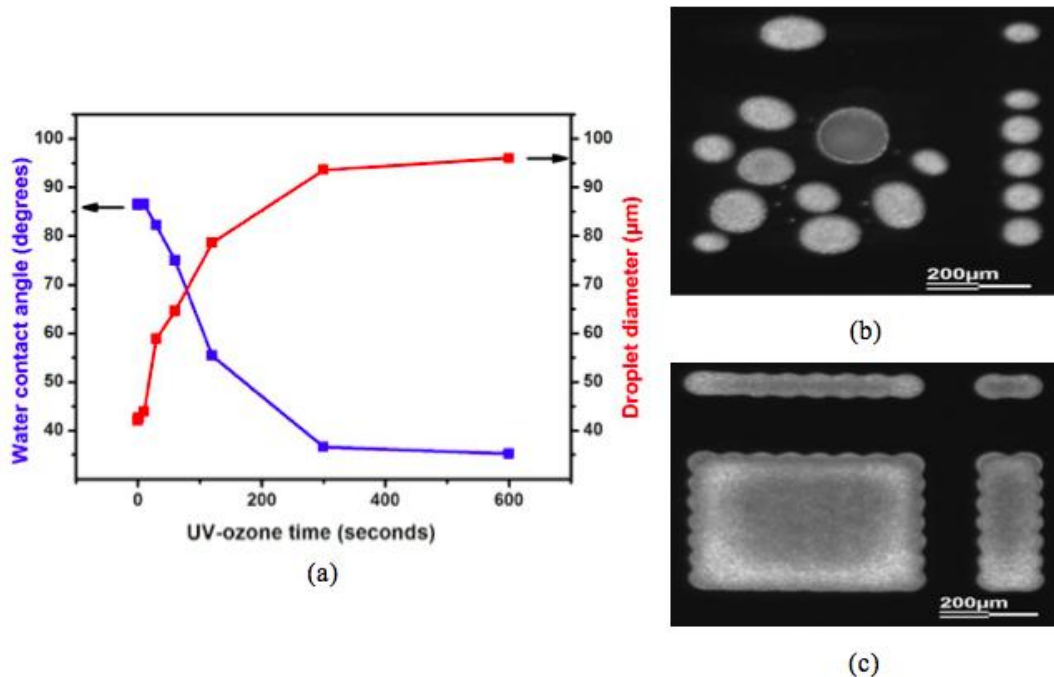


Figure 3-37: (a) Water contact angle on Su8 and droplet diameter as a function of UV-ozone exposure time, (b) Patterns showing dewetting: UV-ozone exposure time equals to 30s, (c) Pattern showing no dewetting: UV-ozone exposure time equals to 1min.

In more detailed, Figure 3-37 shows that UV-ozone treatment effect is observed after 30 seconds. Indeed, water contact angle and droplet diameter doesn't change before 30 seconds. Between 30 seconds and 300 seconds wetting behavior is strongly impact by UV-ozone (water contact angle decreases from 85° to 30° and droplet diameter increases from 45 to 95 μm). After 300 seconds, UV-ozone effect is insignificant. Importantly, optical picture of Figure 3-37 (c) show that after 1 minute UV-ozone treatment well-defined patterns can be fabricated. As a consequence this results show that Su8 after UV-ozone treatment is a printable thin film, that can be used as insulator layers for inkjet printed OTFTs.

In order to deeply characterize Su8 printability, the evolution of line thickness as a function of UV-ozone exposure time has been performed (see in Figure 3-38).

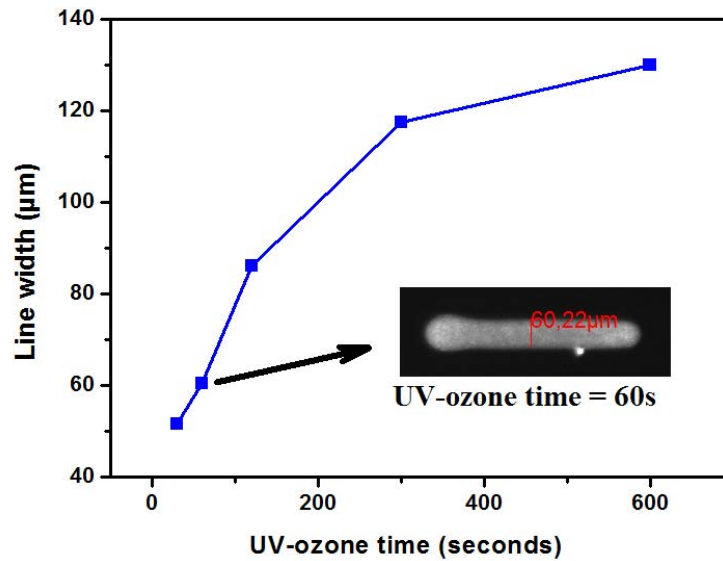


Figure 3-38: Printed line width as a function of UV-ozone exposure time. Drop spacing is 40 μm .

Figure 3-38 shows that printed line width is strongly impacted by UV-ozone exposure time. Indeed, line width is almost three times larger when UV-ozone exposure time increased from 1 to 10 minutes. For the rest of the work UV-ozone exposure time has been fixed at 1 minute in order to fabricate source and drain electrodes with a small width.

- **Patterns optimizations**

- **Requirements**

In bottom-gate and bottom-contact configuration, source and drain electrodes are printed on insulator (Su8 in this study). Channel length will be defined by the distance between these two electrodes. Channel length has to be as short as possible. As explained previously, if overlap parameter is not well optimized, the printed patterns are not well defined. In our case, bulging must be avoided because it can lead to source and drain electrodes connecting. As a consequence, drop spacing has been carefully optimized.

- **Drop spacing impact**

“Vector Test” patterns with different drop spacing have been printed on Su8 in order to optimize the drop spacing. Figure 3-39 and Figure 3-40 show the optical pictures of printed “Vector Test” and morphological characterization, respectively.

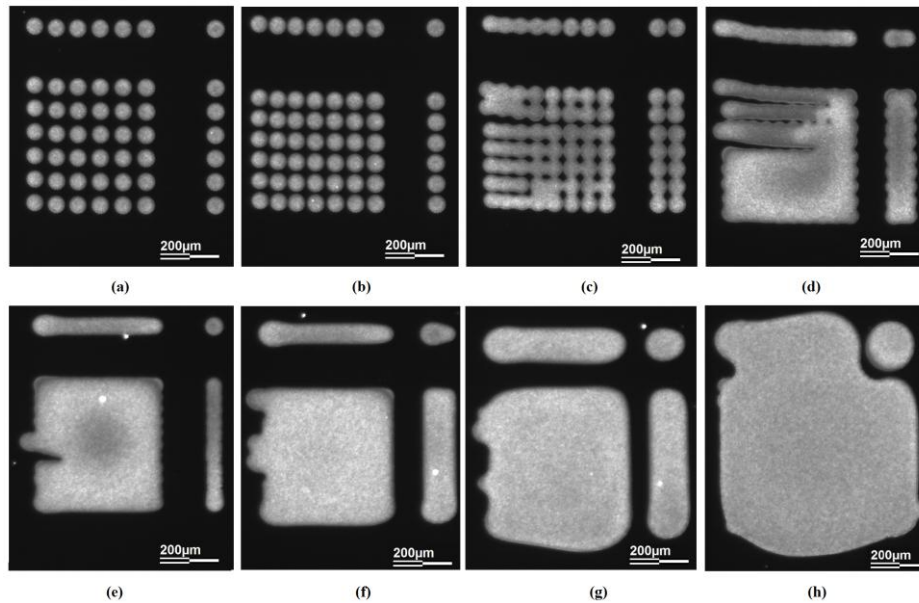


Figure 3-39: Optical images showing drop spacing effect. Drop spacing varies from 65 to 30 μm each 5 μm from (a) to (h).

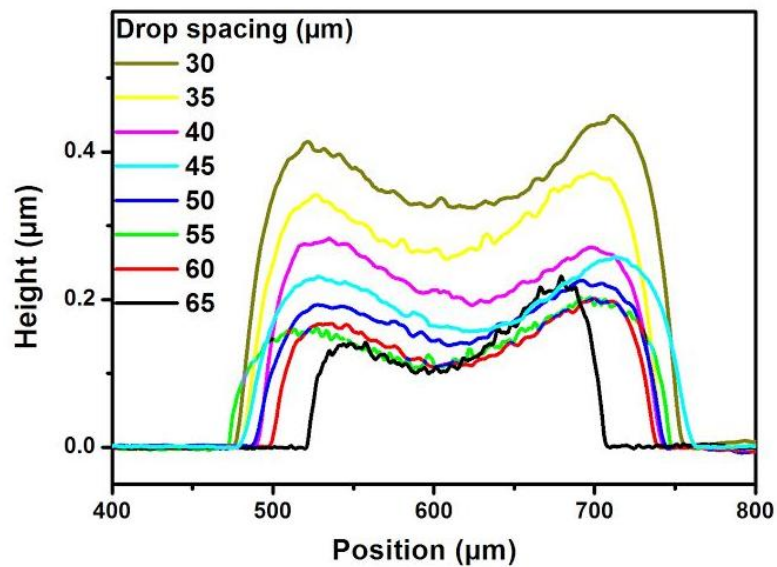


Figure 3-40: Cross-section view obtained with a profilometry measurements of the printed silver patterns on Su8 showing patterns thickness evolution as a function of drop spacing.

As shown in Figure 3-39 and Figure 3-40, drop spacing has a strong effect on resolution of both 2D and 3D.

In summary, when printing source and drain on Su8, after UV-ozone treatment, the surface of Su8 is more hydrophilic, drop spacing of 40 μm is the optimum value leading to obtain line without bulging effect.

II.1.2 Insulator Ink

II.1.2.1 Requirements

As explained previously, Su8 photoresist has been used as insulator layers. Su8 2000.5 processing is well known. However, in field of inkjet printing, it was not commercialized as printable ink. Note that, at the end of this work, MicroChem has launched a commercial ink named Prielec which are based on Su8 photoresist. Indeed, as demonstrated in this study, epoxy based ink (Su8 ink) is a versatile ink allowing the fabrication of devices in the field of printed electronic.

In this section, as epoxy based ink is not a commercial ink, a deeper investigation on its jettability, including jettable windows exploration, will be detailed. Moreover, optimization of insulator morphology and thickness will be performed in order to fit OTFT requirements.

II.1.2.2 Jettability

Understanding the droplet generation mechanism is essential to study custom ink as epoxy based ink used in this work. The idea developed in this section consists of defining jettable bounds (printable windows) of epoxy based ink system. Indeed, inside the printable window (defined previously), optimized jetting conditions will lead to easily tune the droplet velocity and volume leading to an accurate printing. As described in chapter 3 part I, jettability is complex and governed by inertial, viscous, and surface tension forces. Dimensionless numbers including Reynolds (Re), Weber (We), Capillary (Ca), and Z number characterize the droplet formation process.

In order to fully describe Su8 2000 series based ink, a wide concentration range of epoxy based inks must be characterized from a jettability point of view. In this work, we will study inks with three epoxy based ink dilutions whose physical properties are listed in Table 3-5. Moreover, pure cyclopentanone based ink will also be tested as it is the major component of Su8 2000 series based ink with the lowest ink viscosity used in this study.

Ink	η (cp)	σ (mN/m)	ρ (g/mL)
Epoxy ink 3	15.50	33.20	1.15
Epoxy ink 2	7.50	34.00	1.12
Epoxy ink 1	2.49	35.00	1.07
Cyclopentanone	1.00	33.40	1.00

Table 3-5: Physical parameters of epoxy based inks. Epoxy ink 1, 2, 3 corresponds to Su8 2000.5, Su8 2000.2 and Su8 20005, respectively.

Printable windows in a Ca-We coordinated system can be defined by varying droplet velocity. This can be done by tuning voltage applied on piezoelectric actuators. Using experimental data on obtained velocity, rheological parameters (Table 3-5) and equation (4.8), Weber as a function of Capillary (We versus Ca) is plotted for all the tested functional inks, as shown in Figure 3-41.

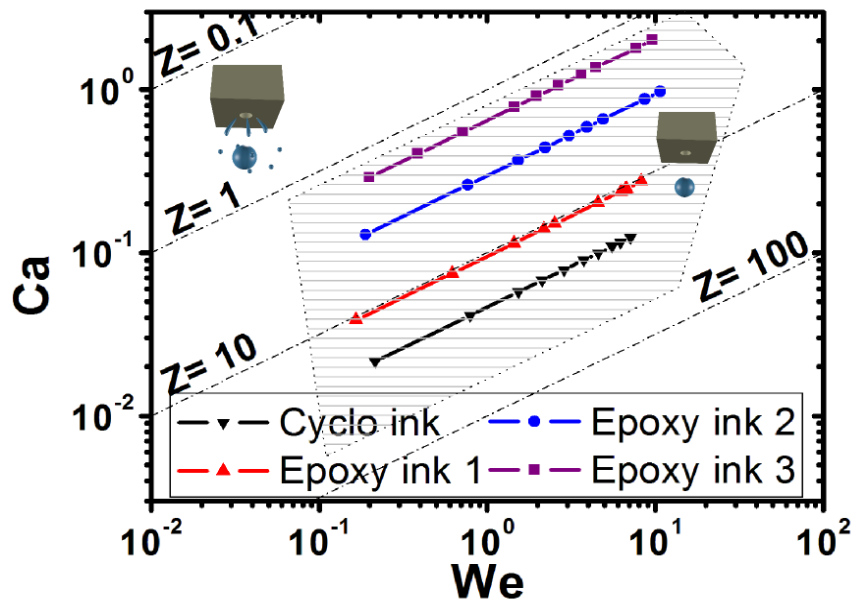


Figure 3-41: Inkjet qualification strategy represented in a Capillary number (Ca) -Weber number (We) coordinated system of the printable inks tested. For each ink, each data point reports a printable condition corresponding to a different velocity. Hatched area: The printable window defined by Subramanian^[34]. Scheme inside the hatched area illustrates well-defined drop jetted from a nozzle. Scheme outside the hatched area illustrates inappropriate jetting conditions (i.e., main drop plus additional satellites droplet).

Results reported on Figure 3-41 show that cyclopentanone and epoxy ink 3, which are the lowest and the highest tested viscosities, respectively, are the printability bounds. This interesting set of experiments demonstrates that epoxy based inks match the same printable windows than the one defined using nanoparticle based ink or pure solvent based ink [34]. It means that ink based on low-molecular-weight components (e.g., epoxy base ink) shows stable printing behavior over a large range of printing conditions. Data related to cyclopentanone reported in Figure 3-41 correspond to high Z values that are far away from the lower printability limits defined by the printable window ($Z = 60$).

This result shows that cyclopentanone is a convenient solvent for inkjet printing technology. As a consequence, very high epoxy dilution in such solvent could be performed to obtain very low film thickness. One could notice that another interesting asset of cyclopentanone printability relies on its use as ink to locally etch Su8 in order to achieve via for electrical interlayer connections. This concept has already been published using alcohol-based ink to etch poly (4-vinylphenol) films [55].

In conclusion this set of experiments constitutes a solid dataset in order to achieve devices with epoxy based ink. However, in this work, all the epoxy based ink dilutions have not been tested for the fabrication of OTFT but will pave the way to other studies. Epoxy based ink 1 has been chosen because it is “in the middle” of printable windows ($Z=10$) and consequently it presents the highest printability.

II.1.2.3 Morphology

In order to fabricate inkjet printed OTFT, requirements have to be satisfied. Indeed, insulator thickness must be controlled in order to avoid leakage current I_{GS} for instance. Consequently, thickness of insulator has been extensively studied using inkjet printing parameters such as drop spacing and substrate temperature. Moreover, insulator layers need more time to print than gate electrodes for instance. Indeed, insulator area is higher than electrodes areas. Consequently, two printing methods have been also studied: The first one uses only one activated nozzle (single-nozzle-printing) and the other uses several nozzles (multiple-nozzle-printing), typically from 1 to 16 (i.e. the maximum number of nozzles available using Dimatix cartridge).

- **Single-nozzle-printing**

- **Printing behavior (isolated droplets)**

As described in section II.1.1, isolated Su8 droplets have been printed on glass substrate in order to understand the drying behavior of epoxy based ink. Indeed, such experiments are mandatory to determine diameter of single droplet (i.e., useful information in order to fix drop spacing range for square shaped films (see in II.1.1.3) and its height).

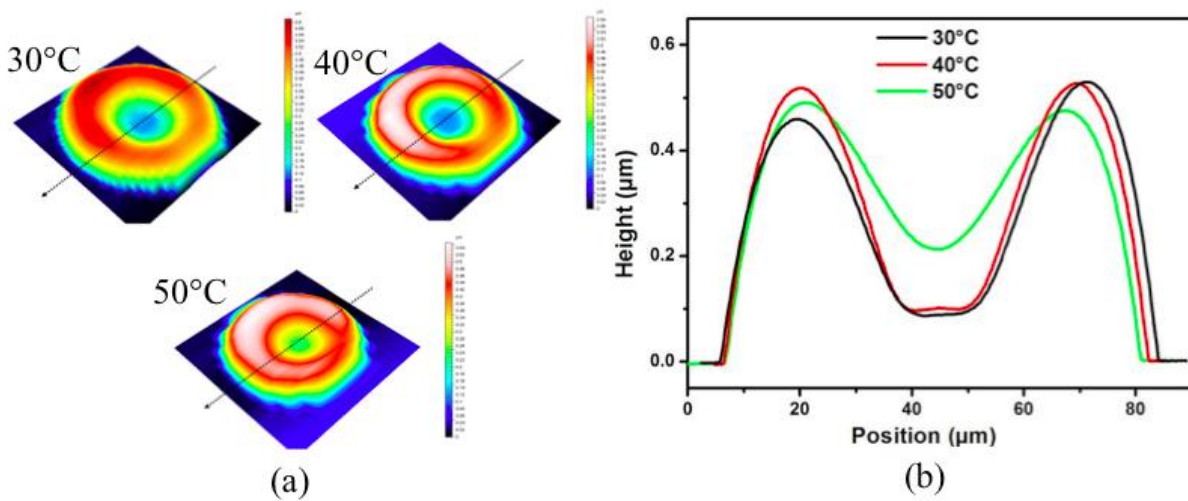


Figure 3-42: (a) Morphological behavior of printed single-droplet-Su8 as a function of substrate temperature: 30°C, 40°C and 50°C. (b) Corresponding two-dimensional profile. 3D pictures and corresponding profiles extracted along the dashed lines of $110 \times 110 \mu\text{m}^2$ square-shaped thin films.

Figure 3-42 shows that droplet diameter, equal to $70\mu\text{m}$, is independent of temperature. However, as observed for silver ink, coffee ring effect is observed. A substrate temperature of 50°C leads to decrease such effect (i.e., recirculation flow are induced). Increasing temperature beyond 50°C could be an interesting way to obtain more uniform films but is technically impossible with the printer used in this study. Moreover, a higher substrate temperature could also dramatically lead to nozzle clogging and constitutes an experimental limitation.

Consequently, experiments performed on square shaped films will be performed at 50°C .

➤ **Printing behavior (film)**

Drying mechanisms are more complex for a film than for an isolated droplet because of the printing sequence described as follows: droplets coalesce along X-axis form one line and lines coalesce along Y-axis form the film. So, additional parameters must be taken into account in order to describe the film drying behavior such as printing frequency and overlap between printed droplets. For this study, printing frequency is fixed at 1 KHz corresponding to $35 \text{ m/s} < V_{(\text{print})} < 50 \text{ m/s}$ depending on overlap distance between droplets. Figure 3-43 shows 3D views and their corresponding profile of $600 \times 600 \mu\text{m}^2$ square-shaped thin films as a function of drop spacing. Note that ink excess is observed essentially at the beginning of the patterned area. The phenomenon has already been described in the literature and seems to be due to the pressure difference in the film along the printing direction, which is strong enough to pump the liquid at the film start [56]. For practical applications, this ink excess must be taken into account and must be out of the active area.

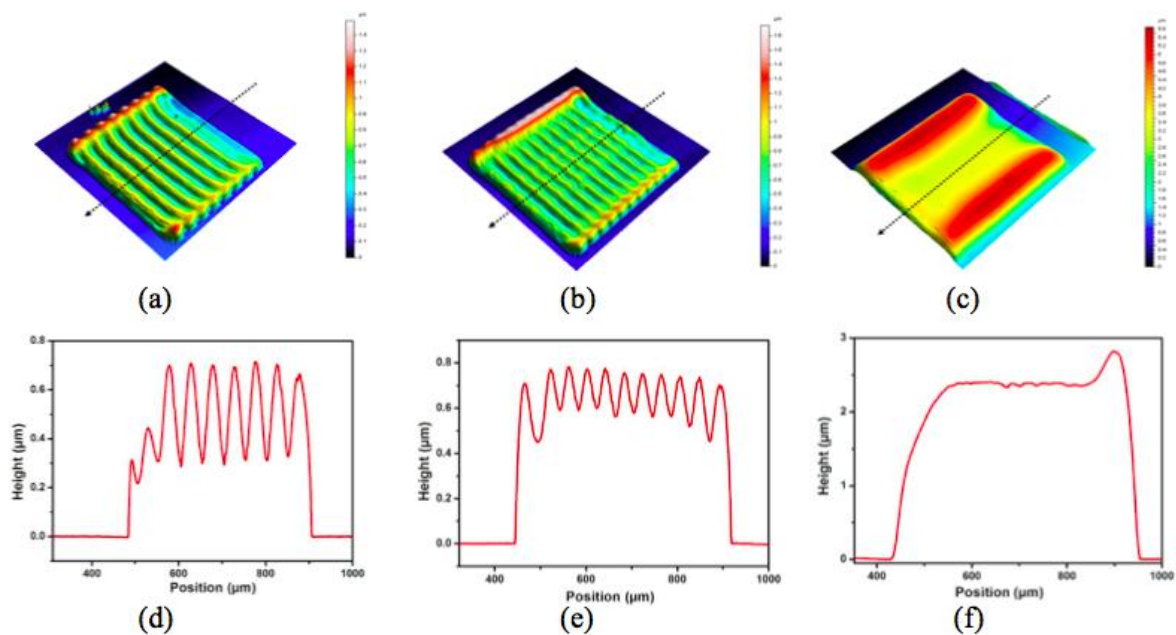


Figure 3-43: Morphological behavior of printed Su8 using single-nozzle as a function of drop spacing: (a) drop spacing = $50 \mu\text{m}$, (b) drop spacing = $40 \mu\text{m}$, and (c) drop spacing = $10 \mu\text{m}$. (d) (e) and (f) are the corresponding two-dimensional profiles of (a) (b) and (c), respectively.

3D pictures and corresponding profiles extracted along the dashed lines of $600 \times 600 \mu\text{m}^2$ square-shaped thin films.

Figure 3-43 shows that two different morphologies can be obtained: from periodically waved film to smoother film. Keeping fixed temperature ($T_{\text{substrate}} = 50\text{ }^{\circ}\text{C}$) and increasing overlap drastically reduces the amplitude of the waves and the period until reaching a smooth film. For this experiment, drying is governed by outward flow and two mechanisms must be taken into account in order to describe film formation in the pattern center. At low overlap, the film formation must be considered at the microscopic scale (lines). Below an overlap limit, the lines are formed independently of each other and the evolution of the wavy-shaped profile is due to the local coffee ring effect, as shown in Figure 3-43 (a) and (d). When the overlap threshold value is reached, there is enough solid on the same surface area (the contact line is pinned) to overcome the coffee ring effect at the local scale. As shown in Figure 3-43 (b) and (e), the lines began to merge. At high overlap, the film formation must be considered at macroscopic scale (films). Adding material at the pinned contact line leads to the increase of the film thickness by passing the coffee ring effect (Figure 3-43 (c) and (f)). Note that such results could be obtained with film thickness between 400nm to several micrometers. Consequently, due to the versatility of epoxy based ink, the fabrication of printed OTFT using single nozzle can be envisaged. However, such printing method needs a long printing time (more than 1 hour to print a 5×5 cm substrate). Consequently, investigations on multi-nozzle-printing have been performed.

- Multi-nozzle-printing

Using single-nozzle-printing, drop spacing is controlled by the adjustment of print-head motor step in the X-axis direction (fabrication direction). Consequently, a line is printed thanks to droplets coalescence. In order to print wider patterns, print-head is moved in Y direction and a second line is printed. Coalescence of two lines is also control using print-head motor step adjustment in Y direction.

As shown in Figure 3-44, using multi-nozzle-printing, the adjustment of Y-axis overlap is performed by tilting the print-head because of the distance between nozzles ($21\mu\text{m}$ for Dimatix cartridge) is fixed. In this case, the angle value of print-head fixes the drop spacing.

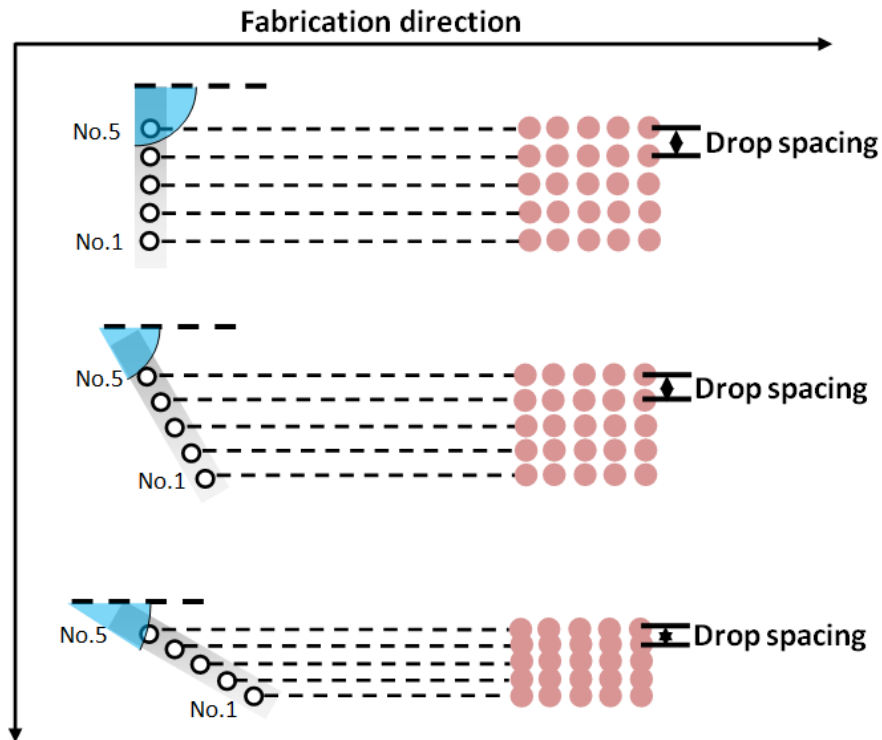


Figure 3-44: Schematic shows drop spacing using print-head angle adjustment.

Using multi-nozzle-printing method, higher printing velocity is obtained. Such printing method is more interesting from industrial point of view.

Figure 3-45 shows the morphological results of printing Su8 patterns as a function of activated nozzles (one, three, five or sixteen). As expected, at fixed overlap, when more nozzles are activated, wider patterns are printed. Interestingly, even if peaks are observed on pattern edges, smooth valley is obtained. Such interesting behavior is useful for OTFT fabrication. Indeed, source and drain electrodes will be printed on top of insulator, using 16 nozzles shows a smooth and large enough area to print such electrodes. In contrary, using 3 nozzles, electrodes fabrication will be not performed on the smooth area (in the center of the pattern) because this one is not enough large ($<100\ \mu\text{m}$).

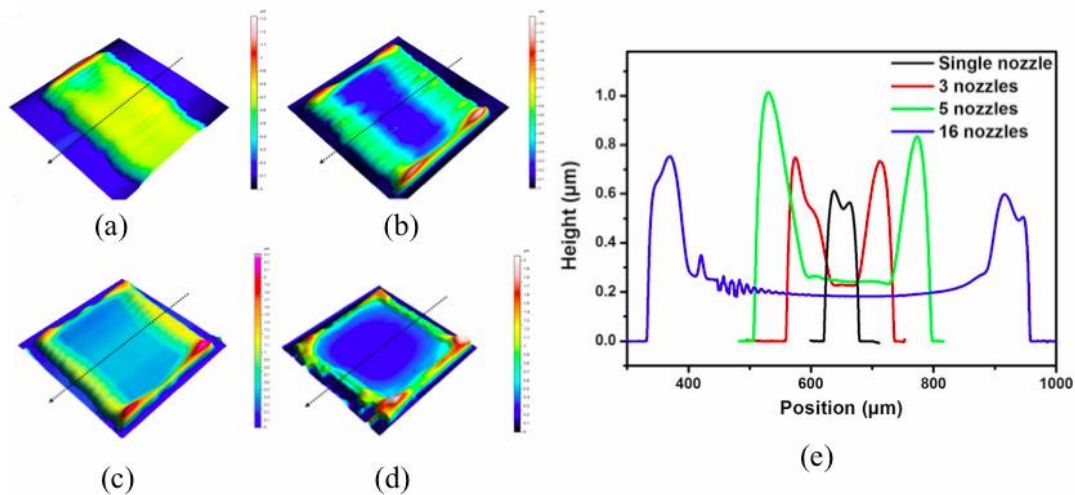


Figure 3-45: Morphological behavior of printed Su8 with (a) one nozzle, (b) three nozzles, (c) five nozzles, and (d) sixteen nozzles. (e) Corresponding two-dimensional profile. 3D pictures and corresponding profiles extracted along the dashed lines of $1000 \times 1000 \mu\text{m}^2$ square-shaped thin films.

Moreover, at fixed overlap, the thickness of insulator in the center of the pattern can't be controlled with number of activated nozzles. Consequently, overlapping effect has also been studied.

➤ **Drop spacing effect (overlap effect)**

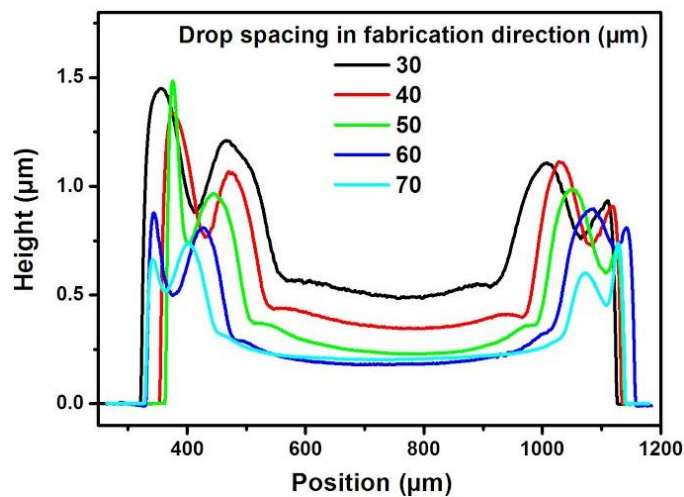


Figure 3-46: Cross-section view of the printed Su8 patterns using sixteen nozzles printing as a function of drop spacing.

Figure 3-46 shows that, at fixed activated nozzles (16), the increase of overlap value leads to increase the insulator thickness. Indeed, as explained previously, the increase of overlap between two droplets (i.e., decrease of drop spacing) leads to increase the amount of material at constant area. However, effect of overlap is less pronounced than for single-nozzle-printing. Indeed, the maximum thickness value (in the center of the pattern) is less than $1\mu\text{m}$. Consequently, another parameter (the capillarity) has been investigated in order to increase insulator thickness.

➤ Capillarity effect

Capillarity is the overlap between two lines printed using multi-nozzles. Such effect can also be used in order to increase the amount of material at constant area and consequently control insulator thickness.

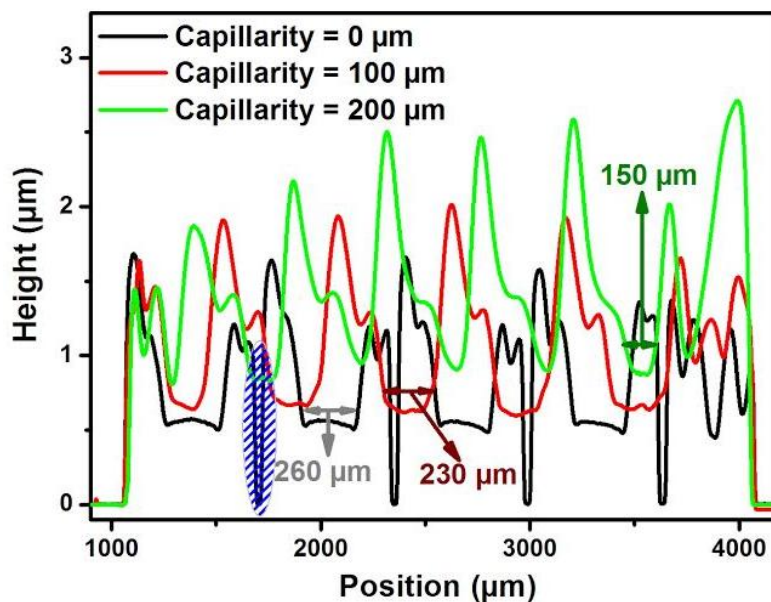


Figure 3-47: Cross-section view of the printed Su8 patterns with sixteen nozzles printing as a function of capillarity, obtained with a profilometry measurement

As show in Figure 3-47 capillarity has a strong impact on insulator thickness but also on its morphology. When capillarity is equal to 0 (no overlapping between each line), lines are not connected (blue hatched area in Figure 3-47) and consequently, the film is not continues. When capillarity increases the mean thickness increase. Moreover, the morphology shows high peaks due to coffee ring effect. However, thickness can be adjusted in order to obtain a value of approximately $1\mu\text{m}$, which will be appropriated in order to fabricate printed OTFT.

In summary, two printing methods (single-nozzle-printing and multi-nozzle-printing) have been investigated in order to obtain insulator thickness, which can be easily controlled. Table 3-6 sums up the optimum printing parameters.

Parameter	Epoxy based a (Su8 2000.5)
Drop spacing	40 μm
Firing voltage	40 V
Maximum jetting frequency	1 KHz
Printing nozzles	Single nozzle or multi-nozzles (16)
Substrate temperature	50°C
Cartridge print height	700 μm
Number of layers	1

Table 3-6: Printing parameters for Su8.

In the following printed OTFT will be fabricated with the two previously described methods in order to determine their impact on electrical behavior. Moreover, the ultimate goal of this work is to achieve fully-printed OTFT, consequently, investigations on printed semiconductor behavior will be described in the next section.

II.1.3 Semiconductor ink

- **Jettability**

All the solvents used in the first part of this work, Toluene ^[57], chlorobenzene ^[58], dichlorobenzene ^[58], and anisole ^[59,60], have ever been inkjet-printed. However, toluene is more difficult to print due to its lower boiling point solvent. Indeed, same conclusions have been obtained: lower boiling point solvents lead to nozzle clogging, unstable printing and non-uniformity of the resulting printed films ^[61]. As Subramanian work (see in Figure 3-14), experiments performed using anisole have shown excellent printing behavior. Moreover, as shown in chapter 2, drop casting Tips-pentacene diluted in anisole leads to very low off-current and gate leakage current. Consequently, semiconductor based (1.5% wt Tips-pentacene in anisole) ink has been jetted. Optimized printing parameters are summed as following: firing voltage and jetting frequency are 40V and 0.5 KHz, respectively. Consequently, morphological study will be performed using anisole as solvent.

- **Morphology**

Semiconductor ink has been inkjet-printed on Su8 surface. Figure 3-48 (a) shows that non-continue film is obtained. A hypothesis can be drawn: there are not enough materials deposited using inkjet printing. Such assertion has been confirmed in Figure 3-48 (b) where semiconductor based ink have been printed on lithographical OTFT. Such effect is a limiting factor of inkjet printing semiconductor based ink.

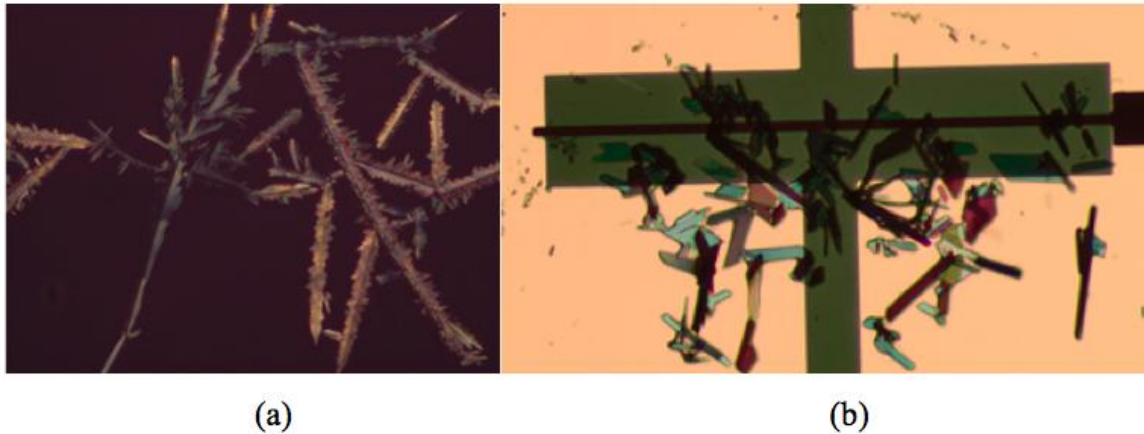


Figure 3-48: a) Semiconductor based ink printed on Su8 chemically modify using UV-ozone treatment; b) Semiconductor based ink printed on OTFT performed using lithography.

In conclusion, inkjet printing semiconductor ink has not shown continues films.

II.2 Printed OTFT

After analyzing, the different possibilities of the deposition of the metallic contacts (Silver), of the gate insulator (Su8) and of the semiconducting active layer by printing technique, we will use these results in the progressive introduction of this technique in the process of OTFTs.

II.2.1 Feasibility of first printing steps (gate contact, gate insulator, source and drain contacts): OTFTs with evaporated semiconductor

Feasibility of first printing steps (gate contact, gate insulator, source and drain contacts) can be better studied if the deposition of the semiconducting active layer is made by reliable technique. Here to avoid any interference between these first printing step and the

deposition technique of the semiconducting layer, the semiconducting active layer is constituted by thermally evaporated C_{60} layer (see fabrication process in Figure 3-49). Indeed, evaporation method gives more reliable results.

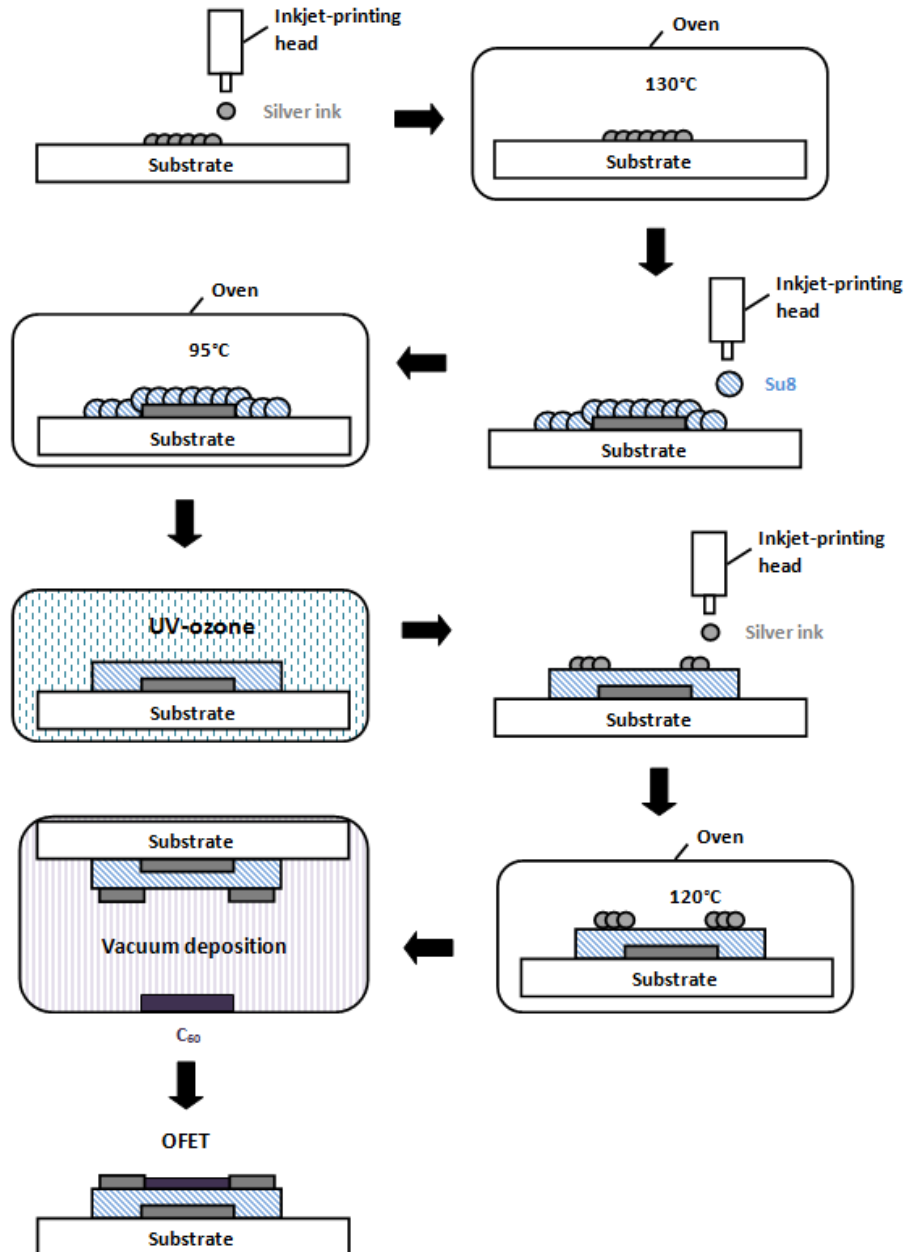


Figure 3-49: Scheme of evaporated semiconductor on inkjet printed OTFT.

Su8 layer is deposited using single-nozzle-printing and multi-nozzle-printing methods. This will lead to investigate in the same time the effect of insulator morphology on OTFT electrical behavior.

Optical pictures, in Figure 3-50, shows printed OTFT using single-nozzle (Figure 3-50 (a)) and multi-nozzles (Figure 3-50 (d)). Inkjet printing parameters (overlap, jetting frequency for each layer...) are those defined in last section.

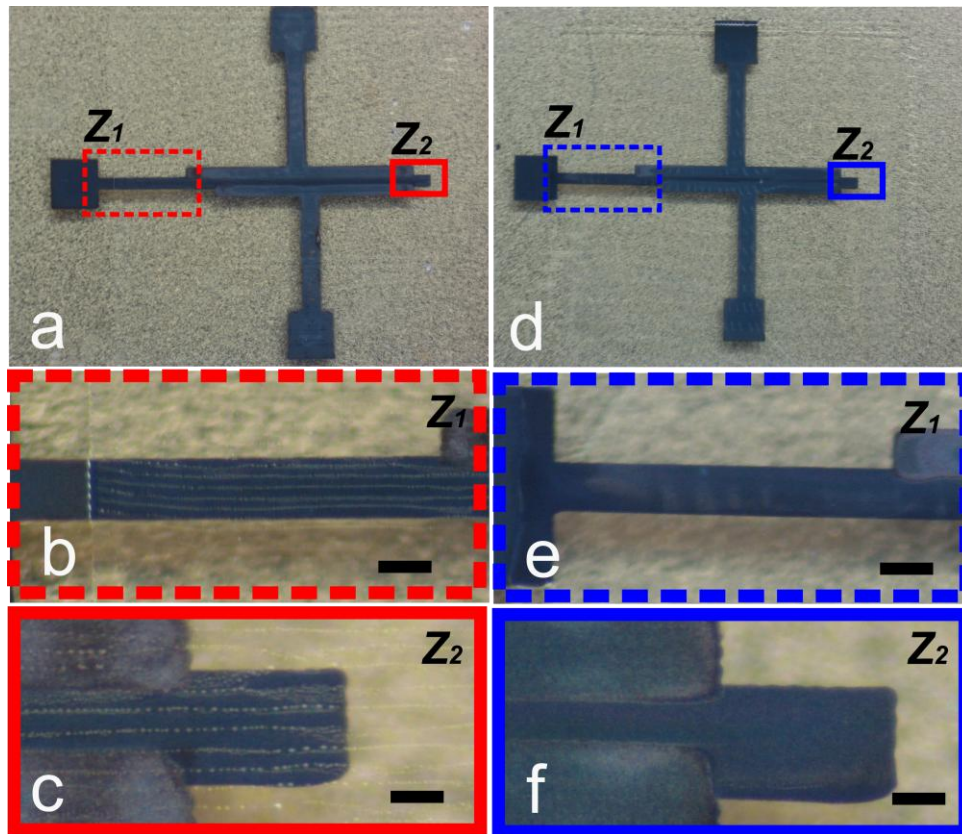


Figure 3-50: OTFT optical observations as a function of insulator morphology: (a) OTFT fabricated using single-nozzle-printing method; (b) Zoom on the edge of insulator corresponding to the device described in (a); (c) Zoom on the channel corresponding to the device described in (a); (d) OTFT fabricated using multi-nozzle-printing method; (e) Zoom on the edge of insulator corresponding to the device described in (d); (f) Zoom on the channel corresponding to the device described in (d).

For both printing methods, even if insulator cross sectional profile is wavy, printed OTFT is performed with accuracy allowing the minimum resolution between source and drain about $60\ \mu\text{m}$. Different insulator thickness have been used for both morphologies. The transfer characteristics of OTFT with those two morphologies are shown in Figure 3-51 and Figure 3-52. Table 3-7 and Table 3-8 show electrical characteristic for OTFT fabricated using insulator printed single-nozzle and multi-nozzle techniques respectively.

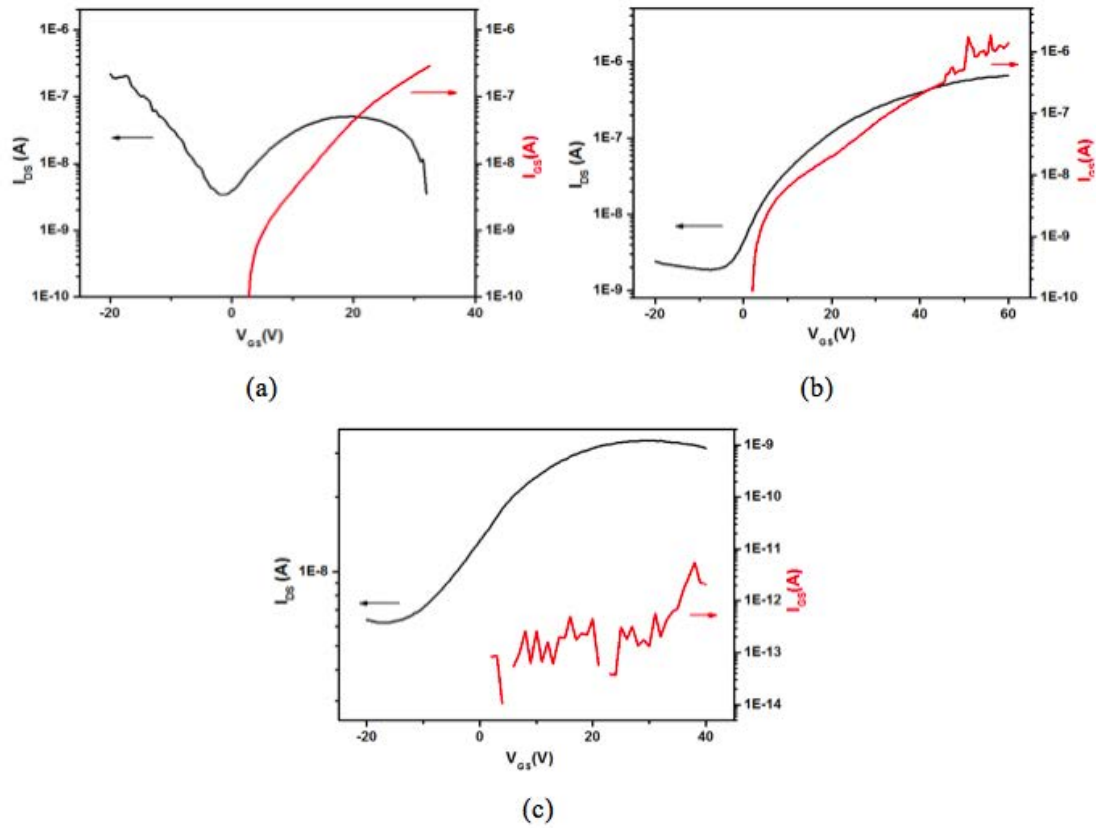


Figure 3-51: 35nm thick C_{60} thermally evaporated on OTFT printed using single-nozzle-printing method; insulator thickness equal: (a) 500 nm; (b) 1.3 μm ; (c) 2 μm . $V_{DS} = 20$ V.

μ (cm^2/Vs)	V_{TH} (V)	SS (V/dec)	I_{on}/I_{off}
0.0072	14.81	10.09	10^2

Table 3-7: Electrical characteristics of OTFT printed using single-nozzle and insulator thickness equal 1.3 μm .

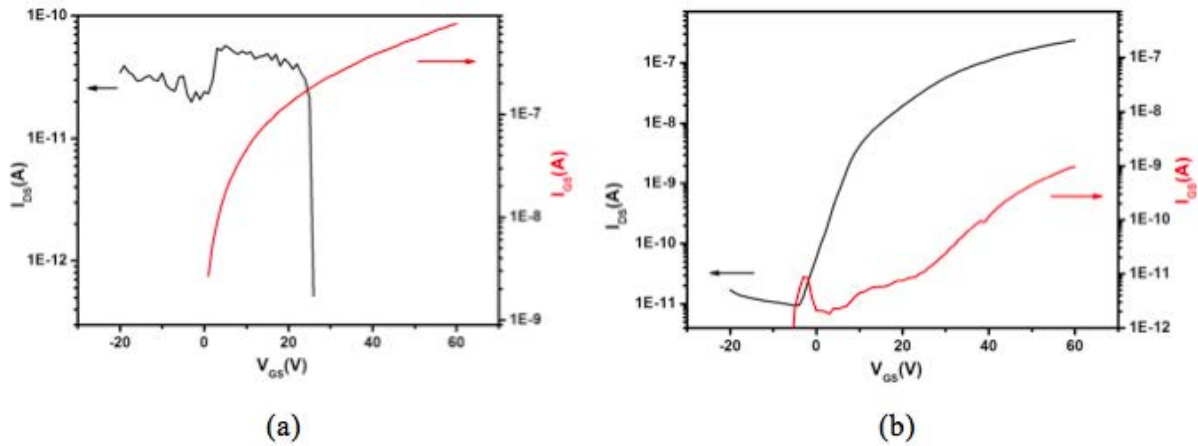


Figure 3-52: 35nm thick C_{60} thermally evaporated on OTFT printed using multi-nozzle-printing method; Insulator thickness equal: (a) 700 nm, (b) 1 μm . $V_{DS} = 10V$.

μ (cm^2/Vs)	V_{TH} (V)	SS (V/dec)	I_{on}/I_{off}
0.0059	21.76	4.72	10^4

Table 3-8: Electrical characteristics of OTFT printed using multi-nozzle and insulator thickness equal 1 μm .

As expected, OTFT electrical behavior is strongly dependent on the insulator thickness whatever the use of single-nozzle-printing or multi-nozzle-printing. When Su8 thickness is too low, the leakage current I_{GS} increases drastically and consequently I_{DS} modulation can't be obtained (Figure 3-51 (a) and 3-52 (a)). Opposite behavior is observed when Su8 is too thick. In this case I_{GS} is low with more or less important modulation of the drain current. Using single-nozzle-printed insulator, less than one decade of drain current modulation is observed with 2 μm thick Su8 insulator.

Using multi-nozzle-printed insulator, the gate leakage current is much lower than the drain current and the drain current is modulated by more than 4 decades with 1 μm thick Su8 (Figure 3-52 (b)). The electrical characteristics of this OTFT are summarized in Table 3-8.

In conclusion, OTFTs fabricated with nearly all-printing steps (except the last semiconductor deposition step) can work with acceptable characteristics. However, it is important to use thick Su8 insulator layer (around 1 μm) and to deposit it multi-nozzle-printing in order to obtain low gate leakage current.

The last step in the way of fully printed OTFT is to check the deposition of the last semiconducting active layer. As inkjet printed Tips-pentacene doesn't form a continuous layer (see II.1.3), this step is challenging, and will be discussed in the following.

II.2.2 Feasibility of solution deposited OTFTs: Printed gate contact, gate insulator, source and drain contacts, Drop-casted Tips-pentacene

Facing to the difficulty to deposit continuous films of Tips-pentacene by inkjet printing, an intermediary step will be described in the next subsection. Indeed, Tips-pentacene has been drop casted on optimized printed structures as defined in the pervious subsection. This prerequisite step will highlight the problem leading to non-continuous semiconductor film deposition.

II.2.2.1 Solution deposited OTFTs with drop-casted Tips pentacene ink

As shown in Figure 3-53, Tips-pentacene has been drop casted on printed structures (source and drain electrodes printed on printed Su8). Such experiments have been performed for Tips-pentacene diluted in 3 solvents (anisole, chlorobenzene and toluene). Figure 3-53 shows the semiconductor drying behavior as a function of time. Importantly, same behavior is observed independently of solvent and after semiconductor completely drying no uniform film can be obtained. The phenomena can be explained as following:

Semiconductor was dried on top of two different materials (Su8 for the gate insulator and Silver for the drain and source contacts). Su8 is more hydrophobic than silver. Consequently, semiconductor is firmly pinned on silver during drying step. At the end of drying step, the liquid splits in two parts and remains on each silver electrodes without depositing semiconductor crystals between electrodes.

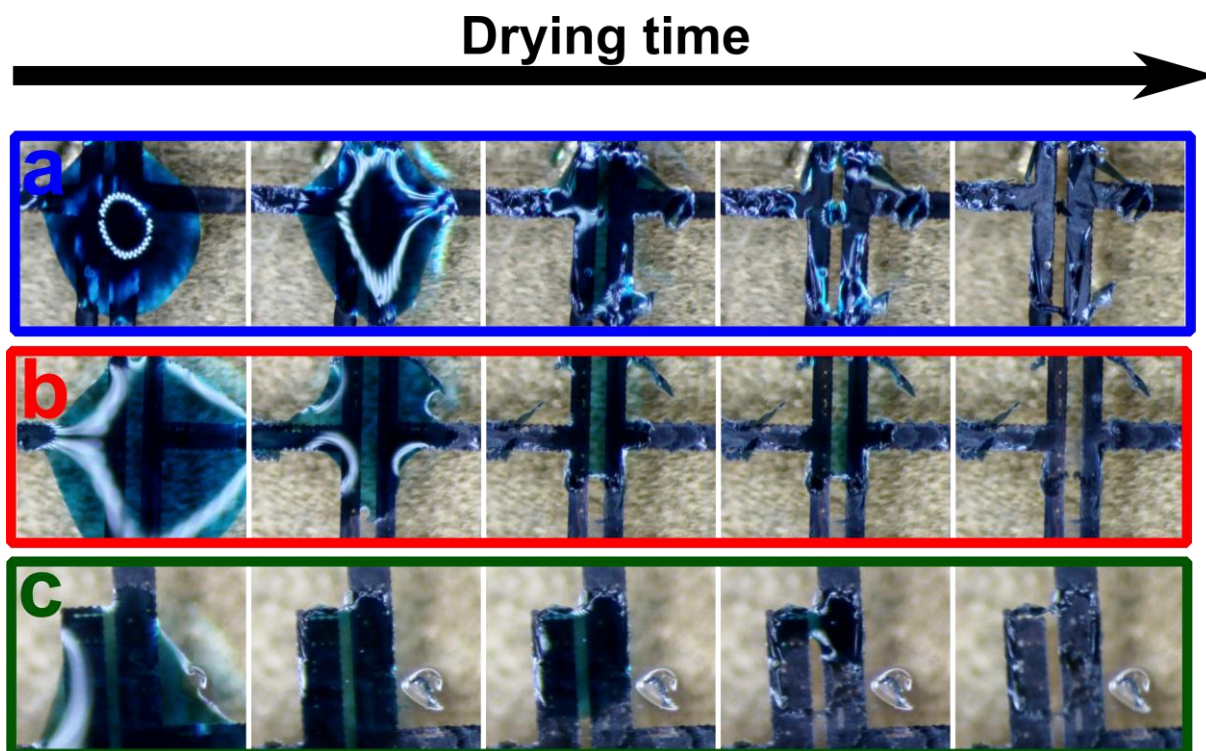


Figure 3-53: Optical picture showing drop casted semiconductor (i.e. on printed source/drain electrodes and printed insulator) drying behavior as a function of time. a) TIPS-pentacene in anisole; b) TIPS-pentacene in chlorobenzene; c) TIPS-pentacene in toluene.

In conclusion, because of this drying behavior, it is not possible to obtain continuous layer of TIPS-pentacene between source and drain, forming a semiconducting active layer of transistor. OTFTs using drop-casted TIPS-pentacene diluted in any solvent cannot work. Consequently, in the following, an original strategy will be presented in order to overcome this drawback.

II.2.2.2 Solution deposited OTFTs with drop-casted polymer based TIPS pentacene (blend semiconductor) ink

It has been reported^[62] that organic semiconductor blends with polymer can be used as active layer in solution processed OTFTs. Moreover, such active layer can improve the semiconductor morphology in terms of more uniform coverage across the device^[63].

Facing to the dewetting problem of TIPS-pentacene diluted in pure solvent, a new concept, which rely on the use of solution deposited TIPS-pentacene blended with Su8 as active layer, has been studied. Indeed, adding Su8 small molecule will help to pin the contact line of the droplet independently of the hydrophobicity of the under layer, and particularly on Su8 gate insulator.

- **Proof of concept**

Polymer blends have been extensively studied over the last few decades because their additional properties cannot be achieved with a single component [64-66]. In particular, blends of semiconducting and insulating materials have attracted increasing interest because they possess both the optical and electrical properties of conjugated molecules and the characteristics of insulating polymers.

James *et al* [63] reported the effect of blending Tips-pentacene with insulating polymer (polystyrene (PS)). They proved that the addition of an insulating polymer does not disrupt the π - π stacking of the Tips-pentacene molecules; instead, the blending improves the Tips-pentacene morphology in terms of more uniform coverage across the device and less variation in pentacene backbone in-plane orientation. The OTFT performance improved, including field-effect mobility, threshold voltage and subthreshold slope, which indicated an improved interface between the Tips-pentacene and channel dielectrics.

This result can be used in this work, with the main idea to avoid the dewetting effect by using Tips-pentacene blended in Su8, deposited on Su8 gate insulator. Adding Su8 molecule will help to pin the contact line of the droplet independently of the hydrophobicity of the under layer. This concept never described until now has been validated as shown in Figure 3-54. Blended Tips-pentacene have been drop-casted on a structure composed by printed Su8 layer and printed silver drain and source electrodes.

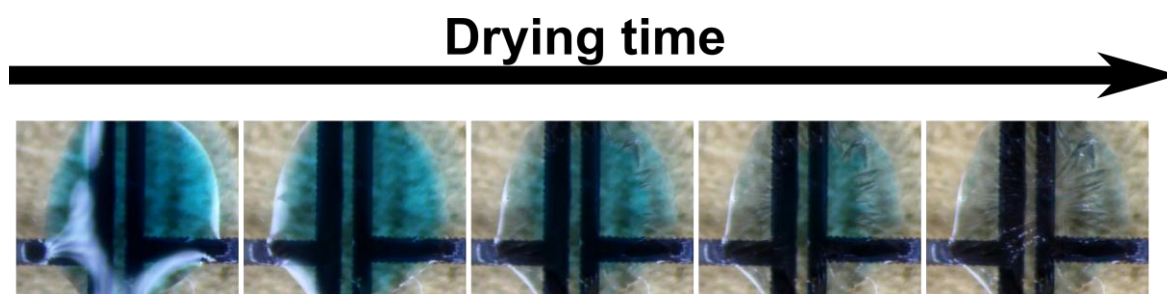


Figure 3-54: Optical picture showing drop casted of blended semiconductor (i.e., on printed source/drain electrodes and printed insulator) drying behavior as a function of time. Blended semiconductor is composed of Su8 2000.5 and Tips-pentacene diluted in anisole.

Compare to pure solvent based ink, the polymer based ink doesn't show dewetting behavior. The droplet contact line is pinned immediately after the deposition regardless of the under layer material is hydrophobic (Su8) or hydrophilic (silver).

- ***OTFTs with drop-casted blended Tips pentacene on printed gate-insulator-drain/source electrodes***

The deposition of continuous drop casted blended Tips-pentacene on printed Su8 and between printed silver source and drain have been performed. Consequently, fully solution processed OTFT have been fabricated. Figure 3-55 shows the transfer characteristics in linear plot of such OTFT. Unfortunately, OTFT electrical behavior is very poor. In particularly because of very low current and very high threshold voltage (more than 20V). An hypothesis can be drawn: blended Tips-pentacene forms a poor electrical contact with printed silver, leading to a low injection of electrical charges inside the channel.

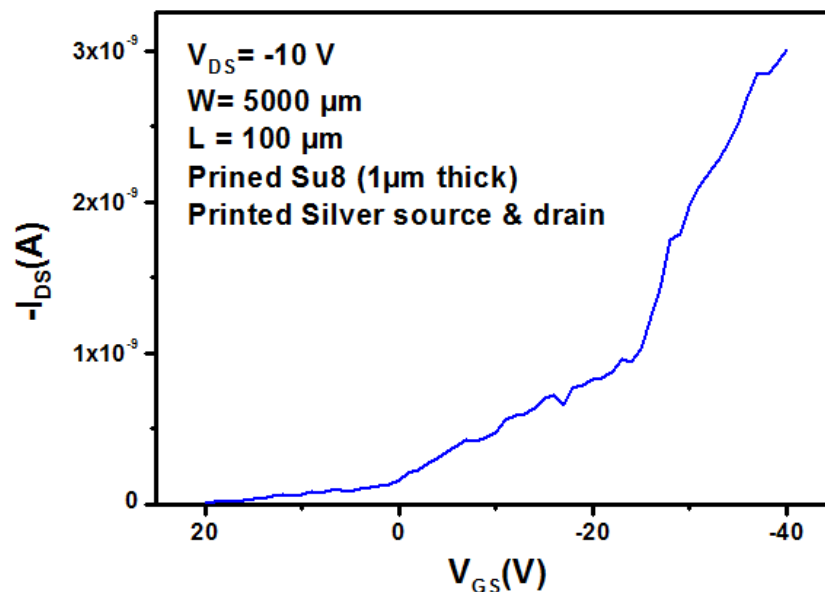


Figure 3-55: Transfer characteristics in linear plot of OTFTs with printed gate electrode, printed Su8 insulator, printed silver drain and source contacts and drop-casted blended Tips-pentacene as active layer.

- ***OTFTs with drop-casted blended Tips-pentacene on printed gate and insulator and evaporated gold drain/source electrodes***

Expecting solving soon the problem of the electrical contact between printed silver electrode and blended Tips-pentacene, evaporated gold drain/source electrodes were used to

check the electrical behavior of OTFTs using drop casted Su8 blended Tips-pentacene on printed Su8 as active layer.

Drop casted Tips-pentacene blended with Su8, as shown in Figure 3-56 (a), exhibits big and uniform crystals. Figure 3-56 (b) shows the transfer characteristics of drop casted Tips-pentacene blended with Su8 as a function of blending ratio (blending ratio is defined as the volume of Tips pentacene on the volume of Su8).

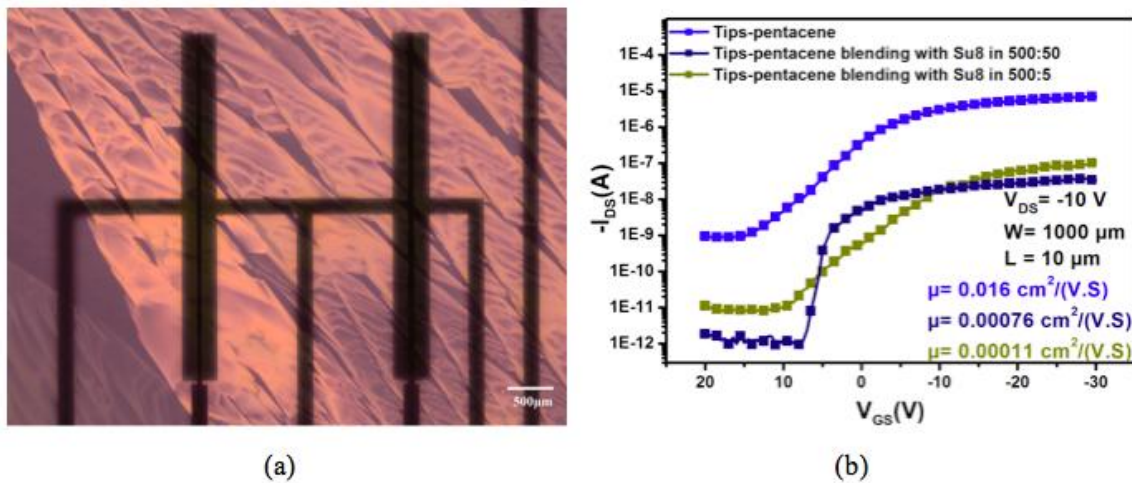


Figure 3-56: (a) Optical picture of drop casted Tips-pentacene blended with Su8 on lithographical structure; (b) Transfer characteristics of Tips-pentacene blended with Su8 as a function of blending ratio.

Moreover, the electrical characteristics have been summarized in Table 3-9.

Tips-pentacene blended with Su8	μ (cm^2/Vs)	V_{TH} (V)	SS (V/dec)	I_{on}/I_{off}
Un-blended Tips-pentacene	0.1	-0.12	4.2	10^4
Tips 500/5 Su8	0.002	-7	4.3	10^4
Tips 500/50 Su8	0.0005	+4	0.9	10^4
Tips 500/100 Su8	--	--	--	--

Table 3-9: Summary of electrical characteristics of drop casted Tips-pentacene blended with Su8 OTFTs as a function of blending ratio.

As shown in Table 3-9 and Figure 3-56, working OTFT can be achieved using organic semiconductor blended with Su8. Note that, electrical behavior is strongly dependent of blending ratio. As expected, more Su8 leads to decrease the conductivity of active layer.

Consequently, the field effect mobility decreases when more Su8 amount is mixed with Tips-pentacene. The best transfer characteristics is obtained with 500/50 blending ratio even if the on-current and then the mobility is lower. Indeed, at this blending ratio value, the subthreshold slope is highly improved, reaching 0.9.

This preliminary study has validated the possibility to fabricate working OTFT using polymer blend organic semiconductor. More works have to be done in order to optimize the blending ratio value. However, this new concept, never reported until now, can be an efficient solution allowing the fabrication of fully solution OTFT.

In the following, a deeper investigation focusing on printing blend semiconductor is presented. Indeed, fully-printed OTFT is the final purpose of this study.

II.2.2.3 Solution deposited OTFTs with printed polymer based Tips-pentacene (blend semiconductor) ink

- ***Film formation***

Tips-pentacene blended with Su8 has been printed on Su8. Note that, overlap between droplets had been kept constant. Square-shaped patterns with various geometries have been performed (see in Figure 3-57 (a)). Figure 3-57 (b) shows optical polarized pictures of printed semiconductor film using: large height/small length and small height/large length. In both cases, semiconductor films don't cover all the printed patterns. However, small length seems to be more efficient in order to obtain more uniform films morphology.

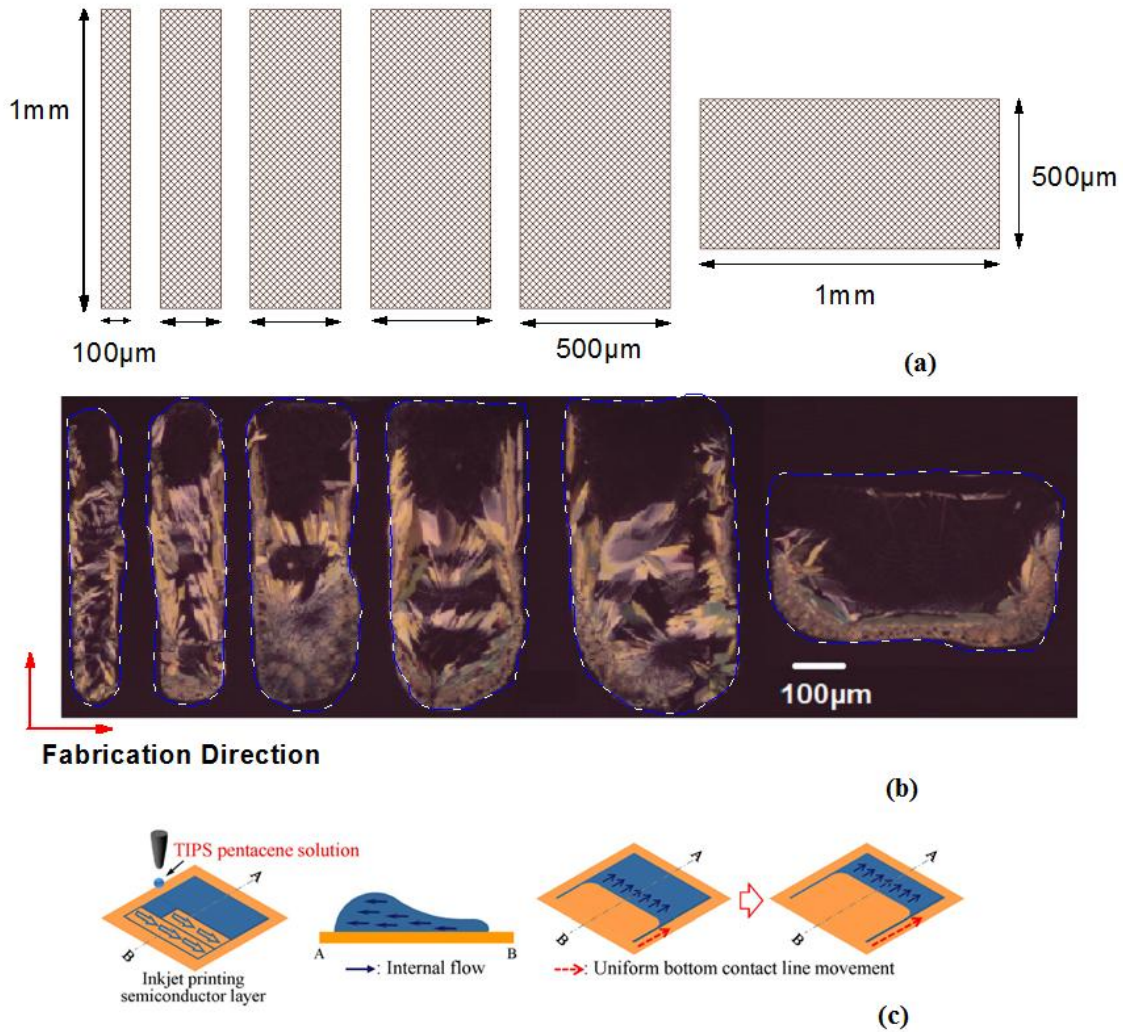


Figure 3-57: (a) Design of inkjet printed patterns: the first five patterns have fixed height (1mm) and various lengths (100μm, 200μm, 300μm, 400μm and 500μm). The last pattern has height of 500μm and length of 1mm. (b) Inkjet-printed Tips-pentacene blended with Su8 in function of patterns design corresponding to design (a); (c) Schematic of the evaporation behavior of drying semiconductor layer inkjet-printed^[67].

Such effect has ever been reported in literature^[67] and can be explained as follows: when a solution is printed (for instance, from A to B in Figure 3-57 (c)) internal flow is orientated toward the beginning of the printing sequence. At pinned contact line, it exists an evaporation rate gradient during the drying process. Indeed, outward convective flow is generated to replenish the evaporation loss at the pinned contact line. Such flow is orientated from the end of the pattern to the pinned contact line and consequently, Tips-pentacene and Su8 molecules are transported to the pattern periphery. That's why most of the semiconductor crystals are orientated towards the pinned contact line (i.e., pattern periphery).

Moreover, as shown in Figure 3-57 (b), at the end of the printing sequence, a vacant region in the semiconductor layer is observed (dark area in the Figure 3-57 (b)). This phenomena can be attributed to the receding of the contact line which remains unpinned due to the replenish flow (Figure 3-57 (c)). This phenomenon is exacerbated when the pattern becomes large (Figure 3-57 (b)).

- ***OTFTs with printed Su8 blended Tips-pentacene as active layer, spin coated Su8 as gate insulator and evaporated gold source/drain electrodes***

As seen in this previous study of the film formation, narrow pattern is favorable for filling the space between source and drain leading to uniform active layer of OTFTs. Semiconductor pattern size (3 mm×400 μm) has been designed. As shown in Figure 3-58 (a), the vacant region is outside the active area of OTFT.

Figure 3-58 (b) shows the transfer characteristics of OTFTs with inkjet printed Tips-pentacene blended with Su8, spin coated Su8 gate insulator and evaporated gold drain/source electrodes. Table 3-10 summarizes the electrical parameters of these OTFTs.

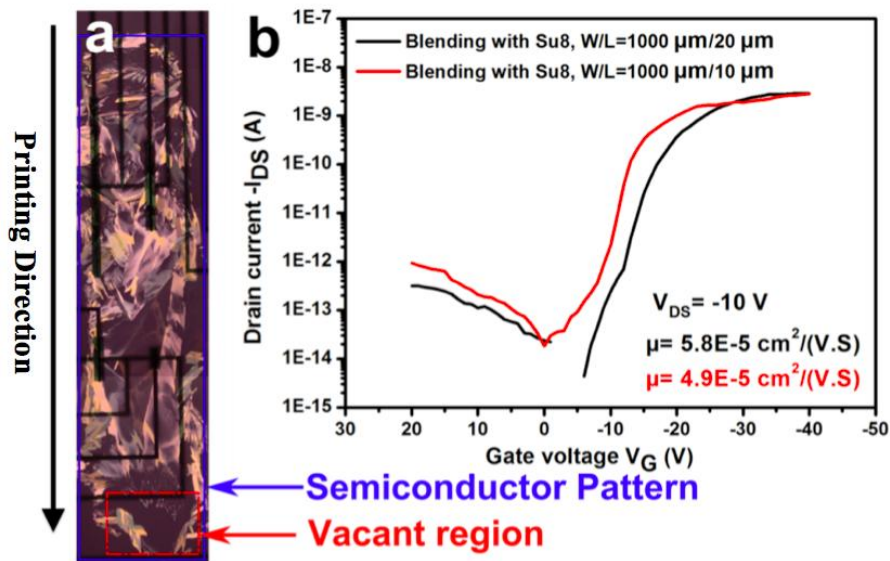


Figure 3-58: OTFTs with Inkjet printed Tips-pentacene blended with Su8 as gate insulator, spin coated Su8 as gate insulator and evaporated gold source/drain contacts. (a) Optical picture, (b) Transfer characteristics.

L/W ($\mu\text{m}/\mu\text{m}$)	Insulator thickness (nm)	μ (cm^2/Vs)	V_{TH} (V)	SS (V/decade)	$I_{\text{on}}/I_{\text{off}}$	V_{DS} (V)
20/1000	400	5×10^{-5}	-19.3	1.85	10^5	-10
10/1000	400	5×10^{-5}	-13.3	2.1	10^5	-10

Table 3-10: Inkjet printed OTFT geometrical and electrical parameters. μ , V_{TH} , Subthreshold Slope, $I_{\text{on}}/I_{\text{off}}$ ratio are extracted from transfer characteristics.

The mobility value, $5 \times 10^{-5} \text{ cm}^2/\text{V}\cdot\text{s}$ is about 10 times smaller than that previously fabricated by drop casting.

- **Fully printed OTFTs: printed Su8 blended Tips-pentacene as active layer, printed Su8 as gate insulator and printed silver source/drain electrodes**

Finally, fully-inkjet-printed OTFTs using Tips-pentacene blended with Su8 as semiconductor have been fabricated. Semiconductor pattern size ($3 \text{ mm} \times 400 \mu\text{m}$) has been designed. As shown in Figure 3-59, the vacant region is outside the active area of OTFT.

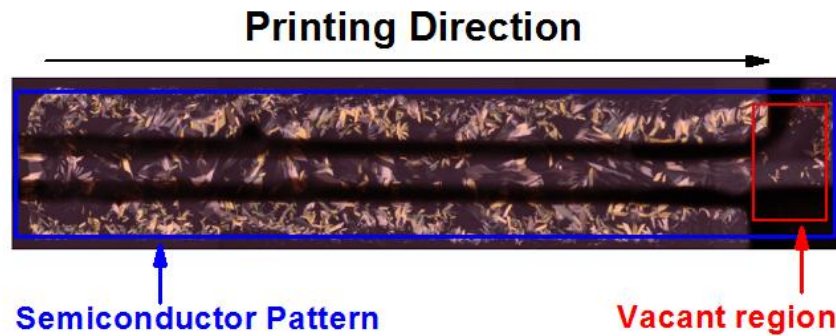


Figure 3-59: Polarized optical picture of fully inkjet printed OTFT

Unfortunately, the OTFT characteristics are so bad (transfer characteristic in Figure 3-60, with very low and not enough modulated current, high threshold voltage), maybe due to the fact that there are not enough crystals cross the channel as shown in Figure 3-59. One approach to overcoming this drawback is to increase the quantity of semiconductor. Consequently, in future it needs more deeply study in order to realize fully-printed OTFT.

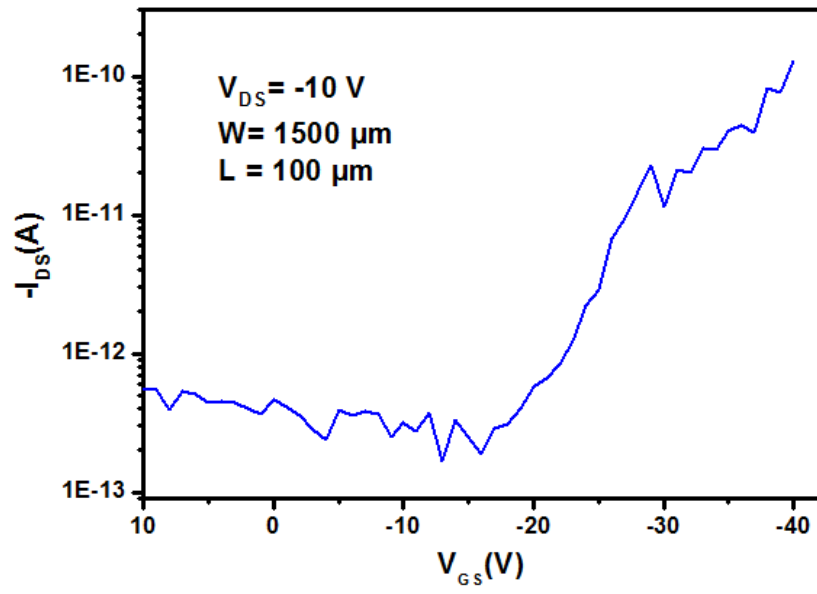


Figure 3-60: Transfer characteristics of fully printed OTFTs.

Conclusion

This chapter was devoted to the study of the parameters leading to the fabrication of fully-printed OTFTs. Fully printed means that all the layers constituting the OTFTs have to be deposited by printing.

In the first part, materials processing (silver, Su8 and semiconductor ink) has been deeply studied. The jettability, the wettability, the printability, and patterns optimization of each ink have been studied in order to achieve well-defined patterns. The deposition parameters of silver and Su8 are well optimized leading to uniform and well-defined patterns. However, many problems occurred during the printing of semiconducting film, Tips-pentacene here. It was not possible to deposit uniform layer.

Facing to this difficulty, the optimization of the deposition parameters of Su8 and silver led to check their use in transistor by fabricating OTFTs with thermally evaporated C₆₀ film as semiconducting active layer. OTFTs work with acceptable characteristics. However, Su8 gate insulator has to be thick (~1 μm) and printed by multi-nozzle method.

Supplementary advance was obtained by checking the possibility of fully solution deposited OTFTs. Indeed, as Tips-pentacene cannot be printed to form continuous film, one intermediary step in the way towards fully printed OTFTs was to check the feasibility of fully solution deposited OTFTs. For example, Tips-pentacene has been drop casted and not printed.

However, due to the difference between hydrophobic Su8 and hydrophilic silver, the deposition of Tips-pentacene did not lead to continuous film between source and drain.

One original idea was to blend Tips-pentacene with Su8. Indeed, Su8 molecule inside Tips-pentacene can help to pin the contact line of the droplet. After verifying this original hypothesis, OTFTs with drop-casted film containing medium content of Su8 inside Tips-pentacene showed interesting parameters. Blended Tips-pentacene with Su8 can act as semiconducting active layer for solution deposited OTFTs.

The following step was to deposit this blended Tips-pentacene by printing and not by drop-casting. Printing blended Tips pentacene was not easy, probably due to the low volume of droplet. The Tips-pentacene film does not fill the entire space between source and drain. Only narrow form of the active layer led to full filling of the space. The characteristics of OTFTs with this high aspect ratio showed interesting behavior, demonstrating the possibility to fabricate OTFTs with nearly all printed layers. Only drain and source electrodes were gold evaporated.

The final step was to check if fully printed, with silver printed source/drain electrodes, OTFTs can work. Unfortunately, transistor characteristics were very bad. This result shows that the problem between silver surface and Su8 surface was not totally solved. Moreover, it seems that the contact between silver and blended Tips-pentacene is not so injecting. A lot of works have been done, reducing more the difference between silver and SU8 or using other printed metal than silver. Some solutions will be proposed at the end of this document.

Finally, what we can conclude from this long chapter is the demonstrated possibility to get fully printed OTFT thanks to old ideas and original one proposed here.

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**Chapter 4: Can surface modification improve
the characteristics of solution-processed OTFTs?
Example of functionalization with 1-
aminoanthraquinone**

I. Introduction of surface modification of OTFTs

OTFT is a complex system comprising of the semiconductor, electrode, and the dielectric. The ultimate performance of OTFT is not only determined by the properties of the individual component, but also affected by the different interfaces, especially the semiconductor-insulator interface. Most recent work in OTFTs has focused on the improvement of this interface through the functionalization of the surface of the first deposited layer: semiconducting active layer for top-gate OTFTs or gate insulator for bottom gate OTFTs. The bottom gate structure used in this work, led us to study a possible functionalization of the surface of SU8 layer before depositing the active layer. For this work, the simple drop-casting technique for the deposition of the active layer is used only to determine the efficiency of the functionalization. Following the results of chapter 2, Tips-pentacene was used as it led to more reliable process than when using C₆₀.

I.1 Main factors at the semiconductor-insulator interface

The charge carrier transport in OTFT is extremely restricted by the first few semiconductor monolayers next to the semiconductor-insulator interface ^[1,2]. Thus, the interface states are especially important for improving the performance of OTFTs. For these reasons, particular attention is focused on the semiconductor-insulator interface to search for the nature at this narrow region for improving performance of OTFTs ^[3,4].

The insulator surface roughness, surface energy, surface polarity and dielectric constant are considered as four important parameters at the semiconductor-insulator interface, as shown in Figure 4-1, and have been discussed widely ^[5,6]. The interfacial effect in transistor is really complicated, because it usually exhibits a composition result of several individual interfacial factors. In this section, four parameters will be discussed in detail.

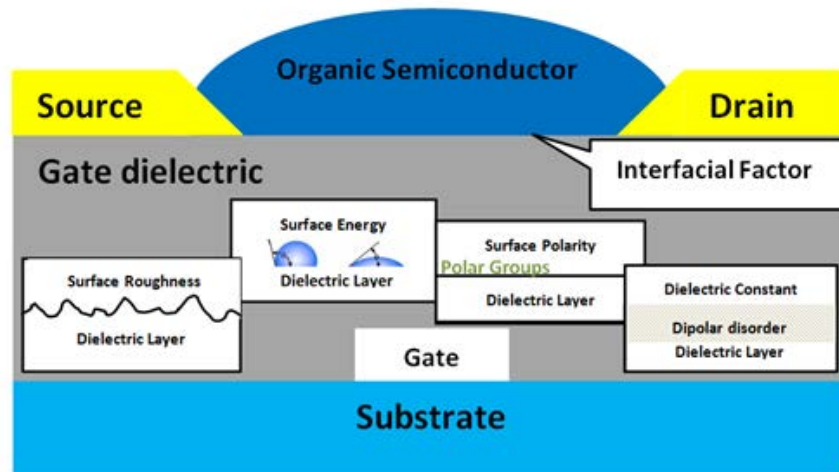


Figure 4-1: Four interfacial factors considered having large impact on the performances of OTFTs ^[7].

I.1.1 Surface roughness of dielectrics

Insulator roughness is often reported as a key parameter that strongly impact OTFT electrical behavior. Although fabricating a top-gate OTFT structure, or using very smooth material (air or vacuum) as gate dielectric can weak or eliminate the effect of dielectric roughness at semiconductor-insulator interface ^[4,8,9], a smooth dielectric surface is still extremely important to a bottom-gate OTFTs. The roughness of the insulator acts as “hills” and “valleys” for charge transportation in OTFTs as shown in Figure 4-2. In a working OTFT, the charge carriers are extremely limited close to the semiconductor-insulator interface under direct gate voltage, and charge carriers just move along the dielectric surface under source-drain voltage. If the dielectric surface is rough, more energy is needed to cross these “hills” and “valleys” for charge carriers. These “hills” and “valleys” act as charge trappers and transport hampers ^[5,10].

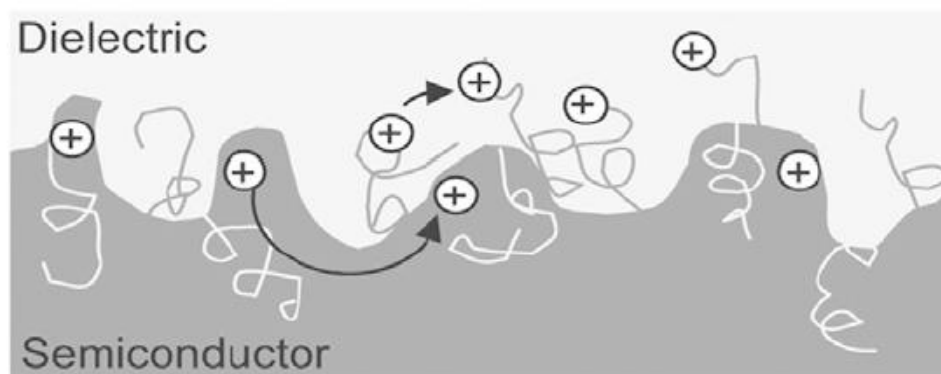


Figure 4-2: Schematic diagram of the interface structure at dielectric-semiconductor interface [10]

Stuedel *et al* have investigated the effect of dielectric roughness on pentacene TFTs [11]. Various roughness of dielectrics surface have been fabricated, and it was found that mobility decreased from 1.0 to 0.02 cm²/Vs as the root-mean-square (RMS) roughness of dielectric surface increased from 0.17 to 9.2 nm. Besides, another work by Chua *et al* found a critical roughness threshold in solution-processed OTFTs [12]. When the roughness was less than the threshold, mobility was constant; when the roughness exceeded the threshold, the mobility decreased significantly. Indeed surface with sharp peaks (high RMS) enhance trapping sites and unfortunately lead to increased trap density.

Besides those effects of RMS roughness on charge transport in OTFTs, other researchers [13] have reported the impact of lateral length scales of dielectric roughness on pentacene OTFTs. More recently other works [14] have proved that for the same RMS value, “bumpy” surfaces reduced charge trapping comparing to those with sharp profile. The RMS roughness is the square root of the averaged sum of height deviations taken from the mean data plane, describing vertical variation on the rough surface. The impact of lateral variations in a rough surface on the film morphology and device performance was also studied. Lin *et al* have investigated the growth of pentacene and OTFT performances as a function of the dielectric surface roughness [14]. Surfaces with shorter correlation lengths showed a more pronounced effect on the charge transport properties of pentacene when compared with the surfaces with long wavelength features.

From these current works, surface roughness including RMS and lateral length scale is a particularly important factor that affects the electrical performance of OTFTs. An increase of

dielectric surface roughness was found to drastically decrease the electrical performance of OTFTs.

I.1.2 Surface energy of the dielectrics

Many researchers have proved performance of solution deposited OTFTs highly affected by the surface energy of dielectric layers [1]. Surface energy of dielectrics could be evaluated by measuring the contact angle of two test liquids; one is polar and another is nonpolar. Several formulas have been reported to calculate the surface energy [15-17].

Yang *et al* have found the grain size of pentacene increased with the increase of dielectric surface energy by fabricating pentacene transistors using surface energy controllable dielectrics [18]. Mobility decreased on high surface energy dielectric due to void obtained in the initial layer of pentacene.

Umeda *et al* have studied the effects of dielectric surface energy on solution-processed OTFTs, and found that mobility increased from 0.4 to 1 cm²/Vs with the surface energy of dielectric decreasing from 35 to 13 mN m⁻¹ [19]. Nayak *et al* [20] and Miskiewicz *et al* [21] also have the similar conclusions.

From those works mentioned above, the relation between surface energy of dielectric and performance of OTFTs could be concluded as below: low surface energy dielectrics can enhance the performance of OTFTs; high surface energy has negative impact on mobility. Indeed, limited charge transport in organic semiconductor is probably due to voids at the interface between organic semiconductor and high surface energy gate insulator.

I.1.3 Surface polarity of dielectrics

The surface polarity of the dielectric surface is based on the ratio of polar component to the total surface energy. The surface polar components are attributed to polar groups on the gate dielectric. If the end groups at the interface are electron-withdrawing groups in n-type OTFTs, electrons transport from semiconductor film will be attracted by the additional holes supplied by those groups. A more positive gate bias is needed to switch off the devices [22]. On the contrary, electron-donating end groups in p-type result in more negative gate bias shift.

Pernstich *et al* [23], Takeya *et al* [24] and Volkel *et al* [25] have estimated the effects of the interfacial polar groups on performances of OTFTs. Researchers found the polar groups on the dielectric layer induced shift of V_{TH} . The polar groups modified the surface potential have the same effect as an applied gate bias, and created more additional trap sites.

The effect of surface polarity of dielectrics can be used to improve the performance of OTFTs. Jang *et al* ^[26] have reported a much higher mobility has been obtained on the insulators with electron-withdrawing groups of pentacene TFTs.

OTFTs with polymer dielectric have the similar conclusions. Park *et al* ^[27] have fabricated three different polymer dielectrics with various surface polarity of pentacene TFTs, obtained that higher polar surfaces afford lower mobility and more negative shift of V_{TH} .

From those works mentioned above, polar groups on the dielectric surface act as charge trappers in OTFTs. The mobility and stability of OTFTs are strongly influenced by those polar groups.

I.1.4 Dielectric constant

The dielectric constant is considered as character of insulators to estimate the dielectric property in OTFTs. A high dielectric constant insulator is usually used to reduce the driving voltage of OTFTs. Recently, many researchers have found that OTFTs with high dielectric constant and low dielectric constant exhibit different performances.

Veres *et al* ^[28] suggested relation between dielectric constant and performance of OTFTs is due to the dipolar disorder in the insulator.

Zhao *et al* ^[29] have investigated the dipolar disorder existed in common polymer dielectrics with dielectric constant larger than 3 leading to an enhanced polaron localization at the interface.

From those works mentioned above, dielectric constant has an important effect on performances of OTFTs.

II. Experimental process of Su8 surface modification with 1-aminoanthraquinone

II.1 Materials

Su8 2000.5 was purchase from MicroChem. Gold and Aluminum were purchased from Neyco. Toluene, 1-aminoanthraquinone, sulfuric acid, sodium nitride, hypophosphorous acid and Tips-pentacene were purchased from Sigma Aldrich Chemical.

Diazonium salt was used for grafting on a surface in the presence of a redactor (hypophosphorous acid). ^[30,31] It has been reported that the performance of FETs with the

dielectric modified with diazonium salt has improved significantly ^[32]. 1-aminoanthraquinone (molecule as shown in Figure 4-3 (b)) was used as precursor of the diazonium salt to modify the insulator surface due to the presence of condensed benzene rings in its structure. Besides, its grafting process is compatible with OTFT fabrication process.

II.2 OTFT fabrication and 1-aminoanthraquinone grafting process

Bottom-gate and bottom-contact geometry was used to fabricate OTFT as described in Figure 4-3(a). The fabrication process of p-type OTFTs is listed as follows: Corning glass was used as substrate. The glass substrate was ultrasonically cleaned in acetone and alcohol baths during 10 minutes, respectively. Aluminum was deposited on glass wafers with a thickness of 150 nm by thermal evaporation, and patterned by wet etching. Su8 2000.5 was spin-coated on glass wafers with a thickness of 400 nm. Aluminum and Su8 were used as the gate contact and insulator, respectively. Then gold was thermally evaporated on the above structure with a thickness of 50 nm, used as source and drain electrodes, and patterned by wet etching. The process is usual till this step. The next step is the chemical modification of Su8 surface.

The substrate was immersed into chemical solution for the grafting, according to the process mentioned described in Figure 4-3(b). 30 mg (0.13 mmol) of 1-aminoanthraquinone were dissolved in 200 mL 0.5 mol L⁻¹ sulfuric acid using ultra bath to accelerate the dissolution. The obtained solution was kept at 0°C and then 100 mg (1.45 mmol) sodium nitrite were added into the mixture. After 20 minutes, 0.67 mL 50 wt % hypophosphorous acid was added. The reaction mixture was stirred at 0°C for 1 hour. Washing with deionized water and then with acetone was carried out to remove excess acid and adsorbed organic species from the modified surface. The substrate was then dried by N₂. Finally, organic semiconductor was used without any purification step and was dissolved in toluene. Organic semiconductor was drop-casted on the active area.

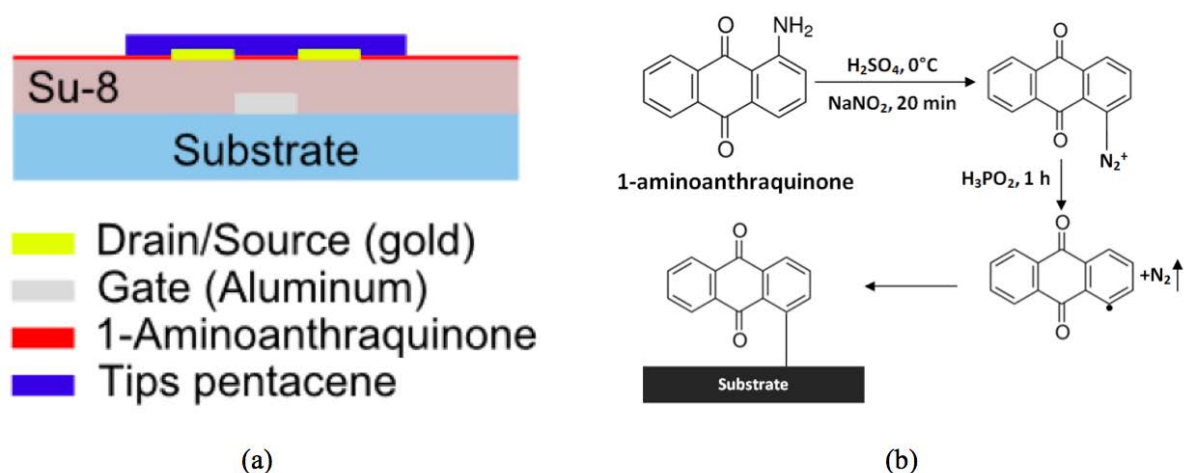


Figure 4-3: Schematic illustration bottom-gate and bottom-contact OTFT structure; b) Grafting protocol of 1-aminoanthraquinone on gate insulator (Su8 2000.5).

The nitrosation of 1-aminoanthraquinone with nitrous acid (generated from sodium nitrite and sulfuric acid used in this work) leads to the formation of the corresponding diazonium salt. In the presence of hypophosphorous acid used as reducing agent, this salt is rapidly converted into a radical after loss of nitrogen. This radical attacks Su8 to form a covalent bond.

In this grafting process of 1-aminoanthraquinone on gate insulator, spontaneous grafting can also occur on gold^[33]. The reaction seems to be more effective on gold than on Su8^[34]. Thus, before immersing OTFT substrate into the chemical solution, protecting gold is necessary. Here, a kind of photoresistor, S1818 was used to protect gold. S1818 cannot be dissolved by sulfuric acid and hypophosphorous acid during grafting process. After grafting process, S1818 can be removed by acetone.

III. Characteristics of Su8 surface after grafting

This section focuses on the four main characteristics of a surface described in section 1: surface roughness, surface energy, surface polarity and dielectric constant. The purpose is to determine which factors have been mainly impacted by chemically modified layer.

III. 1 Surface roughness of dielectrics

Two characterization methods of roughness have been used in this work: RMS roughness and power spectral density (PSD). The RMS roughness and PSD have been

extracted from $2 \times 2 \mu\text{m}$ morphological profile using AFM (Di Caliber Veeco) in tapping mode on bare Su8 and chemically modified Su8 surfaces. Thickness of Su8 gate insulator has been measured using profilometry (TENCOR KLA P6) measurements. The results are summarized in Figure 3-4 and Figure 3-5.

Pictures in Figure 4-4 (a) and (b) show AFM micrograph of surface of bare Su8 and Su8 modified with 1-aminoanthraquinone, respectively. Morphology of modified and unmodified surface shows huge differences. Indeed, 1-aminoanthraquinone grafting step leads to islands creation. Consequently high local z variation (maximum value equal to 10 nm) increases RMS value. Profiles for both surfaces (Figure 4-4 (c) and (d)) along X axis have been extracted and confirmed that bare Su8 presents a sharpest profile than Su8 modified with 1-aminoanthraquinone. For a deeper quantification of lateral variations on the two surfaces, PSD analyzes have been extracted. The PSD indicates the power as a function of the spatial wavelength and is defined as the square modulus of the Fourier transform over the surface profile (Equation 3.1).

$$PSD(f) = 1 \frac{1}{L^2} (\sum_{m=1}^N h_n \exp(2\pi\Delta Lfn)(\Delta L))^2 \quad (3.1)$$

where L represents the surface length in both direction, and f represents the spatial frequency in the X direction. Figure 4-5 shows log-log plot of PSD signal versus the frequency (i.e. $1/\text{spatial wavelength}$) using AFM micrograph from surfaces of bare Su8 and Su8 modified with 1-aminoanthraquinone. Bare Su8 surface shows the lowest PSD signal over the entire frequency range corresponding to a lower RMS value. RMS value and lateral correlation length have been calculated for bare Su8 (RMS = 0.3 nm and lateral correlation length = 46 nm) and Su8 modified with 1-aminoanthraquinone (RMS = 0.6 nm and lateral correlation length = 93 nm).

Compare to bare Su8 surface, surface of Su8 modified with 1-aminoanthraquinone allows the creation of bump but also improves the roughness between bumps (i.e., see hatched area on Figure 4-4 (d)). As a result, regarding surface morphology, surface modification could decrease trapping sites at the interface between organic semiconductor and gate insulator.

The interfacial factor analysis reveals that those contrary effects will be in competition within OTFT structure.

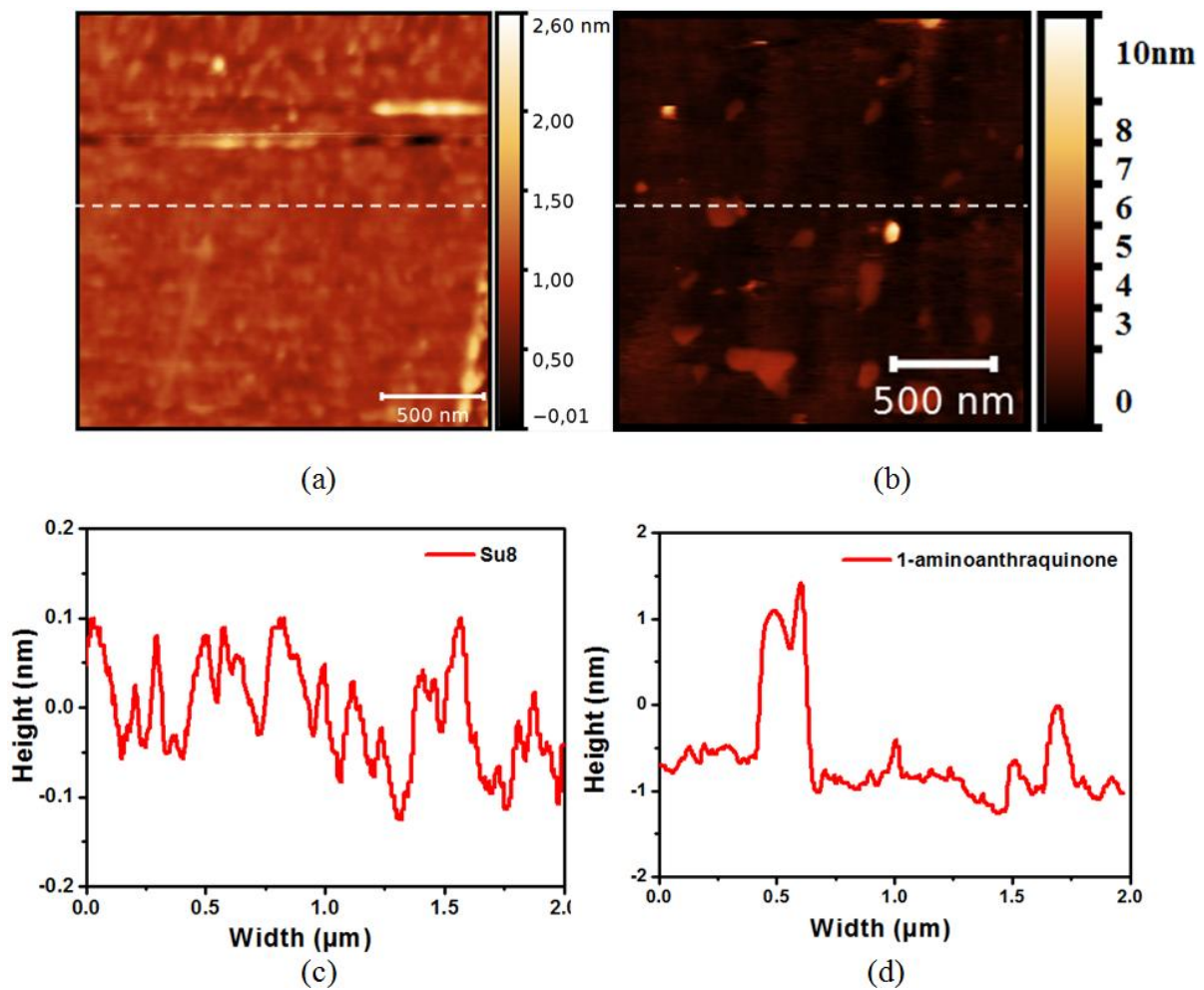


Figure 4-4: Morphological study of bare Su8 and Su8 modified with 1-aminoanthraquinone surface; a) AFM micrograph of 2*2 μm bare Su8 surface; b) AFM micrograph of 2*2 μm modified with 1-aminoanthraquinone surface; c) Profile along X-axis dashed line (Figure 4-4 (a)); d) Profile along x axis dashed line (Figure 4-4 (b)), hashed area revealed low surface roughness between island.

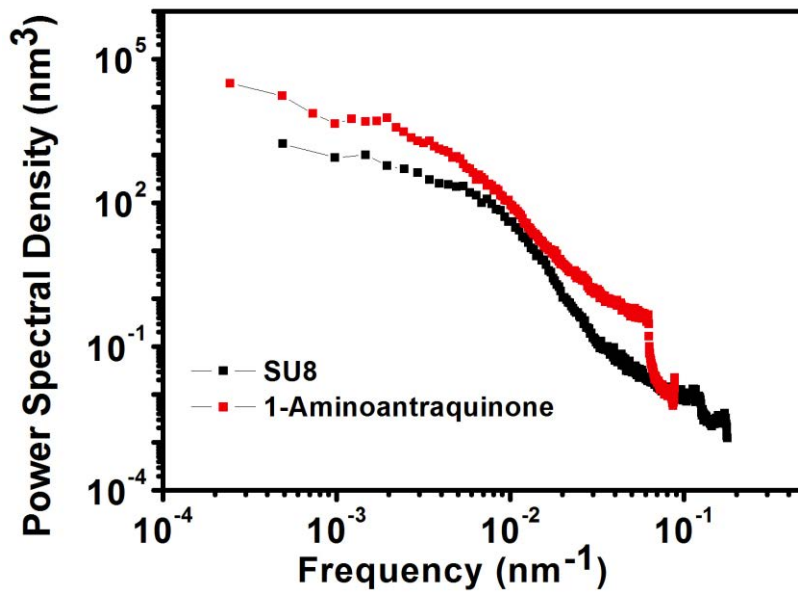


Figure 4-5: PSD analyses for bare Su8 and Su8 modified with 1-aminoanthraquinone surfaces.

III. 2 Surface energy and surface polarity of the dielectrics

Surface energy of dielectrics could be evaluated by measuring the contact angle of two test liquids; one is polar and another is nonpolar. Water and diiodomethane, polar and nonpolar respectively, were used to measure the static contact angle (θ) and then calculate the surface energy (γ_s) of the bare Su8 and Su8 modified with 1-aminoanthraquinone surface. Contact angle was measured using KRUSS DSA30 equipment. Then surface energy was calculated using the following equation (3.2), called Wu method [35]:

$$\gamma_{1s} = \gamma_1 + \gamma_s - 4 \left(\frac{\gamma_1^D * \gamma_s^D}{\gamma_1^D + \gamma_s^D} + \frac{\gamma_1^P * \gamma_s^P}{\gamma_1^P + \gamma_s^P} \right) \quad (3.2)$$

where γ_1 is the surface tension of the test liquid, γ_s is the surface energy of dielectric, and γ_{1s} is the interfacial tension between liquid and dielectric. γ^D and γ^P refer to the dispersive and polar components, respectively. Table 4-1 shows the typical values of liquid used in the work.

	Surface tension (mJ m ⁻²)		
	γ_l^P	γ_l^D	γ_l
Water	52.2	19.9	72.1
Diiodomethane	1.3	49.5	50.8

Table 4-1: Surface tension characteristics of liquid used to calculate surface energy. γ_l^P, γ_l^D are polar and dispersive component respectively.

For the set of experiments, surface energy and polarity have been calculated following Wu's method and summed up in Table 4-2.

	Surface energy (mJ m ⁻²)			Polarity $\chi_p = \gamma_s^P / \gamma_s$
	γ_s^P	γ_s^D	$\gamma_s = \gamma_s^D + \gamma_s^P$	
Bare Su8 2000.5	12.03	33.27	45.3	0.27
1-aminoanthraquinone-Su8	25.79	34.32	60.11	0.43

Table 4-2: Surface energy and polarity of bare Su8 and Su8 modified with 1-aminoanthraquinone surfaces. γ_l^P, γ_l^D are polar and dispersive component respectively.

As shown in Table 4-2, hydrophobic behavior of bare Su8 and Su8 modified with 1-aminoanthraquinone surfaces has been concluded. Bare Su8 surface shows lower surface energy and consequently is more hydrophobic than modified with 1-aminoanthraquinone surface (i.e., θ_{water} of bare Su8 surface = 76° and θ_{water} of Su8 modified with 1-aminoanthraquinone surface = 56°; $\theta_{\text{diiodomethane}}$ of bare Su8 surface = 48° and $\theta_{\text{diiodomethane}}$ of Su8 modified with 1-aminoanthraquinone surface = 46°; data are average on 15 measurements for both surfaces and liquids). The polar component of bare Su8 surface was two times smaller than modified with 1-aminoanthraquinone surface whereas dispersive component was not changed. As a consequence the surface energy and surface polarity are strongly impacted on substrates modified with 1-aminoanthraquinone (increased more than two times). As a result, regarding wetting behavior, surface modification could increase trapping sites at the interface between organic semiconductor and gate insulator.

III.3 Dielectric constant

In this work, Metal-Insulator-Metal (MIM) structure was used to characterize the dielectric constant of insulator. Highly doped n-type silicon wafer was used as substrate, Su8 2000.5 was spin coated on silicon wafer with the thickness of 400 nm as insulator layer. Aluminum was thermally evaporated on Su8 with the thickness of 150 nm then etched according to the design of metal electrode. Chemically grafting process was performed after spin coating Su8. Dielectric constant was dependent on the frequency applied during characterization. Dielectric constant can be calculated as equation (3.3):

$$\epsilon_r = \frac{C \cdot d}{S \cdot \epsilon_0} \quad (3.3)$$

Where C represents the capacitance, d represents the thickness between two plates (two metal plates), S represents the area of the electrode, ϵ_0 represents the vacuum dielectric constant with the value of $8.85 \times 10^{-12} \text{ F m}^{-1}$. Table 4-3 shows the dielectric constant under different frequency.

	100 KHz	200 KHz	300 KHz	400 KHz
Bare Su8 2000.5	4.14	4.04	4.09	4.2
1-aminoanthraquinone -Su8	4.12	3.95	4.01	4.12

Table 4-3: Dielectric constant under different frequency.

No significant difference was obtained between dielectric constant of bare Su8 and Su8 modified with 1-aminoanthraquinone. It can be concluded that 1-aminoanthraquinone modification does not vary the dielectric constant.

In conclusion, chemical modification with 1-aminoanthraquinone has no significant effect on dielectric constant. On the other hand, it shows high surface energy and polarity, which could increase trapping sites at the interface leading to worse performance of OTFTs. In contrary, it improves the surface roughness, which could decrease trapping sites at the interface leading to better performance of OTFTs. In next section, electrical characteristics will be performed in order to check the impact of chemical modification

IV. Electrical properties in OTFTs modified with 1-aminoanthraquinone

This section focuses on the possible improvement of electrical properties in OTFTs modified with 1-aminoanthraquinone. Mobility and stability of OTFTs were characterized to check the improvement. Successive transfer characteristics, hysteresis, gate leakage current, and bias stress measurement were employed to check the stability of OTFTs.

IV.1 Electrical parameters of OTFTs

OTFTs were fabricated in “bottom-gate and bottom-contact” geometry with un-treated insulator surface and chemical modified insulator surface as reported previously. I_{DS} - V_{GS} Figures were used to estimate the field-effect mobility μ , threshold voltage V_{TH} , subthreshold slope SS, and I_{on}/I_{off} ratio.

The transfer characteristics of same size OTFTs ($W=1000 \mu\text{m}$ and $L=5 \mu\text{m}$) with and without surface modification are shown in Figure 4-6 (a). The parameters of these same size transistors are compared in Table 4-4.

	μ ($\text{cm}^2/\text{V.s}$)	V_{TH} (V)	SS (V/dec)	I_{on}/I_{off} ratio
Without surface modification	10^{-3}	5.2	6.6	5×10^2
With surface modification	10^{-2}	20.5	5.1	10^3

Table 4-4: Electrical characteristics of OTFTs with and without surface modification.

Through the mobility, the subthreshold slope and the I_{on}/I_{off} ratio, OTFT with chemical modified insulator surface is highly improved. However, the threshold voltage is much lower for this chemically modified insulator OTFT. It is positive for both transistors that means Su8 gate insulator contains negative charges. However the highly positive threshold voltage of chemically modified transistor means the chemical product introduces extra negative charges that is not expected. However these extra charges do not change the swing of the transistor with even a slight improvement of the subthreshold slope.

The other consequence of the presence of negative charges is the off-current that is higher in the chemically modified insulator OTFT. These negative charges induce an accumulation of positive charges in the active layer that keep it more conductive.

From the point of view of the uniformity of different OTFTs in the same process, Figure 4-6 (b) shows a statistical study of the mobility of differently sized transistors processed without or with chemical modification. This study confirms the higher mobility after surface modification. The mean mobility is 2.74×10^{-2} and $0.58 \times 10^{-3} \text{ cm}^2/\text{V.s}$ respectively. However acceptable uniformity of the mobility is observed in the limit of the 7 characterized transistors in both cases. The standard deviation is 0.5 and $0.2 \text{ cm}^2/\text{V.s}$ with and without surface modification.

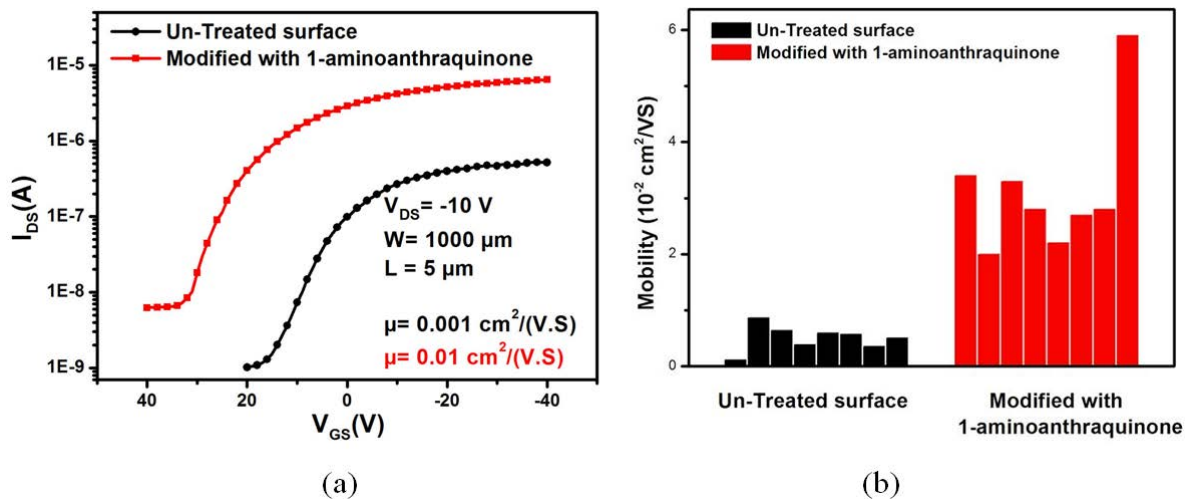


Figure 4-6: (a) Transfer and (b) statistics characteristics of un-treated insulator surface and chemical modified insulator surface.

IV.2 Stability of OTFTs

Stability of OTFTs under functioning is also an important parameter to check. It determines their reliability. In this section, successive measurements, hysteresis characteristics, gate leakage current, and bias stress characteristics are used to characterize the stability.

● Successive measurements of the transfer characteristics

The first part of operational stability test consists in checking the reproducibility of successive plots of transfer characteristics. In the following, transfer characteristics are successively plotted 10 times. Figure 4-7 presents the 10 transfer characteristics for both untreated and treated surface OTFTs and their continuous shift during the 10 measurements.

Obviously the threshold voltage of untreated surface OTFT shifts a lot compared to the shift for treated surface OTFT. The threshold voltage of treated surface OTFT is nearly constant with very small shift. Figure 4-7 shows that this conclusion is valuable even when characterizing 5 transistors fabricated in the same run.

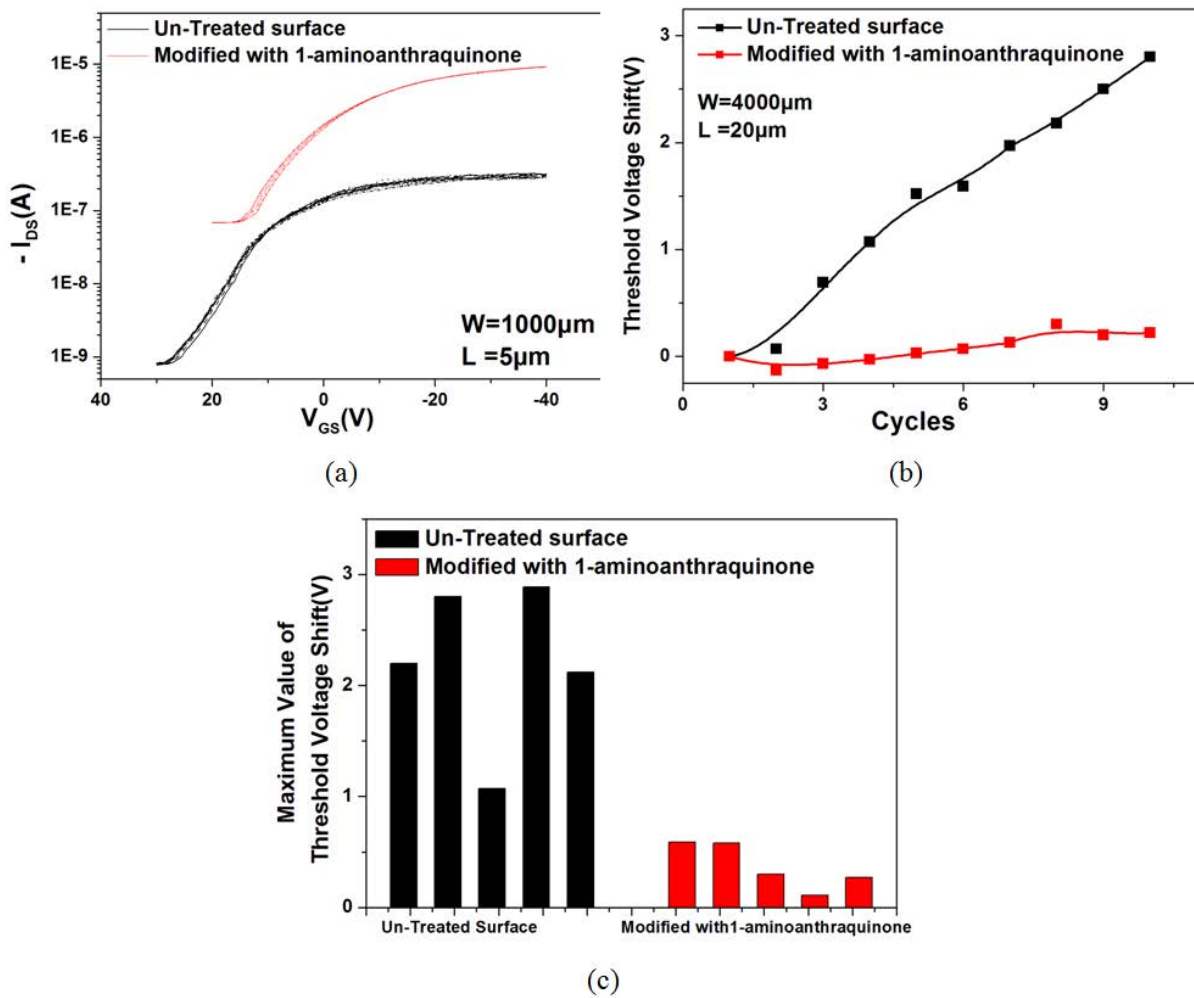


Figure 4-7: Electrical characteristics of OTFTs with and without modified with 1-aminoanthraquinone during 10 times repeated cycling test: (a) Transfer characteristics of 10 times repeated cycles test, (b) Threshold voltage shift of successive transfer characteristics as a function of cycles, (c) Statistics of repeated cycling test with different devices. Repeated cycling test acquired at $V_{DS}=-10V$.

- ***Hysteresis characteristics***

The second part of operational stability test is characterized by a hysteresis when plotting the transfer characteristics from positive to negative gate voltage values and coming back. In papers dealing with OTFTs, statement like “hysteresis must be avoided” or “only negligible hysteresis is observed” can often be found. Hysteresis is quantified by the difference in the source-drain current (I_{DS}) values observed during forward and backward sweeps of the gate voltage (V_{GS}). The reported mechanisms are categorized below ^[36]: i) Effects of mobile charges at the channel; ii) Effects resulting in a polarization of the gate dielectric; and iii) Charge injection from the gate electrode into the dielectric. Lower back sweep current than the forward sweep current is very often attributed to charge carrier trapping close to the channel or charge injected from the semiconductor into the dielectric, whereas higher back sweep current is usually caused by mobile ions in the dielectric, or by polarization of the dielectric.

For hysteresis characterization, at least 10 devices were characterized and for each transistor at least 5 times repeated cycles were measured. An obvious decrease of the hysteresis shift is observed in Figure 4-8 with modified with 1-aminoanthraquinone OTFTs. Figure 4-8 shows that this observation is valuable even when characterizing 6 transistors fabricated in the same run.

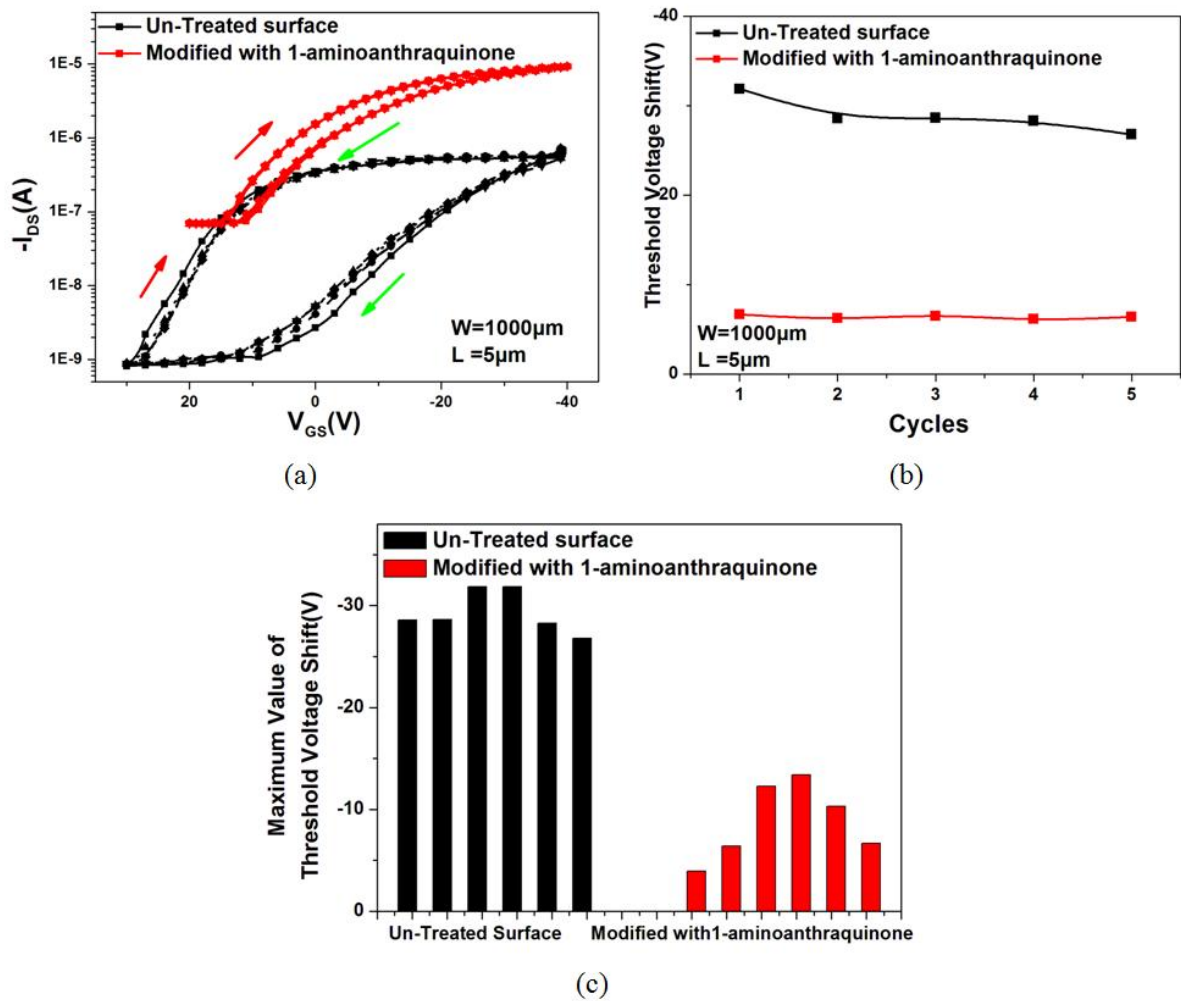


Figure 4-8: Electrical characteristics of OTFTs with and without modified with 1-aminoanthraquinone: (a) Hysteresis characteristics, (b) Threshold voltage shift of hysteresis characteristics as a function of cycles. (c) Statistics of hysteresis characteristics with different devices. Repeated hysteresis cycling test acquired at $V_{DS}=-10V$.

Figure 4-8 (a) shows transfer characteristics where the back sweep current is lower than the forward sweep current for both un-treated Su8 and modified with 1-aminoanthraquinone. As described above, lower back sweep current hysteresis is attributed to charge carrier trapping close to channel or charge injected from semiconductor into the dielectric. Modification with 1-aminoanthraquinone decreases hysteresis due to the fact that surface modification with 1-aminoanthraquinone improves the roughness, decreases trapping sites at the interface between organic semiconductor and gate insulator.

● **Gate leakage current**

In field-effect transistors, gate insulator has to insulate efficiently the gate from the channel insuring efficient field effect of the gate. We have seen before in chapter 2 (Figure 2-8 (a)) that the gate leakage current depends on the intrinsic insulating properties of solution deposited Su8 film but also on the solvent of the semiconducting Tips-pentacene layer. This solvent can weaken the Su8 insulating quality. It can be interesting here to check the effect on the gate current of the functionalization of Su8 before depositing the semiconducting layer.

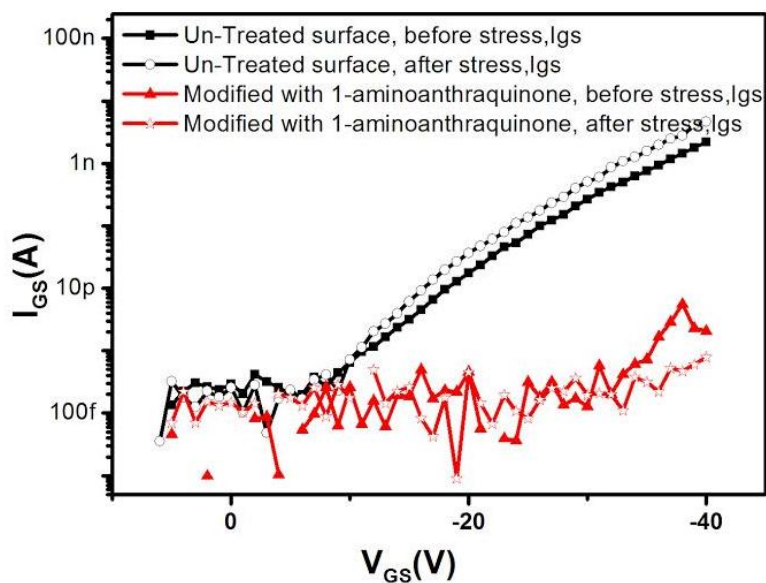


Figure 4-9: Leakage current of un-treated insulator surface and modified with 1-aminoanthraquinone surface before and after bias stress.

Figure 4-9 shows the behavior of the leakage current with the gate voltage for same size OTFTs without and with surface modification of Su8. This behavior is showed before and after gate bias stressing OTFTs. The curves confirm the lower influence of the gate bias stress on the Su8 surface modified transistors.

The new result is the high decrease of the gate current by more than 4 orders after surface modification of Su8. Surface modification by 1-aminoanthraquinone acts efficiently to reinforce the insulation of the gate.

To confirm this conclusion, highly doped Silicon wafer-Su8 (chemically modified surface or not)-Aluminum (Metal-Insulator-Metal) structures have been fabricated. Before depositing the top Aluminum electrode, a drop of toluene have been deposited or not on previously surface modified or not spin-coated Su8 film. The purpose of this drop of toluene

is to simulate the effect of the solvent of Tips-pentacene on the gate insulating. Toluene was chosen following the results given in Chapter 2 where toluene weakens a little bit the Su8 insulator.

Figure 4-10 shows the current-voltage characteristics of these MIM structures.

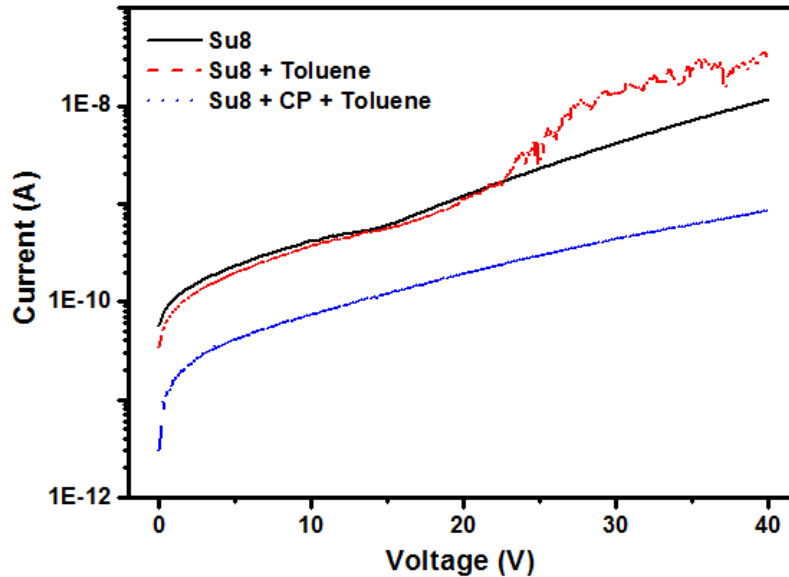


Figure 4-10: Current-voltage characteristics of MIM structures using only Su8 as insulator, or Su8 with a drop of toluene on it or surface modified Su8 with a drop of Su8.

As shown in Chapter 2, drop of toluene on Su8 weaken a little bit the insulating property of Su8 leading to a slight increase of the current. The supplementary result here is that surface modification of Su8 by 1-aminoanthraquinone not only protects Su8 from toluene but reinforces highly the insulating properties of Su8.

- **Effect of gate bias stress**

Figure 4-9 showed the beneficial effect of the surface modification of Su8 on the behavior of the gate leakage current under gate bias stress. In fact, its main effect can be well highlighted by the shift of the threshold voltage under the gate stress. Figure 4-11 shows the much lower shift after surface modification.

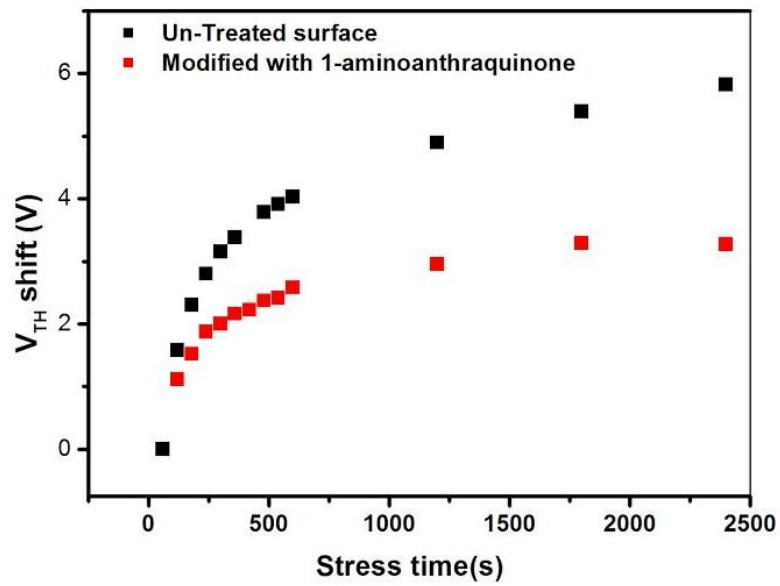


Figure 4-11: Bias stress characteristics of the OTFTs with un-treated insulator surface and modified with 1-aminoanthraquinone surface, acquired at gate bias $V_{GS}=-20V$, $V_{DS}=-10V$.

Conclusion

Functionalizing the surface of the Su8 gate insulator with 1-aminoanthraquinone before depositing Tips-pentacene active layer leads to huge improvement of the electrical parameters of OTFTs. The field effect mobility increases. The subthreshold slope decreases. The on/off current ratio increases. The gate leakage current decreases. The hysteresis of the transfer characteristic decreases. Then nearly all the electrical parameters improve. Only the threshold voltage increases becoming more positive and the off-current increases. The increase of the threshold voltage means the presence of more negatively charged energy levels inside the insulator that are introduced by the chemical product. The negative charges of these levels do not change under the application of the gate voltage as the subthreshold slope do not degrade and even it improves.

The present preliminary study on the effect of a functionalization of the gate insulator before depositing the semiconducting active layer showed all its expected benefit. Here 1-aminoanthraquinone was used as precursor of the diazonium salt to modify the insulator surface due to the presence of condensed benzene rings in its structure. It is only an example. Deep study has to be made in the future.

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Conclusion and perspective

Present work was done in the new trend to get highly flexible electronics by using fully Organic Thin-Film Transistor (OTFT) as the basic element of this electronics. Indeed, only fully organic devices, with all the components made on organic materials, can fulfill the requirement of flexible or stretchable electronics. Adding the requirement of lowest cost, only fully solution processed at ambient temperature devices can fulfill these both requirements.

Then, adding more the requirement of reproducible process, solution fabricated devices can be made only by printing. Indeed, only printing can lead to controllable and then reproducible printed volume and deposition conditions.

This why inkjet printing was the main goal of this work in the final purpose to fabricate reliable electronic functions at the lowest cost on flexible substrate.

Efficient electronics uses both n-type and p-type transistors leading to CMOS electronics.

Fixing the way to reach this final purpose, we started in determining the parameters leading to the best electrical performance of solution fabricated transistors, where both the semiconducting active layer and the gate insulator were made on organic materials. The effect of common parameters of any solution technique, solvent, drying/annealing temperature, and surface functionalization was studied through the use of most simple solution technique, drop-casting, to deposit C₆₀ and Tips-pentacene films as active layer leading to n-type and p-type transistors respectively.

Process of n-type OTFT based on C₆₀ was unreliable, mainly due to the poor solubility of C₆₀ in organic solvent. In the contrary, p-type OTFTs based on Tips-pentacene were more reliable. Great effect of the type of solvent on the performance of these transistors was demonstrated.

After this first attempt, the most reliable solution technique, inkjet printing, was used to reach the most reliable transistor.

In the first step, printing parameters of each ink, jettability, wetting, printability, and patterns optimization, leading to the deposition of conductive contacts, gate insulator and semiconducting active layer were studied. If the printing of silver conductive contacts and photoresist Su8 as gate insulator were well optimized, the study showed the obvious difficulty in the deposition of semiconducting Tips-pentacene layer.

That's why in view of a progressive introduction of printing technique in the transistor's process, OTFTs were fabricated using printing technique only for the deposition of silver layer for the gate contact and drain-source contacts and the deposition of Su8 film for the gate insulator. Semiconducting C₆₀ film was evaporated for the active layer of n-type transistors. Results led to remark that these n-type OTFTs work if printed Su8 gate insulator is enough thick (in the order of 1 μm).

For p-type OTFTs facing to the difficulty to print Tips-pentacene, drop-casted Tips-pentacene was used as active layer were fabricated only to advance in the way towards fully solution deposited OTFTs. However, Tips-pentacene film splits in 2 parts after drying. Su8 being more hydrophobic than silver, semiconductor pins firmly on drain and source silver contacts.

Facing to this dewetting problem of Tips-pentacene diluted in pure solvent, one novel idea was to blend Tips-pentacene with Su8 before depositing it. Adding Su8 molecule will help to pin the contact line of the droplet independently of the hydrophobicity of the under layer, and particularly on Su8 gate insulator. The success of depositing uniform drop casted blended Tips-pentacene on printed Su8 and printed silver source and drain, was the key to fabricate fully solution deposited OTFTs using this blended Tips-pentacene as active layer. OTFTs worked with very bad characteristics however. On-current was very low and threshold voltage very high. It seems blended Tips-pentacene forms bad electrical contact with printed silver, leading to very difficult injection of electrical charges inside the channel.

Then, evaporated gold drain/source electrodes were used to check the functioning of OTFTs using drop casted Su8 blended Tips-pentacene on printed Su8 as active layer. This step was considered as an intermediary one, waiting for a future jump of the problem. Depending on the blending ratio, OTFTs presented interesting characteristics validating the use of drop-casted blended Tips-pentacene as active layer of fully solution deposited transistors. This result was also validated by using printing in place of drop-casting for the deposition of blended Tips-pentacene. However coming back to silver in place of evaporated gold led to bad results. The conclusion is that printed silver is not compatible with solution deposited blended Tips-pentacene. The only solution is to functionalize silver or to use another conductor as carbon for example.

In the last part, we tried to check the effect of a chemical functionalization of the surface of the Su8 gate insulator before depositing the semiconducting active layer. Indeed, the interface between the insulator and the semiconductor influences largely the performance

of any field effect transistor. Here choosing 1-aminoanthraquinone for the functionalization led to obvious improvement of nearly all the electrical parameters of the OTFTs. Deep study on the functionalization of the gate insulator surface has to be given in future.

Finally the present thesis is a large overview of the issues and the difficulties that have been to jump and to solve in the way to fabricate fully printed organic transistors. Some solutions have been given and new ideas have been proposed. However, this work is the first one fully devoted to printed OTFTs. Other works focusing on each of the issues highlighted here have to be given to reach the main goal that is the fabrication of reproducible and high performance fully printed electronics.

Résumé

Le travail entre dans le cadre de la nouvelle tendance à la recherche d'une électronique mécaniquement flexible basée sur des transistors en couche mince constitués uniquement de matériaux organiques (OTFT). OTFT de type n et de type p ont été fabriqués by la technique de dépôt par impression (inkjet) et étudiés. Les paramètres d'impression (jetabilité, mouillabilité, imprimabilité et possibilité d'obtention de différentes formes), de chaque encre permettant le dépôt de couches conductrices, isolantes et semiconductrices, ont été systématiquement étudiés.

Les OTFT de type n basés sur du C_{60} se sont montrés non fiables, principalement du fait de la faible solubilité du C_{60} dans les solvants organiques. Les OTFT de type basés sur du Tips-pentacene ont montré par contre une grande fiabilité.

Le travail global constitue une large revue des problèmes et difficultés rencontrés dans la fabrication de transistors fabriqués entièrement par impression jet d'encre. Des solutions ont été trouvées et de nouvelles idées sont proposées.

Mots clés: Transistors en couche mince constitués uniquement de matériaux organiques, impression, n basés OTFT, p basés OTFT.

Abstract

Present work deals with the new trend to get highly flexible electronics by using fully Organic Thin-Film Transistor (OTFT) as the basic element of this electronics. Fully organic n-type as well as p-type OTFT processed by inkjet printing are studied. Printing parameters of each ink, jettability, wetting, printability, and patterns optimization, leading to the deposition of conductive contacts, gate insulator and semiconducting active layer are studied.

Process of n-type OTFT based on C_{60} is shown as unreliable, mainly due to the poor solubility of C_{60} in organic solvent. In the contrary, p-type OTFTs based on Tips-pentacene are much more reliable.

The work is a large overview of the issues and the difficulties that have been to jump and to solve in the way to fabricate fully printed organic transistors. Some solutions have been given and new ideas have been proposed.

Key words: Organic Thin-Film Transistor (OTFT), inkjet print, n-type OTFT, p-type OTFT.