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Christelle Saber

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Analysis and optimization of the conducted emissions of an on- board charger for electric vehicles

Analyse et optimisation de la CEM conduite d'un chargeur de batteries embarqué dans un véhicule électrique

Thèse de doctorat de l'Université Paris-Saclay
préparée à L'Ecole Normale Supérieure de Cachan
(Ecole Normale Supérieure Paris-Saclay)

École doctorale n°575
Electrical, Optical, Bio-physics and Engineering (EOBE)
Spécialité de doctorat: Génie Electrique

Thèse présentée et soutenue à Cachan, le 19/10/2017, par

M^{me} Christelle SABER

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For all the members of my larger family, I thank you all!

Résumé des travaux de thèse intitulée : Optimisation de la CEM conduite des chargeurs embarqués dans les véhicules électriques

Les travaux présentés dans cette thèse s'inscrivent dans le cadre d'une convention CIFRE. Il s'agit d'une collaboration de recherche entre l'équipe d'Electronique de Puissance et d'Intégration du laboratoire SATIE et l'équipe de Conception en Electronique de Puissance du Technocentre de Renault S.A.S. Elle porte sur l'optimisation d'un chargeur de batteries pour les véhicules électriques (VE).

La charge d'un VE constitue un enjeu stratégique pour les constructeurs automobile et forme un réel défi à relever avant de pouvoir comparer ces véhicules à la simplicité d'usage du véhicule thermique. En effet, l'autonomie limitée, la durée de recharge de la batterie, le coût du déploiement d'une infrastructure de charge rapide, l'impact significatif sur les réseaux électriques et le coût élevé de la batterie sont à l'origine de plusieurs projets de recherche axés sur l'optimisation de la chaîne de recharge du VE.

Il existe diverses solutions qui permettent l'amélioration de l'autonomie d'un VE. A cet effet, soit la capacité de la batterie peut être augmentée soit la charge peut être facilitée en réduisant la durée de recharge. La réduction du temps de charge peut être assurée par l'augmentation de la puissance de charge. Cependant, les infrastructures de charge rapide étant encore limitées, une solution contraignante mais stratégique consiste à embarquer le chargeur dans le véhicule afin d'assurer la conversion ac-dc de l'énergie à partir des prises de courant. Cette solution permet d'augmenter la disponibilité de la charge pour les utilisateurs.

En outre, le chargeur embarqué peut réutiliser tout, ou une partie des éléments déjà existants et nécessaires à la propulsion du véhicule. L'idée étant de pouvoir employer certains éléments de la chaîne de traction électrique, déjà embarqués dans le VE (moteur électrique et onduleur de tension), et d'ajouter un filtre d'entrée et un redresseur afin de concevoir un chargeur intégré à la chaîne de traction. Cette solution permet de réduire le coût du chargeur, sa taille ainsi que le volume nécessaire à l'intégration de ses constituants électriques, on parle alors de chargeur intégré à la chaîne de traction.

Cependant, la réutilisation de l'électronique de puissance embarquée engendre des problèmes de compatibilité électromagnétique (CEM) avec d'autres équipements connectés sur le réseau électrique et aussi avec les dispositifs de protection domestiques. Ceci peut remettre en cause la disponibilité de la charge du VE.

Le problème majeur à lever est donc, la limitation des émissions conduites et plus particulièrement des courants de mode commun dans une gamme de fréquence importante.

Comme réponse aux problèmes d'interférence, il paraît plus simple aux concepteurs de définir des cellules de filtrage en aval de la conception de la structure, que d'intégrer des critères minimisant les perturbations électromagnétiques durant la phase de conception. Ainsi, la solution actuelle consiste à émettre le moins possible en adaptant le contrôle du chargeur et à inclure un filtre CEM composé de plusieurs étages de filtrage en mode commun et en mode différentiel. Ce type de solution dégrade la compacité et le coût du chargeur.

Cette thèse a donc, pour objectifs principaux, l'amélioration de la disponibilité de la charge actuelle tout en réduisant le volume du filtre CEM passif.

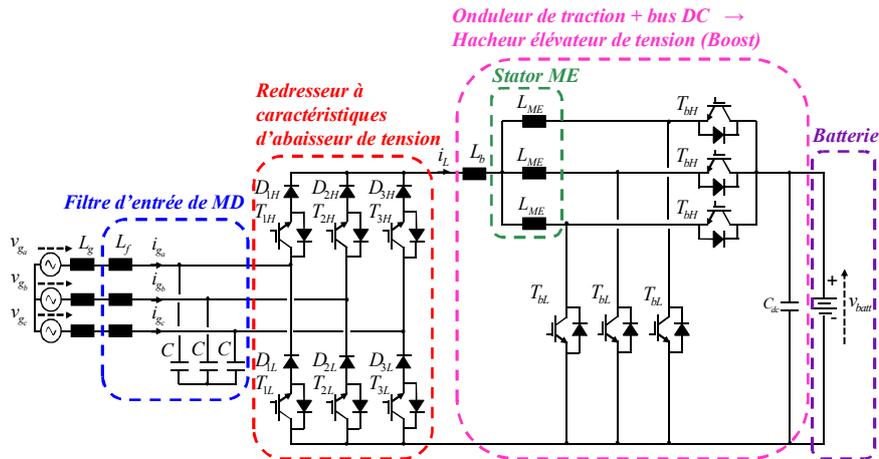


Fig.1. Structure triphasée du chargeur de batterie embarqué dans le VE, intégré à la chaîne de traction électrique et non-isolé (sans isolation galvanique) par rapport au réseau électrique.

Selon des critères définis au démarrage des projets sur le VE, la topologie du chargeur est imposée et ne sera pas remise en question au cours de cette étude. Elle est constituée d'un redresseur triphasé commandé, unidirectionnel en courant dont le fonctionnement permet d'abaisser la tension suivi, pour simplifier, d'un hacheur élévateur de tension. La structure globale du chargeur (Fig.1) utilise les enroulements statoriques de la machine électrique (ME) et l'onduleur de traction en tant qu'hacheur élévateur de tension afin d'adapter le niveau de tension du réseau d'alimentation sur lequel le système se connecte à celui de la batterie suivant l'état de charge de cette dernière. L'étage d'entrée est un redresseur présentant finalement les mêmes fonctionnalités qu'un hacheur abaisseur. Afin d'éviter tout risque lié au développement d'un couple au niveau de la ME à l'arrêt, les bras d'onduleur, configurés pour un fonctionnement en hacheur élévateur de tension, ne sont pas entrelacés et reçoivent des commandes identiques. Ainsi, pour une charge monophasée, étudiée en détail, la topologie équivalente est celle présentée à la Fig.2. L'inductance équivalente définie par la mise en parallèle des enroulements de la machine associés aux trois bras du Boost n'étant pas suffisante pour assurer une ondulation acceptable du courant redressé, une inductance supplémentaire L_b est ajoutée, en série, sur le bus dc intermédiaire entre les deux convertisseurs de puissance.

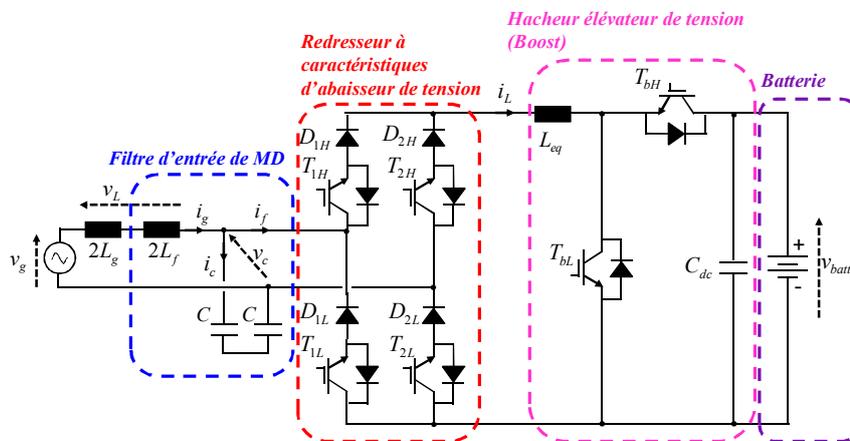


Fig.2. Topologie de charge monophasée avec commande synchrone des bras du Boost.

Nous cherchons, à travers ces travaux, à identifier des domaines d'améliorations possibles, à proposer des solutions à bas coûts et à intégrer des modifications au niveau de la commande et de la topologie afin d'optimiser le comportement CEM, tant en basses fréquences (0 – 2 kHz) qu'en hautes fréquences (150 Hz- 30 MHz), de ce chargeur embarqué intégré sans isolation galvanique. Les propositions doivent répondre simultanément aux besoins de recharge domestique en monophasé (à 3.7 kW et à 7.4 kW) et rapide en triphasé (à 22 kW et à 43 kW) sans pour autant augmenter le volume ni les coûts engendrés.

Chacun des cinq axes de travail étudiés, en vue de la réduction du volume du filtre CEM d'entrée, a été précédé par une étude exhaustive de l'état de l'art. Ceci a permis de faire ressortir les solutions les plus pertinentes et d'en proposer des nouvelles mieux adaptées à la structure de chargeur étudiée. Les axes de travail peuvent être résumés comme suit:

■ *Optimisation du comportement CEM (0-2 kHz) du chargeur en monophasé*

- Proposition d'une nouvelle loi de commande qui assure la correction du facteur de puissance en entrée. Cette commande inclus :
 - Une stratégie pour la régulation de la puissance de charge (Fig.3).
 - Une stratégie pour la correction du facteur de déplacement ($\cos \varphi$) entre les fondamentaux de la tension et du courant réseau mesuré en amont du filtre CEM (Fig.4).
 - Une méthode d'identification en ligne de l'impédance du réseau basée sur la transformée de Fourier discrète.
 - Une répartition astucieuse des commandes du redresseur et du Boost de manière à ce qu'à chaque instant, uniquement, l'un des deux soit en commutation (Fig.5).
- Identification d'un problème de distorsion du courant absorbé au réseau à chaque passage par zéro de la tension du réseau (Fig.6). A travers l'analyse de la structure nous avons pu démontrer que la correction du facteur de déplacement provoque des paliers à zéros dans le courant absorbé par le redresseur qui, à leurs tours, excitent la résonance du filtre de mode différentiel.
- Développement d'une solution à base d'amortissement actif qui permet d'amortir ces résonances à travers l'émulation d'une résistance virtuelle placée en parallèle des condensateurs d'entrée (Fig.7).
- Les apports de cette nouvelle régulation monophasée sont:
 - la réduction des pertes par commutation (les deux convertisseurs ne fonctionnent plus simultanément pendant la charge) ;
 - la réduction du niveau de courant de puissance parcourant la structure ;
 - la réduction des pertes par conduction, par commutation ainsi que la taille des éléments passifs ;
 - l'amélioration du facteur de puissance qui tend vers l'unité ;
 - la réduction du taux de distorsion harmonique (TDH).

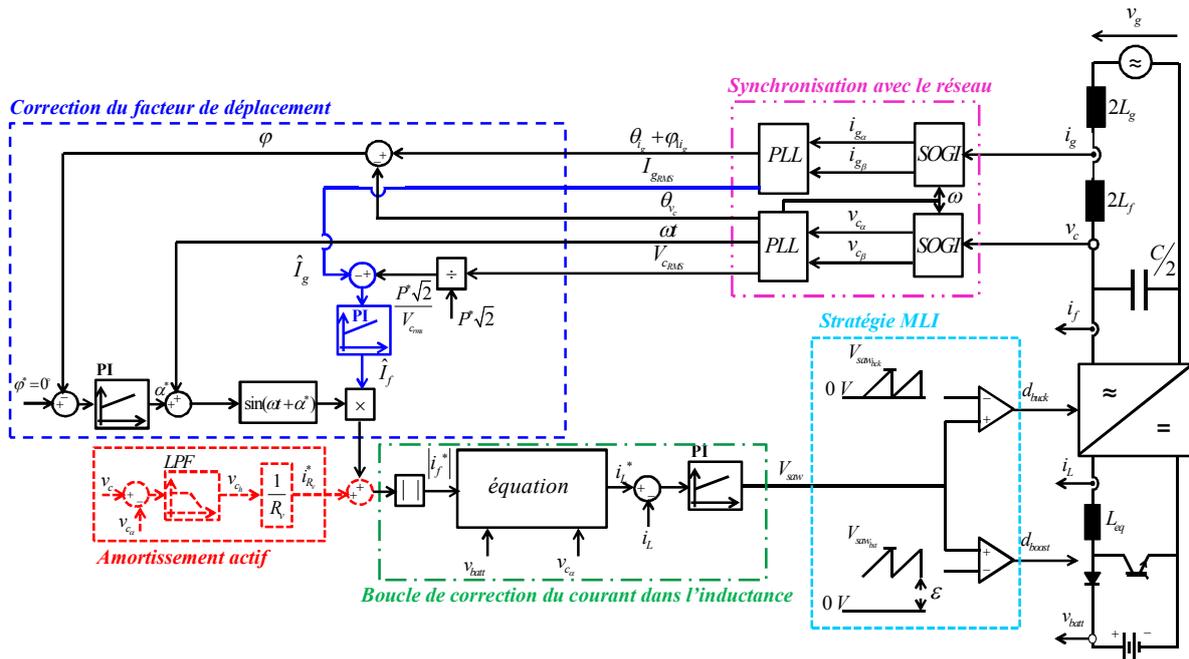


Fig.3. Loi de commande globale proposée pour la charge monophasée de la structure.

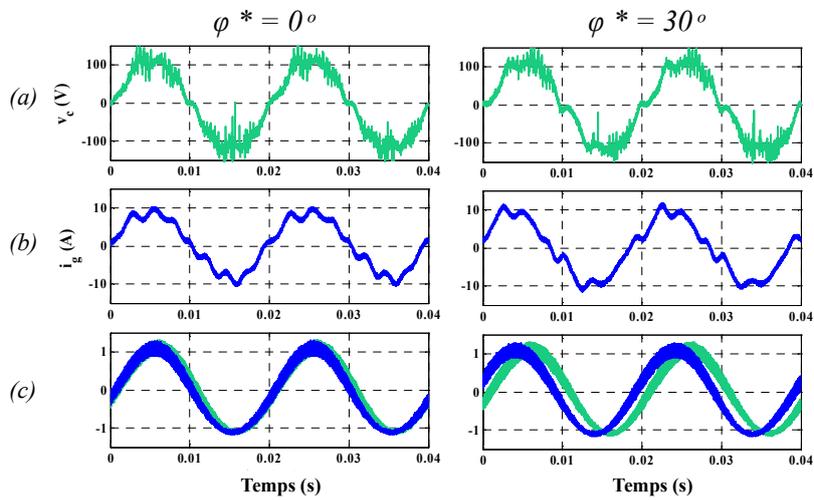


Fig.4. Résultats expérimentaux pour la correction du facteur de déplacement avec deux références de déphasage différentes. (a) Tension en entrée du redresseur. (b) Courant réseau montrant une résonance périodique. (c) Fondamentaux normalisés de la tension (vert) et du courant réseau (bleu).

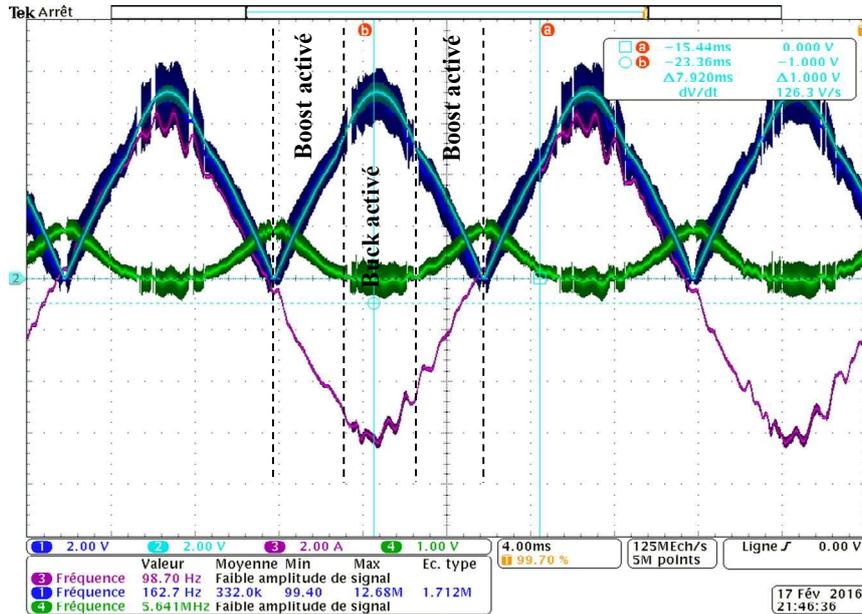


Fig.5. Résultats expérimentaux pour $\varphi^*=0^\circ$ sans amortissement actif en un point de fonctionnement qui montre les deux modes de fonctionnement soit en Buck soit en Boost. (Bleue foncé) Courant mesuré i_L parcourant l'inductance de filtrage. (Cyan) La référence imposée au courant i_L^* . (Rose) Courant réseau (sans filtre CEM). (Vert) Modulante issue de la boucle de correction du courant i_L .

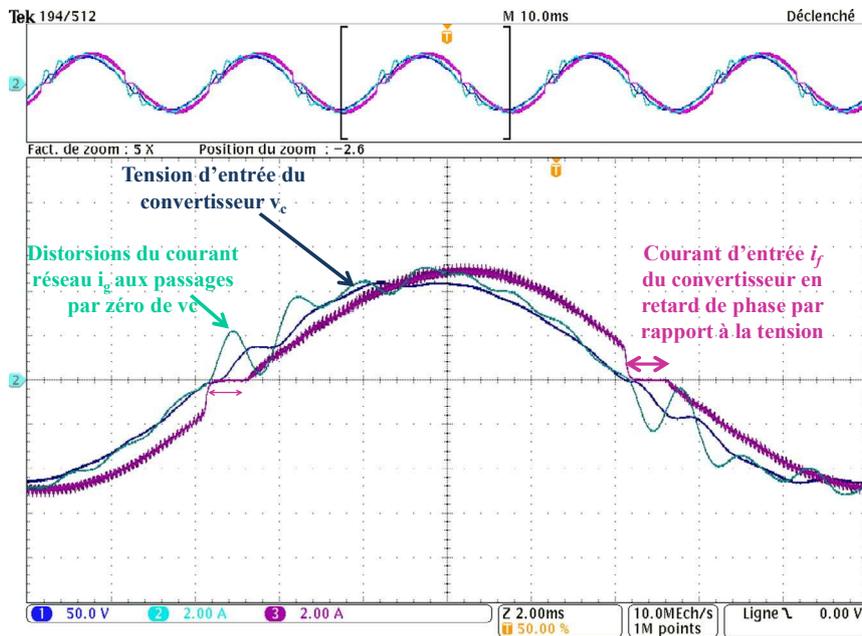


Fig.6. Résultats expérimentaux pour un déphasage nul $\varphi^*=0^\circ$ sans amortissement actif mettant en relief les paliers à zéro du courant absorbé par le redresseur. (Bleue foncé) Tension d'entrée du convertisseur v_c . (Cyan) Courant absorbé au réseau en amont du filtre CEM i_g . (Rose) Courant moyen absorbé par le redresseur i_f , ayant un retard de phase par rapport à la tension d'entrée.

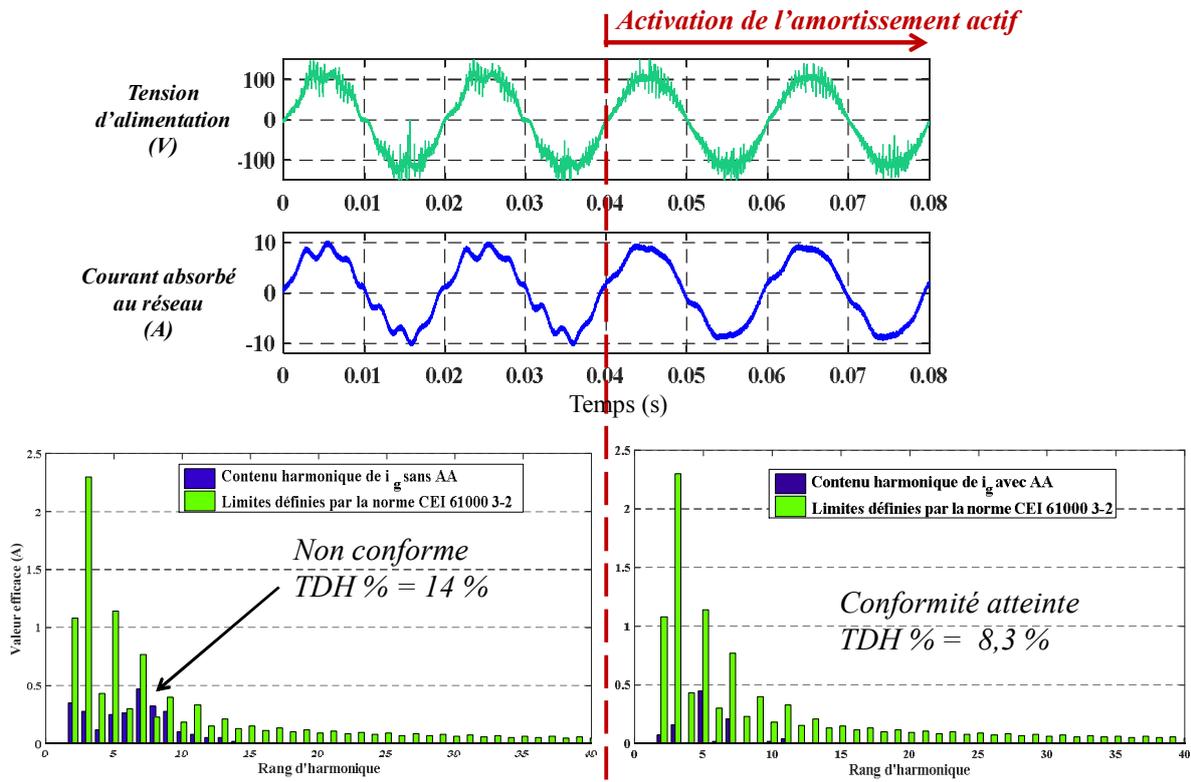


Fig.7. Résultats expérimentaux pour un déphasage nul montrant la qualité du courant absorbé au réseau avant et après l'activation de l'amortissement actif.

■ Optimisation du comportement CEM (0-2 kHz) du chargeur en triphasé

- Proposition d'une nouvelle loi de commande en triphasé pour réduire les harmoniques basses fréquences (Fig.8). Cette commande permet de réduire le niveau du courant de puissance transitant dans la structure à iso-puissance de charge. En outre, elle est conçue de manière à ce que le Boost ne soit pas sollicité pour des niveaux de tensions du réseau de l'ordre de $230 V_{eff}$.
- Proposition d'une nouvelle stratégie de modulation vectorielle pour le pilotage des interrupteurs du redresseur triphasé. Cette stratégie permet de réduire les fluctuations de tensions aux bornes de la capacité parasite formée entre la batterie et le châssis. D'autre part, elle permet également de réduire les pertes par commutations aux bornes des diodes et des IGBT du redresseur.
- Les apports de cette loi de commande en triphasée sont :
 - la réduction des pertes par commutation ;
 - la réduction des pertes par conduction ;
 - le niveau de courant dans l'inductance est beaucoup plus réduit ;
 - la bonne maîtrise du facteur de puissance ;
 - la conformité avec les normes harmoniques.

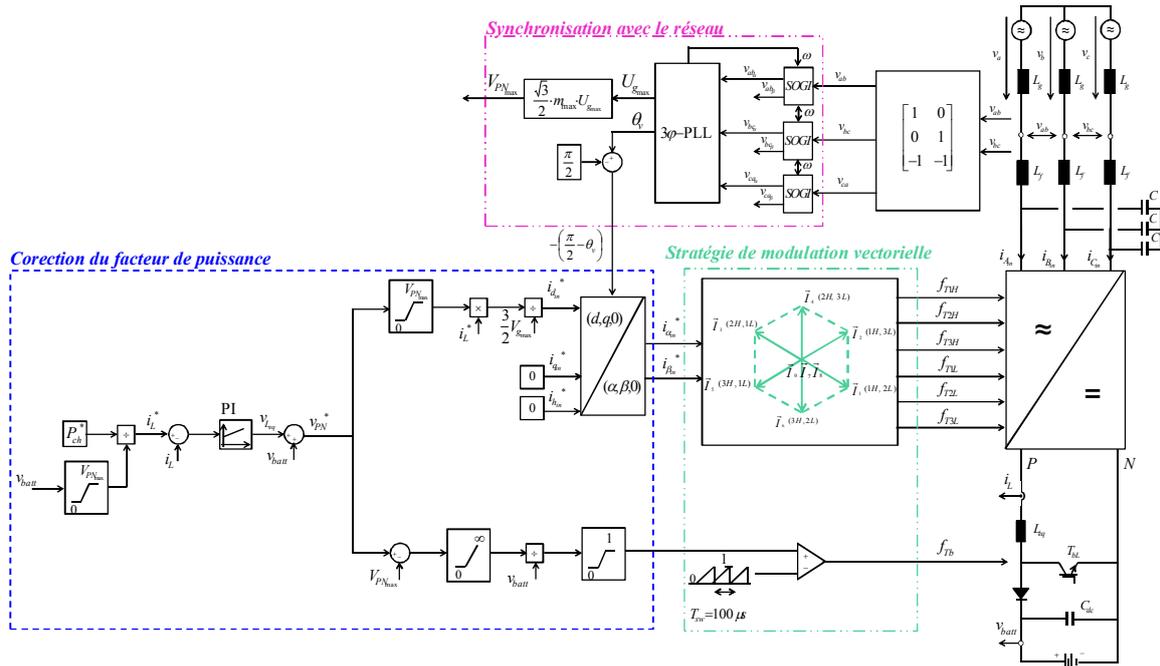


Fig.8. Loi de commande globale proposée pour la charge triphasée de la structure.

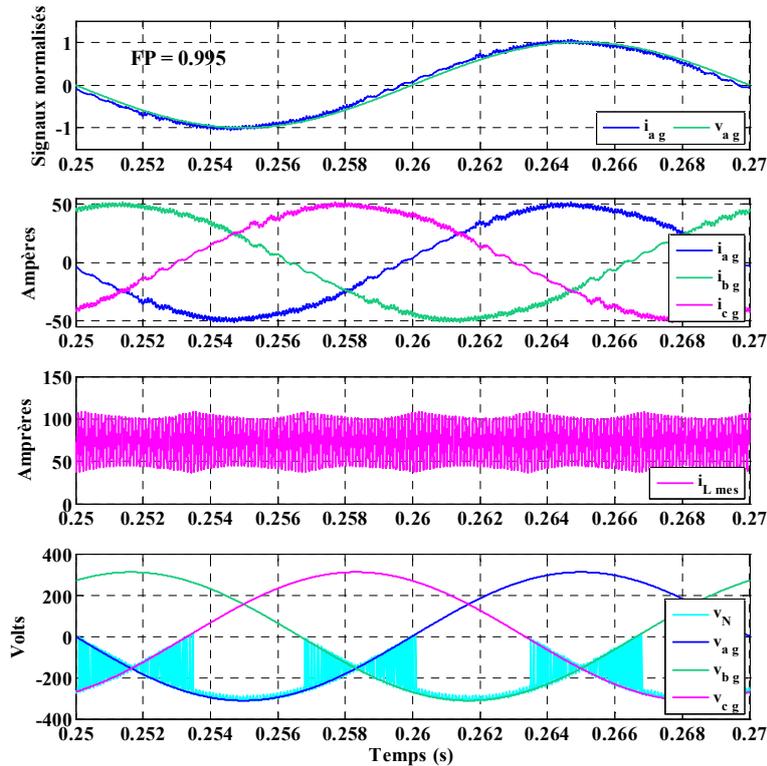


Fig.9. Formes d'onde obtenus avec la stratégie de modulation vectorielle proposée et la loi de commande développée pour le triphasé : les courants absorbés au réseau (i_{a_g} , i_{b_g} & i_{c_g}), le courant mesuré dans l'inductance du bus dc ($i_{L,mes}$), les tensions du réseau (v_{a_g} , v_{b_g} & v_{c_g}) et la tension entre le bus dc- et le châssis v_N .

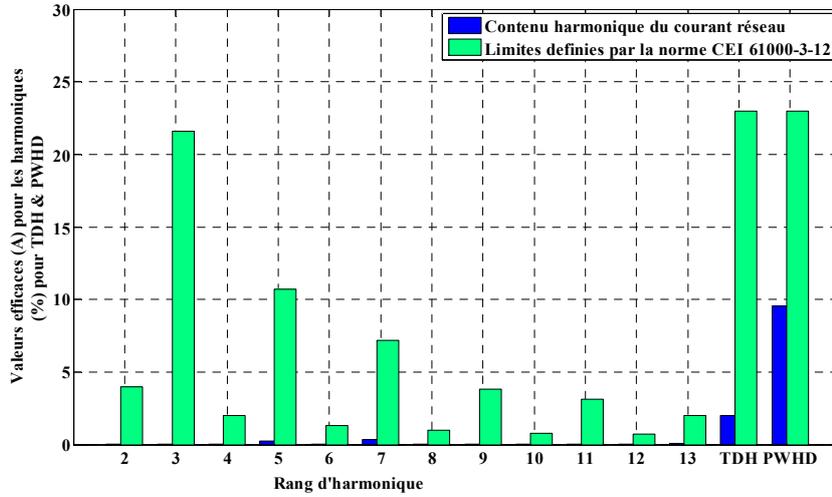


Fig.10. Conformité avec la norme CEI 61000-3-12 avec un taux de distorsion harmonique des courants absorbés au réseau inférieur à 5%.

■ *Développement, mise en œuvre et instrumentation de deux bancs expérimentaux exploités pour l'obtention des précédents résultats:*

- *Le premier banc est caractérisé par l'utilisation de semi-conducteurs (diodes et IGBTs) en Silicium avec une fréquence de découpage de 10 kHz.*

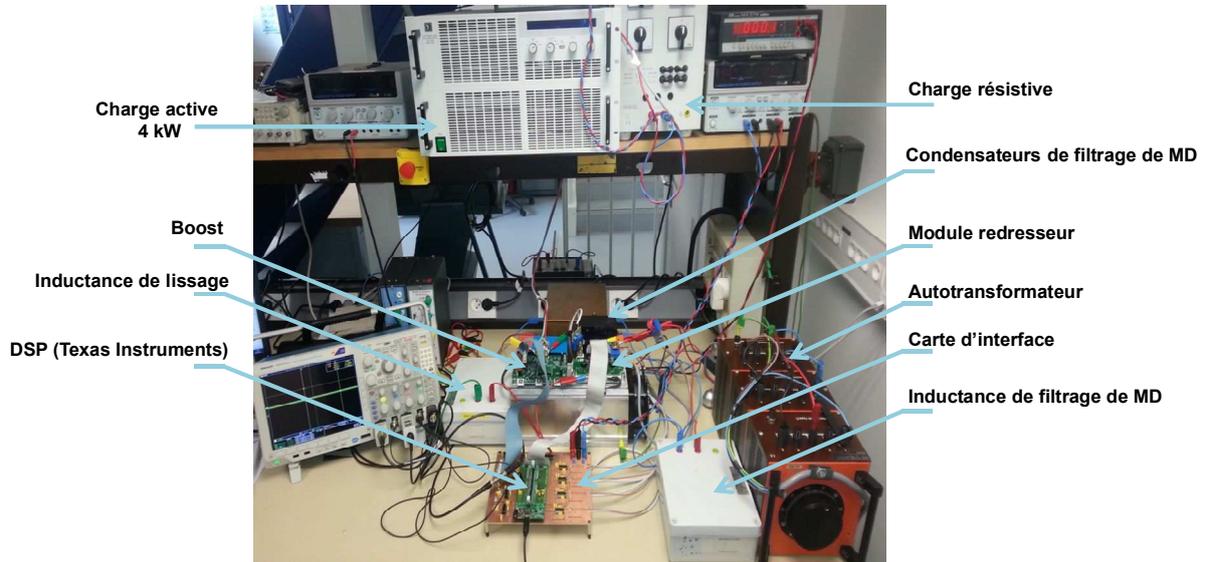


Fig.11. Premier banc expérimental monté au laboratoire SATIE (IGBT & fréquence découpage à 10 kHz).

- *Le second banc* est caractérisé par l'utilisation de semi-conducteurs (diodes et MOSFETs) en Carbone de Silicium avec une fréquence de découpage de 70 kHz.

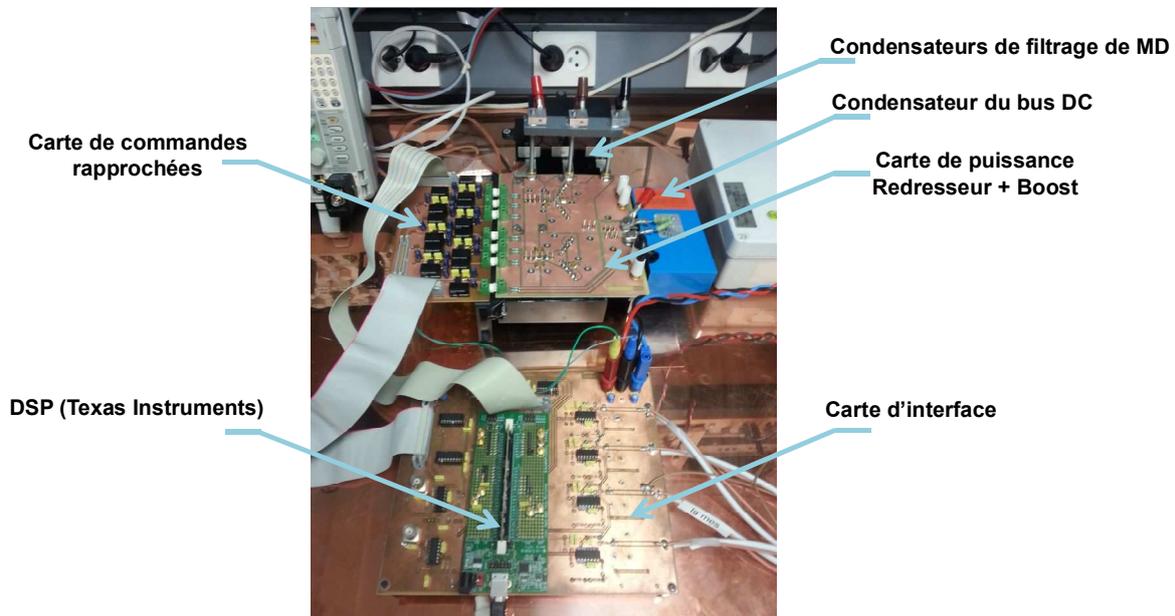


Fig.12. Second banc expérimental pour la montée en fréquence de découpage développé laboratoire SATIE (MOSFETs SiC & fréquence découpage à 70 kHz).

■ ***Proposition d'une approche de modélisation CEM de la structure qui tient compte du mode commun et du mode différentiel***

- Proposition d'une approche de modélisation spécifique des perturbations électromagnétiques conduites générés par les convertisseurs d'électronique de puissance regroupant les émissions de mode commun et de mode différentiel. Ce modèle permet d'estimer les émissions conduites en se basant uniquement sur les fonctions de modulation des semi-conducteurs. Il offre la possibilité de chaîner des modèles afin d'émuler le comportement CEM conduit d'une structure globale de conversion de puissance formée de plusieurs convertisseurs.
- L'approche est appliquée au chargeur non-isolé sous ses formes monophasée et triphasée. L'exemple du modèle CEM développé pour la structure monophasée (Fig.13) est présenté ci-dessous (Fig.14). Les simulations effectuées montrent la validité du modèle développé (Fig.15).
- Avantages : Ces modèles qui nécessitent des temps de calculs réduits peuvent être injectés dans des algorithmes d'optimisation pour le dimensionnement et la conception d'un filtre d'entrée dont nous cherchons par exemple à réduire le volume. En outre, ils permettent d'évaluer l'impact des modifications topologiques sur les fluctuations des potentiels aux différents nœuds internes à la structure.

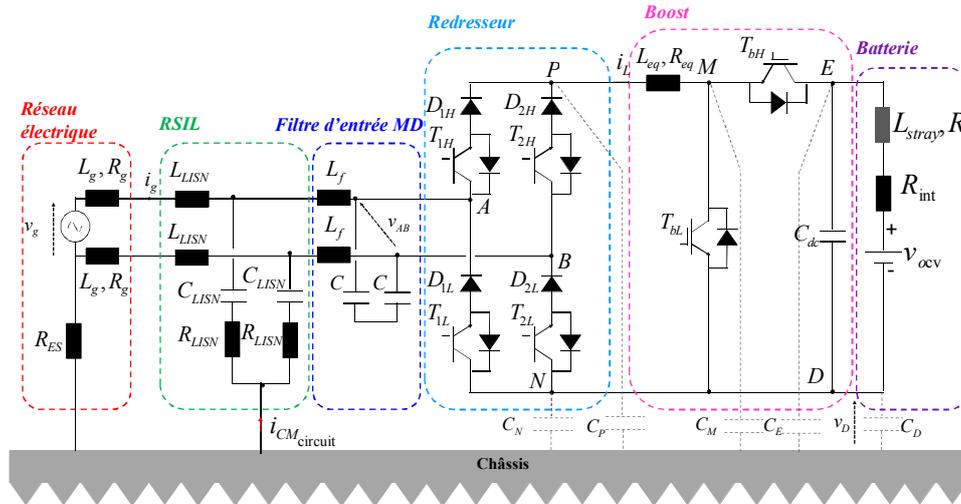


Fig.13. D'autres modifications qui pourraient être envisagées dans le but de réduire davantage les émissions conduites de mode commun surtout en triphasé.

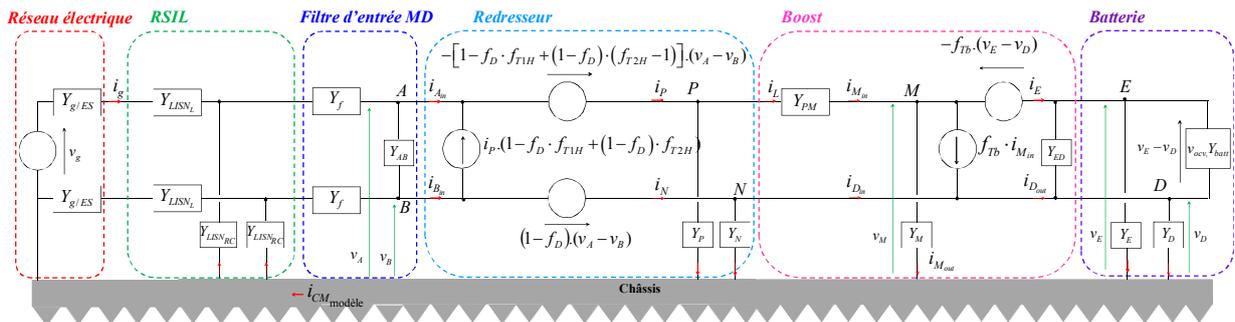


Fig.14. Modèle CEM de la structure de charge en monophasé qui tient compte des émissions conduites de mode commun et de mode différentiel.

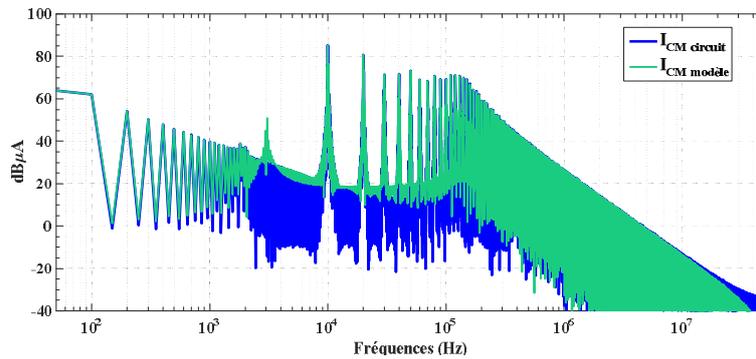


Fig.15. Analyse fréquentiel du contenu spectral du courant de mode commun i_{CM} . Circuit (bleue). Modèle (vert).

■ **Minimisations des émissions conduites (150 kHz – 30 MHz) :**

- Un résumé détaillé des solutions pour la réduction du mode commun, recueillies au niveau de la littérature qui pourraient éventuellement s'appliquer à la structure du chargeur étudié, est fourni.
- Des propositions de modifications topologiques applicables pour le monophasé et le triphasé sont présentés à la Fig.16. Il s'agit d'ajouter une diode de roue libre en sortie du redresseur, de diviser l'inductance additionnelle sur les deux bus dc et de placer une diode supplémentaire sur le chemin de retour du courant en sortie du Boost. Afin d'éviter toute interférence avec la chaîne de traction un relai est ajouté en parallèle avec cette diode pour la court-circuiter pendant la propulsion du VE.
- La contribution de chacune de ces modifications à la réduction des niveaux des émissions conduites est détaillée dans la thèse.
- Ces modifications structurelles ont été accompagnées par des modifications de la stratégie de modulation de la largeur d'impulsion en monophasé ainsi que la stratégie de modulation vectorielle en triphasé.

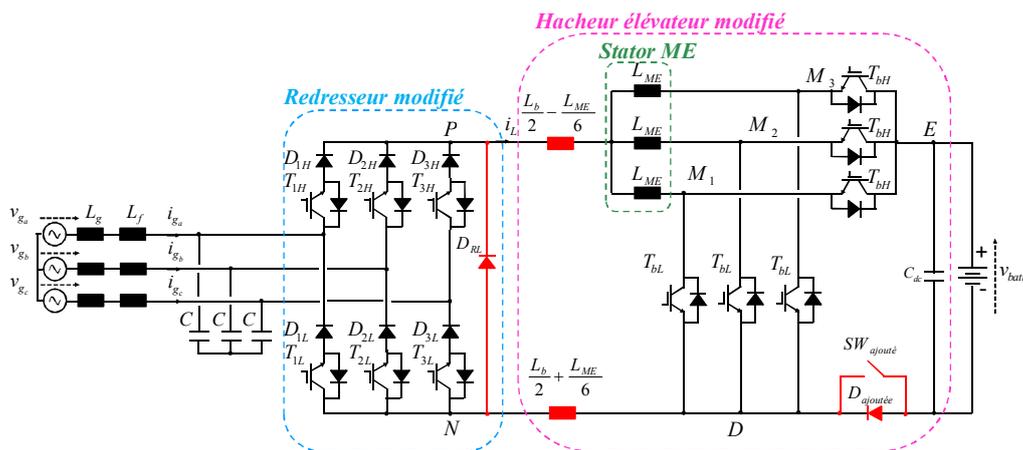


Fig.16. Les modifications topologiques effectuées afin de réduire les émissions de courants de mode commun.

■ **Perspectives:**

Ces travaux ont été effectués dans le but d'aboutir à la réduction des harmoniques basses fréquences et des émissions hautes fréquences afin de permettre la conception d'un nouveau filtre d'entrée moins volumineux et moins cher. Ainsi, des perspectives peuvent être dégagées parmi lesquelles nous pouvons citer :

- la définition de protocoles de mesure sur banc pour la validation expérimentale des modèles CEM proposés et la détermination de la plage de fréquences de validité ;
- l'approfondissement de l'approche de modélisation ;
- la conception et le choix des éléments du filtre CEM ;

- la validation expérimentale des lois de commande triphasées ;
- l'intégration d'autres modifications topologiques comme celles présentées à la Fig.17 surtout pour la réduction des émissions en triphasé.

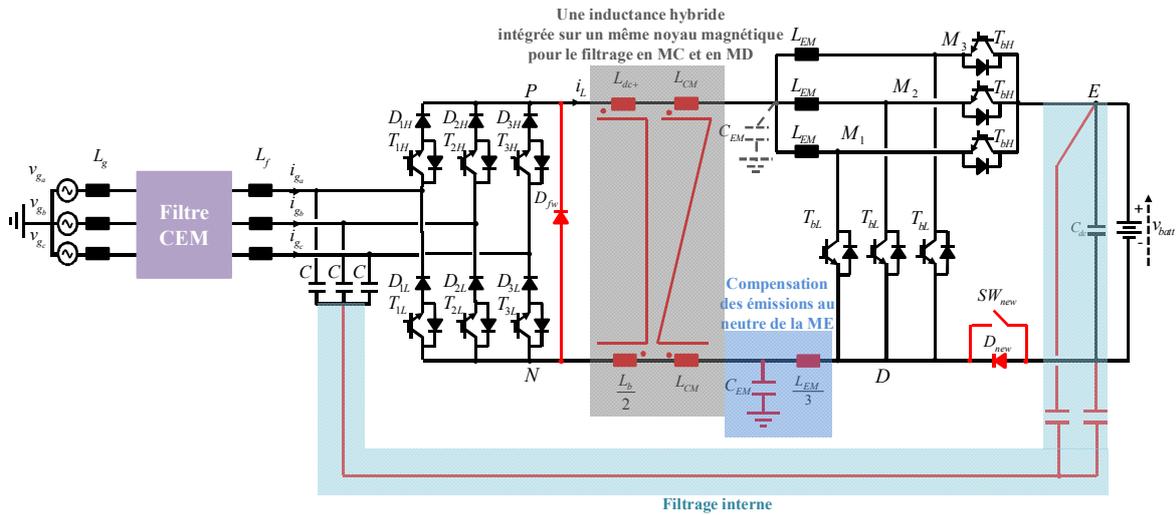


Fig.17. D'autres modifications qui pourraient être envisagées dans le but de réduire davantage les émissions conduites de mode commun surtout en triphasé.

En conclusion, les différents travaux liés à l'optimisation des émissions conduites de ce chargeur, menés au cours des trois dernières années, ont donné lieu aux huit publications suivantes :

Deux articles de revue

1. C. Saber, D. Labrousse, B. Revol & A. Gascher, « Challenges facing PFC of a single-phase on-board charger for electric vehicles based on a current source active rectifier input stage, » IEEE Transactions on Power Electronics, Vol. 31, N°: 9, Septembre 2016, DOI: 10.1109/TPEL.2015.2500958.
2. C. Saber, D. Labrousse, B. Revol & A. Gascher, « Power quality performance optimization of an integrated onboard battery charger for electric vehicles – PFC control for the single-phase charging configuration, » European Journal of Electrical Engineering, date de soumission: Mars 2017. ***Soumis, en attente d'acceptation.***

Deux articles de conférences internationales à comités de relecture

3. C. Saber, D. Labrousse, B. Revol & A. Gascher, « Achieving unity power factor with a unidirectional single-phase four reverse blocking IGBTs Buck-type rectifier, » Proceedings of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe), Mai 2015, Nuremberg, Allemagne.
4. C. Saber, D. Labrousse, B. Revol & A. Gascher, « Novel combined CM & DM conducted EMI modeling approach – Application to a non-isolated on-board single-phase charger for electric vehicles, » Symposium on Electromagnetic Compatibility (EMC Europe), Septembre 2017, Angers, France. ***Accepté.***

Deux articles de conférences nationales à comités de relecture

5. C. Saber, D. Labrousse, B. Revol & A. Gascher, « Correction du facteur de puissance d'un chargeur de batteries intégré aux véhicules électriques, » Symposium de Génie Electrique (SGE), Juin 2016, Grenoble, France.
6. C. Saber, D. Labrousse, B. Revol & A. Gascher, « Amélioration des émissions de courant harmonique d'un chargeur de batteries intégré aux véhicules électriques, » 18^{ème} Colloque International et Exposition sur la Compatibilité ElectroMagnétique (CEM), Juillet 2016, Rennes, France. Lien : <https://hal.archives-ouvertes.fr/hal-01361715/document>. ***Article primé.***

Deux Brevets

7. C. Saber, D. Labrousse, B. Revol & A. Gascher, « Procédé et dispositif de commande en monophasé d'un chargeur de véhicules à traction électrique ou hybride embarqué sans isolation galvanique, » Numéro de publication: FR1651967, cessionnaire d'origine: Renault S.A.S., le Cnam, le CNRS et l'ENS Paris Saclay, date de dépôt: Mars 2016, date de publication: x. ***Accepté par l'INPI.***
8. C. Saber, D. Labrousse, B. Revol & A. Gascher, « Dispositif et procédé de charge d'une batterie réduisant les courants de mode commun dudit dispositif, », cessionnaire d'origine: Renault S.A.S., le Cnam, le CNRS et l'ENS Paris Saclay, date de dépôt: Mars 2017. ***Soumis, en phase d'étude par l'INPI.***

List of Publications and Patents

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1. C. Saber, D. Labrousse, B. Revol & A. Gascher, « Challenges facing PFC of a single-phase on-board charger for electric vehicles based on a current source active rectifier input stage, » in IEEE Transactions on Power Electronics, Vol. 31, Issue: 9, September 2016, DOI: 10.1109/TPEL.2015.2500958.
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Two International Conference Papers With Peer Review

3. C. Saber, D. Labrousse, B. Revol & A. Gascher, « Achieving unity power factor with a unidirectional single-phase four reverse blocking IGBTs Buck-type rectifier, » in Proceedings of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe), May 2015, Nuremberg, Germany.
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6. C. Saber, D. Labrousse, B. Revol & A. Gascher, « Amélioration des émissions de courant harmonique d'un chargeur de batteries intégré aux véhicules électriques, » in 18^{ème} Colloque International et Exposition sur la Compatibilité ElectroMagnétique (CEM), July 2016, Rennes, France.

This article won the best paper award of the conference based on the participants' vote.

Two Patents

7. C. Saber, D. Labrousse, B. Revol & A. Gascher, « Procédé et dispositif de commande en monophasé d'un chargeur de véhicules à traction électrique ou hybride embarqué sans isolation galvanique, » publication number: FR1651967, assignee: Renault SAS, application date: 9 March 2016, publication date: x. *Accepted by INPI.*

8. C. Saber, D. Labrousse, B. Revol & A. Gascher, « Dispositif et procédé de charge d'une batterie réduisant les courants de mode commun dudit dispositif, » publication number: FR xxxxxxxx, assignee: Renault SAS, application date: March 2017, publication date : x. ***Under review.***

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ABSTRACT

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1. History of electric vehicles

1.1. Before the 21st Century : rise (1890s), fall (1920s) & rise again (1970s)

The early development of electric vehicles (EVs) is credited to European and American inventors. It goes back to 1828 when a Hungarian inventor, Ányos Jedlik, created a small-scale model car powered by an electric motor of his own design. Up until the 1840s, newly invented but non-rechargeable batteries were being used in the design of more practical and successful EVs. It was not until 1859 that the Frenchman Gaston Planté invented the first lead-acid rechargeable battery. The capacity of this storage battery was later improved by his fellow Frenchman Camille Faure in 1881; thus, transforming the lead-acid rechargeable batteries into a viable and practical means of storing electricity on-board of a vehicle. In the 1880s, French inventor Gustave Trouvé showcased a three-wheeled EV at the International Exhibition of Electricity in Paris, France, and Englishman Thomas Parker developed a working electric car illustrated in Fig.1 [Chan 2013].



Fig.1. Thomas Parker's electric car in 1884 [Chan 2013].

In the late 19th and early 20th centuries, France, England and the United States were great supporters of the widespread development of EVs. Therefore, several inventions followed leading to the 1900s. At that time, the French electric car manufacturer, Bouquet, Garcin & Schivre designed an EV that achieved the world's longest range record of almost 290 km per charge. Furthermore, the first vehicle to ever reach 100 km/h was an EV named the "Jamais Contente" which was equipped with Faure's lead-acid battery.

In the early 20th century, EVs presented several advantages over gasoline cars; among which, the reduced vibration, smell and noise as well as the ease of use since they did not require the change of gears while driving (at that time, the gear shifter was the most challenging part of the drive system). Furthermore, the distances of travel were limited due to the under-developed roads. Hence, EVs were able to accommodate daily needs on a single charge. This led to the development of the infrastructure such as, General Electric's charging station shown in Fig.2. Furthermore, the concept of exchanging the battery in order to increase the availability of EVs was first proposed in 1896. In 1897, EVs were being used for taxi services in New York City. The rise of EVs continued till the 1920s.

In the 1920s, the roads had been improved and connected different cities which required longer driving ranges. Furthermore, the discovery of the crude oil in Texas, the invention of the electric starter and the mass production of the Internal Combustion Engine (ICE) by Henry Ford transformed the vehicles with ICEs into affordable and efficiently produced cars. During this time period, the EVs started to be regarded as disadvantageous due to their limited driving range, their relatively low speed, low available power and their high cost compared to conventional vehicles.

The availability of oil contributed, around the early 1920s, to the fall of the EVs. These vehicles practically disappeared in the 1930s until their comeback in the 1970s following the oil crisis.

The deployment and the retraction of the EVs from the markets are mainly dictated by the fluctuations of the energy sector; especially, the cost of crude oil, its availability and the dependency on foreign countries in its procurement. If we add to that the 21st century's growing concerns regarding environmental protection and energy conservation, the EVs new rise becomes inevitable.



Fig.2. A General Electric charging station with a Baker EV in the early 1900s [Chan 2013].

1.2. 21st Century's environmental, economic & social concerns

The recent development of electric power trains (electric machines, electric storage systems, power electronics, digital controls...) and the deployment of electric plug-in vehicles are mainly due to growing environmental, economic and social concerns [Chan 2002].

Air pollution, climate change and ozone depletion constitute the major challenges facing sustainable development. On a global level, studies conducted in 2007 show that the transportation industry was solely responsible for 13% of the total greenhouse gas emissions registered in 2004 and contributed up to 17% in the carbon dioxide emissions [IPCC 2007]. On a national level, the transportation sector in France was solely responsible for the majority (33%) of the carbon dioxide emissions in 2008 along with an overwhelming contribution (93%), seen in Fig.3, of the road transportation industry [MEEM 2011].

The gravity of the environmental impact due to the road transport sector forced automobile manufacturers to search for more efficient and ecological solutions. In France, the importance of re-introducing EVs for the protection of the environment was the subject of a report submitted by Senator Pierre Lafitte in 1993 to the National Assembly which was adopted by the Parliamentary Office for the

Evaluation of Scientific and Technological Choices [Laffitte 1993]. Therefore, since the early 21st century, electric power trains and electric vehicles (EV) became true contenders in the race towards achieving sustainable development and reducing the vehicle's carbon footprint.

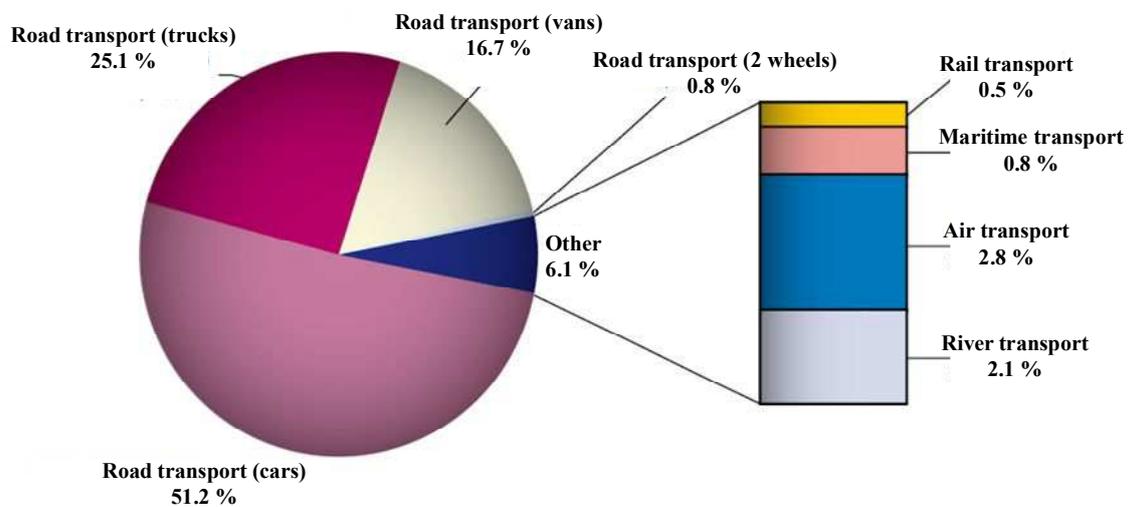


Fig.3. CO₂ emissions by mode of transport in metropolitan France (percentages from a total of 126.4 Mt CO₂ emissions in 2008) [MEEM 2011].

On the other hand, the European Union (EU) is also keen on reducing its energy dependency on foreign countries as well as its external investments in the procurement of foreign gas and oil. Therefore, the EU defined three objectives to be reached by 2020:

- Reducing greenhouse gas emissions by at least 20% compared with the levels scored in 1990
- Increasing the share of renewable energies in the final energy consumption to 20%
- Increasing the energy efficiency by 20%

These climate and energy targets are interrelated and their repercussions on the road transportation industry have led to the exponential growth of the research and development in the field of EVs. The objective set is to reduce the vehicles' emissions from 164.9 gCO₂/km in 2007 to just 95 gCO₂/km in 2020.

Moreover, the development of the Lithium-ion technology, from the 1970s till the first working prototype in the 1980s, was a major technological breakthrough that encouraged the research in the field of EVs.

This time around it seems that EVs are here to stay. They are being considered along with their adequate infrastructure and their impact on power grids. Their deployment is facilitated by the will of the public authorities to defend their use amongst the consumers. For instance, the United Nations organized a climate summit, the Cop 21, which took place in Paris in 2015. The governments of more than 190 nations gathered to discuss a possible new global agreement on climate change that goes beyond 2020. It aimed at reducing global greenhouse gas emissions and promoting the need for more renewable and clean energies in order to avoid the threat of a dangerous climate change.

In fact, the constant increase in the production of renewable energies is a key factor for the development of EVs. In this case, the EVs can be recharged with zero emissions and can be used to

store the energy of wind turbines or photovoltaic panels. Therefore, the future trends in EVs include the use of the cars as regenerative mobile energy storage systems for the grids through vehicle to grid operations as well as the use of EVs to supply the users' homes (and eventually businesses) with the energy stored in the battery through vehicle to home operations. For instance, by slow charging the EV at night, when there is an overflow of electricity, then using that stored energy as the daytime power source for the household, the system helps alleviate consumption of power in peak periods when the demand is at its highest. Furthermore, it can be considered as a backup power supply for emergencies.

The constant technological developments have led to more sophisticated electric vehicles (Fig.4) being sold and deployed especially in Europe, Japan and the USA. Nonetheless, in order for the EVs to reach the ease of use of conventional vehicles, efforts must be made to reduce the recharge time, to increase the driving range of the vehicle and to ensure the charging availability for the users. Hence, the charging of the on-board battery remains as one of the more challenging and most important features of an EV.



Fig.4. Groupe Renault's range of 100% electric vehicles (from left to right): Twizy an urban quadricycle, ZOE a compact city car, Kangoo a "zero emissions" van and Master a "zero emissions" large van.

2. Overview of chargers for electric vehicles

Transportation electrification is environmental friendly, efficient and presents good performances [Chan et al. 1997]. However, compared to mechanical drives, several key issues need to be addressed among which: the achievable driving range, the relatively long recharge time, the deployment of the adequate infrastructure, the significant impact on utilities and grids and the cost of the battery [Sarlioglu et al. 2017]. According to a batteries’ prices survey conducted by Bloomberg New Energy Finance, the cost of the batteries went down from 599 \$/kWh in 2013 (distributed as such: 411\$/kWh for the cells and 188 \$/kWh for the pack) to 273 \$/kWh in 2016 (199 \$/kWh for the cells and 74 \$/kWh for the pack). The decrease in the cost of the batteries is mainly due to constant advances in terms of chemistry and mechanical packaging of the cells and modules. It should be noted that at the moment Tesla is driving the market with its Gigafactory in Reno where the components of its storage units, that have the highest specific energy of the market at 233 Wh/kg, are being built in partnership with Panasonic [Anderman 2014]. Nonetheless, the total cost of the battery remains high compared to the price of a fuel tank in a conventional vehicle.

2.1. On-board of the EV or off-board

Several possibilities exist for increasing the EV’s driving range. The capacity of the battery can be increased or the availability of the charge can be enhanced by reducing the charging time. The latter suggests an increase of the charging power. Nevertheless, the infrastructure dedicated for conductive fast charging (for which the ac-dc converter is incorporated to the charging station) is still limited [Williamson et al. 2015]-[Shi et al. 2017]; therefore, considerable progress is made by placing the ac-dc charger on-board of the EV. Off-board chargers are not constrained by size or weight but introduce additional cost to the infrastructure through the deployment of a high number of charging stations. In order to meet the needs of EV users in terms of the charging availability, on-board chargers that achieve ac/dc conversion are retained. An example of an on-board and an off-board charging system is illustrated in Fig.5. A detailed review of battery charging topologies, charging power levels and infrastructure for plug-in electric and hybrid vehicles can be found in [Yilmaz et al. 2013].

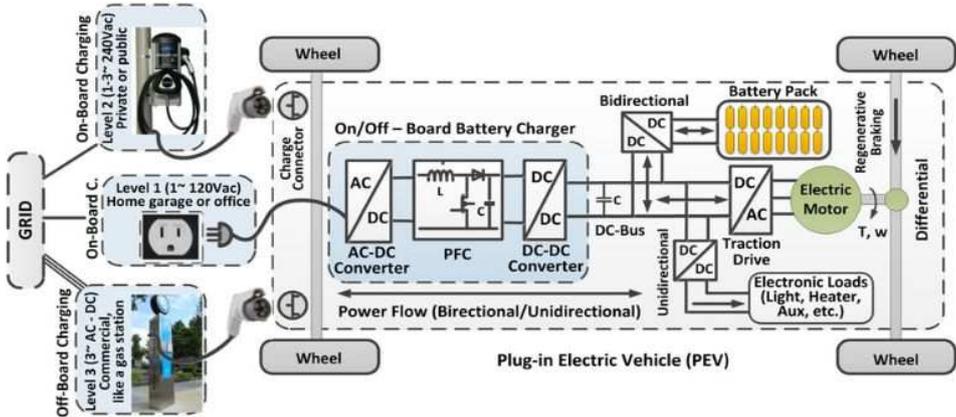


Fig.5. Example of on/off-board charging systems and power levels for EVs [Yilmaz et al. 2013].

2.2. Stand-alone or integrated to the traction’s powertrain

Furthermore, on-board structures are either stand-alone or integrated to the vehicle’s power train. This means that parts of the electric traction power train (i.e. the electric machine windings and/or the

traction’s inverter) are re-used for charging. On-board integrated converters increase the charging availability by allowing to charge from any ac power outlet while reducing the size and the cost of the charger [Haghbin et al. 2013]. Various integrated on-board charger topologies have been studied with regards to different drive systems [Sakr 2016]. A summary is given in Fig.6. Moreover, [Subotic et al. 2016] present an overview of fast on-board integrated battery chargers for electric vehicles based on multiphase machines and power electronics.

2.3. Galvanically isolated or non-isolated from the grid

Moreover, the on-board integrated fast chargers are typically galvanically non-isolated from the grid to avoid the increase of the volume and the cost of the charger for the high charging powers. An isolated solution is presented in [Subotic et al. 2016]; however, the isolation is located on the grid-side (off-board of the EV). This requires the deployment of adequate charging stations. Disadvantages of the on-board integrated non-isolated fast chargers include electromagnetic compatibility issues (grid current harmonics and ground frame leakage currents) and complex control schemes. These problems are less obvious for slow chargers because they mainly present galvanic isolation from the grid and do not use the electric machine’s (EM’s) windings as filtering inductors.

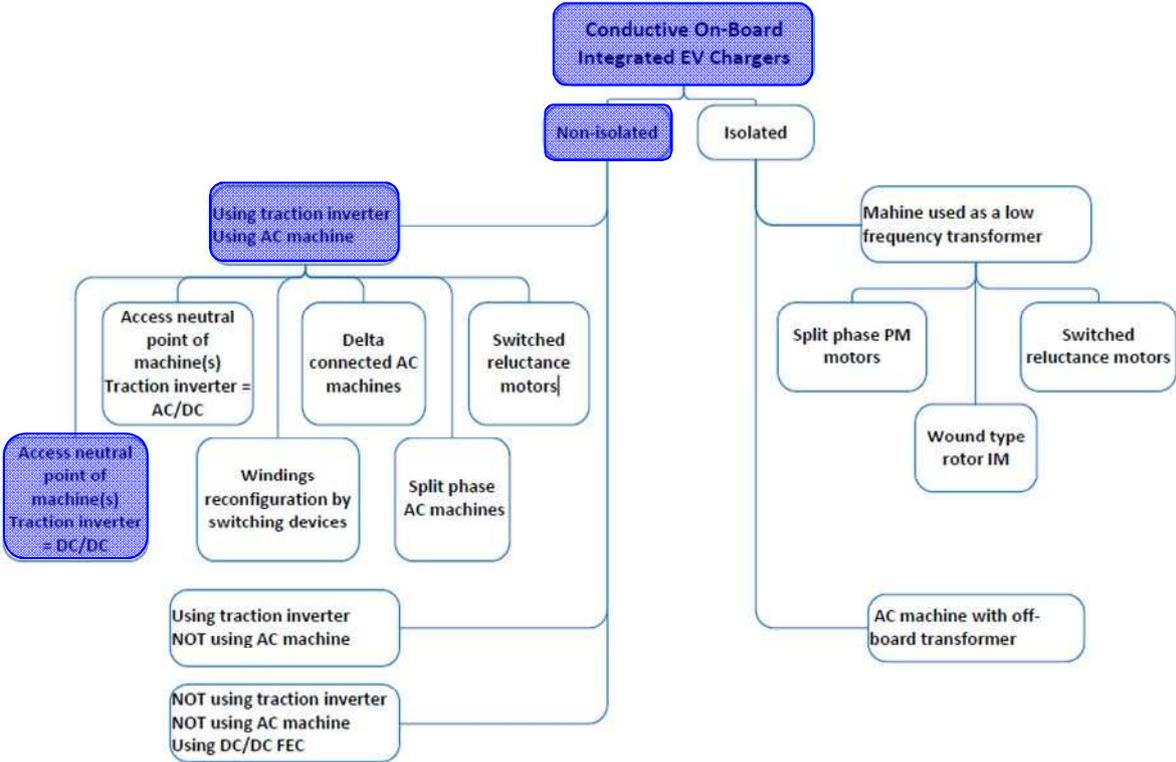


Fig.6. Classification of on-board integrated chargers for EVs according to the drive system. Classification according to whether or not the traction inverter and/or the electric machine’s windings are used for charging. [Sakr et al. 2014]. The highlighted categories are the ones that correspond to the charging system studied throughout this thesis.

2.3.2. Examples of isolated chargers

❖ Nissan Leaf

In the case of the Nissan Leaf, the on-board stand-alone charger is isolated from the grid [Yoshimoto 2014]. Fig.7 shows the mechanical packaging of the charger as well as the associated topology. It consists of a Boost power factor correction input stage followed by an inverter. The output of the inverter is galvanically isolated from the output of the charger via a transformer with two secondary windings. Each secondary winding supplies a diode rectifier. The output voltages of these rectifiers are summed to form the dc output of the charger. Fig.8 shows the technical aspects of the charger that can ensure a slow single-phase charge of 3.6 kW and up to 6.6 kW. A separate dc-dc junction box is used for the 50 kW fast charging using the Chademo power outlet.

❖ BMW i3

BMW's electric vehicle "i3" is equipped with an isolated on-board charger. The mechanical packaging, internal dispositions and technologies are shown in Fig.9. This charger can accommodate 3.7 kW, 7.4 kW and 11 kW charging. An optional dc-dc fast charger (50 kW) can be bought with the EV.

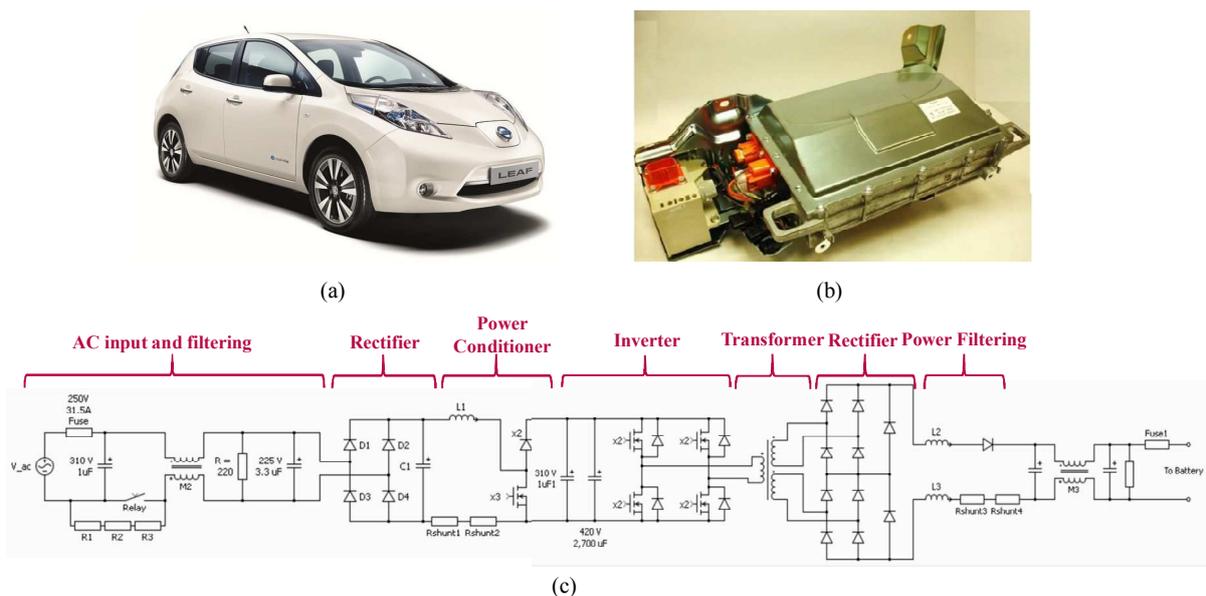


Fig. 7. (a) 2013 Nissan Leaf. (b) Mechanical packaging of the charger. (c) Topology of the isolated charger. [Burruss 2014]

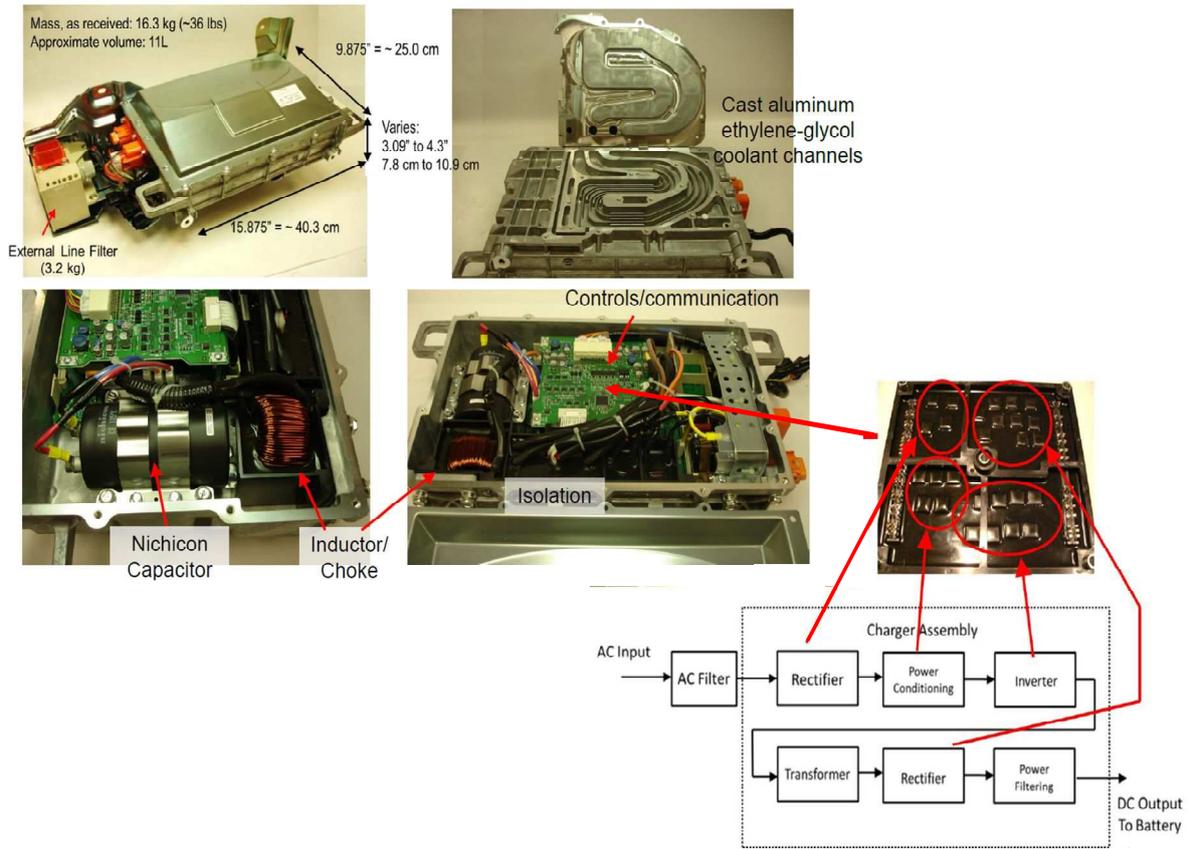


Fig.8. Internal components of the Nissan Leaf isolated on-board charger. [Burruss 2014]

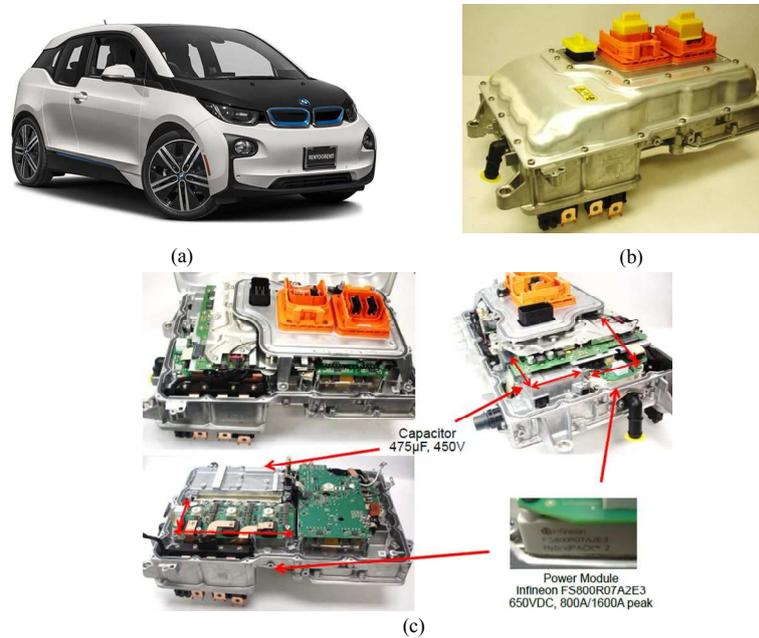


Fig.9. (a) 2016 BMW i3. (b) Mechanical packaging of the charger. (c) Internal components. [Burruss 2016]

2.3.3. *Examples of non-isolated chargers*

❖ BYD

The BYD charger is an on-board integrated non-isolated charger by Build Your Dreams (BYD) [BYD 2012]. It equips BYD's EV 'the e6' shown in Fig.10 (a). It uses the traction's regenerative voltage source inverter as a three-phase Boost power factor correction (PFC) converter during charging. However, the electric machine's windings are not used during charging but rather disconnected using relays (Fig.10). Since the charger needs to accommodate a wide input voltage range, a dc-dc Buck converter is activated, at the output of the PFC, to ensure voltage step down capabilities when needed.

❖ SOFRACI

SOFRACI stands for a high efficiency inverter with a built-in charger. It is a project developed by the French automotive supplier Valeo [De Sousa 2010]. This project aims to develop a power conversion system that allows the propulsion and the recharge of an electric vehicle while optimizing the use of all the elements of the power train. The proposed system makes use of the permanent magnet synchronous machine's windings during charging and does not require any type of reconfiguration (absence of relays) between the traction and the recharge operations. Furthermore, the structure presented in Fig.11 is suitable for any types of power supply networks (single-phase and three-phase).

In order to recharge the battery, it is possible to use the power electronics structure as an ac-dc converter to rectify the currents and the mains' voltages. In this mode of operation, the electric machine's windings are used as filtering inductors. The output dc-dc Buck-type converter adapts the voltage level delivered by the rectifier to that of the batteries.

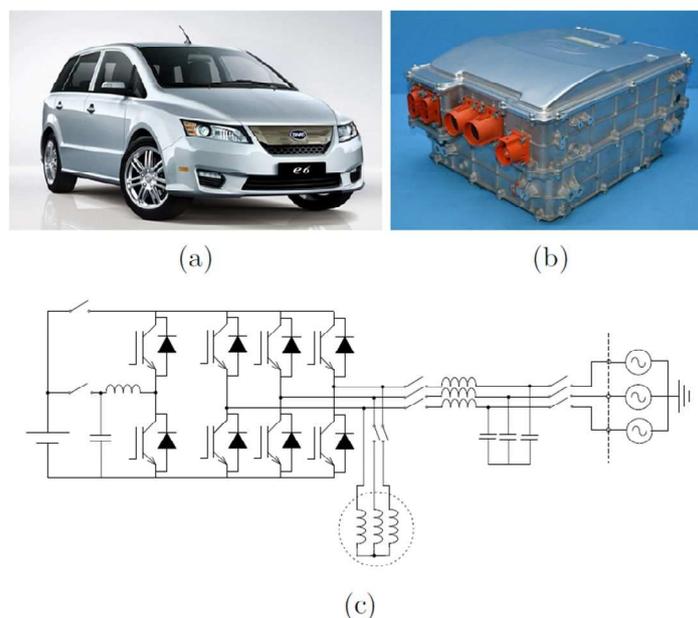


Fig.10. (a) 2015 BYD's e6 EV. (b) Mechanical packaging of the BYD charger. (c) Topology of the BYD charger. [Sakr 2016]

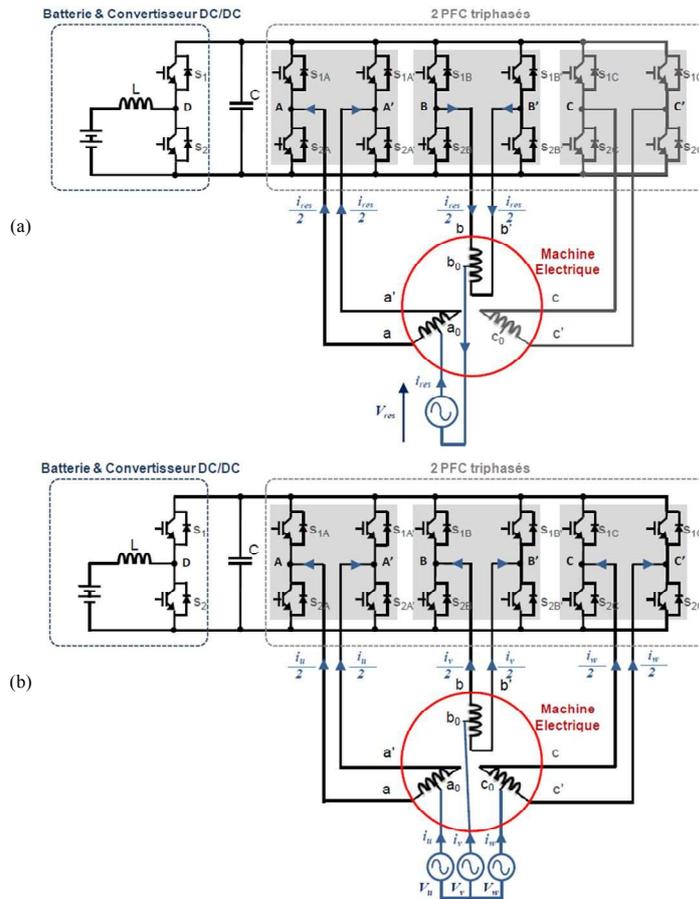


Fig.11. Power conversion structure of the SOFRACI project. (a) Single-phase charging configuration. (b) Three-phase charging configuration. [Lacroix 2013]

❖ Renault Zoe

The Renault Zoe is equipped with the Chameleon charger [Loudot 2010]. It is an on-board integrated non-isolated charger. It uses both the traction inverter and the electric machine's windings during charging. It is called a Chameleon because of its capability to adapt to both single-phase residential slow charging (3.7 kW and 7.4 kW) and three-phase fast charging (11 kW, 22 kW and 43 kW) using public charging stations.

The structure of the charger and its mechanical packaging are shown in Fig.12. It consists of a Buck-type rectifier input stage that accesses the neutral point of the electric machine's windings. These windings form the filtering inductors for the traction inverter used as a three-legged dc-dc Boost output stage. Thus, giving it the capability to both step-up and step-down the grid's voltage.

The charger considered throughout this study is based on a similar structure and will be detailed throughout this study.

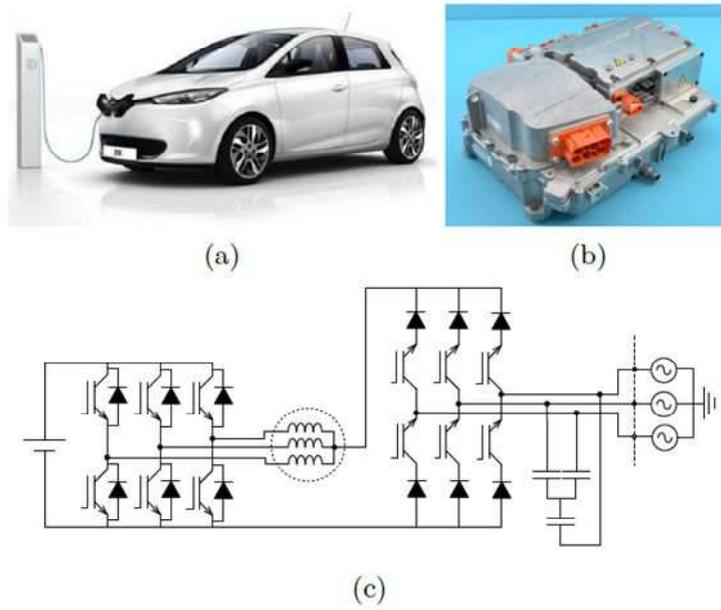


Fig.12. (a) 2013 Renault Zoe ZE. (b) Mechanical packaging of the chameleon charger. (c) chameleon topology: it accesses the electric machine's neutral point via a three-phase Buck-type rectifier and uses the traction inverter as a dc-dc Boost converter. [Sakr 2016]

3. Industrial specifications

Table 1 resumes the possible charging configurations along with the currents absorbed at the grid-side for a 22 kWh Lithium-ion battery. This study focuses on the single-phase residential slow charging rated at 1.8 kW to 7.4 kW as well as the three-phase fast charging rated at 11 kW, 22 kW and 43 kW.

Among the criteria that influence the charging system's characteristics we can cite:

- A limited driving range (120 - 150 km): The need for a well distributed infrastructure.
- The increase of the charging availability: The need to ensure both single-phase and three-phase charging.
- The diversity of the markets, the grids' frequency & voltage levels and the earthing systems where EVs are sold: The need for a "universal charger".
- The reduction of the size, the weight and the cost of the chargers (so that EVs can become competitive with conventional vehicles): The need to re-use parts of the traction power train to ensure the charge as well as the use of non-isolated chargers for high power fast charging.

Table 1. DIFFERENT CHARGING CONFIGURATIONS FOR A LITHIUM-ION BATTERY WITH AN ENERGY CAPACITY OF 22 KWH

Recharge time for a complete state of charge (100%)	Power Supply	Charging Power	Grid Voltage Level (RMS) in France	Input Current Level (RMS)	
6 – 8 h	AC single-phase	3.7 kW	230 V	16 A	Residential charging stations
3 – 4 h	AC single-phase	7.4 kW	230 V	32 A	
2 – 2h 30	AC three-phase	11 kW	400 V	16 A/phase	Public charging stations
1 – 1h 30	AC three-phase	22 kW	400 V	32 A/phase	
20 – 30 min	AC three-phase	43 kW	400 V	63 A/phase	Lack of a dedicated infrastructure
20 – 30 min	DC supply	50 kW	400 Vdc	100 Adc	High cost of the infrastructure (off-board chargers)

Therefore, the studied charging system's specifications can be defined:

- An AC/DC charger;
- non-isolated from the grid;
- placed on-board of the vehicle;
- integrated to the traction power train;
- ensures single-phase residential slow charging;
- & three-phase fast-charging using public charging stations.

4. Description of the studied charger

EVs are deployed in countries with different grid voltage levels which makes it indispensable for the battery chargers to accommodate a wide input voltage range. Table 2 shows the grid voltage levels for various countries [IEC 2017]. It should be noted that an EV's battery is rated between 250V and 430 V, depending on the project.

For this study, the Renault Zoe's first generation Lithium-ion battery is considered. The main supplier is LG Chem providing a blend of Nickel-Manganese-Cobalt with Lithium-Manganese oxide (NMC-LMO) at the cathode and a graphite-based anode. It is formed by 192 Lithium-ion cells and 12 modules (16 cells per module) configured according to 96S2P (i.e. the battery is formed by 2 sets that contain, each, 96 cells placed in series and the sets are connected in parallel between them). Each cell has a nominal capacity of around 36 Ah. The available / usable energy of the battery is rated around 22 kWh (it has since been increased in newer generations to 23.3 kWh and 45 kWh). In addition, the battery presents a nominal voltage of 360 V with a voltage variation of roughly 270V for a typical end-of-discharge and 400V at the end-of-charge.

By comparing the battery's voltage levels with those of the countries' grids, it can be deduced that the charger needs to be able to step-up as well as step-down the input voltage. This is achieved by using two types of converters: a Buck-type and a Boost-type converter.

Table 2. ELECTRICAL CHARACTERISTICS OF THE GRIDS IN THE COUNTRIES AND TERRITORIES OF THE MAIN MARKETS OF THE GROUPE RENAULT

Country / Territory	Grid Voltage Level (RMS)	Grid Frequency
France – Germany – Spain – Italy – UK- Belgium – Luxembourg – India - Algeria	230 V	50 Hz
Brazil	127 V / 220 V Depending on the state	60 Hz
Morocco	127 V / 220 V Depending on the state	50 Hz
Turkey – Russia – Argentina - Iran	220 V	50 Hz
Republic of Korea	220 V	60 Hz
United States of America	120 V	60 Hz

The traction and the charging power trains of the studied vehicle are shown in Fig.13. The synchronous electric motor (7) (50-70 kW) comprises of a stator, a wound rotor, a power electronics controller (that ensures the communication between the engine's electronics and external elements such as the battery, the driver's inputs...) and a reducer with a fixed reduction ratio (it replaces the gearbox in a conventional vehicle). It is illustrated in Fig.14. The junction box (5) includes the input filter as well as relays that ensure the reconfiguration of the input stage to guarantee fast charging. It is

the input of a power electronics bloc (6) that includes an ac/dc rectifier, a three-phase two level inverter that supplies the wound rotor synchronous machine as well as a dc-dc converter for the supply of the low voltage (14V) network (refer to Fig.15). The charger and the inverter are both connected to the electric machine or to parts of it.

The vehicle's charger was initially designed to charge the battery from a 3.7kW/16A home charging wallbox in eight hours, or an hour by visiting a 22kW/32A three phase charging station, or just 30 minutes from a 43kW/63A charging station.

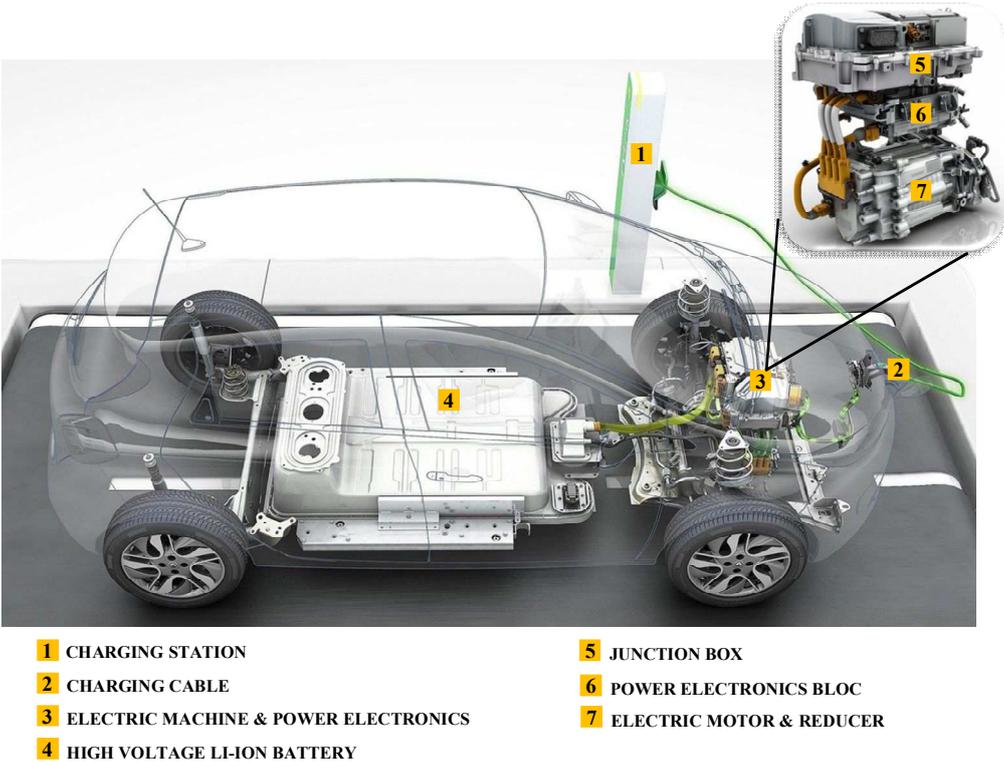


Fig.13. Traction and charging power trains on-board of Renault’s electric vehicle: ZOE.



Fig.14. The electric motor & reducer of Renault’s pure electric vehicle: ZOE.

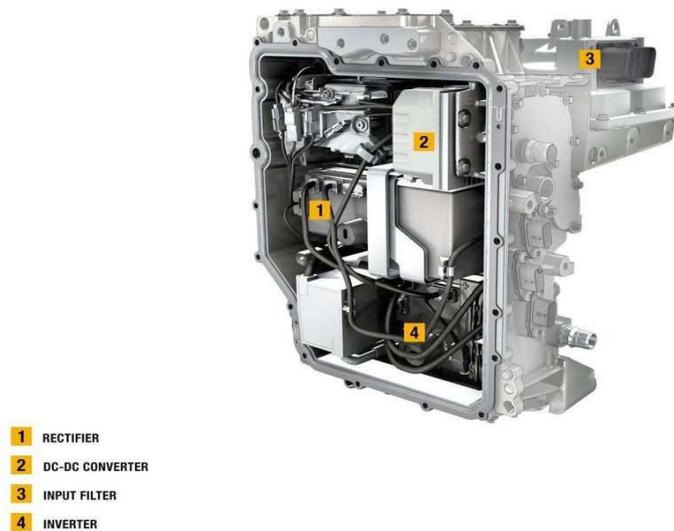


Fig. 15. The on-board power electronics bloc of Renault’s pure electric vehicle: ZOE.

Based on the above description, the charger is an ac/dc on-board integrated non-isolated charger for EVs that can accommodate 22kW or 43 kW three-phase fast charging (see Fig.16) as well as 1.8 to 7.2kW single-phase residential charging (see Fig.17). Since this study is conducted for the automotive industry, cost, size, and security requirements related to these types of chargers constitute major design constraints. Cost and size reductions are achieved through the integration of the traction inverter as well as the electric machine windings into the charging power circuit as shown in Fig.16. Furthermore, the charger was originally designed according to an irreversible specification. In fact, the input stage of the charger is a current unidirectional rectifier.

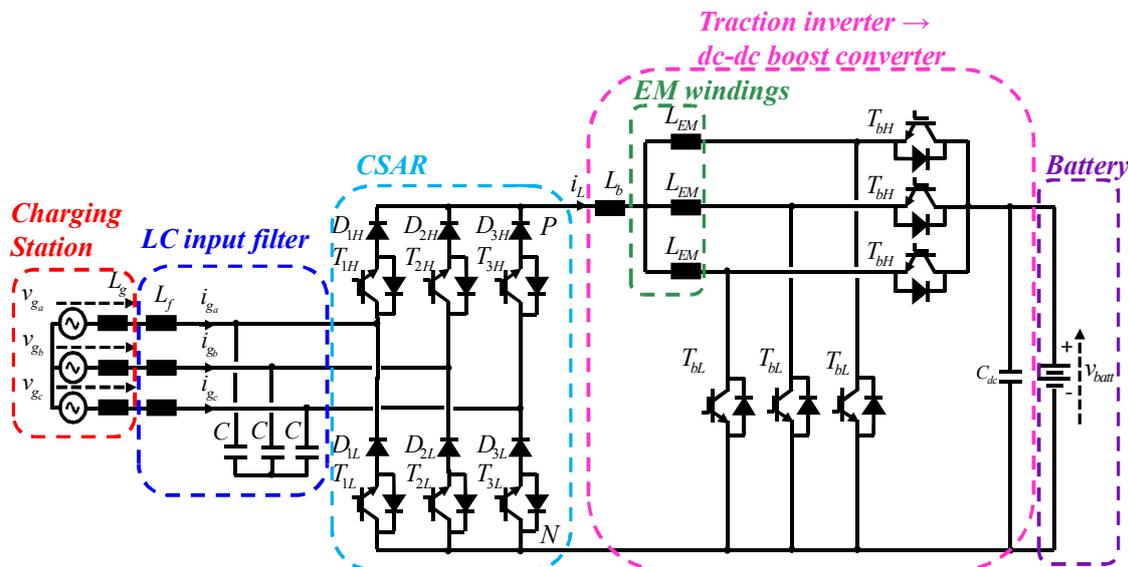


Fig. 16. The on-board integrated non-isolated charger’s three-phase configuration.

The output stage re-uses the synchronous machine’s windings as well as the traction’s regenerative inverter to form a dc-dc Boost converter for charging. Usually, an interleaved boost control presents

several advantages among which a better distribution of the thermal losses, higher system reliability, and reduction of the ripple on the input as well as the output signals of the converter [Wang 2009]. However, integrated chargers must not develop unwanted torque and vibration in the motor during charging therefore; the inverter's legs are chosen to be synchronously controlled to form the equivalent of a boost converter. This yields a dc/dc voltage step-up output stage Fig.17.

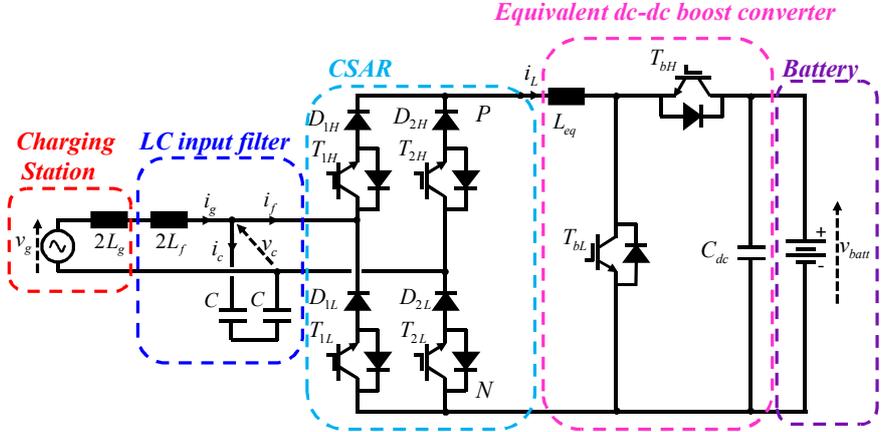


Fig.17. Simplified on-board integrated non-isolated charger for a single-phase configuration with an equivalent dc-dc Boost output stage.

In order to accommodate a wide input voltage range and a varying dc voltage output, the input stage of the converter is a current source active rectifier (CSAR) with voltage step-down capability. It consists of six insulated-gate bipolar transistors (IGBTs) placed in series with six diodes in order to ensure reverse blocking capabilities (Fig.16). Despite their challenging control structures compared to voltage source topologies, current source rectifiers present major security advantages because of their capability of limiting the inrush currents, when the input filtering capacitor is small enough, as well as the dc short-circuit currents [Pires et al. 2016]. They have been widely employed for telecommunications and ac drives [Baumann et al. 2005]-[Wu 2006]. The rectifier used is non-regenerative; however, bidirectional CSAR topologies exist [Rodriguez et al. 2005]-[Soeiro et al. 2013]-[Singh et al. 2004] and [Singh et al. 2003]. Their use would allow vehicle-to-grid operation and smart grid management.

5. Key points to be studied

The topology of the charger is imposed; as such, it will not be challenged throughout this study. However, the main objective of this work is to investigate areas of possible improvement, propose minimal cost solutions and implement new control and topological modifications (minimalistic changes to reduce costs) in order to optimize both the single-phase and the three-phase operation of the charger.

5.1. General points related to non-isolated chargers

5.1.1. *Safety*

On-board chargers share their high-voltage battery's connections with the on-board electronics meant for the ventilation and air conditioning, the 14V power system and other low voltage consumers. This means that the lumped stray capacitance between the negative rail of the high-voltage battery and the frame ground includes the parasitic capacitances of all the systems sharing the battery's dc rails. The value of this parasitic capacitance is dominant (higher than 10 nF) compared to the stray capacitance of a power electronics module. The stray capacitance of an IGBT being rated around 100 pF.

Therefore, the fluctuation of the voltage across this capacitance needs to be minimized; otherwise, high leakage currents could flow towards the chassis. If the high frequency components of the leakage currents are too high, one of two things may happen. The residual current protective devices (RCD) may nuisance trip or it may be blinded. Any event that can cause blinding of an RCD is a huge risk to the user. Therefore, the IEC 61851-21 safety standard specifies that the touch current should not exceed 3.5 mA RMS.

5.1.2. *Electromagnetic Compatibility*

Passive filtering along the propagation path has always been the go-to solution for power electronics designers. Once the prototype is built, a series of emission levels' measurements are conducted and compared to the levels recommended by the standards. The attenuations needed are then used to design an input/output EMI filter for the already-built converter. However, since the reduction of the conducted emissions was not taken into account during the design process, the attenuation levels needed are often high.

Furthermore, the standards limit the maximum value of capacitances for the line to ground capacitors used to filter the common mode (CM) currents. Therefore, in order to achieve the high attenuation levels required with this limitation, the filtering inductors' values increase and lead to a bulky and costly filter usually consisting of multiple filtering stages.

The inductive part (i.e. the CM and the DM inductors) of the input EMI filter is shown in Fig.18 (a). If we add to that the Y-capacitors and the DM capacitors (component n°1 in Fig.18 (b)), the filter's volume and cost increase. Consequently, the switch control laws of the charger need to be designed in order to reduce the common mode emissions so that the EMI analysis can take part of the design process.

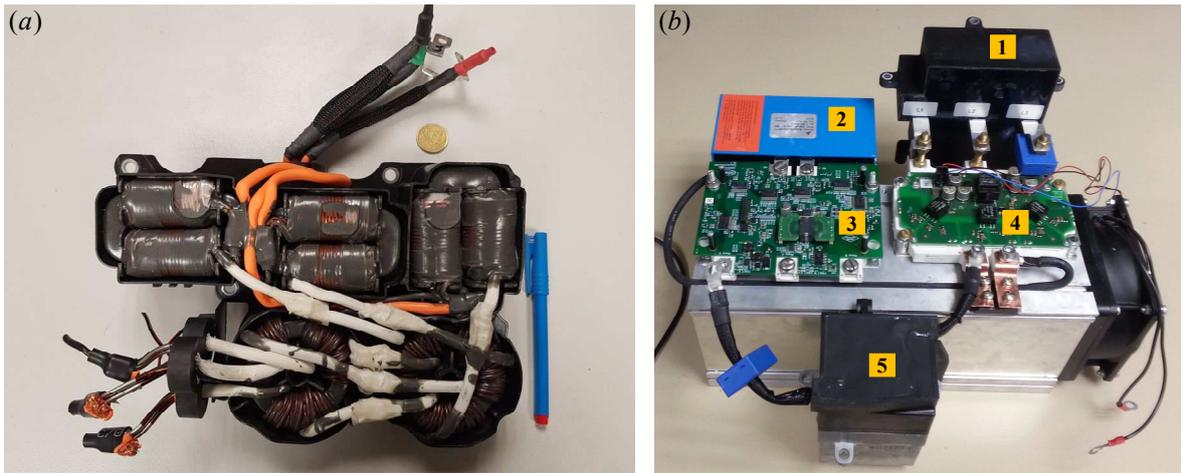


Fig.18. (a) The inductive part of the charger's input EMI filter. (b) 1- DM input capacitors C , 2- DC-link capacitor C_{dc} , 3- Two-level three-phase inverter (i.e. dc-dc Boost converter during charging), 4- CSAR module, 5- additional filtering inductor L_b .

5.2. Specific points related to the structure of the studied charger

5.2.1. Related to the input current source active rectifier

- ❖ Low frequency harmonics (0-2kHz) & damping of the differential mode input filter's resonance

The rectifier's switching takes place on the input side; therefore, a passive differential mode (DM) inductor–capacitor (L_f , C) filter needs to be employed in order to attenuate the input current's switching component. This filter is usually designed in the literature to have a cutoff frequency that ensures the required attenuation for the first input current harmonic [Guzman et al. 2006]. In that way, the current harmonics will be sufficiently attenuated and the parallel filter resonance excited by the switching harmonics avoided. However, the charger maintains the traction's switching frequency at 10 kHz. This would result in a low filter cutoff frequency and a large sized filter. For that reason, a differential mode (DM) inductor L_f is placed in series with the grid impedance. It is designed for high-frequency attenuations and the capacitor is added to ensure proper filtering of the switching component; therefore, the filter's cutoff frequency is around 2 kHz and remains insufficient for proper filtering of the low-frequency current harmonics defined by the standards.

When plugged into a power outlet, the on-board chargers become tied to the grid. As such, they must ensure that the current drawn from the grid presents low harmonic distortion to minimize the power quality impact. Current harmonics reduce the performance and the efficiency of the energy generation and distribution systems. Furthermore, when multiple users are connected to the grid, harmonics generated by one user can interfere with the operation of the other systems simultaneously connected to the grid; therefore, regulations impose tight limits on low frequency (0–2kHz) harmonic current emissions by grid-connected power converters.

Two international standards on electromagnetic compatibility are applicable in the case of EV chargers. On one hand, the IEC 61000-3-2 (Class A) defines the limits for harmonic current emissions in case of equipment having input currents up to and including 16 ARMS per phase, and intended to be connected to public low-voltage distribution systems. On the other hand, the IEC 61000-3-12 complements the previous standard by defining the harmonic currents' limits for input currents

ranging from 16 ARMS to 75 ARMS per phase. For a car manufacturer, on-board electric vehicle chargers are constrained by size, weight and most importantly cost. This leads to a number of hardware limitations such as a low filtering inductance, a reduced number of sensors as well as the re-use of parts of the traction power train. Therefore, the low frequency harmonics covered by these standards need to be investigated through software solutions.

❖ Displacement power factor

The on-board chargers must ensure that the current drawn from the grid presents high displacement power factor to maximize the real power available at the charging station. The displacement angle is the displacement between the fundamental components of the input current, drawn by the charger, and the mains voltage.

In the case of the charger being studied, the DM capacitors’ reactive power results in an input current that is leading the grid’s voltage; hence, displacement power factor correction (DPFC) is needed. In order to refrain from increasing the costs through hardware interventions, the issue will be addressed via software based proposed power factor correction (PFC) control. Different PFC control strategies are developed for the single-phase and the three-phase applications.

5.2.2. Related to the use of the electric machine’s windings

The three-phase fast charging configuration is illustrated in Fig.19. The electric machine’s windings are accessed via the neutral point and used as filtering inductors for the dc-dc Boost converter. This means that the equivalent filtering inductor’s value is relatively low (around 35μH). Therefore, an inductor ($L_b \sim 100\mu\text{H}$) has been added in series. However, the total inductance value remains challenging for a good PFC control and low current ripple especially with a low switching frequency of 10 kHz. On the other hand, the voltage fluctuations across the EM’s stray capacitance, at the neutral point, should be reduced in order to mitigate the CM emissions as well as avoid long term damages to the EM.

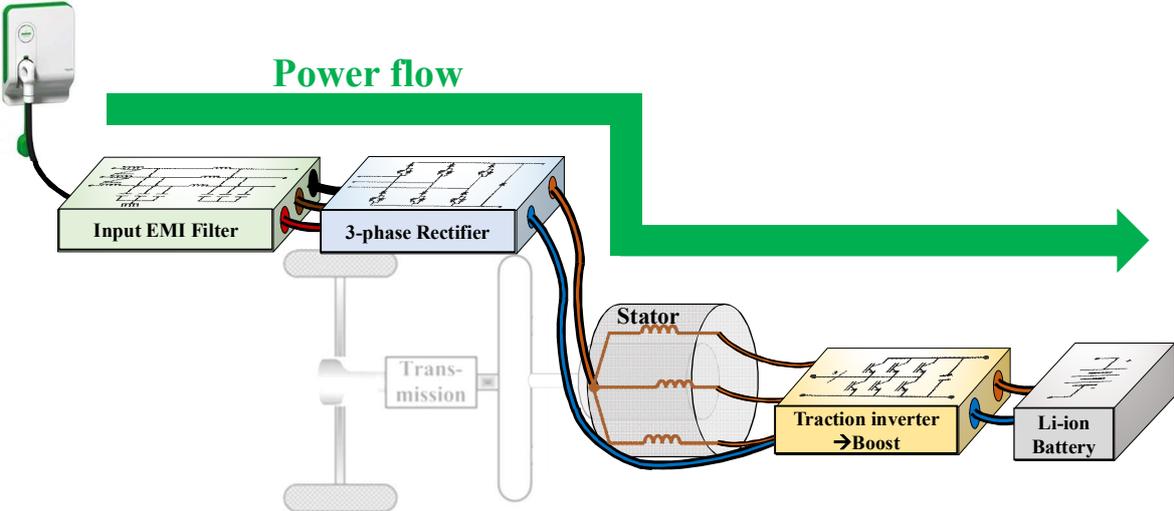


Fig.19. The on-board integrated charger’s three-phase fast charging configuration.

6. Outline and contributions of this study

This work presents the power quality performance analysis and control optimization of an on-board non-galvanically isolated electric vehicle charger integrated to the traction's power train. Different aspects related to the power factor correction of the single-phase as well as the three-phase charging configurations are studied: the control scheme for the regulation of the charging power, the displacement power factor correction, the suppression of the grid current harmonics and the active damping of the input filter resonance. Two experimental test benches are developed using two different technologies (silicon IGBTs vs. silicon carbide Mosfets). Experimental results are provided for different switching frequencies. Moreover, the compliance with the standards for the current harmonics ranging from 100 Hz to 2 kHz is evaluated.

In order to be able to evaluate the high frequency conducted common mode emissions (150 kHz - 30MHz) of a power conversion structure, one needs to develop a good current control scheme that establishes a high-quality low frequency behavior (0 – 2 kHz). Afterwards, these current control structures remain unmodified throughout the study of the common mode emissions. This work also presents a comprehensive approach to modeling the CM & the DM EMI behavior of a power electronics structure. This method is applied to the charger in its single-phase and three-phase configurations. The models allow to evaluate the high-fluctuating internal nodes and to study the effect of various proposed mitigation solutions on the CM emissions. The low computational models are also developed in the intent of being injected into optimization algorithms for the design of an optimal EMI filter.

Therefore, the work is organized into two main Parts (A and B) and a general conclusion with future works is provided.

In Part A, the low frequency current harmonics ($0-2kHz$) are studied. This Part is divided into two Chapters; the first deals with the single-phase charging configuration whereas the second studies the three-phase topology.

Firstly, a single-phase PFC control scheme is proposed. It is based on two modes of operation along a mains period and forms the basis of a current control structure with displacement power factor correction. It allows the reduction of the level of the current flowing through the power circuit which contributes to lowering the switching and conduction losses and offers the possibility of reducing the size of the passive elements. Moreover, a parallel resonance of the input filter is identified and an active damping solution based on a virtual resistance is integrated to the control scheme. Furthermore, a discrete fast Fourier transform algorithm is proposed and tested for the detection of the grid's impedance at the charging station. For the purpose of experimental validation, a test bench was developed at the SATIE laboratory using IGBT modules provided by Renault. The control is implemented on a Texas Instruments DSP. The experimental setup is described and the results are provided. In order to evaluate the use of higher switching frequencies, a new test bench was developed from square one using SiC Mosfets and experimental results are also provided.

The second Chapter of Part A is dedicated to developing a three-phase PFC control scheme. The topology of the charger is studied and a new space vector pulse width modulation strategy is proposed and evaluated. It is proven that lower current levels can also be achieved during three-phase charging and the switching losses can be reduced without affecting the CM behavior of the structure.

In both Chapters, simulation results are confronted between an already existing control scheme (taken from the literature) and the newly proposed PFC controls.

In Part B, the high frequency (150 kHz – 30 MHz) conducted common mode emissions of the charger are studied and evaluated for the single-phase and three-phase operations. It is divided into two Chapters. The first describes a combined CM & DM EMI modeling technique that was developed whereas the second studies the state of the art on conducted CM mitigation techniques and proposes several (minimalistic) modifications to reduce the charger's emissions.

The first Chapter of Part B presents a conducted EMI model for power electronics converters that combines both CM and DM emissions. This model allows the estimation of conducted emissions solely based on the semi-conductors' switching functions. It offers the possibility to chain models in order to emulate the conducted EMI behavior of a global power electronics conversion system. The presented modeling approach is validated through simulations and applied to the non-isolated on-board charger for electric vehicles. Both single-phase and three-phase charging configurations are considered.

In order to reduce the charger's emission levels, the second Chapter of Part B proposes different conducted electromagnetic interference mitigation schemes based on structural and behavioral symmetry. These solutions are assessed using the proposed modeling approach.

Once the EMI reduction techniques adopted and the control laws fixed, an input EMI filter can be designed. Therefore, the study concludes with a quick summary of the contributions and discusses possible future works including the design of a new input EMI filter and the refinement of the EMI modeling process.

With the wide deployment of purely electric as well as plug in hybrid electric vehicles, the future trend in the harmonics' and the CM emissions' limitations tends to be more stringent. Future standards are going to bridge the gap between the current low frequency and high frequency emissions by covering the frequency band from 2 kHz to 150 kHz. Thus, integrating these limitations in the design process of the chargers becomes inevitable.

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Part A

Power Quality & Performance Optimization

The EV charger should meet certain criteria that are set for the external as well as the internal operation of the converter.

Grid-tied power converters must ensure that the current drawn from the grid presents low harmonic distortion and high displacement power factor. Therefore, the EV's charging is subjected to low frequency current harmonics standardized testing. The compliance with the IEC 61000-3-2 (Class A) is verified for charging powers lower than or equal to 3.7 kW in single-phase charging and 11 kW for three-phase charging. Moreover, the compliance with the IEC 61000-3-12 is verified for single-phase charging powers comprised between 3.7 kW and 7.4 kW as well as three-phase charging powers comprised between 11 kW and 51 kW. This emphasizes the need for a single-phase as well as a three-phase PFC control strategies that enhance the external grid-side performance of the charger.

On the other hand, the charger needs to meet internal performance criteria; such as, the minimization of the switching and conduction power losses, the minimization of the voltage fluctuations at the negative side of the battery, the reduction of the conducted common mode emissions and the reduction of the level of the current flowing through the charger. Moreover, for a car manufacturer, onboard electric vehicle chargers are constrained by size, weight and most importantly cost. This leads to a number of hardware limitations; for instance, a low filtering inductance, a reduced number of sensors and a buck-type rectifier input stage. This requires control strategies that regulate the charging power despite these restrictions.

As a result, this study proposes two wholesome PFC control strategies in order to achieve the compliance with these standards through software solutions. Therefore, this Part includes two Chapters.

The first Chapter deals with the power quality analysis for the single-phase configuration. It is organized as follows: the input current source active rectifier (CSAR) stage is analyzed and the phase-shift displacement power factor correction strategy is explained. A periodical distortion is identified in the grid current. By examining the switching states of the input stage, it is demonstrated that the distortion is linked to the input filter's resonance. This comprehensive analysis shows, at each zero crossing of the AC mains, the presence of zero levels in the converter current which could eventually excite the input filter's resonance. This phenomenon is experimentally verified and an active damping solution based on a virtual resistor placed in parallel with the filter's capacitor is applied in accordance with an online Discrete Fourier Transform (DFT) to track the resonance frequency variations. Afterwards, the current control structure that is based on two distinct modes of operation is detailed along with the small-signal model of the converter. The latter allows the design of the inner loop controller and the evaluation of the input filter's impact on the control stability. Two experimental test benches are developed with two different semi-conductor technologies (Silicon and Silicon Carbide) to validate the simulations' theoretical findings. Compliance with the standards is achieved and system limitations are discussed.

The second Chapter presents the power quality analysis and control / performance optimization of the electric vehicle's three-phase charger. The PFC control strategies relevant to the three-phase current source active rectifiers are reviewed. Furthermore, a control strategy applied to a converter, which has a topology similar to that which is being studied, is simulated and analyzed. This allows the identification of areas for improvement. Based on that, a new PFC control is proposed. It includes a current modulation strategy based on space vector modulation. The study is supported by simulation results. An overview of the contributions detailed in Part B is given in Fig.1.

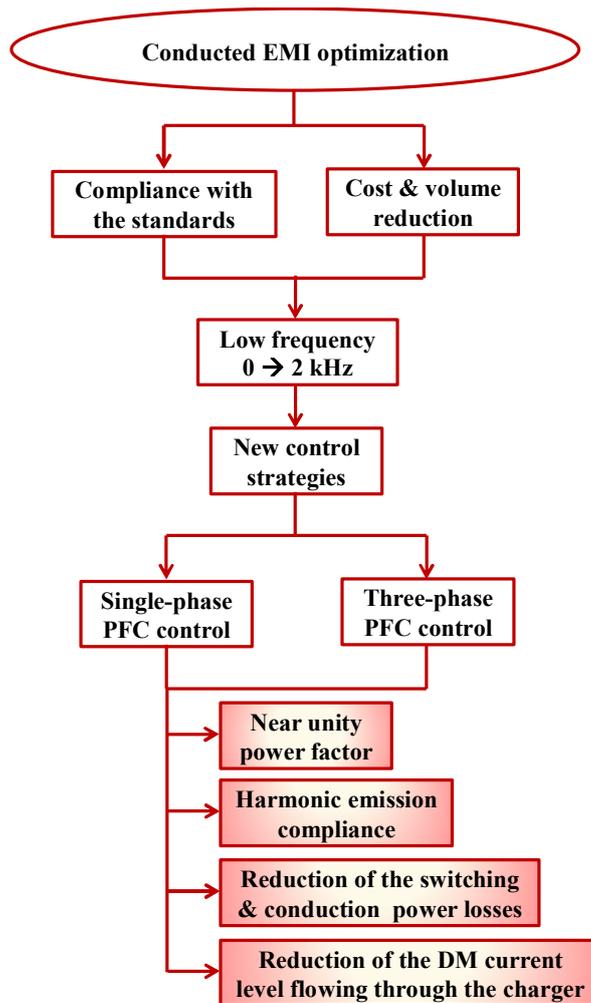


Fig.1. Overview of the low frequency power quality study.

Chapter 1

Single-Phase Charging

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This chapter aims to study the power factor correction (PFC) scheme for the single-phase configuration of the charger illustrated in Fig.I.1.

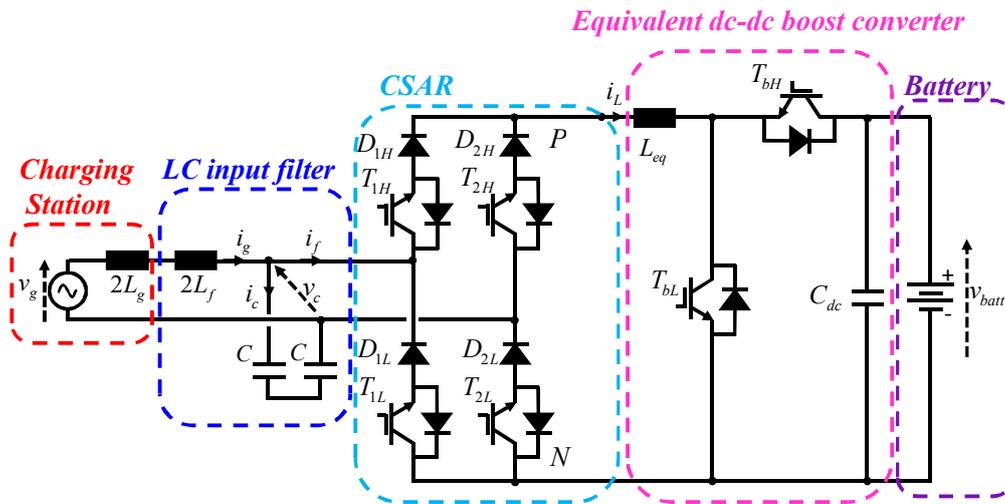


Fig.I.1. Simplified power circuit of the single-phase charger with a CSAR input stage and a dc-dc Boost output stage.

1. Displacement power factor correction

The challenges of achieving unity power factor mainly result from using the CSAR as the charger's input stage. As demonstrated by [Pires et al. 2005], whenever the design of the filter capacitor does not meet the maximum allowed displacement angle between the grid's voltage and current, the need for displacement power factor correction (DPFC) emerges. In this case, the filtering capacitor's reactive power results in an input current that is leading the grid's voltage hence, displacement power factor correction (DPFC) is needed.

Various displacement power factor control schemes have been developed; some are based on reactive power compensation [Monfared et al. 2012] - [Xiao et al. 1998] and others on direct phase-shift control [Michalik et al. 2007] - [Michalik et al. 2008]. However, given the fact that our input stage is a current unidirectional active rectifier, the structure retained is based on phase-shift control for the experimental prototype. In order to highlight the effects of the DPFC on the input side of the charger, the current in the filtering inductor of the boost is controlled, in this section, at a constant level by using a hysteretic current controller. Hence, the CSAR is studied with the equivalent of a current source output stage as shown in Fig.I.2. A freewheeling diode is added at the output of the CSAR to simplify the control implementation (avoid recovery time management between two switches).

1.1. Analysis

Fig.I.3 (a) shows the natural phasor diagram of the angular line frequency components on the input side of the converter. The grid side voltage sensor measures the voltage across the filter capacitors; therefore, v_c is chosen as the phasor diagrams' reference signal. A PFC converter is usually operated so as to draw a converter current i_f with a fundamental component being in phase with the converter voltage v_c (Fig.I.3 (b)). However, the latter causes reactive current i_c to flow through the input capacitor. Consequently, the current i_g drawn from the grid, at the charging station, is naturally leading

the input voltage by the displacement angle φ between their fundamental components. This result in a reduced DPF in eq. (I.1)) and a reduced power factor PF defined in eq. (I.3)) using the ratio of the total harmonic distortion denoted THD in eq. (I.2)).

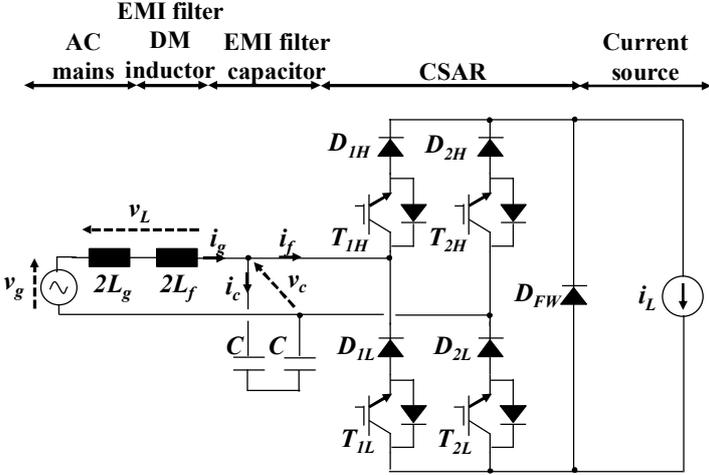


Fig.I.2. Equivalent power circuit of the single-phase charger with a hysteretic current controller applied to the boost output stage.

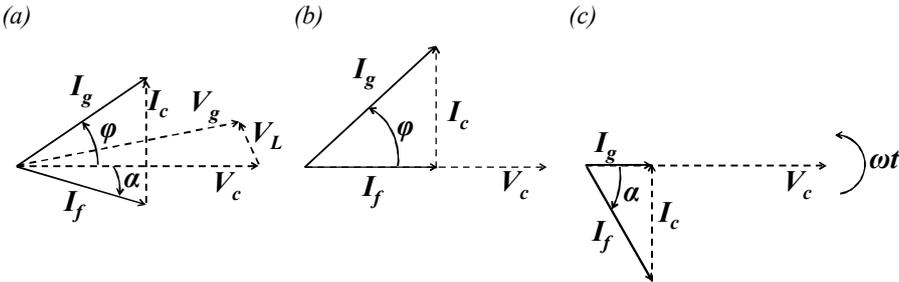


Fig.I.3. Current and voltage phasor diagrams at the grid side considering a constant dc output current and $I_f = I_L$. (a) Natural extended phasor diagram before PFC. (b) Simplified typical PFC configuration showing a phase lead of the grid current. (c) Simplified proposed PFC scheme based on the phase-lag of the converter current.

The design of the input filter’s capacitor is highly dependent on the switching frequency and the charging power. Moreover, it should meet several requirements among which a size constraint, a sufficient attenuation of the switching component as well as achieving control stability by limiting the filter/converter interactions [Vlatkovic et al. 1996]. One additional requirement that should be taken into consideration only when designing power factor correction (PFC) converters is the maximum allowed displacement angle between the filter’s input voltage and current introduced by the capacitor. Whenever this design constraint is not met, the need for DPFC manifests itself.

$$DPF = \cos \varphi \tag{I.1}$$

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} I_{h_{RMS}}^2}}{I_{1_{RMS}}} \quad \text{eq. (I.2)}$$

$$PF = DPF \cdot \sqrt{\frac{1}{1+THD^2}} \quad \text{eq. (I.3)}$$

1.2. Synchronization with the grid using SOGI-PLL scheme

PFC applied to an active rectifier requires the extraction of information from the voltage supply in order to synchronize the control with the line frequency. This is usually achieved through the use of either closed-loop or open-loop methods [Boyra et al. 2011]. The latter include discrete Fourier transformations [McGrath et al. 2005], Kalman filtering techniques [Moreno et al. 2007], adaptive notch filtering methods and weighted least mean square algorithms [Qasim et al. 2014]. However, their performances are highly dependent on their ability to filter distorted signals as well as their adaptability to changes in frequency. On the other hand, closed-loop methods are based on Phase Locked Loops (PLL) whether in their classical definition or modified structures [Yazdani et al. 2009] - [Rodríguez et al. 2012] - [Golestan et al. 2014] - [Wang et al. 2015]. Among those methods, the Second Order Generalized Integrator PLL (SOGI-PLL) allows the filtering of the input signal without introducing phase delay and presents adaptive capabilities to frequency variations [Ciobotaru et al. 2006].

Vector-based single-phase PLLs are inspired from the three-phase synchronous frame PLLs. However, the challenge in single-phase applications consists in generating a signal with a 90 degrees phase-shift with regards to the input fundamental.

Let x represent an electrical variable such as a grid current or voltage eq. (I.4)).

$$x(\theta_x) = X_{1m} \sin(\theta_x + \varphi_{1x}) + \sum_{n=2}^{\infty} X_{nm} \sin(n\theta_x + \varphi_{nx}) \quad \text{eq. (I.4)}$$

The role of the SOGI is to compute a virtual two-phase stationary orthogonal reference frame (α, β) in which the input signal's components (x_α, x_β) are found through the use of two integrators Fig.I.4. The filter's transfer functions are computed in eq. (I.5)) and eq. (I.6)).

$$\frac{x_\alpha}{x}(s) = K_{sogi} \cdot \frac{s/\omega_{pll}}{1 + K_{sogi} \cdot \frac{s}{\omega_{pll}} + \frac{s^2}{\omega_{pll}^2}} \quad \text{eq. (I.5)}$$

$$\frac{x_\beta}{x}(s) = K_{sogi} \cdot \frac{1}{1 + K_{sogi} \cdot \frac{s}{\omega_{pll}} + \frac{s^2}{\omega_{pll}^2}} \quad \text{eq. (I.6)}$$

It can be seen from eq. (I.7)) that x_β has a 90 degrees phase shift with regards to x_α . The latter represents the fundamental component of x . Their expressions are given in eq. (I.8)) and eq. (I.9)).

$$\frac{x_\beta}{x_\alpha}(s) = \frac{\omega_{pll}}{s} \quad \text{eq. (I.7)}$$

$$x_\alpha = X_{lm} \sin(\theta_x + \varphi_{1x}) \quad \text{eq. (I.8)}$$

$$x_\beta = -X_{lm} \cos(\theta_x + \varphi_{1x}) \quad \text{eq. (I.9)}$$

On the other hand, the role of the PLL is to extract the information regarding the angular frequency (ω_{pll}) as well as the information regarding the amplitude of x . By substituting eq. (I.8)) and eq. (I.9)) into the rotation matrix expression eq. (I.10)), we can easily deduce that x_d yields the information regarding the amplitude of x as in eq. (I.12)). On the other hand, substituting eq. (I.11)) and eq. (I.13)) in the PLL's closed loop with a null reference leads to eq. (I.14)).

$$x_d = x_\alpha \cos \theta_{pll} + x_\beta \sin \theta_{pll} \quad \text{eq. (I.10)}$$

$$x_q = -x_\alpha \sin \theta_{pll} + x_\beta \cos \theta_{pll} \quad \text{eq. (I.11)}$$

$$x_d = X_{lm} \quad \text{eq. (I.12)}$$

$$\theta_{pll} = \frac{\omega_{pll}}{s} \quad \text{eq. (I.13)}$$

$$\theta_{pll} = \theta_x + \varphi_{1x} - \frac{\pi}{2} \quad \text{eq. (I.14)}$$

Synchronization between SOGI and PLL is achieved through feedback of ω_{pll} . Assuming that the grid has a reference frequency of $\omega^* = 2\pi \times 50 \text{ (rad.s}^{-1}\text{)}$ that can slowly vary between 48 and 52 Hz, the PLL is able to track the real angular frequency ω_{pll} by adjusting the reference frequency value ω^* through the Proportional Integral (PI) controller output.

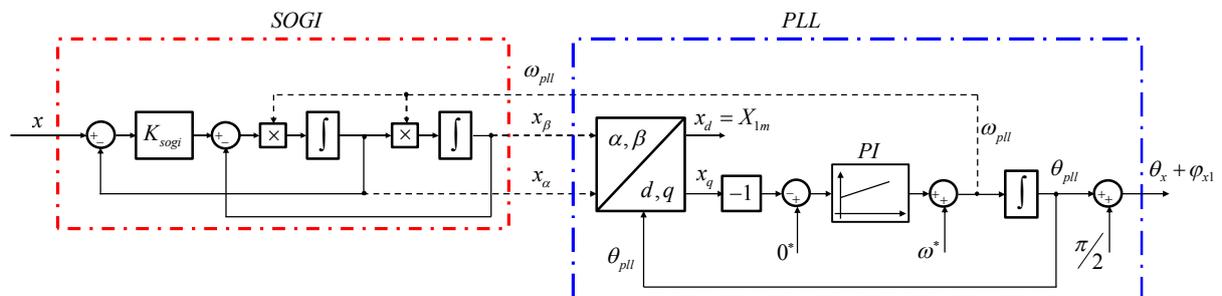


Fig.I.4. Generalized SOGI-PLL synchronization bloc diagram.

1.3. Phase-shift control scheme

In order to compensate for the input capacitor's reactive power, a forced phase lag of an angle α is introduced to the converter current i_f . Thus, a lagging i_f will compensate for a naturally leading i_g , as shown in Fig.I.3(c). The use of the CSAR as an input stage presents the advantage of being able to shape the fundamental component of the converter current i_f and introduce the required phase lag.

Pulse Width Modulation (PWM) linear control of current rectifiers based on Proportional Integrator (PI) controllers varies depending on the control strategy employed [Teodorescu et al. 2011]. Three main strategies are distinguished: current control [Louganski et al. 2007], active/reactive power control [Rivera et al. 2014] - [Monfared et al. 2012] and direct phase control [Wu 2006].

PIs used in PFC current control schemes present limited disturbance rejection capability as well as a steady-state magnitude and phase error since the reference signal is a sinusoidal waveform in phase with the converter voltage. This leads to higher current distortions and reduced displacement power factor. On the other hand, PI current controllers used in the synchronous dq-frame allow for separate active and reactive power controls as well as faster dynamic response due to the constant DC nature of the reference signals. However, this strategy requires more computational efforts from the DSP and the decoupling of the active/reactive powers requires the use of cross coupling terms dependent on the input filter parameters. Finally, the use of PI controllers in direct phase-shift strategies is parameter independent. Furthermore, the phase reference signal is a DC quantity. However, the closed loop is highly dependent on the SOGI-PLL synchronization dynamics. Fig.I.5 shows the employed direct phase-shift DPFC scheme.

Current and voltage sensors are used at the power outlet level. The fundamental components of the measured converter voltage v_{ca} and grid current i_{ga} are determined using the (SOGI) filter described above.

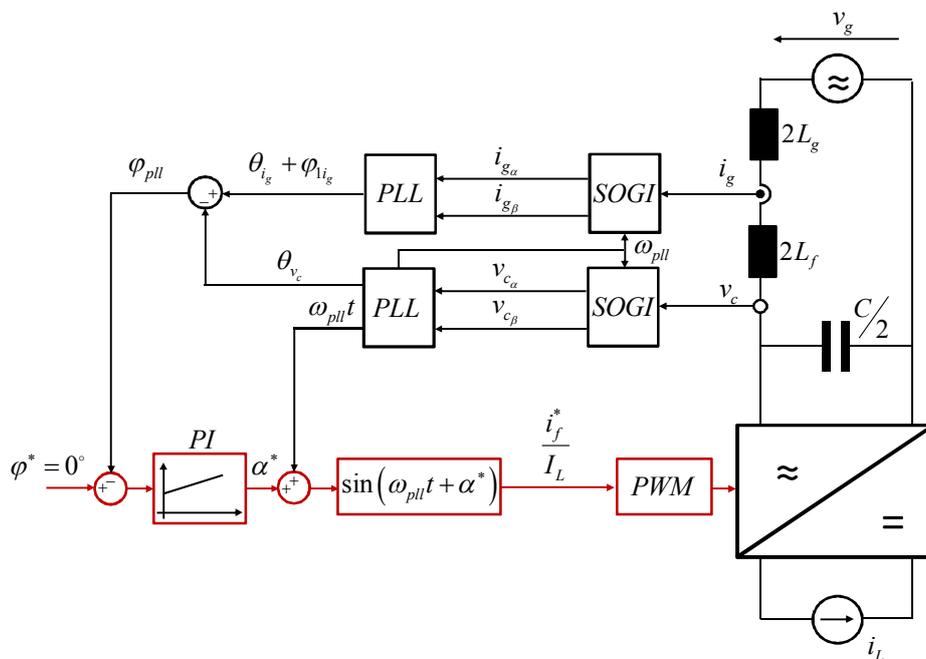


Fig.I.5. DPFC scheme based on phase-shift control.

The information regarding the angular line frequency ω_{pll} and the displacement angle φ_{pll} between these two signals is extracted using two PLLs. The control scheme must compensate the total input reactive power, including any future EMI filter adopted and its additional capacitors. Therefore, the phase lag angle α is not mathematically computed using a known capacitance value; it is however, deduced from a phase-shift control loop. Furthermore, for the sake of simplicity, the maximum converter current is equal to the DC current i_L . However, in order to ensure the possibility of achieving unity DPF, both simulations and experimental validations employ values for i_L that comply with eq. (I.15)).

$$I_L \geq \omega_{pll} \cdot \left(\frac{C}{2}\right) \cdot V_c \quad \text{eq. (I.15)}$$

Computation of the PI controller parameters eq. (I.16)) is achieved through the identification of the transfer function between the grid current's leading phase angle φ and the converter current's lagging phase angle α . The open loop response to a step change in α (Fig.I.6) indicates that the transfer function can be approximated by a first order system presenting a time delayed response eq. (I.17)). The value of the time delay is represented by T_d . The time constant τ_i is chosen through pole placement and the proportional gain k_p is tuned to ensure adequate Gain Margin.

$$PI(s) = k_p \cdot \left(\frac{\tau_i \cdot s + 1}{\tau_i \cdot s}\right) \quad \text{eq. (I.16)}$$

$$\frac{\varphi}{\alpha}(s) \approx \frac{k}{1 + \tau \cdot s} \times \frac{1}{1 + T_d \cdot s} \quad \text{eq. (I.17)}$$

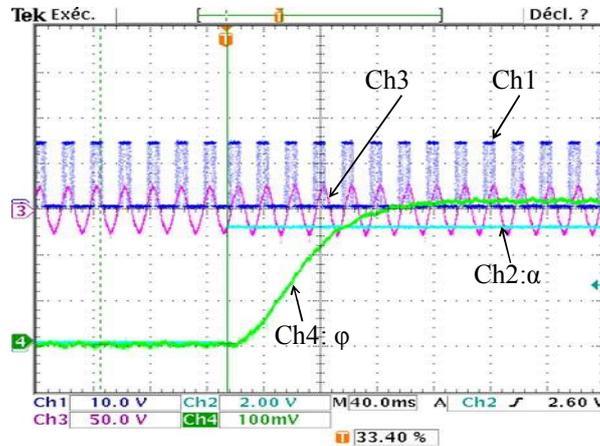


Fig.I.6. Open loop response to a step like variation of the phase-angle α . Ch. 1: Gate signal of T_{1H} . Ch 2: phase angle α of the converter current i_f . Ch 3: Converter voltage v_c and Ch. 4: phase angle φ of grid current i_g .

1.4. Simulation results

Simulation results, for the system parameters provided in Table I.1, are presented in Fig.I.7. In order to emulate a current source, the equivalent boost filtering inductor is deliberately chosen to be high enough to reduce the dc current ripple while maintaining the same switching frequency. The theoretically calculated total harmonic distortion (THD) rate of the grid current is calculated using eq.

(I.18) and is found to be at 17%. Results show a distortion occurring at each zero crossing of the mains voltage as well as the presence of zero levels at the beginning of each half cycle of the converter current.

TABLE I.1. SIMULATION & EXPERIMENTAL SYSTEM PARAMETERS

Symbol	Description	Value (Unit in SI)
L_g	Grid Impedance's imaginary part	2 (mH)
L_f	DM Filter Inductor	60 (μ H)
C	Series input capacitors	100 (μ F)
V_{gm}	Amplitude of the AC mains voltages	$100\sqrt{2}$ (V)
ω	Angular line frequency	$2\pi \cdot 50$ (rad.s ⁻¹)
I_L	Current level controlled by the Boost	8.5 (A)
L_{eq}	Equivalent filtering inductor	2 (mH)
f_{sw}	Switching frequency	10 (kHz)
φ^*	Displacement angle reference	0°
f_s	Sampling frequency	10 (kHz)

$$THD(\%) = 100 \times \sqrt{\sum_{h=2}^{40} \left(\frac{I_{h_{RMS}}}{I_{1_{RMS}}} \right)^2} \quad \text{eq. (I.18)}$$

Furthermore, the investigation of the low frequency content of the grid current highlights the 7th harmonic ($f_7 = 350$ Hz) as the harmonic with the highest amplitude. This odd harmonic coincides with the input filter's resonance frequency defined in eq. (I.19)).

$$f_r = \frac{1}{2\pi \cdot \sqrt{(L_g + L_f) \cdot C}} \cong 350 \text{ Hz} \quad \text{eq. (I.19)}$$

These results are going to be analyzed in the next section. On the other hand, the comparison with the IEC61000 3-2 standard clearly shows that the charger with the present DPFC scheme is non-compliant with the limits defined; moreover, this non-compliance occurs for the harmonics surrounding the input filter's resonance frequency (Fig.I.7 (d)).

The frequency peak due to the resonance is particularly sensitive to the grid impedance change (Fig.I.8), the filter's second order oscillatory response appears on the input current and converter voltage respectively. Therefore, the grid side distortion is a slightly damped periodical resonance phenomenon.

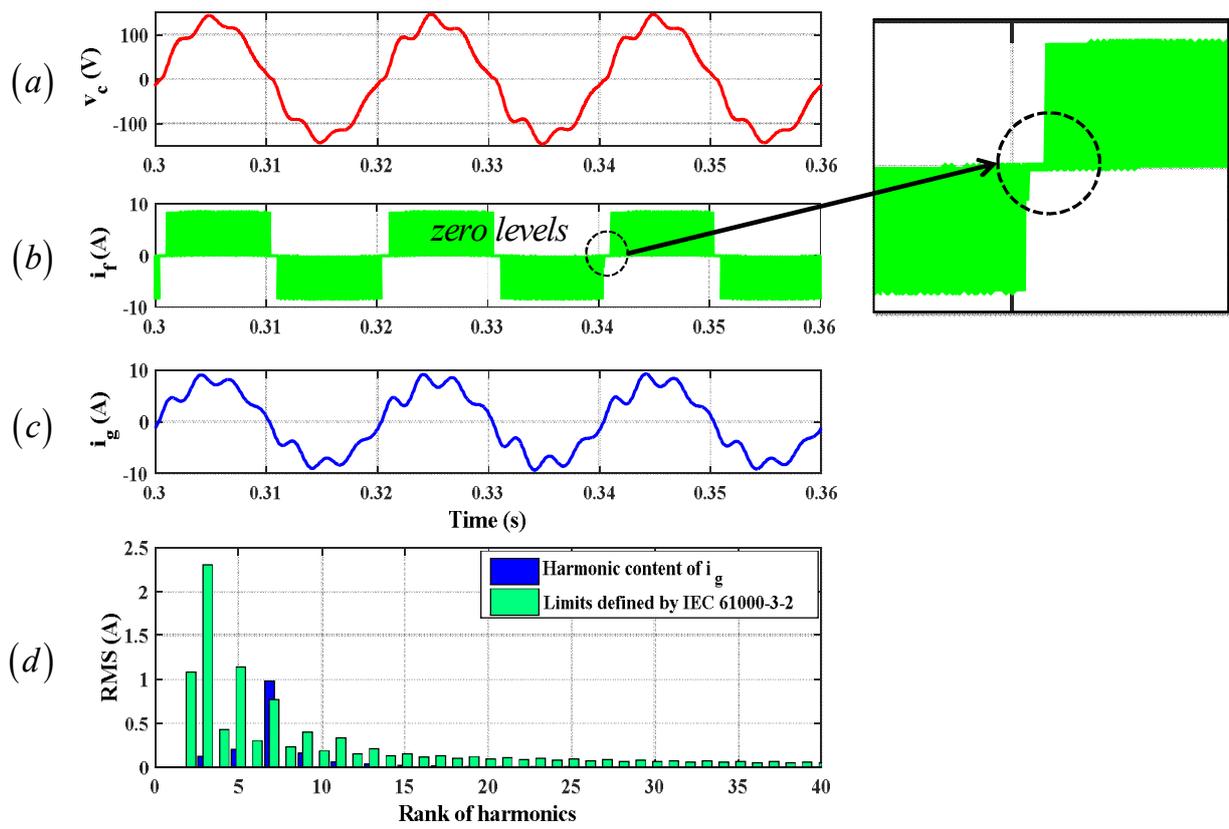


Fig.I.7. DPFC simulation results. (a) Distorted converter voltage. (b) Converter current presenting zero levels. (c) Current drawn from the grid. (d) Harmonic content of the grid current compared with the IEC standard up to 2 kHz.

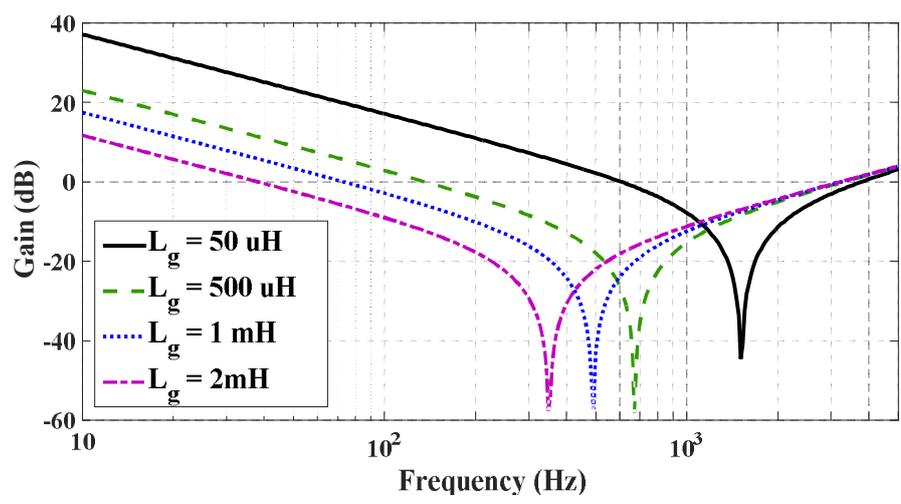


Fig.I.8. Bode gain plot (dB) of the admittance of the input filter for different grid impedance values using Psim.

2. Input filter resonance & active damping solution

Simulation results show a periodical resonance phenomenon that appears on the grid side of the converter. Previous works using single-phase CSARs mainly study the control schemes under grid voltage distortion [Baumann et al. 2005] – [Liu et al. 2011]. However, to our knowledge, the distortion appearing when using phase-shift has not yet been analysed with respect to the excitement of the input filter's resonant mode. In order to verify the origins of the input filter's resonance, a time-domain analysis is conducted using the switching states of the rectifier followed by a frequency-domain analysis.

2.1. Time-domain analysis of the resonance phenomenon

Experimental results shown in [Xiao et al. 1998] also present a periodical resonance at the beginning of each half cycle; however, this phenomenon wasn't investigated. In order to understand the reason behind the excitement of the input filter, we will examine the switching states of the CSAR.

The low-side IGBTs are maintained closed during charging. The switching of the low side diodes depends on the converter's voltage polarity (Fig.I.9). However, the high-side IGBTs' switching states depend on the lagging converter current's polarity. Therefore, at each zero crossing of the mains voltage and as long as i_f is lagging with respect to v_c , the diodes will block the flow of the converter current.

This results in periodical zero levels in the converter current. On another hand, the LC input filter is prone to series and parallel resonances coming from the grid disturbances and the converter harmonics respectively.

In previous work, [Wu 2006] shows that the switching harmonics lead to the resonance of the input filter. The study deals with a three-phase CSAR based on gate-controlled thyristors switching at low frequency 540 Hz. However, our study deals with a single-phase CSAR based on IGBTs switching at 10 kHz hence, the switching harmonics are shifted towards the high frequencies. Since the input filter's resonance for 600 μ H grid impedance is of 619 Hz, nearly 16 times lower than the switching frequency, it's the DPFC scheme rather than the switching harmonics that leads to parallel resonance of the filter.

In order to illustrate that, a simulation is carried where we impose a converter current presenting only periodical zero levels without pulse width modulation (Fig.I.10 (a)) and study the low frequency spectrum, up to 2 kHz, of both the converter and grid current (Fig.I.11 (a)). By isolating the effect of the zero levels from that of the switching we find that the converter current presents a rich low frequency spectrum with an 9th harmonic sufficient to excite the filter's resonant mode (in this example the filter's resonance frequency is around 500 Hz).

Furthermore, the same approach is conducted for a converter current presenting both the zero levels and the switching component at 10 kHz (Fig.I.10 (b)). The study of the low frequency spectrum, up to 2 kHz, of both the converter and grid current is given in Fig.I.11 (b). By comparing both studies, we can deduce that the effects of the switching frequency's harmonics appear at high frequencies and do not affect the low frequencies responsible for the excitement of the input filter's resonance. Therefore, the distortion is essentially due to the zero levels that excite the input filter's parallel resonant mode and produce a second order oscillatory response. This will be verified by means of frequency-domain analysis of the input stage of the charger.

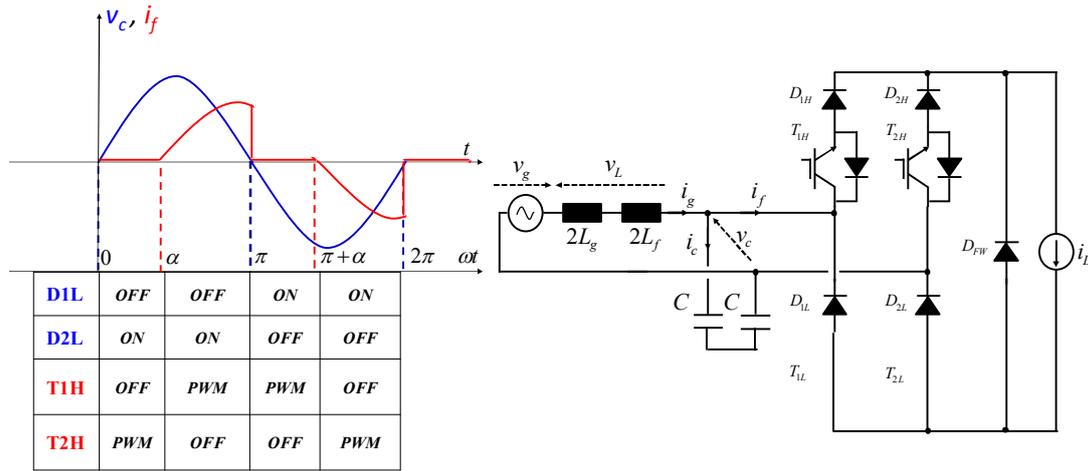


Fig.I.9. Switching states of the input CSAR's reverse blocking IGBTs.

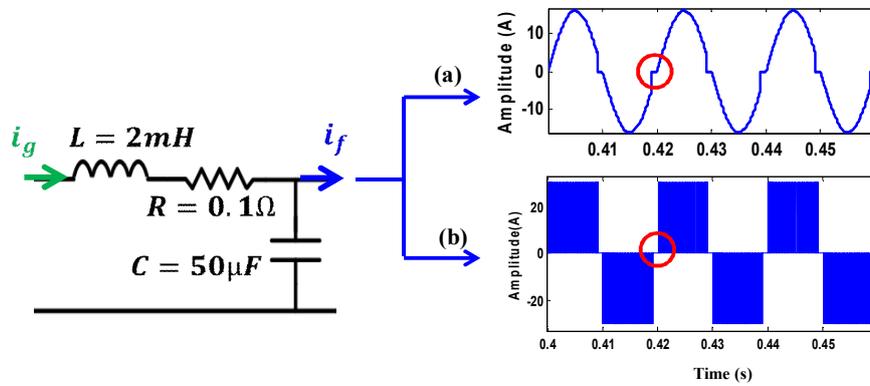


Fig.I.10. Simulation of the grid current obtained at the input of an LC filter for a converter current presenting zero levels: (a) without the switching component. (b) With the switching component.

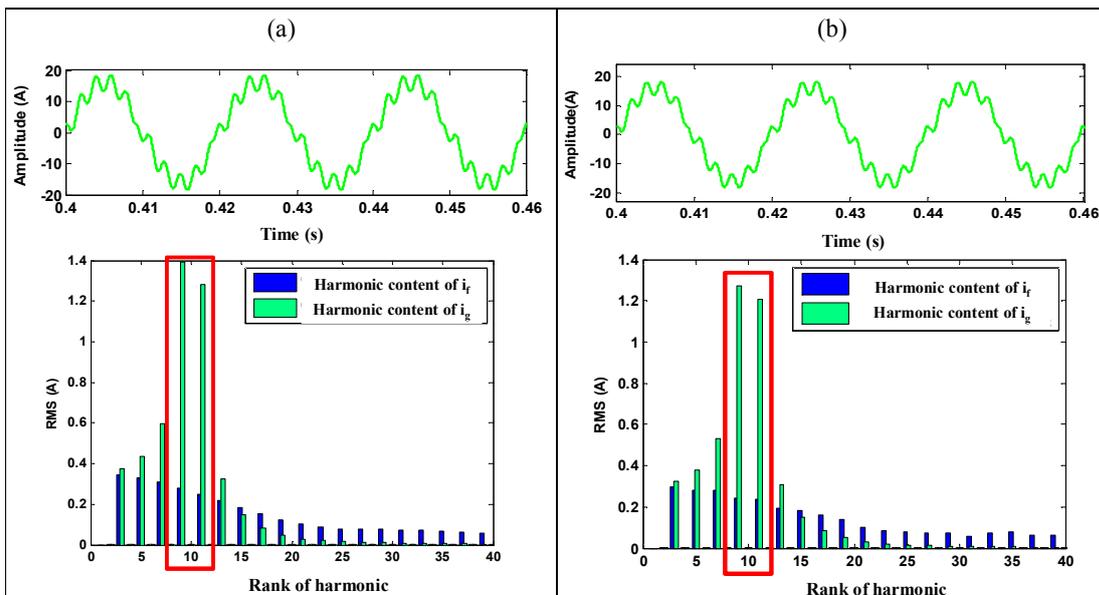


Fig.I.11. . Simulation results of the grid current obtained at the input of an LC filter for a converter current presenting zero levels: (a) without the switching component. (b) With the switching component.

2.2. Frequency-domain analysis of the resonance phenomenon

In this section, the frequency-domain analysis is going to be applied to the same experimental setup used for the experimental validations. Therefore, the input stage of the converter is modeled according to the test bench's setup shown in Fig.I.12 (a). The auto-transformer is employed to gradually increase the voltage. The charger is substituted by a differential mode current source representing the current absorbed at the input side of the rectifier i_f . On the other hand, measurements were carried at the power supply outlet in order to measure the power supply voltage at no load condition $v_{g_{no\ load}}$ and the equivalent impedance of the network Z_g . Furthermore, the auto-transformer is modeled by an ideal transformation ratio m and a total leakage impedance Z_{leak} . The input stage also contains the impedance measurements of the differential mode filtering inductor Z_{L_f} and capacitor Z_C . The measurements are all conducted using an Agilent Technologies E5061B impedance analyzer. The impedance and voltage measurements are going to be detailed in this section.

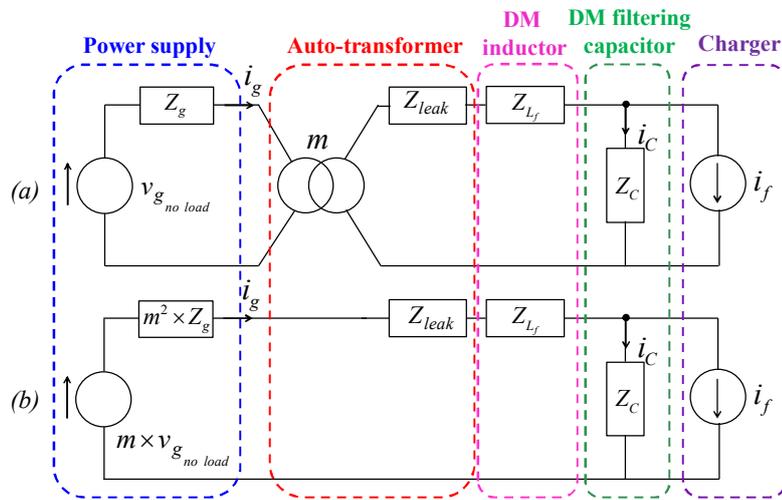


Fig.I.12. (a) DM modeling of the input stage. (b) DM model at the secondary side of the transformer.

2.2.1. Characterization and circuit modeling of the test bench's power supply

a. Measurement of the supply voltage at no-load condition

The single-phase power supply voltage is measured at the test bench's power outlet at no-load condition. The resulting measurement is given in Fig.I.13. It can be seen from the Fast Fourier Transform (FFT) waveform analysis applied to this measurement, that the supply voltage, at no-load condition, already contains LF harmonics. Therefore, the power supply is polluted by other powered equipment in the laboratory. This source of harmonics needs to be taken into account when analyzing the power quality of the current absorbed from the mains.

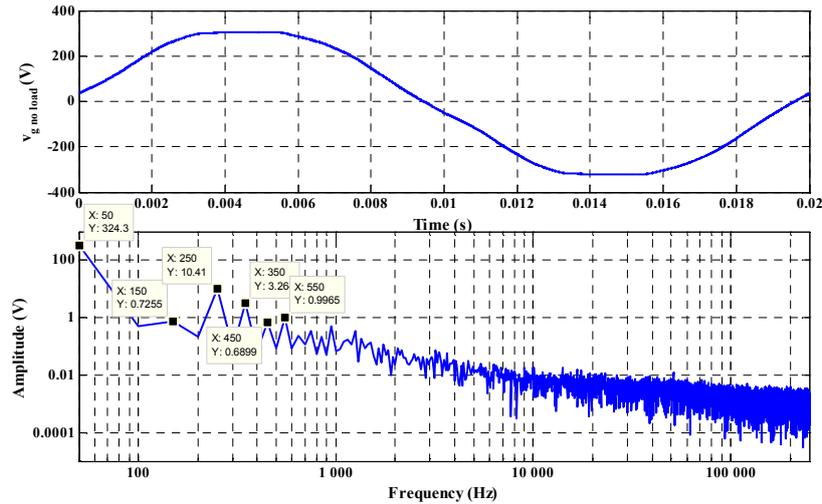


Fig.I.13. LF harmonic content of the supply voltage measured at no-load condition.

b. Measurement of the mains impedance

The power supply's impedance is measured using the overlap phenomenon in a single phase diode bridge with an (R, L) load. The experimental setup is described in Fig.I.14. In fact, the output voltage of the bridge rectifier, during overlap, is zero and all of the supply voltage applies across the source impedance Z_g . Thus, by assuming that the source impedance is mainly inductive, its value is deduced using eq. (I.20)) and replaced in eq. (I.21)) to compute Z_g .

$$L_g = \frac{V_{g_{RMS}} \cdot \sqrt{2}}{2 \times I_{load} \times 2 \cdot \pi \cdot f} \cdot (1 - \cos \theta) = \frac{230 \cdot \sqrt{2}}{2 \times 3.5 \times 2 \cdot \pi \cdot 50} \cdot \left(1 - \cos\left(\frac{0.00008 \times 2 \cdot \pi}{0.02}\right)\right) = 46 \mu H \quad \text{eq. (I.20)}$$

$$Z_g = L_g \cdot \omega \cdot e^{i \cdot \frac{\pi}{2}} \quad \text{eq. (I.21)}$$

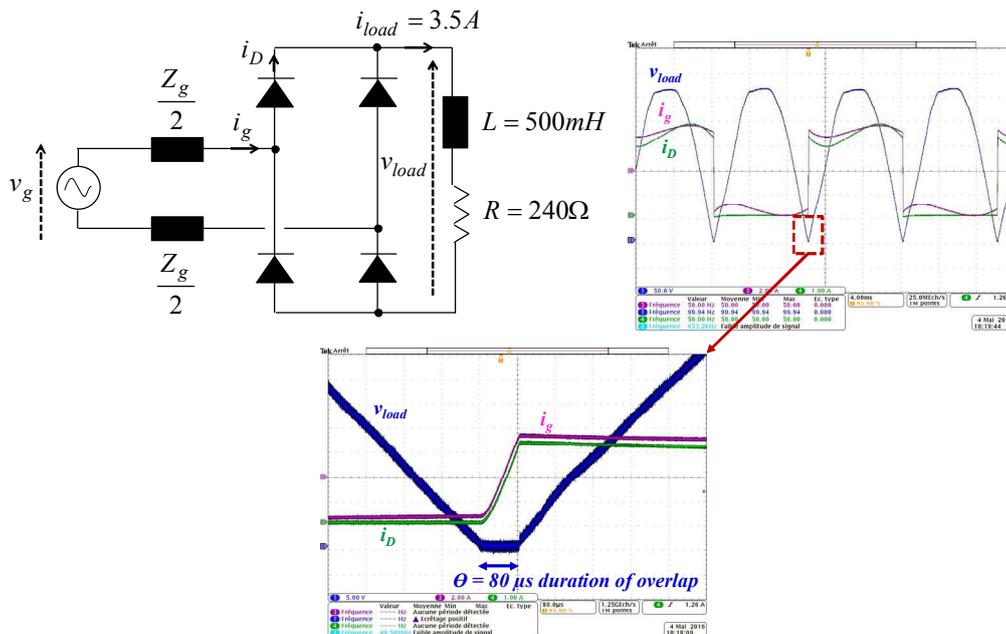


Fig.I.14. Experimental setup for the estimation of the grid impedance.

2.2.2. Characterization and circuit modeling of the input filter

a. DM filtering inductor

The measured filtering inductor's impedance is shown in Fig.I.15. It yields the following expression:

$$Z_{L_f} = Z_L \cdot e^{i \cdot \frac{\pi}{180} \cdot Phase} \quad \text{eq. (I.22)}$$

This measurement allows extracting the value of the inductance which is equal to about 5 mH. The capacitive effects appear at about 270 kHz. Moreover, the complex impedance will be used in the computation of the model.

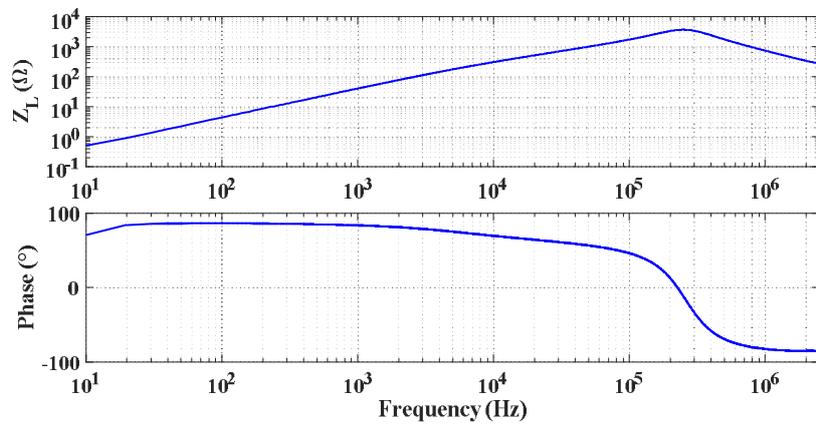


Fig.I.15. Impedance measurement of the DM filtering inductor.

b. DM filtering capacitor

The same goes for the DM filtering capacitor. Its measured impedance is given in Fig.I.16. The capacitance is equal to about 35 μF which is equivalent to the series association of two DM filtering capacitors. The equivalent series inductance becomes preponderant starting from 40 kHz.

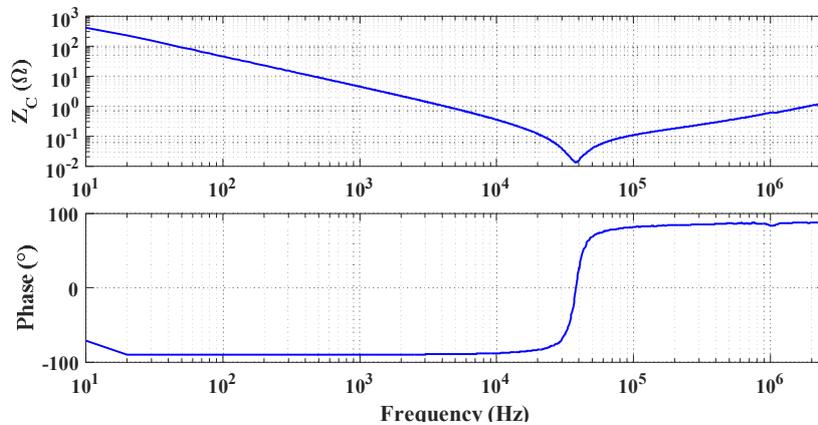


Fig.I.16. Impedance measurement of the DM filtering capacitor.

2.2.3. Characterization of the auto-transformer

The global leakage impedance is measured using the impedance analyzer at the secondary side of the transformer while maintaining the primary side short-circuited. This measurement varies with the transformation ratio ‘m’. It was measured for $m = 20\%$ which is retained for the rest of this section. This impedance behaves as a resistance up to about 1 kHz. Beyond this frequency an inductive behavior is preponderant and the equivalent inductance is equal to about 200 μH . By conducting several measurements for different transformation ratios, we noticed that the leakage inductance varies with m in a ratio that attains a maximum value of 3; however, it remains negligible compared to the value of the DM inductance.

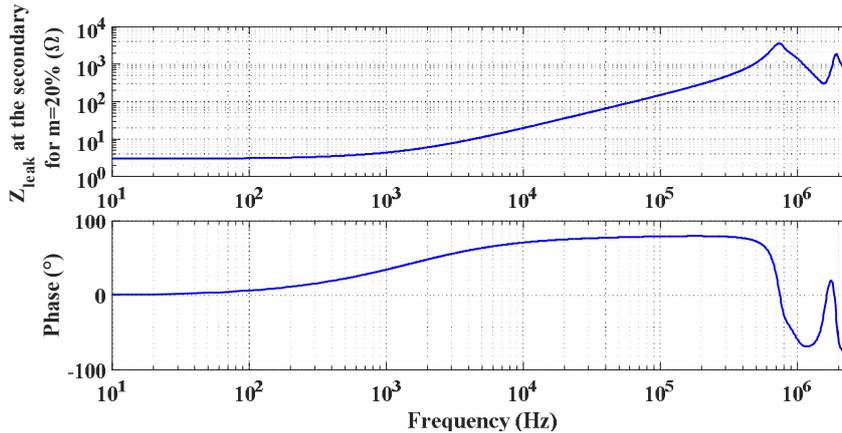


Fig.I.17. Impedance measurement of the total leakage impedance at the secondary side of the autotransformer for a transformation ratio of 20%.

2.2.4. Modeling of the differential mode input current source

At this point, the study focuses only on the input stage of the charger. Thus, the latter’s behavior can be modeled by a differential mode current source representing the current at the input side of the rectifier i_f . Different cases are going to be studied. In each case, a current i_f , either measured or modeled in the frequency-domain, is going to be injected into the model of Fig.I.12 (b). Thus, by means of an inverse Fast Fourier Transform the waveform of the grid current can be re-created.

Once the impedances are well established, the superposition theorem applied to the model in Fig.I.12 (b) shows that the low frequency harmonics of the supply voltage at no-load condition are capable of causing a series resonance of the input filter (Fig.I.18 (a)); while the low frequency harmonics of the current at the input side of the rectifier are capable of exciting a parallel resonance of the filter (Fig.I.18 (b)). Therefore, it is essential to evaluate the impact that each of these two sources of harmonic pollution has on the quality of the current absorbed from the grid.

2.2.1. Low frequency impact of the differential mode current source

The transfer function (TF) between the grid current i_g and the input current of the rectifier i_f is given in eq. (I.23)). The Bode diagram of this transfer function, restricted to 10 kHz since the LF current quality study is limited to 2 kHz, shows that the TF behaves as a second order system (Fig.I.19). A resonance is depicted at 410 Hz and the frequencies between 100 Hz and 570 Hz are amplified.

$$TFi(s) = \frac{i_g(s)}{i_f(s)} = \frac{Z_C}{Z_C + m^2 \cdot Z_g + Z_{leak} + Z_{L_f}} \quad \text{eq. (I.23)}$$

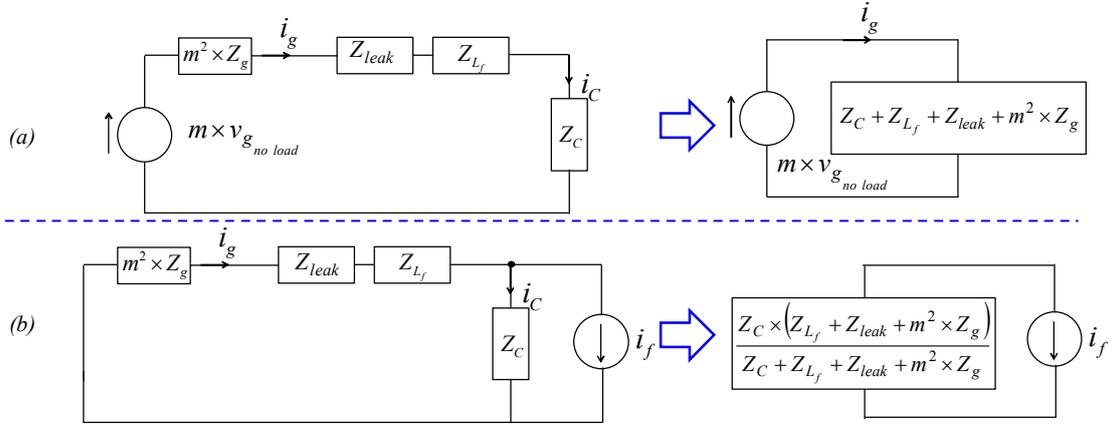


Fig.I.18. (a) Series resonance of the input filter due to the supply voltage harmonics. (b) Parallel resonance of the input filter due to the rectifier's input current harmonics.

2.2.2. Low frequency impact of the supply voltage

Equation eq. (I.24)) defines the expression of the TF between the grid current and the supply voltage at no-load condition at the secondary of the auto-transformer. The Bode diagram of Fig.I.19 shows that the input filter attenuates the harmonics of the supply voltage of at least 15 dB.

$$TFv(s) = \frac{i_g(s)}{m \cdot v_{g_{no\ load}}(s)} = \frac{1}{Z_C + m^2 \cdot Z_g + Z_{leak} + Z_{L_f}} \quad \text{eq. (I.24)}$$

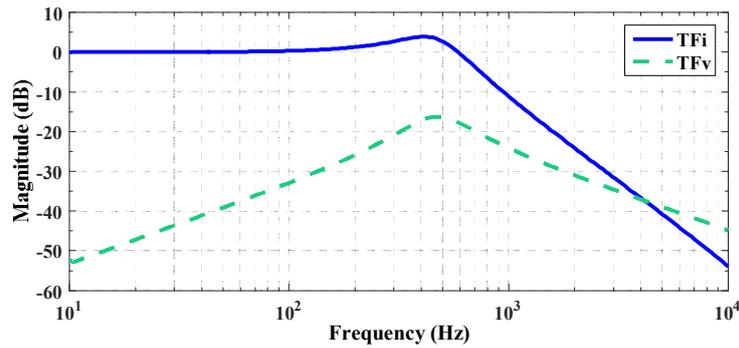


Fig.I.19. Bode diagram magnitude of TFi (blue) and TFv (green).

2.2.3. Analysis

The DM model of the input stage is used in four different study cases. These studies are carried out under the experimental conditions established in Table I.2. The value of the DM filtering inductor is exaggerated (i.e. the DM filtering inductor used on-board the vehicle is multiplied by a ratio of 5 to 1) in order to clearly demonstrate the LF resonance of the input stage.

All the study cases consist in the injection of a DM current i_f and a no-load supply voltage. Afterwards, the LF content of the resulting grid current is compared to that of the grid current measured on the test bench. The study cases are designed in order to allow for the evaluation of the impact that a certain criteria has on the LF harmonics of the grid current.

- Case I: Evaluation of the impact of the zero levels (without the switching component).
- Case II: Evaluation of the impact of the zero levels associated with the switching component.
- Case III: Evaluation of the impact of the supply voltage harmonics (polluted mains).
- Case IV: Evaluation of the impact of the zero levels in case of an ideal supply voltage (unpolluted mains).

The comparison of the harmonic content of the grid current calculated in cases I and II shows that the switching at 10 kHz presents little impact on the LF harmonics (Fig.I.20). On the other hand, case IV, which is carried out for a purely sinusoidal grid voltage, shows that the LF harmonics of the i_f current (mainly due to zero levels) excite the resonance of the input filter (Fig.I.21). In addition, the quality factor of the filter makes it possible to define the range of frequencies amplified by the filter. However, the harmonics of the supply voltage are attenuated by the input filter and their impact on the quality of the mains current is limited with regards to the contribution of the zero levels (case III).

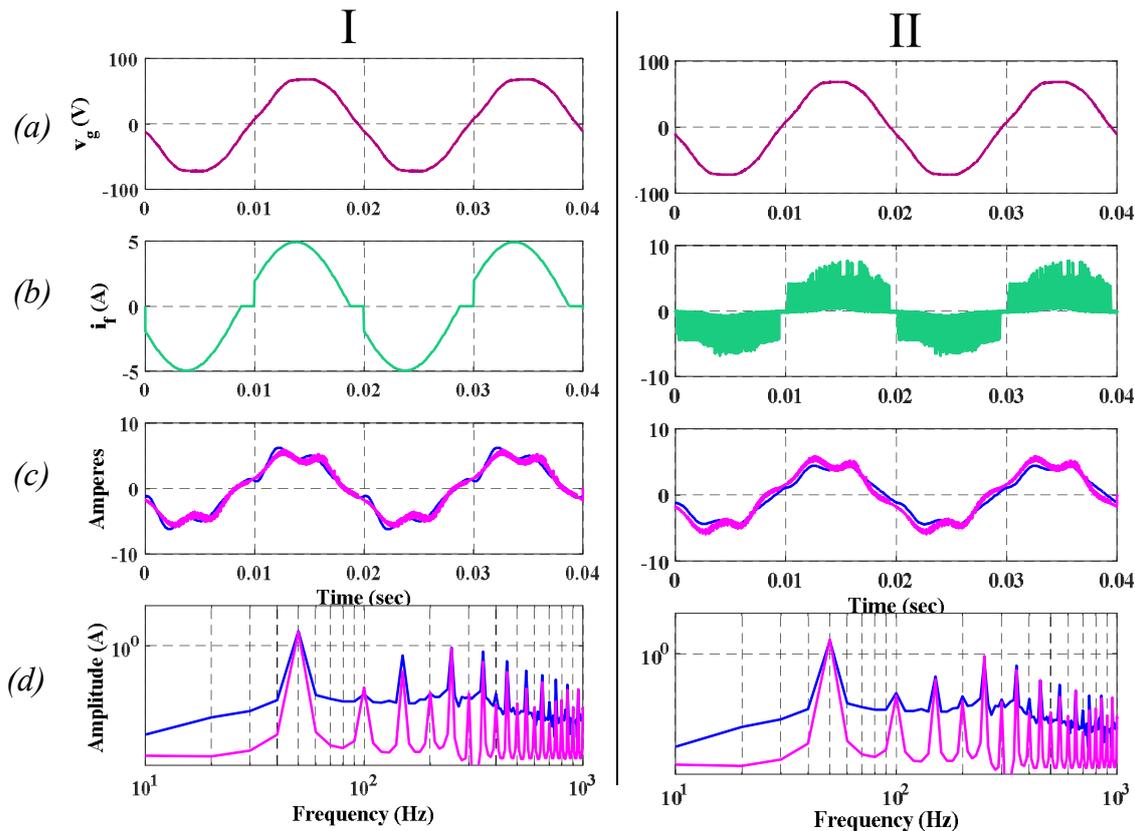


Fig.I.20. Study of the impact of the switching and the zero levels on the LF content of the mains current. (a) Supply voltage measured at the secondary side of the auto-transformer. (b) DM current of the charger: (I) purely theoretical with zero levels, (II) actual measurement on test bench. (c) Grid current measured on bench (pink), calculated grid current (blue). (d) LF harmonic content of the grid current measured on the test bench (pink) and the calculated grid current (blue).

Thus, the zero levels of current i_f resulting from the correction of the displacement angle, behave as a step-like excitation source which causes a damped oscillatory response of the input filter. The literature examines only the impact of switching on the LF harmonics of the grid current. However, since the switching frequency of the charger is at 10 kHz, the LF impact associated with the switching is relatively limited.

TABLE I.2. PARAMETERS USED FOR THE STUDY OF THE INPUT STAGE

Symbol	Description	Value (Unit in SI)
V_{gm}	Amplitude of the AC mains voltages	$50\sqrt{2}$ (V)
m	Transformation ratio	0.22
I_L	Current measurement through L_{eq}	7 (A)
f_{sw}	Switching frequency	10 (kHz)
φ^*	Displacement angle reference	30°

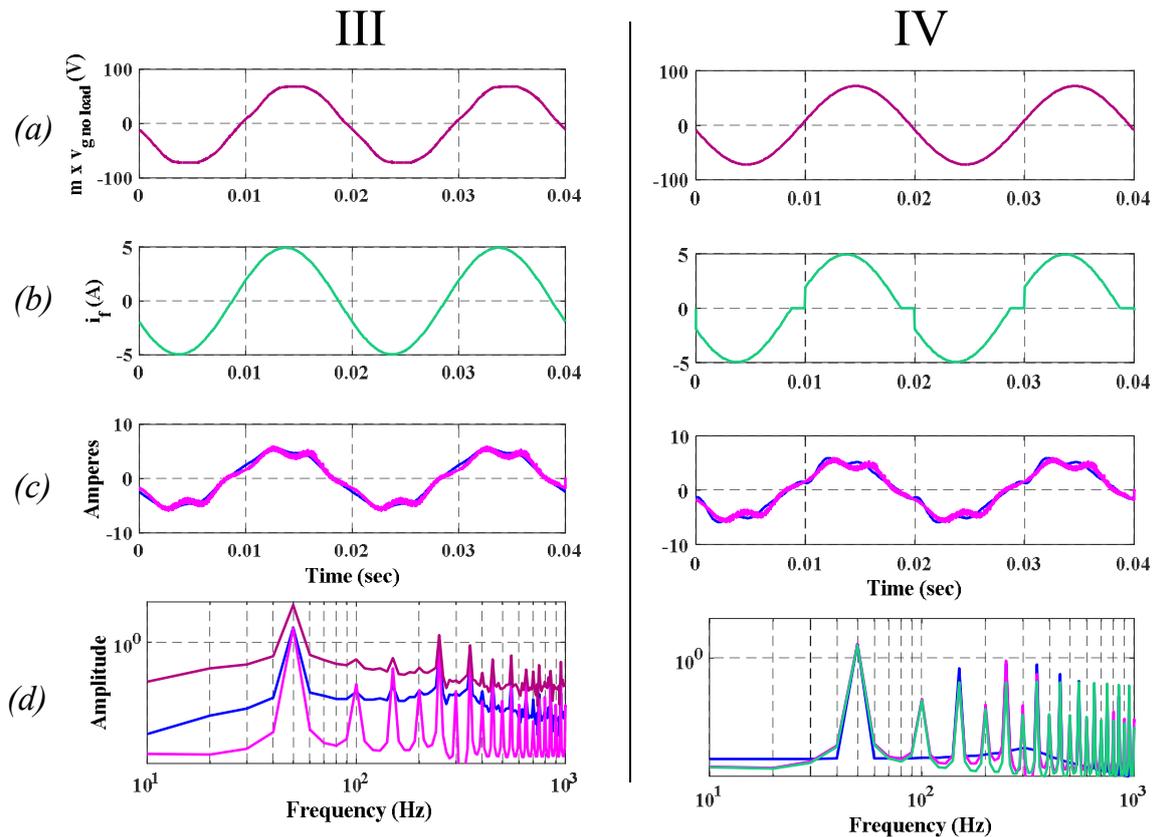


Fig.I.21. Study of the impact of the LF harmonic content of the network (III) and the LF harmonics absorbed by the charger (IV). (a) Supply voltage: measured under no-load condition at the secondary side of the auto-transformer (III), unpolluted (IV). (b) DM current of the charger: unpolluted (III), purely theoretical with the zero levels (IV). (c) Grid current measured on test bench (pink), calculated grid current (blue). (d) LF harmonic content: of the grid current measured on a bench (pink), of the calculated grid current (blue), of the supply voltage measured under no-load condition (red) and of the input current with zero levels (green).

In conclusion, equation eq. (I.25)) shows that the quality of the mains current is essentially governed by the harmonic content of the i_f current and by the resonance frequency of the input filter.

$$i_g(s) = TF_i(s) \cdot i_f(s) + TF_v(s) \cdot m \cdot v_{g_{noload}} \quad \text{eq. (I.25)}$$

2.3. Proposed active damping solution

Power quality solutions are of great interest for electric car manufacturers. Battery chargers for EVs need to be compliant with the IEC's international standards on electromagnetic compatibility which define the limits for harmonic current emissions up to 2 kHz. The grid current's distortion, as analysed in the previous section, can lead to non-compliance with the above-defined standards. For that reason, an active damping with resonance frequency tracking solution is proposed.

2.3.1. Active damping

In order to attenuate the input filter's resonance, an obvious solution would be the use of passive damping. However, the extra physical resistor required leads to additional costs, higher losses and reduced efficiency.

Several methods for resonance harmonic mitigation have been studied in literature [Peña-Alzola et al. 2014] – [Zhang et al. 2015]. Harmonic injection methods, notch filtering that compensates the resonance frequency gain, lead/lag phase compensators as well as selective harmonic elimination techniques are widely employed. However, most of these methods require calibration efforts and extra sensors. In order to enhance the quality of the current drawn from the grid, an active damping solution is proposed. Active damping control uses the rectifier in order to emulate the presence of a virtual resistor in the input filter. [Liserre et al. 2004] and [Wiseman et al. 2005] study different active damping scenarios for three-phase active rectifiers. The optimal placement for the damping resistor, in our case, is in parallel to the input capacitor.

a. Effect on the DPFC scheme

The placement of the virtual damping resistor could vary between series and/or parallel to the input filter's inductor and/or capacitor. Several factors need to be taken into account when choosing an optimal damping strategy.

Table II.3 summarizes the differences between the various possibilities in terms of sensors needed and control implementation. For the application at hand, in order to make use of the sensors already employed to measure the grid current and converter voltage, two configurations are possible: either in series with the grid impedance or in parallel with the filter capacitor. Based on control complexity, the optimal placement would be in parallel with the capacitor which translates at the implementation level into a frequency invariant term to be added to the control as opposed to the need for a differentiator [Dahono 2002].

The virtual resistor (R_v) placed in parallel with the input capacitor reduces the current that is flowing into the capacitor by a value that is proportional to the converter's voltage. We solely use the harmonic component of the capacitor's voltage v_{ch} to compute the required damping current (Fig.I.22).

TABLE II.3. COMPARISON BETWEEN DIFFERENT PLACEMENT SOLUTIONS FOR VIRTUAL DAMPING RESISTOR

Filter element	Placement of resistor	Measurement needed	Control structure	+ Advantages - Disadvantages
Inductor	Parallel	Inductor voltage		+ Simple gain added to the control - Additional voltage sensor or estimator
	Series	Grid current		- Differentiator added to the control + Existing current sensor is used
Capacitor	Parallel	Converter voltage		+ Simple gain added to the control + Existing voltage sensor is used
	Series	Capacitor current		- Differentiator added to the control - Additional voltage sensor or estimator

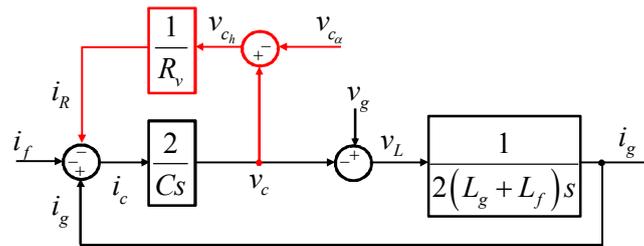


Fig.I.22. Block diagram of the damped input filter using the converter voltage harmonics.

This avoids the injection of an active power that will interfere with the current control. The harmonic extraction method needs to be insensitive to variations in the grid frequency. This is usually achieved in the dq-frame through high pass filtering which eliminates the DC component [Wu 2006]. The latter represents the fundamental of the signal; therefore, the remaining is the dq-component of the harmonics.

However, since our control scheme's SOGI filter is adaptive to frequency variations and introduces no additional delay to the extraction of the fundamental, the voltage harmonics are calculated by subtraction of the fundamental from the measured signal.

Furthermore, a low pass filter places an upper limit on the voltage harmonic frequencies to be injected. In order to respect the system dynamics and allow the carrier signal to incorporate the harmonic frequencies in the pulse width modulation process; those frequencies should be limited at least to one sixth of the switching frequency. Fig.I.23 shows the modifications brought to the previous DPFC to account for the active damping of the input filter's resonance.

method based on extended Kalman filter was proposed in [Hoffmann et al. 2014]; however, this method requires computational efforts.

In this study we decide to make use of the input filter's periodical resonance to estimate the grid's impedance. For that reason, an online Discrete Fourier Transform (DFT) algorithm based on a running summation is developed to track the resonance frequency and adjust the damping resistor value online during charging. This results in a self-tuning active damping scheme.

2.3.2. *Self-tuning active damping based on an online running summation DFT*

With the wide deployment of residential charging stations, EVs' chargers need to maintain their stability and compliance with the standards. However, the variability of the grid's impedance from one charging station to the other, leads to the variation of the resonance frequency and with it the variation of the adequate damping resistor value.

The approach developed for the determination of this value consists in finding the optimal damping for each detected resonance; as a result the determination of the grid's impedance is required. Taking advantage of the periodical resonance phenomenon appearing on the converter voltage, the proposed method is an online DFT with a running summation that tracks the resonance frequency variations.

The running summation principle was first introduced in [Asiminoaei et al. 2005]; however, the approach was applied to a single known inter-harmonic frequency corresponding to an external signal injected into the system. The main disadvantage of such method is related to the choice of the injection signal's amplitude which needs to be high enough to be detected but low enough so it doesn't affect the overall system stability. The running summation algorithm is a digital implementation of the well-known DFT expressions. Fig.I.25 shows the general concept of the algorithm with A_n (eq. (I.28)) and B (eq. (I.29)) being sampling time (T_{sa}) dependent DFT coefficients. It consists of analyzing the harmonic content, up to the 40th rank, of the measured grid current or converter voltage in order to extract the rank of the harmonic presenting the highest amplitude. This harmonic is considered to be the closest multiple of the fundamental period to the actual resonance. However, this renders the algorithm dependent on external grid disturbances with amplitudes higher than the resonance frequency's. The algorithm's flowchart is given hereafter:

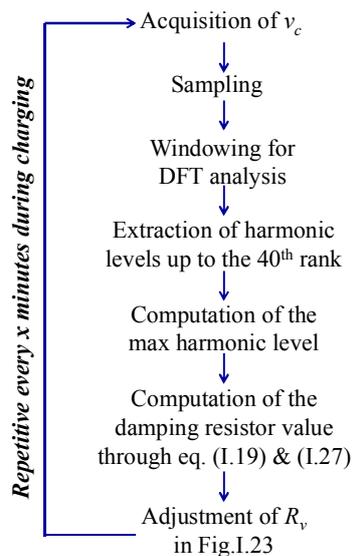


Fig.I.24. Online DFT algorithm flowchart that shows the self-tuning capability of the active damping.

$$A_n = \frac{2\pi \cdot T_{sa} \cdot n}{T_g} ; \text{ with } n \text{ being the running summation variable} \quad \text{eq. (I.28)}$$

$$B = \frac{2 \cdot T_{sa}}{T_g} ; \text{ with } T_g = \frac{2\pi}{\omega_{pll}} \quad \text{eq. (I.29)}$$

Two cases can be distinguished:

- Transient grid disturbances higher than the resonance: the distinction between such distortions and the periodic resonance of the input filter can be achieved through increasing the number of periods (widening the window) chosen for the analysis.
- Permanent grid disturbances higher than the resonance: The algorithm will detect the harmonic closer to this distortion and treat it as a fictitious resonance for which an equivalent grid impedance and a corresponding damping resistor value are computed. Thus, both the resonance frequency and the distortion will be attenuated.

The algorithm is repetitive during charging and adjusts online the value of the damping resistor of Fig.I.23. A drawback of this method is that the computational efforts increase with the number of harmonic ranks to be analysed. Co-simulations between Matlab and Psim are carried and the results, with the system parameters of Table I.1, are presented in Fig.I.26 where the DFT algorithm is activated at 0.33 seconds into charging. Furthermore, simulations under different grid impedance conditions show the effectiveness of the damping scheme developed (Fig.I.27).

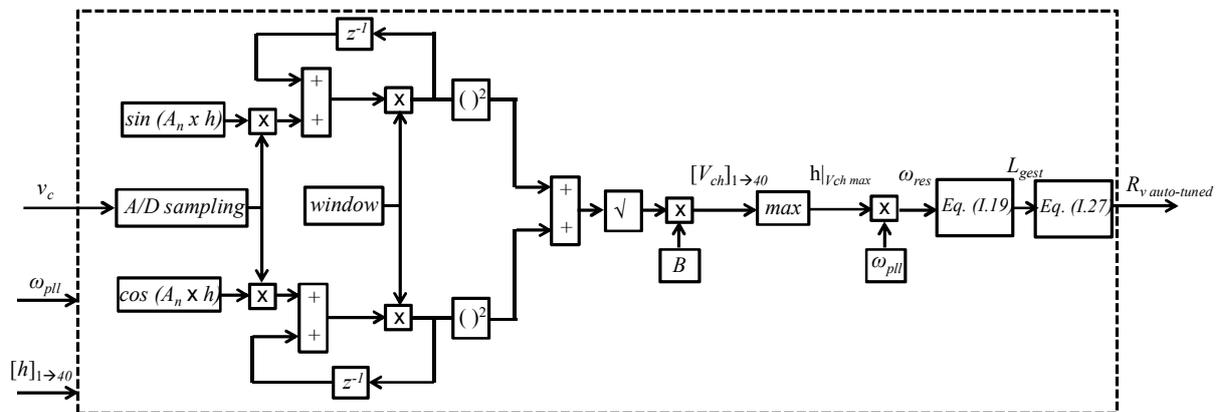


Fig.I.25. Online DFT algorithm based on a running summation and generating a self-tuning damping resistor value.

Let us consider the example of an input stage consisting of a DM filtering inductor of 1 mH, a DM filtering capacitor of 35 μ F, a damping factor ζ of 0.707 (chosen in order to have a damped second order oscillatory response without overshooting while preserving good dynamics) and a grid inductance varying between 50 μ H and 2 mH. In this case, the value of the virtual resistor, as computed by the DFT algorithm, varies between 7.7 Ω and 13 Ω respectively.

These values would have resulted in a bulky physical resistor to be placed in parallel with the input filter's capacitors as well as high power losses. This justifies the use of alternative methods based on active damping using a virtual damping resistor.

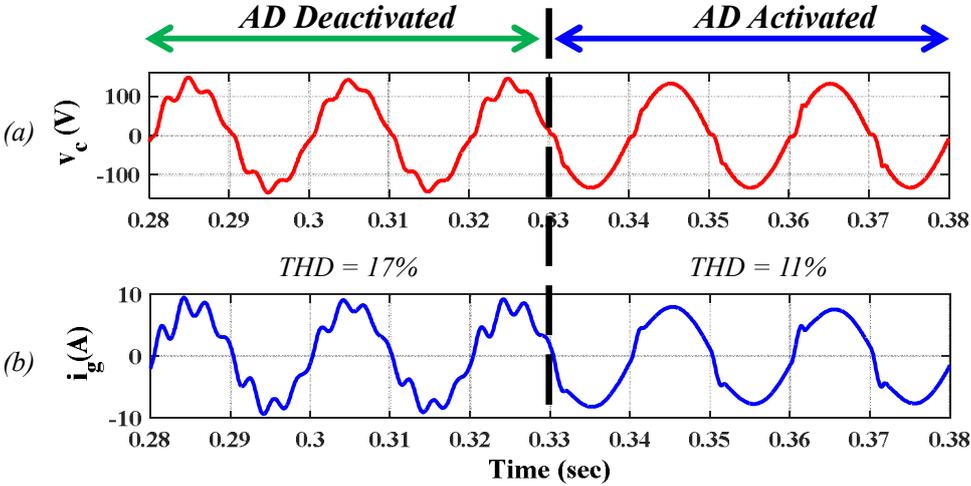


Fig.I.26. Simulation results of the active damping (AD) associated with resonance frequency tracking. (a) Converter voltage before and after AD. (b) Grid current before and after activation of the damping at 0.33s.

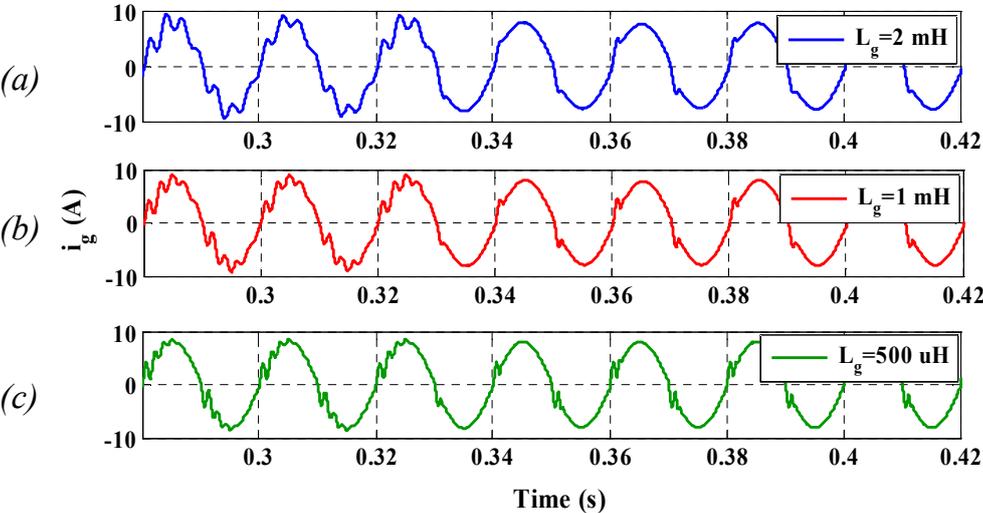


Fig.I.27. Simulation results of the active damping associated with resonance frequency tracking activated at 0.33s for different grid impedance values.

3. Converter dynamics & control

It is inevitable to study the converter dynamics for the design of a current controller with good performances.

3.1. Two distinct modes of operation

The PFC strategy that we aim at optimizing controls both the CSAR and the Boost via pulse width modulation; which means that the semi-conductors of both converters are continuously switching over a mains fundamental period. This leads to high switching power losses and conducted common mode emissions.

However, in the new proposed strategy, in order to fully exploit the advantages of the Buck-Boost topology, the control developed ensures two modes of operation [Ridley et al. 1993] – [Fuld et al. 1993]. On one hand, when the converter voltage level v_c is lower than that of the battery v_{batt} , a voltage step up is required. Hence, the Boost is activated via average current control meanwhile; the Buck-type rectifier is maintained in the ON position and serves the role of a current full wave rectifier. This will be called Boost Mode operation. On the other hand, when the maximum value of the converter voltage is higher than the battery's, a voltage step down is required. Therefore, the Buck-type rectifier is activated via average current control meanwhile; the Boost is maintained in the OFF position and serves only for current flow to the battery (Fig.I.28). This will be called Buck Mode operation.

Table I.4 summarizes the switching states. The low-side switches of the CSAR are maintained ON in order to reduce the switching power losses.

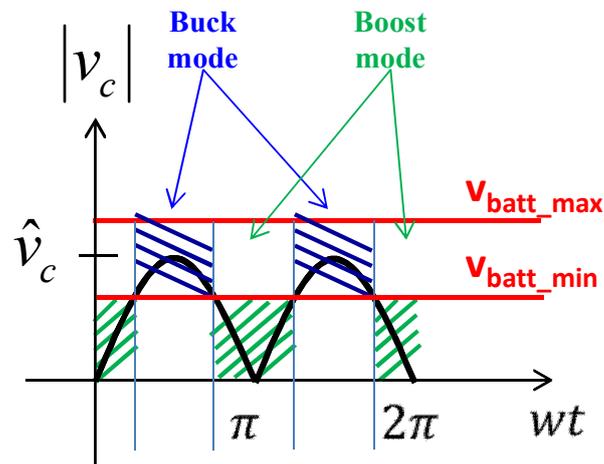


Fig.I.28. Detection of the dual modes of operation depending on the levels of the converter voltage and the battery's measured voltage.

Table I.4. SWITCH CONTROL STRATEGY FOR THE TWO MODES OF OPERATION

Mode of operation	Converter current polarity	Switching States				
		T_{1H}	T_{2H}	T_{1L}, T_{2L}	T_{bL}	T_{bH}
Boost $ vc \leq v_{batt}$	$i_f \geq 0$	ON	OFF	ON	PWM	OFF
	$i_f < 0$	OFF	ON	ON	PWM	OFF
Buck $ vc > v_{batt}$	$i_f \geq 0$	PWM	OFF	ON	OFF	OFF
	$i_f < 0$	OFF	PWM	ON	OFF	OFF

3.2. Proposed current control strategy

The proposed control structure is presented in Fig.I.29. It is based on the control of the current i_L flowing through the filtering inductor of the dc-bus.

The displacement power factor correction loop associated to the active damping generates the converter current's reference i_f^* with the adequately computed phase-lag α^* and the virtual resistor current i_{Rv}^* .

$$i_f^* = \hat{I}_f \cdot \sin(\omega t + \alpha^*) + i_{Rv}^* \quad \text{eq. (I.30)}$$

Eventually an electromagnetic interference (EMI) filter is going to be added between the grid and the converter; therefore, the desired amplitude of the converter current \hat{I}_f is not imposed but rather computed by a PI controller (represented in blue). The role of the controller is to regulate the amplitude of the mains current which is kept at a level proportional to the desired charging power P^* eq. (I.31)). The latter is dictated by the charge profile of the battery [Marra et al. 2012].

$$\hat{I}_g = \frac{P^* \cdot \sqrt{2}}{V_{c_{RMS}}} \quad \text{eq. (I.31)}$$

For obtaining the desired inductor current, two cases can be distinguished according to the mode of operation:

- *Boost-Mode*: in this case the rectifier is kept turned-on. Hence, it is equivalent to a 4 diode rectifier bridge which means that the inductor current is equal to the rectified converter current.
- *Buck-Mode*: in this case the Boost is maintained in turn-off position and the rectifier is controlled via PWM. Therefore, the inductor current is proportional to the rectified converter current with a ratio equal to the Buck-type rectifier's duty cycle s_{bck} .

In order to sum up, the value of the desired inductor current i_L^* is computed using i_f^* as following:

$$\begin{aligned}
& \text{if } v_{c_\alpha} \leq v_{batt} \\
& \quad i_L^* = |i_f^*| \\
& \text{else} \\
& \quad i_L^* = \frac{|i_f^*|}{s_{bck}} \quad ; \quad \text{with } s_{bck} = \frac{v_{batt}}{|v_{c_\alpha}|}
\end{aligned}
\tag{I.32}$$

It should be noted that this PFC strategy employs the same number of current and voltage sensors defined by the industrial specifications. Therefore, the value of the reference for the inductor current correction loop i_L^* is estimated from the signal $|i_f^*|$. An outer current correction loop based on the measurement of i_f is not considered because this signal contains components at the switching frequency (10 kHz). Its measurement requires a current sensor with sufficient bandwidth which leads to higher costs.

The average current control of i_L consists of an inductor current loop. The modulation signal at the output of the controller V_{saw} is compared to two 10 kHz saw tooth carriers with different offsets. The comparisons generate the pulse width modulated duty cycles for the CSAR and the Boost. The two offsets are chosen in order to allow for an automatic detection of the Buck or Boost mode of operation.

The design of the control loop and the saw tooth signals is based on linear control. Therefore, the small-signal AC equivalent circuit modeling is used to extract the converters transfer functions around a steady-state operating point. Around the operating point, the studied converter topology is shown in Fig.I.31 (a).

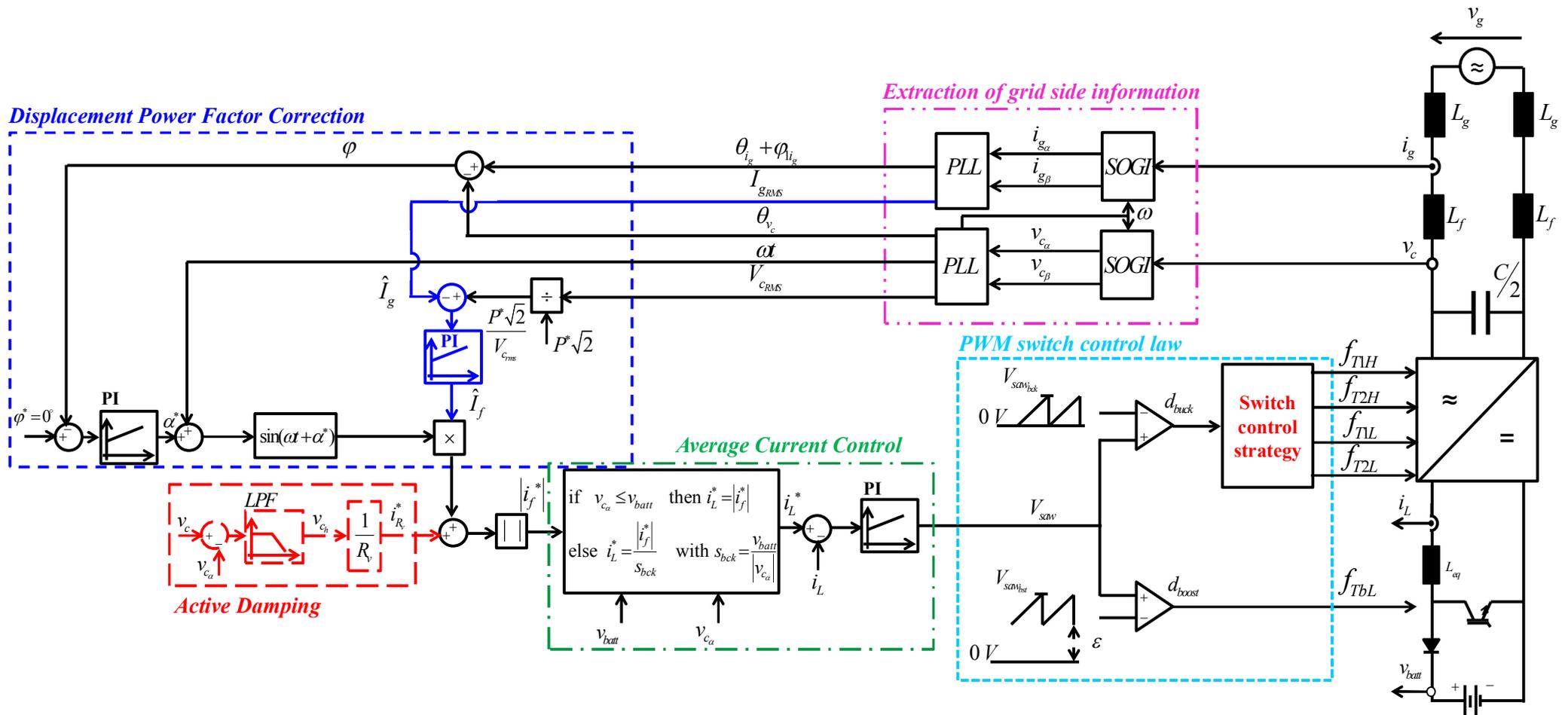


Fig.I.29. Global PFC strategy including a dual-mode current control loop associated with the DPFC scheme and the active damping control.

3.3. Converter dynamics

In order to establish the small-signal analysis of the charger, the input rectifier's properties are considered to be equivalent to those of a single-phase diode bridge followed by a dc-dc Buck converter as shown in Fig.I.30.

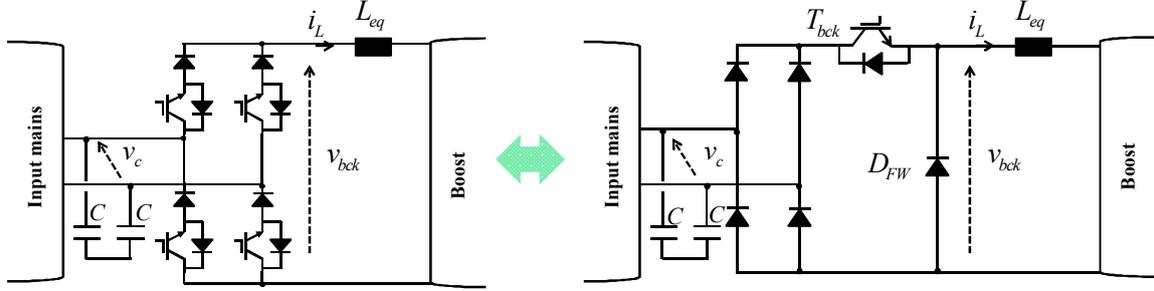


Fig.I.30. Equivalent power circuit model of the single-phase rectifier used for establishing the small-signal analysis.

3.3.1. Averaged model

In this section, let s_{bck} and s_{bst} denote the switching functions of T_{bck} and T_{bst} respectively. Consequently, over one switching period T_{sw} , the IGBTs' duty cycles are referred to as d_{bck} and d_{bst} . Depending on the mode of operation, the converter is represented by the following averaged equations:

$$\begin{cases} \text{Buck Mode: } L_{eq} \cdot \frac{di_L}{dt} = d_{bck} \cdot v_{in} - v_{bst} \\ \text{Boost Mode: } L_{eq} \cdot \frac{di_L}{dt} = v_{bck} - (1 - d_{bst}) \cdot v_{batt} \end{cases} \quad \text{eq. (I.33)}$$

a. Small-signal equivalent circuit model

The small signal analysis of the converter allows for the linearization around a given operating point. Therefore, applying the first order small-signal linearization by replacing each variable y by its variation \tilde{y} around a steady-state value Y , yields:

$$\begin{cases} \text{Buck Mode: } \begin{cases} L_{eq} \cdot \frac{d\tilde{i}_L}{dt} = D_{bck} \cdot \tilde{v}_{in} + V_{in} \cdot \tilde{d}_{bck} - \tilde{v}_{bst} \\ \tilde{i}_{in} = D_{bck} \cdot \tilde{i}_L + I_L \cdot \tilde{d}_{bck} \end{cases} \\ \text{Boost Mode: } \begin{cases} L_{eq} \cdot \frac{d\tilde{i}_L}{dt} = \tilde{v}_{bck} - (1 - D_{bst}) \cdot \tilde{v}_{batt} + V_{batt} \cdot \tilde{d}_{bst} \\ \tilde{i}_{batt} = (1 - D_{bst}) \cdot \tilde{i}_L - I_L \cdot \tilde{d}_{bst} \end{cases} \end{cases} \quad \text{eq. (I.34)}$$

Based on eq. (I.34)), the small-signal model of the charger is given in Fig.I.31 (b).

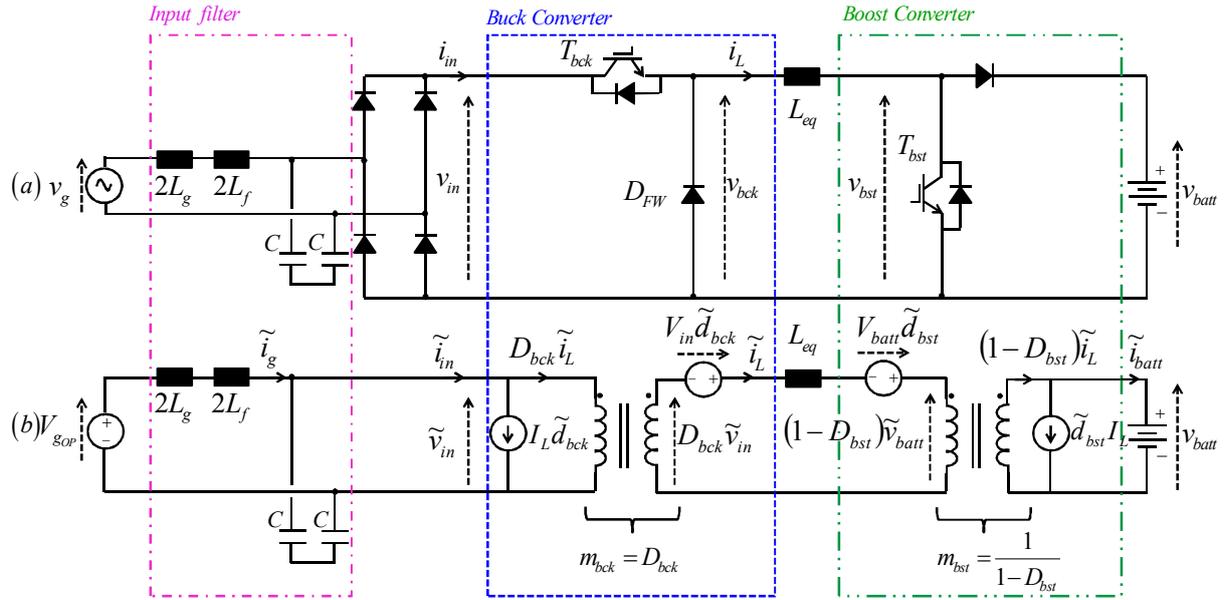


Fig.I.31. Small-signal equivalent circuit model of the converter. (a) Equivalent topology of the charger at a given operating point. (b) Small-signal averaged equivalent model of the charger.

b. Converter transfer functions

Taking into consideration the very slow dynamics of the battery with regards to the controlled variables; the variation of the battery's voltage can be neglected. Furthermore, the variations of the grid's and battery's voltages are considered as external system disturbances. In this preliminary analysis, the transfer functions are deduced without the effect of the input filter. Hence, the input filter's output impedance denoted by Z_f is neglected. Based on eq. (I.34)), for each mode of operation, the transfer function between the inductor current and the duty cycle can be expressed as:

$$\begin{aligned}
 \text{Buck Mode: } G_{i_L d_{bck}}(s) \Big|_{Z_f(s)=0} &= \frac{\tilde{i}_L}{\tilde{d}_{bck}}(s) = \frac{V_{in}}{L_{eq} \cdot s} \\
 \text{Boost Mode: } G_{i_L d_{bst}}(s) \Big|_{Z_f(s)=0} &= \frac{\tilde{i}_L}{\tilde{d}_{bst}}(s) = \frac{V_{batt}}{L_{eq} \cdot s}
 \end{aligned}
 \tag{I.35}$$

The transfer function of the inner control loop between the inductor current i_L and V_{saw} can be expressed as a function of the saw tooth amplitudes as follows:

$$\begin{aligned}
 \text{Buck Mode: } G_{i_L V_{saw}}(s) &= \frac{\tilde{i}_L}{\tilde{V}_{saw}}(s) = \frac{V_{in}}{L_{eq} \cdot s} \times \frac{1}{V_{saw_{bck}}} \\
 \text{Boost Mode: } G_{i_L V_{saw}}(s) &= \frac{\tilde{i}_L}{\tilde{V}_{saw}}(s) = \frac{V_{batt}}{L_{eq} \cdot s} \times \frac{1}{V_{saw_{bst}}}
 \end{aligned}
 \tag{I.36}$$

The amplitudes of the saw tooth signals are chosen to ensure feed-forward of the external disturbances. Hence, the Buck's saw tooth signal needs to be proportional to the input voltage's amplitude; thus, ensuring feed-forward of the input. However, the Boost's saw tooth signal needs to be proportional to the output battery's voltage. Moreover, in order to render the transfer function independent of the mode of operation, the same factor of proportionality $k=0.01$ is chosen for both converters as seen in the following equations:

$$\begin{aligned} V_{saw_{bck}} &= k \times V_{in} \\ V_{saw_{bst}} &= k \times V_{batt} \end{aligned} \quad \text{eq. (I.37)}$$

Consequently, the control to inductor current transfer function can be expressed:

$$G_{i_L V_{saw}}(s) = \frac{1/k}{L_{eq} \cdot s} \quad \text{eq. (I.38)}$$

Furthermore, the offset denoted by ε is chosen to ensure the detection of the adequate mode of operation.

$$\varepsilon = k \times v_{in} \quad \text{eq. (I.39)}$$

In order to reduce the distortion due to the non-linearity of the mode changes between Buck mode and Boost mode; the offset can be reduced so as to ensure a Buck mode and a Buck-Boost mode of operation.

3.3.2. Input filter & control interactions

The choice of the input filter is a critical design step for the converter. The input filter could affect the dynamics of the converter which can lead to control instability. The filter is taken into consideration by adding to eq. (I.34)) the following equations:

$$\begin{cases} L \cdot \frac{d\tilde{i}_g}{dt} = \tilde{v}_g - \tilde{v}_{in} \\ \frac{C}{2} \cdot \frac{d\tilde{v}_{in}}{dt} = \tilde{i}_g - D_{bck} \cdot \tilde{i}_L - I_L \cdot \tilde{d}_{bck} \end{cases} ; \text{ where } L = 2 \cdot (L_g + L_f) \quad \text{eq. (I.40)}$$

The state-space representation of the converter including the input filter can be expressed as: (The bold characters indicate that the variables are matrices)

$$\begin{aligned} \dot{\tilde{\mathbf{x}}} &= \mathbf{A} \cdot \tilde{\mathbf{x}} + \mathbf{B} \cdot \tilde{\mathbf{d}} + \mathbf{P} \cdot \tilde{\mathbf{v}} \\ \text{With, } \tilde{\mathbf{x}} &= [\tilde{i}_L, \tilde{i}_g, \tilde{v}_{in}]^T, \quad \tilde{\mathbf{d}} = [\tilde{d}_{bck}, \tilde{d}_{bst}]^T, \quad \tilde{\mathbf{v}} = [\tilde{v}_g, \tilde{v}_{batt}]^T \end{aligned}$$

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & \frac{D_{bck}}{L_{eq}} \\ 0 & 0 & -\frac{1}{L} \\ -\frac{2 \cdot D_{bck}}{C} & \frac{2}{C} & 0 \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} \frac{V_{in}}{L_{eq}} & \frac{V_{batt}}{L_{eq}} \\ 0 & 0 \\ -\frac{2 \cdot I_L}{C} & 0 \end{bmatrix}, \quad \mathbf{P} = \begin{bmatrix} 0 & -\frac{(1-D_{bst})}{L_{eq}} \\ \frac{1}{L} & 0 \\ 0 & 0 \end{bmatrix} \quad \text{eq. (I.41)}$$

The application of the Laplace transform to this linear system yields:

$$\tilde{\mathbf{x}}(s) = (s \cdot \mathbf{I}_3 - \mathbf{A})^{-1} \cdot \mathbf{B} \cdot \tilde{\mathbf{d}}(s) + (s \cdot \mathbf{I}_3 - \mathbf{A})^{-1} \cdot \mathbf{P} \cdot \tilde{\mathbf{v}}(s) \quad \text{eq. (I.42)}$$

With \mathbf{I}_3 being the 3-by-3 identity matrix and:

$$(s \cdot \mathbf{I}_3 - \mathbf{A})^{-1} = \frac{1}{\det(s \cdot \mathbf{I}_3 - \mathbf{A})} \text{com}(s \cdot \mathbf{I}_3 - \mathbf{A})$$

$$= \frac{1}{s^3 + \left(\frac{2}{L \cdot C} + \frac{2 \cdot D_{bck}^2}{L_{eq} \cdot C} \right) \cdot s} \cdot \begin{bmatrix} \left(s^2 + \frac{2}{L \cdot C} \right) & \left(-\frac{2 \cdot D_{bck}}{L_{eq} \cdot C} \right) & \left(\frac{D_{bck}}{L_{eq}} \cdot s \right) \\ \left(\frac{2 \cdot D_{bck}}{L \cdot C} \right) & \left(s^2 + \frac{2 \cdot D_{bck}^2}{L_{eq} \cdot C} \right) & \left(-\frac{s}{L} \right) \\ \left(\frac{2 \cdot D_{bck}}{C} \cdot s \right) & \left(\frac{2}{C} \cdot s \right) & \left(s^2 \right) \end{bmatrix} \quad \text{eq. (I.43)}$$

The systems' transfer functions that interest us are extracted from eq. (I.42)):

$$G_{i_L d_{bck}}(s) = \left. \frac{\tilde{i}_L}{\tilde{d}_{bck}}(s) \right|_{\substack{\tilde{d}_{bst}(s)=0 \\ \tilde{v}_g(s)=0 \\ \tilde{v}_{batt}(s)=0}} = \frac{V_{in}}{L_{eq} \cdot s} \times \left(\frac{s^2 - \frac{2 \cdot I_L \cdot D_{bck}}{C \cdot V_{in}} \cdot s + \frac{2}{L \cdot C}}{s^2 + \frac{2}{L \cdot C} + \frac{2 \cdot D_{bck}^2}{L_{eq} \cdot C}} \right) \quad \text{eq. (I.44)}$$

$$G_{i_L d_{bst}}(s) = \left. \frac{\tilde{i}_L}{\tilde{d}_{bst}}(s) \right|_{\substack{\tilde{d}_{bck}(s)=0 \\ \tilde{v}_g(s)=0 \\ \tilde{v}_{batt}(s)=0}} = \frac{V_{batt}}{L_{eq} \cdot s} \times \left(\frac{s^2 + \frac{2}{L \cdot C}}{s^2 + \frac{2}{L \cdot C} + \frac{2 \cdot D_{bck}^2}{L_{eq} \cdot C}} \right) \quad \text{eq. (I.45)}$$

The input filter's output impedance is expressed as:

$$Z_f(s) = \frac{L \cdot s}{\frac{L \cdot C}{2} \cdot s^2 + 1} \quad \text{eq. (I.46)}$$

By combining eq. (I.35)) and eq. (I.46)), the equations eq. (I.44)) and eq. (I.45)) can be rewritten as follows:

$$G_{i_L d_{bck}}(s) = G_{i_L d_{bck}}(s) \Big|_{Z_f(s)=0} \times \left(\frac{1 + \frac{Z_f(s)}{Z_{N_{bck}}(s)}}{1 + \frac{Z_f(s)}{Z_D(s)}} \right) \quad \text{eq. (I.47)}$$

$$G_{i_L d_{bst}}(s) = G_{i_L d_{bst}}(s) \Big|_{Z_f(s)=0} \times \left(\frac{1 + \frac{Z_f(s)}{Z_{N_{bst}}(s)}}{1 + \frac{Z_f(s)}{Z_D(s)}} \right) \quad \text{eq. (I.48)}$$

$$\text{With, } Z_D(s) = \frac{L_{eq} \cdot s}{D_{bck}^2}, Z_{N_{bck}}(s) = -\frac{V_{in}}{D_{bck} \cdot I_L}, Z_{N_{bst}}(s) \rightarrow \infty$$

The stability analysis is based on R. D. Middlebrook's Extra Element Theorem [Erickson et al. 2004]. According to the theorem, the control to inductor current modified transfer function can be expressed as:

$$G_{i_{Ld}}(s) = \left(G_{i_{Ld}}(s) \Big|_{Z_f(s)=0} \right) \times \left(\frac{1 + \frac{Z_f(s)}{Z_N(s)}}{1 + \frac{Z_f(s)}{Z_D(s)}} \right) \quad \text{eq. (I.49)}$$

$$\text{With, } Z_D(s) = \frac{\tilde{v}_{in}}{\tilde{i}_{in}}(s) \Big|_{\substack{\tilde{d}_{bck}(s)=0 \\ \tilde{d}_{bst}(s)=0}}, \quad Z_N(s) = \frac{\tilde{v}_{in}}{\tilde{i}_{in}}(s) \Big|_{\tilde{i}_{L}(s) \rightarrow 0}$$

$Z_N(s)$ and $Z_D(s)$ are the input impedances of the converter under ideal closed loop control and open loop control conditions respectively. When the following inequalities are verified, the input filter does not substantially alter the control to inductor current transfer function:

$$\begin{aligned} \|Z_f(s)\| &\ll \|Z_N(s)\| \\ \|Z_f(s)\| &\ll \|Z_D(s)\| \end{aligned} \quad \text{eq. (I.50)}$$

If the grid impedance is not taken into consideration, then we can write $L=2L_f$. Fig.I.32 shows that for both modes of operation, the inequalities are not verified. Therefore, eq. (I.35)) are not sufficient for adequate controller design. The effect of the filter on the control stability must be considered; hence, eq. (I.47)) and eq. (I.48)) should be used for the computation of the inner loop controller. On another hand, this shows the need to passively damp the DM filter for no-load operation of the plugged in charger.

3.3.1. Grid impedance variation effect

The Bode plots of the control to inductor current transfer functions eq. (I.47)) and eq. (I.48)) around an operating point and for grid impedances varying between 50μH and 2mH, as specified by Renault, are given in Fig.I.33.

Note that the peaks should be damped through the equivalent series resistors of the inductors and capacitors that aren't taken into account for this analysis. Since the DM inductor of an integrated charger has a low value of 80μH, the filter resonance is greatly influenced by the variations of the grid impedance at different charging outlets. The controller design needs to achieve a good bandwidth while having a cutoff frequency lower than most of the possible filter resonance frequencies to avoid instabilities. However, high grid impedances result in very low resonance frequencies that are not rejected by the controller's bandwidth. These resonances can lead to non compliance with the IEC standards on harmonic current emissions. Therefore, active damping of the input filter, for those low frequency ranges, is a must.

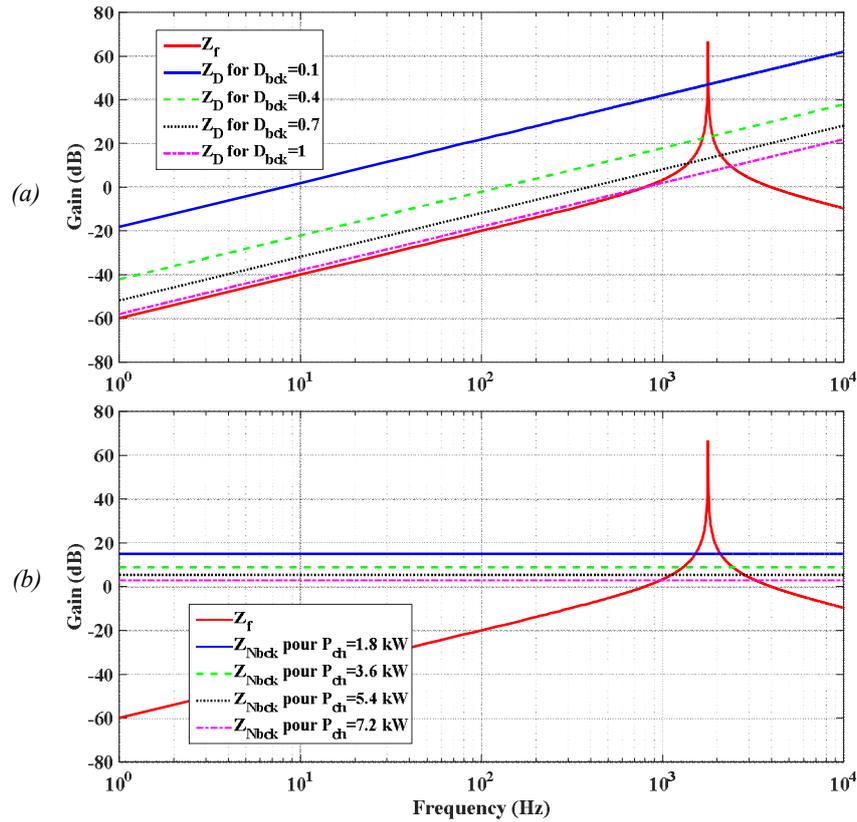


Fig.I.32. Study of the input filter's effect on the control stability through verification of the Extra Element Theorem inequalities. (a) Comparison of the filter's output impedance with Z_D for different operating points. (b) Comparison of the filter's output impedance with Z_N for different single-phase charging powers.

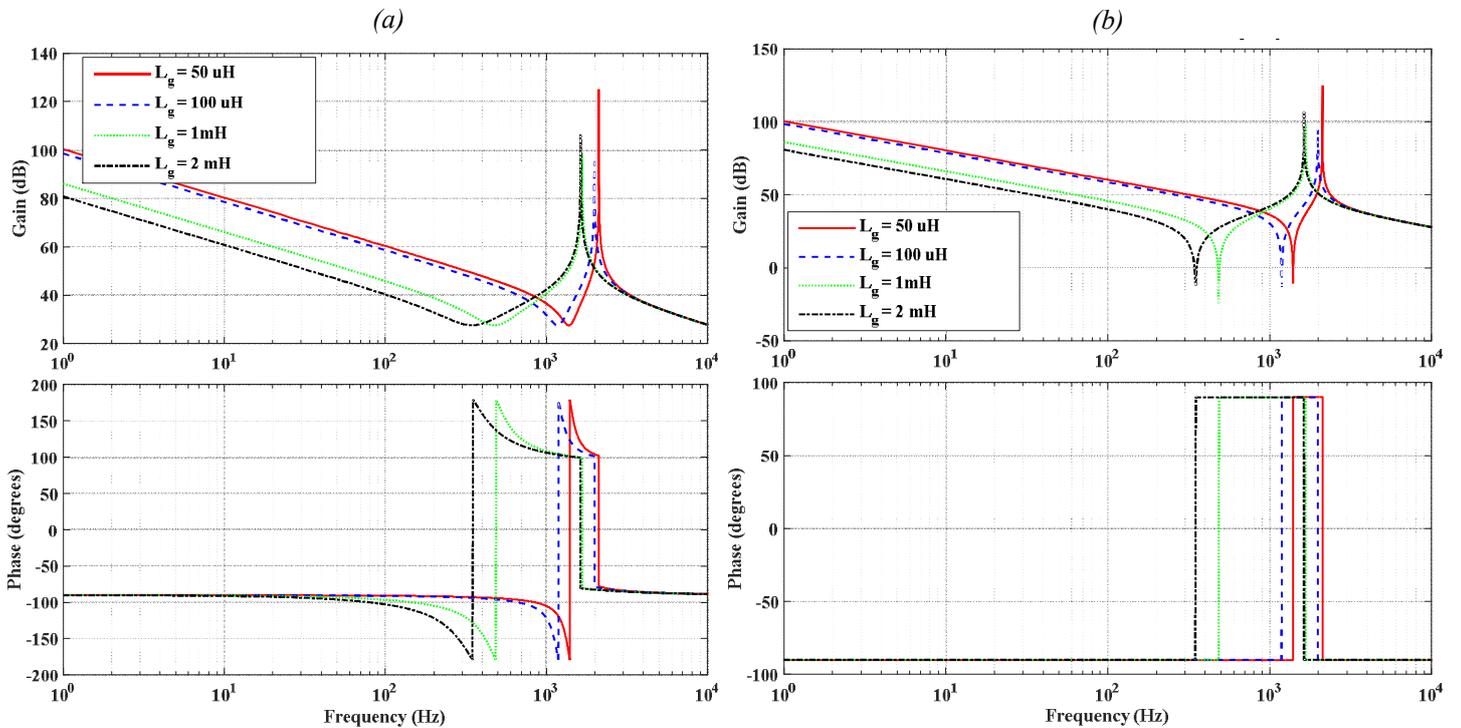


Fig.I.33. Bode plot of control to inductor current transfer function; (a) $G_{ILdbck}(s)$ of the CSAR including input filter effect. (b) $G_{ILdbst}(s)$ of the Boost including input filter effect.

3.4. Simulation results & contributions

Based on all the previous analysis, simulations are carried for the power circuit of Fig.I.1 using the proposed PFC control strategy illustrated by Fig.I.29. Results, presented in Fig.I.34, show the system's operation under the two modes of operation: Buck and Boost modes. Moreover, near unity displacement power factor is achieved and the activation of the active damping shows lower current harmonics in the grid current.

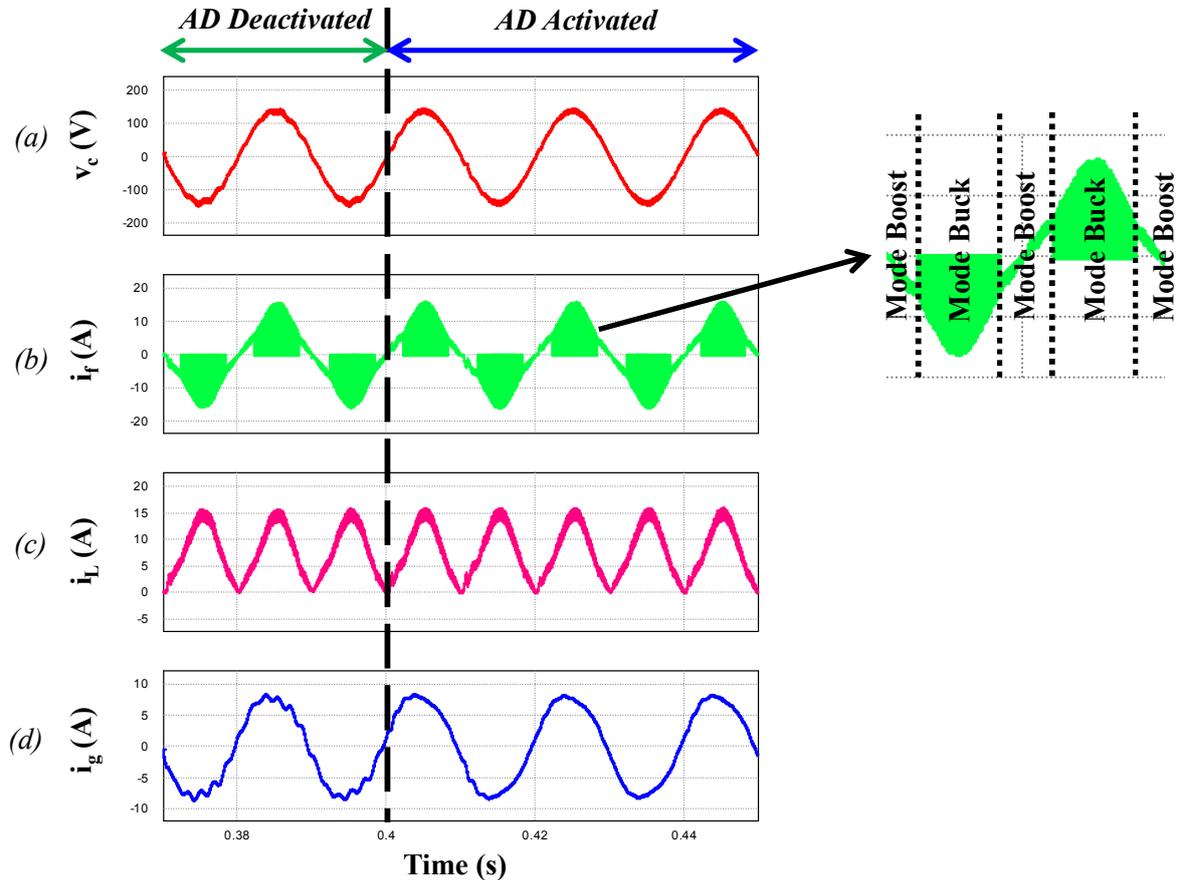


Fig.I.34. Simulation results for 600 W of the global PFC control strategy before and after activation of the AD at 0.4 s. (a) Converter voltage. (b) Converter current. (c) DC-side current flowing through the filtering inductor. (d) Grid current.

These results are going to be compared with those obtained with the PFC control strategy shown in Fig.I.35. This control is presented by [Gati et al. 2014]. It is found in the state of the art and applied to a power conversion structure very similar to our own single-phase charger.

In this strategy, the Buck-type rectifier is always operated via PWM through the duty cycle d_{buck}^* to ensure power factor correction. The PFC is achieved via open-loop control of the grid current i_g .

On the other hand, the Boost output stage regulates the inductor current i_L through closed loop control. The Boost's computed duty cycle d_{boost}^* is then compared to a saw tooth signal in order to generate the switching function of the Boost's low-side switches (as a reminder, the high-side switches of the Boost are always turned-off).

For this control strategy, the displacement power factor is not controlled, the PFC is achieved through open-loop control and the switches of both converters are always commutating at the switching frequency. Furthermore, the authors recommend regulating the inductor current at a relatively high dc value, around 100A, regardless of the charging power and for low filtering inductance values. Since this PFC is not conceived in a closed-loop fashion, this recommendation proves necessary in order to avoid the distortion of the grid current at zero crossings (this phenomenon is typically associated with Boost PFC power circuits). Simulation results for a 7 kW charge power are given in Fig.I.36.

By comparison, our proposed strategy lowers the switching power losses by controlling, at each instant, only one converter via PWM. Moreover, the dc inductor current's level is greatly reduced which allows the reduction of the size of the input DM filter and gives the possibility of increasing the value of the dc-side filtering inductor. In addition, a displacement power factor correction scheme is implemented in closed loop and the current harmonic issues are addressed via active damping of the input filter's resonance.

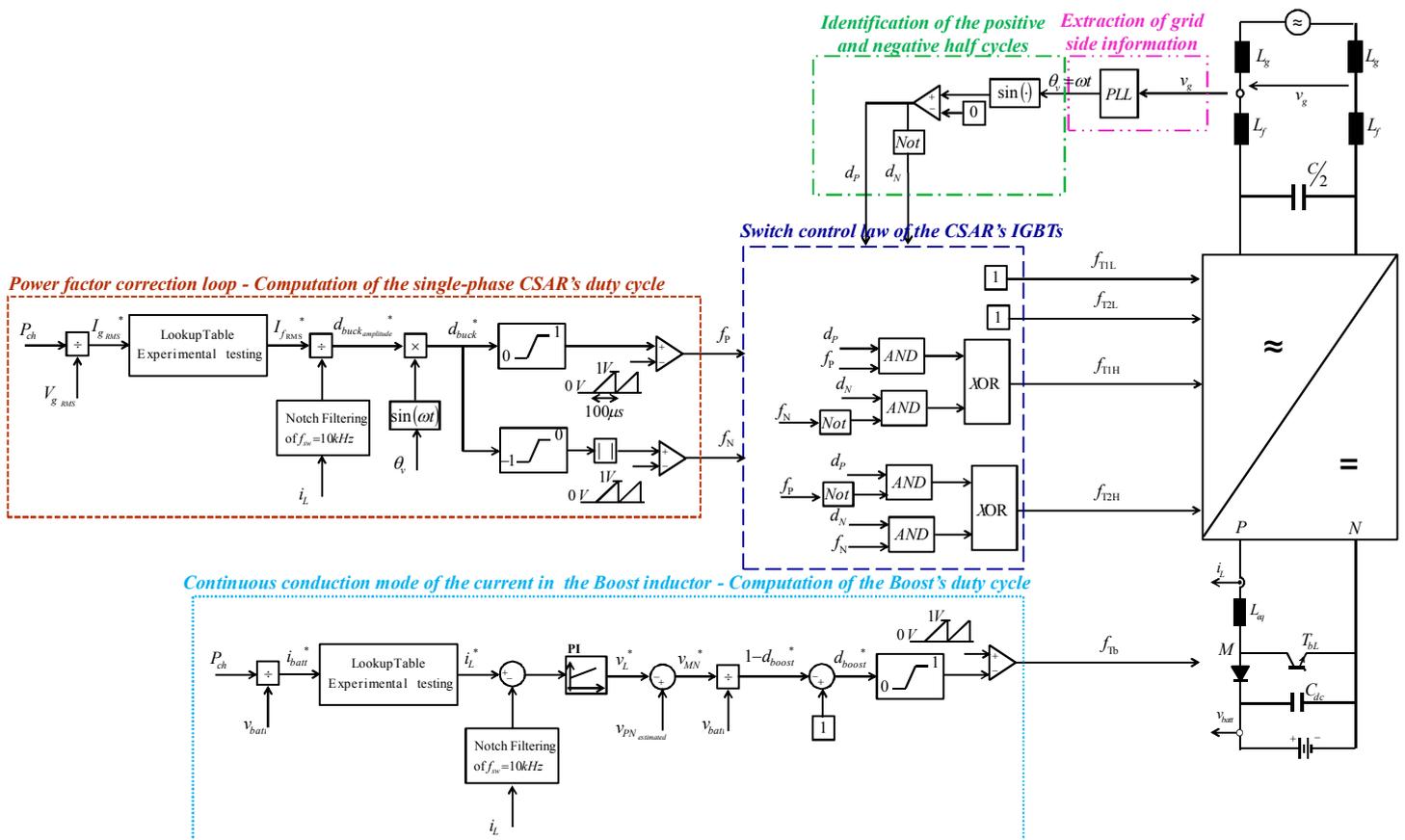


Fig.I.35. State of the art PFC strategy applied to the charger [Gati et al. 2014].

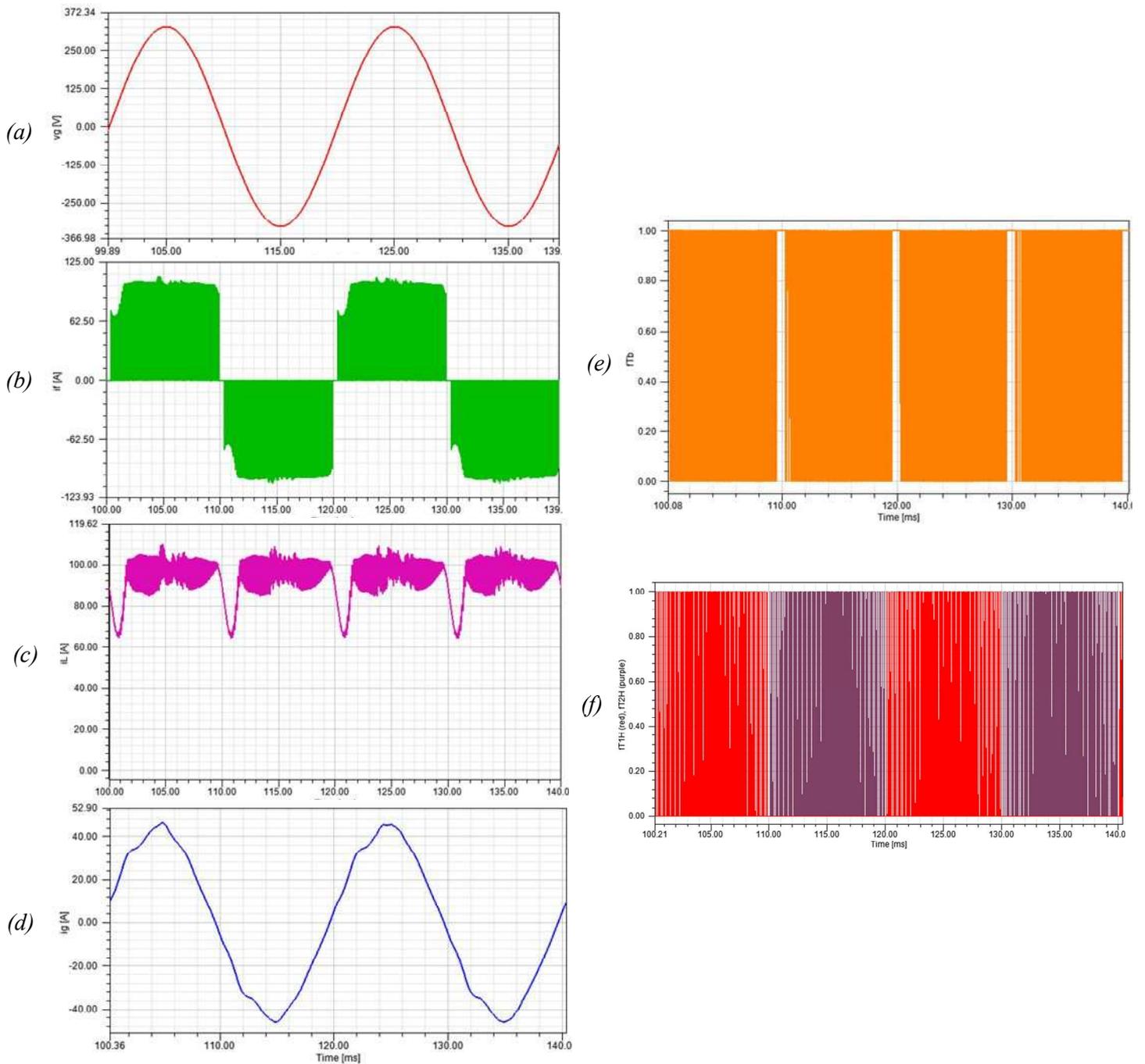


Fig.I.36. Simulation results of the state of the art PFC control strategy. (a) Mains voltage. (b) Converter current. (c) DC-side current flowing through the filtering inductor. (d) Grid current. (e) Switching function of the Boost. (f) Switching functions of the high-side switches of the rectifier: (Red) T_{1H} & (Purple) T_{2H} .

3.5. Requirements for an ideal input current

This paragraph discusses the requirements needed to ensure an ideal input current using a single-phase current source rectifier without taking into consideration the various industrial constraints.

3.5.1. Inherent ripple at twice the line-frequency

Single-phase current source active rectifiers (CSAR) suffer from an undesirable low-frequency ripple that appears on the dc-link side. More specifically the ripple appears at twice the grid frequency i.e. 100 Hz. In fact, assuming that the grid voltage v_g and current i_g are devoid from harmonics, they can be expressed as:

$$\begin{cases} v_g = V \cdot \cos(\omega \cdot t) \\ i_g = I \cdot \cos(\omega \cdot t + \varphi) \end{cases} \quad \text{eq. (I.51)}$$

where φ is the displacement angle. In this case, the instantaneous power at the grid-side can be written:

$$p_g = v_g \cdot i_g = \frac{V \cdot I \cdot \cos\varphi}{2} + \frac{V \cdot I \cdot \cos(2 \cdot \omega \cdot t + \varphi)}{2} \quad \text{eq. (I.52)}$$

The first term represents the average power whereas the second term represents twice the line-frequency ripple power. Assuming power balance (neglecting all power losses), the output voltage of the CSAR can be expressed as a function of the dc-link current i_L as follows:

$$v_{PN} = \frac{v_g \cdot i_g}{i_L} = \frac{V \cdot I \cdot \cos\varphi}{2 \cdot i_L} + \frac{V \cdot I \cdot \cos(2 \cdot \omega \cdot t + \varphi)}{2 \cdot i_L} \quad \text{eq. (I.53)}$$

Usually i_L is controlled to be constant, this means that v_{PN} will become the source of the twice line-frequency ripple power. The dynamic equation of the dc-link inductor is given as a function of the input voltage of the Boost stage v_{MD} :

$$L_{eq} \cdot \frac{di_L}{dt} = v_{PN} - v_{MD} \quad \text{eq. (I.54)}$$

This equation shows that in order to achieve a constant dc-link current, a high value of inductance L_{eq} is required. This is usually called passive decoupling of the double-frequency component and results in a rather bulky dc-link inductor. Active decoupling methods exist (Fig. I.37) and are reviewed by [Sun et al. 2016]; however, they require additional components.

3.5.2. Switch control of the CSAR for an ideal input current

In order to achieve near unity power factor with the six-switch CSAR, two cases can be distinguished depending on whether a freewheeling diode is being used or not.

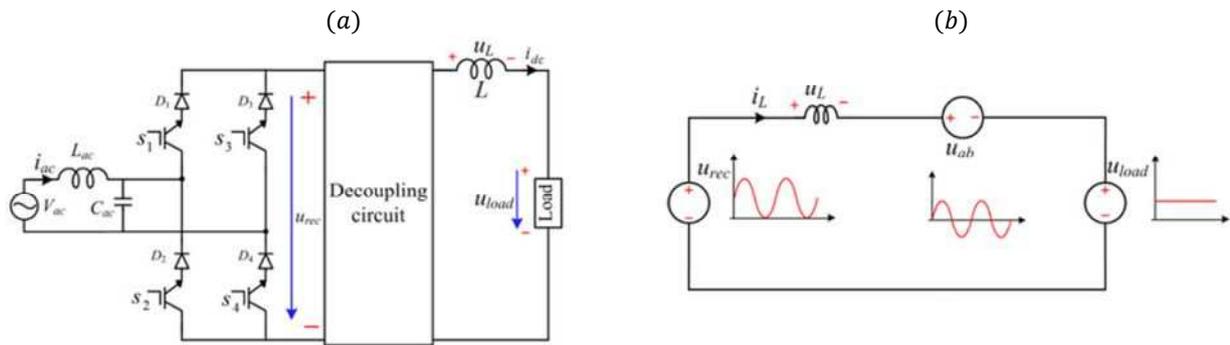


Fig.I. 37. (a) CSC configured with a decoupling circuit. (b) Equivalent circuit of (a). [Sun et al. 2016]

a) Without a freewheeling diode

At the zero crossing of the input voltage, the CSAR is in Boost Mode operation. The switch control strategy that ensures a lagging input current i_f without zero-levels requires the low side switches to be activated as shown in the following table:

Table I.5. SWITCH CONTROL STRATEGY FOR THE BOOST MODE OF OPERATION

Mode of operation	Converter current polarity	Switching States					
		T1H	T2H	T1L	T2L	TbL	TbH
Boost $ v_c \leq v_{batt}$	$i_f \geq 0$	ON	OFF	OFF	ON	PWM	OFF
	$i_f < 0$	OFF	ON	ON	OFF	PWM	OFF

The switching of the low-side switches, according to the polarity of the input current, forces the ON/OFF states of their series diodes (D1L, D2L) regardless of the input voltage's polarity.

In this case, there are no zero-levels in the input current. This results, at each zero crossing of the input voltage and as long as the input current is lagging, in a negative instantaneous input power. Assuming a constant (positive) dc-link current, eq. (I.53) shows that the output voltage v_{PN} of the CSAR needs to take on negative values. Moreover, in order to ensure a constant dc-link current, eq. (I.54) also yields a negative voltage at the input of the Boost v_{MD} .

However, the output regenerative Boost stage, in its current topology, cannot ensure negative voltage at its input unless the polarity of the battery's voltage can be inverted. This is only possible if more components are added to the dc-dc converter as shown in Fig.I.38 for instance. The switching of the additional semi-conductors is based on the polarities of the input voltage and the input current. When these measured signals present opposite polarities, the additional switches are simultaneously turned on; otherwise, they are simultaneously turned off.

b) With a freewheeling diode

If the same switch control law is maintained with the addition of the freewheeling diode, the zero-levels will appear at each zero crossing of the input voltage. In fact, as long as the input current is lagging, the negative value of the output voltage of the CSAR, which is applied across the

freewheeling diode, is sufficient to turn it ON. Therefore, the low-side switches in this study have been maintained in the ON state to reduce switching losses.

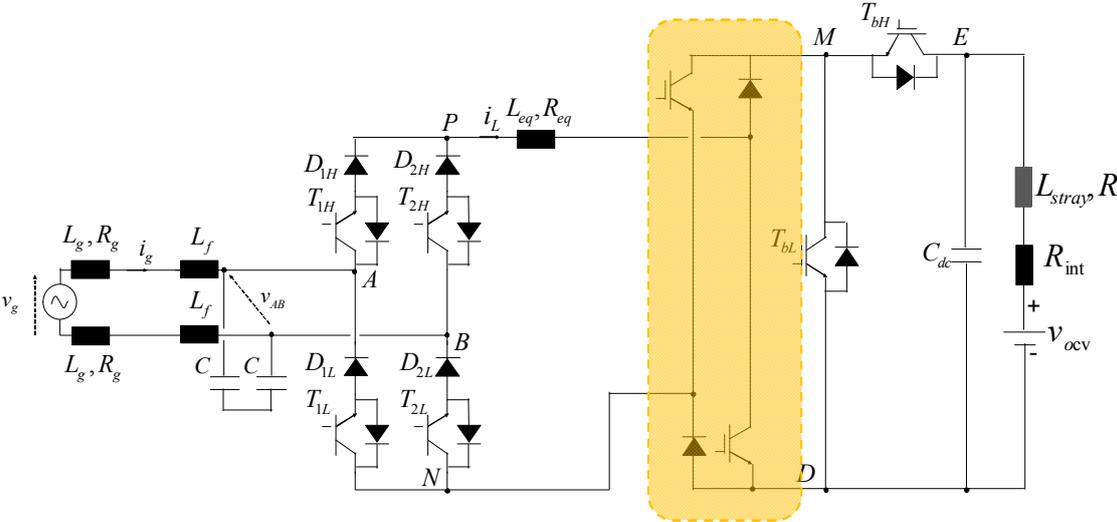


Fig.I. 38. Example of additional components that would allow to change the polarity of the voltage at the input of the Boost.

4. Experimental results

For the purpose of experimental validation, a test bench was developed at the SATIE laboratory (Fig.I.39 and Fig.I.40 for a zoom view). The control is implemented using a Texas Instruments DSP with TMS320F28335 microcontroller. The DSP is plugged into an interface board that adapts the voltage and current sensors' output levels to the DSP's analog to digital converters' requirements. LEM's LA 100-P hall-effect current sensor is used for the grid current measurement and a differential voltage probe measures the converter's voltage. The experimental setup's parameters used for charging are given in Table 3. Unlike simulations, the grid impedance is unknown and varies from one ac power outlet to the other. The experimental results are provided for a 600-W single-phase charger.

A step-by-step experimental validation of each function from the proposed PFC control structure is presented hereafter.

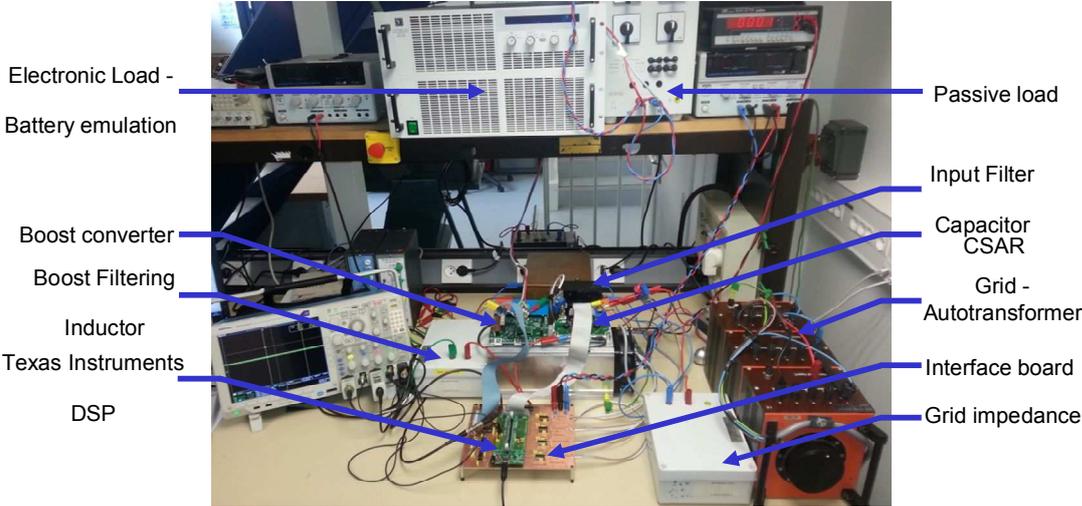


Fig.I.39. Experimental test bench setup at the SATIE laboratory.

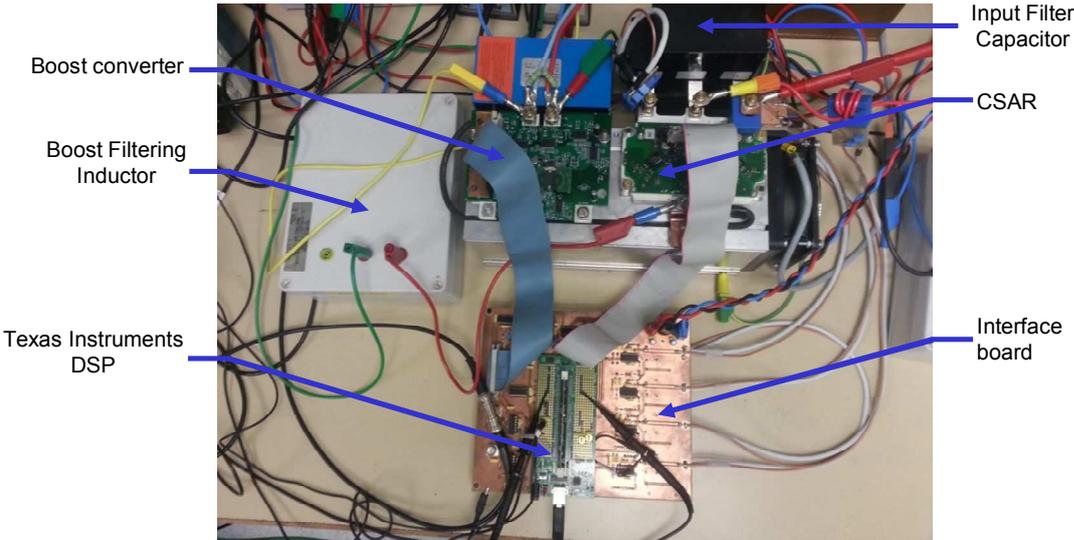


Fig.I.40. Zoom view of the experimental test bench setup at the SATIE laboratory.

4.1. Validation of the synchronization with the grid

In this section, only the SOGI-PLL is implemented on the DSP Fig.I.42. The converter setup used to validate the information extracted from the grid is shown in Fig.I.41. It consists of the current source active rectifier and an (L, R) load. In this section the converter is connected to the grid but the information are extracted at no-load condition. This means that the rectifier does not absorb any current. The grid current consists solely of the current absorbed by the input filter capacitors which presents a 90° phase-shift with regards to the converter voltage.

The experimental results presented in Fig.I.43 validate the operation of the PLL. The information extracted is the phase angle of the converter voltage (in magenta) and the displacement angle $\varphi = 90^\circ$ measured between the converter voltage and the grid current (in green). Moreover, the results shown in Fig.I.44 illustrate the extraction of the fundamental components of the converter voltage (in green) and the grid current (in magenta). This validates the filtering effects of the SOGI scheme.

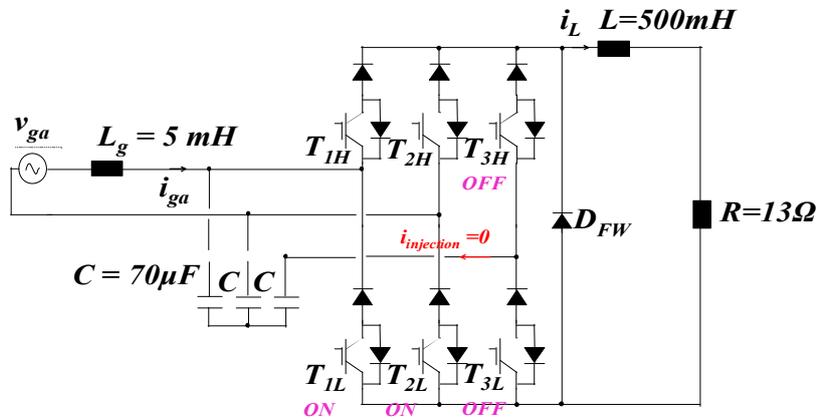


Fig.I.41. Test bench setup used to validate the SOGI-PLL grid synchronization scheme.

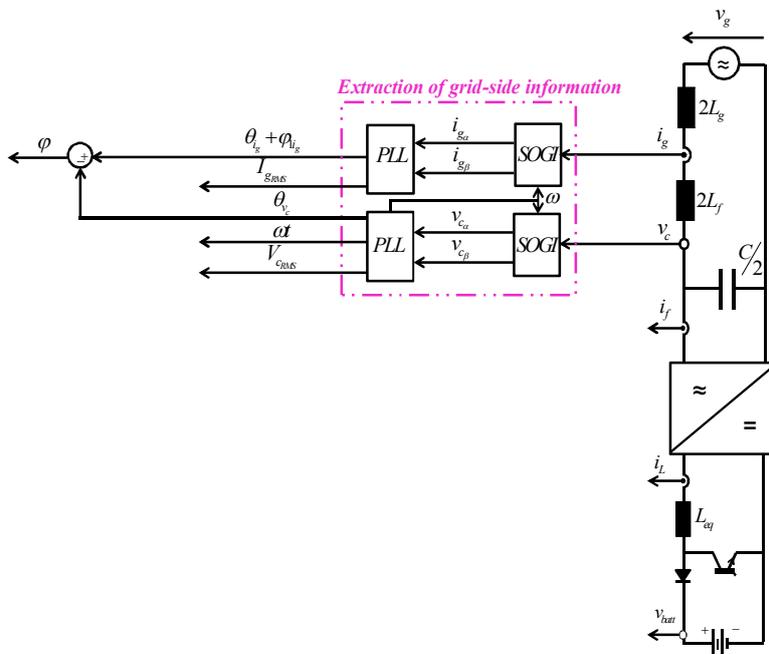


Fig.I.42. The control implemented on the DSP for the validation of the SOGI-PLL.

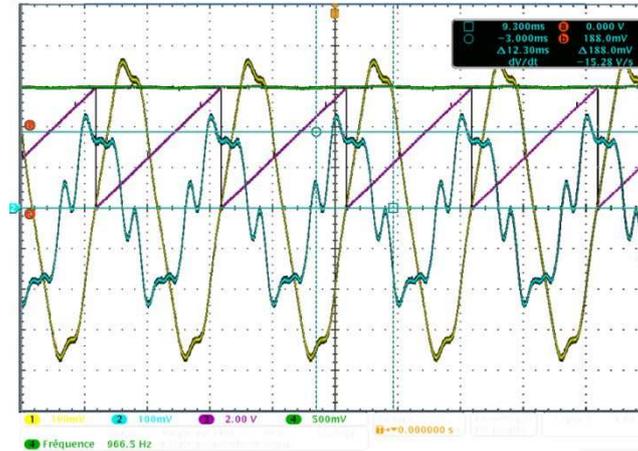


Fig.I.43. Validation of the PLL. (Ch1) Converter voltage v_c (100V/div after compensation of the differential voltage probe's attenuation). (Ch2) Grid current i_g (50 A/V). (Ch3) Extracted converter voltage phase angle θ_{vc} ($57^\circ/V$). (Ch4) Measured displacement angle between the converter voltage and the grid current ϕ ($30^\circ/500mV$).

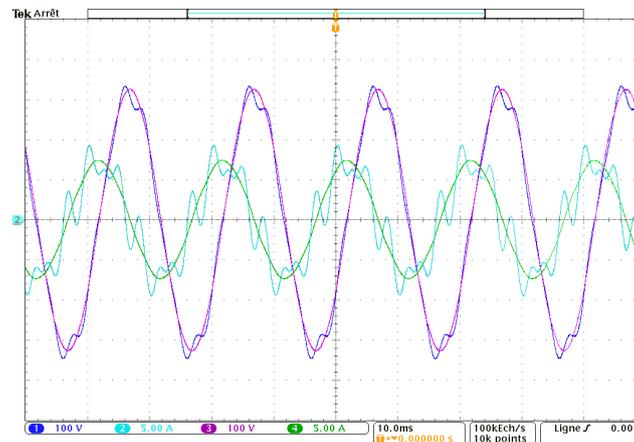


Fig.I.44. Validation of the SOGI filter. (Ch1) Converter voltage v_c . (Ch2) Grid current i_g . (Ch3) Fundamental component of the filtered grid current i_{ga} . (Ch4) Fundamental component of the filtered converter voltage v_{ca} .

4.2. Validation of the DPFC scheme

In order to verify the displacement of the grid current with regards to the converter's voltage using the DPFC scheme recalled in Fig.I.45, tests are run for two different displacement angle references on the experimental setup of Fig.I.41.

The experimental identification of the transfer function used to design the PI controller parameters is shown in Fig.I.46. In this section the Boost is added at the output of the rectifier. For now, the Boost controls the inductor current at 8A via hysteretic control.

Fig.I.47 shows that the grid current can be successfully displaced according to the reference angle ϕ^* chosen. Furthermore, these experimental results show the apparent resonance when applying a displacement angle of 0° and 30° , respectively, between the fundamentals of the two signals.

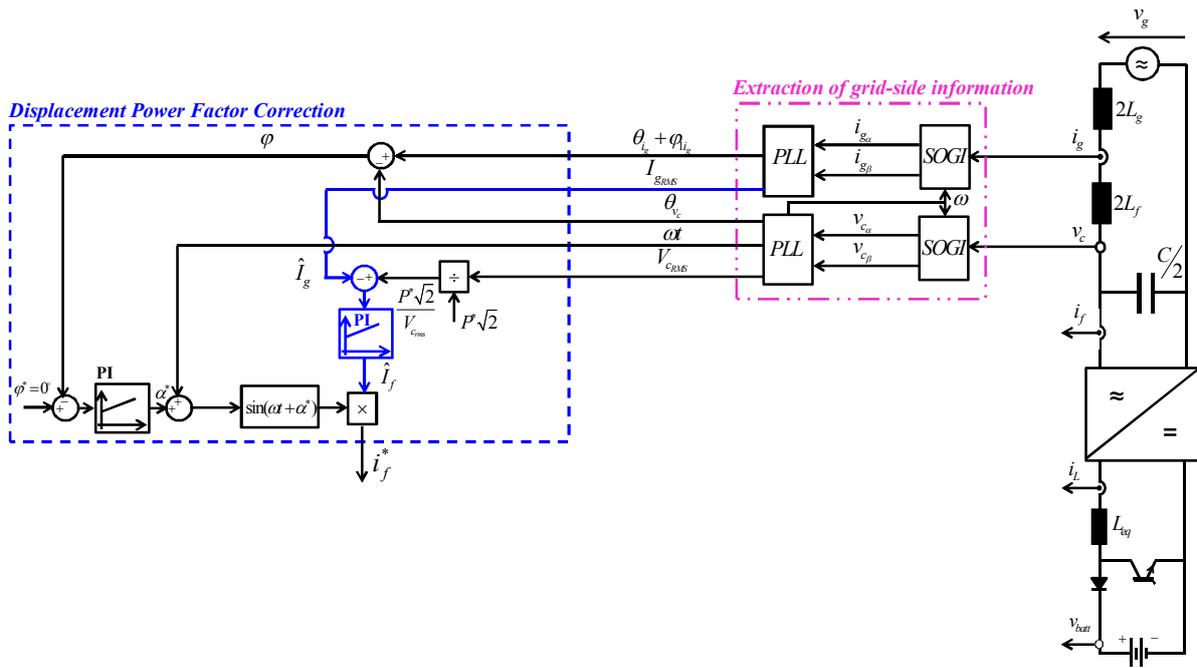


Fig.I.45. The control implemented to validate the DPFC scheme.

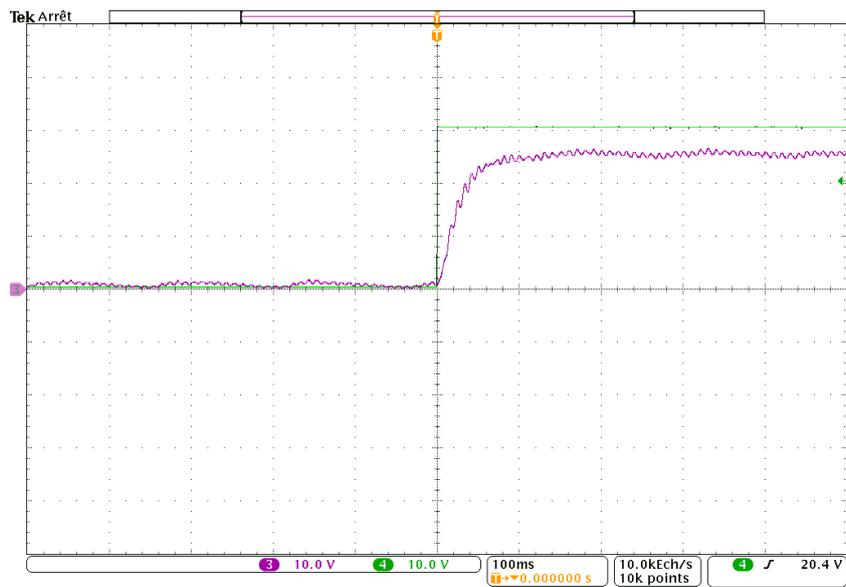


Fig.I.46. Experimental identification of the transfer function. (Ch3) Extracted displacement angle between the fundamentals of the converter voltage and the grid current φ ($1^\circ/\text{V}$). (Ch4) Step change of the phase angle α between the fundamentals of the converter voltage and the converter current i_f ($1^\circ/\text{V}$).

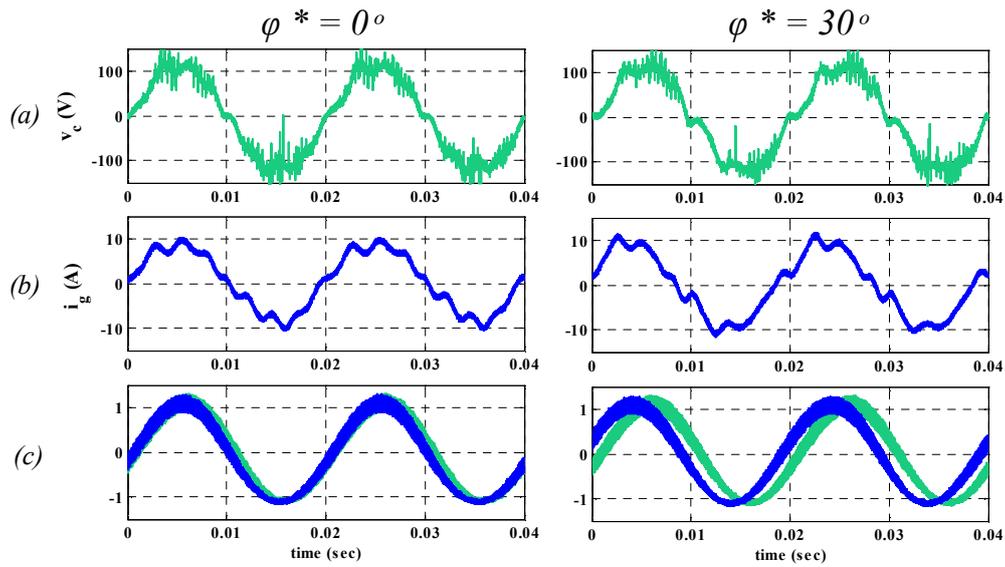


Fig.I.47. Experimental results for two different displacement angle references. (a) Converter voltage. (b) Grid current showing a periodical resonance. (c) Fundamental components of the converter voltage and grid current displaced by φ^* .

4.3. Experimental identification of the zero levels

The zero levels that appear in the converter current are shown in Fig.I.48. They occur at each zero crossing of the converter voltage and excite the resonance of the input filter. This explains the oscillations that are apparent in the converter current and voltage measurements.

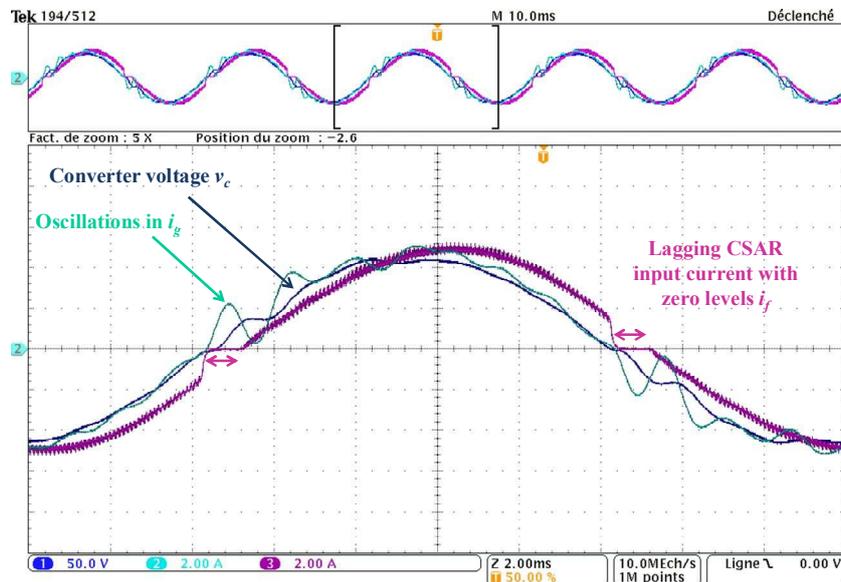


Fig.I.48. Experimental results for $\varphi^*=0^\circ$ without AD emphasizing on the zero levels. (Ch 1) Converter voltage. (Ch 2) Grid current. (Ch 3) Averaged converter current presenting a phase lag with regards to the converter voltage.

4.4. Experimental implementation of the active damping

The damping shown in Fig.I.49 is activated and its effect on the attenuation of the input filter's resonance is clearly shown in Fig.I.51.

The active damping emulates a current drawn by the virtual resistor placed in parallel with the DM filtering capacitors (Fig.I.50). This current represents the injection signal i_{Rv}^* obtained at the output of the active damping loop. The injection signal is depicted in Fig.I.52 (Channel 3). It can be seen that the active damping does not affect the active power since it filters out the fundamental frequency and contains only current harmonics.

As a reminder, in this section the Boost controls the inductor current to a constant level (8 A) using a hysteric controller. Therefore, the remaining harmonics seen in the grid current waveform, after the activation of the damping, are due to the non-controllable phases from which suffers the inductor current i_L around each zero crossings of the input voltage.

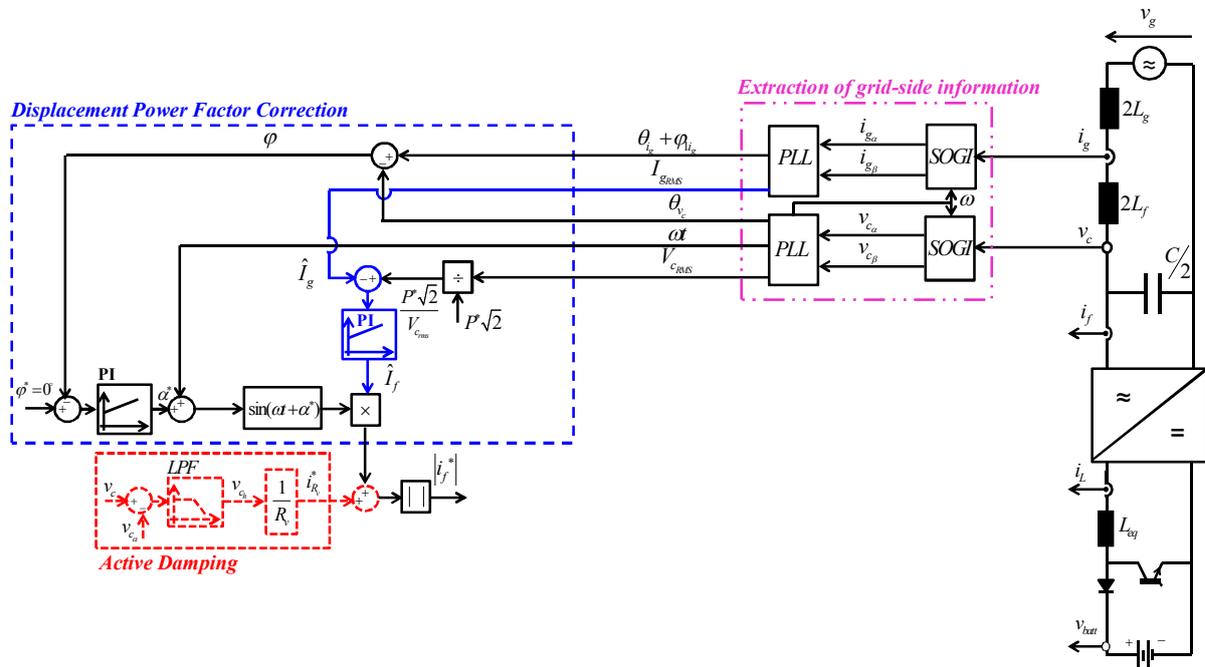


Fig.I.49. The control implemented to validate the active damping scheme.

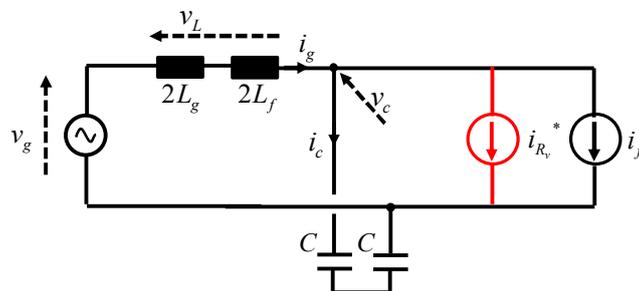


Fig.I.50. Injection signals effect on the converter current.

By adapting the control, we have successfully achieved the damping of the input filter resonance without adding a physical resistor to the DM input filter. This is perfectly in line with the objectives of this research to include low cost solutions for the optimization of the grid-side power quality performances.

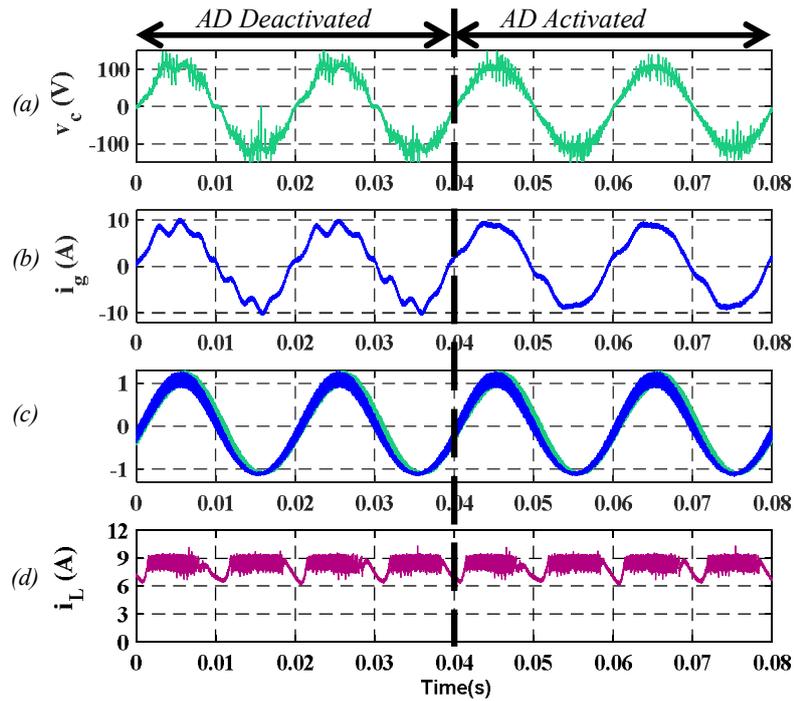


Fig.I.51. Experimental results for $\varphi^*=0^\circ$ before and after activation of the active damping. (a) Converter voltage. (b) Damped grid current. (c) Normalized fundamental components of the converter voltage and grid current. (d) DC current resulting from a Boost hysteretic current control.

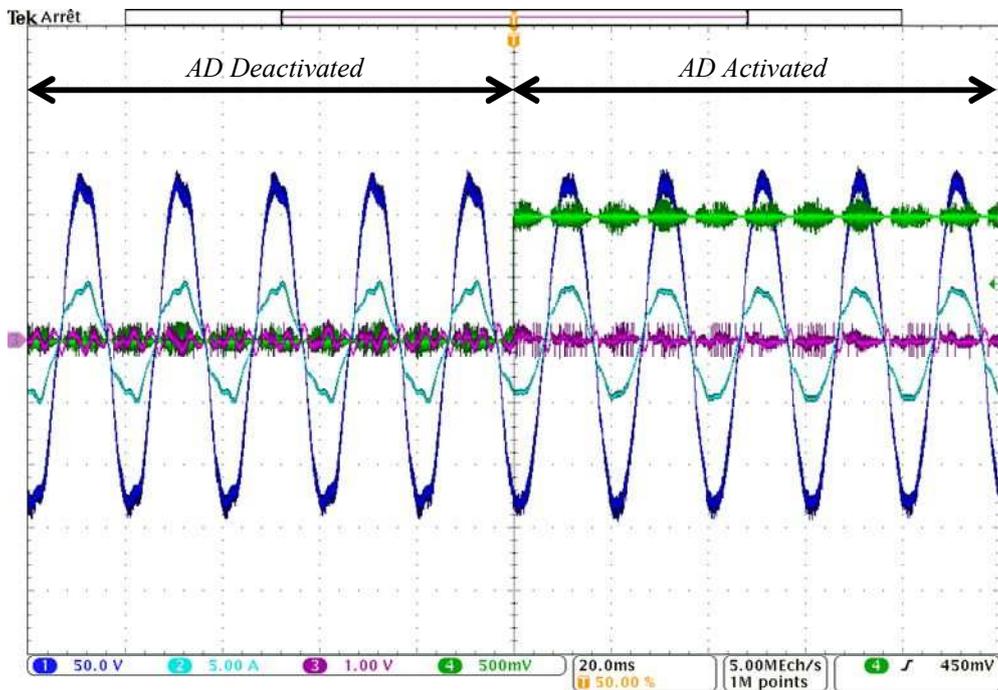


Fig.I.52. Experimental results for $\varphi^*=0^\circ$ before and after activation of the active damping. (Ch 1) Converter voltage. (Ch 2) Grid current. (Ch 3) Injection signal at the output of the active damping loop i_{rv}^* . (Ch 4) Signal that indicates the instant of activation of the AD.

4.5. Harmonic content & compliance with the standards

For charging at 600 W with an RMS value of 6 A for the grid current, the applicable IEC standard is the 61000 3-2. It defines the limits for each of the current harmonics up to the 40th rank. However, it does not specify limitations regarding THD.

Therefore, Fig.I.53 shows the comparison between the measured low-frequency spectrum with the limits defined by the IEC, before [see Fig.I.54 (a)] and after [see Fig.I.54 (b)] activation of the damping. The proposed method achieves the required compliance with the standard.

The fluke 41B single-phase power quality analyzer is used to study the THD levels and low-frequency spectrum of the grid current. The THD level drops from 14% to 8.3% upon activation of the damping and the grid current's distortion is highly attenuated.

These results validate the implementation of the displacement power factor correction scheme associated with the active damping of the input filter resonance in order to achieve a near unity power factor.

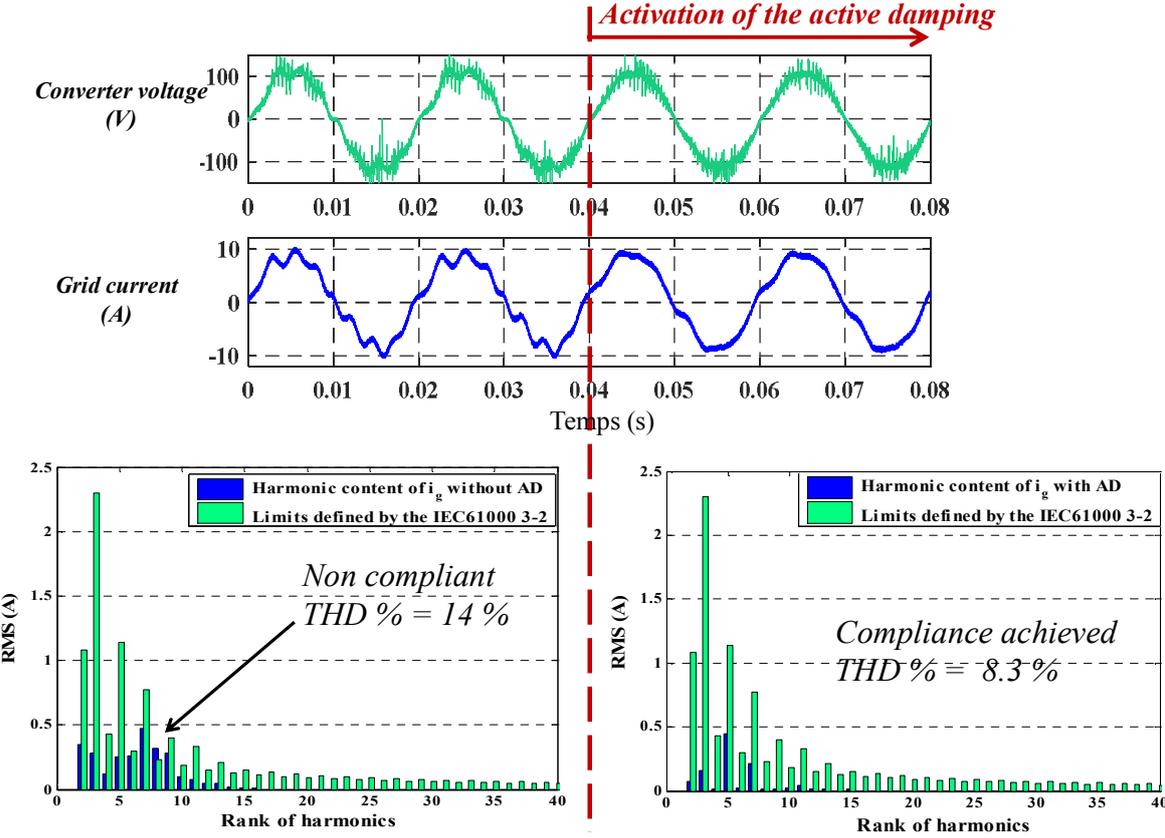


Fig.I.53. Measured harmonic content of the grid current for $\phi^*=0^\circ$ before and after activation of the active damping.

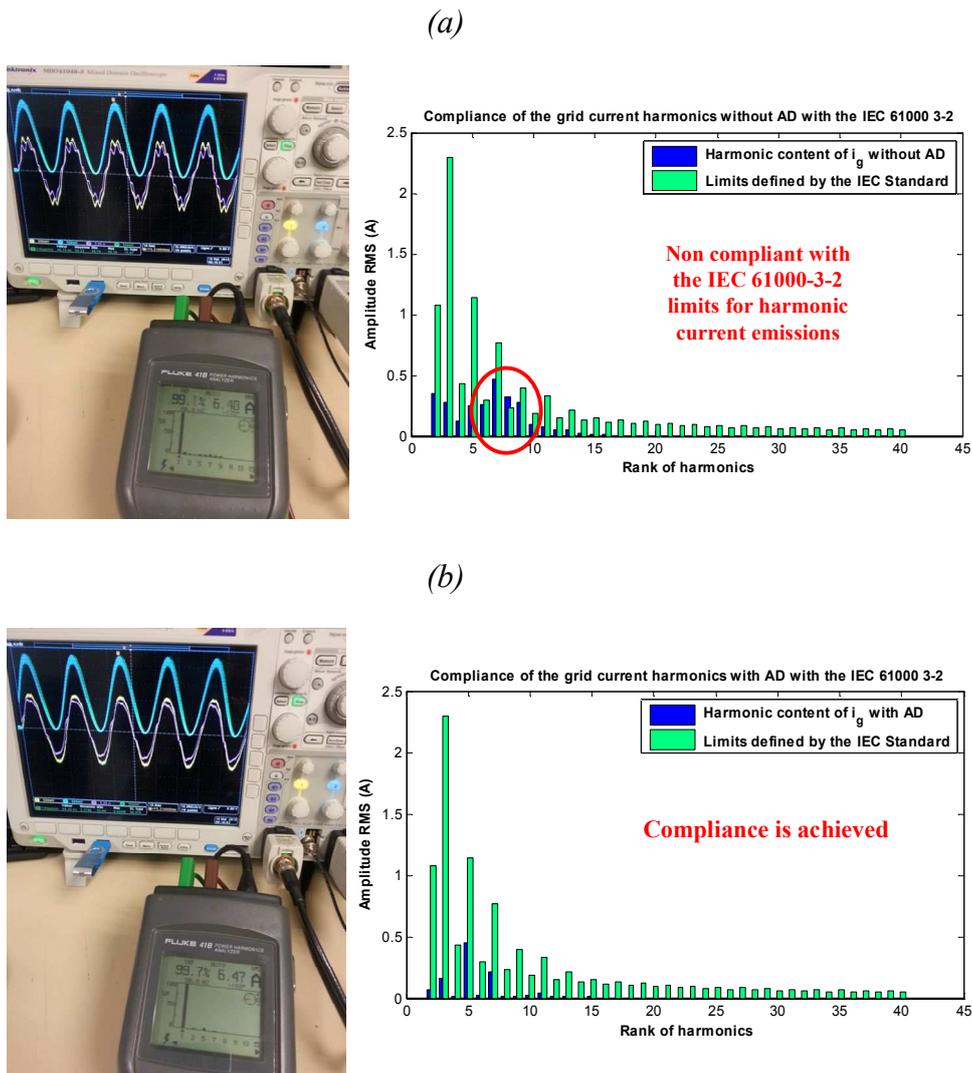


Fig.I.54. Measurement of the harmonic content of the grid current and verification of the compliance with the IEC 61000-3-2. (a) Without active damping. (b) Upon activation of the active damping.

4.6. Implementation of the global PFC control structure

The current control loop with the dual modes of operation is implemented.

On one hand, the global strategy recalled in Fig.I.56 is implemented for a grid voltage of 50 V_{RMS} and the electronic load that emulated the battery tuned at 100 V. For this validation, the experimental bench is setup according to Fig.I.55. Since the output voltage is higher than the amplitude of the converter voltage, only the Boost is activated in PFC mode and the Buck is kept turned on. The experimental results for this case study are given in Fig.I.57.

On the other hand, the strategy of Fig.I.56 is implemented for a grid voltage of 87 V_{RMS} and an output voltage of 100V for the electronic load. Therefore, depending on the instantaneous comparison between the converter voltage and the dc output voltage, the charger operates in Buck mode when $v_c > 100V$ and in Boost mode when $v_c < 100V$ (cf. Fig.I.58).

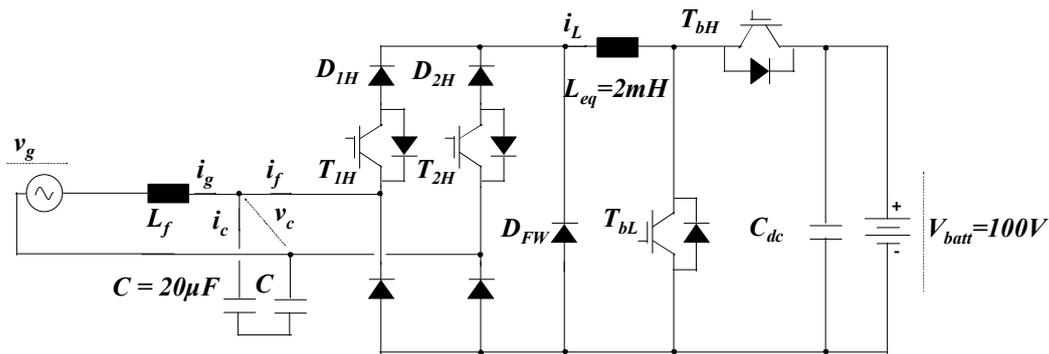


Fig.I.55. Power circuit used for the experimental testing of the global PFC control strategy ($C_{dc}=2400\mu F$, $L_f=2mH$ and a switching frequency of 50 kHz).

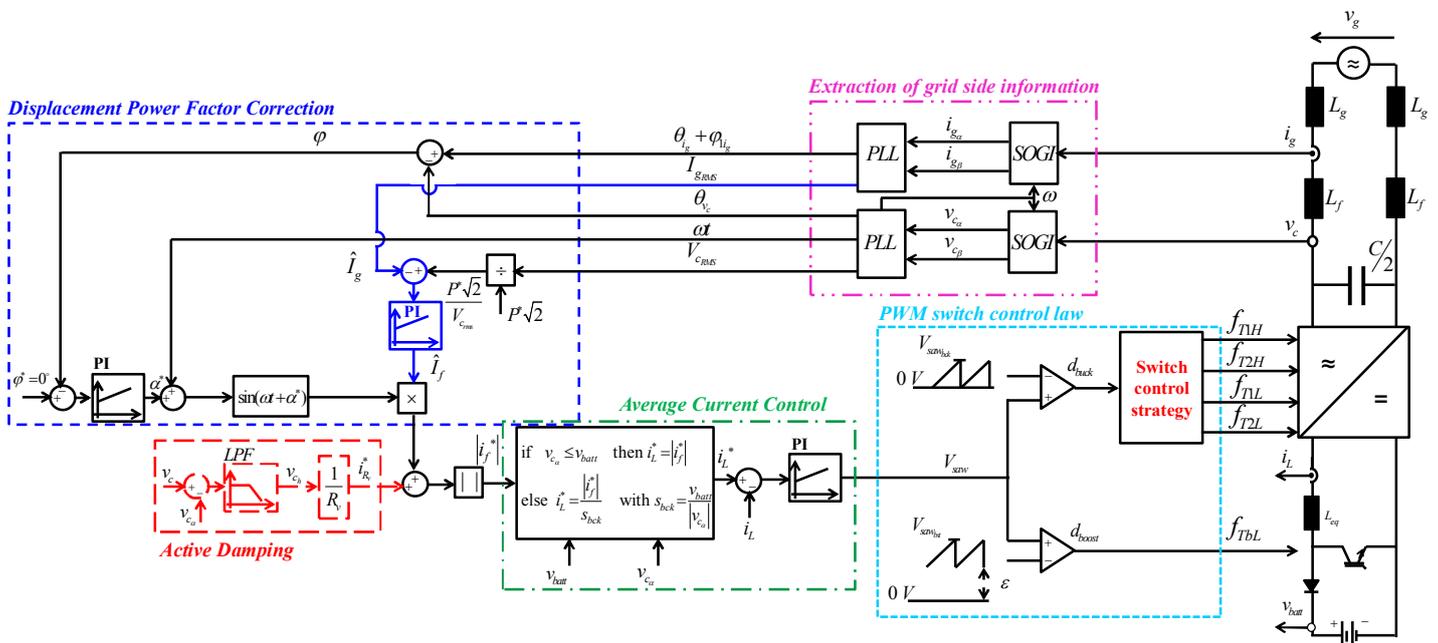


Fig.I.56. Global PFC strategy including a dual-mode current control loop associated with the DPFC scheme and the active damping control.

The entire PFC control scheme has been experimentally validated in this section. The choice of the offset ϵ for the automatic detection of the mode of operation is verified in Fig.I.58.

It should be noted that the algorithm successfully detects, on its own, whether the Buck-type rectifier needs to be activated or not.

In fact, the transition from a full Boost mode of operation in Fig.I.57 to a Buck-Boost mode in Fig.I.58 is realized just by increasing, on-line, the transformation ratio of the test bench's auto-transformer. Based on the input voltage measurement, the control implemented on the DSP automatically adjusts online the duty cycles of both converters.

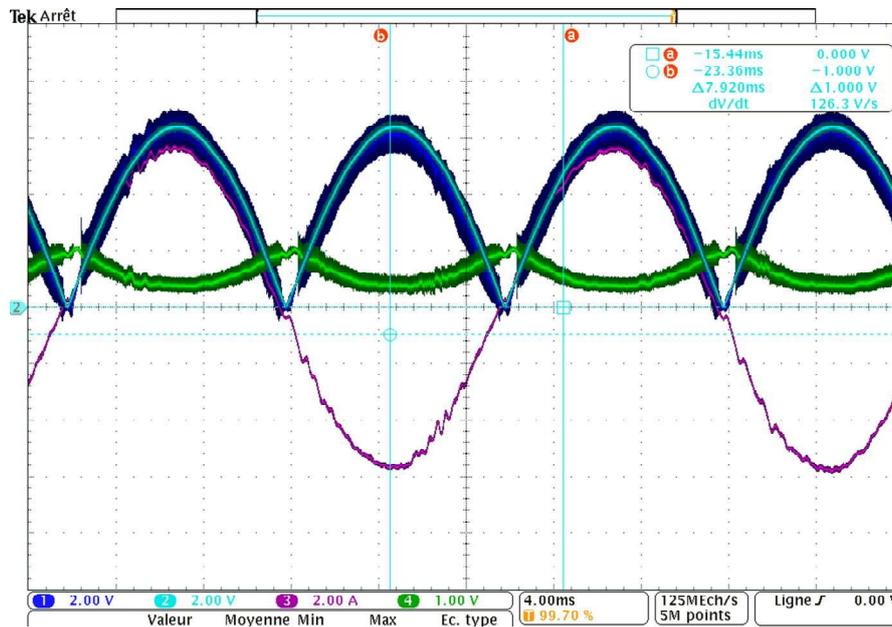


Fig.I.57. Experimental results for $\varphi^*=0^\circ$ without AD in Boost mode operation. (Ch 1) DC-side inductor current i_L . (Ch 2) inductor current reference i_L^* . (Ch 3) Grid current. (Ch 4) Modulation signal V_{saw} .

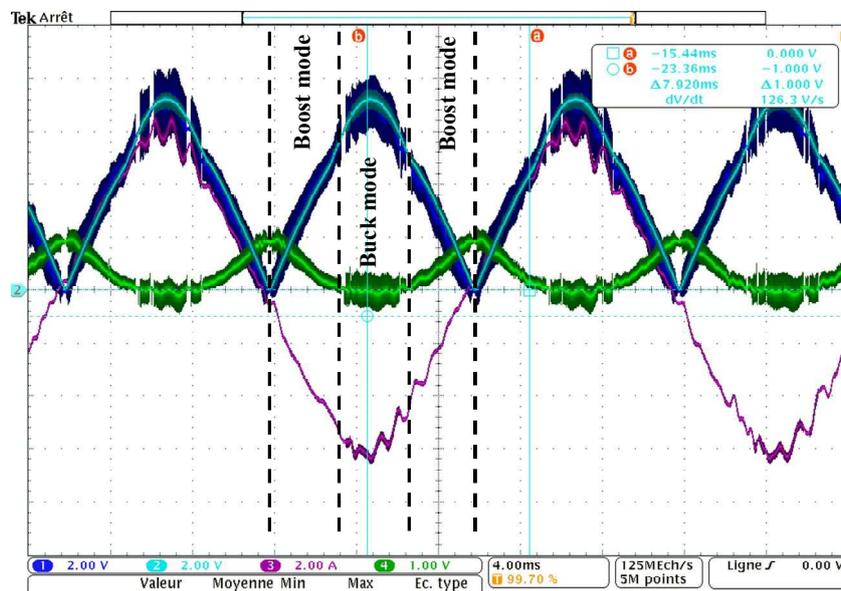


Fig.I.58. Experimental results for $\varphi^*=0^\circ$ without AD in Buck mode and Boost mode operation. (Ch 1) DC-side inductor current i_L . (Ch 2) inductor current reference i_L^* . (Ch 3) Grid current. (Ch 4) Modulation signal V_{saw} .

5. Conclusion & Future works

Power quality requirements for grid connected converters are defined by the IEC standards on harmonic current emissions. Therefore, battery chargers need to significantly enhance the quality of the current drawn from the grid. For onboard chargers capable of accommodating three-phase very fast charging as well as single-phase slow charging, compromises in meeting the input filter's design rules are inevitable.

In this Chapter, a PFC control strategy for the Buck-Boost single-phase onboard charger is proposed. It allows the correction of the displacement power factor along with an active damping solution for the input filter's resonance. Furthermore, the averaged small-signal equivalent model of the converter is developed. It allows the study of the impact that the input filter has on the control stability. This shows the need to integrate the filter parameters in the design of the current controller. Moreover, the average current control is associated with an online detection mechanism that automatically switches between two different modes of operation. The dual-mode operation proposed allows the reduction of the switching losses as well as the reduction of the leakage currents (to be quantified in future works). In addition, simulation results are validated through experimental findings. It is shown that the control proposed achieves near unity displacement power factor. The input filter is effectively damped through a virtual resistor and the global PFC strategy is experimentally validated.

Compared to a state of the art PFC strategy, the proposed control reduces the switching power losses by commutating a single converter at each instant, reduces the conduction power losses by reducing the level of the dc-side inductor current, reduces the common mode conducted emissions by blocking the commutation of each converter over a fraction of the fundamental period, achieves closed-loop PFC control at the input side of the converter and gives way to the possibility of resizing the dc-side inductor for lower current levels.

A more thorough modelling of the passive elements' impedances should be taken into consideration. In all cases, a passive damping of the differential mode input filter stage is required to prevent input filter resonances at no load condition. This can only enhance and facilitate the operation of the active damping. Furthermore, the DFT algorithm proposed is based on running summations for 40 harmonic ranks simultaneously. This requires sufficient microcontroller resources. Therefore, an adequate choice of processor must be considered for this type of implementation and might be too costly for an automotive application. Moreover, interactions between multiple users connected simultaneously to the grid must be investigated with regards to the possibility of shifting the resonance frequency such as in [He et al. 2013] where multiple resonances are treated in a parallel-inverter-based micro-grid.

Lastly, the impact of the PFC strategy on two main components of the integrated charger must be investigated. In fact, the electric machine's windings and the battery's specifications must be respected with regards to the currents flowing through them such as the thermal effects, the conducted common mode currents and EMI study of the battery pack and the electric machine's windings, the life span of the battery defined by its cycle life as well as the possible deterioration of the synchronous machine's bearings and windings due to high frequency common mode currents. For the battery, these characteristics must be studied over the course of a normal charge profile of the battery defined as constant current / constant voltage and can be found in [Sakr 2016].

Moreover, the transition between the Boost mode and the Buck mode seen in Fig.I.58 can be further studied. For instance, a technique that achieves a smooth transition between two modes of operation is presented in [Lee et al. 2009] for a non-inverting Buck-Boost converter.

Future works also include the investigation of non-linear control implementations in order to replace the average current control scheme as well as the study of the low frequency conducted EMI emissions using the Silicon Carbide semi-conductor technology under higher switching frequencies. In fact, with higher switching frequencies, higher control loop bandwidth can be achieved. In that way both the effectiveness and the stability of the active damping control scheme can be enhanced. For this purpose, a new test bench based on Silicon Carbide semi-conductors has been developed. It is shown in Fig.I.59 and a zoom view is given in Fig.I.60.

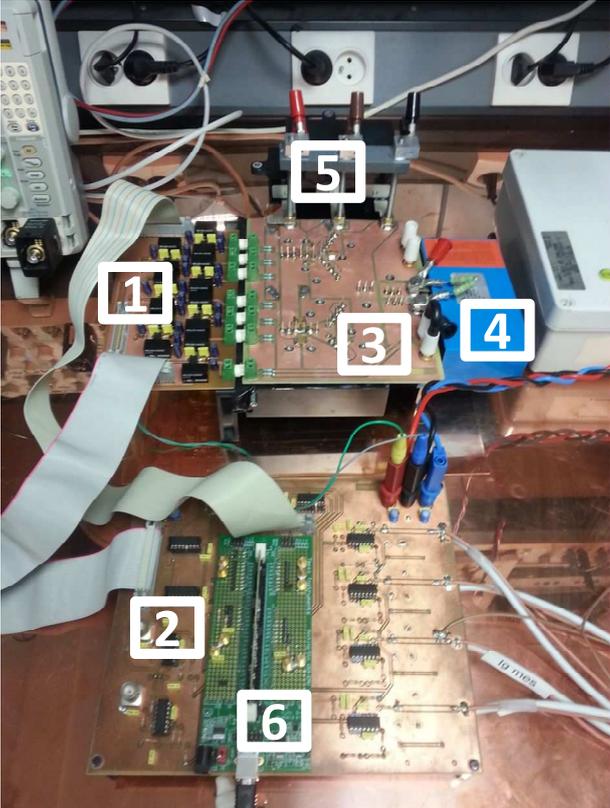


Fig.I.59. Test bench setup for future work. 1- Driver board, 2- Interface board for the TI F28335 DSP, 3- Power board with C2M0080120D Cree MOSFETs and SCS230KE2 ROHM SiC Schottky diodes, 4- DC bus capacitor, 5- DM filtering capacitors, 6- TI F28335 DSP.

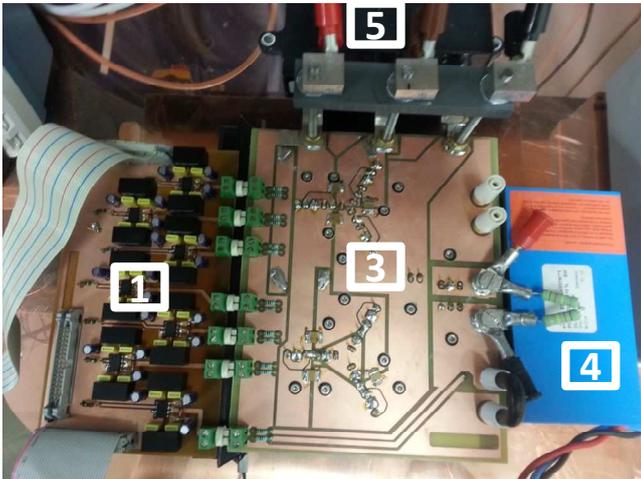


Fig.I.60. Zoom view of the test bench setup for future work. 1- Driver board, 3- Power board with C2M0080120D Cree MOSFETs and SCS230KE2 ROHM SiC Schottky diodes, 4- DC bus capacitor, 5- DM filtering capacitors.

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Chapter 2

Three-Phase Charging

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The onboard charger can be used for the fast charging of the EV's battery using dedicated charging stations with charge powers of 11 kW, 22 kW or 43 kW. Therefore, this chapter aims to study the power factor correction (PFC) scheme for the three-phase configuration of the charger illustrated in Fig.II.1.

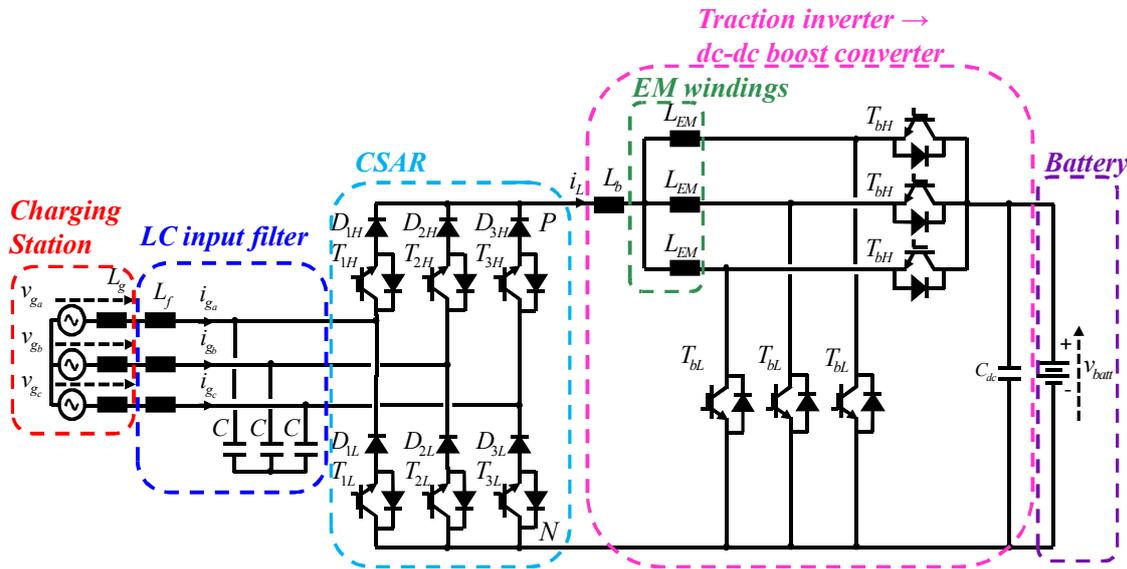


Fig.II.1. The on-board integrated non-isolated charger's three-phase configuration.

1. State of the art

This section attempts to evaluate the performances of the chosen three-phase six-switch current source rectifier (CSR) with respect to other CSR topologies. Afterwards, a quick review of various three-phase PFC control strategies, applicable to CSRs, is presented. A particular PFC strategy, found in literature, which can be applied to the charger's three-phase structure, is studied.

1.1. Three-phase rectifiers

Three-phase ac/dc converters have attained a maturity level that allows them an improved power quality performance through power-factor correction, a reduced total harmonic distortion at the input ac mains, and a well regulated dc output [Singh et al. 2004]. They can be found under unidirectional or bidirectional topologies with characteristics that are similar to Buck, Boost, Buck-Boost or multilevel converters. Bidirectional topologies are interesting for regenerative powers and future vehicle-to-grid (V2G) or vehicle-to-home (V2H) operations. Since the V2G and V2H operations are still in their development phase, the charger in this study utilizes a unidirectional rectifier. Comparative evaluations of three-phase PWM rectifiers have been conducted by [Nussbaumer et al. 2007], [Rodríguez et al. 2005] and [Kolar et al. 2013]. A classification of the known unidirectional three-phase rectifiers is illustrated in Fig.II.2.

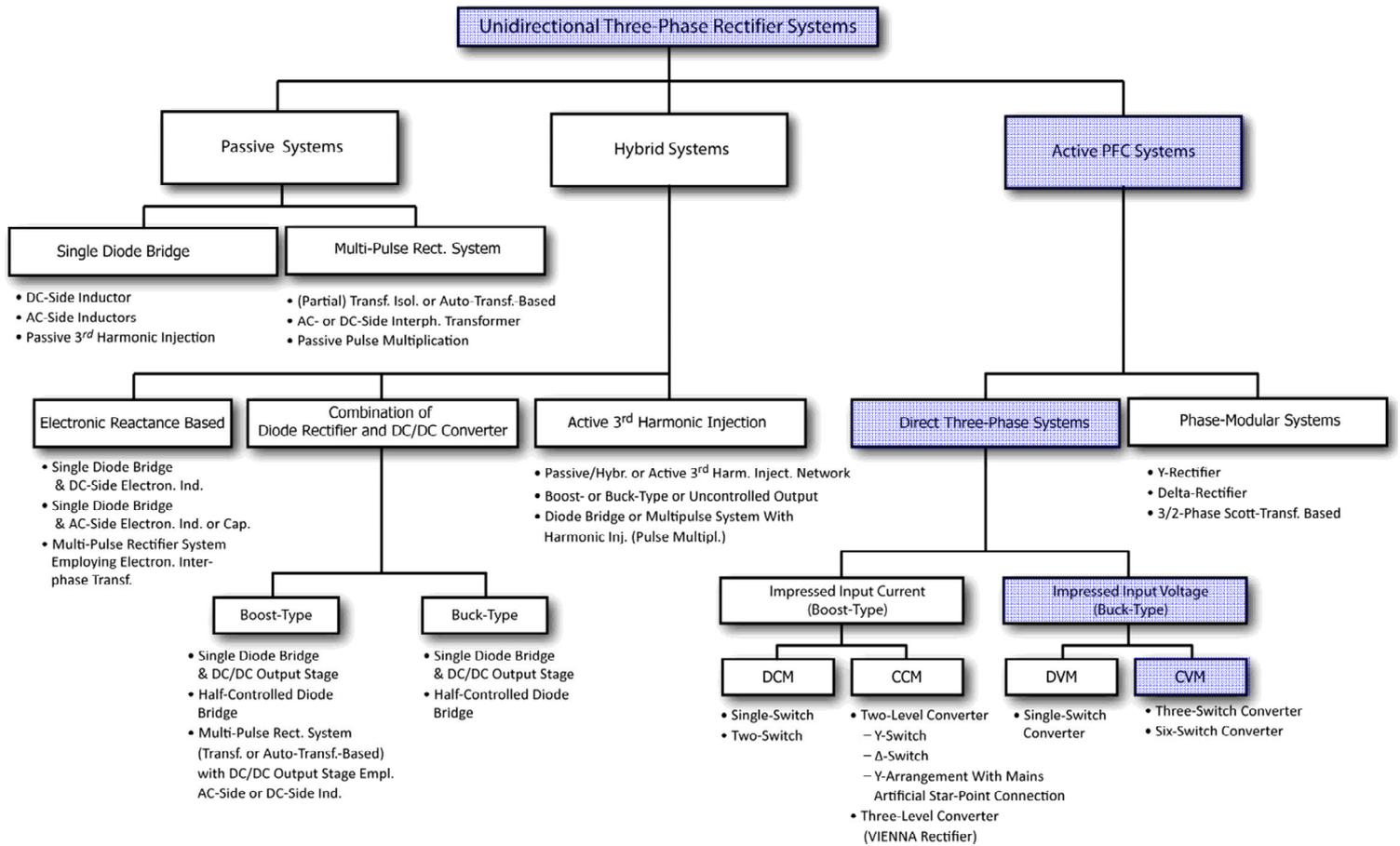


Fig.II.2. Classification of unidirectional three-phase rectifier topologies into passive, hybrid and active systems with Boost or Buck-type characteristics [Kolar et al. 2013]. The three-phase rectifier studied in our application belongs to the highlighted categories.

The six-switch CSAR adopted for our study (Fig.II.3) belongs to the highlighted categories. The presence of the freewheeling diode D_{fw} is optional since the freewheeling can be achieved by the bridge legs; however, its use can reduce the conduction power losses. The six-switch CSAR is chosen because of its ability to improve the power factor, to reduce the harmonic currents at the input ac mains and to regulate the output dc voltage. For this topology, the inrush currents are of low value because the CSAR's switches are connected in series with the input currents.

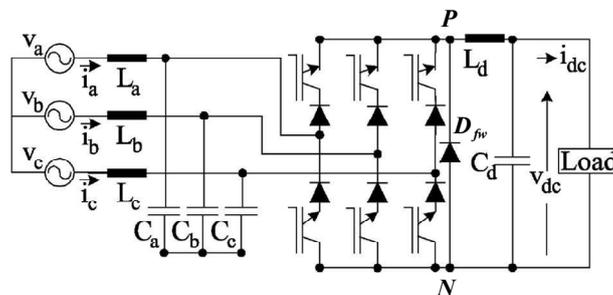


Fig.II.3. Power circuit of the three-phase charger considered for this study.

By examining the structure, we can deduce that the rectifier stage of the charger presents a unidirectional power flow due to the presence of the diodes placed in series with the semi-conductors. This characteristic is imposed by the specifications. However, bidirectional power flow can be achieved if the polarity of the dc output voltage v_{PN} can be inverted. Such bidirectional rectifiers have been proposed in literature, they are labeled as Inverting-Link CSR (IL-CSR). Examples of bidirectional IL-CSR structures are given in Fig.II.4. The power circuit (a) utilizes a lower number of components to ensure bidirectional power flow (lower costs); however, its main drawback is the high number of semiconductors in the current path for both power flow directions. Whereas the power circuit (b) utilizes a higher number of semi-conductors but presents lower conduction power losses.

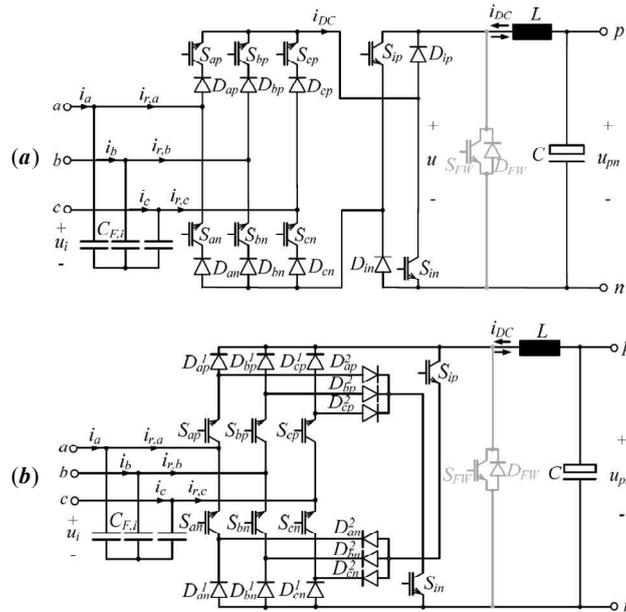


Fig.II.4. Power circuits of IL-CSR systems. (a) A unidirectional six-switch buck-type PFC converter and a current inverting section formed by two power transistors and two diodes, (b) a bidirectional current source converter referred to as integrated inverting-link CSC. Conduction losses for both converters in both power flow directions could be reduced by the implementation of the freewheeling states through S_{FW} and D_{FW} . [Soeiro et al. 2013].

1.2. Three-phase PFC control of current source rectifiers

Various PFC control strategies of three-phase CSRs can be found in the state of art; all of which include an inner current control loop for the management of the power flow throughout the power circuit. For CSRs, the inner control loop consists of either the input ac-side currents or the output dc-side current control of the converter.

1.2.1. DC or AC-side current control

AC-side current control requires the measured input current to be controlled with high dynamics in order to achieve synchronization of the fundamental component of the current with the mains voltages at grid frequency. This is necessary for ensuring a unity power factor (i.e. the converter presents resistive behavior at grid frequency). An example of such control strategy is given in Fig.II.5 (a). However, in the electric vehicle charger, the input current is measured at the input-side of the EMI filter. This means that the current control loop's bandwidth needs to be selected well below the input DM filter's resonance frequency; otherwise, there would be high risks of exciting the input filter's

resonance and inducing control instabilities. Therefore, the inner current control loop is usually combined with the filter capacitor's voltage control. Hence, compromises regarding the choice of the controller's bandwidth must be made.

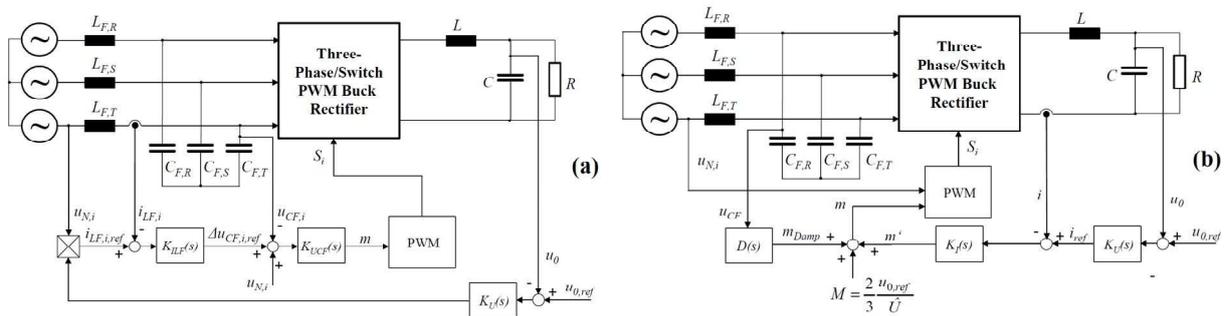


Fig.II.5. Cascaded output voltage control schemes for a three-phase Buck-type rectifier. (a) Inner AC current control combined with the filter capacitor's voltage control and a mains voltage pre-control; (b) inner DC current control combined with an input filter damping [Nussbaumer et al. 2002].

On the other hand, the effectiveness of a DC-side current control has been investigated by [Tooth et al. 2000]. In this case, there is no need to measure the input currents (thus, reducing the number of current sensors); however, input filter damping must be considered in order to suppress the parallel input filter resonances which can lead to the distortion of the input line currents Fig.II.5 (b).

A performance comparison of the two control schemes has been conducted by [Nussbaumer et al. 2002]. The responses of each control concept to a step-like variation of the output voltage, a step-like variation of the input voltages' amplitude and a step-like variation of the output load current have been recorded. The DC-side current control has been found to exhibit a better output voltage tracking and a better rejection of the external disturbances. Therefore, this study will focus on developing a PFC control strategy based on a DC-side current control loop such as the one presented in Fig.II.6 for a six-switch three-phase CSAR.

1.2.2. Displacement phase angle & current harmonics minimization

All power factor correction schemes for CSRs require: the use of a current control loop, the correction of the displacement power factor and the minimization of the input current harmonics.

The control of the active power is achieved through the DC-side current control loop; while the correction of the displacement power factor requires either a direct phase control scheme where a phase lag/lead is added to the rectifier's input currents to compensate for the line currents' phase lead/lag [Wu 2006] - [Yabin et al. 2006] - [Hiti et al. 1994] or a direct power control scheme where the converter's reactive power is compared to a zero reference [Malinowski et al. 2003].

The minimization of the input current harmonics requires the converter to behave as a resistive load over a wide range of low frequencies. Several techniques can be adopted for reducing the input current harmonics among which, the model predictive control [Cortes et al. 2012] - [Rodriguez et al. 2012] and the active damping of the input filter's resonance [Zhang et al. 2015].

This PFC strategy is going to be chosen as the reference strategy for the rest of this Chapter. This means that the strategy developed by [Gati et al. 2013] will be simulated and its simulation results are going to be compared with the results found with my own proposed strategy. The latter is going to be aimed at reducing the level of the dc link current, reducing the switching and conduction power losses as well as achieving better overall performances including a near unity power factor and a low total harmonic distortion rate.

2. Proposed three-phase PFC control

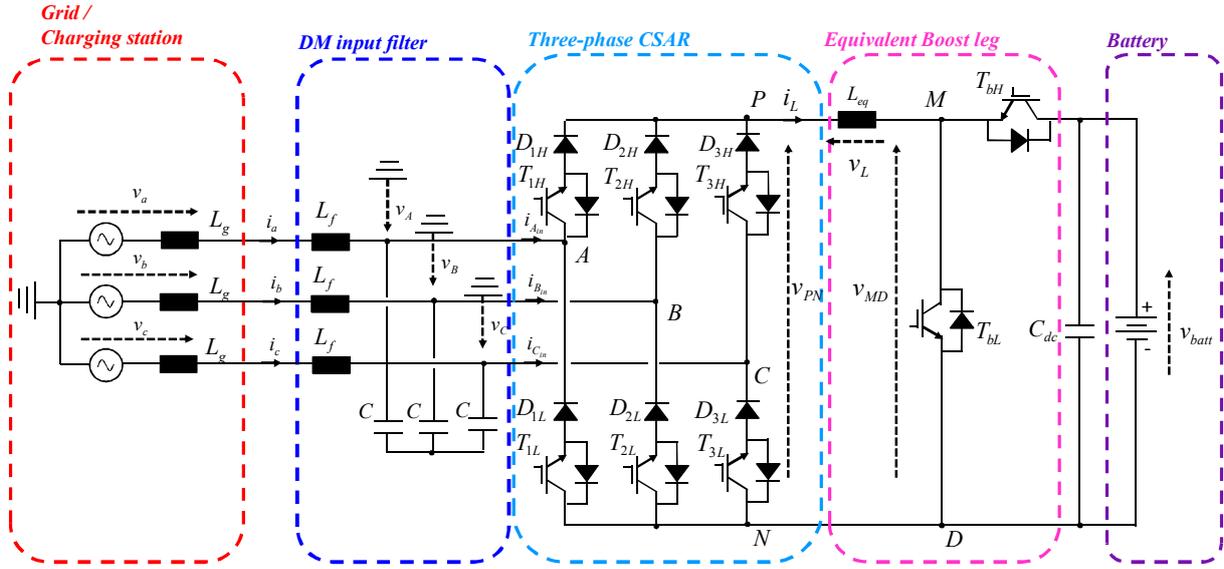


Fig.II.8. Power circuit of the three-phase charger considered for this study.

The three-phase configuration of the charger is given in Fig.II.8. The analysis of the structure is necessary for understanding the power flow management and designing a new PFC control strategy.

2.1. Synchronization with the grid

All PFC control strategies require the extraction of grid-side information. The condition of balanced mains is considered eq. (II.1).

$$v_{ab} + v_{bc} + v_{ca} = 0 \quad \text{eq. (II.1)}$$

Thus, the measurement of two phase-to-phase voltages is sufficient for the extraction of the third phase-to-phase voltage as shown in eq. (II.2).

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ -1 & -1 \end{bmatrix} \cdot \begin{bmatrix} v_{ab} \\ v_{bc} \end{bmatrix} \quad \text{eq. (II.2)}$$

The fundamental components of the phase-to-phase voltages ($v_{ab\alpha}$, $v_{bc\alpha}$, $v_{ca\alpha}$) are extracted using three SOGI filters and are used as inputs for the three-phase PLL. The latter is designed according to Fig.II.9 and provides the information regarding the angular line frequency ω , the amplitude of the phase-to-phase voltages $U_{g\max}$ and the phase of the line voltages θ_v .

In the following, details regarding the three-phase PLL is provided. Let us consider a balanced three-phase system representing the fundamentals of the phase voltages:

$$\begin{cases} v_{a\alpha} = V_{g_{\max}} \cdot \sin(\theta_v) \\ v_{b\alpha} = V_{g_{\max}} \cdot \sin\left(\theta_v - \frac{2\pi}{3}\right) \\ v_{c\alpha} = V_{g_{\max}} \cdot \sin\left(\theta_v + \frac{2\pi}{3}\right) \end{cases} \quad \text{eq. (II.3)}$$

The phase-to-phase voltages can be deduced:

$$\begin{cases} v_{ab\alpha} = U_{g_{\max}} \cdot \sin\left(\theta_v + \frac{\pi}{6}\right) \\ v_{bc\alpha} = U_{g_{\max}} \cdot \sin\left(\theta_v + \frac{3\pi}{2}\right) \\ v_{ca\alpha} = U_{g_{\max}} \cdot \sin\left(\theta_v + \frac{5\pi}{6}\right) \end{cases} \quad \text{eq. (II.4)}$$

For modeling and control design, it is convenient to transform the variables from the a-b-c reference frame to the d-q-0 frame that is rotating at the grid's angular frequency ω . Thus, the transformed steady state variables are invariant in the rotating frame and their coordinates are calculated using the Park transform (based on the Clarke Transform for the conservation of the amplitudes) defined in eq. (II.5). It is applied to the phase-to-phase voltages which yields the expressions in eq. (II.6) of v_d and v_q .

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} \cos(\theta_{PLL}) & \cos\left(\theta_{PLL} - \frac{2\pi}{3}\right) & \cos\left(\theta_{PLL} + \frac{2\pi}{3}\right) \\ -\sin(\theta_{PLL}) & -\sin\left(\theta_{PLL} - \frac{2\pi}{3}\right) & -\sin\left(\theta_{PLL} + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} v_{ab\alpha} \\ v_{bc\alpha} \\ v_{ca\alpha} \end{bmatrix} \quad \text{eq. (II.5)}$$

The q-axis is controlled with a reference value of $v_q^*=0$.

$$\begin{cases} v_d = \frac{2}{3} \cdot \left[\cos(\theta_{PLL}) \cdot v_{ab\alpha} + \cos\left(\theta_{PLL} - \frac{2\pi}{3}\right) \cdot v_{bc\alpha} + \cos\left(\theta_{PLL} + \frac{2\pi}{3}\right) \cdot v_{ca\alpha} \right] \\ v_q = \frac{2}{3} \cdot \left[-\sin(\theta_{PLL}) \cdot v_{ab\alpha} - \sin\left(\theta_{PLL} - \frac{2\pi}{3}\right) \cdot v_{bc\alpha} - \sin\left(\theta_{PLL} + \frac{2\pi}{3}\right) \cdot v_{ca\alpha} \right] \end{cases} \quad \text{eq. (II.6)}$$

The solution of the equation $v_q=0$ is:

$$\theta_{PLL} = \theta_v + \frac{\pi}{2} + \frac{\pi}{6} \quad \text{eq. (II.7)}$$

By replacing this angle in the expression of v_d we can deduce the following:

$$v_d \Big|_{\theta_{PLL}=\theta_v+\frac{\pi}{2}+\frac{\pi}{6}} = -U_{g_{\max}} \quad \text{eq. (II.8)}$$

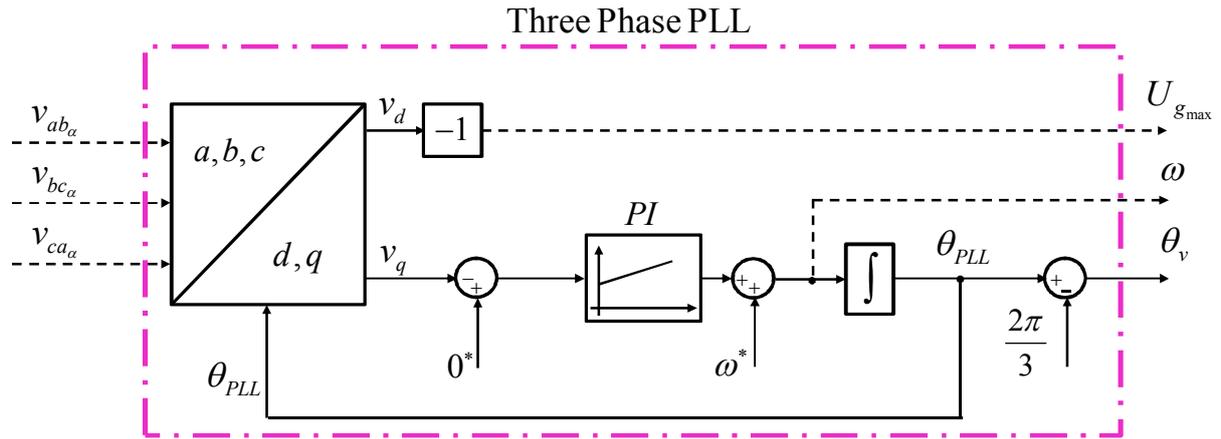


Fig.II.9. Three-phase PLL used for the extraction of the grid-side information.

2.2. Proposed PFC control scheme

This section describes the three-phase PFC control scheme proposed by this study. It ensures the three-phase charging of the EV battery using an ac-dc three-phase six-switch Buck-type current source active rectifier along with a dc-dc Boost output stage.

2.2.1. Control design rules

The PFC control scheme, found in the state of the art, ensures an acceptable power quality performance with regards to the international standards; however, enhancements are proposed by this study in order to further optimize the charger's three-phase operation.

Therefore, the objectives of this new control scheme are:

- the reduction of the levels of the dc current (i_L) flowing through the Boost's filtering inductor for the different operating charging powers;
- the reduction of the levels of the common mode currents flowing towards the frame ground;
- the reduction of the power losses in the charger: switching losses, conduction losses;
- to achieve a near unity power factor: by reducing the harmonic current emissions and regulating the displacement power factor;
- to overcome certain limitations among which: a low filtering inductance on the dc-side, a risk of control instability related to the input EMI filter;
- to only utilize the current and voltage sensors already deployed in the EV charger: dc current sensor (i_L), battery voltage sensor (v_{bat}), grid currents and grid voltages' sensors at the power outlet level (at the input-side of the EMI filter).

2.2.2. Basic principle of operation

A CSAR is characterized by a voltage source at its input and a current source at its output. Therefore, only one high-side (H) and one low-side (L) switch should be turned on at the same time. The instantaneous values of the switching functions of the six switches are given in eq. (II.9).

$$f_{T_{i,j}}(t) = \begin{cases} 1, & \text{if } T_{i,j} \text{ is ON} \\ 0, & \text{if } T_{i,j} \text{ is OFF} \end{cases}; \quad \text{with} \quad \begin{matrix} i = \{1, 2, 3\} \\ j = \{H, L\} \end{matrix} \quad \text{eq. (II.9)}$$

Hence, two switching cells can be distinguished. Each is defined by the three switches of the high-side or the low-side. This translates into eq. (II.10).

$$\sum_{i=1}^3 f_{T_{i,j}}(t) = 1; \quad \text{with } j = \{H, L\} \quad \text{eq. (II.10)}$$

Therefore, the rectifier's input currents can be expressed as a function of the dc current and the defined switching functions, as such:

$$\begin{bmatrix} i_{A_{in}}(t) \\ i_{B_{in}}(t) \\ i_{C_{in}}(t) \end{bmatrix} = \begin{bmatrix} f_{T_{1H}}(t) - f_{T_{1L}}(t) \\ f_{T_{2H}}(t) - f_{T_{2L}}(t) \\ f_{T_{3H}}(t) - f_{T_{3L}}(t) \end{bmatrix} \cdot i_L(t) \quad \text{eq. (II.11)}$$

From here on out, time-domain variables are going to be denoted by lowercase letters without the time insignia. By using the same definitions, the dc output voltage of the rectifier v_{PN} can be expressed as a function of the rectifier's input voltages and the switching functions, as follows:

$$v_{PN} = \begin{bmatrix} f_{T_{1H}} - f_{T_{1L}} \\ f_{T_{2H}} - f_{T_{2L}} \\ f_{T_{3H}} - f_{T_{3L}} \end{bmatrix}^T \cdot \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} \quad \text{eq. (II.12)}$$

At frequencies significantly lower than the switching frequency, the operation of the circuit can be modeled by an average model [Hiti 1995]. The average value of a switching function $f_{T_{i,j}}$ is the duty cycle of the switch $T_{i,j}$ and is denoted as $d_{i,j}$. The following vectors can be defined:

$$\vec{d} = \begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \begin{bmatrix} d_{1H} - d_{1L} \\ d_{2H} - d_{2L} \\ d_{3H} - d_{3L} \end{bmatrix}$$

$$\vec{i}_{in} = \begin{bmatrix} i_{A_{in}} \\ i_{B_{in}} \\ i_{C_{in}} \end{bmatrix} \quad \text{eq. (II.13)}$$

$$\vec{v}_{in} = \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix}$$

Using the definitions presented in eq. (II.13), the average equivalents of eq. (II.10), eq. (II.11) and eq. (II.12) are respectively deduced:

$$\sum_{i=1}^3 d_{i,j} = 1; \text{ with } j = \{H, L\} \quad \text{eq. (II.14)}$$

$$\vec{i}_{in} = \vec{d} \cdot I_L \quad \text{eq. (II.15)}$$

$$V_{PN} = \vec{d}^T \cdot \vec{v}_{in} \quad \text{eq. (II.16)}$$

If only the fundamental components of the variables are considered [Yabin et al. 2006], the fundamental component of the switched input currents of the CSAR can be expressed by:

$$\begin{cases} i_{A_{in}} = I_{in_RMS} \cdot \sqrt{2} \cdot \sin(\theta_v - \alpha) \\ i_{B_{in}} = I_{in_RMS} \cdot \sqrt{2} \cdot \sin\left(\theta_v - \alpha - \frac{2\pi}{3}\right) \\ i_{C_{in}} = I_{in_RMS} \cdot \sqrt{2} \cdot \sin\left(\theta_v - \alpha + \frac{2\pi}{3}\right) \end{cases} \text{ with, } \alpha = \text{angle}(\vec{i}_{in}, \vec{v}_{in}) \quad \text{eq. (II.17)}$$

Using eq. (II.15) and eq. (II.17), the duty cycles are computed:

$$\begin{cases} d_1 = m \cdot \sin(\theta_v - \alpha) \\ d_2 = m \cdot \sin\left(\theta_v - \alpha - \frac{2\pi}{3}\right) \\ d_3 = m \cdot \sin\left(\theta_v - \alpha + \frac{2\pi}{3}\right) \end{cases} \text{ with, } m \text{ being the modulation index} \quad \text{eq. (II.18)}$$

Thus, the modulation index of the CSAR is defined in eq. (II.19) as the ratio of the maximum value of the input line currents over the dc-side current flowing through the filtering inductor [Baumann et al. 2000].

$$m = \frac{I_{in_RMS} \sqrt{2}}{I_L} \quad \text{eq. (II.19)}$$

The range of variation of the CSAR's modulation index is between 0 and a maximum value defined below unity. This is particularly necessary when an active damping of the input filter resonance is implemented alongside the PFC control. It leaves a margin in order to add the modulation index coming from the active damping loop. Here, it is defined at 0.98 because the active damping is not taken into consideration in the control strategy.

$$0 \leq m \leq m_{\max} = 0.98 \quad \text{eq. (II.20)}$$

By substituting eq. (II.3) and eq. (II.18) into equation eq. (II.16), the mathematical model of the rectifier (i.e. the expression of the voltage at the output of the CSAR) can be computed:

$$V_{PN} = \sqrt{\frac{3}{2}} \cdot U_{gRMS} \cdot m \cdot \cos\alpha \quad \text{eq. (II.21)}$$

The maximum voltage that the rectifier can ensure at its output is deduced for $\alpha=0^\circ$.

$$V_{PN_{\max}} = \sqrt{\frac{3}{2}} \cdot U_{gRMS} \cdot m_{\max} \quad \text{with, } U_{gRMS} = \sqrt{3} \cdot V_{gRMS} \quad \text{eq. (II.22)}$$

Moreover, the same analysis regarding the phasor diagrams conducted at the input of the single-phase CSAR can be applied for the input of the three-phase CSAR. This yields the following definition of the phase-angle α between the fundamental components of the input currents of the CSAR (i_{A1in} , i_{B1in} , i_{C1in}) and of the phase voltages (v_{1a} , v_{1b} , v_{1c}).

$$\sin\alpha = \frac{|\bar{I}_C|}{|\bar{I}_{in}|} = \frac{C \cdot \omega \cdot V_{gRMS} \sqrt{2}}{m \cdot I_L} \quad \text{eq. (II.23)}$$

It should be noted that this expression is obtained by neglecting the voltage drop across the line impedances ($L_g\omega + L_r\omega$) at grid frequency.

The charger needs to accommodate a wide input voltage range for the different states of charge of the battery. The battery's voltage reaches 400 V when fully charged. Let us consider a cobalt based Li-ion cell (Table II.1). The battery is formed by 192 cells configured according to two parallel sets each made of 96 cells mounted in series (96S2P). The battery's voltage variation can be deduced in eq. (II.24).

TABLE II.1. VOLTAGE CHARACTERISTICS OF A COBALT BASED LI-ION BATTERY CELL

Nominal cell voltage	Typical end-of-discharge voltage	Maximum charge voltage
3.75 V	2.8 – 3 V	4.2 V

$$96 \times 2.8 = 269V \leq v_{batt} \leq 96 \times 4.2 = 403V \quad \text{eq. (II.24)}$$

On the other hand, the maximum dc output voltage that the three-phase rectifier can provide, for different countries' grid voltage levels, is calculated based on eq. (II.22) and given in Table II.2.

By comparing the range of variation of the battery's voltage with that of the maximum available voltage at the output of the CSAR, we can deduce the following:

- In countries such as Europe, Turkey, Russia, Argentina, Iran, Korea, India and Algeria: the CSAR's output voltage can be controlled to accommodate all the voltage levels of the battery.

- In other countries such as the USA, Brazil and Morocco: The CSAR can provide a maximum output voltage that is lower than the battery's range of voltages, especially the full-charge voltage (400V).

TABLE II.2. ELECTRIC GRID INFORMATION OF THE MAIN MARKETS FOR GROUPE
RENAULT

Main markets for Group Renault*	Grid's Phase Voltage Level (RMS)**	$V_{PN\ max}$
France – Germany – Spain – Italy – UK – Belgium - Luxembourg - India - Algeria	230 V	478 V
Brazil, Morocco	127 V / 220 V (depending on the state)	264 V
Turkey – Russia – Argentina – Iran – Republic of Korea	220 V	457 V
United States of America	120 V	249 V

*Taken from Group Renault's international press releases: <http://media.renault.com/global/fr-fr/rsm/media/pressrelease.aspx?mediaid=74766>

** Taken from the IEC's world plugs standards: http://www.iec.ch/worldplugs/list_bylocation.htm

Based on this analysis, it can be deduced that, for the first set of countries, there is no need to step-up the voltage at the output of the CSAR. Therefore, there is no need for the Boost output stage to be utilized. The Boost's duty cycle is maintained at zero.

However, for the second set of countries, the CSAR is not sufficient on its own to ensure the full-charge operation of the battery. The CSAR can be controlled to provide its maximum dc output voltage $V_{PN\ max}$ and the Boost is operated to ensure the voltage step-up from $V_{PN\ max}$ to v_{batt} .

This yields two modes of operation: a Buck mode operation where the CSAR is controlled via space vector pulse width modulation and the Boost is turned off; and a Buck-Boost mode operation where the CSAR is controlled at its maximum modulation index and the Boost is controlled via PWM.

The control scheme that is elaborated by this study allows the control algorithm to automatically detect whether the Boost converter needs to be activated or not.

2.2.3. Modeling of the CSAR

The design of the power factor correction loop is based on the mathematical description of these two distinct modes of operation presented hereafter.

Equations eq. (II.28) and eq. (II.31) are obtained under the assumption of power conservation in the circuit. This means that the expression of the charging power P_{ch} at the input of the rectifier, in the (d,q,0) frame eq. (II.25), is equalized to the output power eq. (II.26)eq. (II.26).

$$P_{ch} = \vec{v}_{in}^T \cdot \vec{i}_{in} = \frac{3}{2} \cdot V_{g_{max}} \cdot I_{in_d} \quad \text{eq. (II.25)}$$

$$P_{out} = I_L \cdot v_{MD} \quad \text{eq. (II.26)}$$

This yields the CSAR's model in the Buck mode of operation:

$$\text{Buck Mode:} \left\{ \begin{array}{l} v_{batt} \leq V_{PN_{max}} \\ I_{in_d}^* = \frac{I_L^* \cdot v_{batt_{meas}}}{\frac{3}{2} \cdot V_{g_{max}}} \\ d_{boost} = 0 \end{array} \right. \quad \begin{array}{l} \text{eq. (II.27)} \\ \text{eq. (II.28)} \\ \text{eq. (II.29)} \end{array}$$

And the CSAR's model in Buck-Boost mode of operation:

$$\text{Buck-Boost Mode:} \left\{ \begin{array}{l} v_{batt} > V_{PN_{max}} \\ I_{in_d}^* = \frac{I_L^* \cdot V_{PN_{max}}}{\frac{3}{2} \cdot V_{g_{max}}} \\ m = m_{max} = 0.98 \\ d_{boost} = \frac{v_{batt_{meas}} + v_L^* - V_{PN_{max}}}{v_{batt_{meas}}} = 1 - \frac{V_{PN_{max}} - v_L^*}{v_{batt_{meas}}} \end{array} \right. \quad \begin{array}{l} \text{eq. (II.30)} \\ \text{eq. (II.31)} \\ \text{eq. (II.32)} \\ \text{eq. (II.33)} \end{array}$$

Moreover, the rotation matrix used for the transformation from the (d, q, 0) frame to the (α , β , 0) frame is given below:

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = R\left(-\left(\frac{\pi}{2} - \theta_v\right)\right) \cdot \begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix}; \text{ with} \quad \text{eq. (II.34)}$$

$$R\left(-\left(\frac{\pi}{2} - \theta_v\right)\right) = \begin{bmatrix} \cos\left(\frac{\pi}{2} - \theta_v\right) & \sin\left(\frac{\pi}{2} - \theta_v\right) & 0 \\ -\sin\left(\frac{\pi}{2} - \theta_v\right) & \cos\left(\frac{\pi}{2} - \theta_v\right) & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

The control structure can be deduced and is illustrated in Fig.II.10. The interesting part of the control is the use of two saturation blocks with different upper and lower limits that receive the same signal: the desired output voltage of the CSAR v_{PN}^* . The upper and lower limits, of each saturation block, are defined in a way that allows for the algorithm to automatically detect whether the Boost stage needs to be activated or not.

In fact, when the reference signal v_{PN}^* exceeds the maximum voltage that the rectifier can deliver at its output V_{PNmax} , the upper limit of the high-side saturation block forces the rectifier to work at its maximum modulation index, while the rest of the required reference signal is sent to the Boost to be processed. This is the Buck-Boost mode of operation.

However, when the required reference signal v_{PN}^* is lower than the maximum voltage that the rectifier can deliver at its output V_{PNmax} , the rectifier is operated at the adequate modulation index and can achieve the required output voltage on its own. In this case $(v_{PN}^* - V_{PNmax}) < 0$ yields a negative value. As long as this inequality is verified, the low-side saturation block's lower limit forces 0 as the Boost's duty cycle. This is the Buck mode of operation.

It should be noted that our study considers the condition of balanced mains. One can refer to the work presented by [Baumann et al. 2005] for the study of the control structure of a three-phase three-switch CSAR under unbalanced mains. Moreover, the displacement power factor can be taken into consideration by adding a control loop that regulates the amplitude if I_{inq} and the input filter's resonance can be damped by means of active damping.

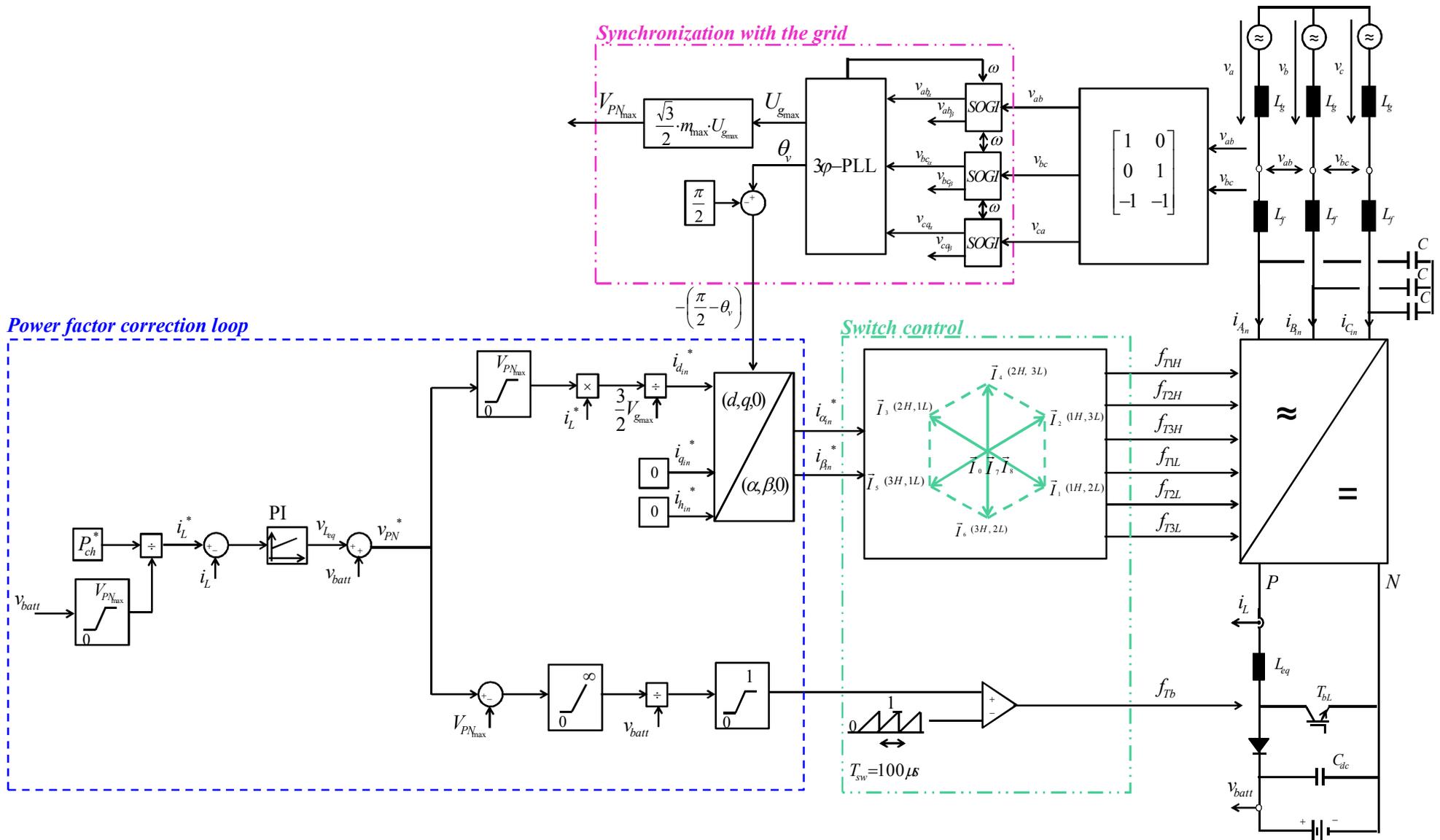


Fig.II.10. Synopsis of the proposed three-phase control strategy.

3. Switch control: Current modulation strategy for the CSAR

The PFC strategy generates reference modulating signals ($i_{\alpha in}^*, i_{\beta in}^*$) at the output of the controller. Based on this desired reference, the duty cycles of the CSAR's switches are generated via a current space vector pulse width modulation technique (SVPWM). In this section, different SVPWM for the six-switch three-phase CSAR are going to be explained, reviewed and evaluated based on certain criteria.

3.1. Extraction of all the possible configurations for the three-phase CSAR

A power converter consisting of n controllable semi-conductors has 2^n possible switching combinations. A non-permissible switching configuration is the one that leads to short-circuiting the voltage source or placing the current source in open-circuit. Therefore, the three-phase CSAR has 2^6 (64) possible switching configurations. When all the permissible switching combinations of the CSAR are considered, only 9 stationary space vectors of the input currents are identified and presented in Table II.3. These permissible combinations consist in turning-on a single switch pair; with one switch belonging to the high-side switches and the other to the low-side switches. The coordinates of these 9 vectors, in the (a, b, c) three-phase stationary reference frame are given as a function of the dc current flowing through the inductor I_L . Among these vectors, 6 represent active state vectors and 3 are zero-state vectors. A zero vector is defined when both switches of the same bridge leg are turned on. This leads to short-circuiting the output dc bus and creates a freewheeling state for the output current flowing through the Boost's filtering inductor.

Table II.3. SVPWM: IDENTIFICATION OF THE CURRENT VECTORS

$f_{T_{1H}}$	$f_{T_{2H}}$	$f_{T_{3H}}$	$f_{T_{1L}}$	$f_{T_{2L}}$	$f_{T_{3L}}$	I_{Ain}	I_{Bin}	I_{Cin}	I_α	I_β	\vec{I}_i	θ_i	
1	0	0	0	1	0	I_L	$-I_L$	0	I_L	$-\frac{1}{\sqrt{3}}I_L$	\vec{I}_1	$-\frac{\pi}{6}$	6 Active State Vectors
1	0	0	0	0	1	I_L	0	$-I_L$	$\frac{1}{\sqrt{3}}I_L$	\vec{I}_2	$\frac{\pi}{6}$		
0	1	0	1	0	0	$-I_L$	I_L	0	$-\frac{1}{\sqrt{3}}I_L$	\vec{I}_3	$\frac{5\pi}{6}$		
0	1	0	0	0	1	0	I_L	$-I_L$	$\frac{2}{\sqrt{3}}I_L$	\vec{I}_4	$\frac{\pi}{2}$		
0	0	1	1	0	0	$-I_L$	0	I_L	$-\frac{1}{\sqrt{3}}I_L$	\vec{I}_5	$\frac{7\pi}{6}$		
0	0	1	0	1	0	0	$-I_L$	I_L	$-\frac{2}{\sqrt{3}}I_L$	\vec{I}_6	$-\frac{\pi}{2}$		
1	0	0	1	0	0	0	0	0	0	\vec{I}_0	-	3 Zero Vectors	
0	1	0	0	1	0	0	0	0	0	\vec{I}_7	-		
0	0	1	0	0	1	0	0	0	0	\vec{I}_8	-		

3.2. Spatial distribution in the (α , β) frame

The coordinates of the stationary space vectors, in the (α , β) reference frame, are also given in Table II.3. The transformation from the (a, b, c) three-phase stationary reference frame to the (α , β , 0) orthogonal stationary reference frame is based on the Clarke transform that retains the amplitudes of the transformed vectors eq. (II.35). However, the calculations made are based on the assumption of a balanced three-phase system. Therefore, the zero sequence's component is null $I_0 = 0$.

$$\begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} I_{A_{in}} \\ I_{B_{in}} \\ I_{C_{in}} \end{bmatrix} \quad \text{eq. (II.35)}$$

The generalized expression of the state vectors is given in eq. (II.36), where $\vec{\alpha}$ and $\vec{\beta}$ represent the unit vectors along the α -axis and the β -axis respectively. On the other hand, the generalized complex expression of the state vectors is given in eq. (II.37) where θ_i represents the angle formed between the α -axis and the state vector \vec{I}_i .

$$\vec{I}_i = I_\alpha \cdot \vec{\alpha} + I_\beta \cdot \vec{\beta} \quad \text{eq. (II.36)}$$

$$\underline{I}_i = \|\vec{I}_i\| \cdot e^{j\theta_i} \quad \text{with} \quad \begin{cases} \theta_i = \arctan 2 \left(\frac{I_\beta}{I_\alpha} \right) & \text{for } i = 1, \dots, 6 \\ \|\vec{I}_i\| = \sqrt{I_\alpha^2 + I_\beta^2} = \frac{2}{\sqrt{3}} I_L & \text{for } i = 1, \dots, 6 \\ \|\vec{I}_i\| = 0 & \text{for } i = 0, 7, 8 \end{cases} \quad \text{eq. (II.37)}$$

The vectors are distributed in a hexagonal shape with the α -axis being merged with the a-axis as can be seen in Fig.II.11. The active state vectors set the limits for 6 sectors numbered from I to VI; each having an opening angle of $\frac{\pi}{3}$.

3.3. Rotating reference vector

A combination of the state vectors, invariant in time and space, is used in the generation of the rotating input current vector of the CSAR. Therefore, Fig.II.11 also shows a reference current space vector \vec{I}_{ref} rotating inside the hexagon at the grid's angular frequency $\omega_v = 2\pi f_g$. In order to maintain a linear control range, the reference vector is located inside the circle inscribed in the hexagon eq. (II.38). This vector's coordinates are the input variables of the SVPWM generation block shown in Fig.II.10.

When the modulation index is larger than unity, the reference vector reaches beyond the circle inscribed in the hexagon. In this case, re-creating the reference vector requires different approaches known as over-modulation techniques. This study will not address this topic; however, several over-modulation techniques applied to three-phase current source converters can be found in [Ojo et al. 2004] – [Zhang et al. 2008] – [Li et al. 2007].

$$\vec{I}_{ref} = i_{\alpha_{in}}^* \cdot \vec{\alpha} + i_{\beta_{in}}^* \cdot \vec{\beta} \quad \text{eq. (II.38)}$$

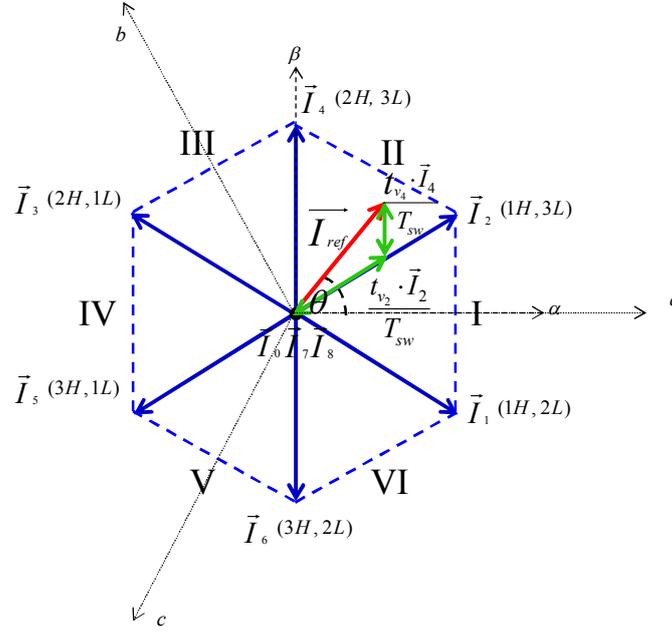


Fig.II.11. Spatial distribution of the current vectors specific to the three-phase CSAR.

3.4. Determination of the sector hosting the reference vector

The method used for the instantaneous detection of the sector in which the reference vector is located is based on the computation of the angle θ between the reference vector and the α -axis.

Since a conventional inverse tangent only generates angles that belong to two quadrants $]-\frac{\pi}{2}, \frac{\pi}{2}[$, it cannot be used to evaluate the position of the reference vector within the entire hexagon. Therefore, the angle is rather calculated using a four-quadrant inverse tangent, $\text{atan2}\left(\frac{y}{x}\right)$, defined as such:

For $i_{\beta_{in}}^* \neq 0$:

$$\theta = a \tan 2 \left(\frac{i_{\beta_{in}}^*}{i_{\alpha_{in}}^*} \right) = \begin{cases} \varphi \cdot \text{sign}(i_{\beta_{in}}^*) & \text{for } i_{\alpha_{in}}^* > 0 \\ \frac{\pi}{2} \cdot \text{sign}(i_{\beta_{in}}^*) & \text{for } i_{\alpha_{in}}^* = 0 \\ (\pi - \varphi) \cdot \text{sign}(i_{\beta_{in}}^*) & \text{for } i_{\alpha_{in}}^* < 0 \end{cases}$$

eq. (II.39)

For $i_{\beta_{in}}^* = 0$:

$$\theta = a \tan 2 \left(\frac{0}{i_{\alpha_{in}}^*} \right) = \begin{cases} 0 & \text{for } i_{\alpha_{in}}^* > 0 \\ \text{undetermined} & \text{for } i_{\alpha_{in}}^* = 0 \\ \pi & \text{for } i_{\alpha_{in}}^* < 0 \end{cases}$$

This is implemented with φ being a single quadrant angle defined as follows:

$$\tan(\varphi) = \left| \frac{i_{B_{in}}^*}{i_{\alpha_{in}}^*} \right| ; \text{ with } 0 \leq \varphi < \frac{\pi}{2} \quad \text{eq. (II.40)}$$

Once the angle θ is computed, a detection algorithm is developed in order to determine the sector in which the rotating reference vector can be found. The logic behind the algorithm is depicted in Table II.4 and takes into account the fact that the four-quadrant inverse tangent generates angles that belong to $]-\pi, \pi[$.

Table II.4. IDENTIFICATION OF THE SECTORS

Sector	Central angle
I	$-\frac{\pi}{6} < \theta \leq +\frac{\pi}{6}$
II	$+\frac{\pi}{6} < \theta \leq +\frac{\pi}{2}$
III	$+\frac{\pi}{2} < \theta \leq +\frac{5\pi}{6}$
IV	$+\frac{5\pi}{6} < \theta \leq +\pi$ and $-\pi < \theta \leq -\frac{5\pi}{6}$
V	$-\frac{5\pi}{6} < \theta \leq -\frac{\pi}{2}$
VI	$-\frac{\pi}{2} < \theta \leq -\frac{\pi}{6}$

The sectors defined by the state vectors of the rectifier's input currents can be further divided into sub-sectors according to the comparison between the mains voltages. However, the input currents $(i_{A_{in}}, i_{B_{in}}, i_{C_{in}})$ can present a delay angle of α° with regards to the input voltages (v_a, v_b, v_c) as illustrated by Fig.II.12. Therefore, two cases are identified: when α can be neglected and when α cannot be neglected.

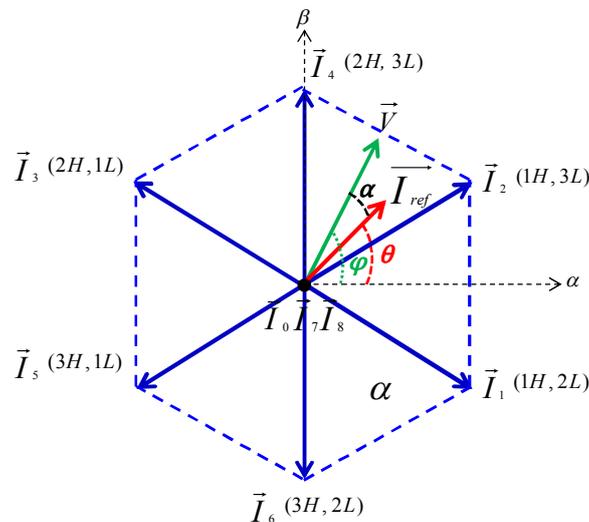


Fig.II.12. Delay angle between the rectifier's input currents and the mains voltages.

3.4.1. Delay angle α° is neglected

If we neglect the delay angle between the mains voltages ($v_{a\alpha}, v_{b\alpha}, v_{c\alpha}$) and the rectifier's input currents ($i_{Ain}, i_{Bin}, i_{Cin}$); each sector can be further divided into 2 subsectors based on the comparison between the instantaneous values of the input voltages deduced in eq. (II.41). These sub-divisions are going to be utilized in the SVPWM strategies to minimize the switching losses.

$$\begin{bmatrix} v_{a\alpha} \\ v_{b\alpha} \\ v_{c\alpha} \end{bmatrix} = \frac{1}{3} \cdot \begin{bmatrix} 2 & 1 \\ -1 & 1 \\ -1 & -2 \end{bmatrix} \cdot \begin{bmatrix} v_{ab\alpha} \\ v_{bc\alpha} \end{bmatrix} \quad \text{for a balanced three-phase system} \quad \text{eq. (II.41)}$$

The boundaries of the 12 subsectors, with regards to the input voltages (Table II.5), are shown in Fig.II.13 and illustrated inside the hexagon in Fig.II.14.

Table II.5. IDENTIFICATION OF THE SUB-SECTORS

Sector	Sub-Sector	Mains voltages	Central angle
I	Ia	$v_{a\alpha} > 0 > v_{c\alpha} > v_{b\alpha}$	$-\frac{\pi}{6} < \theta \leq 0$
	Ib	$v_{a\alpha} > 0 > v_{b\alpha} > v_{c\alpha}$	$0 < \theta \leq +\frac{\pi}{6}$
II	IIa	$v_{a\alpha} > v_{b\alpha} > 0 > v_{c\alpha}$	$+\frac{\pi}{6} < \theta \leq +\frac{\pi}{3}$
	IIb	$v_{b\alpha} > v_{a\alpha} > 0 > v_{c\alpha}$	$+\frac{\pi}{3} < \theta \leq +\frac{\pi}{2}$
III	IIIa	$v_{b\alpha} > 0 > v_{a\alpha} > v_{c\alpha}$	$+\frac{\pi}{2} < \theta \leq +\frac{2\pi}{3}$
	IIIb	$v_{b\alpha} > 0 > v_{c\alpha} > v_{a\alpha}$	$+\frac{2\pi}{3} < \theta \leq +\frac{5\pi}{6}$
IV	IVa	$v_{ab} > v_{c\alpha} > 0 > v_{a\alpha}$	$+\frac{5\pi}{6} < \theta \leq +\pi$
	IVb	$v_{c\alpha} > v_{b\alpha} > 0 > v_{a\alpha}$	$-\pi < \theta \leq -\frac{5\pi}{6}$
V	Va	$v_{c\alpha} > 0 > v_{b\alpha} > v_{a\alpha}$	$-\frac{5\pi}{6} < \theta \leq -\frac{2\pi}{3}$
	Vb	$v_{c\alpha} > 0 > v_{a\alpha} > v_{b\alpha}$	$-\frac{2\pi}{3} < \theta \leq -\frac{\pi}{2}$
VI	VIa	$v_{c\alpha} > v_{a\alpha} > 0 > v_{b\alpha}$	$-\frac{\pi}{2} < \theta \leq -\frac{\pi}{3}$
	VIb	$v_{a\alpha} > v_{c\alpha} > 0 > v_{b\alpha}$	$-\frac{\pi}{3} < \theta \leq -\frac{\pi}{6}$

3.4.2. Delay angle α° cannot be neglected

If the displacement angle is non-zero, the input phase currents are shifted with respect to the input phase voltages (refer to Fig.II.12). In order to minimize the switching voltages irrespective of the displacement angle, the order of the active state vectors should be changed with each transition between sub-sectors.

In this case, a more detailed definition of the sub-sectors' boundaries requires taking the absolute value of the delay angle, defined by $\alpha = |(\widehat{i_{Ain}}, v_{a\alpha})|$, into account.

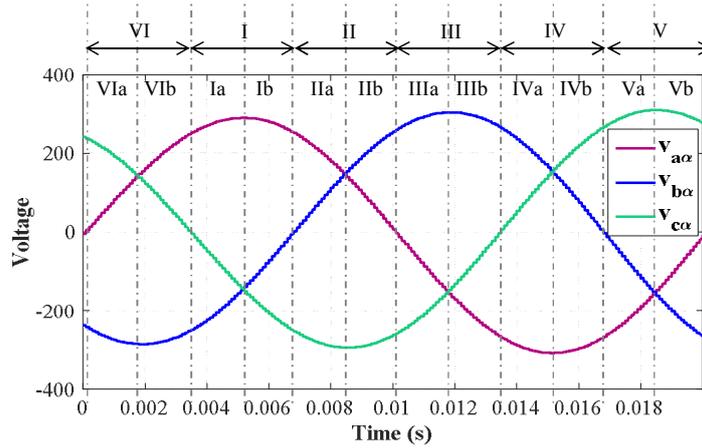


Fig.II.13. Sectors and sub-sectors boundaries with regard to the three-phase input voltages considered to be in phase with the input currents.

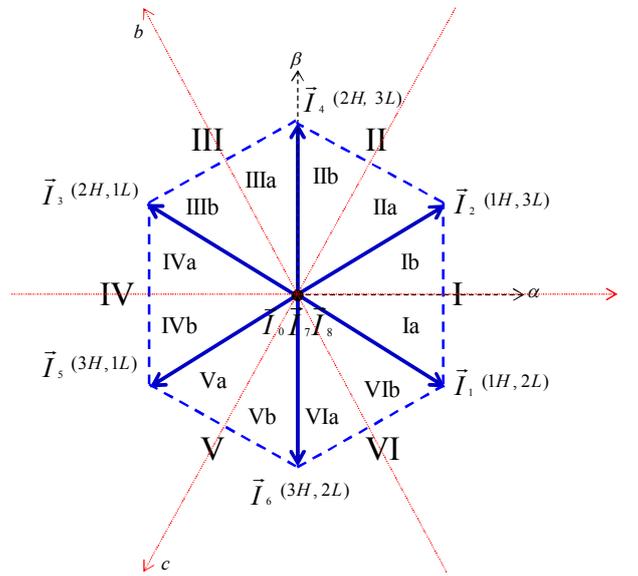


Fig.II.14. Sub-sectors' boundaries inside the hexagon.

The expression of the delay angle α is dependent on the displacement power factor correction scheme. As previously demonstrated, in order to achieve a unity displacement power factor operation, the delay angle should be increased to satisfy the following equation:

$$\alpha \approx a \sin\left(\frac{I_{C\max}}{I_{in\max}}\right) = a \sin\left(\frac{\omega_v \cdot C \cdot V_{g\max}}{m \cdot I_L}\right) \quad \text{eq. (II.42)}$$

The exact definition of the sub-sectors' boundaries, that takes into account the delay angle, helps choosing the order of placement of the vectors inside the switching sequence in a way that optimizes (i. e. minimizes) the switching losses. These boundaries are given in Appendix A.

However, for the sake of simplicity, in the rest of this study we will consider that the delay angle can be neglected in the choice of the space vector modulation strategy. One can refer to [Halkosaari et al. 2000] for the study of a modified full-wave symmetrical modulation scheme that takes the displacement angle into account.

3.5. Computation of the vectors' application durations

The averaged current space vector equal to the reference vector is obtained, usually but not only, as a time weighted linear combination of the two active state vectors adjacent to the reference vector [Yabin et al. 2006]. When the sum of the application durations of the active state vectors is less than the switching period $T_{sw}=100\mu s$, a zero vector ($\vec{I}_0, \vec{I}_7, \vec{I}_8$), noted $\vec{0}$, is applied during the remaining time gap. Taking the example of the current reference vector in sector II, the averaged current space vector is computed in eq. (II.43) using the adjacent vectors \vec{I}_2 and \vec{I}_4 .

$$\vec{I}_{ref} \cdot T_{sw} = \vec{I}_2 \cdot t_{v_2} + \vec{I}_4 \cdot t_{v_4} + \vec{0} \cdot t_{v_0} \quad \text{eq. (II.43)}$$

The objective is to compute the application durations of the active vectors: t_{v_2} & t_{v_4} . Therefore, the previous equation can be re-written as a function of the (α, β) coordinates as follows:

$$\begin{bmatrix} i_{\alpha in}^* \\ i_{\beta in}^* \end{bmatrix} \cdot T_{sw} = \begin{bmatrix} i_{2\alpha} & i_{4\alpha} \\ i_{2\beta} & i_{4\beta} \end{bmatrix} \cdot \begin{bmatrix} t_{v_2} \\ t_{v_4} \end{bmatrix} \quad \text{eq. (II.44)}$$

The extraction of the application durations of the active vectors is made possible by inverting the matrix of coordinates:

$$\begin{bmatrix} t_{v_2} \\ t_{v_4} \end{bmatrix} = T_{sw} \cdot \begin{bmatrix} i_{2\alpha} & i_{4\alpha} \\ i_{2\beta} & i_{4\beta} \end{bmatrix}^{-1} \cdot \begin{bmatrix} i_{\alpha in}^* \\ i_{\beta in}^* \end{bmatrix} \quad \text{eq. (II.45)}$$

Resolving this system leads to the following expressions of the active vector's application durations:

$$\begin{cases} t_{v_2} = m \cdot T_{sw} \cdot \sin(\theta_4 - \theta) = m \cdot T_{sw} \cdot \sin\left(\frac{\pi}{2} - \theta\right) \\ t_{v_4} = m \cdot T_{sw} \cdot \sin(\theta - \theta_2) = m \cdot T_{sw} \cdot \sin\left(\theta - \frac{\pi}{6}\right) \end{cases} \quad \text{eq. (II.46)}$$

Now the zero vectors' application duration can be deduced as such:

$$t_{v_0} = T_{sw} - t_{v_2} - t_{v_4} \quad \text{eq. (II.47)}$$

This method is utilized for the calculation of the vectors' application durations in all of the 6 sectors.

3.6. SVPWM strategies: Choice of the order of the vectors inside a switching sequence

Each state vector can be placed anywhere within the switching period without affecting the averaged space vector computation. This leads to various possibilities for the SVPWM patterns (also called switching sequences).

3.6.1. A common rule leading to the choice of the state vectors

In all cases, the order of the state vectors should minimize the number of switch commutations. Therefore, the transition from one switching state to the next should ensure the commutation of only one pair of switches in order to reduce the switching losses. Therefore, the active state vectors adjacent to the current reference vector are usually chosen for the switching sequence. For instance, if the

reference vector is in sector II, the adjacent active state vectors would be vectors \vec{I}_2 and \vec{I}_4 . The transition between these vectors maintains the switches (T_{3H}, T_{1L} & T_{2L}) OFF and the switch T_{3L} ON. The only pair of switches that commute are T_{1H} & T_{2H}. The same goes for the choice of the zero vector(s) to be employed. This can be generalized to the other sectors.

3.6.2. *Specific criteria dictating the order of the state vectors*

The choice of the order of placement of the state vectors inside a switching sequence depends on a good knowledge of the power electronics topology as well as the criteria to be optimized. Furthermore, each vector can be applied multiple times inside the sequence, if the sum of the application durations of this vector is kept equal to the total computed value. Multiple-criteria can be taken into consideration when choosing the order of the vectors inside the switching sequences; from which we can cite:

a. The minimization of the switching power losses:

a.1. The reduction of the total number of switch commutations per switching period:

This criterion limits the number of times a vector can be applied inside a switching sequence. The variable assigned to the study of this decisive factor is denoted “n”. It refers to the total number of switch commutations per switching sequence.

a.2. The minimization of the voltage fluctuations across the switches during commutation:

In order to compare different modulation strategies under equal conditions, the total switching power losses should be evaluated over a switching period T_s. In order to reduce the switching losses, one should choose the order of the vectors that minimizes the voltages across the switches and series diodes at turn-off.

b. The reduction of the CM voltage generated by the rectifier:

The common mode voltage generated by the three-phase current-source rectifier is defined in eq. (II.48).

$$v_{CM_{rect}} = \frac{v_P + v_N}{2} \quad \text{eq. (II.48)}$$

Therefore, the reduction of the CM voltage is studied with regards to the number and the magnitude of the $\frac{dv_{CM_{CSAR}}}{dt}$ in a switching sequence.

c. The minimization of the dc current ripple:

The dc current is the current flowing through the filtering inductor. In a European grid configuration, the proposed control for the three-phase charging of the battery does not require the activation of the Boost stage. Therefore, the voltage applied across the filtering inductor is expressed as follows:

$$v_L = v_{PN} - v_{batt} \quad \text{eq. (II.49)}$$

Since batteries have very slow dynamics, the battery's voltage can be considered constant for the duration of a switching period. Therefore, the variable used to evaluate the dc current ripple is tied to the dc voltage v_{PN} as such:

$$\frac{di_L}{dt} = \frac{v_{PN} - v_{batt}}{L_{eq}} \quad \text{eq. (II.50)}$$

We will be limiting our study to European grids. However, it is interesting to note that for other types of grids, when the Boost is activated; [Baumann et al. 2002] present an optimized SVM that reduces the amplitude of the inductor current ripple for a Buck+Boost configuration. It is achieved by coordinating the switching operation of the Buck input stage and the Boost output stage. The main difference with our study is that their input stage is a three-switch CSAR whilst our input stage is a six-switch CSAR. Therefore, an adaptation of the SVM strategy of the Buck stage is necessary.

d. The reduction of the input filter capacitor voltage ripple:

This criterion impacts the sizing of the input DM filtering capacitors concerning their voltage stress. Theoretical computations and experimental results for the three-switch Buck-type rectifier are presented in [Baumann et al. 2008] and [Nussbaumer et al. 2008] respectively. The authors evaluate the capacitor voltage ripple through a quality function that is the integral (over a mains period) of the square of the deviation between the actual input capacitor voltage and the reference value. This criterion will not be examined by this study. The main focus being the CM emissions, the switching losses and the output dc current ripple.

e. The minimization of the voltage fluctuations at the negative-side of the dc bus:

On-board chargers share their high-voltage battery's connections with the on-board electronics meant for the ventilation and air conditioning, the 14V low-voltage isolated on-board power system as well as other consumers. Therefore, the stray capacitance formed between the negative side of the battery and the ground frame (chassis) presents a high value, measured around 30nF. Therefore, the minimization of the leakage currents either requires the reduction of this stray capacitance or the minimization of the voltage fluctuations across it (in number and magnitude). However, through software solutions using the SVPWM strategies, it is only possible to reduce the fluctuations of this voltage denoted: dv_N/dt .

3.7. Recovery time management

The control of the current source rectifier needs to provide, at all times, a path for the inductor current to flow. Two cases can be distinguished:

3.7.1. *Absence of a freewheeling diode at the output of the CSAR*

This requires recovery times to be inserted at each vector transition of a switching sequence. These recovery times are necessary in order to prevent, at any moment, over-voltages across the switches and possible failure of the power converter.

Unlike dead-times for voltage source rectifiers, recovery times are ensured by introducing an overlapping time (t_r) between the gating signals of the two IGBTs that are turned-on on each side (the upper as well as the low side) of the CSAR. An example of the recovery time management inside a switching sequence of a CSR, without a freewheeling diode, can be found in [Janiaud et al. 2016] and shown in Fig.II.15.

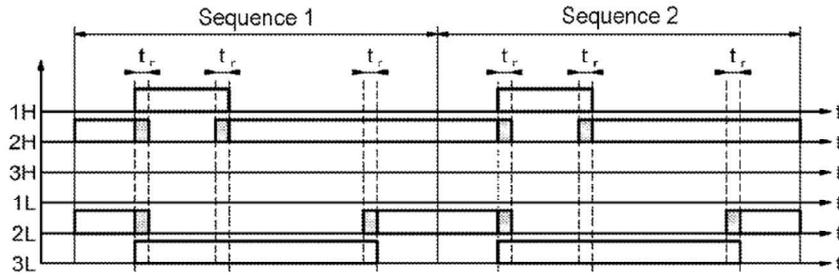


Fig.II.15. Example of the use of recovery times during the transition from one vector to the next inside a switching sequence [Janiaud et al. 2016].

The overlapping time is selected with respect to the gate drive time delays. The value of the overlapping time is kept to a minimum in order to minimize the distortion of the input currents due to “sliding intersections” of the input filter capacitor voltages as described by [Nussbaumer et al. 2006]. “Sliding intersections” might occur when two same-side switches are simultaneously turned-on. In this case, the states of their series diodes are defined by the sign of the phase-to-phase input voltage associated with the two bridge legs being studied. At each sector crossover defined by $(\frac{\pi}{6} + i \times \frac{\pi}{3}, i = 0, \dots, 5)$, Fig.II.13 shows that a phase-to-phase voltage is theoretically equal to zero. However, input voltage ripple around each sector crossover can lead to the simultaneous turn-on of the series diodes. In this case, the voltage across the input DM capacitors placed between these two phases is clamped to zero and a distortion of the currents absorbed from the grid (at the input side of the DM filter) is seen similarly to Fig.II.16.

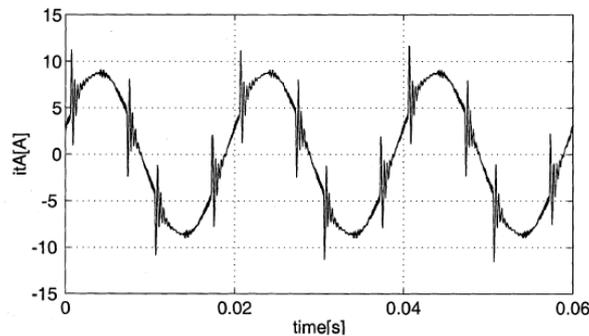


Fig.II.16. Experimental results found in [Salo et al. 2003] showing the supply input current at phase a: i_{tA} showcasing distortions linked to the sliding intersection effect with the absence of overlapping times.

3.7.2. Presence of a freewheeling diode at the output of the CSAR

The presence of a freewheeling diode solves the problem of over-voltages during the transition from one vector to the next. However, if no recovery times are inserted, the differences between the gate drive time delays of the switches will cause short freewheeling states (through the diode) to occur between two active vectors. This multiple switching of the freewheeling diode, inside a switching sequence, increases the switching losses.

In order to maintain the switching losses of the rectifier at minimum; a same-side (upper or lower) CSAR’s IGBT has to be available for current conduction when another same-side IGBT is turned off. This is achieved by introducing an overlapping time of the turn-on states of the same-side switches of both bridge legs [Nussbaumer et al. 2006].

4. Modulation strategies for the six-switch three-phase CSAR

4.1. State of the art: modulation strategies for the six-switch three-phase CSR

Several space vector modulation (SVM) techniques applied to the six-switch CSR can be found in literature and a comparative evaluation is provided. Based on our research, there exist six interesting modulation strategies, presented in literature, for the six-switch three-phase current source rectifier.

The first space vector modulation is presented by [Ripoll et al. 2014]. The study proposes several possible modulation schemes among which we chose to retain the strategy that minimizes the voltage fluctuations at the negative-side of the dc bus. Therefore, we named this strategy Common Mode Reduction Modulation (CMRM) and the sequences applied in each sub-sector are presented in Table II.6.

Furthermore, [Halkosaari et al. 1998] introduce three SVM strategies: the Full-wave Symmetrical Modulation (FSM), the Half-wave Symmetrical Modulation (HSM) and the Modified Half-wave Symmetrical Modulation (MHSM). These are all considered as 4-switch modulation methods. This means that, in each sector, only four switches of the three bridge legs are switched in order to obtain the desired reference phase currents. The last two strategies differ from the FSM through the order of placement of the zero-state vectors for the HSM and the order of placement of the active-state vectors for the MHSM. These strategies do not take into consideration the division of the sectors into two sub-sectors depending on the input voltages.

[Halkosaari et al. 2000-2] present another SVM strategy that shows lower distortion of the supply currents for modulation index lower than 0.64. However, it is a 5-switch strategy since it utilizes two different zero-state vectors in each sector. This could lead to higher switching losses. It is named Centered Space Vector Modulation (CSVM) and is presented in Table II.6.

On the other hand, the same authors [Halkosaari et al. 2000] present a Modified Full-wave Symmetrical Modulation (MFSM) that aims at minimizing the CSAR's switching losses. A similar strategy is presented by [Xu et al. 2013]. The difference amongst these two studies resides in the placement of the zero state vectors inside the switching sequences. The latter shows the loss measurements performed on an all-SiC three-phase Buck rectifier used for data center power supplies [Xu et al. 2015].

Table II.6. SVPWM STRATEGIES FOR THREE-PHASE CURRENT-SOURCE CONVERTERS

Sectors			SVM strategies			
			CMRM	CSVM	MFSM	New MFSM
Switching sequences with respire to the sectors	I	Ia	$[\vec{I}_1][\vec{I}_2][\vec{I}_1][\vec{I}_7]$	$[\vec{I}_7][\vec{I}_1][\vec{I}_2][\vec{I}_0] - [\vec{I}_0][\vec{I}_2][\vec{I}_1][\vec{I}_7]$	$[\vec{I}_0][\vec{I}_2][\vec{I}_1][\vec{I}_1][\vec{I}_2][\vec{I}_0]$	$[\vec{I}_8][\vec{I}_2][\vec{I}_1][\vec{I}_1][\vec{I}_2][\vec{I}_8]$
		Ib	$[\vec{I}_2][\vec{I}_1][\vec{I}_2][\vec{I}_8]$		$[\vec{I}_0][\vec{I}_1][\vec{I}_2][\vec{I}_2][\vec{I}_1][\vec{I}_0]$	$[\vec{I}_7][\vec{I}_1][\vec{I}_2][\vec{I}_2][\vec{I}_1][\vec{I}_7]$
	II	IIa	$[\vec{I}_4][\vec{I}_2][\vec{I}_8]$	$[\vec{I}_0][\vec{I}_2][\vec{I}_4][\vec{I}_8] - [\vec{I}_8][\vec{I}_4][\vec{I}_2][\vec{I}_0]$	$[\vec{I}_8][\vec{I}_4][\vec{I}_2][\vec{I}_2][\vec{I}_4][\vec{I}_8]$	$[\vec{I}_8][\vec{I}_4][\vec{I}_2][\vec{I}_2][\vec{I}_4][\vec{I}_8]$
		IIb			$[\vec{I}_8][\vec{I}_2][\vec{I}_4][\vec{I}_4][\vec{I}_2][\vec{I}_8]$	$[\vec{I}_8][\vec{I}_2][\vec{I}_4][\vec{I}_4][\vec{I}_2][\vec{I}_8]$
	III	IIIa	$[\vec{I}_3][\vec{I}_4][\vec{I}_3][\vec{I}_8]$	$[\vec{I}_8][\vec{I}_4][\vec{I}_3][\vec{I}_7] - [\vec{I}_7][\vec{I}_3][\vec{I}_4][\vec{I}_8]$	$[\vec{I}_7][\vec{I}_3][\vec{I}_4][\vec{I}_4][\vec{I}_3][\vec{I}_7]$	$[\vec{I}_0][\vec{I}_3][\vec{I}_4][\vec{I}_4][\vec{I}_3][\vec{I}_0]$
		IIIb	$[\vec{I}_4][\vec{I}_3][\vec{I}_4][\vec{I}_0]$		$[\vec{I}_7][\vec{I}_4][\vec{I}_3][\vec{I}_3][\vec{I}_4][\vec{I}_7]$	$[\vec{I}_8][\vec{I}_4][\vec{I}_3][\vec{I}_3][\vec{I}_4][\vec{I}_8]$
	IV	IVa	$[\vec{I}_5][\vec{I}_3][\vec{I}_0]$	$[\vec{I}_7][\vec{I}_3][\vec{I}_5][\vec{I}_0] - [\vec{I}_0][\vec{I}_5][\vec{I}_3][\vec{I}_7]$	$[\vec{I}_0][\vec{I}_5][\vec{I}_3][\vec{I}_3][\vec{I}_5][\vec{I}_0]$	$[\vec{I}_0][\vec{I}_5][\vec{I}_3][\vec{I}_3][\vec{I}_5][\vec{I}_0]$
		IVb			$[\vec{I}_0][\vec{I}_3][\vec{I}_5][\vec{I}_5][\vec{I}_3][\vec{I}_0]$	$[\vec{I}_0][\vec{I}_3][\vec{I}_5][\vec{I}_5][\vec{I}_3][\vec{I}_0]$
	V	Va	$[\vec{I}_6][\vec{I}_5][\vec{I}_6][\vec{I}_0]$	$[\vec{I}_0][\vec{I}_5][\vec{I}_6][\vec{I}_8] - [\vec{I}_8][\vec{I}_6][\vec{I}_5][\vec{I}_0]$	$[\vec{I}_8][\vec{I}_6][\vec{I}_5][\vec{I}_5][\vec{I}_6][\vec{I}_8]$	$[\vec{I}_7][\vec{I}_6][\vec{I}_5][\vec{I}_5][\vec{I}_6][\vec{I}_7]$
		Vb	$[\vec{I}_5][\vec{I}_6][\vec{I}_5][\vec{I}_7]$		$[\vec{I}_8][\vec{I}_5][\vec{I}_6][\vec{I}_6][\vec{I}_5][\vec{I}_8]$	$[\vec{I}_0][\vec{I}_5][\vec{I}_6][\vec{I}_6][\vec{I}_5][\vec{I}_0]$
	VI	VIa	$[\vec{I}_1][\vec{I}_6][\vec{I}_7]$	$[\vec{I}_8][\vec{I}_6][\vec{I}_1][\vec{I}_7] - [\vec{I}_7][\vec{I}_1][\vec{I}_6][\vec{I}_8]$	$[\vec{I}_7][\vec{I}_1][\vec{I}_6][\vec{I}_6][\vec{I}_1][\vec{I}_7]$	$[\vec{I}_7][\vec{I}_1][\vec{I}_6][\vec{I}_6][\vec{I}_1][\vec{I}_7]$
		VIb			$[\vec{I}_7][\vec{I}_6][\vec{I}_1][\vec{I}_1][\vec{I}_6][\vec{I}_7]$	$[\vec{I}_7][\vec{I}_6][\vec{I}_1][\vec{I}_1][\vec{I}_6][\vec{I}_7]$

4.2. Evaluation of the strategies based on the performance criteria

In order to evaluate the three current modulation strategies chosen, Fig.II.17 and Fig.II.18 show the comparison of their switching sequences inside an odd (Ia) and an even (IIa) sector respectively. The same analysis is valid for the rest of the sub-sectors. The space vector modulation strategies are being evaluated based on the criteria previously mentioned.

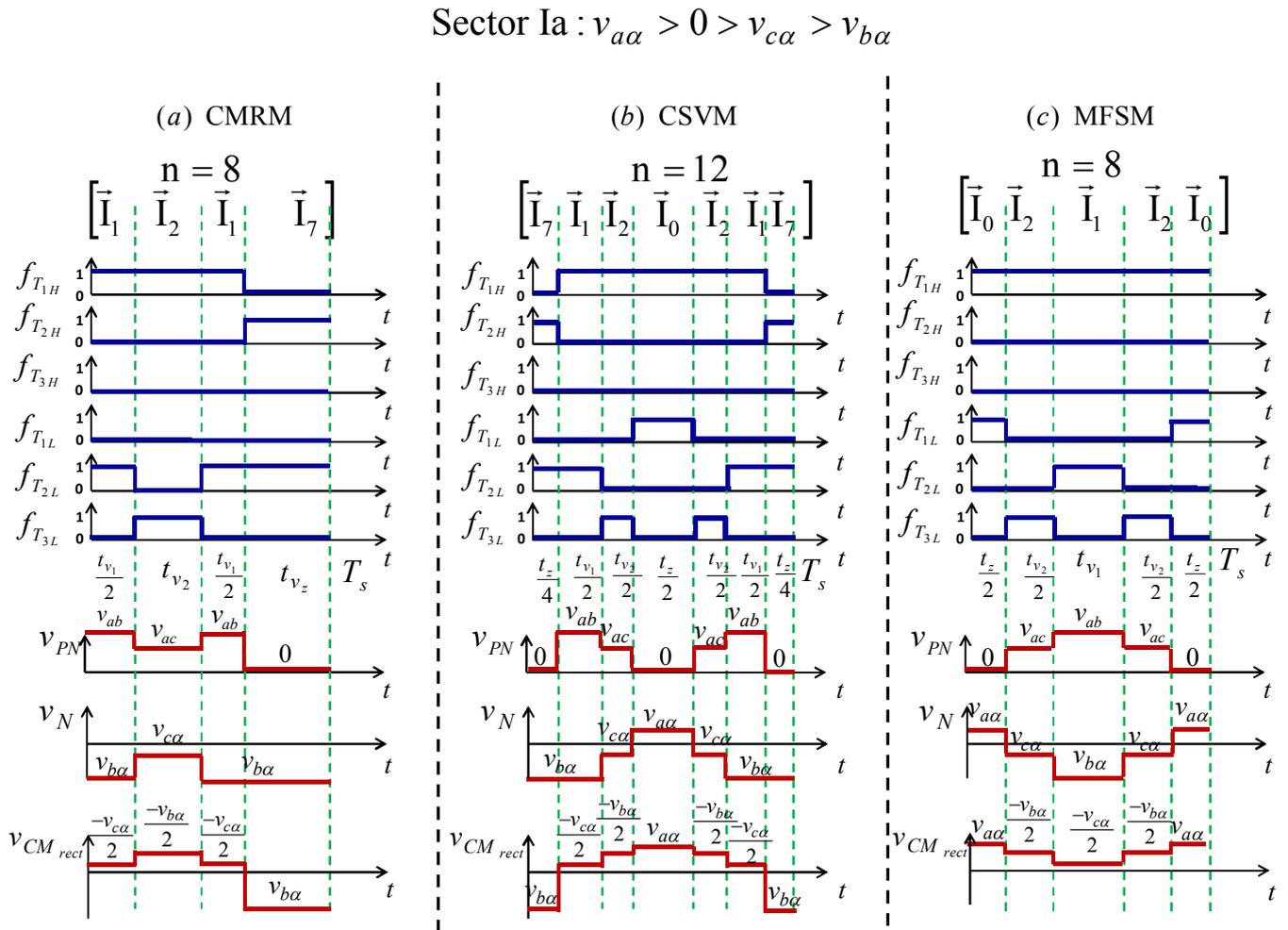


Fig.II.17. Comparison of the performances of the switching sequences inside the odd sub-sector Ia for the following space vector modulation strategies: (a) the CMRM, (b) the CSVM and (c) the MFSM. Evaluation of the total number of switch commutations per switching sequence “n”, the voltage ripple at the output of the CSAR “ v_{PN} ”, the voltage fluctuation across the stray capacitance at the negative side of the battery “ v_N ” and the CM voltage generated by the rectifier “ $v_{CM_{rect}}$ ”.

4.2.1. Minimization of the amplitude and the number of fluctuations of v_N

This is directly related to the high capacitive coupling between the high-voltage battery and the frame ground (it will be further examined in Part B Chapter 2). By investigating the waveforms of v_N inside a switching sequence we can deduce that the CMRM is the one that minimizes the fluctuations of this voltage. In fact, this modulation strategy stabilizes v_N across the even sectors and confines its fluctuations between the negative voltages in each odd sub-sector; thus, reducing the amplitude of the variations. The MFSM presents similar behavior in the even sector; however, it generates more CM

emissions, through the battery's stray capacitance, in the odd sectors. Judging by this criterion, the CSVM shows the least favorable behavior of all three strategies.

Sector IIa : $v_{a\alpha} > v_{b\alpha} > 0 > v_{c\alpha}$

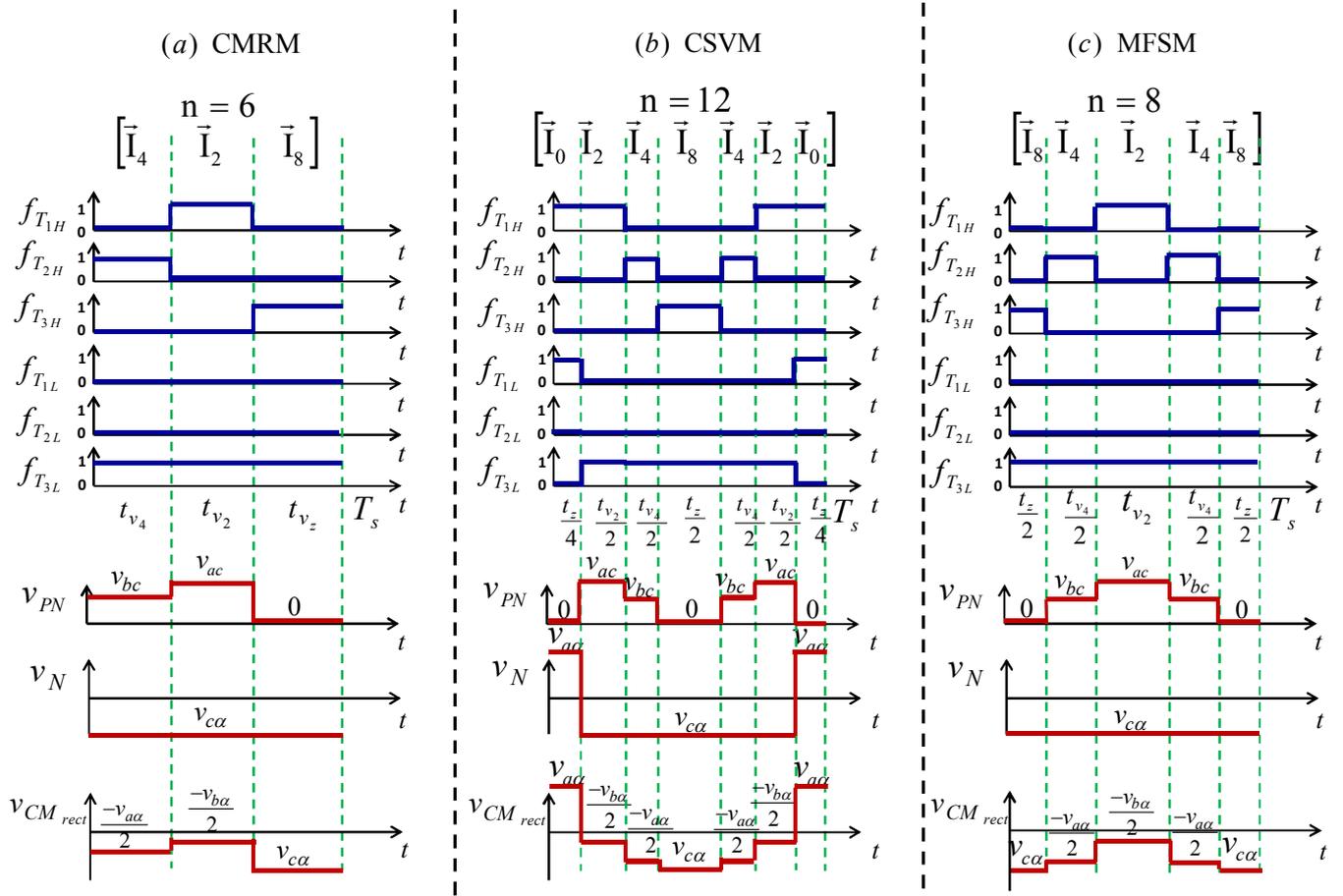


Fig.II.18. Comparison of the performances of the switching sequences inside the even sub-sector IIa for the following space vector modulation strategies: (a) the CMRM, (b) the CSVM and (c) the MFSM. Evaluation of the total number of switch commutations per switching sequence “ n ”, the voltage ripple at the output of the CSAR “ v_{PN} ”, the voltage fluctuation across the stray capacitance at the negative side of the battery “ v_N ” and the CM voltage generated by the rectifier “ v_{CMrect} ”.

4.2.2. Minimization of the switching power losses

a. Minimization of the total number “ n ” of commutations inside a switching sequence

It is clear that the CMRM is slightly superior compared to the rest of the modulation strategies. It requires two less commutations than the MFSM in the even sectors. This contributes to lowering the switching losses.

b. Minimization of the voltage fluctuations across the switches during commutation

Since the CSVM is a 5-switch modulation, it generates the highest switching power losses. Therefore, this paragraph focuses on the study of the voltage fluctuations across the switches at turn-off/on using

the CMRM and the MFSM. To illustrate that, Fig.II.19 and Fig.II.20 shows the voltages across the switches in an odd and an even sector respectively. These voltages are expressed as:

$$\begin{cases} v_{K1H} = v_A - v_P \\ v_{K2H} = v_B - v_P \\ v_{K3H} = v_C - v_P \end{cases} ; \begin{cases} v_{K1L} = v_N - v_A \\ v_{K2L} = v_N - v_B \\ v_{K3L} = v_N - v_C \end{cases} \quad \text{eq. (II.51)}$$

It can be deduced that the MFSM organizes the order of the vectors inside a switching sequence in a way that avoids the application of the phase-to-phase voltage with the highest amplitude across the switches (v_{ab} in sector Ia and v_{ac} in sector IIa).

Sector Ia : $v_{a\alpha} > 0 > v_{c\alpha} > v_{b\alpha}$

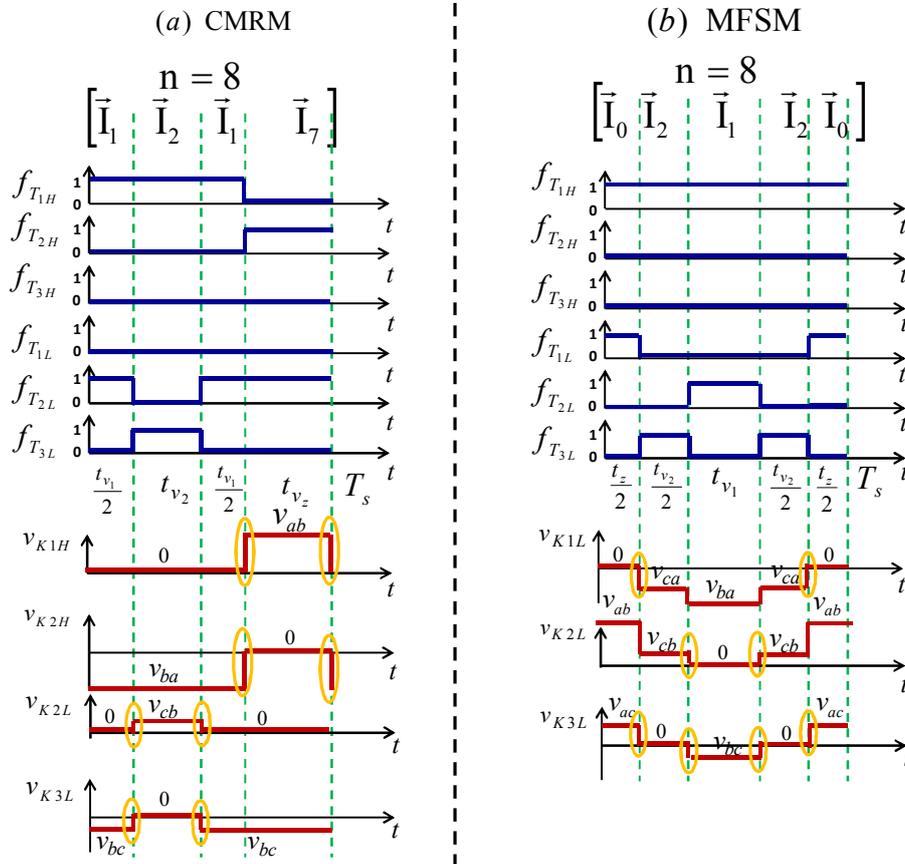


Fig.II.19. Voltages across the switches in the odd sub-sector Ia for the following space vector modulation strategies: (a) the CMRM and (b) the MFSM.

4.2.3. Minimization of the CM voltage generated by the CSAR v_{CMrect}

This criterion is evaluated by considering the number and the amplitude of the CM voltage variations inside a switching sequence. The least favorable being the CSVM.

Sector IIa : $v_{a\alpha} > v_{b\alpha} > 0 > v_{c\alpha}$

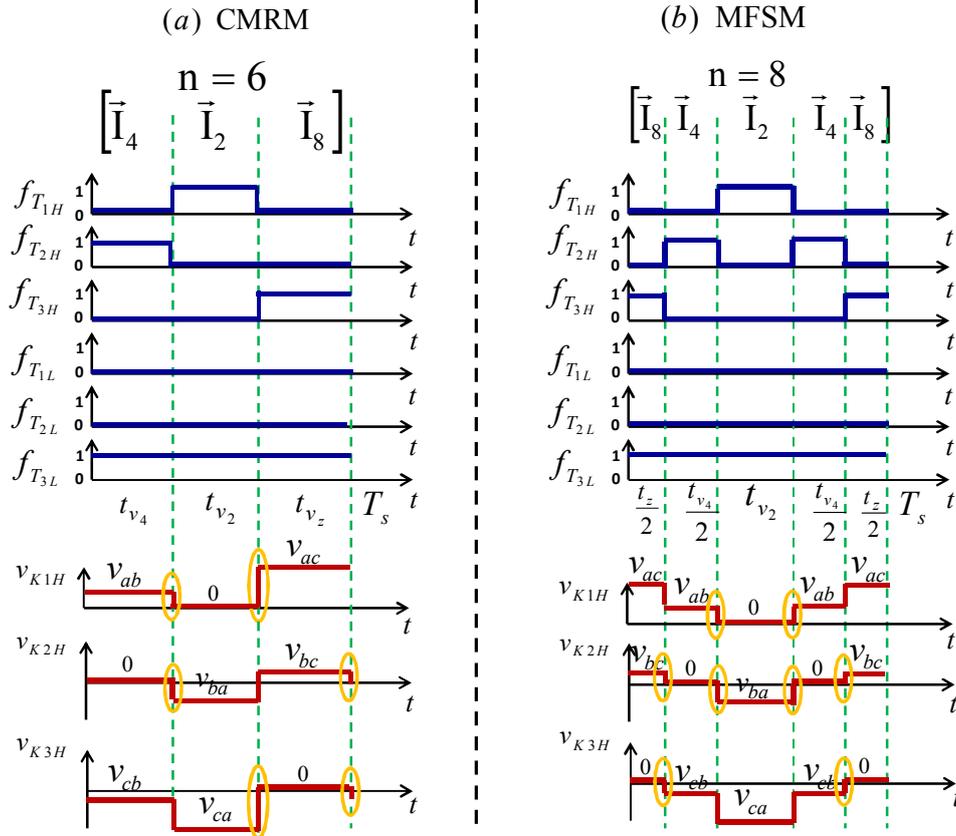


Fig.II.20. Voltages across the switches in the even sub-sector IIa for the following space vector modulation strategies: (a) the CMRM and (b) the MFSM.

4.2.4. Minimization of the ripple of the dc output current

The current ripple at the dc output of the CSAR is evaluated by studying the current's variation given in eq. (II.50). In order to study the current ripple, we will consider the waveforms of v_{PN} in sector Ia. From the latter, we can deduce the waveforms of i_L given in Fig.II.21. The duration of application of the vectors in this sector, for a given reference vector, are the same regardless of the modulation strategy adopted. The absolute values of the current ripples are deduced:

$$\left\{ \begin{array}{l} \Delta i_L|_{CMRM} = \Delta i_L|_{MFSM} = \frac{v_{batt}}{L_{eq}} \cdot t_z \\ \Delta i_L|_{CSV M} = \frac{\Delta i_L|_{CMRM}}{2} = \frac{v_{batt}}{L_{eq}} \cdot \frac{t_z}{2} \end{array} \right. \quad \text{eq. (II.52)}$$

Unlike with the other strategies, in the CSV M, half of the duration of application of the zero-vector is applied at the middle of the sequence. This leads to the reduction of the current ripple by half of the amount.

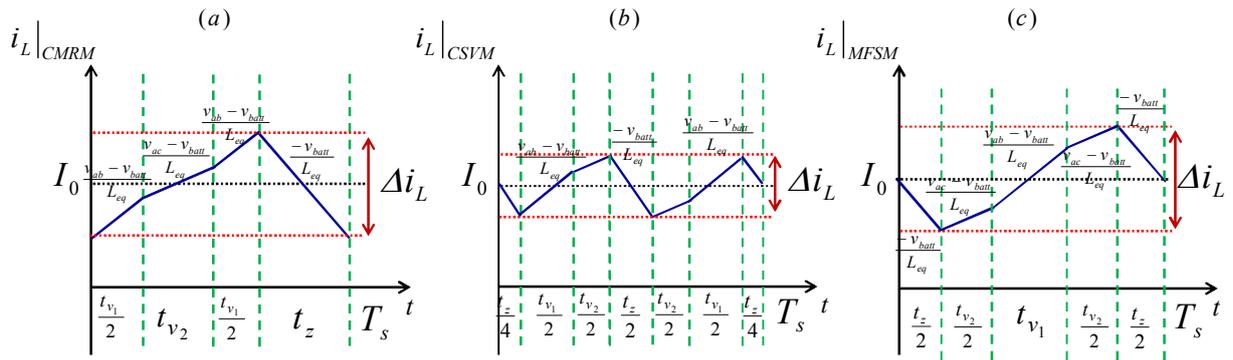


Fig.II.21. Waveforms of the dc output current for a switching sequence inside sector Ia for: (a) CMRM, (b) CSVM and (c) MFSM.

Table II.7 summarizes the comparison between the performances of the three strategies. The CMRM and the MFSM present supreme performances irrespective of the CSVM except for the dc current ripple. Furthermore, the MFSM presents lower switching power losses. The next objective is to modify the MFSM in a way that would enhance (i.e. reduce) the fluctuations of v_N .

Table II.7. EVALUATION OF THE SPACE VECTOR MODULATION STRATEGIES

		Minimization of $\frac{dv_N}{dt}$	Minimization of n	Reduction of V_{CMrect}		Minimization of the switching power losses	Minimization of Δi_L
				Odd sectors	Even sectors		
Current modulation strategy	CMRM	😊	😊	😐	😊	😐	😐
	CSVM	😞	😞	😞		😞	😊
	MFSM	😐	😐	😊	😐	😊	😐
	New MFSM	😊	😐	😊	😐	😊	😐

4.3. Proposed switching sequence

It is named the “new MFSM”. It is obtained by changing the choice of the zero-state vectors made in the odd sectors (I, III and V) of the MFSM and their associated sub-sectors. The new sequences can be found in Table II.6.

Fig.II.22 shows the new modulation strategy’s performances compared to the MFSM. The voltage at the output of the CSAR remains unchanged. This means that the output dc-current ripple is the same as for the MFSM.

Furthermore, changing the zero-vectors used in the odd sectors eliminates two fluctuations from the voltage at the negative side of the battery v_N . This renders the performances of the new MFSM, for this criterion, equivalent to those of the CMRM. Moreover, compared to the CMRM, the new strategy presents the same performances as the MFSM with regards to the CM voltage of the CSAR.

However, the modification of the zero-vectors in the odd sectors comes at the expense of one more switch being commutated in the odd-sectors. The new MFSM becomes a 4-switch modulation in the odd sectors and a 3-switch modulation in the even sectors. Even though more switches are commutated in the odd sectors; nonetheless, the total amount of commutations per switching sequence is maintained at 8 and the voltages across the switches are preserved (confer Fig.II.22). This means that the new MFSM maintains the property of reduced switching losses as the MFSM.

The new strategy presents overall good performances when it comes to reducing the CM emissions and minimizing the switching losses. Even though it does not reduce the dc-current’s ripple, one should keep in mind that the new control strategy allows, for a given charging power, a lower level of dc current to flow through the dc filtering inductor. This leads to the possibility of increasing the inductance value for the same volume of inductor and thus reducing the current ripple by means of hardware modification.

In order to validate the previous analysis, simulations are going to be carried with the control strategy presented in Fig.II.10 for the various current modulation strategies: CMRM, CSVM, MFSM and new MFSM.

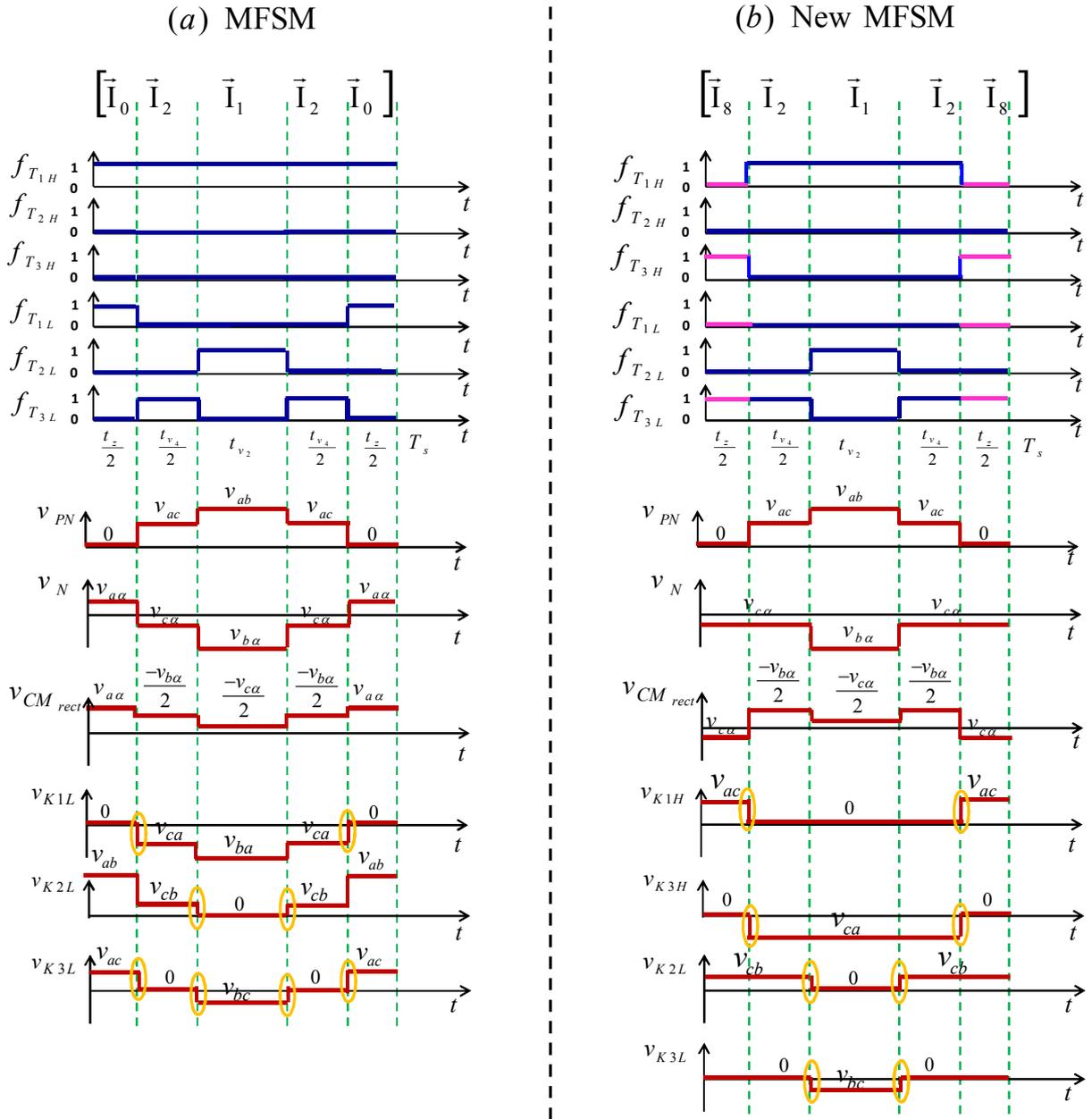


Fig.II.22. Comparison of the performances of the switching sequences inside the odd sub-sector Ia for the following space vector modulation strategies: (a) the MFSM and (b) the new modified MFSM.

5. Simulation results

5.1. Co-simulations between Matlab and Psim

The simulations are carried using a common platform between MATLAB 2011a and PSIM 9.1.3. The co-simulation is made possible through the use of a SimCoupler module added to MATLAB's libraries (Fig.II.23).

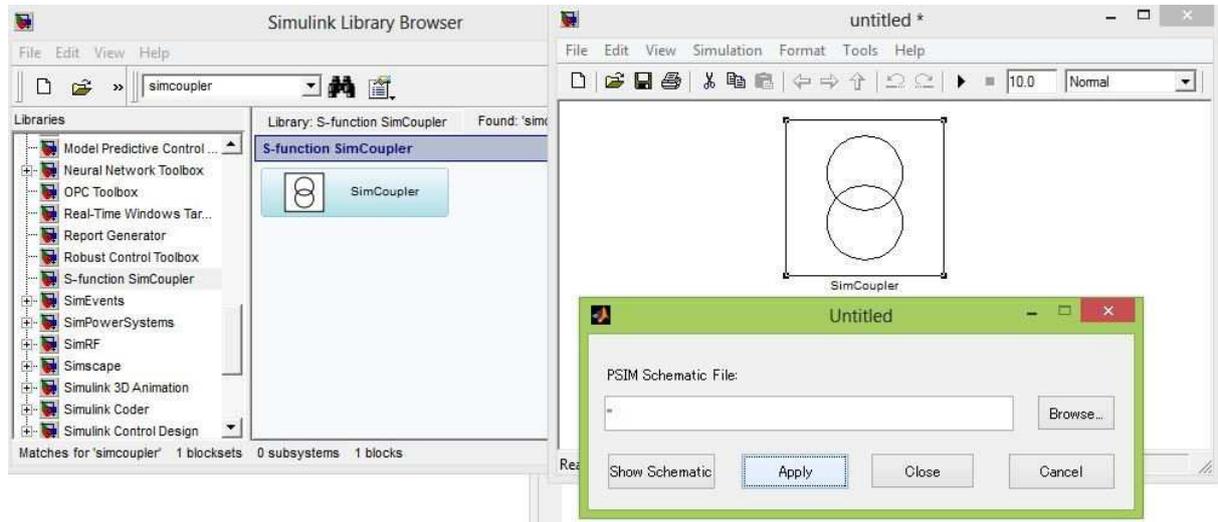


Fig.II.23. The SimCoupler module in MATLAB 2011a.

SimCoupler combines PSIM with MATLAB's Simulink by providing an interface for co-simulations. Therefore, parts of a system can be implemented and simulated in PSIM and the rest in Simulink. Both softwares communicate back and forth by sending signals in and out through SimCoupler.

Therefore, the SimCoupler module enables Simulink users to implement and simulate power circuits in their original circuit form under PSIM. Simultaneously, the same module allows power electronics designers to simulate control in MATLAB's Simulink environment; thus, enhancing PSIM's control simulation capability by providing access to numerous Simulink toolboxes.

An example of the simulations carried in this section is given in Appendix B. The power circuit and the voltage/current sensors are implemented using PSIM and the control (three-phase PFC + space vector current modulations strategies) is implemented using Simulink. The only condition required for a reliable co-simulation is to program both softwares to run with the same fixed-step parameter. One can refer to [Powersys 2004] for a detailed tutorial on the use of the SimCoupler module.

The continuous time control presented in Fig.II.10 is digitalized using the PI controller discretization methods presented in [Buso 2006]. For an ultimate implementation of the control using a digital signal processor (DSP), three main time delays can be identified. They are due to:

1. the sampling of the control signals;
2. the calculation time of the DSP;
3. and the sample-and-hold function of the pulse-width modulator.

Methods for compensating these time delays are presented by [Nussbaumer et al. 2008_2].

5.2. Analysis of the results

The simulations are going to be carried for a 22 kW charging power while considering the voltage across the battery to be around 300 V at the beginning of the charge. The harmonic content of the mains' currents, absorbed at the grid side, is going to be evaluated and the compliance with the appropriate IEC standard is going to be studied [IEC 61000 3-12 2003].

The IEC 61000 3-12 is applicable in the case of a mains current of 32 Arms. It states that the individual harmonics up to the rank 13 should meet the limits specified in Table II.8. Moreover, the Total Harmonic Distortion (THD) and the Partial Weighted Harmonic Distortion (PWHD), defined in eq. (II.53), should be lower than 23%. The PWHD is employed in order to ensure that the effects of the higher order harmonic currents ($n \geq 14$) are sufficiently reduced without specifying their individual limits.

$$\left\{ \begin{array}{l} THD (\%) = 100 \cdot \sqrt{\sum_{n=2}^{40} \left(\frac{I_n}{I_1}\right)^2} \\ PWHD (\%) = 100 \cdot \sqrt{n \cdot \sum_{n=14}^{40} \left(\frac{I_n}{I_1}\right)^2} \end{array} \right. \quad \text{eq. (II.53)}$$

Where, n is the rank of the current harmonic and I_n is the RMS value of the n^{th} harmonic.

Table II.8. LIMITS DEFINED BY THE IEC 61000-3-12 (THE CURRENTS ARE IN ARMS AND THE HARMONIC DISTORTION RATES ARE IN %)

I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	THD	PWHD
4	21.6	2	10.7	1.3	7.2	1	3.8	0.8	3.1	0.7	2	23	23

In total, three simulations are presented below.

➤ Configuration I :

The existing PFC control strategy in the state of the art (i.e. the same as the one presented by [Gati et al. 2013]) is implemented along with the CMRM also taken from literature. The simulation results are presented in Fig.II.24 and Fig.II.25.

➤ Configuration II:

In order to evaluate the impact of the proposed three-phase control strategy, the CMRM is kept the same; however, the new PFC control strategy (Fig.II.10) is implemented. The associated simulation results are presented in Fig.II.26, Fig.II.27 and Fig.II.28.

➤ Configuration III:

Once the new PFC control is evaluated, one can proceed to study the performances of the new space vector current modulation strategy. Therefore, the new proposed PFC control is maintained and the new MFSM is implemented. The associated simulation results are presented in Fig.II.30, Fig.II.31 and Fig.II.32.

By comparing the results obtained in configurations I (Fig.II.24) & II (Fig.II.26), we can deduce that the new proposed PFC control strategy ensures a better power factor (0.996) and reduces the average value of the current flowing through the converter for the same charging power (dc link current goes from 120 A to 73 A).

Moreover, it greatly reduces the switching power losses. In fact, in the proposed PFC control, the Boost is not activated for grid levels of (230 Vrms). This means that the Boost's low-side IGBTs are maintained in the "off" position, for the duration of the charge, while the CSAR is switched according to the switching sequences generated by the CMRM. This is not the case for the state of the art PFC control where the CSAR's switches are commutated according to the CMRM while the Boost's three low-side switches and high-side diodes are simultaneously controlled via pulse width modulation.

Furthermore, the input mains currents present a low frequency distortion which is linked to the DM input filter's parallel resonance. The active damping control that was developed for the single-phase PFC control can also be implemented for the three-phase PFC strategy.

In each configuration, the harmonic content of the currents absorbed at the grid side is compared to the limits defined by the IEC 61000-3-12 standard regarding the harmonic current emissions. By comparing the results shown in Fig.II.25 and Fig.II.27, we can deduce that the proposed PFC control reduces the harmonic content (the total harmonic distortion factor is reduced) and achieves the compliance with the standard with regards to the higher order harmonics (PWHD < 23%).

In order to further enhance the performances achieved with the new proposed PFC control, we shall evaluate the use of the proposed current modulation strategy for the control of the gating signals of the CSAR's switches. To this end, let us study the comparison between the configurations II & III. The difference between these two configurations resides in the choice of the current space vector modulation strategy.

It can be seen that the CMRM (Fig.II.28) and the new MFSM (Fig.II.32) both generate equivalent voltage fluctuations across the stray capacitance at the negative side of the battery (v_N) and equivalent dc current ripple (Fig.II.30), as shown in the previous demonstrations. In addition, the new MFSM reduces even further the switching losses and the harmonic content of the mains currents (Fig.II.31) while keeping a good power factor (0.995).

One should keep in mind that the results are presented with an input filter only consisting of a DM filtering inductor and capacitor. No passive damping is taken into account in these simulations even though passive damping is an industrial requirement. It is necessary since active damping cannot prevent the input filter from oscillating at light loads nor when the charger is plugged-in but turned off. When included, the passive damping will enhance the distortions seen at the mains currents.

In addition, the results, presented in Fig.II.28 / Fig.II.29 and Fig.II.32 / Fig.II.33, validate the theoretical developments and analysis made in Fig.II.17 (a) / Fig.II.18 (a) and Fig.II.22 (b) / Fig.II.18 (c) for the odd and even sectors respectively.

5.2.1. Configuration I: CMRM & state of the art PFC control strategy

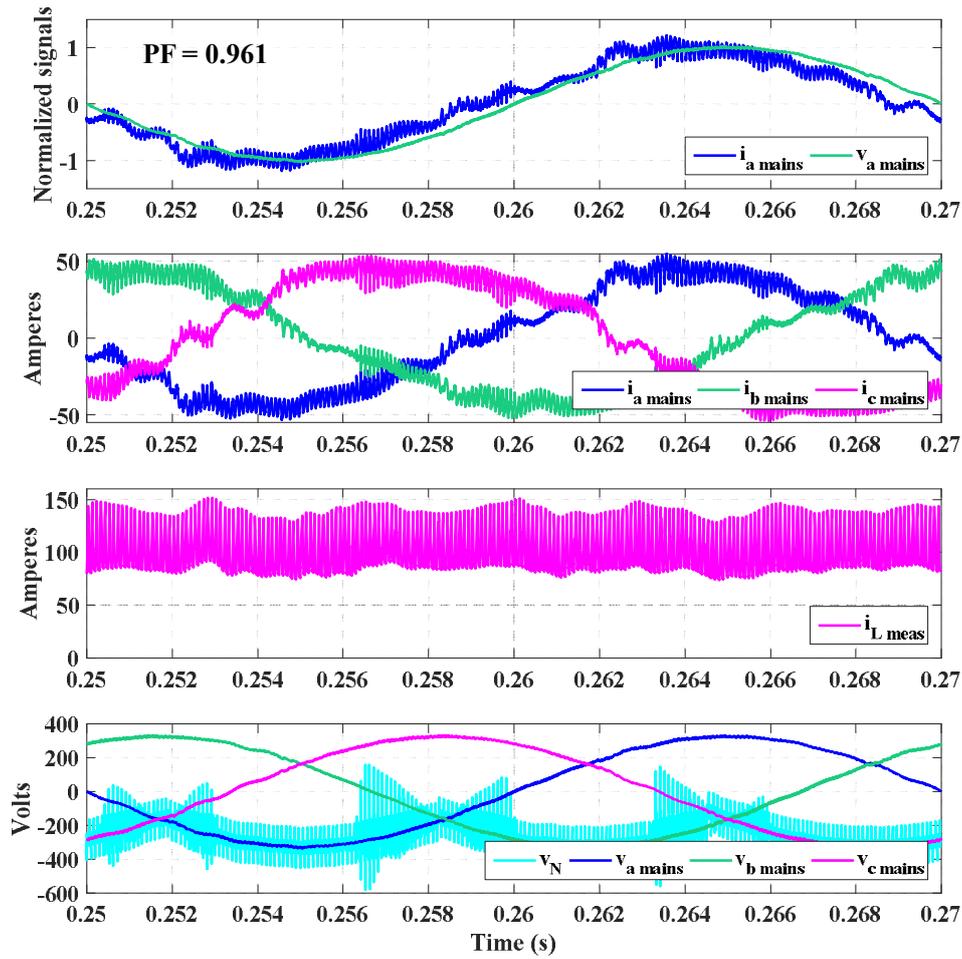


Fig.II.24. Configuration I: Waveforms of the input mains currents ($i_{a \text{ mains}}$, $i_{b \text{ mains}}$ & $i_{c \text{ mains}}$), the measured dc link inductor current ($i_{L \text{ meas}}$), the input mains voltages ($v_{a \text{ mains}}$, $v_{b \text{ mains}}$ & $v_{c \text{ mains}}$) and the voltage between the node N and the frame ground v_N .

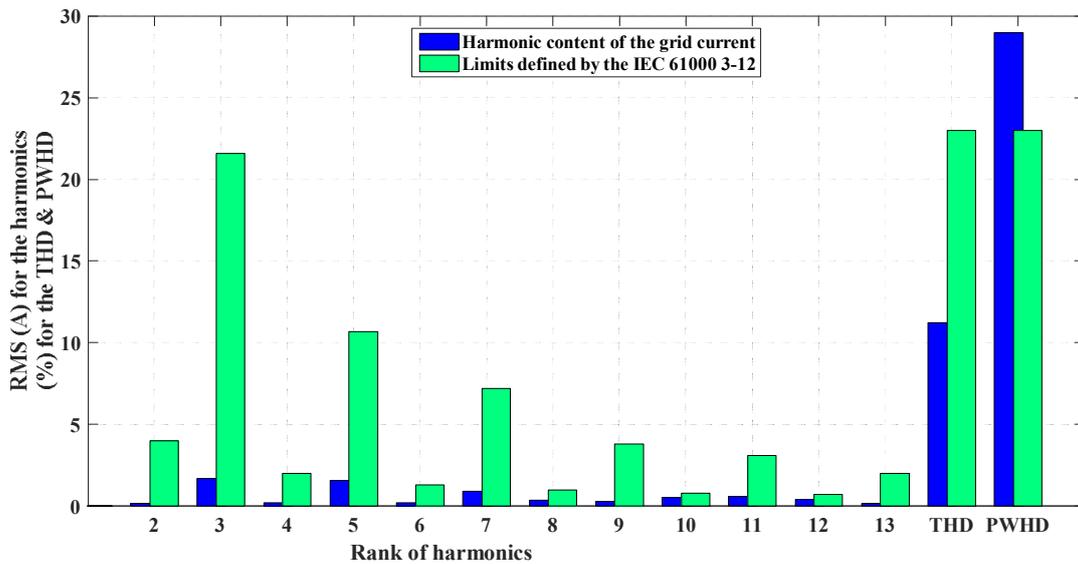


Fig.II.25. Configuration I: Verification of the compliance with the IEC 61000-3-12.

5.2.2. Configuration II: CMRM & new proposed PFC control strategy

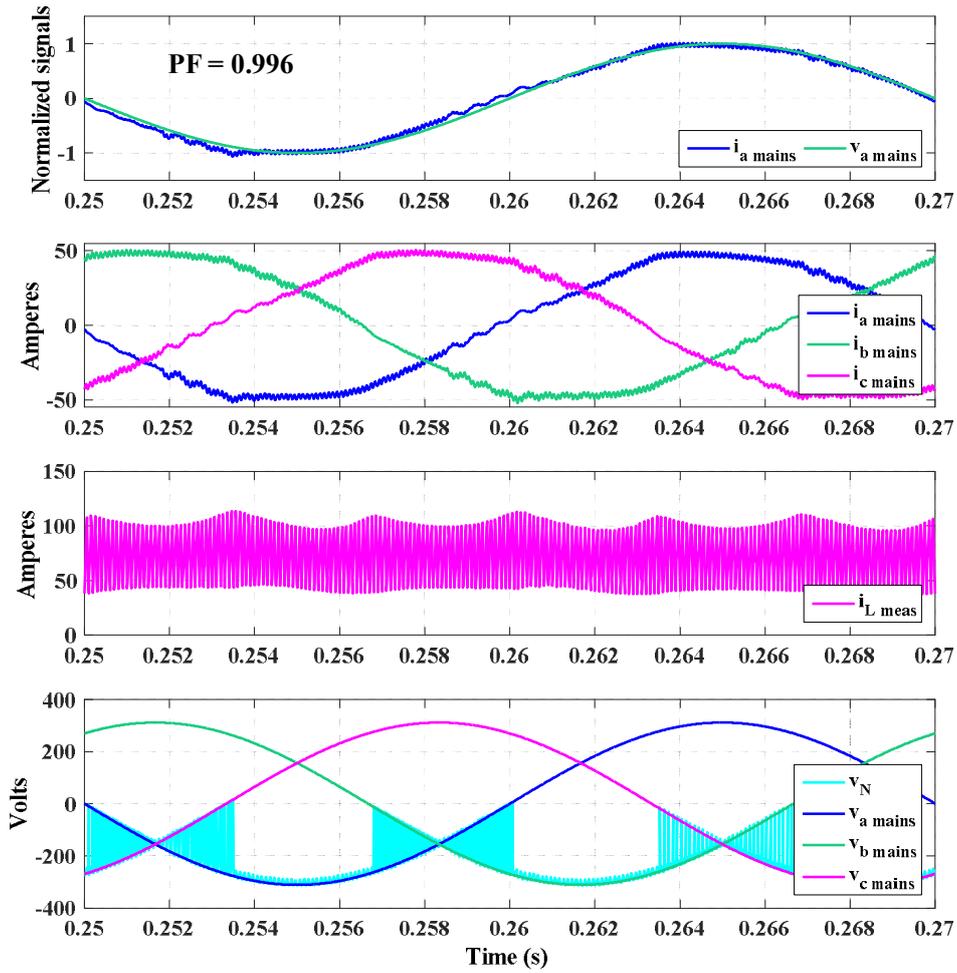


Fig.II.26. Configuration II: Waveforms of the input mains currents ($i_{a \text{ mains}}$, $i_{b \text{ mains}}$ & $i_{c \text{ mains}}$), the measured dc link inductor current ($i_{L \text{ meas}}$), the input mains voltages ($v_{a \text{ mains}}$, $v_{b \text{ mains}}$ & $v_{c \text{ mains}}$) and the voltage between the node N and the frame ground v_N .

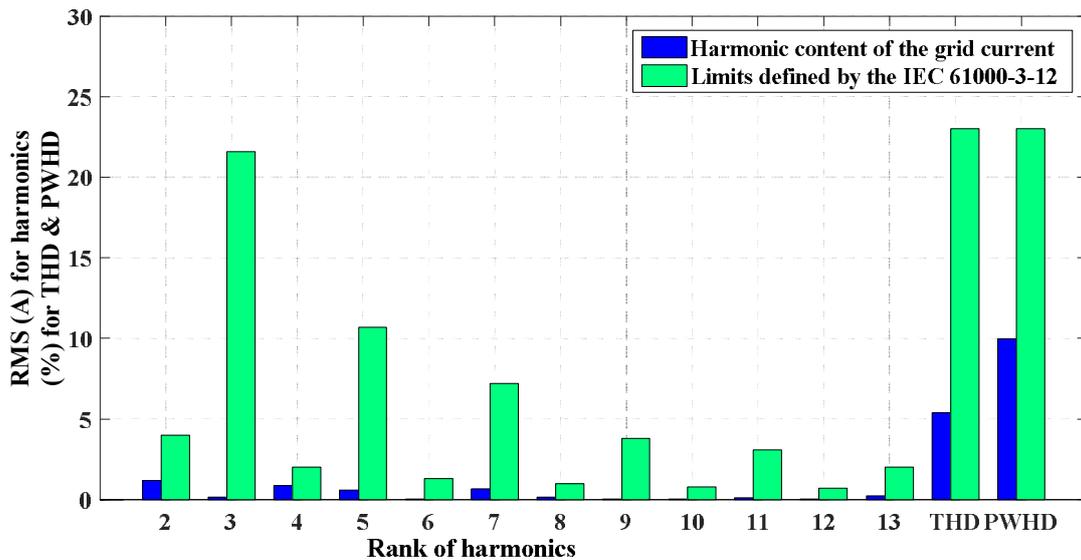


Fig.II.27. Configuration II: Verification of the compliance with the IEC 61000-3-12.

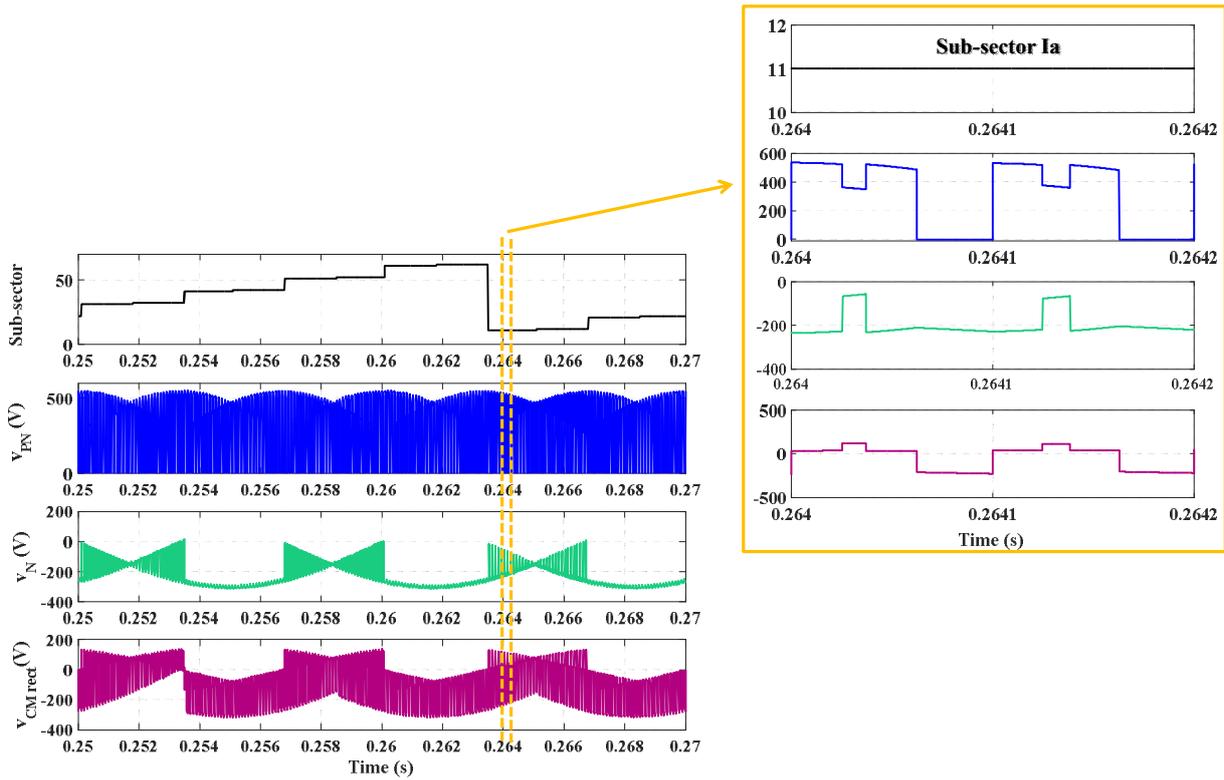


Fig.II.28. Configuration II: Simulation results over a fundamental period (0.02 sec), in sector Ia, showing the sub-sectors detected, the output voltage of the rectifier v_{PN} , the voltage between the dc- bus and the frame ground v_N and the common mode voltage generated by the rectifier $v_{CM_{rect}}$. A zoom view over two switching periods is also shown.

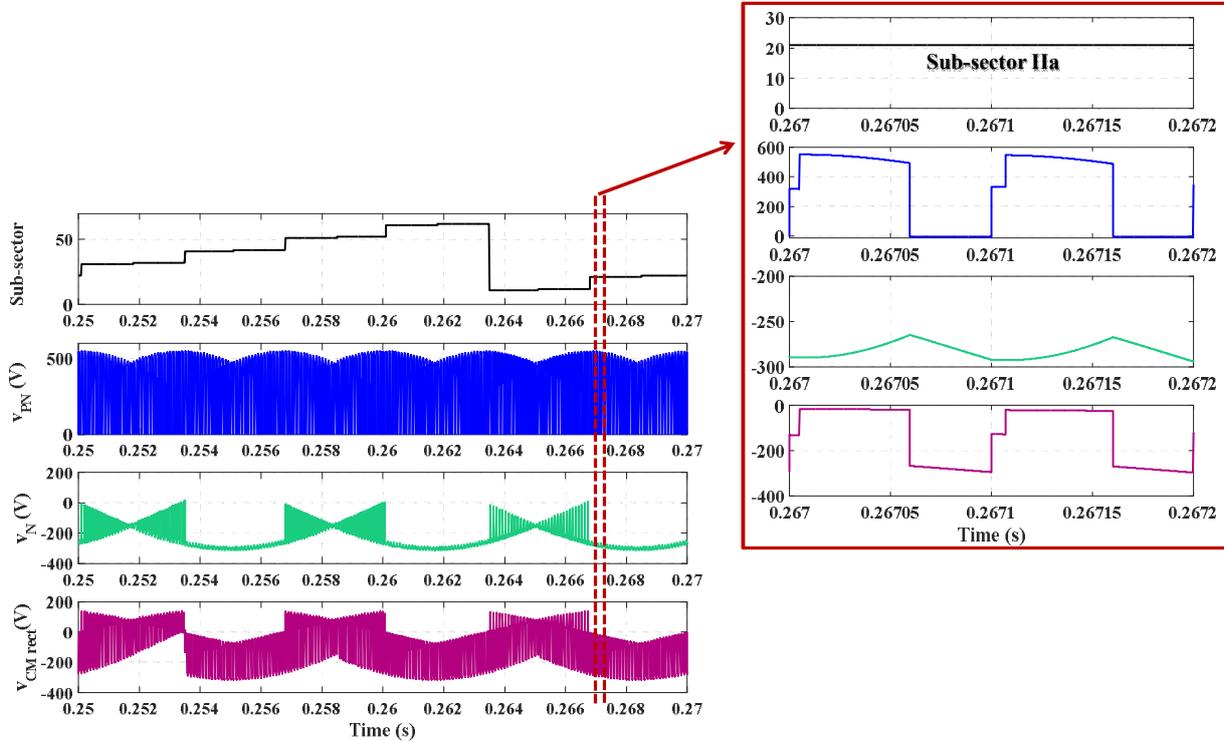


Fig.II.29. Configuration II: Simulation results over a fundamental period (0.02 sec), in sector IIa, showing the sub-sectors detected, the output voltage of the rectifier v_{PN} , the voltage between the dc- bus and the frame ground v_N and the common mode voltage generated by the rectifier $v_{CM_{rect}}$. A zoom view over two switching periods is also shown.

5.2.3. Configuration III: New MFSM & new proposed PFC control strategy

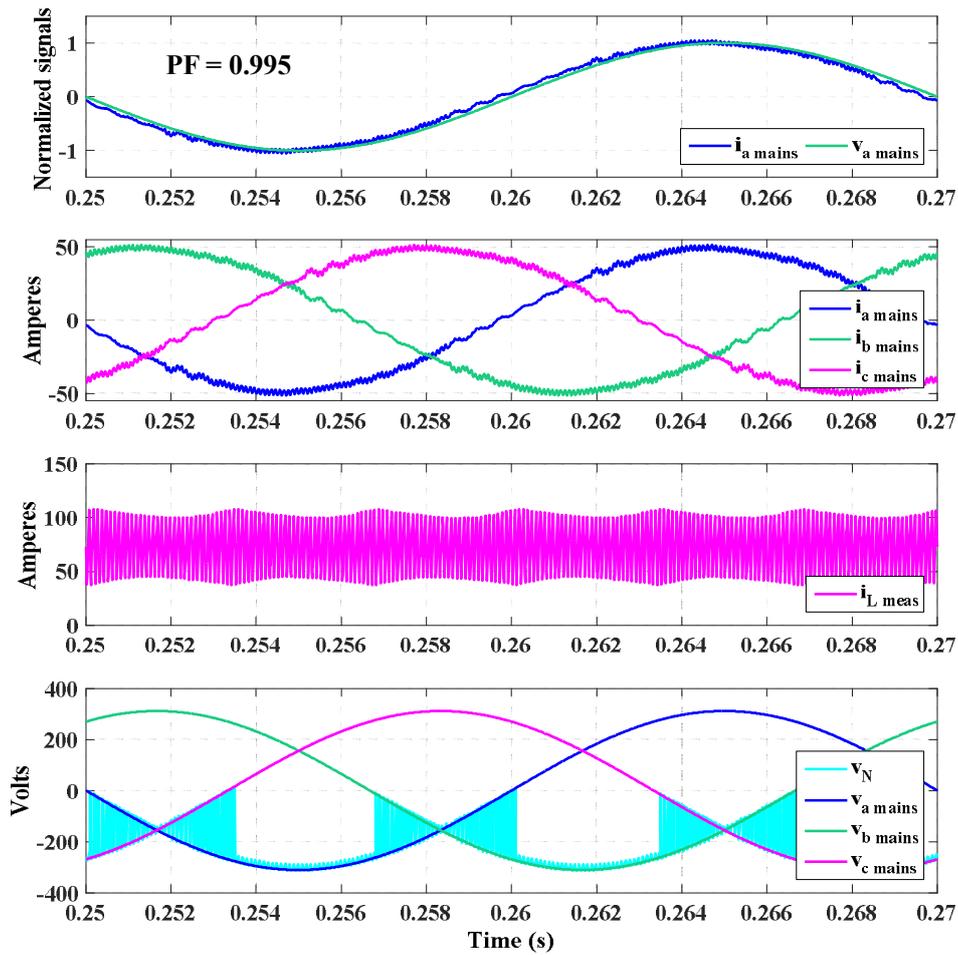


Fig.II.30. Configuration III: Waveforms of the input mains currents ($i_{a \text{ mains}}$, $i_{b \text{ mains}}$ & $i_{c \text{ mains}}$), the measured dc link inductor current ($i_{L \text{ meas}}$), the input mains voltages ($v_{a \text{ mains}}$, $v_{b \text{ mains}}$ & $v_{c \text{ mains}}$) and the voltage between the node N and the frame ground v_N .

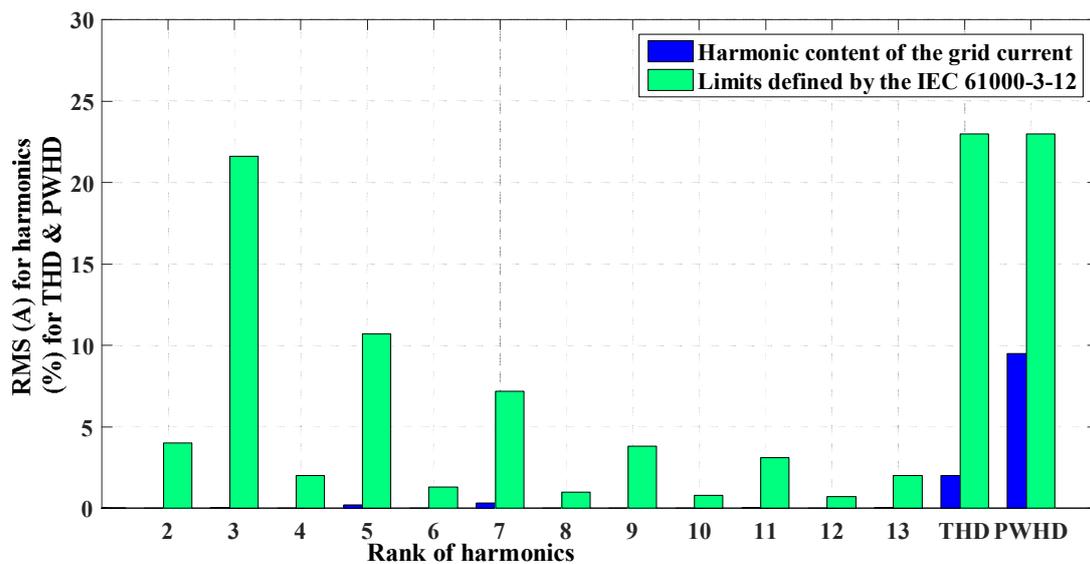


Fig.II.31. Configuration III: Verification of the compliance with the IEC 61000-3-12.

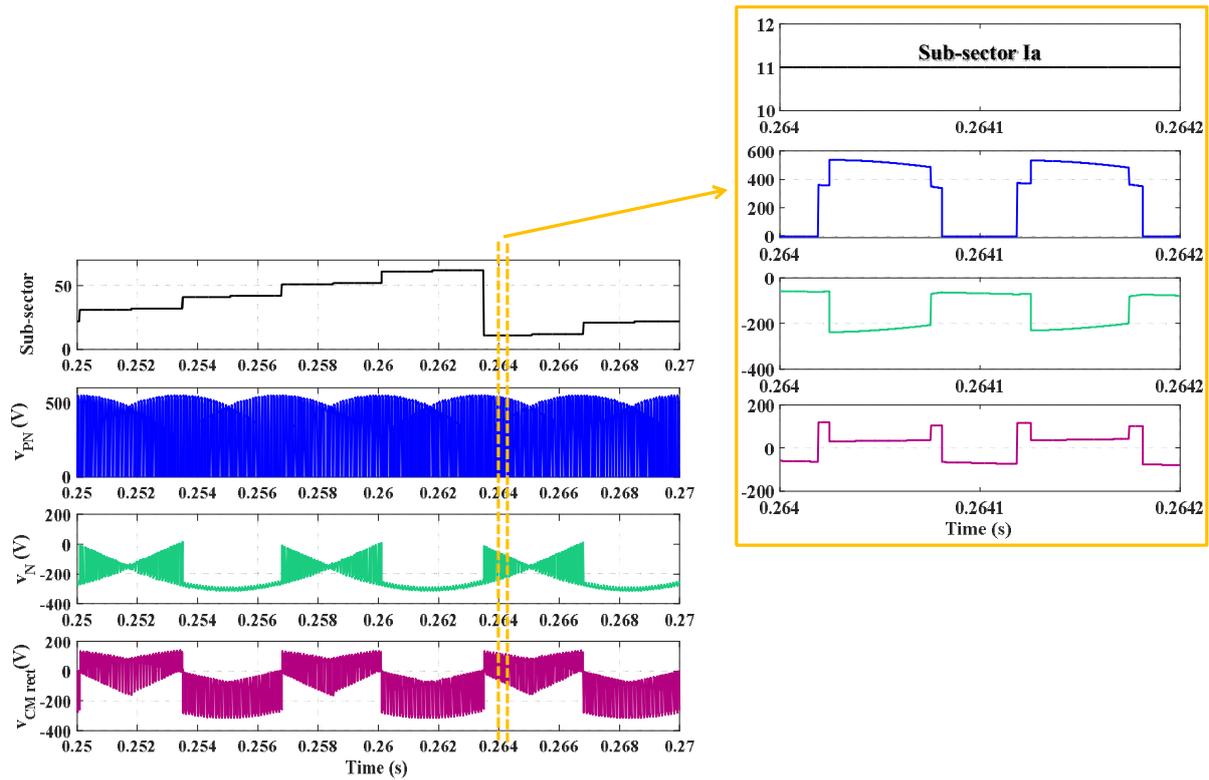


Fig.II.32. Configuration III: Simulation results over a fundamental period (0.02 sec), in sector Ia, showing the sub-sectors detected, the output voltage of the rectifier v_{PN} , the voltage between the dc- bus and the frame ground v_N and the common mode voltage generated by the rectifier $v_{CM_{rect}}$. A zoom view over two switching periods is also shown.

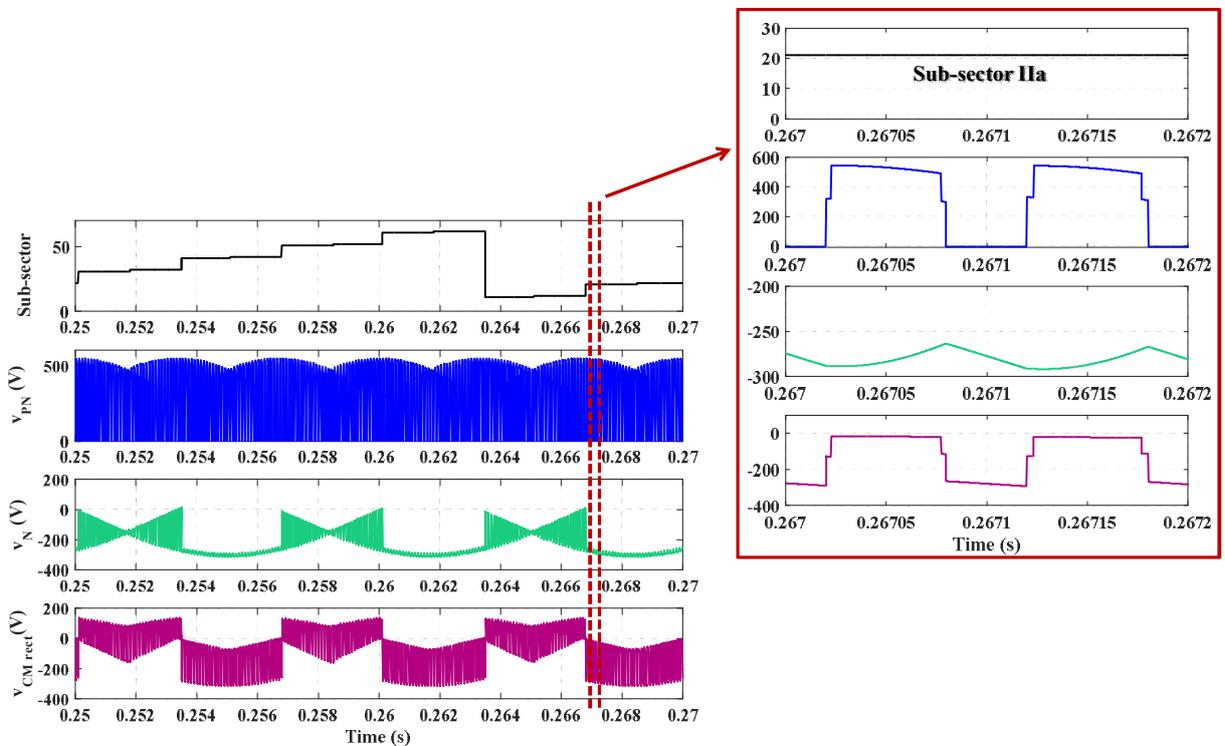


Fig.II.33. Configuration III: Simulation results over a fundamental period (0.02 sec), in sector IIa, showing the sub-sectors detected, the output voltage of the rectifier v_{PN} , the voltage between the dc- bus and the frame ground v_N and the common mode voltage generated by the rectifier $v_{CM_{rect}}$. A zoom view over two switching periods is also shown.

6. Conclusion

It is mainly the input stage of the rectifier that varies between the single-phase and the three-phase charging configurations. Therefore, a comprehensive review of the three-phase current source active rectifiers and their associated PFC control strategies is presented.

A state of the art PFC strategy applied to a structure similar to the charger being studied is used as a benchmark. The results found with this control allowed the identification of key points for improvement.

In order to be able to propose a new PFC strategy that improves the grid-side as well as the dc-side operation of the charger, a complete analysis of the charger's three-phase configuration is conducted. This allows the design of a new enhanced PFC strategy that optimizes the overall performances of the charger.

The simulation results of the state of the art PFC strategy are confronted with the simulation results of the proposed PFC control for the same current modulation strategy. By keeping the SVM strategy unchanged, we can evaluate the direct impact of the designed control over the power quality criteria (power factor and total harmonic distortion) and the dc-side current levels.

For the grid-side performances, it is verified that the proposed PFC control ensures a near unity power factor, achieves compliance with the IEC 61000-3-12 standard, reduces the individual harmonics' levels up to rank 13, reduces the total harmonic distortion rate and minimizes the partial weighted harmonic distortion rate. Moreover, for the same charging power, the new PFC reduces the average value of the dc current flowing through the filtering inductor by about 50 A. This translates into lower switching and conduction power losses for the CSAR's semi-conductors as well as the possibility to increase the value of the additional inductance (L_b) for the same inductor size. This can take part of future investigations and would allow the minimization of the dc current ripple. Furthermore, the new PFC does not activate the Boost converter for grid levels of 230 V_{RMS} and for fast charging power levels (22 kW & 43 kW). This means that the six switches of the Boost are maintained in the turn on/off position for the entire duration of the charge. These yields overall lower switching power losses.

Once the PFC strategy is proposed and evaluated, we proceeded to the analysis of the effects of current SVM strategies on the internal performances of the charger. A quick review of the main SVM strategies applied to the six-switch CSAR is conducted; three of which are retained for thorough evaluation according to several criterion. Based on these comparisons, we were able to identify the MFSM for its ability to further reduce the switching power losses and the CMRM for its capability to minimize the fluctuations of the voltage at the dc- bus (this is a very important feature for the reduction of the conducted common mode emissions and will be discussed in Part B Chapter 2). Therefore, we proposed to modify the MFSM strategy in a way that ensures both: low switching power losses and reduced voltage fluctutaions of the dc- bus. Simulation results validate the performances of this modified strategy.

Compared with a control strategy taken from the state of the art, the proposed control enhances the overall performances of the three-phase charger.

Future work must consist in the experimental verification of the performances of the proposed PFC and current modulation strategies. Moreover, a displacement power factor correction scheme coupled to an active damping of the input filter resonance can be added to the global PFC strategy. Ultimately,

a new input filter is going to be designed. The impact that the input filter has, if any, on the control stability must be taken into account. Fig.II.34 shows the steps to be followed prior to the insertion of the input filter in the power circuit for the design of the current controller.

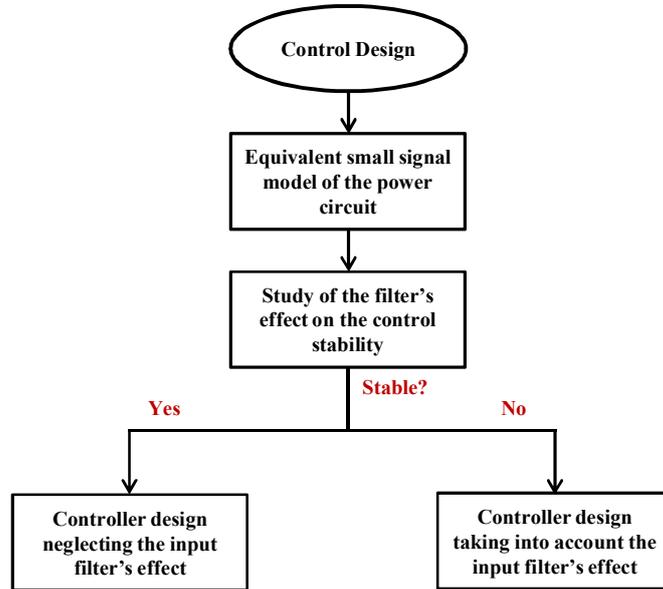


Fig.II.34. Steps required before the design of a controller.

These steps can make use of the small signal analysis of the three-phase charger in the (d, q) reference frame. The small signal model has been computed in Appendix C and presented in Fig.II.35. It can be used to deduce the system's transfer functions. By applying Middlebrook's theorem (shown in Part A Chapter 1), we can evaluate the impact that a new input filter can have on the stability of the three-phase PFC control.

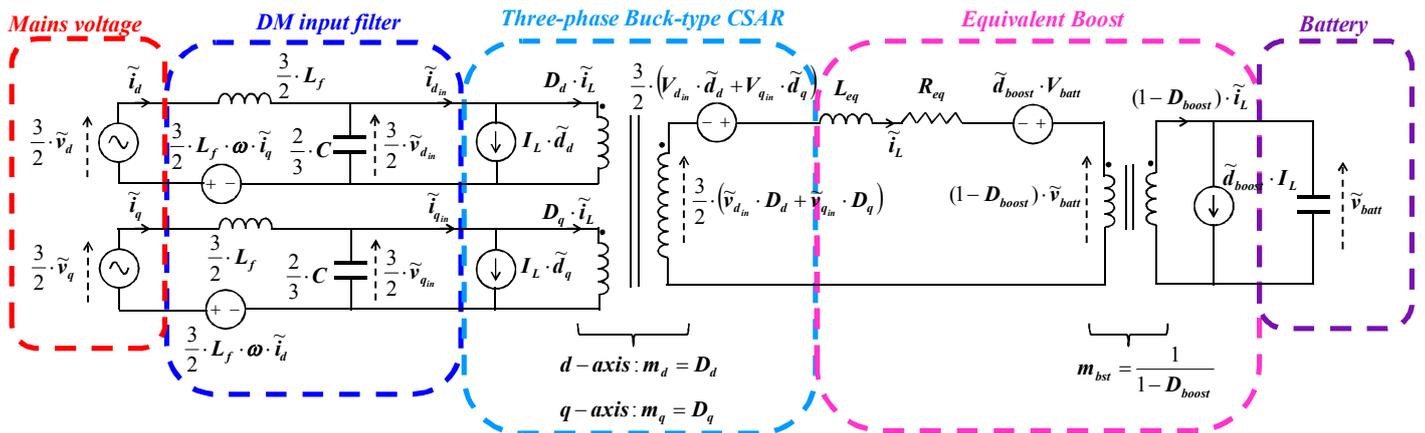


Fig.II.35. Small signal model of the three-phase charger configuration in the (d, q) reference frame.

So far, a good low frequency behavior has been established for both charging configurations and the reduction of the level of the current flowing through the power circuit has been achieved. This constitutes a good basis for the study and the reduction of the high frequency (150 kHz-30 MHz) conducted common mode emissions which ultimately allow reducing the size of the input EMI filter.

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Part B

Conducted Emissions Modeling & Mitigation

Fast switching of semi-conductors leads to high voltage and current variations that result in electromagnetic interference generated from the equipment (noise source) or tolerated by the equipment (victim). Electromagnetic emissions can be classified as radiated or conducted depending on the coupling path between the noise source and the victim. Unlike radiated emissions, the conducted electromagnetic interference is caused by the physical contact of conductors. These emissions flow through physical electrical components, for instance line to ground filtering capacitors or parasitic elements, such as stray capacitances and inductances. High current variations across stray inductances can lead to overvoltage in switching cells. On the other hand, high voltage fluctuations across stray capacitances result in common mode currents flowing through the chassis. These common mode currents can have low frequency as well as high frequency components. As a result, the currents flowing through the chassis are called leakage currents and are subject to standardized testing to ensure the safety of the users.

Common mode currents are unavoidable in power electronics systems. Design engineers are able to reduce the effect of parasitic elements through certain layout techniques; however, noise is always generated by the semi-conductors' switching. Since conducted emissions cannot be fully eliminated, passive EMI filtering along the propagation path has always been the go-to solution for power electronics designers. Nevertheless, deep knowledge about the electrical behavior of the system and its interaction with its surroundings is required in order to design an optimal EMI filter (in terms of reducing the volume, the cost and the attenuation levels required).

Since this study is conducted for the automotive industry, cost, size, and security requirements related to these types of chargers constitute major design constraints. On one hand, if the charger is integrated to the traction power train, cost and size are mainly defined by the volume of the input EMI filter. Therefore, the first main objective of this study is to produce a conducted electromagnetic interference (EMI) model which requires low computational time and resources in order to be used in optimization algorithms destined for designing a reduced volume input filter. Thus, the range of validity sufficient for this study can be limited to a few MHz for switching frequencies ranging from 10 kHz to 100 kHz. On the other hand, ensuring the user's security as well as reducing the size of the filter is achieved by reducing the leakage current emission levels. The latter is achieved by integrating conducted EMI mitigation techniques in the design process. The evaluation of the impact of these techniques requires an EMI behavioral model integrating the internal noise sources and propagation paths for common mode (CM) and differential mode (DM) emissions.

For these reasons, the first Chapter of this Part presents a conducted EMI model for power electronics converters that combines both CM and DM emissions. This model allows the estimation of conducted emissions solely based on the semi-conductors' switching functions. It offers the possibility to chain models in order to emulate the conducted EMI behavior of a global power electronics conversion system. The presented model is validated and applied to the non-isolated on-board charger for electric vehicles. Both single-phase and three-phase charging configurations are considered. In order to reduce the charger's emission levels, the second Chapter studies different conducted electromagnetic interference mitigation schemes based on structural and behavioral symmetry. These solutions are assessed using the proposed modeling approach. Once the EMI reduction techniques adopted and the control laws fixed, an input EMI filter is designed. An overview of the contributions detailed in Part B is given in Fig. 1.

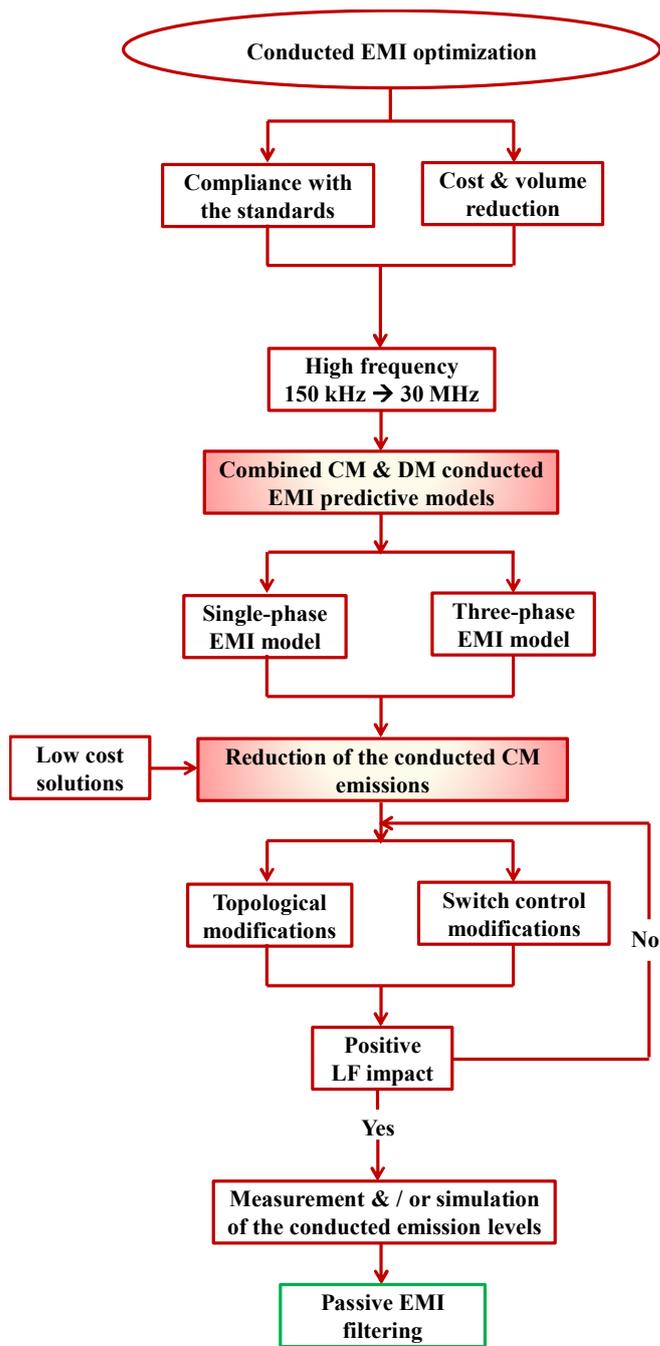


Fig.1. Overview of the high frequency conducted EMI emissions study.

Chapter 1

Combined CM & DM Conducted EMI Modeling

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This Chapter presents a conducted EMI modeling approach applicable to all power electronics converters, including active front-end topologies consisting of cascaded converters. The main purpose is being able to evaluate the emission levels generated by each converter in a given topology. Therefore, the switching cells of each converter are studied separately while being linked to the passive and parasitic elements. As a result, each element of the charger presented in Fig.I.1 is going to be modeled separately: the Boost's switching cell, the CSAR and the Boost's filtering inductor. Afterwards, the various models are combined to form the global EMI model of the structure. This approach allows the evaluation of any given structural or behavioral modification by simply replacing the modified element of the model by its updated version. Furthermore, the obtained model can be easily injected into optimization algorithms for the efficient computation of an EMI filter. The models are developed in frequency-domain and an equivalent circuit representation is given at each step of the modeling process.

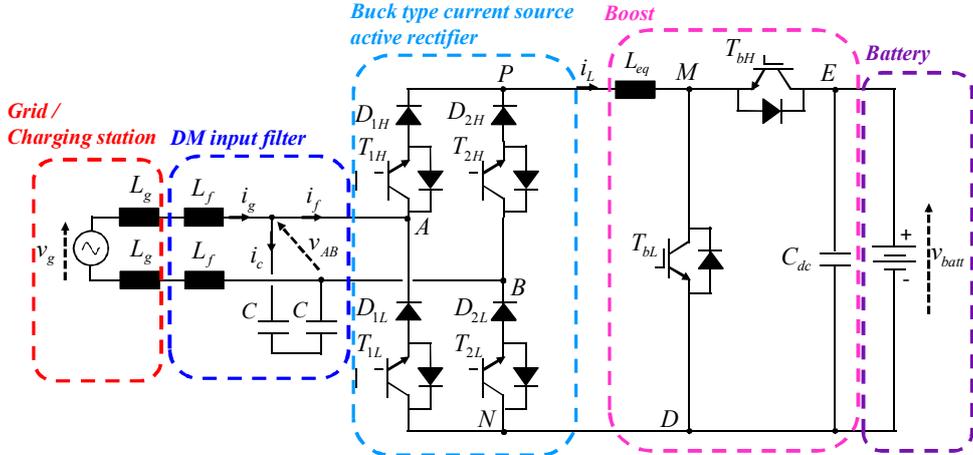


Fig.I.1. Power circuit of the galvanically non-isolated single-phase charger with a CSAR input stage, and a dc/dc Boost output stage.

1. State of the art : conducted EMI modeling techniques

This section presents a review of the conducted EMI modeling techniques found in literature. Their assessment is based on the modeling needs of this study. On one hand, the model should be able to recreate the internal conducted EMI behavior of the EV charger. This means that it needs to properly identify the noise source generators as well as the main propagation paths. This gives the model the capability to evaluate the impact that EMI reduction techniques have on the charger's conducted emissions. On the other hand, this study aims to design an optimal input EMI filter. Therefore, it requires a model that needs reduced computational times and that faithfully recreates the conducted EMI behavior of the EV charger along a frequency range sufficient for EMI filter design purposes.

Several conducted EMI modeling techniques can be found in literature and can be classified into two main categories: physics-based approaches and behavioral modeling approaches.

1.1. Physics-based models

The study of conducted emissions by means of the physical description of the converter elements is based on circuit-type implementation using softwares such as PSpice, Simplorer, Saber, etc. as shown in [Hefner et al. 1994]. However, time-based simulation of a complete system including multiple

power electronics converters along with their switch control strategies and parasitic elements covering the propagation paths is a complex process [Zhu et al. 2001]. In fact, the proper identification of the propagation paths leads to the insertion of numerous distributed or lumped parasitic elements. The Method of Moments (MoM) and the Partial Element Equivalent Circuit (PEEC) are some of the most common methods used to extract the parasitic elements of a power electronics layout [Ardon et al. 2009]. Furthermore, since the switches constitute the noise source generators; a precise conducted EMI time domain simulation requires the accurate reproduction of the on/off commutations of the semi-conductors based on the description of their physical structures. For example, a number of models based on solving differential equations, with different degrees of complexity, exist for each semi-conductor in the SPICE (or PLECS) libraries. Therefore, with the increased number of semi-conductors in a power electronics system, the model complexity increases. In addition, in order to reduce the volume/cost of passive elements in industrial applications, the ongoing trend is to increase the switching frequency. This is rendered possible through the maturation of the wide bandgap semi-conductor technology. Silicon carbide components are being studied for near future industrial applications while gallium nitride components are subject to further research and examination. Based on all of the above, the simulation step time should be small enough (some tens of nanoseconds) to take into account high frequency behavior (for instance, resonances between passive and/or parasitic elements as well as rise and fall times of semi-conductors) but shouldn't be too small in order to avoid high computational times and saturation of available resources. Hence, physics-based simulations present the disadvantages of heavy computational times and high-risk of divergence for the software.

For the EV charger being studied, the HF behavior cannot be dissociated from the control laws developed; therefore, physics-based simulations have been carried out using LTspice and Matlab's SimElectronics library. With LTspice, convergence problems emerged especially with the increased number of physical models for the switches. With Matlab, the control law is easily taken into account; however, the computational time and convergence were not guaranteed. In fact, the solvers used in these types of software are not adequate for EMI analysis. Even if they were able to converge, the results obtained cannot be evaluated. This solution is both heavy and unreliable for use in the evaluation of EMI mitigation techniques and EMI filter optimization algorithms.

1.2. Conducted EMI behavioral models

Behavioral modeling, dedicated for conducted EMI, emerges as a way of emulating the electrical behavior of power electronics systems without having to simulate the non-linearities linked to topological modifications during switching. There are numerous types of conducted EMI models with different characteristics: some are analyzed in time-domain others in frequency-domain or even both, they can either simulate CM behavior or both CM and DM emissions, they can either be predictive models or based on measurements, they can be terminal models or cascaded models... Hence, based on the power electronics designer's needs, the adequate modeling approach can be identified. The most known models of this category are: the Black Box approach, the predictive models, the modular terminal behavioral models (MTB), the quadripolar matrices approach and the un-terminated EMI models.

1.2.1. *Black box models*

A common approach to conducted EMI modeling is based on the "black box" identification [Frantz 2015]. As the name suggests, the system studied is considered as a whole without requiring knowledge of the internal power electronics topologies, layout design and passive elements employed. All that is

required are suitable measurement protocols in order to design a model made of sources and impedances as shown in Fig.I.2. Seen from the outside terminals, the model emulates the behavior of the system under consideration and generates the same CM and DM emissions. However, the model does not identify the internal noise source generators or the propagation paths within the structure. This type of modeling is an excellent tool for analysis and allows the study of a global system; nevertheless, it is a non-predictive approach. Therefore, “black box” identification is suitable for the design of an EMI filter after the prototype is built. However, it cannot take part of an EMI oriented design process and does not allow the study of topological modifications for conducted EMI reduction.

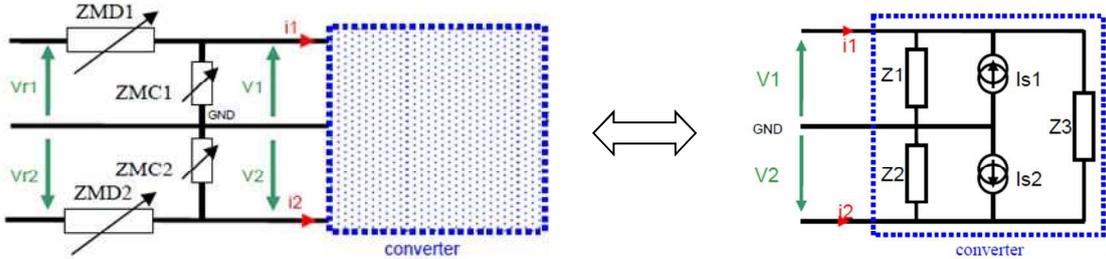


Fig.I.2. Black Box model of a dc/dc or a single-phase ac/dc converter [Foissac et al. 2009].

1.2.2. Predictive models

One of the most common conducted EMI models of a switching cell is studied by [Costa et al. 1999] and shown in Fig.I.3(a). It proposes a voltage source as a CM noise generator and a current source as a DM noise generator. The propagation paths are modeled by a network of distributed impedances. In the context of our study, this model can be easily applied to simple structures having a reduced number of switching cells; however, it becomes less obvious for converters having more complex electrical behavior.

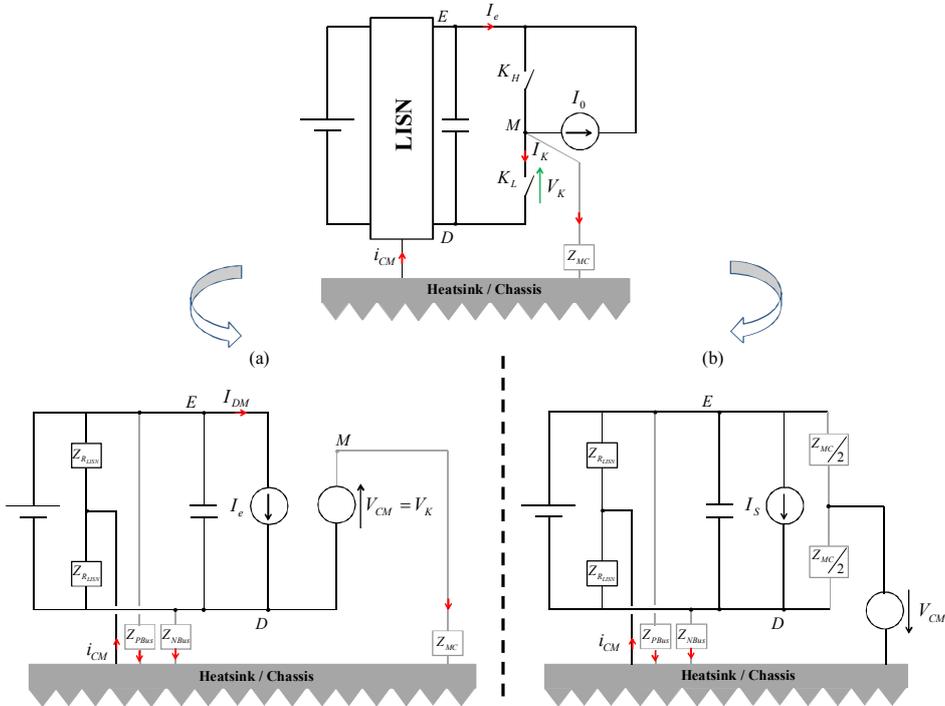


Fig.I.3. Conducted EMI model of a switching phase-leg by (a) [Costa et al. 1999], (b) [Labrousse 2010].

In [Labrousse 2010], a more complex system has been studied. A modeling approach based on the balancing of the CM impedances along the propagation path is proposed (Fig.I.3 (b)). This model only works for switching cells that share the same DC bus such as an EV's traction powertrain, where the inverter and dc/dc chopper field excitation for a wound rotor synchronous machine are both connected to the on-board high-voltage battery. Nonetheless, it is not conceptualized for cascading converters or for modeling the DM emissions generated at each conversion stage.

1.2.3. Modular terminal behavioral models

The same analysis goes to Modular Terminal Behavioral models (MTB). As its name suggests, this modeling approach terminates after a conversion stage and does not allow the cascading of multiple converter models. This model proposed by [Liu 2005] relies on the frequency domain modeling of a switching cell. As can be seen in Fig.I.4, both switches are synthesized by two Norton equivalent circuits where the current source represents the current flowing through the switch and the parallel impedance takes into account the parasitic elements intrinsic to the switch (casing stray inductance, junction capacitance...). The input and the load connected to the switching cell are represented by a single matrix of impedances. Since the model is dependent on the operating point, measurements are inevitable. This model allows the study of CM and DM emissions but it lacks the ability to model cascaded converters.

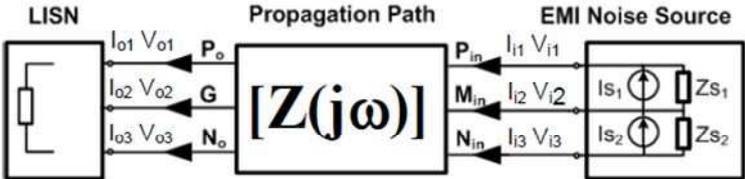


Fig.I.4. Equivalent MTB noise emission model of a switching phase-leg module [Liu et al. 2006].

1.2.4. Quadripolar matrices approach

A method that allows the cascading of models is presented by [Jettanasen 2009]. The CM behavior of a circuit is modeled by a chain of two-port networks, corresponding to each component of the system, and associated in cascade (Fig.I.5). This model is available upon measurement of the CM impedance of each element and the CM voltage generated by the converter. This approach enables the designer to evaluate the CM current at every node of the system; therefore, it can be used to optimize EMI filters or to study EMI reduction techniques. Quadripolar modeling offers the solution to cascading converters; however, it only models CM emissions.

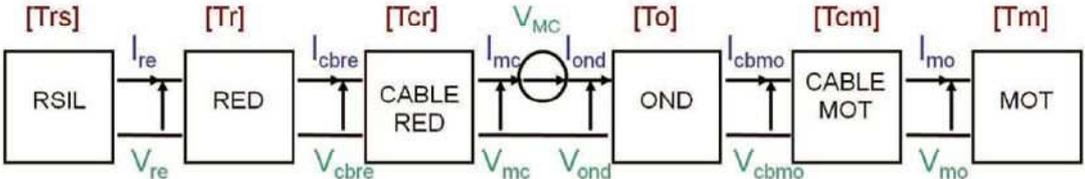


Fig.I.5. Equivalent quadripolar CM noise emission model of a motor-drive [Jettanasen 2009].

1.2.5. Un-terminated EMI behavioral model

A new modeling technique that also allows cascading of converters is presented by [Bishnoi 2013]. It is labeled as an un-terminated EMI model. Bishnoi critiques the previously mentioned terminal EMI models described as operating-point dependant models. They work well for predicting the input side EMI behavior of the converter including any change in the impedance of the input side network; however, any change at the output side would require re-extraction of the behavioral model. Thus, a new model is proposed as a combination of the quadripolar and the MTB models. It is based on two Thevenin noise sources modeled at the input and output terminals of a converter including an impedance matrix to represent the propagation paths (Fig.I.6). However, the model's parameters extraction is time consuming and dependant on measurement protocols.

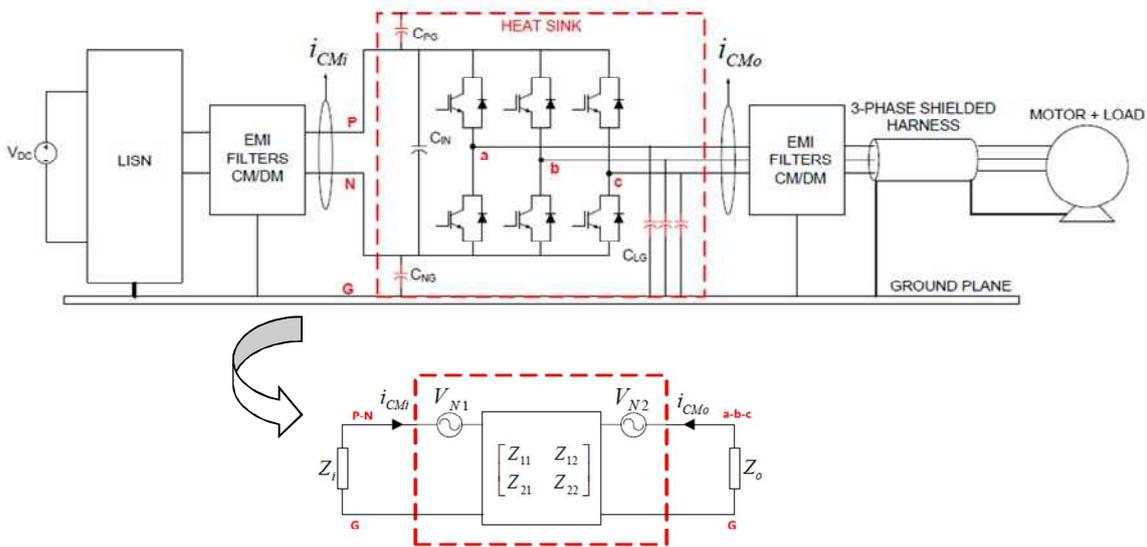


Fig.I.6. Equivalent two-port un-terminated model of a motor-drive [Bishnoi 2013].

To resume, Table I. 1 presents a comparison of the modeling techniques seen based on the criteria that interests this study.

Table I. 1. COMPARISON OF THE CONDUCTED EMI MODELS

		Modeling characteristics				Simulation characteristics	
		Conducted EMI prediction	Chaining of models	Internal noise source identification	DM emissions modeling	Time	Convergence
<i>a. Physics-based models</i>		+	+	+	+	-	-
Behavioral models	<i>Black Box</i>	-	-	-	+	+	+
	<i>Predictive</i>	+	-	+	+	+	+
	<i>MTB</i>	-*	-	+	+	+	+
	<i>Quadripolar</i>	-*	+	+	-	+	+
	<i>Un-terminated</i>	-*	+	-	-	+	+

* These approaches are non-predictive in the sense that measurements are needed in the modeling process.

1.2.6. *Proposed model*

In the scope of this work, conducted EMI modeling is used to evaluate the impact that a topological or control modification has on the reduction (or increase) of the CM emissions as well as the effect it has, if any, on the DM currents. The secondary aim of this study is to use the derived model in the design and sizing of an optimal input EMI filter; even though precision in prediction is not fully required for such a task. The model presented in this study can be considered as a combination of the quadripolar and the MTB models. In fact, this modeling approach presents the cascading capability of the quadripolar approach and the ability to emulate both CM and DM conducted emissions as does the MTB technique. It is a predictive approach based on the prior knowledge of the switch control law of the converter(s). Furthermore, it can be used either for time-domain or frequency-domain analysis.

2. State of the art: Analysis regarding the model's precision in prediction

The precision of a model is evaluated with regards to the frequency range for which the model validity is verified. The precision level depends on:

- A good identification of the propagation paths
- A faithful reconstruction of the noise source generators (i.e. the controlled sources)

A higher degree of precision can be achieved by adopting either one of the following methodologies.

2.1. First methodology to increase the model's precision

2.1.1. *Description*

On one hand, one could chose to include, in the admittance matrices used to model the propagation paths, the parasitic elements inherent to the semi-conductors, the commutation loop's stray inductances in addition to the stray impedances formed with the heatsink/chassis. The extraction of these parameters can be either achieved by analytical computation, or by specific measurement protocols carried on the experimental test bench or even by numerical calculations using softwares such as Maxwell, Ansys, Saber and Pspice to implement parameter extraction methods for instance MoM and PEEC [Roudet et al. May 2004]-[Roudet et al. Aug. 2004]- [Costa 2010]. In this case, it is sufficient for the controlled sources to have idealized trapezoidal behavior since the high frequency switching oscillations are recreated outside of the sources.

2.1.2. *Effect of rise / fall times on spectral content*

The major limitation of the trapezoidal controlled source approach is to accurately obtain the turn-on and turn-off times of the switches. The device manufacturer usually provides the rise and fall times under certain test conditions. For example, the datasheet provided by Cree for their C2M0080120D SiC MOSFET, used for the experimental testing in this Chapter, gives the rise time (20 ns) and the fall time (19 ns) of these devices when tested under an 800V DC bus and a 20A line current with a 40Ω load resistor (Fig.I.7). These testing conditions are rarely the same as the real operating conditions of the applications for which the MOSFETs are used; especially for PFC converters that function under varying operating points. As a result, trapezoidal switching waveforms assumed for the controlled sources are oversimplified. The effect of the rise and fall times intervenes at high frequencies (16 MHz for $t_{\text{rise}}=20\text{ns}$) in the conducted emissions spectrum and defines the start of a -40 dB/decade attenuation [Clayton 2006].

2.2. Second methodology to increase the model's precision

On the other hand, since the switching oscillations come from resonances that exist mainly between the commutation loop's total stray inductance and the inherent parasitic capacitances of the semi-conductors, one can exclude them from the propagation paths and rather include them in the modeling of the noise source generators. In this case, the admittance matrices only contain the parasitic couplings between the power circuits' nodes and the heatsink or chassis and a more realistic on/off switching behavior of the controlled sources is required. The latter should incorporate the identified high frequency oscillations due to the resonances.

$t_{d(on)}$	Turn-On Delay Time		11	ns	$V_{DD} = 800 \text{ V}, V_{GS} = -5/20 \text{ V}$ $I_D = 20 \text{ A}, R_{G(ext)} = 2.5 \Omega,$ $R_g = 40 \Omega$, Timing relative to V_{DS} Per IEC60747-8-4 pg 83	Fig. 27
t_r	Rise Time		20			
$t_{d(off)}$	Turn-Off Delay Time		23			
t_f	Fall Time		19			

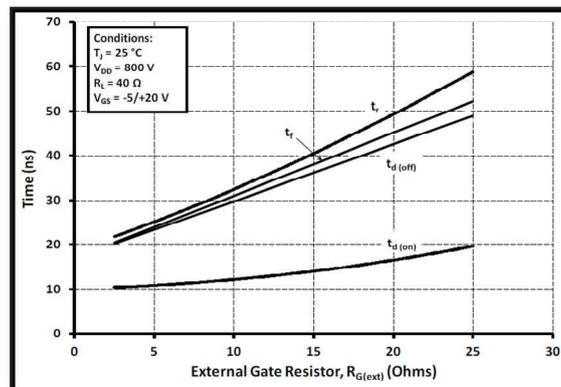


Figure 27. Switching Times vs. $R_{G(ext)}$

Fig.I.7. Extract from the Cree MOSFET C2M0080120D datasheet [Cree 2015].

This is achievable either through measurements or by extracting the signals from a complex and thorough time-domain simulation. The latter is extremely time-consuming; therefore, the author of [Labrousse et al. 2011] models the controlled generators in frequency-domain by introducing two transfer functions that incorporate the parasitic elements of the switching cell; whether linked to the semi-conductors or due to their interaction with their environment (Fig.I.8).

Thus, a higher degree of precision in prediction is achieved with reduced computational times by including the oscillations in the modeling of the turn on/off commutations. However, the method is complex and still in its development phase.

The work presented in this study progressed from the use of IGBTs switching at 10 kHz to the use of silicon carbide MOSFETs with higher switching frequencies (70 kHz). In the scope of this study, the frequency range required for an EMI filter design is around few MHz. Therefore, based on the previous analysis, it is necessary to justify the use of idealized trapeze waveforms to model the controlled sources.

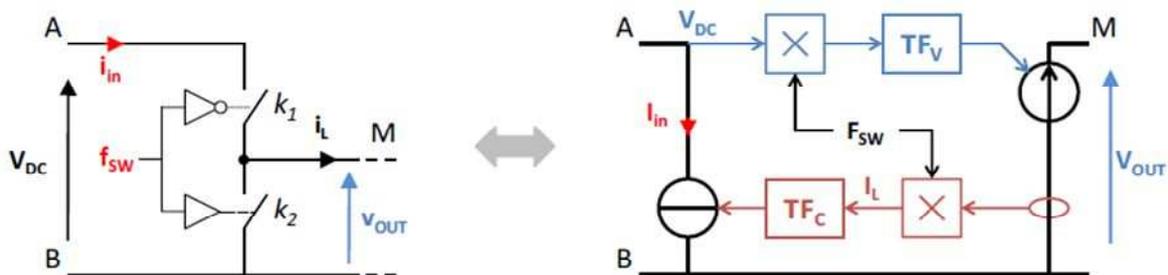


Fig.I.8. Switching cell modeling by transfer function [Labrousse et al. 2011].

3. Proposed modeling approach

3.1. Modeling of the traction inverter used as a dc/dc Boost converter

Comprehensive analysis of a power electronics converter is highly dependent on the control law implemented. The integrated charger being studied uses the traction inverter as a voltage step-up dc/dc converter. The three legs are not interleaved but rather synchronously controlled to form an equivalent one-legged Boost converter. Therefore, the EMI model of the equivalent Boost is presented. A model developed for the three-legged configuration of the dc/dc Boost converter, which can be equally used for a three-phase two-level inverter, is given in Appendix D. In case the three legs are identically controlled, this model can be used to study the effect of numerical implementation delays on the CM emissions of the charger. In other case, the model of Appendix D can be used to study the effects of interleaving the Boost legs on the CM and DM emissions.

The equivalent Boost switching cell is presented in Fig.I.9. The input line currents ($i_{M_{in}}, i_{D_{in}}$) contain both CM and DM components. However, this modeling approach does not assume topological symmetry as in previous literature. Therefore, no prior assumption is made regarding the rate of distribution of the CM current on the input lines. The idea is to be able to take into account the structural asymmetries of a converter while studying the conducted EMI behavior. The same applies to the currents of the output buses ($i_E, i_{D_{out}}$). Moreover, the connection between the midpoint of the switching cell M and the output (in grey) represents a parasitic link. In that sense, the corresponding current $i_{M_{out}}$ depicts only CM behavior through parasitic impedances.

3.1.1. Common mode behavioral model of the Boost

In this sub-section, only the conducted CM behavior is studied. According to Fig.I.9, the following equations can be written:

$$\begin{bmatrix} I_E \\ I_{M_{out}} \\ I_{D_{out}} \end{bmatrix} = [Y_{load}] \cdot \begin{bmatrix} V_E \\ V_M \\ V_D \end{bmatrix}, \text{ with } [Y_{load}] = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \quad \text{eq. (I. 1)}$$

Furthermore,

$$I_{CM_{bst}} = (I_E + I_{M_{out}} + I_{D_{out}}) \Big|_{DM=0} \quad \text{eq. (I. 2)}$$

The expression of the common mode current generated by the Boost's switching cell and flowing through the parasitic elements, whether inherent to the semi-conductors and the layout or formed with its surroundings (such as the heatsink), is deduced by combining eq. (I. 1) and eq. (I. 2).

$$I_{CM_{bst}} = Y_E \cdot V_E + Y_M \cdot V_M + Y_D \cdot V_D \quad \text{where,}$$

$$Y_E = \sum_{i=1}^3 Y_{i1}, \quad Y_M = \sum_{i=1}^3 Y_{i2}, \quad \text{and} \quad Y_D = \sum_{i=1}^3 Y_{i3} \quad \text{eq. (I. 3)}$$

On the other hand, V_M can be expressed as a function of V_D .

$$V_M = V_D + V_{bL} \quad \text{eq. (I. 4)}$$

Moreover, the voltages across the switches depend on the control law that is implemented. Since the switching cell is part of a Boost operation, the upper switch (T_{bH}) is maintained open while the lower switch (T_{bL}) is controlled via pulse width modulation. Hence, the upper switch's anti-parallel diode presents complementary states with regard to T_{bL} 's switching function f_{Tb} defined in eq. eq. (I. 5).

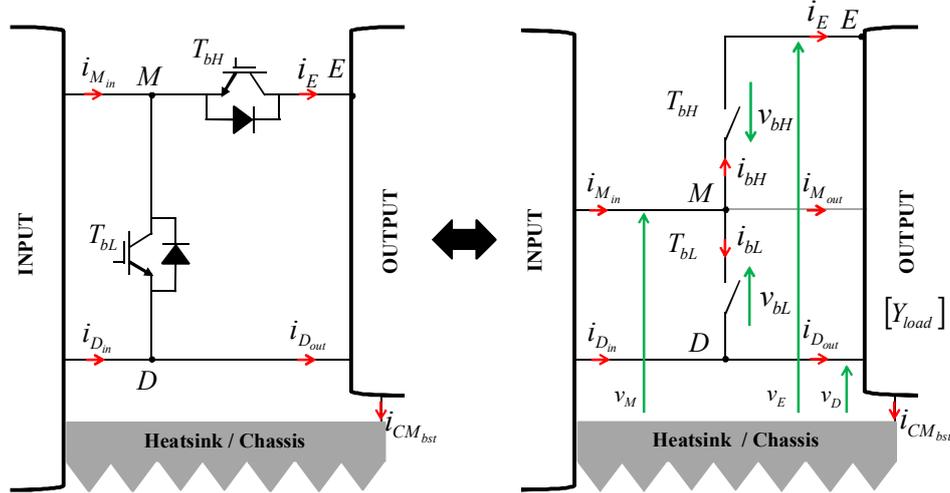


Fig.I.9. Representation of the equivalent Boost's switching cell.

$$\begin{cases} f_{Tb} = 1, & T_{bL} \text{ is ON} \\ f_{Tb} = 0, & T_{bL} \text{ is OFF} \end{cases} \quad \text{eq. (I. 5)}$$

In frequency domain analysis, one should define the Fourier transform of a constant signal as being a Dirac delta function representing a spike (or impulse) at zero frequency. For instance, the Fourier transform of the time-domain expression of the voltage across the low-side switch eq. $\varepsilon\theta$. \square I. 6) is equivalent to the frequency-domain expression eq. $\varepsilon\theta$. \square I. 7). The Dirac delta is the unit element for the convolution (the latter is equivalent to the multiplication in time-domain) as can be seen in the example of eq. $\varepsilon\theta$. \square I. 8). In the rest of this study, frequency domain variables are noted in capital letters and time-domain variables are associated to lowercase letters.

$$v_{bL}(t) = [1 - f_{Tb}(t)] \cdot [v_E(t) - v_D(t)] \quad \text{eq. (I. 6)}$$

$$V_{bL}(f) = [\delta(f) - F_{Tb}(f)] * [V_E(f) - V_D(f)] \quad \text{eq. (I. 7)}$$

$$\delta(f) * [V_E(f) - V_D(f)] = V_E(f) - V_D(f) \quad \text{eq. (I. 8)}$$

All through the modeling process, the frequency index is going to be hidden but implied. Hence, the voltage across the low-side switch can be written as follows:

$$V_{bL} = (\delta - F_{Tb}) * (V_E - V_D) \quad \text{eq. (I. 9)}$$

By combining eq. eq. (I. 4) and eq. eq. (I. 9), the expression of V_M can be deduced.

$$V_M = \frac{V_E + V_D}{2} + (\delta - 2F_{Tb}) * \frac{V_E - V_D}{2} \quad \text{eq. (I. 10)}$$

Hence, the voltage between the node M and the heatsink is a function of the output dc bus's CM voltage $((V_E + V_D)/2)$ and differential voltage $(V_E - V_D)$. The common mode current can be re-written as follows:

$$I_{CM_{bst}} = Y_E \cdot V_E + Y_D \cdot V_D + Y_M \cdot \left[\frac{V_E + V_D}{2} + (\delta - 2F_{Tb}) * \frac{V_E - V_D}{2} \right] \quad \text{eq. (I. 11)}$$

From this expression, a behavioral common mode model for the Boost's switching cell is derived and presented in Fig.I.10 (a).

3.1.2. *Differential mode behavioral model of the Boost*

In this sub-section, only the conducted DM behavior is studied. In order to establish a DM model of the Boost, the equations describing the electrical behavior of line to line variables must be established. According to Fig.I.9, the differential input voltage and the Boost's load current expressions are given in eq. eq. (I. 12) and eq. eq. (I. 13).

$$V_M - V_D = V_{bL} = (\delta - F_{Tb}) * (V_E - V_D) \quad \text{eq. (I. 12)}$$

$$I_E = \left(I_{M_{in}} - F_{Tb} * I_{M_{in}} \right)_{CM=0} \quad \text{eq. (I. 13)}$$

Based on eq. eq. (I. 10), the DM behavior of the Boost's switching cell can be modeled as shown in the circuit representation of Fig.I.10 (b).

3.1.3. *Combined CM & DM model of the Boost converter*

The CM and DM models are combined into a single CM/DM behavioral model shown in Fig.I.11. It can be verified that the modeling approach is based on the detection of the switching cells and their midpoints in a power electronics converter and the replacement of each switching cell with a controlled voltage source (for CM behavior) and a controlled current source (for DM behavior).

These controlled sources help predict the conducted emissions but are not the real noise generators of the switching cell. For example, the controlled current source does not generate the DM current i_E ; however, Kirchhoff's current law applied to the midpoint of the switching cell M leads to the deduction of the output DM current. Furthermore, the controlled voltage source is not equivalent to the CM voltage; nevertheless, Kirchhoff's voltage law helps deducing the CM voltage V_M at the midpoint of the switching cell.

In addition, a network of lumped stray impedances / admittances models the propagation paths and takes into account any fluctuation of the input and output DC buses. In fact, the load admittance matrix presented in eq. εθ. (I. 1) shows that the lumped admittances Y_M , Y_E and Y_D model all the stray elements, whether inherent to the semi-conductor or linked to its environment, present between the three nodes (M , E and D) or between these nodes and the heatsink / chassis.

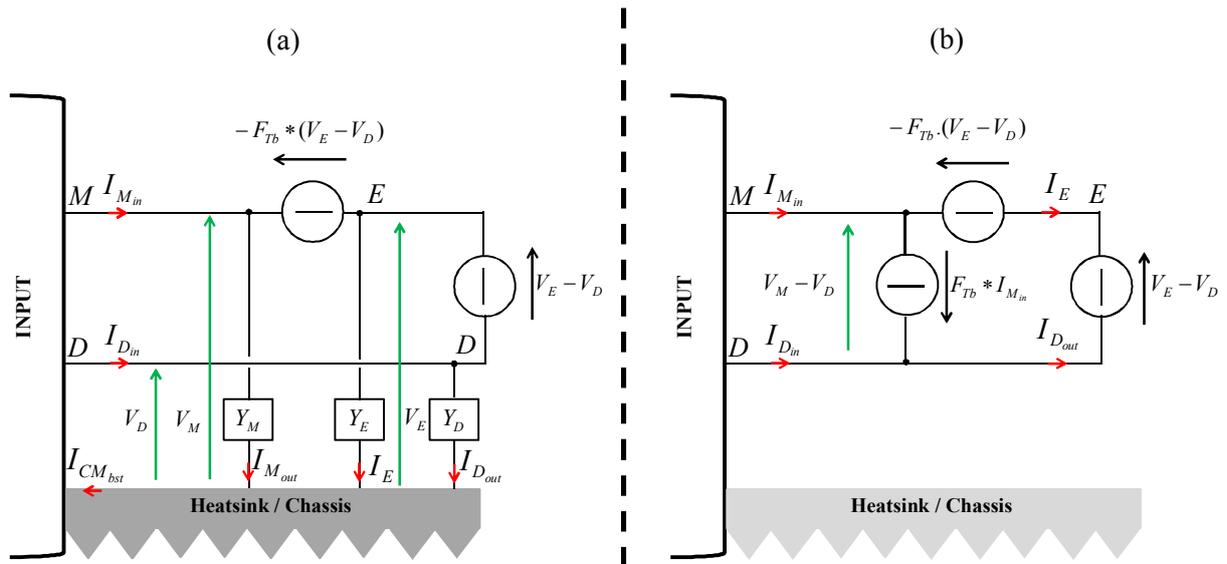


Fig.I.10. Proposed CM/DM models of a Boost switching cell. (a) CM, (b) DM.

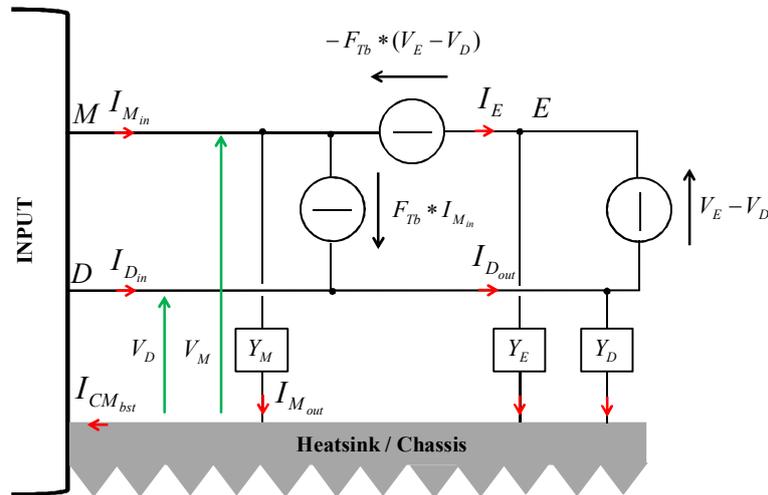


Fig.I.11. Combined CM/DM model of a Boost switching cell.

3.1.4. Simulation results: Model Validation

In order to validate the developed behavioral modeling technique, a circuit-type simulation of a typical Boost converter is carried out. The Boost is controlled in open-loop using a 50% duty cycle and a 10 kHz switching frequency. It is operated in steady-state continuous conduction mode. Furthermore, the IGBT and the diode are modeled using idealized components; thus, rise and fall times are both equal to a single step-time (10 ns).

The evaluation of the modeling approach is achieved by comparing the CM emissions and DM currents resulting from the circuit-type simulation with their counterparts from the model of Fig.I.11. The latter's controlled sources are modeled using trapeze waveforms with rise and fall times both equal to one sampling period (10 ns). This simplification allows a fair comparison under the same operating conditions.

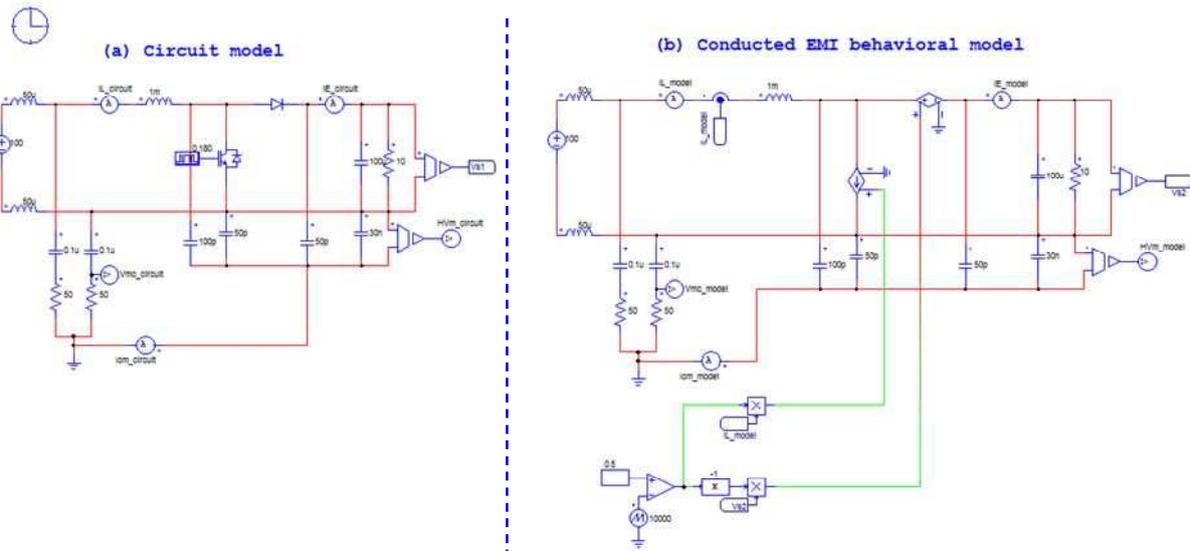


Fig.I.12. Simulation of conducted EMI emissions of a Boost converter using PSIM. (a) Circuit-type simulation, (b) Equivalent conducted EMI behavioral model.

Time-domain simulation results (Fig.I.13) show the current in the Boost's inductor i_L , the DM current at the output of the Boost i_E , the CM current flowing through the single-phase LISN network i_{CM} and the voltage fluctuation of the load's negative DC rail ($HVM = v_D$) for both, the circuit-model (in blue) and the behavioral model (in green).

Furthermore, the Fast Fourier Transform applied to the obtained CM currents is shown in Fig.I.14. These results validate the model's capability to emulate the internal conducted EMI behavior of a Boost converter. The adequacy between the circuit simulation results and the model simulation results validate the modeling approach.

❖ **Discontinuous current conduction mode**

It should be noted that the model is designed for continuous conduction mode of the current in the inductor. In fact, under discontinuous conduction mode the system dynamics are altered and the mathematical equations on which the model is based become invalid.

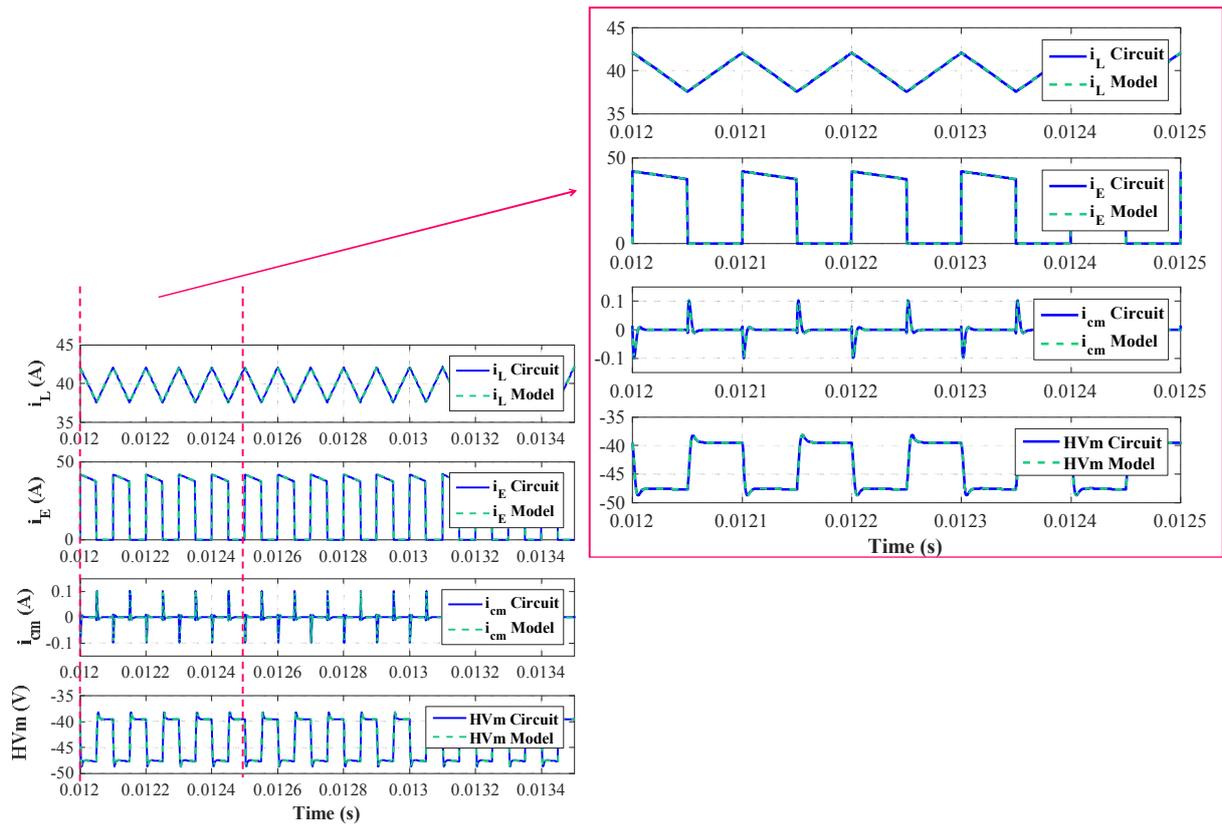


Fig.I.13. Time-domain simulation results of the conducted EMI emissions of a Boost converter using circuit-type simulation (blue) vs. the conducted EMI behavioral model (green).

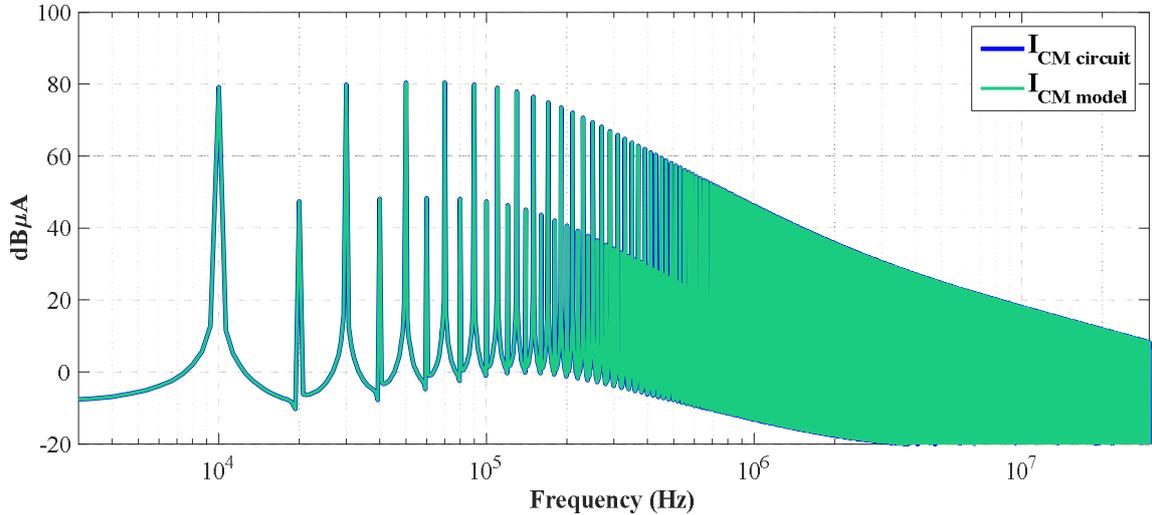


Fig.I.14. Frequency-domain analysis of the CM conducted EMI emissions of a Boost converter using circuit-type simulation (blue) vs. the conducted EMI behavioral model (green).

3.2. Modeling of the single-phase CSAR

As previously mentioned, the input stage of the charger is an ac/dc converter known as a current source active rectifier with voltage step-down capability. It consists of four insulated-gate bipolar transistors (IGBTs) T_{1H} , T_{2H} , T_{1L} and T_{2L} placed in series with four diodes D_{1H} , D_{2H} , D_{1L} and D_{2L} in order to ensure voltage reverse blocking capabilities. Since the EMI modeling approach is highly dependent on the switch control law, it is necessary to explain the switch control strategy. With the absence of a freewheeling diode between the nodes P and N, the freewheeling state of the Boost inductor current needs to be ensured by the rectifier's legs.

Furthermore, there exists a number of switch control strategies for the rectifier. This sub-section handles the case where the lower switches (T_{1L} and T_{2L}) are always turned on in order to reduce the switching losses and the fluctuations of the DC bus' negative side. The importance of minimizing the voltage fluctuation of the negative DC rail is explained in Section 3.3. Therefore, using the functions defined in eq. eq. (I. 14) and eq. eq. (I. 15); the switching states of the rectifier's IGBTs are given in Table I. 2.

$$\begin{cases} f_{TiH} = 1, & TiH \text{ is ON} \\ f_{TiH} = 0, & TiH \text{ is OFF} \end{cases}, \text{ with } i = 1, 2 \quad \text{eq. (I. 14)}$$

$$\begin{cases} f_D = 1, & v_{AB} \geq 0 \\ f_D = 0, & v_{AB} < 0 \end{cases} \quad \text{eq. (I. 15)}$$

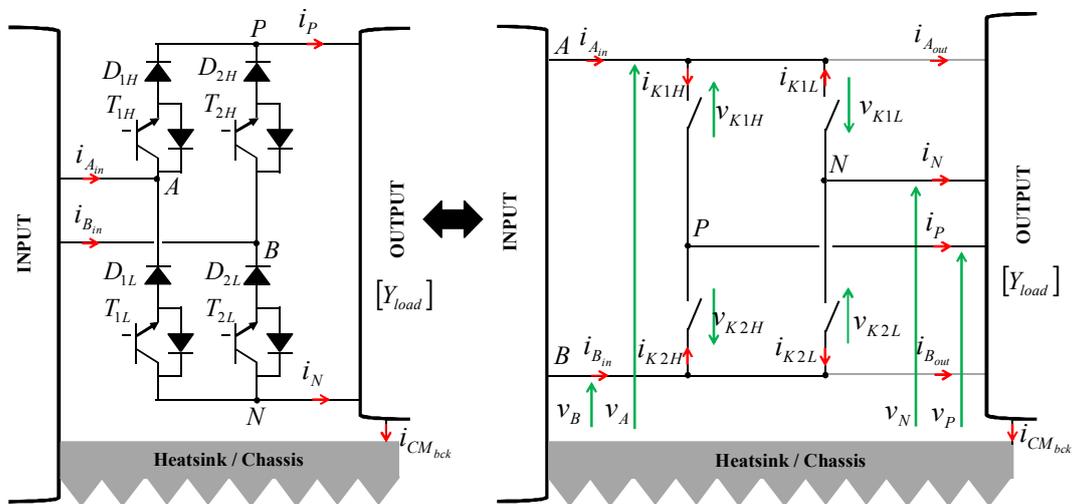


Fig.I.15. Representation of the CSAR's switching cells.

3.2.1. Common mode behavioral model of the CSAR

By following the same modeling approach, the rectifier's switching cells are represented in Fig.I.15. In order to simplify the analysis, each couple formed by an IGBT (T_{1H} , T_{2H} , T_{1L} and T_{2L}) with its series diode (D_{1H} , D_{2H} , D_{1L} and D_{2L}) is replaced by a single switch referred to, respectively, as K_{1H} , K_{2H} , K_{1L} and K_{2L} . The latter's switching functions are a combination of the IGBTs' switching functions and the input voltage's sign detection eq. eq. (I. 15). The high-side switches (K_{1H} & K_{2H}) form a switching cell

having the node P as midpoint and the low-side switches (K_{1L} & K_{2L}) form another switching cell having the node N as midpoint.

Table I. 2. CSAR'S SWITCHING STATES

Grid side input voltage v_{AB}	Switch			
	T_{1H}	T_{2H}	T_{1L}	T_{2L}
Positive half cycle $f_D = 1$	f_{T1H}	$1-f_{T1H}$	ON	ON
Negative half cycle $f_D = 0$	$1-f_{T2H}$	f_{T2H}	ON	ON

Using the definitions of Fig.I.15, the expression of the CM current generated by the CSAR is deduced in eq. eq. (I. 18).

$$\begin{bmatrix} I_{A_{out}} \\ I_N \\ I_P \\ I_{B_{out}} \end{bmatrix} = [Y_{load}] \cdot \begin{bmatrix} V_A \\ V_N \\ V_P \\ V_B \end{bmatrix}, \text{ with } [Y_{load}] = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \quad \text{eq. (I. 16)}$$

$$I_{CM_{bck}} = (I_{A_{out}} + I_N + I_P + I_{B_{out}}) \Big|_{DM=0} \quad \text{eq. (I. 17)}$$

$$I_{CM_{bck}} = Y_A \cdot V_A + Y_N \cdot V_N + Y_P \cdot V_P + Y_B \cdot V_B, \text{ where} \quad \text{eq. (I. 18)}$$

$$Y_A = \sum_{i=1}^4 Y_{i1}, \quad Y_N = \sum_{i=1}^4 Y_{i2}, \quad Y_P = \sum_{i=1}^4 Y_{i3}, \quad \text{and} \quad Y_B = \sum_{i=1}^4 Y_{i4}$$

However, the expression of the CM current can be simplified by replacing V_P and V_N with their expressions eq. eq. (I. 19) that are functions of V_A and V_B .

$$\begin{cases} V_P = V_A - V_{K1H} \\ V_N = V_A + V_{K1L} \end{cases} \quad \text{eq. (I. 19)}$$

Depending on the switch control law adopted for the CSAR's IGBTs (T_{1H} , T_{2H} , T_{1L} and T_{2L}), the voltages across the switches (K_{1H} , K_{2H} , K_{1L} and K_{2L}) can be deduced in Table I. 3. It should be noted that the high-side diodes share the same states as their series IGBTs; however, the low-side diodes depend on the polarity of the input voltage because their series IGBTs are always turned on. The binary numbers are an indication of the state of the IGBT or diode ('0' for turned-off and '1' for turned-on).

Table I. 3. VOLTAGES ACROSS THE CSAR'S SWITCHES

Grid side input voltage v_{AB}	State of IGBT/Diode								Voltages across the switches				Output voltage
	T_{1H}	T_{2H}	T_{1L}	T_{2L}	D_{1H}	D_{2H}	D_{1L}	D_{2L}	v_{K1H}	v_{K2H}	v_{K1L}	v_{K2L}	v_{PN}
Positive half cycle $f_D = 1$	0	1	1	1	0	1	0	1	v_{AB}	0	$-v_{AB}$	0	0 <i>Freewheel</i>
	1	0	1	1	1	0	0	1	0	$-v_{AB}$	$-v_{AB}$	0	v_{AB} <i>Active State</i>
Negative half cycle $f_D = 0$	0	1	1	1	0	1	1	0	v_{AB}	0	0	v_{AB}	$-v_{AB}$ <i>Active State</i>
	1	0	1	1	1	0	1	0	0	$-v_{AB}$	0	v_{AB}	0 <i>Freewheel</i>

It can be deduced that the voltages across the switches K_{1H} and K_{1L} depend on the input differential voltage V_{AB} and the switching functions defined earlier, as such:

$$\begin{cases} V_{K1H} = [\delta - F_D * F_{T1H} + (\delta - F_D) * (F_{T2H} - \delta)] * (V_A - V_B) \\ V_{K1L} = F_D * (V_B - V_A) \end{cases} \quad \text{eq. (I. 20)}$$

Therefore,

$$\begin{cases} V_P = \frac{V_A + V_B}{2} + \frac{[-\delta + 2F_D * F_{T1H} - 2(\delta - F_D) * (F_{T2H} - \delta)]}{2} * (V_A - V_B) \\ V_N = \frac{V_A + V_B}{2} + \frac{[-2F_D + \delta]}{2} * (V_A - V_B) \end{cases} \quad \text{eq. (I. 21)}$$

By replacing the eq. eq. (I. 21) in eq. eq. (I. 18), the CM current generated by the CSAR can be rewritten as follows:

$$\begin{aligned} I_{CM_{\text{back}}} &= Y_A V_A + Y_B V_B + Y_N \left[\frac{V_A + V_B}{2} + \frac{[-2F_D + \delta]}{2} * (V_A - V_B) \right] + \dots \\ &+ Y_P \left[\frac{V_A + V_B}{2} + \frac{[-\delta + 2F_D * F_{T1H} - 2(\delta - F_D) * (F_{T2H} - \delta)]}{2} * (V_A - V_B) \right] \end{aligned} \quad \text{eq. (I. 22)}$$

This leads to the proposed CM model of the CSAR presented in Fig.I.16 (a).

3.2.2. Differential mode behavioral model of the CSAR

According to Fig.I.15, the differential output voltage and the CSAR's input current expressions are given in eq. eq. (I.23) and eq. eq. (I.24) respectively.

$$V_P - V_N = -V_{K1H} - V_{K1L} = [\delta - F_D * F_{T1H} + (\delta - F_D) * (F_{T2H} - \delta)] * (V_A - V_B) + F_D * (V_A - V_B) \quad \text{eq. (I.23)}$$

$$I_{A_{in}} = [F_D * F_{T1H} - (\delta - F_D) * F_{T2H}] * I_P |_{CM=0} \quad \text{eq. (I.24)}$$

Based on these equations, the differential mode behavior of the CSAR's switching cells can be modeled as shown in the circuit representation of Fig.I.16 (b).

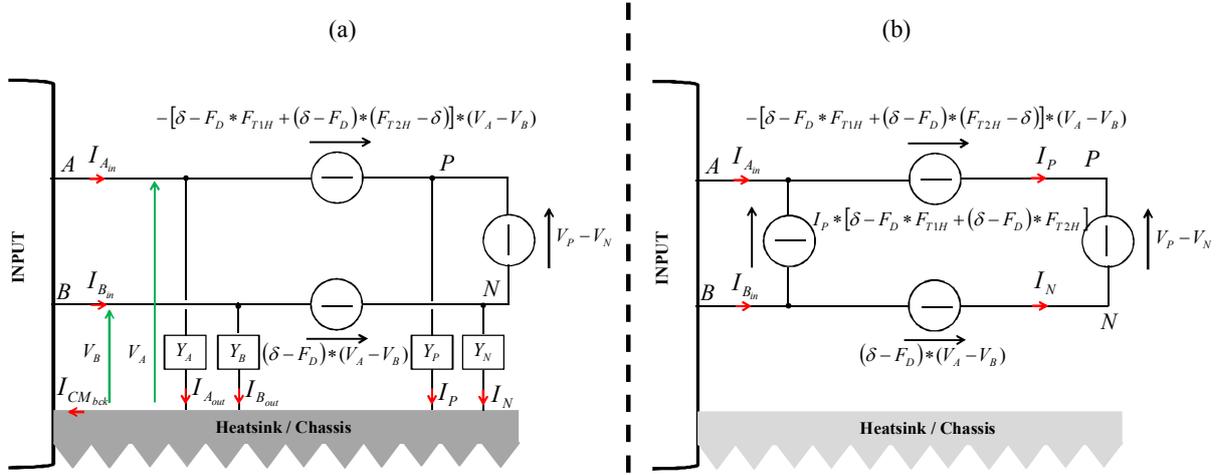


Fig.I.16. Proposed CM/DM models of the CSAR's switching cells. (a) CM, (b) DM.

3.2.3. Combined CM & DM model of the CSAR

Thus, the combined CM & DM model of the CSAR is given in Fig.I.17. Since there are two distinct switching cells, the model contains two controlled voltage sources that define the voltage fluctuations across the stray impedances. Usually two distinct controlled current sources should be modeled; however, in this model, they have been synthesized into a single current source. This is in line with the objective of this study: to find a simple conducted EMI model with a reduced number of sources in order to achieve low computational times and resources for an EMI filter synthesis.

Since the low side switches are always turned on, it can be seen in this model that the DC bus' negative side (at node N) fluctuates at the input mains' frequency leading to higher LF content of the leakage currents. The real source of HF common mode currents is directly linked to the upper switching cell with the voltage fluctuating at the switching frequency.

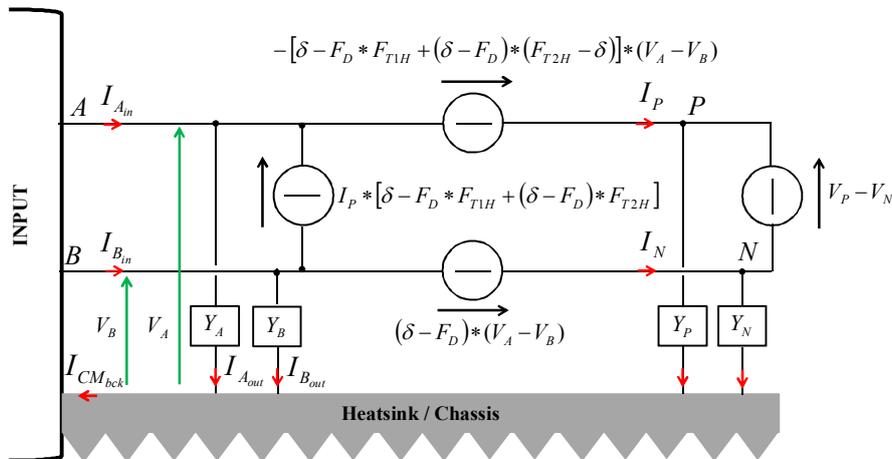


Fig.I.17. Combined CM & DM model of the CSAR switching cells.

3.3. Modeling of the DC bus inductive element

In this section, the Boost inductor is referred to as an inductive element (Fig.I.18). The reason behind this nomenclature is that the inductive element can be either a typical Boost inductor, or two separate inductors placed on both DC buses with equal or different inductance value, or two coupled inductors placed on the DC buses or even the traction's synchronous machine windings.

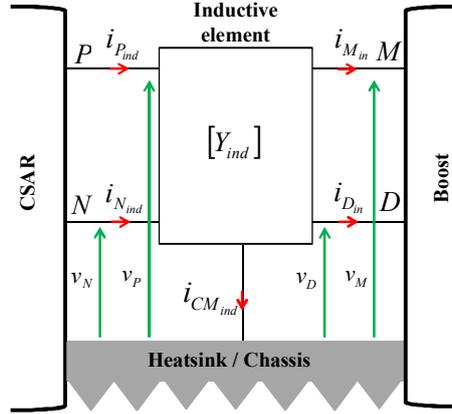


Fig.I.18. Representation of the generalized model of an inductive element placed on the DC bus.

Therefore, the proposed universal EMI model of the inductive element is given in Fig.I.19. The model uses a reduced number of admittances by replacing the localized couplings between the positive and negative ends of the DC bus with a mutual admittance \mathbf{Y}_{mut} . In addition, this mutual admittance also allows modeling the magnetic coupling that exists within an inductive element consisting of two inductors using the same magnetic core to create local CM and DM filtering effects (Refer to Section 3.3). Hence, the generalized admittance matrix representing the inductive element can be written as follows:

$$\begin{bmatrix} I_{P_{ind}} \\ I_{N_{ind}} \\ I_{M_{in}} \\ I_{D_{in}} \end{bmatrix} = \begin{bmatrix} (Y_P + Y_{PM}) & 0 & -Y_{PM} & -\mathbf{Y}_{mut} \\ 0 & (Y_N + Y_{ND}) & -\mathbf{Y}_{mut} & -Y_{ND} \\ Y_{PM} & \mathbf{Y}_{mut} & -(Y_{PM} + Y_M) & 0 \\ \mathbf{Y}_{mut} & Y_{ND} & 0 & -(Y_D + Y_{ND}) \end{bmatrix} \cdot \begin{bmatrix} V_P \\ V_N \\ V_M \\ V_D \end{bmatrix} \quad \text{eq. (I. 25)}$$

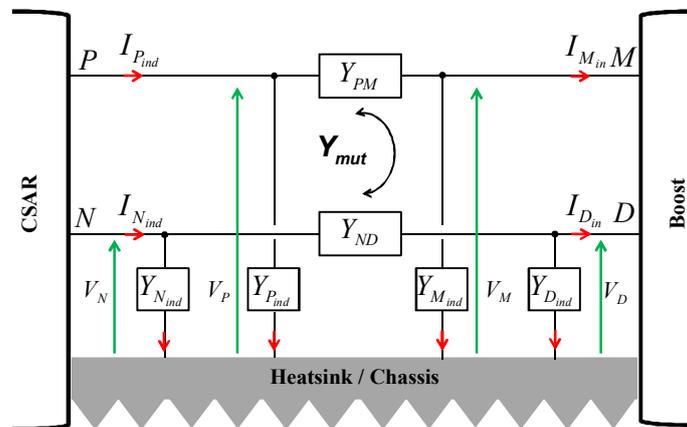


Fig.I.19. EMI model of the inductive element.

4. Application to the single-phase charger

4.1. Combined CM & DM EMI model

A major advantage of the proposed modeling approach is that the CM & DM EMI models developed for each component of the converter can be chained in order to form a global combined EMI model of the charger. The latter can be studied either by coding the mathematical equations transformed into frequency-domain under MATLAB for instance, or by developing a time-based circuit simulation of the model. In this case, simulation time is greatly reduced with regards to physics-based simulations incorporating exhaustive models of the semi-conductors under SPICE, SABER or ANSYS Simplorer.

The single-phase configuration of the charger is presented in Fig.I.20. The interest is directed towards the parasitic capacitances present at fluctuating nodes such as: the midpoints of the CSAR's switching cells C_N and C_P , the midpoint of the Boost's switching cell C_M and the parasitic capacitance between the battery and the chassis C_D .

In addition, the value of the resistive connection between the mains and the earth R_{ES} is dependent on the earthing system adopted. Hence, the charging station can be either directly connected to earth in case of TT and TN networks (very low R_{ES}), or isolated from earth in case of an IT network (very high impedance R_{ES}). In this section, the example will be given for a TT network (a direct connection to earth is established at the charging station level).

Furthermore, a single-phase Line Impedance Stabilization Network (LISN) is placed between the input mains and the charger's DM input capacitors. The LISN is used for conducted EMI measurements on vehicle components as defined by CISPR 16-1-2. The LISN has a dual role. In a normalized frequency range (150 kHz-30 MHz), it must isolate the grid, on which there may be CM and DM disturbances, from the equipment under test. In addition, it must present a fixed low impedance path with regards to the high-frequency disturbances emitted by the device under test, both in CM and in DM, independently of the grid's impedance [Costa et al. 2014].

Hence, the global EMI model of the single-phase charger is deduced by chaining the previously developed models of the CSAR, the inductive element and the Boost. The resulting model is given in Fig.I.21.

A simplified battery model is used. It does not allow the study of the possible interactions between the output dc-bus' capacitor and the high-voltage battery; however, it is sufficient for the validation of the previously developed models. Nonetheless, when compared to experimental findings, a more detailed model will be required for the battery. It will be modeled by a hybrid component that will include at least: the battery's open circuit voltage (which is a function of its state of charge), its internal impedance (which is a function of its state of charge) and its electrical connexions' stray impedances (series stray inductances as well as an additional stray capacitance at node E).

Simulations using PSIM software are carried out in order to validate the global EMI model of the charger.

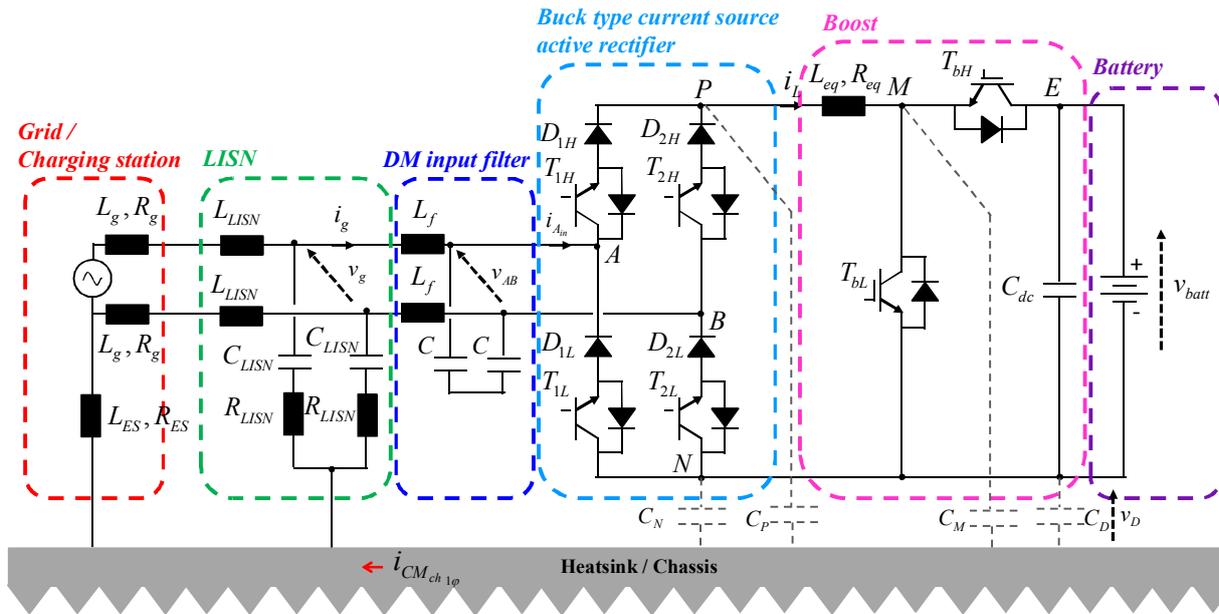


Fig.I.20. Power circuit of the single-phase charger showing parasitic capacitances.

4.2. Description of the control strategy used for simulations

The conducted emissions spectrum is highly dependent on the control strategy adopted and the switch control law implemented. Therefore, Fig.I.22 presents a synopsis of the control strategy used for the validation of the proposed single-phase EMI model.

The control is inspired from the strategy presented in [Gati et al. 2014]. The power factor correction at the input side of the charger is ensured by the duty cycle of the CSAR. The switch control law of the CSAR's IGBTs is given in Table I. 2 and incorporates the freewheeling state by closing a pair of switches belonging to the same bridge leg. On the other hand, the current in the Boost's filtering inductor is controlled in continuous conduction mode via the duty cycle of the Boost. Hence, the CSAR and the Boost are constantly simultaneously switching.

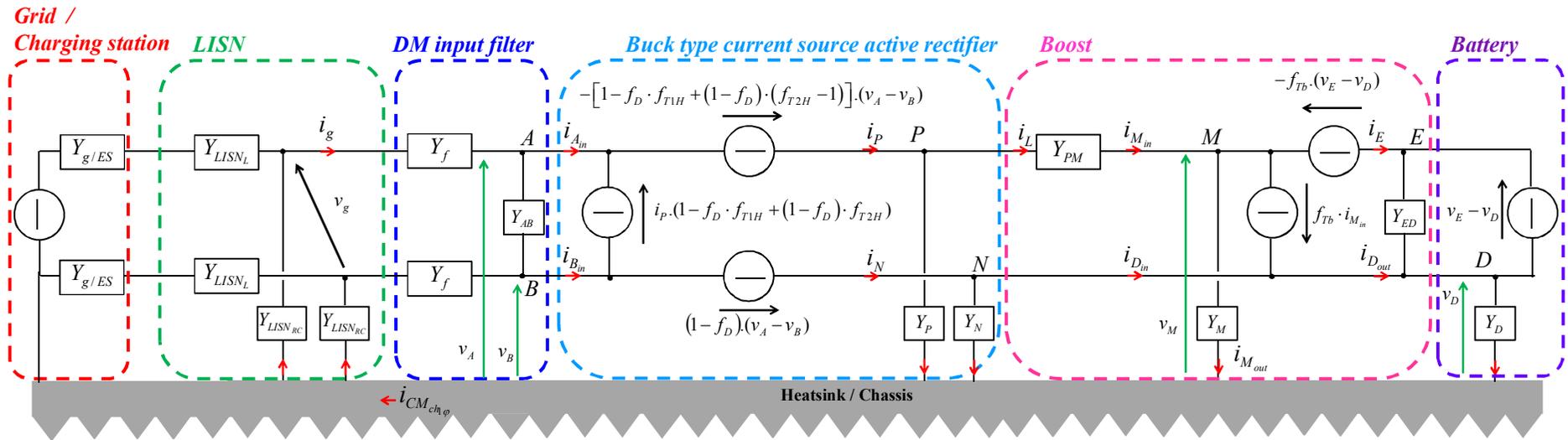


Fig.I.21. Combined CM & DM EMI model of the single-phase charger.

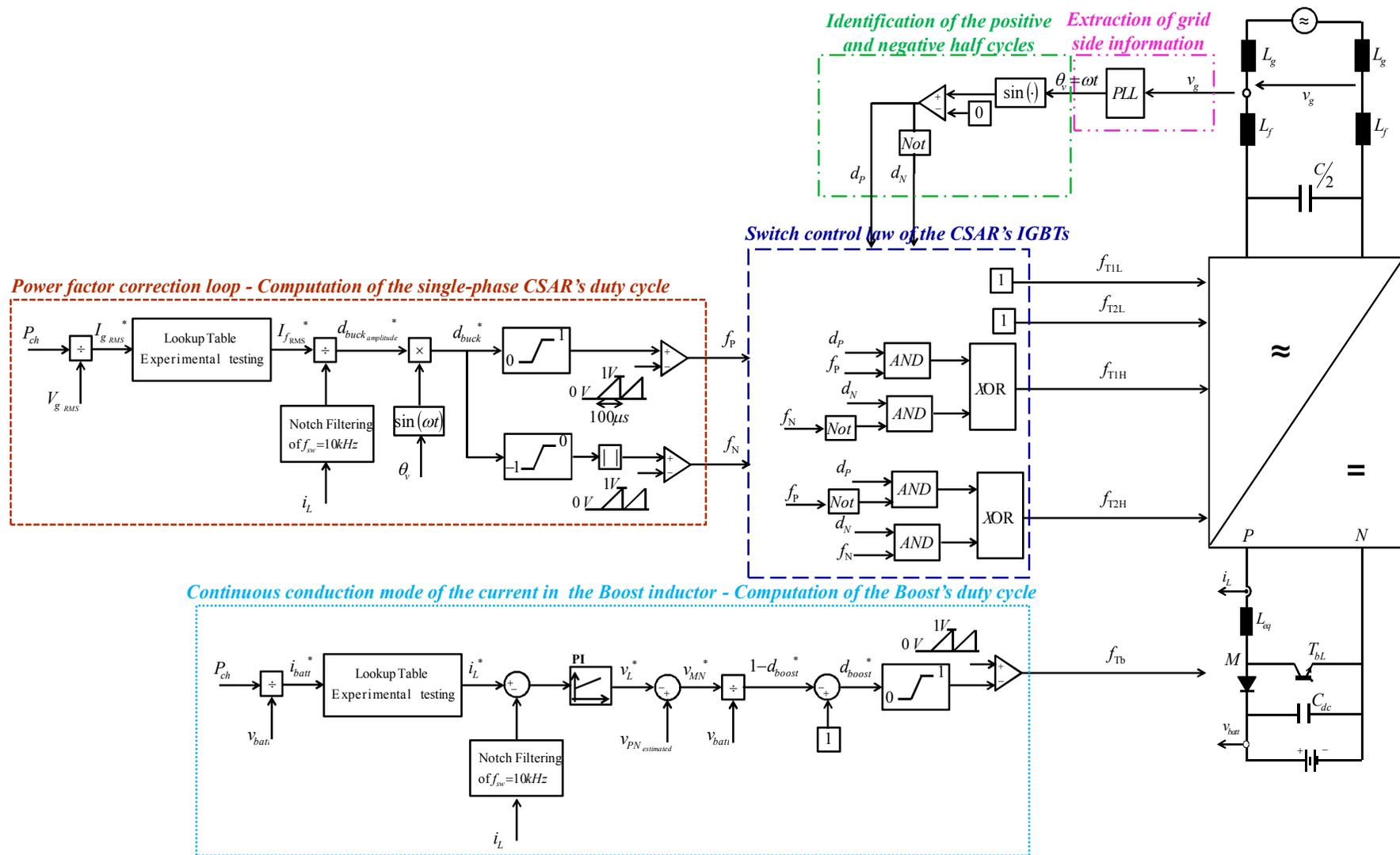


Fig.I.22. Synopsis of the single-phase control strategy used for simulations.

4.3. Simulation results using PSIM software

The control implemented is a closed loop control that ensures continuous conduction mode of the current flowing through the Boost's inductor. On one hand, the time-domain results for the line variables are provided in Fig.I.23. The current flowing through the Boost's inductor i_L as well as the current i_g at the input mains from the model simulation (green) show good adequacy with their counterparts from the circuit simulation (blue).

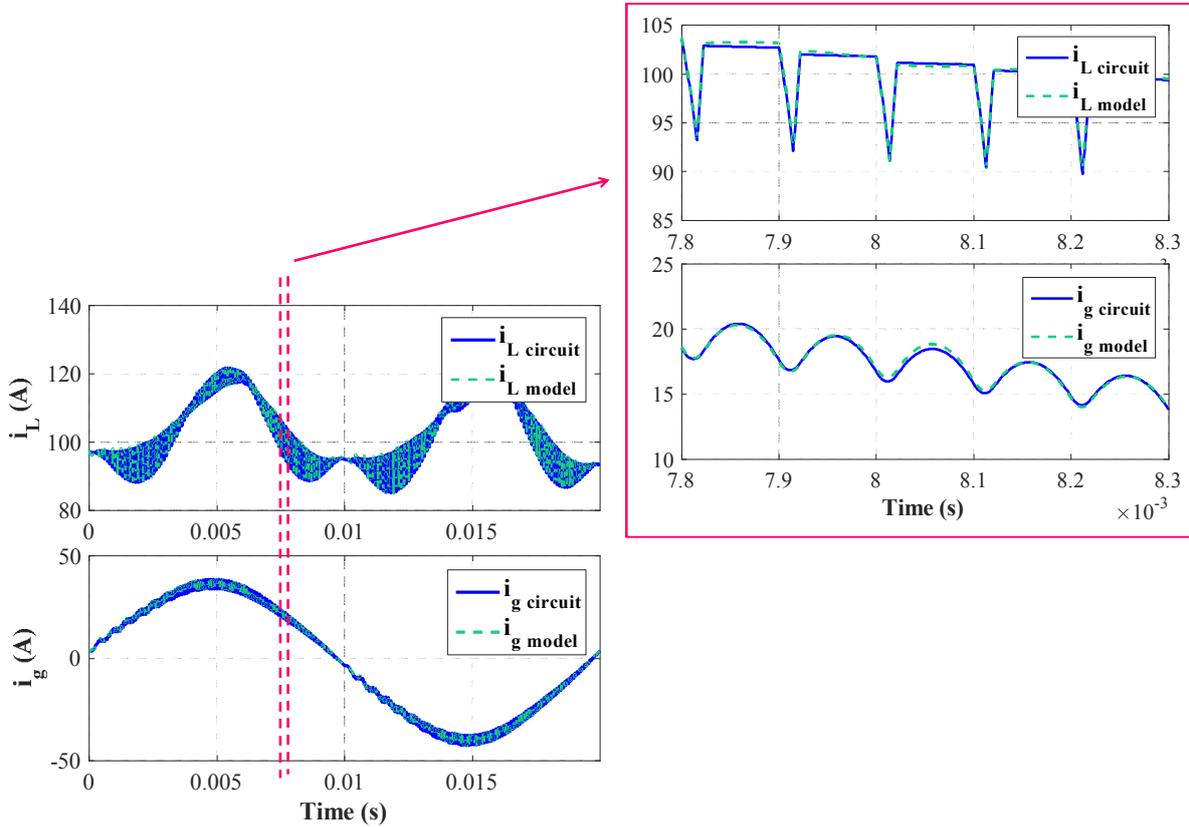


Fig.I.23. Time-domain simulation results. Circuit (blue). Model (green).

Common mode variables such as the common mode current $i_{CMch1\phi}$ generated by the charger and the voltage fluctuations of the negative side of the battery v_D are shown in Fig.I.24.

On the other hand, the frequency-domain analysis of the CM emissions is presented in Fig.I.25. The adequacy between the circuit simulation's results and the model simulation's results validate the modeling approach.

It should be noted that the spectrum shows high emissions at low frequencies (frequencies that are lower than the 10 kHz switching frequency). This is due to the high capacitive coupling between the high-voltage battery and the frame ground which is measured (onboard of the vehicle) at 30 nF. This value is used to model C_D . This coupling is greater than the values of the stray capacitances related to the semi-conductors and typically presenting tens to hundreds of pF. Moreover, Fig.I.24 shows that the voltage applied across C_D has a high low frequency content related to the mains' voltage.

In order to verify this assumption, the stray capacitance of the battery has been omitted from the simulation. The spectral analysis of the new common mode emissions is given in Fig.I.26. It shows that this high capacitive coupling is the main source of low frequency leakage currents that flow towards the chassis of the vehicle.

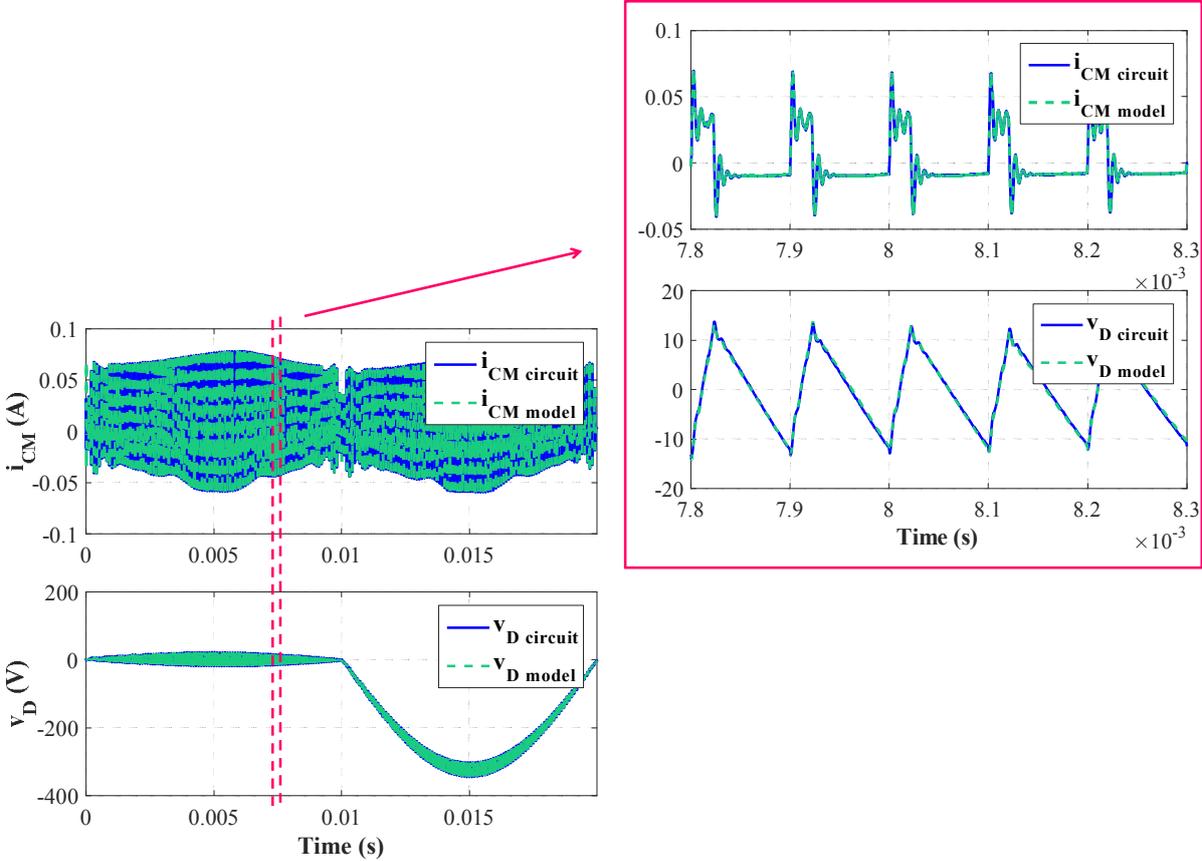


Fig.I.24. Time-domain simulation results. Circuit (blue). Model (green).

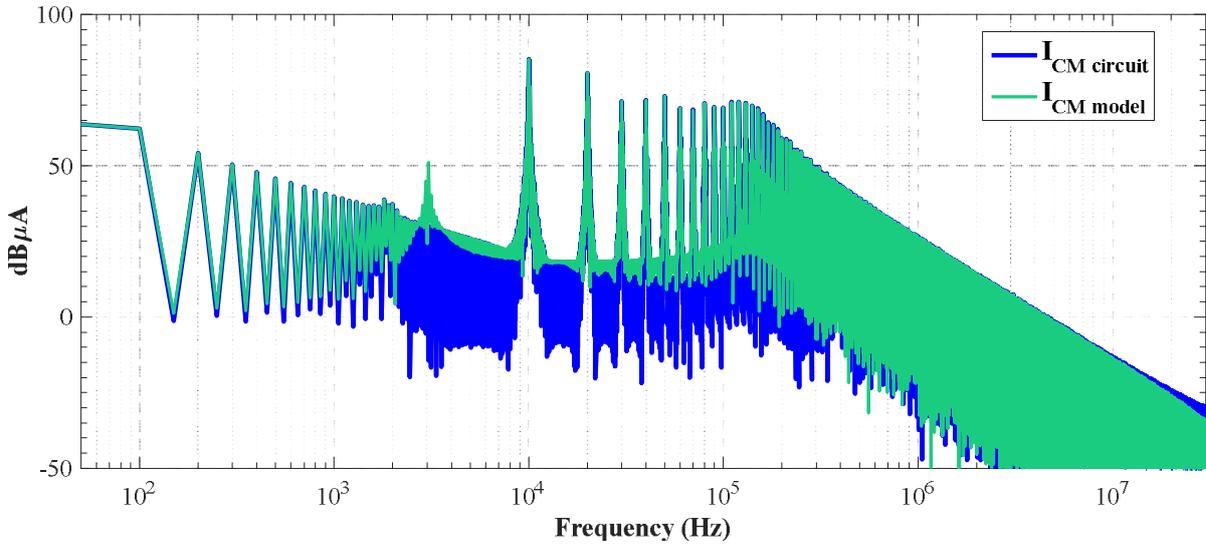


Fig.I.25. Frequency-domain analysis of the common mode emissions $i_{CM_{ch_{1\phi}}}$. Circuit (blue). Model (green).

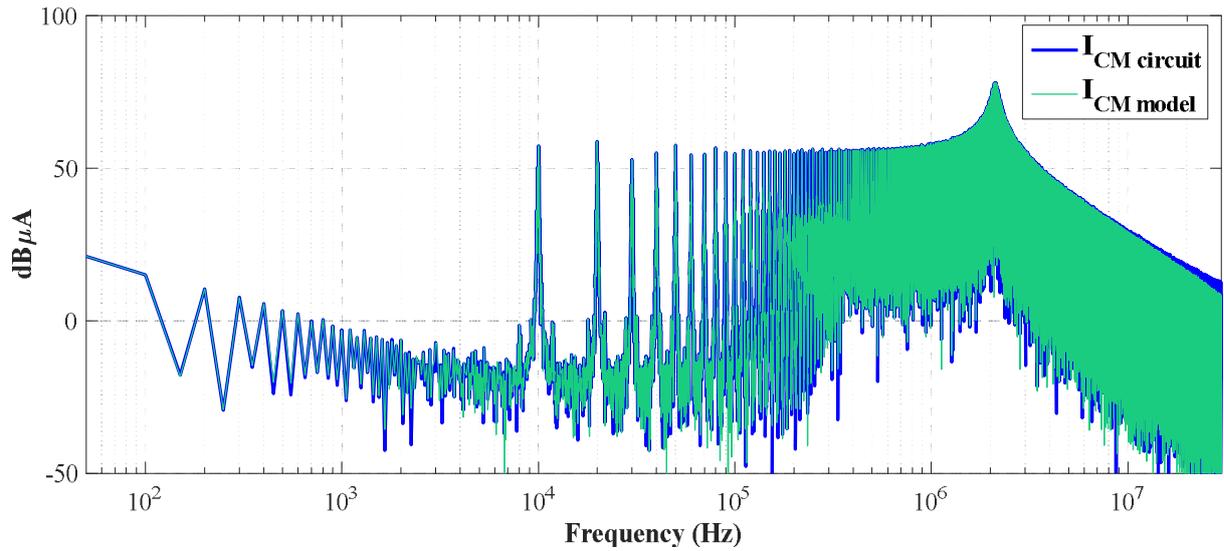


Fig.I.26. Frequency-domain analysis of the common mode emissions $i_{CM_{ch\ 1\phi}}$ without the stray capacitance between the battery and the frame ground C_D . Circuit (blue). Model (green).

Therefore, through this approach, it is possible to model the internal noise sources and propagation paths. It has been applied to a non-isolated on-board single-phase charger for EVs which verifies its chaining capability. Simulation results demonstrate the validity of the various developed models for the single-phase configuration.

Future topological CM mitigation techniques applied to the charger in the single-phase configuration need to be verified for the three-phase charging configuration as well; hence, the need to model the charger under its three-phase configuration.

5. Experimental validation using SiC MOSFETs: single-phase configuration

The experimental setup used to study the model's validity range with trapezoidal switching is presented in Fig.I.27.

The developed test bench consists of a single phase CSAR, with an additional freewheeling diode, connected to the input mains at the secondary side of an auto-transformer. The output of the rectifier is connected to an (R, L) load. The rectifier's switches are controlled in open loop.

A synopsis of the power circuit and the control implemented are shown in Fig.I.28 and the test bench parameters are given in

Table I. 4. The power supply's impedance is measured using the overlap phenomenon in a single phase diode bridge with an (R, L) load as described in Chapter 1 of Part A. (Please refer to Appendix E for the measurement of the total leakage inductance of the autotransformer)

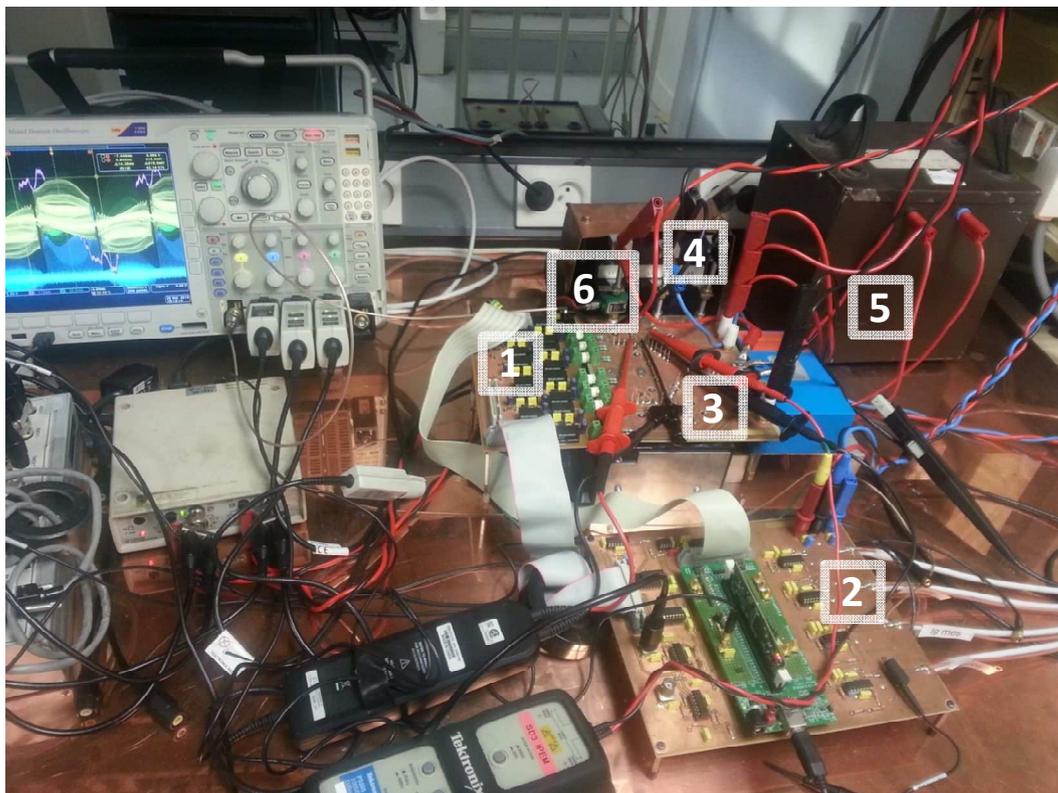


Fig.I.27. Test bench setup used for measurements. 1- Driver board, 2- Interface board for the TI F28335 DSP, 3- Power board with C2M0080120D Cree MOSFETs and SCS230KE2 ROHM SiC Schottky diodes, 4- DM filtering capacitors, 5- Load inductor, and 6- Pearson current monitor reference 2877 ($I_{RMS\ max}=2.5A$ and Bandwidth=300 Hz – 200 MHz).

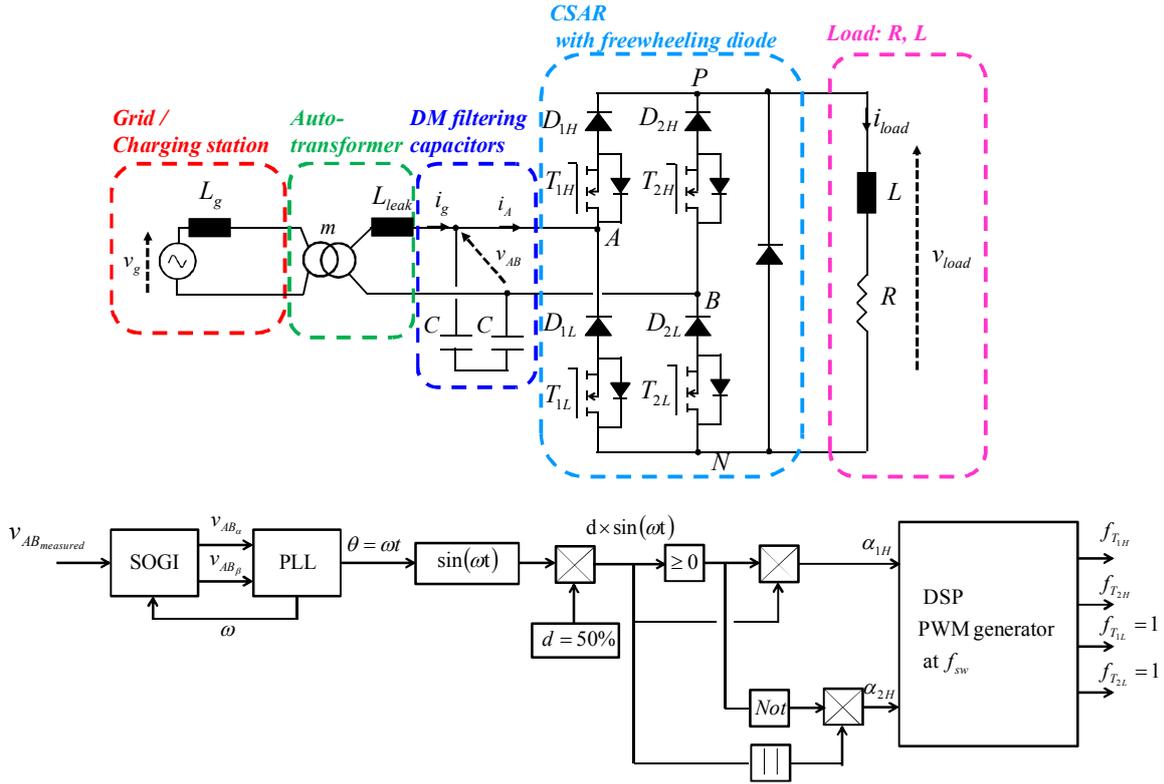


Fig.I.28. Synopsis of the test bench's power circuit and open loop control that is implemented for the measurement of the input current i_A .

Table I. 4. TEST BENCH SYSTEM PARAMETERS

Symbol	Description	Value (Units in SI)
V_{ABm}	Amplitude of the ac mains voltage measured at the secondary side of the autotransformer	$17\sqrt{2}$ (V)
ω	Angular line frequency	$2\pi \times 50$ (rad/s)
L_g	Grid impedance's imaginary part	50 (μ H)
m	Transform ratio	0.1
C	DM filtering capacitor	70 (μ F)
L	Load inductor	500 (mH)
R	Load resistor	30 (Ω)
I_{load}	Output DC load current	275 (mA)
V_{load}	Output DC voltage	8.3 (V)
f_{sw}	Switching frequency	10 (kHz) or 70 (kHz)
d	Duty cycle ratio	0.5

The objective of this experiment is to measure the converter's switched input current i_A in order to compare it to a trapezoidal waveform recreated from the command gate-to-source voltage v_{GS} .

Since the Pearson current monitor used has a bandwidth of 300Hz – 200 MHz and can sustain an RMS current of maximum 2.5 A without saturating, the measurements are conducted at an output voltage of 8.3 V and an output DC current of 275 mA. It should be noted that this operating point is far from the ratings of the semi-conductors used. For instance, the MOSFETs are rated at $V_{DS}= 1200V$ and $I_D=36A$. However, this should not affect the analysis conducted.

The experiments are conducted for two different switching frequencies: 10 kHz and 70 kHz. Each of these switching frequencies leading to measurements resembling the ones gathered in Fig.I.29.

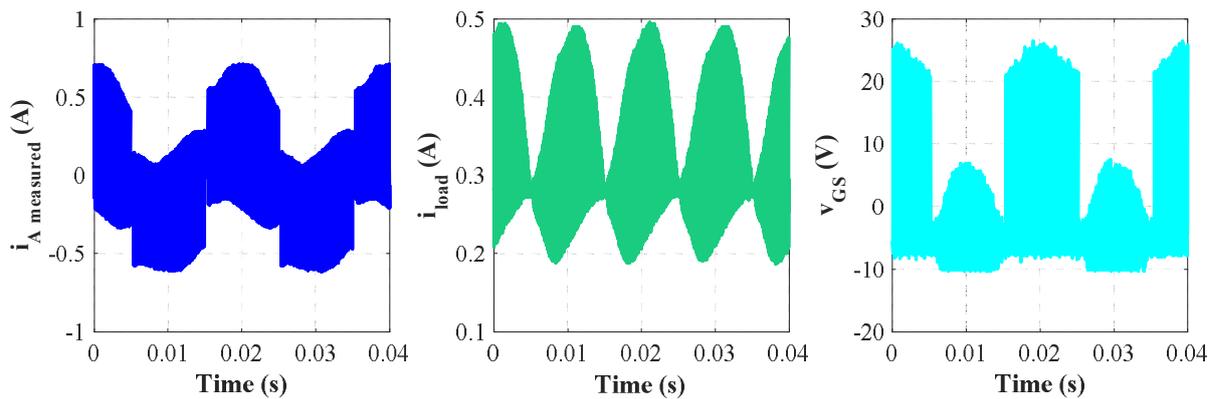


Fig.I.29. Experimental results obtained for a 10 kHz switching frequency. (blue) The converter input current. (green) The output's DC load current. (cyan) The gate-to-source voltage of T_{1H} (v_{GS}).

The main idea is to use the measured gate-to-source voltage of switch T_{1H} in order to recreate a binary signal with instantaneous switching (1V when $v_{GS}=18V$, 0V when $v_{GS}=-5V$) while neglecting the commutation oscillations. This binary signal is then shifted of 180° and returned with respect to zero in order to recreate the behavior during the negative half cycles of the input voltage.

Then, the sum of these two signals is multiplied with the output DC current level (275 mA). The resulting signal is a calculated version of the measured converter's input current $i_{A \text{ measured}}$ with trapezoidal switching.

In order to avoid the aliasing effect at high frequencies, the calculated current ($i_{A \text{ trapeze}}$) is twice convoluted with a 20 ns window in order to soften the commutations ($i_{A \text{ convoluted}}$) as shown in Fig.I.30 for a 10 kHz switching frequency.

The spectral analysis comparison between the measured converter input current and the computed and convoluted input current at a 10 kHz switching frequency is presented in Fig.I.31. The same procedure is applied for a higher switching frequency of 70 kHz and the results are presented in Fig.I.32.

The results obtained show a faithful reconstruction of the frequencies surrounding the switching frequencies. The approach's validity range lays around 1 MHz. Above this frequency, the commutation resonances at turn on and turn off of the switches result in differences between the spectrums. However, for the purpose of designing an input EMI filter, this frequency range of validity is acceptable. Therefore, the simplification of the controlled sources used in the conducted EMI models is justified.

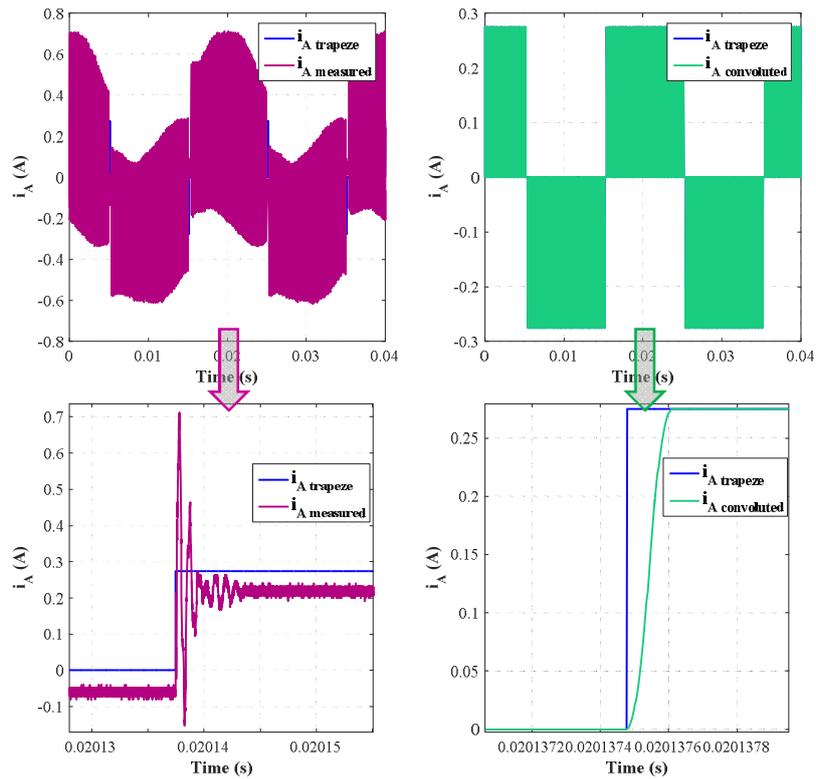


Fig.I.30. For a switching frequency of 10 kHz. The first graphs represent a comparison between the measured converter input current $i_{A \text{ measured}}$ and the idealized trapezoidal calculated converter input current $i_{A \text{ trapeze}}$ with an emphasis on the turn on commutation. The second graphs show the effect of the double convolution ($i_{A \text{ convoluted}}$) on the softening of the idealized commutations.

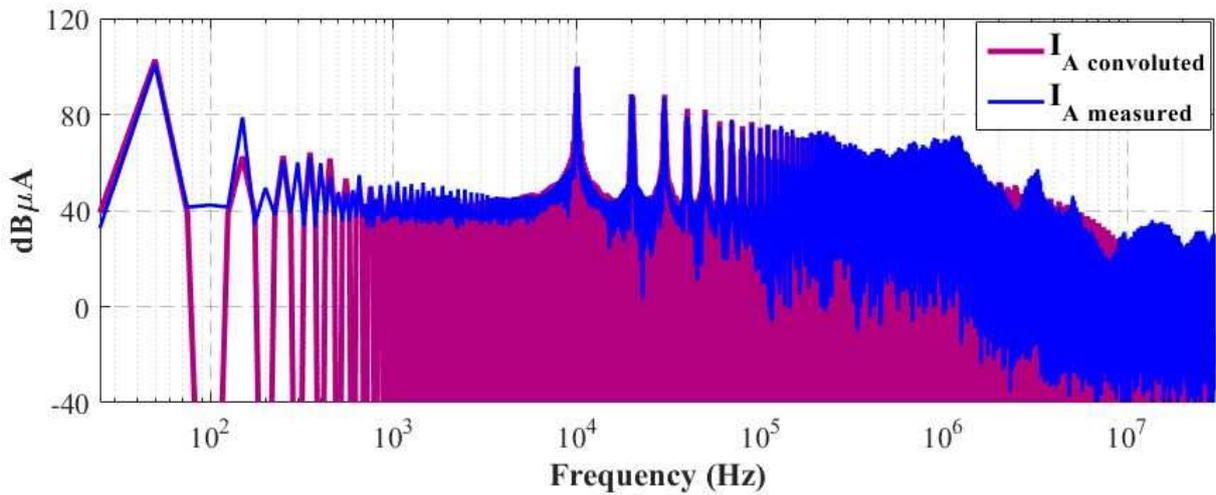


Fig.I.31. Spectral analysis comparison between the measured converter input current and the computed and convoluted idealized input current for a switching frequency of 10 kHz.

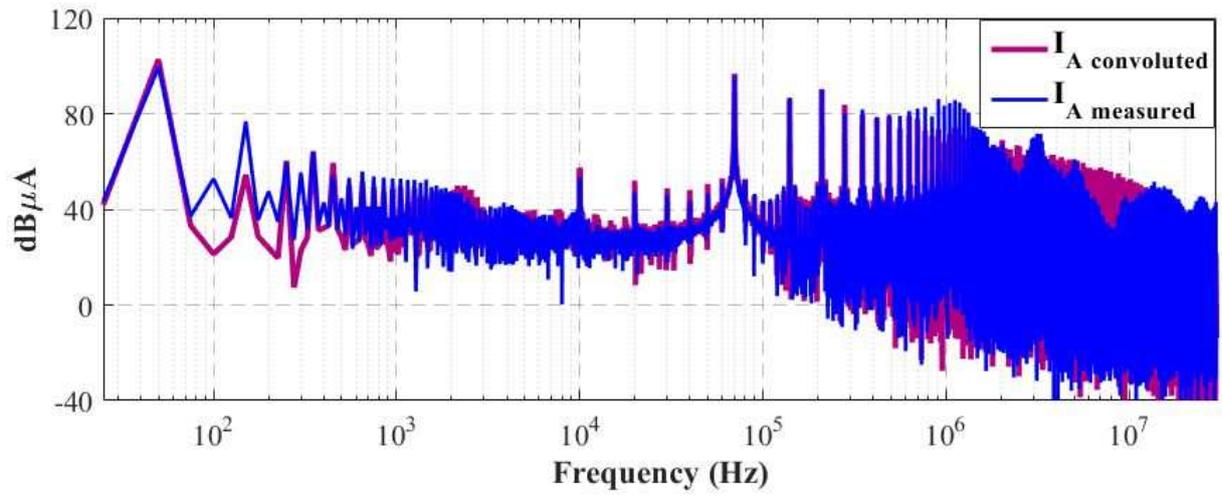


Fig.I.32. Spectral analysis comparison between the measured converter input current and the computed and convoluted idealized input current for a switching frequency of 70 kHz.

6. Application to the three-phase charging configuration

The models of the Boost and its filtering inductor are the same as the ones developed for the single-phase charging configuration. However, the input ac-dc rectifier's topology changes when fast charging the EV. Therefore, the model of the three-phase CSAR needs to be developed.

6.1. Modeling of the CSAR for three-phase charging

For the three-phase charging configuration, the association of each switch with its series diode $\{T_{iH/L}, D_{iH/L}\}$ is modeled by a single switching element $K_{iH/L}$. Two switching cells can be distinguished; the upper switches form a switching cell having the node P as midpoint and the lower switches form a switching cell having the node N as midpoint. Hence, at each switching period only one upper switch and one lower switch are both turned on at the same time. This means that the switches impose the turn on and off states of their series diodes. Therefore, eq. eq. (I. 26) defines the switching functions that are going to be used in the modeling process. The three-phase configuration of the CSAR is given in Fig.I.33.

$$\begin{cases} f_{K_{iH}} = f_{T_{iH}} \\ f_{K_{iL}} = f_{T_{iL}} \end{cases}, \quad i = 1, 2 \text{ or } 3 \quad \text{eq. (I. 26)}$$

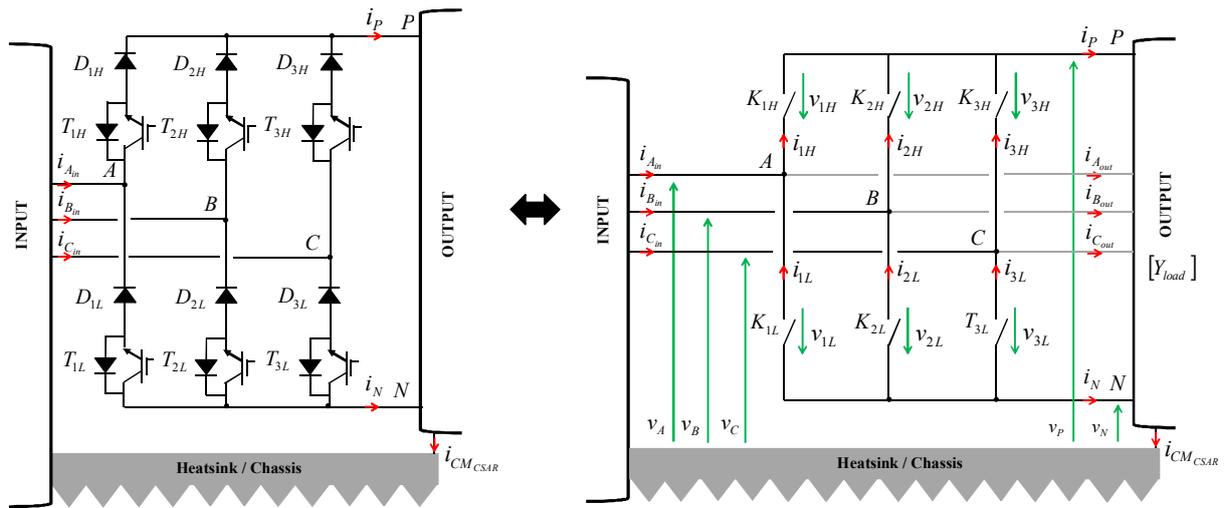


Fig.I.33. Representation of the CSAR used for three-phase charging.

6.1.1. CM modeling of the three-phase CSAR

Using the same modeling approach, the expression of the CM current generated by the three-phase CSAR is obtained in eq. eq. (I. 29) by combining eq. eq. (I. 27) and eq. eq. (I. 28).

$$\begin{bmatrix} I_P \\ I_{A_{out}} \\ I_{B_{out}} \\ I_{C_{out}} \\ I_N \end{bmatrix} = [Y_{load}] \cdot \begin{bmatrix} V_P \\ V_A \\ V_B \\ V_C \\ V_N \end{bmatrix}; \quad \text{avec } [Y_{load}] = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} & Y_{15} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} & Y_{25} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} & Y_{35} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} & Y_{45} \\ Y_{51} & Y_{52} & Y_{53} & Y_{54} & Y_{55} \end{bmatrix} \quad \text{eq. (I. 27)}$$

$$I_{CM_{CSAR}} = \left(I_P + I_{A_{out}} + I_{B_{out}} + I_{C_{out}} + I_N \right)_{DM=0} \quad \text{eq. (I. 28)}$$

$$I_{CM_{CSAR}} = Y_P \cdot V_P + Y_A \cdot V_A + Y_B \cdot V_B + Y_C \cdot V_C + Y_N \cdot V_N; \text{ where}$$

$$Y_P = \sum_{i=1}^5 Y_{i1}, \quad Y_A = \sum_{i=1}^5 Y_{i2}, \quad Y_B = \sum_{i=1}^5 Y_{i3}, \quad Y_C = \sum_{i=1}^5 Y_{i4}, \quad \text{and} \quad Y_N = \sum_{i=1}^5 Y_{i5} \quad \text{eq. (I. 29)}$$

This expression can be written as a function of V_A , V_B and V_C , as follows:

$$\begin{cases} V_P = -V_{1H} + V_A \\ V_N = V_A + V_{1L} \end{cases} \quad \text{eq. (I. 30)}$$

Moreover,

$$\begin{cases} V_{1H} = (\delta - F_{K_{1H}}) * [F_{K_{2H}} * (V_A - V_B) + F_{K_{3H}} * (V_A - V_C)] \\ V_{1L} = -(\delta - F_{K_{1L}}) * [F_{K_{2L}} * (V_A - V_B) + F_{K_{3L}} * (V_A - V_C)] \end{cases} \quad \text{eq. (I. 31)}$$

By replacing eq. eq. (I. 31) into eq. eq. (I. 30):

$$\begin{cases} V_P = [3F_{K_{2H}} * (F_{K_{1H}} - \delta) + \delta] * \frac{V_A - V_B}{3} + [3F_{K_{3H}} * (F_{K_{1H}} - \delta) + \delta] * \frac{V_A - V_C}{3} + \frac{V_A + V_B + V_C}{3} \\ V_N = [3F_{K_{2L}} * (F_{K_{1L}} - \delta) + \delta] * \frac{V_A - V_B}{3} + [3F_{K_{3L}} * (F_{K_{1L}} - \delta) + \delta] * \frac{V_A - V_C}{3} + \frac{V_A + V_B + V_C}{3} \end{cases} \quad \text{eq. (I. 32)}$$

Hence, the CM current generated by the three-phase CSAR can be written as follows:

$$\begin{aligned} I_{CM_{CSAR}} &= Y_P \cdot \left[[3F_{K_{2H}} * (F_{K_{1H}} - \delta) + \delta] * \frac{V_A - V_B}{3} + [3F_{K_{3H}} * (F_{K_{1H}} - \delta) + \delta] * \frac{V_A - V_C}{3} + \frac{V_A + V_B + V_C}{3} \right] + \dots \\ &+ Y_N \cdot \left[[3F_{K_{2L}} * (F_{K_{1L}} - \delta) + \delta] * \frac{V_A - V_B}{3} + [3F_{K_{3L}} * (F_{K_{1L}} - \delta) + \delta] * \frac{V_A - V_C}{3} + \frac{V_A + V_B + V_C}{3} \right] + \dots \\ &+ Y_A \cdot V_A + Y_B \cdot V_B + Y_C \cdot V_C \end{aligned} \quad \text{eq. (I. 33)}$$

6.1.2. DM modeling of the three-phase CSAR

On the other hand, the DM equations are deduced from Fig.I.33 by writing the relations between line to line variables.

$$\begin{cases} I_{A_{in}} = (F_{K_{1H}} - F_{K_{1L}}) * I_P \\ I_{B_{in}} = (F_{K_{2H}} - F_{K_{2L}}) * I_P \\ I_{C_{in}} = (F_{K_{3H}} - F_{K_{3L}}) * I_P \end{cases}_{CM=0} \quad \text{eq. (I. 34)}$$

$$\begin{aligned} V_P - V_N &= F_{K_{2H}} * (F_{K_{1H}} - \delta) * (V_A - V_B) + F_{K_{3H}} * (F_{K_{1H}} - \delta) * (V_A - V_C) - \dots \\ F_{K_{2L}} * (F_{K_{1L}} - \delta) * (V_A - V_B) &- F_{K_{3L}} * (F_{K_{1L}} - \delta) * (V_A - V_C) \end{aligned} \quad \text{eq. (I. 35)}$$

6.1.3. Combined CM & DM model of the three-phase CSAR

The high-side switches $\{K_{1H}, K_{2H}, K_{3H}\}$, form one global switching cell having the node P as midpoint and in which, three sub-switching cells are detected between the following switches $\{K_{1H}, K_{2H}\}$, $\{K_{2H}, K_{3H}\}$ and $\{K_{1H}, K_{3H}\}$. The same goes for the low-side switches $\{K_{1L}, K_{2L}, K_{3L}\}$ where the switching cells' midpoint is at node N. To sum up, two global switching cells and 6 sub-switching cells are identified.

Therefore, two distinct combined CM & DM conducted EMI models for the three-phase CSAR are developed depending on the switching cells retained.

On one hand, a first proposition of a combined CM & DM EMI model is made in Fig.I.34. The latter is based on the 6 sub-switching cells identified. This explains the high number of controlled sources (12) used to model this three-phase rectifier. The expressions of the controlled current sources and voltage sources are given in eq. eq. (I. 36) and eq. eq. (I. 37) respectively.

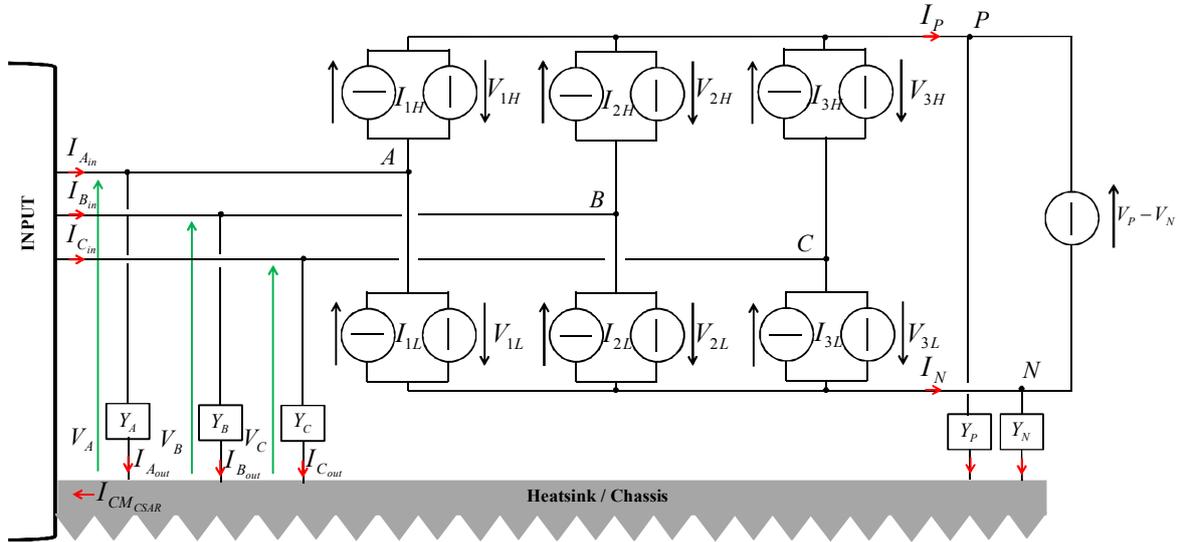


Fig.I.34. An extended combined CM & DM conducted EMI model of the three-phase CSAR.

$$\begin{cases} I_{iH} = F_{K_{iH}} * I_P \\ I_{iL} = F_{K_{iL}} * I_P \end{cases}, i=1, 2 \text{ or } 3 \quad \text{eq. (I. 36)}$$

$$\begin{cases} V_{1H} = (\delta - F_{K_{1H}}) * [F_{K_{2H}} * (V_A - V_B) + F_{K_{3H}} * (V_A - V_C)] \\ V_{2H} = (\delta - F_{K_{2H}}) * [F_{K_{1H}} * (V_B - V_A) + F_{K_{3H}} * (V_B - V_C)] \\ V_{3H} = (\delta - F_{K_{3H}}) * [F_{K_{1H}} * (V_C - V_A) + F_{K_{2H}} * (V_C - V_B)] \\ V_{1L} = (\delta - F_{K_{1L}}) * [F_{K_{2L}} * (V_B - V_A) + F_{K_{3L}} * (V_C - V_A)] \\ V_{2L} = (\delta - F_{K_{2L}}) * [F_{K_{1L}} * (V_A - V_B) + F_{K_{3L}} * (V_C - V_B)] \\ V_{3L} = (\delta - F_{K_{3L}}) * [F_{K_{1L}} * (V_A - V_C) + F_{K_{2L}} * (V_B - V_C)] \end{cases} \quad \text{eq. (I. 37)}$$

On the other hand, under the consideration of a balanced three-phase network, the modeling of the two global switching cells (upper and lower) results in a reduced number of controlled sources as shown in Fig.I.35.

This is in line with the needs of this study to produce a model which requires low computational time and resources. Therefore, this model is retained for the rest of this study.

It is interesting to note that the single-phase model of the CSAR can be naturally deduced from the three-phase model of Fig.I.35 (of course with the adaptation of the content of the sources). In fact, during the single-phase charging, the third leg of the CSAR is disconnected from the phase C of the grid and the switches (T_{3H} & T_{3L}) are turned off. This leads to the model of Fig.I.17 characterized by a single current source and two voltage sources.

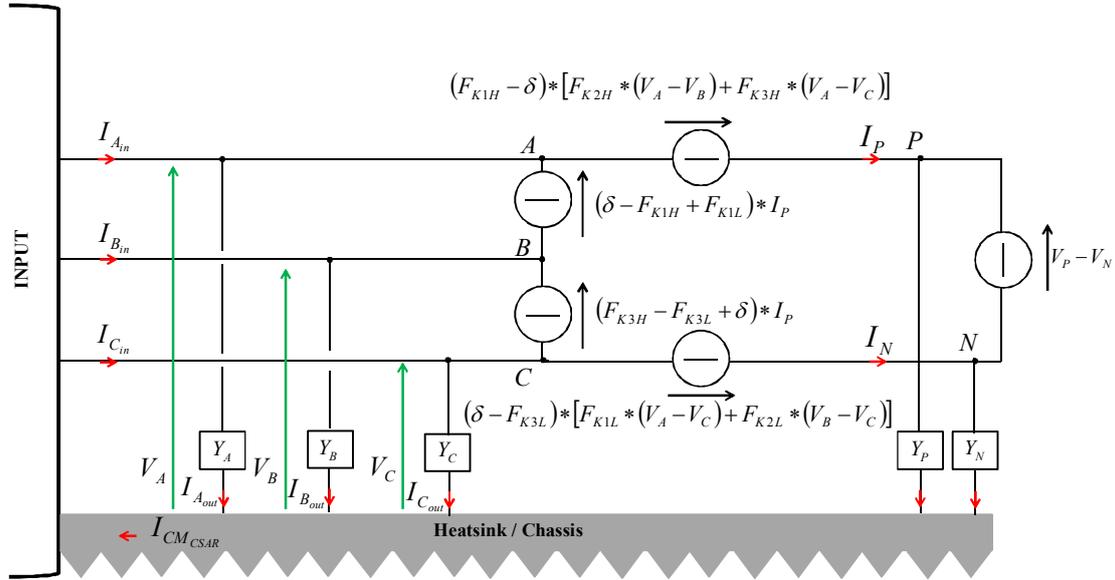


Fig.I.35. A reduced combined CM & DM conducted EMI model of the three-phase CSAR.

6.2. Combined CM & DM conducted EMI model of the three-phase charger

The power circuit of the three-phase charger is given in Fig.I.36 and the corresponding conducted EMI model is shown in Fig.I.37. This global model is obtained by chaining the previously developed models of the three-phase CSAR, the filtering inductor and the Boost. A three-phase LISN is placed at the input of the charger; thus, separating the high frequency emissions from (to) the power converter to (from) the charging station. In order to validate the modeling process, lumped stray capacitances are placed at the midpoints of the switching cells C_N , C_P and C_M . Furthermore, the mainly capacitive coupling between the battery and the chassis is represented by C_D .

The power circuit and the model are going to be simulated with the same control strategy in order to compare the time-domain and frequency content of the CM and DM variables. Therefore, it is necessary to explain the control strategy used for this validation.

As can be seen in Fig.I.38, the control strategy is divided into three main functions. The synchronization with the grid and the power factor correction are developed in Chapter 2 of Part A. However, as seen in the modeling procedure, the switching functions are essential for computing the voltages at the different internal nodes of the model. Hence, the study of the conducted emissions is highly dependent on the switch control law implemented. Therefore, the space vector pulse width modulation (SVPWM) scheme for the three-phase CSAR, used for validating the model of Fig.I.37, is given in Table I. 5. Different switching vector sequences are studied in Chapter 2 of Part A. The one retained for the model validation purposes is the Modified Fullwave Symmetrical Modulation

(MFSM) [Halkosaari et al. 2000]. Each sector is divided into two sub-sectors according to the comparison between the converter input voltages' instantaneous values.

It should be noted that for simplification purposes, the converter input phase voltages are considered to be in phase with the input phase currents of the CSAR. This explains why the power factor correction loop assumes a zero reference along the q-axis.

In addition, as demonstrated in Chapter 2 of Part A, the Boost does not intervene in the three-phase charging configuration (if we consider a grid voltage rated at 230 V_{RMS}). Therefore, the simulation results shown in the next paragraph correspond to the CSAR switching under SVPWM and the Boost switch maintained in the turn off position for the duration of the charge.

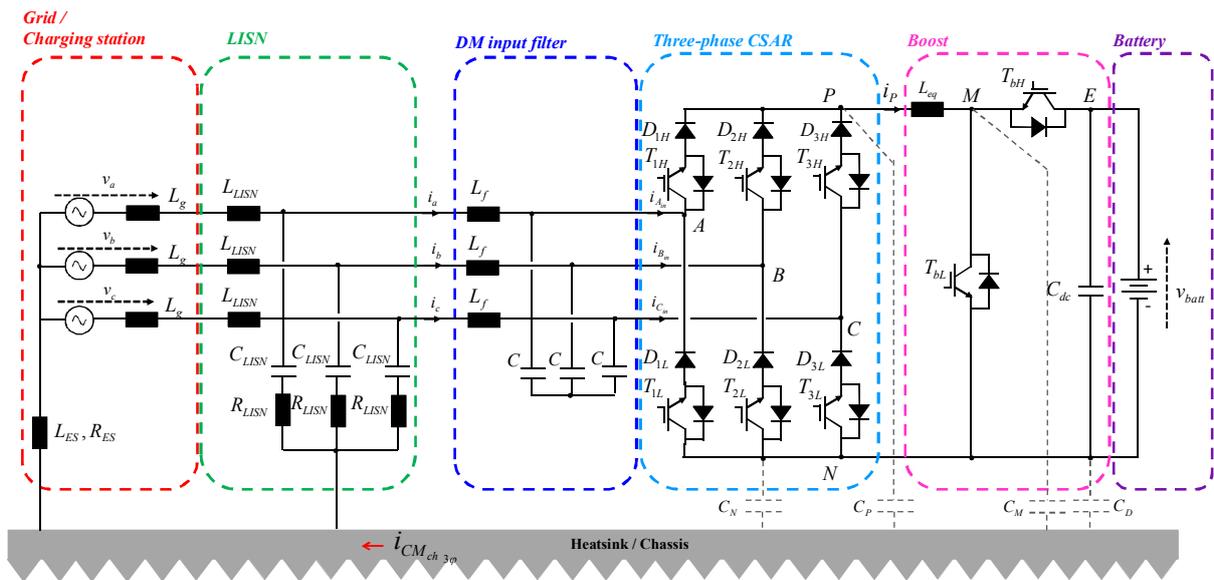


Fig.I.36. Power circuit of the three-phase charger.

6.2.1. Simulation results using co-simulation between PSIM and Matlab softwares

The power circuit of Fig.I.36 and the model of Fig.I.37 are simulated using PSIM (version 9.3). On the other hand, the control strategy of Fig.I.38 is implemented using Matlab (version 2011a). A co-simulation is rendered possible between these two softwares by means of an interface block that sends and receives signals from one software simulation to the other in real-time. Both softwares must have the same sampling period (10 ns) for the signals in order to avoid control divergence problems.

The power circuits are simulated using ideal switches. In order to validate the conducted EMI models developed, the use of trapeze shaped commutations to model the switching of the semi-conductors is justified. This allows for comparing the resulting signals under the same operating conditions. Once the models have been validated, a more realistic switching behavior can be implemented.

The time-domain simulation results of the grid side input line currents (i_a , i_b , i_c) and the output DC side current (i_L) are shown in Fig.I.39. Furthermore, the CM signals consisting of the CM current generated by the three-phase charger using the MFSM modulation strategy (i_{CM}) and the voltage fluctuations measured at the negative side of the battery (v_D) are illustrated in Fig.I.40. A good match between the power circuit's simulation results and the conducted EMI model's simulation results is further demonstrated by the analysis of the high frequency content of the CM currents (Fig.I.41).

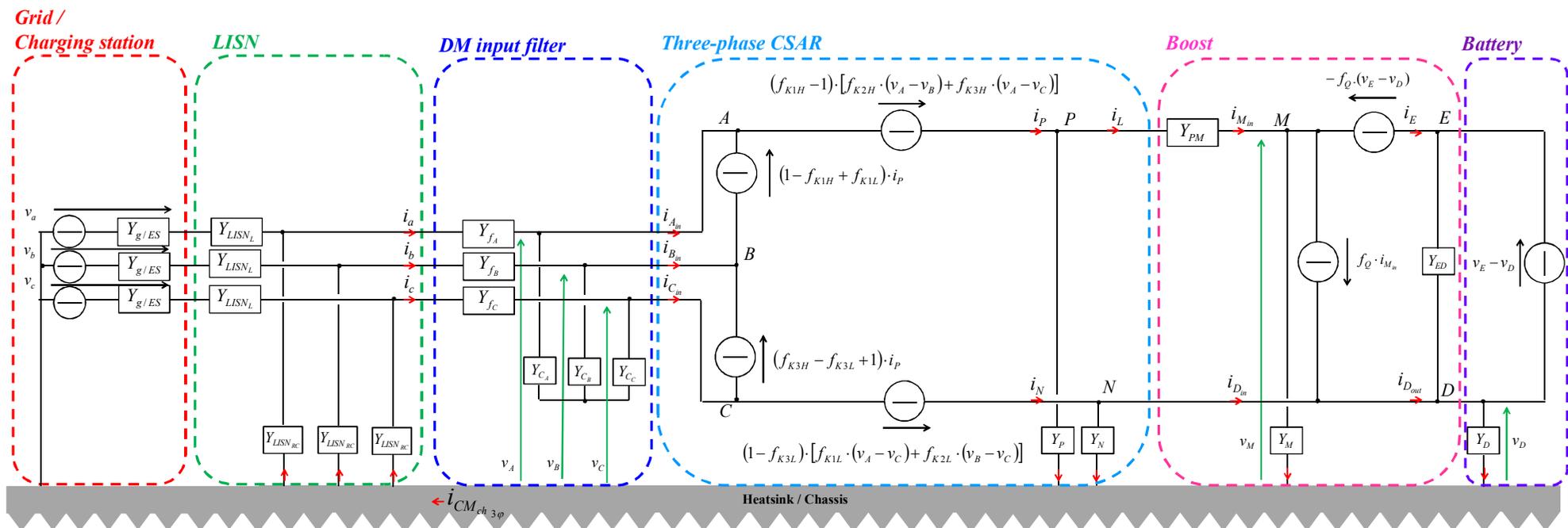


Fig.I.37. EMI model of the three-phase charger.

6.2.2. Description of the control strategy used for simulations

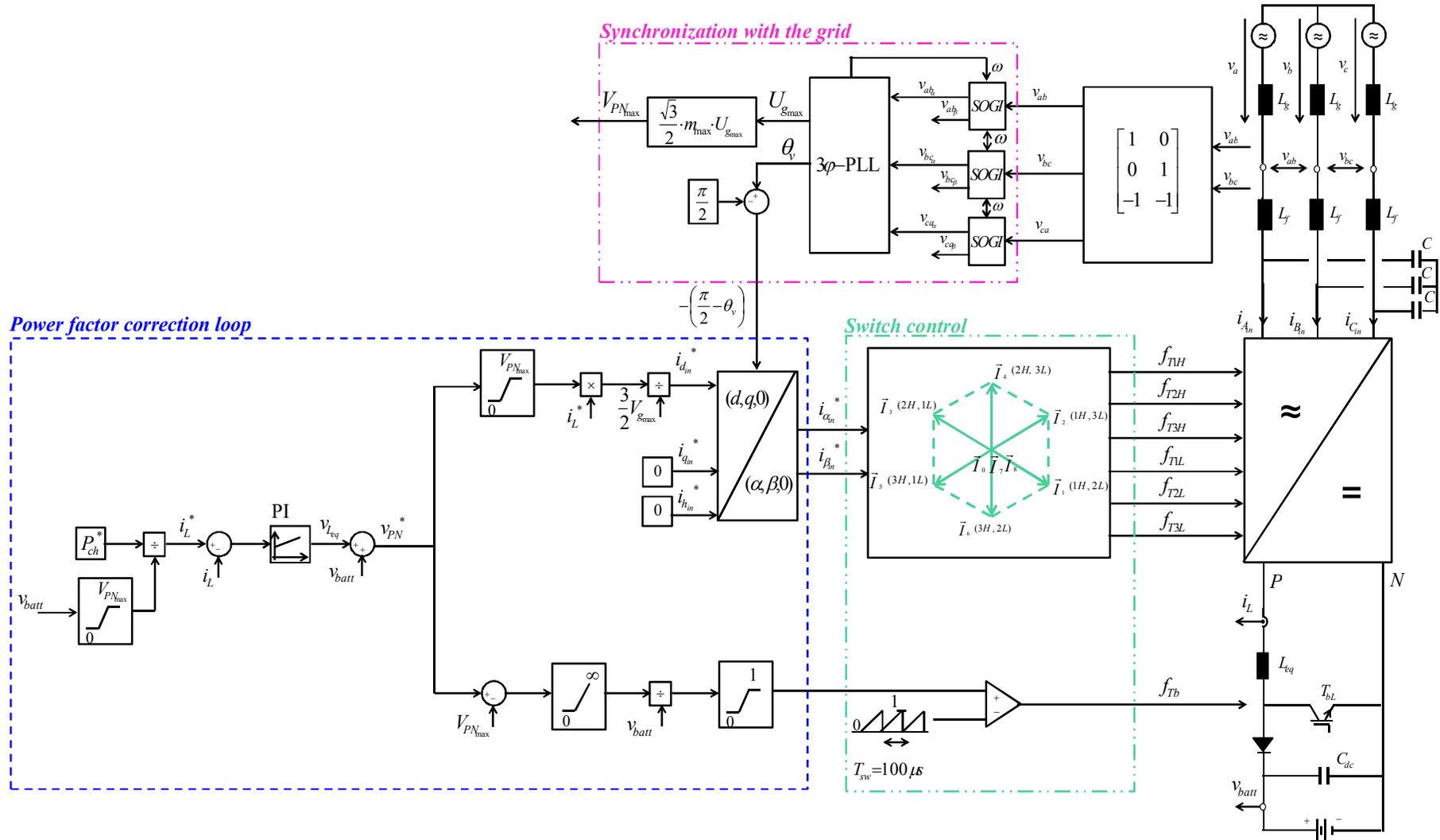


Fig.I.38. Diagram of the three-phase control strategy used for the simulations.

Table I. 5. SPACE VECTOR PULSE WIDTH MODULATION SCHEME

		Sectors		Input Voltages	MFSM Strategy
Sequences with respect to the sectors	I	Ia	$2\pi - \frac{\pi}{6} < \theta \leq 2\pi$	$v_A > 0 > v_C > v_B$	$[\vec{I}_0][\vec{I}_2][\vec{I}_1][\vec{I}_1][\vec{I}_2][\vec{I}_0]$
		Ib	$0 < \theta \leq \frac{\pi}{6}$	$v_A > 0 > v_B > v_C$	$[\vec{I}_0][\vec{I}_1][\vec{I}_2][\vec{I}_2][\vec{I}_1][\vec{I}_0]$
	II	IIa	$\frac{\pi}{6} < \theta \leq \frac{\pi}{3}$	$v_A > v_B > 0 > v_C$	$[\vec{I}_8][\vec{I}_4][\vec{I}_2][\vec{I}_2][\vec{I}_4][\vec{I}_8]$
		IIb	$\frac{\pi}{3} < \theta \leq \frac{\pi}{2}$	$v_B > v_A > 0 > v_C$	$[\vec{I}_8][\vec{I}_2][\vec{I}_4][\vec{I}_4][\vec{I}_2][\vec{I}_8]$
	III	IIIa	$\frac{\pi}{2} < \theta \leq \frac{2\pi}{3}$	$v_B > 0 > v_A > v_C$	$[\vec{I}_7][\vec{I}_3][\vec{I}_4][\vec{I}_4][\vec{I}_3][\vec{I}_7]$
		IIIb	$\frac{2\pi}{3} < \theta \leq \frac{5\pi}{6}$	$v_B > 0 > v_C > v_A$	$[\vec{I}_7][\vec{I}_4][\vec{I}_3][\vec{I}_3][\vec{I}_4][\vec{I}_7]$
	IV	IVa	$\frac{5\pi}{6} < \theta \leq \pi$	$v_B > v_C > 0 > v_A$	$[\vec{I}_0][\vec{I}_5][\vec{I}_3][\vec{I}_3][\vec{I}_5][\vec{I}_0]$
		IVb	$\frac{5\pi}{6} < \theta \leq \pi + \frac{\pi}{6}$	$v_C > v_B > 0 > v_A$	$[\vec{I}_0][\vec{I}_3][\vec{I}_5][\vec{I}_5][\vec{I}_3][\vec{I}_0]$
	V	Va	$\pi + \frac{\pi}{6} < \theta \leq \frac{4\pi}{3}$	$v_C > 0 > v_B > v_A$	$[\vec{I}_8][\vec{I}_6][\vec{I}_5][\vec{I}_5][\vec{I}_6][\vec{I}_8]$
		Vb	$\frac{4\pi}{3} < \theta \leq \frac{3\pi}{2}$	$v_C > 0 > v_A > v_B$	$[\vec{I}_8][\vec{I}_5][\vec{I}_6][\vec{I}_6][\vec{I}_5][\vec{I}_8]$
	VI	VIa	$\frac{3\pi}{2} < \theta \leq \frac{5\pi}{3}$	$v_C > v_A > 0 > v_B$	$[\vec{I}_7][\vec{I}_1][\vec{I}_6][\vec{I}_6][\vec{I}_1][\vec{I}_7]$
		VIb	$\frac{5\pi}{3} < \theta \leq 2\pi - \frac{\pi}{6}$	$v_A > v_C > 0 > v_B$	$[\vec{I}_7][\vec{I}_6][\vec{I}_1][\vec{I}_1][\vec{I}_6][\vec{I}_7]$

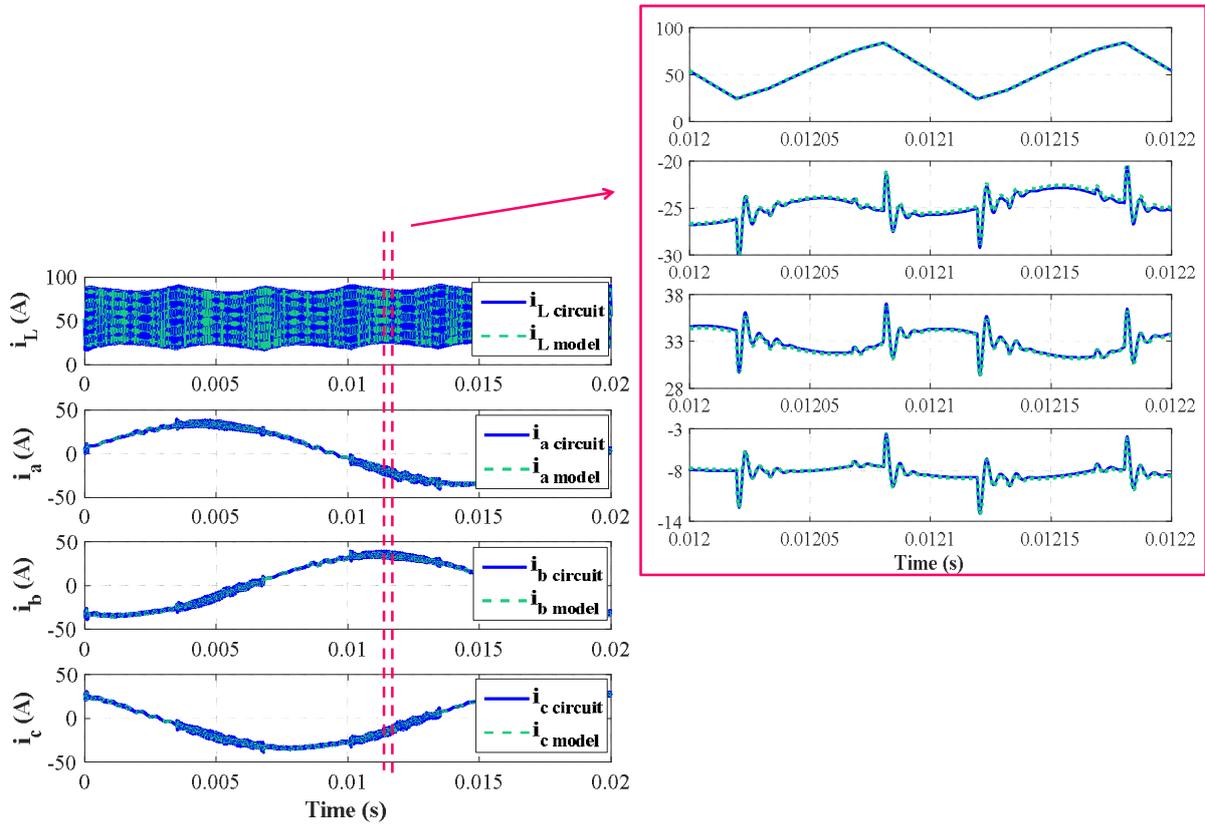


Fig.I.39. Time-domain simulation results of the line currents for the three-phase charger. Circuit (blue). Model (green).

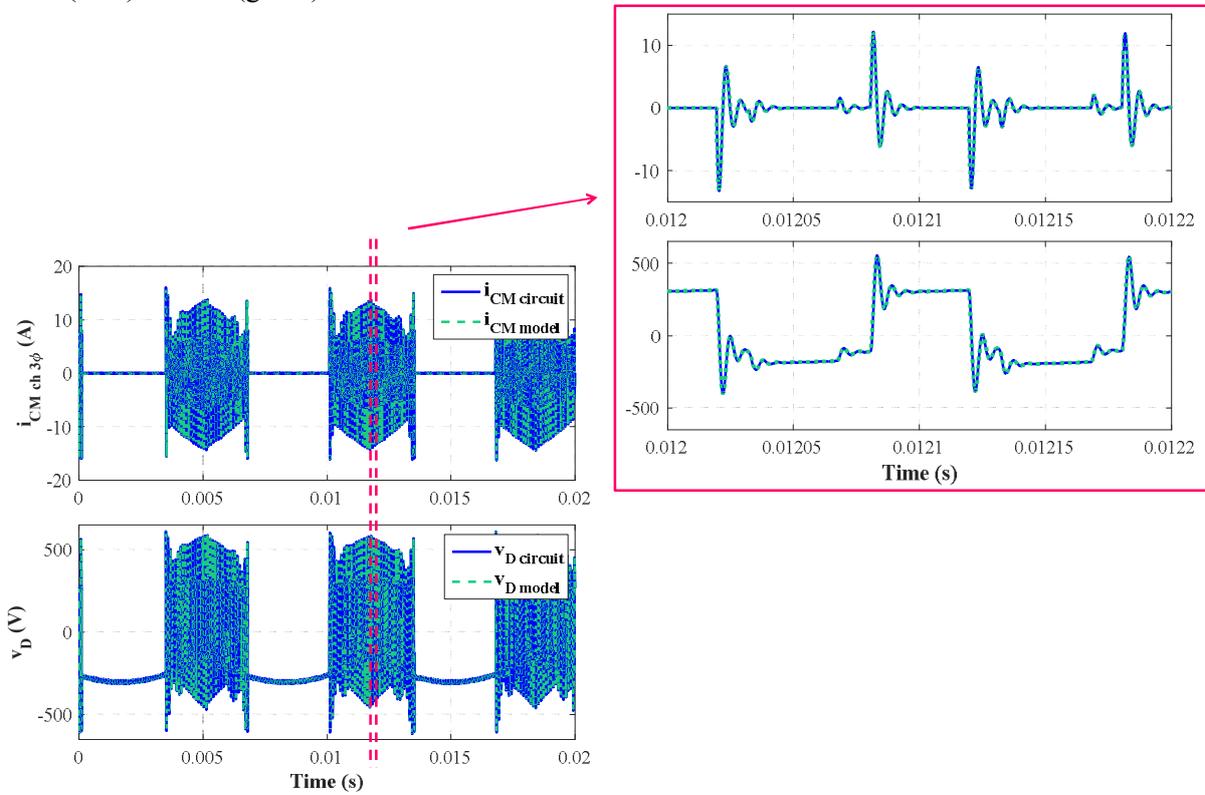


Fig.I.40. Time-domain simulation results of the CM current and the CM voltage at the negative side of the battery. Circuit (blue). Model (green).

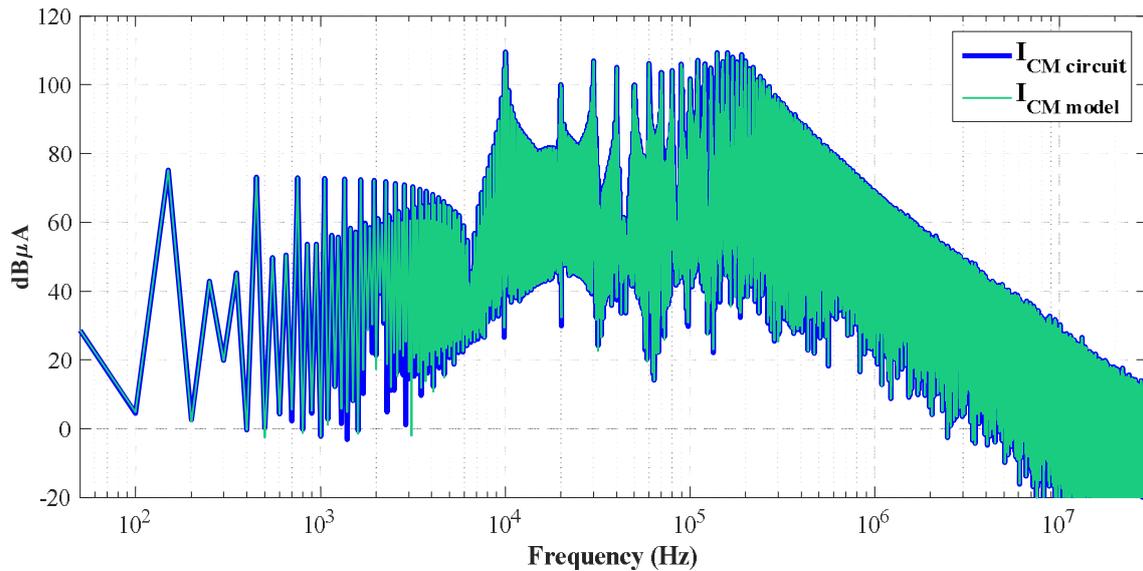


Fig.I.41. Frequency-domain analysis and comparison between the CM currents obtained from the circuit simulation (blue) and the model simulation (green).

It should be noted that, similar to the single-phase configuration, the spectrum shows high emissions at low frequencies due to the high capacitive coupling between the battery and the frame ground.

In order to verify this assumption, the stray capacitance of the battery has been omitted from the simulation. The spectral analysis of the new common mode emissions is given in Fig.I.42. It shows that this high capacitive coupling is the main source of low frequency leakage currents that flow towards the chassis of the vehicle. The remaining low frequency emissions are due to the other stray elements, such as the stray capacitance at node N being subjected to the voltage v_D of Fig.I.40.

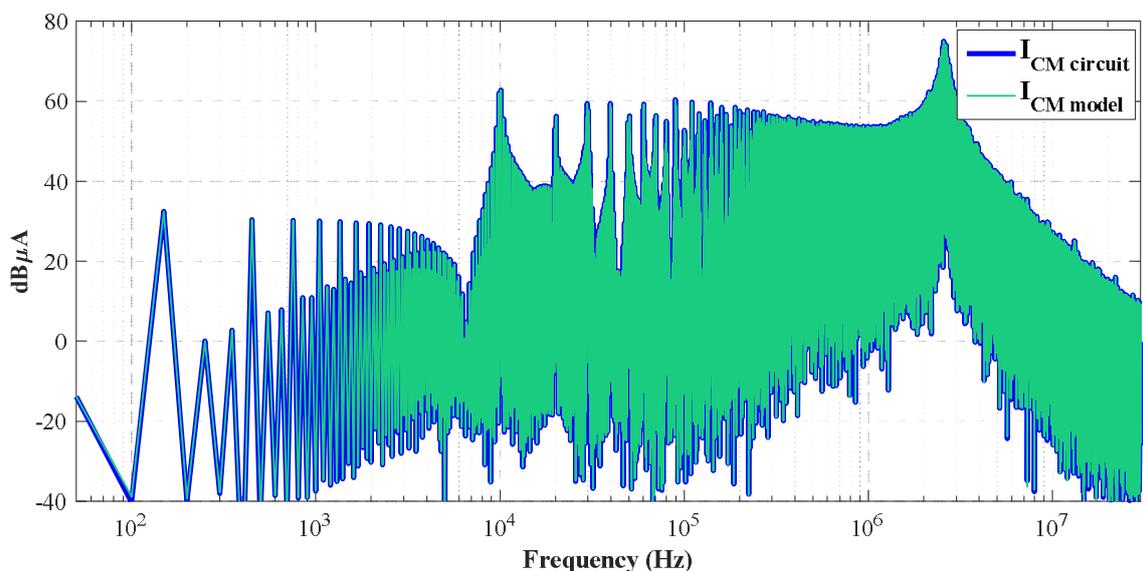


Fig.I.42. Frequency-domain analysis and comparison between the CM currents obtained from the circuit simulation (blue) and the model simulation (green) without the stray capacitance between the battery and the frame ground.

7. Reduction of the stray loop inductances of the CSAR power module

The objective of section is to show how the EMI design constraints should be taken into consideration when designing the power circuit of a converter; especially when it comes to the minimization of the commutation loop’s stray inductance.

The IGBT based module used as a three-phase CSAR is a typical automotive qualified inverter IGBT module hybrid pack 1 adjusted to integrate the series diodes as shown in Fig.I.43. Taking the example of the middle bridge leg between nodes (P, B & N), Fig.I.44 shows that each switch and its series diode are actually formed by placing two silicon dies in parallel in order for the switch and diode to withstand the nominal current. The IGBT’s anti-parallel diode, highlighted in this figure, ensures reverse blocking capabilities whenever the IGBT’s series diode is in reverse recovery. Since the hybrid pack is originally designed for inverter applications, the global design of the module minimizes the commutation loops’ stray inductances for each inverter leg that forms a switching cell. This is achieved by placing a decoupling capacitor at the dc inputs P and N of the inverter. The inverter’s outputs are A, B and C.

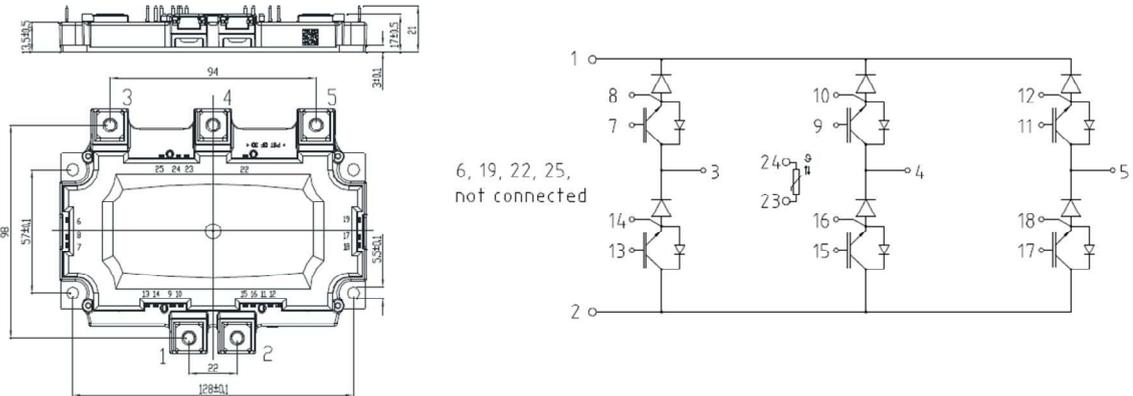


Fig.I.43. Infineon’s hybrid pack 1 adjusted to incorporate the series diodes of the CSAR [Infineon 2012].

However, when the same module is used as a rectifier, the decoupling capacitors are connected to the ac inputs A, B and C. In this case P and N represent the dc output of the rectifier.

Fig.I.45 shows two different commutation loops. It can be seen that the commutation loops are wide and uneven. On one hand, this means that the loops’ stray inductances are not optimal for conducted EMI emissions and uneven between the switching cells. On the other hand, the wide area of the commutation loops leads to higher radiated EMI emissions emanating from the module as well as disturbances received by the module.

The solution proposed in this study and implemented while developing the power circuit board using the SiC MOSFET technology is shown in Fig.I.46 (a). It consists of decoupling all the switching cells using high voltage ceramic capacitors of 68 nF rated at 1500 V (High voltage MLC chips flexitem 2225SC683KAZ1A). The impedance measurement of these capacitors shows good capacitive behavior at high frequencies reaching 10 MHz before its parasitic series inductance’s effect dominates (Fig.I.46 (b)).

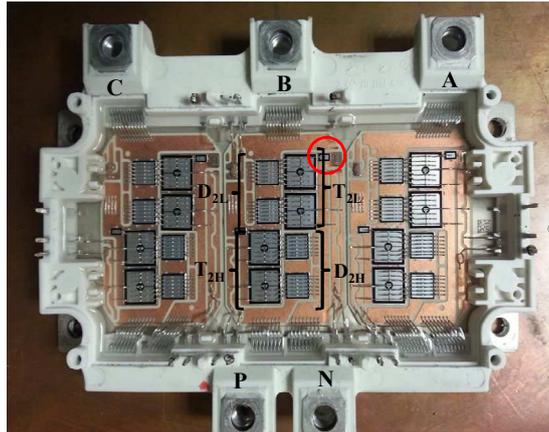


Fig.I.44. Study of a single bridge leg.

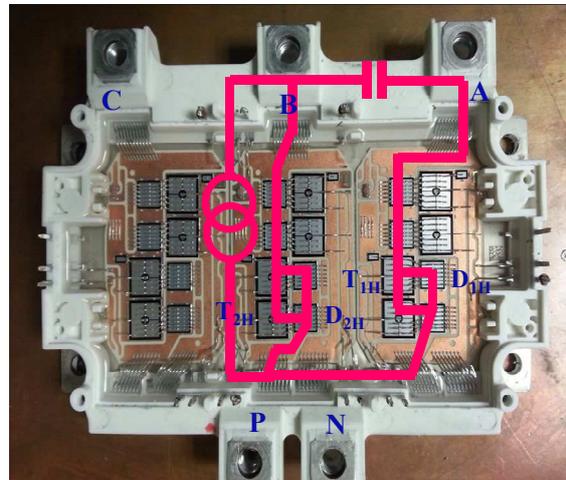
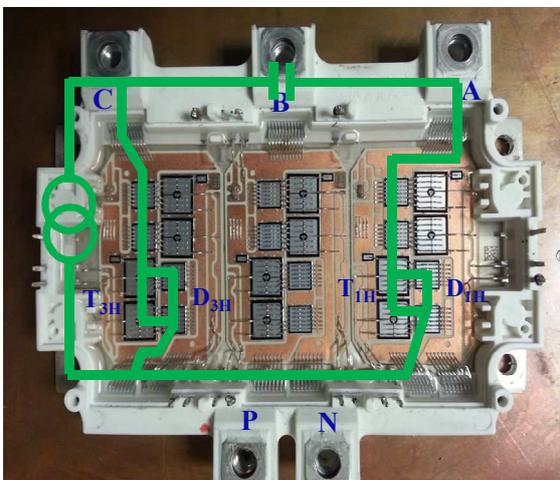


Fig.I.45. Representation of two commutation loops. (green) Between the high-side semi-conductors of bridge legs A and C. (pink) Between the high-side semi-conductors of bridge legs A and B.

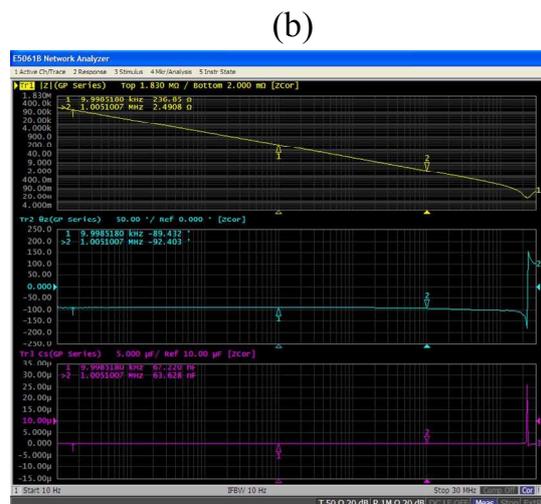
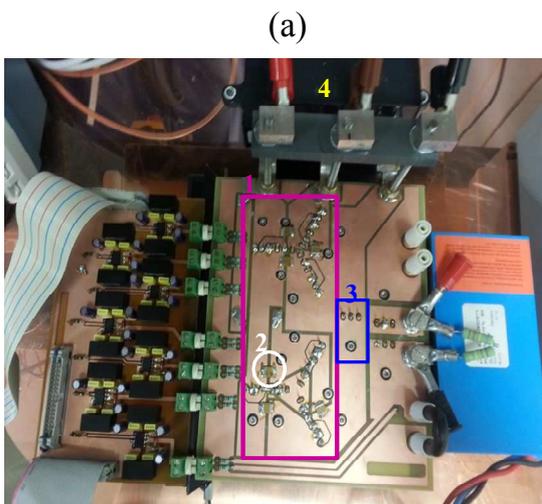


Fig.I.46. (a) Experimental power circuit of the optimized three-phase charger: 1- the three-phase CSAR, 2- Example of the placement of the decoupling capacitor, 3- Additional freewheeling diode and 4- Input filtering capacitors. (b) Impedance measurement of the decoupling capacitor.

The power circuit used to test the switching of MOSFET T_{IH} consists of a Buck converter setup. The Buck converter is formed between the MOSFET and the freewheeling diode (T_{IH} and D_{fw}).

In order to take into account the decoupling of the switching cell, the input dc voltage is placed as shown in Fig.I.47 (a). The equivalent electrical circuit is presented in Fig.I.47 (b).

The importance of including EMI constraints in the design phase of the CSAR is depicted in the experimental measurements presented in Fig.I.48. The amplitude of the resonance at turn off of the diode is linked to the remaining stray inductance of the commutation loop. Hence, it is important to detect the switching cells and decouple them.

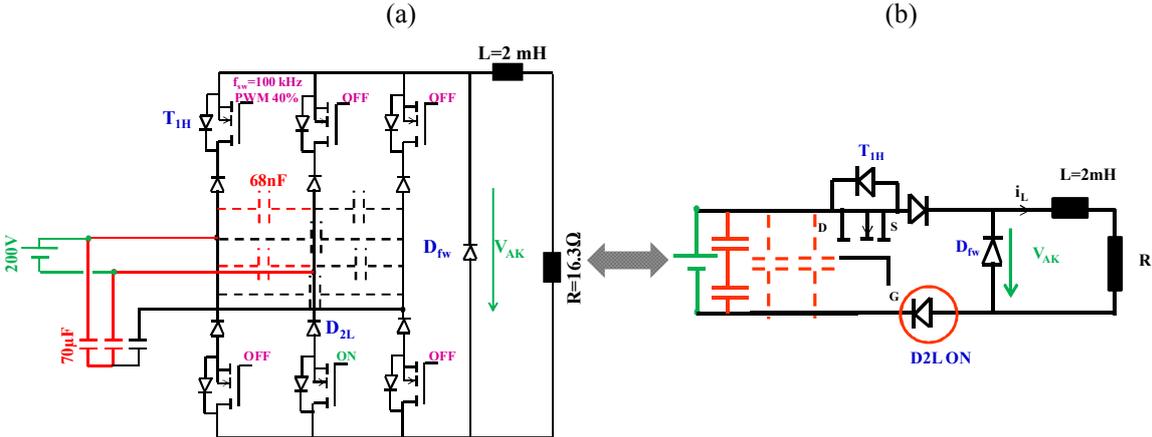


Fig.I.47. Power circuit of the prototype used to test the switching turn on and turn off of T_{IH} . (a) The input voltage (200 V) is placed at the normal input of the CSAR and takes into account the effect of the decoupling capacitors with a switching frequency of 100 kHz. (b) The equivalent electrical circuit of the switching cell.

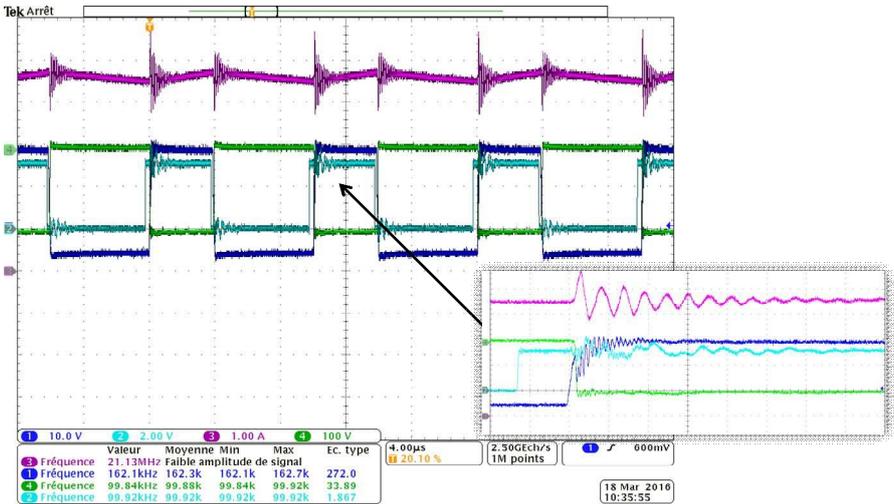


Fig.I.48. Experimental waveforms of the switching commutation of T_{IH} with decoupling capacitors: (blue) Measured gate-to-source voltage of T_{IH} . (cyan) T_{IH} 's binary PWM commands measured at the output of the DSP controller. (green) Voltage across the freewheeling diode V_{AK} . (magenta) Output current i_L .

8. Conclusion

This study has presented a complete and rigorous conducted EMI modeling technique used for CM and DM emissions prediction. It has been verified that the approach allows the modeling of the internal noise sources and propagation paths of a power electronics converter. It is a predictive approach based on the prior knowledge of the switch control law of the converter(s). Furthermore, it can be used either in time-domain or frequency-domain analysis. It has been applied to an on-board charger for EVs, in the single-phase and three-phase charging configurations, which verifies its chaining capability. Time-domain simulation results demonstrate the validity of the various developed models.

In addition, the model presented in this study uses trapezoidal waveforms to model the controlled sources. Experimental verification has been carried to justify this simplification with regards to the ultimate goal of designing an input EMI filter. The approach can be further refined by pushing the modeling degree to take into account the stray elements inherent to the semi-conductors and to define measuring techniques, performed on the test bench, that allow the identification of the propagation paths modeled by the admittance matrices of the conducted EMI models. These refinements should result in more realistic turn on/off switching waveforms for the controlled sources of the model. This would lead to an extended frequency range of validity; thus, giving the model a higher degree of precision in the prediction of conducted emissions.

The next step consists in using this proposed modeling approach in evaluating the impact that a topological or control modification has on the reduction (or increase) of the CM emissions as well as the effect it has, if any, on the DM currents. On the other hand, the derived models need low computational times and resources. Hence, they can be used in the design and sizing of an optimal input EMI filter.

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Chapter 2

Mitigation of the Conducted Emissions

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Passive EMI filtering along the propagation path has always been the go-to solution for power electronics designers. Once the prototype is built, a series of high frequency (150 kHz - 30 MHz) emission levels' measurements are conducted and compared to the levels recommended by the standards (IEC 61000-6-3: Electromagnetic compatibility part 6-3, generic standards- emission standard for residential, commercial and light-industrial environments). The attenuations needed are then used to design an input/output EMI filter for the already-built converter. However, since the reduction of the conducted emissions was not taken into account during the design process, the attenuation levels needed are often high. Furthermore, the standards define the maximum value of touch currents (IEC 61851-21: Electric vehicle conductive charging system part 21, electric vehicle requirements for conductive connection to an ac or dc supply) which limits the maximum value of the capacitances for the line to ground capacitors used to filter the common mode currents. Therefore, in order to achieve the high attenuation levels required with this limitation, the filtering inductors' values increase and lead to a bulky and costly filter usually consisting of multiple filtering stages.

The charger being studied suffers from a similar design process leading to a high-volume input EMI filter. For that reason, this Chapter aims to optimize both the topology as well as the switch control laws of the charger in order to reduce the common mode emissions. Thus, before designing a new input filter, modifications are going to be proposed along the propagation path and at the noise source so that the EMI analysis can take part of the design process.

1. State of the art : mitigation techniques for power electronics converters

This section provides a comprehensive review of the conducted EMI mitigation methods presented in literature for switch-mode power supplies. The reduction of the conducted emissions can take place either at the noise generation level or along the propagation path. This leads to a two branch classification that has been introduced by [Mainali et al. 2010] and has been completed by this study's own research (Fig.II.1).

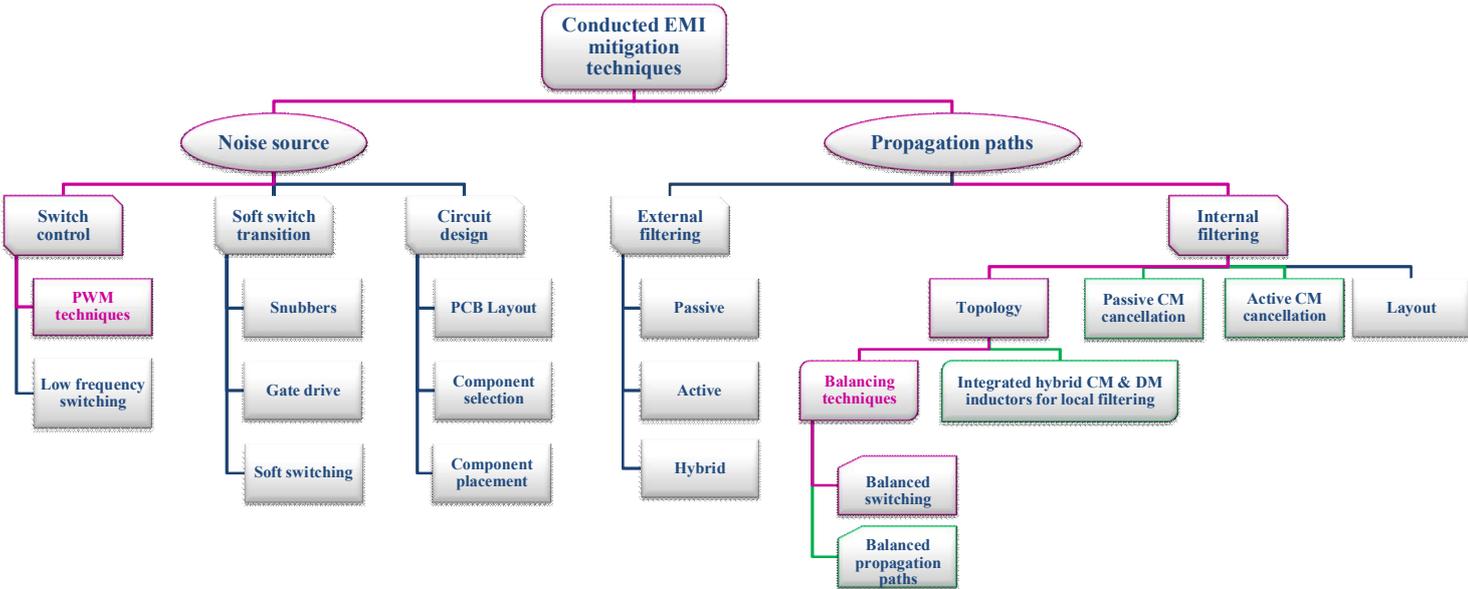


Fig.II.1. Classification of conducted EMI mitigation techniques. (Pink) Methods on which are based the modification proposed in this study, (Green) Categories considered for future improvements.

Furthermore, the conducted EMI reduction methods either rely on switch control approaches or power circuit design modifications. The categories defined are flexible and some techniques belong to more than one sub-category. It is also possible to combine two or more methods in order to come up with a hybrid mitigation approach.

Some of the techniques identified are not going to be applied to the EV charger being studied. In fact, this work is subjected to industrial constraints including cost reductions, volume minimization and safety requirements. Therefore, the mitigation techniques are analyzed according to their compliance with the application's needs; i.e. minimalistic hardware changes.

The external filtering branch is not investigated at this stage of the study. It is assumed that the CM emissions need to be reduced before resorting to external passive & / or active EMI filtering. This consideration is made with the aim of reducing the size and the rating of the passive and the active components respectively.

In addition, the branches corresponding to the soft switch transitions, the circuit design and the internal filtering through layout design will not be examined any further. As a matter of fact, the charger being optimized has already been manufactured and deployed. Therefore, minimal cost modifications require that the analysis takes place at the system and the control levels without intervening at the micro hardware levels. It should be pointed out that areas for improvement in these branches are the subjects of numerous studies such as [Karvonen 2011] for active gate control, [Zhu 2014] and [Basu 2006] for PCB layout considerations, and [Hoene et al. 2007], [Stube et al. 2008] - [Lissner et al. 2007] and [De Oliveira et al. 2010] for the effect of passive components placement on the EMI behavior.

Accordingly, the techniques that are adapted to our study belong to the highlighted sub-categories. Our proposed modifications are based on the categories highlighted in pink; however, the green categories constitute the basis of possible future improvements.

1.1. Conducted EMI mitigation along the propagation paths: Internal filtering

The EV charger consists of a three-phase CSAR followed by a dc-dc Boost converter. The CSAR must fulfill two functions: rectification and step-down of the input voltage. Therefore, the mitigation solutions chosen from the literature are mainly affiliated with the dc-dc Buck and Boost converters. It is assumed that a good knowledge of the CM emission mechanisms in these topologies will allow for a deeper comprehension of the charger's CM generators and propagation paths.

The techniques are presented and followed by our study's own interpretation. It is oriented towards the analysis of the voltage fluctuations at critical nodes identified for the EV charger; such as the switching cells' midpoints and the load's (i.e. battery) negative dc rail.

It is worth mentioning that very few conducted CM mitigation solutions were found for three-phase converters and back-to-back converters.

1.1.1. *Balanced switching techniques for power electronics converters*

This technique consists of well-thought topological changes made to the power converter's circuit in order to ensure a balanced switching. The modifications should reduce the converter's HF CM conducted emissions without affecting its LF behavior.

A- Application to the DC/DC Boost converter

The power circuit of a conventional dc/dc Boost converter is given in Fig.II.2 (a). The aim is to study the effects of circuit balancing on the common mode current emissions. Thus, the parasitic elements specific to the semi-conductors connected to fluctuating nodes, such as the switching cells' midpoints, are illustrated. In addition, the load can present its own parasitic capacitance C_D with regards to the chassis. The switches $\{T, D_H\}$ have complementary switching states in continuous current conduction mode and form a switching cell that has the node A as midpoint. Table II. 1 resumes the voltages across the parasitic capacitances formed at nodes A, B and D for different switching states.

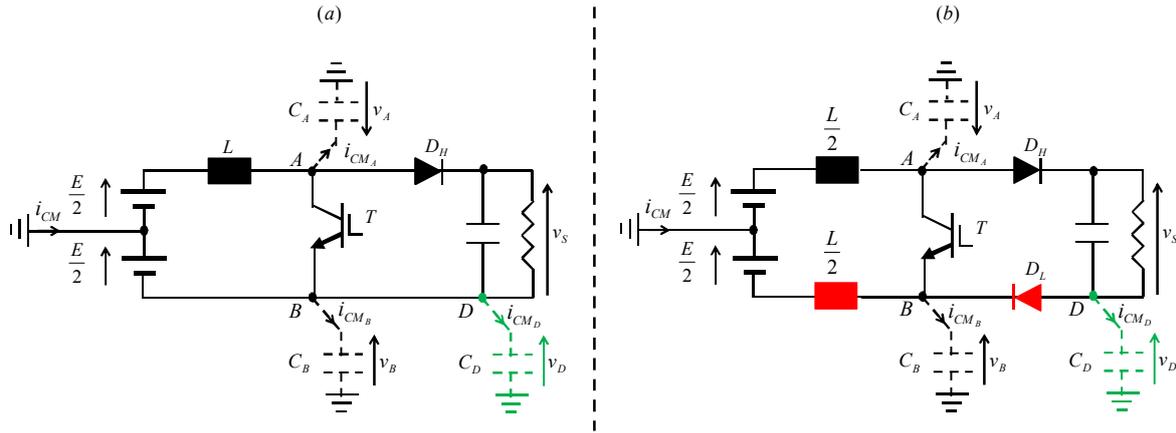


Fig.II.2. (a) Power circuit of a conventional dc-dc Boost converter with parasitic elements. (b) Boost converter's modified topology for CM voltage reduction.

Table II. 1. VOLTAGES ACROSS THE PARASITIC CAPACITANCES OF A CONVENTIONAL BOOST CONVERTER

Switching states	Voltages across parasitic capacitances		
	$v_A (V)$	$v_B (V)$	$v_D (V)$
T ON & D_H OFF	$-\frac{E}{2}$	$-\frac{E}{2}$	$-\frac{E}{2}$
T OFF & D_H ON	$v_S - \frac{E}{2}$	$-\frac{E}{2}$	$-\frac{E}{2}$
Voltage variations Δv	$\pm v_S$	0	0

Table II. 2. VOLTAGES ACROSS THE PARASITIC CAPACITANCES OF A BALANCED BOOST CONVERTER

Switching states	Voltages across parasitic capacitances		
	$v_A (V)$	$v_B (V)$	$v_D (V)$
T ON & $\{D_H, D_L\}$ OFF	0	0	$\frac{v_S}{2}$
T OFF & $\{D_H, D_L\}$ ON	$\frac{v_S}{2}$	$-\frac{v_S}{2}$	$\frac{v_S}{2}$

Switching states	Voltages across parasitic capacitances		
	$v_A (V)$	$v_B (V)$	$v_D (V)$
Voltage variations Δv	$\pm \frac{v_S}{2}$	$\mp \frac{v_S}{2}$	0

It can be deduced that the voltage across parasitic capacitances C_B and C_D maintains the same value during the operation of the converter while the voltage across parasitic capacitance C_A fluctuates constantly at the switching frequency and the value of each variation is dependent on the output voltage as such: $\pm v_s$. Knowing that the output voltage v_s is higher than the input voltage E , the voltage fluctuations are important. This translates into a common mode current generated by the Boost's switching cell and given by eq. (II. 2).

In order to reduce the common mode emissions of the Boost converter, [Shoyama et al. 2003] propose a new topology for the converter based on the structural balancing technique. It consists in mirroring the diode D_H on the other bus by adding a new diode D_L in the path of the returning current as shown in Fig.II.2 (b). The addition of this diode does not affect the LF behavior of the converter. In fact, it shares the same switching states as D_H and complementary states with switch T.

$$\begin{cases} i_{CM_A} = C_A \cdot \frac{dv_A}{dt} \neq 0 \\ i_{CM_B} = C_B \cdot \frac{dv_B}{dt} = 0 = i_{CM_D} \end{cases} \quad \text{eq. (II. 1)}$$

$$i_{CM} = i_{CM_A} + i_{CM_B} + i_{CM_D} = C_A \cdot \frac{dv_A}{dt} \neq 0 \quad \text{eq. (II. 2)}$$

In addition, the inductor is split into two inductors of equal inductance value; each of which is placed on one side of the DC bus. In order to maintain the LF behavior of the converter intact, the split inductors need to maintain the total value of inductance seen by the DM current flowing through the circuit. Hence, the split inductor allows dissociating the node B from the input voltage and the additional diode dissociates the output from the switching cells. Therefore, the modified Boost converter presents two switching cells $\{T, D_H\}$ & $\{T, D_L\}$ having nodes A and B as midpoints.

Table II. 2 shows the voltage fluctuations at these nodes; it can be seen that node B fluctuates by the same amount but in an opposite polarity to the voltage at node A. Furthermore, the voltages fluctuate by half of the amount present in a conventional Boost converter. However, it should be noted that the values presented in this Table are true if an equal voltage distribution amongst the diodes is assumed when they are both turned off.

Furthermore, it is shown that these modifications do not affect the CM behavior of the converter's output load. In fact, the voltage across the load's stray capacitance is independent from the fluctuations linked to the switching cells. The applied modifications allow changing the dependency of the voltage across the load's stray capacitance from the input and shifting it towards the output voltage. It takes on a different value than in the conventional Boost converter; however, it remains invariant with regards to the switching states. Hence, the common mode current generated by the balanced structure eq. (II. 4) is highly reduced with regards to the conventional Boost converter's common mode current found in eq. (II. 2). In addition, symmetrical structures minimize the effects of mixed mode EMI noise. Experimental results show an effective reduction of the CM conducted emissions by at most 20 dB from 150 kHz to 15 MHz.

$$\begin{cases} i_{CM_A} = C_A \cdot \frac{dv_A}{dt} \neq 0 & \uparrow \downarrow \\ i_{CM_B} = C_B \cdot \frac{dv_B}{dt} \neq 0 & \downarrow \uparrow \\ i_{CM_D} = C_D \cdot \frac{dv_D}{dt} = 0 \end{cases} \quad \text{eq. (II. 3)}$$

$$i_{CM} = i_{CM_A} + i_{CM_B} + i_{CM_D} = (C_A - C_B) \cdot \frac{dv_A}{dt} \quad \text{eq. (II. 4)}$$

On the other hand, the split inductor can consist of either two separate inductors placed on both DC buses with equal inductance value, or two coupled inductors sharing the same magnetic core as illustrated in Fig.II.3 (a). For the same total inductance value, magnetically coupled inductors present the advantages of reduced volumes and balanced HF parasitic elements (equivalent parallel capacitance and resistance) compared to their decoupled counterparts (Fig.II.3 (b)).

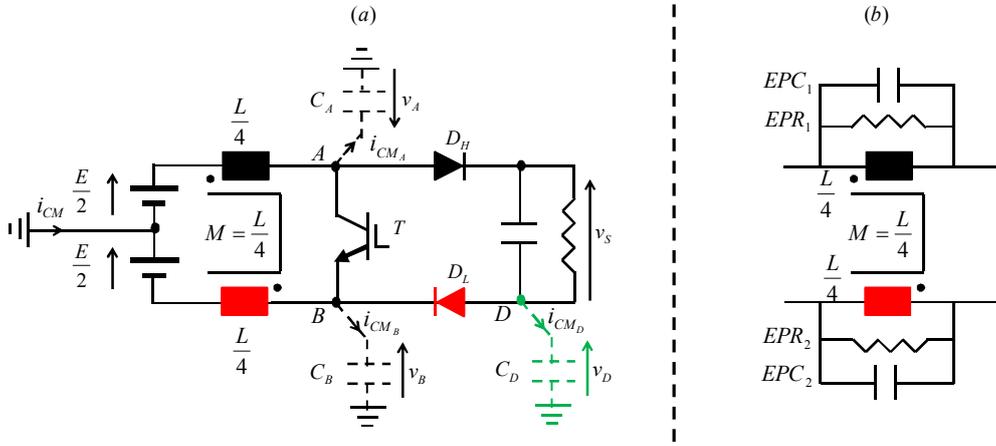


Fig.II.3. (a) Boost converter's modified topology with a coupled DM inductor. (b) Two coupled inductors to balance the HF parasitic.

B- Application to the DC/DC Buck converter

The power circuit of a dc/dc Buck converter is given in Fig.II.4 (a). Table II. 3 resumes the voltages across the parasitic capacitances formed at nodes A, B and D for different switching states.

It can be deduced that the voltage across parasitic capacitances C_B and C_D maintains the same value during the operation of the converter while the voltage across parasitic capacitance C_A fluctuates constantly at the switching frequency and the value of each variation is of $\pm E$. This translates into a global common mode current generated by the Buck's switching cell and given by eq. (II. 5).

$$i_{CM} = i_{CM_A} + i_{CM_B} + i_{CM_D} = C_A \cdot \frac{dv_A}{dt} \neq 0 \quad \text{eq. (II. 5)}$$

[Wittenbreder 2003] presents a new Buck converter design for common mode noise reduction based on a patented method for the synthesis of power conversion circuits. However, the technique requires three coupled windings and a special disposition of the switching elements. It works for simple dc-dc converters; nonetheless it is less obvious to implement for back-to-back topologies sharing the same

dc link. Therefore, it is not considered any further. In order to reduce the common mode emissions of a Buck converter, [Rockhill et al. 1998] propose a new topology for the converter based on the balanced switching technique. It consists in mirroring the transistor T_H on the other bus by adding a new transistor T_L in the path of the returning current as shown in Fig.II.4 (b).

$$i_{CM} = i_{CM_A} + i_{CM_B} + i_{CM_D} = (C_A - C_B) \cdot \frac{dv_A}{dt} \quad \text{eq. (II. 6)}$$

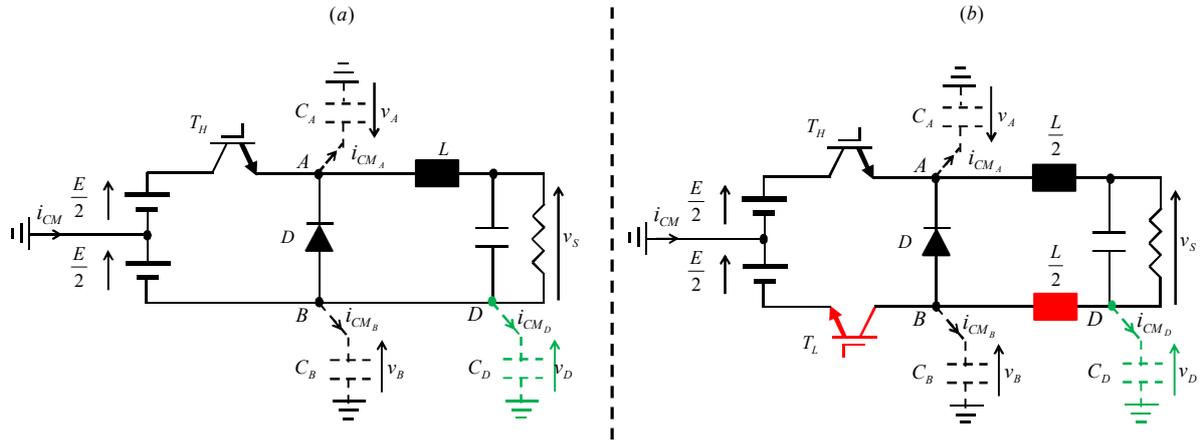


Fig.II.4. (a) Power circuit of a typical dc-dc Buck converter with parasitic elements. (b) Buck converter's modified topology for global CM voltage reduction.

Table II. 3. VOLTAGES ACROSS THE PARASITIC CAPACITANCES OF A CONVENTIONAL BUCK CONVERTER

Switching states	Voltages across parasitic capacitances		
	$v_A(V)$	$v_B(V)$	$v_D(V)$
T_H ON & D OFF	$\frac{E}{2}$	$-\frac{E}{2}$	$-\frac{E}{2}$
T_H OFF & D ON	$-\frac{E}{2}$	$-\frac{E}{2}$	$-\frac{E}{2}$
Voltage variations Δv	$\mp E$	0	0

Table II. 4. VOLTAGES ACROSS THE PARASITIC CAPACITANCES OF A GLOBALLY BALANCED BUCK CONVERTER

Switching states	Voltages across parasitic capacitances		
	$v_A(V)$	$v_B(V)$	$v_D(V)$
$\{T_H, T_L\}$ ON & D OFF	$\frac{E}{2}$	$-\frac{E}{2}$	$-\frac{v_s}{2}$
$\{T_H, T_L\}$ OFF & D ON	0	0	$-\frac{v_s}{2}$
Voltage variations Δv	$\mp \frac{E}{2}$	$\pm \frac{E}{2}$	0

In order for the LF behavior of the converter to remain the same, switch T_L receives the same control commands as T_H . Therefore, it shares complementary states with diode D and they both form a new switching cell that has the node B as midpoint. By applying the same analysis as for the Boost converter, the need to split the inductor emerges (Fig.II.4 (b)). Table II. 4 shows the voltage fluctuations according to the switching states. It can be verified that splitting the inductor leads to the stabilization of the voltage across C_D and to reducing the global CM emissions generated by the Buck converter and its load (eq. (II. 6)).

So far, equal distribution of the voltage across the turned-off switches has been assumed. However, there are no guarantees as to the degree to which they will share the voltage. This is due to static as well as dynamic voltage unbalances. These are linked to the device parameter tolerances such as the gate drives tolerances that might give rise to differing switching speeds. In [Rockhill et al. 1998], examples of snubber circuits are proposed in order to force the switches to share the voltage evenly and ensure an optimal CM current compensation. In all cases, if no measures are taken, the CM current compensation remains effective but not to an optimal degree.

1.1.2. *Balanced propagation paths technique for converters: Application to the Boost*

This concept is based on the detection of the main noise sources in a power electronics converter and the propagation paths associated to each of them. It is shown in [Wang et al. 2007-1st] - [Wang et al. 2010] that the resultant networks formed by the propagation paths resemble a Wheatstone bridge. Hence, by balancing the Wheatstone bridges, one can balance the noise sources' propagation paths and reduce the CM emissions.

For instance, the general balance technique is going to be applied to the propagation paths of a conventional dc-dc Boost converter with a LISN connected at its input (Fig.II.5 (a)). The equivalent simplified noise model of this converter is shown in Fig.II.5 (b), where the switch T is considered as the noise source. The common mode currents are deduced based on the voltages across the parasitic capacitances presented in Table II. 1. This noise model representation is equivalent to an unbalanced Wheatstone bridge; which corroborates why a CM current flows through the LISN's impedances.

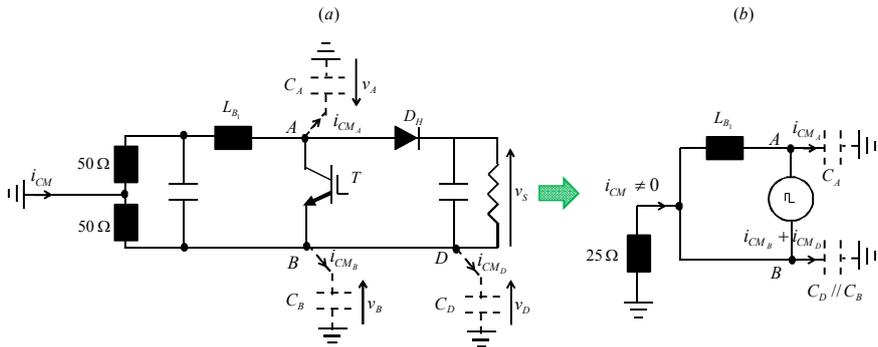


Fig.II.5. (a) Power circuit of a conventional Boost converter with parasitic elements and input LISN. (b) Conventional Boost converter's noise model is an unbalanced Wheatstone bridge.

In order to reduce the CM current in the LISN, one should try to balance the Wheatstone bridge. Therefore, two choices can be made. On one hand, one could choose to split the inductance equally on both DC buses (Fig.II.6). In this case, in order to balance the Wheatstone bridge, physical capacitors can be added at nodes A and B to ensure the balance condition presented in eq. (II. 7).

$$\frac{Z_{L_{B1}}}{Z_{L_{B2}}} = \frac{Z_{C_A // C_1}}{Z_{C_B // C_D // C_2}} = 1 \quad \text{eq. (II. 7)}$$

On the other hand, one can choose not to add physical capacitors. In this case, the inductances should be split according to the ratio of the parasitic capacitances presented in eq. (II. 8).

$$\frac{Z_{L_{B1}}}{Z_{L_{B2}}} = \frac{Z_{C_A}}{Z_{C_B // C_D}} \quad \text{eq. (II. 8)}$$

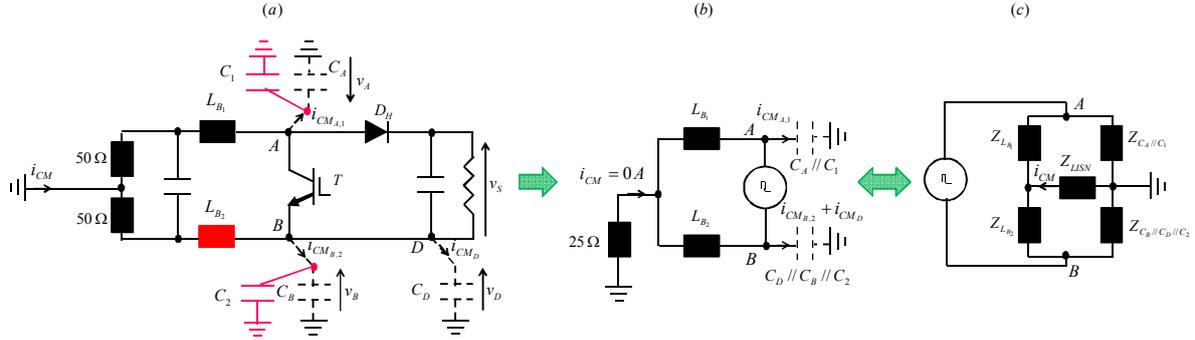


Fig.II.6. (a) Power circuit of a Boost converter balanced along the propagation paths of the CM emissions. (b) Balanced Boost converter's simplified noise model. (c) Equivalent balanced Wheatstone bridge.

This solution is interesting to incorporate during the design phase of the converter. However, it requires a detailed knowledge of the propagation paths and a good estimation / measurement of the parasitic capacitances. Therefore, it is easier to implement on simple topologies formed by a minimum number of switching cells.

It is interesting to note that by combining the balanced propagation paths technique with the previously developed balanced switching technique, the common mode current generated by the dc-dc Boost and Buck converters (in eq. (II. 4)) and eq. (II. 6)) can be further reduced by adding capacitors to balance the ratio of the parasitic capacitances \$C_A\$ and \$C_B\$.

1.1.3. Integrated hybrid CM & DM inductors

The mitigation of the frame ground leakage current is an important challenge during the design of grid-connected power converters such as on-board EV chargers. The ideal configuration is to be able to confine the CM emissions of the charger.

On one hand, this is usually achieved, after the prototype is built, by using common-mode chokes in the design of the input EMI filter. However, without further measures to reduce the CM emissions, the resulting CM chokes are voluminous. In addition, the most common practice consists of using separate CM and DM filtering stages. In recent years, high power density became intensely required for power electronics converters (Google's little box challenge launched in 2016 led to the design of a 2 kW inverter with a power density of 8850 W/liter [CE+T 2016]). Therefore, designers started working on the minimization of the volume of the ac side input EMI filter. One way to achieve this is to combine the CM choke and the input DM filtering inductor into a single component.

On the other hand, solutions have been proposed at the design stage of the converter in order to reduce the CM emissions seen by the input. This is done by creating local CM filtering on the dc side of the converter. Hence, the typical dc link choke is replaced by an integrated dc choke having CM voltage suppression capabilities. The choke produces two inductances, one for differential current ripple reduction and the other for CM voltage suppression.

Whether the EMI filter’s CM choke is combined with DM filtering at the input ac side or the dc link choke is combined with local CM suppression at the dc side, this will be referred to as the hybrid integration of DM & CM inductors into a single component. Hence, we propose to classify the different hybrid integration methods found in literature into three sub-categories according to the methodologies used in their design (Fig.II.7): structural integration, magnetic integration and leakage flux management.

Magnetic integration consists of a magnetic core on which both differential and common-mode windings are placed. Leakage flux management relies on increasing the leakage inductance of CM chokes in order to increase their series differential mode inductance [Cocquerelle 1999]. Structural integration consists of partly / totally sharing the windings over two distinct magnetic cores (one for CM suppression and the other for DM suppression).

Designs for the magnetic integration of DM & CM chokes on the dc link of motor drive applications can be found in[Wu et al. 2001], [Wu et al. 2006], [Xiao et al. 2012], [Chen et al. 2012], [Sodo 2008] and [Hammond 1999].

AC-side integrated hybrid CM & DM chokes are resumed according to their design principle in Table II. 5.

Among other advantages, integrating the CM & DM chokes is especially interesting for volume minimization. However, the integrated inductances require special industrialization processes which are more costly than improving the CM emissions via control schemes and low cost topological modifications.

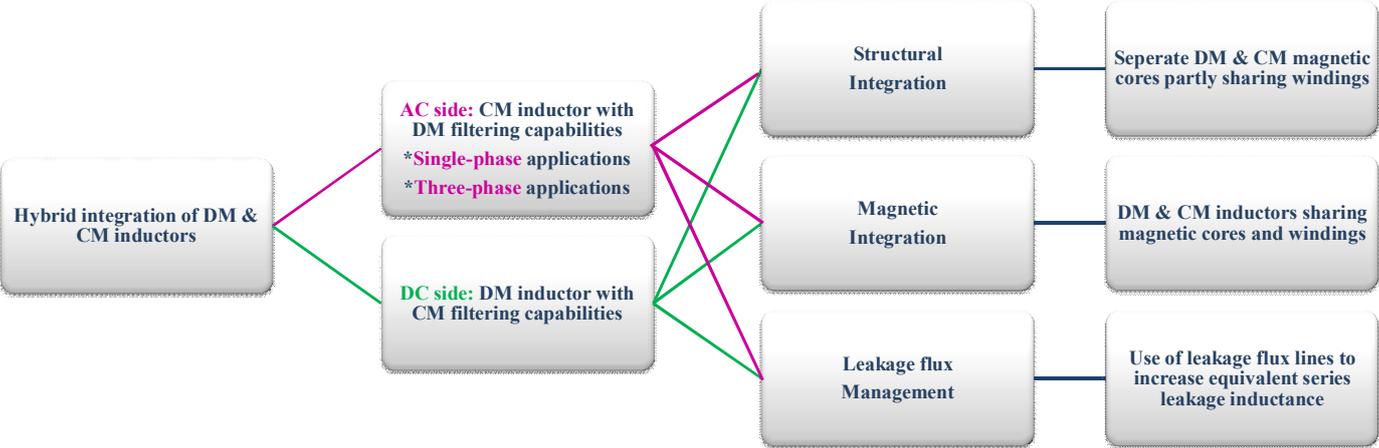


Fig.II.7. Classification of the hybrid integration methods for CM & DM inductors.

Table II. 5. CLASSIFICATION OF DESIGNS FOUND IN LITERATURE FOR THE AC SIDE INTEGRATED HYBRID CM & DM CHOKES

AC side EMI filters with hybrid CM & DM integrated inductors					
Three-phase applications			Single-phase applications		
Magnetic integration	Leakage flux management	Structural integration	Magnetic integration	Leakage flux management	Structural integration
[Zhu et al. 2012]	[Krause 2014]	[Kinnunen et al. 2013]	[Hedayati et al. 2016] [Umetani et al. 2014] [Tarateeraseth 2014] [Jeffries 1994] [Shudarek et al. 2011] [Fu et al. 2013] [Gilmore et al. 2004] [Upadhyay 1994]	[Hu et al. 2003] [Chu et al. 2015] [Tan et al. 2013]	[Yamaguchi et al. 1997] [Yamaguchi 1996] [Lai et al. 2010] [Nan et al. 2006]

1.1.4. Passive CM cancellation

Several passive conducted CM noise cancellation techniques have been studied in literature. The ones chosen to be developed are the ones deemed to be applicable to the charger's topology (i.e. back to back converters and current source active rectifiers). The main advantage of internal filtering is that the modifications take place on the dc-side of the converter. This automatically renders them valid for both types of charging configurations: single-phase and three-phase.

A- Passive compensation circuit

The most common method consists of using an extra winding coupled to the power circuit's inductor and a capacitor to inject a CM current in opposition to the one generated at the switching cell's midpoint. We are going to apply the cancellation principle studied by [Cochrane et al. 2003], [Wang et al. 2007-2nd] and [Xin et al. 2000] to the dc-dc Buck and Boost converters.

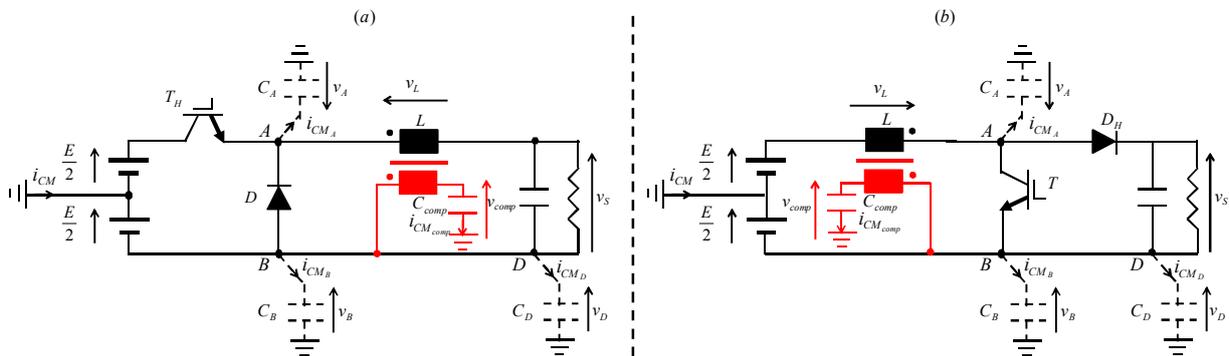


Fig.II.8. Passive compensation circuit applied to the conventional: (a) dc-dc Buck converter; (b) dc-dc Boost converter.

If we take the example of the conventional Buck converter, the voltage fluctuations at the switching cell's midpoint A are given in Table II. 3. No voltage variation is depicted at nodes B and D, which

are dependent on the input voltage. Therefore, the parasitic capacitance C_A is the major source of CM current emissions. The idea behind this mitigation method is to use an extra winding, coupled to the circuit's filtering inductor that generates a 180° out of phase voltage waveform across the added compensation capacitor C_{comp} (Fig.II.8 (a)). The compensation voltage across this capacitor v_{comp} replicates the opposite of the dv/dt seen across the switching cell's parasitic capacitor C_A . The voltages fluctuating in opposition are shown in Table II. 6 for $C_{comp}=C_A$ and for the same number of turns used for the extra winding and the inductor. The CM current's expression is given in eq. (II. 9).

Table II. 6. VOLTAGES AT CRITICAL NODES OF A BUCK CONVERTER WITH A PASSIVE CONDUCTED CM COMPENSATION CIRCUIT

Switching states	Voltages across the parasitic capacitance and the compensation capacitor	
	$v_A(V)$	$v_{comp}(V)$
T_H ON & D OFF	$\frac{E}{2}$	$-\frac{3E}{2} + v_s$
T_H OFF & D ON	$-\frac{E}{2}$	$-\frac{E}{2} + v_s$
Voltage variations Δv	$\mp E$	$\pm E$

The added winding and capacitor are sized for the CM current emissions and do not affect the LF operation of the converter. The same can be applied to the conventional Boost circuit Fig.II.8 (b). However, in case of cascaded converters sharing the same inductive dc link (such as the charger being studied), the passive compensation circuits become more complex. This method is particularly interesting for isolated converters because it can make use of the isolation transformer to add the compensation circuit.

$$i_{CM} = i_{CM_A} + i_{CM_{comp}} = (C_A - C_{comp}) \cdot \frac{dv_A}{dt} \quad \text{eq. (II. 9)}$$

B- Capacitive connection between the output and the input

Another technique can be used for the internal filtering of the conducted CM currents. It consists in creating a physical connection between the center point / star-point of the capacitive elements present at the output dc / ac bus of the converter and the star-point of the DM filtering capacitors of the input EMI filter. The capacitive connection from the output to the input creates an alternative path for some of the CM currents to return to their source. In addition, it contributes to the reduction of the levels of the leakage currents and to lowering the filtering efforts. However, this design requires special attention in order to avoid the saturation of the CM inductors. This method, including the sizing of the output capacitors and the input filter, has been detailed and applied to three-phase systems such as the voltage source rectifiers [Hartmann 2011], the back-to-back converter based motor drives [Hu et al. 2013] - [Hedayati et al. 2013] - [Zhu et al. 2012] - [Qi et al. 2013] and the current source rectifiers [Soeiro et al. 2013] - [Nussbaumer et al. 2006] - [Heldwein 2008] as shown in Fig.II.9.

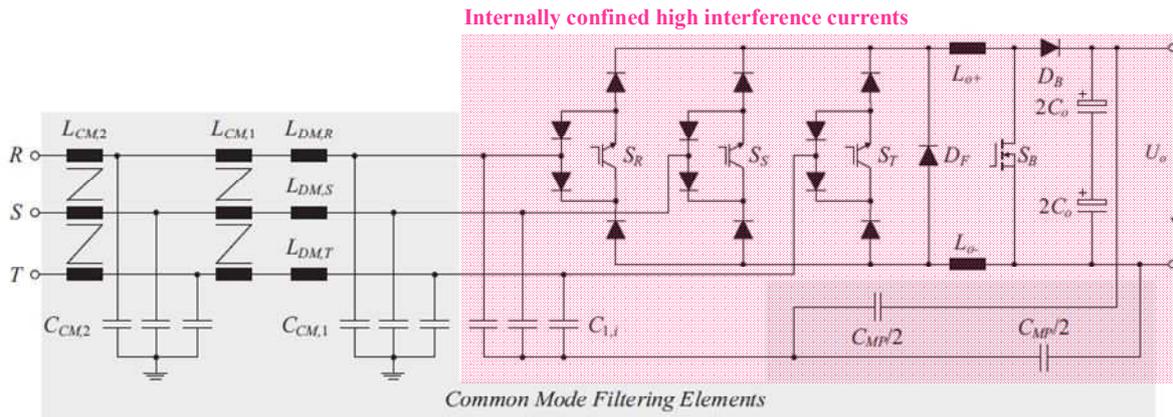


Fig.II.9. Power circuit of a three-phase PWM current source rectifier with an input EMI filter presenting an internal capacitive connection [Heldwein 2008].

In the case of the EV charger, if no measures are taken, the large CM component of the output voltage (i.e. at the battery's terminals) will cause high CM currents to flow towards the frame ground. A connection between the output dc bus' voltage midpoint and the star-point of the DM filtering capacitors could significantly reduce the CM component of the output voltage without violating the safety regulations regarding the maximum tolerated 3.5 mA RMS for the leakage currents [Hartmann 2011].

1.1.5. Active CM cancellation

The methods identified in this category can be further classified into two sub-categories: active linear compensation and solutions based on added power electronics components and their control.

The first sub-category consists of operational amplifier based solutions that have been thoroughly studied by [Vermaelen 2012] - [Schmenger et al. 2015]. It consists in the measurement of the CM voltage generated by the converter followed by its amplification by means of an operational amplifier. The resulting signal is then injected in opposition with the CM voltage generated by the converter. The topology of the converter is not modified; however, an auxiliary active compensation circuit is added to the circuitry.

The second sub-category consists of topological modifications (usually it consists of added power electronics switching components) made to the power circuit associated to specific control schemes in order to ensure the reduction of the CM voltage generated by the converters. An example of the application of this method to a three-phase three-level voltage source inverter is given by [Dagan et al. 2016]. Solutions that are related to the EV charger's topology are presented by [Klumpner et al. 2005] and [Aziz et al. 2007] for the three-phase CSAR. They consist in adding 8 switches on the dc-side of the converter to reduce the dv/dt of the output CM voltage during the application of the zero state vectors (Fig.II.10 (a)).

On the other hand, an idea was found in literature for the minimization of the voltage ripple at the output of a single-phase CSAR as illustrated by Fig.II.10 (b) [Zapata et al. 1998]. However, we believe that by adapting the control scheme of the three legs, it may be transformed into a solution for the reduction of the CM voltage in the single-phase configuration. It could be directly applied to the EV charger since in the single-phase configuration the third rectifier leg is disconnected from the grid. Hence, it becomes connected to the center-point of two input capacitors via the third DM capacitor.

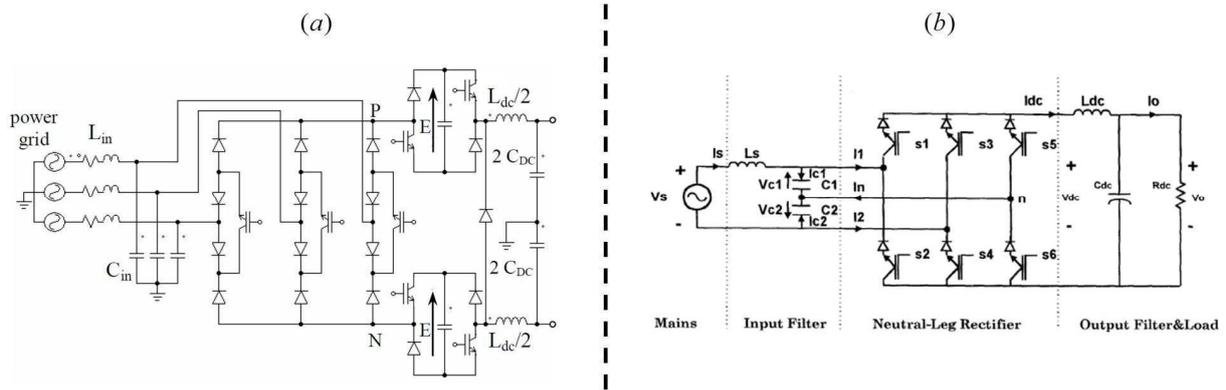


Fig.II.10. Active CM cancellation by added power electronics switches. (a) dc-side solution for the compensation of the CM voltage due to zero vectors in three-phase SVPWM schemes [Klumpner et al. 2005]. (b) Single-phase solution by the use on an extra rectifier leg connected to the center point of the input DM capacitors [Zapata et al. 1998].

There are a number of limitations to the presented active methods of noise cancellation such as the added cost of additional power switching semi-conductors and their associated gate drives and control circuits as well as the reliability of linear active compensation circuits.

1.2. Conducted EMI mitigation techniques at the noise source level : switch control PWM

This category only deals with the three-phase charging configuration for which the CSAR is controlled via space vector PWM techniques. Several random and spread spectrum PWM techniques are studied in literature; however, we choose to focus on the modulation schemes that effectively reduce the conducted CM emissions without spreading the spectrum in order to pass the standardized testing.

Most of the modulation strategies, that minimize the common mode voltage, are found in literature for the two-level voltage source inverter (VSI). Since the principle of the modulation strategies applied to the three-phase VSIs is easier to comprehend, we will start by exposing some of the most known techniques of common mode voltage (CMV) reduction for VSIs. Afterwards, the mechanism of the generation of high dv/dt in three-phase current rectifiers, controlled via space vector modulation, is going to be exposed. It is followed by a review of the CMV reduction modulation strategies found in the literature for three-phase CSARs.

1.2.1. CMV reduction modulation techniques for the two-level three-phase VSI

A- CMV in two-level three-phase VSIs

The power circuit of a conventional two-level three-phase VSI is given in Fig.II.11. The CMV is defined as the voltage between the star-point of the load and the power line ground v_{ng} . Since the variation of the voltage v_{og} is slow compared to v_{no} (varying at the switching frequency), the CMV can be written as follows:

$$V_{CM} = v_{ng} = v_{no} + v_{og} \cong v_{no} \quad \text{eq. (II. 10)}$$

With v_{no} being :

$$v_{no} = \frac{v_{ao} + v_{bo} + v_{co}}{3} \quad \text{eq. (II. 11)}$$

Several criteria need to be considered when designing a space vector modulation technique for the VSI, such as: the minimization of the output current ripple, the reduction of the dc link current ripple (plays a role in the sizing of the dc bus capacitor), the minimization of the switching losses, the CMV reduction... Therefore, several techniques can be found in literature. However, we choose to focus on the CMV reduction as the main criterion.

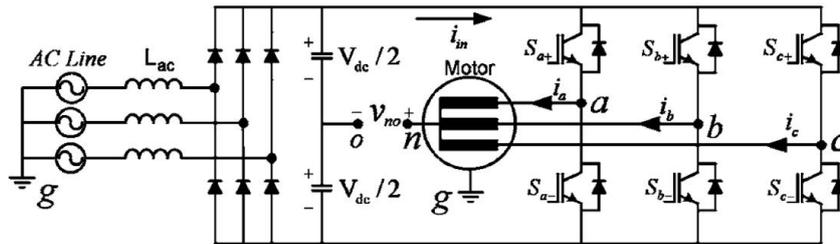


Fig.II.11. Power circuit of a two-level three-phase PWM VSI [Hava et al. 2009].

B- SVM techniques for CMV reduction for two-level three-phase VSIs

The conventional continuous PWM technique is the space vector PWM (SVPWM). It consists in utilizing both zero-voltage vectors V_0 and V_7 along with the active-state vectors adjacent to the desired output vector V_{ref} . The order of placement of the vectors inside the switching sequence is symmetrical and chosen so as to reduce the switching losses.

This modulation technique is illustrated in Fig.II.12 (a). It can be verified through the application of eq. (II. 11) that the odd active vectors V_1 , V_3 and V_5 generate a CMV equal to $-v_{dc}/6$; whereas the even active vectors V_2 , V_4 and V_6 generate a CMV equal to $+v_{dc}/6$. Furthermore, the zero-voltage vectors are responsible for the highest absolute values of CMV. In fact, V_0 generates a CMV of $-v_{dc}/2$ and V_7 leads to $+v_{dc}/2$. It can be deduced from the highlighted elements that this modulation strategy yields high CMV ($\pm v_{dc}/2$).

Thus, the idea behind the reduced CMV PWM techniques is to avoid the use of zero-voltage vectors inside a switching sequence. This would lead to a CMV that only takes up the values related to active vectors ($\pm v_{dc}/6$). Such techniques have been reviewed by [Cavalcanti et al. 2010] - [Hava et al. 2009] - [Hou et al. 2013]. They are identified with regards to the choice of the active vectors used.

➤ *Active Zero State PWM (AZSPWM)*: The desired output voltage is created using the adjacent active vectors. The latter are complemented with either two near opposing active vectors (AZSPWM1, AZSPWM2) or one of the adjacent state vectors and its opposite vector (AZSPWM3: V_1 V_2 V_4 V_2 V_1). The two opposing active vectors are applied for equal time durations to effectively create a zero-voltage vector (Fig.II.12 (b)).

➤ *Remote State PWM (RSPWM)*: The desired output voltage is synthesized from three active state vectors that share the same CM signature either (V_1 , V_3 , V_5) or (V_2 , V_4 , V_6). Several variants exist depending on the switching sequences chosen (Fig.II.12 (c)).

➤ *Near State PWM (NSPWM)*: The desired output voltage is synthesized from three active state vectors: two adjacent active state vectors, and a near-neighbor active vector is selected based on the location of the desired output voltage vector (Fig.II.12 (d)).

It is shown that by applying these modulation techniques, the peak value of the CMV can be greatly reduced.

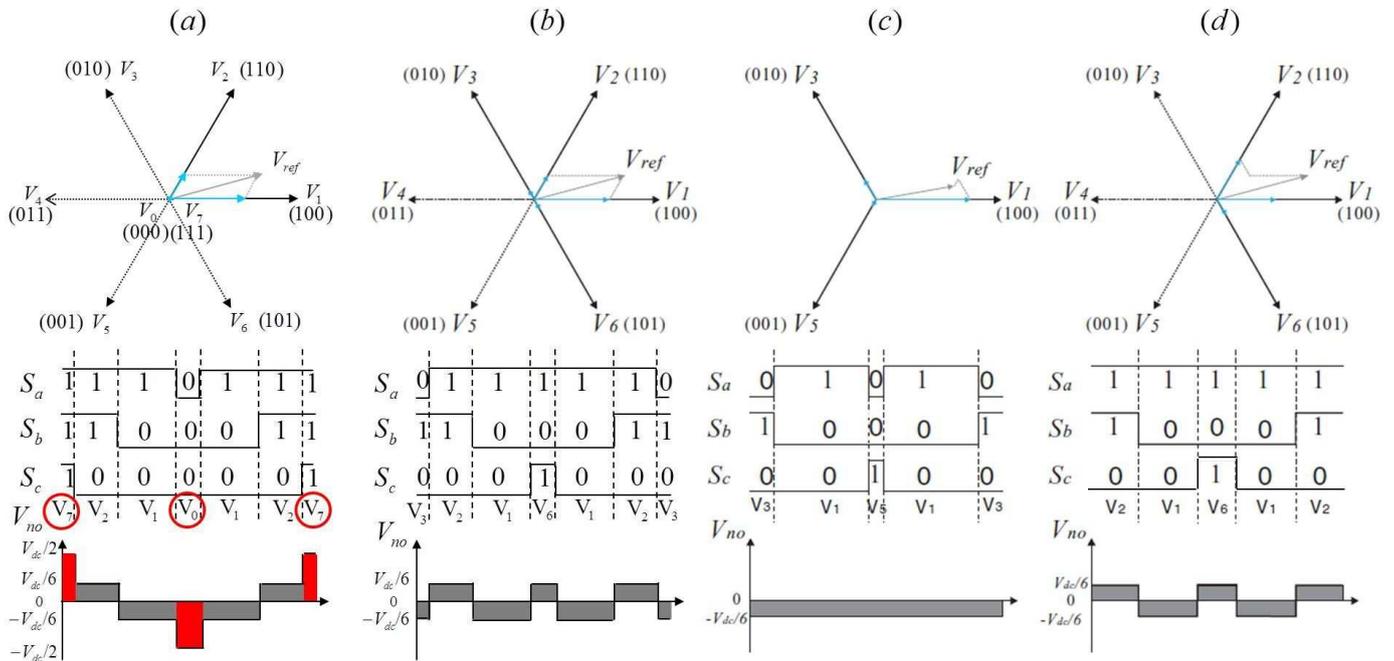


Fig.II.12. Various reduced common mode voltage PWM strategies applied to a reference vector in the first half of Sector I. (a) Conventional SVPWM. (b) AZSPWM1. (c) RSPWM3. (d) NSPWM. (b),(c) & (d) are taken from [Hou et al. 2013].

1.2.2. CMV reduction modulation techniques for the six-switch three-phase CSAR

The works that study the CMV reduction through modulation techniques for three-phase current source converters (CSC) are mainly related to CSC-fed motor drives consisting of a current source rectifier (CSR) placed back-to-back with a current source inverter (CSI). Furthermore, all the studies deal with a filtering inductor split onto both sides of the dc-link (Fig.II.13). This allows dissociating node 2 from node 4. Hence, the CSR imposes the voltage fluctuations at nodes 1 and 2, whereas the CSI determines the voltages at nodes 3 and 4.

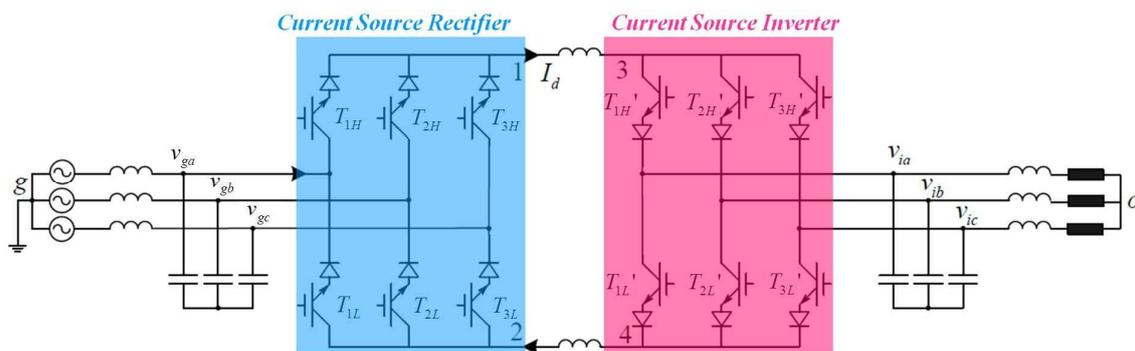


Fig.II.13. Power circuit of a CSC-fed motor drive [Guo et al. 2016].

A- CMV in three-phase CSC

The CMV produced at the output of the CSR is expressed as:

$$v_{CM_{rect}} = \frac{v_{1g} + v_{2g}}{2} \quad \text{eq. (II. 12)}$$

It can be written as a function of the input voltages and the CSR's switching functions as follows:

$$v_{CM_{rect}} = \frac{[(f_{T1H} + f_{T1L}) \quad (f_{T2H} + f_{T2L}) \quad (f_{T3H} + f_{T3L})]}{2} \cdot \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} \quad \text{eq. (II. 13)}$$

The same can be applied to the CMV generated at the input of the CSI:

$$v_{CM_{inv}} = \frac{v_{3o} + v_{4o}}{2} \quad \text{eq. (II. 14)}$$

It can be written as a function of the output voltages and the CSI's switching functions:

$$v_{CM_{inv}} = \frac{[(f_{T1H'} + f_{T1L'}) \quad (f_{T2H'} + f_{T2L'}) \quad (f_{T3H'} + f_{T3L'})]}{2} \cdot \begin{bmatrix} v_{ia} \\ v_{ib} \\ v_{ic} \end{bmatrix} \quad \text{eq. (II. 15)}$$

If the dc-link inductor is equally split onto both dc buses then:

$$v_{13} = v_{42} \quad \text{eq. (II. 16)}$$

Therefore, the global CMV of the motor drive system can be deduced:

$$v_{og} = v_{CM_{rect}} - v_{CM_{inv}} \quad \text{eq. (II. 17)}$$

Based on eq. (II. 13), the values of the CSR's CMV for the different space vectors (refer to Part A Chapter 2) is given in Table II. 7. By using eq. (II. 15), the same can be deduced for the CSI's CMV.

Unlike the VSI, the values taken by the CMV are not constant (i.e. proportional to the voltage of the dc-bus); however, they depend on the three-phase input voltages and vary at the grid's frequency.

Furthermore, in a given sector, it can be deduced that the absolute peak value of the CMV during the application of the zero vectors is twice as important as the absolute peak value of the CMV during the application of the active state vectors.

Table II. 7. CMV FOR THE CSR FOR DIFFERENT SWITCHING STATES

Space vectors	Switching States	$v_1 (V)$	$v_2 (V)$	$v_{12} (V)$	CMV (V)	
6 Active State Vectors	\vec{I}_1	f_{T1H} f_{T2L}	v_{ga}	v_{gb}	v_{gab}	$-v_{gc}/2$
	\vec{I}_2	f_{T1H} f_{T3L}	v_{ga}	v_{gc}	v_{gac}	$-v_{gb}/2$
	\vec{I}_3	f_{T2H} f_{T1L}	v_{gb}	v_{ga}	v_{gba}	$-v_{gc}/2$
	\vec{I}_4	f_{T2H} f_{T3L}	v_{gb}	v_{gc}	v_{gbc}	$-v_{ga}/2$
	\vec{I}_5	f_{T3H} f_{T1L}	v_{gc}	v_{ga}	v_{gca}	$-v_{gb}/2$
	\vec{I}_6	f_{T3H} f_{T2L}	v_{gc}	v_{gb}	v_{gcb}	$-v_{ga}/2$
3 Zero Vectors	\vec{I}_0	f_{T1H} f_{T1L}	v_{ga}	v_{ga}	0	v_{ga}
	\vec{I}_7	f_{T2H} f_{T2L}	v_{gb}	v_{gb}	0	v_{gb}
	\vec{I}_8	f_{T3H} f_{T3L}	v_{gc}	v_{gc}	0	v_{gc}

B- SVM techniques for CMV reduction for CSCs

Therefore, similar to the VSIs, the most common reduced CMV PWM techniques for CSCs avoid the use of the zero state vectors in the synthesis of the reference vector. [Zhu 2013] studies the application of the AZSPWM, the RSPWM and the NSPWM principles for the CSCs.

The findings related to this study are resumed in [Zhu et al. 2013]. They show that the application of these strategies comes with certain limitations for the overall system performances. In fact, with the AZSPWM and the RSPWM, it is difficult to satisfy the requirement that only two commutations occur during the transition between vectors (for reduced switching losses). This might induce higher power losses than in conventional modulation strategies that employ the zero vectors. With the NSPWM and the RSPWM, the linear modulation region is shrunken.

Therefore, instead of minimizing the peak amplitudes of the CMVs generated by the CSR eq. (II. 13) and the CSI eq. (II. 15) by applying the reduced CMV modulation strategies on each of the converters independently; designers started to view the motor-drive system as a whole.

Hence, conventional modulation strategies that utilize the zero vectors (and avoid the limitations of reduced CMV modulation strategies) are applied to both converters with the objective of reducing the global CMV of the back-to-back system eq. (II. 17).

[Hu et al. 2013] present a technique where they fix the conventional switching sequence of one of the converters (for example the CSR) and choose the switching sequence of the other converter (the CSI) based on the minimization of the global CMV of the system. Another approach is proposed by [Guo et al. 2016]. It consists in coordinating the active and zero-state vectors of both rectifier and inverter in order to reduce the difference between the CMVs of both converters.

C- Application to the EV charger: observations and analysis

By examining the charger's conventional power circuit, illustrated in (Fig.II.14), we can deduce that the nodes N and D superimposed. Furthermore, for most grid voltage levels, the Boost is not activated.

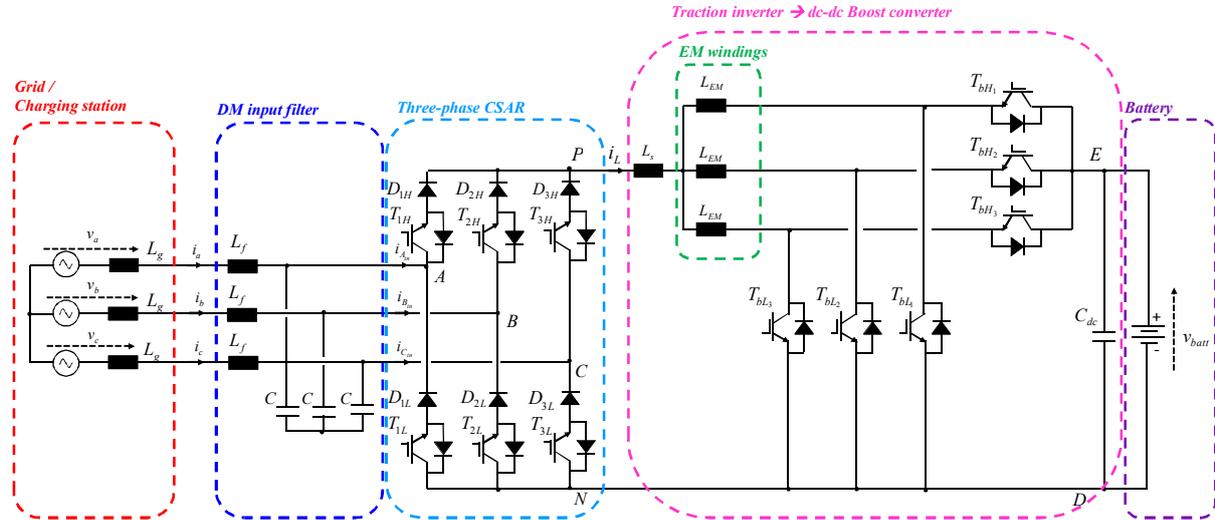


Fig.II.14. Power circuit of the three-phase integrated on-board EV charger.

This means that the CMV is mainly generated by the CSR. In addition, the voltage fluctuations at node N determine the fluctuations across the high voltage battery's negative-side terminal.

So far, the modulation techniques studied aim at the minimization of the peak values of the CMVs. However, it is just as important to reduce:

- The total number of dv/dt occurring inside a switching sequence for the CMV and the voltage at node N with respect to the frame ground.
- The amplitudes of the CMV variations as well as the voltage variations at node N.
- The average values of the CMV and the voltage at node N.

The latter has been studied by [Shang et al. 2014]. The authors present a conventional modulation technique with the order of placement of the vectors inside the switching sequence optimized for the reduction of the average value of the global CMV of the motor-drive system.

In addition, [Ripoll et al. 2014] propose a modulation technique for the CSC, denoted CMRM (Common Mode Reduction Modulation), that aims at minimizing the number and the amplitude of the dv/dt occurring at node N. To sum up, Table II. 8 resumes the modulation methods reviewed for CMV reduction in CSCs.

In summary, a comprehensive review of the various mitigation techniques employed for switch mode power supplies has been presented. The techniques found have been sorted according to their compatibility with the topology of the on-board integrated charger and evaluated with regards to the strict industrial constraints that constitute the framework of our study.

In the following, topological and switch control modifications are going to be proposed for the reduction of the CM emissions at the noise sources and along the propagation path for both charging configurations: single-phase and three-phase.

Table II. 8. MODULATION TECHNIQUES FOR CMV REDUCTION IN CSCs

SVM techniques		Criteria for CMV reduction	Characteristics
Without utilizing the zero-state vectors	AZSPWM	Peak value reduction	Avoid zero-state vectors to reduce the peak value of CMV. Risks of higher switching power losses. Limited range for the linear modulation. Risk of higher LF harmonics.
	RSPWM	Peak value reduction	
	NSPWM	Peak value reduction	
Utilization of the zero-state vectors	CMRM	Reduction of the number and amplitude of dv/dt	The zero-vectors are utilized as in conventional SVM. The harmonics, the linear modulation range and the switching losses are not affected.
	CMV average value reduction	Average value reduction	

2. Proposed modifications for the single-phase configuration

The modifications proposed in this section are inspired from the state of the art. They intervene at the levels of the power circuit and the switch control strategies. At first, they are applied to the single-phase charger: the ac-dc four-switch CSAR and the dc-dc Boost converter.

Since the same charger also needs to accommodate three-phase charging; the topological modifications are then evaluated for the three-phase six-switch CSAR and the switch control strategy is adapted to mitigate the three-phase CM current emissions.

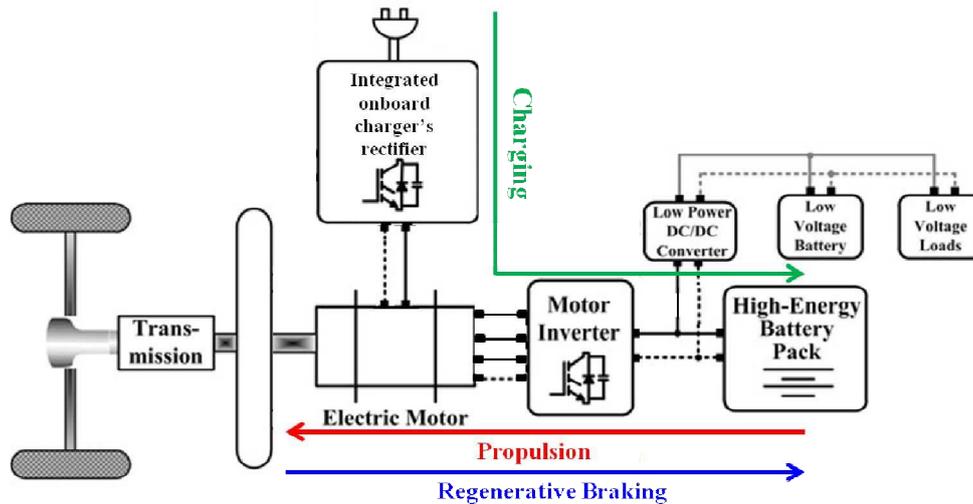


Fig.II.15. Structure of the EV powertrain having an onboard integrated high-voltage battery charger.

The changes must meet the following requirements:

- Each structural modification needs to be compatible with both power conversion topologies (single-phase and three-phase). Ideally, it should have a positive effect on the reduction of the conducted CM emissions in both configurations. However, if a modification has a favorable outcome for one configuration, it cannot be employed unless it is verified to present a positive or a neutral effect on the CM current reduction in the other configuration;
- the structural and the control modifications must not interfere with the LF behavior of the charger. The grid-side power quality, the dc-side current ripple, and the switching / conduction power losses should either be enhanced or maintained at their previous levels;
- the stray capacitance between the high-voltage battery's terminals and the frame ground is measured at 30nF. It includes the stray capacitances of all the onboard equipments sharing the battery's terminals (Fig.II.15). Therefore, the modifications need to minimize the voltage fluctuation of the battery's negative-side terminal;
- the topological modifications must be minimalistic: they should not interfere with the traction's regenerative powertrain, nor increase the volume of the charger, nor induce high costs.

The single-phase charger consists of two back-to-back converters sharing the same dc-link: the CSAR and the three-legs of the Boost converter.

2.1.1. Output stage modifications:

The Boost's low-side switches are considered to be synchronously controlled via PWM and the upper switches are always turned off Fig.II.16 (a). Therefore, the following modifications, made to the output stage, are not optimal in case of interleaving. Furthermore, the digital delays between the gating signals of the three legs are ignored and the differences between the machine's windings are neglected. Under these considerations, the analysis of the conducted CM emissions of the output stage can be conducted over an equivalent Boost leg as shown in Fig.II.16 (b). The value of the equivalent filtering inductor is given in eq. (II. 18).

$$L_{eq} = L_b + \frac{L_{EM}}{3} \quad \text{eq. (II. 18)}$$

The balanced switching of the equivalent circuit can be achieved by adding a new diode in the path of the return current and equally splitting the equivalent filtering inductor onto both dc buses (refer to Fig.II.2(b)). These modifications do not affect the LF behavior of the converter (same current ripple). However, they have a direct effect on the conducted CM emissions. The applied modifications transform the node D into a voltage fluctuating node that varies in opposition to the voltage at node M. Therefore, the modified Boost converter presents two switching cells $\{T_{bL}, D_{bH}\}$ & $\{T_{bL}, D_{new}\}$ having nodes M and D as midpoints.

Moreover, the modifications change the dependency of the voltage across the battery's stray capacitance from the input and shift it towards the output voltage. This is particularly interesting in the case of back-to-back converters. In fact, the CSAR has a fluctuating voltage at its output. In the conventional Boost converter, the voltage at the load's stray capacitance is dependent on the input voltage of the Boost. This means that, if no modifications are made, the voltage across the battery's stray capacitance will vary according to the fluctuations of the CSAR's output voltage. The modified power circuit of the output stage is illustrated in Fig.II.16 (c) and the fluctuations of the battery's negative-side voltage are going to be studied in Section 3.

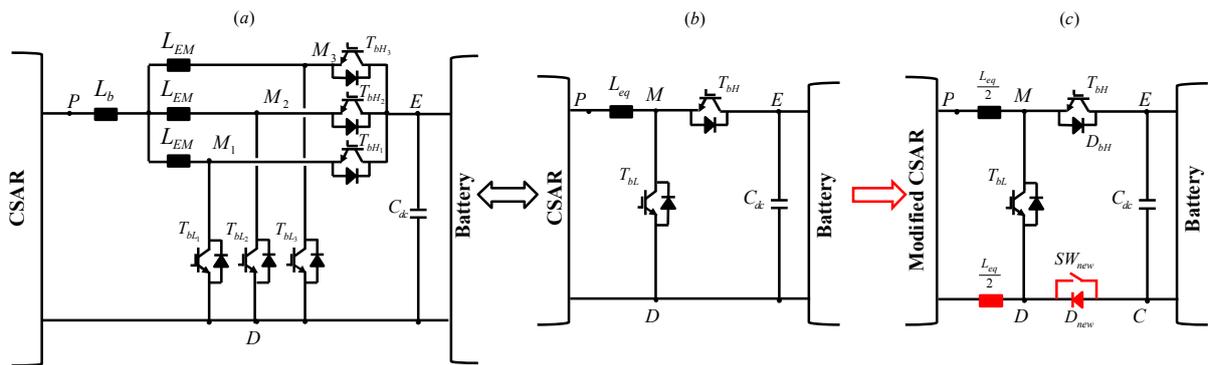


Fig.II.16. (a) Traction inverter used as a dc-dc Boost converter. (b) Equivalent output stage. (c) Modified balanced equivalent output stage.

Nonetheless, the modifications made to the Boost (i.e. the traction's inverter) also intervene in the propulsion powertrain of the EV. Since the added diode blocks the battery's current during traction, a switching element is added (SW_{new}) in parallel to the new diode. It is switched-on during propulsion in

order to short-circuit the new diode and switched-off during charging. It may consist of a relay or a thyristor.

2.1.2. Input stage modifications

If we only consider the input Buck-type CSAR, the Boost and the battery are replaced with an (L, R) load. The operation of the conventional single-phase CSAR is equivalent to the power circuit shown in Fig.II.17. The analysis will take place during the positive half cycle of the input voltage (the same can be applied to the negative half cycle). Furthermore, the switches that are turned-on are illustrated in green.

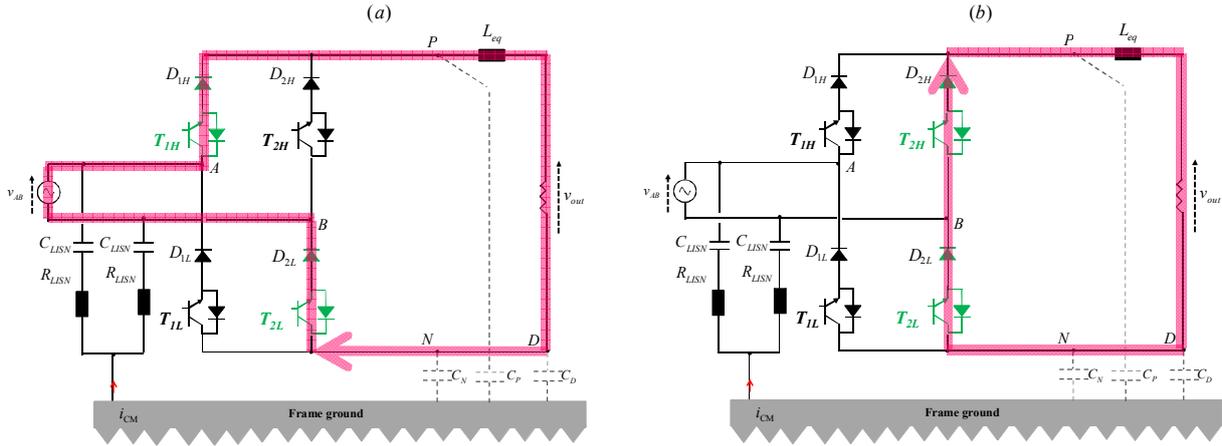


Fig.II.17. Operation of the conventional single-phase CSAR during the positive half-cycle of the input voltage. (a) During the active state. (b) During the freewheeling state.

As seen in Part A Chapter 1, the low-side switches (T_{1L} & T_{2L}) are always turned on. The upper switches (T_{1H} & T_{2H}) are controlled via PWM in order to ensure both active and freewheeling states of the DM current flowing through the inductor. The switching states as well as the voltages at different nodes are given in Table II. 9.

Table II. 9. SWITCHING STATES AND VOLTAGES ACROSS PARASITIC CAPACITANCES OF A CONVENTIONAL SINGLE-PHASE CSAR

	$v_{AB} \geq 0$			$v_{AB} < 0$		
	<i>Active state</i>	<i>Freewheeling state</i>	<i>Voltage variation</i> Δv	<i>Active state</i>	<i>Freewheeling state</i>	<i>Voltage variation</i> Δv
	T_{1H} ON T_{2H} OFF $\{T_{1L}, T_{2L}\}$ ON	T_{1H} OFF T_{2H} ON $\{T_{1L}, T_{2L}\}$ ON		T_{1H} OFF T_{2H} ON $\{T_{1L}, T_{2L}\}$ ON	T_{1H} ON T_{2H} OFF $\{T_{1L}, T_{2L}\}$ ON	
v_P	$\frac{v_{AB}}{2}$	$-\frac{v_{AB}}{2}$	$\mp v_{AB}$	$-\frac{v_{AB}}{2}$	$\frac{v_{AB}}{2}$	$\pm v_{AB}$
v_N	$-\frac{v_{AB}}{2}$	$-\frac{v_{AB}}{2}$	0	$\frac{v_{AB}}{2}$	$\frac{v_{AB}}{2}$	0
v_D	$-\frac{v_{AB}}{2}$	$-\frac{v_{AB}}{2}$	0	$\frac{v_{AB}}{2}$	$\frac{v_{AB}}{2}$	0

It can be deduced that, during each half cycle of the input voltage, the voltages across the parasitic capacitances C_N & C_D do not vary at the switching frequency. However, they present a LF variation dependent on the grid's input voltage v_{AB} . Moreover, the node P presents HF variations of $\pm v_{AB}/2$ at the switching frequency. It represents the major source of conducted CM emissions.

This means that, at each switching period, the operation of the conventional single-phase CSAR is equivalent to that of a single-phase diode bridge followed by a dc-dc Buck converter. This is verified by comparing the voltages obtained across the parasitic capacitances with those of a conventional dc-dc Buck converter given in Table II. 3.

Therefore, the modifications made to the conventional CSAR are inspired from the state of the art related to the balanced switching of the dc-dc Buck converter.

As such, a freewheeling diode is going to be added between the nodes P & N at the output of the CSAR (Fig.II.18). However, this modification is not sufficient on its own. In order to ensure the balanced switching of the CSAR, the switch control laws of the upper and lower switches must be modified as follows:

- During the positive half cycle of the input voltage:

The switches T1H and T2L are both controlled via PWM and receive the same gating commands while the switches T2H and T1L are both switched-off. During the freewheeling state all four switches are turned-off.

- During the negative half cycle of the input voltage:

The switches T2H and T1L are both controlled via PWM and receive the same gating commands while the switches T1H and T2L are both switched-off. During the freewheeling state all four switches are turned-off.

This choice of gating control for the switches allows for balanced switching between the upper switching cells (midpoint P) and the lower switching cells (midpoint N). By doing so, we ensure similar operation to the dc-dc Buck converter's modified topology illustrated in Fig.II.4 (b).

The switching states and the voltages across the parasitic capacitances are given in Table II. 10. It can be seen that the topological modification consisting of the added diode along with the changes made to the switch control laws of the CSAR transform nodes N & D into fluctuating nodes. Furthermore, during each half cycle of the input voltage, the voltage across C_N varies by the same amount ($v_{AB}/2$) but in opposite polarity to the voltage across C_P . This leads to a partial (or total if $C_N=C_P$) compensation of the CM currents generated at these nodes.

On the other hand, the addition of this diode allows the reduction of the conduction losses during the freewheeling state. In fact, in the conventional CSAR, the freewheeling current flows through two switches and two diodes before returning to the inductor. With the added diode, the switches are turned off; hence, the freewheeling current only passes through one diode: D_{fw} [Nussbaumer et al. 2007].

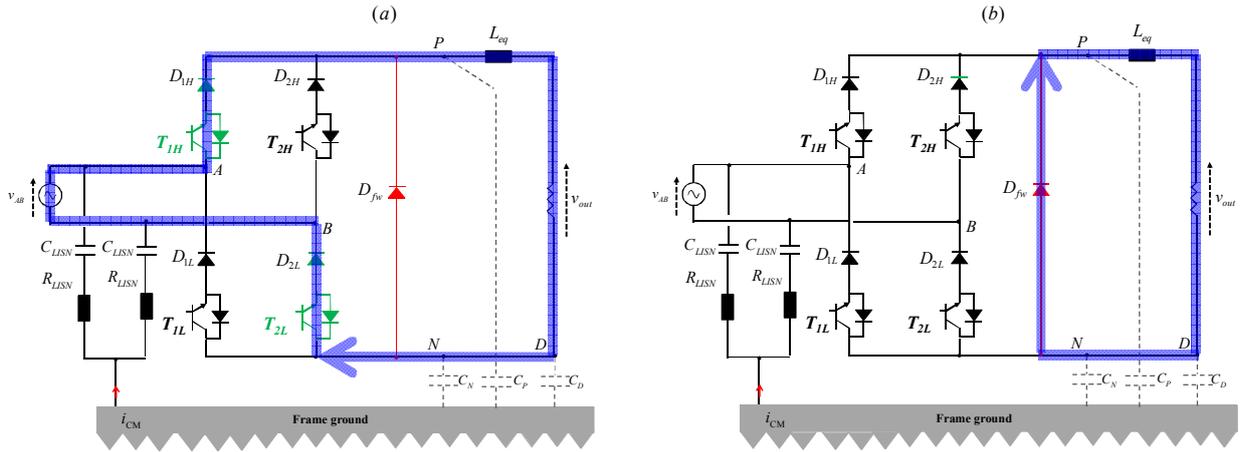


Fig.II.18. Operation of the modified balanced single-phase CSAR during the positive half-cycle of the input voltage. (a) During the active state. (b) During the freewheeling state.

Table II. 10. SWITCHING STATES AND VOLTAGES ACROSS PARASITIC CAPACITANCES OF A THE MODIFIED BALANCED SINGLE-PHASE CSAR

	$v_{AB} \geq 0$			$v_{AB} < 0$		
	<i>Active state</i>	<i>Freewheeling state</i>	<i>Voltage variation</i> Δv	<i>Active state</i>	<i>Freewheeling state</i>	<i>Voltage variation</i> Δv
	T_{1H} ON T_{2H} OFF T_{1L} OFF T_{2L} ON	T_{1H} OFF T_{2H} OFF T_{1L} OFF T_{2L} OFF		T_{1H} OFF T_{2H} ON T_{1L} ON T_{2L} OFF	T_{1H} OFF T_{2H} OFF T_{1L} OFF T_{2L} OFF	
v_P	$\frac{v_{AB}}{2}$	0	$\mp \frac{v_{AB}}{2}$	$-\frac{v_{AB}}{2}$	0	$\pm \frac{v_{AB}}{2}$
v_N	$-\frac{v_{AB}}{2}$	0	$\pm \frac{v_{AB}}{2}$	$\frac{v_{AB}}{2}$	0	$\mp \frac{v_{AB}}{2}$
v_D	$-\frac{v_{AB}}{2}$	0	$\pm \frac{v_{AB}}{2}$	$\frac{v_{AB}}{2}$	0	$\mp \frac{v_{AB}}{2}$

The only disadvantage is that the modifications transform the voltage across the load's parasitic capacitance into a fluctuating voltage presenting variations of $\pm v_{AB}/2$. This capacitance becomes the new source of conducted CM emissions.

Therefore, a final modification is needed in order to dissociate the node D from the low-side switching cell of the CSAR. The modification is compatible with what has been proposed for the Boost stage. It consists in splitting the filtering inductor into two inductors of equal inductance value; each placed on one side of the dc bus as shown in Fig.II.19.

This modification is also in line with the balancing of the dc-dc Buck converter previously presented in Fig.II.4 (b).

Finally, the voltages across the parasitic capacitances for the different switching states are given in Table II. 11.

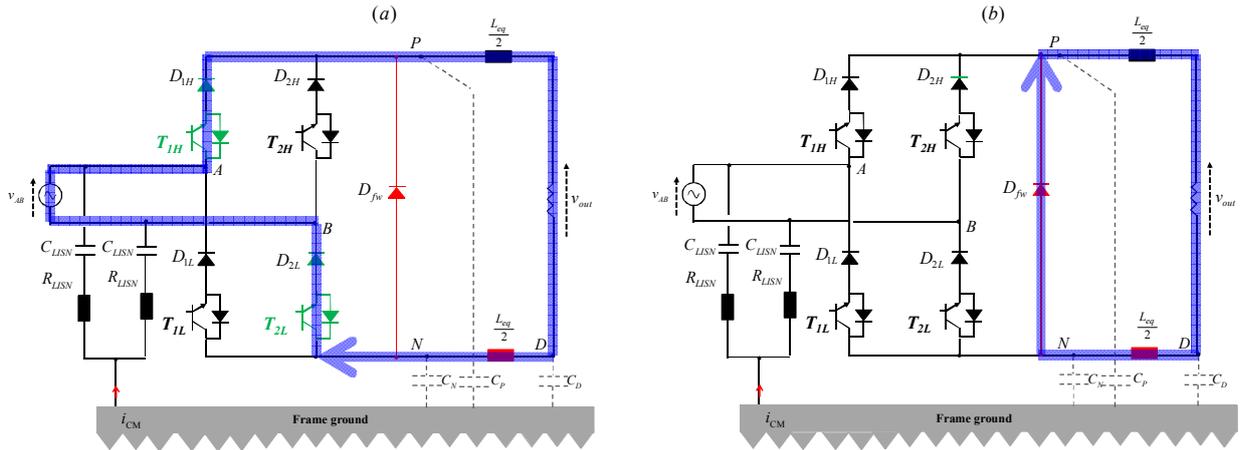


Fig.II.19. Operation of the modified balanced single-phase CSAR with a decoupled output stage during the positive half-cycle of the input voltage. (a) During the active state. (b) During the freewheeling state.

Table II. 11. VOLTAGES ACROSS PARASITIC CAPACITANCES OF A THE MODIFIED BALANCED SINGLE-PHASE CSAR WITH A DECOUPLED OUTPUT STAGE

	$v_{AB} \geq 0$			$v_{AB} < 0$		
	<i>Active state</i>	<i>Freewheeling state</i>	<i>Voltage variation</i> Δv	<i>Active state</i>	<i>Freewheeling state</i>	<i>Voltage variation</i> Δv
	T_{1H} ON T_{2H} OFF T_{1L} OFF T_{2L} ON	T_{1H} OFF T_{2H} OFF T_{1L} OFF T_{2L} OFF		T_{1H} OFF T_{2H} ON T_{1L} ON T_{2L} OFF	T_{1H} OFF T_{2H} OFF T_{1L} OFF T_{2L} OFF	
v_P	$\frac{v_{AB}}{2}$	0	$\mp \frac{v_{AB}}{2}$	$-\frac{v_{AB}}{2}$	0	$\pm \frac{v_{AB}}{2}$
v_N	$-\frac{v_{AB}}{2}$	0	$\pm \frac{v_{AB}}{2}$	$\frac{v_{AB}}{2}$	0	$\mp \frac{v_{AB}}{2}$
v_D	$-\frac{v_{out}}{2}$	$-\frac{v_{out}}{2}$	0	$-\frac{v_{out}}{2}$	$-\frac{v_{out}}{2}$	0

The effects of the entire modifications are clearly visible:

- The voltage across the load's parasitic capacitance is stabilized and its dependency is shifted from the input to the output voltage.
- The voltage across the lower switching cell's parasitic capacitance C_N is transformed into a varying voltage. The variations occur in opposition to the ones detected across the upper switching cell's parasitic capacitance C_P . Thus, compensation of the conducted CM currents is achieved.

After studying the input and the output stages separately, we should regroup the modifications and verify their positive effects on the mitigation of the conducted emissions of the overall back-to-back converter.

D- Summary of the applied modifications in the single-phase configuration

To sum up, the combined modifications that are proposed consist in:

Topological modifications

- Adding a free-wheeling diode at the output of the CSAR: D_{fw} .
- Adding a new diode in the path of the return current of the Boost converter: D_{new} .
- Adding a switching element in parallel with the new diode: SW_{new} .
- Splitting the Boost inductor onto both dc buses: L_{dc+} & L_{dc-} .

Control modification

- Switch control strategy of the CSAR:

$$\begin{aligned}
 \text{if } v_{AB} \geq 0 : & \begin{cases} f_{T1H} = PWM \\ f_{T2H} = 0 \\ f_{T1L} = 0 \\ f_{T2L} = f_{T1H} \\ f_{D_{fw}} = 1 - f_{T1H} \end{cases} \\
 \text{if } v_{AB} < 0 : & \begin{cases} f_{T1H} = 0 \\ f_{T2H} = PWM \\ f_{T1L} = f_{T2H} \\ f_{T2L} = 0 \\ f_{D_{fw}} = 1 - f_{T2H} \end{cases}
 \end{aligned} \tag{II. 19}$$

The equivalent modified single-phase charging power circuit is given in Fig.II.20. The modified / added components are highlighted.

So far, we have studied the conducted EMI mitigation for the equivalent circuit. However, these modifications need to be applied to the actual integrated power circuit (Fig.II.21).

In order to maintain the LF behavior of the converter intact, the split inductors need to maintain the total value of inductance seen by the DM current flowing through the circuit. Therefore, the Boost inductor is split according to eq. (II. 20). The onboard integrated charger's modified topology is illustrated in Fig.II.21.

$$\begin{cases} L_{dc+} = \frac{L_b}{2} - \frac{L_{EM}}{6} \\ L_{dc-} = \frac{L_b}{2} + \frac{L_{EM}}{6} \end{cases} \tag{II. 20}$$

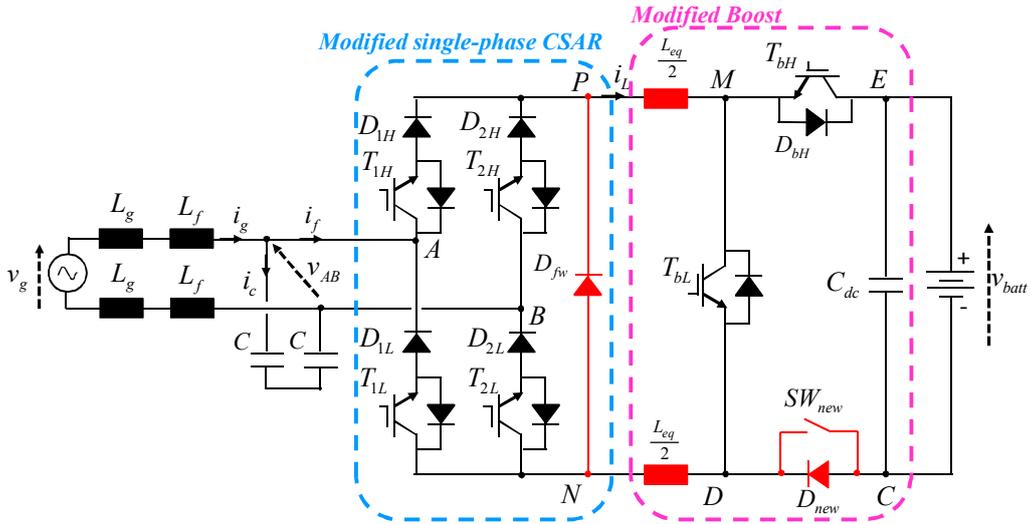


Fig.II.20. Equivalent power circuit of the modified balanced single-phase charger.

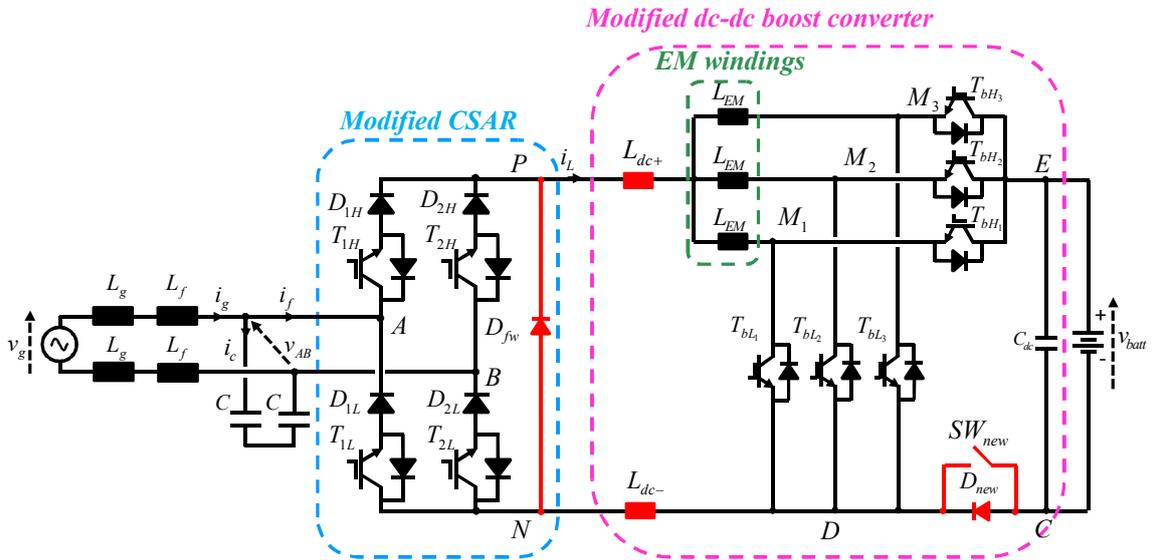


Fig.II.21. Power circuit of the modified balanced single-phase charger.

3. Evaluation of the fluctuation of the battery's low side voltage

On-board chargers share their high-voltage battery's connections with the on-board electronics meant for the ventilation and air conditioning, the 14V low-voltage isolated on-board power system and other consumers as shown in Fig.II.22. This means that the lumped stray capacitance between the negative rail of the high-voltage battery and the frame ground includes the parasitic capacitances of all the systems sharing the battery's DC rails. Therefore, the voltage across this capacitance (depicted by HV_m in Fig.II.23) must vary the least possible otherwise high leakage currents could flow towards the chassis.

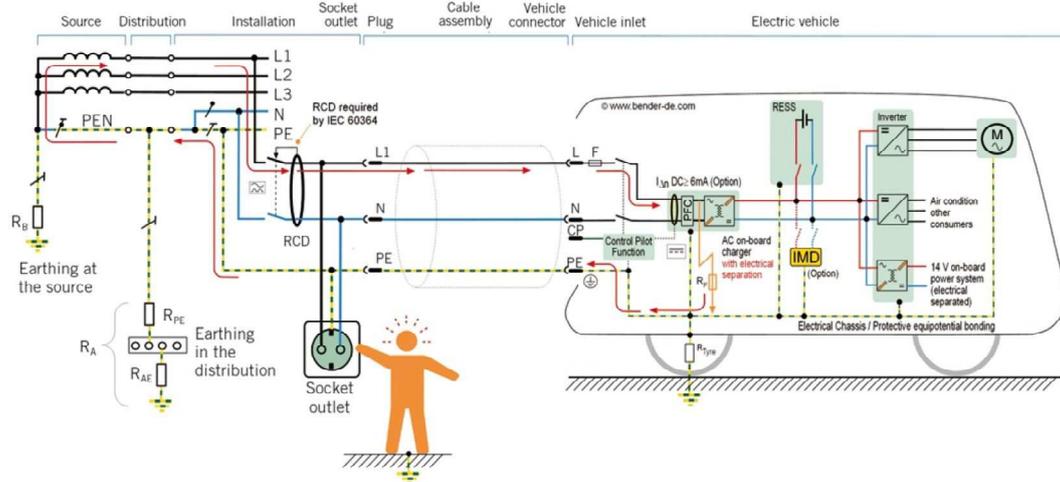


Fig.II.22. Example of a DC fault current's path triggered by insulation fault in Power Factor Correction input stage of an on-board single-phase charger. [Bender 2012].

Line to ground capacitors used for common mode filtering as well as parasitic capacitances are present at various stages of the charger. During charging, these capacitors are excited by the voltages generated across them. These common mode voltages can have low frequency as well as high frequency components. Thus, the voltages applied to the capacitors generate common mode currents that flow to the chassis of the vehicle. As a result, the currents flowing through the chassis are called leakage currents.

Leakage currents are harmless if the chassis is well grounded. However, if the ground circuit is faulty (earth conductor presents a high impedance path or is absent from the installation), the risk of electrical shock for any person touching a bare metal part of the chassis is very high. In this case, the leakage current is called either the “touch current” if the earth connection is absent from the installation or the “contact current” if the earth connection is present but offers a high impedance path for the leakage current. Therefore, the maximum leakage current should not exceed a safe limit specified by the safety regulations. The IEC 60364-7-722 standard (“Low voltage electrical installations –Part 7-722: requirements for special installations or locations – Supply of electric vehicle”) defines the proper residual current protective devices (Type B RCD with a rated residual current lower than or equal to 30 mA and capable of tripping for DC fault currents higher than 6 mA) to be used in order to ensure the protection of persons against indirect electrical shocks. However, if the high frequency components of the leakage current are too high, one of two things may happen. The RCD may nuisance trip or it may be blinded. Any event that can cause blinding of an RCD is a huge risk to the user. Therefore, the IEC 61851-21 safety standard (“Electric vehicle conductive charging

system Part 21: Electric vehicle requirements for conductive connection to an a.c/d.c. supply”) specifies that the touch current should not exceed 3.5 mA RMS. The vehicle test setup is described in NF EN 60990 (“Methods of measurement of touch current and protective conductor current”).

The on-board charger studied presents a high parasitic capacitance (measured at 30 nF) between the negative rail of the battery and the ground. Therefore, in order to evaluate its impact on the CM emissions, one needs to study the variations of HVm .

3.1. Conventional unbalanced single-phase charger

The charger studied is non-isolated from the grid. Hence, the AC leakage currents may contain a component at grid frequency (50/60 Hz) mainly due to the voltage between the battery connections and the frame ground HVm (except for IT earthing systems). In this configuration the node D is connected to node N. Therefore the voltage across C_D is entirely dependent on the input voltage and the control of the CARS’s lower switches.

As previously mentioned, the lower switches are always turned on. Therefore, at each switching period, the common mode behavior of the charger can be described by a single-phase diode bridge followed by a dc/dc Buck converter and a dc/dc Boost converter as shown in Fig.II.23. We can deduce that HVm depends on the grid voltage and does not contain high frequency variations. For all the switching configurations of the Buck and the Boost converter, the expression of HVm is given in eq. (II. 21). Therefore, the parasitic capacitance C_D is excited at grid frequency and generates a LF CM current. If the generated AC leakage current is high enough it can trip the 30 mA RCD.

$$HVm = -\frac{|v_{AB}|}{2} \quad \text{eq. (II. 21)}$$

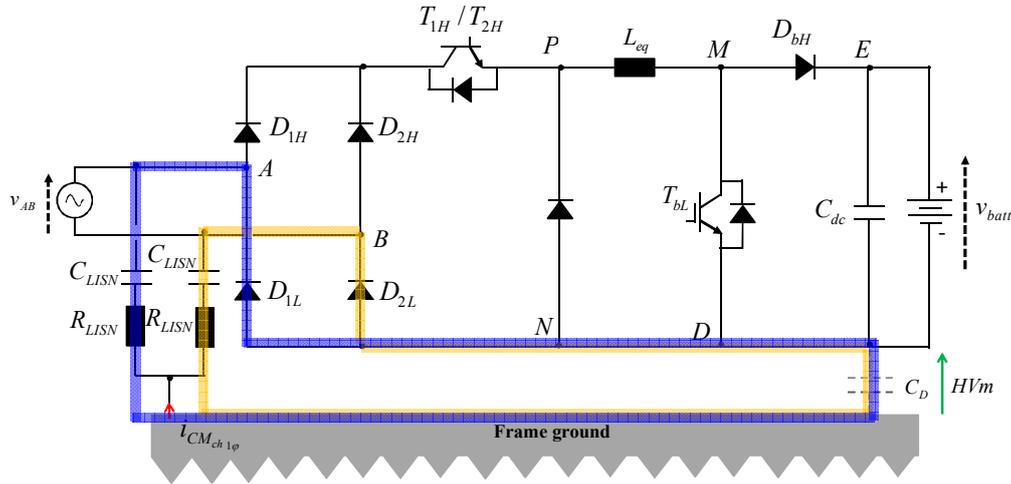


Fig.II.23. Equivalent power circuit of the single-phase charger, at each switching period, for the study of the battery’s common mode voltage. (yellow) Voltage loop during the positive half cycle of the input voltage. (blue) Voltage loop during the negative half cycle of the input voltage.

3.2. Modified balanced single-phase charger

The proposed modifications for the reduction of the CM currents generated at the switching cells’ level have a positive effect on the reduction of the leakage currents due to the fluctuation of HVm . In

fact, following the topological changes, the charger's behavior, at each switching period, is identical to the power circuit presented in Fig.II.24. According to eq. (II. 22), HVm is a function of the voltages across the added elements (split inductor, new diode, and the low side switches of the CSAR) as well as the grid side voltage.

$$HVm = v_{AK} + v_L + v_T - \frac{|v_{AB}|}{2} \quad \text{eq. (II. 22)}$$

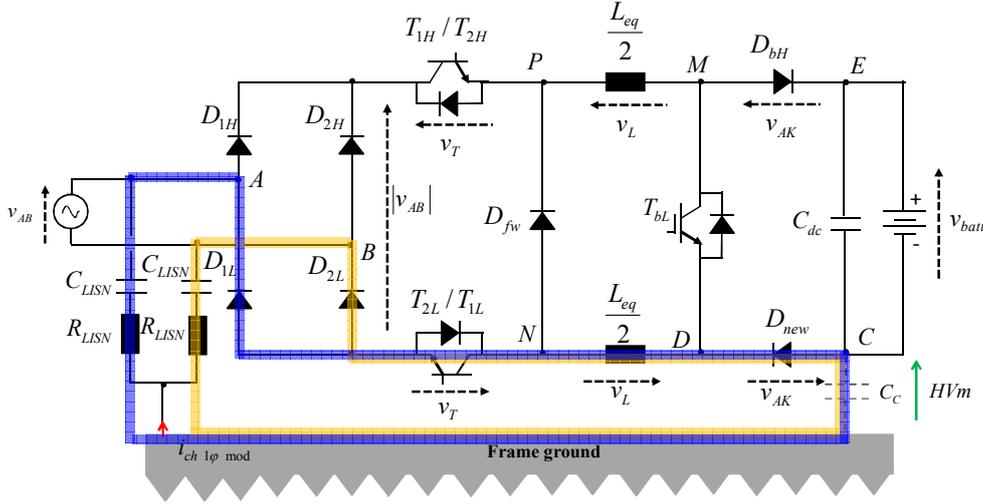


Fig.II.24. Equivalent power circuit of the modified single-phase charger, at each switching period, for the study of the battery's common mode voltage. (yellow) Voltage loop during the positive half cycle of the input voltage. (blue) Voltage loop during the negative half cycle of the input voltage.

Table II. 12 gives the expression of HVm for all the possible switching configurations of the CSAR and the Boost.

Table II. 12. EXPRESSION OF HVm FOR ALL POSSIBLE SWITCHING CONFIGURATIONS

	$\{T_{1H}, T_{2L}\}$ or $\{T_{2H}, T_{1L}\}$ ON D_{fw} OFF		$\{T_{1H}, T_{2L}\}$ or $\{T_{2H}, T_{1L}\}$ OFF D_{fw} ON	
	T_{bl} OFF D_{bH} & D_{new} ON	T_{bl} ON D_{bH} & D_{new} OFF	T_{bl} OFF D_{bH} & D_{new} ON	T_{bl} ON D_{bH} & D_{new} OFF
v_{AK}	$V_{threshold} \downarrow\downarrow$	$-\frac{v_{batt}}{2}$	$V_{threshold} \downarrow\downarrow$	$-\frac{v_{batt}}{2}$
v_L	$\frac{ v_{AB} }{2} - \frac{v_{batt}}{2}$	$\frac{ v_{AB} }{2}$	$-\frac{v_{batt}}{2}$	$0V$
v_T	$V_{ON} \downarrow\downarrow$	$V_{ON} \downarrow\downarrow$	$\frac{ v_{AB} }{2}$	$\frac{ v_{AB} }{2}$
HVm	$-\frac{v_{batt}}{2}$	$-\frac{v_{batt}}{2}$	$-\frac{v_{batt}}{2}$	$-\frac{v_{batt}}{2}$

It can be deduced that this voltage maintains the same DC value which is a function of the battery's voltage. Therefore, the topological modifications induce no leakage current through C_C .

By modifying the single-phase charger's topology along with the input CSAR's switch control law and by admitting equal distribution of the voltages across the semi-conductors at switch off; we managed to eliminate the component of the leakage current that is at grid frequency.

The modifications are going to be evaluated using the previously developed conducted EMI modeling approach.

4. Evaluation of the modifications using the conducted EMI modeling approach

The step by step modeling of the modified balanced single-phase charger (Fig.II.25) is given in Appendix F. By chaining the models developed for the input and the output stages sharing the same dc-link, we can recreate the combined CM & DM conducted EMI model of the modified single-phase EV charger given in Fig.II.26 (b). In order to keep the coherence throughout our demonstration, the case of an IT network where the mains neutral is isolated from the ground is going to be considered.

At this stage, it is interesting to compare the EMI models of the conventional single-phase charger (Fig.II.26 (a)) with that of the modified balanced topology (Fig.II.26 (b)):

- The modifications made to the input stage transform the node N into a fluctuating node varying at the switching frequency and in opposition to the voltage variations at node P (as opposed to slow variations at the grid's frequency in the conventional model of Fig.II.26 (a)). Furthermore, the switch control law adopted ensures that the voltage sources at nodes P and N are of opposite values; hence, the dv/dt at these nodes share the same absolute value.
- The modifications made to the output stage contribute to the addition of an extra voltage source in the path of the return current. It imposes, at node D, voltage fluctuations of opposite values to those present at node M. Moreover, the voltage at the negative side of the battery is independent from the input and presents no variations; neither at grid frequencies nor at the switching frequency.
- When compared to the conventional topology, the modified model's voltage sources vary by half of the original amounts.
- The changes contribute to render the topology symmetrical which contributes to lowering the mixed mode emissions at higher frequencies.

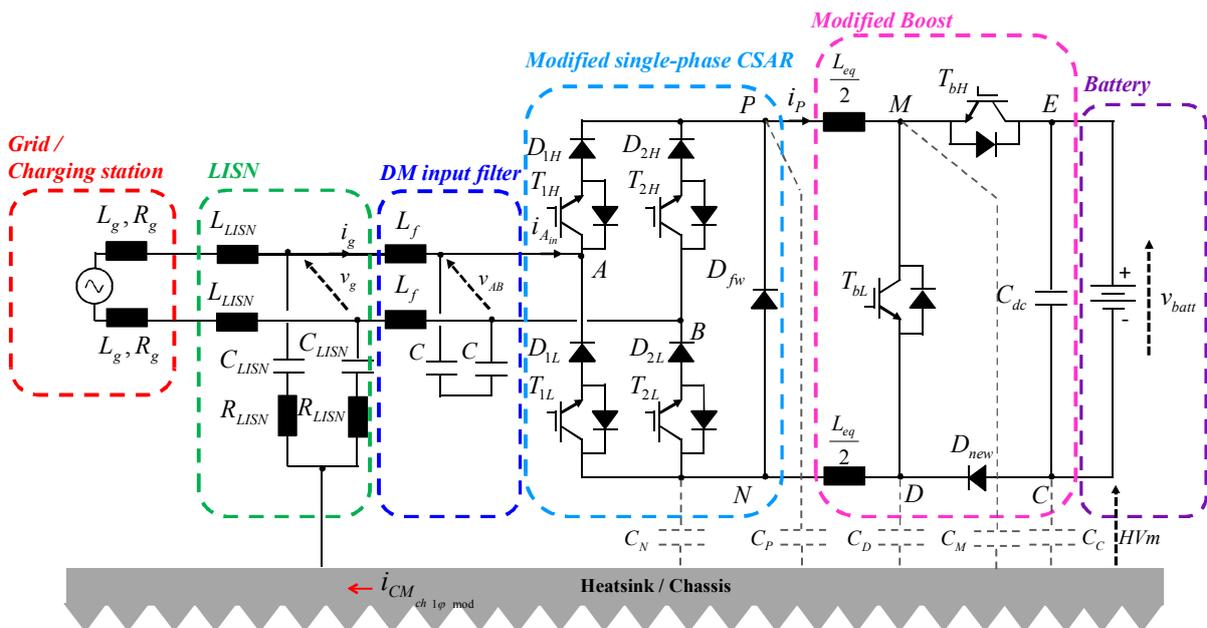


Fig.II.25. Power circuit of the single-phase charger modified to ensure topological symmetry.

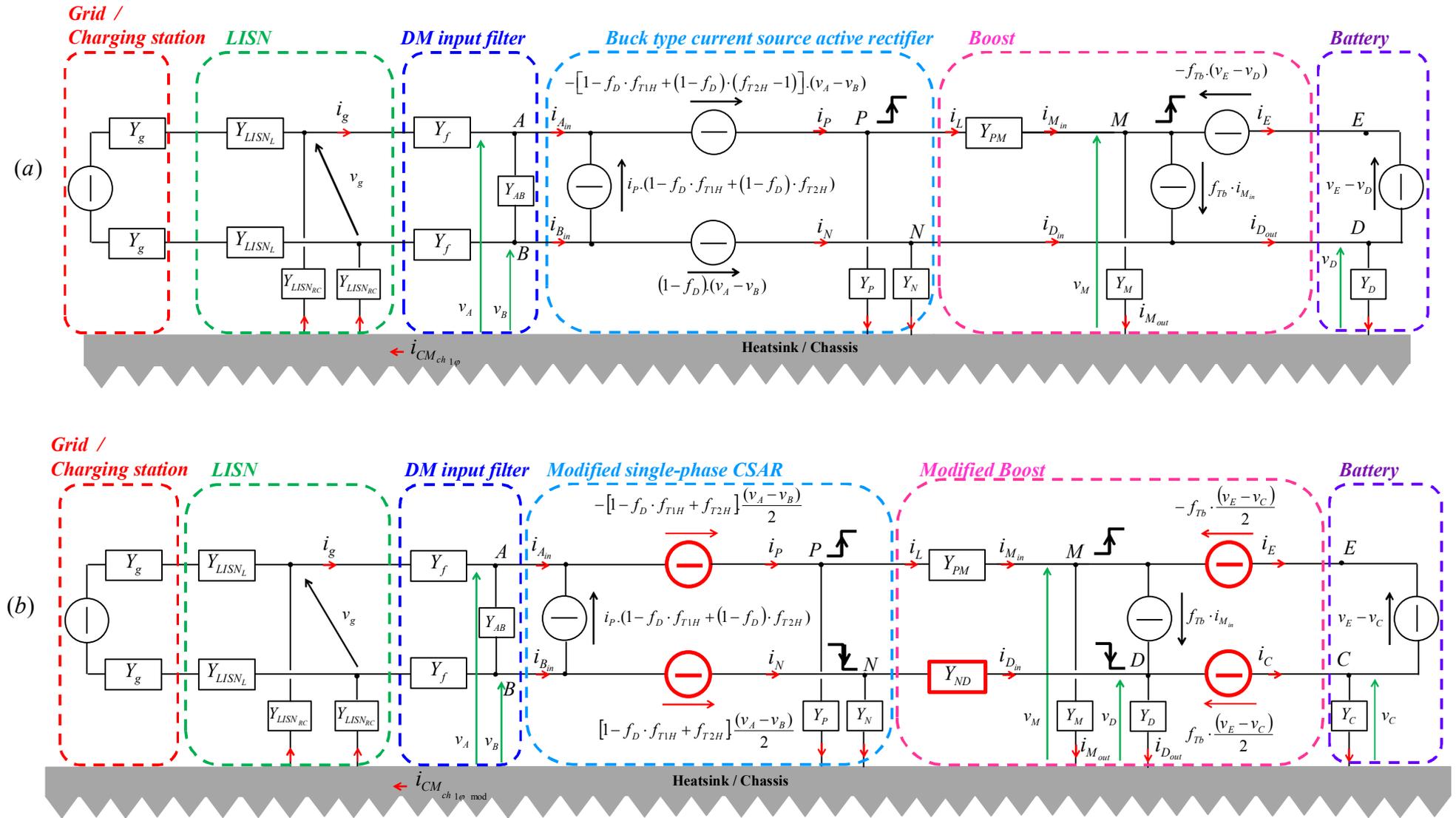


Fig.II.26. EMI model of the single-phase charger (a) Conventional topology. (b) Modified topology and switch control law to ensure balanced switching.

5. Simulation results

The conducted emissions are going to be compared for the conventional charger (without modifications) and the balanced topology (after modifications). Therefore, the control strategy must be the same for both power circuits in order to evaluate the modifications' HF impact on the CM current. Hence, the single-phase control strategy presented in Part B Chapter 1 is going to be employed for all the simulations in the single-phase configuration. The battery is initially considered to be discharged at 260V. Furthermore, for each topology (conventional & modified) the results are going to be provided for the power circuit simulation as well as the corresponding EMI model's simulation.

5.1. Conventional single-phase charger

At the control level, the switch control law of the CSAR is the same as the one described for the conventional charger in Part B Chapter 1. The power circuit simulated represents the conventional charger without topological modifications and the corresponding EMI model is given in Fig.II.26 (a).

5.2. Modified balanced single-phase charger

The switch control law applied is the one presented in eq. (II. 19). The topological modifications are also taken into consideration. The power circuit simulated is the one given in Fig.II.25 and the corresponding EMI model is illustrated in Fig.II.26 (b).

The voltage waveforms at critical nodes of the charger are given in Fig.II.27 along with the instantaneous CM current measured at the input of the LISN. The results are shown over one fundamental period (0.02 sec.). It is clear that in the case of the conventional charger, the nodes at the negative side of the dc bus (v_N , v_D & HVm) are superimposed and undergo mainly LF variations.

The voltages at the midpoint of the high side switching cell v_P and the Boost's switching cell v_M fluctuate at the switching frequency. Therefore, the latter voltages (v_P & v_M) applied across the parasitic capacitances (C_P & C_M respectively) generate the CM current $i_{cm\ ch\ 1\phi}$ that leaks towards the frame ground. In addition, the LF variations of HVm across C_D (30nF) contribute to a rich LF content in the generated CM current as can be seen in Fig.II.29.

On the other hand, the effect of the topological and switch control modifications on the charger's HF behavior is clearly visible in Fig.II.28.

In fact, the input stage modifications (added freewheeling diode and adequate switch control strategy) transform the voltage at node N into a fluctuating voltage. Furthermore, the fluctuations are in opposition to the voltage variations at node P. Under the assumption of the absence of delays between the gating signals of the CSAR's switches and the possibility of using the balanced propagation path technique to balance the stray capacitances at these nodes; compensation of the CM currents at the output of the modified CSAR can be achieved.

Moreover, the split dc-bus inductor and the addition of the diode in the return path of the Boost's output current transform the voltage at node D into a fluctuating voltage with variations in opposition to the ones present at node M. Under the assumption of the absence of delays between the gating signals of the synchronous Boost legs and the possibility of using the balanced propagation path

technique to balance the stray capacitances at these nodes; compensation of the CM currents at the input of the Boost can be achieved.

On the other hand, placing the split inductor on the low side of the dc-bus and adding the diode at the output of the Boost render the voltage across the high-voltage battery's stray capacitance (HVm) independent from the switching cells and the grid. It takes on a negative dc value equal to half of the battery's voltage (-130 V) as presented in Table II. 12.

The positive effect of these changes on the mitigation of the conducted CM emissions of the EV charger can be verified by comparing the waveforms of the CM currents in Fig.II.28.

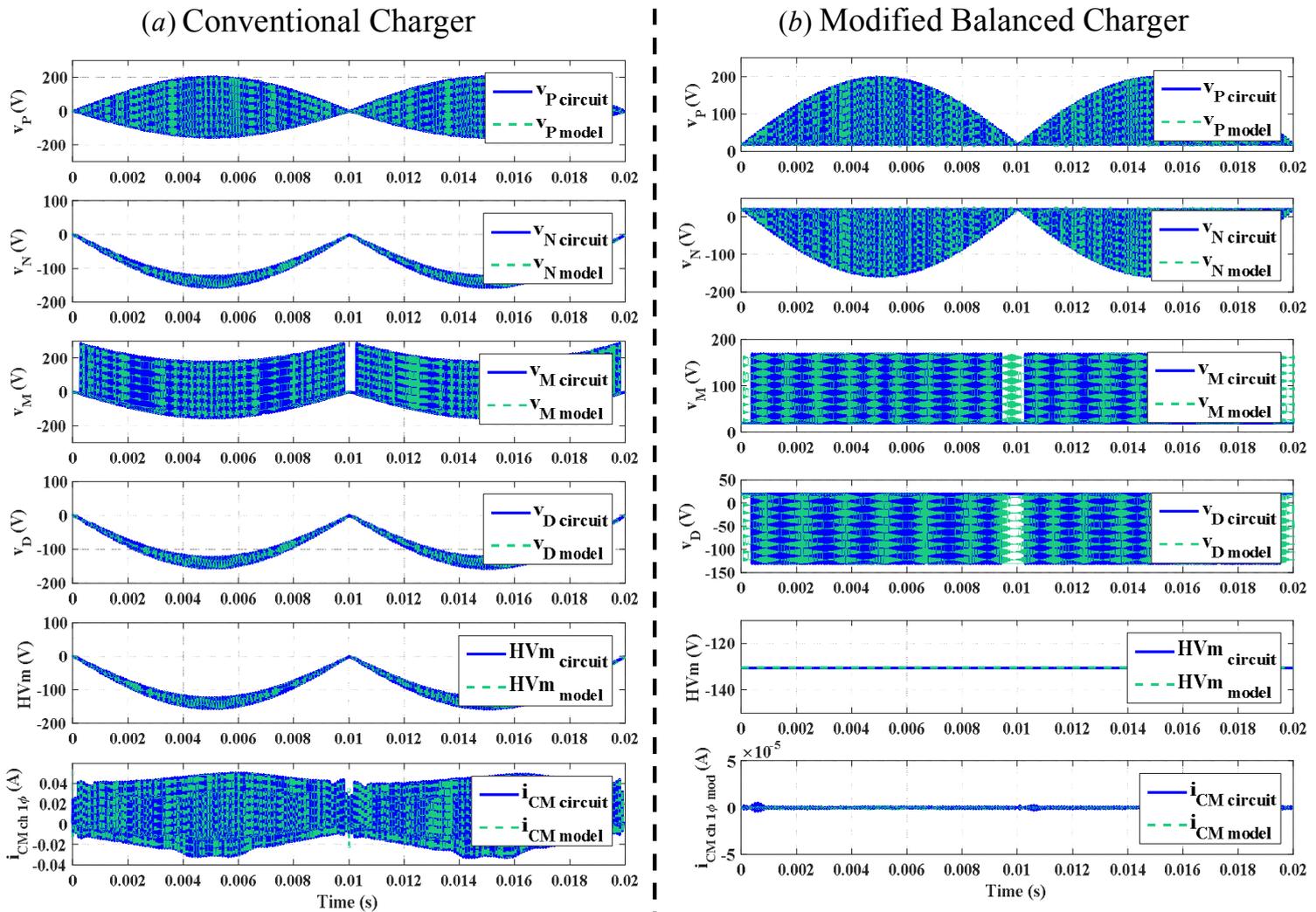


Fig.II.27. Simulation results for the single-phase charger over one fundamental period and for the same charge power (7 kW). (a) Conventional charger. (b) Modified balanced charger.

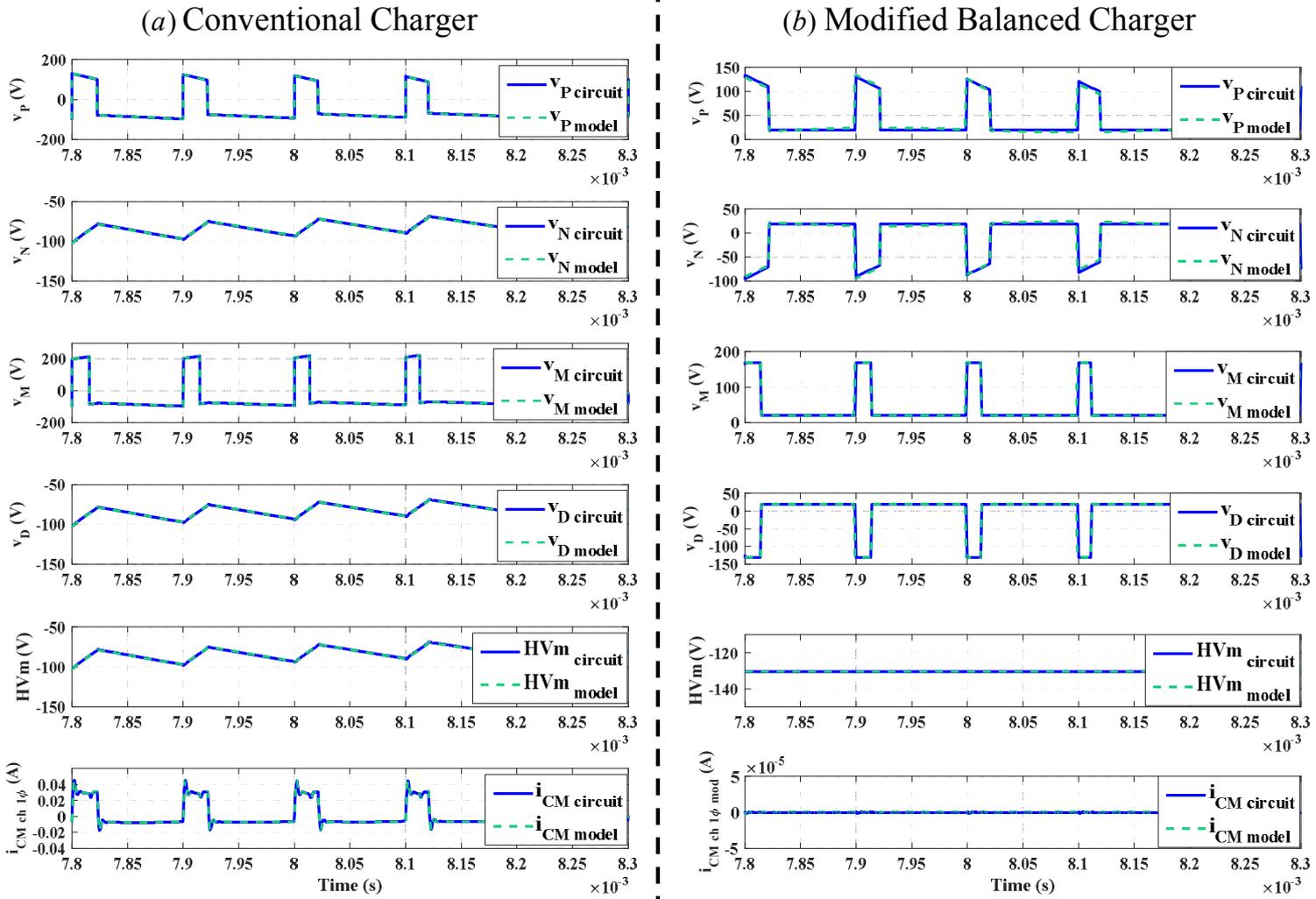


Fig.II.28. Simulation results for the single-phase charger over five switching periods. (a) Conventional charger. (b) Modified balanced charger.

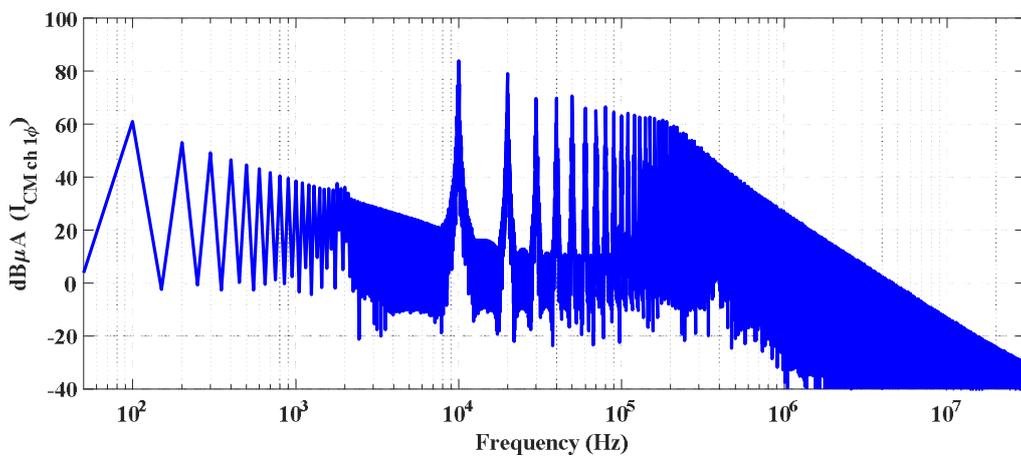


Fig.II.29. Spectral analysis of the common mode current generated by the conventional charger's circuit.

5.3. Impact of non-idealities

So far the balancing method has been developed under certain assumptions, among which:

- An evenly split dc inductor $L_{dc-} = L_{dc+} + \frac{L_{EM}}{3}$
- A perfect synchronization between the gating commands of each set of switches: $\{T_{1H}, T_{2L}\}$ & $\{T_{2H}, T_{1L}\}$
- A perfect synchronization between the gating commands of the three legs of the Boost (i.e. the traction's inverter)
- An equal distribution of the voltages across series switches or diodes at turn-off
- Equal stray capacitances present at nodes P & N as well as equal stray capacitances at nodes M & D

Under these conditions, the obtained CM current equals zero as shown in Fig.II.28. In this paragraph, we aim to study the impact of non-idealities on the effectiveness of the proposed EMI balancing technique. Therefore, some of the previously mentioned assumptions are going to be challenged. In each case study (i.e. the modified topology with a non-ideal behavior), the spectral analysis of the generated CM current is going to be compared with that of the conventional topology (given in Fig.II.29).

The aim is to verify that even under non-ideal behavior, the modifications applied still exhibit the mitigation of the CM emissions. It should be noted that the results are shown for Silicon IGBTs switching at 10 kHz.

5.3.1. Unevenly split dc inductors

It is difficult to obtain two perfectly split inductors with equal inductance values. Therefore we will consider a difference of 10% so that $L_{dc-} = 1.1 \times L_{dc+}$. The simulation of the modified unbalanced power circuit is carried using the values defined in Fig.II.30.

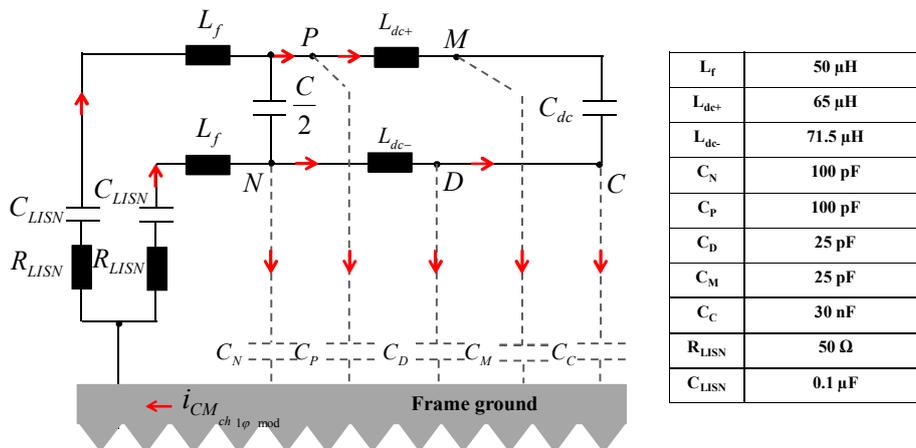


Fig.II.30. Impedances along the CM currents propagation paths (the noise sources such as the CSAR's common mode voltage generator as well as the Boost's are turned off). The numerical values are used for simulating the uneven inductances.

Fig.II.31 shows that even though high frequency emissions exist; however, their levels remain lower than in the conventional power circuit especially for frequencies lower than 1 MHz.

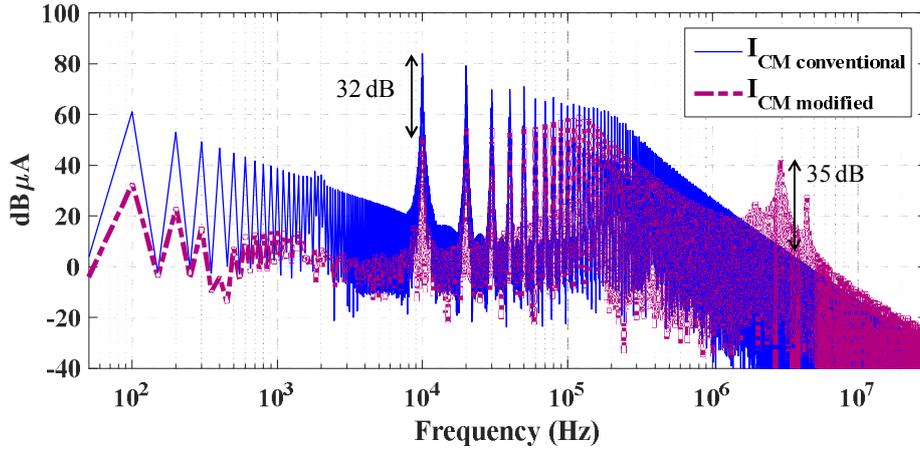


Fig.II.31. Simulation results for the modified structure with unbalanced dc inductors. Comparison of the spectral contents of the CM currents: (blood red) Modified power circuit with uneven dc inductors, (blue) Conventional unmodified power circuit.

The emissions that appear at higher frequencies (between 2 MHz and 5 MHz) are due to the dissymmetry of the structure (the dc side line inductances) which creates mixed-mode conducted EMI noise. A simplified CM admittance that takes into account the dissymmetry of the structure is computed in Appendix G. Its magnitude is given in Fig.II.32. This corroborates the high frequency CM current emissions seen in the red spectrum of Fig.II.31 at around 3 MHz.

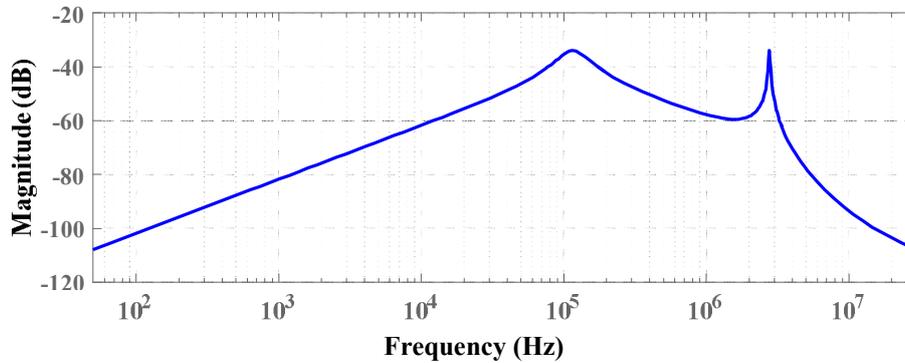


Fig.II.32. Bode plot of the CM admittance computed in case of an unevenly split dc inductor.

In fact, the CM emission's levels around 100 kHz are mainly due to the resonance between the dc-inductor placed on the negative dc bus ($L_{dc-} = 71.5 \mu H$) and the battery's stray capacitance (30 nF). However, the CM emissions around 3 MHz are likely due to the resonance of the LCL circuit formed between (L_f, C_p, L_{dc+}) for the CM current on the positive dc bus and (L_f, C_n, L_{dc-}) for the CM current on the negative dc bus. If we consider the equivalent circuit of the total common mode current, this translates into an LCL resonance between $(\frac{L_f}{2}, 2 \times C_p, \frac{L_{dc+} \times L_{dc-}}{L_{dc+} + L_{dc-}})$ and presents the following resonance frequency:

$$f_{res} = \frac{1}{2\pi} \cdot \sqrt{\frac{\frac{L_f}{2} + \frac{L_{dc+} \cdot L_{dc-}}{L_{dc+} + L_{dc-}}}{\frac{L_f}{2} \cdot \frac{L_{dc+} \cdot L_{dc-}}{L_{dc+} + L_{dc-}} \cdot 2 \cdot C_P}} = 2.96 \text{ MHz} \quad \text{eq. (II. 23)}$$

It should be noted that the attenuation levels indicated on the figures of the spectrums do not take into account the losses at high frequencies. In fact, the dc inductors are modeled as ideal components. A more thorough study should take into account the measured impedances of the dc inductors including their stray elements (equivalent parallel resistance and equivalent parallel capacitance) as well as a more thorough model of the propagation paths.

5.3.2. Different stray capacitances at the various nodes

The method has been developed, so far, by using equal stray capacitance values at nodes P & N (100 pF) and at nodes M & D (25 pF assuming a single Boost leg as in Fig.II.25). However, the stray capacitance at the anode of a diode differs from the stray capacitance developed at its cathode. Furthermore, the stray capacitances at the collector and emitter of an IGBT are not even (the same goes for the drain and source of a Mosfet). For instance, in a standard TO-247-3 package for discrete components such as Mosfets, the surfaces of the dies of the drain and the source are different with regards to the heatsink. As such, the source will exhibit a lower stray capacitance than that of the drain. Therefore we will consider that C_P & C_M are double the capacitances C_N & C_D respectively.

The simulation of the modified unbalanced power circuit is carried using the values defined in Fig.II.33.

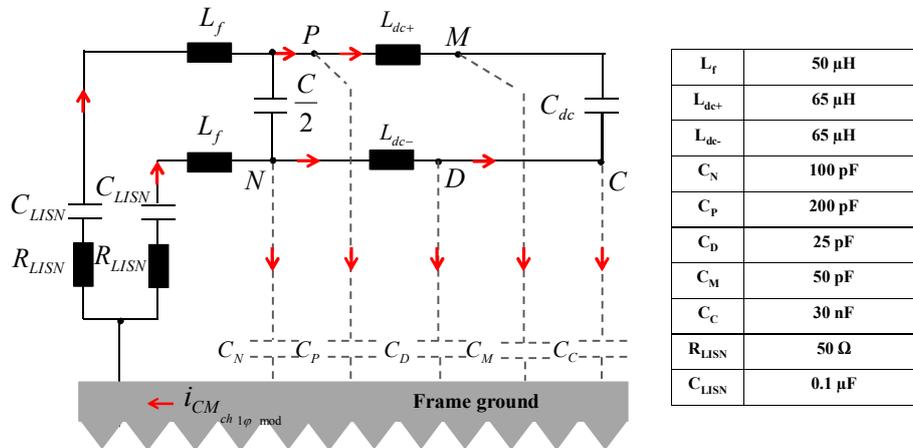


Fig.II.33. Impedances along the CM currents propagation paths (the noise sources such as the CSAR's common mode voltage generator as well as the Boost's are turned off). The numerical values are used for simulating the uneven stray capacitances.

Unlike in the previous case, in this study the power circuit is perfectly balanced ($L_{dc+} = L_{dc-}$). Therefore, the voltages across the stray capacitances at nodes P & M vary in opposition to the voltage fluctuations at nodes N & D respectively. However, the values of the stray capacitances are uneven; therefore, parts of the CM current generated are going to be compensated but others won't. The spectral content of the resulting CM current is given in Fig.II.34. The emissions that appear at higher

frequencies (between 1 MHz and 5 MHz) are due to the dissymmetry of the stray capacitances between the dc bus and the frame ground which creates mixed-mode conducted EMI noise.

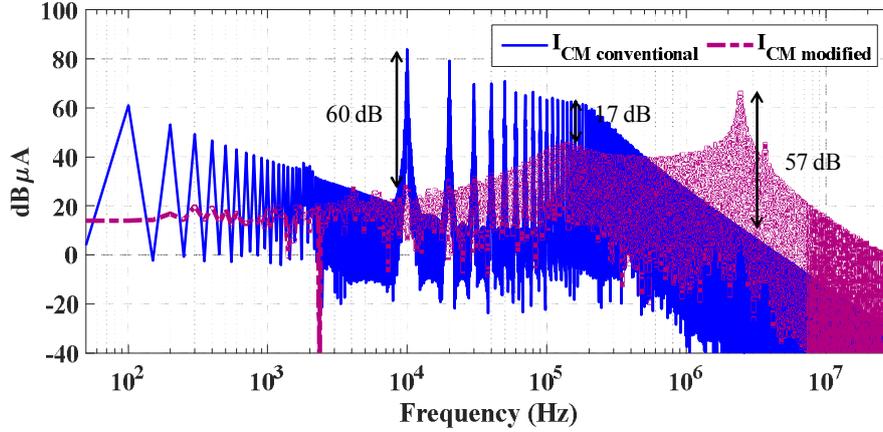


Fig.II.34. Simulation results for the modified structure with unbalanced stray capacitances. Comparison of the spectral contents of the CM currents: (blood red) Modified power circuit with unbalanced stray capacitances, (blue) Conventional unmodified power circuit.

The simplified CM admittance that takes into account the dissymmetry of the structure is computed in Appendix G. When applied to the case of unbalanced stray capacitances, its magnitude is given in Fig.II.35. It corroborates the high frequency CM current emissions seen in the red spectrum of Fig.II.34 at around 2 MHz.

In fact, the CM emissions at around 120 kHz are mainly due to the resonance between the dc-inductor placed on the negative dc bus ($L_{dc-} = 65 \mu H$) and the battery's stray capacitance ($30 nF$); whereas the emissions at higher frequencies at around 2.4 MHz are due to the equivalent LCL filter resonance. If we consider the equivalent circuit of the total common mode current, this translates into an LCL resonance between $(\frac{L_f}{2}, C_N + C_P, \frac{L_{dc+}}{2})$ and presents the following resonance frequency:

$$f_{res} = \frac{1}{2\pi} \cdot \sqrt{\frac{\frac{L_f}{2} + \frac{L_{dc+}}{2}}{\frac{L_f}{2} \cdot \frac{L_{dc+}}{2} \cdot (C_P + C_N)}} = 2.44 MHz \quad \text{eq. (II. 24)}$$

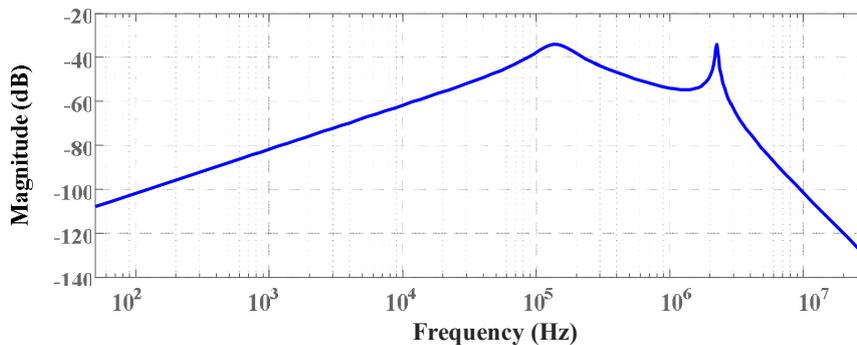


Fig.II.35. Bode plot of the CM admittance computed in case of unbalanced stray capacitances.

This is due to the L_{dc+} inductor that takes on a different value; it is calculated as such:

$$f_{res} = \frac{1}{2\pi} \cdot \sqrt{\frac{L_{dc+} + \frac{L_{EM}}{3}}{L_{dc+} \cdot \frac{L_{EM}}{3} \cdot C_{EM}}} = \frac{1}{2\pi} \cdot \sqrt{\frac{35\mu + 30\mu}{35\mu \times 30\mu \times 50p}} = 5.6MHz \quad \text{eq. (II. 26)}$$

The emissions that persist around 120 kHz are mainly due the resonance between the battery's stray capacitance (C_c) and the inductor placed on the negative dc bus L_{dc-} .

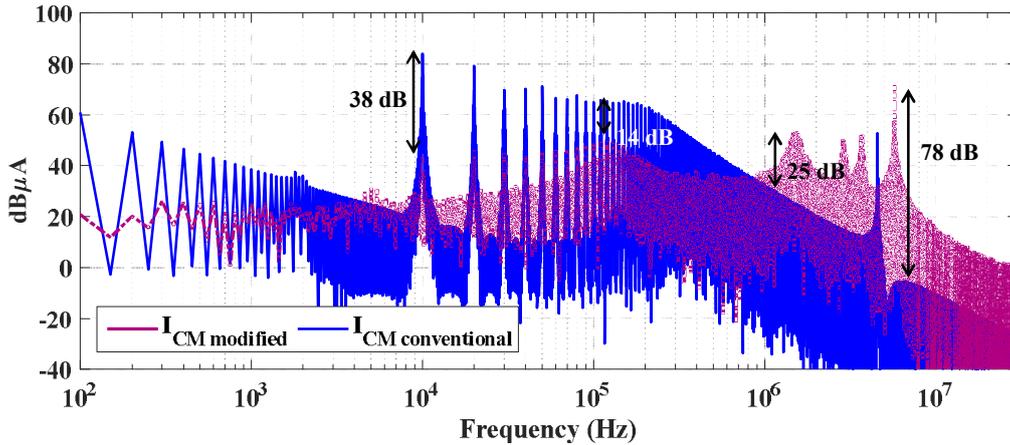


Fig.II.37. Simulation results for the modified structure with synchronous gating commands of the Boost legs. Comparison of the spectral contents of the CM currents: (blood red) Modified power circuit with synchronous commands, (blue) Conventional unmodified power circuit with synchronous commands.

B- Asynchronous commands

In order to study the impact of components dispersion, Fig.II.38 shows the effects of introducing a control delay, of 100 ns, on the gating signal of the second leg's switch. Compared to the previous study, it can be seen that the CM emissions' levels increase but remain lower than the ones found for the conventional power circuit for frequencies lower than 70 kHz. Beyond this frequency, the emissions exceed those obtained for the conventional power circuit. The presence of the electric machine coupled with the asynchronous commands of the Boost results in higher emissions.

Furthermore, the added diode used to balance the Boost's circuit works well for a single Boost leg or for synchronous three-Boost legs; however, when used with asynchronous commands, the ON-OFF states of the diode become dependent on all the legs' switching states which induces more voltage fluctuations at nodes C, M2 and EM.

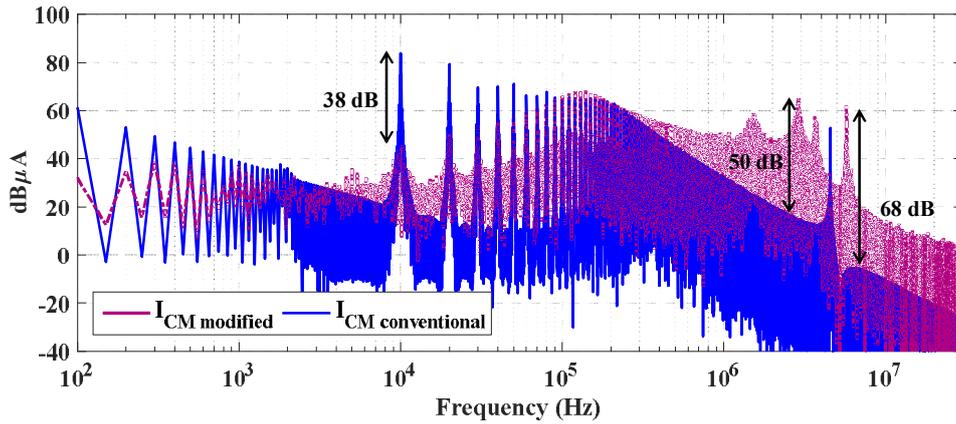


Fig.II.38. Simulation results for the modified structure with a delay of 500 ns in the gating signal of T_{bl2} . Comparison of the spectral contents of the CM currents: (blood red) Modified power circuit with command delays, (blue) Conventional unmodified power circuit.

C- Effect of interleaving

In order to study the effect of interleaving the three legs of the Boost, the same study has been carried with delays (of $\frac{T_{sw}}{3} = 33.4\mu s$ and $\frac{2 \cdot T_{sw}}{3} = 66.7\mu s$) introduced on the gating signals of the second and third Boost legs. Quite like the components' dispersion, it can be seen from the results in Fig.II.39 that interleaving results in higher high frequency emissions starting from 30 kHz. Although interleaving is quite interesting especially since it allows reducing the current ripple on the input side of the Boost; however, from a conducted common emissions point of view it presents a less favorable outcome.

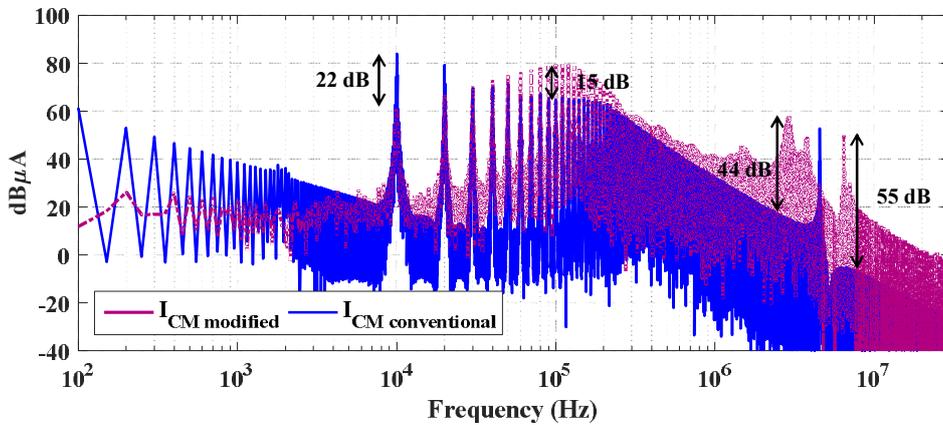


Fig.II.39. Simulation results for the modified structure with a delay of $40\mu s$ in the gating commands of T_{bl2} . Comparison of the spectral contents of the CM currents: (blood red) Modified power circuit with command delays, (blue) Conventional unmodified power circuit.

We can conclude from these studies that the presence of the electric machine in integrated chargers cannot be neglected from a common mode emissions standpoint. The high frequency emissions are mainly due to the presence of the electric machine's windings; this makes it necessary to study the deterioration of the windings and bearings of the machine in the case of integrated chargers. Moreover, interleaving seems like a more interesting solution for reducing the DM current ripple; however, it leads to higher CM conducted emissions. Furthermore, the balancing of the structure relies on a perfect synchronization of the commands of the three Boost legs. However, component dispersion reduces the efficiency of the proposed solutions especially for frequencies higher than 100 kHz.

6. Modified three-phase configuration

Before proceeding with this section, it should be noted that studying the EMI mitigation for three-phase structures is not an easy process and the solutions found in literature mainly focus on the space vector modulation strategies rather than on topological modifications.

The effectiveness of the modifications that have been verified for the single-phase configuration need to be proven for the mitigation of the conducted CM emissions of the three-phase charger. The latter is illustrated in Fig.II.40.

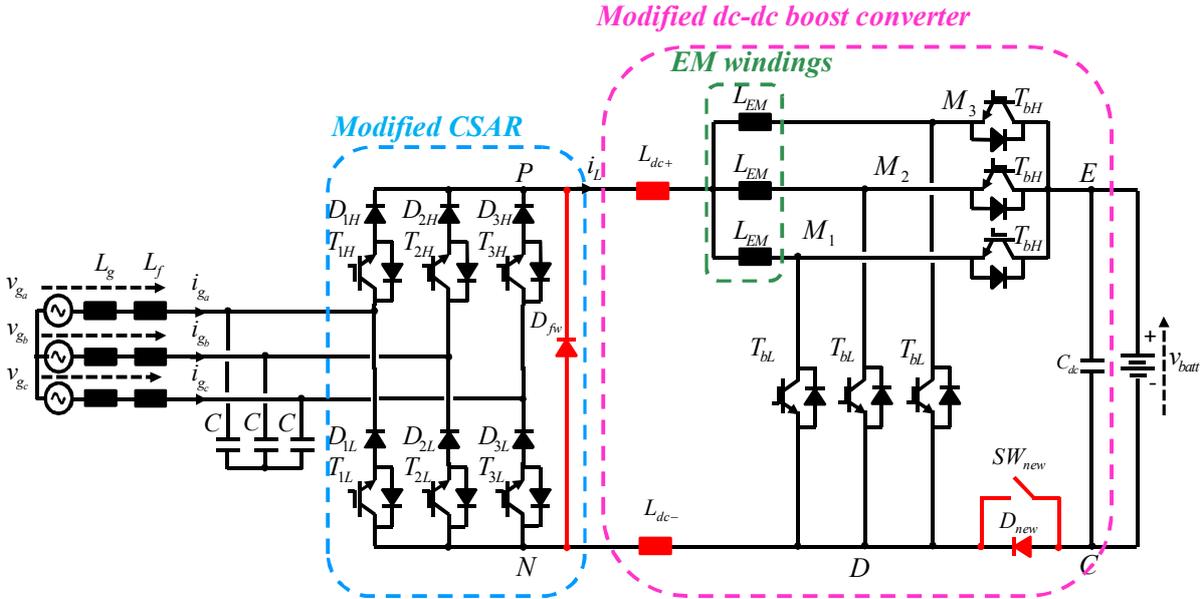


Fig.II.40. Power circuit of the modified three-phase charger to ensure balanced switching.

The dc-side of the charger remains the same regardless of the charging configuration. Therefore, the modification that needs investigating concerns the addition of the freewheeling diode to the output of the three-phase CSAR. Furthermore, the voltage across the battery’s stray capacitance (HVm) needs to be studied with regards to the modulation strategy chosen for the rectifier. The control strategy, used in Part B Chapter 1 is going to be implemented. As a reminder, this strategy does not use the Boost stage (it remains deactivated – low side IGBTs turned off), therefore, the rectifier’s modulation strategy is of great importance for the study of CM emissions.

6.1. Common Mode Reduction Modulation: effect on HVm

The fluctuations of HVm are inevitable when using modulation strategies for the active rectifier. We will start this section by studying the conventional topology of the charger with a modulation strategy, found in literature, developed specifically for the reduction of the fluctuations of HVm; afterwards, we will consider the modified structure for which we will implement the same modulation strategy followed by the analysis of the results obtained.

6.1.1. Conventional charger

The modulation strategy is presented by [Ripoll et al. 2014]. The study proposes several possible modulation schemes among which we chose to retain the switching sequences that minimize the voltage fluctuations at the negative-side of the dc bus. Therefore, we named this strategy Common Mode Reduction Modulation (CMRM). The choice of the CSAR's leg used for the freewheeling state is dependent on the sub-sector detected. In fact, the space-vector's hexagon is divided into three sections as shown in Fig.II.41. Each section delimits a zone where the nearest active vectors' low side switches are identical. Hence, the leg used for the freewheeling state in each of these sections is the one that keeps this low side switch turned on. The sequences applied in each sub-sector are presented in Table II. 13.

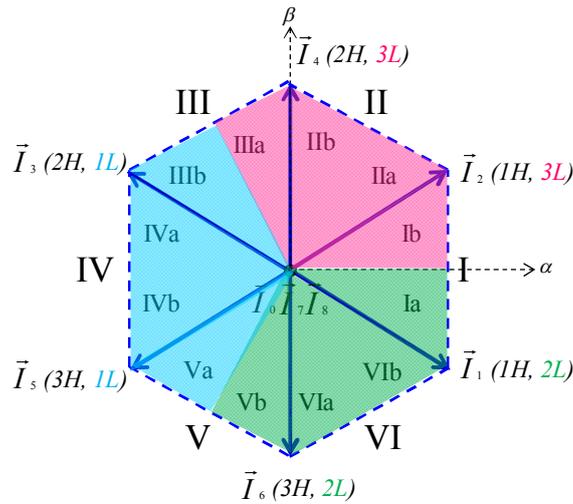


Fig.II.41. Choice of the rectifier leg for the freewheeling state in each subsector according to CMRM. (pink) Third leg (T_{3H} , T_{3L}). (cyan) First leg (T_{1H} , T_{1L}). (green) Middle leg (T_{2H} , T_{2L}).

By keeping the same low side switch turned on, the voltage at node N remains unchanged and directly linked to the corresponding mains phase voltage. Hence, in the even sectors (II, IV and VI), the CMRM induces no voltage fluctuations, at the switching frequency, at the negative side of the battery. Furthermore, this voltage's variations, in the odd sectors, are minimized by confining them between the negative grid voltages in each sub-sector (Fig.II.42). The CMRM strategy minimizes the voltage variations at the negative side of the battery; however, it does not deal with the conducted CM emissions generated at the internal nodes of the charger.

Table II. 13. SWITCHING SEQUENCES FOR THE CMRM

Sectors		Zero vector	CMRM	$v_N = HVm$	$CMV_{rect} = \frac{v_P + v_N}{2}$		
Switching sequences	I	Ia	\vec{I}_7	$[\vec{I}_1][\vec{I}_2][\vec{I}_1][\vec{I}_7]$	$[v_{gb}][v_{gc}][v_{gb}][v_{gb}]$	$[\frac{-v_{gc}}{2}][\frac{-v_{gb}}{2}][\frac{-v_{gc}}{2}][v_{gb}]$	
		Ib	\vec{I}_8	$[\vec{I}_2][\vec{I}_1][\vec{I}_2][\vec{I}_8]$	$[v_{gc}][v_{gb}][v_{gc}][v_{gc}]$	$[\frac{-v_{gb}}{2}][\frac{-v_{gc}}{2}][\frac{-v_{gb}}{2}][v_{gc}]$	
	II	IIa		$[\vec{I}_4][\vec{I}_2][\vec{I}_8]$	v_{gc}	$[\frac{-v_{ga}}{2}][\frac{-v_{gb}}{2}][v_{gc}]$	
		IIb		\vec{I}_0	$[\vec{I}_3][\vec{I}_4][\vec{I}_3][\vec{I}_8]$	$[v_{ga}][v_{gc}][v_{ga}][v_{gc}]$	$[\frac{-v_{gc}}{2}][\frac{-v_{ga}}{2}][\frac{-v_{gc}}{2}][v_{gc}]$
	III	IIIa			$[\vec{I}_4][\vec{I}_3][\vec{I}_4][\vec{I}_0]$	$[v_{gc}][v_{ga}][v_{gc}][v_{ga}]$	$[\frac{-v_{ga}}{2}][\frac{-v_{gc}}{2}][\frac{-v_{ga}}{2}][v_{ga}]$
		IIIb			IV	$[\vec{I}_5][\vec{I}_3][\vec{I}_0]$	v_{ga}
	IVa	$[\vec{I}_6][\vec{I}_5][\vec{I}_6][\vec{I}_0]$		$[v_{gb}][v_{ga}][v_{gb}][v_{ga}]$		$[\frac{-v_{ga}}{2}][\frac{-v_{gb}}{2}][\frac{-v_{ga}}{2}][v_{ga}]$	
	V	Va	\vec{I}_7	$[\vec{I}_5][\vec{I}_6][\vec{I}_5][\vec{I}_7]$	$[v_{ga}][v_{gb}][v_{ga}][v_{gb}]$	$[\frac{-v_{gb}}{2}][\frac{-v_{ga}}{2}][\frac{-v_{gb}}{2}][v_{gb}]$	
		Vb		VI	$[\vec{I}_1][\vec{I}_6][\vec{I}_7]$	v_{gb}	$[\frac{-v_{gc}}{2}][\frac{-v_{ga}}{2}][v_{gb}]$
	VI	VIa					
		VIb					

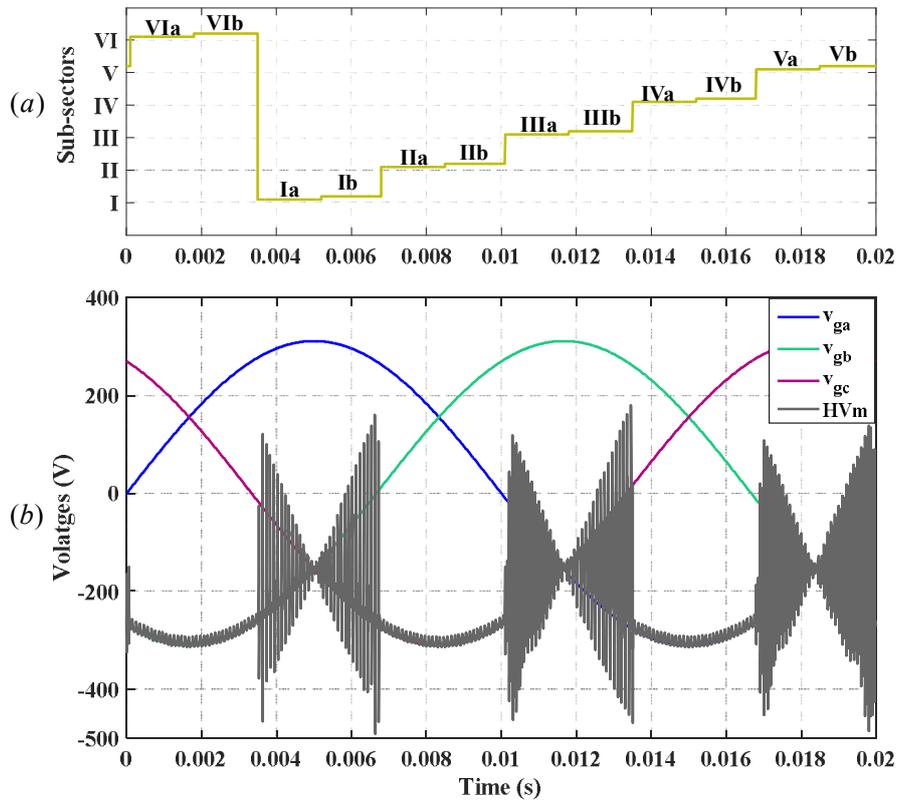


Fig.II.42. Conventional charger simulated with the CMRM strategy. (a) Detection of the sub-sectors. (b) Mains phase voltages and HVm.

6.1.2. Modified charger

The same modulation strategy is going to be applied to the modified structure and the conducted CM emissions are going to be compared with those of the conventional charger. Fig.II.43 shows the comparison between the levels of the conducted CM emissions in each case. It can be seen that the modulation strategies developed for the mitigation of the CM emissions are highly dependent on the structure of the charger. The CMRM is favorable in the case of the conventional topology; however, it generates more high frequency CM emissions when applied to the structurally modified charger. By examining Fig.II.44, we can deduce that the added freewheeling diode and the split inductor degrade the original positive effect of the CMRM on the stabilization of the CM emissions during the even sectors.

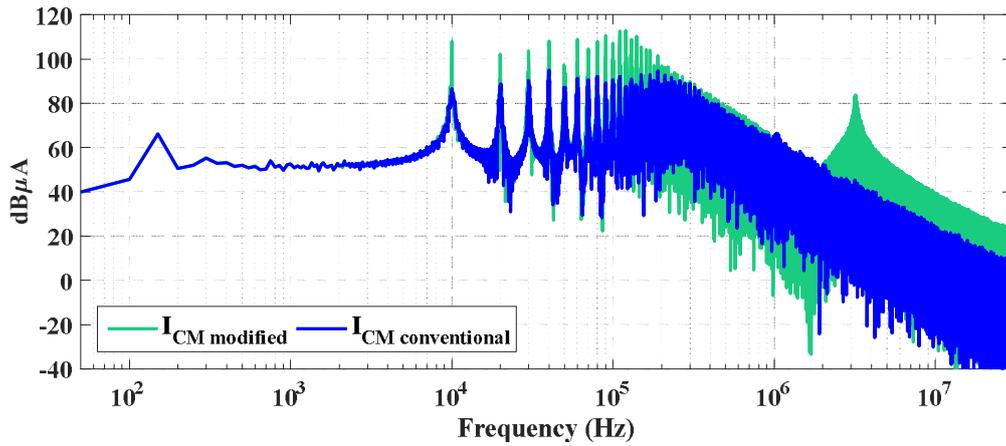


Fig.II.43. Simulation results regarding the spectral analysis of the CM emissions measured for the CMRM applied (blue) to the conventional three-phase structure, and (green) to the modified balanced three-phase charger.

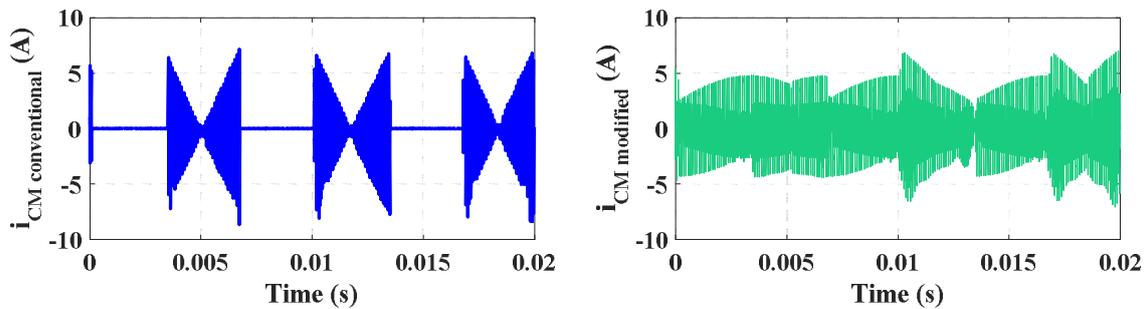


Fig.II.44. Simulation results regarding the waveforms of the CM emissions measured for the CMRM applied (blue) to the conventional three-phase structure, and (green) to the modified balanced three-phase charger.

6.2. Analysis

The topological modifications have been proposed to reduce the CM emissions at the internal nodes of the charger. In the single-phase charger, these modifications also minimize the fluctuations of HVm. In the three-phase configuration, the fluctuations of the battery's low side voltage across the stray capacitance is dominant (tens of nF) compared to the stray capacitances at the internal nodes of the

charger. Therefore, the main criteria for the modulation strategies should be, primarily, the reduction of the fluctuations of HVm.

In order to understand why the CMRM is not effective when used on the balanced structure, one should investigate the modified CSAR.

In fact, the freewheeling state is always achieved through the added freewheeling diode and not through the bridge legs. When a zero-vector is applied to the CSAR (i.e. two switches of the same bridge leg are turned-on), the voltage drops across the 4 switches of the closed bridge leg (2 diodes and 2 series IGBTs) cause the inductor current to flow through the freewheeling diode. Thus, decoupling the nodes P and N from the input mains phase voltages during freewheeling. Therefore, the added diode renders the voltages at the output nodes P and N as floating voltages during freewheeling. This neutralizes the effect of the CMRM during the even sectors and adds more fluctuations at the switching frequency at node N. This leads to fluctuations across HVm.

The freewheeling diode has been added, countless times in literature, at the output of various current source active rectifier topologies. However, to the author's knowledge, the impact of the freewheeling diode hasn't been studied before with regards to the CM emission levels nor with regards to the analysis of the voltage fluctuations at the internal nodes of a converter.

This issue will not be investigated any further; however, a solution might be found in adding a capacitive connection between the output dc bus and the star point of the input DM filtering capacitors. Such a connection will add internal filtering of the CM emissions without affecting HVm in the single-phase configuration.

7. Conclusion

It is more time consuming but less costly (on the long run) and more efficient for the EMC to take part of the design process of an industrial product. This is particularly necessary when it comes to conducted CM filtering for grid-tie converters. In fact, the classical solution that consists in using external filtering after the product has been designed can lead to voluminous passive elements in case of passive EMI filtering or higher ratings for the semi-conductors in case of active or hybrid EMI filtering.

Therefore, this chapter focuses on the mitigation of the conducted emissions as a way of re-integrating the EMI analysis in the design process of the non-isolated onboard integrated EV charger. A thorough review of the conducted CM current mitigation techniques for switch mode power supplies has been presented. Their compatibility with the topology of the EV charger has been analyzed. However, this study falls within the framework of strict industrial constraints, such as cost reduction, volume minimization, safety conditions, etc. Therefore, the solutions that fit within these requirements have been identified and applied to the dc-dc Buck and Boost converters. Studying these basic topologies is deemed necessary in order to allow for a better understanding of the CM generation mechanisms in the EV charger.

Based on this comprehensive state of the art, several efficient topological and control modifications were proposed for both charging configurations: single-phase and three-phase. Their positive effects on the reduction of the conducted CM emissions has been theoretically explained, modeled using the EMI modeling approach developed by this study and verified via simulation results.

This chapter’s contributions are in the field of conducted EMI mitigation. Not only did this study present a comprehensive analysis of the voltage fluctuations at critical nodes of the EV charger; it also provided numerous low cost solutions for the reduction of the conducted CM emissions. The volume and cost gains obtained by this approach can be evaluated once a new input EMI filter is designed with the lower conducted emissions achieved.

If the industrial constraints weren’t an issue, several additional mitigation techniques could have been proposed for this type of topology. They are illustrated in Fig.II.46 and resumed by the following:

Positive effect for CM mitigation of both single-phase and three-phase charging

- Hybrid CM & DM inductor (such as the inductor of Fig.II.45): magnetic integration of the dc-link inductor.

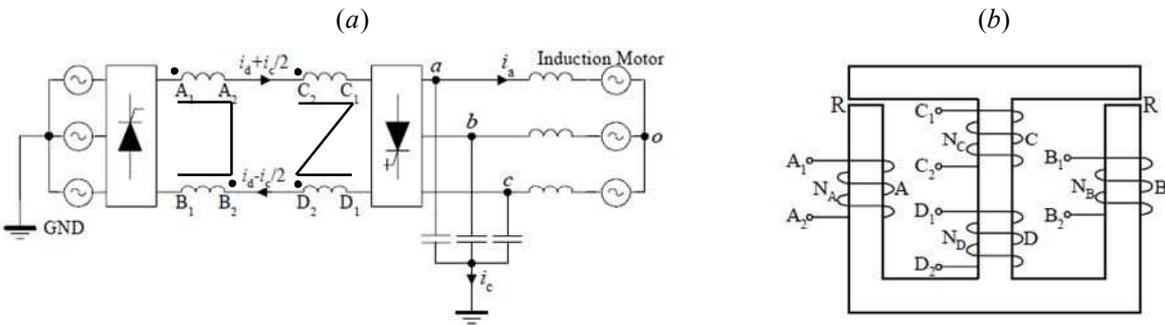


Fig.II.45. (a) Power circuit of a medium voltage drive with an integrated CM & DM dc choke. (b) Integrated dc choke according to [Wu et al. 2001].

- Compensation of the stray capacitance at the star connection of the electric machine's windings.

Positive effect for three-phase charging & neutral effect for single-phase charging

- Capacitive connection between the output and the star connection of the input DM filtering capacitors which should stabilize HVm.

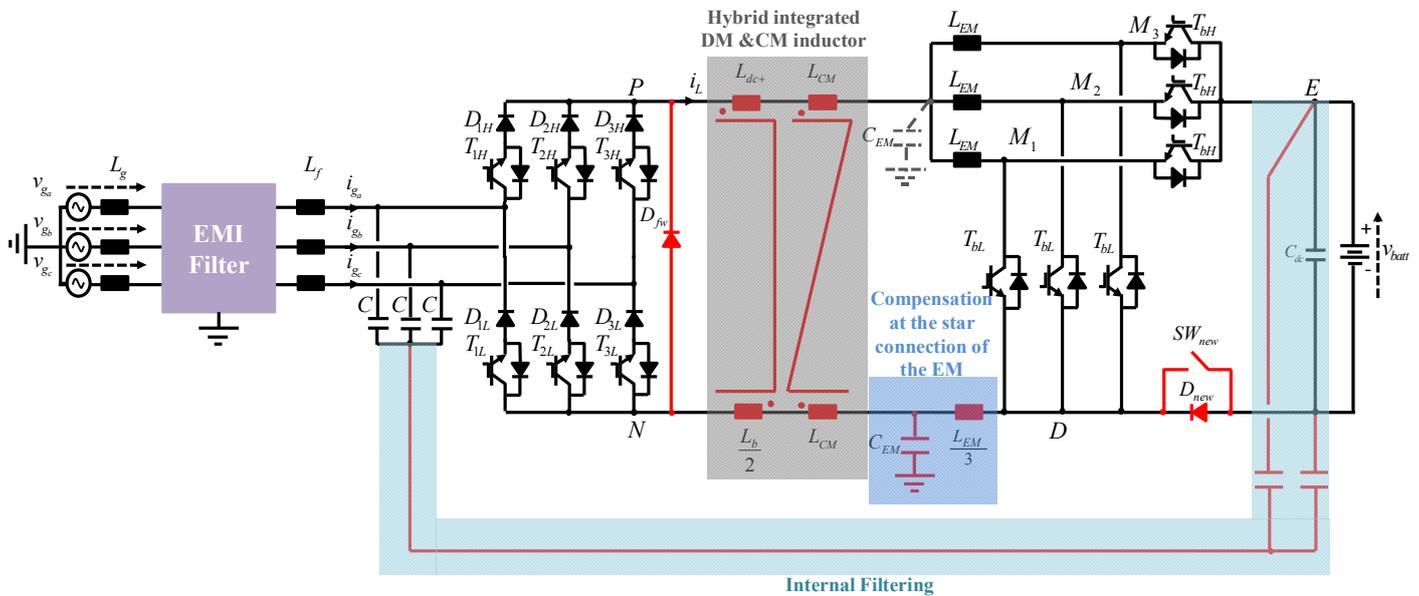


Fig.II.46. Other possible modifications to be applied to the EV charger for conducted CM mitigation.

Future work includes, but is not limited to, the experimental validation of the EMI modeling approach and the proposed solutions for the mitigation of the conducted CM emissions. The effect of delays in the gating signals of the three Boost legs on the emissions' levels can be studied. Moreover, the frequency range for which these solutions effectively reduce the CM emissions can be identified and linked to the dispersion that might exist between the split inductors and the values of the stray capacitances at the nodes presenting opposite voltage variations.

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General Conclusion

This work has been carried with the aim of reducing the low frequency harmonics and the high frequency emissions of an on-board integrated charger currently used for EVs in order to allow the design of a new, less voluminous and cheaper passive input EMI filter.

Grid power quality requirements for on-board EV chargers are defined through the IEC standards on harmonic current emissions. However, with the wide deployment of EVs, these standards are subject to future evolution covering a larger frequency band and stricter harmonic limits. Therefore, PFC battery chargers need to significantly enhance the quality of the current drawn from the grid.

In this scope, we proposed a new power factor correction control for the single-phase charging configuration. It allows the correction of the displacement power factor along with an active damping solution for the input filter's resonance. Furthermore, the averaged small-signal equivalent model of the converter is developed. It allows the study of the impact that the input filter has on the control stability. This shows the need to integrate the filter parameters in the design of the current controller. Moreover, the average current control is associated with an online detection mechanism that automatically switches between two different modes of operation. The dual-mode operation proposed allows the reduction of the switching losses as well as the reduction of the leakage currents. In addition, simulation results are validated through experimental findings. It is shown that the control proposed (Fig.1) achieves near unity displacement power factor. The input filter is effectively damped through a virtual resistor and the global PFC strategy is experimentally validated.

The proposed control reduces the switching power losses by commutating a single converter at each instant, reduces the conduction power losses by reducing the level of the dc-side inductor current, reduces the common mode conducted emissions by blocking the commutation of each converter over a fraction of the fundamental period, achieves closed-loop PFC control at the input side of the converter and gives way to the possibility of resizing the dc-side inductor for lower current levels.

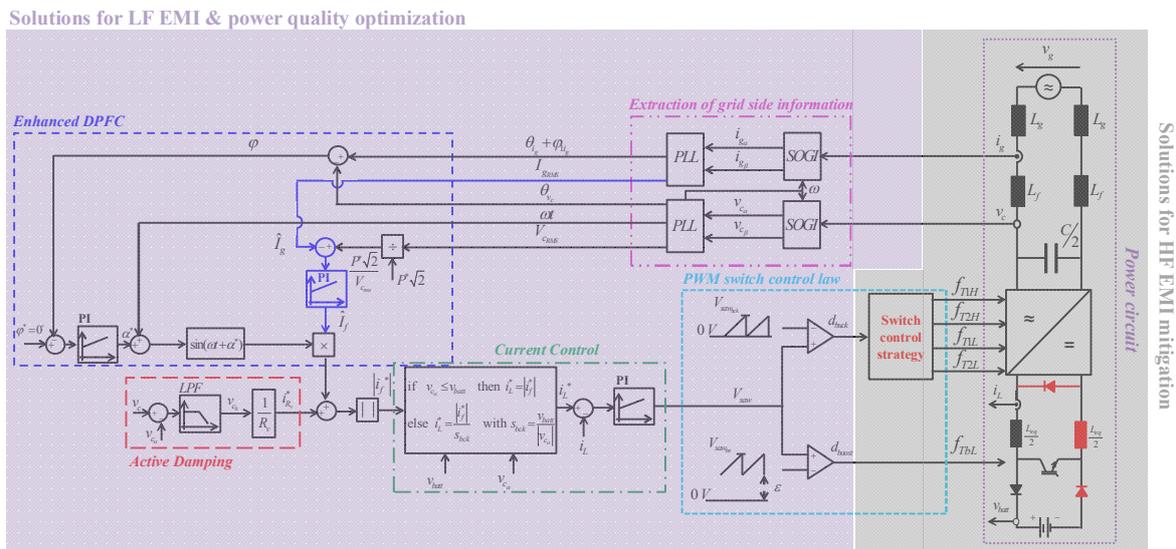


Fig.1. **Single-phase charging configuration:** Definition of the boundaries between the proposed solutions that fall within the HF emissions domain and what belongs to the LF power quality optimization.

For on-board chargers capable of accommodating three-phase very fast charging as well as single-phase slow charging, the three-phase control also needs to be considered.

For the grid-side performances, it is verified that the proposed three-phase PFC control ensures a near unity power factor, achieves compliance with the IEC 61000-3-12 standard, reduces the individual harmonics' levels up to rank 13, reduces the total harmonic distortion rate and minimizes the partial weighted harmonic distortion rate. Moreover, for the same charging power, the new PFC reduces the average value of the dc current flowing through the filtering inductor. This translates into lower switching and conduction power losses for the CSAR's semi-conductors as well as the possibility to increase the value of the dc-side inductor for the same inductor size. This can take part of future investigations and would allow the minimization of the dc current ripple. Furthermore, the new PFC does not activate the Boost converter for grid levels of 230 V_{RMS} and for fast charging power levels (22 kW & 43 kW). This means that the six switches of the Boost are maintained in the turn on/off position for the entire duration of the charge. These yields overall lower switching power losses. Moreover, we proposed a space vector modulation strategy that ensures both: low switching power losses and reduced voltage fluctuations of the dc- bus. Simulation results validate the performances of the control structure shown in Fig.2.

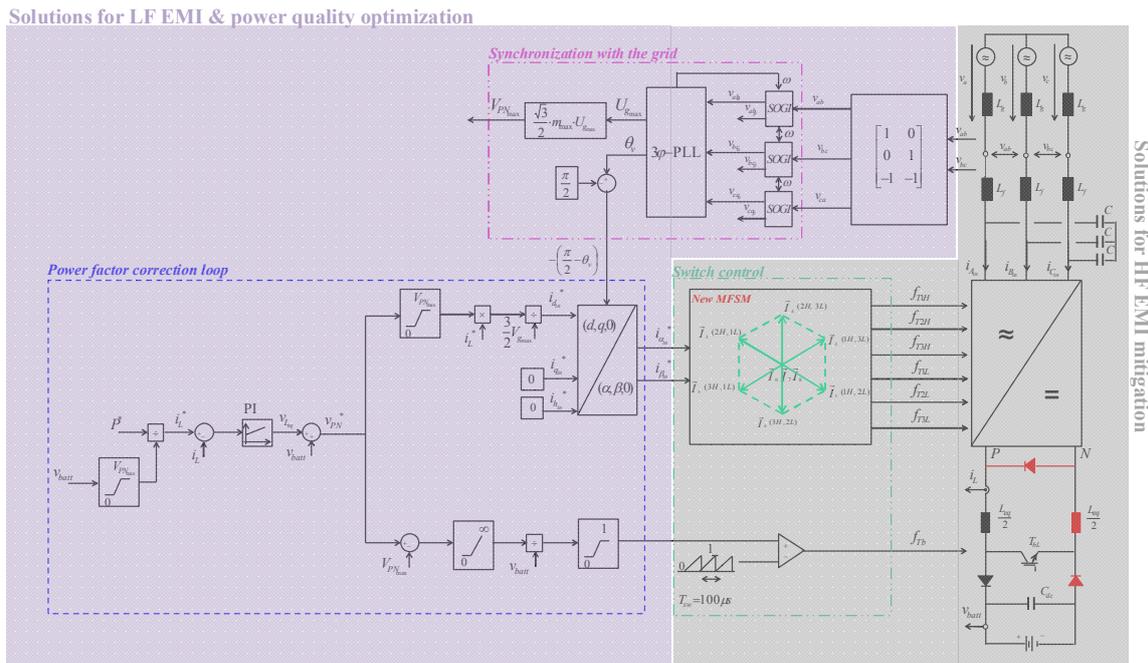


Fig.2. **Three-phase charging configuration:** Definition of the boundaries between the proposed solutions that fall within the HF emissions domain and what belongs to the LF power quality optimization.

Moreover, in this research, conducted EMI modelling is used to evaluate the impact that a topological or control modification has on the reduction of the CM emissions. Therefore, this study has presented a complete and rigorous conducted EMI modelling technique used for CM and DM emissions prediction. It has been verified that the approach allows the modelling of the internal noise sources and propagation paths of a power electronics converter. It is a predictive approach based on the prior knowledge of the switch control law of the converter(s). Furthermore, it can be used either in time-

domain or frequency-domain analysis. It has been applied to an on-board charger for EVs, in the single-phase and three-phase charging configurations, which verifies its chaining capability. Time-domain simulation results demonstrate the validity of the various developed models. The derived model can be used in the design and sizing of an optimal input EMI filter; even though precision in prediction is not fully required for such a task.

In order to integrate the EMI analysis in the design process of the non-isolated onboard integrated EV charger, we study different mitigation techniques for the conducted CM emissions. Based on a comprehensive state of the art, several efficient topological and control modifications were proposed for both charging configurations: single-phase and three-phase. Their positive effects on the reduction of the conducted CM emissions has been theoretically explained, modelled using the EMI modelling approach developed by this study and verified via simulation results for the single-phase configuration. Other modifications need to be considered for the mitigation of the conducted CM emissions in the three-phase configuration. The volume and cost gains obtained by the proposed modifications can be evaluated once a new input EMI filter is designed with the lower conducted emissions achieved.

The summary of the work achieved by this work and the main contributions are given in Fig.3. Future works include, but are not limited to:

- defining measurement protocols for the experimental validation of the proposed EMI models and the determination of the frequency range of validity;
- including a thorough EMI model of the battery that takes into account the state of charge for the study of the effects of the CM conducted emissions on the cells and modules;
- investigating the effects of high frequency emissions on the deterioration of the synchronous machine's windings and bearings;
- examining more structural modifications for the enhancement of the emissions in the three-phase configuration;
- using the combined CM and DM conducted EMI models in optimization algorithms for the design of a reduced size EMI filter;
- taking into account the parasitic elements of the passive EMI filter's components and the placement of the filter's elements which have an impact on the effectiveness of the filter's attenuations at high frequencies;
- designing an input EMI filter adaptable to both charging configurations (single-phase and three-phase) without requiring relays for the reconfiguration of the filter components: this should be tested by imagining new techniques for wiring, around the same magnetic core, the three windings of the CM filtering inductors (the same applies for the DM filtering inductors);
- studying the impact of the designed filter on the control stability by using the small-signal models developed for the single-phase and the three-phase charging configurations and re-adjusting the controllers' parameters accordingly;
- resizing the dc-side inductor;
- conducting efficiency studies and thermal measurements;

- testing the use of the third rectifier's bridge leg, in the single-phase configuration, either for active filtering by reducing the output voltage and input current ripples or for active CM cancellation;
- implementing the control strategies and the topological modifications on the developed SiC test bench in order to test the impact of higher switching frequencies on the grid-side power quality and the effects of faster commutations on the conducted CM emissions.

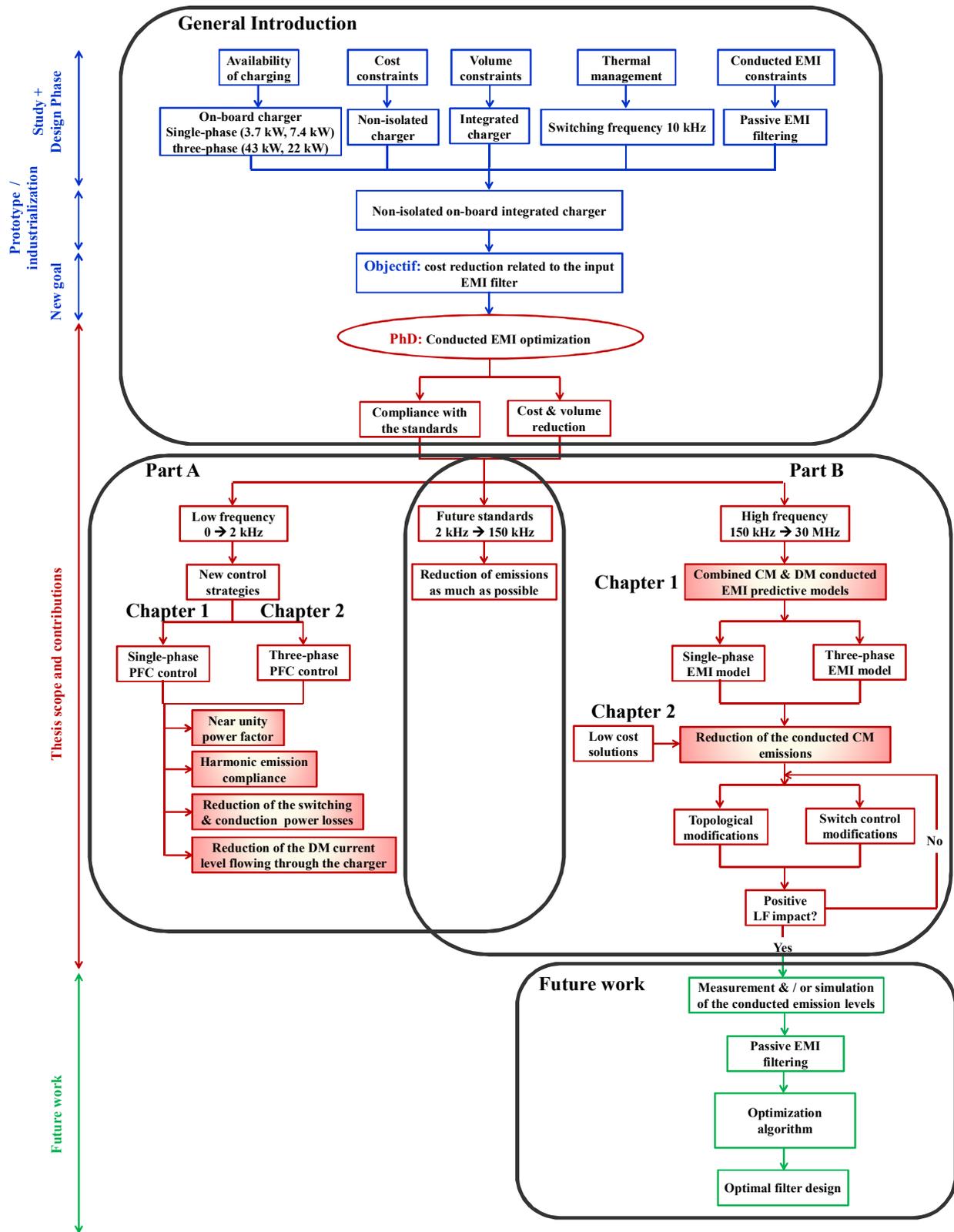


Fig.3. Overview of the charger design process and definition of the scope of this study.

Appendices

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Appendix A: Definition of the sub-sectors in case of a non-zero displacement angle

The modification of the internal and external boundaries to include the delay angle's effect:

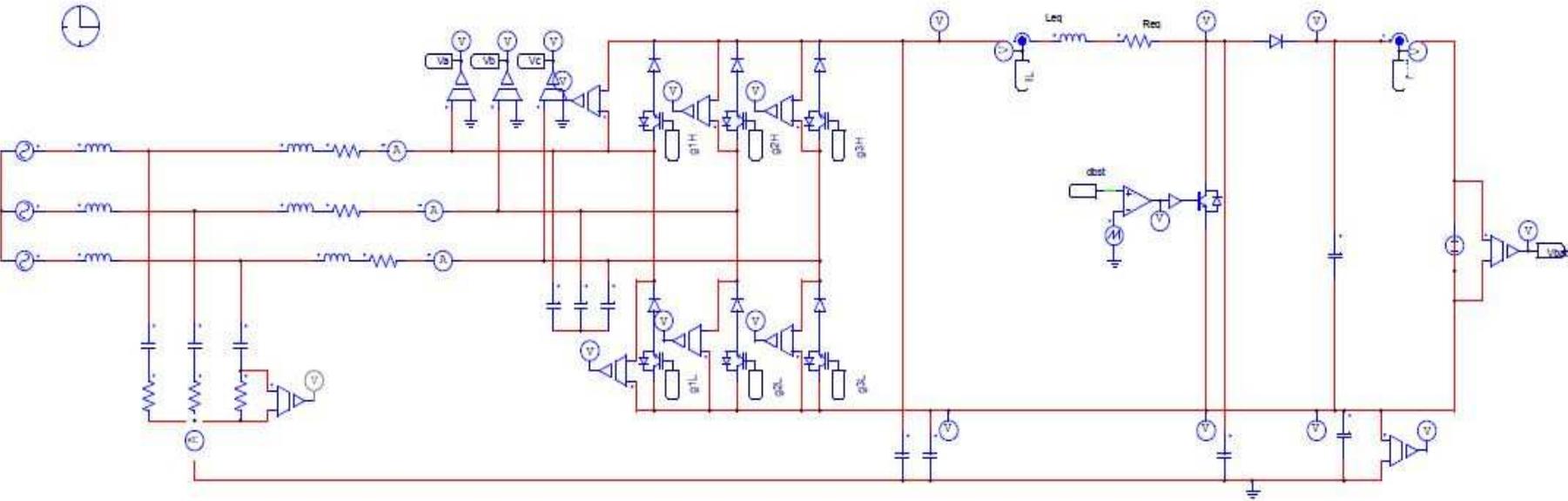
Table.1. IDENTIFICATION OF THE SUB-SECTORS WITH A DELAY ANGLE

Sector	Sub-Sector	Mains voltages	Central angle
I	Ia	$v_{a\alpha} > 0 > v_{c\alpha} > v_{b\alpha}$	$-\frac{\pi}{6} < \theta \leq -\alpha$
		$v_{a\alpha} > 0 > v_{b\alpha} > v_{c\alpha}$	$-\alpha < \theta \leq 0$
	Ib	$v_{a\alpha} > 0 > v_{b\alpha} > v_{c\alpha}$	$0 < \theta \leq +\frac{\pi}{6} - \alpha$
		$v_{a\alpha} > v_{b\alpha} > 0 > v_{c\alpha}$	$+\frac{\pi}{6} - \alpha < \theta \leq +\frac{\pi}{6}$
II	IIa	$v_{a\alpha} > v_{b\alpha} > 0 > v_{c\alpha}$	$+\frac{\pi}{6} < \theta \leq +\frac{\pi}{3} - \alpha$
		$v_{b\alpha} > v_{a\alpha} > 0 > v_{c\alpha}$	$-\alpha < \theta \leq +\frac{\pi}{3}$
	IIb	$v_{b\alpha} > v_{a\alpha} > 0 > v_{c\alpha}$	$+\frac{\pi}{3} < \theta \leq +\frac{\pi}{2} - \alpha$
		$v_{b\alpha} > 0 > v_{a\alpha} > v_{c\alpha}$	$+\frac{\pi}{2} - \alpha < \theta \leq +\frac{\pi}{2}$
III	IIIa	$v_{b\alpha} > 0 > v_{a\alpha} > v_{c\alpha}$	$+\frac{\pi}{2} < \theta \leq +\frac{2\pi}{3} - \alpha$
		$v_{b\alpha} > 0 > v_{c\alpha} > v_{a\alpha}$	$+\frac{2\pi}{3} - \alpha < \theta \leq +\frac{2\pi}{3}$
	IIIb	$v_{b\alpha} > 0 > v_{c\alpha} > v_{a\alpha}$	$+\frac{2\pi}{3} < \theta \leq +\frac{5\pi}{6} - \alpha$
		$v_{ab} > v_{c\alpha} > 0 > v_{a\alpha}$	$+\frac{5\pi}{6} - \alpha < \theta \leq +\frac{5\pi}{6}$
IV	IVa	$v_{ab} > v_{c\alpha} > 0 > v_{a\alpha}$	$+\frac{5\pi}{6} < \theta \leq +\pi - \alpha$
		$v_{c\alpha} > v_{b\alpha} > 0 > v_{a\alpha}$	$+\pi - \alpha < \theta \leq +\pi$
	IVb	$v_{c\alpha} > v_{b\alpha} > 0 > v_{a\alpha}$	$-\pi < \theta \leq -\frac{5\pi}{6} + \alpha$
		$v_{c\alpha} > 0 > v_{b\alpha} > v_{a\alpha}$	$-\frac{5\pi}{6} + \alpha < \theta \leq -\frac{5\pi}{6}$
V	Va	$v_{c\alpha} > 0 > v_{b\alpha} > v_{a\alpha}$	$-\frac{5\pi}{6} < \theta \leq -\frac{2\pi}{3} + \alpha$
		$v_{c\alpha} > 0 > v_{a\alpha} > v_{b\alpha}$	$-\frac{2\pi}{3} + \alpha < \theta \leq -\frac{2\pi}{3}$
	Vb	$v_{c\alpha} > 0 > v_{a\alpha} > v_{b\alpha}$	$-\frac{2\pi}{3} < \theta \leq -\frac{\pi}{2} + \alpha$
		$v_{c\alpha} > v_{a\alpha} > 0 > v_{b\alpha}$	$-\frac{\pi}{2} + \alpha < \theta \leq -\frac{\pi}{2}$
VI	VIa	$v_{c\alpha} > v_{a\alpha} > 0 > v_{b\alpha}$	$-\frac{\pi}{2} < \theta \leq -\frac{\pi}{3} + \alpha$
		$v_{a\alpha} > v_{c\alpha} > 0 > v_{b\alpha}$	$-\frac{\pi}{3} + \alpha < \theta \leq -\frac{\pi}{3}$
	VIb	$v_{a\alpha} > v_{c\alpha} > 0 > v_{b\alpha}$	$-\frac{\pi}{3} < \theta \leq -\frac{\pi}{6} + \alpha$
		$v_{a\alpha} > 0 > v_{c\alpha} > v_{b\alpha}$	$-\frac{\pi}{6} + \alpha < \theta \leq -\frac{\pi}{6}$

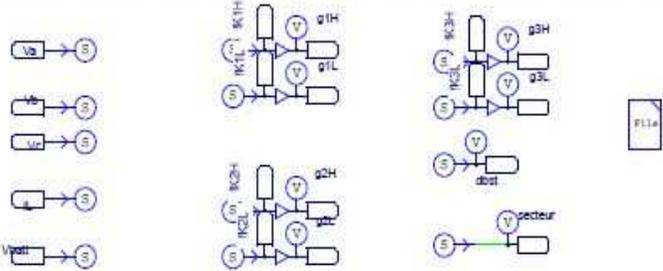
Appendix B: Example of a MATLAB/PSIM co-simulation used in this Chapter

❖ The power circuit implemented, inside the SimCoupler Module, using PSIM 9.1.3 is shown below:

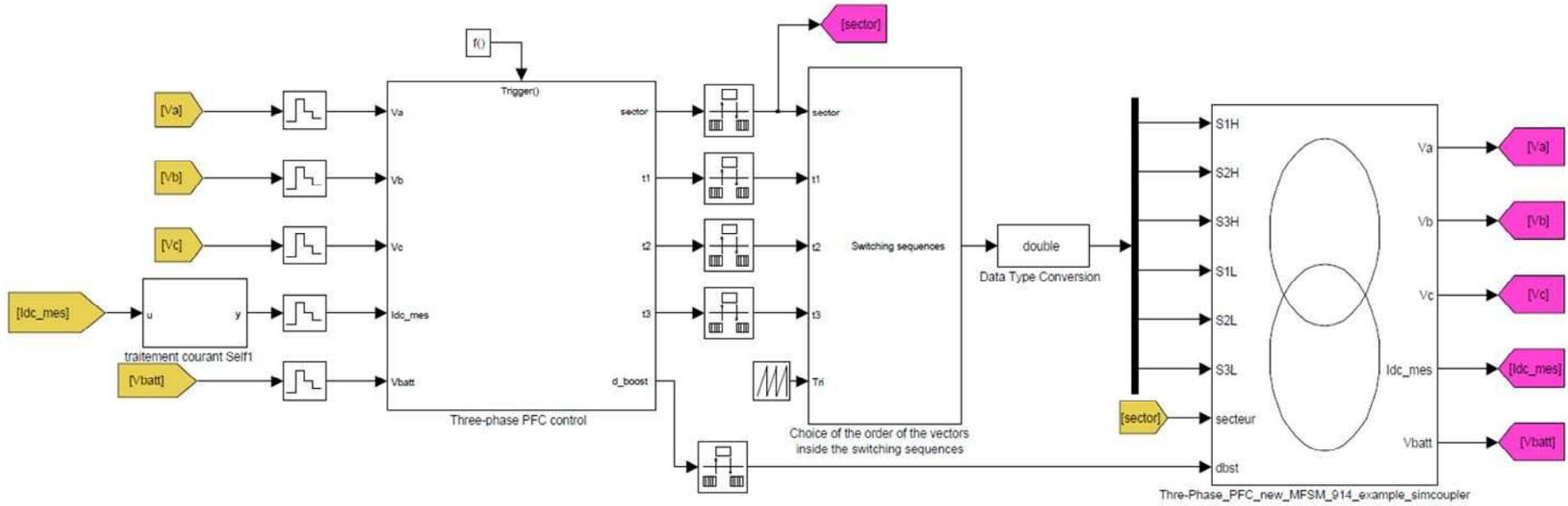
Three-Phase_PFC_new_MFSM_914_example_simcoupler



Three-Phase Control through co-simulation with MATLAB



❖ The PFC control and the current modulation strategy implemented under MATLAB/Simulink:



Appendix C: Small signal model of the three-phase charger with an (L,C) input filter

The control design can be based either on a dc-side current or an ac-side current control loop.

❖ State of the art models for a dc-side current control

If the PFC strategy is based on the dc-side current control, a small signal model of the charger can be computed by linearization of an equivalent dc-to-dc model of the three-phase rectifier.

This method of modeling has been presented by [Nussbaumer et al. 2005]. The authors develop the linearized small-signal model of a Voltage Range Extended 4-Switch Current Source Rectifier (VRX-4) given in Fig.1.

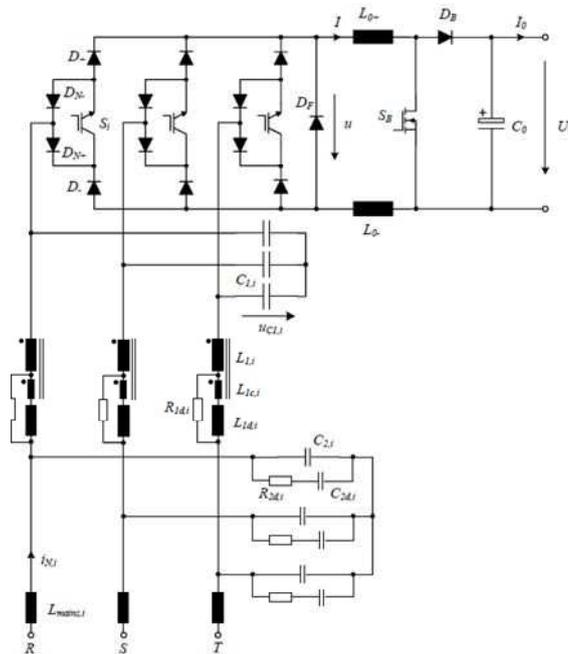


Fig.1. Topology of the VRX-4 including: an input EMI filter, a three-phase three-switch Buck-type rectifier and a Boost output stage [Nussbaumer et al. 2005].

In fact, for a dc-side control the three-phase ac-dc Buck-type rectifier stage shows similar behavior as a simple dc-dc Buck converter with a suitable dc input voltage and appropriate values of the input filter's components. The equivalent dc-dc model of the converter is shown in Fig.2 (a). The linearization of this model leads to the small signal model of the converter given in Fig.2 (b).

❖ State of the art models for an ac-side current control

If the ac-side currents are considered for the PFC control of an active three-phase rectifier, a small-signal model in the (d, q) reference frame allows the extraction of the control transfer functions along the d-axis (for active power control) and along the q-axis (for reactive power control).

Average models in the (d, q) frame have been developed for Boost type three-phase rectifiers [Mao et al. 1998] as well as Buck-type [Gandoy et al. 2000] - [Hiti et al. 1994] as shown in Fig.3.

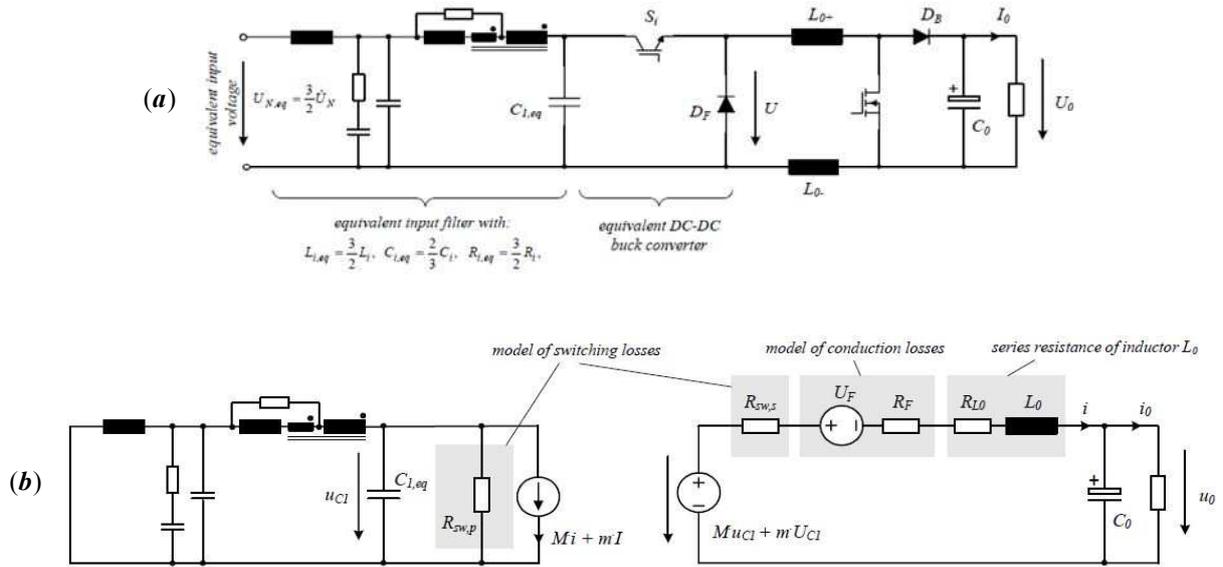


Fig.2. (a) dc-dc model of the VRX-4 system with equivalent input parameters; (b) linearized small signal model of the converter and equivalent resistors modeling switching and conduction losses [Nussbaumer et al. 2005].

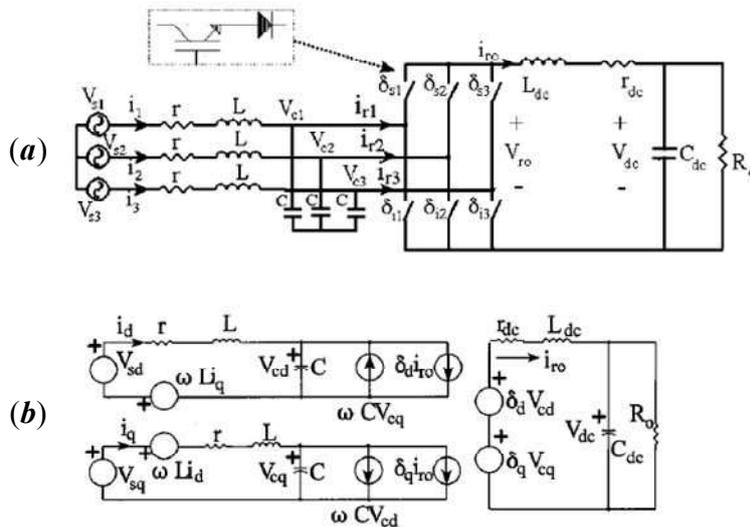


Fig.3. (a) Three-phase six-switch CSAR; (b) circuit representation of the average time-invariant (d, q) model. [Gandoy et al. 2000].

❖ The developed small-signal linearized model of the charger in the rotating (d, q) reference frame

The model developed by this study is a small-signal linearized model in the (d, q) reference frame. We will consider an (L, C) input filter. The same analysis can be used to model an input filter consisting of multiple stages. Even though our PFC strategy controls the dc-side current; the model is developed in

the (d, q) frame because the control of the active power is developed along the d-axis. Eventually, this model will allow the control of the displacement power factor along the q-axis.

The model is based on the following mathematical computations while assuming a balanced three-phase system (i.e. the zero sequence quantities are considered to be equal to zero). By applying the Park transform to the rectifier's input currents, we can deduce:

$$\begin{bmatrix} i_{d_{in}} \\ i_{q_{in}} \end{bmatrix} = \begin{bmatrix} d_d \\ d_q \end{bmatrix} \cdot i_L \quad \text{eq. (1)}$$

Moreover, the Park transform applied to the input power yield:

$$P_{ch} = [v_a \quad v_b \quad v_c] \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \frac{3}{2} \cdot (v_d \cdot i_d + v_q \cdot i_q) \quad \text{eq. (2)}$$

By assuming the conservation of the input power, at the output of the input filter and the output of the rectifier, one can deduce:

$$P_{ch} = \frac{3}{2} \cdot (v_{d_{in}} \cdot i_{d_{in}} + v_{q_{in}} \cdot i_{q_{in}}) = v_{PN} \cdot i_L \quad \text{eq. (3)}$$

However, using the Park transform yields:

$$v_{PN} = \frac{3}{2} \cdot (v_{d_{in}} \cdot d_d + v_{q_{in}} \cdot d_q) \quad \text{eq. (4)}$$

Kirchhoff's voltage law applied to the dc-side leads to:

$$L_{eq} \cdot \frac{di_L}{dt} + R_{eq} \cdot i_L = v_{PN} - v_{MD} \quad \text{eq. (5)}$$

By using eq. (1) and by replacing eq. (4) into eq. (5) and separating the d-axis from the q-axis variables, we can define the following systems of equations:

$$\begin{cases} d - axis : \begin{cases} i_{d_{in}} = d_d \cdot i_L \\ L_{eq} \cdot \frac{di_L}{dt} + R_{eq} \cdot i_L = \frac{3}{2} \cdot v_{d_{in}} \cdot d_d - v_{MD} \end{cases} \\ q - axis : \begin{cases} i_{q_{in}} = d_q \cdot i_L \\ L_{eq} \cdot \frac{di_L}{dt} + R_{eq} \cdot i_L = \frac{3}{2} \cdot v_{q_{in}} \cdot d_q - v_{MD} \end{cases} \end{cases} \quad \text{eq. (6)}$$

The small signal analysis of the converter allows for the linearization around a given operating point. Therefore, we will apply the first order small-signal linearization to eq. (6) by replacing each variable y by its variation \hat{y} around a steady-state value Y :

$$\begin{cases}
d - axis : \left\{ \begin{array}{l} (I_{d_{in}} + \tilde{i}_{d_{in}}) = (D_d + \tilde{d}_d) \cdot (I_L + \tilde{i}_L) \\ L_{eq} \cdot \frac{d(I_L + \tilde{i}_L)}{dt} + R_{eq} \cdot (I_L + \tilde{i}_L) = \frac{3}{2} \cdot (V_{d_{in}} + \tilde{v}_{d_{in}}) \cdot (D_d + \tilde{d}_d) - (V_{MD} + \tilde{v}_{MD}) \end{array} \right. & \text{eq. (7)} \\
q - axis : \left\{ \begin{array}{l} (I_{q_{in}} + \tilde{i}_{q_{in}}) = (D_q + \tilde{d}_q) \cdot (I_L + \tilde{i}_L) \\ L_{eq} \cdot \frac{d(I_L + \tilde{i}_L)}{dt} + R_{eq} \cdot (I_L + \tilde{i}_L) = \frac{3}{2} \cdot (V_{q_{in}} + \tilde{v}_{q_{in}}) \cdot (D_q + \tilde{d}_q) - (V_{MD} + \tilde{v}_{MD}) \end{array} \right.
\end{cases}$$

The separation of the dc and ac state variables along each axis yields the following ac small-signal linearized model of the three-phase rectifier:

$$\begin{cases}
d - axis : \left\{ \begin{array}{l} \tilde{i}_{d_{in}} = D_d \cdot \tilde{i}_L + \tilde{d}_d \cdot I_L \\ L_{eq} \cdot \frac{d\tilde{i}_L}{dt} + R_{eq} \cdot \tilde{i}_L = \frac{3}{2} \cdot \tilde{v}_{d_{in}} \cdot D_d + \frac{3}{2} \cdot V_{d_{in}} \cdot \tilde{d}_d - \tilde{v}_{MD} \end{array} \right. & \text{eq. (8)} \\
q - axis : \left\{ \begin{array}{l} \tilde{i}_{q_{in}} = D_q \cdot \tilde{i}_L + \tilde{d}_q \cdot I_L \\ L_{eq} \cdot \frac{d\tilde{i}_L}{dt} + R_{eq} \cdot \tilde{i}_L = \frac{3}{2} \cdot \tilde{v}_{q_{in}} \cdot D_q + \frac{3}{2} \cdot V_{q_{in}} \cdot \tilde{d}_q - \tilde{v}_{MD} \end{array} \right.
\end{cases}$$

The linearization takes place around the following operating point:

$$\begin{cases}
d - axis : \left\{ \begin{array}{l} I_{d_{in}} = D_d \cdot I_L \\ R_{eq} \cdot I_L = \frac{3}{2} \cdot V_{d_{in}} \cdot D_d - V_{MD} \end{array} \right. & \text{eq. (9)} \\
q - axis : \left\{ \begin{array}{l} I_{q_{in}} = D_q \cdot I_L \\ R_{eq} \cdot I_L = \frac{3}{2} \cdot V_{q_{in}} \cdot D_q - V_{MD} \end{array} \right.
\end{cases}$$

The small-signal model of the Boost output stage does not vary from the one developed in the single-phase configuration.

Based on these equations the Buck-type rectifier input stage and the Boost output converter can be represented by the model in Fig.4.

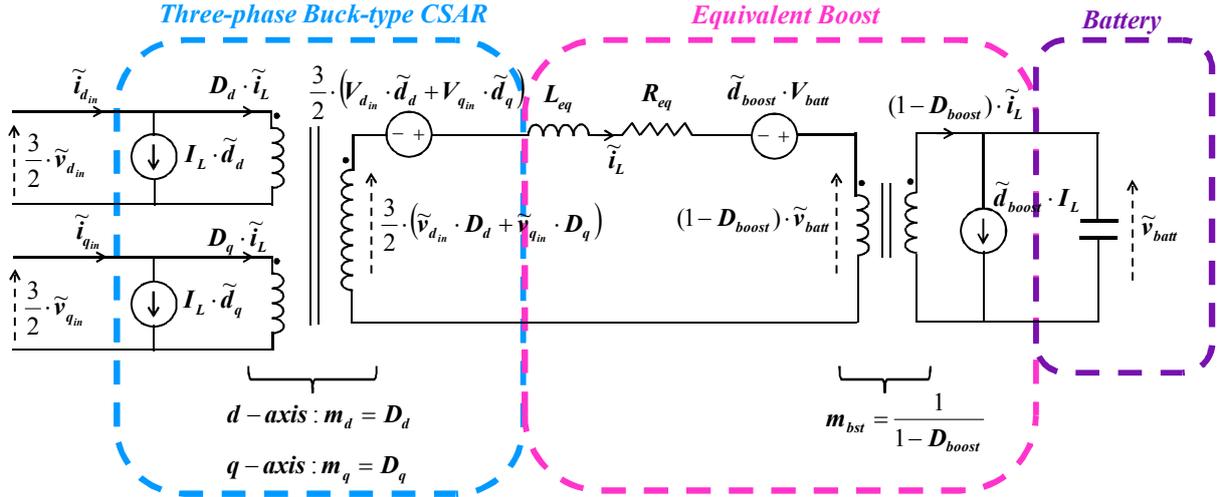


Fig.4. Linearized small-signal model, the (d, q) rotating frame, of the three-phase Buck-type rectifier input stage and the Boost output converter.

The basic model of a three-phase input (L, C) filter in the (d, q) rotating reference frame is given in Fig.3 (b). When coupled to the converter's model of Fig.4, the global small-signal model of the three-phase charger is deduced:

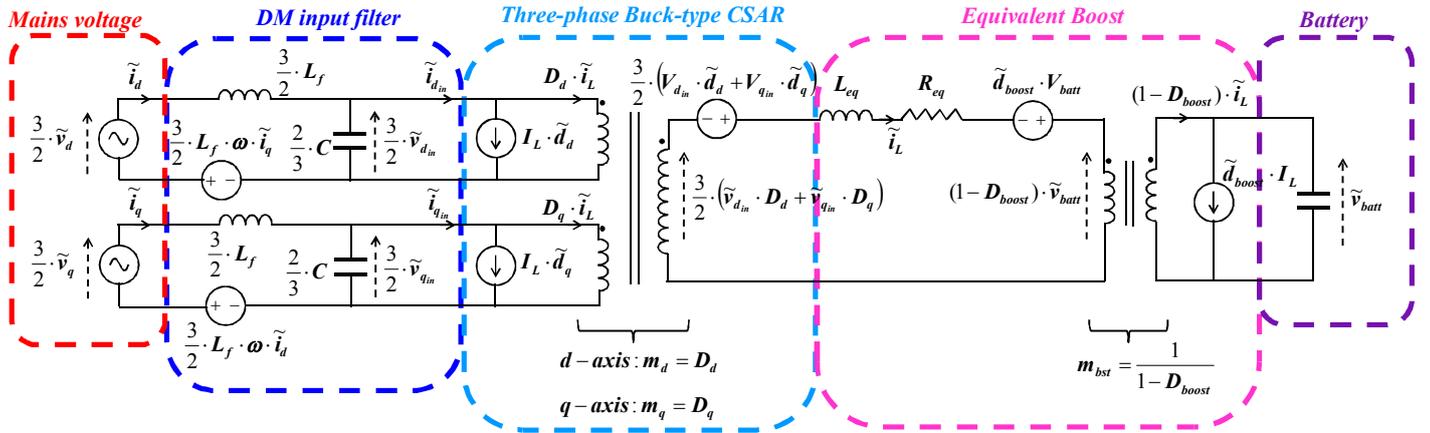


Fig.5. Small signal model of the three-phase charger configuration in the (d, q) reference frame.

The coefficients given to the DM input filter's elements are deduced from the conservation of the amount of energy stored in the input filter's inductors and capacitors between the (d, q) and the (a, b, c) models [Nussbaumer et al. 2002]. For instance, the coefficient of the DM filtering capacitor C is determined as following:

$$\begin{aligned}
E_C &= \frac{1}{2} \cdot C \cdot (V_{g_{\max}} \cdot \sin(\theta_v))^2 + \frac{1}{2} \cdot C \cdot \left(V_{g_{\max}} \cdot \sin\left(\theta_v - \frac{2\pi}{3}\right) \right)^2 + \frac{1}{2} \cdot C \cdot \left(V_{g_{\max}} \cdot \sin\left(\theta_v + \frac{2\pi}{3}\right) \right)^2 \\
&= \frac{1}{2} \cdot x \cdot C \cdot \left(\frac{3}{2} \cdot V_d \right)^2 + \frac{1}{2} \cdot x \cdot C \cdot \left(\frac{3}{2} \cdot V_q \right)^2 \\
&= \frac{3}{4} \cdot C \cdot V_{g_{\max}}^2
\end{aligned} \tag{10}$$

$$\begin{aligned}
E_L &= \frac{1}{2} \cdot L_f \cdot (I_{g_{\max}} \cdot \sin(\theta_v - \varphi))^2 + \frac{1}{2} \cdot L_f \cdot \left(I_{g_{\max}} \cdot \sin\left(\theta_v - \frac{2\pi}{3} - \varphi\right) \right)^2 + \frac{1}{2} \cdot L_f \cdot \left(I_{g_{\max}} \cdot \sin\left(\theta_v + \frac{2\pi}{3} - \varphi\right) \right)^2 \\
&= \frac{1}{2} \cdot y \cdot L_f \cdot (I_d)^2 + \frac{1}{2} \cdot y \cdot L_f \cdot (I_q)^2 \\
&= \frac{3}{4} \cdot L_f \cdot I_{g_{\max}}^2
\end{aligned} \tag{11}$$

Knowing that $V_d = V_{gm}$, $V_q = 0$, $I_d = I_{g_{\max}}$ and $I_q = 0$, we can deduce that $x = \frac{2}{3}$ and $x = \frac{3}{2}$.

This model can also be used to study the input displacement power factor defined only at the line frequency (between the fundamental components of the line current and phase voltage). Therefore, in order to design a phase-shift compensation loop, the input filter's model at frequencies close to the line frequency is sufficient [Hiti et al. 1994]. At these frequencies the impedance of the input filter's series inductors can be neglected. Furthermore, if the input filter has more than one stage, the impedances of all the series inductors can still be neglected at the line frequency, so that the filter is modeled by an equivalent capacitor that represents the sum of all the parallel capacitors per phase of the input filter.

Appendix D: Modeling of the traction's inverter used as a dc-dc Boost converter

In this section, the combined CM & DM conducted EMI model of the traction's two-level three-phase inverter used as a dc-dc Boost converter is developed Fig.6. The model allows the analysis of the effect that interleaving the Boost legs can have on the conducted EMI emissions. On the other hand, it allows also the study of the effect that delays between the synchronous commands can have on the EMI spectrum.

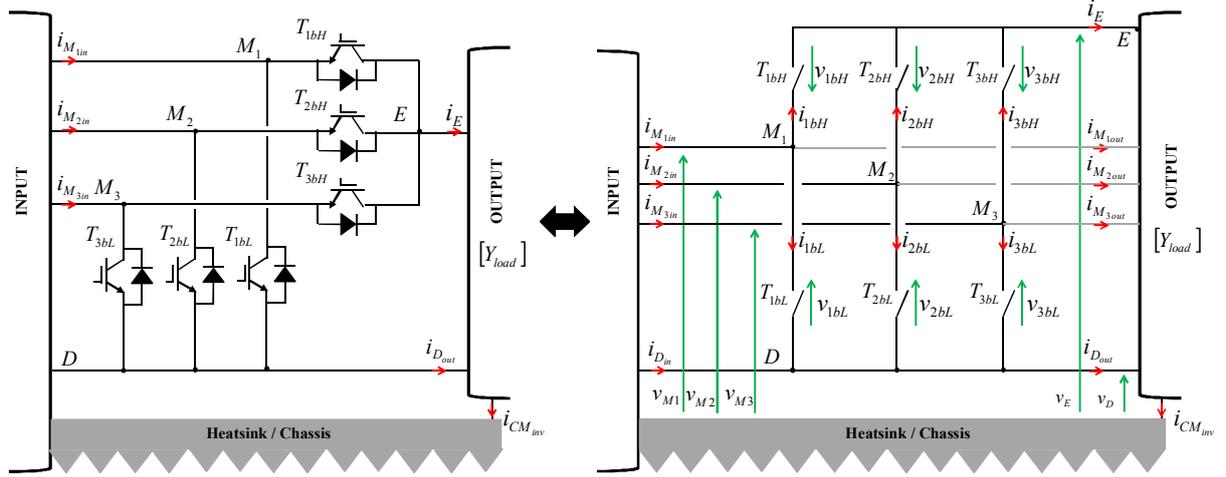


Fig.6. Representation of the traction inverter used during charging.

❖ Common mode behavioral model of the three-legged Boost

The pair of switches belonging to the same bridge leg forms a switching cell. Thus, these switches have complementary switching states. In this section, only the common mode behavior is studied.

$$\begin{bmatrix} I_E \\ I_{M1out} \\ I_{M2out} \\ I_{M3out} \\ I_{Dout} \end{bmatrix} = [Y_{load}] \cdot \begin{bmatrix} V_E \\ V_{M1} \\ V_{M2} \\ V_{M3} \\ V_D \end{bmatrix}; \text{ avec } [Y_{load}] = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} & Y_{15} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} & Y_{25} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} & Y_{35} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} & Y_{45} \\ Y_{51} & Y_{52} & Y_{53} & Y_{54} & Y_{55} \end{bmatrix} \quad \text{eq. (12)}$$

$$I_{CM_{inv}} = \left(I_E + I_{M1out} + I_{M2out} + I_{M3out} + I_{Dout} \right)_{DM=0} \quad \text{eq. (13)}$$

$$I_{CM_{inv}} = Y_E \cdot V_E + Y_{M1} \cdot V_{M1} + Y_{M2} \cdot V_{M2} + Y_{M3} \cdot V_{M3} + Y_D \cdot V_D;$$

where

$$Y_E = \sum_{i=1}^5 Y_{i1}, \quad Y_{M1} = \sum_{i=1}^5 Y_{i2}, \quad Y_{M2} = \sum_{i=1}^5 Y_{i3}, \quad Y_{M3} = \sum_{i=1}^5 Y_{i4}, \quad \text{and} \quad Y_D = \sum_{i=1}^5 Y_{i5} \quad \text{eq. (14)}$$

This expression can be written as a function of V_E and V_D .

$$\begin{cases} V_{M1} = V_D + V_{1bL} \\ V_{M2} = V_D + V_{2bL} \\ V_{M3} = V_D + V_{3bL} \end{cases} \quad \text{eq. (15)}$$

Moreover,

$$\begin{cases} V_{1bL} = (\delta - F_{Tb1}) * (V_E - V_D) \\ V_{2bL} = (\delta - F_{Tb2}) * (V_E - V_D); \text{ with } \begin{cases} f_{Tbi} = 1 \text{ if } T_{ibL} \text{ is ON} \\ f_{Tbi} = 0 \text{ if } T_{ibL} \text{ is OFF} \end{cases} \\ V_{3bL} = (\delta - F_{Tb3}) * (V_E - V_D) \end{cases} \quad \text{eq. (16)}$$

Hence, the common mode current generated by the traction inverter can be written as follows:

$$\begin{aligned} I_{CM_{inv}} = & Y_E \cdot V_E + Y_D \cdot V_D + Y_{M1} \cdot \left[\frac{V_E + V_D}{2} + \frac{(\delta - 2 \cdot F_{Tb1})}{2} * (V_E - V_D) \right] + \dots \\ & + Y_{M2} \cdot \left[\frac{V_E + V_D}{2} + \frac{(\delta - 2 \cdot F_{Tb2})}{2} * (V_E - V_D) \right] + Y_{M3} \cdot \left[\frac{V_E + V_D}{2} + \frac{(\delta - 2 \cdot F_{Tb3})}{2} * (V_E - V_D) \right] \end{aligned} \quad \text{eq. (17)}$$

The common mode model can be deduced and is shown in Fig.7 (a).

❖ Differential mode behavioral model of the three-legged Boost

On the other hand, the differential mode model is deduced by writing the relations between line to line variables.

$$\begin{cases} V_{M1} - V_D = F_{Tb1} * (V_E - V_D) \\ V_{M2} - V_D = F_{Tb2} * (V_E - V_D) \\ V_{M3} - V_D = F_{Tb3} * (V_E - V_D) \end{cases} \quad \text{eq. (18)}$$

$$I_E = \left(F_{Tb1} * I_{M_{1in}} + F_{Tb2} * I_{M_{2in}} + F_{Tb3} * I_{M_{3in}} \right) \Big|_{CM=0} \quad \text{eq. (19)}$$

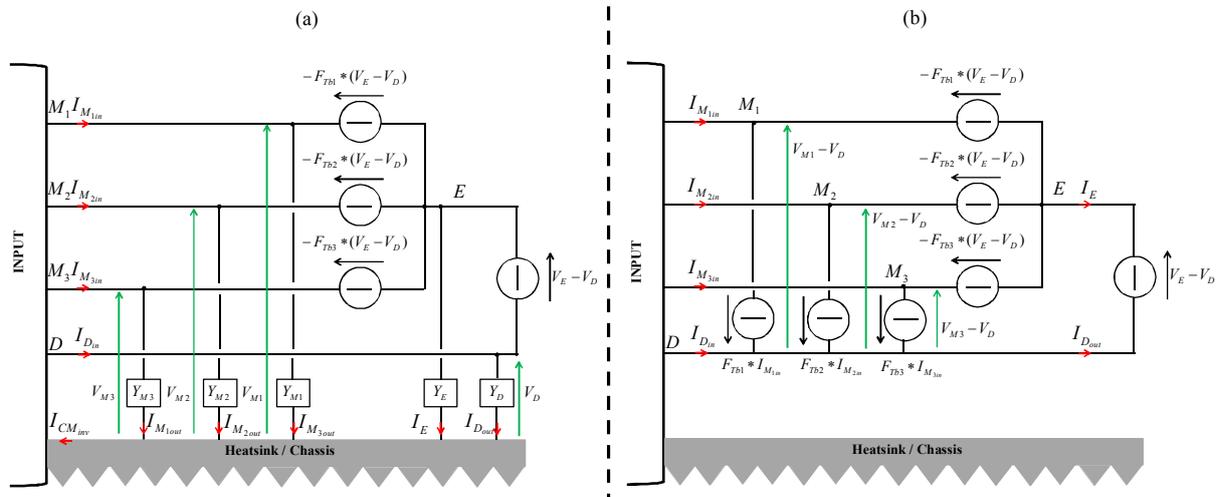


Fig.7. EMI model of the traction inverter used during charging. (a) CM model, (b) DM model.

❖ **Combined EMI model of the three-legged Boost**

The traction inverter's three legs form each a switching cell having M_1 , M_2 and M_3 as midpoint. Therefore, the combined EMI model is based on three controlled voltage sources (for CM behavior) associated to three controlled current sources (for DM behavior).

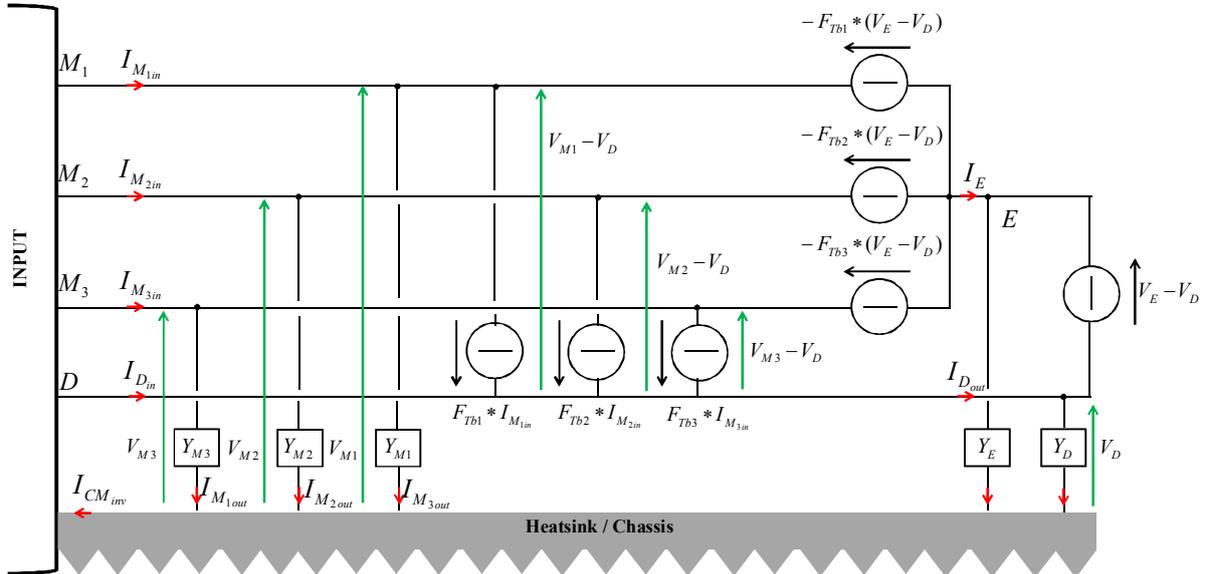


Fig.8. Combined CM/DM EMI model of the traction inverter used during charging.

Appendix E: Measured leakage impedance of the autotransformer

The total leakage impedance of the autotransformer presenting a 10% transform rate is measured at its secondary side while short-circuiting the primary side. The measurements given in Fig.9 are done using an impedance analyzer of type Agilent Technologies E5061B.

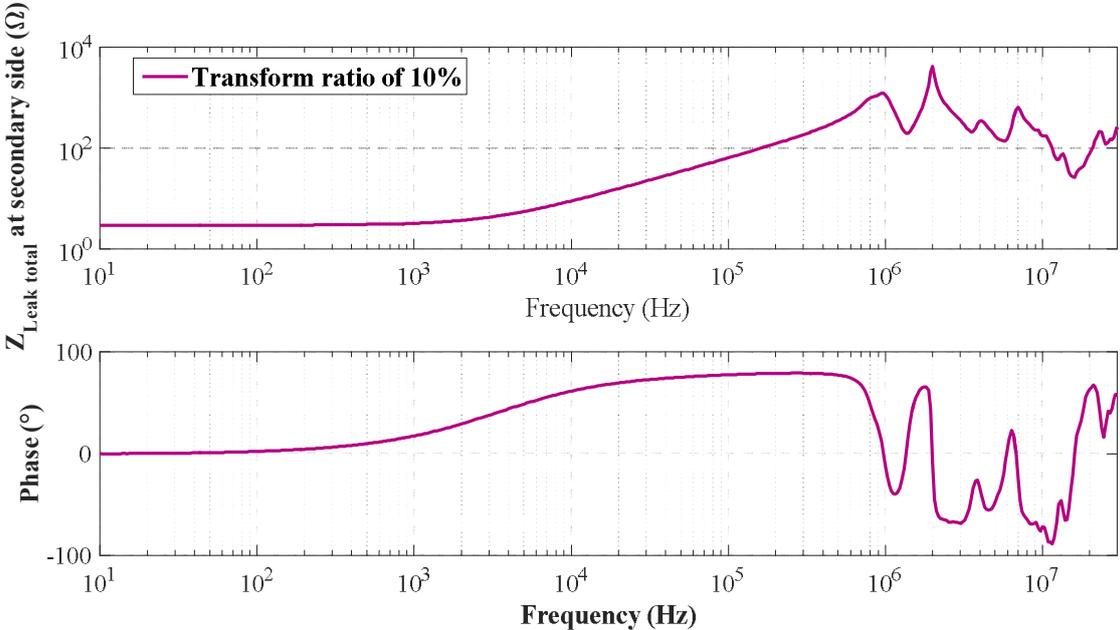


Fig.9. Measurement of the total leakage impedance of the autotransformer at its secondary side with the primary side short-circuited and a transform ratio of 10%.

Appendix F: Combined CM & DM EMI model of the modified single-phase charger

❖ Modeling of the modified Boost

The Boost is modified in order to ensure reduced common mode current generation (Fig.10). The idea is to achieve symmetrical behavior on both DC buses. Therefore, the original switching cell defined by $\{T_{bH}, T_{bL}\}$ and having the node M as midpoint, is going to be mirrored on the other bus by adding a new diode D_{new} . The added diode takes part of a new switching cell defined by $\{T_{bL}, D_{new}\}$ and having the node D as midpoint. The high-side switch is always kept turned off. Therefore, the proposed Boost is characterized by two switching cells and by the creation of a new midpoint (node D) presenting fluctuating states depending on the pulse width modulation strategy.

Furthermore, in the case of integrated chargers, the Boost described in this section can be replaced by the bidirectional traction inverter. Since the added diode removes the current bidirectional property of the inverter, an additional switch is placed in parallel with D_{new} in order to short circuit this diode during traction operation. The switch is turned off during the charging operation.

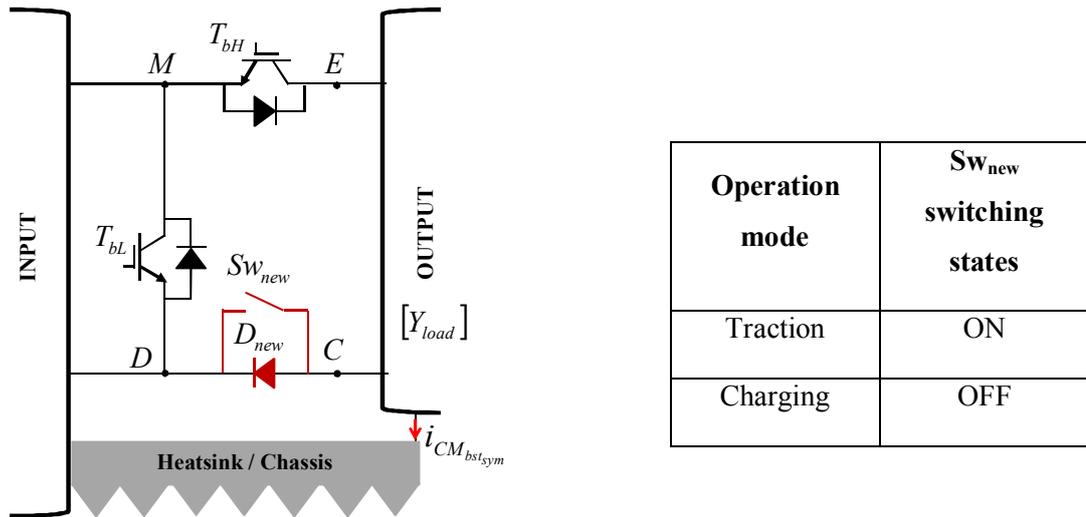


Fig.10. Structure of the proposed modified Boost with two switching cells.

This work analyses the charger, hence, the switch Sw_{new} will no longer be represented and the effects of its parasitic elements on the common mode current generation will be neglected. The electrical representation of the modified Boost's switching cells is given in Fig.11.

a. CM behavioral model

In this sub-section, only the CM emissions are analyzed. The expression of the CM current generated by the modified dc-dc converter is deduced in eq. (22).

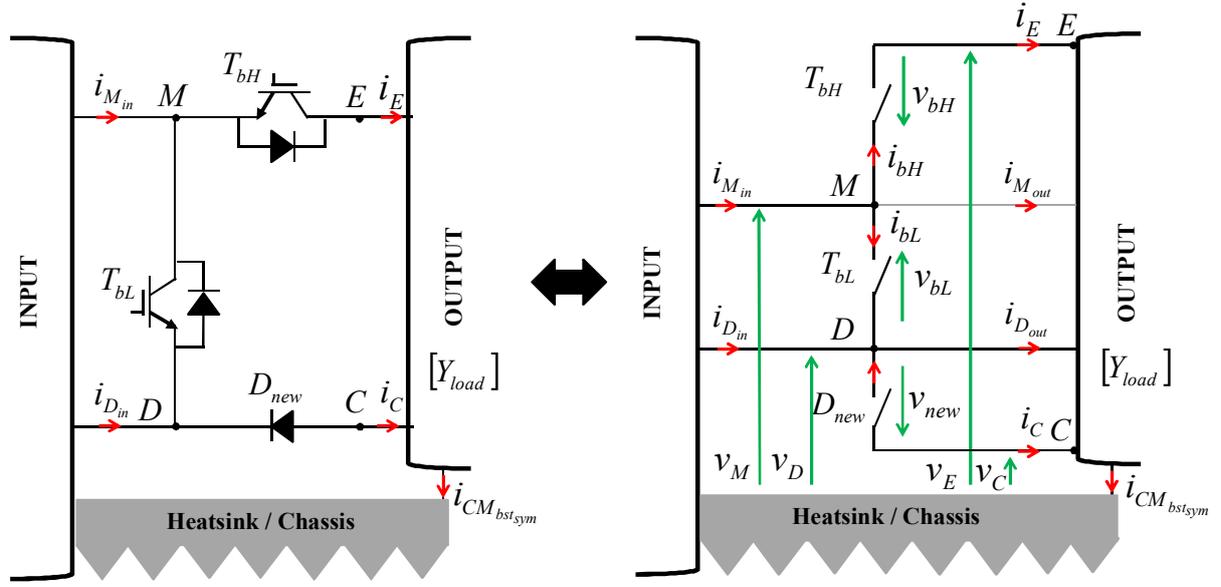


Fig.11. Representation of the modified Boost's switching cells.

$$\begin{bmatrix} I_E \\ I_{M_{out}} \\ I_{D_{out}} \\ I_C \end{bmatrix} = [Y_{load}] \cdot \begin{bmatrix} V_E \\ V_M \\ V_D \\ V_C \end{bmatrix}; \text{ avec } [Y_{load}] = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \quad \text{eq. (20)}$$

$$I_{CM_{bst_{syst}}} = (I_E + I_{M_{out}} + I_{D_{out}} + I_C)_{DM=0} \quad \text{eq. (21)}$$

$$I_{CM_{bst_{syst}}} = Y_E \cdot V_E + Y_M \cdot V_M + Y_D \cdot V_D + Y_C \cdot V_C \quad ; \text{ where}$$

$$Y_E = \sum_{i=1}^4 Y_{i1}, \quad Y_M = \sum_{i=1}^4 Y_{i2}, \quad Y_D = \sum_{i=1}^4 Y_{i3}, \quad \text{and} \quad Y_C = \sum_{i=1}^4 Y_{i4} \quad \text{eq. (22)}$$

This expression can be written as a function of the output DC bus voltages V_E and V_C , as follows:

$$\begin{cases} V_M = V_E + V_{bH} \\ V_D = V_C - V_{new} \end{cases} \quad \text{eq. (23)}$$

Moreover, by using the same definition of the switching function as for the conventional Boost eq. (24); the voltage across the anti-parallel diode of T_{bH} can be deduced in eq. (25). We assume the equal distribution of the output voltage between the diodes (D_{new} , D_{TbH}) when T_{bH} is turned ON.

$$\begin{cases} f_{Tb} = 1, & T_{bL} \text{ is ON} \\ f_{Tb} = 0, & T_{bL} \text{ is OFF} \end{cases} \quad \text{eq. (24)}$$

$$V_{bH} = V_{new} = -F_{Tb} * \left(\frac{V_E - V_C}{2} \right) \quad \text{eq. (25)}$$

This leads to:

$$\begin{cases} V_M = \frac{V_E + V_C}{2} + \frac{(\delta - F_{Tb})}{2} * (V_E - V_C) \\ V_D = \frac{V_E + V_C}{2} - \frac{(\delta - F_{Tb})}{2} * (V_E - V_C) \end{cases} \quad \text{eq. (26)}$$

Hence, the common mode current generated by the proposed modified Boost structure can be written as follows:

$$I_{CM_{bstsym}} = Y_E \cdot V_E + Y_C \cdot V_C + Y_M \cdot \left[\frac{V_E + V_C}{2} + \frac{(\delta - F_{Tb})}{2} * (V_E - V_C) \right] + Y_D \cdot \left[\frac{V_E + V_C}{2} - \frac{(\delta - F_{Tb})}{2} * (V_E - V_C) \right] \quad \text{eq. (27)}$$

Based on this equation, we propose the common mode model that is shown in Fig.12 (a).

It can already be seen from eq. (27) and from Fig.12 (a) that the voltages between nodes M / D and the frame ground vary in opposition across the parasitic admittances Y_M and Y_D respectively.

b. DM behavioral model

On the other hand, the relations between line to line variables are computed in order to be able to propose a corresponding DM model:

$$V_M - V_D = (\delta - F_{Tb}) * (V_E - V_C) \quad \text{eq. (28)}$$

$$I_E = (\delta - F_{Tb}) * I_{M_{in}} \Big|_{CM=0} \quad \text{eq. (29)}$$

Based on these equations, we propose the DM EMI model of the modified Boost illustrated in Fig.12 (b).

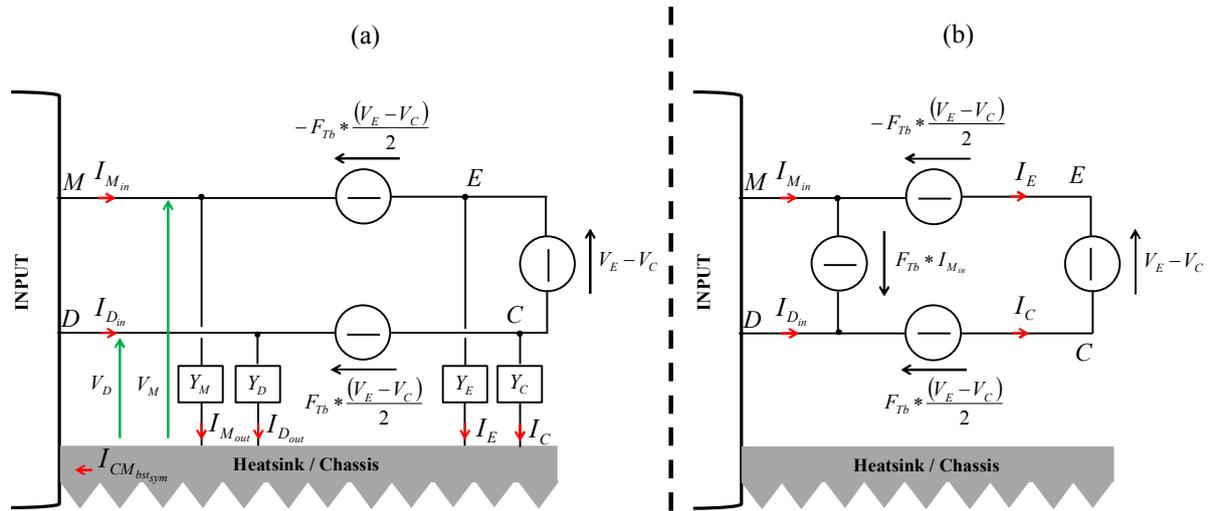


Fig.12. Proposed CM/DM models of the modified Boost's switching cells. (a) CM, (b) DM.

c. Combined CM & DM model of the modified Boost

The combined CM/ DM model of the proposed Boost is given in Fig.13.

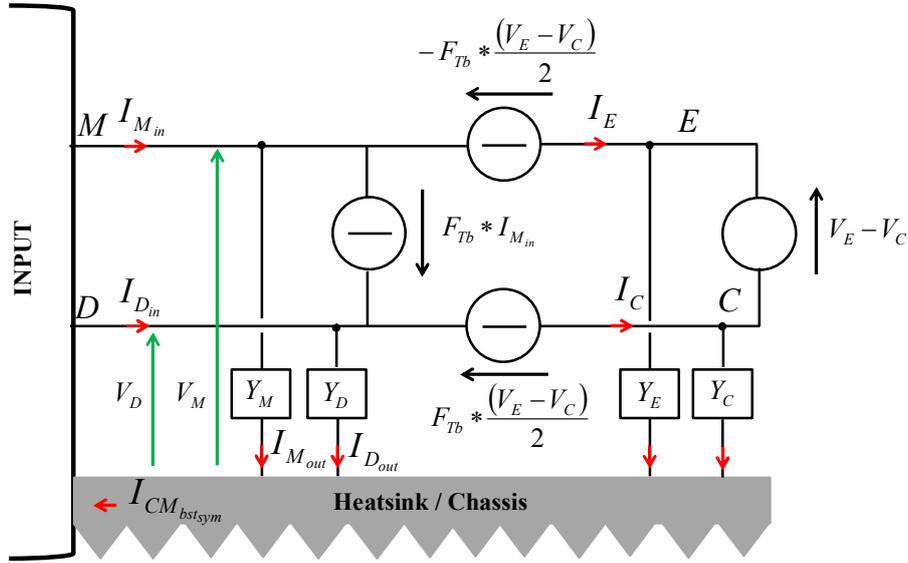


Fig.13. Combined CM/DM model of the modified balanced Boost converter.

❖ Modeling of the modified single-phase CSAR

In order to reduce the emission levels of the CM current generated by the CSAR, a modified structure is proposed along with a specific switch control law. In fact, a freewheeling diode is added at the output of the rectifier and the CSAR's switches, including the low side switches, are all controlled via pulse width modulation. During the freewheeling state all the switches are turned off simultaneously. The switching functions are defined in eq. (30) - eq. (31) and the switching states of the modified rectifier are given in Table.2.

Table.2. SWITCHING STATES OF THE MODIFIED SINGLE-PHASE CSAR WITH A FREEWHEELING DIODE

Grid side input voltage v_{AB}	Switch				
	T_{1H}	T_{2H}	T_{1L}	T_{2L}	D_{fw}
Positive half cycle $f_D = 1$	f_{T1H}	OFF	OFF	f_{T1H}	$1 - f_{T1H}$
Negative half cycle $f_D = 0$	OFF	f_{T2H}	f_{T2H}	OFF	$1 - f_{T2H}$

$$\begin{cases} f_{TiH} = 1, & T_{iH} \text{ is ON} \\ f_{TiH} = 0, & T_{iH} \text{ is OFF} \end{cases}, \text{ with } i = 1, 2 \quad \text{eq. (30)}$$

$$\begin{cases} f_D = 1, & v_{AB} \geq 0 \\ f_D = 0, & v_{AB} < 0 \end{cases} \quad \text{eq. (31)}$$

a. CM behavioral model of the modified single-phase CSAR

The power circuit of the modified balanced single-phase CSAR is given in Fig.14. From this representation, the CM current generated by the converter is computed in eq. (34).

$$\begin{bmatrix} I_{A_{out}} \\ I_P \\ I_N \\ I_{B_{out}} \end{bmatrix} = [Y_{load}] \cdot \begin{bmatrix} V_A \\ V_P \\ V_N \\ V_B \end{bmatrix}; \text{ avec } [Y_{load}] = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \quad \text{eq. (32)}$$

$$I_{CM_{bck_{sym}}} = (I_{A_{out}} + I_P + I_N + I_{B_{out}})_{DM=0} \quad \text{eq. (33)}$$

$$I_{CM_{bck_{sym}}} = Y_A \cdot V_A + Y_P \cdot V_P + Y_N \cdot V_N + Y_B \cdot V_B; \text{ where}$$

$$Y_A = \sum_{i=1}^4 Y_{i1}, \quad Y_P = \sum_{i=1}^4 Y_{i2}, \quad Y_N = \sum_{i=1}^4 Y_{i3}, \quad \text{and } Y_B = \sum_{i=1}^4 Y_{i4} \quad \text{eq. (34)}$$

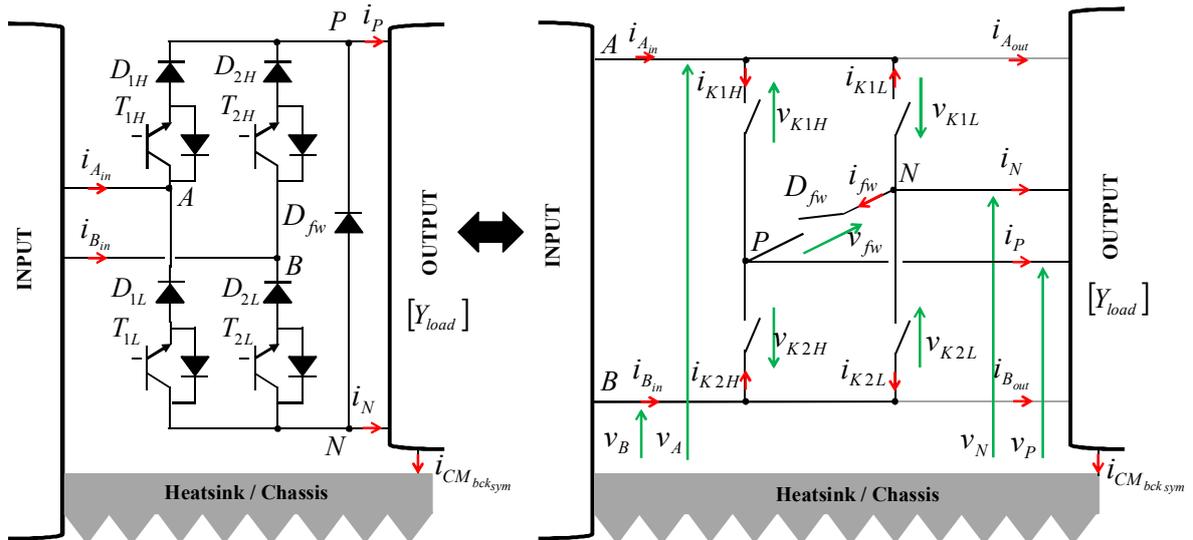


Fig.14. Representation of the modified single-phase CSAR's switching cells.

This expression can be written as a function of the input line to ground voltages V_A and V_B , as follows:

$$\begin{cases} V_P = V_A - V_{K1H} \\ V_N = V_A + V_{K1L} \end{cases} \quad \text{eq. (35)}$$

Depending on the switch control law adopted for the modified CSAR's IGBTs (T_{1H} , T_{2H} , T_{1L} , T_{2L}), the voltages across the switches (K_{1H} , K_{2H} , K_{1L} , K_{2L}) and D_{fw} can be deduced in Table.3. It should be noted that the CSAR's diodes share the same states as their series IGBTs. The binary numbers are an indication of the state of the IGBT or diode ('0' for OFF and '1' for ON). Moreover, an equal distribution of the voltages across two turned-off switches is assumed.

Table.3. VOLTAGES ACROSS THE MODIFIED CSAR'S SWITCHES

Input voltage v_{AB}	State of IGBT/Diode									Voltages across the switches				Output voltage
	T_{1H}	T_{2H}	T_{1L}	T_{2L}	D_{1H}	D_{2H}	D_{1L}	D_{2L}	D_{fw}	v_{K1H}	v_{K2H}	v_{K1L}	v_{K2L}	$v_{PN} = -v_{fw}$
Positive half cycle $f_D = 1$	0	0	0	0	0	0	0	0	1	$\frac{v_{AB}}{2}$	$-\frac{v_{AB}}{2}$	$-\frac{v_{AB}}{2}$	$\frac{v_{AB}}{2}$	0 <i>Freewheel</i>
	1	0	0	1	1	0	0	1	0	0	$-v_{AB}$	$-v_{AB}$	0	v_{AB} <i>Active State</i>
Negative half cycle $f_D = 0$	0	1	1	0	0	1	1	0	0	v_{AB}	0	0	v_{AB}	$-v_{AB}$ <i>Active State</i>
	0	0	0	0	0	0	0	0	1	$\frac{v_{AB}}{2}$	$-\frac{v_{AB}}{2}$	$-\frac{v_{AB}}{2}$	$\frac{v_{AB}}{2}$	0 <i>Freewheel</i>

It can be deduced that the voltages across the switches K_{1H} and K_{1L} depend on the input differential voltage V_{AB} and the switching functions defined earlier, as such:

$$\begin{cases} V_{K1H} = (\delta - F_D * F_{T1H} + F_{T2H}) * \left(\frac{V_A - V_B}{2} \right) \\ V_{K1L} = -[\delta - (\delta - F_D) * F_{T2H} + F_{T1H}] * \left(\frac{V_A - V_B}{2} \right) \end{cases} \quad \text{eq. (36)}$$

This leads to:

$$\begin{cases} V_P = \frac{V_A + V_B}{2} + \frac{(F_D * F_{T1H} - F_{T2H}) * (V_A - V_B)}{2} \\ V_N = \frac{V_A + V_B}{2} + \frac{(\delta - F_D) * F_{T2H} - F_{T1H} * (V_A - V_B)}{2} \end{cases} \quad \text{eq. (37)}$$

Hence, the CM current generated by the proposed CSAR structure can be written as follows:

$$I_{CM_{\text{backsym}}} = Y_A \cdot V_A + Y_B \cdot V_B + Y_N \cdot \left[\frac{V_A + V_B}{2} + \frac{(\delta - F_D) * F_{T2H} - F_{T1H}}{2} * (V_A - V_B) \right] + \dots$$

$$Y_P \cdot \left[\frac{V_A + V_B}{2} + \frac{(F_D * F_{T1H} - F_{T2H})}{2} * (V_A - V_B) \right]$$
eq. (38)

Based on this expression, we propose to model the modified single-phase CSAR with the circuit model of Fig.15 (a).

b. DM behavioral model of the modified single-phase CSAR

On the other hand, the differential mode model is deduced from Fig.14 by writing the relations between line to line variables.

$$V_P - V_N = (F_D * F_{T1H} - F_{T2H}) * (V_A - V_B)$$
eq. (39)

$$I_{A_m} = [F_D * F_{T1H} - (\delta - F_D) * F_{T2H}] * I_P \Big|_{CM=0}$$
eq. (40)

Based on this development, we propose to model the DM emissions of the modified single-phase CSAR by the circuit representation of Fig.15 (b).

c. Combined CM & DM conducted EMI model of the modified single-phase CSAR

The circuit representation of the modified CSAR that allows modeling the CM and the DM emissions is obtained by combining the circuit representations shown in Fig.16.

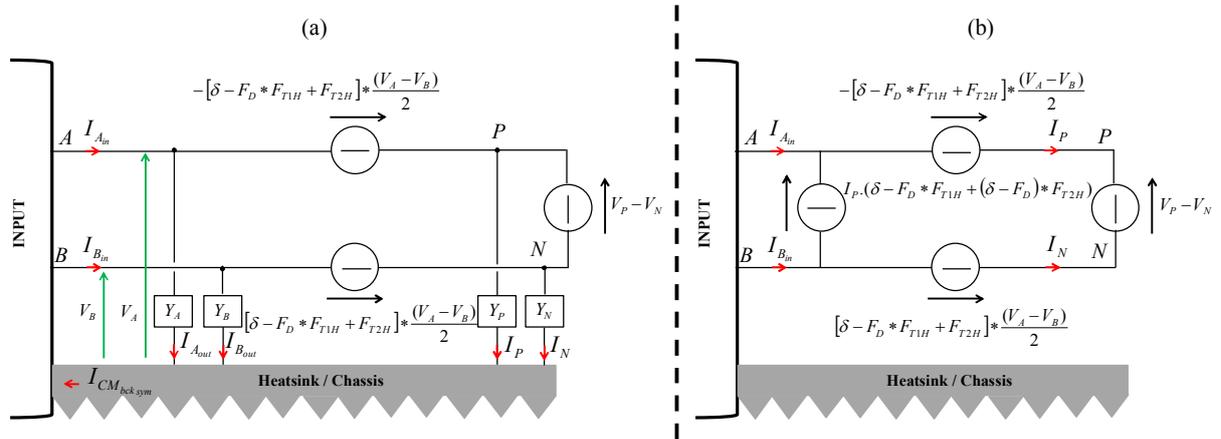


Fig.15. Proposed CM/DM models of the modified single-phase CSAR. (a) CM, (b) DM.

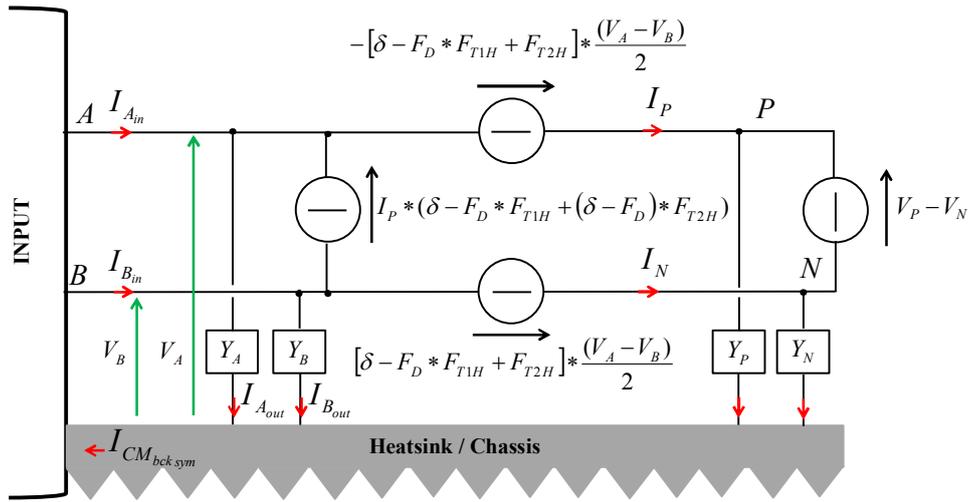


Fig.16. Combined CM/DM model of the modified balanced single-phase CSAR.

Appendix G: Computation of the impedance leading to the mixed-mode noise emissions

By neglecting the line to line impedances, we will expose the general principle leading to the computation of the expression of the CM current generated by a network of impedances. An example of the network of impedances along the path of the CM current is illustrated in Fig.17.

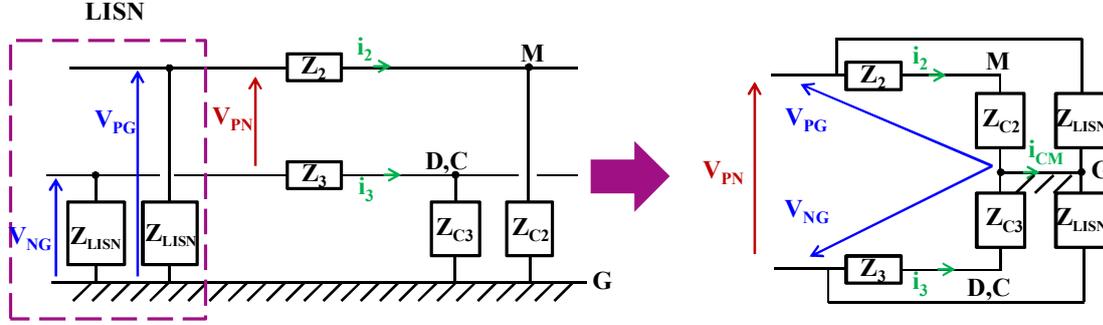


Fig.17. Network of impedances along the propagation path of the CM current (by neglecting the stray capacitances at the output of the CSAR).

The expressions of the line to ground voltages are given by:

$$\begin{cases} V_{PG} = V_{PN} \cdot \frac{Z_{eq1}}{Z_{eq1} + Z_{eq2}} \\ V_{NG} = -V_{PN} \cdot \frac{Z_{eq2}}{Z_{eq1} + Z_{eq2}} \end{cases}; \quad \text{with} \quad \begin{cases} Z_{eq1} = \frac{Z_{LISN} \cdot (Z_{C2} + Z_2)}{Z_{LISN} + Z_{C2} + Z_2} \\ Z_{eq2} = \frac{Z_{LISN} \cdot (Z_{C3} + Z_3)}{Z_{LISN} + Z_{C3} + Z_3} \end{cases} \quad \text{eq. (41)}$$

The equivalent representation of the network of impedances is shown in Fig.18.

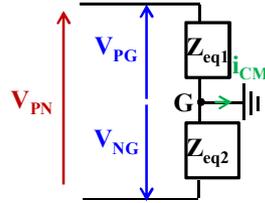


Fig.18. Equivalent representation of the network of impedances.

Hence, the expression of the CM current generated by this network of line impedances, stray capacitances and LISN impedances can be computed along with the CM admittance:

$$\begin{aligned} i_{CM} = i_2 + i_3 &= \frac{V_{PG}}{Z_2 + Z_{C2}} + \frac{V_{NG}}{Z_3 + Z_{C3}} = \frac{V_{PN} \cdot Z_{LISN}}{Z_{eq1} + Z_{eq2}} \cdot \left[\frac{1}{Z_{LISN} + Z_2 + Z_{C2}} - \frac{1}{Z_{LISN} + Z_3 + Z_{C3}} \right] \\ &= V_{PN} \cdot Y_{CM} \end{aligned} \quad \text{eq. (42)}$$

Titre: Optimisation de la CEM conduite d'un chargeur de batteries embarqué dans un véhicule électrique

Mots clés: chargeur monophasé, chargeur triphasé, contrôle commande, correction du facteur de puissance, électronique de puissance, émissions conduites de mode commun, modélisation CEM.

Résumé : La charge d'un véhicule électrique constitue un enjeu stratégique pour les constructeurs automobile et forme un réel défi à relever avant de pouvoir comparer ces véhicules à la simplicité d'usage du véhicule thermique. En effet, l'autonomie limitée, la durée de recharge de la batterie, le coût du déploiement d'une infrastructure de charge rapide, l'impact significatif sur les réseaux électriques et le coût élevé de la batterie sont à l'origine de plusieurs projets de recherche axés sur l'optimisation de la chaîne de recharge du véhicule électrique. Afin d'améliorer l'autonomie d'un véhicule électrique, une solution contraignante mais stratégique consiste à embarquer le chargeur dans le véhicule afin d'assurer la conversion ac-de de l'énergie à partir des prises de courant. Cette solution permet d'augmenter la disponibilité de la charge pour les utilisateurs. En outre, le chargeur embarqué peut réutiliser tout, ou une partie des éléments déjà existants et nécessaires à la propulsion du véhicule. L'idée étant de pouvoir employer certains éléments de la chaîne de traction électrique, déjà embarqués dans le VE (moteur électrique et onduleur de tension), et d'ajouter un filtre d'entrée et un redresseur afin de concevoir le chargeur. Cette solution permet de réduire le coût du chargeur, sa taille ainsi que le volume nécessaire à l'intégration de ses constituants électriques, on parle alors de chargeur intégré à la chaîne de traction. Cependant, la réutilisation de l'électronique de puissance embarquée engendre des problèmes de compatibilité électromagnétique avec d'autres équipements connectés sur le réseau électrique et aussi avec les dispositifs de protection domestique.

Le problème majeur à lever est donc, la limitation des émissions conduites et plus particulièrement des courants de mode commun dans une gamme de fréquence importante. Ce projet de thèse a donc, pour objectif, l'amélioration de la disponibilité de la charge actuelle tout en réduisant le volume du filtre CEM passif. Nous cherchons, à travers ces travaux, à identifier des domaines d'améliorations possibles, à proposer des solutions à bas coûts et à intégrer des modifications au niveau de la commande et de la topologie afin d'optimiser le comportement CEM, tant en basses fréquences (0 - 2 kHz) qu'en hautes fréquences (150 Hz- 30 MHz), de ce chargeur embarqué intégré sans isolation galvanique. Les propositions doivent répondre simultanément aux besoins de recharge domestique en monophasé (à 3.7 kW et à 7.4 kW) et rapide en triphasé (à 22 kW et à 43 kW) sans pour autant augmenter le volume ni les coûts engendrés.

Ainsi, cinq axes de travail sont étudiés: l'optimisation du comportement CEM (0-2 kHz) du chargeur en monophasé ; l'optimisation du comportement CEM (0-2 kHz) du chargeur en triphasé ; le développement, la mise en œuvre et l'instrumentation de deux bancs expérimentaux exploités pour l'obtention de résultats; la proposition d'une approche de modélisation CEM de la structure qui tient compte du mode commun et du mode différentiel ; et la proposition de solutions pour la réduction des émissions conduites (150 kHz – 30 MHz).

Title: Optimization of the conducted emissions of an on-board charger for electric vehicles

Keywords: conducted common mode emissions, control strategies, EMI model, power electronics, power factor correction, single-phase charger, three-phase charger.

Abstract: Battery chargers for electric vehicles are classified as on-board or off-board chargers. Off-board chargers are not constrained by size or weight but introduce additional cost to the infrastructure through the deployment of a high number of charging stations. In order to meet the needs of electric vehicle users in terms of charging availability, on-board chargers that achieve ac/dc conversion are retained. Furthermore, on-board chargers are classified as standalone or integrated systems. By reusing parts of the traction power train for charging, the latter reduces the cost of the charger. Disadvantages of integrated systems include electromagnetic compatibility issues and complex control schemes.

This work presents the power quality performance analysis and control optimization of an on-board non-galvanically isolated electric vehicle charger integrated to the traction's power train. In order to be able to evaluate the high frequency conducted common mode emissions (150 kHz - 30MHz) of a power conversion structure, one needs to develop a good current control scheme that establishes a high-quality low frequency behavior (0 - 2 kHz).

Therefore, different aspects related to the power factor correction of the single-phase as well as the three-phase charging configurations are studied: the control scheme for the regulation of the charging power, the displacement power factor correction, the suppression of the grid current harmonics and the active damping of the input filter's resonance. Two experimental test benches are developed using two different technologies (Silicon IGBTs vs. Silicon Carbide Mosfets). Experimental results are provided.

This work also presents a comprehensive approach to modeling the CM and the DM EMI behavior of a power electronics structure. This method is applied to the charger in its single-phase and three-phase configurations. The models allow to evaluate the fluctuating internal nodes and to study the effect of various proposed mitigation solutions on the CM emissions. The models are also developed in the intent of being injected into optimization algorithms for the future design of an optimal EMI filter.