Fatigue mechanisms in Al-based metallizations in power MOSFETs

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Modes de fatigue des métallisations à base d'aluminium dans les composants MOSFET de puissance

Fatigue mechanisms in Al-based metallizations in power MOSFETs

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ABSTRACT

This thesis, a collaboration between CEMES-CNRS, Satie laboratory (ENS Cachan) and NXP Semiconductors is motivated by the comprehension of the failure mechanisms of low voltage power MOSFET devices produced for applications in the automotive industry.
A limiting factor for the long-term reliability of power modules is the electro-thermal and/or thermo-mechanical aging of the metallic parts of the source: Al metallization and bonding wires. At the temperature reached during the on-off operating cycles (few hundred degrees), the difference in the coefficient of thermal expansion between the metallization and the oxide and semiconductor parts induces an inevitable plastic deformation in the metal, which is the softest material in the complex MOSFET architecture.
We have characterized the metal microstructure before and after accelerated electro-thermal aging tests, by using specific techniques from the field of the physical metallurgy: electron and ion microscopy, grain orientation and chemical composition mapping. For the first time the source metallization has been characterized both away and under the bonding connections, which are one hundred times thicker than the metallization layer. The latter is a critical location for the reliability assessment because the ultrasonic bonding process may weaken the initial metallization microstructure by adding an important plastic deformation prior to aging. This is, however, poorly stated in the literature because of the difficulty to access the metallization under the wires without damaging their bonding, which is known to be particularly weak in case of aged modules.
In order to investigate the wire-metallization interface, we have set up original sample preparations, based on ion polishing, that allowed us to disclose the metallization under the bonding wires without introducing preparation artifacts in the microstructure. The bonding process induces a severe and non-uniform plastic deformation in the metallization under the wires without re-creating a good electrical contact: small cavities and native oxide residues, have been systematically observed at the Al/Al interface, in all the analyzed modules, before and after aging.
The main mechanism behind the device failure is the generation and propagation of fatigue cracks in the aluminum metallization, associated to a local Al oxidation that prevents these crack from closing. Away and under the wire bonds, they run perpendicularly from the surface down to the silicon substrate following the grain boundaries, due to an enhanced intergranular diffusion of

aluminum atoms. In the bonding area, the phenomenon of parallel cracking is favored by the initial imperfections in the wire-metallization bonding. Ion tomography experiments have shown that these cracks are confined to the wire-metal interface and do not propagate in the wire despite its lower strength (pure Al, larger grain structure). Crack propagation along the Al/Al interface can cause a contact reduction between the wire and the source metallization and eventually its failure. Such discontinuities in the metal can explain the local increase in the device resistance and temperature that accelerates the aging process until failure.

This study settled new, dedicated techniques and quantification methods to assess the aging of the metal parts of MOSFET devices. The full characterization of the intrinsically defective interface generated by the bonding process and the metallization degradation during electro-thermal aging indicated paths to possible improvements of current technologies and potential developments of new processes.

RESUMÉ

Cette thèse, effectuée en collaboration entre le CEMES-CNRS, le laboratoire Satie (ENS Cachan) et NXP Semiconductors est motivée par la compréhension des mécanismes de défaillance des dispositifs MOSFET pour les applications dans l'industrie automobile.
Un facteur limitant de la fiabilité à long terme des modules de puissance basse tension est le vieillissement électrothermique et/ou thermo-mécanique des parties métalliques de la source: métallisation en aluminium (ou alliage) et fils de connexion. A cause de la différence de coefficient de dilatation thermique entre la métallisation les oxydes et le substrat semi-conducteur, la température atteinte pendant les cycles de fonctionnement (quelques centaines de degrés), induit une déformation plastique inévitable dans le métal, qui est le matériau le plus mou dans l'architecture complexe du MOSFET.
Nous avons caractérisé la microstructure métallique avant et après les tests de vieillissement électrothermique accélérés, en utilisant des techniques spécifiques du domaine de la métallurgie physique: microscopie électronique et ionique, cartographie d'orientation de grains et de la composition chimique. Pour la première fois, la métallisation de la source a été caractérisée sous les fils de connexion, qui sont cent fois plus épais que la métallisation. Cet emplacement est critique pour la fiabilité du composant, car le processus de soudure par ultrasons induit une déformation plastique importante qui peut affaiblir la métallisation initiale avant le vieillissement. Ceci est peu étudié dans la littérature en raison de la difficulté à accéder à la métallisation sous les fils sans altérer leur interface, souvent endommagée et fragilisée dans les modules vieillis.
Nous avons mis en place des méthodes de préparation d'échantillon, basées sur le polissage ionique, pour étudier cette interface, sans introduire d'artefacts de préparation. Le processus de soudure à froid induit une déformation plastique sévère et non uniforme dans la métallisation sous les fils sans parvenir à recréer un bon contact électrique: de petites cavités et des résidus d'oxyde natif, ont été systématiquement observés à l'interface Al / Al, dans tous les modules analysés, avant et après vieillissement.
Le mécanisme principal de défaillance des modules est la génération et la propagation de fissures de fatigue dans l'aluminium, associée à une oxydation locale qui empêche la fermeture de ces fissures. Sous et en dehors des fils de connexion, ces fissures traversent la métallisation perpendiculairement à la surface jusqu'au substrat en silicium en suivant les joints de grains. Cette fissur-

ation est due à la diffusion intergranulaire accélérée des atomes d'aluminium. Dans la zone de soudure, le phénomène de fissuration parallèle à l'interface est favorisé par les imperfections initiales (cavités, oxyde). Les expériences de tomographie ionique ont montré que ces fissures sont confinées à l'interface fil-métal et ne se propagent pas dans le fil malgré sa plus faible résistance mécanique (Al pur, structure à grains plus grands). La propagation de la fissure le long de l'interface Al/Al peut provoquer une diminution du contact entre le fil et la métallisation de la source et éventuellement son décollement. Les fissures dans le métal source peuvent expliquer l'augmentation locale de la résistance et de la température du module qui accélère le processus de vieillissement jusqu'à l'échec.
Cette étude a établi de nouvelles techniques dédiées et des méthodes de quantification pour évaluer le vieillissement des parties métalliques des modules MOSFET. La caractérisation complète de l'interface soudée, intrinsèquement défectueuse et la dégradation de la métallisation pendant le vieillissement électrothermique ouvrent la voie à l'amélioration possible les technologies actuelles et au développement potentiel de nouveaux procédés.

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KEYWORDS

- Low voltage power MOSFETs
- Failure analysis
- Accelerated electro-thermal aging test
- Plastic deformation
- Fatigue mechanisms
- Wire-metallization interface
- Metallization microstructure aging
- Electron microscopy
- Ion microscopy
- Grain structure mapping

1 INTRODUCTION

Over the last few decades, the automotive industry has started to progressively replace electro-mechanical components by purely electronic devices or miniaturized electro-mechanical systems based on Si-technologies. This paradigm shift has initially involved support electronic systems (e.g. ABS, power-assisted steering, speed limiter, air conditioning, etc.). However, the constant technology evolution and miniaturization have rapidly broadened the field of application of electronics in automotive, involving the main vehicle functions (e.g. propulsion, lighting, brakes, engine, fan control, battery management etc.) and increasingly replacing the conventional mechanical and hydraulic loads.

Nowadays, the power electronic sector is the strongest growth market in automotive. Semiconductor-based power switches are rapidly replacing conventional electromechanical relays in most of the main vehicles functions as well as in comfort, safety and communication applications. An additional growing segment is represented by the market for alternative propulsion technologies, in line with the new regulations for road transport aimed at the reduction of greenhouse gas emission level (30% lower by 2030 in the EU). This trend is seen nowadays with more and more focus on electric vehicle concepts, pure (EV) and hybrid (i.e. micro-, mild-, full-, plug-in-hybrid), until the most recent projects of autonomous cars.

The rise in electronic technology in automotive inevitably creates new demands in terms of low costs, operation under extreme environmental conditions (temperature, humidity, vibration, etc.), greater system power density, increasing miniaturization, etc. Moreover, high levels of reliability are of course required to guarantee the safety of products and people over extended periods of time. This requires an in-depth knowledge of the possible evolutions of the electronic components as a function of operating time and failure mechanisms. Failure analysis and reliability studies are, then, key steps in the manufacture industry, in order to develop devices that are 100% reliable during their life-time. This life-time is one of the parameters required by car manufactures, among others, defined by the Automotive Electronic Council (Qualifications documents, e.g. AEC-Q100, AEC-Q200, etc...).

This work is motivated by the comprehension of the failure mechanisms occurring in power electronic switches produced by NXP Semiconductors company for the automotive industry. During their normal life, these components undergo high power levels over a long time, leading to gradual reduction of

their performance. Here, we present a method to assess the device electro-thermal aging, focusing on a specific study case: power switches, based on the MOSFET (Metal Oxide Semiconductor) technology, used for the automobile lightning system. This application is particularly aggressive for MOSFET components because it involves repetitive on/off cycles associated with high electrical pulses and large temperature excursions, leading to a progressive alteration of the device's initial performances. In particular, its initial resistance in the "ON" state increases over time, which in turn, increases its operating temperature. Our objective is to investigate the phenomena behind the degradation of the microstructure of the critical parts of these devices that have been identified as the metallic ones, probably because of their susceptibility to plastic deformation. This would allow us to determine physical models that can explain the main failure mechanisms to be correlated with the progressive worsening of the whole device electrical performances. To do this, we have settled new dedicated techniques and quantification methods to assess the aging of the metal parts of MOSFET devices.

In the first chapter, we present the state of the art of power electronics technologies. Then, we focus on low-voltage MOSFET power devices used in car applications and we present the LFET1T components, the e-switches from NXP Semiconductors under investigation. We also go through the main reliability issues associated to this kind of devices. They are related to the complex structure of the power component, which integrates different materials at different scale. We explain why, the source metallization and bonding wires are the parts of the LFET1T technology where failure is the most prone to happen in the most recent technologies. Finally we present the electro-thermal aging tests that we have used to accelerate the device degradation and failure.

The second chapter details the specific physical metallurgy techniques that we set up in order to characterize the microstructure of the source metallization during aging at two main locations: away and under the bonding connections. These techniques consist essentially in electron and ion microscopy, and grain structure mapping. Because of the complexity and fragility of the device structure, dedicated sample preparations are also needed and described. We try to point out the choices that have motivated the established experimental protocol and the contribution of each technique to the comprehension of the degradation mechanisms.

In the third chapter we introduce the results of the microstructural characterization of the metallic parts of LFET1Ts for 12V and 24V battery applications. We compare the metal microstructure away and under the bonding wires, and we follow its evolution during aging. The contacted metallization is a critical location because the bonding process induces plastic deformation prior to ag-

ing. We show that the main mechanism behind the metallization degradation is the generation and propagation of intergranular fatigue cracks in both locations. Then, we describe and use original quantification methods that allow us, for the first time, to assess the initial plastic deformation induced by the bonding process and the crack propagation during aging.

These results are discussed in detail in chapter 4. We try to highlight the universal degradation mechanisms behind the electro-thermal aging of the metal and show that many parameters can influence the potential evolution of its microstructure, such as the composition of metallization and wire, the grain size, the interface created between the two metals. At the beginning of the chapter we also show the link between the on-state resistance of the device and the increasing in temperature of the power modules during aging.

Final considerations and possible perspectives of our study conclude this dissertation.

2

POWER ELECTRONICS FOR THE AUTOMOTIVE INDUSTRY, FAILURE MODES AND RELIABILITY ISSUE

At present, power electronics is the most advanced electrical energy conversion technology that attains both high flexibility and efficiency. As an engineering field, power electronics came into existence about 60 years ago, with the development and the market introduction of the so-called silicon controlled rectifier, known today as the thyristor [Owe07] [Holo1] [Lut11]. The structures of today's most important power semiconductor devices are shown in Fig. 1. Details on each power component will be given in the following section 2.1.

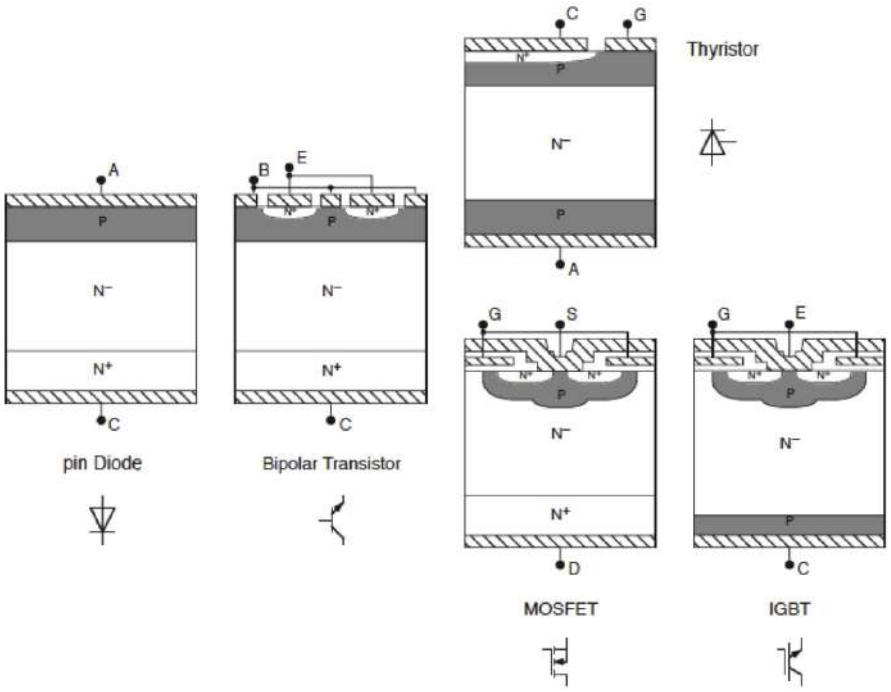

Figure 1: Basic structures of common power semiconductor devices [Lut11].

Fig. 2 illustrates the practical application range of each type of silicon device in classical switching power converters. Note that for these applications the operation ranges are within a hyperboloid. This suggests that the product of switching power (product of maximum voltage and current) and switching frequency that can be attained per device in practical conversion systems using silicon devices appears to be fairly constant. This frequency-power product is

a good performance indicator for how well the designer was able to maximize utilization of the power semiconductors and to improve the power density of the converter [Lut11]. For high power applications (> 10^3 kW), a GTO (gate turn-off) thyristor would be the first choice. However, they will be limited by a low switching frequency. On the other hand, for lower power applications, different possibilities could be taken into account depending on the switching frequency: bipolar transistor for low frequencies (< 10 kHz), the IGBT for medium frequencies (10-100 kHz) and MOSFET for high frequencies (> 100 kHz).

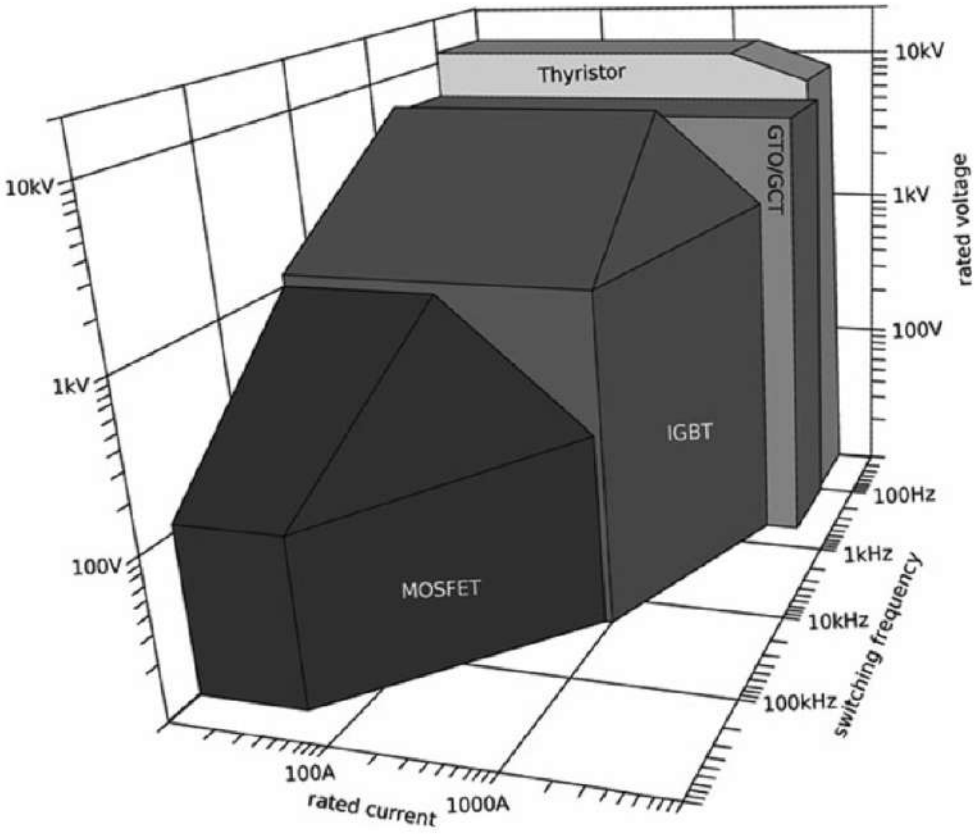

Figure 2: Operating range of silicon power semiconductor devices [Lut11].

In our study, we focus on smart power devices used as switches in automotive applications that require low power and high switching frequency. Thus, we will see that they are based on MOSFET technology, in particular vertical MOSFET controlled by a "smart" circuit that have sensor and protection functions [San99] [Tur03].

The devices under test will be described in section 2.2, together with the main reliability issues intrinsic to the structure and application field of the

devices. On the base of the failure analysis conducted on previous technologies developed by NXP [Mar10] [Mar14] [Kho07b] [Kho05], the weakest parts of the power device complex architecture have been identified as the metallic ones. In this work we will focus, thus, on the failure mechanisms involving the source electrode metallization and the relative bonding connections.

Our method to understand the physical mechanisms behind the device failure is described in section 2.3 and consists in putting the devices under accelerated electro-thermal aging and follow the degradation of the metal microstructure during aging. In this section we will focus on the description of the test protocols, whereas the physical metallurgy approach, used to study the metallization degradation mechanism and constituting the main part of this work, will be detailed in the next chapter.

2.1 POWER ELECTRONICS TECHNOLOGY EVOLUTION

This part provides an insight into the main basic structures of power semiconductor device. It has the purpose to summarize the evolution of the semiconductor electronics since the bipolar transistor until the more recent technologies, in terms of structure and operational mode.

2.1.1 *Bipolar transistor*

The bipolar transistor, or Bipolar Junction Transistor (BJT), was invented in 1948 at the Bell Laboratories by John Bardeen and Walter Brattain under the direction of William Shockley [Sho52]. The basic function of a BJT is to amplify current and they are then used in integrated circuits as amplifiers or switches.

A bipolar transistor consists of a three-layer sandwich of doped semiconductor materials, either NPN or PNP, separated by two PN junctions. The N areas contain an excess of electrons, whereas the P area an excess of holes (or a lack of electrons). The principle of operation of the two transistor types, PNP and NPN, is exactly the same the only difference being in their biasing and the polarity of the power supply for each type. A BJT has three terminals connected to the three doped regions: emitter, collector and base. In a NPN transistor, represented in Fig. 3, the base terminal is connected to the central P-type region, whereas in the PNP type to the central N-type one. The electrical parameters of a BJT are the I_E, I_C and I_B that are respectively the emitter, collector and base current and V_{BE} and V_{CB} that are the emitter base voltage and collector base voltage respectively.

If a tension V_{BE} is applied to the transistor, an electron current flows from the emitter to the base because of the difference of potential between the two electrodes. These electrons can diffuse until the collector, by applying a reverse

tension between the collector and the base (V_{CB}). In this configuration, a current flows from the emitter to the collector by applying a tension at the base (common base configuration). At this point, if V_{CE} is lower than a threshold ($V_{CE\,lin}$), then an important electron-hole recombination takes place at the base and the I_C current gain is low (saturation region). On the other hand, if the V_{CE} is higher enough ($V_{CE} > V_{CE\,lin}$), then majority of the electrons are collected at the collector terminal. The transistor operates in the linear region and the current I_C is independent from the applied tension V_{CB}.

Fig. 4 shows the qualitative characteristic curves of a BJT. The plot summarize the three regions of operation: the saturation, the cutoff, the active (each family of curves is drawn for increasing I_B values):

1. Cutoff region: the base-emitter junction is reverse biased, then no current flows in the device.

2. Saturation region ($V_{CE} < V_{CE\,lin}$): the base-emitter and collector-base junctions are forward biased, with $V_{CE} < V_{BE}$. I_C reaches a maximum value which is independent from V_{CE}.

3. Linear region ($V_{CE} > V_{CE\,lin}$): the base-emitter junction is forward biased, while the collector-base junctions is reverse biased, with $V_{BE} < V_{CE} < V_{CC}$. I_C is proportional to I_B, $I_C = \beta I_B$. The transistor can be considered as a current amplifier with gain β.

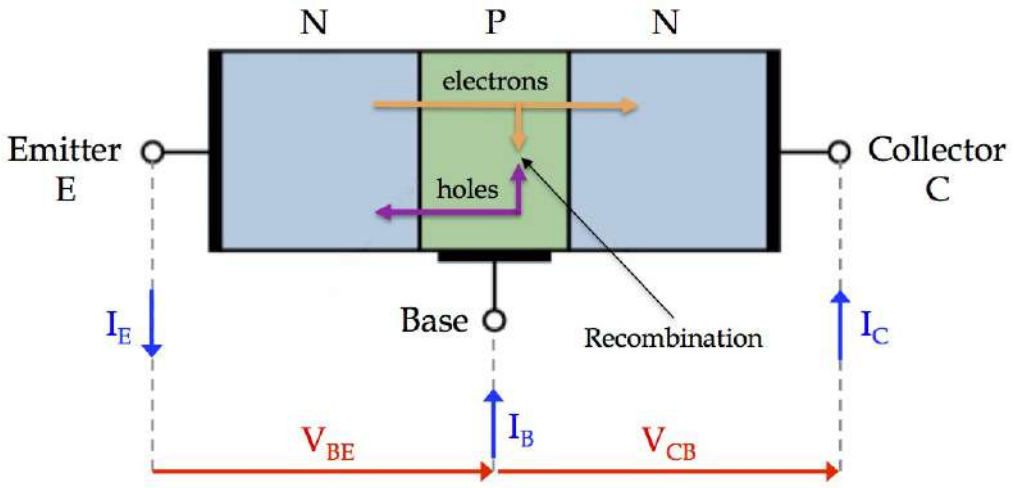

Figure 3: Bipolar transistor general structure.

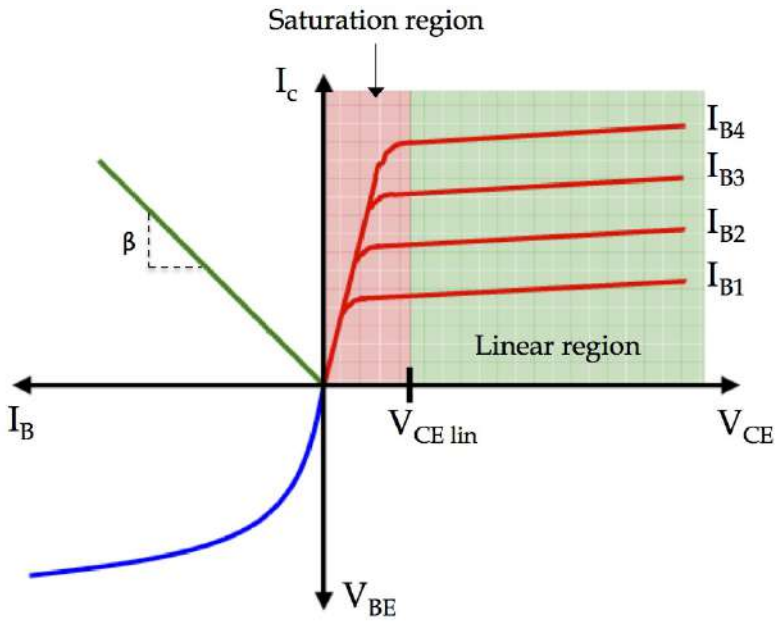

Figure 4: Electrical characteristic curves of a NPN bipolar junction transistor. The blue curve corresponds to V_{BE} = f(I_B). The red curves correspond to I_C = f(V_{CE}) at increasing I_B values. The red area ($V_{CE} < V_{CE\ lin}$) indicates the saturation region whereas the green one ($V_{CE} > V_{CE\ lin}$) the linear region. The green curve corresponds to I_C = f(I_B). β is the curve slope, that is the device gain.

2.1.2 *Thyristor*

Silicon controlled rectifier or thyristor is a family of semiconductor devices introduced by W. Shockley in 1950 [Sho51] and later developed by Ebers [Ebe52] [Mol56] [Mue58] as an evolution of the bipolar transistor.

Thyristor is basically a four layered pn junction device, with two p and two n portions and three p-n junctions J_1, J_2, J_3 (Fig. 5). It has three terminals, the anode and the cathode across the four layers, and the gate attached to the p-type layer near the cathode. As represented in Fig. 6, the thyristor operates in three different modes:

- Reverse blocking mode: the device is reverse-biased and behaves as a blocking diode.
- Forward blocking mode: voltage between anode and cathode (V_{AC}) is applied in the direction that would cause the diode to break down, but the thyristor is not triggered into conduction.
- Forward conducting mode: the thyristor has been triggered into conduction (V_{AC}>V_{BO} or I_G>0) and will remain conducting until the forward current drops below a threshold value (I_{AC}< I_H) known as the "holding current".

When the anode is at a positive potential V_{AC} with respect to the cathode with no voltage applied at the gate, junctions J1 and J3 are forward biased, while junction J_2 is reverse biased. As J_2 is reverse biased, no conduction takes place (Off state). Now if V_{AC} is increased beyond the breakdown voltage V_{BO} of the thyristor, avalanche breakdown of J_2 takes place and the thyristor starts conducting (On state). If a positive potential V_G is applied at the gate terminal with respect to the cathode, the breakdown of the junction J_2 occurs at a lower value of V_{AC}. This means that the value of V_G trigger the switching frequency of the thyristor. Once avalanche breakdown has occurred, the thyristor continues to conduct, independently from the gate voltage V_G, until the potential V_{AC} is removed or the current through the device (I_{AC}) becomes less than the holding current specified by the manufacturer (I_H).

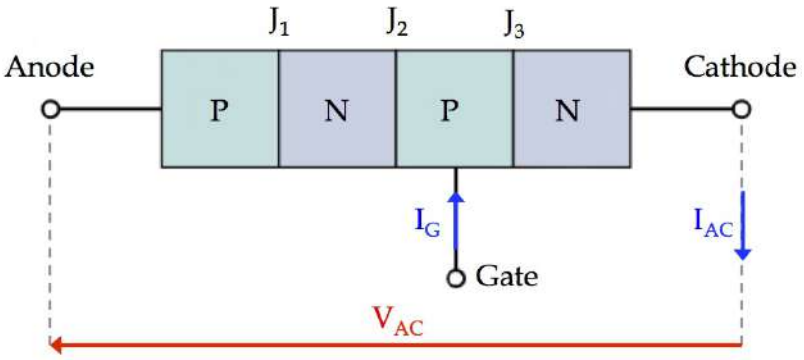

Figure 5: Thyristor general structure. Without the application of any voltage, it has three diffusion regions. If we apply a positive voltage at the anode with respect to the cathode, the junctions J_1 and J_2 become forward biased while J_2 is reverse biased. In this state, if a positive signal is applied at the gate terminal, J_2 turns to forward biased state and current starts to flow. On removal of gate signal, the current continues to flow as charge is drifted from anode to cathode.

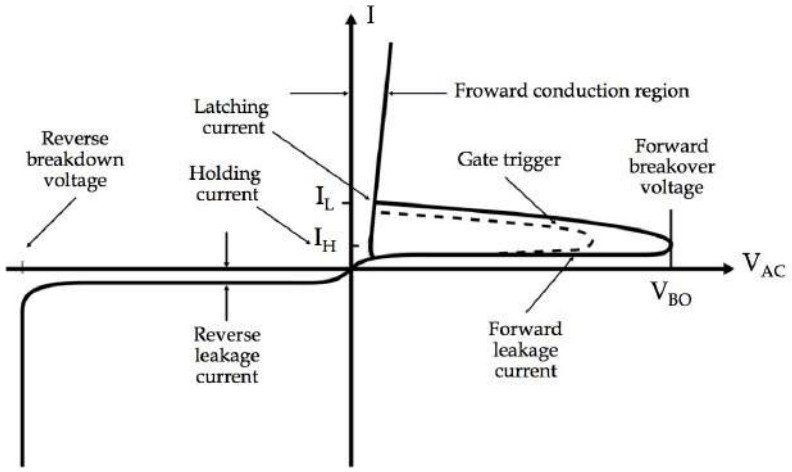

Figure 6: Thyristor static characteristic curve. The thyristor works under three modes: forward conducting mode, forward blocking mode and reverse blocking mode. The minimum anode current that causes the device to stay at forward conduction mode as it switch from forward blocking mode is called the latching current. If the SCR is already conducting and the anode current is reduced from forward conducting mode to forward blocking mode, the minimum value of anode current to remain at the forward conducting mode is known as the holding current.

2.1.3 *MOSFET transistor*

A MOSFET transistor (Metal Oxide Semiconductor Field Effect Transistor) is a semiconductor-base device widely used as switch or signal amplifier in electronic integrated circuits, with applications at high frequencies. The basic principle of the field effect transistor was first patented by Julius Edgar Lilienfeld in 1930 [Lil26], but it's only about thirty years after that Martin Atalla [Sho51] and Dawon Kahng [Sho51] from the Bell Laboratories developed the first MOSFET examples.

The main feature of the MOSFET transistors is the use of an electrical field to control the conductivity of a thin channel inside the semiconductor material. They distinguish operationally and structurally from the bipolar junction transistors since they involve single-carrier-type operation. Two different types of MOSFET exist, depending on the type of charge carriers flowing through the channel: holes in pMOSFETs and electrons in nMOSFETs. These, in turn, can work in depletion or enhancement mode, according to the polarisation of the device. In the following we will consider an n-type enhancement MOSFET as example to describe the transistor operational mode.

A MOSFET transistor consists in four electrodes, represented in Fig. 7: source (S), drain (D), gate (G) and the body (B). It is composed primarily by a large block, the body, of p-type silicon. Into the body, two regions of heavily doped n-type silicon are created to form the source and the drain. Gate is the controlling terminal and it is isolated from the rest of the transistor by an oxide layer sitting between the gate and the channel. This prevents current from flowing into/out of the gate, resulting in a high input impedances ($10^{12} - 10^{14}\Omega$) and a low power consumption, which make the MOSFET the fastest component during switching operations.

The transistor operation modes are represented in Fig. 8a and 8b, which describe respectively the I_D-V_{GS} and I_D-V_{DS} characteristic curves. By applying a potential difference between the gate and the body, the conductive characteristics of the channel region can be changed to allow current flow. If a small positive voltage is applied between gate and body (V_{GB}), the positive potential at the gate repels part of the charges creating a region with a small negative charge known as depletion region. As V_{GB} is increased, the depletion region grows. When V_{GB} is increased beyond some threshold voltage (typically a few V) an inversion layer of electrons is formed near the gate. This provides a conductive channel between drain and source which allows current to flow between source and drain and voltage drop across the two terminals. The body is generally internally connected to the source. This means that the gate to base voltage V_{GB} is the same as the gate to source voltage V_{GS} and to create the inversion layer V_{GS} needs to be above the threshold voltage (V_{th}). If V_{GS}

is less than V_{th}, no inversion layer is present and so no current can flow between source and drain and the transistor is said to be cut-off. When V_{GS} is greater or equal to V_{th}, the transistor is conductive. At this point, if $V_{DS} > 0$, the positive charge of the drain pulls electron away from the channel to be more distributed around the drain, where the inversion layer is smaller and the depletion region is larger than near the source. In this region, where $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$, the transistor is in the linear (or ohmic) region. It behaves as a voltage controlled resistor, where V_{GS} controls the resistance. The current I_D does not depend on V_{DS}. As V_D is increased, the depletion region near the drain continues to get larger and the inversion layer near the drain continues to shrink. At some point, the inversion layer entirely disappears and the drain is said to be pinched-off. Current still flows between source and drain and the potential difference is so large between the two terminals that electrons are able to push through the pinched-off area that contains few carriers. However, further increases in V_D results in minimal further increases in current, as the additional potential overcome the increased pinched-off region. The transistor is said to be in the saturation region.

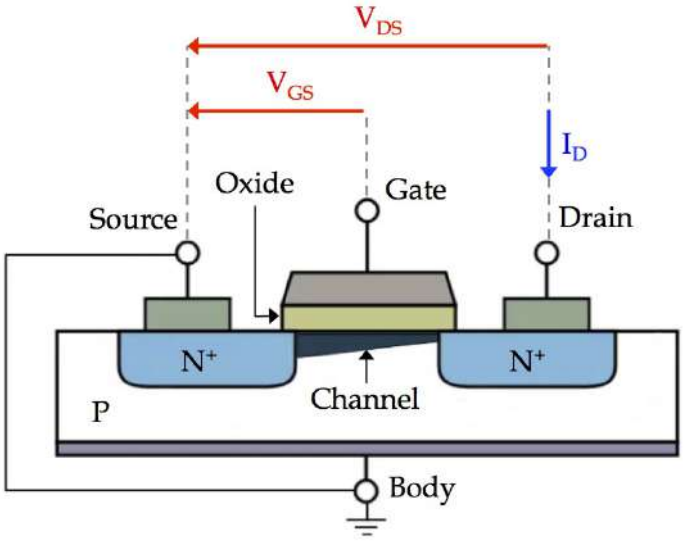

Figure 7: General structure of a nMOSFET. Under a positive V_{GS}, the charge carriers flow through the channel between source and drain.

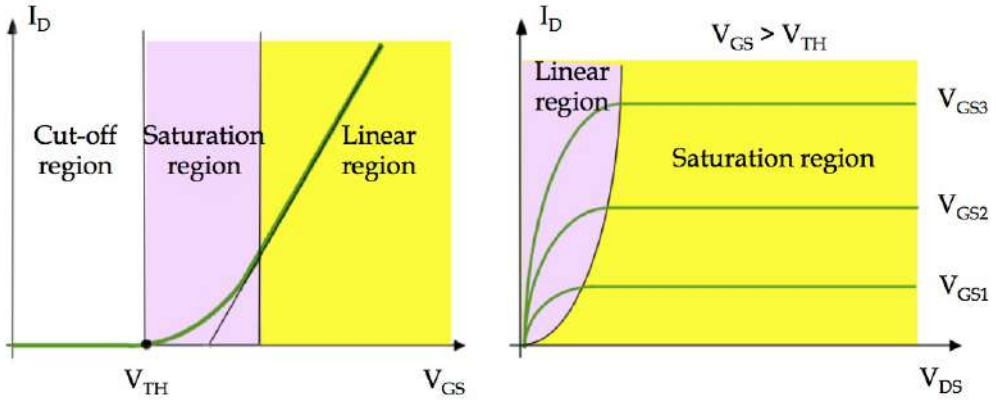

Figure 8: n-type MOSFET characteristics (a) $I_d = f(V_{DS})$ and (b) Id = $f(V_{GS})$

2.1.4 *IGBT transistor*

Insulated Gate Bipolar Transistor (IGBT) is the functional integration of power MOSFET and BJT devices in monolithic form. IGBT was developed in the 1980s by B.W. Scharf and J.D. Plummer to provide a superior alternative to bipolar power transistors [Rus83] [Bal84]. It combines the gate-drive characteristics of MOSFETs (high input impedance and application at high frequency) with the high-current and low-saturation-voltage capability of bipolar transistors (low on state power loss), to achieve the optimal device characteristics. The structure of an IGBT is very similar to a vertical MOSFET (see next section) with the difference that the block connected to the drain terminal is a N^+-type substrate in the vertical MOSFET, whereas in an IGBT it is P^+-substrate (Fig. 9). For this reason the IGBT is often described as an N-channel power MOSFET on top of a p+ type substrate. IGBTs operate in a similar way to MOSFETs. An inversion layer is formed in the P^+ area by applying a tension at the gate. However, if the potential of the collector is increased, the flow of electrons draws positive charges from the p-type substrate into the drift region, significantly increasing the conductivity of the channel region and dramatically reducing the voltage of the IGBT. This property gives the IGBTs a higher current density and capability compared to similarly gate-driven MOSFETs, resulting in low on-state power loss. Thus, IGBTs are specially designed to turn on and off rapidly in high-current applications.

2.1.5 *Recent solutions: trench technology*

In the last years, power semiconductor electronics have rapidly evolved in order meet the requirements of new applications involving smaller and smaller

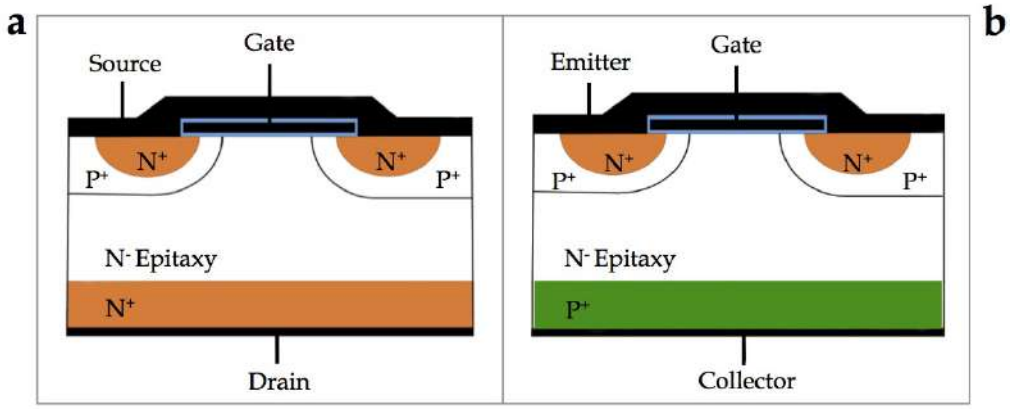

Figure 9: Comparison between (a) a vertical MOSFET and (b) an IGBT. The main difference consists in a n-type substrate in the vertical MOSFET and a p-type substrate in the IGBT (respectively in orange and green).

technology sizes and higher and higher current densities [Bayo8] [Isho4a] [Koro9]. The vertical trench technology is the most common configuration that we can find in the market nowadays, for both MOSFETs and IGBTs used in low power and high current densities application. In the following, a brief description of these components is provided, focusing, as example, on a MOSFET device, which is at the base of the technology under investigation in this work.

2.1.5.1 *Vertical MOSFET*

As suggested by the name, vertical MOSFETs (or VDMOS, Vertical Diffused MOS) differ from the lateral MOSFETs (Fig. 7) for their vertical structure (Fig. 10): the source electrode is placed over the drain, resulting in a current mainly vertical when the transistor is in the on-state [Mor96]. More precisely, the source is connected to a highly doped N^+ region that is confined insight a P region under the gate. The vertical channel is then formed between the latter and the N^- region below, connected to the drain electrode by a N^+ layer. The working principle and electrical characteristic curves of a VDMOS are exactly the same of a planar MOSFET (Section 2.1.3):

- If the gate to source voltage (V_{GS}) is lower than a threshold value (V_{th}), a depletion layer is formed in the P area. The channel is isolated and the transistor is cut-off.
- When V_{GS} is greater than V_{th}, the carrier inversion layer is formed in the channel and the transistor is in the on state: an electron current, linearly proportional to the tension applied at the gate, flows from the source to the drain.

Thanks to its vertical structure, the main advantage of a VDMOS device consists in the possibility of a high integration of many small symmetrical cells connected in parallel to the same source metallization, at surface, and drain layer, which is directly connected to the device substrate. It is, then, the gate width that determines the number of cells which can be integrated in a single VDMOS device. Moreover, contrary to a planar structure, in which the current and breakdown voltage ratings are both functions of the channel dimensions, in a vertical structure, the voltage rating of the transistor is a function of the doping and thickness of the N^+ epitaxial layer, while the current rating is a function of the channel width. This makes it possible for the VDMOS to sustain both high blocking voltage and high current within a compact piece of silicon. For these reasons, vertical power MOSFETs are typically employed in applications that involve high power densities in single device packages of power modules.

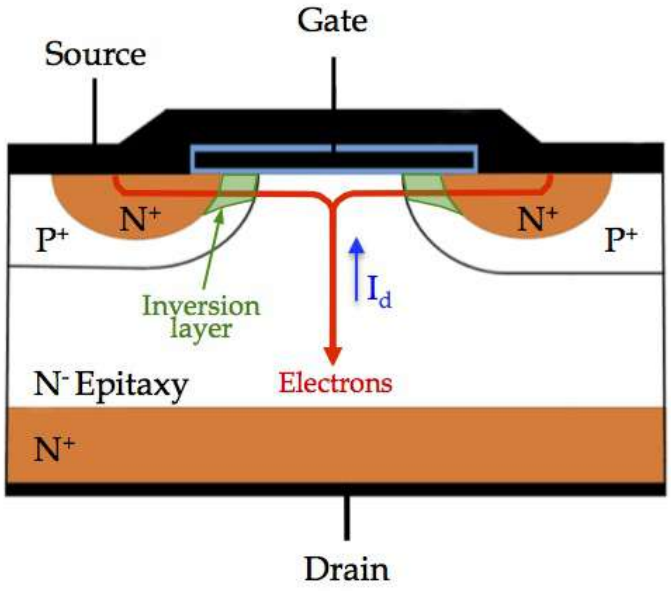

Figure 10: Schema of a VDMOS.

2.1.5.2 *Trench MOSFET*

Different kinds of VDMOS exist depending on their structure: planar MOS, V-groove MOS (VMOS), trench MOS (UMOS), etc.

In a trench MOSFET, also called UMOS, the gate electrode is buried in a trench etched in the silicon. The comparison between a vertical v-groove structure (VMOS) and a trench structure is depicted in Fig. 11.

The fabrication process of a trench MOSFET is shortly described by Williams et al. [Wil17]. As shown in Fig. 11b after forming the VDMOS source and body regions, an etched trench of narrow width (e.g., 0.8 to 1.5 µm across) is oxidized to form a gate oxide lining the trench and subsequently filled with phosphorus in situ doped polysilicon. A polysilicon CVD deposition completely fills the trench, overflowing the etched trench onto the silicon surface. Except for a small masked area needed for gate contact, the polysilicon is then "etched back" so that the top surface of the polysilicon gate is recessed, but still overlapping the N^+ source. Subsequent thermal oxidation caps and seals the recessed polysilicon with a protective layer of oxide. A contact mask then selectively exposes the transistor's surface gate and its numerous cellular source/body regions to an oxide etch (while protecting the oxide above the trench). After contact etch, metal deposition and photolithographic patterning are performed interconnecting a series of separate and distinct trench VDMOS cells into a single three-terminal trench power MOSFET. Except for the polysilicon gate contact, the resulting die surface is nearly planar, so that problematic step coverage issues of the v-groove structure (Fig. 11a) are completely eliminated. The resulting cell pitch was half that of any other vertical device, improving channel-resistance, epitaxial current uniformity, and total $R_{DS(on)}$. As represented in the graph of Fig. 12, increasing cell density of a trench MOSFET decreases the devices $R_{DS(on)}$ hyperbolically. In contrast, planar VDMOS or VMOS exhibit a U-shaped dependence, declining in $R_{DS(on)}$ with increasing density before reaching a minimum, then rising rapidly at higher densities as a result of a decrease in channel packing density and poor current uniformity in the epitaxial layer [Wil17].

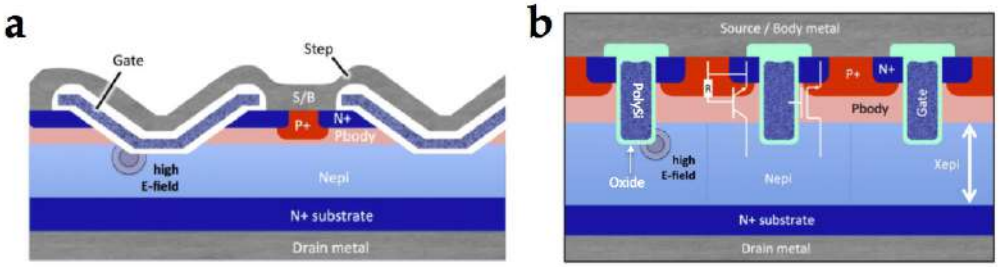

Figure 11: Cross section of (a) a v-groove VDMOS (or VMOS) and (b) of a trench gate vertical MOSFET (or trench VDMOS) [Wil17].

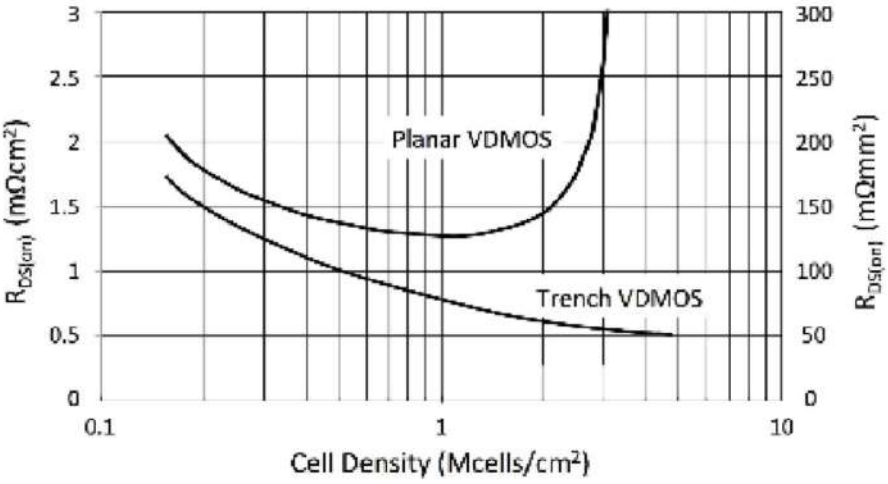

Figure 12: Impact of cell density on $R_{DS(on)}$. Planar VDMOS exhibits a minimum while trench VDMOS benefits from scaling [Wil17].

2.2 SMART POWER MOSFET FOR THE AUTOMOTIVE INDUSTRY: RELIABILITY ISSUE AND DESCRIPTION OF THE DEVICES UNDER TEST

In this work we focus on low voltage MOSFET-based smart power devices used as lightning switches in car and truck applications. Fig. 13a shows an example of e-switch smart power MOSFET from NXP Semiconductors.

Fig. 13b represents the main parts composing the layered structure of a power device for standard low voltage applications:

- Power die. It is theMOSFET active area of the device, consisting mainly in the Si block coated by the source top metallization layer, generally made out of Al or Cu. In the "smart" power modules, the power die is connected to a control die (soldered on the same lead frame) with sensor and protection functionalities.
- Internal bonding connections. They allow a low-resistance current flow through the power die. Al or Cu bonding wires (Fig. 14a) are ones of the most common solution used at the moment. Several wire bondings, which a standard diameter that varies from few tens of micrometers to a maximum of 500µm, are connected in parallel in order to support and distribute high currents. Ribbon (Fig. 14b), clips and ball-bonding (Fig. 14c) are other examples of bonding internal connections that we can find in the commercial power devices.
- Lead frame. It serves primarily to support the chip mechanically during the assembly of plastic packages and to connect the chip electrically with

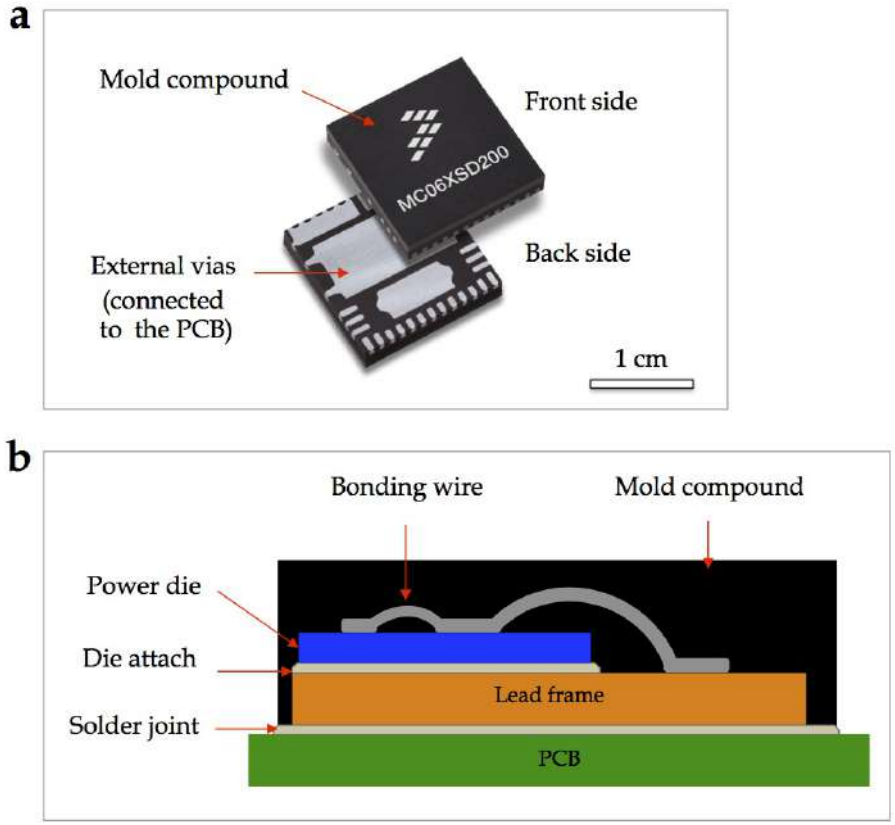

Figure 13: (a) Power MOSFET device from NXP Semiconductors for low voltage applications. (b) Schematic representation of the cross-section of the power MOSFET. The lead frame, made out of Cu, serves as heat sink and is directly soldered on the PCB. The bonding wires are cold welded on the Al top metallization by ultrasonic process. The device is encapsulated in a plastic mold compound.

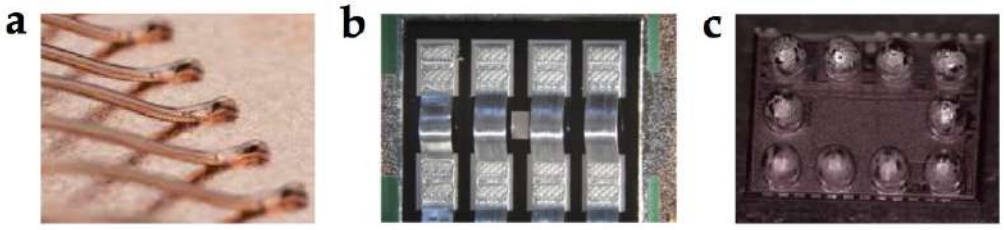

Figure 14: Examples of internal bonding connections in a low voltage power module. (a) Cu bonding wires, (b) Al ribbons, (c) ball-bonding [San17].

the printed circuit board (PCB). It has also the function of a heatsink as it is made of a thick Cu plate.

- Solder joints. They allow the electrical and thermal contact between power die and lead frame and between lead frame and PCB. The most common alloys used nowadays are lead-free and are made out of tin, silver and copper (Sn-Ag-Cu). Many studies are focusing on these replacement solder materials [Lee17] and will be addressed later in section 2.2.2.1.

- Mold compound. It is the most widely used polymer-composite packaging material for encapsulating low voltage power devices [Pro03]. The main function of the epoxy-based package is to provide environmental and mechanical protection for the devices. It must deliver a balanced combination of properties in the areas of mechanical strength and toughness, chemical resistance, electric insulating performance, thermal conductivity and moisture stability in the range of -65 to 200 °C. In order to control thermal conductivity, internal stress characteristics and reliability performances, filler particles (commonly made out of silica or alumina) are integrated in the epoxy resin [Ham89].

2.2.1 *Stress conditions in power electronics for automotive*

Power electronics for automotive must comply with standard qualification requirements described in the AEC-Q100 documents, developed by the Automotive Electronics Council (AEC) component technical committee. These documents contain detailed qualification requirements for integrated circuit and include failure mechanisms based stress test methods. Components meeting these specifications are suitable for use in the harsh automotive environment.

The basic standard lifetime requirements for passengers vehicles today are:

- Lifetime: 15 years
- Operation time: 10.000 hours
- Mileage: 300.000 km

In the following, we provide a short description of the main stresses at which power electronics for automotive are subject during their normal operational mode.

2.2.1.1 *Thermal stress*

During their on-off operating cycles, power components undergo passive and active thermal cycles. They are subject to extremely diverse external climate

conditions. At the same time, when the vehicle is on, the motor compartment warms up to 130°C [Kas01] [Bou08]. This results in passive thermal cycles from - 40°C to 130°C [Sch10]. On the other hand, active thermal cycles correspond to the temperature increase due to Joule heating and thermal dissipation. The combination of these two stresses can severely influence the power electronics reliability, especially when the external temperature is high. In automotive applications, power devices are designed to tolerate a maximum operating temperature of 175°. When this value is reached, the integrated control circuit turns the device off as protection. The thermal amplitude in a single on-off cycle is not critical for the materials composing the device layered structure. However, the iteration of these thermal cycles induces important stresses in the electronics components during their life-time due to the difference in the coefficients of thermal expansion (CTE). These stresses can locally induce plastic deformation in the softest parts (solders, metallization, bonding wire, mold compounds) and cracks in the most fragile parts (oxides and silicon). This problem of CTE difference will be further addressed in "Source metallization" section (2.2.2.2).

2.2.1.2 *Electromagnetic stress*

The electromagnetic interferences (due to high tension power lines, mobile phones, radio waves, etc.) and the vehicle system itself can cause a transient electrical noise that can interfere with the electrical components in the vehicle. Ignition and lighting system, electromechanical actuators, starters, alternators, etc. are the source of potential electromagnetic noise. The manufacturer must comply with electromagnetic compatibility and emission regulations [Mar11].

2.2.1.3 *Mechanical and chemical stress*

Mechanical stress arises from the deformations and vibrations of the engine system. The parts that are the most sensitive to this stress are the solder joints and the bonding connections.

In addition, the devices are affected by environmental conditions as moisture, fog, saline atmosphere, etc. that can cause corrosion in the device components. The plastic packaging play an important role to protect the power device from the aggressive environmental factors.

2.2.2 *Failure modes in power MOSFETs*

Reliability is defined as the ability of an item to perform a required function under stated conditions for a certain period of time, which is often measured by probability of failure, by frequency of failure, or in terms of availability

[Ele12] [Wan13]. Power device failure or degradation can be caused by external factors, such as moisture, temperature, vibrations, mechanical shock, etc. (see previous section 2.2.1), or internal factors, such as, for instance, the normal usage of the component or repetitive high current cycles, associated to thermal cycles (due to the Joule effect), that result in fatigue degradation of the main parts composing the device. These kinds of degradation or failure correspond then to the final part of the typical failure rate profile ("bathtub" curve - Fig. 15) as a function of the device life-time. The failure rate in this stage increases with the usage duration and the device aging and this defines the life-time of the device.

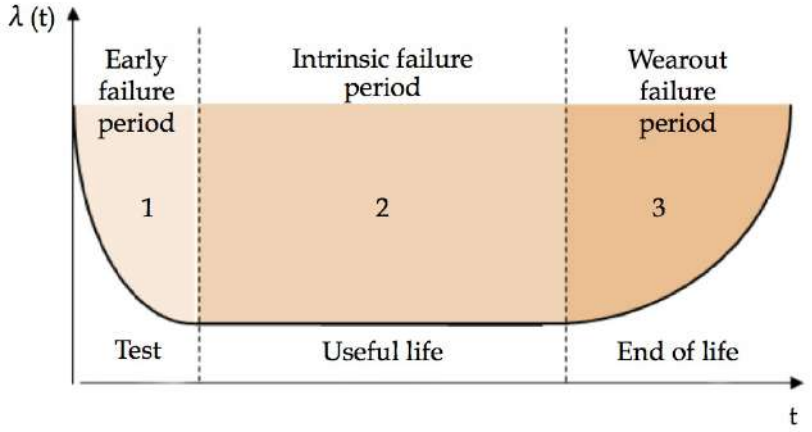

Figure 15: Bathtub curve of failure rate.

Considering our specific application field, power switches driving the vehicle light system are located far from the engine system. Thus, the mechanical stress and the thermal variations generated by the engine system, can be neglected. The main stress they undergone is the electro-thermal one. In fact, during their life, the components undergo several short-circuits and avalanche [Ber10] events, inducing thermo-mechanical effects, added to the normal thermal excursions due of the environment in which they operate. These repetitive electro-thermal stresses produce degradation effects at the interfaces between the different materials composing the device structure, because of the difference in their physical properties (table 1), and in particular in the coefficients of thermal expansion (CTE).

Fig. 16 shows a schema of a smart power device with the main critical parts during electro-thermal aging: the solder joint and the metallic parts (source electrode metallization and bonding wires). In the following the associated failure mechanisms are described. In this work, we will focus on the failure mechanisms of the metallic parts.

Table 1: Physical properties of the main representative materials at 25°Cl [Pie11].

Function	Semiconductor	Conductor		Solder
Material	Si	Al	Cu	$PbSn_5Ag_{2.5}$
CTE $[10^{-6}/K]$	4.15	23.1	16.5	21
Young modulus [GPa]	131	70	120	10
Poisson ratio	0.27	0.35	0.34	0.4
El. cond. $[\Omega^{-1}m^{-1}]$ (doping dependent)	10^{-3}	$37.7 * 10^6$	$59.6 * 10^6$	$6.67 * 10^6$
Thermal cond. $[Wm^{-1}K^{-1}]$	148	237	385	50
Thermal capacity $[Jkg^{-1}K^{-1}]$	752	897	385	150

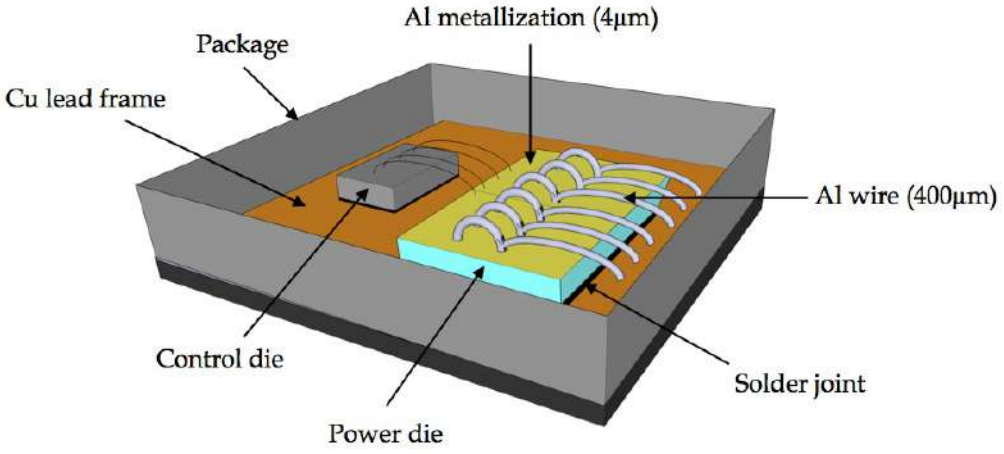

Figure 16: Schematic representation of a LFET1T-like smart MOSFET power device. The critical points subject to electro-thermal stress are: die/leadframe solder joint, Al source metallization, bonding wires.

2.2.2.1 *Die/substrate solder joints fatigue*

The solder joint between the Si substrate of the power die and the Cu lead frame ensures their thermal, electrical and mechanical contact. At increasing temperature, the power die heating is transferred through this connection to the lead frame where it is dissipated. Since 2006, after the restriction of the use of hazardous substances in electronic equipments, the lead-based soldering process has been replaced by high temperature (> 270 °C) process and Pb-free solders, consisting essentially in Sn-Ag-Cu alloy, are more and more used from the electronics manufacturers. The low elastic limit of these materials induces deformation in the solder layer even at low stress. In addition, the CTE mismatch between Si and Cu can strain the solder joint connection, and over the component lifetime can contribute to mechanical solder joint fatigue failure [Lee00]. Two phenomena can then occur during the electro-thermal aging of the device: cavities multiplication and delamination starting from the edges of the solder towards the center (Fig. 17). Both of them limit the current flow in the solder layer, increasing the $R_{DS(on)}$ of the device. It has been demonstrated that the less is the solder thickness the more fragile is the solder [Hay02] [You15] [Gué02]. However, an increase in the thickness results in a increase in the thermal resistance of the solder layer, because of the low thermal conductivity of the materials constituting the solder. A trade-off between thermal conductivity and mechanical strength is then required in phase of design of the solder interface.

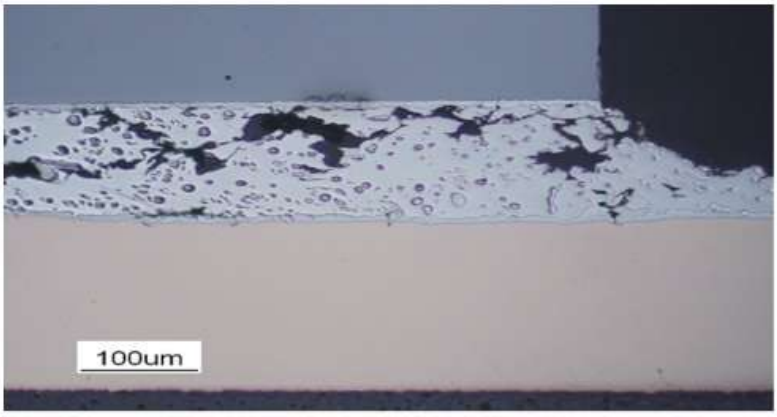

Figure 17: Delamination of a lead-free solder joint between the die Si substrate and the Cu lead frame [Bou08].

2.2.2.2 *Failure modes in the active zone*

The active zone of the power device corresponds to the MOSFET die and the bonding wires connected to the source metallization. In this area, the electro-thermal cycles induce mechanical stress in the softest parts of the complex layered structure that, by nature, consists in the interconnection of different materials (metal-oxide-semiconductor) and constitutes the MOSFET device. They are the Al source metallization and bonding wires, which have higher coefficient of thermal expansion respect to the oxide and the Si (table 1).

Source metallization

Reconstruction of the aluminum metallization is an effect observed since the early times of microelectronics [San69] [Phi71]. During thermal cycling of IGBT and MOSFET devices, periodical compressive and tensile stresses are introduced in the thin metalization film by the different CTEs of the aluminum and of the silicon chip, due to the large thermo-mechanical mismatch between both materials and due to the stiffness of the silicon substrate [Cia02]. The thermo-mechanical stresses in the Al results in the gradual change in its granular structure. Fig. 18 shows the comparison between the Al metallization surface in a power MOSFET before and after electro-thermal cycles. The aged metal is characterized by an higher roughness and cracks along the grain boundaries.

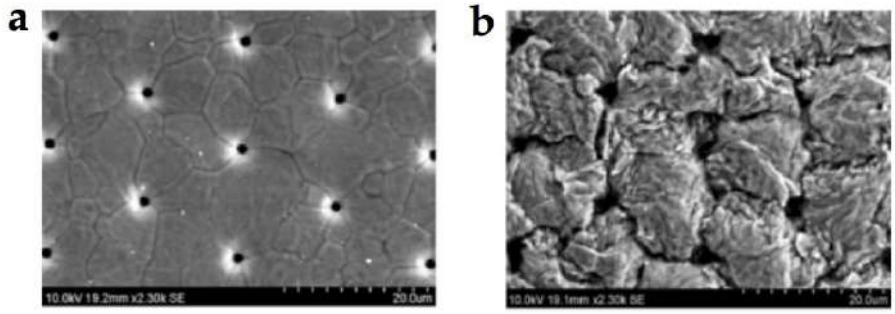

Figure 18: Electro-thermal ageing of the source electrode metallization in a smart power MOSFET. Scanning electron micrograph of the (a) fresh metallization and (b) at failure [Pie11].

To assess the stress seen in interconnects during operation, Flinn and coworkers [Fli87] considered the simplest approximation of a chip: a metal layer deposited on a silicon substrate. They measured the stress arising during thermal

cycles due to the mismatch between both materials using a laser reflectometer set up and the approximation of the Stoney equation [Sto09] [Fre99] [Jan09].

$$\sigma_f = \frac{E_s t_s^2}{6(1-\nu)t_f R} \tag{1}$$

In this equation, only the thicknesses of both film and substrate (t_f and t_s) are needed, along with the substrate Young's modulus and Poisson's ratio (E_s and ν). The film stress σ_f is then directly deduced from the radius of curvature R measured by the laser. Because the substrate is more rigid and does not plastically deform at room temperature, most of the plasticity is expected to occur in the metallic film. In their first paper, the metallization was an Al-1%Si thin film and the cycles were performed from room temperature to 400 °C at a rate of about $20°C/min$. During the process, the Al layer would go from slightly tensile to compressive stresses (max 100 MPa) during heating, before deforming plastically in tension during the cooling, up to a stress of 300 MPa (Fig. 19).

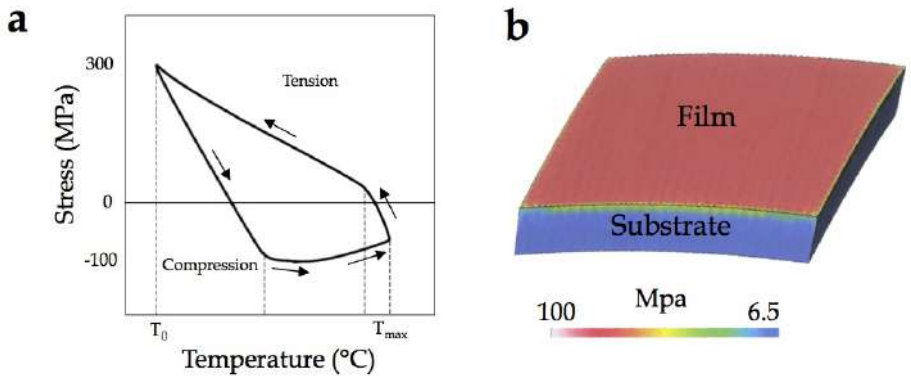

Figure 19: (a) Typical stress-temperature cycle for a 1-µm-thick poly-crystalline Al film on oxidized Si substrate ($T_{max} \sim 450°C$). (b) Finite element simulation showing the Von Mises stresses generated by a temperature change of 50 °C in a 1 cm x 2cm x 0.5 mm specimen (typical size used in wafer curvature) [Leg09].

Several publications followed (a nice and recent review can be found in Wiederhirn's thesis [Wie07] and established that the film strength [1] increased as the inverse of the film thickness. This increase in film thickness was then rationalized in term of threading dislocation movements by Nix in 1989 [Nix98],

1 During thermal cycles, metallic thin films experience two yield stresses, at the end of the elastic compression stage (heating) and in tension during cooling. The maximum stress is usually reached at the end of the cooling and is considered as the "film's strength"- see [Leg06]

from an initial calculation of image forces in thin films by Matthews and Blakeslee [Mat74] [Mat75]. Later on, this model was questioned [Mue98] [Leg09] because the amorphous layer between the Si substrate and the metal film (usually Si oxide), acted as a dislocation sink. This later effect may however reflect an artifact of TEM observation because Si oxide seems to soften significantly under electron beam [Zhe10]. In any case, the reversible motion of threading dislocations (Nix's model) cannot explain the strong and non-crystallographic roughening of Al films on Si, observed in power mosfets ([Pie11] or plain thin Al films on substrates [Tur92] [Leg05] [Kao03].

Another approach consisted in applying the Frost and Ashby deformation mechanisms maps [Fro82] to the stress/temperature cycles. These maps and equation were established for bulk materials and link a given plastic strain rate $\dot{\varepsilon}$ to a given stress and temperature. By comparing the predicted stress/temperature cycles using these maps and the experimentally established one (by laser curvature), Bostrom [Bos01] showed that a large discrepancy existed between both approaches, underlying the fact that thin films on substrate deformed in a specific way.

Recently, a qualitative model adapted to the bamboo-microstructure of thin film was developed to explain how the plastic deformation proceeded by atomic self diffusion of Al atoms along the grain boundaries (GBs) [Mar14]. These GBs, acting as fast diffusion paths would gradually open during tension (cooling phase). During heating, the Al atoms are expelled to the surface through the same GBs, as predicted by the model from Gao [Gao99], and contribute to its roughening. The irreversibility of the process is due to the native oxidation of cracks surfaces that will prevent crack healing during compression.

Bonding wires

Reliability of bonding connections in power modules, and in particular of wire bonds soldered on the source electrode metallization by cold-bonding process, is an important issue for the reliability of power systems because of extending operation temperatures (due to the Joule effect in the wire itself and to the power dissipation in the Si substrate) which induce high levels of thermo-mechanical stress in the bonding area [Cia02] [Gla04] [Dup07]. Ramminger et al. [Ram00] described and modeled this cyclic stress as wire flexure by thermal expansion or wire deformation under mechanical shock loading if the bond surfaces are able to move relatively to each other (Fig. 20).

As consequence of this stress, mainly two kinds of failures of wire bonds have been reported in the literature:

1. Heel crack failure (Fig. 21a), originating from bending caused by thermal expansion or by mechanical deformation of the wire [Meh99] [Cia02].

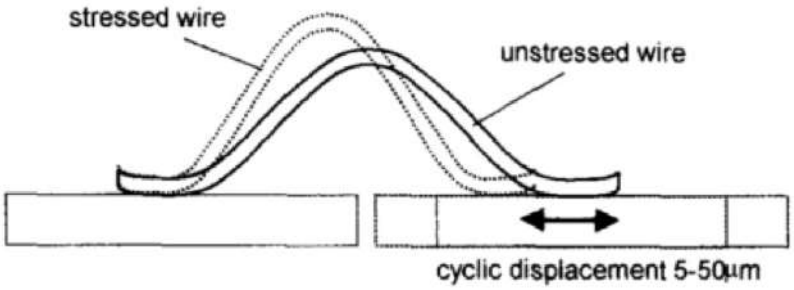

Figure 20: Bonding wire subjected to cyclic mechanical stress applied by lateral displacement of one bonding area relatively to the other in Ramminger et al. experiments [Ramoo].

2. Bond wire lift-off (Fig. 21b), resulting from material fatigue at the chip metallization. This is caused by shear forces which result from the different coefficients of thermal expansion on the interface [Ber98] [Ciao2].

These degradation modes have been mainly observed in components that undergo active cycles and rarely under extreme conditions (avalanche or short-circuit). In the latter case, the metallization is the location most prone to degradation, but even in the cases of faster bonding failure, metallization reconstruction is always observed [Sme11].

The failure mechanisms at the bonding connections are generally studied combining experimental test and simulation. Ramminger has demonstrated, by a finite element model based on stress experiments, that the number of cycles to heel crack failure is strongly dependent on the loop geometry [Ramoo]. He has also considered that cracks in the bonding wires and at the wire-metallization interface do not propagate towards the metallization because of its higher yield strength [Ram98]. The layout of the bonding connection also play a role in the reliability of power device. According to Ishiko et al., the reliability of IGBT components can be improved by optimizing the wire position configuration by thermo-electric simulation in order to make the temperature distribution of the devices more uniform [Isho6].

In parallel to the studies in simulation, the microstructure of the bonding wires has been inspected in order to investigate the influence of the grain structure evolution on the crack growth and the device life-time. Yamada et al. [Yamo7] showed that the crack growth increases with the number of thermal cycles (from -40 °C to 200 °C), resulting in a reduction of the residual bonding length of Al wires that seems to be independent by the limited recrystallization of the wire grains at high temperature.

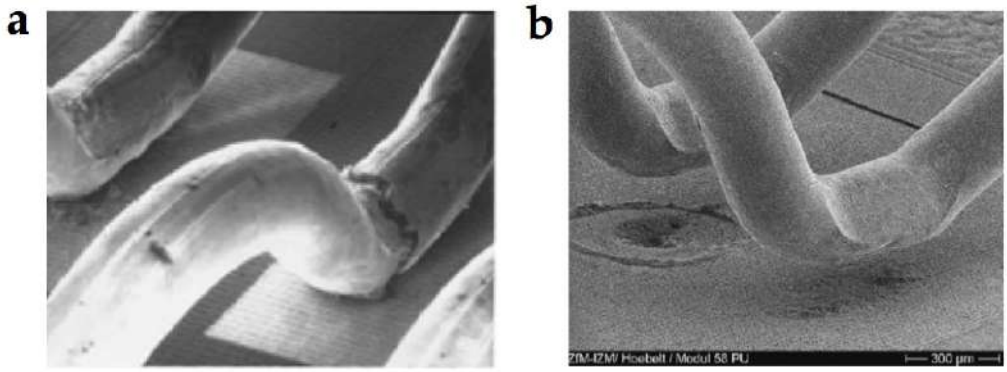

Figure 21: Examples of bond failures in power components: (a) heel crack failure [Cia02] and (b) wire lift-off [Den17].

2.2.3 *Thermosensitive aging indicators*

The electro-thermal aging of power devices, either IGBTs or MOSFETs, is associated with the evolution of the electrical parameters, such as V_{TH}, I_{DSsat}, on-state resistance ($R_{DS(on)}$). They are then aging indicators as they can be monitored during the device testing procedures to assess its aging and predict their life-time. During our characterization we have focused on the $R_{DS(on)}$ evolution.

2.2.3.1 $R_{DS(on)}$

During the on state, in the linear region, the VDMOS can be considered as a resistance between drain and source: the $R_{DS(on)}$, defined as the ratio between the drain voltage and current when V_{DS} approaches zero (Fig. 22a). It is one of the main parameters of a power MOSFET: the goal during the design of a power MOSFET is to lower this resistance in order to limit the device self-heating and the voltage reduction during the on state. The $R_{DS(on)}$ value depends on the voltage applied at the gate terminal, and so on the channel size.

The on-state resistance $R_{DS(on)}$ can be considered as the sum of several components as shown in Fig. 22b:

$$R_{DS(on)}(V_{GS}) = R_S + R_{CH}(V_{GS}) + R_A(V_{GS}) + R_J + R_D + R_{SUB} \tag{2}$$

Where:

- **R_S** = Source diffusion resistance.

  It is made up of three elements: the bonding wires resistance (R_{wire}), the metallization layer resistance (R_{metal}) and the N^+ wells resistance (R_{N^+}).

This contribution is greater than the resistance at the drain (R_{SUB}) because of the high resistivity of the long bonding wires cold welded by ultrasound on the source film. Compared to R_{metal} and R_{wire}, R_{N^+} is then negligible, due to the low thickness ($< 1\mu m$) and high doping of the N^+ well.

- **R_{CH}** = Inversion channel resistance.

  It represents one of the main contribution to the total $R_{DS(on)}$ and it is inversely proportional to the channel width and, for a given die size, to the channel density:

$$R_{CH} = \frac{1}{\frac{W}{L_{eff}} C_o \mu_E (V_G)(V_{GS} - V_{th})} \tag{3}$$

  where W and L_{eff} are respectively width and length of the channel, C_o the electrical capacitance of the gate oxide per surface unit, μ_E the electron mobility in the inversion layer and V_{th} the threshold voltage. On the basis of this equation, three solutions can be adopted to lower the $R_{DS(on)}$:

  1. Shortening the inversion channel length (L_{eff}). However after a limit value (pinch-off) we have the formation of a gap between the source and the drain [Mor96].
  2. Increasing V_{GS}. However, for voltage higher than 20 V there is the risk to damage the gate oxide.
  3. Increasing the inversion channel length (W) per surface unit by decreasing the single cell sizes.

- **R_A** = Accumulation resistance.

  It represents the resistance of the accumulation region in the epitaxial zone under the gate electrode, where the direction of the current changes from horizontal (in the channel) to vertical (to the drain contact). The resistance is described by the following equation [Sun80]:

$$R_A = \frac{1}{3} \frac{1}{\frac{W}{L'_{eff}} C_o \mu_a (V_G)(V_G - V_{TD})} \tag{4}$$

  whereμ_a is the electron mobility in the accumulation layer, L'_{eff} the effective length of the channel in depletion mode and V_{DT} a voltage depending on the doping concentration inside the epitaxial region. In order to reduce this resistance, the channel length needs to be increased, that means that the power device cells must be tightened.

- **R_J** = "JFET" component-resistance between two P body regions.

  It is due to the formation of a bottleneck in the charge carrier path between the two P areas. This is the detrimental effect of the cell size reduction mentioned above: the P implantations form the gates of a parasitic JFET transistor that tend to reduce the width of the current flows in the N^- epitaxial region. This junction is modulated by V_{DS}: an increase in V_{DS} determines the bottleneck shrinkage. In order to prevent this contribution increasing the $R_{DS(on)}$, the distance between the transistor cells must be increased, contrary to the considerations made for the other resistances.

- **R_D** = Drift region resistance

  It represents the resistance of the epitaxial layer. The role of this layer is to sustain the blocking voltage, so R_D is directly related to the voltage rating of the device. A high voltage MOSFET requires a thick, low-doped and highly resistive epitaxial layer, whereas a low-voltage transistor requires a thin layer with a higher doping and less resistive layer. As a result, R_D is the main factor responsible for the resistance of high-voltage MOSFETs.

- **R_{SUB}** = Substrate resistance

  It is the resistance of the drain, including the resistance of the N^+ substrate (R_{N^+}) and the package connection. The R_{N^+} contribution here is significantly higher than in the source because of the higher thickness of the drain layer (few hundreds microns). However, R_{SUB} is overall lower than R_S because of the absence of the wire bondings (the device substrate is directly soldered on the Cu lead frame).

In power MOSFET-based devices for low voltage and high current applications, like the components studied in this work, the sum of the source and drain contributions (R_S+R_{SUB}) represents more or less the 50% of the total $R_{DS(on)}$. In this study, we focus on the metallization that shows degradation and thus resistance increase during electrical cycling [Kho07b].

2.2.4 *Devices under test: 45V and 65V LFET1T technology*

LFET1T is the commercial name of the technology developed in 2008 by NXP Semiconductors (at that time Freescale) for automotive low voltage (< 48V) and frequencies (< 1 kHz) applications and based on trench MOSFET modules. Two versions of this technology have been characterized in this work:

1. 12V SPD06 (Fig. 23a), designed for 12 V batteries in car applications, with breakdown voltage of 45V. They consists in 2 MOSFET sectors, each one connected by 3 bonding wires and having a $R_{DS(on)}$ of 6 mΩ.

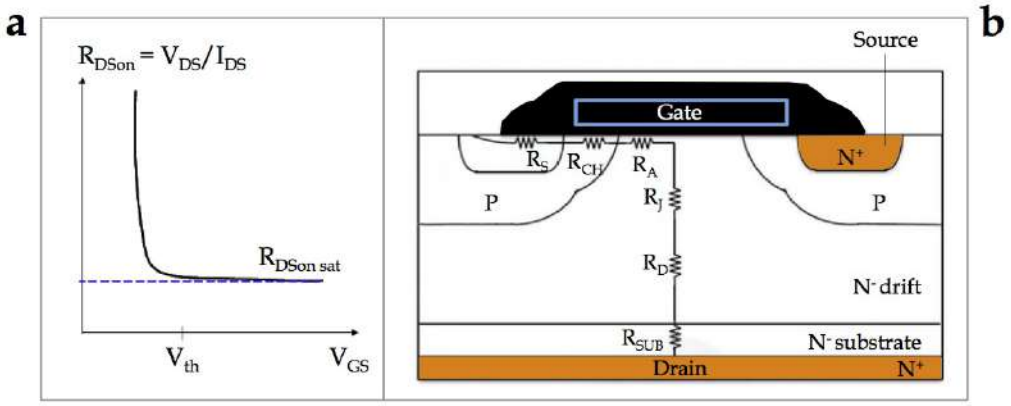

Figure 22: MOSFET vertical structure, showing the total resistances that make up R_{DSon}.

2. 24V T07D17 (Fig. 23b), designed for 24V batteries in truck applications, with breakdown voltage of 65V. They consists in 5 MOSFET sectors, connected by 8 bonding wire and having a $R_{DS(on)}$ of 17 mΩ and 7 mΩ.

The trench MOSFET structure, with a small cell pitch of $\sim 1-2\mu m$ (Fig. 24b) allows the LFET1T modules to get three times higher channel current densities ($> 1000mA/in2$) compared to the previous generation of NXP power MOSFET devices based on a planar structure (Fig. 24a), together with a reduction in die and package sizes (and thus cost). However, this also implies a higher possibility of thermal instability of the device. For this reason, an isolated poly-diode for temperature sense has been integrated in the technology. The details of the technology are summarized in table 2, showing a comparison between the 12V SPD06 and 24V T07D17 modules. The composition and thickness of the source metallization and bonding wire are the same in both modules. The source metallization consists in an aluminum (Al) film of 0.5 wt% of copper (Cu) and tungsten (W), coated (only in the 24 V devices) by a $0.5\mu m$ thick SiO_2 passivation layer everywhere, except in the bonding areas. The wire bonds are made out of pure Al and have a diameter of $400\mu m$. The Al bonding wires are contacted to the Al source metallization by a classical cold-bonding process by ultrasound [Bro15] [Goe12]. The bonding parameters are reported in table 3. The bonding force of 10 N applied to an area of $450 * 750\mu m^2$ results in a bond stress of $\sim 30MPa$. These values are in line with the bonding parameters optimized by Goehre [Goe12].

Table 2: LFET1T Technology Differences.

	LFET1T 45V SPD06	LFET1T 65V T07D17
Epi	4.0µm 0.50Ω ∗ cm	5.3µm 0.85Ω ∗ cm
P-edge Implant	B11, 120keV	B11, 110keV
P-deep Implant	B11, 200keV	B11, 220keV
ISD Poly	6K, As Single wafer	6K, As Single wafer
Source metal	Al (Cu, W) 3.6µm	Al (Cu, W) 3.6µm
Metal passivation	/	SiO_2 0.5µm
Bonding wire	Al 400µm	Al 400µm

Table 3: Bonding parameters.

Bonding force	10 N
Bonding pressure	37 MPa
Bond width	450 µm
Bond length	750 µm
Bond Area	0.265 mm^2 (elliptical)

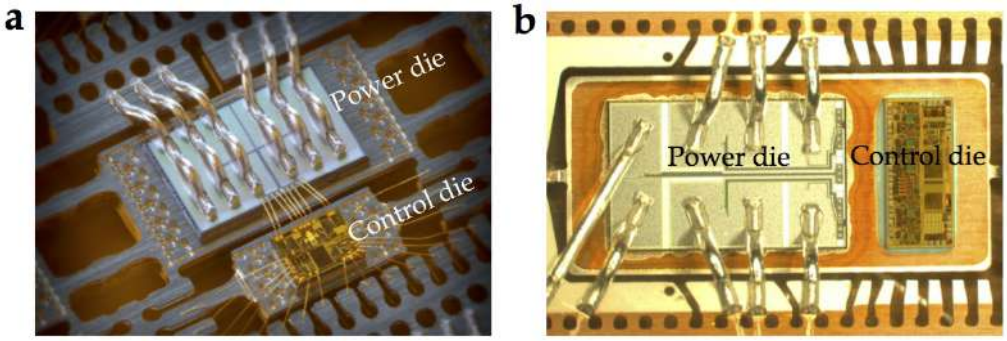

Figure 23: LFET1T smart power MOSFET device from NXP Semiconductors. (a) 45V, 12V SPD06, (b) 65V, 24V T07D17.

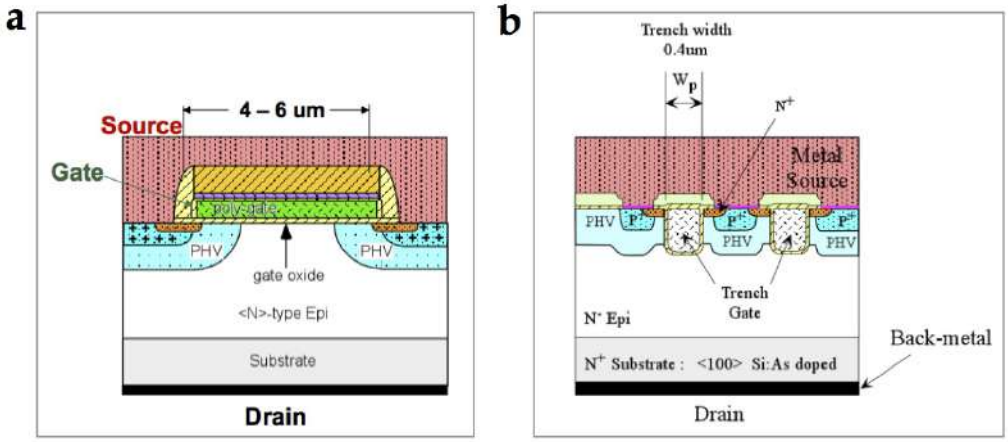

Figure 24: (a) planar vs (b) trench MOSFET structure in NXP power devices.

2.3 RELIABILITY ASSESSMENT OF LFET1T POWER DEVICES: METHODOLOGY AND ACCELERATED AGING TEST DESCRIPTION.

The reliability assessment of power devices is a complex issue that can be address following different approaches. Fig. 25 shows a methodology schema representing the three approaches that are currently adopted to study the robustness of power electronics systems:

1. Experimental testing. The reliability assessment is addressed experimentally by:
   - Accelerating aging test to reproduce the stress at which the device is subject.
   - Localization and identification of the failure.
   - Degradation analysis of the critical points.
2. Degradation mechanisms modelling. The goal is to determine:
   - Accelerating aging factors.
   - Life-time predictive laws.
   - New design strategies.
3. Numerical study, to simulate:
   - The stresses undergone by the device.
   - The correlation between the stresses and the degradation mechanisms.

On the basis of the mission profile, these three methods (or a combination of them) contribute to provide a predictive evaluation of the device life-time and to identify the degradation physical mechanisms.

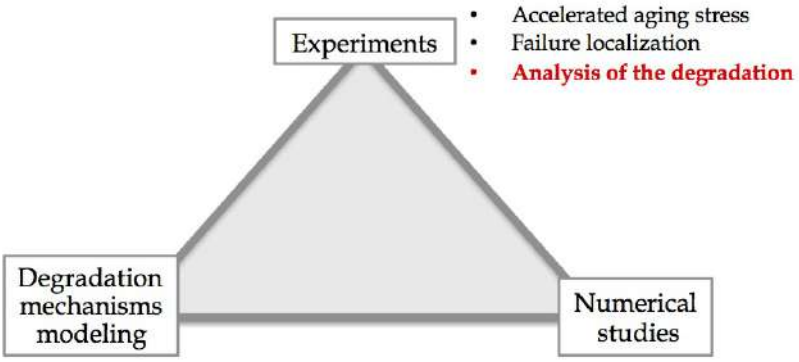

Figure 25: Methodology used to assess the reliability of power devices. In this work we use an experimental approach to assess the degradation of the metallic parts of LFET1T power devices under repetitive accelerated aging conditions.

This work is based on the first approach and tries to give a contribution in the investigation of the degradation mechanisms of the critical points in power devices undergone accelerated electro-thermal aging test. In particular here we focus on the degradation of the metallic parts of of LFET1T power dies. The degradation of the Al source metallization, together with the wire bondings, (section 2.2.2) is assessed following a physical metallurgy approach, described in detail in the next chapter, in order to understand the degradation mechanisms behind the failure of LFET1Ts. The qualification tests used by the microelectronics community, together with the failure localization techniques (SAM, x-rays, OBIRCH, etc.) are nowadays well standardized (AECQ100 standard for the automotive). However, the physical mechanisms at the base of the failure are still difficult to comprehend, because of rapid technology evolution, and of the lack of standard quantification methods. Here we try to offer some paths to quantify the degradation occurring in the source metal through the development of new investigation technologies and systematic measurements of the structure and microstructure of the Al metallization and wires. These dedicated techniques and quantification methods could serve as references for the investigation of other devices.

In this work, the aging tests have been performed in intermittent operating life (IOL) mode, which consists in applying cyclical electrical pulses until the device failure (Fig. 26). This choice is motivated by previous studies [Kho07a]

showing that continuous current tests (steady state operating life mode, SSOL) do not allow to bring the power modules to failure in a reasonable time.

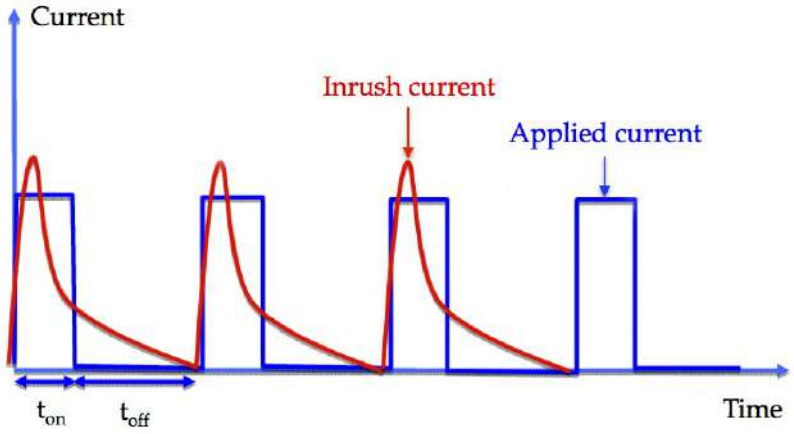

Figure 26: IOL (Intermittent Operating Life) test: the device undergoes electrical pulses during the time interval t_{on}. The test current and t_{on} values are generally limited by the control die, that protects the control die from "bulb inrush" phenomena.

LFET1T devices have undergone two different kinds of IOL accelerated electro-thermal test:

1. Tests at NXP on 65V LFET1T (T07D17).
   They consist in qualification tests, used by the manufacturers to determine the device life-time, in conformity with the AECQ100-12 standard [Kel06]. The objective is to reproduce the power device behaviour in their normal operating mode, regulated by the control die. A repetitive short-circuit (SC) is imposed to the power die. At this point the control die detects a current overflow and turns the power die off. Energy is dissipated at this stage, leading to an increase in the device temperature and affecting the device aging conditions.

2. Tests at Satie laboratory on 45V LFET1T (SPD06).
   These tests are complementary to the previous ones: they have been designed in order to push the devices to their technology limits and monitor the electrical aging indicators during the tests. For these tests, SPD06 devices have been assembled without control die and mold compound, and put under extreme SC conditions in a test bench designed by the Satie laboratory [Ros13]. This original configuration gave us the possibility to bypass the current regulation of the control die and to control the dissipated energy by playing on the duration of the SC pulses (t_{ON}).

During both tests, only one sector undergoes the electrical pulses, the one inside the red rectangle in 45V LFET1Ts (Fig. 27a) and 65V LFET1Ts (Fig. 27b), so we could use the others as reference during the microstructural characterizations.

The test features and conditions are summarized in Table 5 and detailed in the next two sections.

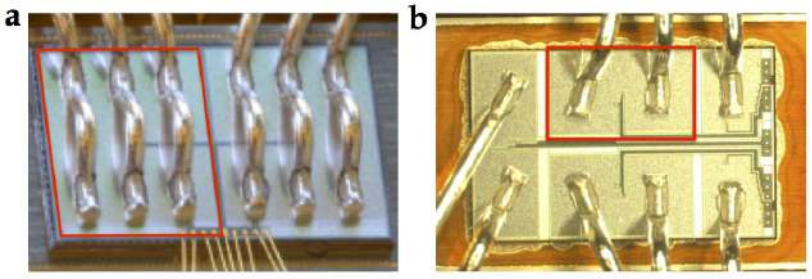

Figure 27: Localization of the MOSFET sector under accelerated aging test (red rectangle) in a (a) LFET1T 45V (SPD06) and (b) LFET1T 65V (T07D17) power device.

Table 4: Accelerated aging test parameters

	Test @ NXP	Test @ SATIE
DUT	T07D17 Normal configuration	SPD06 Without control die and mold compound
Aging test parameters	Current regulated qualification test I_{th} = 120 A f = 2 Hz Vds = 14V L = 5µH R = 10mΩ	SC test without current limitation Ton = 40µ s f = 5 Hz Vds = 30V E = 150 mJ
Test temperature	25 °C 70°C	25°C
Aging indicators monitoring	No Device brought directly to failure without monitoring	Yes Monitoring of the electrical parameter and source metallization evolution during aging
DUT Life-time	5.3 million cycles at 25°C 300k cycles at 70°C	330kcycles

2.3.1 *Test NXP*

2.3.1.1 *Electro-thermal test bench*

Power devices underwent accelerated aging conditions in a dedicated test bench developed by NPX Semiconductors company in 2005 (Fig. 28a). The bench consists in a Climats Sapratin Excal 2223-TE climatic chamber (in red), a power supply unit (in blue), and a control panel (in green), and allows to test 10 devices at the same time at controlled uniform temperature and current conditions.

The temperature in the climatic chamber can be set in the range from $-80°C$ to $180°C$ and its homogeneity inside the chamber has been optimized in a previous thesis work [Kho07a], by placing deflector shields in order to equally distribute the heating flux, and so the thermo-mechanical stress, on each device under test. This allows to age the devices under well-defined thermal conditions.

The 10 printed circuit boards (PCBs), each one containing a power device to test, are placed in a motherboard inside the climatic chamber (Fig. 28b). The 80 V, 200 A motherboard power supply unity integrates an active electrical charge that provides to the system a constant current between 5 and 200 A. In fact, during aging, the increase in R_{dsON} value causes a decrease in the current intensity through the devices under test, and thus the aging conditions change and become less aggressive. The active charge is fundamental to counterbalance this current drop and keep the aging conditions stable during the all test.

A dedicated electronic board in the control panel (in green in Fig. 28a) allows to test one sample at a time. It acts as a switch, turning on the first component for the required duration, while all the others nine are off. Then, the first one is turned off and the second one is activated, and so on, until the complete aging of the 10 power devices. Moreover, a thermocouple (Fig. 28b) is connected to each device package, to follow the global temperature evolution, due to the current flow through the transistors, during aging. This measure, visualized in the display of the control panel, gives useful information about the device behaviour during the test.

2.3.1.2 *Electro-thermal test conditions*

Electrical test circuit and waveforms (according to the AECQ100-12 standard [Kel06]) are depicted respectively in Fig. 29 and Fig. 30. The supply resistance and inductance are fixed at $R = 10m\Omega$ and $L = 5\mu H$, which correspond to an output of $R_{short} = 50m\Omega$ and $L_{short} = 5\mu H$. The current threshold, that is the overload value at which the control die shuts the power die down is set at

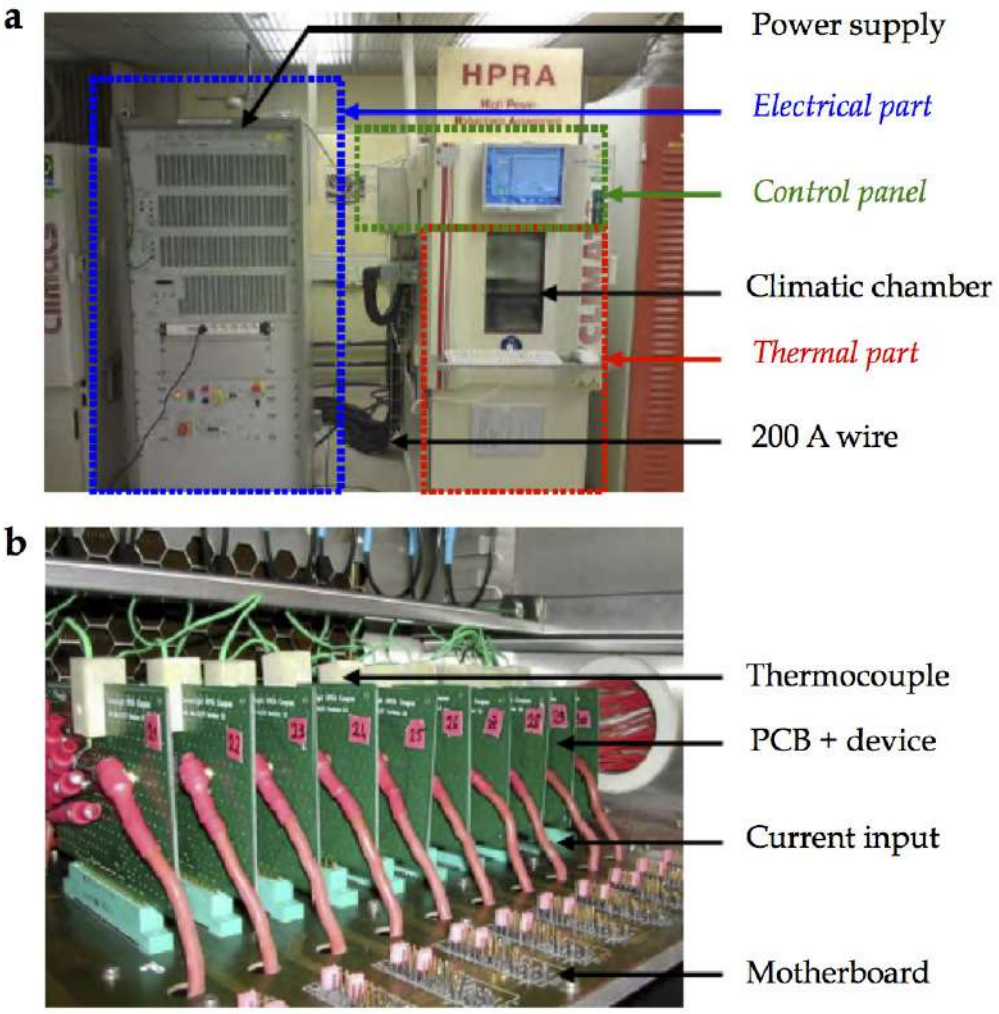

Figure 28: (a) Climats Sapratin Excal 2223-TE test bench at NXP Semiconductros. it consists in an electrical part (in blue), equipped with a 80 V, 200 A power supply and an active charge (5 - 200 A), a climatic chamber (−80°C - 180°C) containing the devices under test (in red), and a control panel (in green) with an electronic board that control the devices switching.
(b) Inner part of the climatic chamber, showing the motherboard and the PCBs containing the power devices to test. The motherboard is in charge of sending the current to the devices and communicates with the control electronic board during the switch stage.

I = 120A. The dissipated energy leads to an increase in the device temperature up to 250 − 300°C. Under these conditions, To7D17 devices have been aged at room temperature and at 70°C, in order to investigate the catalytic role of the temperature in the device failure. In the first case, the components failed at ~ 5.3 million cycles, whereas at higher temperature at ~ 300kcycles.

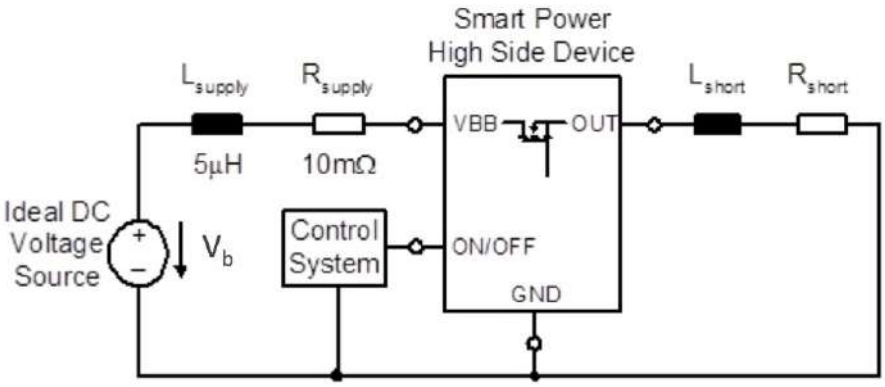

Figure 29: Accelerated aging test circuit.

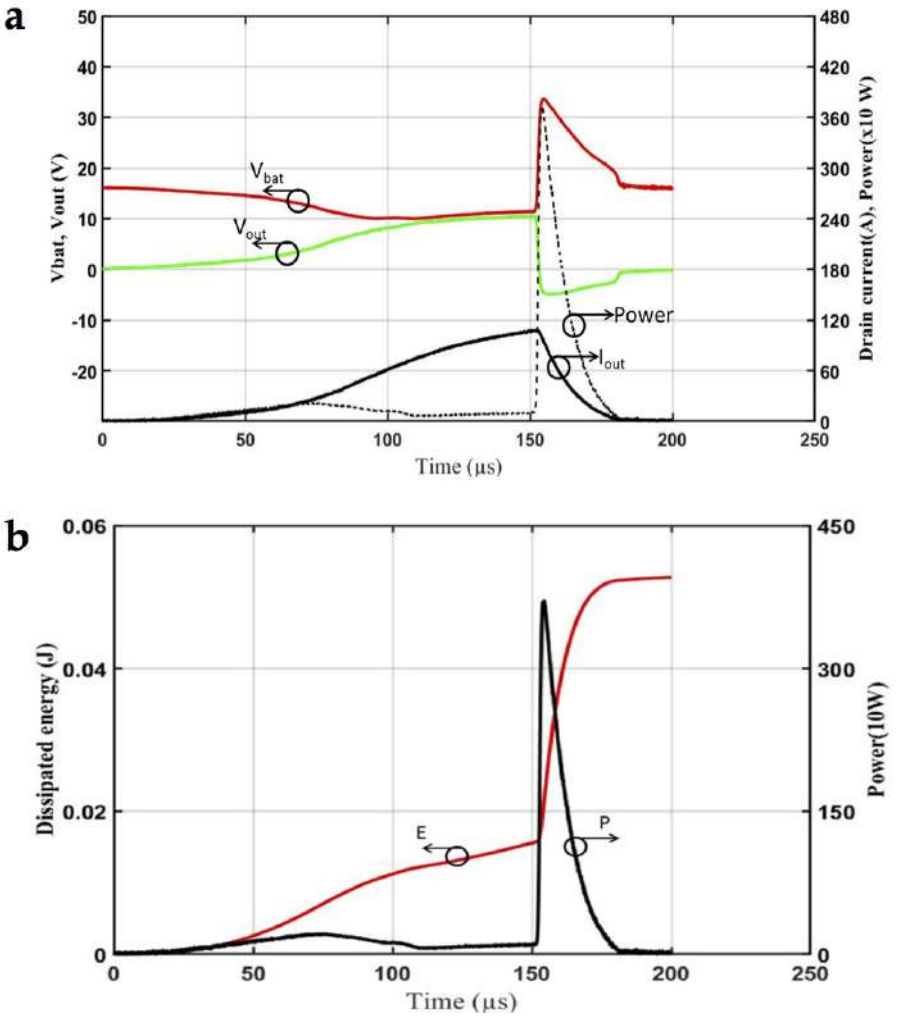

Figure 30: (a) Typical signals during a short cycle event in the power MOSFET by activation of overload protection. (b) Dissipated energy (E) and power (P) during the SC phase.

2.3.2 *Test Satie Laboratory*

2.3.2.1 *Electro-thermal test bench*

This test bench has been designed by the Satie laboratory in Cachan (Paris) in order to perform accelerated electro-thermal aging tests complementary to the industrial qualification tests, with the objective to monitor the aging indicators ($R_{DS(on)}$, V_{th}, etc.) during the test and investigate their correlation with the device life-time. This is done by increasing the power losses, and thus the temperature excursions, in power devices that are deprived of the control die during the test.

The test set-up, controlled by a labVIEW interface, is showed in. Fig. 31a and consists in:

1. Xantrex input power connections (150 V, 8 A).
2. Grouping of capacitors $6 * 1000\mu F$.
3. Climatic chamber head positioned on the device under test. It allow to keep the device under controlled temperature conditions during the test.
4. Driving board, better showed in Fig. 31c, connected to the device under test.
5. Output measurement connections (V_{GS}, V_{DS}, etc.).

As anticipated, the main feature of this set-up consists in the possibility to interrupt the aging test and replace the driving board with a measuring board (showed in Fig. 31b) that allowed us to regularly measure the $R_{DS(on)}$ (from the $I_D = f(V_{DS})$ vs $I_D = f(V_{GS})$ characteristic) without moving the device PCB from the aging set-up.

Three different aging test configuration can be set up in the Satie test bench [Ros13]:

- Normal protection mode (Fig. 32a).
  It simulate the "normal" over-current protection function of the control die. This mode is, then, equivalent to the qualification tests previously described (section 2.3.1). The current is limited by a resistive and inductive load.
- Avalanche switching mode (Fig. 33a).
  Power converter switches off under inductive current load.
- Short-circuit (SC) switching mode (Fig. 34a). It is performed by switching the power die directly on the power source voltage.

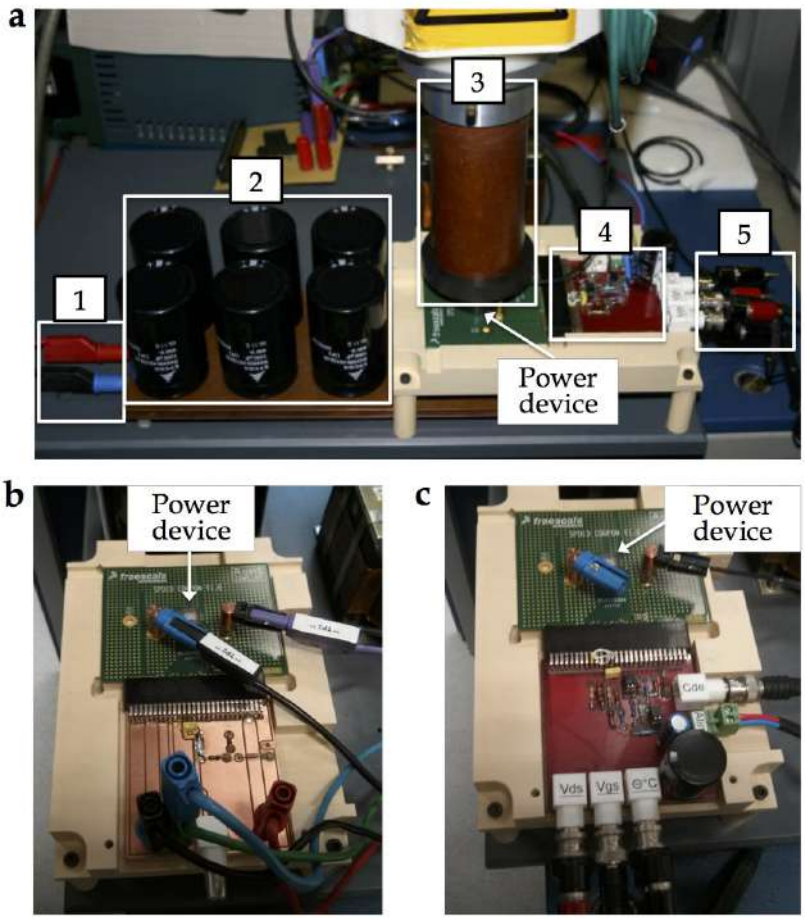

Figure 31: (a) Accelerated aging test bench set up at the Satie laboratory. The device under test can be connected to (b) a measuring board or to (c) the driving board.

In order to compare the life-time of power devices as a function of the different aging modes, Rostaing and colleagues [Ros13] put SPD06 smart power MOSFETs under accelerated aging conditions in these three possible configurations (normal mode, avalanche and SC), keeping the dissipated energy level constant (300-320 mJ) and varying the test duration and supply voltage. The relative test curves are depicted in Fig. 32b, 33b and 34b, respectively for normal mode, avalanche and SC. At equal dissipated energy, they found out that the life-time of the devices that underwent SC conditions was severely decreased compared to the ones under normal and avalanche tests, exhibiting a similar behaviour. Their results are summarized in Fig. 35): for an equal t_{ON} of 50µs, the life-time of the MOSFETs under normal and avalanche mode exceeds 300 kcycles , while under SC is only 55 kcycles.

2.3.2.2 *Electro-thermal test conditions*

On the base of Rostaing et al. results [Ros13] (previous section 2.3.2.1), in this work we have decided to use the test bench in SC mode, in order to put the device under the most extreme and accelerated conditions possible.

The repetitive SC test have been performed at room temperature with a switching frequency set to 5 Hz (1 cycle every 0.2 s) in order to ensure that the temperature of the device returns to ambient temperature after each cycle. Short-circuit phase duration has set to $T_{ON} = 44\mu s$, drain-to-source voltage $V_{DS} = 30V$ and gate-to-source voltage $V_{GS} = 15V$. Note that here T_{ON} (and thus the energy) has been lowered respect to Rostaing et al. tests (they used T_{ON} of 50µs): these allowed us to increase the device life-time (from 55 to 330 kcycles) and monitor the evolution of the device resistance during aging over a longer test duration. Electrical waveforms (current and voltage) are depicted in Fig. 36a, just before failure (300 kcycles) and in Fig. 36b (330 kcycles). During the SC phase, the drain current increases in 10µs until a maximum value of 600 A, that corresponds to a dissipated energy equal to $4J/cm^2$ in the active area during the whole SC phase. This results in an important increase in the power die temperature and in the consequent current decrease. The test has been regularly interrupted at increasing number of cycles (1, 5, 10, 100, 200, 300 kcycles) in order to monitor the electrical parameters of the device and the Al metallization microstructure evolution.

2.3.2.3 *Supplementary characterizations*

During the SC tests, live potential and temperature mapping of the Al source metallization have been performed in order to follow the evolution of these two parameters at increasing number of aging cycles. The thermal mapping is the result of a collaboration with the University of Naples Federico II ultrafast

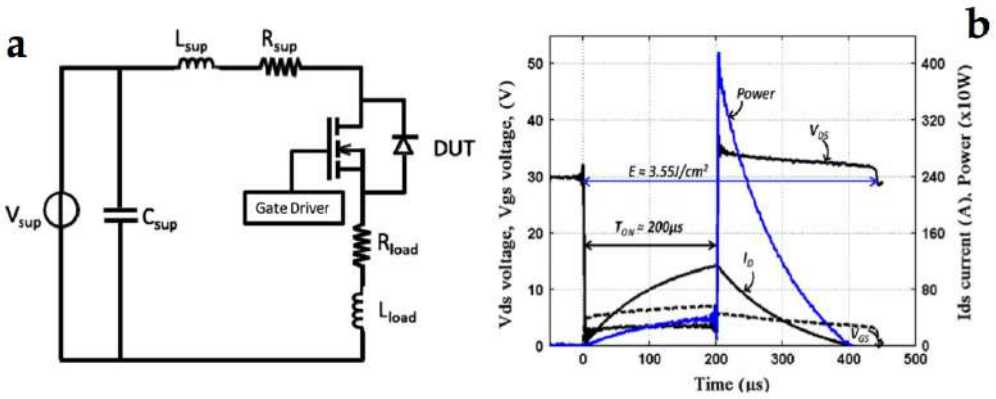

Figure 32: (a) Normal protection mode circuit and (b) waveforms, $V_{SUP} = 30V$, $T_{ON} = 200\mu s$, $T_{AMB} = 25°C$.

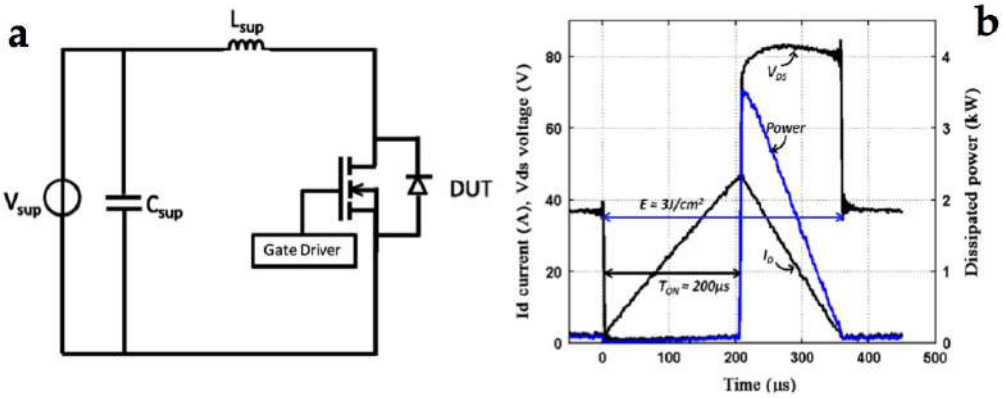

Figure 33: (a) Avalanche switching mode circuit and (b) waveforms, $V_{DSmax} = 84V$, $I_{Dmax} = 50A$, $T_{ON} = 200\mu s$, $E = 300mJ$, $T_{AMB} = 25°C$.

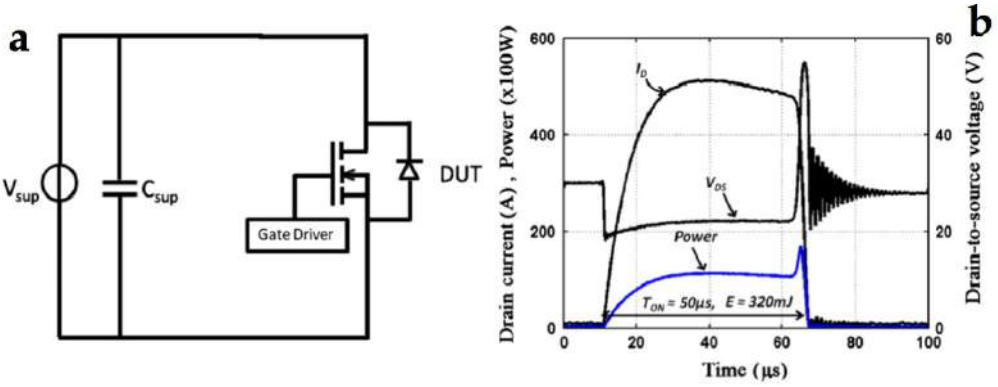

Figure 34: (a) Short-circuit mode circuit and (b) waveforms, $V_{SUP} = 24V$, $T_{SC} = 50\mu s$, $E = 320mJ$.

Mode	Nbr of tested devices	Energy E (J/cm²)	Max Cur. I_{DMAX} (A)	Max Voltage V_{DSMAX} (V)	Average Life time (kcycle)	Standard deviation (kcyle)
Normal	4	3,55	110	34	347	17
Avalanche	5	3	50	84	396	14.4
Short- circuit	3	3,55	580	12	55	15

Figure 35: Rostaing's test protocol [Ros13]. At equal dissipated energy (E), power MOSFETs under normal and avalanche conditions are characterized by a similar life-time (~ 400kcycles), whereas the devices under SC conditions fail much early (~ 50kcycles).

where there is a temperature measurement set-up based on a ultra-fast infrared (IR) camera. The aging test bench (described in section 2.3.2.1) was moved in Naples laboratories in order to reproduce the same aging conditions of the experiments performed in the Satie laboratory.

Potential mapping

The experimental set-up for the source potential measurements is shown in Fig. 37a and consists in a voltage spring probe moved by a three-axes robot (ISEL), connected to a data acquisition device and a PC which controls the overall system and stores the data (current, voltage and 2D position of the voltage sensor). This voltage probe maps the 2D electric potential distribution on the metallization layer along x and y axes (with a 0.1 mm scanning step in the both directions) when the power die is in the conducting state. Fig. 37b shows the probe in contact with the source Al metallization in a SPD06 device during the source potential measurement. During the measurement of the source potential in a device undergoing SC aging pulses, the power die is maintained in the on state ($V_{GS} = 15V$) with a drain current set to 1 A, in order to avoid the device self-heating.

Temperature mapping by IR camera (Naples)

Temperature mapping has been performed in a system developed in 2014 by the Department of Electrical Engineering and Information Technologies of the University of Naples Federico II [Rom14]. Fig. 38 show a schema of the main elements of the measure set-up. The core of the thermal mapping system is the SC7650 IR Camera produced by FLIR Systems. It is equipped with a cooled InSb Focal Plane Array (FPA) of

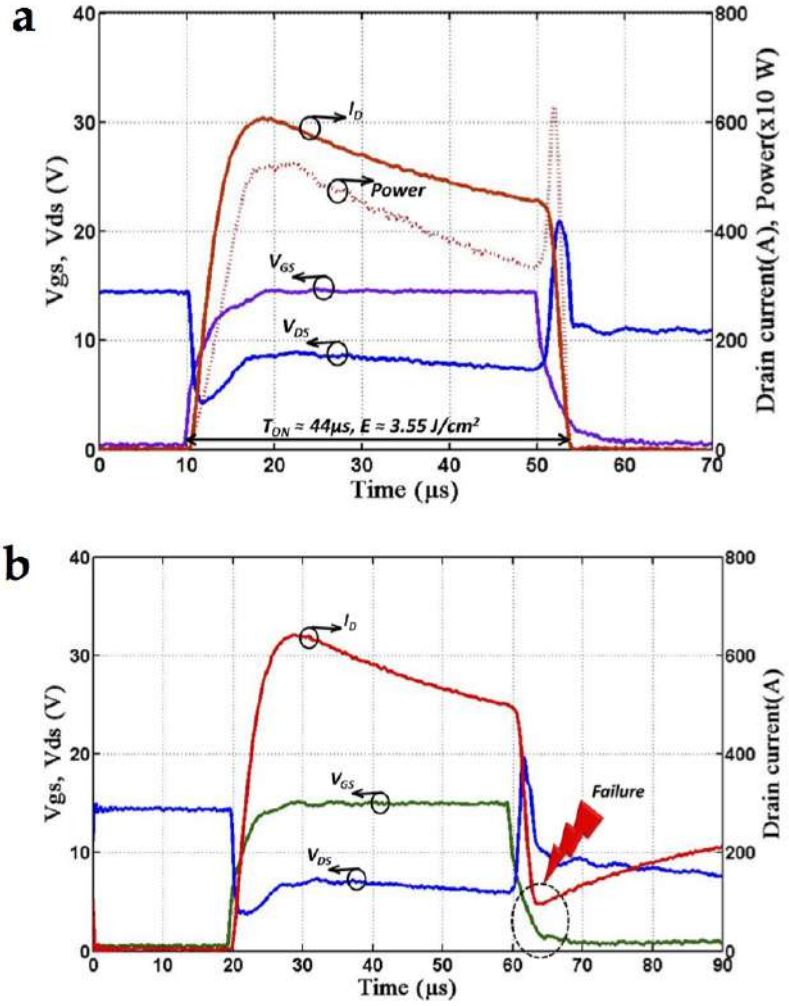

Figure 36: SC characteristics (a) just before failure (after 300 kcycles) and (b) at failure (330 kcycles). $V_{DS} = 15V$, f = 5Hz, $T_{ON} = 40\mu s$.

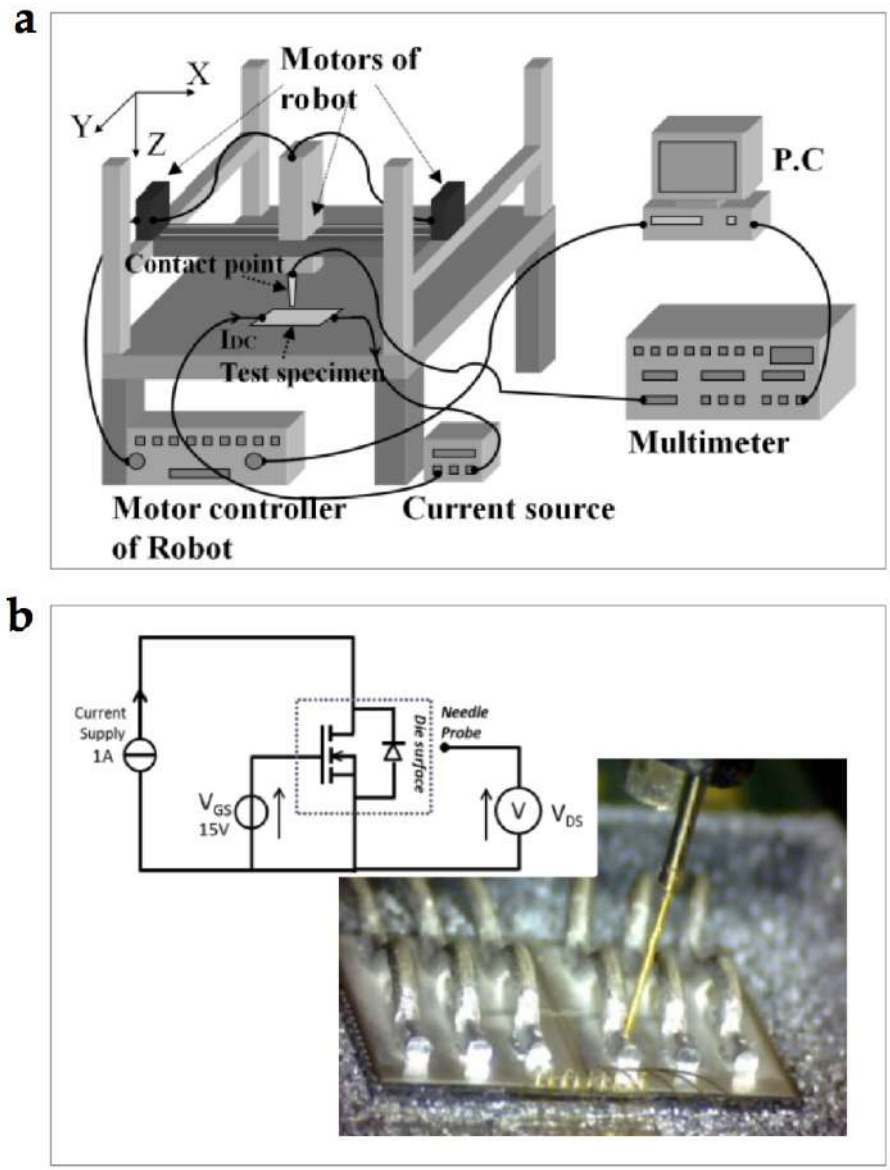

Figure 37: (a) Experimental set-up for source potential mapping of the power die. (b) Spring probe for source potential mapping, $V_{GS} = 15V$, $I_{DS} = 1A$.

640 x 512 pixels. The pixel pitch is 15µm and the maximum real time full-frame acquisition rate is 100 Hz. The spatial resolution depends on the optical magnification and is limited by the diffraction phenomenon to about 2.5µm. The temperature resolution depends on the dynamic input range and the selected integration time of the sensors. To further increase the frame-rate capabilities of the system, a new synchronization network has been realized. It generates timing signals to drive the experiment and trigger the IR camera in equivalent-time acquisition mode, reaching 2.5 MHz equivalent bandwidth. A PC communicates over a Gigabit Ethernet link with the IR camera to send commands and download the stream of IR images into the memory. The synchronization with the digital circuit is implemented on a Cyclon IV FPGA, configurable depending on the experiment and the desired timing. The PC sends all the settings through an USB channel to an MCU board equipped with the ATmega328P microcontroller that ensures the communication with the FPGA. All the instruments are controlled with a MATLAB Graphical User Interface (GUI).

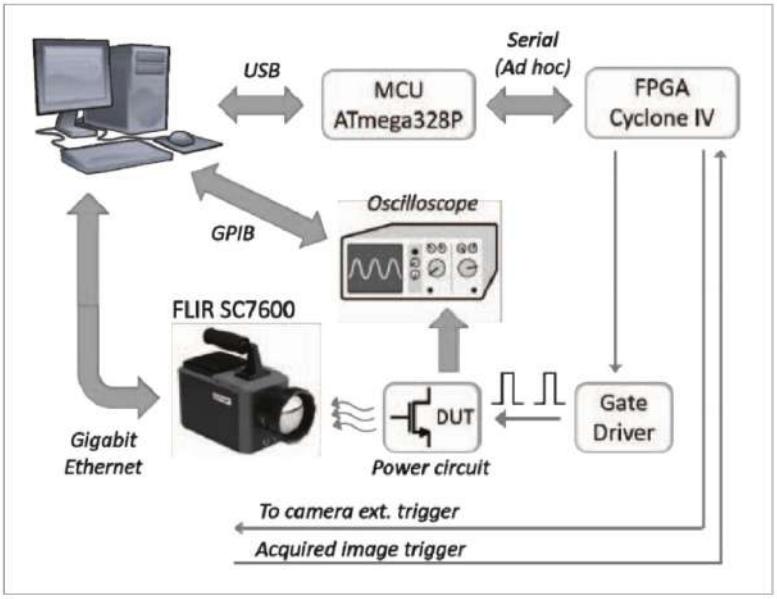

Figure 38: Schema of the IR setup showing the connections between the different parts of the system.

3

MICROSTRUCTURAL CHARACTERIZATION

In the reliability assessment of power modules, the metallic parts, and in particular the Al source metallization and wire bondings, constitute a key link as they are systematically prone to plastic deformation. The main sources of mechanical stress arise from the difference in the CTE between the metal and the oxide/semiconducting parts. As aging progresses, the degradation of the metal may increase its resistance, which in turn increase the temperature of the device in the on-state, therefore augmenting the mechanical stress. This feedback causes a degradation of the top metal through specific processes (see section in chapter 1), occurring at submicron scale. Moreover, the wire bondings, which are cold welded on top of this metallization, complexify significantly the initial device structure, introducing plastic deformation prior to aging in the contact areas.

In order to study these degradation mechanisms, we need to access the inner metallic parts of the devices, which can not be revealed preserving the package integrity, and investigated through fault localization techniques, such as scanning microscopy, X-ray analysis, thermal mapping, optical examination, etc. The complex and fragile power module architecture, involving different kinds of materials assembled at different length scale (from few microns of the MOSFET cells to few centimeters of the entire device), requires to use specific physical metallurgy techniques to observe the microstructure of the metallic parts, preserving at the same time their integrity. These are electron and ion microscopy, together with grain structure mapping techniques. They allowed us to characterize the Al grain structure and follow its degradation during electro-thermal aging in terms of grain size, grain boundaries, dislocations, etc. evolution, to be linked to the evolution of the device mechanical and electrical properties.

This chapter describes the physical metallurgy approach that we used to investigate the Al top metallization and wire bondings degradation of LFET1TB modules upon aging. We will introduce the destructive techniques to image and characterize the metal microstructure before and after aging, at two main locations: away from the bonding contact (we will call this zone "naked metal") and under the bonding wires. For the latter case, we will describe an original preparation, that we have set up in order to preserve the weak bonding contact (especially in the case of aged modules) and analyse the whole wire-metallization interface. These techniques, together with the relative sample

preparation methods, are described following an order that reflects the real needs we encountered during our study, on the basis of the results gradually obtained. First of all, a package decapsulation step is required in order to access the metallic parts of the power devices (Section 3.1). Then, the physical analysis is carried out starting from the surface level (Section 3.2) and, successively, moving deep in the metallization thickness in contact with the MOSFET cells and the Si bulk (Sections 3.3 and 3.4).

A systematic comparison of the metallization surface before and after aging is carried out through Scanning Electron microscopy (Section 3.2.1). Electron Backscattered Diffraction (Section 3.2.2) is used to characterize the initial Al grain structure, but it is not applicable to the aged zones because of the strong surface reconstruction. Thus, cross-sectional cuts are performed by Focused Ion Beam (Section 3.3.1) and Cross Polisher (Section 3.3.2) and the inner Al grain structure is revealed by ion channeling contrast. Finally, these results are compared to a finer cross-sectional analysis by Transmission Electron Microscopy and grain structure mapping (Section 3.4.2) on metallization ultra thin lamella prepared in the focus ion beam (Section 3.4.1).

3.1 PACKAGE DECAPSULATION

Since in their final application the power devices are encapsulated in epoxy molding compounds, a preliminary sample preparation is needed in order to remove the epoxy parts and to disclose the power device on the side of the Al source metallization and the bonding wires (front-side) for their microstructural characterization, as in Fig. 39. This step has been carried out in NXP Analog Mixed-Signal Investigation Laboratory.

Each semiconductor company optimizes its own method for the decapsulation of epoxy-packaged semiconductor devices. Generally laser-based or chemical methods are used [Wen83] [Low08]. We coupled the two techniques, roughly removing a first part of the packaging by IR laser decapsulation system (Fig. 40a) in order to decrease the time of the final step which consists in a chemical attach of the remaining package by a mixture 3:1 of nitric and sulfuric acid in a pressurized jet system (Fig. 40b). Finally, the decapsulated device is rinsed in an ultrasonic bath of cleaning solvents, in order to remove undesired residues from the die surface.

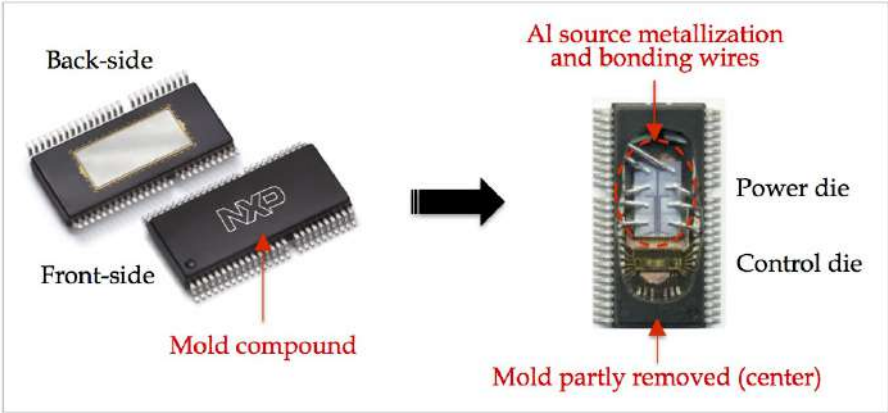

Figure 39: Decapsulation of epoxy-packaged semiconductor devices. Al source metallization and bonding wires are beneath the front epoxy side.

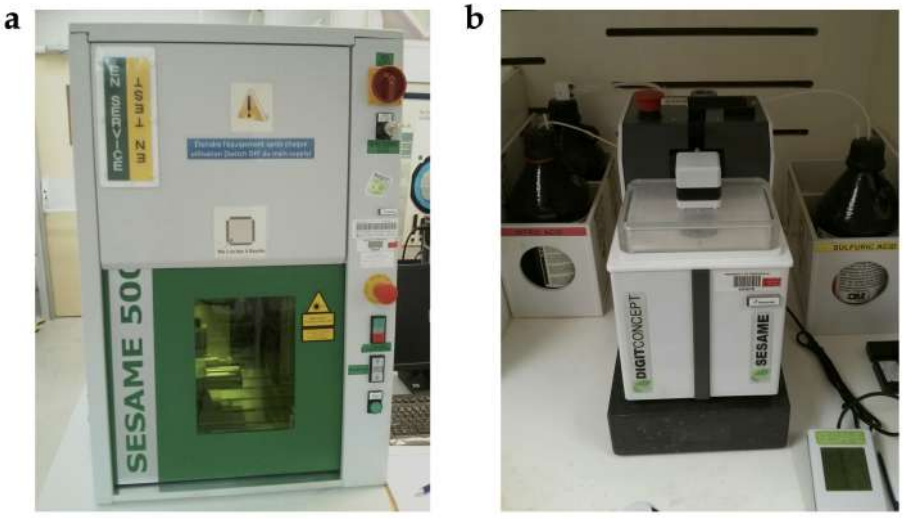

Figure 40: Equipment used for the decapsulation semiconductor devices. (a) IR laser decapsulation system. (b) Pressurized jet system.

3.2 SURFACE ANALYSIS

We performed a preliminary analysis of the top Al metallization surface of power modules in order to follow the evolution of the microstructure during the aging tests. Scanning Electron Microscopy images of the as-processed modules gave us a first idea of the initial granular metal structure, which served as comparison to investigate the high surface reconstruction occurring at failure in the aged modules. In parallel we acquired orientation maps by Electron Back-Scattered diffraction technique. The aim was to follow the evolution of the metallization texture as a result of the plastic deformation during the electro-thermal cycles. Unfortunately, this turned out to be unfeasible because of the heavy degradation of the metal surface together with the diffractions patterns that are collected to build the orientations maps. However the electron back-scattered diffraction analysis gave us useful information about the initial texture of the Al metallization, as well as the grain size and misorientation.

3.2.1 *Scanning Electron Microscopy and Energy Dispersive X-Ray Spectroscopy*

In scanning electron microscopy (SEM), a fine probe of electrons, with energies up to 30 keV, is focused on a specimen and scanned along a pattern of parallel lines. As a result of the interaction of the incident electron beam with the specimen, different signals are generated. These are mainly low-energy secondary electrons (SE), high-energy electrons back-scattered (BSE) from the primary beam, characteristic X-rays, and Auger electrons [Golo3]. The secondary electrons, which provide topographic contrast, are collected to form a grey-scale image of the specimen surface, whereas the x-rays give information about its chemical composition.

For the microstructural inspection of the metallization surface we used a Helios NanoLab 600 DualBeam (FIB/SEM) system (Fig. 41a) from FEI Company (Acht, Eindhoven, The Netherlands). Fig. 41b represents the schematic configuration of the main components of the microscope (described below), used during our characterizations.

1. The microscope is equipped with a high resolution Elstar electron column with a Field Emission Gun (FEG) electron source. The electron beam theoretical resolution is less than 1 nm at 15 kV and less than 2.5 nm at 1 kV.

2. The FIB gun is a liquid Gallium ion (Ga^+) source which allowed us to both image and mill the sample surface. The typical dual-beam column configuration is a vertical electron column with a tilted ion column. In

this case, the sample will be tilted to 52°for milling normal to the sample surface (see Section 3.3.1).

3. Several detectors for the emitted signals are installed in the sample chamber. The majority of SEM images presented in this thesis was collected by using an Everhart-Thornley (ETD) detector for SE signal. The detector consists mainly of a scintillator, surrounded by a Faraday cage, which specifically attracts the SE and converts them in photons. Then, the electrical signal is conducted to a photomultiplier outside the SEM and amplified to form a 2D topographic image of the device surface at different magnifications, as in Fig. 42a and Fig. 42b.

4. The Helios is also equipped with a X-MaxN Silicon (Lithium) Drift Detector (SDD) from Oxford, installed in 2016, for the Energy Dispersive X-Ray Spectroscopy (EDS), used for the chemical characterization of the sample surface. The detector collects the x-rays emitted from the interaction of the primary electron beam with the specimen. Since the x-ray energy is characteristic of the element from which it was emitted, thanks to a dedicated software (AZtecHKL from Oxford Instruments) we can determine the elemental composition of the scanned source metallization (Fig. 42c), with a sub 10 nm spatial resolution.

5. An EBSD (Electron Backsattered Diffraction) detector is installed. The details about this technique, the detector features and the sample-detector configuration are provided in the next section (3.2.2).

6. A multiple gas injection system (GIS) is installed for material deposition (Platinum, Tungsten, Carbon, etc.) in conjunction with either electron or ion beam pattern definition.

7. The Omniproble module consists in a micro manipulator, which allowed us to extract a TEM sample in situ (see Section 3.4.1).

3.2.2 *Electron Backscattered Diffraction*

The Electron Backscattered Diffraction (EBSD) in a SEM is a widely used technique for the characterization of the local microstructure, as well as the distribution of crystallographic orientations (texture) and the structure analysis (phase identification), of poly-crystalline materials at length scale ranging from tens of nanometers to millimeters. The EBSD operates by placing a flat, usually polished bulk sample in a highly tilted configuration (typically 70°), in order to maximize the backscattering efficiency (Fig. 43a). The crystallographic information is provided by the diffraction Kikuchi patterns (also called Kikuchi

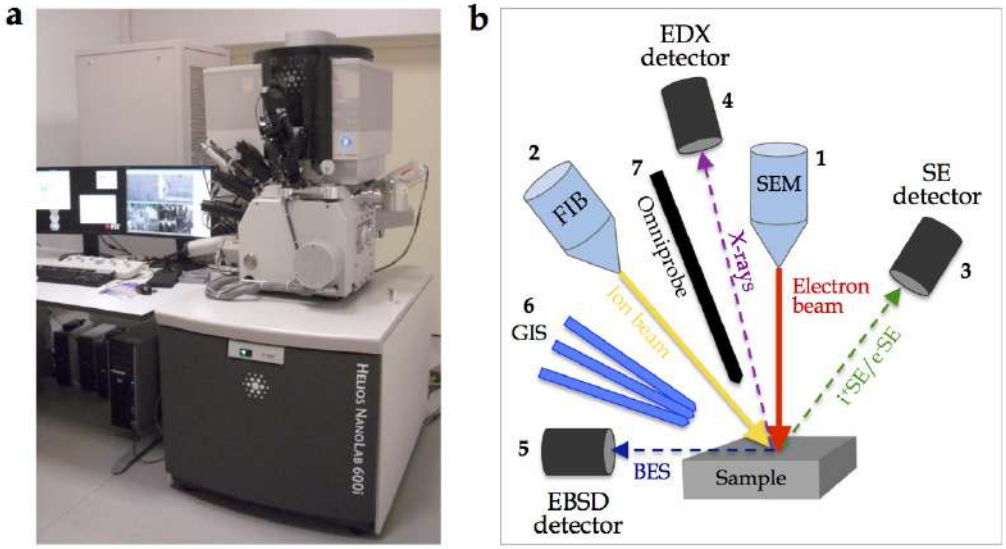

Figure 41: (a) FEI Helios dual beam microscope. (b) Schema of the main components of the microscope.

lines or Kikuchi bands) produced by low energy loss backscattered electrons arising from the interaction of the primary beam with the crystal lattice at the Bragg angle (Fig. 43c), according to the Bragg law:

$$2d_{hkl} \sin \theta_B = n\lambda_e \tag{5}$$

Where d_{hkl} is the inter-planar spacing for a family of planes, θ_B is the Bragg angle, n is an integer value giving the order of reflection (n=1 for EBSD), and λ_e is the electron wavelength. As these diffractions result in two cones (Kikuchi or Kossel cones) of electron radiation generated from a single set of lattice planes hkl, each pair of Kikuchi lines represents the projections in a phosphor screen, placed at short distance to the sample, of the geometry of a single plane in the crystal.

Hence, an automated SEM-based EBSD system consists in three main parts: the SEM, the pattern detector and the software for the indexing procedure. (Fig. 43b) shows the set-up of our experiments: we used the dual beam FEI Helios microscope, in SEM mode (acc. V = 20 kV, I = 11 nA), equipped with a 70°pre-tilted sample holder. The sample is placed at a working-distance of about 10-12 mm from the SEM pole piece. The EBSD signal is collected by a NordlysNano detector from Oxford Instruments. It consists in a CCD camera with four forescatter detectors mounted to the top and bottom of a phosphor screen, giving both orientation and phase contrast of the sample. The detector has motorized insertion and retraction, and can be placed as close as possible

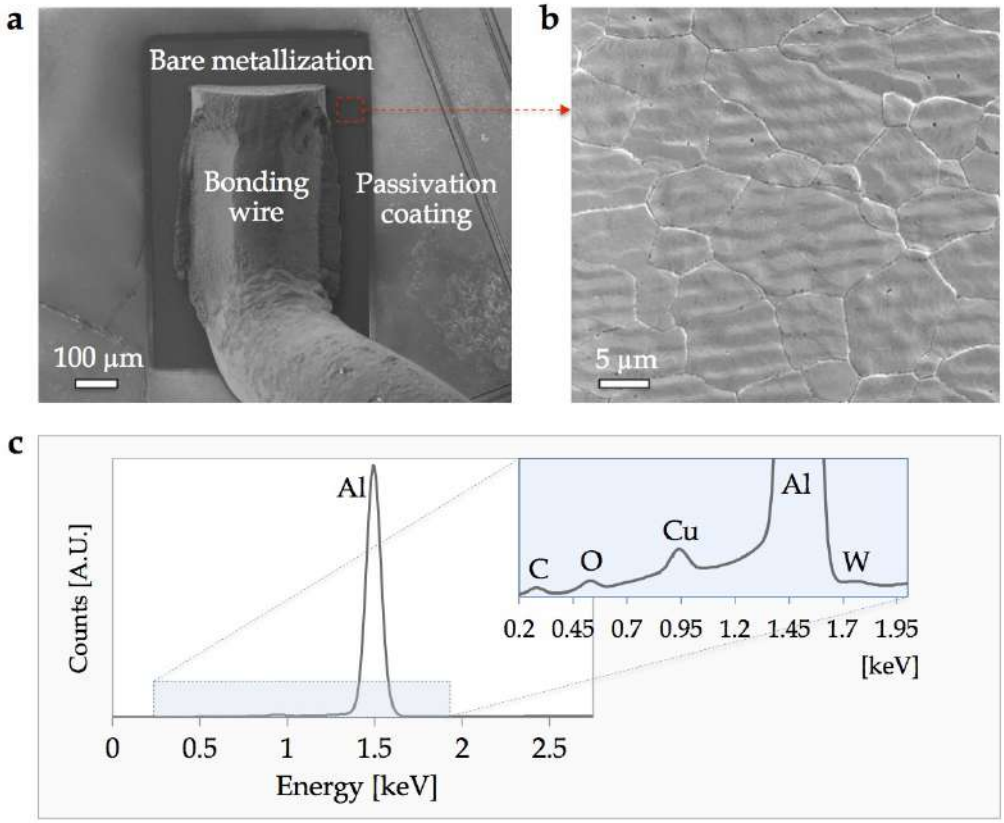

Figure 42: (a) SEM image of an Al bond wire welded on the Al source metallization. (b) At higher magnification, bare metallization of a reference module. (c) EDX spectrum from the Al metallization.

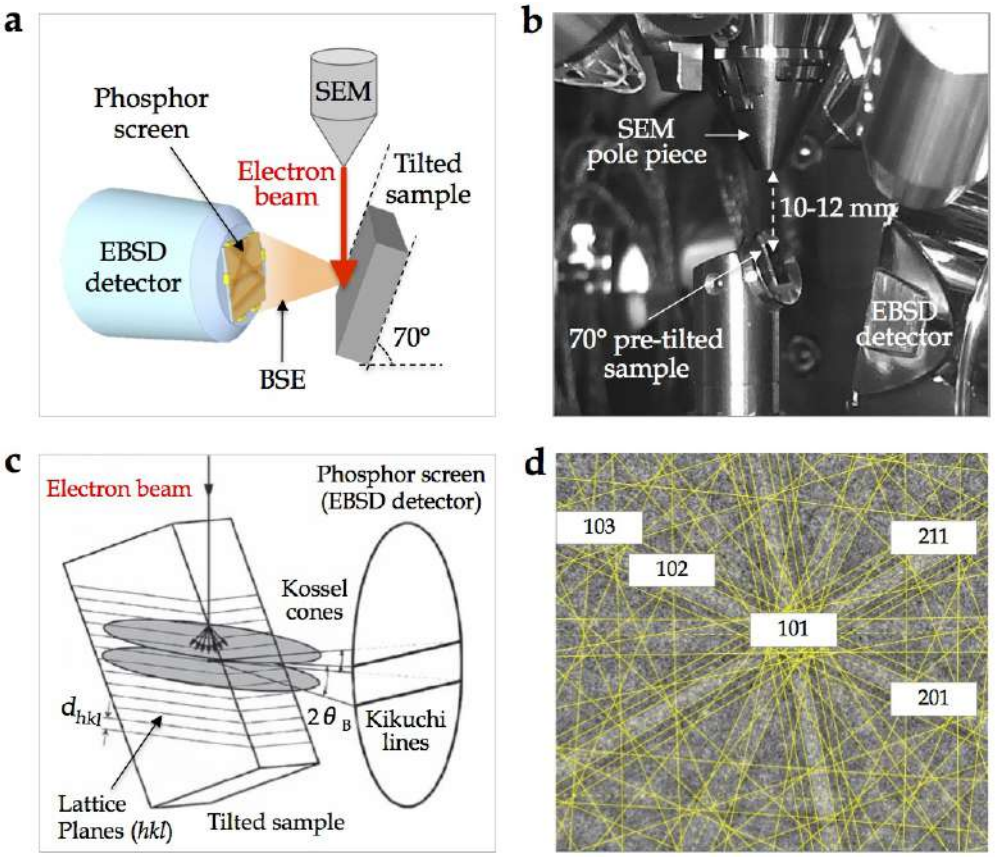

Figure 43: (a) SEM-based EBSD schema and (b) Helios microscope chamber configuration during an EBSD experiment. (c) Kikuchi lines formation schema. (d) Pattern recognition by AZtecHKL

to the sample to maximize the intensity of the acquired diffracted signal. Finally, the camera communicates with the AZtecHKL acquisition software from Oxford Instruments. During the acquisition, the software matches the information from each point of the scanned source metallization with a database of simulated orientations and returns the orientation of each grain (Fig. 43c).

Thanks to a post-processing software (HKL Channel5, Oxford instruments) dedicated to the off-line manipulation and analysis of the EBSD data, we could build orientation maps along the three axis x, y, z. We could also determine the misorientation and grain size distributions of the scanned areas. The sizes are obtained by either grain reconstruction method, approximating each grain to a circle and measuring the equivalent diameter (Fig. 44), or by lineal intercept method [Hum01]. In the former approach, a prior decision about which misorientation constitutes a grain boundary must be taken (15°is often used).

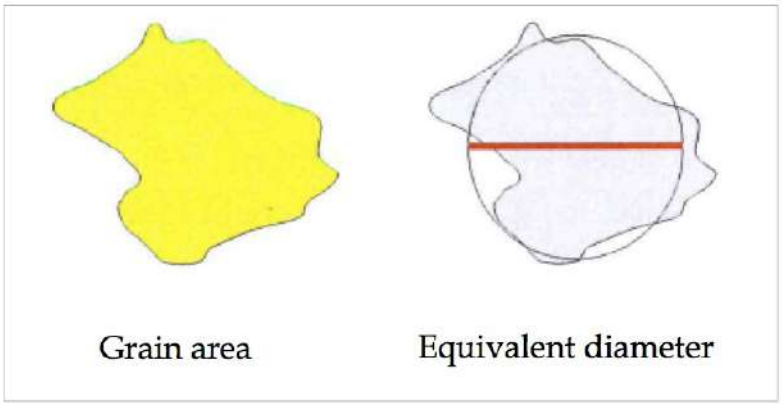

Figure 44: Approximation of a single real grain to a circle shape one for the measurement of a equivalent diameter.

3.3 BULK CROSS-SECTIONAL ANALYSIS

Since it was not possible to follow the evolution during aging of the metallization texture at surface level by EBSD, we decided to move deep insight the material, performing cross-sectional cuts perpendicular to the surface. These cross-sections were then observed using electron and ion channeling contrast. We will further see that ion channeling contrast is strictly related to the grain orientation [Ish97] [Lan15]. Therefore, we used this kind of images to observe the evolution of the grain size and use this information as an indication of the mechanism at play during the aging of the device. For instance, grain growth is commonly observed during thermal annealing while grain reduction could serve as an indicator of severe plastic deformation.

The cross-sectional analysis of the Al metallization before and after aging has been performed at two different locations:

- Under the bonding wire, with particular interest in the wire-metal interface. As discussed before, this zone is critical for the reliability assessment because it is initially deformed during the bonding process.
- Away from the bonding area (naked metallization). At this location the initial metallization is in a non-deformed state and so we could compare it to the metallization beneath the wire.

Two different instruments, based on ion beam milling, have been used to perform the cross-sectional cuts:

- Focused Ion Beam.
- Ion Cross-Polisher.

Both approaches, described below, require a dedicated preliminary sample preparation, in order to access the wire-metal interface for the final milling.

3.3.1 *Focused ion beam milling and microscopy*

For these experiments we used the FEI Helios microscope (Fig. 41a) in its dual-beam functionality, which combines a scanning electron beam produced by a field emission gun (previously used for the surface analysis), with a focused ion beam of gallium ions. Since the electron and ion columns are 52°tilted with respect to each other, the sample is placed at the eucentric position, that is the position where the ion and the electron beam converge with an angle of 52°, as in Fig. 45a and Fig. 45b.

Depending on the geometrical configuration of the sample in the microscope chamber, and on the ion beam energy, the FIB works both as a milling beam and as a probe for a scanning ion microscope (SIM).

- When the microscope stage is tilted at 52°, the sample is perpendicular to the FIB source. In this configuration, the high-energy ion beam is used to cut perpendicular to the sample surface, while the relative images are acquired by the electron column to constantly monitor the preparation progress. More details will be given in the next paragraphs.
- Tilting the stage back to 0°and working at more gentle ion beam currents (to prevent excessive atom sputtering from the sample surface and its consequent amorphisation), we could inspect the prepared cross-sections by ion channeling contrast.

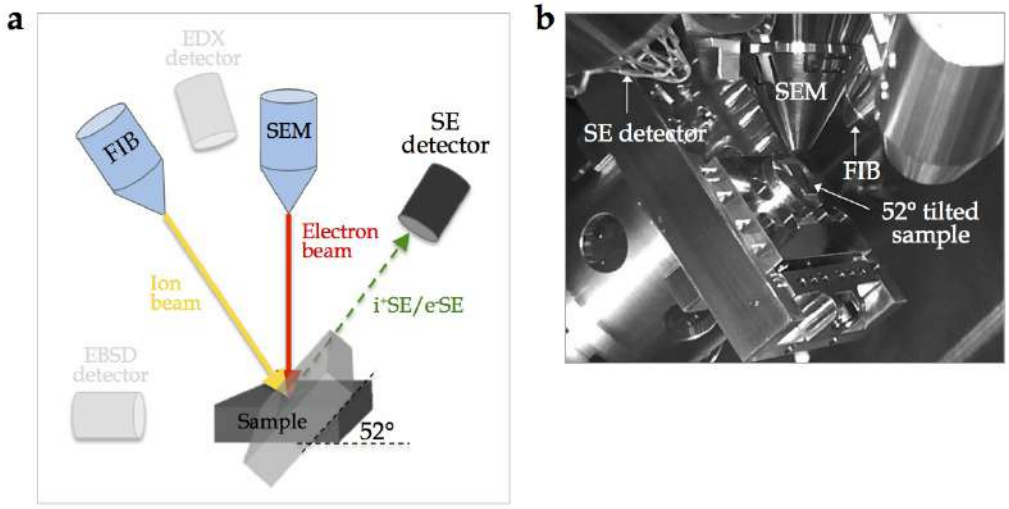

Figure 45: (a) Schematic representation of the dual beam FIB/SEM operational mode. (b) Helios microscope chamber configuration during the cross-section experiments.

Ion channeling behavior is a well-known phenomenon where the ion-solid interactions change drastically with crystal orientation, affecting the sputter yield of the emitted secondary electrons (i^+SE) and imaging contrast [Kem01]. Generally, darker grains sputter more slowly than brighter grains [Gia11]. The dark grains are consistent with ion trajectories parallel (or nearly parallel) to low index crystallography planes where ions will travel long distances prior to losing energy and interacting with the target (Fig. 46a). Since most of the ion-solid interactions occur deeper in the sample, the sputter yield is lower and the gray-scale signal is darker. On the other side, grains, which are oriented greater than the critical angle to the ion trajectory (Fig. 46b), will cause the ions to interact closer to the surface, losing energy more quickly and yielding a brighter signal. Therefore, ion channeling contrast images give us visual information about the grain orientation and, as previously mentioned, they are useful to access the deformation of the Al metallization during aging.

3.3.1.1 *Naked metal cross-section*

To prepare the imaging cross-sectional face of the naked metallization, a rectangular patterned region measuring ~ 1000 μm^2 is milled (Fig. 47a). Essentially, the ion beam (with an energy of 30 KeV) scans the surface and when ions collided with the atoms of the material they are ejected away, until a $50 * 20 \mu m$ face had been milled and all the bulk in the path of the ion beam removed. This has been done in two steps:

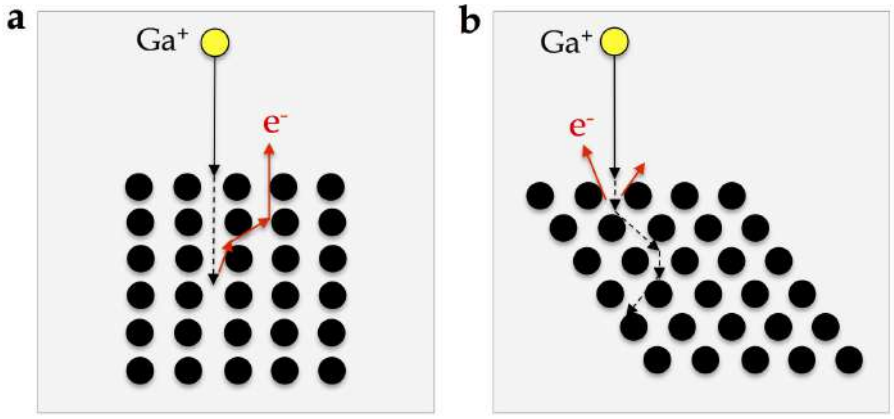

Figure 46: Secondary electrons emission by ion-solid interaction for two different oriented crystals. The ion channeling contrast is darker in (a), where the ion trajectories are parallel to crystallographic planes, whereas is brighter in (b), where the angle between the ion direction and the crystallographic planes increases.

1. A rough cut of the rectangular patterned region at high ion beam current (65 nA) to remove most of the bulk material in the minor time as possible.

2. A finer polishing of the imaging face at decreasing ion beam currents (9.3 nA and 2.5 nA) to get rid of the curtaining and redeposition artefacts of the previous cut.

In parallel, the cross-section preparation progress is monitored by SEM. Fig. 47b shows a SEM image of the final milled area. At higher magnification (Fig. 47c), we can distinguish the layered structure of the power module, including the top source metallization, the MOSFET area and the Si bulk.

The ion beam is used in conjunction with a gas injection system to deposit a thick layer (~ 1 µm) of Platinum (Pt) or Tungsten (W) on the top surface of the sample, above the region of interest. This system releases a precursor gas close to the sample. When the gallium ions interact with the sample, in the presence of this gas, decomposition takes place, causing Pt/W solid to be deposited on the surface of the sample where the ion beam is directed. This additional deposition of a platinum layer (visible in Fig.47c) immediately above the region of interest reduced FIB milling artifacts, particularly prominent in the case of aged module, where the surface roughness is higher. Without it, non-uniform milling can lead to excessive streaking or vertical stripes down to the milled face, known as curtaining effect. Fig. 48 shows the comparison between an ion contrast image of a cross-section prepared without protective coating layer (a) and of another one with 1 µm thick Pt layer deposited prior to milling (b). In

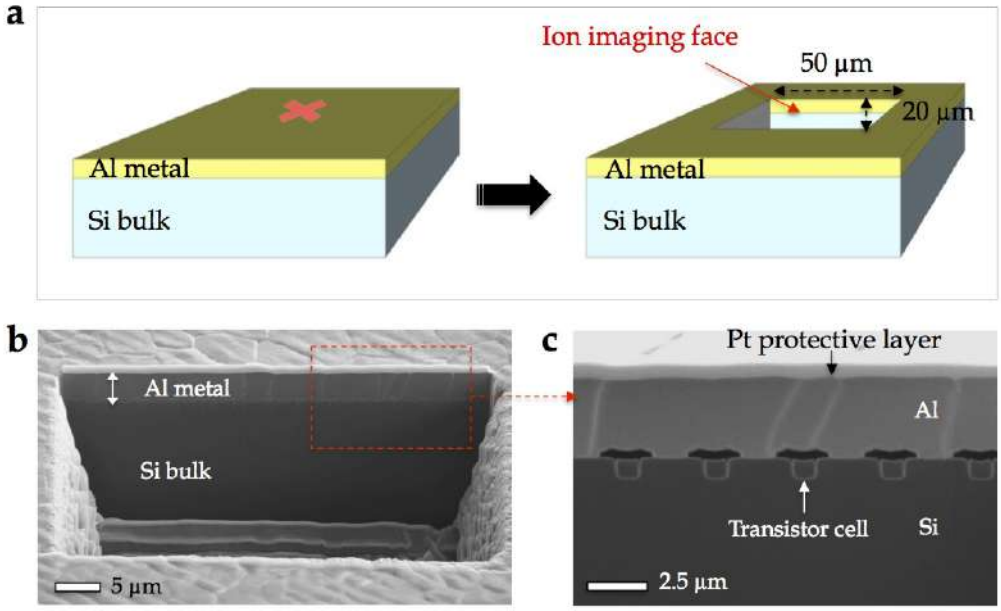

Figure 47: (a) Schematic representation of FIB cross-section from a region of interest (red cross) of the power die naked metallization. (b) SEM image of a FIB cut from a reference module and (c) relative higher magnification of the Al metallization bamboo structure, with the MOSFET area, on the Si substrate.

the former image, the surface roughness affects the imaging face, whereas in the latter one the Pt protective layer leads to a perfectly polished imaging face.

3.3.1.2 *Wire-metallization interface preliminary preparation*

Because aged devices are fragile due to their damaged interface, cross-mechanical polishing may alter the wire-metallization interface or simply remove it. A classical option adopted by other teams is to embed the whole device in epoxy to hold parts, even poorly attached like partial wire-lift-off, together. This approach has been used by Pedersen and co-workers for example to inspect optically the wire bonds of an IGBT [Ped14]. It is however detrimental to SEM and FIB observations because the charged beam is prone to deflections (and then image distortions) when scanning over a strong insulator.

A cross-sectional polishing by ion beam seems to be the best approach to inspect the metallization under the bonding wire, preserving their fragile interface. However, it is practically unfeasible to cut through the entire wire thickness by a FIB ion beam, because it would take too long and redeposition would prevent the observation of large unaffected zones. For this reason, FIB cross-sectional observation of the Al power metallization under the bonding wire requires a specific preliminary sample preparation of the device.

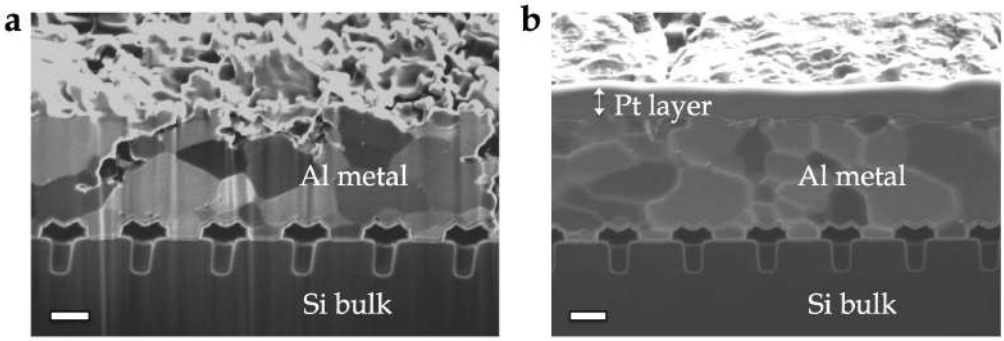

Figure 48: Cross-sectional SEM images of the Al metallization in an aged modules (a) without and (b) with Pt protective layer. Scale bar 1 µm.

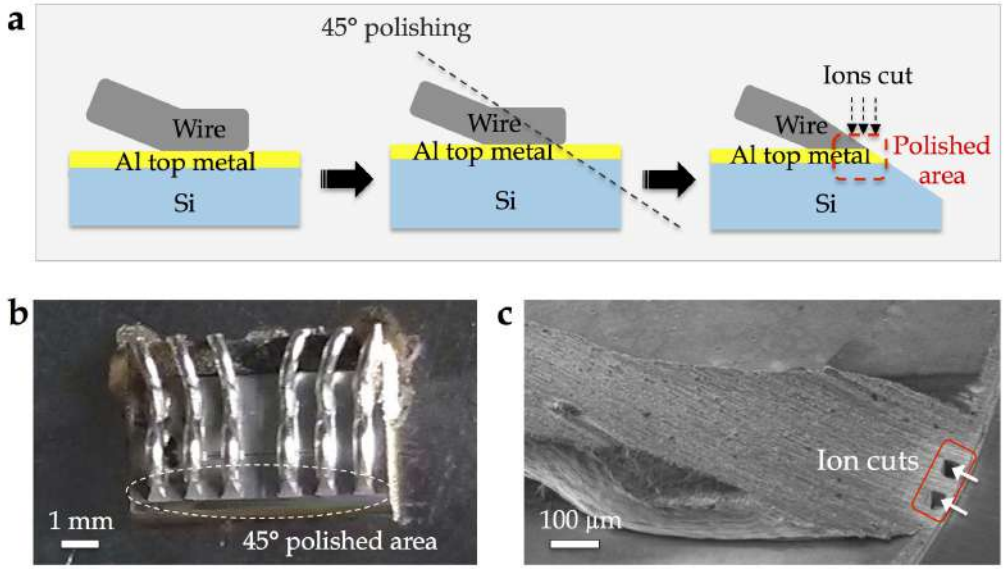

Figure 49: (a) Schematic representation of the preliminary sample preparation for the wire-metal interface FIB inspection. The wire is cut and polished at 45° before being cut by FIB for interface observation. (b) Front-view photograph of a power die prepared for the FIB and (c) relative lateral-view SEM image of a 45°polished wire. The white arrows indicate the imaging direction of the FIB-prepared cross-sectional faces (in red).

The original preparation procedure that we have set up for this study combines a mechanical grinding of the bonding wires at 45°, in order to locally reduce the wires thickness, and a final ion polishing by FIB at various locations (Fig. 49a). In particular, we used a precision diamond wire saw (Fig. 50a) to take the power die out (and get rid of the remaining resin and the control die), and then a polishing machine (Fig. 50b) with silicon carbide papers at decreasing roughness for the manual polishing of the wire-metallization interface at 45°. Fig. 49b and Fig. 49c show respectively a front-view photograph of a power die prepared for FIB milling and the correspondent higher magnification SEM image (lateral-view) of a 45°polished wire-metal interface. The white arrows in Fig. 49c indicate the imaging direction of the FIB sections (inside the red area). Thanks to this preparation we have been able to inspect the metallization both under the bonding wire and in naked locations at the same time. If we embedded the device in resin we would have lost most of the naked metallization parts that are essential to compare them to the metallization beneath the wire.

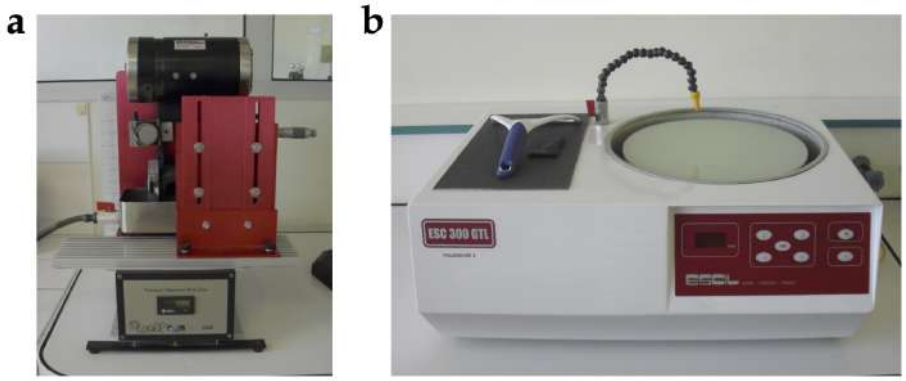

Figure 50: Sample preparation equipment: (a) diamond wire saw and (b) polishing lapping machine.

3.3.1.3 *Metal under the bonding wire cross-section*

Once the wires thickness is locally reduced, the wire-metal interface is ready for the FIB milling. Fig. 51a shows the preparation schema of the polished face for the ion imaging. Since the wire-metal interface is too wide (~ 400 µm) to be entirely milled (because the ion beam would take too long and the redeposition would prevent the observation of the area of interest), several smaller rectangular patterned region ~ 1500 µm² are milled all along the interface (Fig. 51b and Fig. 51c). We followed the same preparation procedure previously explained for the naked metallization:

1. Deposition of a Pt (or W) protective layer to prevent the curtaining artifact on the imaging face.
2. Rough cutting of the rectangular patterned region at high ion beam current (65 nA) to remove most of the bulk material in the minor time as possible.
3. Finer polishing of the imaging face at decreasing ion beam currents (9.3 nA and 2.5 nA) to get rid of the curtaining and redeposition artefacts of the previous cut.

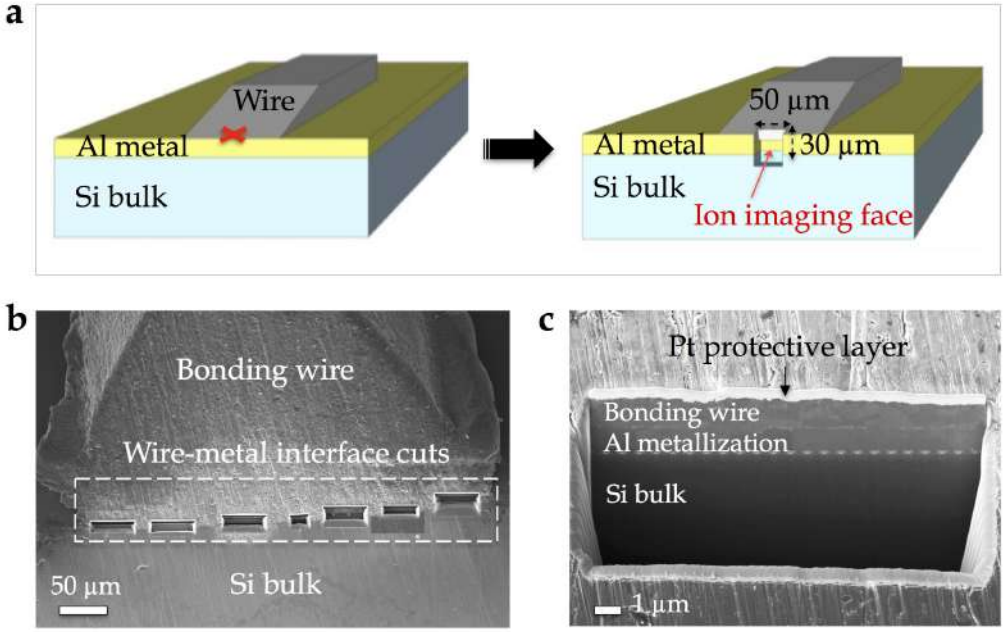

Figure 51: (a) Schematic representation of FIB cross-section from a region of interest (red cross) of the power die wire-metal interface. (b) SEM image of FIB cuts along the wire-metal interface and (c) higher magnification of a single cut, showing the layered structure: Al bonding wire, Al top metallizaiton, MOSFET area and Si substrate.

At this location, the deposition of a Pt (or W) protective layer (step 1) and the final polishing (step 3) are even more critical because the face to be polished, which includes also a piece of the bonding wire, is higher. Fig. 52 shows a ion image of the Al metallization under the bonding wire, where we can notice the presence of Cu-W precipitates detected also at the naked metal surface by EDX.

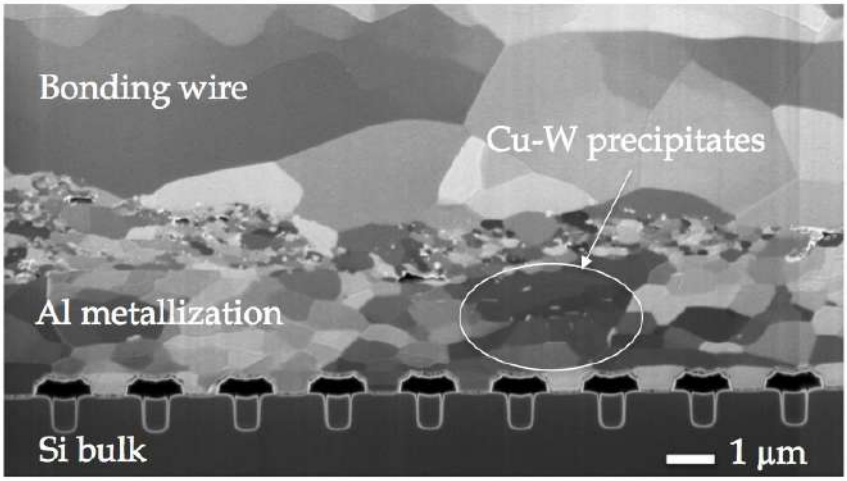

Figure 52: SIM image of the wire-metallization interface. In the Al metallization some Cu-W precipitates are visible in white contrast.

3.3.2 *Cross-polisher milling and ion imaging*

In order to increase the observation area without damaging the sample, an alternative to the FIB cross-sectional preparation could be an ion milling by cross-polisher system. In particular, we used a Cross Section Polisher IB-09010CP from JEOL USA (Fig. 53a). The cross polisher (CP) operating principle is based on a broad argon ion (Ar^+) beam with selectable acceleration voltage range of 2 to 6 kV. The beam irradiates the region of interest and creates a mirrored face for the FIB/SEM inspection, by placing a masking plate across the selected area (Fig. 53b).

Use of the broad argon ion beam eliminates the problems associated with the conventional mechanical polishing and, at the same time, allows for larger high quality cross-sectional areas to be prepared with precision compared to FIB methods. A single cut is typically up to 1 mm wide and several hundreds of microns deep. This means that we could polish the whole wire-metal interface ($\sim$ 400 µm wide) and have a global vision of the metallization under the bonding wire.

However, in order to obtain a highly polished face, this method needs the sample surface to be perfectly flat and parallel to the CP shield. This is not the case of our devices, where the bonding wires on top of the Al metal don't allow a perfect sample-shield contact, which is mandatory to prevent the curtaining artifacts during polishing. For this reason, a preliminary sample preparation prior to cross-polishing is needed, in order to make the device surface flat and the area of interest (wire-metal interface) perpendicular to the CP ion beam.

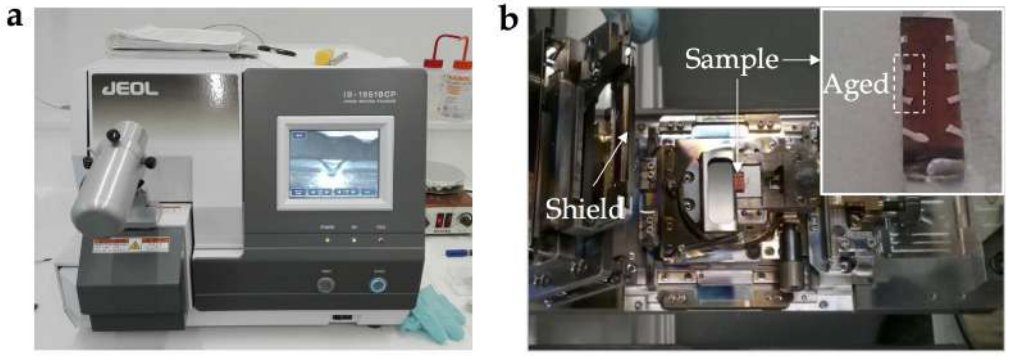

Figure 53: (a) Cross Section Polisher IB-09010CP from JEOL USA. (b) CP inner chamber: the shielding plate is in its lifted position to allow the sample (also visible at higher magnification in the upper-right insert) to be positioned.

3.3.2.1 *Preliminary sample preparation*

Fig. 54 shows a schema of the whole CP procedure, from the preliminary preparation of the power die for the cross polisher (steps 1-7) to the investigation by FIB/SEM of the polished face (step 8).

1. The power die is first covered by G-1 epoxy (Gatan Inc.) to form a solid block by an over-night curing at ~ 80°C. In order to prevent excessive charging effects and image distortion during the electron/ion microscopy, we added to the epoxy mixture few drops of conductive carbon paint (Agar Scientific).
2. The block is then mechanically polished (by diamond papers at decreasing roughness) parallel to the device bulk, in order to create a flat surface still including the bonding wire part in contact with the device top metal.
3. A 90°mechanical polishing is needed to prepare a rough polished face of the wire-metal interface.
4. Now the device is perfectly flat, with the top surface parallel to the bulk, and the perpendicular face ready for the CP milling.
5. Inside the CP, a shielding plate is superposed on the block surface. Only few tens of micrometers (generally ~ 50 µm) exceed the mask to be milled by the Ar^+ beam.
6. The ion beam (6 kV) hits perpendicular to the sample surface and makes a cross section perpendicular to the surface.
7. At the end of the process we obtain a clean mirrored face ~ 1mm wide and deep (Fig. 55a).

8. Finally, the sample can be transfer in the dual-beam microscope for the electron/ion contrast imaging (Fig. 55b and Fig. 55c).

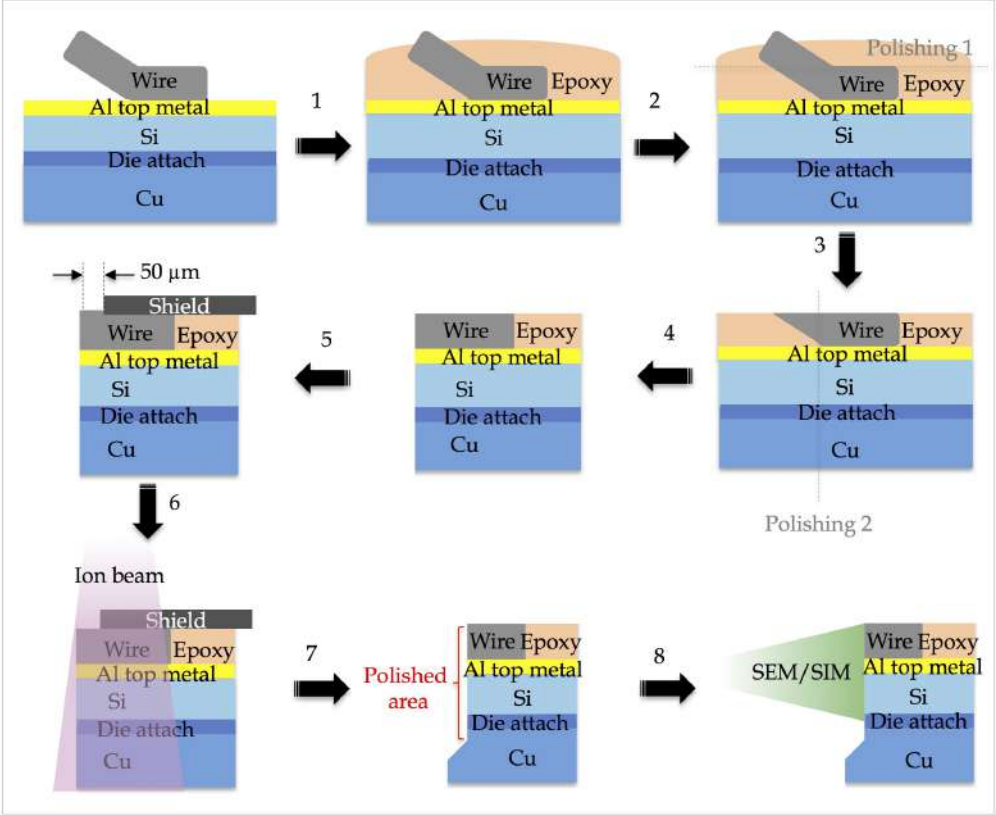

Figure 54: Schema of the sample preparation prior to CP cross-section.

3.3.2.2 *SEM, SIM and EDX analysis*

Once we have mechanically polished the device-epoxy block from both sides (insert in Fig. 53b), according to the preparation previously explained, the sample presents eight wire-metal interfaces that can be finer polished by CP. Two of them, in the aged module, underwent the repetitive electro-thermal cycles and can be investigated by SEM and SIM in comparison to the corresponding non-aged ones.

For the acquisition of ion contrast images of the metallization under the bonding wire we used the MAPS Automation software (FEI). MAPS allows to automatically acquire high resolution images over the large wire-metal interface area (Fig. 56), by setting the horizontal field of view (HFW) of each tile (green rectangles).

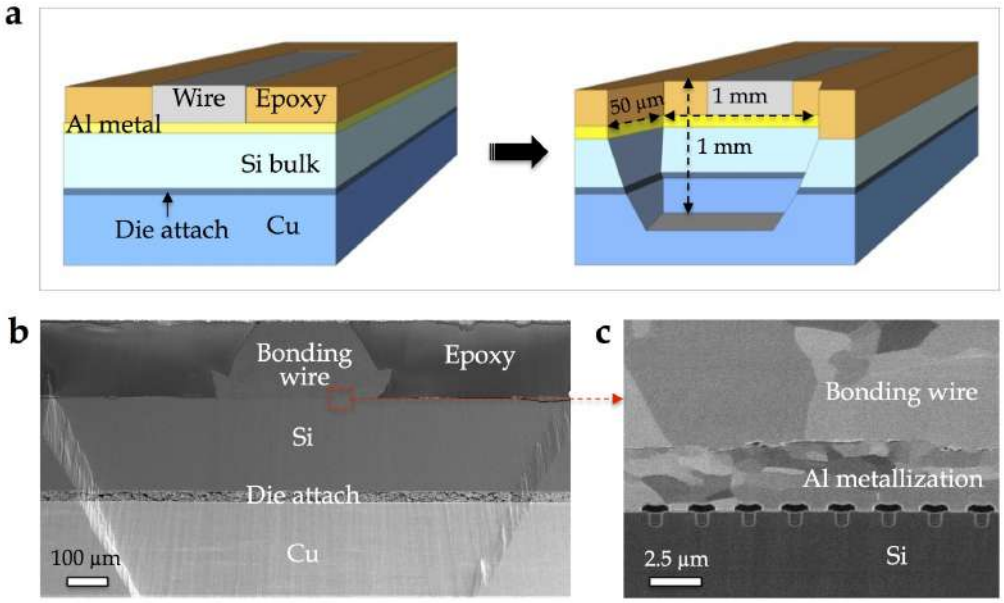

Figure 55: (a) Representation of the solid epoxy-device block (only one wire is represented for sake of simplicity) before and after CP sectioning. (b) SEM low-magnification image of the polished face, showing the layered structure: Al bonding wire, Al top metal, Si substrate, die attach and Cu radiator. (c) In the SIM higher magnification image also the MOSFET area is visible.

In the case of abruptly failed modules, where a severe crack propagation affects not only the Al parts but also the Si bulk, the EDX analysis in the FIB/SEM microscope turned out to be a useful technique to study the diffusion phenomena of the two materials along the fatigue cracks. The polished face is place at 90°to the SEM beam, in order to maximize the x-rays counts to the EDX detector, for the elemental mapping of the regions of interest.

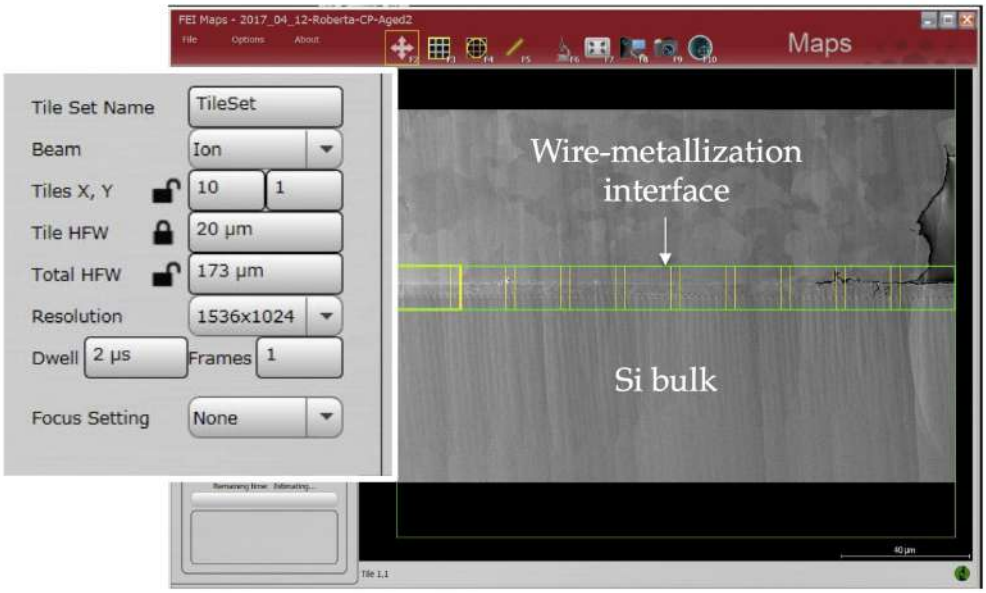

Figure 56: MAPS program interface. The wire-metal interface is split in consecutive tiles (green rectangles) of user-defined size, superposed of few microns. Each tile corresponds to a high resolution SIM image.

3.3.3 *Focused ion beam tomography*

The ion channeling contrast imaging of the power die cross-sectional cuts provides useful information about the microstructure of the metallic parts before and after aging. However, this is a punctual 2D information limited to a precise location of a significantly bigger area. Focused ion beam tomography, that is the acquisition of high-resolution 3D images by performing an in-situ milling, allows us to follow the evolution of the metal critical points in a user-defined volume.

We use the FEI Helios FIB/SEM, equipped with the Auto Slice and View software (FEI), which completely automates the tomography process. The sample is placed at the eucentric position, where the ion and the electron beam converge with an angle of 52°. While the ion beam is used to mill and polish

serial thin sections (slices), the relative images stack is acquired by the electron column (Fig. 57a and Fig. 57b).

Fig. 57c shows the Auto Slice and View software interface relative to the preparation or the region of interest (ROI) prior to the serial sectioning. It consists in the following steps:

1. Deposition of a Pt (or W) protective layer (~ 0.5 µm thick) on the top surface of the ROI, which is typically 20 µm wide and 10 µm deep (yellow rectangular pattern).

   As already explained, this step is fundamental to avoid curtaining artifacts during imaging.

2. Preparation of the parallelepiped to section.

   This step consists in roughly milling by ion beam (30 kV, 9.3 nA) three trenches (blue and magenta patterns), ahead and on either side of the region of interest previously defined, by ion beam.

   - The front trench (in magenta) needs to disclose and polish the imaging face. It must be wide at least as the milling area and deep enough to disclose the entire imaging face.
   - The lateral ones (in blue) need to prevent redeposition on the imaging face. Milling trenches to the same depth (or even more) as the ROI depth and 5-10 µm wide provides sufficient space for sputtered material to deposit innocuously during the serial milling.

   The preliminary trenching is crucial for the success of the FIB tomography. Fig. 58a shows an example of bad preparation of the ROI, compared to a good one (Fig. 58b). We can clearly understand that the trenches size setting is fundamental in order to avoid the redeposition that, especially during the final steps of the milling, becomes an obstacle to the imaging of the polished face. In this case the lateral trenches were not deep enough and the front trench not wide enough.

3. Creation of a reference mark close to the area of interest (red cross in Fig. 57c), for the automated drift correction.

The sample is then ready for the serial sectioning and acquisition of the SEM images stack. We set the thickness of each slice (z-spacing) to 50 nm and so the result is a sequence of 200 SEM images representing the 10 µm deep volume (Fig. 57d). The current of the ion beam used for the serial milling (2.5 nA) is lower than the one used for the preliminary rough trenching (9.3 nA), in order to provide perfectly polished imaging faces. We collected SEM images stacks from the metallization both away and under the bonding wire. They

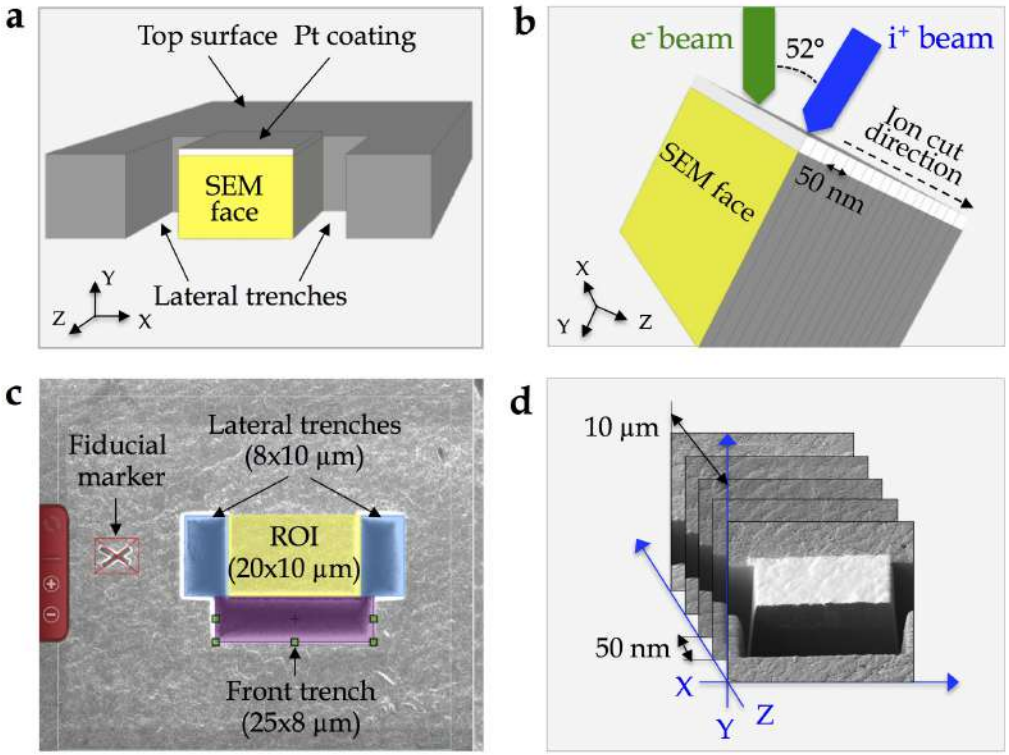

Figure 57: Schematic illustration of the serial sectioning procedure by dual-beam FIB: (a) front view and (b) lateral view of the 52°tilted sample inside the FIB chamber. (c) Slice and View FEI software interface for the preliminary trenching preparation. (d) Stack of SEM images with a z-spacing of 50 nm, through 10 µm (200 images in total).

allow us to investigate the crack propagation inside the metallization volume of the aged modules. We could also perform statistical analysis at the wire-metal interface, to access the proportion of weak interface vs perfectly Al-Al contact area.

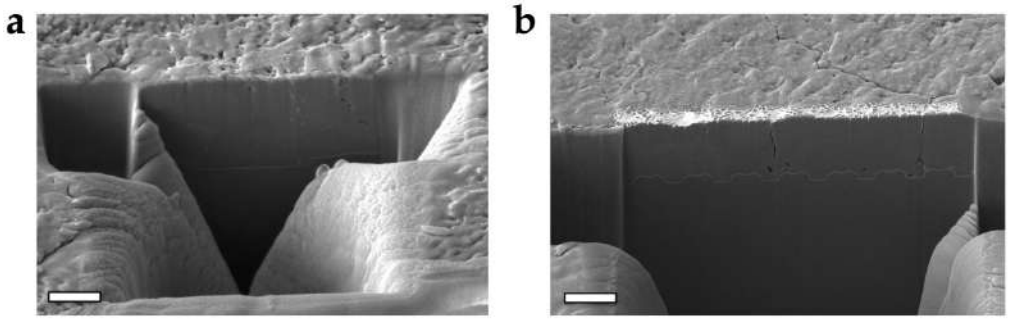

Figure 58: Comparison between two SEM imaging faces during the last steps of the serial milling. (a) The redeposition hides part of the face to be inspected because of a bad preliminary trenching. (b) The imaging face is redeposition-free thanks to an adequate trench size setting. Scale bar 2 µm.

3.4 FINER CROSS-SECTIONAL ANALYSIS

The SIM images gave us direct information about the grain size and orientation. However this in only a qualitative measure, based on the image gray-level. It is not possible to know the real misorientation between grains and, consequently, the real grain size. In fact, we are not able to distinguish between grains and subgrains (grains with a misorientation smaller than 15°).

Different approaches can be adopted to complement the results obtained by FIB cross-sectional analysis. We chose to prepare thin lamella by FIB of the Al metallization (Fig. 59a) and wire-metallization interface (Fig. 59b) to be investigated by transmission electron microscopy.

Transmission electron microscopy (TEM) is an imaging technique in which an electron beam is transmitted through an ultra-thin specimen and focused onto an imaging system to form a grey-scale image with nanometric resolution. Fig. 60a and Fig. 60b show two of the transmission electron microscopes installed in the CEMES laboratory, used for our analysis: they are respectively a Jeol 2010 HC and a Philips CM20 FEG, both operating at 200 kV and equipped with several sample holders (e.g. heating in-situ holder, single and dual-axis rotation holder, etc.).

Fig. 60c represents a typical TEM column inner structure. The emission source (electron gun) consists in a thermionic lanthanum hexaboride (LaB_6) tip in the Jeol 2010, and a field emission tungsten (W) filament in the Philips

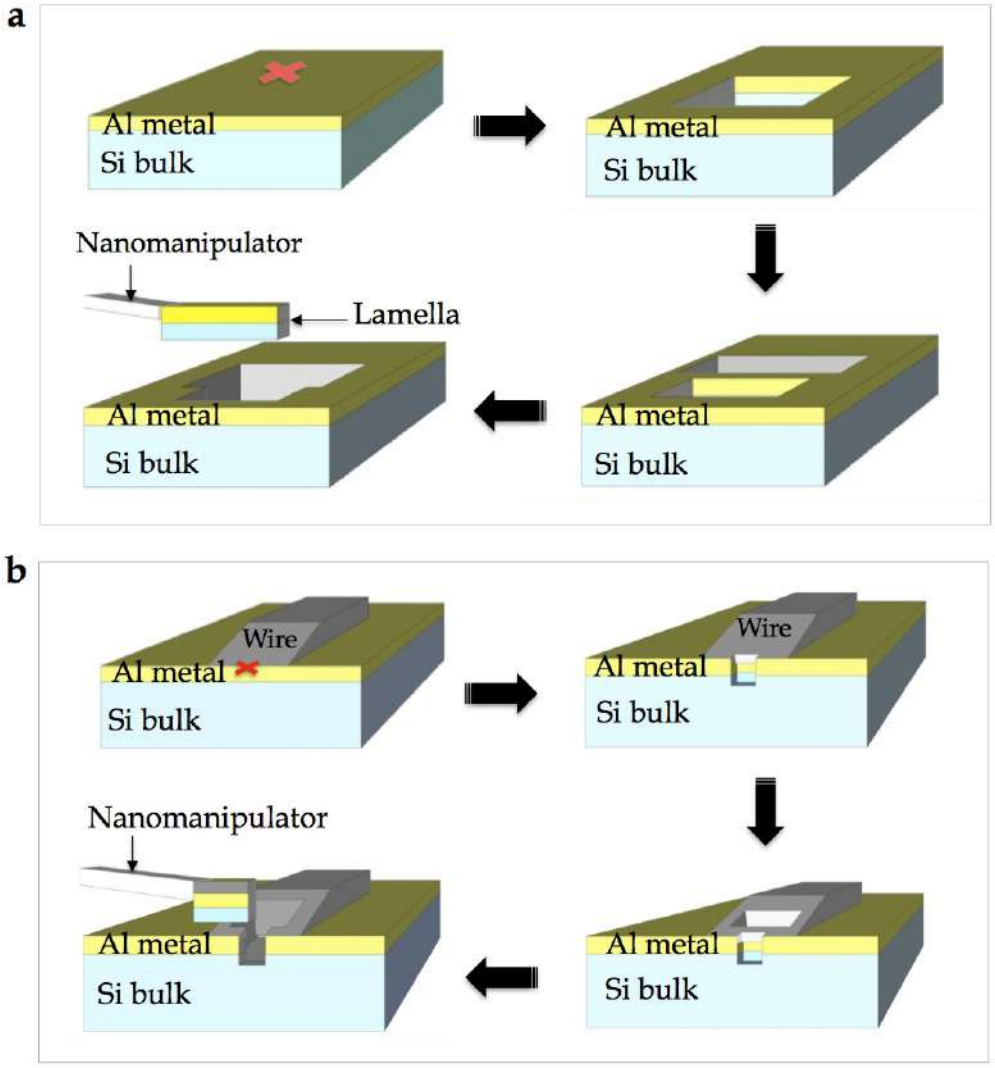

Figure 59: Schematic representation of FIB lamella preparation of the metallization (a) away and (under) the bonding wire.

CM20 FEG. The emitted electrons are accelerated by a high potential difference (200 kV) to form a convergent electron beam that is focused onto the sample through an electromagnetic lenses system. The sample holder is positioned just above the objective aperture, which forms a first (intermediate) image of the sample. The TEM image contrast is due to the absorption of electrons in the material, which depends on its thickness and composition. Under the sample, other lenses (projector and intermediate) highly magnifie the final image that is projected on the imaging system (typically a fluorescent screen or a CCD camera).

The described operational mode (known as conventional TEM mode) gave us structural information of the power device critical points, thanks to high-magnification images formed by an electron beam going through the sample and transmitted on the imaging system. It is also possible to work in diffraction mode (Fig. 60d), by using a selective area diffraction aperture (SAED) and collecting the transmitted electron signal. The obtained diffraction patterns gave us information about the orientation of the crystalline parts crossed by the electron beam.

However, the main drawback of this technique is related to the characteristics of the sample. In fact, it has to fit the TEM sample holder size (3 mm of radius) and to be thin enough to the electron transparency (typically 100 nm). Therefore, our power modules cannot be directly inserted in the TEM as they are: they need a dedicated sample preparation of the metallic parts in order to satisfy the size requirements.

3.4.1 *TEM lamella preparation by FIB*

3.4.1.1 *Why we used the FIB*

The choice of the most appropriate sample preparation technique is crucial in order to have reliable and reproducible results for the transmission electron microscopy analysis of the Al metallization and its interface with the bonding contacts. In particular, as already explained, we have to take into account that our devices present big bonding wires welded on the top metallization and a fragile wire-metallization interface, especially in the case of aged modules. A classical mechanical polishing by tripod would require getting rid of the bonding wires and would increase the risk of loosing the fragile Al-Al contact, in the case of wire-metallization interface analysis.

The main advantages of using the FIB for TEM sample preparation are:

- No other technique can select the target area as precisely as FIB. Lamella can be prepared with a spatial accuracy of tens of nanometers.

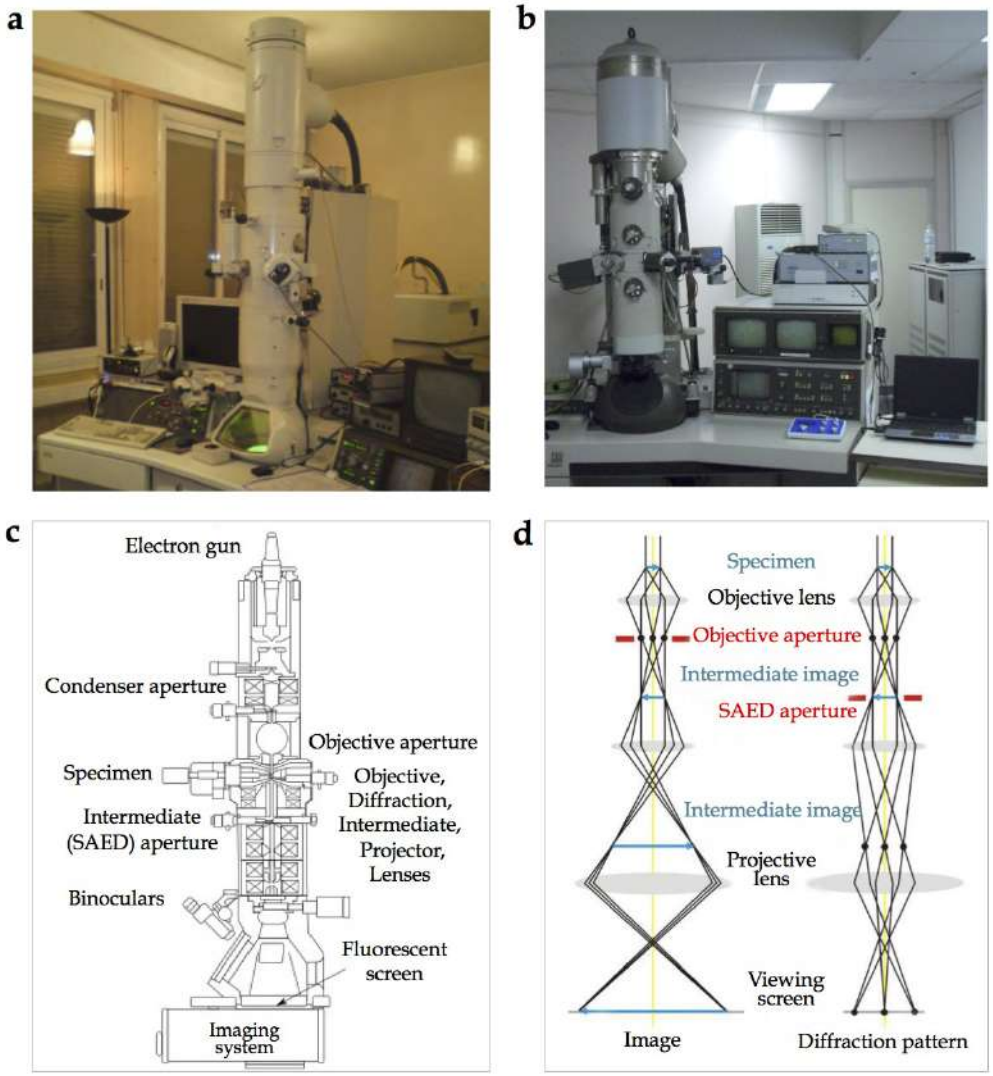

Figure 60: (a) Jeol 2010 HC and (b) Philips CM20 FEG installed in the CEMES laboratory. (c) Schema of a TEM inner column. (d) Conventional TEM imaging mode vs diffraction mode.

- There is no need of a preliminary destructive sample preparation. Once we have selected a ROI by surface and/or cross-sectional analysis, we can directly extract in the FIB a thin lamella for the final polishing in the TEM support.
- We can rapidly obtain (in ~5 hours) thin lamella up to 15 µm wide and deep enough to include the Al metllization, together with a small piece of Si bulk and bonding wire (in the case of wire-metal interface analysis).

On the other side, the main disadvantage of the FIB is caused by the nature of the milling process: the ion collisions, at the base of the sputter removal, can also lead to ion implantation and cause damage to the material. However, various procedures have been developed to reduce this damage [Mayo7].

3.4.1.2 *Sample preparation protocol*

Fig. 61 shows the configuration of the FEI Helios FIB/SEM, used for the TEM lamella preparation. The sample is placed at the eucentric position, where the two beams converge with and angle of 52°, so that the ion machining process is monitored by SEM images in real time. In addition, the gas injection system (GIS) for the deposition of Pt or W is used, as well as a nanomanipulator for the lamella lifting-out (Omniprobe, Oxford Instruments) [Gia11].

The following images, presented to explain the lamella preparation protocol, refer to the metallization away the bonding wire, but the same considerations can be made for the preparation at the wire-metal interface. However the presence of the bonding wire requires a few adaptations that will be further explained.

1. Selection of the area of interest and protective layer deposition.

   The area of interest is selected by performing systematic cross-sectional cuts in order to precisely localize by ion imaging the features for the TEM (Fig. 62a). A Pt layer, with a thickness on the order of 2 µm, deposited just above the region of interest (Fig. 62b) by ion beam (30 kV, 80 pA), is fundamental to protect the lamella during the preparation. Without this protection, the lamella would be destroyed by the ion beam during the final thinning and polishing steps.

2. Bulk-out.

   A sample piece ~ 2 µm thick, containing the final lamella, is cut by removing matter behind the region of interest (Fig. 63). This is done in two steps: we dig close to the lamella by a fast rough milling at high ion beam current (30 kV, 9.3 nA) and we complete with a finer milling at lower ion beam current (30 kV, 2.5 nA).

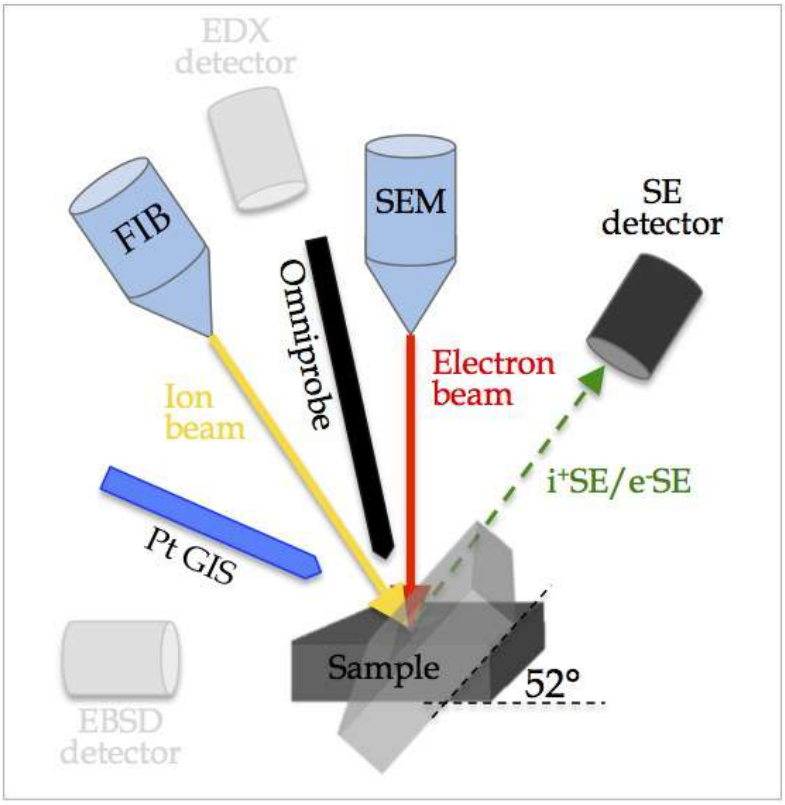

Figure 61: Schematic representation of the dual beam FIB/SEM during the TEM lamella preparation.

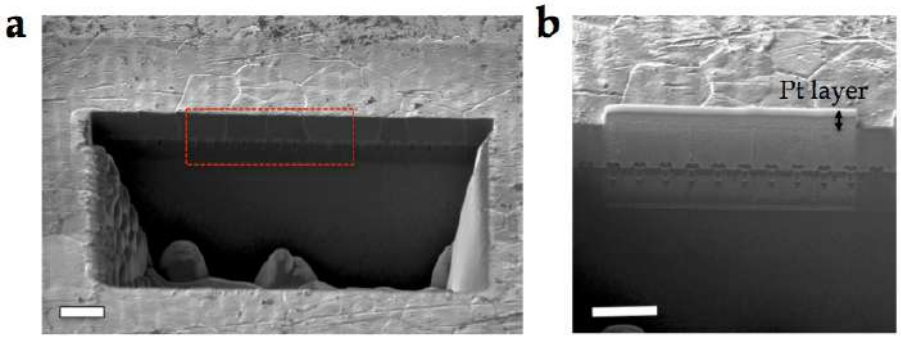

Figure 62: SEM images of the step 1: (a) selection of the region of interest and (b) Pt deposition above it.)

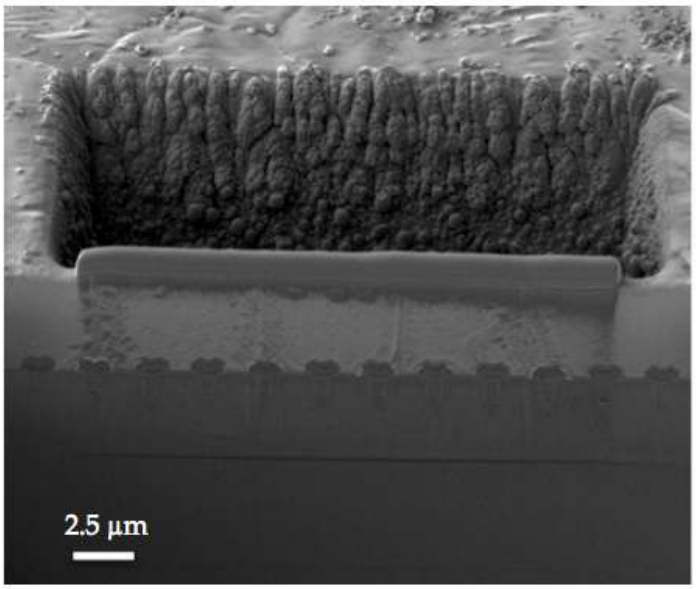

Figure 63: SEM image of the step 2: preparation of a ~ 2 µm thick lamella, by removing matter behind the region of interest.

3. Lamella cut.

   This step consists in cutting the lamella for the extraction. Only a small portion of sample remains attached to the bulk to ensure the lamella stability. The remaining part will be further cut, after the bonding to the Omniprobe. Due to the cut shape (Fig. 64), this step is often called U-cut.

4. Lamella lift-out and TEM grid positioning.

   In this step the lamella is welded to a dedicate TEM support (TEM grid). The transfer is done by a nanomanipulator Omniprobe, consisting in a W tip with the extremity curvature radius of ~ 500 nm. Fig. 65 shows the main steps of the transfer. The GIS is inserted and the Omniprobe is put in contact with the lamella, so that a Pt/W welding deposition fixes the lamella to the Omniprobe (Fig. 65a). Once the lamella is totally cut, the nanomanipulator is moved to the TEM grid for the lamella welding, again by Pt/W deposition. Now the lamella is fixed to the TEM support, so the Omniprobe tip can be cut away and retracted (Fig. 65b).

5. Rough thinning.

   At this stage, the lamella is ~ 2 µm thick with both faces contaminated by amorphous material, due to the previous ion beam machining (Fig. 66a). This step consists in removing the amorphous from both faces and thinning the lamella until 1 µ - 500 nm (Fig. 66b), by using a quite intense

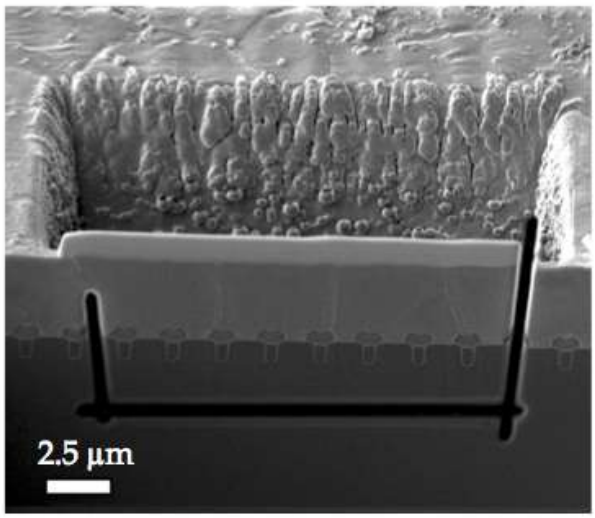

Figure 64: SEM image of the step 3: lamella U-cut prior to the lift-out.

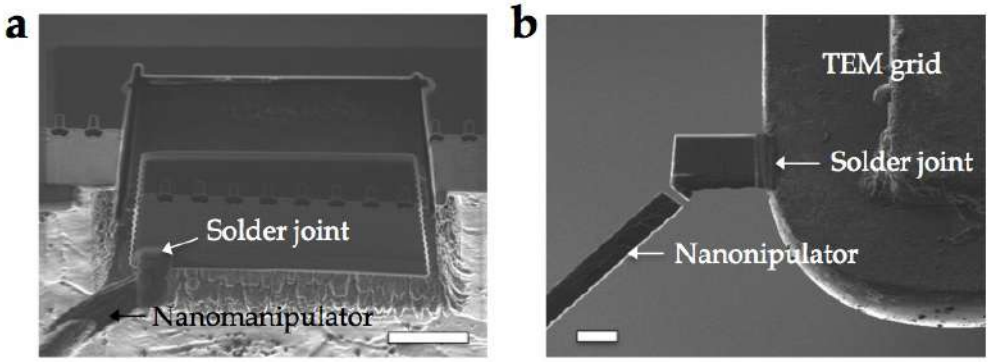

Figure 65: FIB images of the step 4: (a) lamella lift-out and (b) lamella bonding to the TEM grid. Scale bar 5 µm.

ion beam (30 kV, 0.79 nA) with an incident angle of 1°to the normal to the sample surface (in order to obtain two parallel faces [Isho4b].

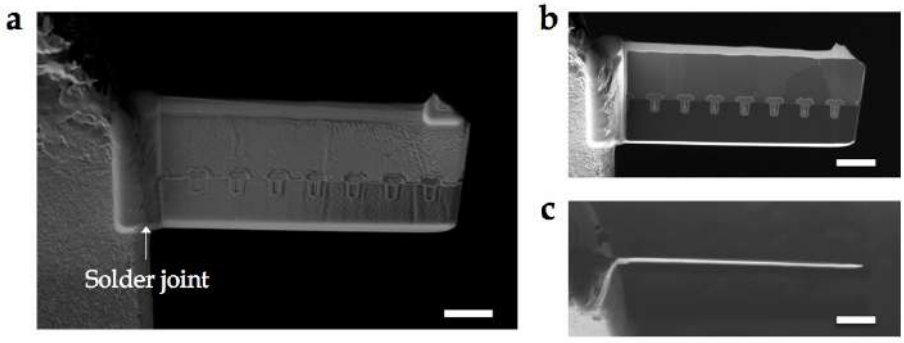

Figure 66: Front-view SEM image of the lamella (a) before and (b) after thinning/polishing step (step 5). (c) Top-view of the final lamella (after step 6 and 7) to check the required thickness of 100-150 µm. Scale bar 2.5 µm.

6. Final thinning.

   In this step we thin and polish each face of the lamella, still too thick for the TEM, until getting a final thickness on the order of 100 nm, required for the electron transparency. The first face is thinned in two steps by an ion beam at decreasing energies and increasing incident angles to the normal to the sample surface, in order to limit the amorphisation of the lamella edges [Isho4b]:

   - 30 kV, 80 pA at 1°;
   - 16 kV, 45 pA at 2°.

   For the second face we follow the same protocol, after a rotation of 180°of the FIB stage, until we obtained the suitable lamella thickness.

7. Finishing stage.

   It consists in removing part of the amorphous on each lamella face by a finer low-energy ion polishing (5 kV, 15 pA) at an incident angle of 3°to the normal to the sample surface. Thanks to the possibility of constantly monitoring the preparation process, we can check the final thickness and make sure that the thin lamella is perfectly straight (Fig. 66c).

The entire procedure is summarized in Fig. 67.

3.4.1.3 *Lamella preparation at the wire-metal interface*

The most critical step when we want to prepare a TEM lamella that includes the wire-metallization interface (Fig. 68) is the matter digging behind the region

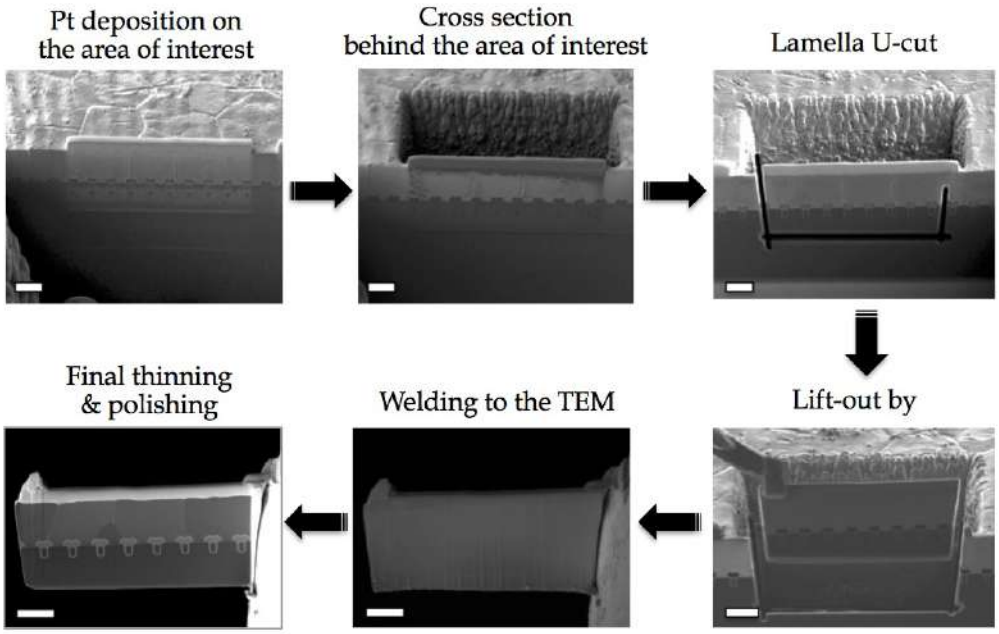

Figure 67: Summary of a FIB lamella preparation for the TEM inspection of the device top Al metallization. Scale bar 2.5 µm.

of interest (point 2 in the previous section). In fact, despite the wire thickness has been locally reduced by a 45°mechanical polishing prior to FIB machining, it is still more than ten times higher than the metallization thickness. So the cross-sectional cut behind the region of interest must be deep enough to remove matter behind the whole piece of wire, down to the metallization and the MOSFET area. Increasing the cut depth means not only increasing the cut duration but also the amount of redeposition gathering at the base of the lamella back-face, making the U-cut impossible to perform.

It is therefore mandatory to increase the cut pattern high behind the wire-metallization lamella (Fig. 69), in order to provide sufficient space for the redeposited matter to spread out in the cut area. In this way, making a rotation of 180°with respect to the front-face, we could also monitor the cut progress and directly check the lamella back-face polishing.

3.4.2 *TEM techniques*

3.4.2.1 *Automated Crystal Orientation Mapping*

The Automated Crystal Orientation Mapping (ACOM) is a transmission electron microscope technique, developed in 1999 by Edgar Rauch (SIMAP, Greno-

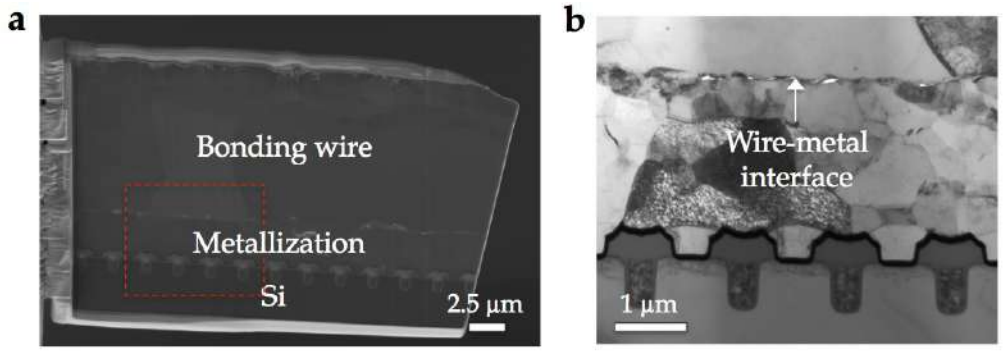

Figure 68: (a) SEM image of a wire-metallization interface lamella prepared by FIB and (b) relative high-magnification TEM image.

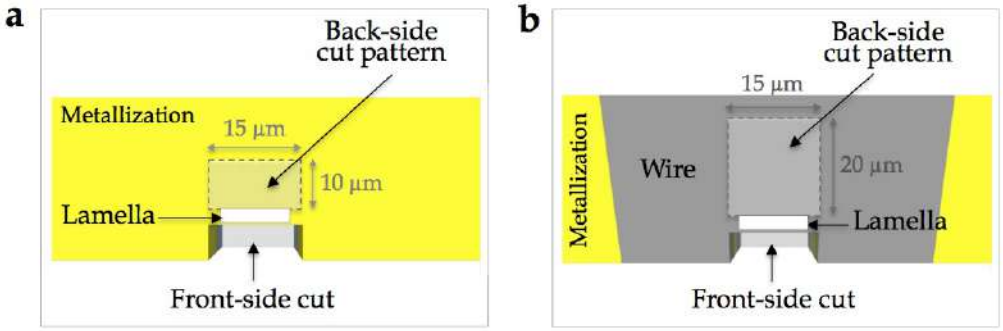

Figure 69: Top view schematic representation of the metallization (a) naked and (b) under the bonding wire, during the lamella preparation by FIB. The dashed rectangular patterns represent the sample area to be milled behind the region of interest, in order to obtain a 1µm thick lamella prior to the lift-out and the final polishing. The pattern in (b) is higher because the area to be milled is deeper, due to presence of the bonding wire.

ble) in collaboration with NanoMEGAS, that allows the characterization of crystalline materials by indexing the diffraction patterns [Rau08] [Rau14]. Orientation mapping, usually performed in SEM by EBSD, is extended down to nanoscale thanks to the reduced probe sizes available in FEG-TEM.

The NanoMEGAS ACOM unit (Fig. 70b) is installed in the Philips CM20 FEG microscope, operating in micro-diffraction mode: it controls the deflection coils, making sure that the electron beam scans the sample, to generate a diffraction pattern from each point of the area of interest (Fig. 70c). At the same time an external fast-rate camera acquires the diffraction signal and send it to a computer, equipped with a software dedicated to the pattern recognition (Fig. 70a).

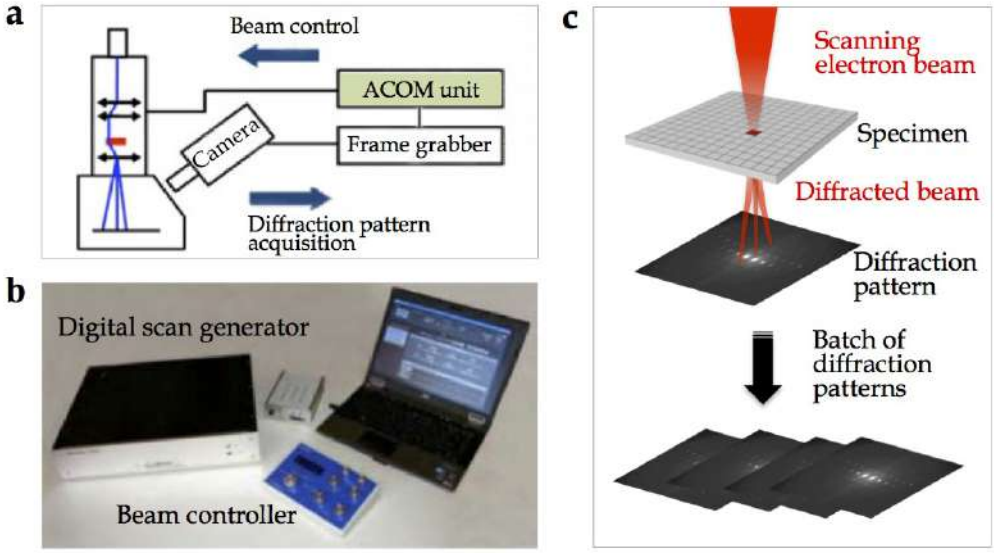

Figure 70: Automated Crystal Orientation Mapping (ACOM).
(a) The NanoMEGAS ACOM unit collects the diffraction signal, acquired by an external fast-rate camera, and controls the electron beam in the TEM.
(b) The NanoMEGAS ACOM unit consists in a digital scan generator, a beam controller console and a computer with the pattern-recognition software.
(c) The digital scan generator controls the electron beam which scans the sample to generate a diffraction pattern from each point of the area of interest.

The software matches the diffraction patterns from the sample with a database of simulated diffraction patterns to identify the most plausible crystallographic orientation of each point (Fig. 71a). The result is then an orientation map of the region of interest, as in Fig. 71b.

This technique allowed us to identify the domains with the same crystallographic orientation (grains), as well as the morphology and the orientation of each grain, in case of multicrystalline materials, with a resolution of about 5 nm. We performed orientation mapping of thin lamella prepared by FIB, to validate the qualitative results of the SIM on Al metallization layer cross-sections, both away and under the bonding wire.

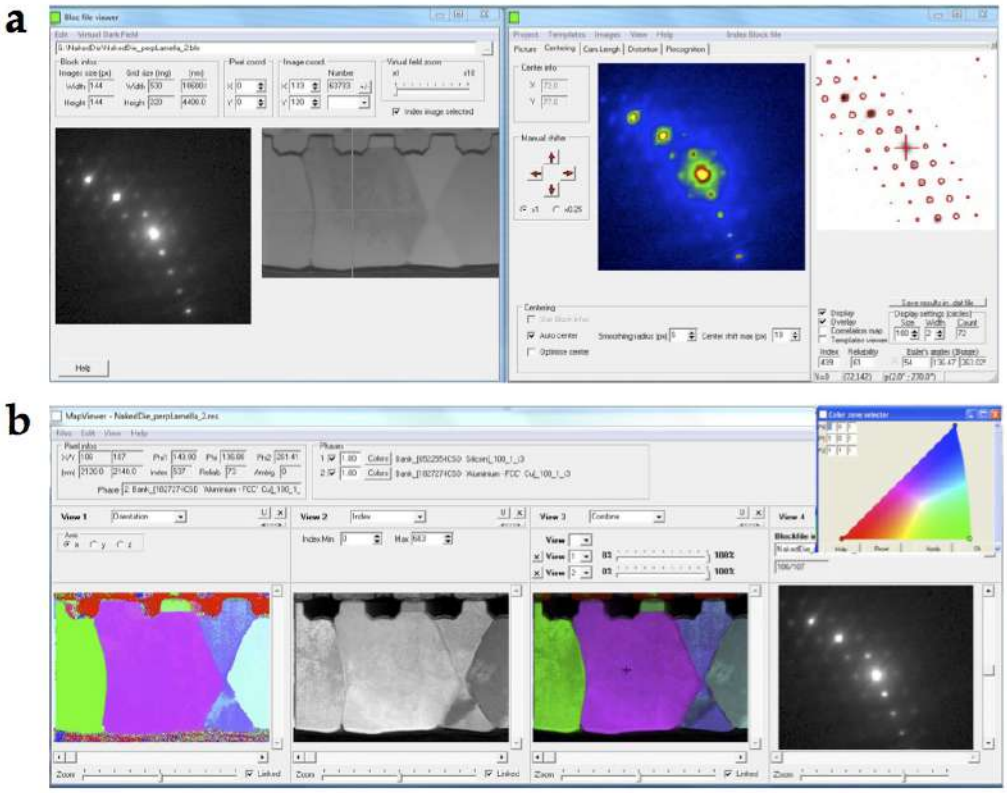

Figure 71: ACOM pattern recognition software windows.
(a) The diffraction image from each point of the area of interest is digitized and compared with simulated diffraction patterns of a databank.
(b) The result of the matching can be visualized in an orientation map, where each color represents a specific crystallographic orientation.

3.4.2.2 *Chemical Analysis: EDX and EELS*

The CM20 FEG microscope is also equipped with an EDX detector for the chemical analysis at nanometric scale of ultra-thin lamella. The x-rays are emitted from the sample, under the interaction with the electron beam, in the TEM operating in STEM (Scanning Transmission Electron Microscopy) mode. As in the SEM, we could have information about the chemical composition of the Al

top metallization. For instance, we could exploit the higher resolution of the TEM to image the Cu-W precipitates in the metallization (Fig. 72a and Fig. 72b) and perform a compositional mapping of the elements present in the region of interest (e.g. Cu in Fig. 72c).

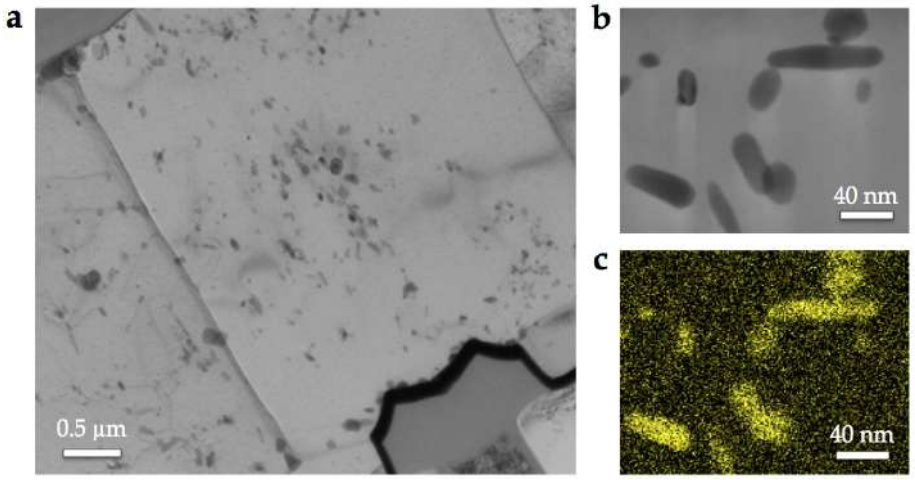

Figure 72: (a) TEM image of the Al metallization decorated with Cu/W precipitates. (b) Higher magnification TEM image of some of these precipitates and (c) relative EDX map, corresponding to the Cu element.

In parallel, Electron Energy Loss Spectroscopy (EELS) was carried out in a Tecnai TEM from FEI. EELS is an analytical technique that measures the change in kinetic energy of electrons after they have interacted with the specimen, giving information about its structure and chemical composition [Ege08], with higher spatial resolution and best analytical sensitivity compared to the EDX [Tit89]. We used EELS in order to investigate the chemical composition of the wire-metal interface, and, in particular, to detect possible bonding process residues of aluminum oxide (AlO_2), that could affect the good contact between the two Al parts. The reason why we preferred EELS to EDX is that, in the EELS spectra, we can clearly distinguish the contribution of the oxygen in its linked-state from the surface contamination. However, this technique requires a TEM lamella thickness between 50 and 70 nm, lower than the one needed for conventional TEM imaging and orientation mapping (100-150 nm). Consequently, the final thinning-polishing step of the FIB preparation has been particularly demanding in this case. In order to avoid the risk of amorphization and bending of the final lamella, we had to reduce the size of the region of interest.

3.4.2.3 *In situ heating experiment*

The TEM in situ technique allows us to observe in real time the evolution of the sample micro and/or nanostructure, when a controlled change to the specimen environment is made. In our work, temperature experiments have been carried out. In particular, we were interested in studying the temperature-induced degradation mechanisms of the Al metallization layer, deposited onto the silicon substrate. In fact, at this location, the temperature changes result in mechanical stress due to the difference in the CTS between the Al and the Si [Leg09]. The TEM, generally used in conventional mode, allowed us to follow the dislocations and grain boundaries evolution inside the Al metallization during the temperature cycles.

In situ experiments was carried out in the JEOL 2010 TEM, equipped with a double tilt heating holder from Gatan (Fig. 73b). It consists in a heating micro-resistance and a temperature sensor (Fig. 73b), both controlled by a dedicated module for the temperature setting (Fig. 73a). The sample holder can reach 500 °C, without cooling system, and 1100 °C, by activating an external water-cooling system. However, in our experiments we did not need to exceed 500 °C. In fact, during the normal life of a device, the control die prevents the power die getting this temperature. So we decided to perform repetitive cycles from ambient temperature to 450 °C, with a rate of 50 °C/min. At the same time, the TEM CCD camera, connected to a recording device, acquired the sample structural evolution.

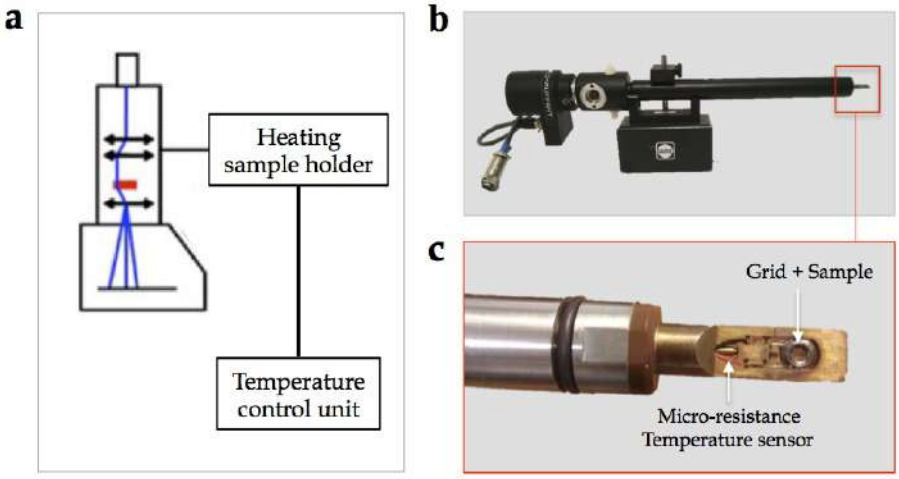

Figure 73: In situ heating TEM settings. (a) The JEOL 2010 is equipped with a (b) double tilt heating holder (Gatan) connected to a temperature control unit. (c) The TEM grid containing the sample is placed at the extremity of the sample holder and it is connected to a heating micro-resistance and a temperature sensor.

4

RESULTS

This chapter presents the results of the study of Smart Power SPD06 and T07D17 devices that underwent accelerated electro-thermal aging conditions (described in Section 2.2.4). During the on-off cycles, the top source metallization increases its resistance, and thus its temperature, until failure. Our objective is to correlate the evolution of the electrical parameters during aging with the parallel microstructural degradation of the metallic parts. We go down to the submicrometric scale, trying to understand the physical phenomena behind the resistance and temperature increase. Our characterizations, based on the physical-metallurgy approach described in the previous chapter, focus on the grain structure of the metallization and on the interface of this metallization with the bonding wires. Previous studies [Cia02] have shown that these locations are the most prone to deterioration. This will be confirmed in the first paragraphs of this chapter. We systematically compare the module under test –we call it "aged" or "failed"– with the modules of the device that did not underwent the electro-thermal cycles –we call it "as-is" or "as processed"–.

The main mechanism associated to the mechanical stress of the metallic parts is the generation of fatigue cracks in the Al metallization. We demonstrate that these cracks follows the grain boundaries. For this reason, we focus on the Al grain structure, which is subject to plastic deformation during the electro-thermal cycles. We characterize the grains evolution by electron backscattered diffraction, at surface, and by ion microscopy and automated crystal orientation mapping, in cross-section.

The cross-sectional analysis of the Al metallization constitutes the main contribution of this work, as at surface level the grain structure upon aging is lost because of a heavy surface reconstruction. The metallization is inspected at two different locations: under the bonding wires and away from the bonding contact (naked metallization). In the latter case, we investigate also the areas coated by SiO_2 passivation (when present). We present the results of the study on the two types of LFET1T technology in two different Sections:

- Section 4.1 : 24V SPD06 components
- Section 4.2 : 12V T07D17 components

This organization is due to the fact that NXP Semiconductors provided us with the devices at different times, so we adapted our research to the industrial needs evolution. First, the SPD06 (in production since 2008) served as

test components to optimize the techniques, together with the relative sample preparations used in this work. Since they underwent gradual short-circuit conditions, we could follow the degradation mechanisms at increasing electrothermal cycles until failure and identify the points of interest. On the other side, the T07D17 (in production since 2009) components have been provided later by the company. Those were endured industrial aging tests until failure. We used these devices to improve our study, on the basis of the previous results, and to investigate the effects of abrupt electrical overstress (EOS) on the Al microstructure. Moreover, the instrument availability evolved during this work. This is the reason why we could perform large scale cross-sectional cut by Cross Polisher only to study the entire wire-metallization interface of T07D17 components, while we have been limited to smaller cross sectional cuts by Focused Ion Beam for the SPD06 ones. However, both types of device belong to the same technology batch, and there is no difference in terms of their critical features of our analysis, such as Al metallization thickness, MOSFET type, wires bonding process and size. Therefore, in the following we have assumed that the results found for the T07D17 modules are valid also for the SPD06s.

4.1 AGING OF SPD06 COMPONENTS

For SPD06 devices under increasing electro-thermal cycles, we have systematically compared the metallization microstructure of the aged module and the as-processed one, until 300kcycles, just before failure (which occurs at ~ 315kcycles). At the end of the aging test, a clear change in the metal surface is easily visible even by optical microscopy (Fig. 74): the failed module looks darker and less bright compared to the adjacent one, that did not undergo the electro-thermal cycles. We investigate the finer evolution of the metal microstructure at higher resolution, first by SEM (Section 4.1.1), and by FIB and TEM later (Section 4.1.2), in order to find a possible explication of the on-state resistance increasing in the Al degradation mechanisms.

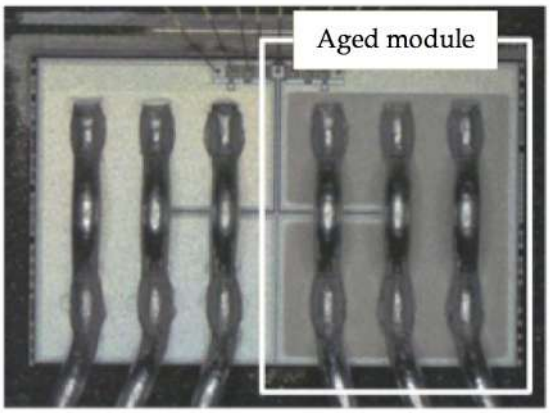

Figure 74: Optical image of an SPD06 power die after accelerated aging test (300 kcycles at room temperature). Only one module underwent the electro-thermal cycles, whereas the other one serves as reference for the microstructural characterization of the critical points.

4.1.1 *Topographical study*

A closer inspection by SEM of the Al top metallization confirms the optical result (Fig. 74): the Al microstructure image at failure (Fig. 75b, c) is significantly different to the relative as-is part (Fig. 75a) and reveals a heavy surface reconstruction, which is not uniform in the analyzed module. Some zones, close to the central wire contacts, presents a higher roughness (Fig. 75b), in others the Al grain structure is still visible but large cracks propagate along the grain boundaries (GBs) (Fig. 75c), or a mix of the two.

In the following we focus before on the as-processed Al structure and then we show its evolution at increasing number of electro-thermal cycles.

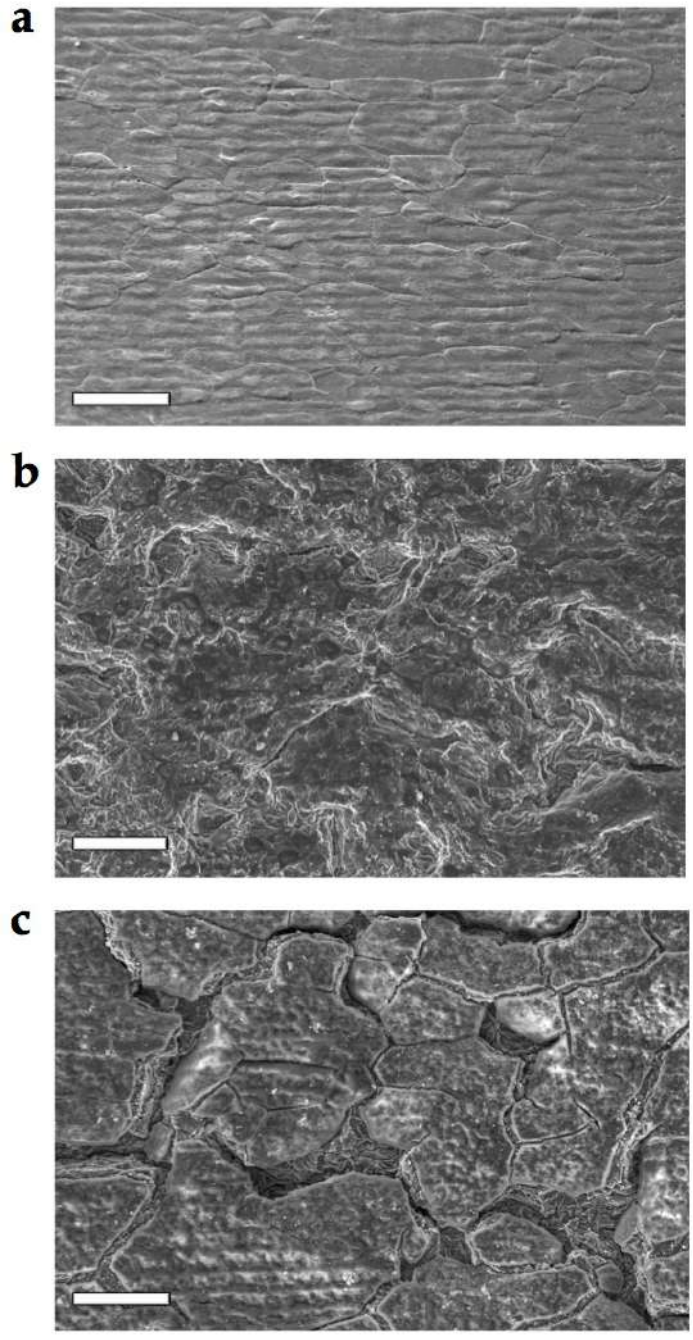

Figure 75: Top view SEM images showing the Al metallization of (a) an as-is module and (b), (c) a failed one at two different locations. The grain structure is visible in all of them as GBs are slightly grooved in (a) and more heavily cracked in (b) and (c). Scale bar 10 μm.

4.1.1.1 *As-is metallization microstructure*

(Fig. 75a) shows that the initial Al metallization is characterized by a granular microstructure that is made visible by the grooves formed by the intersection of the GBs at the surface [Mul93]. The horizontal "wave" pattern is due to the underlying transistor architecture. EBSD orientation maps of as-is metallization portions (Fig. 76a) allowed us to accurately characterize the initial Al microstructure. They reveal a strong <111> texture along z, that is the deposition direction. From these maps, we can also determine the grain misorientation and size distributions. To identify the grains, and therefore calculate their size, the definition of a critical misorientation angle is required, so that all boundary segments with an angle higher than the defined angle are considered grain boundaries (GBs). The critical angle between low- and high-angle grain boundaries is usually set between 10 and 15 ° [Hum01] depending on the crystal structure. The physical reason for this value lies in the fact that dislocations constituting low-angle grain boundaries (or sub-grain boundaries) are discernable while they become close to each other and thus indiscernable in high angle GBs. From the analyzed area (Fig. 76a), we can plot a grain misorientation distribution (Fig. 76b), from which we decided to take the lower peak (10°) as the critical angle between low angle and high angle GBs. From this, the grain size distribution (Fig. 76c) is then calculated by grain reconstruction method (see Section 3.2.2). We can see in the plot that the mean grain size (~4 µm) is on the same order, or even larger, than the Al metallization thickness.

4.1.1.2 *Aged metallization microstructure*

Fig. 75b and Fig. 75c show an important degradation of the Al metallization structure at failure. It is characterized by an increase in surface roughness and the presence of several large cracks along the grain boundaries. In some cases, it is no possible anymore to recognize the initial grain structure.

We asked ourselves when the surface reconstruction starts to show up during the life of a SPD06 component. To answer this question we observed by SEM the Al metallization evolution after increasing aging until failure, which occurs at 315 kcycles. Fig. 77 shows the metal microstructure a) before aging and after b) 1, c) 10, d) 100, e) 200 and f) 300 kcycles. One can notice a weak change in the Al surface starting from 10kcycles (Fig. 77c), but it is only after 100kcycle (Fig. 77d) that we observe a significant reconstruction. For sake of accuracy, we have to precise that each SEM image in Fig. 77 refers to a different SPD06 device aged at increasing number of cycles. We tried to follow the evolution of the same metallization portion, in the same device, but it turned out to be impossible. In fact, every time we stopped the aging cycles to inspect the metallization by electron beam, the device systematically failed as soon as we

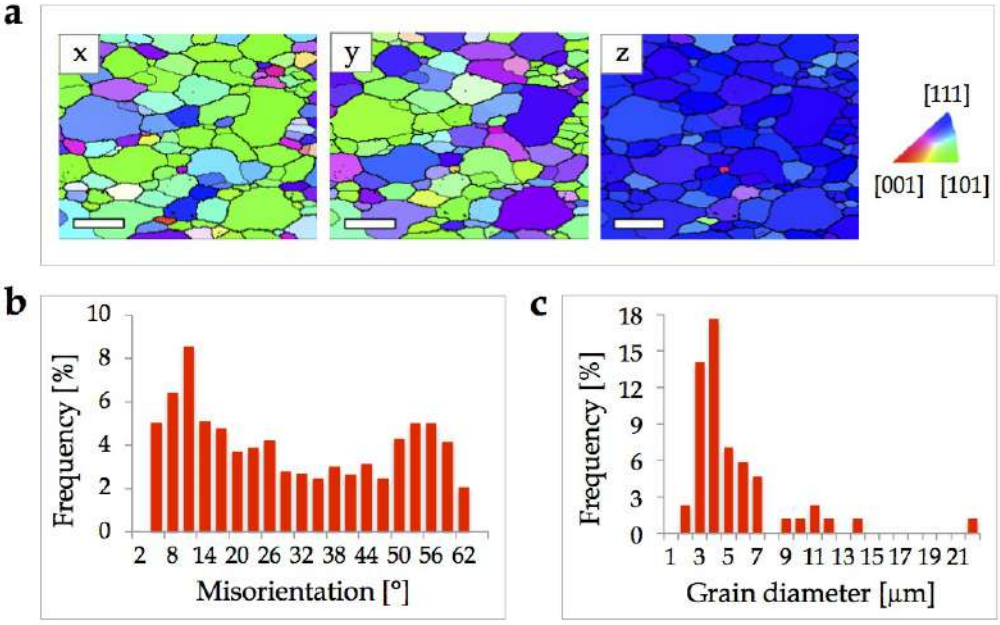

Figure 76: (a) EBSD orientation mapping along x, y and z axis of the Al metallization of a reference module and relative histograms of the (b) grain misorientation and (c) grain size (equivalent diameter).

restart the test. We suppose that this is due to a charge accumulation during the interaction with the electron beam in the SEM, that causes the failure when the device is put again in the on-state. However, since the device production is highly reproducible and the initial metal structure is similar in all the analyzed modules, we assume that all the devices age similarly.

Observations:

- After 1kcycles (Fig. 77b) we do not observe any sign of surface reconstruction, the grain structure is preserved and the horizontal transistor wave pattern is still visible. However, some grains are characterized by a sort of ridge-notch pattern (white arrows). It is evident at higher magnification in Fig. 78a (in the big central grain). This could remind the intrusions and extrusions formation at the basis of fatigue cracks initiation in metals under stress cycles [Sur98]. If so, the inner Al structure beneath the ridges should be characterized by slip bands along the <111> direction, containing stack of several aligned dislocations. However, the TEM image (Fig. 78c) of a FIB lamella perpendicular to the ridge-notch pattern from the grain of interest (Fig. 78b) does not present these features: only

few dislocations (black contrasted traits in the TEM image) are uniformly distributed in the grain portion close to the surface.

- After 10kcycles we start observing a surface reorganization (Fig. 77c): the grain boundaries are less defined and we loose the transistor wave pattern.
- But it's only at 100kcycles that the Al surface reconstruction occurs (Fig. 77d). The Al metallization here looks similar to the failed one close to the bonding contacts (Fig. 75b).
- However, several cracks propagate along the grain boundaries and it seems that they become larger and larger at the final aging steps (Fig. 77e and 77f).

This means that, starting from 100 kcycles until failure, the evolution of the metallization surface occurs at the grain interfaces. It could have been interesting, then, to follow possible rearrangements of the grain structure until failure by EBSD. In particular the apparent grain size reduction that is observed by FIB (see Martineau et al. [Mar10], Bernoux et al. [Ber09]], and following paragraphs) could have been quantified in terms of misorientations and validated or invalidated. However, this turned out to be unfeasible because of the high surface reconstruction. This reconstruction strongly increases the surface roughness which is a known factor to impede the EBSD signal-noise ratio [Mic07], [Rei86] [Schoo]. The few attempts to obtain pseudo Kikuchi EBSD patterns from aged metallization confirmed this impossibility. For this reason, we decided to prepare cross-sections of the metallization perpendicular to the surface and observe the inner grain structure by ion channeling contrast.

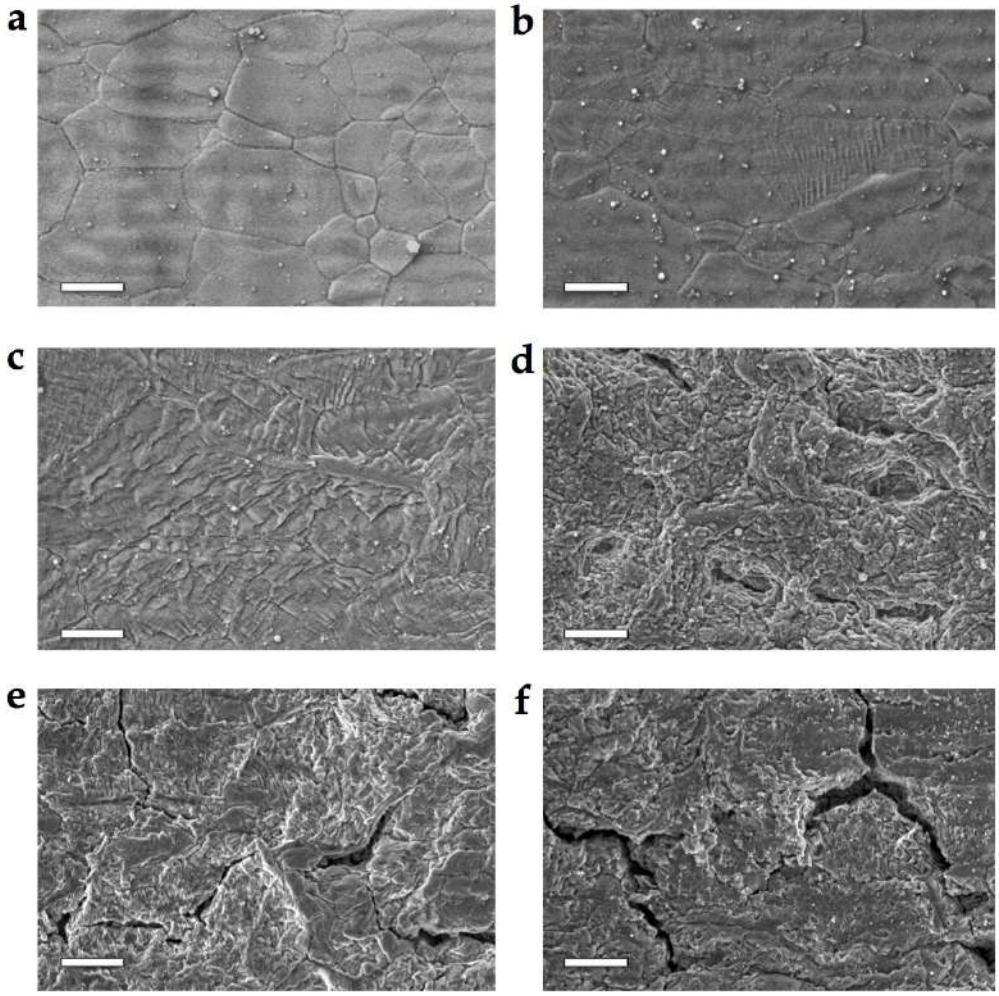

Figure 77: Top view SEM images showing the evolution of the Al source metallization surface. Grain structure (a) before starting the accelerated aging and after (b) 1 kcyles, (c) 10 kcycles, (d) 100 kcycles, (e) 200 kcycles and (f) 300 kcycles. Scale bar 5 μm.

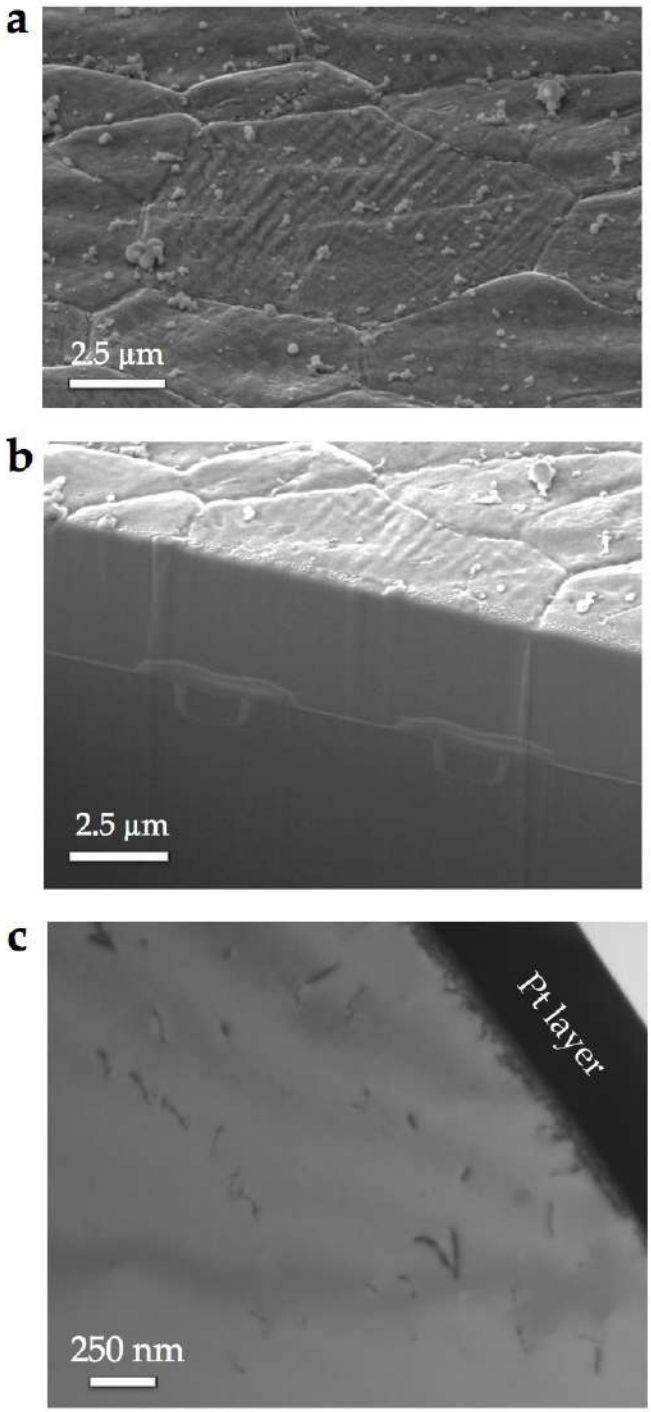

Figure 78: (a) SEM image of the Al metallization from a 1kcycles aged module. The bigger central grain is characterize by a ridge-notch pattern. We have investigated the dislocation distribution beneath this area by TEM, preparing an ultra-thin lamella by FIB. The first step of the preparation (a cross-sectional cut perpendicular to the surface, ahead of the region of interest) is depicted in (b). (c) The TEM image just below the Al metallization surface (covered by a dark-contrasted Pt protective layer) reveals the presence of few uniformly distributed dislocations (dark lines) and the absence of slip bands.

4.1.2 *Cross-sectional study*

Systematic cross-sectional cuts of the metallization in the vicinity of the bonding wire (naked metallization) have been prepared by FIB (Section 3.3.1.1). Thanks to the original sample preparation that we set up to locally reduce the wire thickness (Section 3.3.1.2), we could also access the metallization under the bonding connections and compare it to naked parts.

In the following, the results of the aged metal refers to modules underwent 100kcycles and more, characterized by an evident surface reconstruction (Fig. 77).

4.1.2.1 *Naked metallization*

Using SIM imaging, the initial grain size appears on the order or larger than the metallization thickness (Fig. 79a) outside of the wire bonds area. This kind of structure is called "bamboo" as most of the grain boundaries run perpendicular to the surface down to the substrate ([Arz11], [Joo94], [Wal92a]). A TEM cross-section oriented using the ACOM system (Fig. 80) reveals a strong <111> texture along the deposition direction. This confirms the results of the EBSD mapping of the initial metallization surface (Fig. 76a) and shows that each grain orientation is conserved from the surface down to the transistor region.

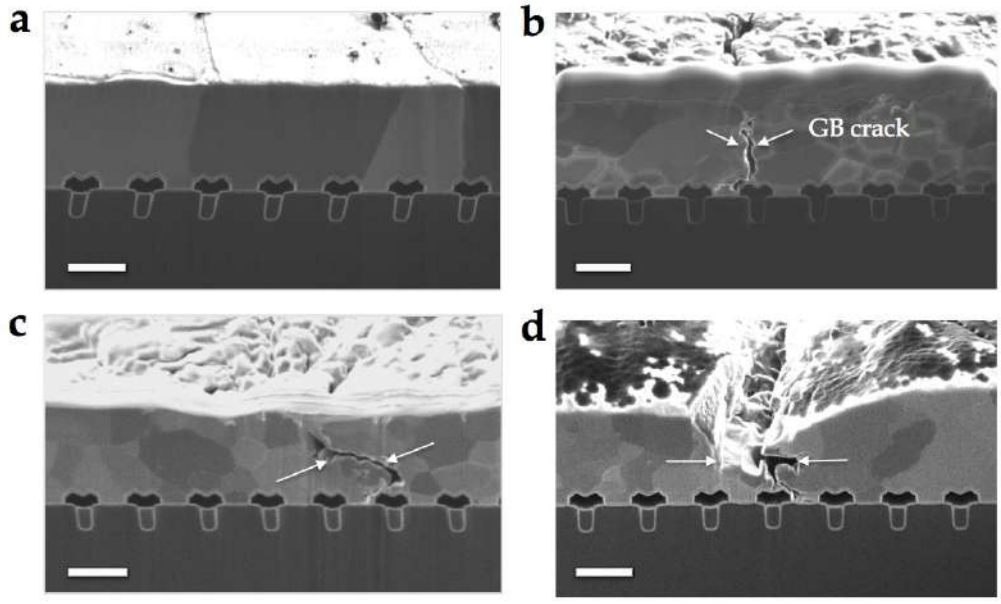

Figure 79: SIM imaging of the Al source metallization of an (a) as-is and (b) 100, (c) 200 and (d) 300 kcycles aged power modules. Scale bar 2 µm.

In Fig. 79b-d we can observe the metallization cross-sections of aged modules, respectively at 100, 200 and 300 kcycles. Aging seems to lower the grain size, as also observed by Bernoux [Ber09] and Martineau [Mar14]. We tried to measure the average grain size in a tens of SIM images from as-is and aged modules by lineal intercept method. This method take into account the number of times that a series of uniformly distributed lines drawn on the SIM images intercepts the grain boundaries and returns a mean lineal intercept length, which can be associated to the grain size [Tom45]. The result for a 100kcycles aged device is reported in Fig. 81, showing that the average grain size is ~ 4 times lower in the aged metallization compared to the as-is one.

However, ACOM mapping shows that most of the grain domains revealed by FIB have a small misorientation, less than 10°. Fig. 82 shows this as two grains

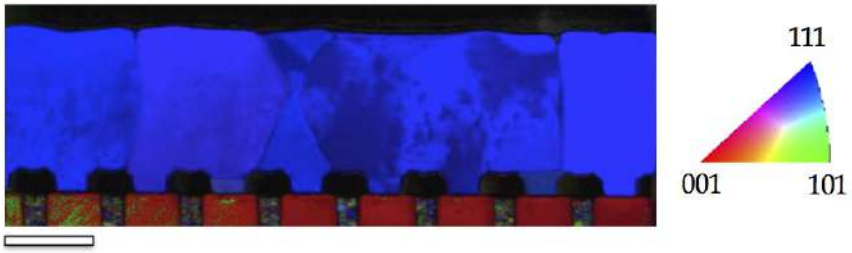

Figure 80: ACOM mapping of the cross-section of an as-is module, showing a strong <111> texture of the Al grains along the deposition direction. The standard stereographic triangle gives the color codes of the grain orientations, taken here along the vertical growth direction. Scale bar 2.5 µm.

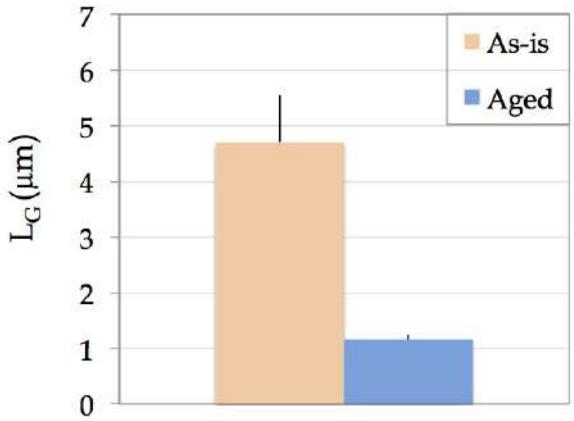

Figure 81: Grain size calculated by lineal intercept method in 10 FIB cross-sections of each analysed module, both aged at 130 kcycles (in blue) and as-processed (in orange).

(1 and 2) visible in ionic contrast (Fig. 82a) have only an 8°misorientation when measured by the ACOM system (Fig. 82b and c). These are then subgrains potentially formed by the gathering of pre-existing dislocations inside a single initially large bamboo grain [Mar14]. This process may occur very early during aging and does not seem to have impact on further GB cracking.

Moreover, many cracks, running from the surface to the Si substrate, are observed (Fig. 79b-d). They follow the grain boundaries and broaden at the end of the life of the device, confirming the previous observations at surface level (Fig. 77d-f).

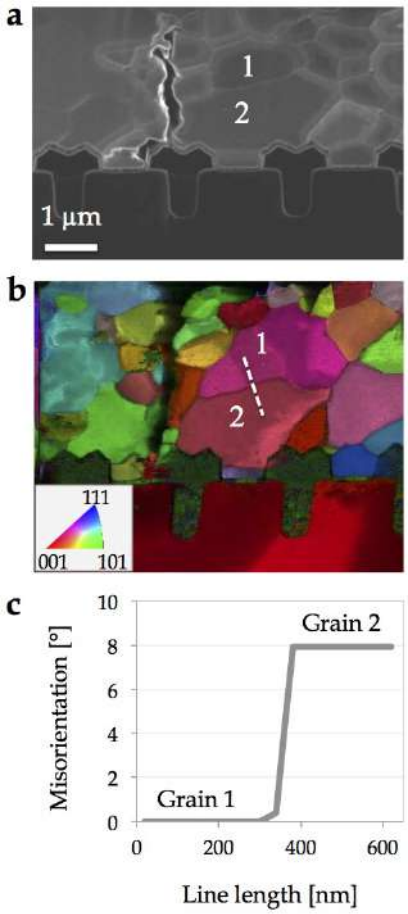

Figure 82: (a) FIB imaging and (b) ACOM orientation mapping of the source metal of an aged module (short circuit, 130k cycles) at the interface with the Si substrate. The standard stereographic triangle gives the color codes of the grain orientations, taken here along the horizontal direction. (c) The plot represents the misorientation between the grains 1 and 2 along the white line in b).

4.1.2.2 *Metallization under the bonding wire*

Fig. 83 shows SIM images of the wire-metallization interface from the side of the bonding contact (Fig. 83b and c) and at the center (Fig. 83d-g) for an as-is module (left) and a 100kcycles aged one (right), according to the larger view in Fig. 83a. Under the wire, the initial Al metallization has endured plastic deformation, due to the cold-bonding process, and the initial grain size seems systematically smaller compared to the bamboo structure of the naked metallization (Fig. 79a).

One can also notice that the wire-bonding interface is not uniform all along the bonding, for both the as-is and the aged part.

- The contact between the two metals is systematically absent at the two edges (for ~ 10µm towards the inside) even prior to aging (Fig. 83b and c). This demonstrates that only a fraction of the nominal metallization area impacted by the bonding (0.25mm², according to the LFET1T standard specifications) is truly in contact with the wire of metallization surface is truly in contact with the wire. A very coarse estimation would lead to a third of the metallization being impacted by wire-bonding plastic deformation [1].

- In the central area (Fig. 83d-g), the bonding between the metallization and the wire shows initial imperfections, probably due to Al oxide (appearing in white contrast in SIM imaging) and small cavities. Moreover, the plastic deformation is highly uneven along the applied stress of the wire bonding, which is perpendicular to the wire-metal interface. Some section shows a straight interface (Fig. 83d and e), whereas in other ones (Fig. 83f and g) the source metallization is more deformed.

We tried to quantify the plastic deformation of the source metallization under the wires, by measuring the minimum metallization thickness in the FIB sections (Fig. 84b) and taking the initial metallization thickness (away from the

1 To estimate the effective imprint of the wire on the metallization, we made the following calculation and assumption: The plastic deformation of the metallization imposed by the bonding process is about 10% in average in compression (Fig. 85). If we assume that the yield stress of the metallization is only dictated by its grain size (which is an underestimate because we neglect the effect of alloying), it should have deformed at stresses between 100 to 150 MPa (values given by Tsuji et al [Tsu02]). The force imposed to the 0.25mm^2 metallization by the wire is on the order of 10 N which correspond to a stress of 40 MPa only. This should not be sufficient to deform the metallization unless only a portion of the metallization is impacted. A simple rule of mixture leads to about 1/3rd of the surface of the wire imprint ($40 * 3 = 120$MPa).

wire) as a reference (Fig. 84a). The deformation is then locally calculated as follow:

$$\epsilon = \frac{l_{ref} - l_{min}}{l_{ref}} \tag{6}$$

Fig. 85 shows the plastic deformation values of the Al metallization under the bonding wires of as-is and aged modules for three devices: aged at 1, 100 and 300 kcycles. Plastic deformation ranges from 5% to 25% in the measured sections (7 for each analyzed module, each one $\sim$ 15μ m wide). This wide range may be due to the fact that the number of measured cross-sections (7 for each sample) is not enough to have consistent statistics or to the fact that the wire-metallization interface is highly uneven along the wire-metal interface (in line with the high standard deviation relative to each data set). Moreover, we can notice that the metal under the bonding wire is severely deformed prior to aging and upon electro-thermal cycles the amount of plastic deformation perpendicular to the interface does not change significantly. However, grain growth is observed, at variance with what happens outside the wire-bonding area. The initial dislocation density is also higher in this zone, which forecasts larger rearrangements, cell formations and subsequent grain boundaries creation.

These results have been further exploited in the next session, relative to the microcharacterization of T07D17 power device. We have improved the number of analyzed cross-sections and proposed different methods for the measurement of plastic deformation.

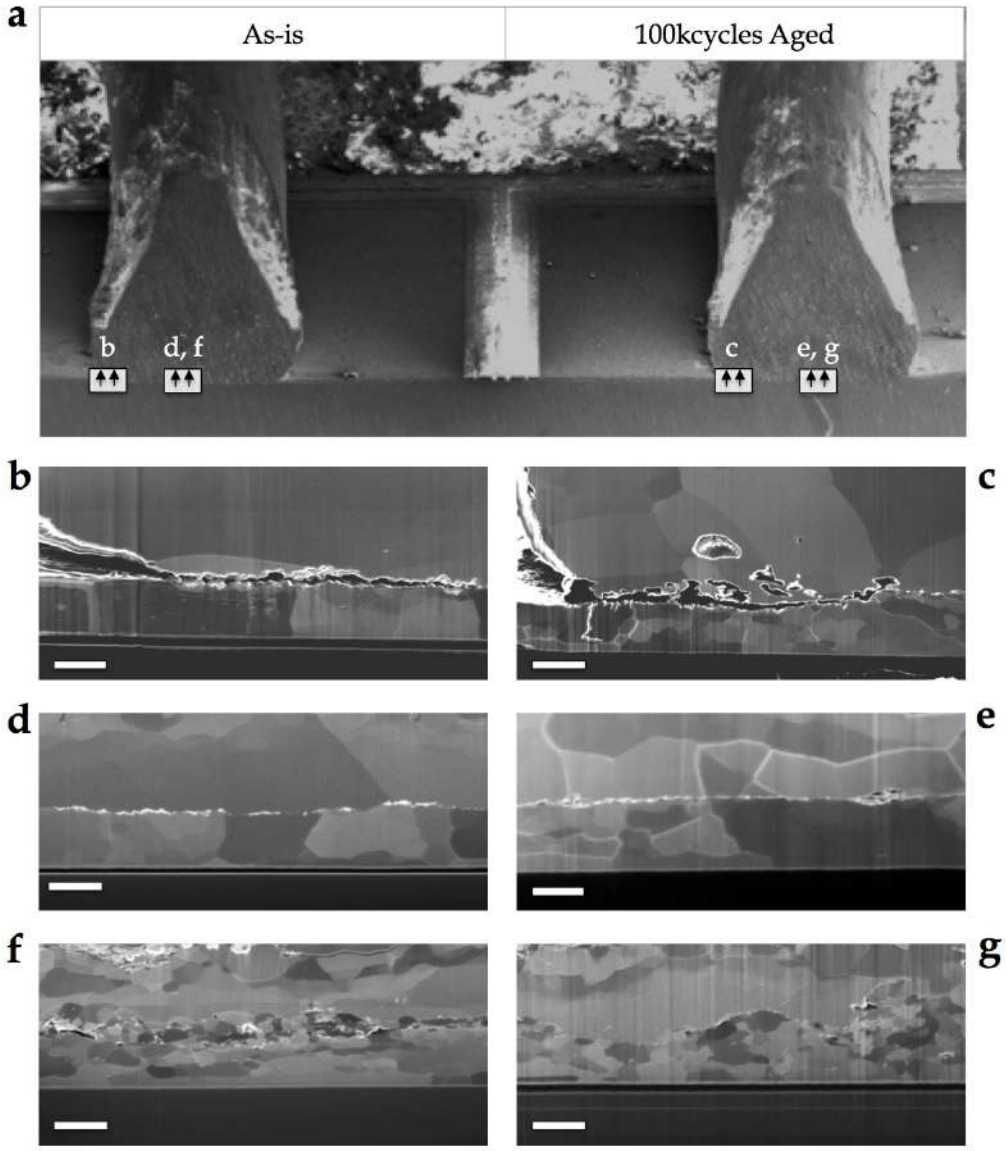

Figure 83: (a) FIB cross-sectioning schema under a 45°polished bonding wire from an as-is module (left) and an aged one (right). The arrows indicate the imaging direction.
The relative SIM images have been collected from the edge of the bonding wire of the (b) as-is and (c) aged (100 kcycles) module, and at the center of the bonding wire of the (d,f) as-is and (e,g) aged (100 kcycles) module. Scale bare 2.5 µm.

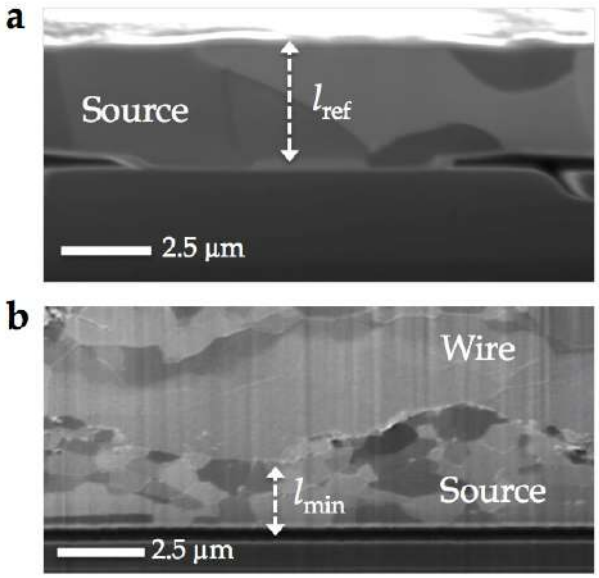

Figure 84: SIM images of the Al metallization (a) away and (b) under the bonding wire. The naked metal thickness (l_{ref}) serves as reference for the measurement of the minimum thickness (l_{min}) in the deformed sections under the bonding wires.

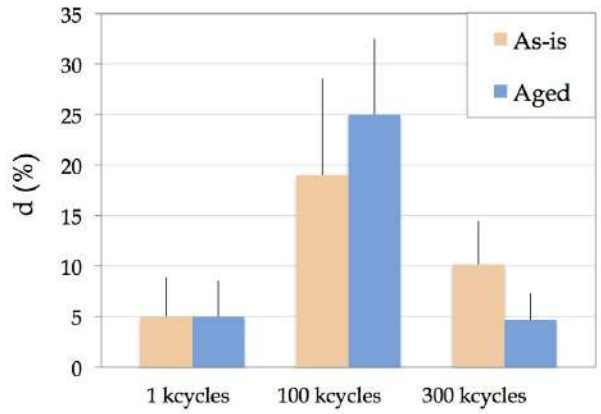

Figure 85: Plastic deformation of the Al metallization under the bonding wires of the as-is and the aged module of three different devices: aged at 1, 100 and 300 kcycles. The deformation has been calculated as the minimum metallization thickness in the wire-metallization FIB sections (7 for each analyzed module, each one ~ 15µ m wide), taking the initial metallization thickness (away from the bonding wire) as a reference.

4.1.3 *Temperature cycles: TEM heating in situ experiments*

To observe the behavior of the dislocations and grain structure of the metallization under thermal cycling, cross-sectional TEM samples were prepared and in situ heated and cooled, in the microscope, between 25 °C and 450 °C by steps of 10-50 °C. A complete cycle takes roughly 40 minutes for the first one (20 °C/min in average) and usually faster for the subsequent ones (because the dislocation movements are more scarce). The dislocation propagation inside the Al grains are observed in real time. It is induced by stresses due to the difference of CTE between silicon, silicon oxide and aluminum. Two types of samples were prepared: one with a FIB lamella welded to a Cu grid, and another one with a tripod polisher. The reason for this is that in a FIB lamella, the leftover of the Si substrate is too small to induce significant stresses in the Al layer.

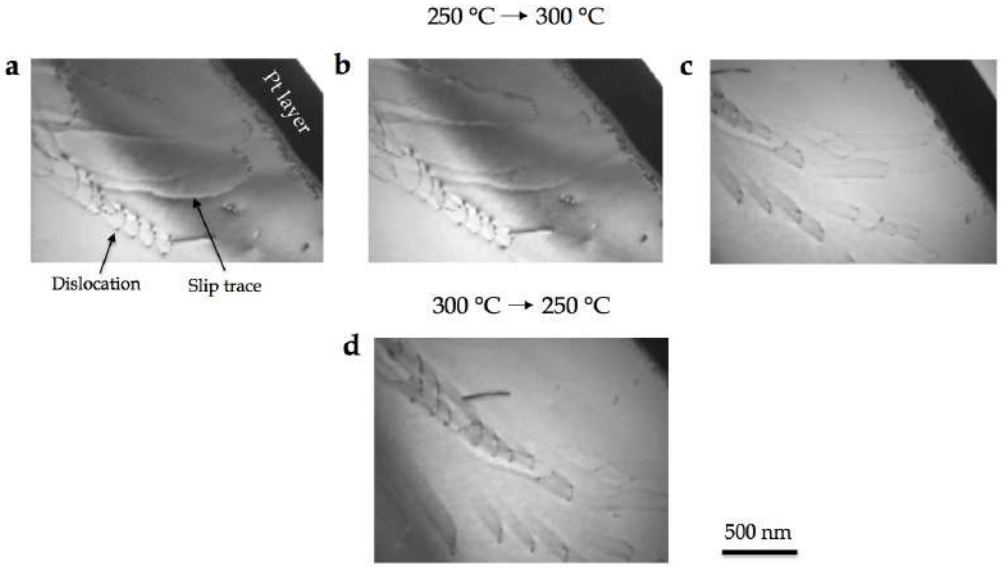

Figure 86: In situ TEM thermal cycling of a device FIB-prepared cross-section from 25°C to 450°C. (a)-(c) are snapshots captured during the heating up phase from 250°C to 300 °C, showing curved slip traces associated to a combination of dislocation climbing and gliding. Once the dislocations are dispersed, during the correspondent cooling down phase (d), no reverse motion is observed because the Si substrate is too thin to induce significant stress in the Al film.

This is verified in Fig. 86 : during heating a group of dislocation starts to move at around 300 °C. These movements are probably generated by the repulsive interaction between the dislocations that seem to have all the same Burgers vector (same contrast). Once they are dispersed, the absence of stress

due to the very thin Si substrate leftover is not able to reverse their motion during cooling. As anticipated, a subsequent cycle (50-450 °C) did not make the dislocations move again. One can note that the slip traces are curved, which indicates that, in this temperature range (> 300°C), dislocation motion involve a strong proportion of climb (in pure planar glide, the slip traces would be straight, and if cross-slip was present, they would display a zig-zag pattern).

A second type of sample was prepared using tripod polishing (procedure in Appendix A). In this cross-section configuration, the full substrate thickness is preserved (in a thin foil, of course), retaining part of the deltaCTE-originated stresses. As a result dislocations motions are partly reversible, following the stress inversion expected in a Al/Si substrate thin film (Fig. 87g). As observed previously, dislocations are "activated" during heating up. At variance from the FIB lamella, those dislocations move even if they are apart from each others (Fig. 87a, b) , suggesting that the stress originates from the delta CTE. This is even further confirmed during cooling where reversible motion of the dislocations left in the interiors of grain is observed. They are first straightening (Fig. 87c) before bowing in opposite direction (Fig. 87d) and moving towards the oxide and the grain boundaries. Once they reach these spots, they are trapped and do not move further (Fig. 87e, f). This is why the dislocation density decreases rapidly over the first cycles. In a TEM, where there are free surfaces created when preparing the thin foil, the phenomenon is accelerated, and after a couple cycles, no moving dislocation can be observed anymore. As previously observed, dislocations move using a mix of climb and glide, the first process being important above 350 °C and the second around 200 °C and below.

In both experiments, no grain growth was observed. No subgrain formation was observed during these heating experiments.

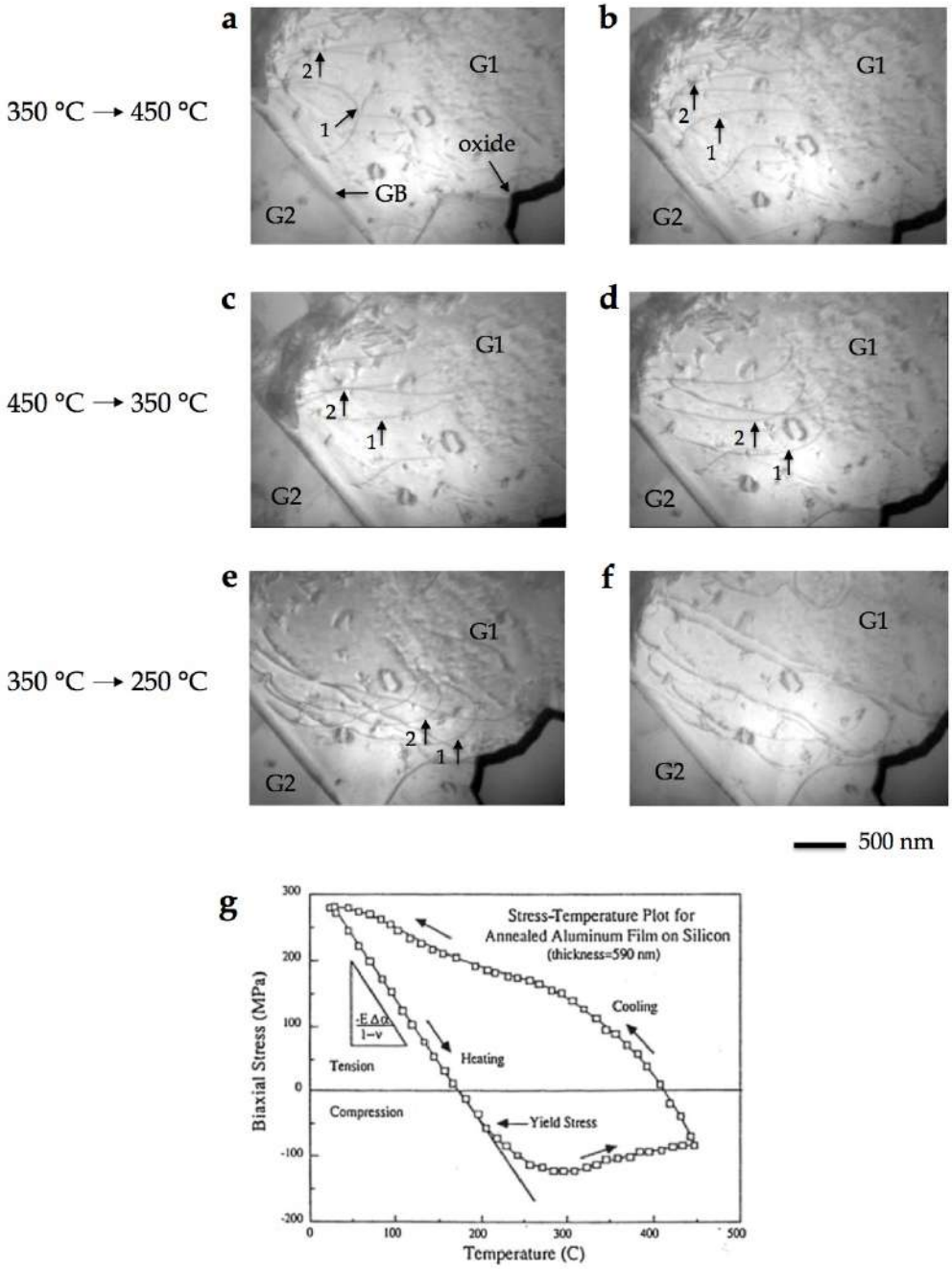

Figure 87: In situ TEM thermal cycling from 25°C to 450°C of a device cross-section prepared by tripod. The Si substrate is preserved, inducing a reversible motion, according to the stress inversion for a Al/Si substrate thin film in the stress-temperature curve [Fli87]. (a)-(b) are snapshots captured during the heating up phase from 350°C to 450 °C, showing the dislocation activation. During the cooling down phase, the reversible motion is characterized by an initial dislocation straightening (c) followed by a bowing in the opposite direction (d), towards the oxide (d)-(e).

4.2 AGING OF T07D17 COMPONENTS

In this Section we present further results of the metal microstructural characterization of LFET1T components. We assess the effects of operational mission profile tests performed on T07D17 components at two different temperatures (25 °C and 70 °C) in the failure analysis laboratories of NXP Semiconductors. On the basis of the preliminary results from SPD06 components that underwent gradual short-circuit conditions (Section 4.1), here we focus on the metallization structure away and under the bonding wire to address two main degradation mechanisms:

- Crack propagation through the Al metallization upon aging.
- Plastic deformation of the initial metallization under the wire due to the bonding process.

We have expanded the microstructural characterizations and the statistical analysis proposed for the SPD06 devices. For the T07D17, we have collected a consistent number of FIB cross-sectional images (15 for each sample instead of 7 as for the SPD06s) to quantify the cracks in the naked metallization and the deformed area under the bonding contacts. Moreover, the preparation by cross-polisher of the wire-metal interface offers us a broader vision, compared to the smaller FIB cuts, of the whole bonding area, down to the Si bulk under the MOSFET region.

From the point of view of the microstructural analysis of the Al parts, TO7D17 power devices differ from SPD06 ones only in the presence of a SiO_2 passivation layer, which covers the source metallization everywhere, except in the bonding areas to allow the electrical contact (Fig. 88a). Fig. 88b shows the metallization surface close to the bonding wire (where the passivation layer is absent) for and as-is module. As for the SPD6 modules, we can distinguish the Al grain structure an the "wave" pattern due to the MOSFET trenches below the metallization.

As expected, we observe at failure a heavy surface reconstruction, with many cracks running along the grain boundaries, for both the 25°C and 70°C tested module (Fig. 89a and b). We have investigated the propagation of these cracks through the metallization thickness, together with the Al grain microstructure. In the following, we present a cross-sectional analysis of the metallization close to the bonding contacts, by a systematic comparison of as-is, 25°C and 70°C aged modules.

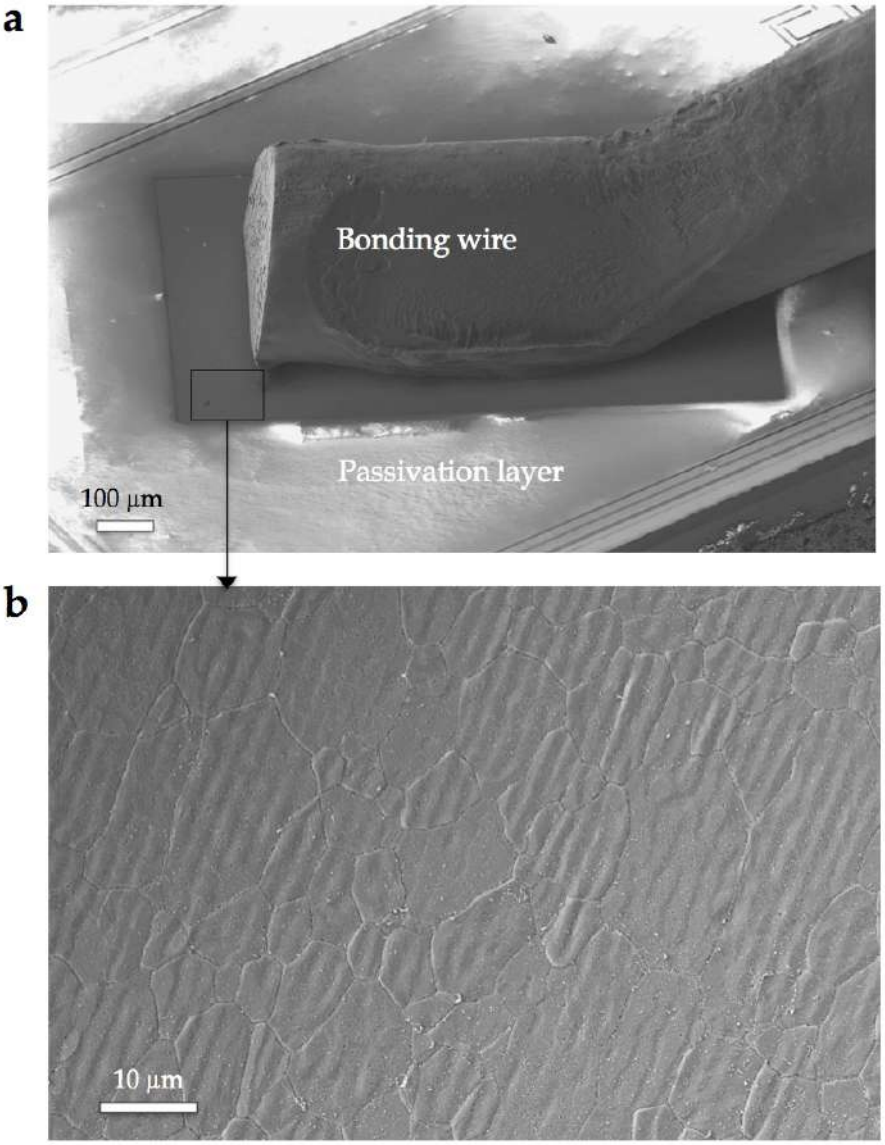

Figure 88: (a) SEM image of an Al bond wire welded on the Al source metallization on an as-is module. Away from the bonding area the metallization is coated by a SiO_2 passivation layer. (b) Higher magnification of the bare metallization close to the bonding wire.

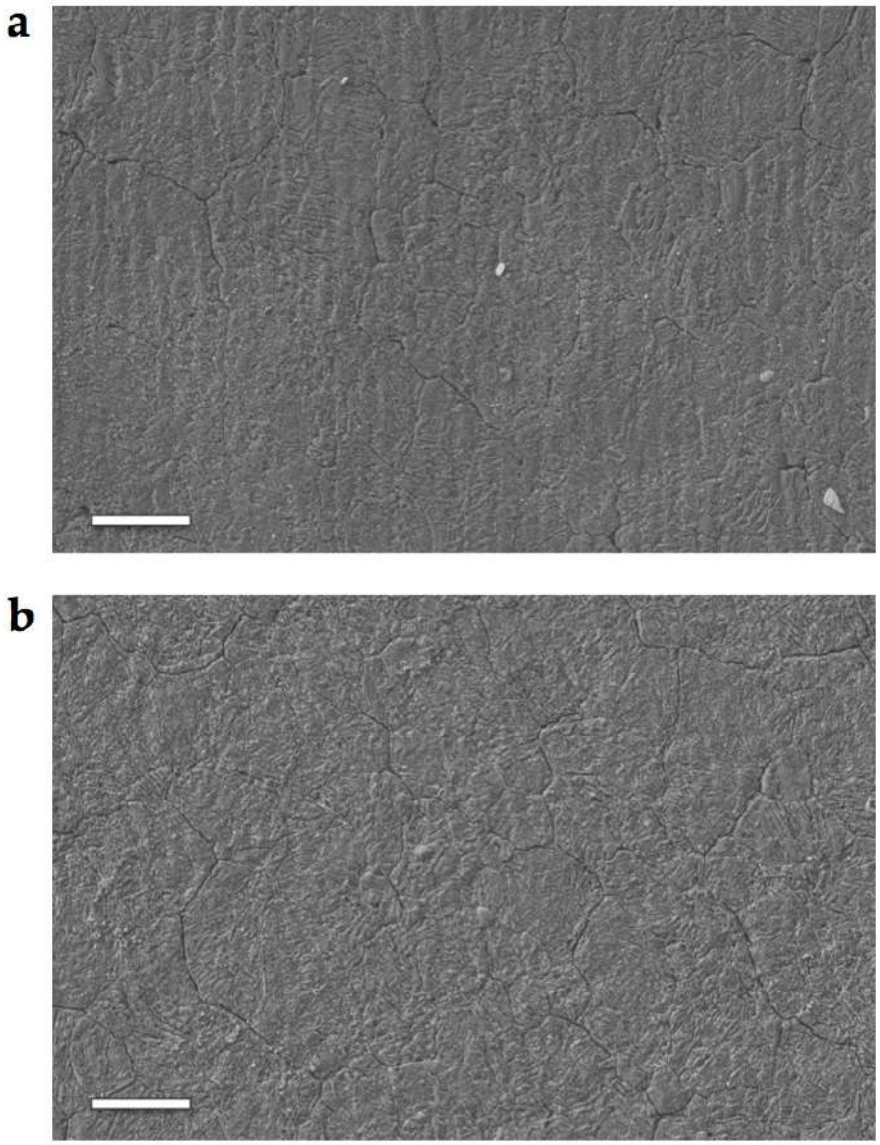

Figure 89: SEM images of the Al metallization close to the bonging wire in a (a) 25°C aged module (failed after 5.3 million cycles) and in a (b) 70°C aged one (failed after 300 kcycles). Scale bar 10 µm

4.2.1 *Naked metallization cross-sectional study*

The structure of the metallization close to the bonding area (without passivation coating) was observed by ion channeling contrast after having made FIB cross-sectional cuts. Fig. 90 shows the comparison between a non-aged module (a) and an aged one at 25°C (b), failed after 5.3 million cycles, and 70°C (c), failed after 300 kcycles. The SIM images reveal a strong degradation upon aging of the initial bamboo structure, with many cavities and cracks running vertically from the surface, following the grain boundaries, and horizontally along the transistor interface. In Fig. 90c one can also notice that the fist transistor from the right is fractured. This could be due to the propagation of the cracks from the metal to the transistor area and then to the semiconductor below.

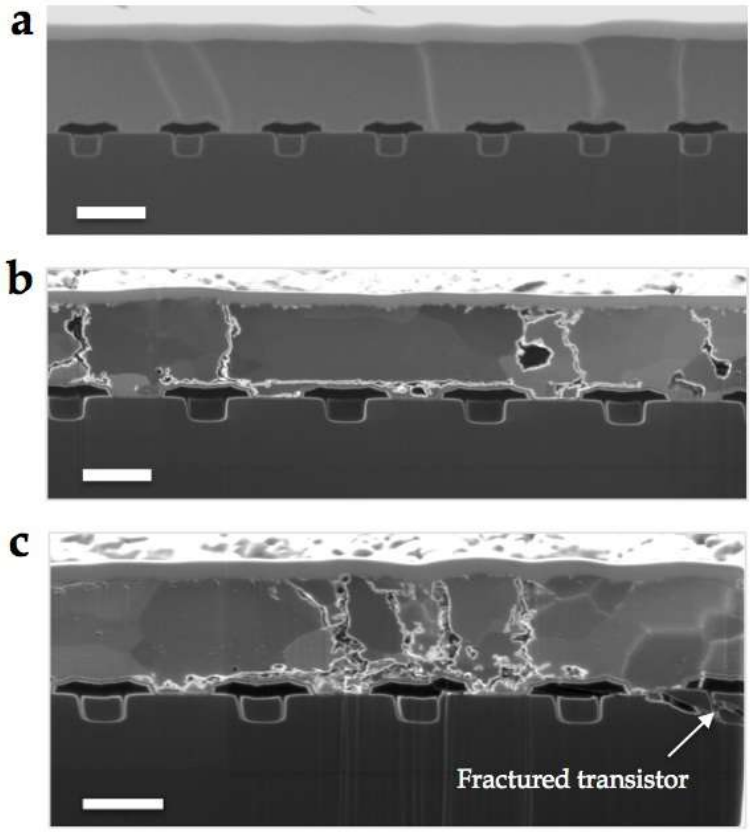

Figure 90: SIM images of the naked metallization cross-sections of (a) as-is, (b) 70°C aged and (c) 25°C aged power modules. The top layer (~ 1µm thick) is the Pt protective coating to prevent curtaining artefacts on the imaging faces. Scale bar 2.5 µm.

Cavities and cracks in the Al top metallization are also visible at higher resolution in the TEM images (Fig. 91) of thin lamella prepared by FIB from a non-aged module (a, b) and an aged one at 25°C (c, d) and 70°C (e, f):

- Fig. 91a shows the columnar grain structure of the as-processed metallization. The dark-contrasted layer on top is the Pt protection used during the lamella preparation. At higher mangification, in Fig. 91b, we can better see small grains between the transistors, formed in the early stage of the Al deposition process, prior the the bamboo grain growth.
- Fig. 91c and Fig. 91d refer to a 25°C aged module. Vertical cracks run from the surface along the grain boundaries and branch off alongside the transistors.
- These cracks are also visible in the metallization of a 70°C aged module. In few rare case, some grain results fractured and the crack (pointed out by the white arrows in Fig. 91e) does not follow the grain boundaries. However most of the cracks follow the grain boundaries (Fig. 91e).

The previous images (Fig. 90, Fig. 91) show also a grain shrinkage upon aging. However, as we also see for the SPD06 components, the orientation mapping by ACOM-TEM system (Fig. 92) reveal that most of the grain domains in the aged metallization (at 25°C in Fig. 92d and 70°C in Fig. 92f) have a small misorientation as they have very similar colors. We reported directly in the figures the misorientations between a few grains. These misorientations are less than 10°. This means that most of the grains with different gray scale colour in the FIB and TEM images are subgrains, probably formed by the gathering of pre-existing dislocations inside a single initially large bamboo grain (Fig. 92b) at the beginning of the electro-thermal cycles [Mar14]. This is clearly visible for the 25°aged module (Fig. 92d), where we can recognize three bamboo domains (the misorientations between them are higher, $\sim 30°$) with vertical cracks along the grain boundaries, and smaller subgrains inside each domain. These images confirm again that cracks propagate along the GBs and not along the sGBs.

We can conclude that during aging no change of the metallization texture occur. In other words, the Al metallization, away from the bonding wire, is not subject to a heavy dislocation-based plastic deformation that could justify the device failure. On the other hand, we have observed a heavy crack propagation along the GBs due to an enhanced intergranular diffusion of Al atoms during aging. This can, for sure, explain a local increase in the metal resistance and temperature that accelerate the aging process until failure. In the next section, we propose a method to quantify these cracks, in order to access the effect of the intergranular Al diffusion both in the naked parts and under the passivation.

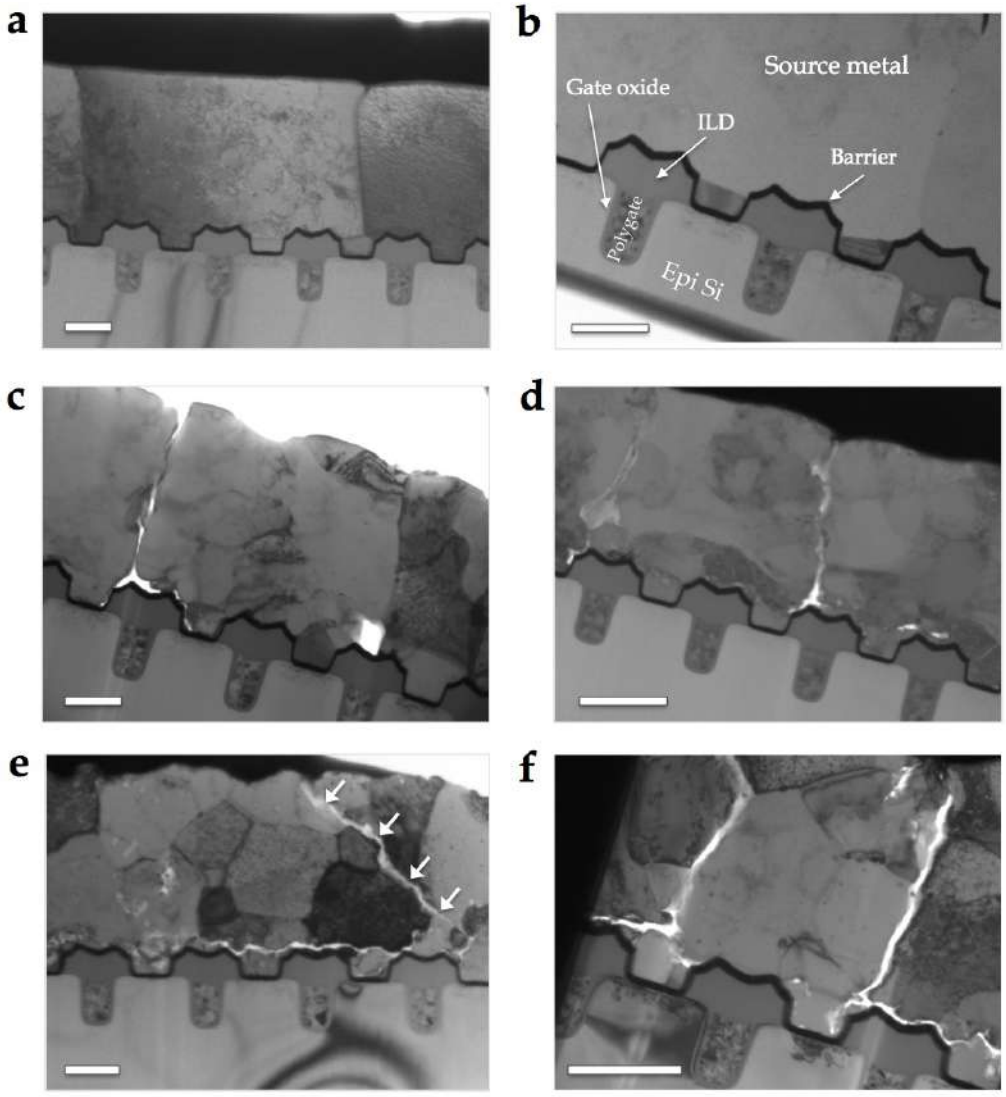

Figure 91: TEM images of some details of the transistor/metallization area from the naked metallization of an (a, b) as-is, (c, d) 25°C aged and (e, f) 70/degree C aged power modules. The trench MOSFET layered structure is described in (b) and consists in: source metal, inter-layer dielectric (ILD), gate oxide and polySi (Polygate), epitaxial Si. Scale bar: 1 μm.

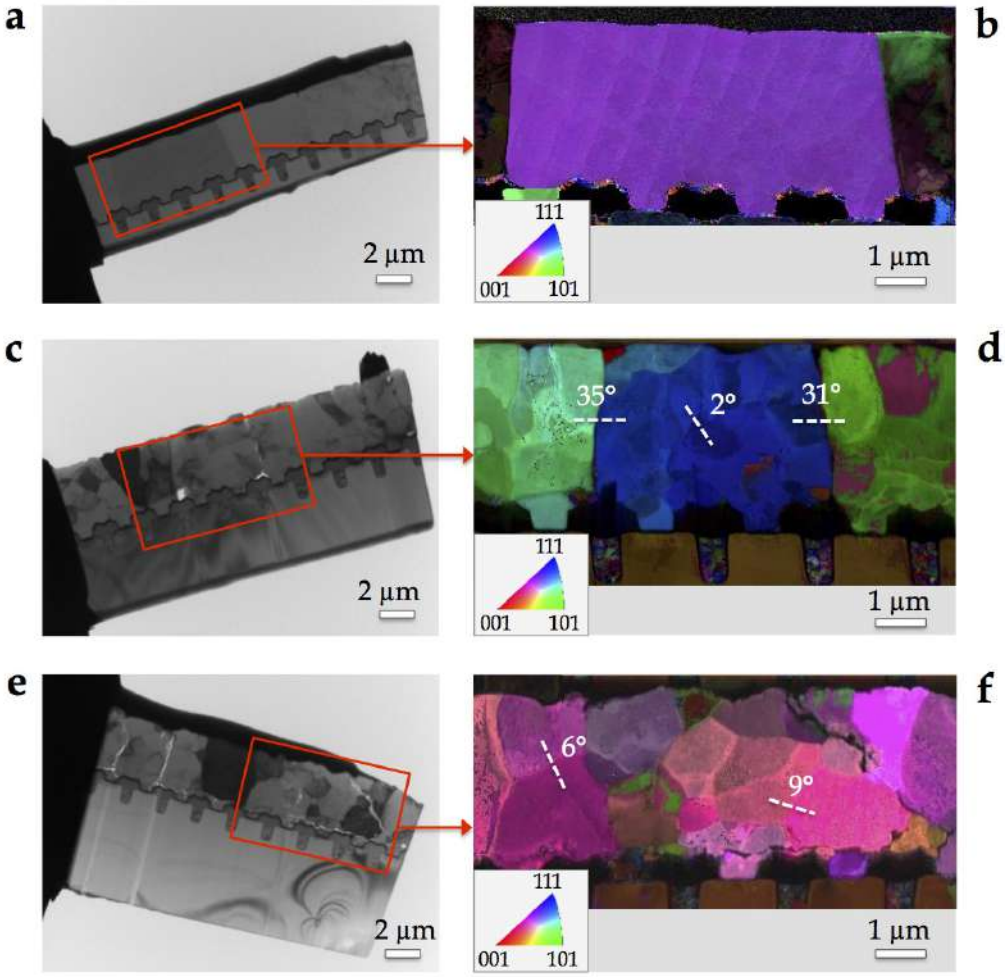

Figure 92: TEM images of FIB lamella extracted from the naked metallization of an (a) as-is, (c) 25°C aged and (d) 70°C aged power modules.
ACOM mapping relative to the red area in the TEM images for the (b) as-is, (d) 25°C aged and (f) 70°C aged lamella. The standard stereographic triangle gives the color codes of the grain orientations, taken here along the horizontal direction, perpendicular to the growth direction, in order to have better visibility (the relative misorientation between subgrains does not change along the three axis).

4.2.1.1 *Cracks propagation statistics*

SIM (Fig. 90) and TEM (Fig. 91) images reveal a heavy fatigue cracking of the Al source metallization of T07D17 modules at failure, both at 25°C and 70°C. The cracks run vertically from the metallization surface down to the Si bulk and horizontally along the transistor area, following the grain boundaries.

We tried to quantify these fatigue cracks in the FIB images of the naked Al metallization, aged at 25°C and 70°C. In order to perform a coherent statistical analysis on the two batch of images (~ 40 for each aging temperature), we had to determine a clear criterion to count the cracks affecting the metallization cross-sections. On the basis of our observations, we defined two different criteria to count vertical and horizontal cracks (Fig. 93a):

1. Vertical cracks.
   Since vertical cracks propagate along the grain boundaries starting from the metal surface, we decided to count the number of grain boundaries (GBs) affected by cracks or cavities at surface. For instance, in Fig. 93a, we can distinguish 8 GB, out of which one (GB_5) is cracked. Then, in this section we count 1 cracked GB and 7 undamaged. An so on for all the images we collected from the naked metallization of 25°C and 70°C aged modules. At the end, we summed up all the cracked GB in the analysed sections and we obtained the ratio of cracked grain boundaries to the undamaged ones. These percentage values are represented in Fig. 93b, for the 25°C aged module and in Fig. 93c, for the 70°C aged one.
   We can conclude that the metallization affected by vertical fissurations in the analyzed sections is 31% in the 25°C aged module and 33% in the 70°C aged one.

2. Horizontal cracks.
   On the other side, horizontal cracks run alongside the transistors, at the interface with the Si bulk. For this reason we decided to count the number of MOSFET units with cracks on top. As depicted in Fig. 93a, a MOSFET unit consists not only in the area upon the transistor itself but also in the adjacent area before the next one. This allowed us not to neglect the case in which the cracks propagate between two transistors. For instance, In Fig. 93a there are 4 MOSFET units, 2 of which are affected by cracks. We summed up the number of cracked MOSFET units in the analyzed sections to obtain the ratio of crack unit to the undamaged ones. These percentage values are represented in Fig. 93d, for the 25°C aged module and in Fig. 93e, for the 70°C aged one.
   The metallization affected by horizontal fissurations in the analyzed sections is 50% in the 25°C aged module and 67% in the 70°C aged one.

If we suppose that fatigue cracking initiates at surface, then we can conclude that vertical crack propagation along the GBs saturates when ~ 30% of the Al metallizatation is fractured in the analyzed sections, for both modules aged at 25°C and 70°C. At this point, cracks start propagating horizontally deep in the source metal, close to the transistor area at the interface with the semiconductor bulk. On the basis of our statistics, the percentage of transistor units affected by cracks is greater in the module aged at higher temperature (67%) than in the module aged at ambient temperature (50%).

4.2.1.2 *Cracks propagation under the passivation layer*

We have also characterized the microstructure of the Al metallization in the aged modules outside the bonding apertures, under the SiO_2 passivation layer. This coating layer is generally used in power devices to prevent reconstruction phenomena during electro-thermal aging.

SIM imaging reveals that the metallization aging is not uniform under the passivation, as we can see in Fig. 94, which represents two close FIB cross-sections from the same 70°C aged module. The metallization portion in Fig. 94a looks similar to an as-is part, with an undamaged columnar grain structure. On the contrary, the close section in Fig. 94b shows clear signs of aging, as for the naked metallization next to the wires (Fig. 90 and Fig. 91), with the formation of subgrains and many cracks running along the grain boundaries from the surface to the MOSFET region.

We have quantified these cracks in the passivated metallization FIB sections (~ 20) from a 25°C and 70°C aged module. We have applied the same method, reported in the previous section (Fig. 93a), to count the cracked GBs and the MOSFETs units. The percentage of passivated metallization affected by vertical and horizontal cracks is reported respectively in Fig. 95a and Fig. 95c for the 25°C aged module and in Fig. 95b and Fig. 95d for the 70°C aged one. The amount of cracked metallization in the analyzed sections under the passivation layer is lower than in the naked metallization (Fig. 93b - b). This confirms that the passivated metallization does not age uniformly: the initial bamboo structure is preserved in some zones, whereas fatigue cracks concentrate in others. If we look at the vertical crack propagation, the ratio of cracked to undamaged metallization is not so different under the passivation layer and in the naked areas close to the bonding wires (25% vs 31% for the 25°C aged module and 20% vs 33% for the 70°C aged module). However, the horizontal propagation of fatigue cracks alongside the transistors is drastically reduced under the passivation (15% for the 25°C aged module and 6% for the 70°C aged one) compared to the values obtained from the naked metallization (50% for the 25°C aged module and 67% for the 70°C aged one).

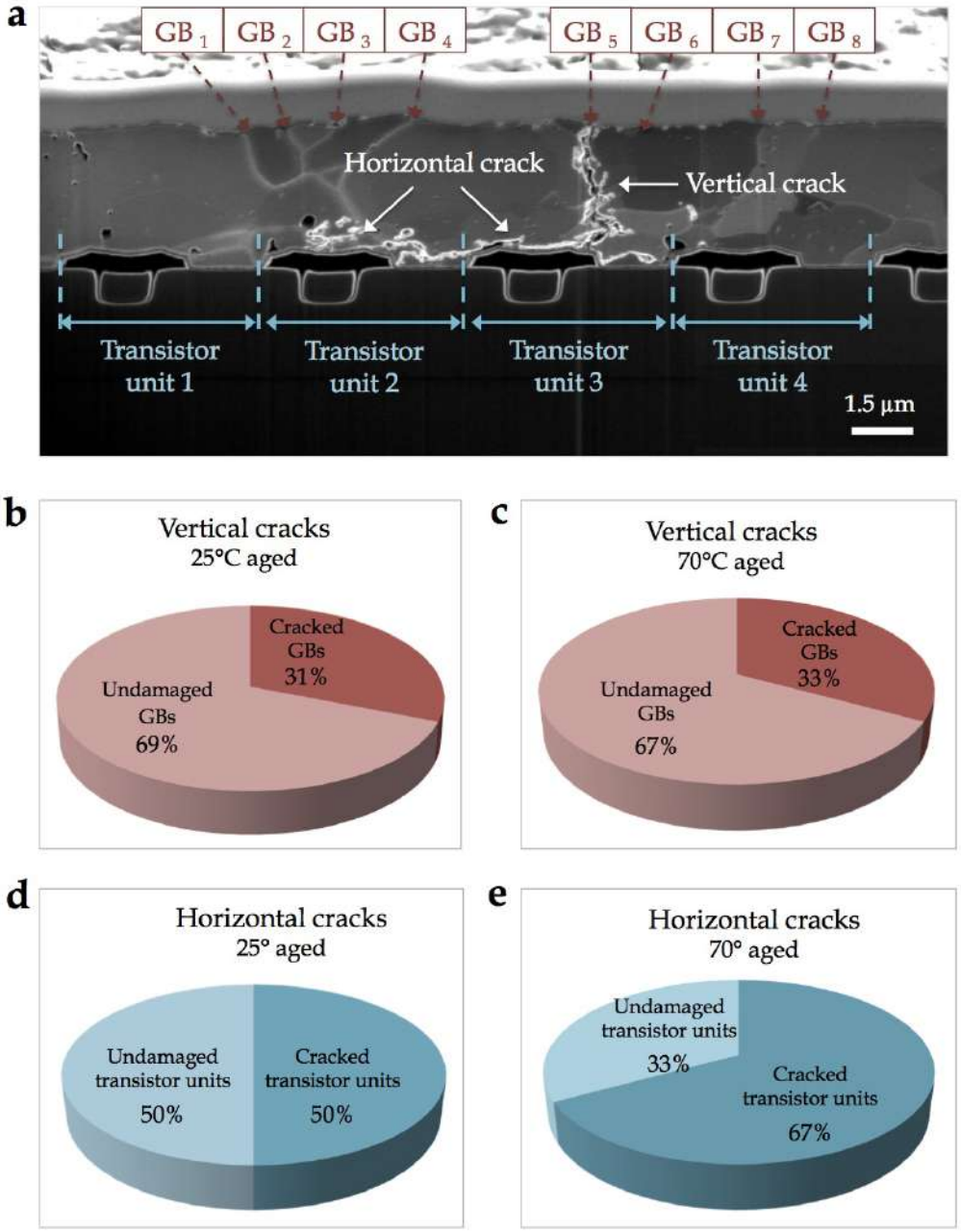

Figure 93: Horizontal and vertical cracks statistics in a 25°C and 70°C aged module. (a) Vertical cracks are evaluated by counting at the metal surface the number of cracked (GB_5) and undamaged ($GB_1 - GB_4$ and $GB_6 - GB_8$) grain boundaries . Horizontal cracks are evaluated by counting the number of transistor units with cracks on top (Transistor unit 2 and Transistor unit 3) with respect to the undamaged ones (Transistor unit 1 and Transistor unit 4).
The ratio of cracked vs undamaged GBs is showed in (b) for a 25°C aged module and in (c) for a 70 °C aged one.
The ratio of cracked vs undamaged transistor units is showed in (d) for a 25°C aged module and in (e) for a 70 °C aged one.

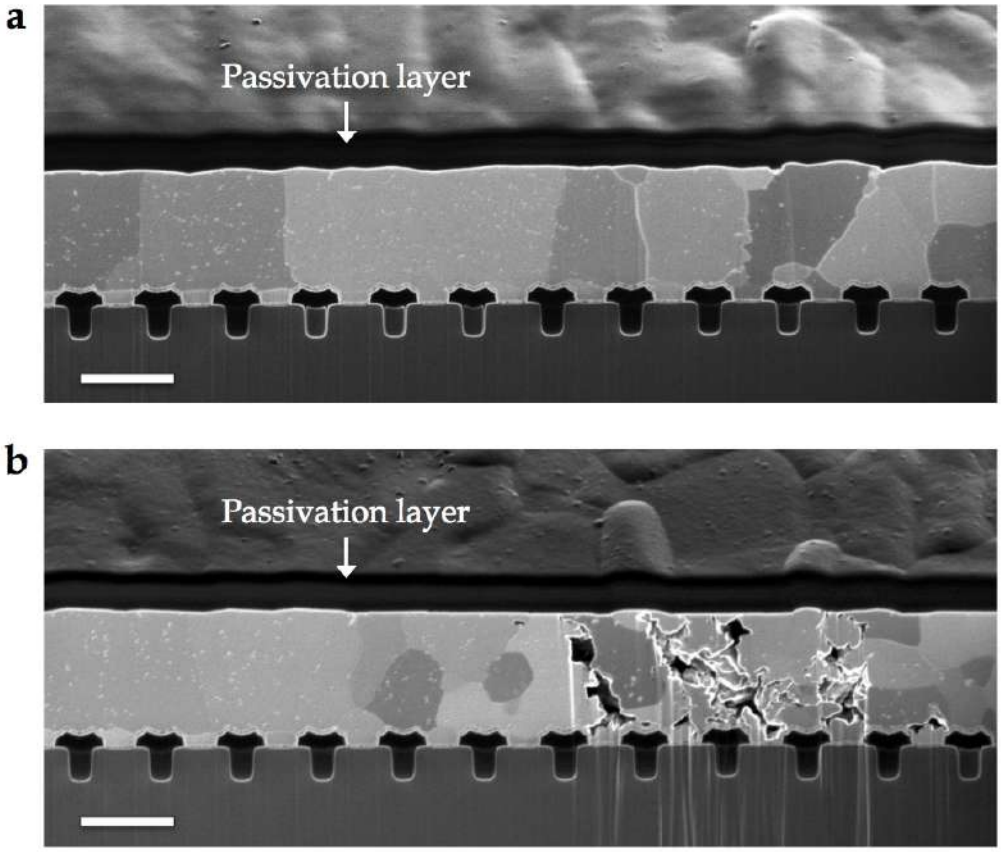

Figure 94: SIM image of the Al top metallization coated by SiO_2 passivation from two close cross-sections in a 70°C aged module.

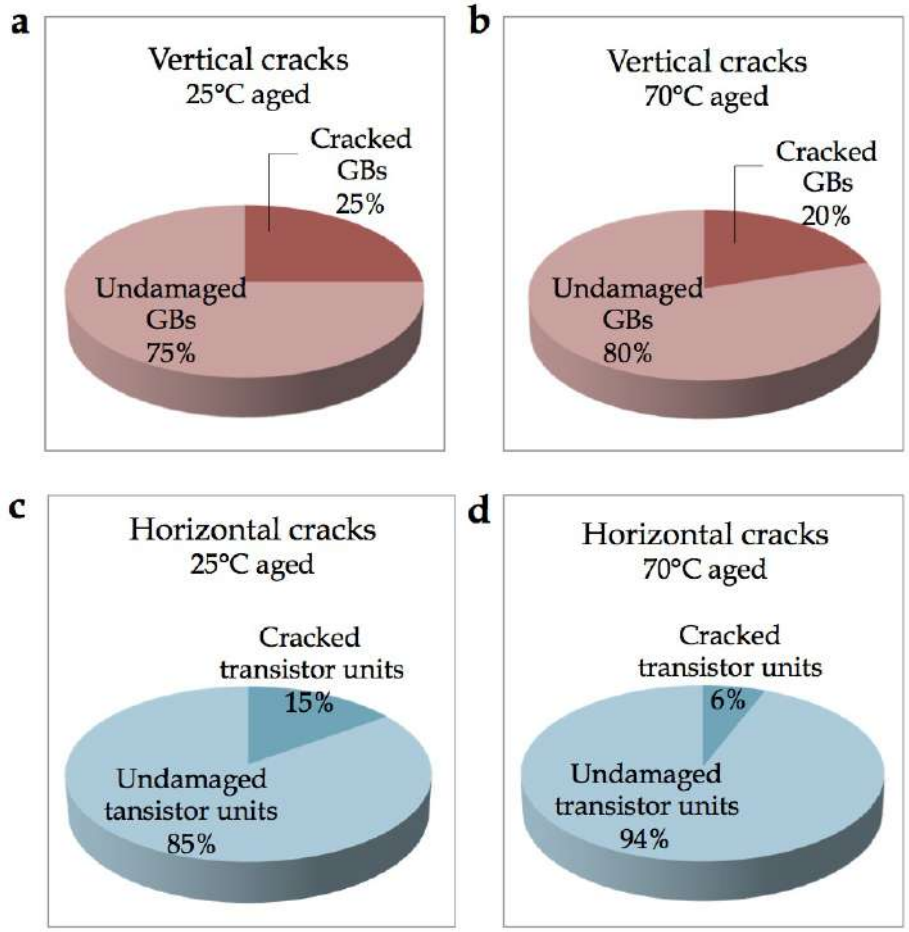

Figure 95: Ratio of cracked vs undamaged GBs in (a) a 25°C aged module and in a (b) 70 °C aged one.
Ratio of cracked versus undamaged transistor units in (c) a 25°C aged module and in a (d) 70 °C aged one.

4.2.2 *Metallization under the bonding wire*

Under the bonding wire we find again that the bonding process causes plastic deformation of the Al metallization prior to aging. Fig. 96 shows a FIB cross-section of the metallization under the wire in an as-si module. Here the initial grain size seems systematically smaller compared to the bamboo structure of the naked metallization prior to aging (Fig. 90a).

To confirm the apparent grain reduction under the wire bond observed in ionic contrast, we have also performed ACOM mapping on a TEM lamella from the interface region (Fig. 97a). As expected, the grains in the bonding Al wire are much larger and the plastic deformation of the interface is highly uneven. The grain size reduction in the metallization is here appending with a real grain reorientation, as exemplified by the large grain boundaries that are created under the wire. In Fig. 97b the misorientation between grain 1 and grain 2 is above 30°.

The metal microstructure and the uneven wire-metallization profile do not significantly change at failure, as we can see in Fig. 98a and Fig. 98c, which refer respectively to a 25°C and a 70°C aged metallization taken at the center of the bonding contact. However, as for the aged naked metallization, many cracks run from the metallization surface to the transistor area following the grain boundaries. This has been particularly observed when the wire-metallization contact is not tight, closer to the edge of the bonding interface (Fig. 98b, from a 25°C aged module and Fig. 98d for a 70°C aged one).

In the following, we focus first on the wire-metallization interface imperfections and then we quantify the plastic deformation in the metallization layer.

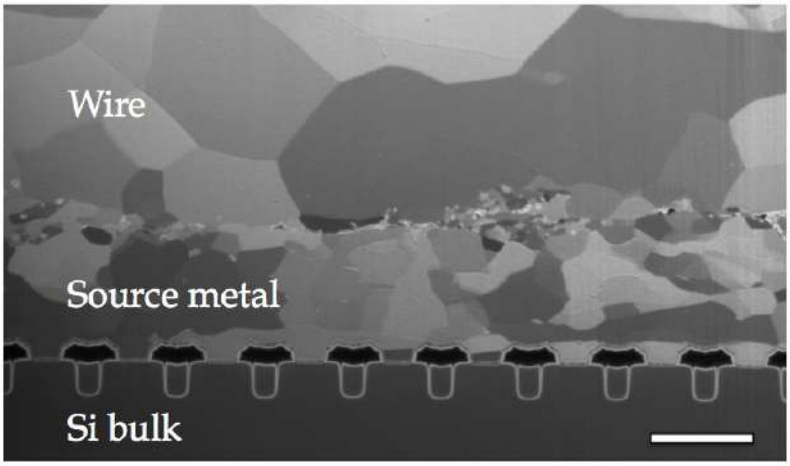

Figure 96: SIM images of the wire-source metallization interface, at the center of the bonding wire, in an as-processed module. Scale bar 2.5 µm.

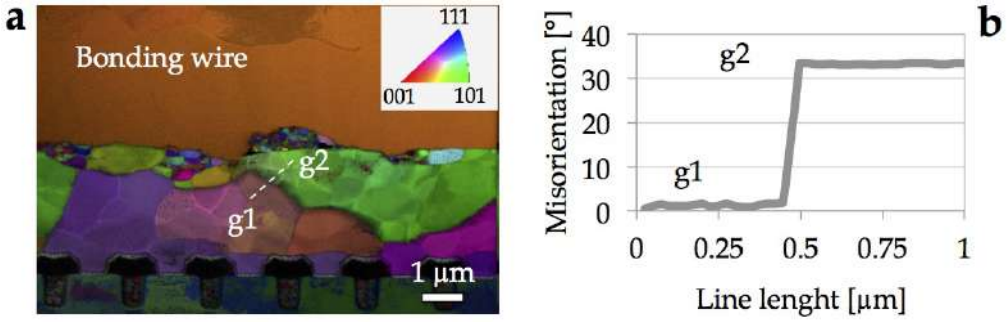

Figure 97: (a) ACOM map of the wire-metal interface of an as-processed module. (b) Misorientation between the grains 1 and 2 along the white dashed line respectively in (a). The standard stereographic triangle gives the color codes of the grain orientations, taken here along the horizontal direction.

4.2.2.1 *Wire-metallization interface*

The bonding between the metallization and the wire is characterized by small cavities and initial imperfections, visible in white contrast in Fig. 99a. This white contrast suggests that the material is very different. In order to analyze the chemical composition of these imperfections, we have prepared thin lamella from the wire-metal interface area and we inspect them in a TEM equipped with an EELS detector. Fig. 99b shows the EELS spectra from the wire (in blue), the metallization (in green) and the wire-metallization interface (in red). The spectrum at the wire-metallization interface reveals the presence of oxygen, proving that the initial imperfections are linked to the presence of Al oxide. The most probable explanation for this presence is that the native oxide is not fully broken during the bonding process.

During aging, cracks can propagate along these imperfections, causing a reduced contact between the wire and the metallization or, at worst, the wire lift-off. Cracks also run perpendicularly to the interface under the wires, as in the metallization away form the bonding area.

Crack propagation upon aging has been investigated by FIB-tomography experiments. In Fig. 100, a series of six (non consecutive) SEM images from the wire-metallization interface of a 70°C aged module are showed. In the analyzed area, the contact between the wire and the metallization is severely affected by the electro-thermal aging (image 1). A measure of the horizontal delamination surface using the complete stack of tomographic SEM sections leads to a delamination ratio of 78% over the tested volume. If we assume that about 33% of the wire was attached to the metallization (see Section 4.1.2.2), then the delamination affected another 10% of the expected contact during aging. Of course, the volume tested by FIB is too small to make robust statis-

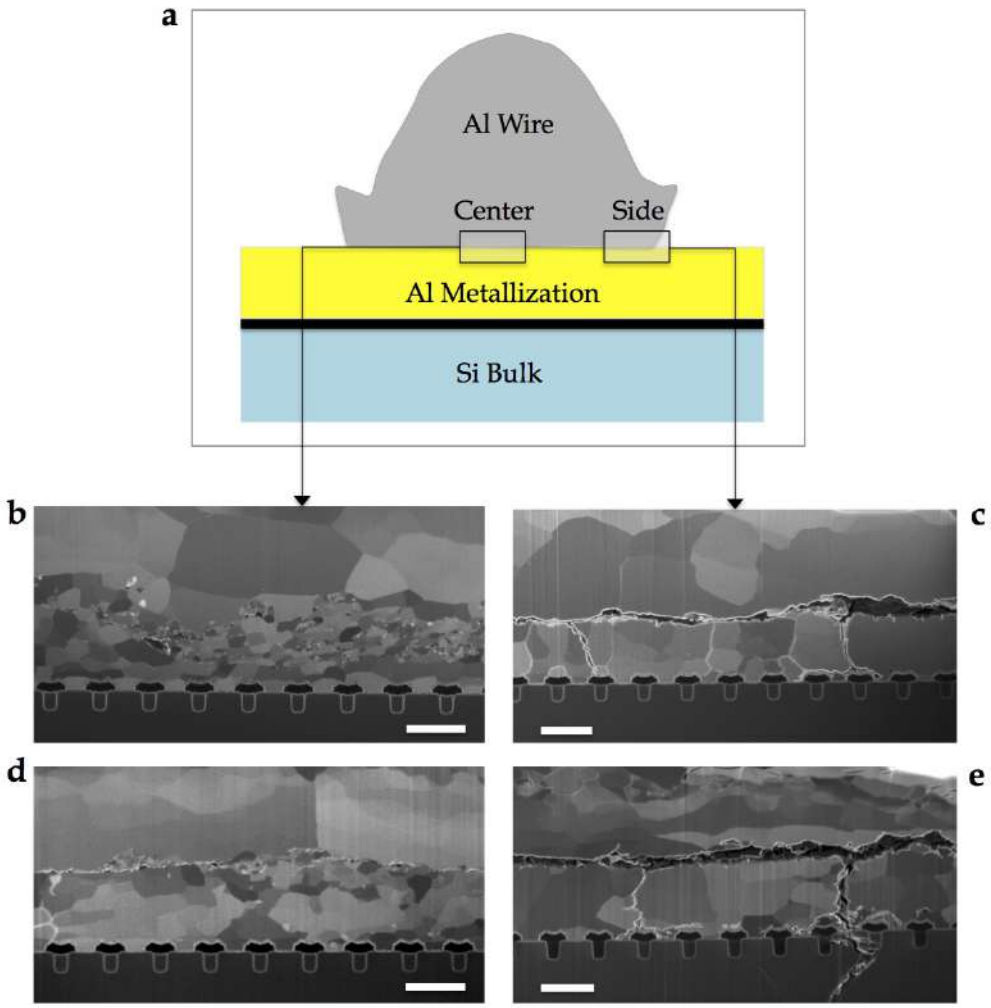

Figure 98: (b) Central and (c) side SIM images of the wire-metallization interface in a 25°C aged module. (d) Central and (e) side SIM images of the wire-metallization interface in a 70°C aged module. The images correspond to the FIB cross-section locations ("center" and "side") in the schema in (a). Scale bar 2.5 µm.

tics, but we have gathered convergent observations showing that a significant delamination occurs between the wire and the metallzation it is attached to. Going through the metallization volume, one can note some cavities appear (image 43) and subsequently constitute a single crack running from the bond interface to the transistor area (image 228). This crack splits in two new cracks (images 135 and 166) that propagate in the Al metallization (image 176). As demonstrated in Fig. 98, the same mechanisms are observed in devices tested at 25°C and 70°, but at different number of cycles. Temperature is therefore accelerating mechanisms that are the same in both cases.

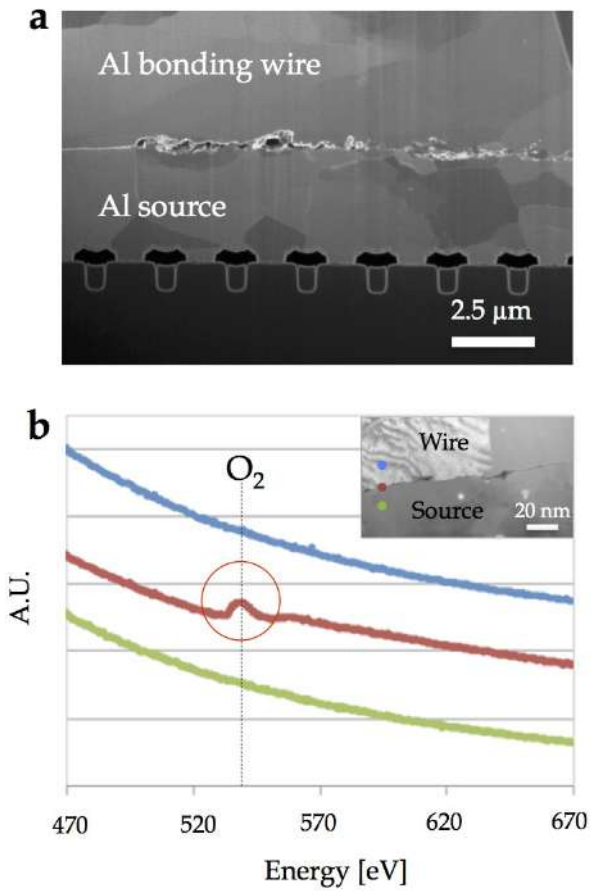

Figure 99: (a) SIM image of the initial artifacts which characterize the wire-metallization bonding of an as-is module. (b) EELS spectra from the wire (in blue), the metallization (in green) and the wire-metallization interface (in red). The red spectrum at the wire-metallization interface reveals the presence of oxygen.

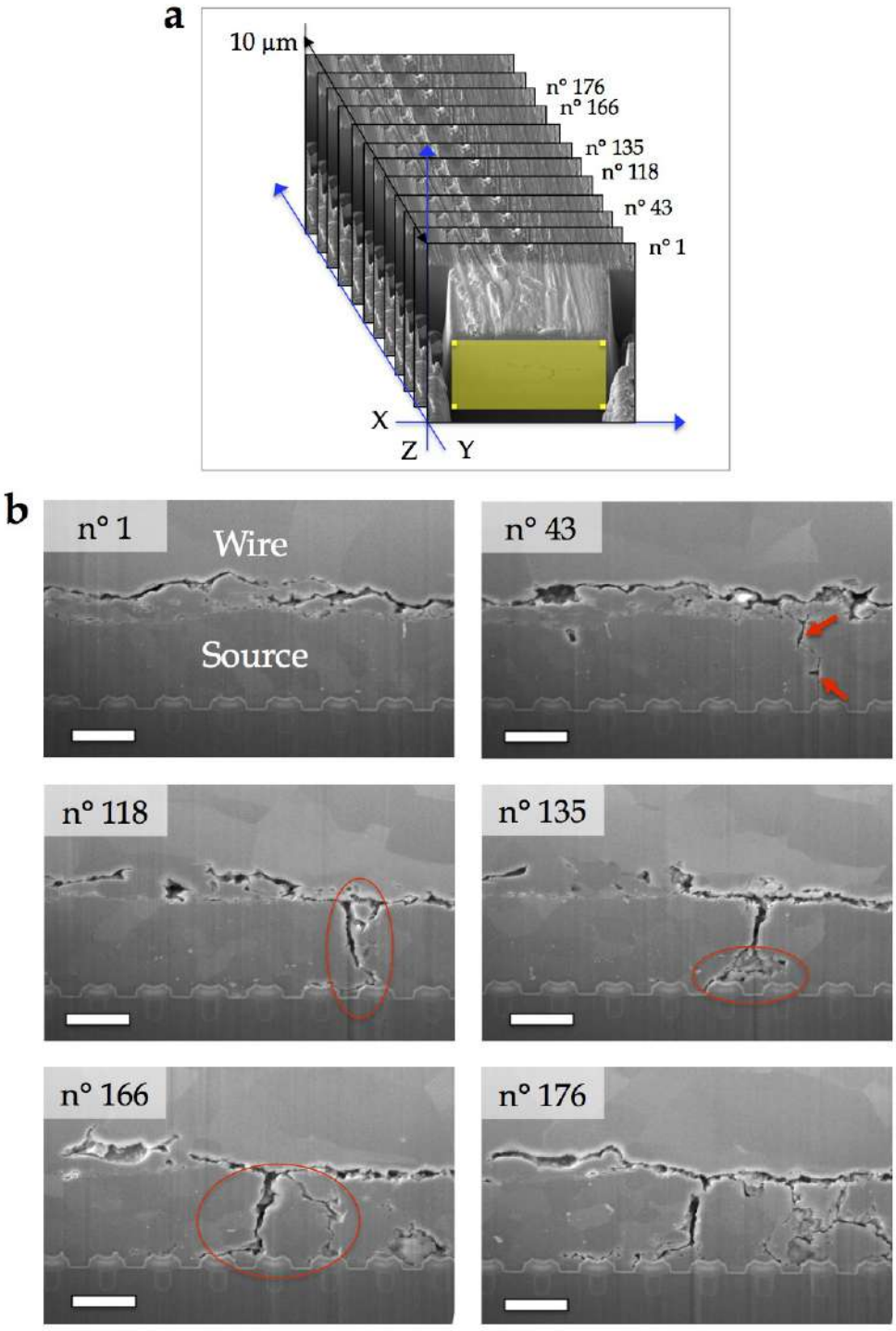

Figure 100: (b) Selection of six non consecutive SEM images from the data stack of the wire-metallization interface (according to the schema in (a)) of a 70 °C aged device (slicing distance 50 nm). The yellow rectangle in (a) represents the milled imaging face. Scale bar 2.5 µm.

4.2.2.2 *Plastic deformation due to the bonding process - Statistics*

We have also assessed the uneven plastic deformation along the applied stress of the wire bonding, that is perpendicular to the wire-metallization interface. We developed and used two different methods to quantify the deformation metallization under the wire:

1. Minimum thickness based statistics.
   In Section 4.1.2.2 we locally measured the deformation in as-is and aged SPD06 modules as the minimum metallization thickness in the analyzed sections, by taking the initial metallization thickness away from the bonding wire (in a non-aged device) as reference. We did the same for T07D17 power devices aged at 25°C and 70°C, increasing the number of analyzed sections (~ 15 for each T07D17 module, ~ 7 for each SPD06 module), in order to have a more consistent statistics.
   Fig. 101 shows the mean deformation percentages in a 25°C and 70°C aged module, and in the relative as-is parts. Here, we found out that plastic deformation ranges between 21% and 12% in average in the measured sections. This range is narrower than the one obtained for the SPD06 devices (Fig. 85), probably due to the fact that we measure a higher number of T07D17 sections. However, the standard deviation of the sets of values is comparable, or even higher, compared to the SPD06 data sets, confirming that the wire-metallization interface is highly uneven.

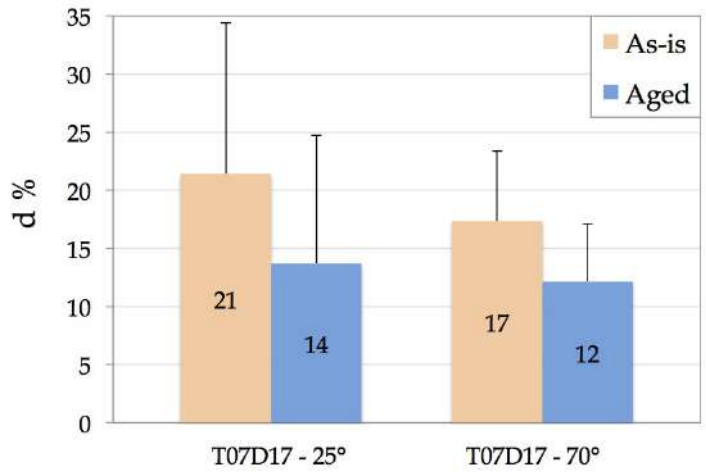

Figure 101: Plastic deformation of the Al metallization under the bonding wires of the as-is and aged modules in a 25°C and 70°C aged device. The deformation has been calculated as the minimum metallization thickness in the wire-metallization FIB section, taking the initial metallization thickness (away from the bonding wire) as a reference.

2. Deformed area based statistics.
   The previous method takes into account only the metallization parts in compression under the bonding wire, measuring the metallization thickness minimum value respect to the reference thickness (measured away from the bonding wire). However, under the bonding we can observe the succession of compression and extrusion parts, corresponding to the zones where the metallization thickness is lower and higher than the reference thickness (102 and Fig. 103). This second method, illustrated in Fig. 102, has been developed in order to considered both parts. The deformation is measured with respect to a reference that corresponds to the initial position of the metallization free surface (red line) by computing the metallization areas under (zones -) and over (-zones +) this reference. The deformation is then calculated as follows:

$$\text{Deformed Area Ratio} = \frac{\text{Area}_{def}}{\text{Area}_{ref}} \tag{7}$$

where:

$$\text{Area}_{def} = \sum_i A_i \tag{8}$$

$$\text{Area}_{ref} = l_{cut} * h_{ref} \tag{9}$$

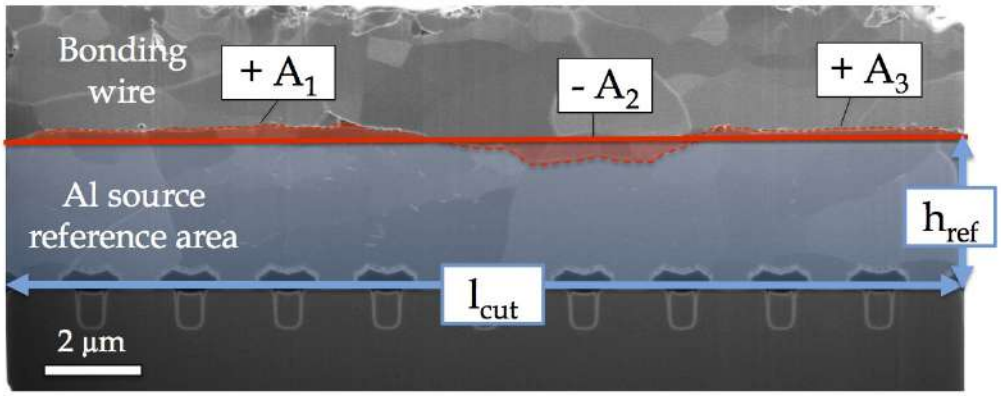

Figure 102: Schematic illustration of the area-based measurement method of the plastic deformation imposed to the Al source metallization by the bonding process. h_{ref} = initial metallization thickness, h_{ref} = image width.

The method takes in account the fact that the initial deformation is not uniform along the wire-metallization interface, that the interface is not straight, and that both extrusion and compression of the metallization occur during the bonding process. This is clearly seen in Fig. 103, showing

two closed cross-sections of the Al metallization under the same bonding wire: in Fig. 103a the wire-metal interface is almost straight without deformation, whereas in Fig. 103b a severe plastic deformation significantly changes the interface profile, provoking a thinning of the metallization on the sides of the micrograph and a bulging in the middle.
As plotted in Fig. 104, the deformation ranges from a minimum value of -0.4% (the - sign indicates that the extruded parts dominate in this section) to a maximum of +36% (the + sign indicates that the compressed parts dominate in this section) in average in the measured sections ($\sim$ 10 for each module, equivalent to Fig. 102). The images corresponding to these two peak values are shown in Fig. 103. This wide range is in agreement with the results obtained with the previous method.

The wide deformation ranges obtained with the two proposed methods confirm that the wire-metal interface is highly uneven in the measured sections and that the plastic deformation is also very non uniform. But they also prove that these measurements strongly depend on the location of the sections along the bonding interface. However, FIB preparation does not allow to cut the entire bonding area, and so measuring the total deformation in the whole cross-section was impossible until recently.

In the following, we proposed an alternative cross-sectional preparation, using the JEOL Cross-Polisher system, that allowed us to cut and visualize the whole wire-metallization interface without introducing additional deformation, which was the initial challenge that we had to overcome.

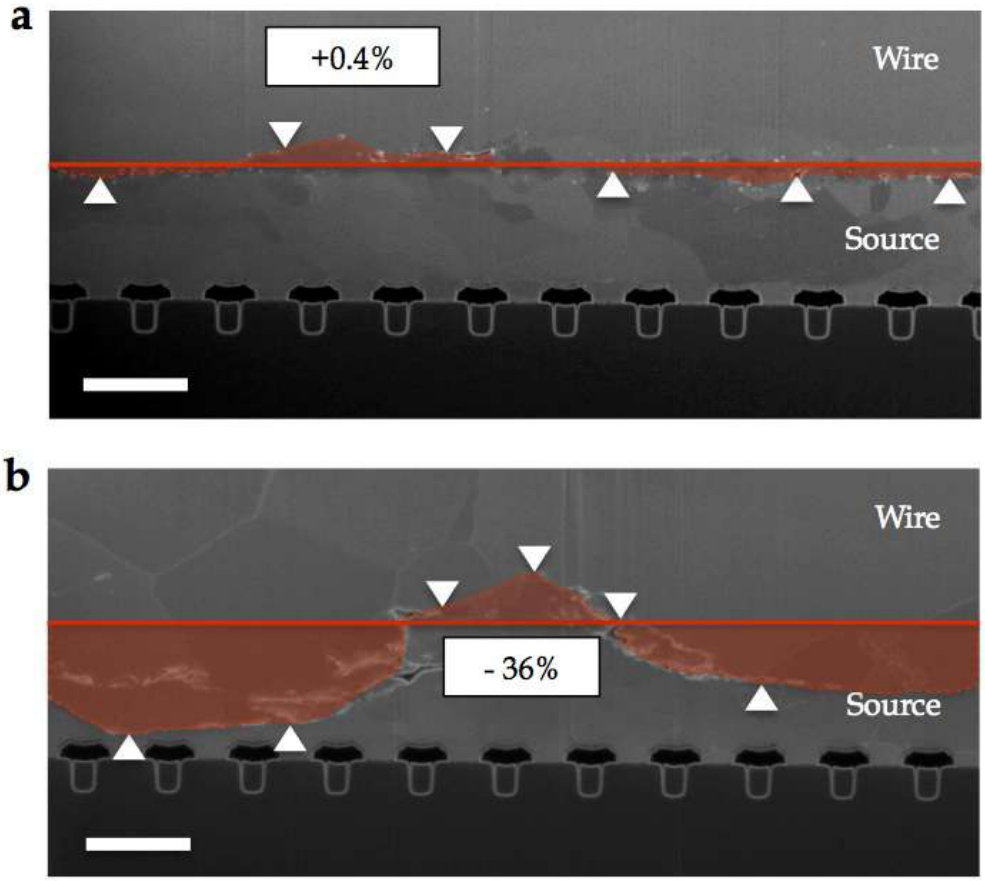

Figure 103: SIM images of the wire-metallization interface in two close areas under the same bonding wire. The images refer to a non-aged module. The red straight line represents the initial metallization surface. White arrows show how the interface moved from this initial position after wire bonding. Scale bar 2.5 μm.

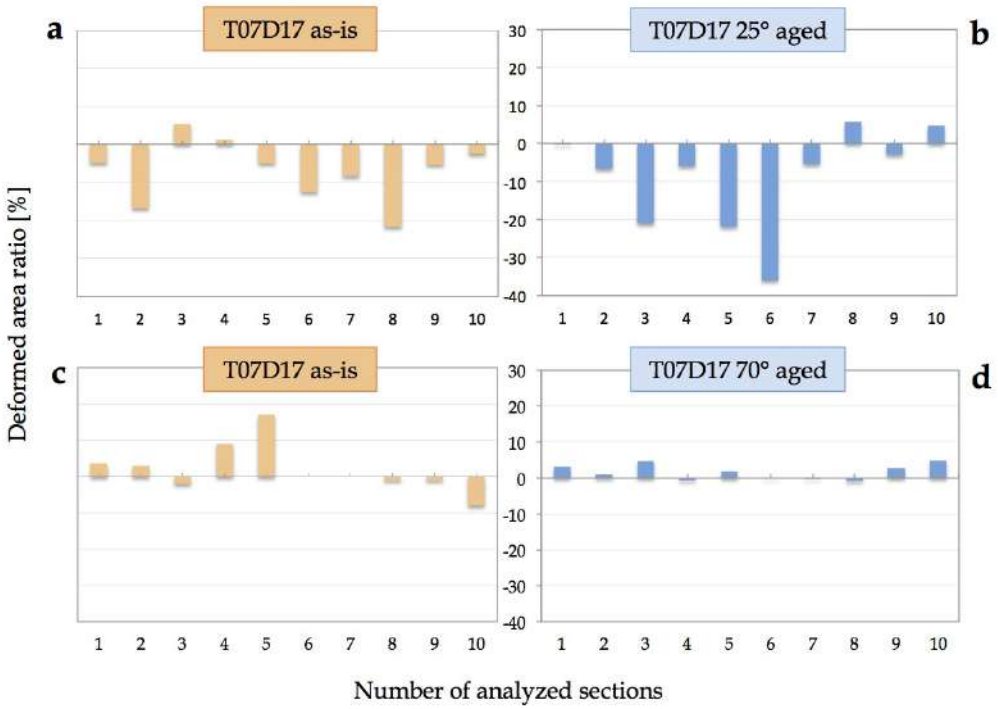

Figure 104: Deformed area ratio of the Al metallization under the bonding wires of a module aged at 25°C (b), with the relative as-is part (a), and of a 70°C aged module (d), with the relative as-is part (c).
The deformation has been measured in 10 sections for each analysed module according to the method represented in Fig. 102.

4.2.3 *In depth investigation of the whole wire-metallization interface by Cross Polisher preparation*

Up to now we have focused on local studies that do not allow to observe the degradation phenomena occurring at larger scale. The study showed in this section, instead, focuses on a lager field of view and allow us to address these phenomena. FIB cross-sections of the Al source metallization of T07D17 modules limit the microstructural investigation to a few tens of micrometers wide areas and few micrometers deep in the Si bulk, below the interface with the MOSFETs. This forced us to perform several time-consuming cuts in the as-is and aged module, both away and under the bonding wires, in order to collect a sufficient number of SEM and SIM images for a thorough study. However, as shown in the previous paragraphs where statistics where sometimes limited, we felt the need of a larger field of view:

- The measurements of plastic deformation proposed in the previous section (4.2.2.2) are based on local methods. Hence, the obtained deformation values are strictly dependent on the location of the analyzed cross-sections along the bonding interface. The cut of the whole wire-metallization interface could allow us to compute the total deformed area under the wire in the analyzed section.

- A few SIM images of the aged metallization away and under the wires (Fig. 90c and Fig. 98d) showed the propagation of fatigue cracks from the Al to the Si bulk, through the MOSFET area. A deeper cross-sectional cut could allow us to follow these cracks in the semiconductor and investigate their extension.

- In many cases, the region of the device where failure arises is easily recognizable. For instance, in the power module of Fig. 105a (aged at 25°C) we can observe the local melting of the bonding wire with a severe cracking of the bonded metallization (Fig. 105b) and of the passivated area around it (Fig. 105c). When we looked at the inner metallization below these zones, by FIB cross-sectional cuts, we observed a generalized crack propagation, not only in the Al top metal but also in the Si bulk. This is visible in (Fig. 106a), under the passivated metallization, and in (Fig. 106b, 106c), under the naked metallization closer to the wire. It is not easy to determine the origin of these cracks, if they propagate from the semiconductor to the metal surface or the other way around. A wider inspection of the device layered structure below the failed bonding wire could help us to investigate these failure mechanisms.

Here we try to address these points, showing the results of the preparation by the CP system, which allowed us to section $\sim 1mm * 1mm$ bonding areas of T07D17 devices, to be imaged by electron and ion contrast.

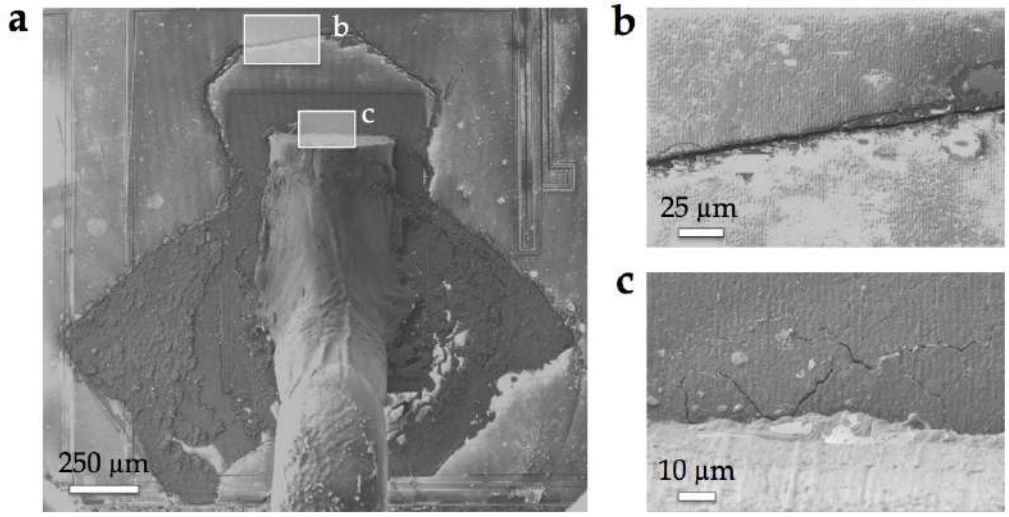

Figure 105: (a) Top view SEM image of an Al bond wire welded on the Al source metallization in a 25°C aged device, after a short-circuit event. At higher magnification, big cracks propagating in (b) the passivated metallization and (c) next to the bonding wire (located in the boxes (b) and (c) in (a)).

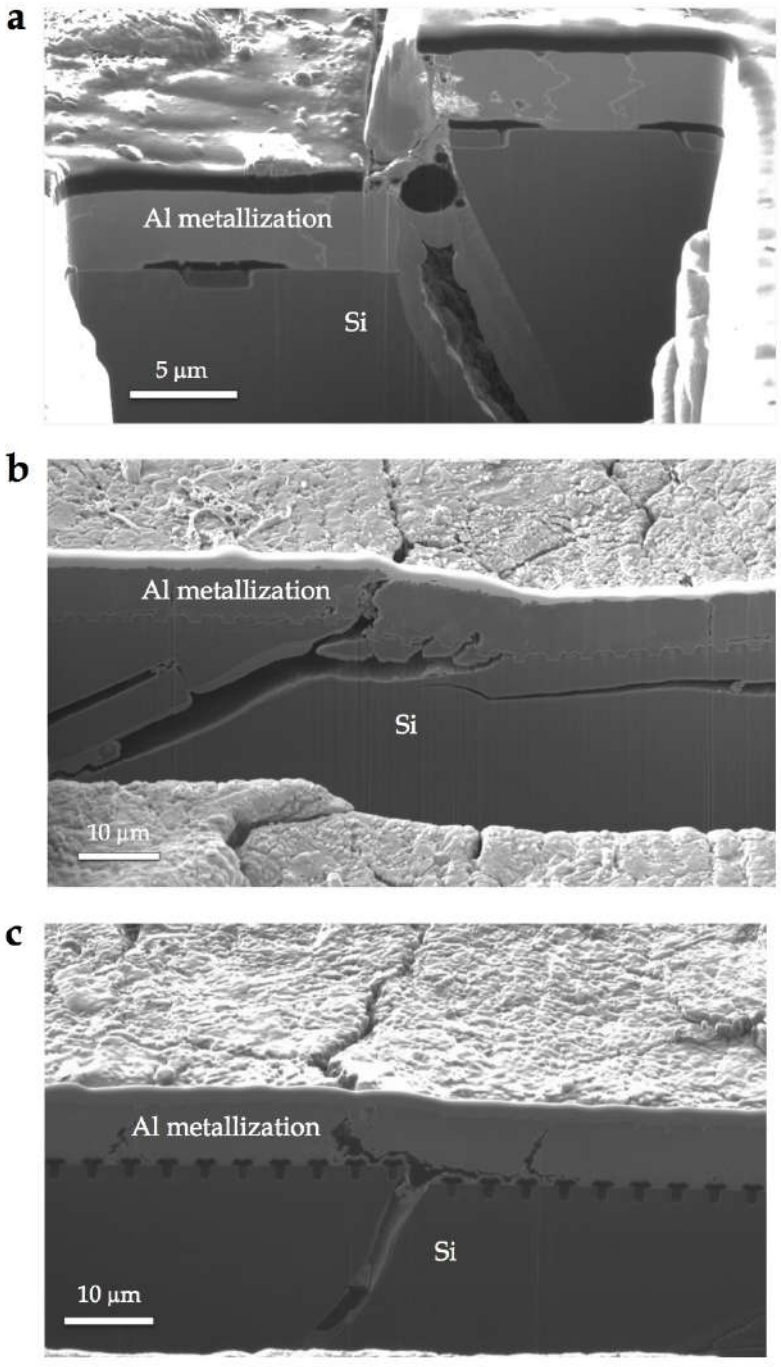

Figure 106: Cross-sectional SEM images of the heavily cracked metallization (a) in the passivated area and (b) close to the melted bonding wire of the module depicted in (Fig. 105a).

4.2.3.1 *Plastic deformation of the initial metallization under the bonding wire*

In the SEM micrograph of Fig. 107 we can see the overview of a cross-section prepared by CP from an as-is module. It includes the Al bonding wire and the Si bulk, attached to the Cu heat sink below. The Al source metallization on the transistor area, at interface with the semiconductor, together with the wire-metallization interface, are not visible at this magnification. The red area indicates the location of the interface between the Al wire and metallization that is depicted at higher magnification in Fig. 108b. We have collected a mosaic of 12 consecutive SIM images (according to the schema in Fig. 108a) to reconstruct the entire bonding area at a resolution good enough to distinguish the grain Al microstructure of the two metallic parts and their interface. Below the metallization we can also notice the transistor units at the interface with the Si bulk.

We used these images to measure the total deformation in the initial Al metallization due to the bonding process. We applied the second method explained in Section 4.2.2.2, based on the measurement of the metallization areas under and over a reference corresponding to the initial position of the metallization free surface. If we sum up the absolute values of the compression and extrusion areas under the bonding wire, then we obtained a total plastic deformation of 4.9% in the analyzed section. This value is confirmed for other bonding areas: in the relative aged module of the same device, for instance, we found out a plastic deformation of 5.2%.

The ion contrast images of Fig. 108 gave us also a visual idea of the granular Al structure, both in the wire and in the metallization. As previously observed in the FIB sections and confirmed by ACOM mapping (Fig. 96, 97a, 98), the grains size in the wire is generally larger than in the Al metallization. We can also observe that the grain refinement in the source metallization is not uniform along the bonding area. In some zones, we can notice some columnar larger grain (as in Fig. 108l). This is particularly true at the extremity of the bonding (Fig. 108n), where the two metallic parts are not in contact. Moreover, the Al-Al interface is more uneven in some parts (Fig. 108e, g) than in others (Fig. 108l), which are more straight. This confirms the results of the local investigation by FIB cuts in the previous section (4.2.2.2), that plastic deformation is not uniform in the metallization under the bonding wires.

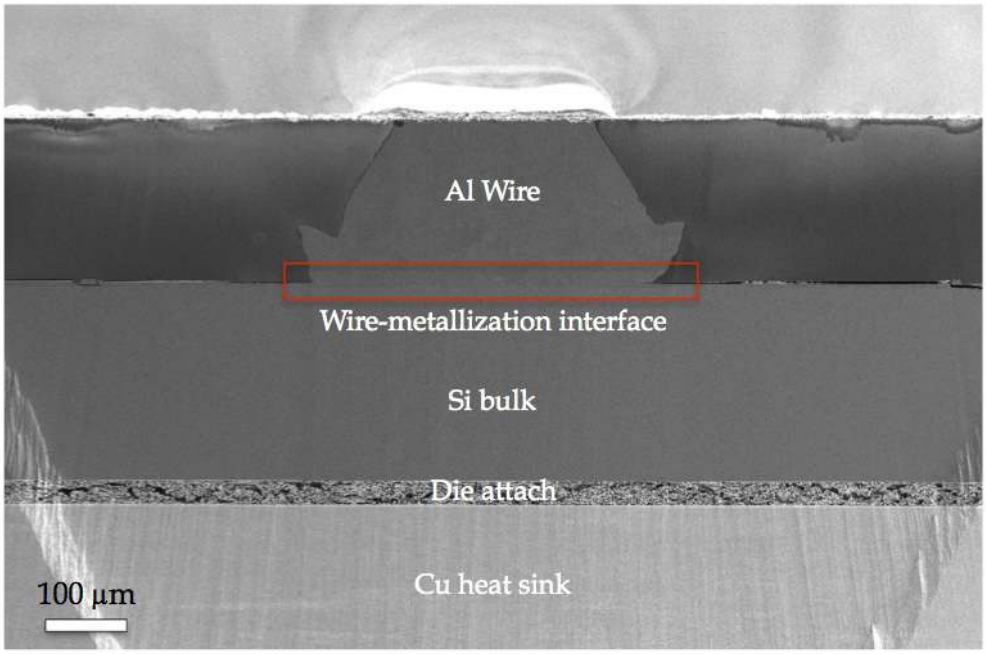

Figure 107: SEM image of a cross-section prepared by Cross Polisher system in an as-is module. The large cut area shows the power die layered structure: Al wire, Si bulk and Cu heat sink. The Al source metallization on the transistor area, at interface with the semiconductor, is not visible at this scale. The red area indicates the location of the Al wire-metallization interface that is shown in detail in Fig. 108a - n.

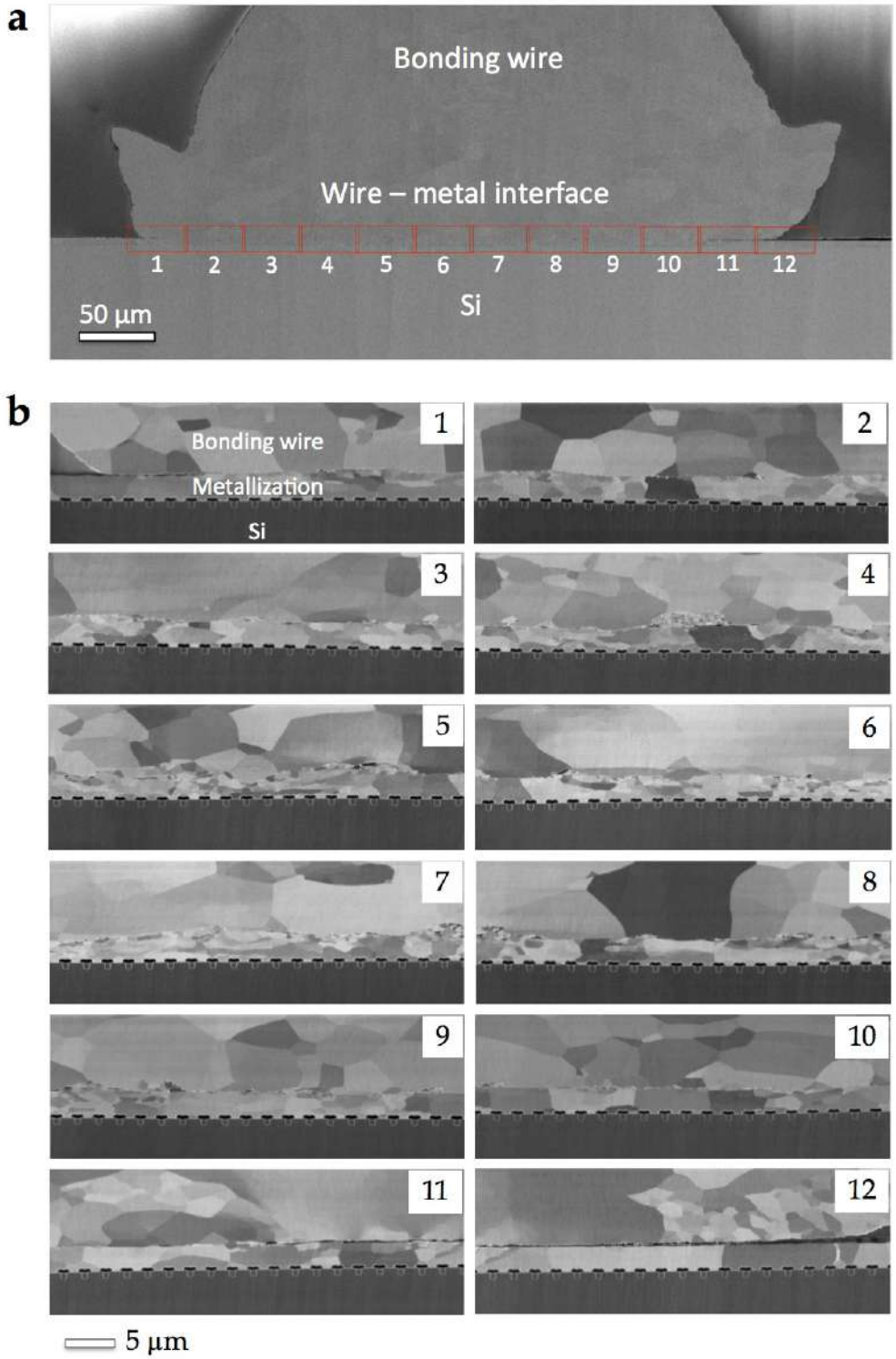

Figure 108: (b) SIM images mosaicing of the whole wire-metallization cross-section prepared by cross-polisher, according to the schema in (a). The images sequence offers a global vision of the metallization grain structure under the bonding wire and of the wire metallization interface. It can be used to calculate the total amount of deformed area due to the bonding process.

4.2.3.2 *Crack propagation in the metal and semiconductor of the aged modules*

We have investigated the cross-sectional inner structure of the aged module, in correspondence to the superficial metallization melting point that indicates the failure location (Fig. 105a). Large scale cross-sectioning reveals that under this area, the Si substrate is affected by a severe cracking. In the following, we present these degradation phenomena observed in two aged module, the first one at 70°C and the second one a 25°C.

70°C aged module.

The SEM image in Fig. 109 shows a 70°C aged module with the two bonding connections. In the insert we can see their position in the power device. Under the left wire in the SEM micrograph (named wire 1), large cracks propagate in the Si layer close to the metallization surface and down to the die attach, at the interface with the heat sink. A closer inspection under wire 1 (Fig. 110) shows two different crack types:

1. a thicker one, visible at lower magnification in Fig. 110a,
2. and a finer one, showed at higher magnification in Fig. 110c, 111a and 111b.

The latter is connected to cavities in the Al metallization (Fig. 110c) that are larger and rounder than the fatigue cracks generated during electro-thermal aging (Fig. 110b). Moreover, these bound cracks are filled with Al as shown in the EDX maps of a crack portion (Fig. 111c) and in the relative live scan plot (Fig. 111d), representing the element distribution along the dashed line in Fig. 111c. This suggests that local melting or large Al diffusion took place in a device that remained hot long enough, or that keep conducting a current despite not functioning anymore (these damages are too important to keep the device operational and have obviously destroyed several transistors). On the other side, we have verified that the larger cracks in the Si bulk are not filled with Al, meaning that the device was completely failed, non-conductive and cold when they opened.

A similar scenario could be envisaged under the passivated metallization between the two wires (Fig. 112). Here we can see a large crack in the Si layer branching out and propagating until the metallization surface, which in some cases appears completely broken (Fig. 112b). This remind us the FIB images of a 25°C aged module seen at the beginning of this section (Fig. 106a). Moreover, in Fig. 112 we can also observe finer Si cracks in the MOSFET region (on the left in Fig. 112a) and connected to

Al cavities (Fig. 113a). The EDX mapping confirms that these finer cracks are filled with Al (Fig. 113c).

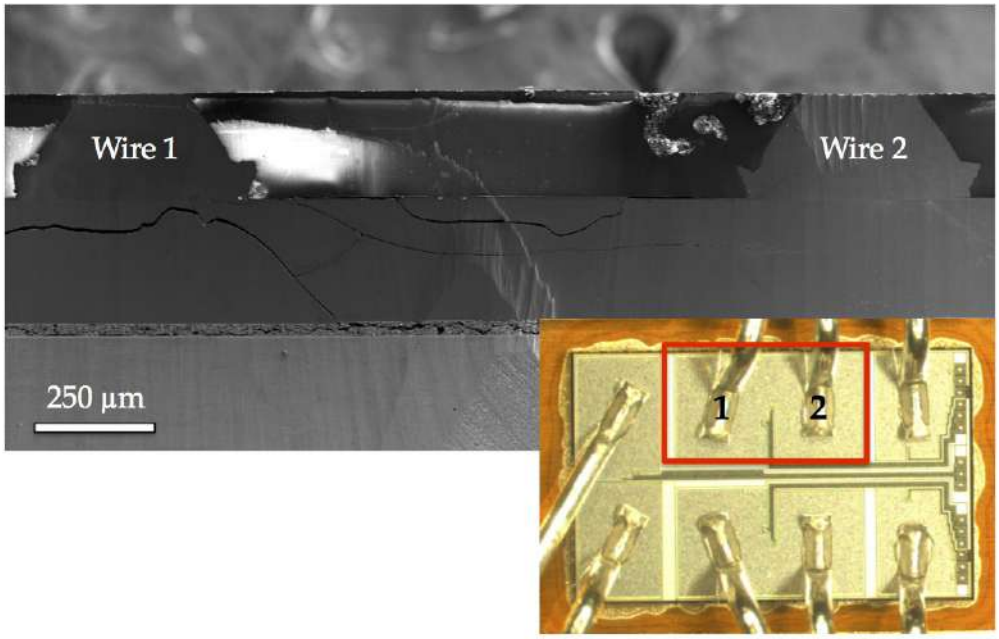

Figure 109: SEM overview of a 70°C aged module prepared by CP for the SEM/SIM inspection. In the insert, optical image image of the T07D17 device, showing the position in the aged module (in red) of wire 1 and 2 under investigation.

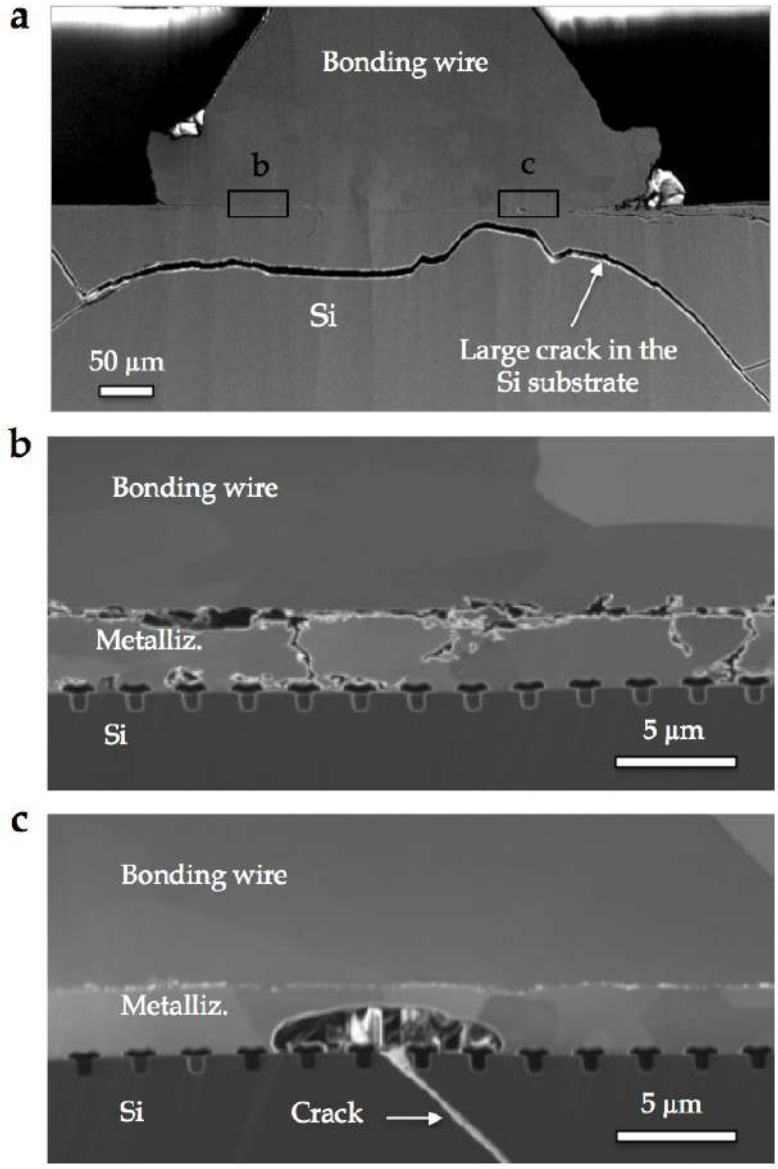

Figure 110: (a) SEM cross-sectional imaging of the bonding wire from an aged power module (70 °C aged) showing different types of cracks; (b), (c) ionic higher magnification images of the wire- metallization interface located in the boxes (b) and (c) in (a). The die crack resulted from an electro-thermal event occurring at failure time.

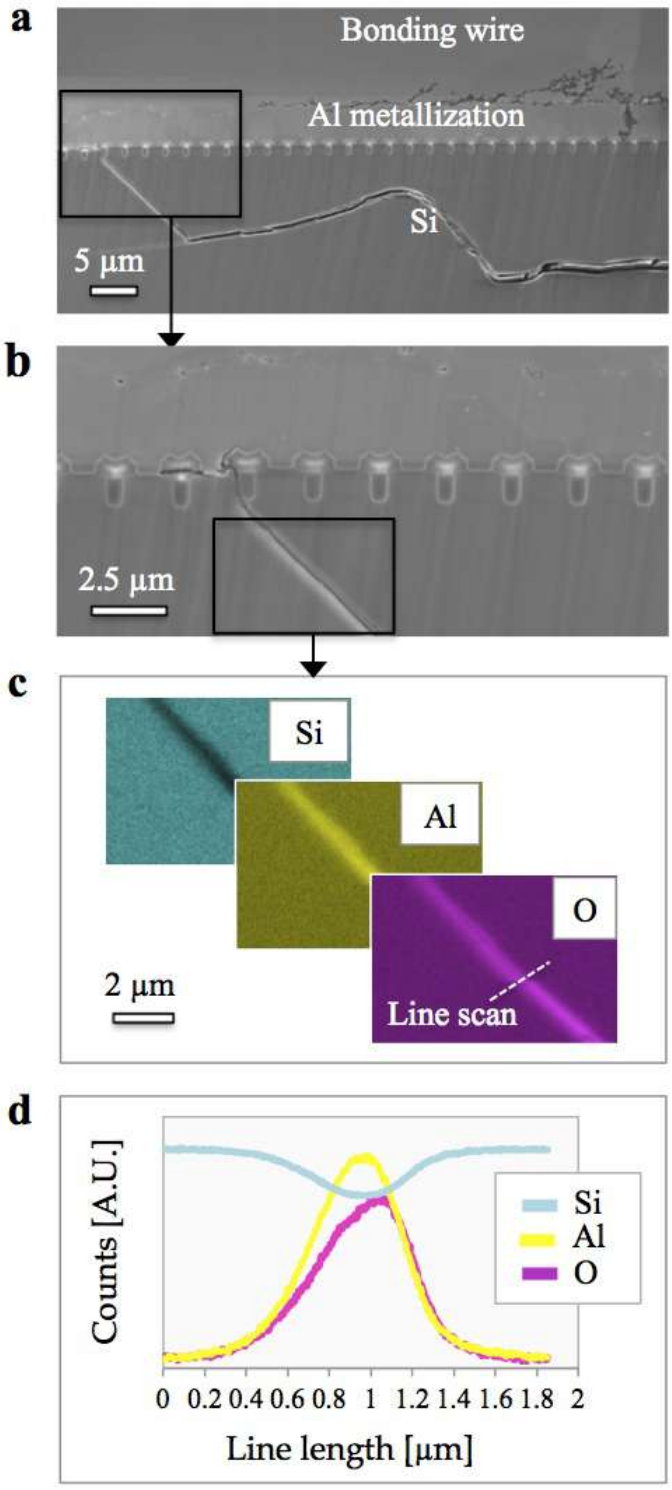

Figure 111: (a) Low and (b) high magnification SEM image of the cracked Si bulk under the bonding contact. (c) EDX mapping of the crack in the Si bulk and (d) relative line scan plot showing the element distribution along the dashed line in (c).

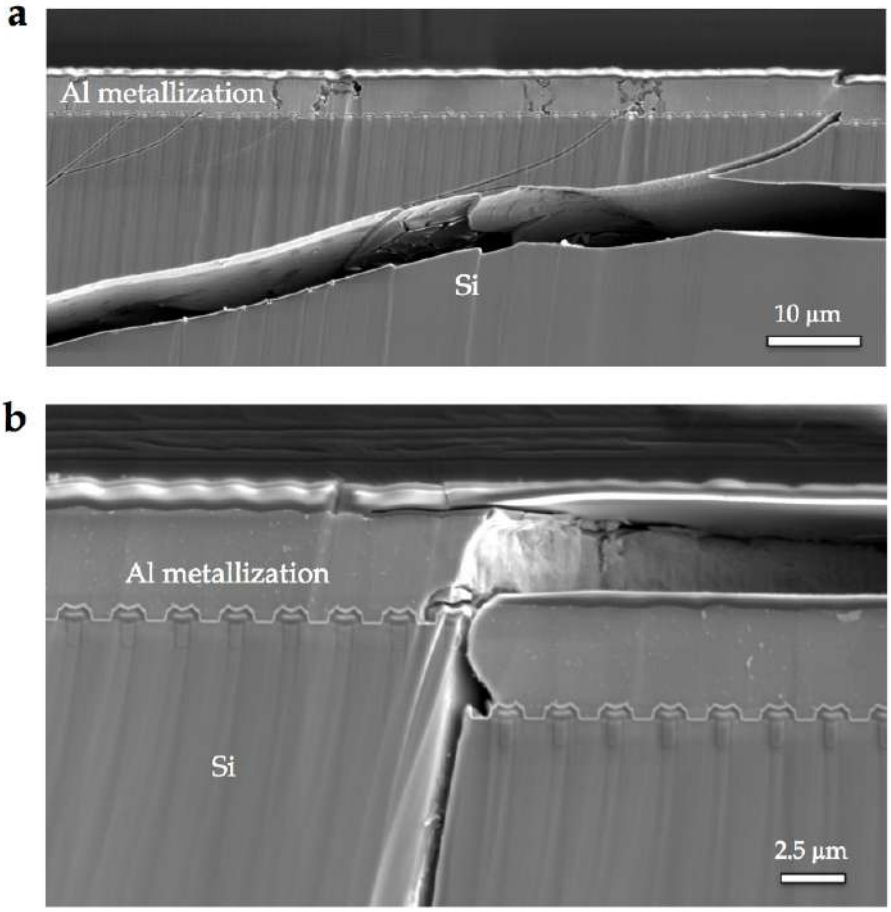

Figure 112: (a) SEM cross-sectional imaging of the naked metallization between the two bonding wire of the 70 °C aged module, showing different types of cracks: fatigue cracks in the metallization layer and fragile cracks in the Si substrate; (b) at higher magnification, the Al top metallization continuity results abruptly compromised as result of the crack propagation in the Si substrate until the surface.

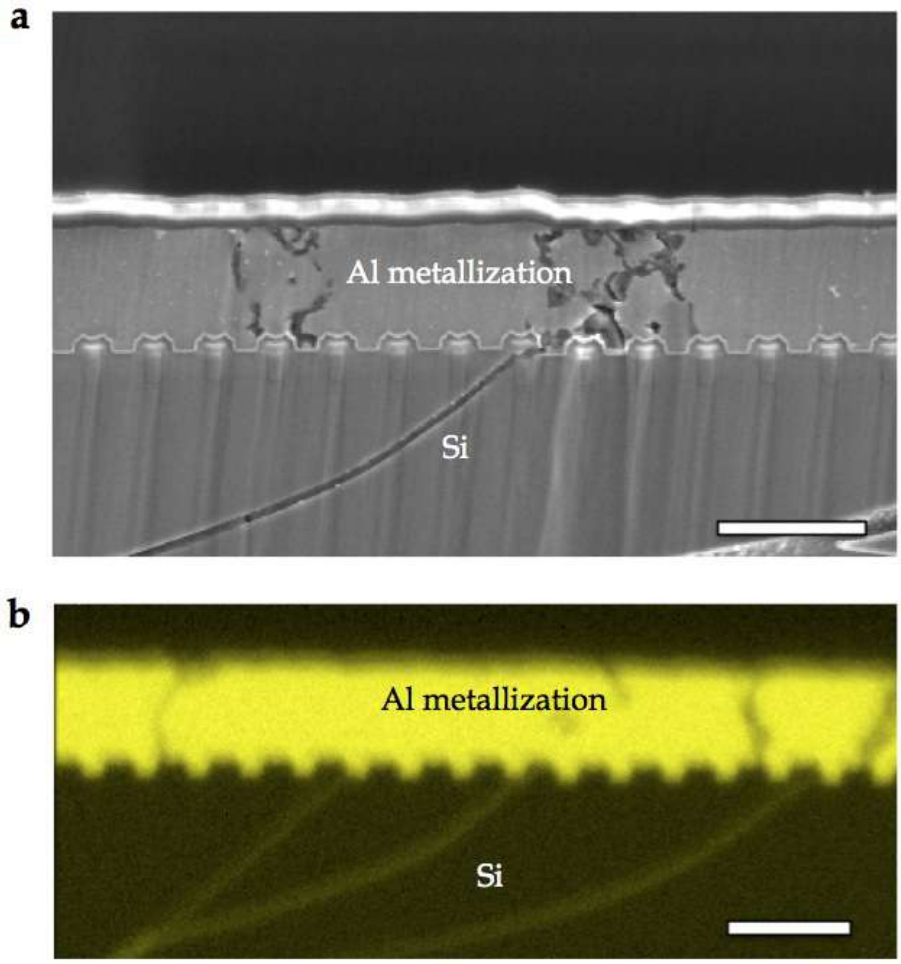

Figure 113: (a) SEM cross-sectional image of a fine crack in the Si layer contacted to the Al metallization in a 70°C aged module. (b) Al mapping by EDX showing some of these Si fine cracks filled with Al. Scale bar 5µm

25°C aged module.

Similar degradation phenomena have been observed in a 25°C aged module. The Si layer under one of the two wires results considerably fractured (Fig. 114a). The position of this wire is the same as wire 1 in the 70°C aged module previously observed (Fig. 109). Then, it seems that failure in the two analyzed modules occurs always at the same location, corresponding to the region beneath wire 1 in the insert of Fig. 109. Here, a large crack branches out everywhere in the Si substrate: upwards, through the interface with the MOSFETs area, breaking a dozen of transistors under the center of the bonding (Fig. 114a) and others under at the edge (Fig. 114c), and downwards until the die attach.
But the feature that has drawn the most of our attention is the round-shape area of $\sim 100\mu m$ of diameter in the Si layer, visible at low magnification in Fig. 114a and at higher magnification in Fig. 115a. Since its contrast looks similar to the one of the Al, we decided to analyze its chemical composition. In Fig. 115b we can see the EDX mapping of this zone, revealing that the round-shape feature is filled with Al. It means that the Al metallization and bonding wire melted and diffused in the Si because of the the high temperatures during failure. This is in accordance with the situation at surface level (Fig. 105b), showing a heavy melting of the bonding wire. EBSD mapping (Fig. 116) in the same zone reveals that the Al material diffused in the Si bulk is characterized by a granular microstructure. This means that the melted Al recrystallized when the device ceased to operate and cooled down.
At this point, in the highest magnification images of the area close to the bonding wire (Fig. 114b and Fig. 114c) we can notice that the Al-Al interface is no more visible in this bonding contact. On the contrary, SEM images (Fig. 117a and Fig. 117b) and EBSD mapping (Fig. 117c) from the adjacent bonding in the same aged module (corresponding to wire 2 in the insert in Fig. 109) show a normal structure : we can still distinguish a well defined wire-metallization interface with a finer granular microstructure in the Al metallization and larger grains in the bonding portion on top. This demonstrate that the warm-up has been localized in the first bonding area, where failure occurred. Here, the high temperature caused the melting of the two initial metallic parts, creating a new Al microstructure, and the diffusion of material in the Si below.

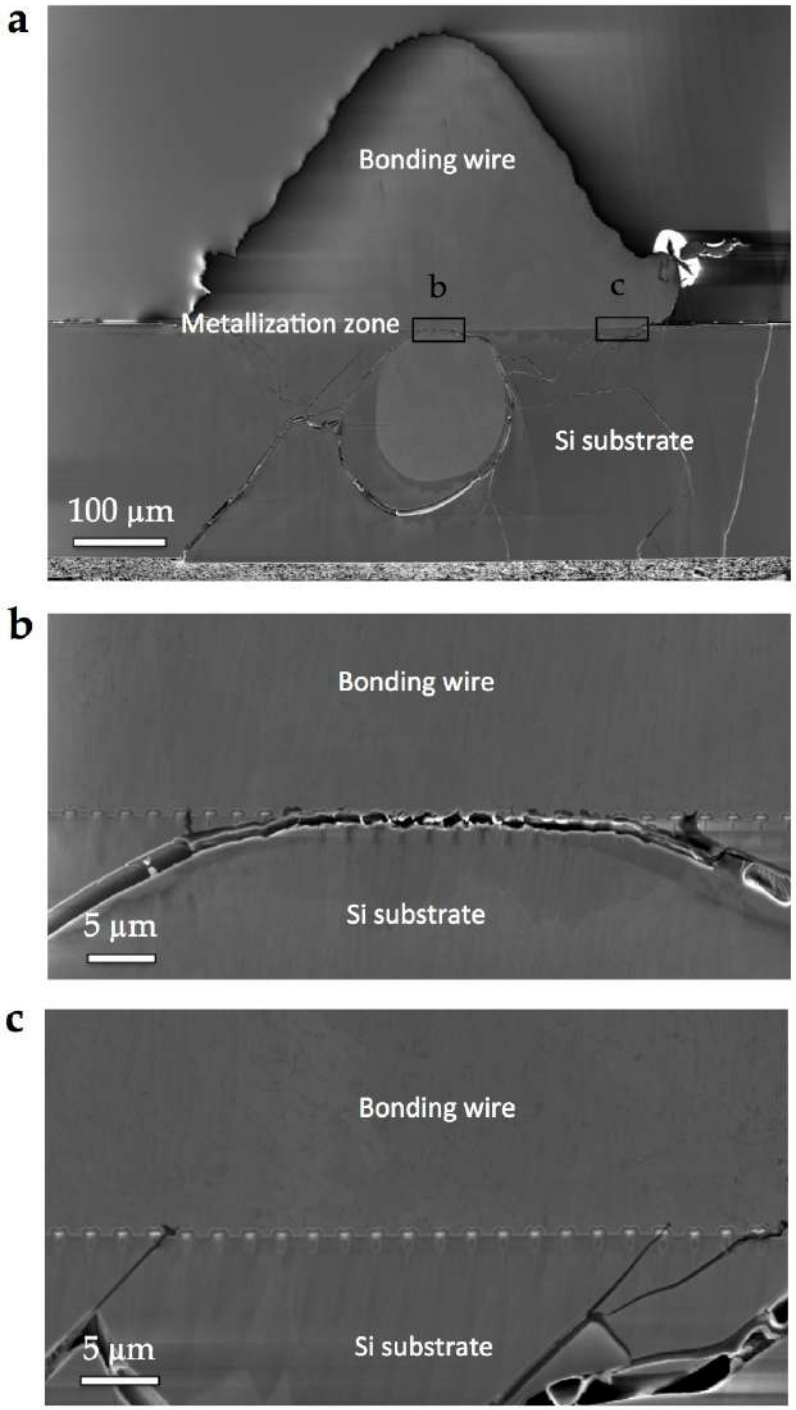

Figure 114: (a) SEM cross-sectional imaging of the bonding wire from an aged power module (25 °C aged) showing different types of cracks; (b), (c) higher magnification images of the wire- metallization interface located in the boxes (b) and (c) in (a). The die crack resulted from an electro-thermal event occurring at failure time.

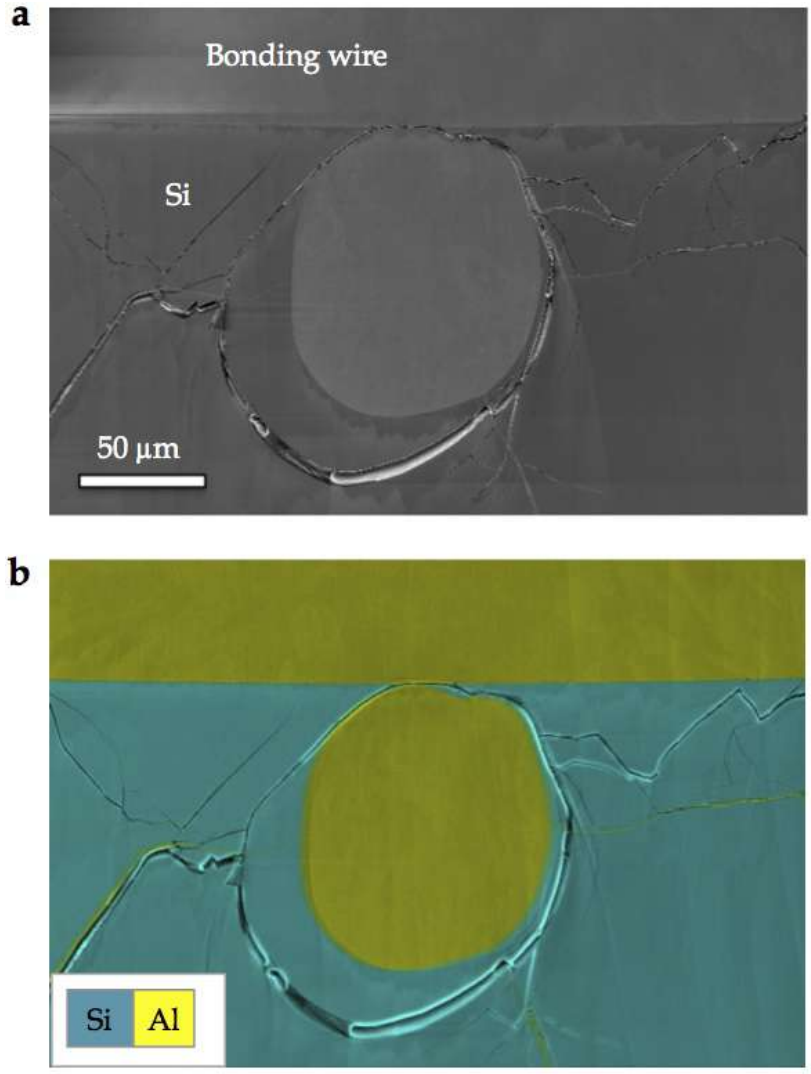

Figure 115: (a) SEM cross-sectional imaging of the round shape feature in the Si substrate (Al contrasted like) from an aged power module (25 °C aged); in (b) the corresponding EDX maps of the Si (in light blue) and Al (in yellow) are overlapped, showing that the round shape feature in the Si substrate is made out of Al. This has probably diffused from the top wire during the short-circuit event, because of the local melting of the metallic parts at high temperature.

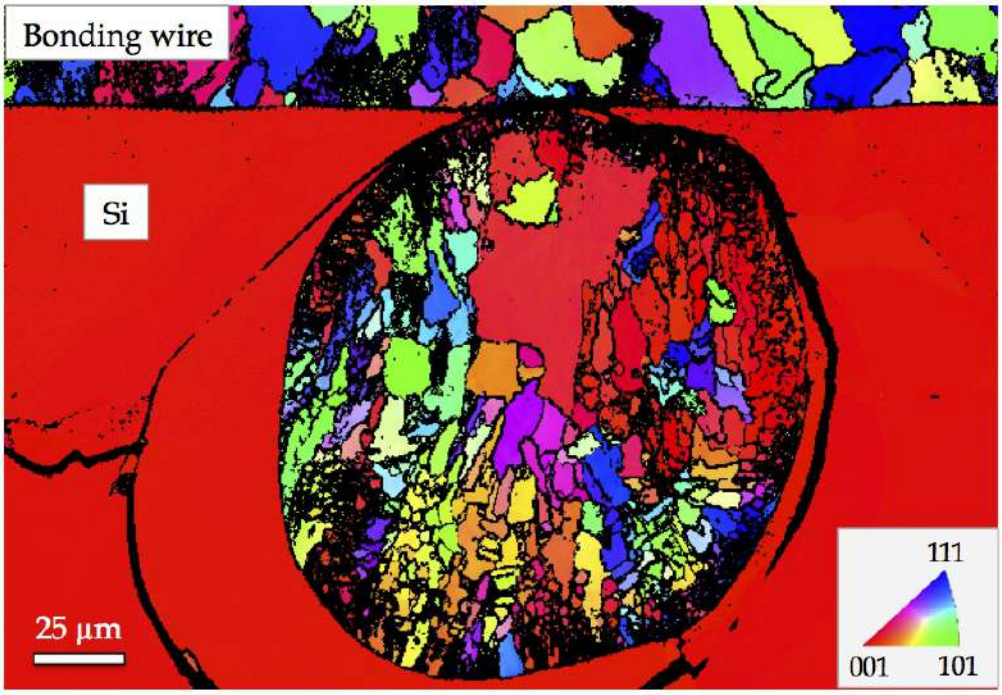

Figure 116: EBSD map of the melted area at the wire-metal cross-sectional interface from a 25 °C aged module. The standard stereographic triangle gives the color codes of the grain orientations, taken here along the horizontal direction.

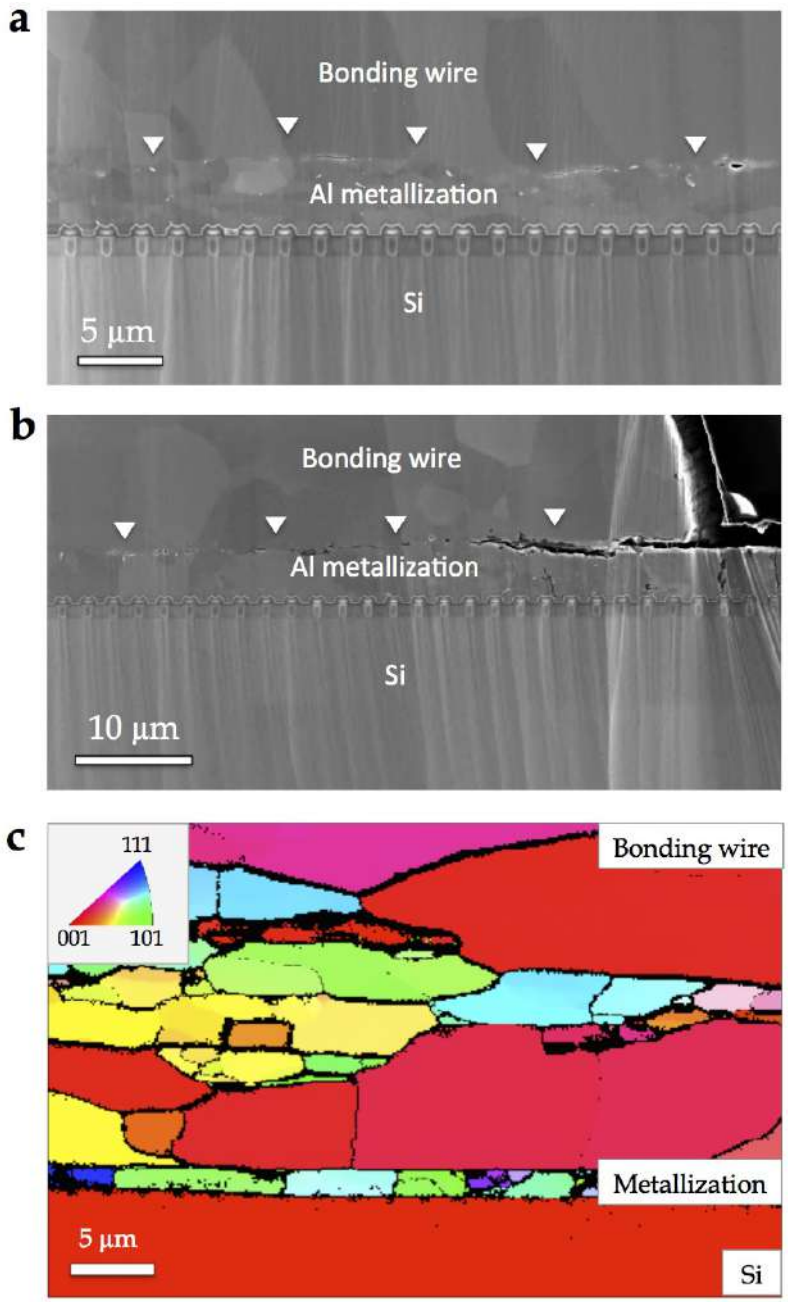

Figure 117: (a) SEM cross-sectional imaging of the wire-metallization interface pointed by the white arrows, (a) at the center and (b) at the extremity of the bonding area. (c) Relative EBSD map of the wire-metallization-semiconductor layered structure. The standard stereographic triangle gives the color codes of the grain orientations, taken here along the horizontal direction.

5

DISCUSSION

Device burnout is a common failure mode in power modules approaching their lifetime limit. Temperature runaway leading to this type of failure is often attributed to an increase of the drain-source resistance. In particular, the metal parts of power modules such as IGBT and MOSFET show alterations that could lead to such an increase of resistance. The alterations seen by these metallic parts are often attributed to their poor resistance to mechanical deformation, even if the mechanisms by which the alterations occur remain unclear.

Because solders and wire bondings failures are in part process- and in part material-dependent, tuning the mechanical resistance of these metal parts may increase their reliability. In fact, new generations of power devices have been designed to delay such failures, transferring some of the load to the source metal. This is particularly true for solders in the case of NXP power modules: the LFET1T power MOSFETs studied in this work aged mainly through metallization degradation The aging of the source metallization, instead, cannot be fully controlled and seems governed by intrinsic and universal degradation mechanisms that will be discussed in this chapter. The Al technology employed here is rather representative of many back-end packaging in the field: Al wires are ultrasonic-welded to the metallization. Aside from the subsequent electrothermal cycling, many parameters can influence the potential evolution in this set-up:

- the composition of both the wire and the metallization. Alloying will increase its mechanical and ohmic resistance;
- the grain size of both elements will influence their hardness and microstructural stability (small grains will make the metal harder but will be prone to grain growth);
- the interface created between the wire and the metallization will depend on the bonding parameters, may affect the microstructure of both the wires and the metallization and introduce external elements.

We will first recall how the $R_{ds(on)}$ can be linked to the elevating temperature of the module during aging. Then we will compare the as-process and aged microstructures of both metallization and wires, and then discuss the possible mechanisms of aging for each parts, focussing on the metallization (passivated or not) and the evolution of the wire/metal interface.

5.1 $R_{ds(on)}$ EVOLUTION DURING ELECTRO-THERMAL AGING

The device burnout is the failure mode mainly observed in the LFET1T components under investigation (Fig. 118), as consequence either of a failure event occurring somewhere in the device or of its wear out [Cia02]. It is associated with the short-circuit conditions imposed during the accelerated aging tests, which compel the device to endure large current flows while the battery voltage is applied. This leads to thermal stress peaks, corresponding to a local increase in the $R_{ds(on)}$, which accelerate the device aging until the final failure [Cia02] [Ber10] [Kho07a] [Mar14].

During the first part of this work, we have set up a test protocol that allowed us to monitor the device aging through the evolution of the $R_{ds(on)}$ and, in parallel, the change in the microstructure of the Al source metallization. The result is reported in Fig. 119. The plot shows the $R_{ds(on)}$ at increasing number of SC cycles and confirms an increase, of about 14%, in the Rdson during aging, until failure. As seen in details in the previous chapter (section 4.1) and summarized in 120), this is associated to a progressive Al surface metallization reconstruction, that to clearly show up after ~ 100 kcycles.

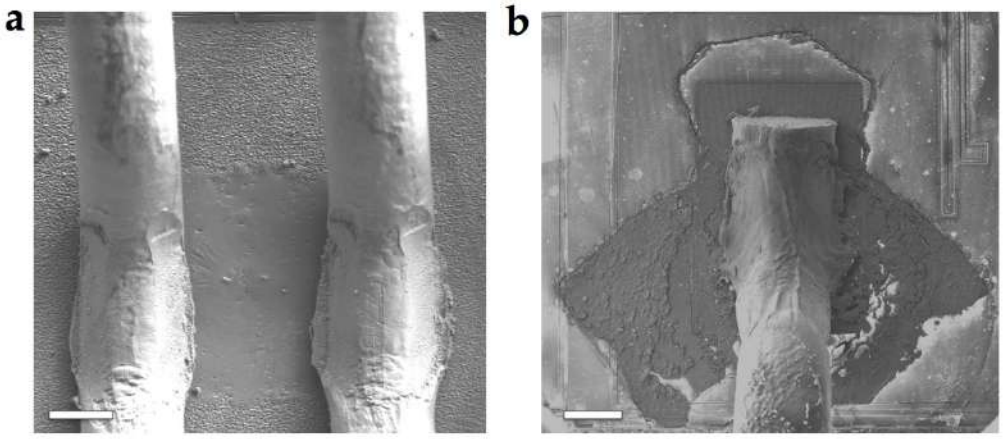

Figure 118: Burnout spots detected after failure (a) between two bond wires in a SPD06 module and (b) at the bonding connection in a T07D17 module. Scale bar: 250µm.

5.1.1 *Potential and temperature mapping*

In order to assess the role of the top metal resistivity in the Rdson curve, potential mapping have been performed on the top surface of the DUT at 1kcycles, 50 kcycles, 200 kcycles and 300 kcycles (Fig. 121). Due to the damages induced

by the probe during the potential measurement, each map has been acquired from a different device. Therefore, the obtained results are not consistent for a quantitative comparison of the ageing factors. However, we can observe a metallization voltage drop arising in the center of the device during aging. An increase of approximately 0.6 mV at 1 A DC occurred between the initial state (1Kcycles in Fig. 121a), and the end of life (300kcycles in Fig. 121a). This means that the electrical resistivity of the top metal layer has significantly increased with the ageing of the DUT. The short circuit current with a maximum value of 600 A will be responsible for a greater increase in the source potential.

A similar analysis has been conducted using an IR thermal mapping system. The ageing effects on the device electro-thermal behavior has been assessed by measuring the time- dependent temperature increase on the top surface of the DUT. The thermal measurements have been performed in equivalent time domain using 500 kHz frame rate. The short circuit pulse has been periodically repeated during each measure. Also in this case, different devices have been used to evaluate different ageing levels. As result, Fig. 121b depicts the hottest maps for 1 kcycles, 50 kcycles, 200 kcycles and 300 kcycles respectively. IR maps show relatively homogeneous temperature increase during short circuit event for low aged devices while the middle of the device experiences the highest temperature area. The locations of the hottest points on the DUT have been marked on the maps by black arrows. For components having undergone a significant number of short-circuit events, we observe the emergence of hot spot close to the wire bonding pads location with a reduced temperature peak at the device center, as predicted by the source potential analysis [Rom14]. This hot spot is the result of focusing of the current and it is the main cause of device performance degradation and eventually failure [Ira05]. It can also be connected to the metallization reconstruction and the depolarization of the gate in areas distant from wire bonding. It is also clearly shown that the positioning of the on chip temperature sensor becomes critical as the ageing factor increases [Ira05]. In fact, as stated above, the hottest point changes position, moving from the device center to the bonding wires locations.

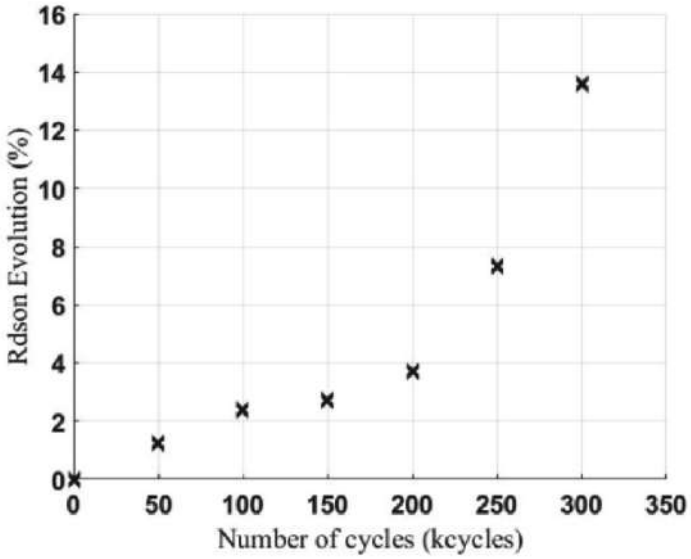

Figure 119: Increase of about 14% in the on-state resistance after repetitive SC events (3.55 J/cm²) at ambient temperature. At 300kcycles the device failed.

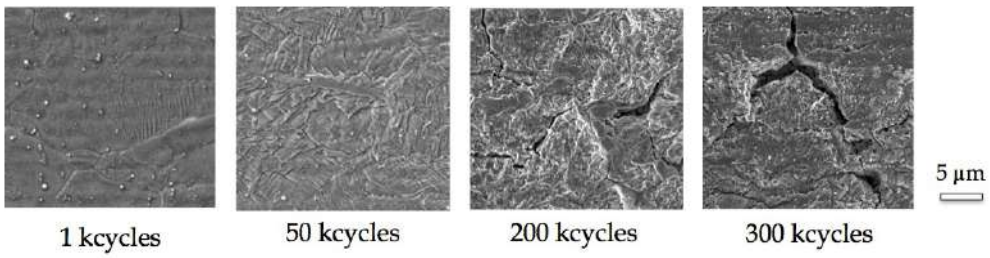

Figure 120: Increase of about 14% in the on-state resistance after repetitive SC events (3.55 J/cm²) at ambient temperature. At 300kcycles the device failed.

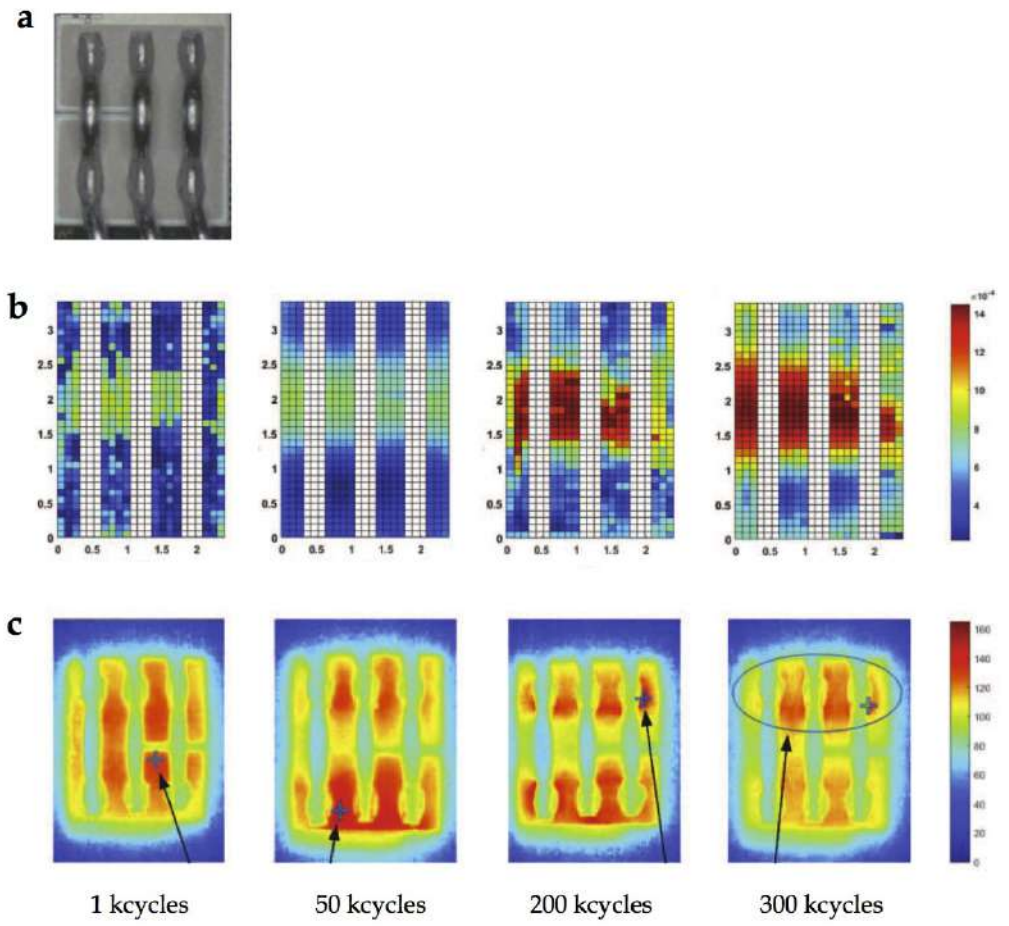

Figure 121: (a) Active module of an SPD06 device under aging test. Potential and temperature mapping of its surface have been performed during aging.
(b) Source voltage mapping [V] at $I_D = 1A$ under SC conditions, after 1kcycles, 50 kcycles, 200 kcycles and 300 kcycles.
(c) Temperature distribution [K] under SC conditions, after 1kcycles, 50 kcycles, 200 kcycles and 300 kcycles. Areas where the temperature is lowest correspond the bonding connections, according to the picture of the active module in (a).

5.2 SOURCE METALLIZATION RECONSTRUCTION AND CRACK PROPAGATION - NAKED METALLIZATION

A systematic SEM and SIM study of the Al source metallization of SPD06 and T07D17 modules that underwent different electro-thermal aging conditions reveals common metal degradation mechanisms. They consist in a heavy metallization reconstruction in the vicinity of the bonding connections. It occurs, at surface level, by an increase in the metallization roughness compared to the initial granular Al structure Fig. 122, and, deep inside the material, by an apparent grain shrinkage (Fig. 123. At the same time, fatigue cracks run from the Al surface down to the transistor area, following the grain boundaries.

The results of our microstructural characterization are in line with the degradation mechanisms described in the literature for Al and Cu metallizations [Gla04] [Cia02] [Mar14] [Nel11] [Nel13]:

- Before tests, the metallization surface is smooth and fits the wave-pattern structure of the transistors (Fig. 122a). As in standard Al films, grains are detected at the surface and little depressions define the grain boundary grooving. They form at grain boundaries and triple junctions in order to balance grain boundary surface energy and metallization surface energy [Mar14] [Mul93] [Thooo]. Inside the layer, the interface between grains are visible by ion channeling contrast; bamboo Al grains, with 4µm average diameter and height equal to the layer thickness, fill all the metallization volume. The high diffusivity of atoms at grain boundary and at the surface explains the formation of these depressions after deposition at high temperature and cooling or during thermal cycles [Hei10]. In aluminum, surface diffusion is supposed to be shut off by the natural oxide that grows almost instantly when bare Al atoms are in contact with oxygen. Grain boundary grooves are however systematically observed in bare Al thin films, especially those deposited at high or medium temperature, as for these sputtered metallizations. This means that oxidation probably occurs after the films are cooled, or that surface and grain boundary diffusion, aided by the tensile stress state of the film on cooling remains sufficiently active to overcome surface oxidation and provide stress relaxation.

- After tests, the metallization surface is modified and shows a strong alteration due to plastic deformation and extrusions; the initial structure of transistors is almost no longer visible. Inside the layer, grains are divided in smaller grains and inter granular cracks appear.

We have then developed various hypothesis of mechanisms that could lead to this transformation of the metallization:

- an increased surface roughness with no particular crystallographic orientation;
- a grain size that seems smaller than the initial bamboo structure;
- an accentuation of the initial GB grooves that dive down to the transistor area.

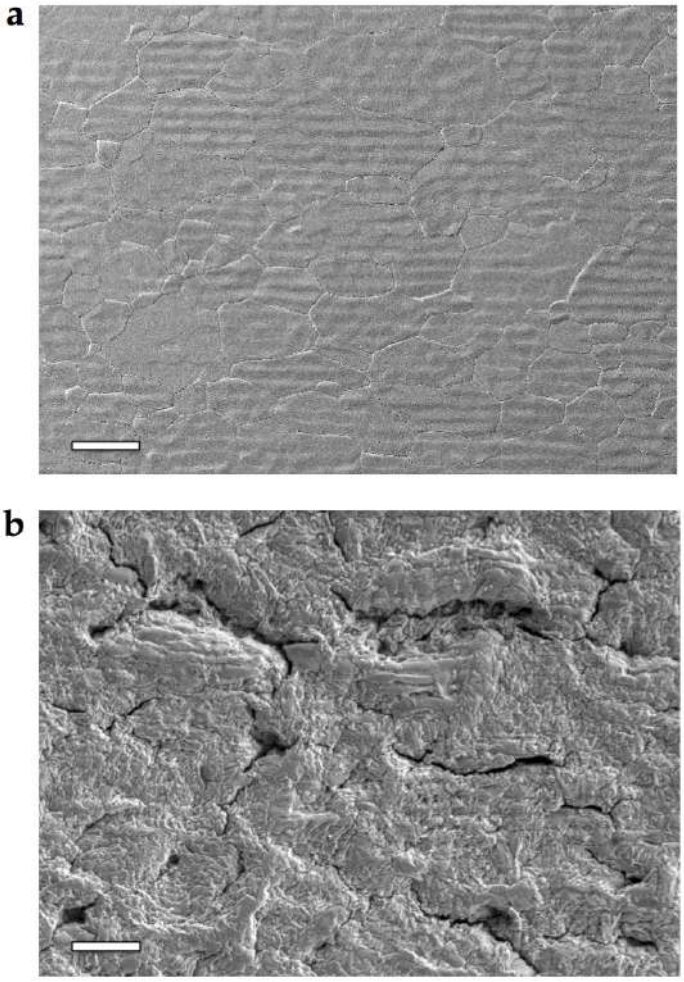

Figure 122: Al source metallization top view. (a) The initial Al structure is smooth and fits the underlying MOSFETs structure. (b) After electro-thermal aging the metallization roughness increases and many cracks propagate along the grain boundaries. The grain structure and the transistor pattern are almost no longer visible. Scale bar: 10μm.

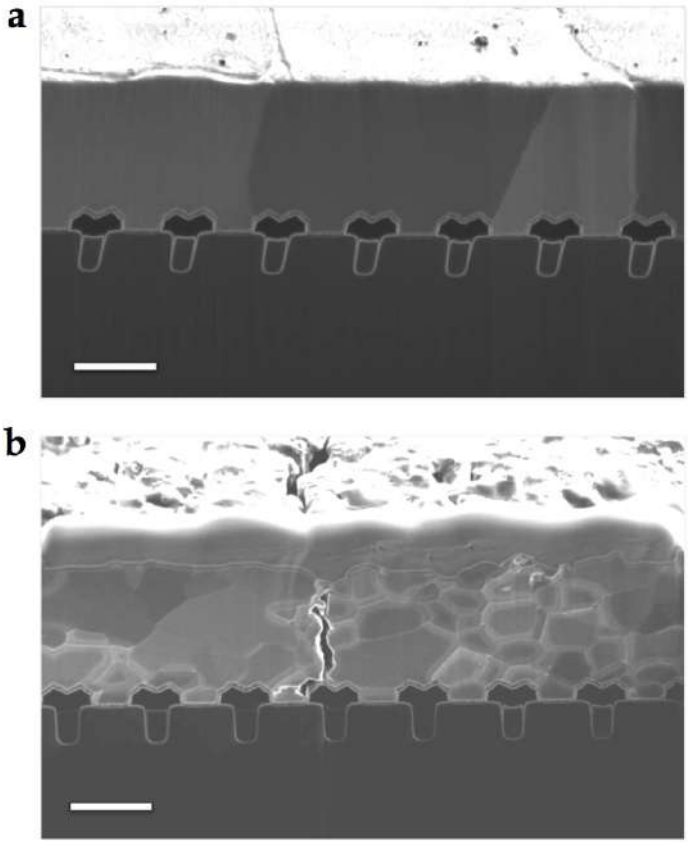

Figure 123: Cross-sectional cuts through the Al source metallization. (a) Before aging, bamboo Al grains fill all the metallization volume. After electro-thermal aging, an apparent grain shrinkage and crack propagation along the grain boundaries are observed. Scale bar: 2.5μm.

5.2.1 *Possible deformation mechanisms*

Several approaches are possible to assess the possible mechanisms at play. A first manner would be to refer to the "*Deformation Mechanisms Maps*" from Frost and Ashby [Fro82] who have compiled the dependency of stress, temperature and plastic strain rates for various materials (in bulk form). For each type of material (metals and ceramics) they define different domains in a stress versus temperature chart in which the deformation rate is predicted. Obviously, a piece of aluminum loaded at high stress and high temperature will deform faster than the same piece at low stress and low temperature. Some mechanisms are also predictable:

- at low stress and high temperature, deformation can occur through various type of diffusions ("Coble creep" when the atoms diffuse through grain boundaries and "Nabarro-Herring creep" at higher temperature when this diffusion is massive through the crystalline lattice).
- At high stress and low temperature, deformation will very probably take place through dislocation glide processes.

In the materials, there is no defined frontier between the various mechanisms and these charts were definitely not intended to be universal and may be adapted for various situations. For instance, the maps are microstructure-dependent: the grain size will play a role in the Coble creep diffusion. The smaller the grain size, the denser the GBs in the material, and thus the higher strain rate for a given temperature and stress when Coble creep is activated. Also, mixed mechanisms such as dislocation climb (often included in the more vague denomination " power-law creep ") appear to be effective between the two extremes (low T- high stress, high T, low stress).

This approach constitutes one of the reasons why we tried to set up a stress measurement system during this thesis. Our system, described in Appendix B was first tested in mid-2017 after multiple technical issues. We were able to retrieve a few stress/temperature curves, as the one in Fig. 124 before additional technical issues stopped us. This plot describes the evolution of the bi-axial stress in a naked SPD06 die (without bonding wires) after being cooled to liquid nitrogen. Initially (at 25°C), the Al is in compression because it expands more than the Si substrate on which it is attached. Very rapidly (at around 50 MPa), it relaxes plastically until 160°C where the heating (20 °C/min) is reversed to cooling. We chose this point as the zero stress [1]. The stress then increases linearly until 100MPa in tension (this linear part corresponds to an

1 In absence of absolute wafer curvature prior to the device fabrication, we don't have an absolute value of the stress in the wafer + film system. The stress variations are real, but relative.

elastic loading) before remaining constant from about 80°C down to 25°C. This plateau is also the signature of a plastic relaxation. Such plot would therefore indicate two temperature segments in which the Al metallization deforms plastically :

- From 40 to 160°C in compression
- From 80 down to 25°C in tension

The stress amplitude is lower than 150MPa. If we refer to the Frost and Ashby maps for these stress and temperature, the mechanism predicted is clearly dislocation-based plasticity.

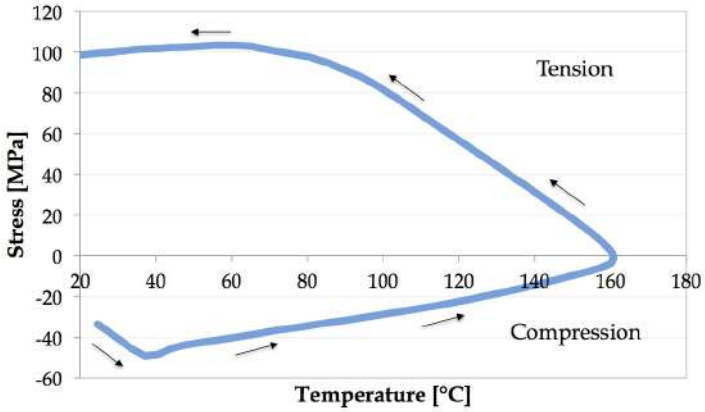

Figure 124: Stress-temperature plot for a 20-160 °C temperature cycle performed on a naked SPD06 die. The stress is directly deduced from the die curvature (measured by laser reflectometry - see Appendix B) using the Stoney equation (chapter 2, section 2.2.2).

It is interesting to note that O. Bostrom in 2001 [Bos01] followed the same approach for Al films deposited on Si substrates: stress measurements based on wafer curvature and Frost and Ashby mechanisms maps. By building a map for the specific case of a 1µm thick Al film with a bamboo structure deposited on an oxidized Si wafer, he concluded that the equations of [Fro82] underestimated grossly the stress in the film at medium and high temperatures and were unable to reproduce the experimental stress/temperature curves obtained by profilometry.

Expanded from epitaxial semiconductors [Mat74], a dislocation-based plasticity model was also set-up by Nix in the late 1980's. In this model, that mainly focus on the yield stress of thin metal films, plastic deformation is exclusively resulting from the motion of so-called "threading dislocations". These dislocations, by shearing the film, also lied down a dislocation segment at the metal/-substrate interface. The thinner the film, the higher the stress to stabilize this

interfacial dislocation segment. Analytical calculations lead to a 1/film thickness dependence of the yield stress, a relation that has been widely verified in many metal/substrate systems [Wie07]. This model has been implemented by Thompson [Thooo] to take in account the role of grain size in polycrystalline films, such as the bamboo structure present in the present DUT metallizations. In this dislocation-based approach, the smallest dimension (grain size or film thickness) will dictate the yield stress of the film, provided the dislocations are stopped by the interface or the GBs.

5.2.2 *Plasticity by dislocation propagation*

A more straightforward approach to test the possible deformation mechanisms at play in the metallization is to perform temperature cycles on a cross-sectional sample inside a TEM. TEM is one of the few tools able to image dislocations with the appropriate resolution, and probably the only one able to capture dislocations movements at video rate inside single Al grains. As described in chapter 4, section 4.1.3. The difference between the silicon and aluminum CTE is large enough to induce irreversible dislocation motion. In our experiments, dislocations movements did not start before 300°C, both in the FIB lamella and the tripoded sample. It is important to point out that the dislocation activity linked to Δ CTE effect has only been observed in the TEM specimen having the Al layer in contact with the entire Si substrate thickness. This was not the case for the ultra-thin TEM lamella, prepared by FIB, that we used for the ACOM mapping of the Al metallization. In this later case, the small remnant of the Si substrate is not able to impose a stress to the Al layer. Although the thickness of the TEM specimen is much smaller than in the real metallization, the absolute level of stress should be similar (about 20% lower for the Von Mises stress [Leg09]. This explain why it is usually necessary to reach higher temperatures in an in-situ TEM compared to a wafer-curvature experiment. However, the differences that we see here are important (300°C in the TEM and less than 100 °C in the wafer curvature experiments). This discrepancy is not completely explained as for now, but much more wafer curvature experiments (with varying parameters such as temperature gradients, temperature holds...) and in situ TEM temperature cycles (different grain orientations, initial microstructures, ...) would be needed to rationalize it.

What has been clearly demonstrated during these in-situ experiments and those previously reported in the literature [Mar14] is that the density of moving dislocations decreases during successive thermal cycles. They escape through surfaces and crystal-amorphous interfaces [Leg02] but are also trapped in subgrains they contribute to form. These observations are in line with Martineau et al. results and with the observations by FIB of grain shrinkage after thermal

cycling reported in our work and in the literature [Ber09]. At first instance, this division surprised us as grain growth is usually observed for polycrystalline Al thin films on Si submitted to thermal cycles [Leg02] [Sch93]. However, ACOM-TEM mapping showed that this division is due to the high sensitivity of electron channeling in FIB imaging. In fact, misorientations between these smaller grains is less than 10°, which means that they are subgrains formed by the gathering of preexisting dislocations inside a single "mother grain" [Hum05]. This means that the plastic deformation generated by dislocations is very low (Martineau et al. reported a value of 0.3% per cycle from 25 °C to 450 °C for an Al layer of 10µm [Mar14]) and cannot lead to the formation of voids between the various grains, as observed (Fig. 122b and 123b). Moreover, we can expect very low stress values at the end of a cycle owing to the layer thickness (4µm), as it has been experimentally shown that this stress varies inversely proportional to the thickness [Nix89] [Nix98] [Wie07].

Thus, on the base of in-situ TEM observations, we can conclude that after this first phase of very low plastic deformation and grain reorganization (that probably happens in the very first cycles) other mechanisms than dislocation-based plasticity must occur to explain the Al source metallization plasticity and degradation.

5.2.3 *Plasticity by atom diffusion*

Plasticity by diffusion is described by an analytical model developed by Gao in 1999 [Gao99] [Wei01]. According to Gao's model, a tensile stress is relaxed by the diffusion of matter from the free surface towards the film interior. Travelling along grain boundaries, the extra atoms contribute to the formation of a flexion boundary, which can be seen as an array of edge dislocations. Since the film is constrained by the substrate, the stress concentrates at the grain boundary/substrate interface and may generate emission of dislocations along the film substrate interface. The opposite mechanisms, that is the compression stresses, has not been taken into account. Gao's model has been validated on ultra fine copper films (200 nm) during heating experiments in a TEM [Bal03]. It is supposed to work for ultra fine films (< 300 nm) with bamboo structure (in which the diameter is equal or smaller than the film thickness) and without native oxide. It can, therefore, explain gold and copper film behavior, but it is not applicable to thicker, self-oxidized Al metallization layers.

However, it has been showed by Legros et al. that this deformation mechanism can be generalized to more complex systems including Al films [Leg03] [Leg05]. Moreover, a few years ago, Pietranico et al. studied by SEM the evolution of the source metallization structure during the aging of power MOSFETs-based devices without packaging [Pie11] [Pie09]. This is exactly what we did

as first step to characterize the Al microstructure of SPD06 power modules at increasing aging cycles. In line with our observations, the authors showed an increased grain boundaries grooving with the number of cycles, with the consequent formation of fatigue cracks and extrusion close to the grain boundaries. On the basis of these considerations, supported also by similar observations with thin films on substrate submitted to thermal cycles [Hei10], we can conclude that the plasticity of these metal layers takes place at grain boundaries and that diffusion is the main deformation mechanism behind the metal degradation.

Based on the Gao's theory, Martineau et al. were the first ones to propose a qualitative model to explain the crack initiation and propagation during positive and negative electro-thermal stresses of power MOS metallizations [Mar14]. This model, presented in Fig. 125, fits well the experimental observations on the LFE1T under investigation. The initial Al bamboo grain structure is represented in yellow on the Si substrate in blue (Fig. 125a). At their interface, the line layer represents the transistor area, whereas at surface the self-oxidation layer is in red. The model is described by Martineau [Mar14] as following:

> During the first thermal cycles, dislocations in the large grains of the Al as-processed film rearrange themselves in cells (Fig. 125b), and then in sub-grain boundaries (Fig. 125c). Remaining mobile dislocations are absorbed at oxide interface and free surface. At this point, there is no more easy plastic deformation vector and diffusion takes over. Upon heating, the Al layer expands more than silicon but, constrained by the substrate, goes in compression. Aluminum atoms move toward the free surface along grain boundaries that are the more rapid paths for diffusion. If the stress is large enough or lasts long enough, they can go through the oxide barrier located at the bottom of the thermal grooves and oxidize when exposed to the atmosphere. The accumulation causes small, oxidized hillocks that cannot annihilate by surface diffusion (Fig. 125d). During cooling, the layer stress turns tensile causing boundary grooving to self-passivates through surface oxidation (Fig. 125e). These grooves cannot bond again during compression because of the oxidation layer formed at the Al free surface (Fig. 125f). Over repeated cycles, grooves become deeper cracks as they duck down into the Al (Fig. 125e). Some of them reaching the interface with silicon (Fig. 125g), causing a local electrical disconnection between neighboring Al grains.

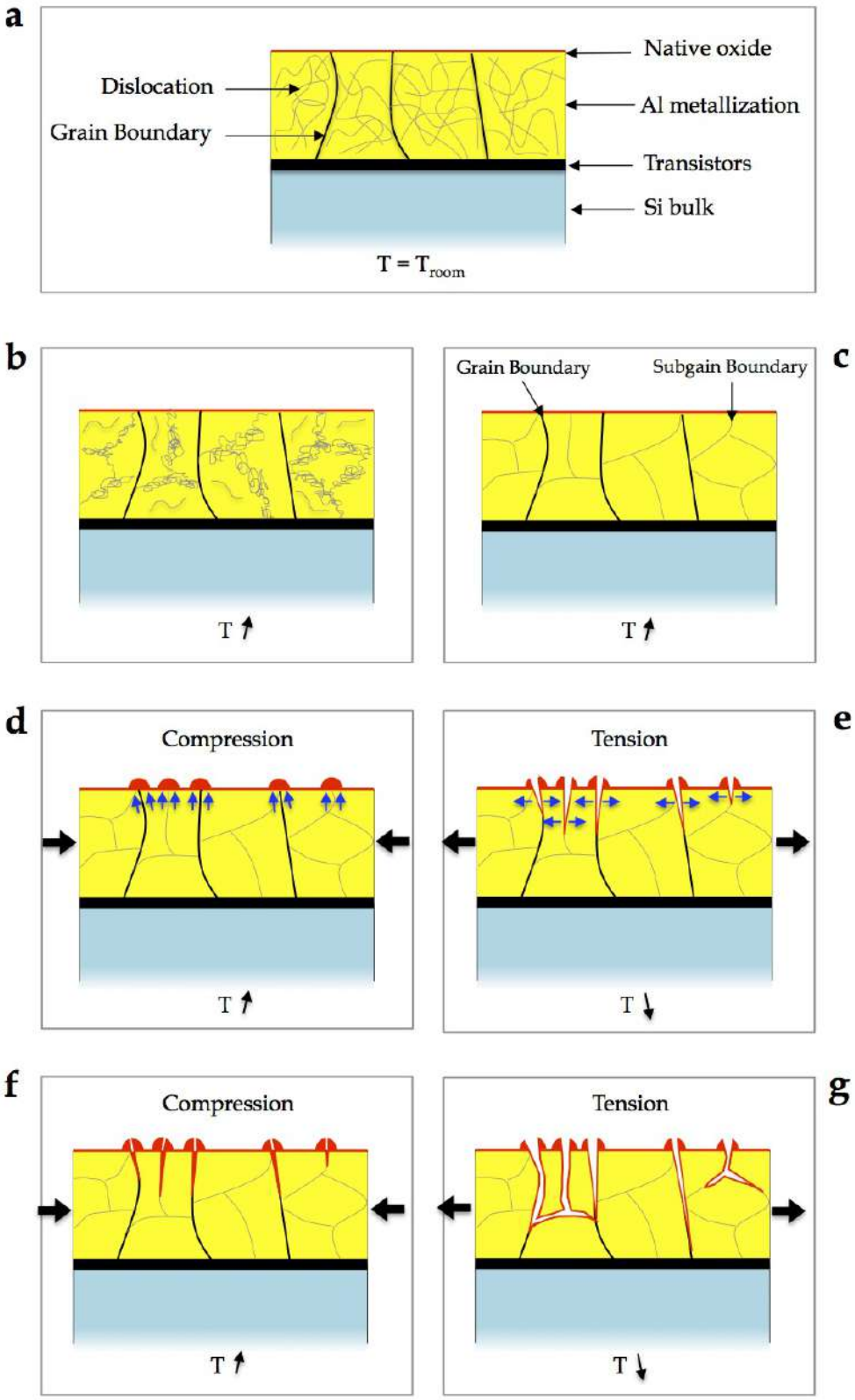

Figure 125: Gao's model extended to Al layers undergoing tension and compression stresses during thermal cycles [Mar14]. (a-c) The dislocation density decreases by recombination in sub grain boundaries and absorption at GB interfaces. (d-g) Al diffusion along grain boundaries, and subsequent oxidation causing crack propagation through the Al layer.

5.2.4 *Plasticity by electromigration*

Another possible explanation for the formation of hillocks and the degradation of metal layer in the vicinity of the bonding connections is electromigration. This mechanism, consisting in the transport of mass in metals stressed at high current densities, has been reported in literature since the '60s as a failure mode in aluminum-based metallizations for semiconductor devices [Bla69] [Vai80]. The electron flow drags metal atoms resulting in the formation of voids, where atoms are ejected, and extrusion, in the area where they gather [Zen02]. This can lead to the formation of an open circuit in the Al metallization due to void formation by condensation of vacancies. Another consequence is the growth of etch pits into Si, where electrons leave and enter the Al, by the solid-state dissolution of Si into Al and the transport of the solute ions at the Al-Si interface [Bla69]. However, current densities needed for this mechanism are significantly higher than the ones present in the present MOSFET wires and metallization [Lie05].

During the microstructural characterization of LFET1T power devices, we have never observed neither any asymmetry in the degradation of the surface layer, according to the direction of the polarization, nor accumulation/depletion of atoms whether at the Al surface or at the Si interface. We did not either observe electro migration evidence near bonding as it was observed by Tse and Latch [Tse95]. We can therefore conclude that, if electro migration is an active mechanism, it is not observed here, either because it is too weak, or because its effects are largely compensated by another phenomenon like surface or GB diffusion [Mar14]. This conclusion as also been reached by researchers in Denmark that have cycled power diodes [Bri15] [Bri16].

5.2.5 *Fatigue crack propagation: SPD06 vs T07D17*

According to the previous discussion, we can conclude that metallization degradation in LFET1T power modules starts with a grain division by dislocation glide that rapidly exhausts, followed by an accelerated diffusion of Al atoms through the grain boundaries from the metallization interior to the surface. This justifies the formation of fatigue cracks along the grain boundaries that are bound to propagate deeper and deeper in the Al layer until failure (they can not heal during compression phases because of the oxidation of Al free surface). During aging, cracks propagate along GBs and not along sGBs. This is because they are initiates at the GB grooves at the early stage of aging and sGBs are formed after.

At this point, two different degradation mechanisms have been observed in the LFET1T power modules under test, according to the schema in Fig. 126:

- Cross-sectional images of the bare Al metallization (without mold and oxide passivation) in SPD06 power modules under progressive aging cycles show a generalized broadening of the fatigue cracks in the final stage of the device life (Fig. 126a). In same points, the metallization roughness is comparable to its thickness, resulting in one or more MOSFET cells almost uncoated, without conducting layer on top (Fig. 126b).

- On the other side, T07D17 components have been inspected only after failure, so we do not have information about the crack evolution during aging. However, at failure we could observe that here vertical cracks are finer than the ones observed in SPD06 failed modules and branch out deep in the Al. At this stage horizontal cracks propagate along the interface with the oxide and the Si bulk (Fig. 126c and Fig. 126d).

These models of crack propagation along grain boundaries could explain both the metal degradation morphologies during thermal cycles and the associated local rise of metallization resistance and temperature. In the case of SPD06 devices, aging seems to be more localized at surface level in the Al metal layer, where larger and larger voids interrupt the current flow through the conductor until a failure event. Whereas, cracking in T07D17s systematically affect also the deeper layers, the oxide and the semiconductor 127.

It is difficult to compare the different failure mechanisms and draw a certain conclusion about the failure origin because the devices under study have been tested at different aging conditions. Anyway, we can suppose that this difference in the crack propagation models is due to the fact that the SPD06s have been depackaged before test, in order to follow the metallization surface evolution during aging, whereas T07D17 power modules remained closed in

the mold compound, as during the normal operation. Moreover, in T07D17 modules, the metallization is coated by a SiO_2 passivation layer.

We can, therefore, suppose that the presence of the mold compound and the oxide passivation slow down the groove broadening. However, despite its perfect adherence to the metallization and its stiffness, the oxide passivation layer does not completely block the grooving at the GBs. SGs formation and cracking are observed during aging in the passivated zones, as in the bare ones (Fig. 128). The formation of SBs means that passivated areas are subject to the same initial dislocation-based plasticity mechanisms observed in the bare metal. On the other hand, crack initiation and propagation is more difficult to explain since the adherent passivation film is expected to shut-out surface diffusion and thus the grooves opening. However this phenomenon has already been observed in studies on self-passivated thin films [Kra02], which proves that diffusion at GBs remains efficient even in a context of diminished surface diffusion. These results have been also confirmed by the statistical measurements on crack propagation, detailed in the following.

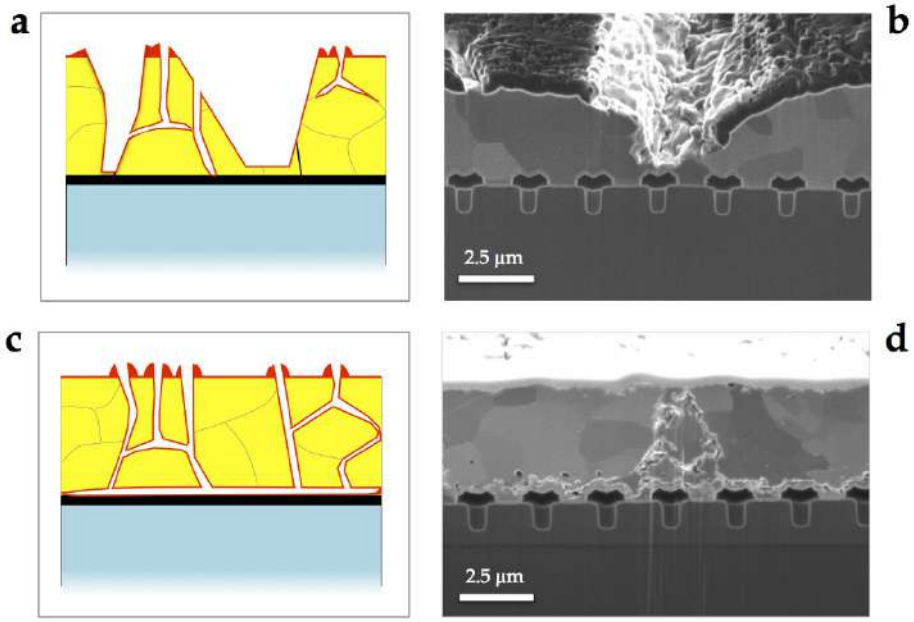

Figure 126: Crack propagation models through the Al layer at failure. (a) For SPD06 power modules at the final aging stage until failure, fatigues cracks running from the surface along the grain boundaries become broader and broader. (b) SIM cross-sectional image of the cracked metal in a failed SPD06, showing a crack width on the same order of the metallization thickness. (c) In T07D17 failed power modules, finer vertical cracks branch out and propagate horizontally all long the MOSFETs region. (d) Relative SIM cross-sectional imaging form a 70°C aged module.

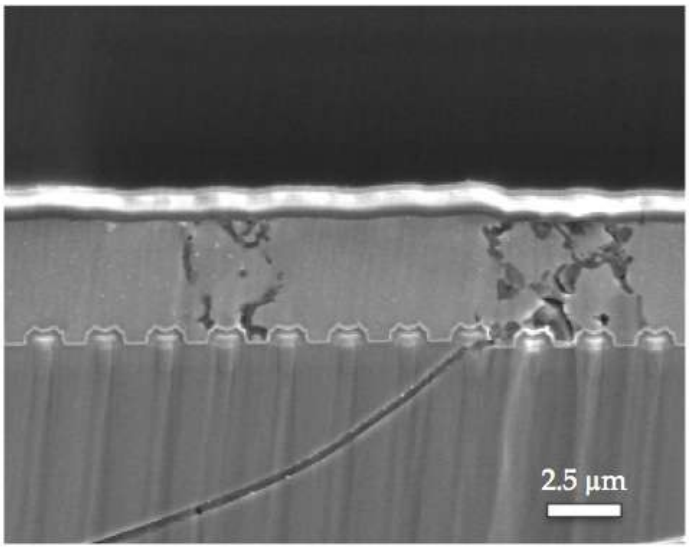

Figure 127: SEM cross-sectional image showing the whole metal-oxide-semiconductor crossed by cracks in a 70°C aged T07D17 module.

5.2.6 *Passivation and temperature effect on crack propagation*

The oxide passivation coating, around the bonding areas, in T07D17 devices is supposed to limited the Al diffusion at surface [Cia02], and consequently along the GBs, preventing the Al reconstruction phenomenon. Fig. 128 shows the crack propagation in a passivated (a) and bare - the metallization is coated only by the mold compound - (b) zone.

In order to quantify these cracks, we have established the method described in section 4.2.1.1, which consists in measuring the number of cracked and undamaged vertical GBs, and the number of MOSFET cells horizontally cracked and undamaged. The result of the statistics is summarized in Fig. 129. The plot clearly shows that cracks in the passivated zones thin out, especially in the case of horizontal cracks. These observations suggest that horizontal cracks initiate and propagate once the vertical ones reach the transistor area, starting from the metal surface. If we take as reference the naked metallization and we assume that vertical cracking saturates when 30% of GBs are cracked, then we can explain why horizontal cracks are reduced in the passivated parts, where a minor number of vertical GBs is cracked (20%).

The temperature effect is also more pronounced in the case of bare metallization. Here the horizontal crack percentage in the analyzed sections is significantly higher at 70°C then at room temperature. This difference is lowered in the passivated parts.

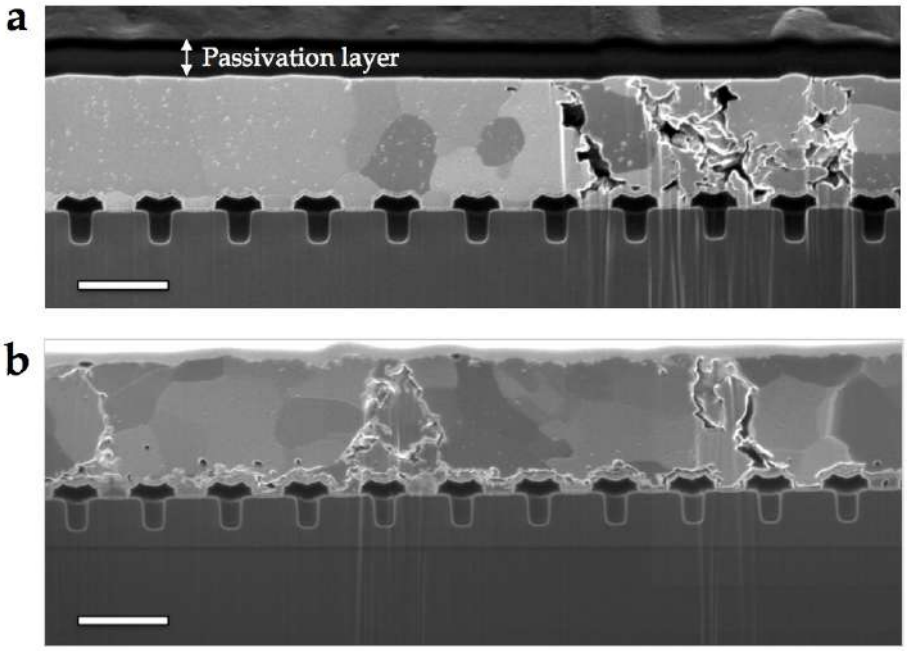

Figure 128: Cross-sectional SIM images of the (a) passivated and (b) bare Al source metallization, showing a localized propagation of vertical cracks in the first one and a generalized degradation in the second one, with horizontal cracks branching out all along the metal-transistor interface. Scale bar: 2.5µm

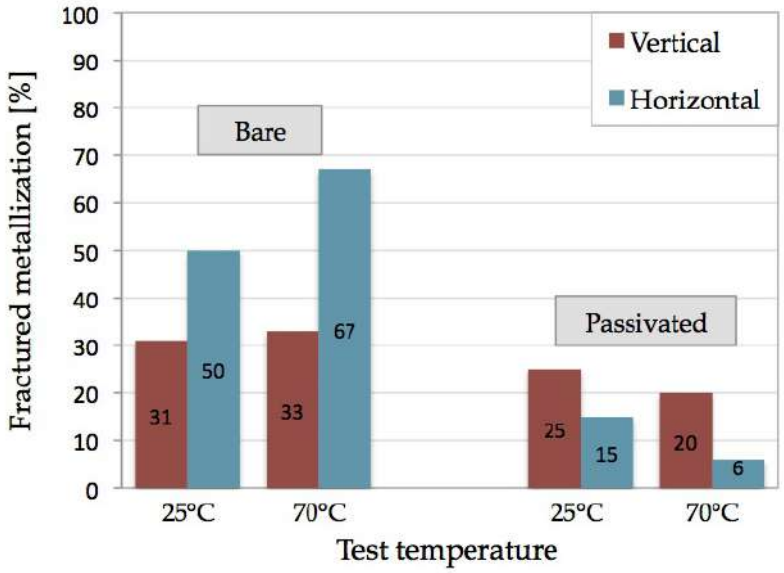

Figure 129: Metallization crack statistics for a T07D17 module aged at 25 °C and 70 °C, in non passivated –bare– (left) and passivated (right) zones.

We can conclude that, as expected [Cia02], crack initiation and propagation in the source metallization of LFET1T modules is controlled by the oxide passivation layer. However, this coating does not completely block the intergranular diffusion of Al along the GBs and discontinuities in the passivated metal – even if reduced in number and more localized compared to the bare parts– can generate a peak thermal stresses that can accelerate the aging process.

5.3 WEAKENING OF THE BONDING CONNECTIONS - METALLIZATION UNDER THE BONDING WIRE

The surface reconstruction of the Al metallization away from the bond connections is one of the aging effect that has been reported since the early times of microelectronics and considered as one of the main failure mechanisms of modern power modules[Cia02] [Phi71] [San69].. We also reported this metal aging effect in the LFET1T power die studied in this work in the vicinity of the bond wires. This surface reconstruction is well described by existing models of Al atom diffusion along the grain boundaries [Gao99] [Mar14] leading to heavy fatigue crack propagation through the Al thickness. This aging mechanism and can provide an explanation of the increase in the metal resistance detected at failure.

However, a large part of the Al source metallization, located under the bonding connections, is not taken into account in these models. One reason is the poor accessibility of this zone. SPD06 and T07D17 devices include pure Al bonding wires, respectively 6 and 8, connected to the active zone of the power modules. They are 400µm in diameter and they are cold welded by ultrasound to the 4µm thick Al source metallization, for a total bond area of $\sim 0.3mm^2$ each connection. We expect, therefore, that plastic deformation induced by the bonding process complexifies considerably the situation in the Al metallization under the bond wires prior to aging. At the same time, during the normal device operation and the electro-thermal tests this zone is particularly critical because of the highest currents and temperatures concentrating under the bond connections.

A wide literature exist on wire bondings, describing the influences of techniques, geometries (sections and loop shape [Cel11], composition [Agy11] and bonding parameters [Lum06]) on the adherence and long-term reliability of this contact through thermal or thermo-mechanical stress. In our case, the wire is made of pure Al, bonded on an Al metallization, which excludes all the potential problem of intermetallic formation [Xu11]. The metallization is also reinforced with Cu and W atoms. This, added to the fact that the grains in the wire are larger than in the metallization (section 4.2.2) let us anticipate that the wire will be softer than the metallization.

Despite several authors have studied the wire bonding process and its impact either on the wire structure itself, the metallization or the cracks developing at the interface [Bro15] [Krz89] [Goe10], to the best of our knowledge no systematic studies of the granular microstructure of the metallization under the bond wires has been published. However, such resolution could give us useful feedback about the bonding quality before and after aging or about the initial deformed condition of the bonded metallization. This zone is partic-

ularly difficult to access and investigate by electron and ion microscopy, due to the presence of the bonding connections that are 100 times thicker that the Al metallization below. Recent studies [Yam07] showing a grain mapping of wires observed in cross-section confirmed that the grain size in the wire was in the range of a 100µm, much larger than in the metallization. This grain size clearly decreases near the interface and also under the cutting tool (lower and upper portion of the wire, respectively), but the authors did not focus on the interface microstructural changes. Thanks to the original sample preparation that we set up in this work to locally reduce the wire thickness before FIB sectioning, we have been able to disclose the metallization under the bonding wires in the as-is and aged power modules. This also allowed us to compare the microstructure of the metal away and under the bonding wire, using ion channeling contrast and the grain orientation techniques.

5.3.1 *Initial wire-metallization interface*

Before bonding process, the wires are in the form of Al cylinders of ~ 400µm of diameter. During the bonding process, a bond force of ~ 10N is applied to the two sides of the cylinder extremity along the black fleshes in the schema in Fig. 130a, representing the cross-section of the wire on the metal-oxide-semiconductur layered structure. The result is a total bond area of ~ 0.3mm² with two tail sides (Fig. 130b) and an elliptical profile (Fig. 132c). Cross-sectional SIM and TEM investigation of the bonding area before electro-thermal aging allowed us to observe at high resolution the wire-metallization interface and the Al-Al microstructure. Fig. 131 shows a cross-section through a bonding wire before aging. The white arrow points out the transition from the non-bonded to the welded region, in line with the literature images for analog bonding processes [Cia02]. A higher magnification of these two zones is reproposed here, in Figs. 132a (non-bonded part) and 132b (bonded part). The very first observation which arises from this kind of images is that a wire-metallization interface is still visible passing from the non-bonded to the bonded part. An Al-Al interface exists even in the central areas of the bonding, meaning that no Al atoms interdiffusion occurred between the two metallic parts during the bonding process. If the bonding had been perfect, the wire material would not have been distinguished from the Al metallization [Cia02]. Here, instead, the bonding interface is characterized by initial imperfections which have been linked to the presence of small cavities and Al oxide residues, according to our SIM/SEM images and TEM chemical analysis. The most probable explanation for this presence is that the Al native oxide is not fully broken during the bonding process at room temperature, avoiding the interdiffusion of the Al atoms and the formation of a perfect bonding. The Al-Al interface delimits two

different granular microstructures. The grains in the bonded metallization are finer than the ones in the bond wire (Fig. 132b), and also in the non-bonded metallization part (Fig. 132a). This is due to the severe plastic deformation imposed by the bonding process to the Al metallization. TEM grain orientation mapping of the metallization under the wires demonstrates that the grain refinement here is real, and is not related to a FIB artefact (as for the subgrains formed in the first stage of the electro-thermal aging away from the bonding wire).

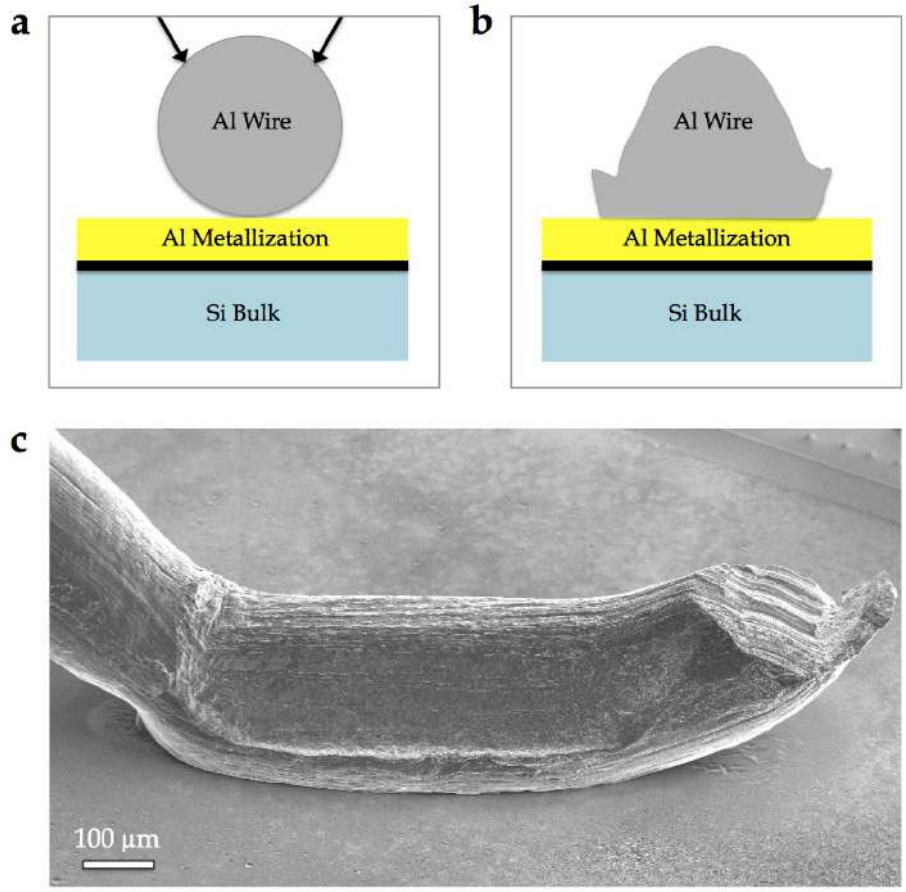

Figure 130: Cross-sectional schema of the cylindric wire on the top metallization (a) before and (b) after bonding process. The black flashes in (a) represent the force direction during the bonding process. (c) Lateral view SEM image of the elliptical bond area.

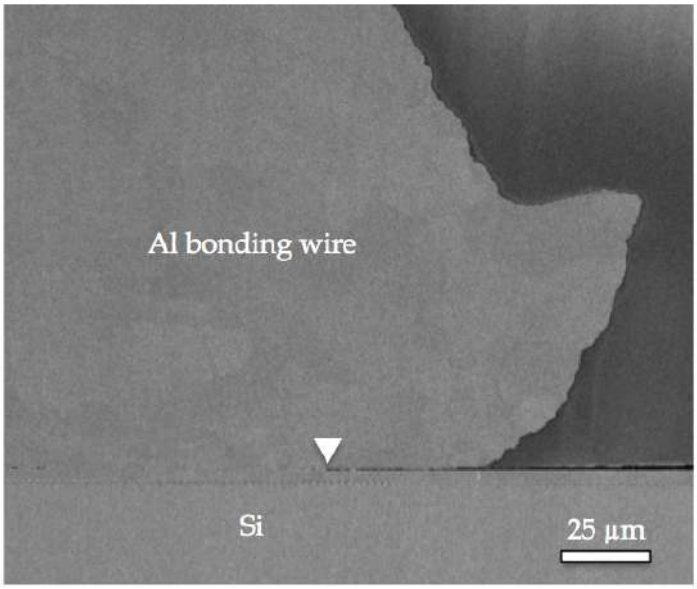

Figure 131: SEM Cross-sectional image of the tail side of an as-processed wire on Al metallization, showing the transition from the non-bonded to the welded region

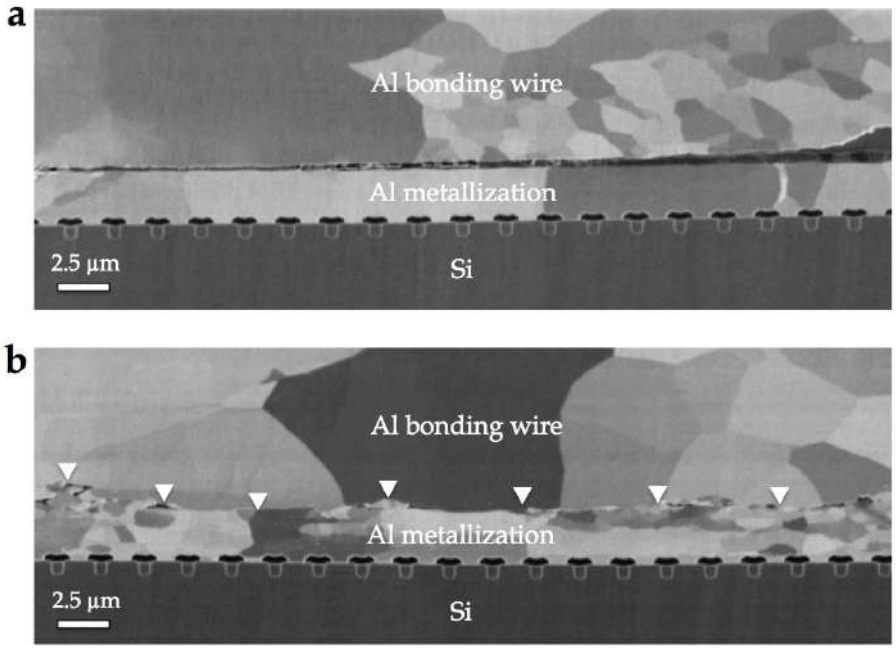

Figure 132: High magnification SIM image of the (a) non-bonded region and (b) the welded one, showing that no Al-Al interdiffusion between the two metallic parts occurred during the bonding process.

5.3.2 *Initial Plastic deformation*

On the basis of the previous considerations, SIM and SEM cross-sectional images gave us a useful feedback about the bonding process in the as-processed LFET1T devices: the Al-Al bond is not perfect and the two metal structures remain overall separated by a finer interface composed by native Al oxide residues and small cavities. Moreover, due to the bonding process, the metallization layer undergoes a severe plastic deformation prior to aging. These images give also a useful feedback about the stress distribution during the bonding process. According to the schema in Fig. 130a, the maximum stress in the bond wire concentrates in the center, resulting in a uniform distribution of the stress in the metallization under the wire. This is demonstrated by the fact that overall the Al metallization thickness is uniform all along the wire-metallization interface in the analyzed sections (Fig. 133a, c). If not, we would have observed an ellipsoidal profile similar to the one in Fig. 133b, with a significant and non-uniform thinning of the central part of the metallization under the wire, compared to the initial metallization thickness away from the bonding wire (represented by the red dashed line as a reference). In our case, instead, we have observed an uneven wire-metallization interface profile characterized by the succession of straight segments and extrusion and compression parts (Fig. 133c). As proof of this, the difference between the thinning and bulging metallization areas is almost zero in the analyzed cross-sections. This also means that plastic deformation is not uniform along the applied stress of the wire bonding perpendicular to the wire-metal interface. It is $\sim 5\%$, if we consider entire sections and ranges between 5% and 25% in average if we calculate the deformation in smaller FIB sections, confirming that plastic deformation in the metallization under the bond wires is variable and the wire-metallization profile is highly uneven. These values are obtained on a total section area of $\sim 1300\mu m^2$, which is small compared to the volume impacted by the wire bonding ($\sim 0.3mm^2$), but not negligible. Taking in account the pressure applied during the ultrasonic process, the average compressive stress on the metallization is $\sim 30MPa$. This stress is much smaller than the yield stress of a commercially pure Al with a grain size in the range of $1-2\mu m$, typically in the range of $100-150MPa$ [Tsu02]. To explain that significant plastic deformation occurred under this small load, we have to assume that only a fraction of the $0.3mm^2$ of the metallization surface was truly in contact with the wire. A very coarse estimate would lead to a third of the metallization being impacted by wire-bonding plastic deformation. This also explains why the surface is deformed very inhomogeneously. The fact that only a portion of the wire is welded to the metallization and that this portion decreases upon aging is supported by previous experiments [Goe10]. Knowing more precisely the

mechanical properties of both the wire and the metallization (which depends heavily on impurity content, grain size, etc.) would be needed to perform a better estimation of the impacted metallization surface, but predicting the very heterogeneous deformation of the interface would remain out of reach anyway.

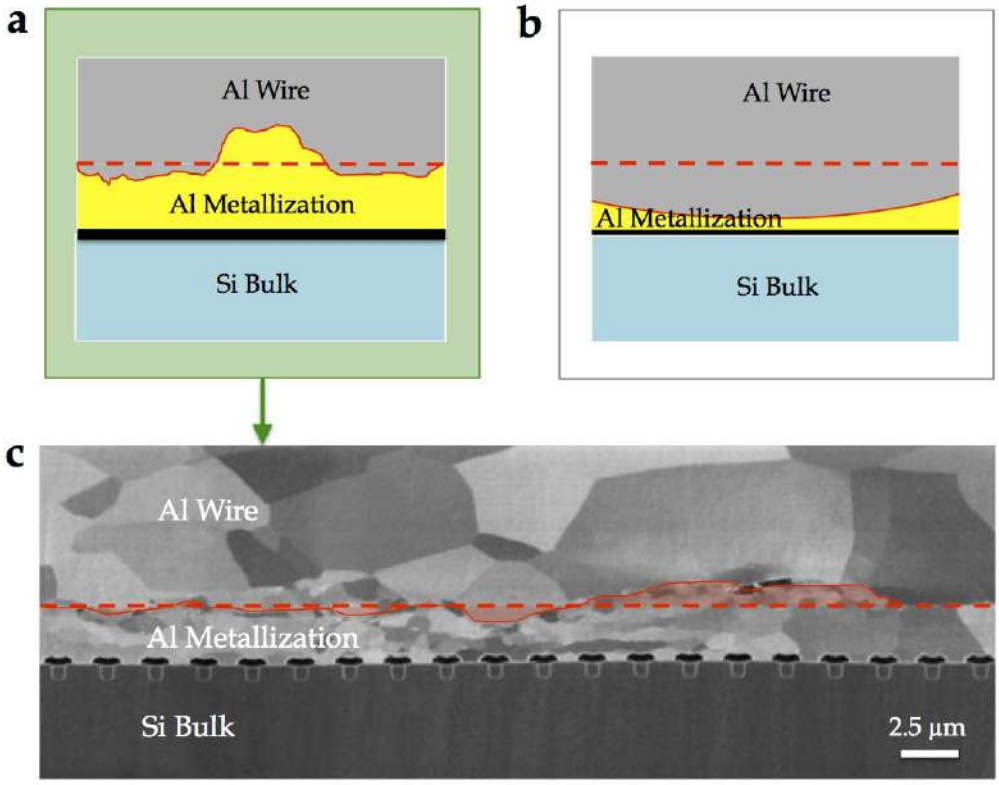

Figure 133: (a) Schema of the wire-metallization interface corresponding to (a) a uniform and (b) non uniform bonding stress along the interface. (c) SEM image of the uneven wire-metallization interface of a LFET1T power device, according to the schema in (a).

5.3.3 *Aging in the metallization under the bonding wires*

We have asked ourselves if the initial plastic deformation in the contacted metallization could influence and favour aging in these bonding areas. This could happen if grain shrinking multiply GBs, then the number of potential crack paths. However, the presence of an Al/Al interface complicates this issue.

When plastic deformation is weak ($\sim$ 1%), only dislocation-based phenomena and SGs formation take place. On the other hand, when several percentage of deformation are applied, we can expect a grain structure rearrangement, with new cell formation, and a grain refinement. The results of our measurements state that plastic deformation due to the bonding process can locally reach high values, up to 20 or 30 %, that are enough to induce grain fragmentation. This has been confirmed by ACOM-TEM mapping, showing a a refinement of the initially large bamboo grains, with the formation of new grain domains having a relative misorientation of $\sim 30°$. Despite the GBs multiplication, associated to new potential paths for crack propagations, we have not observed an evident increase in the number of cracks in the metal under the wires. They are, on the contrary, limited to the zones chracterized by a loss in contact between the wire and the metal (Fig. 134b), where the surface metallization is free and diffusion phenomena can favour fatigue vertical crack initiation and propagation, as we have seen in naked metallization.

We have, then, focuses on the effects of aging on the grain size. According to Thompson theories on structure evolution during thermal processing of polycrystalline films [Thooo], we should expect a grain growth during aging from an initially smaller grain size. A grain growth in the bonding region could change the wire-metal interface, favouring an improvement of the bonding process. However, no significant grain growth have been observed in the metallization under the bonding wire during aging. This can explain the systematic presence of a well-defined wire-metal interface also in the modules that underwent electro-thermal aging. These consideration are only based on qualitative results, a consistent statistics on the grain size before and after aging should be performed.

5.3.4 *Crack propagation during electro-thermal aging*

High resolution imaging by ion and electron microscopy shows that the metallization under the bond wires is significantly different from the naked metallization, as the bonding process induce plastic deformation prior to aging. Moreover, during the bonding process, the native Al oxide covering the metallization layer is not fully broken. The result of the bonding is therefore an Al-Al interface, consisting in small cavities and Al oxide residues (Fig. 134a),

which prevents the interdiffusion of Al atoms between the two metallic parts. This is a possible explanation of the fact that no signs of bond wire fatigue, heel cracking or complete lift off [Cia02] have been detected in the failed modules. During aging, all the electro-thermal and/or thermo-mechanical load is transmitted to the metallization beneath the bonding area and affects the wire-metallization interface. This basically occurs by propagation of fatigue cracks along the initial bonding imperfections, causing a reduced contact between the wire and the metallization (Fig. 134b). Cracks also run perpendicularly to the interface under the wires along the grain boundaries, as in the metallization away from the bonding area.

The high density of metal breaks revealed by the tomography stacks can explain the increase of the R_{dson}, which implies that subsequent electrical pulses will generate more heat, thus more deformation, and crack propagation. The same aging mechanisms are observed in devices tested at room temperature and at 70°C, but at different number of cycles. This means that the mechanisms are probably the same and they are just accelerated by the overall temperature increase, explaining the lower life-time of the components aged at 70°C. In these tests, the self passivation of the Al layers are observed as the thickness of the initial oxide keeps increasing upon aging, which is in agreement with the observation of oxygen content increase in the metallization of diodes undergoing electro-thermal aging [Bri16]. However, contrary to what has been observed by these authors, this growth does not prevent the propagation of cracks. In our devices, most of the horizontal crack propagation remains confined at the metallization/wire.

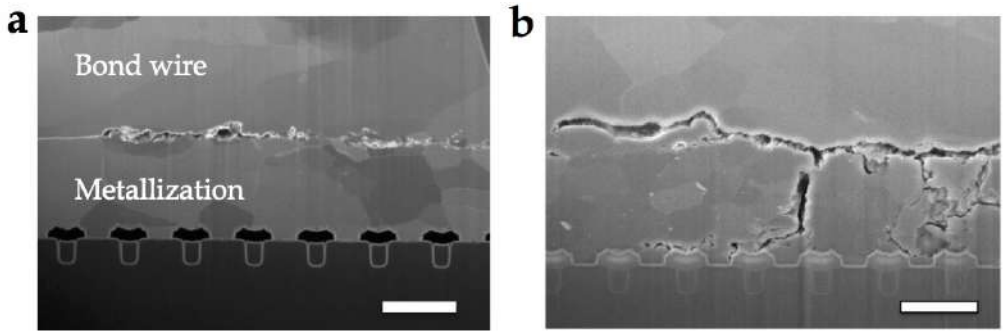

Figure 134: Wire-metallization interface (a) before and (b) after aging (at 70°C). The Al-Al interface of as-processed modules presents initial imperfections, consisting in small cavities and native Al oxide residues. During aging, cracks propagate along these imperfections, causing a reduced contact between the wire and the metallization. Scale bar 2.5µm

This is a strong indication that this interface is weak. Indeed, if the Al-Al bonding were initially perfect, the crack would deviate to the softer material that is here the wire, because of its larger grain size. This is only observed scarcely, and often the crack deviates again towards the interface, creating small cavities above it, as showed in Fig. 134b. Further statistical analysis is required to better assess the proportion of weak interface vs perfectly welded Al-Al contact area, but our study clearly show that weak bonding is linked to the presence of oxide, and this favor an horizontal crack propagation at the interface.

The amount of plastic deformation does not change significantly upon aging in the analyzed sections under the bonding wires. As observed in the metallization away from the bonding connections, the aging mechanisms are driven by a severe metal breaking due to an enhances self-diffusion of Al atoms. On the contrary plastic deformation induced by the electro-thermal load is not significant and does not explain the local increase in the R_{dson}.

6

CONCLUSION AND PERSPECTIVES

The main goal of this thesis was to assess the aging mechanisms of the Al-based (or Al alloys) source metallization in power MOSFET devices. The electro-thermal and/or thermo-mechanical aging of the metallic parts is one of the intrinsic limiting factors for the long term reliability of power MOSFETs. During the on-off operating cycles, the temperature changes result in mechanical stress due the difference in the coefficient of thermal expansion between the metal and the oxide/semiconducting parts. Since Al has a low mechanical yield stress, the source metallization is expected to deform plastically even at moderate temperature excursions (200 °C), while the Si remains in its elastic domain. As aging progresses, the degradation of the metal increases its resistance, which in turn will increase the temperature of the device in the on-state and therefore augment the mechanical stress. This feedback causes a degradation of the top metal through specific processes.

We have investigated the Al degradation mechanisms in a specific case study: LFET1T power MOSFETs from NXP Semiconductors, used as lightning switches in the automotive industry. This work has been motivated by real industrial exigences, as the comprehension of the LFET1T technology limits would serve as reference for new MOSFET generations that are currently under development.

Standard qualification tests have been performed by NXP at different temperatures in order to determine the device life-time and localize the critical points. In parallel, reference LFET1T power dies, unpackaged and disconnected from the control die, have undergone extreme short-circuit conditions in a dedicated test bench, developed by the Satie laboratory with the aim to monitor the thermo-sensitive parameters during aging and, at the same time, follow the evolution of the metal degradation. Common failure mechanisms resulted from these tests, but at different life-times, involving mainly the metallization around the bonding connections.

Our contribution consisted in characterizing the metal microstructure under electro-thermal aging, using dedicated physical metallurgy techniques, such as ion and electron microscopy and grain structure mapping. We have set up specific characterization and quantification methods to assess the main feature influencing the device aging: fatigue crack propagation and plastic deformation in the metallization due to the bonding process.

In particular we focused on the bonding areas. This has required the use of dedicated sample preparation in order to preserve the Al/Al bonding, particularly fragile in case of aged devices. The original preparation method that we have proposed, combines a preliminary 45°mechanical polishing with final FIB cuts to locally reduce the thickness of the bonding wires and disclose the metallization below, without introducing preparation artefacts and altering the metal microstructure. This allowed us not only to assess the initial bonding quality in reference modules, but also to inspect the bonding area evolution during aging, even if fragile. To increase the observation area with respect to the FIB-based preparation and gain some statistical data, we also performed ion beam polishing in a cross-polisher system.

During our characterizations, we have systematically compared the metallization microstructure away and under the bonding wire, before and after aging.

Aging of the Al metallization away from the bonding wires

- During the first stage of aging, the initial "bamboo" grain structure structure undergoes a limited dislocation-based plastic deformation, that explains the apparition of subgrain boundaries leading to an apparent grain shrinkage in FIB imaging. Aging is dominated by an enhanced diffusion of Al atoms along the grain boundaries. This mechanisms is at the base of initiation and propagation of fatigue cracks running perpendicular to the surface down to the Si substrate, following the initial grain boundaries.

- At failure, cracking is different in bare, mold passivated and SiO_2 passivated metallization.
  - In bare metallization (from unpackaged power dies under test), GB grooves become equivalent (or even larger) to the inter-transistor spacing.
  - Mold passivated metallization is even fractured, but cracks are finer, and they branch out and propagate horizontally at the oxide/semiconductor interface.
  - A stiffer and more adherent oxide passivation layer slows down GB diffusion but does not completely stop it. Cracks are more localized and concentrated, but still present.

  What is the best in terms of electrical and thermal dissipation through the metallization layer is still an open question. Crack propagation is slowed down by the oxide passivation layer and it is concentrated in specific zones. However, could this induce more harmful peak thermal stresses and provoke an abrupt failure event?

Aging of the bonding area

- The initial bonding area is characterized by the systematic presence of an uneven wire-metallization interface, made out of Al-oxide residues and small cavities. This means that the bonding is not perfect and no Al-Al interdiffusion occurs during the cold-bonding process.
  Aging accentuates the initial bonding defects, that are the starting point to horizontal crack propagation at the wire-metallization interface, causing an even more reduced contact between the two metals. In this poorly-contacted zones, cracks can also propagate vertically down to the Si bulk following the grain boundaries, as in the naked parts. Cracks remain limited to the wire-metal interface and do not propagate in the wire. This is a strong indication that the Al/Al interface is weak and its presence induces specific degradation phenomena. If the bonding were initially perfect, cracks would deviate to the softest material that is here the wire, with a larger grain structure.

- Under the wire, the initial metallization microstructure is finer than elsewhere (naked metallization and wire). The rearrangement of the grain structure, proved by grain orientation mapping, is due to an important and not uniform plastic deformation imposed by the bonding process. We have measured this plastic deformation to be 10% in average in compression, with local peaks up to 30%. Contrary to our expectations, this initially deformed microstructure does not significantly change upon aging and does not influence crack propagation to the wire.

- The local increase in temperature during aging is not sufficient to influence the wire-metallization interface. This interface remains systematically present during aging and no real grain reconstruction between the wire and the metallization has been observed until melting.

Crack propagation in the Si substrate

Thermal runaway due to metallization degradation and resistivity increase seems like the major failure mechanism. A severe crack propagation has been observed in the Si substrate, around and under the failed wires, where hot spot are detected. We have distinguished primary and secondary cracks:

- Primary cracks are smaller and filled with Al. This is probably due to diffusion of melted Al inside the brittle Si substrate during runaway [Jac13].

- Secondary cracks are larger and not filled with Al. They probably occur during the cooling down of the whole device, when the Al can not extrude, after the final failure.

This observation may indicate that, even after the formation of primary fragile cracks in Si, the device keeps conducting current and remains hot for periods of time long enough to create Al melting and recrystallization inside the Si substate.

In conclusion, the aging of the Al source metallization in LFET1T technology can be associated to two phenomena:

- a heavy metal reconstruction characterized by the generation of GB cracks that are specific of Al-based power device and location.
- A systematic poor bonding of the wires due to Al natural oxide, that is never broken until complete Al meting (associated with the device's failure) and along which, parallel cracks propagate.

Both mechanisms concur to increase the local resistivity and to favor hot spots that can lead to the melting of the Al and to the Si substrate fracture.

Although changing industrial processes are difficult and definitely beyond the scope of this thesis, our study suggests possible ways to improve the reliability of this type of device and also some future paths to complete the present conclusions.

- The cold-bonding bonding process does not provide a perfect Al/Al contact and the presence of a defective interface remains until failure. At that point only, a real reconstruction of the metallization-wire microstructure is achieved. Ideally, the Al oxide should be broken during or just prior to the wire bonding. This could be achieved by performing a reduction of the metal and wire, or by doing this bonding at high temperature, or may be changing the wire shape to create local spikes that would create enough stress concentration as well as increasing the adherence surface to initiate a grain growth (by local diffusion) at the interface. We showed that a significant plastification of the metal under the wire is probably very bearable for the device.
- A change in the metal type would also make a difference. Copper on copper bonding should not encounter this type of adherence problem. However, it is well known that Cu interconnects require a much more severe chemical insulation from the Si substrate.
- Our few attempts to quantify the info about the stress increase in the metal during aging are insufficient. Curvature experiments to measure the stress and to possibly correlate it (or not) with the surface reconstruction might be useful.

- Passivation of the metallization by an oxide seems to reduce the crack density and increase the life-time. However, it does not seem possible to completely passivate the metal around the wire bonding feet, leaving and possibly concentrating metal degradation to this location. Also, we don't have enough statistics on the topic and the main question is wether this type of passivation may favor earlier catastrophic events by concentrating the hot spots. In other terms, for an increased number of cycles, the time at which a failure occurs may strongly diverge.

Part I

APPENDIX

A

CONVENTIONAL CROSS-SECTION TEM SAMPLE PREPARATION

There are many ways to prepare a TEM specimen, depending on what we want to study and the characteristics of the material [Wil09]. No matter the method used, the primary requirement is that the specimen must be ultra-thin (typically ~ 100µm or less) to be electron transparent. Of course, heavy materials (Au, W, Pt,...) need to be thinned more than light ones (Be, Al, Si,...), and the type of microscopy (conventional, high-resolution, chemical analysis, holography,...) also requires different thicknesses. "Conventional TEM preparation" refers to several different methods that involve mechanical thinning (by grinder or tripod) followed, if needed, by an ion milling to prepare bulk electron transparent specimen for TEM inspection [Wil09].

In this work, we have distinguished such a preparation from the lamella preparation by ion beam in the FIB-SEM microscope. The dual beam microscope offered us the possibility to precisely localise the area of interest (the Al metallization) and directly extract and sample lamella for the successive TEM investigation and grain structure mapping in TEM. These lamella include the Al metallization layer, that is 4µm thick, and, at most, a comparable thickness of Si bulk. In case of wire-metallization lamella preparation, the Si is even thinner. This turned out to be an issue during our in situ heating experiments: the leftover of the Si substrate was too thin to induce significant stresses in the Al layer and a scarce dislocation activity was detected.

For this reason, we chose to perform in parallel a conventional sample preparation, that allowed us to obtain a final ~ 100µm thin cross-section foils, preserving the entire Si bulk thickness. This mode of preparation is well-suited for a thin film deposited on a Si substrate because the Si provides a stiff support during mechanical polishing. Another advantage is that the electron-transparent areas are usually much wider than the one accessible by FIB. On the other hand, fragile interfaces, such as the wire-bonding metallization interface, may not sustain such mechanical polishing, and be prone to an alteration of its microstructure. This is why tripod polishing was specifically dedicated to the naked die.

The main steps of the preparation are shown in Fig. 135 and described in the following. It consists in a mechanical thinning by tripod system and a final ion milling by precision ion polishing system (PIPS).

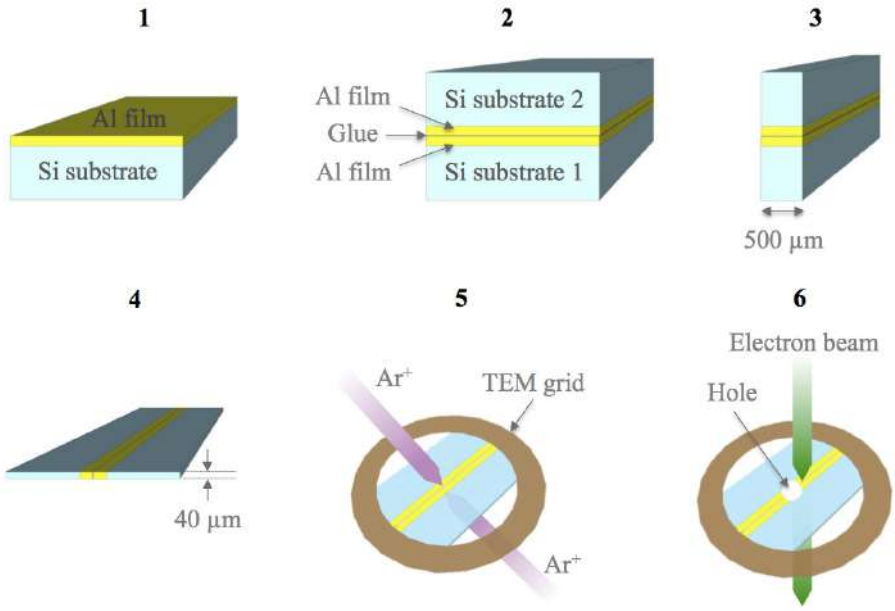

Figure 135: Sketch of the conventional TEM sample preparation procedure.

1. The sample surface is carefully cleaned in solvent in order to obtain a perfectly clean surface.

2. Two pieces of substrate-film are glued together using an epoxy glue (G1 from Gatan), in order to prevent polishing damages on the metallic film. The sandwich is introduced in a press to obtain a very thin glue film and the whole mounting is placed in a oven at 80°C for 2 hours to ensure a proper glue polymerization.

3. The sandwich is then sliced by diamond wire saw into ~ 500µm thick pieces to reduce the block thickness for the polishing step.

4. The first face of the piece is thinned down and polished by tripod system, using progressively finer diamond lapping paper (30µm down to 1µm) in order to obtain a scratch-free surface. Then the sample is turned upside down an the second face is thinned and polished until a final thickness of a few tens of microns.

5. The two side polished thin foil is glued using a fast-curing epoxy on a TEM copper grid and transferred in the PIPS for the final ion milling of the cross-section. A dual argon beam system is focused from the top and the bottom on the middle of the sample in order to create an hole at the film-glue-film interface.

6. By playing on the beam angle and energy parameters (generally we start the milling at $\pm 6°$ and 6 keV and then we finish at $\pm 4°$and 3 keV), at the edge of the hole the sample should thin enough to be electron transparent for the TEM observation.

Classical tripod polishing may skip this ion-beam final milling by using finer diamond papers (0.5µm) and colloidal silica, but involves more risk in obtaining an artifact-free Al layer (mechanical damages). Fig. 136 represents a low magnification TEM image of the electron transparent region around the PIPS hole: we can notice the two metallization films on the Si bulks and small glue residues between them. During heating in the TEM, both epoxy glues are temperature-resistant enough (450°C is generally considered slightly above their temperature application range, but since there is no large stresses on the sample, adhesion remains sufficient). If this would not be the case (heating above 500°C for instance), a small drop of alumina- or zirconia-based cement is used to attach the sample to its grid.

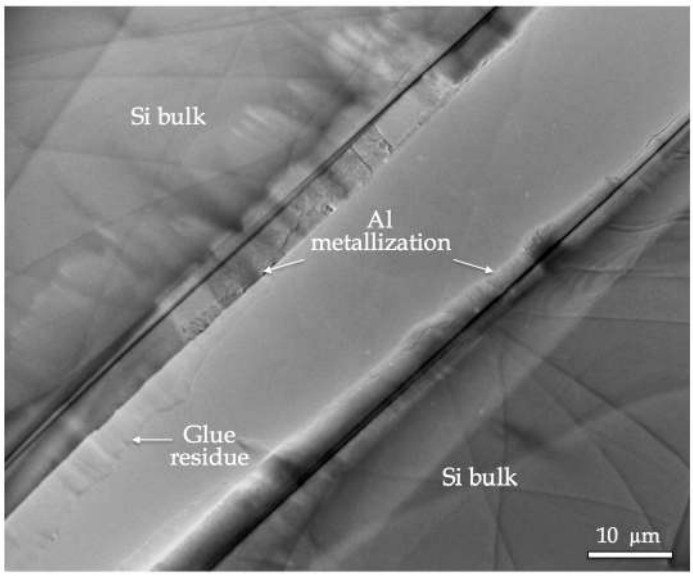

Figure 136: Low magnification TEM image showing the electron transparent cross-section of two bulk-film-film-bulk sandwich prepared by tripod and ion milling.

B

CURVATURE EXPERIMENT

During curvature experiments, metallic films deposited onto Si or ceramic substrates undergo thermal-only cycles. The difference in CTE between bulk and film is sufficient to strain the film, first elastically and then plastically. This generates a curvature (Fig. 139b), that can be directly related to the stress variation in the film using the Stoney equation [Sto09] [Jan09].

$$\sigma_f = \frac{E_s t_s^2}{6(1-\nu_s)t_f R} \tag{10}$$

where σ_f is the average biaxial stress in the film, E_s, ν_s and t_s are, respectively, the Young's modulus, Poisson's ratio and thickness of the substrate; R is the curvature measured by the laser; t_f is the film thickness. The robustness of this equation and measurement method is in the fact that no assumption is needed regarding the film's elastic properties, as only those of the substrate are needed [Leg03] [Fli87]. A typical thermal cycle where the film yields first in compression (during heating) before being stressed in tension (upon cooling) is shown in Fig.137.

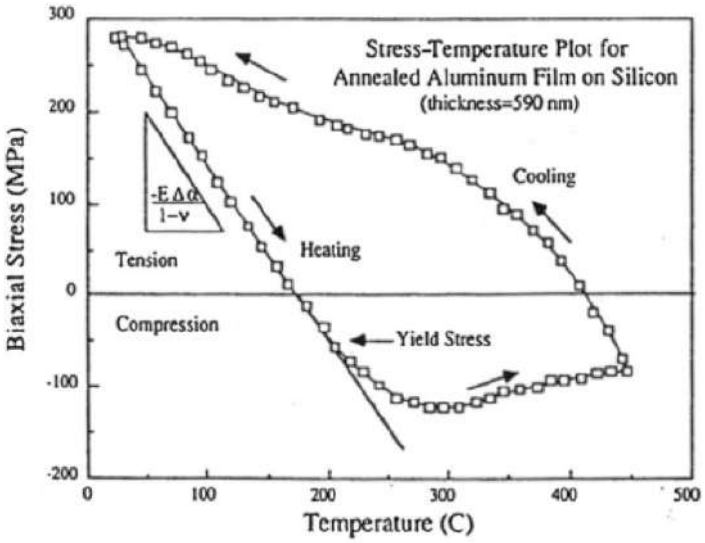

Figure 137: Typical stress-temperature cycle for a 590 nm thick poly-crystalline Al film on oxidized Si substrate ($T_{max} \sim 450°C$) [Fli87].

In this work, thermal cycles were performed under vacuum between -190°C and 350°C in a home-made test bench based on a KSA MOS laser reflectometer and an ARS cryo-holder. The tested samples are reference power dies, without the bonding wire connections. We considered it, in a first approximation, as an equivalent of a 4 micron thin Al film deposited on a 260 micron thick Si substrate. The first experiments that we performed (Fig. 140) showed that this may be wrong.

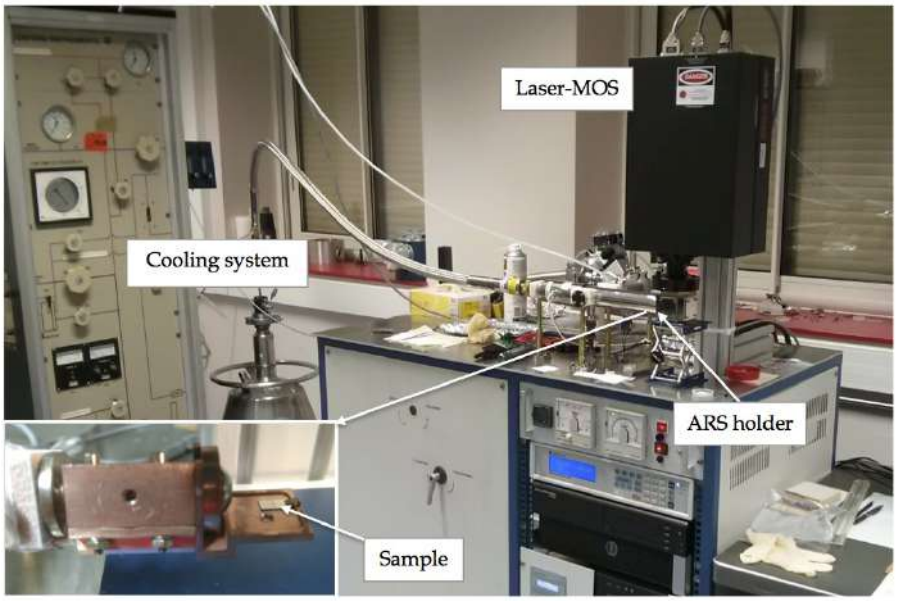

Figure 138: Laser reflectometry test bench assembled for curvature experiments. The sample (reference SPD06, before assembly) is placed under vacuum on a Cu support, inside the ARS sample holder.

Fig. 138 represents the main parts of the experimental set-up, described in the following:

- KSA MOS laser module, from K-Space.
  The module focuses several laser beams on the reflective surface (film) of the sample (Fig. 139b) and measure the curvature imposed by the Al film to the Si substrate by laser profilometry (on the base of the laser spots divergence or convergence - Fig. 139c). The laser unit and its operating principle are showed respectively in Fig. 139a and b.

- ARS cryogenic sample holder.
  It allows to heat the sample up to 525 °C and cool it down until the liquid nitrogen temperature. This temperature range is significantly higher with respect to the real operating temperatures of power devices [Pie09].

However, the T gradient is set to 20°C/min, probably orders of magnitude lower than the real ones [Sau08]. An innovative faster set-up, based on a high speed camera, has been recently developed by the KAI center (Villach, Austria) [Isl15] in order to monitor the material behavior at heating rates comparable to the ones occurring during usage.

- PC station. Two computers communicate respectively with the holder controller and the laser module.
- Vacuum pump system. The whole system is under vacuum during the thermal cycles.

Fig. 140 shows one of the cycles that we have performed between -190°C and 350°C. Starting the experiment at -190°C, the metallic layer yields in compression (c) during heating, before being stressed in tension (t) upon cooling. As in Fig. 124 in Chapter 5, in absence of an absolute value of the wafer curvature prior to the die construction, we chose the zero stress state at the end of the heating ramp. Further experiments would have been necessary to understand the full physics of the deformation of the die as this figure entails several features, some expected, and some that we don't understand as for now. As expected, the elastic regime is shorter at high temperature than at low temperature. This is because the yield stress, that is probably thermally activated (most of the mechanisms described in Chapter 5 - Section 5.2.1 are thermally activated) will occur at higher values at low T and at lower values at high T. Between these elastic parts in tension and compression, most of the stress relaxes by plastic deformation. The dominant role of diffusion in the relaxation is evidenced by the much lower stress levels reached at high temperature (diffusion is more dependent on temperature than dislocation glide). However, the fact that the stress decreases in tension below 200 °C and then increases again in compression below 0 °C does not make sense, no matter the relaxation mechanism invoked. The film should be in tension at the end of the cooling. Right now, we don't have an explanation for this. Possible hypothesis would be that our simplified view of the die as an Al metallization over a Si substrate is oversimplified. If other layers (oxydes, poly Si, nitrides) play a significant role, we may have stresses building up in more complex ways. An artifact of the die moving during the experiment also cannot be ruled out as we haven't been able to run additional tests (power control break down of the set-up at the end of 2017).

Also, the temperature amplitude of the thermal cycles performed in the reflectometer is larger than the temperature gradients occurring during electrothermal aging. The goal of extending this amplitude was to compensate the slow temperature rate (and thus strain rate) of this experiment where only a

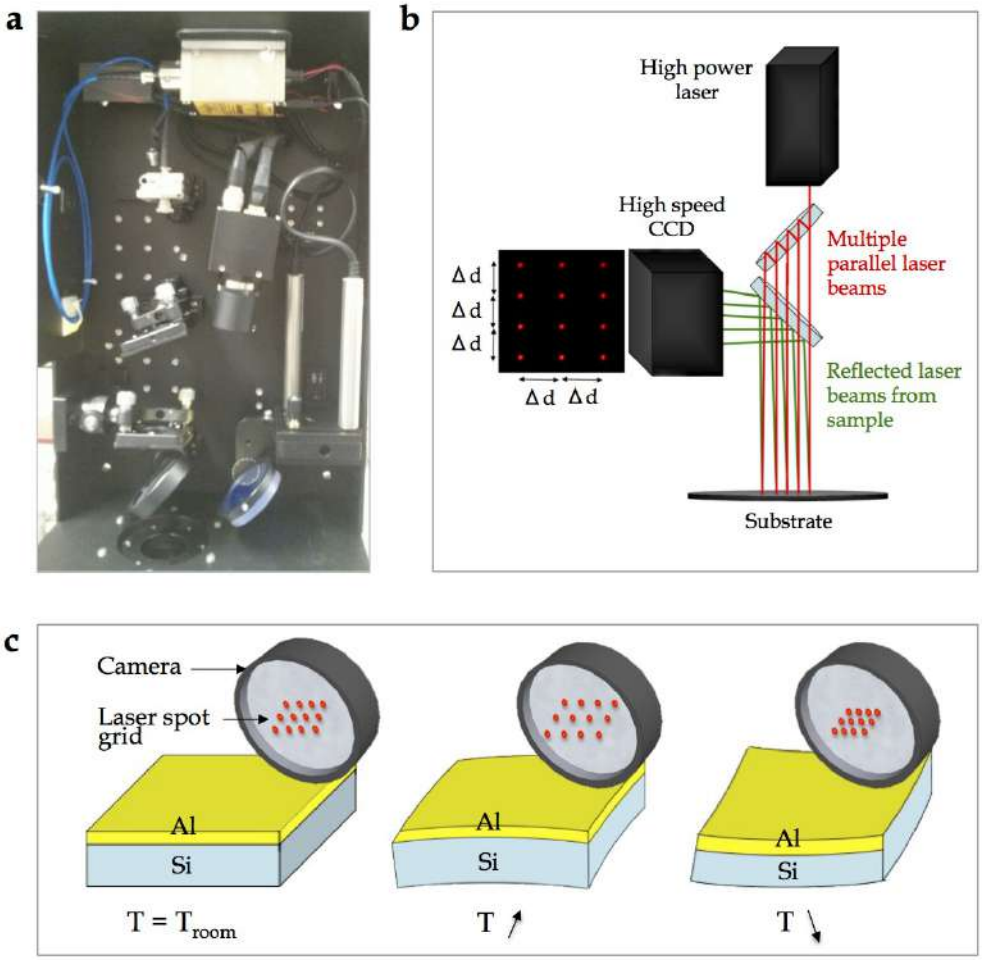

Figure 139: (a) MOS K-space module interior and (b) laser operating principle. (c) The larger CTE of the Al film compared to the Si substrate induces elastic and plastic strains in the film. The Al film is then stressed in compression during the heating phase and in tension upon cooling.

few cycles can performed, compared to the fast temperature excursions in the die in operation, smaller but repeated millions of time.

If we consider an Al film on Si, the total strain is 1% for a cycle of -190 °C to 350 °C (in the reflectometer) and 0.3% for a cycle from 25 °C to 160°C (if we assume that 160 °C is a typical temperature attained in the die at the end of the ON state [Sauo8]). After about 5 cycles, no surface change (cracks, slip traces) has been observed using SEM/FIB and EBSD mapping.

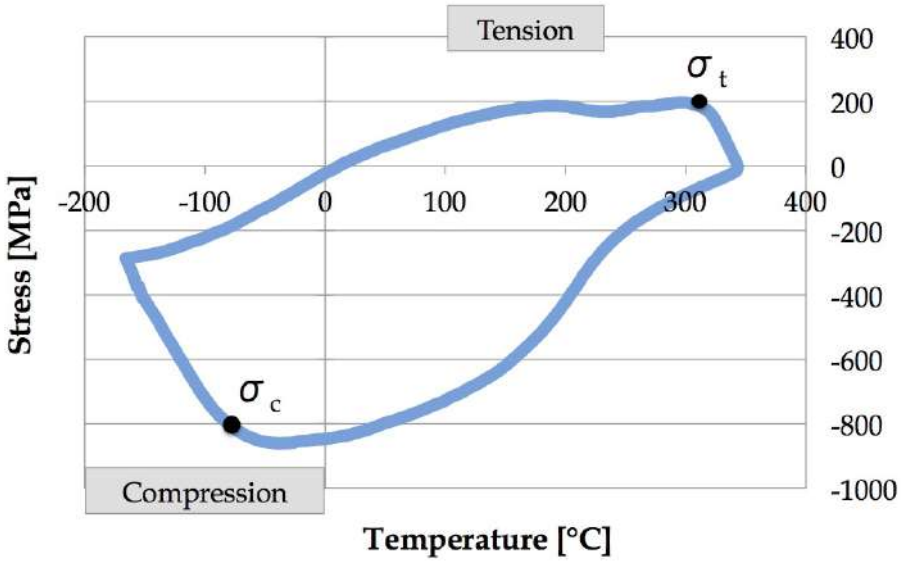

Figure 140: Stress-Temperature cycle for the Al thin film deposited onto the Si wafer. The relative stress is measured along the larger die dimension, and the zero value is here taken at 350°C. The cycle is initiated at $T = -190°C$, and the T gradient is set to $20°C/min$ during heating and cooling.

Part II

RÉSUMÉ ÉTENDU

C

MODES DE FATIGUE DES MÉTALLISATION À BASE D'ALUMINIUM DANS LES COMPOSANTS MOSFET DE PUISSANCE

C.1 INTRODUCTION ET OBJECTIFS

Depuis plusieurs décennies, l'industrie automobile remplace de plus en plus les composants électromécaniques par des dispositifs purement électroniques ou des systèmes électromécaniques miniaturisés basés sur des technologies Si. Ce changement de paradigme a initialement intéressé les fonctions électroniques d'assistance (par exemple ABS, direction assistée, limiteur de vitesse, climatisation, etc.). Cependant, une constante évolution technologique et miniaturisation ont fait que le champ d'application de l'électronique dans l'automobile se propage sur les fonctions principales du véhicule (injection, éclairage, freins, gestion des batteries, etc.) en remplaçant l'ensemble des liaisons mécaniques ou hydrauliques.

Le secteur de l'électronique de puissance est actuellement le marché le plus important dans l'automobile. Les commutateurs de puissance à semi-conducteurs remplacent rapidement les relais électromécaniques classiques dans la plupart des fonctions principaux des véhicules, ainsi que dans les applications de confort, de sécurité et de communication. Le marché de la propulsion automobile alternative représente un autre secteur en croissance, conformément à la nouvelle réglementation du transport routier visant à réduire les émissions de gaz à effet de serre (reduction du 30% d'ici au 2030 pour l'UE). Cette tendance se voit de plus en plus avec le development des concepts de véhicules électriques, purs (EV) et hybrides (micro-, mild, full-, plug-in-hybrid), jusqu'aux projets les plus récents de voitures autonomes.

L'evolution de la technologie électronique dans l'automobile crée inévitablement de nouvelles exigences en termes de reduction des coûts, fonctionnement dans des conditions environnementales extrêmes (température, humidité, vibrations, etc.), une plus grande densité de modules de puissance, une miniaturisation croissante, etc. De plus, un niveau élevé de fiabilité est nécessaires pour garantir la sécurité des produits et des personnes sur de longues périodes. Cela nécessite une connaissance approfondie de l'evolution des composants électroniques en fonction du temps de fonctionnement et des mécanismes de défaillance. L'analyse des défaillances et les études de fiabilité sont donc des étapes clés dans l'industrie manufacturière, afin de développer des disposi-

tifs 100% fiables pendant toute leur durée de vie. La durée de vie est un des paramètres requis par les constructeurs automobiles définis par l'Automotive Electronic Council (documents de qualification, par exemple AEC-Q100, AEC-Q200, etc ...).

Cette étude est motivé par la compréhension des mécanismes de défaillance survenant dans les commutateurs électroniques de puissance produits par l'entreprise NXP Semiconductors pour l'industrie automobile. Au cours de leur vie, ces composants transportent des niveaux de puissance élevés pendant de longues périodes, ce qui peut conduire à une baisse graduelle de leurs performances.. Ici, nous présentons une méthode pour évaluer le vieillissement électrothermique du composant de puissance, en se concentrant sur un cas d'étude particulier: les commutateurs de puissance à base de MOSFET (Metal Oxide Semiconductor), utilisés pour la commutation de l'éclairage des voitures. Cette fonction est particulièrement agressive pour les composants MOSFET car l'allumage d'une lampe s'accompagne d'une impulsion de courant très intense que le composant doit supporter un très grande nombre de fois. Elles s'accompagnent à des grandes variations de température, conduisant à une degradation progressive du composant. Notre objectif est d'étudier les phénomènes à la base de la dégradation de la microstructure des parties critiques, en ciblant la métallisation qui est la partie qui concentre les dégradations microstructurales inévitables du vieillissement de ces dispositifs. Cela a nous permis de déterminer des modèles physiques pouvant expliquer les principaux mécanismes de défaillance à corréler avec l'aggravation progressive des performances électriques de l'ensemble du dispositif.

C.2 TECHNOLOGIE LFET1T ET VIEILLISSEMENT ACCÉLÉRÉ DES COMPOSANTS

Dans le cadre de cette thèse nous avons étudié les mécanismes de dégradation de la métallisation et des fils de connexion en aluminium (Al) dans un cas spécifique: les MOSFET de puissance LFET1T produits par NXP Semiconductors et utilisés pour la commutation de l'éclairage des voitures et camions. Ce travail a été motivé par des exigences industrielles réelles, car la compréhension des limites de la technologie LFET1T serve de référence pour les nouvelles générations de MOSFET actuellement en cours de développement à NXP. Des tests de qualification ont été effectués par NXP à différentes températures afin de déterminer la durée de vie des composants et de localiser les points critiques. En parallel, des puces de puissance LFET1T de référence, débôités et déconnectées de la puces de contrôle, ont été soumis à des conditions extrêmes de court-circuit au sein d'un banc d'essai développé par le laboratoire SATIE afin de suivre les paramètres thermosensibles au cours du vieillissement, et, au même temps, la dégradation des métaux.

C.2.1 *Technologie LFET1T*

LFET1T est le nom commercial de la technologie développée en 2008 par NXP Semiconductors (à l'époque Freescale) basée sur des modules MOSFET trench, pour des applications à basse tension (<48V) et fréquence (<1 kHz). Il s'agit de smart power MOSFETs, où le term "smart" indique que la puce de puissance est contrôlé et protégé par une puce de control. Deux versions de cette technologie ont été caractérisées dans cette étude:

- 12V SPD06 power die (Fig. 141a), conçu pour les batteries 12 V (applications voitures), avec une tension de breakdown de 45V. Ils sont constitués de 2 secteurs MOSFET, chacun connecté par 3 fils de bonding et ayant un $R_{DS(on)}$ de 6mΩ.
- 24V T07D17 power die (Fig. 141b), conçu pour les batteries 24V (applications camions), avec une tension de breakdown de 65V. Ils sont constitués de 5 secteurs MOSFET, connectés par 8 fils de bonding et ayant un $R_{DS(on)}$ de 17mΩ et 7mΩ.

La composition et l'épaisseur de la métallisation et des fils de connection sont les mêmes dans les deux modules de puissance. La métallisation se compose d'un film d'Al avec 0.5% en poids de cuivre (Cu) et de tungstène (W). Dans le cas seulement des T07D17s, la métallisation est passivée par une couche mince de SiO_2 de 0.5µm d'épaisseur (sauf dans les zones de bonding). Les fils de connection sont en Al pur et ont un diamètre de 400µm. Ils sont mis en contact avec la métallisation par un procédé classique de soudage à froid par ultrasons [Bro15] [Goe12]. La force de bonding de 10 N, appliquée à une surface de $450 * 750\mu m^2$ entraîne une contrainte de bonding de ~ 30MPa, en ligne avec les paramètres de bonding optimisés par Goehre et al [Goe12].

C.2.2 *Tests de vieillisssement accéléré*

Les modules LFET1T ont subi deux différents tests électrothermiques accélérés de type IOL (Intermittent Operating Life), qui consiste en une alternance de périodes où le composants sont à l'état passant (on) e de périodes où le composants sont à l'état non-passant (off).

1. Tests à NXP sur 65V LFET1T (T07D17).
   Ils consistent en des tests de qualification, utilisés par les fabricants pour déterminer la durée de vie du composant, conformément à la norme AECQ100-12 [Kel06]. L'objectif est de reproduire le comportement des puces de puissance dans leur mode de fonctionnement normal, régulé par la puce de contrôle. Un court-circuit répétitif est imposé à la puce

de puissance. La puce de contrôle alors détecte un excès de courant et éteint la puce de puissance. De l'énergie est dissipée à ce stade, entraînant une augmentation de température du composant et affectant les conditions de vieillissement de l'appareil. La durée de vie des composants est 5.3 milion de cycles pour les tests effectués à température ambiante et diminue à 300 kcycles à 70°C.

2. Tests au laboratoire SATIE sur 45V LFET1T (SPD06).
   Ces tests sont complémentaires aux précédents: ils ont été conçus pour pousser les dispositifs à leurs limites technologiques et suivre, au même temps, les indicateurs de vieillissement électrique pendant les tests, et notamment l'evolution de la resistance du dispositif ($R_{DS(on)}$) et de la temperature à la surface de la métallisation de source. Les SPD06s ont été soumis à des conditions extrêmes de court-circuit dans un banc d'essai conçu par le laboratoire Satie [Ros13]. Cette configuration particulière a nous donné la possibilité de contourner la puce de contrôle et de contrôler l'énergie dissipée en jouant sur la durée des singles impulsions de courant (t_{ON}). Avec $t_{ON} = 40\mu s$, les dispositifs arrivent à défaillance après ~ 330 kcycles .

Les conditions des deux types de test sont résumées dans le tableau 5 suivante et les relatives formes d'onde au moment de la défaillance sont montrée en Fig. 142.

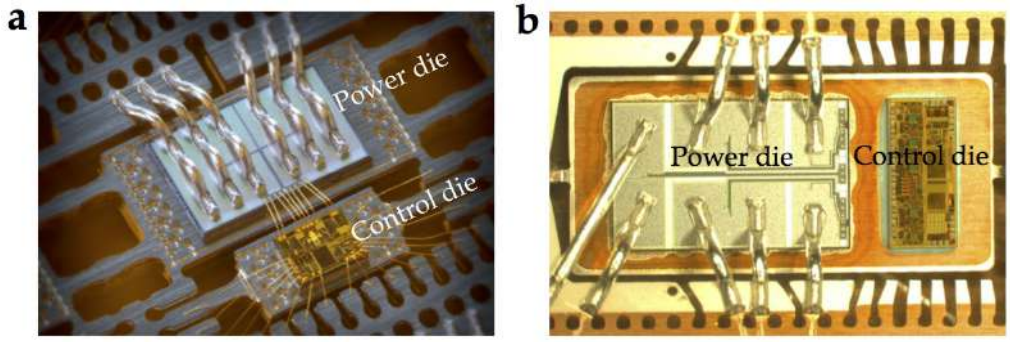

Figure 141: Composants de puissance de type LFET1T smart power MOSFET, produits par NXP Semiconductors. (a) 45V, 12V SPD06, (b) 65V, 24V T07D17.

C.3 TECHNIQUES EXPÉRIMENTALES DE CHARACTERIZATION MICROSTRUCTURELLE DE LA MÉTALLISATION

Notre contribution a consisté à caractériser la microstructure métallique sous vieillissement électrothermique, en utilisant des techniques de métallurgie dédiées,

Table 5: Tests de vieillissement accelerés

	Test @ NXP	Test @ SATIE
Composant	T07D17 configuration normale	SPD06 Sans puce de controle et bôite
Paramètres des test de vieillissement	Test de qualification à regulation de courrant I_{th} = 120 A f = 2 Hz Vds = 14V L = 5µH R = 10mΩ	SC test Sans limitation de courrant Ton = 40µ s f = 5 Hz Vds = 30V E = 150 mJ
Test temperature	25 °C 70°C	25°C
Aging indicators monitoring	Non	Oui
DUT Life-time	5.3 million cycles at 25°C 300k cycles at 70°C	330kcycles

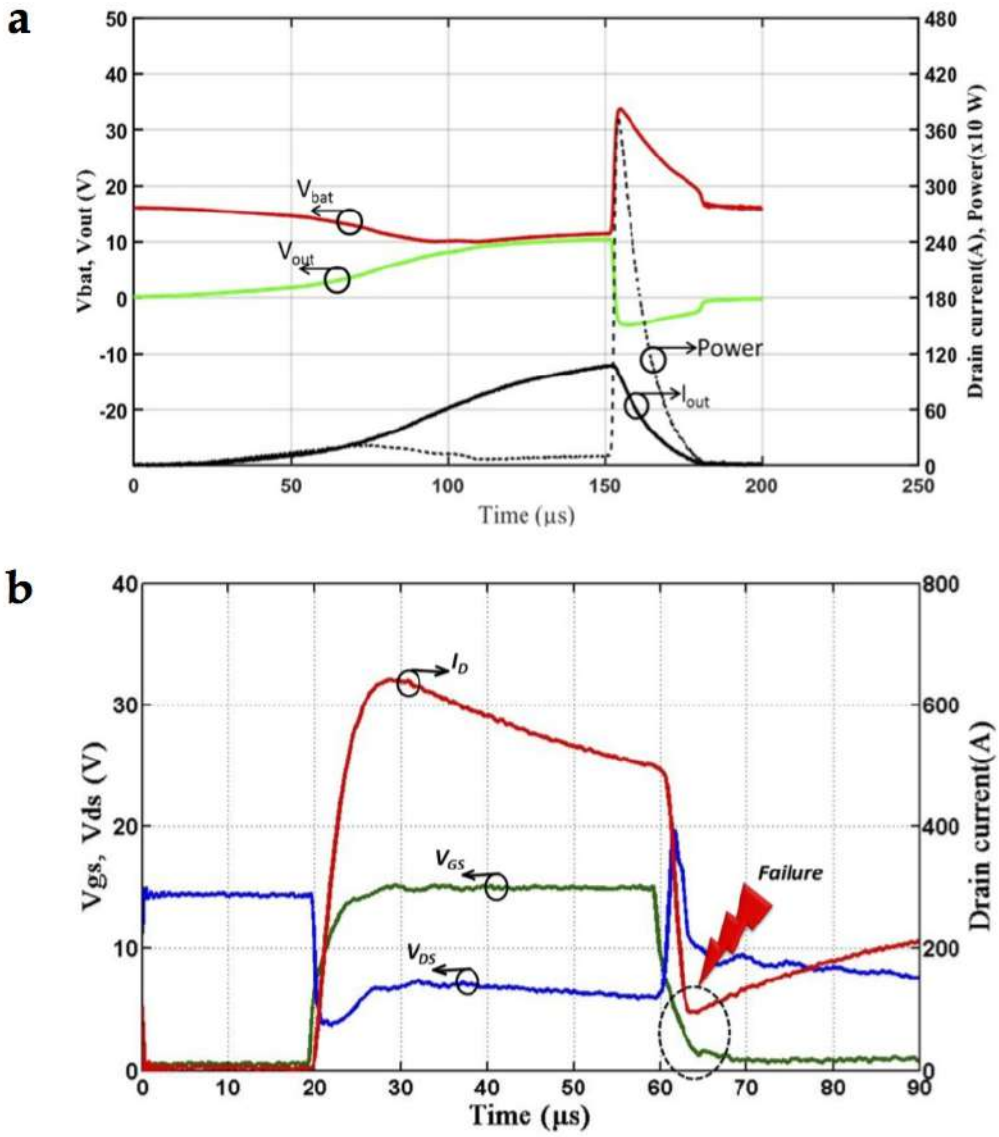

Figure 142: Formes d'onde au moment de la défaillance pour un composant (a) T07D17 soumis à des tests de qualification standard chez NXP et (b) SPD06 vieilli au sain du laboratoire SATIE par de test de court-circuit extrêmes.

comme la microscopie ionique (SIM –Scanning Ion Microscopy–) et électronique (SEM –Scanning Electron Microscopy– et TEM –Transmission Electron Microscopy–), et la cartographie de la structure des grains. Nous avons mis au point des méthodes de caractérisation et de quantification spécifiques pour évaluer le principale caractéristique qui influence le vieillissement du dispositif: la propagation de fissures dans le métal et la déformation plastique due au processus de bonding.

Nous nous sommes concentrés sur les zones de bonding. Contrairement à la métallisation de source qui recouvre les transistors, la partie qui se trouve sous les fils de bondings a subi une importante déformation plastique lors du procédé de soudage à froid. Pour y accéder, il est nécessaire de faire une coupe mais une action mécanique va masquer sur plusieurs microns l'état réel de cette interface. Les gravures ioniques ne peuvent se faire sur de trop grandes profondeurs et on ne peut donc pas traverser les 200 µm de fils pour atteindre l'interface et l'étudier selon le processus décrit ci-dessus. La solution originale que nous avons proposé dans cette étude consiste à découper la partie puissance à l'aide de fil diamant et à polir l'attache des fils à 45°ce qui produit une surface écrouie mais que l'on peut ensuite enlever avec la gravure ionique (Fig. 143a et b). Cette preparation a nous permis pas seulement d'évaluer la qualité du bonding à l'état initial (Fig. 143c), dans les modules de référence, mais aussi de suivre l'évolution de la zone de bonding au cours du vieillissement. Pour augmenter la zone d'observation par rapport à la préparation basée sur le FIB et obtenir des données statistiques, nous avons également effectué un polissage par faisceau ionique dans un cross-polisher system. Lors de nos caractérisations, nous avons systématiquement comparé la microstructure de métallisation à l'extérieur et sous le fil de liaison, avant et après le vieillissement.

C.4 ETUDE DU VIEILLISSEMENT DE LA METALLISATION ET DES FILS DE CONNEXTION

Le burnout est un mode de défaillance courant dans les modules de puissance qui s'approchent de leur limite de durée de vie. Ce type de défaillance est souvent associé à une soudaine augmentation de la résistance drain-source. En particulier, les parties métalliques des modules de puissance IGBT et MOSFET montrent des altérations qui pourraient conduire à une telle augmentation de la résistance. Les altérations observées par ces pièces métalliques sont souvent attribuées à leur faible résistance à la déformation mécanique, même si les mécanismes par lesquels les altérations se produisent restent peu clairs. Puisque les défaillances des soudures et des fils de connextion dépendent en partie du processus et en partie du matériau, le control de la résistance mécanique

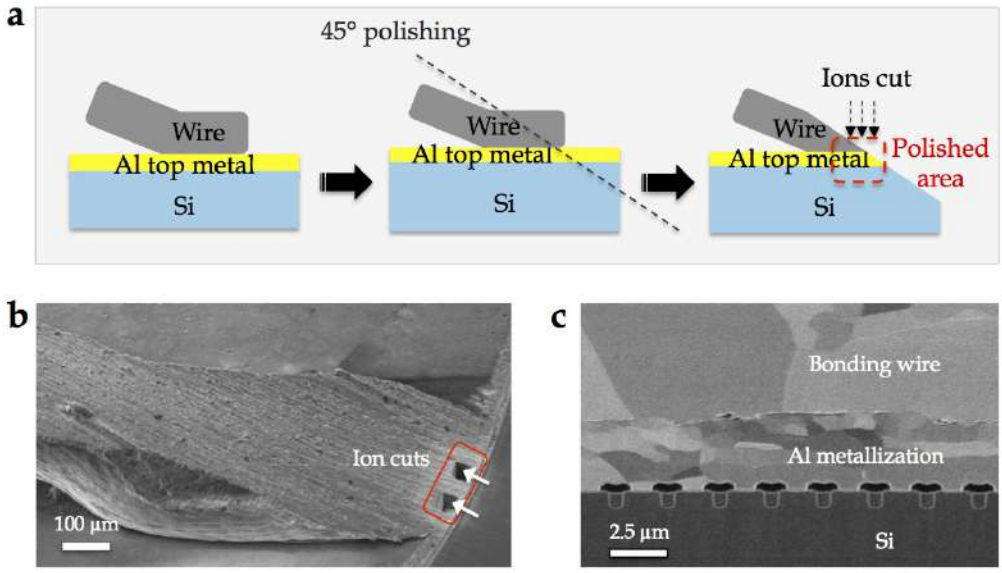

Figure 143: (a) Schématisation du procédé de preparation de l'interface métallisation-fils de bonding d'un composant LFET1T: la zone de gravure au FIB est préalablement polie à 45°. (b) Le résultat de la preparation est répresenté dans l'imagerie SEM à bas grandissement, où on peut voir le fils coupé à 45°et deux gravures FIB à niveau de l'interface fil / métallisation. (c) À plus fort grandissement, l'imagerie ionique permet de montrer le bonding Al / Al: les microstructures du fil et de la métallisation sont très différentes notamment en terme de taille de grain.

de ces parties métalliques peut augmenter leur fiabilité. En fait, de nouvelles générations de dispositifs d'alimentation ont été conçues pour retarder telles défaillances, en transférant une partie de la charge électrique au source métal. Ceci est particulièrement vrai pour les soudures dans le cas des modules de puissance NXP: les MOSFET de puissance LFET1T étudiés dans ce travail vieillissent principalement par dégradation de métallisation. Le vieillissement de la métallisation de source ne peut pas être entièrement contrôlé et elle semble être contrôlée par des mécanismes de dégradation intrinsèques et universels. La technologie Al utilisée ici est plutôt représentative de nombreux back-end packaging utilisés. Indépendamment des cycles électrothermiques, nombreux paramètres peuvent influencer la potentielle évolution de ce set-up:

- la composition du fil et de la métallisation. Des alliages augmenteront leur résistance mécanique et ohmique;
- la taille des grains des deux éléments influera sur leur dureté et la stabilité de la microstructure (les petits grains rendront le métal plus dur mais seront sujets à la croissance des grains);
- l'interface créée entre le fil et la métallisation dépend des paramètres de bonding (dans le cas des LFET1Ts, les fils d'Al sont soudés par ultrasons à la métallisation), peut affecter la microstructure des fils et de la métallisation et introduire des éléments externes.

Nous montreront dans la suite les principaux mécanismes de dégradation de la métallisation de source observés lors de nos caractérisations. Nous avons systématiquement comparé la microstructure de métallisation autour et sous les fils de connection, avant et après vieillissement. Cette progressive dégradation des parties métalliques s'accompagne à une augmentation de $R_{ds(on)}$ on, comme il est démontré par la Fig. 144. Le graphique montre une augmentation du14% de$R_{ds(on)}$ pour un composant SPD06 à défaillance (après $\sim$ 330kcycles).

C.4.1 *Métallisation nue (hors zone de bonding)*

Une étude SEM et SIM systématique de la métallisation de source Al des modules SPD06 et T07D17 qui ont subi différentes conditions de vieillissement électrothermique révèle des mécanismes de dégradation de la métallisation communs. Il s'agit d'une significative reconstruction de la métallisation au voisinage des fils de connexion. Elle se produit à niveau de surface, par une augmentation de la rugosité (Fig. 145a) par rapport à la structure granulaire initiale de l'Al (Fig. 145a) et, à l'intérieur du matériau, par un apparent rétrécissement des grains et l'apparition des fissures (Fig. 145d). Ces résultats sont

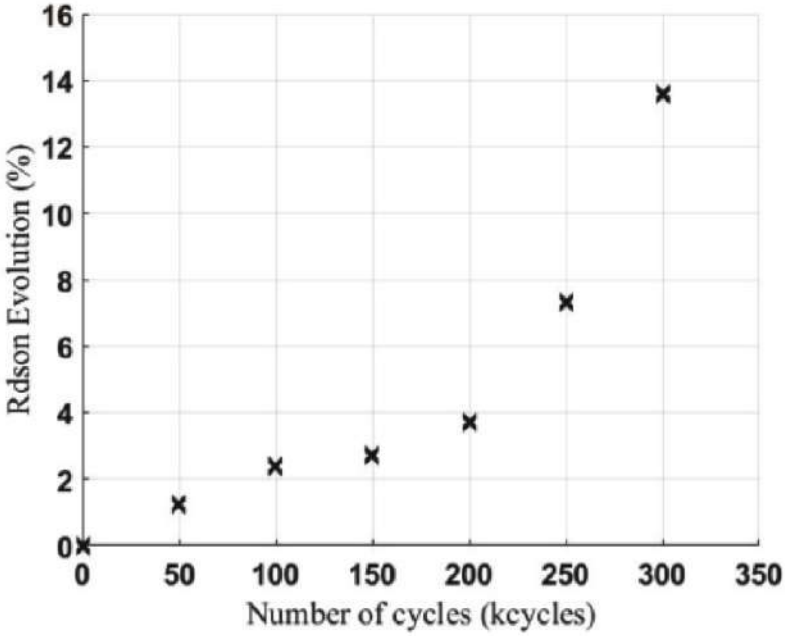

Figure 144: Evolution de $R_{ds(on)}$ en cours de vieillissement, jusqu'à defaillance (après $\sim$ 330kcycles).

en accord avec les mécanismes de dégradation décrits dans la littérature pour les métallisations Al et Cu [Gla04] [Cia02] [Mar14] [Nel11] [Nel13].

- Avant les tests, la surface de la métallisation est lisse et suive la structure des ondes des transistors (Fig. 145a). Comme pour les films Al classiques, des grains sont détectés à la surface et de petites dépressions définissent les rainures des joints de grains. À l'intérieur de la couche, l'interface entre les grains est visible par le contraste ionique (Fig. 145c): es grains d'Al bambou [Arz11] [Joo94] [Wal92b], avec un diamètre moyen de 4µm et une hauteur égale à l'épaisseur de la couche, remplissent tout le volume de la métallisation.

- Après les test de vieillissement, la surface de la métallisation est modifiée et présente une forte altération due à la déformation plastique et aux extrusions Fig. 145b; la structure initiale des transistors n'est presque plus visible. À l'intérieur de la couche, les grains sont divisés en sous-joins (grains avec une désorientation < 15°, mesurée par cartograhie ASTAR, Fig. 146) et des fissures intergranulaires s'étendent de la surface jusqu'à la zone du transistor (Fig. 145d). Ces résultats révèlent que la structure granulaire a subi une déformation plastique limitée par dislocation, ce qui explique l'apparition de sous-grains conduisant à un rétrécissement

apparent du grain dans l'imagerie FIB. Le vieillissement de la métallisation est dominé par une diffusion accrue des atomes d'Al le long des joints de grain, à la base de l'initiation et propagation des fissures intergranulaires perpendiculaires à la surface jusqu'au substrat de Si [Mar14].

À défaillance, nous avons observé une différente fissuration dans la métallisation nue, passives par le mold compound et avec passivation SiO2 (Fig. 147).

- Dans la métallisation nue (Fig. 147a), les rainures GB deviennent équivalentes (voire plus grandes) à l'espacement entre les transistors.
- La métallisation passivée par le mold compound (Fig. 147b) est aussi fracturée, mais les fissures sont plus fines et se propagent horizontalement à l'interface oxyde / semiconducteur.
- Une couche de passivation d'oxyde plus rigide (Fig. 147c) et plus adhérente ralentit la diffusion du GB mais ne l'arrête pas complètement. Les fissures sont plus localisées et concentrées, mais toujours présentes.

Pour essayer de quantifier les fissuration dans les zones passivées seulement par le mold compound ("bare" dans le graphique en Fig. 148b) et par une couche supplémentaire en SiO_2 ("passivated" dans le graphique en Fig. 148b), nous avons inventé la méthode suivante: étant donné que la métallisation est constituée de joints de grain bambou, disposés de façon à peu près proportionnelle aux transistors, nous avons compté le nombre de joints verticaux fissurés/non fissurés et le nombres de cellules fissurées horizontalement (le long de l'interface métal/substrat) par rapport à celles ne contenant aucune fissure. Ce qui est résumé sur la Fig. 148a. Les résultats sont donnés sur la Fig. 148b. Il apparaît clairement que la fissuration est plus clairsemée dans les parties passivées avec SiO_2, mais cette différence est plus marquée sur la fissuration horizontale. Les précédentes observations montrent que la fissuration horizontale se déclenche lorsque la fissuration verticale atteint la zone des transistors depuis la surface. Si on suppose que cette fissuration verticale "sature" lorsque 30% des joints sont atteints (métallisation non passivée) on peut expliquer que la fissuration horizontale soit limitée dans le cas de la métallisation passivée seulement par le mold compound, puisque 20% des joints sont atteints dans ce cas. L'effet de la température est aussi plus marqué dans le cas de la métallisation sans SiO_2, puisque les fissures horizontales sont beaucoup plus développées à 70°C qu'à 25°C, effet que l'on retrouve moins dans la métallisation passivée par SiO_2.

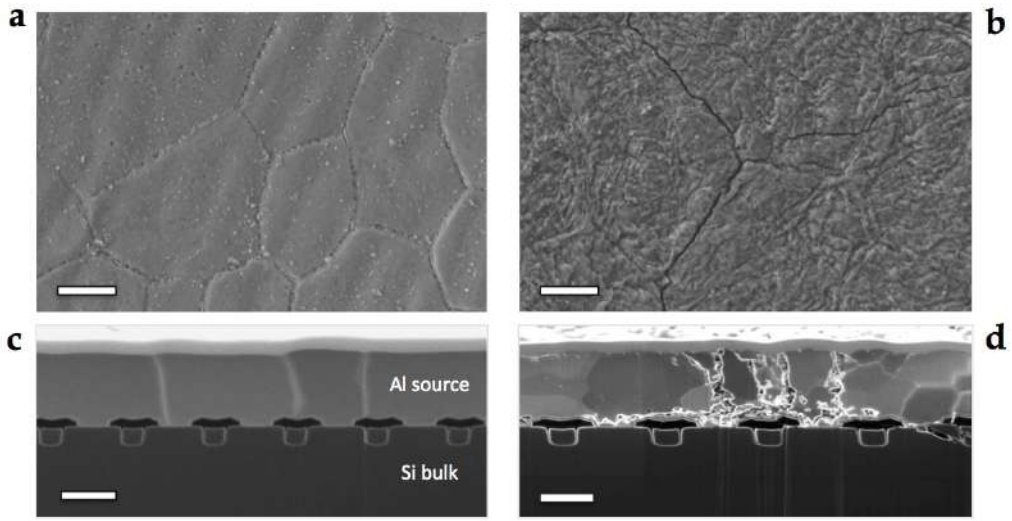

Figure 145: Évolution de la microstructure de la métallisation à base d'aluminium de SPD06 pendant vieillissement à température ambiante. Les observations en surface (a) avant et (b) après vieillissement sont faites en SEM. Les coupes transverses (c) avant et (d) après vieillissement sont faite en FIB / SEM et les images sont faites par contraste ionique. Barre d'échelle: 2.5µm.

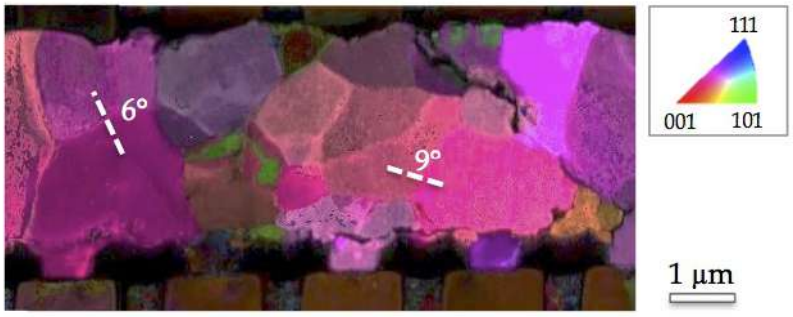

Figure 146: Mesures de taille de grains par MET-ACOM sur un module T07D17 vieilli à 25°C. Les relatives images ionique (Fig. 145d) montre parfois des domaines cristallins qui ne sont que des sous-grains (désorientation inférieure à 10°).

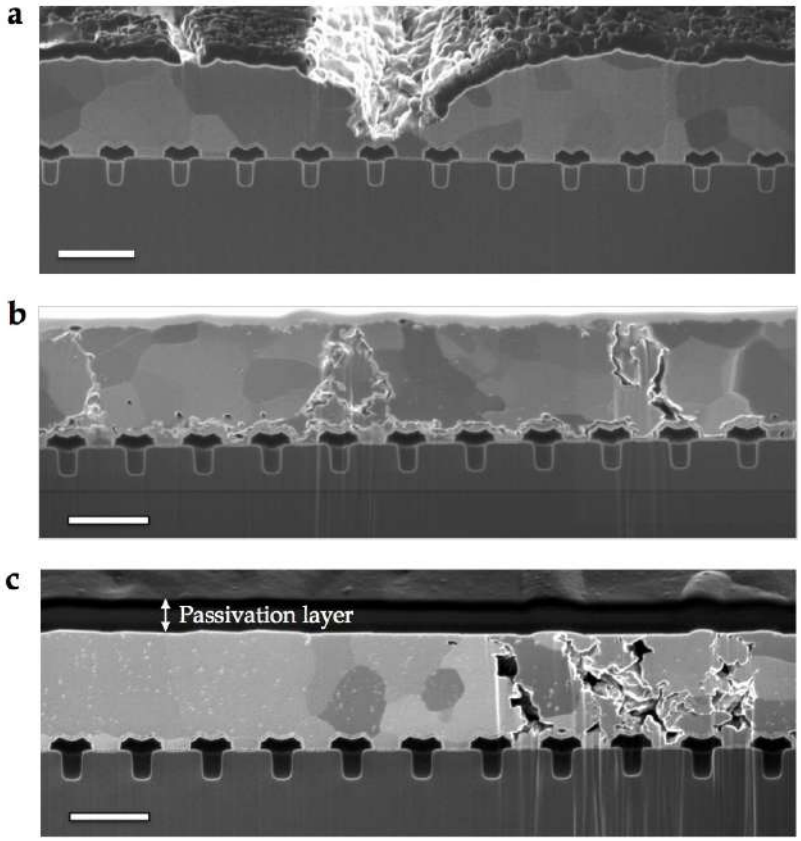

Figure 147: Fissuration de la métallisation développée dans une zone (a) non passivée, (b) passivée par mold compound et (c) passivé par SiO_2 (plus mold compound). Barre d'échelle: 2.5µm.

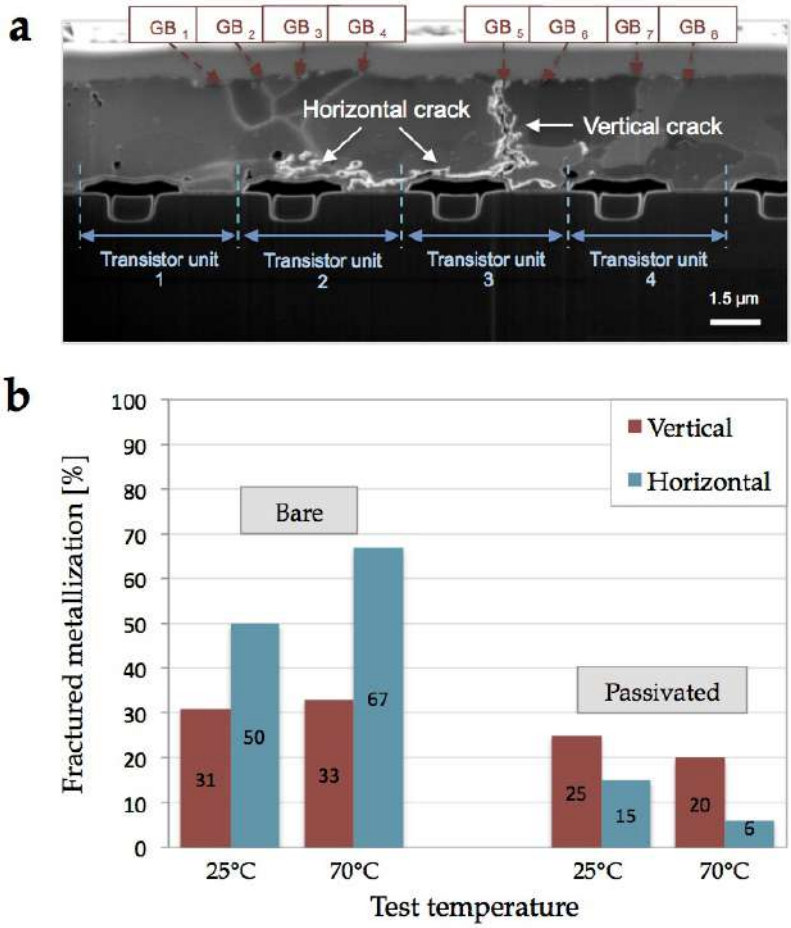

Figure 148: (a) Méthode de comptage des fissures verticales et horizontales en fonction des joints de grains (verticaux) et des cellules de transistor (pour les fissures horizontales).
(b) Statistiques de fissuration de la métallisation pour des modules T07D17 vieillis à 25°C et 70°C, dans les zones passivées uniquement par le mold compound (gauche) et passivées par une couche de SiO_2 (gauche).

C.4.2 *Interface métallisation / fils*

- La zone de bonding initiale est caractérisée par la présence systématique d'une interface bien définie et irrégulière entre la métallisation et le fil (Fig. 149a), faite par de résidus d'oxyde d'aluminium (Fig. 149c) et de petites cavités. Cela signifie que le bonding n'est pas parfaite et qu'il n'y a pas d'interdiffusion Al-Al à cause de la barrière d'oxyde natif qui n'est pas casé pendant le processus de soudage à froid. Le vieillissement accentue ces défauts initiaux, qui sont le point de départ de la propagation horizontale de fissures à l'interface entre la métallisation le fil, causant une réduction de contact entre les deux métaux (Fig. 149b). Dans ces zones peu contactées, les fissures peuvent également se propager verticalement jusqu'à le substrat de Si suivant les joints de grains, comme dans les parties autour des fils. Il est important de remarquer que les fissures restent limitées à l'interface fil-métal et ne se propagent pas dans le fil. Ceci est une forte indication que l'interface Al / Al est faible et sa présence induit des phénomènes de dégradation spécifiques. Si la liaison était initialement parfaite, les fissures auraient dévié vers le matériau le plus mou qui est le fil, puisque il a des grains plus larges.

- Sous le fil (Fig. 150b), la microstructure de la métallisation initiale est plus fine que ailleurs (métallisation nue et fil). Le réarrangement de la structure granulaire, prouvé par l'ASTAR (Fig. 150c), est dû à une déformation plastique importante et non uniforme engendrée par le procédé de bonding sur la métallisation de source. Nous essayé pour la première fois à mesurer cette deformation. La méthode que nous avons mis au point est montrée en Fig. 151a. On compte les déformations par rapport à une référence (ligne rouge) en mesurant des aires de métal enfoncées (zone -) ou dépassant (zone +) de cette référence qui correspond à la position initiale de la surface de la métallisation. La déformation est ensuite calculée en comparant ces aires ($Area_{Def}$) par rapport à l'aire initiale ($Area_{Ref}$) de la métallisation dans la zone observée. La déformation plastique mesurée est de 5% en moyenne, si on considère des sections entières et varie entre 0% et 25% si l'on calcule dans des sections FIB plus petites. Ces résultats confirment que la déformation plastique induite par le procédé de bonding est très dishomogène, comme nous l'avons observé qualitativement dans les images élétroniques, qui montre une iterface fil-métallisation très irrégulière. Les valeurs précédentes sont obtenues sur une section totale de $\sim 1300\mu m^2$, ce qui est petit par rapport au volume impacté par le fil de bonding ($\sim 0.3mm^2$), mais pas négligeable. Compte tenu de la pression appliquée pendant le processus à ultrasons, la contrainte de compression moyenne sur la métallisation

est de ~ 30MPa. Cette contrainte est beaucoup plus faible que la limite d'élasticité d'un Al commercial pur avec une granulométrie comprise entre 1 et 2µm, typiquement comprise entre 100 et 150 MPa [Tsu02]. Pour expliquer le fait qu'une déformation plastique si importante se produise avec cette petite charge, nous avons supposé que seulement une fraction de $0.3mm^2$ de la surface de métallisation était réellement en contact avec le fil. Une estimation très grossière conduirait à un tiers de la métallisation impactée par une déformation plastique liée au fil. Ceci explique aussi pourquoi la surface est déformée de manière très inhomogène. Le fait que seulement une partie du fil est soudé à la métallisation et que cette partie diminue au vieillissement est supporté par des expériences précédentes [Goe10]. Il serait nécessaire de connaître plus précisément les propriétés mécaniques du fil et de la métallisation (qui dépendent fortement des impuretés présentes, de la granulométrie, etc.) pour mieux estimer la surface de métallisation influencée par le bonding, mais la prédiction de la déformation très hétérogène de l'interface resterait, de toute façon, hors de portée.

- Contrairement à nos attentes, cette microstructure initialement déformée ne change pas de manière significative au curs du vieillissement et n'influence pas la propagation des fissures vers le fil. L'augmentation locale de la température n'est pas suffisante pour influencer l'interface entre la métallisation et le fil. Cette interface reste systématiquement présente pendant le vieillissement et aucune reconstitution significative des grains du fil et de la métallisation a été observée jusqu'à la fusion finale du metal.

C.5 FISSURATION DANS LE SEMICONDUCTEUR

L'augmentation local et incontrôlé de temperature, due à la dégradation de la métallisation et à l'augmentation de sa résistivité, semble être le mécanisme de défaillance le plus récurrent. Nous avons observé une sévère propagation de fissures dans le substrat de Si, autour et sous les fils défectueux, où des points chauds ont été détectés (Fig. 152a). Nous avons observé des fissures primaires et secondaires (Fig. 152b):

1. Les fissures primaires sont plus petites et remplies d'Al (Fig. 152c). Ceci est probablement dû à la diffusion de l'aluminium fondu à l'intérieur du substrat de Si.

2. Les fissures secondaires sont plus larges et pas remplies d'Al. Elles provoquent probablement la défaillance finale du périphérique.

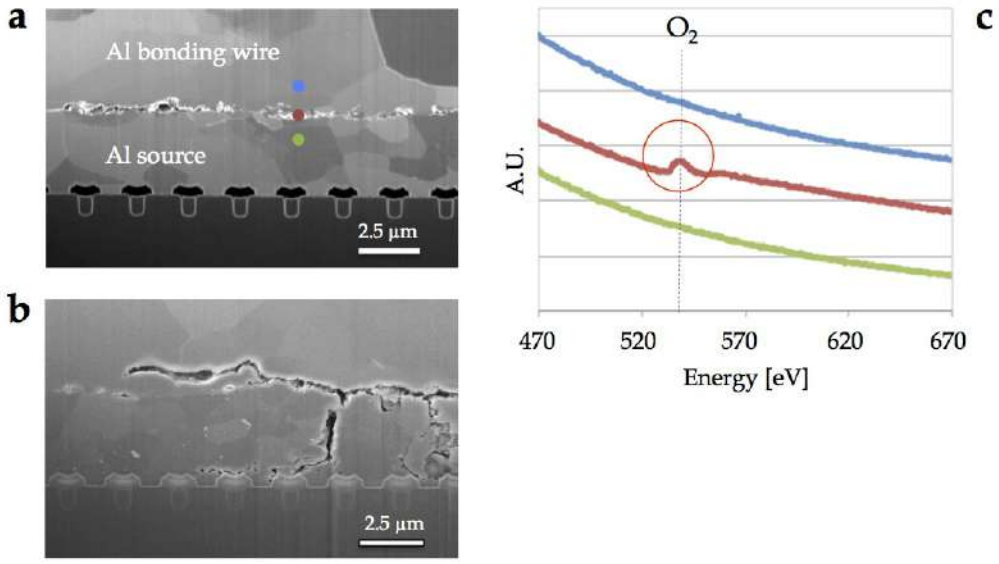

Figure 149: (b) Spectres EELS enregistrés à trois endroits, relatives aux points colorés en (a), proche de l'interface fil/métallisation dans un composé non vieilli. Le pic correspondant à l'oxygène ne ressort qu'à l'interface et prouve donc la présence d'oxyde localisé. (c) Pendant vieillissement, ces imperfections favorise la propagation de fissures le long de l'interface fil/métallisation, qui determine un détachement local de deux métal. À cette endroit, des fissures verticales along the joints de grains peuvent aussi se propager jusqu'au substrat de Si, comme dans les portions de métallisation nues.

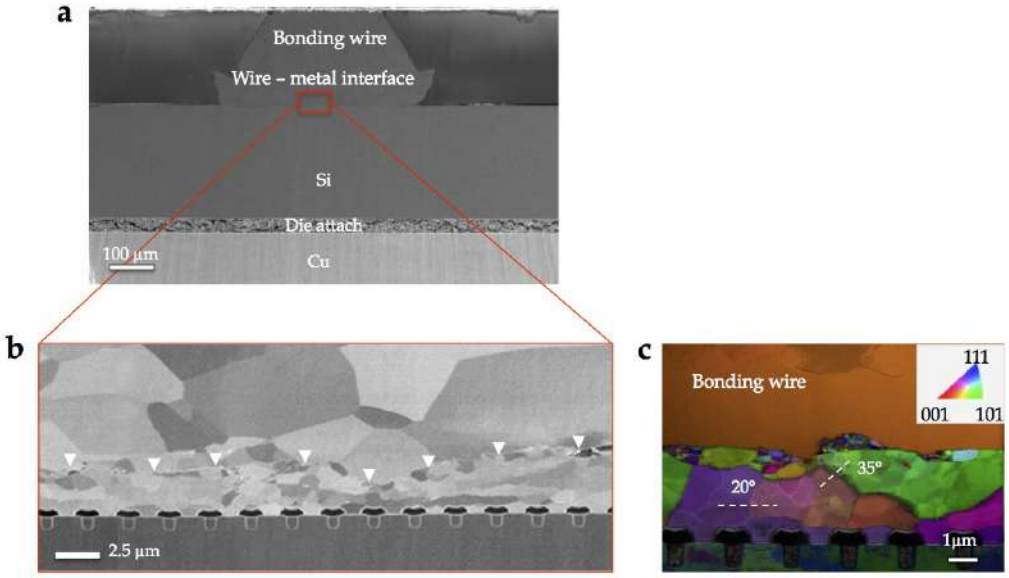

Figure 150: (a) Cross section SEM d'un module To7D17 non vieilli effectuée par un cross-polisher system. (b) L'encart est réalisé en image ionique afin d'observer les grains de l'interface fil/métallisation. (c) Mesures de taille de grains par MET-ACOM sur des sections équivalents à (b).

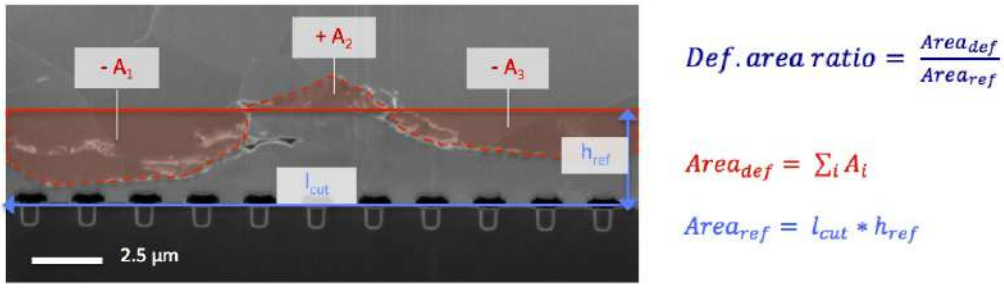

Figure 151: Méthode de mesure de la déformation plastique imposée par les fils de bonding (en haut) à la métallisation de la source (en bas).

Ces deux types de fissures peuvent indiquer que après la formation de fissures primaires dans le Si, le dispositif continue à conduire de la courant et reste chaud pendant une période suffisamment longue pour créer une fusion et une recristallisation d'Al à l'intérieur du substrat de Si.

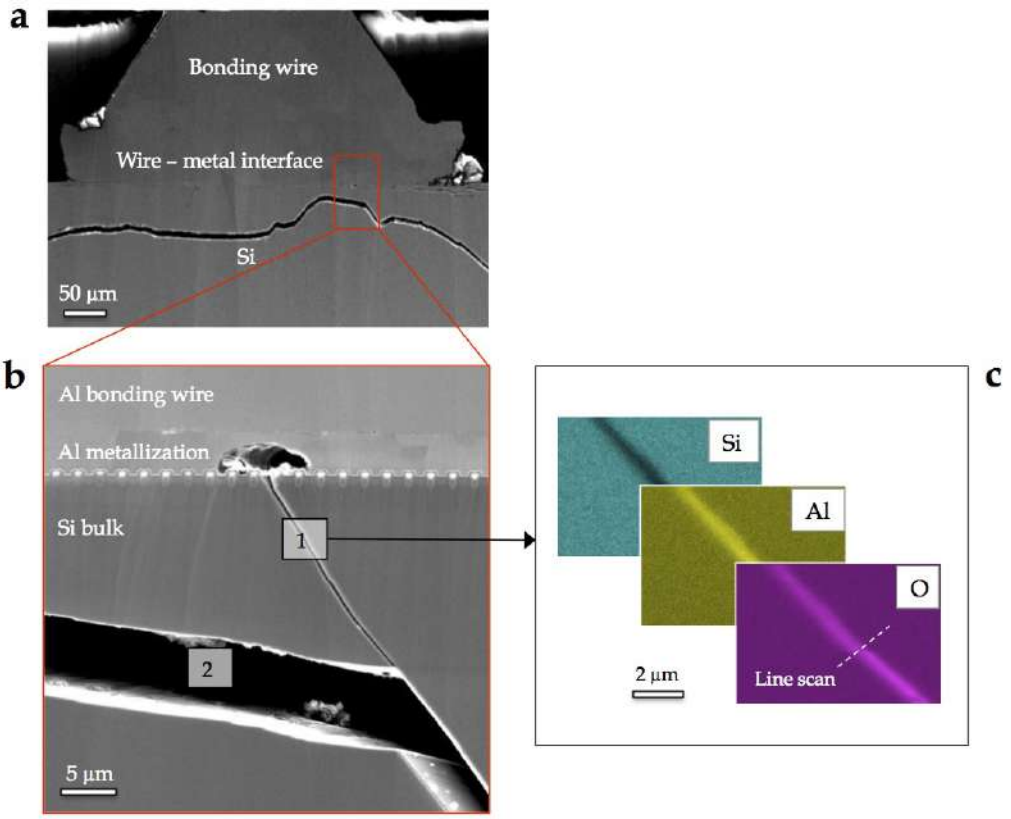

Figure 152: Image SEM à bas (a) et plus fort (b) grossissement du substrat de Si fissuré sous le fil de contact (1 = fissure primaire, 2 = fissure secondaire). (c) Cartographie EDX d'une fissure plus fine dans le Si, qui montre qu'elle est remplie d'Al.

Une preuve plus flagrante de diffusion d'Al dans le Si est montrée en Fig. 153a. Un précipité de forme circulaire est placé sous le fil. Son diamètre est d'environ 200µm, du même ordre de grandeur que le diamètre du fil d'amenée de courant. L'analyse EDX montre sans ambiguïté que c'est de l'Aluminium, et qu'à cette échelle d'observation, il est quasi pur (Fig. 153b). Cela signifie que le fil de bonding et la couche de métallisation d'Al ont fondu et diffusé dans le Si en raison des températures élevées pendant la défaillance. La cartographie EBSD (Fig. 153c) dans la même zone révèle que le matériau d'Al diffusé dans le volume Si est caractérisé par une microstructure granulaire. Cela signifie que l'Al fondu a recristallisé lorsque l'appareil a cessé de fonctionner et s'est

refroidi. À ce stade, nous pouvons remarquer que l'interface Al-Al n'est plus visible dans la zone de bonding. Au contraire, la cartographie EBSD provenant du fil adjacente dans le même module vieilli montre une structure normale (Fig. 154): on peut encore distinguer une interface de métallisation de fil bien définie avec une microstructure granulaire plus fine dans la métallisation Al et des grains plus gros dans la partie de liaison supérieure. Ceci démontre que l'échauffement a été localisé dans la première zone de bonding, où la défaillance s'est produite. Ici, la température élevée a provoqué la fusion des deux parties métalliques initiales, créant la diffusion du matériau dans le Si dessous et une nouvelle microstructure d'Al.

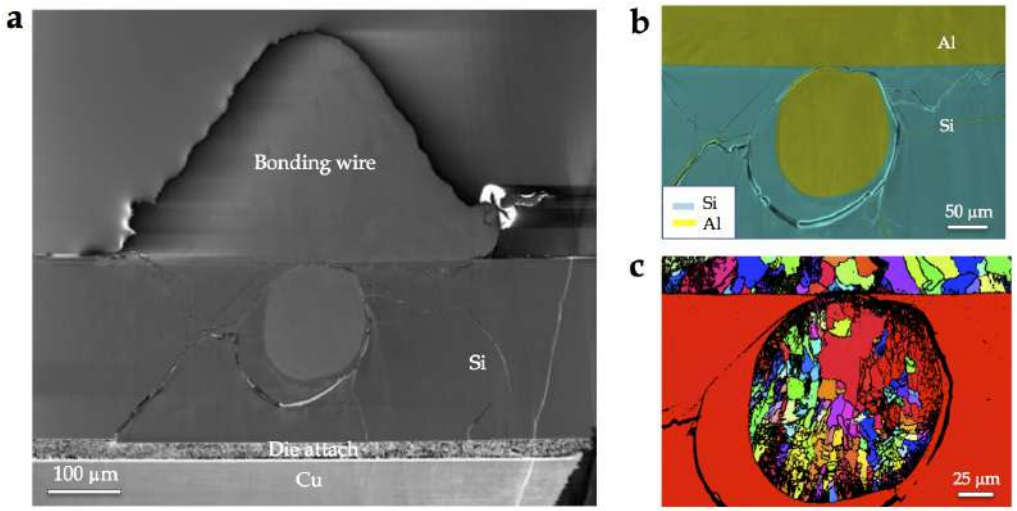

Figure 153: (a) Précipité quasi-millimétrique d'Al situé dans le substrat de Si dans un composant vieilli à défaillance. (b) Coupe FIB et cartographie EDX (Si bleu et Al-jaune). (c) Cartographie EBSD du précipité d'Al recristallisé dans le substrat. Chaque domaine de couleur correspond à une cristallite d'orientation distincte. Noter le domaine rouge au centre du grain, sans doute cristallisé en dernier.

C.6 CONCLUSIONS ET PERSPECTIVES

En conclusion, le vieillissement de la métallisation de source dans la technologie LFET1T peut être associé à deux phénomènes:

- Une reconstruction significative du métal, caractérisée par la génération de joints de grain spécifiques des modules de puissance à base d'Al.
- Une systématique mauvaise adhérence des fils à la métallisation, due à l'oxyde native d'Al, qui n'est jamais cassé avant la fusion finale d'Al (as-

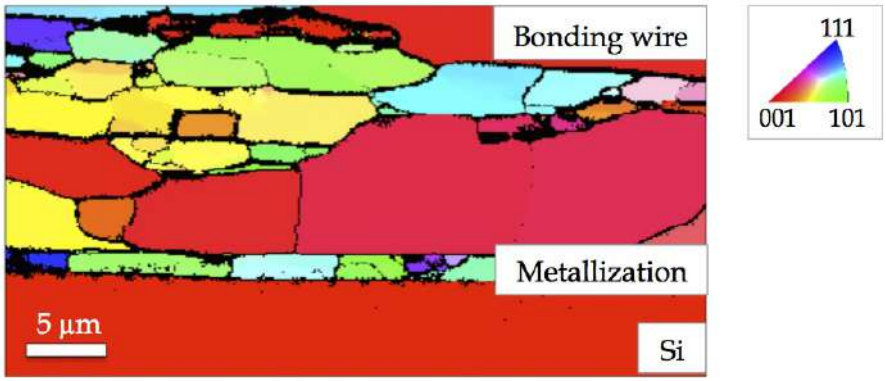

Figure 154: Cartographie EBSD d'une portion de la zone de bonding non fondue dans un module vieilli.

sociée à la défaillance de l'appareil). Des fissures se propagent parallèles le long de l'interface entre le deux métals.

Ces deux mécanismes concourent à augmenter la résistivité locale et à favoriser les points chauds, et peuvent conduire à la fusion de l'Al et à la fracture du substrat de Si. Même si le changement des processus industriels est difficile et il est hors du cadre de cette thèse, notre étude suggère des possibles moyens d'amélioration de la fiabilité de ce type de dispositif, ainsi que des voies futures pour compléter les présentes conclusions.

- Le procédé de soudage à froid ne fournit pas un contact Al / Al parfait et la présence d'une interface défectueuse persiste jusqu'à la défaillance. À ce stade seulement, une vrai reconstruction de la microstructure de fil de métallisation est réalisée. Idéalement, l'oxyde d'aluminium devrait être cassé pendant ou juste avant la connexion par fil. Ceci pourrait être réalisé en effectuant une réduction du métal et du fil, ou en effectuant cette soudure à haute température. On peut changer la forme du fil pour créer des pointes locales qui créeraient une concentration de contrainte suffisante et augmenteraient la surface d'adhérence pour favoriser la croissance des grains (par diffusion locale) à l'interface. Nous avons montré qu'une plastification importante du métal sous le fil est probablement très tolérable de la part du composant.

- Un changement de type de métal pourrait également faire une différence. Une connexion cuivre / cuivre ne devrait pas avoir ce type de problème d'adhérence. Cependant, il est bien connu que les interconnexions Cu nécessitent une isolation chimique beaucoup plus sévère du substrat Si.

- Nos avons fait de tentatives pour quantifier l'information sur l'augmentation du stress dans le métal au cours du vieillissement, mais ils sont insuffisantes. À ce propos, des expériences de courbure pour mesurer le stress et le corréler (ou non) avec la reconstruction de la surface pourraient être utiles.
- La passivation de la métallisation par un oxyde semble réduire la densité de fissure et augmenter la durée de vie des puces de puissance etudiés. Cependant, il ne semble pas possible de passiver complètement le métal autour des fils de bonding, pour concentrer la dégradation du métal à cet endroit. En plus, nous n'avons pas assez de statistiques sur ce sujet. La question principale est de savoir si ce type de passivation peut favoriser des événements catastrophiques précoces, associés à des concentration de points chauds. Pour un nombre accru de cycles, le moment auquel une panne se produit peut fortement diverger.

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