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Système de radiocommunication télé-alimenté par voie radiofréquence à 2.45 GHz

Dean Karolak

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POUR OBTENIR LE GRADE DE

DOCTEUR DE

L'UNIVERSITÉ DE BORDEAUX

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SPÉCIALITÉ : ÉLECTRONIQUE

Dean KAROLAK

**DESIGN OF RADIOFREQUENCY ENERGY HARVESTERS IN CMOS
TECHNOLOGY FOR LOW-POWER APPLICATIONS**

Sous la direction de : Prof. Yann DEVAL
(co-directeur : Prof. Thierry TARIS)

Soutenue le 27 Novembre 2015

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Design of Radiofrequency Energy Harvesters in CMOS technology for Low-Power Applications

Abstract

Wireless Powered Receivers (WPR) hold a promising future for generating a small amount of electrical DC energy to drive full or partial circuits in wirelessly communicating electronic devices. Important applications such as RFIDs and WSNs operating at UHF and SHF bands have emerged, requiring a significant effort on the design of high efficient WPRs to extend the operating range or the lifetime of these portable applications. In this context, integrated rectifiers and antennas are of a particular interest, since they are responsible for the energy conversion task. This thesis work aims to further the state-of-the-art throughout the design and realization of high efficient WPRs from the antenna up to the storage of the converted DC power, exploring the interfacing challenges with their fully integration into PCBs.

Keywords: Wireless Powered Receiver; RF Harvester; Rectifier; Wireless Power Transmission; Wireless Sensor Network, Antenna; Far-field propagation.

Système de radiocommunication télé-alimenté par voie radiofréquence à 2.45 GHz

Résumé

Récepteurs récupérateurs d'énergie sans fil (WPR) détiennent un avenir prometteur pour la génération d'énergie électrique continue afin d'alimenter complètement ou partiellement les circuits compris dans les systèmes de communication sans fil. Applications importantes telles que l'identification par radiofréquence (RFID) et les réseaux de capteurs sans fils (WSN) fonctionnant aux bandes de fréquences UHF et SHF sont apparues, nécessitant un important effort sur la conception de WPRs d'haute efficacité pour étendre la distance de fonctionnement ou de la durée de vie de ces applications portables. Dans ce contexte, les redresseurs intégrés et les antennes sont d'un intérêt particulier, car ils sont responsables pour la tâche de conversion d'énergie. Ce travail de thèse vise à faire progresser l'état de l'art à travers de la conception et réalisation de WPRs d'haute efficacité, dès l'antenne jusqu'au stockage de la puissance DC convertie, en explorant les défis d'interconnexion avec leur pleine intégration sur PCBs.

Mots clés : Récepteur télé-alimenté; Récupération d'énergie; Redresseur; Transmission d'énergie sans fil; Réseau de capteurs sans fil, Antenne; Télé-alimentation.

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To my family and friends,

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List of Abbreviations

AC	Alternative current
BEOL	Back End Of Line
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DCMT	Diode Connected MOS Transistors
DUT	Device Under Test
EIRP	Equivalent Isotropically Radiated Power
EM	Electromagnetic
FCC	Federal Communication Commission
GSM	Global System for Mobile Communication
ISM	Industrial, Scientific and Medical
PCB	Printed Circuit Board
RF	Radiofrequency
PMU	Power Management Unit
WEH	Wireless Energy Harvesting
WE/PT	Wireless Energy / Power Transmission
WPT	Wireless Power Transmission
WPR	Wireless Powered Receivers
WSN	Wireless Sensor Network

General Introduction

Nowadays there is a growing demand for large-scale applications as RFID circuits and sensor-based wireless networks. Within such context, the need for green communication strategies and inexpensive solutions is of great importance. One approach is to set up a network comprising self-powered nodes, *i.e.*, nodes that can harvest ambient energy from a variety of natural and manmade sources for sustainable network operations. This yields to a significant reduction in the maintenance costs associated with periodically replacing batteries and extend of battery lifetime by implementing highly efficient power management capabilities.

Among the several energy sources for harvesting applications, this thesis work explore the viability in using RF energy as a source to supply low-power devices. One good reason for using this kind of power source is that it is considered as the less expensive option due to its simplicity to be embedded in electronic systems, such as Wireless Sensor Networks (WSN) applications. Furthermore, the expansive increase of RF electronic devices and a relatively high energy conversion efficiency achieved by RF harvesters make this kind of energy a potential harvesting source.

In all of these applications, there must be a power conversion circuit that can extract enough DC power from the incident electromagnetic waves to ensure a proper power supply for the devices. Previously reported far-field RF powered devices generally operate from distances of less than 10 meter from the RF source, due to the high power loss from RF wave propagation at UHF frequencies. Other previous works achieved good power efficiency levels, however, they provide low output voltage or demand high input power levels. Hence, making them inadequate for use in most passively powered wireless sensor networks. A highly efficient passive power conversion circuit is needed for long distance passive sensing in distributed sensor networks.

GENERAL INTRODUCTION

The industrial, scientific, and medical (ISM) bands particularly at 900 MHz and 2.4 GHz are a good option for RF energy harvesting. Indeed, higher effective isotropic radiated power (EIRP) are allowed at these frequencies and also the most current electronic devices operate within these frequency bands, which contributes to increased ambient power density. Furthermore, the size of the radiating element correlated to the operating frequency remains compact at these ISM bands.

For a given RF source, the operating range is limited by the sensitivity of the energy harvesters, *i.e.*, the minimum incident RF power converted into a DC power. Due to the low power available at the antenna, RF energy harvesters are often based on multi-stage rectifier to increase their sensitivity. The sensitivity is dictated by the threshold voltage of the rectifying devices. To overcome such limitation in conventional rectifiers, several low-threshold techniques have been extensively studied and proposed in the literature, either relying on technology solutions or based on proper compensation circuits.

In many power harvesting applications, such as WSNs and RFID, the cost prevails over the performances. In order to be cost effective in such applications, the sensor nodes must be of low cost and low maintenance. This presents challenges regarding supply efficiency and power management.

Within a context of efficient trade-off between system performance and implementation cost, the WPRs reported in this thesis work are developed in low-cost processes to make their large-scale production viable.

This thesis report is organized as it follows:

Chapter I introduces the most recent trends related to wireless harvesting systems, describing them through historical advances up to recent WPT applications found in the market today.

Chapter I concerns the study, design and implementation of low-power rectifiers. High efficient topologies are proposed, using bulk-biasing and threshold compensation techniques to overcome the intrinsic voltage drop of standard CMOS devices. This chapter also presents the validation of these RF rectifier architectures in silicon and compares the measured results with most recent rectifier circuits found in the literature.

GENERAL INTRODUCTION

Chapter I is dedicated to design and realization of the entire wireless energy harvesting system developed to operate in a low-power / low-consumption context at 900 MHz and 2.45 GHz frequency bands. This chapter describes two different scenarios for its implementation:

- WPRs operating with a standard 50 Ω antenna, allowing its integration within most electronic communication systems existing today.
- And WPRs operating with inductive antennas for custom applications.

This chapter also presents the design and implementation of antennas and matching networks developed to operate into RF harvesting systems. Finally, several WPRs have been prototyped and validated with the integration of all system blocks into a common low-cost substrate, PCB.

Chapter I synthesizes this thesis work, showing the most important results achieved through the design of low-power WPRs operating at UHF bands.

Introduction générale

Aujourd'hui, il y a une demande croissante pour des applications sans fil à grande échelle comme les circuits pour l'identification à distance et les réseaux de capteurs sans fil. Dans ce contexte, la nécessité de solutions de faible coût et de différentes stratégies de communication et alimentation est d'une grande importance. Une approche consiste à mettre en place un réseau comprenant des nœuds autoalimentés, *i.e.* nœuds qui peuvent récupérer de l'énergie ambiante à partir d'une variété de sources naturelles et anthropiques pour assurer que l'opération de ces types de réseaux sans fil soit durable. Cette technique réduit significativement les coûts de maintenance associés au remplacement périodique des batteries et peut aussi, le cas échéant, prolonger leur durée de vie à travers d'une gestion plus efficace des divers types de l'énergie récupérées.

Parmi les différentes sources d'énergie utilisées pour la télé-alimentation des applications sans fil, ce travail de thèse vise à explorer la viabilité de l'utilisation de l'énergie de type radiofréquence (RF) comme une source de puissance pour alimenter des appareils de faible consommation. Une des avantages de l'utilisation de ce type d'énergie est son faible coût d'implémentation en raison de la simplicité de son intégration dans des systèmes électroniques, tels que des applications de réseaux de capteurs sans fil (WSN en anglais). En outre, l'augmentation expansive de l'utilisation des dispositifs électroniques RF et un rendement de la conversion énergétique relativement élevée obtenue par les modules télé-alimentés par voie RF font ce type d'énergie une potentielle source pour la télé-alimentation.

Afin d'assurer une alimentation continue adéquate pour les différentes applications périphériques, un circuit de conversion de puissance capable d'extraire assez d'énergie DC à partir des ondes électromagnétiques incidentes se fait nécessaire. Dispositifs RF destinés aux applications fonctionnant en champs lointain rapportés auparavant rarement atteignent un rayon d'opération de l'ordre de quelques dizaines de mètre de la source émettrice, essentiellement en

INTRODUCTION GÉNÉRALE

raison de la perte de puissance élevée dans la propagation des ondes RF à des ultra hautes fréquences (UHF). Des travaux précédents ont obtenu de bons niveaux d'efficacité de puissance, cependant, soit ils fournissent une faible tension de sortie, soit exigent des niveaux de puissance d'entrée élevés. Par conséquent, ce qui en fait insuffisantes pour une utilisation dans les réseaux de capteurs sans fil complètement passives. Pour que les dispositifs électroniques soient auto-suffisantes en utilisant la télé-alimentation par voie RF, une conversion énergétique très efficace est nécessaire ainsi que l'obtention d'un niveau de tension adéquat.

Les bandes de fréquences dédiées aux applications industrielles, scientifiques et médicales, domestiques ou similaires, (bandes ISM), sont en général des fréquences idéales pour effectuer la télé-alimentation par voie RF, en particulier à 900 MHz et 2.4 GHz. En effet, des niveaux de puissances isotropes rayonnées (EIRP en anglais) plus élevés sont autorisés à ces fréquences et aussi la majorité des appareils électroniques présents dans nos jours fonctionnent dans ces bandes de fréquences, qui contribuent à l'augmentation de la densité de puissance existant dans l'environnement. En outre, la taille de l'élément rayonnant en corrélation avec la fréquence de fonctionnement reste compacte dans ces bandes ISM.

Concernant une source RF donné, la plage de fonctionnement est limité par la sensibilité des modules télé-alimentés par voie RF, *i.e.*, la puissance incidente minimale en RF converti en une puissance continue DC. En raison de la faible puissance disponible à l'antenne, ces modules télé-alimentés sont souvent basées sur les redresseurs de multi-étages pour augmenter leur sensibilité. La sensibilité est déterminée surtout par la tension de seuil des dispositifs utilisés pour la conversion d'énergie. Pour surmonter cette limitation présente dans les redresseurs classiques, plusieurs techniques de faible tension de seuil ont été largement étudiées et proposées dans la littérature, soit en appuyant sur des solutions liées aux améliorations technologiques, soit basées sur des circuits de compensation appropriées.

Considérant les nombreuses applications pour la télé-alimentation, telles que les réseaux de capteurs sans fil et l'identification par RF (RFID), le coût l'emporte sur les performances. Pour que la production à grande échelle de ce type d'applications soit rentable, les nœuds de capteurs sans fil doivent être de faible coût et d'entretien réduit. Cela pose des défis concernant la gestion de l'alimentation en puissance et l'efficacité de ces systèmes RF télé-alimentés.

INTRODUCTION GÉNÉRALE

Dans un contexte de compromis entre la performance du système et le coût total de la mise en œuvre, les WPRs rapportés dans ce travail de thèse sont développées en utilisant des processus de fabrication à faible coût pour rendre leur production à grande échelle viable.

Ce rapport de thèse est organisé comme il suit:

Chapitre I présente les tendances les plus récentes concernant les systèmes télé-alimentés par divers types de source d'énergie sans fil, les décrivant par des avancées historiques jusqu'aux applications récentes pour la télé-alimentation trouvées aujourd'hui sur le marché.

Chapitre II concerne l'étude, la conception et la mise en œuvre de redresseurs de faible puissance. Topologies d'haute efficacité sont proposées, en utilisant des techniques de polarisation de substrat et de compensation de la tension de seuil pour surmonter la chute de tension intrinsèque des dispositifs CMOS standard. Ce chapitre présente également la validation de ces architectures de redresseurs RF en silicium et compare les résultats de mesure avec la plupart des circuits redresseurs récentes dans la littérature.

Le chapitre III est consacré à la conception et à la réalisation de l'ensemble du système de télé-alimentation par voie RF développé pour fonctionner dans un contexte de faible puissance / faible consommation dans les bandes de fréquences de 900 MHz et 2,45 GHz. Ce chapitre décrit deux scénarios différents pour sa mise en œuvre:

- WPRs fonctionnant avec une antenne standard de 50Ω , permettant son intégration au sein de la plupart des systèmes de communications électroniques existants aujourd'hui.
- Et WPRs fonctionnant avec des antennes inductives pour des applications personnalisées.

Ce chapitre présente également la conception et la mise en œuvre des antennes et des réseaux d'adaptation développés pour fonctionner dans ces systèmes télé-alimentés par voie RF. Finalement, plusieurs WPRs ont été prototypés et validés avec l'intégration de tous les blocs du système dans un substrat commun à faible coût, PCB.

Chapitre IV synthétise ce travail de thèse en montrant les résultats les plus importants obtenus à travers de la conception des WPRS de faible puissance et d'haute efficacité fonctionnant dans la bande UHF.

Chapter I

Chapter I. Wireless Harvesting Systems

1 Introduction to Harvesting Techniques

Today, sustaining the power requirement for autonomous wireless and portable devices is an important issue. In the recent past, energy storage has improved significantly. However, this progress has not been able to keep up with the development of microprocessors, memory storage, and wireless technology applications. For instance, in battery powered wireless sensors, the modules are expected to last for a long period of time, but the energy limitation of batteries cannot provide enough power to ensure it. Hence, requiring maintenance from time to time. The major issue of this inconvenience is to provide battery maintenance for a large-scale network consisting of hundreds or even thousands of sensor nodes, which may be difficult, if not impossible.

Ambient power sources, as a replacement for batteries, come into consideration to minimize the maintenance and the cost of operation. Power scavenging may enable wireless and portable electronic devices to be completely self-sustaining, so that battery maintenance can be eventually removed.

Recently, researchers have performed many studies in alternative energy sources that could provide small amounts of electricity to electronic devices, and it is depicted that energy harvesting can be obtained from different energy sources, such as mechanical vibrations, electromagnetic (EM) sources, light, acoustic, airflow, heat, and temperature variations. Energy harvesting, in general, is the conversion of ambient energy into usable electrical energy. When compared with energy stored in common storage elements, such as batteries, super capacitors, and the like, the environment represents a relatively infinite source of available energy.

Systems continue to become smaller, which also limits the amount of available energy on board, leading to a short run-time for a device or battery life. Researchers continue to build high-energy density batteries, but the amount of energy available in the batteries is not only finite but also low, which contributes to decrease the life time of the systems. Hence, extended life of the electronic devices is very important; it also has more advantages in systems with limited accessibility, such as those used in monitoring of machines or instruments in manufacturing plants with dangerous environments.

The general structure diagram of energy harvesting systems for power supply low-power devices is shown in Figure I.1 with the purpose of achieving stable long-term operation of the system. Hence, it is possible to use the available energy in the environment to generate electricity at any given location to power supply electronic devices. These energy sources include solar energy, mechanical vibration, temperature gradient, wind energy, water flow, and magnetic energy, among other options, which are now being used in a wide variety of applications. The harvested energy can be used directly or stored into energy storage device according to the magnitude of output power and impedance. There is need to combine the design and fabrication with appropriate interface circuit for the purpose of realizing self-powered systems.

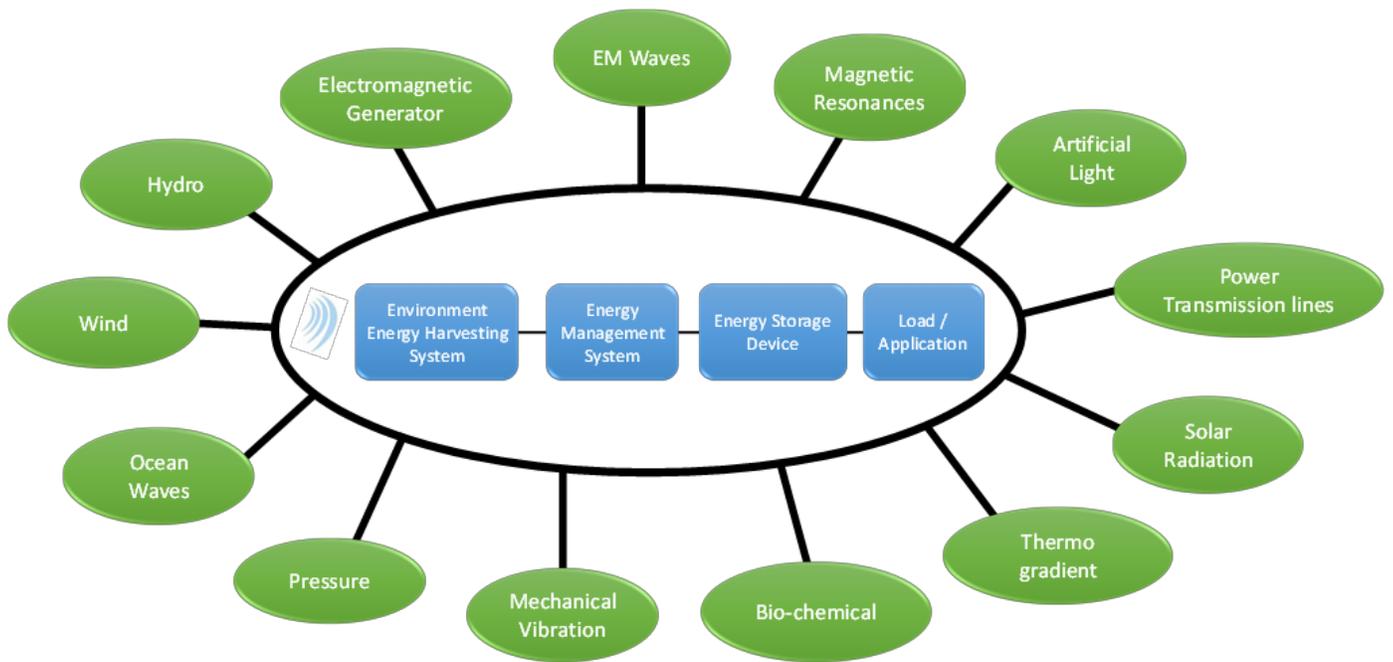


Figure I.1: General structure diagram of wireless energy harvesting system.

The critical long-term solution should therefore be independent of the limited energy available during the life-time of such devices. TABLE I.1 compares the estimated power and challenges of various ambient energy sources in studies performed in recent years. Values in the table were derived from a combination of published studies, experiments performed by the authors, theory, and information that is commonly available in textbooks.

The comparison table, TABLE I.1, provides a broad range of potential methods to scavenge and store energy from a variety of ambient energy sources, as well as the respectively energy conversion efficiency achieved lately and the relative cost in comparison with each other.

TABLE I.1 Power density comparison of different energy harvesting methods.

Energy source	Power density	Efficiency	Cost	References
Acoustic noise	3 nW/cm ³ @75 dB 960 nW/cm ³ @100 dB	Low – up to 10%	High	[1]-[2]
Temperature variation	25 μW/cm ² (Human body) 1~10 mW/cm (Industry)	Low – up to 11%	High	[3]-[7]
Ambient Radio Frequency	100 nW/cm @900 MHz 1 nW/cm @2.4 GHz	Moderate – up to 40%	Low	[8]-[11]
Ambient light	100 mW/cm ² (Direct sun) 100 μW/cm (Illuminated Office)	Moderate – up to 40%	High	[12]-[15]
Vibration/Motion	4 μW/cm ² (Human) 100 μW/cm (Industry)	Low – up to 20%	Low	[16]-[18]
Magnetic field energy	130 μW/cm ³	-	Low	[19]-[20]
Wind flow	15 μW/cm ³	High – (~80%)	High	[21]-[22]

Considering the amount of power density present in the ambient, we can highlight the thermal and light sources. However, even if a large amount of power is available, the temperature differences across a chip are typically low, which limits the thermal energy conversion. In contrast,

solar can be a significant source of energy, but it is highly dependent on the application and environment to which the system is subjected. Also, the photovoltaic devices, responsible for the energy conversion, are quite expensive yet.

Conversely, piezoelectric materials, mostly responsible for vibration energy conversion, have the advantages of mature manufacturing process and can be considered low cost. But piezoelectric ceramic is fragile and unable to bear large strain. Thus, it is easy to produce fatigue crack and brittle fracture on the impact of high-frequency cyclic load.

It is important to notice that today the literature review shows that no single power source is sufficient to supply the different kind of applications, and that the selection of energy sources must be considered according to the application characteristics. Another important characteristic, which must be also taken into account, is the overall system cost to become large-scale production of wireless powered devices viable.

Among the several energy sources for harvesting applications, this thesis work explore the viability in using RF energy as a source to supply low-power devices. Even if it is being ranked among the worst sources considering the power density available in the ambient, when the production cost comes into play, it is considered as the less expensive option due to its simplicity to be embedded in electronic systems, such as Wireless Sensor Networks (WSN) applications. Furthermore, with the expansive increase of RF electronic devices and a relatively high energy conversion efficiency achieved with RF harvesters make this kind of energy a potential harvesting source.

2 Wireless Power Transmission / RF Energy Harvesting

Recent advancements in wireless power transmission (WPT) technologies are enabling several engineering applications with potential product implementation. WPT can be used to charge the batteries inside the device and/or power supply some circuits of the system to save power without the need of a wire connection. For devices requiring only very low power, they can become batteryless and operate only with the energy harvested from ambient radio frequency (RF) and microwave radiation. WPT can be performed via radio waves or microwaves, using wireless

communication technologies or by using other type of techniques, such as resonant and inductive coupling.

2.1 History of Wireless Power Transmission

The first steps leading to research on Wireless Power Transmission (WPT) began in the 19th century. Three major milestones made a significant impact pioneering the researches to this promising subject:

- the invention of electromagnets demonstrated practically by William Sturgeon in 1825;
- André-Marie Ampère studies, showing that electric current produces a magnetic field, which led to the emergence of Ampère circuital law in 1826;
- Michael Faraday studies, describing the electromagnetic force induced in a conductor by a time-varying magnetic flux. They also led to the emergence of a law known as Faraday's law of induction in 1831.

With the discovery of electromagnetic induction and how electromagnetic waves are produced, WPT was the next subject of researches. Figure I.2 depicts a brief histogram of most important WPT researches performed from 19th century until so far. In 1862 the first theoretical basis of WPT were formulated by James Clerk Maxwell, which gave rise to the equations widely known today as Maxwell's equations [23].

These equations allowed the behavioral understanding of electromagnetism and radio electricity, which together with the concept of the Poynting vector, describing the radio wave propagation as an energy flow [24], give directions to Nikola Tesla dream. Tesla claimed that all electricity would be provided wirelessly. To prove it, he performed the first WPT experiments at the end of 19th century [25]-[30]. He tried to transmit a power of approximately 300 kW throughout a frequency of 150 kHz radio wave [29], [30]. The results obtained of his experiment has not been as satisfactory as he expected to be, mainly due to the difficulty to generate such a high power and radio waves scattering operating at high frequencies.

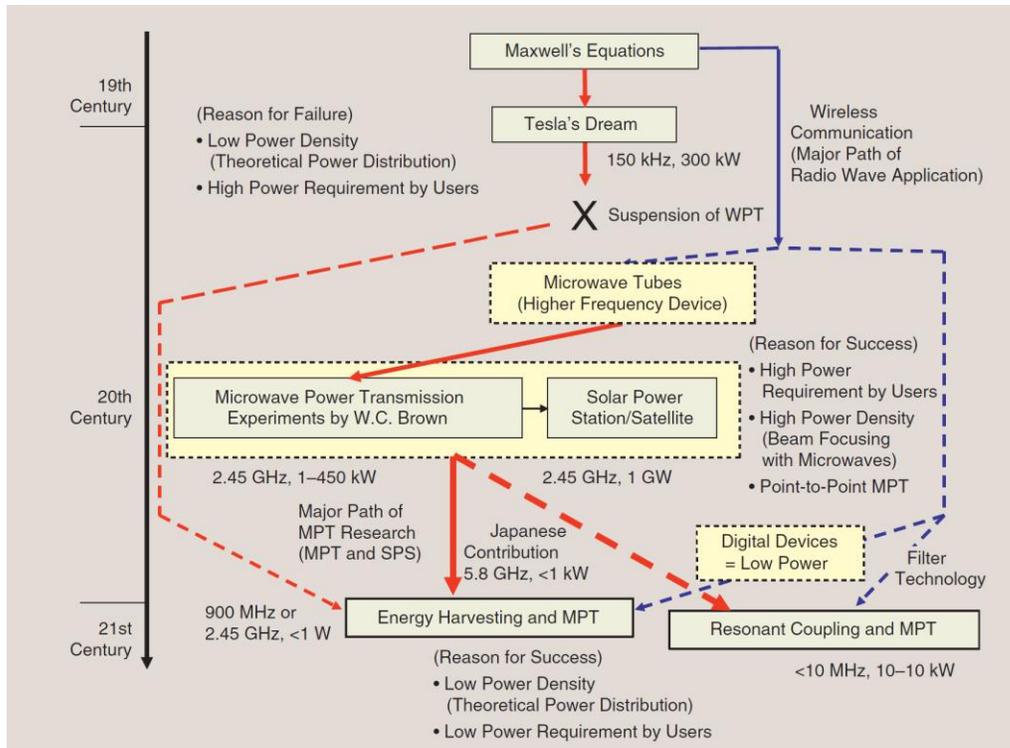


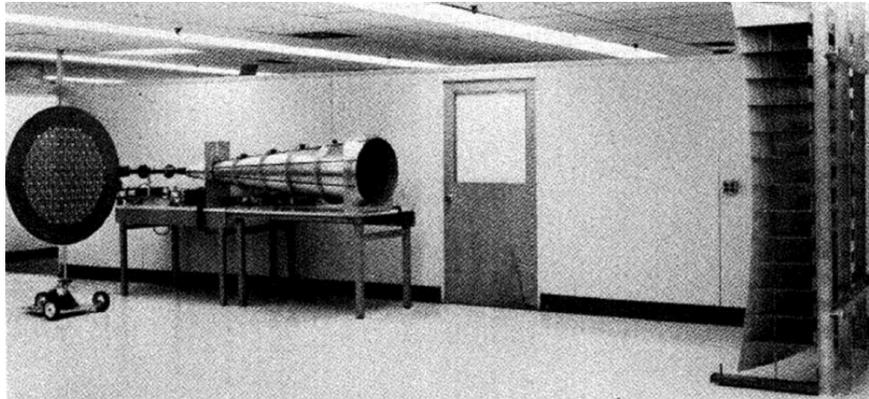
Figure I.2: WPT histogram [31].

The high cost of Tesla experiments and mainly after Marconi communication system starting regular transatlantic transmissions in 1903 requiring less expensive equipment directed the course of the history of radio-wave development to be more focused on wireless communication and remote sensing rather than WPT per se. Hence, researches on WPT stagnated for approximately half of a century.

However, even if the works on WPT have been stalled for a while, the advances in wireless communication helped to improve WPT techniques afterwards. Also, the invention of the microwave magnetron [32], and development of radar performed during the World War II improved much the antenna and microwave generator technologies, contributing to the feasibility of WPT.

In the 1960s, the WPT researches were restarted by William Brown, but this time counting with high-efficiency microwave technologies, such as magnetrons and klystrons. He performed several WPT experiments operating at 2.45 GHz ISM band [33]-[34]. He first developed a rectifying antenna, which he called “rectenna,” for receiving and rectifying microwaves. The efficiency of his first rectenna developed in 1963 was 50% to deliver an output DC power of 4 W

and 40% at an output DC power of 7 W, respectively [33]. With the rectenna, Brown succeeded in transmission of power by microwaves to a tethered helicopter in 1964, and to free-flying helicopter in 1968. In 1975, the overall power conversion efficiency achieved was up to 54% to deliver an output DC power of 495 W, using a magnetron in the Raytheon Laboratory [35]. This measurement scenario is illustrated in Figure I.3 (a).



(a)



(b)

Figure I.3: Different WPT experiment scenarios performed by W. Brown in 1975, (a) in the Raytheon Laboratory, (b) in JPL.

Brown also made part of the team, which succeeded in the largest WPT demonstration in 1975 at the Venus Site of the Jet Propulsion Laboratory (JPL), Goldstone Facility [36]. This time, a microwave power of 450 kW at a frequency of 2.388 GHz was transmitted throughout a parabolic

antenna measuring 26 meters of diameter, Figure I.3 (b). For the reception, rectennas array measuring 3.4 x 7.2 m was placed at a distance of 1.54 km from the transmitting antenna and the achieved rectified DC power of 30 kW was evaluated with 82.5% rectifying efficiency.

Although Brown has succeeded in the WPT field experiments, the system size was still large and high cost, which made it unfeasible for any realizable practical applications transmitting power at this magnitude.

All these advances in WPT, radar applications and wireless communication contribute to the development of radio frequency identification (RFID). Some inventions, such as “Remotely activated radio frequency powered devices” by Robert Richardson in 1963 and “Passive data transmission techniques utilizing radar beams” by J. H. Vogelman in 1968, [37], gave directions to the invention of the first RFID tags in the 1970s. The 1970s for RFID devices were characterized primarily by developmental work. Several patents were submitted, such as [38]-[40], where most intended applications were for animal tracking, vehicle tracking, and factory automation.



Figure I.4: Disposable RFID tags used for race timing.

In the 2000s, the development of mobile phones along with transistor technology scaling decreased considerably the required power supply of electronic devices. These achievements allowed the development of smaller portable systems and push WPT back into consideration for commercial applications. The concept that it is possible to receive enough power via microwaves, just as with wireless communication was introduced. This was designated “ubiquitous power source”, meaning that the source of microwave power is available every time and in everywhere in order to supply even batteryless electronic devices [41].

Today, besides the interest in developing low-cost RFID tags, Figure I.4, to identify products and replace bar codes, the popularity and applications of large-scale wireless sensor networks (WSN) are being widely employed in several fields, including military and urban applications.

The ability to power supply electronic devices without wires and the availability of internet everywhere aroused the idea that we can interact not only with contents in websites but also with real objects. This concept brought into play the possibility to live in so-called “Smart Cities”, Figure I.5, where wireless sensors are spread everywhere in order to get a fast access to information on critical issues which could interfere in the quality-of-life of the human being.

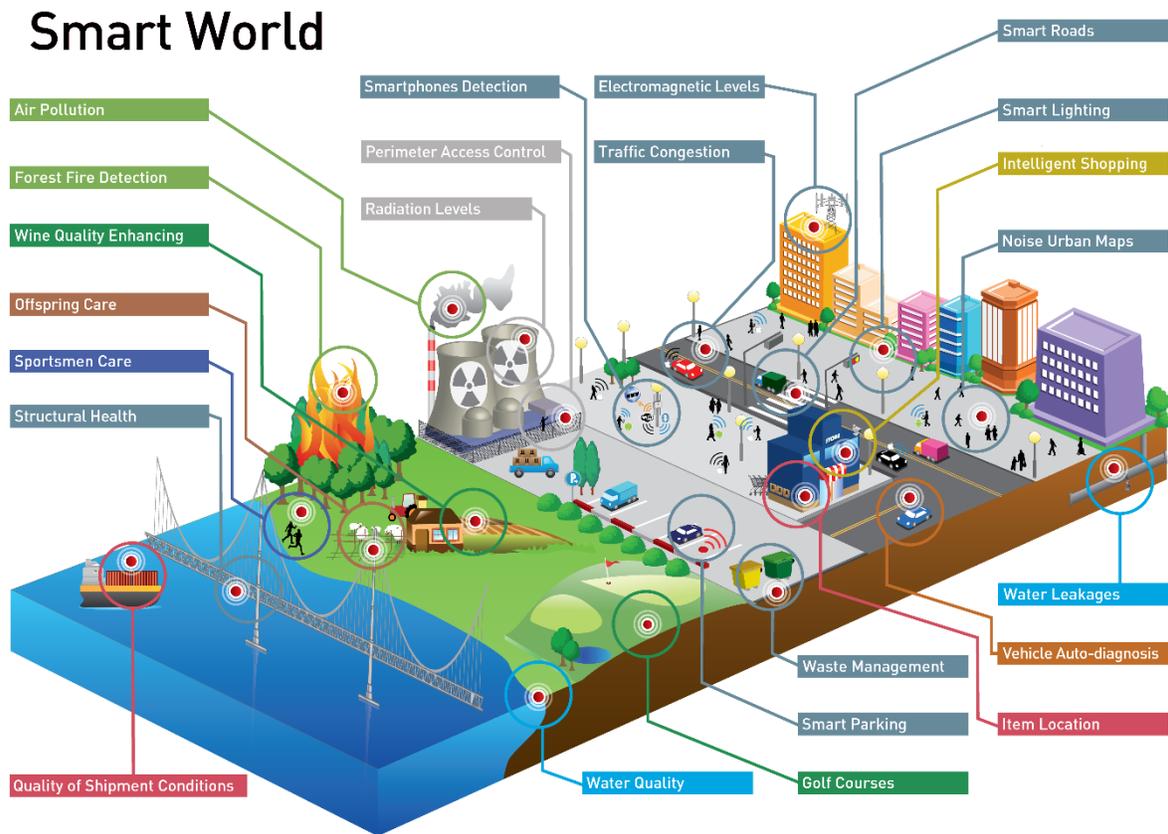


Figure I.5: Smart city concept.

With such increase in the interest in developing low cost WSN production and maintenance to hold the possibility in making smarter cities, RF energy harvesting might be a solution to effectively power supply some WSN among the several existing applications.

3 Approach for Long Distance Operation

WPT using RF as a means of energy propagation can typically be simplified as a 3-step process:

- First, the AC or DC electric power is supplied to a high frequency generator and, then, taken to the electromagnetic emitter structure.
- Second, the EM waves are propagated to the receiving structure through the air.
- And finally, the EM energy is captured and converted into DC current and then used to power supply a load.

There are mainly 3 system approaches which can be used to perform WPT considering this RF energy transmission process. They are known as:

- Inductive magnetic coupling,
- Resonant inductive coupling,
- Radiative transfer.

Since the first two systems operate using the magnetic field propagation between two coils, the receiving coil must be covered by the magnetic field of the emitting coil, which limits the system operating range. However, operating in a near-field region provides a high power conversion efficiency [42]-[43]. Due to this characteristic, this technique is widely employed in wireless charging applications, such as mobile phones and electric vehicles, Figure I.6.

Even if this systems can be very efficient and the resonant inductive coupling technique improves the operating range compared with its predecessor non-resonant [44], the overall range achieved is of only a few centimeters. For this reason, these short-range systems will not be further discussed in this thesis work, where systems operating at long distances are targeted.

Conversely, wireless energy can also be transmitted at longer distances throughout a radiation field. Circuits operating at these conditions are known as far-field systems. As mentioned in section I.2.1, the wirelessly transfer of large amounts of power over distances of several kilometers has already been achieved, using rectifiers with efficiencies of up to 80%. However, the number of feasible application today at these power levels is mainly restricted by two reasons:

physically, due to the antenna size required to operate at frequencies below UHF and, humanly, to the sanitary regulation standards. For these reasons, most WPT systems operating at long distance today are intended to low-power applications, such as RFID tags and WSN.



(a)



(b)

Figure I.6: Wireless charging solutions developed to supply (a) mobile devices by Powermat Technologies ltd., (b) electric vehicles by Witricity.

3.1 Principle of Wireless Power Transmission at far-field region

The wireless powered receiver (WPR) is a device capable of directly convert microwave energy into DC electricity. Other designations could be found in literature such as harvester, due to its ability to scavenge the surrounding energy from the environment, or rectenna, for embed together an antenna and a rectifier. During the last two decades, many works were focused on microwave WPRs operating in the UHF and SHF ISM bands [45]-[49]. Compared to the first high-power WPRs addressed in the 1960s and 1970s, these wireless receivers are typically intended for environments where the available microwave power is very low; a few milliwatts or less. They show RF-to-DC conversion efficiencies ranging approximately from 20% to 80%, depending on the amount of the required input power and the directivity of the antenna used.

The principle of wireless power transmission using a WPR is illustrated in Figure I.7. A transmitter generates a RF signal that drives the transmitting antenna. This antenna converts the RF signal in electromagnetic radio waves that create a specific power density P_d , expressed in W/m^2 , at each point in space. As will be seen in equation (I.3), this power density decreases in $\frac{1}{d^2}$, where d is the distance to the transmitter. The antenna of the WPR captures some power from its

surroundings (this power is available in the form of a specific power density P_d) and converts it in an alternating voltage. This voltage is converted in DC power with a rectifier, which can be implemented with a single diode in the simplest case. A large storage capacitor placed at the output filters the high-frequency ripples generated by the rectifier and provides a clean DC supply voltage to the output.

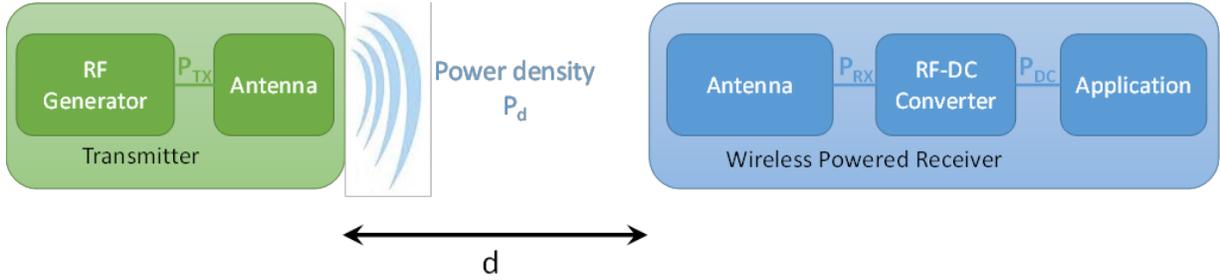


Figure I.7: Principle of WPT.

An electromagnetic (EM) wave is formed of two components (electrical, \vec{E} , and magnetic, \vec{B}), which travel through space carrying radiant energy. The behavior relation of these components depends on the propagating region where they are analyzed. For EM waves propagating in far-field region, \vec{E} and \vec{B} oscillate in phase, in perpendicular planes with respect to each other and relative to the direction of propagation, \vec{k} . Figure I.8 illustrates electrical and magnetic oscillations at far-field region. The components \vec{E} and \vec{B} obey the following relations:

$$\nabla^2 \vec{E} = \mu_0 \epsilon_0 \frac{\partial^2 \vec{E}}{\partial t^2} \tag{I.1}$$

$$\nabla^2 \vec{B} = \mu_0 \epsilon_0 \frac{\partial^2 \vec{B}}{\partial t^2} \tag{I.2}$$

Regarding the case of an isotropic emitting antenna, in a certain point in space the power is distributed uniformly over the surface of a sphere of radius d , where d is the distance between the transmitting antenna and the observation point. The power density at any point on the surface of the sphere can be written as:

$$P_d = \frac{P_{TX} \cdot G_{TX}}{4\pi \cdot d^2} \quad [\text{W/m}^2] \tag{I.3}$$

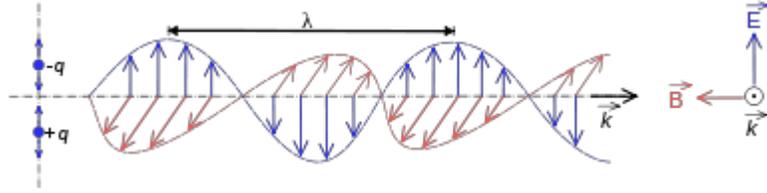


Figure I.8: The electromagnetic waves behavior at far-field region.

The product $P_{TX} \cdot G_{TX}$ is generally combined in a single parameter known as the effective isotropically radiated power (EIRP), equation (I.4) [50]. This figure can often be found in radio licensing regulations, where it is fixed to a maximum value, usually expressed in watts or dBm. By defining a maximum value for P_{EIRP} , the peak power density observed in the main radiation direction of the transmitting antenna is limited to a specific value, which is independent of the antenna design used in practice.

$$P_{EIRP} = P_{TX} \cdot G_{TX} \quad (I.4)$$

The power available at the receiving antenna, P_{RX} , is directly proportional to the effective area of a WPR antenna and to the power density P_d at the point where the antenna is located. P_{RX} is called the available power because it is the maximum power that can be obtained from the antenna terminals and can be expressed as:

$$P_{RX} = P_d \cdot A_e \quad (I.5)$$

where A_e is the effective area of an antenna, expressed in m^2 , and it is defined as the ratio of the available power at the terminals of a receiving antenna to the power flux density of a plane wave incident on the antenna [51]. This concept provides a way to relate the power density P_d around the antenna to the power P_{RX} that can be delivered to a matched load, Figure I.9. The effective area A_e of a receiving antenna with gain G_{RX} is given by:

$$A_e = \frac{\lambda^2}{4\pi} G_{RX} \quad (I.6)$$

Combining the equations (I.3) and (I.6) into (I.5), leads to a possible way to write the Friis transmission equation [52], (I.7), which relates the power received to the power transmitted between two antennas separated by a distance d large enough to ensure that far-field coupling condition can be assumed.

$$P_{RX} = P_{TX} G_{TX} G_{RX} \left(\frac{\lambda}{4\pi d} \right)^2 \quad (I.7)$$

It is noticed in this equation that the available power P_{RX} is proportional to λ squared. Thus, operating at lower frequencies allows to increase the available power for a given distance. However, the dimensions of antennas are proportional to the wavelength used, so this comes with the cost of larger wireless receiver sizes.

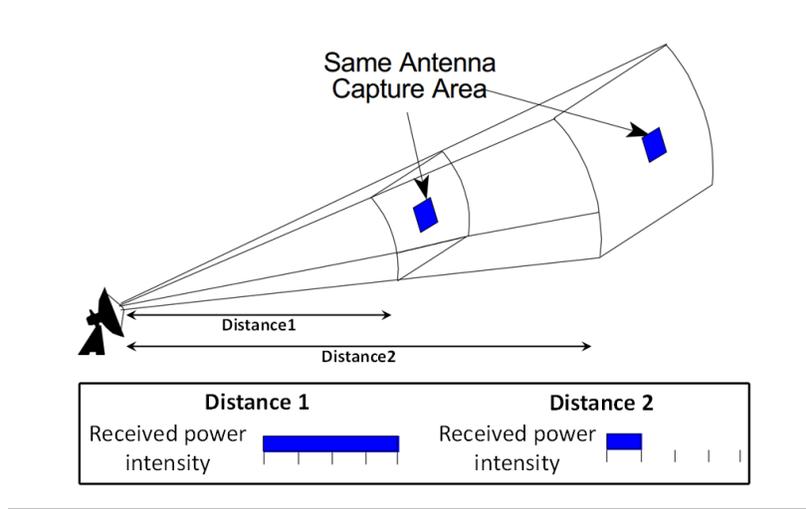


Figure I.9: Power density vs operating distance.

A limitation of Friis transmission equation, (I.7), is that it assumes systems operating in free space conditions. In a real-world propagation environment, the available power P_{RX} may significantly differ from the prediction using this equation. A reason for this is that, in a practical environment, the transmitted waves may reflect on different objects present in the antenna surroundings. Hence, the signal received by the wireless powered receiver (WPR) is the sum of several signals traveling along different paths and presenting different amplitudes and phases. This multipath effect modifies the way the transmitted power spreads into space. The polarization mismatch between the transmitting and receiving antennas, and their reflection coefficients when connected with other system circuits also contribute to the power transmission losses. An expression can be more accurately estimated from Friis transmission equation to also take into account these effects, (I.8).

$$P_{RX} = P_{TX} G_{TX} G_{RX} \left(\frac{\lambda}{4\pi d} \right)^2 (1 - S_{11})(1 - S_{22}) |\vec{u} \cdot \vec{v}|^2 \left(1 + \sum_{n=1}^N \Gamma_n \cdot \frac{d}{d_n} e^{-j\frac{2\pi}{\lambda}(d_n - d)} \right) \quad (I.8)$$

where S_{11} and S_{22} represents the reflection coefficients of the transmitting and receiving antennas, respectively. The term $|\vec{u} \cdot \vec{v}|^2$ considers the losses due to polarization mismatch, which is usually caused by antennas having different polarizations or by antennas having the same polarization but not aligned in relation to the electromagnetic waves propagation. Γ_n is the reflection coefficient of the n^{th} reflecting object (including ground), d_n is the length of the n^{th} reflected ray path, and N is the total number of reflections. The multipath effect is compensated by the sum expansion of the reflection coefficient of the n^{th} reflecting object [53].

Regarding the delivered DC power, P_{DC} , at the load, it can be defined as:

$$P_{DC} = \frac{1}{T} \int_T v_{OUT}(t) \cdot i_{OUT}(t) \approx V_{OUT} \cdot I_{OUT} \quad (\text{I.9})$$

where V_{OUT} and I_{OUT} are the RMS values of voltage and current supply delivered to an application.

As a parameter to evaluate the WPR performance, the power conversion efficiency compares the amount of continue power delivered to a load with the power available at receiving antenna terminals and can be expressed as:

$$\eta = \frac{P_{DC}}{P_{RX}} \quad (\text{I.10})$$

3.2 Equivalent Model for a Wireless Powered Receiver

Figure I.10 illustrates the equivalent circuit of a WPR supplying an application. The antenna impedance, which is the impedance seen at antenna terminals, is the combination of a resistance R_{ant} and a reactance X_{ant} . At the resonance frequency of the system, the reactive behavior of the antenna, X_{ant} , tends to cancel the reactive behavior of the following circuit attached to it, X_C . The resistive element, R_{ant} , is a combination of radiation resistance, R_{rad} , and loss resistance R_{loss} of an antenna. The impedance of the circuitry attached to the antenna is divided into resistive and reactive elements, represented by R_C and X_C , respectively.

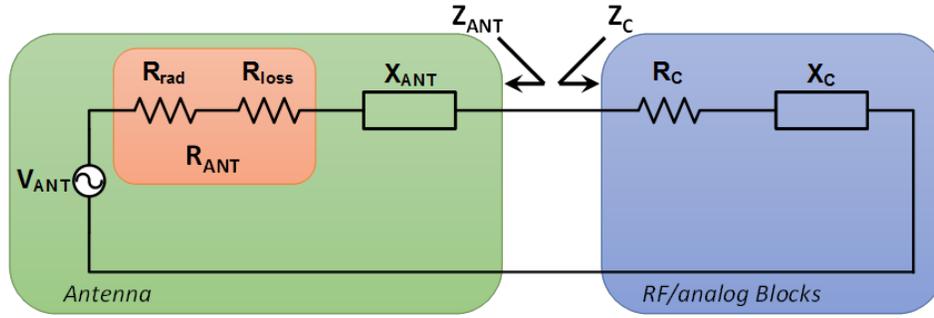


Figure I.10: Equivalent circuit of a WPR.

The incident electromagnetic waves at the antenna surface induces the generation of AC currents, which flows along the antenna path. In the equivalent circuit, this conversion mechanism is represented by an AC voltage source, V_{ant} . The current flowing through the antenna is dissipated in resistors R_{rad} , R_{loss} and R_C . The power dissipated in R_C corresponds to the useful power transferred to the following circuits and must be optimized in order to power supply an application. The power dissipated in R_{loss} is wasted as heat, whereas in R_{rad} the power dissipated is radiated as electromagnetic waves. Therefore, antennas presenting the ratio $\frac{R_{loss}}{R_{ant}}$ tending to zero are considered efficient.

The maximum power is delivered to the load in the matching conditions, which occurs when:

- $R_{ant} = R_C$
- $X_{ant} = -X_C$

In other words, the antenna impedance Z_{ant} is equal to the complex conjugate of the circuit impedance, Z_C^* . In these conditions and assuming a lossless antenna ($R_{loss} = 0$), half of the captured power is delivered to the circuit and the other half is re-radiated. This indicates that in order to deliver half of the power to the circuit, the other half must be re-radiated.

The input impedance of an antenna is generally a function of frequency [51]. Thus the antennas can be matched to circuits connected to them only within a limited bandwidth. In addition, the input impedance of the antenna depends on many factors including geometry, its method of excitation, and its proximity to surrounding objects. Because of their complex geometries, most of practical antennas developed in this work have also been investigated electromagnetically, besides the theoretical analysis, and are further discussed in Chapter III.2.

3.3 Behavioral model at resonance

Considering a WPR with a lossless antenna and that the system is operating at its resonance frequency, the loss resistor R_{loss} and the reactances X_{ant} and X_C of the model illustrated in Figure I.10 can be disregarded. The antenna can be seen as an alternating voltage source V_{ant} with only an input resistance of R_{rad} . As the wireless receiver operates at its resonance frequency, the antenna and circuit reactances, X_{ant} and X_C , cancels each other. Hence, the behavioral WPR model can be simplified as shown in Figure I.11. Using this simplified model, the relation between the available power P_{RX} and the properties of the AC voltage source V_{ant} can be easily analyzed.

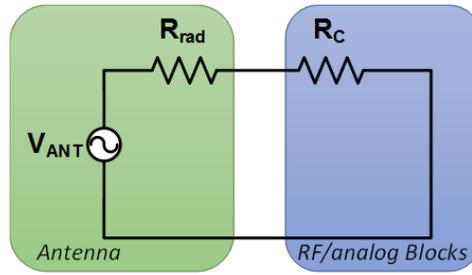


Figure I.11: Equivalent circuit of a WPR with a lossless antenna operating at resonance frequency.

The source generates an alternating voltage that can be represented by:

$$V_{ant}(t) = \hat{V}_{ant} \sin(\omega t) \quad (\text{I.11})$$

where \hat{V}_{ant} is the amplitude of the alternating signal generated through the antenna and $\omega = 2\pi f$, with f being the frequency of the radio waves captured by the antenna. The time varying voltage across the circuit model R_C can be characterized by its amplitude, \hat{V}_C , which can be defined as:

$$\hat{V}_C = \frac{R_C}{R_{rad} + R_C} \hat{V}_{ant} \quad (\text{I.12})$$

The power consumption required by the circuit represented as R_C can be expressed as:

$$P_{RX} = \frac{\hat{V}_C^2}{2R_C} = \frac{\hat{V}_{ant}^2}{2} \frac{R_C}{(R_{rad} + R_C)^2} \quad (\text{I.13})$$

Considering the maximum energy transfer theorem, the available power P_{RX} achieves its maximum value when the equivalent antenna resistance R_{ant} is matched to the circuit resistance R_C , ($R_{rad} = R_C$). Hence, the maximum power transferred to the circuit is:

$$P_{RX_{max}} = \frac{\hat{V}_{ant}^2}{8R_{rad}} \quad (I.14)$$

With increasing demand to supply low-power applications requiring high efficient circuits (represented by low R_C values using series model), it is expected that the available R_{ant} is as low as R_C to ensure the maximum energy transfer. Therefore, optimizing circuits to present low R_C is as important as developing antennas with low equivalent resistance R_{ant} , which is limited by the antenna constraints, such as materials and geometry.

3.4 Feasibility in the communication frequency spectrum

Knowing that WPT systems generate and radiate RF electromagnetic waves, they can be classified as radio systems. The function of other radio services as radio, television, mobile telephones must under no circumstances be disrupted or impaired by the operation of WPT systems. Therefore, some heed is necessary concerning the use of radio communication spectrum, which significantly restricts the range of suitable operating frequencies available to a WPT system. A few frequency ranges have been reserved specifically for industrial, scientific or medical (ISM) applications. These are the frequencies classified worldwide as ISM frequency bands, and, thus, they can also be used for WPT applications.

The most important frequency bands for WPT systems are in 0-150 kHz range, and the ISM frequencies around 6.78MHz, 13.56MHz, 27.12MHz, 40.68MHz, 433.92MHz, 867MHz, 915MHz, 2.45 GHz, 5.8 GHz, 24.125 GHz, 61.25 GHz, 122.5 GHz and 245 GHz [4], [111]. The WPT modules addressed in this thesis operate in far-field conditions, at ranges of a few meters with a nominal power consumption under the milliwatt.

Considering the lower operating frequency range, some issues can be identified. Firstly, the system minimum operating distance corresponding to far-field (approximately achieved after a distance of 2λ) is much larger than the aimed range of a few meters. This can be easily noticed at the numerical examples given in TABLE I.2. Secondly, the size of the transmitter and receiver

antennas are proportional to the wavelength λ . Thus, either they have to be huge, which makes wireless receivers less suitable for small applications, or they have to operate with poor performances and the harvester probably will not collect enough power for a proper operation. For all these reasons, the operating frequency at 433.92 MHz and below are not suitable for small WPRs and are disregarded in this work context.

TABLE I.2 Characteristics of systems operating at different ISM bands.

Frequency	150 kHz	13.56 MHz	434 MHz	900 MHz	2.4 GHz	5.8 GHz	24 GHz
Wavelength	2 km	22.1 m	69 cm	33.3 cm	12.5 cm	5.2 cm	1.25 cm
Far-field Condition	>4 km	>44.2 m	>138 cm	>66.6 cm	>25 cm	>10.4 cm	>2.5 cm
Distance¹	50 km	556 m	17.4 m	8.4 m	3.14 m	1.3 m	31 cm
FSPL² [dB]	Near-field	Near-field	39.2	45.5	54	61.7	74

¹ Distance to receive -20 dBm sending 30 dBm considering a 0 dBi receiver antenna

² Free-Space Path Loss (FSPL) for a distance of 5 m

Regarding the ISM bands for circuits operating at higher frequencies, another issues arise. The main one is the free-space path loss (FSPL), which increases proportionally to the square of the distance between the transmitter and receiver, according to (I.15). In other words, the propagation distance of the transmitted power is directly influenced by the radio signal frequency wavelength due to the λ^2 factor. Consequently, reaching an operating range of a few meters is really challenging with carriers frequencies of 5.8 GHz and above.

$$FSPL = \left(\frac{4\pi d}{\lambda} \right)^2 \tag{I.15}$$

In conclusion, the choice for suitable ISM frequencies to supply fully passive devices and far-field WPRs addressed in this thesis are a tradeoff between the operating distance and the overall WPR size. Hence, the energy carrier frequencies investigated in this work are the 900 MHz and 2.45 GHz ISM bands. Furthermore, RF sources operating at these frequencies are allowed by standard regulations to transmit more powerful signals in indoor/outdoor environments, which provides higher power densities for the WPRs. TABLE I.3 summarizes some rules established by FCC for low-power, non-licensed transmitters.

TABLE I.3 Federal Communication Commission (FCC) regulations for some ISM frequency bands [54].

Frequency Band	Type of Use	Emission limit
110-160 kHz	Any	$\frac{2400}{f[\text{kHz}]}$ $\mu\text{V/m}$ @300m
13.553-13.567 MHz	Any	10 mV/m @30m
410-470 MHz	Any	200 $\mu\text{V/m}$ @3m
806-902 MHz	Any	200 $\mu\text{V/m}$ @3m
902-928 MHz	Spread Spectrum Transmitters	1 Watt max output power (or 36 dBm EIRP)
	Field Disturbance Sensors	500 mV/m @3m
	Any	50 mV/m @3m
2.4-2.4835 GHz	Spread Spectrum Transmitters	1 Watt max output power (or 36 dBm EIRP)
	Any	50 mV/m @3m
2.435-2.465 GHz	Field Disturbance Sensors	500 mV/m @3m
5.725-5.85 GHz	Spread Spectrum Transmitters	1 Watt max output power
	Any	50 mV/m @3m
5.785-5.815	Field Disturbance Sensors	500 mV/m @3m
24.075-24.175 GHz	Field Disturbance Sensors	2.5 V/m @3m
	Any	250 mV/m @3m

3.5 Technology Choice

Considering the large-scale production feasibility, in many power harvesting applications, such as WSNs and RFID, the cost prevails over the performance. As further discussed in Chapter II.2.3, Schottky diodes are considered as an attractive candidate to perform the charge transfer task due to their low forward voltage drop and fast switching speed. However, Schottky diodes are not supported in all CMOS technologies which restricts their use in low-cost applications. Therefore,

a standard CMOS technology was chosen to implement the rectifier design. The Back-End-Of-the-Line (BEOL) of some technologies are illustrated in Figure I.12.

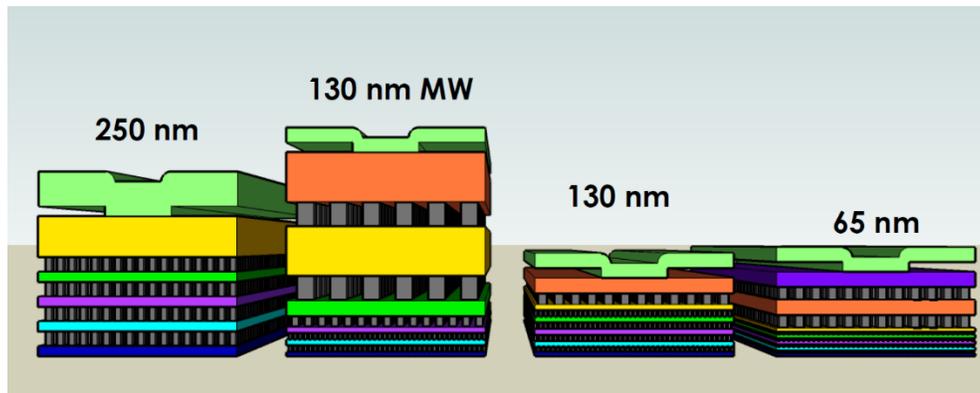


Figure I.12: BEOL of different silicon technologies.

The technologies having thicker metals more distant from the substrate, as 250 nm and 130 nm MW, are better from the point of view of RF losses, which improves:

- PADs losses associated to the circuit,
- RF tracks used to rout the devices, avoiding undesired RF losses to the substrate,
- Passives performances.

However they are also more expensive, hindering the large-scale production.

Another technology widely used due to very low production cost is the 0.35 μm . However, even if it is a cheaper solution, this technology does not present any devices intended for UHF applications, which increases much the undesired RF losses in the system. In a tradeoff between performance and large-scale production cost, the 65 nm and 130 nm CMOS technology appears as good solutions to implement RF circuits.

Comparing both of them, the RF losses not change much, since the distance from the higher metal to the substrate and the metal thickness are very similar in these technologies. In terms of devices performance, both technologies should present equivalent results, not showing much difference in case of scaling to 65 nm technology. The 130 nm is a more mature technology, which makes it cheaper than 65 nm in terms of cost. Therefore, the technology chosen to perform the ICs intended to the WPRs developed in this work is the 130 nm.

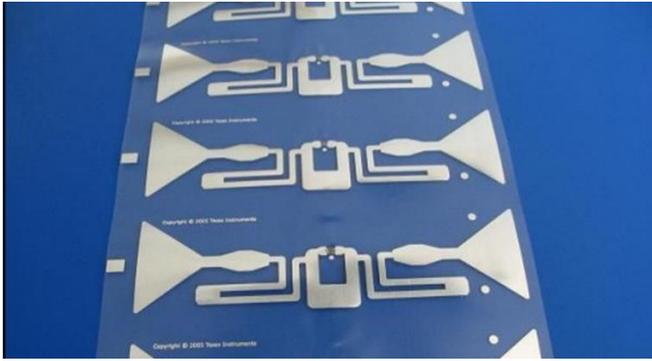
4 Recent Trends in WPT Applications

RF-powered devices provide an enabling technology for the deployment of low-cost wireless devices. Such devices rely on the extraction of energy from propagating radio waves instead of internal power sources. Many biomedical implanted equipment exploit radio waves to extend their lifetime. Other possible applications also include telemetry systems, structural monitoring, and home automation. Today, it can be highlighted two main applications using RF-powered systems to replace internal batteries and operate at long distances: Passive radio frequency identification (RFID) systems and Wireless Sensor Networks (WSN).

4.1 RFID

Every passive, far-field RFID tag uses the principle of the WPT to generate its internal DC supply voltage. In the context of RFID, the reader plays the role of the transmitter, while the WPR is embedded in the tag. This communicating principle led off to countless applications since its first introduction in the 1970s. This technology is commonly used in transportation, logistics, manufacturing, processing and security [55]. Just to provide a few examples, RFID is nowadays used for preventing theft of automobiles and merchandise, collecting tolls without stopping, managing traffic, building access control, automatic parking, controlling access of vehicles to gated communities, corporate campuses and airports, dispensing goods, ski lift access, tracking library books, railway rolling stock identification, movement tracking, and last but not least, for supply chain and retail stock management [56]-[60].

Tags are available in a wide variety of shapes, sizes and protective housings. Animal tracking tags are approximately 10 mm long and 1 mm in diameter and injected beneath the skin. Tags intended for access control are often encapsulated in credit card or key case sized packages. The smallest devices commercially available measure 0.4 x 0.4 mm and are thinner than a sheet of paper [55]. Figure I.13 shows some examples of RFID tags, which are becoming common in everyday life.



(a)



(b)

Figure I.13: Commercial RFID tags used in (a) tracking and logistics management, (b) passports.

The biometric passport is a typical application of RFID to the security area. Some companies, such as Smartrac and Smart Packaging Solutions, market the so-called “ePassport inlays”. This product contains a chip embedded within a sheet of paper, which stores the same personal information printed in the passport, including the digital picture of the owner.

4.2 WSN

Wireless sensor network is an emerging technology with a great potential in several applications. The ability to add remote sensing points, without the need of running wires, results in many advantages including energy and material saving costs. Several application fields may benefit from WSNs, such as medical applications. Over the last few years, it has been noticed the increase growth of body sensor network platforms and number of wireless sensor nodes for monitoring different types of biological and physiological signals [61]. These sensor nodes differ by form factor, autonomy, and their building blocks, but they all face the same technological challenges such as autonomy, functionality and manufacturing costs.

A leading sector concerning the development of wireless sensor networks is the automotive. Increasingly, sensors are placed in cars to provide safety, convenience and affordability. Tire pressure monitoring systems (TPMSs) are examples of WSNs used for safety, Figure I.14.

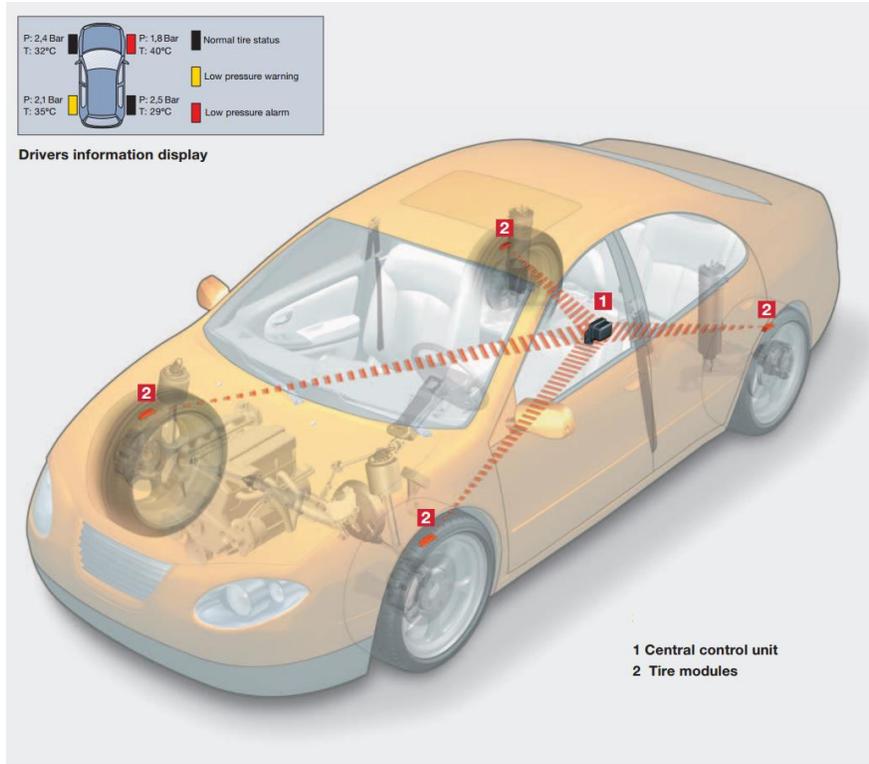


Figure I.14: Tire pressure monitoring system.

Today such systems are powered by relatively large batteries, which limit both data transmission frequency and overall system lifetime. To overcome these limitations, WSN applications may be powered by wireless energy harvesting systems.

Environmental and structural monitoring is another important application field of WSNs. Sensors embedded into these applications enable condition-based control and maintenance. Habitat monitoring at Great Duck Island, [62], [63], is an example. Wireless sensor networks monitor the microclimates in and around nesting burrows used by the Leach's Storm Petrel (a particular species of duck). Their goal is to develop a habitat monitoring kit that enables researchers worldwide to engage in the non-intrusive and non-disruptive monitoring of sensitive wildlife and habitats. These typical usages of WSN are for cases with low data rate, small data size, low duty cycle, and extreme emphasis on low power consumption.

Regarding structural health monitoring applications, structures or machines are inspected at regular time intervals, and components are repaired or replaced based on their hours in service or on their working conditions. However, this approach is expensive if the components are in good working order or if a damage occurs between two inspection intervals. Thanks to wireless sensing

devices, equipment may be inspected when it is needed, reducing maintenance costs and preventing possible catastrophic failures. Applications of WSN to monitor large civil infrastructures are good examples, such as the WSNs deployed on the Golden Gate Bridge to measure ambient structural vibrations [64].

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Chapter II

Chapter II. Design and Characterization of Rectifiers for Low-Power Applications

1 Introduction

The rectifier circuitry is found in almost all of today's electrical appliances which demand a DC voltage as energy supply. They are components responsible for the conversion from the mains AC voltage/current supply into a DC output voltage. The most common example of this use is the battery charger, very used to power supply devices such as computers, mobile phones, cameras, etc.

With the growing demand for wireless electronic devices, rectifiers have recently been increasingly subjects of study in systems operating at UHF bands for power supply circuits without the need of internal batteries. Converting the EM energy into DC, these systems are capable of identifying objects and supply remote devices with a reduced need for maintenance, such as passive RFID TAG, WSN, etc.

In Wireless Energy / Power Transmission (WE/PT) scenario, the RF / DC conversion circuit can be seen as the third phase of the Wireless Energy Harvesting (WEH) process. The essential module of a Wireless Powered Receiver (WPR) is the RF / DC converter, since it is the block which provides the necessary power-supply for any given electronic circuit, sensors, etc. Figure II.1 shows the simplified block diagram of a WPR, which generally consists of a receiving antenna, a matching network, a stage of diode-based rectification and a storage device.

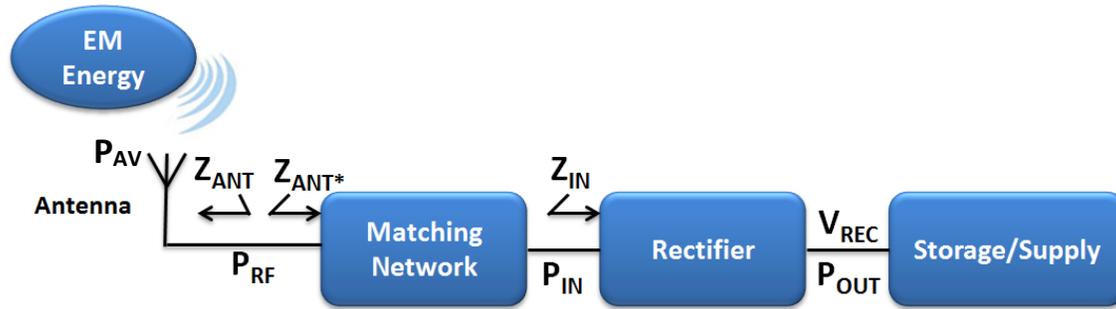


Figure II.1: Simplified building block structure of a wireless powered receiver.

The matching network yields the impedance matching between the antenna and the rectifier block in order to avoid returning losses and so maximizing the energy transfer. The storage device can be seen as a low-pass filter, which rejects the higher order harmonics generated during the nonlinear rectification process. The output load is any type of device supplied by a DC power.

The power conversion efficiency of a rectifier is influenced by the amount of power lost in the devices (transistors or diodes), the quality of the impedance matching and the RF to DC converter module, together with the efficiency of the antenna. The full wireless power receiver module is further detailed in Chapter 3. In this chapter only the rectifier block issues are discussed and detailed in the following sections.

2 Rectifier Architectures

As mentioned, the rectifier architectures are RF to DC converters to power-supply a load from the EM waves sent by a wireless power transmitter and/or from EM waves already existing at the environment sent by other wireless devices. The rectifier is loaded by an energy storage element, in the case of energy harvesting, or a circuit, in the case of Wireless Power Transfer. Most of UHF rectifiers commonly used today for this type of system are based on the power electronics topologies used for high-energy physics experiments and lightning safety test, such as the Cockcroft-Walton generator [65].

Rectifiers are divided into two classes:

- Half wave rectification – which recovers only the energy of one cycle (Either positive cycle, or negative cycle)

- Full wave rectification. – which recovers the energy of both cycles.

2.1 Half wave rectifiers

2.1.1 Series Architecture

The simplest half wave rectifier can be made using a single diode as shown in Figure II.2 (a).

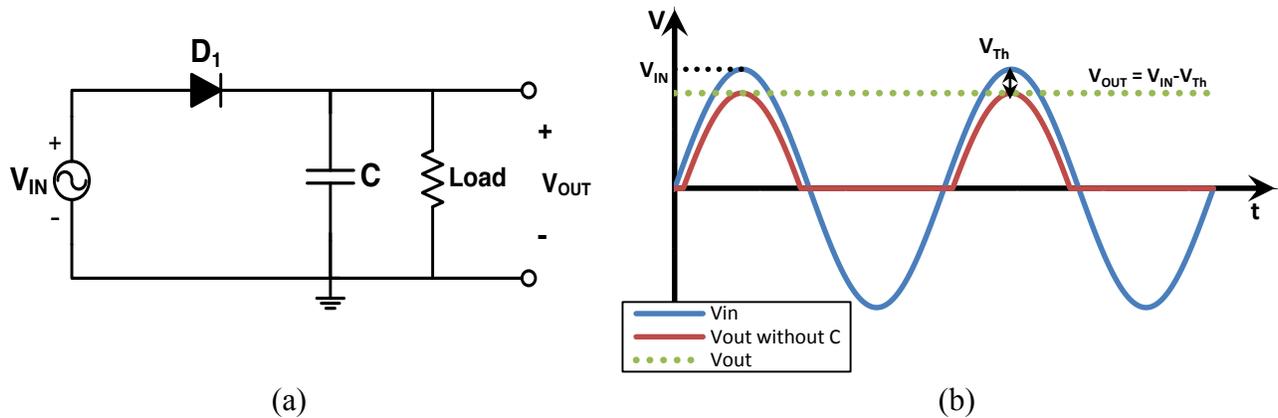


Figure II.2: a) Series rectifier configuration, b) Voltages' waveforms as function of time at steady state condition.

In this circuit, the load is purely resistive and ideally current can only flow in one direction thanks to the blocking action of the diode. During the positive half cycle of the AC supply, V_{IN} , the diode D_1 is forward biased and current starts to flow to the load. Then, during the alternate negative cycle of V_{IN} , D_1 becomes reversed biased and the output current is blocked. Hence, the circuit is known as a half wave rectifier. Concerning the DC output ripple, for half wave rectification is at the same frequency as the AC supply.

A capacitor C added at the output will store charges and progressively build a DC voltage V_{OUT} . The diode D_1 will only turn on if the absolute value of V_{IN} becomes larger than $V_{OUT} + V_{Th}$, where V_{Th} is the diode drop voltage. At steady-state, when no load is connected to the output V_{OUT} , C has built a voltage that is large enough so that the diodes do not turn on anymore. As shown in Figure II.2b, the output voltage is constant and stabilized to:

$$V_{OUT} = \hat{V}_{IN} - V_{Th} \quad (II.1)$$

If the rectifier is performed with an ideal diode, (II.1) simplifies to:

$$V_{OUT} = \hat{V}_{IN} \quad (II.2)$$

Depending on the operating power, rectifiers implemented with Schottky diodes, which have a low threshold voltage V_{Th} , generate an output voltage that can be very close to this theoretical value.

2.1.2 Shunt Architecture

In the shunt topology represented in Figure II.3 (a), the diode is connected in parallel between the input coupling capacitor and the output storage capacitor. The anode or cathode of the diode is connected to ground, depending on the voltage polarity desired.

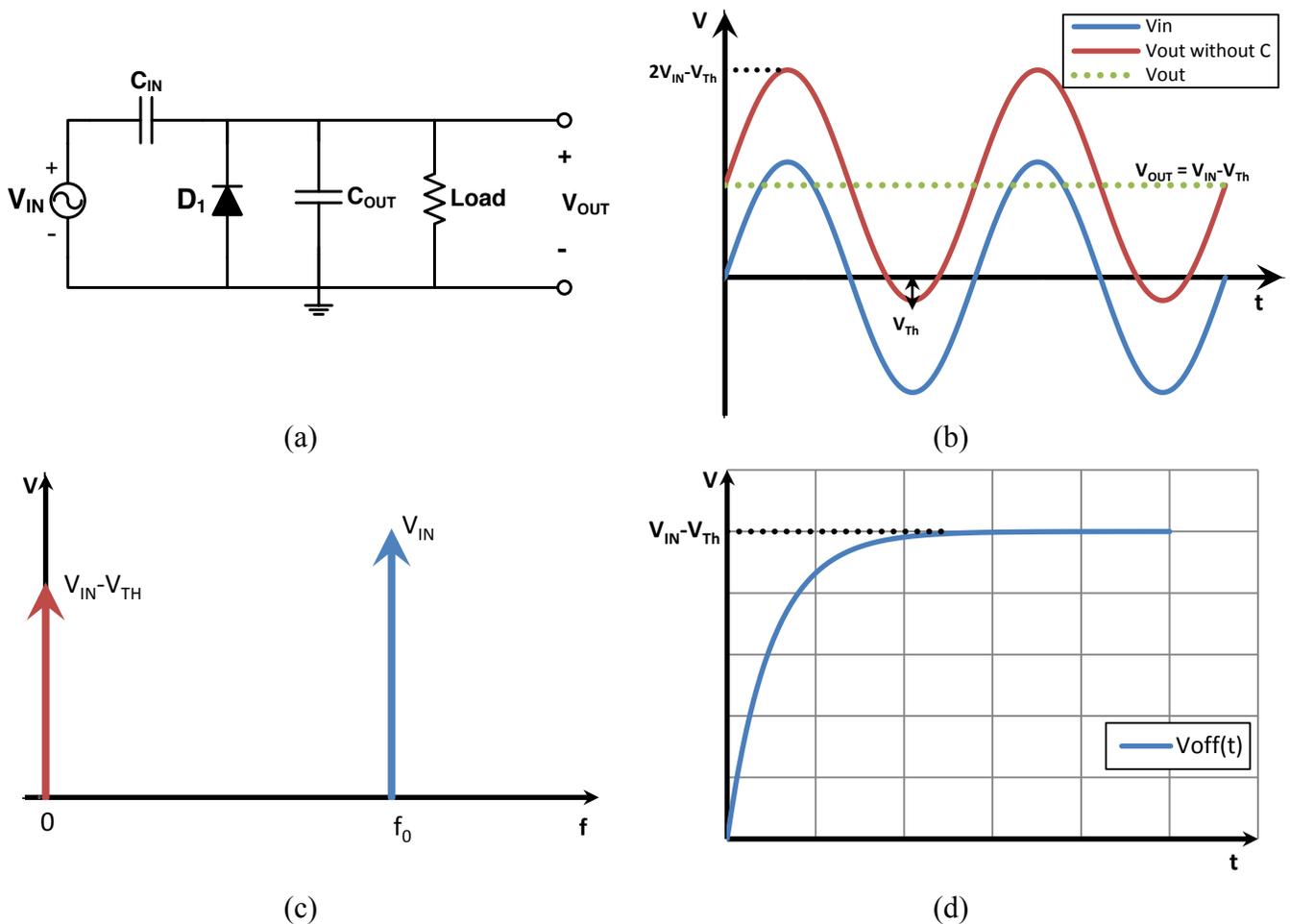


Figure II.3: a) Shunt rectifier configuration, b) Waveforms as function of time at steady-state, c) V_{OUT} spectrum, (d) V_{off} as a function of time.

Considering the case where a positive output voltage is desired and at steady state condition, the diode is directly polarized by a DC offset voltage, V_{off} , generated by the structure plus the input voltage V_{IN} .

Analyzing the operating principle, during the negative half cycle, the diode D_1 is turned on and the charge start to be stored into the input capacitor, generating in this way an offset voltage $V_{\text{off}}(t)$ represented in Figure II.3 (d). This phenomena occurs until the stabilization of V_{off} voltage, (II.4). During the positive half cycle, the diode D_1 is blocked and the energy is transferred from the input capacitor to the storage capacitor, which behaves as in the case of the single diode structure connected in series, filtering the RF signal and recovering only the DC voltage.

Thus, the expression of the output voltage can be estimated as:

$$V_{\text{OUT}}(t) = V_{\text{IN}}(t) + V_{\text{off}}(t) \quad (\text{II.3})$$

where, at steady state:

$$V_{\text{off}} = \hat{V}_{\text{IN}} - V_{\text{Th}} \quad (\text{II.4})$$

If the rectifier is performed with an ideal diode, (II.4) simplifies to:

$$V_{\text{off}} = \hat{V}_{\text{IN}} \quad (\text{II.5})$$

Despite this structure is able to provide a peak output voltage higher than the input voltage, when connected to the storage block and the load, only the DC component of the V_{OUT} is recovered and delivered to the load, i.e. only V_{off} is available to the load.

2.1.3 Voltage Multiplier Architecture

The voltage multiplier architecture, Figure II.4 (a), can be seen as the connection between the series and shunt structures described above. The circuit is driven by an AC source with amplitude \hat{V}_{IN} .

Concerning the voltage multiplier operation, at startup, capacitor C_{IN} of the shunt circuit is discharged. C_{IN} is large enough so that it represents a negligible impedance at the operating frequency. It can thus be considered as a short-circuit, and the voltage $V_{\text{CG}}(t)$ starts to follow the source voltage V_{IN} at the beginning until its steady-state condition represented in Figure II.4 (b). During the negative half cycle of the RF input signal, when $V_{\text{IN}} < -V_{\text{Th}1}$, the diode D_1 turns on and limits $-V_{\text{CG}}$ to $-V_{\text{Th}}$ while diode D_2 is blocked since $V_{\text{CG}}(t) < V_{\text{OUT}}(t) - V_{\text{Th}2}$. The charge

then starts to be transferred to the input capacitor C_{IN} , which progressively builds a DC voltage that tends to prevent $V_{CG}(t)$ from going negative. The DC offset voltage of $V_{CG}(t)$ at steady-state is therefore $\hat{V}_{IN} - V_{Th}$.

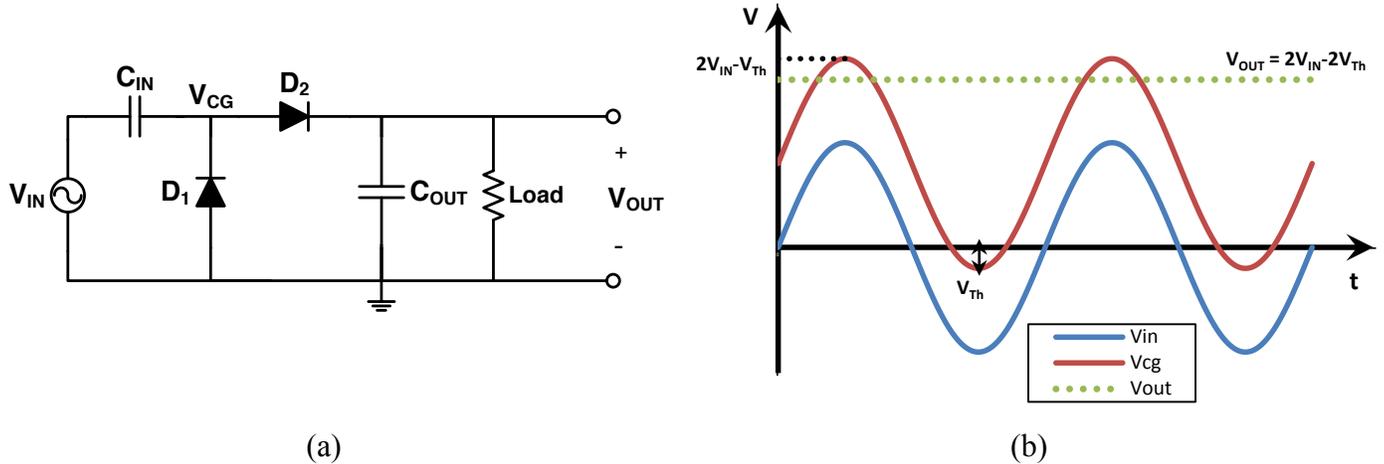


Figure II.4: a) Voltage multiplier configuration, b) Waveforms as function of time at steady-state.

When the input changes to the positive half cycle, the diode D_1 turns off while diode D_2 turns on and the charge is transferred from the capacitor C_{IN} to the capacitor C_{OUT} . The capacitor C_{IN} is the coupling capacitor, which is responsible for the electric charge transfer. At the end of the cycle, the energy is stored in C_{OUT} , storage capacitor. The final available output voltage V_{OUT} is expressed as:

$$V_{OUT} = 2\hat{V}_{IN} - V_{Th1} - V_{Th2} \quad (II.6)$$

Considering that non-linear devices are the same, i.e. $V_{Th} = V_{Th1} = V_{Th2}$ the expression simplifies to:

$$V_{OUT} = 2(\hat{V}_{IN} - V_{Th}) \quad (II.7)$$

Combining a shunt structure with a series structure provides the alternate input voltage increase through the shunt module. The series module allows the transfer of this energy available at its input to the storage capacitor. As we can realize from (II.7), the advantage of this architecture is the ability to provide an output voltage indeed higher than the amplitude RF input signal.

2.1.4 N-Stage Voltage Multiplier Architecture

For even higher power supply voltages, it is possible to take advantage of the ability to duplicate the voltage of the Voltage multiplier previously analyzed and built an architecture cascading several cells of it, as shown in Figure II.5. This architecture is known as n-stage voltage multiplier.

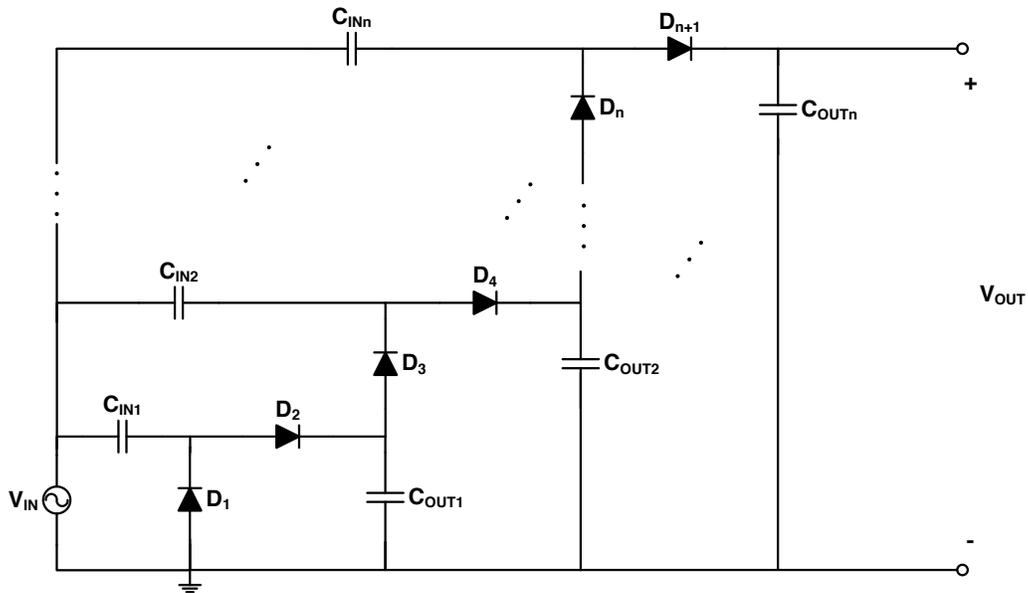


Figure II.5: N-Stage voltage multiplier configuration.

In this case, a higher output voltage is obtained through the accumulation of stored charge transferred from the output of one stage to the input of the following. After cascading several voltage multipliers, the generated voltage at C_{OUTn} is multiplied by the number of used stages:

$$V_{OUT} = 2N(\hat{V}_{IN} - V_{Th}) \tag{II.8}$$

Equation (II.8) figures out that the threshold voltage has a significant effect on the output voltage in an n-stage configuration, since the diode losses is multiplied by 2 times the number of stage employed.

2.2 Full-Wave Rectifiers

2.2.1 Bridge Architecture

The bridge rectifier architecture shown in Figure II.6 (a) is very common and widely used in HF contact-less smart cards [66]. The circuit is driven by an AC source V_{IN} with amplitude V_{IN} . The principle of this circuit is easier to understand by first assuming that there is no output capacitor C_{OUT} .

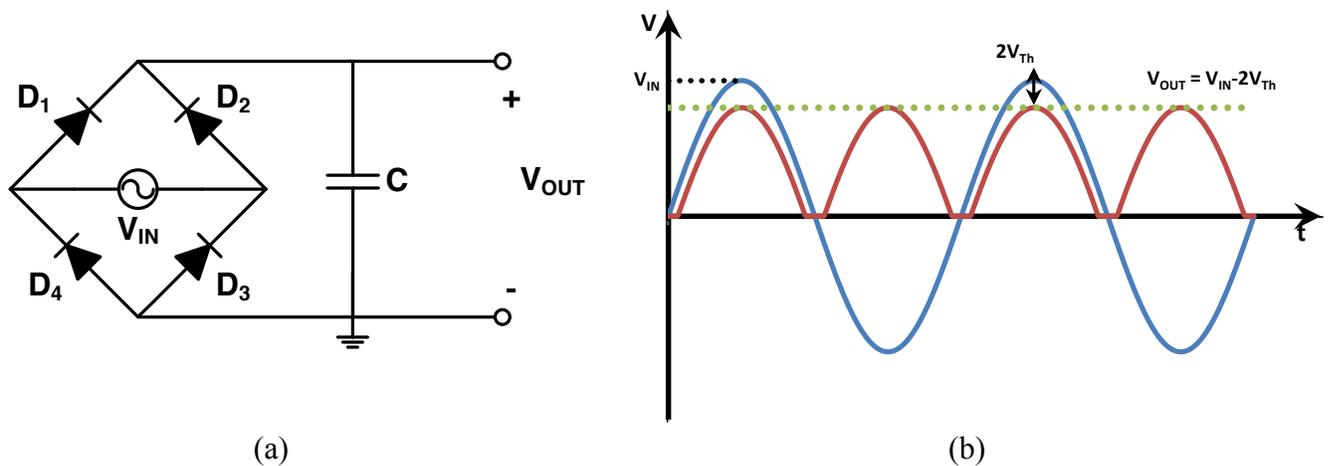


Figure II.6: a) Bridge rectifier configuration, b) Waveforms as function of time.

This circuit starts operating as soon as the amplitude of the input signal reaches twice the threshold voltage V_{Th} of the diodes. When V_{IN} is positive, the diodes D_1 and D_3 are turned on while D_2 and D_4 are turned off. A current flows from the source to the output through D_1 and D_3 . The voltage at the output V_{OUT} follows the source voltage V_{IN} , with a negative offset of $2V_{Th}$ caused by the presence of two series diodes. Conversely, when V_{IN} is negative, the diodes D_2 and D_4 are turned on while D_1 and D_3 are blocked. A current flows from the source to the output through D_2 and D_4 . Note that this current flows in same direction than the current flowing through D_1 and D_3 when V_{IN} is positive. This time, the voltage at the output V_{OUT} follows the opposite of the source voltage V_{IN} , with an offset of $2V_{Th}$.as represented in Figure II.6 (b).

A capacitor C added at the output will store charges and progressively build a DC voltage V_{OUT} . The diodes D_3 and D_4 will only turn on if the absolute value of V_{IN} becomes larger than $V_{OUT} + 2V_{Th}$. At steady-state, when no load is connected to the output V_{OUT} , C_{OUT} has built a

voltage that is large enough so that the diodes do not turn on anymore and the output voltage is constant and stabilized to:

$$V_{OUT} = \hat{V}_{IN} - 2V_{Th} \quad (II.9)$$

2.2.2 Full Wave Voltage Multiplier

The differential structure is built from half wave assembly described in Figure II.4 by duplicating symmetrically this basic cell as represented in Figure II.7. The direction inversion of the diodes in the inferior part of the circuit provides a negative voltage V_{OUT-} .

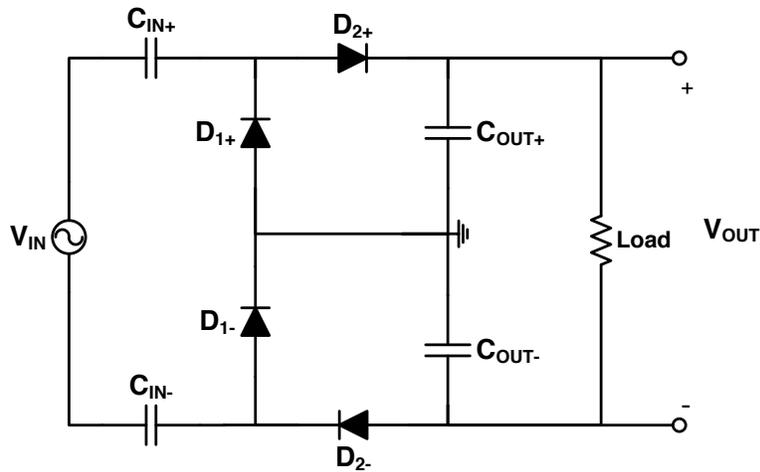


Figure II.7: Full wave voltage multiplier architecture.

The behavior of this architecture is similar to the voltage multiplier described in II.2.1.3. The difference is that the voltages delivered to the terminals are in opposition to each other. Therefore, the output voltage available for the charge at the output can be expressed as:

$$V_{OUT} = V_{OUT+} - V_{OUT-} = 4(\hat{V}_{IN} - V_{Th}) \quad (II.10)$$

It is interesting to note that in this case, unlike the half-wave rectification, the input voltage and output are not referenced to the same potential and the delivered output voltage to the charge do not have ground as reference. Moreover, the ripple amplitude is 2 times increased when compared to the half wave rectification.

2.3 Implementation of the Diodes

RF / DC converters are generally based on diodes or transistors. Most rectifiers have been performed using Schottky diodes, since they have low forward voltage drop, low substrate losses and fast switching speed. However, their integration is complex and expensive. Thus, they are not supported by standard CMOS technologies which focuses on low-cost applications throughout a high level of integration.

One of the aims of this thesis is to perform a WPR in a standard CMOS process at minimum cost. Such process do not provide Schottky diodes, nor any kind of diode with HF performances. Therefore, it is necessary to rely on another approach to realize one of the rectifying circuits previously discussed. The diodes are implemented with diode connected MOS transistors (DCMT), as shown in Figure II.8. The transistor has its gate shorted to its drain.

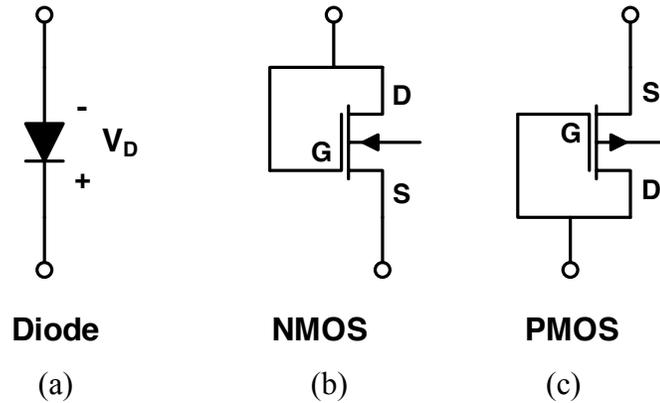


Figure II.8: a) Diode, DCMT (b) NMOS, (c) PMOS

Compared to the I_D - V_D characteristic of a real diode, the characteristic of a DCMT has several differences, such as a larger threshold voltage V_{Th} , which means that a rectifier built with these diodes will generate a lower output voltage, as can be deduced from (II.8) and (II.10) for example. If a load is connected to the rectifier output, a DC current flows from the source to the load, and passes through all the DCMTs. Since they have a limited conductivity, the voltage drop induced by each DCMT significantly increases, which further deteriorates the output voltage.

Conversely, a Schottky diode has an excellent conductivity once forward biased. The voltage drop caused by the diode is small and remains quite constant when the forward current increases. If the diodes in the rectifiers previously discussed suffer from reverse leakage, this causes a fraction of the charges stored in the output capacitor C_{OUT} to flow back to the source or

to ground. This effect, which is typically stronger for DCMTs than diodes, has a negative impact in terms of output voltage and power efficiency.

3 State-of-the-Art

To improve the power efficiency of rectifiers operating with low input power, there is basically 2 options. First the power losses need to be lowered in the device throughout specific sizing/design to minimize the RF losses, which is mostly relied on the technology. Alternatively, the device threshold voltage V_{Th} can be reduced.

As shown in (II.8) and (II.10), the reduction in the threshold voltage of the transistor or the diode allows to increase the output voltage of the multiplier without changing the number of stages. Hence, many studies have been conducted to artificially reduce the threshold voltage. To perform the V_{Th} reduction, there are several techniques using either technology solutions, or additional circuitry.

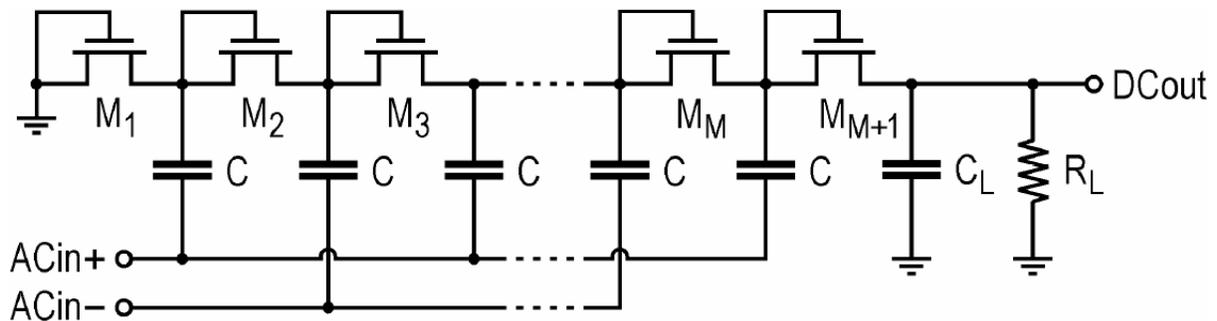


Figure II.9: Schematic of a Dickson n-stage rectifier

The circuit solutions adopted for the implementation of low-power rectifiers are mostly based on the Dickson's topology, which relies on the use of DCMT as charge-pump devices. Such common architecture is shown in Figure II.9, where the DC input has been grounded as required in fully passive harvesting applications [67]-[68]. The performance of the Dickson's topology is substantially affected by the threshold of the rectifying devices, which reduces the AC/DC conversion efficiency and sets a minimum input voltage needed to turn the circuit on. Indeed, the DC output voltage of a Dickson rectifier with pumping devices can be expressed as:

$$V_{OUT} = M \left(\frac{C}{C + C_P} V_{IN} - \frac{I_{OUT}}{f(C + C_P)} - V_{Th} \right) - V_{Th} \quad (\text{II.11})$$

where V_{IN} is the peak-to-peak voltage of the AC input signals, C is the coupling capacitor, C_P is the parasitic capacitance at each transistor node, I_{OUT} is the average current drawn by the output load and f is the operating frequency. According to (II.11), the condition to obtain a positive output voltage is satisfied when:

$$V_{IN} > \left(\frac{C + C_P}{C} \right) \left(\frac{M + 1}{M} \right) V_{Th} + \frac{I_{OUT}}{fC} \quad (\text{II.12})$$

Therefore, even with negligible output currents, a minimum input voltage V_{IN} amplitude must be guaranteed for proper circuit operation, such amplitude increases for larger V_{Th} values. This results in an input power threshold, which is also known as “dead zone” of rectifiers.

This issue is particularly critical when a rectifier is exploited for RF energy harvesting, since the signal levels available at the receiver antenna are typically much smaller than usual MOSFET threshold voltages. Indeed, far-field propagation of radio waves implies that the power density drops quickly when the distance from the radiating source is increased.

3.1 Technology improvement

The problem of rectifiers’ dead zone can be faced by taking advantage of some specific technology options. For instance, Schottky diodes and zero- transistors are exploited as rectifying components in [69] and [70], respectively.

The reference [69] shows that the rectifier built with Schottky diodes can achieve a power efficiency of 14.5% to provide an output power of 1.4 μW (1.5 V at 0.95 μA) with a sensitivity of -20 dBm operating in 869 MHz As reference [70] shows a 10-stage voltage multiplier using zero-threshold voltage transistors, this circuit reaches a 33.69% of power efficiency to provide an output power of 13.64 μW (0.974 V at 14 μA) operating at 900 MHz. The sensitivity estimated is -13.9 dBm for these conditions. Despite the improvement either in sensitivity or in efficiency, the use of non-standard technology options results in an increased production cost.

On the other hand, low-voltage transistors are commonly available in standard CMOS processes and can be used for the same purpose as presented in [71]. This reference exhibit a 16-stage voltage multiplier using low V_{Th} PMOS transistors, which needs an input power of

-12 dBm to provide an output power of 6.91 μ W with an 1 M Ω load operating at 450 MHz, in terms of power efficiency this result represents 10.94%. Though achieving a comparatively lower performance in terms of dead zone compensation, the production cost will be significantly decreased.

3.2 Circuit Techniques

3.2.1 Threshold voltage compensation

As an alternative to technology-based approaches, smart circuit solutions can be exploited in order to compensate the rectifying devices' threshold voltage. Such compensation can be ideally performed by supplying a static bias offset between the gate and drain transistors terminals, as represented in Figure II.10. This arrangement has the same effect of a V_{Th} net reduction, since the turn on condition $V_{GS} \geq V_{Th}$ is reached for lower input voltages and thus yielding an improvement of the rectifier performance. In other words, the bias voltage V_{Bias} added to the circuit provides an offset voltage to the forward drop voltage of the device, which changes to:

$$V_{Drop} = V_{Th} - V_{Bias} \quad (II.13)$$

And the equation (II.8) may now be expressed as:

$$V_{OUT} = 2N(\hat{V}_{IN} - V_{Th} + V_{Bias}) \quad (II.14)$$

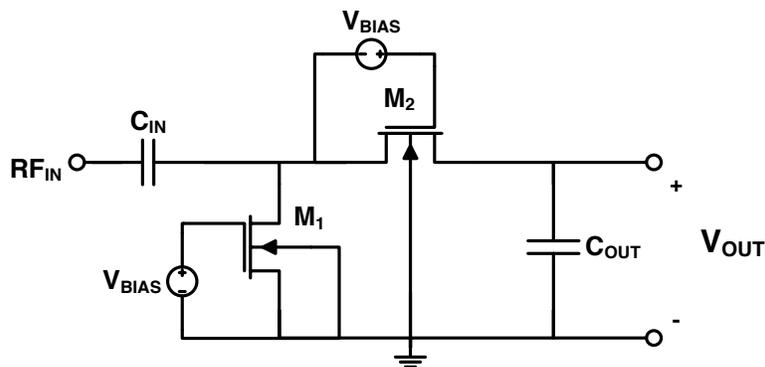


Figure II.10: Voltage multiplier with the V_{Th} compensation.

Several compensation techniques have been proposed according to this general approach. A threshold compensator is suggested in [72], Figure II.11, relying on a proper bias voltage generator and distributor.

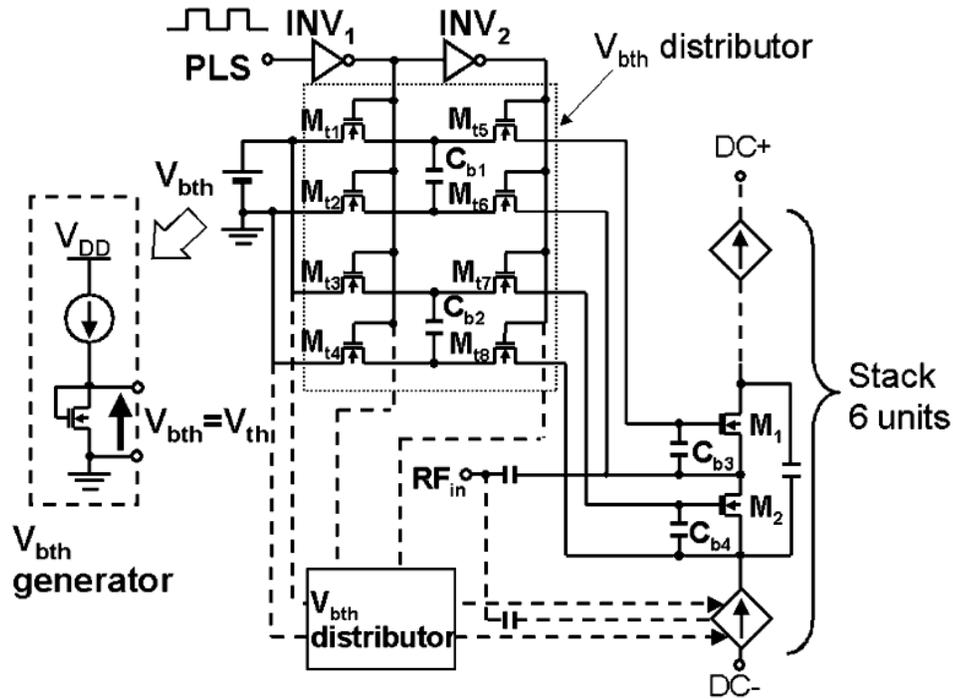


Figure II.11: Compensation V_{Th} through V_{Bias} generator.

This V_{Th} compensator architecture mounted in a 6-stage voltage multiplier shows be capable of operating at 950 MHz with a sensitivity of -14 dBm to provide an output voltage supply of 1.5 V at 0.4 μ A current (600 nW). Despite the improvement in sensitivity, this compensator is not completely passive since the generator requires an individually power supply to provide the V_{Bth} voltage.

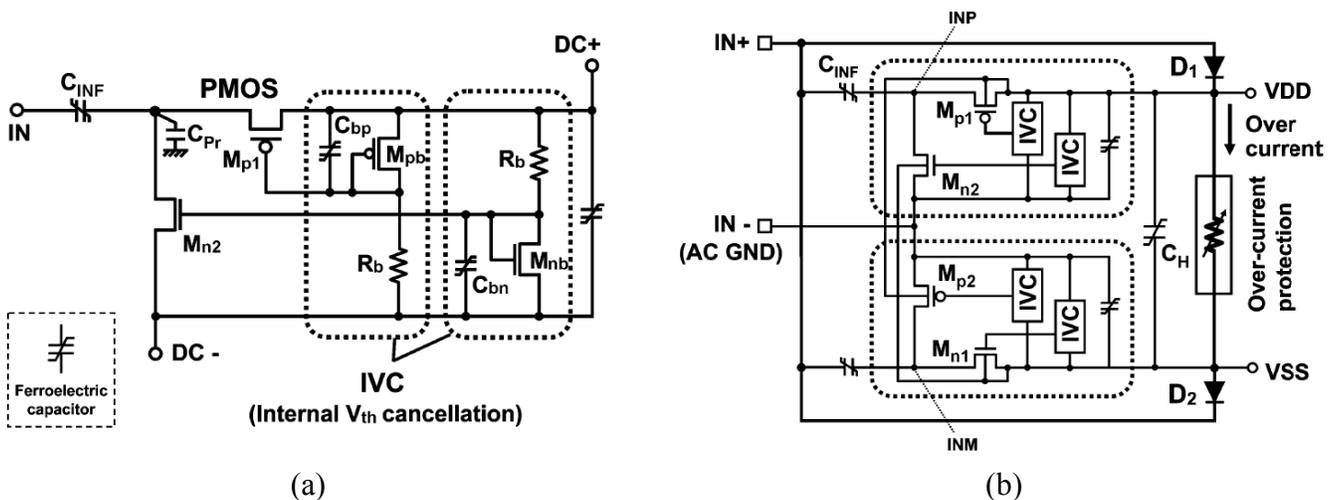


Figure II.12: (a) one cell of the voltage multiplier, (b) entire full-wave rectifier with mirror-stacked architecture.

A passive mirror-stacked threshold compensation is proposed in [73], Figure II.12. In this reference the entire full wave rectifier using a compensation V_{Th} by a mirror-stacked architecture exhibits a power efficiency of 36.6% requiring an input power of -6 dBm. They also compare this structure with a previous work [72], which presents an efficiency of 11% at the same conditions. However, this new circuit presumes the use of large capacitance and resistance values, potentially resulting in a large silicon die area occupation for n-stage implementations.

An auxiliary rectification chain is exploited in [74], Figure II.13, to generate the compensating gate bias offset voltages. Though proposed for charge pump applications, this arrangement can effectively reduce the dead zone of a RF harvester. However, it should be considered that the auxiliary chain and associated coupling capacitors increase significantly the silicon die area to fabricate this circuit. Moreover, the auxiliary chain could also increase the power dissipation, reducing the overall power conversion efficiency.

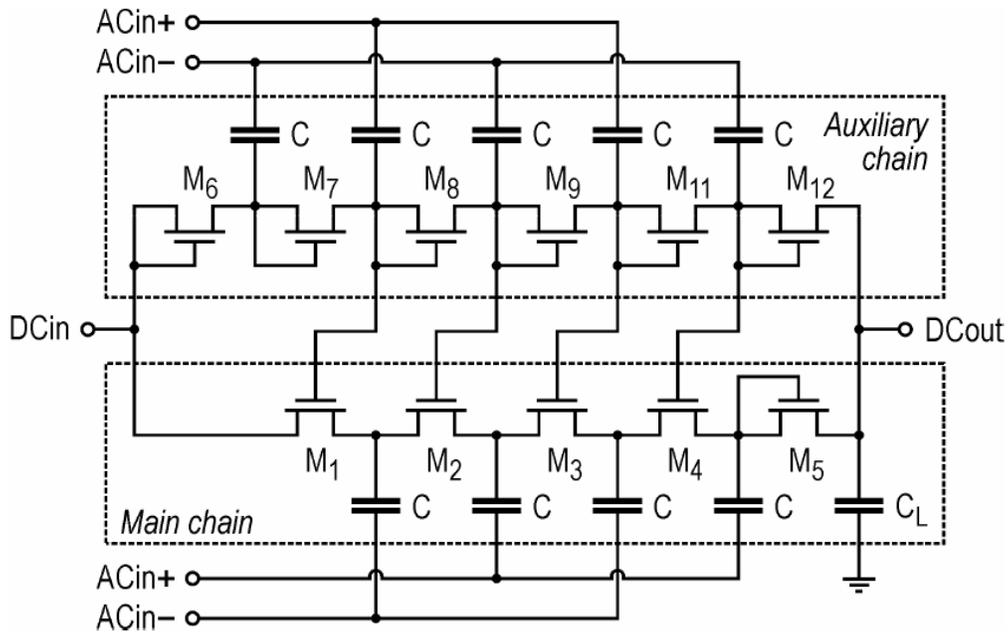


Figure II.13: N-stage voltage pumping circuit.

The rectifier proposed in [75], Figure II.14, consists of two separate rectifiers operating together in the same architecture, the first one act only as a compensation voltage generator for the standard CMOS transistors in the main rectifier.

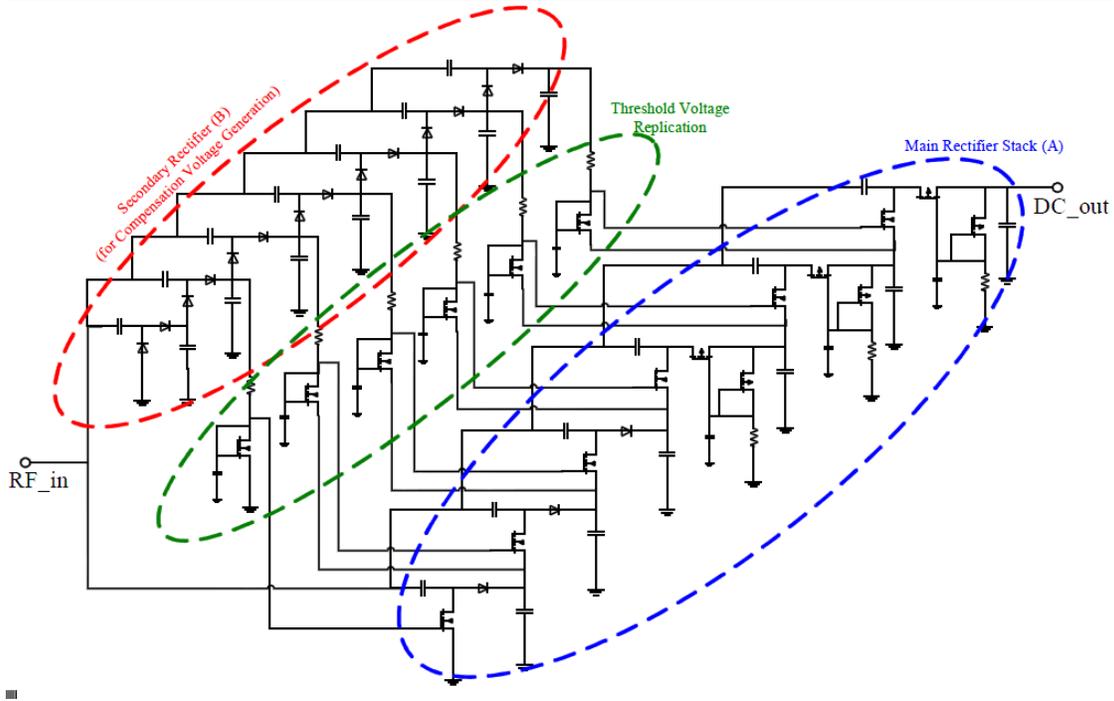


Figure II.14: a) Compensation using a second rectifier diagram, b) Compensation using a second rectifier circuit.

The second rectifier is an n-stage rectifier implemented with Schottky diodes, which with a threshold voltage replication, injects a voltage bias to main rectifier. The structure reported in this reference power supplies a 300 k Ω load with 1.5 V, requiring an input power of -11.3 dBm, representing an estimate power conversion efficiency of 7%. This performance is compared to a conventional Schottky diode multiplier measured under the same conditions, which requires an input power of about -8.6 dBm, 3.6% of efficiency.

Even if this structure provides a threshold cancellation, there is always the power consumption degradation due to the insertion of the secondary rectifier and the use of Schottky diodes, not available in standard CMOS technology.

3.2.2 Floating-gate technique

The threshold voltage can be decreased by implementing transistors with dual-poly gate technology, where one poly-gate is floating, such as the transistors found in a memory EEPROM technology. Therefore, pre-biasing the floating gate, the transistors voltage may be parameterized.

The papers [76]-[77] use this type of transistor to improve the performance of its rectifier, but as it says, most standard CMOS technologies do not include dual-poly gate. Furthermore, additional steps in the manufacturing process is required for programming the floating gate.

Pseudo floating-gate transistors are used in [78], Figure II.15b, which are able to store a pre-charged compensation voltage. It is called pseudo floating-gate, because it is not a structure using dual-poly gate technology, but common transistors connected as a capacitor and then implemented between the gate and source as shown in Figure II.15a.

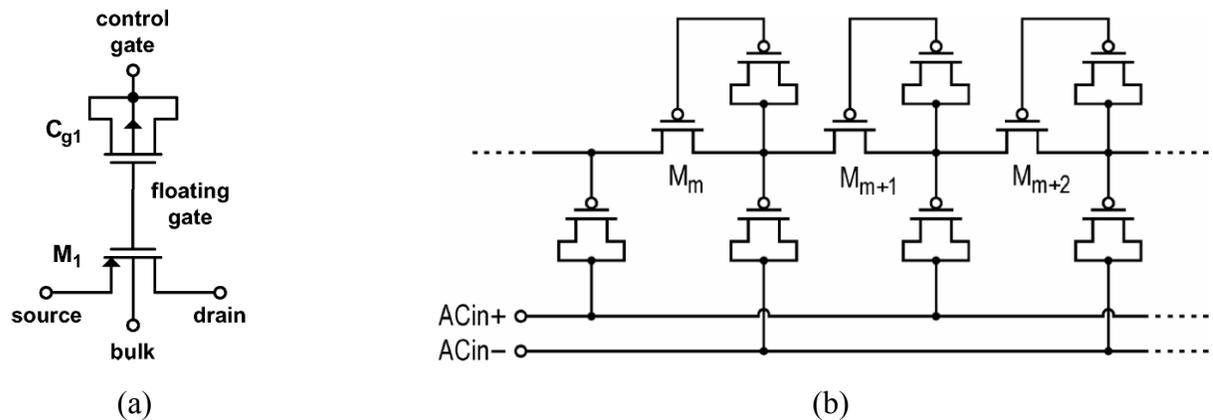


Figure II.15: a) Floating-gate transistor implementation, b) PMOS floating-gate rectifier.

The RF/DC rectifier circuits presented in [78] are 16 and 36-stage voltage multiplier using this pseudo floating-gate technique. They exhibit good sensitivity operating in an unloaded mode, -19 dBm and -26 dBm, respectively, to provide an output voltage of 1 V. And when charged with a 330 k Ω load, the 32-stage rectifier deliver 1 V requiring an input power of about -14 dBm, which in terms of power efficiency represents 7.6%. Despite the good improvement in the range operation, this technique needs to be initially programmed, making the system unsuitable for battery-less platforms.

3.2.3 Self-compensation structure

Another smart technique is to perform rectifiers taking advantage of a self-threshold voltage cancellation scheme, which the V_{Th} of MOSFETs is cancelled by applying a gate bias voltage generated by the rectifier itself. Very simple circuit configuration and no power dissipation feature

of the schematic, which improves the power conversion efficiency, especially in small RF input power conditions, as presented in [79].

Figure II.16 illustrates the reference [79] circuit, where the diode connected MOS transistor, M_2 , generates the bias voltage, V_b , and the capacitor C_b ensure the V_{Bias} voltage between V_{Drain} and V_{Gate} terminals of the diode connected PMOS transistor M_1 , decreasing the effective V_{Th} as demonstrated in (II.13).

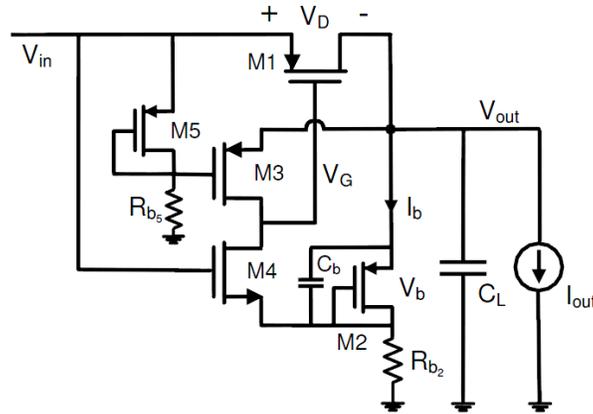


Figure II.16: PMOS rectifier with internal V_{Th} cancellation.

Despite the improvement in power conversion efficiency of about 80%, they do not show the applicability of this circuit for UHF operation.

A self-compensation structure is also proposed in [80]. This circuit is based on the conventional voltage multiplier described in II.2.1.3 using DCTM as diodes, except that the gate electrodes of NMOS transistor and PMOS transistor are connected to the output and ground terminals, respectively, Figure II.17. This connection boosts gate-source voltages of the DCTMs as much as the output DC voltage.

The major advantage of this system is its simplicity. The voltage threshold could be compensated without adding extra circuitry. The maximum efficiency of this structure is about 29% requiring an input power of -9.9 dBm to provide an output voltage of approximately 0.5~0.6 V, which is not enough to supply some kind of applications. After this optimum point, to obtain higher voltages, the power consumption increases dramatically, reducing the efficiency. As it is a single stage rectifier, one solution to increase the V_{OUT} , as described in II.2.1.4, could be cascading several cells in order to build an n-stage configuration.

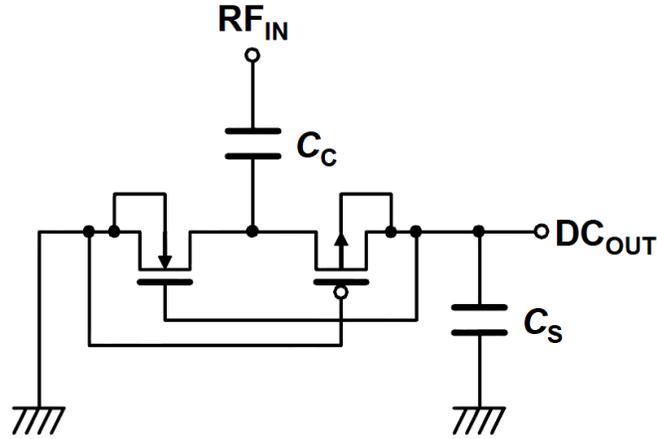


Figure II.17: Self V_{th} cancellation rectifier circuit.

3.2.4 Cross-coupled bridge rectifier

In order to decrease the rectifier “dead zone” and simultaneously develop a circuit capable of operate with small leakage current condition, a differential rectifier structure using the cross-coupled technique has been studied in [81] and is shown in Figure II.18.

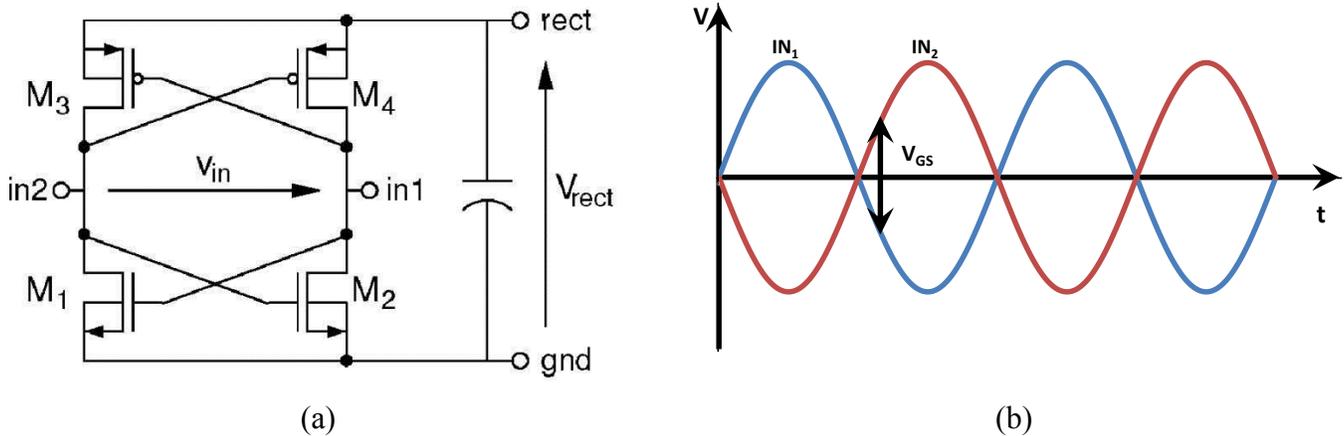


Figure II.18: (a) Cross-coupled bridge rectifier, (b) Waveform of the differential bias voltage.

It consist of differential CMOS with a bridge structure, described in II.2.2.1, except that the transistors used are no more connected as DCMTs, but as switches. In this differential structure, the transistors’ gate are biased by a differential signal. From Figure II.18, the RF signal of IN_1 and IN_2 nodes are out of phase and the waveform of this signals are represented in Figure II.18 (b).

As it can be depicted from Figure II.18 (b), when the transistors are turned on, the V_G and V_S voltages are out of phase, halving the threshold voltage and so decreasing the rectifier dead zone. Thus, the provided output voltage of this differential circuit can now be expressed as:

$$V_{OUT} = \hat{V}_{IN} - V_{Th} \quad (\text{II.15})$$

However, the drawback of this configuration is that, at the steady-state, the output voltage V_{OUT} achieves its maximum voltage for a given input power, and when the amplitude RF signal starts to decrease, the series transistor will conduct backwards, increasing the losses. Despite this problem, the overall power efficiency tends to be improved when compared with other architectures, as shown in [82], which exhibits an power efficiency of 75% at 953 MHz, requiring an input power of approximately -25 dBm. However, as (II.15) predicts, the obtained output voltage is lower than the input voltage amplitude. Hence, they are mostly brought into play in circuits, where higher voltages are easily achieved [83].

4 Design Methodology

The aim of this thesis is to perform a WPR capable of properly operate in low power conditions to replace the battery function through harvesting the available EM energy at the environment and power supplying an application. To perform this task, the rectifier is one of the most important key parts of the system.

Designing a custom rectifier depends on the load which is expected to be driven. Indeed, the current consumption at the same voltage condition could change dramatically with the applications. For this reason most front-end systems have a power management unit (PMU) to control the output current maintaining the output voltage constant.

We are interested in developing an architecture capable of power supplying typical low-power applications, such as WSNs, while operating over long distances, at least a few meters. These typical low-power applications could operate under a power supply of 1 V for a few μA current, which requires a high efficiency rectifier in order to obtain high sensitivity operating system.

The strategy adopted is to design a rectifier able to provide an output current of 3 μA and an output voltage of 1.2 V, supplying an overall power of 3.6 μW to the charge. A higher output voltage is chosen predicting the addition of some PMU circuitry to regulate an output voltage fixed at 1 V. The goal is to obtain a power conversion efficiency as high as possible to minimize the input power required, and so optimizing the system operating distance for a constant power supply. TABLE II.1 summarizes the design specifications adopted to perform the rectifier.

TABLE II.1 Design specifications for the rectifier block.

Specifications	
Sensitivity [dBm]	Better than -15
Output voltage [V]	1.2
Output current [μA]	3
Output power [μW]	3.6

4.1 Transistor's Choice

Considering the large-scale production feasibility, in many power harvesting applications, such as WSNs and RFID, the cost prevails over the performance. As discussed in II.2.3, Schottky diodes are considered as an attractive candidate to perform the charge transfer task due to their low forward voltage drop and fast switching speed. However, Schottky diodes are not supported in all CMOS technologies which restricts their use in low-cost applications.

The technology chosen for the rectifiers implementation is a standard 130nm CMOS from ST Microelectronics in a tradeoff between cost and performances as discussed in Chapter I. In this technology, there are several types of transistors available as standard option intended for different types of applications. They are basically classified according to:

- Operating voltage – ranging from 1.2 to 8 V,
- Threshold voltage – ranging from 300 to 700 mV,
- Turn-off current – ranging from a few pA/ μm to a few $\mu\text{A}/\mu\text{m}$.

As our circuit is operating in low-power condition for supplying a load with 1.2 V, the transistors designated for high voltage applications can be discarded, since they have higher threshold voltages values, which decreases the rectifiers' sensitivity. Normally the threshold voltage and the turn-off current are inversely proportional, which means that transistors optimized for high speed have more leakage and the ones optimized for low leakage are slower. For rectifiers, both parameters are important. On the one hand, high speed transistors have low threshold voltage, decreasing the rectifier dead-zone and so improving the energy conversion. On the other hand, low leakage transistors conserve during more time the converted energy stored at the rectifier output. For the transistor's choice, both parameters are analyzed comparing two different transistors, one high speed and one low leakage, in order to define which one prevails over the other.

Figure II.19 presents the High Speed and Low Leakage I_D - V_{IN} characteristics as a function of time. In the chart, when forward voltage is applied to the diode-connected MOS transistor (from t_0 to t_1), the transistor turn-on and forward current flows to current supply the output load. When input voltage changes to the negative cycle (from t_1 to t_2), only leakage current flows backwards.

The energy losses, represented by the rectifier circuit dead-zones, is mainly caused by the resistive losses at forward bias condition. The power needed to exceed this resistive limitation directly affects the efficiency. Hence, the lower the threshold voltage of the MOS transistor is, the lower the effective on-resistance becomes, increasing the PCE.

However, when the threshold voltage of MOS transistor is too small to the point of becoming negative, reverse leakage current increases significantly, which directly results in increased energy loss since charges flowing in a reverse direction are wasted. As a result, excessive reduction in the threshold voltage cancel the advantage obtained by the reduction in the on-resistance and causes severe reduction in efficiency.

Analyzing Figure II.19, first, it is depicted that the High Speed transistor has a higher current density, which results in a decreased size configuration for the same task. Another improvement is the dead-zone reduction due to lower threshold voltage, which can provide more energy to the load. In other words, the power integration in time results in a reduced power loss for the High Speed transistor.

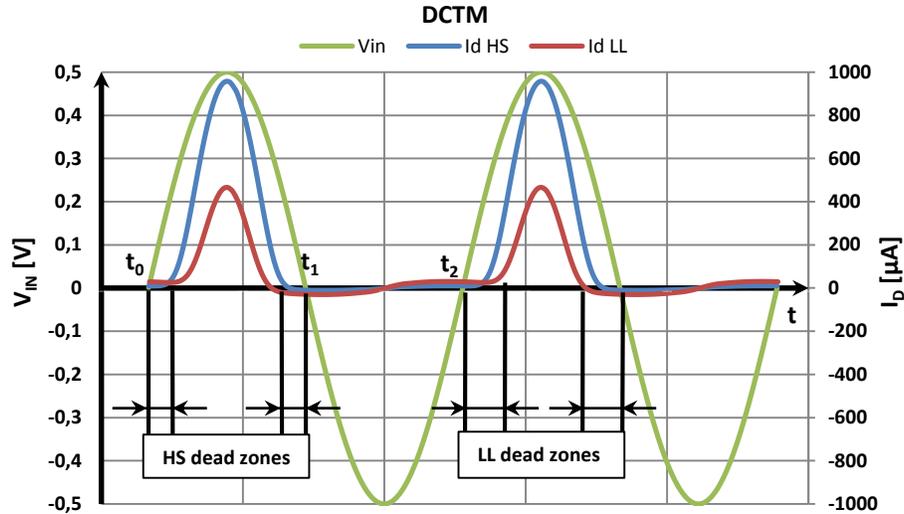


Figure II.19: V_{IN} and I_D for High Speed and Low Leakage using DCTM configuration.

To compare which advantage results in a better power transfer, a single stage voltage multiplier was analyzed considering a fixed input power of $10 \mu\text{W}$ for power supply a load of $400 \text{ k}\Omega$. Figure II.20 shows the output voltage as a function of time, it is noticed that even if the low leakage transistors provides reduced power losses during turn-off cycle, the higher energy conversion achieved by high speed transistors overcomes the leakage losses disadvantage.

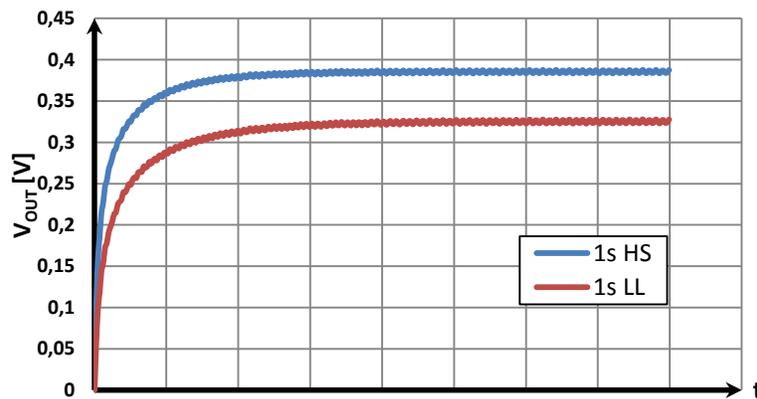


Figure II.20: V_{OUT} as a function of time for 1-stage voltage multiplier.

4.2 Simulation Setup

Before the simulation results analysis, it is important to setup an appropriate simulation method and comparison standard. Sensitivity, input impedance, delivered output voltage and power conversion efficiency (PCE) are the parameters to be considered when analyzing the rectifier circuit. The PCE parameter is one of the most important performance parameter of the rectifier circuit, since it is the parameter which predicts the harvester sensitivity required for proper operation and, thus, optimizing it improves the operating distance of the module. The PCE, η , is defined as:

$$\eta = \frac{P_{OUT}}{P_{IN}} \quad (\text{II.16})$$

where P_{OUT} is the average output power dissipated on the load and P_{IN} is the RF input power of the rectifier block.

First, to characterize only the rectifiers and in order to simplify the circuitry complexity, the resonant circuits and the impedance matching network are not incorporated in the simulation setup. A voltage source or power source is placed in the schematic to supply the rectifiers with the required RF power. At the output node, a passive resistor and a coupled capacitor are employed as shown in Figure II.21. The resistor replaces the load of an application attached to the rectifier, whereas the shunt capacitor filters the non-linearity behavior of the output power provided by the rectifiers and stores a DC power to supply the load.

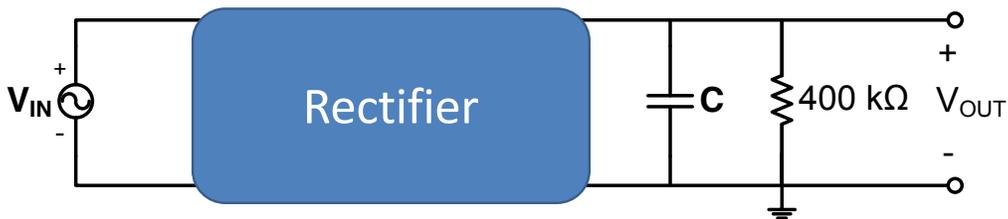


Figure II.21: Simulation setup of the rectifiers.

4.2.1 Different power concepts

Since the input of the rectifier is an AC power source, some issues concerning the definition of power appears and they are not as clear as the simple definition used to estimate the power in DC. Basically, there are four types of power in AC state conditions:

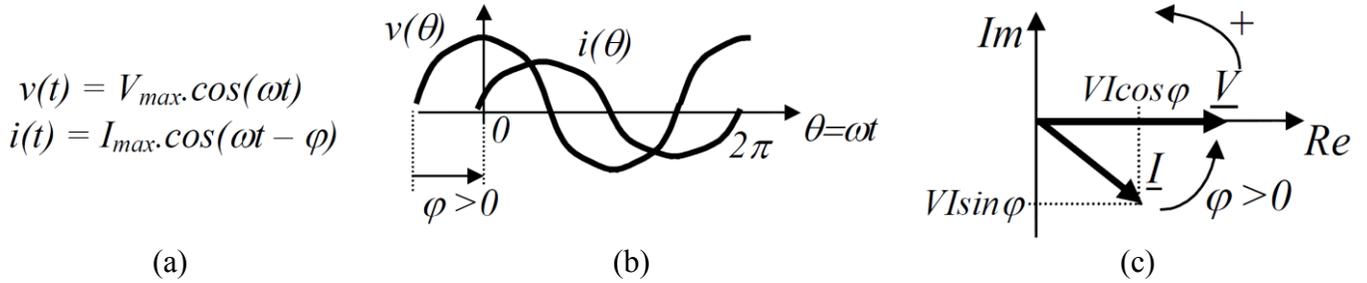


Figure II.22: a) voltage and current formulas, b) voltage and current waveforms as a function of time c) phasor diagram representation in sinusoidal AC system.

a) Instantaneous power

Instantaneous power is the quantity of power moving at single instant in continuous time. It is the value of power p at a given time t , which is equal to the voltage at time t times the current at time t . In general, it is defined as follows:

$$p(t) = v(t) \cdot i(t) \tag{II.17}$$

Considering in a sinusoidal AC state, as represented in Figure II.22, the instantaneous power $p(t)$ can also be defined as:

$$p(t) = V_{max} \cdot \cos(\omega t) \cdot I_{max} \cdot \cos(\omega t - \varphi) \tag{II.18}$$

$$p(t) = \frac{V_{max} \cdot I_{max}}{2} \cdot \cos(\varphi) + \frac{V_{max} \cdot I_{max}}{2} \cdot \cos(2\omega t - \varphi) \tag{II.19}$$

$$p(t) = V_{rms} \cdot I_{rms} \cdot \cos(\varphi) + V_{rms} \cdot I_{rms} \cdot \cos(2\omega t - \varphi) \tag{II.20}$$

where rms^l signals can be defined as:

$$S_{rms} = \sqrt{\frac{1}{T} \int_T s^2(t) dt} = \frac{S_{max}}{\sqrt{2}} \quad (\text{II.21})$$

¹Root Mean Square, also known as effective value

b) Average power

Average power, also known as real, true and active power, is the average of the instantaneous power over one time period. This power can be seen as a dissipation power due to active elements (resistances and mechanical elements), i.e. the elements that actually consume and dissipate energy. The active power is expressed as:

$$P_{avg} = \frac{1}{T} \int_T v(t) \cdot i(t) \cdot dt \quad [W] \quad (\text{II.22})$$

c) Reactive power

Reactive power flow is needed in an alternating-current transmission system to support the transfer of real power over the network. In alternating current circuits, energy is stored temporarily in inductive and capacitive elements, which can result in the periodic reversal of the direction of energy flow. After being averaged over a complete AC waveform, the amount of power which is temporarily stored in such devices in the form of magnetic or electric fields and then returned to source is known as *reactive power* and, considering sinusoidal signals, can be expressed as:

$$Q = V_{rms} \cdot I_{rms} \cdot \sin(\varphi) \quad [var] \quad (\text{II.23})$$

The reactive power is not considered as a power consumption or dissipation, since it returns to the source, but it is required for circuit proper operation, which increases the available power needed. It is also interpreted as the difference between the source and circuit imaginary part of the impedance. If the circuit has a capacitive reactance, the source must present an inductive reactance in order to cancel the reactive power and so optimize the power required.

d) Effective power

Effective power or apparent power is the power representation combining the average and reactive power. It consists in take into account the active power consumption of a device, but also comprising the “parasitic” reactive power and so analyzing the entire power required for a circuit proper operation.

The effective power is important because all practical electrical applications will contain a combination of resistive, capacitive and/or inductive elements. Therefore, any practical AC circuit or system has a combination of both average and reactive power, which vary the phase angle between voltage and current. The desired outcome is to maximize the active power while limiting the reactive power. Taking both into account, the end result considering average and reactive power is called effective power, which is defined as:

$$S = V_{rms} \cdot I_{rms} \quad [VA] \tag{II.24}$$

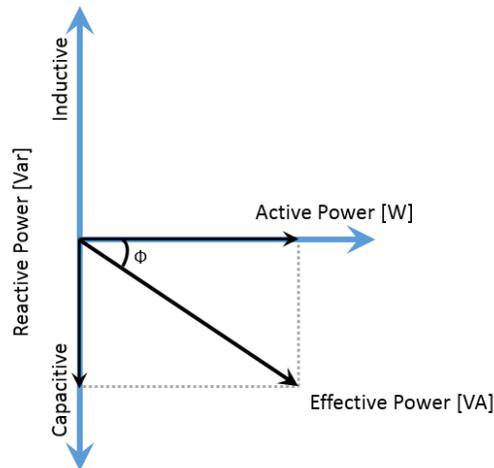


Figure II.23: Phasor diagram for the different concepts of power.

Analyzing the phasor diagram represented in Figure II.23, it is depicted that both power elements, active and reactive, affect the apparent power value. Indeed, the vector summation of the average and reactive power results in the effective power, which depends directly of the active and reactive power magnitudes and the phase shift between the voltage and the current. With this analysis, another expression can be deduced from Figure II.23 to relate all these three power parameters together, which is:

$$S^2 = P^2 + Q^2 \quad (\text{II.25})$$

After regarding in more details the power concepts which can be used to analyze the rectifier behavior, one question comes up: which power use to study it, average or effective power? On the one hand, the average power presents the rectifier power consumption used to perform the energy conversion task, neglecting the presence of reactive phenomenon and the power required by them. On the other hand, the effective power takes into account both of powers and, thus, representing the real power required under the circuit conditions.

Considering the system analyses, the best power to study its behavior is the effective power, since it is the power which must be generated to power supply the system. However, analyzing only the rectifier this power considers all the parasitic devices present in the circuit, which will be compensated after adding an antenna with an appropriate impedance or a matching network. Therefore, when just the rectifier circuit is studied, the best power analysis is performed with the average power.

Furthermore, taking into account the reactive power over the parasitic devices could degrade the power conversion task when optimizing the rectifier, since modifying the transistors size W/L changes the energy conversion, but also generates a different value on the reactive parasitic elements. In low-power conditions, the amount of reactive power used to be greater than average power, due to low resistance and high capacitance characteristics of the rectifier input impedance. Therefore, the optimum size of the transistors would be defined to decrease the reactive power and, in some cases, sacrificing the energy conversion to improve the overall effective power.

4.2.2 Simulator engines

To perform high frequency analysis, it is important to choose an appropriate simulation environment to characterize the RF circuits. The two most popular simulation and design softwares are Cadence framework and Advanced Design Systems (ADS), developed by Agilent Technologies. Facilities access leads us to Cadence and Spectre RF platform. Various simulations can address the analysis of RF rectifiers, we can classify them into 2 types:

- Time domain – Transient simulation.

- Frequency domain – Scattering Parameters (SP), Periodic Steady State (PSS), Harmonic Balance (HB), Large Signal Scattering Parameters (LSSP).

Both domains are important to characterize the rectifier. On the one hand, the time domain simulation shows the energy transfer evolution, which identifies the circuit operation at transient and steady-state conditions. On the other hand, a frequency domain simulation is necessary to quickly describe the circuit specifications, such as impedance, multitone response, non-linearity behavior, under steady-state condition.

a) Transient analysis

Time simulation is a SPICE type analysis, which consists of solving a set of integrodifference equations expressing the time-dependent current and voltage of an electronic circuit using numeric integration to find an approximation to the analytical solution at discrete time points

The transient analysis in SPICE relies on the availability of 3 different integration methods to evaluate the time behavior, which are summarized in TABLE II.2. Depending on the expected waveform, one may have an advantage over another according to two main characteristics, accuracy and stability.

TABLE II.2 The different integration methods available for transient simulation

Method	Equation	Description
Trapezoidal	$x_{n+1} = x_n + h \cdot \frac{(\dot{x}_{n+1} + \dot{x}_n)}{2}$	Better accuracy than stability
Backward Euler	$x_{n+1} = x_n + h \cdot \dot{x}_{n+1}$	Average accuracy and stability
Gear-2	$x_{n+1} = \frac{4}{3}x_n - \frac{1}{3}x_{n-1} + \frac{2}{3}h \cdot \dot{x}_{n+1}$	Better stability than accuracy

Temporal analysis is performed entirely in the time domain, which means this type of analysis is not able to take account easily the frequency behavior in distributed elements, such as microstrip lines or components described through S-parameters. These elements are often represented by frequency independent simplifications as localized passive elements, transmission lines without dispersion, short circuits or open circuits. These approximations are generally acceptable and

realistic at low frequencies, however, this type of simulation becomes less accurate when the frequency increases.

b) S Parameters

The S-parameter simulation is a small-signal simulation type most often used to characterize RF passive components or to determine the small signal characteristics of a device under bias and temperature specific conditions. Non-linear components are linearized around the operating point. The resulting linear circuit is analyzed as a multi-port network. Each port is excited sequentially by small signals and the response is measured and converted into S-parameters

Concerning the characterization of a circuit which is composed by linear elements or nonlinear elements working in small signals conditions so that they can be considered as linear, it is possible to define a network or a system only through the parameters measured in the respective in/out ports, without worrying about the exact content inside it. Once these parameters are determined, it is possible to predict the exact behavior of the system applying any external stimuli, even without knowing its real composition.

The S-parameters can be better understood analyzing a behavioral representation of a 2-port system shown in Figure II.24.

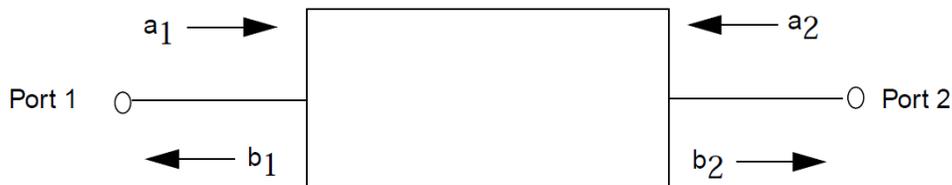


Figure II.24: Representation of a two-port system.

The S-parameter matrix for the 2-port network is probably the most commonly used and serves as the basic building block for generating the higher order matrices for larger networks. In this case the relationship between the reflected, incident power waves and the S-parameter matrix is given by:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \cdot \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \quad (\text{II.26})$$

where:

- a1 is the circuit input signal at port 1 node,
- a2 is the circuit input signal at port 2 node,
- b1 is the reflected signal at port 1 node,
- b2 is the reflected signal at port 2 node.

Each 2-port S-parameter has the following generic descriptions:

- S11 is the input port voltage reflection coefficient,
- S22 is the output voltage reflection coefficient,
- S12 is the reverse voltage gain,
- S21 is the forward voltage gain.

For a generic multi-port network, each of the ports is allocated an integer n ranging from 1 to N, where N is the total number of ports. In this generic case the equation (II.26) can be expressed as:

$$\begin{pmatrix} b_1 \\ \vdots \\ b_n \end{pmatrix} = \begin{pmatrix} S_{11} & \cdots & S_{1n} \\ \vdots & \ddots & \vdots \\ S_{n1} & \cdots & S_{nn} \end{pmatrix} \cdot \begin{pmatrix} a_1 \\ \vdots \\ a_n \end{pmatrix} \quad (\text{II.27})$$

c) Periodic Steady-State

The PSS analysis computes the periodic steady-state response of a circuit at a specified fundamental frequency, with a simulation time independent of the time-constants of the circuit. The PSS analysis also determines the circuit's periodic operating point which is the required starting point for the periodic time-varying small-signal analyses, such as PAC, PSP, PXF, and Pnoise.

Spectre simulation in the Cadence framework uses a technique called the shooting method to implement PSS analysis. This method is an iterative, time-domain method that finds an initial condition that directly results in a steady-state. It starts with a guess of the initial condition and

tries to converge to the real value. To facilitate the convergence, a parameter called $tstab$ can be adjust and so improving simulation time.

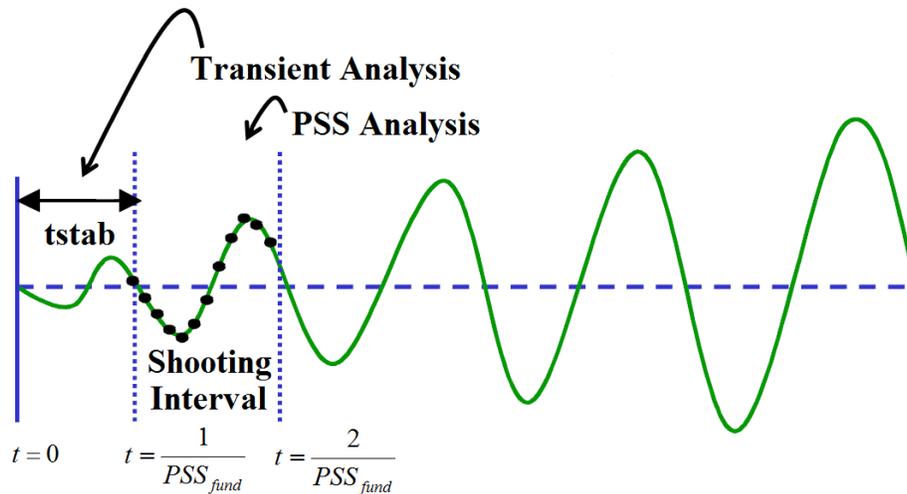


Figure II.25: Operating principle of PSS analysis.

The shooting method requires few iterations if the final state of the circuit after one period is a near-linear function of the initial state. This is usually true even for circuits that have strongly nonlinear reactions to large stimuli. Typically, shooting methods need about five iterations on most circuits, and they easily simulate the nonlinear circuit behavior within the shooting interval. This is the strength of shooting methods over other steady-state methods such as harmonic balance. Moreover, Cadence's Fourier integral method approaches the accuracy of harmonic balance simulators for near-linear circuits, and far exceeds it for strongly nonlinear circuits.

d) Harmonic Balance

Harmonic balance is a highly accurate frequency-domain analysis technique to obtain the steady state solution of nonlinear circuits and systems. It is usually the method of choice for simulating analog RF and microwave problems that are most naturally handled in the frequency domain. Once the steady state solution is calculated, the harmonic balance simulator can be used to characterize the circuit.

CHAPTER II DESIGN AND CHARACTERIZATION OF RECTIFIERS FOR LOW-POWER APPLICATIONS

The harmonic balance method assumes that the input stimulus consists of a few steady-state sinusoids. Therefore the solution is a sum of steady state sinusoids that includes the input frequencies in addition to any significant harmonics or mixing terms.

The objective is to compute the steady state solution of a nonlinear circuit. In the simulator, the circuit is represented as a system of N nonlinear ordinary differential equations, where N represents the size of the circuit. The method is based on the assumption that any solution can be expressed as a linear combination of sinusoidal which satisfies Kirchoff's laws. In other words, the sources and the solution waveforms are approximated by truncated Fourier series. Therefore, a successful simulation will yield the Fourier coefficients of the solution waveforms.

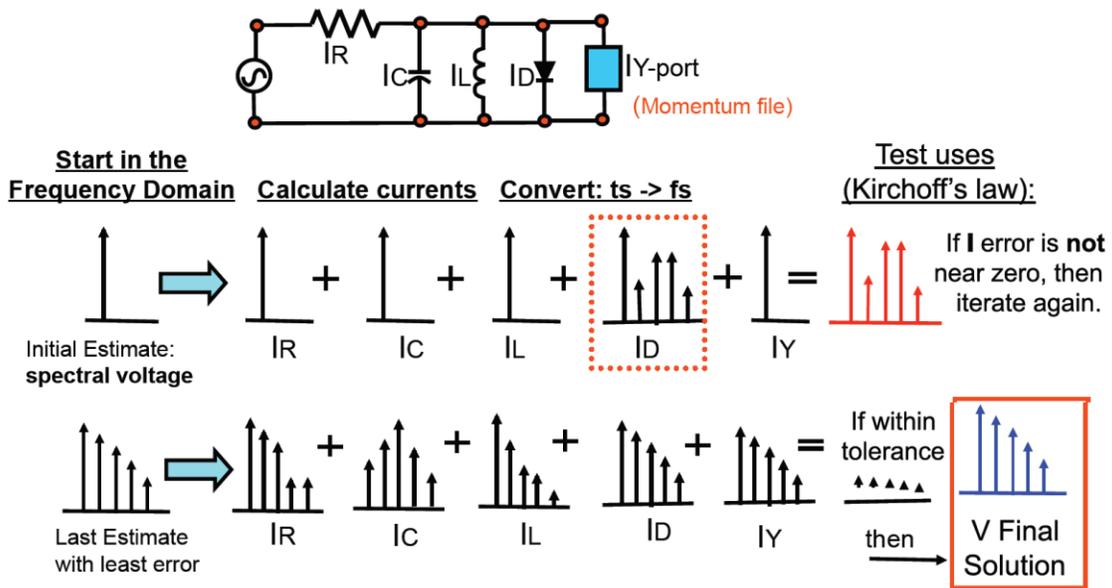


Figure II.26: Operating principle of HB analysis.

Basically the non-linear devices such as transistors and diodes are sampled in the time domain and their response is transformed to the time domain using an FFT. According to Kirchoff's laws, the sum of all the currents leaving a node is zero. It is very unlikely that this condition is achieved from the first iteration. Thus, an error function which is the sum of all currents of each starting node is thus created. This error function is used to calculate the adjustments to be performed in the voltage amplitudes and phases at the nodes, in order to minimize the error function. The algorithm stops when the error becomes lower than the set tolerance. The simulation process flow is summarized in the diagram presented in Figure II.27.

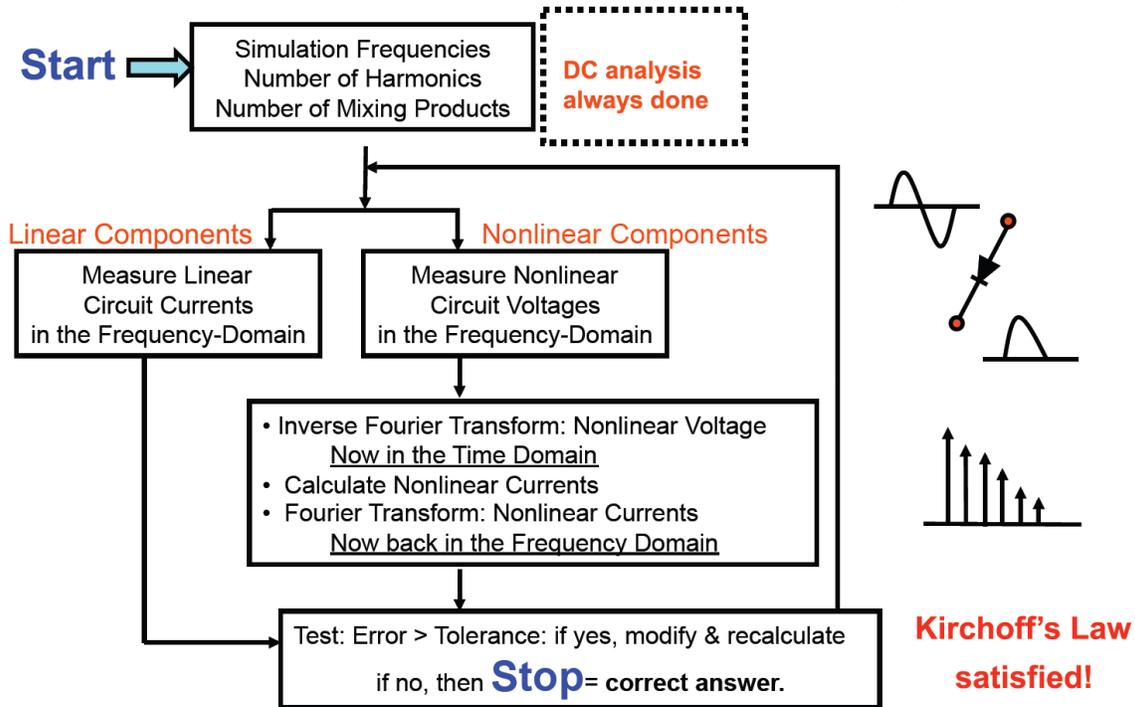


Figure II.27: HB analysis process flow.

e) Large Signal S Parameter

The LSSP Simulation is an engine from ADS to compute S-parameters for nonlinear circuits and it is based on the harmonic balance simulation, thus, it uses harmonic balance techniques to perform the circuit analysis.

Unlike small-signal S-parameters, which are based on a small-signal simulation of a linearized circuit, large-signal S-parameters are based on a harmonic balance simulation of the full nonlinear circuit. Since harmonic balance is a large-signal simulation technique, its solution includes nonlinear effects such as compression. This means that the large-signal S-parameters can change as power levels are varied. For this reason, large-signal S-parameters are also called power-dependent S-parameters. Like small-signal S-parameters, large-signal S-parameters are defined as the ratio of reflected and incident waves:

$$S_{ij} = \frac{B_i}{A_j} \tag{II.28}$$

The incident and reflected waves are defined, respectively, as:

$$A_j = \frac{V_j + Z_{0j} \cdot I_j}{2\sqrt{R_{0j}}} \quad (\text{II.29})$$

$$B_i = \frac{V_i + Z_{0i} \cdot I_i}{2\sqrt{R_{0i}}} \quad (\text{II.30})$$

where:

- V_i and V_j are the Fourier coefficients, at the fundamental frequency, of the voltages at ports i and j ,
- I_i and I_j are the Fourier coefficients, at the fundamental frequency, of the currents at ports i and j ,
- Z_{0i} and Z_{0j} are the reference impedances at ports i and j ,
- R_{0i} and R_{0j} are the real parts of Z_{0i} and Z_{0j} .

This definition is a generalization of the small-signal S-parameter definition in that V and I are Fourier coefficients rather than phasors. For a linear circuit, this definition simplifies to the small-signal definition.

The simulator performs the following operations to calculate the large-signal S-parameters for a two-port:

- Terminates port 2 with the complex conjugate of its reference impedance. Then applies a signal with the user-specified power level P_1 at port 1, using a source whose impedance equals the complex conjugate of that port's reference impedance. Using harmonic balance, calculates the currents and voltages at ports 1 and 2, thus, founding S_{11} and S_{21} .
- Terminates port 1 with the complex conjugate of its reference impedance. Then applies a signal of power $P_2 = |S_{21}|^2 \cdot P_1$ at port 2 using a source whose impedance equals the complex conjugate of the reference impedance of port 2. Using harmonic balance, calculates the currents and voltages at ports 1 and 2, thus, founding S_{12} and S_{22} .

Comparing with the S-parameters simulation, LSSP can be performed on nonlinear circuits and thus includes nonlinear effects. Therefore, it is preferred when simulating non-linear circuits, where the behavior is highly dependent on power levels, as the case of rectifiers.

Since the rectifier circuit has a nonlinear behavior, with the exception of SP simulation, all the others can be performed to analyze the rectifiers. The simulator choice is predicted by behavioral analysis of the circuits. The most accurate simulation is the transient for voltage/current analysis, as it shows the rectifiers time behavior. It also identifies the circuit stabilization, which is important for proper operation in energy conversion. However, the steady-state of this kind of circuit is much greater than the input signal period, which requires higher simulation steps and so long simulation time.

It is advised to perform at least once the transient simulation to observe the circuit stabilization, after it is preferred to continue the analysis and modifications with PSS, LSSP or HB, since they are generally faster and must be performed to analyze the frequency dependent characteristics. Normally when studying the rectifiers PCE, sensitivity and delivered output voltage performed with the different simulators, the results are very close from one simulator to another, then, they can be considered reliable.

4.3 Topology's Choice

For an operating system working at long distance, a small amount of power will be available to be converted by the wireless receiver module. This is the reason why the design of efficient RF/DC converters with low sensitivity is of major importance. However, considering the entire frond-end, it should be noted that the power required at rectifier input is not the only issue to be optimized in a far-field operating range, but also the input voltage level necessary to appropriately power supply the load. The peak voltage available at the input, under perfect power matching condition, is given by [81]:

$$V_{IN} = \sqrt{\frac{P_{AV}}{R_A} \frac{1}{\omega C}} \quad (\text{II.31})$$

where P_{AV} is the available power at the antenna terminals, R_A is the antenna equivalent resistance, ω is the resonance frequency of the antenna impedance and C is the chip equivalent input capacitance.

To enhance the input voltage seen by the chip, R_A has to be minimized; however, the minimum antenna impedance is dictated by geometrical constraints and maximum efficiency. So, at a long distance from the source radiating RF power, where the incident power is small, a small input voltage is received at the input of the circuit, which impairs the proper operation of the rectifier. Thus, to ensure a long range of operation, a small turn-on voltage is as important as a small power-up threshold.

Considering all rectifier topologies available, described in the sessions II.2.1 and II.2.2, the most suited for WE/PT operating at long distances are the ones based on voltage multiplier architecture. Although the architectures containing a reduced amount of devices can obtain higher PCE values, they are not able to deliver higher output voltage levels without requiring more input power. So, in low-power conditions, the architectures capable of regulating the tradeoff between the required input power and input voltages are preferred.

4.4 Traditional Voltage Multiplier

In order to study the rectifiers' impact in low-power conditions and to provide a reference circuit for further comparisons, a traditional voltage multiplier is first analyzed. The scheme of a traditional half-wave rectifier using DCMT devices is illustrated in Figure II.28. To describe its operating principle, a single stage rectifier is here analyzed.

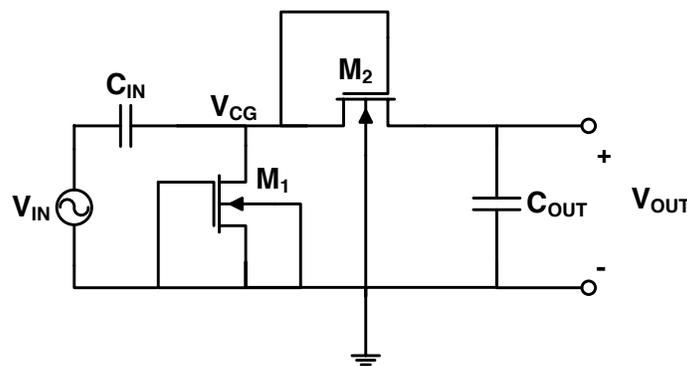


Figure II.28: One-stage traditional voltage multiplier architecture.

During the negative half cycle of the RF signal, when $V_{CG} < V_{DrainM1} - V_{Th}$, the transistor M_1 turns on while transistor M_2 turns off as $V_{CG} < V_{OUT}$ and the charge starts to be transferred to

capacitor C_{IN} . The transistor M_1 charges C_{IN} until the V_{CG} average is equal to $\hat{V}_{IN} + V_{DrainM1} - V_{Th}$.

When the input changes to the positive half cycle the transistor M_1 turns off while transistor M_2 turns on and the charge is transferred from capacitor C_{IN} to capacitor C_{OUT} . The capacitor C_{IN} is the coupling capacitor, which is responsible for the transfer of electric charge. At the end of the cycle, the energy is stored in C_{OUT} , storage capacitor. The final available output voltage V_{OUT} is expressed as described by equation (II.7).

The maximum voltage that can be achieved in a single stage traditional voltage multiplier is twice the RF amplitude voltage minus twice the threshold voltage of the diode-connected MOS. To increase the rectified voltage, several cells of the basic multiplier can be cascaded as described in II.2.1.4, implementing CMOS transistors to perform the energy conversion task as shown in Figure II.29.

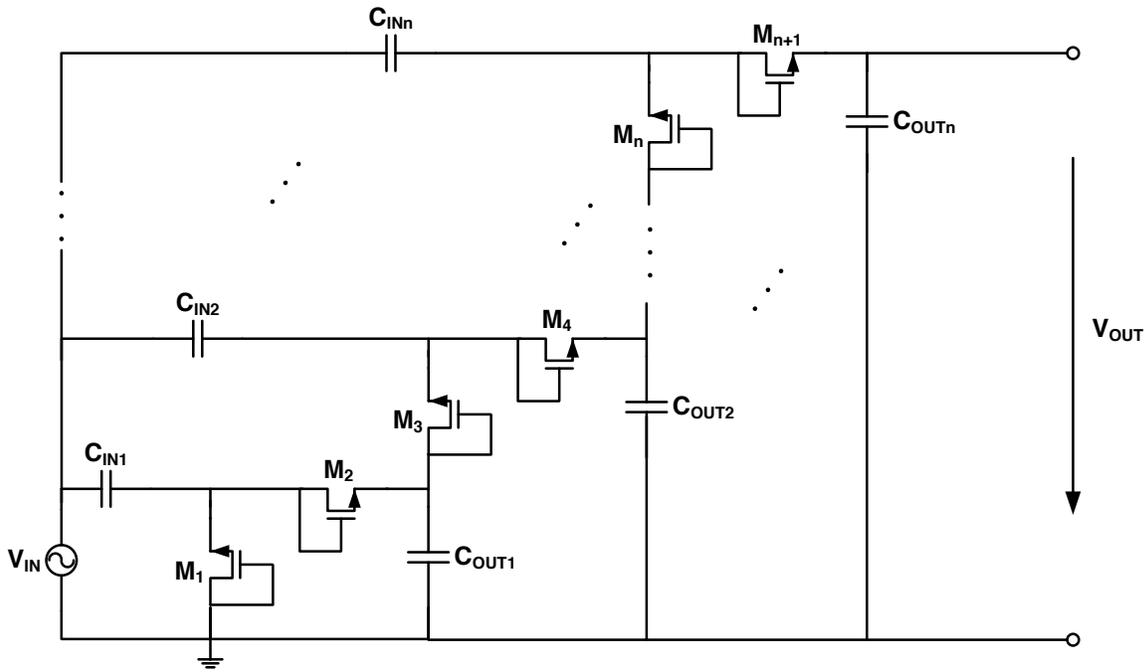


Figure II.29: *N*-stage traditional voltage multiplier architecture.

In this case, a higher output voltage is obtained through the accumulation of stored charge transferred from the output of one stage to the input of the following. After cascading several voltage multipliers, the retrieved voltage at C_{OUTn} is multiplied by the number of employed stages as previously described by equation (II.8).

Although higher output voltages can be obtained implementing this architecture, increasing the number of stages practically impairs the circuit sensitivity, since power losses are increased by the number of devices and, consequently, degrades the power conversion efficiency.

Figure II.30 presents the efficiency, η , and the input voltage, V_{IN} , required to power supply a load of 400 k Ω for several n-stage traditional voltage multiplier configurations with an input power of -21 dBm. First, it is noticed that increasing the number of stages, the efficiency decreases. However, the input voltage required to achieve an equivalent output voltage reduces with the number of stages, which improves the overall sensitivity of the rectifier.

Knowing the drawback about low input power and voltage received in a long distance operation previously discussed, the number of stage choice is a tradeoff between the efficiency, η , and the required input voltage V_{IN} . For this reason, a 3-stage voltage multiplier is chosen for the rectifier implementation. The PCE is sacrificed in order to make the rectifier more suited to operate with very low input power.

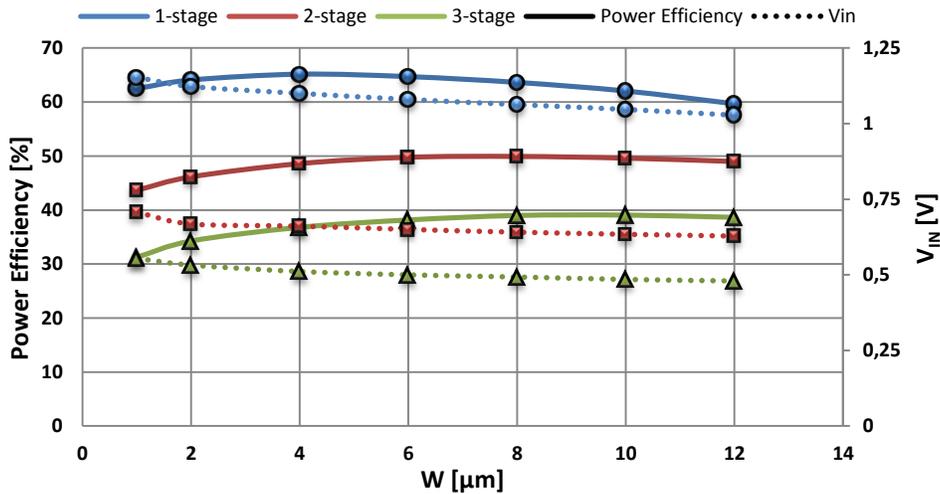


Figure II.30: V_{IN} and η as a function of W for different N -stage traditional voltage multiplier architecture at 900 MHz.

Furthermore, the figure II.30 also shows that the performances of the rectifier depends on the transistor width W . The optimum varies with the number of stages and ranges from 4 μm to 10 μm . For our architecture, the optimum point is achieved for a W of 8 μm . Figure II.31 also shows the stabilized V_{OUT} of 1.12 V for an input power of -21 dBm at steady-state conditions.

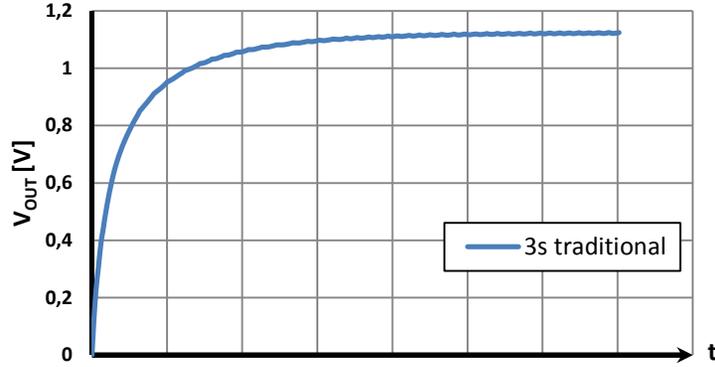


Figure II.31: 3-stage traditional V_{OUT} at steady-state condition.

4.5 Bulk-biased Voltage Multiplier

Threshold voltage is a process dependent parameter which is linked to the oxide properties. Some standard CMOS processes offer low and medium threshold devices which could be used to perform low-threshold designs. However, their availability is not yet generalized, and such devices are subject to significant leakage due to higher channel doping leading to excessive power consumption and reliability problems. Thus, low-threshold devices are generally not good candidates to be integrated in the main flow of current towards the load.

As mentioned and according to (II.8), one approach to improve the rectifier performance is to decrease the transistors threshold voltage drop. If we consider the analytic expression of a MOS threshold voltage proposed in (II.32), V_{Th} can be adjusted by controlling V_{SB} voltage. The transistor MOS threshold voltage is expressed as:

$$V_{Th} = V_{Th0} + \gamma \left(\sqrt{2|\varphi_s| + V_{SB}} - \sqrt{2|\varphi_s|} \right) \quad (\text{II.32})$$

where V_{Th0} is the threshold voltage of the long channel device at zero substrate bias, γ the body bias coefficient and φ_s the surface potential; all these parameters are related to the technology.

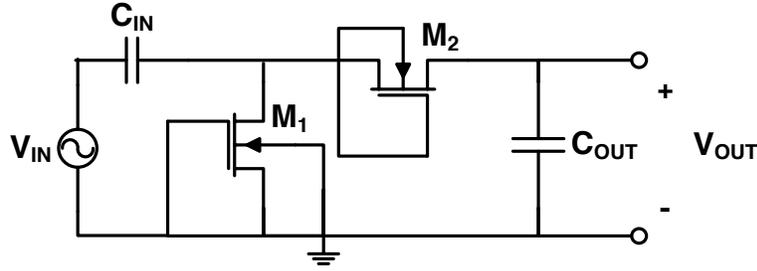


Figure II.32: Bulk-biasing configuration.

The bulk-biasing configuration applied to a voltage multiplier is presented in Figure II.32. It is noticed that the transistors operate either in saturation or in sub-threshold mode. During the conduction phase, the sources of transistors M_1 and M_2 are respectively connected to V_{CG} and V_{OUT} nodes. In this case, their gates are tied to their drains, making a positive V_{GS} required to turn on the transistors. As stated in (II.32), V_{Th} can be decreased by applying a negative V_{SB} voltage.

Considering the non-conduction phase, the transistors change their polarity. Now the drain of M_1 and the source of M_2 are connected to V_{CG} node and their gates are tied to their sources, ensuring sub-threshold operating mode. The leakage current in this operating phase can be expressed as:

$$I_D \approx I_{D0} \cdot e^{\frac{\kappa(V_G - V_{Th}) - V_S}{V_T}} \quad (\text{II.33})$$

where I_{D0} is the current at $V_{GS} = V_{Th}$, the thermal voltage $V_T = \frac{kT}{q}$ and the channel divider $\kappa = \frac{C_{ox}}{C_{ox} + C_D}$ with capacitance of depletion layer C_D and capacitance of the oxide layer C_{ox} .

From equation (II.33), it is noticed that the threshold voltage must be increased in the turn-off mode in order to decrease the leakage current. Hence, the ideal bulk-biasing occurs when V_{SB} is negative in forward bias condition and positive in backwards bias condition, which ensures faster turn on during the conduction phase while reducing the leakage current during the non-conducting phase. However, to perform such configuration, two drawbacks appears: first, some circuitry must be include in the rectifier, which increases the consumption; second, implementing this kind of switch operating in UHF frequencies is very challenging.

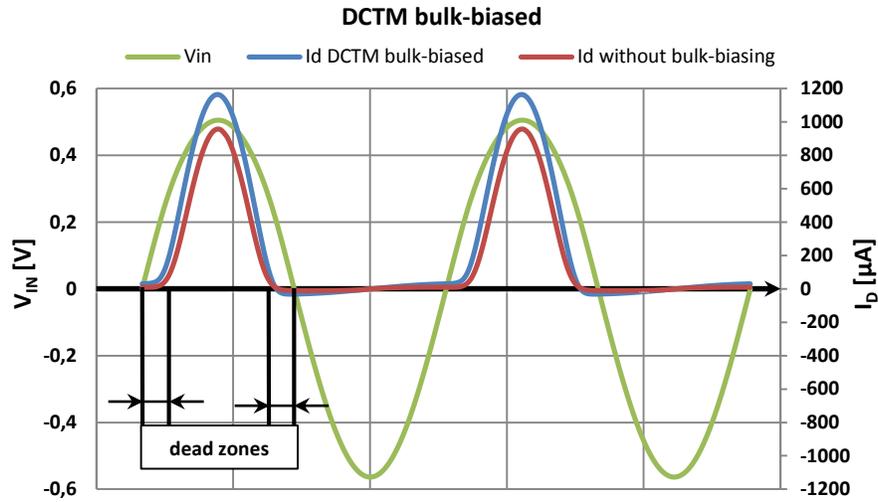


Figure II.33: V_{IN} and I_D for DCTM configuration using bulk-biasing technique.

Figure II.33 shows the I_D - V_{IN} characteristics of a rectifier transistor using the bulk-biasing technique as a function of time. It is depicted that threshold voltage is decreased when compared with traditional configuration as described in II.4.4, which confirms the ability to transfer more energy when this technique is applied.

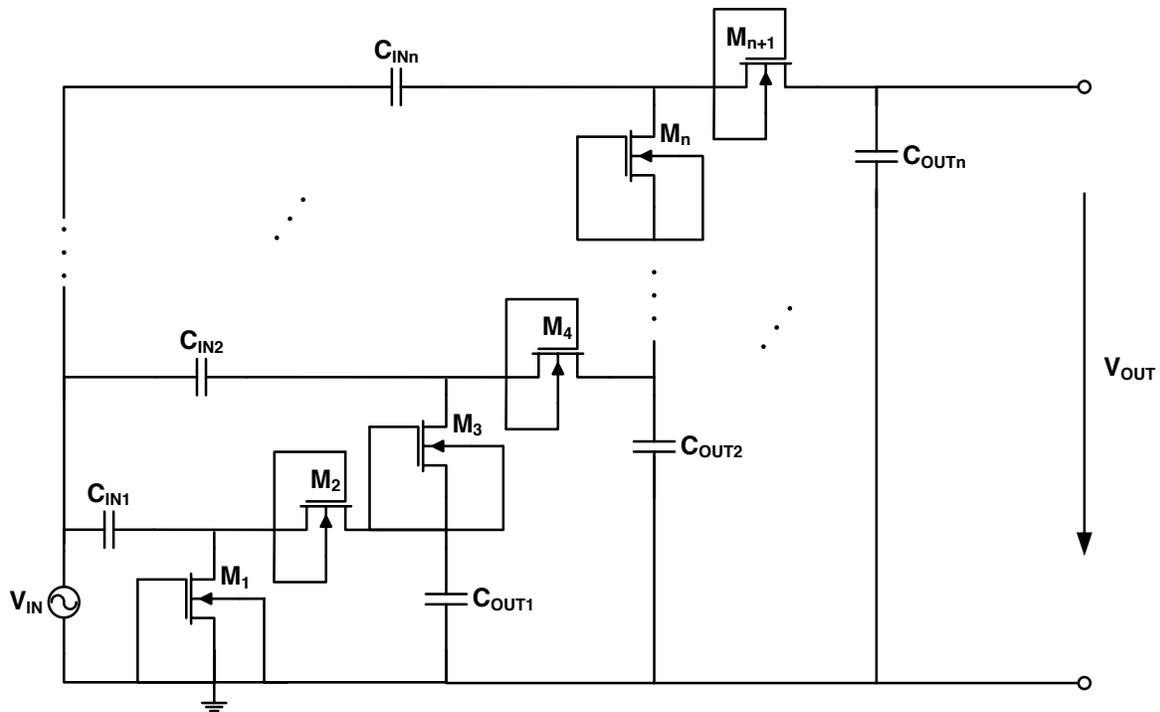


Figure II.34: N-stage bulk-biased voltage multiplier.

As a fully passive solution, the bulk-biasing technique studied here consists in taking advantage of the different voltages provided by the rectifier itself to properly perform the V_{SB} bias. One approach is to connect the transistors bulk with its gate as represented in Figure II.34. This connection provides an improvement in turn-on phase, since the gate voltage is always higher than the source, implementing a dynamic bulk-bias. However, in turn-off phase, V_{SB} is always zero, as source node is attached to bulk. Comparing with the traditional connection to the ground, this new bulk-bias slightly increases the leakage current, but even so the overall power conversion efficiency is improved with body bias technique.

For a fixed input power of -21 dBm, the 3-stage bulk-biased voltage multiplier provides an output voltage of 1.22 V at steady-state condition as shown in Figure II.35. Indeed, as this configuration consists in a variation of the traditional voltage multiplier, the same behavior is noticed with an improved efficiency due to body effect.

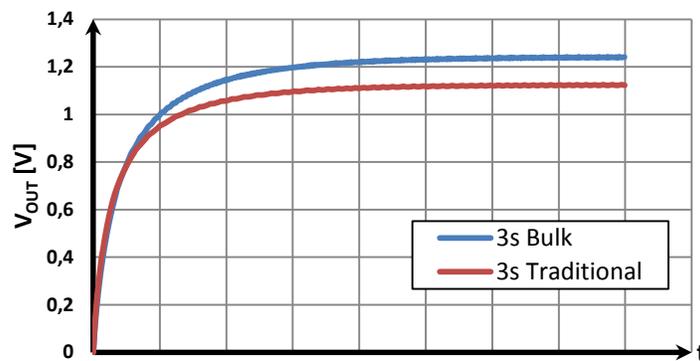


Figure II.35: 3-stage bulk-biased V_{OUT} at steady-state condition.

4.6 DC Bulk-biased Voltage Multiplier

Another topology is performed taking advantage of the same body effect technique described in previous architecture. In this case, the different DC voltages provided by a multi stage rectifier are analyzed. Considering, for instance, an architecture with at least 2 stages and optimizing the transistors of the first stage, Figure II.36. During turn-on phase, higher V_{SB} voltage could be provided to bulk-bias the transistors M_1 and M_2 using the available voltage at V_{DC1} or higher, which increases the body effect, resulting in an improved energy transfer.

However, considering turn-off phase, PN junctions must be taken into account. Actually, bulk-biasing the transistors in this operation mode could turn on parasitic diodes, mainly if V_{BS} voltage exceeds 500mV, where forward bias of PN junction begins to degrade the rectifier performances for low-power applications.

Usually to power supply a load of $3.6\mu\text{W}$ at 1.2V, the input voltage amplitude required must be higher than 250mV, which easily results in a V_{BS} higher than forward PN junction conduction limits, since it is estimated as $2V_{IN}$ in worst case. For this reason the voltages available at V_{DC-N} or higher are avoided when biasing a stage N under these conditions. So a topology is proposed in Figure II.36 to improve the voltage multiplier performances throughout body biasing technique with a DC voltage provided by stage N-1. This configuration implements a lower V_{SB} voltage in turn-on phase, but, in addition, decreases the leakage current in turn-off phase when compared with the traditional circuit, ensuring a stable operation without degrading power conversion efficiency due to parasitic devices further discussed in section II.4.8.

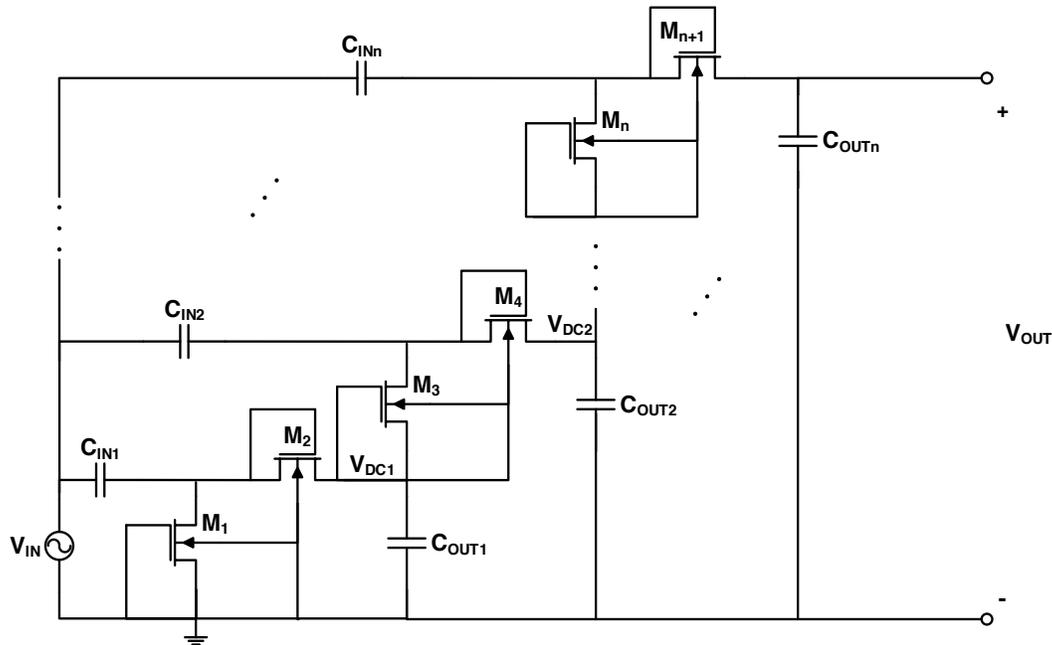


Figure II.36: N-stage DC bulk-biased voltage multiplier.

The PCE, η , and the input voltage, V_{IN} , required to operate under the conditions imposed by the specifications is presented in Figure II.37 for several stages using the DC bulk-biasing technique considering a sensitivity of -21 dBm. As expected, the increase in number of stages decreases the efficiency, whereas the input voltage required to perform the energy conversion is

reduced. The tradeoff behavior between the power conversion efficiency and the input voltage is also observed in this topology. Hence, a 3-stage configuration using a W/L of 62 is also implemented in this architecture for the same reasons as discussed in II.4.4.

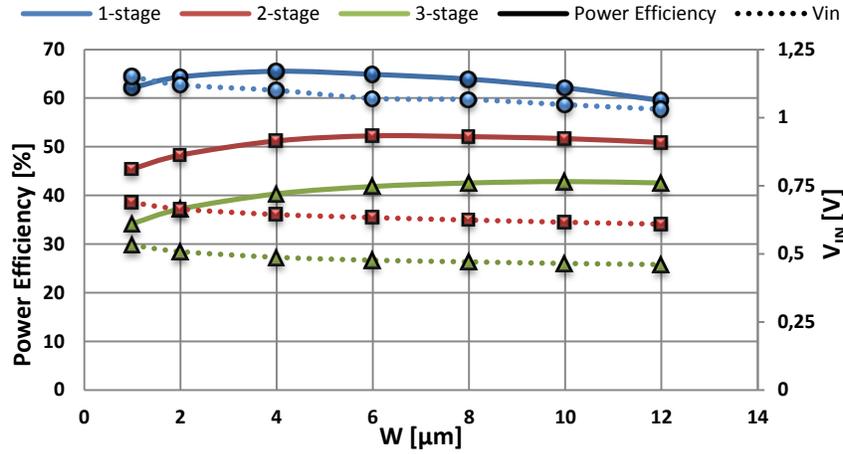


Figure II.37: V_{IN} and η as a function of W for different N -stage DC bulk-biased voltage multiplier architecture at 900 MHz.

For a fixed input power of -21 dBm, the 3-stage DC bulk-biased voltage multiplier provides an output voltage of 1.17 V at steady-state condition as shown in Figure II.38.

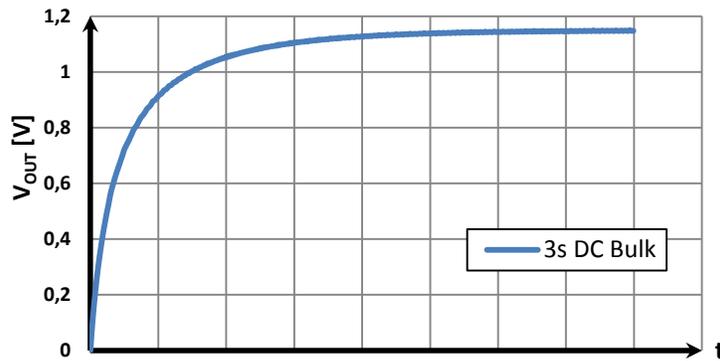


Figure II.38: 3-stage DC bulk-biased V_{OUT} at steady-state condition.

One condition to apply the body-biasing technique and to properly bias the bulk of a NMOS transistor is to guarantee the transistor substrate is isolated. Another one is to ensure a good operation mode by connecting the isolation to the highest DC voltage node of the circuit.

All transistors used into these rectifying circuits are NMOS, so an N type well insulation is required to surround them, which includes PN parasitic diodes into the circuit. As the different DC power supplies existing in such devices are converted by themselves, it is difficult to avoid

nodes with higher peak voltages inside the circuit than the provided DC voltages in output stages. Therefore, connecting the anode side into an AC signal is not a good option, since that could start the parasitic diodes conduction, increasing the losses.

To guarantee that the N-well insertion does not increase the power dissipation, the bulk-biasing strategy chosen in this topology consists in connecting all transistor's bulks with a DC voltage, which improves the power conversion on turn on mode, but not as good as dynamic bulk-biasing as detailed in II.4.5, and at the same time ensures all probably parasitic devices to be turned off. Among several DC nodes, the transistor body bias in this architecture uses the DC voltage provided by previous stage as shown in Fig. 4.

4.7 Cross-coupled Voltage Multiplier

A common configuration to compensate the V_{Th} is the cross-coupled technique applied in some VCO architectures and some rectifiers, where input voltage amplitude is higher than provided output voltage [81], as described in II.3.2.4 . The topology proposed here is to combine the cascaded approach of voltage multiplier with cross-coupled technique. Figure II.39 illustrates a differential cross-coupled architecture applying this technique to perform one-stage full-wave rectifier using two voltage multipliers. Concerning the voltage multipliers they are implemented with NMOS and PMOS transistors in order to take advantage of differential signals to proper generate the desired DC voltage.

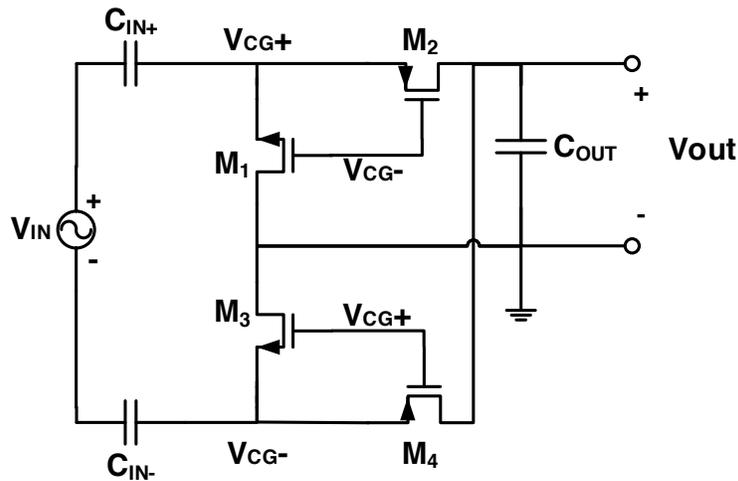


Figure II.39: 1-stage cross-coupled voltage multiplier architecture.

The basic operating principle assumes that the RF signals V_{CG+} and V_{CG-} are large enough to turn the transistors on and off. During the positive half cycle of input signal, V_{CG+} is high and V_{CG-} is low. In this case M_2 and M_3 are on and M_1 and M_4 are off. The current flows to V_{OUT} through M_2 and some charges start to be accumulated into C_{IN-} through M_3 . During the last half of the cycle, M_2 and M_3 turn off and M_1 and M_4 are on, this time the current flows to V_{OUT} through M_4 and the charge is stored into C_{IN+} through M_1 .

As the matter of consequences the V_{GS} voltage must be greater than the transistor voltage-drop, V_{Th} . The gate and source terminals of M_1 and M_2 follow V_{CG+} and V_{CG-} , which are out of phase. Then, when source voltage is slightly below $-\frac{V_{Th}}{2}$, gate voltage is slightly above $\frac{V_{Th}}{2}$, making a V_{GS} required for transistor conduction as presented in Figure II.40. Thanks to this technique the threshold voltage is decreased by 50% in relation to traditional voltage multiplier and the available voltage observed at C_{OUT} is expressed as:

$$V_{OUT} = 2 \cdot \hat{V}_{IN} - V_{Th_{NP}} \quad (II.34)$$

where, V_{IN} is the amplitude of the differential signals and $V_{Th_{NP}} = \frac{V_{Th_{NMOS}}}{2} + \left| \frac{V_{Th_{PMOS}}}{2} \right|$. Thus, the maximum output voltage not exceeds $2V_{IN}$. The output voltage is substantially increased with the cross-coupled technique, since a simultaneous reduction in the turn-on voltage and leakage current is achieved, which in turn leads to higher power conversion efficiency for small input powers.

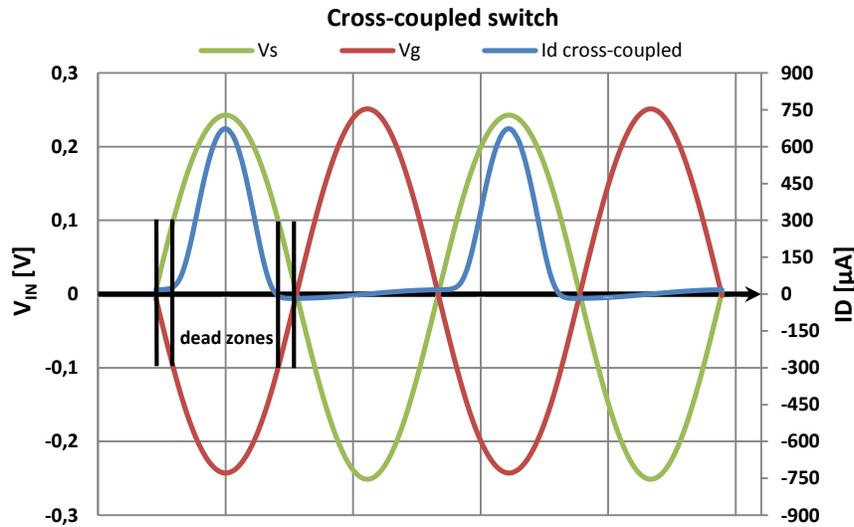


Figure II.40: V_{IN} and I_D for a switch PMOS transistor using cross-couple technique.

It is also noticed that the transistors of a cross-coupled architecture are no longer diode-connected, since they act as switches to minimize the voltage drop between V_D and V_S . Therefore, the 3 operating modes of the transistors can be observed during the RF to DC energy conversion. When:

- $V_S(t) \leq \left| \frac{V_{Th}}{2} \right|$, the transistors are operating in weak inversion mode,
- $\left| \frac{V_{Th}}{2} \right| < V_S(t) \leq |V_{Th}|$, they are operating in saturation mode,
- $V_S(t) > |V_{Th}|$, triode mode is observed.

The advantage of implementing this switched structure compared to a voltage multiplier using DCMT devices is the reduction in turn-on voltage and, thus, providing higher output voltage for the same input voltage amplitude. However, the cross-coupled structure suffers from a reverse conduction during a short period of time at steady-state conditions when the transistors interchange their polarity, which increases the leakage current. Figure II.41 illustrates this phenomenon which creates additional power losses in both transistors NMOS and PMOS.

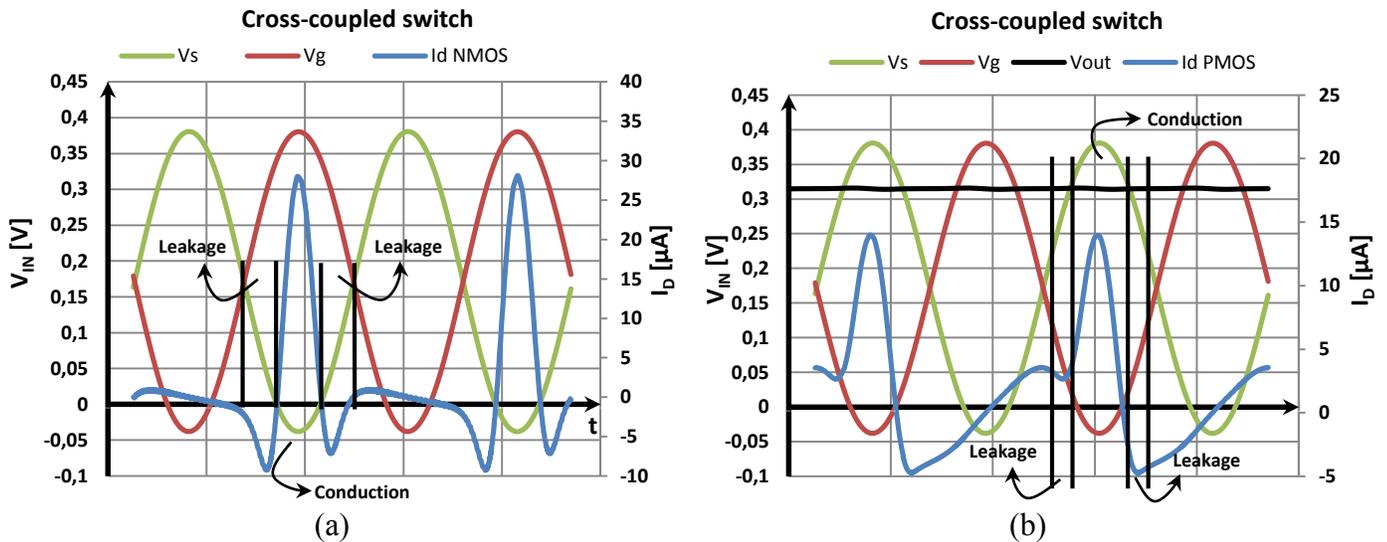


Figure II.41: Transistors behavior at steady-state conditions: (a) NMOS, (b) PMOS.

A multi stage approach implementing several cascaded cross-couple voltage multipliers in order to increase the output voltage delivered to the load is proposed in Figure II.42. The output DC voltage V_{OUT} of this full answer differential rectifier, assuming n stages, can be estimated as:

$$V_{OUT} = N \cdot (2\hat{V}_{IN} - V_{ThNP}) \quad (II.35)$$

architecture number of stages due to low input voltage available at long distance, the choice here is to implement a 5-stage cross-coupled voltage multiplier.

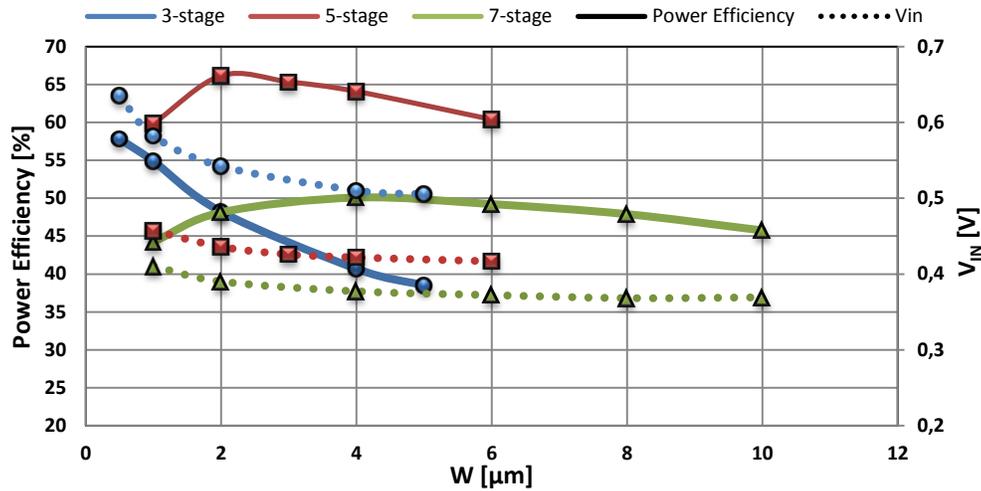


Figure II.43: V_{IN} and η as a function of W for different N -stage cross-coupled voltage multiplier architecture at 900 MHz.

Furthermore, the chart from Figure II.43 shows that the variation in transistors width, W , becomes an important factor over the performances and the design must be handle with care in order to avoid discrepancies in measurements. For this architecture, the optimum point is achieved for a W of 2 μm . Figure II.44 also shows the stabilized V_{OUT} of 1.45 V for an input power of -21 dBm at steady-state conditions.

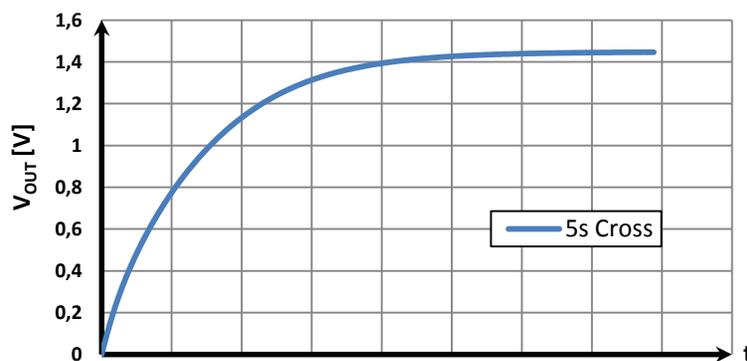


Figure II.44: 5-stage cross-coupled V_{OUT} at steady-state condition.

4.8 Layout Considerations

4.8.1 RF Losses

Part of RF losses comes from the electromagnetic coupling between the metal transmitting the RF signal and the substrate. In microelectronic circuits, these losses are present both in the metal lines and in the RF input pad, since they occupy a considerable large area in silicon. Figure II.45 describes the parasitic devices distributed in integrated structures, which demonstrates a formation of a parasitic high-pass filter between the different metal levels and substrate. The filter resistance comes from the substrate resistivity, whose the value cannot be disregarded in CMOS technology and the filter capacitance is formed by the parasitic between the metals with RF signal and substrate. The cut-off frequency can be estimated as:

$$f_c = \frac{1}{2 \cdot \pi \cdot R_{Substrate} \cdot C_{coupling}} \quad (\text{II.36})$$

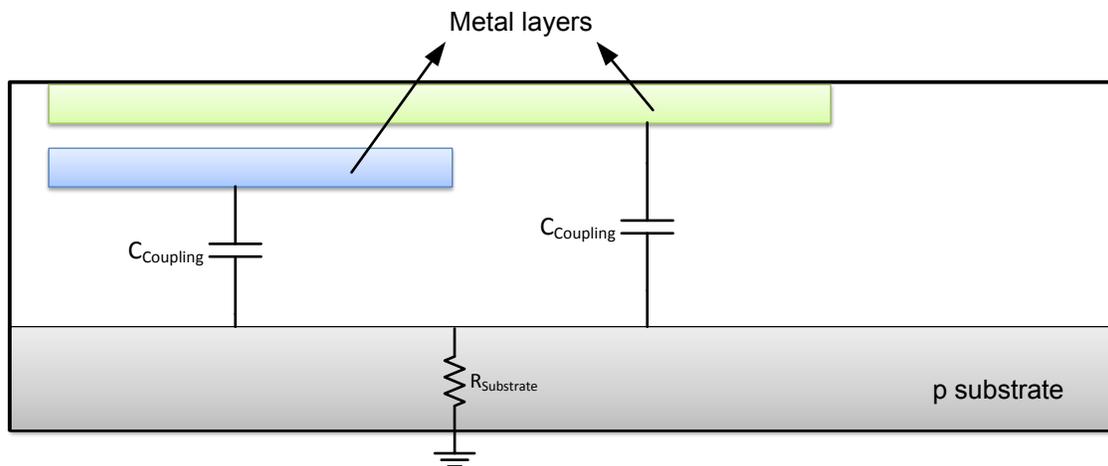


Figure II.45: 2D view of parasitic RF losses.

From the equation (II.36), it is noticed that with the increase of parasitic values, the cut-off frequency tends to decrease, which increases the RF losses for lower frequencies. To lower the losses, it is necessary to reduce the parasitic resistance and capacitance. Optimizing the parasitic capacitance demands the use of highest metal layer available in the technology, since these circuits

are fabricated to operate in low power conditions, the metal series resistance can be neglected, thus, only one metal is enough to conduct the current under these conditions. As discussed in Chapter I, the technology chosen to fabricate the rectifiers is a standard 130nm CMOS with six metal levels. Therefore, the RF signals and PADS are routed mostly in the highest metal layer 6, thus, avoiding the losses throughout parasitic capacitances.

Concerning the parasitic resistance, the technique consists in using a layer less resistive to perform the ground connection, isolating the substrate. This is the reason why a ground plan is important when designing circuits operating at UHF and beyond. It consists in protecting the RF tracks and PADs with metal layer 1, which is less resistive than the substrate and the farthest metal layer from metal 6. Hence, decreasing the connection resistance to the ground, whereas avoiding a large increase in capacitance.

Despite metal 1 is located in a layer above substrate, which slightly increases the parasitic capacitance, the improvement in the parasitic resistance overcomes this drawback. For instance, in this technology, using the ground plan in metal layer 1, the parasitic resistance can be reduced by approximately 10 times, whereas the capacitance is slightly increased by 20%. Under these conditions, the cut-off frequency using the ground plan is now located almost at one decade above, which results in a reduction of 10 dB in power losses.

4.8.2 N Isolation

For the body biasing implementation feasibility in the standard NMOS transistors such as the ones used in the architectures proposed in II.4.5 and II.4.6, a substrate isolation is required in order to properly bias with different potential each NMOS transistor bulk separately. To perform such isolation, a doped N-well must surround the transistor to separate the bulk from the common P substrate. Figure II.46 illustrates the isolation performed with N-well as well as the intrinsic parasitic devices due to its insertion.

One drawback arising from the implementation of an N-well isolation is the intrinsic parasitic devices included with its insertion. Indeed, these parasitic devices impact the rectifier performances, since they increase the overall circuit power consumption due to undesired parasitic forward conduction. To avoid losses, it is better bias the N well with a DC voltage, since if connected in a UHF AC signal could cause a delay to achieve a steady-state potential. Another

issue which comes up with this AC bias is the possibility of a parasitic thyristor conduction due to a NPNP configuration formed between drain or source, bulk, N-well and global silicon. Regarding the proposed architectures using bulk-biasing technique, II.4.5 and II.4.6, both of them suffer from this intrinsic effect due to the need of an N-well insertion.

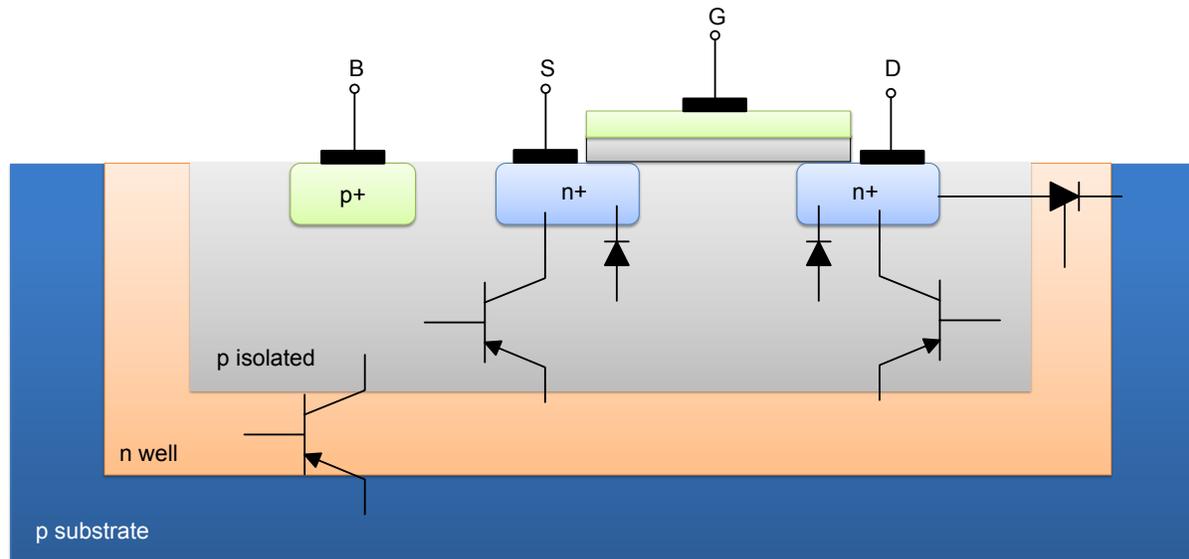


Figure II.46: 2D view of the N isolated transistor with intrinsic parasitic devices.

Disregarding any losses coming from the parasitic devices, the bulk-biased rectifier, II.4.5, presents better performances when compared with the DC bulk-biased architecture. However, when taking them into account, they overcome the benefits of the body-biasing configuration on the bulk-biased circuit. Two main factors contribute to this phenomenon. The first one is the parasitic diodes conduction formed from body P (p isolated) and isolation N (n well) in the last stage transistor bulk M_{N+1} , Figure II.34, in the bulk-biased rectifier, described in II.4.5. As mentioned before, it is preferable to bias an N-well isolation with a DC bias to avoid undesirable losses. However, as the highest DC voltage provided in V_{OUT} is lower than the drain voltage in M_{N+1} for a short period of time, the N-well bias at last stage is not high enough to avoid the parasitic forward conduction, causing undesirable losses. The second factor contributing to the increase in power consumption is the isolation area size, which is larger in bulk-biased configuration, since each transistor must be isolated separately instead of isolated by stage, as it is the case with the DC bulk-biased architecture.

In order to perform reliable rectifiers when a N isolation is needed and taking into account all issues concerning the parasitic devices described before, the bulk-biased rectifier was not prototyped, since either biasing the N isolation with a DC or AC signal causes parasitic devices conduction, decreasing the overall rectifier power efficiency and making this topology less advantageous than the DC bulk-biased for fully passive applications. However, if these circuits are intended for more complex systems, such as semi-passive or active RFID TAGs, where other higher DC signals could be used to bias the N isolation, the bulk-biased architecture becomes more interesting, since all issues concerning the forward conduction of parasitic diodes are avoided, ensuring a better performance.

4.9 Comparison Results

To compare the rectifier circuits prototyped in this thesis work, described in II.4.4, II.4.5, II.4.6 and II.4.7, we first consider the power conversion efficiency to evaluate the rectifiers. Figure II.47 (a) and Figure II.48 (a) depict the efficiency behavior of the rectifiers as a function of input power. It is noticed that the traditional and DC bulk-biased voltage multiplier achieve an efficiency higher than 70% at -6 dBm, whereas the maximum of the cross-coupled topology peaks at approximately 67% requiring -20 dBm. Afterwards, the PCE starts to drop significantly.

Analyzing the traditional and DC bulk-biased architectures after the peak power efficiency, it is noticed an excessive leakage current, which increases the overall circuit consumption. This leakage occurs due to breakdown voltage of the parasitic PN junction diodes in rectifiers' last stage, which is achieved when the voltage across them exceeds 10 V in prototyped technology.

The current behavior in cross-coupled topology, Figure II.42, acts differently, it starts to increase dramatically when the output voltage reaches 1.5 V. This increase in current consumption comes from the leakage in both NMOS and PMOS transistors as previously mentioned and described in II.4.7. This phenomenon is more critical in transistors of the first stage, M_{1+} , M_{2+} , M_{1-} and M_{2-} , since the leakage current of these transistors flows directly to the source reference instead of being "re-stored" into the coupling capacitors (C_{OUT1+} until C_{OUTn+}), as it is the case for the leakage current from second stage up to n-stage.

Furthermore, this transistor leakage is proportional to the input voltage amplitude, since the transistors V_{GS} voltage becomes higher and higher with the increase of input power, which makes the reverse conduction of the transistor becomes longer as the voltage increases. Therefore,

the cross-coupled power conversion efficiency is dictated by a tradeoff between the improvement in voltage conversion and the leakage current loss.

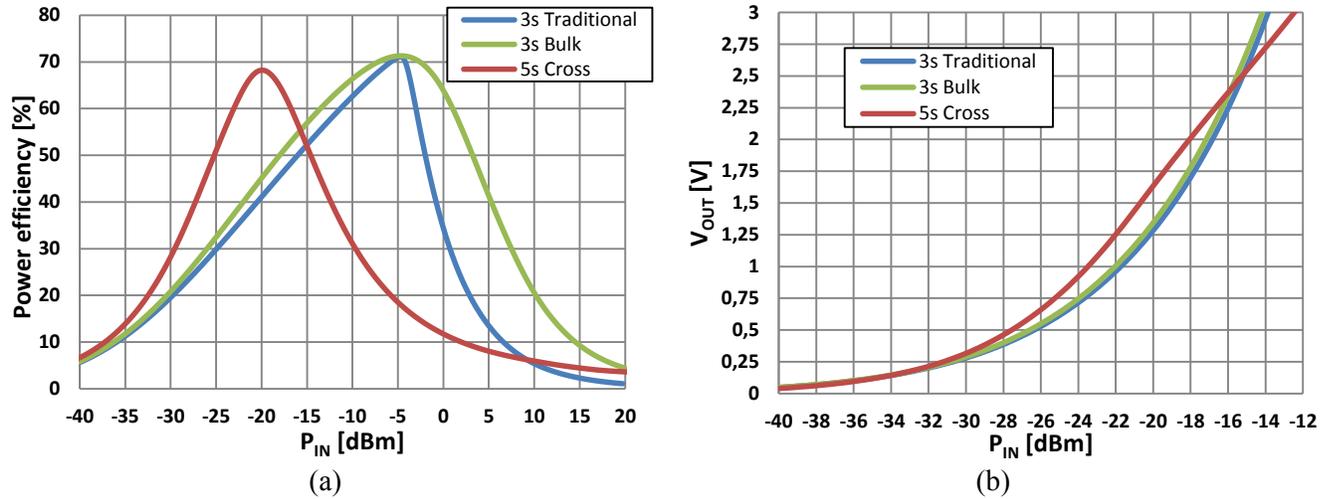


Figure II.47: (a) Rectifiers power efficiency as a function of input power, (b) V_{OUT} as a function of P_{IN} at 900 MHz.

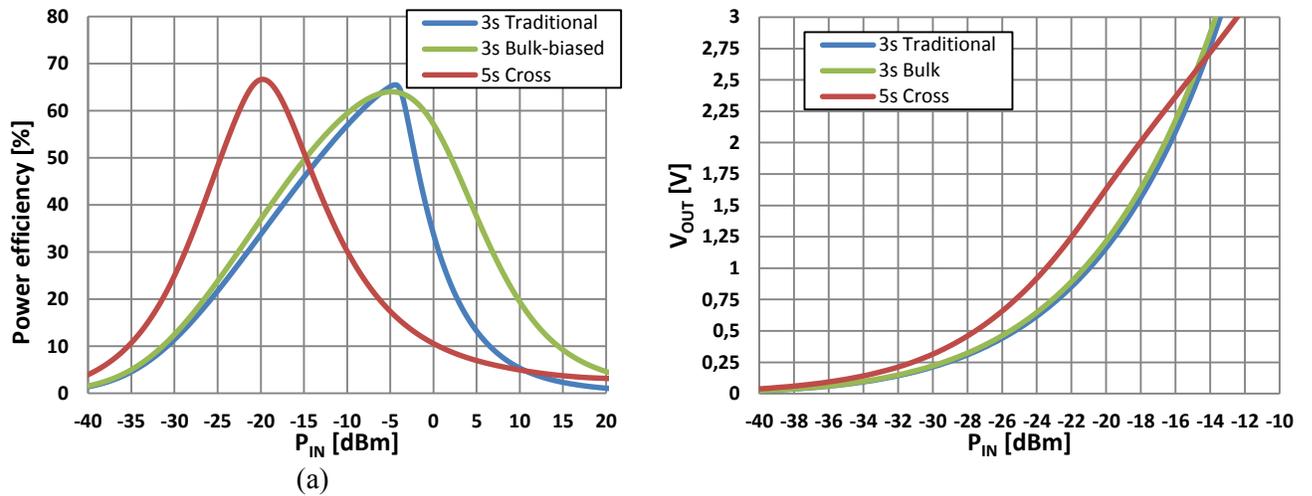


Figure II.48: (a) Rectifiers power efficiency as a function of input power, (b) V_{OUT} as a function of P_{IN} at 2.4 GHz.

Considering the operation in low-power region, where the rectifier is designed for, TABLE II.3 summarizes the rectifier performances for a fixed output power of $3.6 \mu\text{W}$ delivering 1.2 V, as required by the specifications. Under this conditions, it is noticed that the cross-coupled voltage

CHAPTER II DESIGN AND CHARACTERIZATION OF RECTIFIERS FOR LOW-POWER APPLICATIONS

multiplier presents the best sensitivity, -22.4 dBm, followed by the DC bulk-biased circuit, -21 dBm, and the conventional rectifier, -20.4 dBm.

Analyzing the behavior of the rectifiers at different operating frequencies, the single architectures present a degradation of approximately 0.5 dB when the operating frequency goes from 900 MHz to 2.4 GHz, whereas only 0.1 dB is observed for the differential architecture. First, the rectified power at 900 MHz is higher than 2.4 GHz as expected. This difference comes from parasitic losses of MOS devices, which increase with their frequency. Hence, at higher frequencies, the rectifiers' sensitivity is lower, since they need more power to compensate this losses.

TABLE II.3 PLS results of different voltage multiplier performances in 900 MHz and 2.4 GHz for a fixed output power.

	3s Traditional		3s Bulk-biased		5s Cross-coupled	
	900 MHz	2.4 GHz	900 MHz	2.4 GHz	900 MHz	2.4 GHz
V_{OUT} [V]	1.2	1.2	1.2	1.2	1.2	1.2
V_{IN} [mV]	505	505	450	450	390	390
P_{IN} [dBm]	-20.4	-20	-20.9	-20.5	-22.4	-22.3
η [%]	41	34	44	37	63	61
Z_{IN} [Ω]	31-j682	4.7-j256	35-j683	5.4-j257	70-j954	9.7-j360

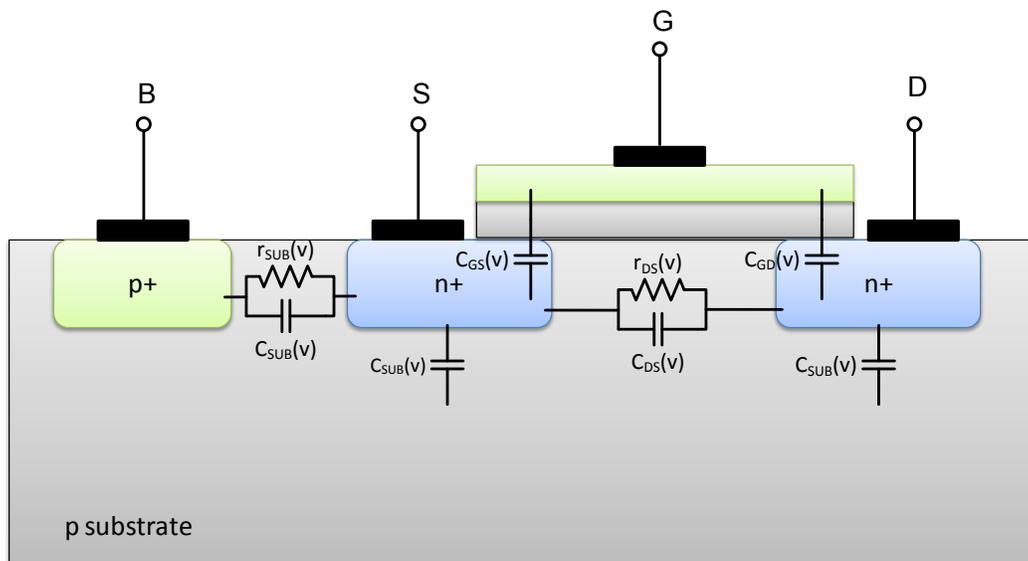


Figure II.49: Transistor MOS intrinsic devices.

Another important parameter of the rectifiers is the input impedance. Indeed the power transfer from the antenna to the rectifier will be further conditioned by the ability to perform impedance matching, which is primordial when performing the entire wireless receiver to transfer the maximum power available at the antenna to the rectifier. Usually, the input impedance of rectifiers has a negative imaginary part due to the MOS transistor intrinsic capacitor. To investigate the origin of input impedance characteristics, the different voltage multipliers are analyzed taking into account the transistor MOS intrinsic devices as represented in Figure II.49.

In the topologies described in II.4.4, II.4.6 and II.4.7, it is noticed that the transistors seen by input are in shunt configuration, since the input and output capacitors, C_{IN} and C_{OUT} , can be neglected at the operating frequencies, 900 MHz and 2.4 GHz, due to their high values. Figure II.50 shows the equivalent circuits for an n-stage voltage multiplier.

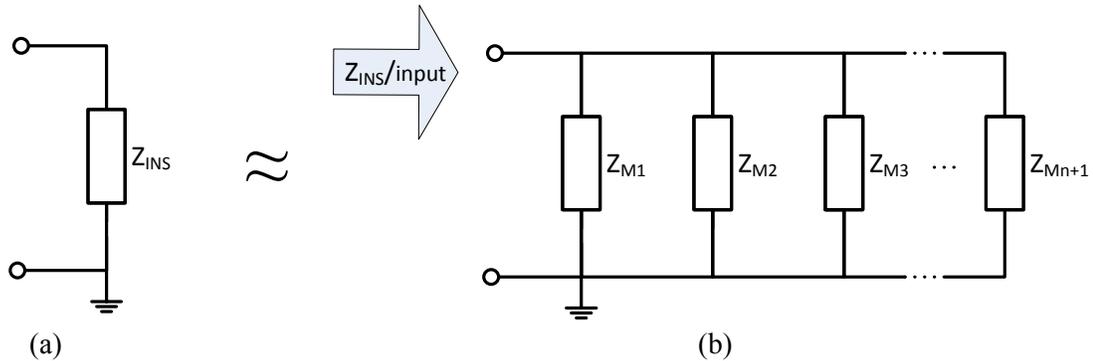


Figure II.50: Equivalent impedance circuit seen by every input of voltage multipliers.

As the n-stage voltage multipliers are built-in cascading several single-stage blocks, we will further consider that every stage implemented into the final structure adds a parallel impedance to the equivalent circuit as represented in Figure II.50. One-stage is first analyzed and for a single stage, we have:

$$Z_{INS} = Z_{M1} // Z_{M2} \tag{II.37}$$

If both transistors could be considered similar, $Z_M = Z_{M1} = Z_{M2}$, as is the case for the single rectifiers, the input impedance simplifies to:

$$Z_{INS} = \frac{Z_M}{2} \tag{II.38}$$

As shown in Figure II.49, the impedance presented by a transistor, Z_M , is mostly influenced by the turn on resistance and parasitic capacitors, resulting in an equivalent RC configuration.

$$Z_M = R_M // \frac{1}{j\omega C_M} \quad (\text{II.39})$$

where:

$$R_M = r_{DS} // r_{SUB} \quad (\text{II.40})$$

$$C_M = c_{DS} + c_{GS} + c_{SUB} \quad (\text{II.41})$$

Taking into account the several stages in the input impedance analysis, it is noticed that the devices of every stage is added in a parallel configuration in the equivalent circuit. Therefore, the rectifier overall input impedance can be expressed as:

$$Z_{INS} = \frac{Z_M}{2N} \quad (\text{II.42})$$

where:

$$R_{INS} = \frac{R_M}{2N} \quad (\text{II.43})$$

$$C_{INS} = 2N \cdot C_M \quad (\text{II.44})$$

PADs and RF traces also contribute to the input impedance of the rectifier. Of capacitive type, it affects the imaginary part of the impedance. Considering their surface in the die, they increase considerably the capacitance value. An equivalent circuit of a single stage rectifier is proposed in Figure II.51, it includes PADs and RF path contributions to its input impedance –i.e. $C_{RFtraces}$ and C_{PADs} –.

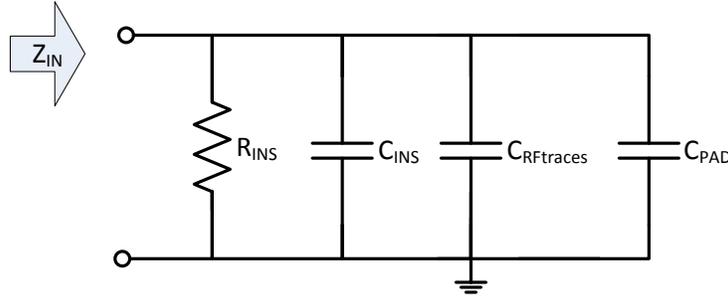


Figure II.51: Representation of devices contributing to single rectifier input impedance.

Investigating the cross-coupled voltage multiplier, the behavior is similar to the equivalent circuit impedance in single topologies, except in this differential architecture the simplification $Z_{M1} = Z_{M2}$ is no longer valid, since different types of transistors are used, NMOS and PMOS. Thus, the impedance seen by each input is, at this moment, estimated as:

$$Z_{INS} = \frac{Z_{NMOS}}{N} // \frac{Z_{PMOS}}{N} \quad (II.45)$$

The differential input impedance for the cross-coupled topology results in an addition of both positive and negative inputs. As it is symmetric designed, both inputs see a similar impedance. Then:

$$Z_{IND} = 2Z_{INS} = R_{IND} // \frac{1}{j\omega C_{IND}} \quad (II.46)$$

where:

$$R_{IND} = \frac{2}{N} \cdot (r_{DSn} // r_{DSP} // R_{SUBn} // R_{SUBp}) \quad (II.47)$$

$$C_{IND} = \frac{N}{2} (c_{DSn} + c_{GSn} + c_{GDn} + c_{DSP} + c_{GSp} + c_{GDp} + c_{SUBn} + c_{SUBp}) \quad (II.48)$$

n: NMOS
p: PMOS

Analogously to the description of single stages circuits, taking into account both transistors and layout parasitic devices contributing to the differential input impedance, the Figure II.52 shows an equivalent circuit for this differential architecture.

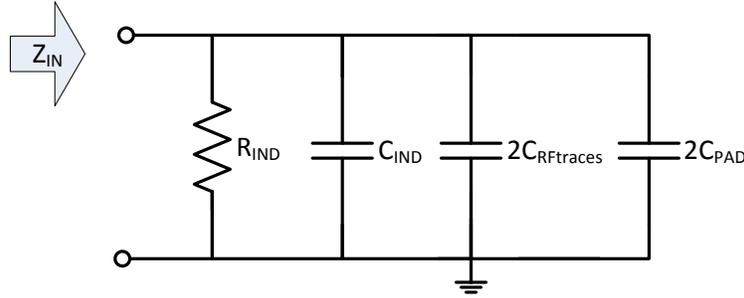


Figure II.52: Representation of devices contributing to differential rectifier input impedance.

Modeling a rectifier with an equivalent parallel RC circuit provides the possibility to easily predict the overall power consumption and also the voltage gain when a matching network is implemented, further discussed in Chapter III.3. Since the impedance is usually expressed in series form $\left(R + \frac{1}{j\omega C}\right)$, a series-parallel transposition is needed to convert into an RC equivalent circuit. The impedance can be expressed as:

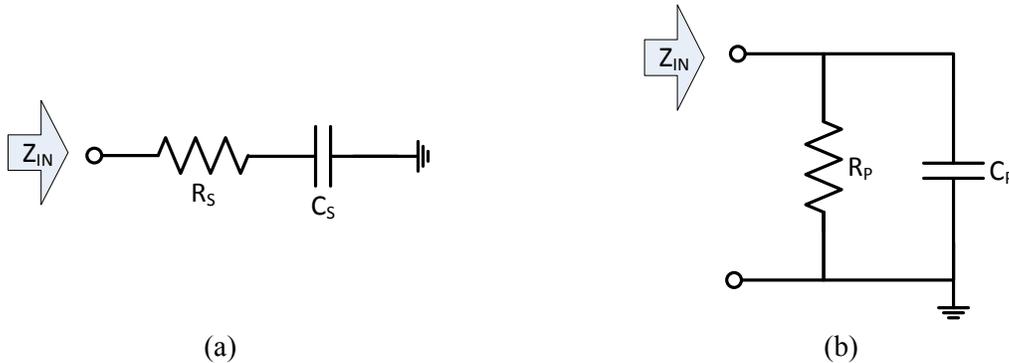


Figure II.53: Rectifier input impedance: (a) series and (b) parallel representation.

$$Z_{IN} = R_S - j\omega C_S = R_P // \frac{1}{j\omega C_P} \quad (II.49)$$

Developing the equation (II.49), it is find out:

$$R_S - j\omega C_S = \frac{R_P}{1 + (\omega R_P C_P)^2} - \frac{j\omega R_P^2 C_P}{1 + (\omega R_P C_P)^2} \quad (II.50)$$

Simplifying the equation (II.50) and isolating the desired variables R_P and C_P :

$$R_p = R_s + \frac{(\omega C_s)^2}{R_s} \quad (\text{II.51})$$

$$C_p = \frac{C_s}{R_p R_s} \quad (\text{II.52})$$

Based on (II.51) and (II.52), we can express generically in a simpler way the rectifier power consumption. Indeed, the active power, previously described in II.4.2.1b), for a sinusoidal input signal is simplified to (II.53) and (II.54), for series and parallel equivalent circuit, respectively.

$$P_{avg} = \frac{1}{2} \cdot \text{Re}(Z_{IN}) \cdot \frac{|V_{RF}|^2}{|Z_{IN}|^2} \quad [\text{W}] \quad (\text{II.53})$$

$$P_{avg} = \frac{1}{2} \cdot \frac{|V_{RF}|^2}{R_p} \quad [\text{W}] \quad (\text{II.54})$$

Considering the equations (II.53) and (II.54), it is noticed that the parallel expression is more convenient for easily calculate either the power consumption P_{avg} , or the input voltage V_{RF} of a rectifier, since it avoids algebraic operations with impedance complex values. For this reason the equivalent parallel RC model is considered to evaluate the rectifier specifications.

Figure II.54 shows the input impedance of the designed rectifiers as a function of input power at 900 MHz and 2.4 GHz operating frequencies. Converting to a parallel equivalent circuit with (II.51) and (II.52) equations, it is interesting to notice that the capacitive value C_p is not sensitive neither to power, nor to frequency as it remains constant over the range of study. TABLE II.4 summarizes the equivalent circuit RC values for the different voltage multipliers. The parameter which most contributes to the impedance variation is R_p , due to its dependence to r_{DS} . It is inversely proportional to the applied voltage and to the power consumption.

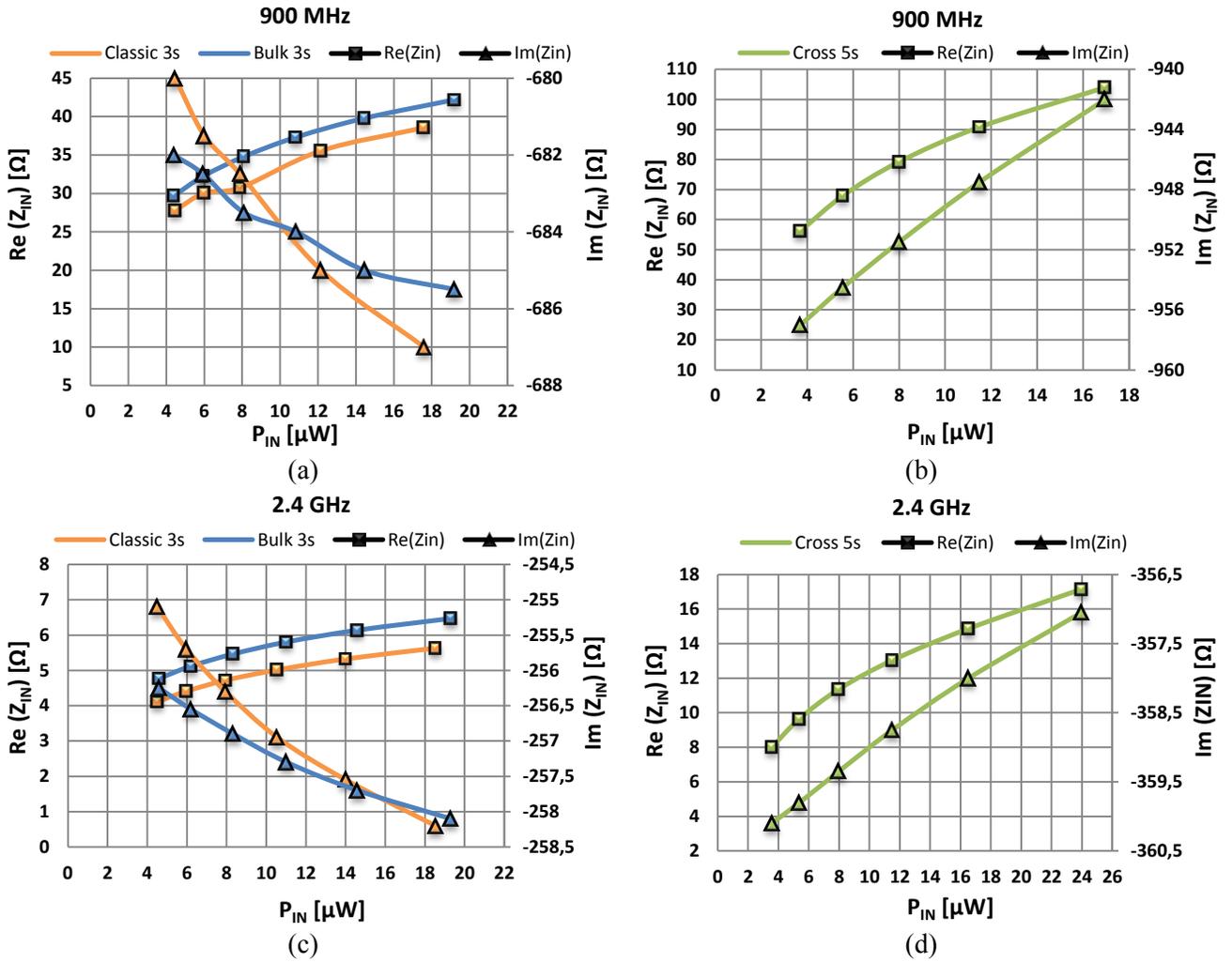


Figure II.54: Input impedance as a function of input power for single architectures (a), (c) and differential architecture (b), (d) at 900 MHz and 2.4 GHz.

TABLE II.4 Equivalent circuit R_P and C_P variations in P_{IN} range at 900 MHz and 2.4 GHz.

	Classic 3s		Bulk 3s		Cross 5s	
	900MHz	2.4GHz	900MHz	2.4GHz	900MHz	2.4GHz
R_P [kΩ]	12~17	11.5~16	11.2~15.7	10.3~13.8	8.5~16.5	7.5~16.5
C_P [fF]	257~259	257~259	257~259	257~259	184~185	184~185

5 Measurement Results

Figure II.55 depicts the micrograph of the different designed voltage multipliers. The die takes place within 0.86 mm including PADs. The entire chip contains 4 circuits:

- An optimized 3-stage traditional voltage multiplier,
- An optimized 3-stage bulk-biased rectifier,
- An optimized 5-stage cross-coupled architecture,
- and an additional 5-stages bulk-biased.

The core of 3-stage rectifiers occupies an on-chip area of $80 \times 100 \mu\text{m}$, whereas 5-stage rectifiers occupies $90 \times 185 \mu\text{m}$. The 5-stage bulk-biased architecture is also included to compare simultaneously the tradeoff number of stages versus power consumption with 3-stages bulk and the performances of the 5-stages cross-coupled with a similar architecture in terms of voltage gain.

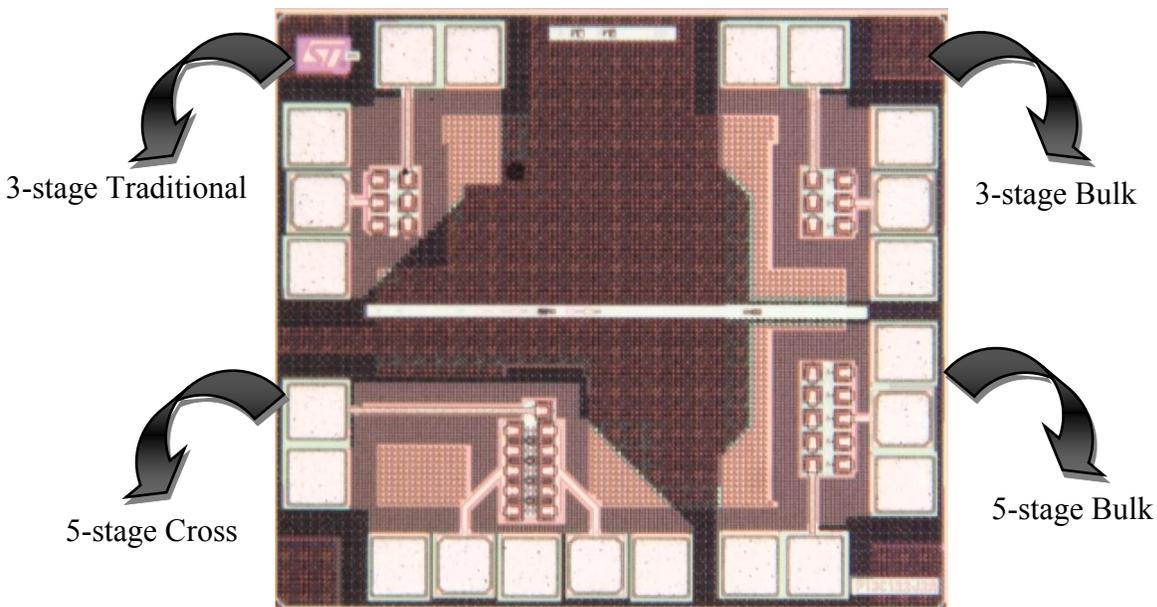


Figure II.55: Micrograph of the voltage multipliers.

Measurements were performed with an Agilent PNA network analyzer E8361A using single configuration with a reference impedance of 50Ω to measure S-parameters at the desired operating frequencies – i.e. 900 MHz and 2.4 GHz –. A common HP multimeter 34401A was also used to measure the output DC voltage provided to the specified load, as outlined in Figure II.56 (a) and illustrated in (b). These measurements were carried out on-chip with an RF Ground-Signal-

Ground (GSG) probe. During the characterization, the device under test (DUT) is excited with an RF source power ranging from approximately -10 to 5 dBm.

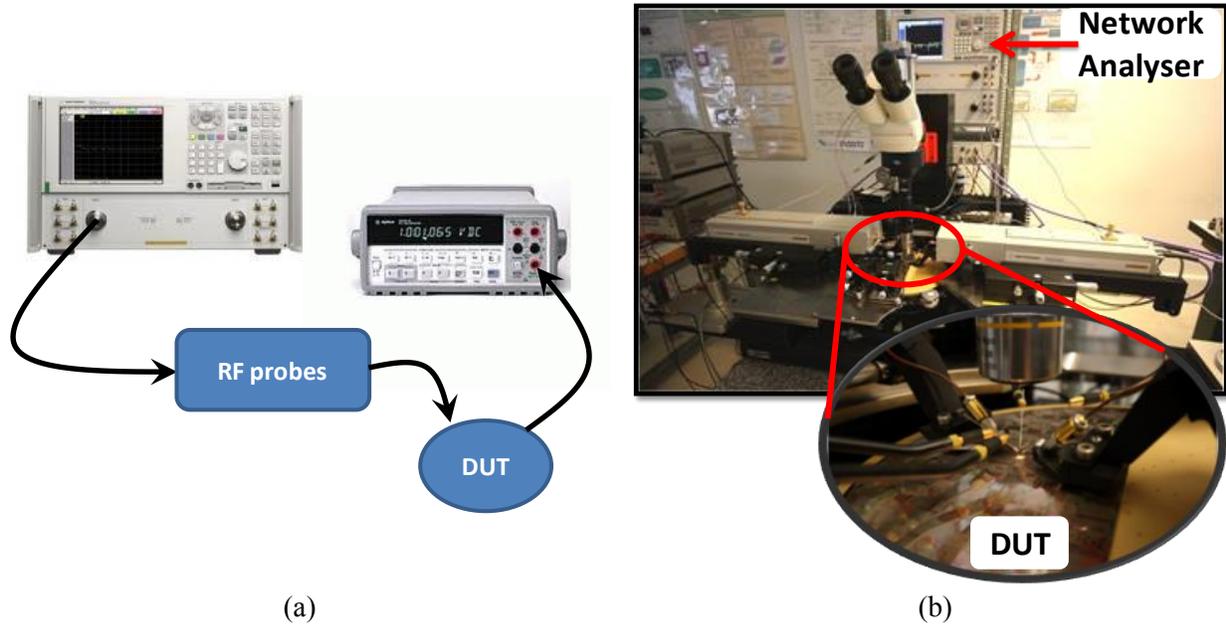


Figure II.56: Measurement setup.

Since the rectifiers are not on-chip matched to 50Ω , to characterize the voltage multipliers in terms of sensitivity, the reflection coefficient must be taken into account to evaluate their power consumption. Thus, the average input power disregarding the mismatch between the equipment and DUT can be estimated as:

$$P_{IN} = P_{source} \cdot (1 - |\Gamma|^2) \quad [W] \quad (II.55)$$

where P_{IN} is the input power required by the DUT, P_{source} the available power send by the PNA network analyzer and Γ the reflection coefficient.

The power efficiency evaluation as a function of input power is presented in Figure II.57 at 900 MHz and 2.4 GHz. It figures out the 3-stage bulk-biased voltage multiplier provides a higher output power with respect to the other two rectifiers over the entire range of considered power, from -30 dBm to -12 dBm reaching its maximum value at approximately 65%, for an input power of -16 dBm. Considering an output power fixed to $3.6 \mu W$ under a 1.2 V voltage supply, the 3-stage bulk-biased voltage multiplier presents an increase of approximately 50% in power

transfer efficiency, compared to the conventional architecture. TABLE II.5 summarizes the results under the specification conditions.

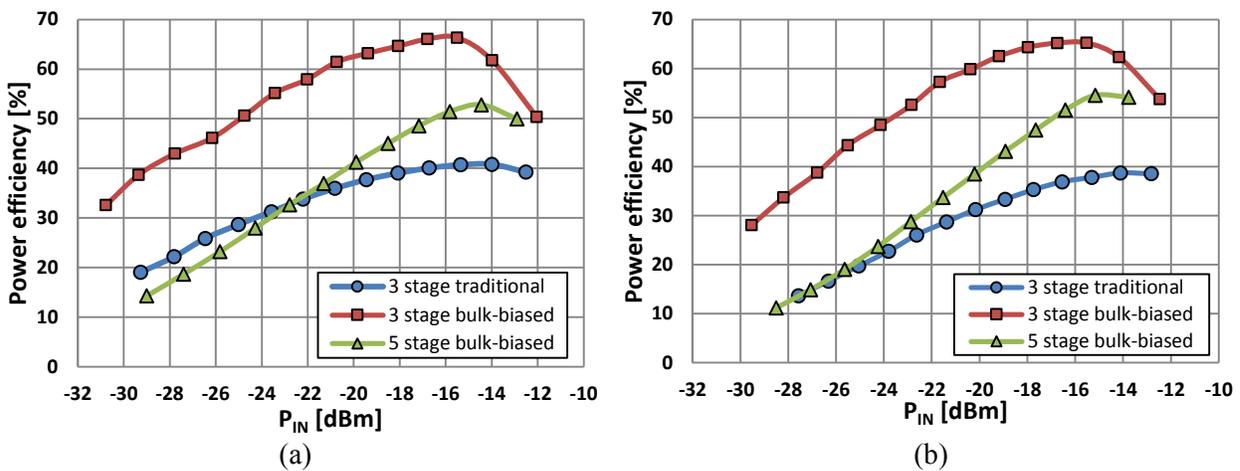


Figure II.57: Rectifier power efficiency as a function of input power at (a) 900 MHz and (b) 2.4 GHz.

TABLE II.5 Measurement results of different voltage multiplier at 900 MHz and 2.4 GHz for a fixed output power.

	3-stage Traditional		3-stage Bulk		5-stage Bulk	
	900 MHz	2.4 GHz	900 MHz	2.4 GHz	900 MHz	2.4 GHz
V_{OUT} [V]	1.2	1.2	1.2	1.2	1.2	1.2
V_{IN} [mV]	440	440	400	400	310	310
P_{IN} [dBm]	-20.2	-19.5	-22	-21.7	-20.7	-20.2
η [%]	38	33	58	56	41	38
Z_{IN} [Ω]	70-j825	12-j311	55-j816	9-j308	70-j613	12-j233
R_P [k Ω]	10	8.5	12.5	11.5	5.5	5
C_P [fF]	213	213	215	215	285	284

According to Figure II.58, when the 3-stage bulk-biased harvester achieves the desired conditions at 1.2 V, the other two voltage multipliers provide an output voltage of approximately 0.9 V, which represents an improvement in voltage conversion of 33%. TABLE II.6 summarizes and compare the results obtained in this thesis with the state-of-the-art structures.

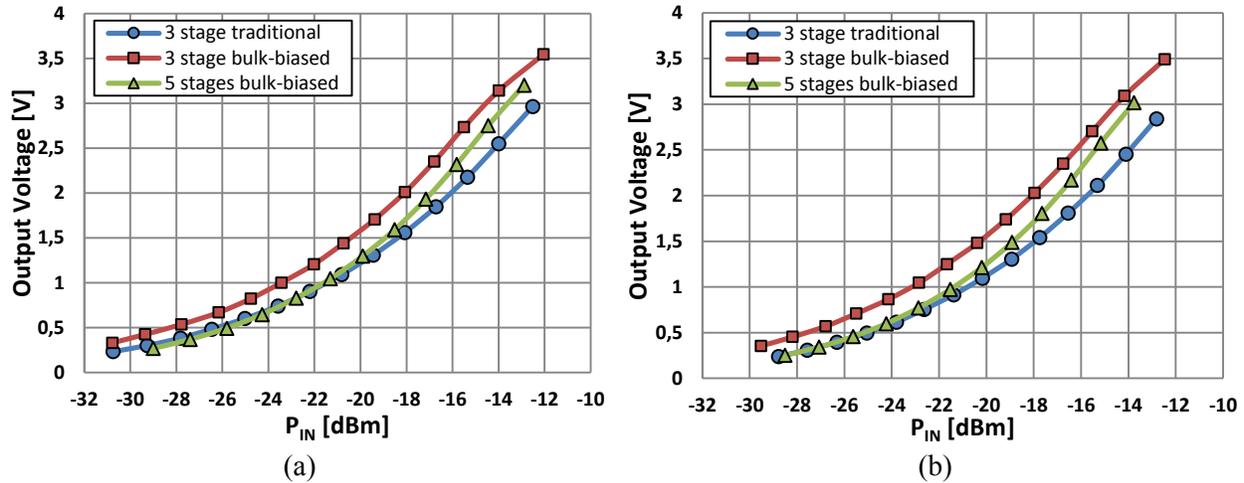


Figure II.58: Rectifier output voltage as a function of input power at (a) 900 MHz and (b) 2.4 GHz.

Analyzing the input impedance of the voltage multipliers, it is observed a variation of approximately 20% in parasitic devices mainly due to an overestimation from parasitic extractor in the Cadence design framework. A process variation in transistors is also noticed, which improves both the input voltage and the threshold voltage when a V_{SB} voltage is different from zero. For this reason the structures using the bulk-biasing technique showed better measurement results than simulation.

6 Conclusions

This chapter concerns the design and characterization of low-power rectifiers operating at 900 MHz and 2.4 GHz. Several basic and state-of-the-art topologies are discussed considering the inconvenients of this circuit dedicated to operate at long distances. Under this low-power availability, the main issue is to properly deliver output voltages greater than the ones available at the rectifier input. For this reasons, the proposed architectures are based on voltage multipliers due to their high ability to perform such purpose.

Another important consideration, prioritized in the development of the RF-to-DC converters, is the power efficiency, since most devices existing today presents very poor performances when operating under -20 dBm input power. Furthermore, a design methodology to

CHAPTER II DESIGN AND CHARACTERIZATION OF RECTIFIERS FOR LOW-POWER APPLICATIONS

the realization of high efficient low-power rectifiers, from the choice of the devices to the layout considerations, is introduced.

The most relevant results related to the low-power RF-to-DC converters are summarized in TABLE II.6 with some realizations of the state-of-the-art rectifiers and the rectifiers developed in this thesis work. It is depicted that the state-of-the-art rectifiers either prioritizes the sensitivity, sacrificing the overall output power delivered, as in [84] and [86] with an input power as low as – 21 dBm. Or increases the input power in order to prioritize the overall power efficiency, as [85]. Furthermore, different design decisions are observed. For instance, the reference [84] prefer to deliver a high output voltage instead of output current, making this design more suited for harvesting applications. For this reason they employ several stages architecture, which sacrifices the power efficiency in order to deliver more output voltage. Whereas references [85] and [86] prefer to deliver higher output current instead, which makes their design more convenient for power transfer applications.

TABLE II.6 Comparison with the State-of-the-Art rectifiers.

	<i>[84]</i>	<i>[85]*</i>	<i>[86]</i>	<i>This work¹</i>		<i>This work²</i>		<i>This work^{3*}</i>	
Freq [GHz]	0.915	0.95	0.95	0.9	2.4	0.9	2.4	0.9	2.4
P_{RF} [dBm]	-18.8	-18.7	-20.7	-20.2	-19.5	-22	-21.7	-22.4	-22.3
V_{OUT} [V]	1.2	0.6	0.5	1.2		1.2		1.2	
Load [MΩ]	1	0.05	0.125	0.4		0.4		0.4	
η [%]	11	54	24	38	33	58	57	63	61
Number of stages	17	3	2	3		3		5	
Technology	90nm CMOS	130nm CMOS	180nm CMOS	130nm CMOS		130nm CMOS		130nm CMOS	

¹ Traditional voltage multiplier

² Bulk-biased voltage multiplier

³ Cross-coupled voltage multiplier

* PLS results

Comparing the results of the circuits designed and prototyped in this thesis work with the state-of-the-art ones, it is noticed that the topologies using body-biasing and cross-coupled technique improves the overall power efficiency, which reaches 63% under the conditions to

deliver 1.2 V @3 μ A and, at the same time, decreases the input power required, providing enough output voltage level to supply most low power applications. This higher sensitivity of the multi-stage voltage multiplier architectures makes them more suited for a long range wireless power transfer –*i.e.* over several meters– as well as opportunistic RF energy scavenging.

The cross-coupled voltage multiplier could not be characterized with the probe station, due to its complexity to be measured with differential inputs. The measurement results of this rectifier is further discussed in Chapter III.4.3 with its characterization in a complete wireless powered receiver module.

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Chapter III

Chapter III. Wireless Energy / Power Transmission

1 Introduction

Advances in low-power electronics and wireless communication devices enable the development of energy-efficient devices, such as RFID tags, wireless sensor nodes for structural health monitoring, as well as other engineering applications [87]-[88]. Much has been written about the benefits of these devices and the potential of energy harvesting to provide power for their life-time.

Disposable, long-life batteries will continue to be used in some wireless sensor applications, but the lifetime of such rechargeable systems can be significantly extended throughout wireless energy harvesting. The greatest potential, however, lies in a new class of devices that will be battery-free and thus enable applications that would have been prohibitively expensive due to the maintenance cost of eventual and repeated battery replacement. Furthermore, the ability to operate systems wirelessly opens up to a ubiquitous implementation of smart devices for which a wired connection cannot be completed.

As previously discussed in Chapter I, the EM energy is a popular solution to perform wireless energy transmission. This approach relies on the use of electromagnetic radiation to provide DC power, which is accomplished by receiving radio waves from the host structure or its surrounding environment with an antenna, converting the signal, and conditioning the output power [89]–[91], as schematically described in Figure II.1. It has been discussed in Chapter I, there are multiple approaches to convert an RF signal to DC power, depending on the desired operating condition. The amount of power available for the end device depends on several factors including

the source power, distance from the source, antenna gain, matching, and overall conversion efficiency.

In this scenario, this chapter describes several Wireless Power Receivers (WPRs) designs developed to operate in a low-power / low-consumption context at 900 MHz and 2.45 GHz. According to the simplified wireless energy harvesting schematic presented in Figure II.1, the antenna and matching blocks are studied and described in this chapter to accomplish a full custom WPR. The RF-DC converter block of the system is implemented with the CMOS low-power rectifiers previously validated in Chapter I.

2 Antennas

Together with the power sensitivity of the integrated rectifiers, the antenna of a wireless receiver plays a key role in the overall performances of a Wireless Energy / Power Transmission (WE/PT) system. Regarding these performances, the overall size, covering distance, directivity and compatibility with other wireless devices are some of the utmost concerns.

Directive antennas, such as patch, Yagi Uda, spiral, horn and parabolic [92]-[95] exhibit a high gain, but only in a limited direction, which is convenient to systems operating in line-of-sight condition. In tracking or harvesting applications, antennas with isotropic radiation characteristics are more suitable to ensure a stable operation when the RF source emits from an unpredicted direction.

Among the several radiation patterns of the antennas, the nearest to the ideal isotropic radiation is the omnidirectional. That is the reason why sometimes the antenna gain is also reported in relation to the typical gain of a standard dipole antenna, dBd, instead to the ideal isotropic antenna, dBi. Since the typical gain of a standard dipole antenna is 2.15 dBi, the relation between dBi and dBd can be expressed as:

$$dBd = dBi - 2.15 \quad (III.1)$$

Most of the antennas for UHF omnidirectional wireless systems are commonly fabricated as modified printed dipoles [96]-[97]. The antenna design purpose is to collect a maximum of EM energy and to perform the complex conjugate of the rectifier front end impedance within a compact

area. These features intend to ensure maximum energy transfer and to make wireless devices as portable as possible. The state-of-the-art proposes a lot of techniques to address this tradeoff, [98]-[99]. Some of them has been applied to develop the antennas proposed in this work

The antennas developed in this thesis focus on an omnidirectional radiation, i.e. dipole antennas, to let the WPRs operational as close as possible to the isotropic radiation pattern and so covering a larger area to harvest emitting RF sources. Several types of dipole antennas are studied and discussed in the following sections to operate at 900 MHz and 2.45 GHz frequency bands.

2.1 Theory of Antenna

An antenna is an electrical device which converts electric power into radio waves, and vice versa [100]. In the domain of telecommunications, the antenna is usually connected to a transceiver, which includes a transmitter part (T_X) and a receiver part (R_X). In R_X , the radiating element intercepts some of the power of an electromagnetic wave in order to deliver an AC voltage at its terminals. Transmission lines then guide these electrical signals to the receiver front end.

The propagation of electromagnetic waves from a radiating element generates different fields according to the distance, Figure III.1. This behavior can be described by Maxwell's equations [101]. However, a direct solution of these equations is complex, since it involves difficult integrations. A general form for the electric field can be expressed as a multipole expansion solution, equation (III.2), obtained from an expansion of spherical harmonics multiplied by spherical Bessel functions [102]:

$$\vec{E} = j30k^2 Idz \left(\frac{j}{kd} + \frac{1}{(kd)^2} + \frac{1}{(kd)^3} \right) \sin\theta e^{-jkd} \quad (\text{III.2})$$

where Idz is the moment of differential current element, d the distance from the radiating antenna to the \vec{E} measuring point and $k = \frac{2\pi}{\lambda}$.

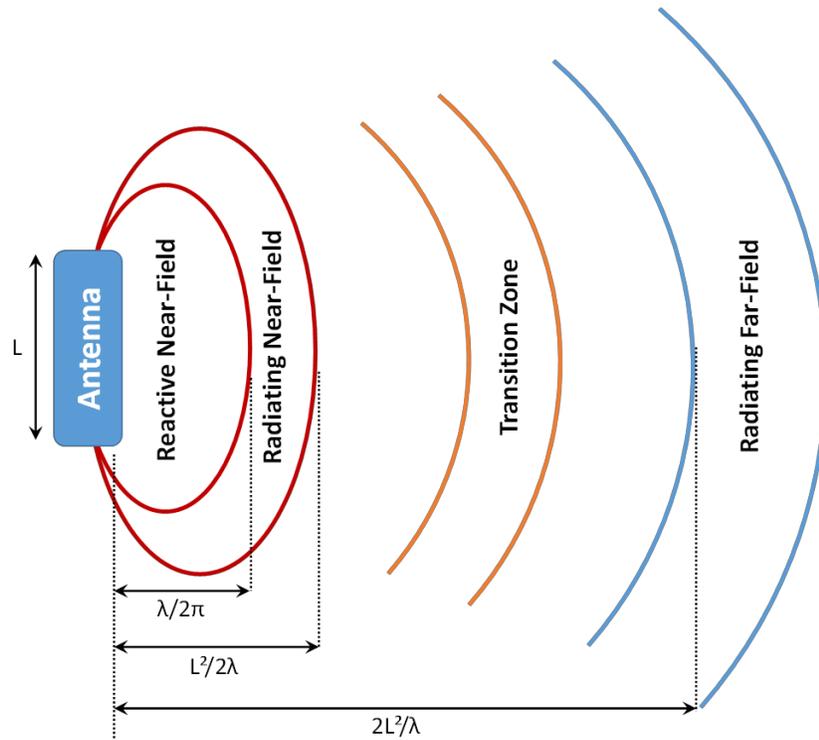


Figure III.1: Field regions for antennas

The fields surrounding an antenna are divided into 3 main regions:

- Reactive Near-field;
- Radiating Near-field or Fresnel Region;
- Far-field or Fraunhofer Region.

The near-field is remarkable for reproducing classical electromagnetic induction and electric charge effects on the EM field, which effects tend to be neglected with increasing distance from the antenna, d , (with magnetic field magnitude proportional to $\frac{1}{d^3}$ and electric field magnitude proportional to $\frac{1}{d^2}$). The near-field impact in overall EM field decreases much more rapidly compared to the classical radiated EM far-field (\vec{E} and \vec{B} fields proportional to $\frac{1}{d}$).

Considering long distance operations, only far-field effects prevail. Therefore, only far-field region is taken into account in this thesis work and further discussed.

2.1.1 Properties of Antennas

a) Radiation Pattern

In the field of antenna design the term radiation pattern, also known as antenna pattern or polar diagram, refers to the angular direction dependence of the strength of the radio waves from the antenna or other RF sources [103].

Figure III.2 and Figure III.3 illustrate the typical 3D and plane sections representation of radiation pattern often used to describe the antennas behavior.

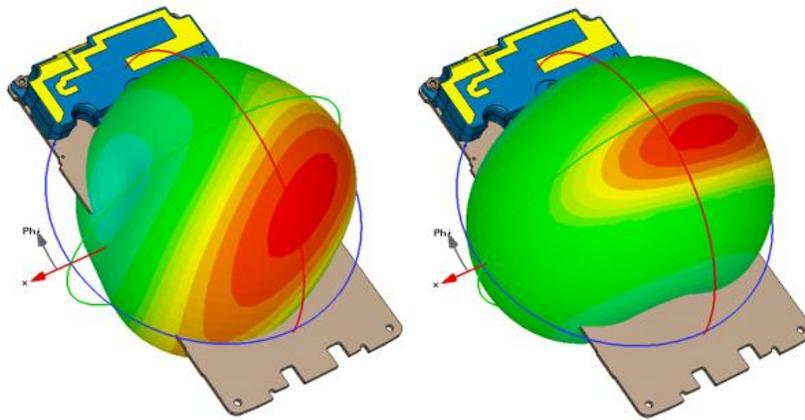


Figure III.2: 3D radiation pattern of a mobile phone antenna operating at 900 MHz and 1.8 GHz GSM bands [104].

A physical antenna has a radiation pattern that varies with direction. It is a fundamental property of antennas that the receiving and transmitting patterns are identical. This is a consequence of the reciprocity theorem of electromagnetics [106]. Therefore, the antenna pattern can be discussed interchangeably either for transmitting or receiving modes.

The radiation pattern is also a function of frequency. However, except where noted, it will be assumed only a single frequency is of interest (described by the corresponding wavelength λ) and can be represented as a single 3D graph or as separated graphs cutting the 3D radiation in the vertical and horizontal plane, as exemplified in Figure III.2 and Figure III.3.

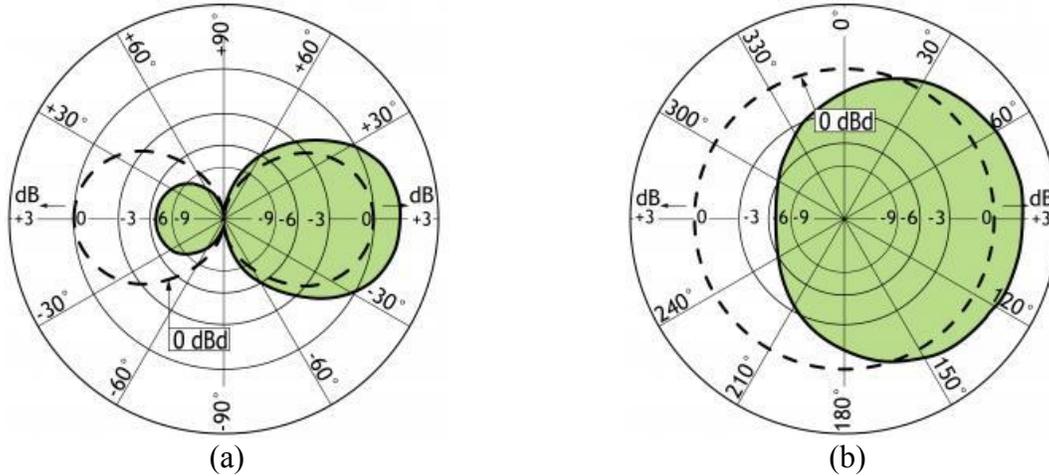


Figure III.3: Radiation pattern in the (a) vertical and (b) horizontal planes for a folded dipole antenna operating at 450 MHz band [105].

b) Radiation in Far-field Region

The far-field region can be defined as the location where the angular field distribution emitted from a radiating object with a non-neglected dimension L is essentially independent of the distance from the antenna. Furthermore, this region is also dominated by radiated fields with \vec{E} and \vec{B} fields orthogonal to each other and the direction of propagation as with plane waves. Considering an antenna with a maximum physical length, L , the far-field region starts at a distance, d , which must satisfy the 2 following conditions, (III.3) and (III.4):

$$d > \frac{2L^2}{\lambda} \quad (III.3)$$

$$d \gg \lambda \quad (III.4)$$

where λ is the wavelength of the radio wave.

From (III.3), it is noticed that large size antennas, such as parabolic or antenna arrays [107]-[108], considerably extends the near-field effects. Conversely, when the antenna size is low enough to be neglected, equation (III.4) prevails over (III.3) and the near-field is larger at low frequencies.

c) Directivity

The antenna directivity is the ratio of the radiation intensity in a given direction from the antenna to the radiation intensity averaged over all directions. It is an important parameter which describes how much more directional an antenna is from a reference source, usually an isotropic radiator. The higher the directivity, the more pointed or directional the antenna pattern is. Directivity, D , can be expressed as:

$$D = \frac{U}{U_0} = 4\pi \frac{U}{P_{rad}} = \frac{4\pi}{\int_0^{2\pi} \int_0^\pi |fn(\theta, \varphi)|^2 \sin\theta \, d\theta \, d\varphi} \quad (\text{III.5})$$

where D is the directivity, U the radiation intensity, U_0 the radiation intensity of isotropic source, P_{rad} the total radiated power and $fn(\theta, \varphi)$ the radiation pattern in spherical coordinates normalized to the isotropic radiation pattern.

d) Efficiency

The efficiency of an antenna is defined as the power delivered to the antenna and the power radiated or dissipated within the antenna. A high efficiency antenna has most of the power available at the antenna input radiated to the environment. A low efficiency antenna has most of the available power absorbed as losses into the antenna, and/or reflected due to impedance mismatch.

The losses associated within an antenna are typically of conduction type (ohmic losses) and dielectric, which depend on the material properties. The radiation efficiency, e_L , can be written as the ratio of the radiated power, P_{rad} , to the input power, P_{IN} , required by the antenna:

$$e_L = \frac{P_{rad}}{P_{IN}} \quad (\text{III.6})$$

e_L evaluates the structural efficiency of an antenna, but it does not take into account the impedance mismatch. For simplicity reasons in measurements, the efficiency of an antenna can be expressed considering also the mismatch losses. This overall efficiency or total efficiency, e_T , is defined as the ratio of P_{rad} to the available power, P_{AV} , at antenna input:

$$e_T = \frac{P_{rad}}{P_{AV}} \quad (III.7)$$

From (II.55), the total efficiency, (III.7), can be rewritten as:

$$e_T = (1 - |\Gamma|^2) \frac{P_{rad}}{P_{IN}} = e_{match} \cdot e_L \quad (III.8)$$

where Γ is the reflection coefficient between the antenna and the receiving or transmitting circuit and e_{match} the matching efficiency of the impedance matching network.

e) Gain

Another useful parameter to evaluate the performance of a given antenna is the gain. It is a measure which takes into account the antenna directional capabilities, 2.1.1.c), as well as its efficiency, 2.1.1.d). Since it provides a complete information about the antenna performances considering its losses, the antenna gain is commonly quoted in a real antenna specification sheet and it can be expressed as:

$$G = e_L \cdot D \quad (III.9)$$

Since the directivity, D , is a normalized expression, it can never theoretically be lower than unit. However, the maximum antenna gain can arbitrary be inferior to 0 dB due to losses or low efficiency, which is usually the case of electrically small antennas. Hence, the gain becomes more attractive to express the antenna performance.

Another important information related with the gain is the aperture angle in a given direction in which an acceptable gain level is maintained. Typically, the angular separation in which the magnitude of the radiation pattern decreases by 50% (or -3dB) is considered. This angle is also known as Half Power Beam Width (HPBW) and it is illustrated in Figure III.4.

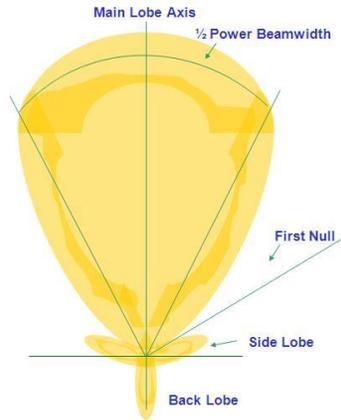


Figure III.4: Representation of the HPBW.

f) Polarization

The polarization of an antenna refers to the electromagnetic field orientation of the radio waves and it is determined by the physical structure and orientation of an antenna.

The polarization of the EM field describes how the direction and magnitude of its vectors, \vec{E} and \vec{H} , at a fixed location in space behave in time. It is considered in theory of antennas that the EM field is polarized in the plane orthogonal to the direction of wave propagation, since this is the plane defined by the vectors at far-field. According to the shape obtained from EM vectors evolution in time, the polarization is classified into three different types: linear, circular and elliptical (e.g., the polarization of a dipole antenna is linear).

If an antenna is attempting to receive a signal from an electromagnetic wave, it must be matched to the polarization of the incoming wave. If the wave is not matched to the receiving antenna, the energy will not be properly detected [100].

This concept is important for antenna to antenna communication. For instance, a horizontally polarized antenna will not communicate with a vertically polarized antenna, due to the reciprocity theorem, which describes that antennas transmit and receive in exactly the same polarization. Hence, a vertically polarized antenna transmits and receives vertically polarized fields.

In general, for two linearly polarized antennas that are rotated from each other by an angle θ , the power loss due to this polarization mismatch will be described by the Polarization Loss Factor (PLF), (III.10).

$$PLF = \cos^2\theta \tag{III.10}$$

In this thesis report, unless otherwise noted, it will be assumed that the EM waves produced by the antennas are properly matched one to each other, communicating at maximum energy transfer in terms of polarization.

2.2 Design of Antennas for 900 MHz and 2.45 GHz

2.2.1 50Ω Antenna

As mentioned in the introduction of this chapter, the topology selected to perform the WPRs is a dipole antenna. This kind of antenna exhibits a good tradeoff between gain and directivity. In addition, the size of dipole antennas is usually smaller than other topologies, which contributes to the miniaturization of devices.

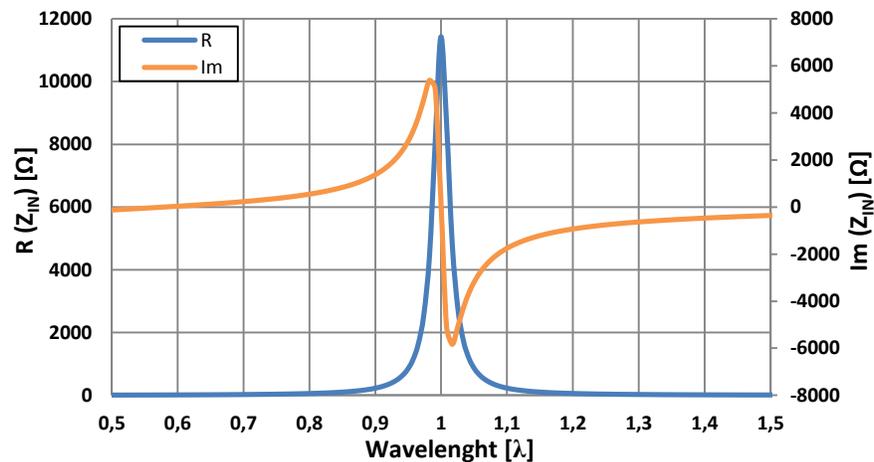


Figure III.5: Standard dipole input impedance as a function of its length.

Considering the dipole input impedance as a function of its length, represented in Figure III.5, it becomes purely resistive at $\frac{\lambda}{2}$ and λ . Although, an antenna with electrical length of λ has good radiation performances, it has a very narrow bandwidth, which limits its range of applications. Therefore, it is not usually designed to operate in this region. It is more convenient to operate at $\frac{\lambda}{2}$, since the variation of imaginary impedance is smoother than the one at λ , thus, providing better results in terms of bandwidth.

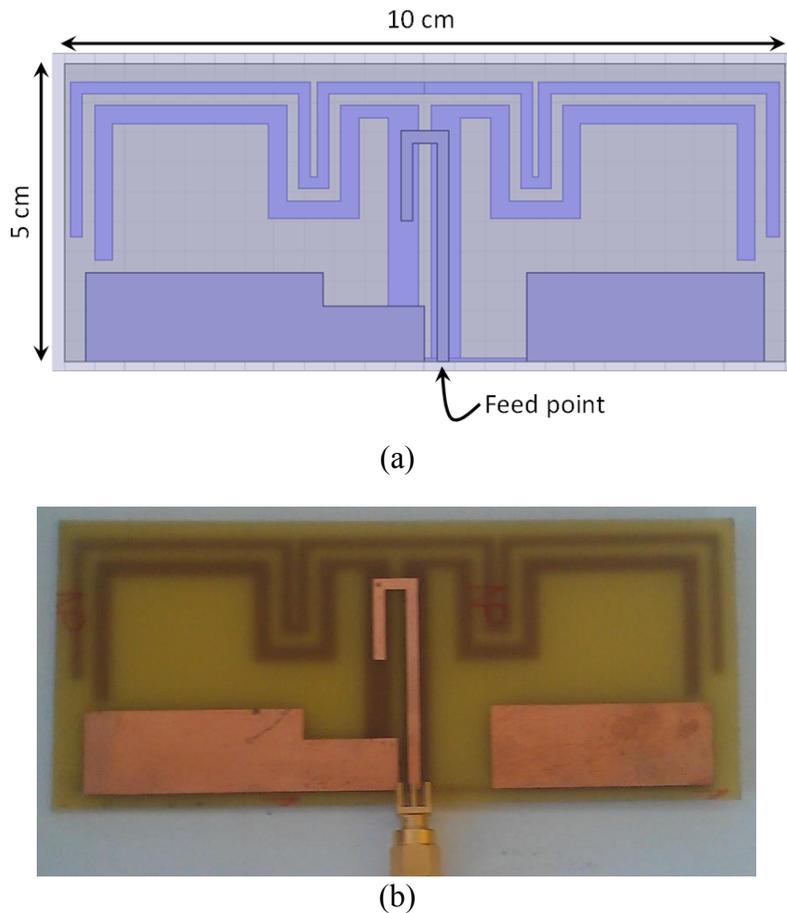


Figure III.6: (a) structure of the proposed 50Ω antenna and (b) the 50Ω antenna fabricated on a FR4 substrate.

In UHF bands, the larger dimension of an antenna can reach a few tens of centimeters. It is a serious drawback for the implementation of compact RF harvesters. To decrease the antenna size, the meandering technique can be used. It consists in folding the arms of a dipole antenna along its path to miniaturize the antenna shape [109]-[111]. Based on microstrip dipole antennas

and applying the meandering technique, the design of the proposed antenna for 50Ω applications is shown in Figure III.6 (a).

The antenna of Figure III.6 (b) is implemented on a 1.6 mm FR4 substrate. The design is performed based on 3D EM simulation with HFSS from Ansoft Designer. Figure III.7 shows the simulated and measured antenna performances.

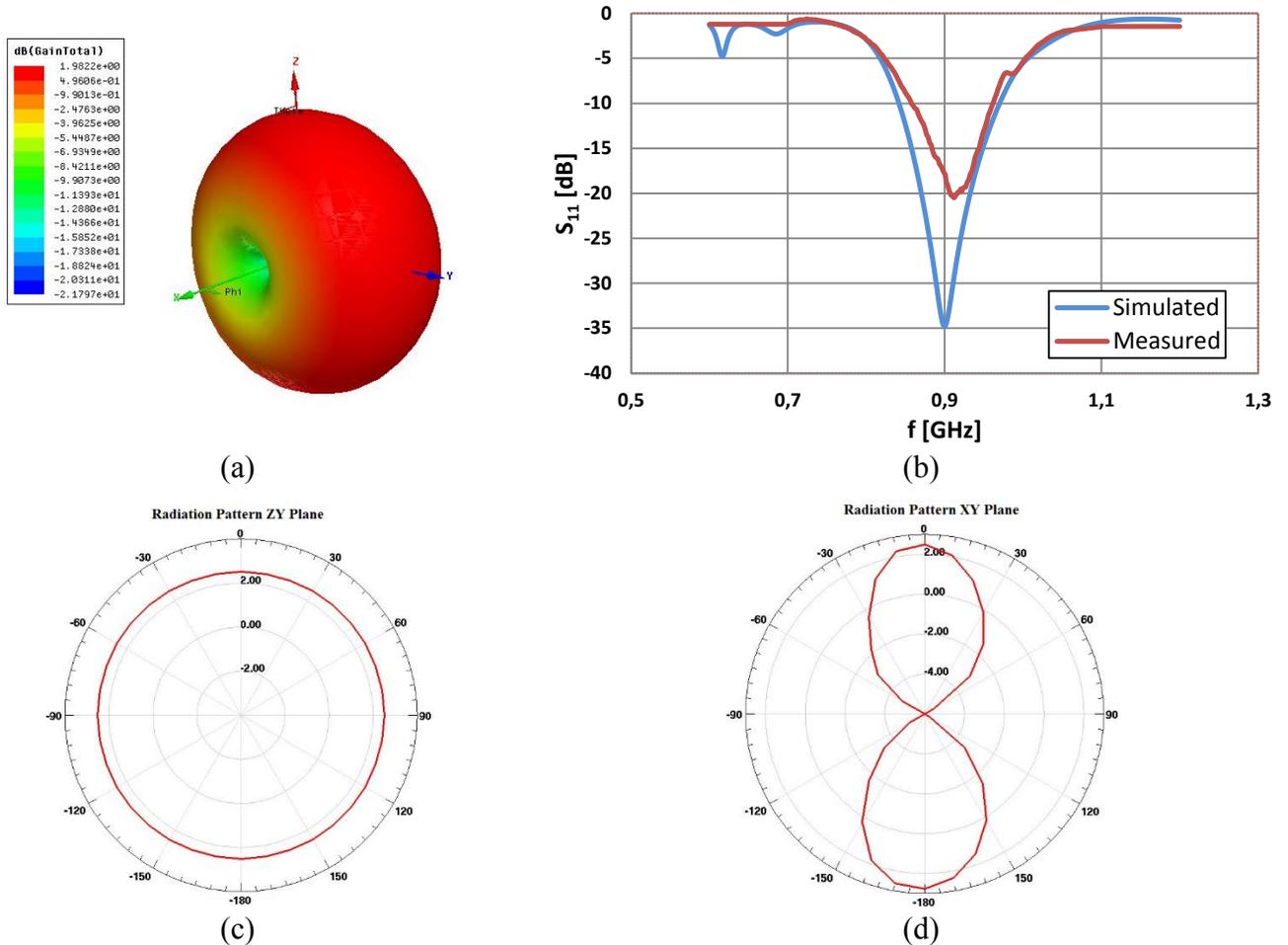


Figure III.7: 50Ω antenna performances: (a) 3D view of the gain, G (b) S_{11} parameter to a 50Ω source (c) (d) radiation pattern to ZY and XY planes.

The measured return loss, S_{11} in Figure III.7 (b), achieves a minimum value of -20 dB at 900 MHz, which is in good agreement with the simulation results. The bandwidth defined at $S_{11} < -10$ dB is of 105 MHz, ranging from 857 MHz to 962 MHz, thus, covering the entire ISM Band.

Analyzing the antenna gain, it is noted that a maximum gain of 2 dBi is reached in the plane perpendicular to the dipole axis, ZY, Figure III.7 (c). The half power beamwidth (HPBW) is of 80° , which gives some flexibility in the space orientation of the WPRs.

2.2.2 Inductive Antennas

To transfer a maximum of collected power to the rectifier, the antenna is assumed to achieve a conjugate matching impedance. As described in Chapter I, the impedance of the voltage multiplier is of capacitive type, which implies the realization of an inductive antenna.

Assuming sinusoidal current distribution, it is possible to estimate analytically the input impedance with simplified equations for some basic geometry antennas (e.g. patch and dipole antennas [100]), which simplifies much the design of an antenna for a given input impedance. However, for an accurate design embedding microstrip lines, this simplified analysis is not sufficient to capture the actual behavior of the device. To address such purpose EM simulations are necessary.

One way to determine the input impedance of inductive antennas is to perform a behavioral study of the input complex impedance as a function of their geometry throughout parametric simulations from an advanced solver based on finite element, integral equation or hybrid methods. This study allows to identify the parameters, which influence most on the active and reactive input impedance and adapt them to properly match the antenna and the IC.

In reference [112], a behavioral analysis based on a microstrip line modeling is presented. This principle is reported for a dipole element. The footprint of the dipole and its equivalent electrical model are proposed in Figure III.8. The lines can be designed to be more inductive or capacitive to present the desired impedance. Figure III.8 (a) and (b) exemplify basic models according to the microstrip line shape. Meandered lines can be designed in order to create coupling capacitors, as shown in Figure III.8 (a). Also, the line width can be modified to add more inductive behavior, as presented in Figure III.8 (b). Both techniques can be employed to modify the antenna impedance and compensate appropriately the reactive behavior in order to match the circuits.

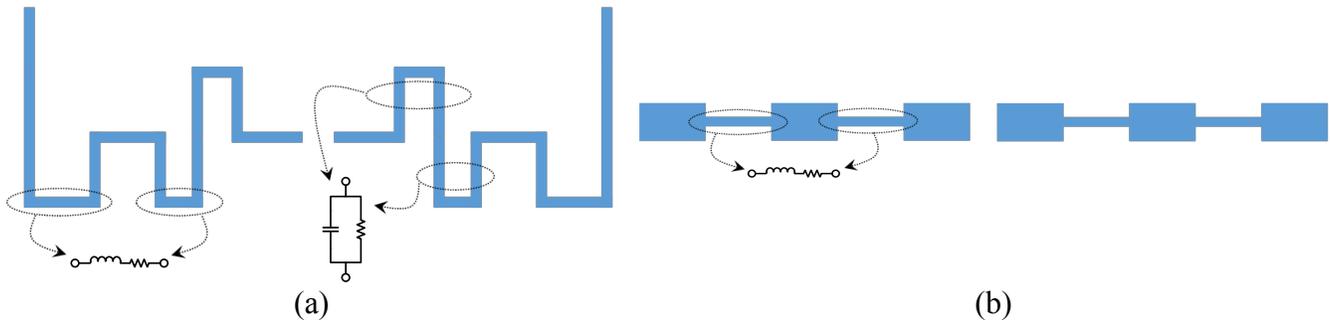


Figure III.8: Equivalent RLC model according to the microstrip line antenna geometry.

Among the different rectifiers implemented and presented in the Chapter II.5, two of them are selected for the demonstration of WPT. The bulk-biased architecture, which exhibits better performances than a traditional topology, and the cross-coupled, which could not be characterized with the probe station. The input impedance of each RF-to-DC converter is reported in TABLE III.1. Since the input impedance of the 5-stage cross-coupled voltage multiplier could not be measured, it is estimated instead with post layout simulation results.

TABLE III.1 Estimated impedances of voltage multipliers to be matched to the inductive antennas taking into account the wire bonding interconnection.

	Impedances	
	900 MHz	2.45 GHz
5s Bulk-biased	46-j473	9-j133
5s Cross-coupled	57-j755	10-j244

The traditional design of dipole antennas does not yield a high reactive and low resistive impedance values, such as the ones presented by low-power rectifiers. When connected to these kind of circuits, the antenna provides poor radiation conditions, resulting in low overall efficiency. Hence, the integration of distributed elements is mandated to increase the reactive part of the impedance with an acceptable efficiency. Several techniques are exposed and discussed in the following sections.

Dipole antenna matched by a series inductive element

Since the rectifier input impedance is highly capacitive, one approach consists in compensate it throughout the implementation of distributed inductive elements in series with the dipole arm. The RLC circuit model of a WPR comprising a series inductive antenna is represented in Figure III.9.

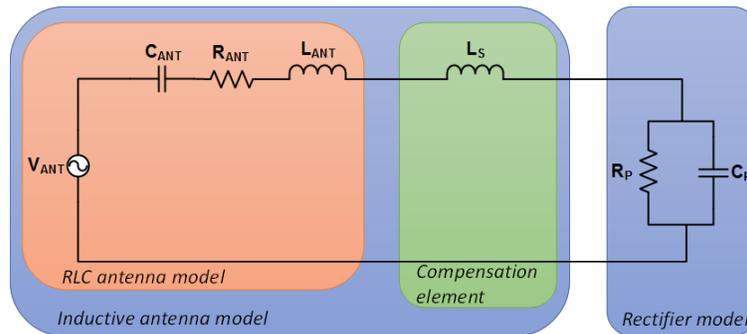


Figure III.9: WPR electrical model implemented with a series inductive antenna.

Figure III.10 is a dipole element including a meandered line in each arm to make up for the capacitive impedance of the RF-to-DC converter. This positive reactance is controlled by the width, W_I , and length, L_I , of the meander path, which also contributes to extend the electrical wave length of the antenna. The size of the dipole is still close to $\frac{\lambda}{2}$.

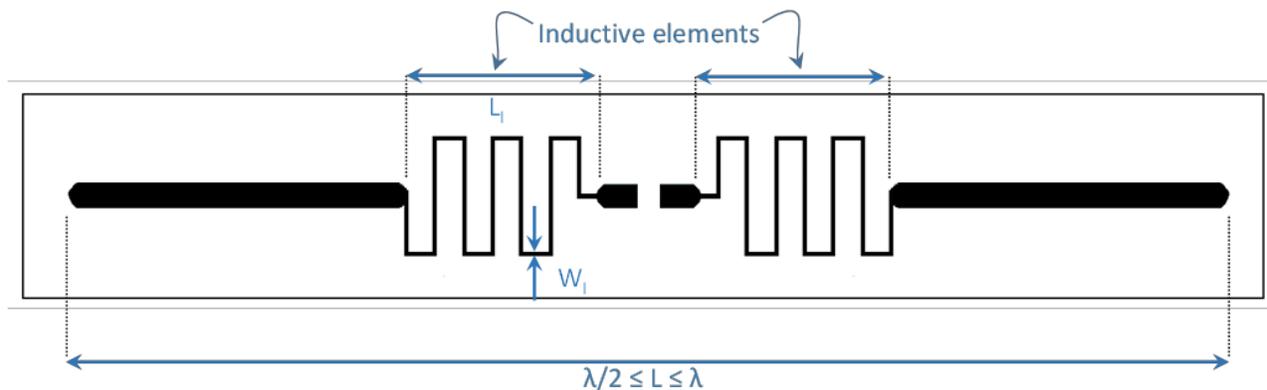


Figure III.10: Inductive antenna geometry using series compensation.

Dipole antenna matched by a parallel inductive element

The capacitance of the rectifier impedance can also be compensated by a shunt distributed inductive element, according to the configuration presented in Figure III.11.

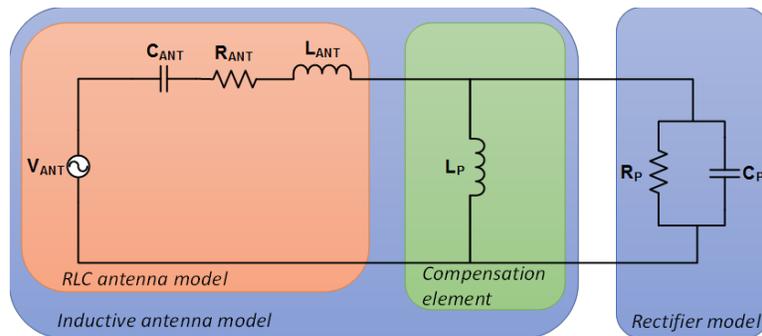


Figure III.11: WPR electrical model implemented with a series inductive antenna.

Unlike the series inductive compensation, proposed in Figure III.9 and illustrated in Figure III.10, the compensation with a shunt element L_P , Figure III.11, does not increase the physical length, L , of the antenna as exemplified in Figure III.12, resulting in antennas larger than series compensation.

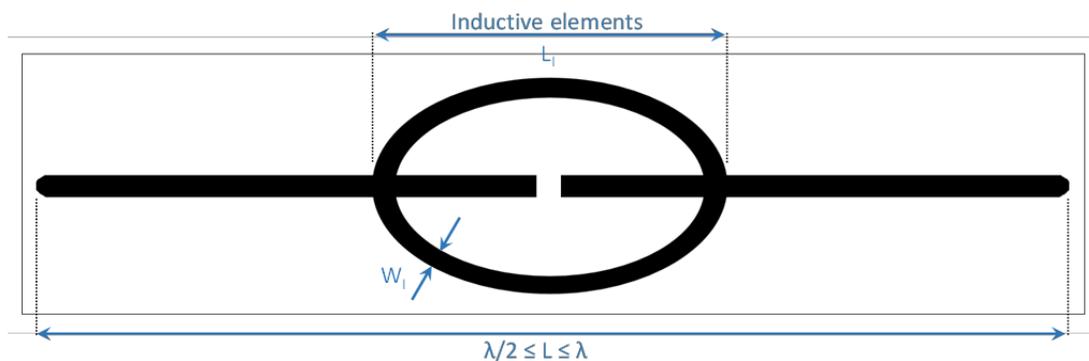


Figure III.12: Inductive antenna geometry using parallel compensation.

However, this technique helps to prevent electrostatic discharges (ESD) due to the short-circuit path connection between the port terminals of the antenna. Therefore, it is commonly used

in some today applications, such as RFID. Furthermore, this loop path added to the antenna can also be designed to resonate at a different frequency, making its use very interesting for dual band applications.

Dipole antenna matched by magnetic coupling

The insertion of a magnetic coupling compensation, Figure III.13, can be seen as a shunt transformer connected in parallel to the conventional dipole antenna.

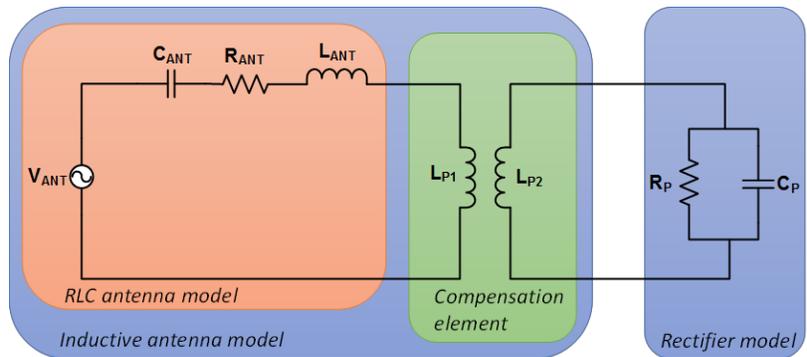
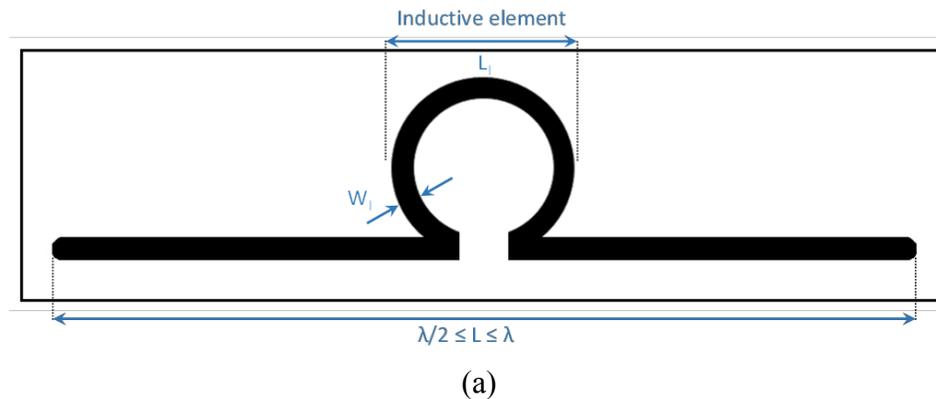


Figure III.13: WPR electrical model implemented with a magnetic coupled antenna.

The electrical energy transferred from one segment to another throughout the magnetic coupling can be designed to behave as an inductive segment, Figure III.14, which electrically separates the dipole antenna to the input terminals of the rectifier.



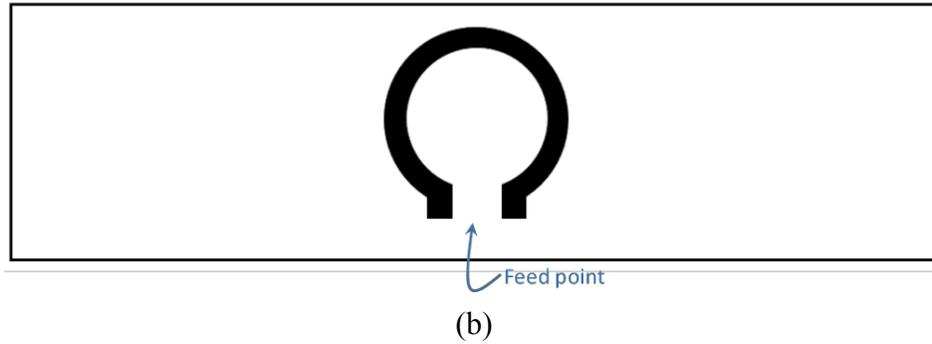


Figure III.14: Inductive antenna geometry using magnetic coupling compensation (a) top (b) bottom view.

This transformation approach gives more design flexibility to achieve the impedance matching both at the antenna and rectifier terminals. However this approach is very sensitive to the misalignment of the inductive element trace. It is also more expensive, as it requires a substrate with two conductive layers.

2.2.3 Inductive antennas at 900 MHz

A previous study on antennas designed for RFID applications compared some of these compensation topologies [113]. It is depicted that several compensation approaches applied to dipole antennas can provide a complex conjugate impedance to some high capacitive circuits, such as the ones commercially found in RFID tags.

Among the different techniques exposed in the previous sections, the series compensation approach has been selected. This solution offers a good tradeoff between the design flexibility, to control the impedance, and the overall size of the antenna.

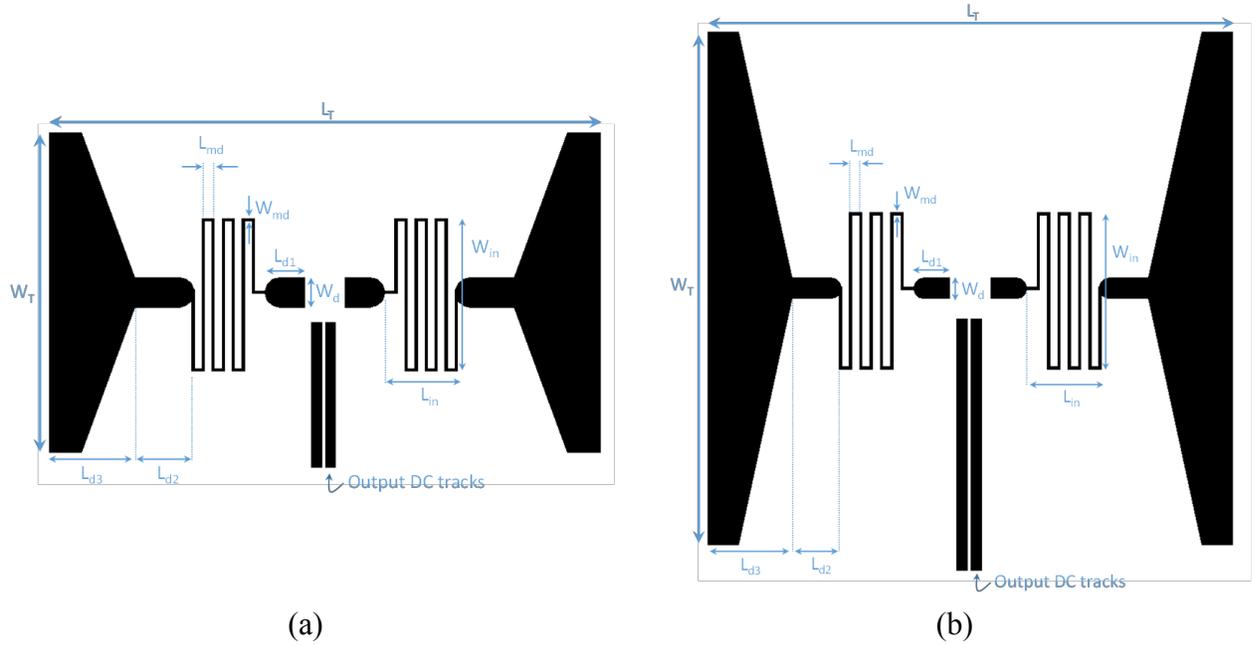


Figure III.15: Structure of the proposed inductive antennas for (a) bulk-biased and (b) cross-coupled voltage multipliers operating at 900 MHz.

The inductive antennas are designed on common FR4 substrate and simulated with HFSS-Ansoft from ANSYS, which analyzes the electromagnetic behavior of the antennas. Figure III.15 illustrates the shape of the antennas, including the design parameters. TABLE III.2 gives the dimension of the featuring elements to tune the antenna impedance to the complex conjugate of the bulk-biased and cross-coupled impedances, reported in TABLE III.1.

TABLE III.2 Measure of inductive antennas.

Circuit to match	Measures [mm]									
	W_T	L_T	W_d	L_{d1}	L_{d2}	L_{d3}	W_{in}	L_{in}	W_{md}	L_{md}
5s Bulk-biased	55	32	3	4	6	8.5	15.25	7	0.25	1.25
5s Cross-coupled	50	51	2	3.5	4.8	8.2	15.25	7	0.25	1.25

The synthesis of an impedance with a low real part and a large imaginary part is challenging. To give more free degree in the design of such element, the width of the last section of the dipole is not constant and looks like a funnel-shaped. The angle of the transition between the sections L_{d2} and L_{d3} , Figure III.15, allows to reduce the real part of the antenna impedance.

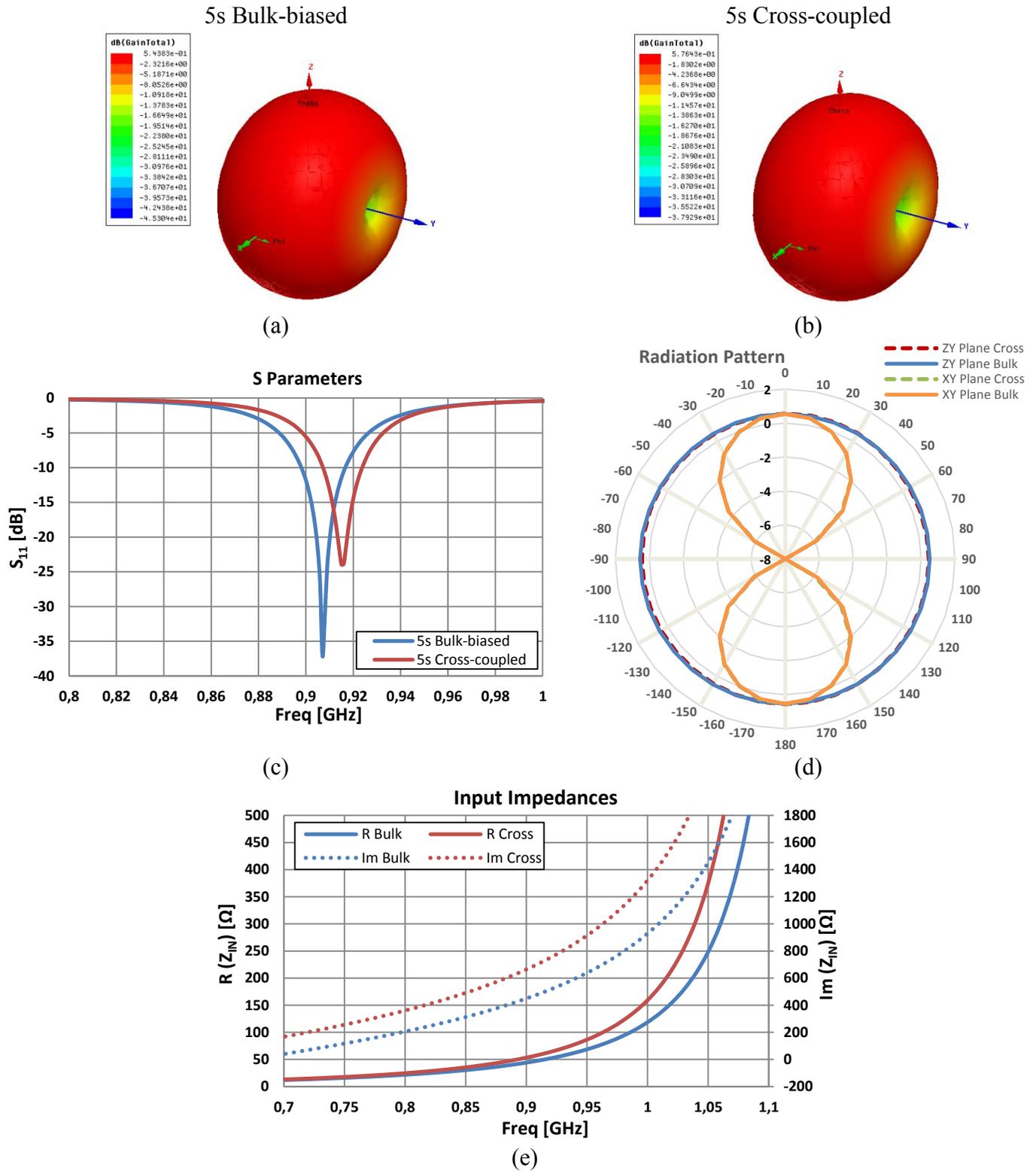


Figure III.16: Inductive antenna performances: (a) (b) 3D view of the gain, G (c) S_{11} parameter to the voltage multiplier impedances (d) radiation pattern to ZY and XY planes (e) the input impedances of the antennas.

As depicted in Figure III.16, the radiation performances of the antennas for both, bulk-biased and cross-coupled compensations are similar. They achieve a gain of approximately 0.5 dBi, Figure III.16 (a) (b), with a half power beam width (HPBW) of 100 degrees, Figure III.16 (d).

As expected the impedance, Figure III.16 (e), is inductive. The complex conjugate of the bulk-biased and cross-coupled input impedances is achieved at 908 MHz and 915 MHz, respectively. The return loss, S_{11} , which is normalized to the complex conjugate impedance of each rectifier, is kept lower than -10 dB from 898 MHz to 918 MHz and from 906 MHz to 925 MHz, respectively.

2.2.4 Inductive antennas at 2.45 GHz

The series compensation technique is also applied to synthesize the complex conjugate of the rectifiers impedance at 2.45 GHz.

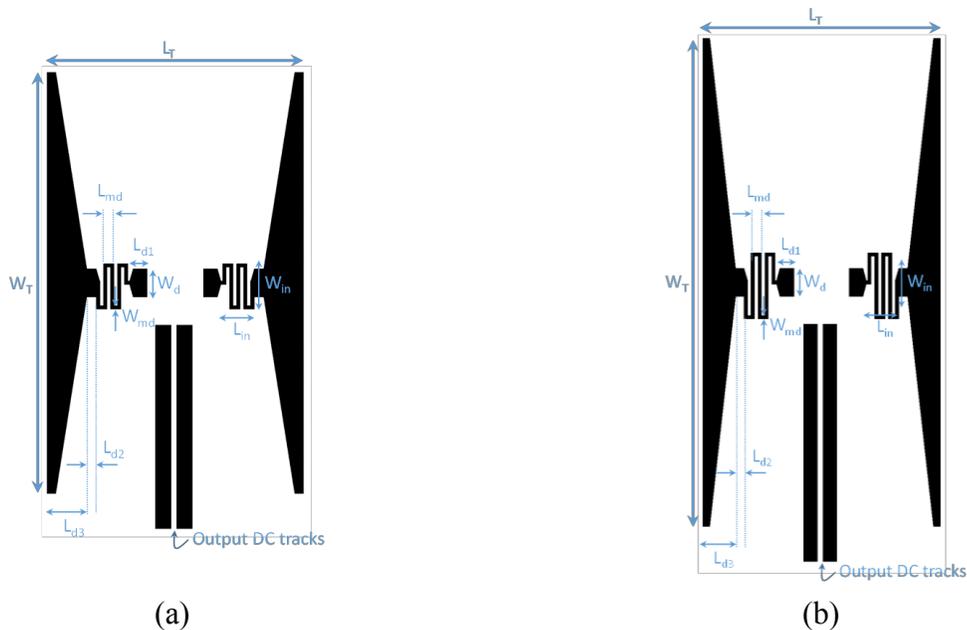


Figure III.17: Structure of the proposed inductive antennas for (a) bulk-biased and (b) cross-coupled voltage multipliers operating at 2.45 GHz.

The shape of the antennas is illustrated in Figure III.17 for the two RF-to-DC converters – i.e. the 5-stage bulk-biased and 5-stage cross-coupled voltage multipliers–. The dimensions are reported in TABLE III.3 and the radiation performances are shown in Figure III.18.

TABLE III.3 Measure of inductive antennas.

Circuit to match	Measures [mm]									
	W_T	L_T	W_d	L_{d1}	L_{d2}	L_{d3}	W_{in}	L_{in}	W_{md}	L_{md}
5s Bulk-biased	30	18	2	1.3	0.95	2.8	3.25	2.25	0.25	0.75
5s Cross-coupled	35	17	2	1.3	0.9	2.4	4.75	2.25	0.25	0.75

The size of the antennas, Table III.3, is smaller at 2.45GHz than 900MHz. As consequences, the performances of the prototype are more sensitive to the fabrication process at higher frequencies. We have access to 2 different types of process: CNC drilling machine and chemical etching method.

The first method uses a drill to remove the copper from the PCB. The imprecision in this method comes on the calibration process performed by a human being, who must calibrate a drill with a precision of 200 nm. The second method counts with a chemical process to corrode the copper, which also presents some inaccuracy to control the corrosion rate and the PCB etching. To deal with these process imprecisions and limitations, the design of antennas are compromised at higher frequencies, such as 2.4 GHz ISM band, thus, restricting the degree of freedom in the dipole transmission lines design.

As detailed in Figure III.18, the antenna radiation performances for both, bulk-biased and cross-coupled, compensations are similar. They achieve a gain of approximately 1.6 dBi, Figure III.18 (a) (b), and a HPBW of 80 degrees, Figure III.18 (d). This designs offer a good tradeoff between the antenna total gain and the directivity.

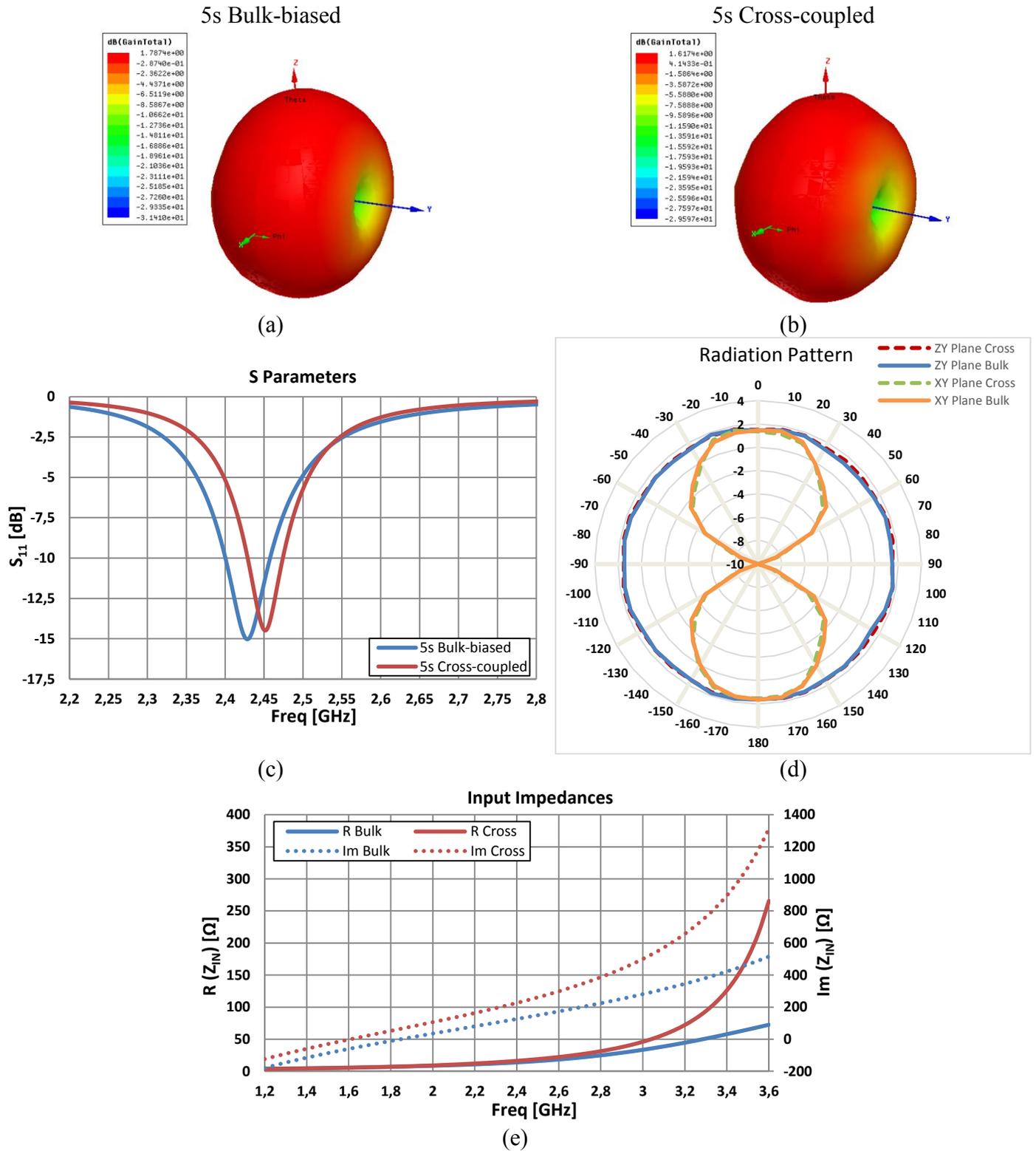


Figure III.18: Inductive antenna performances: (a) (b) 3D view of the gain, G (c) S_{11} parameter to the voltage multiplier impedances (d) radiation pattern to ZY and XY planes (e) the input impedances of the antennas.

Considering the impedance of these 2.4 GHz inductive antennas, Figure III.18 (e), both inductive antennas show the input impedance complex conjugate of the rectifiers to operate into 2.4 GHz ISM band, where they are better matched at approximately 2.45 GHz.

3 Matching Networks

Matching the source and load to the transmission line or waveguide in a general microwave network is necessary to deliver maximum power from the source to the load. In many cases, it is not possible to choose all circuits impedances such that overall matched conditions result. Hence, these situations require that matching networks be used to eliminate the reflections between them, ensuring maximum power transfer condition [114]-[116].

Depending on the application, matching may be required over a band of frequencies, which makes the bandwidth of the matching network an important design parameter. Furthermore, the bandwidth also plays a key role in the system to ensure low levels of power reflections if the load impedance varies over a given range. Otherwise more complex architectures must be employed such as the auto-tuning matching networks.

The matching networks are preferably implemented with reactive components to reduce the losses and the noise penalty. The bandwidth can be of narrow band type or wide band type and a lot of techniques can perform the same impedance at a given frequency [117]-[118]. The quality factor, Q , is an important characteristic of the matching network. For narrowband solutions, it is defined in (III.11) as the ratio between the stored energy at the resonant frequency, and the average power dissipated in the network.

$$Q = \omega_0 \frac{\text{energy stored}}{\text{average power dissipated}} \quad (\text{III.11})$$

3.1 RLC Matching circuits

The principle of narrow band matching aims the synthesis of complex conjugate impedance throughout the insertion of LC elements in order to deliver a maximum power from the source to the load. This situation can be represented as a simple series RLC circuit, Figure III.19.

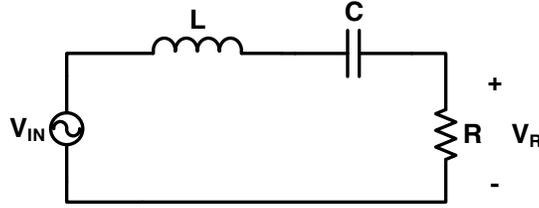


Figure III.19: RLC model for matching circuits.

To analyze the frequency response of the RLC circuits proposed in Figure III.19, the magnitude of the transfer function $\frac{V_R}{V_{IN}}$ is first driven in (III.12).

$$H(\omega) \equiv \frac{V_R}{V_{IN}} = \frac{\omega RC}{\omega RC + j(\omega^2 LC - 1)} \quad (\text{III.12})$$

The maximum power transfer occurs when the magnitude of $H(\omega)$ is unitary. It takes place at the resonant pulsation, ω_0 , defined in (III.13), for the circuit of Figure III.19.

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (\text{III.13})$$

The bandwidth of this network is defined by the frequencies which correspond to an attenuation of $\frac{1}{\sqrt{2}}$ or -3 dB in decibels. This situation is described in (III.14), and the solutions are ω_1 and ω_2 , defined in (III.15) and (III.16), considering the behavior of the matching network at frequencies slightly displaced from resonance, $\omega = \omega_0 \pm \Delta\omega$. ω_1 represents the lower limit and ω_2 the upper limit of the -3 dB bandwidth.

$$\frac{1}{\sqrt{2}} = \frac{\omega RC}{\omega RC + j(\omega^2 LC - 1)} \quad (\text{III.14})$$

$$\omega_1 = -\frac{R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 + \frac{1}{\omega_0^2}} \quad (\text{III.15})$$

$$\omega_2 = \frac{R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 + \frac{1}{\omega_0^2}} \quad (\text{III.16})$$

By combining equations (III.11), (III.15) and (III.16), the relation between the quality factor, Q , bandwidth, BW , and center frequency, ω_0 , can be written as:

$$\frac{BW}{\omega_0} = \frac{1}{Q} \quad (\text{III.17})$$

where we can notice that the bandwidth is inversely proportional to the Q factor. Figure III.20 shows the bandwidth behavior as a function of the Q factor. For a given resonant frequency, a higher Q implies in a narrower bandwidth, and a network more sensitive to the parasitics and fabrication process.

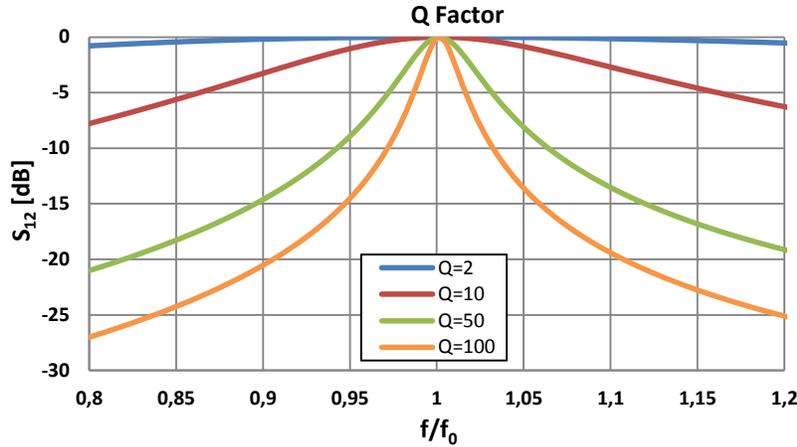


Figure III.20: Bandwidth as a function of Q factor.

Recalling the series-parallel impedance transformation using a LC network [119], the source and load impedances can be matched or “transformed” according to (III.18), where it may also be deduced that the quality factor, Q , can be estimated as (III.19).

$$R_{load} = (1 + Q^2)R_{source} \quad (\text{III.18})$$

$$Q = \sqrt{\frac{R_{load}}{R_{source}}} - 1 \approx \frac{V_{OUT}}{V_{IN}} \quad (\text{III.19})$$

3.2 Matching Network Topologies

There are three basic matching networks used in RF designs: L, Π and T configurations. Each presents some advantages and drawbacks according to the applications.

3.2.1 L-Section Match

The L-section is the simplest network to achieve any impedance in the smith chart. Thus, it is able to present the complex conjugate of any load impedance. Figure III.21 illustrates the regions covered by different combinations of L-section elements.

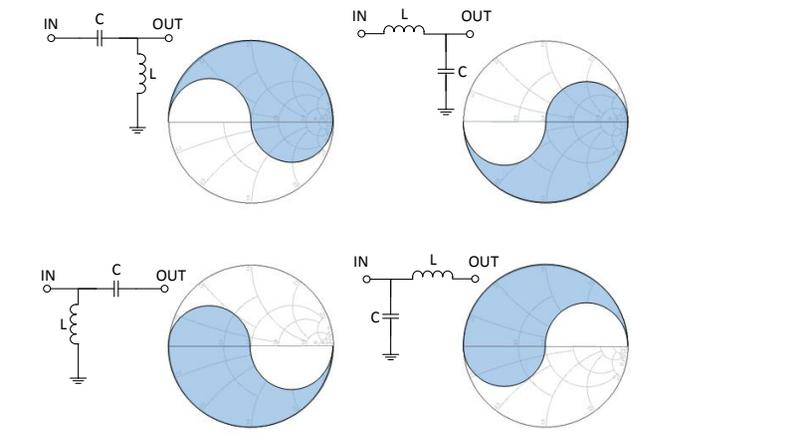


Figure III.21: Regions of impedance covered by L-section match

This approach offers only two degrees of freedom through the choice of L and C . Hence, once the impedance transformation ratio and resonant frequency have been specified, the quality factor, Q , is imposed. If a different value of Q is desired, a network which offers more degrees of freedom is needed. The following sections expose some of these solutions.

3.2.2 Π -Section Match

The π -network can be seen as a combination of 3 reactive elements, which provides a tuning with 3 degrees of freedom. The most convenient approach to analyze this matching network is to consider it as a cascade of two L-sections, as illustrated in Figure III.22. The last two elements brings the output impedance to an intermediary impedance, Z_{INTER} in Figure III.22 (b), which is lower than the source impedance. Z_{INTER} becomes the complex conjugate of the input impedance throughout another L-section stage.

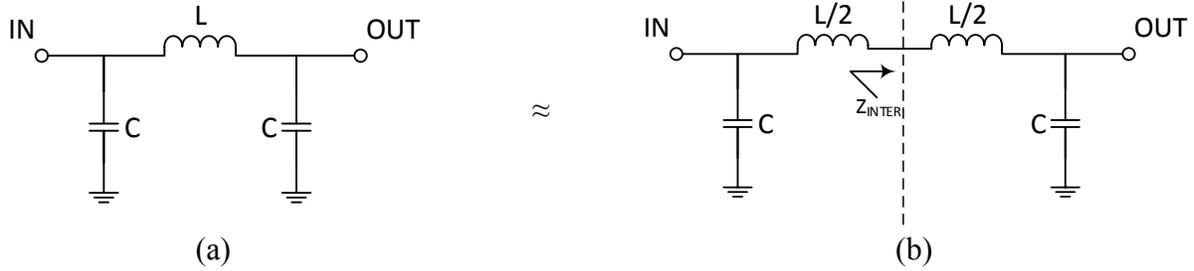


Figure III.22: Π -section matching network.

3.2.3 T-Section Match

The T-section matching circuit, illustrated in Figure III.23 (a), also provides a third degree of freedom in the impedance transformation. Likewise the π -section in Figure III.22, the T-section can be analyzed as the cascade of two L-sections according the Figure III.23 (b). However, in the T-section case, the combination of L-sections are connected to each other inversely, where the intermediary impedance is placed between shunt elements, instead of series ones as in the Π -section network.

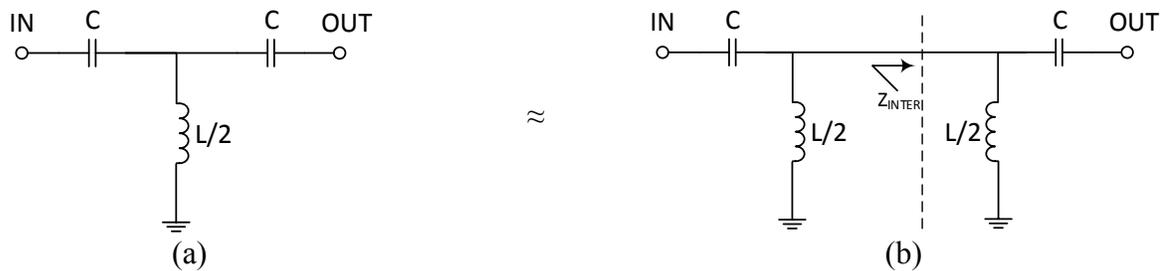


Figure III.23: T-section matching network.

3.3 Matching Network Design

As discussed in the previous sections, the matching network, of narrow band type, can be analyzed as a cascade of multiple L-sections. The characteristics considered in the synthesis of such a network are: the Q factor and bandwidth, which are related to the desired frequency band and source to load impedances transformation.

The TABLE III.4 summarizes the estimated voltage multiplier impedances taking into account the QFN packaging. This evaluation is performed throughout an EM simulation in ADS momentum considering the 3D structure of QFN and wire bonding insertion.

TABLE III.4 Voltage multipliers input impedance taking into account QFN packaging and wire bonding insertion.

	3-stage Traditional		3-stage Bulk		5-stage Bulk	
	900 MHz	2.4 GHz	900 MHz	2.4 GHz	900 MHz	2.4 GHz
$Z_{IN-Rectifiers} [\Omega]$	70-j825	12-j311	55-j816	9-j308	70-j613	12-j233
$Z_{IN-QFN} [\Omega]$	45-j600	6.8-j210	36-j598	5.2-j209	36.5-j466	5.86-j162
$R_P [k\Omega]$	8	6.5	10	8.5	6	4.5
$C_P [fF]$	293	315	295	316	377	408
$Q [50\Omega]$	12.6	11.3	14.1	13	10.9	9.43

The quality factor, Q , is estimated based on a 50Ω impedance matching. According to TABLE III.4, it ranges from 10 to 14 with the frequency and rectifier topology. These large Q imply selective matching networks. The main issue concerns the impedance mismatch occurring with the variations of fabrication process and device values. To ensure an acceptable return loss S_{11} , several L-sections are cascaded to achieve the impedance transformation. However increasing the number of devices yields more losses. To address the trade-off between robustness and performances, a configuration with a T-section combined with an L-section, equivalent to 3 L-sections, is selected.

3.3.1 Matching the rectifiers impedances at 900 and 2.4 GHz

The capacitive nature of MOS based diodes makes the input impedance of the rectifiers close to the open circuit region. Impedances located in this region, in most cases, impairs a good match with the antenna.

Our case of study is the matching of an n-stage rectifier, Z_{IN} , to a 50Ω antenna, Z_{ANT} , with the combination of a T-section and an L-section. The transformation of Z_{IN} into Z_{ANT} , Figure

III.24 (a), takes 5 branches in the Smith chart. The length of each path is short, which reduces the impact of device mismatch and process variation on the impedance transformation. A single L-section would perform the same transformation with only two long branches, but it would be very sensitive to any variation.

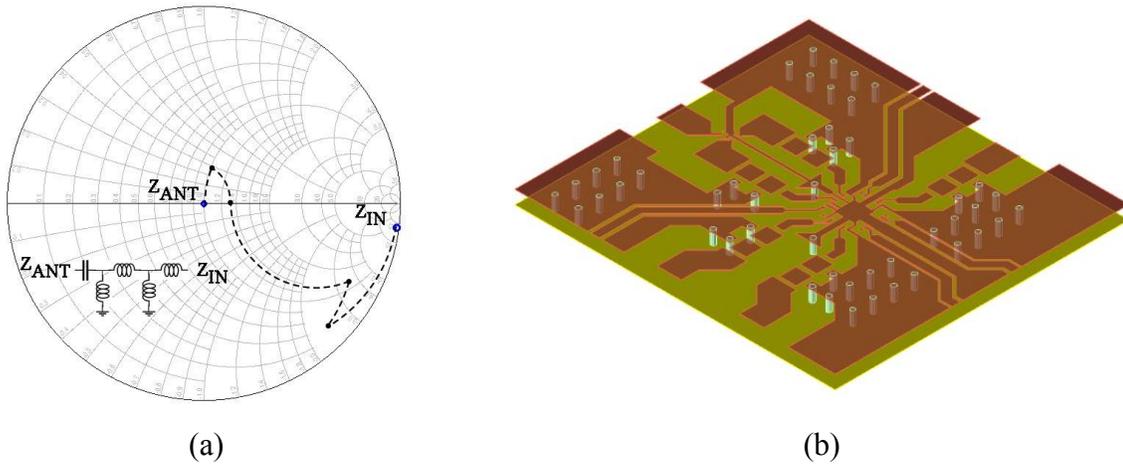


Figure III.24: (a) Matching network diagram, (b) 3D view of the PCB structure.

The T-section is first connected to the voltage multiplier input to absorb the capacitive input impedance presented by the rectifiers and also to regrowth the real part of the impedance. The last L-section further increase the real part to match it to 50Ω .

Figure III.24 (b) shows the PCB structure adopted to implement the matching networks and to mount the packaged voltage multipliers. Electromagnetic (EM) simulations were accomplished using ADS Momentum to evaluate the matching structure influence on the impedance, increasing its exactitude. A co-simulation approach for system-level analysis was also performed using the COTS devices from muRata design kit with the 3D structure model. The S-parameters evaluation of the matching network block is shown in Figure III.25 for both operating frequencies, taking into account the estimated impedances of the packaged rectifiers shown in TABLE III.4.

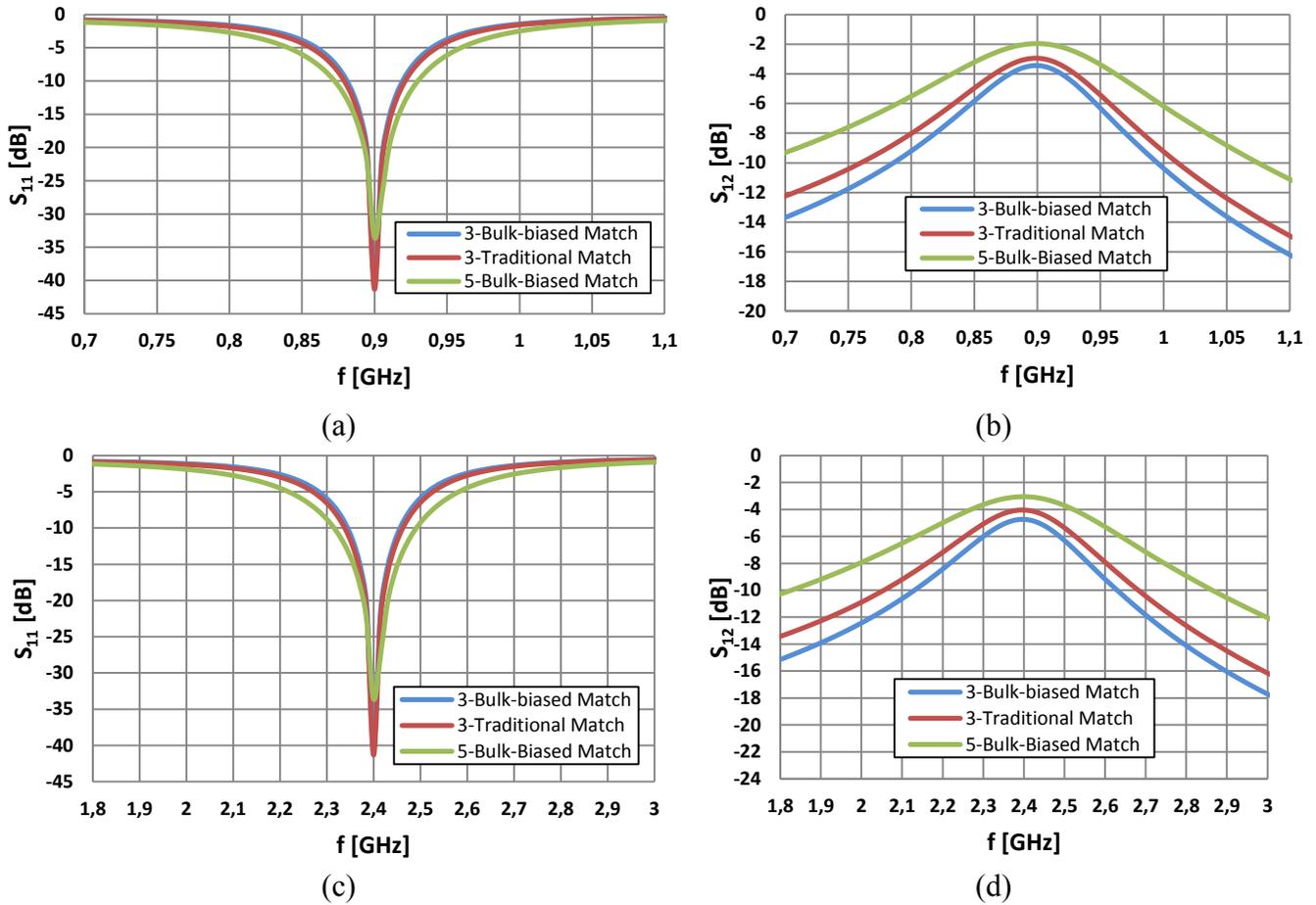


Figure III.25: Simulation results of PCB return loss, S_{11} , at 900 MHz (a) and 2.4 GHz (c), attenuation S_{21} at 900 MHz (b) and 2.4 GHz (d).

The six circuits exhibit a low return loss. The S_{11} , Figure III.25 (a) (c), is lower than -30 dB for all configurations. The power losses, S_{21} , are, in the worst case, close to 3.5 dB at 900 MHz, Figure III.25 (b), and 5 dB at 2.4GHz, Figure III.25 (d). Most of the 1.5 dB additional loss at 2.4GHz comes from the substrate. Indeed, the performances of 1.6 mm FR4 start to degrade substantially above 1GHz. This difference impacts directly in the sensitivity of the WPRs.

4 Wireless Powered Receivers at 900 MHz and 2.45 GHz

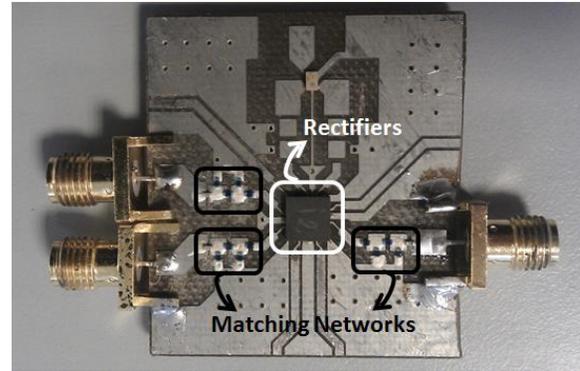
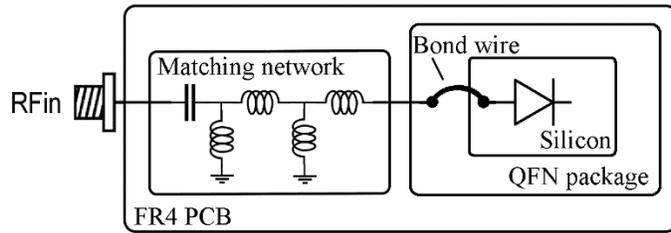
In this last section the remote powering of the assembled RF harvesters is presented and discussed. The different rectifiers designed and prototyped in a standard 130 nm CMOS technology, discussed in Chapter II.5, are implemented according to two different scenarios of WPRs:

- With a $50\ \Omega$ antenna at 900 MHz and 2.4 GHz, discussed in sections III.4.1 and III.4.2,
- With an antenna directly matched to the complex conjugate of the circuit impedance at 900 MHz and 2.4 GHz, discussed in the section III.4.3.

The antennas and the matching networks used in these systems are those presented at the beginning of this chapter, sections III.2 and III.3, respectively. First, only the systems comprising the matching network and the rectifiers are measured, section III.4.1, in order to evaluate the overall losses, especially the matching network and QFN package losses. Afterwards, they are connected to the $50\ \Omega$ antenna, III.2.2.1, and then the entire wireless powered receivers are characterized over the distances, section III.4.2. Finally, section III.4.3, presents experimental results with the inductive antennas directly wire bonded to the rectifiers complex conjugate impedance on a FR4 substrate.

4.1 Wireless powered module - Setup 1: Matching Networks and Rectifiers at 900MHz and 2.45 GHz

A schematic of the proposed Wireless Powered Receivers (WPR) for the first measurement setup is shown in Figure III.26 (a). The circuits prototyped in a 130nm standard CMOS process and discussed in Chapter II.5 are wire-bonded to a QFN package and mounted on a FR4 printed circuit board in order to measure a system level comprising the rectifiers and matching networks. A WPR prototype is presented in Figure III.26 (b). To measure the modules, a Vector Network Analyzer 8720D from Agilent and a multimeter 34401A from HP are used to work out the return loss and the rectified voltage, as presented in Figure III.27.



(a)

(b)

Figure III.26: a) WPRs schematic, b) WPR modules on a FR4 PCB.

The matching network blocks were designed to match the rectifiers impedance to 50Ω at 900 MHz and 2.4 GHz. The inaccuracy of bonding wire lengths, modeling of packaging modules and accuracy in PCB fabrication shift the impedance matching up to 910 MHz and down to 2.3 GHz at 900 MHz and 2.4 GHz design, respectively, as illustrated in Figure III.28 (a) and (b). These shift values of 10 MHz and 100 MHz represents a variation of approximately 1% and 4% at 900 MHz and 2.4 GHz frequencies, which are acceptable with respect to the accuracy of the fabrication process.

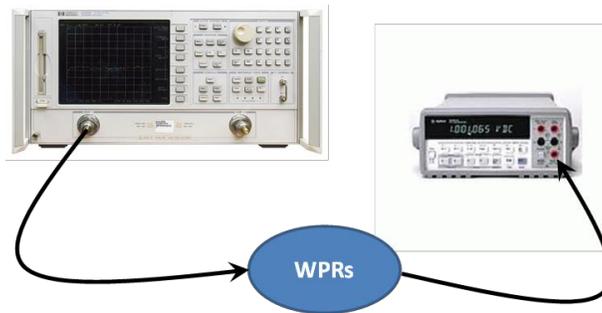


Figure III.27: Measurement setup.

The measurement results of the WPRs are presented in Figure III.28, Figure III.29 and Figure III.30. The measured output DC voltage, V_{OUT} , as a function of the available input power, P_{RF} , for different load resistances is reported in Figure III.29. It figures out that the sensitivity of WPRs exploiting the bulk-biased technique is increased compared to the traditional topology. To deliver an output power of $3.6 \mu W$, the bulk-biased WPR needs an available input power, P_{RF} , of $-17.3 \text{ dBm}@900 \text{ MHz}$ / $-15.8 \text{ dBm}@2.4 \text{ GHz}$ to drive a $400 \text{ k}\Omega$ load at 1.2 V, whereas the

traditional WPR requires $-16.4 \text{ dBm}@900 \text{ MHz}$ / $-14.8 \text{ dBm}@2.4 \text{ GHz}$, which is an improvement of about 1 dB in sensitivity.

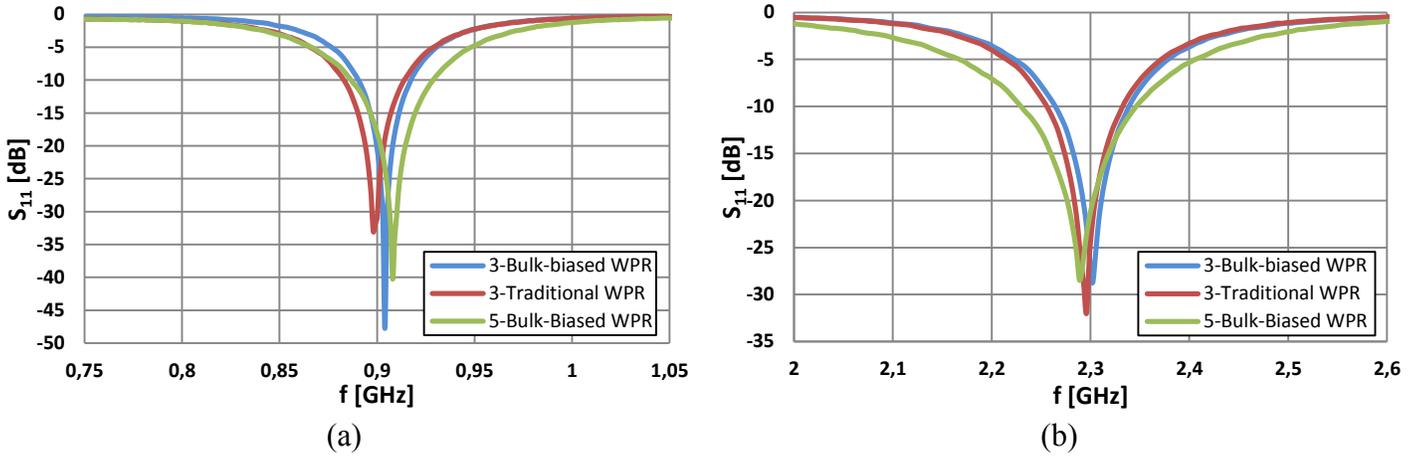
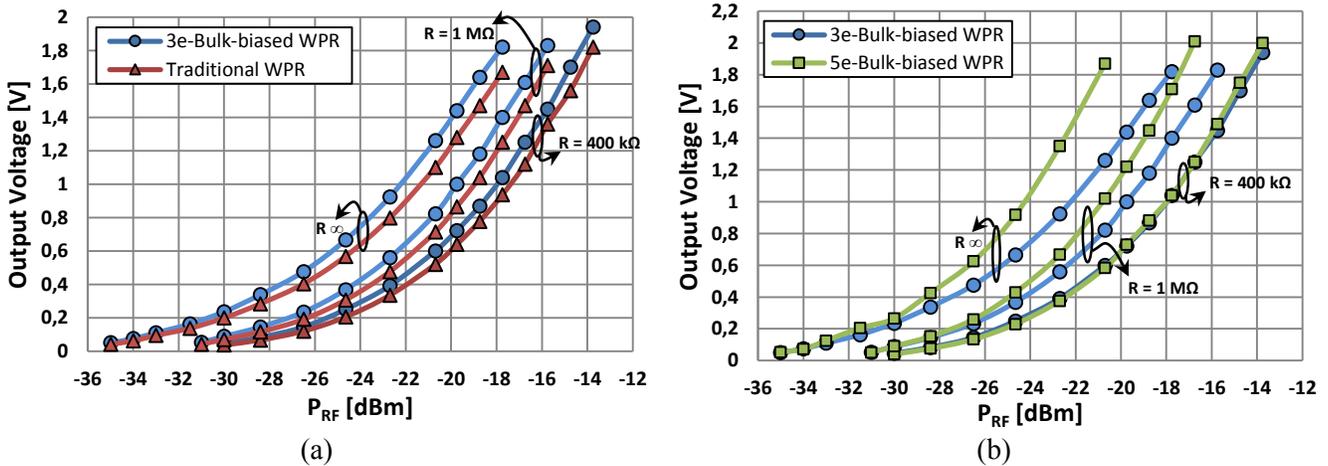


Figure III.28: Measured S_{11} parameter of WPRs operating within specification design at (a) 900 MHz and (b) 2.4 GHz.

Comparing the sensitivity of the rectifiers in both, 900 MHz and 2.4 GHz, operating frequencies, the bulk-biased topology with 3-stages improves it in approximately 1.5 dB compared to the conventional architecture, according to TABLE II.5. However, analyzing the sensitivity of the WPRs using these rectifier architectures, it only shows an improvement of 1 dB. This difference of 0.5 dB comes from the additional loss of the matching network for the bulk-biased circuit, as discussed in section III.3.



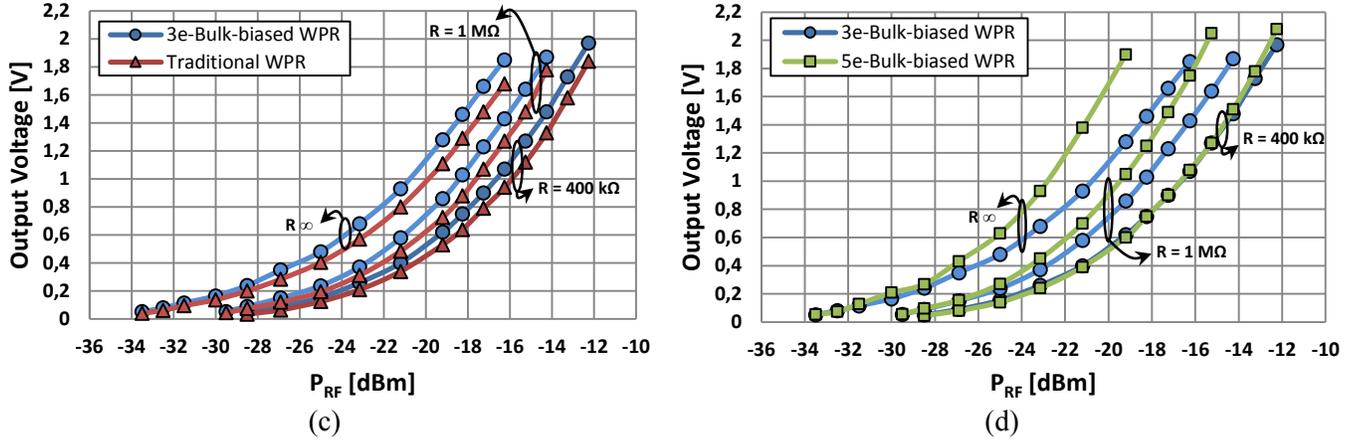


Figure III.29: Measured output voltage as a function of the available input power at (a) (b) 900 MHz and (c) (d) 2.4 GHz.

Loaded with a 1 M Ω resistance, the circuits deliver a nominal output voltage of 1.2 V for an available input power, P_{RF} , of -18.8 dBm@900 MHz / -17.3 dBm@2.4 GHz for the 3-stage bulk-biased circuit, and -17.8 dBm@900 MHz / -16.3 dBm@2.4 GHz for the 3-stage traditional topology, whereas the 5-stage architecture requires only -20 dBm@900 MHz / -18.5 dBm@2.4 GHz, which is in accordance with the theory. The topologies employing more stages have a higher sensitivity for lower current loads.

As discussed in Chapter I.3.1 and stated in (I.10), the efficiency is the ratio between the different power levels evaluated at the output and input of a block. For instance, the voltage multipliers are estimated considering the provided DC power at its output and the average power available at its input, as previous stated in equation (II.16) and discussed in Chapter II.4.2.

To evaluate the power conversion efficiency of the wireless powered modules, different power levels are considered for its analytic estimation. As illustrated in Figure II.1, the powers concerned for the WPRs characterization are the effective power delivered to the matching network input, P_{RF} , and the power available electromagnetically at the antenna input, P_{AV} . Therefore, the WPR overall efficiencies can be expressed as:

$$\eta_{RF} = \frac{P_{OUT}}{P_{RF}} \quad (III.20)$$

$$\eta_{AV} = \frac{P_{OUT}}{P_{AV}} \quad (III.21)$$

These overall PCEs then take into account the consumption of the circuits concerned and also the mismatch losses between the different blocks. Thus, given a more realistic estimation of the WPR performances.

The WPRs power efficiency, η_{RF} , as a function of the available input power is presented in Figure III.30 for different load conditions. Under the design specifications to supply 1.2 V for a 400 k Ω load, the circuits reaches up to 18.5% and 15.5% for bulk-biased and traditional harvesters, respectively.

The losses introduced by the matching network and the substrate significantly contribute to lower the overall power efficiency of the harvesting modules.

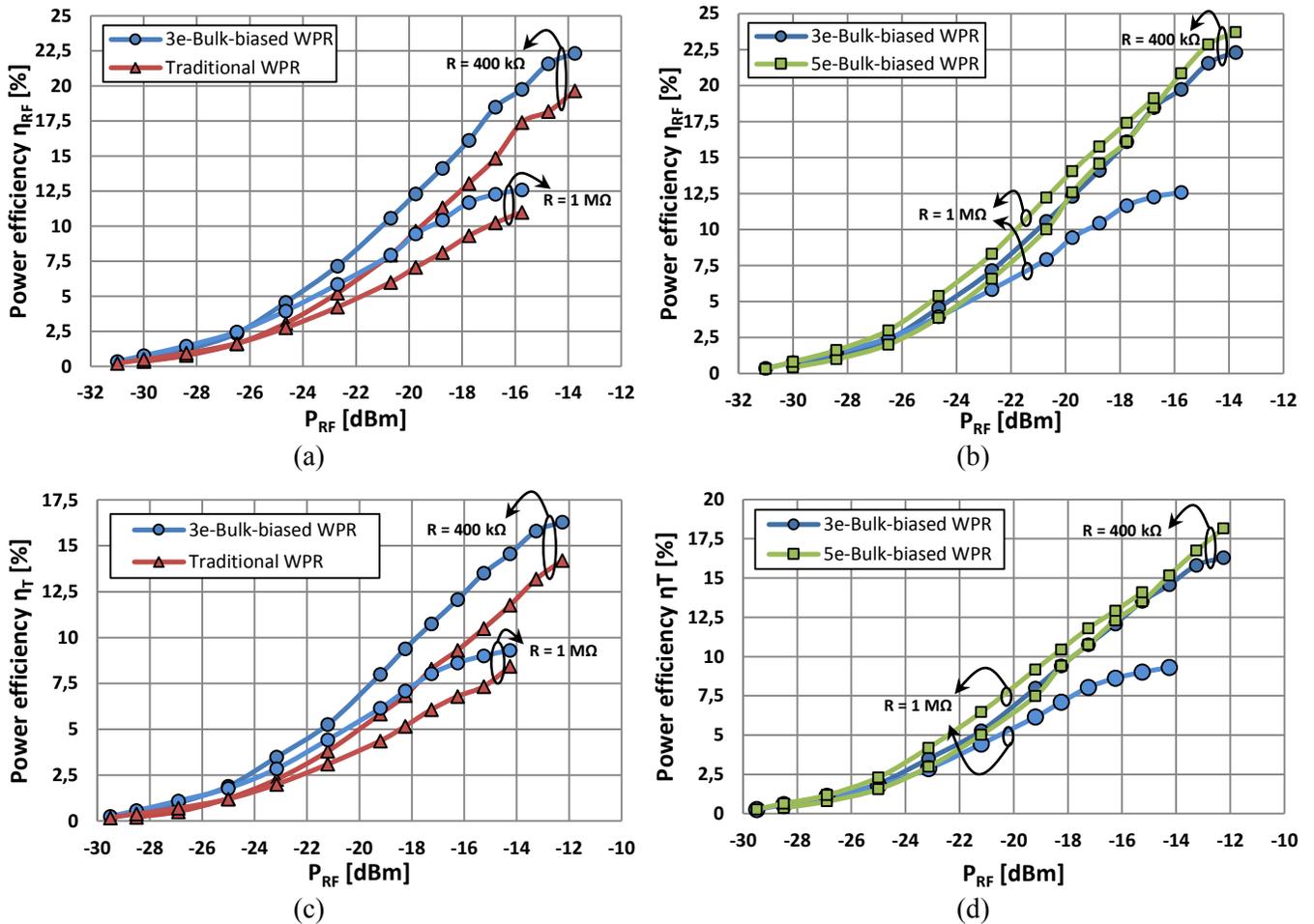


Figure III.30: Overall power efficiency as a function of input RF power at (a) (b) 900 MHz and (c) (d) 2.4 GHz.

The efficiency of rectification decreases with the number of stages, due to the increase of losses. The measurement, and simulation, results of the rectifiers figure out the 3-stage bulk biased WPR exhibit better performances than the 5 stage configuration.

However, it is noticed in Figure III.29 (b) (d) and Figure III.30 (b) (d) the overall efficiency of the 3-stage and 5-stage bulk biased WPRs are similar with the optimized load of 400 kΩ. The reason for this difference in the efficiency behavior at system level and in the rectifier circuit comes from the matching network. Indeed, the impedance presented by the 3-stage rectifier is more difficult to match to 50 Ω than the 5-stage rectifier, with a combination of a T-section and an L-section. This result highlights the overall efficiency of a WPR is a tradeoff between the rectifier efficiency and the losses of the 50 Ω matching network, as discussed in [120].

TABLE III.5 summarizes the results obtained with a probe station and with the PCBs for the optimized load: 1.2 V / 400 kΩ. Neglecting the losses caused by the matching networks and packaging, it is depicted that the bulk biased technique significantly improves the efficiency of RF-to-DC conversion with 51% for the 3-stage bulk biased, and only 34% for the 3-stage in a traditional configuration. These results are pretty much similar to the ones obtained with the probe station.

TABLE III.5 Measurement results of different voltage multiplier at 2.4 GHz for a fixed output power of 3.6 μW.

	PCB			Insertion Losses		Probe station	
	P _{RF} [dBm]	η [%]	η _{WL} [%]	Matching [dB]	QFN [dB]	P _{IN} [dBm]	η [%]
3s Traditional	-14.8	11	34	4	1	-19.5	33
3s Bulk	-15.8	13.7	51	4.7	1	-21.7	54
5s Bulk	-15.8	13.7	36	3.1	1	-20.2	38

4.2 Wireless powered module - Setup 2: 50 Ω Antenna, Matching Network and Rectifiers at 900 MHz

The WPR modules operating at 2.4 GHz were planned to be measured with an available commercial grade 2.4 GHz whip antenna. Unfortunately the return loss of this antenna, reported in Figure III.31, does not cover the 50 Ω input bandwidth of the 2.4 GHz harvesters, which are actually centered at 2.3 GHz, as depicted in Figure III.28 (b). For this reason, the WPRs operating at this frequency are not presented in this section for the 50 Ω matching case and are further analyzed in III.4.3 with the integration of inductive antennas.

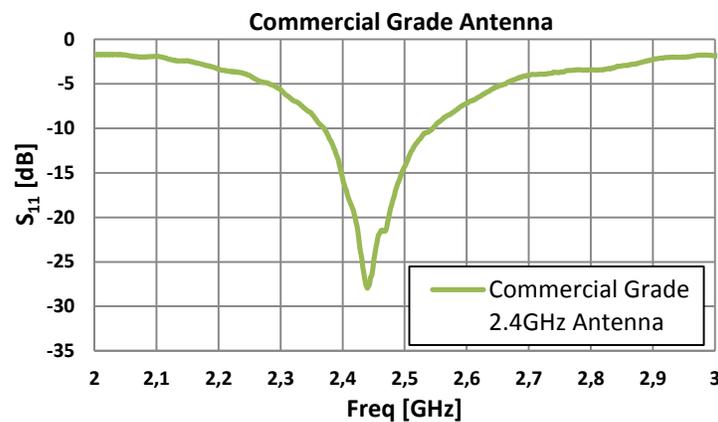


Figure III.31: Commercial grade 2.4 GHz antenna performances.

At 900 MHz, a custom antenna was carried out as described in section III.2.2.1. This meandered dipole, Figure III.6, exhibits a wide bandwidth, the S_{11} is lower than -10 dB from 855 MHz to 960 MHz, which properly matches the input impedance of the RF harvester modules from 880 MHz to 930 MHz.

To test the overall performance of the RF wireless energy receivers, the custom antenna operating in 900 MHz ISM band is connected to the RF harvester modules, as shown in Figure III.33 (a).

The Wireless Energy / Power Transmission (WE/PT) setup for the experimental results is shown in Figure III.32. The RF transmitter is built with an HP/Agilent 8665A RF signal generator attached to a similar 50 Ω antenna used in the WPR modules. Accounting for the antenna gain and connection losses, this RF transmitter is able to radiate a maximum power of 27 dBm EIRP.

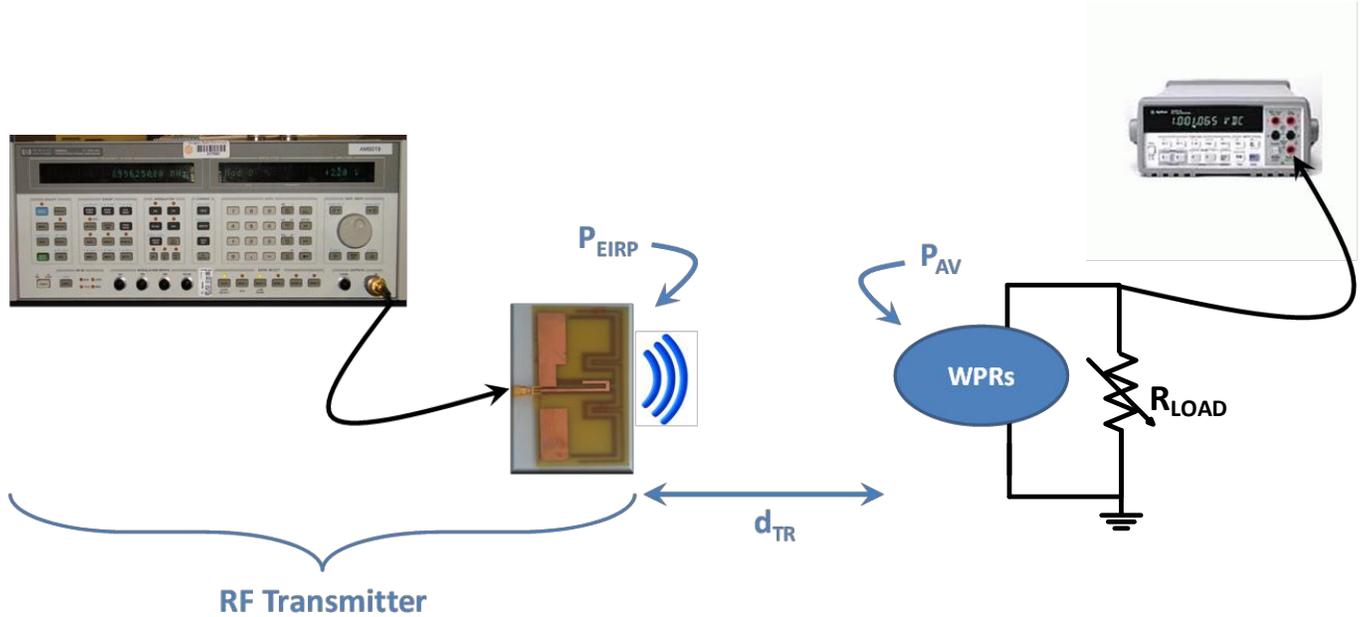
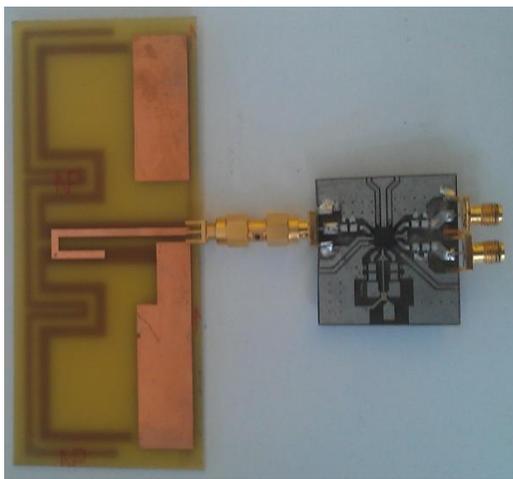


Figure III.32: Schematic of WE/PT measurement setup.

First, the antenna is placed at a distance, d_{TR} , of 3 meters from the RF generator and the collected power is measured with a HP EMP-441A power meter, which works out the sum of the received power at different frequencies in the spectrum range. The received power is also measured with an HP 8593E spectrum analyzer to evaluate the power available at the desired operating frequency.



(a)



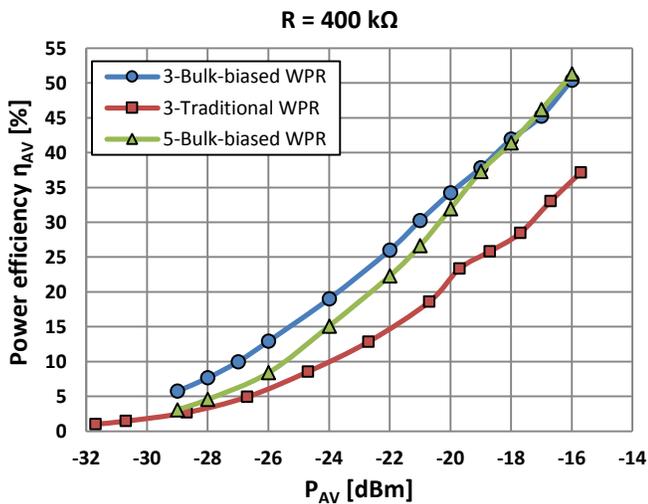
(b)

Figure III.33: The WPR modules with antenna (a) and the wireless measurement scene (b).

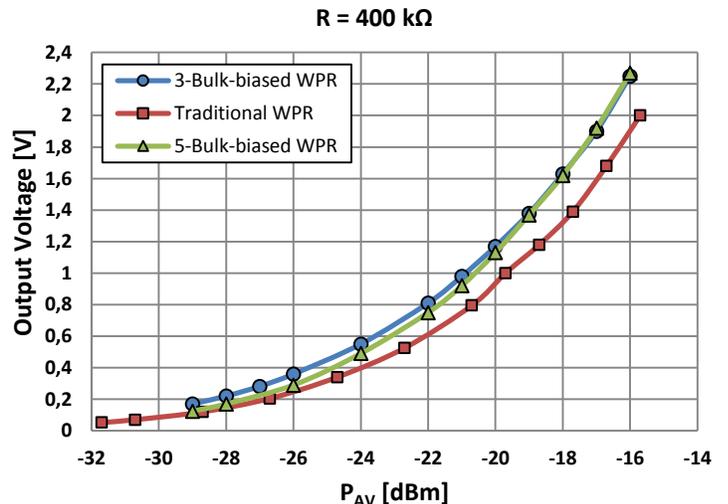
With this measurement setup, a received power of -28.5 dBm is measured when the RF signal generator source sends to the transmitting antenna a power of 7.5 dBm. It should be noted that in practice, it is very difficult to accurately estimate the path loss between the transmitter and receiver, as some reflection, diffraction and scattering occur along the propagation of the EM energy. The gain of the custom 50Ω antenna is theoretically 2.2 dBi, Figure III.7 (c) (d), and it is measured to 2.5 dBi in the proposed scenario of wireless power transmission. This first comparison allows validating the measurement set up and conditions of EM propagation.

After characterizing the path loss between the transmitter and receiver, the full-WPR modules, Figure III.33 (a), are measured according to the scenario illustrated in Figure III.33 (b). Figure III.34 shows the output voltage, V_{OUT} , and power efficiency, η_{AV} , for different loads as a function of the available input power at antenna, P_{AV} . The input power is calculated from the Friis equation considering the free-space propagation loss, (I.7) and (I.8), for the 3 WPR modules.

The slope of the output voltage curves is relatively constant over the full range, since the output voltage is inversely proportional to the log of the operating distance. These measurement results are in good agreement with the characterization of the RF to DC conversion modules presented in section Chapter III.4.1. With the reference load, $400k\Omega$, the input power required to rectify $1.2V$ is -20 dBm, Figure III.34 (b), with 35% of power efficiency, Figure III.34 (a).



(a)



(b)

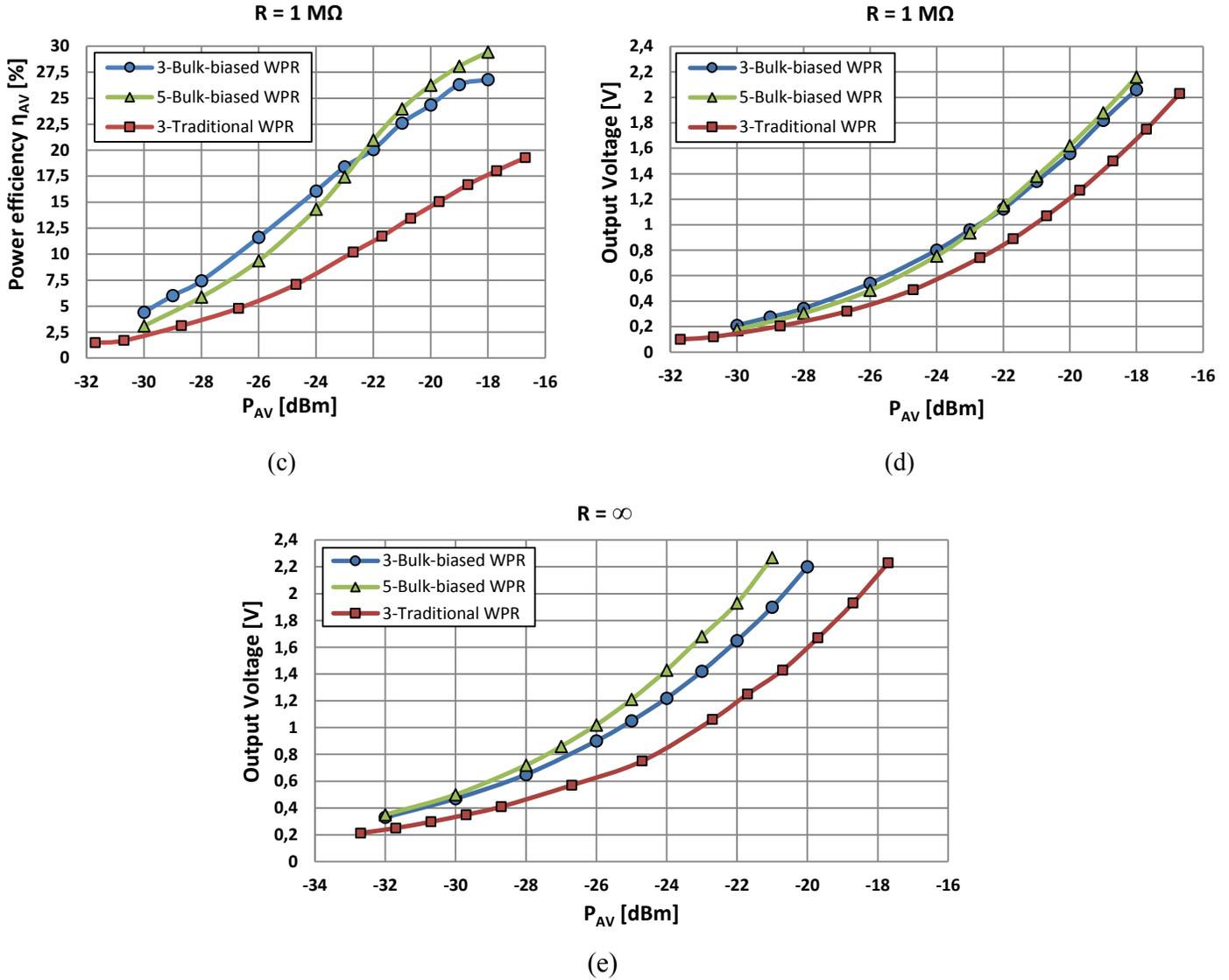


Figure III.34: The power conversion efficiency (a) (c) and the output voltage (b) (d) (e) as a function of input power for the 3 WPR modules under different load circumstances.

A second scenario of WPT is also considered. The RF transmitter radiates a fixed power of 21.5 dBm EIRP and the distance between the transmitter and receiver varies from 2 to 6 meters. The results are illustrated in Figure III.35. Delivering an output voltage of 1.2 V to a 400 kΩ load, the WPRs can operate up to 3 meters, achieving an overall efficiency of 35% and 26% for bulk-biased and traditional harvesters, respectively.

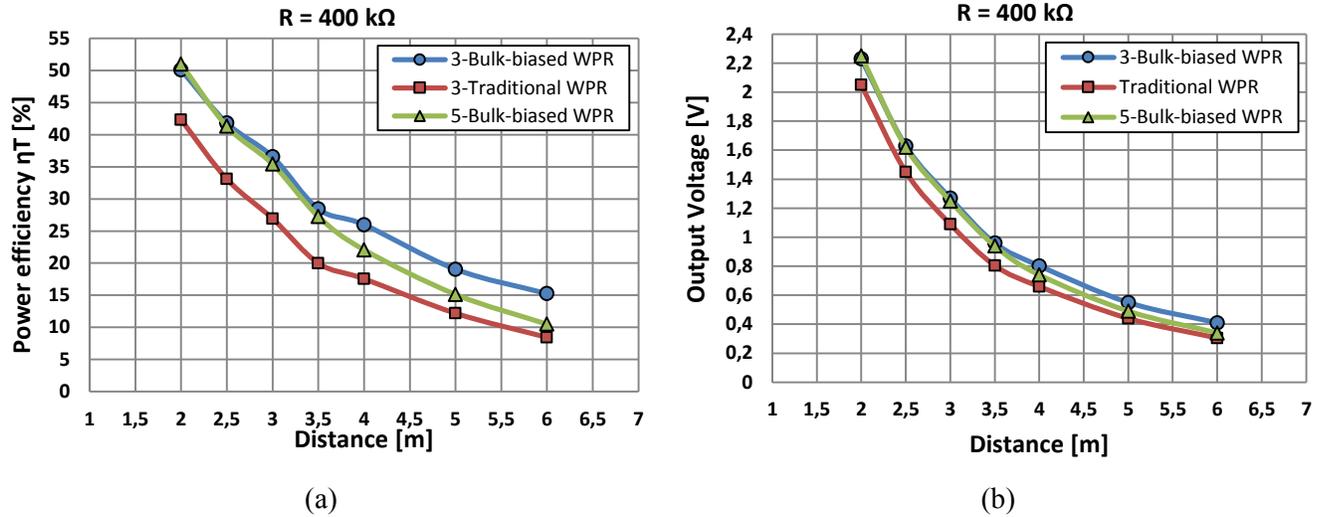
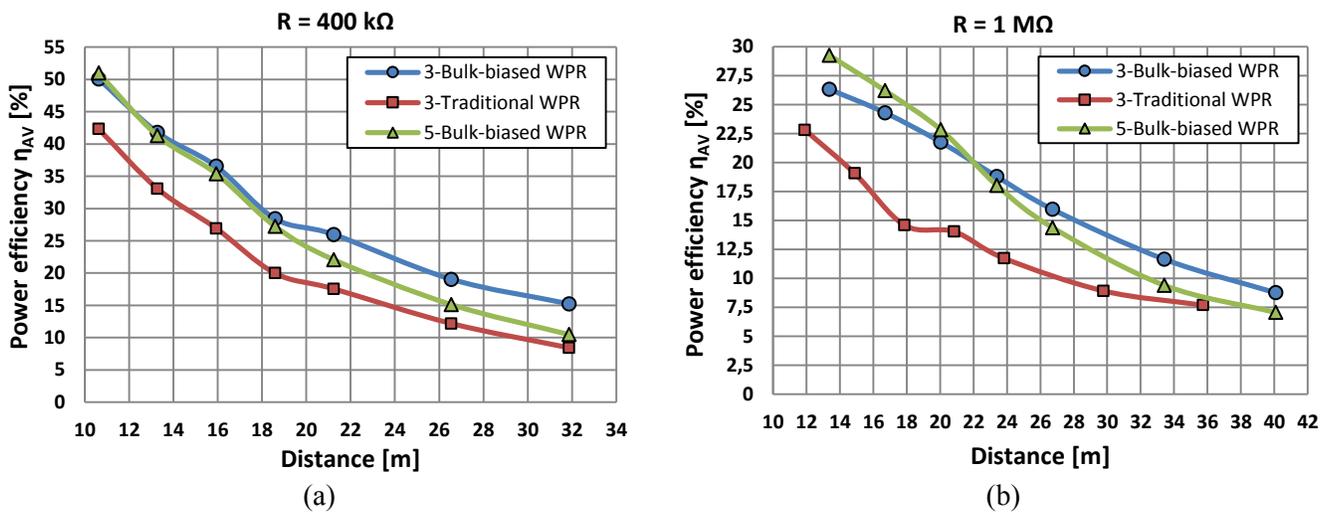


Figure III.35: The power conversion efficiency (a) and the output voltage (b) as a function of distance for the 3 WPR modules loaded with 400 kΩ.

Based on the WE/PT results obtained in the two WPT scenarios, and according to the equation (I.7), an estimation of the operating distance is presented in Figure III.36 for a fixed radiated power of 36 dBm EIRP allowed by standard regulations at UHF frequencies, [121].



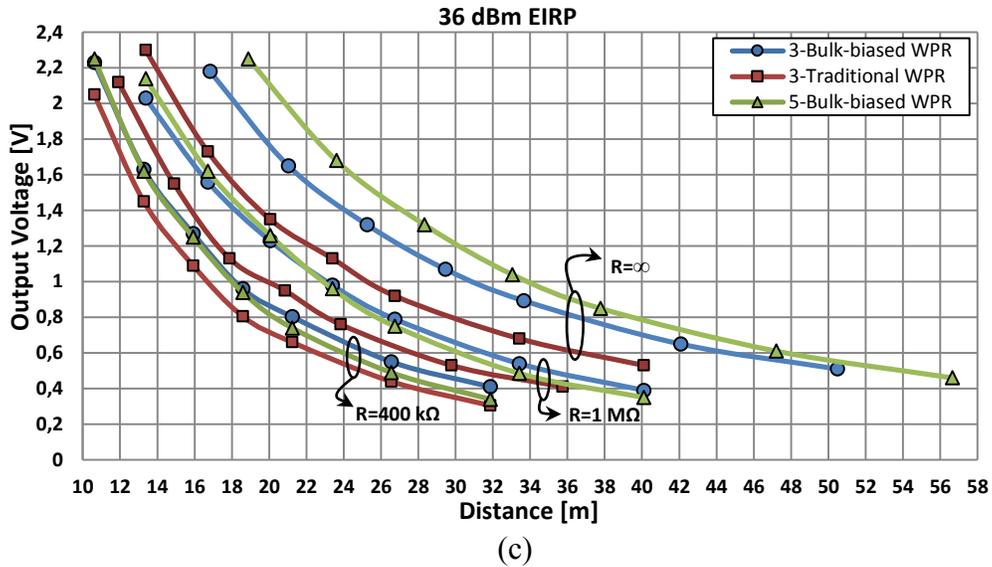


Figure III.36: The power conversion efficiency (a) (b) and the output voltage (c) as a function of distance for the 3 WPR modules sending a power of 36 dBm EIRP.

It is worth-noting the WPRs are capable of rectifying more than 2 V over 10 meters with a 36 dBm radiating source. The measured output DC voltage decreases with the distance and, or, lowering the load resistance. With a 400 kΩ load, the harvesters would theoretically operate up to 15 meters ensuring a 1.2V rectified voltage. The operating distance of the harvesting modules faster reduces for large current load –i.e. small load resistance–. For instance, from 21 to 32 meters the output voltage of the 3-stage bulk-biased WPR is decreased by 37% with an infinite load, and by 50% with 400kΩ, Figure III.36 (c).

Figure III.37 shows the power conversion efficiency achieved by WPRs for an available input power of – 20 dBm with different load resistances. As expected, the maximum efficiency is achieved for a 400 kΩ resistance load. Two factors contribute to this behavior. First, the integrated rectifiers are optimized to properly power supply this load. Second, the input impedance changes with the required load. The impedance transformation is designed to match a 50 Ω source with a 400 kΩ load, the mismatch imposed by different loads contributes to decrease the overall power efficiency.

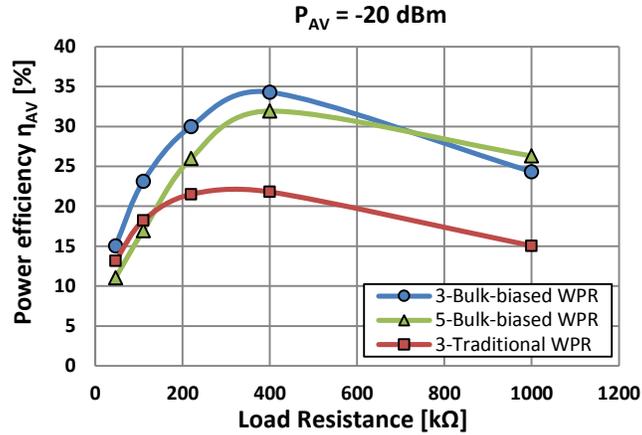


Figure III.37: Maximum power efficiency achieved by WPRs for different loads at -20 dBm.

4.3 Wireless powered module - Setup 3: Inductive Antennas and Rectifiers at 900 MHz and 2.45 GHz

The inductive antennas developed in this work are used as a complex conjugate to the RF-to-DC converters impedances. The two rectifiers selected for such purpose are: the 5-stage bulk-biased rectifier, and the 5-stage cross-coupled configuration, described in Chapter I and sections III.4.1 and III.4.2.

The inductive antenna, discussed in section Chapter III.2.2.2, is supposed to directly match the rectifier impedance. The chip is mounted, and wire bonded, on a FR4 board, which hosts the inductive antenna, as illustrated in Figure III.38. At 900 MHz, the size of the PCB does not exceed $5 \times 5\text{cm}^2$, Figure III.38 (a) (b). At 2.45 GHz, it is only $1.7 \times 5\text{cm}^2$ for the cross-coupled WPR, Figure III.38 (d). It is noticed that the co-design with an inductive antenna is a better option than 50Ω matching for compact solutions.

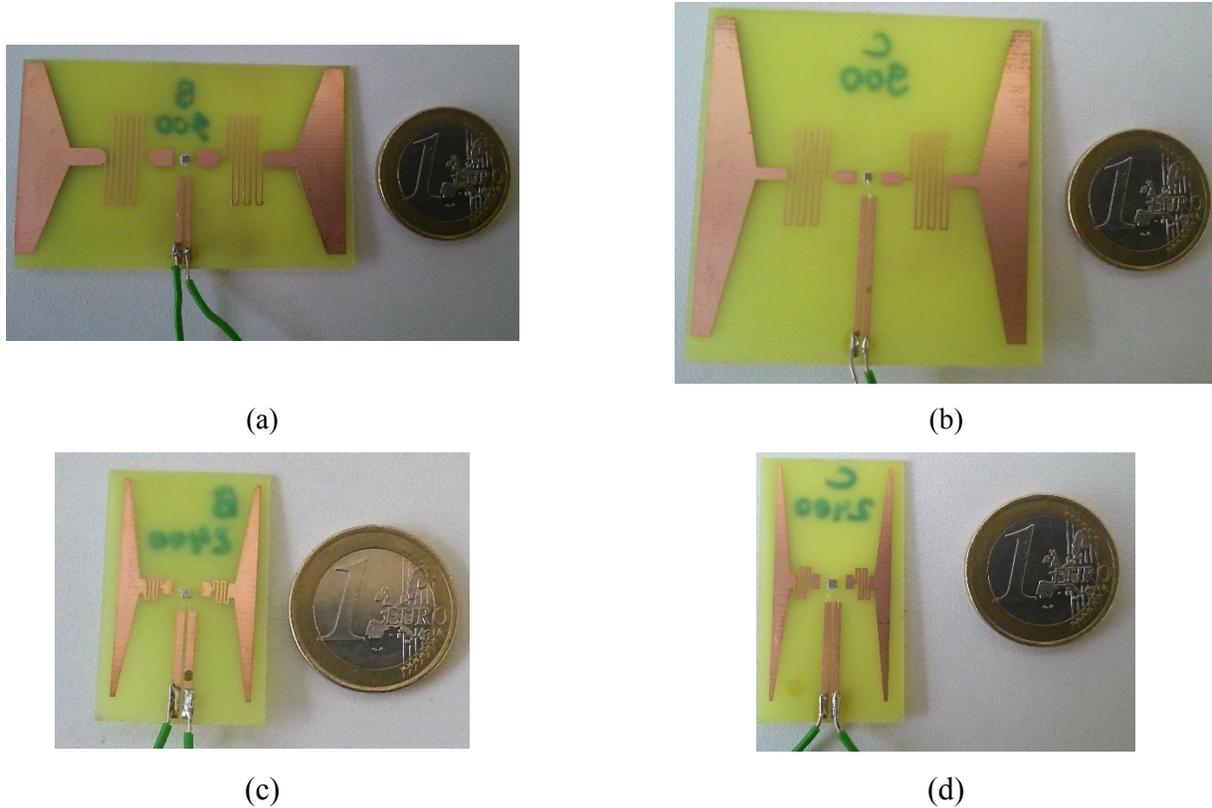


Figure III.38: Bulk-biased (a) (c) and cross-coupled WPRs (b) (d) operating at 900 MHz (a) (b) and 2.45 GHz (c) (d).

The WPT scenario for the measurement of the WPRs using inductive antennas is the same described in section Chapter III.4.2 and represented in Figure III.32. The experimental results are reported in Figure III.39. These WPRs designed to achieve better results at 910 MHz and 2.45 GHz, Figure III.16 (c) and Figure III.18 (c), actually, exhibit best performances at 915 MHz and 2.48 GHz, respectively. These small frequency shifts come from the estimation of the wire-bonding length. These discrepancies are acceptable and do not affect the overall performances of the RF harvesters.

The analysis of the measurement results presented in Figure III.39 figures out the behavior of the cross-coupled rectifier is close to the simulations reported in Chapter II.4.9. The maximum power efficiency of the cross-coupled WPR, Figure III.39 (a), occurs at a P_{av} of -21dBm, which yields a 1.5V@400k Ω , Figure III.39 (b). At 900 MHz, the efficiency η_{av} is of 73% with an input power of -21dBm and, at 2.45 GHz, it is of 83% with a P_{av} of -21.8dBm. The 0.8 dB difference comes from the gain of the antenna, which is 1 dB lower at 900 MHz.

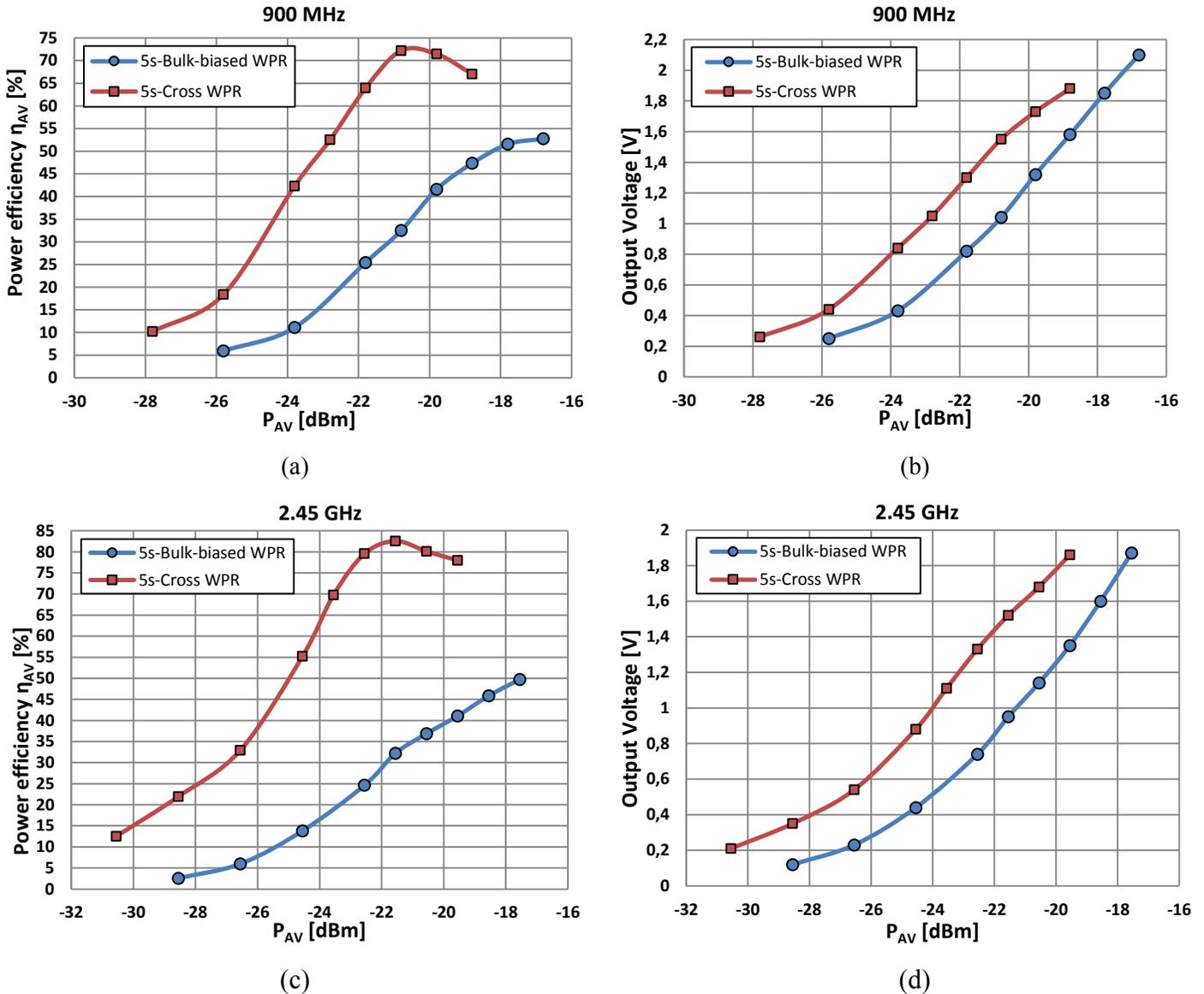


Figure III.39: Bulk-biased and cross-coupled WPRs overall power efficiency (a) (c) and output voltage (b) (d) as a function of input power operating at specification conditions.

Under a specific condition to deliver a DC power supply of 1.2 V@ 3 μ A, the cross-coupled WPR also presents better performances compared to the bulk-biased architecture. It delivers an output power of 3.6 μ W for an input power of -22.3 dBm @900 MHz and -23.2 dBm @2.45 GHz, which represents an overall efficiency of approximately 60% and 75%, respectively. To yield the same output power, the bulk-biased architecture requires an input power of -20.3 dBm with 38% of efficiency.

5 Conclusions

This chapter addressed the realization of wireless powered receivers (WPRs) operating at 900 MHz and 2.45 GHz. According to the system block diagram, Figure II.1, the harvesting modules include, at least, an antenna and a rectifier to properly deliver a DC output voltage to further supply an application or to store the energy in a capacitor. The Chapter I presents:

- the design of different antennas according to two strategies for WPR implementation;
- the full characterization of the rectifiers exposed in Chapter I;
- the measurement results of the WPRs in a scenario of wireless power transfer.

The most relevant results related to the WPRs, embedding the outcome of the antenna investigations and rectifier characterizations, are reported in TABLE III.6 with some realizations of the state-of-the-art operating in the 900 MHz and 2.4 GHz ISM bands for comparison. Many systems of the state-of-the-art present a high efficient power conversion, such as [123] and [125] with 56% and 90%, respectively. However, it is achieved at a relatively high input power, -10dBm in [123] and -8dBm in [125], thus limiting the receivers operating range.

The decrease of the input power directly impacts in the power efficiency of the rectifier, as illustrated in TABLE III.6: in [126], the maximum power efficiency is 25% @ $P_{AV} = -20\text{dBm}$; in [127], it is 14% @ $P_{AV} = -20\text{dBm}$. To address this purpose, we worked on improving the power efficiency of RF rectifier at low power level. Two solutions were proposed: the bulk biased technique and the cross-coupled configuration. The first figures out a significant increase with a power efficiency of 35% with an input power, P_{AV} , of approximately -20dBm . The second approach achieves among the best power efficiency reported so far for a WPR operating below -20dBm : it is 73% @900 MHz with an available input power of -21dBm , and 83% @2.45 GHz with a P_{av} of -21.8dBm .

Besides the investigations on the rectifier optimization, we consider two strategies in the development of the WPRs. The first is the assembly of a $50\ \Omega$ antenna with a rectifier combined to an intermediate matching network. The second approach is the design of an inductive antenna

directly matched to the rectifier input impedance. Such rectenna allows a smaller footprint compared to a 50 Ω matching implementation. At 900 MHz, the size of the 50 Ω bulk-biased WPR is 10×5 cm², and it is only 5×5 cm² for the cross-coupled rectifier co-designed with an inductive dipole element.

TABLE III.6 Comparison with the State-of-the-Art WPRs.

	[122]	[123]	[124] ¹	[125]	[126] ²	[127]		This work ³	This work ⁴	
Freq [GHz]	2.45	2.45	5.8	2.45	0.9	0.9	2	0.9	0.9	2.45
Sensitivity [dBm]	-12.6	-10	-13	-8	-20	-19.3	-19	-20	-22.3	-23.2
V_{OUT} [V]	1	-	1	-	2	1.1		1.2	1.2	
Output current [μA]	0.1	-	1	-	0.4	1.15		3	3	
η [%]	16	56	14	90	25	14	12	35	60	75
Operating distance [m]	-	1@20dBm EIRP	-	2.5@40dBm EIRP	15@36dBm EIRP	-		3@21dBm EIRP	3@18.9 dBm	1.2@18.7 dBm
Size [cm²]	-	15 x 18	-	10 x 10	15 x 2	-		10 x 5	5 x 5	1.7 x 3.5
Technology	130nm CMOS	HSMS-2820	130nm CMOS	HSMS-2852	250nm CMOS	130nm CMOS		130nm CMOS	130nm CMOS	

¹ Schottky diodes

² Floating gate transistors

³ Bulk-biased WPR for 50Ω systems

⁴ Cross-coupled WPRs for dedicated systems

The measurement results reported in this chapter investigates the capability of low cost, and power efficient, CMOS RF harvesters to collect EM energy from a low power environment. Focusing on the implementation and characterization of WPRs, it has been demonstrated that the co-design of the antenna together with the rectifier yields the best performances with:

- a sensitivity of 1.2V at 3 meters for a radiated power of 18.9dBm @900 MHz;
- a power efficiency of 83% for an input power of – 23.2dBm at 2.45GHz;

The co-design approach also contribute to decrease the size of the WPRs, which is only 1.7 x 3.5 cm² at 2.4 GHz and 3 x 5 cm² at 900MHz.

Most of wireless powered receivers existing today embeds expensive devices and materials, such as commercial enhanced schottky diodes, floating gate transistors, high performance PCB, etc., to increase the sensitive in harvesting applications. This thesis work, from the design of custom antennas to the development of high efficient integrated low-power rectifiers, demonstrates the feasibility of low cost wireless powered receivers with high power efficiency in 900 MHz and 2.45 GHz bands.

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Chapter IV

Chapter IV. Conclusions

A limitation of current wireless communicating systems is the finite energy sources used to supply these kind of devices inside the operating field. Battery technology has only progressed incrementally; this is in contrast to Moore's law encountered in the microprocessor and wireless domains. Given the ubiquity of portable devices present in everyday use, battery technology might become mature at an increasing rate in the future. In the meantime, other solutions are needed to address the strong dependence that wireless communicating devices currently have on finite battery sources.

One approach proposed by the research community to solve the limitation of current battery technologies is wireless energy harvesting. This entails the use of transducers capable of converting ambient energy sources into usable and storable electrical energy. A number of wireless power-harvesting devices have been proposed to take advantage of several potential sources to scavenge energy available at the environment.

The nature of many low-power wireless applications means that energy harvesting is an attractive method of meeting their energy requirements. However, it is clear that a good understanding of the nature of the several energy sources and of the different conversion mechanisms available is necessary if the most appropriate solution is to be found.

Based on the published data considered, it can be seen that there is a large range of device volumes and power levels achieved lately by different wireless harvesting methods. RF energy harvesting is one of the most viable technologies to perform wireless power transfer. Two main features contributes to it: RF power can be easily provided when needed, in every location, by means of intentional radiators and its simplicity to be integrated with other electronic circuits.

This thesis work focused on advancing the wireless harvesting research towards improvements in power conversion efficiency of RF scavenging circuits throughout the design and

implementation of high-efficient WPRs. Regarding the overall wireless powered receiver, the system includes an RF-to-DC converter module, implemented through high-efficient n-stage voltage multiplier, a matching network and an antenna.

The n-stage voltage multiplier circuits were prototyped in a 130 nm standard CMOS technology by ST Microelectronics to deliver an output power of 3.6 μ W (1.2 V, 3 μ A). The sensitivity achieved by these rectifiers goes down to – 22 dBm, providing enough output voltage level to supply most low power applications. This higher sensitivity of the multi-stage voltage multiplier architectures makes them more suited for a long range wireless power transfer.

Regarding the entire WPRs operating at 900 MHz and 2.45 GHz bands, they were prototyped in PCBs and characterized to operate in two different systems:

- Standard (50 Ω matched): where the integration of WPRs is performed to complement the wireless communication devices in order to power supply fully or partially its circuitry,
- Custom: where they are developed to operate only for its own purpose, such as RFIDs and wireless sensors applications.

Considering the WPRs embedded in 50 Ω systems, it is depicted that the integration of matching circuits present much higher RF losses to perform the rectifier to antenna impedance transformation, where they require at least half of the available power. This wasted power to match the impedances compromises the WPRs range of operation for low-power applications.

Using low-loss PCB substrate and high-Q COTS devices optimized for UHF purpose could increase the overall WPR performances. However, it also increases the overall fabrication cost, limiting the goal of the low-cost WPRs development in first place. Despite the losses, the best power conversion efficiency achieved in this systems is of 35%, with the bulk-biased voltage multiplier and relying on the 2 dBi gain of the 50 Ω antenna. This harvested energy is enough to power supply applications consuming 3.6 μ W@1.2 V, operating at – 20dBm sensitivity region.

In relation to the custom WPRs, inductive antennas with high difference between real and imaginary impedances have been developed. This achievement properly matches the high capacitive nature of voltage multipliers, which operate more effectively at low-power region to power supply low consumption applications.

Concerning the performances of these systems, the power conversion efficiency achieves 75%, requiring an input power less than -23 dBm to power supply applications consuming $3.6 \mu\text{W}@1.2$ V.

The realization of low-cost wireless powered receivers with high sensitivity to power supply low-power applications has been validated throughout several experimental tests. The operating range concerned is the UHF frequencies in which the low-power WPRs are able to achieve high performances even at frequencies as high as 2.45 GHz. These WPRs were prototyped using low-cost materials, such as standard CMOS devices, to perform the integrated rectifiers, and standard single layer FR4 substrate, for the antennas realization and common substrate support to mount the IC devices. With these advances in RF energy harvesting systems and as IC power threshold decreases, ambient RF energy harvesting will become feasible and available in more areas.

Regarding future works, a PMU must be considered, since every electronic circuit is designed to operate under some supply voltage, which is usually assumed to be constant. This PMU module provides this constant DC output voltage and contains circuitry that continuously holds the output voltage at the designed value regardless of changes in load current or input voltage.

The challenge in designing such a circuit to regulate the output voltage provided by a WPR is to properly operate within a high range variation of the supplied voltage, *i.e.*, ensuring a constant output voltage under different input power levels. Furthermore, the PSSR must be handled with care, since its value tends to degrade with frequency, especially at UHF.

Another area to be explored is the storage device, since, nowadays, they are not much efficient yet in order to ensure long lifetime for wireless energy harvesting applications. The drawbacks to each of the existing methods are numerous, though. For instance, even rechargeable batteries wear out after a few hundred charge/discharge cycles, which implies in periodically replacement. There is also supercapacitors with high density storage capabilities, but eventually they change their characteristics, self-discharging rapidly, causing much of the converted energy to be wasted. So, a more robust and permanent solution must be developed to eliminate the need for replacement. Hence, supporting higher charge/discharge cycles and self-discharging slowly with time.

Conclusions

Un des inconvénients des systèmes de communication sans fil actuels est l'énergie finie des sources d'alimentation utilisées dans ces dispositifs électroniques pour assurer leur fonctionnement correct à l'intérieur du champ de communication. Les différentes technologies des batteries n'ont progressées que de manière incrémentielle, qui est en contraste avec la loi de Moore toujours présent dans les domaines de la microélectronique et communication sans fil. Compte tenu de l'omniprésence des divers appareils portables présents dans l'usage quotidien en utilisant des batteries comme source d'énergie, leur avancement technologique pourrait se développer plus rapidement à l'avenir. Cependant, d'autres solutions sont nécessaires pour répondre à la forte dépendance que les dispositifs de communication sans fil ont actuellement sur les sources d'énergie finies.

Une approche proposée par la communauté de recherche pour résoudre la limitation des technologies de batteries actuelles est la récupération d'énergie sans fil. Cela implique l'utilisation de capteurs capables de convertir l'énergie fournie par divers types de sources présentes dans l'environnement en énergie électrique utilisable et stockable. Un certain nombre de dispositifs télé-alimentés ont été proposées afin de profiter de ces potentielles sources énergétiques pour prolonger la durée de vie des batteries ou, même, devenir complètement autonome sans la nécessité de leur utilisation.

La nature de nombreuses applications sans fil de faible consommation signifie que la télé-alimentation est une méthode intéressante de répondre à leurs besoins énergétiques. Cependant, il est clair qu'une bonne compréhension de l'origine des différentes sources d'énergie ainsi que des différents mécanismes de conversion disponibles est nécessaire si la solution la plus appropriée doit être trouvée.

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D'après certaines informations publiées sur ce sujet, on s'aperçoit qu'il existe une large gamme d'applications et aussi une grande variété des niveaux de puissance obtenus par différents procédés de télé-alimentation développés récemment. La récupération d'énergie par voie RF est une des technologies les plus viables pour effectuer le transfert d'énergie sans fil. Deux caractéristiques principales y contribuent:

- De la puissance RF peut être facilement fourni dans tous les lieux, si nécessaire, à travers de la distribution des émetteurs RF intentionnels,
- et grâce à sa simplicité à être intégré avec d'autres circuits électroniques.

Ce travail de thèse a porté sur l'avancement de la recherche de la télé-alimentation par voie RF des dispositifs électroniques en améliorant l'efficacité globale de la conversion d'énergie des modules télé-alimentés. Cette amélioration a été démontrée à travers de l'étude, conception et réalisation des WPRs d'haute sensibilité. Concernant la structure de ces modules télé-alimentés, le système comprend un circuit convertisseur RF-DC, implémenté par un multiplicateur de tension d'haute efficacité à n-étages, un réseau d'adaptation et une antenne.

Les circuits multiplicateurs de tension à n-étages ont été prototypés en technologie CMOS 130 nm standard par ST Microelectronics. Ces multiplicateurs de tension fournissent une puissance de sortie de 3,6 uW (1,2 V, 3 uA) et leur sensibilité atteint des valeurs aussi faibles que -22 dBm, en assurant des niveaux de tension de sortie suffisamment élevés pour alimenter la plupart des applications de faible consommation. Cette sensibilité élevée atteint par ces architectures de multiplicateurs de tension les rend plus adaptées pour réaliser le transfert d'énergie sans fil à longue portée.

En ce qui concerne l'ensemble des WPRs fonctionnant à 900 MHz et 2,45 GHz, ils ont été prototypés sur PCB et caractérisés pour être appliqués dans deux types différents de systèmes:

- Standard (adapté à 50 Ω): où l'intégration de WPRs est effectuée pour compléter les dispositifs de communication sans fil afin de les alimenter complètement ou partiellement,
- Personnalisé: où ils sont développés pour des solutions particularisées, comme les étiquettes RFID et certaines applications en utilisant de capteurs sans fil.

Par rapport aux WPRs incorporés dans les systèmes classiques à 50 Ω , on s'aperçoit que l'intégration des circuits d'adaptation pour effectuer la transformation de l'impédance de l'antenne standard à l'impédance du redresseur présente des pertes RF très élevés. La consommation minimale exigée par ces circuits est d'au moins la moitié de la puissance RF disponible à l'antenne.

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Ce gaspillage de puissance pour effectuer l'adaptation des impédances compromet la distance de fonctionnement des WPRs pour les applications de faible consommation.

L'utilisation d'un substrat de type PCB à faible perte et des composants COTS avec Q élevé, qui sont optimisés pour les UHF, pourraient augmenter la performance globale des WPRs à 50Ω . Toutefois, le coût total de fabrication serait beaucoup plus élevé, qui limite l'objectif initial de la réalisation des modules à faible coût. Malgré les pertes, la meilleure efficacité de conversion de puissance obtenue dans ces modules à 50Ω est de 35%, avec le multiplicateur de tension en utilisant l'effet de corps des transistors et en comptant sur un gain de 2 dBi de l'antenne. Cette énergie récupérée est suffisant pour alimenter des applications consommant $3,6 \mu\text{W}@1.2 \text{ V}$ et fonctionnant à la région de sensibilité de -20dBm .

Pour les WPRs personnalisés, antennes inductives avec une forte différence entre les impédances réelles et imaginaires ont été développés. Cette réalisation adapte correctement à la nature capacitive élevée des multiplicateurs de tension, qui fonctionnent de manière plus efficace à la région de faible puissance pour alimenter des applications à faible consommation.

Concernant la performance de ces systèmes personnalisés, l'efficacité de conversion de puissance atteint 75%, c'est-à-dire que ces modules nécessitent d'une puissance d'entrée inférieure à -23 dBm pour alimenter des applications consommant $3,6 \mu\text{W}@1.2 \text{ V}$.

La réalisation de récepteurs télé-alimentés par voie RF à faible coût avec une haute sensibilité dédiée aux applications de faible consommation a été validé à travers des plusieurs tests expérimentaux. La plage de fonctionnement fréquentiel concerné est les UHF dans lesquelles les WPRs de faible puissance sont capables d'atteindre des performances élevées, même à des fréquences aussi hautes que 2,45 GHz. Ces WPRs ont été prototypés en utilisant des matériaux à faible coût, tels que les dispositifs CMOS standard, pour réaliser les redresseurs intégrés, et des substrats de type FR4 simple couche, pour la réalisation des antennes et de support pour monter les circuits intégrés. Grâce à ces avancements dans les systèmes télé-alimentés par voie RF et aussi à la diminution de la puissance de seuil des circuits intégrés, la récupération d'énergie électromagnétique ambiant deviendra réalisable et disponible dans plusieurs domaines à l'avenir.

Par rapport aux travaux futurs, une PMU doit être considérée, car chaque circuit électronique est conçu pour fonctionner sous une tension d'alimentation, qui doit généralement être constant. Ce module PMU assure une tension de sortie continue constante et contient des

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circuits qui maintiennent en permanence la tension de sortie figée à une valeur indépendamment des changements de courant de charge ou de la tension d'entrée.

Le défi dans la conception d'un tel circuit pour réguler la tension d'alimentation fourni par un WPR est de maintenir une tension régulée constante dans une plage de variation de la tension d'alimentation relativement large. – *i.e.*, en assurant une tension de sortie constante sous différents niveaux de puissance disponibles à l'entrée des WPRs—. En outre, le PSSR doit être manipulé avec soin, puisque sa valeur a tendance à se dégrader avec la fréquence, en particulier aux UHF.

Un autre domaine à explorer est le dispositif de stockage, puisque, actuellement, il n'est pas encore très efficace pour assurer une durée de vie élevée aux applications sans fil en utilisant la télé-alimentation. Les inconvénients de chacune des méthodes existantes sont encore nombreux. Par exemple, même les batteries rechargeables s'épuisent après quelques centaines de cycles de charge / décharge, ce qui implique leur remplacement périodique. Il existe également des supercondensateurs connus pour avoir une densité de stockage très élevée, mais au fur et à mesure leur caractéristiques changent et perdent cette capacité élevée de stockage. Donc, ils s'auto-déchargent rapidement, provoquant le gaspillage d'une grande partie de l'énergie convertie. Ainsi, une solution plus robuste et stable doit être développée afin d'éliminer la nécessité d'une intervention manuelle pour l'entretien des dispositifs télé-alimentés. Par conséquent, batteries en supportant cycles de charge / décharge élevés et s'auto-déchargeant lentement avec le temps sont nécessaires.

Scientific Productions

International Journals:

Karolak, D.; Taris, T.; Deval, Y.; Bégueret, J.-B.; Mariano, A., "Design of High Sensitivity Radiofrequency Energy Harvesters Dedicated to Low-Power Applications," *Journal of Low Power Electronics (JOLPE)*, v. 10, p. 72-83, 2014.

International Conferences:

Karolak, D.; Taris, T.; Deval, Y.; Bégueret, J.-B.; Mariano, A., "Design comparison of low-power rectifier dedicated to RF energy harvesting," *IEEE Electronics, Circuits and Systems (ICECS)*, 2012 19th (2012), pp. 524–527.

Karolak, D.; Taris, T.; Deval, Y.; Bégueret, J.-B.; Mariano, A., "Bulk Biased RF Energy Harvesting Dedicated to 900MHz/2.4GHz ISM Bands," *Workshop on Circuits and Systems Design (WCAS)*, 2013 3rd Symposium, Sept. 2 2013-Sept. 6 2013.

National Conferences:

Karolak, D.; Taris, T.; Deval, Y.; Bégueret, J.-B.; Mariano, A., "Comparaison de conception de redresseurs à faible puissance dédiés à la récupération d'énergie RF," *Journées Nationales Microondes (JNM)*, Paris 2013.

Systeme de radiocommunication télé- alimenté par voie RF

Aujourd'hui, la gestion de l'énergie requise par les dispositifs autonomes sans fil et portables est une question importante. Ultérieurement, le stockage de l'énergie a été significativement amélioré. Toutefois, ce progrès n'a pas été suffisant pour suivre le développement de microprocesseurs, mémoire de stockage, et des applications de la technologie sans fil. Par exemple, dans les capteurs sans fil alimentés par batteries, les modules devraient avoir une longue durée de vie. Cependant, la limitation énergétique des batteries ne peuvent pas fournir assez de puissance pour l'assurer. Par conséquent, l'entretien devient nécessaire de temps en temps. Le problème majeur de cet inconvénient est de garantir l'entretien efficace des batteries pour un réseau à grande échelle contenant des centaines, voire des milliers de nœuds de capteurs, ce qui peut être une lourde tâche, voire impossible.

Les sources d'alimentation provenant de la nature, pour effectuer le remplacement des batteries, sont envisagées afin de réduire au minimum l'entretien et le coût d'opération du système. La télé-alimentation peut activer des appareils électroniques sans fil et portables pour devenir complètement autonome, de telle sorte que l'entretien des batteries peut être finalement supprimé.

Les avancements technologiques de l'électronique à faible puissance et des dispositifs de communication sans fil permettent le développement de systèmes plus efficaces en termes d'énergie, tels que les étiquettes RFID et les nœuds de capteurs sans fil. Beaucoup a été écrit sur les bénéfices de l'utilisation de ces dispositifs et le potentiel de la télé-alimentation pour fournir de l'énergie pendant leur durée de vie.

L'énergie électromagnétique est une solution populaire pour réaliser le transfert de l'énergie sans fil. Cette approche s'appuie sur l'utilisation des rayonnements électromagnétiques pour fournir une puissance continue utilisable. L'énergie RF est récupérée par une antenne à partir des émissions radio intentionnelles ou des sources non-intentionnelles déjà existantes dans l'environnement. La conversion des signaux reçus et le conditionnement de la puissance de sortie réalisé par un module télé-alimenté (WPR) est décrit schématiquement sur la Figure 40. Il existe

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plusieurs approches pour convertir un signal RF en courant continu, en fonction de la condition de fonctionnement désirée. La quantité d'énergie disponible au dispositif final dépend de plusieurs facteurs, notamment de la puissance de la source émettrice, la distance entre le module et la source, gain de l'antenne, adaptation, et l'efficacité globale de la conversion.

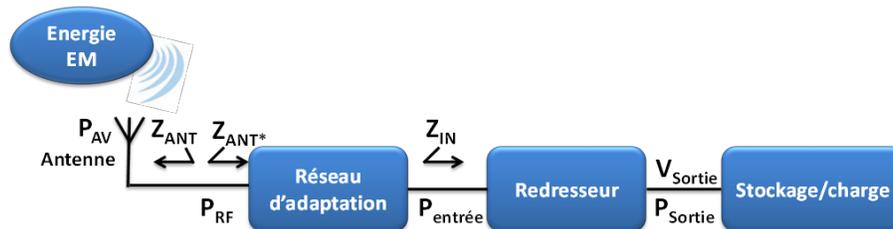


Figure 40: Structure simplifiée d'un récepteur télé-alimenté (WPR).

Le réseau d'adaptation réalise la transformation d'impédance entre l'antenne et le circuit redresseur afin d'éviter les pertes de retour et ainsi maximiser le transfert d'énergie. Le dispositif de stockage peut être considéré comme un filtre passe-bas, qui rejette les harmoniques de l'ordre élevé générées pendant la procédure non-linéaire de redressement. La charge de sortie est tout type de dispositif alimenté par une source DC.

L'objectif de cette thèse est de réaliser un WPR capable d'alimenter efficacement certains dispositifs électroniques sous les conditions de faible puissance disponible. Cette approche pourra remplacer le besoin de l'utilisation d'une batterie grâce à la télé-alimentation et à la récupération de l'énergie EM disponible dans l'environnement. Pour effectuer cette tâche, le redresseur est l'une des parties les plus importants du système.

La sensibilité, impédance d'entrée, tension de sortie délivrée et l'efficacité de conversion de puissance sont les paramètres à prendre en compte lors de l'analyse d'un circuit redresseur. L'efficacité est l'un des paramètres de performance les plus importants de ce type de circuit, car il est ce qui prédit la sensibilité des modules télé-alimentés requise pour un fonctionnement correct. Une sensibilité élevée implique en une amélioration de la distance de fonctionnement maximale atteinte par le WPR.

Pour améliorer l'efficacité de puissance des redresseurs fonctionnant à partir d'une faible puissance d'entrée, il existe essentiellement 2 options. Soit, les pertes de puissance doivent être réduites dans le dispositif actif à travers d'un dimensionnement / conception spécifique pour minimiser ces pertes RF, qui se sont principalement reposées sur la technologie. Soit, la tension de seuil des dispositifs, V_{Th} , doit être réduite.

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Deux architectures ont été proposées pour réduire la tension de seuil des transistors d'une technologie CMOS standard et, ainsi, augmenter les rendements des circuits redresseurs. Une architecture compte sur la réduction de la tension de seuil globale du circuit par un contrôle de la polarisation du substrat des transistors. La deuxième approche est une compensation réalisée par un décalage de tension généré entre les bornes de la grille et drain des transistors. Cette dernière configuration a le même effet d'une réduction direct sur le V_{Th} des transistors, vu que la condition $V_{GS} \geq V_{Th}$ est atteinte pour des tensions d'entrée inférieures à V_{Th} et, donc, améliorant la performance par rapport à la condition traditionnelle.

Les figures Figure 41 et Figure 42 compare la performance de tous les 3 architectures des redresseurs, couplage-croisé, polarisation de substrat et traditionnelle, prototypées en technologie 130nm CMOS standard de ST Microelectronics.

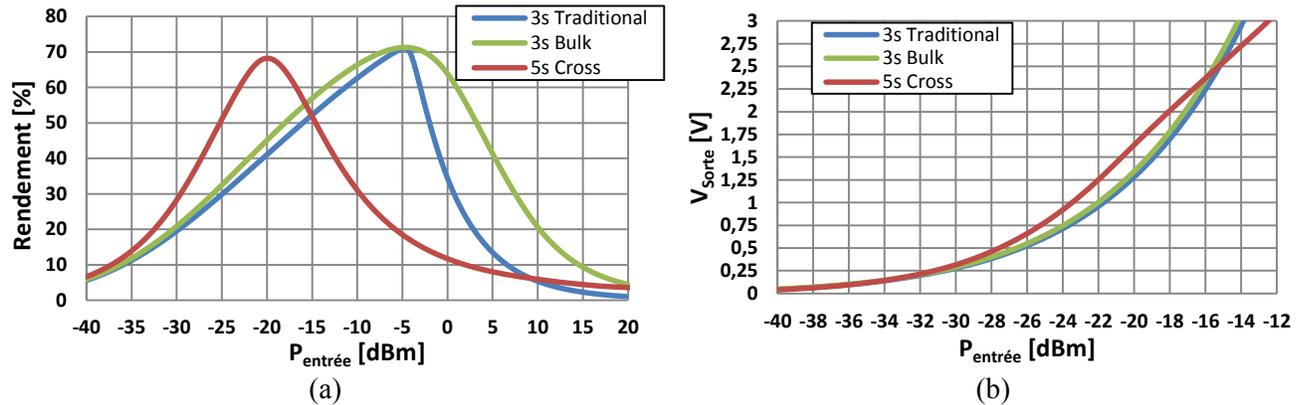


Figure 41: (a) Rendement des redresseurs en fonction de la puissance d'entrée, (b) Tension de sortie en fonction de la puissance d'entrée à 900 MHz.

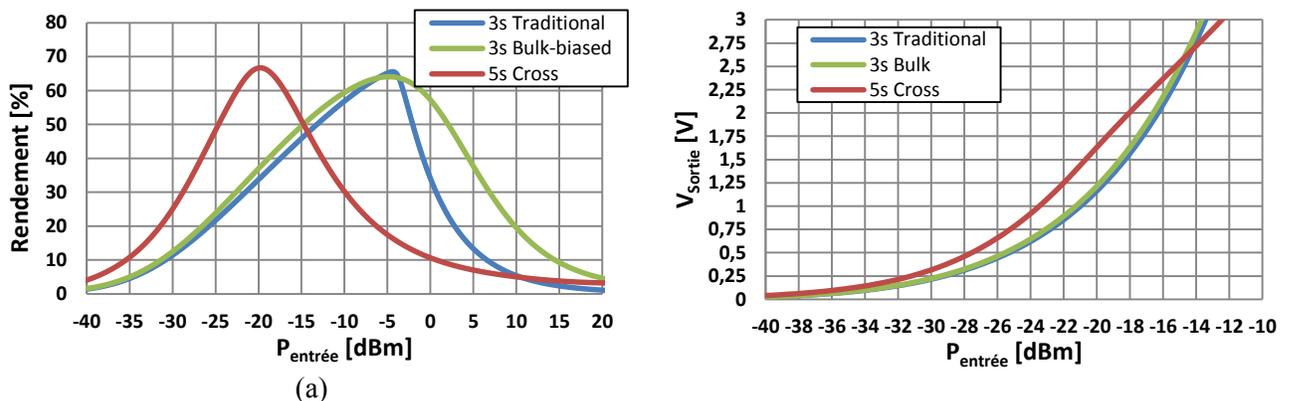


Figure 42: (a) Rendement des redresseurs en fonction de la puissance d'entrée, (b) Tension de sortie en fonction de la puissance d'entrée à 2.4 GHz.

On s'aperçoit que les architectures proposées montrent des performances supérieures en comparaison avec la topologie de redressement traditionnelle. Pour répondre aux spécifications

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imposées par le cahier des charges, le meilleur rendement atteint 63% contre 40% de l'architecture traditionnelle. La sensibilité améliorée par les topologies proposées varie de 1 à 2 dB.

Les différents redresseurs conçus et prototypés en une technologie CMOS standard ont été intégrés aux récepteurs télé-alimentés (WPRs) selon deux scénarios différents:

- Avec une antenne adaptée à 50Ω aux fréquences de 900 MHz et 2,45 GHz,
- Avec une antenne directement adaptée au complexe conjugué de l'impédance des multiplicateurs de tension à 900 MHz et 2,45 GHz.

La Figure 43 présente ces modules télé-alimentés réalisés durant ce travail de thèse, ainsi que le scénario utilisé pour effectuer leurs caractérisations.

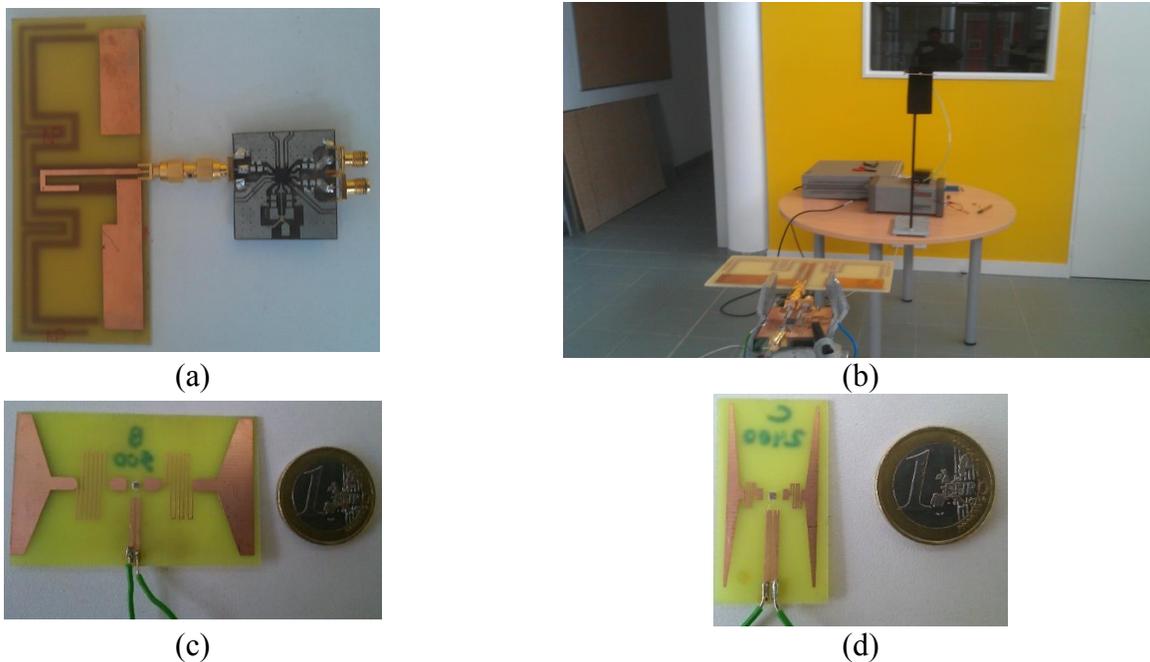


Figure 43: (a) Modules WPR adaptés à 50Ω , (b) le scénario pour les mesures expérimentales, (c) WPR inductive à 900 MHz et (d) WPR inductive à 2.45 GHz.

Les résultats les plus pertinents liés aux modules WPRs, intégrant les antennes et les redresseurs réalisés, sont présentés sur le Tableau 1, ainsi que certains modules télé-alimentés présents dans l'état de l'art en fonctionnant dans les bandes ISM. La diminution de la puissance disponible aux bornes d'un WPR influe directement sur le rendement en puissance du redresseur. Pour résoudre cet inconvénient, nous avons travaillé sur l'amélioration de l'efficacité de transfert de puissance des redresseurs fonctionnant dans la région à faible niveau de puissance.

Outre l'optimisation des redresseurs, les deux stratégies pour le développement des modules télé-alimentés ont été considérées. La première est l'assemblage d'une antenne 50Ω à un

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redresseur à travers d'un réseau d'adaptation intermédiaire, qui montre une augmentation significative de la performance avec une efficacité énergétique de 35% pour une puissance d'entrée d'environ -20 dBm. La seconde est la conception d'une antenne inductive directement adaptée à l'impédance d'entrée du redresseur, qui atteint un des meilleurs résultats d'efficacité énergétique rapportés jusqu'ici pour des WPRs fonctionnant en dessous de -20 dBm: ils sont 73% @900 MHz, avec une puissance d'entrée de -21 dBm, et 83% @2.45 GHz, avec une P_{AV} de -21.8 dBm.

La plupart des récepteurs télé-alimentés efficaces existants aujourd'hui embarque dispositifs et matériaux coûteux, tels que des diodes Schottky, transistors à grille flottante, PCBs d'haute performance, etc., pour augmenter leur sensibilité. Ce travail de thèse, de la conception des antennes personnalisées au développement des redresseurs intégrés efficaces à faible puissance d'entrée, démontre la faisabilité de récepteurs sans fil à faible coût avec une efficacité de puissance élevée fonctionnant aux fréquences de 900 MHz et 2,45 GHz.

Tableau 1 : Comparaison avec des modules télé-alimentés de l'état de l'art.

	[122]	[123]	[124] ¹	[125]	[126] ²	[127]		<i>This work</i> ³	<i>This work</i> ⁴	
Freq [GHz]	2.45	2.45	5.8	2.45	0.9	0.9	2	0.9	0.9	2.45
Sensibilité [dBm]	-12.6	-10	-13	-8	-20	-19.3	-19	-20	-22.3	-23.2
V_{Sortie} [V]	1	-	1	-	2	1.1		1.2	1.2	
Curent de sortie [μA]	0.1	-	1	-	0.4	1.15		3	3	
η [%]	16	56	14	90	25	14	12	35	60	75
Distance d'opération [m]	-	1@20dBm EIRP	-	2.5@40dBm EIRP	15@36dBm EIRP	-		3@21dBm EIRP	3@18.9 dBm	1.2@18.7 dBm
Taille [cm²]	-	15 x 18	-	10 x 10	15 x 2	-		10 x 5	5 x 5	1.7 x 3.5
Technologie	130nm CMOS	HSMS-2820	130nm CMOS	HSMS-2852	250nm CMOS	130nm CMOS		130nm CMOS	130nm CMOS	

¹ Diodes Schottky

² Transistors avec grille flottante

³ WPR avec polarisation du substrat pour les systèmes 50 Ω

⁴ WPR avec couplage-croisée pour les systèmes personnalisés

