Caractérisation et modélisation de UTBB MOSFET sur SOI pour les technologies CMOS avancées et applications en simulations circuits

Theano Karatsori

ARISTOTLE UNIVERSITY OF THESSALONIKI

Communauté UNIVERSITÉ Grenoble Alpes

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Présentée par

Théano KARATSORI

Thèse dirigée par **Prof. Gérard GHIBAUDO** et
codirigée par **Prof. Charalabos DIMITRIADIS**

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Francis BALESTRA
Directeur de recherche CNRS Alpes, Président
Brice GAUTIER
Professeur, INSA-Lyon, Rapporteur
Nathalie MALBERT
Professeur, Université de Bordeaux, Rapporteur
Spyridon NIKOLAIDIS
Professeur, Université Aristote de Thessalonique, Examinateur
Dimitrios TASSIS
Professeur Associé, Université Aristote de Thessalonique, Examinateur
Charalabos DIMITRIADIS
Professeur, Université Aristote de Thessalonique, invité
Gérard GHIBAUDO
Directeur de recherche CNRS Alpes, invité

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Electrical characterisation and modeling of advanced nano-scale ultra-thin body and burried oxide (UTBB) MOSFETs and applications in circuit simulations

Thesis defended in public on the **12 Juillet 2017**,
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Research director CNRS Alpes, President
Brice GAUTIER
Professor, INSA-Lyon, Rapporteur
Nathalie MALBERT
Professor, University of Bordeaux, Rapporteur
Spyridon NIKOLAIDIS
Professor, Aristotle University of Thessaloniki, Examiner
Dimitrios TASSIS
Associate Professor, Aristotle University of Thessaloniki, Examiner
Charalabos DIMITRIADIS
Professor, Aristotle University of Thessaloniki, invited
Gérard GHIBAUDO
Research director CNRS Alpes, invited

SIGILLUM UNIVERSITATIS GRATIANOPOLITANAE 1339

Abstract

The progressive down-scaling of CMOS technology has driven the semiconductor industry to the realization of faster and lower power consumption VLSI circuits and systems. Among the most common solutions for high performance nano-scale area devices are the fin-shaped field-effect transistors (FinFETs) and the fully-depleted silicon-on-insulator (FDSOI) MOSFETs, which can provide a high immunity to the short-channel effects (SCEs), low threshold voltage variability and an improved drain-induced barrier lowering level (DIBL). Compared to FinFET, the UTBB FDSOI technology utilizes a much simpler fabrication process thanks to its planar structure. Furthermore, its back-gate bias option makes it particularly interesting for multi-V_t applications.

The present thesis is dealing with issues arising from the scaling of new-era devices in the modern MOSFET design: the development of an analytical and compact drain current model, valid from weak to strong inversion, describing accurately the transfer and output characteristics of short-channel FDSOI devices and the investigation of performance issues -namely reliability and variability issues- of such advanced nano-scale transistors. Meanwhile, the accurate determination of the MOSFET electrical parameters is also essential for understanding the physics and engineering of the devices, particularly if we take into account that as the supply voltage is reduced with device scaling, the operating gate bias moves closer to the threshold voltage (near threshold operation), and the assumption that the inversion charge varies approximately linearly with gate voltage overdrive becomes less and less accurate. Thus, an additional goal is the development of a methodology which allows the extraction of MOSFET parameters over the full gate voltage range i.e. from weak to strong inversion region, enabling to fully capture the transition between subthreshold and above threshold region, despite the reduction of supply voltage.

First, we present a new full gate voltage range methodology using a Lambert W function based inversion charge model, for extracting the electrical parameters in FDSOI nano-MOSFET devices. Split capacitance-voltage measurements carried out on 14 nm technology FDSOI devices show that the inversion charge variation with gate voltage can be well described by the Lambert W function. Based on the drain current equation in the linear region including the inversion charge described by the Lambert function of gate voltage and the standard mobility equation enables the extraction of five electrical MOSFET parameters from experimental transfer characteristics (ideality factor, threshold voltage, low field mobility, first and second order mobility attenuation factors). The extracted parameters were compared with those extracted by the well-known Y-function in strong inversion region. The present methodology for extracting the electrical MOSFET parameters has been verified over a wide range of channel lengths and back gate voltages on nano-scale FDSOI devices, demonstrating its simplicity, accuracy and robustness.

Second, we have derived simple expressions for the minimum value of the front and back gate surface potentials with which we have developed analytical models for the respective threshold voltages and ideality factors with back gate control of lightly doped short channel UTBB FDSOI MOSFETs. The threshold voltage and ideality factor models of the front and back gates have been verified with numerical simulations in terms of the device geometry parameters and the applied bias voltages, as well as with experimental results for devices with channel length down to 17 nm. Based on these models we have developed an analytical drain current compact model for lightly doped short-channel UTBB FDSOI

MOSFETs with back gate control. The model, which includes the effects of drain-induced barrier lowering, channel-length modulation, saturation velocity, mobility degradation, quantum confinement, velocity overshoot and self-heating, has been validated by comparing with experimental transfer and output characteristics of various devices and back-bias conditions. The good accuracy of the model makes it suitable for implementation in circuit simulation tools. Indeed, the drain current compact model is implemented via Verilog-A code for simulation of fundamental circuits in circuit simulators.

Following the drain current compact model development, reliability issues including hot-carrier injection (HCI) and negative bias temperature instability (NBTI) are discussed for these nano-scale UTBB FDSOI MOSFETs. The hot-carrier effect, which occurs near the drain end due to hot carriers accelerated in the channel, is prominent in n-MOS devices, while the NBTI is prominent in p-MOS devices along the entire channel when negative gate-to-source voltage is applied.

- ✓ In our analysis, the hot-carrier (HC) induced traps are investigated by low-frequency noise (LFN) measurements in the frequency and time domain. The measured noise spectra are composed of 1/f and Lorentzian-type components. The Lorentzian noise is due either to generation-recombination noise or to random telegraph noise (RTN). Based on the LFN results, the effect of the HC-stress on FDSOI MOSFETs is investigated after short and long-time stress. Analysis of RTN traps detected in fresh and HC-stressed devices indicate that the RTN amplitude is uncorrelated to the trap time constants, i.e. the impact of the trap depth from the interface is masked by that of the trap location over the channel. The overall results lead to an analytical expression for the RTN amplitude, enabling to predict the RTN changes from the subthreshold to the above threshold region. After we identified the degradation mechanisms and based on our analytical compact drain current compact model, we developed a semi-empirical aging hot-carrier model predicting with good accuracy the device degradation stressed under different bias conditions using a unique set of model parameters.
- ✓ Concerning the NBTI phenomenon, the threshold voltage shifts during stress at different temperatures and gate bias voltage conditions show that the NBTI is dominated by trapping of holes in pre-existing traps of the gate dielectric, while the recovery transient follows a logarithmic-like time dependence. In this way, we have developped an NBTI model capturing the temperature and gate voltage dependence in such UTBB FDSOI p-MOSFETs with zero back gate bias and small drain bias voltage.

Finally, the last part of our research work which is covering a significant part of the thesis, deals with the local variability phenomenon in advanced nano-scale devices. The main sources of drain and gate current local variability have been thoroughly studied. In this aspect, we developed a fully functional drain current mismatch model, valid for any gate and drain bias condition, including all main sources of drain current local variability assumed to be uncorrelated, namely the threshold voltage, the current gain factor, the source-drain series resistance and the subthreshold slope ideality factor mismatches. Concerning the gate current local variability modeling the local fluctuations of the threshold voltage and the gate oxide thickness were taken into account. The proposed models for the drain and gate current mismatch were verified, using a Lambert function based compact model and performing

Monte Carlo simulations that reproduce accurately the experimentally measured current variations. Then, owing to the proposed mismatch models, we characterized various advanced technologies in terms of local and global variability performance. Indeed, a detailed statistical characterization of drain current local and global variability in 14 nm Si bulk FinFET devices and in sub 15 nm gate length Si/SiGe trigate nanowire p-MOSFETs is performed. To this end, we extracted the main matching parameters showing that, despite their very aggressive dimensions, such devices exhibit relatively good local and global variability performance. Furthermore, we investigated the impact of the source-drain series resistance mismatch on the drain current variability for 28 nm Bulk MOSFETs. Finally, we performed a complete investigation of the gate and drain current mismatch in 14 nm FDSOI devices. In conclusion, these drain and gate current mismatch compact models can easily be implemented in circuit simulation tools for circuit design and are applicable to both bulk and FDSOI technologies. To this end, our drain current compact model implemented in Verilog-A code has been used to examine the impact of drain current variability on fundamental circuits in Cadence Spectre.

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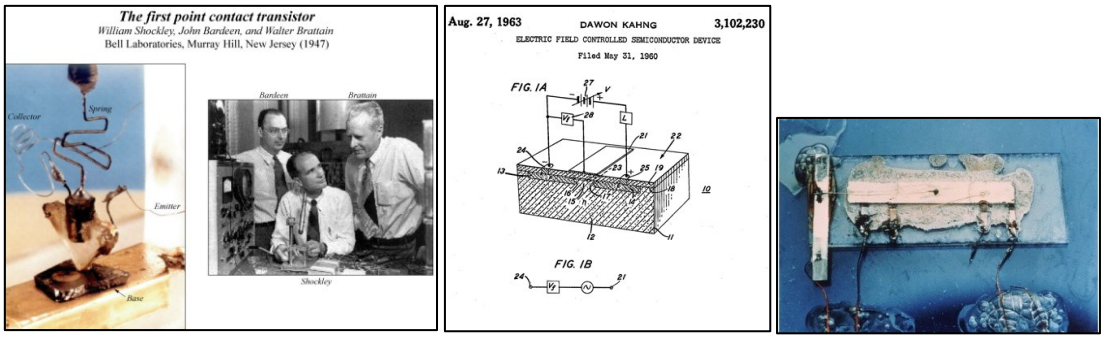
I Introduction

I.1 Overview of microelectronics evolution

Microelectronic components are the core elements of all modern technological devices that serve the needs of informatics, communications and audiovisual systems. They consist of conductor, semiconductor and insulator materials, arranged in a certain way to create new electrical properties. Although the first experiments on the electrical properties of semiconductor materials date back to the beginning of 19th century, the event that brought them on the edge was the invention of the Bipolar Junction Transistor (BJT) by W. Shockley, J. Bardeen and W. Brattain (Figure I-1(a)) at Bell Laboratories at the end of 1947 [1]. Almost ten years later, in 1959 D. Kahng and M. M. Atalla invented the Metal-Oxide-Semiconductor (MOS) Field Effect Transistor (FET) (Figure I-1(b)) as an offshoot to the already patented by J. E. Lilienfeld, FET design [2], [3]. At the same time, in September 1958 J. Kilby of Texas Instruments presented the first working Integrated Circuit (IC) (Figure I-1(c)) [4].



(a) **(b)** **(c)**

Figure I-1 The first working (a) BJT, (b) MOSFET and (c) IC.

Very soon, the successful development of the MOSFET led to the progress of the IC technology, since these devices were incorporated into integrated circuits in the early 1970s. Almost at the same period of time G. Moore estimated that the number of transistors per chip would double about every two years [5] (Figure I-2), since the idea was that smaller devices improve almost every aspect of an IC's operation, including the reduction of cost and switching power consumption per transistor, as well as the memory capacity and speed enhancement.

The semiconductor industry's need to transform Moore's observation into reality led to the creation of the International Technology Roadmap for Semiconductors (ITRS) in the early 90's. Therefore, the ITRS is a comprehensive guide produced by a group of semiconductor industry experts for advanced semiconductor device research and manufacturing purposes [6]. Since the first edition of the roadmap, the Moore's 'law' and the ITRS have been complementing each other. Even though Moore's 'law' has been successfully followed until recently, pursuing MOSFET scaling trend becomes more difficult as time passes. According to ITRS many challenges have to be overcome in order to continue progress to the same direction concerning the transistor's performance. Silicon (Si) remains the main semiconductor material for the time being but the required performance improvements for the end of the roadmap concerning high performance, low and ultra power applications as well as memories will lead to a substantial widening in the number of new materials, fabrication processes and device architectures used.

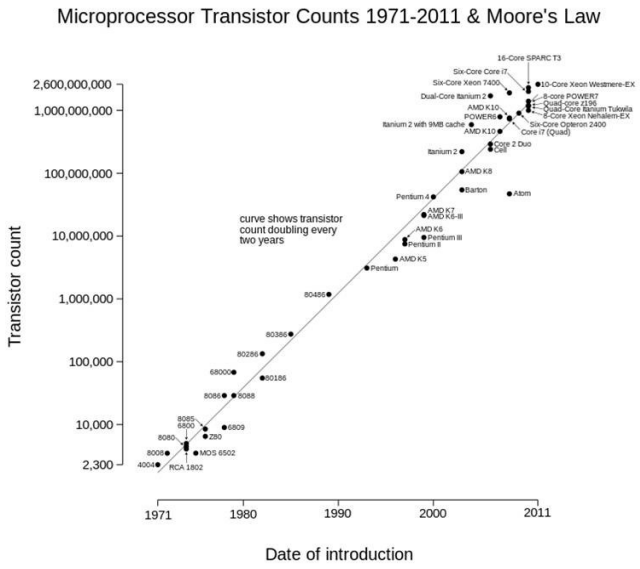


Figure I-2 Microprocessor transistor counts versus year plotted together with Moore's law.

I.2 Advanced nano-scale devices

It is clear that the main aspect in modern era microelectronics is concerning the device area: how to effectively reduce the device size without compromising its functionality [4] is the constant question in all electronic engineers' mind. The main advantage of reducing the transistor active area is the power consumption decrease since the voltage needed for the device operation is reduced accordingly to its size [7], [8]. On the other hand, loss of electrostatic control [9], mobility degradation [10], [11], short-channel effects (SCEs), and inability of further reducing the series resistance are some of the main disadvantages arising from the device shrinking. Finally, variability and reliability issues are also other crucial impacts of reducing the MOSFET area. These latter issues are addressed by the present work.

To address the problems mentioned above, various technological concepts have already been absorbed and used from transistor technology. Planar bulk silicon MOSFET has been the traditional workhorse of the semiconductor industry to achieve continuous scaling. However, bulk planar FETs suffer from SCEs as the electric field lines propagate through the depletion regions associated with the junctions (Figure I-3(A)). To overcome this problem Silicon-On-Insulator (SOI) substrates have been proposed. Indeed, these devices are interesting candidates for the manufacturing of mainstream semiconductor products like microprocessors or low-power devices [12]. As illustrated in Figure I-3(B) in a fully depleted SOI (FDSOI) device, most of the field lines propagate trough the buried oxide (BOX) before reaching the channel region. However, the improvement regarding the SCEs in FDSOI devices depends on device parameters such as the silicon film thickness, buried oxide thickness, and doping concentrations. With reducing the BOX thickness from the typical 145-300 nm value down to 8-25 nm, the device is called ultra-thin body and buried-oxide (UTBB) FDSOI MOSFET [13]. The silicon film thickness can vary from around 7 to 14 nm. Another solution contributing to the reduction of SCEs in FDSOI MOSFETs is the addition of a thin buried oxide layer and an underlying ground plane. In that case, most of the electric field lines from the source and drain terminate on the buried ground plane instead of the channel region (Figure I-3(C)).

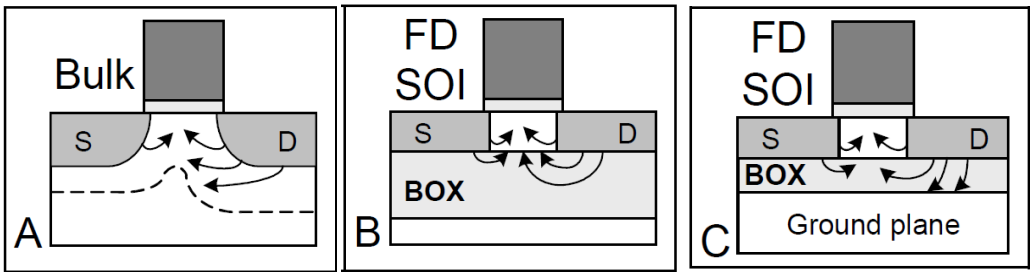


Figure I-3 Electric field lines from source (S) and drain (D) on the channel region in (A) bulk, (B) FDSOI and (C) FDSOI with thin buried oxide and ground plane MOSFETs [14].

In Figure I-4 the "Smart Cut" fabrication process for manufacturing ultrathin SOI wafers is illustrated, achieving a complete division between an ultrathin film of single crystalline silicon and the bulk substrate [15].

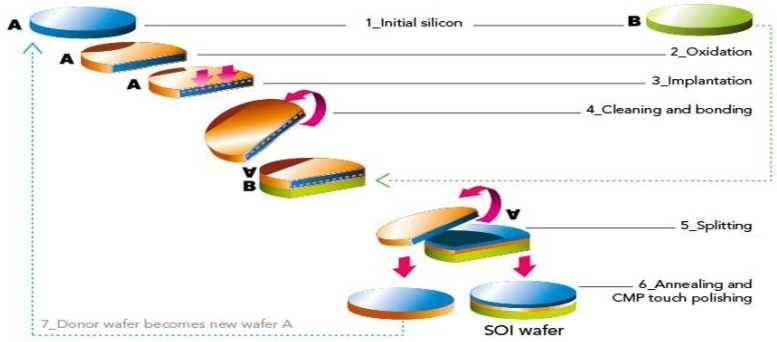


Figure I-4 Fabrication process of manufacturing ultrathin SOI via Smart Cut process [15].

Furthermore, other technological solutions suggested and applied in order to maintain the level of performance while shrinking down the device area, include:

- ✓ Gate stacks consisting of more than two material layers combined with high-k materials, like hafnium oxide HfO_2, instead of SiO_2 as gate insulators to decrease tunneling leakage current and increase gate capacitance [16].
- ✓ Techniques like substrate rotation, stress or strain to improve mobility [17], [18].
- ✓ Insertion of Halo implants near the drain and source contacts [19] in order to eliminate the SCEs and drain-induced barrier lowering (DIBL) effect.
- ✓ Shallow trench isolation (STI) technique [20] to electrically isolate one device from the other and thus to prevent leakage currents.

In Figure I-5 a typical bulk and an FDSOI MOSFET fabricated by ST Microelectronics in France are presented. This PhD thesis is addressing various new technologies, among which the 28 nm and 14 nm FDSOI technologies as well as the 28 nm bulk technology.

Another configuration, proposed for the first time in 1984 [22] and considered to be a further promising candidate to have a larger immunity for SCEs compared to classical single planar gate devices is the multi-gate structure. Indeed, multi-gate devices (double, triple, quadruple, and gate all around structures presented in Figure I-6) provide several advantages such as enhanced gate controllability, increased gate-drive current, reduced sub-threshold swing and subsequently suppressed gate leakage current, reinforced pinch off effects, and

improved process reliability [9], [23]. On the other hand, however, there are technological and economical challenges such as the fabrication cost and process complexity that make these devices not as compatible as conventional bulk planar CMOS devices.

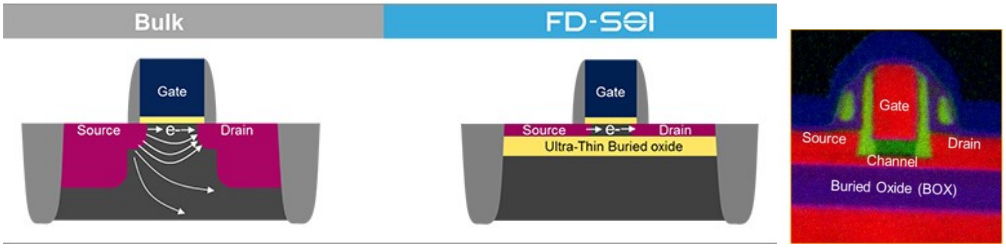


Figure I-5 Representation of a (a) bulk and an (b) FDSOI MOSFET fabricated by ST Microelecronics. In (c) a scanning electron microscopy (SEM) cross section of an FDSOI MOSFET is presented. [21]

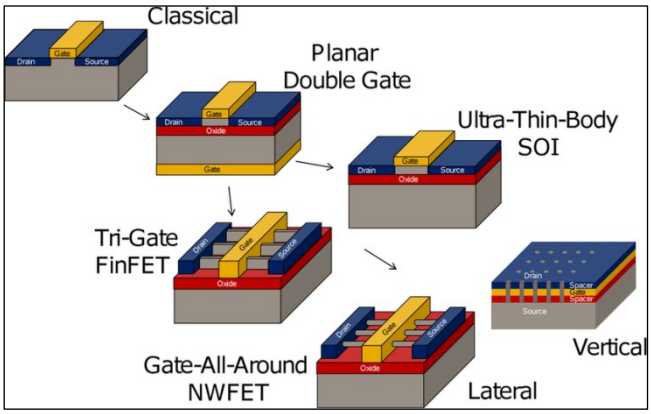


Figure I-6 Evolution of the field effect transistor Architecture [24].

Furthermore, another design idea that seems to prevail over the bulk CMOS technology is the Fin-Shaped FET (FinFET). As illustrated in Figure I-7 in FinFET devices, where the channel width plays here the role of t_{Si}, the body has a fin-like shape and is surrounded by the gate electrode. Due to this design SCEs can be well suppressed, demonstrating lower DIBL [25] and enhanced field-effect mobility [26]. Nevertheless, as FinFETs are three-dimentional (3D) devices, they demonstrate additional challenges for manufacturing and circuit design [27].

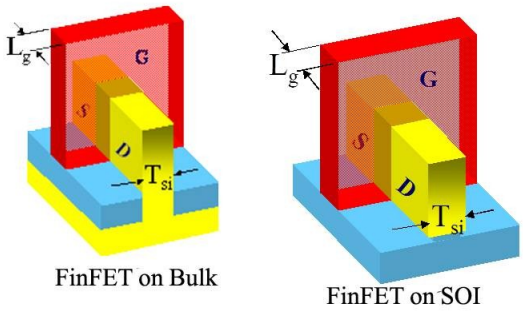


Figure I-7 Representation of a FinFET device on bulk and SOI substrates.

Finally, tri-gate nanowire (NW) MOS transistors are nowadays recognized as promising architectures for continuing the scaling down beyond FinFET and FDSOI CMOS technologies [28], [29], [30]. By wrapping a gate around the NW, the optimal control of the NW conduction by the gate potential is ensured. A large number of techniques exist to

fabricate silicon nanowires, that can be classified into bottom-up and top-down fabrication techniques. Superior gate control, immunity of threshold voltage from substrate bias and excellent carrier transport properties along with more aggressive channel length scaling possibility have made gate-all-around (GAA) architecture with semiconductor NW channel a potential candidate for post-planar transistor design.

I.3 Impact of scaling on the device performance

In order to achieve performance improvement, reduced power consumption and higher-density integration by shrinking down the device dimensions, major reliability and variability issues have emerged. The first case includes phenomena like hot carrier injection (HCI), and negative bias temperature instability (NBTI), while the second one, as indicated from the term, variations of the main device parameters. These reliability mechanisms cause drifts in the MOS transistor parameters; namely, threshold voltage shift and mobility degradation. Additionally, dispersions in device level are propagated on a circuit level (e.g. SRAM) leading to reduced circuit performance and functionality. Consequently, it is evident that the study of these issues is considered of great importance and this is the reason they cover a large part of the present thesis. Before analyzing these phenomena, some basic elements of the MOS device reliability and variability are described.

I.3.1 Reliability issues in MOSFETs

I.3.1.1 Negative Bias Temperature Instability

Bias Temperature Instability (BTI) is a phenomenon that introduces a significant reliability issue in advanced devices and in circuit operation. It occurs when the device is subjected to elevated temperatures (0°C to 300°C) and high gate voltages (creating electric fields up to approximately 10 MV/cm) while the remaining MOSFET terminals are grounded [31]. These conditions, usually referred to as stress, have detrimental effects on the device characteristics, as they result in positive charge built-up in the gate insulator causing shift in device parameters, like for example in the threshold voltage or in the sub-threshold slope. However, as soon as the stress conditions are removed, the device characteristics are found to recover, meaning that the device parameters slowly revert towards their initial values. The effect has been identified to be stronger in p-type transistors under negative bias conditions and this is the reason it is called NBTI.

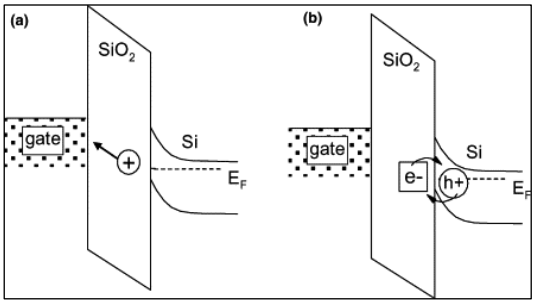


Figure I-8 Effect of negative gate bias on MOS capacitor. (a) Positive ion drift causes a reduction in the net amount of positive charge near the Si/SiO_2 interface. The resulting flat band shift is positive. (b) Charge exchange with the Si substrate, either hole trapping or electron detrapping causes an increase in the net positive charge at the Si/SiO_2 interface. The resulting flat band shift is negative [32].

As indicated in Figure I-8, at first the phenomenon was remarkable as an increase in positive charge under negative gate bias implicated a mechanism distinct from the migration of mobile ions which were of much concern [32].

Although this phenomenon is not a new topic - it was first reported in 1966 [33] - there are still significant issues to study concerning the nature and modeling of NBTI, especially in advanced nano-scale devices.

I.3.1.2 Hot Carrier Injection

At small channel dimensions, the electric fields are high near the drain region resulting in hot carrier (HC) degradation issues. First of all, by using the term "hot" we mean that the mean carrier energy is significantly larger than that associated with the lattice in thermal equilibrium, namely $E>(3/2)kT$. Indeed, electrons (or holes) can gain enough energy passing through high electric fields so that they are injected into normally "forbidden" regions of the device, as the gate dielectric, where they can get trapped or lead to generation of interface traps at the silicon-oxide interface known as fast surface states. As a result, MOSFET parameters such as threshold voltage, sub-threshold swing and on-current will be modified limiting the lifetime of the transistor and causing degradation of the ICs performance.

In general, hot carriers can be introduced into the gate dielectric with 4 different mechanisms [34]:

1. Channel HC injection
2. Drain avalanche HC injection
3. Secondary generated HC injection
4. Substrate HC injection

In this thesis we are interested mainly in the first case, illustrated in Figure I-9 where some "lucky" carriers [35] flowing in the MOSFET inverted channel ($V_{gs}>V_t$), gain significant energy beyond the channel pinch-off point [31].

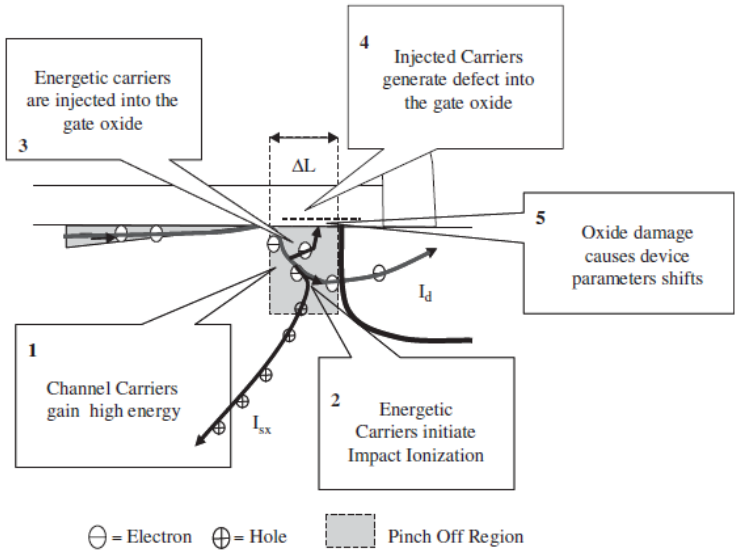


Figure I-9 Physical mechanisms participating in the channel HC induced device degradation in MOSFET in saturation [31].

I.3.2 Variability issues in MOSFETs

As new technology nodes with their decreasing geometries come into existence, process variations in general and especially intra-die (differences between areas on the same die) and inter-device (differences between "matching" pair devices on the same die) variations become increasingly significant. As shown in Figure I-10, process variations, which are observed at several levels and in one way or the other, are related to distance, can be categorized into global and local variations.

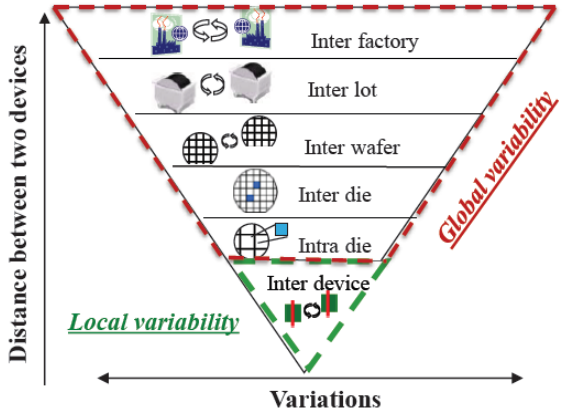


Figure I-10 Variability at several levels [36].

Additionally, local variability, usually referred to as mismatch, can be further divided into systematic and stochastic. Systematic mismatch stems from sources that can be predicted, like asymmetries in layout [37] and therefore it can be reduced to a certain degree by following more mismatch-aware practices, like for example use of "dummies" in MOS transistors conception [38].

On the other hand stochastic variations arise from intrinsic sources of random dispersions within the devices. This means that these variations stem from the random nature of processing steps in general, for example due to the discrete nature of dopant impurities or point defects. Stochastic fluctuations are independent of the distance between the devices under study, and by this they determine the maximal obtainable accuracy within a certain technology [39]. In this work, we study the stochastic fluctuations of the MOSFET and from this point on we will refer to this kind of fluctuations as mismatch or local variability.

In general, the physical mechanisms that are responsible for these local fluctuations were identified as: 1) doping fluctuations in the channel, 2) doping fluctuations in the gate, which are enhanced by the poly-grain structure of the gate material, 3) fluctuations in fixed-oxide charge, 4) fluctuations due to Coulomb scattering and 5) fluctuations due to surface roughness scattering. These mechanisms affect transistor behavior by influencing: 1) the threshold voltage, 2) the amount of gate depletion, 3) the magnitude of quantum mechanical effects, 4) the effective field, 5) the amount of carrier screening and 6) the mobility in general. It was found that none of the above mentioned effects can safely be neglected [39].

Concerning the research on the mismatch phenomenon, the majority of the works done dates from 1998 and beyond. The first mismatch studies, however, demonstrating that local fluctuations on MOSFET operation need to be taken into account for accurate modeling of the weak inversion current, were conducted in 1973 by Van Overstraeten, Declerck and Broux [40]. Keyes study in 1975 was focused on the creation of a model to predict the amplitude of the threshold voltage variations, without considering the MOSFET operation

[41]. One of the most referred to the literature and popular studies has been realized by Pelgrom in 1989 who translated the mismatch in MOSFET parameters into a mismatch in the drain current [42]. Indeed, in this work a direct dependency was demonstrated between the local fluctuations of an electrical MOSFET parameter and the channel area through a coefficient A. This way, the so-called Pelgrom's Law was derived:

"*The standard deviation of the local variability of a MOSFET parameter is found to be inversely proportional to the square root of the device area.*"

These preliminary studies, in combination with the shrinking of the device dimensions, have set the ground for increasing research efforts aimed at achieving a deeper understanding of the causes of mismatch phenomena and characterizing their effects, with the objective of guaranteeing reliable integrated circuits performance.

I.4 Necessity of compact modeling in MOSFETs

Device models are essential tools for electronics engineers in order to design and simulate electronic systems. All integrated circuit designs are verified using circuit simulators before being reproduced in real silicon since detecting errors early in the design process avoids the costly and time consuming prototyping. The first circuit simulator, SPICE (Simulation Program with Integrated Circuit Emphasis), was developed in 1973 by Laurence Nagel of University of California, Berkeley [43]. Since then, many advanced circuit simulators have been developed such as HSPICE (Avant!), SSPICE (Silvaco) or SPECTRE (Cadence), with a single goal of reducing the time-to-market for IC designs.

Electronic circuit simulations demand clearly defined requirements in order to predict the performance of a CMOS design. First of all, the simulator should be user-friendly, fast and precise. Second, it should utilize accurate models which are capable to describe the behavior of the transistors in the circuit. It is obvious that most of the requirements are related to the device models the simulator applies. Besides, device models form a bridge between the design world and the manufacturing world with which the designers can design circuits without worrying about the intricate details of transistor fabrication. The goal of a device model is to accurately predict the transistor's electrical characteristics - terminal currents, charges and capacitances for a given transistor bias and transistor temperature.

In general, device models can be divided in three groups [44]:

- Numerical device models
- Table look-up models
- Analytical (or compact) models.

Concerning the first group, there are two- and three-dimensional numerical models [45]. Both of them use device geometry, doping profiles, and carrier transport equations, which are solved numerically, to get the device electrical characteristics. The main disadvantage of this kind of models is that they are computationally intensive and thus they are not applied for large circuits' simulations. Regarding the table look-up models, the measured device current and capacitance are presented as functions of bias voltages and device sizes in a tabular form for access by the circuit simulators [46]. A disadvantage of this second category is the need of extensive measurements and large set of tables so that the

models cover a large range of transistor geometry, bias and temperature. Secondly this kind of models is based on measured data from measured devices making them non-predictive.

The most popular and appropriate for circuit simulations models are those described by the third group. Indeed, compact device models describe the device characteristics of a manufacturing technology by a set of physics-based analytical expressions with technology-dependent device model parameters that are solved by a circuit simulator for circuit analysis during IC design [47]. As illustrated in Figure I-11, a compact model consists of a core model -describing the drain current and capacitance behavior of the device or more precisely of the MOSFET of a specific technology- along with the various models to account for the effects of the geometry and physical phenomena in the device. The compact model equations are almost always long and complex as they describe the device characteristics accurately in all the operation regimes [48], [49], [50], [51]. Moreover, to improve the accuracy of the model fitting parameters are introduced.

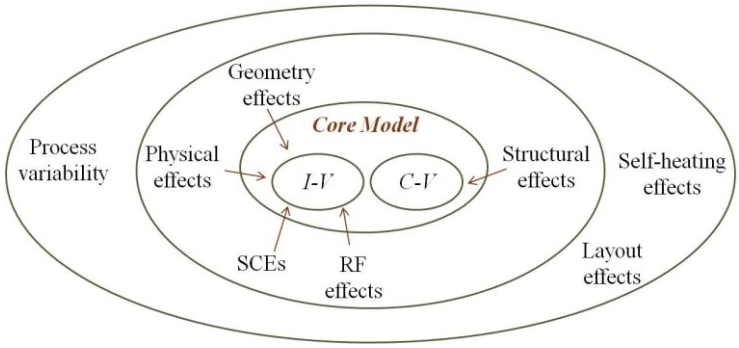


Figure I-11 A typical composition of a compact model of a specific technology: the core model includes the basic behavior of a large area device and is accompanied by models for physical phenomena within the devices and geometry and other structural effects, while the final compact model includes all the external phenomena like process variability or layout effects.

Compact models can be further categorized in:

- Threshold-voltage-based models,
- Surface-potential-based models
- Charge-based models.

Threshold-voltage-based modeling is founded on the computation of the inversion charge density in the MOSFET channel in terms of the terminal voltages, namely gate and drain voltages [52]. In this approach a linear approximation is made between the surface potential and the applied drain and gate voltages. This eliminates the surface potential and relates the input gate voltage to the output drain current giving a relatively simple current-voltage equation. In these models all the main parameters are defined based on the threshold voltage and this is the reason they are called "threshold-voltage-based" models. The initial version of SPICE models falls into this category. The main advantages of these models are the simplicity and flexibility to add features resulting from technology advancements. Unlike the surface-potential-based models based on internal quantities (like potentials etc.), the threshold-voltage-based models based on experimentally measured external quantities (like threshold voltage, ideality factor) are expected to be more efficient for low-frequency noise (LFN/RTN), reliability (NBTI/HCI) and variability compact modelings.

Concerning the charge-based-models, the current is formulated in terms of the inversion charge density at the source and drain ends of the channel. EKV model [53] for example falls into this category.

Finally, the surface-potential-based models are based on the calculation of the channel potential, as indicated by the term. Although accurate MOSFET device physics is applied in such models -thus they are more accurate than threshold-voltage-based models- difficult and complex iterative techniques are required to solve the implicit relations of the surface-potentials making them unpractical.

To conclude, it is obvious from all the above that in general, the use of compact models -regardless of the category they fall into- in circuit simulators allows the optimization of circuit performance for robust IC design and cost-effective IC products. This optimization is getting more and more difficult as device area is shrinking down. As already mentioned in the previous sections phenomena like SCEs, variability and reliability issues become critical for such advanced devices, making extremely difficult and hard the understanding and prediction of the performance of VLSI circuits containing billions of nano-scale devices. Therefore nowadays the main motivations for compact model development include [47]:

- ✓ Improving design efficiency using compact models instead of measured data from billions of transistors with different dimensions operating under different voltages that are used in an IC chip.
- ✓ Bypassing the conventional manual techniques for design and analysis of today's complex VLSI circuits.
- ✓ Designing an IC chip under the worst case conditions in order to examine the manufacturing tolerances before the production.
- ✓ Design-for-reliability enabling designers to predict and optimize circuit performance.
- ✓ Design-for-variability performing statistical analysis to optimize circuits in terms of the induced variability to circuit level.

I.5 Dissertation goals and outline

The progressive scaling-down of CMOS technology has driven the semiconductor industry for the realization of faster and lower power consumption VLSI circuits and systems. Currently, silicon technology has entered the nano-CMOS era with 28 nm gate length MOSFETs in mass production, while sub-10 nm transistor is scheduled for production within 2017 [54], [55]. FDSOI transistors and FinFETs are the most promising architectures for scaling CMOS devices down to nanometer size, since they allow a significant reduction of the short channel effects. This dissertation seeks to contribute towards the development of generic simple and accurate compact models for advanced nano-scale MOSFETs and more precisely for FDSOI MOSFETs, suitable for incorporation into design tools, enabling the circuit designers to make projections beyond the available scaled dimensions and also to achieve device/circuit co-optimization. In this thesis we have decided to mainly study the FDSOI technology, because apart from the direct access to different FDSOI technologies, these devices offer efficiency in many levels. Compared to the fin-shaped field-effect transistors, the UTBB FDSOI technology has a much simpler fabrication process, thanks to its planar structure. Furthermore, its back-gate bias option makes it particularly interesting for multi-V_t applications. Nevertheless, as already stated, at the same time serious reliability and performance issues emerge in such advanced nano-scale CMOS technologies. Besides the reliability phenomena, another challenge faced by researchers chasing the "scaling trend" is the transistor local variability.

Consequently, the motivations of this dissertation on the key issues arising from the scaling of new-era devices in the modern MOSFET design are two: the development of an analytical and compact drain current model, valid from weak to strong inversion, below and above threshold describing accurately the transfer and output characteristics of short-channel FDSOI devices and the investigation of reliability and variability issues of such advanced nano-scale transistors.

Chapter II provides a more detailed theoretical and technical background for better understanding of this dissertation, focusing on the critical MOSFET electrical parameters and the techniques for their extraction. More precisely, it demonstrates the so-called Y-Function and Split-CV methodologies for electrical characterization in diverse types of semiconductor devices based on current-voltage (I-V) and capacitance-voltage (C-V) measureremnts. The influence of AC signal oscillator level on the effective mobility measurement by split C-V technique in MOSFETs is also analyzed. Additionally, a new methodology allowing the extraction of MOSFET parameters is presented, based on the Lambert W (LW) function for the inversion charge which is valid over the full gate voltage range, i.e. from weak to strong inversion region and from linear to saturation region. At the end of the chapter, some fundamental issues concerning characterization of the low-frequency noise (LFN) in MOSFETs are described.

Chapter III presents the analytical drain current compact modeling in nanoscale FDSOI MOSFETs. First, simple analytical models for the front and back gate threshold voltages and ideality factors have been derived in terms of the device geometry parameters and the applied bias voltages with back gate control. Then, an analytical compact model for the drain current has been also developed for lightly doped short-channel UTBB FDSOI MOSFETs with back gate control, accounting for small geometry and other significant in such technologies effects like, saturation velocity, mobility degradation, quantum mechanical, velocity overshoot and self-heating effects. Finally, the drain current compact model is implemented via Verilog-A code for simulation of fundamental circuits in Cadence Spectre.

Chapter IV is dealing with reliability issues in FDSOI transistors. The hot-carrier degradation of nanoscale UTBB FDSOI n-MOSFETs has been investigated under different drain and gate bias stress conditions. The degradation mechanisms have been identified by combined LFN measurements at room temperature in the frequency and time domains. Additionally, the impact of the HC degradation on the device parameters has been expressed with semi-empirical models in terms of the stress time, channel length, drain bias and gate bias. Based on our analytical compact model of Chapter III, an HC aging model is proposed enabling to predict the device degradation stressed under different bias conditions, using a unique set of few model parameters determined for each technology through measurements. Finally, the NBTI stress characteristics and the recovery behavior under positive bias temperature stress of HfSiON gate dielectric UTBB FDSOI p-MOSFETs have been investigated. A model for the NBTI has been developed by considering hole-trapping/detrapping mechanisms, capturing the temperature and bias voltage dependence.

In Chapter V, studies of variability issues in advanced nano-scale devices are presented. The main sources of drain and gate current local variability have been thoroughly studied. First, the impact of the source-drain series resistance mismatch on the drain current variability has been investigated for 28 nm Bulk MOSFETs. A mismatch model that takes into consideration the source-drain series resistance local variability has been developed and

used to extract all mismatch parameters, including $\sigma(\Delta V_t)$, $\sigma(\Delta\beta/\beta)$ and $\sigma(\Delta R_{sd})$, in the linear and saturation regions. Then, a detailed statistical characterization of the drain current local and global variability in sub 15 nm Si/SiGe tri-gate nanowire p-MOSFETs and in 14 nm Si bulk FinFETs has been conducted. The main local and global variability MOSFET parameters ($\sigma(\Delta V_t)$, $\sigma(\Delta\beta/\beta)$, $\sigma(\Delta R_{sd})$ and $\sigma(\Delta n/n)$) have been extracted owing to a generalized analytical mismatch model valid in linear region. Finally, a complete investigation of the gate and drain current mismatch in advanced FDSOI devices has been performed. In this aspect, a fully functional drain current mismatch model, valid for any gate and drain bias condition has been developed. Finally, the drain current compact model of Chapter III implenteded in Verilog-A code has been used to examine the impact of drain current variability on fundamental circuits in Cadence Spectre.

An overall summary of this dissertation is presented in Chapter VI, which highlights the key research contributions and future research directions are suggested.

II Characterization techniques and parameter extraction

II.1 Introduction

In this chapter, firstly the basic structure of a MOSFET and the modes of operation are briefly described in Section II.1, assuming that the fundamental semiconductor concepts are already known. Next, using the long-channel MOS model, the expression of drain current as a function of the applied voltage bias is presented in Section II.2. In view of the fact that the accurate determination of the MOSFET electrical parameters is essential for understanding the physics and engineering of the devices, particularly for advanced ultra-scaled devices, the powerful and useful Y-function method is analyzed in Section II.3 [56]. Furthermore, the concept of the new modified Y-Function method for parameter extraction of nanoscale MOSFETs is recalled.

Concerning the extraction of the intrinsic MOSFET parameters, like oxide thickness t_{ox}, oxide capacitance C_{ox}, effective mobility μ_{eff} and doping concentration (N_D for n-MOS or N_A for p-MOS), the well-known split C-V method is presented in Section II.4. However, especially regarding the extraction of μ_{eff}, this methodology always leads to underestimated mobility values below threshold voltage [10], [57], [58], [59], [60], [61], [62]. A too large amplitude of the drain voltage, V_d could be one of the reasons for this collapse below threshold due to the extreme non linear $I_d(V_d)$ characteristics in weak inversion [59]. Another reason could reside in a systematic difference between the threshold voltage of the inversion charge Q_i (deduced from gate-to-channel capacitance C_{gc}) and drain current transfer characteristics, yielding overestimation of the real inversion charge [59], [60], [62]. Within this context, one of the aims of this section is to investigate how the μ_{eff} extraction is influenced by the AC signal oscillator level used by the impedance meter to measure the gate-to-channel capacitance of the MOS transistor. Indeed, as with the amplitude of the drain voltage in I_d measurement, a too large AC signal level could induce a significant overestimation of the gate-to-channel capacitance below threshold due to the strong non linearity (exponential dependence) of inversion charge variation with gate voltage.

In Section II.5 a new MOSFET parameter extraction methodology is presented, which is based on the Lambert W function and allows the exploitation of the full gate voltage range i.e. from weak to strong inversion region, enabling to fully capture the transition between subthreshold and above threshold region, despite the reduction of supply voltage. A lot of methods have been proposed for the MOSFET parameter extraction - one of the most popular will be described in Section II.3 - but they are generally restricted to the above threshold region and mostly assume that the inversion charge varies linearly with gate voltage overdrive [56], [63], [64], [65], [66], [67], [68], [69], [70], [71], [72]. As the supply voltage V_{dd} is reduced with device scaling, the operating gate bias moves closer to the threshold voltage (near threshold operation), and the assumption that the inversion charge varies approximately linearly with gate voltage overdrive becomes less and less accurate. Few attempts to extend the parameter extraction from above to near threshold region was carried out using $g_m/I_d(V_g)$ derivative [73], Lambert W function [74] or logarithmic function [75] of gate voltage overdrive for the inversion charge control, but it was not applied to the entire gate voltage range from weak to strong inversion. To this end, we first validate the usefulness of the LW function to describe accurately the gate-to-channel capacitance characteristics $C_{gc}(V_g)$, and, by turn, the MOSFET inversion charge $Q_i(V_g)$ from weak to strong inversion region. Then, in conjunction with the conventional mobility expression, we apply this

analytical $Q_i(V_g)$ law for the parameter extraction in advanced MOS devices from a 14 nm FDSOI CMOS technology. Finally, the new methodology has been validated for a wide range of back bias voltage and different channel lengths.

In order to characterize the quality and reliability of MOS transistors, low-frequency noise characteristics are rated especially important, since they can provide information like the oxide trap distribution and density, as well as the carrier scattering mechanisms. Furthermore, the scaling down of the transistors has led to the observation of a new type of noise, namely the random telegraph signal noise (RTN) due to individual carrier trapping at the silicon-oxide interface. To this aspect, the fundamental noise mechanisms as well as the basic LFN/RTN models used for the characterization of MOSFETs will be discussed in Section II.6.

II.2 Basic operation of bulk MOS transistors

In this section the basic MOSFET operation principles will be recalled. MOSFET is a device where minority carriers (electrons for an n-MOS or holes for a p-MOS) flow in a conducting channel between the source and the drain creating current which is controlled by a voltage applied to the gate. Figure II-1 presents the basic structure of a bulk n-MOS transistor. The description that follows refers to the operation of the n-MOSFET, since the p-MOSFET operates in just the opposite way concerning the carriers and the polarizations. As shown in Figure II-1, the structure consists of three layers and four terminals, namely the Drain, Source, Gate and Substrate terminals. Regarding the first layer, the preferred gate material initially was the polycrystalline silicon. Nevertheless, metal gates with a high-k dielectric are used in modern CMOS transistors. The intermediate layer constitutes the dielectric layer which separates the gate terminal from the underlying source and drain terminals as well as the conducting channel that connects source and drain when the transistor is on, as is explained below. Finally, the last layer is the doped silicon body where the conducting channel will be developed.

As can be seen, the body is grounded and a voltage, V_g is applied to the gate. In case the applied voltage is negative (Figure II-1(a)), negative charges will be gathered in the gate while holes will be accumulated beneath it. Thus, this mode of operation is called accumulation mode. If a small positive gate voltage is applied (Figure II-1(b)) then we proceed to the depletion mode, where some positive charges will be gathered in the gate, while beneath the gate a layer without charges will be developed. Finally, if the applied gate voltage range is sufficient (Figure II-1(c)), namely $V_g > V_t$ where V_t is a critical gate voltage value, more positive charges will be attracted to the gate, consistuting an inverted charge with regards to the initial p-type substrate, this is the reason it is called inversion layer.

Figure II-2 demonstrates an n-MOS transistor and its three regions of operation, namely the *cutoff*, *linear* and *saturation* regions. When the gate-to-source voltage, V_{gs}, is lower than the threshold voltage, V_t, the transistor is in the *cutoff* or *subthreshold* mode of operation (Figure II-2(a)). At this state, the source and drain have free electrons, while the body has free holes [76]. If the source is grounded and the body and drain or source junctions are zero-biased or reverse-biased, the electron charge is small and the drain current is called *subthreshold current* [77], [78]. Only for reasons of simplicity, this current can be sometimes approximated equal to zero.

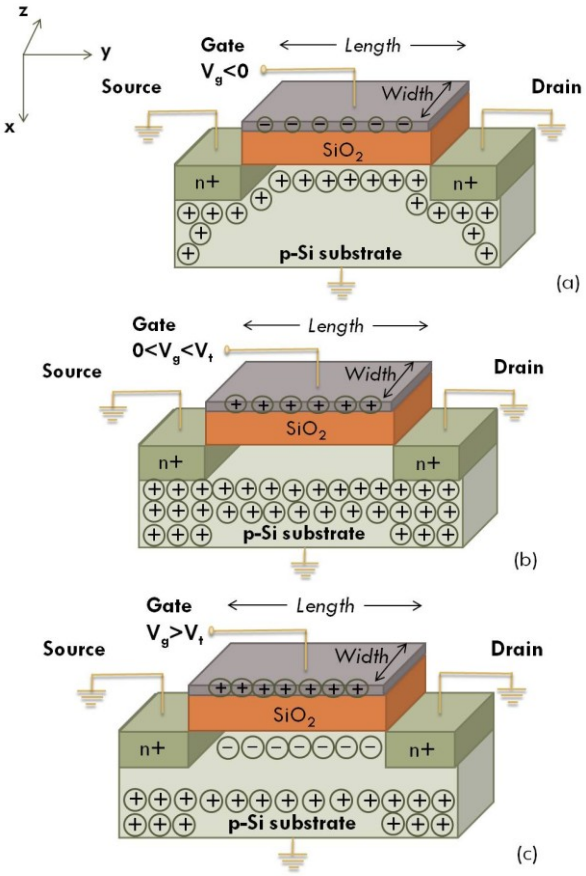


Figure II-1 n-MOS structure illustrating the accumulation (a), depletion (b) and inversion (c) modes of operation.

When V_{gs} is greater than V_t, the *channel* is formed and connects the source and drain current depends on both the gate and drain voltage, is called *linear* or *triode*. If the drain-to-source voltage, V_{ds} is zero (Figure II-2(b)), there is no electric field to push the drain current from drain to source. But as V_{ds} increases Figure II-2(c), drain current flows through the channel from drain to source. While V_{ds} continues increasing, there is a critical value of drain-to-source voltage, $V_{ds,sat}$ in which the gate-to-channel voltage at the drain end, V_{gd} becomes equal to V_t. Under this condition, namely at $V_{ds}= V_{gs} - V_t$ we say that that the channel is *pinched off* (Figure II-2(d)). Above this drain voltage the channel depends only on the gate voltage and the transistor is in *saturation* or *active* mode of operation.

Mathematically, in order to produce the basic drain current equations for every region of operation, the MOSFET gradual channel approximation is used. According to this, if a drain voltage, V_{ds} is applied, then the voltage along the channel, U_c varies. Consequently, at every position x (see Figure II-1(a)) of the channel, a channel voltage U_c is applied, implying that the charge density in the inversion layer, Q_i also varies along the channel. Thus, we have:

$$I_d(V_{ds},V_{gs}) = W\, Q_i(V_{ds},V_{gs})\,\mu_{eff}\,\frac{dU_c}{dx} \;\Leftrightarrow\; I_d(V_{ds},V_{gs}) = \int_0^{V_{ds}} \frac{W}{L}\, Q_i(V_{ds},V_{gs})\,\mu_{eff}\, dU_c \qquad \textbf{Eq. II.1}$$

where W is the channel width and μ_{eff} the effective mobility defined in the next paragraph.

In subthreshold region, namely in weak inversion where $V_{gs}<V_t$, the charge in the channel will be [79]:

$$Q_i(V_{ds},V_{gs}) = Q_{i0}(V_{ds},V_{gs})e^{\frac{q}{kT}U_C} \qquad \textbf{Eq. II.2}$$

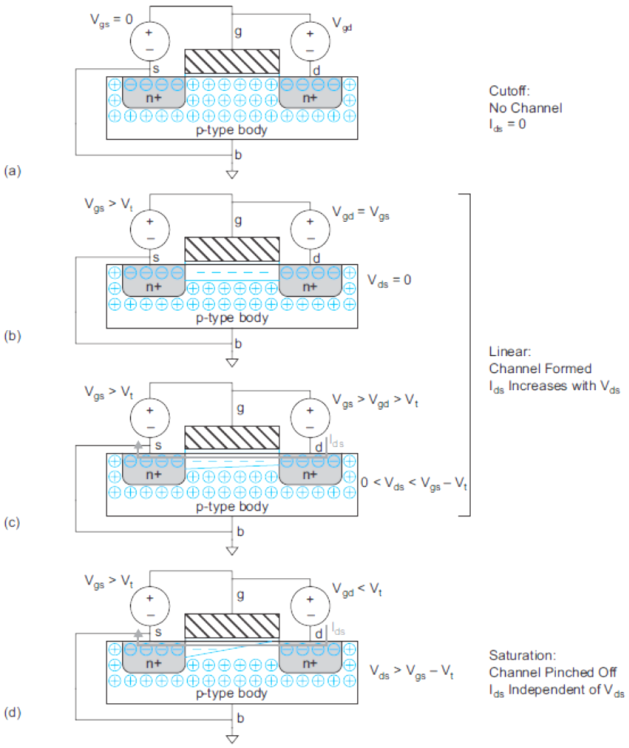


Figure II-2 n-MOS transistor demonstrating cutoff, linear and saturation regions of operation [76].

Yielding to the exponential drain current equation in weak inversion:

$$I_d(V_{ds},V_{gs}) = I_{d0}\left(1 - e^{\frac{q}{kT}V_{ds}}\right) \qquad \textbf{Eq. II.3}$$

In strong inversion where $V_{gs}>V_t$, we have for the inversion charge:

$$Q_i(V_{ds},V_{gs}) \approx -C_{ox}(V_{gs} - V_t - U_c) \qquad \textbf{Eq. II.4}$$

And thus, we obtain the following two equations for the drain current in linear and saturation region, respectively:

$$I_d(V_{ds},V_{gs}) = \frac{W}{L}\cdot\mu_{eff}\cdot C_{ox}\cdot(V_{gs}-V_t)\cdot V_{ds} \quad \text{if } V_{ds} < V_{gs}-V_t \qquad \textbf{(a)}$$

$$I_d(V_{gs}) = \frac{W}{2\cdot L}\cdot\mu_{eff}\cdot C_{ox}\cdot(V_{gs}-V_t)^2 \quad \text{if } V_{ds} \geq V_{gs}-V_t \qquad \textbf{(b)}$$

Eq. II.5

II.2.1 Effective Mobility

As it has been already mentioned, the presence of V_{ds} creates a lateral electric field along the channel. Therefore, due to this field, each carrier in the channel is accelerated to an average velocity, v, which will be proportional to it:

$$v = \mu \cdot E \qquad \textbf{Eq. II.6}$$

where μ is a constant called *mobility* [80]. When strong lateral or vertical electric field is applied, Eq. II.6 is no longer valid since degradation in the carriers' effective mobility is observed.

Mobility degradation in the linear region of operation can be modeled by replacing μ with a smaller μ_{eff} that is a function of V_{gs}:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1\left(V_{gs} - V_t\right) + \theta_2\left(V_{gs} - V_t\right)^2} \qquad \textbf{Eq. II.7}$$

where μ_0 is the *low-field mobility*, and θ_1 and θ_2 are the first and second order mobility attenuation factors [81]. Parameter θ_1 describes the phonon scattering due to enhanced confinement and larger wave function overlap integrals, while θ_2 describes the surface roughness scattering.

Concerning the saturation region where higher electric fields are applied the carriers gain considerable energy from the field so that their velocity reaches a value, the so-called saturation velocity, v_{sat}. This effect can be introduced to the effective mobility as follows:

$$\mu_{eff} = \frac{\mu_0}{1 + \mu_0 \dfrac{V_{ds}}{L \cdot v_{sat}}} \qquad \textbf{Eq. II.8}$$

II.2.2 Source-Drain Series Resistance

Another component which has an important impact on the drain current is the *Source-Drain (SD) Series Resistance, R_{sd}*. As the channel length is scaled down, the R_{sd} (R_{sd}= R_s+ R_d) contributes more and more to the total device resistance, R_{tot} (R_{tot}= R_{ch}+ R_s+ R_d) as indicated in Figure II-3. At this point it should be mentioned that source resistance R_s and similarly drain resistance R_d, include all the parasitic resistance elements related to the source and the drain respectively, as presented in Figure II-4.

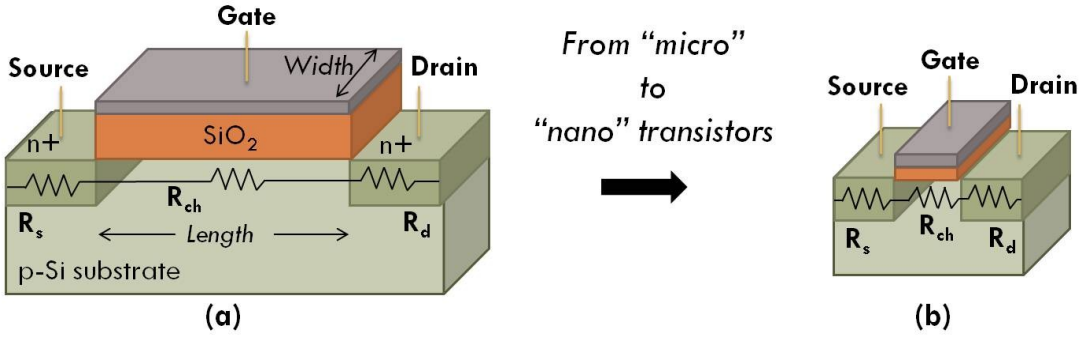


Figure II-3 Impact of R_s and R_d on the total resistance, R_{tot} in a long (a) and a short (b) channel bulk n-MOSFET.

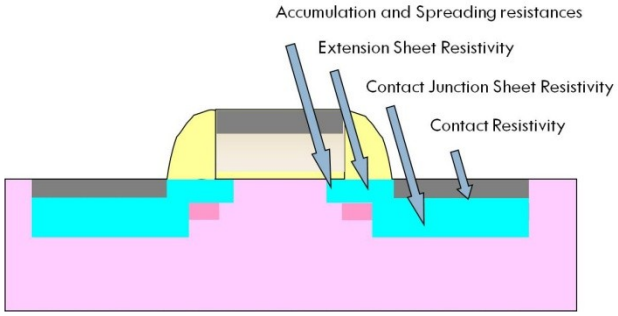


Figure II-4 Parasitic resistance elements in MOSFETs [82].

In general, due to the presence of source and drain resistances, R_s and R_d respectively, when a gate-to-source and a drain-to-source voltage is applied to the device, then a difference is observed between these external voltages on the outer pad, indicated as $V_{gs}^{'}$ and $V_{ds}^{'}$ respectively, and the internal voltages V_{gs} and V_{ds}. Therefore:

$$V_{gs}^{'} = V_{gs} + R_s \cdot I_d \qquad \textbf{Eq. II.9}$$

$$V_{ds}^{'} = V_{ds} + \left(R_s + R_d\right) \cdot I_d \qquad \textbf{Eq. II.10}$$

Consequently, taking into account the SD series resistance, the measured attenuation factor, θ_1 is [81]:

$$\theta_1 = \theta_{1,0} + G_m \cdot R_{sd} \qquad \textbf{Eq. II.11}$$

where $\theta_{1,0}$ is the intrinsic first order mobility attenuation factor and G_m is the static transconductance parameter:

$$G_m = \frac{W}{L} \cdot C_{ox} \cdot \mu_0 \qquad \textbf{Eq. II.12}$$

II.3 Y-Function Methodology

A powerful and physically meaningful method to extract the MOSFET parameters, namely V_t, μ_0, L_{eff}, θ_1 and θ_2 is the *Y-Function*. This useful function, firstly presented in [56], is defined as following:

$$Y = \frac{I_d}{\sqrt{g_m}} \qquad \textbf{Eq. II.13}$$

where I_d is the drain current in linear region (Eq. II.5(a)) and g_m is the *transconductance*, one of the most important MOSFET quantities:

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \qquad \textbf{Eq. II.14}$$

Combining Eq. II.5(a) and Eq. II.14 we have:

$$g_m = \frac{W}{L} C_{ox} \frac{\mu_0 \cdot \left(1 - \theta_2 \left(V_{gs} - V_t\right)^2\right)}{\left(1 + \theta_1 \left(V_{gs} - V_t\right) + \theta_2 \left(V_{gs} - V_t\right)^2\right)^2} V_{ds} \Leftrightarrow g_m = \beta \frac{\left(1 - \theta_2 \left(V_{gs} - V_t\right)^2\right)}{\left(1 + \theta_1 \left(V_{gs} - V_t\right) + \theta_2 \left(V_{gs} - V_t\right)^2\right)^2} \qquad \textbf{Eq. II.15}$$

where β represents the *current gain factor*:

$$\beta = \frac{W}{L} \cdot C_{ox} \cdot \mu_0 \cdot V_{ds} \qquad \textbf{Eq. II.16}$$

Consequently, from equations II.5(a), II.13 and II.15, we obtain:

$$Y = \sqrt{\beta} \cdot \frac{\left(V_{gs} - V_t\right)}{\sqrt{1 - \theta_2\left(V_{gs} - V_t\right)^2}} \qquad \textbf{Eq. II.17}$$

In Figure II-5(a) the calculated Y-Function, $Y(V_g)$, is depicted for several gate lengths of n-MOS transistors issued from a 14 nm FDSOI CMOS technology. In strong inversion the Y-Function varies linearly with V_g and thus, normally the threshold voltage can be extracted from the x-axis intercept. The current gain factor β and thus, G_m can also be extracted from the slope of the curves. Therefore, μ_0 can be calculated from Eq. II.12.

Afterwards, in order to extract the first and second order mobility attenuation factors, we define θ_{eff}:

$$\theta_{eff} = \frac{\beta}{I_d} - \frac{1}{V_{gs} - V_t} \quad \Leftrightarrow \quad \theta_{eff} = \theta_1 + \theta_2\left(V_{gs} - V_t\right) \qquad \textbf{Eq. II.18}$$

By plotting parameter θ_{eff} with the gate overdrive voltage, $V_{gt} = V_{gs} - V_t$ for different gate lengths, we observe that θ_{eff} reaches a plateau for high gate overdrive voltages. Indeed, an example for 14 nm FDSOI n-MOSFETs is presented Figure II-6(a). Consequently, we obtain θ_1 from the x-axis intercept of θ_{eff} - $(V_{gs}-V_t)$ plot and θ_2 from the corresponding slope. Therefore, after having extracted θ_1 for several gate lengths, we can plot θ_1 as a function of G_m. This plot will ideally, result in a straight line, whose slope corresponds to the SD series resistance (Eq. II.11). An example of the plot θ_1- G_m for 14 nm FDSOI devices is illustrated in Figure II-6(b).

As can be seen in Figure II-5(a), the presence of θ_2 results in a non-linearity of $Y(V_g)$ curves in strong inversion. In order to overcome this problem, we applied the new Y-Function method [83]. In general, this method relies on *i iteration steps*, until a linear curve is obtained (see Figure II-5(b)). More precisely, after having applied the Y-Function as described above and obtained a first approximation of θ_2, we make a correction by eliminating the influence of θ_2.

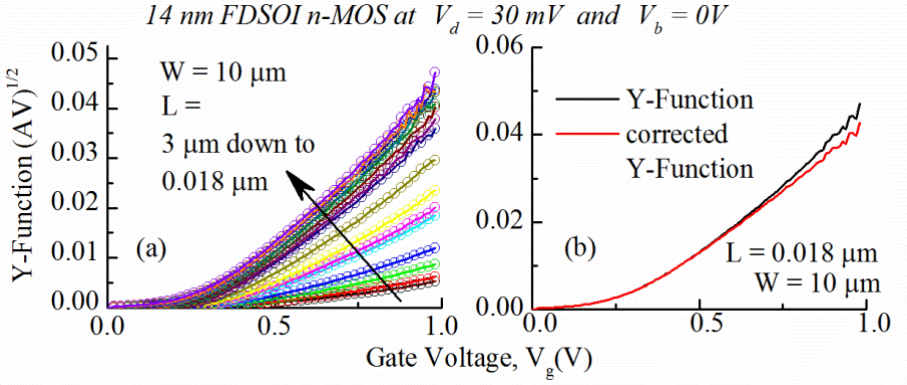


Figure II-5 Y-Function as a function of the gate voltage for different gate lengths of n-MOS 14 nm FDSOI devices in linear region (a) and Y-Function before (black line) and after correction (1 iteration step) (red line) of an FDSOI MOSFET with L=0.018 µm (b).

For this reason it is defined:

$$Y_{i+1}(V_{gs}) = Y_i(V_{gs}) \cdot \sqrt{1 - \theta_{2,i}(V_{gs} - V_t)^2} \qquad \textbf{Eq. II.19}$$

It is obvious from the example presented in Figure II-5(b), that Y-Function becomes more linear in a wider range of V_g in strong inversion even from the first round of iteration and thus, resulting in a more precise parameter extraction.

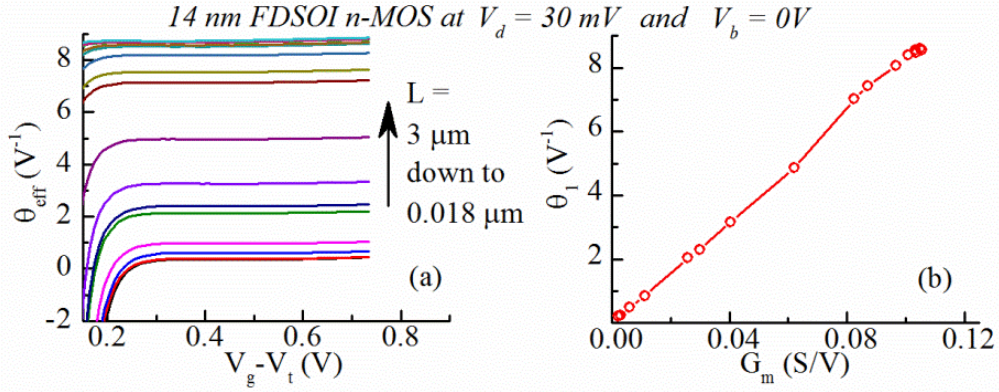


Figure II-6 θ_{eff} as a function of ($V_g - V_t$) for different gate lengths of n-MOS 14 nm FDSOI devices in linear region (a) and the corresponding θ_1 as a function of G_m (b).

II.4 Split C-V Methodology

Except for the drain current transfer characteristics (I_d-V_g) in linear region, it is widely known that capacitance characteristics (*C-V*) are also useful for transport parameter extraction in MOSFETs. Especially, *split C-V technique* is one of the most popular methods for the extraction of several intrinsic channel properties, like C_{ox}, L_{eff}, the flat-band voltage, V_{fb} or the substrate doping concentration, N_A or N_D. This method relies on the mobile channel charge density measurement and composes of gate-to-channel capacitance, C_{gc}, gate-to-bulk capacitance, C_{gb} and total capacitance, C_{tot}, measurements.

Concerning the C_{gc} measurement, this is realized by connecting the "high" terminal of an LCR-meter to the gate (*G*) of the device, the "low" terminal to the Source (*S*) and Drain (*D*) and the Substrate (*B*) to the ground (Figure II-7(a)).

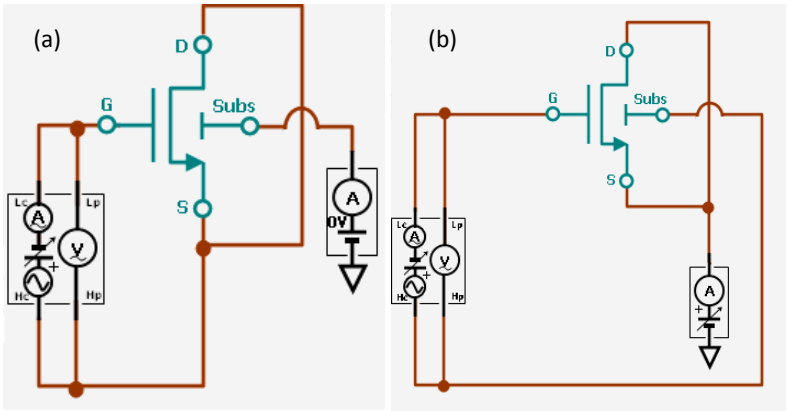


Figure II-7 Configuration for C_{gc} (a) and C_{gb} (b) measurements.

On the other hand, in order to obtain the C_{gb}, the gate has to be connected again to the "high" terminal of the LCR-meter, but this time the substrate to the "low", while the source and the

drain have to be grounded (Figure II-7(b)). Finally, the C_{tot} measurement consists of a superposition of the two previous measurements since $C_{tot}= C_{gc}+ C_{gb}$. This means that the gate is connected to the "high" terminal while the source, drain and substrate are shorted and connected to the "low" terminal.

II.4.1 Principle of effective mobility extraction

As has been already mentioned, the split C-V technique is one of the most popular methods for the extraction of the effective mobility in MOSFETs. To achieve this, the inversion charge, $Q_i(V_g)$ has to be calculated by integrating the $C_{gc}(V_g)$ curves starting from the accumulation until the inversion region of operation [57], [58]:

$$Q_i(V_g) = \int_{V_{acc}}^{V_{g,\max}} \frac{C_{gc}(V_g)}{W \cdot L_{eff}} dV_g \qquad \textbf{Eq. II.20}$$

The drain current of a MOSFET in linear operation is given by Eq. II.5(a). Further, in the linear regime, where V_{ds} is small, the drain current can be expressed in terms of the inversion charge:

$$I_d = \frac{W_{eff}}{L_{eff}} \cdot \mu_{eff} \cdot V_{ds} \cdot Q_i \qquad \textbf{Eq. II.21}$$

Thus, the effective mobility can be extracted by combining both drain current and capacitance measurements in the linear region as a function of the gate voltage.

$$\mu_{eff} = \frac{L_{eff}}{W \cdot V_{ds}} \cdot \frac{I_d}{Q_i} \qquad \textbf{Eq. II.22}$$

II.4.2 Influence of AC signal oscillator level on effective mobility measurement by split C-V technique in MOSFETs

When capacitance measurements are performed, some critical points in the measurement configuration should be taken into account. One of them for example is the measurement frequency. Usually we select a high frequency range, namely in MHz range, in order to eliminate the influence of possible interface states, which contribute also to the capacitance especially in the transition between the accumulation and inversion region. Another critical point is the choice of the AC signal oscillator level. Thus, we investigated the impact of the AC signal oscillator level on the effective mobility measurement by *split C-V technique* in MOSFETs [84].

II.4.2.1 Device fabrication process and electrical measurements conditions

Both $C_{gc}(V_g)$ and $I_d(V_g)$ characteristics were measured on 10×10 µm^2 nMOS transistors from an advanced FDSOI technology [85]. The gate stack consists of TiN/Hf-based oxide dielectric with equivalent oxide thickness 1.2 nm. The channel Si thickness is about 6-7 nm and the buried oxide BOX is 20 nm thick. Capacitance and drain current measurements were performed at wafer level with an Agilent B1500 semiconductor parameter analyzer. The AC signal oscillator level (ΔV_g) was varied from 10 to 250 mV for

capacitance measurements carried out at 1 MHz frequency. The drain voltage V_d for $I_d(V_g)$ acquisition was changed from 5 to 50 mV.

II.4.2.2 Results

Figure II-8 shows typical $C_{gc}(V_g)$ and corresponding $Q_i(V_g)$ characteristics obtained for various AC signal oscillator levels. Note the huge overestimation of the capacitance and inversion charge in weak inversion region below threshold (here V_t=*0.35V*) as the oscillator level increases.

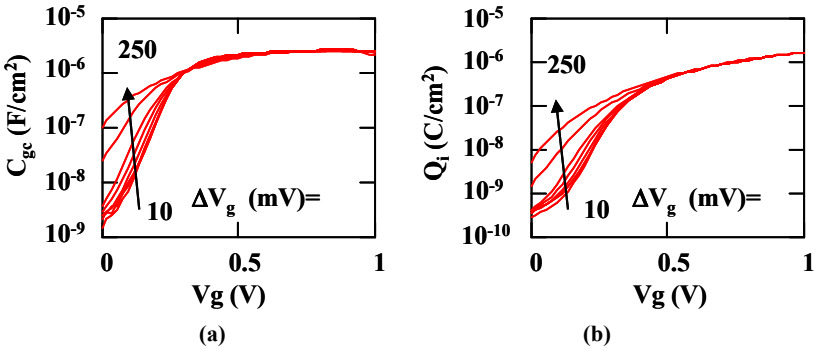


Figure II-8 Typical $C_{gc}(V_g)$ and $Q_i(V_g)$ characteristics as obtained on 10×10 µm^2 nMOS transistors for various oscillator levels ΔV_g.

Figure II-9(a) displays typical $I_d(V_g)$ characteristics obtained with various drain voltage varying from 5mV to 50mV. In Figure II-9(b) are shown the associated $\mu_{eff}(V_g)$ curves calculated with Eq. II.22 for various oscillator levels ΔV_g and using the $I_d(V_g)$ curve measured with the smallest V_d value (*5mV*) for minimizing the error due to V_d [59]. Moreover, provided that the measurement was performed on a large device, the difference between the effective and the real dimensions is negligible. Note the strong influence of the oscillator level on the effective mobility below threshold.

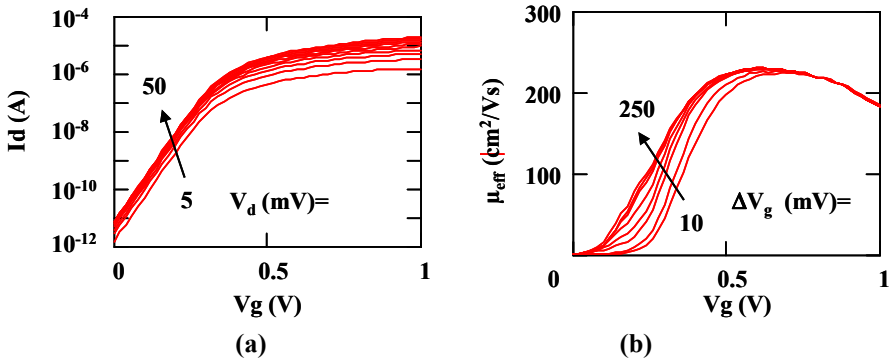


Figure II-9 a) Typical $I_d(V_g)$ for various drain voltages and b) $\mu_{eff}(V_g)$ characteristics as obtained on 10×10 µm^2 n-MOS transistors for various oscillator levels ΔV_g (V_d=5mV).

However, even for the smallest oscillator level (here *10mV*), μ_{eff} is still cancelling out for very low gate voltage values (here V_g<*0.15V*). This means that, despite the use of very small oscillator amplitude, the C_{gc} capacitance could not be measured with enough accuracy at very small gate voltage in order to follow the huge dynamic of $Q_i(V_g)$ and, by turn, of $I_d(V_g)$ variations (5-6 decades) in weak inversion.

Figure II-10 shows the variations of the inversion charge and associated effective mobility with the AC signal oscillator amplitude for different values of gate voltage going from very weak to medium inversion region. As can be seen from this figure, the oscillator

level has a strong influence on the inversion charge and related effective mobility even for oscillator level ΔV_g as small as few tens of mV. Actually, the effective mobility decreases linearly with ΔV_g up to 100mV for gate voltage below threshold. Then, μ_{eff} smoothly tends to zero for large ΔV_g values due to enhanced non linear distortion. Indeed, for gate voltage above threshold, μ_{eff} becomes nearly independent of the oscillator level, as the transistor operates more and more in linear region at strong inversion regime.

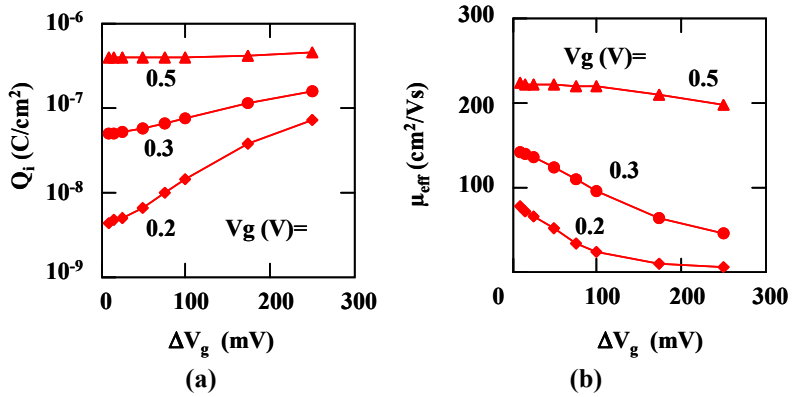


Figure II-10 a) Variations of Q_i and b) μ_{eff} with AC signal oscillator level ΔV_g for various gate voltages (V_g=0.2V, 0.3V, 0.5V).

II.4.2.3 Modeling and Simulation

For modeling the impact of the oscillator level on the gate-to-channel capacitance, we remark that C_{gc} is no longer exactly equal to the derivative of Q_i with respect to V_g, as it should be for very small ΔV_g values. Instead, we consider that the apparent measured capacitance, C_{gcapp}, is now given by the average of the inversion charge variation over one period of time (t) of the AC sinusoidal signal, $\delta V_g(t) = \Delta V_g.sin(2\pi t/T_p)$, applied on top of the DC gate voltage such that,

$$C_{cgapp}(V_g, \Delta V_g) = \frac{1}{T_p}\int_0^{T_p} \frac{Q_i(V_g + \delta V_g(t)) - Q_i(V_g)}{\delta V_g(t)}.dt \qquad \textbf{Eq. II.23}$$

where T_p is signal period.

The associated apparent inversion charge, $Q_{iapp}(V_g, \Delta V_g)$ is then obtained by integration over gate voltage of $C_{gcapp}(V_g)$ as done for measured data.

For the inversion charge modeling, we assume that it is well described by a Lambert W function, which provides a very good analytical approximation of $Q_i(V_g)$ as shown elsewhere [86].

For the effective mobility modeling, we adopt an approach combining, using the Matthiessen rule, a screened Coulomb scattering limited mobility below threshold and a surface roughness limited mobility well above threshold [87] such that μ_{eff} reads as a function inversion charge,

$$\mu_{eff}(Q_i) = \left[\frac{1}{\mu_C(1 + Q_i/Q_c)} + \frac{1 + \theta_2.(Q_i/C_{ox})^2}{\mu_0}\right]^{-1} \qquad \textbf{Eq. II.24}$$

where μ_C refers to the unscreened Coulomb mobility below threshold and μ_0 to the phonon limited low field mobility, θ_2 is the second order mobility attenuation coefficient,

$Q_c \approx kT.C_{ox}/(2q)$ is a critical charge delineating the unscreened Coulomb scattering upper limit, C_{ox} is the gate oxide capacitance per unit area and kT/q is the thermal voltage.

The apparent effective mobility μ_{effapp} is then calculated using Eq. II.22 but with the apparent inversion charge $Q_{iapp}(V_g, \Delta V_g)$ and the modeled drain current obtained using the mobility law $\mu_{eff}(Q_i)$ of Eq. II.24.

By this way, we have been able to reproduce reasonably well both the variations of the apparent inversion charge Q_{iapp} and apparent effective mobility μ_{effapp} with the oscillator level as well as the variation of μ_{effapp} with the inversion charge as shown in Figure II-11 and Figure II-12, respectively.

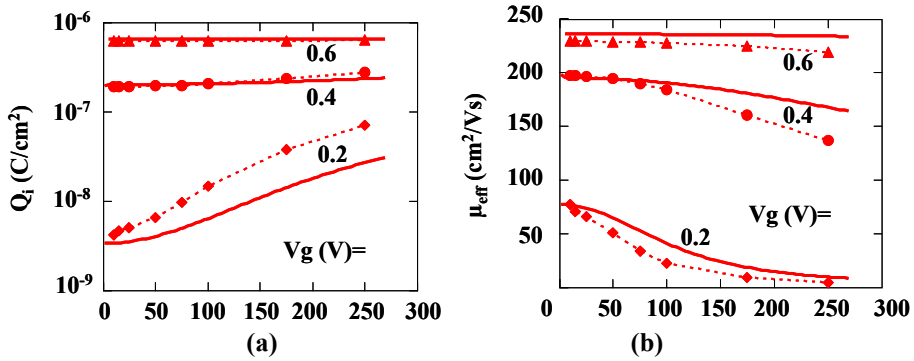


Figure II-11 Experimental (symbols) and modeled (solid lines) variations of Q_i and μeff with AC signal oscillator level ΔV_g for various gate voltages (V_g=0.2V, 0.4V, 0.6V).

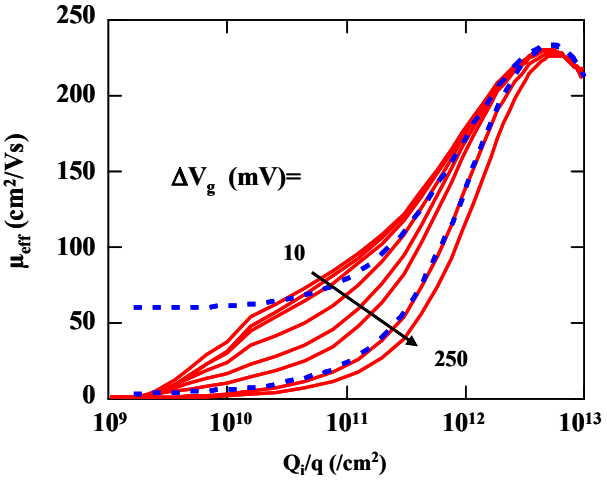


Figure II-12 Experimental (solid lines) and modeled (dashed lines) variations of the effective mobility μeff with the inversion charge density Q_i/q for various oscillator levels.

In particular, the huge decrease of μ_{effapp} with the oscillator level is well predicted for low gate voltage well below threshold. Moreover Figure II-12 shows that the $\mu_{effapp}(Q_i)$ curves are validated down to low inversion charge density - here around $10^{10}/cm^2$, provided the oscillator is sufficiently small ($< 20\ mV$). However, for very small inversion charge density ($< 10^{10}/cm^2$), C_{gc} and, by turn, Q_i is not measured with enough accuracy to allow for a real determination of the effective mobility as it is still cancelling out to zero, whatever the oscillator level is.

II.5 Lambert-W Function Methodology

The goal of this subsection is to present a new methodology based on the Lambert W function [88], which allows the extraction of MOSFET parameters over the full gate voltage range i.e. from weak to strong inversion region, enabling to fully capture the transition between subthreshold and above threshold region, despite the reduction of supply voltage V_{dd} [86]. To this end, we first validate the usefulness of the LW function to describe accurately the gate-to-channel capacitance characteristics $C_{gc}(V_g)$, and, by turn, the MOSFET inversion charge $Q_i(V_g)$ from weak to strong inversion region. Then, in conjunction with the conventional mobility expression, we apply this analytical $Q_i(V_g)$ law for the parameter extraction in advanced MOS devices from a 14 nm FDSOI CMOS technology at zero back bias voltage. Finally, we present a validation of the new approach for a wide range of back bias voltage and different channel lengths, followed by an overview of the extracted parameters properties [89].

II.5.1 Full gate voltage range Lambert-function based methodology for FDSOI MOSFET parameter extraction

II.5.1.1 Device fabrication process and electrical measurements conditions

Electrical measurements were performed on both n-MOS and p-MOS transistors issued from an advanced FDSOI CMOS technology [85]. They were fabricated on (100) SOI wafers with 20 nm thin BOX and a Si (SiGe for p-MOS) body thinned down to 6 nm. The mid-gap metal gate/high k dielectric front gate stack features a 1.2 nm equivalent oxide thickness (*EOT*) and 1.5 nm for n-MOS and p-MOS respectively. The Si or SiGe channels are left undoped. The channel length (L) is varying from 3 down to 0.018 µm and the channel width (W) is fixed at 10 µm. Both gate-to-channel capacitance and drain current measurements were performed for a wide range of back bias voltages (V_b = *0V, ±1V, ±2V, ±3V*) using the Agilent B1500/1530 Semiconductor Device Analyzer.

II.5.1.2 Parameter extraction methodology

The proposed parameter extraction methodology was developed with the following steps. First, typical $C_{gc}(V_g)$ characteristics were obtained on large area 14 nm FDSOI MOS devices. Note that $C_{gc}(V_g)$ measurements were not carried out on smaller area single devices for accuracy reason, since no specific test structure was available in our test mask with many devices in parallel for permitting such measurements on small gate lengths. These data were used to calculate the corresponding inversion charge $Q_i(V_g)$ and to fit the gate-to-channel capacitance with a theoretical expression, and extract the gate oxide capacitance per unit area C_{ox} and the subthreshold ideality factor n. Then, the inversion charge data were fitted with the LW function based model using three parameters, i.e. C_{ox}, n and the threshold voltage V_t, validating the adequacy of the LW function for describing the inversion charge from weak to strong inversion in a continuous way.

In a second step, the drain current $I_d(V_g)$ data obtained in linear region on varying channel length devices were fitted using the LW based $Q_i(V_g)$ expression and the standard three parameter mobility model, including the low field mobility μ_0 and the first order θ_1 and second order θ_2 attenuation coefficients [74], [90].

a) Lambert W function based inversion charge control law with gate voltage

The Lambert W function has been shown to be very efficient for describing $C_{gc}(V_g)$ characteristics in FDSOI devices [91]. Here, we further verify that it is still applicable to 14 nm FDSOI devices. Indeed, considering the charge conservation equation in FDSOI devices and the fact that in standard FDSOI the relation $C_{box}<<C_{ox}$ is valid, where C_{box} is the BOX oxide capacitance the front gate-to-channel capacitance can be described by:

$$C_{gc}(V_g) = \frac{bQ_i(V_g)C_{ox}}{C_{ox} + bQ_i(V_g)} \qquad \textbf{Eq. II.25}$$

where $b=q/(nkT)$, n is the ideality factor, q is the electron charge and kT is the thermal energy.

Figure II-13 shows that Eq. II.25 provides a very good description of $C_{gc}(V_g)$ for 14 nm FDSOI devices both in linear and logarithmic scales using C_{ox} and n in Eq. II.25 as fitting parameters. As is usual in split C-V technique, the inversion charge can be deduced by integration of $C_{gc}(V_g)$ curve between $V_g = 0$ and V_g. It should be noted that the calculated maximum fitting error does not exceed ≈10% over the whole gate voltage range, which is really good given the large C_{gc} dynamic investigated (≈ 3 decades).

Therefore, the experimental $Q_i(V_g)$ characteristics can be reproduced using the Lambert W function of gate voltage for the inversion charge Q_i in terms of the gate oxide capacitance per unit area C_{ox}, the subthreshold ideality factor n and the threshold voltage V_t [91]:

$$Q_i(V_g) = C_{ox} n \frac{kT}{q} LW\left(e^{q.\frac{V_g - V_t}{nkT}}\right) \qquad \textbf{Eq. II.26}$$

The Lambert W function can be well approximated as indicated in Eq. II.27:

$$Q_i(V_g) = C_{ox} n \frac{kT}{q} \ln\left(1 + e^{q.\frac{V_g - V_t}{nkT}}\right)\left(1 - \frac{\ln\left(1 + \ln\left(1 + e^{q.\frac{V_g - V_t}{nkT}}\right)\right)}{2 + \ln\left(1 + e^{q.\frac{V_g - V_t}{nkT}}\right)}\right) \qquad \textbf{Eq. II.27}$$

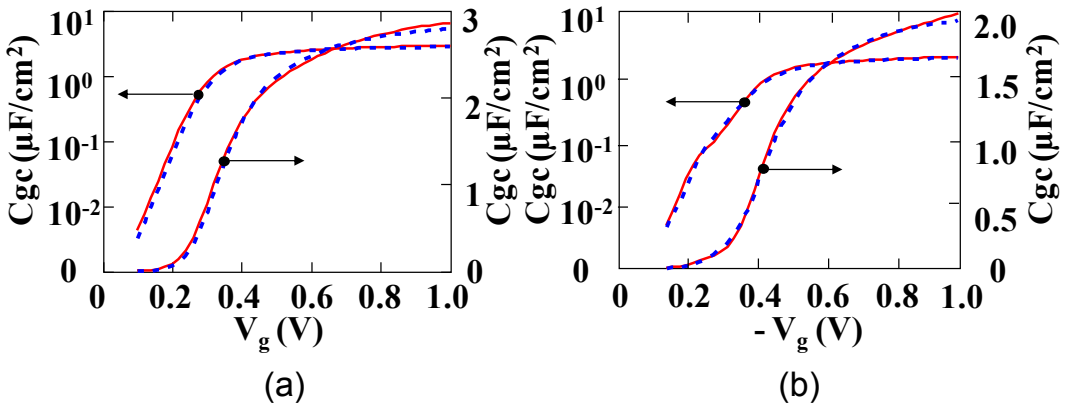


Figure II-13 Experimental (solid lines) and modeled (dashed lines) $C_{gc}(V_g)$ characteristics of n- and p-channel FD-SOI MOSFETs with channel width W = 10 µm and channel length L = 3 µm. The modeled results were obtained using the parameters: $C_{ox} = 2.6 \times 10^{-6}$ F/cm² and n = 1.37 for the n-MOS device (a) and $C_{ox} = 1.44 \times 10^{-6}$ F/cm² and n = 1.53 for the p-MOS device (b).

Figure II-14 shows that the LW function in II.26 enables a very good fitting of the inversion charge from weak to strong inversion using the three parameters C_{ox}, n and V_t. In

this example, a Levenberg-Marquardt non linear regression has been used to extract the best fitting parameters: $C_{ox} = 2.6 \times 10^{-6}\ F/cm^2$, $n = 1.37$ and $V_t = 0.30\ V$ in n-MOS devices and $C_{ox} = 1.44 \times 10^{-6}\ F/cm^2$, $n = 1.53$ and $V_t = 0.34\ V$ in p-MOS devices. It should be mentioned that the extracted values of C_{ox} and n were consistent with those used for the $C_{gc}(V_g)$ fitting (see Figure II-13) and the calculated maximum fitting error is no more than ≈ 11% for n-MOS and ≈ 25% for p-MOS for the *whole* V_g range. This finding demonstrates that the LW function in II.26 constitutes an accurate, continuous and analytical expression for the MOSFET inversion charge with gate voltage applicable from weak to strong inversion both in linear and logarithmic scale.

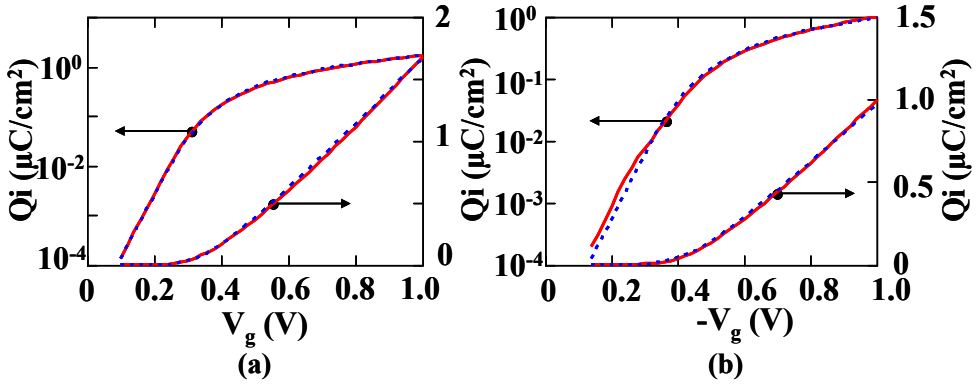


Figure II-14 Experimental (solid lines) and modeled (dashed lines) Qi(Vg) characteristics of n- and p-channel FD-SOI MOSFETs with channel width W = 10 µm and channel length L = 3 µm. The modeled results were obtained using the parameters: $C_{ox} = 2.6\times10^{-6}$ F/cm², n = 1.37 and V_t = 0.30 V for the n-MOS device (a) and $C_{ox} = 1.44\times10^{-6}$ F/cm², n = 1.53 and V_t = 0.34 V for the p-MOS device (b).

b) MOSFET parameter extraction procedure from drain current characteristics

From the conventional formulation of the effective mobility in strong inversion, i.e. with gate voltage drive [90], μ_{eff} can be expressed with the inversion charge as:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1 \frac{Q_i}{C_{ox}} + \theta_2 \left(\frac{Q_i}{C_{ox}} \right)^2} \qquad \textbf{Eq. II.28}$$

Since the LW function based inversion charge expression of Equation II.26 is well appropriate from weak to strong inversion region; it can be used in Equations II.21 and II.28 for a full gate voltage range MOSFET parameter extraction with overall 5 parameters, i.e. V_t, n, μ_0, θ_1 and θ_2. We assume that C_{ox} is previously extracted from specific $C_{gc}(V_g)$ characteristics measured on large area devices (here $W = 10\ \mu m$ and $L = 3\ \mu m$).

In order to optimize the parameter extraction accuracy, the extraction routine is decomposed in two steps: i) A first non-linear regression is performed with the $log(I_d)$ vs V_g data, enhancing the influence of the subthreshold region and mainly determining V_t, n and μ_0; ii) A second non-linear regression is carried out in linear scale on the $I_d(V_g)$ data, keeping the previous values of V_t, n, μ_0 parameters and refining the extraction of the remaining mobility attenuation factors θ_1 and θ_2 in strong inversion region.

II.5.1.3 Results and discussion

The previous parameter extraction methodology has been applied to a set of $I_d(V_g)$ characteristics measured on MOS devices with varying gate lengths ($L = 18\ nm$ to $3\ \mu m$) from

a 14 nm FDSOI technology. Figure II-15 shows the comparison between experimental and modeled $I_d(V_g)$ curves using best fit parameters obtained from Levenberg-Marquardt non-linear regression algorithm (see below the gate length dependence of extracted parameters). Note the excellent agreement obtained from weak to strong inversion with a calculated mean error of 1.5% for n-MOS and 1.3% for p-MOS for all gate lengths and full gate voltage range.

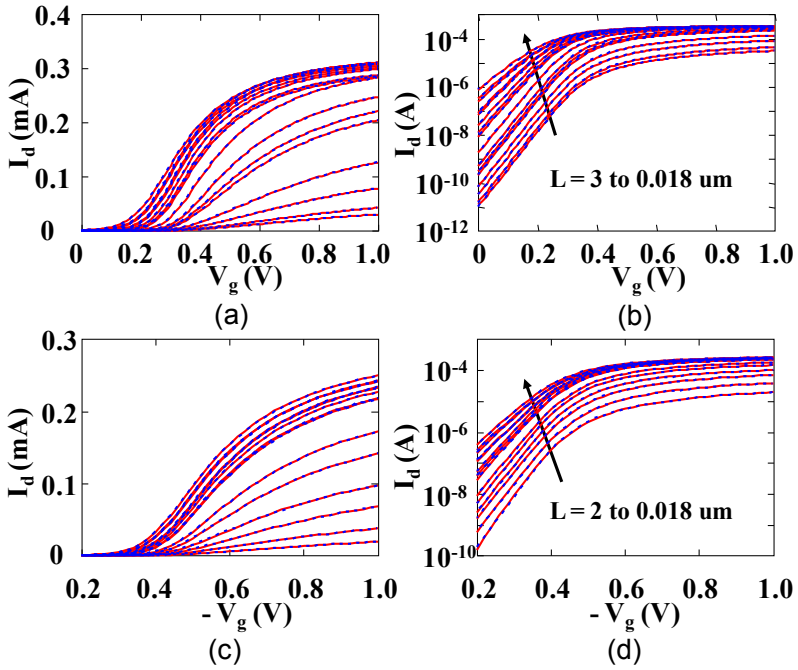


Figure II-15 Experimental (solid lines) and modeled (dashed lines) $I_d(V_g)$ characteristics at V_d=30mV of n-MOS (a, b) and p-MOS (c, d) FD-SOI devices in linear (a, c) and logarithmic (b, d) scales with gate lengths L ranging from 18 nm to 3 µm and channel width W = 10 µm fixed.

Figure II-16 displays the corresponding plot for the transconductance $g_m(V_g)$ for all gate lengths and for specific short and long channel cases. A very good agreement between experimental data and fitting results is also obtained with a computed mean error of 6.5% for n-MOS and 4.3% for p-MOS for all gate lengths and V_g values.

All the MOSFET parameters, extracted using the full gate voltage range methodology, are displayed as a function of gate length in Figures II-17, II-18 and II-19, along with those obtained using the Y-function method, for the sake of comparison with a standard strong inversion extraction technique [56]. Note that the ideality factor n obtained from the LW function based best fit extraction methodology falls in very good agreement with that directly deduced from the maximum subthreshold slope (Figure II-17). Its increase at small gate length is a consequence of short channel effects, also visible on the $V_t(L)$ roll off.

Moreover, as seen from Figure II-18, the parameters V_t and μ_0 take values close to those extracted applying the Y-function method, even though slightly different due to the specificity of each method. However, it is worth noting that they follow the same trend versus L or G_m, emphasizing the consistency of this new methodology. The mobility attenuation parameter θ_1 is also well in line with that from Y-function method (Figure II-19(a) and (b)). Only the second order parameter θ_2 is larger than the one obtained with the Y-function method (Figure II-19(c) and (d)) but their relatively low values have a small influence on the effective mobility as compared to θ_1, especially for small gate lengths. It is likely that, for small gate length, the θ_2 values obtained by non linear regression loose sensitivity as

compared to those extracted by Y-function method. However, we believe that the θ_2 values should remain nearly constant with gate length.

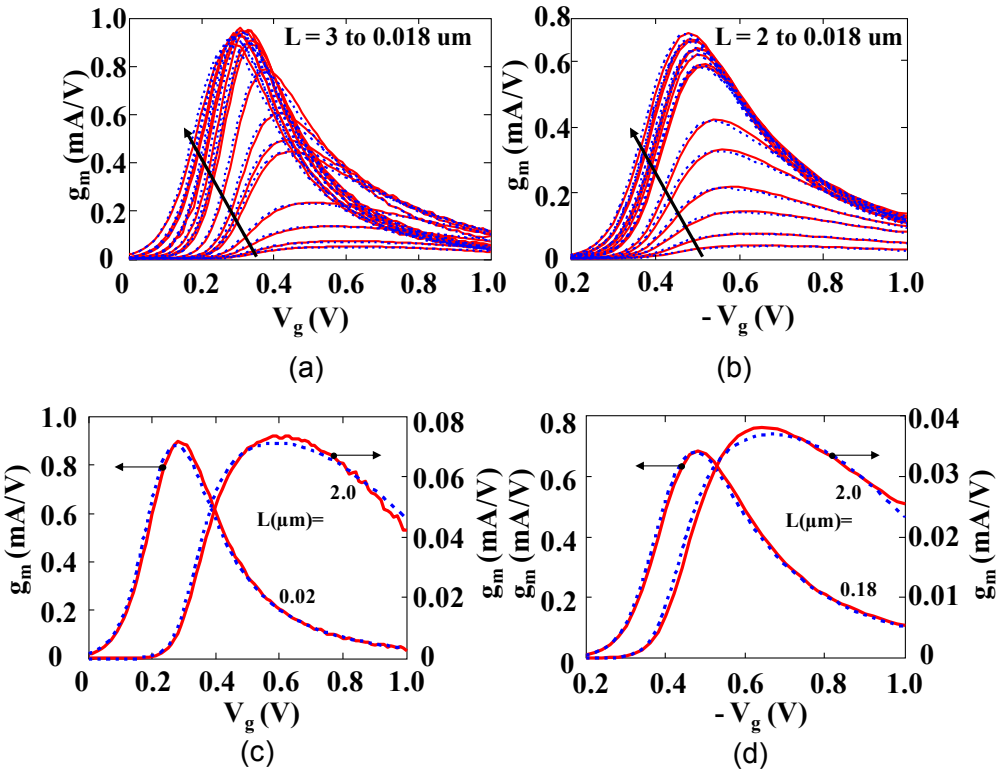


Figure II-16 Experimental (solid lines) and modeled (dashed lines) $g_m(V_g)$ characteristics of n-MOS (V_d=30mV) (a, c) and p-MOS (V_d=-30mV) (b, d) FD-SOI devices for all gate lengths (a, b), for a short channel device (c) and a long channel device (d) with channel width W = 10 µm fixed for all the cases.

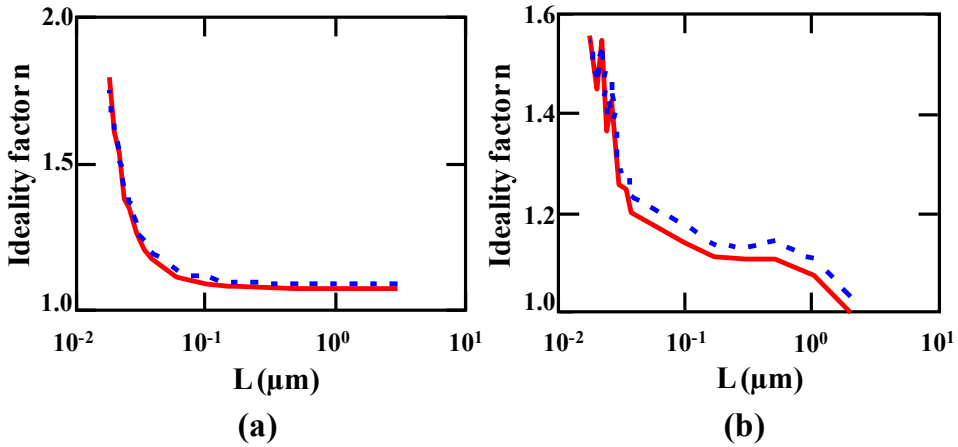


Figure II-17 Variation of the ideality factor n with gate length in n-MOS (a) and p-MOS (b) FD-SOI devices. Solid line: n directly extracted from subthreshold slope, dashed line: n extracted from best fitting.

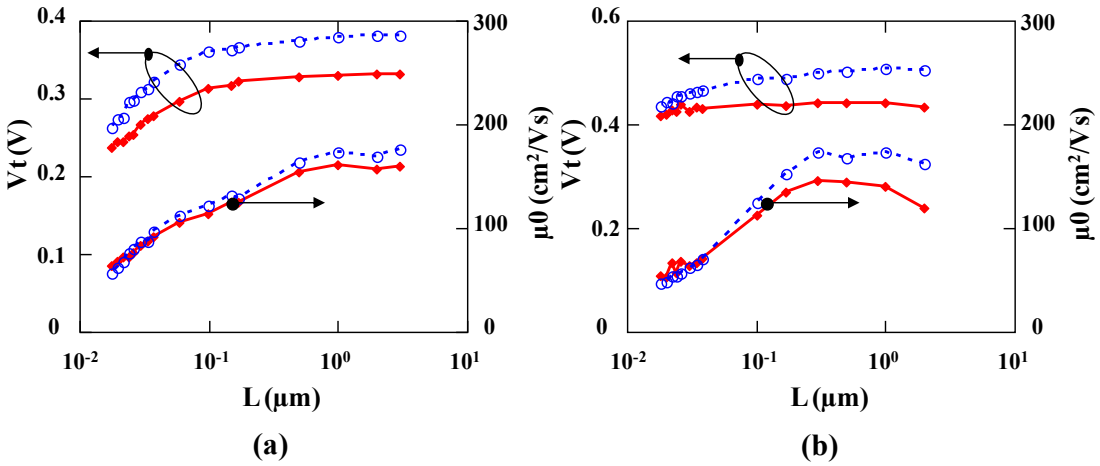


Figure II-18 Variation of parameters V_t and μ_0 with gate length in n-MOS (a) and p-MOS (b) FDSOI devices. Solid line: V_t and μ_0 extracted from the full gate voltage range LW-function methodology, dashed line: V_t and μ_0 extracted using the Y-function method.

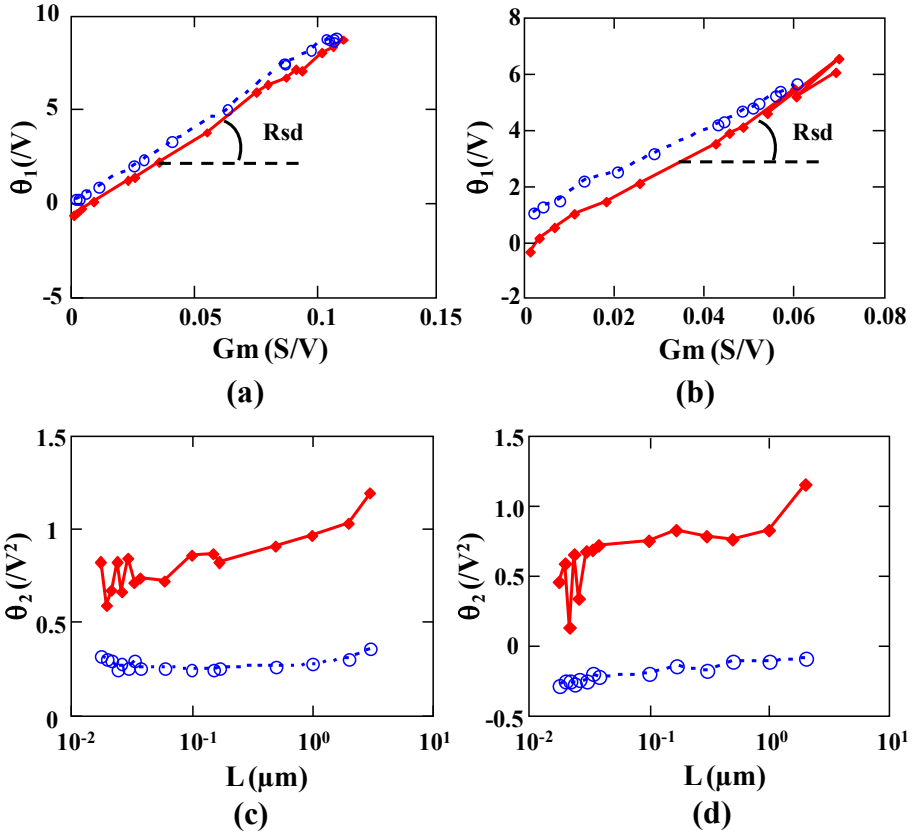


Figure II-19 Plots of θ_1 versus G_m (a, b) and θ_2 versus gate length (c, d) in n-MOS (a, c) and p-MOS (b, d) FDSOI devices. The parameters θ_1 and θ_2 were extracted from the full gate voltage range LW-function methodology (solid lines) or from the Y-function method (dashed lines).

As is usual [56], the series resistance R_{sd} can be extracted from the linear dependence of the first order coefficient θ_1 with G_m (Figure II-19(a) and (b)). Here for devices with fixed channel width $W=10\ \mu m$, we found $R_{sd} = 84\ \Omega$ in n-MOS and $R_{sd} = 92\ \Omega$ in p-MOS devices in good agreement with the values obtained from the Y-function method (respectively $R_{sd}=83\ \Omega$ and $R_{sd}=87\ \Omega$).

Next, in order to emphasize the usefulness of our methodology, we extracted the MOSFET parameters using different ranges of gate voltage, starting at $V_g=0V$ and changing each time the maximum value of V_g (i.e. for $V_{g,max}=0.4, 0.5, ..., 1V$). This way, the parameters were extracted from weak inversion to either moderate or strong inversion region. As can be seen from Figure II-20, for the proposed LW function methodology which encompasses weak to strong inversion regions, the parameters η, V_t, μ_0 and θ_1 are roughly stable with $V_{g,max}$ down to 0.4V. Nevertheless, as expected, the influence of the gate voltage range is stronger in the extraction of μ_0 and θ_1, which are underestimated when the strong inversion part of the curve is not fully taken into account.

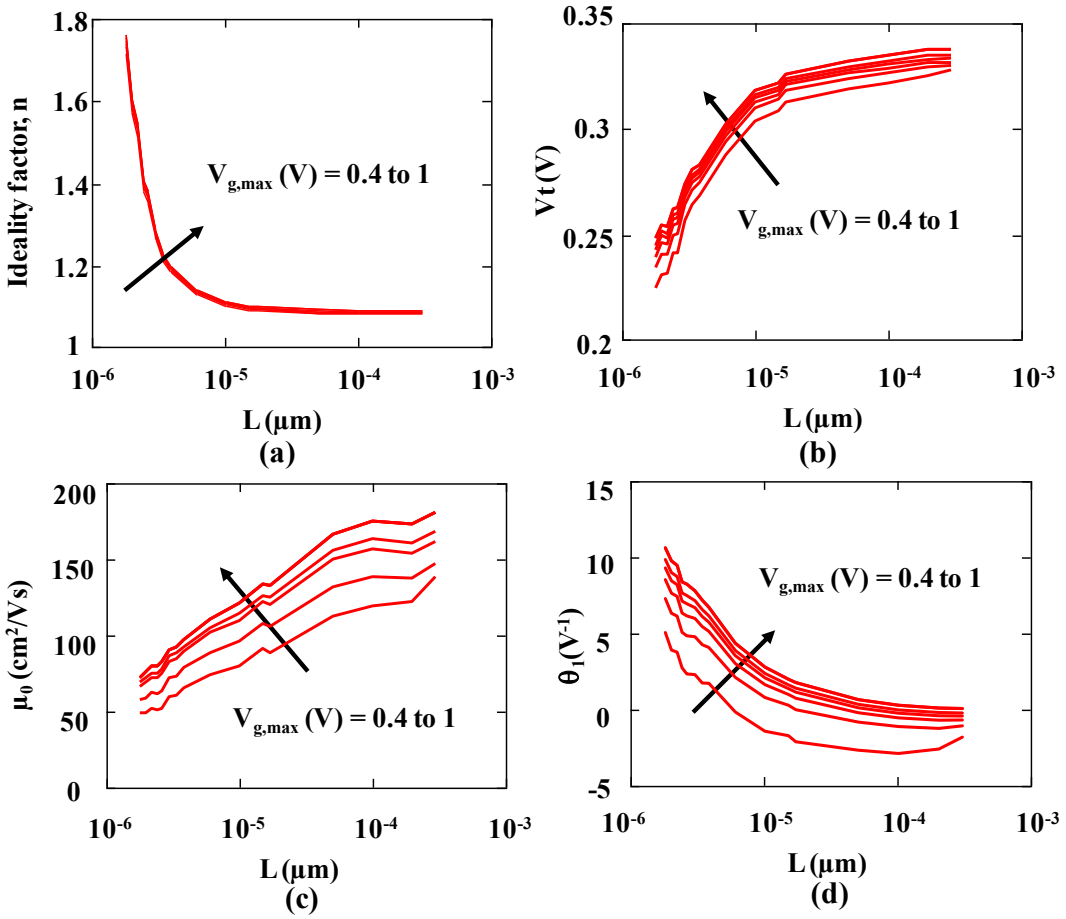


Figure II-20 Variation of the ideality factor (a), threshold voltage (b), low-field mobility (c) and first order attenuation factor (d) with the gate length for various gate voltage ranges for nMOS FDSOI devices.

For each gate length, the effective mobility $\mu_{eff}(V_g)$ has been reconstructed using II.28 with the best fit parameters (μ_0, θ_1 and θ_2) and corrected from the R_{sd} effect using the expression valid in linear region:

$$\mu_{eff\,0} = \frac{\mu_{eff}}{1 - R_{sd} \cdot \frac{I_d}{V_d}} \qquad \textbf{Eq. II.29}$$

in order to obtain the intrinsic effective mobility $\mu_{eff}(V_g)$ free from series resistance influence.

It is clear from Figures II-21 and II-22 that, even after the R_{sd} correction, the effective mobility still exhibit strong gate length dependence but a weak gate voltage variation. This

confirms that the main origin of the mobility degradation with gate length is not due to the series resistance effect but due to the decrease of the low field mobility μ_0 in short channel devices, likely stemming from enhanced scattering rate near source and drain regions [92], [93]. It is also worth noting from Figure II-21 that, after R_{sd} correction, the intrinsic mobility μ_{eff0} shows some little increase above V_t before decreasing at strong inversion. This feature could be due to the negative value of θ_{10} (≈ -0.5 V^{-1}), presumably reflecting the presence of screened Coulomb scattering that enhances μ_{eff} around threshold [94].

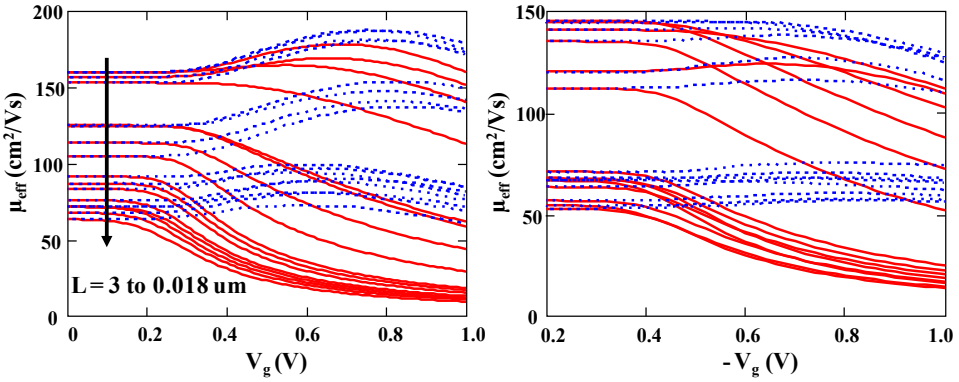


Figure II-21 Variation of the effective mobility μ_{eff} with gate voltage as obtained from full gate voltage range LW-function methodology without (solid line) and with (dashed line) R_{sd} correction in n-MOS (a) and p-MOS (b) FDSOI devices with gate lengths L ranging from 18 nm to 3 µm.

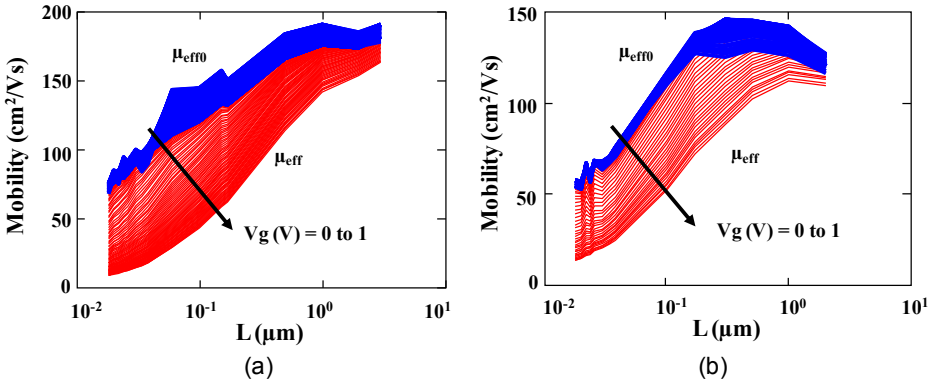


Figure II-22 Variation of the effective mobility μ_{eff} and μ_{eff0} with gate length with V_g as a parameter in n-MOS (a) and p-MOS (b) FD-SOI devices.

II.5.2 Extension of the LW function parameter extraction methodology to a wide back gate voltage range

We applied the methodology described in II.5.1 to extract the electrical parameters of CMOS FDSOI devices as a function of both front and back gate voltages, as well as the gate length. In Figure II-23(a) and (b), the measured transfer characteristics for $V_d = 30\ mV$, with back bias voltages V_b varying from -3 to +3 V, are presented in both linear and semi-logarithmic plots. It is observed that the fitting results, obtained with the LW function-based model of II.26 using V_t, μ_0, η, θ_1 and θ_2 as fitting parameters, are in very good agreement with the experimental data for a wide range of back bias. It is notable that the calculated mean error is less than 1.6% for the entire range of V_g and V_b. In order to check further the accuracy

of the model, the transconductance g_m has been examined. Indeed, the computed mean error was found lower than 9% for all gate lengths and V_g and V_b values. In Figure II-24 two examples of the corresponding plot for the transconductance $g_m(V_g)$ for n-MOS devices with $L = 34\ nm$ and $L = 0.1\ \mu m$ and $W = 10\ \mu m$ fixed are displayed. As it can be seen from these figures, there is a good agreement between the g_m values as calculated from the experimental data and those obtained by the LW function.

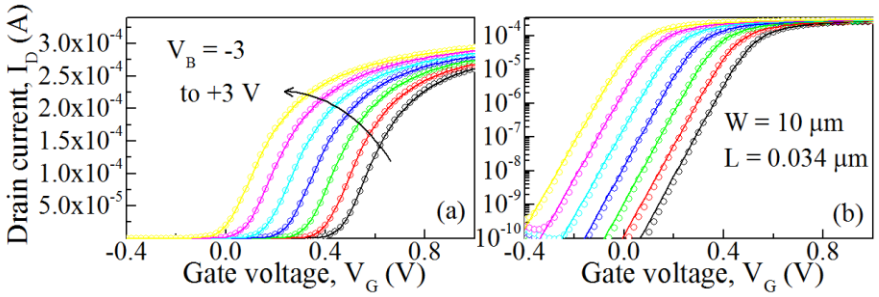


Figure II-23 Experimental (symbols) and modeled (line) transfer characteristics of n-MOS FDSOI devices in linear (a) and logarithmic scales (b) with back bias voltage V_B=V_b ranging from -3V to +3V.

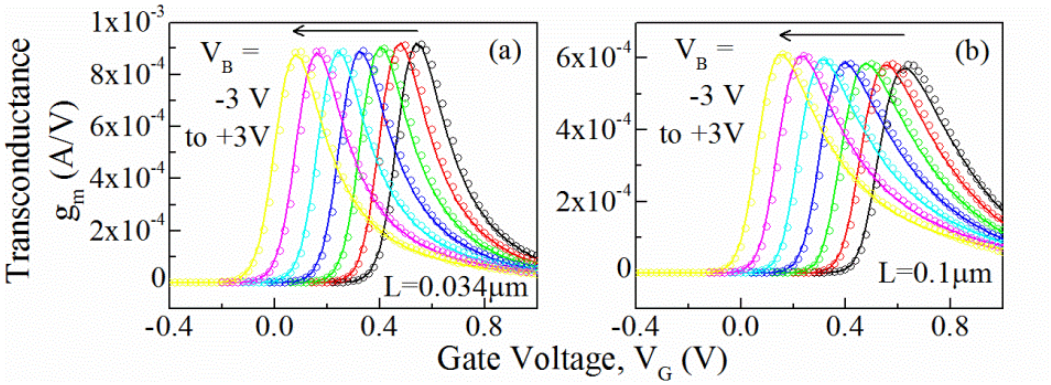


Figure II-24 Experimental (symbols) and modeled (line) g_m-V_g characteristics of n-MOS FDSOI devices with L = 0.034 µm (a) and L = 0.1 µm (b).

Next are shown the electrical parameters obtained by the LW function-based method for all values of V_b. The expected linear dependence of threshold voltage with V_b is shown in Figure II-25(b) proving the consistency of our method with regard to V_t roll-off short channel effect (SCE) and back gate coupling phenomenon. Moreover, as is presented in Figure II-26(a) the method also well captures the increase of ideality factor at small gate length, which is extremely important in advanced technologies. As illustrated in II-26(b), the ideality factor is almost constant with the back bias, since the electrostatic integrity remains unchanged.

The variations of the low field mobility μ_0 with V_b (Figure II-27(a)) indicate weaker dependence for small gate length. This is consistent with the huge decrease of μ_0 in short channel devices for every V_b (Figure II-27(b)), likely due to strong change of scattering mechanism in short channels [6]. The first order attenuation factor θ_1 depends linearly on G_m (see Figure II-28(a)) in agreement with Eq. II.11 for all V_b, further proving the consistency of our method. From the θ_1-G_m slope, we found an almost constant value of the series resistance $R_{sd} \approx 85\ \Omega$ with V_b. The second order attenuation factor θ_2 does not show specific trend with L (Figure II-28(b)) but is increased as V_b is reduced due to enhanced vertical electric field and by turn surface roughness contribution.

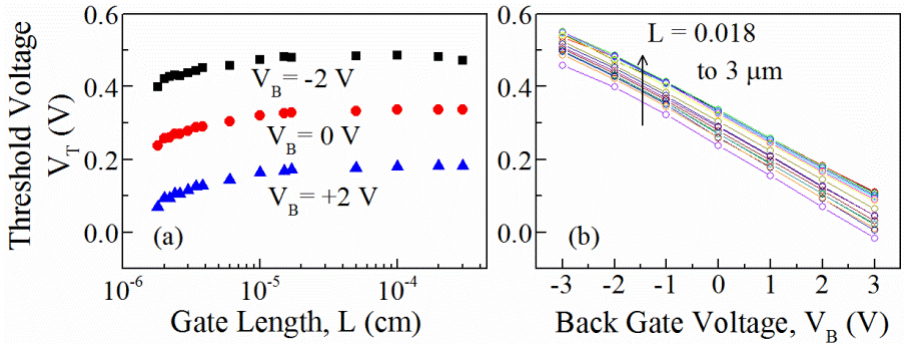


Figure II-25 Variation of V_t extracted from best fitting with gate length (a) and back bias voltage V_b (b) in nMOS FD-SOI devices.

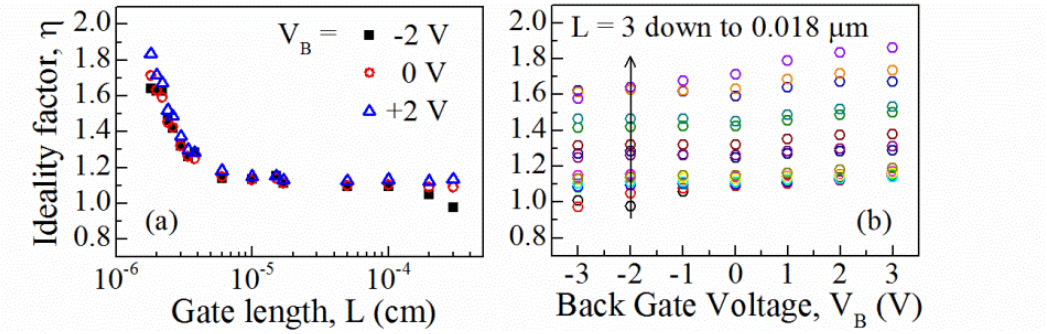


Figure II-26 Variations of η extracted from LW-function methodology with gate length (a) and back gate voltage (b) in n-MOS FD-SOI devices with fixed channel width W=10µm.

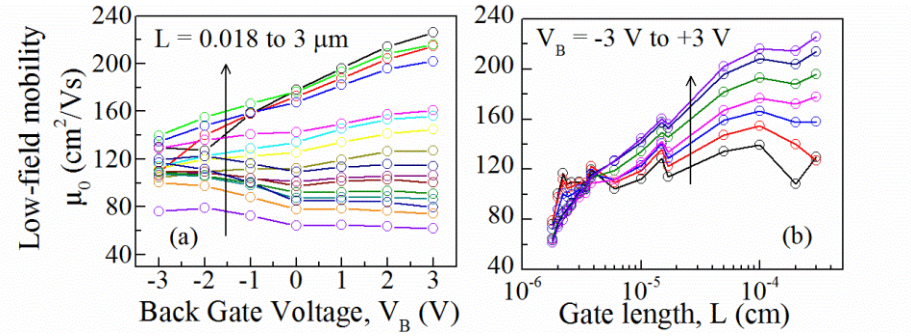


Figure II-27 Variation of μ_0 extracted from best fitting with back bias voltage V_B=V_b in n-MOS FDSOI with different channel length L and fixed channel width W=10 µm.

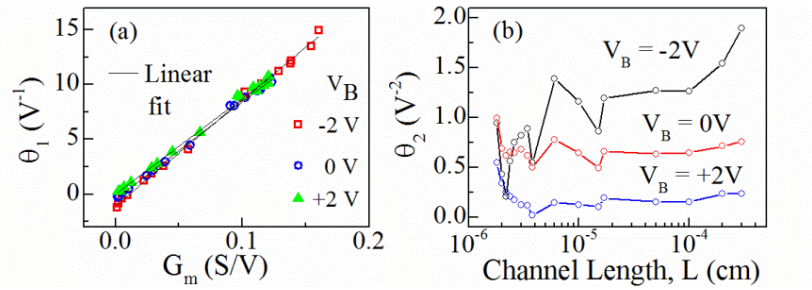


Figure II-28 Mobility attenuation factors θ_1 and θ_2 extracted from best fitting versus G_m (a) and gate length L (b) respectively for nMOS FDSOI MOSFETs with fixed channel width W=10µm.

Finally, in order to examine the effect of R_{sd}, we calculated the effective mobility, μ_{eff0}, without its influence (Eq. II.29). Figures II-29 and II-30 demonstrate the strong

dependence of both of μ_{eff0} and μ_{eff} on the gate length and the back gate voltage, respectively, as well as the influence of R_{sd}.

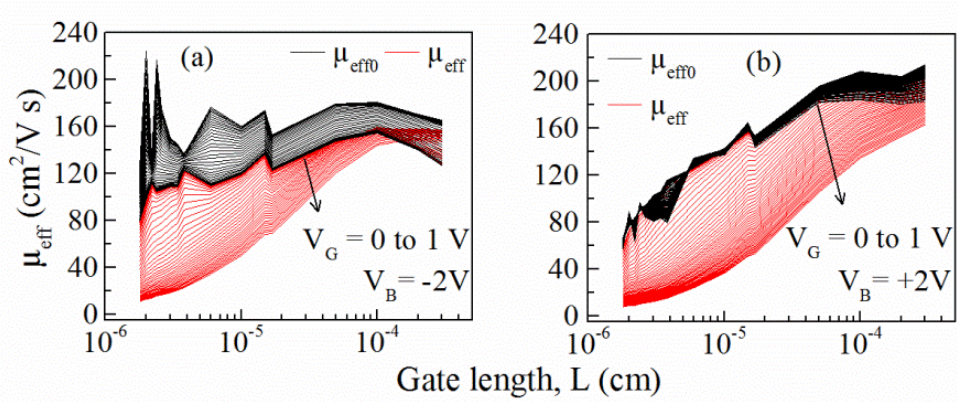


Figure II-29 Modeled effective mobility versus channel length with (red line) and without (black line) the series resistance R_{sd} for V_b = -2V (a) and V_b = +2V (b).

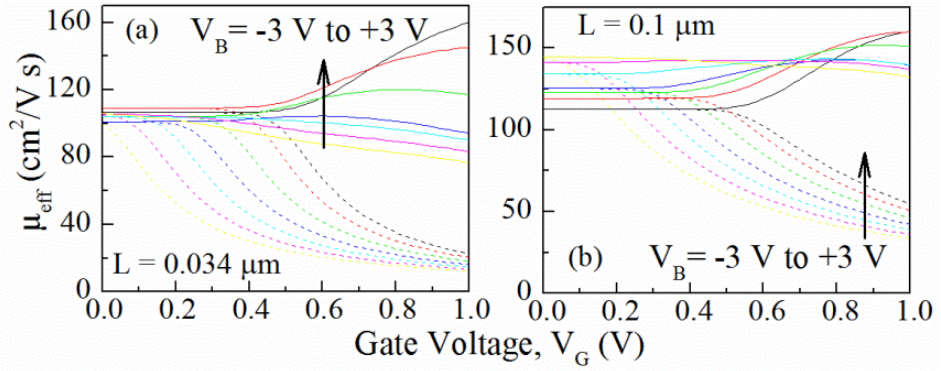


Figure II-30 Variation of the effective mobility μ_{eff} with gate voltage as obtained from full gate voltage range LW-function methodology without (solid line) and with (dashed line) R_{sd} correction for various back gate voltages in n-MOS FDSOI devices with gate lengths L = 0.034 µm (a) and L = 0.1 µm (b).

II.6 Low-Frequency Noise in Semiconductor Devices

Although noise is an unwanted phenomenon, it is generated in all electronic circuits. It can be categorized as noise originating from external sources, like adjacent circuits or AC power lines or noise originating from internal random fluctuations in physical processes governing the electron transport in a medium. In this manuscript we are interested only in the second type of noise, namely in the noise of the device, which is a random spontaneous perturbation of a deterministic signal inherent to the physics of the device [95].

In this context the result of drain current noise in a MOSFET is always a time variation of the current value around a median value. An example is illustrated in Figure II-31. In this figure the drain current fluctuations are presented as a function of time, and consequently we are talking about a time domain measurement. If we use the fast Fourier transform (FFT), we can also exploit the frequency domain [96], namely the plot S_{Id} as a function of the frequency f, where $S_{Id} = (\Delta I_d)^2/Hz$ is the power spectral density (PSD).

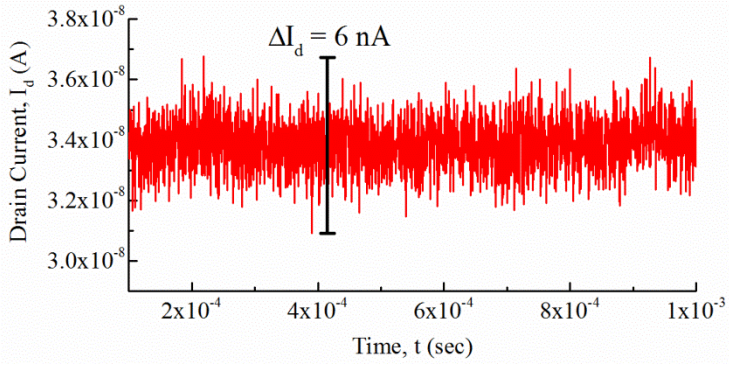


Figure II-31 An example of drain current noise in an n-MOS FDSOI transistor with L=0.03µm and W=0.5µm measured in V_g=0.2V.

II.6.1 Fundamental Noise Mechanisms

As dimension of the devices are shrinking more and more, the study of low-frequency noise becomes more and more crucially important, since *1/f noise* increases as the reciprocal of the device area [97], [98], [99], [100].

The fundamental noise mechanisms, briefly described below, are the following: thermal noise, shot noise, Generation-Recombination (G-R) noise, Random Telegraph Signal (RTS) noise and flicker noise.

II.6.1.1 Thermal Noise

Thermal or "*Johnson-Nyquist*" or "*white*" noise can be regarded as the background noise of any LF fluctuations. This type of noise was firstly measured by John B. Johnson at Bell Labs in 1926 and explained by Harry Nyquist [101], [102]. Its existence is due to the random motion of the carriers in the conducting material, which results in a frequency independent power spectrum. Thus, every resistor produces thermal noise, calculated from the following equation:

$$S_V = 4kTR \left[V^2/Hz\right] \Leftrightarrow S_I = 4kTG \left[A^2/Hz\right] \qquad \textbf{Eq. II.30}$$

where k is the Boltzmann's constant, T is the temperature, R is the resistance and G is the ohmic conductance. Consequently, every semiconductor device will also produce thermal noise which will be proportional to its dynamic resistance [103].

II.6.1.2 Shot Noise

Shot or "*Poisson*" noise was firstly introduced in 1918 by Walter Shottky during his studies of current fluctuations in vacuum tubes [104]. The shot noise is associated with the discrete nature of the electrons flowing through a potential barrier, like a p-n junction, during a period of time. A shot noise is produced when the electrons cross the barrier independently and randomly, resulting in a PSD:

$$S_I = 2qI \left[A^2/Hz\right] \qquad \textbf{Eq. II.31}$$

where q is the electron charge and I is the DC current across the barrier.

II.6.1.3 Generation-Recombination Noise

G-R noise occurs when the phenomenon of carriers trapping-detrapping at a discrete trap level is taking place in a semiconductor device and the fluctuation duration is random. More specifically, G-R noise occurs when one of the following phenomena is taking place:

- ✓ recombination of a free electron and a free hole,
- ✓ generation of a free electron and a free hole,
- ✓ trapping of a free electron in an empty trap,
- ✓ trapping of a free hole in a filled trap

The result is a "Lorenzian-like" spectrum [105], which will be described as following:

$$S_{I_d} = \frac{A}{\left(1+\frac{f}{f_c}\right)^2} \quad \left[A^2/Hz\right] \qquad \textbf{Eq. II.32}$$

where A is the plateau at low frequencies and f_c the corner frequency above which the spectral density is proportional to the inverse square of the frequency (see Figure II-32(b)).

Consequently, if the G-R noise is caused by N carrier number fluctuations due to their interaction with N_T (empty and filled) traps, then the PSD is given by [95]:

$$S_N = 4 \cdot \overline{\Delta N^2} \frac{\tau}{1+(2\pi f)^2 \tau^2} \qquad \textbf{Eq. II.33}$$

In Eq. II.33, assuming that the Fermi energy level is within a few kT close to the trap energy level and $N>>N_T$, the variance $\overline{\Delta N^2}$ will be:

$$\overline{\Delta N^2} = \frac{1}{4} N_T \qquad \textbf{Eq. II.34}$$

and τ, the time constant of the transitions:

$$\tau = \left(\frac{1}{\tau_c} + \frac{1}{\tau_e}\right)^{-1} \qquad \textbf{Eq. II.35}$$

where τ_c and τ_e are the capture and emission time of traps, respectively.

II.6.1.4 Random Telegraph Signal Noise

Random telegraph signal or "*popcorn*" or "*burst*" noise, which is observed in small area devices (*surface* < $1\mu m^2$) [106], is attributed to individual carrier trapping at the silicon-oxide interface [107], [108], [109]. It should be emphasized that RTS observation is verified by the time domain signal. In this case only a few traps are involved and consequently the drain current can switch between two or more states -as presented in Figure II-32- due to random trapping-detrapping of carriers.

Similarly to the G-R noise, the PSD of RTS is also "Lorenzian-like" and is described by Eq. II.36 [110].

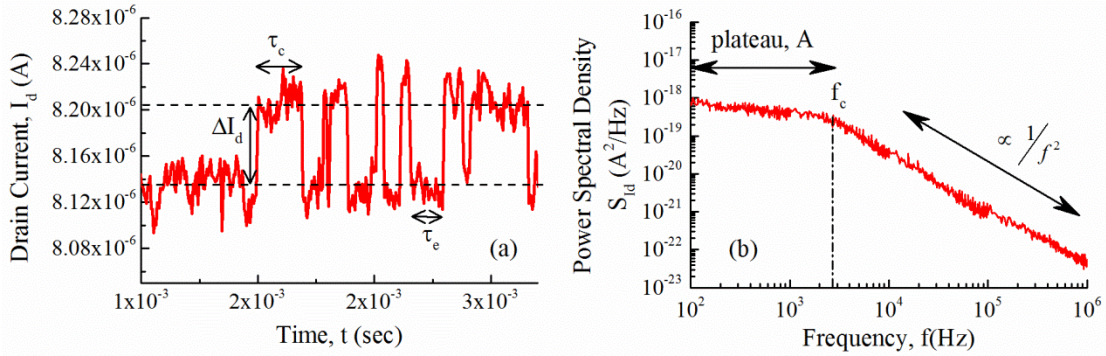


Figure II-32 RTS noise example (a) and the corresponding power spectral density (b) produced by an n-MOS FDSOI transistor with L=0.03 µm and W=0.5 µm measured in V_g=0.48 V.

$$S_{Id} = 4A \cdot \Delta I_d^2 \frac{\tau}{1+(2\pi f)^2 \tau^2} \qquad \textbf{Eq. II.36}$$

where ΔI_d is the average drain current RTS amplitude, τ is given by Eq. II.35, and A is the space mark ratio:

$$A = \frac{\tau}{\tau_c + \tau_e} = f_t(1 - f_t) \qquad \textbf{Eq. II.37}$$

where the capture and emission time of the trap, which are in general determined by Shockley-Read-Hall statistics, are given by the following equations [111]:

$$\tau_c = \frac{1}{\sigma \cdot n_s \cdot \upsilon_{th}} \qquad \textbf{Eq. II.38}$$

$$\tau_e = \frac{1}{\sigma \cdot n_1 \cdot \upsilon_{th}} \qquad \textbf{Eq. II.39}$$

where υ_{th} is the thermal velocity, n_s the surface carrier concentration and n_1 the surface carrier concentration when the Fermi level E_f equals to the trap energy E_t. Furthermore, σ is defined:

$$\sigma = \sigma_0 \cdot e^{-\frac{x_t}{\lambda}} \qquad \textbf{Eq. II.40}$$

where σ_0 is the intrinsic cross-section, an important quantity which characterizes the trap, x_t the in-depth location of the trap into the oxide and λ the tunneling attenuation length. Additionally, the trap occupancy factor f_t is:

$$f_t = \frac{1}{1 + e^{(E_t - E_f)/kT}} \qquad \textbf{Eq. II.41}$$

where E_t is the trap energy and E_f the Fermi level position.

II.6.1.5 Flicker Noise

Flicker or "*1/f*" noise is the combination of a few Lorenzian-type spectra. In general, this is the type of noise that dominates in MOSFETs, namely the noise produced by a group of traps in the gate oxide located at very small distances from the interface (*0* to *3 nm*) [112]. The PSD is described by:

$$S_{Id} = K \frac{I_d^{\beta}}{f^{\gamma}}$$ **Eq. II.42**

where K is a constant, β the drain current exponent and γ the frequency exponent. If $\gamma=1$, then the density of the traps is uniform in oxide depth and energy. If $\gamma<1$, then the trap density is increasing near the Si-SiO_2 interface, while if $\gamma>1$, the trap density is increasing deeper in the gate oxide.

II.6.2 Low-Frequency Noise Approaches in Large Area Devices

In general, two physical mechanisms are responsible for the drain current fluctuations: carrier number fluctuations and/or mobility fluctuations.

II.6.2.1 Carrier Number and Correlated Mobility Fluctuations Model

As mentioned above, the main source of the flicker noise is the trapping-detrapping of a group of traps near the gate oxide interface. This interface charge fluctuations δQ_{it} correspond to flatband voltage variations, δV_{fb}:

$$\delta V_{fb} = \frac{-\delta Q_{it}}{(WLC_{ox})}$$ **Eq. II.43**

Then, the drain current fluctuations will be:

$$\delta I_d = -g_m \cdot \delta V_{fb}$$ **Eq. II.44**

where g_m is the device transconductance.

Additionally, the interface charge fluctuations modulate the scattering rate causing a supplementary mobility change, $\delta\mu_{eff}$. Thus, the drain current fluctuations can be modeled as following [113]:

$$\delta I_d = -g_m \delta V_{fb} \mp I_d \mu_{eff} a_{sc} C_{ox} \delta V_{fb}$$ **Eq. II.45**

where μ_{eff} is the effective mobility and α_{sc} the Coulomb scattering coefficient. The sign "–" corresponds to acceptor-like traps, while "+" to donor-like traps.

Therefore, the PSD of the drain current variations induced by carrier number fluctuations with correlated mobility fluctuations (CNF/CMF) will be described by Eq. II.46:

$$S_{I_d} = g_m^2 S_{Vfb} \left(1 \pm a_{sc} \mu_{eff} C_{ox} \frac{I_d}{g_m} \right)^2$$ **Eq. II.46**

where S_{Vfb} is the flatband voltage PSD. If the carrier trapping-detrapping takes place through a tunneling process, then this parameter has the form:

$$S_{Vfb} = \frac{q^2 \lambda k T N_t}{f^{\gamma} W L C_{ox}^2}$$ **Eq. II.47**

where λ is the tunneling attenuation length. According to [98] λ is around 1Å. N_t is the oxide trap surface state density and γ the frequency exponent described in II.6.1.5.

At this point, it is useful to introduce a new quantity, the so-called input-referred gate voltage noise, S_{Vg} [113]:

$$S_{Vg} = \frac{S_{Id}}{g_m^2} \;\Leftrightarrow\; S_{Vg} = S_{Vfb}\left(1 \pm a_{sc}\mu_{eff}C_{ox}\frac{I_d}{g_m}\right)^2 \qquad \textbf{Eq. II.48}$$

If the correlated mobility fluctuations do not have a significant impact on the drain current noise then $\alpha_{sc} \approx 0$ and consequently, $S_{Vg} \approx S_{Vfb.}$

II.6.2.2 Hooge Mobility Fluctuations Model

A totally different approach was proposed by Hooge [99]. In this model the drain current fluctuations are caused by carrier mobility fluctuations, which by turn are induced only by phonon scattering [114], while each conducting carrier contributes independently to the mobility fluctuations [99]. According to these assumptions, the PSD is described as following:

$$S_{Id} = I_d^2 \frac{q\alpha_H}{WLfQ_i} \qquad \textbf{Eq. II.49}$$

where α_H is the Hooge parameter and Q_i the inversion charge.

This approach was proven valid only in bulk semiconductors and metals [115], while was not shown to be applicable in MOSFETs, where the trapping-detrapping of oxide traps is dominant.

II.6.3 Low-Frequency Noise as a Characterization Tool

It is deduced from the above theory that the analysis of LFN measurements has been proven to be extremely useful for the characterization of traps in semiconductor devices and for the reliability of the devices as well. At first when an unknown device is characterized, the dominant noise mechanism and the spatial location of the noise source have to be determined. For this purpose, the bias and geometry dependence of noise should be studied, usually for a small drain voltage. The LFN spectra are composed of 1/f and Lorenzian-type noise components.

Concerning the LFN as a diagnostic tool for the characterization of large area devices, the slow oxide trap density, N_t from Eq. II.47 can be extracted. Indeed, this quantity is shown to be extremely important for the evaluation of the oxide quality after applying specific technological or electrical procedures like for example nitridation [116], [117] and stressing under uniform [118] or hot carrier injections [118], [119]. Then, the Coulomb scattering coefficient, α_{sc} can also be obtained from Eq. II.48 in order to characterize the scattering rate induced by the interface charge fluctuations.

Regarding to the special case of the RTS noise in small area devices, information like the trap time constants, τ_c (Eq. II.38) and τ_e (Eq. II.39), and consequently the location and the energy level of the traps can be extracted by the analytical and careful study of the "Lorenzian-like" spectra. A useful quantity for the extraction of trap characteristics is also the drain current RTS amplitude. Supposing that the trapping of an elementary charge q in the channel changes the local conductivity, then the drain current RTS amplitude in a first order approximation can be calculated as following [100], [118]:

$$\frac{\Delta I_d}{I_d} = \frac{g_m}{I_d}\frac{q}{WLC_{ox}}\left(1 - \frac{x_t}{t_{ox}}\right) \qquad \textbf{Eq. II.50}$$

where x_t is the distance of the trap to the Si-SiO_2 interface and t_{ox} the gate oxide thickness.

II.7 Summary

As transistors are scaling down the accurate determination of their parameters becomes more and more essential in order to understand the physics and to proceed to device optimization. The Y-Function method and the modified Y-Function, suitable for nanoscale MOSFETs are analyzed.

Additionally, the split C-V technique for the extraction of the intrinsic device parameters is discussed. More precisely the huge influence of the AC signal oscillator level on the extracted effective mobility as measured by split C-V technique has been presented. In fact, due to strong non linearity below threshold, the gate-to-channel and, by turn, the channel inversion charge increases linearly with the oscillator level, resulting in a decrease of the extracted effective mobility. The use of small enough oscillator level allows to extracting reliable μ_{eff} values for inversion charge down to 10^{10}q/cm^2 in the very weak inversion region. A physical model accounting for these observations has been developed, which enables to obtain a quantitative description of both inversion charge and effective mobility variations with the oscillator level and the gate voltage.

Furthermore, a new methodology for FDSOI MOSFET parameter extraction was presented. It was verified that the Lambert W function can describe correctly the inversion charge with gate voltage in advanced FDSOI devices making it suitable for a full gate voltage range parameter extraction from weak to strong inversion region. The proposed methodology which takes into account both the back gate voltages and the channel length can be readily applied to evaluate all electrical MOSFET parameters, namely n, V_t, μ_0, θ_1 and θ_2 in parametric test routines. Finally, LFN in MOSFETs and its necessity as a characterization tool is discussed. Representative LFN models are described theoretically.

III Analytical Compact Modeling in FDSOI MOSFETs

III.1 Introduction

As has been already mentioned in Chapter I FDSOI MOSFETs are considered as one of the best candidates for control of SCEs in future sub-28 nm CMOS generations. In order to exploit the benefits of FDSOI UTBB transistors, an accurate and fast simulation tool is required. The threshold voltage is very crucial device parameter for compact modeling of the drain current and consequently of the low-frequency noise through the transconductance of the front and back gates [120]. Analytical models of the threshold voltage for FDSOI MOSFETs have been proposed based on the concept of two dimensional (2D) charge sharing between gate and source/drain regions, leading to underestimated threshold voltage roll-off [121], [122]. Using three-zone Green's function technique to solve the 2D Poisson's equation, the front and back surface potentials were determined from which the threshold voltage expression was obtained [123], [124], [125]. However, although these methods are accurate for channel lengths down to 0.1 μm, they are not suitable for compact modeling as complicated infinite series expansions are involved. Furthermore, analytical threshold voltage models were developed in SOI MOSFETs, where the 2D potential in the silicon body was derived by satisfying Poisson's equation only at the front gate/silicon interface [126], [127].

Recently, a simple analytical threshold voltage model of asymmetrical FDSOI MOSFET has been proposed based on the lateral variations of the front and back surface potentials [128]. In this model, the threshold voltage is defined as the gate voltage at which the surface potential becomes twice the Fermi potential from mid-gap. This definition becomes questionable for modern devices with undoped silicon body and with shrinking the channel length. In [128], the threshold voltage model has been verified for channel lengths down to 0.1 μm, showing underestimated threshold voltage roll-off at short channel lengths. Recently, Biswas and Bhattacherjee [129] developed a threshold voltage model for undoped symmetric double-gate (DG) MOSFETs, in which the impact of the back gate bias and interface roughness on the threshold voltage is included. However, in this model the threshold voltage can be determined by the method of iteration using an equation which includes parameters obtained by numerical solutions of other equations. In [130], a simple analytical threshold voltage model for nano-scale undoped symmetrical double-gate MOSFETs has been developed, defined as the gate voltage at which the minimum carrier charge sheet density reaches a certain value to achieve the turn-on condition.

One of the main purposes of this Chapter is to extend the work of [130] for developing fully analytical expressions for the threshold voltage and ideality factor of lightly doped FDSOI UTBB MOSFETs with asymmetric and independent front and back gates, capturing the impact of the SCEs and back gate bias on these parameters. The models are verified with simulation and experimental results of the front and back gate threshold voltage and ideality factor with variable parameters being the back gate voltage, the drain bias voltage, the channel length, the silicon thickness, the front gate oxide thickness and the back gate oxide thickness. Analytical modeling for the threshold voltage and ideality factor with back gate control is of vital importance for compact modeling of the drain current and transcapacitances of lightly doped FDSOI UTBB MOSFETs, since such modeling will enable existing electronic design automation (EDA) tools for single gate devices to accommodate those new devices.

In the literature, several compact models for asymmetric independent DG MOSFETs have been reported [131], [132], [133], [134], [135], [136], [137], [138], [139], [140], [141]. These models are based on the inversion charge [131], [132], surface potential [133], [134], [135], [136], [137], [138], [139] and threshold voltage [140], [141]. However, most of them either concern long-channel devices or are based on numerical techniques which are less desirable due to the poor speed of simulation. Although the surface potential-based models become more popular, for independent DG MOSFET they are very complex because of the three substrate operating modes: inversion, depletion and accumulation. Recently, an accurate and computationally efficient surface-potential-based model for UTBB SOI MOSFETs has been presented, which provides accurate results when the interface between body and buried oxide is depleted and the back gate is biased in the reverse and low forward bias range [138]. Although this model predicts well the behavior of long and short channel devices, equations for short channel modeling are not discussed. The model presented in [138] has been extended to capture the substrate depletion effect in short channel devices, but without capturing the backside inversion effect [142]. Recently, a surface potential compact model has been proposed covering all operating modes [139]. However, the front surface potential is calculated from a complicated equation by developing an algorithm requiring different computation steps and fundamental effects (such as velocity overshoot and self-heating) in short channel FDSOI devices were not considered. The threshold voltage-based models predict well the behavior of long-channel devices [140] or short-channel devices in the substrate accumulation operating mode [141].

In this Chapter, a threshold voltage-based compact model is proposed, which is accurate for a wide range of back-gate bias in all operating modes and for all channel lengths using few model parameters. Based on the analytical models for the voltage and ideality factor, a complete analytical charge-based compact model for the drain current was derived valid in all regions of operation with back gate control, which includes the channel-length modulation (CLM), DIBL, saturation velocity, mobility degradation, quantum confinement, velocity overshoot and self-heating effects. The proposed model has been validated by comparing the transfer and output characteristics with experimental results and for a wide range of back gate bias voltages. Finally, the drain current compact model has been implemented via Verilog-A code for simulation of fundamental circuits in Cadence Spectre.

III.2 Surface Potential Model Formulation

A schematic cross-section of an asymmetric n-channel FDSOI UTBB MOSFET and the definition of the geometrical characteristics are shown in Figure III-1.

The width of the device is considered to be large to avoid narrow width effects. In narrow width channels, the 3D Poisson's equation leads to complicated expression for the potential distribution, which needs high-class series coefficients to achieve good agreement between numerical solution and analytical expression [123], [124], [125]. Considering the depletion charge in Poisson's equation, in the subthreshold region of lightly doped FDSOI UTBB MOSFETs, the 2D potential distribution $\varphi(x,y)$ along the channel can be expressed with good accuracy as follows [143]:

$$\varphi(x,y) = \varphi_1(x,y) + \varphi_2(x,y)V_g' \qquad \textbf{Eq. III.1}$$

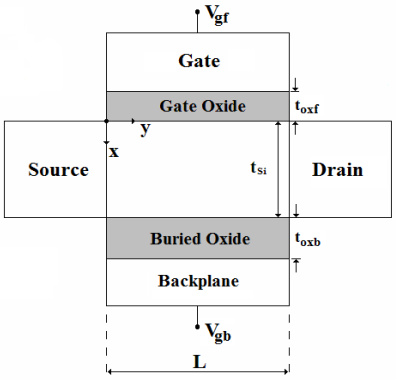


Figure III-1 Schematic representation of the UTBB FDSOI MOSFET cross-section, where V_{gf}= V_g, V_{gb}= V_b, t_{oxf}= t_{ox} and t_{oxb}= t_{box}.

where

$$\varphi_1(x,y)=\frac{\left(e^{\frac{2L-y}{\lambda(x)}}-e^{\frac{y}{\lambda(x)}}\right)V_{bi}+\left(e^{\frac{L+y}{\lambda(x)}}-e^{\frac{L-y}{\lambda(x)}}\right)(V_{bi}+V_d)}{e^{\frac{2L}{\lambda(x)}}-1}+\frac{\left(e^{\frac{L-y}{\lambda(x)}}-e^{\frac{-y}{\lambda(x)}}\right)\left(e^{\frac{L}{\lambda(x)}}-e^{\frac{y}{\lambda(x)}}\right)\left(e^{\frac{y}{\lambda(x)}}-1\right)V_b'\,\beta(x)}{e^{\frac{2L}{\lambda(x)}}-1} \quad \textbf{(a)}$$

Eq. III.2

$$\varphi_2(x,y)=\alpha(x)\frac{\left(1-e^{\frac{-y}{\lambda(x)}}\right)\left(e^{\frac{L}{\lambda(x)}}-e^{\frac{y}{\lambda(x)}}\right)}{e^{\frac{L}{\lambda(x)}}+1} \quad \textbf{(b)}$$

and

$$\alpha(x)=\frac{\varepsilon_{Si}t_{box}+\varepsilon_{ox}(t_{Si}-x)}{\varepsilon_{Si}(t_{ox}+t_{box})+\varepsilon_{ox}t_{Si}} \quad \textbf{(a)}$$

Eq. III.3

$$\beta(x)=\frac{\varepsilon_{Si}t_{ox}+\varepsilon_{ox}x}{\varepsilon_{Si}(t_{ox}+t_{box})+\varepsilon_{ox}t_{Si}} \quad \textbf{(b)}$$

The natural length λ at any position x along the channel layer is given by:

$$\lambda(x)=\sqrt{\frac{\varepsilon_{Si}t_{ox}t_{Si}}{2\varepsilon_{ox}}}\cdot\sqrt{\left(\frac{2\varepsilon_{Si}t_{box}+\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}(t_{ox}+t_{box})+\varepsilon_{ox}t_{Si}}+\frac{\varepsilon_{ox}}{\varepsilon_{Si}t_{ox}}\frac{2\varepsilon_{Si}t_{box}+\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}(t_{ox}+t_{box})+\varepsilon_{ox}t_{Si}}x-\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{x^2}{t_{ox}t_{Si}}\right)} \quad \textbf{Eq. III.4}$$

where ε_{Si} is the dielectric permittivity of silicon, ε_{ox} is the dielectric permittivity of the oxide, t_{ox} is the front gate oxide thickness and t_{box} is the back gate oxide thickness.

In Eq. III.2(a) V_{bi} is the built-in potential across the source/drain-channel junctions given by:

$$V_{bi}=V_{th}\cdot\ln\left(\frac{N_A N_{SD}}{n_i^2}\right) \quad \textbf{Eq. III.5}$$

with V_{th} as the thermal voltage, N_{SD} the donor concentration of the source/drain contacts and n_i the intrinsic carrier concentration of silicon.

Additionally we define $V_g^{'}$ and $V_b^{'}$ as following:

$$V_g^{'} = V_g - V_{fb,f}$$
$$V_b^{'} = V_b - V_{fb,b} \qquad \textbf{Eq. III.6}$$

with V_g the gate voltage of the front gate, V_b the gate voltage of the back gate and $V_{fb,f}$, $V_{fb,b}$ are the flat band voltages of the front and back gates, respectively calculated by the following equations:

$$V_{fb,f} = \Delta\varphi_{ms,f} = \varphi_{m,f} - V_{th} \cdot \ln\left(\frac{N_A}{n_i}\right) \quad \textbf{(a)}$$
$$V_{fb,b} = \Delta\varphi_{ms,b} = \varphi_{m,b} - V_{th} \cdot \ln\left(\frac{N_A}{n_i}\right) \quad \textbf{(b)} \qquad \textbf{Eq. III.7}$$

where $\Delta\varphi_{ms,f}$ and $\Delta\varphi_{ms,b}$ are the front and back gate's work function difference between metal gate/silicon, respectively and $\varphi_{m,f}$ and $\varphi_{m,b}$ are the front and back gate's metal work function respectively.

From equation III.4, the natural lengths of the front gate (λ_{fs}) and back gate (λ_{bs}) associated with the surface potentials φ_s ($x = 0$) and φ_b ($x = t_{Si}$), respectively, are given by:

$$\lambda_{fs} = \sqrt{\frac{\gamma t_{ox} t_{Si}\left(2\gamma t_{box} + t_{Si}\right)}{2\left(t_{Si} + \gamma t_{ox} + \gamma t_{box}\right)}} \quad \textbf{(α)}$$
$$\lambda_{bs} = \sqrt{\frac{\gamma t_{box} t_{Si}\left(2\gamma t_{ox} + t_{Si}\right)}{2\left(t_{Si} + \gamma t_{ox} + \gamma t_{box}\right)}} \quad \textbf{(β)} \qquad \textbf{Eq. III.8}$$

where $\gamma = \varepsilon_{Si}/\varepsilon_{ox}$. It is noticed that these expressions are exactly the same with Suzuki's model [144].

The potential distribution model has been verified by comparing the surface potential with TCAD simulations employing the commercial device simulator ATLAS [145].

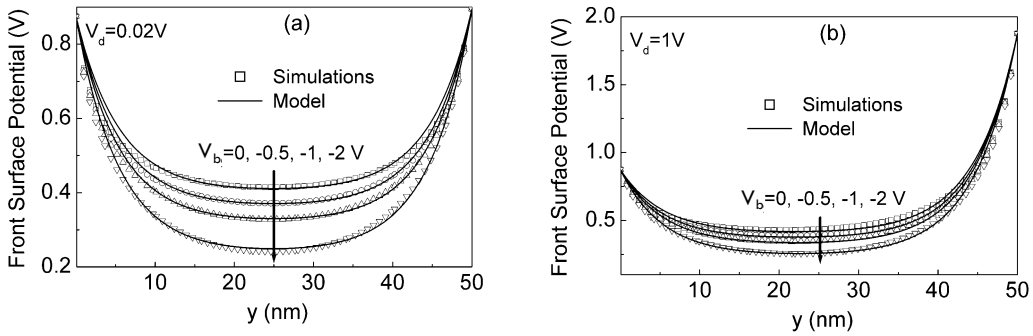


Figure III-2 Front surface potential distribution for a typical long channel (L=50 nm) FDSOI UTBB MOSFET for various values of the back gate voltage V_b. Device parameters: t_{Si} = 10 nm, t_{ox} = 1 nm, t_{box} = 10 nm, V_g = 0.1 V, V_d = 0.02 V (a) and V_d = 1 V (b). Symbols are simulation results and lines are model results.

The device parameters are: t_{ox} = *1.2 nm*, t_{box} = *10 nm*, t_{Si} = *10 nm*, W = *10 μm*, L = *50 nm*, N_A = 10^{15} cm^{-3}, N_{SD} = 10^{20} cm^{-3} and mid-gap gate metal. Excellent matching is observed between the numerical simulations and the analytical model for the surface potential along the channel for different back gate voltages V_b, as shown in Figure III-2 for both low and high drain voltages. The model has been validated for several channel dimensions and bias voltages.

III.3 Threshold Voltage Model

The potential distribution described by Eq. III.1 can be used to model the threshold voltage of UTBB FDSOI MOSFETs, defined quantitatively as the gate voltage at which the minimum carrier charge sheet density Q_{inv} at the effective conductive path reaches a value Q_{thf} adequate to achieve the turn-on condition.

Following the analysis of [130], for effective conductive path located at a distance $x = x_c$ from the front gate interface in weak inversion, the value of V_g at which $Q_{inv} = Q_{thf}$ leads to the simple and explicit expression for the front gate threshold voltage V_{tf}:

$$V_{tf} = V_{fb1} + A_f V_{th} \ln\left(\frac{Q_{thf} N_A}{n_i^2 t_{Si}}\right) - B_f\left[V_{bi} - V_{th}\ln\left(\frac{Q_{thf} N_A}{n_i^2 t_{Si}}\right)\right]^{1/2} \cdot \left[V_{bi} + V_d - V_{th}\ln\left(\frac{Q_{thf} N_A}{n_i^2 t_{Si}}\right)\right]^{1/2} - C_f\left[2V_{bi} + V_d + \beta_f \cosh\left(\frac{L}{\lambda_f}\right)V_b' - \beta_f V_b'\right] \quad \textbf{Eq. III.9}$$

where A_f, B_f and C_f are parameters given by:

$$A_f = \frac{8e^{\frac{2L}{\lambda_f}} \sinh^2\left(\frac{L}{2\lambda_f}\right)\left[1+\cosh\left(\frac{L}{\lambda_f}\right)\right]}{\alpha_f\left(e^{\frac{L}{\lambda_f}} - 1\right)^4} \quad \textbf{(a)}$$

$$B_f = \frac{2e^{\frac{L}{2\lambda_f}}\left(e^{\frac{L}{\lambda_f}} + 1\right)}{\alpha_f\left(e^{\frac{L}{\lambda_f}} - 1\right)^2} \quad \textbf{(b)} \qquad \textbf{Eq. III.10}$$

$$C_f = \frac{8e^{\frac{2L}{\lambda_f}} \sinh^2\left(\frac{L}{2\lambda_f}\right)}{\alpha_f\left(e^{\frac{L}{\lambda_f}} - 1\right)^4} \quad \textbf{(c)}$$

where λ_f, α_f and β_f are obtained from equations III.3 and III.4 for $x = x_c$. The last term of the right hand side of Eq. III.9 reflects the effect of the back gate voltage V_b on V_{tf}. It is noticed that for symmetric lightly doped DG MOSFET one has $V_{fb,f} = V_{fb,b}$, $t_{ox} = t_{box}$, $V_g = V_b$ and Eq. III.9 reduces to the threshold voltage of symmetric DG MOSFET [130].

The value of V_{tf} meets the threshold condition for the onset of the inversion channel creation, i.e. V_{tf} corresponds to the value of V_g which deviates from the exponential relationship in the I_d-V_g semi-logarithmic plot. Thus, the ideality factor of the front interface η_f

can be obtained from the derivative of the minimum potential $\varphi(x_c,y_{min})$ with respect to V_g at $V_g = V_{tf}$ and is given by:

$$\eta_f = \frac{1}{\alpha_f} \cdot \left[1 - K_f \frac{\left(2V_{bi} - 2A_{fc} + V_d\right) e^{\frac{L}{2\lambda_f}} \left(e^{\frac{L}{\lambda_f}} - 1 \right)}{\left(e^{\frac{L}{\lambda_f}} + 1 \right) \left[\left(V_{bi} - A_{fc}\right) \left(e^{\frac{L}{\lambda_f}} - 1 \right) - V_d \right]} \right]^{-1} \qquad \textbf{Eq. III.11}$$

where

$$A_{fc} = \alpha_f V_{tf} + \beta_f V_b' \qquad \textbf{Eq. III.12}$$

$$K_f = \sqrt{\frac{\left(V_{bi} - A_{fc}\right) \left(e^{\frac{L}{\lambda_f}} - 1 \right) - V_d}{\left(V_{bi} - A_{fc}\right) \left(e^{\frac{L}{\lambda_f}} - 1 \right) + V_d \, e^{\frac{L}{\lambda_f}}}} \qquad \textbf{Eq. III.13}$$

Analogous expressions for the back gate threshold voltage V_{tb} and ideality factor η_b can be derived by replacing: λ_f, α_f and β_f with λ_b, α_b and β_b obtained from equations III.3 and III.4 for $x = t_{Si} - x_c$, $V_{fb,f}$ with $V_{fb,b}$ and by exchanging the bias voltages V_g and V_b and the gate capacitances C_{oxf} and C_{oxb}.

For large channel length L, the second term of the right hand side of Eq. III.11 tends to unity and η_f for the front gate interface approaches the ideality factor of long channel transistor given by:

$$\eta_f = \frac{1}{\alpha_f} = 1 + \frac{C_{Si} C_{oxb}}{C_{oxf} \left(C_{Si} + C_{oxb} \right)} \qquad \textbf{Eq. III.14}$$

It is mentioned that in actual nanoscale devices, high-k gate dielectrics are used to control the front gate leakage current, degrading the interface quality compared to the pure thermal oxide of the BOX. If acceptor-type traps appear at the front gate interface of density $D_{it,f}$ per unit area per unit energy, the ideality factor η_f and the flat-band voltage $V_{fb,f}$ which affects the threshold voltage and DIBL should be modified as:

$$\eta_f' = \eta_f + \frac{q^2 D_{it,f}}{C_{oxf}} \qquad \textbf{Eq. III.15}$$

and

$$V_{fb,f}' = V_{fb,f} - \frac{q^2 D_{it,f} \varphi_F}{C_{oxf}} \qquad \textbf{Eq. III.16}$$

where $q\varphi_F$ is the Fermi energy as the device is operated at threshold voltage.

III.3.1 Model Validation

III.3.1.1 Simulation Results

First, the front gate threshold voltage model has been verified by comparing the model with simulation results obtained using the commercial simulator Atlas (Silvaco). Extensive device simulations were performed using physical models accounting for the drift-diffusion (DD) carrier transport using the Boltzmann approximation. In order to simplify the simulations, we consider constant low-field mobility ($\mu_0 = 150\ cm^2/Vs$) in the subthreshold region ignoring mobility degradation and saturation velocity $\upsilon_{sat} = 10^7\ cm/s$. The device parameters are: channel width $W = 10\ \mu m$, channel length $L = 20\text{-}90\ nm$, silicon thickness $t_{Si} = 10\text{-}30\ nm$, front gate equivalent oxide thickness $t_{ox} = 1\text{-}2\ nm$, back gate oxide thickness $t_{box} = 10\text{-}30\ nm$, doping concentration of silicon $N_A = 10^{15}\ cm^{-3}$, doping concentration of source/drain contacts $N_{SD} = 10^{20}\ cm^{-3}$ and mid-gap gate metal with work-function $4.61\ eV$. Quantum effects, which become significant as the silicon layer thickness is scaled below 10 nm, were not considered in the TCAD simulations by excluding the Bohm quantum potential model [145]. However, as the future CMOS devices will be scaled down by both channel length and Si body thickness, the quantum correction to inversion charge due to gate field induced electrostatic confinement should be taken into account even for Si body thickness above 10 nm.

It is noticed that the DD transport model describes accurately the drain current of single-gate and DG MOSFETs with channel lengths down to 40 nm [146]. For channel lengths shorter than 30 nm, Quasi-ballistic transport could become more dominant, resulting in an overestimation of the on-currents compared to the on-currents obtained by the DD transport. It has been shown that simple modification of the saturation velocity in the DD model reproduces the same on-current as the Monte Carlo method [146]. However, in the subthreshold region the DD current is not affected by the ballistic transport as shown in [146], indicating that the parameters V_t and n are correct as extracted from the transfer characteristics of the DD model.

In the real device applications, the back-gate in UTBB FDSOI is used to tune the threshold voltage defined by the front-gate. Within this regime, the back-gate is more or less depleted instead of inverted. As confirmed by numerical simulations [147], the inversion charge density distribution across the silicon layer of the front gate strongly depends on the bias V_b of the back gate. When the back interface is depleted, i.e. in the negative V_b range, the peak of the inversion charge distribution is close to the front gate interface, suggesting that the effective conductive path is located near the front gate interface. Larger negative V_b value pushes the peak of the inversion charge distribution closer to the front gate interface. The relative impact of the back gate bias on the location x_c of the effective conductive path from the silicon surface can be modeled with the relation:

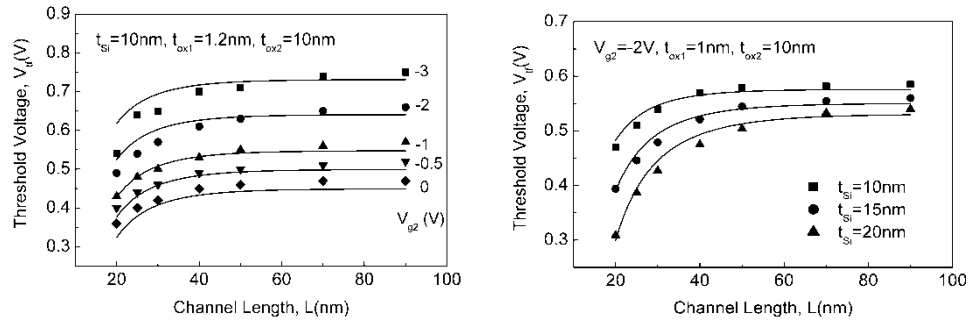
$$\frac{x_c}{t_{Si}} = A_c\, e^{\frac{V_b}{B_c}} \qquad \textbf{Eq. III.17}$$

where the constants A_c and B_c are model parameters.

The front gate threshold voltage V_{tf} has been calculated from the transfer characteristics measured at drain voltage $V_d = 20\ mV$ using the constant current method [124]. In this method, V_{tf} is defined as the V_g value for which the normalized drain current $I_{d,,norm}$ =

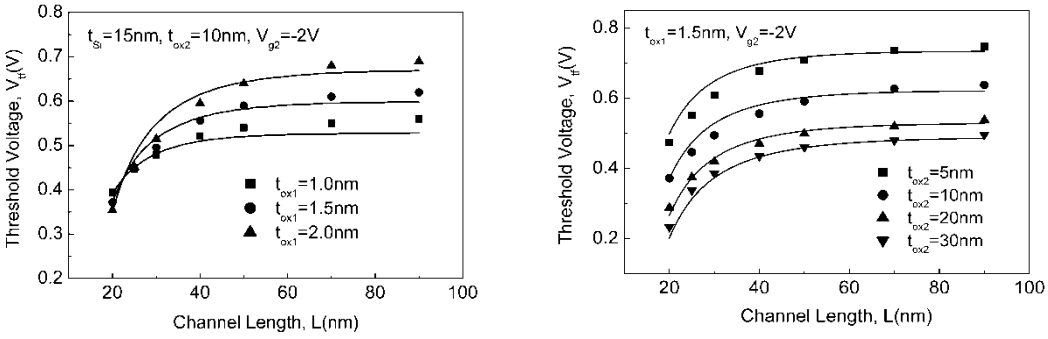
(L/W)I_d reaches a certain magnitude I_{ref}, used as a reference current. The reference current is defined as the normalized current at $V_g = V_{tf}$ of long channel device operating at low V_d, in which V_{tf} is extracted using the extrapolation method on the I_d-V_g curve at V_g where the maximum transconductance occurs [124]. The analytical front gate threshold voltage model (Eq. III.9) matches the simulation results for all drain voltages and combinations of device dimensions. Figures III-3, III-4 and III-5 show the simulation results of V_{tf} versus L for UTBB FDSOI MOSFETs with the back gate voltage V_b, the silicon thickness t_{Si}, the front gate oxide thickness t_{ox}, the back gate oxide thickness t_{box} and the drain bias voltage V_d as parameters. For geometrical parameters lying within wide ranges in real device applications [120], [148], i.e. for $L = 20\text{-}90\ nm$, $t_{Si} = 10\text{-}20\ nm$, $t_{ox} = 1\text{-}2\ nm$ and $t_{box} = 5\text{-}30\ nm$, over wide bias ranges the resulting model parameters for the effective conductive path are $A_c = 0.05$, $B_c = 3.1\ V$ and the functional dependence of Q_{thf} on V_d has been found to be:

$$Q_{thf} = 7 \cdot 10^{10} \left[1 + 8 V_d \frac{\lambda_f}{L} + 4 \frac{t_{ox}}{t_{box}} \right]^{-2} \qquad \textbf{Eq. III.18}$$



(a) **(b)**

Figure III-3 Front gate voltage versus channel length for various values of the back gate voltage $V_{g2} = V_b$ of FDSOI UTBB MOSFETs with $t_{Si} = 10$ nm (a) and for various values of the silicon thickness t_{Si} with $V_{g2} = V_b = -2$ V (b). The front and back gate oxide thicknesses are $t_{ox1} = t_{ox} = 1$ nm and $t_{ox2} = t_{box} = 10$ nm, respectively. Symbols are simulation results and lines are model results.



(a) **(b)**

Figure III-4 Front gate threshold voltage versus channel length for various values of front gate oxide thickness $t_{ox1} = t_{ox}$ of FDSOI UTBB MOSFETs with $t_{ox2} = t_{box} = 10$ nm (a) and for various values of back gate oxide thickness, t_{box} with $t_{ox1} = t_{ox} = 1.5$ nm (b). The channel thickness is $t_{Si} = 15$ nm and the back gate voltage is $V_{g2} = V_b = -2$ V. Symbols are simulation results and lines are model results.

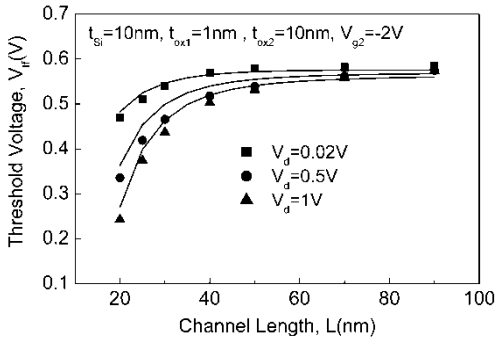


Figure III-5 Front gate voltage versus channel length for various values of the drain bias voltage of FDSOI UTBB MOSFETs with t_{Si} = 10 nm, t_{ox1} = t_{ox} = 1 nm, t_{ox2} = t_{box} = 10 nm and V_{g2} = V_b = -2 V. Symbols are simulation results and lines are model results.

The physical mechanism behind Eq. III.18 consists in the penetration of the drain field laterally within the BOX toward the source and channel inversion [149]. In this way, the drain electrode plays a role of a secondary gate contributing to electrostatic induction of carriers in the inversion layer [149], which is modeled by a decrease of Q_{thf} with increasing V_d according to Eq. III.18. Figure III-6 shows the dependence of the front gate threshold voltage on the back gate bias V_b. The threshold voltage V_{tf} increases almost linearly with $|V_b|$ for channel lengths 20 and 70 nm. The results of Figure III-6 show that the short-channel immunity is rather insensitive to the back gate bias. The above results demonstrate the validity of the proposed threshold voltage model for ratio t_{Si}/L, controlling the electrostatic integrity of the device, up to 1.

The back gate threshold voltage V_{tb} has been derived using the critical threshold carrier charge sheet density Q_{thb} adequate to achieve the turn-on condition, defined as:

$$Q_{thb} = 7 \cdot 10^{10} \left[1 + 8 V_d \frac{\lambda_b}{L} + 4 \frac{t_{box}}{t_{ox}} \right]^{-2} \qquad \textbf{Eq. III.19}$$

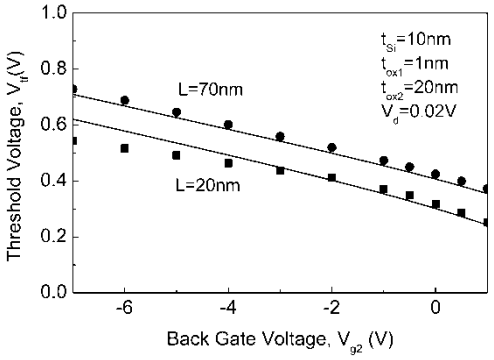


Figure III-6 Front gate threshold voltage versus channel length for various values of the back gate bias voltage V_{g2} = V_b of FDSOI UTBB MOSFETs with t_{Si} = 10 nm, t_{ox1} = t_{ox} = 1 nm, t_{ox2} = t_{box} = 20 nm and channel lengths L = 20 and 70 nm. Symbols are simulation results and lines are model results.

The dependence of the back gate threshold voltage V_{tb} on the channel length is shown in Figure III-7 for different values of V_g. As can be seen, the present model predicts with very good accuracy also the back gate threshold voltage for different front gate biases.

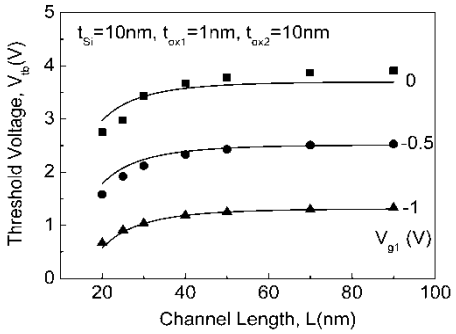


Figure III-7 Back gate threshold voltage versus channel length for various values of the front gate voltage $V_{g1} = V_g$ of FDSOI UTBB MOSFETs with t_{Si} = 10 nm, $t_{ox1} = t_{ox}$ = 1 nm and $t_{ox2} = t_{box}$ = 10 nm. Symbols are simulation results and lines are model results.

The DIBL effect, which characterizes the SCEs, is defined as the difference between the linear ($V_{d,low} = 0.02\ V$) and saturation ($V_{d,high} = 1\ V$) threshold voltages. From Eq. III.9, the DIBL parameter of the front gate UTBB FDSOI MOSFETs can be written as:

$$DIBL_f = A_f V_{th} \ln\left(\frac{Q_{thf,low}}{Q_{thf,high}}\right) + B_f\left[V_{bi} - V_{th}\ln\left(\frac{Q_{thf,high}N_A}{n_i^2 t_{Si}}\right)\right]\cdot\sqrt{V_{d,high}\left[V_{bi} - V_{th}\ln\left(\frac{Q_{thf,high}N_A}{n_i^2 t_{Si}}\right)\right]}$$
$$- B_f\left[V_{bi} - V_{th}\ln\left(\frac{Q_{thf,low}N_A}{n_i^2 t_{Si}}\right)\right]\cdot\sqrt{V_{d,low}\left[V_{bi} - V_{th}\ln\left(\frac{Q_{thf,low}N_A}{n_i^2 t_{Si}}\right)\right]} + C_f\left(V_{d,high} - V_{d,low}\right) \quad \textbf{Eq. III.20}$$

The variation with channel length of the $DIBL_f$ coefficient described by Eq. III.20 shows good agreement with the numerical results for a FDSOI MOSFET with $t_{ox} = 1\ nm$, $t_{box} = 10\ nm$, $t_{Si} = 10\ nm$ and $V_b = -2\ V$ as shown in Figure III-8, confirming the accuracy of the V_{tf} model. It is observed that the parameter $DIBL_f$ is degraded for channel lengths below 40 nm due to enhancement of the V_{tf} roll-off with decreasing L at a constant V_d, as shown in Figure III-5.

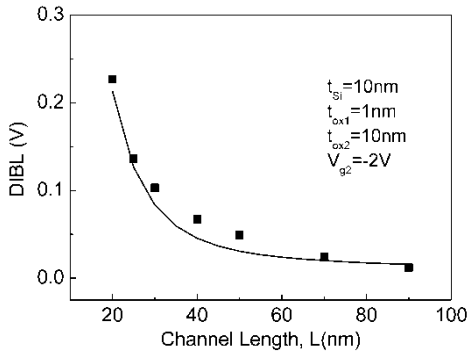


Figure III-8 DIBL versus channel length for FDSOI UTBB MOSFETs with t_{Si} = 10 nm, $t_{ox1} = t_{ox}$ = 1 nm, $t_{ox2} = t_{box}$ =10 nm and $V_{g2} = V_b$ = -2V. Symbols are simulation results and lines are model results.

III.3.1.2 Experimental Results

Furthermore, the front gate threshold voltage model has been verified by comparing the model with experimental results. The devices measured for this purpose are n-channel transistors issued from 14 nm FDSOI CMOS technology with channel width $W = 10\ \mu m$ and channel lengths $L = 17,\ 37$ and $87\ nm$, fabricated in LETI-CEA in France. The doping concentration of the channel is $N_A = 10^{15}\ cm^{-3}$ and the doping concentration of the source/drain contacts is $N_{SD} = 10^{20}\ cm^{-3}$ The front gate stack consists of TiN/Hf-based oxide with equivalent oxide thickness 1.2 nm, the back gate oxide thickness is 10 nm and the silicon film thickness is 8.7 nm [148]. The front gate threshold voltage and ideality factor were extracted from the transfer characteristics, measured at $V_d = 30\ mV$ and different back gate voltages V_b.

In the experimental UTBB FDSOI MOSFETs, as the silicon thickness is scaled below 10 nm, structural confinement and transverse electric field-induced confinement lead to carrier-energy quantization, which results in increased V_{tf} and degraded gate capacitance or reduced inversion charge [150]. Thus, for complete threshold voltage modeling considering for structural confinement along the silicon thickness direction the lowest-subband, the quantum effects are modelled with increasing the threshold voltages V_{tf} and V_{tb} by the amount [151], [152]:

$$\Delta V_t^{QM} = \frac{(\pi \hbar)^2}{2qm_{eff}t_{Si}^2} \qquad \textbf{Eq. III.21}$$

where $\hbar$ is the reduced Planck's constant and m_{eff} is the effective mass of electrons along the confinement direction (e.g. $m_{eff} = 0.7\ m_0$, where m_0 is the free electron mass). In addition to the structural confinement, quantum distribution of the inversion charge results in an increase of the front gate oxide thickness by [151], [152]:

$$t_{ox}^{QM} = t_{ox} + \Delta z \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \qquad \textbf{Eq. III.22}$$

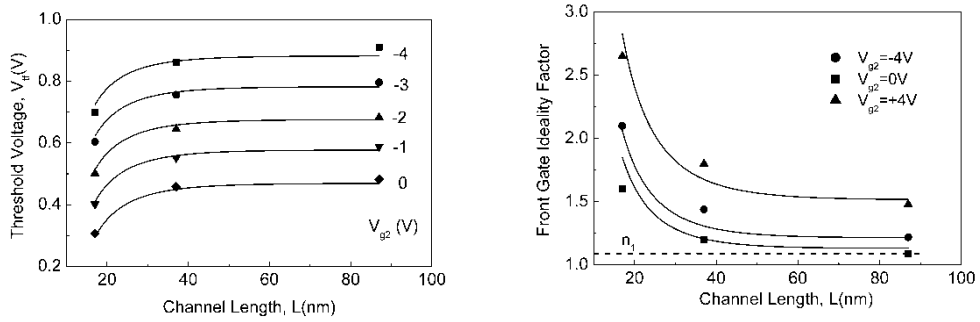
where $\Delta z = 0.3\ nm$. The quantum effect of the inversion charge distribution on the back gate oxide is negligible due to its large thickness. Thus, including the quantum effects, t_{ox} is replaced with t_{ox}^{QM} and V_{tf} with $V_{tf} + \Delta V_t^{QM}$. The experimental plots of V_{tf} versus L for different back gate voltages V_b at $V_d = 0.03\ V$ and the results obtained by our model are shown in Figure III-9(a). It is observed that the V_{tf} values from the analytical model are in close proximity with the experimental results. It is emphasized that threshold voltage shift due to interface roughness is insignificant for channel thickness exceeding 5 nm [129].

The variation of the measured front gate ideality factor $\eta_{f,meas}$ with the gate length for different back gate voltages V_b for the experimental devices are presented in Figure III-9(b). When the back-gate is biased in the depletion mode ($V_b = -4\ V$), the measured ideality factor $\eta_{f,meas}$ of long channel devices coincides with the ideality factor of the front interface η_f calculated from Eq. III.14. For channel lengths below 40 nm, $\eta_{f,meas}$ is degraded due to the SCEs. By changing the bias voltage of the back gate from depletion to the inversion mode ($V_g = +4\ V$), $\eta_{1,meas}$ of long channel devices increases approaching the value of the ideality factor of the back interface $\eta_b = 3.44$ calculated from an expression analogous to Eq. III.14 by exchanging C_{oxf} and C_{oxb}. This experimental finding indicates the involvement of the back gate in the measured ideality factor of the front gate. Taking into account the relative impact

of the back gate interface on the ideality factor of the front gate, the measured ideality factor $\eta_{f,meas}$ can be modeled as:

$$\eta_{f,meas} = \eta_f \left(1 - \frac{x_c}{t_{Si}}\right) + \eta_b \frac{x_c}{t_{Si}} \qquad \textbf{Eq. III.23}$$

where the normalized effective conductive path x_c/t_{Si} is given by Eq. III.17 in terms of the back-gate bias. Using the function for the critical threshold carrier sheet density (Eq. III.18), the $\eta_{f,meas}$ values from the analytical model are in good agreement with the experimental results as shown in Figure III-9(b). Thus, the overall results show that the presented analytical models of the threshold voltage and ideality factor for the front and back gates of FDSOI UTBB MOSFETs are in good agreement with simulation and experimental results within a wide range of bias voltages and device dimensions.



(a) **(b)**

Figure III-9 Front gate threshold voltage versus channel length (a) and front gate ideality factor versus channel length (b) for various values of back gate voltage $V_{g2} = V_b$ of experimental FDSOI UTBB MOSFETs with t_{Si} = 8.7 nm, t_{ox} = 1.2 nm and t_{box} = 10 nm measured at V_d = 0.03 V. Symbols are experimental results and lines are model results.

III.3.2 Improvement of the Threshold Voltage Model: Analytical Threshold Voltage Model

The threshold voltage described in the previous section [153] is defined quantitatively as the gate voltage at which the minimum carrier charge sheet density at the effective conductive path reaches a value Q_{th} adequate to achieve the turn-on condition. The empirical expression for Q_{th} (equations III.18 and III.19) has been derived in terms of the drain bias V_{ds}, the device geometrical parameters and the effective conductive path parameters to fit the model with simulated results. In this section, we derive an analytical threshold voltage model for FDSOI MOSFETs, using a definition from the literature based on the electron density at the front and back channels simultaneously [154].

In deep submicrometer FDSOI MOSFETs, it has been shown that the threshold voltage can be defined analytically and with good accuracy as the gate voltage at which the sum of the electron densities at the front and the back channels reaches the doping density of the silicon body [154]. Considering that the work functions of the front and back metal gates are close, in the case where the front gate oxide is much thinner, the case for dominance of the front channel is sufficient to explain the experimental results for a wide range of back gate bias. Furthermore, to derive analytical expression for the threshold voltage, the effective conductive path concept, which has already been introduced in the previous section, should be

accounted for [153]. Thus, for thinner front gate oxide, the threshold voltage is defined as the gate voltage at which the electron density at the effective conductive path located at a distance $x = x_c$ from the front interface is equal to the doping density N_A of the silicon body, i.e.:

$$n_i e^{\frac{\varphi(x_c,y_m)}{V_{th}}} = N_A \qquad \textbf{Eq. III.24}$$

where $\varphi(x_c,y_m)$ (Eq. III.1) is the channel potential at the conductive path x_c and the position y_m of the minimum potential which shows weak dependence on the gate voltage in the subthreshold region [155], V_{th} is the thermal voltage and n_i is the intrinsic carrier concentration of silicon.

Thus, using the surface potential model described above, the front gate threshold voltage can be derived from the relation:

$$n_i e^{\frac{\varphi_1(x_c,y_m)+\varphi_2(x_c,y_m)V_{tf}}{V_{th}}} = N_A \qquad \textbf{Eq. III.25}$$

from which we obtain the explicit expression:

$$V_{tf} = V_{fb,f} + \frac{V_{th}}{\varphi_2(x_c,y_m)} \ln\left(\frac{N_A}{n_i} e^{\frac{-\varphi_1(x_c,y_m)}{V_{th}}}\right) \qquad \textbf{Eq. III.26}$$

In Eq. III.26, the V_{tf} dependence on V_b is captured through the potential $\varphi_1(x_c,y_m)$ which is described by Eq. III.2(a).

For compact modeling, the quantum confinement effect has been considered in the model with decreasing the semiconductor work function φ_s by the minimum energy of the lowest conduction sub-band to a new work function φ_{snew} [156]. Thus, the shift in V_{tf} due to quantum confinement is included in the model considering the work function difference as [156]:

$$\Delta\varphi = \varphi_m - \varphi_{snew} \qquad \textbf{Eq. III.27}$$

where φ_m is the gate metal work function. The shift in the threshold voltage due to the quantum confinement is:

$$\Delta V_{tf} = 0.085 + \frac{2.178}{t_{Si}^2} \qquad \textbf{Eq. III.28}$$

proposed in BSIM-IMG [138], where t_{Si} is expressed in nm. The application of compact models in ultra thin symmetric common double gate and asymmetric independent double gate MOSFETs demonstrates that the threshold voltage shift due to structural confinement is sufficient to predict with good accuracy the current-voltage characteristics, without considering the quantum degradation of the gate capacitance [138], [156].

The threshold voltage model has been verified by comparing the model with experimental results. The devices measured are n-MOS transistors with back-plane, issued from 28 nm FDSOI CMOS technology with channel width $W = 0.5\ \mu m$, channel length $L = 30\ nm$, fabricated by ST Microelectronics in France [157]. The doping concentration of the channel is $N_A \approx 10^{15}\ cm^{-3}$ and the doping concentration of the source/drain contacts is $N_{SD} \approx 10^{20}\ cm^{-3}$. The front gate stack consists of TiN/HfO_2-based dielectric with equivalent oxide thickness 1.55 nm, the BOX thickness is 25 nm and the silicon film thickness is 7 nm. The change of the TiN work function from 4.3 to 4.65 eV depending on the process parameters

[158] and the variability of the TiN work function due to grain-orientation [159] introduce uncertainty for determining $\Delta\varphi_{ms,f}$. The substrate is standard p-type lightly doped silicon, implanted with In to form a thin localized highly doped (~ 10^{18} cm^{-3}) p-type layer underneath the BOX. Taking the value of 4.05 eV for the electron affinity of the silicon, the determined work function difference for the back gate is $\varphi_{m,b}$ = 0.17 V. Considering a decrease of the silicon work function by about 0.13 V due to quantum confinement for $t_{Si} = 7\ nm$, then it is $\varphi_{m,b} = 0.3\ V$.

Figure III-10 shows the dependence of the front gate threshold voltage V_{tf} on the back gate bias V_b. The values of V_{tf} calculated from the model are compared with the experimental values extracted from the transconductance linear extrapolation method [155], as both values are determined at the onset of inversion. The impact of the back gate bias on the location of the effective conductive path x_c has been modeled with the empirical relations:

$$\frac{x_c}{t_{Si}} = A_c e^{\left(\frac{V_b}{B_c}\right)} \quad \text{if} \quad V_b \le 0 \qquad \textbf{(a)}$$

$$\frac{x_c}{t_{Si}} = A_c + 0.04 V_b \quad \text{if} \quad V_b > 0 \qquad \textbf{(b)}$$

Eq. III.29

which are in qualitative agreement with simulation results of the mean channel position in UTBB FDSOI MOSFETs [160]. The model values of V_{tf} were obtained using $\varphi_{m,f} = 0.37\ V$, $A_c = 0.2$ and $B_c = 3.1\ V$ for the devices of the investigated SOI technology. It is noticed that $\varphi_{m,f} = 0.37\ V$ is primarily an adjustment to the real V_{tf} values, which includes the V_{tf} shift due to quantum confinement [138] and interface traps [153], in addition to the work function difference between metal gate and silicon. The results of Figure III-10 demonstrate the validity of the modified threshold voltage model. The parameters $\Delta\varphi_{ms,f}$, A_c and B_c, extracted from the experimental data of V_{tf} versus V_b, are used in the drain current model, described in the next section.

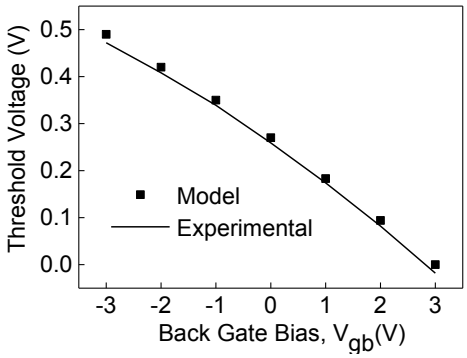


Figure III-10 Front gate threshold voltage V_{tf} versus back gate voltage $V_{gb} = V_b$ of UTBB FDSOI MOSFET with W = 0.5 µm, L = 30 nm, t_{ox} = 1.55 nm, t_{box} = 25 nm, t_{Si} = 7 nm and $N_A = 10^{15}$ cm^{-3}

Concerning the improvement in the modelling of the increase of the front gate oxide thickness due to quantum distribution of the inversion charge, this effect is taken into account in modifying the ideality factor prior the drain current calculation. In UTBB FDSOI MOSFETs, positive V_b moves the mean channel position deeper away from the front gate interface into the silicon film [160]. Thus, in addition to the threshold voltage described by Eq. III.26 in terms of the mean channel position, the following back gate bias dependent equivalent thicknesses for the front gate oxide and silicon body are applied to η_f (Eq. III.11) to refine afterwards, the drain current calculation [160]:

$$t_{ox,eq} = t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{Si}} x_c \quad \textbf{(a)}$$

$$t_{Si,eq} = t_{Si} - \frac{\varepsilon_{ox}}{\varepsilon_{Si}} x_c \quad \textbf{(b)}$$

Eq. III.30

III.4 Analytical Drain Current Model

In charge-based models, the drain current calculation is usually based on the linear or exponential dependence of the channel charge density in the strong or in the subthreshold regions of operation, respectively. In independent asymmetric double gate device operation, the front interface charge becomes relevant to compute the drain current by defining the threshold voltage and ideality factor at an effective conductive path controlled by the back gate bias [153]. Starting from the channel charges, in subthreshold region the charge sheet density is defined as [141]:

$$Q_i^{wi} = \eta_f \, C_{oxf} \, V_{th} \, e^{\frac{V_g - V_{tf} - \eta_f V_y}{\eta_f V_{th}}} \qquad \textbf{Eq. III.31}$$

and in strong inversion region it becomes:

$$Q_i^{si} = C_{oxf}\left(V_g - V_{tf} - \eta_f \, V_y\right) \qquad \textbf{Eq. III.32}$$

In equations III.31 and III.32, C_{oxf} is the front gate oxide capacitance per unit area, η_f is the ideality factor of the front gate interface and V_y the quasi Fermi potential in the channel ($V_y = 0$ at the source and $V_y = V_{ds}$ at the drain). The short-channel effects and the coupling of the front and back gates are included in these equations through the parameters V_{tf} and η_f [153].

In order to obtain a single expression for the inversion charge density denoted by Q_i, valid from the sub-threshold to the strong inversion region, the first order approximation of the Lambert W-function has been used:

$$Q_i = \eta_f \, C_{oxf} \, V_{th} \ln\left(1 + e^{\frac{V_g - V_{tf} - \eta_f V_y}{\eta_f V_{th}}}\right) \qquad \textbf{Eq. III.33}$$

Using the normalized inversion sheet charge density

$$q_i = \frac{Q_i}{C_{oxf} \, V_{th}} \qquad \textbf{Eq. III.34}$$

which is valid in all regions of operation, Eq. III.33 becomes:

$$q_i = \eta_f \ln\left(1 + e^{\frac{V_g - V_{tf} - \eta_f V_y}{\eta_f V_{th}}}\right) \qquad \textbf{Eq. III.35}$$

The expression for the drain current is derived taking into account the charge distribution in the entire channel instead of the charge sheet approximation, which introduces some error in the moderate inversion region. Based on drift-diffusion transport, the drain current at any point y in the channel is given by [138]:

$$I_{ds} = W\mu\, C_{oxf}\, V_{th}\, q_i \frac{dV_y}{dy} \qquad \textbf{Eq. III.36}$$

where μ is the electron mobility, W is the gate width and L is the gate length. With including the carrier saturation velocity effect, the mobility can be approximated as follows [156]:

$$\mu = \frac{\mu_{eff}}{1 + \frac{\mu_{eff}}{\upsilon_{sat}} \left| \frac{d\varphi_s}{dy} \right|} = \frac{\mu_{eff}}{1 + \frac{\mu_{eff}\, V_{th}}{\upsilon_{sat}} \frac{dq_i}{dy}} \qquad \textbf{Eq. III.37}$$

where φ_s is the surface potential, υ_{sat} is the saturation velocity with best value in MOS transistors $\approx 2 \times 10^7$ *cm/s* [161] and μ_{eff} is the effective carrier mobility which includes the effect of the transversal field. From Eq. III.35, we obtain:

$$\frac{dq_i}{dy} = \frac{\eta_f}{V_{th}} \left(e^{\frac{-q_i}{\eta_f}} - 1 \right) \frac{dV_y}{dy} \qquad \textbf{Eq. III.38}$$

Using equations III.37, III.38, integration from the source to the drain results in the following drain current equation in terms of the normalized charges at the source (q_s) and drain (q_d) electrodes:

$$I_{ds} = W \frac{\mu_{eff}}{L + \frac{\mu_{eff}\, V_{th}}{\upsilon_{sat}} (q_s - q_d)} C_{oxf} \frac{V_{th}}{\eta_f} \int_{q_s}^{q_d} \frac{q_i}{e^{\frac{-q_i}{\eta_f}} - 1} dq_i \qquad \textbf{Eq. III.39}$$

The integral in Eq. III.39 can be written in terms of a dilogarithm function:

$$I_{ds} = \frac{W\mu_{eff} C_{oxf}\, V_{th}^2\, \eta_f}{L + \frac{\mu_{eff} V_{th}}{\upsilon_{sat}} (q_s - q_d)} \left[poly\log\left(2.1 - e^{\frac{q_i}{\eta_f}} \right) - \frac{\pi^2}{6} \right]_{q_s}^{q_d} \qquad \textbf{Eq. III.40}$$

In order to express the drain current equation explicitly in terms of the charge densities q_s and q_d, in Eq. III.40 the dilogarithm function is replaced by the first two terms of the Taylor series expansion as:

$$poly\log\left(2.1 - e^{\frac{q_i}{\eta_f}} \right) = -\frac{q_i}{\eta_f} - \left(\frac{q_i}{2\eta_f} \right)^2 \qquad \textbf{Eq. III.41}$$

In Eq. III.41, the error between the exact value of the dilogarithm function of the left hand side and the analytical function of the right hand side is up to about 60% in the strong inversion region, as shown in Fig. III-11. This error is minimized with the analytical function (Eq. III.42) for the dilogarithm function (Fig. III-11):

$$poly\log\left(2.1 - e^{\frac{q_i}{\eta_f}} \right) = -\frac{q_i}{\eta_f} - \frac{q_i^2}{2\eta_f^2} \qquad \textbf{Eq. III.42}$$

This analytical function (Eq. III.42) is used in Eq. III.40 for compact modeling purpose. Thus, combining these two equations, we obtain the following analytical expression for I_{ds} in terms of the normalized charges q_s and q_d:

$$I_{ds} = \frac{W\mu_{eff} C_{oxf} V_{th}^2}{L + \frac{\mu_{eff} V_{th}}{\upsilon_{sat}}(q_s - q_d)} \left[(q_s - q_d) + \frac{1}{2\eta_f}\left(q_s^2 - q_d^2\right) \right] \qquad \textbf{Eq. III.43}$$

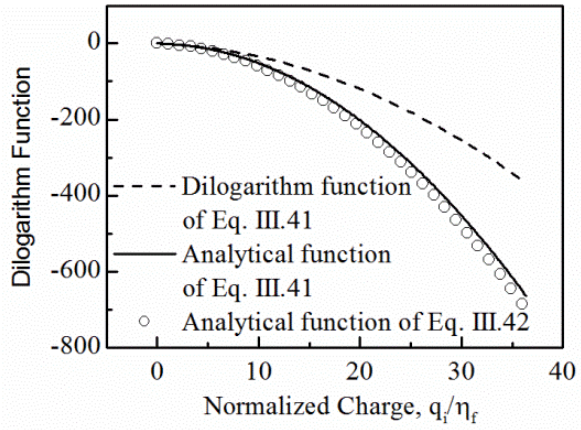


Figure III-11 Dilogarithm function of Eq. III.41 and analytical function of the right hand side of Eq. III.41 as a function of q_i/η_f showing large error in the strong inversion region. The error is minimized using the optimized analytical function of Eq. III.42.

We note that Eq. III.43 constitutes the basic structure of compact drain current models like Berkeley Short-channel IGFET model (BSIM) [156], [162].

The effective mobility μ_{eff} degradation due to the vertical gate field is expressed in terms of the charge at the source side q_s as [163]:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1 V_{th}\, q_s + \theta_2 (V_{th}\, q_s)^2} \qquad \textbf{Eq. III.44}$$

where μ_0 is the low-field mobility, θ_1 and θ_2 are the mobility attenuation factors of first and second order, which can be extracted from experimental data at low drain voltage using a modified Y-function method, as described in Section II.3. The parameter θ_2 is correlated to the surface roughness scattering, while θ_1 includes phonon scattering and Coulomb scattering. Taking into account the effect of the series resistance R_{sd}, the mobility attenuation factor θ_1 is described by Eq. II.11.

In saturation region, based on [103], [164] the channel length shortening ΔL due to the channel length modulation effect can be modelled as:

$$\Delta L = \lambda_f \ln\left(1 + \frac{(V_{ds} - V_{dsat} + 0.05)\tanh\left(\frac{V_{ds}}{V_{dsat}}\right)^3}{V_E} \right) \qquad \textbf{Eq. III.45}$$

where λ_f is the natural length at the conductive path and V_E is a fitting parameter. It should be noted that Eq. III.43 will lead to an implicit expression for the saturation drain voltage V_{dsat}. Considering that the second charge term in the brackets of Eq. III.43 is dominant in the above-threshold region, an explicit expression for V_{dsat} can be obtained from the relation $dI_{ds}/dV_{ds} = 0$ yielding:

$$V_{dsat} = \sqrt{\left(\frac{\upsilon_{sat} L}{\mu_{eff}}\right)^2 + \frac{2 q_s V_{th} \upsilon_{sat} L}{\mu_{eff}}} - \frac{\upsilon_{sat} L}{\mu_{eff}} + \frac{q_s V_{th}}{\eta_f} - q_s V_{th} \qquad \textbf{Eq. III.46}$$

Including the channel length modulation effect, the drain current equation becomes:

$$I_{ds} = \frac{W \mu_{eff} C_{oxf} V_{th}^2}{L_{eff} + \frac{\mu_{eff} V_{th}}{\upsilon_{sat}}(q_s - q_d)} \left[(q_s - q_d) + \frac{1}{2\eta_f}\left(q_s^2 - q_d^2\right) \right] \qquad \textbf{Eq. III.47}$$

where

$$L_{eff} = L - \Delta L \qquad \textbf{Eq. III.48}$$

The first charge term in the brackets of Eq. III.47 dominates in weak inversion, while the second charge term in the brackets and the charge term in the denominator dominate in the strong inversion region. As the threshold voltage V_{tf} is determined at the onset of inversion [153], we found that for a smooth transition from weak to strong inversion, the charge of weak inversion should be obtained from Eq. III.35 with increasing V_{tf} by $2.5 \times V_{th}$ and the charge terms of strong inversion with increasing V_{tf} by $5 \times V_{th}$.

III.4.1 Improvement of the Drain Current Compact Model

The SCEs, the mobility degradation, the saturation velocity, the quantum-mechanical effects (QMEs) and the coupling of front-back gates were already taken into account in the model through the threshold voltage, the sub-threshold swing coefficient and the carrier mobility. In order to improve the accuracy of the model, we include some other important effects, namely, the velocity overshoot and the self-heating effects.

In short-channel transistors, in contrast to the classical drift-diffusion models, the saturated velocity in the saturation region can achieve higher values than υ_{sat} due to non-stationary effects. This phenomenon is known as velocity overshoot (VO) [165]. Taking into consideration the velocity overshoot effect for nanoscale devices, the contribution of the velocity overshoot in Eq. III.47 is introduced in a simple way by adding a term in the saturation velocity as [165]:

$$\upsilon_{sat,vo} = \upsilon_{sat}\left(1 + \frac{2\lambda_w}{L}\right) \qquad \textbf{Eq. III.49}$$

where λ_w is the energy-relaxation length defined as $\lambda_w \approx 2\upsilon_{sat}\tau_w$, with τ_w being the energy relaxation time constant.

Due to the thin silicon thickness in short UTBB FDSOI devices, the self-heating (SH) effect is expected to be significant [166]. Experimental evidence for the presence of SH effects in the investigated UTBB FDSOI transistors has been presented in a recent work [167]. Due to the ultra-thin body, very small channel length and thin-BOX of the fully-depleted device, heat conduction from the channel to the substrate is very quick. Therefore, the rise of the lattice temperature can be assumed to be uniform throughout the channel, and , in turn, linearly related to the power dissipated in the device as [140], [166]:

$$T - T_0 = R_{th} V_{ds} I_{ds} \qquad \textbf{Eq. III.50}$$

where T is the lattice temperature, T_0 is the ambient temperature and R_{th} is the thermal resistance:

$$R_{th} = \frac{1}{2W}\sqrt{\frac{t_{box}}{K_{ox}\,K_{Si}\,t_{Si}}} \qquad \textbf{Eq. III.51}$$

with K_{ox} = *1.4 W/m·K* and K_{Si} = *63 W/m·K* the thermal conductivities of SiO_2 and silicon, respectively. Once the lattice temperature T is obtained, the saturation velocity, the threshold voltage and the mobility have to be recalculated to obtain the drain current at that temperature. For typical temperature rise by 80 K, the saturation velocity $\upsilon_{sat} = 2.4 \times 10^7/(1 + 0.8 \times exp(T/600))$ decreases from 1.03×10^7 cm/s at 300 K to 0.96×10^7 cm/s at 380 K. Thus, υ_{sat} has weak temperature dependence and it can be considered constant in our model. Furthermore, it has been demonstrated that in lightly doped UTBB SOI MOSFETs the effect of temperature on the threshold voltage is negligible [168].

In addition to the mobility reduction due to the vertical gate oxide field as described by Eq. III.44, the carrier mobility is degraded with increasing the temperature by the SH effect due to different scattering mechanisms. Whereas in TCAD simulations the local temperature is considered, in compact modeling the mobility cannot be explicitly derived considering local temperature variations. For compact modeling, taking uniform the lattice temperature throughout the channel of nanoscale UTBB FDSOI devices [140], [166] and considering as is usual a power law for the temperature dependence of the mobility,the effective mobility $\mu_{eff,sh}$ at temperature T is expressed in terms of the effective mobility μ_{eff} at the ambient temperature T_0 as:

$$\mu_{ef,sh} = \mu_{eff}\left(\frac{T_0}{T}\right)^r = \frac{\mu_{eff}}{\left(1+\frac{R_{th}V_{ds}I_{ds}}{T_0}\right)^r} \qquad \textbf{Eq. III.52}$$

where r is a fitting parameter. Note that for typical UTBB SOI devices, the term $R_{th}V_{ds}I_{ds}/T_0$ is of the order of 10^{-2}, which makes possible the first order expansion of the power term in Eq. III.52 as:

$$\mu_{ef,sh} \approx \frac{\mu_{eff}}{1+\frac{rR_{th}V_{ds}I_{ds}}{T_0}} \qquad \textbf{Eq. III.53}$$

In Eq. III.47, substituting μ_{eff} with $\mu_{eff,sh}$ we get a quadratic expression in terms of I_{ds} the solution of which is given by:

$$I_{ds} = \frac{-A_2 + \sqrt{A_2^2 + 4A_1A_0}}{2A_1} \qquad \textbf{Eq. III.54}$$

where:

$$A_0 = \frac{W\mu_{eff}C_{oxf}V_{th}^2}{L_{eff}}\left[(q_s - q_d) + \frac{1}{2\eta_f}\left(q_s^2 - q_d^2\right)\right] \quad \textbf{(a)}$$

$$A_1 = \frac{rR_{th}V_{ds}}{T_0} \quad \textbf{(b)} \qquad \textbf{Eq. III.55}$$

$$A_2 = 1 + \frac{V_{th}\mu_{eff}}{\upsilon_{sat,vo}L_{eff}}(q_s - q_d) \qquad \textbf{(c)}$$

III.4.2 Drain Current Model Validation

The drain current compact model has been verified by comparing the model with experimental results. The devices measured are n-MOS transistors with back-plane, issued from 28 nm FDSOI CMOS technology with channel width $W = 0.5\ \mu m$ and channel length $L = 30$ and $240\ nm$ as described in section II. The parameters of the device under study, extracted from the transfer characteristics measured at $V_{ds} = 30\ mV$ at different back gate voltages using the Y-function method [83], are listed in Table III-1. It is noted that the mobility is close to $93.5\ cm^2/Vs$, while the parameters θ_1 and θ_2 are increased with negative V_b due to stronger surface roughness and phonon scattering mechanisms at the front interface. This is consistent with the finding that the effective carrier mobility is degraded by the proximity with the HfO_2-based front gate dielectric [169].

V_b (V)	μ_0 ($cm^2/V{\cdot}s$)	θ_1 (V^{-1})	θ_2 (V^{-2})
-3	93.0	0.70	0.67
-2	93.5	0.60	0.60
-1	94.0	0.50	0.60
0	93.5	0.40	0.55
1	95.0	0.37	0.50
2	93.5	0.40	0.42
3	93.0	0.40	0.42

Table III-1 Extracted mobility parameters for UTBB FDSOI MOSFET with L = 30 nm.

Figures III-12(a) and (b) present the measured transfer characteristics for $V_{ds} = 0.1$ and $1\ V$, with back bias voltages V_b varying from -3 to +3 V and Figures III-13(a), (b) the output characteristics with parameter the front gate bias V_g and different V_b values. Good agreement between model results and experimental measurements in all operation regimes and for a wide range of back bias is obtained, using fixed values for the parameters: $\varphi_{m,f} = 0.37\ V$ for the front gate, $\varphi_{m,b} = 0.3\ V$ for the back gate, $V_E = 0.5\ V$, $\lambda_w = 100$ and $70\ nm$ for $V_b \leq 0$ and $V_b > 0$, respectively and $r = 0.5$, which is close to the value of $r = 0.6$ found for nanoscale ($L = 22\ nm$) DG MOSFETs [170]. The low value of the temperature exponent r in nanoscale FD-SOI devices has been confirmed from experimental measurements of the electron mobility with temperature [171], [172]. It has been found that the mobility temperature exponent decreases as the gate length is reduced, which is attributed to attenuation of the phonon scattering mechanism with respect to the source/drain process-induced defect scattering mechanism [172].

Figures III-14(a) and (b) show the dependence of the electron mobility on the effective electric field, E_{eff} (Eq. III.56) and the temperature T for different back gate voltages, used to obtain the results of Figures III-12 and III-13, justifying the proposed mobility model.

$$E_{eff} = \frac{qN_A t_{Si}}{\varepsilon_{Si}} + \frac{C_{oxf}(V_g - V_{tf})}{2\varepsilon_{Si}} \qquad \textbf{Eq. III.56}$$

In order to check further the accuracy of the model, the small-signal parameters of transconductance g_m and output conductance g_{ds} have been examined. Figures III-12(c), (d) and Figures III-13(c), (d) show the plots of g_m versus V_g and g_{ds} versus V_{ds}, respectively,

derived from the experimental data of Figures III-12(a), (b) and Figures III-13(a), (b). The agreement between the experimental and modeled results is very good for back gate bias varying in the range of -3 to +3 V, supporting the good accuracy of the compact model.

As shown in Figure III-15, for two typical back gate voltages V_b, the drain is significantly underestimated without taking into account both the VO and SH effects or overestimated without considering the SH effect. These results indicate the necessity to include both SH and VO effects for good model accuracy.

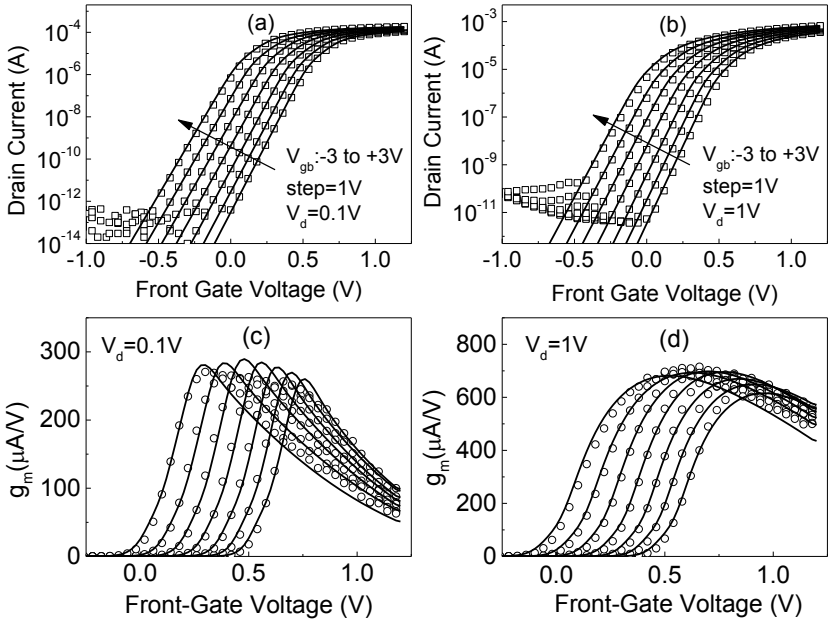


Figure III-12 Experimental (symbols) and modeled (solid lines) transfer (a), (b) and transconductance (c), (d) characteristics of silicon UTBB FDSOI MOSFET with W = 0.5 µm, L = 0.03 µm, t_{Si} = 7 nm and t_{ox} = 1.55 nm, measured at drain voltage 0.1 and 1 V and different back gate voltages $V_{gb} = V_b$.

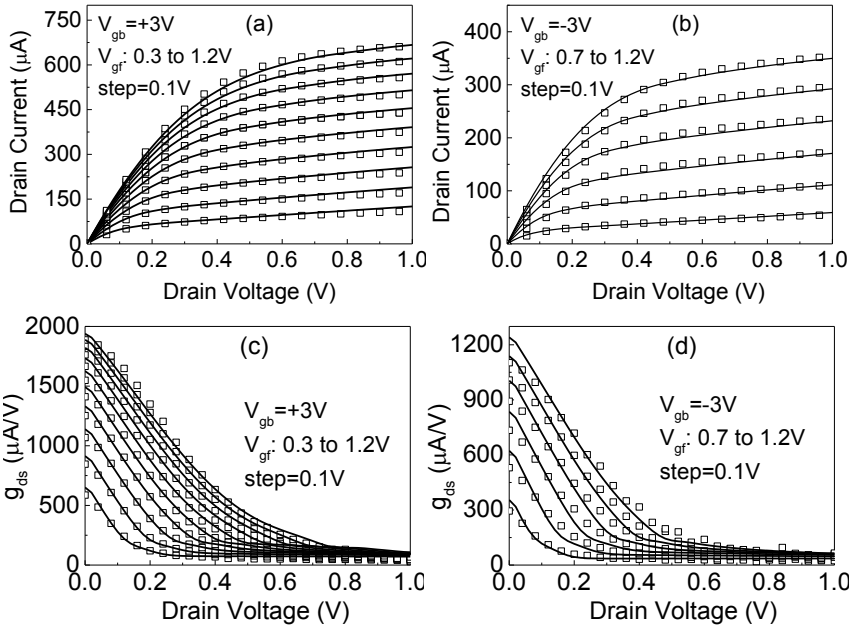


Figure III-13 Experimental (symbols) and modeled (solid lines) output characteristics (a), (b) and output conductance (c), (d) of silicon UTBB FDSOI MOSFET with W = 0.5 µm, L = 0.03 µm, t_{Si} = 7 nm and t_{ox} = 1.55 nm, measured at back gate voltages $V_{gb} = V_b$ = +3 and -3 V.

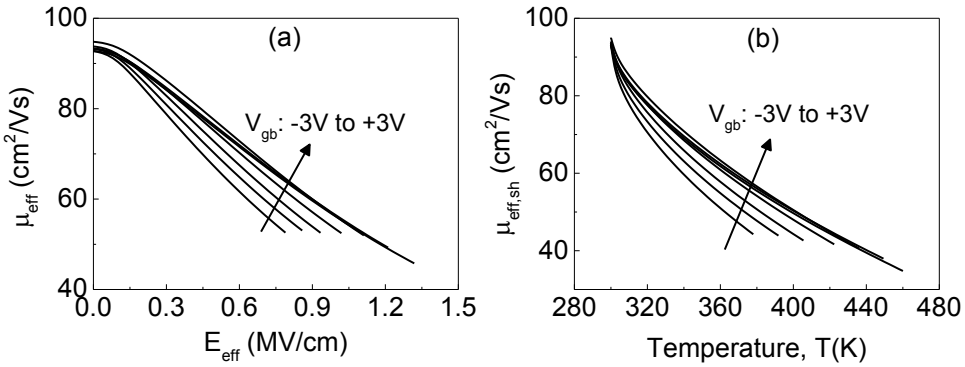


Figure III-14 Dependence of the electron mobility on the effective electric field E_{eff} (a) and the temperature T due to the SH effect (b) used to reproduce the transfer and output characteristics of Figures III-12 and III-13.

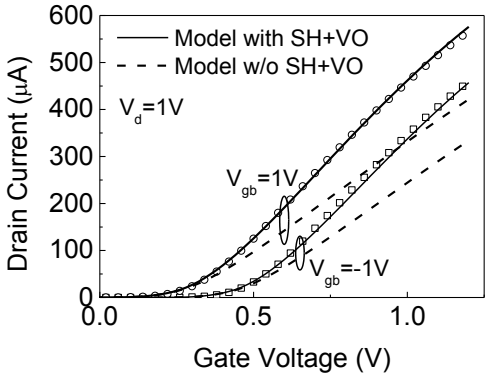


Figure III-15 Experimental (symbols) and modeled (solid lines) transfer characteristics in linear representation of silicon UTBB FDSOI MOSFET with W = 0.5 µm, L = 0.03 µm, t_{Si} = 7 nm and t_{ox} = 1.55 nm, measured at drain voltage 1V and different back gate voltages $V_{gb} = V_b$ with considering the SH and VO effects (solid lines), without considering the SH and VO effects (dash lines) and without considering the SH effect (dash-dot lines).

The model has been evaluated also for the device with larger gate length (*L = 240 nm*). Comparison between model and experimental I_{ds}-V_g and I_{ds}-V_{ds} characteristics are shown in Figure III-16 for the typical values of V_b = *-2, 0* and *+2 V*, which demonstrate good model accuracy. The model parameters are the same as for *L = 30 nm*, except for $\varphi_{m,f}$ = *0.27 V*. The lower value of $\varphi_{m,f}$ in the long-channel device can be attributed either to the process-induced traps near the source/drain regions or to the work function variability of TiN caused by the different grain-orientation, the effect of which becomes more pronounced in the short-channel device. The extracted mobility parameters are reported in Table III-2.

V_b (V)	μ_0 (cm^2/V·s)	θ_1 (V^{-1})	θ_2 (V^{-2})
-2	193	-0.20	0.65
0	200	-0.30	0.55
2	225	-0.05	0.3

Table III-2 Extracted mobility parameters for UTBB FDSOI MOSFET with L = 240 nm.

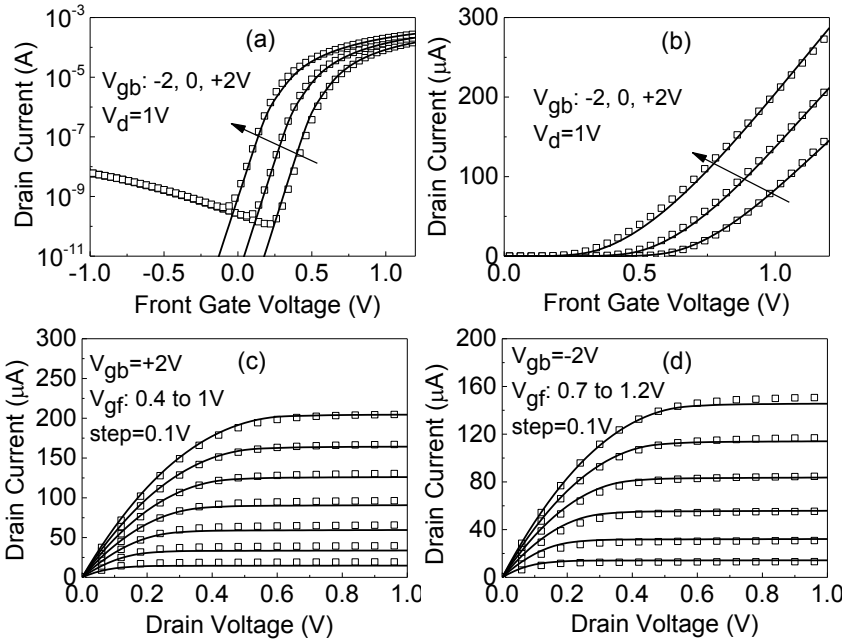


Figure III-16 Experimental (symbols) and modeled (solid lines) transfer characteristics (a)-(b) and output characteristics (c)-(d) of the UTBB FDSOI MOSFET with L = 240 µm, measured at different back gate voltages $V_{gb} = V_b$.

III.5 Drain Current Modeling for Electronic Circuit Simulations

Verilog-A Hardware Description Language (HDL) defines a behavioral language for analog systems used by Cadence Spectre circuit simulator. It is a very powerful and useful tool, since it provides the potential for full description of a circuit netlist, as well as the behavior of a single device and its interface connections. Over the last few years, Verilog-A has been adopted by leading compact model developers. Indeed, when the current-voltage characteristics are described by analytical and compact mathematical equations valid in all regions of operation, these equations can be written in the Verilog-A code and implement an analytical model.

III.5.1 Verilog-A Drain Current Model Development

The Verilog-A implementation of the drain current is based on the model described in this Chapter. The Verilog-A code implementing this model was developed successfully for $V_b=0V$ and is presented in detail in Appendix A. In this section only some basic elements of the code will be described.

The code begins with the "//" characters, which constitute a comment, in order for the code to be easier to be understood. Then the next two lines follow:

```
`include "constants.vams"
`include "disciplines.vams"
```

where "**include**" specifies the Verilog-A libraries that are used in the code that follows. The lines that begin with "**module**" and "**endmodule**" specify the behavior of the module. The part of the code that describes the analog behavior of the module is between the lines that

begin with "**analog begin**" and "**end**" and is called the analog block. Outside the analog block but within the module, terminals, variables and parameters are declared. Just before the analog block begins, the following two lines have been written:

```
inout b, d, s, g;
electrical b, d, s, g;
```

which describe the direction and the type of the ports. The FDSOI MOSFET is a four terminal device, and this is why the ports b, d, s, g are necessary. Furthermore, the direction "**inout**" means that these ports can sense and affect the signals that they are connected to. Finally, the last line before the analog block ends, namely:

```
I(d,s) <+ (-A2+sqrt(pow(A2,2)+4*A1*A0))/(2*A1);
```

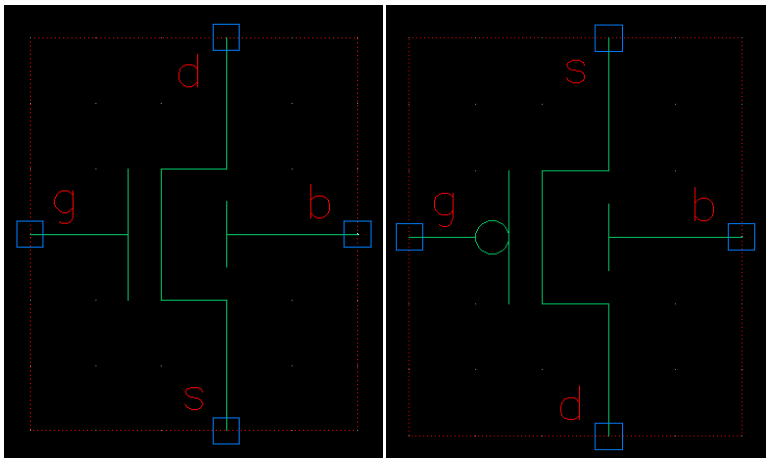
constitutes a contribution statement. This kind of statements take the form of a branch signal on the left side of the contribution operator "<+" followed by an expression on the right side in order to describe continuous time behavior [173].

Concerning the Verilog-A code describing the FDSOI p-MOSFET, note that the only differences with the code presented in Appendix A are the declaration of the voltage across the ports and the lower low-field mobility:

n-MOSFET	p-MOSFET
(g, s)	(s, g)
(d, s)	(s, d)
(b, s)	(s, b)
μ_0	$\mu_0 \cdot 3/8$

Table III-3 Differences between the n- and p-MOSFET declaration in Verilog A.

After the codes have been developed, the symbols for the n- and p-MOSFETs (Figures III-17(a) and (b) respectively) were created.

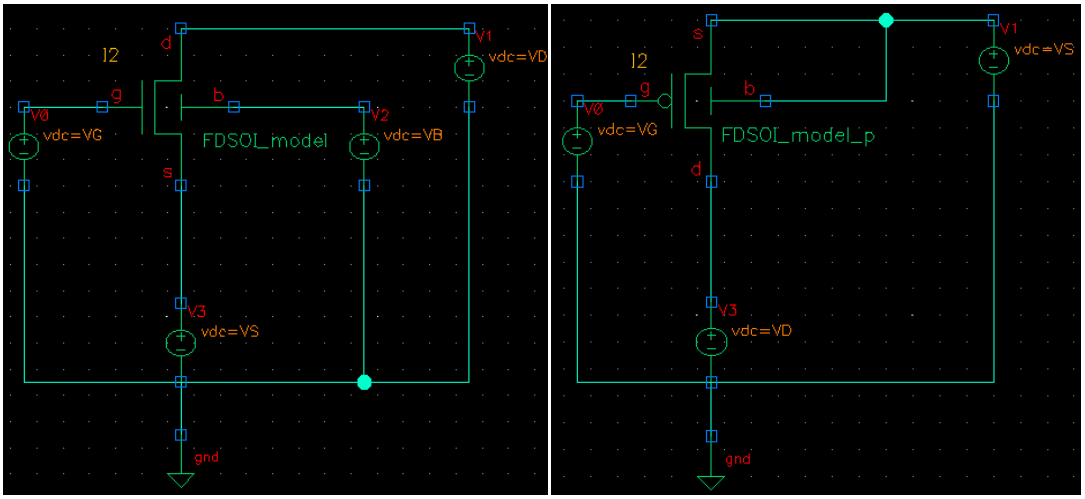


(a) **(b)**

Figure III-17 n-FDSOI (a) and p-FDSOI (b) symbols created in Verilog-A.

III.5.2 FDSOI Single Device

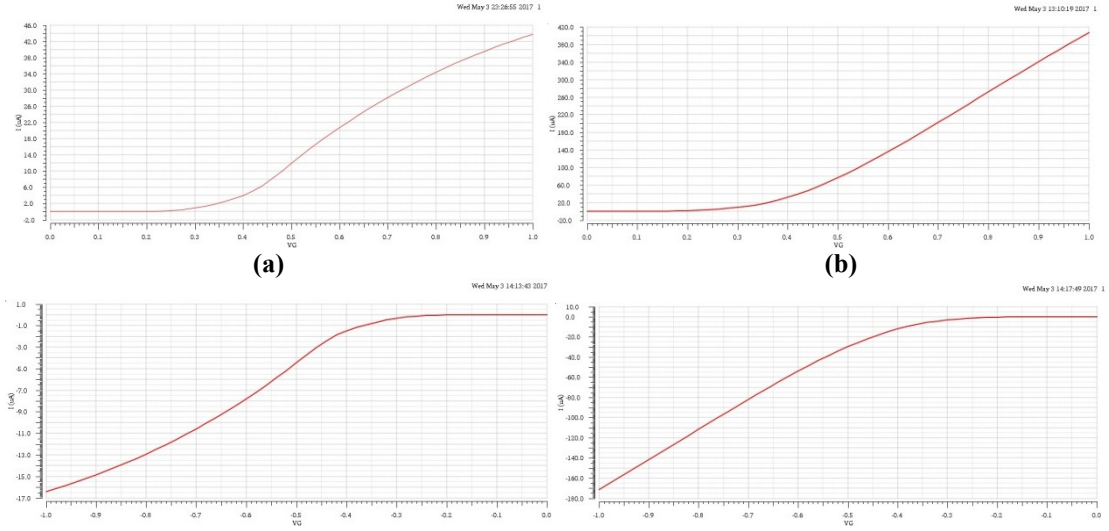
The successful simulation of a single device in Verilog-A is prerequisite for the development of circuit simulation tools. In order to verify the correct behavior of the devices, the simple circuits illustrated in Figure III-18 were developed.



(a) **(b)**

Figure III-18 Schematic for single device behavior verification: n-FDSOI (a) and p-FDSOI (b).

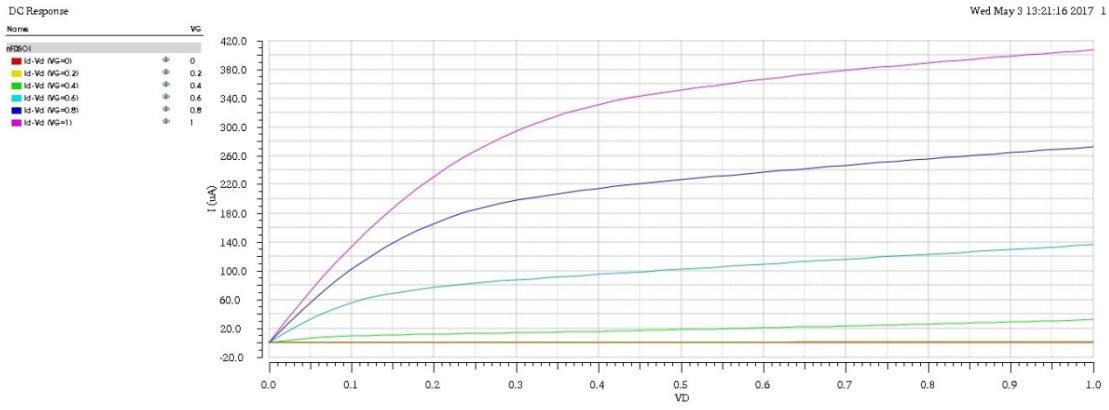
Both the input and the output characteristics were simulated in both cases using the parameters described in Sections III.3 and III.4. Indeed, the expected behavior of the devices was verified as indicated in Figures III-19 and III-20.



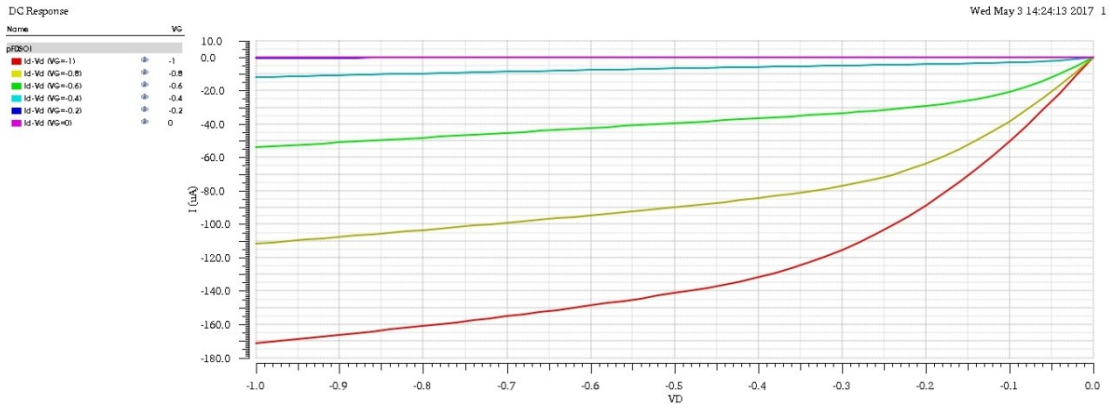
(a) **(b)**

(c) **(d)**

Figure III-19 Simulated transfer characteristics in linear ($|V_d|$=30mV) (a)-(c) and saturation ($|V_d|$=1V) (b)-(d) regions for n-FDSOI (a)-(b) and p-FDSOI (c)-(d) devices with L=0.03µm and W=0.5µm.



(a)



(b)

Figure III-20 Simulated drain current as a function of drain voltage for the n-FDSOI and p-FDSOI devices with L=0.03µm and W=0.5µm developed in Verilog-A.

Additionally, to further verify that there were not any mistakes in the Verilog-A code, it has been compared with the one written in Mathcad software. As seen in Figure III-21, both implementations fully agree.

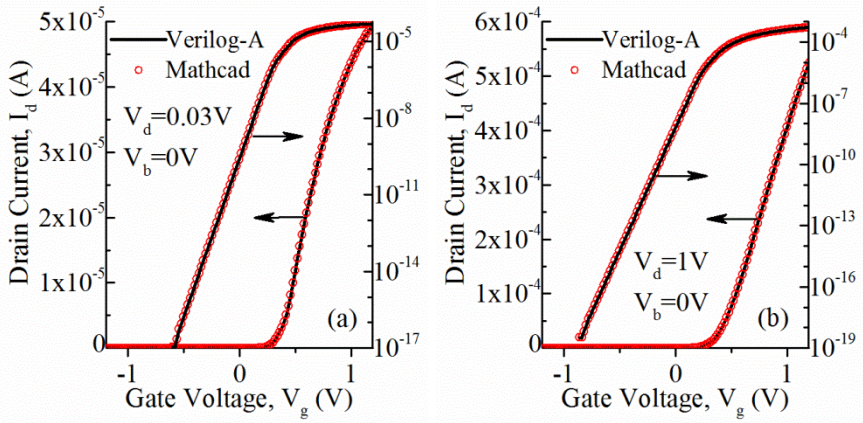


Figure III-21 Comparison between model transfer characteristics implemented in Mathcad and Verilog-A in linear (a) and saturation (b) regions of operation for an n-FDSOI MOSFET with L=0.03µm and W=0.5µm.

III.5.3 FDSOI CMOS SRAM cell

One of the most useful and simple circuits to perform simulation tests on is the CMOS inverter, due to the fact that it consists of only two transistors, one n-MOS and one p-MOS. The typical CMOS inverter schematic is illustrated in Figure III-22.

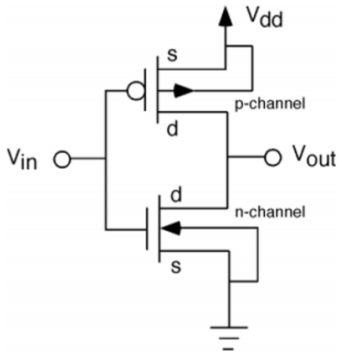


Figure III-22 Typical CMOS inverter schematic.

The core cell of another fundamental circuit, the Static Random Access Memory (SRAM) Cell is formed by two CMOS inverters, where the output potential of each inverter, V_{out} is fed as input into the other, V_{in}. SRAMs can retain their stored information as long as power is supplied. Nowadays the study of the SRAM cell is of high interest since modern SRAMs strive to increase bit counts while maintaining low power consumption and high performance. The 6 Transistor (6T) SRAM cell has been designed to Virtuoso Schematic Editor, as seen in the following Figure.

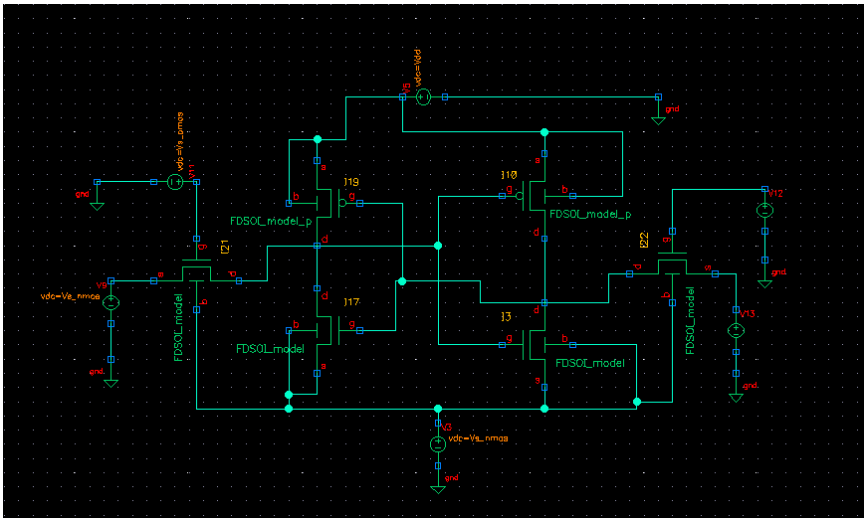


Figure III-23 6T SRAM cell in Virtuoso Schematic Editor.

The analytical drain current model for each device described in Sections III.5.1 and III.5.2 was used of the circuit for the 6T SRAM cell using n-FDSOI MOSFETs with W_n=0.5 μm, while p-FDSOI MOSFETs with $W_p=(8/3)\cdot W_n$, since the low-field mobility ratio between the n- and p-MOSFET was found : $\mu_{0,p}/\mu_{0,n}=3/8$. The channel length was equal to 30 nm for all the transistors. In fact, perfect symmetry and matching between the two devices was considered in all simulations. In Figure III-24 the so-called SRAM "butterfly" curve is depicted.

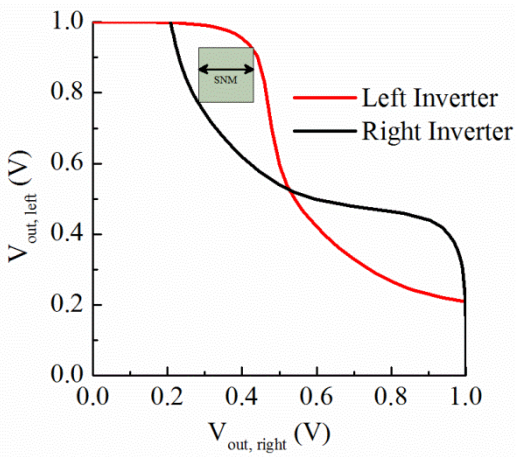


Figure III-24 The SRAM "butterfly" curve: V_{out} of the left inverter as a function of V_{out} of the right one. The window in the "butterfly" curve illustrates the SNM.

A significant quantity that characterizes the SRAM cell's stability is the so-called Static Noise Margin (SNM). Noise Margin (NM) is defined as the maximum spurious signal that can be accepted by the device when used in as system while still maintaining is correct operation. Assuming that the noise is present long enough for the circuit to react, then it is dc

noise or static [174]. This is where the term SNM has arisen from. This quantity can be extracted by nesting the largest possible square in the two Voltage Transfer Curves (VTC) of the involved CMOS inverters, as seen in Figure III-24. Indeed, it is defined as the side-length of this square and is given in volts.

III.6 Summary

Based on the minimum values of the front and back surface potentials of lightly doped UTBB FDSOI MOSFETs, simple analytical models for the front and back gate threshold voltages and ideality factors have been derived in terms of the device geometry parameters and the applied bias voltages with back gate control. The model results were found to be in very good agreement with both numerically simulated and experimental results for devices with channel length down to 17 nm. Thus, the present models for estimating the front and back gate threshold voltages and ideality factors can be used for drain current compact modeling of lightly doped short channel UTBB FDSOI MOSFETs.

An analytical compact drain current model was developed for lightly doped short-channel UTBB FD-SOI MOSFETs with back gate control, accounting for small geometry, saturation velocity, mobility degradation, quantum mechanical, velocity overshoot and self-heating effects. Summarizing, in addition to the mobility parameters (μ_o, θ_1, θ_2) and threshold voltage parameters ($\Delta\phi_f$, A_c, B_c) extracted from experimental data, a limited number of fitting parameters (V_E, λ_w, r) is needed in the proposed drain current compact model. Using these parameters, the transfer and output characteristics of UTBB FDSOI MOSFETs can be predicted with good accuracy for a wide range of back gate bias covering the inversion, depletion and accumulation operation regimes. The good level of accuracy makes the compact model suitable for implementation in circuit simulation tools.

IV Reliability Issues in FDSOI Devices

IV.1 Introduction

As has been already mentioned in Chapter I, UTBB FDSOI MOSFETs have attracted much attention in sub-28 nm CMOS generations due to their high immunity to SCEs [175], [176] and the threshold voltage controllability with back gate bias instead of using different channel doping concentrations, thus avoiding variability due to random dopant fluctuations [177]. However, at small channel dimensions, the electric fields are high resulting in hot-carrier degradation issues. Therefore, identification of the HC-induced traps is a very important topic in short-channel FDSOI transistors.

HC studies in UTBB FDSOI MOSFETs are limited to few works referred on investigation of the degradation mechanism by studying the evolution with stress time of the device parameters [178], [179], [180], [181] and on HC degradation modelling limited in the saturation region [182]. The LFN technique has been proposed as a non-destructive diagnostic tool to evaluate traps located within the gate dielectric, at the gate dielectric/silicon interface and within the depleted silicon film [183], [184]. Recently, the LFN technique has been used in as-fabricated UTBB FDSOI MOSFETs to characterize the processing-induced interface traps at both front and back gate dielectric/silicon interfaces and bulk traps located within the silicon film next to the source and drain contacts [185]. The measured LFN spectra are composed of 1/f and Lorentzian-type noise components. As has been already analyzed in Chapter II the Lorentzian-type noise can be due either to the G-R noise resulting from a number of traps with discrete energy levels or to the RTS noise attributed to a single trapping level within the gate dielectric. The superposition of many Lorentzians leads to 1/f type noise spectra. Recently, the origin of the 1/f and g-r noise components in as-fabricated UTBB FDSOI n-MOSFETs has been investigated in detail by LFN measurements in the frequency domain [185], [186].

In this chapter, first, we investigate the impact of HC-stress on nanoscale UTBB FDSOI n-MOSFETs with thin gate dielectric by combined LFN measurements in the frequency and time domain. Based on these measurements, a thorough study of the gate dielectric traps, g-r traps in the silicon film and RTN traps located at the gate dielectric/silicon interface is performed. The results indicate that the RTN time constants are uncorrelated to the RTN amplitude, i.e. the impact of the trap depth from the interface on the RTN amplitude is masked by that of the trap location over the channel. In previous work, the RTN amplitude for a single trap has been modelled considering the carrier number fluctuation model [113], [187], [188], [189]. In this work, the RTN amplitude is formulated with an analytical expression including parameters related to both carrier number and mobility fluctuations and to the statistical variability of the trap location over the channel. These model parameters can be extracted from experimental data of the RTN relative amplitude, enabling to predict the RTN amplitude from the subthreshold to the above threshold regions.

Second, using the static current-voltage characteristics measurements and based on our analytical compact model for nano-scale FDSOI MOSFETs [190], an HC degradation model is developed using the threshold voltage shift, the ideality factor shift and the mobility degradation with stress time, predicting the device performance under different bias conditions.

Finally, an analytical study of the negative bias temperature instability (NBTI) in nano-scale FDSOI MOSFETs is presented. NBTI has not been investigated extensively in FDSOI UTBB devices [178], [180], [191] although it has been recognized as a major reliability issue in recent bulk p-MOSFETs [192]. The NBTI is prominent in p-MOS devices along the entire channel when negative gate-to-source voltage is applied, while as is apparent from the above, the hot-carrier effect is prominent in n-MOS devices which occurs near the drain end due to hot carriers accelerated in the channel. In this work, the NBTI behavior of nano-scale UTBB FDSOI MOSFETs with zero back gate bias and small drain bias voltage has been characterized and modelled. In particular, models predicting the temperature and gate voltage dependence of the threshold voltage shift during the NBTI stress and recovery phases of FDSOI transistors are presented.

IV.2 Hot Carrier Injection (HCI) in FDSOI n-MOS

IV.2.1 Experimental Details

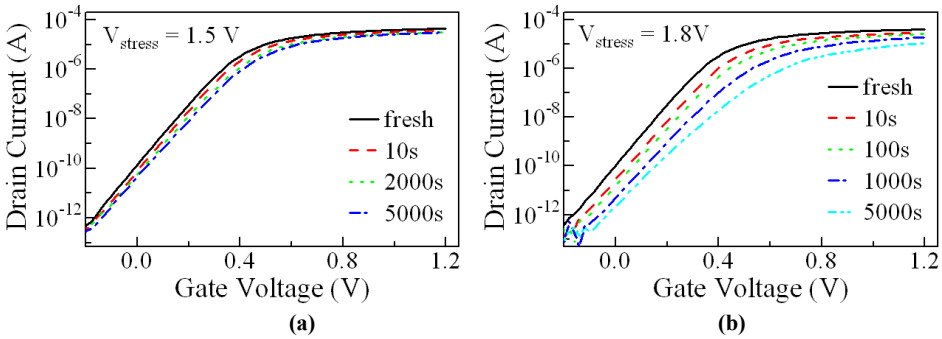
The HC experiments were performed on FDSOI n-MOSFETs with channel width $W = 0.5\ \mu m$ and channel length L ranging from 30 to 100 nm, fabricated by ST Microelectronics in France [157]. The front gate stack consists of TiN/HfO_2-based dielectric with equivalent oxide thickness 1.55 nm, the BOX thickness is 25 nm and the silicon film thickness is 7 nm.

In the HC experiments, the devices were stressed at room temperature by applying stress voltage to the drain and gate electrodes, with the source terminal grounded and back gate bias $V_b = 0\ V$. In short-channel devices, it has been confirmed that the worst HC stress condition occurs at $V_{dstress} = V_{gstress}$ [193]. The stress was interrupted at selected stress times to measure the transfer characteristics in the front-gate mode using an Agilent B1500 Semiconductor Device Analyzer. LFN measurements were performed before and after stress using either the 3PNMS Noisys system or the Agilent B1530 WGFMU module with an FFT applied on the time domain data in order to obtain the corresponding spectra. It is mentioned that the measurements before and after stress were performed on the same devices.

IV.2.2 Hot Carrier Degradation Mechanisms in Nano-scale FDSOI MOSFETs

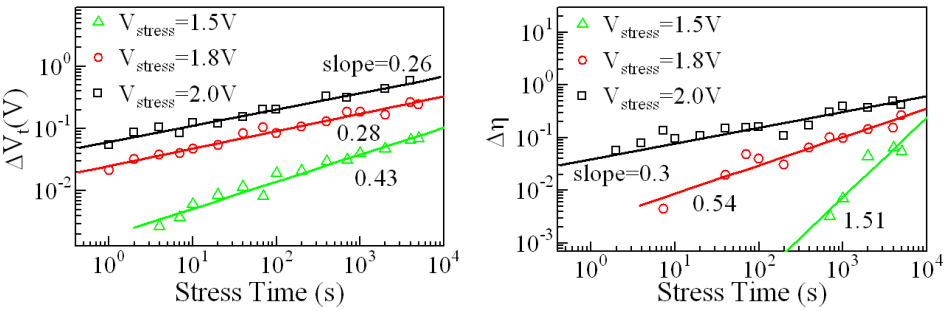
Figure IV-1 shows two examples of the I_{ds}-V_{gs} characteristics measured at $V_d = 0.03\ V$ of fresh and stressed devices at $V_{stress} = 1.5$ and $1.8\ V$ for different stress times. Degradation of the threshold voltage V_t, subthreshold swing coefficient η and on-state current is observed.

The positive threshold voltage shift ΔV_t that is observed, follows a time dependent power-law with exponent n close to 0.5 at $V_{stress} = 1.5\ V$ showing that the interface degradation is the dominant mechanism, whereas at higher stress voltages n is close to 0.26 indicating that electron trapping into the gate dielectric defects becomes the dominant mechanism (Figure IV-2(a)) [194]. This finding is in accordance with the time exponent n for degradation of η varying from 1.51 to 0.3 as V_{stress} increases from 1.5 to 2 V (Figure IV-2(b)). However, the increase of ΔV_t with stress time is faster compared to $\Delta\eta$ at high stress voltages as shown in Figure IV-3, suggesting the dominance of the electron trapping degradation mechanism.



(a) (b)

Figure IV-1 I_{ds}-V_{gs} transfer characteristics before and after stress at V_{stress} = 1.5 V (a) and V_{stress} = 1.8 V (b).



(a) (b)

Figure IV-2 Threshold voltage (a) and subthreshold swing coefficient (b) shift with stress time at different stress conditions.

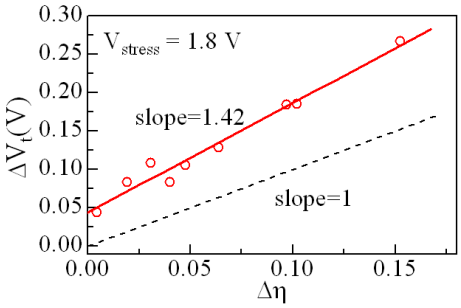


Figure IV-3 Correlation between ΔV_t and $\Delta\eta$ after stress at V_{stress} = 1.8 V.

Figures IV-4(a) and (b) show the noise spectra before and after stressing at $V_{stress} = 2$ V for 5000 s. The spectra show the co-existence of two noise components: $1/f^{\gamma}$ and Lorentzian-like.

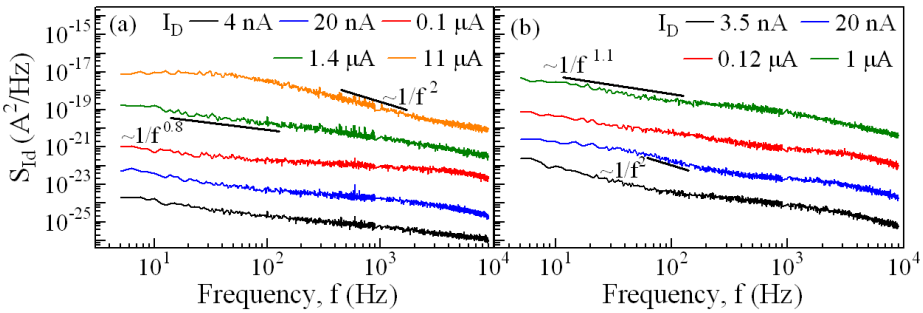


Figure IV-4 Drain current noise spectra before (a) and after (b) stress (V_{stress} = 2 V for 5000 sec) for different values of current.

In order to investigate in depth the effect of the HC stress on FDSOI n-MOSFETs, short-time and long-time HC stress were performed. The first case is referred to 100 sec stress time, while the second one to 5000 sec stress time. Furthermore, time domain drain current measurements were necessary so that the noise components are clarified.

IV.2.2.1 Short-Time Hot Carrier Stress

Figure IV-5 shows the degradation of the transconductance g_m for a typical fresh FD-SOI n-MOSFET with threshold voltage $V_t = 0.33\ V$, measured at drain voltage $V_{ds} = 0.03\ V$, after HC stress at $V_{dstress} = V_{gstress} = 1.5\ V$ for short-time causing a positive threshold voltage shift by about 10%. The maximum g_m degradation and the simultaneous parallel g_m shift indicate interface degradation and charge trapping into the gate dielectric defects [194].

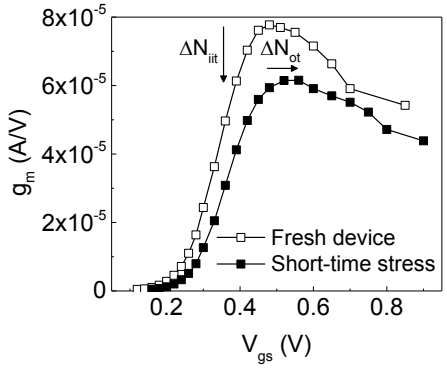


Figure IV-5 Transconductance (g_m) of UTBB FDSOI n-MOSFET, measured at V_{ds}=0.03V before and after short-time HC stress.

In order to clarify the degradation mechanisms, the HC-induced interface and gate dielectric traps were studied with LFN measurements. Figure IV-6 shows typical plots of $S_{Id} \times f$ versus f, where S_{Id} is the drain current noise spectral density and f is the frequency, measured at drain voltage $V_{ds} = 0.03\ V$ and different gate voltages V_{gs} in UTBB FDSOI MOSFET after short-time stress. The general expression for the LFN spectrum can be represented as a synthesis of a flicker and Lorentzian noise components as [195]:

$$S_{I_d} = \frac{K_f}{f} + \sum_{i=0}^{N} \frac{A_i}{1+\left(\frac{f}{f_{ci}}\right)^2} \qquad \textbf{Eq. IV.1}$$

where K_f is a coefficient characterizing the intensity of the *1/f* noise and the second term represents a sum of the Lorentzian components with A_i the plateau value and f_{ci} the corner frequency of the traps. A least-square fit to the experimental $S_{Id} \times f$ versus f data allow us to distinguish the contributions of the flicker and Lorentzian components. Time-domain measurements can be implemented to identify the origin of the Lorentzian noise, i.e. whether it is G-R noise or RTN. In the case of RTN due to a single trap, the histogram of instantaneous drain current values derived from the time domain signal has a two-level RTN distribution [196].

Figure IV-7 shows the normalized flicker noise component $S_{1/f} / I_{ds}^2$ versus drain current I_{ds} of a device before and after short-time stress, measured at frequency $f = 10\ Hz$. Recently, in both n- and p-channel UTBB FDSOI MOSFETs with thin gate dielectric, it has been demonstrated that the 1/f noise amplitude can be described by the conventional CNF/CMF model considering contribution from both interfaces [185]. This finding indicates

that the trap time constants are uncorrelated to the noise amplitude in MOSFETs with thin gate dielectrics, otherwise we would not be able to observe very good correlation to the CNF/CMF model when a large number of traps is averaged.

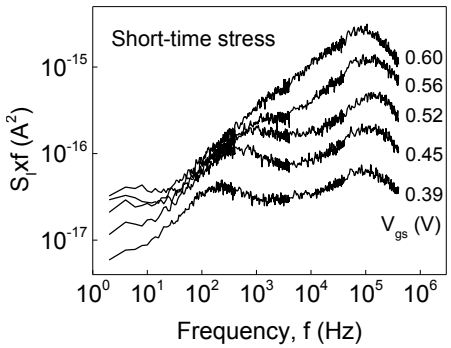


Figure IV-6 Normalized LFN spectra of short-time HC stressed UTBB FDSOI n-MOSFET at different gate voltages, showing the presence of a flicker and Lorenzian noise components.

According to the generic CNF/CMF model (Eq. II.46) which is valid in all regions of operation, the analytical compact model for $S_{I/f}$ is described by the single equation [197]:

$$\frac{S_{1/f}}{I_{ds}^2} = \left(\frac{g_m}{I_{ds}}\right)^2 \left(1 + \Omega \frac{I_{ds}}{g_m}\right)^2 S_{Vfb} \qquad \textbf{Eq. IV.2}$$

where the flat-band voltage power spectral density, given by Eq. II.47, for $\lambda = 1\text{Å}$ and $\gamma = 1$ becomes:

$$S_{Vfb} = \frac{q^2 kTN_{ot}}{fWLC_{ox}^2} \qquad \textbf{Eq. IV.3}$$

where it is reminded that N_{ot} is the areal density of the gate dielectric traps with continuous energy distribution located close to the gate dielectric/silicon interface, q the elementary charge, kT the thermal energy and C_{ox} the gate dielectric capacitance per unit area. In Eq. IV.2, Ω is called the noise parameter related to the Coulomb scattering coefficient α_{sc}, as deduced from Eq. II.46. Because the device is biased in the front-gate mode, it has been demonstrated that the contribution of the back gate interface to the noise parameters Ω and S_{Vfb} can be considered as negligible [185]. Furthermore, using a technique based on capacitance measurements, it has been shown that in FDSOI MOSFETs, only the front gate interface is degraded during a classical HC stress [179]. The plots of $S_{1/f} / I_{ds}^2$ versus I_{ds} in Figure IV-7 follow the model described by Eq. IV.2, suggesting that the 1/f noise can be described by the CNF/CMF model. From the extracted value of S_{Vfb}, the areal gate dielectric trap density is $N_{ot} = 1.6 \times 10^{10}\ cm^{-2}\ eV^{-1}$ for the fresh device and $N_{ot} = 2 \times 10^{10}\ cm^{-2}\ eV^{-1}$ for the short-time stressed device explaining the parallel g_m shift in Figure IV-5.

The Lorentzian noise components can originate from traps with discrete energy level located within the gate dielectric close to the gate dielectric/silicon interface or within the silicon film [198]. To identify the origin of the Lorentzian noise, the corner frequency f_c and the plateau amplitude A_i of the obtained Lorentzian components are presented in Figures IV-8(a) and (b), respectively. Two G-R traps are detected with corner frequencies dependent of V_{gs} and plateau values exhibiting maximum at V_{gs} where the corner frequency starts increasing. These specific variations of the corner frequencies and the plateau values indicate

that the G-R noise originates from traps located within the channel [186]. The results of Figure IV-8(b) show attenuation of g-r traps after short-time HC stress.

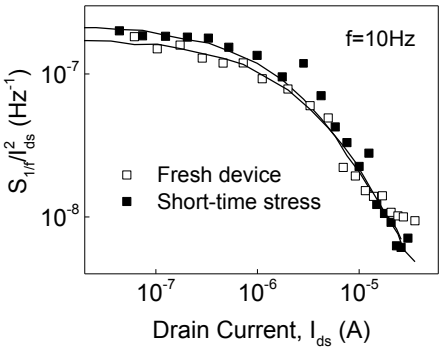


Figure IV-7 Normalized measured drain current power spectral density $S_{1/f}/ I_{ds}^2$ versus drain current I_{ds} of the fresh and short time stressed UTBB FDSOI MOSFETs. The symbols correspond to experimental data and the lines to noise model (Eq. IV.2) with $\Omega = 4\ V^{-1}$ and $N_t = 1.6 \cdot 10^{10}\ cm^{-2}eV^{-1}$ for the fresh device and $\Omega = 4\ V^{-1}$ and $N_t = 2 \cdot 10^{10}\ cm^{-2}\ eV^{-1}$ for the stressed device.

Similar behavior regarding the g-r traps attenuation has been observed systematically for other devices subjected to similar short-time HC stress. To understand the reason for attenuation of the silicon g-r traps after short-time HC stress, we consider the interface degradation model of Si-H bond breaking under HC stress [199]. The Si-H bonds are dissociated releasing hydrogen, which annihilate at the initial stages of stress the silicon g-r traps.

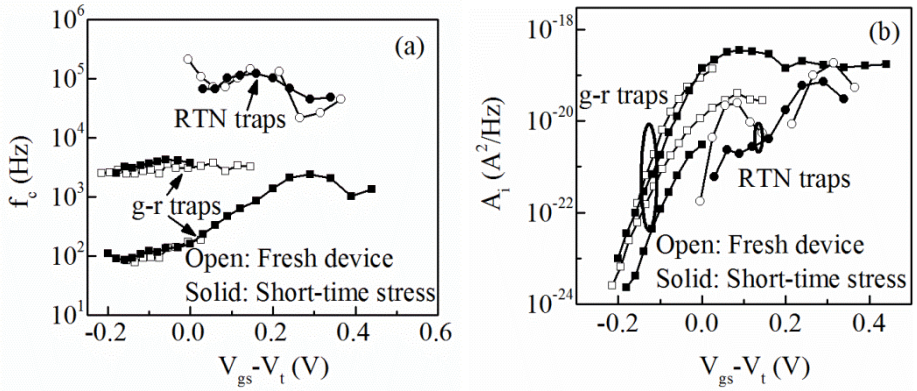


Figure IV-8 Dependence of (a) corner frequency f_c and (b) plateau amplitude A_i for the G-R noise components of fresh and short-time stressed FDSOI nMOSFETs.

In Figure IV-8, the Lorentzian noise observed in the above threshold region of the fresh device ($I_{ds} > 1\ \mu A$) corresponds to RTN, which is confirmed by the behavior of the drain current in the time domain and the histogram of instantaneous drain current values as shown in Figures IV-9(a) and (b), respectively. The RTN data were obtained with sampling frequencies $f_s = 2\ kHz,\ 20\ kHz,\ 200\ kHz$ and $2\ MHz$ and 10^5 points for each sampling, allowing us to detect all possible RTN pulses with widths between $1\ \mu s$ and $100\ s$. In Figure IV-9(a), the dashed-line shows an example of the pulse fit, obtained with threshold-detecting algorithm developed to determine the distribution of the emission and capture time constants. For each gate voltage bias, we extracted the average time constants $<\tau_e>$ and $<\tau_c>$ by fitting the distributions of τ_c and τ_e to the exponential distribution $A \times exp(-t/<\tau>)$ as shown in Figure IV-10, assuming the phenomenon follows the Poisson process [200], [201]. We note that the RTN amplitude is decreased after short-time HC stress, following a behavior similar to that of the silicon G-R traps [Figure IV-8(b)].

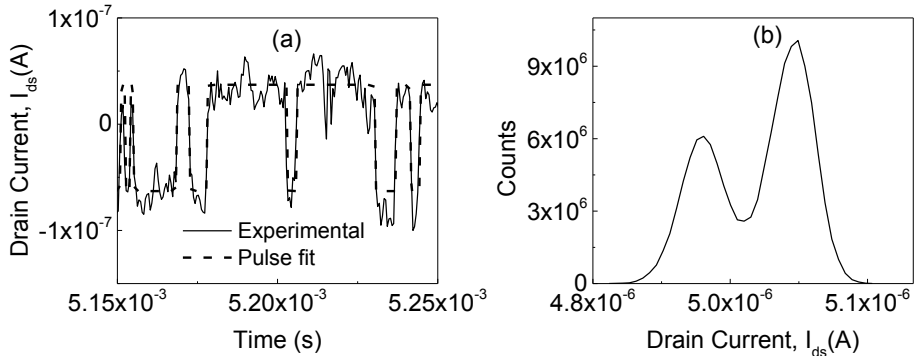


Figure IV-9 Typical one trap RTN waveform of fresh FDSOI nMOSFET and the (b) corresponding histogram of amplitude. The measurement was performed at drain current I_{ds} = 4.9 µA with a sampling frequency of f_s = 2 MHz.

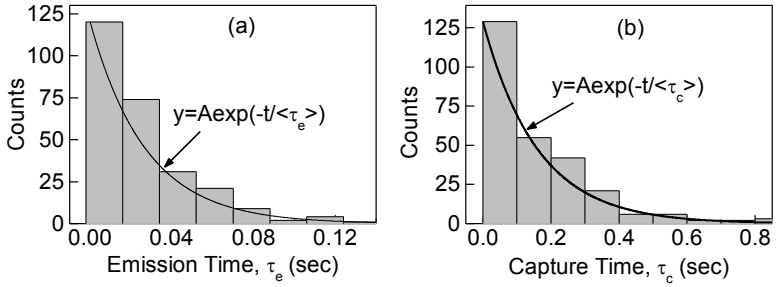


Figure IV-10 Extraction of the average time constants: (a) <τ_e> and (b) <τ_c> from RTN waveform data for a given sampling frequency and gate bias voltage.

Figure IV-11 presents the extracted values of τ_c and τ_e as a function of the gate voltage for the fresh device. Although the RTN trap is characterized over a relatively small V_{gs} range ($\sim 0.1\ V$), a curvature appears in the plot of the time constant τ_c, whereas the emission time increases symmetrically to the decrease of τ_c. This finding indicates that the single trap responsible for the observed RTN should be a metastable defect [202], [203], [204]. Metastable traps have been observed also in 45 nm CMOS bulk transistors [205]. Based on advanced non-radiative multiphonon (NMP) theory developed recently in [202], [203], [204], the introduction of a metastable defect with intermediate state yields a curvature in τ_c, explaining the data over a wide range of gate voltage and temperature. In Figure IV-8, the Lorentzian noise observed in the above threshold region of the fresh device ($I_{ds} > 1\ \mu A$) corresponds to RTN, which is confirmed by the behavior of the drain current in depth and the RTN amplitude could be uncorrelated to the time constants τ_c and τ_e [200], [206], [207].

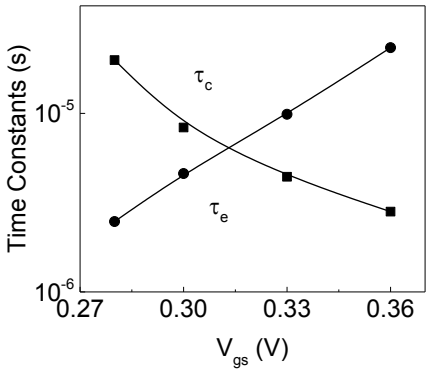


Figure IV-11 Dependence of the extracted time constants τ_c and τ_e on the gate voltage V_{gs} of the fresh device.

In addition, in nanoscale MOS devices with thin gate dielectric, the gate bias dependence of the ratio τ_c/τ_e strongly depends on the trap position over the channel in both subthreshold and above-threshold regimes [207]. Since the trap position over the channel is unknown variable in experimental devices, the possibility to extract the trap position within the gate dielectric from fluctuation of the RTN amplitude is limited.

IV.2.2.2 Long-Time Hot Carrier Stress

Figure IV-12 shows the degradation of g_m for a typical fresh FDSOI n-MOSFET with threshold voltage $V_t = 0.38\ V$, measured at drain voltage $V_{ds} = 0.03\ V$, after HC stress at $V_{dstress} = V_{gstress} = 1.5\ V$ for long-time causing a positive threshold voltage shift by about 20%. The maximum g_m is degraded with a simultaneous parallel shift, as in the case of short-time stress. The plots of S_{Id} / I_{ds}^2 versus I_{ds} of the fresh and long-time stressed device, measured at frequency $f = 10\ Hz$, are presented in Figure IV-13(a). The extracted data of the 1/f noise component show that the 1/f noise is described by the CNF/CMF model [Figure IV-13(b)]. From the extracted values of S_{Vfb}, the average gate dielectric trap density N_t determined for the long-time stressed device is $N_{ot} = 2.7 \times 10^{10}\ cm^{-2}\ eV^{-1}$, which is higher by a factor of ~2.2 compared to that of the fresh device.

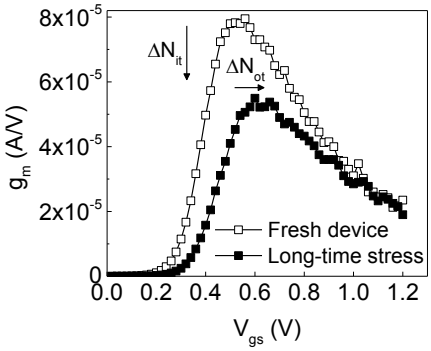


Figure IV-12 Transconductance (g_m) of the FDSOI nMOSFET, measured at V_{ds} = 0.03 V before and after long time stress.

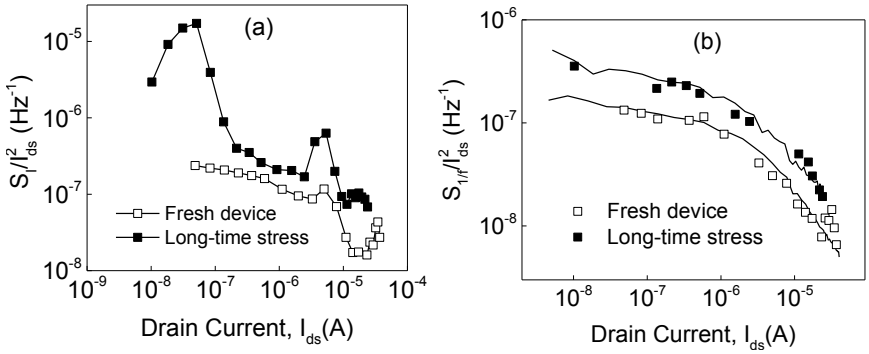


Figure IV-13 (a) Normalized measured drain current power spectral density S_{Id} / I_{ds}^2 versus drain current I_{ds} of the long time stressed UTBB FDSOI MOSFET. (b) Plots $S_{1/f} / I_{ds}^2$ versus I_{ds} of a device before and after long-time stress. The symbols correspond to experimental data and the lines to model (Eq. IV.2) with $\Omega = 4\ V^{-1}$, $N_t = 1.2 \cdot 10^{10}\ cm^{-2}eV^{-1}$ for the fresh device and $\Omega = 7\ V^{-1}$, $N_t = 2.7 \cdot 10^{10}\ cm^{-2}eV^{-1}$ for the stressed device.

In Figure IV-13, a Lorentzian noise is observed in the above threshold region of the fresh device ($I_{ds} > 1\ \mu A$) corresponding to RTN as confirmed by the drain current behavior in the time domain [Figure IV-14(a)]. The extracted values of τ_c and τ_e as a function of the gate voltage presented in Figure IV-14(b) show a behavior similar to that of Figure IV-10,

explained by the advanced NMP theory [202]. In Figure IV-13(a), the occurrence of the strong peak in the subthreshold region of the stressed device ($I_{ds} < 0.1\ \mu A$) is a clear evidence for dominance of a Lorentzian component over the 1/f noise. This Lorentzian noise is correlated with complex RTN, which is confirmed by the behavior of the drain current in the time domain as shown in Figures IV-15(a) and (b). The corresponding histogram of the RTN amplitude, measured at sampling frequency $f_s = 20\ kHz$, shows a typical RTN signal of two traps [Figure IV-15(c)]. The spacing of the first level to the intermediate two levels gives the RTN magnitude of each of the two traps [204], [208]. Since multiple-trap analysis is difficult, we selected sampling frequencies exhibiting single-trap (two-level) RTN as shown in Figure IV-15(d). In the above threshold range, we observed typical RTN signals on one trap.

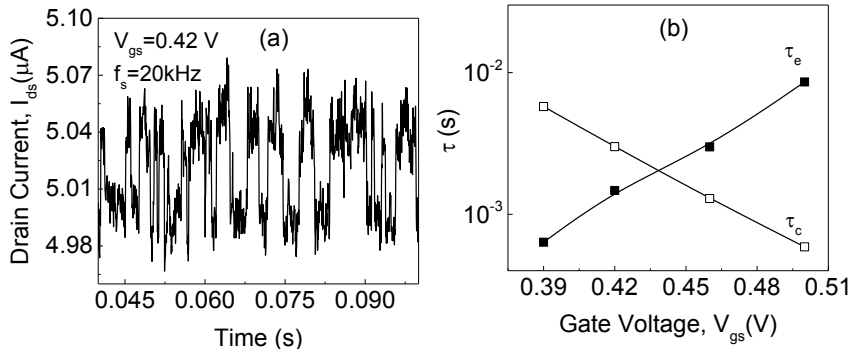


Figure IV-14 (a) RTN waveform measured at gate voltage V_{gs} = 0.42 V and sampling frequency f_s = 20 kHz and (b) time constants τ_c and τ_e versus gate voltage V_{gs} of the FDSOI nMOSFET before long-time stress.

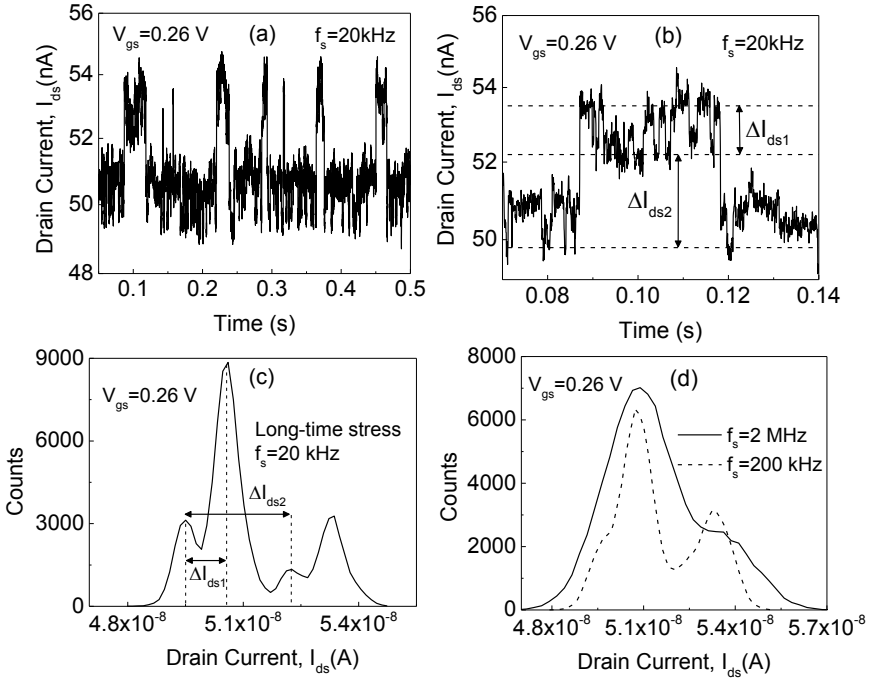


Figure IV-15 (a) RTN waveform and (b) two traps RTN waveform after long-time stress of the FDSOI nMOSFET, measured at gate voltage V_{gs} = 0.26 V with a sampling frequency of f_s =20 kHz. Histograms of amplitude measured at (c) f_s = 20 kHz and (d) f_s = 200 kHz and 2MHz.

The corner frequency f_c and the plateau amplitude A_i of the obtained Lorentzian components are presented in Figures IV-16(a) and (b), respectively. The G-R noise originating from traps in the channel, detected in the gate overdrive range 0.2-0.5 V of the

fresh device is also observed in the long-time stressed device as shown in Figure IV-16. However, the plateau amplitude of both RTN and G-R traps is increased dramatically after long-time HC stress, indicating the generation of more g-r and RTN traps due to HC stress.

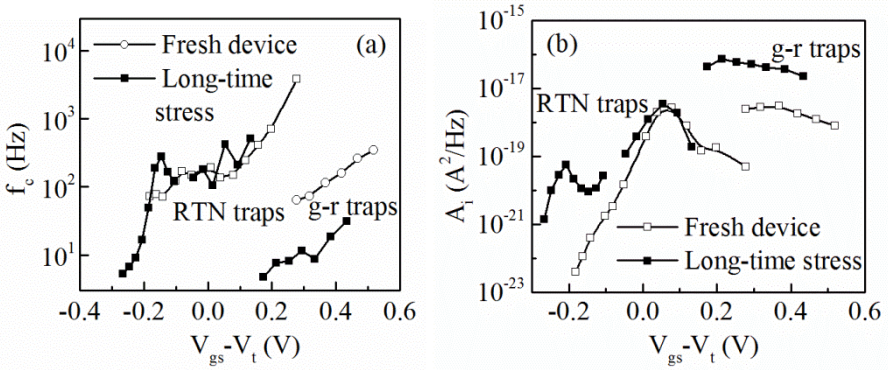


Figure IV-16 Dependence of the corner frequency f_c (a) and plateau amplitude A_i for the g-r noise component of HC-stressed UTBB FDSOI n-MOSFETs.

Figure IV-17(a) presents the V_{gs} dependence of τ_c and τ_e of the RTN traps detected in the long-time stressed FDSOI UTBB n-MOSFET. Three RTN traps are detected in the long-time stressed device. Trap 1 is associated with the RTN observed in the subthreshold region and traps 2 and 3 are responsible for the two-level RTN signals observed in the above threshold region. In general, the plots of the time constant present a curvature described by the extended NMP model using metastable defect configurations [202]. Moreover, the characteristic time constant τ_o defined as the cross-point value of the τ_c-V_{gs} and τ_e-V_{gs} curves in Figure IV-17(a), show no clear correlation with the RTN relative amplitude $\Delta I_{ds}/I_{ds}$ presented in Figure IV-17(b). This indicates that the RTN time constants and the amplitude are weakly correlated, i.e. $\Delta I_{ds}/I_{ds}$ is mainly dominated by the channel lateral trap location in agreement with the results of previous work [206] and [207].

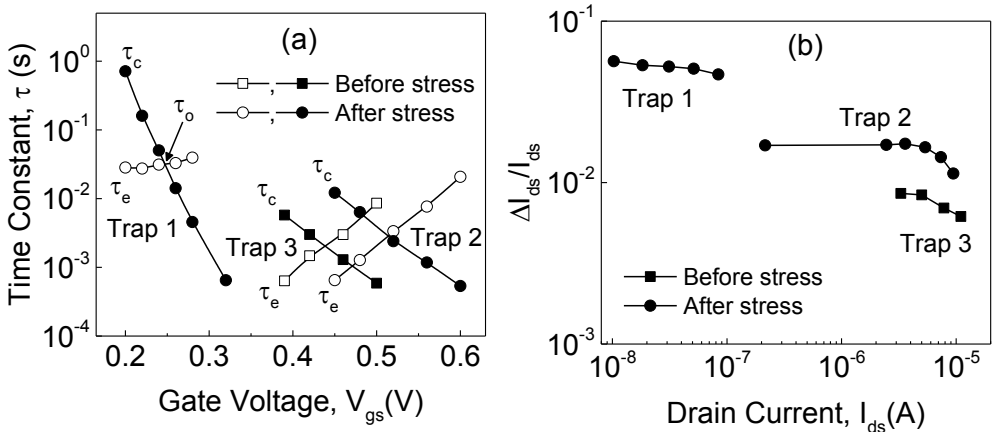


Figure IV-17 (a) Dependence of the extracted τ_c and τ_e on the gate voltage V_{gs} and (b) RTN amplitude ($\Delta I_{ds}/I_{ds}$) on the drain current I_{ds} of the RTN traps of the long-time stressed UTBB FDSOI MOSFETs.

IV.2.2.3 RTN Amplitude

Recently, large RTN fluctuations were observed in the subthreshold regime of nanoscale n-MOSFETs [209]. For a single gate dielectric trap, it has been demonstrated that the RTN amplitude of the drain current fluctuations is related to carrier number and carrier

mobility fluctuations [210], [211], i.e. the RTN amplitude is still determined by the electrostatic impact of trapped charge. Three-dimensional distortion of the potential caused by the defect charge can lead to a non-uniform charge density along the channel, which is known to have large impact on the drain current fluctuation amplitude depending on the trap location over the channel [187], [188], [212]. Furthermore, it has been demonstrated that the RTN amplitude has no correlation to the mean emission and capture time constants and it is mainly dominated not by the trap depth from the interface, but by the randomness of the lateral trap location [206], i.e. the impact of the trap depth from the interface is masked by that of the trap location over the channel.

The RTN relative amplitude ($\Delta I_{ds}/I_{ds}$) can be calculated assuming that trapping of an elementary charge q in the trap located at or near the Si/gate dielectric interface changes the local conductivity stemming from CNF [113]. It has been shown that the relative RTN amplitude for a single trap, located at or near the gate dielectric/silicon interface, can be approximated by [113], [187]:

$$\frac{\Delta I_{ds}}{I_{ds}} = \xi \frac{g_m}{I_{ds}} \frac{q}{WLC_{ox}} \qquad \textbf{Eq. IV.4}$$

where ξ is a fit parameter. Considering the CNF/CMF drain current fluctuation model developed in [197] and including in Eq. IV.4 the mobility fluctuation due to the trap scattering, a generic model for the relative RTN amplitude can be constructed based on the equation:

$$\frac{\Delta I_{ds}}{I_{ds}} = \xi \frac{g_m}{I_{ds}} \frac{q}{WLC_{ox}} \left(1 + \Omega' \frac{I_{ds}}{g_m} \right) \qquad \textbf{Eq. IV.5}$$

with two physical parameters, namely Ω' related to the mobility fluctuation and ξ related to the trap location over the channel. The parameter ξ is introduced to take into account the statistical variability of the trap location over the channel. This is consistent with recent results showing that the threshold voltage is highly sensitive to the charge position, with the most critical position located in the middle of the channel [189].

Figures IV-18(a) and (b) show the plots of $\Delta I_{ds}/I_{ds}$ versus g_m/I_{ds} for typical fresh and HC-stressed devices, respectively. A linear relationship between $\Delta I_{ds}/I_{ds}$ and g_m/I_{ds} is observed as expected from Eq. IV.5. Both parameters ξ and Ω' can be extracted experimentally from the slope ($= \xi q/WLC_{ox}$) and the intercept with the vertical axis ($= \xi\Omega' q/WLC_{ox}$) of the straight lines $\Delta I_{ds}/I_{ds}$ versus g_m/I_{ds}, presented in the insets of Figures IV-18(a) and (b). The knowledge of these two parameters provides a good description of the RTN relative amplitude as shown in Figures IV-18(c) and (d). The large variation of η can be attributed to the huge variability of the threshold voltage associated to single charge trapping, the histogram of which exhibits an exponential distribution due to impact of the trap location over the channel and in the gate dielectric [189], [213].

Figure IV-19 presents experimental results of $\Delta I_{ds}/I_{ds}$ versus I_{ds} for more than ten RTN traps detected in fresh and HC-stressed devices. In fresh devices of the present technology, the detected RTN traps are observed in the above threshold voltage region with $\Delta I_{ds}/I_{ds}$ within 0.25% - 1.1% at $I_{ds} = 10\ \mu A$. However, after HC-stress RTN traps are observed also in the subthreshold region with $\Delta I_{ds}/I_{ds}$ within 1.6% - 5.5% at $I_{ds} = 10\ nA$. For RTN modeling and reliability prediction, the above findings should be taken into account.

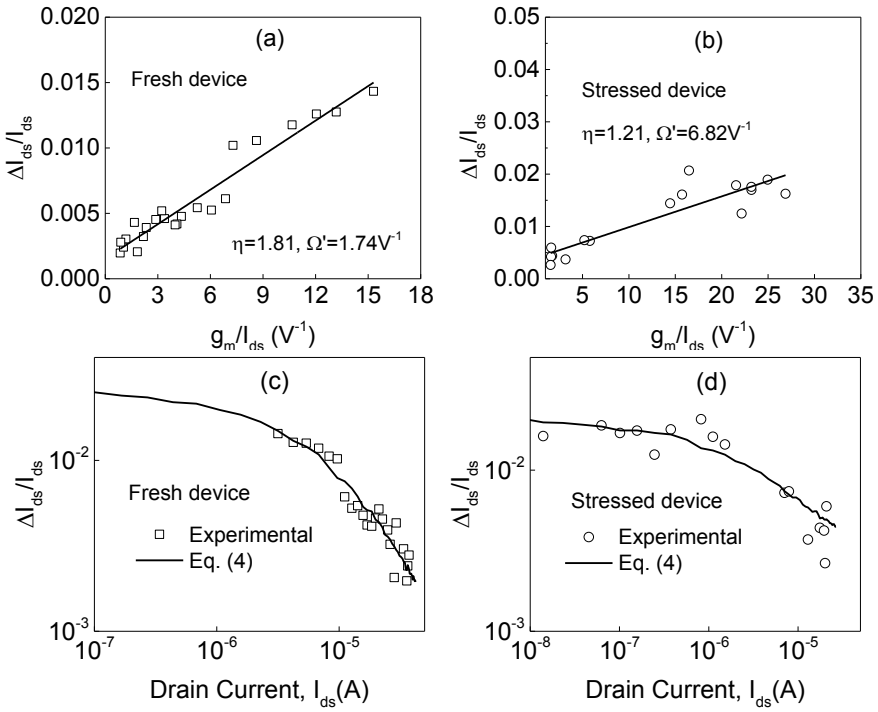


Figure IV-18 Variation of $\Delta I_{ds}/I_{ds}$ with g_m/I_{ds} of RTN traps detected in the (a) fresh and (b) HG-stressed UTBB FDSOI MOSFETs. Insets: parameters ξ=η and Ω´ extracted from the slope and intersect with the vertical axis of the straight lines. Using the extracted parameters ξ=η and Ω´, a comparison between the experimental $\Delta I_{ds}/I_{ds}$ versus I_{ds} data and model results obtained from Eq. IV-8 is presented for the (c) fresh and (d) stressed devices, respectively.

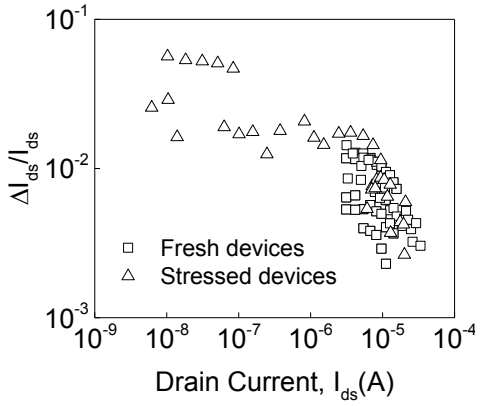


Figure IV-19 RTN relative amplitude ($\Delta I_{ds}/I_{ds}$) versus drain current I_{ds} of RTN traps detected in the UTBB FDSOI MOSFETs before and after HC stress.

IV.2.3 Hot Carrier Degradation Modeling in Nano-scale FDSOI MOSFETs

The transfer characteristics before stress, after stress at $V_{stress} = 1.5\ V$ for 5000 s and the recovery behavior (after 5000 s at $V_{ds} = V_{gs} = 0$) are presented in Figure IV-20(a). No recovery is observed, verifying the findings presented above, namely that interface and/or bulk trap generation are the main degradation mechanisms, which result in degradation of the transistor parameters. From analysis of the transfer characteristics in the linear region, the degradation of the threshold voltage V_t and the subthreshold ideality factor η were obtained. The threshold voltage was extracted from the transconductance linear extrapolation method [155].

Figure IV-20(b) illustrates the transfer characteristics in the saturation region (V_{ds} = *1 V*) before stress and after stress at V_{stress} = *1.5 V* for 5000 s in the forward and reverse mode (with the source and drain electrodes exchanged). The drain current is reduced after stress, indicating that the interface trap generation is extended beyond the pinch-off region, as generated hot-carriers dominate over the entire channel length in short-channel devices [194]. In addition, the drain current is further reduced in the reverse mode, indicating that the trap generation is enhanced near the drain region. These findings are supported with the experimental results of a modified charge-pumping technique [214], demonstrating the generation of HC stress-induced interface traps along the channel length and border traps within a tunnelling distance of the gate oxide/Si interface, located above the pinch-off region near the drain.

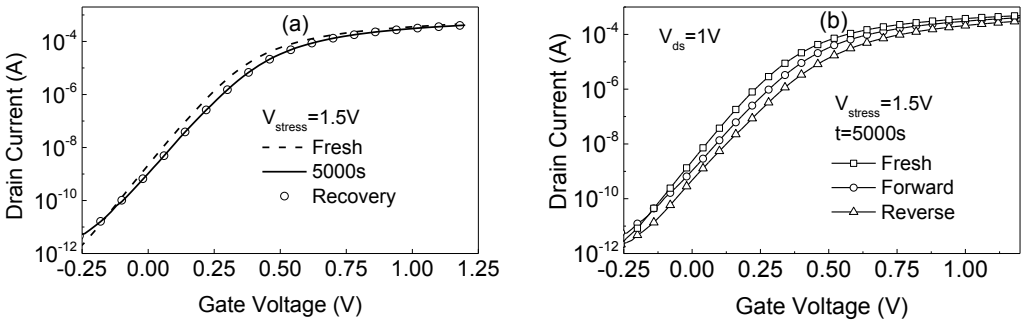


Figure IV-20 (a) Transfer characteristics of UTBB FDSOI MOSFET with W = 0.5 µm and L = 30 nm before stress, after stress at V_{stress} = 1.5 V for 5000 sec and a recovery after stress, measured at V_{ds} = 1 V. (b) Transfer characteristics before stress and after stress at V_{stress} = 1.5 V for 5000 sec in the forward and reverse modes measured at V_{ds} = 1 V.

As has been already mentioned above (see Figure IV-2(a)) for stress times above 1 s the positive threshold voltage shift ΔV_t follows a single time dependent power-law of the form $\Delta V_t \sim t^n$ with the exponent $n \approx 0.28$, indicating the generation of interface traps [179]. Note that in FDSOI MOSFETs, the value of n is smaller than that of bulk n-MOSFETs ($n \sim 0.4$-0.5) for the interface trap generation mechanism and only the front gate interface is degraded during HC stress as shown by a new technique based on capacitance measurements [179]. At short stress times (< 0.1 *s*), it has been demonstrated by fast measurements that the HC degradation is equivalent to the positive bias temperature instability (PBTI) degradation due to the impact of "cold carriers", exhibiting a value for n lower than 0.25 [179].

In Chapter III a complete analytical charge-based compact model for the drain current of nano-scale UTBB FDSOI MOSFETs has been presented, valid in all regions of operation with back gate control [190]. The model includes the device parameters V_t, η and the effective mobility μ_{eff}, which were modeled taking into account the effects of DIBL, CLM, saturation velocity, mobility degradation, quantum confinement, velocity overshoot and self-heating. Thus, modeling the degradation of these parameters could lead to the prediction of the HC-induced device degradation. Analytical models for the threshold voltage with localized interface charges were developed in single-gate bulk MOSFETs [215] and symmetrical double-gate MOSFETs [216]. Because such model is missing for UTBB FDSOI MOSFETs including localized interface and bulk charges, we provide semi-empirical aging models for the transistor parameters, which are widely used in circuit reliability investigations [217].

The impact on the threshold voltage shift of the stress voltages $V_{stress} = V_{ds} = V_{gs}$ and V_{gs} varying from 1.2 to 2 V with drain voltage fixed at V_{ds} = *2 V* is shown in Figures IV-21(a) and (b), respectively.

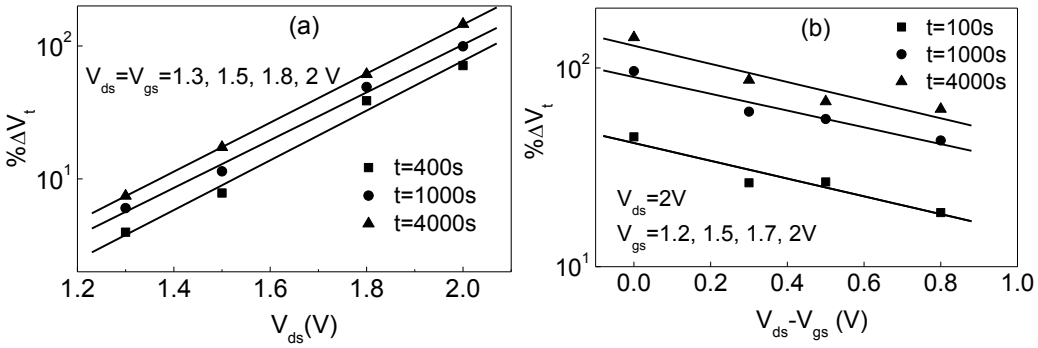


Figure IV-21 Dependence of $\%\Delta V_t$ degradation of UTBB FDSOI MOSFETs with W = 0.5 µm and L = 30 nm on stress voltages $V_{stress} = V_{ds} = V_{gs}$ (a) and (V_{ds} - V_{gs}) with drain voltage fixed at V_{ds} = 2 V and varying gate voltage V_{gs} = 1.2, 1.5, 1.7 and 2 V (b) for different stress times.

The results confirm that the worst case bias condition is at $V_{stress} = V_{ds} = V_{gs}$ following the dependences of the form $\%\Delta V_t \sim exp(c_1 V_{ds})$ and $\%\Delta V_t \sim exp[-c_2(V_{ds}-V_{gs})]$. The plots $\%\Delta V_t$ versus $exp(c_1 \times V_{ds}) \times t^n$ for different values of $V_{stress} = V_{ds} = V_{gs}$ demonstrate that all the data points lie on a straight line for $n = 0.277$ and $c_1 = 3.64\ V^{-1}$ (Figure IV-22(a)) and the plots $\%\Delta V_t$ versus $exp[-c_2(V_{ds}-V_{gs})] \times t^n$ for different values of V_{gs} with fixed $V_{ds} = 2\ V$ demonstrate that all the data points lie on a straight line for $n = 0.277$ and $c_2 = 1.2\ V^{-1}$ (Figure IV-22(b)). Figure IV-22(c) presents the dependence of the $\%\Delta V_t$ with the reciprocal of the channel length, induced by HC stress at $V_{stress} = 1.8\ V$ for different stress times. The inset of Figure IV-22(c) presents the relationship between the $\%\Delta V_t$ degradation and $1/L$, showing that the V_t degradation is strongly dependent on the channel length.

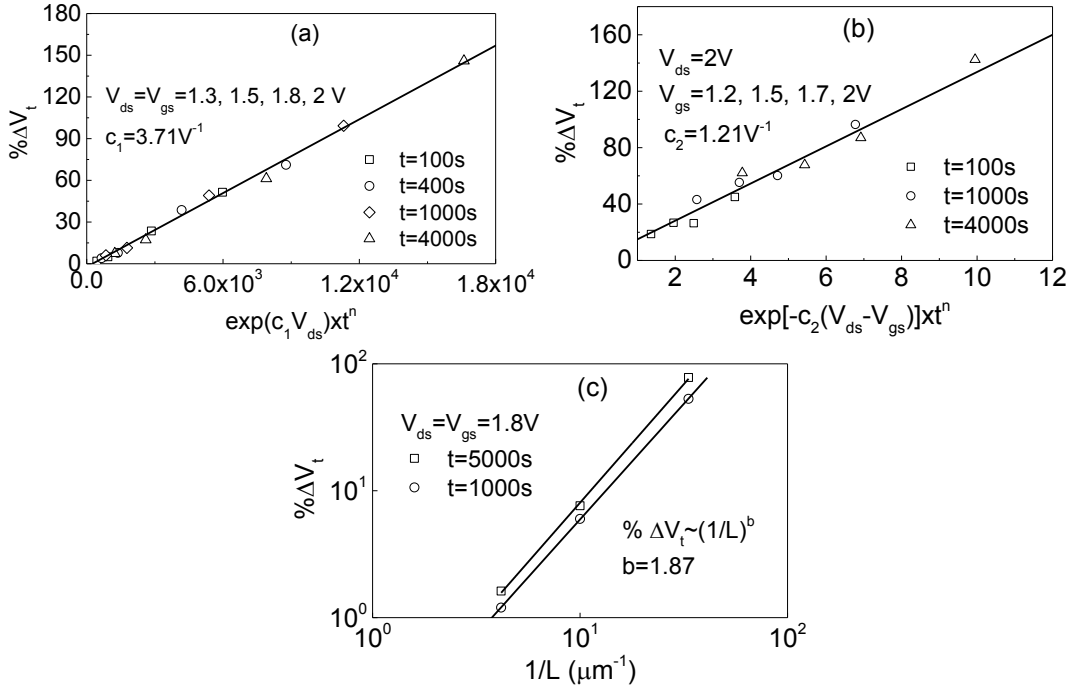


Figure IV-22 (a) Dependence of $\%\Delta V_t$ on $exp(c_1 \times V_{ds}) \times t^n$ of UTBB FD-SOI MOSFET with W = 0.5 µm and L = 30 nm stressed at $V_{stress} = V_{ds} = V_{gs}$ = 1.3, 1.5, 1.8 and 2 V for different times. (b) Dependence of $\%\Delta V_t$ on $exp[-c_2 \times (V_{ds}-V_{gs})] \times t^n$ after stress at V_{ds} = 2 V and V_{gs} = 1.2, 1.5, 1.7 and 2 V for different times. (c) Dependence of $\%\Delta V_t$ degradation on the reciprocal of the channel length L after stress at V_{stress} = 1.8 V for 1000 s and 5000 s.

For the UTBB FDSOI devices of the present technology, taking into account all factors affecting the HC effect, the $\%\Delta V_t$ degradation can be expressed as:

$$\%\Delta V_t = Ct^n \left(\frac{1}{L}\right)^b \exp(c_1 V_{ds}) \exp\left[-c_2 (V_{ds} - V_{gs})\right] \qquad \textbf{Eq. IV.6}$$

In Eq. IV.6, C is a process related prefactor, $n = 0.277$ is the time exponent which is typically in the range of 0.2-0.5 [217], $b = 1.87$ is the gate length dependency which is typically in the range of 2-4 [217] and $c_1 = 3.71\ V^{-1}$, $c_2 = 1.21\ V^{-1}$ denote the drain and gate voltage sensitivity, respectively, which are also process related. Expressing the channel length in nm, Eq. IV.6 fits the experimental data of $\%\Delta V_t$ versus t for $C = 5.46$ for different bias stress conditions, as shown in Figures IV-23(a) and (b). In the model of HC aging prediction, the temperature behaviour can be modelled as Arrhenius law with a thermal activation energy, which can be determined by performing HC stress measurements as different temperatures [217]. In the proposed HC degradation model, the effect of temperature is incorporated in the constant C. Note that the V_t degradation model (Eq. IV.6) has been also successfully applied in double-gate FinFET with model parameters close to those of the UTBBB FDSOI device.

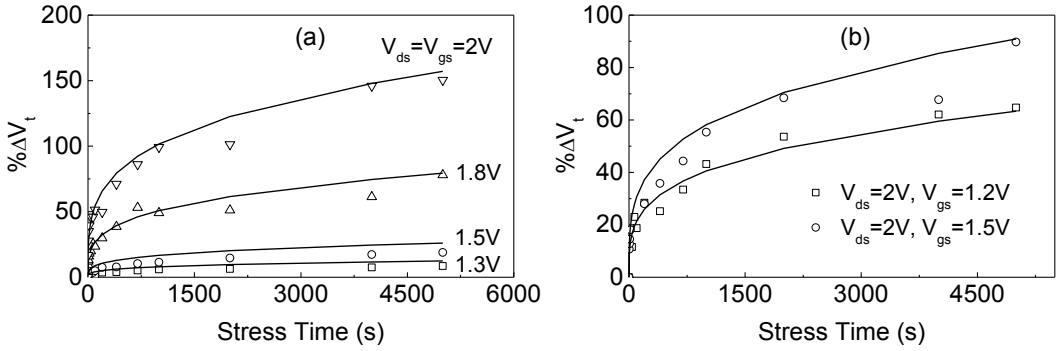


Figure IV-23 Variation $\%\Delta V_t$ with stress time of UTBB FD-SOI MOSFETs with W = 0.5 µm and L = 30 nm stressed at: (a) $V_{stress} = V_{ds} = V_{gs}$ = 1.3, 1.5, 1.8 and (b) V_{ds} = 2 V and V_{gs} = 1.2 and 1.5 V. The symbols correspond to the experimental data and the lines to the model (Eq. IV.6) for C = 5.46.

The change in the effective electron mobility μ_{eff} due to the formation of interface traps in the transistor inversion region is described by the empirical relation [218], [219]:

$$\mu_{eff} = \frac{\mu_{eff,0}}{1 + a_1 \Delta N_{it}} \qquad \textbf{Eq. IV.7}$$

where $\mu_{eff,0}$ is the effective carrier mobility of the fresh device which is degraded by the vertical gate field [190], ΔN_{it} is the HC generated interface trap density and α_1 is a process dependent mobility degradation parameter. In UTBB FDSOI MOSFETs, due to the thin silicon thickness, it has been demonstrated that the self-heating effect is significant [190]. Thus, in addition to the mobility degradation due to the vertical gate field, the electron mobility is degraded with increasing temperature by the SH effect due to different scattering mechanisms. The impact of the SH effect on the HC degradation has been considered by including the temperature rise in the effective carrier mobility [190].

If acceptor-type interface traps appear at the front gate interface of density ΔN_{it} per unit area per unit energy, the ideality factor η should be modified as:

$$\eta = \eta_0 + \frac{q^2 \Delta N_{it}}{C_{ox}} \qquad \textbf{Eq. IV.8}$$

where η_0 is the subthreshold swing coefficient of the fresh device, q is the electron charge and C_{ox} is the gate oxide capacitance per unit area. Thus, the ideality factor degradation due to HC generated interface traps is modelled by the empirical formula:

$$\eta = \eta_0 + a_2 \Delta N_{it} \qquad \textbf{Eq. IV.9}$$

where α_2 is a process dependent subthreshold swing coefficient degradation parameter. However, the HC generated interface trap density ΔN_{it} can be extracted either experimentally by the forward gated-diode method using numerical calculation of integrals involved in the model [220] or with a model based on a deterministic Boltzmann transport equation solver [221]. Thus, for the needs of compact modeling, in Equations IV.7 and IV.9, ΔN_{it} has to be replaced by ΔV_t which can be determined analytically from the empirical formula of Eq. IV.6.

To determine the correlation between ΔN_{it} and ΔV_t, the generated interface trap density ΔN_{it} was assessed by monitoring the ideality factor degradation $\Delta\eta$ exploiting the relation [222]:

$$\Delta N_{it} = \frac{\Delta\eta \, C_{ox} \, \Delta E}{q^2} \qquad \textbf{Eq. IV.10}$$

In Eq. IV.10, ΔN_{it} is quoted as an average value over the Si band gap ΔE and it has a dimension of traps/cm^2. For the case of the worse stress condition ($V_{ds} = V_{gs}$), it is found that $\Delta N_{it} \propto \Delta V_t$ and for constant ΔN_{it} the threshold voltage change ΔV_t increases with V_{ds} (Figure IV-24(a)), while for bias stress $V_{ds} > V_{gs}$ it is $\Delta N_{it} \propto \Delta V_t$ and for constant ΔN_{it} the threshold voltage change ΔV_t increases with (V_{ds}-V_{gs}) (Figure IV-24(b)).

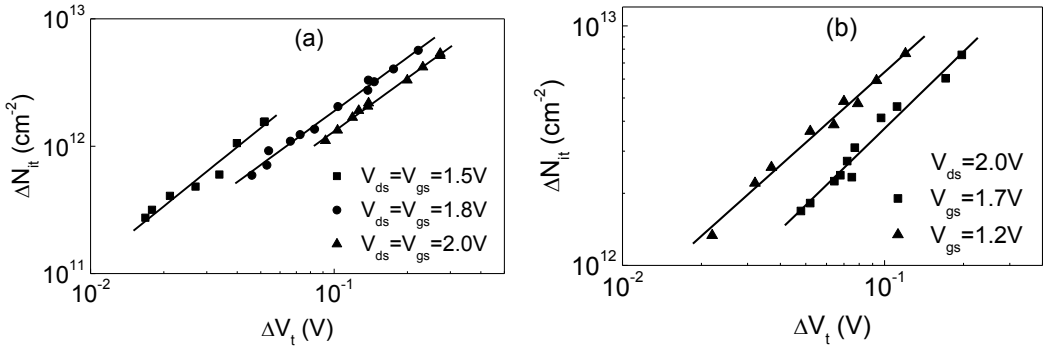


Figure IV-24 Plots of ΔN_{it} versus ΔV_t of UTBB FDSOI MOSFETs with W = 0.5 µm and L = 30 nm stressed at: (a) $V_{stress} = V_{ds} = V_{gs}$ = 1.5, 1.8 and 2 V and (b) V_{ds} = 2 V and V_{gs} = 1.2, 1.7 and 2 V.

Plotting the experimental data of Figures IV-24(a) and (b) in the form of ΔN_{it} versus $\Delta V_t/V_{ds}$ (Figure IV-25(a)) and ΔN_{it} versus $[0.32 + (V_{ds}\text{-}V_{gs})]\Delta V_t$ (Figure IV-25(b)), respectively, all data lie on straight lines.

Therefore, the empirical expressions for the mobility and ideality factor of nanoscale UTBB FDSOI MOSFETs are written as:

$$\mu_{eff} = \frac{\mu_{eff,0}}{1 + a_1\left(0.32 + V_{ds} - V_{gs}\right) \cdot \dfrac{\Delta V_t}{V_{ds}}} \qquad \textbf{Eq. IV.11}$$

$$\eta = \eta_0 + a_2\left(0.32 + V_{ds} - V_{gs}\right)\cdot\frac{\Delta V_t}{V_{ds}} \qquad \textbf{Eq. IV.12}$$

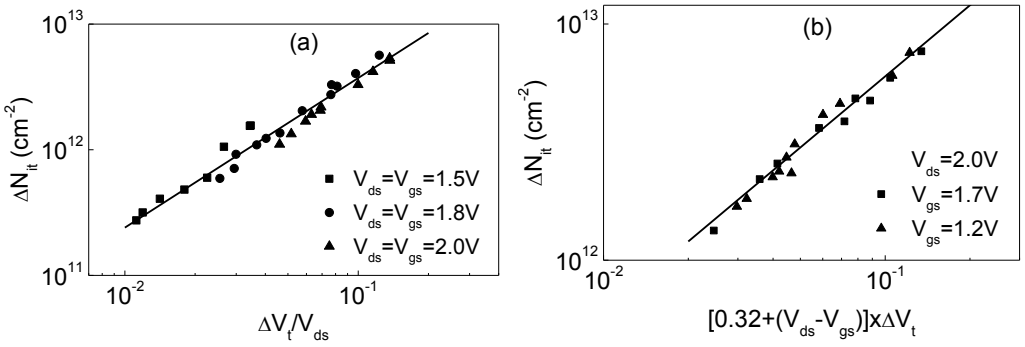


Figure IV-25 (a) Plots of ΔN_{it} versus $\Delta V_t/V_{ds}$ of UTBB FDSOI MOSFETs with W = 0.5 μm and L = 30 nm stressed at $V_{stress} = V_{ds} = V_{gs}$ = 1.5, 1.8 and 2 V and (b) plots of ΔN_{it} versus [0.32 + (V_{ds}-V_{gs})]ΔV_t of transistors stressed at V_{gs} = 1.2, 1.7 and 2 V with fixed V_{ds} = 2 V.

The model described by Eq. IV.12 has been verified for devices of the present FDSOI technology with $\alpha_2 = 7.35\ V^{-1}$, stressed at different bias voltages, as shown in Fig. 9.

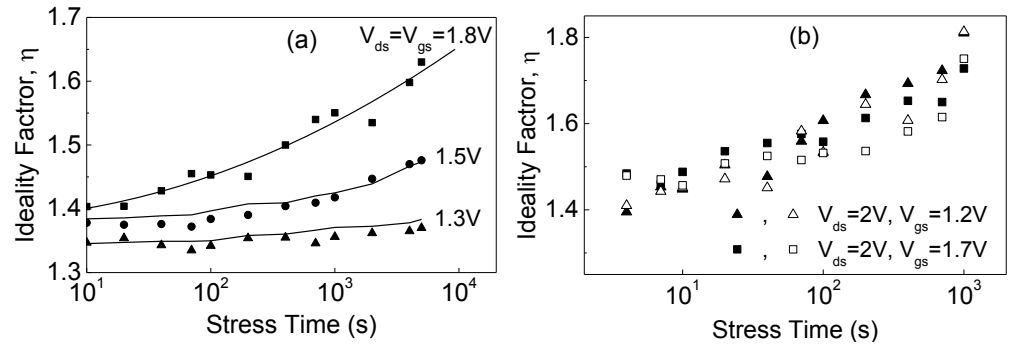


Figure IV-26 Dependence of the ideality factor η with stress time of UTBB FDSOI MOSFETs with W = 0.5 μm and L = 30 nm for different stress voltages V_{stress}. The solid symbols correspond to the experimental data and the solid lines (a) and open symbols (b) to the model (Eq. IV.12) using the parameter $\alpha_2 = 7.35\ V^{-1}$.

Combining equations IV.6 - IV.12 and the analytical compact model [190] described in the previous Chapter, the impact of the HC effect on the device performance can be predicted for different bias stress conditions using the same set of model parameters for all devices. The first step is to calibrate the fresh device by extracting the parameters of the drain current compact model [190]. Then, after extraction of the HC degradation model parameters as described above, the evolution of the device performance with stress time can be predicted for any bias stress condition using the same set of parameters. Figures IV-27 and IV-28 present the experimental and model transfer characteristics of devices stressed at different combinations of stress bias conditions and stress times, using the unique set of model parameters: $C = 5.46$, $n = 0.277$, $b = 1.87$, $c_1 = 3.71\ V^{-1}$, $c_2 = 1.21\ V^{-1}$, $\alpha_1 = 44.76\ V^{-1}$ and $\alpha_2 = 7.35\ V^{-1}$. It is mentioned that in the saturation region ($V_{ds} = 1\ V$), the HC-generated traps are located in the pinch-off region near the drain and the apparent electron mobility reduces to the effective mobility of the unstressed transistor $\mu_{eff,0}$ (i. e. $\alpha_1 = 0$). However, in the saturation region the HC model satisfies the experimental data when the subthreshold swing coefficient degradation parameter η remains unchanged (i.e. $\alpha_2 = 7.35\ \ V^{-1}$). This finding indicates that the HC-generated traps are shallow trap levels affecting only the carrier mobility [223]. The

generation of shallow trap levels located in the silicon body has been demonstrated by low-frequency noise measurements.

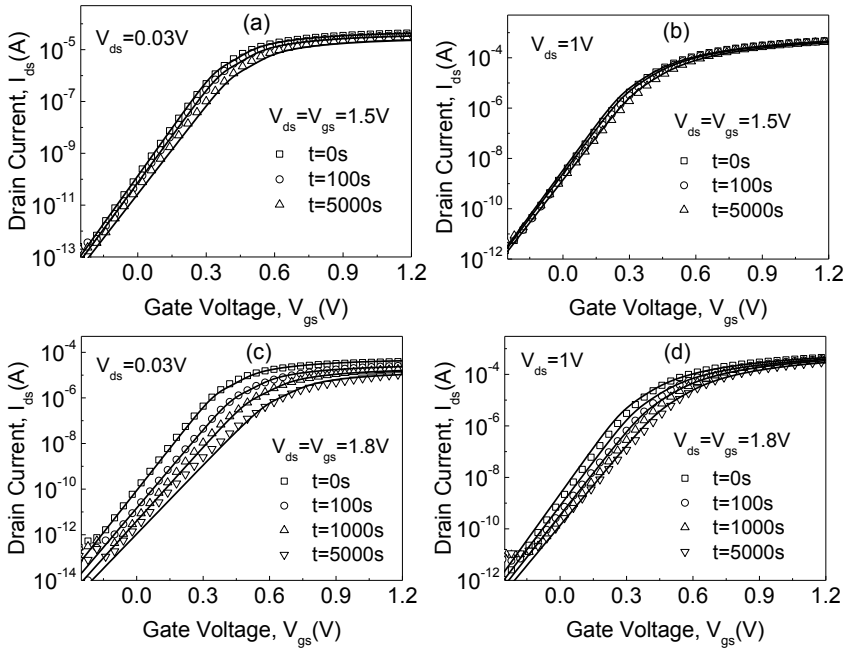


Figure IV-27 Experimental (symbols) and model (lines) transfer characteristics of FDSOI MOSFETs with W = 0.5 μm and L = 30 nm stressed at $V_{ds} = V_{gs} = 1.5$ and 1.8 V for different times, using the unique set of model parameters: C = 5.46, n = 0.277, b = 1.87, $c_1 = 3.71\ V^{-1}$, $c_2 = 11.2\ V^{-1}$, $\alpha_1 = 44.76\ V^{-1}$ and $\alpha_2 = 7.35\ V^{-1}$.

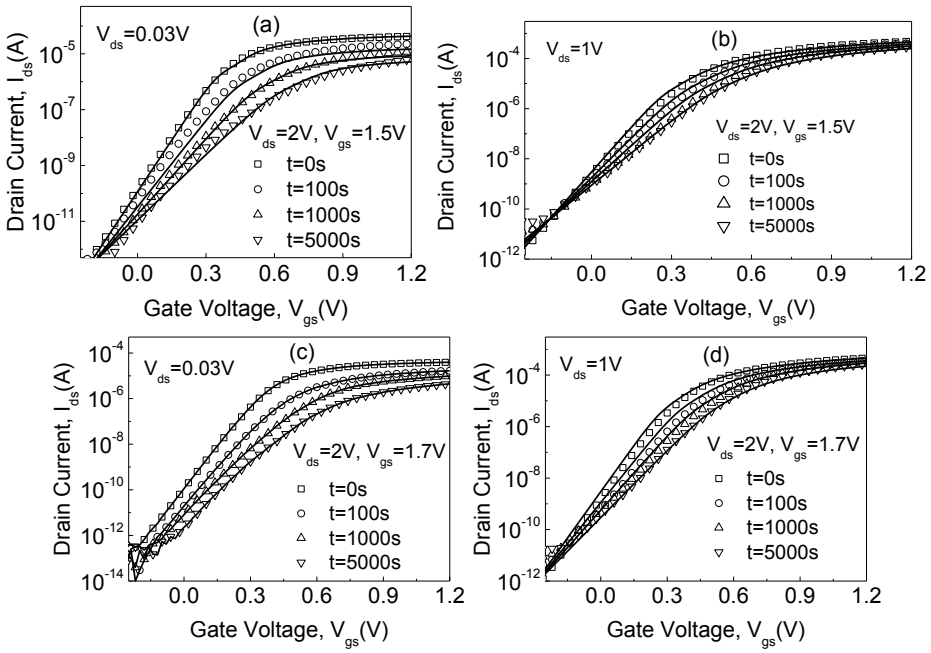


Figure IV-28 Experimental (symbols) and model (lines) transfer characteristics of FDSOI MOSFETs with W = 0.5 μm and L = 30 nm stressed at $V_{ds} = 2$ V and $V_{gs} = 1.5$ and 1.7 V for different times, using the unique set of model parameters: C = 5.46, n = 0.277, b = 1.87, $c_1 = 3.71\ V^{-1}$, $c_2 = 11.2\ V^{-1}$, $\alpha_1 = 44.76\ V^{-1}$ and $\alpha_2 = 7.35\ V^{-1}$.

To extend the empirical model of mobility form linear to saturation region, an extra term is introduced in Eq. IV.11:

$$\mu_{eff} = \frac{\mu_{eff,0}}{1+\gamma \cdot a_1\left(0.32+V_{ds}-V_{gs}\right)\cdot \dfrac{\Delta V_t}{V_{ds}}} \qquad \textbf{Eq. IV.13}$$

where γ is a parameter to indicate for each drain bias the fraction of the interface traps located in the inversion region, which are responsible for the threshold voltage shift [224]. In our model, γ is a function of V_{ds} as:

$$\gamma = \begin{cases} 1 \quad \text{if} \quad V_{ds} \le 0.1V \\ 1.75 \cdot \exp\left(\dfrac{-V_{ds}}{0.18}\right) \quad \text{if} \quad V_{ds} > 0.1V \end{cases} \qquad \textbf{Eq. IV.14}$$

With including the parameter γ in Eq. IV.13, the HC model describes with good accuracy the experimental transfer characteristics for V_{ds} varying from the linear to the saturation region. Figure IV-29 shows an example for the transfer characteristics measured at V_{ds} *=0.6 V* of FDSOI devices stressed at various bias conditions and Figure IV-30 shows the output characteristics of a transistor stressed at $V_{ds} = V_{gs} = 1.5$ *V* for 1000 s.

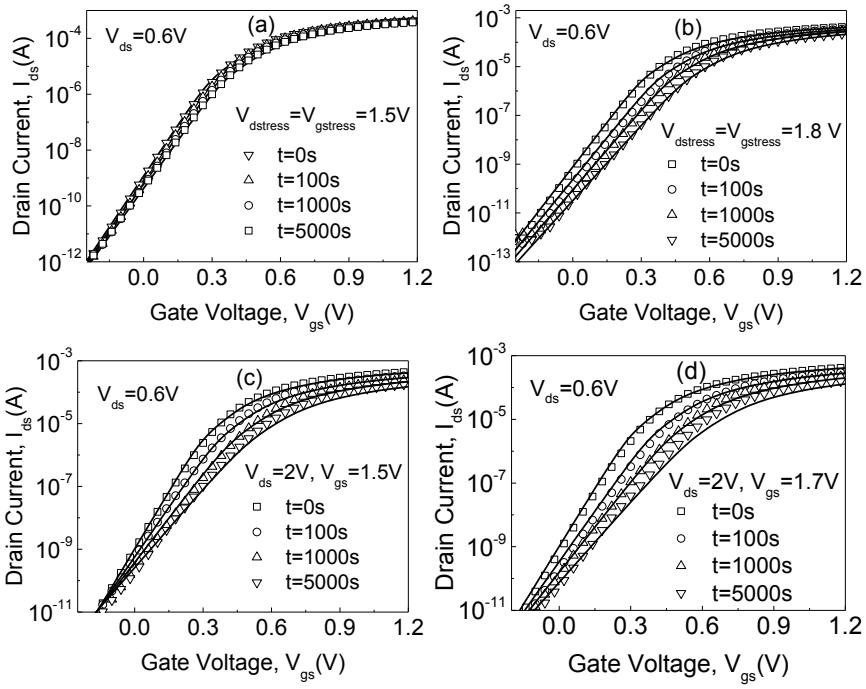


Figure IV-29 Experimental (symbols) and model (lines) transfer characteristics measured at V_{ds} = 0.6 V of FDSOI MOSFETs with W = 0.5 μm and L = 30 nm stressed at various bias conditions, using the mobility model (Eq. IV.13) and the unique set of model parameters: C = 5.46, n = 0.277, b = 1.87, c_1 = 3.71 V^{-1}, c_2 = 11.2 V^{-1}, α_1 = 44.76 V^{-1} and α_2 = 7.35 V^{-1}.

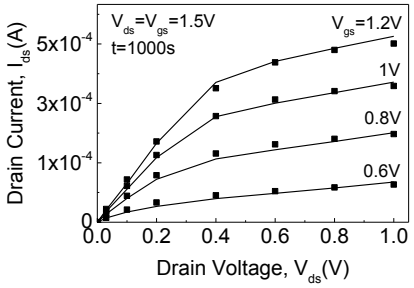


Figure IV-30 Experimental (symbols) and model (lines) output characteristics of FDSOI MOSFET with W = 0.5 μm and L = 30 nm, stressed at V_{ds} = V_{gs} = 1.5 V for 1000 s.

The HC model has been verified for FD-SOI devices with different channel lengths, as shown in Figure IV-31 for *L = 100 nm*. Figures IV-27 - IV-31 show that the agreement between the experimental and model results is good from the subthreshold to the above threshold region, with drain voltage varying from the linear to the saturation region and for any combination of stress bias conditions. Thus, the overall results verify the validity of the proposed HC degradation analytical model, which is suitable for circuit simulators.

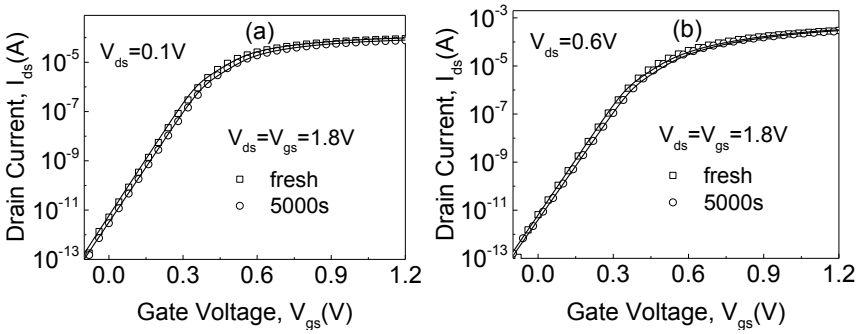


Figure IV-31 Experimental (symbols) and model (lines) transfer characteristics measured at V_{ds} = 0.1 and 0.6 V of FDSOI MOSFETs with W = 0.5 μm and L = 100 nm stressed at V_{ds} = V_{gs} =1.8 V for 5000 s, using the mobility model (Eq. IV.13) and the unique set of model parameters: C = 5.46, n = 0.277, b = 1.87, c_1 = 3.71 V^{-1}, c_2 = 11.2 V^{-1}, α_1 = 44.76 V^{-1} and α_2 = 7.35 V^{-1}.

IV.3 Negative Bias Temperature Instability in FDSOI p-MOSFETs

IV.3.1 Experimental Details

The devices under study were issued from an advanced FDSOI CMOS technology, fabricated by ST Microelectronics as in the case of the HCI experiments. The channel width of the measured devices is *W = 10 μm* and the channel length ranging from 30 to 100 nm. The NBTI effect has been investigated for zero back gate bias and small drain bias voltage (V_{ds} = *-30 mV*) to avoid the influence of the lateral electric field on the NBTI effect.

In order to monitor the threshold voltage (V_t) degradation one has to pause the stress process at selected times to measure the transfer characteristic. However, because the NBTI-related degradation is largely and quickly recoverable, the presence of recovery artifacts during the stress has to be avoided. Using the FastIV module of Agilent B1530, we were able to reduce sufficiently the measurement time in between the stress steps. The transfer characteristics I_{ds}-V_{gs} were measured in a narrow gate bias region around the threshold voltage using one current measurement range. In this way, the stress process was being stopped for the duration of 10 μs, to minimize the measurement delay in such a way that the true recovery is approached. From the measured I_{ds}-V_{gs} characteristics, the threshold voltage V_t was extracted. During the NBTI stress, the applied negative gate bias was $V_{gstress}$ = *-1.5, -1.7* and *-2 V*. During recovery, immediately after stress the device was positively gate biased at V_{grecov} varying from +1.5 to +2 V. Each stress and recovery cycle was performed in different individual devices under a temperature *T* ranging from 50 ^{o}C to 125 ^{o}C to enable determination of the thermal activation energy of the NBTI degradation. For confidentiality

reason, the time unit is not displayed and the time scale is normalized to the maximum stress time t_{max}, which is of the order of several thousands of seconds.

IV.3.2 Characterization of NBTI in nanoscale UTBB FDSOI MOSFETs

The impact of the transistor scaling on the NBTI has been investigated on devices with channel lengths 100, 50 and 30 nm. Figure IV-32 shows the evolution of the threshold voltage shift ΔV_t with the normalized stress time t_{stress}/t_{max} under NBTI stress at $V_{gstress} = -2\ V$ and $T = 125\ ^oC$. The data of Figure IV-32 show no influence of the channel length on the NBTI degradation, in agreement with a recent work demonstrating that the average BTI degradation is independent of the transistor area [225]. The effect of the back bias V_b on the NBTI induced threshold voltage and linear drain current shifts was also investigated, showing negligible influence of V_b on the NBTI degradation in both forward back biasing (accumulation regime) and reverse back biasing (inversion regime) [178], [180]. Therefore, modeling of the NBTI for $V_b = 0\ V$ in UTBB FDSOI MOSFETs with channel length $L = 30\ nm$ can be generalized for the transistors of the present technology.

Figure IV-33 shows the time evolution of the threshold voltage shift ΔV_t during stress at $V_{gstress} = -1.5\ V$ at $T = 75$ and $125\ ^oC$.

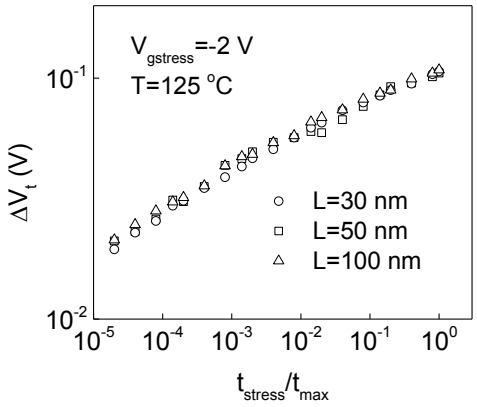


Figure IV-32 Evolution of ΔV_t with the normalized stress time t_{stress}/t_{max} in UTBB FD-SOI p-MOSFET with L = 30, 50 and 100 nm after NBTI stress/recovery cycles at bias stress $V_{gstress}$ = 2 V, V_{grecov} = 2 V and at temperature T = 125 °C.

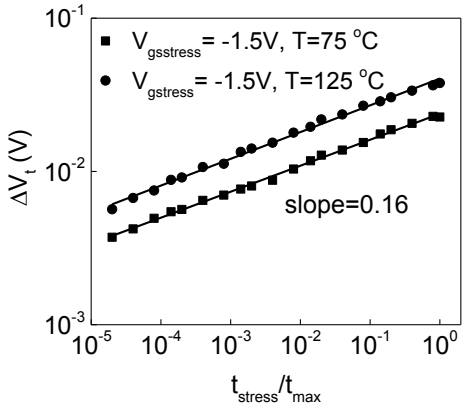


Figure IV-33 Evolution of ΔV_t with the normalized stress time t_{stress}/t_{max} in UTBB FDSOI p-MOSFET with L = 30 nm under NBTI stress at $V_{gstress}$ = -1.5 V and temperatures T = 75 and 125 °C.

A power-law time dependence is observed with time exponent $n = 0.16$ for both temperatures, indicating that the degradation behavior is due to tunneling of holes into the gate dielectric which are captured by pre-existing gate dielectric traps [226], [227]. It is worth noticing that the value of the extracted power-law exponent depends significantly on the delay introduced during the measurement. The temperature-independent exponents in the range 0.07 – 0.2 have been extracted from delay-free measurements [228], [229], [230]. Thus, the results of Figure IV-33 indicate that the delay of 10 μs is enough to make recovery negligible. Similar values for the delay time for current readings were found guaranteeing reliable NBTI measurements [231], [232].

Figure IV-34 shows the dynamics of the V_t shift by reversing the polarity of the gate bias immediately after the negative gate bias stress at temperature $T = 125\ ^oC$. The main feature of these results is a fast V_t recovery (more than 50%) within 2×10^{-5} of the stress time which is difficult to measure experimentally, followed by a slow non-exponential transient. As the time scale is normalized to the maximum stress time, the V_t recovery is described by the recovery fraction defined as the measured V_t shift during recovery divided by its shift just after the NBTI stress. In order to determine the relative importance of the interface and gate dielectric traps on the V_t shift, the recovery fraction of V_t versus t_{recov}/t_{stress} is presented in Figure IV-35 for different recovery voltages. The data show that ΔV_t decays linearly on a logarithmic timescale and the higher positive gate voltage favors the V_t recovery. The above findings indicate that positive charges in the gate dielectric contribute mainly in the recovery of V_t It is worth to mention that in the relaxation transients of Figure IV-35, discrete NBTI relaxation ΔV_t steps are clearly observed, which can be attributed to individual discharging events due to random distribution of defect times and defect number variation in small area devices [233]. However, from a macroscopic modeling point of view, we consider smooth V_t relaxation transients.

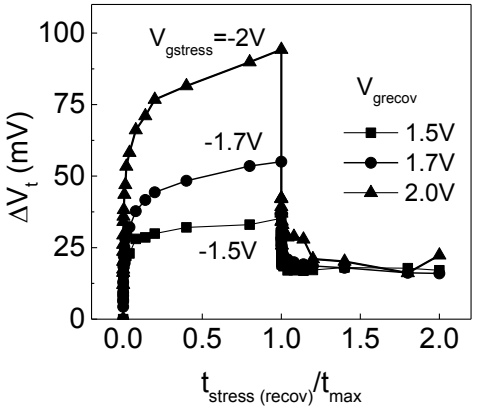


Figure IV-34 Variation of the threshold voltage shift ΔV_t with normalized stress time (t_{stress}/t_{max}) and recovery time (t_{recov}/t_{max}) in UTBB FD-SOI p-MOSFET with L = 30 nm, measured at temperature T = 125 °C under different stress and recovery biases shown in the insets.

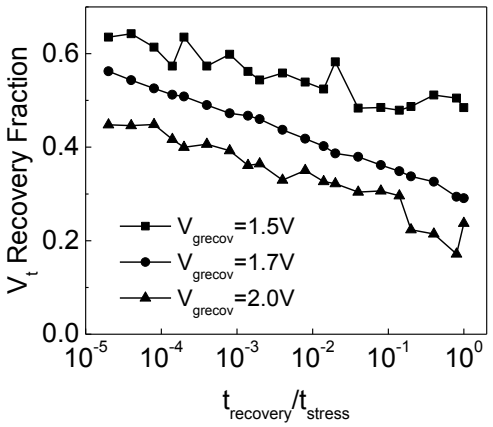


Figure IV-35 Variation of V_t recovery fraction with the normalized recovery time t_{recov}/t_{stress} under different recover voltages Vgrecov at temperature T = 125 °C in UTBB FD-SOI p-MOSFETs with L = 30 nm.

Positive charge built-up within the gate dielectric has been suggested to result from trapping of holes in nitrogen-related pre-existing to stress defects in the gate dielectric [234]. Since LFN is related to the gate dielectric trap density [197], we have characterized the LFN of the same individual device before and after NBTI stress/recovery cycles. Figure IV-36 shows the input-referred gate voltage noise S_{Vg} (Eq. II.48) versus drain current I_{ds} of the

device prior and after NBTI stress/recovery cycle at different bias conditions. The normalized LFN remains almost unchanged before and after stress/recovery cycle at bias stress $V_{gstress}$ = *-1.5 V*, V_{grecov} = *1.5 V* [Figure IV-36(a)], demonstrating that no gate dielectric traps are generated during NBTI stress. Similar behavior of the LFN before and after NBTI stress, averaged on 20 devices has been observed in transistors of the same technology [234]. However, after stress/recovery cycle at higher biases ($V_{gstress}$ = *-2 V*, V_{grecov} = *2 V*) the normalized LFN of the unstressed device increases [Figure IV-36(b)], showing that oxide defects are created due to NBTI stress that is in agreement to previous reports [233], [235]. Injection of electrons from the accumulation layer of the n-silicon layer into the gate dielectric under positive gate bias neutralizes the positive gate dielectric traps, contributing to the V_t recovery. By performing experiments using ultra-fast temperature changes during recovery [236], the neutralization of the NBTI induced positive gate dielectric traps has been interpreted considering inelastic phonon-assisted tunneling of electrons from the n-silicon substrate.

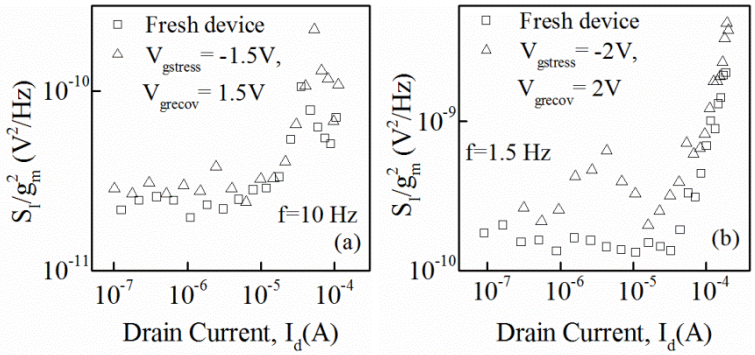


Figure IV-36 Normalized low frequency noise prior and after NBTI stress/recovery cycles at bias stresses: (a) $V_{gstress}$ = -1.5 V, V_{grecov} = 1.5 V and (b) $V_{gstress}$ = -2 V, V_{grecov} = 2 V and at temperature T = 125 °C.

For assessing the relative importance of positive charges from interface states, the generated interface trap density was extracted from the subthreshold slope change ΔSS using the relation:

$$\Delta N_{it} = \frac{\Delta SS \cdot C_{ox} \cdot \Delta E}{q \cdot k \cdot T \cdot \ln(10)} \qquad \textbf{Eq. IV.15}$$

where $k \cdot T$ is the thermal energy, C_{ox} is the gate capacitance per unit area and ΔE is the energy range over which the interface states contribute to the positive charge. As a first-order estimation of the contribution from interface states to ΔV_t, we assume a uniform energy distribution of interface states. Since the charge neutrality level is located approximately $E_g/3$ above the valence-band edge for Si [237], we assume that the donor-like interface traps located below the charge neutrality level contribute to positive charges, i.e. we use $\Delta E \approx 0.37$ *eV*. Figure IV-37 compares the threshold voltage shift due to generated interface states $\Delta V_{it} = q\Delta N_{it}/C_{ox}$ with the measured ΔV_t. We conclude that the NBTI is dominated by positive charges trapped in pre-existing defects within the gate dielectric, with small contribution of generated interface states. The larger contribution of positive charges to the V_t shift than that of generated interface states has been demonstrated in previous work for thin gate dielectrics [238], [239], [240]. Nitridation introduces additional hole traps, enhancing further the contribution of positive charges from gate dielectrics to ΔV_t [227], [234], [241].

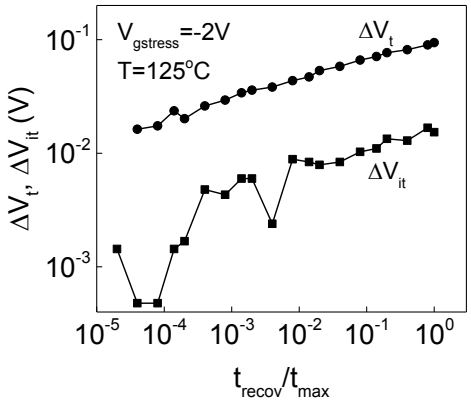


Figure IV-37 Comparison of the measured ΔV_t with the threshold voltage shift ΔV_{it} due to generated interface states under NBTI stress at $V_{gstress}$ = -2 V and temperature T = 125 °C.

IV.3.3 Modeling of NBTI in nanoscale UTBB FDSOI MOSFETs

In the stress phase, for compact modeling we consider the hole trapping in pre-existing gate dielectric defects. According to the universal prediction model [226], [227], the V_t shift due to capture of holes by the gate dielectric traps is described as power-law function of stress time with time exponent $n = 0.16$ and ΔV_t is inversely proportional to C_{ox}. Furthermore, the density of holes injected into the gate dielectric is linearly proportional to the holes density and exponentially dependent on the temperature and the gate dielectric electric field $E_{ox} = (V_{gs} - V_t)/t_{ox}$ [242]. In this work, the NBTI stress of FD-SOI p-MOSFETs was evaluated and found to be reasonably well described by the function (for $V_{ds} \approx 0$):

$$\Delta V_t = A \cdot t_{ox} \cdot \sqrt{\varepsilon_{ox} E_{ox}} \cdot \exp\left(\frac{E_{ox}}{E_0}\right) \cdot \exp\left(\frac{-E_a}{kT}\right) \cdot t^n \qquad \textbf{Eq. IV.16}$$

In Eq. IV.16, A is the field acceleration pre-factor related to the density of holes injected into the gate dielectric, t_{ox} is related to $1/C_{ox}$, $\varepsilon_{ox}E_{ox}$ is related with the density of holes in the channel, E_0 is parameter related to the gate dielectric and E_a is the activation energy. Using the model of Eq. IV.16, Figure IV-38 verifies the change of V_t under different NBTI bias stress conditions and temperatures. For the FD-SOI devices of the present technology, with t_{ox} in cm, the model parameters are: $n = 0.16$, $A = 3.72 \times 10^9$ $V/C^{1/2}$, $E_0 = 3.47$ MV/cm and $E_a = 0.084$ eV which is in agreement with the activation energy measured in similar devices [241].

Within the framework of trapping/detrapping of holes in gate dielectric traps, the recovery fraction can be expressed as a function of the ratio of stress time over recovery time t_{recov}/t_{stress}. In the model reported in [243], derived from a work where the V_t shift is caused by elastic tunneling of channel charge into the gate dielectric traps [244], the recovery function is described by the logarithmic time dependence:

$$\mathrm{Recovery Function} = K_r \cdot V_{gs}^c \cdot \frac{\ln\left(1 + \frac{\tau_e t_{stress}}{\tau_c t_{recov}}\right)}{\Delta V_{ts}} \qquad \textbf{Eq. IV.17}$$

where ΔV_{ts} is the threshold voltage shift at the end of the stress phase. We found that the model of Eq. IV.17 describes well the recovery behavior, with all model parameters found to vary with the recovery voltage, complicating the modeling requirements. However, the work

relying on elastic tunneling can be considered outdated, since literature data show that the single trap time constants are strongly temperature activated [245].

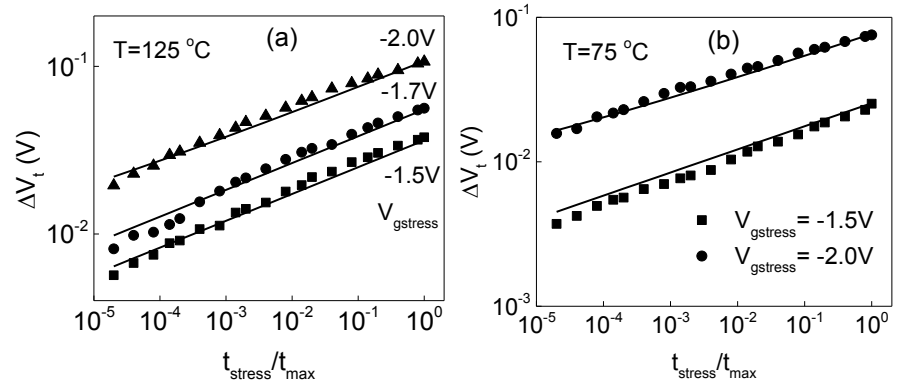


Figure IV-38 Evolution of ΔV_t with the normalized stress time t_{stress}/t_{max} in UTBB FDSOI p-MOSFET with L = 30 nm under different NBTI stress voltages Vgstress at temperatures T = 125 °C (a) and 75 °C (b). The symbols are experimental data and the lines are the results of the model of Eq. IV.16.

In a universal relaxation law model reported in [230], [246], the recovery phase is modeled by the simple function:

$$Recovery Function = \left[1 + B\left(\frac{t_{recov}}{t_{stress}}\right)^{\beta}\right]^{-1} \qquad \textbf{Eq. IV.18}$$

with two model parameters (B, β), which has been applied successfully in 22 nm tri-gate transistors [247]. In this model, the parameter B is a function of the recovery voltage and β is approximately constant simplifying the modeling requirements [247]. In our work, a modified version of the functional form of Eq. IV.18 was found to describe better the recovery behavior of UTBB FDSOI devices given by:

$$Recovery Function = 1 - B\left(\frac{t_{recov}}{t_{stress}}\right)^{\beta} \qquad \textbf{Eq. IV.19}$$

More recently [248], the time evolution of the recovery has been described with empirical expression which includes the contributions of both transient interface trap occupancy and holes trapping/detrapping models. However, the model reported in [248] is more complex than the simple model of Eq. IV.19, which makes it not suitable for implementation in circuit simulation tools. It is noticed that that the recovery function (Eq. IV.19) can be applied up to time for complete recovery, i.e. for recovery fraction zero.

The NBTI recovery in p-MOS devices has been shown to be accelerated by increasing the temperature [249]. Figure IV-39(a) shows the V_t shift as a function of t_{recov}/t_{max} under recovery voltage $V_{grecov} = 2\ V$ and at temperatures 75 and 125 °C. It is clearly observed that the V_t shift is enhanced with increasing the temperature. However, the V_t recovery is faster at the lower temperature as shown in Figure IV-39(b). The results of Figure IV-39 are in agreement with the results reported in [249]. These findings can be explained considering that the permanent part of degradation (interface trap creation) is enhanced with increasing the temperature, whereas the recoverable part (hole trapping/detrapping in preexisting gate dielectric traps) remains unchanged.

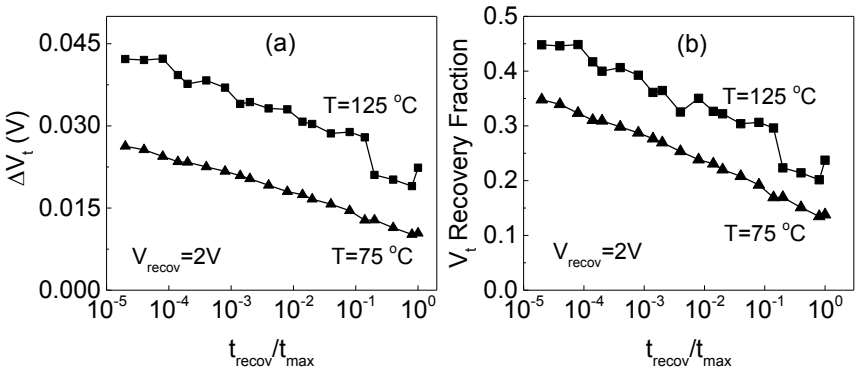


Figure IV-39 Evolution of the V_t shift (a) and the recovery fraction (b) with the normalized recovery time t_{recov}/t_{max} in UTBB FDSOI p-MOSFET with L = 30 nm under recovery voltage V_{grecov} = 2 V at temperatures: T = 125 °C and 75 °C.

Figure IV-40 shows recovery data compared to Eq. IV.19 for different passivation gate voltages and temperatures, for normalized recovery time t_{recov}/t_{max} varying from 2×10^{-5} to 1, capturing the recovery trend very well.

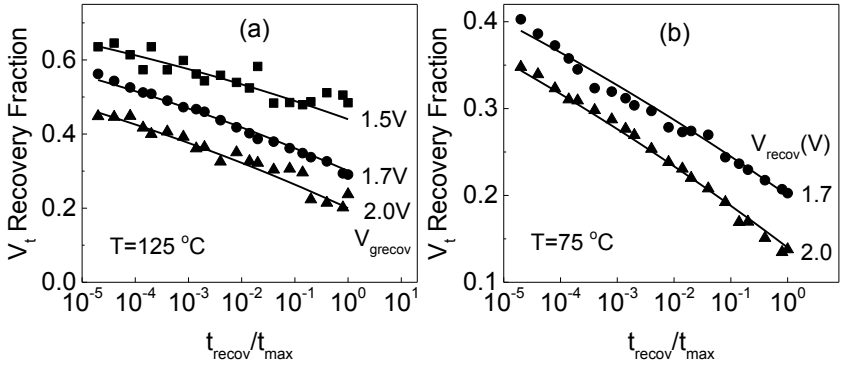


Figure IV-40 Variation of the V_t recovery fraction with the normalized recovery time t_{recov}/t_{max} of UTBB FDSOI p-MOSFETs under different recovery voltages V_{grecov} and at temperatures: (a) T = 125 °C and (b) T = 75 °C.

To predict the temperature dependence of the recovery in simple analytical models, the recovery time was scaled by the activation energy of the assumed Arrhenius behavior [246]. In this work, we found that the temperature dependence of the recovery is captured by scaling the coefficients B and β by (T/T_0), where T_0 is the room temperature. For any combination of recovery temperature T and recovery gate voltage V_{grecov}, the values of the normalized recovery coefficient follows a unified relation of the form:

$$B \cdot \frac{T}{T_0} = 0.154 + 0.44 \cdot V_{grecov} \qquad \textbf{Eq. IV.20}$$

as shown in Figure IV-41(a). For a wide temperature range, the recovery model of Eq. IV.19 captures the recovery trend very well for constant values of $\beta \times (T_0/T) = 0.021$, simplifying the compact modeling. These values of B and β complete the recovery model (Eq. IV.19) for the nanoscale FDSOI devices of the present technology that includes both temperature and recovery voltage dependencies. We mention that our NBTI data show a remarkably suppressed recovery in comparison with the familiar R-D model of [225], [250]:

$$\mathrm{Recovery Function} = 1 - B \cdot t_{recov}^{n} \qquad \textbf{Eq. IV.21}$$

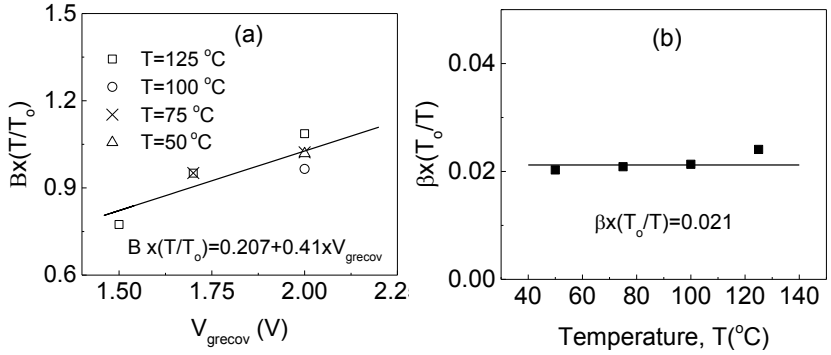


Figure IV-41 (a) Normalized recovery coefficient B × (T/T_0) versus recovery gate voltage V_{grecov}. (b) Normalized recovery coefficient β × (T_0/T) versus temperature. The symbols are experimental data and the lines are the best fitted lines.

Summarizing, a limited number of parameters is needed in the models of the V_t shift during the NBTI stress and the recovery phases in nanoscale UTBB FDSOI p-MOSFETs with TiN/HfSiON gate dielectric stack. The impact of the NBTI stress on the device performance can be captured through V_t included in the analytical drain current compact models reported in [139] and [190]. However, individual devices of small gate area are expected to show important statistical dispersions. Threshold voltage V_t relaxation transients measured on a large number of small area devices have shown significant device-to-device spread, with a mean transient behaving as that of a large device [233]. From statistical analysis of the model parameters extracted from such data, the average values of the model parameters and the errors of the average values can be obtained, which can be used for implementation of the NBTI modeling in circuit simulation tools.

IV.4 Summary and conclusions

Reliability issues including HCI and NBTI have been thoroughly studied in nanoscale UTBB FDSOI MOSFETs. The hot-carrier degradation of nanoscale UTBB FDSOI n-MOSFETs has been investigated under different drain and gate bias stress conditions. A detailed study showed that the worst degradation condition occurs at $V_{gs} = V_{ds}$. The degradation mechanisms have been identified by combined LFN measurements at room temperature in the frequency and time domains. In fresh devices, the measured noise is composed of 1/f noise related to gate dielectric traps within a tunnelling distance from the interface and Lorentzian noise components related either to G-R traps in the silicon film or to metastable RTN traps located at or near the gate dielectric/silicon interface. After HC-stress for short-time, the results show that G-R and RTN traps are annihilated, which has been attributed to hydrogen released due Si-H dissociation by HC-stress. However, after HC-stress for long-time, the LFN is dominated by large RTN from the subthreshold to the above threshold regions. In addition to the traps detected in the fresh device, analysis of simple RTN observed in the HC-stressed device revealed the presence of additional RTN traps in the subthreshold region.

Analysis of the RTN amplitude of several individual traps detected in fresh and HC-stressed devices show the lack of correlation between RTN amplitude and trap time constants. The results indicate that the RTN amplitude is determined by the electrostatic impact of the trapped charge, following a modified CNF/CMF model. An analytical expression for the RTN

amplitude is proposed including two physical parameters: Ω' related to the carrier number and mobility fluctuations and ξ related to the trap location over the channel. These parameters can be extracted from experimental data of the RTN relative amplitude, enabling to predict the RTN level from the subthreshold to the above threshold region.

Additionally, the impact of the HC degradation on the device parameters has been expressed with semi-empirical models in terms of the stress time, channel length, drain bias and gate bias. Based on our analytical compact model, HC aging model is proposed enabling to predict the device degradation stressed under different bias conditions, using a unique set of few model parameters determined for each technology through measurements.

Finally, the NBTI stress characteristics and the recovery behavior under positive bias temperature stress of HfSiON gate dielectric UTBB FD-SOI p-MOSFETs have been investigated. Comparison of the measured V_t shift with that due to generated interface states indicate that the NBTI is dominated by exchange of channel charge carriers with pre-existing traps in the gate dielectric. In the recovery phase, the V_t shift includes a fast initial transient, followed by a very slow non-exponential transient. A model for the NBTI has been developed by considering hole-trapping/detrapping mechanisms, capturing the temperature and bias voltage dependence. The presented NBTI model can be implemented for development of reliability simulation tools in nanoscale FDSOI devices.

V Variability Issues in nano-scale MOSFETs

V.1 Introduction

As has been already mentioned in Chapter I, process variations within CMOS technologies are usually categorized into global and local variations. Concerning the global variations, the device parameters change smoothly all over the wafer. On the other hand, for local variability or mismatch, each MOS transistor is affected differently even from its close neighbor.

Mismatch is by nature an uncorrelated stochastic process, which is increasing due to the scaling down of CMOS technologies - implying the reduction of the device area - inevitably leads to important issues related to the statistical parameters variability [42], [251]. As a result, a crucial issue in MOSFETs and especially in advanced nano-scaled devices is the study of drain current local variability, as it affects the performance of analog and digital circuits such as current mirrors or SRAM cells [252]. In FDSOI technologies, the drain current mismatch has been studied in terms of the electrical parameters fluctuation and the silicon thickness variation [253], [254]. Furthermore, a drain current mismatch model was proposed for FinFET devices, which is valid only in the subthreshold region [255]. However, in order to accurately predict the stochastic variations, a model that describes well the drain current variability sources in all operation regions is required.

In this chapter, first we present the mismatch measurement system and the test structures used to characterize the phenomenon.

Second, a drain current mismatch model based on the main sources of drain current local variability, valid from linear to saturation region is presented [256]. More precisely according to the first mismatch studies, the main sources of the drain current, I_d mismatch are related to the local fluctuations of the threshold voltage, V_t and the current gain factor, β [42], [251]. The source-drain series resistance mismatch and its impact on the drain current variability of FDSOI devices has been reported in recent works [257], [258], [259]. Indeed, we studied the SD series resistance mismatch on the drain current variability in bulk n-MOS transistors processed with 28 nm Gate-first technology and extended for the first time the drain current local variability model in the saturation region as well.

Next, a drain current local variability model valid in linear region but including all the mismatch sources is presented [260]. Therefore, this model relies on four parameters, namely the fluctuations of the threshold voltage, V_t, the current gain factor, β, the SD series resistance and the ideality factor, n. The proposed model has been validated experimentally and by simulations. More precisely, it was used to characterize advanced CMOS technologies, like sub 15 nm Si/SiGe Trigate nanowire p-MOSFETs [260] and 14nm Si bulk FinFETs [261].

Afterwards, a thorough study of the drain current local variability in advanced FDSOI MOSFETs and, for the first time, a fully functional drain current mismatch model valid in all operation regions is presented [262]. In addition, it has been demonstrated that the gate oxide thickness scaling is responsible for the high leakage currents due to tunneling through the gate oxide [52]. Since the gate current can be used as a characterization tool for the oxide thickness, investigation of the gate current local variability and development of a model which properly describes these variations are also required. Indeed, for the first time, we

present a gate current local variability model, based on the local fluctuations of the threshold voltage, V_t, and the gate oxide thickness, t_{ox}. The proposed models for the drain and gate current mismatch were verified, using a Lambert function based compact model and performing Monte Carlo simulations that reproduce accurately the experimentally measured current variations.

Finally, the drain current compact model of Chapter III implenteded in Verilog-A code has been used to examine the impact of drain current variability on fundamental circuits in Cadence Spectre.

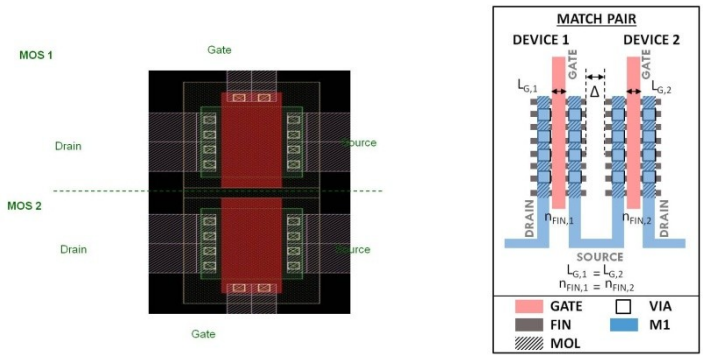
V.2 Mismatch test structures

Variability measurements require special equipment such as the fully automatic probe station depicted in Figure V-1.

Figure V-1 300mm Cascade MicroTech probe station.

The mismatch phenomenon is characterized by measuring two identical MOS devices (namely, MOS1 and MOS2) within the same die, the so-called "pair" transistors. These transistors have the following main features:

- ✓ Placed in pairs
- ✓ Spaced by the minimum allowed distance defined by the technology node
- ✓ Laid out in an identical environment
- ✓ Electrically independent with symmetric connections.



(a) **(b)**

Figure V-2 Example of paired (a) Bulk MOSFETs and (b) FinFETs.

Examples of matched transistors are illustrated in Figure V-2 for two different technologies.

Every time we perform local variability measurements, a large number of pair transistors is necessary in order to ensure a significant statistical population. For this reason 300 mm wafers and a B1500 Agilent unit with a fully automatic 300mm Cascade MicroTech probe station were used in our experiments.

V.3 Drain Current Local Variability from Linear to Saturation Region

V.3.1 Drain current mismatch model from linear to saturation region

In order to build a general drain current mismatch model, the main sources of drain current local variability have to be taken into account through the sensitivity of the drain current to the MOSFET parameters, i.e V_t, β and R_{sd}. Therefore, considering the first order Taylor approximation, the drain current variation can be expressed as the sum of the principal contributions as [258],

$$\frac{dI_d}{I_d} = \left(\frac{1}{I_d}\cdot\frac{\partial I_d}{\partial V_t}\right)\cdot dV_t + \left(\frac{1}{I_d}\cdot\frac{\partial I_d}{\partial \beta}\right)\cdot d\beta + \left(\frac{1}{I_d}\cdot\frac{\partial I_d}{\partial R_{sd}}\right)\cdot dR_{sd} \qquad \textbf{Eq. V.1}$$

After calculating the partial derivatives of I_d with respect to V_t, β and R_{sd}, the expression describing the drain current mismatch in the linear region is obtained as [258],

$$\sigma^2\left(\Delta I_d / I_d\right) = \left(\frac{g_m}{I_d}\right)^2\cdot\sigma^2\left(\Delta V_t\right) + \left(1 - G_d\cdot R_{sd}\right)^2\cdot\sigma^2\left(\frac{\Delta\beta}{\beta}\right) + G_d^2\cdot\sigma^2\left(\Delta R_{sd}\right) \qquad \textbf{Eq. V.2}$$

where $\sigma(\Delta V_t)$ $\sigma(\Delta\beta/\beta)$ and $\sigma(\Delta R_{sd})$ are the standard deviations of the threshold voltage, the gain factor (Eq. II.16) and the SD series resistance mismatch respectively, g_m is the transconductance and G_d is the channel conductance in the linear region.

Furthermore, a useful approach concerning the mismatch study in linear operation is based on the Y-Function (Equation II.13), which is independent of R_{sd}. Indeed, a Y-Function based methodology has been proposed in order to extract directly the V_t and β local variations, using the mismatch of the Y-Function [258]. According to [257], the Y-Function mismatch can be modeled from weak to strong inversion by,

$$\sigma^2\left(\Delta Y / Y\right) = \left(\frac{\beta\cdot\sigma^2\left(\Delta V_t\right)}{4\cdot\beta\cdot n^2\cdot\left(k\cdot T/q\right)^2 + Y^2}\right) + \frac{1}{4}\cdot\sigma^2\left(\frac{\Delta\beta}{\beta}\right) \qquad \textbf{Eq. V.3}$$

The limitation of all above equations is that they are only valid in the linear operation regime. In the present work, the drain current local variability model described in [257] has been extended in order to include the saturation region in the calculation of the drain current mismatch. Using again the sensitivity analysis as in Eq. V.1 and making the assumption that

$$R_s = R_d = R_{sd}/2 \qquad \textbf{Eq. V.4}$$

the partial derivative of I_d with respect to R_{sd} can be calculated as,

$$\frac{1}{I_d}\frac{\partial I_d}{\partial R_{sd}} = \frac{g_m}{2} + g_d \qquad \textbf{Eq. V.5}$$

where g_d is the output conductance.

As a result, combining Equations V.1 and V.5, it is easy to show that the drain current local variability from weak to strong inversion in both linear and saturation regions can be described by,

$$\sigma^2\left(\frac{\Delta I_d}{I_d}\right) = \left(\frac{g_m}{I_d}\right)^2 \cdot \sigma^2(\Delta V_t) + \left(\left(1 - \left(\frac{g_m}{2} + g_d\right) \cdot R_{sd}\right)^2\right) \cdot \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \left(\frac{g_m}{2} + g_d\right)^2 \cdot \sigma^2(\Delta R_{sd}) \qquad \textbf{Eq. V.6}$$

Note that, as compared to Eq. V.2 which is valid in the linear region, Eq. V.6 is generalized by including also the saturation region as manifested by the transconductance contribution that may dominate the output conductance term for large drain voltage.

V.3.2 Drain current mismatch model validation

V.3.2.1 Experimental Results

The devices measured in this work are bulk n-MOS transistors, issued from a 28nm planar CMOS technology with channel width (W) varying from 10 down to 0.08 µm and channel length (L) varying from 5 down to 0.03 µm. The devices were fabricated by ST Microelectronics in France and present also pocket implants. A sample of 70 pairs of identical MOS transistors (namely, MOS1 and MOS2), was necessary for matching measurements. Drain current measurements in both linear ($V_d = 30\ mV$) and saturation regions ($V_d = 1\ V$) were performed. Figures V-3(a)-(d) present typical I_d-V_g characteristics in both linear and saturation regions, illustrating the single device variability over full wafer for the nominal device.

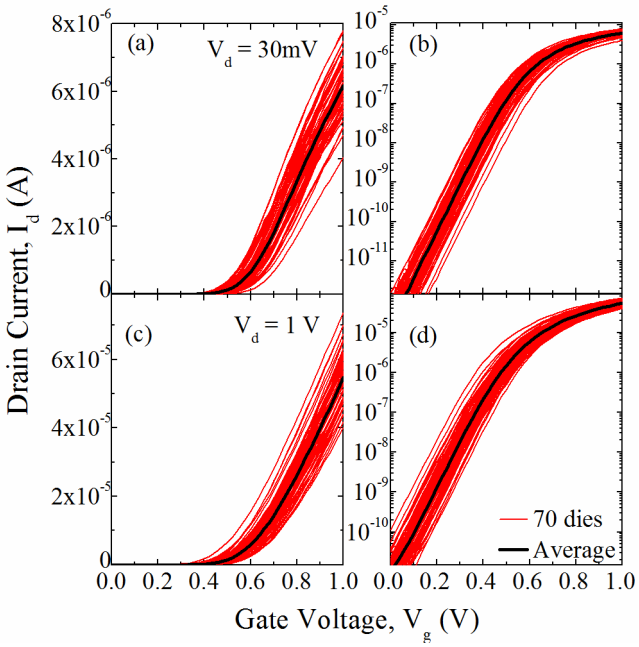


Figure V-3 Experimental $I_d(V_g)$ variability characteristics and their mean value in linear (a, c) and logarithmic scale (b, d) at low (a, b) and high (c, d) drain voltage of an ensemble of 70 bulk n-MOSFETs with channel width W = 0.08 µm and channel length L = 0.03 µm.

As in nominal dimension devices, the drain current difference between two paired transistors might reach several decades, the drain current mismatch, $\Delta I_d/I_d$, is no longer evaluated with a linear difference but using the log difference as [257],

$$\Delta I_d / I_d = \ln\left(I_{d2} / I_{d1} \right) \qquad \textbf{Eq. V.7}$$

where I_{d1} and I_{d2} refer to the drain current of MOS1 and MOS2 pair.

Figure V-4(a) presents the drain current local variability of n-MOS paired transistors of the nominal geometry, measured in the linear region. Note that the drain current deviation below threshold voltage exceeds 2 decades, making essential the use of the logarithm in Eq. V.7. The respective Y-parameter mismatch presented in Figure V-4(b) shows a similar trend.

Moreover, the drain current mismatch at high drain voltage is illustrated in Figures V-4(c) and (d) for a small and a large area device, respectively. As expected, according to Pelgrom's Law, the drain current mismatch is significantly lower in large area devices.

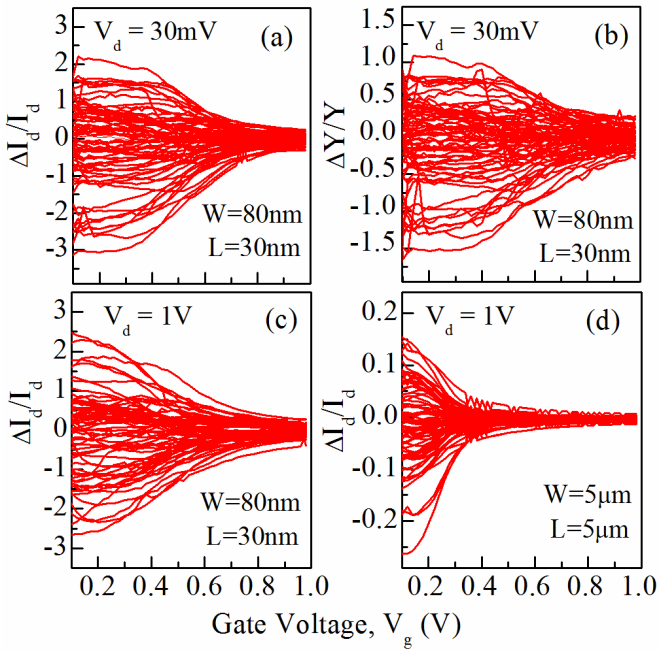


Figure V-4 Typical $\Delta I_d/I_d(V_g)$ (a) and $\Delta Y/Y(V_g)$ (b) curves in linear region for n-MOS devices with W = 0.08 µm and L = 0.03 µm. The corresponding $\Delta I_d/I_d(V_g)$ characteristics at saturation region for a small (c) but also for a large area device (d).

In Figures V-5(a) and (b), the normalized standard deviation of the drain current mismatch, $\sigma(\Delta I_d/I_d)$, is plotted as a function of the gate voltage, V_g for various geometries in the linear and saturation regions, respectively. Note that, at low drain voltage, there are clearly cases at strong inversion where an increase of $\sigma(\Delta I_d/I_d)$ with V_g is observed. This increase, which is not observed in all geometries, was attributed to SD series resistance variability in FDSOI devices [257]. Therefore, it appears that this phenomenon also exists in bulk devices. On the other hand, we observe that, for the same geometries, no such behavior is clearly observed in the saturation region (see Figure V-5(b)).

In order to verify our model, we used Eq. V.6 to fit the experimental data with 3 fitting parameters, the threshold voltage mismatch, $\sigma(\Delta V_t)$, the current gain factor mismatch, $\sigma(\Delta\beta/\beta)$ and the R_{sd} mismatch, $\sigma(\Delta R_{sd})$, in all operation regions. The value of R_{sd} was extracted with the Y-Function method using several gate lengths [56].

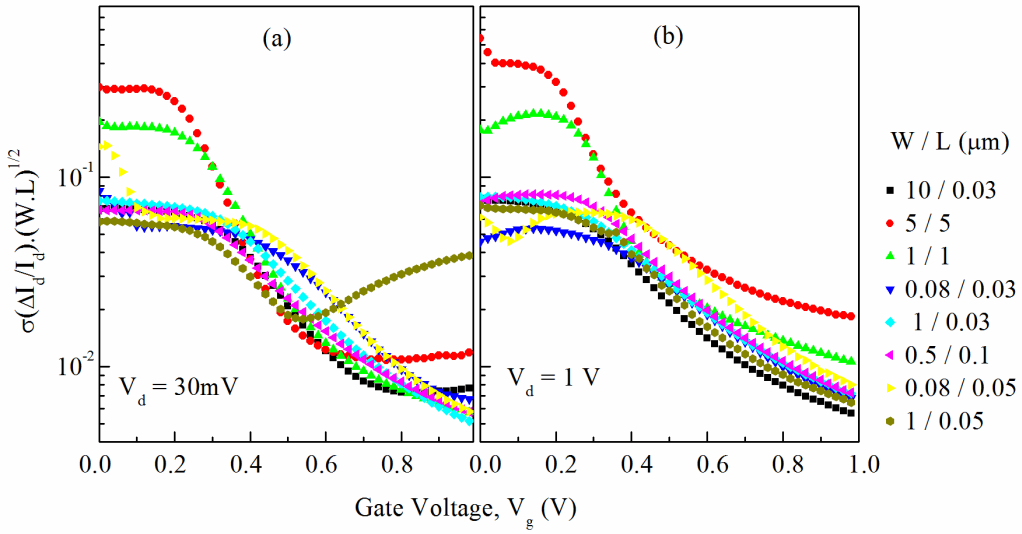


Figure V-5 Normalized standard deviation of the drain current mismatch versus gate voltage, V_g, for different geometries in linear (a) and saturation region (b).

The results are displayed in Figures V-6(a) and (b). Concerning the saturation region, we extracted values for $\sigma(\Delta V_t)$, $\sigma(\Delta\beta/\beta)$ and $\sigma(\Delta R_{sd})$, which are consistent with those extracted in the linear region. As shown in Figure V-6(b), we achieved good agreement between experimental and model results. This indicates that the influence of ΔR_{sd} can be significantly attenuated in the saturation region.

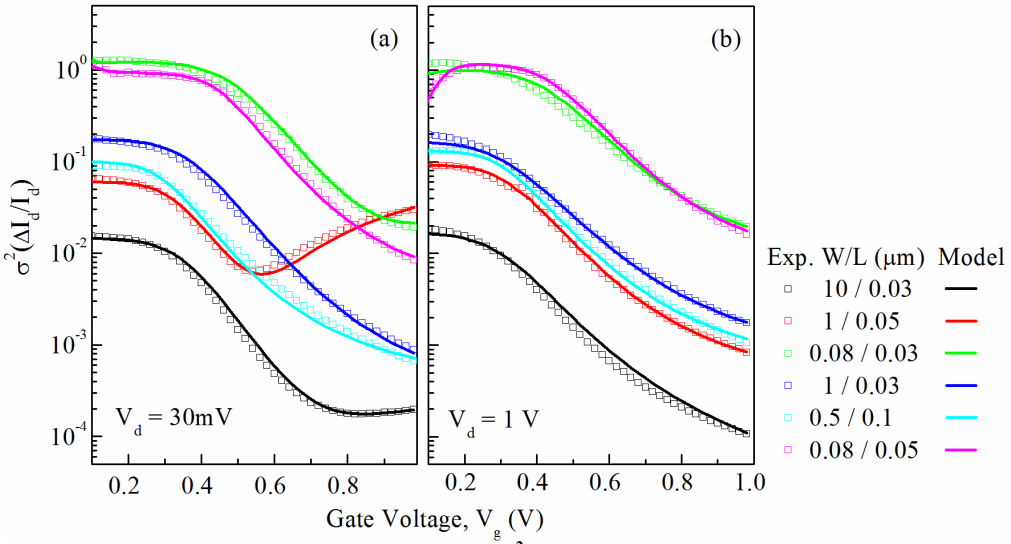


Figure V-6 Experimental results (symbols) of $\sigma^2(\Delta I_d/I_d)$ versus gate voltage, V_g, for small and large area devices in linear (a) and saturation (b) region and Model (lines).

This feature can be understood through the last term of Eq. V.6 which relates the drain current sensitivity with ΔR_{sd}, indicating that I_d is at least twice less sensitive to R_{sd} in the saturation region, where g_d is almost equal to 0 (see Figure V-7). This observation is confirmed in Figures V-8(a) and (b), where the individual matching parameter $iA_{\Delta Vg}(V_g)$ (Eq. V.8) is presented for various geometries in the linear and saturation regions, respectively.

$$iA_{\Delta Vg} = \left[\sigma\left(\frac{\Delta I_D}{I_D}\right) \Big/ \left(\frac{g_m}{I_D}\right)\right] \cdot \sqrt{W \cdot L} \qquad \textbf{Eq. V.8}$$

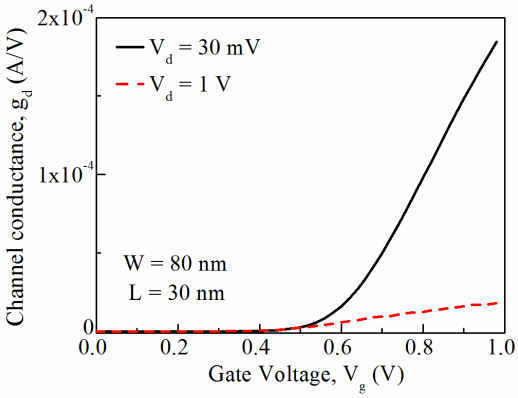


Figure V-7 Channel conductance, g_d as a function of the gate voltage, V_g, in linear (solid line) and saturation region (dashed line) calculated from the nominal device ($W = 0.08\ \mu m$ and $L = 0.03\ \mu m$).

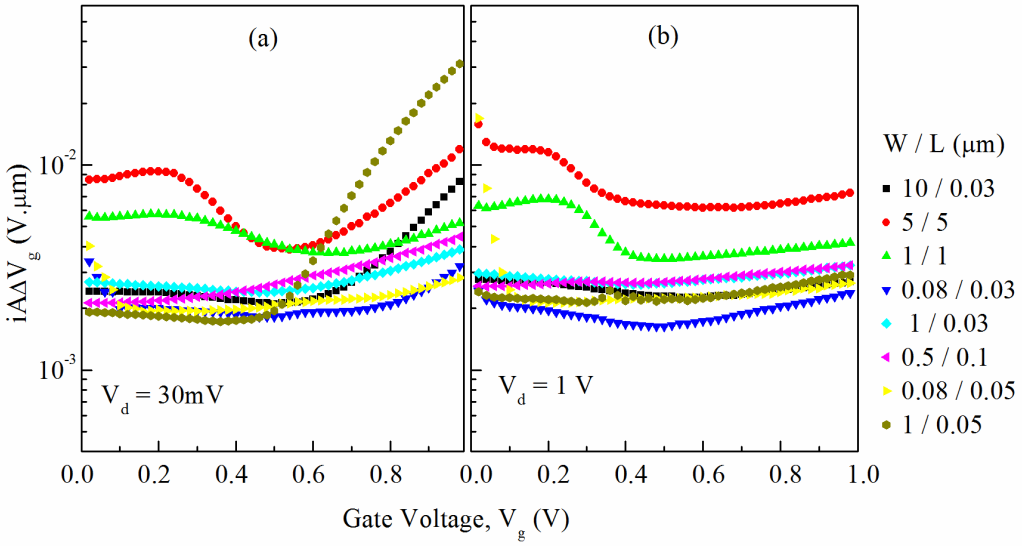


Figure V-8 Individual matching parameter $iA_{\Delta Vg}$ versus gate voltage, V_g extracted by experimental data in linear (a) and saturation region (b) for different geometries.

The plateau observed in Figure V-8 at low gate voltages nearly corresponds to the individual matching parameter $iA_{\Delta Vt}$ (Eq. V.9). Note that the abnormal behavior of $iA_{\Delta Vg}(V_g)$ observed at low gate voltages in long channel devices is due to the fact that the devices are pocket implanted [263].

$$iA_{\Delta Vt} = \sigma(\Delta V_t) \cdot \sqrt{W \cdot L} \qquad \textbf{Eq. V.9}$$

As we can see in more detail in Figure V-9, $\sigma(\Delta V_t)$ has almost the same value for both linear and saturation regions. The difference observed between the two regions at high V_g values is due to the $\sigma(\Delta R_{sd})$ difference, while the slight increase of $iA_{\Delta Vg}$ in strong inversion is due to $\sigma(\Delta\beta/\beta)$. From Fig. V-9, it is also clear that the parameter $iA_{\Delta Vg}$ is smaller at V_d=1V, since the impact of ΔR_{sd} on the drain current variability is less in the saturation region (Eq. V.6).

Figures V-10(a) and (b) present the individual matching parameters $iA_{\Delta Vt}$ and $iA_{\Delta\beta/\beta}$, respectively, as a function of the gate length (Equations V.9 and V.10).

$$iA_{\Delta\beta/\beta} = \sigma\left(\Delta\beta/\beta\right)\cdot\sqrt{W\cdot L} \qquad \textbf{Eq. V.10}$$

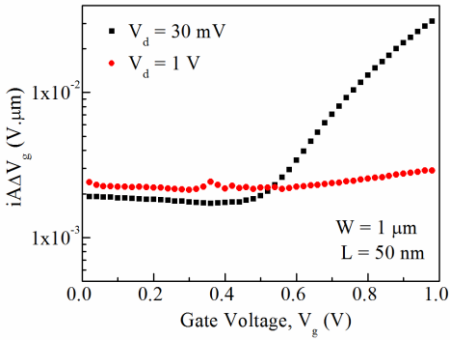
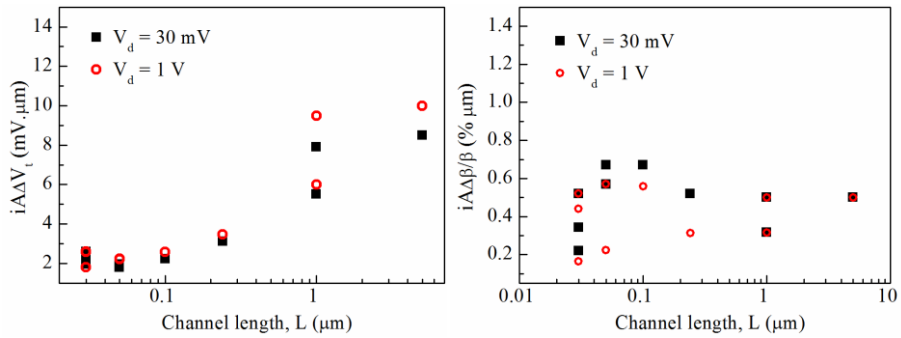


Figure V-9 Individual matching parameter, $iA_{\Delta Vg}$ versus gate voltage, V_g in linear (black symbols) and saturation region (red symbols) for an n-MOS with W = 1 µm and L = 0.05 µm.



(a) **(b)**

Figure V-10 $iA_{\Delta Vt}$ (a) and $iA_{\Delta\beta/\beta}$ (b) versus channel length, L in linear (black symbols) and saturation region (red symbols) for 28nm BULK nMOSFETs.

The values corresponding to the $iA_{\Delta Vt}$ parameter are ranging between 2 and 6.5 mV·µm, in agreement with [264], increasing slightly with the gate length. Moreover, $iA_{\Delta\beta/\beta}$ ranges from 0.4 to 0.6 %·µm, verifying that our fitting with including the gain factor mismatch is correct. Last but not least, the standard deviation of the SD series resistance mismatch versus the channel width is presented in Fig. V-11. As can be seen, the R_{sd} and the $\sigma(\Delta R_{sd})$ follow the same trend and more specifically their values decrease as the channel width increases. Furthermore, a dependence on the gate length is observed at fixed width. Finally, it was found that the normalized series resistance local variability, $\sigma(\Delta R_{sd})/R_{sd}$, is of the order of 5-20%, which is similar to FDSOI technologies [257].

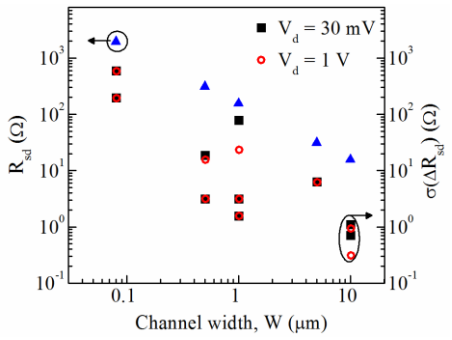


Figure V-11 Source – Drain, SD series resistance (blue symbols) and its mismatch both in linear (black symbols) and saturation region (red symbols) versus channel width, *W* for 28nm BULK n-MOSFETs.

V.3.2.2 Simulation Results

To further verify the findings presented above, numerical simulations of drain current mismatch characteristics were performed in both linear and saturation regions. In order to accurately reproduce the drain current local variability behavior, a MOSFET compact model based on Lambert W-function was used and is recalled below [265],

$$I_d(V_g,V_d)=\frac{\frac{W}{L}\int_0^{V_d}\mu_{eff}(V_g,U_c).Q_i(V_g,U_c).dU_c}{1+\frac{1}{L}\int_0^{V_d}\frac{\mu_{eff}(V_g,U_c)}{v_{sat}}.R(V_g,U_c).dU_c} \qquad \textbf{Eq. V.11}$$

where the inversion charge Q_i is given by,

$$Q_i(V_g,U_c)=C_{ox}n\frac{kT}{q}LW\left(e^{q.\frac{V_g-V_t-U_c}{nkT}}\right) \qquad \textbf{Eq. V.12}$$

with U_c being the quasi Fermi potential along the channel, C_{ox} being the gate oxide capacitance, kT/q the thermal voltage, n the subthreshold ideality factor and v_{sat} the saturation carrier velocity. The factor R is related to inversion capacitance and gate oxide capacitance as [265],

$$R(V_g,U_c)=\frac{C_{inv}}{C_{inv}+C_{ox}} \qquad \textbf{Eq. V.13}$$

where C_{inv} is the inversion charge capacitance. This factor allows to activate the saturation velocity effect in strong inversion ($R\approx 1$) and to cancel it in weak inversion ($R\approx 0$). The effective mobility μ_{eff} is related as usual to the inversion charge by the first order approximation,

$$\mu_{eff}=\frac{\mu_0}{1+\theta_1.(Q_i/C_{ox})} \qquad \textbf{Eq. V.14}$$

where μ_0 is the low field mobility and θ_1 is the first order mobility attenuation coefficient.

The effect of the SD series resistance has then been taken into account through the gate and drain voltage drops as

$$V_g=V_{g0}-\left(R_{sd}/2\right)\cdot I_d \quad \textbf{(a)}$$
$$V_d=V_{d0}-R_{sd}\cdot I_d \quad \textbf{(b)} \qquad \textbf{Eq. V.15}$$

with V_{g0} and V_{d0} being the intrinsic gate and drain to source voltages, respectively.

Then, based on the above MOSFET model, the standard deviation of the drain current variability has been calculated numerically using the sensitivity equation V.1 for I_d with respect to V_t, β and R_{sd} for any gate and drain voltage. Figure V-12 shows typical simulated variations of $\sigma(\Delta I_d/I_d)$ with V_g in the linear and saturation regions. It confirms that the ΔR_{sd} mismatch has a smaller impact on the drain current variability in the saturation region, thus verifying the experimental results behavior. This finding is also supported by the simulated individual matching parameter characteristics, $iA_{\Delta Vg}(V_g)$, which is also lower in saturation region (see Fig. V-13).

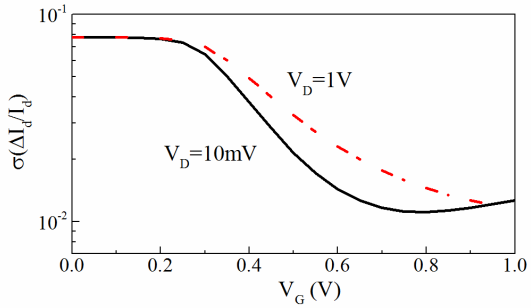


Figure V-12 Simulation results of $\sigma(\Delta I_d/I_d)$ versus gate voltage for n-MOS devices with channel length L =1 μm and channel width W = 1 μm for linear (solid line) and saturation (dashed line) regions.

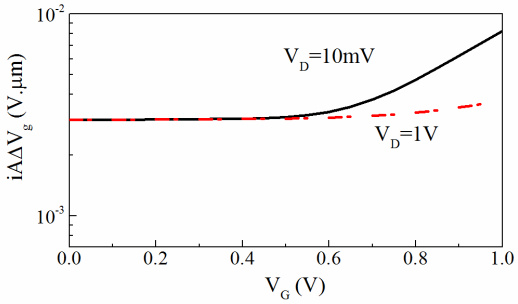


Figure V-13 Simulation results of parameter $iA_{\Delta Vg}$ versus gate voltage for n-MOS with channel length L = 1 μm and channel width W = 1 μm for linear (solid line) and saturation (dashed line) regions.

V.4 Drain Current Local Variability in linear region including all drain current mismatch sources

V.4.1 Drain current local variability model in linear region including all drain current mismatch sources

In the previous section, in order to build the drain current mismatch model of Eq. V.2, the partial derivatives of the drain current, I_d with respect to the threshold voltage V_t, the current gain factor β and the source-drain series resistance R_{sd} have been calculated. However, the sensitivity of the drain current to the MOSFET's subthreshold slope (SS) was not taken into account. Therefore, the need of a model including all the main sources of drain current local variability led us to the extension of Eq. V.2. This way, the drain current mismatch in linear region is obtained as

$$\sigma\left(\frac{\Delta I_d}{I_d}\right)^2 = \left(\frac{g_m}{I_d}\right)^2 .\sigma(\Delta V_t)^2 + (1 - G_d.R_{sd})^2.\sigma(\Delta\beta/\beta)^2 + \ldots$$
$$\ldots G_d^2.\sigma(\Delta R_{sd})^2 + \left[\ln\left(\frac{I_d}{I_{d,th}}\right)\right]^2\left[\exp\left(-\frac{I_{d,th}}{I_d}\right) - 1\right]^2.\frac{\sigma(\Delta n)^2}{n^2} \qquad \textbf{Eq. V.16}$$

where $I_{d,th}$ is a constant current near threshold and n is the ideality factor through which the SS variability is described, since

$$n = \frac{q}{k \cdot T \cdot SS} \qquad \textbf{Eq. V.17}$$

Consequently, this model relies on four matching parameters: $\sigma(\Delta V_t)$, $\sigma(\Delta\beta/\beta)$, $\sigma(\Delta R_{sd})$ and $\sigma(\Delta n)$.

Similarly, the Y-Function mismatch model described by Eq. V.3 has been also extended so as it includes all the main sources of drain current mismatch:

$$\sigma\left(\frac{\Delta Y}{Y}\right)^2 = \frac{\beta \cdot \sigma(\Delta V_t)^2}{4 \cdot \beta \cdot n^2 \cdot (kT/q)^2 + Y^2} + \frac{1}{4}.\sigma(\Delta\beta/\beta)^2 + \ldots$$
$$\ldots\left[\ln\left(\frac{I_d}{I_{d,th}}\right)\right]^2\left[\exp\left(-\frac{I_{d,th}}{I_d}\right) - 1\right]^2.\frac{\sigma(\Delta n)^2}{n^2} \qquad \textbf{Eq. V.18}$$

V.4.2 Drain current mismatch model validation in sub 15nm Si/SiGe Trigate MOSFETs

Tri-gate nanowire MOS transistors are nowadays recognized as promising architectures for continuing the scaling down beyond FinFET and FDSOI CMOS technologies [28], [29], [30]. High performance strained Si/SiGe Trigate NW p-MOSFETs, fabricated at CEA-LETI according to a process detailed in [266], were demonstrated down to 15nm gate length. In such advanced technologies, the device-to-device variability should become a critical issue, jeopardizing the functionality of analog and logic circuits like SRAM cells.

Both Si and SiGe(30%) channels made on SOI or SGOI substrates with 145 nm BOX were available. The NW features 12 nm film thickness and 2 nm EOT HfSiON gate dielectric with TiN metal gate. SiGe(30%) source-drain compressive stressors were added to enhance the strain in the device. The channel mask width W was varied from 30 nm up to 10 µm (effective width 20 nm smaller). The channel length L was ranging from 10 nm up to 1µm.

The $I_d(V_g)$ MOSFET transfer characteristics were recorded in linear region (V_d = $20mV$) at wafer level. The local variability was measured owing to paired MOS devices (MOS1 & MOS2) on a maximum number of dies up to 270.

V.4.2.1 Local Variability

Figures V-14(a) and (b) show typical statistical set of $I_d(V_g)$ curves obtained on Si and SiGe p-MOSFETs for MOS1 structure. Note the huge drain current variability below threshold (> 2 decades), which implies evaluating the drain current mismatch between pair using the log difference (Eq. V.7), instead of the linear. An example of $\Delta I_d/I_d(V_g)$ mismatch characteristics is shown in Figures V-14(c) and (d) for SiGe and Si p-MOSFETs.

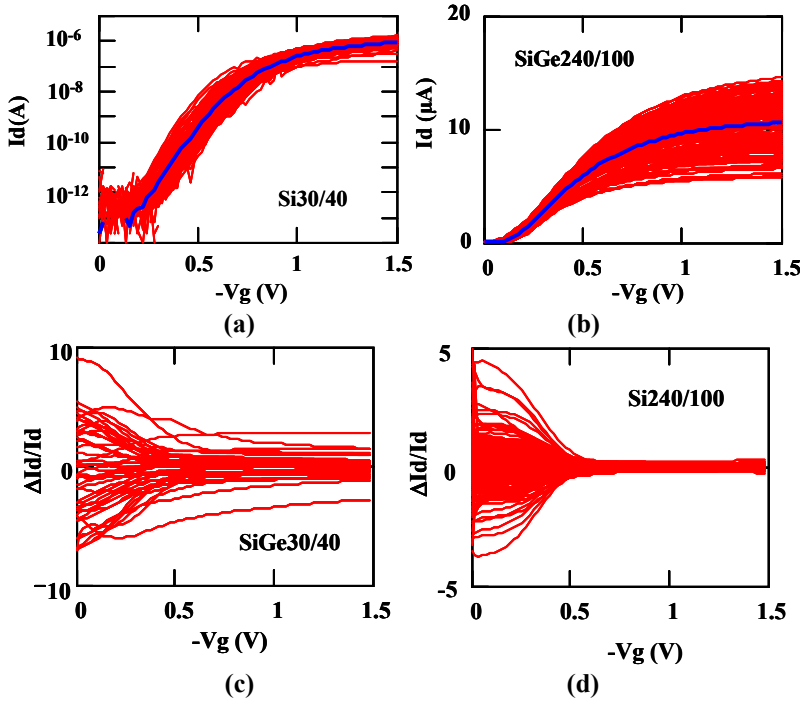


Figure V-14 Typical set of $I_d(V_g)$ and $\Delta I_d/I_d(V_g)$ curves for Si and SiGe pMOSFETs. Bold line shows mean value of $I_d(V_g)$ (W/L in nm).

The standard deviation of the associated drain current $\sigma(\Delta I_d/I_d)$ and Y-function $\sigma(\Delta Y/Y)$ mismatch are shown in Figure V-15 versus gate voltage (symbols). The best fit characteristics obtained with the mismatch models of Equations V.16 and V.18 are also reported in Figure V-15 (solid lines).

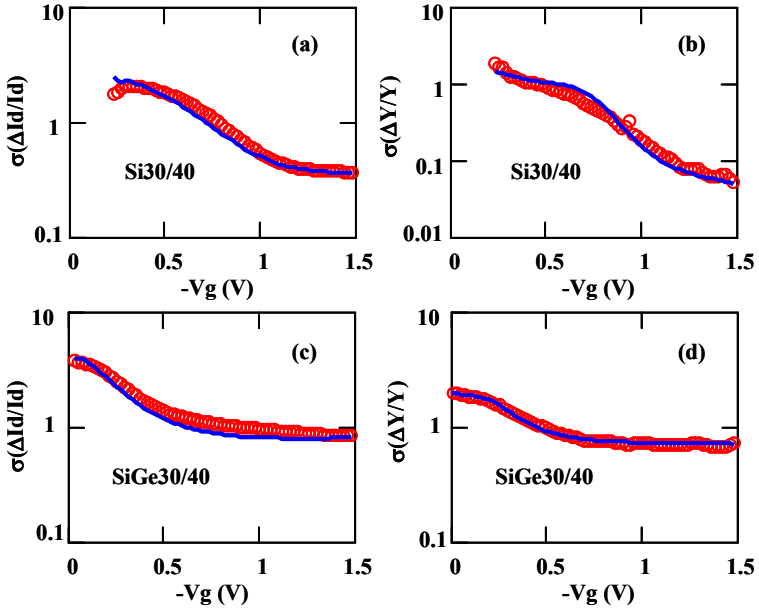


Figure V-15 Typical experimental (symbols) and modeled (solid lines) variations of $\sigma(\Delta I_d/I_d)$ (a,c) and $\sigma(\Delta Y/Y)$ (b,d) with V_g for local variabiliy in Si and SiGe p-MOSFETs (W=30 nm, L=40 nm).

The extracted normalized matching parameters are summarized in Table V-1 for two geometries. The $iA_{\Delta Vt}$ and $iA_{\Delta\beta/\beta}$ parameters were calculated by Equations V.9 and V.10. Except for SiGe30/40 devices, the matching parameters are typically 2-3 times larger than in state-of-the-art 14/28 FDSOI or 20/28 bulk technologies [259], which is quite reasonable for such very advanced devices with not yet optimized processes.

W/L (nm)	$iA_{\Delta Vt}$ (mV·µm)	$iA_{\Delta\beta/\beta}$ (%·µm)	$\sigma(\Delta R_{sd}/R_{sd})$	$\sigma(\Delta n/n)$
Si 240/100	2.2	1.6	10%	6%
Si 30/40	2.6	1.4	70%	11%
SiGe 240/100	2.4	1.4	30%	17%
SiGe 30/40	4.5	4.8	95%	20%

Table V-1 Matching parameters obtained from model fit for Si and SiGe NW p-MOSFETs.

A better comparison between matching results can be obtained by plotting the input referred normalized matching parameter $iA_{\Delta Vg}$ (Eq. V.8) and is shown in Fig. V-16. As has been already mentioned above, in these plots, the minimum values of $iA_{\Delta Vg}$ roughly correspond to $iA_{\Delta Vt}$, whereas the increase at strong inversion mainly stems from $\sigma(\Delta\beta/\beta)$ and $\sigma(\Delta R_{sd})$ contributions [257], [259]. Note the worse behavior of SiGe devices against Si p-MOSFETs as already pointed out in Table V-1.

Once the matching parameters have been extracted, the model (Eq. V.16) can also be used to evaluate the contributions of channel and SD series resistance to the total mismatch of the devices, *%CH* and *%SD*, respectively:

$$\%CH = \frac{\sigma(\Delta I_d/I_d)^2[\sigma(\Delta V_t),\sigma(\Delta\beta/\beta),\sigma(\Delta n/n),\sigma(\Delta R_{sd})=0]}{\sigma(\Delta I_d/I_d)^2[\sigma(\Delta V_t),\sigma(\Delta\beta/\beta),\sigma(\Delta n/n),\sigma(\Delta R_{sd})]} \quad \textbf{(a)} \qquad \textbf{Eq. V.19}$$

$$\%SD = 1 - \%CH \quad \textbf{(b)}$$

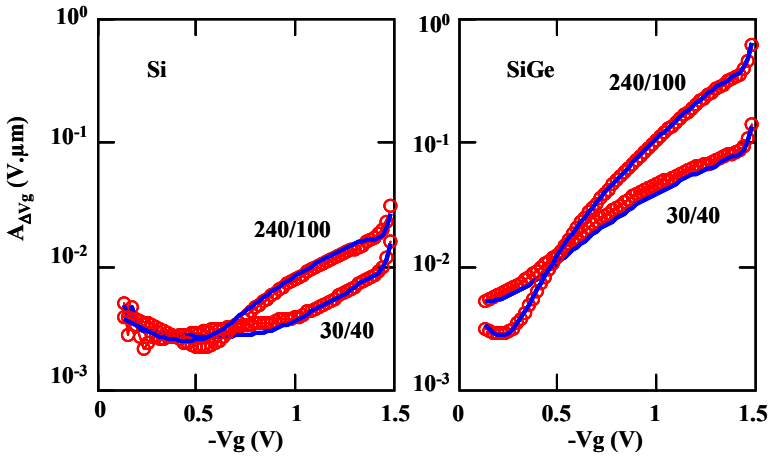


Figure V-16 Experimental (symbols) and modeled (solid lines) variations of $iA_{\Delta Vg}$ with V_g for Si and SiGe p-MOSFETs (W/L in nm).

Figure V-17 shows typical variations of *%CH* and *%SD* with V_g and indicates that SiGe devices suffer more SD contribution than Si p-MOSFETs.

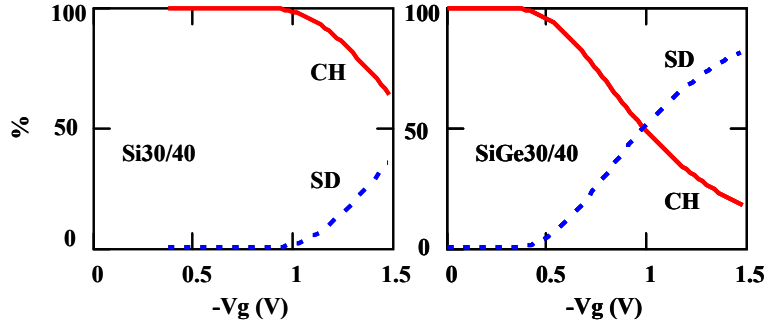


Figure V-17 Variations with V_g of channel (CH) and source-drain (SD) series resistance to total device mismatch percentage for Si and SiGe p-MOSFETs (W/L in nm).

V.4.2.2 Global Variability

The global variability of the drain current characteristics can also be studied with the same procedure. Indeed, in this case, the drain current mismatch is no longer evaluated between pair but between drain current values of devices from various dies all over the wafer and a reference value here chosen as the mean value, $I_{d,mean}$, for all dies. Indeed, the log difference

$$\Delta I_d / I_d = \ln\left(I_d / I_{d,mean} \right) \qquad \textbf{Eq. V.20}$$

corresponds now to the global variability of the drain current. As for mismatch (local variability), the standard deviation of the drain current global variability, $\sigma(\Delta I_d/I_d)$, can be calculated as well. Figure V-18 (symbols) shows typical global variability $\sigma(\Delta I_d/I_d(V_g)$ characteristics obtained on MOS1 structures for both Si and SiGe devices. A similar behavior with V_g as compared to the drain current local variability of Figure V-15 is observed.

Therefore, the matching model of Eq. V.16 can be used to fit the characteristics and, by turn, to extract the global variability parameters as for mismatch (Figure V-18, solid lines). Since the local variability can be regarded as a local noise source, for the sake of comparison,

the global variability of drain current has been normalized to the local variability such as $\sigma(\Delta I_d/I_d)_{Global}/\sigma(\Delta I_d/I_d)_{Local}$ and plotted versus V_g in Figure V-19.

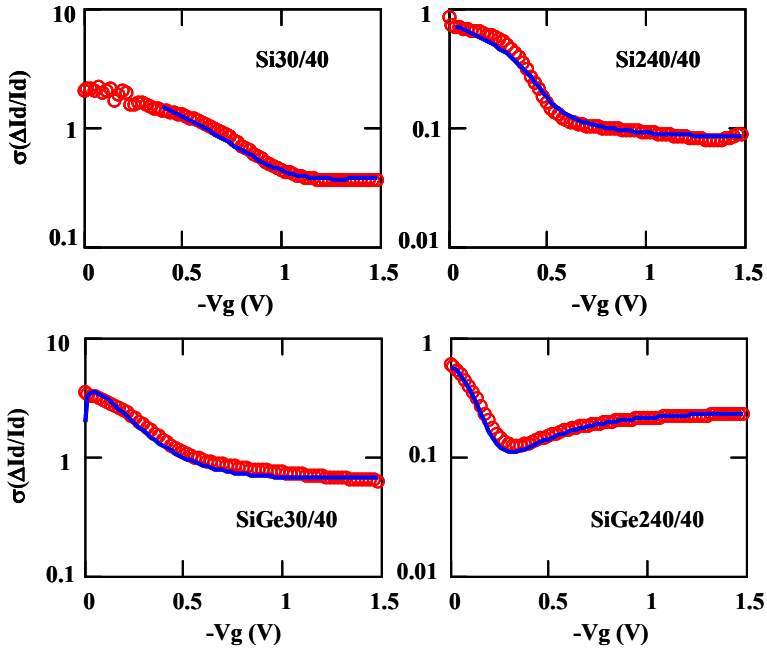


Figure V-18 Experimental (symbols) and modeled (solid lines) variations of $\sigma(\Delta I_d/I_d)$ with V_g for global variability in Si and SiGe p-MOSFETs (W/L in nm).

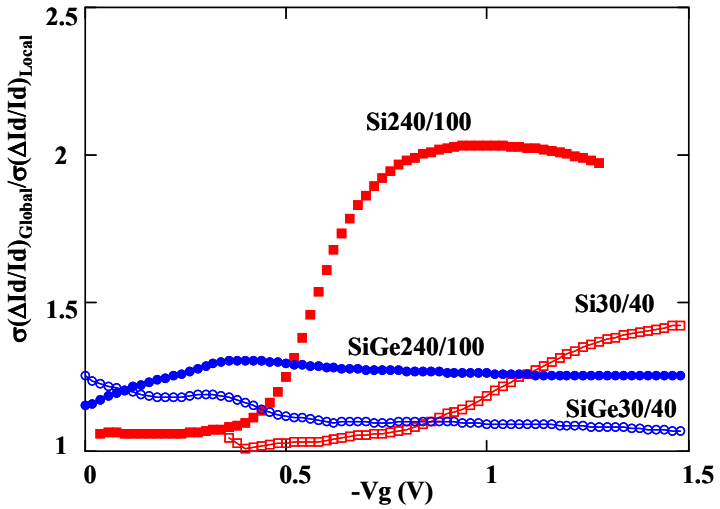


Figure V-19 Variation with V_g of global variability normalized by local variability (W/L in nm).

This figure indicates that, for SiGe devices, the global variability exceeds by 10 to 25% the local mismatch, whereas, for Si p-MOSFETs, the difference increases at strong inversion going up to a factor 1.5 to 2. This is in agreement with the extracted parameters used to fit the data of Figure V-18 where:

$$\sigma(\Delta V_t)_{Global} \approx \sigma(\Delta V_t)_{Local} \quad \textbf{(a)}$$

$$\sigma\left(\Delta\beta/\beta\right)_{Global} \approx 1.5\text{-}2\times\sigma\left(\Delta\beta/\beta\right)_{Local} \quad \textbf{(b)} \qquad \textbf{Eq. V.21}$$

$$\sigma(\Delta R_{sd})_{Global} \approx 1.3\text{-}1.8\times\sigma(\Delta R_{sd})_{Local} \quad \textbf{(c)}$$

Note also that the global variability increases with respect to the local variability in larger area devices. This is in agreement with the fact that the local mismatch scales as the reciprocal square root of device area, whereas the global mismatch is nearly constant with device area.

V.4.2.3 Monte Carlo modeling of drain current variability

The MOSFET compact model based on Lambert W function [86] analyzed in Chapter II and described by Equations II.26, II.21 and II.28 has been used to reproduce the variability characteristics of these NW Trigate devices. The mean value of the MOSFET parameters (V_t, μ_0, n and R_{sd}) have been extracted for various geometries from I_d-V_g mean curves, enabling very good fit of characteristics to be obtained as illustrated in Figure V-20. Then, based on the experimentally extracted matching parameters ($\sigma(\Delta V_t)$, $\sigma(\Delta\beta/\beta)$, $\sigma(\Delta R_{sd})$, $\sigma(\Delta n/n)$) reported in Table V-1, the individual MOSFET parameters were randomly generated by a Monte Carlo (MC) process using a normal or log-normal distribution and, by turn, employed for generating statistical set of $I_d(V_g)$ characteristics for each geometry. It should be noted that the log-normal distribution was used for huge variations of normalized β or R_{sd} parameters in order to avoid the onset of negative values in the random generation process.

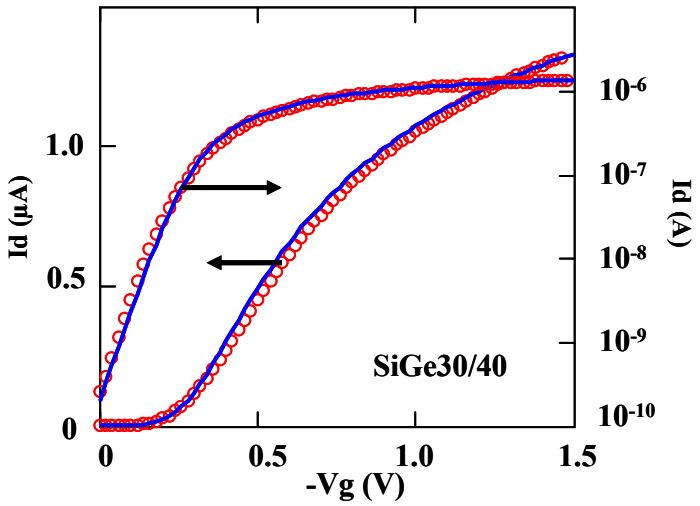


Figure V-20 Example of good correlation between experimental (symbols) and Lambert W function (solid lines) of I_d with V_g for SiGe pMOSFETs (W/L in nm).

Based on this model, the variations with gate voltage of $\Delta I_d/I_d$, $\Delta Y/Y$, $\sigma(\Delta I_d/I_d)$ and $\sigma(\Delta S/S)$ were simulated and compared to the experimental data (Figure V-21). As can be seen from Figures V-21(a) and (b), the mismatch characteristics of $\Delta I_d/I_d$ and $\Delta Y/Y$ are well reproduced by the Monte Carlo modeling. In addition, the standard deviation of drain current I_d and voltage gain S mismatch characteristics are also well described (Figures V-21(c) and (d)). The voltage gain is defined as

$$S = g_m / I_d \qquad \textbf{Eq. V.22}$$

It should be noted that, here, we put forward the voltage gain mismatch as being a quantity insensitive to β factor and mostly depending on threshold voltage, ideality factor and SD series resistance variability. Moreover, note that the features of $\sigma(\Delta S/S)$ with V_g can be well predicted by the MC compact modeling, emphasizing its physical soundness. However, no

close-formed analytical equation as V.16 or V.18 has been derived for $\sigma(\Delta S/S)$, justifying the usefulness of our MC compact modeling.

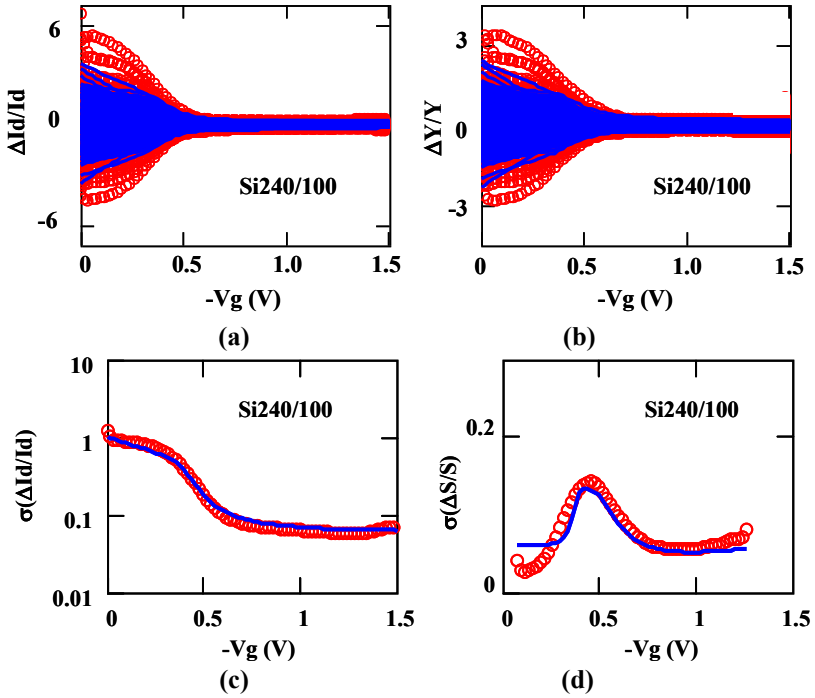


Figure V-21 Experimental (symbols) and modeled (solid lines) variations of $\Delta I_d/I_d$, $\Delta Y/Y$, $\sigma(\Delta I_d/I_d)$ and $\sigma(\Delta S/S)$ with V_g for local variability in Si p-MOSFETs (W/L in nm).

V.4.3 Drain current mismatch model validation in 14nm FinFETs

As already mentioned in Chapter I, Bulk Si FinFETs are very attractive devices for sub 22nm CMOS technologies as they are presenting several advantages against planar bulk MOSFETs [267], [268]. Indeed, they offer improved short channel behavior due to their ultra thin body structure and expected low variability due to their lightly-doped channel. Previous studies have reported good variability performance of FinFETs in terms of threshold voltage and current gain factor mismatch for Fin width down to 10nm both experimentally [269] and from simulation [270]. Nevertheless, in such advanced technologies, the local variability could become a critical issue for very narrow Fin subject to aggressive etching process, jeopardizing the functionality of analog and logic circuits like SRAMs.

The Si bulk FinFET devices under study have been fabricated at IMEC according to a process detailed in [271]. Self-aligned double patterned fins receive a dual interconnect process sequence. The gate stack consists of a 1.8 nm HfO_2 high-k dielectric completed by a dual work-function metal for n-MOS/p-MOS. The S/D of the devices is respectively built from Si:P and SiGe:B (≈70% Ge content) epitaxially regrown on recessed fins. The flow is concluded by a single layer of metallization and passivation. The Fin structure has a $W_{fin}=7$ *nm* width and a $H_{fin}=26$ *nm* height. The NMOS and PMOS devices under test have gate lengths varying between 28 nm and 34 nm and feature multi-fingers structures with number of fins N_{fin} ranging between 2 and 22 as depicted in Figure V-22.

The $I_d(V_g)$ MOSFET transfer characteristics were recorded in linear region ($V_d=50$ *mV*) at wafer level. The statistical analysis has been performed on at least 140 dies of paired

devices (MOS1 and MOS2) in order to ensure a good accuracy for the mean value (< 3%) and standard deviation (< 6%) estimations. Similarly to the previous analysis, the drain current mismatch was evaluated using the log difference (Eq. V.7).

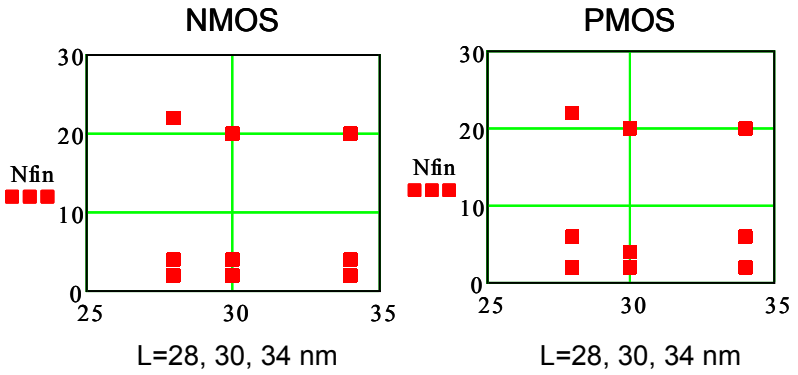


Figure V-22 Dimensions of tested FinFET devices: number of fins N_{fin} versus gate length L.

V.4.3.1 Local Variability

Figures V-23(a) and (b) show typical statistical set of $I_d(V_g)$ curves in linear and log scale obtained on n-MOS FinFETs for MOS1 structure. As in 28 nm Bulk MOSFETs and in Trigate FinFETs note again the huge drain current variability below threshold (> 3 decades), which implies evaluating the drain current mismatch between pair using the log difference (Eq. V.7). Examples of $\Delta I_d/I_d(V_g)$ and $\Delta Y/Y(V_g)$ mismatch characteristics are shown in Figure V-23(c) and (d) n-MOS FinFETs with $N_{fin}=2$ and $L=28\ nm$. Similar results were also obtained for p-MOS FinFETs.

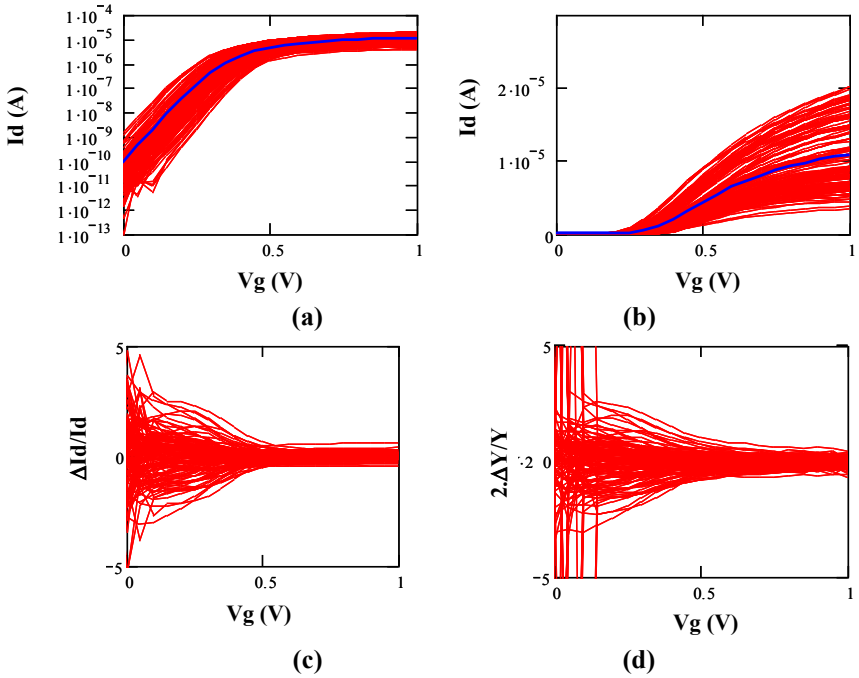


Figure V-23 Typical set of $I_d(V_g)$, $\Delta I_d/I_d(V_g)$ and $2\cdot\Delta Y/Y(V_g)$ curves for n-MOS FinFETs with $N_{fin}=2$ and L=28nm. Bold blue line shows the mean value of $I_d(V_g)$ characteristics.

The standard deviation of the associated drain current $\sigma(\Delta I_d/I_d)$ and Y-function $\sigma(\Delta Y/Y)$ mismatch were calculated from mismatch characteristics versus gate voltage are

shown in Figure V-24 (solid red lines). The best fit characteristics obtained with the mismatch models of Equations V.16 and V.18 are also reported in the same figure (dashed blue lines).

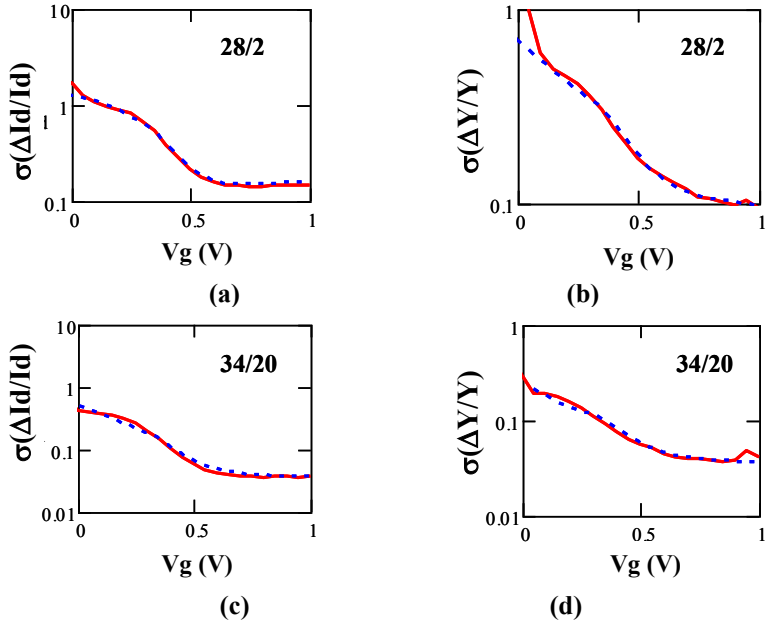


Figure V-24 Typical experimental (solid line) and modeled (dahsed line) variations of $\sigma(\Delta I_d/I_d)$ and $\sigma(\Delta Y/Y)$ with V_g for local variabiliy in n-MOS FinFETs with L=28 nm/N_{fin}=2 ((a)-(b)) and L=34 nm/N_{fin}=20 ((c)-(d)).

The extracted area normalized matching parameters, $iA_{\Delta Vt}$ and $iA_{\Delta\beta/\beta}$ have also calculated from Equations V.9 and V.10 respectively and are plotted as a function of area in Figure V-25 for n and p-MOS FinFETs.

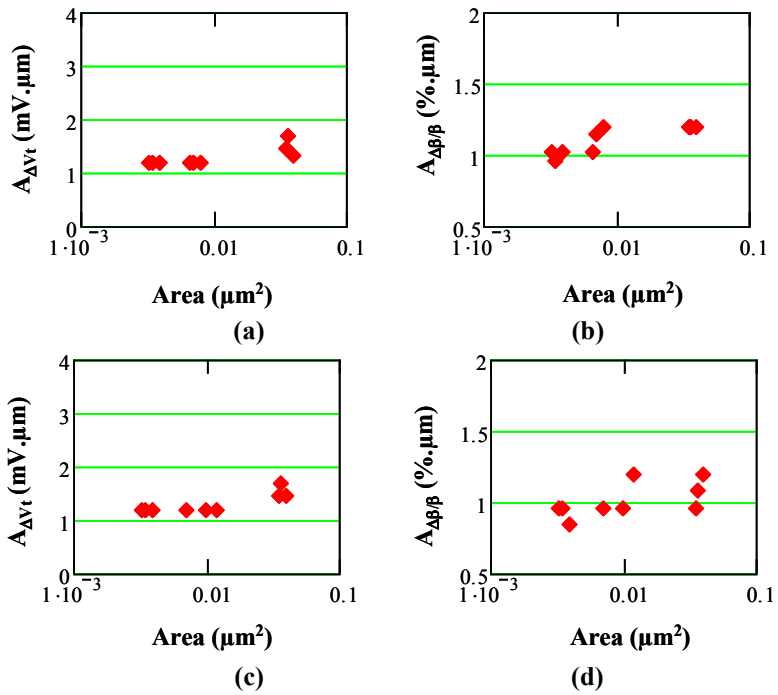


Figure V-25 Variations of normalized matching parameters $iA_{\Delta Vt}$ and $iA_{\Delta\beta/\beta}$ with device area for n ((a)-(b)) and p ((c)-(d)) MOS FinFETs.

Note that the threshold voltage matching parameter, $iA_{\Delta Vt}$, is ranging between 1.2 mV·µm to 1.7mV·µm for both n and p MOS FinFETs, which constitutes state-of-the-art values for such advanced devices, especially for the smallest ones. The gain factor matching parameter, $iA_{\Delta\beta/\beta}$, is also taking very good values around 1%·µm, which is quite remarkable for such ultra thin body, underlining the very good etching process of the Fin fabrication. It should also be noted that these matching parameters compare very well to 14/28 nm FDSOI planar results [259].

The SD access resistance mean value R_{sd} and standard deviation $\sigma(\Delta R_{sd})$ are plotted in Figure V-26 versus effective device width W_{eff}, calculated as,

$$W_{eff} = 2 \cdot H_{fin} + W_{fin} \qquad \textbf{Eq. V.23}$$

Note that, as already found for 14/28 FDSOI devices [259], they nearly scale as $1/W_{eff}$ and that $\sigma(\Delta R_{sd})/R_{sd}$ is almost constant around ≈10-15%.

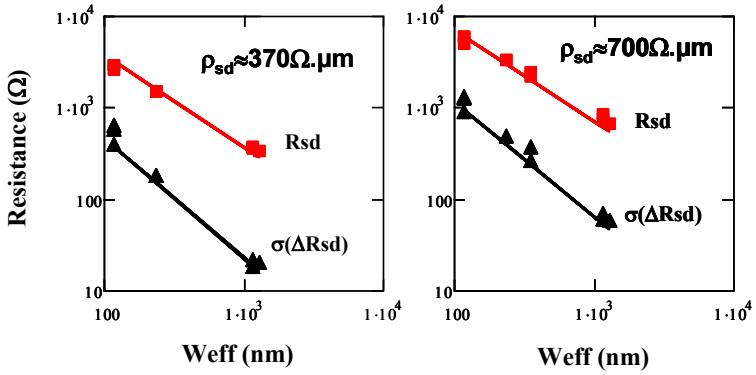


Figure V-26 Variations of R_{sd} and $\sigma(\Delta R_{sd})$ with device effective width W_{eff} for n (left) and p (right) MOS FinFETs.

Once the matching parameters have been extracted, the drain current mismatch model (Eq. V.16) has also been used to evaluate the contributions of channel and SD series resistance to the total mismatch of the devices, %CH and %SD, respectively, as already done in trigate nanowires. Figure V-27 shows typical variations of %CH (Eq. V.19(a)) and %SD (Eq. V.19(b)) with gate voltage and indicates that the SD contribution increases significantly above threshold, especially for the smallest device ($L=28nm/N_{fin}=2$), whereas the channel contribution dominates below threshold as expected.

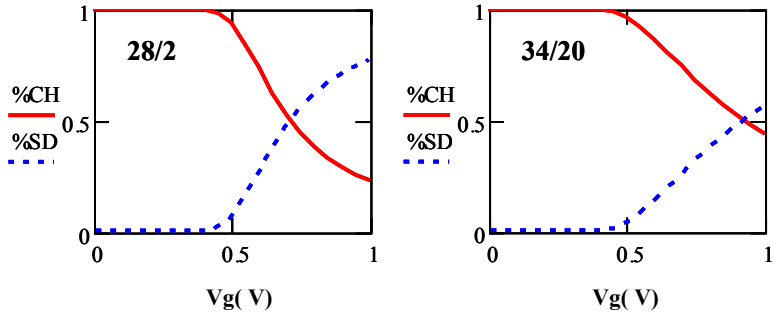


Figure V-27 Variations with V_g of channel (CH) and source-drain (SD) series resistance to total device mismatch percentage for n-MOS FinFETs with L=28 nm/N_{fin}=2 (left) and L=34 nm/N_{fin}=20.

V.4.3.2 Global Variability

The global variability of the drain current characteristics of these bulk FinFETs can also be handled with the same procedure. By applying the same methodology explained in the previous section, the drain current global variability and its' standard deviation have been calculated. Figure V-28 (solid red line) shows typical global variability $\sigma(\Delta I_d/I_d)(V_g)$ and $\sigma(\Delta Y/Y)(V_g)$ characteristics obtained on nMOS1 structures for 2 geometries. Again, as in the case of trigate nanowires, a similar behavior with gate voltage as compared to the drain current and Y-function local variability of Figure V-24 is observed. Therefore, the matching model of Eq. V.16 has also been used to fit the characteristics and, in turn, to extract the global variability parameters as for mismatch (Figure V-28, dashed blue lines).

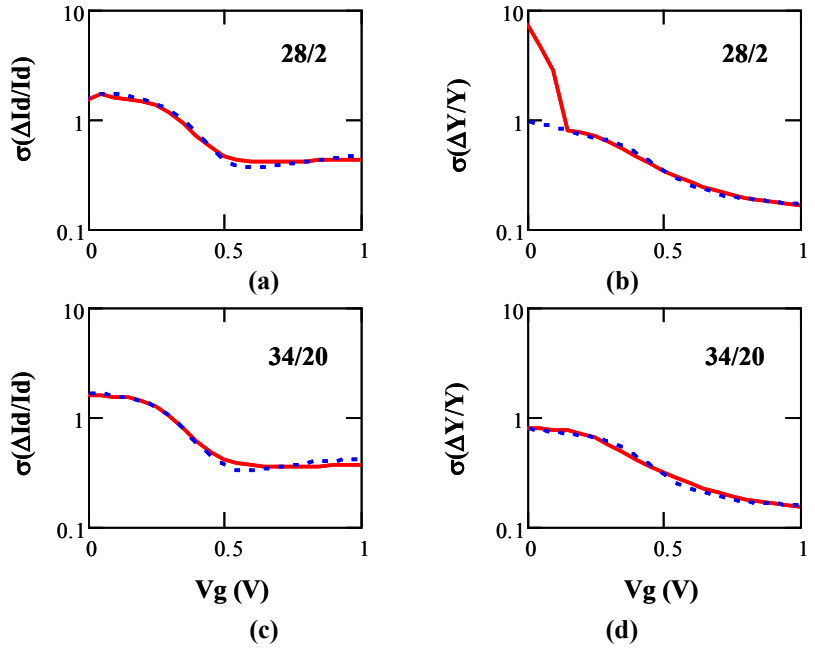


Figure V-28 Experimental (solid red line) and modeled (dashed blue line) variations of $\sigma(\Delta I_d/I_d)$ and $\sigma(\Delta Y/Y)$ with V_g for global variability in n-MOS FinFETs with L=28nm/N_{fin}=2 (top) and L=34nm/N_{fin}=20 ((c)-(d))

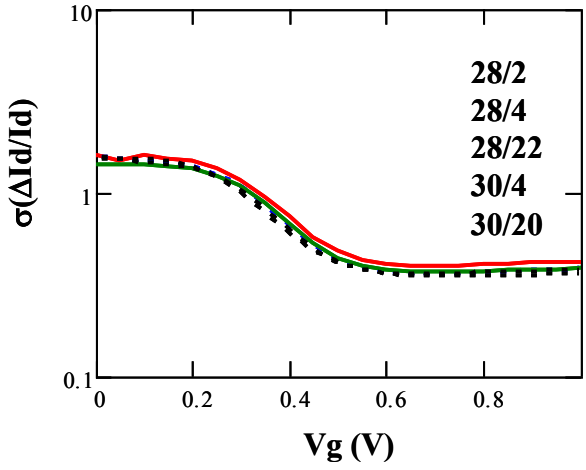


Figure V-29 Variations of $\sigma(\Delta I_d/I_d)$ with V_g for the global variability in n-MOS FinFETs for all studied geometries.

The global variability parameters used to fit all the data have been found nearly independent of device area investigated here:

$$\sigma\left(\Delta V_t\right)_{Global} \approx 40mV \quad \textbf{(a)}$$
$$\sigma\left(\Delta n/n\right)_{Global} \approx 15\%$$
$$\sigma\left(\Delta\beta/\beta\right)_{Global} \approx 30\% \quad \textbf{(b)} \qquad \textbf{Eq. V.24}$$
$$\sigma\left(\Delta R_{sd}\right)_{Global} \cdot W_{eff} \approx 240\Omega \cdot \mu m \quad \textbf{(c)}$$

This feature is in agreement with the fact that the local mismatch scales as the reciprocal square root of device area, whereas the global mismatch is nearly constant with device area as confirmed in Figure V-29 where the drain current global variability characteristics are represented for all the geometries.

V.4.3.3 Monte Carlo modeling of drain current variability

In order to further validate the drain current local variability model, a Monte Carlo process was applied as described in details in V.4.2.3. Indeed, using the MOSFET compact model based on Lambert W function [86], the variability characteristics of these FinFET devices were reproduced. The mean value of the MOSFET parameters (V_t, μ_0, n and R_{sd}) have been extracted for various geometries from I_d-V_g mean curves, enabling very good fit of characteristics to be obtained as illustrated in Figure V-30. Then, based on the experimentally extracted matching parameters ($\sigma(\Delta V_t)$, $\sigma(\Delta\beta/\beta)$, $\sigma(\Delta R_{sd})$ and $\sigma(\Delta n/n)$) reported in Figures V-25 and V-26, the individual MOSFET parameters were randomly generated by a Monte Carlo process using a normal or log-normal distribution and, in turn, employed for generating statistical set of $I_d(V_g)$ characteristics for each geometry.

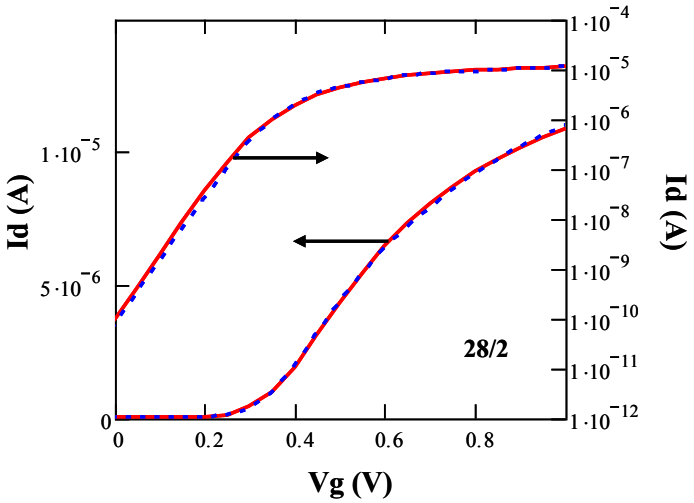


Figure V-30 Experimental (solid red lines) and modeled (dashed blue lines) variation of the drain current, I_d with the gate voltage, V_g for an n-MOS FinFET with L=28nm/N_{fin}=2.

Using this model, the variations with gate voltage of $\Delta I_d/I_d$, $\Delta Y/Y$, $\sigma(\Delta I_d/I_d)$ and $\sigma(\Delta S/S)$ were simulated and compared to the experimental data (Figure V-31). As can be seen from Figures V-31(a) and (b), the mismatch characteristics of $\Delta I_d/I_d$ and $\Delta Y/Y$ are well reproduced by the Monte Carlo modeling. Moreover, the standard deviation of drain current I_d and the voltage gain S (Eq. V.22) mismatch characteristics are also well simulated (Figures V-31(c) and (d)).

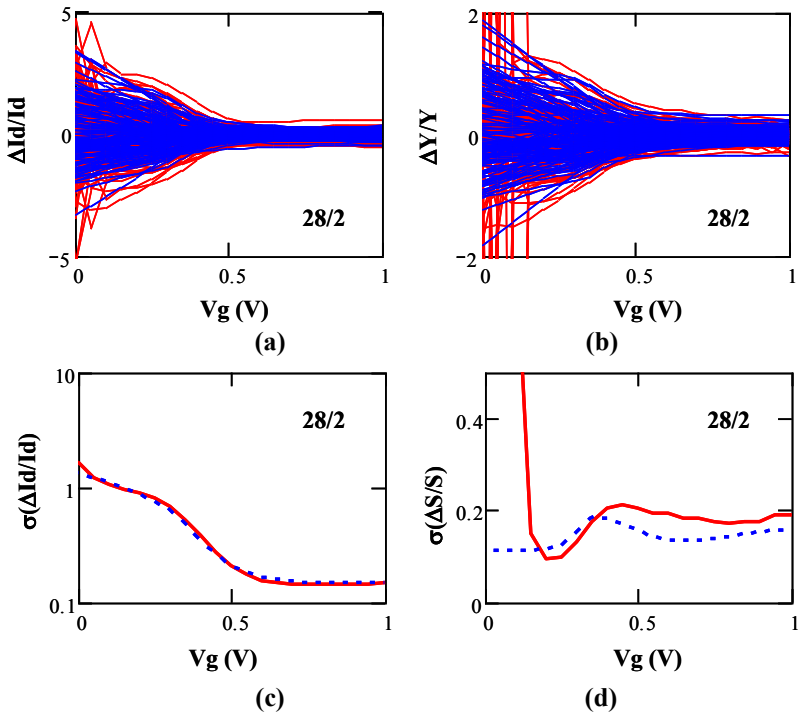


Figure V-31 Experimental (solid red lines) and MC modeled (solid blue lines) variations of $\Delta I_d/I_d$, $\Delta Y/Y$, $\sigma(\Delta I_d/I_d)$ and $\sigma(\Delta S/S)$ with V_g for local variability in n-MOS FinFETs with L=28nm/N_{fin}=2.

V.5 All operation region Drain Current Local Variability

After having verified in linear region the validity of the drain current local variability model including all the main sources of drain current mismatch (Eq. V.16), it was considered necessary to extend this model to all operation regions. Indeed, combining the models described by Equations V.6 and V.16, a universal mismatch model was developed, valid in all operation regimes and including all main sources of drain current local variability -assumed to be uncorrelated- namely the threshold voltage, $\sigma(\Delta V_t)$, the current gain factor, $\sigma(\Delta\beta/\beta)$, the source-drain (SD) series resistance, $\sigma(\Delta R_{sd})$ and the subthreshold slope (*SS*) ideality factor, $\sigma(\Delta n/n)$ mismatches and is given by:

$$\sigma^2\left(\frac{\Delta I_d}{I_d}\right)=\left(g_m/I_d\right)^2\cdot\sigma^2(\Delta V_t)+\left[1-\left(\frac{g_m}{2}+g_d\right)\cdot R_{sd}\right]^2\cdot\sigma^2\left(\Delta\beta/\beta\right)+$$
$$+\left(\frac{g_m}{2}+g_d\right)^2\cdot\sigma^2(\Delta R_{sd})+\left[\ln\left(\frac{I_d}{I_{d,th}}\right)\right]^2\cdot\left[\exp\left(\frac{-I_{d,th}}{I_d}\right)-1\right]^2\cdot\sigma^2\left(\Delta n/n\right) \qquad \textbf{Eq. V.25}$$

It should be noted that this model goes beyond Croon's model [251] as it includes the series resistance mismatch, and beyond Magnone's [255], which was limited in the subthreshold region. Moreover, unlike Croon's and Magnone's studies, our modeling approach is extended to the non-linear operation, therefore providing drain current mismatch as a function of both gate and drain voltages from weak to strong inversion.

V.5.1 Drain current mismatch model validation in 14nm FDSOI MOSFETs

In order to confirm the proposed model (Eq. V.25) an advanced FDSOI CMOS technology [85] was employed. The devices measured in this work are n-MOS transistors fabricated by ST Microelectronics in France. The channel lengths (L) and widths (W) are lying in the range of 0.02 to 0.35 µm, and 0.06 to 0.3 µm, respectively. The mid-gap metal gate/high k dielectric front gate stack features a 1.2 nm equivalent oxide thickness (EOT) while the undoped silicon channel thickness is $t_{si} = 6\ nm$ and the buried oxide (BOX) thickness is $t_{BOX} = 20\ nm$.

Static drain current measurements as a function of drain voltage were performed on an ensemble of 90 pairs of identical MOS transistors distributed over the 300mm wafer.

V.5.1.1 Local Variability

Figure V-32 presents typical $I_d(V_g)$ and $I_d(V_d)$ characteristics for different polarizations, revealing the variability over full wafer for the nominal device ($W = 0.06\ \mu m$ and $L = 0.02\ \mu m$).

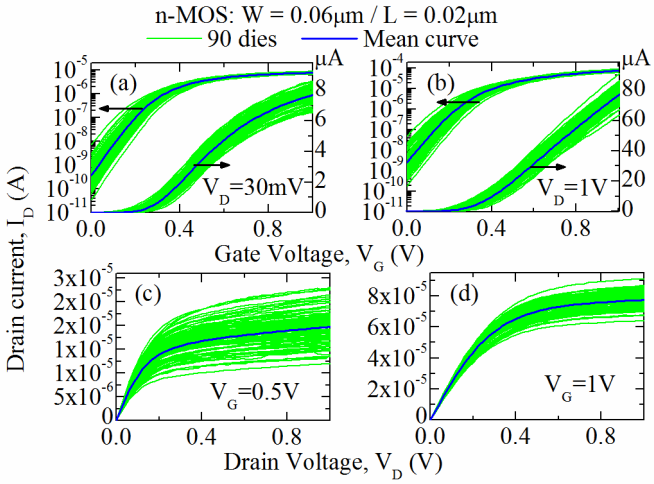


Figure V-32 Experimental input, $I_d(V_g)$ (a, b) and output, $I_d(V_d)$ (c, d) characteristics and their mean value for different polarizations.

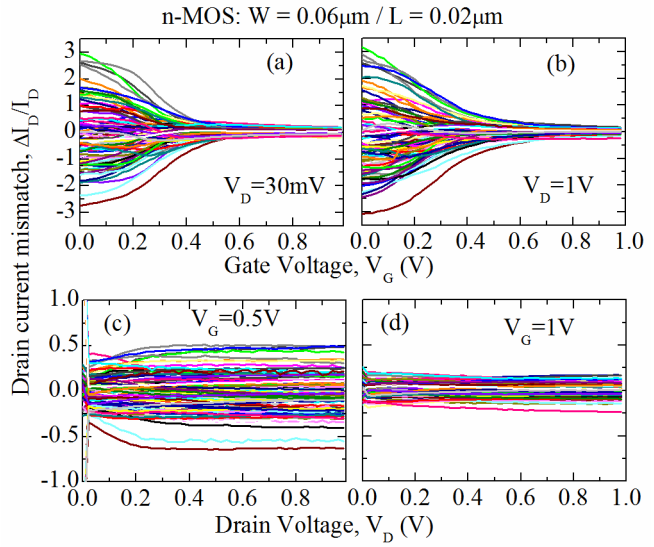


Figure V-33 $\Delta I_d/I_d$ curves versus gate (a, b) and drain (c, d) voltage for different polarizations.

The corresponding drain current mismatch, $\Delta I_d/I_d(V_g)$ and $\Delta I_d/I_d(V_d)$ is then calculated using the logarithmic difference of the drain currents, I_{d1} and I_{d2} (Eq. V.7) [257] and the results are illustrated in Figure V-33.

To quantify drain current variations, we calculated the standard deviation of its mismatch, $\sigma(\Delta I_d/I_d)$, normalized by $(W{\cdot}L)^{1/2}$ [42]. In Figure V-34, the normalized standard deviation of the drain current mismatch as a function of gate voltage is presented for various small and large area devices operating at linear region ($V_d = 30\ mV$). As can be seen in Figure V-35(a), the dependence of $\sigma(\Delta I_d/I_d)$ on the gate voltage is changing from linear ($V_d = 30\ mV$) to saturation ($V_d = 1\ V$) region and the dependence on drain voltage is also affected from moderate ($V_g = 0.5\ V$) to strong ($V_g = 1\ V$) inversion (see Figure V-35(b)).

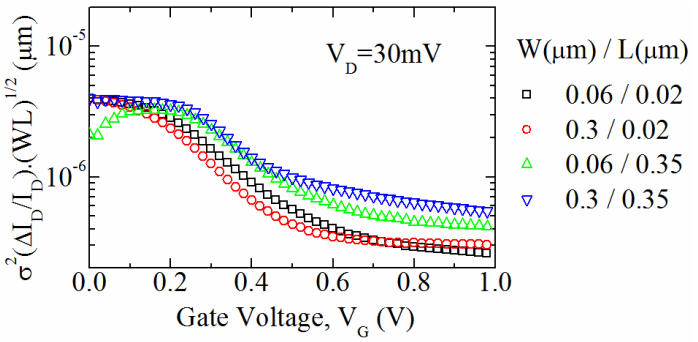


Figure V-34 Normalized standard deviation of the drain current mismatch versus gate voltage.

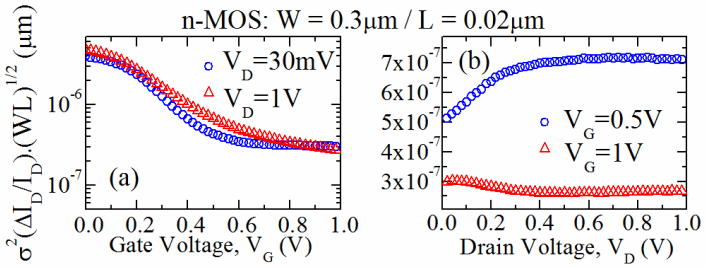


Figure V-35 Normalized drain current mismatch variance versus gate (a) and drain (b) voltage.

In order to capture this behavior the universal drain current mismatch model of Eq. V.25 was used. In fact, using 4 fitting parameters ($\sigma(\Delta V_t)$, $\sigma(\Delta\beta/\beta)$, $\sigma(\Delta R_{sd})$ and $\sigma(\Delta n/n)$), and the Levenberg-Marquardt algorithm, the experimental data were fitted in all operation regimes. As illustrated in Figure V-36, a very good agreement between experimental and model results was achieved for all cases.

Afterwards, the gate input referred normalized matching parameter $iA_{\Delta Vg}$ (Eq. V.8) that can probe the current mismatch variations in a more insightful way was calculated for all cases. In Figure V-37, the dependence of $iA_{\Delta Vg}$ with gate and drain voltage is presented. Indeed, as was already explained in section V.3.1, it appears that the influence of ΔR_{sd} is attenuated in saturation region. In Figure V-38, $iA_{\Delta Vg}$ is plotted versus I_d/g_m for all the different polarizations, revealing a common curve whatever the bias conditions, similarly to the gate input referred noise S_{Vg} behavior in MOSFETs [197]. As in the S_{Vg} analysis, where the dependence of S_{Vg} on I_d/g_m is related to the mobility fluctuations impact, the slope of the plot $iA_{\Delta Vg}$ versus I_d/g_m mainly depends according to Eq. V.25, on the individual matching parameter $iA_{\Delta\beta/\beta}$ and $iA_{\Delta Rsd}$, whereas the intercept with the vertical axis is directly related to $iA_{\Delta Vt}$.

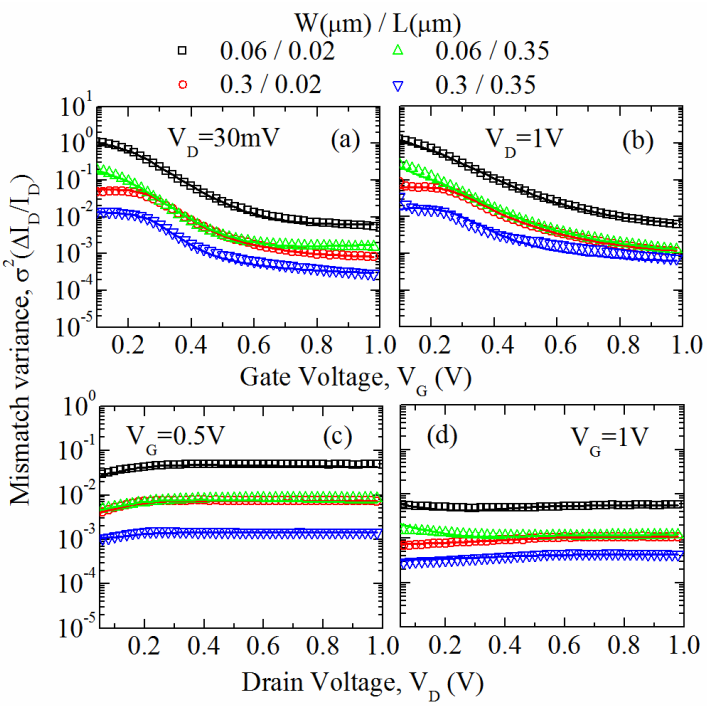


Figure V-36 Experimental results (symbols) and model (lines) of $\sigma^2(\Delta I_d/I_d)$ versus gate (a, b) and drain (c, d) voltage.

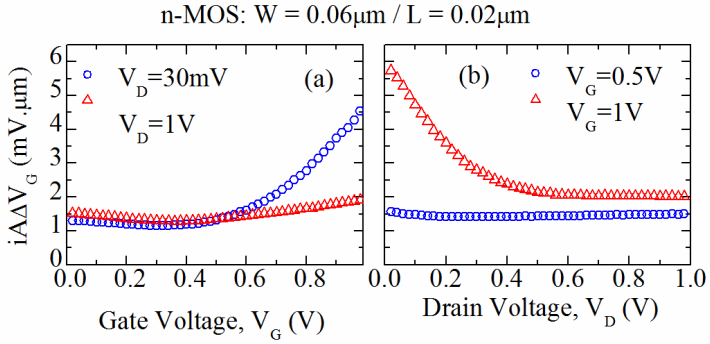


Figure V-37 Individual matching parameter, $iA_{\Delta Vg}$ versus gate (a) and drain (b) voltage.

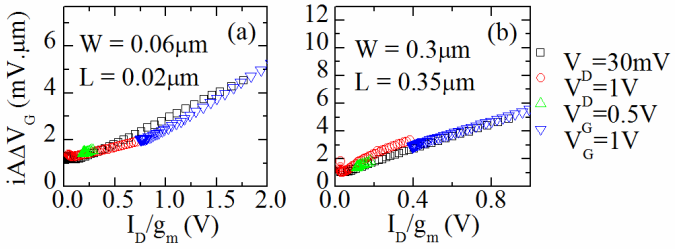


Figure V-38 Individual matching parameter, $iA_{\Delta Vg}$ versus I_d/g_m for a small (a) and a large (b) area device.

We can thus extract $iA_{\Delta Vt}$ and an effective $iA_{\Delta\beta/\beta}$* (including β and R_{sd} fluctuations) for various channel geometries using linear fit on the data of Figure V-39. As a result, although the trend is the same, there is a small deviation between the values extracted from matching model (Eq. V.25) and those obtained using the above methodology, as illustrated in Figures V-40 and V-41, reflecting for some geometries the extra contribution of R_{sd} variations to $iA_{\Delta\beta/\beta}$*.

Therefore, this $iA_{\Delta Vg}^2$ vs $(I_d/g_m)^2$ extraction method can only be regarded as a simple procedure to get a first approximate of the main matching parameters i.e. $iA_{\Delta Vt}$ and $iA_{\Delta\beta/\beta}$, useful for characterization purpose.

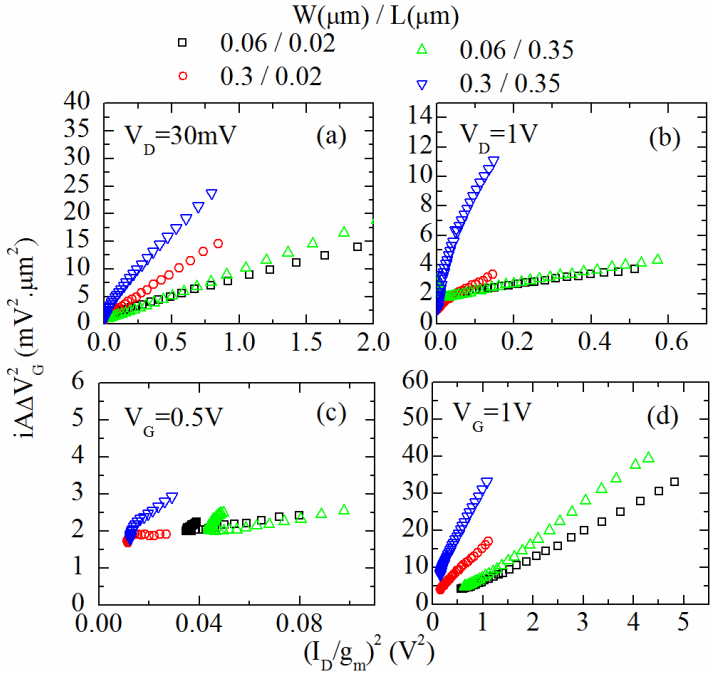


Figure V-39 Individual matching parameter, $iA_{\Delta Vg}^2$ versus $(I_d/g_m)^2$ extracted by experimental input (a, b) and output (c, d) characteristics for different geometries.

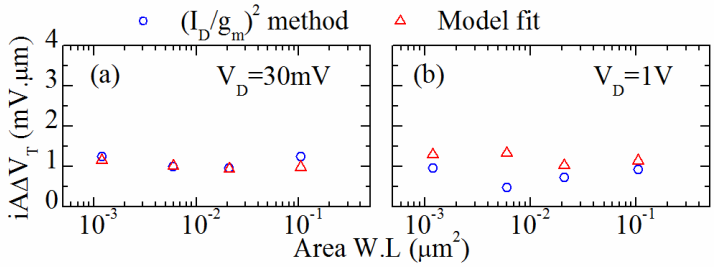


Figure V-40 Extracted values of $iA_{\Delta Vt}$ versus area (W·L) from the model (red symbols) and from Figure V-39 characteristics (blue symbols).

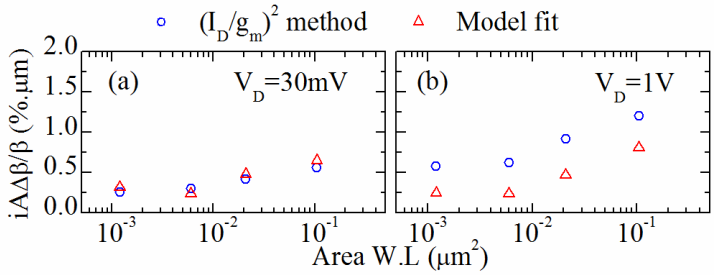


Figure V-41 Extracted values of $iA_{\Delta\beta/\beta}$ (red symbols) and $iA_{\Delta\beta/\beta^*}$ (blue symbols) versus area (W·L).

In Figure V-42, the values of $iA_{\Delta Vt}$ (Eq. V.9) and $iA_{\Delta\beta/\beta}$ (Eq. V.10) extracted from the matching model (Eq. V.25) for all cases are presented as a function of the device area.

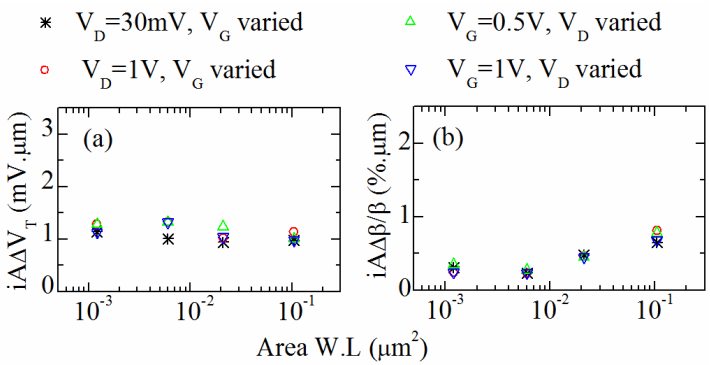


Figure V-42 Extracted values of $iA_{\Delta Vt}$ and $iA_{\Delta\beta/\beta}$ by input and output experimental data versus area (W·L) for 14nm FDSOI devices.

In Figures V-43(a) and (b), we present the standard deviations of the ideality factor and the SD series resistance as a function of the gate area and the channel width, respectively. As can be seen from Figure V-43(a), the ideality factor as well as its mismatch, are almost constant with the device area. Moreover, as presented in Figure V-43(b), R_{sd} and $\sigma(\Delta R_{sd})$ follow overall the same trend and more specifically their values decrease as the channel width increases with some insignificant variation with gate length at fixed gate width. Additionally, the ideality factor and series resistance mismatch parameters for both cases were calculated and $iA_{\Delta n/n}$ was found to be around 0.2 to 0.6 %·µm while $\sigma(\Delta R_{sd})/R_{sd}$ around 1-10%. Finally, from Figures V-42 and V-43 it is clear that almost the same values were extracted for all bias combinations, verifying the validity and the universality of the model.

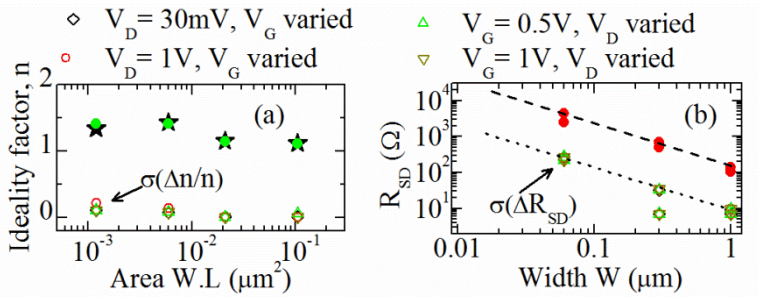


Figure V-43 Subthreshold slope ideality factor versus area (W·L) (a) and SD series resistance versus width (b). Their corresponding standard deviation is plotted with open symbols.

V.5.1.2 Monte Carlo modeling of drain current variability

To further verify the findings presented above, Monte Carlo simulations of drain current mismatch characteristics in all modes of operation were applied. For this purpose, the compact model of Eq. V.26, valid in all operation regions, was used. Indeed, the MOSFET drain current compact model based on the Lambert-W function [86] that was described in Chapter II, was successfully extended in all operation regimes. The extended model is presented in the following Equations V.26-V.30:

$$I_d = \frac{I_{d,0}}{1 + g_{m,0} \cdot \left(R_{s,eff} + \frac{R_{sd}}{2} \right) + g_{d,0} \cdot R_{sd}} \qquad \textbf{Eq. V.26}$$

where

$$I_{d,0} = \frac{\beta}{C_{ox} \cdot V_d}\left[\frac{nkT}{C_{ox}} \cdot \left[\frac{1}{2 \cdot nkT} \cdot Q_{i|V_d=0}^2 + C_{ox} \cdot Q_{i|V_d=0} - \frac{1}{2 \cdot nkT} \cdot Q_i^2 + C_{ox} \cdot Q_i\right]\right] \quad \textbf{Eq. V.27}$$

$$Q_i\left(V_g + DIBL \cdot V_d, V_d, V_t, n\right) = \frac{nkT}{q} C_{ox} \cdot LW\left(e^{q \cdot \frac{\left(V_g + DIBL \cdot V_d\right) - V_t - V_d}{nkT}}\right) \quad \textbf{Eq. V.28}$$

$$R_{s,eff} = \frac{1}{W \cdot C_{ox} \cdot v_{sat}} \quad \textbf{Eq. V.29}$$

$$g_{d,0} = \frac{\beta}{C_{ox} \cdot V_d} \cdot Q_i \quad \textbf{Eq. V.30}$$

The *DIBL* and v_{sat} were used as fitting parameters, whereas for the other parameters (V_t, μ_0, n, R_{sd}) the extracted values from the measured $I_d(V_g)$ and $I_d(V_d)$ mean curves were used. As can be seen in Figure V-44, a very good fitting with the experimental characteristics for all cases was achieved with only two fitting parameters, namely *DIBL* and v_{sat}.

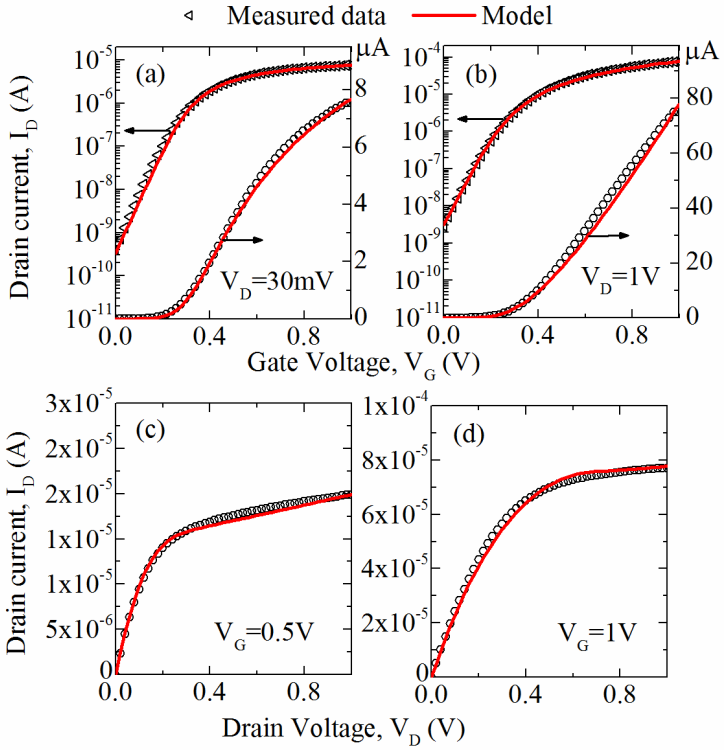


Figure V-44 Experimental (symbols) and Lambert W function (lines) results of drain current versus gate (a, b) and drain (c, d) voltage for n-MOS SOI devices with W=0.06µm and L=0.02µm.

Afterwards, based on the experimentally extracted matching parameters, a random generation of the individual MOSFET parameters was performed using a MC process with a normal distribution in order to compare the MC simulation results to the experimental data (see Figures V-45 and V-46). It should be emphasized that the variations of $\Delta I_d/I_d$, as well as $\sigma(\Delta I_d/I_d)$, were very well reproduced as a function of both gate and drain voltages.

Finally, it should be mentioned that our local variability (matching) characterization and MC modeling verification methodologies are simpler than the variability-aware compact model methodology developed in [272] for circuit design. Our approach is more dedicated to matching characterization purpose as materialized by the matching model of Eq. V.25.

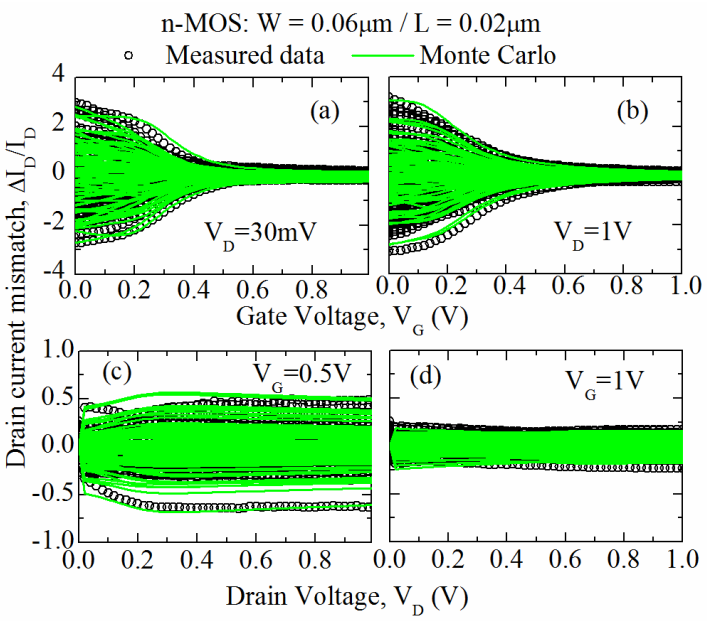


Figure V-45 Experimental (symbols) and modeled (lines) variations of $\Delta I_d/I_d$ versus gate (a, b) and drain (c, d) voltage of an ensemble of 90 n-MOS SOI devices.

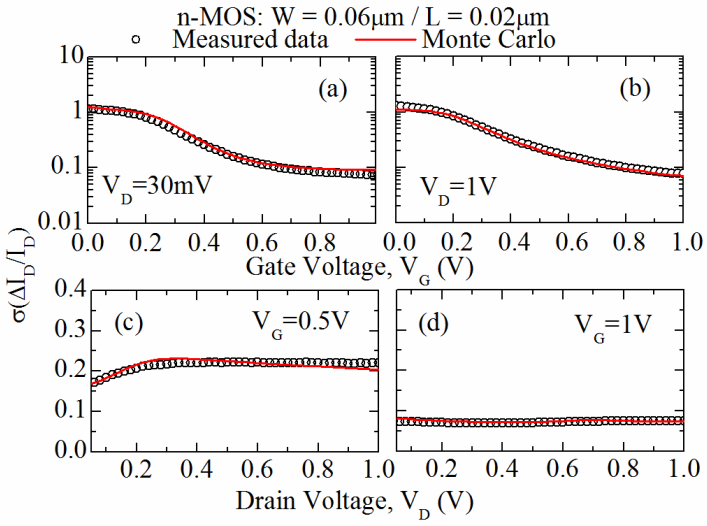


Figure V-46 Experimental (symbols) and modeled (lines) variations of $\sigma\Delta I_d/I_d$ versus gate (a, b) and drain (c, d) voltage of an ensemble of 90 n-MOS SOI devices.

V.6 Gate Current Local Variability

V.6.1 Gate Current Mismatch Modeling

In Figure V-47, typical $I_g(V_g)$ characteristics measured at $V_d = 30\ mV$ are presented, revealing the gate current variability for a small and a large area device as well.

The corresponding gate current local variability, $\Delta I_g/I_g(V_g)$ is calculated with the same way as for the drain current (see Figure V-48), namely:

$$\Delta I_g / I_g = \ln\left(I_{g2} / I_{g1} \right) \qquad \textbf{Eq. V.31}$$

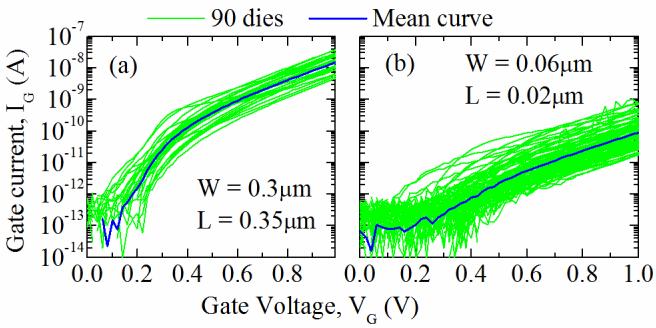


Figure V-47 Experimental $I_g(V_g)$ characteristics and their mean value at V_d=30mV for a large (a) and a small (b) area device.

Based on the fact that the main sources of the gate current mismatch are the local fluctuations of the threshold voltage, V_t, and the gate oxide thickness t_{ox}, a simple expression for the gate current variability was derived (Eq. V.34), using the sensitivity functions, SS_g and S_{tox}:

$$SS_g = \delta \ln(I_g) / \delta V_g \qquad \textbf{Eq. V.32}$$

$$S_{tox} = \delta \ln(I_g) / \delta t_{ox} \qquad \textbf{Eq. V.33}$$

$$\sigma^2\left(\Delta I_g / I_g\right) = SS_g^2 \cdot \sigma^2(\Delta V_t) + S_{tox}^2 \cdot \sigma^2(\Delta t_{ox}) \qquad \textbf{Eq. V.34}$$

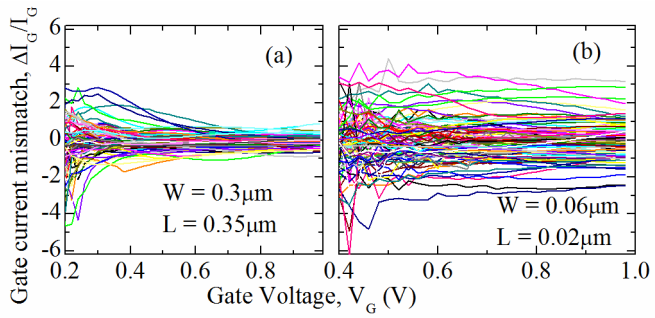


Figure V-48 $\Delta I_g/I_g$ curves versus gate voltage at V_d=30mV for a large (a) and for a small (b) area device.

In Equations V.32 and V.33, the gate current was modeled based on the Lambert function for the inversion charge (Eq. V.28) in the linear region and the simple gate current model (Eq. V.35) [273]:

$$I_g = W \cdot L \cdot f \cdot Q_i \cdot \exp\left(-t_{ox} \cdot HK / \lambda_{ox}\right) \cdot \exp\left(\frac{Q_i}{\varepsilon_{ox}} \cdot \frac{t_{ox}}{V_{ox}}\right) \qquad \textbf{Eq. V.35}$$

where

$$V_{ox} = \left(\frac{4\,\Phi\,\lambda_{ox}}{t_{ox} \cdot HK}\right) \qquad \textbf{Eq. V.36}$$

$$\lambda_{ox} = \left(1.5 \cdot K \cdot \Phi^{1/2}\right)^{-1} \qquad \textbf{Eq. V.37}$$

$$K = \frac{4}{3\hbar} \cdot \sqrt{2 \cdot q \cdot m_{ox}} \qquad \textbf{Eq. V.38}$$

In Equations V.35-V.38, f is the mean escape frequency, m_{ox} the effective electron mass and q the electron charge, $\hbar$ the reduced Planck constant, HK is the thickness enhancement factor which accounts for the physical thickness of the high-k gate dielectric and

Φ is the barrier height. Notice that the parameters HK and Φ have the same values for all geometries:

$$HK = 1.9 \quad \textbf{Eq. V.39}$$

$$\Phi = 1V \quad \textbf{Eq. V.40}$$

With $\sigma(\Delta V_t)$ and $\sigma(\Delta t_{ox})$ as fitting parameters, a good agreement between the model and the experimental data was achieved (see Figure V-49), emphasizing the model functionality. However, the parameter $\sigma(\Delta V_t)$ extracted from the gate current mismatch is found to be larger (× 2-4) than the one obtained from the drain current mismatch, revealing additional variability sources not fully accounted for by Eq. V.34.

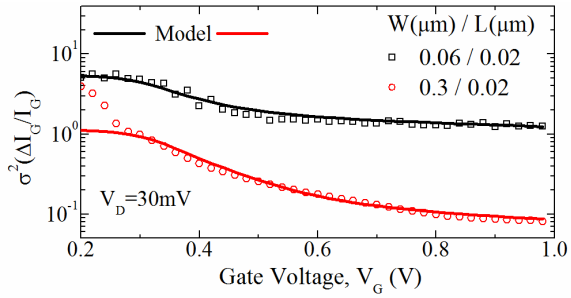


Figure V-49 Experimental (symbols) and model (lines) results of $\sigma^2(\Delta I_g/I_g)$ versus gate voltage for a small and a large area device.

V.6.2 Gate Current Mismatch Model Verification through Monte Carlo Simulation

In a similar way with the MC simulations of the drain current mismatch characteristics, the same procedure was applied in order to reproduce the $I_g(V_g)$ characteristics. Using the gate current model of Eq. V.35, the I_g-V_g mean curves were accurately reproduced as shown in Figure V-50. Notice the very good agreement with the experimental data with only two parameters, namely HK and Φ, constant for all geometries and equal to the values used in Section V.6.1.

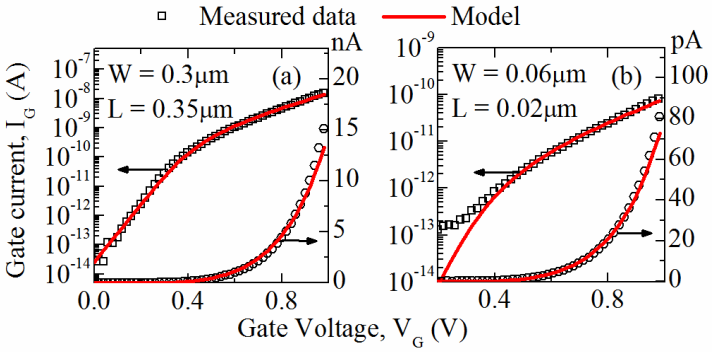


Figure V-50 Experimental (symbols) and model (lines) results of gate current versus gate voltage for a large (a) and a small (b) area device.

Finally, after MC simulations, the $\Delta I_G/I_G$ variations and $\sigma(\Delta I_G/I_G)$ were reproduced in very good agreement with the experimental data (see Figure V-51), revealing once more the consistency of our mismatch model.

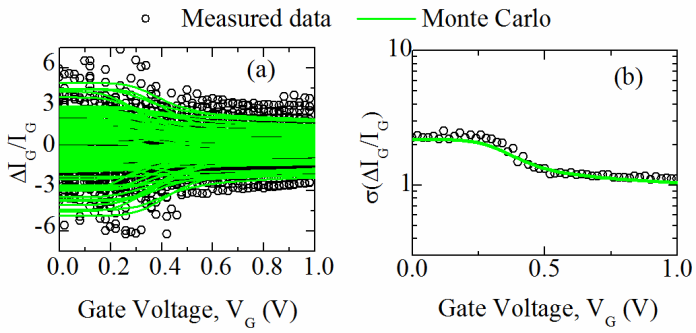


Figure V-51 Measured (symbols) and modeled (lines) variations of $\Delta I_g/I_g$ and $\sigma\Delta I_g/I_g$ versus gate voltage in FDSOI devices with W=0.06 μm and L=0.02 μm.

V.7 Impact of Drain Current Local Variability on a Circuit's Operation

In order to demonstrate the impact of the drain current mismatch on a circuit's performance, the 6T SRAM cell was simulated once more, this time including local fluctuations. The local fluctuations of the threshold voltage, the ideality factor, the current gain factor and the source-drain series resistance were taken into account by modifying the corresponding lines of the code of Appendix A this way:

```
Vtf = Vfb_f + ( (Vth/f2) * ln( (NA/ni) * (1/(exp(f1/Vth))) ) ) +dVt;
h1 = h1*(1+dn_n);
u0=93.5*exp(dbeta_beta);
```

where "dVt", "dn_n" and "dbeta_beta" correspond to ΔV_t, $\Delta n/n$ and $\Delta\beta/\beta$ respectively. It is obvious from the last line that the current gain factor fluctuations where incorporated into the low-field mobility, μ_0 in our model. This results from the following relationship, considering constant W, L and C_{ox}:

$$\beta = \frac{W}{L}\mu_0 C_{ox} \Leftrightarrow \mu_0 = \frac{\beta \cdot L}{W \cdot C_{ox}} \Leftrightarrow \Delta\mu_0 = \Delta\beta \cdot \frac{L}{W \cdot C_{ox}} \Leftrightarrow \Delta\mu_0 = \frac{\Delta\beta \cdot \mu_0}{\beta} \Leftrightarrow \frac{\Delta\mu_0}{\mu_0} = \frac{\Delta\beta}{\beta}$$

Therefore, considering also log-normal distribution for the current gain factor local fluctuations:

$$\mu_0 = e^{\ln(\mu_{0,initial})\frac{\Delta\beta}{\beta}} \Leftrightarrow \mu_0 = \mu_{0,initial} e^{\left(\frac{\Delta\beta}{\beta}\right)}$$

Moreover, in order to include the source-drain series resistance local fluctuations in our model, the following two lines were added in the Verilog-A code:

```
V(d,d_in)<+I(d_in,s_in)*(Rsd+dRsd)/2
V(s_in,s)<+I(d_in,s_in)*(Rsd+dRsd)/2
```

where dRsd corresponds to $\sigma\Delta R_{sd}$. This means that Figure V-52 has been considered for the MOSFET and therefore the terminals d and s in the code of Appendix A were replaced by d_in and s_in respectively.

Then, in order to declare these local variations, the next following lines have been added in the code:

```
(* cds_inherited_parameter *) parameter real dVt=0;
(* cds_inherited_parameter *) parameter real dbeta_beta=0;
(* cds_inherited_parameter *) parameter real dRsd=0;
(* cds_inherited_parameter *) parameter real dn_n=0;
```

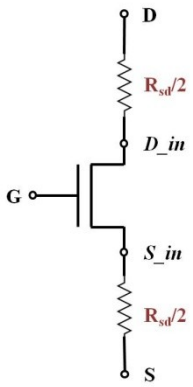


Figure V-52 Representation of n-MOSFET in Verilog-A including the effect of source-drain series resistance.

This way, these parameters disengage themselves from the component initialization so that they can be externally modified on a netlist level and used by the simulator (Spectre in our case). Thus, an extra input file is needed where the parameters initial values as well as their variations are declared, as follows:

```
parameters dVt=0 dbeta_beta=0 dn_n=0 dRsd=0 dVt_p=0 dbeta_beta_p=0 dn_n_p=0 dRsd_p=0
statistics {
        mismatch {
                vary dVt dist=gauss std=0.03 percent=no
                vary dbeta_beta dist=gauss std=0.09 percent=no
                vary dn_n dist=gauss std=0.07 percent=no
                vary dRsd dist=gauss std=370 percent=no

                vary dVt_p dist=gauss std=0.03 percent=no
                vary dbeta_beta_p dist=gauss std=0.09 percent=no
                vary dn_n_p dist=gauss std=0.07 percent=no
                vary dRsd_p dist=gauss std=140 percent=no
                }
        }
```

At this point notice that typical local variation parameter values for this technology were used while for reasons of simplicity and symmetry same values for both transistor types were declared.

In our circuit n-MOSFETs with the nominal dimensions for the 28 nm FDSOI technology ($W=80$ *nm* and $L=30$ *nm*) were used. For symmetry reasons, the p-MOSFETs channel width was defined as $W_p=(8/3)\cdot W_n$. After performing the SRAM "butterfly" curve

simulation including the MOSFET parameters local fluctuations in the drain current model of Chapter III, Figure V-53 was obtained, where an almost 52% degradation of SNM is observed for the worst case.

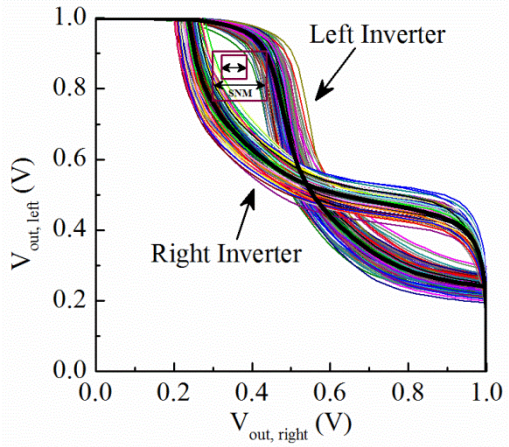


Figure V-53 Impact of drain current mismatch on a 6T-SRAM cell. Black lines represent the mean values of the curves.

On one hand, this finding further demonstrates the significance of local variations in advanced nano-scale electronic circuits. On the other hand, since our implementation is based on values extracted from experimental results, we can predict the impact of local variability on any circuit's behavior following a simple procedure.

V.8 Summary and Conclusions

The main sources of drain and gate current local variability have been thoroughly studied. First, the impact of the SD series resistance mismatch on the drain current variability has been investigated for 28 nm Bulk MOSFETs. A mismatch model that takes into consideration the R_{sd} local variability was developed and used to extract all mismatch parameters, including $\sigma(\Delta V_t)$, $\sigma(\Delta\beta/\beta)$ and $\sigma(\Delta R_{sd})$, in the linear and saturation regions. It has been demonstrated that the impact of R_{sd} on the drain current variability is reduced in the saturation region due to the lower drain current sensitivity from the series resistance variation. Furthermore, as in FDSOI devices, the SD series resistance mismatch, $\sigma(\Delta R_{sd})$, was found to scale down with gate width as R_{sd}, and the normalized series resistance local variability parameter $\sigma(\Delta R_{sd})/R_{sd}$ takes similar values as in FDSOI, demonstrating very good access resistance control in bulk technology.

Then, a detailed statistical characterization of the drain current local and global variability in sub 15 nm Si/SiGe Trigate NW p-MOSFETs and in 14 nm Si bulk FinFETs has been conducted. The main local and global variability MOSFET parameters ($\sigma(\Delta V_t)$, $\sigma(\Delta\beta/\beta)$, $\sigma(\Delta R_{sd})$ and $\sigma(\Delta n/n)$) have been extracted owing to a generalized analytical mismatch model valid in linear region. Our results indicate that, despite their very aggressive dimensions, such devices maintain relatively good variability performance. Finally, a MC compact modeling of the drain current variability has been developed. It provides a statistical MC simulation of the local and global variability of drain current and voltage gain for such advanced devices.

Eventually, a complete investigation of the gate and drain current mismatch in advanced FDSOI devices has been performed. In this aspect, a fully functional drain current mismatch model, valid for any gate and drain bias condition has been developed. The model

was validated using a Lambert function based compact model and performing full gate and drain voltage range Monte Carlo simulations. In parallel, a gate current mismatch model accounting for the main sources of variations has been also presented for the first time, and verified by Monte Carlo simulations. These drain and gate current mismatch compact models can easily be implemented in circuit simulation tools for circuit design and is applicable to both bulk and FDSOI technologies.

Finally, the impact of MOSFET parameters local fluctuations on a circuit performance has been demonstrated. Indeed, the drain current compact model of Chapter III implenteded in Verilog-A code has been used to examine the impact of drain current variability on a 6T SRAM cell. An almost 52% SNM reduction has been observed for the worst case for a 28 nm FDSOI technology.

VI Conclusions and Perspectives

VI.1 Summary and Conclusions

The goals of this dissertation arising from the scaling of new-era devices in the modern MOSFET design were two: the development of an analytical and compact drain current model, valid from weak to strong inversion, below and above threshold describing accurately the transfer and output characteristics of short-channel FDSOI devices and the investigation of reliability and variability issues of such advanced nano-scale transistors.

In the present thesis, we have developed a full gate voltage range methodology using a Lambert W function based inversion charge model, for extracting the electrical parameters in nano-MOSFET devices. We have also developped an analytical and compact drain current model, valid from weak to strong inversion, below and above threshold describing accurately the transfer and output characteristics of short-channel FDSOI devices. Additionally, we have explored reliability issues, including HCI and NBTI of such nano-scale transistors. Finally we have investigated variability phenomena in advanced devices of different technologies, including 28 nm Bulk MOSFETs, sub-15nm Si/SiGe Trigate NW MOSFETs, 14 nm Bulk FinFETs and 14 nm FDSOI transistors.

As far as the MOSFET parameter extraction in terms of I-V and C-V measurements is concerned, we have introduced a new methodology for MOSFET parameter extraction based on the Lambert W function. We have verified that the Lambert W function can describe correctly the inversion charge with gate voltage in advanced FDSOI devices making it suitable for a full gate voltage range parameter extraction from weak to strong inversion region. The proposed methodology which takes into account both the back gate voltages and the channel length can be readily applied to evaluate all electrical MOSFET parameters, namely n, V_t, μ_0, θ_1 and θ_2 in parametric test routines. A very good agreement between experimental data and fitting results has been also obtained for both n- and p-MOSFETs for various gate lengths, front and back gate voltage values. Furthermore, the split C-V technique for the extraction of the intrinsic device parameters has been also explored. More precisely, we have studied the impact of the AC signal oscillator level on the extracted effective mobility as measured by split C-V technique. We found that the use of small enough oscillator level allows extracting reliable effective mobility values for inversion charge down to 10^{10}q/cm^2 in the very weak inversion region. Finally, based on these observations, we have developed a physical model enabling a quantitative description of both inversion charge and effective mobility variations with the oscillator level and the gate voltage.

Concerning the drain current compact modeling study, we have developed a threshold-voltage-based model, since such models are based on based on experimentally measured external quantities and therefore they are expected to be more efficient for low-frequency noise (LFN/RTN), reliability (NBTI/HCI) and variability compact modelings. Indeed, we have derived simple analytical models for the front and back gate threshold voltages and ideality factors based on the minimum values of the front and back surface potentials of lightly doped UTBB FD-SOI MOSFETs. These models taking into account the device geometry parameters and the applied bias voltages with back gate control were found to be in very good agreement with both numerically simulated and experimental results for devices with channel length down to 17 nm. Furthermore, we used these models in order to develop an analytical compact drain current model for lightly doped short-channel UTBB

FDSOI MOSFETs. Indeed we have shown that our drain current compact model accounting for small geometry, saturation velocity, mobility degradation, quantum mechanical, velocity overshoot and self-heating effects, can describe with good accuracy the input and output characterisitics of 28 nm FDSOI MOSFETs for a wide range of back gate bias covering the inversion, depletion and accumulation operation regimes. Finally, after implementing our compact model in Verilog-A, we have simulated the so-called SRAM "butterfly" curve improving its adequacy for implementation in circuit simulation tools.

Afterwards, we have thoroughly studied reliability issues including HCI and NBTI in nanoscale UTBB FDSOI MOSFETs. Regarding to the first case, taking into account the fact that the worst degradation condition occurs at $V_{gs} = V_{ds}$, we have investigated hot-carrier degradation of nanoscale UTBB FDSOI n-MOSFETs under different drain and gate bias stress conditions. After perfoming LFN measurements at room temperature in the frequency and time domains, we have concluded that in fresh devices, the measured noise is composed of 1/f noise related to gate dielectric traps within a tunnelling distance from the interface and Lorentzian noise components related either to g-r traps in the silicon film or to metastable RTN traps located at or near the gate dielectric/silicon interface. After HC-stress for short-time, the results show that g-r and RTN traps are annihilated, which has been attributed to hydrogen released due Si-H dissociation by HC-stress. However, after HC-stress for long-time, the LFN is dominated by large RTN from the subthreshold to the above threshold regions. In addition to the traps detected in the fresh device, analysis of simple RTN observed in the HC-stressed device revealed the presence of additional RTN traps in the subthreshold region. Additionally we found that there is no correlation between RTN amplitude and trap time constants. The results also indicate that the RTN amplitude is determined by the electrostatic impact of the trapped charge, following a modified CNF/CMF model. We have proposed an analytical expression for the RTN amplitude including two physical parameters: Ω' related to the carrier number and mobility fluctuations and ξ related to the trap location over the channel. These parameters can be extracted from experimental data of the RTN relative amplitude, enabling to predict the RTN level from the subthreshold to the above threshold region.

Additionally, we have implemented semi-empirical models in terms of the stress time, channel length, drain bias and gate bias in order to express the impact of the HC degradation on the device parameters, enabling at the same time the possibility to predict the device degradation stressed under different bias conditions, using a unique set of few model parameters determined for each technology through measurements.

Concerning the NBTI stress, we have studied the device stress characteristics and the recovery behavior under positive bias temperature stress of HfSiON gate dielectric UTBB FDSOI p-MOSFETs. We have concluded that the NBTI stress is dominated by exchange of channel charge carriers with pre-existing traps in the gate dielectric, while in the recovery phase, the V_t shift includes a fast initial transient, followed by a very slow non-exponential transient. Last but not least, we have also developed an NBTI model by considering hole-trapping/detrapping mechanisms, capturing the temperature and bias voltage dependence.

Eventually, we have studied in detail the gate and drain current local variability phenomenon in advanced nanoscale devices. In this aspect, we have developed a fully functional drain current mismatch model, valid for any gate and drain bias condition including all main sources of drain current local variability, namely the local fluctuations of the threshold voltage, current gain factor, source-drain series resistance and ideality factor.

We have validated our mismatch model using a Lambert function based compact model and performing full gate and drain voltage range Monte Carlo simulations. This way, we have extracted all mismatch parameters, including $\sigma(\Delta V_t)$, $\sigma(\Delta\beta/\beta)$, $\sigma(\Delta R_{sd})$ and $\sigma(\Delta n/n)$. We applied our model to various advanced technologies proving its proper functionality. Then, we have characterized in terms of drain current local and global variaibility, 14 nm FDSOI MOSFETs, 14 nm bulk FinFETs and sub 15 nm Si/SiGe Trigate NW p-MOSFETs demonstrating that despite their very aggressive dimensions, such devices maintain relatively good variability performance. Additionally, using our model we have investigated the impact of the source-drain series resistance mismatch on the drain current variability for 28 nm Bulk MOSFETs. In parallel, a gate current mismatch model accounting for the main sources of variations -namely the local fluctuations of the threshold voltage and the gate oxide thickness- has been also presented and verified by Monte Carlo simulations. Finally, we have shown the impact of MOSFET parameters local fluctuations on 6T SRAM cell, demonstrating an alsmost 52% SNM reduction for the worst case for a 28 nm FDSOI technology.

VI.2 Future Research Directions

The compact model developed in this dissertation can be further completed in several ways. Some specific recommendations based on the present work are as follows:

- On one hand the transistor channel length tends to shrink down more and more, while on the other hand the channel interactions are expected to significantly decrease (thanks to the FDSOI structures), and as a consequence, the carrier mean free path should increase in such structures. Therefore inclusion of ballistic transport phenomena will strengthen the accuracy of the model.
- The accurate transistor's capacitances prediction is also considered fundamental. Therefore, the development of capacitance models for these UTBB FDSOI MOSFETs would allow predict the discrimination between the channel and the parasitic capacitances, as well as the respective overlap/spacer or BOX contributions to the total device capacitance.
- Finally, as the transistor area is scaled down, the low frequency noise appears more Lorentzian-like instead of 1/f shape and it exhibits more device-to-device variations. The variability in low frequency noise (both flicker noise and Random Telegraph Noise) is becoming increasingly important for circuits using scaled CMOS and needs to be included in the compact models.

Regarding the implementation of our reliability models in circuit simulators, serious challenges need to be addressed. More precisely, advanced methods have to be developed to take into account the transient parameter shift under time-varying (non-stationary) bias conditions.

Concerning the gate current variability model, as already stated, the local fluctuations of the threshold voltage and the gate oxide thickness were already taken into account in our model. Nevertheless, additional variability sources should be inversigated.

Eventually, apart from the above studies performed within the frame of this thesis, there are open questions regarding the introduction of new channel materials and devices in order to to maintain pace with Moore's law. For example, III-V materials like InAs and

InGaAs are widely regarded as leading candidates for increased drive current digital applications. Consequently, the application of the extraction methods or the reliability/variability models presented in this thesis in such novel devices would be of great interest.

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Appendices

Appendix A: Drain current compact model in Verilog-A

The following code has been used for the description of the drain current of the FDSOI n-MOSFET.

```
// VerilogA for Theanooo, threshold_voltage, veriloga


`include "constants.vams"
`include "disciplines.vams"


module nmos_FDSOI(b,d,s,g);


//Definition of constants as variables
real k, q, epsSi, epsOx, ni, Cox_f, Cox_b, Vth, Vbi, Vfb_f, Vfb_b, u0, theta1, theta2, lamdaw, Sn, vsat0, r, Kox, KSi, V_Ei;


//Definition of parameteres in order to be shown in the simulations
parameter real T=300;   //temperature (K)
parameter real NA=1.0e15;   //acceptor's concentration (cm to minus 3)
parameter real Nd=1.0e20;   //doping concentration (cm to minus 3)


// GEOMETRY
parameter real L=30e-7;   //channel length (cm)
parameter real W=0.5e-4;   //channel width (cm)
parameter real tox=1.55e-7;   //front gate oxide thickness (cm)
parameter real tbox=25e-7;   //back gate oxide thickness (cm)
parameter real tsi=7e-7;   //silicon thickness (cm)


// MODEL PARAMETERS
parameter real Ac=0.2;
parameter real Bc=3.1;
parameter real factor=0.04;


parameter real fms_f=0.37;   //front gate metal-silicon work function difference (V)
parameter real fms_b=0.3;   //back gate metal-silicon work function difference (V)


//Definition of variables
real Vgbtonos, xcf, toxeq, tsieq, Coxfeq, lamdaf, lamdafeq, af, afeq, bf, bfeq, ymf, f1, f2, Vtf, Afc, Afceq, Kf, Kfeq, h1, qfs, qfd, qfstonos, qfdtonos, vsat, ueff_f, Vd_sat, Leff_f, DL, Rth, A0, A1, A2, Idf;
```

```
inout b, d, s, g;
electrical b, d, s, g;

// MODEL
analog begin

//Constants
k=1.38e-23;   //boltzmann's constant (J/K)
q=1.6e-19;   //electron charge (C)
epsSi=12*8.85e-14;   //electrical permittivity of silicon (F/cm)
epsOx=4*8.85e-14;   //electrical permittivity of oxide (F/cm)
ni=1.45e10;   //carrier concentration in intrinsic silicon (cm to minus 3)
Cox_f=epsOx/tox;   //front gate oxide capacitance (F/cm)
Cox_b=epsOx/tbox;   //back gate oxide capacitance (F/cm)
Vth=(k*T)/q;   //thermal voltage (V)
Vbi=Vth*ln( (NA*Nd)/pow(ni,2) );   //build-in potential (V)
Vfb_f = fms_f - Vth*ln( NA/ni );   //front gate flatband voltage (V)
Vfb_b = fms_b - Vth*ln( NA/ni );   //back gate flatband voltage (V)

        Vgbtonos = V(b,s) - Vfb_b;

        //definition of conductive path
        if (V(b,s)<=0)
                xcf = Ac * exp( V(b,s)/Bc ) * tsi;
        else
                xcf = ( Ac + factor * V(b,s) ) * tsi;

        toxeq = tox + (epsOx/epsSi) * xcf;   //equivalent thickness for the front gate oxide
        tsieq = tsi - (epsOx/epsSi) * xcf;   //equivalent thickness for the silicon body
        Coxfeq = epsOx/toxeq;   //equivalent oxide thickness

        //natural length at the conductive path
        lamdaf = sqrt ( ( epsSi*tox*tsi*( 2*epsSi*tbox + epsOx*tsi ) + epsOx*tsi*( 2*epsSi*tbox + epsOx*tsi )*xcf - epsOx*( epsSi*( tox+tbox )+ epsOx*tsi ) * pow(xcf,2) ) / ( 2*epsOx*( epsSi*(tox+tbox) + epsOx*tsi ) ) );
        //equivalent natural length
        lamdafeq = sqrt ( ( epsSi*toxeq*tsieq*( 2*epsSi*tbox + epsOx*tsieq ) + epsOx*tsieq*( 2*epsSi*tbox + epsOx*tsieq )*xcf - epsOx*( epsSi*( toxeq+tbox )+ epsOx*tsieq ) * pow(xcf,2) ) / ( 2*epsOx*( epsSi*(toxeq+tbox) + epsOx*tsieq ) ) );
```

```
//potential distribution
af = ( epsSi*tbox + epsOx*( tsi-xcf ) ) / ( epsSi*( tox+tbox ) + epsOx*tsi );
afeq = ( epsSi*tbox + epsOx*( tsieq-xcf ) ) / ( epsSi*( toxeq+tbox ) + epsOx*tsieq );

bf = ( epsSi*tox + epsOx*xcf ) / ( epsSi*( tox+tbox ) + epsOx*tsi );
bfeq = ( epsSi*toxeq + epsOx*xcf ) / ( epsSi*( toxeq+tbox ) + epsOx*tsieq );

//minimum potential position
ymf = (L/2) - ( (lamdaf/2) * ln( ( ( (Vbi - (bf*Vgbtonos)) * (exp(L/lamdaf) - 1) ) + (V(d,s) * exp(L/lamdaf)) ) / ( (Vbi - (bf*Vgbtonos)) * (exp(L/lamdaf) - 1) - V(d,s)) ) );

//potential at the conductive path f=f1+(f2*Vgtonos)
f1 = ( (( exp(((2*L)-ymf)/lamdaf) - exp(ymf/lamdaf) ) * Vbi) + ( ( (exp((L+ymf)/lamdaf)) - (exp((L-ymf)/lamdaf)) ) * (Vbi+V(d,s)) ) + ( ( exp((L-ymf)/lamdaf)-exp(-ymf/lamdaf) ) * ( exp(L/lamdaf) - exp(ymf/lamdaf) ) * ( exp(ymf/lamdaf) - 1 ) * Vgbtonos * bf ) ) / ( (exp((2*L)/lamdaf)) - 1 );

f2 = af * ( ( ( 1- exp(-ymf/lamdaf) ) * ( (exp(L/lamdaf)) - (exp(ymf/lamdaf)) ) ) / (1+exp(L/lamdaf)) );

//THRESHOLD VOLTAGE
Vtf = Vfb_f + ( (Vth/f2) * ln( (NA/ni) * (1/(exp(f1/Vth))) ) );

//-----------------------------------------------------------------------------------------------------------

Afc = (af*Vtf) + (bf*Vgbtonos);
Afceq = (afeq*Vtf) + (bfeq*Vgbtonos);

Kf = sqrt (((Vbi-Afc)*((exp(L/lamdaf))-1) - V(d,s)) / ((Vbi-Afc)*((exp(L/lamdaf))-1) + (V(d,s)*(exp(L/lamdaf)))));
Kfeq = sqrt (((Vbi-Afceq)*((exp(L/lamdafeq))-1) - V(d,s)) / ((Vbi-Afceq)*((exp(L/lamdafeq))-1) + (V(d,s)*(exp(L/lamdafeq)))));

//IDEALITY FACTOR
h1=1/(afeq*(1-Kfeq*(2*Vbi-2*Afceq+V(d,s))*exp(L/(2*lamdafeq))*(exp(L/lamdafeq)-1)/((exp(L/lamdafeq)+1)*((Vbi-Afceq)*(exp(L/lamdafeq)-1)-V(d,s)) ) ));

//CONSTANTS
u0=93.5;
theta1=0.4;
theta2=0.55;
```

```
        lamdaw=1e-5;
        Sn=1.0;
        vsat0=2.06e7;
        r=0.5;
        Kox=1.4;
        KSi=63.0;
        V_Ei=0.5;

        //SHEET CHARGE CALCULATION
        qfs=h1*Sn*ln(1+exp((V(g,s)-Vtf-2.5*Vth-h1*0)/(h1*Vth*Sn)));
        qfstonos=h1*Sn*ln(1+exp((V(g,s)-Vtf-5.0*Vth-h1*0)/(h1*Vth*Sn)));
        qfd=h1*Sn*ln(1+exp((V(g,s)-Vtf-2.5*Vth-h1*V(d,s))/(h1*Vth*Sn)));
        qfdtonos=h1*Sn*ln(1+exp((V(g,s)-Vtf-5.0*Vth-h1*V(d,s))/(h1*Vth*Sn)));

        //DRAIN CURRENT CALCULATIONS
        vsat=vsat0*(1+2*lamdaw/L);

        ueff_f=u0/(1+theta1*Vth*qfs+theta2*pow(Vth,2)*pow(qfs,2));

        Vd_sat=sqrt(pow((vsat*L/ueff_f),2)+2*Vth*qfs*vsat*L/ueff_f)-vsat*L/ueff_f+Vth*qfs/h1-
Vth*qfs;

        DL=lamdafeq*ln(1+((V(d,s)-Vd_sat+0.05)*tanh(pow((V(d,s)/Vd_sat),3)))/V_Ei);

        Leff_f=L-DL;

        Rth=sqrt(tbox/(tsi*Kox*KSi))/(2.0*W*1e-2);

        A0=(W*ueff_f*Cox_f*pow(Vth,2)*(qfs-qfd+(pow(qfstonos,2)-
pow(qfdtonos,2))/(2.0*h1)))/Leff_f;

        A1=r*Rth*V(d,s)/T;

        A2=1+(Vth*ueff_f*(qfstonos-qfdtonos))/(Leff_f*vsat);

        I(d,s) <+ (-A2+sqrt(pow(A2,2)+4*A1*A0))/(2*A1);

end
endmodule
```

Appendix B: Scientific Publications

Scientific Journals

1) Nikolaos Fasarakis, **Theano Karatsori**, Dimitrios H. Tassis, Christoforos G. Theodorou, Francois Andrieu, Olivier Faynot, Gerard Ghibaudo, Charalabos A. Dimitriadis. "*Analytical Modeling of Threshold Voltage and Interface Ideality Factor of Nanoscale Ultrathin Body and Buried Oxide SOI MOSFETs With Back Gate Control*", IEEE Transactions on Electron Devices, Vol. 61, Issue: 4, pp. 969-975, April 2014.
2) **T.A. Karatsori**, C.G. Theodorou, E.G. Ioannidis, S. Haendler, E. Josse, C.A. Dimitriadis, G. Ghibaudo. "*Full gate voltage range Lambert-function based methodology for FDSOI MOSFET parameter extraction*", Solid-State Electronics, Vol. 111, pp. 123-128 September 2015.
3) **Theano A. Karatsori**, Andreas Tsormpatzoglou, Christoforos G. Theodorou, Eleftherios G. Ioannidis, Sebastien Haendler, Nicolas Planes, Gerard Ghibaudo, Charalabos A. Dimitriadis. "*Analytical Compact Model for Lightly Doped Nanoscale Ultrathin-Body and Box SOI MOSFETs With Back-Gate Control*", IEEE Transactions on Electron Devices, Vol. 62, Issue: 10, pp. 3117-3124, October 2015.
4) **T.A. Karatsori**, C.G. Theodorou, S. Haendler, N. Planes, G. Ghibaudo, C.A. Dimitriadis. "*Hot-carrier degradation model for nanoscale ultra-thin body ultra-thin box SOI MOSFETs suitable for circuit simulators*", Microelectronic Engineering, Vol. 159, pp. 9-16, June 2016.
5) **Theano A. Karatsori**, Christoforos G. Theodorou, Xavier Mescot, Sebastien Haendler, Nicolas Planes, Gérard Ghibaudo, Charalabos A. Dimitriadis. "*Study of Hot-Carrier-Induced Traps in Nanoscale UTBB FD-SOI MOSFETs by Low-Frequency Noise Measurements*", IEEE Transactions on Electron Devices, Vol. 63, Issue: 8, pp. 3222-3228, August 2016.
6) **T. A. Karatsori**, C. G. Theodorou, C. A. Dimitriadis, G. Ghibaudo. "*Influence of AC signal oscillator level on effective mobility measurement by split C–V technique in MOSFETs*", Electronics Letters, Vol. 52, Issue: 17, August 2016.
7) **Theano A. Karatsori**, Christoforos G. Theodorou, Sebastien Haendler, Nicolas Planes, Gérard Ghibaudo, Charalabos A. Dimitriadis. "*Characterization and Modeling of NBTI in Nanoscale UltraThin Body UltraThin Box FD-SOI MOSFETs*", IEEE Transactions on Electron Devices, Vol. 63, Issue: 12, pp. 4913-4918 December 2016.
8) **T. A. Karatsori**, C. G. Theodorou, S. Haendler, C. A. Dimitriadis, G. Ghibaudo. "*Drain current local variability from linear to saturation region in 28nm bulk NMOSFETs*", Solid-State Electronics, Vol. 128, Special Issue, pp. 31-36, February 2017.
9) **Theano A. Karatsori**, Christoforos G. Theodorou, Emmanuel Josse, Charalabos A. Dimitriadis, Gérard Ghibaudo. "*All Operation Region Characterization and Modeling of Drain and Gate Current Mismatch in 14-nm Fully Depleted SOI MOSFETs*", IEEE Transactions on Electron Devices, Vol. 64, Issue: 5, pp. 2080-2085, May 2017.

International Conferences

1) **T. A. Karatsori**, C. G. Theodorou, E. G. Ioannidis, S. Haendler, E. Josse, C. A. Dimitriadis, G. Ghibaudo. "*Full front and back gate voltage range method for the parameter extraction of advanced FDSOI CMOS devices*", 73rd Annual Device Research Conference (DRC), Columbus, Ohio (USA), June 2015.
2) **T. A. Karatsori**, C. G. Theodorou, S. Haendler, N. Planes, G. Ghibaudo, C. A. Dimitriadis. "*Hot carrier degradation mechanisms of short-channel FDSOI n-MOSFETs*", 73rd Annual Device Research Conference (DRC), Columbus, Ohio (USA), June 2015.
3) **T. A. Karatsori**, C. G. Theodorou, S. Haendler, C. A. Dimitriadis, G. Ghibaudo. "*Drain current local variability from linear to saturation region in 28nm bulk NMOSFETs*", Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), Vienna (Austria), January 2016.
4) R. Lavieville, **T. Karatsori**, C. Theodorou, S. Barraud, C.A. Dimitriadis, G. Ghibaudo. "*Statistical characterization of drain current local and global variability in sub 15nm Si/SiGe Trigate pMOSFETs*", 46th European Solid-State Device Research Conference (ESSDERC), Lausanne (Switzerland), September 2016.
5) **T. A. Karatsori**, C. G. Theodorou, R. Lavieville, T. Chiarella, J. Mitard, N. Horiguchi, C. A. Dimitriadis, G. Ghibaudo. "*Statistical Characterization and Modeling of Drain Current Local and Global Variability in 14 nm bulk FinFETs*", 30th International Conference on Microelectronic Test Structures (ICMTS), Grenoble (France), March 2017.

Appendix C: List of Abbreviations

2D	→	Two Dimensional
3D	→	Three Dimentional
6T	→	6 Transistor
AC	→	Alternating Current
B	→	Substrate
BOX	→	Buried Oxide
BTI	→	Bias Temperature Instability
CLM	→	Channel Length Modulation
CMOS	→	Complementary Metal–Oxide–Semiconductor
CNF/CMF	→	Carrier Number Fluctuations with Correlated Mobility Fluctuations
C-V	→	Capacitance-Voltage
D	→	Drain
DD	→	Drift Diffusion
DG	→	Double Gate
DIBL	→	Drain-Induced Barrier Lowering
EDA	→	Electronic Design Automation
FDSOI	→	Fully Depleted Silicon-On-Insulator
FET	→	Field Effect Transistor
FFT	→	Fast Fourier Transform
FinFET	→	Fin-Shaped Field Effect Transistor
G	→	Gate
GAA	→	Gate-All-Around
G-R	→	Generation-Recombination
HC	→	Hot Carrier

HCI	→	Hot Carrier Injection
HDL	→	Hardware Description Language
IC	→	Integrated Circuit
ITRS	→	International Technology Roadmap for Semiconductors
I-V	→	Current-Voltage
LFN	→	Low-Frequency Noise
LW	→	Lambert W
MOS	→	Metal-Oxide-Semiconductor
NBTI	→	Negative Bias Temperature Instability
NM	→	Noise Margin
NMP	→	Non-Radiative Multiphonon
NW	→	Nanowire
MC	→	Monte Carlo
PBTI	→	Positive Bias Temperature Instability
PSD	→	Power Spectral Density
QMEs	→	Quantum-Mechanical Effects
RTN	→	Random Telegraph Noise
RTS	→	Random Telegraph Signal
S	→	Source
SCEs	→	Short-Channel Effects
SD	→	Source-Drain
SGOI	→	Silicon Germanium-On-Insulator
SH	→	Self-Heating
Si	→	Silicon
SiGe	→	Silicon Germanium
SNM	→	Static Noise Margin

SOI	→	Silicon-On-Insulator
SPICE	→	Simulation Program with Integrated Circuit Emphasis
SRAM	→	Static Random Access Memory
STI	→	Shallow Trench Isolation
TCAD	→	Technology Computer Aided Design
UTBB	→	Ultra-Thin Body and Buried-oxide
VLSI	→	Very-Large-Scale Integration
VO	→	Velocity Overshoot
VTC	→	Voltage Transfer Curves

Appendix D: Greek Abstract

Τίτλος Διατριβής

«Ηλεκτρικός Χαρακτηρισμός και ανάπτυξη μοντέλων προηγμένων MOSFET νανοκλίμακας υπέρλεπτου υμενίου και εμφυτευμένου οξειδίου και εφαρμογή σε προσομοίωση κυκλωμάτων»

Περίληψη

Η προοδευτική κλιμάκωση της τεχνολογίας CMOS οδήγησε τη βιομηχανία ημιαγωγών στην πραγματοποίηση ταχύτερων και χαμηλότερης κατανάλωσης ισχύος κυκλωμάτων και συστημάτων VLSI. Μεταξύ των πιο συνηθισμένων λύσεων για διατάξεις νανο-κλίμακας υψηλής απόδοσης είναι τα τρανζίστορ επίδρασης πεδίου τριών πυλών (Fin-shaped Field Effect Transistors - FinFET) καθώς και διατάξεις MOSFET δύο πυλών πλήρους κένωσης πυριτίου-πάνω σε-μονωτή (Fully Depleted Silicon-On-Insulator – FDSOI MOSFET), τα οποία παρουσιάζουν πολύ καλές επιδόσεις όσον αφορά φαινόμενα μικρού μήκους καναλιού (Short-Channel Effects - SCEs) και σχετικά με το φαινόμενο μείωσης του φράγματος δυναμικού της επαφής πηγής-διαύλου που προκαλείται λόγω της τάσης απαγωγού-πηγής (Drain-Induced Barrier Lowering - DIBL). Βέβαια σε σύγκριση με την τεχνολογία των FinFET, αυτή των FDSOI χρησιμοποιεί μια πιο απλούστερη διαδικασία παρασκευής χάρη στην επίπεδη δομή τους. Επιπλέον, η δυνατότητα πόλωσης της πίσω πύλης την καθιστά ιδιαίτερα ενδιαφέρουσα και χρήσιμη για εφαρμογές πολλαπλών-τάσεων κατωφλίου (multi-V_t).

Η παρούσα διδακτορική διατριβή θέτει ως στόχο την αντιμετώπιση ζητημάτων που προκύπτουν από την ελάττωση στις διαστάσεις των διατάξεων τελευταίας τεχνολογίας στον σύγχρονο σχεδιασμό MOSFET, δηλαδή την ανάπτυξη ενός αναλυτικού και συμπαγούς μοντέλου ρεύματος απαγωγού, που θα ισχύει σε όλες τις περιοχές λειτουργίας του τρανζίστορ, από την ασθενή εώς την ισχυρή αναστροφή και που θα περιγράφει με ακρίβεια τις χαρακτηριστικές εισόδου και εξόδου των διατάξεων νανο-κλίμακας FDSOI και την διερεύνηση ζητημάτων επιδόσεων -δηλαδή αξιοπιστίας (reliability) και μεταβλητότητας (variability)- αυτών των προηγμένων διατάξεων νανοκλίμακας. Στο μεταξύ, ο ακριβής προσδιορισμός των ηλεκτρικών παραμέτρων των MOSFET είναι επίσης απαραίτητος για την κατανόηση της φυσικής και του σχεδιασμού των διατάξεων, ιδιαίτερα εάν λάβουμε υπόψη ότι καθώς η τάση τροφοδοσίας μειώνεται με την ελλάτωση των διαστάσεων των τρανζιστορ, η τάση λειτουργίας της πύλης μετατοπίζεται πλησιέστερα στην τάση κατωφλίου (λειτουργία κοντά στην τάση κατωφλίου) και η υπόθεση ότι το φορτίο αναστροφής ποικίλλει περίπου γραμμικά με την ενεργό τάση πύλης ($V_{ov} = V_{gs} - V_t$) καθίσταται όλο και λιγότερο ακριβής. Έτσι, ένας επιπλέον στόχος είναι η ανάπτυξη μιας μεθοδολογίας που επιτρέπει την εξαγωγή των παραμέτρων των MOSFET σε ολόκληρη την περιοχή τάσης της πύλης δηλαδή από την περιοχή ασθενούς εως την περιοχή ισχυρής αναστροφής, επιτρέποντας την πλήρη κάλυψη της περιοχής κάτω και πάνω από την τάση κατωφλίου, παρά τη μείωση της τάσης τροφοδοσίας.

Αρχικά, παρουσιάζουμε μια νέα μεθοδολογία για την εξαγωγή των ηλεκτρικών παραμέτρων διατάξεων νανοκλίμακας FDSOI MOSFET που ισχύει σε όλο το εύρος της τάσης πύλης και βασίζεται στην συνάρτηση Lambert W. Με χρήση των μετρήσεων χωρητικότητας επιβεβαιώνεται ότι η συνάρτηση Lambert W μπορεί να περιγράψει πολύ καλά

το φορτίο αναστροφής σαν συνάρτηση της τάσης της πύλης για αυτά τα τρανζίστορ. Με βάση την εξίσωση του ρεύματος απαγωγού στην γραμμική περιοχή που περιλαμβάνει το φορτίο αναστροφής που περιγράφεται από τη συνάρτηση Lambert της τάσης πύλης και την τυπική εξίσωση ευκινησίας επιτυγχάνεται η εξαγωγή των πέντε βασικών ηλεκτρικών παραμέτρων (τάση κατωφλίου - V_t, συντελεστής κλίσης υποκατωφλίου -ideality factor - η, ευκινησία χαμηλού πεδίου - μ_0, συντελεστές εξασθένησης της ευκινησίας πρώτης και δεύτερης τάξης - θ_1 και θ_2) των MOSFET από τις πειραματικές χαρακτηριστικές εισόδου. Στην συνέχεια, οι παράμετροι που εξήχθησαν συγκρίνονται με τις αντίστοιχες παραμέτρους όπως αυτές εξάγονται με την γνωστή μέθοδο Y-Function στην περιοχή της ισχυρής αναστροφής. Η παρούσα μεθοδολογία για την εξαγωγή των ηλεκτρικών παραμέτρων των MOSFET έχει επαληθευτεί σε ένα ευρύ φάσμα μηκών καναλιού καθώς και τάσεων της πίσω πύλης σε διατάξεις νανο-κλίμακας FDSOI, αποδεικνύοντας έτσι την απλότητα, την ακρίβεια και την ανθεκτικότητα της.

Έπειτα, αναπτύσσουμε απλές εκφράσεις για την ελάχιστη τιμή των κατανομών του δυναμικού κατά μήκος του καναλιού της μπροστά και πίσω πύλης με την βοήθεια των οποίων αναπτύσσουμε αναλυτικά μοντέλα για τις τάσεις κατωφλίου και τους συντελεστές ιδανικότητας της μπροστά και πίσω πύλης για τα τρανζίστορ χαμηλής συγκέντρωσης προσμίξεων υπέρλεπτου υμενίου και εμφυτευμένου οξειδίου (Ultra Thin Body and Box - UTBB) FDSOI MOSFETs. Τα μοντέλα αυτά έχουν επαληθευτεί τόσο με αριθμητικές προσομοιώσεις - στα πλαίσια των γεωμετρικών παραμέτρων των διατάξεων και των εφαρμοζόμενων τάσεων πόλωσης - όσο και με πειραματικά αποτελέσματα για διατάξεις με μήκος καναλιού έως 17 nm. Με βάση τα μοντέλα των τάσεων κατωφλίου και των συντελεστών ιδανικότητας αναπτύσσουμε ένα αναλυτικό και συμπαγές μοντέλο για το ρεύμα του απαγωγού για τα χαμηλής συγκέντρωσης προσμίξεων UTBB FDSOI MOSFETs με έλεγχο της πίσω πύλης, με βάση το οποίο μπορεί και περιγράφεται μόνο με μία εξίσωση ρεύματος η συμπεριφορά του τρανζίστορ σε όλες τις περιοχές λειτουργίας του. Το μοντέλο ρεύματος -το οποίο περιλαμβάνει το φαινόμενο μείωσης του φράγματος δυναμικού της επαφής πηγής-διαύλου λόγω της τάσης απαγωγού-πηγής (DIBL), το φαινόμενο διαμόρφωσης μήκους του καναλιού (Channel-Length Modulation - CLM), το φαινόμενα υποβάθμισης της ευκινησίας και του κορεσμού της ταχύτητας των ηλεκτρονίων, τα κβαντικά φαινόμενα καθώς και τα φαινόμενα αυτοθέρμανσης (self-heating) και αύξησης της ταχύτητας κόρου (velocity overshoot)- επιβεβαιώθηκε συγκρίνοντας με πειραματικά αποτελέσματα χαρακτηριστικών εισόδου και εξόδου για τρανζίστορ με μήκη καναλιού 30 και 240 nm και με πόλωση της πίσω πύλης που κυμαίνεται από -3 έως +3 V. Οι παράμετροι ευκινησίας (μ_0, θ_1 και θ_2) καθώς και οι παράμετροι της τάσης κατωφλίου (A_c, B_c και $\Delta\varphi_f$) εξήχθησαν από τα πειραματικά δεδομένα ενώ στο μοντέλο χρησιμοποιούνται μόνον τρεις παράμετροι προσαρμογής (V_E, r και λ_w). Η καλή ακρίβεια του μοντέλου το καθιστά κατάλληλο για εφαρμογή σε εργαλεία προσομοίωσης κυκλώματος. Πράγματι, το αναλυτικό μοντέλο ρεύματος απαγωγού υλοποιείται μέσω κώδικα Verilog-A για προσομοίωση θεμελιωδών κυκλωμάτων στο Cadence Spectre.

Μετά την ανάπτυξη του αναλυτικού συμπαγούς μοντέλου ρεύματος απαγωγού, μελετώνται ζητήματα αξιοπιστίας για αυτά τα τρανζίστορ SOI νανοκλίμακας υπέρλεπτού υμενίου και εμφυτευμένου οξειδίου, συμπεριλαμβανομένου της ηλεκτρικής καταπόνησης λόγω θερμών φορέων (Hot Carrier Injection stress - HCI) και υπό συνθήκες αρνητικής πόλωσης της πύλης σε υψηλή θερμοκρασία (Negative Bias Temperature Instability - NBTI). Το φαινόμενο των θερμών φορέων παρατηρείται κοντά στο άκρο του απαγωγού εξαιτίας

θερμών φορέων επιταχυνόμενων στο κανάλι και κυριαρχεί σε διατάξεις n-MOS , ενώ αντίθετα, το φαινομενο NBTI κυριαρχεί σε διατάξεις p-MOS κατά μήκος ολόκληρου του καναλιού όταν εφαρμόζεται αρνητική τάση πύλης-πηγής:

- ✓ Κατά το φαινόμενο της ηλεκτρικής καταπόνησης HCI τα τρανζίστορ καταπονούνται εφαρμόζοντας τάση "καταπόνησης" στα ηλεκτρόδια της πύλης και του απαγωγού. Σύμφωνα με την βιβλιογραφία για τα τρανζίστορ νανο-κλίμακας η χειρότερη περίπτωση εμφανίζεται όταν εφαρμόσουμε ίσες τάσεις στην πύλη και στον απαγωγό. Στην ανάλυσή μας, οι παγίδες που προκαλούνται από θερμούς φορείς (Hot Carriers - HC) διερευνώνται με μετρήσεις θορύβου χαμηλών συχνοτήτων (Low Frquency Noise - LFN) τόσο στο πεδίο της συχνότητας όσο και στο πεδίο του χρόνου. Τα μετρούμενα φάσματα θορύβου αποτελούνται από συνιστώσες τύπου 1/f (flicker noise) καθώς και Lorentzian. Ο Lorentzian θόρυβος μπορεί να οφείλεται είτε σε θόρυβο γένεσης-επανασύνδεσης (generation-recombination - g-r) είτε σε θόρυβο τυχαίου τηλεγραφικού σήματος (Random Telegraph Signal - RTS). Βάσει των αποτελεσμάτων των μετρήσεων χαμηλής συχνότητας, η επίδραση της ηλεκτρικής καταπόνησης λόγω θερμών φορέων σε FDSOI MOSFETs διερευνάται για δύο περιπτώσεις: κάτω από συνθήκες σύντομης και μεγάλης διάρκειας καταπόνησης. Η ανάλυση των RTS παγίδων που ανιχνέυονται στο «φρέσκο» τρανζίστορ (δηλαδή σε αυτό που δεν έχει υποστεί ηλεκρική καταπόνηση) υποδεικνύει ότι το πλάτος του RTS θορύβου δεν σχετίζεται με τις σταθερές χρόνου της παγίδας, δηλαδή η επίδραση του βάθους της παγίδας από την διεπαφή (interface) καλύπτεται από εκείνη της θέσης της παγίδας πάνω από το κανάλι. Το σύνολο των αποτελεσμάτων οδηγεί σε μια αναλυτική έκφραση για το πλάτος του RTS θορύβου, επιτρέποντας την πρόβλεψη των μεταβολών του RTS θορύβου από την περιοχή κάτω από την τάση κατωφλίου μέχρι και στην περιοχή πάνω από την τάση κατωφλίου. Αφού εντοπίσαμε τους μηχανισμούς υποβάθμισης και χρησιμοποιώντας το αναλυτικό μοντέλο ρεύματος απαγωγού, αναπτύσσουμε ένα ημι-εμπειρικό μοντέλο που προβλέπει με καλή ακρίβεια την υποβάθμιση των διατάξεων που υπόκεινται σε συνθήκες ηλεκτρικής καταπόνησης λόγω θερμών φορέων κάτω από διαφορετικές συνθήκες καταπόνησης και χρησιμοποιώντας ένα μοναδικό σύνολο παραμέτρων.
- ✓ Όσον αφορά το φαινόμενο του NBTI, οι μετατόπισεις της τάσης κατωφλίου κατά τη διάρκεια της ηλεκτρικής καταπόνησης σε διαφορετικές συνθήκες θερμοκρασίας και τάσης πόλωσης δείχνουν ότι το NBTI κυριαρχείται από την παγίδευση οπών σε προϋπάρχουσες παγίδες του διηλεκτρικού της πύλης, ενώ η διεργασία της επαναφοράς (recovery) ακολουθεί μια λογαριθμική χρονική εξάρτηση. Αξιοποιώντας τις πειραματικές παρατηρήσεις αναπτύσσούμε ένα μοντέλο NBTI που προβλέπει την εξάρτηση τόσο από την θερμοκρασία όσο και από την πόλωση της πύλης για αυτές τις διατάξεις UTBB FDSOI p-MOSFETs με μηδενική πόλωση της πίσω πύλης και μικρή τάση πόλωσης του απαγωγού.

Τέλος, το τελευταίο μέρος της ερευνητικής μας εργασίας που καλύπτει ένα σημαντικό μέρος της συνολικής εργασίας, ασχολείται με το φαινόμενο της τοπικής μεταβλητότητας (local variability) σε προηγμένες διατάξεις νανο-κλίμακας. Οι κύριες πηγές

που προκαλούν το φαινόμενο της τοπικής μεταβλητότητας των ρευμάτων του απαγωγού και της πύλης μελετώνται διεξοδικά. Έτσι λοιπόν, αναπτύσσουμε ένα πλήρους λειτουργίας μοντέλο που περιγράφει το φαινόμενο των τοπικών μεταβολών του ρεύματος απαγωγού, το οποίο ισχύει για οποιαδήποτε κατάσταση πόλωσης της πύλης και του απαγωγού. Το μοντέλο αυτό συμπεριλαμβάνει όλες τις κύριες πηγές τοπικής μεταβλητότητας του ρεύματος απαγωγού -για τις οποίες θεωρούμε ότι δεν υπάρχει κάποιος μεταξύ τους συσχετισμός- δηλαδή τις τοπικές διακυμάνσεις της τάσης κατωφλίου, του συντελεστή κέρδους, της αντίστασης σειράς απαγωγού-πηγής καθώς και του συντελεστή ιδανικότητας. Όσον αφορά στην μοντελοποίηση της τοπικής μεταβλητότητας της πύλης, λαμβάνονται υπόψη οι τοπικές διακυμάνσεις της τάσης κατωφλίου και του πάχους του οξειδίου της πύλης. Τα προτεινόμενα μοντέλα που περιγράφουν τις τοπικές μεταβλητότητες των ρευμάτων του απαγωγού και της πύλης επαληθεύονται χρησιμοποιώντας ένα συμπαγές μοντέλο που βασίζεται στην συνάρτηση Lambert και εκτελώντας προσομοιώσεις Monte Carlo που αναπαράγουν με ακρίβεια τις πειραματικά μετρημένες μεταβολές ρεύματος. Στη συνέχεια, χάρις στα προτεινόμενα μοντέλα τοπικών μεταβλητότητων, χαρακτηρίζουμε διάφορες προηγμένες τεχνολογίες από την άποψη της απόδοσης τους σε τοπικές (local) και καθολικές (global) μεταβλητότητες. Πράγματι, διεξάγεται λεπτομερής στατιστικός χαρακτηρισμός των τοπικών και καθολικών διακυμάνσεων του ρεύματος απαγωγού σε τραζίστορ πυριτίου (Si) FinFET τεχνολογίας 14 nm και σε διατάξεις τριπλής πύλης πυριτίου/πυριτίου-γερμανίου (Si/SiGe) νανοσυρμάτων p-MOSFETs τεχνολογίας κάτω από 15 nm. Για το σκοπό αυτό, εξάγουμε τις παραμέτρους της τοπικής μεταβλητότητας, οι οποίες δείχνουν ότι, παρά τις εξαιρετικά μικρές τους διαστάσεις, οι διατάξεις αυτές παρουσιάζουν σχετικά καλή απόδοση όσον αφορά στην τοπική αλλά και την καθολική μεταβλητότητα. Επιπλέον, διερευνούμε την επίπτωση των τοπικών διακυμάνσεων της αντίστασης σειράς πηγής-απαγωγού στην συνολική τοπική μεταβλητότητα του ρεύματος απαγωγού σε διατάξεις MOSFETs μεγάλου πάχους καναλιού τεχνολογίας 28 nm. Τέλος, διεξάγουμε μια πλήρη διερεύνηση των τοπικών μεταβλητοτήτων των ρευμάτων πύλης και απαγωγού σε προηγμένες διατάξεις UTBB FDSOI MOSFETs τεχνολογίας 14 nm. Στο σημείο αυτό αξίζει να τονισουμε πως αυτά τα συμπαγή μοντέλα που περιγράφουν τις τοπικές μεταβλητότητες των ρευμάτων της πύλης και του απαγωγού και εφαρμόζονται τόσο σε μεγάλου πάχους καναλιού όσο και σε FDSOI τεχνολογίες, μπορούν εύκολα να υλοποιηθούν σε εργαλεία προσομοίωσης κυκλώματων για σχεδιασμό κυκλώματων. Έτσι λοιπόν, σε μια πρώτη εφαρμογή, χρησιμοποιούμε το αναλυτικό, συμπαγές μοντέλο του ρεύματος απαγωγού που υλοιποιήθηκε ήδη σε κώδικα Verilog-A για να εξετάσουμε την επίδραση της μεταβλητότητας του ρεύματος ρευμαγωγού σε θεμελιώδη κυκλώματα στο Cadence Spectre.

Appendix E: French Abstract

Titre de la Thèse

«Caractérisation et modélisation de UTBB MOSFET sur SOI pour les technologies CMOS avancées et applications en simulations circuits»

Résumé

La mise à l'échelle progressive de la technologie CMOS a conduit l'industrie des semi-conducteurs à la réalisation de circuits et de systèmes VLSI plus rapides et de faible consommation d'énergie. Parmi les solutions les plus courantes pour les dispositifs à l'échelle nanométrique de haute performance se trouvent les transistors à effet de champ à ailettes (FinFET) et les MOSFETs à silicium sur isolant totalement désertées (FDSOI), qui présentent une immunité très élevée aux effets des canaux courts (SCE), une faible variabilité de la tension de seuil et un niveau amélioré de l'abaissement de la barrière induite par le drain (DIBL). Par rapport au FinFET, la technologie UTBB FDSOI utilise un processus de fabrication beaucoup plus simple grâce à sa structure plane. En outre, son option de polarisation arrière est particulièrement intéressante pour les applications multi-V_t.

Cette thèse traite des problèmes soulevés par la mise à l'échelle des dispositifs de la nouvelle ère dans la conception de MOSFET contemporain : le développement d'un modèle de courant de drain analytique et compact, valable dans toutes les régions d'opération, décrivant précisément les caractéristiques de transfert (I_d-V_g) et de sortie (I_d-V_d) des dispositifs FDSOI à canaux courts et l'étude des problèmes de fiabilité et de variabilité de ces transistors à l'échelle nanométrique. De plus, la détermination précise des paramètres électriques des MOSFETs est également essentielle pour la compréhension de la physique et l'ingénierie des dispositifs, et particulièrement si l'on tient compte du fait que lorsque la tension d'alimentation est réduite avec la mise à l'échelle des dispositifs, la polarisation de fonctionnement de la grille se rapproche de la tension de seuil (fonctionnement proche du seuil) et l'hypothèse selon laquelle la charge d'inversion varie approximativement linéairement avec l'overdrive de la tension de grille devient de moins en moins précise. Ainsi, un objectif supplémentaire est le développement d'une méthodologie qui permet l'extraction des paramètres des MOSFETs sur la gamme de tension de grille complète permettant de décrire la transition entre les regions en dessous et au dessus du seuil, malgré la réduction de la tension d'alimentation.

Tout d'abord, on présente une nouvelle méthodologie sur la gamme de tension de grille complète en utilisant un modèle de charge d'inversion basé sur la fonction de Lambert W, pour extraire les paramètres électriques des dispositifs FDSOI MOSFET à l'échelle nanométrique. Les mesures de la capacité-tension par la technique Split-CV, effectuées sur les dispositifs FDSOI de technologie de 14 nm, montrent que la variation de charge d'inversion avec la tension de grille peut être bien décrite par la fonction de Lambert W (Figure 1).

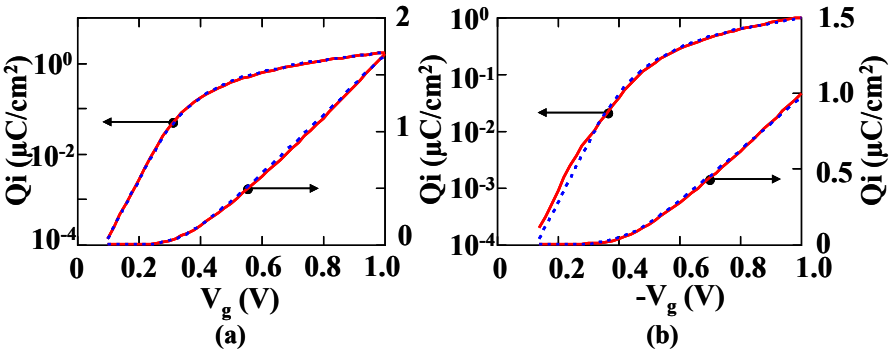

Figure 1: Caractéristiques $Q_i(V_g)$ expérimentales (lignes solides) et modélisées (lignes pointillées) des MOSFET FDSOI à canal de type n (a) et p (b) avec largeur de canal W = 10 µm et longueur de canal L = 3 µm. Les résultats modélisés ont été obtenus en utilisant les paramètres: C_{ox} = 2,6×10^{-6} F / cm^2, n = 1,37 et V_t = 0,30 V pour les dispositifs n-MOS (a) et C_{ox} = 1,44×10^{-6} F / cm^2, n = 1,53 et V_t = 0,34 V pour les dispositifs p-MOS (b).

Basé sur l'équation du courant de drain dans la région linéaire, comprend qui la charge d'inversion décrite par la fonction de Lambert de la tension de grille et l'équation standard de la mobilité, l'extraction de cinq paramètres électriques des MOSFETs est accomplie par les caractéristiques expérimentales de transfert (facteur d'idéalité, tension de seuil, mobilité de champ faible, facteurs d'atténuation de la mobilité de première et deuxième ordre). Les paramètres extraits ont été comparés à ceux extraits par la fonction Y bien connue dans la région d'inversion forte. Cette nouvelle méthodologie pour l'extraction des paramètres électriques des MOSFETs a été vérifiée sur une large gamme de longueurs de canaux (Figure 2) et des tensions de grille arrière sur des dispositifs FDSOI à nano-échelle, démontrant sa simplicité, sa précision et sa robustesse.

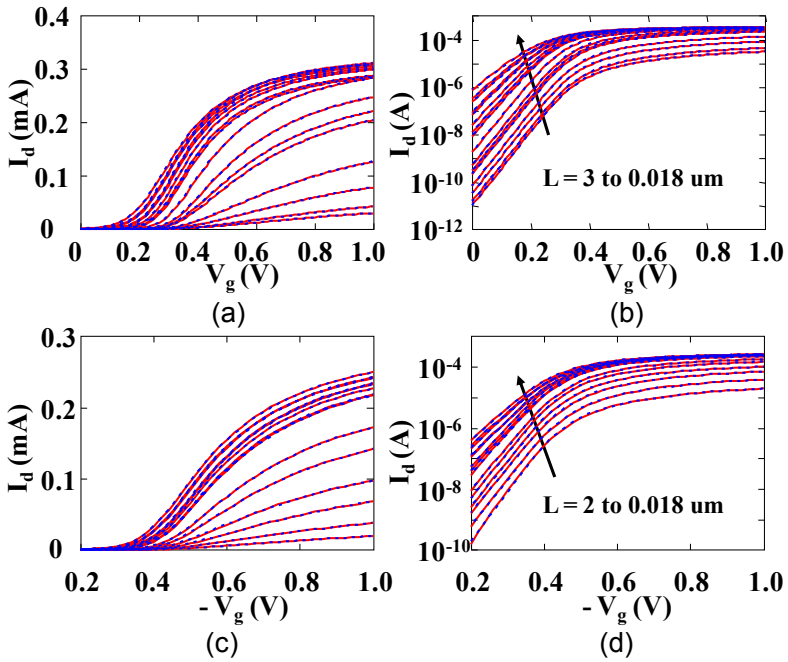

Figure 2: Caractéristiques $I_d(V_g)$ expérimentales (lignes solides) et modélisées (lignes pointillées) à V_d = 30mV des dispositifs FD-SOI n-MOS (a, b) et p-MOS (c, d) en linéaire (a, c) et à échelle logarithmique (b, d) avec des longueurs de grille L allant de 18 nm à 3 µm et largeur de canal W = 10 µm fixée.

Deuxièmement, on a dérivé des expressions simples pour la valeur minimale des potentiels de surface de la grille avant et arrière avec lesquels on a développé des modèles

analytiques pour les tensions de seuil respectives et les facteurs d'idéalité avec le contrôle de la grille arrière des MOSFETs UTBB FDSOI à canaux courts légèrement dopés. Les modèles de tension de seuil et de facteur d'idéalité des grilles avant et arrière ont été vérifiés avec des simulations numériques en termes de paramètres de géométrie des dispositifs et de tensions de polarisation appliquées, ainsi qu'avec des résultats expérimentaux pour des dispositifs avec une longueur de canal de 17 nm. Basé sur ces modèles nous avons développé un modèle de courant de drain compact et analytique pour les MOSFETs UTBB FDSOI à l'échelle nanométrique, légèrement dopés avec contrôle de la grille arrière. Le modèle, qui comprend les effets de l'abaissement de la barrière induite par le drain (DIBL), la modulation de la longueur du canal (CLM), la vitesse de saturation, la dégradation de la mobilité, le confinement quantique, le dépassement de vitesse de saturation (velocity overshoot) et l'auto-échauffement (self-heating), a été validé en comparant les caractéristiques expérimentales de transfert (Figure 3) et de sortie (Figure 4) de divers dispositifs et diverses conditions de polarisation de la grille arrière. La bonne précision du modèle le rend adapté à la mise en œuvre dans les outils de simulation de circuits. En effet, le modèle compact de courant de drain est implémenté en Verilog-A pour la simulation de circuits fondamentaux dans les simulateurs de circuit.

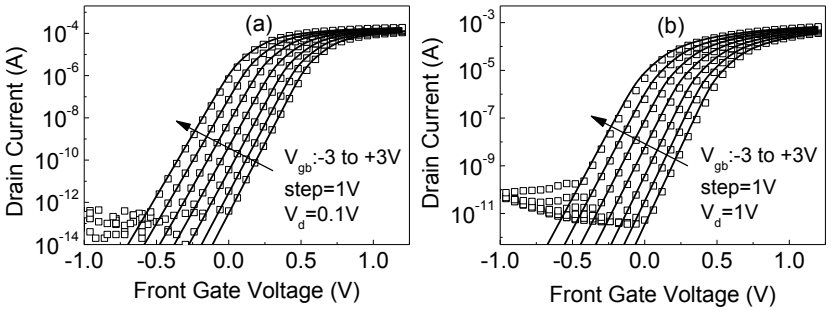

Figure 3: Caractéristiques de transfert expérimentales (symboles) et modélisées (lignes solides) des UTBB FDSOI MOSFETs avec W = 0,5 µm, L = 0,03 µm, t_{Si} = 7 nm et t_{ox} = 1,55 nm, mesurées à la tension de drain 0,1 (a) et 1 V (b) et aux tensions différentes de la grille arrière $V_{gb} = V_b$.

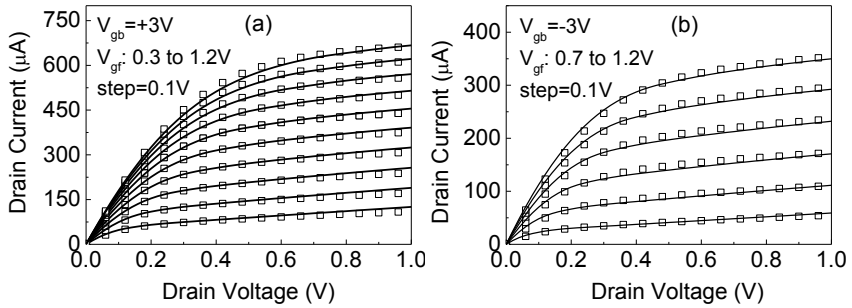

Figure 4: Caractéristiques de sortie expérimentales (symboles) et modélisées (lignes solides) des UTBB FDSOI MOSFETs avec W = 0,5 µm, L = 0,03 µm, t_{Si} = 7 nm et t_{ox} = 1,55 nm, mesurées aux tensions de la grille arrière $V_{gb} = V_b$ = +3 (a) et -3 V (b).

Suite au développement du modèle compact du courant de drain, les problèmes de fiabilité, y compris l'injection de porteurs chauds (HCI) et l'instabilité de la température de polarisation négative (NBTI), sont discutés pour ces MOSFETs UTBB FDSOI à l'échelle nanométrique. L'effet des porteurs chauds, qui se produit près de l'extrémité de drain à cause des porteurs énergétiques accélérés dans le canal, est notable dans les dispositifs n-MOS, tandis que le NBTI est notable dans les dispositifs p-MOS le long de l'ensemble du canal quand une tension de la grille à la source negative est apliquée.

- ✓ Dans notre analyse, les pièges induits par les porteurs chauds (HC) sont étudiés par des mesures de bruit à basses fréquences (LFN) dans les domaines de la fréquence et du temps. Les spectres du bruit mesurés sont composés de bruit 1/f et de type Lorentzien. Le bruit de type Lorentzien vient soit du bruit de génération-recombinaison (G-R), soit du bruit télégraphique aléatoire (RTN). Basé sur les résultats de LFN, l'effet du stress à cause des porteurs chauds est étudié après un stress court et long. L'analyse des pièges de RTN détectés dans les dispositifs frais et dégradés à cause des porteurs chauds indique que l'amplitude de RTN n'est pas corrélée aux constantes de temps de piègeage, c'est-à-dire que l'impact de la profondeur du piège de l'interface est masqué par celui de l'emplacement du piège dans le canal. La totalité des résultats conduisent à une expression analytique pour l'amplitude de RTN, permettant de prédire les changements de RTN de la région sous le seuil à la région au dessus du seuil. Après avoir identifié les mécanismes de dégradation et basé sur notre modèle de courant de drain compact et analytique, on a développé un modèle de vieillissement HC semi-empirique permettant de prédire la dégradation du dispositif stressé dans différentes conditions de polarisation, en utilisant de paramètres uniques déterminés pour chaque technologie extraits par des mesures (Figure 5).

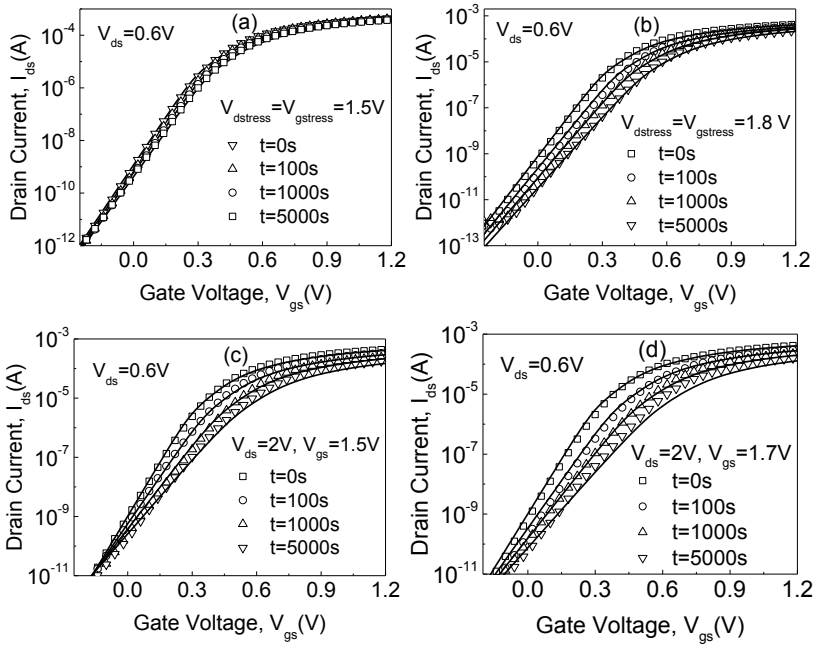

Figure 5: Caractéristiques de transfert expérimentales (symboles) et modélisées (lignes) mesurées à V_{ds} = 0,6 V des MOSFETs FDSOI avec W = 0,5 µm et L = 30 nm, après stress à différentes conditions de polarisation, en utilisant le modèle de mobilité (équation IV.13) et un ensemble unique de paramètres du modèle: C = 5,46, n = 0,277, b = 1,87, c_1 = 3,71 V^{-1}, c_2 = 11,2 V^{-1}, α_1 = 44,76 V^{-1} et α_2 = 7,35 V^{-1}.

- ✓ En ce qui concerne le phénomène NBTI, les déplacements de la tension de seuil pendant le stress à différentes températures et polarisations de la grille montrent que le NBTI est dominé par le piégeage de trous dans des pièges préexistants du diélectrique de grille, tandis que la récupération transitoire suit une dépendance logarithmique en fonction du temps. De cette façon, on a développé un modèle NBTI capturant les dépendances de la température et de la tension de la grille pour ces dispositifs p-MOSFETs UTBB FDSOI avec

une polarisation de la grille arrière égale à zéro et une faible polarisation de drain (Figure 6).

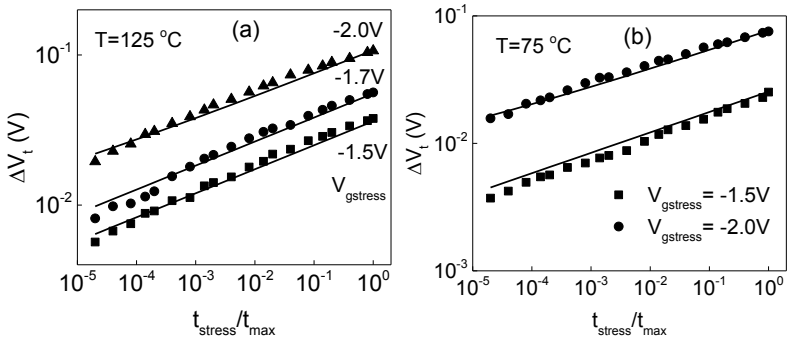

Figure 6: Evolution de ΔV_t avec le temps de stress normalisé t_{stress} / t_{max} des dispositifs UTBB FDSOI p-MOSFETs avec L = 30 nm sous différentes tensions de stress NBTI $V_{gstress}$ à des températures T = 125 °C (a) et 75 °C (b). Les symboles sont les données expérimentales et les lignes sont les résultats du modèle de l'équation IV.16.

Enfin, la dernière partie de notre recherche qui couvre une partie importante de cette thèse traite du phénomène de variabilité locale dans les dispositifs CMOS avancés à l'échelle nanométrique. Les sources principales de la variabilité locale de courants de drain et de grille ont été étudiées en détail. Dans cet aspect, on a développé un modèle de la variabilité locale du courant de drain entièrement fonctionnel, valable pour toutes les conditions de polarisations de grille et de drain, y compris toutes les sources principales de la variabilité locale du courant de drain supposées non corrélées, à savoir les fluctuations locales de la tension de seuil, du facteur de gain de courant, de la résistance série de drain et de source et du facteur d'idéalité de la pente sous le seuil (Figure 7).

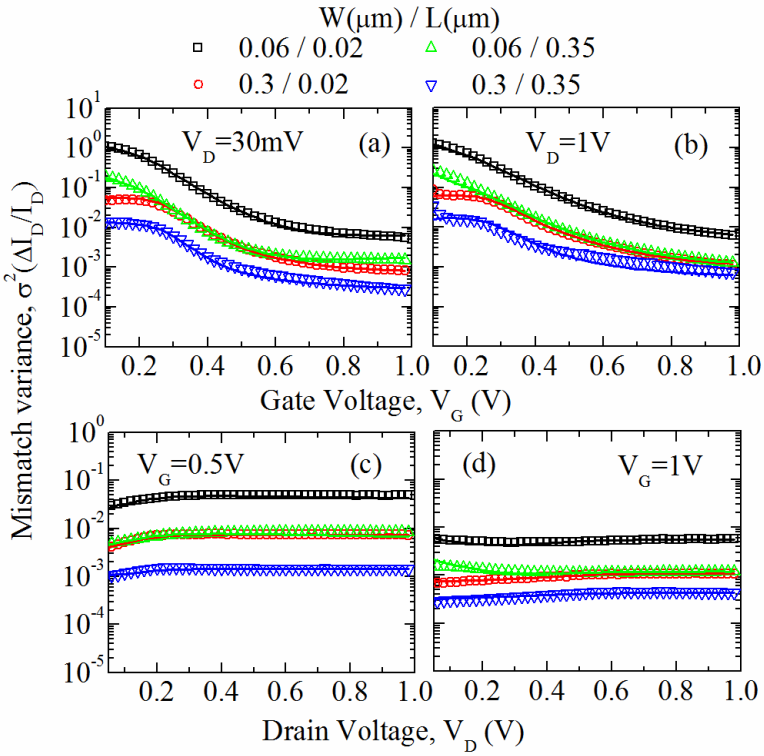

Figure 7: Résultats expérimentaux (symboles) et modèle (lignes) de $\sigma^2(\Delta I_d/I_d)$ en fonction de la tension de grille (a, b) et de la tension de drain (c, d).

En ce qui concerne la modélisation de la variabilité locale du courant de la grille, les fluctuations locales de la tension de seuil et l'épaisseur de l'oxyde de grille ont été prises en compte. Les modèles proposés pour les variabilités locales des courants de drain et de grille ont été vérifiés, en utilisant un modèle compact basé sur la fonction de Lambert W et en effectuant des simulations Monte Carlo qui reproduisent avec précision les variations des courants mesurées expérimentalement. Ensuite, grâce aux modèles de variabilité locale proposés, on a caractérisé diverses technologies avancées en termes de performance de variabilités locale et globale. En effet, on a effectué une caractérisation statistique détaillée de la variabilité locale et globale du courant de drain dans les dispositifs 14 nm Si bulk FinFET et dans les nanofils Si/SiGe sous 15nm. Puis on a extrait les paramètres principaux de la variabilité locale montrant que, malgré leurs dimensions très agressives, ces dispositifs présentent une performance de variabilité locale et globale relativement bonne. En outre, on a étudié l'impact de la résistance série de source et de drain sur la variabilité du courant de drain pour les dispositifs 28 nm bulk MOSFETs. Enfin, on a effectué une étude complète de la variabilité locale des courants de drain et de grille dans les dispositifs FDSOI de 14 nm. En conclusion, ces modèles compacts de la variabilité locale des courants de drain et de grille peuvent être facilement implémentés dans des outils de simulation de circuits pour la conception de circuits et sont applicables aux technologies bulk et FDSOI. De cette manière, notre modèle compact de courant de drain pour les UTBB FDSOI déjà implémenté en Verilog-A, a été utilisé pour examiner l'impact de la variabilité du courant de drain sur les circuits fondamentaux au moyen du logiciel Cadence Spectre.