Digitally controlled CMOS low noise amplifier for adaptative radio

Marcelo de Souza

THÈSE EN COTUTELLE PRÉSENTÉE

POUR OBTENIR LE GRADE DE

DOCTEUR DE

L'UNIVERSITÉ DE BORDEAUX

ET DE L'UNIVERSITÉ TECNOLOGIQUE FEDERALE

DU PARANÁ

ÉCOLE DOCTORALE DES SCIENCES PHYSIQUES ET DE L'INGENIEUR

PROGRAMME D'ETUDES SUPERIEURES EN GENIE ELECTRIQUE ET INFORMATIQUE

SPÉCIALITÉ: ÉLECTRONIQUE

Par Marcelo DE SOUZA

CONCEPTION D'AMPLIFICATEUR FAIBLE BRUIT RECONFIGURABLE EN TECHNOLOGIE CMOS POUR APPLICATIONS DE TYPE RADIO ADAPTATIVE

Sous la direction de Thierry TARIS
et de André MARIANO

Soutenue le 15 decembre 2016

Membres du jury :

M. G. O. BRANTE, Glauber	Professeur	UTFPR, Curitiba	Président
M. NUNES DE LIMA, Robson	Professeur	UFBA, Salvador	Rapporteur
M. RANGEL DE SOUSA, Fernando	Professeur	UFSC, Florianópolis	Rapporteur
M. TARIS,Thierry	Professeur	IMS Bordeaux	Directeur de thèse
M. MARIANO, André	Professeur	UFPR, Curitiba	Co-directeur de thèse

Titre : CONCEPTION D'AMPLIFICATEUR FAIBLE BRUIT RECONFIGURABLE EN TECHNOLOGIE CMOS POUR APPLICATIONS DE TYPE RADIO ADAPTATIVE

Résumé : Les systèmes de communication mobiles permettent l'utilisation de l'information en environnements complexes grâce à des dispositifs portables qui ont comme principale restriction la durée de leurs batteries. Des nombreux efforts se sont focalisés sur la réduction de la consommation d'energie des circuits électroniques de ces systèmes, une fois que le développent des technologies des batteries ne avance pas au rythme nécessaire. En outre, les systèmes RF sont généralement conçus pour fonctionner de manière fixe, spécifiés pour le pire cas du lien de communication. Toutefois, ce scénario peut se produire dans une petite partie du temps, entraînant ainsi en perte d'énergie dans le reste du temps. La recherche des circuits RF adaptatifs, pour adapter le niveau du signal d'entrée pour réduire la consommation d'énergie est donc d'un grand intérêt et de l'importance. Dans la chaîne de réception radiofrequence, l'amplificateur à faible bruit (LNA) se montre um composant essentiel, autant pour les performances de la chaîne que pour la consommation d'énergie. Au cours des dernières décennies, des techniques pour la conception de LNAs reconfigurables ont été proposées et mises en œuvre. Cependant, la plupart d'entre elles s'applique seulement au contrôle du gain, sans exploiter Le réglage de la linéarité et du bruit envisageant l'économie d'énergie. De plus,ces circuits occupent une grande surface de silicium, ce qui entraîne un coût élevé, ou NE correspondent pas aux nouvelles technologies CMOS à faible coût. L'objectif de cette étude est de démontrer la faisabilité et les avantages de l'utilisation d'um LNA reconfigurable numériquement dans une chaîne de réception radiofrequence, du point de vue de la consommation d'énergie et de coût de fabrication.

Mots clés : CMOS, LNA, Haute Linearité, Faible Bruit, Large Bande, Reconfigurable, Gain variable, Sans Inductance, Faible Consommation de Surface, Faible Consommation de Puissance, Faible Coût, Radio Adaptative.

TITLE : DIGITALLY CONTROLLED CMOS LOW NOISE AMPLIFIER FOR ADAPTIVE RADIO

Abstract : Mobile communication systems allow exploring information in complex environments by means of portable devices, whose main restriction is battery life. Once battery development does not follow market expectations, several efforts have been made in order to reduce energy consumption of those systems. Furthermore, radio-frequency systems are generally designed to operate as fixed circuits, specified for RF link worst-case scenario. However, this scenario may occur in a small amount of time, leading to energy waste in the remaining periods. The research of adaptive radio-frequency circuits and systems, which can configure themselves in response to input signal level in order to reduce power consumption, is of interest and importance. In a RF receiver chain, Low Noise Amplifier (LNA) stand as critical elements, both on the chain performance or power consumption. In the past some techniques for reconfigurable LNA design were proposed and applied. Nevertheless, the majority of them are applied to gain control, ignoring the possibility of linearity and noise figure adjustment, in order to save power. In addition, those circuits consume great area, resulting in high production costs, or they do not scale well with CMOS. The goal of this work is demonstrate the feasibility and advantages in using a digitally controlled LNA in a receiver chain in order to save area and power.

Keywords : CMOS, LNA, High Linearity, Low Noise, Wide-band, Reconfigurable, Variable Gain, Inductorless, Low-area, Low-power, Low-cost, Adaptive Radio.

TÍTULO : AMPLIFICADOR DE BAIXO RUÍDO DIGITALMENTE CONTROLADO PARA APLICAÇÕES DE RÁDIO ADAPTATIVO

Resumo : Os sistemas de comunicação móveis permitem a exploração da informação em ambientes complexos através dos dispositivos portáteis que possuem como principal restrição a duração de suas baterias. Como o desenvolvimento da tecnologia de baterias não ocorre na velocidade esperada pelo mercado, muitos esforços se voltam à redução do consumo de energia dos circuitos eletrônicos destes sistemas. Além disso, os sistemas de radiofrequência são em geral projetados para funcionarem de forma fixa, especificados para o cenário de pior caso do link de comunicação. No entanto, este cenário pode ocorrer em uma pequena porção de tempo, resultando assim no restante do tempo em desperdício de energia. A investigação de sistemas e circuitos de radiofrequência adaptativos, que se ajustem ao nível de sinal de entrada a fim de reduzir o consumo de energia é assim de grande interesse e importância. Dentro de cadeia de recepção de radiofrequência, os Amplificadores de Baixo Ruído (LNA) se destacam como elementos críticos, tanto para o desempenho da cadeia como para o consumo de potência. No passado algumas técnicas para o projeto de LNA reconfiguráveis foram propostas e aplicadas. Contudo, a maioria delas só se aplica ao controle do ganho, deixando de explorar o ajuste da linearidade e da figura de ruído com fins de economia de energia. Além disso, estes circuitos ocupam grande área de silício, resultando em alto custo, ou então não se adaptam as novas tecnologias CMOS de baixo custo. O objetivo deste trabalho é demonstrar a viabilidade e as vantagens do uso de um LNA digitalmente configurável em uma cadeia de recepção de radiofrequência do ponto de vista de custo e consumo de potência.

Palavras-chave: CMOS, LNA, Alta linearidade, Baixo Ruído, Banda Larga, Reconfigurável, Ganho Variável, Sem Indutor, Pequena Area, Baixo Consumo de Potência, Baixo Custo, Rádio Adaptativo.

Unité de recherche

Laboratoire d'Intégration du Matériau au Système, UMR 5218, 351 Cours de la Libération 33405 Talence

ACKNOWLEDGEMENTS

To my family, especially my wife, for always supporting and encouraging me. To my parents, my eternal masters, that guided me in the long walk here and always guide me.

I would like to thank CAPES - Brazilian Federal Agency for R&D Support of the Brazil Ministry of Education for facilitating my experience in France.

I would also like to give special thanks to:

My three homes during this time: the Federal Technological University – Parana, UTF-PR, the Federal University of Parana, UFPR, and the Bordeaux University, UB.

My advisors Prof. Dr. André A. Mariano, Prof. Dr. Thierry Taris and Prof. Dr. Volnei A. Pedroni, for the great collaboration in this work. For the technical and personal support, and several hours of work, design and paper reviews. For the opportunity to develop this first cooperation UTF-PR, UFPR, UB.

The professors Oscar Gouveia, Luis Lolis, Bernardo Leite, Sibilla França and members of the Group of Integrated Circuits and Systems – GICS of the UFPR, for the access to the GF 130 nm and the RF circuit development tools. Aside from the help and dedication in important moments.

Magali de Matos and the IMS lab for the chip measurement support.

John Nicot for the paper reviews.

My collegues and friends at the IMS lab.

All the people that helped me directly or indirectly in this work and were not mentioned above.

LIST OF FIGURES

LIST OF FIGURES

LIST OF FIGURES

LIST OF TABLES

LIST OF ABREVIATIONS

ADC	Analog to Digital Converter
BEOL	Back-End-Of-Line
BER	Bit Error Rate
CP1	1dB Compression Point
CMOS	Complementary Metal Oxide Semiconductor
DSP	Digital Signal Processor
F	Noise Factor
IF	Intermediate Frequency
IIP3	Third-order Input Intercept Point
IM3	Third-order Intermodulation Product
FBB	Forward Body Bias
FDM	Frequency Division Multiplexing
FET	Field Effect Transistor
LNA	Low Noise Amplifier
MI	Moderate Inversion
MiM	Metal-Isolating-Metal
MIMO	Multi-Input-Multi-Output
MOS	Metal Oxide Semiconductor
NF	Noise Figure
PA	Power Amplifier
P1dB	1dB Compression Point
PVT	Process, Voltage, Temperature
Q	Quality Factor
RF	Radio Frequency
RMS	Root Mean Square
Rx	Receiver
SAW	Surface Acoustic Wave
SI	Strong Inversion
SoC	System-On-a-Chip
Tx	Transmitter
UWB	Ultra Wide Band
ULP	Ultra Low Power

LIST OF ABREVIATIONS

ULV	Ultra Low Voltage
VLSI	Very Large Scale Integration
WI	Weak inversion
WSN	Wireless Sensor Network

SUMMARY

SUMMARY

1 INTRODUCTION

The need for communication is part of human nature and long distance communication has being a challenge since the ancient times. In the last two centuries, the telecommunication evolved dramatically, with Maxwell, Hertz, Marconi, and many others who contributed to the development of radio communications we know today. Long distance broadcasting happened and the world got smaller. With market competition, new technologies were developed, lowering costs, and making wireless communications more and more affordable. This evolution changed the world, and since the development of microelectronics, the human societies changed as well. The creation of mobile phones, with AMPS, GSM and CDMA technologies, popularized cell phone systems, allowing millions of people to communicate with each other giving rise to new ways of communication. As wireless devices got more popular, the limited spectrum became a problem, and new ideas were proposed to address this technical challenge. Modulation schemes combined with multiple access mechanism made possible the increase of users over the same limited frequency spectrum. New services were born, short message services (SMS), data communication, multimedia message services (MMS), video calls, and by the middle of the 2000s, the computer and the mobile phones were merged, giving rise to smartphones. With the smartphones the internet actually get into the mobile world, and mobile computers spread out. In these mobile hyper-connected devices, battery life is key, where the success or failure of a product depends on it. Much research effort has been made to increase the energy storage density of batteries. However, the pace of chemical and physical development is not fast enough, so battery life is being extended in a faster pace through power saving from the electronics side. New digital technologies evolving according to Moore's Law, have greatly increased the computation power, with reduced power consumption.

Table 1.1 - Wireless standards for data transmission

	Frequency	Max Range	Max Rate	Modulation	Application
Bluetooth	2.4 GHz	10m	3 Mbit/s	FHSS/GFSK	Headsets, audio, sensor data
GPS/GNSS	1.57 GHz	Several km	50 bit/s	DSSS/BPSK	Navigation /Geolocation
GSM	900, 1800, 1900 MHz	Several km	384 kbps (EDGE)	GMSK	Cellular phone
UMTS	1.9 – 2.1 GHz	Several km	2 Mbit/s	QPSK	Cellular phone
UWB	3.1 – 10.6 GHz	10 m	480 Mbit/s	OFDM	Video transfer
WiFi 802.11 a/b/g/n/ac	2.4 and 5GHz	100 m	11 to 800 Mbit/s	DSSS/OFDM	WLAN
WiMAX	2.3, 2.5 GHz	50 km	25 Mbit/s	OFDM/ 64QAM	WMAN, broadband internet access
WirelessHD	60 GHz	10 m	3 Gbit/s	OFDM/ 16QAM	Video
WirelessUSB	2.4 GHz	10 m	480 Mbit/s	OFDM/ QPSK	USB, video
ZigBee 802.15.4	2.4 GHz	100 m	250 kbit/s	OQPSK	Sensor networks

All these fast evolutions, resulted in the continuous development of wireless standards, as illustrated in Table 1.1, each of them aiming to address a specific requirement: geolocation (GPS,GNSS), wireless sensor networks (WSN), metropolitan area networks (WMAN), wireless local area networks (WLAN), wireless personal area network (WPAN), to name a few. Short or long range, low or high data rate, the power consumption and cost remain the key factors for any standard adoption and success.

1.1 A BRIEF STORY OF WIRELESS STANDARDS

A new telephony technology generation has appeared approximately every 10 years and reached its peak 20 years after launch, as shown in Figure 1.1. Each generation typically refer to non-backward-compatible cellular standard, meaning that it shall use different infrastructure and spectrum. The first generation (1G), represented mostly by the Analog Mobile Phone System (AMPS) standard, operating in the 850 MHz band, featured heavy and expensive devices, with only voice capability. The AMPS employed Frequency-Division Multiple Access (FDMA) and paved the

way to commercial cellular systems allowing a large number of user throughout the deployment of cells and the local frequency reuse.

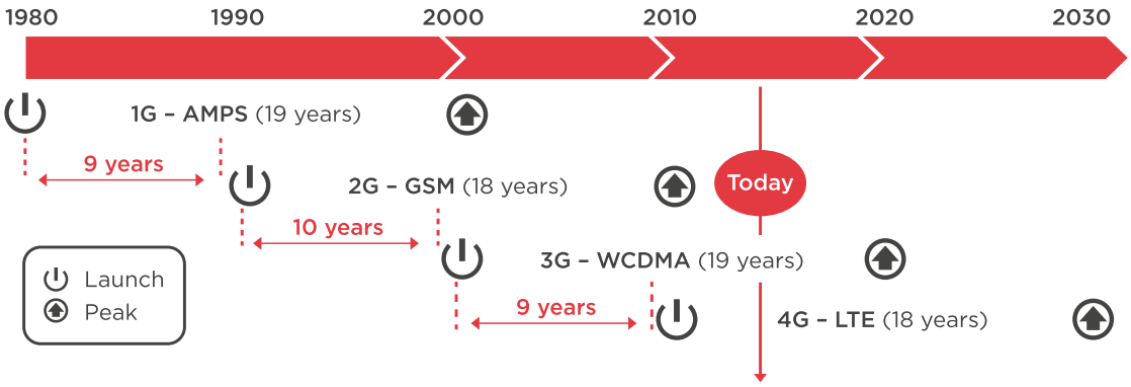


Figure 1.1 – Evolution of mobile technology by generation
Source: (GSMA, [s.d.])

By the early 1990s the 2G emerged, with Global System for Mobile Communication (GSM) in the Europe, in the 900 MHz band, and later the Interim Standard 95 (IS-95) in the USA, in the 850 MHz. With the development of GSM, the DCS and PCS subsystems emerged, including the 1800 and 1900 MHz bands. These standards employed different access schemes to increase the number of simultaneous users, the Time-Division Multiple Access (TDMA) in combination with FDMA with 200kHz channel, and the Code division Multiple Access (CDMA), with 1.25 MHz channel width, respectively. These standards initially provided voice and very low data rates services only. Later with the development of the Internet and the increasing need for data communications, extensions to the GSM and IS-95 were released. The General Packet Radio Service (GPRS) and the Enhanced Data Rates for GSM Evolution (EDGE), on the GSM side, increased the data rates of 2G up to 40 times.

The 3G began in the early 2000s with the evolutions of 2G standards, Universal Mobile Telecommunication System (UMTS) and CDMA2000 were developed to replace GSM and IS-95 respectively. Operating on the 1900 MHz to 2100 MHz band, both standards use CDMA based access method, the UMTS employed Wideband CDMA (W-CDMA) with a pair of 5 MHz wide channels, while the CDMA2000 used one or more available 1.25 MHz channels for each direction of communication. On the 3G, the data rates were increased a ten-fold from the 2G.

In 2004 a 4G standard was developed by the 3GPP and standardized by the ETSI. The Long Term Evolution (LTE), introduced in 2008, is the access part of the

Evolved Packet System (EPS). The LTE was developed as a natural evolution of UMTS and CDMA2000 systems. The main requirements for the new access network are: high spectral efficiency, high peak data rates, short round trip time, as well as flexibility in frequency and bandwidth (3GPP, [s.d.]). The EPS is purely IP based, where both real time services (voice and video) and data communication services are carried by the IP protocol. The new access method is based on Orthogonal Frequency Division Multiple Access (OFDMA). In combination with higher order modulation (up to 64QAM), large bandwidths (up to 20 MHz), and spatial multiplexing in the downlink (up to 4x4), it achieves high data rates. The highest theoretical peak data rate on the transport channel is 75 Mbps in the uplink, while in the downlink, the rate can be as high as 300 Mbps.

The 5G is expected to be launched in the early 2020s. However, there is a significant debate on what 5G is and what is not. According to GSMA (GSM Association) there are two possible visions of the technology (GSMA, [s.d.]):

1. The hyper-connected vision: Mobile operators would create a blend of pre-existing technologies covering 2G, 3G, 4G, WiFi and others to allow higher coverage and availability, and higher network density in terms of cells and devices. Where the key differentiator is the greater connectivity, which would enable Machine-to-Machine (M2M) services and the Internet of Things (IoT). This vision may include a new radio technology to enable low power, low throughput field devices with long duty cycles of ten years or more.
2. Next-generation radio access technology: With specific targets for data rates and latency being identified, such new radio interfaces can be assessed against such criteria. This in turn makes a clear demarcation between a technology that meets the criteria for 5G, and another that does not.

Both of these approaches are important for the progression of the industry, but they are distinct sets of requirements associated with specific new services. To address this issue, many industry initiatives have worked on identifying a set of eight basic requirements for this generation:

- 1-10Gbps connections to end points in the field (i.e. not theoretical maximum)
- 1 ms end-to-end round trip delay (latency)

- 1000x bandwidth per unit area
- 10-100x number of connected devices
- (Perception of) 99.999% availability
- (Perception of) 100% coverage
- 90% reduction in network energy usage
- Up to ten year battery life for low power, machine-type devices

Because these requirements are specified from different perspectives, they do not make an entirely coherent list – it is difficult to conceive a new technology that could meet all of these conditions simultaneously.

Parallel to the development of mobile cellular communication systems, other wireless standards focusing on data transfer were developed and gain importance in the telecommunication domain. Among them, the most successful are the short-range Bluetooth and medium range WLAN (WiFi) standards. Initiated in the late 1980s and standardized in 1999, the Bluetooth standard was developed with focus on low cost, low power consumption and up to 10 m range. Operating in the 2.4 GHz ISM band, it used Frequency Hopping Spread Spectrum (FHSS) access method with 1 MHz channel width, GFSK modulation, it achieves up to 1 Mbit/s. In 1997, the IEEE established the 802.11 WLAN standard, with 22 MHz channel width, operating at the 2.4 GHz ISM band, it used the Direct Sequence Spread Spectrum (DSSS) modulation and reached up to 2 Mbit/s in a range of 100 m. Recent revisions of this standard as 802.11n and 802.11ac, operate at 2.4 GHz and 5 GHz bands, with channels up to 160 MHz wide, Multi-Input Multi-Output (MIMO) OFDM modulation, reaching 800 Mbit/s over a range of 35 m. Besides these standards, other systems emerged, such as the long range Worldwide Interoperability for Microwave Access (WiMAX or IEEE 802.16). Initially designed to reach 30 Mbit/s and deliver last-mile broadband services, WiMAX yields 1Gbit/s in short distances, or a few of MBit/s up to 50 km. The IEEE 802.16m revision of the standard, was developed for use in ITU's IMT-Advanced recommendation and is a competitor of LTE-Advanced on the 4G.

All these wireless data standards are considered as complementary to cellular ones, and there is a strong need for interoperability between them. Multifunction terminals, gathering a maximum of standards in an optimized way, have emerged over the last decade. Such hyper-connected devices are expected to provide a

seamless connectivity anywhere at any time. Nowadays a smartphone is supposed to cover more than 15 standards located in a 0.4 GHz to 6 GHz band, as illustrated in Figure 1.2.

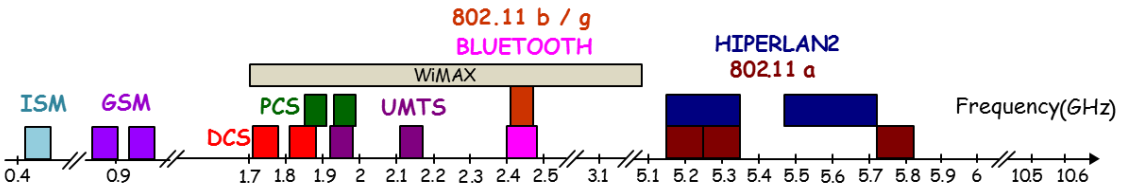


Figure 1.2 – Continuous development wireless standards

The increasing demand for higher data rates, wider bandwidths, higher integration and lower power consumption draw the canvas of this thesis work.

1.2 RADIO CONCEPT IN SMARTPHONE: OVERVIEW AND LIMITATION FOR THE FUTURE

Nowadays we find many connected devices in our environment. By 2019, 5 billion of them, including smartphones, tablets and laptops, are expected to co-exist with a 9% yearly growth. Such a huge number of devices will broaden the service and the quality of service (QOS), the data traffic will grow by 57% per year, reaching almost 25 Exabytes per month. As shown in Figure 1.3, mobile video will represent about 80% of this traffic. This demand for more data rate, calls for more bandwidth, higher complexity modulation schemes, MIMO and carrier aggregation techniques.

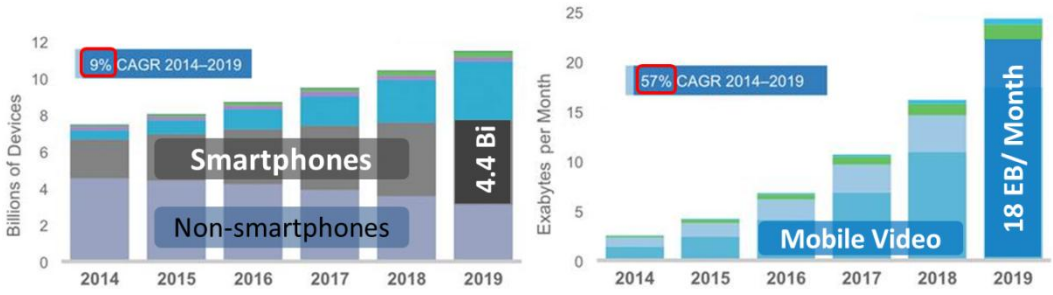


Figure 1.3 – Number of smart devices and mobile video expected growth
Source: Adapted from (CISCO, 2016)

To address this purpose multi-standard Tx/Rx architectures are actually implemented with several single band/standard transceivers on the same chip as illustrated in Figure 1.4, for the WiFi/Bluetooth chip of iPhone 5S (Apple). However, the

competitive market of smartphone pushes harder toward low cost developments, low power consumption and high quality systems. These restrictions put strict challenges on the development of future radio that the basic concept of current transceivers cannot address. Some of these points are first introduced and discussed now.

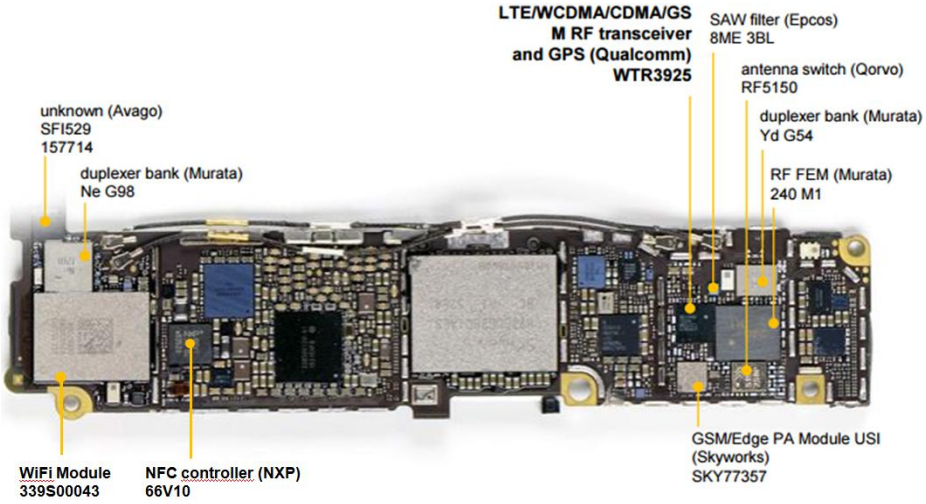


Figure 1.4 – Apple iPhone 6S board showing the multi-chip RF design. Source: (CHIPWORKS INC., 2015)

Recent smartphones are still implemented with multi-chip architectures. Where each group of standards, with defined and fixed frequency bands, is implemented in a different chip as illustrated in Figure 1.4, for the case of a 2.4/5GHz WiFi. This strategy is expensive, and do not allow upgrading, since the processing of a new standard or frequency band, not originally planned, requires the design of a new circuit and the sale of a new device, hindering flexibility. (MOY; PALICOT, 2015). Furthermore, redundant low noise amplifiers, mixers and frequency synthesis modules significantly increase the overall power consumption of such devices. Therefore, the multi-chip/multi-front-end solution is not sustainable over the long term. Even a recent work, shown in Figure 1.5 (GEORGANTAS et al., 2015), with integrated power amplifiers, and variable gain LNAs, still do not cover geolocation or data standards, so one or more chips are needed to cover all the needed standards.

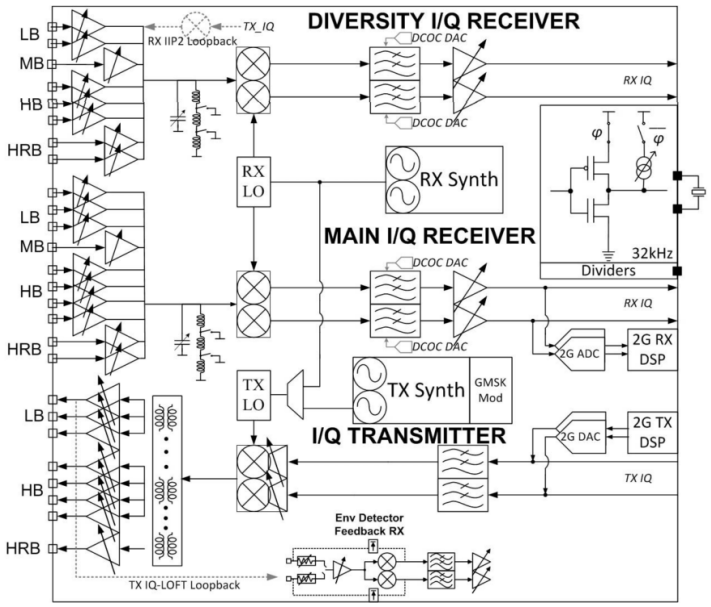


Figure 1.5 – Broadcom 13mm^2 40nm GSM/EDGE/HSPA+/TDSCDMA/LTE Transceiver
Source: (GEORGANTAS et al., 2015)

These transceivers features multiple receiving paths and are placed on the single die, with a fair number of external passive devices such as SAW filters and switches scattering off-chip, as shown in Figure 1.6. Passive devices can be integrated with the silicon die using 3-D stack-up packaging to save the board area. However, the cost of System-In-Package (SiP) is still prohibitively high for wide adoption (CHEN, 2009).

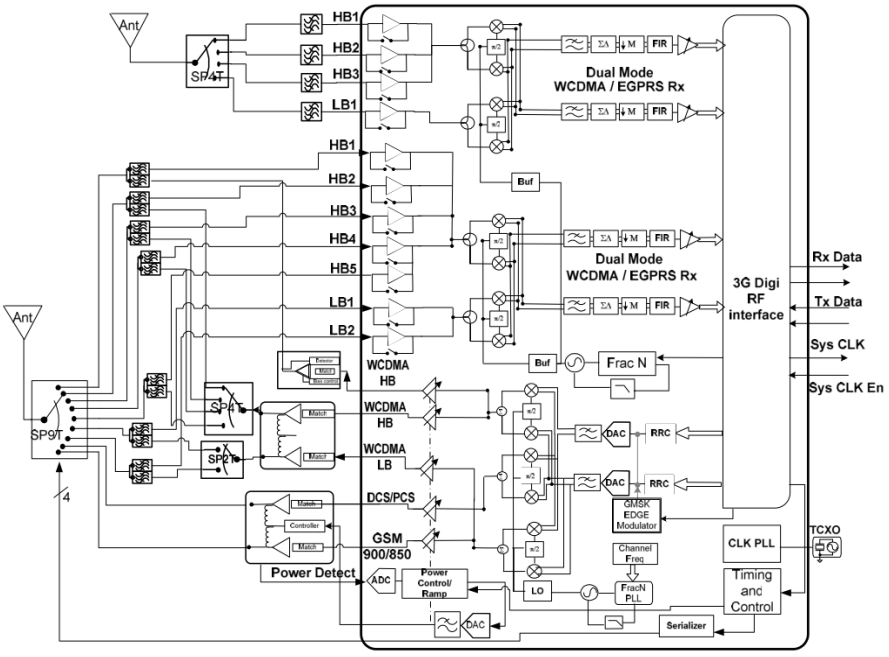


Figure 1.6 – Skyworks Digital RF 3G transceiver
Source:(SOWLATI et al., 2009)

The power consumption of such chips is not optimized, as their radio performances, at system level, are designed and fixed for the worst-case scenario (LOLIS et al., 2015). For example, if a phone is close to a base station, the signal would be strong but the receiver would amplify it expending the same amount of power as it would if the signal were weak, wasting battery energy.

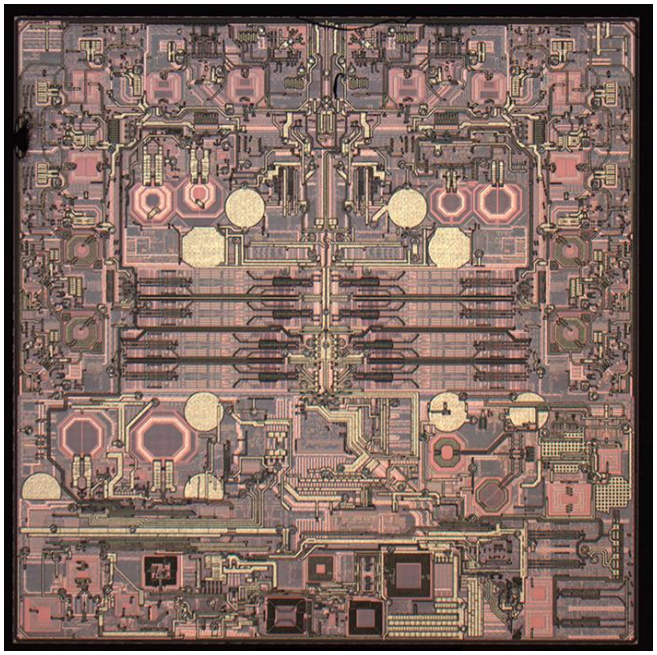


Figure 1.7 – Qualcomm WTR3925 die. 28 nm RF transceiver used in Samsung Galaxy S6 and Apple iPhone 6S
Source: (TECHINSIGHTS INC., 2015)

These RF blocks use many inductances, which are implemented on silicon for cost saving and a reduction of footprint. However, the size of the integrated inductors remains large compared to active devices that significantly limit the density of integration of RF systems as illustrated in Figure 1.7. Whereas the speed of transistor directly benefits from technology shrink, the quality of passive devices, and especially inductors, does not improve at all. The analog performance of MOS devices degrade with the reduction of the gate length. Short channel effects, DIBL, velocity saturation, flicker noise and linearity deteriorate for each new CMOS generation. Moreover, the radio specifications of modern devices become more stringent at each generation. A new approach in RF circuits and systems is required to address the challenge of future radio implementation in advanced CMOS Process.

1.3 A BRIEF ON RX ARCHITECTURES

A wireless communication system uses electromagnetic waves propagation properties to transmit information over the air (Figure 1.8). After radiation by the antenna, the modulated signal travels away from transmitter being subject to several perturbations (attenuation, distortion) due to scattering, fading, multipath interference, and other propagation effects.

Figure 1.8 – Wireless communication system, transmitter and receiver

The signal received by the antenna shall be transposed back to a low frequency range so the information can be extracted. This is the down-conversion process or demodulation, which is carried out by the RF receiver chain.

1.3.1 Conventional Receivers and Limitations

Over the years, several RF receiver architectures were proposed. They are all derived from one of the 3 most popular solutions which are: the heterodyne, the homodyne and the low-IF architecture. These 3 basic architectures are based on a same concept of RF analog signal processing represented in Figure 1.9. The signal collected by the antenna is first filtered by a high-Q pass band filter to select the standard of communication. The Low Noise Amplifier (LNA) is responsible for the sensitivity of the receiver, and a part of the RF gain. The frequency down conversion embedding a mixer and a frequency synthesis shifts the RF band to low frequency. This operation enables the channel selection by filtering. The Voltage Gain Amplifier (VGA) adapts the signal dynamic to the scale of the Analog to Digital Converter (ADC).

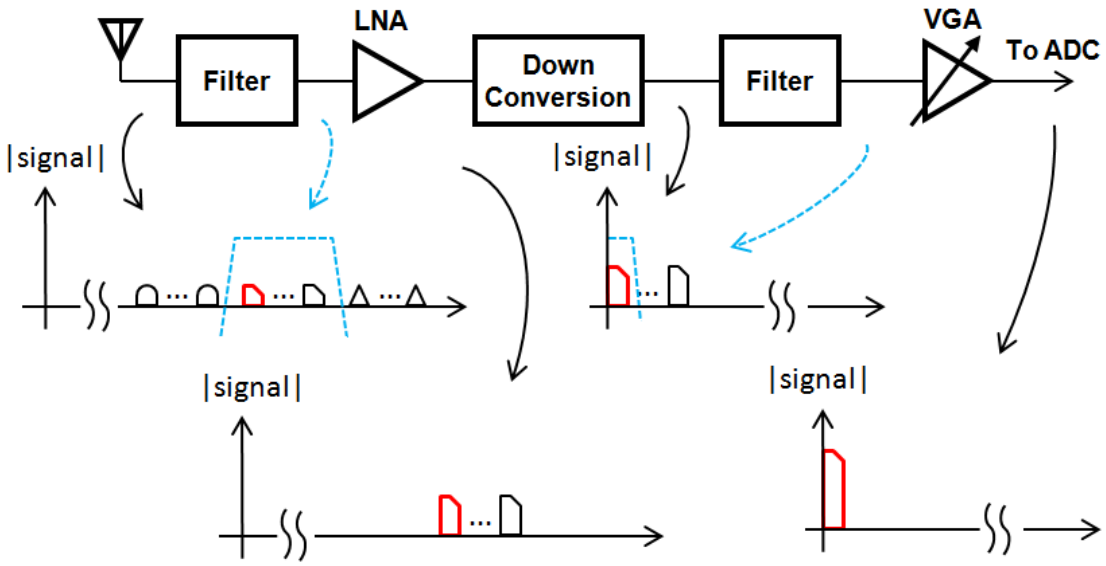


Figure 1.9 – Conventional RF Analog Signal processing in a receiver

The heterodyne class of receivers features a two-step frequency down conversion as illustrated in Figure 1.10.a). The first mixer in Figure 1.10 shifts the signal to an intermediate frequency (IF) equals to 1.28 GHz. It is further filtered out by the Surface Acoustic Wave (SAW) and amplified by the PGA before the second, and final, frequency down conversion. The IF step generates the folding of the image frequency which requires a high-Q pass-band filter before the first mixer to attenuate the image. The problem of image rejection was lately solved with the Weaver architectures presented in Figure 1.10.b). The processing of the RF signal with parallel and quadratic paths cancels out the image. The image rejection filter is no longer needed which improves the integration and flexibility of heterodyne receiver. The large number of high-Q pass band filter remains a limitation in terms of integration, sensitivity, reliability and flexibility.

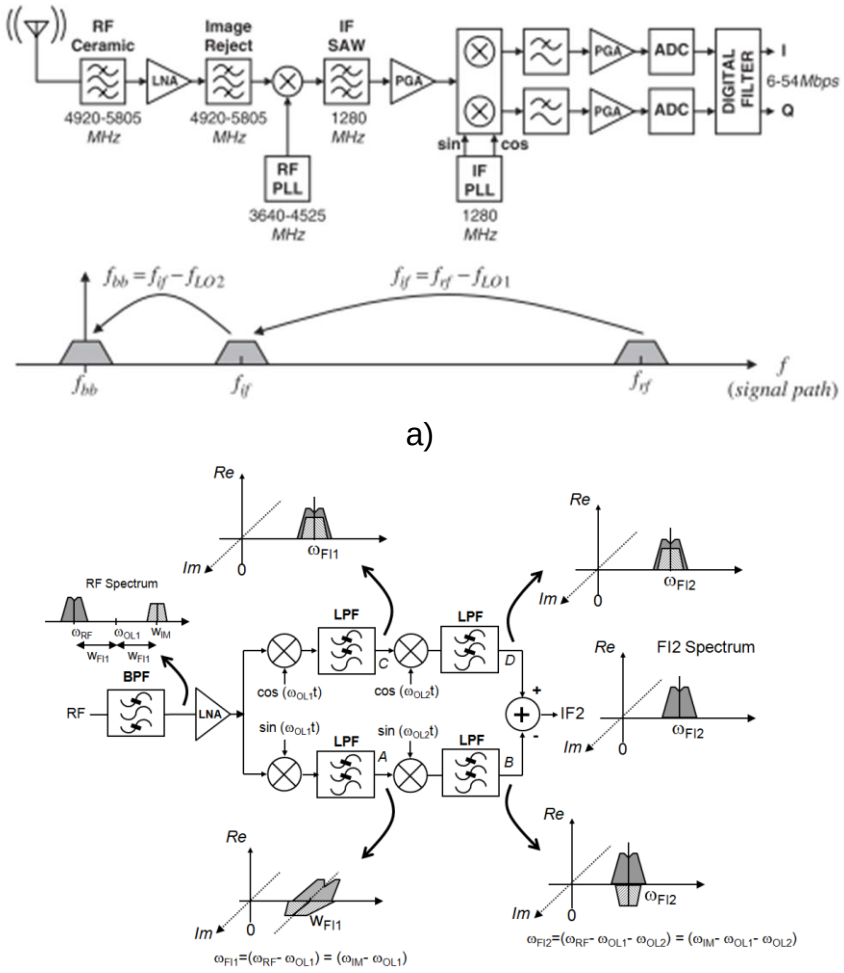


Figure 1.10 – a) Super-heterodyne receiver. b) Principle of Weaver receiver. Source: (BEHZAD, 2007)

The problem of image rejection does not occur in the homodyne receiver, Figure 1.11. Indeed the RF signal is directly down converted to base band by selecting a local oscillator (RF PLL in Figure 1.11) at the same frequency of the RF signal, hence the image is the signal itself. The high integration and low power consumption of homodyne receiver makes it interesting for radio implementation. However, it has several drawbacks among them are: the sensitivity to flicker noise, the desensitization due to DC-offset, the need for high linearity to name a few.

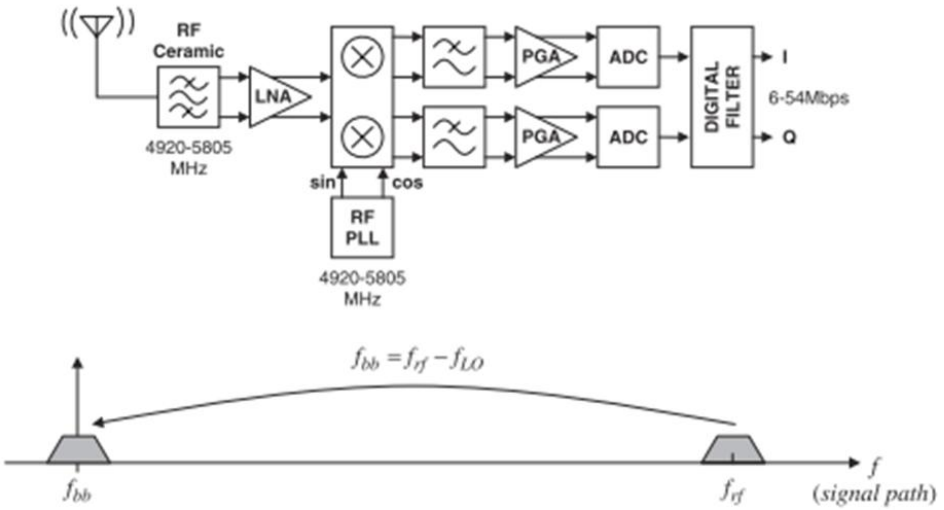


Figure 1.11 – Homodyne 802.11a receiver
Source: (BEHZAD, 2007)

The concept of the Low IF receiver is close to the principle of the direct-conversion architecture: the signal is directly translated to baseband to be filtered and demodulated after analog to digital conversion. However, the IF is not zero, it is equals to 2 or 3 time the channel bandwidth. This frequency plan makes the low IF receiver less sensitive to flicker noise and DC offset generation. However, this architecture reintroduces the problem of image rejection inherent in heterodyne receivers. To solve it a poly-phase pass band filter is introduced after the complex down-conversion, Figure 1.12.a). It allows for image rejection and channel selection. Indeed the combination of I/Q paths, Figure 1.12.b), in the polyphase filter yields a complex processing of the signal which results in a filtering of the negative frequency attenuating the image, as illustrated in Figure 1.12.c). Nowadays the low IF receiver is a very popular architecture since it features the best trade-off in terms of performance, cost and integration compared to heterodyne and homodyne receivers.

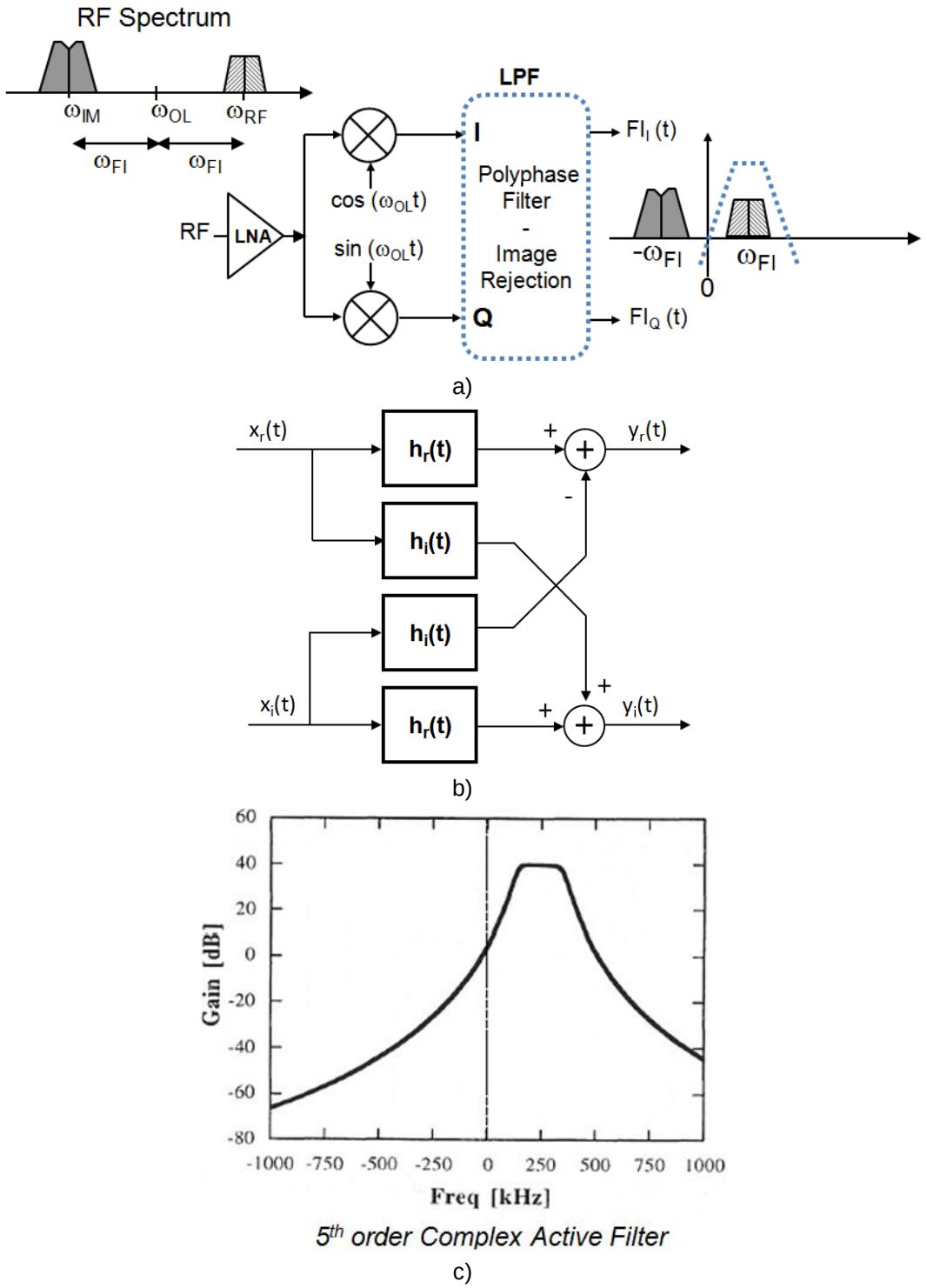


Figure 1.12 – a) Low IF receiver. b) General description of a polyphase filter. c) frequency response of a 5th order active band-pass complex filter.

The conventional receivers described in this section, and their derived versions, feature the radio module of our wireless devices. The principle of frequency down conversion by RF mixing with a local oscillator is narrowband by nature. To address a multi-band operation several receivers are parallelized as illustrated in Fi-

gure 1.6. This approach is definitely suited to address the challenge of a wideband, adaptive and low cost radio. The next section reports on some new approaches of RF signal processing which circumvent most of the standard architecture issues.

1.3.2 Multi-standard/multi-band receiver Rx Architectures attempts

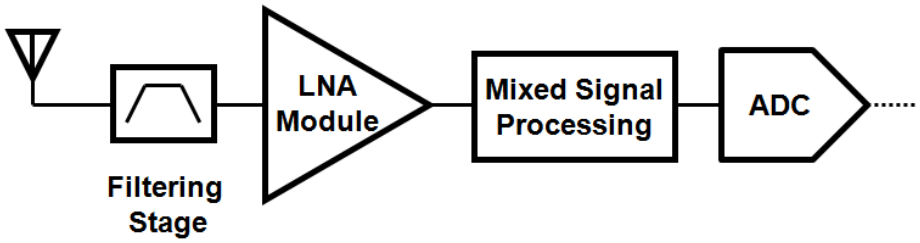


Figure 1.13 – The concept of an adaptive radio receiver

The Software Radio (SR), a concept introduced by Mitola (MITOLA, 1995), is actively being researched as a promising solution to address the challenge of multi-band/multi-standard flexible radio. This concept, illustrated in Figure 1.13, is to replace the standard RF analog signal processing – implemented with RF mixers, frequency synthesizer, base-band filters and automatic gain control loops – by a high frequency mixed-signal processing module. As SR applications are still in their infancy, many solutions are being developed in current literature to perform digital/mixed signal processing. To name a few: a) the subsampling track-and-hold architecture (DEVRIES; MASON, 2008). Using a sample and hold circuit clocked at a lower frequency than the incoming RF carrier signal, it allows the use of a much lower power synthesizer compared to a direct conversion or low-IF receiver, which requires an RF PLL. Targeted to the 900 MHz band, it consumes 7.7 mW, has a NF of 8 dB, with image frequency attenuation of 25 dB. b) The RF-sampling architecture, shown in Figure 1.14 (GEIS et al., 2010), where the output of a gain programmable multiband LNA is sampled at full Nyquist rate of the signal's carrier. After the sampling process a strong shaped band-pass FIR filter, is applied before the signal is down-converted by means of subsampling. Consuming 115 mW, it covers the GSM, UMTS and WiMAX (3GHz) standards, with BW selection from 200 kHz to 20 MHz. It reaches NF of 5.1 dB, with gain in the -2 dB to 60 dB range. It also presents in-band IIP3 of +1 dBm and out-of-band (OOB) IIP3 of -3 dBm. c) The N-path filter receiver of Figure 1.15 (CHEN; HASHEMI, 2014), (ZHU; KRISHNASWAMY; KINGET, 2015) exploits a discrete time switched capacitor array to achieve High-Q filtering at RF frequency

together with a down conversion over a wide frequency range. Consuming up to 600 mW, it covers the 0.5 to 3 GHz frequency range, has NF of 6.8 dB, maximum gain of 35 dB, IB IIP3 of -12 dBm and OOB IIP3 of +11 dBm.

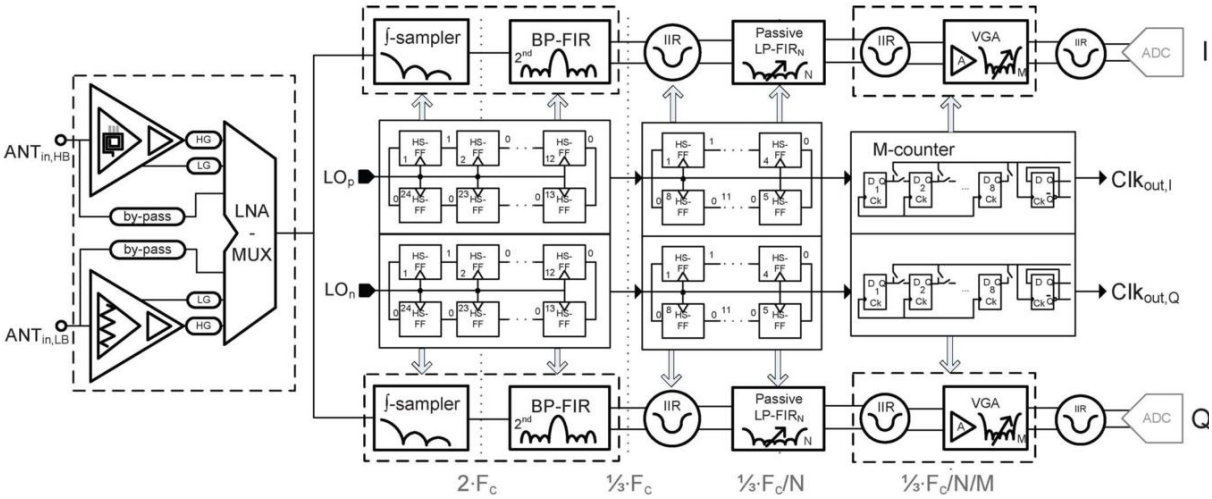


Figure 1.14 – Discrete-time RF-sampling receiver architecture
Source: (GEIS et al., 2010)

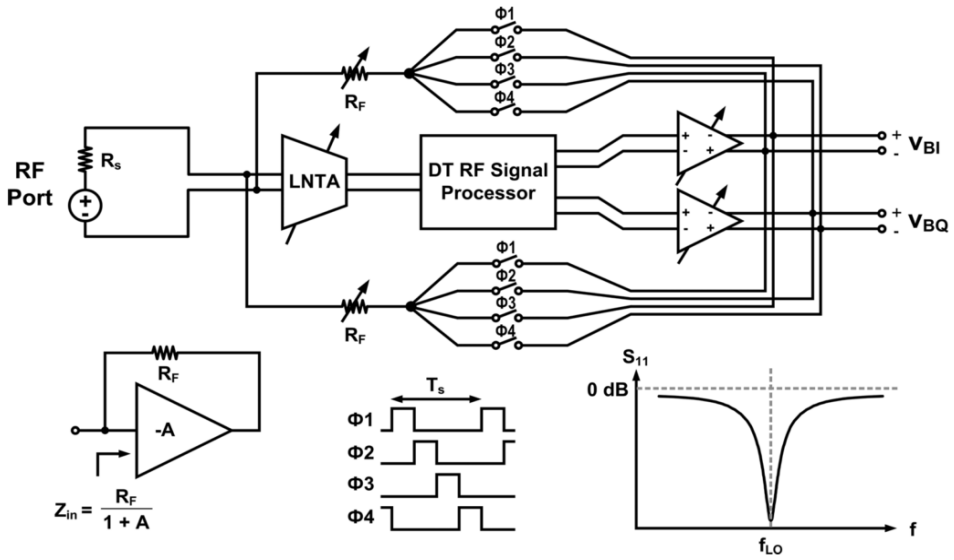


Figure 1.15 – Software-Defined Radio Receiver Using Discrete-Time RF Signal Processing
Source: (CHEN; HASHEMI, 2014)

More solutions based on very different approaches are reported in the literature. None of them clearly dominates because they cannot achieve a complete set of performance in terms of: bandwidth/resolution bandwidth, blocker tolerance/Linearity, dynamic range and power consumption due to system complexity. Interestingly, they all features a low noise amplification module before digital/mixed signal processing to adjust, at least, the dynamic of the signal and the signal-to-noise ratio.

1.4 LNA BASICS : FROM SYSTEM APPROACH TO CIRCUIT METRICS

The low noise amplifier (LNA) is the first active block of the receiver chain. It is placed after the band selection filter. Its function is to amplify the signal received by the antenna, which is usually very weak (in the range of -100 dBm), with minimum distortions (moderate 3th order Intermodulation Point (IP3)), and without introducing too much noise (low Noise Figure) to preserve the signal to noise ratio. The gain of the LNA must be large enough to minimize the noise contribution of the subsequent stages (see Appendix A). Together with the topology choice, the noise matching and the input matching contribute to achieve a large gain and a low noise figure. The linearity is supported by the architecture of the LNA.

To cope with a low power consumption, a small silicon footprint and the increasing number of wireless standards, the research efforts currently focus on the development of broadband, highly linear and reconfigurable LNA for the concept of SR receiver presented in Figure 1.16.a). This reconfigurable low noise amplification module is expected to achieve the behavioral response proposed in Figure 1.16.b) which includes:

- An adjustable wideband response
- A sliding/tunable narrow-band response
- Allow a variation of the voltage gain and the noise figure
- A control of the linearity

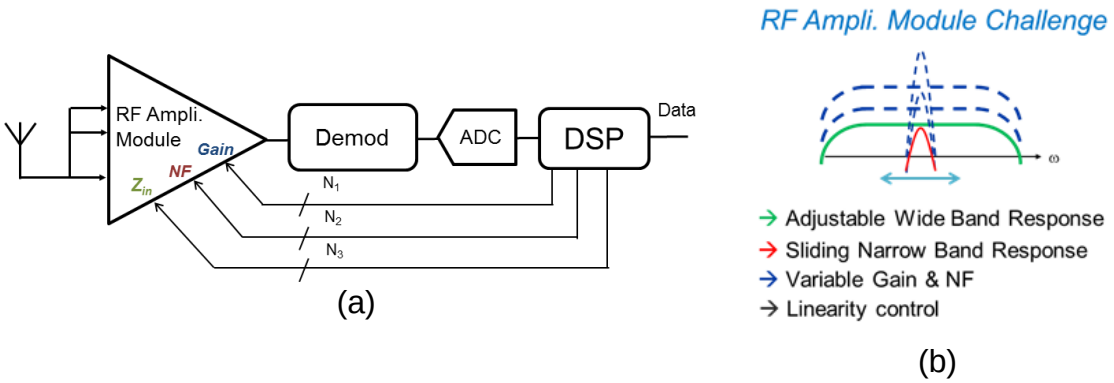


Figure 1.16 – Reconfigurable receiver and the adaptive RF amplifier challenge

This work aims the development of a generic, wideband LNA, with a digital tuning of the performance. To reduce the silicon footprint, and the cost of implementation, an inductorless architecture is preferred. The LNA will address at least 8 different communication standards: WCDMA, E-GSM, DCS, PCS, WLAN (2.4GHz and 5GHz), Bluetooth, WiMAX and LTE. The specifications, in terms of voltage gain, noise figure (NF) and linearity (IIP3), required for each standard (ATALLAH et al., [s.d.]; BRANDOLINI et al., 2005; INIEWSKI, 2007), are summarized in Table 1.2, and are referred to the worst-case scenario for the radio link – i.e. maximum sensitivity and high linearity. A power saving can be obtained if the receiver does not need to demodulate all the standards at the same time, or if the radio link conditions improve. For instance, if the level of the blockers is low, the IP3 can be reduced, or if the level of desired signal is higher than the minimum required for sensitivity (high SNR_{in}), the NF specification can be relaxed. In such scenarios, the LNA is able to be adapted to the radio link conditions, and to operate with reduced power consumption.

Table 1.2 - LNA requirements by wireless standard

	Frequency Band (MHz)		Requirement		
Standard	**Low**	**High**	**Gain (dB)**	**NF (dB)**	**IIP3 (dB)**
WCDMA	1920	2170	18	2	0
E-GSM	880	960	18	3	-5
DCS	1710	1800	18	3	-5
PCS	1850	1990	18	3	-5
WLAN (2.4GHz)	2400	2483	18	3	-5
WLAN (5 GHz)	5150	5850	18	3	-5
WiMAX	1700	5000	20	3	-10
Bluetooth	2400	2480	18	5	-5
LTE	700	3800	18	5	-10

1.5 RESEARCH GOAL AND THESIS ORGANIZATION THIS

This research focuses on the design of low-power, low-area and wideband reconfigurable CMOS LNA suitable for adaptive multi-standard/multi-band radios. Even if the design methodology for inductor based narrowband LNA has been well explored in the literature for the last two decade, the correlation between low noise, linearity and broadband impedance matching of inductorless LNA, still needs to be

investigated to work out the right tradeoff. Moreover, the wideband operation of the LNA, in a multi-standard/multi-band scenario, requires higher linearity performance than the conventional specifications defined for each standard. This constraint calls for advanced and new circuit techniques. Furthermore, the orthogonal control of the LNA characteristics would give more flexibility to the receiver. All these considerations draw the framework of this thesis that is organized as follows:

- Chapter 2 reviews inductorless LNAs and reconfiguration techniques. Two solutions are proposed and analyzed through the derivation of the LNA characteristics.
- Chapter 3 introduces the design guide proposed to explore the LNA design space, and to define the device sizes with respect to a set of specifications.
- Chapter 4 exposes the measurement results of the two inductorless reconfigurable LNA prototypes developed in 130nm CMOS technology. Through a large set of measurement in different mode of operation, the optimum configurations are worked out and discussed. Besides some specific scenario are proposed to test the circuit tolerance to concurrent standard blockers.
- Chapter 5 draws conclusions of this research and discussions for future investigations.

2 PROPOSED TOPOLOGY

This chapter introduces the state of the art on wideband and reconfigurable LNAs. Next, the proposed topology is presented with a detailed analysis of the performance. Due to the low cost requirement presented in Chapter 1, only inductorless wideband solutions are discussed.

2.1 WIDEBAND INDUCTORLESS LNA TOPOLOGIES

The impedance matching presents a crucial step in LNA design to guarantee a good trade-off between gain and noise factor (GIRLANDO; PALMISANO, 1999). The challenge is to achieve a high voltage gain $(\mathrm{A_V})$ and a good input matching (Z_{in}) over the band of interest, with a low power consumption (P_{DC}). The state of the art of wideband LNA topologies will be discussed focusing on the basic configurations shown in Figure 2.1. In this section, the existing wideband LNA families will be presented along with a comparison of the different advantages and disadvantages of each structure.

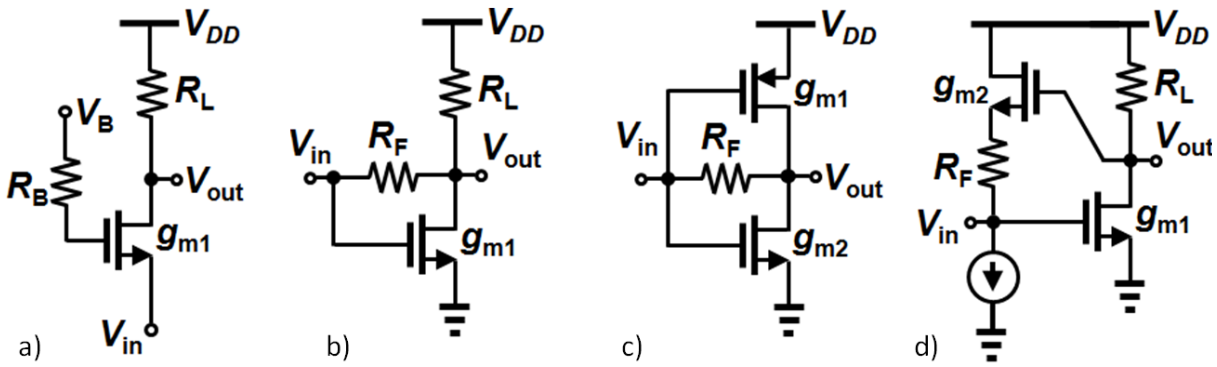


Figure 2.1 – Inductorless LNA structures. a) Common-gate b) Resistive SFB c) Current-reuse d) Active SFB.

In the state of the art, single-ended inductorless LNAs are based on either common-gate (CG) topology (Figure 2.1.a), or shunt-feedback (SFB) architectures (Figure 2.1.b, Figure 2.1.c, Figure 2.1.d).

Common-gate (CG) amplifiers, Figure 2.1.a), enable both high gain and low input impedance as g_{m1} increases:

$$A_V = +g_{m1}(R_L||r_{o1}) \tag{1}$$

$$Z_{in} = \frac{1}{g_{m1}} \tag{2}$$

Input matching is achieved over a wide frequency range when $g_{m1} = R_S^{-1}$, which results in $g_{m1} = 20\,mS$ for a source impedance of 50Ω. The power consumption P_{DC} is basically fixed by the source impedance and is still large for low power applications. Some g_m-boosted solutions have successfully alleviated this compromise by exploiting the complementary nature of differential topologies (BELMAS; HAMEAU; FOURNIER, 2012; HAN; JUNG; KIM, 2015; SOBHY et al., 2011). Unfortunately, this approach makes the design of the antenna and front-end RF filter difficult, and sensitive to mismatching.

Figure 2.1.b) shows the resistive shunt feedback amplifier (SFB) (CHEN; LIU, 2012; PERUMANA et al., 2008). Applying the KCL in the loop we find

$$g_{m1}V_{in} = \left(\frac{-V_{out}}{R_L}\right) + \left(\frac{V_{in} - V_{out}}{R_F}\right) \tag{3}$$

The voltage gain found solving (3) for V_{out} and V_{in},

$$A_V = \frac{V_{out}}{V_{in}} = -G_m R_{out} \tag{4}$$

where, the effective transconductance is $G_m = \left(g_m - \frac{1}{R_F}\right)$ and the output resistance is $R_{out} = (R_F||R_L)$, or accounting for channel length modulation $R_{out} = R_F \| R_L \| r_o$. The input impedance Z_{in} is defined by the ratio of the feedback resistance R_F and the voltage gain A_V. The input matching is achieved when $R_F = R_S(1 + |A_V|)$ according (5).

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{\left(\frac{V_{in} - A_V V_{in}}{R_F}\right)} = \frac{R_F}{1 - A_V} = \frac{R_F}{1 + |A_V|} \approx \frac{R_F}{|A_V|} \tag{5}$$

This structure presents a trade-off between V_{DD} and A_V, as a higher value of R_L requires a higher value of $V_{DD}$for the same drain current. It also presents a compromise between A_V and R_F as the latter shunts the output thus reducing the output resistance. Lower values of R_F reduces the effective transconductance and reduces A_V (TARIS; BEGUERET; DEVAL, 2007).

To circumvent this problem, the resistive load R_L in Figure 2.1.b) is replaced by a PMOS transistor M_2 in the current-reuse (CR) structure Figure 2.1.c) (EL-NOZAHI et al., 2011). M_1 and M_2 biased with the same DC current act as a current source for the other, and the configuration of Figure 2.2.a) is equivalent to the two half circuit of Figure 2.2.b). For small signal analysis the current reuse stage is modeled as a resistive SFB stage biased by a single current source as illustrated in Figure 2.2.c).

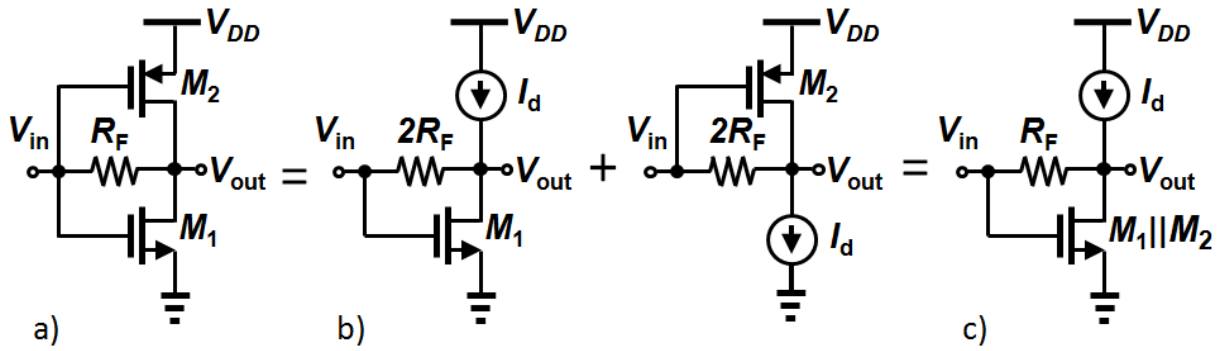


Figure 2.2 – CR small signal model. a) CR b) Superposition of two ideal resistive SFB c) Final model of the resistive SFB with a single transistor combining M1 and M2 in parallel driven by a ideal current source.

The voltage gain is the same as the resistive SFB with:

$$G_m = g_{m1} + g_{m2} - 1/R_F \tag{6}$$

and

$$R_{out} = R_F \| r_{o1} \| r_{o2} \tag{7}$$

Neglecting the channel length modulation and assuming $R_F \gg 1/(g_{m1} + g_{m2})$, it yields:

$$A_V \approx -R_F(g_{m1} + g_{m2}) \tag{8}$$

The magnitude of the voltage gain is proportional to R_F, capable of reaching very high values. The matching criterion, further defined in Table 2.1, imposes $g_{m1} + g_{m2} = \frac{1}{R_S}$, which leads to :

$$A_V \approx -\frac{R_F}{R_S} \tag{9}$$

In practice, channel length modulation reduces the output resistance and the maximum achievable gain. The input impedance is highly capacitive due to the gate

to source capacitors of M1 and M2, and the bandwidth is limited. Still, this topology achieves the highest A_V/P_{DC} ratio of any single stage amplifier configuration, which makes it interesting for low power applications.

Another approach to minimize the trade-off between A_V and Z_{in} is the active SFB which introduces a source follower along with R_F, as illustrated in Figure 2.1.d) (BELOSTOTSKI; MADANAYAKE; BRUTON, 2012; CHEN et al., 2008; RAMZAN; ANDERSSON, 2007; WANG; ZHANG; YU, 2010). The trade-off between A_V and R_F is relaxed as the feedback transistor M_2 does not drain current from the output. The voltage gain is the same as the resistive SFB with:

$$G_m = g_{m1} \tag{10}$$

and,

$$R_{out} = R_L \| r_o \tag{11}$$

And,

$$A_V = -g_{m1} R_L \tag{12}$$

The input impedance is the ratio of R_F and the resistance viewed at the source of M_2 over the voltage gain:

$$Z_{in} = \frac{1 + g_{m2} R_F}{g_{m2}(1 + |A_V|)} = \frac{\left(\frac{1}{g_{m2}} + R_F\right)}{1 + |A_V|} \approx \frac{\left(\frac{1}{g_{m2}} + R_F\right)}{|A_V|}, \tag{13}$$

The input matching is completed if

$$g_{m2} = \frac{1}{R_S(1 + |A_V|) - R_F} \tag{14}$$

The active SFB of Figure 2.1.d) achieves good performance in terms of gain, NF and input matching over a wide bandwidth. Unfortunately the combination of active feedback with a resistive common source amplifier introduces some distortions which significantly degrade the linearity of the LNA (BORREMANS et al., 2008).

Table 2.1 summarizes the voltage gain, input impedance and matching conditions of each basic inductorless topology in the state of the art.

Table 2.1 – Indutorless LNA summary

	R_{out}	A_V	Z_{in}	Matching condition
Resistive SFB	$R_L \| R_F \| r_{o1}$	$-\left(g_{m1} - \frac{1}{R_F}\right) R_{out}$	$\frac{R_F}{1 + \lvert A_V \rvert}$	$R_F = R_S(1 + \lvert A_V \rvert)$
Active SFB	$R_L \| r_{o1}$	$-g_{m1} R_{out}$	$\frac{1 + g_{m2} R_F}{g_{m2}(1 + \lvert A_V \rvert)}$	$g_{m2} = \frac{1}{R_S(1 + \lvert A_v \rvert) - R_F}$
Common-Gate	$R_L \| r_{o1}$	$+g_{m1} R_{out}$	$\frac{1}{g_{m1}}$	$g_{m1} = \frac{1}{R_S}$
Current-Reuse	$R_F \| r_{o1} \| r_{o2}$	$-\left(G_m - \frac{1}{R_F}\right) R_{out}$	$\frac{R_F}{1 + \lvert A_V \rvert}$	$g_{m1} + g_{m2} = \frac{1}{R_S}$

Table II sums up the discussion about the pros and cons of the basic configurations for the implementation of wideband low power and highly linear LNA.

Table 2.2 – Classical LNA topologies comparison.

Topology	Gain	NF	Linearity	Consumption	Integration	Bandwidth	High frequency impedance matching
Resistive termination	Moderate	High	High	High	High	wide	Low
Common-gate	Moderate	Moderate	High	Moderate	High	wide	Moderate
Resistive SFB	Moderate	Moderate	Moderate	High	High	wide	Moderate
Current-reuse	High	Moderate	High	Low	High	wide	Moderate
Active SFB	Moderate	Moderate	Moderate	Moderate	High	wide	High

The resistive termination architecture responds to the high integration requirements as it embeds few passive components. However, it is not suited for wideband operation due to the significant degradation of the noise figure at high frequencies. The same argument holds for the resistive feedback architecture, which also exhibits a large power consumption. These two topologies are finally not relevant since they achieve average performance and do not comply with the low power requirement.

The common-gate architecture is interesting in terms of linearity and gain. However, the minimum noise figure is limited to 3.5 dB, which is too large for some standards.

The current-reuse architecture achieve high gain, low power consumption but its noise performance and impedance matching pose as limiting factor to meet higher frequency standards requirements. The active feedback topology, however, shows

good balance among most of the characteristics being limited by its linearity and gain.

In this work, we combined the current-reuse and active shunt feedback topologies, taking advantage of the positive aspects of each one, creating a novel LNA architecture, called from now on Gyrator-like architecture (DE SOUZA; MARIANO; TARIS, 2015). This structure is used as the core of all 3 prototypes fabricated and is used to demonstrate the feasibility of a compact, low-power, performance reconfigurable LNA.

2.2 RECONFIGURABLE LNA TECHNIQUES

Chapter 1 shows that an adaptive receiver needs a LNA that enables the reconfiguration of its Gain, NF, IIP3 and operating frequency. In the state of the art, most of the solutions address at most two of these parameters, generally in a non-orthogonal manner, as will be shown next.

2.2.1 Biasing control

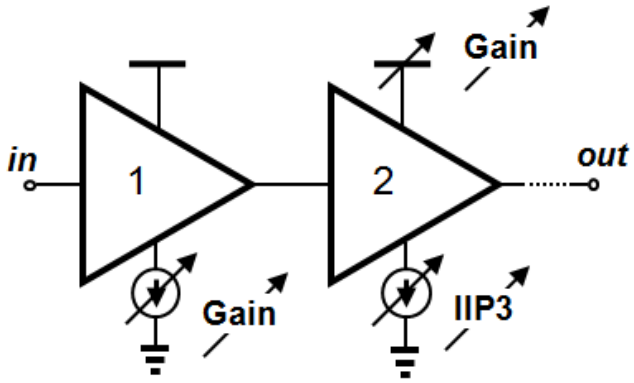


Figure 2.3 – LNA reconfiguration: Bias control.

The first approach exploits the control of bias conditions through current steering and, or, V_{DD} variation to reconfigure the LNA performance.

A generic 2-stage LNA is represented in Figure 2.3 with some solutions of bias control of the state of the art. The variation of bias current/V_{DD} only concerns the reconfiguration of the gain and the linearity.

A variable gain LNA featuring a two stage stacked cascade in common-source configuration is presented in (WANG; LU, 2005). These stages reuse the same bias current, achieving a high A_V/P_{DC}, thus enabling power saving. The circuit

is implemented in 180 nm CMOS technology and the gain control is achieved by the bias voltage of the second stage. The prototype reaches 8 dB gain control range, with maximum gain of 16.4 dB, 1 GHz bandwidth, NF of 3.5 dB and P_{DC} of 3.2 mW.

In (ZHANG; KINGET, 2006) a programmable gain distributed LNA is proposed. Fabricated in 180 nm CMOS, composed by three cascode stages, it presents 8.6 dB gain through a 7 GHz bandwidth and gain control range of 20 dB, including 10 dB attenuation. With minimal NF of 4.2 dB, IIP3 of +3 dBm, power consumption of 9 mW, it occupies a large 1.16 mm^2 area. The gain control is made through the analog variation of cascode gate voltages. It presents large bandwidth and linearity, however uses a large silicon area.

(SEN et al., 2012) propose an LNA with orthogonal gain and IIP3 control, through the bias currents of each stage. The circuit uses two stages, being the first a complementary resistive feedback amplifier and the second a source-follower amplifier. The gain is changed through the variation of the bias current, while the IIP3 is controlled the variation of the bias current of the second stage. Despite the interesting orthogonal capabilities, the performances of the fabricated circuit are moderate. Implemented in 180 nm CMOS, the circuit shows poor input impedance matching ($|S_{11}| \geq -6$ dB), low gain ($S_{11max} = 12.8$ dB) and bandwidth (BW = 1 GHz). The power consumption varies between 18 mW and 39 mW and the IIP3 between -26 dBm and -9.7 dBm, which is insufficient for most wireless portable applications.

2.2.2 Impedance control

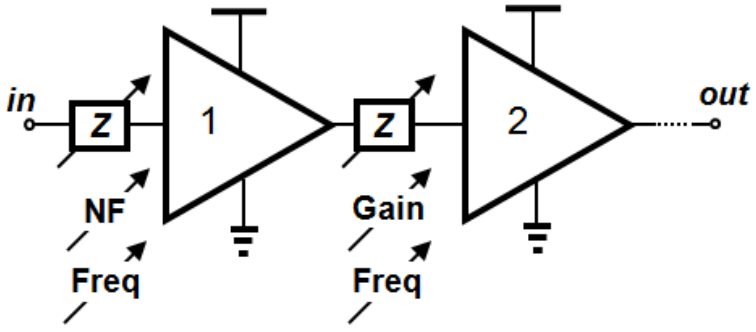


Figure 2.4 – LNA reconfiguration: impedance control.

The second approach exploits the variation of impedance to reconfigure the LNA. Figure 2.4 illustrates some solutions of LNA reconfiguration through impedance variation. The control of the input impedance changes the power and noise matching, the frequency response and NF of the LNA are reconfigured and after possibility is to

insert a variable load between the LNA stages. The gain and the frequency response can be controlled with this technique.

Reported in (EL-NOZAHI; SANCHEZ-SINENCIO; ENTESARI, 2009), a variable input impedance LNA was implemented in 130 nm CMOS, and is composed of an inductive degenerated cascode (IDC) amplifier, with adjustable narrowband input matching network. It achieves the continuous selection of the matching frequency through an analog control voltage. The NF is minimized at the selected matching frequency while the gain remains almost independent of the selection. The BW remains in about 500 MHz with very little central frequency shift. This circuit, however, is not fully integrated, it uses three external inductors and two integrated inductors, which result in great silicon area consumption. The LNA achieves NF between 3.2 dB and 3.7 dB, IIP3 of -6.7 dBm with P_{DC} of 17 mW. This solution renders the popular IDC topology frequency reconfigurable. However, it is limited to this particular topology. It is difficult to integrate and shows a noise performance worse than other topologies.

(HSIEH et al., 2011) proposes a wideband amplifier operating in the 60 GHz band, it uses attenuation cells at output of the first stage and input of the second stage to digitally control the gain. Moreover, this circuit uses positive feedback, to increase the bandwidth without gain decrease. In the first stage, the attenuation cell digitally connects resistors in parallel changing the effective load, and thus the gain, without altering the input matching circuit. The gain control is achieved without any benefit on power consumption, which remains in 45 mW regardless the configuration used.

In (FU et al., 2008), an LNA which combines two techniques: bias control and impedance variation is presented. Implemented in 130 nm CMOS, allows reconfigurable operating frequency and gain. With a 0.49 mm^2 area, is composed by two stages and the measurement buffer. In the first stage, a broadband amplifier with controllable output DC level employing double reactive feedback. This DC level is used to change the biasing of the second stage, controlling the IIP3 from -18.2 dBm to -9.7 dBm. The second stage is a cascode amplifier, where the frequency selection is achieved by the combination of a varactor and an integrated multi-tapped inductor. The gain is controlled from 10.5 dB to 24.8 dB, through current steering in a binary-segmented transistor, where the switches are connected to sources of the transistor to reduce the parasitic loading. This circuit presents five operating frequencies (2.40,

3.43, 3.96, 4.49 and 5.40 GHz) and three operating mode each, high gain (HG), low gain with enhanced linearity (LG1), low gain - low power (LG2). The frequency sub-bands are superposed so that between frequency selections, the gain is in a 3 dB range, what ensures covering the whole 2.4 to 5.4 GHz band with less than 3 dB gain variation. In HG mode it consumes 4.6 mW, while in LG2 the power consumptions reaches 3.1 mW. This LNA presents low power consumption and good level of reconfigurability, with frequency, gain and IIP3 selected independently. However, it requires two large inductors, one of them with a complex segmented layout. Another important aspect is that the switches at the sources of the segmented transistor in the second stage slight degrade the performance by adding parasitic resistive degeneration to the amplifier.

2.2.3 Adaptive feedback

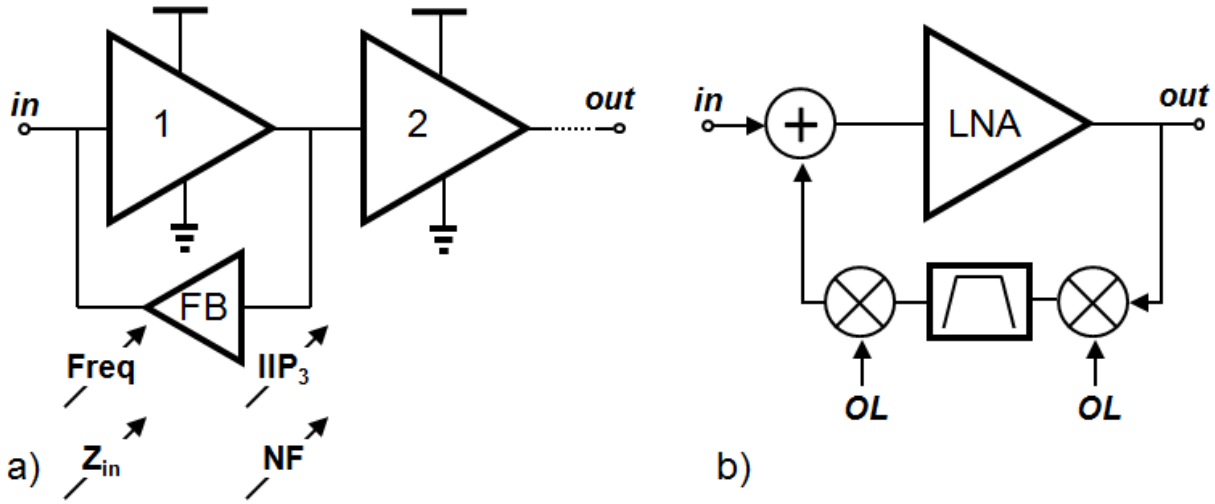


Figure 2.5 – LNA reconfiguration: a) adaptive feedback. b) N-Path filter LNAs

The third technique is only compatible with the LNA topologies, featuring a feedback path, as illustrated in Figure 2.5.a). The feedback (FB) is reconfigured to change the LNA performances: input matching, linearity, frequency response and noise figure. FB can be implemented as a translational transfer function, such as an N-path filter, as shown in Figure 2.5.b).

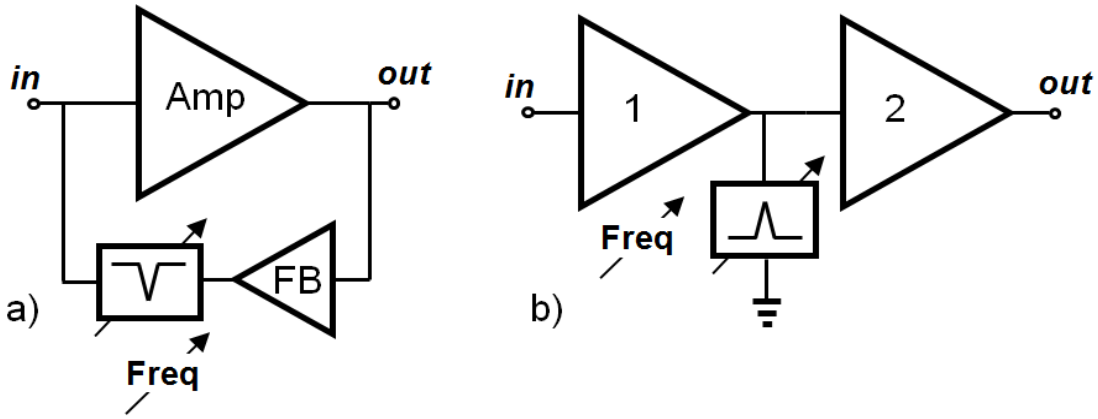


Figure 2.6 – N-Path filter LNAs. a) Notch-filter in the feedback b) Band-pass filter as the load of the first stage

With the development of technological nodes smaller than 65 nm in recent years, very low capacitance and resistance switches became available, and a technique from the 1960s could be used in RF, the N-path filters (FRANKS; SANDBERG, 1960). Figure 2.6.a). shows a family of N-path filter based LNAs, a feedback LNA with a notch filter in the feedback path (PARK; RAZAVI, 2014; ZHU; KRISHNASWAMY; KINGET, 2015). This allows the selection of the operating frequency with great selectivity (300 kHz < BW < 20MHz), increasing linearity and enabling the creation of receivers resistant to strong blockers (0 dBm). These can be implemented without band filters and called SAW-less receivers. Figure 2.6.b). shows another approach for the N-path filters, a band-pass filter is added after the first stage changing the load behavior, that presents high value in the pass-band and low impedance in the stop-band (HEDAYATI et al., 2015). This allows frequency selection and moderate power blocker filtering, however, in the presence of high power blockers the NF is heavily degraded (NF ≈14 dB). In both cases, the central frequency can be very largely, according to the frequency of the phase generators driving the filters. However, depending on the type of filter, this switching frequency can be as high as 8 times the center frequency, which results in high power consumption in the frequency synthesizer.

The frequency selection and blocker filtering of N-path filters look very promising. However, a scaled technology ($L \leq 65$ nm) is required for its implementation and the additional power consumption of the high frequency phase generators can be prohibitive for low power circuits.

This study shows that no solution address all the reconfigurability identified needs. Most of the reconfigurable LNAs were designed focusing on frequency selection or gain variation to avoid saturation of subsequent stages. On one side, they allow the reconfiguration of at most two characteristics concurrently, and on the other, the control is rarely orthogonal. This leads to our proposal of a topology capable of reconfiguration of gain, NF, IIP3 and power consumption. Where, this control must be as orthogonal as possible. This is one objective of this thesis.

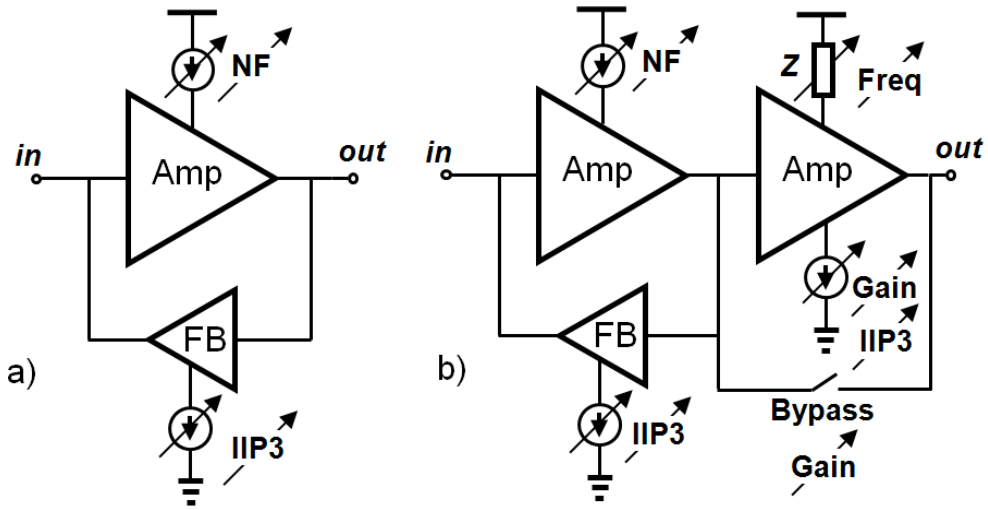


Figure 2.7 – Proposed solutions. a) single-stage inductorless Gyrator-like LNA b) two-stage bandwidth extension fully reconfigurable LNA

Figure 2.7 shows the functional schematics of the proposed solutions. In Figure 2.7.b), a reconfigurable two-stage LNA is proposed. The first stage is a feedback amplifier, the gyrator-like LNA (Figure 2.7.a), the core circuit, is intended to allow control of NF and IIP3, maintaining wideband impedance matching. The second stage is an inductive peaking stage, designed to allow bandwidth extension, coarse frequency selection, gain and IIP3 control. A bypass switch is also proposed to allow power saving when the characteristics of the second stage are not needed, i.e. standards with frequency below 2.4 GHz. These stages will be presented in detail in next sections.

2.3 GYRATOR-LIKE LNA

The gyrator-like LNA architecture is composed of two transconductance stages that exploit the output parasitic capacitances to create an inductive behavior at the input, and cancel out the input capacitances. It combines the CR stage of Figure 2.1.c) with the source follower of Figure 2.1.d), as shown in Figure 2.8.a). Its

small signal equivalent circuit, Figure 2.8.b), resembles the active SFB of Figure 2.1.d), but without the load resistor R_L. The structure works as a gyrator (Figure 2.8.b) and takes benefit of the high A_V/P_{DC} of the CR structure and solve the highly capacitive input impedance.

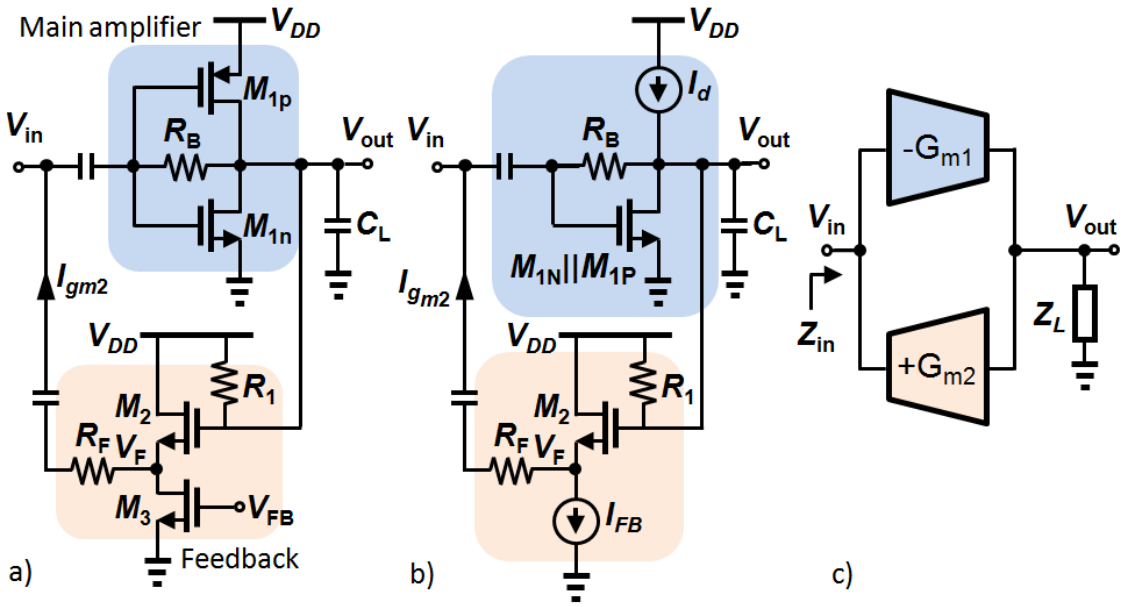


Figure 2.8 – a) Proposed LNA b) small signal equivalent circuit c) gyrator circuit

2.3.1 Gain and bandwidth

The voltage gain of the proposed amplifier in Figure 2.8.a) is given by

$$A_V = -\left(G_{m1} - \frac{1}{R_B}\right) Z_{out} \tag{15}$$

where, $G_{m1} = g_{m1N} + g_{m1P}$, $Z_{out} = R_B \| r_{o1} \| 1/j\omega C_L$ and $r_{o1} = r_{o1N} \| r_{o1P}$.

The gain is maximized when R_B is large, i.e. $R_B^{-1} \approx 0$, and the low frequency gain is

$$A_{VLF} = -G_{m1} r_{o1} \tag{16}$$

The main poles of the circuit are:

$$p_1 = R_S(C_{GS} + C_{pad}) \tag{17}$$

$$p_2 = R_S C_{gd}(1 + A_V) \tag{18}$$

$$p_3 = C_L r_{o1} \tag{19}$$

Then a small C_L is used ($C_L \leq C_{gd}$), p_2 dominates, due to the Miller effect and the high voltage gain of the amplifier. The 3 dB bandwidth is then given by

$$BW = \frac{1}{2\pi(1 + A_V)C_{gd1}R_S} \tag{20}$$

2.3.2 Input impedance

A gyrator, Figure 11.c), presents at its input a reciprocal version of the impedance connected to its output,

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{G_{m1}G_{m2}Z_L} = \frac{Z_L^{-1}}{G_{m1}G_{m2}} = \frac{Y_L}{G_{m1}G_{m2}} \tag{21}$$

When a purely capacitive load $Z_L = 1/j\omega C_L$ is connected to the output, the input impedance becomes: $Z_{in} = j\omega C_L/G_{m1}G_{m2}$, i.e. an inductive impedance is presented at the input of the circuit. This inductive behavior can be used to cancel-out the parasitic capacitances at the input, i.e. capacitances at the gates of the MOS transistors, metal lines and bond pads. However, a purely inductive impedance in not capable of achieving impedance match. The input impedance must be the complex conjugate of the source, i.e. $Z_{in} = Z_S^*$. Considering a load $Z_L = R_L||X_{C_L}$formed by a resistor R_L in parallel with a capacitor C_L, whose admittance is $Y_L = G_L + j\omega C_L$. The input impedance is

$$Z_{in} = \frac{1}{G_{m2}G_{m1}R_L} + j\frac{\omega C_L}{G_{m1}G_{m2}} \tag{22}$$

The real part is constant where as the imaginary part is inductive and grows linearly with the frequency.

Considering that the parasitic capacitance C_{par} are connected in parallel with the source resistance R_S, we find

$$Z_S = \frac{R_S}{1 + \omega^2 R_S^2 C_{par}^2} - j\frac{\omega R_S^2 C_{par}}{1 + \omega^2 R_S^2 C_{par}^2} \tag{23}$$

Imposing the matching condition, we find

$$\frac{1}{G_{m2}G_{m1}R_L} = \frac{R_S}{1+\omega^2 R_S^2 C_{par}^2} \therefore R_L = \frac{1+\omega^2 R_S^2 C_{par}^2}{G_{m2}G_{m1}R_S} \tag{24}$$

$$j\frac{\omega C_L}{G_{m1}G_{m2}} = j\frac{\omega R_S^2 C_{par}}{1+\omega^2 R_S^2 C_{par}^2} \therefore C_L = \frac{G_{m1}G_{m2}R_S^2 C_{par}}{1+\omega^2 R_S^2 C_{par}^2} \tag{25}$$

The values of R_L and C_L are frequency dependent, indicating that impedance matching is only achieved at a specific frequency. However for $\omega^2 R_S^2 C_{par}^2 \ll 1$, which is true for small parasitic capacitances up to several GHz, we have:

$$R_L \approx \frac{1}{G_{m2}G_{m1}R_S} \tag{26}$$

and,

$$C_L \approx G_{m1}G_{m2}R_S^2 C_{par} \tag{27}$$

For $R_S = 50\ \Omega$, $G_{m1} = 100\ \text{mS}$, $G_{m2} = 10\ \text{mS}$ and $C_{par} = 200\ \text{fF}$ we find: $R_L \approx 20\ \Omega$, $C_L = 2.5\, C_{par} = 500fF$. The input impedance behavior is shown in Figure 2.9, where the $Re(Z_{in})$ and $Im(Z_{in})$ are almost constant up to 4 GHz and then increase with the frequency. S_{11} remains below -10 dB from 10MHz to 10 GHz. In a practical circuit, the remaining parasitics and second order effects will reduce the achievable matching bandwidth.

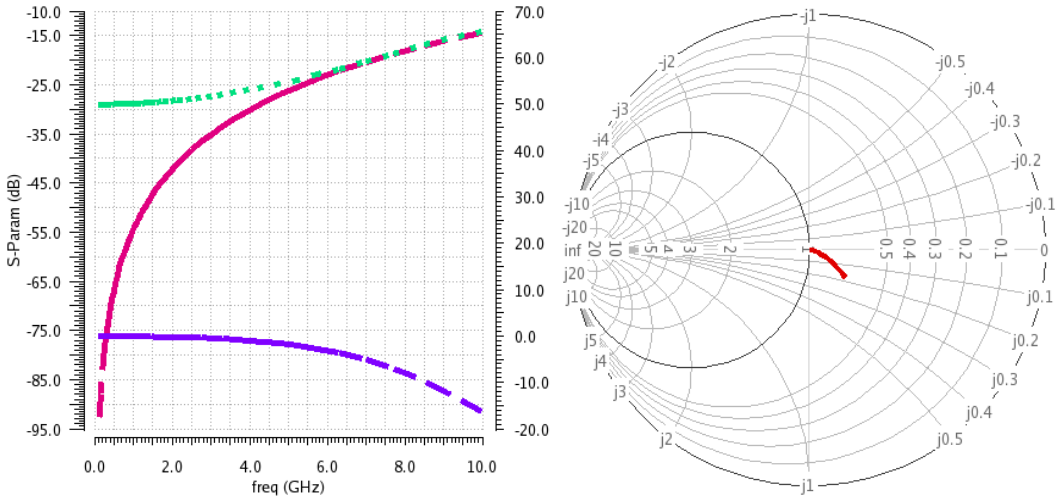


Figure 2.9 – a) Re(Z_{in}) - green, Im(Z_{in}) - blue and S_{11} - red b) Smith chart

2.3.3 Noise

A small signal model of the circuit accounting for the noise sources M_{1N}, M_{1P}, M_2, M_3, R_B and R_F is proposed in Figure 2.10. Assuming the noise sources are not correlated, the noise factor F (28) is the sum of the noise contributions of each noise source independently. The calculation is derived in current mode and yields to (29) (see Appendix B).

$$F = F_{R_S} + F_{M_{1N}} + F_{M_{1P}} + F_{M_2} + F_{M_3} + F_{R_B} + F_{R_F} \tag{28}$$

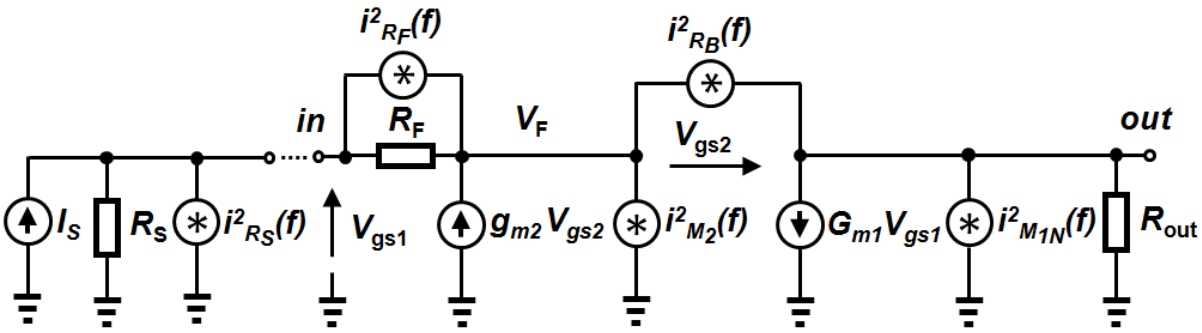


Figure 2.10 – LNA small signal model with noise sources

$$\begin{aligned}
F =& 1 && \leftarrow F_{R_S} \\
&+ \frac{\gamma_{1N} g_{m1N}}{\alpha_{1N} G_{m1}^2} . R_S . \left[\frac{1}{R_S} + \frac{g_{m2}}{1 + g_{m2} R_F}\right]^2 && \leftarrow F_{M_{1N}} \\
&+ \frac{\gamma_{1P} g_{m1P}}{\alpha_{1P} G_{m1}^2} . R_S . \left[\frac{1}{R_S} + \frac{g_{m2}}{1 + g_{m2} R_F}\right]^2 && \leftarrow F_{M_{1P}} \\
&+ \frac{\gamma_2 g_{m2}}{\alpha_2} . \frac{R_S}{(1 + g_{m2} R_F)^2} && \leftarrow F_{M_2} \\
&+ \frac{\gamma_3 g_{m3}}{\alpha_3} . \frac{R_S}{(1 + g_{m2} R_F)^2} && \leftarrow F_{M_3} \\
&+ \frac{1}{R_B} . \frac{R_S}{(1 + g_{m2} R_F)^2} && \leftarrow F_{R_B} \\
&+ R_S R_F \left[\frac{g_{m2}}{(1 + g_{m2} R_F)}\right]^2 && \leftarrow F_{R_F}
\end{aligned} \tag{29}$$

where, R_s is the signal source resistance, γ is the thermal noise excess factor, $\alpha = \frac{g_m}{g_{d0}}$ and g_{d0} is the output transconductance at $V_{ds} = 0$V (LEE, 2004).

To reduce the noise factor whilst minimally affecting the LNA's performance, the expression (29) is further analyzed. F_{M1N} and F_{M1P} are lowered if the transconductance G_{m1} of the current reuse stage is large. However, the size of the MOS devices M_{1N} and M_{1P} also define the bandwidth (20) and the voltage gain (15) of the circuit. The specifications on BW and A_V limit the reduction of F_{M1P} and F_{M1N}. R_F is introduced to reduce the noise contribution of the M_2 and M_3. F_{RF}, F_{M2} and F_{M3} benefits from a large R_F, however increasing R_F reduces the gyrator effect, which degrades the input matching. Therefore, the value of R_F is limited by the tuning of the input impedance. The DC feedback resistor R_B is made as large as possible.

If $A_V \gg 1$, the analytic expression (29) can be reduced to (30) which further illustrates the discussion on the impact of the devices on F:

$$F \approx 1 + \frac{\gamma_{1N} g_{m1N}}{G_{m1}^2 R_S} + \frac{\gamma_{1P} g_{m1P}}{G_{m1}^2 R_S} + \frac{R_F}{R_S A_V^2} + \frac{\gamma_2}{A_V}\left[1 - \frac{R_F}{R_S A_V}\right] + \gamma_3 g_{m3} R_S \left[1 - \frac{R_F}{R_S A_V}\right]^2 + \frac{R_S}{R_B}\left[1 - \frac{R_F}{R_S A_V}\right]^2 \quad (30)$$

2.3.4 Stability

The circuit in Figure 2.8.b) can be modeled as a gyrator, for this we use the feedback theory of a two-port (GRAY et al., 2009), shown in Figure 2.11. We calculate the y-parameters as shown in Appendix B.

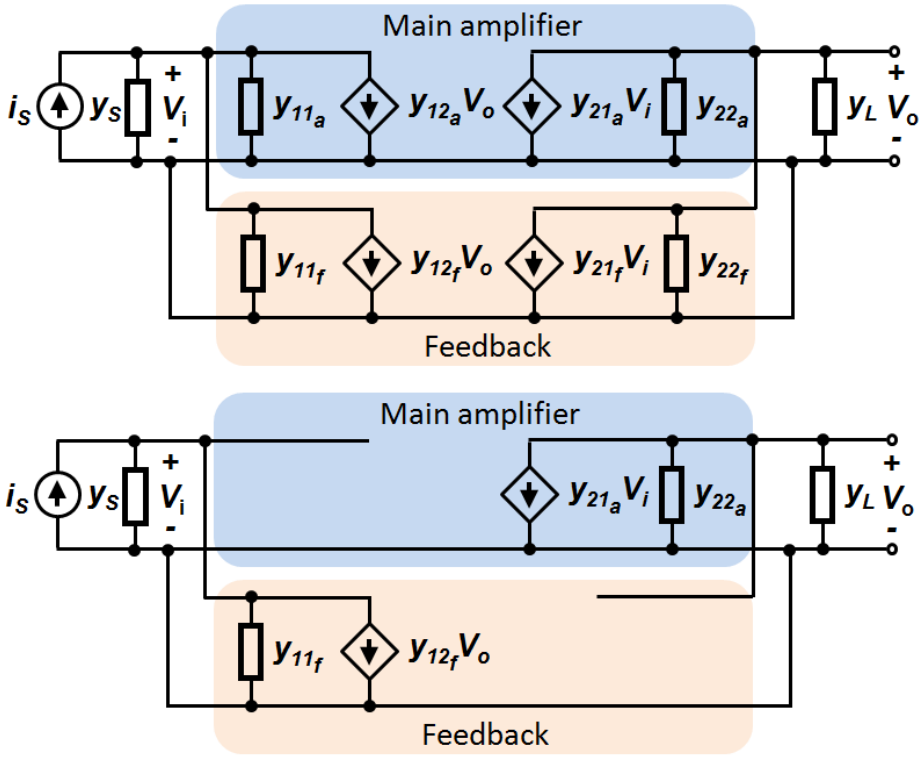


Figure 2.11 – a) y-parameter of a shunt-feedback amplifier b) simplified circuit when $y_{21a} \gg y_{12a}$ and $y_{12f} \gg y_{21f}$, $y_{11a} \approx 0$ and $y_{22f} \approx 0$, the case of the amplifier in Figure 2.8(a).

Table 2.3 – Gyrator-like LNA low frequency y-parameters

	y_{11}	y_{12}	y_{21}	y_{22}
Main amplifier	0	0	Gm_1	0
Feedback	$\frac{g_{m2}}{(1+g_{m2}R_F)}$	$\frac{-g_{m2}}{(1+g_{m2}R_F)}$	0	0

The low-frequency y-parameters shown in Table 2.3 allow us to simplify the circuit as shown in Figure 2.11.

The stability can be evaluated with the loop gain T, and the Nyquist stability criterion (GRAY et al., 2009), that states that closed loop circuit will be stable if the loop gain is smaller than 1 when phase shift is $-180°$ or larger than -1.

According to (GRAY et al., 2009), the loop gain T is given by $T = af$, where f is the feedback amplifier gain, given by $f = y_{12f}$; a is the gain of the basic amplifier, given by $a = -\frac{y_{21a}}{y_i y_o}$, while y_i and y_o are the input and output admittances that load the amplifier and are given by $y_i = y_S + y_{11}a + y_{11f}$ and $y_o = y_L + y_{22a} + y_{22f}$, respectively.

$$T = \left(-\frac{y_{21a}}{(y_S + y_{11}a + y_{11f})(y_L + y_{22a} + y_{22f})}\right)(y_{12f})$$

Replacing with the parameters in Table 2.3, we find the low frequency loop gain:

$$T = \left(-\frac{g_{m2}}{1 + g_{m2}R_F}\right)\left(-\frac{g_{m1}Z_L R_S}{1 + \left(\frac{g_{m2}}{1 + g_{m2}R_F}\right)R_S}\right)$$

$$T = \frac{g_{m1}Z_L}{1 + \left(\frac{1 + g_{m2}R_F}{g_{m2}R_S}\right)}$$

Applying the matching condition (14), yields

$$T = \frac{+G_{m1}Z_L}{1 + (1 + G_{m1}Z_L)} \tag{31}$$

Assuming $|A_V| = G_{m1}Z_L$, yields

$$T = \frac{G_{m1}Z_L}{2 + G_{m1}Z_L} = \frac{|A_V|}{2 + |A_V|} \tag{32}$$

Applying the Nyquist stability criterion $T > -1$, or $|T| < 1$,

$$|T| = \frac{|A_V|}{2 + |A_V|} < 1 \tag{33}$$

where this expression is valid upon matching. Given the low loop gain, the circuit is unconditionally stable upon match, even when parasitics are considered.

2.3.5 Linearity

Any weakly nonlinear system can be characterized by the first three terms of a Taylor series as proposed in (34).

$$y(t) = A_1 x(t) + A_2 x^2(t) + A_3 x^3(t) \tag{34}$$

where A_1, A_2 and A_3 represent the first-, second- and third-order transfer functions, respectively. They are defined as $A_k = \frac{1}{k!}\frac{\partial^k V_{out}}{\partial V_{in}^k}$.

In an LNA, the major source of distortion is due to the nonlinear transconductance, g_m, as the conversion of input voltage into an output current is inherently nonlinear (ZHANG; SANCHEZ-SINENCIO, 2011). The linearity is usually characterized by the -1 dB gain compression (CP1) and the third-order intercept point (IP_3). CP1 distortion is produced when input signals saturate the LNA. In practice, because the level of input power never exceeds -20 dBm, the CP1 is not an issue in LNA design. The IP_3 reduces the LNA's sensitivity when modulated signals are present in adjacent channels (in-band blockers), or when signals of a moderate power level are present out of the operating band (out-of-band blockers). The high spectral density of current radio-communications makes IP_3 a very important characteristic. Furthermore, the inherent non-selectivity of wideband LNA makes them more sensitive than narrowband LNA to the intermodulation phenomenon. Consequently, an inductorless wideband LNA dedicated to multi-standard communications must possess a high IP_3.

According to (WAMBACQ; SANSEN, 1998), the input-referred IP_3 or IIP_3 of an amplification system can be defined in the frequency domain as:

$$IIP3 = \sqrt{\frac{4}{3}\frac{A_1(j\omega_1)}{A_3(-j\omega_1, j\omega_2, j\omega_2)}} \tag{35}$$

where $A_1(s)$ and $A_3(s)$ can either be, respectively, the first and third-order Volterra kernels.

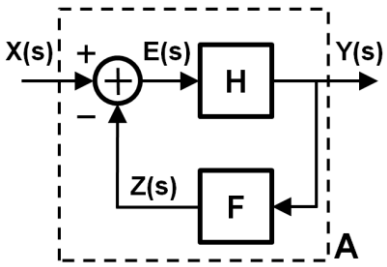


Figure 2.12 – Nonlinear amplifier A, composed of a nonlinear main amplifier H and a nonlinear feedback amplifier F.

In this work, we consider the case of an amplifier based on a negative feedback topology, as illustrated in Figure 2.12. It is composed of an amplification stage, H, in the main path, and a feedback block F. We further assume the system is memoryless, which is typically sufficient for hand analysis of wideband RF circuits (ZHU; KRISHNASWAMY; KINGET, 2015), and true when the system bandwidth is

higher than the second harmonic frequency (KIM; APARIN; LARSON, 2011). With this assumption, the IIP_3 is given by (36). The added feedback path alters the IIP_3: the third-order response (H_3 and F_3), the second-order response (F_2 and H_2), as well as the fundamental response (H_1 and F_1) all contribute to the IP3 derived from (WAMBACQ et al., 1999):

$$IIP_3 = \sqrt{\frac{4}{3}\left|\frac{H_1}{R^3[H_3 - 2H_2^2F_1R + H_1^4(2H_1F_2^2R - F_3) - 4H_1^2H_2F_2R]}\right|} \tag{36}$$

Where, $R = (1 + H_1F_1)^{-1}$ is the feedback gain reduction factor.

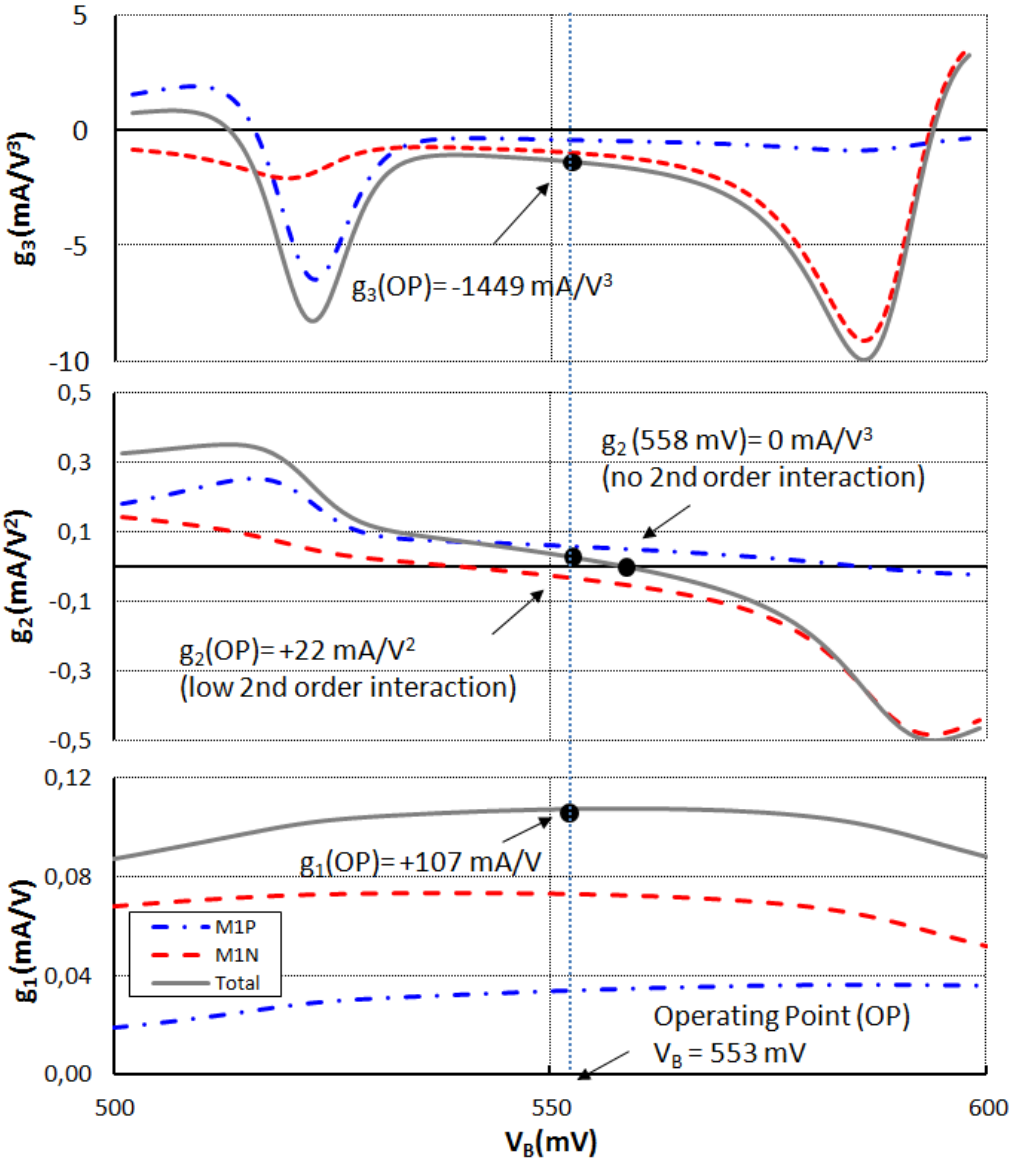


Figure 2.13 – Current-reuse block complementary derivative superposition. g_k versus bias voltage V_B. At the operating point, set by R_B, V_B = 553 mV, leading to g_2 = 0.2 g_1 and g_3 = -13.1 g_1.

In the proposed LNA, the main amplifier H is implemented with a current-reuse topology. This complementary configuration using a PMOS and an NMOS transistor can be sized to improve the overall linearity (APARIN; LARSON, 2005). In Figure 2.13, the first- (g_1), second- (g_2) and third-order (g_3) transconductances of the NMOS, PMOS, and current-reuse amplifier, are represented as a function of biasing. The circuit is self-biased, so the operating point (OP) is defined as $V_{GS_{1N}} = V_{DS_{1N}}$, achieved via the bias resistor R_B. For this bias condition the overall transconductance (g_1) is maximal, $|g_3|$ is small and g_2 is close to zero. This allows the main amplifier to have the highest gain, with minimal third-order intermodulation and a theoretical cancellation of the second-order interaction $(H_2 \approx 0)$. H_2 is responsible for combining first- and second-order terms generating additional third-order harmonics in an SFB configuration.

We assume the forward stage H, implemented with a current reuse configuration, does not produce any second order harmonics (H_2=0), the overall IIP_3 of the proposed LNA, accounting for the feedback stage F, can be rewritten as follows (37):

$$IIP_3 = \sqrt{\left|\frac{H_1}{H_3}\frac{(1+T)^3}{\left[1-\frac{H_1^4}{H_3}(F_3 - 2\frac{F_2^2}{F_1}\frac{T}{(1+T)})\right]}\right|} \tag{37}$$

with $H_k = \frac{1}{k!}\frac{\partial^k V_{O_{CR}}}{\partial V_{I_{FB}}^k}$, $F_k = \frac{1}{k!}\frac{\partial^k V_{O_{FB}}}{\partial V_{I_{FB}}^k}$,

where, $V_{I_{CR}}, V_{O_{CR}}$ represent the voltages at the input and output of the current-reuse stage, respectively. $V_{I_{FB}}, V_{O_{FB}}$ are the voltage at the input and output of the feedback stage, respectively, and $T = H_1F_1$ is the loop gain. If $F_1 \gg F_2$, then the expression of IIP_3 proposed in (37) can be simplified to (38):

$$IIP_3 = \sqrt{\left|\frac{H_1}{H_3}\frac{(1+T)^3}{\left[1-\frac{H_1^4}{H_3}F_3\right]}\right|} \tag{38}$$

The denominator of (38) can be minimized by properly sizing and biasing the feedback block F. Indeed H_1 and H_3, related to the current-reuse amplification stage, are fixed by OP, but F_3 can still be adjusted to reduce the denominator.

Summarizing the behavior of the circuit with respect to linearity, we find:

The intermodulations are always generated by nonlinear transfer function $I_d(V_{gs})$.

The main intermodulations come from the current-reuse stage, an amplifier exclusively driven by V_{gs}.

The feedback transmits the IM2 and IM3 of the CR stage, and adds its own IM3.

The feedback recombines the IM2 of the CR with its fundamental to create IM3 with opposing sign with respect to those of the CR, thus increasing the overall IIP3

2.4 SHUNT PEAKING STAGE

In the 130 nm technology, due to the intrinsic MOS parasitics , the Gyrator-like LNA is not capable of reaching a -3 dB bandwidth of 6 GHz, thus preventing its use in standards as WiFi.a/n/ac, LTE higher bands, and WiMAX. To overcome this problem, an additional inductor based stage is needed. This second stage, illustrated in Figure 2.7, is referred from now on as the peaking stage. The low-Q, integrated inductor L creates a shunt peaking effect, extending the overall bandwidth of the LNA.

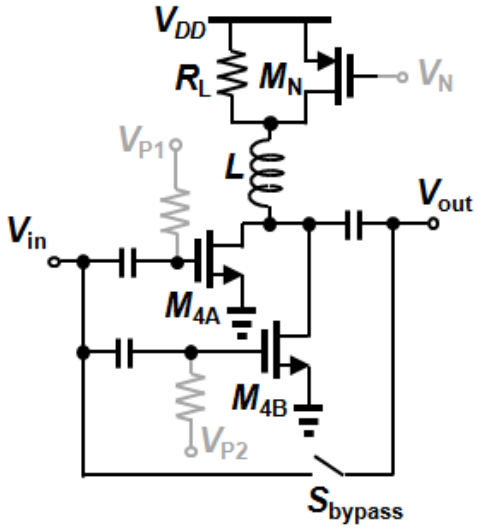


Figure 2.14 – Peaking stage

The load resistor R_L is used to reduce the Q-factor of the inductor and thus enhance the gain flatness. The bandwidth extension can be turned off by bypassing the resistor R_L with the transistor M_N, this increases the Q-factor, increasing the maximum gain. Besides the transconductance stage is composed by two parallel NMOS transistors employing the derivative superposition technique (APARIN; LARSON, 2005). The auxiliary transistor M_B and the main transistor M_A are biased in different inversion levels to cancel out the overall g_3, thus improving the IIP3. The gain is controlled through the bias current configuration in the Gm stage.

2.5 SUMMARY

Future adaptive receivers need highly integrated LNAs with reconfiguration capabilities of the gain, the NF, the IIP3 and the operating frequency. This chapter reviewed the state of the art of inductorless wideband LNAs and reconfiguration techniques for LNA implementations. Two wideband topologies were identified as promising solutions: the current-reuse configuration for its high A_V/P_{DC} ratio, and the active shunt-feedback for its wideband input matching and relatively low NF, even though it presents a low linearity. About the reconfiguration capability, most of the reviewed solutions implement the tuning in the second stage to guarantee a good impedance matching and low NF. Besides it allows the control of at most two characteristics. This kind of approach limits the range of reconfiguration and the flexibility of the system. To address the purpose, we propose to steer the bias current of a G_m stage to reconfigure the gain, the NF and the IIP3. Whereas the operating frequency and bandwidth are controlled with the variation of a load impedance in a second stage.

A novel topology, namely gyrator-like LNA (Figure 2.8), combines a current reuse stage with an active shunt-feedback amplifier. This inductorless solution achieves a large gain, a high IIP3 and a low NF at low P_{DC} over a wide frequency range. By changing the bias current of the main amplifier, the NF can be modified, tuning of the current in the feedback stage controls the IIP3 and the input matching.

To extend the bandwidth and the gain of the gyrator-like amplifier, a two stage version is also proposed (Figure 2.7.b). This second stage allows for gain variation through the bias current of the Gm stage, and bandwidth extension by the modification of the load impedance. Increasing the number of stage, the linearity be-

comes an issue for the last stage (RAZAVI, 2012). The derivative superposition technique (APARIN; LARSON, 2005) is applied to circumvent this problem, thus enabling IIP3 control in the second stage as well. A bypass mode is added to save power when no gain control nor bandwidth extension are required. This two stage LNA enables orthogonal adjusting of: NF and Gain, NF and IIP3, IIP3 and Gain. Its implementation in 130nm CMOS technology from Global Foundries is further exposed in the next chapter.

3 CIRCUIT DESIGN

This chapter reports our work on a design methodology for low-power wideband LNAs. First, we describe the circuit design flow, and apply it to the tuning of the Gyrator-like LNA presented in Chapter 2. Then the simulated results are discussed and compared to the specifications presented in Chapter 1. Two versions of the LNA are implemented in Global Foundries 130 nm CMOS technology to validate the design method and the reconfiguration capabilities:

- the inductorless single-stage Gyrator-like LNA - CHIP1
- The two-stage Gyrator-like – CHIP2

3.1 WIDEBAND LNA DESIGN METHODOLOGY

Even though the analytical models presented in Chapter 2 provide a solid base for the design of the proposed LNAs, a design methodology is required to size the circuit for a set of specifications at minimum power consumption. The design of low-power narrowband LNAs is well documented (SHAEFFER; LEE, 1997). However, the design of low-power inductorless wideband LNA needs investigations. In this section, a simulation-assisted design methodology is presented to address this issue.

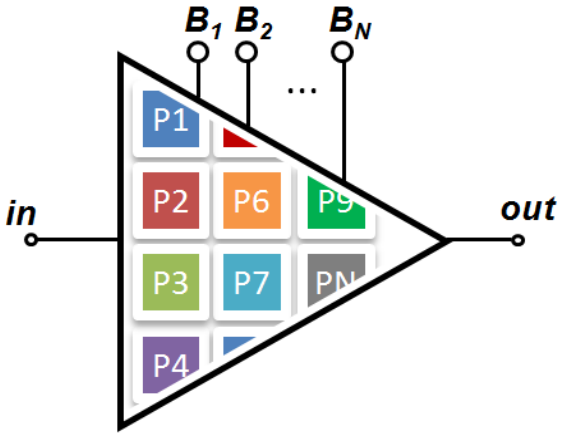


Figure 3.1 – LNA parameters and bias variables

The design variables are the component sizes and biasing conditions, shown in Figure 3.1. A set of design variables is defined by the vector

$$\vec{x} = [P_i, \ldots, P_N] \text{ where } 1 \leq i < N \quad (1)$$

where P_i is one of N design parameters (width, length, bias current/voltage, etc).

The design space is limited by

$$\begin{gathered}\vec{x}_{min} \leq \vec{x} \leq \vec{x}_{max} \\ \vec{x}_{min} = [P_{imin}, \dots, P_{Nmin}] \\ \vec{x}_{max} = [P_{imax}, \dots, P_{Nmax}]\end{gathered} \tag{2}$$

where P_{imin} and P_{imax} are one of N minimum and maximum allowed parameter values, respectively.

The frequencies of interest are defined by the vector

$$\vec{f} = [f_{std1}, f_{std2}, \dots, f_{stdn}], \tag{3}$$

where f_{stdi} is the operating frequency of each target wireless standard.

The design space is explored with parametric simulations. The results are exported and post-processed in order to compare them with the design objectives. The design of RF building blocks is a multi-objective multi-variable optimization problem, which needs data filtering method to deliver the right set of design variables.

To help the selection process the figure of merit (FOM) defined in (4) is considered as an objective function. It combines the most relevant performance of the LNA into a single measure. It is derived from the ITRS FOM defined for narrowband LNAs (ITRS, 2007), where the operating frequency (f_o) is replaced by the -3 dB bandwidth (BW).

$$FOM(\vec{x}, \vec{f}) = 20 \log\left(\frac{G_{max}.IIP_{3max}.BW}{(F_{min}-1).P_{DC}}\right), \tag{4}$$

where G_{max} is the maximum voltage gain, expressed in V/V; IIP_{3max} is the maximum input-referred third-order intercept point expressed in mW; BW is the -3 dB bandwidth in GHz; F_{min} is minimum noise factor in linear; and P_{DC} is the static power consumption of the LNA in mW each one defined for a frequency set $\vec{f}$ and a set of circuit parameters $\vec{x}$.

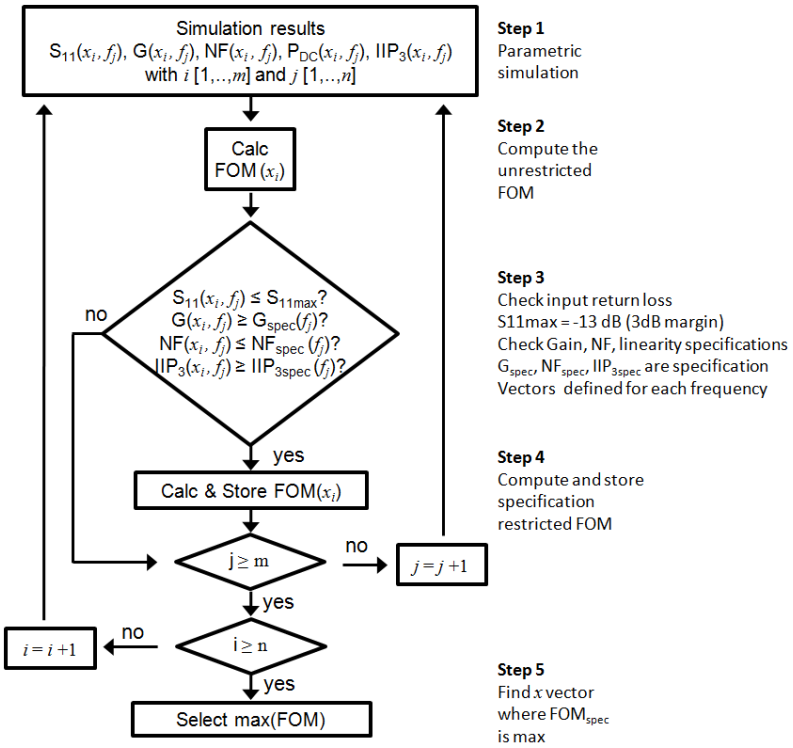


Figure 3.2 – Parameter set selection algorithm

The region containing the highest FOM may not fully comply with the specifications, i.e. the region contains invalid solutions to the problem. To address this issue, the design flow, presented in Figure 3.2, is used to filter-out the parameter sets that do not comply with the specifications. A parameter set is rejected if it does not ensure unconditional stability of the LNA, or if the resulting performance parameter is out of specifications for a given frequency (step 3). The parameter sets that address all the wireless standards specifications are selected and stored (step 4). They are further considered in the specification restricted figure of merit, namely FOM_{spec}, where the maximum value of FOM_{spec} is filtered out as the final solution (step 5).

3.2 CHIP1: GYRATOR-LIKE LNA

3.2.1 Design

The design methodology presented in Section 3.1. is applied to the gyrator-like LNA of Figure 3.3 in the implementation of CHIP1.

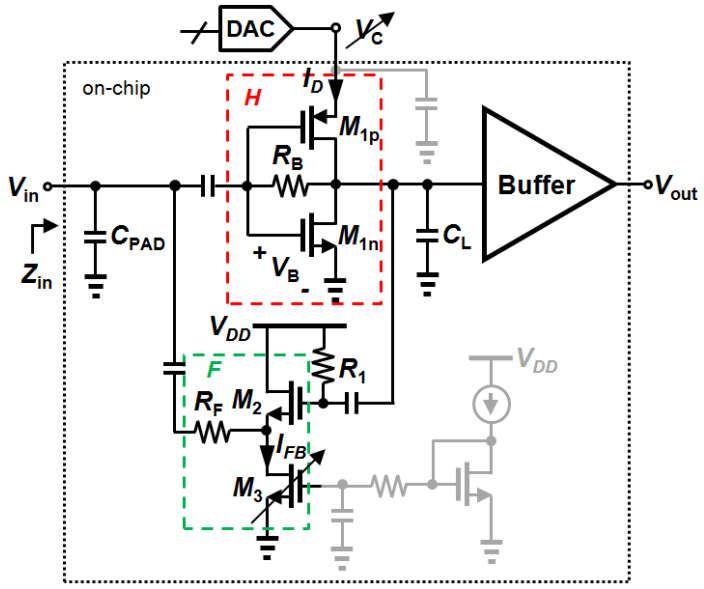


Figure 3.3 – CHIP1: implemented circuit

The design variables are the sizes of the components. A set of these component sizes is defined by the vector

$$\vec{x} = [W_{M1N}, W_{M1N}, W_{M2}, W_{M3}, R_F, R_B, V_C, I_{FB}] \quad (5)$$

where W_{M1N}, W_{M1P}, W_{M2} and W_{M3} are the widths of the transistors M_{1N}, M_{1P}, M_2, M_3, respectively; R_F and R_B are the feedback and bias resistors, respectively; and V_C, and I_{FB} are the current-reuse stage control voltage and feedback stage bias current, respectively. The size of the devices is optimized for high performance operation.

The design space is limited by

$$W_{min} \leq W_{Mi} \leq W_{max}$$
$$0 < V_C \leq V_{max}$$
$$0 < I_{FB} \leq I_{max}$$

where W_{min} and W_{max} are the minimum and maximum allowed transistor widths, respectively worth $1\,\mu m$ and $300\,\mu m$. V_{max} is the highest allowed voltage that should be applied to a transistor, fixed here to $1.5\,V$. I_{max} is the maximum allowed current, here 10 mA. The channel length L is fixed to the smallest value allowed by the technology, 130 nm, in order to reduce the parasitic capacitances and achieving large gain and low NF in higher frequency bands.

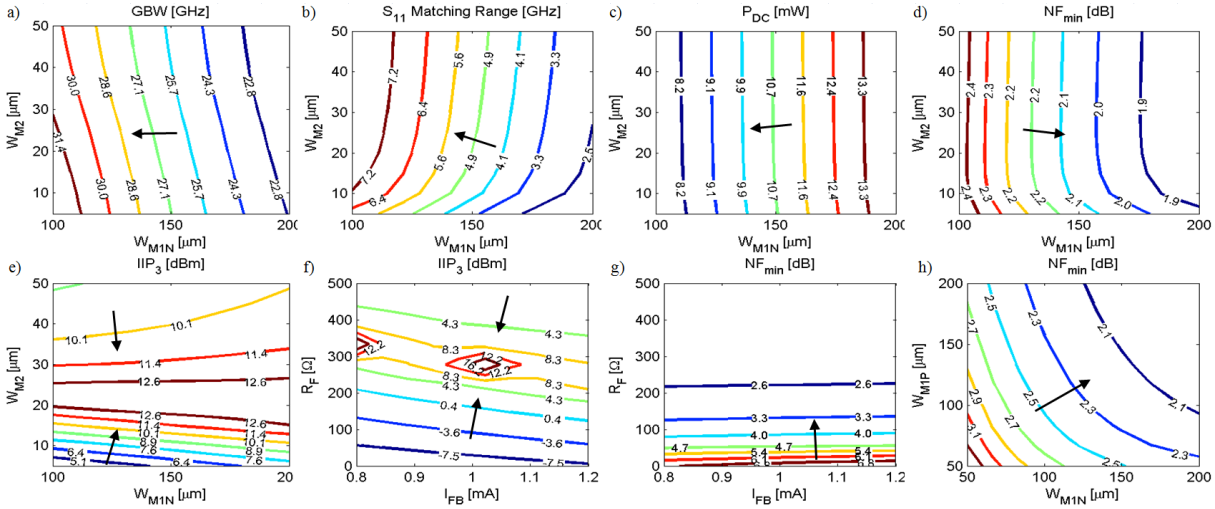


Figure 3.4 – Design space exploration. LNA performance parameters vs design variables. a) Gain-bandwidth product b) Input matching (S_{11}< S_{11max}) frequency range c) Power consumption. d) Minimal noise figure e) IIP_3. [a to e] vs [W_{M1N}, W_{M2}] with $W_{M1P} = W_{M1N}$ for a set of [$W_{M3}, R_F, R_B, V_C, V_{FB}$]. f) IIP_3 g) NF_{min}[f and g] vs [R_F, I_{FB}] for a set of [$W_{M1N}, W_{M1P}, W_{M2}, W_{M3}, R_B, V_C$]. h) NF_{min} [h] vs [W_{M1N}, W_{M1P}], for a set of [$W_{M2}, W_{M3}, R_F, R_B, V_C, V_{FB}$].

The design space is explored with parametric simulations in SpectreRF, and using the foundry's physical design kit. The gain-bandwidth product (GBW), input impedance matching (S_{11}) range, power consumption (P_{DC}), minimal NF within the bandwidth (NF_{min}), and IIP_3, as functions of W_{M1n} and W_{M2} (all other parameters made constant), are reported in Figure 3.5.a) to Figure 3.5.e), respectively. The IIP_3 and NF_{min} as functions of R_F and I_{FB} are shown in Figure 3.5.f) and Figure 3.5.g). Finally, the NF_{min} as a function of W_{M1n} and W_{M1p} is proposed in Figure 3.5.h). The arrows denote the direction of performance enhancement. These results illustrate a part of the interdependency of LNA's performance in terms of component parameters. It can be noted that P_{DC} increases with W_{M1n} and is virtually independent of W_{M2}. However, the NF_{min} decreases with M_{1n}'s width, while being quasi-independent of M_2's width for $W_{M2} > 10\,\mu m$. As shown with these design variables and performance results, important trade-offs exist and need a data filtering method to provide a solution that complete the set of specifications.

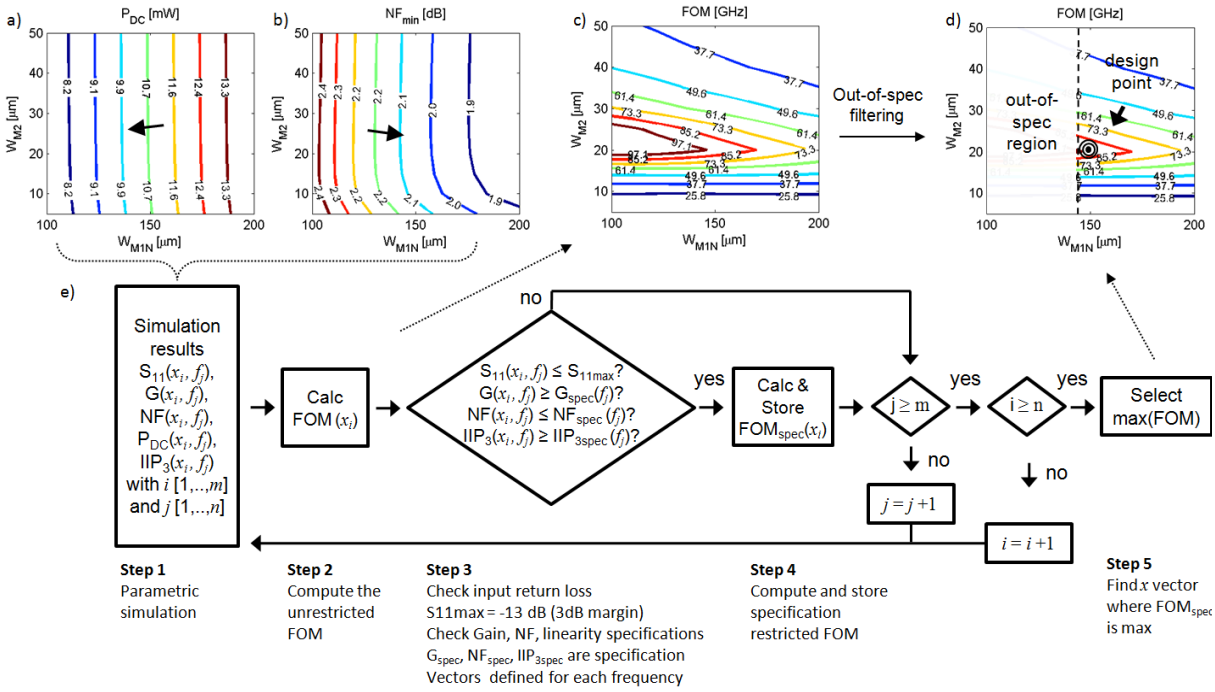


Figure 3.5 – Selection process of parameter sets to address the specifications and FOM optimization. a) $P_{DC}(W_{M1n}, W_{M2})$ b) $NF_{min}(W_{M1n}, W_{M2})$ c) Unrestricted $FOM(W_{M1n}, W_{M2})$ d) Specification restricted $FOM(W_{M1n}, W_{M2})$ e) Design flow.

Considering the simulation results, presented in Figure 3.5.a) and Figure 3.5.b), derived from Figure 3.5.c) and Figure 3.5.d), the maximum FOM occurs for small values of W_{M1n}, as illustrated in Figure 3.5.c). Indeed, for this circuit, the FOM is more sensitive to the P_{DC} and IIP_3 than to G, NF, BW. However, the region containing the highest FOM does not fully comply with the specifications. The algorithm of Figure 3.2, reproduced in Figure 3.5.e), is applied to filter-out the out-of-specifications parameter sets. The sets that address all the wireless standards specifications are selected and stored at step 4. They are further considered in the specification-restricted figure of merit, namely FOM_{spec}, to work out the maximum value of FOM_{spec} (step 5), as illustrated in Figure 3.5.d).

This design procedure is applied to the circuit described in Figure 3.3, taking into account the specifications of Table 1.II from Chapter 1. If the input capacitance of the output buffer, C_L, is $40\,fF$, the set of device sizes which achieve the best FOM_{spec} is:

$$\vec{x}_{opt} = [150\ \mu m, 150\ \mu m, 30\ \mu m, 10\ \mu m, 300\Omega, 14k\Omega, 1.3\ V, 1\ mA] \quad (6)$$

Figure 3.6 shows the schematic of the implemented LNA. It consists of a common-source P/NMOS inverter pair as the forward amplifier, together with a

common-drain amplifier in the feedback path. The forward amplifier reuses the same DC bias current to save power consumption.

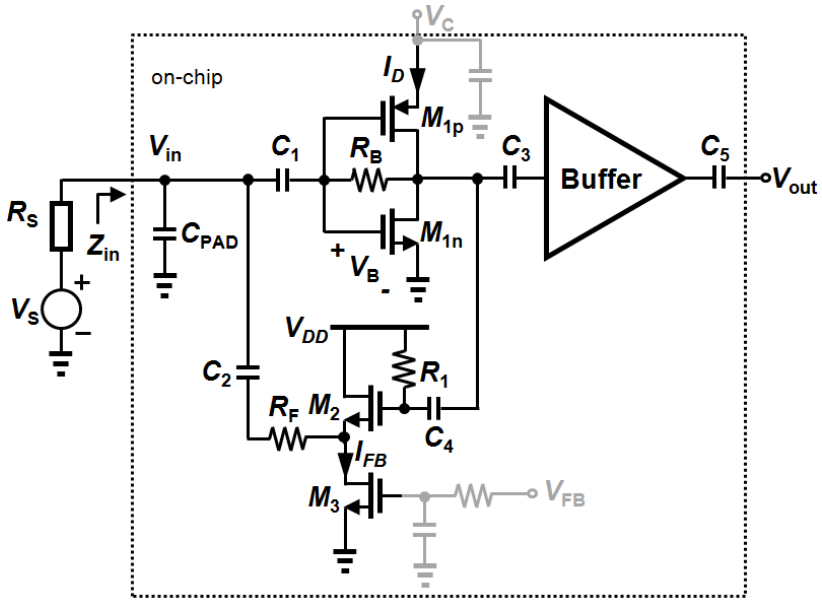


Figure 3.6 – LNA schematic

Table 3.1 summarizes the implemented device sizes.

Table 3.1. Device sizes

M_{1N}	30 x 5 µm/130 nm	R_F	300 Ω	C_2	3 pF
M_{1P}	30 x 5 µm/130 nm	R_B	14 kΩ	C_3	2.14 pF
M_2	6 x 5 µm/130 nm	R_1	14 kΩ	C_4	0.68 pF
M_3	2 x 5 µm/130 nm	C_1	10 pF	C_5	13.6 pF

3.2.2 Layout considerations

After the device sizing, the components are laid-out using the physical design kit of the foundry. Figure 3.7 shows the chip layout.

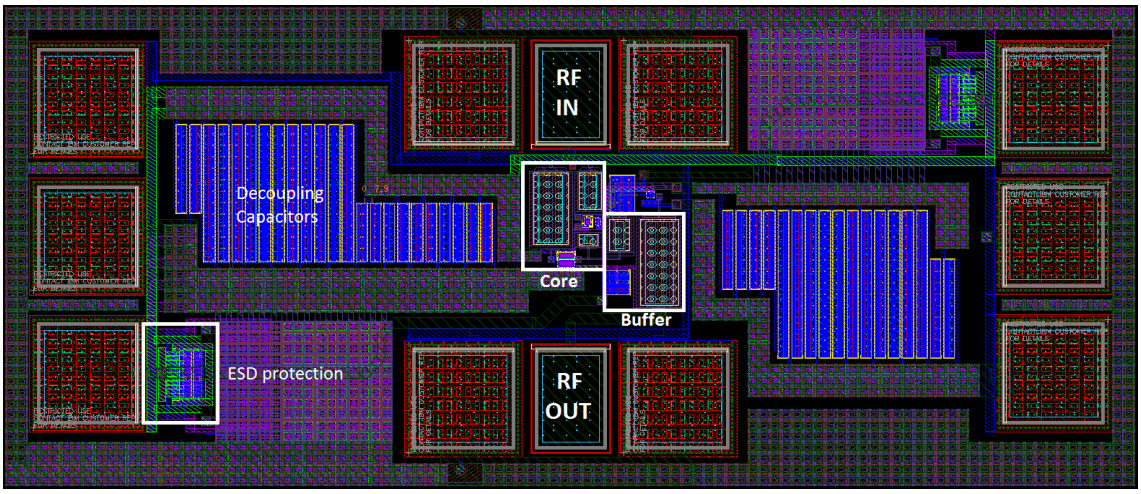


Figure 3.7 – CHIP1 layout

The LNA core is placed as close as possible to the input RF pad to reduce the access resistance that degrades the NF and input matching. All the RF paths are routed with the high metal layers. A ground plane is created inside and around the circuit, combining all metal layers it achieves a low resistance, which is important for noise and gain performance. MOS capacitors are distributed in a large area to ensure a stable DC supply. ESD protection diodes are positioned close to control pads.

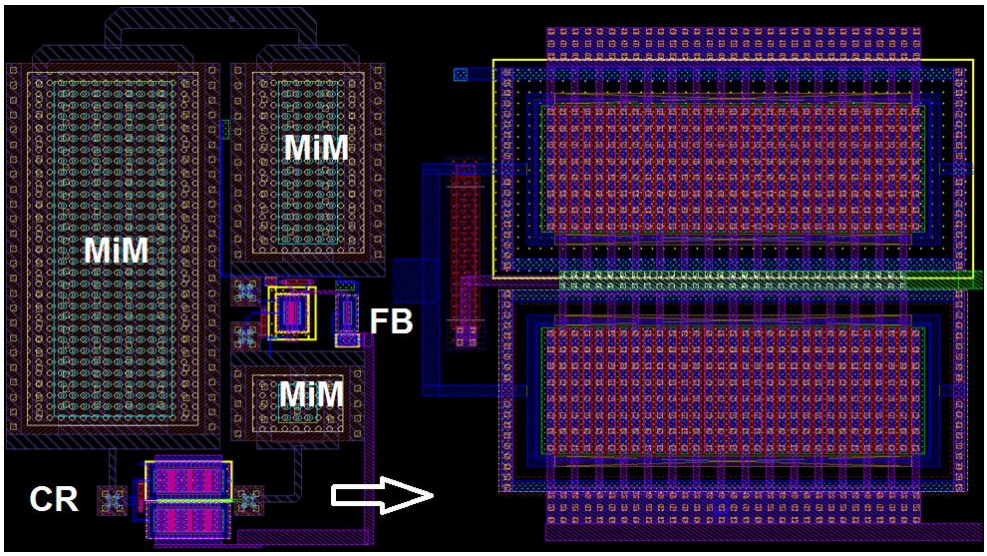


Figure 3.8 – Gyrator-like LNA and current-reuse structure layout

Figure 3.8 shows the core of the LNA. Most of this area is dedicated to Metal-Insulator-Metal (MiM) AC coupling capacitors C_1 to C_5. The amplification transistors of the current-reuse structure, are symmetrically drawn for better matching. Transistors M_1 to M_3 are implemented with different number of 5 µm/0.13µm fingers to reduce gate noise resistance. Double-sided gate contacts are used to minimize the parasitic

resistance of the poly gate material. Resistors are implemented with high-valued P+ poly layer to reduce the silicon footprint, except for R_F which requires an accurate value. RC filters are distributed along the bias lines to deliver stable DC voltages.

3.2.3 Post-layout simulation results

The performance of the circuit is simulated taking into account the parasitics extracted from the layout. Figure 3.9 shows the post layout simulation (PLS) results of the designed circuit at nominal conditions (V_{DD}=1.3 V and P_{DC}=7 mW).

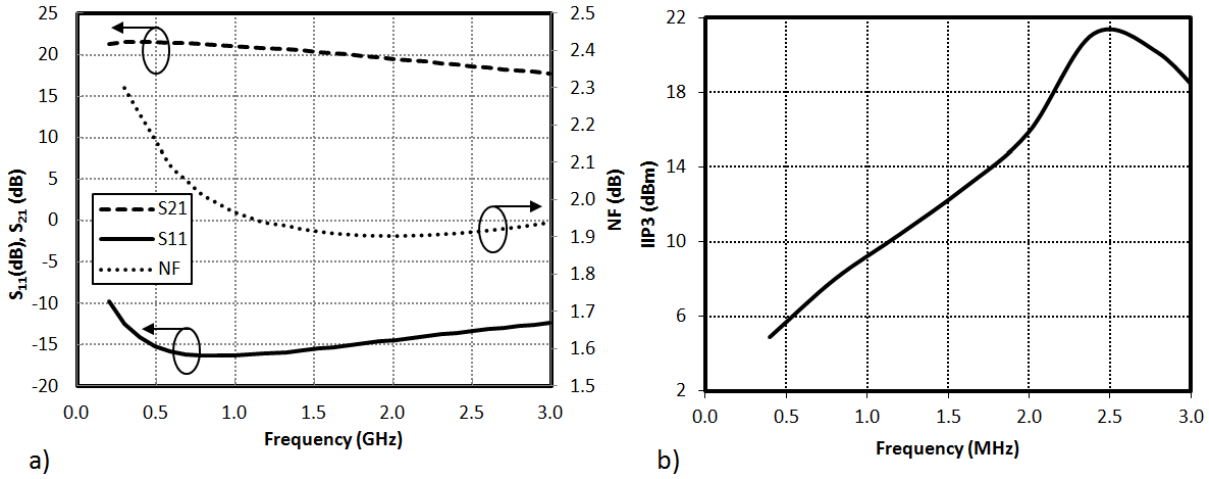


Figure 3.9 – PLS results at best performance (P_{DC} = 7 mW). a) S21, S11 and NF b) IIP3

Figure 3.9 a) shows the gain response (S_{21}) versus frequency. It behaves like a first order system with -3 dB bandwidth of 2.5 GHz. The maximum gain is 21.5 dB at 580 MHz, the circuit still achieves 17.5 dB at 3 GHz, which is enough to reduce the noise contribution of the following stages featuring a receiver chain. The return loss S_{11} remains below -12 dB from 300 MHz to 3 GHz, which ensures a broadband input matching. The linearity is represented by the two tones test response (IIP_3) of Figure 3.9.b). The IIP_3 increases with the frequency up to +21 dBm at 2.4 GHz. Indeed, at low frequency the linearity is degraded as the first orders of harmonic distortions fall into the bandwidth, thus producing more harmonics by recombination. As the frequency increases, the harmonics fall outside the bandwidth thus limiting recombination and inter-modulations, the overall linearity improves.

The NF is also reported in Figure 3.9.a), the minimum value is 1.9 dB at 2 GHz, and it remains below 2.3 dB over the entire bandwidth. Table 3.2 shows the noise contribution of each component in the overall NF.

Table 3.2 – Overall noise breakdown

Component	Contribution	Channel Noise	Flicker Noise	Resistive Thermal Noise
M1N	57.3%	35.2%	10.1%	12.0%
M1P	15.1%	15.1%	-	-
RF	19.7%	-	-	19.7%
M2	4.0%	3.2%	0.8%	-
M3	2.8%	2.1%	0.7%	-
RB	1.0%	-	-	1.0%
Total	100.0%	55.6%	11.6%	32.8%

Considering the total noise generated by the LNA components, 57% is generated by M_{1N}, R_F accounts for 20% of the total noise. 12% of the total NF noise is due to the flicker noise, mostly added by M_{1N} with a negligible contribution of $M_{1P.}$ R_B is only intended for self-biasing of the current reuse stage, it is designed to be as large as possible which reduces its impact on the noise figure, approximately 1% of the overall noise. Further analysis of the thermal noise contributions can be found in Appendix B.

3.2.4 PVT sensitivity

The circuit sensitivity to process, voltage and temperature (PVT) variations is evaluated through corners simulations. Table 3.3 shows the evaluated corner list. Each corner is named as PVT, where P is the process P = [TT, SS, FS, SF and FF]; V is the nominal supply voltage with 10% variation V = [**U**ndervoltage(1.2 V), **T**ypical(1.3 V), **O**vervoltage(1.4 V)]; and T is the temperature T = [**C**old(-40°C), **T**ypical(27°C), **H**ot(+125°C)]. For example, the FSOC corner refers to *FS* process corner, supply voltage of 1.4 V (*O*) at -40°C (*C*). The nominal corner is the where every condition is typical and it is named TTTT.

Table 3.3 – PVT corner list. Evaluated (black), unevaluated (gray)

		Process				
VDD	**Temp**	**TT**	**SS**	**SF**	**FS**	**FF**
1.4 (O)	-40 (C)	TTOC	SSOC	SFOC	FSOC	FFOC
	27 (T)	TTOT	SSOT	SFOT	FSOT	FFOT
	125 (H)	TTOH	SSOH	SFOH	FSOH	FFOH
1.3 (T)	-40 (C)	TTTC	SSTC	SFTC	FSTC	FFTC
	27 (T)	TTTT	SSTT	SFTT	FSTT	FFTT
	125 (H)	TTTH	SSTH	SFTH	FSTH	FFTH
1.2 (U)	-40 (C)	TTUC	SSUC	SFUC	FSUC	FFUC
	27 (T)	TTUT	SSUT	SFUT	FSUT	FFUT
	125 (H)	TTUH	SSUH	SFUH	FSUH	FFUH

The gain of this LNA is almost insensitive to PVT variations. As shown in Figure 3.10, the gain deviation is lower than 1.6 dB at 0.9GHz and 1.2dB at 2.4GHz over the entire set of corners.

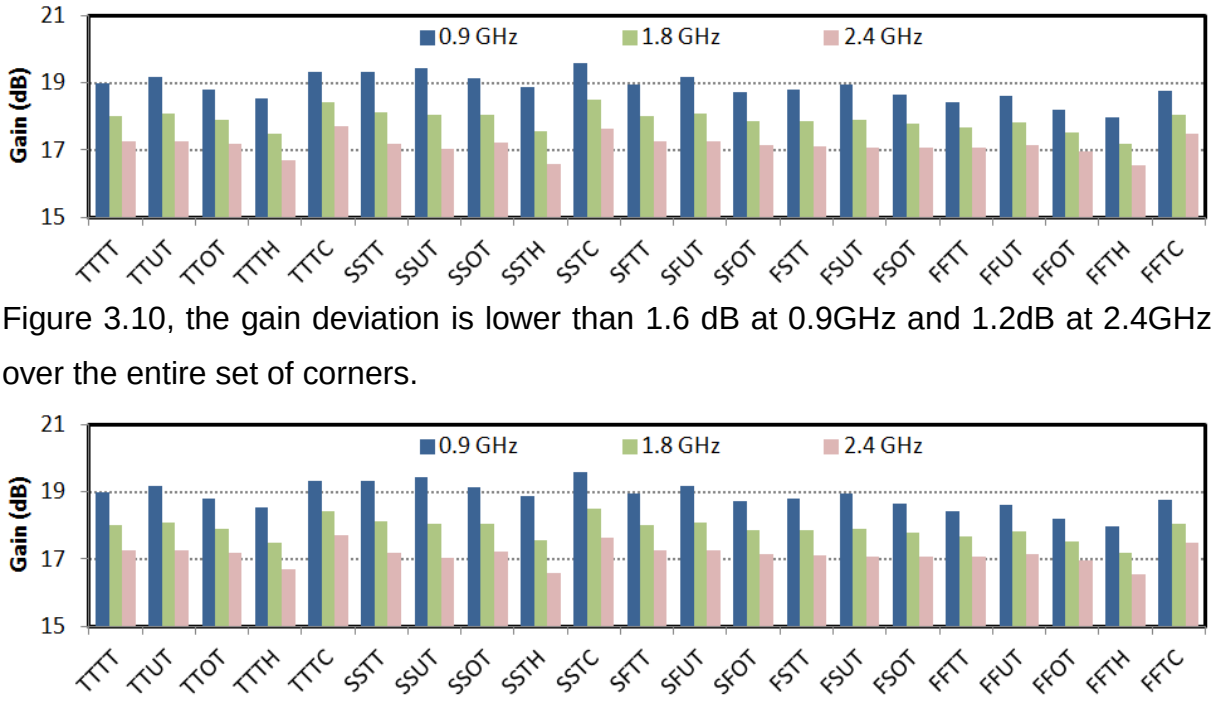


Figure 3.10 – Gain variation to PVT corners

In the worst case corner, the gain is still 17 dB at 2.4 GHz, FF, 27°C and 1.3 V (FFTT), which is enough to reduce the noise contribution of the following stages of a receiver chain in most of applications.

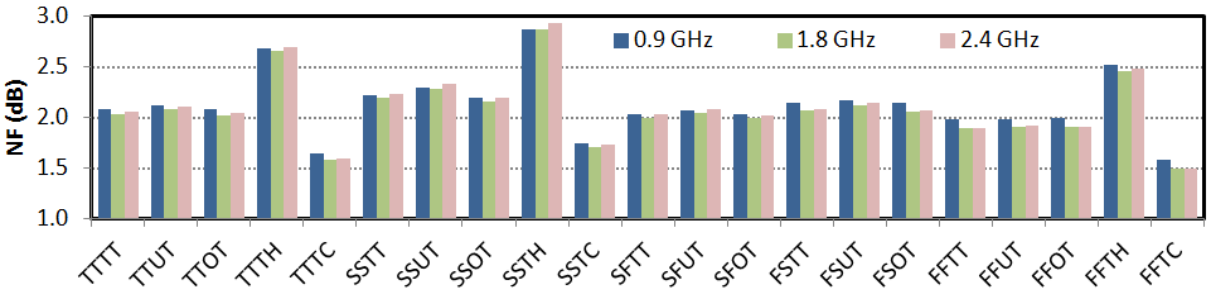


Figure 3.11 – NF variation to PVT corners

The NF of the LNA is also not very sensitive to voltage and process variations, with less than 0.3 dB variation across all process corners. However, as the NF is dominated by thermal noise, it is sensitive to temperature. It increases by 0.6 dB from nominal to TTTH test, as illustrated in Figure 3.11. In the worst case, the NF reaches 2.93 dB at SS, 125°C, 1.2V and 2.4 GHz (SSTH), which is an acceptable performance for most 2.4 GHz applications.

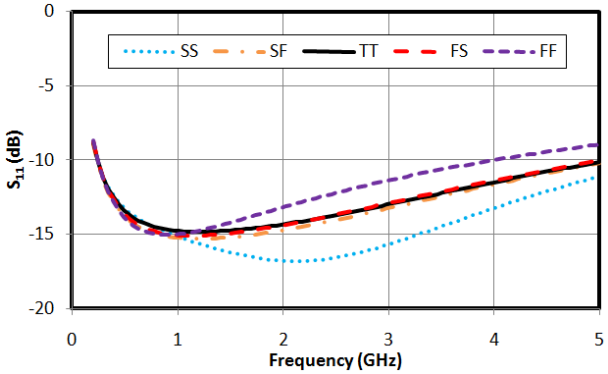


Figure 3.12 – S_{11} variation to process corners at 27°C and 1.3V

Figure 3.12 shows the behavior of the input matching versus process corners at 27°C and 1.3V. We can note the input matching bandwidth is reduced in FF corner, the S_{11} is lower than -12 dB from 300 MHz to 3 GHz. For this worst case condition the input matching still covers the targeted bandwidth, it is not an issue. The degradation of the input return loss is mainly caused by the increase in G_{m1} which reduces the real part of the input impedance $\Re(Z_{in})$. It can be compensated by the reduction of the current on the main amplifier, through the control voltage V_c.

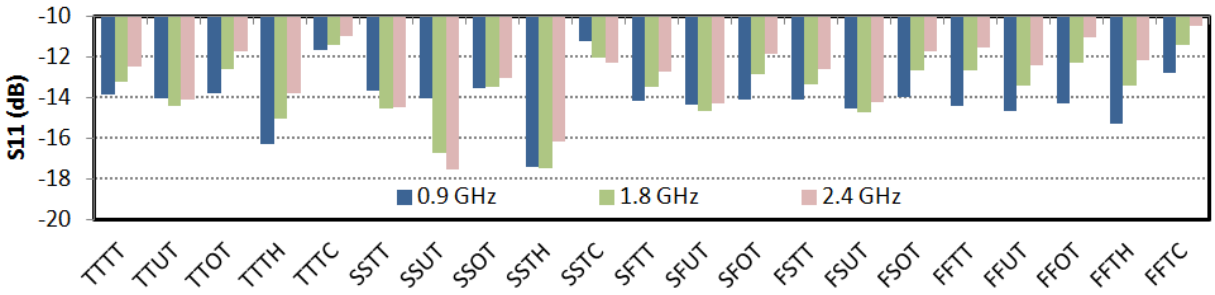


Figure 3.13 – S_{11} variation to PVT corners

Figure 3.13 shows the S_{11} performance at three frequencies of interest for the PVT corners. It shows almost the same variability with process, voltage or temperature, deviating less than 2 dB from the nominal corner. In the worst case corner, at 2.4 GHz, the S_{11} is -10.5 dB at FF -40°C and 1.3V (FFTC), which is adequate for most applications, guaranteeing less than 10% return loss.

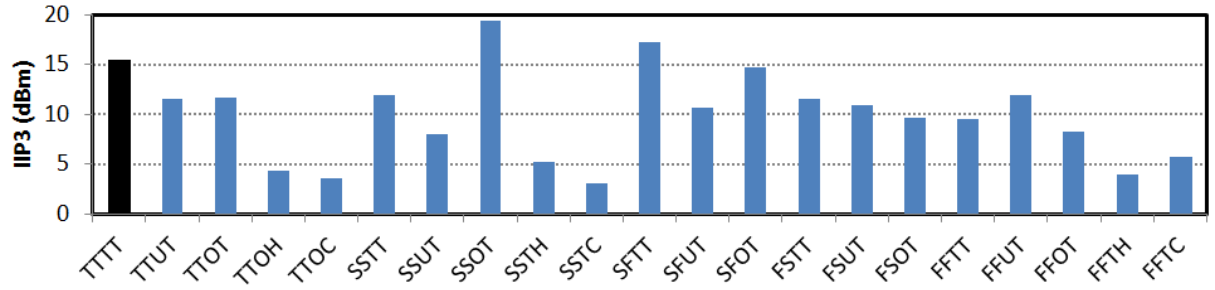


Figure 3.14 – IIP3 variation to PVT corners

The IIP_3 is the most sensitive performance of this LNA, the range of variation is 16 dB over the evaluated PVT corners as illustrated in figure 3.14. It is more sensitive to temperature than to process or voltage variations. The worst case IIP_3 is +3.1 dBm, at SS, -40°C and 1.3V (SSTC) which is an acceptable performance regarding the specifications. Besides the process and temperature variation can be compensated via the control voltage V_C.

It can be noted that NF and gain are not as sensitive to corners as IIP_3. All process variations can be compensated by appropriate values of V_C and I_{FB}.

3.2.5 Reconfigurability

This LNA has two reconfiguration knob, the supply voltage V_C which controls the bias current of the CR stage, and the feedback bias current I_{FB}. The NF can be controlled by changing V_C, as shown in Figure 3.15 a). As the bias current is

reduced, so does the transconductance, leading to an increase of NF. The gain is not affected by the variation of the bias current through V_c. Indeed the decrease (resp. increase) of the transconductance partially compensates the increase (resp. decrease) of the output resistance of the CR structure. Besides the increase of the output resistance (R_{out}) reduces the bandwidth as the dominant pole –i.e. $(1/(A_{V.}R_{out}C_{gd}))$- moves to a lower frequency.

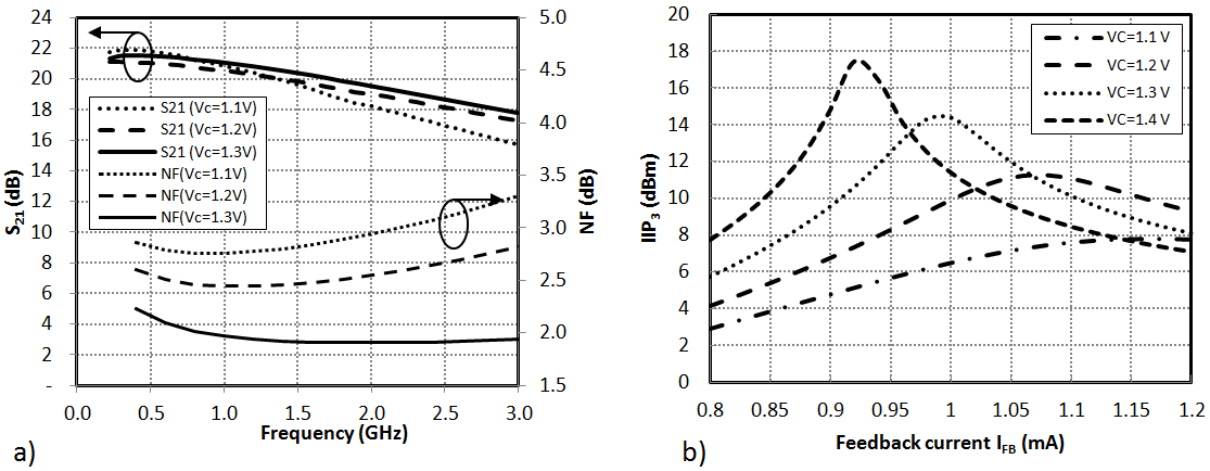


Figure 3.15 – LNA reconfigurability. a) S21, NF b) IIP3

Figure 3.15 b) shows the IIP_3 behavior versus the feedback current I_{FB} for different V_C. The IP3 improves as CR bias current increases, and for each value of V_c there is a specific current I_{FB} which optimizes the IP3, as demonstrated in chapter 2. However, the improvement of IP3 peak through V_C reduces the range of I_{FB} that control this maximum. At a V_C of 1.4V as a 5% change in I_{FB} value represents a 6 dB reduction in the IIP_3 according the PVT analysis of Section 3.2.4, whereas a 5% change in I_{FB} at a V_c of 1.2 V decreases the IP3 of only 3 dB.

3.3 CHIP2: DIGITAL FULLY RECONFIGURABLE LNA

The LNA implemented in CHIP1 has a bandwidth limited to 2.6 GHz, to extend it a two-stage version of the circuit is developed. This second LNA includes a control of the gain bandwidth and level. Two biasing DACs features the digital interface enabling a digital assisted reconfiguration of the LNA.

3.3.1 Design

Due to its limited bandwidth, the Gyrator-like LNA of CHIP1 only covers 802.11a/n/ac and LTE (higher bands). To extend the bandwidth and gain level, an additional stage is added as illustrated in Figure 3.16.

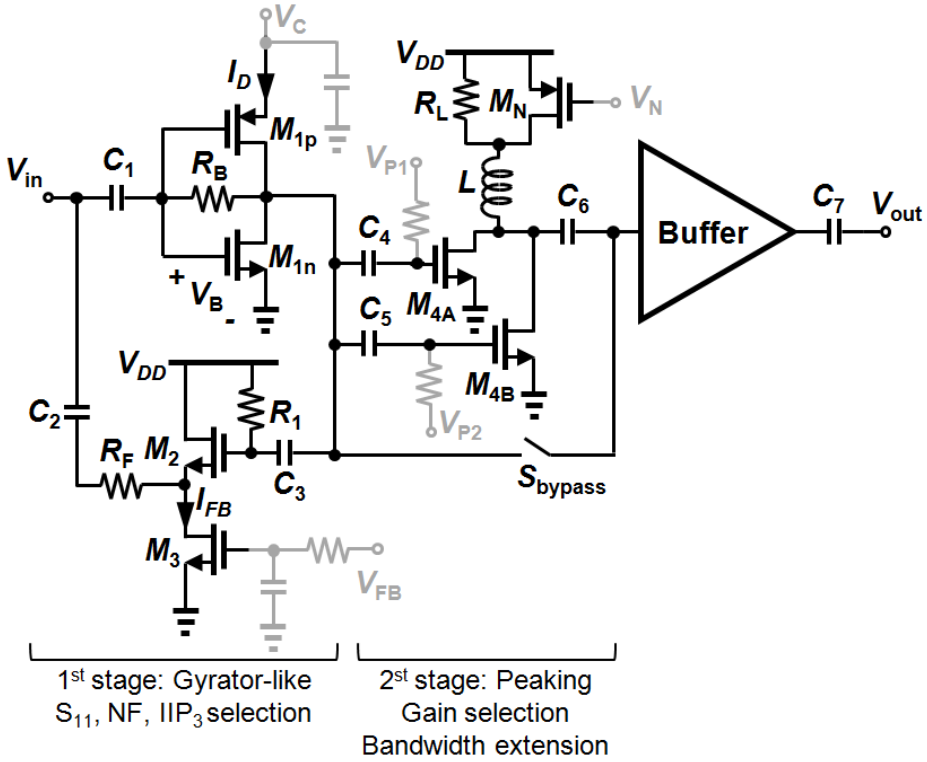


Figure 3.16 – Bandwidth extension and gain control stage

The second stage of Figure 3.16 is basically a common source configuration loaded by a low-Q peaking inductor. The level of gain is adjusted by a variation of the transconductance g_m. A current mirror controlled by a DAC steers the current of the common source stage. The shunt peaking is performed by the inductor L in series with resistor R_L. At low frequency R_L dominates which does not change the shape of the gain response. At high frequency the inductor L compensates for the -20dB/dec roll-off of the first stage thus extending the overall bandwidth of the LNA (SHEKHAR; WALLING; ALLSTOT, 2006). The transistor M_N is used as a switch to bypass the resistor R_L. When R_L is by-passed the quality factor (Q) of L increases and a narrowband behavior is achieved. To effectively improve Q the on-state resistance R_{on} of the switch S_{narrow} must be as small as possible, a large transistor is needed. However increasing the size of the transistor yields to large parasitic capacitors which

reduces the bandwidth of second stage. A good trade-off for transistor ML is $W_{S_{narrow}} = 100\ \mu m$ in this case.

The linearity of a cascade multistage LNA ($IIP3_{LNA}$) is reported in (7). The contribution of the N^{th} stage ($IIP3_{stageN}$) is magnified by the gain G_1 to G_{N-1} of the previous stages (RAZAVI, 2012). In our case, the linearity of the second stage ($IIP3_{stage2}$) is critical since the gain of the first stage (G_1) is large. The second stage of our LNA is based a common-source configuration, which basically yields large IM2 and IM3.

$$\frac{1}{IIP3_{LNA}} = \frac{1}{IIP3_{stage1}} + \frac{G_1}{IIP3_{stage2}} + \frac{G_1 G_2}{IIP3_{stage3}} + \cdots + \frac{G_1 G_2 \ldots G_{N-1}}{IIP3_{stageN}} \quad (7)$$

To enhance the linearity of the second stage, it is implemented with a modified version combining to parallel common source stages. The principle of the derivative superposition (DS) method (APARIN; LARSON, 2005) is exposed in Figure 3.17. The NMOS transistors M_A and M_B, Figure 3.17a), are not biased in the same region of operation: M_A is in super-threshold region and M_B is in sub-threshold region. The derivatives of the transconductance g_{3A} and g_{3B} cancel-out for a range of V_{gs} close to 0.5V, Figure 3.17b), thus resulting in a g_3 close to zero and a significant improvement of the IP3. The cancellation of g_3 with DS method offers a larger range of biasing control than the optimal gate biasing (APARIN; BROWN; LARSON, 2004) technique. Hence the DS approach is more robust to PVT variations.

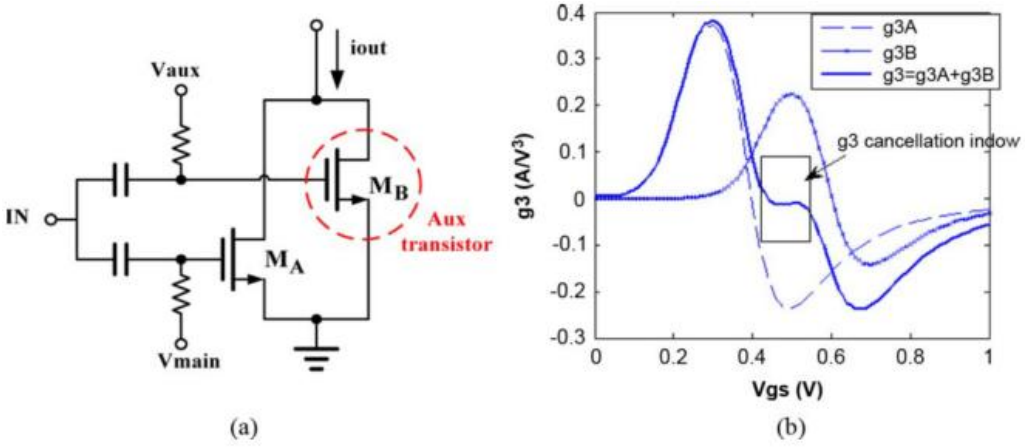


Figure 3.17 – DS method with dual-NMOSs. (b) Third-order distortion terms of the main transistor (g_{3A}), auxiliary transistor (g_{3B}), and total output (g_3)
Source: Adapted from (ZHANG; SANCHEZ-SINENCIO, 2011)

The region of operation of M_A and M_B in Figure 3.17 is first estimated with V_{GS} control. The DS configuration (M_{4A},M_{4B}) of Figure 3.16 is steered by two digitally controlled current, detailed in the next section, to further increase the robustness to

process variations. AC coupling between stages is implemented with the aid of MiM capacitors C_1 to C_7. Resistors are implemented with high-valued P+ poly layer to reduce the silicon footprint, except for R_F which requires an accurate value. RC filters are distributed along the bias lines to deliver stable DC voltages.

Transistors M_1 to M_4 are implemented with different numbers of 5 µm/0.13µm fingers to reduce gate noise resistance. Double-sided gate contacts are used to minimize the parasitic resistance of the poly gate material. The CHIP2 is laid-out with the same approach of CHIP1. Table 3.4 summarizes the implemented device sizes.

Table 3.4. Device sizes

M_{1N}	30 x 5 µm/130 nm	M_{F0}	4 x 5 µm/130 nm	L	4 nH	C_7	13.6 pF
M_{1P}	30 x 5 µm/130 nm	M_{F1}	4 x 5 µm/130 nm	C_1	10 pF	C_{F0}	0.68 pF
M_2	6 x 5 µm/130 nm	R_F	300 Ω	C_2	3 pF	C_{F1}	1.36 pF
M_3	2 x 5 µm/130 nm	R_B	14 kΩ	C_3	0.68 pF		
M_{4A}	12 x 5 µm/130 nm	R_1	14 kΩ	C_4	1 pF		
M_{4B}	4 x 5 µm/130 nm	R_L	50 Ω	C_5	1 pF		
M_N	20 x 5 µm/130 nm	R_{4A}	4 kΩ	C_6	2.14 pF		

The bypass switch S_{bypass} of Figure 3.16 is implemented as shown in the Figure 3.18. The parasitic capacitors are mainly due to the gate capacitors of the devices and the junction capacitors between the drain and source implants and the p-substrate of the chip. The gate capacitors consist of the gate-oxide capacitors and the overlap of the gate area with the source and drain areas. A resistor is placed in series with the gate in order to isolate the gate capacitors to ground which limits the bandwidth of the switch (DOGAN; MEYER; NIKNEJAD, 2008).

The sizing of the switch has to deals the on-resistance, the parasitic capacitance and the generation of harmonic distortions. Large dimensions lower on-resistance and insertion loss, but it increases capacitance in off-state (MADAN et al., 2011), leading to bandwidth reduction. To improve the linearity of the switch, the bulk and N-well terminals of triple-well NMOS are kept floating (from an RF standpoint) to avoid forward biasing of parasitic diodes under large input signal. In addition, the source and drain are biased at the same DC potential with a polysilicon resistor, to reduce power consumption.

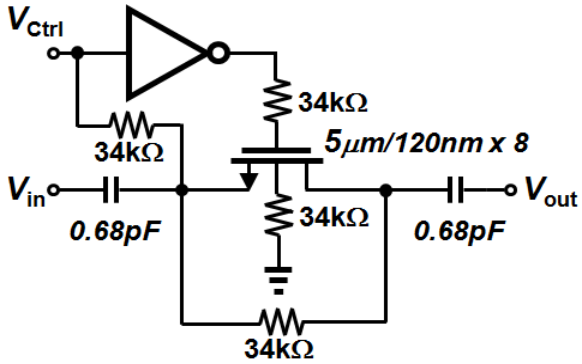


Figure 3.18. Bypass switch schematic

Isolated triple-well NMOS devices use deep N-well to isolate the P-well and divide the voltage swing in a stack of devices. The deep N-well separates the bulk of the NMOS transistors from the P-substrate. The P-well and deep N-well are left floating (from a RF standpoint), thus reducing the parasitic loss by increasing the effective impedance in the body of the device. The P-well is DC-biased at 0 V, and the deep n-well is DC-biased at V_{DD} through high valued polysilicon resistors to reverse bias the P-N junctions, reducing the parasitic capacitance associated with the diodes.

3.3.1.1**Biasing**

The LNA of CHIP2 is a complex system with several functional settings and biasing. Some adjustments, such as bandwidth selection, are controlled by switches and are inherently digital. The gain, NF and linearity, however, are controlled by the bias voltages and currents, which require digital-to-analog converters (DAC), as shown in Figure 3.19.

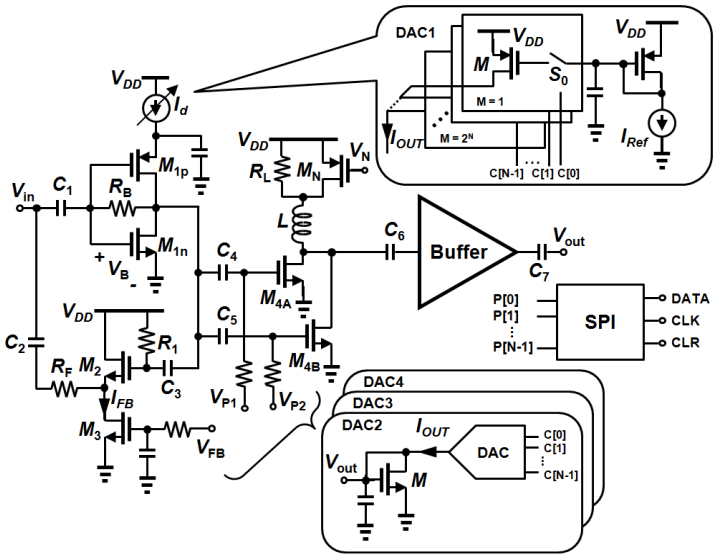


Figure 3.19 – LNA biasing with current mode DACs

To make the LNA robust to PVT variations all the biasing are implemented via current mode DACs. Four DACs are used, DAC1 to control the CR bias current I_d, with 4 bit resolution; DAC2 to control the feedback bias I_{FB}, with 3 bits; DAC3 with 4 bits to control the peaking stage main transistor M_{4A} current; and DAC4 with 3 bits to control the auxiliary linearizing transistor M_{4B}. For this purpose, a single DAC architecture is used throughout the chip. A schematic of the design is shown in Figure 3.22 (PLETCHER; RABAEY, 2008). A simple current mirror-based topology is used, where the gate-source voltage from a reference mirror is distributed through a switch network to a device array. The current range is defined according the operating modes presented in Table 3.6, controlled via a digital word applied to the bit lines. The unit devices are sized with a length of 0.35 μm to the overall output resistance of the current DAC and robustness to process variations. Cascoding the output devices is not possible due to the low supply voltage, but the linearity of the DAC is not a primary concern for the intended bias application.

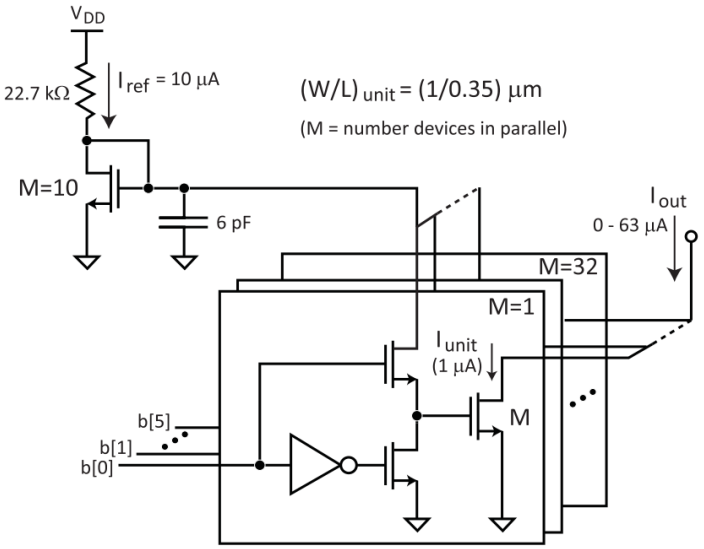


Figure 3.20 – Width variable current source
Source: Adapted from (PLETCHER; RABAEY, 2008)

As already mentioned, in the current-reuse structure, the gate-source voltage is set by the resistor R_B in a self-biased configuration that maintains $V_{GS} = V_{DS}$. To reconfigure this stage the current I_d is controlled via P version of the DAC connected to the source of the M_{1P}. The source of M1P is AC coupled to the ground with C_{bypass} in Figure 3.21b).

In the feedback, however, the source of M_2 is connected to a signal node and a capacitance would shunt the signal down. The best strategy is to use a single transistor M_3 and bias it through a current mirror. In the reference current of this current mirror, a P-mode DAC must be added to control M_2 bias current. A low pass filter is needed at the gate of M_3 to reduce the noise bandwidth and noise contribution of the current mirror.

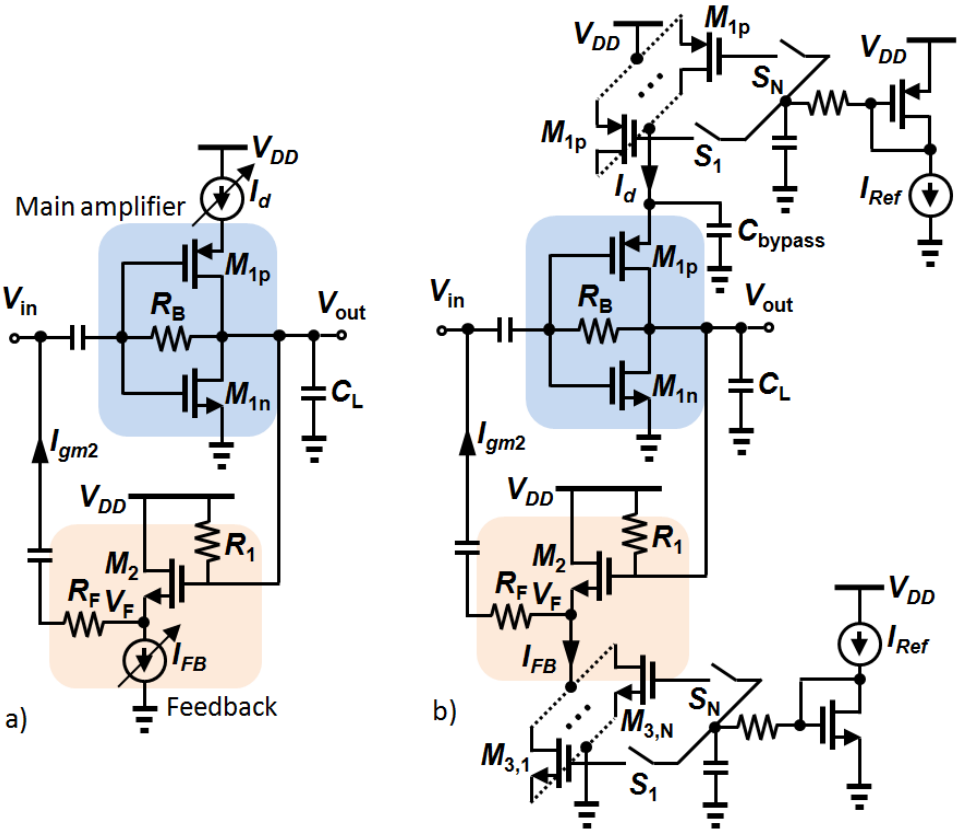


Figure 3.21 – Current-reuse biasing a) Reconfigurability b) Transistor level implementation

Similarly to the feedback is the biasing of the second stage, Figure 3.22. As the RF signal is connected to the gate of M_{4A} and M_{4B}, a special attention is needed for the biasing. A DAC is used to control the reference current of a current mirror (HU et al., 2008), which in turn controls the transistor bias current. This configuration avoids a segmented approach for the mirroring transistor that would need a coupling capacitor for each branch (Figure 3.22.b). Small transistors are preferred for the implementation of the switches. Indeed a small parasitic capacitance allows for a better control of the capacitive charge that affects the first stage, and reduces the silicon area.

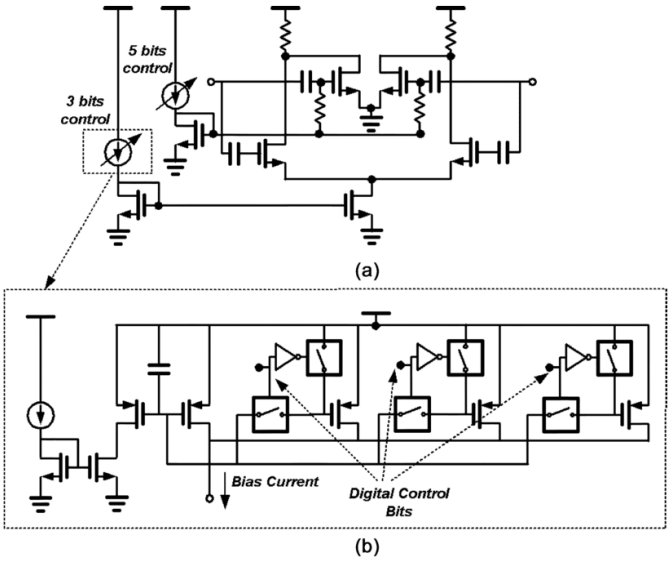


Figure 3.22 – Width variable current source
Source: Adapted from (KIM; KIM, 2006).

With these biasing considerations, the LNA can be reconfigured with a minimal degradation of noise performance, furthermore the PVT variations can be compensated in the field, leading to a flexible and robust solution.

3.3.1.2 **Design for testability**

Several digital inputs are required to control the DACs and the bypass switches. A digital serial peripheral interface (SPI) and register set presented in Figure 3.23 are integrated on chip. It receives the configuration words from a computer and stores the digital settings on-chip. This digital approach of the control saves I/O pads (4 instead of 18) and simplifies the test set up by reducing the number of supply access. In the implementation of a single-chip CMOS Tx/Rx system, the DSP directly addresses the LNA registers through a data bus.

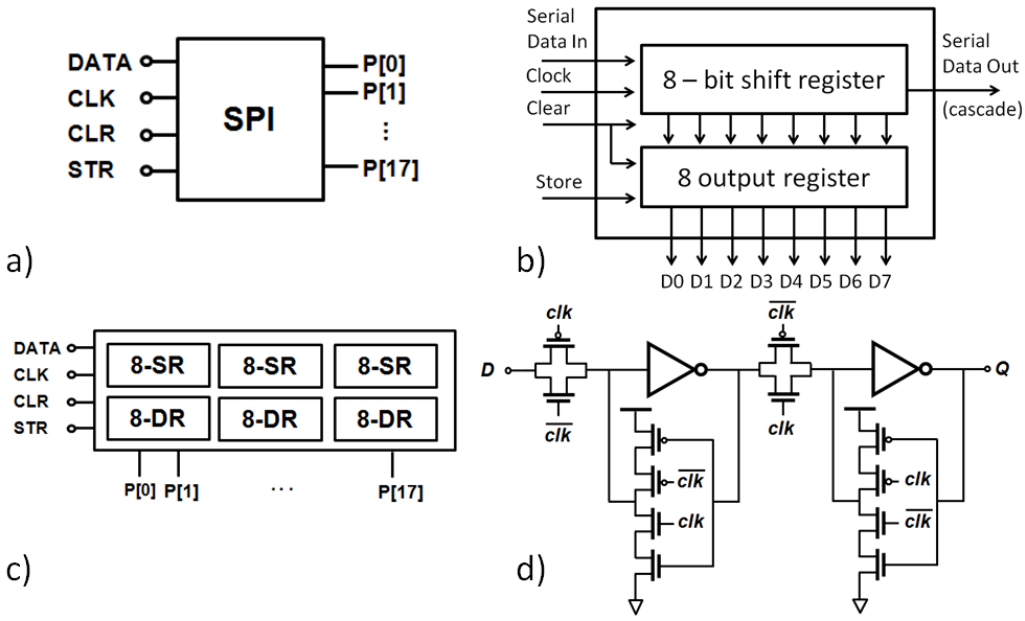


Figure 3.23 – a) Serial peripheral interface b) block diagram c) 8 bit shift register and output register d) TG-C^{2}MOS DFF

The SPI block is implemented with three shift registers (SR) and D-type register (DR) blocks cascaded as shown in Figure 3.23.c). Each block is composed of an 8-bit SR and a storage register (DR). The configuration data (DATA) is a serial stream sent from the external controlling board. At each clock (CLK) pulse, the data shifted across the SR and the output of one SR is connected to the input is connected to the next. At the end of the 24 bit word, the bit lines (P0-P17) are modified with a pulse (STORE). To reduce the chances of failure of the SPI, since an LNA would be reconfigured only a few times per second, a low clock frequency (20 kHz) is chosen. The registers of the SPI are implemented with an static Flip-Flop structure, a TG-C^{2}MOS DFF (Transmission Gate – Clocked CMOS D-type Flip-Flop) (PEDRONI, 2008), as shown in Figure 3.23. Due to access restrictions of digital blocks layout in the 130 nm technology provided by MOSIS service, and then the inability to simulate the digital and analog parts together, the SPI was manually designed and laid-out.

3.3.2 Layout considerations

Figure 3.24 shows the layout of CHIP2 featuring a digital reconfiguration of the LNA.

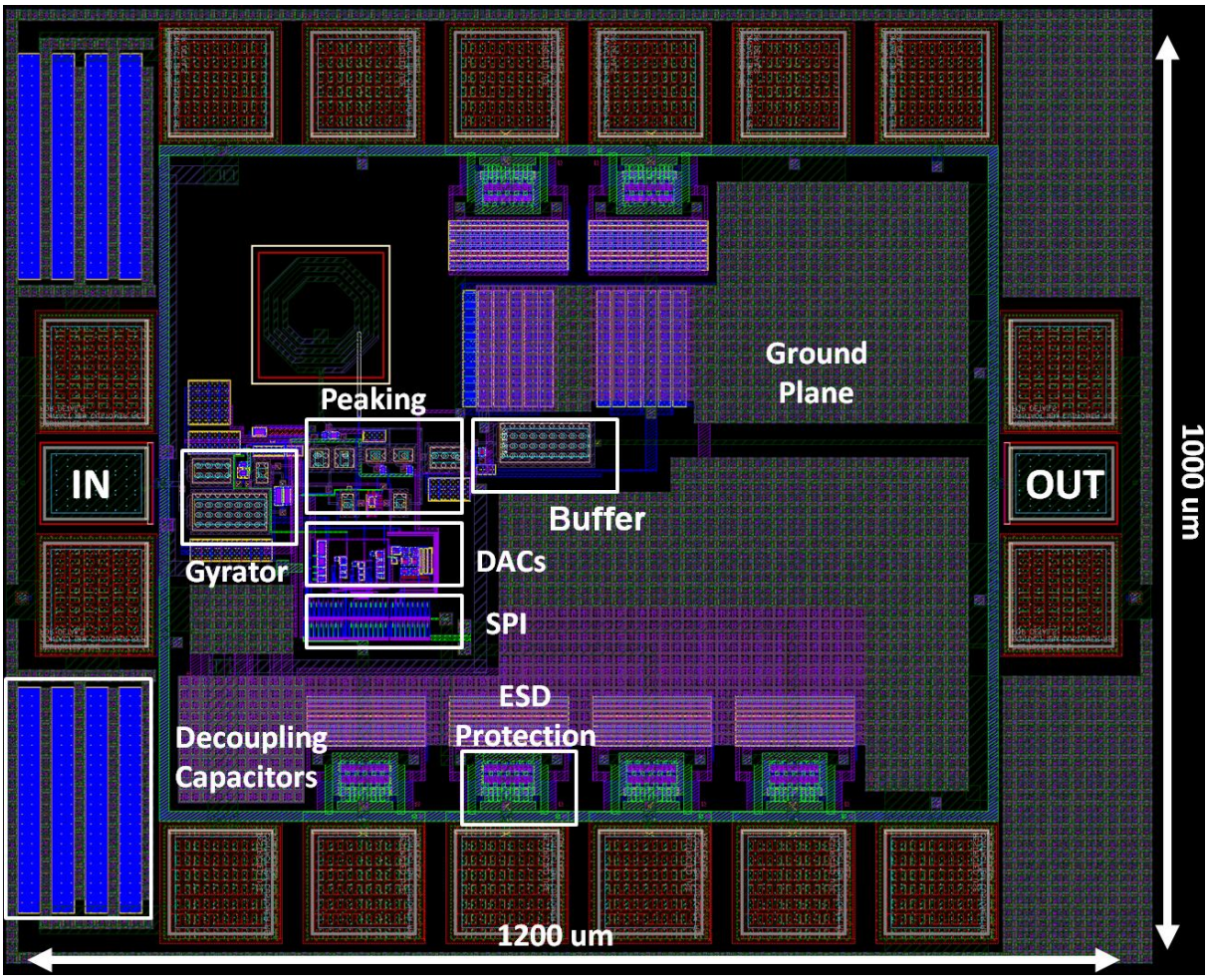


Figure 3.24 – CHIP2 Layout

With 1200 um x 1000 um, the circuit is pad-limited, and most of the area is filled with the ground plane. The first stage based on gyrator-like configuration of CHIP1 is placed as close as possible to the input, to reduce the resistance access. Next, the RF signal is amplified by the second stage, then the output buffer is connected the output pad. Below the peaking stage are the DACs and the SPI. MOS capacitors are distributed across the chip for decoupling proposes.

Reverse-biased P^+ and N^+ diffusion diodes are used for pin-to-rail ESD power clamp. Each diode has an area of approximately 50 um x 70 um and capacitance of 250 fF. The low resistance discharge of the diodes contribute to stabilize the DC I/O, the main supply voltage V_{DD} and the common ground GND (MAK; MARTINS, 2009). Due to the high capacitance of the clamp diodes, and the thick oxide used in the 130 nm technology, the RF pins are not ESD protected. The ESD robustness of these pins is simulated using the Human Body Model (HBM)

reference circuit (ESDA; JEDEC, 2012). The simulation results shows the pin withstand 4 kV of ESD testing.

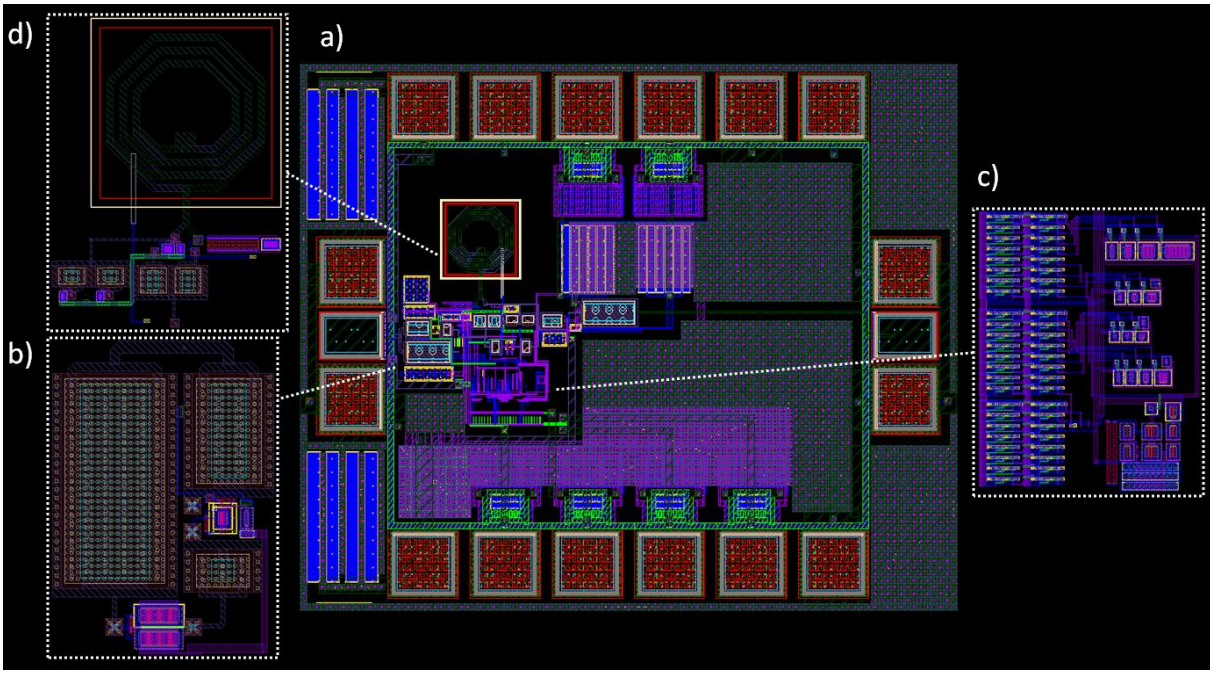


Figure 3.25 – Digital LNA layout. a) chip layout b) gyrator stage c) peaking stage d) SPI and bias generation

Figure 3.25 shows a zoom in of the main blocks. In Figure 3.25(b) is the first stage of the chain, the gyrator block, laid-out as close as possible to the input pads. The area is dedicated to the coupling capacitors. The CR structure is on the bottom, the feedback is placed on the right side. The active blocks take place in a 410 um x 250 um area only. Figure 3.25(d) shows the peaking stage where most of the area is occupied by the inductor. Figure 3.25(c) shows, on the left, the SPI and on the right the bias generation circuit. On the bottom-right is the current reference and on the top-right are the current DACs.

3.3.3 Post-layout simulation results

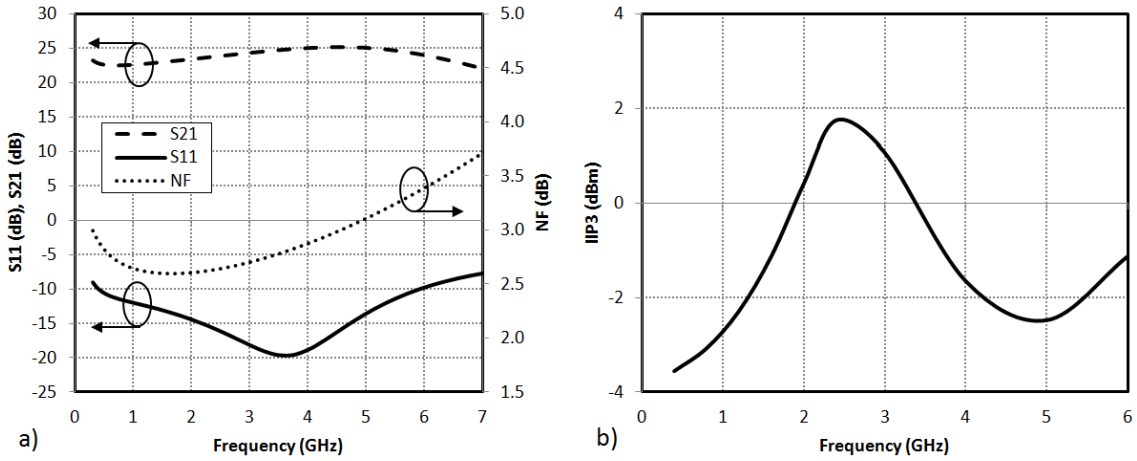


Figure 3.26 – PLS results at high performance (P_{DC} = 16.9 mW). a) S_{21}, S_{11} and NF b) IIP3

Figure 3.14 shows the PLS results of the LNA in high performance mode. The voltage gain, Figure 3.27.a), reaches a maximum of 25 dB and achieves a -3 dB bandwidth of 7 GHz. The input return loss (S_{11}) is lower than -10 dB from 400 MHz to 6 GHz which is consistent with the gain bandwidth. The NF remains below 3.5 dB across this entire band, with a minimum of 2.6 dB at 1.8 GHz. The IIP_3 is shown in Figure 3.26.b), the maximum is 1.8 dBm at 2.4 GHz, the minimum is -3.6 dBm at 300 MHz. The IIP_3 performance of the two-stage LNA is clearly below the simulated results of the gyrator-like LNA of CHIP1. In CHIP2 the linearity is dominated by the second stage because it deals with a signal already amplified by the first stage. Indeed a large amplification in the first stage is prompt to saturate the second stage. The overall IP3 of the LNA is limited by the linearity of the second stage and the gain of the first.

3.3.4 PVT sensitivity

Table 3.5 – PVT corner list. Evaluated (black), unevaluated (gray)

		Process				
VDD	**Temp**	**TT**	**SS**	**SF**	**FS**	**FF**
1.4 (O)	-40 (C)	TTOC	SSOC	SFOC	FSOC	FFOC
	27 (T)	TTOT	SSOT	SFOT	FSOT	FFOT
	125 (H)	TTOH	SSOH	SFOH	FSOH	FFOH
1.3 (T)	-40 (C)	TTTC	SSTC	SFTC	FSTC	FFTC
	27 (T)	TTTT	SSTT	SFTT	FSTT	FFTT
	125 (H)	TTTH	SSTH	SFTH	FSTH	FFTH
1.2 (U)	-40 (C)	TTUC	SSUC	SFUC	FSUC	FFUC
	27 (T)	TTUT	SSUT	SFUT	FSUT	FFUT
	125 (H)	TTUH	SSUH	SFUH	FSUH	FFUH

To evaluate the circuit sensitivity to PVT, it is configured in high performance mode and is tested with the corner simulations highlighted in Table 3.5.

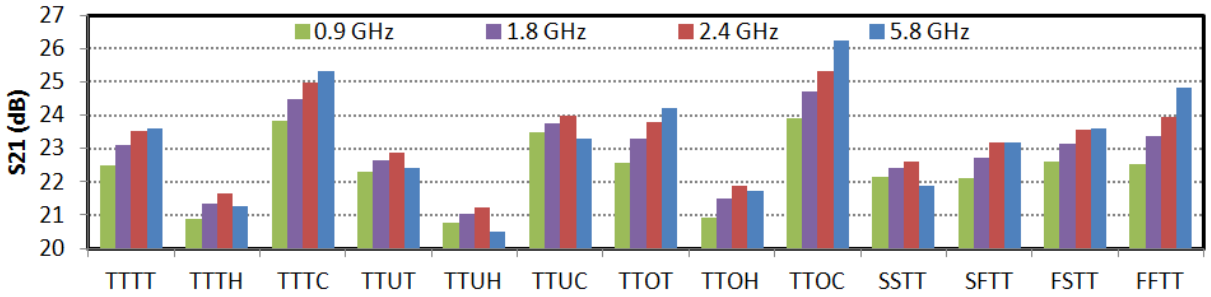


Figure 3.27 – S_{21} variation to PVT corners

Figure 3.27 shows the dependency of gain to PVT for four frequencies of interest. It shows less than 2 dB variation with temperature, from 27°C (TTTT) to 125°C (TTTH) or -40°C (TTTC), for all frequencies. The gain and frequency ripple increase with temperature decrease. However it is low sensitive to voltage with an increase of only 1dB from 1.2 V (TTTT) to 1.1 V (TTUT) or 1.3 V (TTOT). The sensitivity to process is also very low, only 1 dB variation across all process corners. The gain flatness, however, varies from less than 1 dB to almost 3 dB from SS to FF. In the worst-case scenario, at TT process, 1.1V and 125°C (TTUH) the gain reaches about 21 dB which is sufficient for most applications.

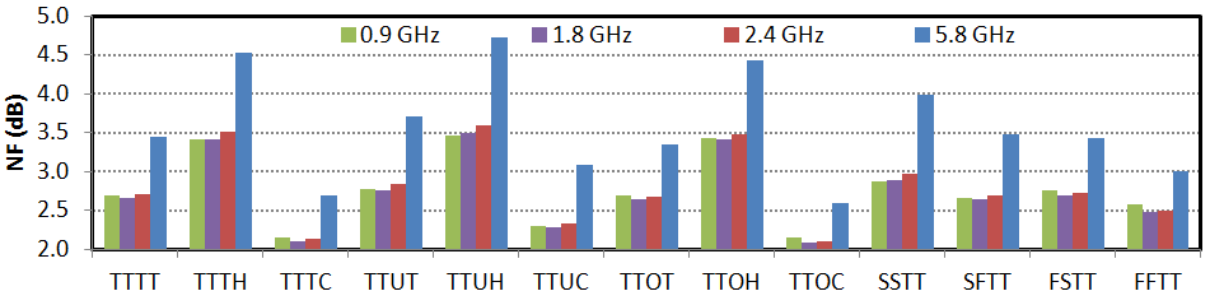


Figure 3.28 – NF variation to PVT corners

Figure 3.28 shows the NF variation with PVT for the four frequencies of interest. As shown in Figure 3.26a), the NF at 5.8 GHz is approximately 1 dB higher than at lower frequencies due to the gain rolls-off of the first stage. Figure 3.28 shows that the NF is moderately sensitive to temperature, varying about 0.9 dB from nominal to TTTH corners, and 0.6 dB from nominal to TTTC. The sensitivity to process is lower, the NF variation remains below 0.6 dB across all the evaluated corners. The only process corner that degrades linearity from the nominal is the SS, the NF increase is only 0.3 dB in this case, which is still acceptable for most of targeted applications. In the worst-case scenario, at TTUH, the NF is 4.7 dB at 5.8 GHz and remains below 3.6 dB in the other targeted frequencies.

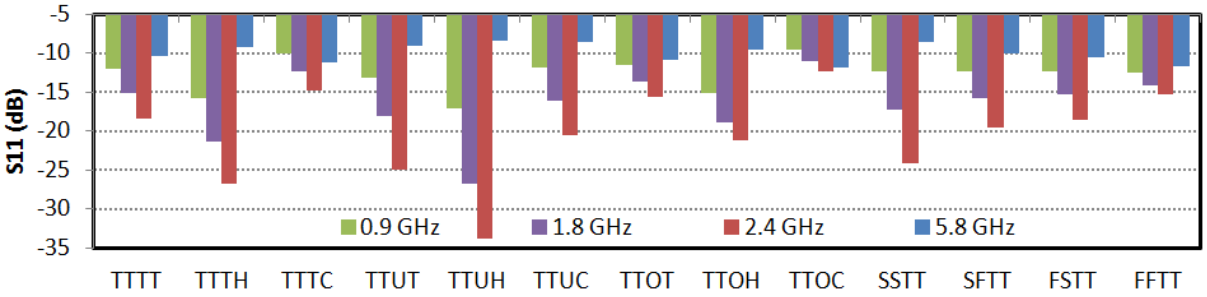


Figure 3.29 – S_{11} variation to PVT corners

Figure 3.29 shows the input impedance matching performance across the different PVT corners for the four frequencies of interest. The input impedance matching provided by the gyrator-like stage is dependent to frequency and PVT. At 900 MHz the variability to temperature, voltage or process remains below 5 dB from nominal corner. However, the combination of them produces a larger variability, but still guarantees good results. From 900 MHz to 2.4 GHz, good impedance matching is achieved at all corners. At 5.8 GHz, at some of the corners the S_{11} is between -8 dB and -10 dB, which is not ideal, but still adequate for most applications as the power reflected to the antenna remains below 16%.

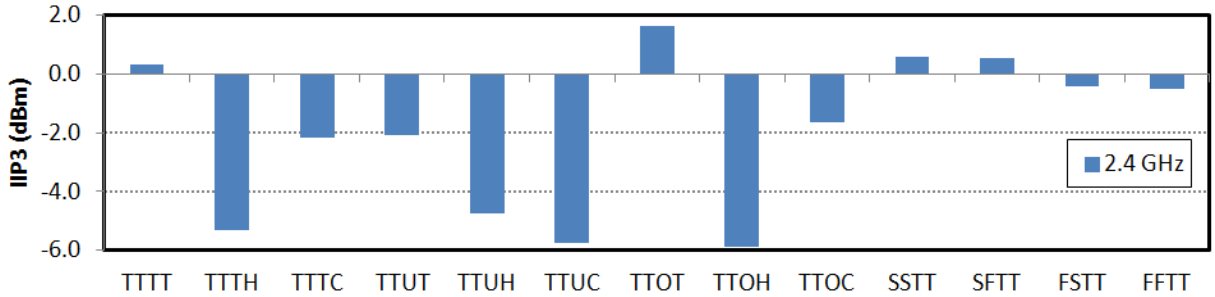


Figure 3.30 – IIP3 variation to PVT corners

To evaluate the IIP_3 sensitivity to PVT, a frequency at the middle of the available bandwidth is used, in this case 2.4 GHz, the results are shown in Figure 3.30. The linearity of the circuit is almost insensitive to process with less than 1dB variation. It is more sensitive to temperature, with almost 6 dB variation between TTTH and nominal corners. However, this sensitivity can be partially reduced through the bias reconfiguration of the LNA. The sensitivity to supply voltage is lower than to temperature and can be mitigated with the DACs in post-production calibration or built-in self-tests (BIST).

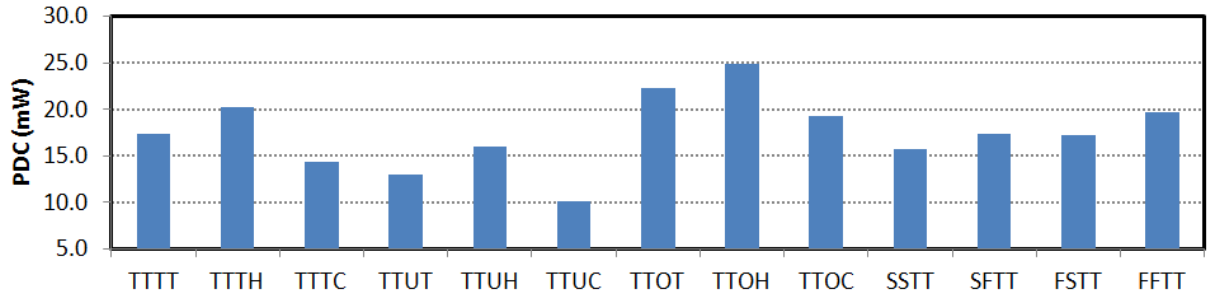


Figure 3.31 – P_{DC} variation to PVT corners

Figure 3.31 shows the dependence of the power consumption to PVT corners. We observe a 10% variation through process corners, 17% variation through the temperature corners and 28% variation to supply voltage, from nominal to TTOT corners. This behavior is explained by the self-biased current-reuse structures of the gyrator-like stage. It can be compensated with the current mode DAC steering the current of the CR stage.

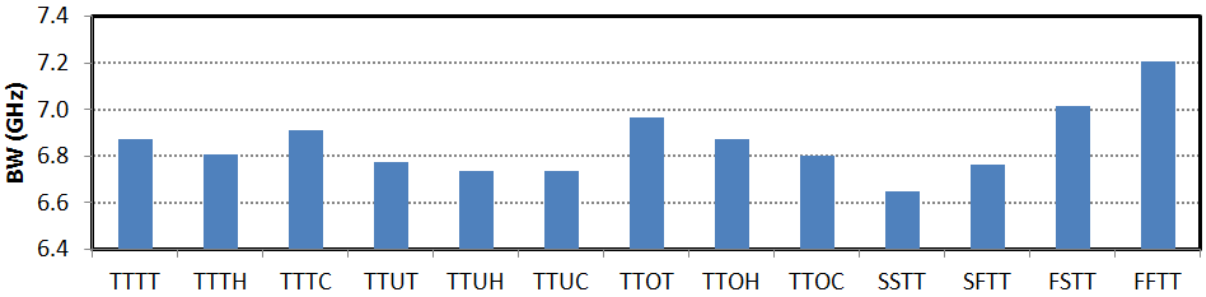


Figure 3.32 – BW variation to PVT corners

The -3 dB bandwidth (BW) variation to PVT corners is shown in Figure 3.32. It is almost insensitive to temperature or supply voltage. A low sensitivity to process is observed with 5% variation. The BW reduction at SSTT is due to the reduced f_T of the MOS transistors. In the worst-case scenario, the BW is still 6.6 GHz which is enough to cover all the targeted standards.

3.3.5 Reconfiguration

The NF of the LNA is dominated by the gyrator stage that can be adjusted by changing G_{m1} through I_{d1} bias current with a DAC. The gain ($A_V = G_{m1}r_o$) of this stage is almost insensitive to I_{d1}, as the output resistance is inversely proportional to I_{d1} and $G_{m1}$is directly proportional to it. The gain is then controlled by the bias of the peaking stage, as shown in Figure 3.33. It achieves a control of the signal level at the input of the mixer, preventing for saturation or incorrect signal demodulation. The input impedance is tuned by the feedback bias current I_{FB}.

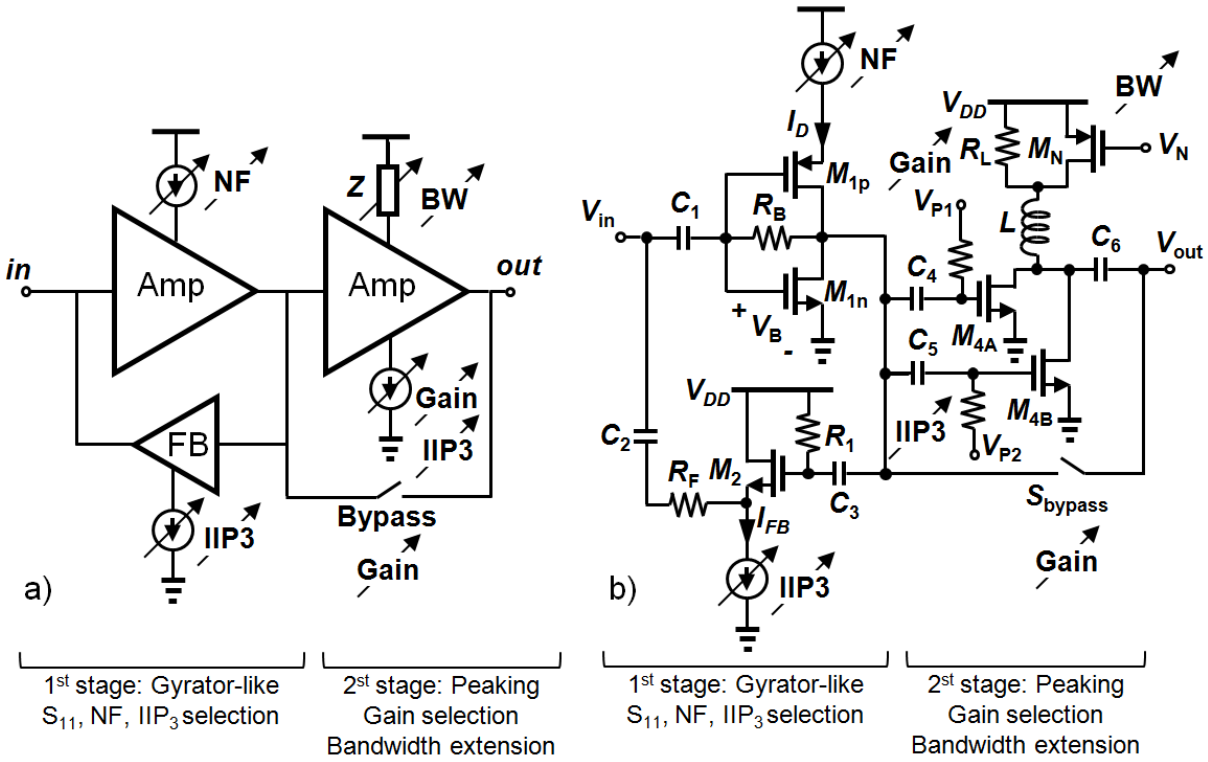


Figure 3.33 – LNA reconfiguration. a) system level b) transistor level

The peaking stage is only needed at high frequency, above 2.6 GHz, and/or a higher gain is required. To save power and improve the linearity, a bypass switch can shunt the second stage when the LNA operates below 2.5 GHz. In the gyrator stage, the IIP_3 is adjusted through I_D and I_{FB}, as illustrated in the previous section.

With this capabilities, the LNA can be reconfigured in S_{11}, NF, Gain, IIP_3 and bandwidth to adapt different scenarios of radio link with power saving.

Among the large number of bias current and switch combinations, some relevant configurations of them are reported in Table 3.6 with the corresponding mode of operation of the LNA.

Table 3.6 – CHIP2 Operation Modes.

Name	Mode	Band	I_{CR} (mA)	I_{FB} (mA)	I_{P1} (mA)	C	S_{bypass}	V_N
BHL	high linearity	bypass	7.3	1.00	0.5	0	high	high
BLN	low noise	bypass	5.0	0.13	0	0	high	high
BLP	low power	bypass	3.1	0.13	0	0	high	high
NHL	high linearity	narrow	7.3	1.00	9.2	0.1	low	low
NLN	low noise	narrow	5.0	0.13	5.4	0	low	low
NLP	low Power	narrow	3.1	0.25	2.2	0	low	low
WG2	low noise	wide	5.0	0.13	2.2	0	low	high
WG3	low noise	wide	5.0	0.13	1.2	0	low	high
WG4	low noise	wide	5.0	0.13	0.5	0	low	high
WG5	low noise	wide	5.0	0.13	0.5	0	high	high
WHL	high linearity	wide	7.3	1.00	9.2	0.1	low	high
WLN	low noise	wide	5.0	0.13	5.4	0	low	high
WLP	low power	wide	3.1	0.25	2.2	0	low	high

The results of post-layout simulations of the LNA for these configurations are shown next.

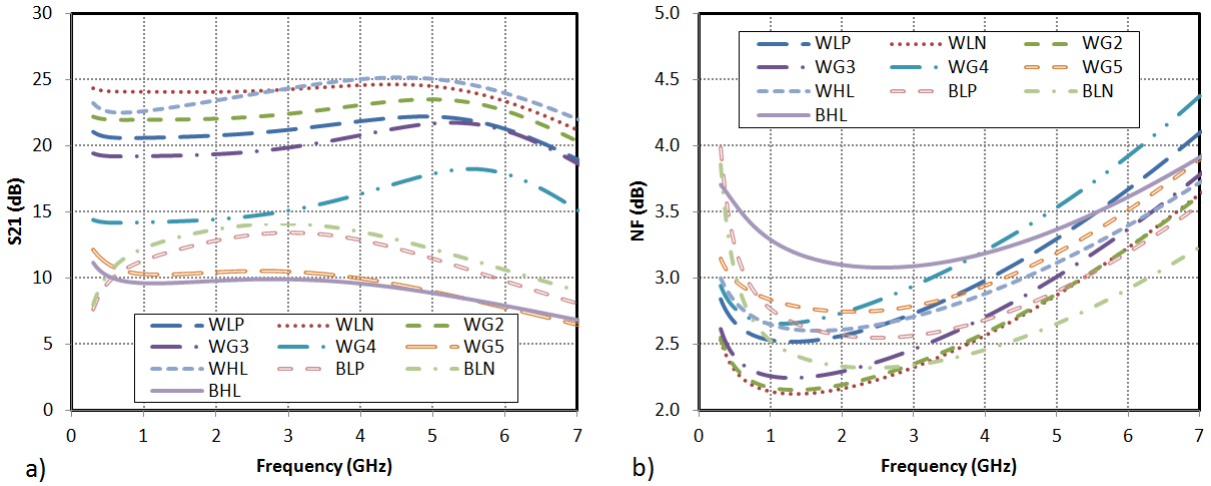


Figure 3.34 – Reconfigurability a) S21 b) NF

Figure 3.25.a) illustrates the gain for each configuration. It shows more than 15 dB gain control ratio, with different bandwidths. In Figure 3.25.b) shows that the NF varies by 1dB with a 0.1 dB to 0.2 dB step. Interestingly the NF is below 4 dB up to 6 GHz even in low power modes (WLP, BLP).

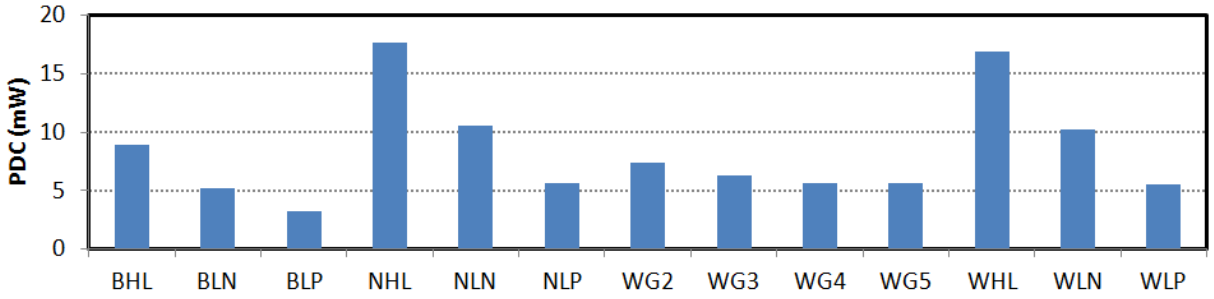


Figure 3.35 – P_{DC} vs Configuration

Figure 3.35 shows the power consumption for the different modes. In the lowest power mode (BLP), with the peaking stage turned off, the LNA consumes 3 mW with 5 GHz bandwidth, 10 dB gain a NF lower than 3.5 dB over the entire bandwidth. In WLP mode, with the peaking stage on, the LNA consumes 5.5 mW, reaching a bandwidth of 7 GHz with a maximum gain of 20 dB. In WLN mode, the consumption reaches 10.2 mW, the bandwidth is 6.5 GHz with a flatness band of 5GHz. The NF is only 2.1 dB from 1 to 2GHz, and below 3dB up to 5.4 GHz.

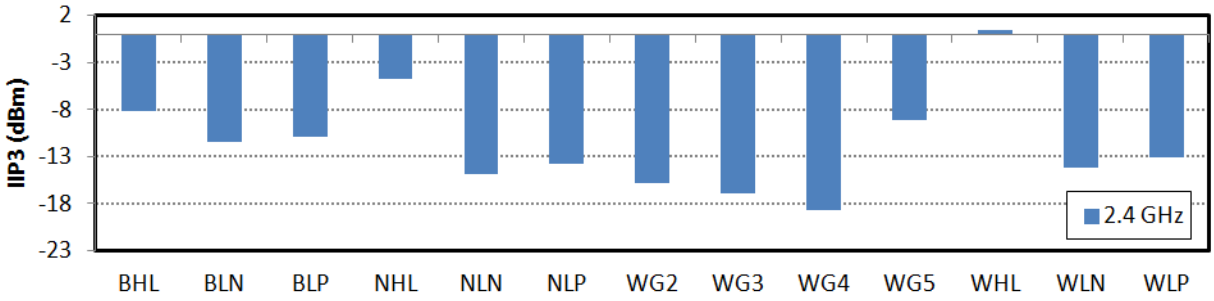


Figure 3.36 – IIP3 vs Configuration

Figure 3.36 shows the IIP_3 for each configuration at 2.4 GHz, which is a popular frequency. As discussed, the linearity of this two stage LNA is inferior to the linearity of CHIP1. In WHL, it reaches +1 dBm, which meets the requirements presented in Chapter 1. However, this linearity is achieved at a cost of a large power consumption, 17 mW. In a receiver, this configuration will be selected when the level of the desired signal is weak and a strong blocker is present.

3.4 SUMMARY

In this chapter, two inductorless wideband LNAs with reconfiguration capabilities are investigated. A design methodology is proposed and discussed. It is further applied to implementation of the circuits. CHIP1 is an inductorless gyrator-like

LNA featuring an IP3 optimization, a variation of NF and 3 modes of operation. CHIP2 is a two stage LNA combining a first stage based on the LNA core of CHIP1, and a peaking stage to extend the overall bandwidth and control the voltage gain. The second LNA includes several bias DACs and a digital interface to tune the voltage gain, the bandwidth, the linearity and the NF. 5 modes of operation are proposed for this LNA among 64 possible combinations. The PLS results of each mode of operation are reported in Table 3.7. To compare both LNAs, the NF, Gain and IIP_3 are simulated at 2.4 GHz and the result are applied to the FOM equation (4).

Table 3.7. LNA Performance Summary (PLS)

Ref	BW (GHz)	NF (dB)	Gain (dB)	IIP3 (dBm)	Supply (V)	P_{DC} (mW)	Area (mm^2)	FOM (dB)
CHIP1, mode 1	1.4	3.1	17.2	+5.3	1	1.5	0.007	26.8
CHIP1, mode 2	2.1	2.6	18.3	+7.7	1.1	3.1	0.007	32.0
CHIP1, mode 3	2.0	2.4	18.8	+17.6	1.3	7.0	0.007	45.8
CHIP2, BLP	5.6	2.5	13.2	-10.8	1.4	3.3	0.102	-1.8
CHIP2, WLP	6.9	2.6	20.9	-13	1.4	5.5	0.102	-1.6
CHIP2, WG5	4.9	2.7	10.5	-9.1	1.4	5.7	0.102	-8.0
CHIP2, WLN	6.8	2.2	24.2	-14.2	1.4	10.2	0.102	-4.3
CHIP2, WHL	6.9	2.6	23.8	+0.5	1.4	16.9	0.102	18.6

CHIP1 is a single stage LNA featuring a specific tuning to optimize the IP3. This linearity does compare favorably with CHIP2 which is a two stage LNA. However, the bandwidth of CHIP2 is more than 3 times larger than the bandwidth of CHIP1, with similar noise performance. CHIP2 allows for 13.7 dB gain control, the gain of CHIP1 is fixed. For the two LNA the power consumption can be reduced by a factor of 4.

The circuits were fabricated through MOSIS service (“MOSIS Educational Program (MEP)”, [s.d.]), in Sep-2015, and characterized in Feb-2016. The measurement results are reported and discussed in Chapter 4.

4 EXPERIMENTAL RESULTS

The two LNAs presented in Chapter 3 are implemented in Global Foundries 130 nm CMOS process. The circuits are developed with standard-V_t transistors with no specific manufacture feature. Only RF Metal-Insulator-Metal (MiM) capacitors are used for their high linearity and high capacitance density. The circuits were designed at IMS Laboratory/Bordeaux as part of a 12-month internship of an International Joint Doctorate Supervision Brazil/France (UTF-PR/UB). The chips were sent to fabrication to the MOSIS service/USA through the (“MOSIS Educational Program (MEP)”, [s.d.]), in Sep-2015, and characterized in Feb-2016 at the IMS Laboratory.

4.1 MEASUREMENT SETUP

The measurement investigations aim to validate the performance of the circuits for any of the proposed configurations. A comparison between the simulated and experimental results will determine the effect of non-idealities (parasitics, temperature variations, substrate leakage, device failure, effects of interferers and noise sources, etc.). To evaluate the intrinsic performance of the circuits, a micro-probe test set up is performed on the wafer. The probe station used for the characterization of the circuits is shown in Figure 4.1, along with a micrograph of the device under test (DUT).

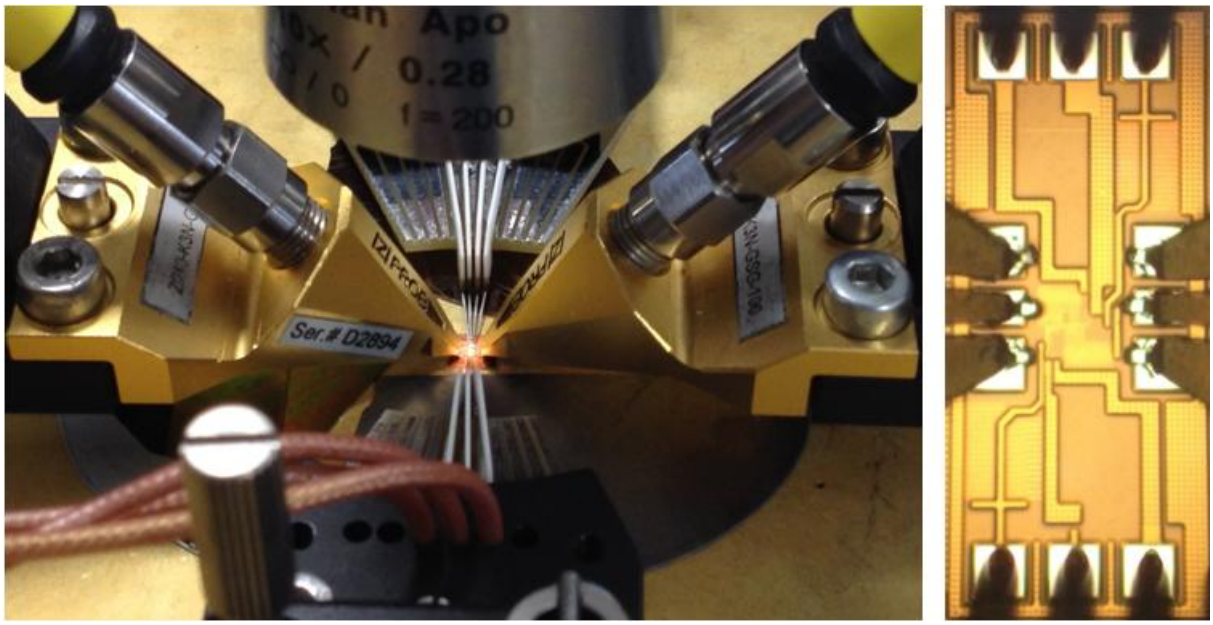


Figure 4.1 – RF wafer probe station and chip under measurement

Each period of measurement starts with a short, open, load, through (SOLT) calibration before the test of any circuit.

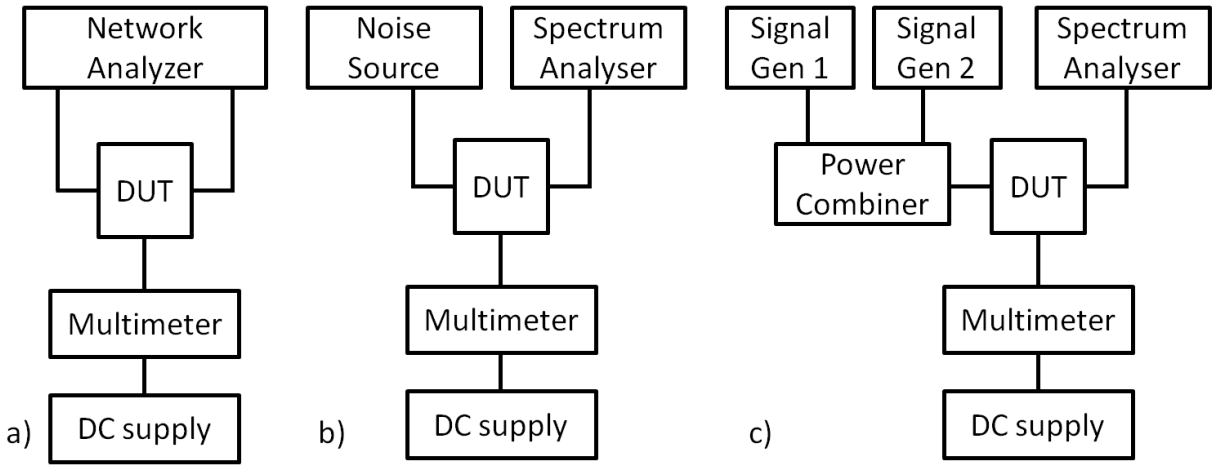


Figure 4.2 – Measurement setups. a) S-parameters setup b) NF setup c) IIP3 setup.

The measurement setups used to evaluate the S-parameters, NF and IIP3 are shown in Figure 4.2. The list of facilities used for the tests are listed in Table 4.1.

Table 4.1 – Measurement instruments

Instrument	Description
Spectrum Analyzer	Rohde&Schwarz FSUP Signal Source Analyzer
Network Analyzer	Keysight PNA-X Network Analyzer N5242A
Signal Generator 1	HP E4433B (250kHz - 4GHz)
Signal Generator 2	Rohde & Schwarz SMF 100A
Power combiner	ET industries D-0518-2
Noise Source	HP 346C
Multimeter	HP 34401A

Due to the 4 GHz limit of the Signal Generator 1 and the 1 GHz lower limit of the Signal Gererator 2, the IIP3 is only evaluated in a 1 to 4 GHz range.

The losses of the measurement setup and the output buffer are de-embedded in the measurement results discussed in this chapter.

4.2 CHIP1: SINGLE STAGE INDUCTORLESS GYRATOR-LIKE LNA

The broadband inductorless gyrator-like LNA is first tested. It is expected to cover a 0.4-3.0 GHz band. The targeted wireless standards are: GSM, UMTS, LTE, Bluetooth, 802.11b/g.

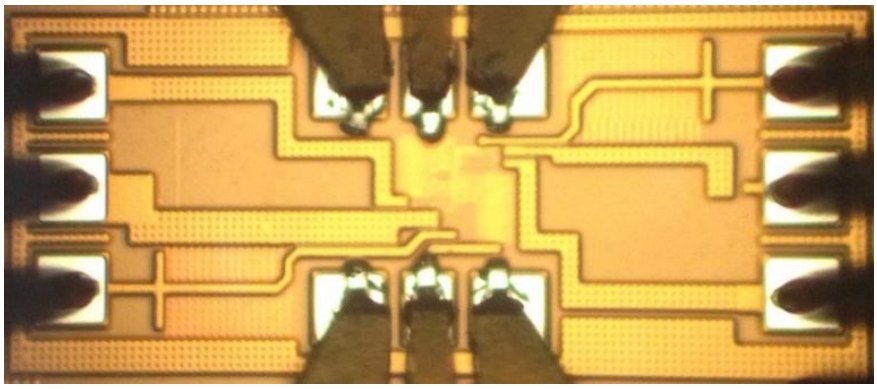


Figure 4.3 – CHIP1 micrograph.

The micrograph of the LNA is shown in Figure 4.3. It occupies an area of 0.0072 mm^2, including the MIM capacitors and excluding pads. The die size is limited by the surrounding pads dedicated to the test of the circuit. To allow for more flexibility, this circuit is biased with current/voltage sources directly connected to the diode-connected reference branch of the current mirrors.

4.2.1 Measurement results

The chip measurements are performed by on-wafer probing. DC decoupled micro-probes were used to guarantee stable DC supply voltages. The power consumption is 7 mW in mode 3, 3.1 mW in mode 2, and 1.5 mW in mode 1. A Keysight N5242A network analyzer is used to work out the S-parameters.

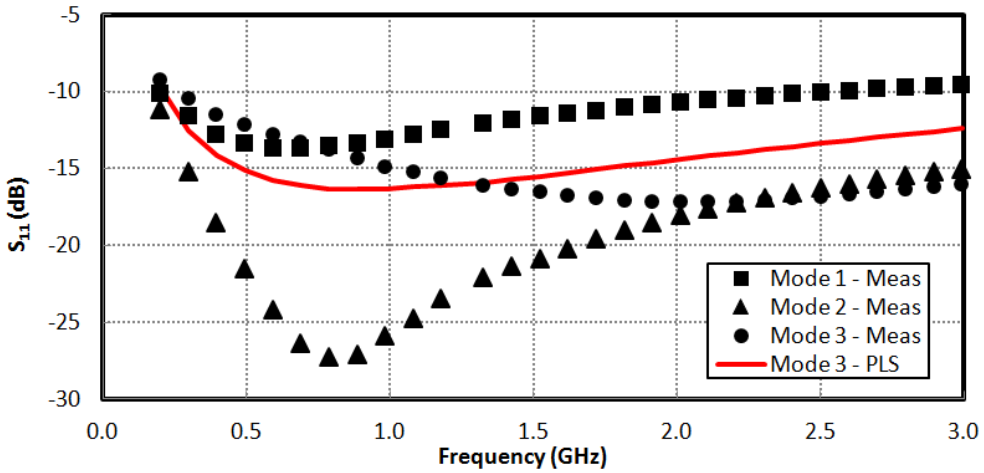


Figure 4.4 – S_{11}, measured vs PLS (post layout simulation).

The measured input return loss in mode 1, 2 and 3, along with post layout simulation (PLS) results for mode 3 (for comparison issues), are presented in Figure 4.4. The measured S_{11} is below -10 dB from 400 MHz to 3 GHz, for all modes of

operation as expected. A larger input bandwidth is achieved in mode 2 and 3 as an increase of the current in the CR stage broaden the gyrator effect.

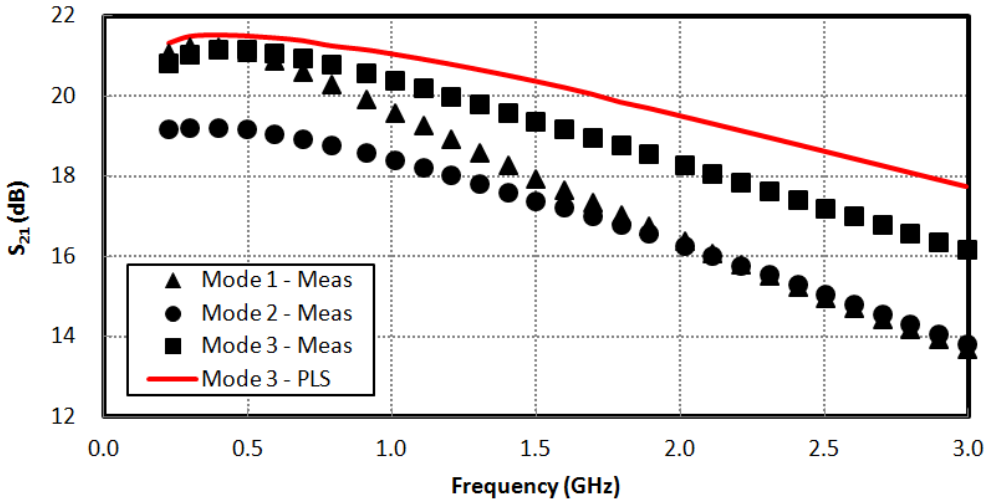


Figure 4.5 – S_{21}, measured vs PLS.

The measured S_{21} is displayed in Figure 4.5. The gain of the LNA is produced by the main amplifier – i.e. CR stage. In modes 3 and 2, the bandwidth, 2.1 GHz, is identical. The maximum gain is, respectively, 21.1 dB and 19.1 dB at 900 MHz. In mode 1, namely low power configuration, the bandwidth is reduced to 1.2 GHz with a maximum gain of 21 dB at 900 MHz. It is interesting to note that the S_{21} remains higher than 14 dB over the entire bandwidth for any mode of operation. Hence, this LNA can significantly reduce the noise contribution of any subsequent stages in any configuration.

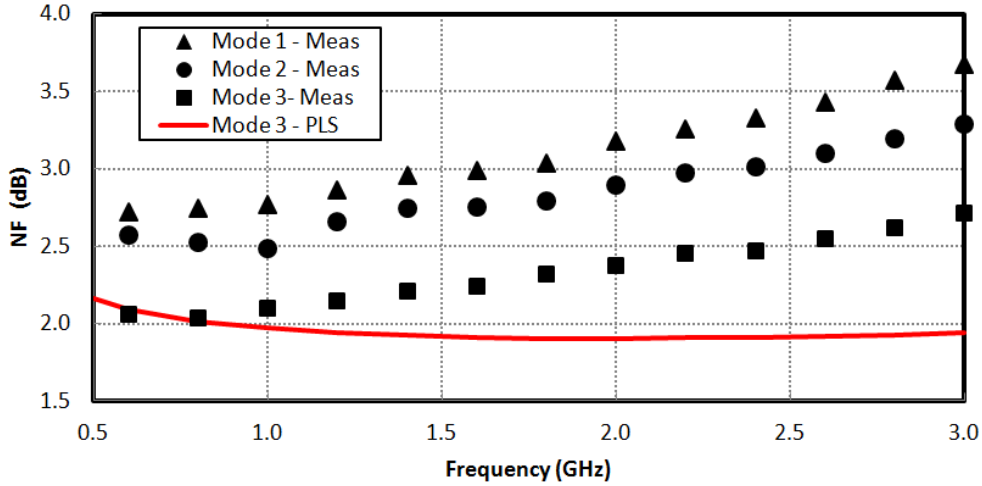


Figure 4.6 – Noise figure, measured vs PLS.

Noise performance is measured using a R&S FSUP spectrum analyzer, along with a HP 346C noise source. The measured noise figure is plotted in Figure 4.6. The noise figure is minimum at 900 MHz : 2 dB in mode 3, 2.6 dB in mode 2, and

3.1 dB in mode 1. Above 900 MHz, the NF grows monotonically with the frequency. At 2.8 GHz, the NF increase is 0.6 dB, but it is still relatively low: 2.6 dB in mode 3, 3.1 dB in mode 2 and 3.6 dB in mode 1. If we consider the frequency response of the circuit up to 3.8 GHz, the NF of the LNA never exceeds 3 dB in mode 3.

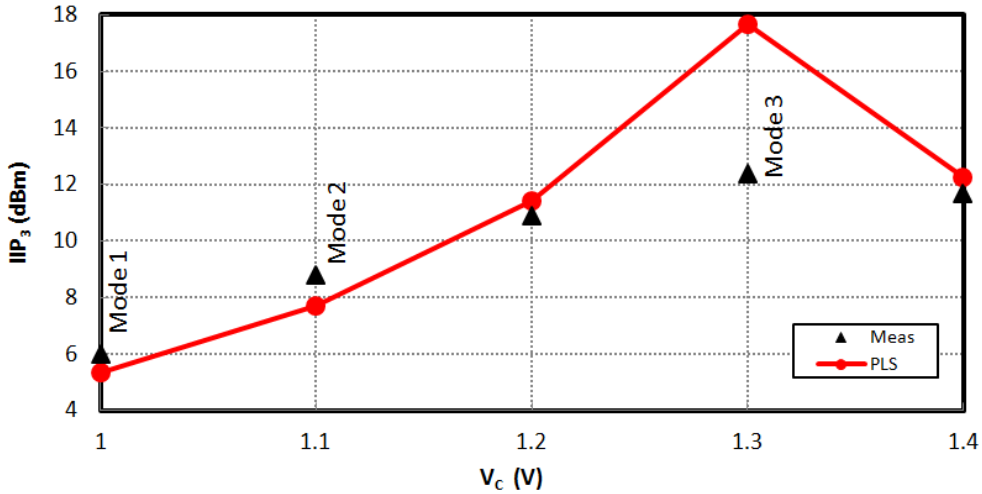


Figure 4.7 – IIP_3 for different values of V_C and respective operating modes at f_0 = 2 GHz and Δf = 20 MHz.

A two-tone measurement of intermodulation distortion is carried-out at different frequencies (f_0), with different two-tone spacings (Δf). Figure 4.7 shows the IIP_3 at $f_0 = 2\,GHz$ and $\Delta f = 20$ MHz, as a function of the supply voltage of the CR stage V_C. The measured performance closely matches the simulation results red dotted line in Figure 4.7. The combination of the derivative superposition technique in the CR stage, and the compensation of active feedback network results in a highly linear LNA. In mode 3, namely linear mode, for which the circuit is optimized to achieve the best FOM, the IIP_3 exceeds +12.4 dB. In low-power mode, the IIP_3 is still +6 dBm.

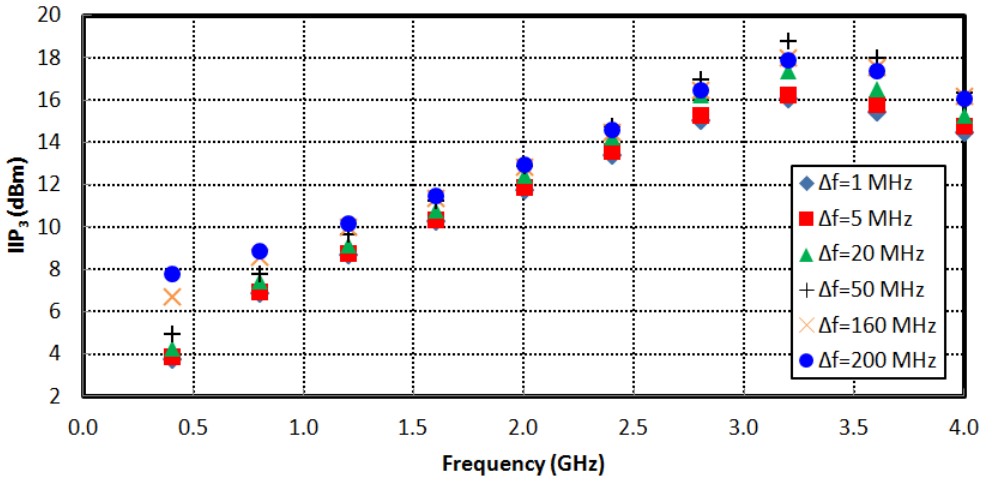


Figure 4.8 – IIP_3 vs frequency for different tone spacings (Mode 3).

In mode 3, the IM_3 is measured from 400 MHz to 4 GHz for different frequency spacings. The results (Figure 4.8) show that the IIP_3 varies less than 2 dB at a fixed frequency band, for a two-tone spacing ranging from 1 MHz to 200 MHz. We can conclude the linearity of the circuit is not dependent to the in-band blocker spacing. It must be noted that the IIP_3 improves with frequency. Indeed, the low pass response of the transfer function of the LNA filters out high order harmonics. The IIP_3 exceeds +14 dBm above 2.4 GHz, reaching +18 dBm at 3.2 GHz. It decreases to +9 dBm at 1.2 GHz and +6 dBm at 400 MHz.

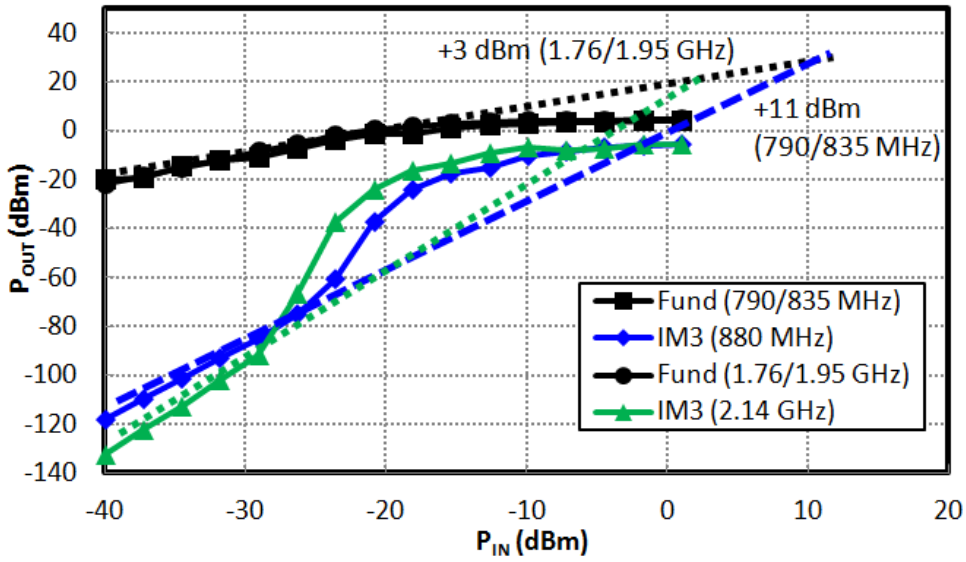


Figure 4.9 – Measured IIP_3 while evaluating the effects of cross-band blockers (Mode 3).

In broadband receivers, the effect of out-of-band blockers is critical as no filtering is performed. Notably, it is difficult to consider all the possible scenarios of desensitization caused by out-of-band blockers. However to illustrate this phenomenon, two tests are considered:

a) two continuous wave (CW) signals are generated at 1.76 GHz (DCS) and 1.95 GHz (PCS) to create an IM_3 signal at 2.14 GHz (LTE band 1/ WCDMA).

b) two CW signals are generated at 790 MHz (LTE band 14) and 835 MHz (LTE band 5) to create an IM_3 signal at 880 MHz (LTE band 6).

In configuration a) the frequency spacing is 190 MHz and in b), it is 45 MHz, with a measured IIP_3 of +11 dBm and +3 dBm respectively. In both cases the IM_3 signals remaining below -100 dBm until blocker input power reaches -30 dBm and -35 dBm, respectively. These results are illustrated in Figure 4.9 for the mode 3. The proposed LNA is robust to multi-standard cross-modulations which can frequently occur in a broadband receiver.

A single-tone test is performed at 2 GHz to measure the 1 dB compression point. The measured ICP1 is -15 dBm which is consistent with the simulation results.

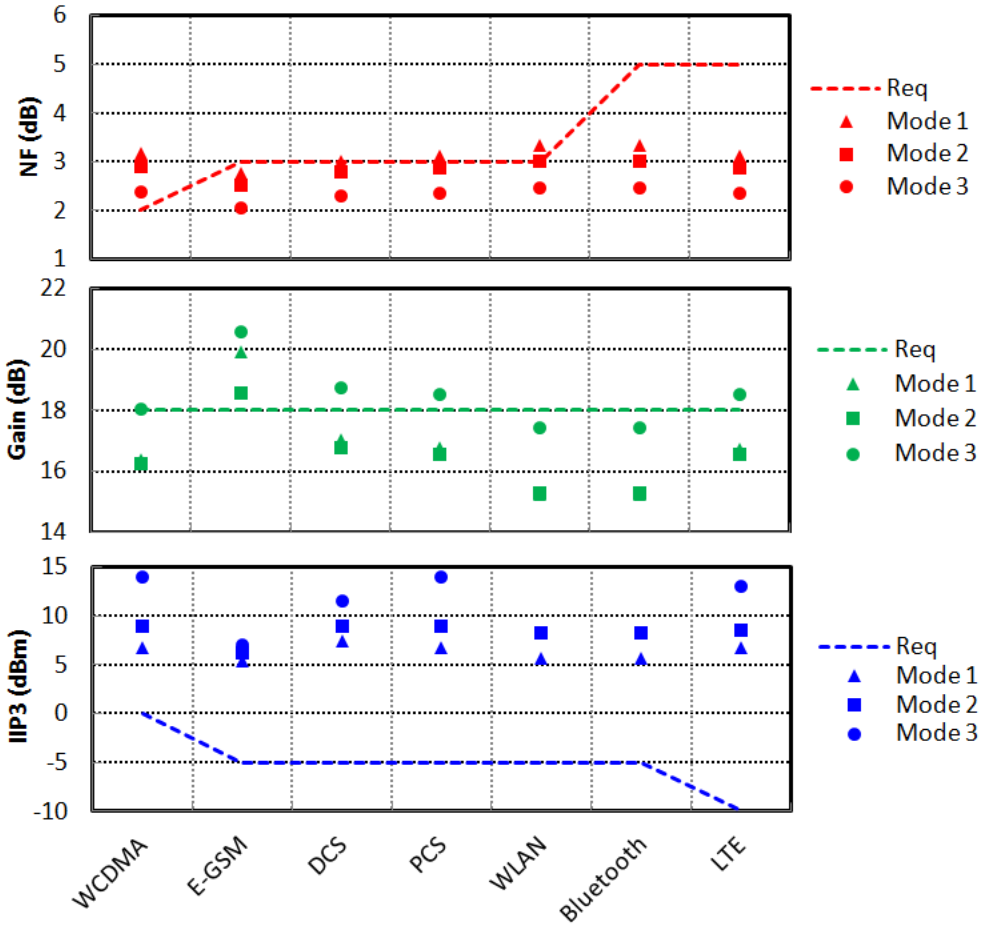


Figure 4.10 – Measured performance vs requirements.

Figure 4.10 shows the measured Gain, NF and IIP_3 (markers) for each wireless standard, with respect to the specifications (dashed line) specified in

(BRANDOLINI et al., 2005) and (INIEWSKI, 2007). The proposed LNA meets all the standard requirements in mode 3 (dot markers), except for the NF in WCDMA, which is 0.3 dB above the specification. In mode 2 (square markers) the LNA achieves almost 50% of power savings compared to mode 3. It still addresses most of the standards in terms of linearity and NF. The gain specification, set to 18 dB, is not always reached but it can be compensated with an additional gain stage in the receiver chain. In mode 1, the power consumption of the LNA is only 1.5 mW, which represents 78% more power saving compared to mode 3. In this low power mode, the NF and IIP3 of four wireless standard specifications are addressed: E-GSM, DCS, Bluetooth and LTE. The specifications in Table 1.2 are defined for a worst-case scenario of communication conditions, even though wireless devices do not always operate under these worst cases. Interestingly, the LNA performance can be also adjusted in real-time according radio link conditions in order to save more power (GIANNINI et al., 2009). Depending on the resolution of the DAC that manages the control voltage, V_C (Figure 3.3), the LNA proposed in this work can offer a great deal of performance. The digital reconfiguration of the LNA should enable the implementation of broadband software radio receivers with adaptive characteristics.

4.2.2 Discussions

To compare the different LNAs with the literature, two figures of merit are considered:

$$FOM = 20\log\frac{G.IIP_3.BW}{(F-1).P_{DC}} \quad (1)$$

$$FOM_{area} = 20\log\frac{G.IIP_3.BW}{(F-1).P_{DC}.A} \quad (2)$$

where G is the maximum gain in linear, IIP_3 is the maximum IIP_3 in mW, BW is the -3 dB bandwidth in GHz, F is the noise factor in absolute values, P_{DC} is the DC power consumption in mW and A is the active circuit area in mm^2.

The performance of the LNA is summarized in Table 4.2 along with published works. The proposed circuit achieves a very high linearity with moderate power consumption. To the best of the authors' knowledge, this LNA, which addresses most of the wireless standards in the 0.4 GHz to 2.5 GHz range, exhibits the highest FOM and FOM_{area} reported so far in literature for a broadband amplifier. Interestingly, the

technology of implementation, 130 nm CMOS, is not a limiting factor, as several works use more advanced processes, such as 90 nm and 65 nm CMOS and do not achieve a better FOM and FOM_{area}. This work demonstrates state-of-the-art noise figure and exceptionally high IIP3 for a 0.4 to 3 GHz unfiltered inductorless LNA.

Table 4.2 – Performance Comparison Of Inductorless LNAs

Ref		Tech (nm)	BW (GHz)	NF (dB)	Gain (dB)	IIP3 (dBm)	Supply (V)	P_{DC} (mW)	Area (mm^2)	FOM (dB)	FOM_{Area} (dB)
(ZHU et al., 2015)	JSSC	65	0.2-1.6	3.6	24	+14.5	1.6	20.2	0.200	27.6	41.6
(BELMAS et al., 2012)	JSSC	130	0.1-2.7	4	20	-12	1.2	1.32	0.007	-1.7	41.4
(SOBHY et al., 2011)	TMTT	90	0.1-1.77	1.85	23	-2.85	2	2.8	0.030	18.3	48.8
(PERUMANA et al., 2008)	TMTT	90	0.5-7	2.3	22	-11	1.2	12	0.012	-2.2	36.2
(CHEN; LIU, 2012)	TCAS	65	0.1-10	2.7	10.5	-3.5	1	13.7	0.020	2.0	35.9
(EL-NOZAHI et al., 2011)	JSSC	90	0-2.3	1.4	21	-1.5	1.8	18	0.060	8.5	33.0
(CHEN et al., 2008)	JSSC	130	0.8-2.1	2.6	14.5	+16	1.5	17.4	0.099	25.7	45.8
(WANG; ZHANG; YU, 2010)	TCAS	130	0.2-3.8	2.8	19	-4.2	1	5.7	0.025	7.5	39.5
(BELOSTOTSKI et al., 2012)	MWCL	65	0.01-2.8	1	32	-13.6	1.2	40	0.035	-6.6	22.5
(BORREMANS et al., 2008)	JSSC	90	0-6.5	2.7	16.5	-2	1.2	9.7	0.002	10.3	65.7
CHIP1, mode 1		**130**	**0.1-1.2**	**2.6**	**21.2**	**+6.0**	**1**	**1.52**	**0.007**	**32.2**	**75.0**
CHIP1, mode 2		**130**	**0.1-2.1**	**2.4**	**19.2**	**+8.6**	**1.1**	**3.11**	**0.007**	**35.1**	**78.0**
CHIP1, mode 3		**130**	**0.1-2.1**	**2.0**	**21.2**	**+12.4**	**1.3**	**7.059**	**0.007**	**39.8**	**82.6**

4.3 CHIP2: DIGITAL FULLY RECONFIGURABLE LNA

The two-stage LNA with digital reconfiguration proposed in chapter 3 is also implemented in the same 130nm process of Global Foundries. It is expected to cover a 0.4 to 6GHz frequency band, and to address 10 wireless standard specifications: GSM, UMTS, LTE, Bluetooth, 802.11a/b/g/n/ac and WiMAX.

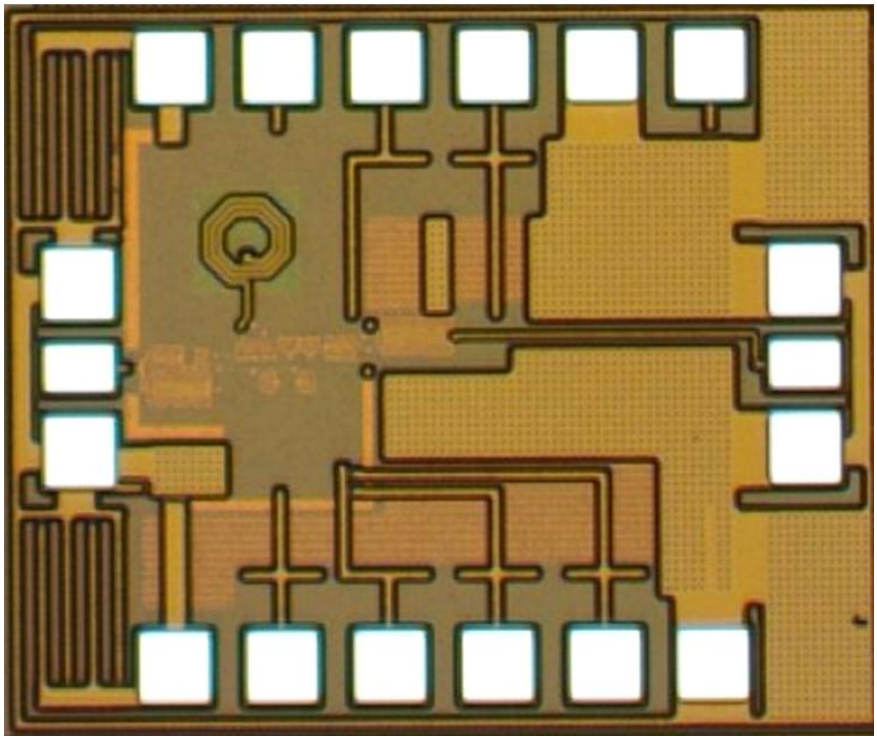


Figure 4.11 – CHIP2 micrograph.

The micrograph of the LNA is shown in Figure 4.11. It occupies an active area of 0.102 mm^2. The circuit footprint is larger than the area of the single stage gyrator LNA, CHIP1, because an inductor is required in the second stage of CHIP2. The die size remains limited by the surrounding pads dedicated to the test of the circuit.

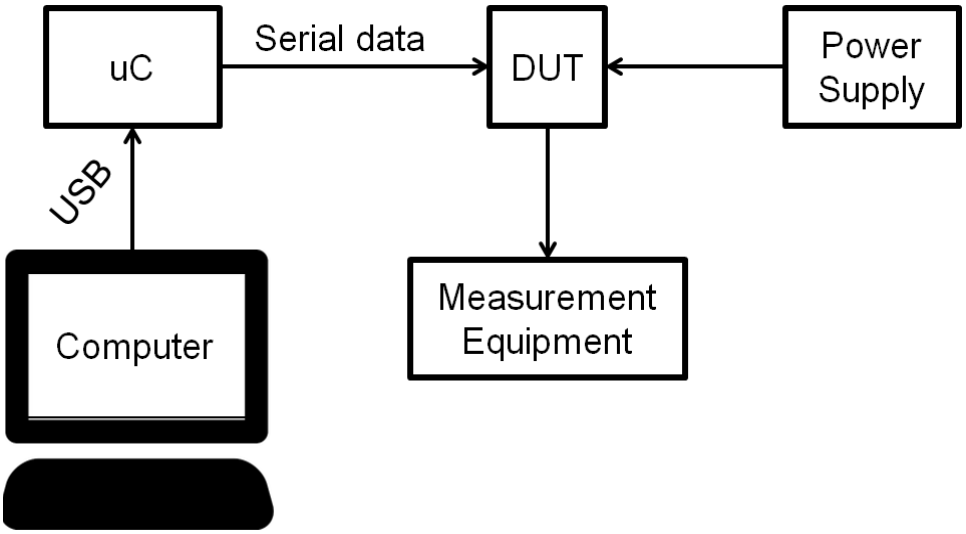


Figure 4.12 – CHIP2 measurement setup: Digital configuration of the SPI.

To control the LNA the configuration of the SPI is done through a microcontroller (μC), connected to a computer, as shown in Figure 4.12. A computer

program was developed to send the configuration words to the μC through USB port. The μC receives the configuration codes and generates the signals needed to program the SPI inside the chip. Table 4.3 shows the most relevant configuration codes that were used in measurements.

Table 4.3 – Operating mode codes

	Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mode	Word (HEX)	CR3	CR2	CR1	CR0	FB2	FB1	FB0	PK13	PK12	PK11	PK10	PK22	PK21	PK20	PK Byps	PK Wide
BHL	FE02	H	H	H	H	H	H	H	L	L	L	L	L	L	L	H	L
BLN	C802	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L
BLP	2402	L	L	H	L	L	H	L	L	L	L	L	L	L	L	H	L
NHL	FFF0	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L
NLN	C900	H	H	L	L	H	L	L	H	L	L	L	L	L	L	L	L
NLP	2480	L	L	H	L	L	H	L	L	H	L	L	L	L	L	L	L
WG2	C901	H	H	L	L	H	L	L	H	L	L	L	L	L	L	L	H
WG3	C881	H	H	L	L	H	L	L	L	H	L	L	L	L	L	L	H
WG4	C841	H	H	L	L	H	L	L	L	L	H	L	L	L	L	L	H
WG5	C821	H	H	L	L	H	L	L	L	L	L	H	L	L	L	L	H
WHL	FFF1	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	H
WLN	C98H	H	H	L	L	H	L	L	H	H	L	L	L	L	L	L	H
WLP	248H	L	L	H	L	L	H	L	L	H	L	L	L	L	L	L	H

The configuration words are composed by 16 bits, organized as follows: 4 bits to configure the bias current in the current reuse stage (CR3 to CR0); 3 bits for the feedback current (FB2 to FB0); 4 bits for peaking stage's main transistor current (PK13 to PK10); 3 bits for the auxiliary transistor (PK22 to PK20); 1 bit for peaking stage bypass (PK Byps) and 1 bit to control the Q factor of the peaking inductor (PK Wide). The codes shown in hexadecimal notation (HEX) in Table 4.3 vary from chip to chip, as the least significant bits of each bit block are used to compensate PVT variations. Each combination of these bits represents an operating mode of the LNA, named: 1) BHL, bypass, high linearity; 2) WLN, wideband, low-noise; and 3) NLP, narrowband, low-power.

4.3.1 Measurement results

Using the setup of Figure 4.2 (a), the S-parameters are measured with a Keysight N5242A network analyzer.

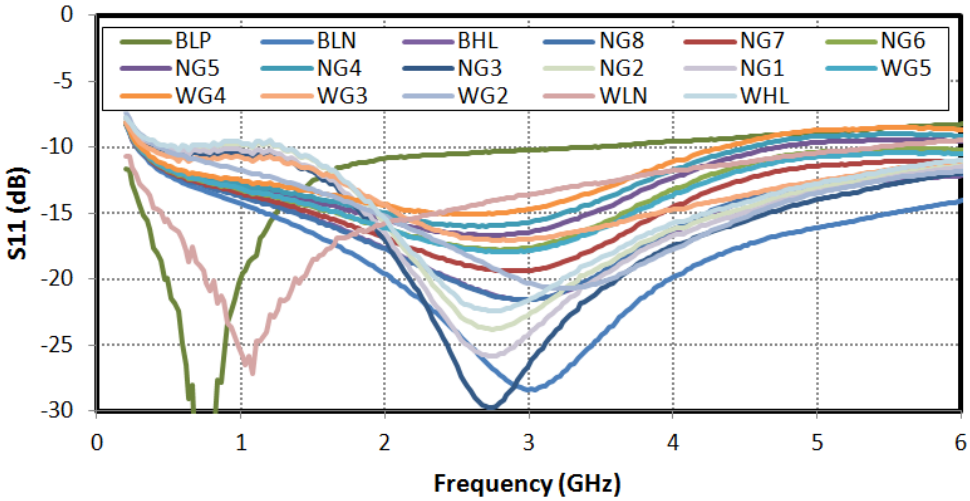


Figure 4.13 – Measured input impedance vs operating modes

The input impedance is shown in Figure 4.13 for different modes of operation. We observe two type of responses: one group with a smooth variation (WG2 to WG5), and the other group with a more significant variation (WLN, BLP, etc). The first group corresponds to a change of the bias current in the peaking stage, which changes the capacitance charging the gyrator stage. The second group corresponds to a change of the bias current in the gyrator stage. Obviously the variation of the current in the first stage has more effect on the input impedance than the second stage. Interestingly all configurations achieve a good impedance matching up to 6 GHz as illustrated with simulation results.

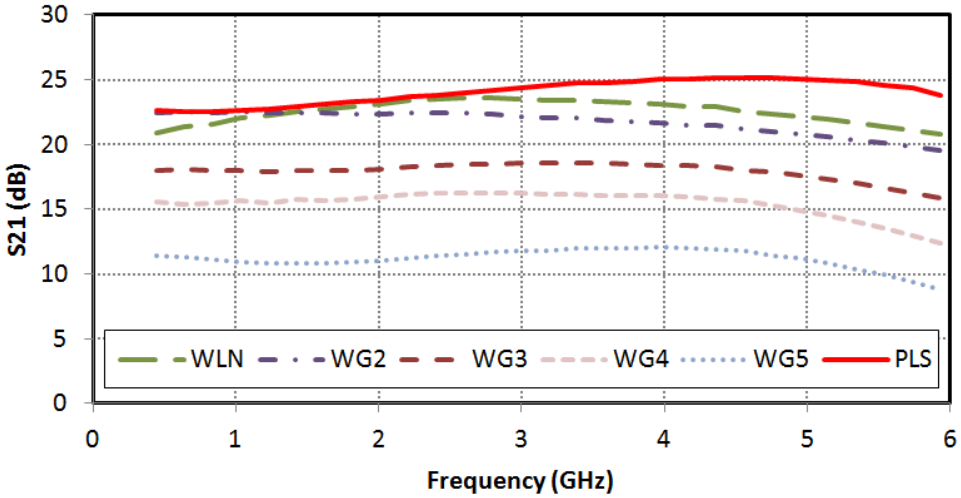


Figure 4.14 – Wideband gain control

Figure 4.15 shows the measured gain in wideband modes, which cover a 6GHz frequency band. A gain control of more than 10 dB is achieved over the entire bandwidth, with a maximum gain of 23.6 dB. The post layout simulation result is also

reported for the WLN mode, continuous red curve in Figure 4.15. The measurement and PLS results show a close form up to 3 GHz, then the measured gain slightly decreases with a maximum difference of 4 dB at 6 GHz. It is supposed that the Quality-factor of the peaking inductor is lower than expected due to parasitics and process variations. The measured performance remain consistent with PLS results, and the LNA achieves a large and broadband voltage gain in wideband modes.

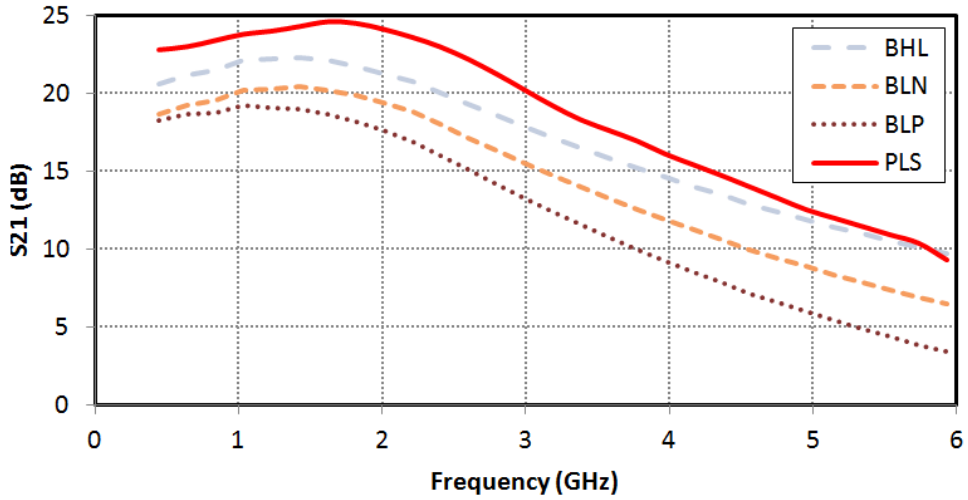


Figure 4.15 – Second stage bypassed gain control

Figure 4.15 shows the measured gain when the second stage is bypassed. Again, there is less than 3 dB difference between measurement and PLS results. A maximum gain of 22.3 dB is achieved with a -3 dB bandwidth of 2.9 GHz. According the measurement results presented for CHIP1, the gyrator-like stage does not offer a large variation of gain. The decrease of the overall transconductance is partially compensated by the increase of output resistance.

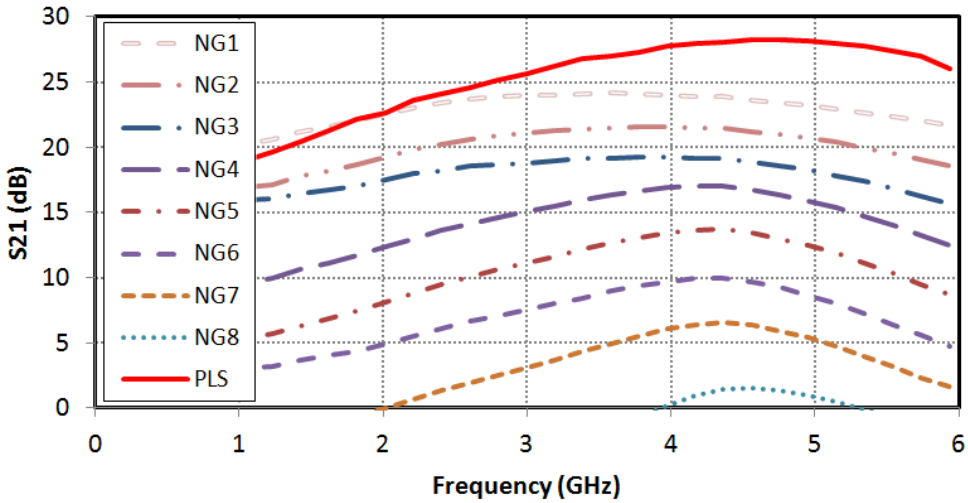


Figure 4.16 – Peaking stage gain control

Figure 4.16 shows the measurement results in enhanced gain modes, the second stage is only loaded by the inductor, the series resistor is by-passed. The gain control is large, with more than 22 dB variation. In this mode, the bandwidth is defined by the Quality-factor of the inductor and would not exceed 2.5GHz.

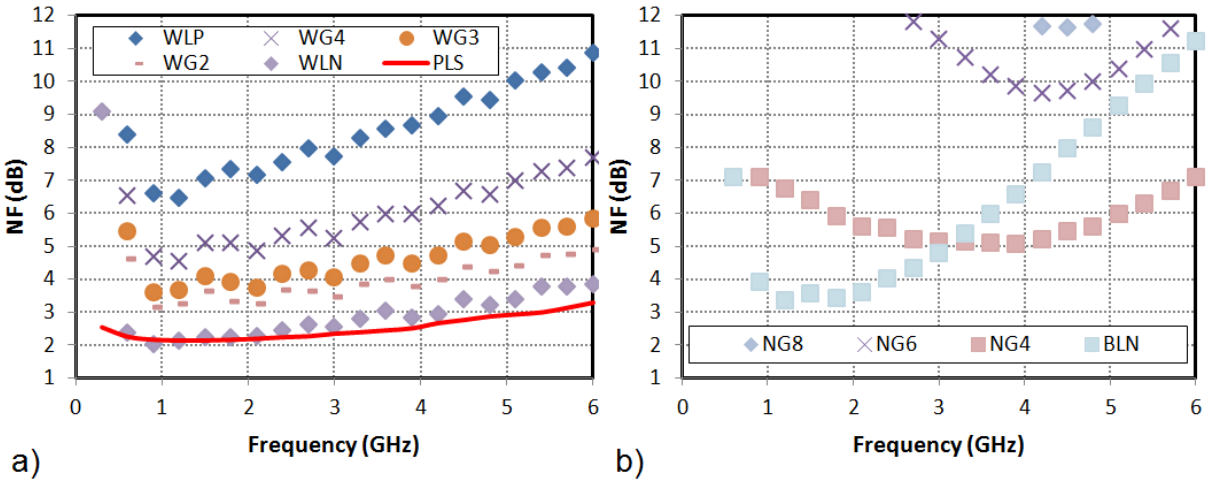


Figure 4.17 – NF control. a) Measured NF in wideband modes and low-noise mode (WLN) PLS result b) Measured NF in narrowband and bypass modes

The NF is measured according to the setup presented in Figure 4.2.b). Figure 4.17 shows the measured NF for different modes of operation. In Figure 4.17.a) is the NF results in wideband modes, a control range of almost 5 dB is possible. This NF variation allows for a large power saving which corresponds to favorable conditions of the radio link – i.e. the Signal to Noise Ratio (SNR) of the signal collected at the antenna is large, the receiver does not need the maximum sensitivity. The simulated (continuous red line) and measured NF in WLN mode exhibit very close form, less than 0.5 dB difference over the entire bandwidth. The NF reported in Figure 4.17.b) corresponds to narrowband and bypass modes. Depending on the scenario, these modes can be used to save power or to prevent saturation of the mixer. In the presence of a strong received signal, and large SNR_{in}, the gain would be reduced and the NF is no longer constrained. The conditions of operation are possible in mode NG8, which reduce the gain to 2.8 dB and the NF is 11dB. In this mode of operation the power consumption of the LNA is dramatically reduced.

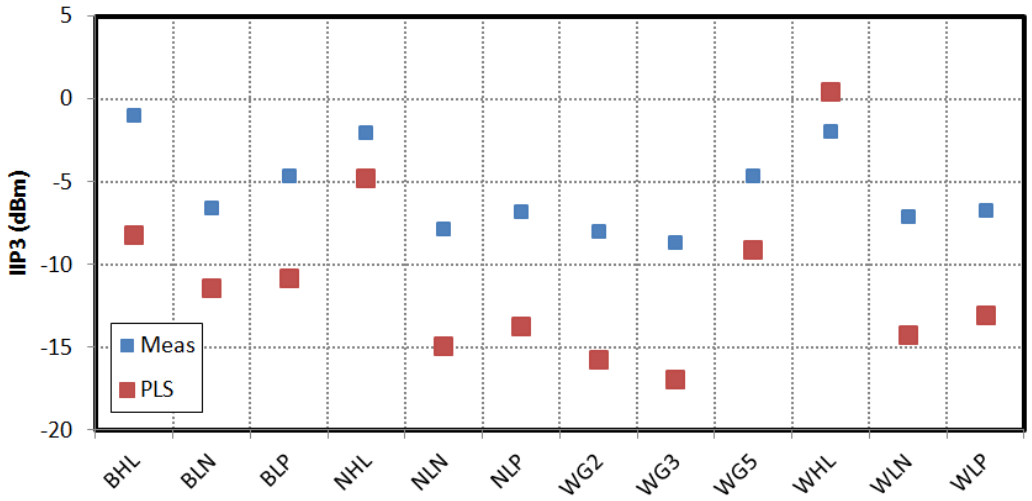


Figure 4.18 – Measured IIP3 vs PLS results in different operating modes

The IIP3 at 2.4 GHz is shown in Figure 4.18, it is measured according to the setup shown in Figure 4.2 (c) with a two-tone spacing of 20 MHz. The expected evolution of the linearity in the different mode is the same for measurement results. However, the value of measured IIP3 is 5 to 7dB above the PLS results. We suppose the linearity improvement by derivative superposition is not properly estimated with Periodic Steady State (PSS) analysis in SpectreRF. The IIP3 control range is close to 10 dB. This variation of linearity can be explored to achieve power saving when no specific blocker or jammer is present in the signal as instance.

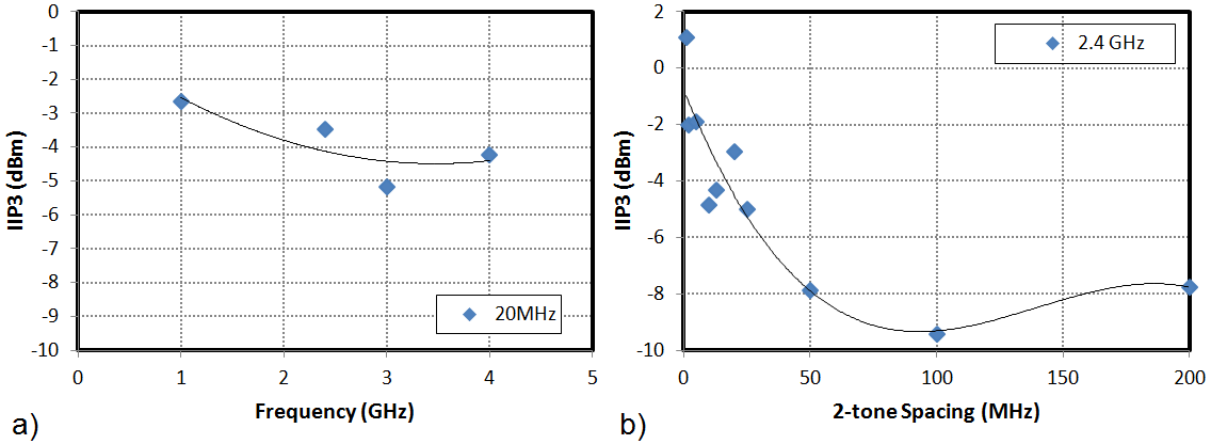


Figure 4.19 – Measured IIP3 a) IIP3 vs frequency variation at Δf = 20 MHz b) IIP_3 vs different tone spacings at f_0 = 2.4 GHz

Figure 4.19 (a) shows the measured IIP3 response as a function of frequency in WHL mode. Using a two-tone spacing of 20 MHz, the measurement is performed from 1 to 4 GHz due to the frequency limitation of the signal generator. The best performance are achieved at low frequency, below 3GHz, as illustrated by the tendency line, with only 3 dB variation over the evaluated frequency range.

Another important characteristic of wideband LNA dedicated to multi-standard operation, is the behavior of IIP3 for different interferer spacing (THI; NGA, 2012). A two-tone test with different frequency spacing (Δf) is applied. The resulting IIP3 performance, at 2.4GHz, is shown in Figure 4.19 (b). The IIP3 is fairly dependent on Δf, with more than 10 dB variation from 1 MHz to 200 MHz. Interestingly the linearity significantly increases for smaller Δf, indicating robustness against adjacent channel interference.

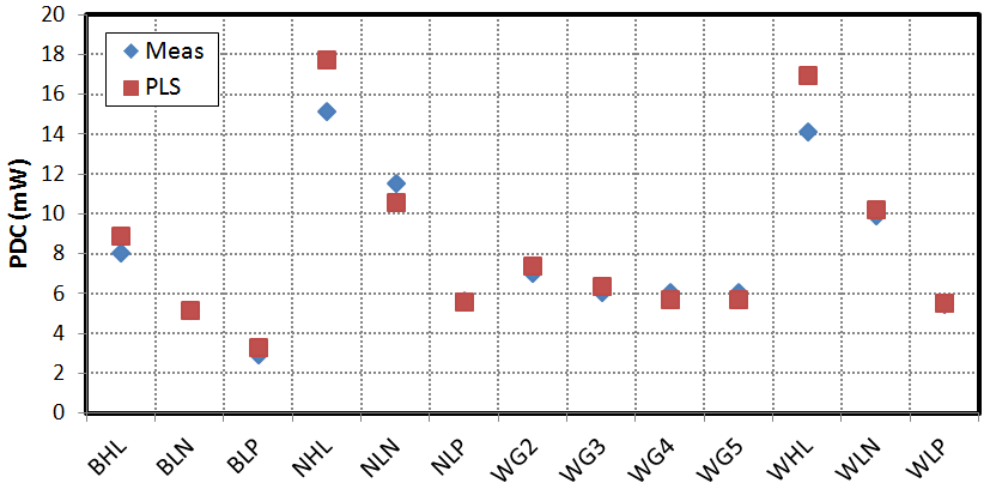


Figure 4.20 – Measured P_{DC} with different operating modes

Figure 4.20 shows the measured power consumption of the LNA in the different mode of operation. We observe a very good agreement between PLS and measured power consumptions. Only high linearity modes (WHL and NHL) exhibit a measured power 10% below the PLS results. In the peaking stage one transistor of the CS derivative superposition operates in weak inversion region. In this region of operation, the drain current is exponentially dependent to Vgs, which makes it sensitive to any process deviation. This sensitivity is strengthened by the small size of the device and the moderate matching of the current mirror controlling the biasing.

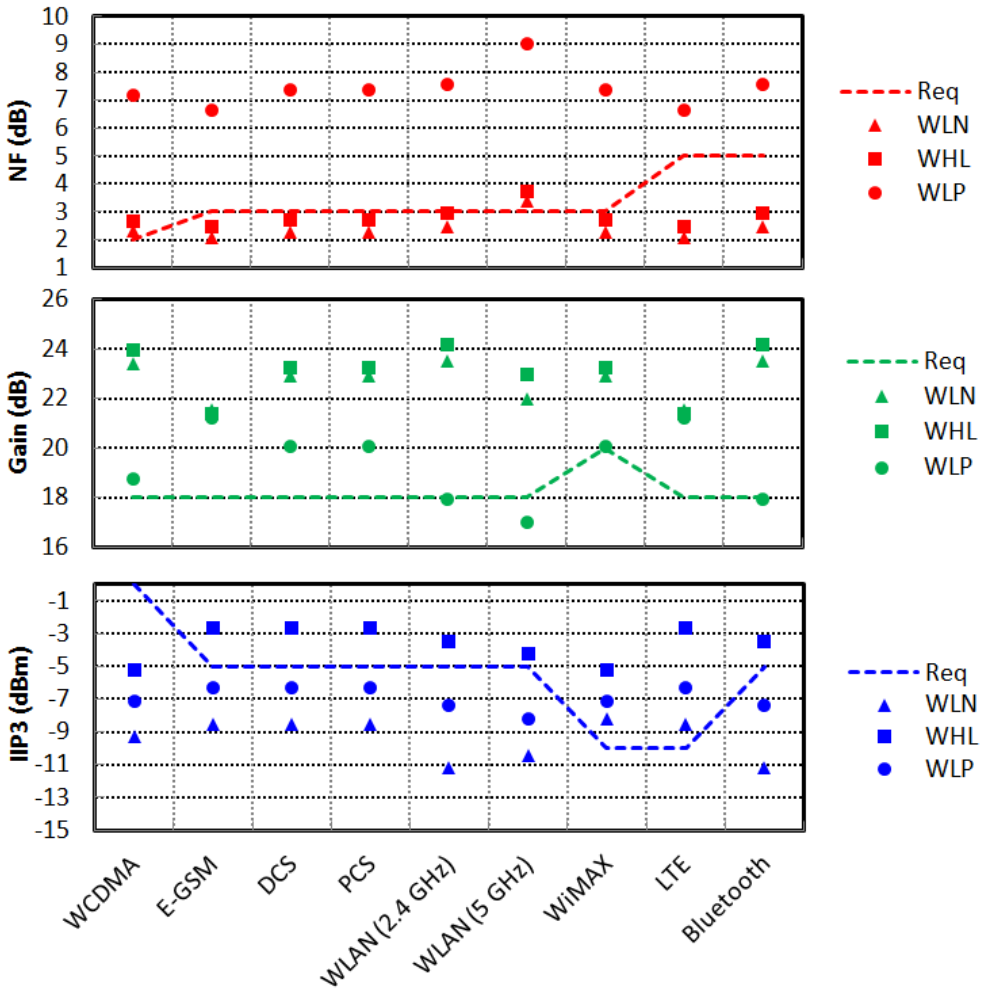


Figure 4.21 – Measured performance vs requirements

Figure 4.21 shows the NF, gain and IIP3 of the wideband modes together with the specifications of each standard according Table 1.2. For each performance metric and each standard, there is a mode that can fulfill the requirement, except for the IIP3 of WCDMA. However, the achieved IIP3 is high enough to allow its use in a system with a different IIP3 distribution, demanding a more linear mixer as instance.

Table 4.4 - Performance Comparison Of Multistandard LNAs

Ref		Tech (nm)	BW (GHz)	NF (dB)	Gain (dB)	IIP3 (dBm)	Supply (V)	P_{DC} (mW)	Area (mm^2)	FOM (dB)	FOM_{Area} (dB)
(BORREMANS et al., 2008)	JSSC	90	0-6.5	2.7	16.5	-2	1.2	9.7	0.002	10.3	65.7
(CHANG; HSU, 2010)	MTT	130	3.1-10	2.7	12.4	-3.8	1.8	14.4	0.031	-0.3	29.9
(CHEN; LIU, 2012)	TCAS	65	0.1-10	2.7	10.5	-3.5	1	13.7	0.020	2.0	35.9
(IM; LEE, 2016)	MTT	180	0.05-3.0	3.4	10.1	7.1	1.5	18.5	0.120	7.0	25.4
(LEE et al., 2012)	MWCL	90	0.2-2.6	1.9	24	-3	1	9	0.046	12.4	39.1
(PARK et al., 2010)	MTT	180	2.0-5.0	2.5	23	-7	1.8	18	0.880	-4.4	-3.3
(PARVIZI et al., 2016a)	MTT	130	0.1-2.2	4.9	12.3	-9.5	1	0.4	0.005	1.3	47.0
(PARVIZI et al., 2016b)	JSSC	130	0.6-4.2	4	14	-10	0.5	0.25	0.390	13.6	21.8
(PERUMANA et al., 2008)	TMTT	90	0.5-7	2.3	22	-11	1.2	12	0.012	-2.2	36.2
(ZHAN; TAYLOR, 2006)	ISSCC	90	0.5-8.2	1.9	25	-4	2.7	42	0.025	7.5	39.5
CHIP2, WHL		**130**	**0.1-6.0**	**2.5**	**24.3**	**1.1**	**1.4**	**14.1**	**0.102**	**21.1**	**40.9**
CHIP2, WLN		**130**	**0.1-6.0**	**2.1**	**23.6**	**-8.2**	**1.4**	**9.9**	**0.102**	**6.9**	**26.7**
CHIP2, WLP		**130**	**0.1-2.4**	**6.6**	**21.5**	**-6.2**	**1.4**	**5.5**	**0.102**	**-9.5**	**10.3**

The performance of this LNA is summarized in Table 4.4, and is compared to previously published works. The proposed circuit achieves state-of-the-art performance in terms gain, linearity, noise figure and power consumption. To the best of the authors' knowledge, this LNA, which addresses most of the wireless standards in the 0.4 GHz to 6 GHz range, exhibits the highest FOM reported so far in literature in WHL mode. It also presents a competitive performance/area ratio. In low noise mode (WLN), it achieves comparable noise and power consumption to inductive degeneration configurations. This LNA achieves broadband performance, and features a tuning control of the gain, the IIP3 and the NF. CHIP2 is capable of digital reconfiguration of performance to achieve power saving according radio link conditions.

4.4 SUMMARY

This chapter presented the measurement results of two wideband LNA implemented in 130nm CMOS technologies. In Section 4.2, the inductorless gyrator-like LNA is discussed. A very high linearity, a large gain and a low noise are performed at low power consumption. The active area is minimalist, which makes it suited for new deep submicron technologies. The circuit allows for IIP3 and NF configuration, offering a significant power saving. In Section 4.3, a two-stage version

with digitally reconfiguration is presented. With a broader response, this circuit significantly extends the connectivity ability of the proposed LNA. The digital control of the gain, the NF and the IIP3 gives a lot of flexible for the tuning. More than 96 effective configurations are possible. The extended bandwidth is achieved at the expense of an increased power consumption and a larger silicon area due to a low-Q inductor in the peaking stage. These two LNAs are among the best circuits reported so far in the literature.

5 CONCLUSION AND PERSPECTIVES

5.1 CONCLUSIONS

In this work, the top-down design of a wideband digitally reconfigurable LNA (Low Noise Amplifier) is presented. The proposed topology, suited to highly integrated multi-standard radio receivers, takes advantage of a current-reuse technique to achieve both high gain and low power consumption. The use of an inductorless first stage and a low-Q inductor enables low power consumption and high level of integration. This first stage, Gyrator-like, architecture uses an active feedback loop to achieve a wideband input matching from 0.4 to 6 GHz, with an active die area of only 0.007 mm^2. The cancellation of second-order harmonics in the current-reuse stage, along with the possible parameterization of the third-order response of the feedback path makes the Gyrator-like stage highly linear. Starting from the wireless standard requirements, system-level considerations are presented and block-level solutions are discussed and designed for GF 130 nm complementary metal-oxide-semiconductor (CMOS) process. The use of fully reconfigurable LNAs in the implementation of adaptive receivers is a new and promising topic. The circuits presented, fabricated and measured in this thesis not only have unique features, but also achieve power consumption as low as 1.5 mW. Being fully reconfigurable, the LNA reaches performance comparable to the best LNAs for wireless applications found in literature with noise figure of 2 dB, gain of 19 dB, and IIP3 of +14.4 dBm. The proposed LNA is capable of addressing 9 different communication standards: WCDMA, E-GSM, DCS, PCS, WLAN (lower bands), Bluetooth and LTE, WiMAX, HyperLAN/WLAN (higher bands). The architecture is implemented mainly using inverter-like transconductors, which are amenable to CMOS implementation in advanced CMOS processes.

5.2 SUMMARY OF CONTRIBUTIONS

The main contributions of this thesis are summarized as follows:

• A novel high-linearity, low-noise, low-power, low-area inductorless wideband LNA topology. Implemented in 130 nm CMOS, the measurement results

show state-of-the art performance with maximum power consumption of 7 mW. The LNA allows NF and IIP3 reconfiguration through biasing control. Due to its low-area characteristics it is suited for recent and future deep submicron CMOS technologies.

• A top-down simulation-assisted design method for wideband LNAs. Focusing on balancing the different performance axis, while meeting designer's requirements, it results in high performance low power LNAs.

• A digitally reconfigurable LNA for radio adaptive applications. With a large range of tuning of bandwidth, gain, NF, IIP3, it can be configured by the DSP on-the-fly, according to link conditions and the standard being demodulated. This approach opens up to a new generation of general purpose LNA allowing not only power saving but radio flexibility.

5.3 PERSPECTIVES FOR FUTURE WORK

The use of the proposed architectures in low power receivers is innovative. It shows promising performance for Adaptive or Software Defined Radio applications. Since this work focused on a proof-of-concept, it opens several possibilities for future work as listed below.

- A study of concurrent standard demodulation using the implemented high linearity Gyrator-like LNA in a receiver.
- Implementing an inductorless receiver with the Gyrator-like LNA.
- Implement the Gyrator-like LNA in a more advanced CMOS node.
- Adapt the Gyrator-like topology including the N-path filter solution to enable reconfigurable frequency selection, blocker filtering, focusing on a SAW-less receiver (ongoing work of Gabrielle Guiton at IMS Lab).
- Develop built-in self-tests (BISTs) to compensate and calibrate the reconfigurable LNAs for PVT variations. The reconfiguration of a LNA can improve the production yield and the robustness as performance adjustments are enabled after fabrication. Some variations inherent to fabrication process, including supply voltages and temperature can be compensated. The built-in self test (BIST) is then required and need to

be accurate enough to ensure, with a sufficiently high probability, that the internally-measured performance can be brought to within the targeted range for it (ELAHI; MUHAMMAD; BALSARA, 2006). A design of a BIST is being carried out as a Masters subject at GICS/UFPR under supervision of Prof. André Mariano and this author.

- Develop a link condition detection solution and a control algorithm that allows the implementation of a self-reconfigurable receiver.
- Implement an adaptive receiver using the digitally controlled LNA.
- Automate the simulation-assisted design method.

5.4 SCIENTIFIC PRODUCTIONS

International Journals

DE SOUZA, M. ,MARIANO, A. TARIS, T. Reconfigurable Inductorless Wideband CMOS LNA for Wireless Communications. **IEEE Transactions on Circuits and Systems I: Regular Papers**, DOI: 10.1109/TCSI.2016.2618361, 2016.

International Conferences

DE SOUZA, M.; MARIANO, A. A.; TARIS, T. Inductorless low power wideband LNA in 130 nm CMOS. **Conference Proceedings - 13th IEEE International NEW Circuits and Systems Conference, NEWCAS 2015**. Grenoble: 2015

LOLIS, L; DE SOUZA, M.; ZAMBON, L.B; MARIANO, A.A. Impact of a fully reconfigurable LNA on an RF front-end: A system level analysis. **2014 21st IEEE International Conference on Electronics, Circuits and Systems, ICECS 2014**, p. 662–665, 2015.

BIBLIOGRAPHY

3GPP. **LTE**. Available at: <http://www.3gpp.org/technologies/keywords-acronyms/98-lte>.

APARIN, V.; BROWN, G.; LARSON, L. E. Linearization of CMOS LNA's via optimum gate biasing. **2004 IEEE International Symposium on Circuits and Systems** (IEEE Cat. No.04CH37512). Anais...IEEE, 2004Available at: <http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1329112>. Accessed in: 21 abr. 2014

APARIN, V.; LARSON, L. E. Modified derivative superposition method for linearizing FET low-noise amplifiers. **IEEE Transactions on Microwave Theory and Techniques**, v. 53, n. 2, p. 571–581, fev. 2005.

ATALLAH, J. G. et al. A Direct Conversion WiMAX RF Receiver Front-End in CMOS Technology, **International Symposium on Signals, Circuits and Systems**, p. 1-4, 2007

BEHZAD, A. **Wireless LAN Radios: System Definition to Transistor Design**. Wiley – Interscience, 2008.

BELMAS, F.; HAMEAU, F.; FOURNIER, J. A Low Power Inductorless LNA With Double Gm Enhancement in 130 nm CMOS. **IEEE Journal of Solid-State Circuits**, v. 47, n. 5, p. 1094–1103, maio 2012.

BELOSTOTSKI, L.; MADANAYAKE, A.; BRUTON, L. T. Wideband LNA With an Active-C Element. **IEEE Microwave and Wireless Components Letters**, v. 22, n. 10, p. 524–526, out. 2012.

BORREMANS, J. et al. Low-Area Active-Feedback Low-Noise Amplifier Design in Scaled Digital CMOS. **IEEE Journal of Solid-State Circuits**, v. 43, n. 11, p. 2422–2433, nov. 2008.

BRANDOLINI, M. et al. Toward multistandard mobile terminals - fully integrated receivers requirements and architectures. **IEEE Transactions on Microwave Theory and Techniques**, v. 53, n. 3, p. 1026–1038, mar. 2005.

CHANG, P.; HSU, S. A Compact 0.1–14-GHz Ultra-Wideband Low-Noise Amplifier in 0.13-CMOS. **IEEE Transactions on Microwave Theory and Techniques**, v. 58, n. 10, p. 2575–2581, 2010.

CHEN, K.; LIU, S. Inductorless Wideband CMOS Low-Noise Amplifiers Using Noise-Canceling Technique. **IEEE Transactions on Circuits and Systems I: Regular Papers**, v. 59, n. 2, p. 305–314, fev. 2012.

CHEN, R.; HASHEMI, H. A 0.5-to-3 GHz Software-Defined Radio Receiver Using Discrete-Time RF Signal Processing. **IEEE Journal of Solid-State Circuits**, v. 49, n. 5, p. 1097–1111, maio 2014.

CHEN, W. **Designs of Broadband Highly Linear CMOS LNAs for Multiradio Multimode Applications**. Ph.D. thesis, UC Berkeley, 2009.

CHEN, W.-H. et al. A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation. **IEEE Journal of Solid-State Circuits**, v. 43, n. 5, p. 1164–1176, maio 2008.

CHIPWORKS INC. **Apple iPhone 6s Complementary Teardown Report**. [s.l: s.n.]. Available at: <http://www.chipworks.com/sites/default/files/Apple_iPhone_6s_A1688_Smartphone_Chipworks_Teardown_Report_BPT-1509-801_with_Commentary.pdf>.

CISCO. **Visual Networking Index: Global Mobile Data Traffic Forecast 2015–2020**. Available at: <http://www.cisco.com/c/en/us/solutions/collateral/service-provider/visual-networking-index-vni/mobile-white-paper-c11-520862.html>. Accessed in: 1 nov. 2016.

DE SOUZA, M.; MARIANO, A. A.; TARIS, T. Inductorless low power wideband LNA in 130 nm CMOS. **13th IEEE International NEW Circuits and Systems Conference, NEWCAS 2015**. Conference Proceedings Grenoble: 2015 Available at: <http://www.scopus.com/inward/record.url?eid=2-s2.0-84945162037&partnerID=40&md5=9933eb59c2538fb7a3d0bca95e74fb56>

DEVRIES, C. A.; MASON, R. D. Subsampling architecture for low power receivers. **IEEE Transactions on Circuits and Systems II: Express Briefs**, v. 55, n. 4, p. 304–308, 2008.

DOGAN, H.; MEYER, R. G.; NIKNEJAD, A. M. Analysis and Design of RF CMOS

Attenuators. **IEEE Journal of Solid-State Circuits**, v. 43, n. 10, p. 2269–2283, out. 2008.

ELAHI, I.; MUHAMMAD, K.; BALSARA, P. T. I/Q mismatch compensation using adaptive decorrelation in a low-IF receiver in 90-nm CMOS process. **IEEE Journal of Solid-State Circuits**, v. 41, n. 2, p. 395–403, 2006.

ELIEZER, O.; STASZEWSKI, R. B. Built-In Measurements in Low-Cost Digital-RF Transceivers. **IEICE Transactions on Electronics**, v. E94–C, n. 6, p. 930–937, 2011.

EL-NOZAHI, M. et al. An Inductor-Less Noise-Cancelling Broadband Low Noise Amplifier With Composite Transistor Pair in 90 nm CMOS Technology. **IEEE Journal of Solid-State Circuits**, v. 46, n. 5, p. 1111–1122, maio 2011.

EL-NOZAHI, M.; SANCHEZ-SINENCIO, E.; ENTESARI, K. A CMOS Low-Noise Amplifier With Reconfigurable Input Matching Network. **IEEE Transactions on Microwave Theory and Techniques**, v. 57, n. 5, p. 1054–1062, maio 2009.

ESDA; JEDEC. ANSI/ESDA/JEDEC JS-001 **Human Body Model Testing of Integrated Circuits**. Rome, NY: [s.n.]. Available at: <http://www.jedec.org/sites/default/files/JTR001-01-12 Final.pdf>.

FRANKS, L. E.; SANDBERG, I. W. An Alternative Approach to the Realization of Network Transfer Functions: The N-Path Filter. **Bell System Technical Journal**, v. 39, n. 5, p. 1321–1350, 1960.

FU, C. et al. A 2.4–5.4-GHz wide tuning-range CMOS reconfigurable low-noise amplifier. **IEEE Transactions on Microwave Theory and Techniques**, v. 56, n. 12, p. 2754–2763, 2008.

GEIS, A. et al. A 0.5 mm2 Power-Scalable 0.5-3.8-GHz CMOS DT-SDR Receiver With Second-Order RF Band-Pass Sampler. **IEEE Journal of Solid-State Circuits**, v. 45, n. 11, p. 2375–2387, nov. 2010.

GEORGANTAS, T. et al. 9.1 A 13mm 2 40nm Multiband GSM/EDGE/HSPA+/TDSCDMA/LTE Transceiver. **International Solid State Circuits Conference**, ISSCC Procedings 2015.

GIANNINI, V. et al. A 2-mm2 0.1-5 GHz Software-Defined Radio Receiver in 45-nm Digital CMOS. **IEEE Journal of Solid-State Circuits**, v. 44, n. 12, p. 3486–3498, dez. 2009.

GIRLANDO, G.; PALMISANO, G. Noise figure and impedance matching in RF cascode amplifiers. **IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing**, v. 46, n. 11, p. 1388–1396, 1999.

GRAY, P. R. et al. **Analysis and Design of Analog Integrated Circuits**. 5th. ed. New York: Wiley, 2009.

GSMA. **Understanding 5G**. Available at: <https://gsmaintelligence.com/research/?file=141208-5g.pdf&download>.

HAN, H. G.; JUNG, D. H.; KIM, T. W. A 2.88 mW +9.06 dBm IIP3 Common-Gate LNA With Dual Cross-Coupled Capacitive Feedback. **IEEE Transactions on Microwave Theory and Techniques**, v. 63, n. 3, p. 1019–1025, mar. 2015.

HEDAYATI, H. et al. A 1.8 dB NF Blocker-Filtering Noise-Canceling Wideband Receiver With Shared TIA in 40 nm CMOS. **IEEE Journal of Solid-State Circuits**, v. 50, n. 5, p. 1–17, 2015.

HSIEH, Y.-K. et al. A 60 GHz Broadband Low-Noise Amplifier With Variable-Gain Control in 65 nm CMOS. **IEEE Microwave and Wireless Components Letters**, v. 21, n. 11, p. 610–612, nov. 2011.

HU, J. et al. A Fully Integrated Variable-Gain Multi-tanh Low-Noise Amplifier for Tunable FM Radio Receiver Front-End. **IEEE Transactions on Circuits and Systems I: Regular Papers**, v. 55, n. 7, p. 1805–1814, 2008.

IM, D.; LEE, I. Y. A High IIP2 Broadband CMOS Low-Noise Amplifier With a Dual-Loop Feedback. **IEEE Transactions on Microwave Theory and Techniques**, v. 64, n. 7, p. 2068–2079, 2016.

INIEWSKI, K. **Wireless Technologies: Circuits, Systems, and Devices**. [s.l.] CRC Press, 2007.

ITRS. **ITRS 2007 - System Drivers**. Available at: <http://www.itrs2.net/itrs-

reports.html>. Accessed in: 12 out. 2016.

KIM, N.; APARIN, V.; LARSON, L. E. Analysis of IM3 Asymmetry in MOSFET Small-Signal Amplifiers. **IEEE Transactions on Circuits and Systems I: Regular Papers**, v. 58, n. 4, p. 668–676, abr. 2011.

KIM, T.; KIM, B. A 13-dB IIP3 improved low-power CMOS RF programmable gain amplifier using differential circuit transconductance linearization for various terrestrial mobile D-TV applications. **IEEE Journal of Solid-State Circuits**, v. 41, n. 4, p. 945–953, 2006.

LEE, H. C.; WANG, C. S.; WANG, C. K. A 0.2-2.6 GHz wideband noise-reduction Gm-boosted LNA. **IEEE Microwave and Wireless Components Letters**, v. 22, n. 5, p. 269–271, 2012.

LEE, T. **The design of CMOS radio-frequency integrated circuits**. 2 edition ed. Cambridge University Press, 2004.

LOLIS, L. et al. Impact of a fully reconfigurable LNA on an RF front-end: A system level analysis. **2014 21st IEEE International Conference on Electronics, Circuits and Systems**, ICECS 2014, p. 662–665, 2015.

MADAN, A. et al. Fully Integrated Switch-LNA Front-End IC Design in CMOS: A Systematic Approach for WLAN. **IEEE Journal of Solid-State Circuits**, v. 46, n. 11, p. 2613–2622, nov. 2011.

MAK, P. I.; MARTINS, R. Design of an ESD-protected ultra-wideband LNA in nanoscale CMOS for full-band mobile TV tuners. **IEEE Transactions on Circuits and Systems I: Regular Papers**, v. 56, n. 5, p. 933–942, 2009.

MITOLA, J. The software radio architecture. **IEEE Communications Magazine**, v. 33, n. 5, p. 26–38, maio 1995.

MOSIS, **MOSIS Educational Program (MEP)**. Available at: <https://www.mosis.com/ pages/products/mep/index>.

MOY, C.; PALICOT, J. Software radio: A catalyst for wireless innovation. **IEEE Communications Magazine**, v. 53, n. 9, p. 24–30, 2015.

PARK, J. et al. A direct-conversion CMOS RF receiver reconfigurable from 2 to 6 GHz. **IEEE Transactions on Microwave Theory and Techniques**, v. 58, n. 9, p. 2326–2333, 2010.

PARK, J. W.; RAZAVI, B. Channel Selection at RF Using Miller Bandpass Filters. **IEEE Journal of Solid-State Circuits**, v. 49, n. 12, p. 3063–3078, 2014.

PARVIZI, M.; ALLIDINA, K.; EL-GAMAL, M. N. An Ultra-Low-Power Wideband Inductorless CMOS LNA with Tunable Active Shunt-Feedback. **IEEE Transactions on Microwave Theory and Techniques**, v. 64, n. 6, p. 1843–1853, 2016a.

PARVIZI, M.; ALLIDINA, K.; EL-GAMAL, M. N. Short Channel Output Conductance Enhancement Through Forward Body Biasing to Realize a 0.5 V 250 ??W 0.6-4.2 GHz Current-Reuse CMOS LNA. **IEEE Journal of Solid-State Circuits**, v. 51, n. 3, p. 574–586, 2016b.

PEDRONI, V. A. **Digital electronics and design with VHDL**. [s.l.] Morgan Kaufmann, 2008.

PERUMANA, B. G. et al. Resistive-Feedback CMOS Low-Noise Amplifiers for Multiband Applications. **IEEE Transactions on Microwave Theory and Techniques**, v. 56, n. 5, p. 1218–1225, maio 2008.

PLETCHER, N.; RABAEY, J. M. Ultra-Low Power Wake-Up Receivers for Wireless Sensor Networks. **Electrical Engineering**, v. 22, n. April, p. 147, 2008.

RAMZAN, R.; ANDERSSON, S. A 1.4V 25mW Inductorless Wideband LNA in 0.13um CMOS. **International Solid-State Circuits Conference**, p. 7–9, 2007.

RAZAVI, B. **RF Microelectronics**. 2 nd ed. Prentice Hall, 2012.

SEN, S. et al. A Power-Scalable Channel-Adaptive Wireless Receiver Based on Built-In Orthogonally Tunable LNA. **IEEE Transactions on Circuits and Systems I: Regular Papers**, v. 59, n. 5, p. 946–957, maio 2012.

SHAEFFER, D. K.; LEE, T. H. A 1.5-V, 1.5-GHz CMOS low noise amplifier. **IEEE Journal of Solid-State Circuits**, v. 32, n. 5, p. 745–759, maio 1997.

SHEKHAR, S.; WALLING, J. S.; ALLSTOT, D. J. Bandwidth extension techniques for CMOS amplifiers. **IEEE Journal of Solid-State Circuits**, v. 41, n. 11, p. 2424–2438, 2006.

SOBHY, E. A. et al. A 2.8-mW Sub-2-dB Noise-Figure Inductorless Wideband CMOS LNA Employing Multiple Feedback. **IEEE Transactions on Microwave Theory and Techniques**, v. 59, n. 12, p. 3154–3161, dez. 2011.

SOWLATI, T. et al. Single-Chip Multiband WCDMA/HSDPA/HSUPA/EGPRS Transceiver with Diversity Receiver and 3G DigRF Interface Without SAW Filters in Transmitter / 3G Receiver Paths. **International Solid State Circuits Conference**, ISSCC procedings 2009.

TARIS, T.; BEGUERET, J.; DEVAL, Y. A low voltage current reuse LNA in a 130nm CMOS technology for UWB applications. Microwave Integrated Circuit Conference, **2007. EuMIC 2007. European. Procedings Munich**: IEEE, out. 2007Available at: <http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm? arnumber=4412710>

TECHINSIGHTS INC. **Circuit Analysis of the Qualcomm WTR3925**. Available at: <http://www2.techinsights.com/l/8892/2015-03-19/jrbnk>.

THI, T.; NGA, T. **Ultra low-power low-noise amplifier designs for 2.4 GHz ISM band applications**. Ph.D. thesis, Nanyang Singapore, 2012.

WAMBACQ, P. et al. High-frequency distortion analysis of analog integrated circuits. **IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing**, v. 46, n. 3, p. 335–345, mar. 1999.

WAMBACQ, P.; SANSEN, W. M. **Distortion Analysis of Analog Integrated Circuits**. Harlow, U.K.: Kluwer Academic Publishers, 1998.

WANG, H.; ZHANG, L.; YU, Z. A Wideband Inductorless LNA With Local Feedback and Noise Cancelling for Low-Power Low-Voltage Applications. **IEEE Transactions on Circuits and Systems I: Regular Papers**, v. 57, n. 8, p. 1993–2005, ago. 2010.

WANG, Y.; LU, L. 5.7 GHz low-power variable-gain LNA in 0.18 um CMOS. **Electronics Letters**, v. 41, n. 2, p. 11–12, 2005.

ZHAN, J.-H. C.; TAYLOR, S. S. A 5GHz resistive-feedback CMOS LNA for low-cost multi-standard applications. **IEEE International Solid State Circuits Conference**, Digest of Technical Papers, 2006.

ZHANG, F.; KINGET, P. Low-power programmable gain CMOS distributed LNA. **IEEE Journal of Solid-State Circuits**, v. 41, n. 6, p. 1333–1343, 2006.

ZHANG, H.; SANCHEZ-SINENCIO, E. Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial. **IEEE Transactions on Circuits and Systems I: Regular Papers**, v. 58, n. 1, p. 22–36, jan. 2011.

ZHU, J.; KRISHNASWAMY, H.; KINGET, P. R. Field-Programmable LNAs With Interferer-Reflecting Loop for Input Linearity Enhancement. **IEEE Journal of Solid-State Circuits**, v. 50, n. 2, p. 556–572, fev. 2015.

APPENDIX A - RF Block Definitions and Characteristics

From the study of receiver architectures, it can be noted that all of them are based upon the same building blocks: low noise amplifiers, mixers, frequency synthesizers and filters. Here we will identify the role of each block and remember the general characteristics in terms of gain, impedance match, noise and linearity.

A.1 BLOCK DEFINITIONS

A.1.1 Low Noise Amplifier

The RF signal is strongly attenuated through the path from the transmitter to the receiver, due to fading, scattering and reflections, Figure A.1. The signal power decays along the path (*R*) according to:

$$L_{path}(R) = 10\log\left[\left(\frac{4\pi}{\lambda}\right)^2 R^n\right] + L_{atten} \quad \text{(A.1)}$$

Where, λ is the wavelength of the carrier, *n* is the scattering exponent and L_{atten} is the scattering attenuation parameter. In free space, n and L_{atten} are 2 and 0 dB, respectively, reaching 4 and 10 dB in indoor applications (TARIS et al., 2010).

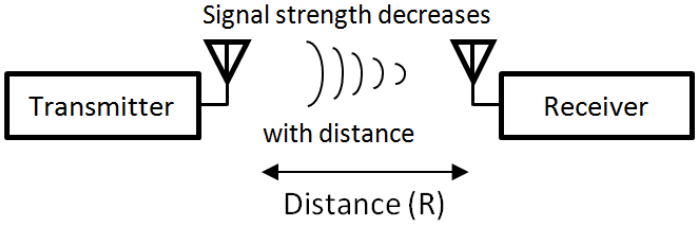


Figure A.1 – Signal is strongly attenuated over the air

At the maximum distance allowed by the standard, the transmitter will transmit at the maximum available power and the receiver will receive the minimum amount of power. The minimum signal level that a receiver can detect with acceptable quality is called the sensitivity of the receiver. The acceptable quality of detection is defined as the SNR at the output of the receiver that reach the maximum allowable error rate, the bit error rate (BER). These very weak signals can have power levels in the range of -120 dBm (0.8 fW for a WCDMA receiver) and need first to be amplified and then be processed by the blocks after the antenna.

The receiver must be able to distinguish these weak signals from the noise floor, to do that it shall minimize the Signal-to-Noise Ratio degradation. Once all the active devices add noise to the signal during processing, the further the signal travels through the receiver, the noisier it gets, and the noise from one stage is amplified by the next. This makes the detection more difficult as the signal goes through the chain. The noise figure ($NF = \frac{SNR_{in}}{SNR_{out}}$) is used to measure the SNR degradation, being at most 1 for a noiseless circuit and greater than one for noisy circuits.

To prevent SNR degradation, the first active stage is key. As Friis equation (A.11) states, its NF adds directly to the total NF of the receiver, while the following stages have their NF divided by the total gain before them. Therefore, the first stage gain is responsible to reduce the influence of the noise of the other stages. Providing enough amplification the input signal and adding the minimal amount of noise, its goal is to reach NF as close as possible to 1 (0 dB) and the highest gain possible. This first active stage is generally referred as Low Noise Amplifier – LNA.

Another important aspect of an LNA is that it shall present a given input impedance to the preceding blocks. This is required because external passive components that connect to the LNA (filters, antennas, transmission lines, etc) are designed for a certain characteristic impedance. If the input impedance deviates from the required value, the external components may not behave as intended. As most communications systems are designed for 50Ω characteristic impedance, the LNA shall provide an input impedance with real part close to 50Ω and imaginary part as close to 0Ω over the band of interest (BEHZAD, 2007).

These are the main aspects that make the LNA an unavoidable and critical RF block.

A.1.2 Mixer

The mixer is the component responsible for frequency translation of a signal without corruption of the information it carries. It is a 3 port device that performs the multiplication of the input signal by the local oscillator resulting in the output signal. There are two operation modes possible, up-converter and down-converter. The first is used in transmitters and corresponds to the shifting the signal frequency from

baseband f_{BB} to radio frequencies f_{RF}. The second is used in the receiver and converts the f_{RF} back to f_{BB}.

A.1.3 Frequency synthesizer

The frequency synthesizer block is responsible for supplying a stable signal in both frequency and amplitude. The frequency can be varied or not according to each standard requirement. Generally, it is generated with the help of an external reference, like quartz crystal.

A.1.4 Filters

The filters used in the RF reception chain have multiple functions. They are employed to select the band of interest, usually by means of a surface acoustic wave (SAW) or bulk acoustic wave (BAW) filter, mechanical filters with high selectivity. Even though this is commercially the norm, many studies of SAW-less receivers were made in the recent years, following the external component elimination trend. Among the methods proposed, the use of N-path filters is of interest, showing great potential with the scaled CMOS switching capabilities.

The filters are also used to reject the image frequency signal and to prevent aliasing in the digital conversion.

A.2 PERFORMANCE CHARACTERISTICS

A.2.1 Scattering parameters

The voltage or current measurement at high frequencies is somewhat difficult, whereas that of average power is more straightforward. For this reason, microwave theory models devices and circuits by means of parameters that can be obtained through the measurement of power quantities. They are called scattering parameters or S-Parameters.

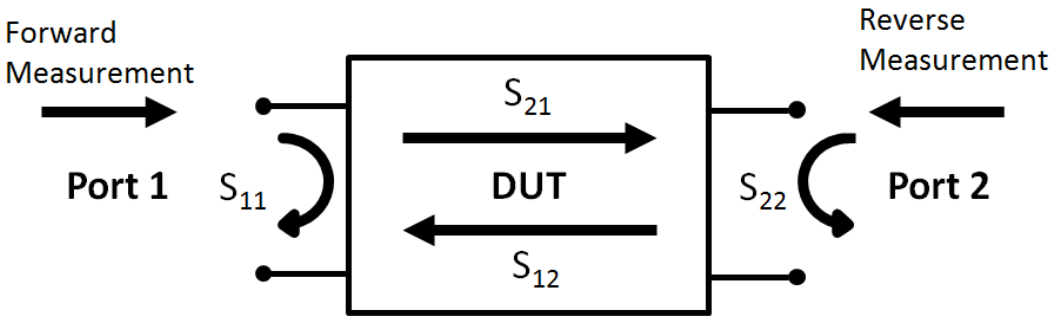


Figure A.2 – S-Parameters of a two-port network

In Figure A.2 a two-port network is shown with corresponding S-parameters indicated. S_{NM} refers to the amount of power leaving port N as a function of the power arriving at port M. S_{21} represents the amount of power transmitted to Port 2 with respect to the power received in Port 1 and is called forward transmission coefficient. S_{12} measures the reverse transmission coefficient. S_{11} and S_{22} measure the reflection coefficient of Ports 1 and 2 respectively.

A.2.2 Impedance match

The antenna and the filters after it are designed for a given impedance and may not work if not terminated properly. To help demodulate the signal, the LNA shall first completely absorb the signal power, avoiding reflections, uncharacterized loss and voltage attenuation. Let us define the conditions for a maximum power transfer, from source to load, from Figure A.3.

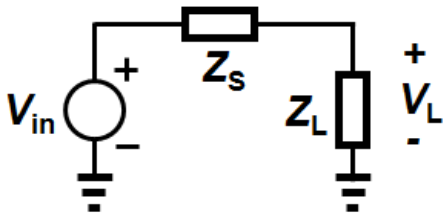


Figure A.3 – Power transfer and impedance match

The power absorbed by the load is given by:

$$P_{\mathrm{L}} = V_L I^* \tag{A.2}$$

Where I^* is the complex conjugate of I.

The maximum power transfer is obtained by deriving (A.27), where the impedance condition for this is:

$$Z_{\mathrm{S}} = Z_L^* \tag{A.3}$$

This condition is called impedance match. To achieve this, the LNA shall present at its input, an impedance that is the complex conjugate of the antenna or filter preceding it. The quality of the input match is expressed by the input return loss, defined as the reflected power divided by the incident power. For a source impedance R_S, the return loss is given by

$$\Gamma = \left|\frac{Z_{in} - R_S}{Z_{in} + R_S}\right|^2 \quad \text{(A.4)}$$

where Z_{in} denotes the input impedance. An input return loss of -10 dB means that 1/10 of the received power is reflected, a typical acceptable value. This quantity is usually measured the S-Parameter S_{11}.

A.2.3 Gain

The gain of a block is defined as a ratio of an output by an input quantity, being it a voltage or power. In RF is generally measured by the S-Parameter S_{21}. In a matched circuit, S_{21} equals to the voltage gain.

$$S_{21} = 20\ log\left(\frac{V_{out}}{V_{in}}\right), \text{ when } Z_{in} = Z_{source} = Z_{out} = Z_{load} \quad \text{(A.5)}$$

A.2.4 Noise

Noise is a random process that limits the minimum signal level that can be processed with acceptable quality.

Many are the sources and types of noise. Among them the most relevant for CMOS design are:

- **Thermal noise**: Produced by the random motion of electrons in a conductor. It introduces fluctuations in the voltage across the conductor even if the average current is zero. Its spectrum is proportional to the temperature and the resistance of the conductor. Can be found in any device with physical resistance, real resistors, inductors and MOSFETs are affected by thermal noise.
- **Flicker noise**: Produced at the interface between gate oxide and the silicon substrate in MOSFETs by dangling bonds that traps some charge carriers randomly. Its value is inversely proportional frequency and size. The lower the frequency or size, the higher the noise level.

A.2.4.1 Noise figure of a stage

At the circuit level, one of the most important characteristics of a receiver is its noise figure. There are several definitions for the noise figure, and it can be easily shown that these definitions are equivalent. The noise figure can be defined in terms of the signal-to-noise ratio (SNR) as

$$\mathrm{NF} = 10\log(F);\ \mathrm{F} = \frac{SNR_{in}}{SNR_{out}} \tag{A.6}$$

where, F is called the noise factor and the SNR is the ratio of the signal power over the noise power, shown in(A.7).

$$SNR = \frac{P_{signal}}{P_{noise}} \tag{A.7}$$

Since the SNR at the output can never be larger than the SNR at the input (real circuits can only add noise; they cannot take away noise), the minimum NF achievable is 0 dB (ratio of 1). In practice, this can never happen and NF is always a number greater than 0 dB.

The noise factor (F) can be also defined as the ratio of the total output noise power over the output noise power due to the input source. It can be developed from the two-port noise modeling (LEE, 2004), as shown in Figure A.4. Where $\overline{I_s^2}$ is the noise current source associated to the admittance of the source Y_S; $\overline{I_n^2}$ and $\overline{V_n^2}$ are, respectively, the equivalent noise current and voltage sources of the given stage.

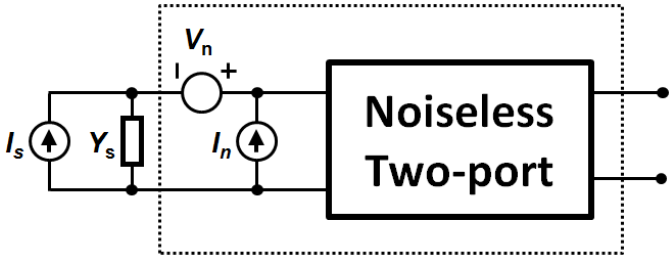


Figure A.4 – Two-port noise modeling
Source: Adapted from (LEE, 2004)

The noise factor is defined as:

$$F = 1 + \frac{|\overline{I_n + Y_S V_n}|^2}{\overline{I_s^2}} \tag{A.8}$$

If $\overline{V_n}$na $\overline{I_n}$ are correlated, $\overline{I_n}$ can be devided into two parts, one correlated with $\overline{V_n}$ and other not:

$$I_n = I_c + I_u \tag{A.9}$$

Where, $I_c = Y_c V_n$ and $Y_c = G_c + jB_n$ is the correlation admittance.

The noise factor can then be defined as:

$$F = 1 + \frac{\overline{I_u^2} + \overline{V_u^2}|Y_c + Y_S|^2}{\overline{I_S^2}} \quad \text{(A.10)}$$

This calculation method is very general and used in several research works in order to perform minimal noise figure sizing of the block (GOO et al., 2000; LEE, 2004).

A.2.4.2 Noise in a cascade

Since many stages appear in a receiver chain, it is desirable to determine the NF of the overall cascade in terms of each stage.

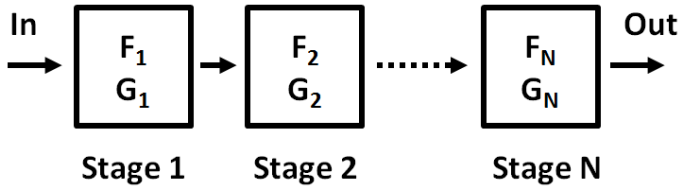


Figure A.5 – Noise factor of a cascade of N stages

The total noise factor of a system made of a chain of N stages, as shown in Figure A.5, is given by:

$$F_{tot} = 1 + (F_1 - 1) + \frac{(F_2 - 1)}{G_1} + \frac{(F_3 - 1)}{G_1 G_2} + \cdots + \frac{(F_N - 1)}{G_1 G_2 \ldots G_{N-1}} \quad \text{(A.11)}$$

Where G_i and F_i are respectively the gain and the noise factor of the stage i.

Frequently referred as the Friis equation (FRIIS, 1944), its result suggests that the noise contributed by each stage decreases as the total gain preceding that stage increases, implying that the first few stages in a cascade are the most critical. In fact, the gain and noise factor of the first stage dominates the global noise factor. Therefore, to lower the overall noise factor, the first active stage must be carefully designed. This shows the importance of the LNA, which is usually, the first active stage of a receiver chain. A design method is needed to study its noise, which depends mostly upon the sizing and biasing of the input transistor or transistors.

A.2.5 Linearity

Frequently electronic components and systems are treated as linear structures, but in fact, all real components cause some type of distortion the signals that pass through them. These nonlinearities contribute to the degradation of the signal transmission quality over the communication chain. Therefore, the transfer functions of real systems are not linear. Considering, for example, the following equation:

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots + \alpha_n x^n(t) \quad \text{(A.12)}$$

Where $y(t)$ is the output of the system, $x(t)$ is the input signal and α_n are the non-linearity coefficients of order n, as shown in Figure B.6.

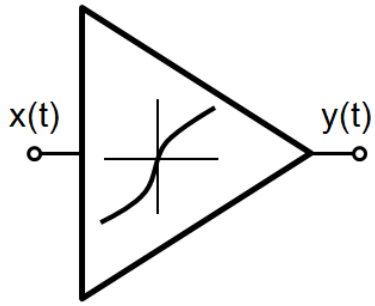


Figure B.6 – A non-linear system
Source: (RAZAVI, 2012)

Different types of non-linearity can be produced (LEE, 2004; RAZAVI, 2012):

- Compression gain, caused by the gain saturation.
- Harmonic distortion, generation of harmonics of the input signal
- Intermodulation: generation of undesirable signals that are a combination of input signals at different frequencies.
- Next, these different types of distortion will be detailed:

A.2.5.1 Gain compression

Applying a sinusoid $A\cos(\omega t)$ as the input signal $x(t)$to equation (A.12), and limiting to the third order, the output signal $y(t)$can be expressed as (RAZAVI, 2012):

$$y(t) = \alpha_1 A\cos(\omega t) + \alpha_2 A^2\cos^2(\omega t) + A^3\cos^3(\omega t) + \cdots \quad \text{(A.13)}$$

$$y(t) = \alpha_1 A\cos(\omega t) + \frac{\alpha_2 A^2}{2}[1 + \cos(2\omega t)] + \frac{\alpha_3 A^3}{4}[3\cos(\omega t) + \cos(3\omega t)] + \cdots \quad \text{(A.14)}$$

$$y(t) = \underbrace{\frac{\alpha_2 A^2}{2}}_{\text{DC}} + \underbrace{\left[\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right]\cos(\omega t)}_{\text{Fundamental}} + \underbrace{\frac{\alpha_2 A^2}{2}\cos(2\omega t) + \frac{\alpha_3 A^3}{4}\cos(3\omega t)}_{\text{Harmonics}} + \cdots \quad \text{(A.15)}$$

In a first order analysis, the system is studied with small signals, this way $\alpha_1 A$ is bigger than all the other harmonic factors and the gain of the system is linear and given by α_1. However, for large signals, the gain is not linear and depends on other coefficients. The term $\frac{3\alpha_3 A^3}{4}$ becomes important with respect to $\alpha_1 A$. In the circuits studied here, the third-order gain α_3 is negative and the term $\frac{3\alpha_3 A^3}{4}$ limits the linear amplification, adding a negative term to $\alpha_1 A$. Therefore, the fundamental gain can be expressed as:

$$G = \alpha_1 + \frac{3\alpha_3 A^2}{4} \quad \text{(A.16)}$$

To evaluate this effect the 1 dB compression point (P1dB or CP1) was defined. It corresponds to the input signal power from which the fundamental gain follows 1 dB with respect to its small signal value, as shown in Figure A.7.

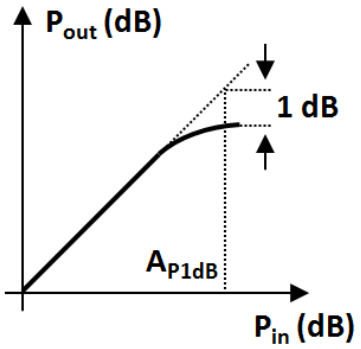


Figure A.7 – 1 dB compression point
Source: (RAZAVI, 2012)

Figure A.7 shows the extrapolated linear gain, when the circuit operates at low or medium power levels, given by $20\log(\alpha_1)$. It also shows the real output power with respect of the input power, given by $20\log\left(\alpha_1 + \frac{3\alpha_3 A^2}{4}\right)$. When the real output power differs 1 dB from the predicted by the linear case, the P1dB is defined. The input power level A_{P1dB} is the one that satisfies $20\log|\alpha_{P1dB}| - 1dB = 20\log\left|\alpha_1 + \frac{3\alpha_3 A_{P1dB}^2}{4}\right|$, which results in (A.17).

$$A_{P1dB} = \sqrt{0.145 \left|\frac{\alpha_1}{\alpha_3}\right|} \tag{A.17}$$

In the reception chain, the compression point is usually defined with respect to the input, denoted by ICP1. Meanwhile, in the transmission, the relevant measure is the output compression point, OCP1 (MABROUKI, 2010).

The P1dB gives the information about the ability of circuit to transmit power linearly in its operation frequency.

A.2.5.2 Harmonics

According to (A.15), if a sinusoid signal is applied to a non-linear system, at its output, is found a DC component, a component at the same frequency of the input signal or fundamental (responsible for gain compression) and components at integer multiples of the fundamental, also called harmonics. Except from the fundamental, all the other signals are considered distortions. In many RF circuits, harmonic distortion is unimportant because intermodulation poses as a much more severe restriction, as will be shown next.

A.2.5.3 Intermodulation

In RF systems harmonics of the carrier fall far away from the useful band of the signal. Since communication systems are usually multi-carriers, is more useful to study the intermodulation products because they yield components close to the carrier. This is done by means of the two-tone test, where two carriers in different frequencies (representing adjacent channels) of form $x(t) = A\cos\omega_1 t + B\cos\omega_2 t$ are applied at the input of a non-linear circuit, as shown in Figure B.6. The analytical expression of $y(t)$ shows different components that can be classified as (RAZAVI, 2012):

$$
\begin{aligned}
y(t) = \frac{1}{2}\alpha_2(A^2 + B^2)\Big\} &\quad \text{DC} \\
+ \alpha_1 A\cos(\omega_1 t) + \alpha_3\left(\frac{3}{4}A^3 + \frac{3}{2}AB^2\right)\cos(\omega_1 t)\Big\} &\quad \text{Fundamental } \omega_1 \\
+ \alpha_1 B\cos(\omega_2 t) + \alpha_3\left(\frac{3}{4}B^3 + \frac{3}{2}A^2 B\right)\cos(\omega_2 t)\Big\} &\quad \text{Fundamental } \omega_2 \\
+ \frac{1}{2}\alpha_2 A^2\cos(2\omega_2 t) + \frac{1}{2}\alpha_2 B^2\cos(2\omega_2 t)\Big\} &\quad \text{2nd order harmonics} \\
+ \frac{1}{4}\alpha_3 A^3\cos(3\omega_1 t) + \frac{1}{4}\alpha_3 B^3\cos(3\omega_2 t)\Big\} &\quad \text{3rd order harmonics} \\
+ \alpha_2 AB\cos\big((\omega_1 - \omega_2)t\big) + \alpha_2 AB\cos\big((\omega_1 + \omega_2)t\big)\Big\} &\quad \text{IM}_2 \text{ products} \\
+ \frac{3}{4}\alpha_3 A^2 B\cos\big((2\omega_1 - \omega_2)t\big) + \frac{3}{4}\alpha_3 AB^2\cos\big((2\omega_2 - \omega_1)t\big)\Big\} &\quad \text{IM}_3 \text{ products} \\
+ \frac{3}{4}\alpha_3 A^2 B\cos\big((2\omega_1 + \omega_2)t\big) + \frac{3}{4}\alpha_3 AB^2\cos\big((2\omega_2 + \omega_1)t\big)\Big\} &\quad \text{IM}_3 \text{ products} \\
+ \cdots &\quad \text{Higher order products}
\end{aligned}
\tag{A.18}
$$

The desired gain of the amplifier results from α_1. The α_2 term is responsible for the DC component, second-order harmonics (H_2) and second-order intermodulation products (IM_2). While α_3 is responsible for gain compression (as it is usually assumes as negative value), third-order harmonics (H_3) and third-order intermodulation products (IM_3).

The resulting spectrum of a two-tone test applied to a non-linear system is shown in Figure A.8.

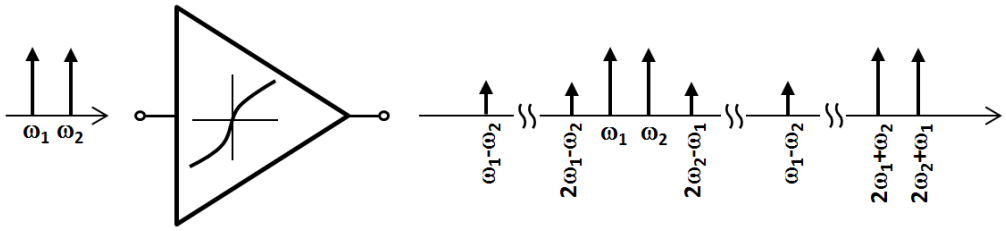


Figure A.8 – Two-tone test applied to a non-linear system

The effects of harmonic distortion are reduced if the harmonics would be out of the band of the system, since they would be suppressed by the filters of the receiver. However, this is not the case of the intermodulation products, especially if the input frequencies are close together.

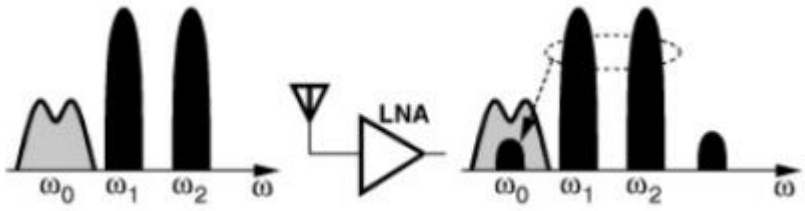


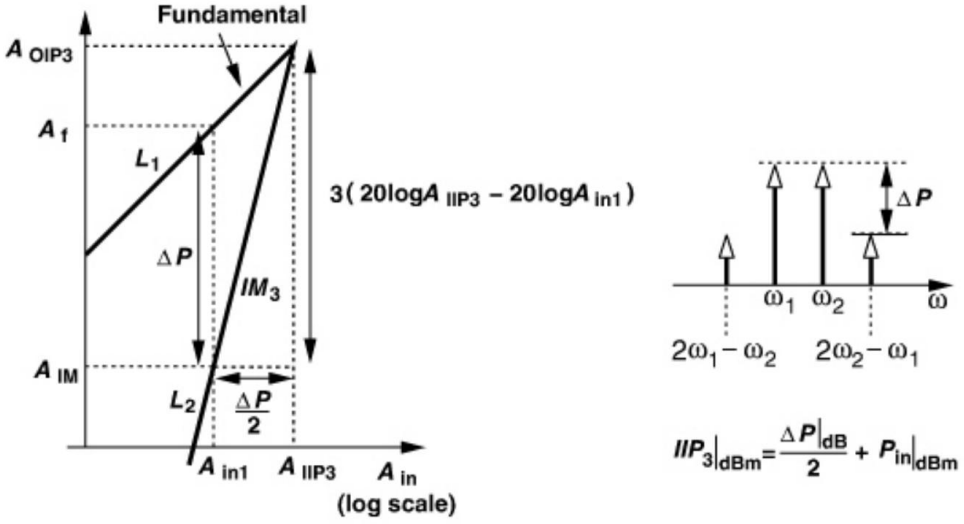
Figure A.9 – Signal corruption due to intermodulation
Source: (Razavi2011)

The third-order intermodulation products IM_3, situated at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, are close to the fundamentals and can corrupt the signal, Figure A.9. The intermodulation distortion IMD can be calculated from the intermodulation products that can be inside the bandwidth of the system, IM_2 and IM_3, that correspond respectively to $\omega_1 - \omega_2$and $2\omega_1 - \omega_2, 2\omega_2 - \omega_1$. IMD_2 is defined as the ratio of IM_2 over the fundamental and IMD_3 as the ratio of IM_3 over the fundamental. If the amplitude of the two tones are equal, A=B, then:

$$IMD_2 = \frac{\alpha_2}{\alpha_1}A \text{ or } IMD_2[dB] = IM_2[dBm] - P_{in}[dBm] + G[dB] \quad \text{(A.19)}$$

$$IMD_3 = \frac{3}{4}\frac{\alpha_3}{\alpha_1}A^2 \text{ or } IMD_3[dB] = IM_3[dBm] - P_{in}[dBm] + G[dB] \quad \text{(A.20)}$$

Comparing intermodulation distortion expressions IMD_2 (A.19) and IMD_3 (A.20) with harmonic distortion HD_2 and HD_3, we can find that $IMD_2 = 2HD_2$ and $IMD_3 = 3HD_3$. This confirms that linearity restrictions come especially from intermodulation distortion.



(a) (b)

Figure A.10 – Third-order Input Intercept Point – IIP_3
Source: (RAZAVI, 2012)

Figure A.10 shows a log-log plot of the fundamental and IM_3 as functions of the input signal power. The IM_3 grow at a triple of the rate of the fundamental. The point where the lines intercept each other is called third-order intercept point IP3, and the power level at the input at this point is the Input-IP3 or IIP3, the main linearity parameter of most receiver chains.

The IIP3 can be calculated as

$$\alpha_1 A_{IIP_2} = \alpha_2 A_{IIP_2}^2 \xrightarrow{yields} A_{IIP_2} = \frac{\alpha_1}{\alpha_2} \;\therefore\; IIP_2 = 20\log\left(A_{IIP_2}\right) \tag{A.21}$$

$$\alpha_1 A_{IIP_3} = \frac{3}{4}\alpha_3 A_{IIP_3}^2 \xrightarrow{yields} A_{IIP_3} = \sqrt{\frac{4}{3}\frac{\alpha_1}{\alpha_3}} \;\therefore\; IIP_3 = 20\log\left(A_{IIP_3}\right) \tag{A.22}$$

It can also be expressed as a function of the power of the applied carriers:

$$IMD_3 = \frac{3}{4}\frac{\alpha_3}{\alpha_1}A^2 \text{ and } IMD_2 = \frac{\alpha_2}{\alpha_1}A \tag{A.23}$$

$$IMD_3 = \frac{A_{in}^2}{A_{IIP_3}^2} \therefore A_{IIP_3} = \frac{A_{in}}{\sqrt{IMD_3}} \text{ and } IMD_2 = \frac{A_{in}}{A_{IIP_2}} \therefore A_{IIP_2} = \frac{A_{in}}{IMD_2} \tag{A.24}$$

$$IIP_3 = P_{in} - \frac{IMD_{3[dB]}}{2} \therefore IIP_3 = P_{in} - \frac{IM_3 - P_{in} - G}{2} \tag{A.25}$$

$$IIP_3 = P_{in} - IMD_{2[dB]} \therefore IIP_2 = P_{in} - IM_2 - P_{in} - G \tag{A.26}$$

In a wideband LNA the IIP_3 is an important measure, as no filtering is present. Not only an adjacent channel signal can corrupt the desired signal, but also signals at frequencies far from it. They can excite the third-order nonlinearities and generate IM3 products falling in the band of interest.

After defining the linearity characteristics of a system, it is important to relate them to the quality of its data transmission. Here we consider that intermodulation products IM_n produce disturbances in the signal similar to the noise sources present in the system. In the worst-case scenario their power levels are estimated to be below the noise floor of the system P_{noise}, which is defined by link budget:

$$P_{noise} = \underbrace{-174}_{\substack{\text{Noise floor}\\ \text{at 290K}}} + \underbrace{10\log(BW)}_{\text{Bandwidth}} = \underbrace{S}_{\text{Sensitivity}} - NF - SNR_{\min} \tag{A.27}$$

Where S is the sensitivity of the system, BW is the bandwidth, NF is the noise figure, and SNR_{min} is the minimal signal-to-noise ratio imposed by the bit error

rate (BER). Plugging (A.27) into (A.25) the expression (A.28) is obtained. It links the linearity characteristics of a system, the IIP_3, with the minimal acceptable quality of the data transmission of the system, the SNR_{min}, which is directed related to the BER.

$$IIP_3 = P_{\text{in}} + \frac{P_{\text{in}} + NF + SNR_{\text{min}} - S + G}{2} \therefore IIP_3 = P_{\text{in}} + \frac{P_{\text{in}} + SNR_{\text{min}} - S}{2} \quad \text{(A.28)}$$

APÊNDICE B - Gyrator-like LNA Analysis

B.1 Y-PARAMETERS ANALYSIS

The LNA presented in Chapter 2.3 can be modeled as a gyrator, for this we use the feedback theory of a two-port (GRAY et al., 2009), shown in Figure B.1. We first calculate the feedback y-parameters, disconnecting it from the main amplifier.

$\boldsymbol{y_{11f}}$:

$$y_{11f} = \frac{i_1}{v_1}\Big|_{v_o=0} = \frac{-g_{m2}(0 - v_F)}{v_i}\Big|_{v_o=0} \tag{B.1}$$

$$g_{m2}(v_o - v_F) = \frac{v_F - v_i}{R_F} \therefore v_F = \frac{v_i}{(1 + g_{m2}R_F)} \tag{B.2}$$

$$y_{11f} = \frac{-g_{m2}\left(-\frac{v_1}{(1 + g_{m2}R_F)}\right)}{v_1} = \frac{g_{m2}}{(1 + g_{m2}R_F)} \tag{B.3}$$

$\boldsymbol{y_{12f}}$:

$$y_{12f} = \frac{i_1}{v_o}\Big|_{v_i=0} = \frac{-g_{m2}(v_o - v_F)}{v_o}\Big|_{v_i=0} \tag{B.4}$$

$$g_{m2}(v_o - v_F) = \frac{v_F - v_1}{R_F} \therefore v_F = \frac{g_{m2}R_F v_o}{(1 + g_{m2}R_F)} \tag{B.5}$$

$$y_{12f} = \frac{-g_{m2}\left(v_o - \frac{g_{m2}R_F v_o}{(1 + g_{m2}R_F)}\right)}{v_o} = \frac{-g_{m2}}{(1 + g_{m2}R_F)} \tag{B.6}$$

$\boldsymbol{y_{21f}}$:

$$y_{21f} = \frac{i_o}{v_i}\Big|_{v_o=0} = \frac{0}{v_i}\Big|_{v_o=0} = 0 \tag{B.7}$$

$\boldsymbol{y_{22f}}$:

$$y_{22f} = \frac{i_o}{v_o}\Big|_{v_i=0} = \frac{0}{v_o}\Big|_{v_i=0} = 0 \tag{B.8}$$

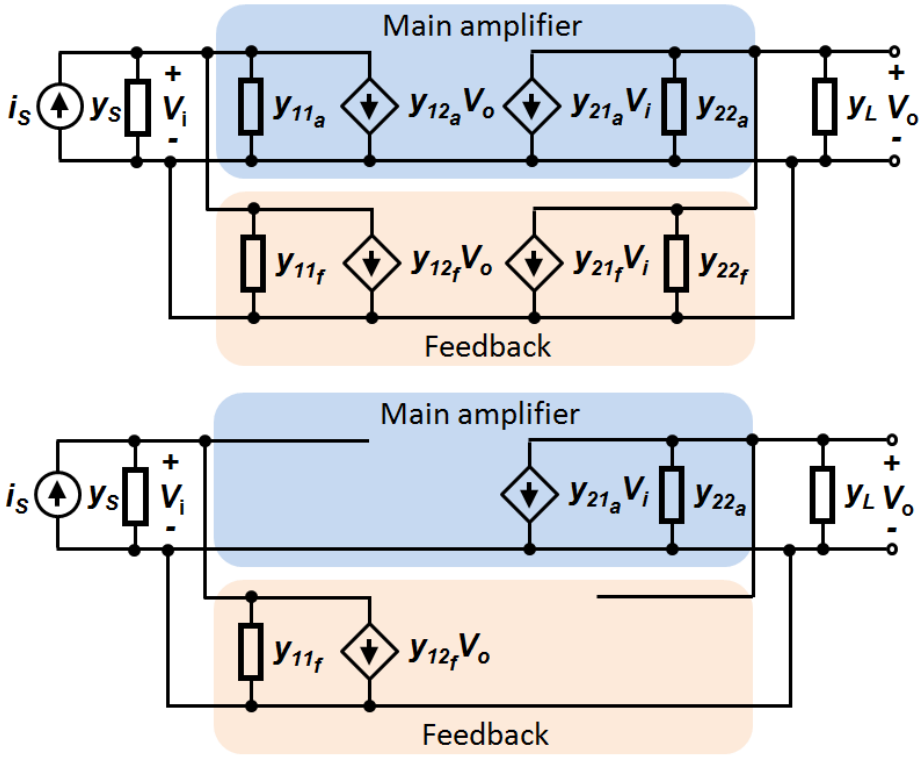


Figure B.1. a) y-parameter of a shunt-feedback amplifier b) simplified circuit when $y_{21_a} \gg y_{12_a}$ and $y_{12_f} \gg y_{21_f}$, $y_{11_a} \approx 0$ and $y_{22_f} \approx 0$, the case of the Gyrator-like LNA.

Then, the y-parameters of the main amplifier are calculated, also disconnecting it from the rest of the circuit.

$\boldsymbol{y_{11a}}$:

$$y_{11a} = \frac{i_i}{v_i}\bigg|_{v_o=0} = 0 \tag{B.9}$$

$\boldsymbol{y_{12a}}$:

$$y_{12a} = \frac{i_i}{v_o}\bigg|_{v_i=0} = 0 \tag{B.10}$$

$\boldsymbol{y_{21a}}$:

$$y_{21a} = \frac{i_o}{v_i}\bigg|_{v_o=0} = \frac{g_{m2}v_i}{v_i}\bigg|_{v_o=0} = G_{m1} \tag{B.11}$$

$\boldsymbol{y_{22a}}$:

$$y_{22a} = \frac{i_o}{v_o}\bigg|_{v_i=0} = \frac{G_{m1}0}{v_o}\bigg|_{v_i=0} = 0 \tag{B.12}$$

Table B.1. Gyrator-like LNA low frequency y-parameters

	y_{11}	y_{12}	y_{21}	y_{22}
Main amplifier	0	0	Gm_1	0
Feedback	$\frac{g_{m2}}{(1+g_{m2}R_F)}$	$\frac{-g_{m2}}{(1+g_{m2}R_F)}$	0	0

The low-frequency y-parameters shown in Table B.1 allow us to simplify the circuit as shown in Figure B.1.b).

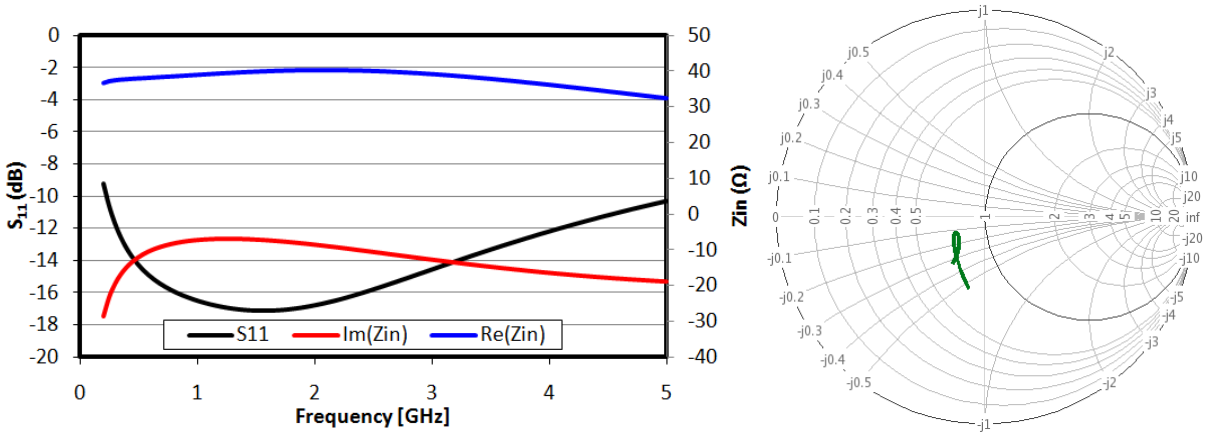


Figure B.2. Implemented Gyrator-like LNA simulated input impedance a) S_{11}, $Re(Z_{in})$ and $Im(Z_{in})$ b) Z_{in} Smith plot

The input impedance of the Gyrator-like LNA is given by:

$$Z_{in} = \frac{1}{Gm_1 Gm_2 Z_L} \tag{B.13}$$

Replacing $G_{m1} = y_{21a}$, $G_{m2} = -y_{12f}$ in (B.13), and considering the loading y_{11f}, we find the input impedance:

$$Z_{in} = \frac{1}{-y_{21a}y_{12f}Z_L} || y_{11f} \tag{B.14}$$

$$1/Z_{in} = \frac{g_{m2}G_{m1}Z_L}{(1+g_{m2}R_F)} + \frac{g_{m2}}{(1+g_{m2}R_F)} = \frac{g_{m2}(1+G_{m1}Z_L)}{(1+g_{m2}R_F)} \tag{B.15}$$

$$Z_{in} = \frac{1+g_{m2}R_F}{g_{m2}(1+G_{m1}Z_L)} \tag{B.16}$$

The input matching occurs when

$$g_{m2} = \frac{1}{R_S(1+G_{m1}Z_L) - R_F} \tag{B.17}$$

Figure B.2 shows the input impedance of the proposed LNA. The impedance matching is sustained from 200 MHz (due to the DC blocking capacitor) until 5 GHz.

B.2 NOISE FIGURE CALCULATION

In the proposed Gyrator-like LNA circuit the main noise contributions come from MOS devices, as well as from resistors R_B and R_F. The noise factor F of the LNA can therefore be written as:

$$F = \eta_{R_S} + \eta_{M_{1N}} + \eta_{M_{1P}} + \eta_{M_2} + \eta_{M_3} + \eta_{R_B} + \eta f_{R_F} \tag{B.18}$$

The value of the noise factor F can be calculated as the sum of the noise contributions of each noise source independently.

- M_{1N} contribution

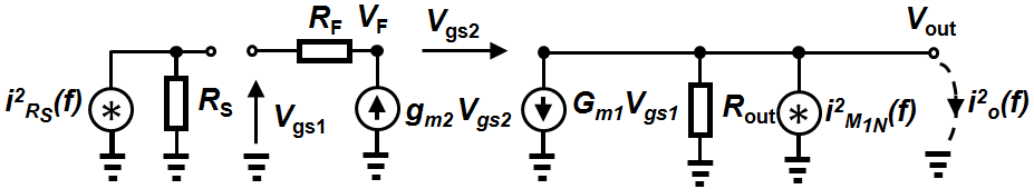


Figure B.3. Model for the calculation of the noise contribution of M_{1N}

The noise factor contribution of M_{1N} is given by the ratio of $i_o^2(f)|_{M_{1N}}$, the output short-circuit noise current due to M_{1N}, to $i_o^2(f)|_{R_S}$, the output short-circuit noise current due to the source R_S, expressed in (21).

$$\eta_{M_{1N}} = \frac{i_o^2(f)\,|_{M_{1N}}}{i_o^2(f)|_{R_S}} \tag{B.19}$$

where,

$$i_o^2(f)|_{R_s} = \left[R_S || \left(\frac{1}{g_{m2}} + R_F\right)\right]^2 . G_{m1}^2 . i_{R_s}^2(f) \tag{B.20}$$

$$i_{R_s}^2(f) = \frac{4k_B T \Delta f}{R_S} \tag{B.21}$$

$$i_o^2(f)|_{M_{1N}} = i_{M_{1N}}^2(f) = 4k_B T \Delta f \frac{\gamma_{1N} g_{m1N}}{\alpha_{1N}} \tag{B.22}$$

where is k_B the Boltzmann's constant, T is the absolute temperature, Δf is the noise bandwidth, γ is the thermal excess noise factor.

Substituting (4) in (3), and (3) and (5) in (2), considering the same Δf, gives

$$\eta_{M_1N} = \frac{\gamma_{1N} g_{m1N}}{\alpha_{1N}} . R_S . \frac{1}{G_{m1}^2} . \left[\frac{R_S + R_F + \frac{1}{g_{m2}}}{R_S\left(R_F + \frac{1}{g_{m2}}\right)}\right]^2 \tag{B.23}$$

Further manipulating and considering $\alpha_{1N} = 1$, results

$$\eta_{M_{1N}} = \frac{\gamma_{1N} g_{m1N}}{G_{m1}^2} . R_S . \left[\frac{1}{R_S} + \frac{g_{m2}}{1 + g_{m2} R_F}\right]^2 \quad \text{(B.24)}$$

Applying the matching condition $g_{m2} = \frac{1}{R_S(1+A_V)-R_F}$, yields:

$$\eta_{M_{1N}} = \frac{\gamma_{1N} g_{m1N}}{G_{m1}^2 R_S} \left[\frac{(2 + A_V)}{(1 + A_V)}\right]^2 \quad \text{(B.25)}$$

which for $A_V \gg 1$ gives

$$\eta_{M_{1N}} = \frac{\gamma_{1N} g_{m1N}}{G_{m1}^2 R_S} \quad \text{(B.26)}$$

- M_{1P} contribution

Once M_{1N} and M_{1P}can be modeled as being in parallel, the same calculation done to $F_{M_{1N}}$ applies to $F_{M_{1P}}$, i.e. substituting $\gamma_{1N}, g_{m1N}, \alpha_{1N}$ by $\gamma_{1P}, g_{m1P}, \alpha_{1P}$ into (B.18):

$$\eta_{M_{1P}} = \frac{\gamma_{1P} g_{m1P}}{\alpha_{1P} G_{m1}^2} . R_S . \left[\frac{1}{R_S} + \frac{g_{m2}}{1 + g_{m2} R_F}\right]^2 \quad \text{(B.27)}$$

The noise of M_{1N} directly adds to the noise factor, without reduction by R_F or A_V, which explains it being the most noisy component in the circuit and is validated by Friis equation.

- R_F contribution

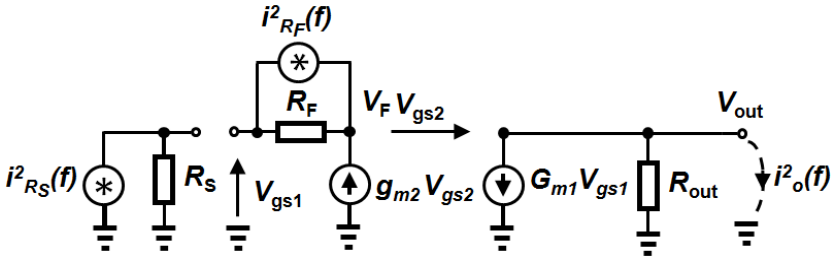


Figure B.4. Model for the calculation of the noise contribution of R_F

$$i_o^2(f)|_{R_F} = i_{R_F}^2(f) G_{m1}^2 . R_S^2 \left[\frac{R_F}{R_S + \frac{1}{g_{m2}} + R_F}\right]^2 \quad \text{(B.28)}$$

$$i_o^2(f)|_{R_s} = i_{R_s}^2(f) G_{m1}^2 \left[\frac{R_S(R_F + 1/g_{m2})}{R_S + R_F + 1/g_{m2}}\right]^2 \quad \text{(B.29)}$$

$$\eta_{R_F} = \frac{i_o^2(f)|_{R_F}}{i_o^2(f)|_{R_S}} = \frac{i_{R_F}^2(f)}{i_{R_s}^2(f)} \frac{G_{m1}^2 . R_S^2 \left[\frac{R_F}{R_S + \frac{1}{g_{m2}} + R_F}\right]^2}{G_{m1}^2 \left[\frac{R_S(R_F + 1/g_{m2})}{R_S + R_F + 1/g_{m2}}\right]^2} \tag{B.30}$$

$$\eta_{R_F} = \frac{i_{R_F}^2(f)}{i_{R_s}^2(f)} R_S^2 \left[\frac{R_F}{R_S + \frac{1}{g_{m2}} + R_F}\right]^2 \left[\frac{R_S + R_F + \frac{1}{g_{m2}}}{R_S\left(R_F + \frac{1}{g_{m2}}\right)}\right]^2 \tag{B.31}$$

$$\eta_{R_F} = \frac{\frac{1}{R_F}}{\frac{1}{R_S}} R_S^2 \left[\frac{R_F}{R_S + \frac{1}{g_{m2}} + R_F} . \frac{R_S + R_F + \frac{1}{g_{m2}}}{R_S\left(R_F + \frac{1}{g_{m2}}\right)}\right]^2 \tag{B.32}$$

$$\eta_{R_F} = \frac{R_S^3}{R_F} \left[\frac{R_F}{R_S\left(R_F + \frac{1}{g_{m2}}\right)}\right]^2 = \frac{R_S^3 R_F^2}{R_F R_S^2} \left[\frac{1}{\left(R_F + \frac{1}{g_{m2}}\right)}\right]^2 \tag{B.33}$$

$$\eta_{R_F} = R_S R_F \left[\frac{g_{m2}}{(1 + g_{m2} R_F)}\right]^2 \tag{B.34}$$

- M_2 contribution

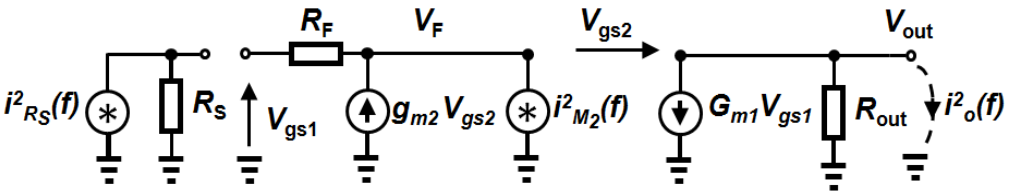


Figure B.5. Model for the calculation of the noise contribution of M_2

$$i_o^2(f)|_{M_2} = i_{M_2}^2(f) . G_{m1}^2 . R_S^2 \left[\frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m2}} + R_F + R_S}\right]^2 \tag{B.35}$$

$$i_o^2(f)|_{R_s} = i_{R_s}^2(f) . G_{m1}^2 . \left[\frac{R_S(R_F + 1/g_{m2})}{R_S + R_F + 1/g_{m2}}\right]^2 \tag{B.36}$$

$$\eta_{M_2} = \frac{i_o^2(f)|_{M_2}}{i_o^2(f)|_{R_S}} \tag{B.37}$$

$$\eta_{M_2} = \frac{i_{M_2}^2(f).G_{m1}^2.R_S^2\left[\frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m2}}+R_F+R_S}\right]^2}{i_{R_s}^2(f).G_{m1}^2.\left[\frac{R_S\left(R_F+\frac{1}{g_{m2}}\right)}{R_S+R_F+\frac{1}{g_{m2}}}\right]^2} \tag{B.38}$$

$$\eta_{M_2} = \frac{i_{M_2}^2(f)}{i_{R_s}^2(f)}.R_S^2\left[\frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m2}}+R_F+R_S}\right]^2\left[\frac{R_S+R_F+\frac{1}{g_{m2}}}{R_S\left(R_F+\frac{1}{g_{m2}}\right)}\right]^2 \tag{B.39}$$

$$\eta_{M_2} = \frac{\frac{\gamma_2 g_{m2}}{\alpha_2}}{\frac{1}{R_S}}.R_S^2\left[\frac{\frac{1}{g_{m2}}}{R_S\left(R_F+\frac{1}{g_{m2}}\right)}\right]^2 \tag{B.40}$$

$$\eta_{M_2} = \frac{\gamma_2 g_{m2}}{\alpha_2}.R_S^3\left[\frac{\frac{1}{g_{m2}}}{R_S\left(R_F+\frac{1}{g_{m2}}\right)}\right]^2 \tag{B.41}$$

$$\eta_{M_2} = \frac{\gamma_2 g_{m2}}{\alpha_2}.\frac{R_S^3}{R_S^2\, g_{m2}^2}\left[\frac{g_{m2}}{1+g_{m2}R_F}\right]^2 \tag{B.42}$$

$$\eta_{M_2} = \frac{\gamma_2 g_{m2}}{\alpha_2}.\frac{R_S}{(1+g_{m2}R_F)^2} \tag{B.43}$$

- M_3 contribution

The same calculation of M_2 applies to M_3, as they are in parallel, from the noise point of view, leading to:

$$\eta_{M_3} = \frac{\gamma_{bias} g_{m3}}{\alpha_{bias}}.\frac{R_S}{(1+g_{m2}R_F)^2} \tag{B.44}$$

- R_{OUT} contribution

The circuit is loaded by a capacitance C_L, R_{OUT} is the output resistance due to channel length modulation of the transistors M_{1N} and M_{1P}, from which the noise was already taken into account.

- R_B contribution

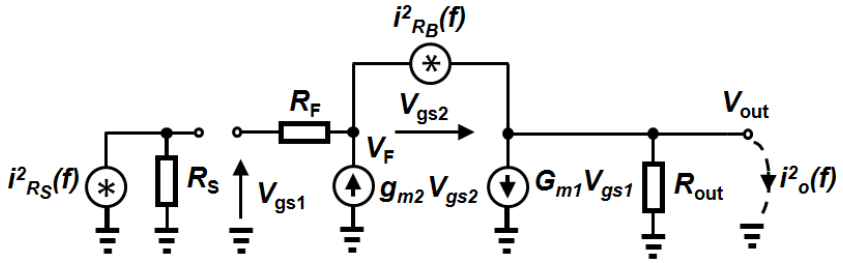


Figure B.6. Model for the calculation of the noise contribution of R_B

$$i_o^2(f)|_{R_B} = i_{R_B}^2(f).G_{m1}^2.R_S^2\left[\frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m2}}+R_F+R_S}\right]^2 \tag{B.45}$$

$$i_o^2(f)|_{R_s} = i_{R_s}^2(f).G_{m1}^2.\left[\frac{R_S(R_F+1/g_{m2})}{R_S+R_F+1/g_{m2}}\right]^2 \tag{B.46}$$

$$\eta_{R_B} = \frac{i_o^2(f)|_{R_B}}{i_o^2(f)|_{R_S}} \tag{B.47}$$

$$\eta_{R_B} = \frac{i_{R_B}^2(f).G_{m1}^2.R_S^2\left[\frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m2}}+R_F+R_S}\right]^2}{i_{R_s}^2(f).G_{m1}^2.\left[\frac{R_S\left(R_F+\frac{1}{g_{m2}}\right)}{R_S+R_F+\frac{1}{g_{m2}}}\right]^2} \tag{B.48}$$

$$\eta_{R_B} = \frac{i_{R_B}^2(f)}{i_{R_s}^2(f)}.R_S^2\left[\frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m2}}+R_F+R_S}\right]^2\left[\frac{R_S+R_F+\frac{1}{g_{m2}}}{R_S\left(R_F+\frac{1}{g_{m2}}\right)}\right]^2 \tag{B.49}$$

$$\eta_{R_B} = \frac{\frac{1}{R_B}}{\frac{1}{R_S}}.R_S^2\left[\frac{\frac{1}{g_{m2}}}{R_S\left(R_F+\frac{1}{g_{m2}}\right)}\right]^2 \tag{B.50}$$

$$\eta_{R_B} = \frac{1}{R_B}.R_S^3\left[\frac{\frac{1}{g_{m2}}}{R_S\left(R_F+\frac{1}{g_{m2}}\right)}\right]^2 \tag{B.51}$$

$$\eta_{R_B} = \frac{1}{R_B}.\frac{R_S^3}{R_S^2\,g_{m2}^2}\left[\frac{g_{m2}}{1+g_{m2}R_F}\right]^2 \tag{B.52}$$

$$\eta_{R_B} = \frac{1}{R_B}.\frac{R_S}{(1+g_{m2}R_F)^2} \tag{B.53}$$

Substituting (B.26), (B.27), (B.34), (B.43), (B.44) and (B.53) into (B.18), yields:

$$
\begin{aligned}
F = & 1 && \leftarrow \eta_{R_S} \\
& + \frac{\gamma_{1N} g_{m1N}}{\alpha_{1N} G_{m1}^2} . R_S . \left[\frac{1}{R_S} + \frac{g_{m2}}{1 + g_{m2} R_F} \right]^2 && \leftarrow \eta_{M_{1N}} \\
& + \frac{\gamma_{1P} g_{m1P}}{\alpha_{1P} G_{m1}^2} . R_S . \left[\frac{1}{R_S} + \frac{g_{m2}}{1 + g_{m2} R_F} \right]^2 && \leftarrow \eta_{M_{1P}} \\
& + R_S R_F \left[\frac{g_{m2}}{(1 + g_{m2} R_F)} \right]^2 && \leftarrow \eta_{R_F} \\
& + \frac{\gamma_2 g_{m2}}{\alpha_2} . \frac{R_S}{(1 + g_{m2} R_F)^2} && \leftarrow \eta_{M_2} \\
& + \frac{\gamma_3 g_{m3}}{\alpha_3} . \frac{R_S}{(1 + g_{m2} R_F)^2} && \leftarrow \eta_{M_3} \\
& + \frac{1}{R_B} . \frac{R_S}{(1 + g_{m2} R_F)^2} && \leftarrow \eta_{R_B}
\end{aligned}
\tag{B.54}
$$

where R_s is the signal source resistance, γ is the thermal noise excess factor, $\alpha = \frac{g_m}{g_{d0}}$ and g_{d0} is the output transconductance at $V_{ds} = 0$V (LEE, 2004).

When $A_V \gg 1$, it yields

$$
\begin{aligned}
F \approx 1 + \frac{\gamma_{1N} g_{m1N}}{G_{m1}^2 R_S} + \frac{\gamma_{1P} g_{m1P}}{G_{m1}^2 R_S} + \frac{R_F}{R_S A_V^2} + \frac{\gamma_2}{A_V} \left[1 - \frac{R_F}{R_S A_V} \right] + \gamma_3 g_{m3} R_S \left[1 - \frac{R_F}{R_S A_V} \right]^2 \\
+ \frac{R_S}{R_B} \left[1 - \frac{R_F}{R_S A_V} \right]^2
\end{aligned}
\tag{B.55}
$$

To reduce the noise factor whilst minimally affecting the LNA's performance, the expression (B.18) is further analyzed. To lower F_{RB}, R_B is made as large as possible. The noise current generated by the transistors M_2 and M_3, directly contributes to the total noise of the circuit. F_{M2} and F_{M3} in (B.18) can be reduced by adding an extra resistor R_F in series with the feedback path. However, increasing R_F reduces the gyrator effect, which degrades input matching. Therefore, the value of R_F is limited by the tuning of the input impedance. If some input mismatch is allowed, the noise contribution of the feedback can be reduced. The noise factor also benefits from the large transconductance (g_{m1P}, g_{m1N}) of the current-reuse amplifier. The size of MOS device M_1 also defines the bandwidth of the circuit, which is limited by parasitic capacitors. The determination of F_{M1P} and F_{M1N} in (B.18) depends on the gain and bandwidth specifications. Interestingly, the contribution of F_{M1p} and F_{M1n} decreases with technology scaling as the transit frequency, $f_T \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})}$ improves.

Table B.2. Thermal noise component contributions

Noise factor contribution	Comp	Noise Factor	Excuding Source
$F = 1$	R_S	1	-
$+\frac{\gamma_{1N} g_{m1N}}{\alpha_{1N} G_{m1}^2} . R_S . \left[\frac{1}{R_S} + \frac{g_{m2}}{1 + g_{m2} R_F}\right]^2$	M_{1N}	0.32	53.4%
$+\frac{\gamma_{1P} g_{m1P}}{\alpha_{1P} G_{m1}^2} . R_S . \left[\frac{1}{R_S} + \frac{g_{m2}}{1 + g_{m2} R_F}\right]^2$	M_{1P}	0.09	17.1%
$+R_S R_F \left[\frac{g_{m2}}{(1 + g_{m2} R_F)}\right]^2$	R_F	0.11	22.3%
$+\frac{\gamma_2 g_{m2}}{\alpha_2} . \frac{R_S}{(1 + g_{m2} R_F)^2}$	M_2	0.02	3.7%
$+\frac{\gamma_3 g_{m3}}{\alpha_3} . \frac{R_S}{(1 + g_{m2} R_F)^2}$	M_3	0.02	2.4%
$+\frac{1}{R_B} . \frac{R_S}{(1 + g_{m2} R_F)^2}$	R_B	0.01	1.2%
Total		**1.56 (1.94 dB)**	**100%**

Table B.2 shows the thermal noise contribution of the Gyrator-like LNA implemented in this work. More than half of the total noise is due to the M_{1N} transistor, followed by the feedback resistor R_F and the PMOS transistor M_{1P}.