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# Contribution to the study of transmitters at millimeter frequencies on emerging and advanced technologies

Tony Hanna

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THÈSE PRESENTÉE  
POUR OBTENIR LE GRADE DE  
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**ÉCOLE DOCTORALE DES SCIENCES PHYSIQUES ET DE L'INGÉNIEUR**  
SPECIALITÉ : ÉLECTRONIQUE

**Tony HANNA**

**Contribution à l'étude de transmetteurs aux fréquences millimétriques  
sur des technologies émergentes et avancées**

Sous la direction de : Nathalie DELTIMPLE

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## **Title: Contribution to the study of transmitters at millimeter frequencies on emerging and advanced technologies**

**Abstract:** For nearly half a century, the microelectronics industry has flourished based on the scaling of the silicon CMOS transistor technology. However, the race to transistor miniaturization encounters inevitable physical barriers. Thus, many technological works are under way for the realization of future transistors on emerging and advanced technologies. These technologies, notably the graphene and the CMOS FD-SOI, represent great opportunities for research in the fields of microelectronics, and especially for the design of radiofrequency and millimeter circuits. Besides, with the rising evolution of wireless devices and services, researchers are intensively working on the fifth generation (5G) wireless systems. The demand for high speed data and the need for more spectrum, have motivated the use of millimeter wave carrier frequencies. Therefore, the 5G research is faced with an evolving set of challenges. One of the major challenges of the next generation communication technology is reducing energy consumption. In fact, the power efficiency is directly related to the reliability and cost of the communication systems. It is widely known that the radiofrequency power amplifier is the most power consuming component in the radio transceivers, and is also one of the most critical building blocks in radio front-end. Therefore, research in this area is crucial for next generation communication systems. Consequently, the objective of this thesis is to study and design power amplifiers on emerging and advanced technologies for 5G applications.

**Keywords:** Power amplifiers, 5G, Graphene, CMOS FD-SOI, Integrated circuits.

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## **Titre : Contribution à l'étude de transmetteurs aux fréquences millimétriques sur des technologies émergentes et avancées**

**Résumé :** Depuis près d'un demi-siècle, l'industrie de la microélectronique a prospéré grâce à la miniaturisation des transistors Si CMOS. Cependant, la course à la miniaturisation se heurtera dans les prochaines années à des barrières physiques incontournables. Ainsi, de nombreux travaux technologiques sont en cours de réalisation sur les technologies émergentes et avancées. Ces technologies, notamment le graphène et la CMOS FD-SOI, représentent de grandes opportunités dans le domaine de la microélectronique, et notamment pour la conception de circuits radiofréquences et millimétriques. En outre, avec l'évolution croissante des objets et services connectés, les chercheurs travaillent intensivement sur les systèmes sans fil de cinquième génération (5G). La demande de débit de données et le besoin de spectre ont motivé l'utilisation de fréquences millimétriques. Par conséquent, la recherche 5G est confrontée par un ensemble de défis. L'un des défis majeurs de la 5G est la réduction de la consommation d'énergie. En fait, l'efficacité énergétique est directement liée à la fiabilité et au coût des systèmes de communication. L'amplificateur de puissance est l'élément le plus consommateur d'énergie, et l'un des blocs les plus critiques des émetteurs-récepteurs radio. Ainsi, la recherche dans ce domaine est cruciale pour les systèmes de communication de la prochaine génération. Par conséquent, l'objectif de cette thèse est d'étudier et de concevoir des amplificateurs de puissance sur les technologies émergentes et avancées pour les applications 5G.

**Mots clés :** Amplificateurs de puissance, 5G, Graphène, CMOS FD-SOI, Circuits intégrés.

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### **Research unit**

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*To my loved ones*



## TABLE OF CONTENTS

# TABLE OF CONTENTS

<b>LIST OF FIGURES</b>	11
<b>LIST OF TABLES</b>	15
<b>GLOSSARY</b>	16
<b>LIST OF PUBLISHED WORKS</b>	18
<b>GENERAL INTRODUCTION</b>	20
<b>CHAPTER I CONTEXT AND BACKGROUND</b>	23
Introduction	24
1. Wireless Communication	25
1.1. A Brief History of Wireless Communication	25
1.2. Mobile Communication Technologies	26
1.2.1. The Deployed Generations	26
1.2.2. The Fifth Generation	27
1.3. Radiofrequency Transmitters	31
1.3.1. Homodyne Transmitters	31
1.3.2. Heterodyne Transmitters	32
1.3.3. Power Amplifiers in Transmitters	32
2. Power Amplifiers Bibliographic Review	33
2.1. Definitions and General Principles	33
2.1.1. Output Power	33
2.1.2. Gain	34
2.1.3. Efficiency	34
2.1.4. Linearity	35
2.2. Power Amplifier Architectures	36
2.2.1. Power Amplifier Structures	36
2.2.2. Power Amplifier Topologies	37
2.3. Power Amplifier Classes	37
2.3.1. Sinusoidal Classes	37
2.3.2. Switching Classes	39
2.3.3. Waveform Engineering Classes	40
2.4. Impedance Matching	42
2.4.1. Conjugate Matching	42
2.4.2. Load-pull Matching	42
2.5. Combination of stages	43
3. Transistor Technologies	44
3.1. A Brief History of Transistors	44

## TABLE OF CONTENTS

3.2. Transistor Evolution and Scaling	45
3.2.1. Moore's Law	45
3.2.2. Emerging Technologies	46
3.2.3. Advanced Technologies	46
3.3. Transistors Types	47
Conclusion	49
References	50
<b>CHAPTER II POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY</b>	<b>53</b>
Introduction	54
1. Graphene Physics	55
1.1. Graphene Properties	55
1.2. Graphene Fabrication Methods	56
2. Graphene Field-Effect Transistors	58
2.1. GFET Structure	58
2.2. GFET State of the Art	58
2.3. GFET $f_T$ , $f_{max}$ and Scaling	62
2.4. GFET Contact Resistances	64
2.5. GFET Current Saturation	65
2.6. GFET Process Variability	66
3. State of the Art of Graphene RF Circuits and Amplifiers	67
3.1. State of the Art of Graphene Circuits	67
3.2. State of the Art of Graphene Amplifiers	69
4. Graphene Transistors Properties and Characteristics	71
4.1. GFET with Graphene Synthesized on SiC Substrate	71
4.2. GFET with CVD-grown Graphene on Si/SiO <sub>2</sub> Substrate	72
4.3. GFET with Mechanically Exfoliated Graphene and h-BN Dielectrics	73
5. GFET Compact Model	75
5.1. Model Description	75
5.2. Model Parameters	76
6. Graphene Power Amplifiers Design	78
6.1. GFET with Graphene Synthesized on SiC Substrate PA	80
6.2. GFET with CVD-grown Graphene on Si/SiO <sub>2</sub> Substrate PA	81
6.3. GFET with Mechanically Exfoliated Graphene and h-BN Dielectrics PA	82
7. Post-layout Simulation Results	83
7.1. GFET with Graphene Synthesized on SiC Substrate PA Results	83
7.2. GFET with CVD-grown Graphene on Si/SiO <sub>2</sub> Substrate PA Results	84
7.3. GFET with Mechanically Exfoliated Graphene and h-BN Dielectrics PA Results	84
8. Results Discussion	85
9. Multistage GFET Amplifiers	88
Conclusion	91
References	92

## TABLE OF CONTENTS

<b>CHAPTER III POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY</b>	97
<i>Introduction</i>	98
<b>1. The 28 nm CMOS FD-SOI Technology</b>	99
1.1. CMOS Technologies	99
1.2. The CMOS FD-SOI Transistor	100
1.3. The 28 nm FD-SOI Transistors Types and Body Biasing	101
1.4. The 28 nm FD-SOI Transistor Characteristics	103
1.5. The 28 nm FD-SOI Technology Back-End of Line	104
1.6. The 28 nm FD-SOI Technology Design Rules	105
<b>2. Overview of 5G Power Amplifiers</b>	106
2.1. 5G Power Amplifier Specifications	106
2.2. State of the Art of CMOS 5G Power Amplifiers at 28 GHz	108
2.3. Review of State of the Art 5G CMOS Power Amplifiers	111
<b>3. Review of Power Amplifier Architecture for 5G Applications</b>	113
3.1. Highly Efficient Modes of Operation	113
3.2. Sinusoidal Classes Optimization	114
3.3. State of the Art of Class J Amplifiers	115
<b>4. Design and Analysis of Class J Power Amplifiers</b>	118
4.1. Class J Amplifier Theory	118
4.2. Class J Amplifier Design	120
4.3. Class J Amplifier Versus the Frequency	121
<b>5. Power Amplifier Design Methodology</b>	123
<b>6. Power Amplifier Design</b>	125
6.1. Transistor Sizing and Layout	125
6.2. Power Amplifier Topology	127
6.3. Class J Power Stage Design	128
6.4. Driver Stage and Matching Networks Design	130
6.5. Layout of the Amplifier	131
<b>7. Post-layout Simulation Results</b>	133
<b>8. Circuit Measurement</b>	135
<i>Conclusion</i>	139
<i>References</i>	140
<b>GENERAL CONCLUSION AND PERSPECTIVES</b>	143



## LIST OF FIGURES

### LIST OF FIGURES

Fig. 1.1	Marconi's first transmitter incorporating a monopole antenna.	25
Fig. 1.2	Evolution of mobile communication technologies.	27
Fig. 1.3	Variation of mobile subscribers with the years.	27
Fig. 1.4	Cisco VNI [I.6] (a) Future data usage (b) Growth of mobile traffic data per region in 2016.	28
Fig. 1.5	The three ITU regions.	30
Fig. 1.6	The 5G frequency candidates above 6 GHz.	30
Fig. 1.7	Sea level atmospheric attenuation (10 – 300 GHz).	31
Fig. 1.8	Simplified homodyne transmitter block diagram.	31
Fig. 1.9	Simplified heterodyne transmitter block diagram.	32
Fig. 1.10	Power consumption breakdown of a 4G smartphone [I.15].	32
Fig. 1.11	Characteristic parameters of a PA.	33
Fig. 1.12	Output power in function of the input power of a sine signal.	35
Fig. 1.13	AM/AM and AM/PM conversions.	36
Fig. 1.14	Power amplifier structures.	36
Fig. 1.15	Power amplifier topologies.	37
Fig. 1.16	Power amplifier sinusoidal classes biasing points.	38
Fig. 1.17	Class D and E waveforms and schematics.	39
Fig. 1.18	Class F waveform and schematic.	40
Fig. 1.19	Typical class J amplifier drain source current and voltage waveforms.	41
Fig. 1.20	Source and load impedances.	42
Fig. 1.21	Example of output power and PAE load-pull contours for different impedances.	43
Fig. 1.22	A replica of the bipolar transistor developed at Bell Labs in 1947.	44
Fig. 1.23	CMOS device structure from Fairchild Semiconductor patent.	44
Fig. 1.24	Transistor count, clock speed and thermal design power evolution with the years [I.23].	45
Fig. 1.25	Standard versus FinFET transistor [I.23].	46
Fig. 1.26	Electron flow in bulk and FD-SOI CMOS transistor.	47
Fig. 1.27	Power level versus frequency per process.	48
Fig. 2.1	Scanning probe microscopy image of graphene [II.3].	55
Fig. 2.2	Energy band structure around the first Brillouin zone of large area-graphene, GNR, unbiased and biased bilayer graphene [II.17].	56
Fig. 2.3	Classification of graphene methods of preparation per quality and price [II.2].	56
Fig. 2.4	Illustration of the Dirac points of the CVD graphene and the graphene synthesized on SiC.	57
Fig. 2.5	Cross sectional view of a GFET structure.	58
Fig. 2.6	The first demonstrated GFET [II.24] (a) SEM image (b) Transfer characteristic.	59
Fig. 2.7	GFETs in [II.31] (a) The graphene wafer and schematic cross-sectional view of the GFET (b) $I_D$ vs. $V_G$ for gate length of 240 nm (c) $I_D$ vs. $V_D$ for gate length of 240 nm (d) Measured small-signal current gain $ h_{21} $ as a function of frequency.	59
Fig. 2.8	GFETs in [II.32] (a) Cross-section TEM image of graphene transistor of gate length of 40 nm (b) Cut-off frequency of the 550 nm and 40 nm devices (c) GFETs cut-off frequencies versus gate length (d) Drain current versus the drain and gate voltages for the 550 nm and 40 nm devices.	60

## LIST OF FIGURES

Fig. 2.9	<i>GFETs in [II.33] (a) Optical image of self-aligned graphene transistors (b) Cross-sectional TEM image of a device (c) <math>I_{DS}</math> vs. <math>V_{DS}</math> of 300 nm gate length (d) <math>f_T</math> for 220 nm gate length (e) <math>f_T</math> for 100 nm gate length (f) <math>f_T</math> for 46 nm gate length.</i>	61
Fig. 2.10	<i>GFETs in [II.34] SEM image of a 100 nm gate length device (b) <math>f_T</math> before and after de-embedding for two 100 nm devices (c) <math>f_{max}</math> before and after de-embedding for two 100 nm devices.</i>	61
Fig. 2.11	<i>GFETs in [II.35] (a) SEM image (b) Photo of the 3 inch wafer on Si substrate (c) <math>I_{DS}</math> vs. <math>V_{DS}</math> for 60 nm gate length GFET (d) <math>f_T</math> of GFET before and after de-embedding (e) <math>f_{max}</math> of GFET before and after de-embedding.</i>	62
Fig. 2.12	<i>Small-signal equivalent circuit of a FET.</i>	63
Fig. 2.13	<i><math>f_{max}</math> dependence on the gate resistance [II.37].</i>	63
Fig. 2.14	<i>Frequency performances of state of the art Si, GaAs, InP and graphene transistors [II.38].</i>	64
Fig. 2.15	<i>Illustration of the GFET contact and access resistances.</i>	64
Fig. 2.16	<i>(a) <math>f_T/f_{max}</math> of five 400 nm GFETs in [II.37] (b) Distribution of peak gm of fourteen 550 nm GFETs in [II.45].</i>	66
Fig. 2.17	<i>[II.46] (a) Percentage of working devices (b) Histogram of the average contact resistance of each die over the wafer (c) Contact resistance versus percentage of working devices.</i>	66
Fig. 2.18	<i>Graphene receiver in [II.47] (a) Optical micrograph (<math>1020 \times 600 \mu\text{m}^2</math>) (b) Circuit schematic (c) Measured waveforms of RF input signal amplitude modulated at a rate of 20 Mb/s, IF output signal, and restored binary code after rectifying and low-pass filtering IF signal (d) Receiver output waveforms taken from the oscilloscope.</i>	67
Fig. 2.19	<i>Graphene based high data rate communication landscape [II.48] (a) A perspective view of high data rate link based on graphene transmitter and receiver (b) Fabricated chip (<math>15 \times 15 \text{ mm}^2</math>) consists of frequency mixer ICs (left: <math>1.35 \times 1.1 \text{ mm}^2</math>) and integrated power detector ICs (right: <math>1.35 \times 0.7 \text{ mm}^2</math>).</i>	68
Fig. 2.20	<i>The 185 to 215 GHz graphene subharmonic mixer [II.52] (a) Schematic of the circuit (b) Micrograph of the fabricated circuit.</i>	69
Fig. 2.21	<i>Schematics and photos of state of the art graphene-based amplifiers (a) [II.60] (b) [II.61] (c) [II.62] (d) [II.64] (e) [II.65].</i>	70
Fig. 2.22	<i>GFET with graphene synthesized on SiC substrate (a) Schematic of the cross section of the device (b) SEM image of the device.</i>	71
Fig. 2.23	<i>GFET with graphene synthesized on SiC substrate (a) Output characteristic <math>I_{DS}</math> in function of <math>V_{DS}</math> for different <math>V_{GS}</math> measurements and simulations (b) S-parameters for <math>V_{DS} = 1</math> and 3 V and <math>V_{GS} = -3</math> and 2 V, dotted lines are measurements and complete lines are simulations.</i>	72
Fig. 2.24	<i>GFET with CVD-grown graphene on Si/SiO<sub>2</sub> Substrate (a) Schematic of the cross section of the device (b) SEM image of the device.</i>	72
Fig. 2.25	<i>GFET with CVD-grown graphene on Si/SiO<sub>2</sub> substrate (a) Output characteristic <math>I_{DS}</math> in function of <math>V_{DS}</math> for different <math>V_{GS}</math> measurements and simulations (b) S-parameters for <math>V_{DS} = 1.5</math> V and <math>V_{GS} = 0.5</math> and 1 V, dotted lines are measurements and complete lines are simulations.</i>	73
Fig. 2.26	<i>GFET with mechanically exfoliated graphene and h-BN dielectrics (a) Schematic of the device structure (b) Optical micrograph of the device.</i>	74
Fig. 2.27	<i>GFET with mechanically exfoliated graphene and h-BN dielectrics output characteristic <math>I_{DS}</math> in function of <math>V_{DS}</math> for different <math>V_{GS}</math> measurements and simulations.</i>	74
Fig. 2.28	<i>Equivalent circuit of GFET electrical compact model.</i>	76
Fig. 2.29	<i>Schematic of the single stage common source GFET amplifiers.</i>	78
Fig. 2.30	<i>Smith chart reporting <math>S_{11}</math> parameter of the tree GFET devices.</i>	78

## LIST OF FIGURES

Fig. 2.31	Maximum available power gain in function of the frequency of a GFET synthesized on SiC power amplifier for $V_{DS} = 3$ V and $V_{GS} = -2$ V.	79
Fig. 2.32	Metal stack used for designing the graphene amplifiers.	79
Fig. 2.33	Layout of the GFET synthesized on SiC amplifier ( $1.2 \times 1.2$ mm <sup>2</sup> ).	80
Fig. 2.34	Layout of the CVD-grown GFET amplifier ( $1.2 \times 1.2$ mm <sup>2</sup> ).	81
Fig. 2.35	Layout of the mechanically exfoliated GFET amplifier ( $1.2 \times 1.2$ mm <sup>2</sup> ).	82
Fig. 2.36	S-parameters of the GFET with graphene synthesized on SiC PA for both max. PAE and $P_{OUT}$ Bias points.	83
Fig. 2.37	Large signal results of the GFET with graphene synthesized on SiC amplifier for both max. PAE and $P_{OUT}$ bias points.	83
Fig. 2.38	(a) S-parameters results of the GFET with CVD-grown graphene amplifier (b) Large signal results of the GFET with CVD-grown graphene amplifier.	84
Fig. 2.39	(a) S-parameters results of the GFET with mechanically exfoliated graphene amplifier (b) Large signal results of the GFET with mechanically exfoliated graphene amplifier.	84
Fig. 2.40	GFET and Si CMOS characteristics comparison.	86
Fig. 2.41	Variation of the output power and PAE of the GFET synthesized on SiC amplifier in function of $R_D$ and $R_S$ .	87
Fig. 2.42	Schematic of the two-stage common source GFET amplifier.	88
Fig. 2.43	Layout of the two stages GFET synthesized on SiC amplifier ( $2 \times 1.2$ mm <sup>2</sup> ).	89
Fig. 2.44	S-parameters results of the two stages GFET synthesized on SiC amplifier.	89
Fig. 2.45	Large signal results of the two stages GFET synthesized on SiC amplifier.	90
Fig. 3.1	System in Package versus System on Chip transceiver integration.	99
Fig. 3.2	CMOS, SiGe and GaAs technologies comparison [III.2].	99
Fig. 3.3	Forecast of the $f_T$ and $f_{max}$ of the MOS technologies [III.3].	100
Fig. 3.4	CMOS bulk and FD-SOI transistors cross section.	101
Fig. 3.5	Hybridization in UTBB FD-SOI technology.	101
Fig. 3.6	FD-SOI conventional well and flip well transistors with body biasing ranges.	102
Fig. 3.7	Variation of the foreword body bias in bulk and FD-SOI NMOS.	102
Fig. 3.8	$I_{DS}$ versus $V_{DS}$ measurements for LVT transistors in 28nm Bulk and 28nm FD-SOI [III.2].	103
Fig. 3.9	Measurements of $H_{21}$ and MSG/MAG for LVT transistors in 28 nm Bulk and 28 nm FD-SOI [III.2].	103
Fig. 3.10	The ten metals version of the Back-end of line of the 28 nm FD-SOI technology.	104
Fig. 3.11	Number of design rules to be respected per CMOS technology node [III.2].	105
Fig. 3.12	The final 5G frequency candidates above 6 GHz.	106
Fig. 3.13	Number of published papers on RF PAs per year [III.12].	106
Fig. 3.14	Example of the typical output power and efficiency curves in a PA [III.13].	107
Fig. 3.15	PA in [III.14] (a) Schematic of the circuit (b) Die micrograph.	108
Fig. 3.16	PA in [III.14] (a) Gain, drain efficiency and PAE in function of the output power at 30 GHz (b) Power and efficiency performances versus the frequency.	108
Fig. 3.17	PA in [III.15] (a) Schematic of the circuit (b) Die photograph.	109
Fig. 3.18	PA in [III.15] (a) Measured and simulated S-parameters (b) Measured and simulated large-signal characteristics at 28 GHz.	109
Fig. 3.19	PA in [III.16] (a) Block diagram of the balanced PA (b) Schematic of the PA power cells (c) Die photograph.	110
Fig. 3.20	PA in [III.16] (a) Measured S-Parameters (b) Power gain and PAE versus the output power at 27 GHz.	110
Fig. 3.21	Source current in single-ended and differential structures.	111
Fig. 3.22	Class E and F amplifiers schematics and output waveforms.	113

## LIST OF FIGURES

Fig. 3.23	Doherty PA [III.20] (a) Schematic (b) Efficiency versus output power in ideal conditions (c) Simulated efficiency versus output power at 60 GHz.	113
Fig. 3.24	PA output power and efficiency in function of the conduction angle [III.22].	114
Fig. 3.25	Harmonic composition of the output current in function of the conduction angle [III.17].	114
Fig. 3.26	The first demonstrated class J power amplifier [III.25].	115
Fig. 3.27	Number of fabricated class J amplifiers per technology.	116
Fig. 3.28	Schematics and photograph of the demonstrated integrated class J amplifiers (a) [III.26] (b) [III.27] (c) [III.28] (d) [III.29].	117
Fig. 3.29	(a) Continuous drain voltage waves in function of $\alpha$ (b) Smith chart of the fundamental and second harmonic impedances of the continuous waves modes.	119
Fig. 3.30	(a) Class AB and J output waveforms (b) Smith chart of a class J amplifier harmonic impedances with $R_{opt} = 10 \Omega$ .	120
Fig. 3.31	The fundamental and second harmonic output impedances of the $\pi$ matching network.	121
Fig. 3.32	Values of the inductance and its equivalent series resistance of a class J $\pi$ network versus the frequency (transistor width = 200 $\mu\text{m}$ ).	121
Fig. 3.33	Design flowchart of the power amplifier on 28 nm FD-SOI technology.	124
Fig. 3.34	(a) Elementary transistor layout view (b) 4 fingers transistor layout view.	125
Fig. 3.35	$f_{max}$ in function of the finger width and channel length.	125
Fig. 3.36	$I_{DS}$ vs. $V_{DS}$ of an LVT nFET in function of $W$ for $V_{GS} = 0.3 \text{ V}$ and $V_{BB} = 0 \text{ V}$ .	126
Fig. 3.37	(a) Layout of a 52 fingers transistor and its interconnections (b) Four parallel 52 fingers transistor blocks connected.	127
Fig. 3.38	Common source and cascode schematics.	127
Fig. 3.39	Chosen schematic of the power amplifier.	128
Fig. 3.40	Power stage class J schematic.	129
Fig. 3.41	Driver stage schematic.	130
Fig. 3.42	Smith chart of the input and inter-stage matching networks at 28 GHz.	131
Fig. 3.43	Layout of the power amplifier ( $1050 \times 740 \mu\text{m}^2$ ).	132
Fig. 3.44	3D view of (a) MOM capacitance (b) RF pads (c) Ground plane elementary cell.	132
Fig. 3.45	Post-layout results of the S-parameters of the amplifier.	133
Fig. 3.46	Large signal post-layout simulation results (a) The output power and PAE at 28 GHz (b) The saturated power versus the frequency.	133
Fig. 3.47	Large signal post-layout simulation results at 28 GHz (a) PAE for different $V_{BB1}$ (b) Output power for different $V_{BB2}$ .	134
Fig. 3.48	(a) Power amplifier photograph (b) Measurement setup (c) Biasing setup.	135
Fig. 3.49	S-parameters measurements (solid lines) and redo simulations (dashed lines).	136
Fig. 3.50	Simulated schematic of the amplifier showing the RF ground path.	136
Fig. 3.51	S-parameters measurements (solid lines) and redo simulations (dashed lines) with DC sources turned OFF.	137
Fig. 3.52	Measured output power and PAE of the amplifier at 8 GHz.	138
Fig. 3.53	Layout with the added ground pads in the upper-side of the circuit.	138

## LIST OF TABLES

## LIST OF TABLES

<i>Table 1.1</i>	<i>Graphene properties.</i>	<i>46</i>
<i>Table 1.2</i>	<i>Comparison of transistor/IC substrates [I.27].</i>	<i>47</i>
<i>Table 2.1</i>	<i>Graphene properties obtained by different methods [II.2].</i>	<i>57</i>
<i>Table 2.2</i>	<i>State of the art of metal/graphene contact resistances [II.43].</i>	<i>65</i>
<i>Table 2.3</i>	<i>State of the Art of graphene-based amplifiers.</i>	<i>69</i>
<i>Table 2.4</i>	<i>Extracted compact model parameters of the three GFETs.</i>	<i>77</i>
<i>Table 2.5</i>	<i>Performances of the graphene PAs.</i>	<i>85</i>
<i>Table 3.1</i>	<i>State of the art CMOS 5G power amplifiers operating in the 28 GHz band.</i>	<i>112</i>
<i>Table 3.2</i>	<i>State of the art of the integrated class J amplifiers.</i>	<i>116</i>
<i>Table 3.3</i>	<i>Common source and cascode topologies comparison.</i>	<i>128</i>
<i>Table 3.4</i>	<i>Post-layout simulation results comparison with state of art 28 GHz PAs.</i>	<i>134</i>

## GLOSSARY

## GLOSSARY

<i>0G</i>	<i>Mobile Radio Telephony</i>
<i>1G</i>	<i>First Generation of Wireless Cellular Technology</i>
<i>2G</i>	<i>Second Generation of Wireless Cellular Technology</i>
<i>3G</i>	<i>Third Generation of Wireless Cellular Technology</i>
<i>4G</i>	<i>Fourth Generation of Wireless Cellular Technology</i>
<i>5G</i>	<i>First Generation of Wireless Cellular Technology</i>
<i>AC</i>	<i>Alternative Current</i>
<i>ACLR</i>	<i>Adjacent Channel Leakage Ratio</i>
<i>BEOL</i>	<i>Back-End of Line</i>
<i>BJT</i>	<i>Bipolar Junction Transistor</i>
<i>BO</i>	<i>Back-off</i>
<i>BOX</i>	<i>Buried Oxide</i>
<i>BW</i>	<i>Bandwidth</i>
<i>CAD</i>	<i>Computer Aided Design</i>
<i>CL</i>	<i>Conversion Loss</i>
<i>CMOS</i>	<i>Complementary Metal-Oxide-Semiconductor</i>
<i>CP1</i>	<i>1 dB Compression Point</i>
<i>CPW</i>	<i>Coplanar Wave Guide</i>
<i>CVD</i>	<i>Chemical Vapor Deposition</i>
<i>DC</i>	<i>Direct Current</i>
<i>DE (<math>\eta_d</math>)</i>	<i>Drain Efficiency</i>
<i>DRC</i>	<i>Design Rules Check</i>
<i>DRM</i>	<i>Design Rules Manual</i>
<i>ESR</i>	<i>Equivalent Series Resistance</i>
<i>EVM</i>	<i>Error Vector Magnitude</i>
<i>FBB</i>	<i>Forward Body Bias</i>
<i>FDE</i>	<i>Frequency Domain Equalization</i>
<i>FD-SOI</i>	<i>Fully Depleted Silicon on Insulator</i>
<i>FEM</i>	<i>Finite Element Method</i>
<i>FET</i>	<i>Field-Effect Transistor</i>
<i><math>f_{max}</math></i>	<i>Maximum Oscillation Frequency</i>
<i><math>f_r</math></i>	<i>Cut-off Frequency</i>
<i><math>g_{ds}</math></i>	<i>Source-Drain Conductance</i>
<i>GFET</i>	<i>Graphene Field-Effect Transistor</i>
<i><math>g_m</math></i>	<i>Transconductance</i>
<i>GNR</i>	<i>Graphene Nanoribbon</i>
<i><math>H_{21}</math></i>	<i>Small-signal Current Gain</i>
<i>HBT</i>	<i>Heterojunction Bipolar Transistor</i>
<i>HEMT</i>	<i>High Electron Mobility Transistor</i>

## GLOSSARY

<i>IC</i>	<i>Integrated Circuit</i>
<i>ICP1</i>	<i>Input 1 dB Compression Point</i>
<i>IF</i>	<i>Intermediate Frequency</i>
<i>IoT</i>	<i>Internet of Things</i>
<i>IP</i>	<i>Internet Protocol</i>
<i>ITRS</i>	<i>International Technology Roadmap for Semiconductors</i>
<i>ITU</i>	<i>International Telecommunication Union</i>
<i>LDMOS</i>	<i>Laterally Diffused MOSFET</i>
<i>LVS</i>	<i>Layout Versus Schematic</i>
<i>LVT</i>	<i>Low Voltage Threshold</i>
<i>M2M</i>	<i>Machine-to-Machine</i>
<i>MAG</i>	<i>Maximum Available Gain</i>
<i>MESFET</i>	<i>Metal Semiconductor Field-Effect Transistors</i>
<i>MIMO</i>	<i>Multiple-Input Multiple-Output</i>
<i>MMIC</i>	<i>Monolithic Microwave Integrated Circuit</i>
<i>MOM</i>	<i>Metal Oxide Metal</i>
<i>MOSFET</i>	<i>Metal Oxide Semiconductor Field-Effect Transistor</i>
<i>MSG</i>	<i>Maximum Stable Gain</i>
<i>NF</i>	<i>Effective Doping Density</i>
<i>OCP1</i>	<i>Output 1 dB Compression Point</i>
<i>OFDM</i>	<i>Orthogonal Frequency-Division Multiplexing</i>
<i>PA</i>	<i>Power Amplifier</i>
<i>PAE</i>	<i>Power Added Efficiency</i>
<i>PAPR</i>	<i>Peak-to-Average Power Ratio</i>
<i>PCB</i>	<i>Printed-Circuit Board</i>
<i>PDC</i>	<i>Consumed DC Power</i>
<i>PDK</i>	<i>Process Design Kit</i>
<i>Pin</i>	<i>Input Power</i>
<i>PLS</i>	<i>Post-Layout Simulation</i>
<i>PNA</i>	<i>Purpose Network Analyzer</i>
<i>Pout</i>	<i>Output Power</i>
<i>Psat</i>	<i>Saturated Output Power</i>
<i>RBB</i>	<i>Reverse Body Bias</i>
<i>RF</i>	<i>Radiofrequency</i>
<i>RVT</i>	<i>Regular Voltage Threshold</i>
<i>SOA</i>	<i>Safe Operating Area</i>
<i>SoC</i>	<i>System on Chip</i>
<i>SOI</i>	<i>Silicon on Insulator</i>
<i>URLLC</i>	<i>Ultra-Reliable Low Latency</i>
<i>UTBB</i>	<i>Ultra-Thin Body and Buried oxide</i>
<i>VNI</i>	<i>Visual Networking Index</i>
<i>Vsat</i>	<i>Saturation Velocity</i>
<i>Vth</i>	<i>Threshold Voltage</i>

## LIST OF PUBLISHED WORKS

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#### International journals:

T. Hanna N. Deltimple, M. S. Khenissa, E. Pallecchi, H. Happy and S. Frégonèse, '2.5 GHz Integrated Graphene RF Power Amplifier on SiC Substrate', Solid-State Electronics, Volume 127, January 2017, Pages 26–31.

T. Hanna, N. Deltimple and S. Frégonèse, 'Class J Power Amplifier Design in 28 nm CMOS FD-SOI Technology', Journal of Integrated Circuits and Systems (accepted).

#### International conferences:

T. Hanna, N. Deltimple and S. Frégonèse, 'A Class-J Power Amplifier for 5G Applications in 28nm CMOS FD-SOI Technology', 30th Symposium on Integrated Circuits and Systems Design, Fortaleza, Brazil, September 2017.

T. Hanna, N. Deltimple and S. Frégonèse, 'A Wideband Highly Efficient Class-J Integrated Power Amplifier for 5G Applications', The 15th IEEE International New Circuits and Systems Conference (NEWCAS), Strasbourg, France, June 2017.

T. Hanna, N. Deltimple and S. Frégonèse, 'Wideband High Efficiency Power Amplifier for 5G Applications', 3rd International Congress on Advanced Technologies, Safi, Morocco, April 2017.

#### French national conferences:

T. Hanna, N. Deltimple and S. Frégonèse, 'Design of 2.5 GHz Integrated Graphene RF Power Amplifiers', Colloque 2016 du GDR SoC/SiP, Nantes, France, June 2016.





# GENERAL INTRODUCTION

Since the discovery of transistors, the evolution of these devices by making them smaller, faster, less power consuming and cheaper has been a constant motivation for the electronics industry over numerous decades. However, in the last few years, scaling-down transistors started to seem unattainable as the size of the silicon transistors has reached the atomic scale. In fact, the laws of physics would be impacted by quantum effects and new technological challenges arise as a consequence, which sets a limit to further development.

Therefore, the scientific community has been intensively searching for alternate solutions in order to continue the evolution of electronics. Two promising solutions are underway: new materials (emerging technologies) and new device concepts (advanced technologies).

Besides, with the rising evolution of wireless devices and services, researchers are working on the fifth generation of wireless systems (5G). The demand for high speed data and the need for more spectrum, have motivated the use of millimeter wave carrier frequencies. Therefore, the next generation research is faced with an evolving set of challenges. One of the major challenges of the next generation communication technology is reducing energy consumption. In fact, the power efficiency is directly related to the reliability and cost of the communication systems.

It is widely known that the radiofrequency power amplifier is the most power consuming component in the radio transceivers, and is also one of the most critical building blocks in radio front-end. Therefore, research in this area is crucial for next generation communication systems.

Consequently, the objective of this thesis is to study and design power amplifiers on emerging and advanced technologies for 5G applications. Two choices of orientation are taken in this work:

- On the emerging technologies part, graphene is the precursor candidate. Thanks to its outstanding physical properties, many laboratories and companies demonstrated state of the art graphene transistors with high frequency performances. However, few graphene circuits and even fewer amplifiers have been demonstrated. Thus, many details about the potential performance of graphene transistors in electronics applications remain unclear. For instance, the large signal performances of graphene amplifiers have never been reported. Consequently, in this work we carry out an investigation and evaluation of different graphene transistors, with different methods of fabrications and substrates, in power amplification. Our study is done in the lower frequency candidates of the 5G.
- On the advanced technologies part, the CMOS Fully Depleted Silicon on Insulator (FD-SOI), presents great threat to substitute the conventional CMOS transistor in many applications. In addition, this technology presents great opportunities for circuit designers. Therefore, this technology is used for designing a linear, highly efficient and wideband power amplifier for 5G applications. Our study is done in the higher frequency candidates of the 5G.

## GENERAL INTRODUCTION

This work is divided into three main chapters.

Chapter I presents the context of the thesis. It is divided into three axes:

- The first axis focuses on the wireless communication systems. First, each mobile technology from the 0G to the 4G is presented briefly. Then the next generation is discussed with a focus on its applications, specifications, technological solutions and frequency of operation. This axis concludes with the brief presentation of radiofrequency transmitters and the importance of power amplifiers in these systems.
- The second axis of the first chapter addresses power amplifiers. Bibliographical concepts of power amplifiers are listed, such as important design parameters and power amplifier architectures and classes.
- The first chapter ends with a presentation of the evolution of transistors technologies and the physical barriers encountered by this evolution. Then, two main solutions to the Moore's law continuation are described: emerging and advanced technologies.

The chapter one concludes with the choices of orientation of this thesis with regard of the constraints: Research on power amplifier for 5G applications on emerging (graphene) and advanced (28 nm CMOS FD-SOI) technologies.

In chapter II, the graphene technology is studied and evaluated for power amplification. The physics of graphene are presented, the graphene transistors are described and integrated graphene power amplifiers are designed and discussed. This chapter is divided into two main axes:

- The first axis addresses graphene field-effect transistors. The state of art graphene devices are presented since the discovery of graphene in 2004. Then, important subjects in graphene transistors such as scaling, contact resistances, current saturation and process variability are discussed. Afterwards, state of art of graphene circuits and amplifiers are listed.
- The second axis is the power amplifier design on graphene technology. Three common source fully-integrated graphene power amplifiers are designed based on three graphene transistors with different fabrication methods and substrates. Then, the results are discussed and evaluated and projected with the graphene technological enhancements.

In chapter III, the 28 nm CMOS FD-SOI technology is used for designing a linear, highly efficient and wideband power amplifier for 5G applications. This chapter is divided into two axes:

- The first axis presents the 28 nm CMOS FD-SOI technology: the transistor types, characteristics are reported. Then, state of art 5G power amplifiers on advanced CMOS nodes are presented.
- The second axis is the power amplifier design on this technology. After presenting the design methodology, the amplifier specifications are chosen. Then, a study on the power amplifier architectures is carried out in order to choose the topology that fits best the desired specifications. Afterwards the power amplifier is designed and results are discussed.

Finally, this work ends with a general conclusion which provides an overview of the thesis and perspectives for further works.



CHAPTER I: CONTEXT AND BACKGROUND

**Table of Contents**

<i>Introduction</i>	24
<i>1. Wireless Communication</i>	25
1.1. <i>A Brief History of Wireless Communication</i>	25
1.2. <i>Mobile Communication Technologies</i>	26
1.2.1. <i>The Deployed Generations</i>	26
1.2.2. <i>The Fifth Generation</i>	27
1.3. <i>Radiofrequency Transmitters</i>	31
1.3.1. <i>Homodyne Transmitters</i>	31
1.3.2. <i>Heterodyne Transmitters</i>	32
1.3.3. <i>Power Amplifiers in Transmitters</i>	32
<i>2. Power Amplifiers Bibliographic Review</i>	33
2.1. <i>Definitions and General Principles</i>	33
2.1.1. <i>Output Power</i>	33
2.1.2. <i>Gain</i>	34
2.1.3. <i>Efficiency</i>	34
2.1.4. <i>Linearity</i>	35
2.2. <i>Power Amplifier Architectures</i>	36
2.2.1. <i>Power Amplifier Structures</i>	36
2.2.2. <i>Power Amplifier Topologies</i>	37
2.3. <i>Power Amplifier Classes</i>	37
2.3.1. <i>Sinusoidal Classes</i>	37
2.3.2. <i>Switching Classes</i>	39
2.3.3. <i>Waveform Engineering Classes</i>	40
2.4. <i>Impedance Matching</i>	42
2.4.1. <i>Conjugate Matching</i>	42
2.4.2. <i>Load-pull Matching</i>	42
2.5. <i>Combination of stages</i>	43
<i>3. Transistor Technologies</i>	44
3.1. <i>A Brief History of Transistors</i>	44
3.2. <i>Transistor Evolution and Scaling</i>	45
3.2.1. <i>Moore's Law</i>	45
3.2.2. <i>Emerging Technologies</i>	46
3.2.3. <i>Advanced Technologies</i>	46
3.3. <i>Transistors Types</i>	47
<i>Conclusion</i>	49
<i>References</i>	50

### Introduction

As French philosopher Auguste Comte said: « On ne connaît pas complètement une science tant qu'on n'en sait pas l'histoire » meaning that one does not know completely a science as long as one does not know its history. This chapter begins with a presentation of the history of wireless communication, and the specification of each mobile technology from the 0G to the 4G. Subsequently, the 5G standard is discussed, its applications, specifications, technological solutions and frequency of operation are presented. The first part of this chapter ends with a brief description of the radiofrequency transmitters and the importance of power amplifiers in the wireless systems.

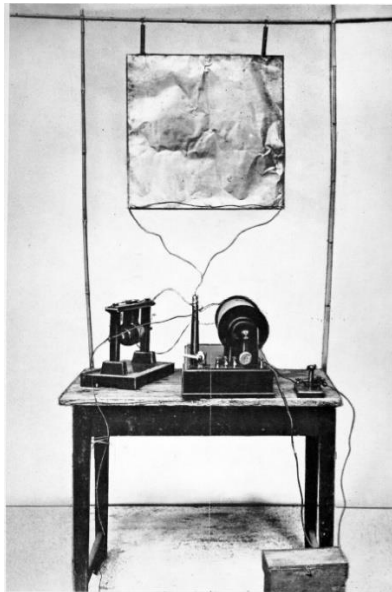
The second part of this chapter presents a bibliographic review of power amplifiers: first, definitions and general principles are described; then, different power amplifier structures, topologies and classes are reported. Finally, this part discusses impedance matching and combination of stages in an amplifier.

The last part of this chapter addresses transistor technologies and their evolution and scaling. The two main solutions for the Moore's law continuation are presented i.e. the emerging and advanced technologies. Finally, this part concludes with a brief description and comparison of different existing transistor types used for amplification.

### 1. Wireless Communication

#### 1.1. A Brief History of Wireless Communication

Most people are surprised to find that wireless technology dates back over 200 years. In fact, it all started in 1819, when the Danish physicist Hans Christian Ørsted noted that a compass needle would move in the presence of an electrical field, thus establishing the fundamental relationship between electricity and magnetism, and founding the field of electromagnetism. The next major progress was the result of theoretical works by the Scottish scientist James Clerk Maxwell. Maxwell published "On a Dynamical Theory of the Electromagnetic Field" in 1865, and "A Treatise on Electricity and Magnetism" in 1873, which became what are known Maxwell's Equations. These are a series of differential equations which describe the movement of electromagnetic waves through space. Maxwell's work was based on many empirical and theoretical works developed by Gauss, Ampere, Faraday, and others [1.1]. Remarkably, Maxwell's equations are still used to this day. Maxwell's formulation was cast in its modern form by Oliver Heaviside during the period from 1885 to 1887. Heaviside removed many of the mathematical complexities of Maxwell's theory, introduced vector notation, and provided a foundation for practical applications of guided waves and transmission lines. Subsequently, German physicist Heinrich Hertz carried out a set of experiments during the period from 1887 to 1891 that validated Maxwell's theory of electromagnetic waves.



*Fig. 1.1: Marconi's first transmitter incorporating a monopole antenna.*

Nikola Tesla was the first to transmit energy between two points without wire, demonstrating electromagnetic induction. However, no information was carried in this process. The recognition for the radio communication is often referred to the Italian engineer Guglielmo Marconi who in 1895 sent a radio telegraph transmission across the English Channel, and in 1901 a transmission across the Atlantic [1.2]. Because of the lack of reliable microwave sources and other components, the growth of radio technology in the early 1900s occurred primarily in the 3 to 300 MHz range. In the 1940s, with the start of radar development during World War II, microwave theory and technology received considerable interest. Wired and wireless communications systems using microwave technology began to be developed soon after the development of the radar, benefiting from much of

## CHAPTER I: CONTEXT AND BACKGROUND

the work that was done for radar systems. Since then, wireless communication applications and needs kept increasing and hence offering objectives and challenges to the scientific research.

### 1.2. Mobile Communication Technologies

#### 1.2.1. The Deployed Generations

Since the emergence of mobile communications in the 1970s, a new generation is deployed every decade. In this subsection, we briefly present the services and specifications of every mobile generation.

Mobile radio telephone systems referred to as 0G were introduced in 1970s where wireless service offerings were a rare and high-priced way of communication. In this generation, the telephone was mounted on the dashboard of a vehicle and contained buttons for manual selection of an available radio frequency.

The first generation (1G) was deployed in the early 1980s. This generation used analog radio waves to communicate with the base stations that were developed across the world. However, different 1G standards were used worldwide. The main difference between the 0G and 1G systems was the discovery of the cellular technology. The 1G systems were limited to only voice traffic and suffered from limitations of low capacity, unreliable handoff, poor voice links, and no security at all since anybody with an all-band radio receiver could listen to the conversation [I.3].

The 2G was commercially launched in 1991 [I.3]. The 2G networks employed digital modulation and advanced call processing capabilities. The phone conversations are converted into digital pulses, which can be encrypted for more security. Additionally, 2G mobile phone networks provided services such as text, picture and multimedia messages. The 2G systems are significantly more efficient on the spectrum than the 1G, allowing greater mobile phone penetration levels. Later 2G releases, the 2.5G and 2.75G, are bridging technologies between the 2G and 3G standards.

The first 3G networks were introduced in 1998. While the 1G and 2G standards were diverse for different parts of the world, the 3G aims to provide services independent of the technology platform and whose network design standards are the same globally [I.4]. To meet the 3G requirements, a system is required to provide peak data rates of at least 200 kbit/s. Moreover, 3G services include wireless voice telephony, mobile internet access, fixed wireless internet access, video calls and mobile television. Later 3G releases, often denoted 3.5G and 3.75G, also provide mobile broadband access of several Mbit/s to smartphones and mobile modems in laptop computers.

The 4G standard has been commercially deployed since 2009. The main aim of the 4G is to integrate all the existing mobile technologies with simplified structure. The factors that distinguish the 4G networks [I.3] are roaming across networks, Internet Protocol (IP) interoperability and higher speeds (100 Mbit/s for high mobility communication and 1 Gbit/s for low mobility communication). The spread spectrum radio technology used in 3G systems, is abandoned in all 4G systems and replaced by Orthogonal Frequency-Division Multiplexing (OFDM) multi-carrier transmission and other Frequency-Domain Equalization (FDE) schemes, making it possible to transfer very high bit rates despite extensive multi-path radio propagation. In addition, the peak bit rate is further improved by smart antenna arrays for Multiple-Input Multiple-Output (MIMO) communications.

Fig. 1.2 recapitulates the evolution of mobile generations from the 1G arriving to the 5G.



## CHAPTER I: CONTEXT AND BACKGROUND

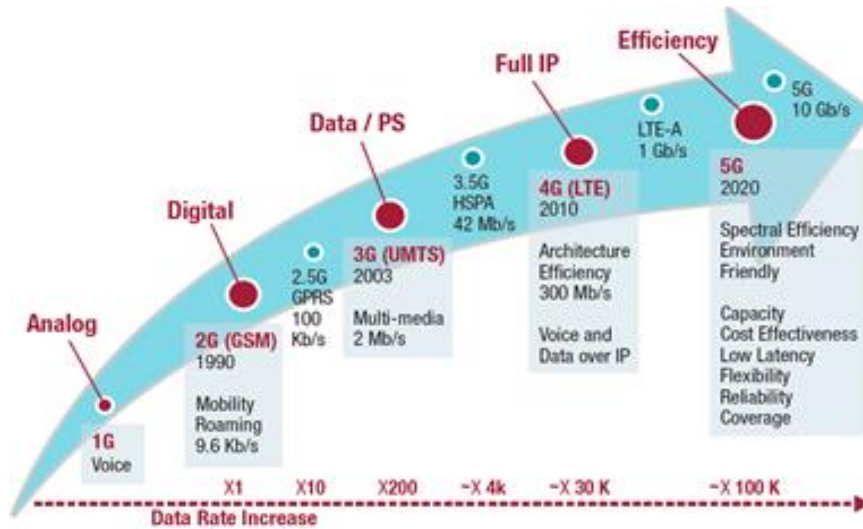


Fig. 1.2: Evolution of mobile communication technologies.

### 1.2.2. The Fifth Generation

The 4G system has been deployed and is reaching maturity. However, with the exponential growth of wireless mobile devices and services, there are still some challenges that can't be accommodated even by the 4G, such as spectrum crisis and high energy consumption. Therefore, wireless system designers have started the research on the fifth generation of wireless systems that is expected to be deployed beyond 2020 [I.5].

### Near Future Data Usage

Before addressing the 5G specifications, it is necessary to review the evolution that the mobile market will perceive up until 2020. Fig. 1.3 shows the number of mobile subscribers per generation from 1985 to the present day where an exponential growth can be seen. In fact, the number of mobile subscriptions went from 2 billion in 2005 to 8 billion in 2017.

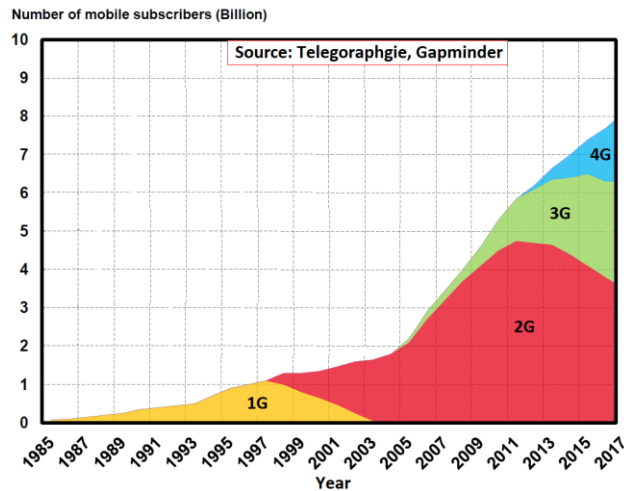


Fig. 1.3: Variation of mobile subscribers with the years.

## CHAPTER I: CONTEXT AND BACKGROUND

This growth is most likely to continue in the next decade. Fig. 1.4 (a) shows the near future data usage according to the Cisco Visual Networking Index (VNI) [1.6]. The overall mobile data traffic is expected to grow to 49 exabytes per month by 2021, a sevenfold increase over 2016. Asia Pacific will account for 46.7 % of global mobile traffic by 2021, the largest share of traffic by any region, followed by Europe (19.3 %) the Middle-East and Africa (15 %), North America (13 %), and Latin America (6 %).

Global mobile data traffic grew an estimated 63 % in 2016. Growth rates varied widely by region (Fig. 1.4 (b)), with Middle-East and Africa having the highest growth rate (96 %) followed by Asia Pacific (71 %), Latin America (66 %), and Central and Eastern Europe (64 %). At the country level, Indonesia, China, and India led global growth at 142, 86, and 76 percent, respectively.

Furthermore, almost half a billion (429 million) mobile devices and connections were added in 2016. Smartphones accounted for most of that growth, followed by Machine-to-Machine (M2M) modules. Moreover, mobile networks carried 400 petabytes per month in 2011, indicating an 18-fold growth of mobile data traffic between 2011 to 2016. This is mainly due to the video traffic which accounted for 60 % of total mobile data traffic in 2016. This trend will continue accounting for 78 % of total mobile data traffic by the end of 2021.

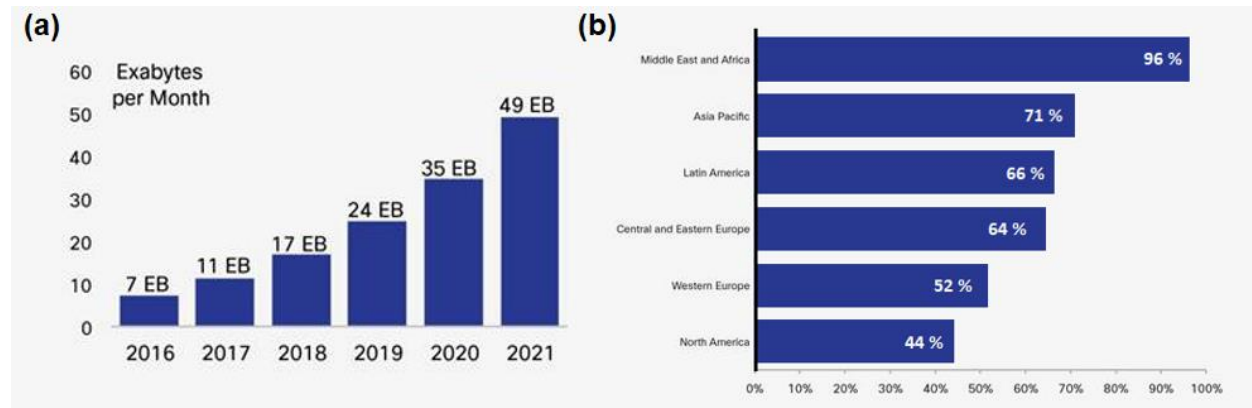


Fig. 1.4: Cisco VNI [1.6] (a) Future data usage (b) Growth of mobile traffic data per region in 2016.

### 5G Applications

Two significant trends are driving the wireless industry to develop the fifth generation:

- The growing increase in demand for wireless broadband services needing faster, higher-capacity networks that can deliver video and other content-rich services.
- The Internet of Things (IoT) that is driving a need for massive connectivity of devices, and also a need for ultrareliable, ultra-low-latency connectivity over internet protocols.

Therefore, a number of distinct applications can be identified:

- Mobile broadband.
- Smart city and smart homes applications.
- Industrial automation and utility applications.
- Vehicle-to-vehicle and vehicle-to-infrastructure transportation systems.
- Wireless health services.
- Virtual and augmented reality services.

## CHAPTER I: CONTEXT AND BACKGROUND

### 5G Specifications

According to the International Telecommunication Union (ITU) report [I.7], the technical requirements for the 5G include:

**Data rate:** The specification calls for at least 20 Gb/s downlink and 10 Gb/s uplink per mobile base station. This is the total amount of traffic that can be handled by a single cell. In theory, fixed wireless broadband users might get speeds close to this with 5G, if they have a dedicated point-to-point connection.

**Connection density:** 5G must support at least 1 million connected devices per square kilometer. This specification is aimed for the Internet of Things applications.

**Mobility:** 5G specification calls for base stations that can support users in high speed vehicles. The specification indicates that different physical locations will need different cell setups.

**Energy efficiency:** The radio interfaces must be energy efficient when under load, but also drop into a low energy mode quickly when not in use. To enable this, the 5G radio should switch from full-speed to battery-efficient states within few milliseconds.

**Latency:** 5G networks should offer users a maximum latency of just 4 ms, down from about 20 ms on 4G cells. The 5G specifications also calls for a latency of just 1 ms for Ultra-Reliable Low Latency Communications (URLLC).

**Spectral efficiency:** The peak spectral efficiency required is at 30 bits/Hz downlink and 15 bits/Hz uplink.

**Reliability:** Data packets should get to the base station within 1 ms, and the interruption time when moving between 5G cells must be instantaneous with no drop-outs.

As no standard will be available until 2019, these specifications will be subject to change. But once installed, the 5G networks will address the need for greater capacity and new services by providing high-speed data transmission, support for a large number of connected devices, low latency, low power consumption and extremely high reliability.

### 5G Technological Solutions

To increase network coverage and data rates, network ultra-densification is necessary, corresponding to an increase in active nodes per zone and frequency. The use of small-cells [I.8] in addition to macro-cells as well as the use of backhaul techniques [I.9] are possible solutions and present in the literature. Also, the use of dynamic allocation of frequency according to application and environment is the concept behind cognitive radio [I.10] allowing better use of spectrum and available resources.

The improvement in spectral efficiency, i.e. the number of bits transmitted per second per hertz, is also important. The use of massive MIMO systems [I.11], based on the MIMO concept already used for Wi-Fi or 3G, is a solution to improve spectral efficiency. The latency time can be improved by bringing the communicating cells closer, thanks to the ultra-densification of the network and the backhaul. OFDM modulation, widely adopted by 4G, is favored for the development of 5G, but some limitations that could affect latency, among other things, lead to thinking about potential alternatives [I.12]. Finally, reducing the energy consumption of the network will not be possible without the use of energy-saving systems.

**5G Frequency of Operation**

The high data rates specification of the 5G is only achievable throughout increasing transmission bandwidth significantly. While the current 4G maximum bandwidth is 100 MHz, the 5G signal bandwidth must be in the order of GHz. This bandwidth is only available in frequencies above 6 GHz.

The radio spectrum regulations are coordinated by the ITU. Currently, the ITU is aiming to harmonize frequency regulation worldwide. However, different parts of the world are using the available radio spectrum in different way and global harmonization is a challenging task.

Three regions are defined by the ITU as shown in Fig. 1.5. In the World Radio Conference 2015 which took place in Geneva, the 5G frequency candidates were discussed for the first time. Each region submitted proposals, and the congress concluded with a list of frequency bands for 5G standardization [1.5].



Fig. 1.5: The three ITU regions.

The 5G will use the frequency bands below 6 GHz used in the current standards. But in order to achieve the demanded high data rates, the research is directed towards the millimeter waves.

Fig. 1.6 shows the frequency bands candidates above 6 GHz proposed by each ITU region with the final selected frequency candidates to be studied for 5G. These bands present large bandwidth allowing high data rates. Nevertheless, the link budget decreases with higher frequencies.

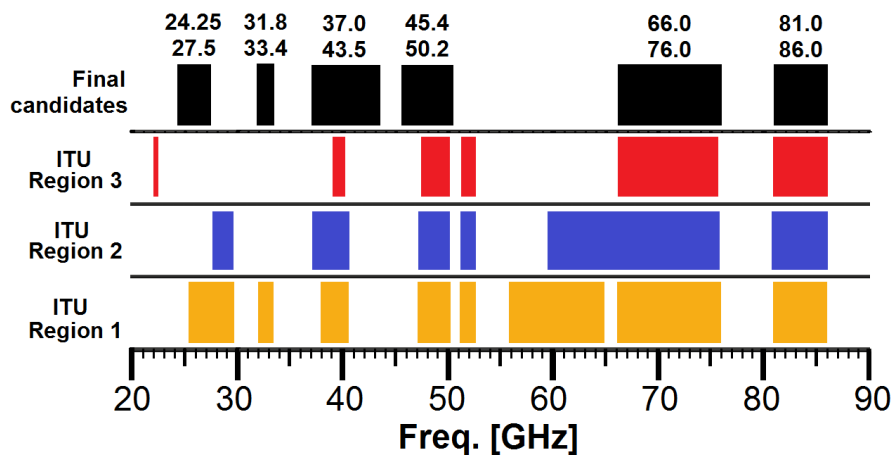


Fig. 1.6: The 5G frequency candidates above 6 GHz.

## CHAPTER I: CONTEXT AND BACKGROUND

Fig. 1.7 shows the sea level atmospheric attenuation for frequencies above 10 GHz. This figure shows the advantage of the first two frequency candidates for the 5G (i.e. 24.25 – 27.5 GHz and 31.8 – 33.4 GHz) where the atmospheric attenuation more than 10 times lower than the other candidates.

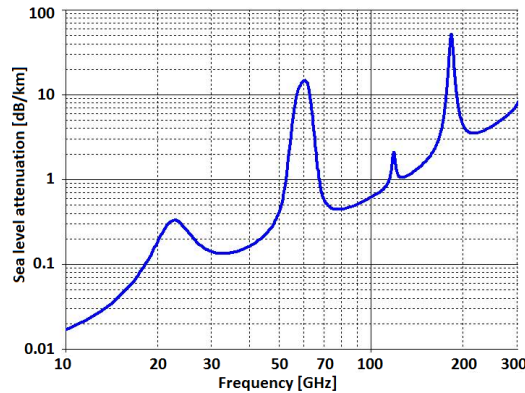


Fig. 1.7: Sea level atmospheric attenuation (10 – 300 GHz).

### 1.3. Radiofrequency Transmitters

After presenting the wireless standards, in this section we briefly present the core of the wireless systems, the transmitters. The transmitters main purpose is radio communication of information over a distance. Information to be transmitted is attached to a sinusoidal carrier signal by modulating the carrier amplitude, frequency, or phase either analogically or digitally. The two basic transmitter architectures homodyne and heterodyne are presented below [I.13].

#### 1.3.1. Homodyne Transmitters

Homodyne transmitters are characterized by direct frequency conversion from baseband to the desired radiofrequency (RF). The block diagram is shown in Fig. 1.8 where the orthogonal components I and Q are considered to be already modulated either by analog or digital means. The mixers are responsible for frequency conversion and the power amplifier is mainly responsible of amplifying the signal.

One of the recurrent problems of this structure concerns the pulling phenomenon of the oscillator [I.14]. In fact, the amplifier and the oscillator operate at close frequencies and can be coupled via the substrate. Since the output power of the amplifier is much greater than that of the oscillator, the latter is shifted in frequency. These two blocks must therefore not be next to each other although it is almost impossible to completely eliminate the coupling.

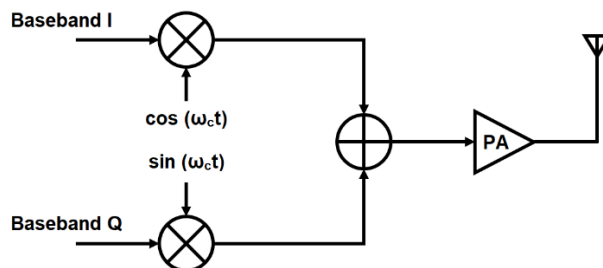


Fig. 1.8: Simplified homodyne transmitter block diagram.

## CHAPTER I: CONTEXT AND BACKGROUND

### 1.3.2. Heterodyne Transmitters

This transmitter structure is the most used and is illustrated in Fig. 1.9. The baseband signal is translated into an Intermediate Frequency (IF) and then into the RF carrier frequency. Because of the different frequencies among the modulated RF signal generated by the amplifier and all the oscillators in the system, the problem of leakage is mitigated. The signal still leaks but it causes negligible effects. However, the solution for the leakage comes at the expense of a larger complexity and power consumption as more blocks are needed in this system.

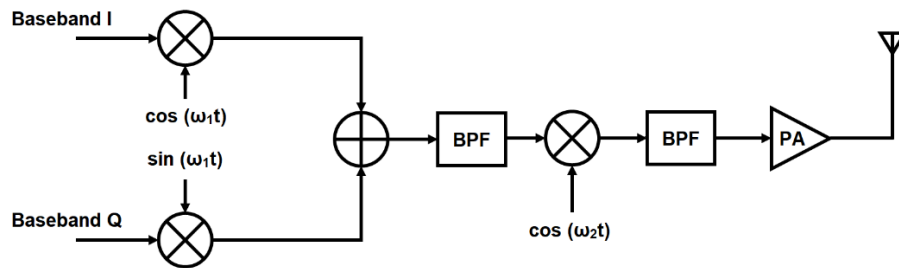


Fig. 1.9: Simplified heterodyne transmitter block diagram.

### 1.3.3. Power Amplifiers in Transmitters

The Power Amplifier (PA) is the most critical element in a transmitter. In fact, the main purpose of a transmitter is to produce a signal that have enough power, a very accurate frequency range, and has a clean enough spectrum so that it does not disturb users of other radio systems. As seen in the two subsections above, the power amplifier is often the last stage of the transmitter before the antenna. Therefore, the performances of the PA are critical for the transmitter. PA Design goals often include gain, power output, bandwidth, power efficiency, linearity, input and output impedance matching, and heat dissipation.

In addition, the power amplifier is the most power consuming element in a transceiver. Fig. 1.10 shows the power consumption breakdown of a 4G smartphone at the maximum transmission power of 23 dBm where the PA consumes 44 % far higher than other components. This power consumption issue is a major problem in the communication systems as it affects critical aspects such as battery cost, weight of power supplies, electrical power expenses, operational time and size of cooling systems and consequently have a significant impact on the environment.

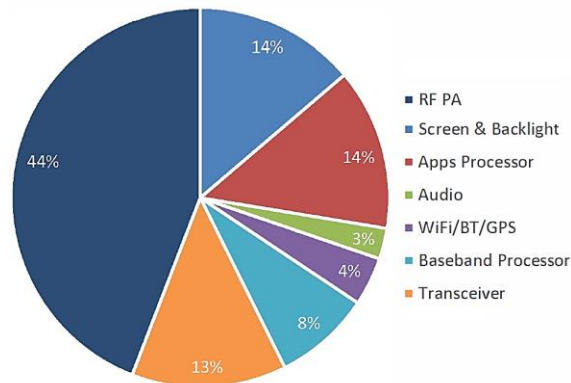


Fig. 1.10: Power consumption breakdown of a 4G smartphone [I.15].

## 2. Power Amplifiers Bibliographic Review

### 2.1. Definitions and General Principles

The design of power amplifiers requires taking into account several parameters characterizing the operation of the circuit. These parameters serve as figures of merit and will allow the comparison of the performance of the PA with the state of the art. The main parameters include the output power, linearity, efficiency, gain, stability, bandwidth and the occupied area.

#### 2.1.1. Output Power

As the name suggests, the essential job of a power amplifier is to increase the power level of the input power applied, without altering the content of the applied signal. The output power of a PA is defined as the active real power delivered into the antenna load at the operation frequency. In the antenna, the electrical power is then dissipated under the form of a radiated electromagnetic wave.

Fig. 1.11 illustrates the input and output power paths in a generic amplifier. Where  $E_S$  is assumed to be an RF source delivering a signal at a frequency  $f_0$ .

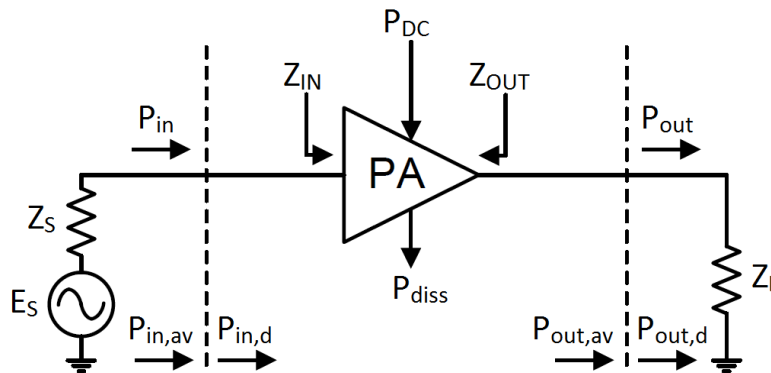


Fig. 1.11: Characteristic parameters of a PA.

with

$P_{in}$	Input power of the PA
$P_{out}$	Output power of the PA
$P_{in,av}$	Power available from the source
$P_{in,d}$	Power delivered to the amplifier
$P_{out,av}$	Power available from the amplifier
$P_{out,d}$	Power delivered to the load
$P_{DC}$	DC power supplied to the amplifier
$P_{diss}$	Power dissipated by the amplifier
$Z_S$	Source impedance of the generator
$Z_L$	Load impedance of the PA
$Z_{in}$	Input impedance of the PA
$Z_{out}$	Output impedance of the PA

## CHAPTER I: CONTEXT AND BACKGROUND

### 2.1.2. Gain

The power gain of a two-port network, amplifier in our study, is defined as the ratio of the output power to input power. Several reflections are present due to mismatching problems while the signal passes through the PA from the generator to the load. This phenomenon has power gain penalties and leads to different gain definitions:

$$\text{Transducer gain} \quad G_T = \frac{P_{out,d}}{P_{in,av}} \quad (1.1)$$

$$\text{Available gain} \quad G_A = \frac{P_{out,av}}{P_{in,av}} \quad (1.2)$$

$$\text{Operating gain} \quad G_P = \frac{P_{out,d}}{P_{in,d}} \quad (1.3)$$

The delivered power differs from the available power because of matching imperfections. Assuming that the matching is perfectly realized:

$$P_{in,av} = P_{in,d}$$

$$P_{out,av} = P_{out,d}$$

The transducer gain is the most used in the design of RF power amplifiers, since it is easily measurable and takes into account input and output mismatches. Consequently, the shortened term “gain” is used with the intended meaning of “transducer gain”. The other gain definitions are used in small signal domain to analyze the stability and matching network losses.

### 2.1.3. Efficiency

The PA efficiency characterizes how much of the Direct Current (DC) power supply energy is converted into the RF signal. The efficiency of a PA should be as high as possible in order to make the PA consume less power. As mentioned earlier, the efficiency affects critical aspects of communication systems such as battery cost, electrical power expenses, weight of power supplies, operational time and size of cooling systems.

There are two main definitions of efficiency:

The Drain Efficiency ( $\eta_d$  or DE) is the ratio of output power to the consumed power:

$$\eta_d = DE = \frac{P_{out}}{P_{DC}} \quad (1.4)$$

And the Power Added Efficiency (PAE) is the ratio between the additional power provided by the PA (the difference between the output power and the input power) and the consumed power ( $P_{DC}$ ):

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \quad (1.5)$$

Using the expression of the transducer gain, it can be shown that:

$$PAE = \eta_d \left(1 - \frac{1}{G_T}\right) \quad (1.6)$$



## CHAPTER I: CONTEXT AND BACKGROUND

Consequently, when the transducer gain increases, the PAE will tend to a maximum which is the drain efficiency. The PAE expression is much more used than the  $\eta_d$  because it takes into consideration the input power.

### 2.1.4. Linearity

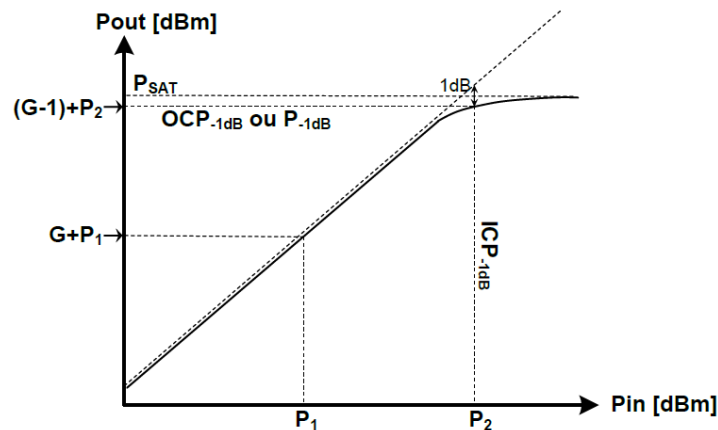
Linearity transcribes the ability of a PA to amplify an input signal with minimal distortion. This parameter imposes a trade-off with the efficiency.

The first step in designing an amplifier is to apply a sine signal to the input while performing a power sweep ( $P_{in}$ ) as shown in Fig. 1.12. In linear operation, the output power is proportional to the input power of a gain factor  $G$ :

$$P_{out} [dBm] = G [dB] \times P_{in} [dBm] \quad (1.7)$$

Non-linear operation occurs when gain  $G$  begins to decrease.

The 1 dB compression point (CP1) is one of the major features to characterize the linearity of a PA. By definition, the CP1 of a PA is the output power level, at which the transfer characteristic of the PA deviates from the ideal linear transfer characteristic by 1 dB. The higher the input 1 dB compression point (ICP1) is, the more linear the PA is.

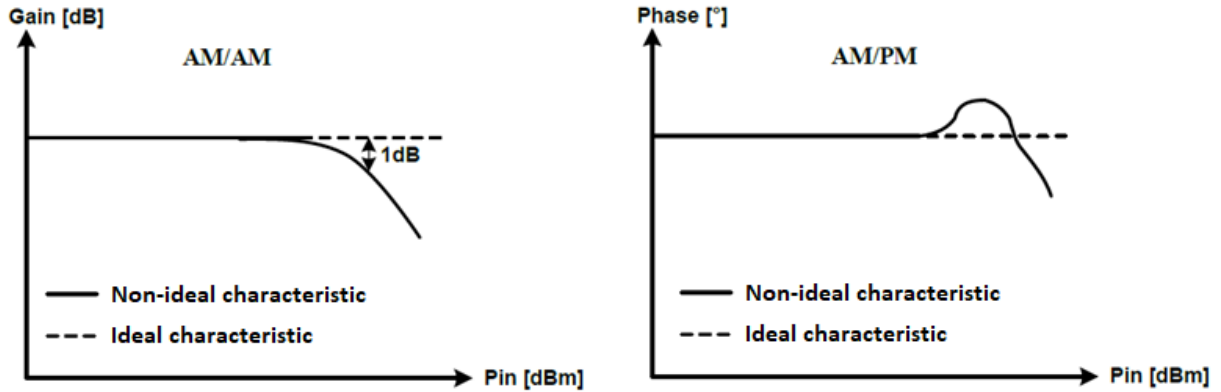


*Fig. 1.12: Output power in function of the input power of a sine signal.*

In terms of gain (Fig. 1.13), the CP1 is the PA power level at which the gain decreases by 1 dB with respect to the gain in the linear region. These amplitude non-linearities can also be referred to as AM/AM gain conversion. By plotting the phase of the output signal as a function of the input power, a second non-linearity characteristic of the amplifier is highlighted: AM/PM amplitude-phase conversion.

The non-linearities create a distortion of the signal, which affects the EVM (Error Vector Magnitude) and the Adjacent Channel Leakage Ratio (ACLR), parameters used in complex modulation signals.

## CHAPTER I: CONTEXT AND BACKGROUND



*Fig. 1.13: AM/AM and AM/PM conversions.*

### 2.2. Power Amplifier Architectures

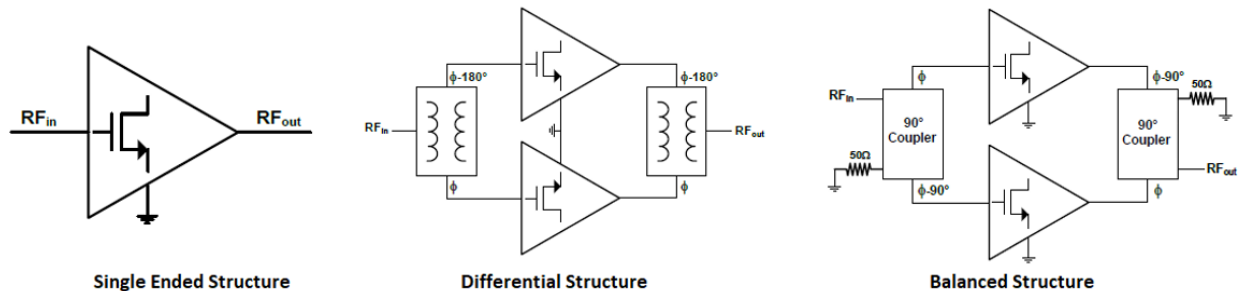
#### 2.2.1. Power Amplifier Structures

Several PA architectures have been reported in the literature. They can be classified into three categories: single-ended, differential, and balanced (Fig. 1.14).

**Single-ended structure:** Most PAs have been designed as a cascade of single-ended stages. Two reasons account for this choice: the antenna is typically single-ended and single-ended RF circuits are much easier to test than their differential counterparts. On the other hand, the performance and the stability of this structure are sensitive to the ground return path which must be perfectly mastered.

**Differential structure:** This structure requires dividing and combining two channels  $180^\circ$  out of phase with baluns (BALanced to UNbalanced). At millimeter frequencies, these baluns can be implemented as integrated transformers, thus acting as a conversion mode and impedance matching circuits. This structure has the advantage of being less sensitive to the ground return path.

**Balanced structure:** In this structure, the input signal is fed through a quadrature coupler and equally divided and injected into the inputs of two parallel amplifiers. The amplified signal at the output of each amplifier is then combined by a quadrature coupler.



*Fig. 1.14: Power amplifier structures.*

### 2.2.2. Power Amplifier Topologies

There are two basic topologies in the PA design: the common source and the cascode (Fig. 1.15).

**Common source topology:** This topology has fewer components and occupies smaller area. A common source transistor has a low power gain, low stability and a low output impedance [I.13]. The  $C_{GD}$  capacitance acts as a feedback loop and degrades the isolation and the gain. The capacitance  $C_{DS}$  increases with the size of the transistor and consequently reduces the output impedance. A particular attention must be paid to the routing in order to minimize these parasitic capacitances. However, this structure allows a high efficiency and linearity.

**Cascode topology:** By stacking transistors, it is possible to provide higher supply voltage levels  $V_{DD}$  allowing higher output power levels. The cascode structure presents a better gain and stability than the common source structure [I.13]. In addition, the cascode topology presents better isolation. This circuit is, on the other hand, much more sensitive to parasitics, in particular those related to the connection between the two transistors.

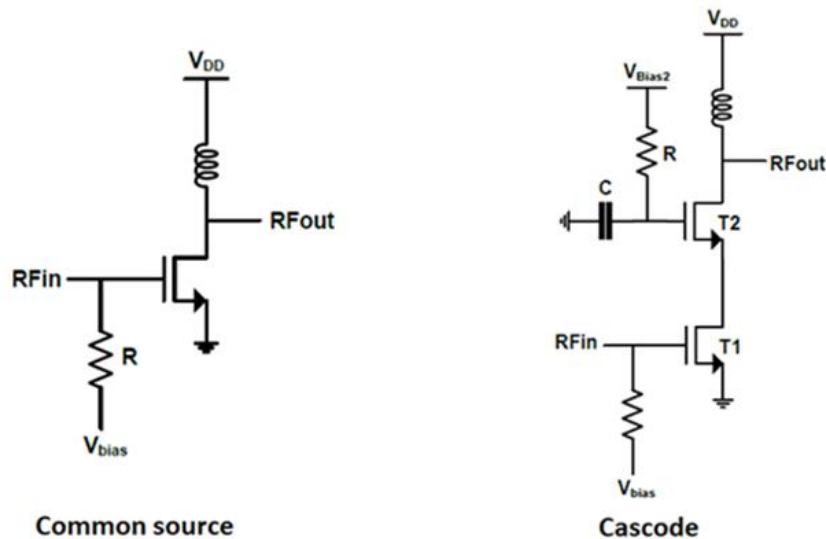


Fig. 1.15: Power amplifier topologies.

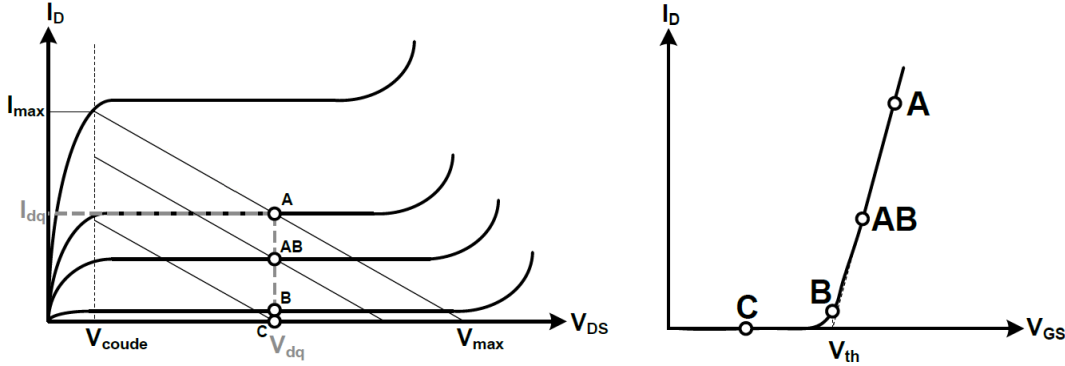
### 2.3. Power Amplifier Classes

The PAs are identified by their operating classes that depend on the relationship between the input signal and the output signal. These operating classes are distinguished both by the biasing applied to the transistor and by the matching circuits processing the harmonics of the signals. In the next three subsections, the sinusoidal classes A, B, AB and C, and switched classes D, E and waveform engineering classes F and J, are presented.

#### 2.3.1. Sinusoidal Classes

The sinusoidal classes are suitable for amplifiers requiring high linearity. The transistor acts as a current source and the output power is proportional to the input power.

## CHAPTER I: CONTEXT AND BACKGROUND



*Fig. 1.16: Power amplifier sinusoidal classes biasing points.*

### Class A

In class A, the active device is conducting at all times for a full cycle ( $360^\circ$ ) of the input sinusoidal signal. In this case the quiescent point (Fig. 1.16) is selected approximately at the center of the device current and the linear output power is maximized by properly selecting the load match. The class A amplifier is designed essentially in the same manner as a small-signal linear amplifier and has the same characteristics in that the output signal is an amplified replica of the input signal. The theoretical efficiency of a class A is 50 % (eq. 1.8).

$$\eta_{classA} = \frac{P_{out,ClassA}}{P_{DC}} = \frac{\frac{1}{4} (V_{DD} - V_K) I_{max}}{\frac{1}{2} V_{DD} I_{max}} = 50 \% \quad (1.8)$$

With  $V_{DD}$  the supply voltage,  $V_K$  the knee voltage and  $I_{max}$  the maximum drain current.

### Class B

In this class the biasing point is set at the cutoff of the device current and the active device conducts only for one half-cycle, that is,  $180^\circ$  of the input sinusoidal signal. In this case the load match is designed to obtain the best gain, maximum output power, and maximum efficiency. However, class B amplifiers have lower linearity performance than the class A PAs. The theoretical efficiency of a class B is 78.5 % (eq. 1.9).

$$\eta_{classB} = \frac{P_{out,ClassB}}{P_{DC}} = \frac{\frac{1}{4} (V_{DD} - V_K) I_{max}}{\frac{\pi}{V_{DD} I_{max}}} = 78.5 \% \quad (1.9)$$

### Class AB

In class AB, the device bias conditions are chosen somewhat in between the class A and class B operations. In this case the biasing current is between 5 and 30 % of the total device current depending on the frequency of operation, noise figure, efficiency, and linearity requirements. This class is commonly used in single-ended power amplifiers and has greater efficiency than class A and better linearity than class B. The theoretical efficiency of a class AB is between 50 % and 78.5 % (eq. 1.10).

## CHAPTER I: CONTEXT AND BACKGROUND

$$\eta_{classAB} = \frac{P_{out,classAB}}{P_{DC}} = \frac{1}{2} \frac{V_{DD} - V_K}{V_{DD}} \frac{\theta - \sin \theta}{2 \sin(\theta/2) - \theta \cos(\theta/2)} \quad (1.10)$$

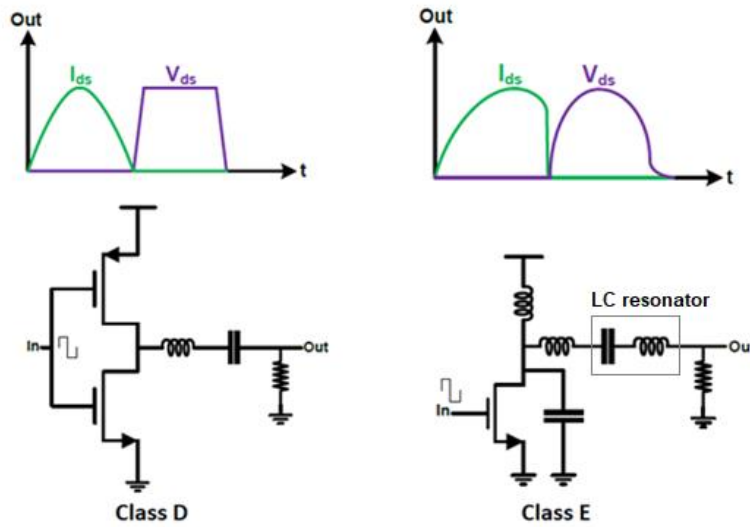
With  $\theta$  being the conduction angle whose value is between  $\pi$  (class B) and  $2\pi$  (class A).

### Class C

In a class C amplifier, the biasing point is set well below the cutoff point of the device current. In this case the device conducts over 25 to 45 % of the RF cycle, and only some portion of the positive half of the sine wave is actually amplified at the output, which is similar to an impulse function. These amplifiers are very nonlinear because the output waveform is very different from the input signal. Since the device is turned on for less than half a cycle, the efficiency of this class is higher than class A, B, or AB, that is, the theoretical drain efficiency is higher than 78.5 %.

### 2.3.2. Switching Classes

The switching operating classes allows to optimize the efficiency with power transistors used as switches. Unlike sinusoidal classes where the input is a sinusoid, the input of the switching classes is a square wave. These classes are preferred for constant envelope amplification for which there's no linearity constraint.



*Fig. 1.17: Class D and E waveforms and schematics.*

### Class D

The class D amplifier is composed of two transistors that conduct current alternately leading to minimize the power consumed (Fig. 1.17). LC resonators are associated with these switches in order to retrieve the fundamental frequency at the load and eliminate the harmonics. Since the output current and voltage waveforms do not overlap, a theoretical efficiency of 100 % can be achieved.

$$\eta_{classD} = \frac{P_{out,classD}}{P_{DC}} = \frac{\frac{1}{\pi} V_{DD} I_{max}}{\frac{1}{\pi} V_{DD} I_{max}} = 100 \% \quad (1.11)$$

## CHAPTER I: CONTEXT AND BACKGROUND

This class is functional only at very low frequency where the impact of the parasitic drain capacitance of the transistors is negligible. In fact, in addition to the fact that the power dissipated during the charging of this capacitance increases with frequency, the waveforms are distorted and an overlap between the current and the drain voltage appears.

### Class E

In class E amplifiers (Fig. 1.17), the transistor works as a switch with two working cycles. In fact, the transistor is controlled by a square wave voltage at the gate allowing current flow only when the drain voltage is zero. An LC resonator is generally used so that the load impedance is only seen at the fundamental frequency. For the other harmonics, only the parasitic drain capacitance is seen. Thus, this class has the advantage of absorbing the drain capacitance through its output matching network [1.16]. In addition, an inductance is introduced at the output of the transistor in order to decrease the voltage and current waves overlapping thus increasing the efficiency of the amplifier to a theoretical maximum of 100 %.

### 2.3.3. Waveform Engineering Classes

Similarly to the sinusoidal classes, the input of the waveform engineering classes is a sinusoidal wave. These classes however, use impedance networks in order to shape the output waveforms of an amplifier and thus enhance the performances.

### Class F

The class F amplifier (Fig. 1.18) is biased as a Class B circuit. The output matching network consists of resonators to recover odd harmonics and generate a square output voltage. These resonators must be placed in series in order to present an open circuit to the transistor for the odd harmonics and to absorb the even harmonics. The area of overlap between the voltage and the drain current is thus reduced and the efficiency can be improved above 78.5 % with a theoretical maximum of 100 %. However, the efficiency is easily reduced due to the drain parasitic capacitance and the numerous filters required that introduce significant insertion losses.

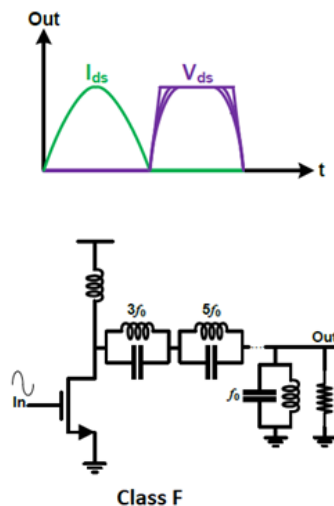


Fig. 1.18: Class F waveform and schematic.

## CHAPTER I: CONTEXT AND BACKGROUND

### Class J

The class J has been presented in 2006 [I.17] as a mode of operation where both intrinsic drain voltage and current waveforms are theoretically half-wave rectified sinusoidal waves. The drain current is obtained by choosing a class B bias point. To obtain the half-wave rectified sine drain voltage, a complex inductive load is presented at the fundamental frequency, and a pure capacitive load impedance is presented at the second harmonic. In fact, these fundamental and second harmonic impedances render a phase shift and boost the drain source voltage across the transistor to shape the waveform as shown in Fig. 1.19.

Consequently, the slight overlapping of the drain voltage and current waveforms makes the amplifier highly efficient, and the non-switch mode of operation makes the class J PA as linear as the class AB [I.17]. In addition, the absence of harmonic impedance terminations and traps, makes it potentially broadband.

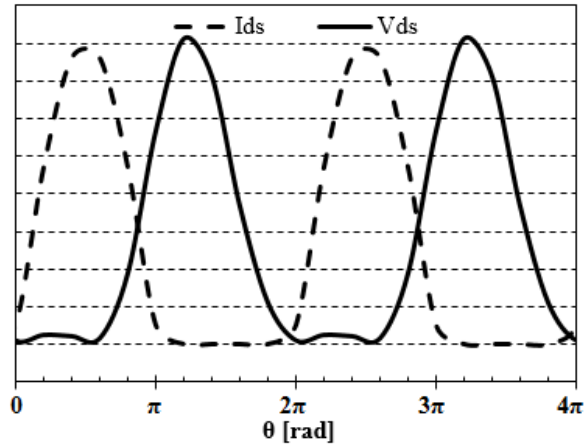


Fig. 1.19: Typical class J amplifier drain source current and voltage waveforms.

Therefore, dividing the expression of the half-wave rectified sine voltage over the half-wave rectified sine current, will lead us to obtain the harmonic composition of the output load impedance:

$$Z_{f_0} = R_{opt} + j R_{opt} \quad (1.12)$$

$$Z_{2f_0} = 0 - j \frac{3\pi}{8} R_{opt} \quad (1.13)$$

$$Z_{>2f_0} = 0 \quad (1.14)$$

Where  $R_{opt}$  is the fundamental load-line resistance.

The class J mode of operation and its design are presented extensively in Chapter III.

## 2.4. Impedance Matching

Impedance matching is one of the most important concepts in amplifier design in order to maximize the power transfer and performances. In this section, we present the conjugate matching and the load-pull matching techniques.

### 2.4.1. Conjugate Matching

When the dimensions of the circuit are no longer small compared to the wavelength, the propagation of the electrical signal introduces the notion of incident signal and reflected signal [I.1].

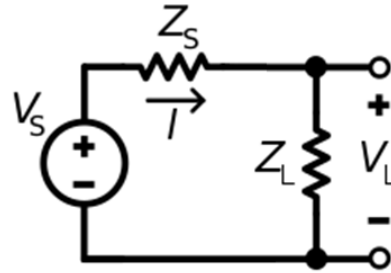


Fig. 1.20: Source and load impedances.

According to Fig. 1.20, the power delivered to the load is given by:

$$P = \frac{1}{2} \operatorname{Re}(V_L \cdot I^*) = \frac{V_S^2}{2} \frac{R_L}{(R_L + R_S)^2 + (X_L + X_S)^2} \quad (1.15)$$

Where  $R_S$ ,  $R_L$  and  $X_S$ ,  $X_L$  are the real and imaginary parts of  $Z_S$  and  $Z_L$  respectively.

Therefore, according to this equation, the generator delivers its maximum power if it is loaded by its conjugate impedance i.e.  $R_L = R_S$  and  $X_L = -X_S$ . The objective of the impedance matching will consequently be to present the conjugate impedance in order to maximize the power transfer.

### 2.4.2. Load-pull Matching

The non-linear circuits characterization method load-pull is based on a simple principle: the component to be tested is considered as a “black box” and no information concerning geometrical or physical characteristics is required.

The Load-pull measurements allow to determine the optimal performances in terms of power, PAE, and gain of the components tested. These measurements consist of studying, for a bias condition, a given frequency and a given input power the behavior of the transistor when the load impedance presented at its output is varied. The load-pull characterization technique is a method that optimizes the operating conditions of transistors, especially when no nonlinear model is available to describe its behavior in an authentic way.

Moreover, this method makes it possible to validate the nonlinear parameters of a model by experimentally verifying the results obtained by the simulation [I.18].



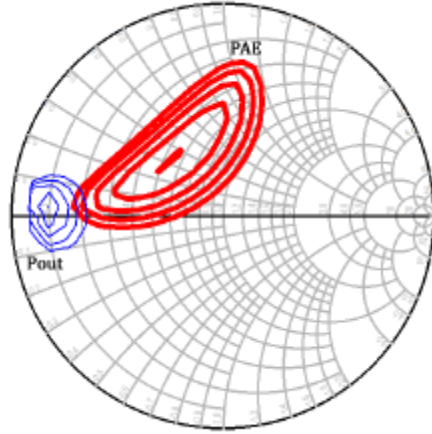


Fig. 1.21: Example of output power and PAE load-pull contours for different impedances.

## 2.5. Combination of stages

In order to obtain larger power gain, a power amplifier may be composed of more than one stage. In the case of having a power amplifier composed by 2 stages, the total gain, in dB, is given by:

$$G_T = G_1 + G_2 \quad (1.16)$$

Where  $G_1$  and  $G_2$  represent the gain of first and second stage respectively, while  $G_T$  is the total gain of the power amplifier.

The PAE of the composite amplifier is given by [1.19]:

$$PAE_T = \frac{\eta_2}{1 + \frac{\eta_2}{\eta_1 \cdot G_1 \cdot G_2}} \quad (1.17)$$

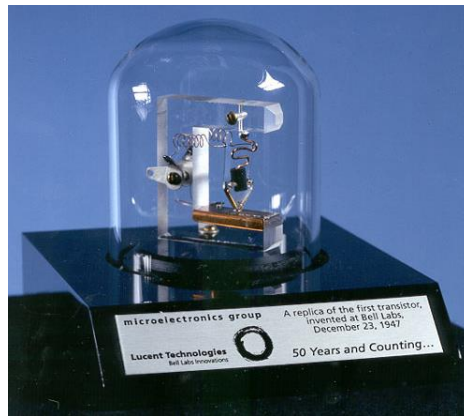
This equation demonstrates that the overall efficiency is dominated by the efficiency of the second stage if the gain of the power amplifier is sufficiently high.

### 3. Transistor Technologies

#### 3.1. A Brief History of Transistors

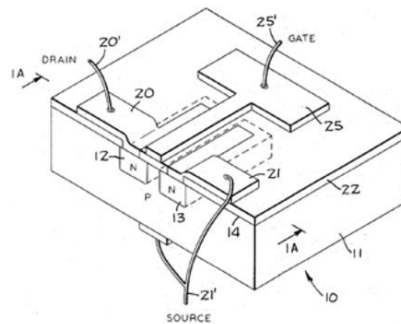
Solid state amplification is dominated by the use of three-terminal transistors (originally named transfer resistor). A transistor is fundamentally a semiconductor device used to amplify or switch electronic signals and electrical power.

The initial step towards solid-state devices was taken in 1874, when German inventor Karl Ferdinand Braun discovered the metal-semiconductor contact. However, it took 51 years after this discovery until the Field-Effect Transistor (FET) was patented by the physicist Julius Edgar Lilienfeld in 1925. Afterwards in 1947, a bipolar transistor device was developed by John Bardeen, Walter Brattain and William Shockley at Bell Labs.



*Fig. 1.22: A replica of the bipolar transistor developed at Bell Labs in 1947.*

The first Integrated Circuit (IC) was developed in 1958 at Texas Instruments. This circuit consisted of a transistor, a capacitor, and resistors on a piece of germanium [I.20]. In the following year Fairchild Semiconductor invented an IC with planar interconnections using photolithography and etching techniques still used today [I.21]. In 1963, the same company developed the Complementary Metal-Oxide-Semiconductor (CMOS) process, which enabled the integration of both NMOS and PMOS transistors on the same chip. The first demonstration circuits were an inverter and a ring-oscillator [I.22].



*Fig. 1.23: CMOS device structure from Fairchild Semiconductor patent.*

### 3.2. Transistor Evolution and Scaling

#### 3.2.1. Moore's Law

In 1975 Gordon Moore, one of Intel's co-founders, predicted that the number of transistors in an IC would double every two years. This prediction became known as "Moore's law" and became a roadmap principle that has emerged as one of the driving principles in the semiconductor industry. In fact, engineers and researchers have been challenged to deliver constant breakthroughs to comply with the trend of evolution.

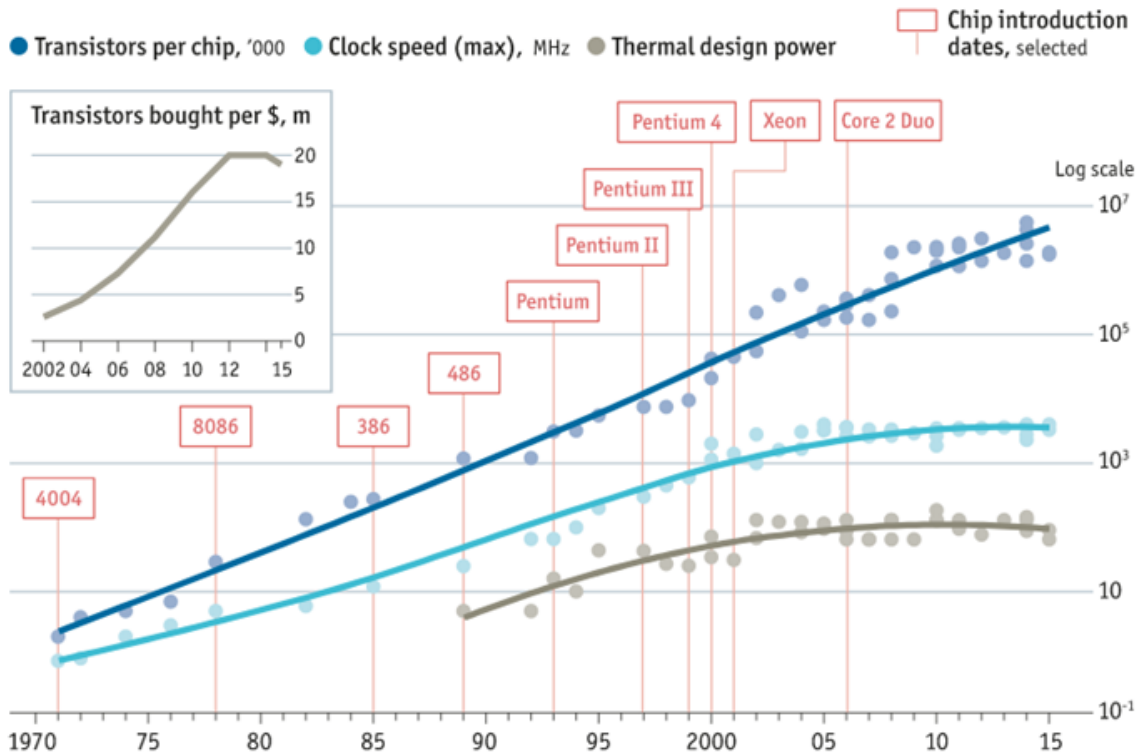


Fig. 1.24: Transistor count, clock speed and thermal design power evolution with the years [1.23].

The fulfilment of this evolution was made possible largely because transistors become faster and less power consuming as their channel length decreases. In fact, as the channel length scales down, a transistor can be turned on and off with less power and at higher speeds. This meant a chip can contain more and faster transistors without needing more power or generating more heat.

However, the scalability of transistors encounters inevitable physical barriers. In fact, as the transistor shrinks, the length of the gate is reduced, the control the gate exercises over the channel region is also reduced, lowering the transistor performances. This is largely due to the leakage current that is not transmitted from the source to the drain of a transistor. The leakage currents are increasing with every new generation of transistors, and represent a growing proportion of power consumption.

Therefore, in order to ensure the evolution of semiconductor electronics in the future, researchers are intensively working on two areas: emerging technologies (new materials), and advanced technologies (new device concepts).

## CHAPTER I: CONTEXT AND BACKGROUND

### 3.2.2. Emerging Technologies

Since its discovery in 2004, graphene, a semimetal (a zero-gap semiconductor), one atom-thick carbon-based material, has generated a significant interest in physics and electronic applications. Its record carrier mobility and unique physical properties (Table 1.1) have motivated many research groups to develop radio frequency Graphene Field-Effect Transistors (GFET). Intrinsic cut-off frequencies ( $f_T$ ) of a few hundreds of GHz [I.24], and intrinsic maximum oscillation frequencies ( $f_{max}$ ) of 106 GHz [I.25] have been achieved so far. However, existing graphene transistors suffer from the lack of an energy bandgap inducing a weak current saturation.

Property	Graphene	Comparison
Current density	$10^{12}$ A/cm <sup>2</sup>	6× higher than copper
Electric conductivity	$0,96 \cdot 10^6$ S/cm	$0.60 \cdot 10^6$ S/cm (copper)
Thermal conductivity	5000 W/m·K	2500 W/m (diamond)
Electron Mobility	$2.105$ cm <sup>2</sup> /V·s	1350 (Silicon)
Breaking force (2D)	42 N/m	0,084 - 0,4 N/m (steel)
Transparency per layer	97.4 %	-

Table 1.1: Graphene properties.

While the first 2D (two dimensional) material to be discovered was graphene, its study has triggered experiments on many other 2D atomic crystals such as BN, NbSe<sub>2</sub>, TaS<sub>2</sub>, MoS<sub>2</sub> and many others. The graphene technology is detailed in the Chapter II.

### 3.2.3. Advanced Technologies

One solution to the problem of the leakage current is to redesign the channel of the transistor. The first design is proposed by Intel in 2012, and it consists on adding a third dimension to the conventional transistor planar structure. These transistors are known as “FinFET”, and feature a channel wrapped by a thin silicon “fin”. Thus, the gate covers the channel’s three exposed sides (Fig. 1.25). This gate structure provides improved electrical control over the channel and reduces leakage currents. Moreover, these devices switch faster and consume less power than planar transistors of the same size. However, these three-dimensional transistors use complex manufacturing processes and thus are more expensive.

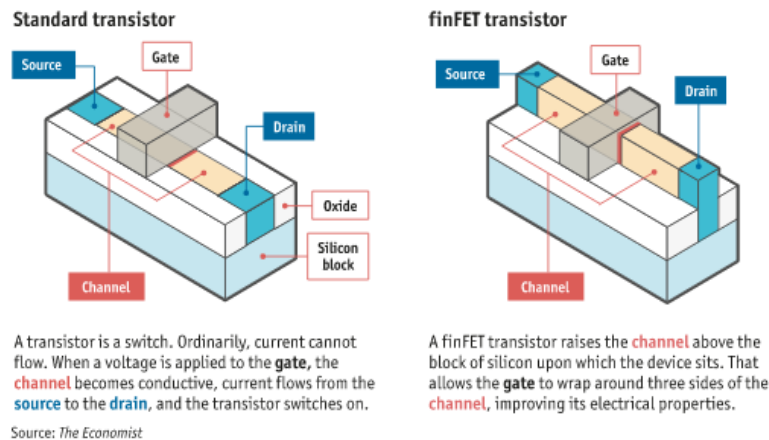


Fig. 1.25: Standard versus FinFET transistor [I.23].

## CHAPTER I: CONTEXT AND BACKGROUND

The other solution is the Fully Depleted Silicon on Insulator (FD-SOI). Unlike FinFETs, the FD-SOI transistor does not change the fundamental geometry of the transistor and thus is less costly while simplifying the manufacturing process. In FD-SOI the innovation lies in the buried oxide insulator layer positioned just below the channel. This layer confines the electron when flowing from the source to the drain, reducing the leakage current from the channel to the substrate. Moreover, this layer eliminates the need to add dopants to the channel, making it fully depleted. Another key feature of this technology is the back-gate who can be biased up to 2 V, lowering the device threshold ( $V_{th}$ ) by 200 mV [I.26] and thus allowing efficient control and reconfigurability of the device. This technology is detailed in Chapter III.

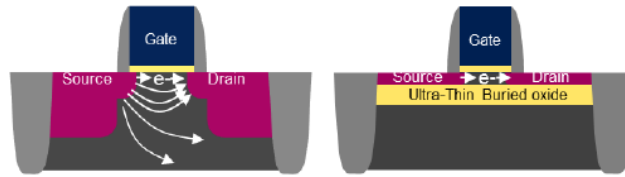


Fig. 1.26: Electron flow in bulk and FD-SOI CMOS transistor.

### 3.3. Transistor Types

The major types of transistors used to develop amplifier circuits are:

- Silicon Bipolar Junction Transistors (BJT).
- Silicon Metal Oxide Semiconductor Field-Effect Transistors (MOSFET).
- Silicon Laterally Diffused Metal Oxide Semiconductor (LDMOS).
- GaAs Metal Semiconductor Field-Effect Transistors (MESFET).
- GaAs, GaN and InP based High Electron Mobility Transistors (HEMT).
- SiGe and GaAs based Heterojunction Bipolar Transistors (HBT).
- Silicon carbide (SiC) based FETs.

Fabrication of transistors starts with the selection of a wafer type or substrate. Various substrate materials used for active devices. Silicon is the dominant substrate, GaAs is a distant second before less mature technologies such as indium phosphide (InP), SiC, and GaN [I.27].

The electrical and physical properties of these substrate are compared in Table 1.2.

Property	Silicon	SiC	GaAs	InP	GaN
Semi-insulating	No	Yes	Yes	Yes	Yes
Resistivity ( $\Omega \cdot \text{cm}$ )	$10^1 - 10^5$	$>10^{10}$	$10^7 - 10^9$	$\sim 10^7$	$>10^{10}$
Dielectric constant	11.7	9.7	12.9	14	8.9
Electron mobility ( $\text{cm}^2/\text{V}\cdot\text{s}$ )	1450	500	8500	4000	800
Saturation velocity ( $\text{cm/s}$ )	$9 \times 10^6$	$2 \times 10^7$	$1.3 \times 10^7$	$1.9 \times 10^7$	$2.3 \times 10^7$
Radiation hardness	Poor	Excellent	Very good	Good	Excellent
Density ( $\text{g/cm}^3$ )	2.3	3.1	5.3	4.8	6.1
Thermal conductivity ( $\text{W/cm}\cdot^\circ\text{C}$ )	1.45	3.5	0.46	0.68	1.3
Operating temperature ( $^\circ\text{C}$ )	250	$>500$	350	300	$>500$
Energy gap (eV)	1.12	2.86	1.42	1.34	3.39
Breakdown field ( $\text{kV/cm}$ )	$\approx 300$	$\geq 2000$	400	500	$\geq 5000$

Table 1.2: Comparison of transistor/IC substrates [I.27].

## CHAPTER I: CONTEXT AND BACKGROUND

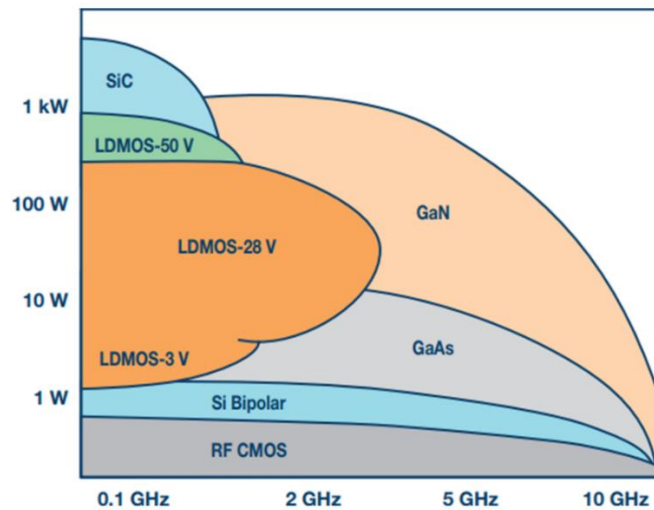
Fig. 1.27 shows the power level versus frequency per process. For high-power and high-temperature applications, wide bandgap materials with relatively high thermal conductivity, such as SiC and GaN (gallium nitride), play a significant role. In fact, recent advancements in epitaxial techniques have made it possible to develop active devices on these substrates. However, until now these processes are costly.

Concerning GaAs (gallium arsenide) devices, their semi-insulating substrates provide isolation up to 100 GHz. In fact, the GaAs FET as a single discrete transistor has widely been used in hybrid microwave integrated circuit amplifiers for broadband, medium-power, high-power, and high-efficiency applications. This wide utilization of GaAs FETs can be attributed to their high frequency of operation and versatility.

Silicon-germanium (SiGe) technology has been evolving over the last two decades. One of the major advantages of SiGe is that it can easily be integrated into standard silicon processes. The performance advantages of SiGe over traditional silicon devices are the high cutoff frequency and the improved power added efficiency at low voltages.

Finally, the LDMOS is an asymmetric power MOSFET designed for higher breakdown voltages in order to achieve higher power levels. These transistors are widely used for base-station RF power amplification. In fact, they are less expensive than GaN and GaAs devices, however, their frequency of operation is lower.

For wide-ranging information on transistor types and technologies refer to [1.27].



*Fig. 1.27: Power level versus frequency per process.*

### Conclusion

With the rising evolution of wireless devices and services, researchers are intensively working on the fifth generation of wireless systems. The demand for high speed data and the need for more spectrum, have motivated the use of millimeter wave carrier frequencies. Thus, the 5G research is faced with an evolving set of challenges.

One of the major challenges of the next generation communication technology is reducing energy consumption. In fact, the efficiency is directly related to the cost, size and reliability of the communication systems. Another key challenge is the wide bandwidth requirement. It is widely known that the radiofrequency power amplifier is the most power consuming component in the radio transceivers, and is also one of the most critical building blocks in radio front-end. Therefore, research in this area is crucial for next generation communication systems.

Besides, the transistor scaling course comes to an end in the near future. Researchers are working on new materials (emerging technologies) and device concepts (advanced technologies) to insure the healthy evolution of semiconductor electronics.

The objective of this chapter was to introduce the context of this thesis and the choices of orientation with regard of the constraints (i.e. research on power amplifier for 5G applications on emerging and advanced technologies).

Consequently, the next two chapters present power amplifier study and design for 5G applications on emerging (Chapter II) and advanced (Chapter III) technologies.

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## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

### Table of Contents

<i>Introduction</i>	54
<i>1. Graphene Physics</i>	55
1.1. <i>Graphene Properties</i>	55
1.2. <i>Graphene Fabrication Methods</i>	56
<i>2. Graphene Field-Effect Transistors</i>	58
2.1. <i>GFET Structure</i>	58
2.2. <i>GFET State of the Art</i>	58
2.3. <i>GFET <math>f_T</math>, <math>f_{max}</math> and Scaling</i>	62
2.4. <i>GFET Contact Resistances</i>	64
2.5. <i>GFET Current Saturation</i>	65
2.6. <i>GFET Process Variability</i>	66
<i>3. State of the Art of Graphene RF Circuits and Amplifiers</i>	67
3.1. <i>State of the Art of Graphene Circuits</i>	67
3.2. <i>State of the Art of Graphene Amplifiers</i>	69
<i>4. Graphene Transistors Properties and Characteristics</i>	71
4.1. <i>GFET with Graphene Synthesized on SiC Substrate</i>	71
4.2. <i>GFET with CVD-grown Graphene on Si/SiO<sub>2</sub> Substrate</i>	72
4.3. <i>GFET with Mechanically Exfoliated Graphene and h-BN Dielectrics</i>	73
<i>5. GFET Compact Model</i>	75
5.1. <i>Model Description</i>	75
5.2. <i>Model Parameters</i>	76
<i>6. Graphene Power Amplifiers Design</i>	78
6.1. <i>GFET with Graphene Synthesized on SiC Substrate PA</i>	80
6.2. <i>GFET with CVD-grown Graphene on Si/SiO<sub>2</sub> Substrate PA</i>	81
6.3. <i>GFET with Mechanically Exfoliated Graphene and h-BN Dielectrics PA</i>	82
<i>7. Post-layout Simulation Results</i>	83
7.1. <i>GFET with Graphene Synthesized on SiC Substrate PA Results</i>	83
7.2. <i>GFET with CVD-grown Graphene on Si/SiO<sub>2</sub> Substrate PA Results</i>	84
7.3. <i>GFET with Mechanically Exfoliated Graphene and h-BN Dielectrics PA Results</i>	84
<i>8. Results Discussion</i>	85
<i>9. Multistage GFET Amplifiers</i>	88
<i>Conclusion</i>	91
<i>References</i>	92

### Introduction

While many research laboratories and companies demonstrated state of the art graphene transistors with high frequency performances, many details about the potential performance of graphene transistors in electronics applications remain unclear. In fact, few graphene circuits and even fewer amplifiers have been demonstrated. Besides, the large signal performances of graphene amplifiers haven't been studied yet, such as the efficiency which has never been reported. Thus, in this chapter we aim to investigate the graphene technology performances not as a single transistor, but as a circuit for radiofrequency power amplification.

This chapter begins with a brief presentation of graphene remarkable physical properties and its methods of fabrication. In the second part, state of the art graphene field-effect transistors are studied and their performances are analyzed. The third part of this chapter is a bibliographic review on graphene based RF circuits and amplifiers.

The fourth part addresses the three graphene transistors, with different fabrication methods and substrates, used in this work for power amplifier design. First, the structure and properties of each transistor are presented. Then, the DC and RF measurement and model parameters are displayed and compared for each transistor. Subsequently, the compact model used for the three transistors is described in the fifth part of this chapter.

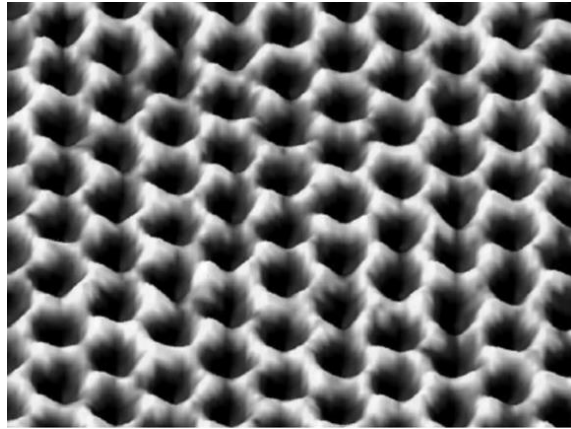
In the sixth part of this chapter, three common source integrated graphene power amplifiers are designed. The design methodology and environment are presented. Then, the layout of each amplifier is described. Afterwards, the seventh part reports the small and large signal results for each amplifier. The results are discussed, compared and evaluated in the eighth part of this chapter. Afterwards, results projections are made with the GFET technological enhancements. Finally, this chapter ends with the design and discussion of multistage graphene amplifiers.

### 1. Graphene Physics

#### 1.1. Graphene Properties

Carbon is the fourth most abundant element in the universe after hydrogen, helium, and oxygen. Many different carbon-based structures can be found in nature (coal, diamond and graphite) or be synthesized due to the flexibility of its bonding. Graphene was first synthesized in 2004 [II.1] by peeling graphite layers with scotch-tapes. Since then, the worldwide research activities on graphene have boomed.

Graphene (Fig. 2.1), is a two-dimensional (one atomic layer thick) hexagonal lattice in which one carbon atom forms each vertex. This material holds a multitude of beneficial physical properties due to its planar structure. These properties are very interesting for wide-ranging fields of applications [II.2], particularly electronics.



*Fig. 2.1: Scanning probe microscopy image of graphene [II.3].*

One of the most remarkable properties of graphene for electronics is its very high carrier mobility at room temperature [II.4]. In the absence of ripples and charged impurities, a carrier mobility in excess of  $2 \times 10^6$   $\text{cm}^2/\text{V}\cdot\text{s}$  has been reported [II.5]. In perspective, carrier mobilities of 77000, 8500 and 1400  $\text{cm}^2/\text{V}\cdot\text{s}$  have been obtained for Indium Antimonide (InSb) [II.6], Si CMOS [II.7] and GaAs [II.8] respectively. In addition, experiments revealed saturation velocities ( $V_{\text{SAT}}$ ) of between  $3 \times 10^7$  and  $6 \times 10^7$   $\text{cm/s}$  for gapless large-area graphene [II.9] [II.10], for Silicon and GaAs,  $V_{\text{SAT}}$  is in the order of  $1 \times 10^7$   $\text{cm/s}$  and  $1.2 \times 10^7$   $\text{cm/s}$  respectively.

Furthermore, graphene holds the record in thermal conductivity with  $5 \times 10^3$   $\text{W/m}\cdot\text{K}$  at room temperature [II.11] 30 times higher than silicon.

Graphene mechanical properties are also unique with a 2D tensile strength of 42  $\text{N/m}$  and a Young's modulus of 1 TPa which allow it to stretch up to 20 % without breaking [II.12]. Additionally, graphene is also nearly optically transparent with 2.3 % of optical absorption for a single layer of graphene [II.13].

On the other hand, while all conventional semiconductors have a sizeable bandgap, natural graphene is a zero-gap material and the missing gap has consequences for the operation of graphene transistors (Fig. 2.2). The most obvious effect is that FETs with gapless channels do not switch off and therefore, are not suited for digital applications. Using narrow graphene nanoribbons (GNRs)

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

[II.14] is one way to open a gap, but preparing GNRs with a defined width of a few nanometers is yet a difficult process. Another method is using bilayer graphene in a dual gate GFET [II.15]. Nevertheless, graphene owns its high mobility due to its gapless structure, thus when opening a gap in graphene the mobility declines rapidly [II.16].

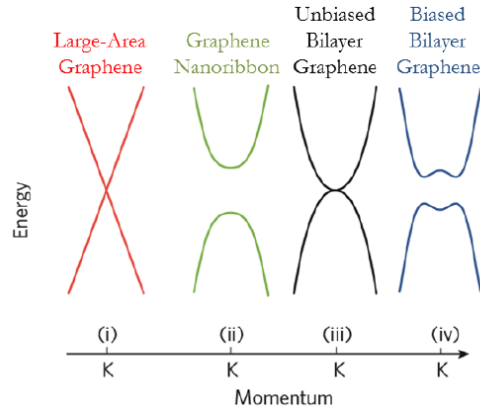


Fig. 2.2: Energy band structure around the first Brillouin zone of large area-graphene, GNR, unbiased and biased bilayer graphene [II.17].

### 1.2. Graphene Fabrication Methods

The market of graphene applications is essentially driven by the progress in the production of graphene with properties appropriate for the specific application, and this situation is likely to continue until each of graphene’s many potential applications meets its own requirements. Currently, there are many methods being used and developed to prepare graphene of various dimensions, shapes and quality. The three most advanced methods for electronic applications are:

- Thermal decomposition on SiC [II.18].
- Chemical Vapor Deposition (CVD) [II.19].
- Mechanical exfoliation [II.20].

Fig. 2.3 presents a classification of the cited graphene preparation methods per quality and price and Table 2.1 summarizes the properties obtained by these methods. For an extensive explanation of these methods of fabrication refer the references cited above and to [II.2].

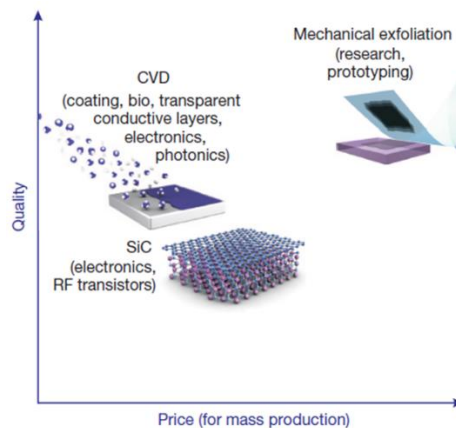


Fig. 2.3: Classification of graphene methods of preparation per quality and price [II.2].

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

So far, the mechanical exfoliation method presents the best graphene quality with a mobility surpassing  $200,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ . However, this method is very costly and is only used for research purposes since the size of the sample is limited (Table 2.1).

The CVD method is one of the most promising methods to produce graphene on an industrial-scale due to its ability to yield high-quality, continuous films over large areas [II.21]. Moreover, it is considered highly suitable for FET application with various substrates [II.22].

The thermal decomposition on SiC method is also promising for producing large samples of good quality graphene. However, this fabrication method requires temperatures higher than  $1,000 \text{ }^\circ\text{C}$ , and SiC wafers are costly, and large size SiC wafers are not available due to the technical limitations of SiC crystal growth.

Despite that the CVD method produces graphene with better quality, the synthesis on SiC method is primarily used for RF electronics, as this method produces transistors with lower contact resistances. However, both of these methods present a current saturation problem, but for different reasons (Fig. 2.4):

- In the thermal decomposition on SiC method, charges are trapped at the graphene/SiC interface. This reduces the layer resistivity but shifts the voltage of the Dirac point which makes saturation difficult to attain.
- Concerning the CVD method, the good-quality graphene is naturally slightly doped, and the Dirac point is centered. On the other hand, this method produces transistors with very high contact resistances which deforms the output network and prevents the current saturation.

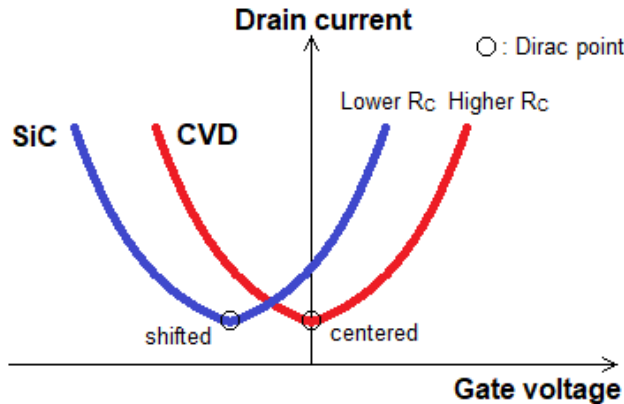


Fig. 2.4: Illustration of the Dirac points of the CVD graphene and the graphene synthesized on SiC.

Method	Crystallite size [ $\mu\text{m}$ ]	Sample size [mm]	Charge carrier mobility [ $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ ]	Applications
Mechanical exfoliation	> 1000	> 1	> 200,000	Research
CVD	1000	~1000	10,000	Photonics, nanoelectronics, transparent conductive layers, sensors, bio applications
Synthesis on SiC	50	100	10,000	High-frequency transistors and other electronic devices

Table 2.1: Graphene properties obtained by different methods [II.2].

## 2. Graphene Field-Effect Transistors

Since the first graphene samples were fabricated, physicists and device engineers raced on designing graphene-based transistors. In this part we present the study and the state of the art of the most advanced graphene transistor type: The Graphene Field-Effect Transistor (GFET).

### 2.1. GFET Structure

Fig. 2.5 shows a cross sectional view of a single-gate GFET structure. Basically, the GFET has the same structure as a typical MOSFET. The difference is that instead of silicon the channel is made of graphene. A graphene field-effect transistor is constructed from the substrate, the graphene channel, the dielectric layer and the source, drain and gate electrodes.

The graphene channel can be a single graphene layer, bilayer graphene, few layer graphene or graphene nanoribbon. The characteristics of the GFET differ greatly with different graphene channel. For instance, single and few layer graphene are semi-metals and have no band gap, and bilayer and GNR have a band gap. In this work, we focus on the monolayer GFET as it is the most studied and advanced type of graphene transistors.

Finally, it is worth to be noted that the two gate-finger structure is mostly used for RF measurements due to the symmetry of the device which minimizes the effects of parasitic capacitances.

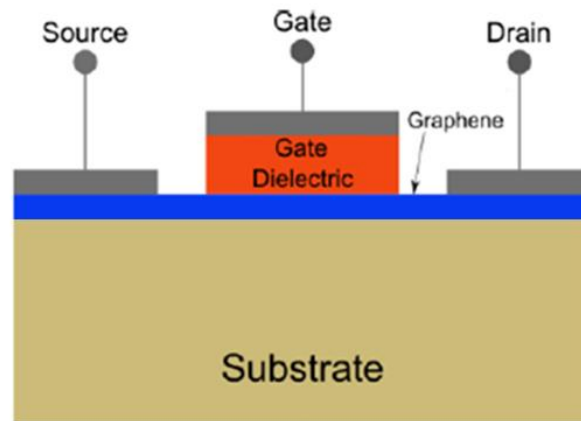


Fig. 2.5: Cross sectional view of a GFET structure.

### 2.2. GFET State of the Art

The electric field-effect in graphene devices was first demonstrated in 2004 by two different groups (from Manchester University [II.1] and Georgia Institute of Technology [II.23]) within few months of each other. In [II.1], the graphene flake was mechanically exfoliated on top of a highly doped silicon wafer with SiO<sub>2</sub> acting as gate oxide. Afterwards, metal contacts (source and drain contacts) were placed on the flake of graphene.

The first demonstrated GFET device (Fig. 2.6 (a)) was reported in 2007 by Lemme et al. [II.24], using the same method of fabrication described above. This pioneering work presented the current-voltage characteristics (Fig. 2.6 (b)), demonstrating the impressive potential of graphene for future electronic devices, and thus initiated the research and engineering of graphene transistors.



## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

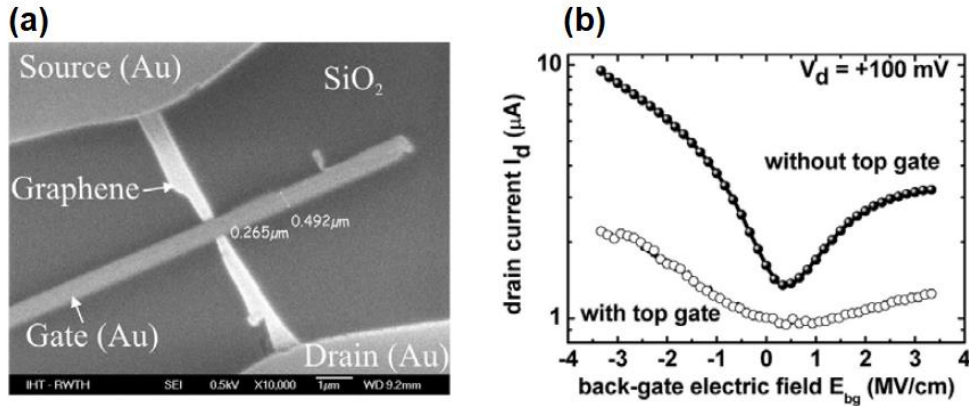


Fig. 2.6: The first demonstrated GFET [II.24] (a) SEM image (b) Transfer characteristic.

Since the gapless channel hinders graphene transistor potential in digital applications, enormous efforts have been carried out in order to inspect the properties of graphene in high frequency applications, and many research groups began to develop radio frequency graphene field-effect transistors [II.25 – II.30].

In 2010, the cut-off frequency ( $f_T$ ) of GFET devices surpassed 100 GHz [II.31]. In this publication, a team from IBM succeeded in fabricating high-frequency transistors, with gate lengths as low as 240 nm, from wafer-scale graphene using the thermal decomposition on SiC substrate. As Fig. 2.7 (b) and (c) show, the Dirac point is shifted and these devices don't show a distinct current saturation.

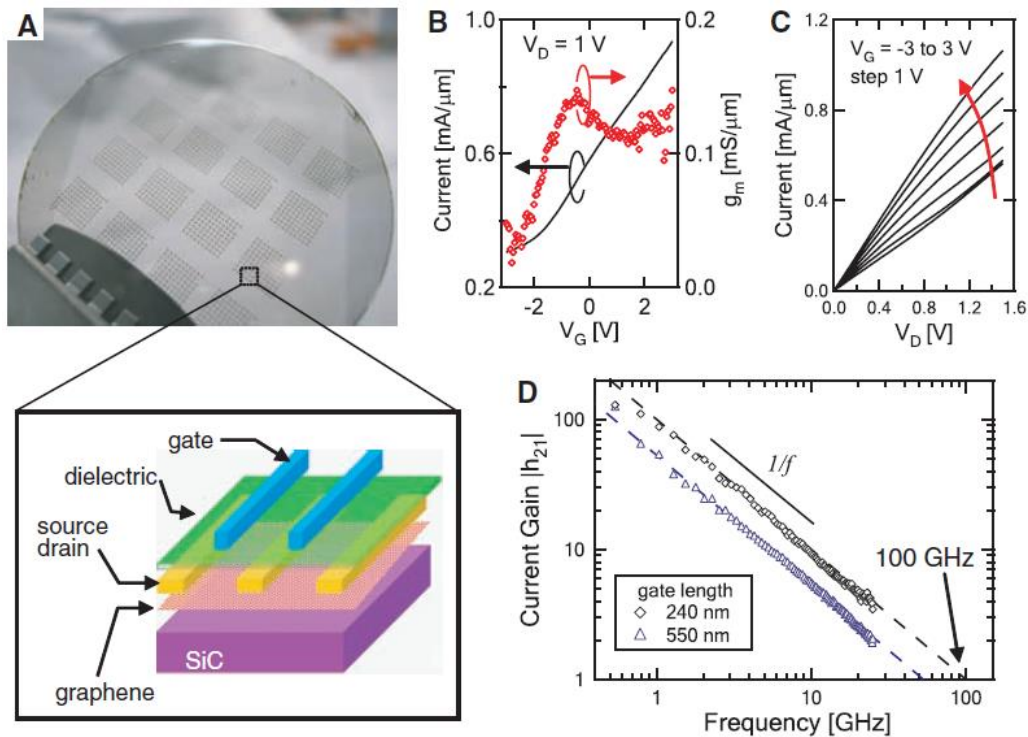


Fig. 2.7: GFETs in [II.31] (a) The graphene wafer and schematic cross-sectional view of the GFET (b)  $I_D$  vs.  $V_G$  for gate length of 240 nm (c)  $I_D$  vs.  $V_D$  for gate length of 240 nm (d) Measured small-signal current gain  $|h_{21}|$  as a function of frequency.

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

The next year, in 2011, the same IBM team demonstrated the advantages of the scalability of the graphene FETs [II.32]. This time the graphene was grown by CVD on copper film and transferred to a wafer of diamond-like carbon. Cut-off frequencies as high as 155 GHz have been obtained for the 40 nm transistors (Fig. 2.8 (b)), and the cut-off frequency was found to scale as  $1/(\text{gate length})$  (Fig. 2.8 (c)). In Fig. 2.8 (d), the Dirac point is not centered as a result of impurity charge doping possibly induced during the transfer process. Besides, this figure shows that these devices don't attain current saturation and that the gate modulation of the short-channel device is much weaker than that of the long channel one. This highlighted the dominant role of the contact resistances in short channel graphene devices.

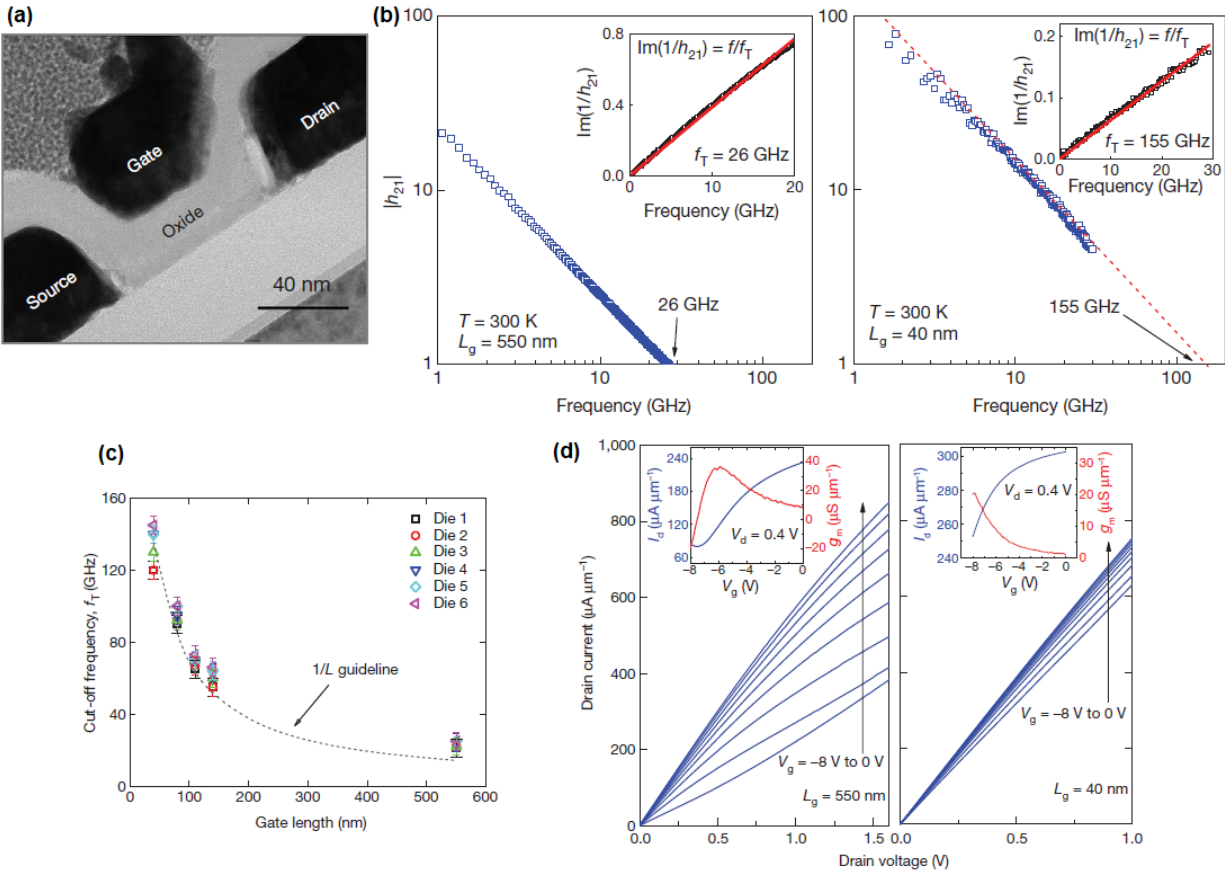


Fig. 2.8: GFETs in [II.32] (a) Cross-section TEM image of graphene transistor of gate length of 40 nm (b) Cut-off frequency of the 550 nm and 40 nm devices (c) GFETs cut-off frequencies versus gate length (d) Drain current versus the drain and gate voltages for the 550 nm and 40 nm devices.

The improvements of the  $f_T$  continued and in 2012 GFETs with a cutoff frequency exceeding 400 GHz (Fig. 2.9) have been demonstrated for a 46 nm gate length device [II.33]. In this publication, a scalable method was developed to fabricate self-aligned CVD graphene transistors on glass with transferred gate stacks. Also, the scalability of  $f_T$  with the channel length was confirmed in this work.

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

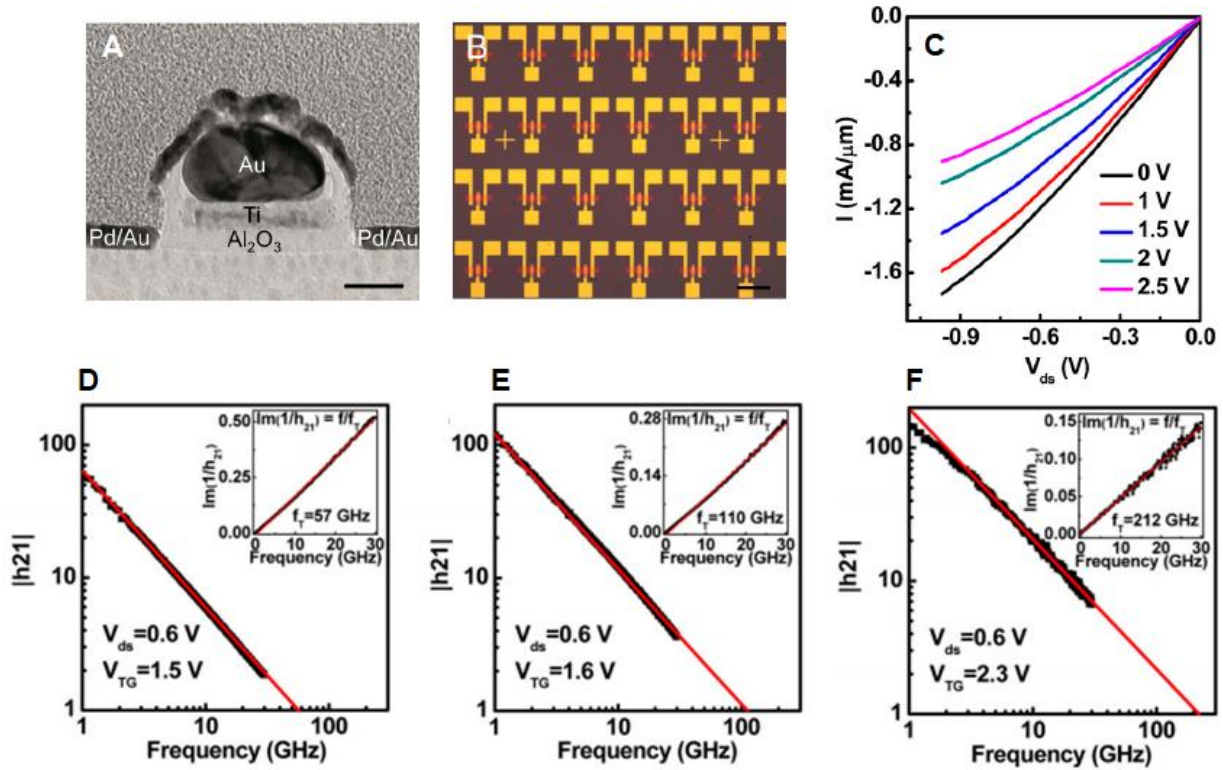


Fig. 2.9: GFETs in [11.33] (a) Optical image of self-aligned graphene transistors (b) Cross-sectional TEM image of a device (c)  $I_{DS}$  vs.  $V_{DS}$  of 300 nm gate length (d)  $f_T$  for 220 nm gate length (e)  $f_T$  for 100 nm gate length (f)  $f_T$  for 46 nm gate length.

In contrast of the advances in terms of  $f_T$  performances, until 2016 the highest reported intrinsic and extrinsic maximum oscillation frequency ( $f_{max}$ ) in graphene FETs were 70 and 38 GHz respectively [11.34] (Fig. 2.10). In these devices, graphene was fabricated on the C-face of SiC, unlike most of the graphene devices synthesized on SiC substrate where graphene is grown on the Si-face of the SiC.

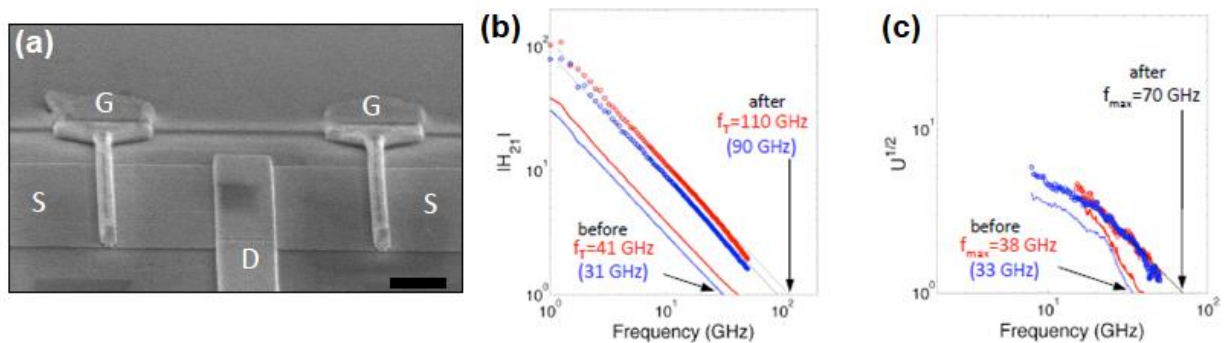


Fig. 2.10: GFETs in [11.34] SEM image of a 100 nm gate length device (b)  $f_T$  before and after de-embedding for two 100 nm devices (c)  $f_{max}$  before and after de-embedding for two 100 nm devices.

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

In 2016, [II.35] presented a novel transfer method for CVD graphene on Si wafer, which can prevent graphene from organic contamination during the fabrication process of the devices. Using a self-aligned gate deposition process, the graphene transistors with 60 nm gate length exhibited a record high  $f_{max}$  of 106 and 200 GHz before and after de-embedding, respectively. However, with all the advances in the CVD fabrication method, the current saturation is not achieved yet (Fig. 2.11 (c)).

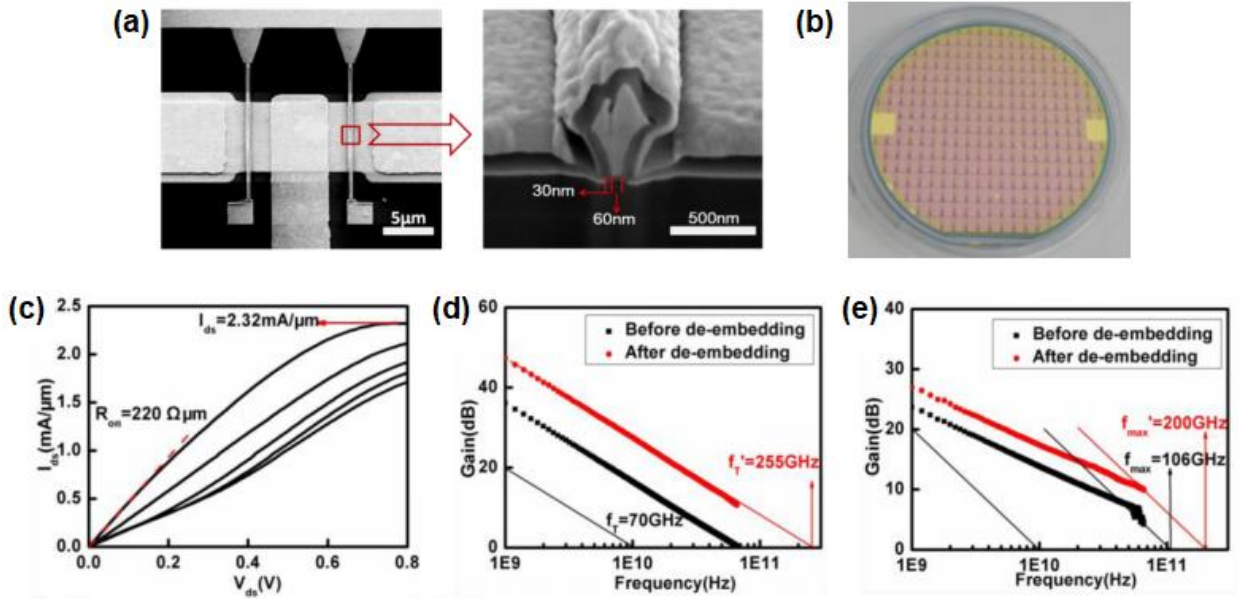


Fig. 2.11: GFETs in [II.35] (a) SEM image (b) Photo of the 3 inch wafer on Si substrate (c)  $I_{DS}$  vs.  $V_{DS}$  for 60 nm gate length GFET (d)  $f_T$  of GFET before and after de-embedding (e)  $f_{max}$  of GFET before and after de-embedding.

In the next sections we discuss three of the most important subjects in graphene transistors: scaling, contact resistances, current saturation and process variability.

### 2.3. GFET $f_T$ , $f_{max}$ and Scaling

As discussed above, it has been proved that the cut-off frequency of GFETs follow the same scaling trend as MOSFETs [II.36]. In fact, downscaling the channel mostly increase the transconductance  $g_m$  and decrease the gate capacitances  $C_{gs}$  and  $C_{gd}$  (Fig. 2.12). Thus, decreasing the channel length will increase the intrinsic cut-off frequency of the transistor given by the equation:

$$f_{T-int} = \frac{g_m}{2\pi (C_{gs} + C_{gd})} \quad (2.1)$$

However, while in theory shortening the channel should increase  $f_T$ , in practice it's more complex due to the short channel effects. These effects are brought along by the drain and source coming closer together thus strengthening the electric field along the vertical axis. Nevertheless, although the performance of the intrinsic transistor may be improved with a short channel, some effects such as the contact resistances ( $R_D$  and  $R_S$  in Fig. 2.12), do not scale with channel length. Thus, scaling the transistors is not sufficient to solve the major obstacles the GFET technology is encountering.



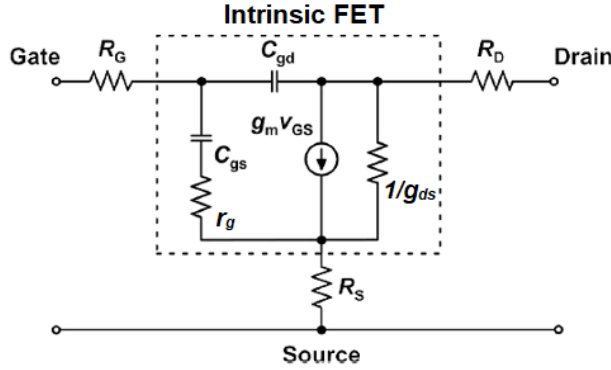


Fig. 2.12: Small-signal equivalent circuit of a FET.

Furthermore, the slower improvement of  $f_{max}$  is mostly due to the fact that it does not always scale with channel length. In fact, as equation (2.2) shows, contrarily to  $f_T$ ,  $f_{max}$  highly depends on the gate resistance ( $r_g$  in Fig. 2.12) and the source-drain conductance ( $g_{ds}$ ). Therefore, the large  $g_{ds}$  of GFETs caused by the weak drain current saturation, combined with the non-optimized gate resistance, deteriorate seriously the  $f_{max}$  of graphene transistors.

$$f_{max-int} = \frac{g_m}{4\pi C_{gs} \sqrt{r_g} g_{ds}} \quad (2.2)$$

Fig. 2.13 shows the study carried out in [II.37] of the effect of the gate resistance  $r_g$  on the  $f_{max}$ , where it was verified that  $f_{max}$  is inversely proportional to the square root of  $r_g$  which is consistent with theoretical derivation.

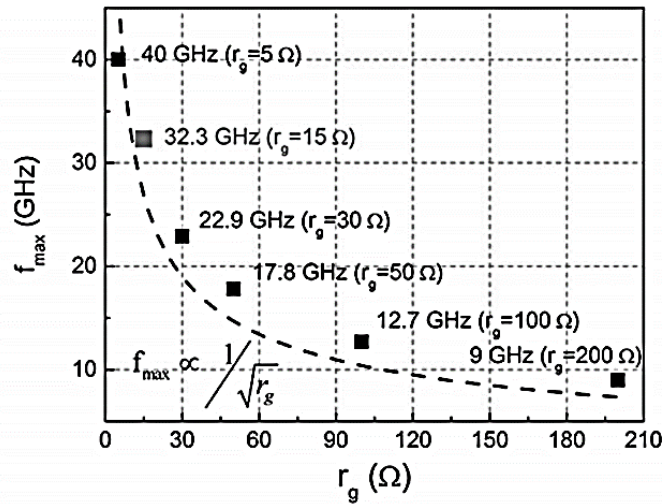


Fig. 2.13:  $f_{max}$  dependence on the gate resistance [II.37].

Fig. 2.14 shows the up-to-date state of the art frequency performances of the graphene compared to Si, GaAs and InP devices. The graph shows that currently the  $f_{max}/f_T$  performance of graphene devices is still modest compared to other technologies.

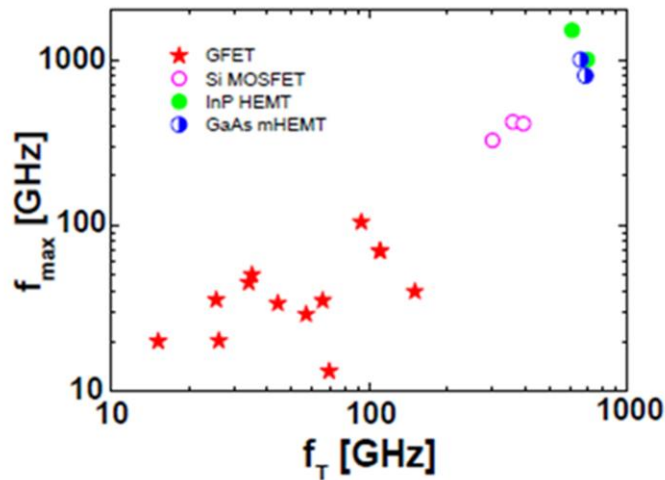


Fig. 2.14: Frequency performances of state of the art Si, GaAs, InP and graphene transistors [11.38].

It is worth to be noted that another way to achieve higher transconductance is to improve the gate control over the channel, which usually means thinning the gate oxide. However, since the gate oxide deposition has been problematic in GFETs in general, the straightforward way to improve  $g_m$  is to shorten the transistor.

#### 2.4. GFET Contact Resistances

Graphene-metal contact resistance (Fig. 2.15) has proven to be one of the major issue of graphene transistors so far. The contact resistance is the resistance between the source/drain metal and the graphene channel. The specific contact resistance is denoted with  $R_c$  and the total series parasitic resistance of a GFET is denoted with  $R_S$  or  $R_D$ . The total series parasitic resistance is the sum of  $R_c$  and the resistance of the ungated channel. Contact resistances have a large impact on the transistor performance merits, such as the cut-off frequency, extrinsic transconductance, maximum frequency of oscillation and the  $(I_D, V_G)$  linearity.

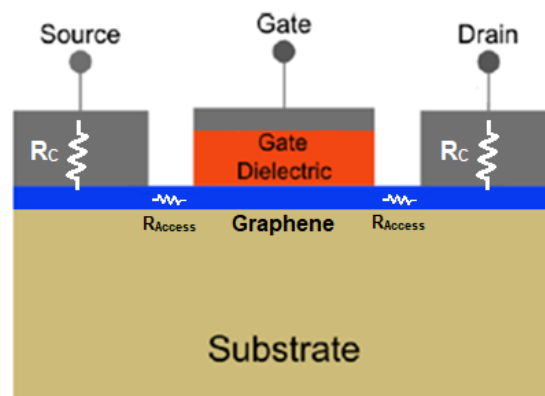


Fig. 2.15: Illustration of the GFET contact and access resistances.

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

As discussed above, the excellent intrinsic properties of graphene transistors are masked by the contact resistance. Especially for short channel GFETs, the contact resistance is detrimental since  $R_c$  does not scale down with length, thus the total GFET resistance is dominated by  $R_c$  [II.39].

Contact resistance is affected by many factors which makes the investigation of contact effects complicated. Main factors include the choice of metal and substrate, metal doping, Fermi level pinning, distance between graphene and metal layer, processing steps and contact geometry [II.40] and processes used in fabrication [II.41].

Table 2.2 summarizes contact resistances from literature. The lowest resistances are obtained with gold and nickel/gold stack with sheet resistances of 793 and 977  $\Omega/\text{sq}$  respectively. In perspective, the ITRS (International Technology Roadmap for Semiconductors) target silicide sheet resistance of 8.7  $\Omega/\text{sq}$  at 17 nm, increasing to 14.9  $\Omega/\text{sq}$  at 9.7 nm [II.42]. Thus, improving the contact resistance is of highest priority for graphene transistors.

Metal/Graphene	Channel width (W) ( $\mu\text{m}$ )	$R_{SH}$ ( $\text{k}\Omega/\text{sq}$ )	$R_c W$ ( $\Omega \mu\text{m}$ )	Measurement condition
Au (81 nm)	40	0.793	(500 $\pm$ 213)	Air
Pd (75 nm)	40	1.149	(968 $\pm$ 317)	Air
Ni (75 nm)	40	1.919	(2248 $\pm$ 417)	Air
Ni (25 nm) + Au (50 nm)	40	0.977	(404 $\pm$ 382.9)	Air
Pt (25 nm) + Au (50 nm)	40	1.799	(1068 $\pm$ 514.6)	Air

Table 2.2: State of the art of metal/graphene contact resistances [II.43].

### 2.5. GFET Current Saturation

When a transistor operates in the saturation region, the output current is nearly constant for a wide range of voltages, thus the transistor acts as a current source and is used for amplification. Without drain current saturation, a transistor is technically a voltage controlled resistor and thus its usage is incomplete.

Until now, most graphene transistors do not show complete current saturation. Reasonably, this is mainly originated from the semi-metallic (zero-gap semiconductor) nature of graphene. However, several scientific publications analyze that the origins of the absence of saturation is due to the device quality and fabrication process [II.44].

Therefore, the reasons for not detecting a complete current saturation in graphene transistors can be attributed to:

- Absence of bandgap in graphene.
- Trapped charges between the substrate and the gate oxide.
- High transistor resistances.
- Low gate control of the channel.
- Graphene's impurities.

Thus, studying these matters in order to achieve current saturation is essential for graphene transistors.

### 2.6. GFET Process Variability

Most of the publications on graphene devices show only the best performances obtained. In fact, GFETs fabricated with the same properties and on the same wafer can present very different performances. This problem increases the difficulty of modelling GFETs and designing graphene circuits.

Fig. 2.16 (a) shows the  $f_T/f_{max}$  of five GFETs fabricated with the CVD method on the same wafer and of the same gate length of 400 nm [II.37]. While four transistors present values of  $f_T$  around 25 GHz, the third device present a much lower value of 19.6 GHz. In addition, the fourth and the fifth device present similar  $f_T$ , but they present 8 GHz of difference in terms of  $f_{max}$ .

Fig. 2.16 (b) presents the distribution of the peak transconductance of 14 GFETs with the same gate length of 550 nm, all fabricated on the same wafer with the thermal decomposition on SiC method [II.45]. This histogram shows the difference in performance of the fabricated devices with transconductance values ranging between 0.02 and 0.09 mS/ $\mu$ m.

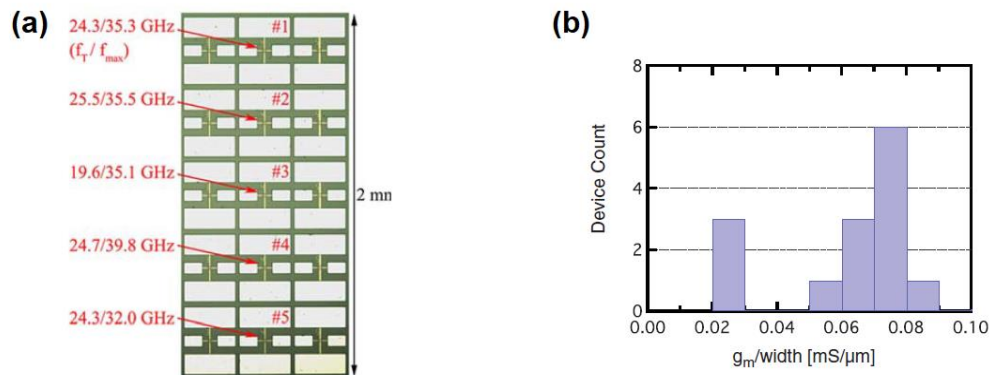


Fig. 2.16: (a)  $f_T/f_{max}$  of five 400 nm GFETs in [II.37] (b) Distribution of peak  $g_m$  of fourteen 550 nm GFETs in [II.45].

In [II.46], a statistical analysis was carried out on wafer scale CVD graphene transistors. Fig. 2.17 (a) shows the percentage of working devices on each die of the measured wafer. The right side of the wafer has a lower percentage of working transistors. Fig. 2.17 (b) and (c) show the variability of the values of contact resistances of each die of the wafer.

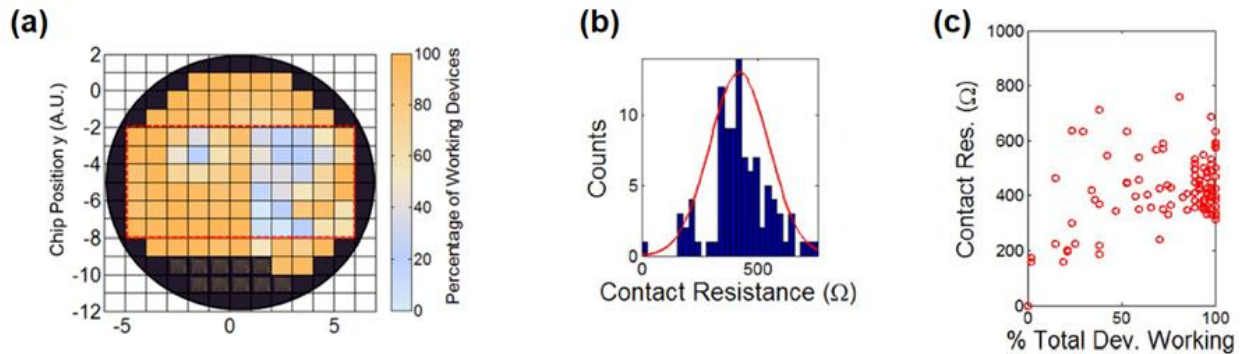


Fig. 2.17: [II.46] (a) Percentage of working devices (b) Histogram of the average contact resistance of each die over the wafer (c) Contact resistance versus percentage of working devices.



### 3. State of the Art of Graphene RF Circuits and Amplifiers

#### 3.1. State of the Art of Graphene Circuits

In order to inspect the capabilities of graphene devices in circuit level, various RF circuits have been reported.

On the system level, a CVD graphene RF receiver integrated circuit on silicon was developed in 2014 [II.47]. Fig. 2.18 (a) and (b) show the circuit which is composed of 11 passive and active components designed on four metal levels, with a process fully compatible to current silicon foundry process flow. As shown in Fig. 2.18 (c) and (d) the original bit stream comprising 3 letters (24 bits) was recovered by the graphene receiver with very low distortion.

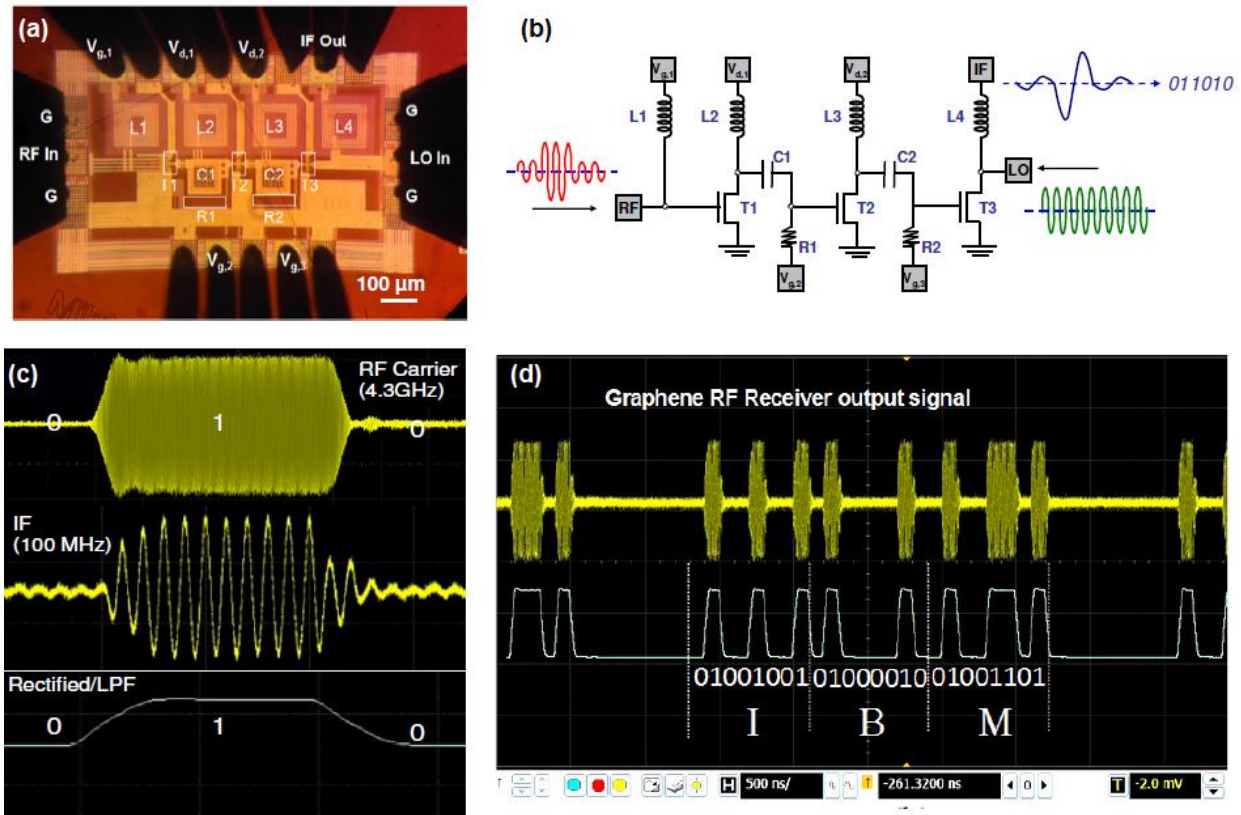
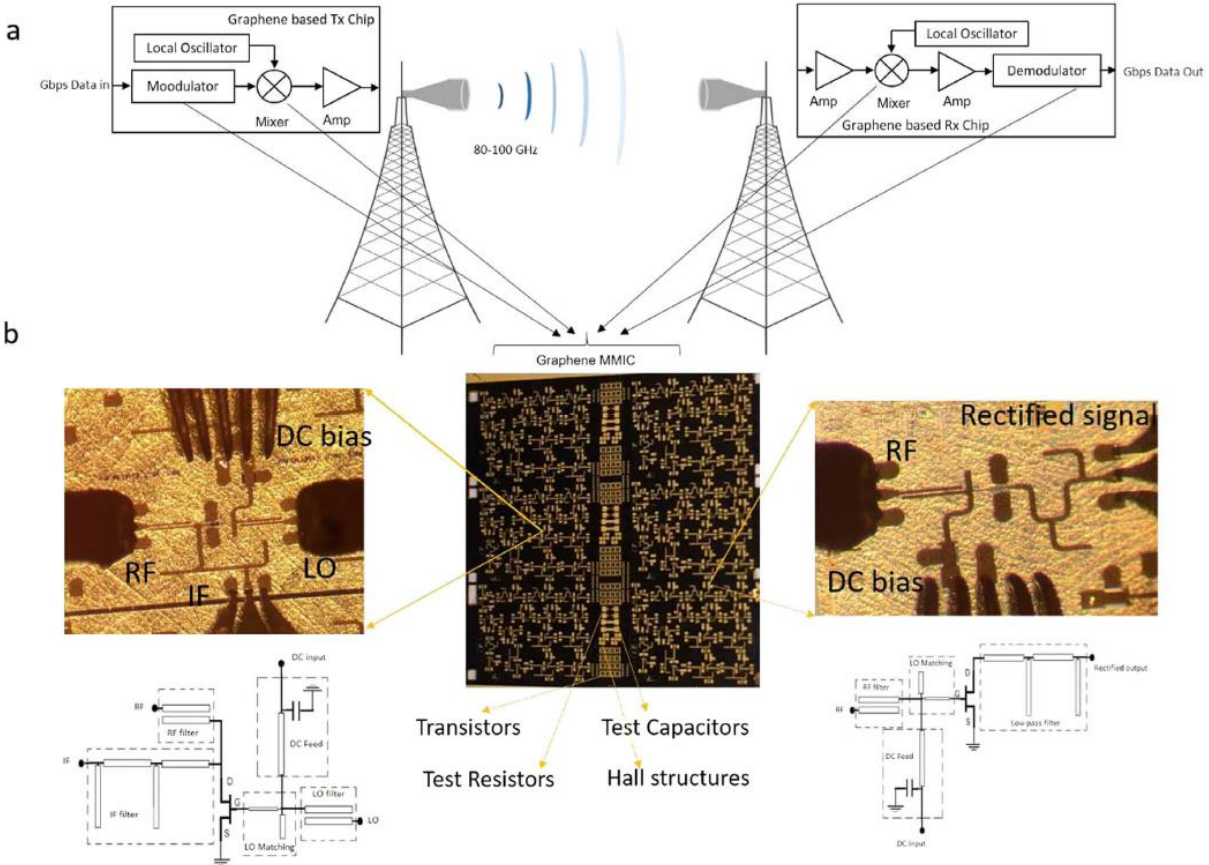


Fig. 2.18: Graphene receiver in [II.47] (a) Optical micrograph ( $1020 \times 600 \mu\text{m}^2$ ) (b) Circuit schematic (c) Measured waveforms of RF input signal amplitude modulated at a rate of 20 Mb/s, IF output signal, and restored binary code after rectifying and low-pass filtering IF signal (d) Receiver output waveforms taken from the oscilloscope.

Moreover, monolithic integrated circuits based on graphene, operating at frequencies between 80 and 100 GHz were demonstrated [II.48]. The demonstrated circuits (Fig. 2.19) are capable of encoding/decoding of multi-gigabit per second information into/from the amplitude or phase of the carrier signal. The chip is fabricated on a  $70 \mu\text{m}$  thick SiC and consists mainly of frequency mixers and integrated power detectors.

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY



*Fig. 2.19: Graphene based high data rate communication landscape [II.48] (a) A perspective view of high data rate link based on graphene transmitter and receiver (b) Fabricated chip ( $15 \times 15 \text{ mm}^2$ ) consists of frequency mixer ICs (left:  $1.35 \times 1.1 \text{ mm}^2$ ) and integrated power detector ICs (right:  $1.35 \times 0.7 \text{ mm}^2$ ).*

Besides, graphene mixers have been investigated in different configurations. The fundamental single-ended [II.49] and double-balanced [II.50] resistive GFET mixers have achieved the Conversion Loss (CL) values of 14 dB at 2 GHz and 33 dB at 3.6 GHz, respectively. Subharmonic resistive GFET mixer was developed and achieved a CL of 19 dB at 24 to 31 GHz [II.51]. The GFET subharmonic mixer implementation uses a single transistor and no balun is required, making the circuit topology more compact. Recently, an integrated subharmonic GFET mixer circuit on silicon (Fig. 2.20) was developed in [II.52], it operates at 185 to 215 GHz, which is the highest frequency of operation reported for any graphene integrated circuit. The mixer was realized in the air-bridged coplanar wave technology with a CVD grown graphene transistor. The CL of this mixer is  $29 \pm 2$  dB across the 185 to 210 GHz band with 12.5 to 11.5 dBm of local oscillator pump power.

Moreover, millimeter wave [II.53] [II.54] and terahertz [II.55] [II.56] power detectors have been reported. Besides, frequency doublers and multipliers [II.57] [II.58], and ring oscillators [II.59] have been demonstrated on graphene technologies.

Until now, graphene technology hasn't reached silicon CMOS performances for high frequency applications. However, these pioneering works present a step toward the potential future use of graphene in millimeter wave and even terahertz wave transceivers.

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

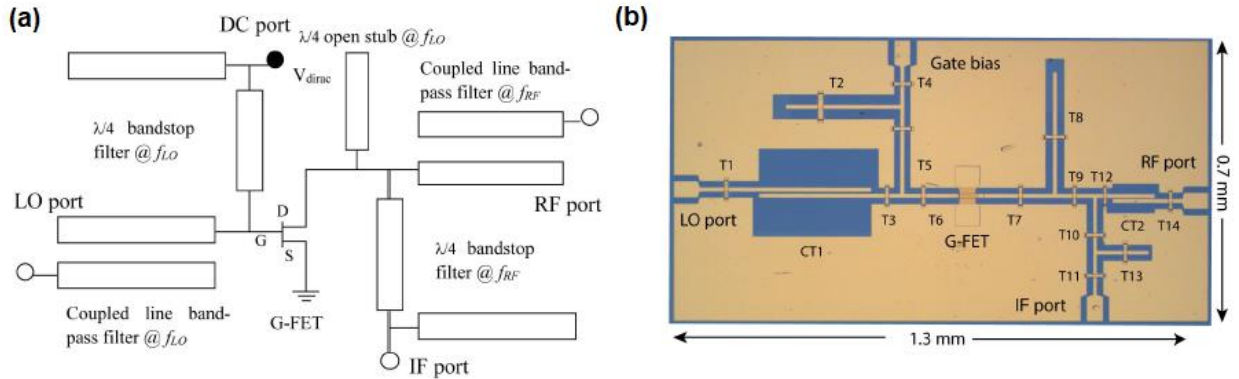


Fig. 2.20: The 185 to 215 GHz graphene subharmonic mixer [II.52] (a) Schematic of the circuit (b) Micrograph of the fabricated circuit.

### 3.2. State of the Art of Graphene Amplifiers

In addition to the circuits cited above, some works evaluating the amplifying characteristics of graphene have been proposed (Table 2.3):

- S.-J. Han et al. [II.60] were the first to study amplification of GFETs. [II.60] presents a graphene voltage amplifier using a grounded source CVD-grown Graphene FET with external bias tees. This demonstrated amplifier showed 5 dB of gain at 460 MHz (Fig. 2.21 (a)).
- J. Lee et al. [II.61] implemented a CVD-grown GFET amplifier (Fig. 2.21 (b)) on a Printed-Circuit Board (PCB) with a gain of 1.3 dB at 380 MHz.
- M. A. Andersson et al. [II.62] realized a 1 GHz amplifier with a mechanically exfoliated graphene FET and external inductor and bias tees (Fig. 2.21 (c)). This amplifier exhibited a small signal power gain of 10 dB at 1 GHz. The same team with O. Habibpour et al. [II.63] showed the feasibility of amplifiers with 6-7 dB gain per stage up to 4 GHz.
- J. D. Aguirre et al. [II.64] implemented a GFET amplifier with graphene synthesized on SiC substrate. This circuit shows a 2 dB of gain at 0.2 GHz. The amplifier gain is enhanced using an input matching LC circuit, which is connected to the GFET through standard RF probes (Fig. 2.21 (d)).
- C. Yu et al. [II.65] presented a GFET MMIC (Monolithic Microwave Integrated Circuit) low noise amplifier (Fig. 2.21 (e)) with graphene synthesized on SiC. This amplifier achieved a small signal gain of 3.4 dB and a noise figure of 6.2 dB at 14.3 GHz.

Parameter	[II.60]	[II.61]	[II.62]	[II.64]	[II.65]
Freq. [GHz]	0.46	0.38	1	0.2	14.3
L [nm]	500	180	1000	270	200
W [μm]	30	32	60	48	40
V <sub>DS</sub> [V]	-1.3	1	-1.25	4	-1.7
V <sub>GS</sub> [V]	-0.1	0	1	-3	0.2
Max. Gain [dB]	5	1.3	10	2	3.4
P <sub>OUT</sub> [dBm / mW]	-	-	-	-	-
PAE [%]	-	-	-	-	-

Table 2.3: State of the Art of graphene-based amplifiers.

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

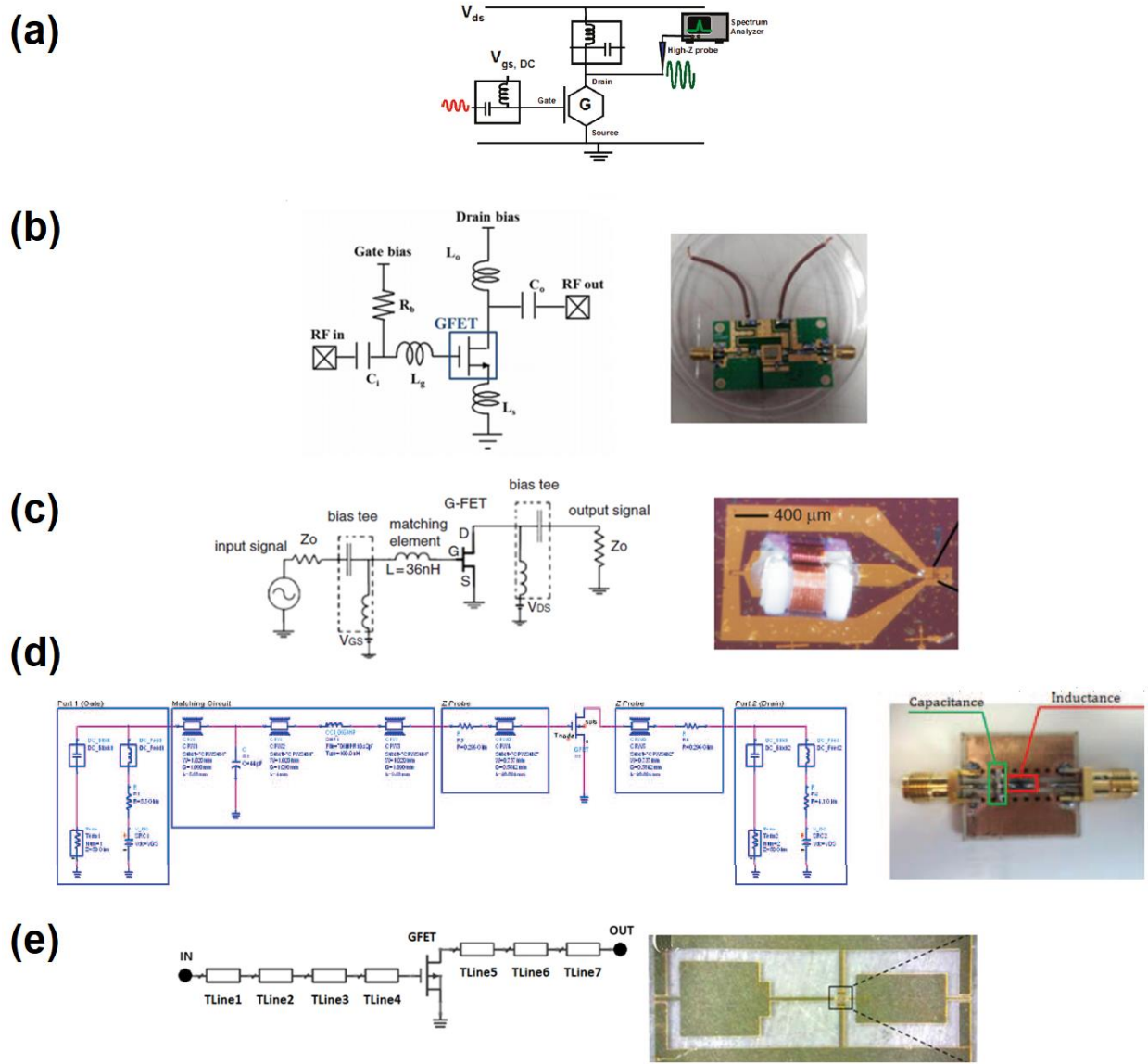


Fig. 2.21: Schematics and photos of state of the art graphene-based amplifiers (a) [II.60] (b) [II.61] (c) [II.62] (d) [II.64] (e) [II.65].

In the face of these pioneering works of graphene amplifiers, GFETs have generally been regarded as being hard to provide large gain. This is largely due to the weak current saturation in the DC output characteristics. Remarkably, none of the graphene amplifiers mentioned earlier presents the large signal performances, particularly the output power and the efficiency have never been reported.

In the next parts of the chapter, aiming to investigate the large signal performance of graphene amplifiers, particularly the power gain, the output power and the efficiency, we report the analysis and design of integrated power amplifiers based on three graphene FETs with different fabrication methods and substrates.



## 4. Graphene Transistors Properties and Characteristics

In this part, we present the properties and characteristics of the three graphene transistors, with different fabrication methods and substrates, used in this work:

- GFET with graphene synthesized on SiC substrate.
- GFET with CVD-grown graphene on Si/SiO<sub>2</sub> substrate.
- GFET with mechanically exfoliated graphene and h-BN dielectrics.

These three methods of fabrication are presented in section 1.2 of this chapter.

### 4.1. GFET with Graphene Synthesized on SiC Substrate

This Graphene FET is fabricated by thermal decomposition on the Si-face of a silicon carbide wafer (Fig. 2.22). The transistor has a typical gate length of 270 nm, an effective gate width of 48 μm with two fingers of 24 μm each and a 12 nm Al<sub>2</sub>O<sub>3</sub> gate dielectric layer (shown in Fig. 2.22 (a)). Source and drain ohmic contacts are metallized with Ni/Au (50/300 nm).

This transistor is fabricated at the University of Lille, France, it is demonstrated and measured in [II.66].

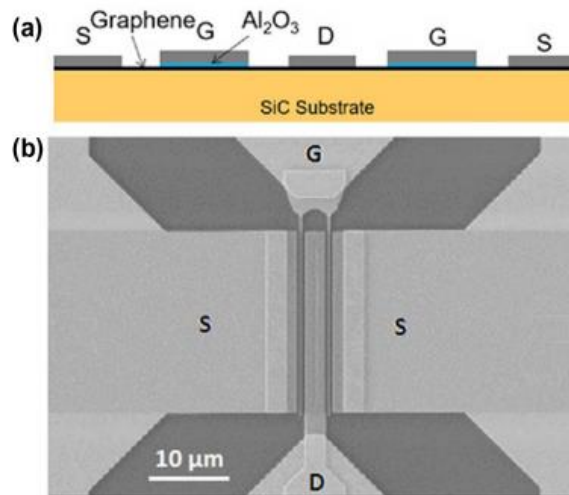


Fig. 2.22: GFET with graphene synthesized on SiC substrate (a) Schematic of the cross section of the device (b) SEM image of the device.

Output characteristics ( $I_{DS}$  vs.  $V_{DS}$ ) of the GFET device (Fig. 2.23(a)) don't show a distinct current saturation. The compact model simulation results are also illustrated in Fig. 2.23 (a) in comparison with the measurement which shows good accuracy for  $0 \text{ V} \leq V_{DS} \leq 3 \text{ V}$  and  $-4 \text{ V} \leq V_{GS} \leq 1 \text{ V}$ .

RF measurements of this device show an  $f_T$  of 20.6 GHz and an  $f_{max}$  of 15.8 GHz [II.64] for the same gate length device de-embedded from open pad. S-parameters measurements and model simulations are compared in Fig. 2.23 (b), and a good agreement is observed for different bias points. At low frequencies, the  $S_{11}$  parameter is very close to the border of the Smith chart which makes the input matching difficult.

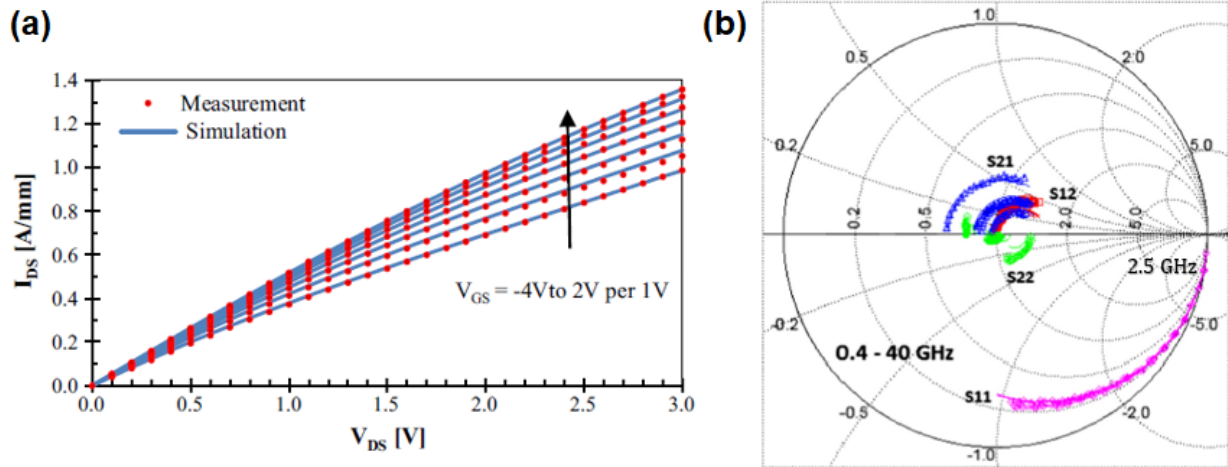


Fig. 2.23: GFET with graphene synthesized on SiC substrate (a) Output characteristic  $I_{DS}$  in function of  $V_{DS}$  for different  $V_{GS}$  measurements and simulations (b)  $S$ -parameters for  $V_{DS} = 1$  and  $3$  V and  $V_{GS} = -3$  and  $2$  V, dotted lines are measurements and complete lines are simulations.

#### 4.2. GFET with CVD-grown Graphene on Si/SiO<sub>2</sub> Substrate

In this GFET, the graphene is synthesized by chemical vapor deposition (CVD) on copper and transferred over pre-patterned back-gated devices on Si/SiO<sub>2</sub> substrate (Fig. 2.24). As the first described GFET, this device has two gate fingers with a coplanar access structure making it suitable for RF measurements. The source and the drain ohmic contacts of a Ni/Au alloy were formed by evaporation and lift-off process. The width of the device is of 24  $\mu\text{m}$  (2 gate fingers of 12  $\mu\text{m}$  each) and the gate length is 300 nm.

This transistor is fabricated is also fabricated at the University of Lille, France, its fabrication and measurements are presented in [II.67].

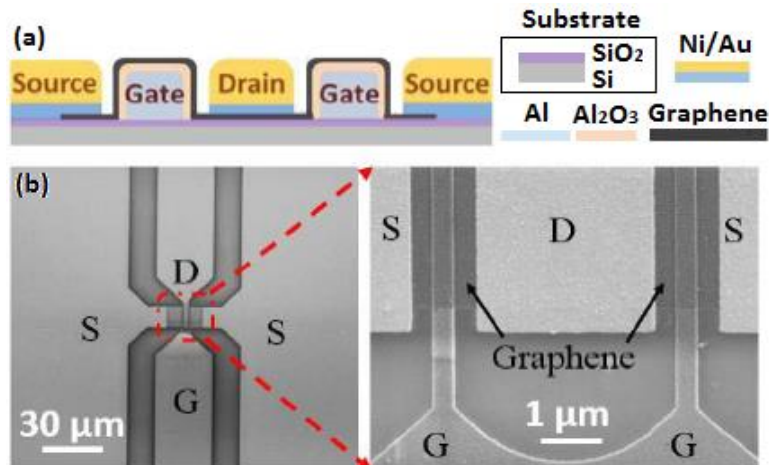


Fig. 2.24: GFET with CVD-grown graphene on Si/SiO<sub>2</sub> Substrate (a) Schematic of the cross section of the device (b) SEM image of the device.

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

Fig. 2.25 (a) shows the output characteristics of the device where the current saturation is absent and the agreement between the measurements and simulations can be seen for  $0 \text{ V} \leq V_{DS} \leq 1.5 \text{ V}$  and  $-1 \text{ V} \leq V_{GS} \leq 1.5 \text{ V}$ .

RF measurements show a  $f_T$  of 6.5 GHz and  $f_{max}$  of 5 GHz for 300-nm gate length device de-embedded from open pad. Fig. 2.25 (b) shows the agreement of S-parameters measurements and simulations for different bias points. Similarly to the first GFET, the  $S_{11}$  parameter is very close to the border of the Smith chart at low frequencies.

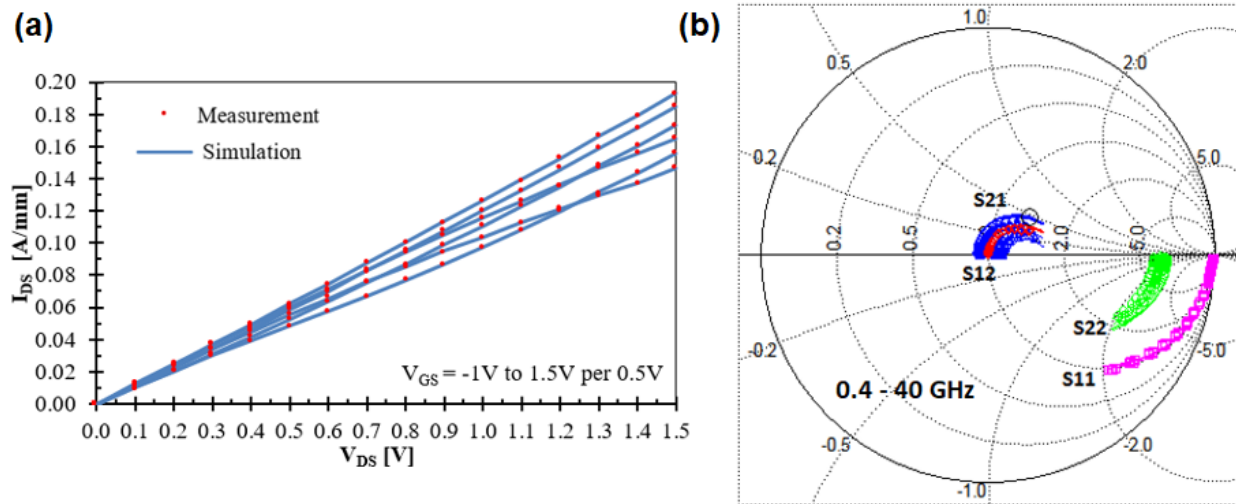


Fig. 2.25: GFET with CVD-grown graphene on Si/SiO<sub>2</sub> substrate (a) Output characteristic  $I_{DS}$  in function of  $V_{DS}$  for different  $V_{GS}$  measurements and simulations (b) S-parameters for  $V_{DS} = 1.5 \text{ V}$  and  $V_{GS} = 0.5$  and  $1 \text{ V}$ , dotted lines are measurements and complete lines are simulations.

### 4.3. GFET with Mechanically Exfoliated Graphene and h-BN Dielectrics

The last studied graphene FET (Fig. 2.26) is based on hexagonal boron nitride (h-BN) gate dielectric, a wide bandgap (5.97 eV) insulating isomorph of graphene. Using a mechanical transfer process, the h-BN layers are exfoliated from pure h-BN single crystals and transferred onto the metal gate. The h-BN has an atomically smooth surface and high surface phonon energy, its use significantly reduces impurities and charged traps. However, it is difficult to obtain a reproducible h-BN film with high quality and large area. The transistor has a gate length of 440 nm, the largest of the three transistors, an effective gate width of 48  $\mu\text{m}$  with two fingers of 24  $\mu\text{m}$  each and a 12 nm.

This transistor is fabricated by the University of Columbia, USA, it is demonstrated and measured in [II.68].

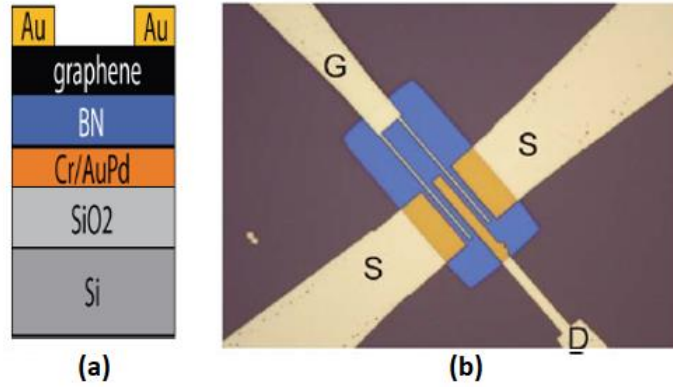


Fig. 2.26: GFET with mechanically exfoliated graphene and h-BN dielectrics (a) Schematic of the device structure (b) Optical micrograph of the device.

Fig. 2.27 shows the output characteristics the device for  $-1.5 \text{ V} \leq V_{DS} \leq 0 \text{ V}$  and  $-0.5 \text{ V} \leq V_{GS} \leq -2 \text{ V}$ . Contrarily to the two GFETs presented above, this device exhibits a current saturation. The observed current saturation is attributed to velocity saturation due to coupling to optical phonon modes. Under specific combinations of drain and gate biasing, the channel can be rendered ambipolar, resulting in a pronounced “kink” in the curves [II.44].

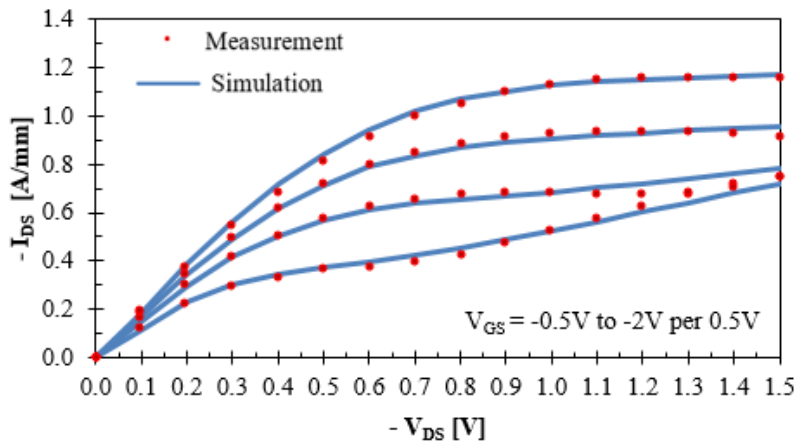


Fig. 2.27: GFET with mechanically exfoliated graphene and h-BN dielectrics output characteristic  $I_{DS}$  in function of  $V_{DS}$  for different  $V_{GS}$  measurements and simulations.



## 5. GFET Compact Model

In this section, we briefly present the GFET compact model developed at the University of Bordeaux. This model is used to obtain the DC and RF simulation results for the three GFETs shown in the three sections above. The same model is used for the three GFETs, only the model parameters differ. The basics of this model have been presented in [II.69] [II.70] [II.71], where the model has been verified using different measurements from the literature, and furthermore, its scalability was demonstrated.

GFETs are often evaluated only as a single transistor using  $f_T/f_{max}$  figures of merit, which may mislead in interpreting how GFETs will work in actual circuits. Indeed, the evaluation of GFET devices for circuit applications starts within a design environment by using electrical compact models that represent properly the electrical behavior of the device for Alternative Current (AC), DC and transient simulations.

In fact, nowadays IC design relies heavily on computer simulations. The operation of an IC is described by a number of device models and equations which describe the connections between elements. Each device model consists of a large number of equations describing the operation in each bias point. A circuit simulator solves the resulting large number of equations in thousands of operation points. In order to design ICs simple yet accurate models are needed. These two requirements are contradicting, since accuracy is often achieved with added complexity.

Analytical or compact models have been proposed by Ryhzii et al. [II.72], Meric et al. [II.73], Shepard et al. [II.74], Scott et al. [II.75], Wang et al. [II.76], Jimenez et al. [II.77] [II.78], Champlain [II.79] [II.80], Habibpour et al. [II.81], and Thiele et al. [II.82].

### 5.1. Model Description

The University of Bordeaux model [II.69] proposes a new large signal compact model based on the work from [II.67] and [II.82]. Compared to [II.67] the charge model is improved; it includes the specific density of states of graphene, and furthermore, the equations proposed in [II.82] are modified to get Verilog-A language-compatible equations for further circuit simulations. This large signal model has been developed implemented at in Verilog-A code and can be used for simulation in a standard circuit design environment such as Cadence Virtuoso or Keysight Advanced Design System (ADS).

The modeling effort is summarized as follows: first an accurate electrostatic description of the vertical metal-graphene-insulator structure is performed to compute the bias dependent charge in the graphene layer  $Q_{net}$ . Then, using a drift-diffusion model, one can integrate the charge along the channel, to express the drain current:

$$I_D = \mu W \frac{\int_0^{V_{DSi}} (|Q_{net}| + e n_{puddle}) dV}{L + \mu \left| \int_0^{V_{DSi}} \left( \frac{1}{v_{SAT}} \right) dV \right|} \quad (2.2)$$

Where  $\mu$  the mobility,  $e$  the electronic charge,  $W$  the width of the graphene sheet,  $L$  the channel length, and  $v_{SAT}$  is the saturation velocity in the graphene layer.  $n_{puddle}$  parameter is the residual carrier density, which is induced by the spatial inhomogeneity within the graphene layer [II.83].

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

The equivalent circuit of the compact model is presented in Fig. 2.28. It consists of: the drift-diffusion current source  $I_{DSDD}$  in parallel with a tunneling component  $I_{DStunnel}$ . The gate source capacitance  $C_{GS}$ , and the drain source capacitance  $C_{GD}$  with the parasitic gate-drain and gate-source capacitors  $C_{parGD}$  and  $C_{parGS}$ . And lastly, the drain, source, and gate access resistances  $R_D$ ,  $R_S$ , and  $R_G$ .

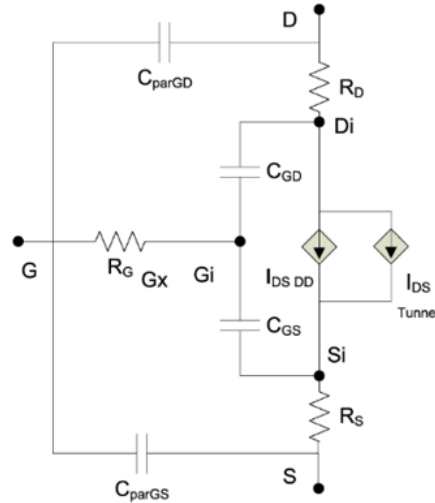


Fig. 2.28: Equivalent circuit of GFET electrical compact model.

The main compact model parameters are:

- The gate length ( $L$ ).
- The gate width ( $W$ ).
- The thickness of the top gate insulator ( $T_{ox}$ ).
- The relative permittivity of the top gate insulator ( $\epsilon_r$ ).
- The mobility ( $\mu$ ).
- The effective doping density (NF).
- The source resistance ( $R_S$ ).
- The drain resistance ( $R_D$ ).
- The gate resistance ( $R_G$ ).
- The gate source capacitance ( $C_{GS}$ ).
- The gate drain capacitance ( $C_{GD}$ ).

### 5.2. Model Parameters

Table 2.4 shows the extracted compact model parameters for the three different GFETs used in this work.

The values used for the gate length and width are taken from the devices fabricated in [II.66] [II.67] [II.68].

At  $7000 \text{ cm}^2/\text{V}\cdot\text{s}$ , the mobility of the exfoliated GFET is extremely high and its effective doping density (NF) is very low compared to the other devices since its Dirac point is around 0 V. The mobilities of the CVD-grown and the synthesized on SiC GFETs are 100 and  $500 \text{ cm}^2/\text{V}\cdot\text{s}$  respectively.

Concerning the resistances ( $R_S$ ,  $R_D$  and  $R_G$ ), compared to silicon based devices, the values of these resistances are critically high, resulting in a direct degradation of the transconductance ( $g_m$ ). The exfoliated GFET presents the lower resistances, followed by the GFET synthesized on SiC and the

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

CVD-grown GFET. As a result, the maximum  $g_m$  of the CVD, synthesized on SiC and exfoliated GFETs are 1.2, 4.5 and 29 mS respectively.

The exfoliated GFET has the highest  $C_{GS}$  and  $C_{GD}$ , followed by the CVD and the synthesized on SiC GFETs. These capacitances affect directly the S-parameters of the device. For instance, the lower the  $C_{GS}$ , the less is the variation of the  $S_{11}$  with the frequency, resulting a harder input impedance matching. On the other hand, lower values of  $C_{GS}$  result in a higher  $f_T$  and  $f_{max}$ . In fact, generally the values of these figures of merit, increase with higher  $g_m$  and smaller capacitive elements of the equivalent circuit [II.16].

Parameter	GFET synthesized on SiC	CVD-grown GFET	Exfoliated GFET
L [nm]	270	300	440
W [ $\mu\text{m}$ ]	48	24	48
$T_{ox}$ [nm]	12	3	8.5
$\epsilon_r$	9	5.18	3.54
$\mu$ [ $\text{cm}^2/\text{V}\cdot\text{s}$ ]	500	100	7000
NF [ $\text{cm}^{-2}$ ]	$3.61 \times 10^{13}$	$1.29 \times 10^{12}$	$< 10^{11}$
$R_S$ [ $\Omega \cdot \mu\text{m}$ ]	590	3217	188
$R_D$ [ $\Omega \cdot \mu\text{m}$ ]	590	3217	232
$R_G$ [ $\Omega/\text{sq}$ ]	0.95	5	0.1
$C_{GS}$ [fF]	35.7	39.9	70
$C_{GD}$ [fF]	16.5	30.1	36.5

*Table 2.4: Extracted compact model parameters of the three GFETs.*

## 6. Graphene Power Amplifiers Design

The classic topology of the common source amplifier is chosen to evaluate the three graphene devices in power amplification. Fig. 2.29 shows the schematic of the GFET amplifiers. The device's source is grounded and the drain and gate are biased. The input and output matching networks serve, with the bias inductances, to match the device to the 50 Ω input and output ports.

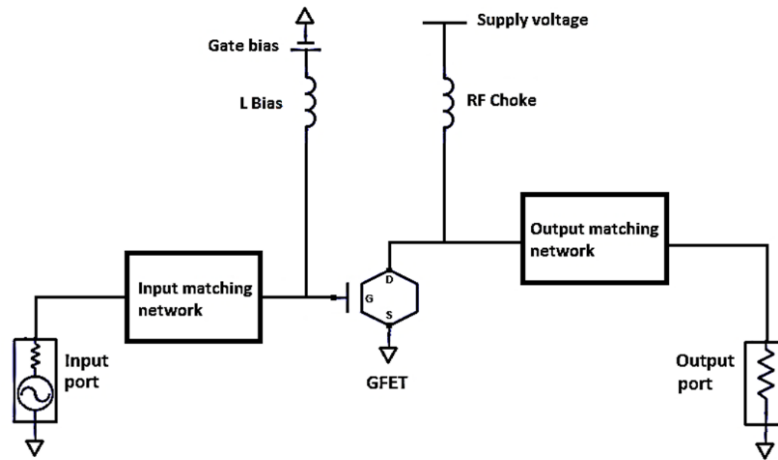


Fig. 2.29: Schematic of the single stage common source GFET amplifiers.

The major difficulty in designing graphene amplifiers is the impedance matching. In fact, as shown in Fig. 2.30 the input port reflection coefficient  $S_{11}$  is very close to the open circuit at 2.5 GHz for the three devices. This is mainly due to a very small input capacitance combined with a moderate working frequency of the transistor. As analyzed in [II.70] a large inductor is necessary for input matching in the GHz range to avoid strong reflection. At higher frequencies, the  $S_{11}$  will drift from the open circuit, but the gain and the performance of the transistor and amplifier will decline drastically (Fig. 2.31).

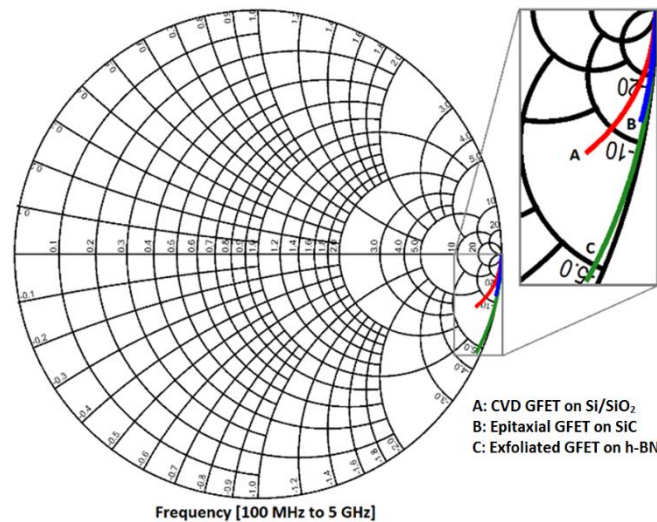


Fig. 2.30: Smith chart reporting  $S_{11}$  parameter of the three GFET devices.

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

Consequently, the center frequency of operation is chosen to be 2.5 GHz to evaluate graphene amplifying performances, since the graphene devices don't exhibit significant gain at the millimeter wave 5G frequency candidates, and also because of abundance of RF applications at this frequency.

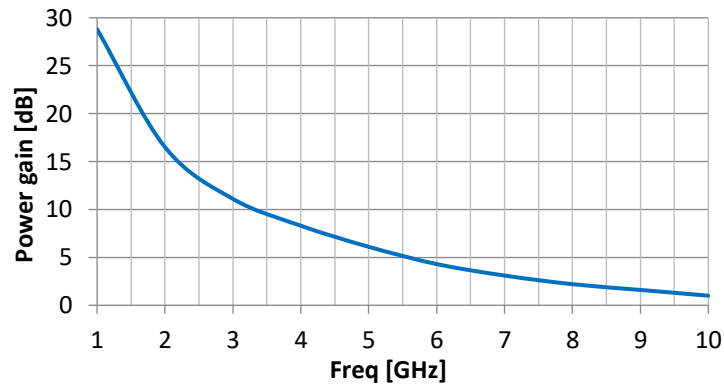


Fig. 2.31: Maximum available power gain in function of the frequency of a GFET synthesized on SiC power amplifier for  $V_{DS} = 3 V$  and  $V_{GS} = -2 V$ .

Concerning the circuit design, we propose the use of Coplanar Wave Guide (CPW) technology. In fact, the CPW are commonly used in the radiofrequency range for their technological simplicity and high performances.

The stack used for the circuits design [II.84] is shown in Fig. 2.32. Metal 1 is used as a first layer for capacitance design, the nitride serves as the capacitance dielectric. Metal 2 is a second layer of capacitances, for circuit interconnections, for inductors and for CPW design. Finally Metal 3 is used for air bridge design.

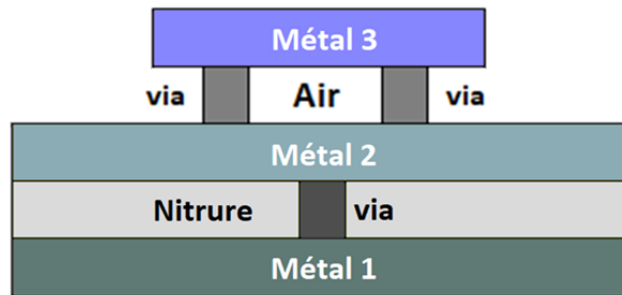


Fig. 2.32: Metal stack used for designing the graphene amplifiers.

A 2.5D Finite Element Method (FEM) electromagnetic simulation is used to simulate accurately the complete passive elements and interconnections using Momentum Microwave of Keysight Advanced Design System. Then, a complete mixed simulation is run using the FEM simulation results model with the DC and RF response of the GFET being extracted from the compact model described above.

Therefore, based on the agreement between the compact model simulations and the DC and RF measurement results of the three transistors, we present in the next three sections the design and layout of three graphene power amplifiers.

### 6.1. GFET with Graphene Synthesized on SiC Substrate PA

Choosing the bias voltages of this amplifier will lead to a tradeoff between the output power and the PAE since these two factors behave oppositely in terms of  $V_{DS}$  and  $V_{GS}$ . In fact, with higher  $V_{DS}$ , the output power increases but the PAE decreases due to the high  $P_{DC}$ . Additionally, in terms of  $V_{GS}$  the maximum output power is achieved for  $V_{GS} = 2\text{ V}$  and the maximum PAE is obtained for  $V_{GS} = -3\text{ V}$ .

Consequently, we present two bias points for this amplifier: maximum PAE ( $V_{DS} = 1\text{ V}$ ,  $V_{GS} = -3\text{ V}$ ), and maximum  $P_{OUT}$  ( $V_{DS} = 3\text{ V}$ ,  $V_{GS} = 2\text{ V}$ ).

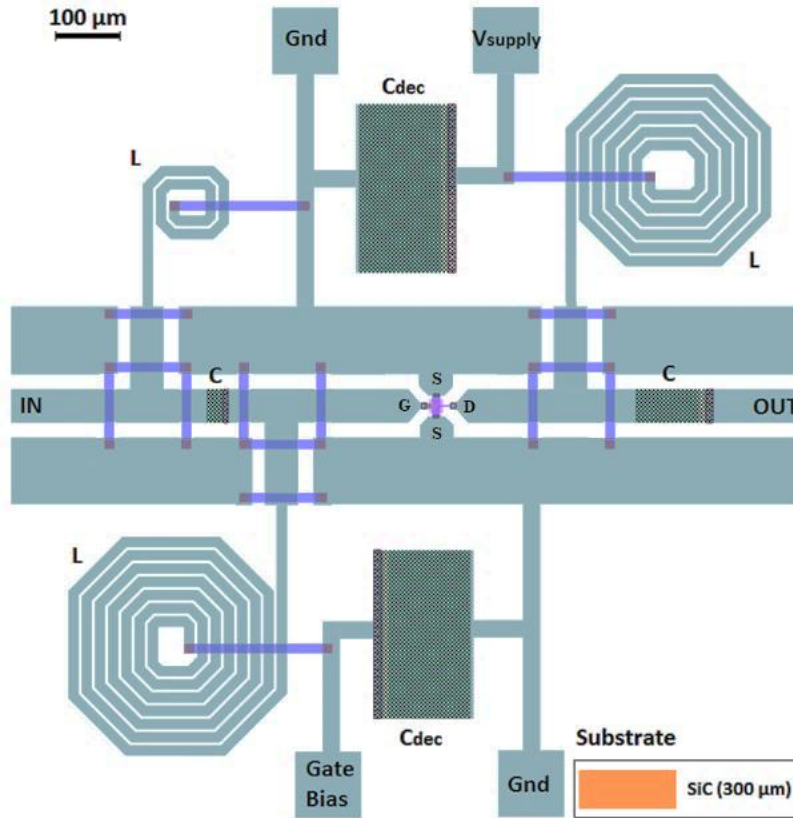


Fig. 2.33: Layout of the GFET synthesized on SiC amplifier ( $1.2 \times 1.2\text{ mm}^2$ ).

Fig. 2.33 shows the final layout of the amplifier. The substrate is a  $300\text{ }\mu\text{m}$  thick SiC with dielectric constant of 9.66 and a resistivity of  $6000\text{ }\Omega\cdot\text{cm}$ . The elements used in the circuit are a  $9\text{ nH}$ ,  $6\text{ nH}$  choke inductances and  $0.7\text{ nH}$  inductance at the input, with a  $1\text{ pF}$  and  $370\text{ fF}$  DC Block capacitances. It is worth noting that the RF chokes (inductances) and the DC block capacitances serve in the matching networks. In addition, two  $4\text{ pF}$  decoupling capacitances are used between the gate and drain biasing and the ground, and all the grounds of the circuit are connected.

6.2. GFET with CVD-grown Graphene on Si/SiO<sub>2</sub> Substrate PA

The bias voltages of the CVD GFET are chosen to exhibit a maximum power gain, since the output power and the PAE of this device are very low at all bias conditions. Thus, this amplifier is biased at the maximum transconductance of the transistor ( $V_{DS} = 1.5$  V,  $V_{GS} = 1.2$  V).

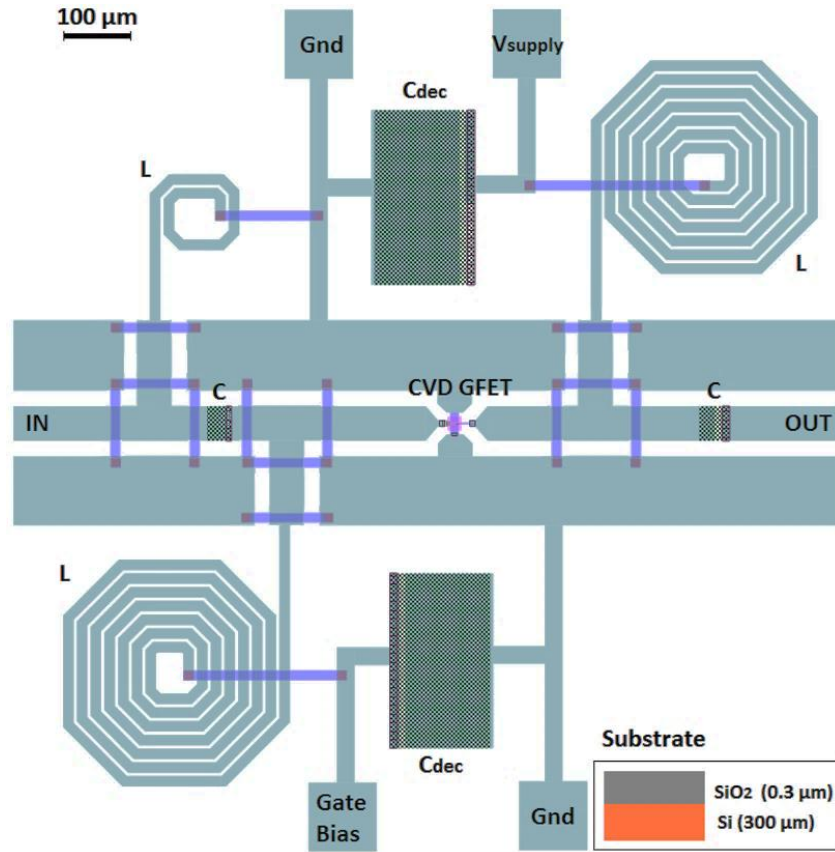


Fig. 2.34: Layout of the CVD-grown GFET amplifier ( $1.2 \times 1.2$  mm<sup>2</sup>).

Fig. 2.34 shows the final layout of the amplifier. The substrate of the CVD GFET circuit is a 300 μm thick silicon, having a dielectric constant of 11.9 and a resistivity of 5000 Ω·cm. The above layer is the 0.3 μm dielectric SiO<sub>2</sub>, having a relative permittivity of 3.9.

The elements used in this circuit are a 9 nH, 7 nH choke inductances and 0.5 nH inductance at the input, with a 400 fF and 360 fF DC block capacitances. Similarly to the first layout, the RF chokes and the DC block capacitances serve in the matching networks and two 4 pF decoupling capacitances are used between the gate and drain biasing and the ground.

6.3. GFET with Mechanically Exfoliated Graphene and h-BN Dielectrics PA

In this device, the variations of the power gain, output power and efficiency are nearly the same with the bias voltages, resulting minor tradeoffs. In fact, the maximum performances are obtained with  $V_{DS} = -1.2\text{ V}$ ,  $V_{GS} = -2\text{ V}$ .

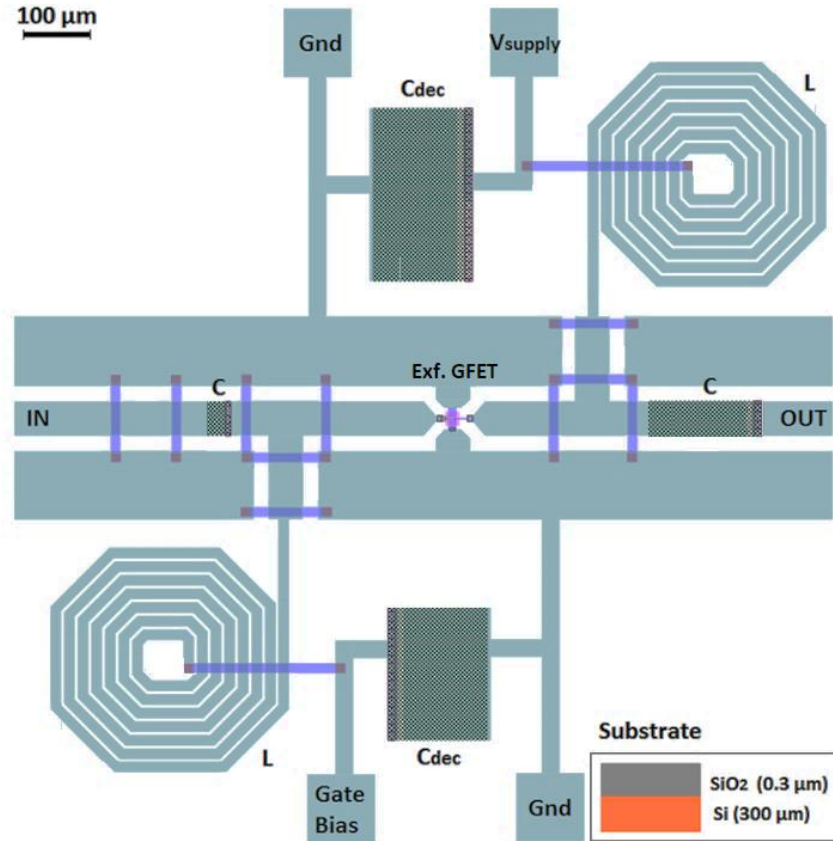


Fig. 2.35: Layout of the mechanically exfoliated GFET amplifier ( $1.2 \times 1.2\text{ mm}^2$ ).

Fig. 2.35 shows the final layout of the amplifier. The substrate is constituted of a  $300\text{ }\mu\text{m}$  thick silicon, having a dielectric constant of 11.9 and a resistivity of  $5000\text{ }\Omega\cdot\text{cm}$ . The above layer is the  $0.3\text{ }\mu\text{m}$  dielectric  $\text{SiO}_2$ , having a relative permittivity of 3.9.

The elements used in the circuit are two  $10\text{ nH}$  choke inductances, with a  $1.5\text{ pF}$  and  $150\text{ fF}$  DC Block capacitances. Only the RF chokes and the DC block capacitances are used for input and output matching.



## 7. Post-layout Simulation Results

### 7.1. GFET with Graphene Synthesized on SiC Substrate PA Results

Fig. 2.36 shows the S-parameters of the first amplifier. At 2.5 GHz, the  $S_{11}$  and  $S_{22}$  parameters are substantially low indicating the reliable matching and insignificant losses especially at the input. The peak gain  $S_{21}$  is 4.9 dB and 6.8 dB for the maximum output power and PAE respectively. In addition, the amplifier is unconditionally stable for the two bias conditions in the operating frequency range.

Concerning the large signal performances (Fig. 2.37), in terms of power gain, a gain expansion occurs for both bias points allowing higher power gain. This phenomenon generally happens in class B and class AB amplifiers where the transistor is biased below 20 % of its saturated drain current [11.85]. The peak power gain values are 8.9 and 8.2 dB for the maximum PAE and maximum  $P_{OUT}$  bias points respectively. The maximum output power of this device is 5.2 dBm, and the maximum PAE is 2.2 %. The  $P_{OUT}$  for the maximum PAE bias point is -3.2 dBm (0.5 mW) and the  $PAE_{max}$  for the maximum  $P_{OUT}$  bias point is 1.4 %.

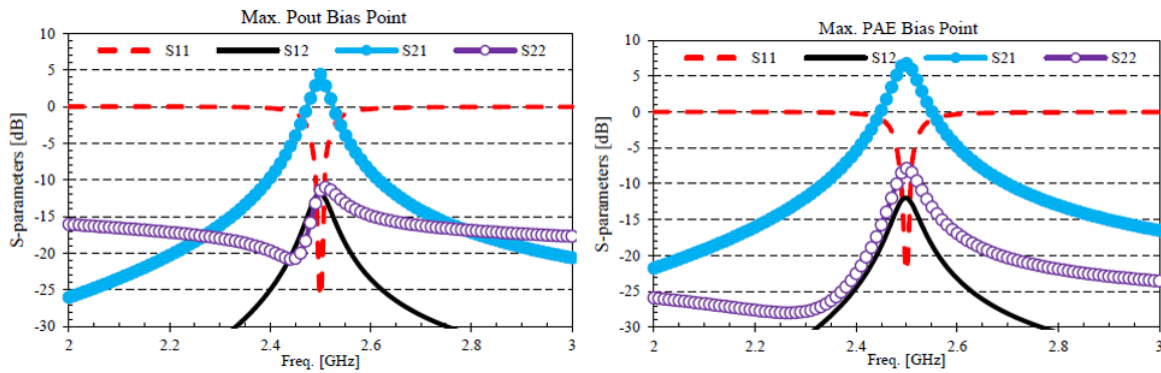


Fig. 2.36: S-parameters of the GFET with graphene synthesized on SiC PA for both max. PAE and  $P_{OUT}$  bias points.

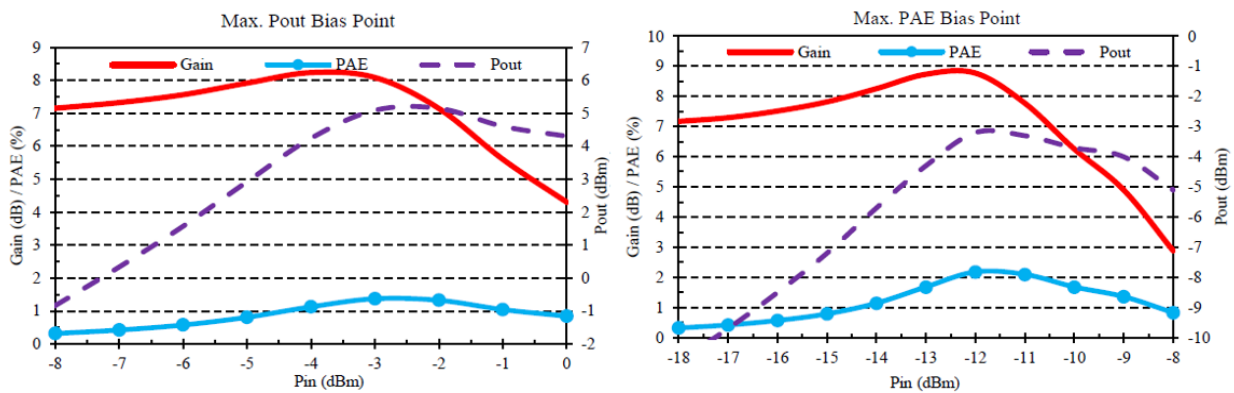


Fig. 2.37: Large signal results of the GFET with graphene synthesized on SiC amplifier for both max. PAE and  $P_{OUT}$  bias points.

7.2. GFET with CVD-grown Graphene on Si/SiO<sub>2</sub> Substrate PA Results

Fig. 2.38 (a) shows the S-parameters of the CVD-grown GFET amplifier. For the operating frequency range, the PA is unconditionally stable, the  $S_{11}$  and  $S_{22}$  parameters values are around -20 dB and the maximum gain  $S_{21}$  of this amplifier is 7.3 dB.

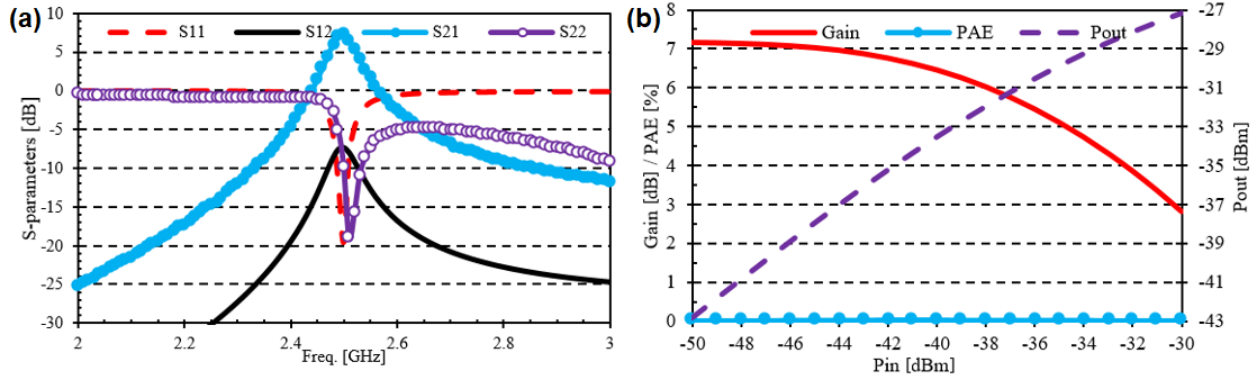


Fig. 2.38: (a) S-parameters results of the GFET with CVD-grown graphene amplifier (b) Large signal results of the GFET with CVD-grown graphene amplifier.

Large signal results (Fig. 2.38 (b)) show that the CVD GFET amplifier presents a maximum power gain of 7.2 dB. The output power of this amplifier is very low, its value is 2  $\mu$ W when the amplifier presents a 7 dB of power gain. Consequently, the PAE of this amplifier is also very low, its value does not exceed 0.1 %. These results can be foreseen from the large contact resistances and absence of current saturation of this transistor.

7.3. GFET with Mechanically Exfoliated Graphene and h-BN Dielectrics PA Results

Fig. 2.39 (a) shows the S-parameters results of the last amplifier. At 2.5 GHz, the  $S_{11}$  and  $S_{22}$  parameters values are around -10 dB and the maximum gain  $S_{21}$  of this amplifier is 12.3 dB, the highest reported among the three devices. Additionally, the PA is unconditionally stable.

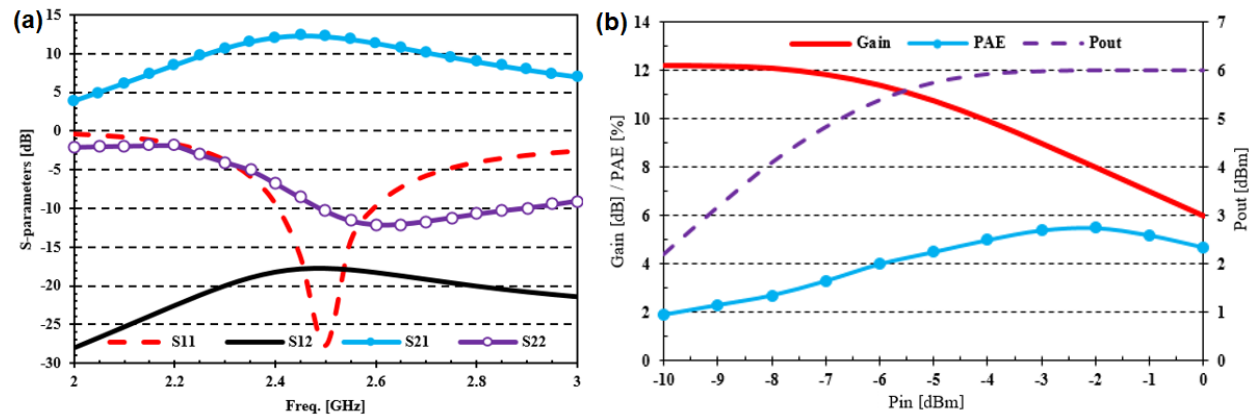


Fig. 2.39: (a) S-parameters results of the GFET with mechanically exfoliated graphene amplifier (b) Large signal results of the GFET with mechanically exfoliated graphene amplifier.

Large signal results (Fig. 2.39 (b)) show that the mechanically exfoliated GFET amplifier presents a maximum power gain of 12.1 dB, an output power of 6 dBm and a PAE of 5.6 %. This indicates that this device presents the best performances among the three transistors due to its current saturation and to the lower contact resistances.

## 8. Results Discussion

Table 2.5 summarizes the results of the graphene amplifier presented in this work.

Parameter	GFET synthesized on SiC		CVD GFET	Exfoliated GFET
	Max. P <sub>OUT</sub>	Max. PAE		
Freq. [GHz]	2.5	2.5	2.5	2.5
L [nm]	270	270	300	440
W [μm]	48	48	24	48
V <sub>DS</sub> [V]	3	1	1.5	-1.2
V <sub>GS</sub> [V]	2	-3	1.2	-2
Max. Gain [dB]	8.2	8.9	7.2	12.1
P <sub>OUT</sub> [dBm]	5.2	-3.2	-27	6
P <sub>DC</sub> [mW]	198.9	18.9	3	61.1
PAE [%]	1.4	2.2	0.01	5.6

Table 2.5: Performances of the graphene PAs.

### Gain

With a power gain between 7 and 12 dB at 2.5 GHz for a single stage, contrary to the general reputation, the gain of GFETs devices is remarkable and in the same order of magnitude than single stage silicon amplifiers. In fact, despite the high intrinsic resistances and the high output conductance, the gain is boosted due to the high electron mobility but at the expense of a higher drain current density.

### Output Power

Concerning the output power, the maximum value obtained is 6 dBm with the mechanically exfoliated device. 5.2 dBm is obtained with the GFET synthesized on SiC despite a supply voltage of 3 V. As described in Fig. 2.40, thanks to its low and constant output conductance on a large V<sub>DS</sub> range, the silicon CMOS reaches large saturated power (P<sub>SAT</sub>) with a large modulation of V<sub>DS</sub> and a small variation of I<sub>DS</sub> and its associated transconductance. On the other hand, in the graphene based devices, the power is obtained with a more balanced variation of I<sub>DS</sub> and V<sub>DS</sub>. In fact, the V<sub>DS</sub> variation around bias point is reduced compared to the CMOS and compensated by a larger variation of drain current. Unfortunately, this large variation of drain current results in a large variation of the transconductance, and introduces the saturation of the power gain.

### Power Added Efficiency

The first results of the efficiency of graphene amplifiers presented in this work allow us to draw the conclusion that the power added efficiency, which takes into account the output power and the DC power consumption, is low compared to the silicon counterpart.

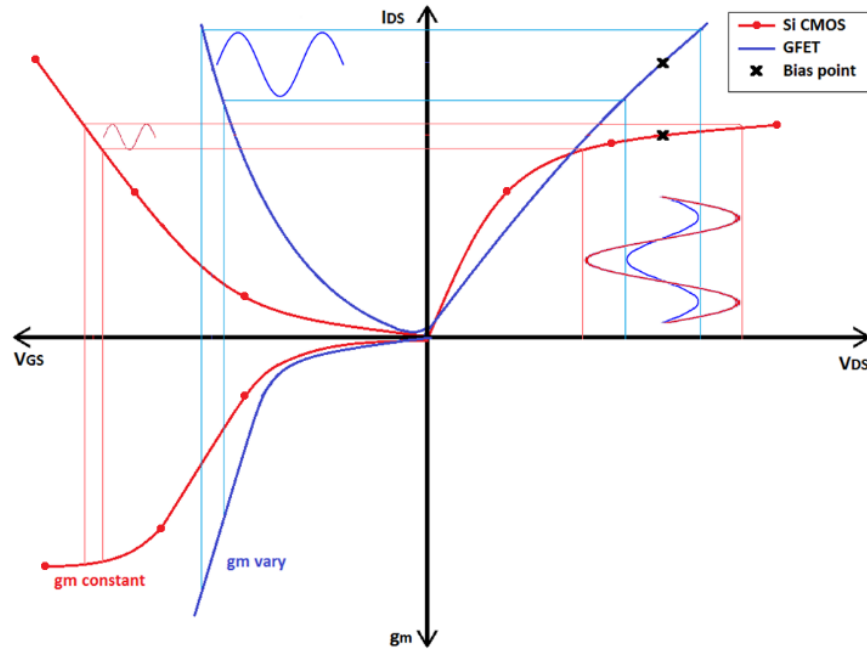


Fig. 2.40: GFET and Si CMOS characteristics comparison.

**Fabrication Methods**

The best results are obtained with the mechanically exfoliated device. However, exfoliated graphene is costly and mainly used for research purposes and not for commercial products. Although the CVD method is the most advantageous for mass production, until now, the large contact resistances and the absence of current saturation hinders this methods in RF amplifying applications. On the other hand, the synthesis on SiC method produces transistors with better current saturation and lower contact resistances and thus presents better RF amplification.

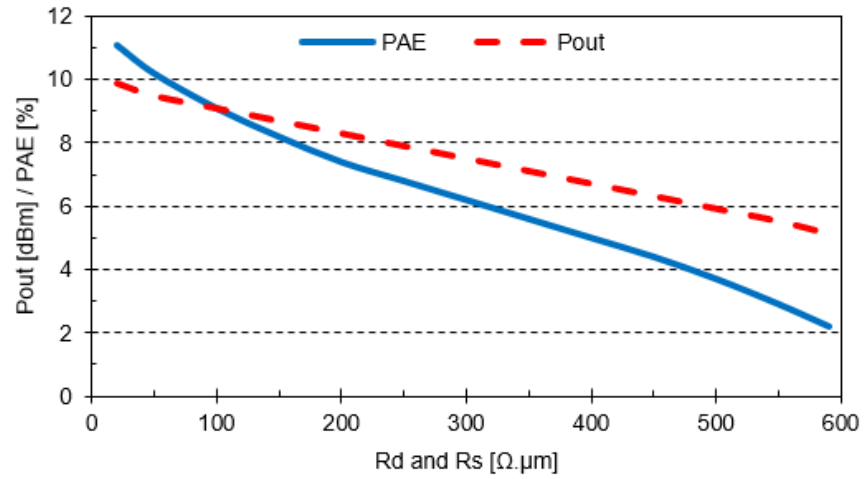
**Performances Improvement with Technological Projections**

With the advances of GFET fabrication process, lower contact resistances will be achieved, which will lead to lower power dissipation. For instance, changing the values of  $R_D$  and  $R_S$  from the actual value of  $590 \Omega \cdot \mu\text{m}$  to the ITRS projections of  $20 \Omega \cdot \mu\text{m}$  in the compact model of the GFET synthesized on SiC, will allow the amplifier with graphene on SiC to achieve 10 dBm of output power and 11.2 % of PAE (Fig. 2.41).

Additionally, improving the current saturation of the graphene devices, and consequently decreasing the high knee voltage, will allow higher output voltage swings and thus better performances.

These observations, can lead us to conclude that GFET devices could find their way to RF power amplification depending on the progress of research activities on its contact resistances and current saturation.

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY



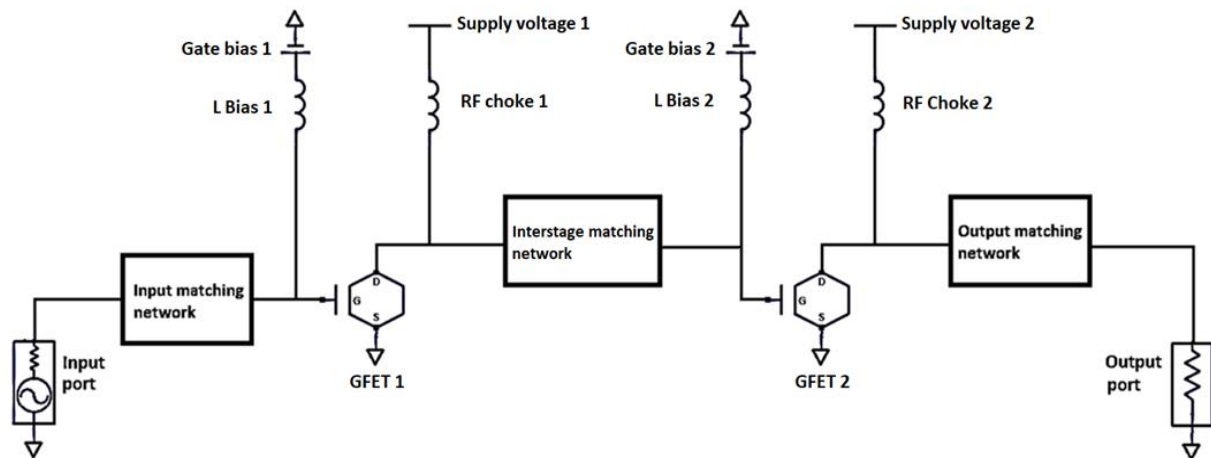
*Fig. 2.41: Variation of the output power and PAE of the GFET synthesized on SiC amplifier in function of  $R_D$  and  $R_S$ .*

## 9. Multistage GFET Amplifiers

In the sections above, single stage graphene amplifiers were designed in order to evaluate the graphene technology for power amplification.

Subsequently, two stage 2.5 GHz graphene amplifiers were designed and layouted in order to see the performances obtained in this technology while combining stages. For non-repetition purposes, we present only the layout of the two stages GFET Synthesized on SiC Substrate.

This GFET was chosen in accordance with the discussion on fabrication methods in the part 8 of this chapter. In fact, this device's fabrication method is more pertinent for mass production than the mechanical exfoliation, and presents better RF amplification than the CVD device.



*Fig. 2.42: Schematic of the two-stage common source GFET amplifier.*

Fig. 2.42 shows the schematic of the two-stage amplifier. The amplifier consists of two common source transistors.

First the power stage is designed and optimized for maximum output power. Then the second stage is designed and optimized for maximum power gain. The output impedance of the first stage is then matched to the input impedance of the second stage.

Fig. 2.43 shows the layout of the amplifier. The elements used in the circuit are 9 nH, 6 nH, 0.6 nH and 0.5 nH inductances, with a 650 fF, 460 fF and 370 fF capacitances and four 4 pF decoupling capacitances.

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

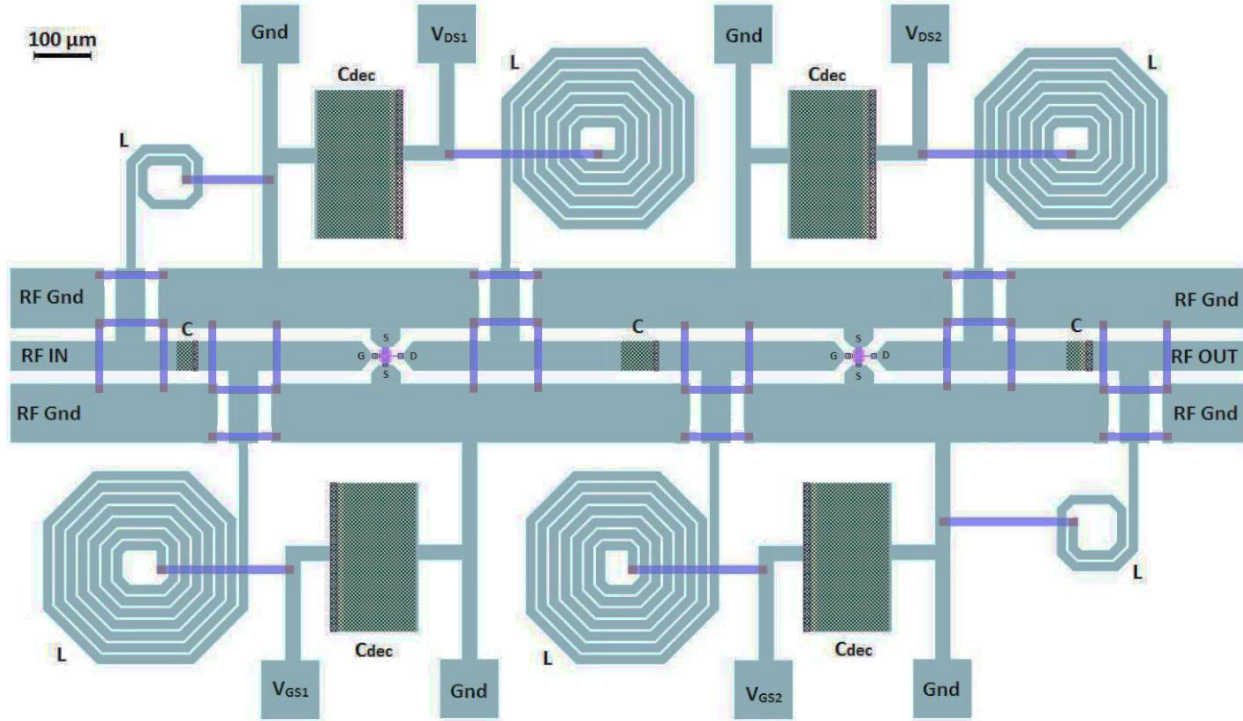


Fig. 2.43: Layout of the two stages GFET synthesized on SiC amplifier ( $2 \times 1.2 \text{ mm}^2$ ).

Fig. 2.44 shows the S-parameters of the amplifier. The  $S_{11}$  and  $S_{22}$  parameters are lower than -10 dB at 2.5 GHz indicating the reliable matching and insignificant losses. The gain  $S_{21}$  is 19 dB at 2.5 GHz.

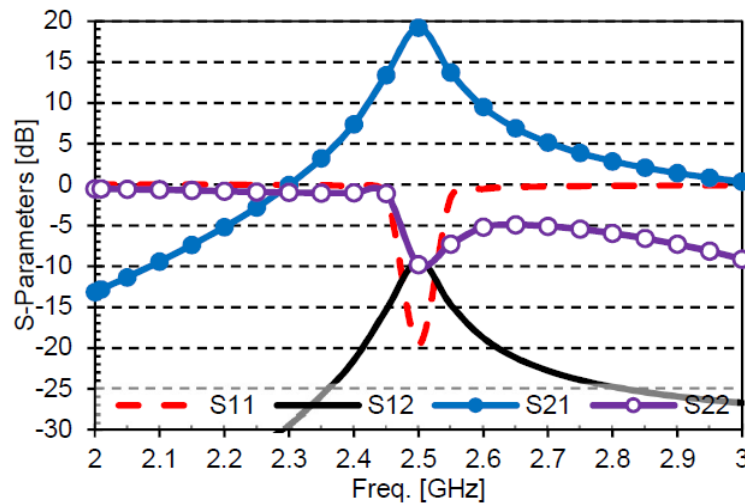


Fig. 2.44: S-parameters results of the two stages GFET synthesized on SiC amplifier.

Concerning the large signal performances (Fig. 2.45), the maximum power gain is 18.2 dB, the maximum output power is 5.1 dBm. The PAE of this amplifier is 2 %, due to the 158 mW of DC power consumption. Finally, the output 1 dB compression point (OCP1) is 5 dBm indicating the high linearity of this amplifier.

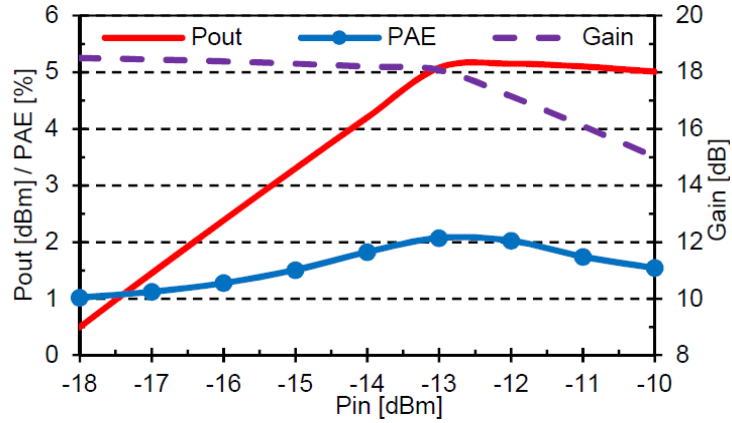


Fig. 2.45: Large signal results of the two stages GFET synthesized on SiC amplifier.

These results show that combining two stages of the GFET with graphene synthesized on SiC and choosing the optimum bias voltages, results in a better output power/efficiency tradeoff. In fact, the obtained output power and PAE approach the best results obtained in a single stage amplifier. Moreover, the power gain is boosted since it is the sum of the gain of the two stages with the first stage being optimized for maximum gain.



### Conclusion

In this chapter, we presented a study and analysis of the graphene technology in power amplification. In fact, while graphene transistors have been extensively studied and developed since 2007, performances of graphene transistors in circuit level, particularly amplifiers, remained unclear.

Three 2.5 GHz integrated common source power amplifiers, based on three graphene FETs with different fabrication methods, were designed with accurate transistor modeling and electromagnetic simulations. Results show power gains ranging between 7 and 12 dB per stage. The maximum output power and PAE reported for a single stage are 6 dBm and 5.6 % respectively obtained with the GFET with mechanically exfoliated graphene. Results were discussed and analyzed, and projected with the GFET technological enhancements. Then, two stage GFET PA were designed. Results show the advantage of stage combining in terms of power gain, while achieving better tradeoffs between the performances. Given the short history of graphene transistors the power gain of these devices is remarkable. However, the output power and efficiency of these devices hinder their potential in RF PA applications.

Nevertheless, the development of the GFET has passed a lengthy way since peeling graphite with scotch-tape. Nowadays, it is possible to fabricate graphene integrated circuits in wafer-scale. However, despite the progress in graphene transistors, there are still many issues that need to be solved before graphene has commercial potential. In particular, improving the current saturation and developing a fabrication process for achieving low contact resistances is absolutely vital for graphene power amplifiers. Promising directions that could be pursued in graphene research are exploring transistor structures such as the Graphene Bipolar Transistors or to complement the conventional semiconductors instead of trying to replace them.

Finally, this work and further technology improvements will pave the way for graphene's potential in RF applications.

## CHAPTER II: POWER AMPLIFIERS ON THE GRAPHENE TECHNOLOGY

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## CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

### Table of Contents

<i>Introduction</i>	98
<i>1. The 28 nm CMOS FD-SOI Technology</i>	99
<i>1.1. CMOS Technologies</i>	99
<i>1.2. The CMOS FD-SOI Transistor</i>	100
<i>1.3. The 28 nm FD-SOI Transistors Types and Body Biasing</i>	101
<i>1.4. The 28 nm FD-SOI Transistor Characteristics</i>	103
<i>1.5. The 28 nm FD-SOI Technology Back-End of Line</i>	104
<i>1.6. The 28 nm FD-SOI Technology Design Rules</i>	105
<i>2. Overview of 5G Power Amplifiers</i>	106
<i>2.1. 5G Power Amplifier Specifications</i>	106
<i>2.2. State of the Art of CMOS 5G Power Amplifiers at 28 GHz</i>	108
<i>2.3. Review of State of the Art 5G CMOS Power Amplifiers</i>	111
<i>3. Review of Power Amplifier Architecture for 5G Applications</i>	113
<i>3.1. Highly Efficient Modes of Operation</i>	113
<i>3.2. Sinusoidal Classes Optimization</i>	114
<i>3.3. State of the Art of Class J Amplifiers</i>	115
<i>4. Design and Analysis of Class J Power Amplifiers</i>	118
<i>4.1. Class J Amplifier Theory</i>	118
<i>4.2. Class J Amplifier Design</i>	120
<i>4.3. Class J Amplifier Versus the Frequency</i>	121
<i>5. Power Amplifier Design Methodology</i>	123
<i>6. Power Amplifier Design</i>	125
<i>6.1. Transistor Sizing and Layout</i>	125
<i>6.2. Power Amplifier Topology</i>	127
<i>6.3. Class J Power Stage Design</i>	128
<i>6.4. Driver Stage and Matching Networks Design</i>	130
<i>6.5. Layout of the Amplifier</i>	131
<i>7. Post-layout Simulation Results</i>	133
<i>8. Circuit Measurement</i>	135
<i>Conclusion</i>	139
<i>References</i>	140

### Introduction

This chapter addresses the second choice of orientation of this thesis, that is the study and design of power amplifiers on advanced technologies for 5G applications. The technology chosen is the 28 nm CMOS FD-SOI. This advanced technology node is very promising to substitute the conventional CMOS transistor in many applications. In addition, the 28 nm CMOS FD-SOI offers great opportunities for circuit designers such as the back-gate basing. Therefore, this technology is evaluated and used for designing a linear, highly efficient and wideband power amplifier for 5G applications.

This chapter begins with the presentation of the 28 nm CMOS FD-SOI technology. Transistor types, DC and RF characteristics, back-gate biasing and back-end of lines of this technology are discussed.

In the second part of the chapter, 5G power amplifiers specifications are studied, and state of art CMOS 5G power amplifiers are presented. This leads to the next part of the chapter which consists of evaluating different amplifier modes in order to satisfy the 5G requirements. Afterwards, in the fourth part of the chapter, the class J mode is addressed in details, its theory and design are presented.

Subsequently, the amplifier design methodology is described extensively. Then, post-layout simulation results are presented and evaluated. Finally, circuit measurements are presented, analyzed and discussed.



## 1. The 28 nm CMOS FD-SOI Technology

### 1.1. CMOS Technologies

CMOS technologies are particularly interesting for mass markets. The objective is ultimately to integrate all the functions of a transceiver (radiofrequency, analog and digital) on a single System on Chip (SoC), in order to reduce the costs significantly (Fig. 3.1). In fact, the majority of the transceiver blocks at millimeter frequencies have been integrated successfully on the same substrate in CMOS technology [III.1].

By far, power amplifiers are the most difficult radio transceiver blocks to integrate in CMOS. In fact, the PA design requires simultaneously low-loss passives and high-voltage devices and is usually implemented in a high cost technology that is designed for RF applications. On the other hand, standard CMOS is inexpensive but it is also optimized for digital circuits with high substrate losses as well as low supply voltage devices.

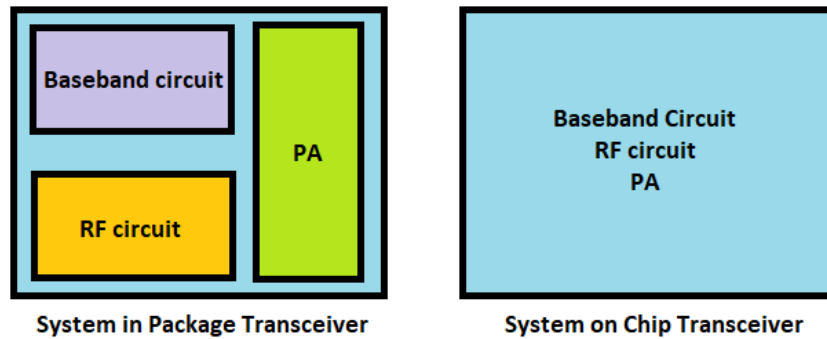


Fig. 3.1: System in Package versus System on Chip transceiver integration.

Fig. 3.2 shows a comparison between CMOS, SiGe and GaAs technologies. III-V technologies, such as GaAs or InP, are very often used at millimeter wave frequencies because they provide much better power performance than the CMOS technology. SiGe technology is a good alternative to III-V components. Nevertheless, SiGe technologies remain expensive and present much lower integration density than the CMOS.

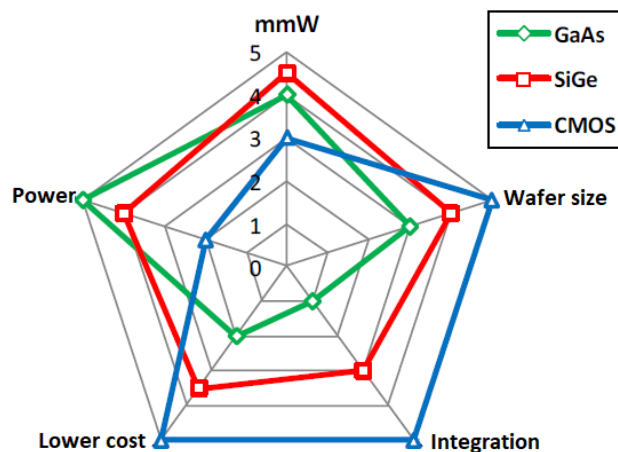


Fig. 3.2: CMOS, SiGe and GaAs technologies comparison [III.2].

## CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

Therefore, driven by the very high demand for integrated CMOS products, the performances of MOS transistors have constantly been improved thanks to its scaling. Particularly, the cut-off and maximum oscillation frequencies have continuously increased, allowing better RF performances.

Yet, as discussed in Chapter I, the scalability of transistors encounters inevitable physical barriers. First, the channel length cannot be scaled down below the atomic scale of some nanometers. Second, as the transistor shrinks, unwanted leakage current flows, this leakage current has been increasing with every new generation of transistors, and represents a growing proportion of power consumption.

Consequently, researchers are intensively working on advanced CMOS architectures. According to the International Technology Roadmap for Semiconductors (ITRS) the two main solutions, FinFETs and FD-SOI technologies, will allow the continuous improvement of MOS RF performances (Fig. 3.3).

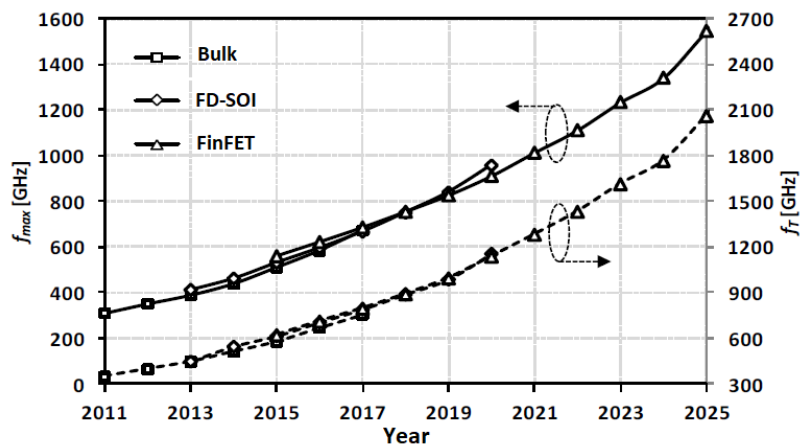


Fig. 3.3: Forecast of the  $f_T$  and  $f_{max}$  of the MOS technologies [III.3].

### 1.2. The CMOS FD-SOI Transistor

Introduced in the 1980s to compensate the possible interferences produced by strong radiations in space applications, Silicon on Insulator (SOI) technology most often used a sapphire substrate. At that time, the use of this technology had already been identified as a possible way to improve the performance of CMOS beyond the improvements introduced by the transistor scaling.

After more than a decade, SOI technology found its way for commercial applications. This was largely due to the improvement of the quality of the substrates used, and most importantly the progress made in CMOS technology. SOI technology is considered by many as the future solution for high performance applications with high integration density.

Fig. 3.4 shows a cross section of a bulk and Fully Depleted SOI (FD-SOI) transistors. In FD-SOI the innovation lies in the buried oxide insulator layer positioned just below the channel. This layer confines the electron when flowing from the source to the drain, reducing the leakage current from the channel to the substrate. Moreover, this layer eliminates the need to add dopants to the channel, making it fully depleted and thus reducing the process variability.

## CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY



Fig. 3.4: CMOS bulk and FD-SOI transistors cross section.

Unlike FinFETs, FD-SOI transistors are planar. These transistors are fabricated in a very thin (7 nm) layer of silicon sitting over a 25 nm layer of buried oxide (BOX) [III.4]. This is why this technology is named Ultra-Thin Body and Buried oxide (UTBB).

The 28 nm FD-SOI process flow is a modified 28 nm bulk process using the same Back-End of Line (BEOL) and same gate module. There is less than 20 % change with respect to a classical CMOS bulk flow. At this node, more than 10 % of the process steps and seven masks are saved, resulting in an overall manufacturing process cost saving of 10% [III.5]. In Fact, several process steps, specifically channel implants, halo implants and masking levels are removed compared to the traditional 28 nm bulk technology because of the undoped FD-SOI channel.

Moreover, to be compliant with already existing designs developed in bulk technology, a hybrid solution has been introduced enabling the co-integration of bulk and SOI devices on the same die. The hybrid section is obtained prior to device fabrication by etching the top silicon and BOX as shown in Fig. 3.5.

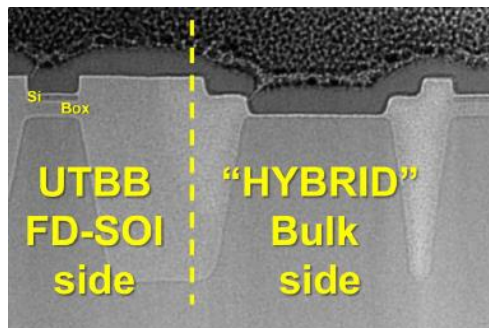


Fig. 3.5: Hybridization in UTBB FD-SOI technology.

### 1.3. The 28 nm FD-SOI Transistors Types and Body Biasing

The 28 nm UTBB FD-SOI offers two types of transistors as seen in Fig. 3.6.

- RVT (Regular Voltage Threshold) or conventional well.
- LVT (Low Voltage Threshold) or flip well.

For an LVT transistor, a positive body bias  $V_{BB}$  (also called Forward Body Bias or FBB) reduces the threshold voltage of the transistor at a rate of 85 mV/V, increasing the transconductance at the same time. The breakdown voltage of FBB is around 3 V. A negative voltage (Reverse Body Bias or RBB) can also be applied, as long as it does not conduct the parasitic diodes (below 0.3 V).

### CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

For an RVT transistor, a negative body bias  $V_{BB}$  RBB increases the threshold voltage and reduces the leakage currents. The dynamic range of this voltage is from -3 V to  $V_{DD}/2 + 300$  mV.

The LVT transistor is used in this work since lower threshold voltage is highly needed for power amplification.

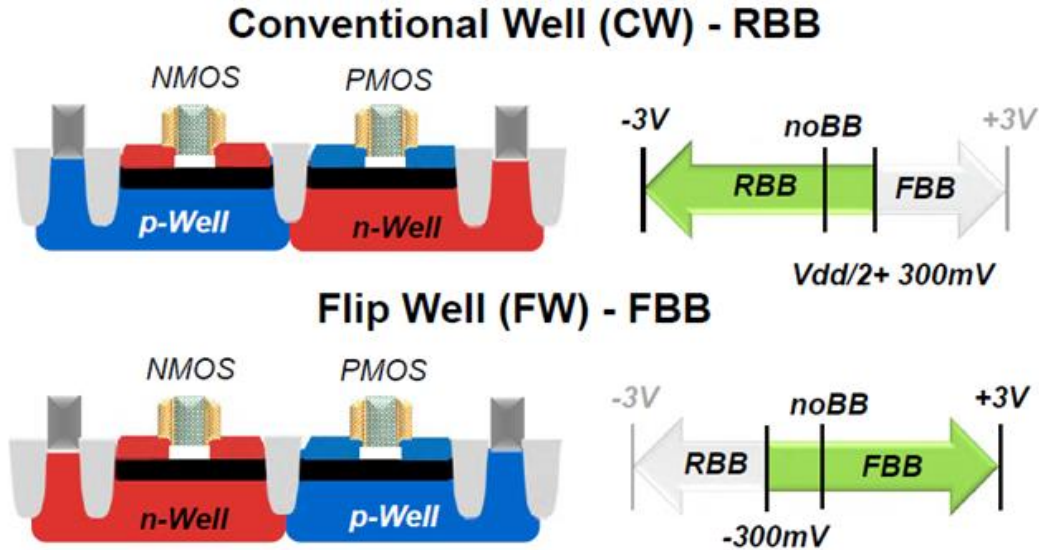


Fig. 3.6: FD-SOI conventional well and flip well transistors with body biasing ranges.

Body biasing (back-gate biasing) is the key feature of the FD-SOI technology. It consists in applying a voltage just under the BOX of the transistor in order to shift its threshold voltage to either gain in performance or reduce the leakage power consumption. The principle is well known and widely applied in bulk technology [III.6] but unfortunately less and less efficient in advanced CMOS technologies. One of the major advantages in UTBB FD-SOI is that the body bias efficiency does not degrade with scaling: it can indeed be maintained or increased by the modulation of the silicon film and buried oxide thicknesses at each technology node. Moreover, thanks to its better electrostatics, UTBB FD-SOI exhibits a higher body factor over its bulk counterpart, 85 mV/V versus 25 mV/V (Fig. 3.7).

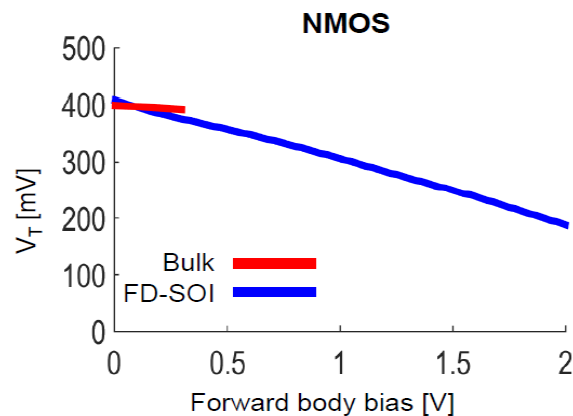


Fig. 3.7: Variation of the forward body bias in bulk and FD-SOI NMOS.

1.4. The 28 nm FD-SOI Transistor Characteristics

Fig. 3.8 shows the output characteristics measurements ( $I_{DS}$ ,  $V_{DS}$ ) for different  $V_{GS}$  for LVT (Low Voltage Threshold) transistors in 28 nm Bulk and 28 nm FD-SOI. It is clear that the drain current in FD-SOI is higher than the bulk transistor for the same biasing points ( $V_{DS}$ ,  $V_{GS}$ ). Moreover, the current saturation is improved in FD-SOI.

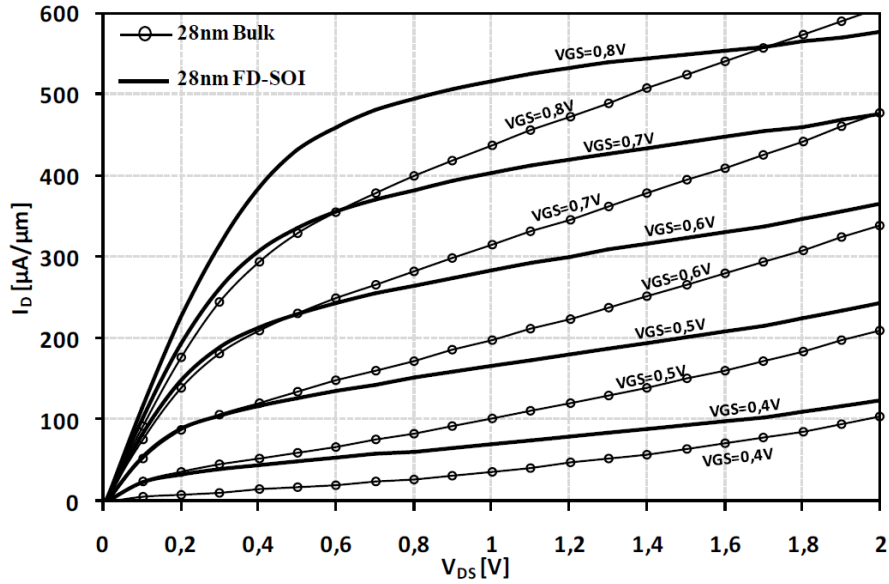


Fig. 3.8:  $I_{DS}$  versus  $V_{DS}$  measurements for LVT transistors in 28nm Bulk and 28nm FD-SOI [III.2].

Fig. 3.9 shows the measurements of the current gain ( $H_{21}$ ) and Maximum Stable Gain / Maximum Available Gain (MSG/MAG) for LVT transistors in 28nm Bulk and 28nm FD-SOI. These curves show that the FD-SOI achieves higher gain than the bulk transistor at higher frequencies. In addition, both  $f_T$  and  $f_{max}$  of the 28 nm FD-SOI transistor surpass 300 GHz.

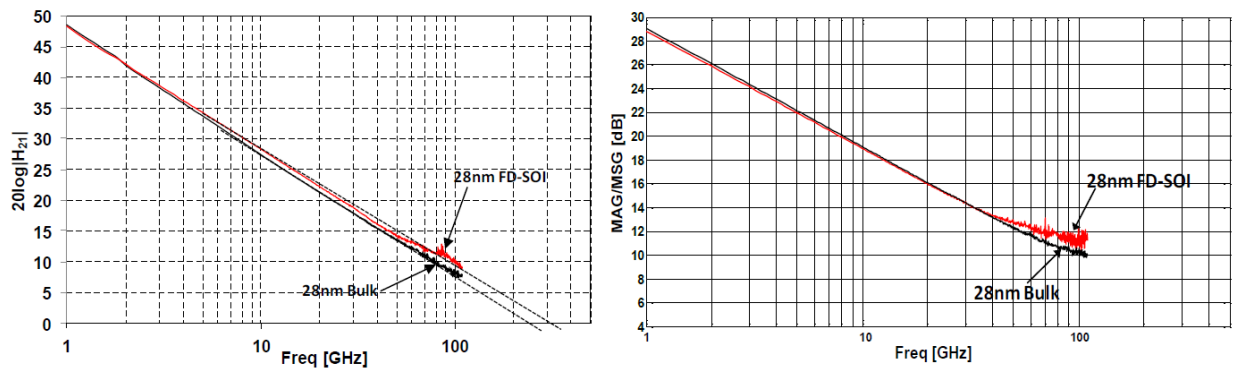


Fig. 3.9: Measurements of  $H_{21}$  and MSG/MAG for LVT transistors in 28 nm Bulk and 28 nm FD-SOI [III.2].

### 1.5. The 28 nm FD-SOI Technology Back-End of Line

Before 2017, the 28 nm FD-SOI technology presented a BEOL of 10 metal layers with an Aluminum cap layer (Alucap) (LB in Fig. 3.10). The 10 metals layers are divided into 3 categories with same properties and sizes (Fig. 3.10):

- 6 thin metal layers (M1 to M6).
- 2 medium thickness metal layers (B1 and B2).
- 2 thick metal layers (IA and IB).

The lower layers (M1 to B2) being too thin, they are only used in resistances, capacitances and for connecting the transistors to the passive networks.

The top metal layers (IA and IB) and the Alucap layer are used for RF components design such as transmission lines, inductances and transformers. In fact, the resistance of these elements must be as low as possible.

In 2017, an 8 metal BEOL was introduced by removing the medium thickness layers B1 and B2. This will result in the decrease of the manufacturing time and cost. But on the other hand, the passives quality will be reduced since the top layers will approach the substrate resulting higher parasitic capacitances.

In this work, the 8 metals BEOL is used.

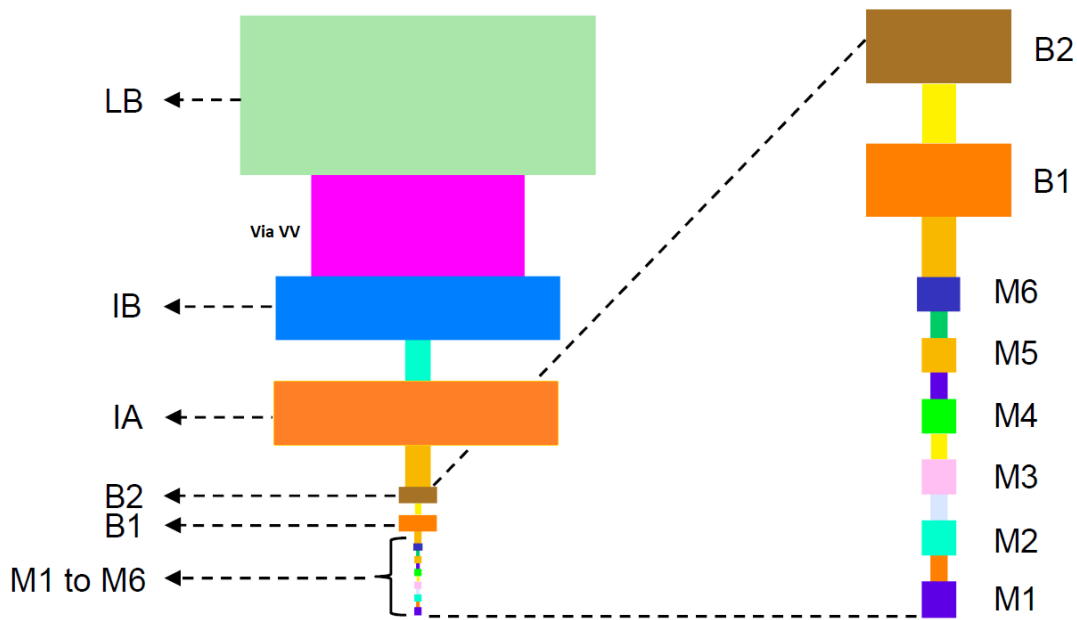


Fig. 3.10: The ten metals version of the Back-end of line of the 28 nm FD-SOI technology.

### 1.6. The 28 nm FD-SOI Technology Design Rules

One of the main difficulties in designing circuits with advanced technologies is the number of design rules to be respected (Fig. 3.11). With channel lengths larger than 65 nm, fewer than 1000 rules are counted per technology. As the channel length decreases, the number of rules grows rapidly. In fact, the 28 nm FD-SOI technology presents more than 5000 design rules. These rules have a considerable impact on the design time of the circuit.

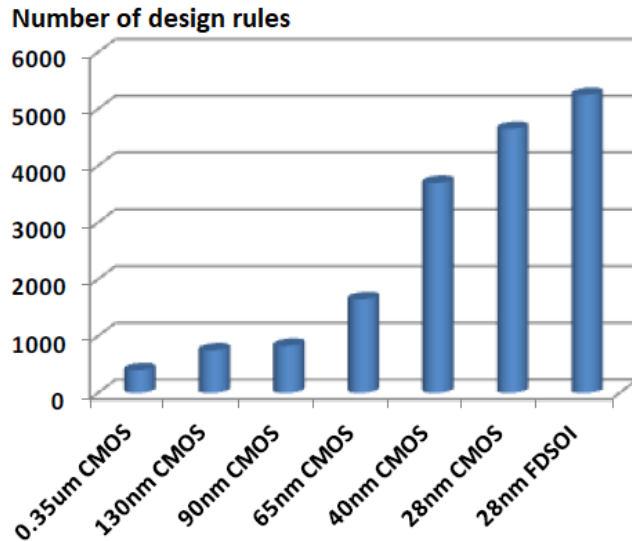


Fig. 3.11: Number of design rules to be respected per CMOS technology node [III.2].



## 2. Overview of 5G Power Amplifiers

### 2.1. 5G Power Amplifier Specifications

Fig. 3.12 shows the final frequency candidates above 6 GHz selected for 5G standardization announced during the World Radio Conference 2015. As discussed in Chapter I, one of the major objectives of the 5G is attaining data rates of multigigabits per second, and these rates are not achievable without a wideband frequency of operation. In fact, while wireless communication has been focused on specified RF bandwidths due to the congested spectrum allocations, the large bandwidth is one of the most desired specifications for the next generation systems.

The first two frequency bands candidates shown in Fig. 3.12 present many advantages compared to the others. In fact, they offer better wave propagation, and lower atmospheric attenuation. In addition, most of the works and studies on the 5G are carried out in this frequency band [III.7 – III.11].

Consequently, in this chapter, we aim to design an integrated power amplifier centered at 28 GHz, and covering the first two frequency bands candidates shown in Fig. 3.12 from 24.25 to 33.4 GHz.

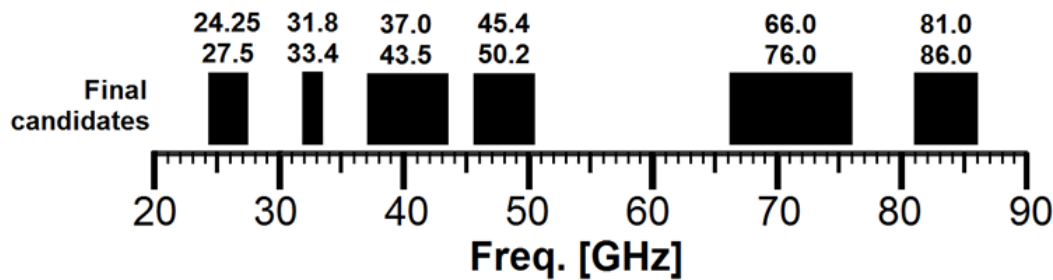


Fig. 3.12: The final 5G frequency candidates above 6 GHz.

Another main objective of our PA design is to achieve high efficiency. As mentioned earlier, enhancing the PA efficiency and reducing power consumption is critical for the 5G standard.

Fig. 3.13 shows the number of published papers on RF power amplifiers per year from 1969 to 2013. The red curve shows that the trend of PA research is in constant rise. In addition, since the beginning of the 21<sup>st</sup> century, this trend is on an increasing acceleration. In fact, this tendency is largely driven by the very high consideration on reducing the PA power consumption.

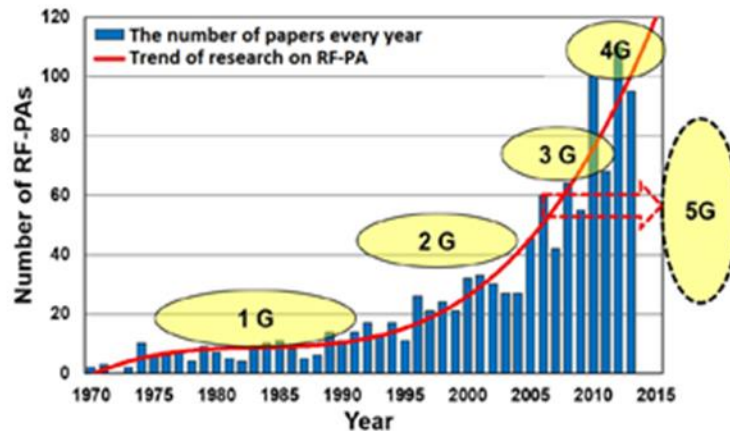


Fig. 3.13: Number of published papers on RF PAs per year [III.12].



### CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

Another key feature demanded for the 5G power amplifiers is the linearity. In fact, while the modulation techniques to be used in the 5G is not defined yet, the use of complex multicarrier modulation techniques such as the OFDM currently used for the 4G systems is the most probable. These types of modulations result in a high value of Peak-to-Average Power Ratio (PAPR) of the signal imposing severe requirements on the linearity of the power amplifiers.

Nonetheless, the compromise between linearity and consumption is well known in power amplifier design. As shown in Fig. 3.14, the high efficiency operation of the PA is achieved in the non-linear region. This fact exemplifies a strong trade off in power amplifier design between the linearity and the efficiency.

Thus, researchers and power amplifier designers are faced with finding new technological solutions for reducing this tradeoff and improving the PAE at back-off power (BO) operation.

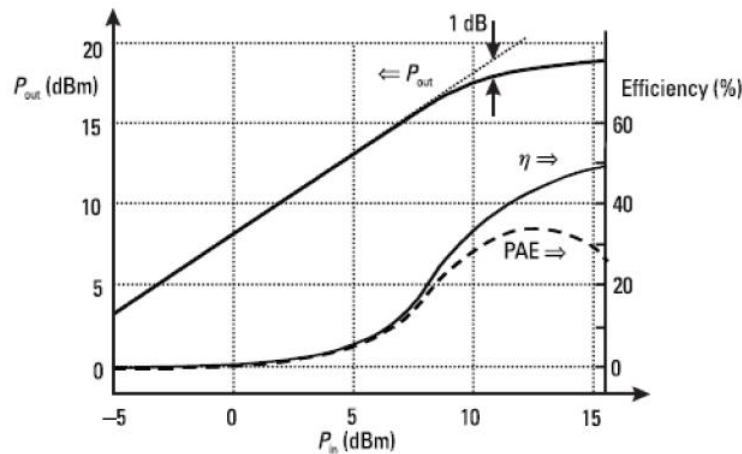


Fig. 3.14: Example of the typical output power and efficiency curves in a PA [III.13].

To summarize, the ideal 5G PA will have the following characteristics:

- Low power consumption and high PAE.
- Linear operation.
- Large bandwidth.

In addition, the reconfigurability of the PA is highly desirable in order to achieve the maximum performances with the different modes and frequencies of operation.

### 2.2. State of the Art of CMOS 5G Power Amplifiers at 28 GHz

In this section, we present the state of art of the CMOS power amplifiers operating in the 28 GHz band.

In [III.14] a PA is implemented on the 28 nm CMOS bulk technology. The PA is composed of two differential common source class AB stages. At the input and output of the PA, two baluns perform the conversion of the single-ended mode to the differential mode (and vice versa) as well as the impedance matching (Fig. 3.15).

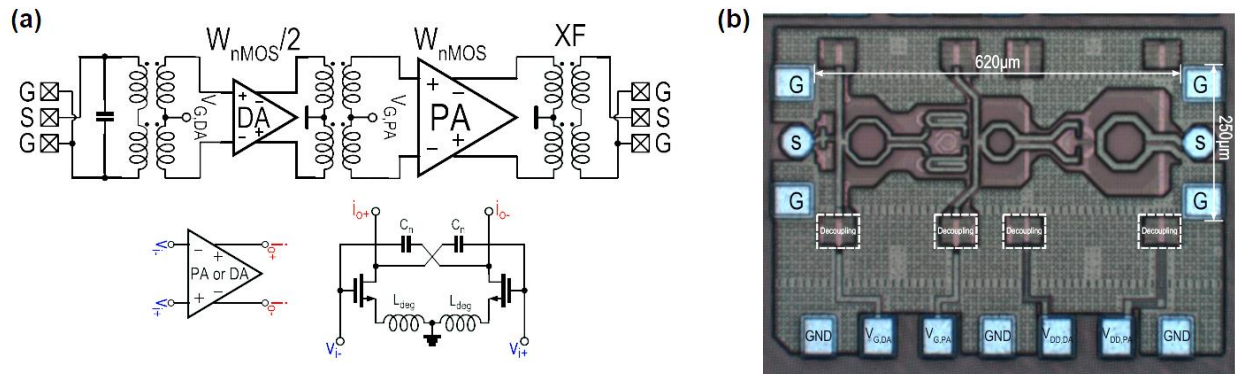


Fig. 3.15: PA in [III.14] (a) Schematic of the circuit (b) Die micrograph.

At 30 GHz, this amplifier presents a  $P_{SAT}$  and OCP1 of 14 and 13.2 dBm respectively, with a power gain of 15.7 dB and a PAE of 35.5 % (Fig. 3.16 (a)). The efficiency at 8 dB back-off operation from  $P_{SAT}$  is 12 %. The 3 dB bandwidth of this circuit is from 27 to 31 GHz, and the peak PAE surpasses 30 % across this band (Fig. 3.16 (b)).

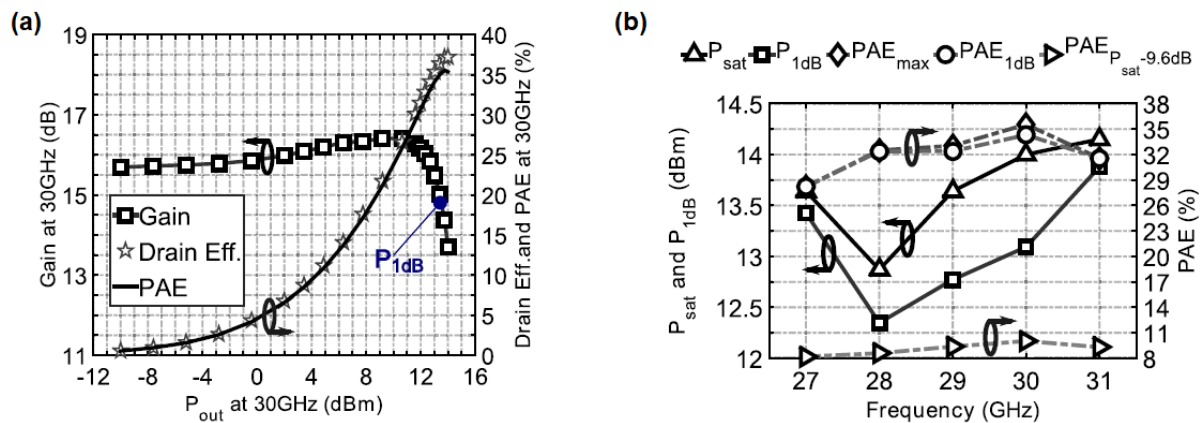


Fig. 3.16: PA in [III.14] (a) Gain, drain efficiency and PAE in function of the output power at 30 GHz (b) Power and efficiency performances versus the frequency.

### CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

Another 28 nm CMOS bulk PA was developed in [III.15] operating at 28 GHz. This amplifier is composed of one class AB cascode stage and also uses the differential structure (Fig. 3.17).

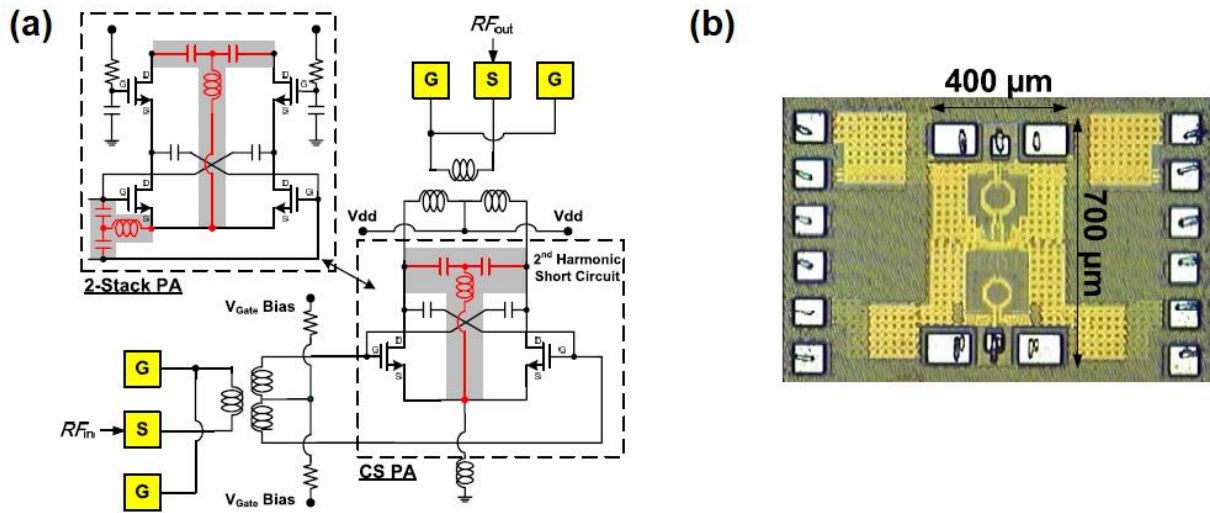


Fig. 3.17: PA in [III.15] (a) Schematic of the circuit (b) Die photograph.

This differential PA presents at 28 GHz a  $P_{SAT}$  of 19.8 dBm and an OCP1 of 18.6 dBm, a maximum and 8 dB back-off PAE of 43.3 % and 16 % respectively and a power gain of 13.6 dB (Fig. 3.18 (b)). The frequency performance of this PA is not studied. However, the S-parameters show a 3 dB bandwidth between 26 and 31 GHz (Fig. 3.18 (a)).

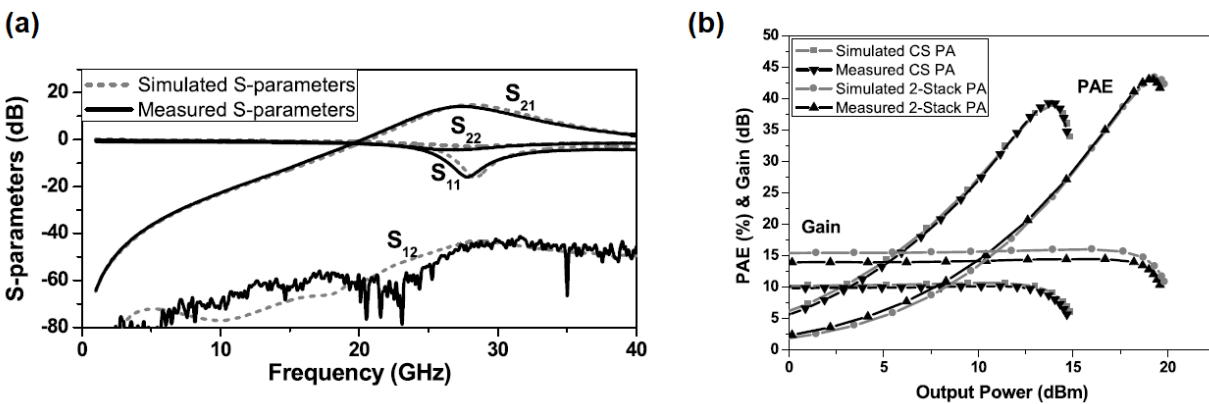


Fig. 3.18: PA in [III.15] (a) Measured and simulated S-parameters (b) Measured and simulated large-signal characteristics at 28 GHz.

### CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

Lastly, a 28 GHz PA is developed in [III.16] with the 28 nm CMOS FD-SOI technology. The PA uses a balanced architecture with integrated quadrature hybrid couplers for 5G phased array applications (Fig. 3.19 (a)). Each power cell (Fig. 3.19 (b)) is based on class AB segmented biased push-pull topology.

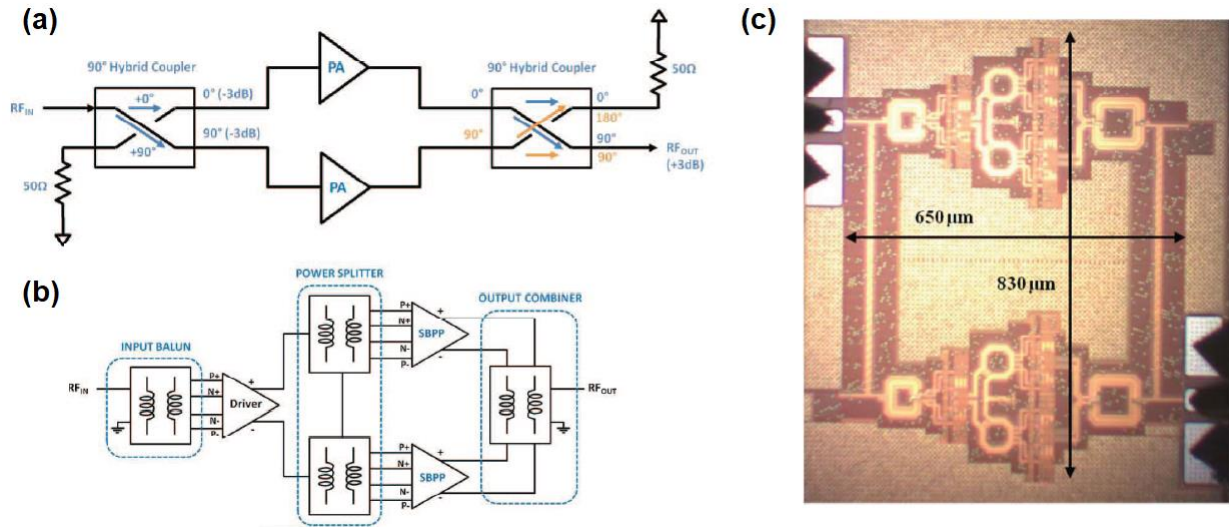


Fig. 3.19: PA in [III.16] (a) Block diagram of the balanced PA (b) Schematic of the PA power cells (c) Die photograph.

This amplifier achieves at 27 GHz, a saturated output power of 18.7 dBm and a peak PAE of 12.4 % with 17.5 dB of power gain (Fig. 3.20 (b)). S-parameters of this PA (Fig. 3.20 (a)) show a 3 dB bandwidth between 26 and 28 GHz.

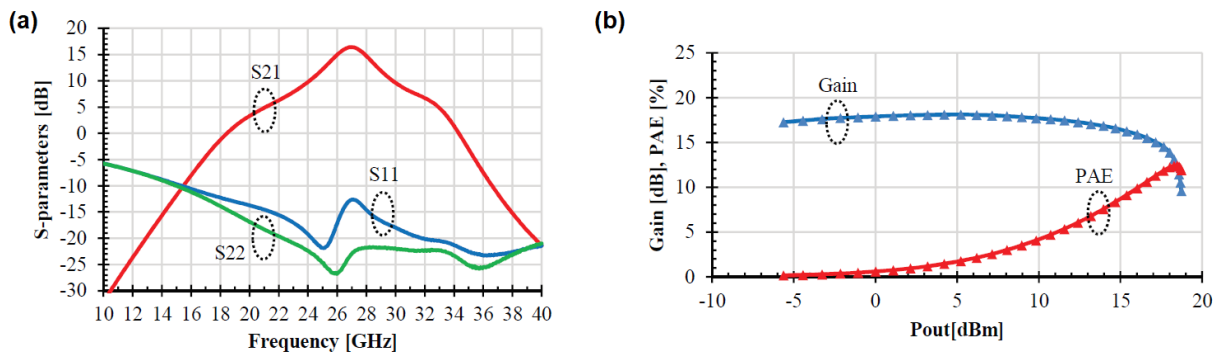


Fig. 3.20: PA in [III.16] (a) Measured S-Parameters (b) Power gain and PAE versus the output power at 27 GHz.

### 2.3. Review of State of the Art 5G CMOS Power Amplifiers

Table 3.1 summarizes the performances of the state of art CMOS power amplifiers operating in the 28 GHz band. Up to our knowledge, currently only three PAs are demonstrated in this frequency range, all using 28 nm CMOS technology nodes (Bulk and FD-SOI).

Increasing the maximum efficiency and the efficiency at back-off operation was one of the main objectives of these demonstrated PAs. [III.14] and [III.15] reported highly efficient PAs with 35.5 and 43.3 % of maximum PAE respectively.

In addition, to attain the 5G high linearity requirements, all the demonstrated PAs used the sinusoidal class AB. Highly efficient classes such as classes E and F were not used since they offer lower linearity.

In Table 3.1, the percent bandwidth is defined by:

$$BW [\%] = 100 \times \frac{f_H - f_L}{f_c} \quad (3.1)$$

With  $f_c$  the frequency where the power gain reaches its peak, and  $f_H$  and  $f_L$  are the high and low frequencies where the gain decreases 3 dB from its maximum value.

As seen in Table 3.1, the demonstrated 28 GHz amplifiers don't show a particularly wideband behavior with the percentage bandwidth ranging between 7 and 14 % for the three amplifiers.

Concerning the PA structure, despite the wide usage of the single-ended structure, no CMOS single-ended power amplifier is demonstrated in the 28 GHz band, only differential and balanced structures are used. This is largely due to increase the PA output power, since CMOS devices present lower power at higher frequencies. Another main reason is attributed to the ground return path (Fig. 3.21). In fact, while laying out the amplifier, an inductance is introduced between the source of the transistor and the ground. Since the inductance is proportional to the frequency, this inductance becomes very problematic at higher frequencies. However, thanks to its symmetric structure, the differential amplifier eliminates the effect of the ground-source inductance since the currents of the two transistors are recombined in quadrature of phase in the source-ground path.

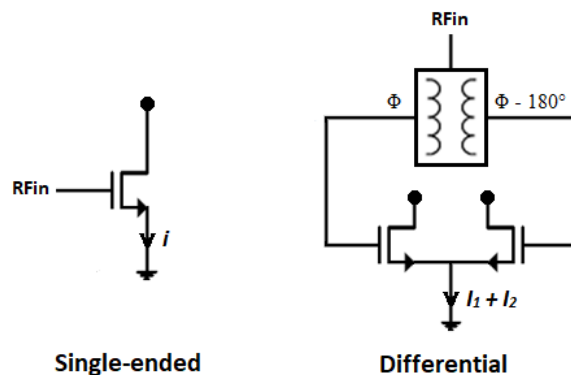


Fig. 3.21: Source current in single-ended and differential structures.

### CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

Parameter	[III.14]	[III.15]	[III.16]
Technology	28 nm CMOS Bulk	28 nm CMOS Bulk	28 nm CMOS FD-SOI
Structure	Differential	Differential	Balanced
Class	AB	AB	AB
Freq. [GHz]	30	28	27
BW [%]	14	11	7
BW [GHz]	27.4 – 31.2	27 – 30	26 – 28
Gain [dB]	15.7	13.6	17.5
P <sub>SAT</sub> [dBm]	14	19.8	18.7
PAE <sub>max</sub> [%]	35.5	43.3	12.4
PAE 8 dB BO [%]	12	16	5

*Table 3.1: State of the art CMOS 5G power amplifiers operating in the 28 GHz band.*

Therefore, in order to investigate its performances, and to achieve higher bandwidth of operation, the single-ended structure is chosen to be studied in this work for 5G power amplifier design on the 28 nm CMOS FD-SOI technology.

Consequently, in the next part of this chapter, we concentrate on studying and defining a single-ended PA architecture that allow us to achieve a highly efficient wideband PA while maintaining the linearity.



### 3. Review of Power Amplifier Architecture for 5G Applications

#### 3.1. Highly Efficient Modes of Operation

Classically, switching and harmonically tuned power amplifiers (classes E and F) are mostly used to achieve high efficiency amplification. As described in Chapter I, the overlapping of the output voltage and current of the transistor is reduced resulting in lower power consumption (Fig. 3.22). However, the performance of these classes relies on a very specific multi-harmonic impedance environment (resonators, frequency traps and terminations), narrowing their bandwidth [III.17]. Moreover, the switching mode of operation will reduce the linearity of the amplifier [III.18]. Thus, these classes present higher efficiency, but at the expense of the linearity and the bandwidth.

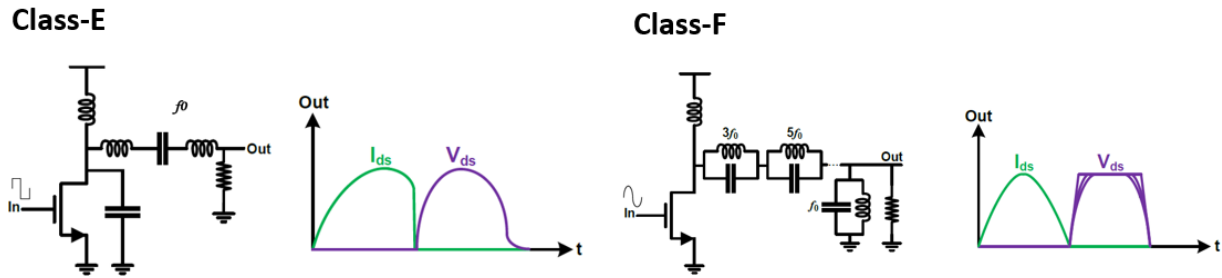


Fig. 3.22: Class E and F amplifiers schematics and output waveforms.

The Doherty technique is widely discussed recently for efficiency improvement at back-off operation. The technique was proposed by William H. Doherty in 1936 [III.19] and aims to keep the efficiency of the amplifier at a high value over a wide range of power. This structure is composed of a main amplifier and an auxiliary amplifier whose outputs are generally interconnected by quarter-wave line. The main amplifier is polarized in class A / AB and the auxiliary in class C. In order to recombine the signals in phase, another line (or coupler) is added before of the auxiliary amplifier (Fig. 3.23 (a)).

Under ideal conditions, it is possible to keep high efficiency over a power range of about 6 dB (Fig. 3.23 (b)). However, the back-off efficiency enhancement provided by the Doherty architecture remains much more modest at higher frequencies [III.20] (Fig. 3.23 (c)). In fact, the design of a low-loss matching circuit which provides high impedance when the auxiliary amplifier is turned off becomes much difficult at millimeter frequencies. Besides, the Doherty amplifier bandwidth is rather narrow because of the requirements of accurate phase matching between the two paths. Many works are underway for the improvement of this architecture [III.21] [III.22].

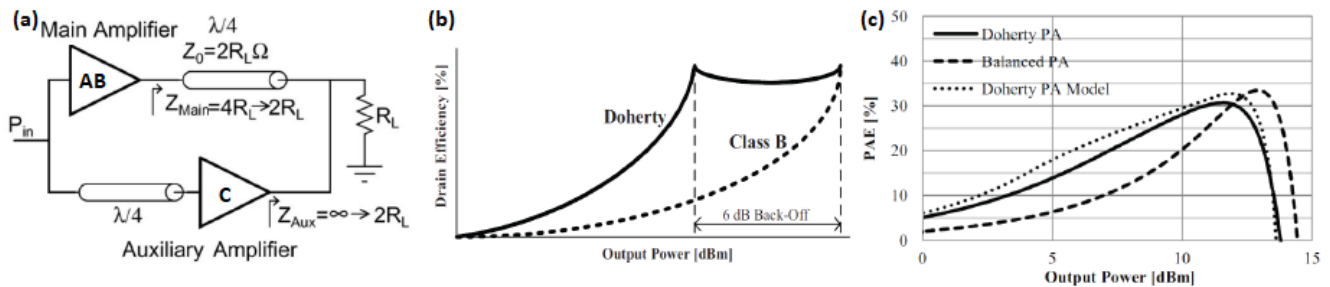


Fig. 3.23: Doherty PA [III.20] (a) Schematic (b) Efficiency versus output power in ideal conditions (c) Simulated efficiency versus output power at 60 GHz.

### 3.2. Sinusoidal Classes Optimization

Sinusoidal power amplifier classes, presented in Chapter I, are classified by their conduction angle. If the amplifier conducts all the time, the class of operation is the class A, and while decreasing the conduction angle the amplifier operates in classes AB, B and C. As shown in Fig. 3.24 the output power and efficiency of the PA behave oppositely with the conduction angle, and the classes that present the best tradeoff are the classes AB and B.

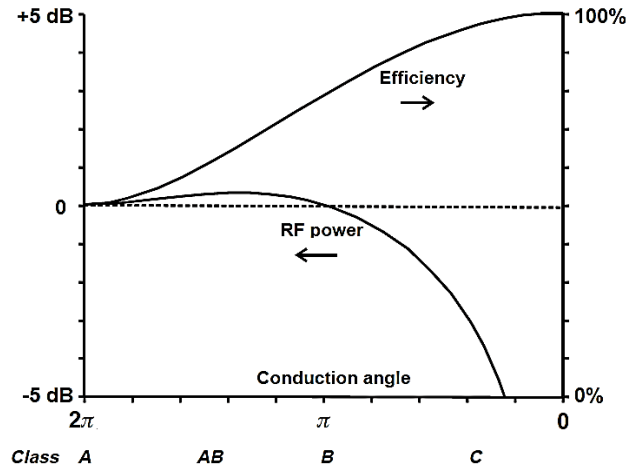


Fig. 3.24: PA output power and efficiency in function of the conduction angle [III.17].

Fig. 3.25 shows the harmonic composition of the output current  $I_{DS}$  in function of the conduction angle. In fact, as the conduction angle decreases, the  $I_{DS}$  sinusoid start to be rectified, and thus other harmonics are generated at the output of the transistor. For instance, in a class B the second harmonic presents one third of the current.

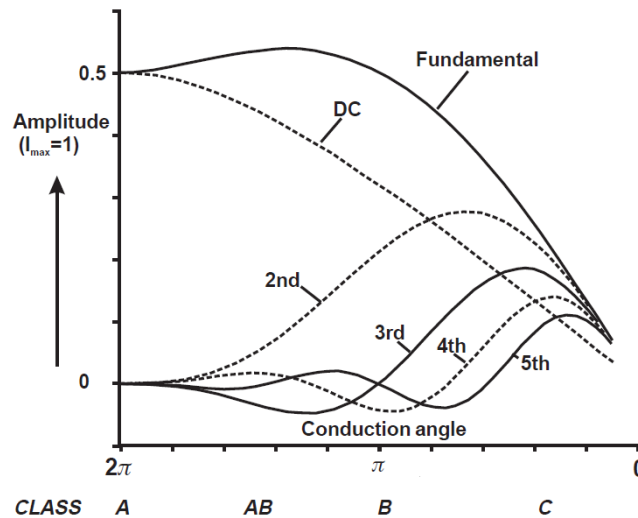


Fig. 3.25: Harmonic composition of the output current in function of the conduction angle [III.17].



## CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

And while designing a sinusoidal class of operation, only the fundamental frequency impedance is optimized without optimizing the other harmonic impedances. In fact, typically a load-pull simulation is done at the fundamental frequency and the optimum impedance at this frequency is presented at the output of the amplifier.

This means, that it is possible to obtain better performances with the sinusoidal classes while optimizing the fundamental frequency impedance and the other harmonic impedances.

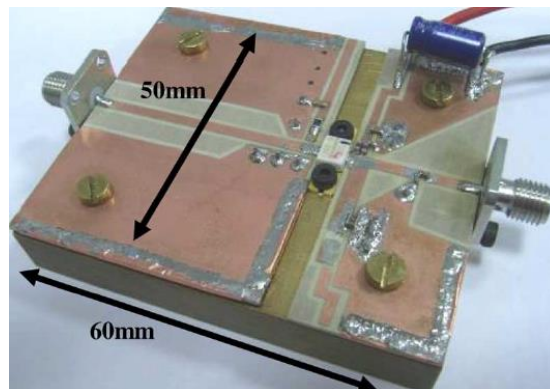
Consequently, we investigate one of the most promising improvements of the sinusoidal classes, the class J mode of operation.

### 3.3. State of the Art of Class J Amplifiers

Recently, a class J mode of operation has demonstrated its potential for high efficiency and wide bandwidth applications, while maintaining the linearity [III.17]. The class J amplifier is a derivative of class AB. Its theory involves engineering the output current and voltage waveforms of the amplifier using complex fundamental and second harmonic output impedances.

Before discussing the theory and design of the class J PA, we present the state of the art of the demonstrated class J amplifiers, to see if their performances are in accordance with the required specifications of our study.

This mode of operation was developed by S. C. Cripps [III.17] based on works of J. D. Rhodes [III.23] and F. H. Raab [III.24]. In the first published paper on this mode [III.25] a class J PA was demonstrated with a GaN transistor (Fig. 3.26) where it has been found to present better tradeoffs between power and efficiency over a substantial RF bandwidth. This amplifier presented a 3 dB bandwidth between 1.2 GHz and 2.5 GHz, an average drain efficiency of 60 % across the bandwidth with a saturated power of 40 dBm at 2 GHz.



*Fig. 3.26: The first demonstrated class J power amplifier [III.25].*

Fig. 3.27 recaps the state of the art of the fabricated class J amplifiers. As the histogram shows, most of the class J amplifiers are done with GaN and GaAs technologies. Only five integrated class J amplifiers were demonstrated and no class J PA is reported with a CMOS technology. Besides, most of these amplifiers operate at frequencies below 3 GHz.

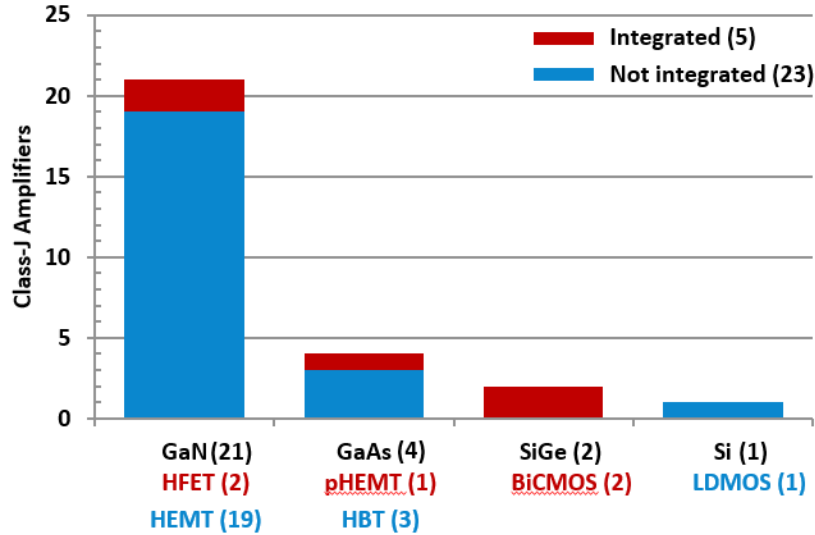


Fig. 3.27: Number of fabricated class J amplifiers per technology.

Fig. 3.28 shows the schematics and photographs of the state of art integrated class J amplifiers and Table 3.2 presents their performances.

This table demonstrate that all of these integrated amplifiers present high efficiency over a large bandwidth. In fact, for the first three columns in this table, the maximum PAE surpassed 50 % with the percentage bandwidth in the order of 30 %.

The 28 GHz 120 nm SiGe BiCMOS amplifier, represented in the last column of the table, achieves a power gain of 15.3 dB with an output power of 18.6 dBm and a 34 % of PAE. The bandwidth of this PA can't be concluded from the paper but the showed results indicate that the bandwidth is no less than 26 to 30 GHz.

Parameter	[III.26]	[III.27]	[III.28]	[III.29]
Topo. / Tech.	CS / GaN	CS / GaAs	CS / SiGe	Cascode / SiGe
Freq. [GHz]	2.8	9.5	0.7	28
BW [%]	32	35	29	-
Gain [dB]	8	5	12	15.3
P <sub>SAT</sub> [dBm]	24	28	31.5	18.6
PAE <sub>max</sub> [%]	51	60	60	34

Table 3.2: State of the art of the integrated class J amplifiers.

CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

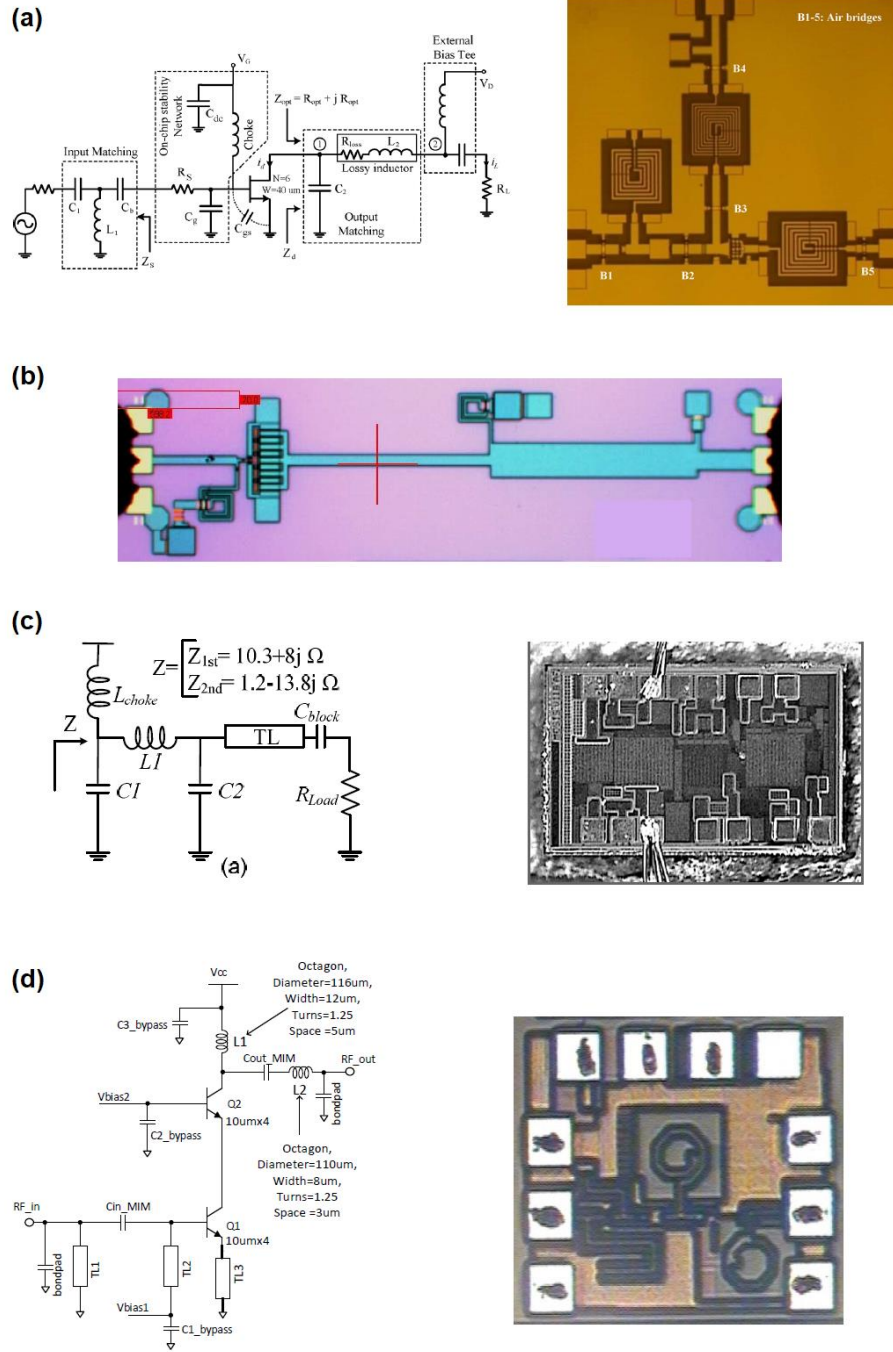


Fig. 3.28: Schematics and photograph of the demonstrated integrated class J amplifiers (a) [III.26] (b) [III.27] (c) [III.28] (d) [III.29].

## 4. Design and Analysis of Class J Power Amplifiers

After presenting the state of the art of the demonstrated class J PAs, and analyzing their highly efficient and broadband behavior, we present in this part of the chapter the methodology of designing a class J amplifier.

### 4.1. Class J Amplifier Theory

As described in the previous part of this chapter, sinusoidal classes of operation are usually optimized for the fundamental frequency of operation, without optimizing the harmonic impedances. In this section we present the theory of the continuous sinusoidal modes of operation or the class J theory [III.30].

The theory is originated from the conventional class B or ‘deep’ class AB, where the drain current is a half-wave rectified sinusoid. These classes present the best compromise in terms of output power and efficiency.

Considering the first two harmonics, the half wave rectified sinusoidal current is given by the equation:

$$I(\theta) = I_{max} \left( \frac{1}{\pi} + \frac{1}{2} \cos(\theta) + \frac{2}{3\pi} \cos(2\theta) \right) \quad (3.2)$$

Where  $\theta$  is the angular phase, and  $I_{max}$  is the transistor maximum drain current.

Concerning the drain voltage waveforms  $V(\theta)$ , two criteria should must be verified in order to maintain a linear behavior:  $V(\theta)$  should be always higher than the knee voltage  $V_k$  and no RF power should be delivered to the load harmonic frequencies. A set of voltages can meet the criteria above representing a family of continuous waves expressed by:

$$V(\theta) = V_k + (V_{DC} - V_k) (1 - \cos(\theta) - \alpha \sin(\theta) + \frac{\alpha}{2} \sin(2\theta)) \quad (3.3)$$

Factorizing this equation give:

$$V(\theta) = V_k + (V_{DC} - V_k) (1 - \cos(\theta))(1 - \alpha \sin(\theta)) \quad (3.4)$$

Where  $V_{DC}$  is the supply voltage and  $\alpha$  is a unitless parameter with  $-1 \leq \alpha \leq 1$ .

The normalized continuous drain voltages are shown in Fig. 3.29 (a). For  $\alpha = 0$  the class B is obtained, for  $\alpha = 1$  the class J and for  $\alpha = -1$  the class J\*.

For  $\alpha = 0$  the maximum voltage is  $V_{DC}$ , for  $\alpha = 1$  or  $-1$  the maximum voltage is  $3 V_{DC} - 2 V_k$ . For technologies with high breakdown voltage like GaN and GaAs, this will not cause a constraint. But with CMOS transistors,  $\alpha$  must be chosen with specific attention not to surpass the breakdown voltage of the transistor.

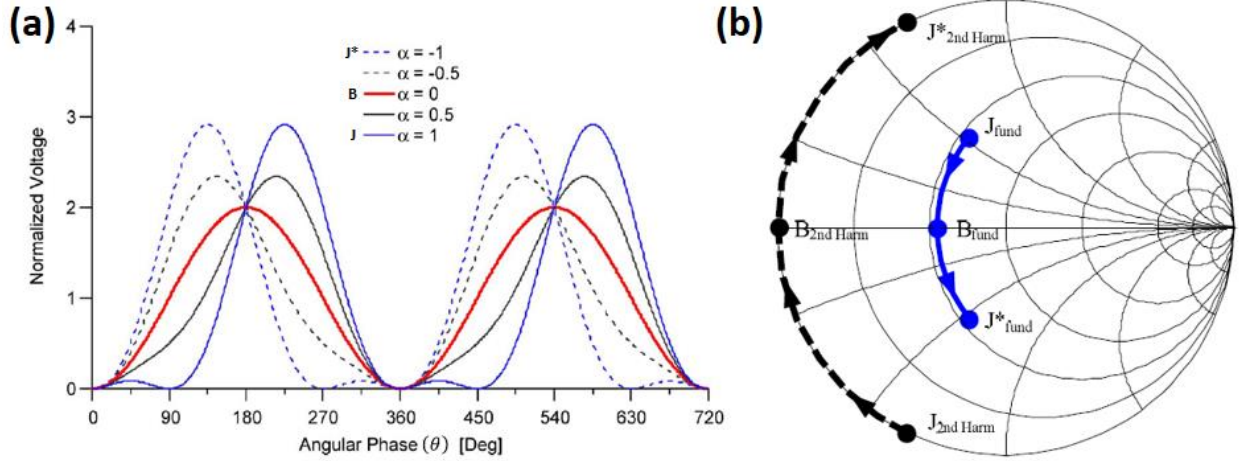


Fig. 3.29: (a) Continuous drain voltage waves in function of  $\alpha$  (b) Smith chart of the fundamental and second harmonic impedances of the continuous waves modes.

Subsequently, the harmonic impedances ( $Z_n$ ) could be calculated by the formula:

$$Z_n = \frac{V_n}{-I_n} \quad (3.5)$$

Where  $n$  is the harmonic number.

Using equations (3.2), (3.3) and (3.5) the harmonic impedances could be expressed as follows:

$$Z_1 = \frac{(V_{DC} - V_k)(1 + j\alpha)}{I_{max}/2} = (1 + j\alpha)R_{opt} \quad (3.6)$$

$$Z_2 = -j \frac{(V_{DC} - V_k)\alpha}{2(I_{max}/3\pi)} = -j \frac{3}{8\pi} \alpha R_{opt} \quad (3.7)$$

With  $R_{opt}$  is the loadline impedance of the transistor defined by:

$$R_{opt} = \frac{2(V_{DC} - V_k)}{I_{max}} \quad (3.8)$$

Finally, since the harmonics of order 3 and above were eliminated from the beginning of the study, their impedances are theoretically shorted:

$$Z_{>2} = 0 \quad (3.9)$$

Fig. 3.29 (b) shows a Smith chart representation of the fundamental and second harmonic impedances of the continuous waves modes. Of course, the values of the impedances depend on  $R_{opt}$  and thus the DC characteristics of the transistor. As shown in this figure, the class J mode is obtained for a complex inductive load at the fundamental, and a purely capacitive load at the second harmonic.

### 4.2. Class J Amplifier Design

The starting point in designing a class J PA is the class AB / B bias point. This will result in a rectified sinusoidal  $I_{DS}$ .

Then, presenting a complex inductive load at the fundamental and a pure capacitive load at the second harmonic will shift and boost the  $V_{DS}$  of the class AB, in order to obtain a rectified  $V_{DS}$  (Fig. 3.30 (a)).

As a result, the slight overlapping between the  $V_J$  and  $I_J$  will make this mode highly efficient. And the non-switch mode of operation allows this class to maintain the linearity of a class AB [III.17].

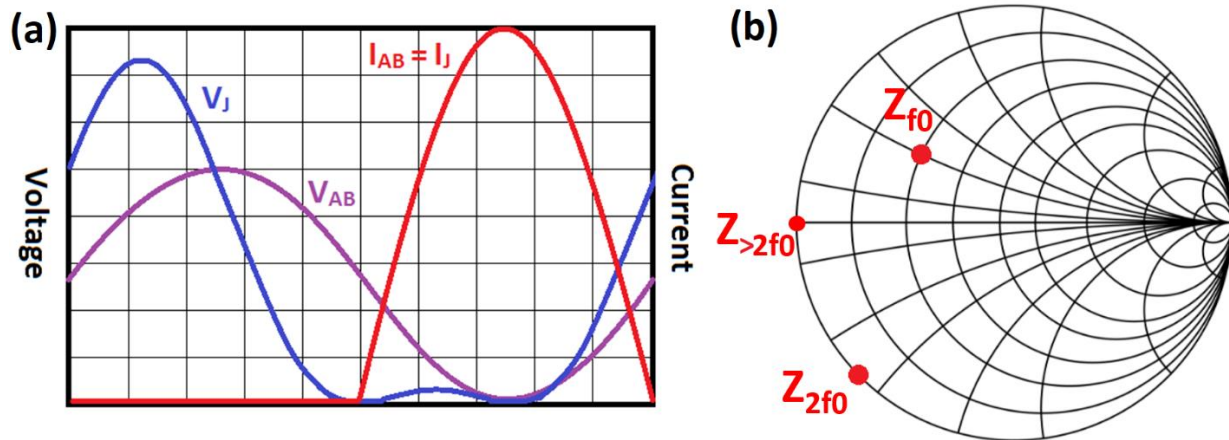


Fig. 3.30: (a) Class AB and J output waveforms (b) Smith chart of a class J amplifier harmonic impedances with  $R_{opt} = 10 \Omega$ .

Fig. 3.30 (b) shows an example ( $R_{opt} = 10 \Omega$ ) of the required harmonic impedances to obtain the half-wave rectified sinusoid  $V_J$ . Basically, two methods are used to achieve these impedances. The first is the transmission line networks, the second is the use of a  $\pi$  network. Since most of the demonstrated class J amplifiers are not integrated, the transmission lines are mostly used. However, regardless of their ease of design and layout, the transmission lines occupy large area of the integrated circuit, resulting in a direct consequence on the size and cost of the circuit. Thus, the  $\pi$  network method is used in this work.

The  $\pi$  network is constituted of two parallel capacitances and a series inductance. As Fig. 3.31 shows, the resulting fundamental impedance is complex inductive, and the second harmonic impedance is purely capacitive. In addition, the harmonic impedances of order above two will approach the short circuit. Thus, a class J PA could be designed using this network.

Moreover, the large bandwidth of this network and the absence of harmonic impedance traps and terminations will result in a broadband behavior of the amplifier.

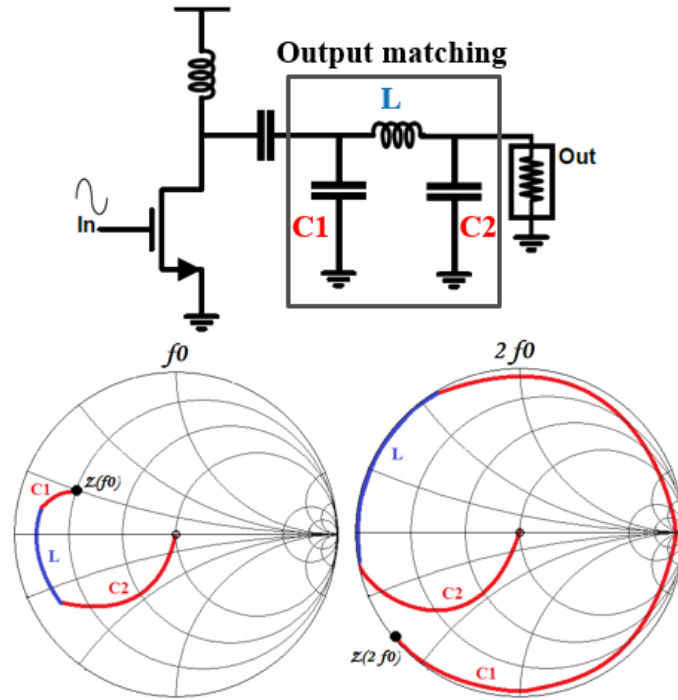


Fig. 3.31: The fundamental and second harmonic output impedances of the  $\pi$  matching network.

### 4.3. Class J Amplifier Versus the Frequency

Before starting the design of the class J amplifier at 28 GHz, it is important to check if this PA mode is suitable for high frequency applications. Therefore, a study was conducted on the class J mode of operation versus the frequency. The study was focused on the  $\pi$  network as it is the main distinction of a class J PA.

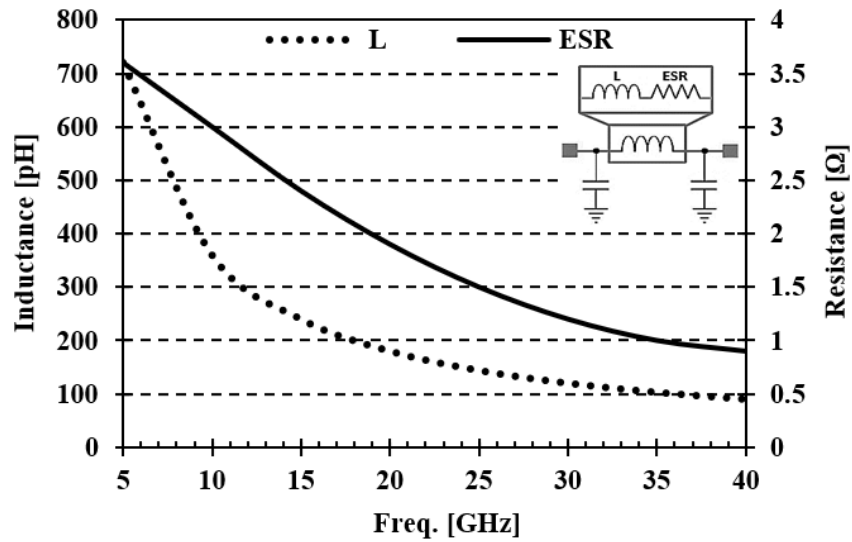


Fig. 3.32: Values of the inductance and its equivalent series resistance of a class J  $\pi$  network versus the frequency (transistor width = 200  $\mu\text{m}$ ).

### CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

The inductance is the most critical element in the  $\pi$  network as it is in the main path of the RF output wave which carries the largest current in the circuit. Thus, minimizing its Equivalent Series Resistance (ESR) will result in a direct increase of the output power and the PAE of the amplifier.

Fig. 3.32 shows the values of the inductance of the  $\pi$  network allowing to obtain a class J behavior for frequencies between 5 GHz and 40 GHz. In the same graph is represented the values of its ESR obtained by the electromagnetic simulations of the inductances. Since the product of L and the frequency is almost constant, as the frequency increases, the value of the inductance of this network will decrease. Most importantly, the value of its series resistance will also decrease allowing lower power consumption and higher output power and efficiency.

Concerning the capacitances of the  $\pi$  network, they don't pose any problem at higher frequencies since they are grounded and not in the main path of the output wave. In addition, their values and sizes are reduced at higher frequencies.

These observations can lead to the conclusion that the class J and the  $\pi$  network are more suitable for higher frequency power amplification.



### 5. Power Amplifier Design Methodology

In this part we present the design of a highly efficient, wideband power amplifier for 5G applications.

All the simulations presented are carried out with the CAD (Computer Aided Design) tool Cadence Virtuoso version IC 6.1.5. The design kit used is PDK\_STM\_CMOS28FDSOI\_AMS\_6U1x\_2U2x\_LB version 2.9 provided by the multi project wafer provider 'Circuit Multi-Projets' (CMP).

To recapitulate, the PA scope statement:

- The technology used is the 28 nm CMOS FD-SOI of STMicroelectronics.
- The center frequency of the PA is 28 GHz.
- The targeted bandwidth is above 10 GHz.
- Highly efficient behavior is needed at saturation and back-off operation.
- Reconfigurability of the linearity with the back-gate bias is needed to meet the linearity requirement at a specific time.
- A saturated power of 15 dBm and a power gain of 15 dB.

As analyzed in the previous part, the class J is a very suitable mode of operation for these PA requirements.

Fig. 3.33 shows a simplified flowchart of designing the power amplifier described in this chapter. There are no reliable analytic equations for designing integrated power amplifiers for particular specifications, which imposes the use of an iterative method [III.31]. One of the main reasons is the large number of parameters to be taken into consideration while designing the PA (topology, transistor sizing, biasing, input power, etc.). What makes the task much harder is the variation of the optimum impedances of this non-linear system with large signals.

The design begins with the determination of the desired specifications, performances and characteristics of the power amplifier.

After defining the desired performances, comes the most critical part of the design: the electrical schematic simulation. In this part the topology of the circuit is defined in accordance with the desired performances. Then, the transistors sizing, biasing, input power and matching networks are designed in the schematic. Usually, ideal components are used at first, then they are replaced by the real component of the Process Design Kit (PDK).

If the desired performances are achieved while respecting the voltage restrictions in the Safe Operating Area (SOA) of the transistors, the layout part of the design begins. During the layout design, the positioning of each polygon must follow strict rules that are checked by the DRC (Design Rules Check). In addition, the connections made between the components must be identical to the schematic, which are checked by the LVS (Layout Versus Schematic) process.

After concluding the layout with success (correct DRC and LVS) and respecting the chip area defined by the budget, the parasitic extraction must be done and then a Post-Layout Simulation (PLS) is performed. This simulation shows the impact of the parasitics on the circuit performance. After the PLS, it is typical make changes in the layout or even in the schematic to achieve better performances.

The design cycle continues with the electromigration calculations of the metals and vias in the circuits. The electromigration rules are defined in the Design Rule Manual (DRM) of the technology in order to ensure circuit operation for a minimum of 10 years at different temperatures (up to a maximum junction temperature of 150 °C). In fact, the phenomenon of electromigration corresponds

### CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

to the displacement of atoms in a conducting track caused by the flow of electrons [III.32]. Material displacement may, in the long run, lead to breakage of the track, but also breakage of the passivation layer, leaving the field free to corrosion.

After validating the circuit reliability, final corrections are normally done on the layout to respect final metal density rules. In fact, to fabricate the chip there are many density rules that must be respected with the risk of the chip being damaged during the fabrication process or even to damage other chips from other designers that are positioned on the same wafer. For respecting the density rules, many blocks of metals (dummies) are spread on the layout without being connected to anything.

Finally, the layout of the circuit is exported and sent to the foundry for fabrication.

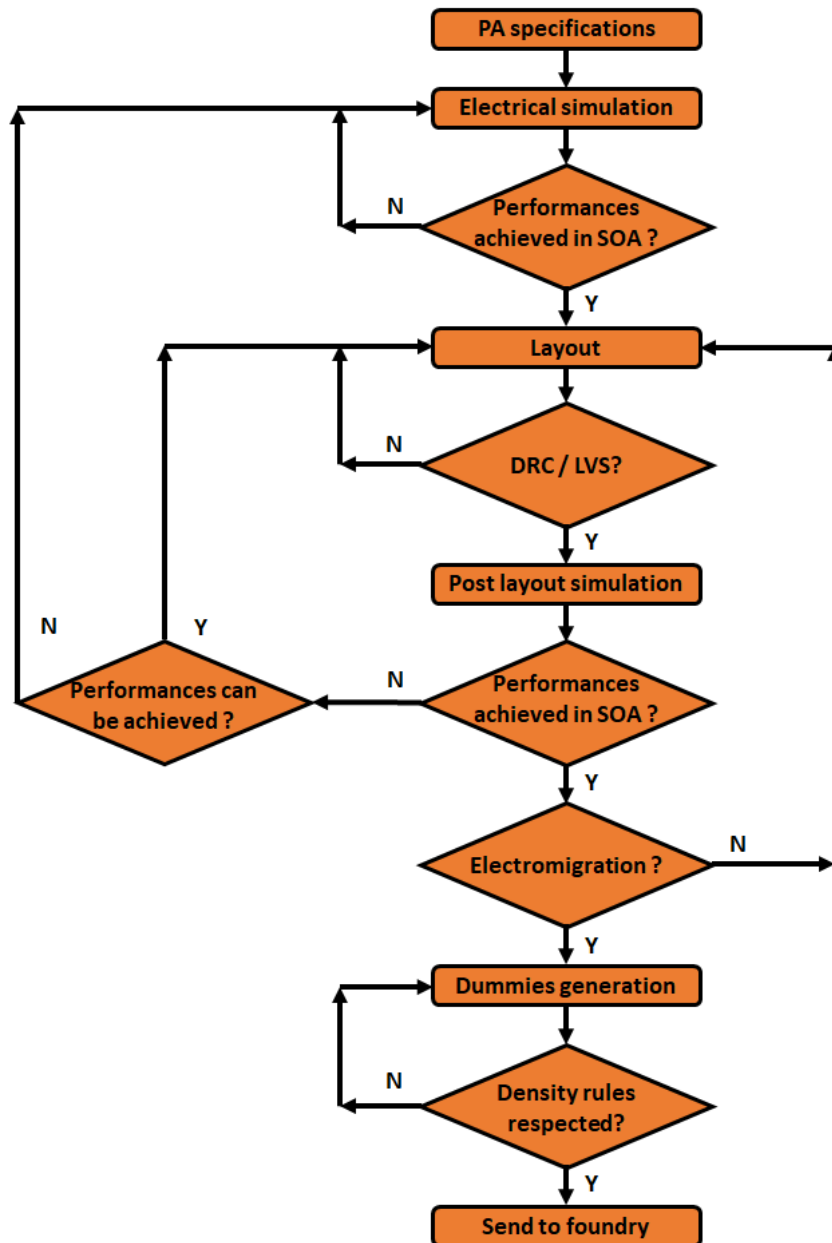


Fig. 3.33: Design flowchart of the power amplifier on 28 nm FD-SOI technology.

## 6. Power Amplifier Design

### 6.1. Transistor Sizing and Layout

The first element to be designed and sized in an amplifier is the transistor.

A transistor of width  $W$  is composed of a number  $N_f$  of elementary transistors (fingers) with each a width of  $W_f$  with  $W = N_f \times W_f$  (Fig. 3.34).

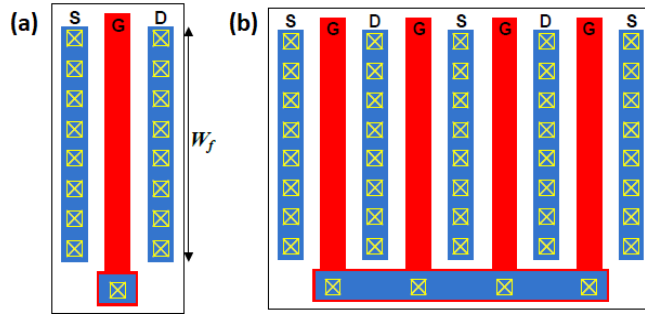


Fig. 3.34: (a) Elementary transistor layout view (b) 4 fingers transistor layout view.

The finger width  $W_f$  is critical for RF applications. In fact, it has a direct effect on the gate resistance responsible for the degradation of the figure of merit  $f_{max}$ . Charts have been published in [III.33] to select the appropriate gate width  $W_f$  in function of the technological node (Fig. 3.35). Therefore, finger widths in the order of  $1 \mu m$  were used in this work.

The parasitic capacitances and the complexity of the modeling increase when the number of fingers  $N_f$  of the transistor increases. On the other hand, a higher number of fingers makes it possible to minimize the gate resistance. The impact of parasitic capacitances, and in particular the drain-source capacitance  $C_{DS}$ , leads to a size limit of  $W$  of approximately  $350 \mu m$  at 28 GHz, in order to avoid reducing the output impedance too much. In general, the empirical formula is [III.2]:

$$W_{max} [\mu m] = \frac{10^4}{freq. [GHz]} \quad (3.10)$$

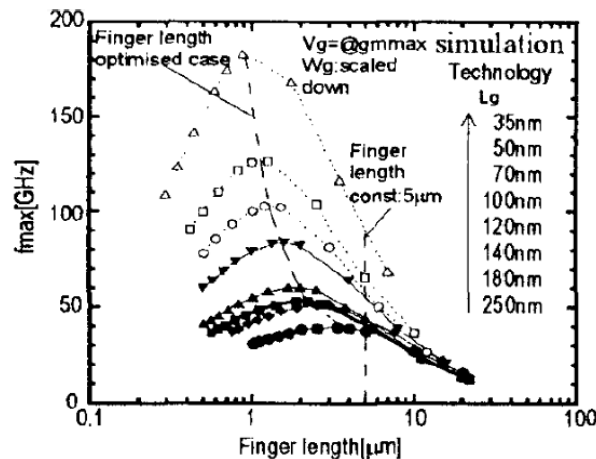


Fig. 3.35:  $f_{max}$  in function of the finger width and channel length.

### CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

As shown in Fig. 3.36, with larger transistors, higher output current can be achieved. For the bias conditions presented in this figure with a supply voltage  $V_{DS} = 1$  V, the  $I_{DS}$  current passed from 40 mA to 100 mA and 145 mA for  $W = 100$ , 200 and 300  $\mu\text{m}$  respectively.

This demonstrates that the main criteria in choosing the width of the transistor is the output current and power needed.

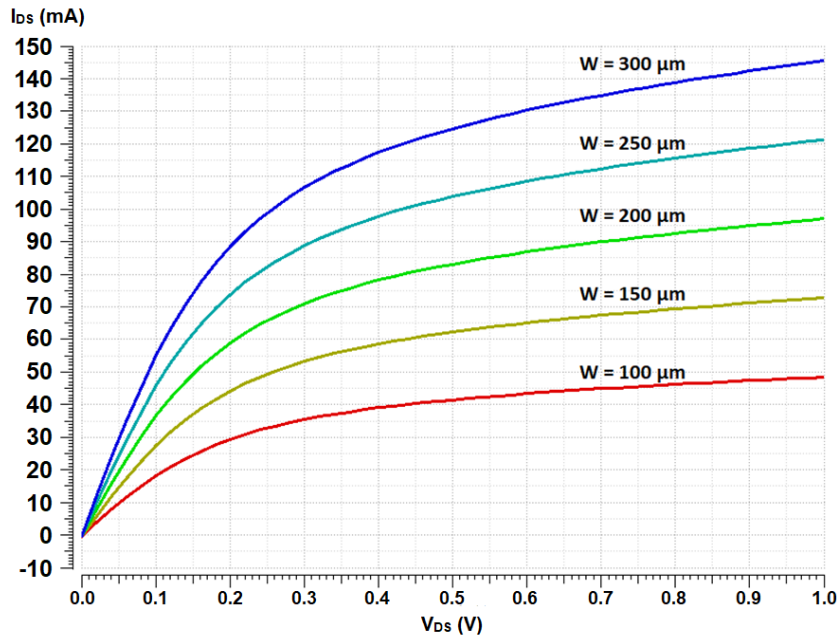


Fig. 3.36:  $I_{DS}$  vs.  $V_{DS}$  of an LVT nFET in function of  $W$  for  $V_{GS} = 0.3$  V and  $V_{BB} = 0$  V.

Currently, the FD-SOI design kit does not provide the interconnects of the transistors, so this task must be done manually by the designer. Simulating the provided transistor model without the interconnects will lead to ignoring their parasitic effects. These effects are very important to take into consideration especially with higher frequencies and when the used transistor gets larger in order to provide higher power. Therefore, in order to obtain accurate results, the transistor and its interconnects must be layouted, and the parasitic effects must be extracted and added to the transistor model.

While layouting transistors a special care must be taken in order to decrease the parasitic effects as possible. The general rules are to use larger metals more vias between the metals in order to decrease the resistances.

Fig. 3.37 (a) shows the layout of a 50  $\mu\text{m}$  transistor with 52 fingers of  $W_f = 0.962 \mu\text{m}$ . When the number of fingers gets high, the transistor gets wider resulting in larger source and drain inductances. Thus, for designing larger transistors, elementary transistor blocs are connected in parallel. For example, to design a 200  $\mu\text{m}$  transistor, 4 blocks of the 50  $\mu\text{m}$  transistor shown in Fig. 3.37 (a) are connected in parallel (Fig. 3.37 (b)).

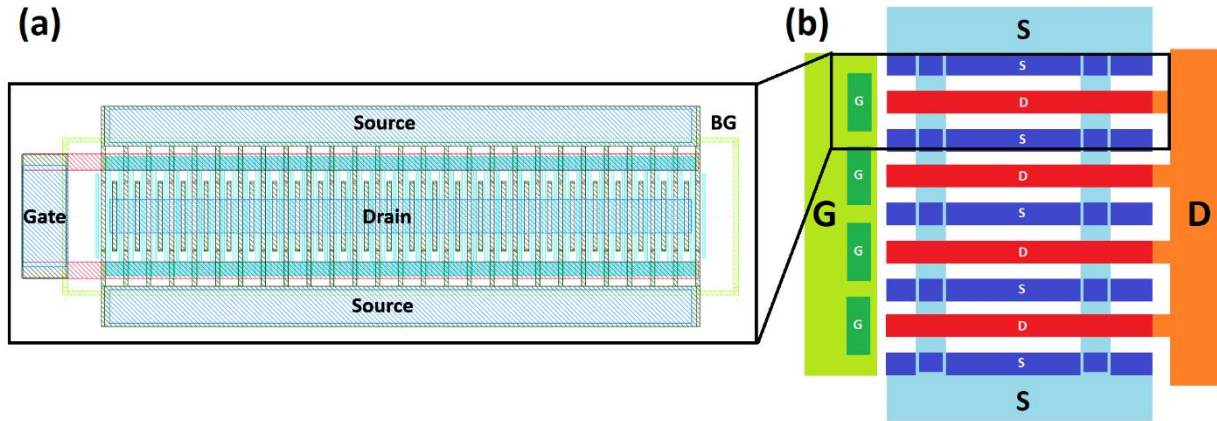


Fig. 3.37: (a) Layout of a 52 fingers transistor and its interconnections (b) Four parallel 52 fingers transistor blocks connected.

## 6.2. Power Amplifier Topology

The two main topologies of a single-ended amplifier are the common source and the cascode.

Comparing these two topologies is not an easy task since the comparison must be fair and take into consideration all the parameters. Nevertheless, single stage PAs of these two topologies were designed and compared at 28 GHz with the 28 nm FD-SOI. The comparison was made in the schematic (Fig. 3.38) using passives of the FD-SOI design kit. The two amplifiers were biased for the same conduction angle, and with the transistors having the same widths. The results of the comparison are summarized in Table 3.3 where it is shown that tradeoffs have to be made to choose between these two topologies.

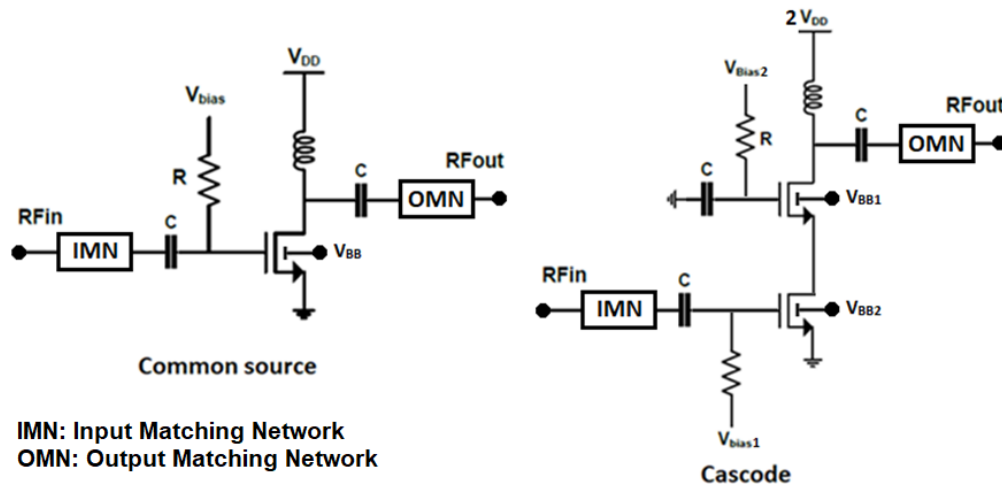


Fig. 3.38: Common source and cascode schematics.

The cascode topology showed higher gain and output power, since stacking transistors allow the use of higher supply voltages. Also, this topology presented better stability yet both amplifiers are unconditionally stable with the use of passives.

## CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

The bandwidth of these topologies is dependent on the matching networks, but generally both of the topologies present substantial bandwidth.

The common source topology is easier to design since the number of elements and parameters is reduced. Besides, the common source circuit is smaller resulting a direct effect on the cost which is an important constraint especially for the used technology. In addition, this topology presented better efficiency, mostly because the number of transistors and elements is reduced. Finally, the common source PA was found to be more linear than the cascode counterpart.

Topology	Efficiency	Bandwidth	Gain	Linearity	Output power	Stability	Size
Common source	☺	☺	☹	☺	☹	☹	☺
Cascode	☹	☺ <sup>+</sup>	☺	☹	☺	☺	☹

Table 3.3: Common source and cascode topologies comparison.

Consequently, in accordance with the desired specifications, the common source topology was chosen.

Fig. 3.39 shows the chosen schematic of the PA, it is composed of two common source stages. The power stage is a class J with a  $\pi$  output matching network. A driver stage is used in this design in order to improve the overall power gain of the amplifier.

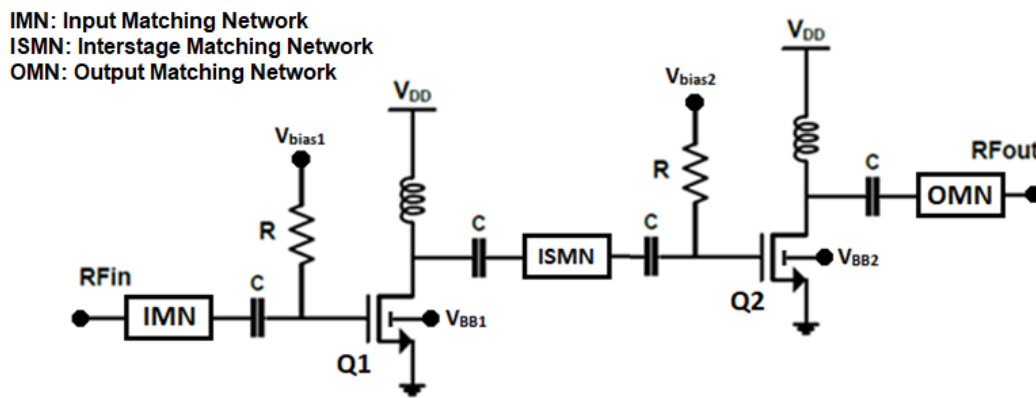


Fig. 3.39: Chosen schematic of the power amplifier.

### 6.3. Class J Power Stage Design

Fig. 3.40 shows the schematic of the class J power stage.

The supply voltage  $V_{DD}$  is 1 V and the gate is biased with  $V_{bias} = 0.2$  V in order to obtain a deep class AB behavior.

After fixing the bias voltages, the conjugate input impedance of the transistor is put into the input port.

The  $C_{in}$  and  $C_{out}$  are the input and output DC block capacitances of 1.4 pF, their impedances at 28 GHz is very low. These capacitances are of type MOM (metal oxide metal) chosen from the process design kit (Fig. 3.44 (a)).

The RF Choke is also taken from the design kit, its selected value is 1.5 nH. This value was optimized in regard of the size and performances.

### CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

In the single-ended structure, the source-ground path must be accurately modeled in order to obtain precise simulation results. Thus, the source of the transistor is directly connected to a ground pad. This source-pad path must be as conductive as possible using many metal layers. Additionally, to decrease the inductance of this path, the transistor must be as close as possible to the ground pad. The inductance of this path is a very limiting factor especially at higher frequencies since its equivalent impedance increases. In the layout, the inductance of this path is 50 pH, obtained from simulating the multi-metal path with Momentum. This path will decrease the gain of the amplifier but reinforce its stability.

In order to achieve an output power level above 15 dBm, taking into account the losses, the transistor size of the power stage was chosen to be 250  $\mu\text{m}$ . It is constituted of 5 parallel 50  $\mu\text{m}$  transistors (Fig. 3.37 (a)). After the 250  $\mu\text{m}$  transistor is layouted with the interconnections, the parasitic extraction is carried out. A DC simulation is then done to obtain the  $R_{opt}$  of the device, the resulting value is  $R_{opt} = 0.2 \times 50 = 10 \Omega$ .

The layout of the power transistor will result in a high  $C_{DS}$  capacitance of 350 fF. This capacitance is integrated into the  $\pi$  network in order to obtain a class J behavior. This highlights another advantage of the class J mode at higher frequencies as it absorbs the parasitic capacitances of the transistor.

Finally, the RF pad (Fig. 3.44 (b)) will create a ground capacitance of 32 fF, this value must be taken into consideration in the output network.

To obtain the class J behavior  $L_0$  and  $C_0$  must be calculated, this is done by finding the expression of the  $Z_d$  impedance showed in Fig. 3.40:

$$Z_d = \left( \left( \left( R_{port} \parallel Z_{cpad} \right) + Z_{cout} \right) \parallel Z_{C_0} \right) + Z_{L_0} \parallel Z_{C_{ds}} \quad (3.11)$$

Developing this equation in function of the angular frequency gives:

$$Z_d(\omega) = \left( \left( \left( R_{port} \parallel (1/j \omega C_{pad}) \right) + (1/j \omega C_{out}) \right) \parallel (1/j \omega C_0) \right) + (j \omega L_0) \parallel (1/j \omega C_{ds}) \quad (3.12)$$

With the port resistance  $R_{port} = 50 \Omega$ , the only two unknowns in this equation are the values of  $L_0$  and  $C_0$ . Their values are calculated by solving for  $\omega_1 = 2 \pi f_0$  and  $\omega_2 = 4 \pi f_0$  with  $Z_d(\omega_1)$  and  $Z_d(\omega_2)$  obtained from equations (3.6) and (3.7) respectively. Taking into consideration the impedances of the interconnections in the layout will result in  $L_0 = 120 \text{ pH}$  and  $C_0 = 160 \text{ fF}$ .

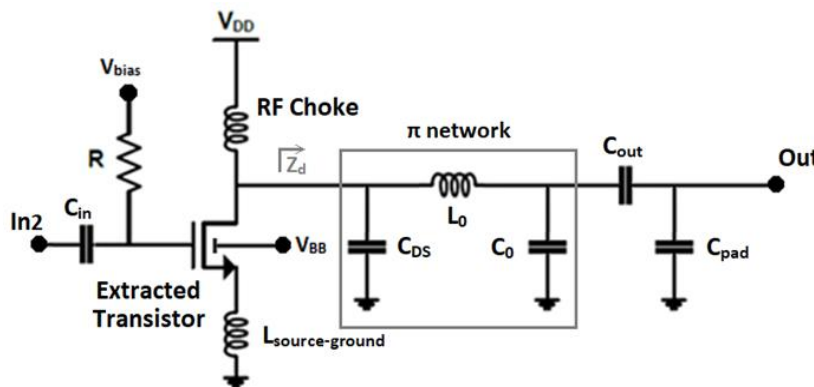


Fig. 3.40: Power stage class J schematic.

### 6.4. Driver Stage and Matching Networks Design

Fig. 3.41 shows the schematic of the driver stage.

The supply voltage  $V_{DD}$  is 1 V, the gate bias is selected as  $V_{bias} = 0.3$  V (conduction angle of  $220^\circ$ ). This bias point is chosen because it offers good tradeoffs between gain, linearity and efficiency.

The  $C_{in}$ ,  $C_{out}$  and RF choke are the same as their counterparts in the power stage presented above. In addition, the source ground inductance has the same value of 50 pH since the layout of the amplifier is chosen to be symmetrical. In addition, the input RF pad of the amplifier creates a 32 fF capacitance with the ground.

The transistor size is chosen to be  $120 \mu\text{m}$  in order to achieve the input power required for the power stage, taken into consideration the losses.

After fixing the parameters, and conjugately matching the input port, a load-pull simulation is done in order to present the output impedance that allows the highest gain and efficiency with respect to the desired output power.

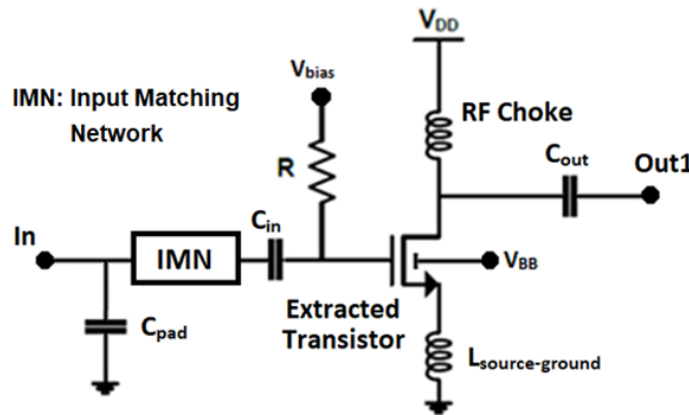


Fig. 3.41: Driver stage schematic.

The next part of the PA design is the input and inter-stage matching networks (Fig. 3.42).

Concerning the input matching, only one series inductor of 120 pH is used to match the input of the PA ( $50 \times (0.41 + j 0.13) \Omega$ ) to the input pad. This value does not perfectly match the input at 28 GHz, in fact it is chosen as a compromise between the gain at 28 GHz and the bandwidth of the amplifier.

The same compromise between the gain at 28 GHz and the bandwidth is done for the inter-stage matching network. In fact, in order to match the conjugate input impedance of the second stage ( $50 \times (0.42 - j 0.1) \Omega$ ), to the optimal impedance of the second stage ( $50 \times (0.44 + j 0.14) \Omega$ ), only an 80 pH inductor is used.

It is worth to be noted that after adding any component or interconnection a fine tuning is done in order to obtain the best results possible.



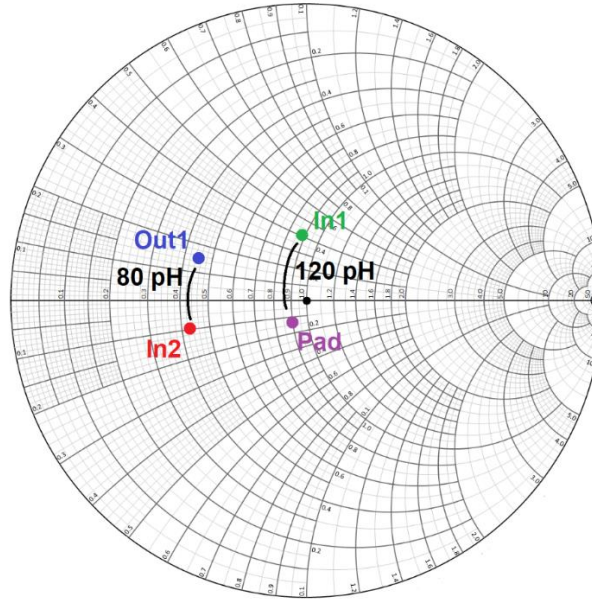


Fig. 3.42: Smith chart of the input and inter-stage matching networks at 28 GHz.

### 6.5. Layout of the Amplifier

The layout of the PA is presented in Fig. 3.43. The circuit size with pads is  $1050 \times 740 \mu\text{m}^2$ .

Four DC pads are placed in the upper side of the circuit, and six DC pads are placed in the lower side. In the right and the left sides of the circuit there's the RF pads constituted of the RF signal pad surrounded by two RF ground pads.

An important constraint in the circuit design is the distance between the pads. In fact, the distance between the centers of the DC pads must be no less than  $150 \mu\text{m}$ . Moreover, the distance between the center of the RF ground pads and the DC pads must be higher than  $300 \mu\text{m}$ .

Concerning the upper pads, a pair of two DC pads (ground/signal) is used to supply each stage of the amplifier. These pads are decoupled by  $3 \text{ pF}$  bypass capacitances. The sources of the transistors are approached as possible to the ground pads in order to reduce the source-ground inductance.

The lower pads are connected to the gate and the back-gate biases of each stage. In addition, two sense pads are used to measure the supply current of each stage.

A ground plane, that connects all the ground pads of the circuit, is designed manually by stacking all the 8 metal layers of the BEOL in order to homogenize the grounds of the circuit and to minimize inductances and resistances of the plane. This plane covers all the lower-side and some of the upper-side of the circuit and is constituted of connected elementary cells (Fig. 3.44 (c)).

Finally, the thick top-level metals of the technology and the Alucap are used for designing the low loss interconnects and inductors.

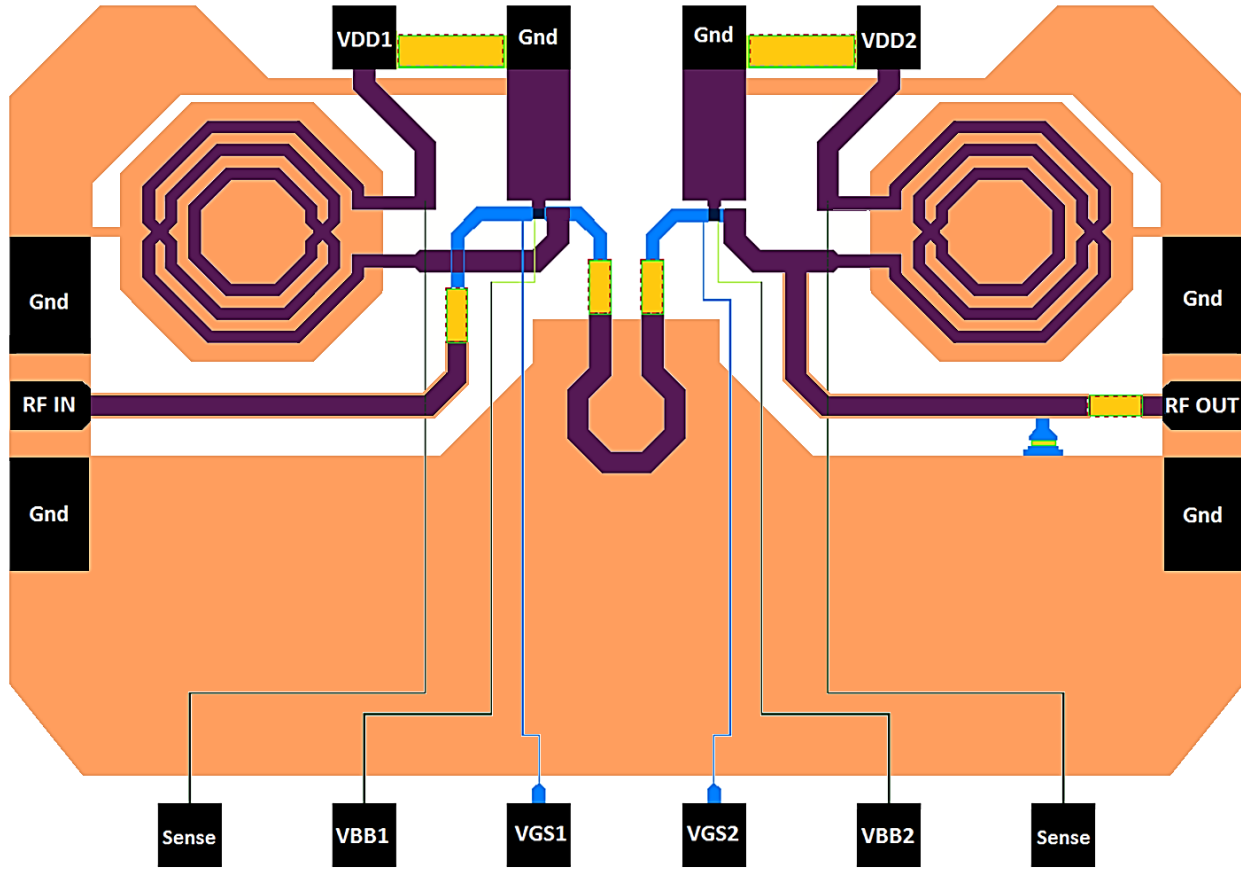


Fig. 3.43: Layout of the power amplifier ( $1050 \times 740 \mu\text{m}^2$ ).

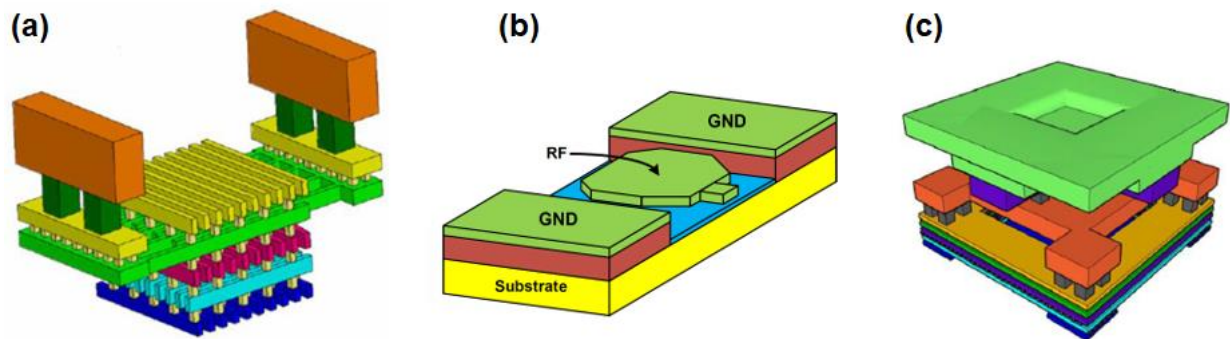


Fig. 3.44: 3D view of (a) MOM capacitance (b) RF pads (c) Ground plane elementary cell.

## 7. Post-layout Simulation Results

Fig. 3.45 presents the S-parameters results of the power amplifier. A power gain  $S_{21}$  of 15 dB is achieved. The 3 dB bandwidth is from 22 GHz to 34 GHz covering the two 5G frequency bands candidates. The  $S_{11}$  and  $S_{22}$  parameters are below -10 dB across all the bandwidth of the PA. In addition, the PA is unconditionally stable in this frequency range for the different biasing conditions.

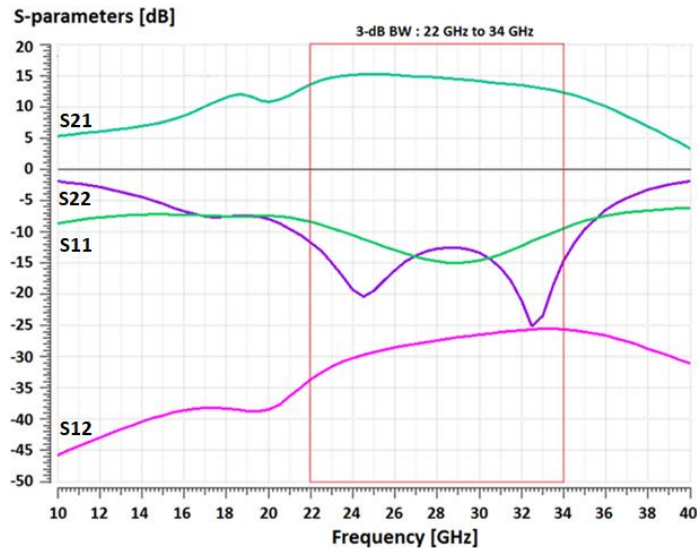


Fig. 3.45: Post-layout results of the S-parameters of the amplifier.

Fig. 3.46 (a) shows the large signal performance of the power amplifier at 28 GHz. The PA presents a saturated output power of 16.2 dBm and an output 1 dB compression point of 13.2 dBm. Furthermore, the amplifier achieves a maximum PAE of 38 %, and the DC power consumption of the PA is 54 mW.

The saturated output power is plotted versus the frequency in Fig. 3.46 (b). The 3 dB bandwidth of  $P_{SAT}$  covers the frequency range from 22 to 32 GHz.

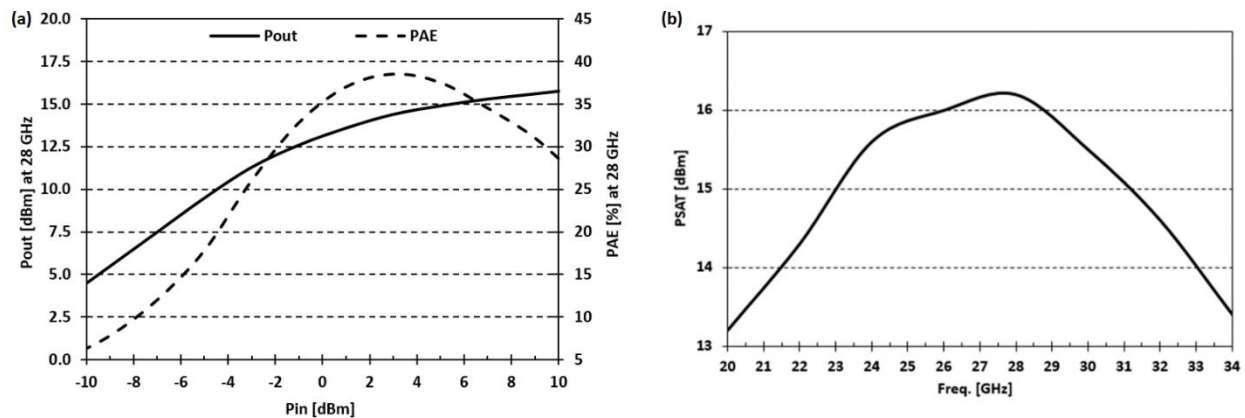


Fig. 3.46: Large signal post-layout simulation results (a) The output power and PAE at 28 GHz (b) The saturated power versus the frequency.

### CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

As mentioned earlier, one of the key advantages of the 28 nm CMOS FD-SOI technology is the back-gate bias.

Fig. 3.47 (a) shows the variation of the PAE of the amplifier with the back-gate bias of the second stage ( $V_{BB2}$ ). Decreasing  $V_{BB2}$  will decrease the maximum PAE, but increase the PAE at back-off operation. In fact, the 8 dB BO PAE is increased from 15 % to 21 % for  $V_{BB2} = 2$  and 0 V respectively. Therefore, the efficiency of the PA is reconfigurable with the back-gate bias of the second stage.

Fig. 3.47 (b) shows the variation of the output power of the amplifier with the back-gate bias of the first stage ( $V_{BB1}$ ). As the  $V_{BB1}$  decreases, the gain of the PA decreases while the input compression point increases indicating higher linearity. In fact, decreasing the  $V_{BB1}$  from 2 to 0 V will increase the input CP1 of 5 dB while maintaining the  $P_{SAT}$ . Consequently, the linearity of the PA is reconfigurable with the back-gate bias of the first stage, and the amplifier can adapt its behavior for the linearity requirements at a specific time.

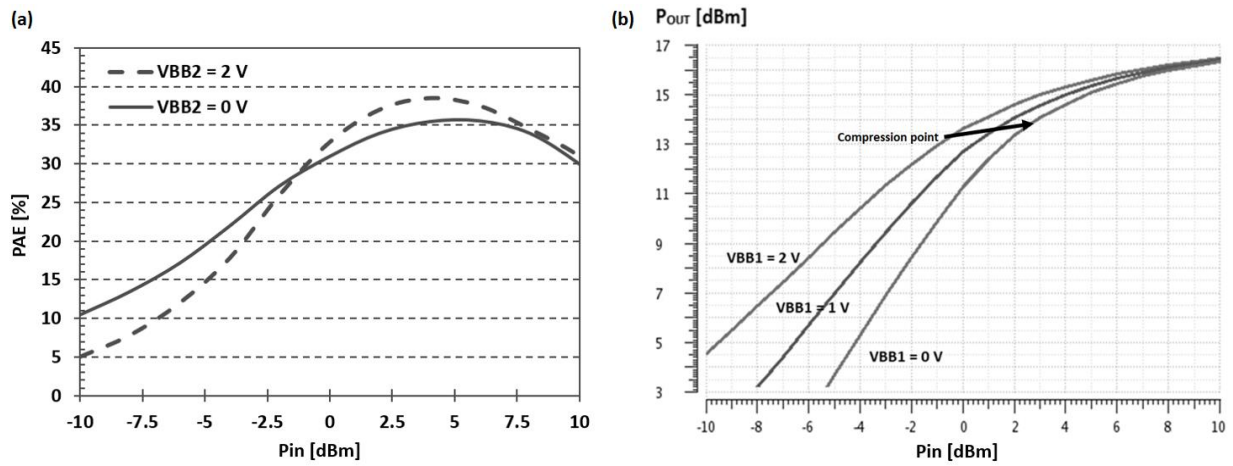


Fig. 3.47: Large signal post-layout simulation results at 28 GHz (a) PAE for different  $V_{BB1}$  (b) Output power for different  $V_{BB2}$ .

Table 3.4 shows a performance comparison of the post-layout simulation results of this work with state of the art 28 GHz power amplifiers. Post-layout simulation results show that the single-ended structure and the class J mode of operation allows us to obtain much larger bandwidth than other PA architectures. Besides, this mode of operation is highly efficient. In addition, the PAE at back-off operation is boosted with the back-gate bias of the 28 nm CMOS FD-SOI technology.

Parameter	PLS	[III.14]	[III.15]	[III.16]	[III.29]	[III.34]
Technology	28nm CMOS FD-SOI	28nm CMOS Bulk	28nm CMOS Bulk	28nm CMOS FD-SOI	120nm BiCMOS	130nm BiCMOS
Freq. [GHz]	28	30	28	27	28	28
BW [%]	42	14	17	7	-	14
Gain [dB]	15	15.7	13.6	17.5	15.3	21.2
$P_{SAT}$ [dBm]	16.2	14	19.8	18.7	18.6	17.1
PAE <sub>max</sub> [%]	38	35.5	43.3	12.4	34	41
PAE 8 dB BO [%]	21	12	16	-	13	19

Table 3.4: Post-layout simulation results comparison with state of art 28 GHz PAs.

## 8. Circuit Measurement

Fig. 3.48 (a) shows the photograph of the power amplifier. The measurement setup is shown in Fig. 3.48 (b) and (c). For the measurements, the PNA (Purpose Network Analyzer) E8361A from Agilent Technologies is used. The operating frequency of this network analyzer ranges between 10 MHz and 67 GHz.

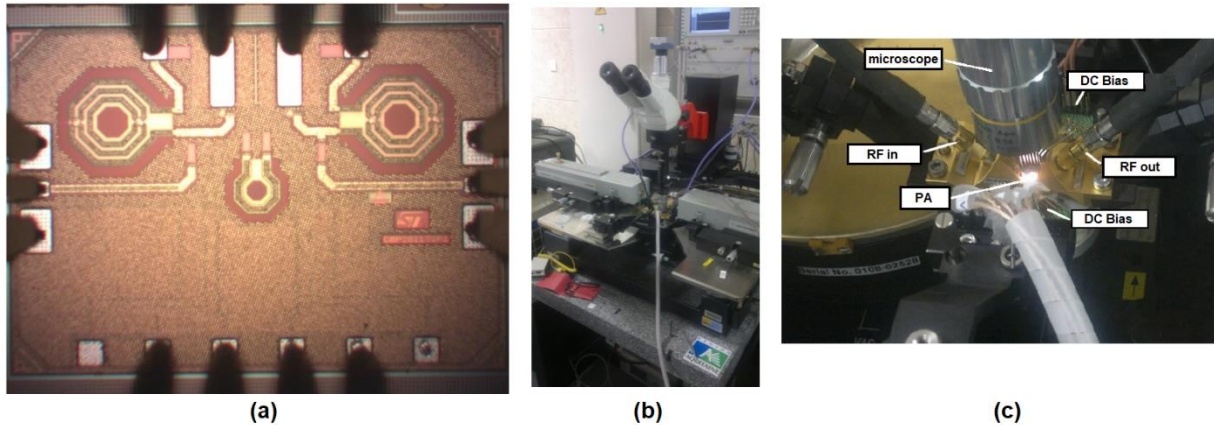


Fig. 3.48: (a) Power amplifier photograph (b) Measurement setup (c) Biasing setup.

S-parameters measurements show that the frequency of operation is importantly shifted compared to the simulation results. As shown in Fig. 3.49, the amplifier shows 15 dB of power gain at 8 GHz and the 3 dB bandwidth covers frequencies between 4.5 and 9 GHz (BW = 56 %). The DC current consumption of this amplifier is 54 mA, the same value obtained with the post-layout simulation results.

In fact, while simulating the amplifier, both the DC and RF grounds were considered as a ground reference in the circuit. In reality, the network analyzer and the DC source do not provide the same physical ground references. Despite that these grounds are connected via measurement cables, this path is very inductive due to the cables. Therefore, the path that provides the lesser impedance between the DC and RF grounds is the path in the integrated circuit.

In the simulations, two grounds were connected to the DC and RF sources, therefore the inductive/resistive paths between the RF ground and the DC ground at the input and the output of the amplifier were not taken into consideration. This will result in a direct change of the input and the output matching networks and the amplifier will not be matched to the  $50 \Omega$  ports at 28 GHz and hence the frequency of operation of the circuit will be shifted.

While designing the circuit, the focus was made to minimize the impedance of the path between the source of the transistor and the DC ground pad. And in order to know the accurate value of the impedance of the ground return path of the transistor sources, the DC ground pads are connected via inductive path to the RF ground pads (Fig. 3.53). A redesign of the circuit will present two new ground pads in the upper-side of the circuit (Fig. 3.53). However, since the distance  $D_0$  must be higher than  $300 \mu\text{m}$  in order to measure the circuit,  $D_H$  or  $D_V$  must increase in length. Increasing  $D_0$  will result in an increase of the ground source inductance of the transistors, and increasing  $D_H$  will result in longer path of the RF path travelling from the input port to the output port.



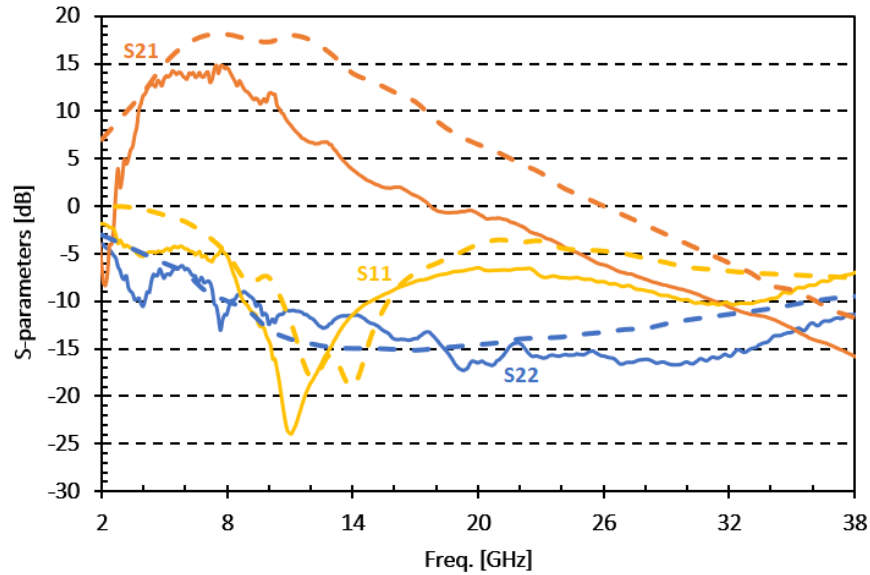


Fig. 3.49: S-parameters measurements (solid lines) and redo simulations (dashed lines).

Redo simulations were made while removing the ground references placed on the RF pads. As shown in Fig. 3.50 the results are in accordance with the measurement results and the S-parameters of the amplifier were shifted due to the mismatch.

The minor deviations between the redo simulation results and the measurements are attributed to many factors such as the metal stack and model inaccuracies, the measurement cables and environment and the process variations. In fact, the value of the capacitances of this technology process varies above 20 % [III.35], this will affect the results since a capacitance is used in the output matching network of the circuit.

Changing the input and output ports load impedances in order to cancel the effects of the RF ground impedance can be done via source-pull and load-pull measurements. In this way the circuit could be matched at 28 GHz but with performance penalties.

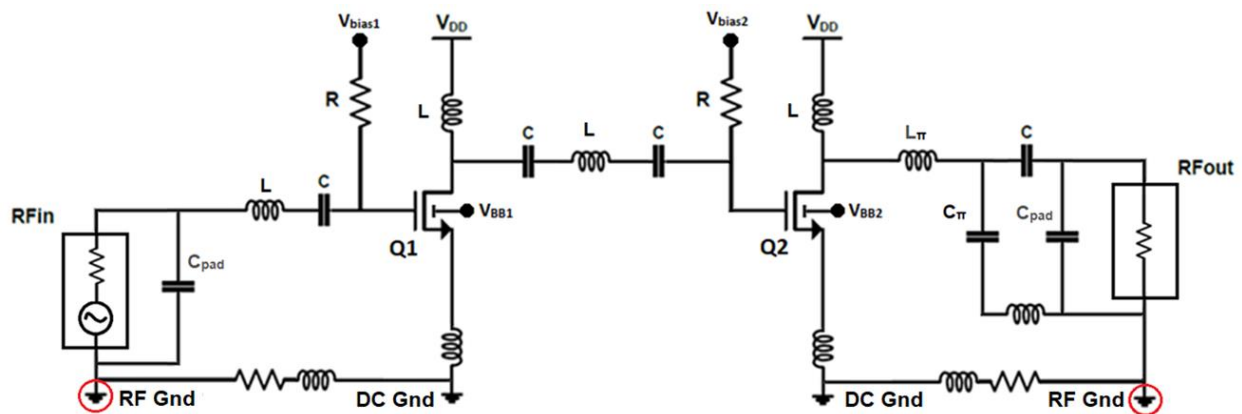


Fig. 3.50: Simulated schematic of the amplifier showing the RF ground path.

### CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

Fig. 3.51 shows the S-parameters of the PA when the DC sources were turned OFF. In this state the maximum gain is reached in the 28 GHz band and there is no shift in the frequency of operation. As shown in Fig. 3.51, the redo simulations with zero DC voltages show an agreement with the measurements.

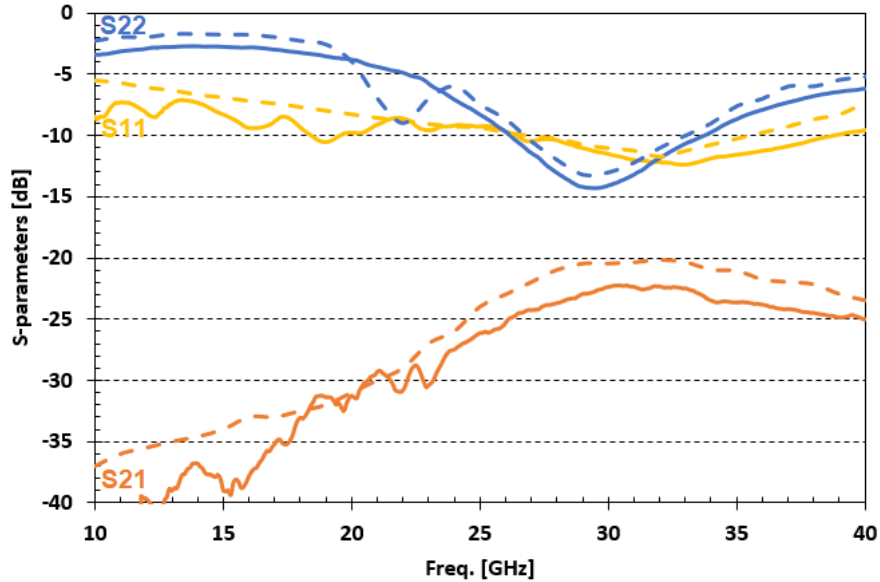


Fig. 3.51: S-parameters measurements (solid lines) and redo simulations (dashed lines) with DC sources turned OFF.

A power sweep was carried out to this circuit at 8 GHz. With  $50 \Omega$  input and output ports, this circuit achieves 10 dBm of saturated output power and 12.8 % of PAE (Fig. 3.52). As mentioned above, the DC current consumption of this amplifier is around 54 mA, the same value obtained with the original PLS results.

Since the matching networks were not optimized at 8 GHz, load-pull measurements were carried out. As shown in Fig. 3.52, the PAE and the saturated power increased to 20.2 % and 11.9 dBm respectively although the input and inter-stage matching networks were not optimized at 8 GHz.

CHAPTER III: POWER AMPLIFIERS ON THE 28 NM CMOS FD-SOI TECHNOLOGY

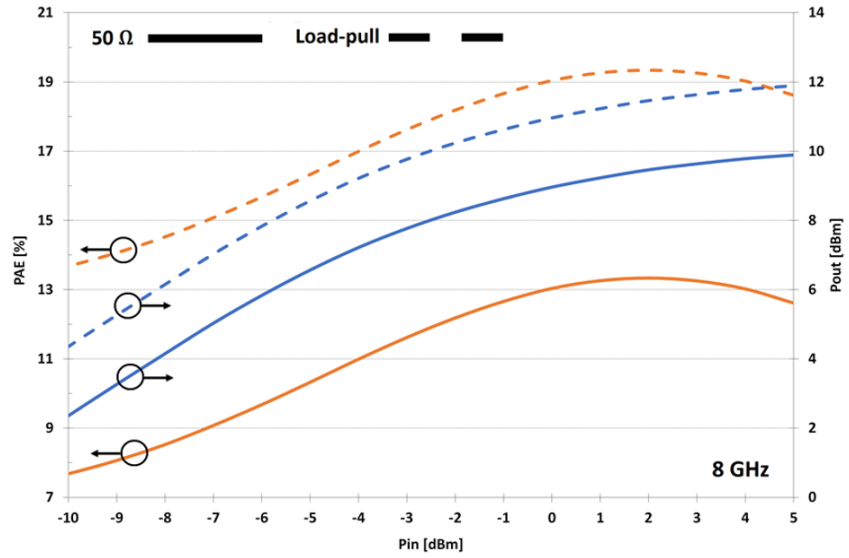


Fig. 3.52: Measured output power and PAE of the amplifier at 8 GHz.

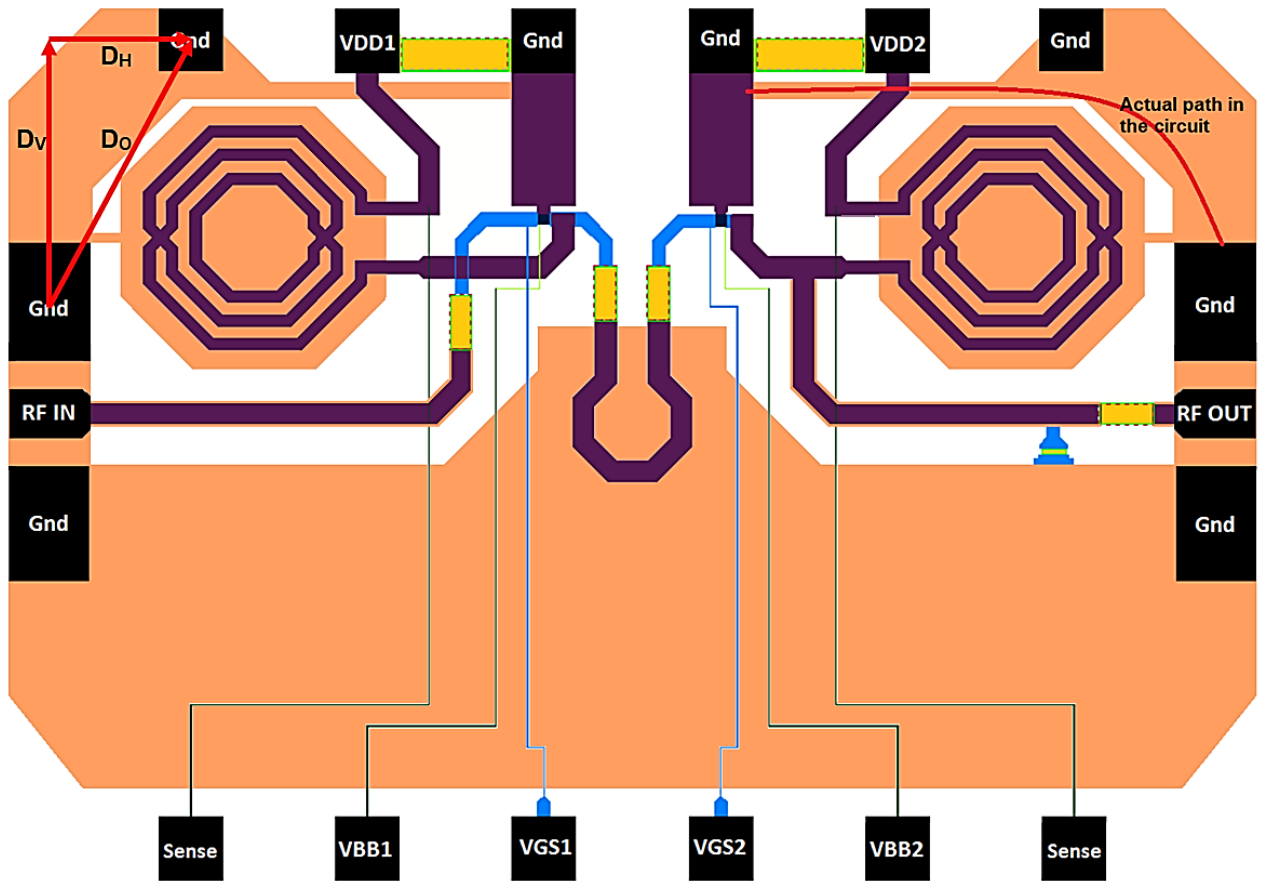


Fig. 3.53: Layout with the added ground pads in the upper-side of the circuit.



### Conclusion

In this chapter, we presented a study and analysis of the advanced technology, the 28 nm CMOS FD-SOI, for 5G power amplifier applications. This advanced technology node is very promising to boost the CMOS potential in RF circuits. In addition, the 28 nm CMOS FD-SOI offers many opportunities for circuit designers such as the back-gate basing.

After reviewing the 5G power amplifiers specifications, it is concluded that the high efficiency, particularly at back-off operation, the linear behavior and the wide bandwidth of operation are among the most needed requirements. Afterwards, the overview of the state of art CMOS 5G PAs showed that no single-ended amplifier was demonstrated. However, since this structure presents many advantages such as the wide bandwidth, it was chosen in our design. In addition, the class AB has always been chosen in the state of art 5G CMOS PAs. Analyzing the different modes of operations made us conclude that the class AB could be improved while optimizing the harmonic impedances. Therefore, the class J mode was chosen to be studied in this work. In fact, state of art class J amplifiers achieve highly efficient behavior over a wide bandwidth, while maintaining the linearity. The evaluation of this class made us conclude that it is highly adequate for millimeter wave frequencies thanks to its output matching network and since it absorbs the parasitic capacitance of the transistor.

Consequently, a single-ended two stage class J amplifier was designed with the 28 nm CMOS FD-SOI technology of STMicroelectronics. Post-layout simulation results show at 28 GHz a power gain of 15 dB, a saturated output power of 16.2 dBm and a maximum PAE of 38 %. In addition, the back-off PAE is boosted and the linearity of the amplifier is reconfigurable with the back-gate biases of the PA. Moreover, the percentage bandwidth of this amplifier is 42 % covering the 5G frequency bands candidates from 24 to 34 GHz.

Finally, circuit measurements show that the frequency of operation of the circuit is shifted since the ground reference was not properly set between the DC and the RF sources, introducing a mismatch at the input and the output of the PA. This highlights the difficulty of designing a single-ended amplifier topology at millimeter wave frequencies since the ground return path present impedances that increase with higher frequencies resulting in a decrease of the performances. These impedances are canceled in the differential structure thanks to its symmetry.

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# GENERAL CONCLUSION AND PERSPECTIVES

The thesis presented in this manuscript focuses on the design of integrated power amplifiers on emerging and advanced technologies for 5G applications.

In fact, as the size of the silicon transistors is reaching the atomic scale, the scientific community is intensively searching for new materials (emerging technologies) and new device concepts (advanced technologies) in order to guarantee the evolution of solid-state electronics.

Besides, with the rising evolution of wireless devices and services, the race to deploy fifth generation of wireless technologies is ongoing. The research is directed on the millimeter wave carrier frequencies as a result of the demand for high speed data and the need for more spectrum bandwidth. One of the major challenges of the 5G is reducing energy consumption. In fact, the power efficiency is directly related to the reliability and cost of the communication systems.

The radiofrequency power amplifier is one of the most critical building blocks in the radio transceivers as it is the most power consuming element in these systems. Thus, 5G PAs are being spotlighted and research in this area is crucial for next generation communication systems.

Consequently, the objective of this thesis is to study and design power amplifiers on emerging and advanced technologies for 5G applications. Therefore, the contribution of this work is carried out on two different axes.

On the emerging technologies axis, graphene is the precursor candidate. Thanks to its exceptional physical properties, many state of the art graphene transistors with high frequency performances were reported. However, few graphene circuits and even fewer amplifiers have been demonstrated. Hence, many details about the potential performance of graphene transistors in electronics applications remain ambiguous. For instance, the large signal performances of graphene amplifiers have never been reported. Consequently, in this work we carried out an investigation and evaluation of different graphene transistors, with different methods of fabrications and substrates, for power amplifier applications.

Three 2.5 GHz integrated common source power amplifiers, based on three graphene FETs with different fabrication methods, were designed with accurate transistor modeling and electromagnetic simulations. A major difficulty in designing these amplifiers is to match them to the 50  $\Omega$  input and output ports. Post-layout simulation results show power gains ranging between 7 and 12 dB per stage. The maximum output power and PAE reported for a single stage are 6 dBm and 5.6 % respectively. Then, two stage GFET PA were designed. Results show the advantage of stage combining in terms of power gain, while achieving better tradeoffs between the performances. Conclusively, given the recent history of graphene transistors the power gain of these devices is remarkable. However, the output power and efficiency of graphene transistors block their potential in RF PA applications.

Concerning the perspectives for this technology, it is very difficult to predict the future of graphene circuits as it all depend on the progress in the fabrication methods. Despite the advancements in GFETs, there are still many issues that need to be solved before graphene has commercial potential.

## GENERAL CONCLUSION AND PERSPECTIVES

In particular, improving the current saturation and developing a fabrication process for achieving low contact resistances is absolutely vital for graphene in order to find its way in power amplifier applications.

Research on new graphene device concepts such as the Graphene Bipolar Transistor can be promising. Moreover, since graphene transistors must offer serious advantages in order to replace the well-established technologies, a promising direction that could be pursued in graphene research is to complement the conventional semiconductors instead of trying to replace them. In addition, graphene could find its way in specific applications such as flexible electronics.

On the advanced technologies axis, the 28 nm CMOS FD-SOI is very promising to boost the CMOS potential in RF circuits applications. With both  $f_T$  and  $f_{max}$  exceeding 300 GHz, this advanced technological node offers many opportunities for RF circuit designers such as the back-gate basing. Therefore, this technology is used for designing an amplifier according to the analyzed 5G PA specifications: the high efficiency, particularly at back-off operation, the linear behavior and the wide bandwidth of operation.

The contribution of the thesis in this axis is also focused on examining different PA architectures in accordance with the analyzed 5G specifications and in order to achieve large bandwidth. The overview of the state of art CMOS 5G PAs showed that no single-ended PA is demonstrated despite the advantage of this structure in terms of bandwidth. In addition, the sinusoidal class AB has always been chosen. Studying the different classes of operations made us conclude that the class AB could be improved while optimizing the harmonic impedances. Therefore, the class J mode was chosen to be studied in this work. In fact, state of art class J amplifiers achieve highly efficient behavior over a wide bandwidth, while maintaining the linearity. With no evaluation of this class in the CMOS technology, our study concluded that this class is highly adequate for millimeter wave frequencies thanks to its output matching network and since it absorbs the parasitic capacitance of the transistor.

Consequently, a single-ended 28 GHz two stage class J amplifier was designed with the 28 nm CMOS FD-SOI technology of STMicroelectronics. Post-layout simulation results show at 28 GHz a power gain of 15 dB, a saturated output power of 16.2 dBm and a maximum PAE of 38 %. In addition, the back-off PAE is boosted and the linearity of the amplifier is reconfigurable with the back-gate biases of the PA. Moreover, the percentage bandwidth of this amplifier is 42 % covering the 5G frequency bands candidates from 24 to 34 GHz.

Circuit measurements show that the frequency of operation of the circuit is shifted since the ground reference was not properly set between the DC and the RF sources, introducing a mismatch at the input and the output of the PA. This highlights the difficulty of designing a single-ended amplifier topology at millimeter wave frequencies since the ground return path present impedances that increase with higher frequencies decreasing the performances.

DC measurements show a 54 mW of DC consumed power, the same value obtained with the simulations. S-parameters show a maximum gain of 15 dB at 8 GHz with a very large bandwidth of 56 %. Large signal measurements with 50  $\Omega$  ports show a 10 dBm of saturated power and 12.8 % of PAE. These performances are improved with the load-pull measurements at 8 GHz that boosted the PAE and the saturated power to 20.2 % and 11.9 dBm respectively.

## GENERAL CONCLUSION AND PERSPECTIVES

Concerning the perspectives of this part of the work, source-pull and load pull measurements at 28 GHz can eliminate the mismatches at the input and output ports. Besides, the reconstruction of the ground plane of the circuit while properly setting the ground reference will lead to the desired performances at 28 GHz.

On the other hand, it can be very interesting to design a class J amplifier with a differential structure. However, no implementation or even theoretical study on this subject are done to this day. In fact, the design of baluns, that present a complex inductive load at the fundamental and a pure capacitive load at the second harmonic, is still an undiscovered field.