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Methodology for EMC Analysis in a GaN Based Power Module

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Methodology for EMC Analysis in a GaN Based Power Module

Méthodologie d'Analyse de la CEM dans un Module de Puissance à Composants GaN

Thèse de doctorat de l'Université Paris-Saclay
préparée à L'École Normale Supérieure de Cachan
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Thèse présentée et soutenue à Cachan, le 20/12/2017, par

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PREFACE

This chapter at the very beginning of the dissertation has been finished at the very end of the writing period. It brings reflection on what has been gone through the past three years and a half as well as the acknowledgement to people it may concern.

The first question that comes to my mind is: What has a PhD brought to me? (or isn't it a waste of time since I decided to go to industry anyway?) Even being titled "Dr LIU", people would say that you work as an engineer which you should have started to do so three years ago; and during these years you have got lower payment and your colleagues of your age might have gain their three years' professional experiences and even have been promoted somehow.

My answer is: A pleasure to do a research. A pleasure, a curiosity to analyze, to understand, to extract, to communicate and to optimize; not only in professional domains like science and engineering, but also in personal life as being a husband or father in proper ways. Various difficulties, whether physical or mental, have been gone through during these years, these experiences do make me more easily to comprehend, to summarize and to figure them out. After all, there is no single methodology for all but there is indeed a spirit to guide you to an effective and efficient one.

I would like to express my gratitude to all people involved in my PhD, from those I spend time together every day to those I hardly speak with: "Thank you, thank you all!"

As a PhD student of SATIE laboratory, I feel so grateful to encounter these researchers and classmates providing me an environment full of innovating and rigorous spirit as well as humorous moments. It is my proud moment to say "I am a saticien". Only some words are far from sufficient to express how I would love to keep a life long relationship with you people, both personal and professional.

From my PhD defense examiners to those who questioned me as I was presenting my work at a conference, I would also present my thanks. You helped me a lot to improve my communication skills and left me inspirations.

As my PhD funding project, MEGaN allowed me to learn how a national level research project works involving both universities and industries. As a contributor and an observer, I was able to better understand the cooperation in different research units.

RESUME

Grâce aux propriétés physiques du matériau et à l'avancement de l'ingénierie et de la fabrication, les composants à semi-conducteurs basés sur le nitrure de gallium (GaN) sont des candidats prometteurs pour la conception des modules de puissance à haute fréquence, à haut rendement et donc à haute densité de puissance. Cependant, la commutation rapide des composants GaN entraîne des très fortes variations de tension (dV/dt) et de courant (dI/dt) pendant la commutation. Elles, combiné avec des éléments parasites inductifs (L) et capacitifs (C) dans le module de puissance, donnent lieu aux perturbations électromagnétiques (EMI) dans une large gamme de fréquences. Cette thèse est axée sur la méthodologie d'analyse de la CEM dans un module de puissance basé sur des composants GaN.

Afin d'étudier les problèmes susmentionnés, un module de puissance complet comprenant les composants de puissance au GaN et le conditionnement du module doit être caractérisé et modélisé afin que les performances CEM puissent être reconstruites par simulation avec ces modèles. Les méthodes de modélisation d'un transistor à haute mobilité électron (HEMT) et d'un module de puissance conçu au laboratoire sont décrites respectivement aux chapitres I et II,

- La modélisation du composant GaN se compose de la partie statique et de la partie dynamique. Le premier concerne de la modélisation des caractéristiques I-V y compris la conduction inverse ; le seconde permet de représenter les capacités intrinsèques non linéairement dépendantes de la tension entre chaque paire de bornes. La méthode de modélisation est basée sur les caractéristiques extraites de la fiche technique et peut être adaptée à tous les e-mode composants GaN HEMT.

- La modélisation du packaging du module implique principalement l'extraction des capacités parasites entre le module et le radiateur et les inductances parasites entre le condensateur de bus DC et les dispositifs d'alimentation. Les extractions sont traitées à la fois par calcul numérique avec logiciel ANSYS Q3D et par mesure d'impédance avec un analyseur de réseau vectoriel E5061B. Les résultats de ces deux approches correspondent bien de l'un à l'autre.

Une fois que le modèle complet du module de puissance est construit, il est validé par un test de commutation expérimental où les formes d'onde de tension de commutation et les

perturbations CEM simulées sont comparées aux mesures respectivement aux chapitres III et IV. Le banc d'essai extérieur du module de puissance GaN est modélisé pour compléter le modèle de simulation. Les précautions de mesure sont également présentées.

- Les formes d'onde de commutation sont obtenues en mode de double impulsions et en commutation permanente et sont comparées à celles simulées; elles sont cohérentes avec une bonne précision. La minimisation des surtensions aux bornes des transistors en utilisant des condensateurs embarqués dans le module C_X est analysée et finalement la valeur du condensateur C_X est recommandée selon différentes situations.

- Les perturbations CEM sont mesurés en termes de courants de mode commun (MC) et de mode différentiel (MD) grâce à des réseaux stabilisés d'impédance de ligne (RSIL) et sont comparées avec celles simulées entre 100 kHz et 30MHz. Les chemins des propagations de la perturbation de MC du module et de la charge de l'inducteur de résistance. Les effets des condensateurs C_X et C_Y sont étudiés. Enfin, la répartition des condensateurs de filtrage de MC dans différents localisations est étudiée par simulation.

ABSTRACT

Thanks to the material's physical properties and the advancement in the engineering and manufacturing, power semiconductor devices based on Gallium Nitride (GaN) are promising candidates for high frequency, high efficiency and thus high power density power module design. However, GaN devices' fast switching results in high slew rate in switching voltage (dV/dt) and current (dI/dt), combined with parasitic inductive (L) and capacitive (C) elements within the power module, gives rise to electromagnetic interference (EMI) noise in a wide frequency range. This dissertation is focused on the methodology for EMC analysis in a GaN based power module.

In order to study the aforementioned issues, an entire power module including the GaN power devices and the module's packaging are to be characterized and modeled so that the EMI performances can be reconstructed by simulation with these models. The modeling methods of a commercial enhancement-mode (e-mode) GaN High-Electron-Mobility-Transistor (HEMT) and a lab-designed power module are discussed respectively in chapter I and II,

- The device modeling involves the static part and the dynamic part, where the former is modeled to represent the forward I-V characteristics and the reverse diode-like conducting ones and the latter is modeled to represent the nonlinearly voltage dependent intrinsic capacitances between each pair of terminals. The modeling method is based on the characteristics extracted from datasheet and can be scaled to all e-mode GaN HEMT.
- The packaging modeling involves mainly the extraction of the stray capacitances between the module and the heatsink and the parasitic inductances between the DC link capacitor and the power devices. The extractions are processed by both numerical calculation with software ANSYS Q3D and impedance measurement with a vector network analyzer E5061B. The results from these two approaches match well from one to the other.

Once the full model of the GaN based power module is built, it is validated with experimental switching tests where the simulated switching waveforms and the EMI noises are compared with the measured ones, respectively in chapter III and IV. The test bench apart from

the GaN power module is modeled to complete the full simulation model. The measurement precautions are presented as well.

- The switching waveforms are obtained in double pulse and permanent switching tests and are compared to the simulated ones, where they are correctly matched. The minimization of the switching voltage's overshoot by using between DC+ and DC- the in-module capacitors C_X is analyzed and finally the capacitor C_X 's value is recommended in different situations.
- The EMI noises are measured in terms of common mode (CM) and differential mode (DM) currents in the Line-Impedance-Stabilized-Network (LISN) and are compared with the simulated ones where they are correctly matched from 100 kHz up to 30MHz. The CM noise propagation paths from the power module and from the resistor-inductor load are analyzed. The effects of the in-module capacitors C_X and the CM filter ones C_Y are studied. Finally the distribution of filter capacitors in different locations is studied by simulation.

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ABBREVIATION

CM – Common Mode	SC-FP – Source Connected Field plate
DM – Differential Mode	Si -- Silicon
d-mode – Depletion mode	SiC – Silicon Carbide
DUT – Device under test	SMD – Surface Mounted Device
EMI – Electromagnetic Interference	2DEG – Two Dimensional Electron Gas
e-mode – Enhancement mode	VNA – Vector network analyzer
ESL – Equivalent Series Inductance	WBG – Wide Bandgap
ESR – Equivalent Series Resistance	
FFT – Fast Fourier transformation	
GC-FP – Gate Connected Field plate	
GaN – Gallium Nitride	
GIT – Gate Injection Transistor	
HEMT – High Electron Mobility Transistor	
HFET – Heterostructure Field Effect Transistor	
HV – High voltage	
IC – Integrated Circuit	
IGBT – Insulated Gate Bipolar Transistor	
LISN – Line Impedance Stabilized Network	
LV – Low voltage	
MLCC – Multilayer Ceramic Capacitor	
MOSFET – Metal Oxide Semiconductor Field Effect Transistor	

GENERAL INTRODUCTION

The presented research work in this dissertation has been carried out at Laboratoire des Systèmes et Applications des Technologies de l'Information et de l'Energie (SATIE) of the Ecole Normale Supérieure de Cachan – Paris Saclay University from February 2014 to August 2017. This research work is funded by the national industrial research project – MEGAN (Module Electronique en Nitrure de Galium), in which it contributes to the GaN power device's modeling and advanced power module design optimization regarding to electromagnetic interference reduction. The GaN power module and GaN power devices developed by CEA-LETI are supposed to be studied in this work; however, due to its unavailability during the entire PhD, a commercial GaN power device and a lab manufactured power module have been studied instead. The methodologies are to be scaled to other similar GaN technologies.

Scope of the work

Thanks to the material's physical properties and the investment in the engineering and manufacturing infrastructure, power semiconductor devices based on Gallium Nitride (GaN), such as high-electron-mobility-transistor (HEMT), allows faster switching and less power losses comparing to Silicon (Si) and/or Silicon Carbide (SiC) devices. Therefore they are promising for high-frequency, high current and high efficiency power conversion. With GaN HEMT's small die formed packages, high power density and modularized design can be achieved.

However, GaN HEMT's fast switching results in high slew rate in voltage (dV/dt) and current (dI/t). These high dV/dt and dI/dt combined with parasitic inductive and capacitive elements in the power module will result in electromagnetic interference (EMI) noise in a wide frequency range, which will cause both conducted and radiated emission problems in differential mode (DM) and common mode (CM).

The main research topic of this dissertation is the modeling of a power module based on GaN HEMT for the purpose of understanding the switching and EMI characteristics under the influence of the parasitic elements. Afterwards, optimization approaches will be pointed out in the power module design's point of view.

The modeling of a power module includes the modeling of the power semiconductor device – the GaN HEMT and the modeling of the power module's packaging. The former is

based on the coding of the mathematical representations of the measured static and dynamic characteristic of the power device; the latter is based on the representation of the equivalent lumped impedance network of the conductive structure.

In order to validate the above mentioned models, a test bench should be designed, manufactured and finally tested in order to compare the measured results with the simulated ones. After the validation with the measurement of the test bench, the model can be further explored for parametric studies in order to develop general optimization approaches.

The main approaches have been carried out:

- GaN device modeling

The modeling of the enhancement mode (e-mode) GaN HEMT is based on the static and dynamic characteristics, as in traditional modeling process. The static part of an e-mode GaN FET is different from a traditional Si MOSFET since the former is a bidirectional switch whose reverse conduction bias depends on the gate turn-on voltage; the dynamic part, similar to other power transistors, have voltage dependent capacitances between each pair of electrodes. Both the static and dynamic characteristics are represented by mathematical equations which are adapted to SPICE-like (or VHDL-AMS) coding.

- Power module and switching environment modeling

The power module's packaging can be modeled with lumped impedance by software as ANSYS Q3D, which is based on the concept of partial inductance; meanwhile, the main parasitic elements of the module's model can be verified by impedance measurement with an impedance analyzer or a vector network analyzer (VNA). In addition, the rest of the switching environment – the DC link capacitor, the Line Impedance Stabilization Network and the load resistor and inductor – are modeled with lumped impedance by the impedance measurement with proper calibration and compensation procedures.

- Validation

The combination of the models of different parts of the switching system (GaN HEMT, power module's packaging, load, DC link capacitor and the LISN) are validated by the test bench in terms of the switching and the EMI noises evaluations. The former is essential since the

waveforms of switching voltage and current determines the switching loss and the EMI noises; the latter allows validating the modeling of both the EMI noise sources and their propagation path.

Chapter preview

Based on the scope of the work, this dissertation is divided into four chapters:

In Chapter 1, the GaN technologies – from the semiconductors material’s properties to the state-of-the-art power device’s structure and characteristics – are presented at first; then the behavioral modeling process of a typical e-mode GaN HEMT is presented with the mathematical expressions and the coding techniques.

In Chapter 2, the power module design based on wide band gap (WBG) devices and the relevant parasitics’ concern are reviewed; then an academic GaN power module is designed and modeled, together with its associated elements such as the DC link capacitor and the gate driver board.

In Chapter 3, the switching performance of this GaN power module is evaluated under the double pulse test; the using of the ceramic capacitor close to the GaN HEMT in order to minimize the switching voltage overshoot is analyzed.

In Chapter 4, the DM and CM EMI noises are measured without and with different value/type in-module ceramic capacitors, in different load connection configurations; these measurements are compared with the simulation results. Finally a parametric study with the in-module and external ceramic capacitors is done in order to evaluate their filtering effects.

CHAPTER 1

MODELING OF HIGH VOLTAGE E-MODE GAN HEMT

The power semiconductor device is the core of a power module and it determines the power module's electric performances together with the parasitic elements due to its packaging and its gate driver system. Therefore, in order to investigate into a Gallium Nitride (GaN) based power module, the GaN based power devices should be investigated at first.

This chapter starts with a review of the GaN technologies, from the material's physical properties and the structure of the two-dimension electron gas (2DEG) to the state-of-the-art 600V GaN power transistor of both cascode structure and enhancement mode (e-mode). In addition the devices' packaging is discussed.

Then a commercial 600V e-mode GaN HEMT (GS66508X from GaNSystems) with die formed package is characterized and modeled as an example since it will be used for the following study in this dissertation. The modeling includes the behavioral mathematical representations and coding process. The modeling procedure is divided into the static and dynamic parts, where the former is temperature dependent. This modeling method is adapted to global e-mode GaN HEMT.

1.1 GaN overviews – from material to device

The physical properties of the semiconductor materials combined with the manufacturing and engineering make birth a power device such as MOSFET or IGBT applied for ~mW RF amplifiers up to ~MW railway inverters. Reviewing a semiconductor technology such as GaN is an issue from the material's physics to the power device structure.

1.1.1 GaN material basics

1.1.1.1 Why GaN ?

Silicon (Si) has been a dominant material for power switches for the last half century. Its advantages over earlier semiconductors (e.g. germanium or selenium) could be expressed in the following four categories [LIDOW 15]:

- 1) New application enabled
- 2) More reliable
- 3) Easier to use
- 4) Lower cost

Compared to Si, Wide Band Gap (WBG) materials such as Gallium Nitride (GaN) and Silicon Carbide (SiC) are promising candidates for the next generation power devices for enabling faster switching and lower power loss. A brief comparison between the relevant properties of the three different semiconductors is shown in **Fig. 1-1**.

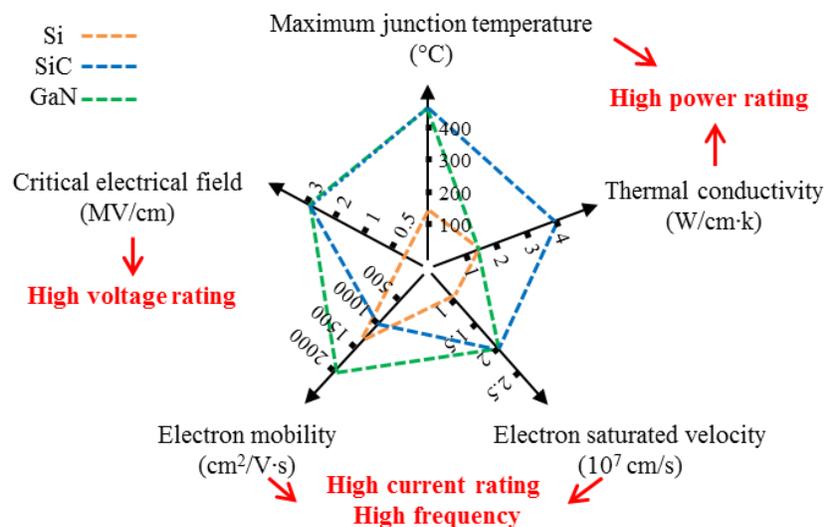


Fig. 1-1: Si, SiC and GaN materials' properties

It is explicit to calculate the best theoretical performance for each of the three materials to evaluate the corresponding power device's performances such as the break down voltage (V_{BR}) and the on-state resistance ($R_{DS(on)}$).

WBG results in higher critical electrical field (E_{crit}) needed to initiate impact ionization, thus causing avalanche breakdown. The V_{BR} could be approximated with the following equation **Eq 1-1**, which shows that V_{BR} is proportional to the width of the drift region (w_{drift}) and the E_{crit} . Since the E_{crit} of SiC or GaN can be 10 times higher than that of Si, the w_{drift} of SiC or GaN could be 10 times smaller than that of Si for the same V_{BR} .

$$V_{BR} = \frac{1}{2} \cdot w_{drift} \cdot E_{crit} \quad \text{Eq 1-1}$$

In order to support this critical electric field, the number of carriers (e.g. electrons in an N-type semiconductor) between the two terminals could be calculated by Poisson's equation **Eq 1-2**. The total number of electrons in the drift region (N_D) can be 100 times greater in the same V_{BR} , based on the analysis above. This is the reason why GaN and SiC outperform Si in power conversion.

$$q \cdot N_D = \frac{\epsilon_o \cdot \epsilon_r \cdot E_{crit}}{w_{drift}} \quad \text{Eq 1-2}$$

The $R_{DS(on)}$ of this majority carrier device is therefore:

$$R_{DS(on)} = \frac{w_{drift}}{q \cdot \mu_n \cdot N_D} \quad \text{Eq 1-3}$$

According to **Eq 1-2** and **Eq 1-3**, it could be rewritten as **Eq 1-4**, which could be plotted with black lines as shown in **Fig. 1-2**. It should be noted that real semiconductor devices are not always ideal structures. In the case Si MOSFET, it took 30 years to achieve the theoretical limit. The actual GaN device designs, in the range of 600V/900V/1200V voltage rating and either of normally-on or normally-off, are far away from their theoretical limit.

$$R_{DS(on)} = \frac{4 \cdot \mu_n \cdot V_{BR}^2}{\epsilon_o \cdot \epsilon_r \cdot E_{crit}^3} \quad \text{Eq 1-4}$$

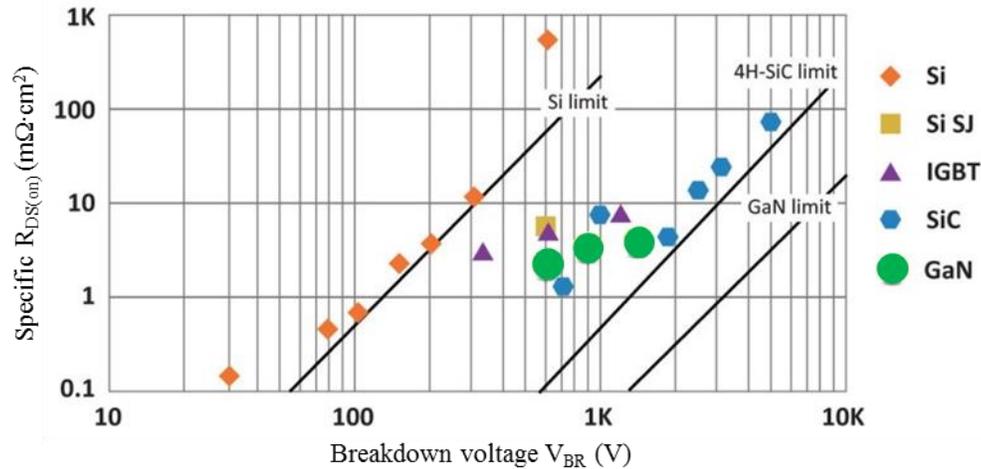


Fig. 1-2: $R_{DS(on)}$ vs. V_{BR} limits for Si, SiC and GaN based devices [Transphorm 16]

1.1.1.2 Two dimensional electron gas (2DEG)

In addition to the material's advantages, the two dimensional electron gas (2DEG) structure reinforces the electrons' mobility. The hexagonal structure of crystalline GaN results in piezoelectric properties, which leads to very high conductivity. This piezoelectricity in GaN is predominantly caused by the displacement of charged elements in the crystal lattice – if the lattice is subjected to strain, the deformation will cause a miniscule shift in the atoms of the lattice that generate an electric field; the higher the strain, the greater the electric field. By growing a thin layer of AlGa_N on top of a GaN crystal, a strain is created at the interface that induces a compensating 2DEG [Asbeck 97] as shown schematically in **Fig. 1-3**. This 2DEG is highly conductive, due to the confinement of the electrons in a very small region at the interface. This confinement also increases the mobility of the electrons from about 100 cm²/V·s (in unstrained GaN) to 1500~2000 cm²/V·s (in the 2DEG region). The high concentration of electrons with very high mobility is the basis for the high electron mobility transistor (HEMT).

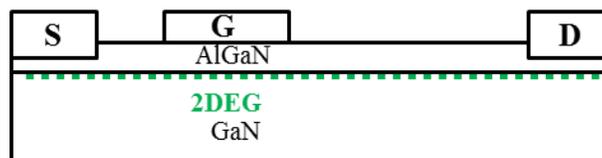


Fig. 1-3: 2DEG in the cross section of AlGa_N/Ga_N interface

1.1.2 GaN devices' structures

GaN based power device could be designed vertically or laterally according to their current flowing direction.

1.1.2.1 Vertical devices

The vertical devices, using structure similar to their Si and SiC counterparts, takes fully advantages of the superior GaN material's properties. According to different layers' organization, GaN-on-GaN design by Hughes Research Laboratories (HRL) [Nie 14] and GaN-on-Si one by Massachusetts Institute of Technology (MIT) [Palacios 15] have been shown with their cross sections in **Fig. 1-4**. However, the lack of availability of high quality and low cost GaN wafers has limited these prospects [Jones 16]. This is the reason why none of the above vertical devices has yet been produced to a commercial level.

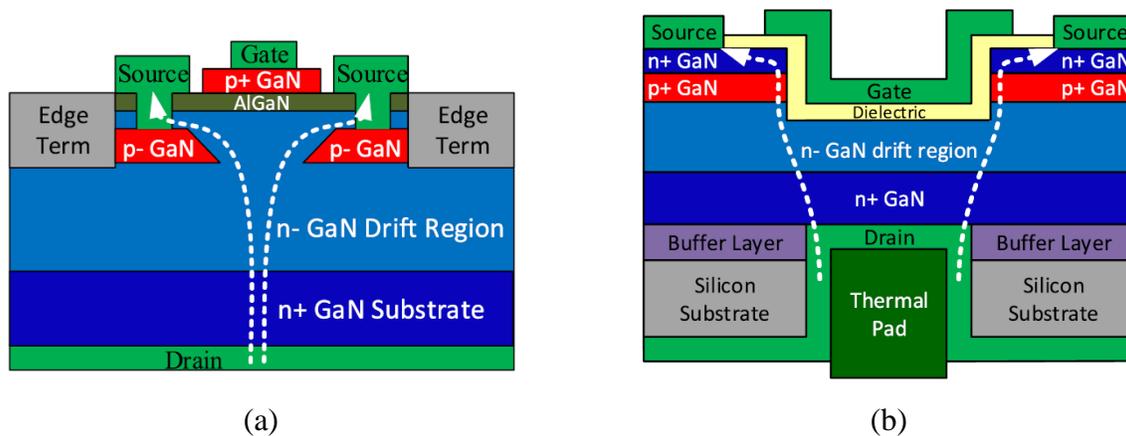


Fig. 1-4: GaN-on-GaN (a) and GaN-on-Si (b) vertical power devices [Jones 16]

1.1.2.2 Lateral devices – depletion mode

Compared to their vertical counterpart, the lateral GaN based device, known as heterojunction field-effect transistor (HFET) or high electron mobility transistor (HEMT), typically rated at 600V up to 1200V, has already entered the power device's market. **Fig. 1-5** shows a basic structure of a lateral GaN HEMT.

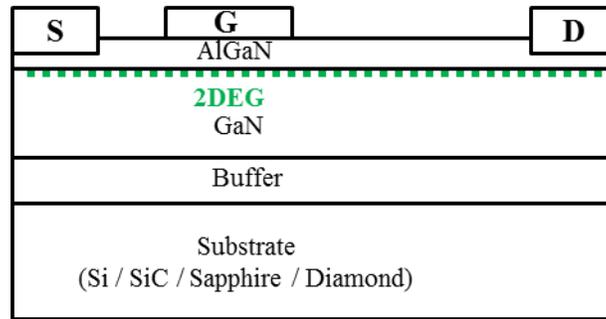


Fig. 1-5: Cross section of a lateral GaN HEMT (normally-on)

The substrate is typically Si or SiC, where the former costs less and the latter costs more but has better thermal performances. In order to deposit the GaN layer on the substrate, a buffer layer (several thin layers of GaN, AlGaN and AlN) has been added between them to provide strain relief. Since the 2DEG layer forms a native conductive channel between the source and the drain, the HEMT is inherently a depletion-mode (d-mode) device. Since a d-mode power transistor is not always desirable in power converter design (e.g. in voltage source inverter, using d-mode device could result in a potential shoot-through during the start-up), it is designed and engineered, by mainly two methods, to switch as a normally-off power device:

- The cascode solution
- The enhancement-mode solution.

1.1.2.3 *Lateral devices – cascode*

The cascode structure in general requires copackaging of a high-voltage (HV) depletion-mode (d-mode) GaN HEMT and a low-voltage (LV) enhancement-mode (e-mode) Si MOSFET. Two typical structures are available in the market:

1) The cascode structure of devices from Transphorm and IR/Infineon (**Fig. 1-6a**) where the two dies are connected in such a way that the drain-source voltage of the low-voltage Si MOSFET determines the gate-source voltage of the high-voltage GaN HEMT. Meanwhile both of them share the same current channel as turned on and their blocking voltages are distributed between them as turned off. This complete normally-off device can be driven by a conventional low-voltage MOSFET driver.

2) The cascode structure of devices from TI and VisIC uses a slight different structure (**Fig. 1-6b**) where the high-voltage GaN HEMT and low-voltage Si MOSFET are connected in series and their gates (G1 and G2) are driven separately by different signals. TI has integrated a driver IC inside the power device package [**TI 16**], which is capable for over-current and over-temperature protections.

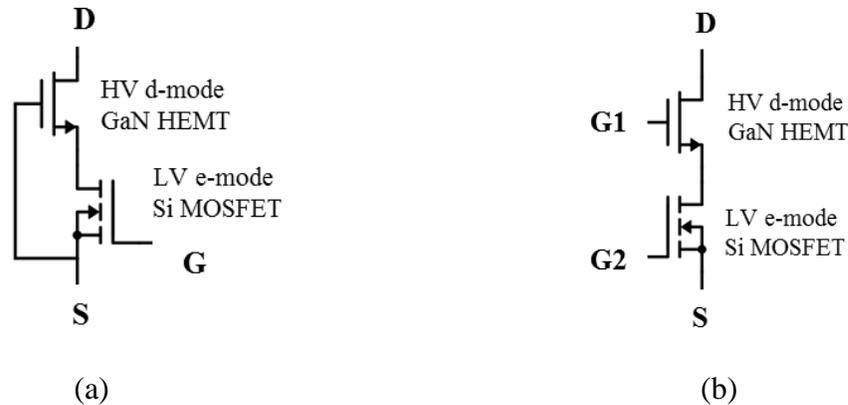


Fig. 1-6: Cascode GaN power device structures of Transphorm (a) and TI/VisIC (b)

The packaging technologies are important since the switching performances of the cascode device rely heavily on 1) the parasitic inductances in the package, especially between the two dies and 2) the match of the junction capacitances in the two devices. Either high parasitic inductance or mismatched capacitances will increase the switching losses significantly [**Huang 14**]. In this case, careful design in a planar architecture instead of wire bonding is more desirable [**Lee 15**].

Another concern is that the low-voltage Si MOSFET adds its own $R_{DS(on)}$ to high-voltage GaN HEMT. However, since $R_{DS(on)}$ increases with the V_{BR} of the device, cascode solution is quite effective when GaN HEMT is high-voltage and the MOSFET is very low-voltage. The chart in the **Fig. 1-7** shows the added $R_{DS(on)}$ to the cascode device by the e-mode low-voltage MOSFET. Apparently the interest of 600V cascode GaN HEMT is proven by 3% added $R_{DS(on)}$ due to low-voltage MOSFET.

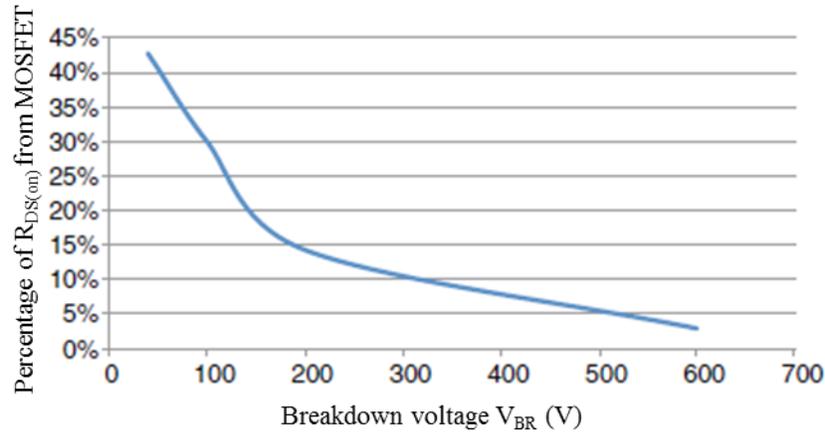


Fig. 1-7: Added $R_{DS(on)}$ to the cascode GaN device by low-voltage Si MOSFET [Lidow 15]

Tab. 1-1 shows the commercial status of main 600V cascode GaN devices. Transphorm is the only vendor selling cascode GaN devices in a relatively large scale while other vendors have produced engineering samples.

Tab. 1-1: Status of 600V cascode GaN devices

Manufacturer	I_{DS} rating (A)	$R_{DS(on)}$ (m Ω)	Q_g (nC)	Package	Availability
Transphorm	9/17/34	290/150/52	6.2/6.2/19	PQFN/TO247	Online ordering
Infineon/IR	10	125	--	PQFN	Samples
VisIC	50	15	35	PQFN	Samples
TI	10	70	--	PQFN	Samples

1.1.2.4 Lateral devices – enhancement mode

Although the 2DEG makes the lateral HEMT naturally depletion mode, the gate can be modified to shift the threshold voltage (V_{TH}) to a positive level and thereby make an enhancement mode (e-mode) device. **Fig. 1-8** illustrates two most commonly used gate modification techniques, which are used to deplete the 2DEG carriers beneath the gate when no voltage bias is applied. A positive gate voltage higher than the V_{TH} then is required to “enhance” the 2DEG channel and thus turn on the switch.

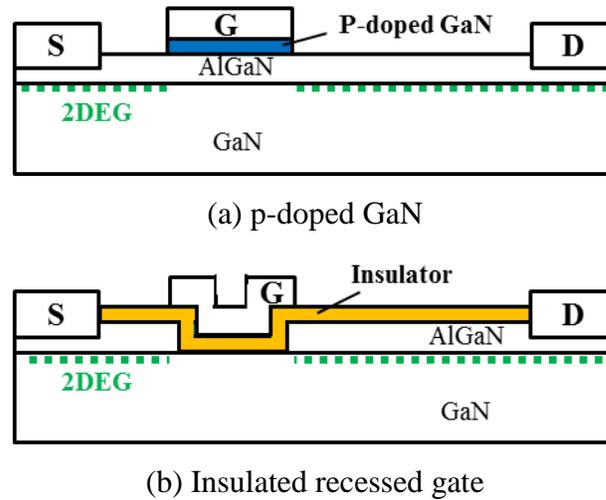


Fig. 1-8: Main gate modification techniques for e-mode GaN HEMTs

EPC, as the first company commercializing e-mode GaN devices up to 200V, uses a p-doped GaN layer beneath the gate (**Fig. 1-8a**). This creates a diode-like characteristic on the gate which shifts the V_{TH} from zero to about 1.5V – a magnitude of the diode voltage drop [**Lidow 15**]. In order to make the 2DEG channel entirely conductive, the gate should be biased at ~5V.

Panasonic uses also a p-doped GaN layer beneath the gate (**Fig. 1-8a**) to create 600V e-mode GaN HEMT. However, maybe due to the etching depth beneath the p-doped GaN layer [**Jones 16**], devices' V_{TH} is about 1.2V and to fully make the 2DEG channel conductive the gate voltage should be at ~3V [**Panasonic 13**].

HRL, later licensing its lateral GaN portfolio to Navitas Semiconductor, uses a recessed gate structure (**Fig. 1-8b**). It involves etching away the AlGaN beneath the gate to a precise depth and depositing with an insulating material which is AlN [**Chu 13**].

CEA-Leti uses also recessed technique as the gate modification since “it has more potential in future to go to lower on-resistance” [**Bush 15**].

GaN Systems, as the first 600V e-mode GaN device supplier in the market, has not published their gate structure. [**Jones 15**] states that they appear to have an insulated gate based on the characterization results.

Tab. 1-2 shows the commercial status of 600V e-mode GaN devices. Even though GaN Systems and Panasonic have launched online ordering, their devices are still pre-engineering ones which means they cannot be used for industrial products.

Tab. 1-2: Status of 600V e-mode GaN devices

Manufacturer	I_{DS} rating (A)	$R_{DS(on)}$ (m Ω)	Qg (nC)	Package	Availability
GaN Systems	15/60	110/27	3/12	Chip scale	Online ordering
Panasonic	15	65	11	TO220/DFN	Online ordering
HRL	15	350	--	--	Samples
CEA-Leti	30/100	--	--	--	Samples

1.1.2.5 *Devices' package*

Fast switching transients increases the impact of parasitic inductances in power and gate loops, which are constituted by device package, printed circuit board (PCB) traces and DC link capacitors' equivalent series inductance (ESL). These parasitic inductances can be lumped as L_d , L_s and L_g (**Fig. 1-9a**):

1) L_d is the main parasitic inductance contributing to the power loop by the device package. The dI/dt of current switching on L_d creates the voltage overshoot which increases switching losses and the device stress.

2) L_s is the common parasitic inductance between the power loop and the gate loop. It couples the dI/dt from the power loop into the gate loop by creating a voltage drop which slows down switching transients and thus worsening switching losses.

3) L_g is the main gate loop parasitic inductance. It increases the impedance of the gate loop and thus increases the possibility of the unintentional CdV/dt turn-on, which will increase the switching loss until a shoot-through.

As for GaN, the device package should be improved from the conventional ones such as TO220 which introduces easily ~ 10 nH in either $L_d + L_s$ or L_g . The strategy should be to remove L_s totally and reduce L_d and L_g as much as possible. The former could be done by using Kelvin source connection (SS connection in **Fig. 1-9b**) and the latter could be improved by minimizing the device package to chip scale. In addition, planar connection is preferred to wire bonding like connections in order to reduce relevant parasitic inductance [**Lee 15**].

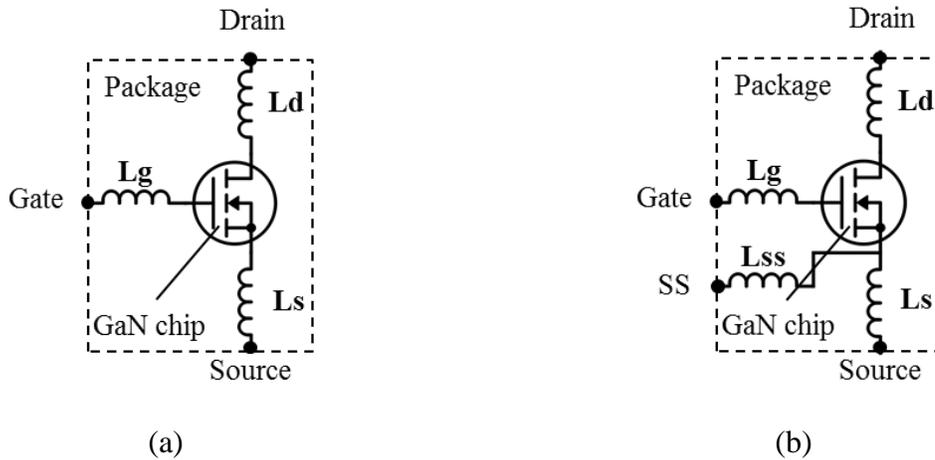


Fig. 1-9: Lumped parasitic inductances in a GaN device package without (a) and with (b) Kelvin sense connection (SS)

Chip scaled device package has been firstly introduced by EPC for its low-voltage GaN devices up to 200V. For 600V device, GaN Systems has several chip scale packages, involve complex fabrication process; while Transphorm, Infineon and Panasonic use traditional surface-mounted PQFN package (8mm×8mm) for their 600V GaN devices in conjunction with some improved internal connection techniques to reduce the parasitics. **Fig. 1-10** compares the sizes of different GaN device (rated 600V/15A) packages with the traditional TO220.

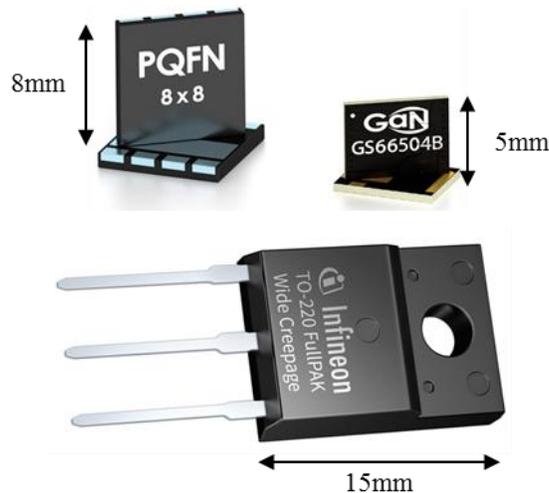


Fig. 1-10: Different package for 600V/15A GaN device – PQFN (top left), GaN Systems (top right) and traditional TO220 (bottom).

Fig. 1-11 shows the complex internal structure of a 10mm×10mm package for a 600V/30A e-mode device which enables the electrical connection and the Si substrate connection at the same side; it is claimed in datasheet that this package introduces only 0.4nH in total for Ld, zero Ls and 1nH for Lg.

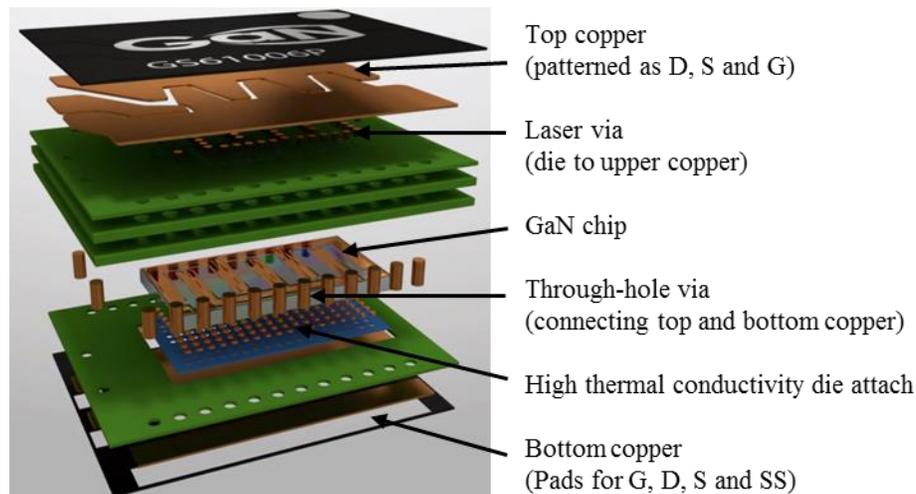


Fig. 1-11: Device package for a 600V/30A GaN HEMT from GaN Systems (GS66508P)

Last but not the least, thermal dissipation path for lateral GaN device is mainly through its Si substrate even though the drain and source contacts contribute as well. Device package design is in two categories: either the drain and source connections are on the opposite sides (**Fig. 1-12a**) to the Si substrate or on the same side (**Fig. 1-12b**). It should be noted that for 600V GaN device, the Si substrate potential must be connected to the source in order to have a stable $R_{DS(on)}$ (further discussed in 1.1.3.2).

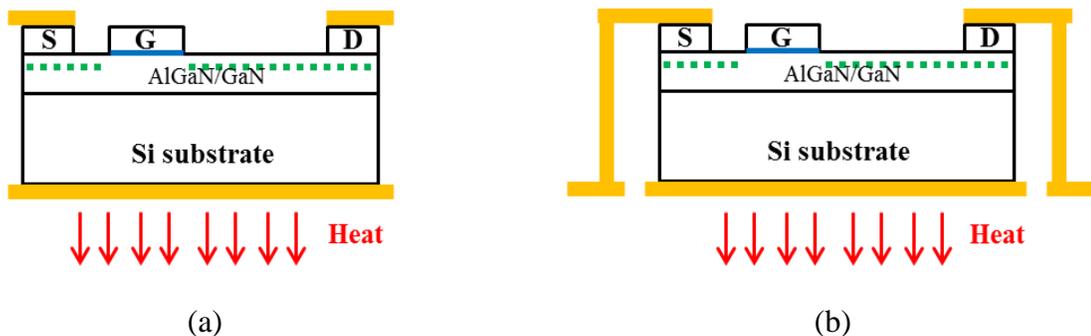


Fig. 1-12: Different electrical connection configurations of lateral GaN device package

1.1.3 E-mode GaN HEMT's characteristics

The material's specialties and the specific device design have made e-mode GaN HEMT some characteristic properties that differentiate it from the previous Si counterparts.

1.1.3.1 *Reverse conduction behavior*

GaN HEMT does not have a body diode as the conventional MOSFET, however, reverse conduction mechanism exists in both cascode and e-mode GaN HEMTs.

In a cascode device, the body diode of the low-voltage MOSFET will turn on when the cascode is reverse biased, then it will turn on the GaN HEMT's channel as well. Since the low-voltage MOSFET's reverse recovery charge (Q_{rr}) is much less than a HIGH-VOLTAGE (real power) MOSFET, the additional Q_{rr} in the cascode is relatively low (since the GaN HEMT has nearly no Q_{rr}).

In an e-mode device, the symmetry of the device makes the channel bidirectionally conductive – The channel will turn on forwardly when the gate source voltage V_{GS} exceeds its threshold $V_{GS(TH)}$ or reversely when the gate drain voltage V_{GD} exceeds its threshold $V_{GD(TH)}$. Typically $V_{GS(TH)}$ and $V_{GD(TH)}$ can be approximated equaling to V_{TH} (**Eq 1-5**). V_{GD} could be represented by **Eq 1-6**. As discussed above, the reverse conduction voltage drop happens at the moment of V_{GD} just exceeds $V_{GD(TH)}$ (**Eq 1-7**).

$$V_{GS(TH)} = V_{GD(TH)} = V_{TH} \quad \text{Eq 1-5}$$

$$V_{GD} = V_{GS} - V_{DS} \quad \text{Eq 1-6}$$

$$V_{GD} = V_{GD(TH)} \quad \text{Eq 1-7}$$

Therefore, the voltage drop in reverse conduction V_{DS} could be represented by **Eq 1-8**, deducing from **Eq 1-5**, **Eq 1-6** and **Eq 1-7**. It should be noted that V_{GS} in **Eq 1-8** is the off-state gate driving voltage which could be zero or negative values.

$$V_{DS} = V_{GS} - V_{TH} \quad \text{Eq 1-8}$$

It is obvious that a negative off-state driving voltage is not desirable because it increases the voltage drop in reverse conduction. **Fig. 1-13** shows a typical reverse conduction characteristic for an e-mode GaN HEMT with different driving voltage V_{GS} .

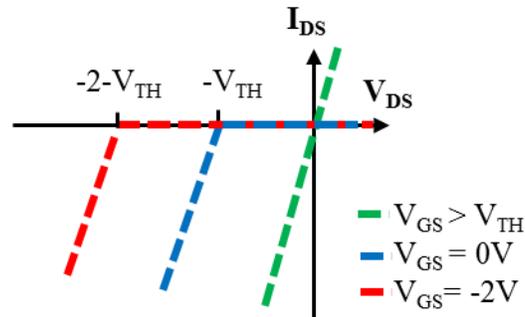


Fig. 1-13: Reverse conduction characteristic of e-mode GaN HEMT

With a V_{GS} of either 0V or -2V, the source-drain voltage drop in reverse conduction is higher than a quality schottky diode which is often used antiparallel with an IGBT. Therefore, dead time control is a must to reduce the reverse conduction losses [Roschatt 17]. Another option for both cascode and e-mode device is to copackage the GaN HEMT with antiparallel Schottky diode, with a compromise of increased switching losses (since the output capacitance of the device is increased) [Morita 12].

1.1.3.2 Dynamic on-resistance $R_{DS(on)}$

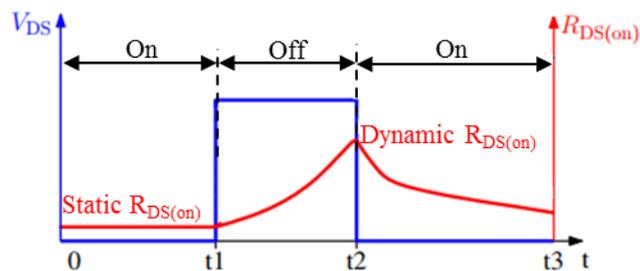


Fig. 1-14: Illustration of dynamic $R_{DS(on)}$ [Li 17]

This phenomenon (also called “current collapse”) in lateral GaN device result in a temporary increase in $R_{DS(on)}$ after certain time on off-state, which is proportional to blocking voltage between drain and source (V_{DS} in blue in figure) and related to the blocking time (t_1 to t_2 in figure). This “dynamic” $R_{DS(on)}$ occurs primarily through two mechanisms: 1) the trapping of surface charges under the gate terminal near the drain edge when the device is turned off; 2) the injection of hot electrons into even deeper traps within the device, particularly in traps caused by carbon doping in the buffer layer.

GaN device manufacturers have made progress to mitigate this phenomenon. Panasonic’s x-GaN GIT uniquely adds a second p-doped drain contact next to the ohmic drain to counteract dynamic $R_{DS(on)}$ [Kaneko 09]. Besides, a primary approach is to use field plates, as shown in Fig. 1-15. Source (S-FP) and gate (G-FP) field plates help to redistribute the gate – drain electric field away from the gate edge [Radhakrishna 13]. In addition, the Si substrate also acts as a field plate so it is recommended to connect the substrate with the source terminal, especially for HIGH-VOLTAGE GaN HEMT [Ikeda 10].

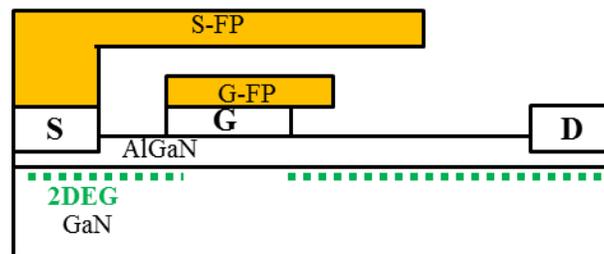


Fig. 1-15: Dual field plates on gate and source of e-mode GaN HEMT

1.1.3.3 Intrinsic capacitances

Charging and discharging between different electrodes during switching introduce capacitive performance for GaN devices, just as their Si counterparts. Three capacitances are lumped as C_{GS} , C_{GD} and C_{DS} whose values are non-linearly variable with voltage between drain and source/gate. The C - V_{DS} profile can be measured by a curve tracer such as B1505a from Agilent with a good precision (\sim pF). Three terminal capacitances can be measured at 1MHz or 100kHz separately thanks to guarding technique [Agilent 11]. Fig. 1-16 shows the measured C - V_{DS} profiles of a commercialized 600V30A e-mode GaN HEMT from GaN Systems

(GS66508P). Several roll-off points are observed. The C_{DS} and C_{GD} capacitance's drop as the voltage bias increases is basically due to the gradual depletion of the free electrons in the 2DEG [p176, Meneghini 16].

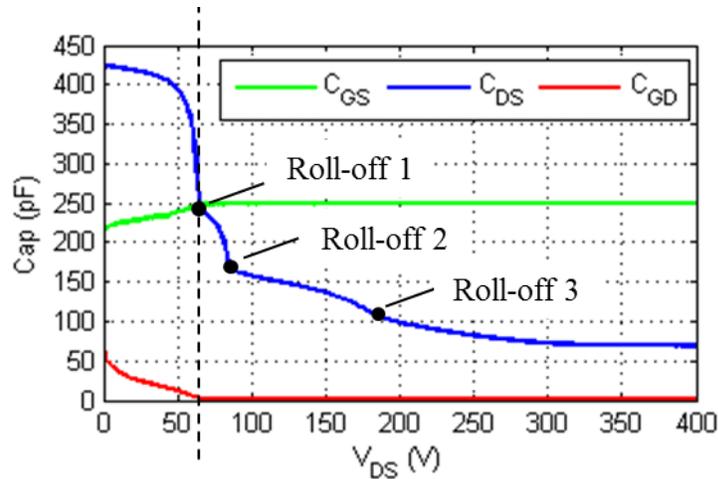


Fig. 1-16: Measured C-V of a 600V/30A e-mode GaN HEMT (GS66508P)

As illustrated in **Fig. 1-17**, with V_{DS} increasing, the electrons' depletion proceeds from the drain-end edge under the gate towards the drain contact. Three roll-off points are observed in the measurement.

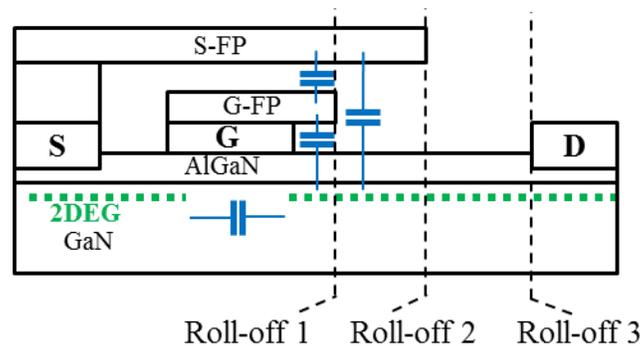


Fig. 1-17: Distribution of capacitances in GaN chip and the frontiers of roll-off points

Roll-off 1 (V_{DS} around 65V) and roll-off 2 (V_{DS} around 85V) are in correspondence with the V_{DS} for which the 2DEG depletion reaches the gate-connected field plate (G-FP) and the source-connected one (S-FP). The incorporation of the two field plate results in the first two capacitance's drop [Ahsan 16]. Roll-off 3 (V_{DS} around 185V) corresponds to the V_{DS} at which

the 2DEG depletion reaches the drain contact. After that, the C_{DS} value decreases very little with a factor of $1/\sqrt{V_{DS}}$ as in traditional MOSFET. Similarly, C_{GD} 's has only one obvious drop due to the depletion of electrons under the GC-FP. C_{GS} 's value is relatively voltage independent since a parallel plate capacitance between the overlying G-FP and S-FP. [Ahsan 16] also shows a temperature dependence of C_{OSS} , this will be beyond the dissertation's concern since the variance is quite small.

1.2 E-mode GaN HEMT's modeling

Accurate modeling of in-circuit power device's behavior is challenging since not only the semiconductor device's characteristics but also the high-frequency parasitic elements in the circuit should be modeled. Most of these parasitics are not only from the device package but from the external electrical connections such as PCB trace or module layout. Specially, cascode device's modeling requires not just accurate models for semiconductor chips, but also all relevant parasitic interconnect elements between the Si MOSFET and the GaN HEMT which influence the switching performance significantly [Huang 14].

In this dissertation, only e-mode GaN HEMT's modeling will be considered. Although it operates similarly to Si MOSFET, previous MOSFET model, such as the BSIM series [BSIM 13], cannot be used directly since in some way they are different in physics. In the following study, a 600V e-mode GaN HEMT from GaN Systems (GS66508P) will be taken as an example for the modeling method developed in this dissertation. Fig. 1-18 shows a side view of a GaN HEMT chip and the corresponding equivalent circuit, consisting various building blocks such as voltage dependent current source I_{CH} , capacitors (C_{GS} , C_{GD} and C_{DS}) and a resistor (R_{dd}), to emulate the actual switching behavior. Before establishing the model, the influences of each element on switching performance are analyzed.

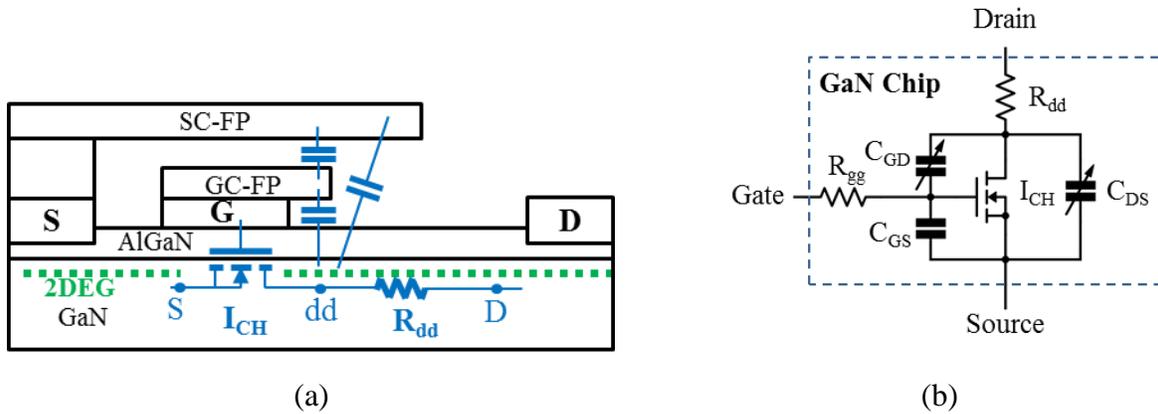


Fig. 1-18: Cross section of a GaN chip (a) and its equivalent circuit (b)

- C_{DS} , C_{GD} : charging and discharging the sum of the two capacitances (C_{oss}) determines the dV/dt especially at turn-off; therefore, they should be precisely modeled to predict the drain-source voltage switching waveforms, thus the common mode EMI noise source in high-frequency range.
- C_{GS} : charging and discharging it determines the variation of the gate voltage and thus the current variation in the 2DEG channel. Since its value is voltage independent it is treated simply as a constant one.
- I_{CH} : determining the transfer characteristic from the gate voltage to the channel current and thus the dI/dt ; therefore, it should be precisely modeled to predict the drain-source current switching waveforms, thus the differential mode EMI noise source.
- R_{dd} : taking a great fraction of the total $R_{DS(ON)}$; responsible for the ohmic loss between every two switching. It is important for the estimation of the total power loss but much less concerned with the switching waveform.
- R_{gg} : influencing the charging time of the gate capacitance; its value is treated constant and can be found in datasheet (1Ω).

All these elements should be modeled through static (I_{CH} and R_{dd}) and dynamic (C_{GS} , C_{GD} and C_{DS}) measurements of the power device by a curve tracer or in datasheet. The following modeling procedure will be based on the characteristics in the datasheet.

1.2.1 Static characteristics modeling

Fig. 1-19 illustrates the static behavior in a lateral high voltage e-mode GaN HEMT, which is determined by a series of a voltage controlled current source I_{CH} and a resistor R_{dd} .

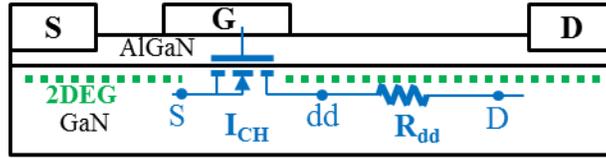


Fig. 1-19: static characteristic of an e-mode GaN HEMT

Under the gate the current source I_{CH} represents the gate-to-2DEG modulation effect, i.e. this current source is conductive or not depending on the voltage applied between the gate (G) and the source (S) or between the gate and the internal drain (dd). In addition, it is also influenced by the voltage applied between the internal drain (dd) and the source (S). This results in a channel resistance R_{CH} when the 2DEG is turned on. Since this modulation effect is totally symmetrical, which means I_{CH} can be bidirectional, this current source can be presented with **Eq 1-9**.

$$I_{CH} = \begin{cases} f(V_{GS}, V_{dds}) & V_{dds} \geq 0 \\ -f(V_{Gdd}, -V_{dds}) & V_{dds} < 0 \end{cases} \quad \text{Eq 1-9}$$

The distance between the gate and the drain contact is relatively long especially in high voltage device. Therefore the resistance of this part of 2DEG (R_{dd}) takes a great fraction of the total channel resistance. The total on-resistance of the device $R_{DS(ON)}$ can be approximated by the sum of R_{CH} and R_{dd} (by neglecting the source side 2DEG resistance, the parasitic resistances in terminal metals and contacts). Therefore,

$$V_{DS} = -V_{SD} = V_{dds} + I_{CH} \cdot R_{dd} \quad \text{Eq 1-10}$$

More equations from the circuit model in **Fig. 1-19** are presented below:

$$I_{DS} = -I_{SD} = I_{CH} \quad \text{Eq 1-11}$$

$$V_{GS} = V_{Gdd} - V_{Sdd} \quad \text{Eq 1-12}$$

Therefore, proper function determining I_{CH} and the R_{dd} should be modeled in order to reconstruct the static characteristic in the full range of temperature.

1.2.1.1 R_{dd} definition at 25°C

The transfer ($I_{DS} = f(V_{GS})$) and reverse ($I_{SD} = f(V_{SD})$) characteristics at 25°C (extracted from datasheet) is shown in **Fig. 1-20**.

In **Fig. 1-20a**, I_{DS} increases with a slight decreasing rate after a threshold voltage (V_{TH}). Still, in low current area, the increasing rate can be reasonably approximated as a constant g_{m1} . Therefore, the current I_{DS} can be represented as in the following equation:

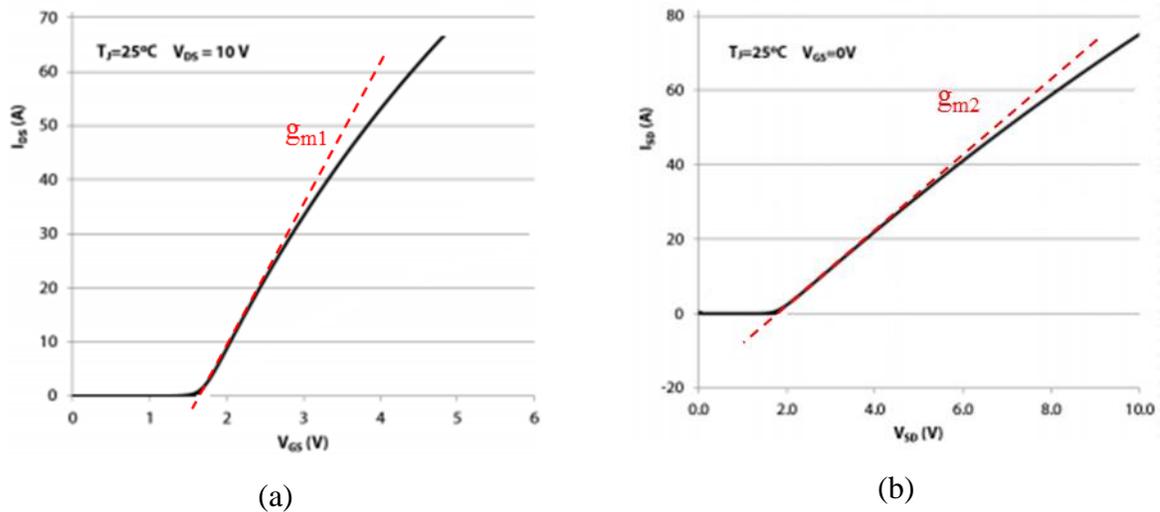


Fig. 1-20: $I_{DS} = f(V_{GS})$ with $V_{DS} = 10V$ (a) and $I_{SD} = f(V_{SD})$ with $V_{GS} = 0V$ (b) characteristics at 25°C (from GS66508P's datasheet)

$$I_{DS} = I_{CH} = g_{m1}(V_{GS} - V_{TH}) \quad \text{Eq 1-13}$$

Since the gate-modulated channel is symmetrical, equation for reverse current I_{SD} can be deduced from **Eq 1-13** as:

$$I_{SD} = -I_{CH} = g_{m1}(V_{Gdd} - V_{TH}) \quad \text{Eq 1-14}$$

From Eq 1-10, Eq 1-12 and Eq 1-14, the following equation is deduced:

$$R_{dd} = \frac{1}{\frac{I_{SD}}{V_{SD} - V_{TH} + V_{GS}}} - \frac{1}{g_{m1}} \quad \text{Eq 1-15}$$

In Eq 1-15, $I_{SD} / (V_{SD} - V_{TH} + V_{GS})$ can be determined by finding the constant increasing rate at low current area in Fig. 1-20b, named as g_{m2} . Therefore, Eq 1-15 can be rewritten as:

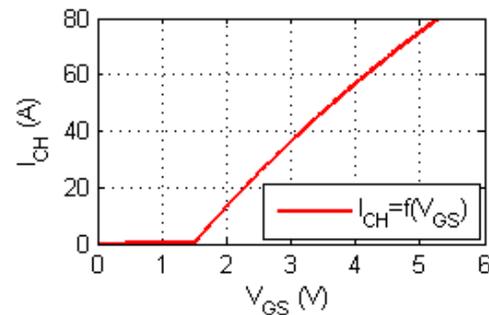
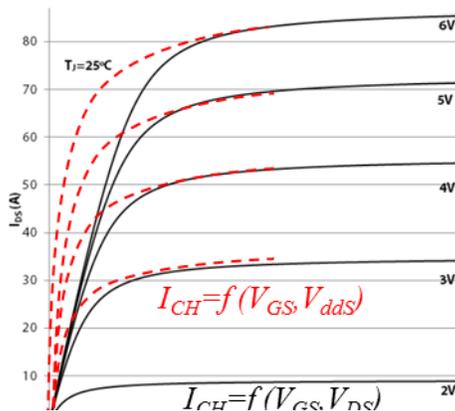
$$R_{dd} = \frac{1}{g_{m2}} - \frac{1}{g_{m1}} \quad \text{Eq 1-16}$$

Finally, R_{dd} at 25°C can be found as 50mΩ by finding g_{m1} and g_{m2} in Fig. 1-20.

1.2.1.2 I_{CH} definition at 25°C

The characteristic of $I_{CH} = f(V_{GS}, V_{ddS})$ can be determined by applying Eq 1-9, Eq 1-10 and Eq 1-11 to the characteristic of $I_{DS} = f(V_{GS}, V_{DS})$, as shown in Fig. 1-21a. This characteristic can be decoupled as $I_{CH} = f(V_{GS})$ and $I_{CH} = f(V_{ddS})$ as shown in Fig. 1-21b and Fig. 1-21c with the relation that:

$$I_{CH} = f(V_{GS}, V_{ddS}) = f(V_{GS}) \cdot f(V_{ddS}) \quad \text{Eq 1-17}$$



(b)

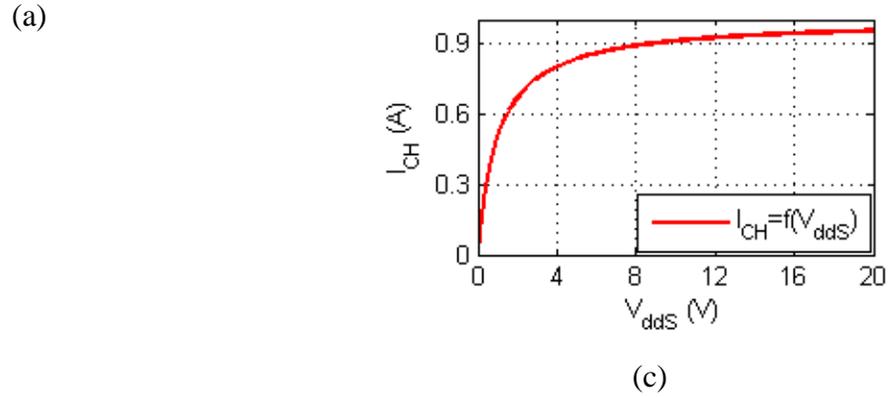


Fig. 1-21: $I_{CH} = f(V_{GS}, V_{ddS})$ characteristic (a) and the corresponding $I_{CH} = f(V_{GS})$ (b) and $I_{CH} = f(V_{ddS})$ (c)

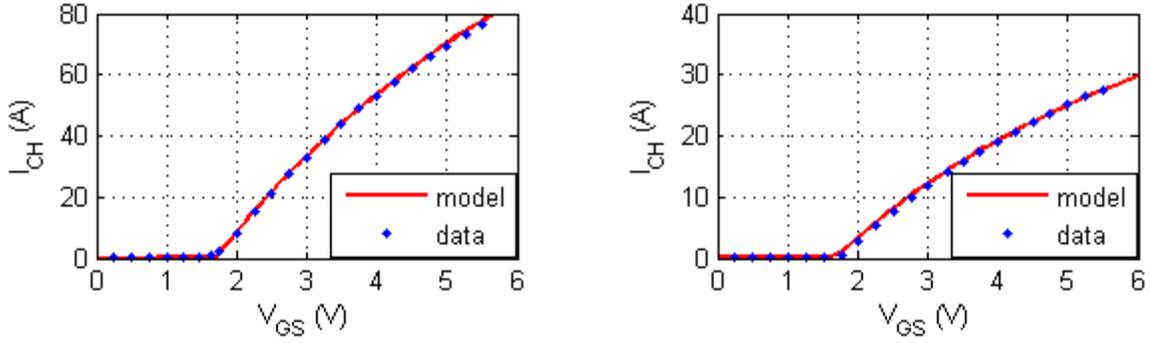
$I_{CH} = f(V_{GS})$ can be found in the transfer characteristic as previously shown in **Fig. 1-20a**. I_{CH} is zero when V_{GS} under the threshold voltage V_{TH} ; then it increases with V_{GS} at a slight decreasing rate. This characteristic can be modeled with **Eq 1-18** given below:

$$I_{CH} = \frac{\ln(1 + \exp(g_m(V_{GS} - V_{TH})))}{1 + b \cdot V_{GS}} \quad \text{Eq 1-18}$$

The term in the numerator is a combination of the two functions in **Eq 1-19**, with g_m representing the trans-conductance at the very beginning. The term in denominator $1 + b \cdot V_{GS}$ tunes the increasing factor g_m to make it decreasing with V_{GS} ; the higher the b is, the faster the g_m decreases.

$$I_{CH} = \begin{cases} 0 & V_{GS} < V_{TH} \\ g_m(V_{GS} - V_{TH}) & V_{GS} > V_{TH} \end{cases} \quad \text{Eq 1-19}$$

g_m , V_{TH} and b can be determined by fitting (e.g. by curve fitting application in Matlab) **Eq 1-18** to the transfer characteristic in **Fig. 1-20a**. The result is shown in **Fig. 1-22**.


 (a) $g_m=37.2$, $V_{TH}=1.7$, $b=0.15$

 (b) $g_m=13.3$, $V_{TH}=1.7$, $b=0.15$
Fig. 1-22: Model fitting to $I_{CH} = f(V_{GS})$ at 25°C (a) and 150°C (b), with $V_{DS}=10V$

$I_{CH} = f(V_{dds})$ can be modeled as *tanh* formed equation as in [Angelov 10] or as **Eq 1-20** shown below, with a_1 / a_2 determining the final value of I_{CH} when V_{dds} is high enough and a_2 the tuning coefficient for the I_{CH} increasing rate. With a constant a_1 / a_2 , the higher the a_1 (or a_2) is, the faster I_{CH} reaches its final value.

$$I_{CH} = \frac{a_1 \cdot V_{dds}}{1 + a_2 \cdot V_{dds}} \quad \text{Eq 1-20}$$

By combining (multiplying) the **Eq 1-18** and **Eq 1-20**, the full equation for I_{CH} could be written as:

$$I_{CH} = \frac{\ln(1 + \exp(g_m(V_{GS} - V_{TH})))}{1 + b \cdot V_{GS}} \cdot \frac{a_1 \cdot V_{dds}}{1 + a_2 \cdot V_{dds}} \quad V_{dds} > 0 \quad \text{Eq 1-21}$$

The a_1 and a_2 should be adjusted especially to fit the curve $I_{CH} = f(V_{dds})$ with $V_{GS}=5V$ or $6V$, depending on at what voltage the device is turned on. **Eq 1-21** is fit to V_{GS} of $6V$, a_1 and a_2 are determined respectively as 4.2 and 4.1 (**Fig. 1-23a**). Even though $I_{CH} = f(V_{dds})$ does not fit well in ohmic part, $I_{CH} = f(V_{DS})$ will finally fit well since the ohmic part is essentially determined by R_{dd} (**Fig. 1-23b**).

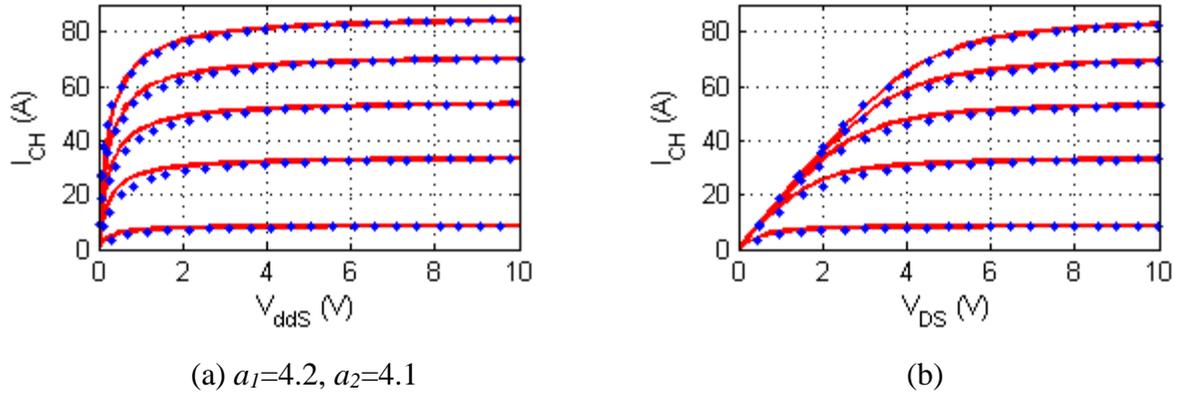


Fig. 1-23: Model fitting to $I_{CH} = f(V_{GS}, V_{ddS})$ (a) and $I_{CH} = f(V_{GS}, V_{DS})$ (b)

Due to the symmetry of the channel, the reverse conduction's equation can be written as:

$$I_{CH} = -\frac{\ln(1 + \exp(g_m(V_{Gdd} - V_{TH})))}{1 + b \cdot V_{Gdd}} \cdot \frac{a_1 \cdot (-V_{ddS})}{1 + a_2 \cdot (-V_{ddS})} \quad V_{ddS} \leq 0 \quad \text{Eq 1-22}$$

Finally reverse characteristic with different V_{GS} value (6V, 0V and -2V) is verified in **Fig. 1-24**. It shows that the reverse voltage drops are correctly modeled.

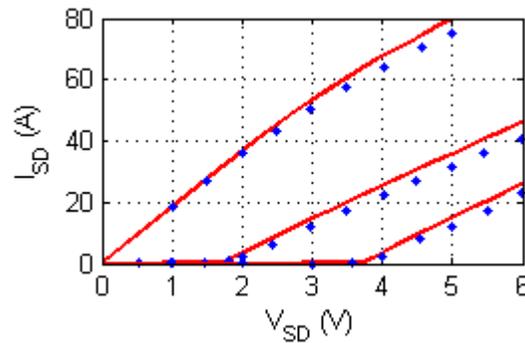


Fig. 1-24: Model fitting to $I_{SD} = f(V_{GS}, V_{SD})$ at 25°C

1.2.1.3 R_{dd} definition at different temperatures

As discussed in 1.1.1.1, the R_{dd} is determined by the number and the mobility of the electrons in the device's 2DEG channel volume between the gate and the drain contact; it has a constant temperature coefficient about $1.3 \cdot 10^{-2}/^\circ\text{C}$ [Lidow 15]. Therefore, it is reasonable to

estimate that R_{dd} varies linearly with temperature. It is already known that $R_{dd@25^{\circ}C}=50m\Omega$; the $R_{dd@150^{\circ}C}$ is yet to determine. It can be determined with the characteristics of the datasheet at $150^{\circ}C$ (**Fig. 1-25**).

The characteristic of $I_{CH} = f(V_{GS})$ with $V_{DS}=10V$ at $150^{\circ}C$ in datasheet is shown in **Fig. 1-25a**. I_{CH} with $V_{GS}=6V$ and $V_{DS}=10V$ can be defined as 30A. Then the $I_{CH} = f(V_{dds})$ with $V_{GS}=6V$ at $150^{\circ}C$ can be defined as in **Eq 1-23** (red curve in **Fig. 1-25b**).

$$I_{CH} = f(V_{dds}) = 30 \frac{a_1 \cdot V_{dds}}{1 + a_2 \cdot V_{dds}} \quad \text{Eq 1-23}$$

The black curve in **Fig. 1-25b** represents the equation below at $150^{\circ}C$:

$$I_{CH} = f(V_{DS}) \quad \text{Eq 1-24}$$

Deducing from the **Eq 1-10**, **Eq 1-23** and **Eq 1-24**, R_{dd} at $150^{\circ}C$ can be found as $150m\Omega$.

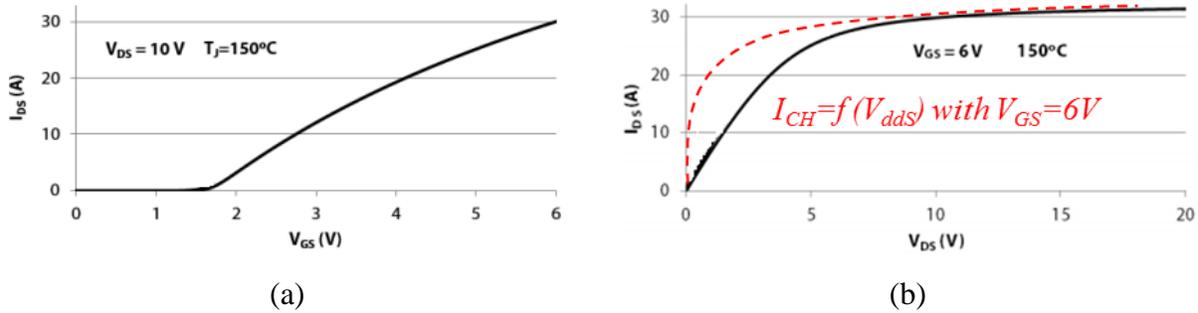


Fig. 1-25: $I_{DS} = f(V_{GS})$ with $V_{DS}=10V$ (a) and $I_{DS} = f(V_{DS})$ with $V_{GS}=6V$ (b) at $150^{\circ}C$

With $R_{dd@25^{\circ}C} = 50m\Omega$ and $R_{dd@150^{\circ}C} = 150m\Omega$, the R_{dd} at different temperature ($R_{dd@Tj}$) can be determined as below:

$$R_{dd@Tj} = R_{dd@25^{\circ}C} + \frac{R_{dd@150^{\circ}C} - R_{dd@25^{\circ}C}}{150 - 25} (T_j - 25) \quad \text{Eq 1-25}$$

From the **Eq 1-25**, R_{dd} values at different temperature (T_j) from $25^{\circ}C$ to $150^{\circ}C$ are shown in **Tab. 1-3**.

Tab. 1-3: R_{dd} at different temperature (25°C to 150°C)

T_J	25°C	50°C	75°C	100°C	125°C	150°C
R_{dd}	50 mΩ	70 mΩ	90 mΩ	110 mΩ	130 mΩ	150 mΩ

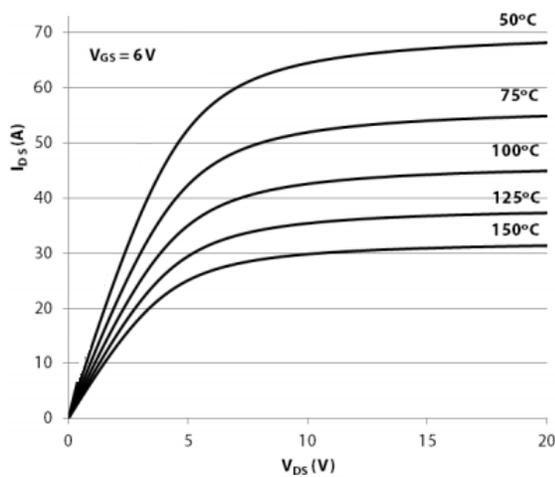
1.2.1.4 I_{CH} definition at different temperatures

The threshold voltage V_{TH} for GaN power device changes quite little with temperature compared with its Si counterparts [Lidow 15], therefore it will be treated as temperature independent.

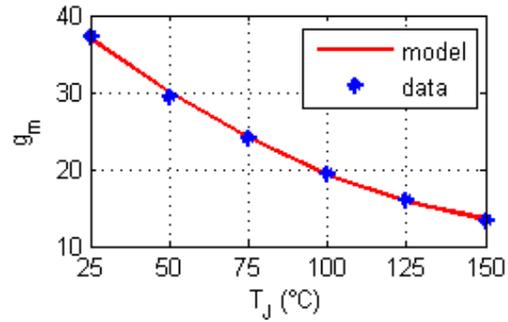
In Eq 1-21 only g_m is treated as temperature dependent. At $V_{GS}=6V$ it can be written as in Eq 1-26:

$$I_{CH} = \frac{\ln(1 + \exp(g_{m@T_J} (6 - 1.7)))}{1 + 0.15 \cdot 6} \cdot \frac{4.2 \cdot V_{dds}}{1 + 4.1 \cdot V_{dds}} \quad \text{Eq 1-26}$$

Then by introducing Eq 1-10 and comparing it with the characteristic $I_{CH} = f(V_{DS})$ with $V_{GS}=6V$ at different temperatures as shown in Fig. 1-26a, $g_{m@T_J}$ at different temperatures (T_J) can be found, as shown in Tab. 1-4.



(a)



(b)

Fig. 1-26: $I_{DS} = f(V_{DS})$ from 50°C to 150°C (a) and the corresponding g_m (b)

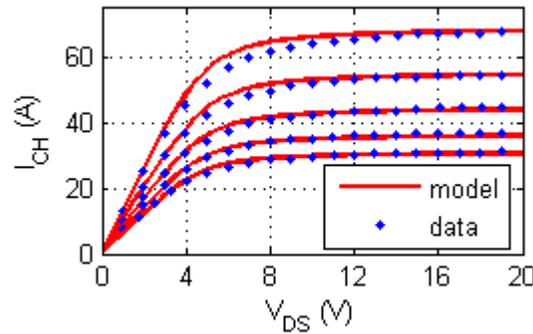
Tab. 1-4: g_m at different temperatures (25°C to 150°C)

T_J	25°C	50°C	75°C	100°C	125°C	150°C
g_m	37.2	29.5	24	19.5	16	13.3

g_m at different temperatures can be modeled as a second order polynomial function as shown in **Eq 1-27**, with $g_0 = 45.2$, $g_1 = -0.353$ and $g_2 = 942.9e-6$. **Fig. 1-26b** shows a comparison between this equation and the data.

$$g_{m@T_J} = g_0 + g_1 \cdot T_J + g_2 \cdot T_J^2 \quad \text{Eq 1-27}$$

A final comparison of $I_{CH} = f(V_{DS})$ when $V_{GS}=6V$ at different temperatures from 50°C to 150°C is shown in **Fig. 1-27**.


Fig. 1-27: Model fitting to $I_{DS} = f(V_{DS})$ with $V_{GS} = 6V$ at different temperature (Downwardly 50°C, 75°C, 100°C, 125°C and 150°C)

1.2.1.5 Final equations and coefficients

The final model is composed by a series of a voltage controlled current source I_{CH} and a resistor R_{dd} . The former is described by **Eq 1-21** and **Eq 1-22**, with the coefficient g_m whose temperature dependence being defined with **Eq 1-27**; the latter is described with a temperature

dependent equation **Eq 1-25**. The temperature is defined manually as a constant value in the model. The final equations and coefficients for the GS66508P GaN HEMT are shown in **Tab. 1-5**:

Tab. 1-5: Equations and coefficients for static modeling of GS66508P GaN HEMT

$$R_{dd} = R_{dd@25^{\circ}C} + \frac{R_{dd@150^{\circ}C} - R_{dd@25^{\circ}C}}{150 - 25} (T_J - 25)$$

$$g_m = g_0 + g_1 \cdot T_J + g_2 \cdot T_J^2$$

$$I_{CH} = \frac{\ln(1 + \exp(g_m (V_{GS} - V_{TH})))}{1 + b \cdot V_{GS}} \cdot \frac{a_1 \cdot V_{dDS}}{1 + a_2 \cdot V_{dDS}} \quad V_{dDS} > 0$$

$$I_{CH} = -\frac{\ln(1 + \exp(g_m (V_{Gdd} - V_{TH})))}{1 + b \cdot V_{Gdd}} \cdot \frac{a_1 \cdot (-V_{dDS})}{1 + a_2 \cdot (-V_{dDS})} \quad V_{dDS} \leq 0$$

$R_{dd@25^{\circ}C} = 50m\Omega$, $R_{dd@150^{\circ}C} = 150m\Omega$, $g_0 = 45.2$, $g_1 = -0.353$, $g_2 = 942.9e-6$ and $V_{TH} = 1.7$

1.2.2 Dynamic characteristics modeling

The charging and discharging of capacitances between different terminals, i.e. C_{GS} , C_{GD} and G_{DS} , voltage dependent but temperature independent (c. f. 1.1.3.3), determine the dV/dt during the switching and thus the switching loss and common mode EMI noise source.

In analytical analysis, these non-linear capacitance variations are often treated as piecewise functions or simply two values respectively for low voltage and high voltage. In simulation, more complicated compact model can be applied for a better precision. A sum of sigmoid functions has been used in this dissertation. The sigmoid function is often used in time domain simulation since it provides better stability and convergence properties [**Napoles 16**]. This function is shown in **Eq 1-28** with C the capacitance value and V the voltage bias. This function describes a value falling from an initial to zero. a_1 , a_2 and a_3 are tuning coefficients.

$$C = a_1 \frac{\exp\left(\frac{-V + a_2}{a_3}\right)}{1 + \exp\left(\frac{-V + a_2}{a_3}\right)} \quad \text{Eq 1-28}$$

- a_1 represents the initial value of C ;
- a_2 is the parameter determining the capacitance's falling point; when $V = a_2$, C falls to the half of its initial value.
- a_3 determines the falling slew rate; the higher a_3 is, the lower is the slew rate.

Two examples are given in with different a_2 (**Fig. 1-28a**) and a_3 (**Fig. 1-28b**).

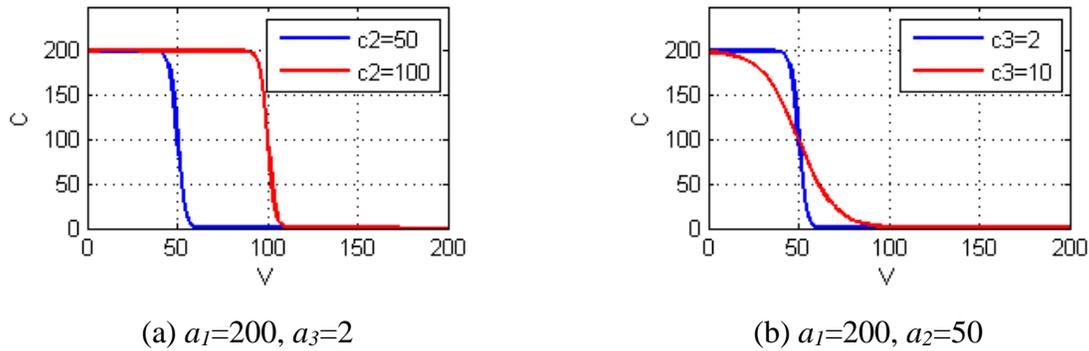


Fig. 1-28: Coefficient influences on the equation **Eq 1-28**

In SPICE like language (PSPICE, LTSPICE etc), capacitance is often modeled with its charge equation. The sigmoid function shown previously (**Eq 1-28**) can be easily integrated on V to obtain a representation of electrical charge (**Eq 1-29**). This is beneficial because it is more robust to model the capacitance in their charge representations to avoid discontinuity and divergence problem [**Mahseredjian 08**].

$$Q = \int C dV = a_1 \cdot a_3 \cdot \ln\left(1 + \exp\left(\frac{-V + a_2}{a_3}\right)\right) \quad \text{Eq 1-29}$$

1.2.2.1 Modeling of the capacitance C_{DS}

Even though the capacitance C_{DS} has three physical capacitance drops (**Fig. 1-16**), the first and second drops can be combined as a single one. **Fig. 1-29a** shows the modeling of the

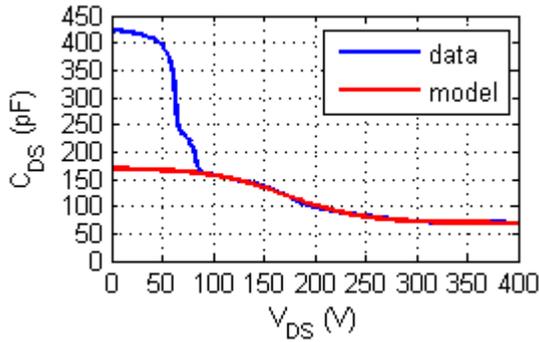
last capacitance drop which is relatively smooth. One sigmoid equation and a constant coefficient a_{cds0} are employed as shown in **Eq 1-30**. The coefficient a_{cds0} can be easily defined as the capacitance at high voltage; the coefficient a_{cds1} is defined as the difference between the starting C_{DS} value and a_{cds0} . The coefficients a_{cds2} and a_{cds3} can be tuned by fitting the curve to the measurement.

$$C_{DS} = a_{cds0} + a_{cds1} \frac{\exp\left(\frac{-V_{DS} + a_{cds2}}{a_{cds3}}\right)}{1 + \exp\left(\frac{-V_{DS} + a_{cds2}}{a_{cds3}}\right)} \quad \text{Eq 1-30}$$

Based on the previous modeling, another sigmoid function is added to **Eq 1-30** in which all coefficients are already determined. The modeling procedure is the same as the previous one and the final result is shown in **Fig. 1-29b** with **Eq 1-31**.

$$C_{DS} = a_{cds0} + a_{cds1} \frac{\exp\left(\frac{-V_{DS} + a_{cds2}}{a_{cds3}}\right)}{1 + \exp\left(\frac{-V_{DS} + a_{cds2}}{a_{cds3}}\right)} + a_{cds4} \frac{\exp\left(\frac{-V_{DS} + a_{cds5}}{a_{cds6}}\right)}{1 + \exp\left(\frac{-V_{DS} + a_{cds5}}{a_{cds6}}\right)} \quad \text{Eq 1-31}$$

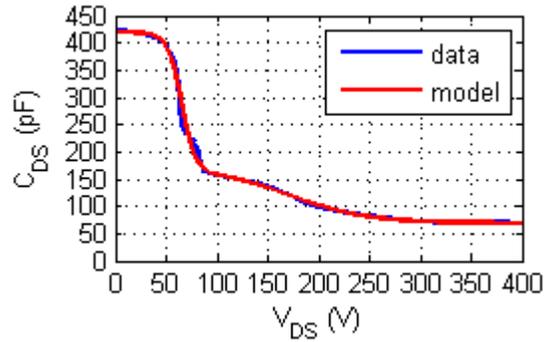
Of course this final equation can be applied directly to some curve-fitting program such as the application of Curve-fitting in Matlab.



$a_{cds0}=69e-12, a_{cds1}=101e-12, a_{cds2}=173, a_{cds3}=38$

(Eq 1-30)

(a)



$a_{cds4}=251e-12, a_{cds5}=65, a_{cds6}=7$

(Eq 1-31)

(b)

Fig. 1-29: Model fitting to $C_{DS} = f(V_{DS})$

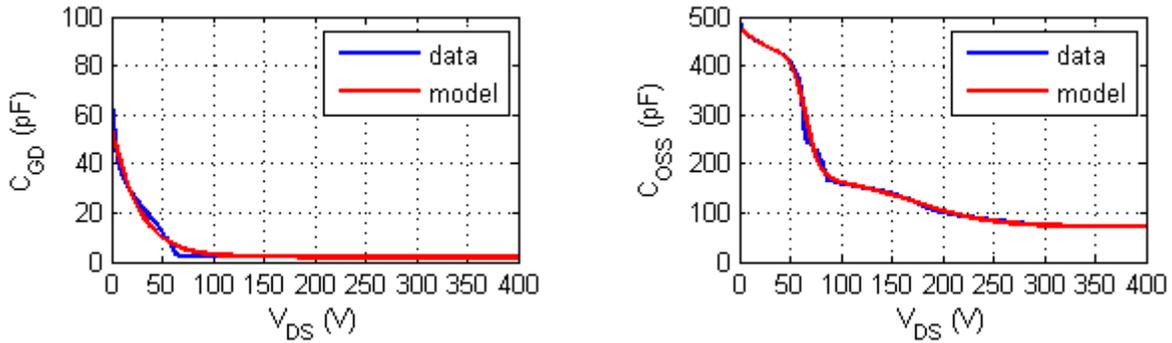
1.2.2.2 Modeling of the capacitance C_{GD}

The modeling of C_{GD} is simple since there is only one capacitance drop. By fitting Eq 1-32 to the measurement, the coefficients are determined as shown in Fig. 1-30a. A comparison of C_{OSS} ($C_{GD}+C_{DS}$) between measurement and model is shown in Fig. 1-30b.

$$C_{GD} = a_{cgd0} + a_{cgd1} \frac{\exp\left(\frac{-V_{DS} + a_{cgd2}}{a_{cgd3}}\right)}{1 + \exp\left(\frac{-V_{DS} + a_{cgd2}}{a_{cgd3}}\right)} \quad \text{Eq 1-32}$$

1.2.2.3 Modeling of the capacitance C_{GS}

Even though there is a small capacitance increase at low voltage, the value of C_{GS} which influences the switching is the one at high voltage V_{DS} . Therefore, C_{GS} is modeled as a constant value 249pF.



$$a_{cgd0}=2e-12, a_{cgd1}=309e-12, a_{cgd2}=-38, a_{cgd3}=24$$

(Eq 1-32)

(a)

(b)

Fig. 1-30: Model fitting to $C_{GD} = f(V_{DS})$

1.2.3 Package parasitics

GS66508P has a package a little larger than its GaN chip in form as shown in **Fig. 1-12b**. Its internal structure is shown in **Fig. 1-31** by x-ray analysis. In the earliest datasheet of the device and the actual official model of the device, 0.2nH has been given for L_d and L_s ; 1nH has been given for L_g and L_{ss} .

However, it is obvious that the common parasitic inductance between the power loop and the gate loop (L_m) cannot be eliminated totally. In fact L_m is not only contributed by the common path of the power loop and gate loop but also by the mutual inductive effect of the two loops. It is reasonable to estimate the L_m value to 0.5nH~1nH (value comparable to L_g or L_{ss}). Even though L_m 's value is quite slight, coupling with a very high dI/dt will still create very significant effect. This will be further discussed in the following chapter (c. f. 3.2.1).

1.2.4 Coding

The e-mode GaN HEMT GS66508X's model is coded in SPICE language, based on a commercial device model [**EPC 11**] (c. f. Appendix A). It should be noted that only the power semiconductor die is modeled, all the parasitic elements will be added manually in simulation.

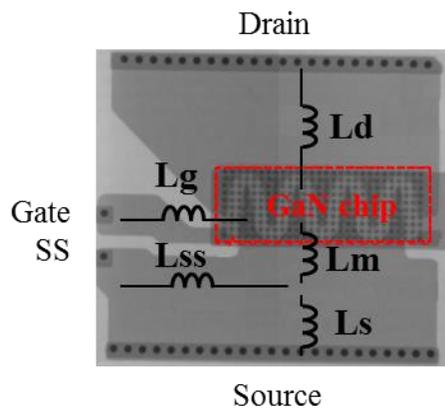


Fig. 1-31: X-ray internal structure in the package of GS66508P and equivalent parasitics

1.3 Conclusions

As the heart of a power module, the GaN based power device is investigated and modeled in this chapter.

In the first half of this chapter, the GaN technologies are reviewed, from the material's physical properties and the structure of the two-dimension electron gas (2DEG) to the state-of-the-art 600V GaN power transistor of both cascode structure and enhancement mode (e-mode). In addition the devices' packaging is discussed.

In the second half of this chapter, a commercial 600V e-mode GaN HEMT (GS66508X from GaNSystems) with die formed package is modeled as an example. This modeling approach is based on the device's characteristics in the datasheet and it is divided into the static and dynamic part, where the former is temperature dependent. The behavioral mathematical equations and coding process are presented in detail. This modeling method is adapted to global e-mode GaN HEMT.

CHAPTER 2

DESIGN AND MODELING OF GAN POWER MODULES

The switching event of the semiconductor device is the origin of both switching loss and EMI noises. The variation of the switching speed (dI/dt and dV/dt) and the switching frequency is a contradictive issue since the unidirectional variation only favorable for the reduction of either EMI noises or switching loss. Therefore, the choice of switching speed and frequency is a tradeoff between the EMI and power losses – which is quantified by the volume of EMI filter and the power devices' heatsink.

The switching waveforms not only depend on the semiconductor devices' characteristics but also are influenced by the parasitic elements in a switching cell which is formed by a DC link capacitor and a pair of semiconductor devices, as long as the gate driver. In addition, certain parasitic elements especially capacitive ones, between the semiconductors' terminals and the ground potential, form the propagation path for the common mode EMI noise. Therefore, the identification of the relevant parasitic elements is essential for the EMI prediction.

The modeling of the GaN power device has been developed previously, then the modeling of a power module, which contributes essentially relevant parasitic elements to the switching event or EMI propagation path, is discussed in this chapter.

This chapter starts with a brief resume of the relevant parasitic elements in a power module and discusses the design rule for the fast switching wide band gap (WBG) power devices. Then the state-of-the-art low inductive power module designs are presented followed with the two module designs in MEGAN project. Finally the SATIE power module's design, which is for academic research purpose in this dissertation, is presented.

This chapter finishes with the modeling of the SATIE power module with the DC link capacitor and its gate driver board. The modeling methods are based on numerical calculation and impedance measurement.

2.1 Requirement for WBG power module design

2.1.1 Parasitics in power modules

The discrete power device (single chip packaged) has been discussed in the last chapter. However, the most used power units (beyond hundreds of watts) are the power modules. A power (semiconductor) module involves power semiconductor chips, forming certain functional topology (e.g. one or several inverter legs) via some kinds of interconnection (bonding-wires, busbar or the top layer of substrate), being attached (soldered or sintered) to some electrically insulating but thermally well conductive substrate (ceramic etc). The backside of this substrate is attached to a grounded heatsink. These power modules provide higher power density, better thermal management and higher reliability compared to discrete power devices

A power module should be in conjunction with some other obliged units (**Fig. 2-1**): 1) a gate driver board to control the power chips of the module; 2) DC link capacitor(s) to store energy or filter low frequency ripple.

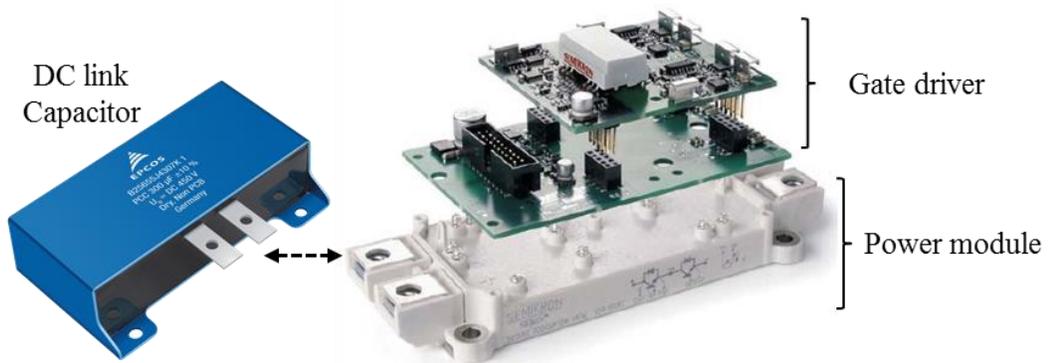


Fig. 2-1: Classic configuration of a power module system

Due to the interconnections between different power units, parasitic elements appear. A power module of one inverter leg, connected to a bulk capacitor to form a “switching cell”, is taken as example. The main relevant parasitic elements are presented as lumped impedances as shown in **Fig. 2-2**.

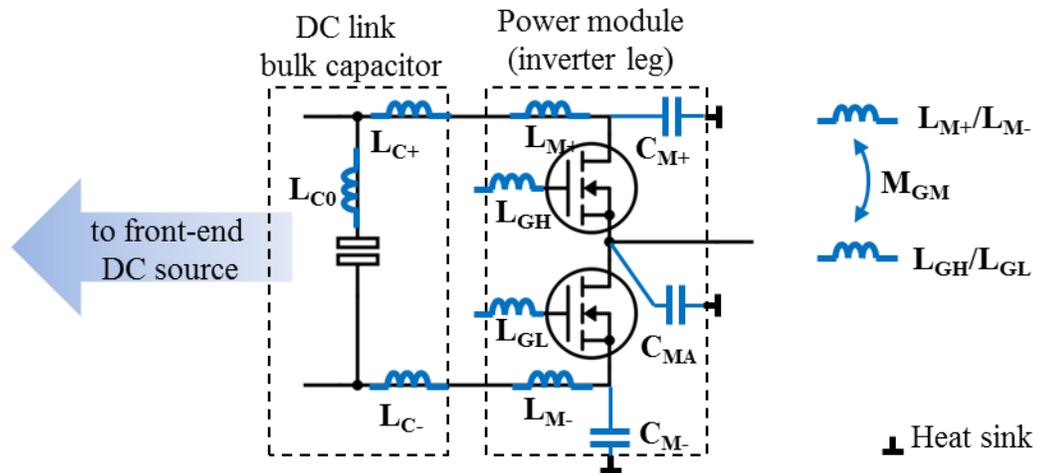


Fig. 2-2: Main parasitic elements in an inverter leg power module

- L_{C0} : The equivalent series inductance (ESL) of the DC link capacitor, due to the inductive current effect in the capacitor; it acts like a trans-impedance if the capacitor is treated as a 2-port network.
- L_{C+} , L_{C-} : The partial inductances due to the pinouts/connectors of the capacitor.
- L_{M+} , L_{M-} : The partial inductances due to the layout/geometry of the power module and the interconnections of the DC terminals.
- L_{GH} , L_{GL} : The partial inductances of the gate terminals.
- M_{GM} : The mutual inductance between gate loop (L_{GH}/L_{GL}) and power loop (L_{M+}/L_{M-}) of the power module.
- C_{M+} , C_{M-} and C_{MA} : Parasitic capacitances between the DC/AC terminals and the grounded heatsink.

The above mentioned parasitic elements will 1) significantly influence the switching performances and 2) contribute to EMI noise's propagation paths. The fast switching of the emerging wide bandgap (WBG) power devices will further enhance these parasitic effects. Therefore, these parasitic elements should be carefully treated in order to fully benefit from WBG devices' advantages.

2.1.2 Design rule for WBG power module

2.1.2.1 *Influences of different parasitics*

In general a power module should be designed so that 1) the semiconductors switch safely as fast as possible (thus reduce the switching loss) and 2) the EMI emissions decrease as much as possible in both conducted and radiated modes. The influences of the parasitic elements mentioned in 2.1.1 to switching and EMI will be discussed below:

1) *Switching*

The sum of L_{C0} , L_{C+} , L_{C-} , L_{M+} and L_{M-} forms the power loop inductance which creates the switching oscillation and the voltage overshoot between the drain and the source of the power semiconductors. This voltage overshoot will certainly increase the switching loss and might overstress the power chip. As a rule of thumb, the voltage overshoot can be estimated as $L \cdot di/dt$ where L is the sum of the above mentioned parasitic inductances and the di/dt is the switching current slew rate. The di/dt is 4~8 A/ns for a typical IGBT and it can reach 50~100A/ns for a SiC or GaN device.

The L_{GH} and L_{GL} do not influence the switching speed [Wang 13]. However, they do increase the possibility of the unintentional turn-on since the current injected by $C_{GD} \cdot dV/dt$ goes through C_{GS} mostly rather than L_G and thus creates a voltage bias on C_{GS} probably superior than the threshold voltage; this will increase the switching loss and even result in a shoot through [Zhang 14].

Even though Kelvin connection configuration assures the least common source inductance between the gate loop and the power loop, the mutual inductance between the two loops M_{GM} serves as a non-welcome one just like the former one [Merienne 96].

Whatever parasitic capacitances in parallel with the three intrinsic capacitances (C_{GS} , C_{GD} and C_{DS}) will have a negative effect on fast switching, especially in WBG case. For some GaN device, the values of their intrinsic capacitances (from ~pF to ~50pF) are in or under the range of the parasitic capacitances due to a typical module layout (~50pF to ~100pF).

Therefore, all these parasitic elements should be minimized to ensure fast and clean switching.

2) Electromagnetic interferences (EMI)

The sum of L_{C0} , L_{C+} , L_{C-} , L_{M+} and L_{M-} associated with the C_{OSS} capacitance of the semiconductor device result in the switching oscillation and thus creates a resonance peak at the oscillation frequency at the differential mode (DM) EMI noise source (the switching current) [Costa 92]. Therefore this oscillation should be damped which means all the above mentioned parasitic inductances should be minimized.

L_{C0} influences directly the filter effect of the DC link capacitor as it determines the insertion voltage gain (ratio of voltage at load without filter and the one at load with filter) of the DC link capacitor as a DM EMI noise filter.

C_{MA} , the mid-point capacitance, determines directly the flat part level of the common mode (CM) conducted EMI emission in frequency range from 150kHz to ~MHz. It should be in priority minimized. C_{M+} and C_{M-} recycle the CM EMI noise as a CM filter. Therefore their values are preferred to be maximized.

In addition, mode transformation (from CM to DM or vice versa) happens when the DC sides' impedances are not balanced, which means either $C_{M+} \neq C_{M-}$ or $L_{M+}+L_{C+} \neq L_{M-}+L_{C-}$. This transfer phenomenon should be avoided since the filter design is based on DM and CM decoupling.

2.1.2.2 Design recommendations

Tab. 2-1 shows a resume of the design recommendations for different parasitic elements of power module based on WBG semiconductors to ensure both fast (thus low switching loss), clean switching and low EMI.

Tab. 2-1: WBG power module parasitics' design recommendation

	$L_{C0}/L_{C+}/L_{C-}/L_{M+}/L_{M-}$ ^[1]	$L_{GH}/L_{GL}/M_{GM}$	C_{M+}/C_{M-} ^[2]	C_{MA}	C_P ^[3]
EMI	↓	--	↑	↓	--
Switching	↓	↓	--	--	↓

^[1] $L_{M+}+L_{C+}$ should equal $L_{M-}+L_{C-}$ ^[2] C_{M+} should equal C_{M-}

^[3] C_P represents any parasitic capacitance in parallel with C_{GS} , C_{GD} or C_{DS}

2.1.3 State-of-the-art low inductive WBG power module

Since 2012 the industries have been competing in the race towards low-inductive power modules aiming for fast and clean switching [Wolfgang 14]. The following section will discuss the state-of-the-art design of the low inductive power module with respect to different parasitic elements mentioned in previous sections as in Fig. 2-2.

A. Module layout inductances – L_{M+} and L_{M-}

In general, thanks to the improvement of the interconnection technique between semiconductors and the power terminals' design, the power loop parasitic inductances in WBG power modules are significantly reduced ($<10\text{nH}$) comparing to traditional IGBT power modules ($>30\text{nH}$). The WBG module design depends primarily on the semiconductor dies' structure, which is vertical or lateral according to the current flow direction.

The vertical semiconductors, dominantly such as SiC MOSFET, are perfect candidates for double-side cool module design. Fig. 2-3 shows the two ways to realize double-side cooling power module and their references. Even though this design emphasizes on thermal improvement, the power loop inductance has been reduced as well thanks to the size reduction of the module. Furthermore, these double-side heatsink designs serve as shielding of the radiated EMI noise.

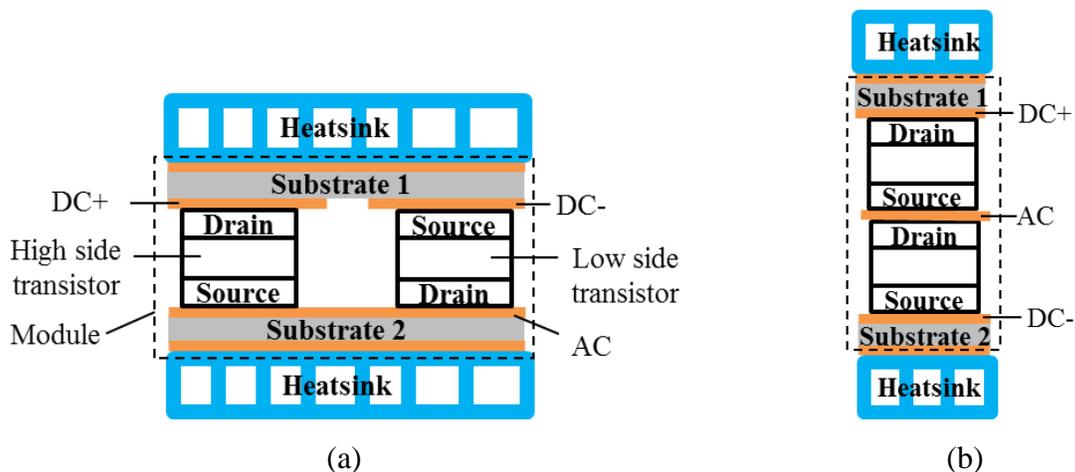


Fig. 2-3: Double side cooling power module designs for vertical semiconductor device (a) [Ramelow 08] [Ishino 14] [Liang 14]; (b) [Vagnon 10] [Regnat 16]

The lateral semiconductors, dominantly such as GaN HEMT, stand for different module design approaches. First of all, GaN HEMT's lateral structure has given a unique advantage to monolithically integrate high-side and low-side transistors on the same semiconductor die substrate. Therefore, the reduction of the size of power loop results in the decreasing of the power loop inductance. **Fig. 2-4** shows a monolithic inverter leg by EPC. In fact, even a monolithic three phase inverter has been demonstrated [Uemoto 09].

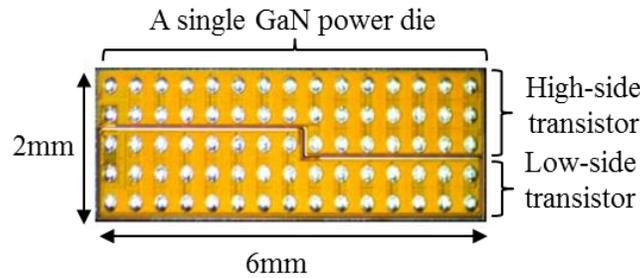


Fig. 2-4: A monolithic inverter leg from EPC (100V 23A)

The busbar structure is widely considered to terminal-out the DC connections in order to reduce loop inductance. A busbar structure is formed by two copper foils and an insulation layer between them as shown in **Fig. 2-5**. The loop inductance of a busbar structure is estimated as in **Eq 2-1**. Wide, short copper and thin insulation layer (respecting the industrial clearance requirement) are desirable for low inductive design.

$$L = \mu_r \cdot \mu_0 \cdot \frac{H \cdot L}{W} \quad \text{Eq 2-1}$$

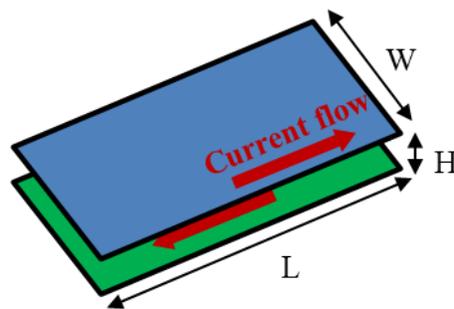


Fig. 2-5: Busbar structure inductive loop

The lowest inductive busbar-like solution is the flexible two-layer PCB of SKiN technology of SEMIKRON [Beckedahl 16], which could result in less than 4nH power loop inductance (c.f. discussion on L_{C+} , L_{C-} and L_{C0}).

The conventional module design has only active power devices inside the module. This allows the users to adapt the DC link capacitors to module for different applications. However, the use of low profile surface mounted (SMD) multilayer ceramic capacitors (MLCC) directly inside the module becomes a more and more common way to nearly eliminate the effects of L_{M+}/L_{M-} . There are two ways to put MLCC capacitors as close as possible to the power GaN devices to form a vertical power loop (Fig. 2-6a) or a horizontal one (Fig. 2-6b). The former creates a busbar structure above the two GaN chips and put the MLCC on; the latter leave the power devices and the MLCC on the same side of the module substrate to form a minimum power surface. The vertical loop concept is widely used in [Luo 14] [Reusch 14] and [Klein 16]. The horizontal loop concept [Thollin 16] is more suitable to traditional module design since it uses only one substrate layer.

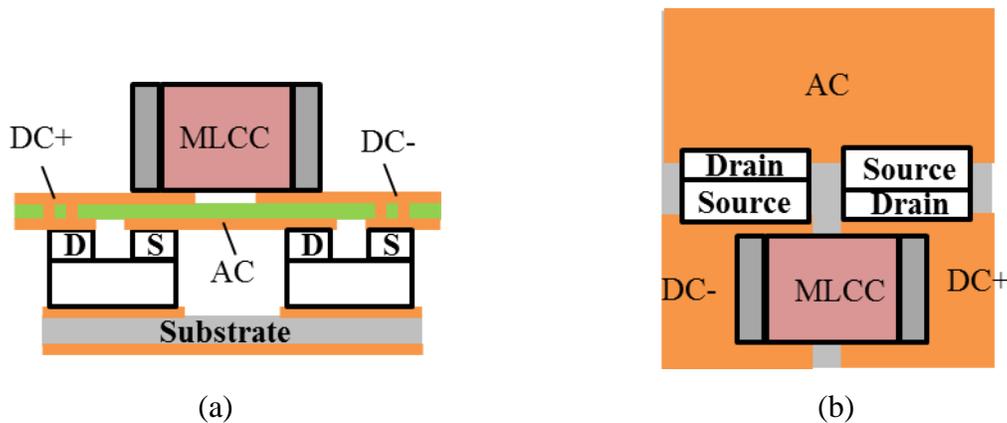


Fig. 2-6: The vertical loop (b) and the horizontal loop (a) between the GaN devices and the MLCC.

Despite of the advantages mentioned above, the probable failure under thermal and vibration stress [Taylor] is the main reason that MLCC capacitors are not widely used in industrial designs.

B. DC link capacitor's parasitic inductances – L_{C+} , L_{C-} and L_{C0}

The parasitic inductances due to the DC link capacitor might be dominant in the total power loop inductance. Not only the capacitor itself but also the connections between the capacitor and the power module contribute significantly to the inductive effect.

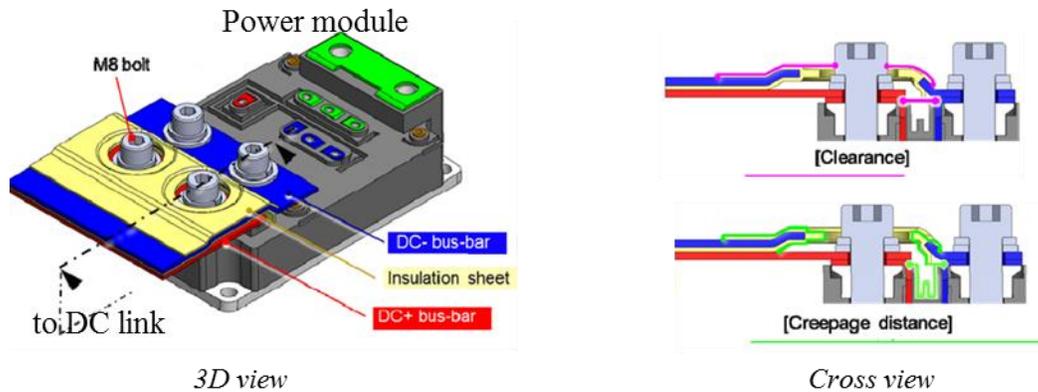
A low ESL capacitor is pursued for the DC link. ESL is mainly due to the geometry of the capacitor. The volume and the distance between the pinouts of the capacitor are essential to the contribution of parasitic inductance. In general, ceramic material, compared to polypropylene, can reduce the capacitor's volume at the same value. In addition, some inductive compensation structure can further reduce the ESL. **Fig. 2-7** shows a commercial 500V 30 μ F ceramic DC link capacitor [**Epcos 17**] and its internal design for ESL compensation. It is claimed with an ESL as low as 3nH and a volume of 20mm \times 30mm \times 15mm. This can be compared with a polypropylene film DC link capacitor from Panasonic [**Panasonic 10**], which has 10nH of ESL and a volume of 40mm \times 30mm \times 50mm. It should be noted that this inductive compensation structure has MLCC version – X2Y capacitors [**X2Y**] which are widely used in decoupling capacitors in power delivery distributions. When numbers of capacitors are used, some compensation method, such as inverting the paralleled inductive field polarities, could be used to further reduce the parasitic inductance [**Cree 15**].



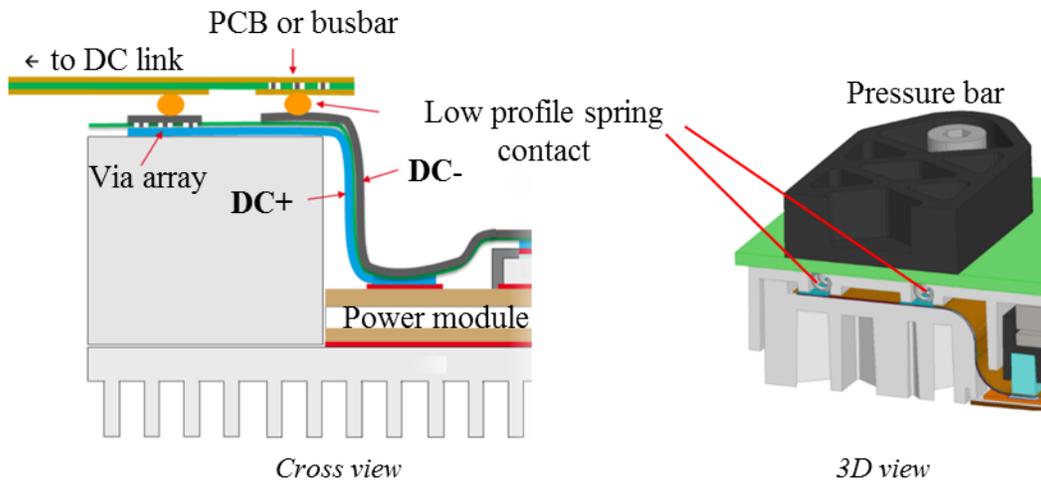
Fig. 2-7: A ceramic DC link capacitor rated 500V30 μ F (a) and the ESL inductive compensation principle (b)

In addition, the interconnection between the power module and the DC link capacitor should keep in low inductive profile. Supposing the power terminals of the module are in busbar structure, traditional design would be two side-by-side through holes respectively in upper and lower copper foils for screwing (**Fig. 2-8a**), which requires large openings or additional isolation

sleeves to extend the creepage length between the upper and the lower sides. This increases the power loop area, especially for high voltage applications when the isolation distance becomes higher. A better solution is to design both the power module terminals and the capacitor-supporting PCB board as bus-bar structure; then connecting the two by paralleled low profile spring connectors, as shown in **Fig. 2-8b**.



(a) by screws [Saito 16]



(b) by spring contact [Beckedahl 16]

Fig. 2-8: Power modules' interconnection solutions

C. Gate parasitic inductances – L_{GH} , L_{GL} , M_{GM}

In a “system-on-chip” point of view, as in power part, the most effective way to reduce gate loop parasitic inductance is to monolithically integrate a push-pull stage just beside the power chip on the same substrate [Moench 15] [Roberts 14], as shown in Fig. 2-9a; In a “system-in-package” point of view, discrete gate driver IC chip could be placed as close as possible to the power chip inside the module and be connected to the power chip by means of bond wire for example [Moench 16], as shown in Fig. 2-9b. An alternative way is to put the driver just outside the optimized (size minimized) module’s housing to reduce the distance between the driver and the power chip [Klein 16].

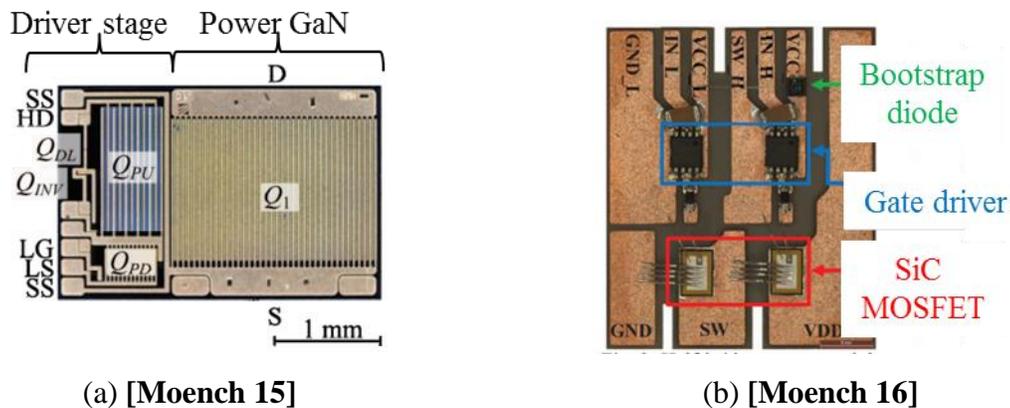


Fig. 2-9: Examples of monolithic integrated gate driver (a) and in-module driver (b)

In order to minimize the mutual inductive effect between the power loop and the gate loop: 1) in some traditional power module design, the gate pinouts and the power ones are configured in different sides of the module package in order to keep the two loops far away from each other [Ishino 14]; 2) in some recent integrated design, the gate loops are configured purposely perpendicular with the power loop to minimize the mutual inductance between the two [Luo 14].

D. Module stray capacitances – C_{M+} , C_{M-} and C_{MA}

Since the capacitances between the DC sides and the GND are quite beneficial, in addition to the parasitic capacitances, using discrete MLCC directly inside the power module is an efficient way. Fig. 2-10 shows a power module using two discrete MLCCs as common mode filter capacitor to attenuate the high-frequency CM EMI noise.

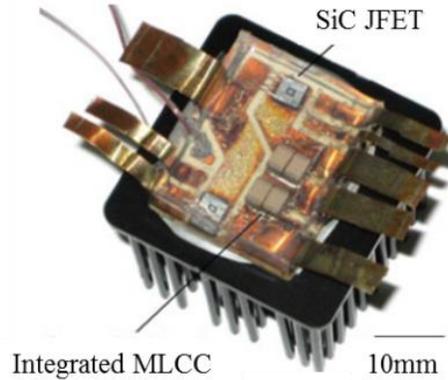


Fig. 2-10: A SiC power module with integrated MLCC as CM filter [Robutel 14]

2.2 GaN power module design

Since there is no GaN based power module available until the beginning of the experimental work, a GaN power module, which is lab-made, suitable for switching and EMI studies and comparable to the power module designs in the MEGAN project, will be designed and manufactured. A review of the two GaN power module design in MEGAN project is presented before the one in SATIE.

2.2.1 Power module designs in the MEGAN project

2.2.1.1 *Gen3 power module*

The “Gen3” power module [Thollin 16] in the MEGAN project, designed for aircraft applications, involves one 600V GaN HEMT based inverter leg (Fig. 2-11a). This module uses two ceramic substrate (Si_3N_4) layers of different thickness (640 μm and 320 μm) as a basic structure. The two GaN HEMT dies designed and manufactured by CEA-LETI are embedded in the cavity of the top ceramic layer (Fig. 2-11b) so that the surface of the GaN chips are in the same level of the top ceramic layer’s copper. Lead frame is used to connect the GaN chips and the top copper in order to avoid inductive wire bonding. This structure has advantages in thermal and mechanical aspects compared to a one layer module [Thollin 16].

In addition, the electrical advantages, mainly in EMI reduction and fast switching enabling, are concluded as below:

- Integrated C_X (differential mode filter) and C_Y (common mode filter) capacitors result in both switching voltage overshoot reduction and high-frequency EMI filtering.
- Busbar structure is applied between the DC+ (red) on upper layer and DC- (blue) on lower layer, even though the through-hole design seems less efficient compared to the spring connector mentioned in **Fig. 2-8**.

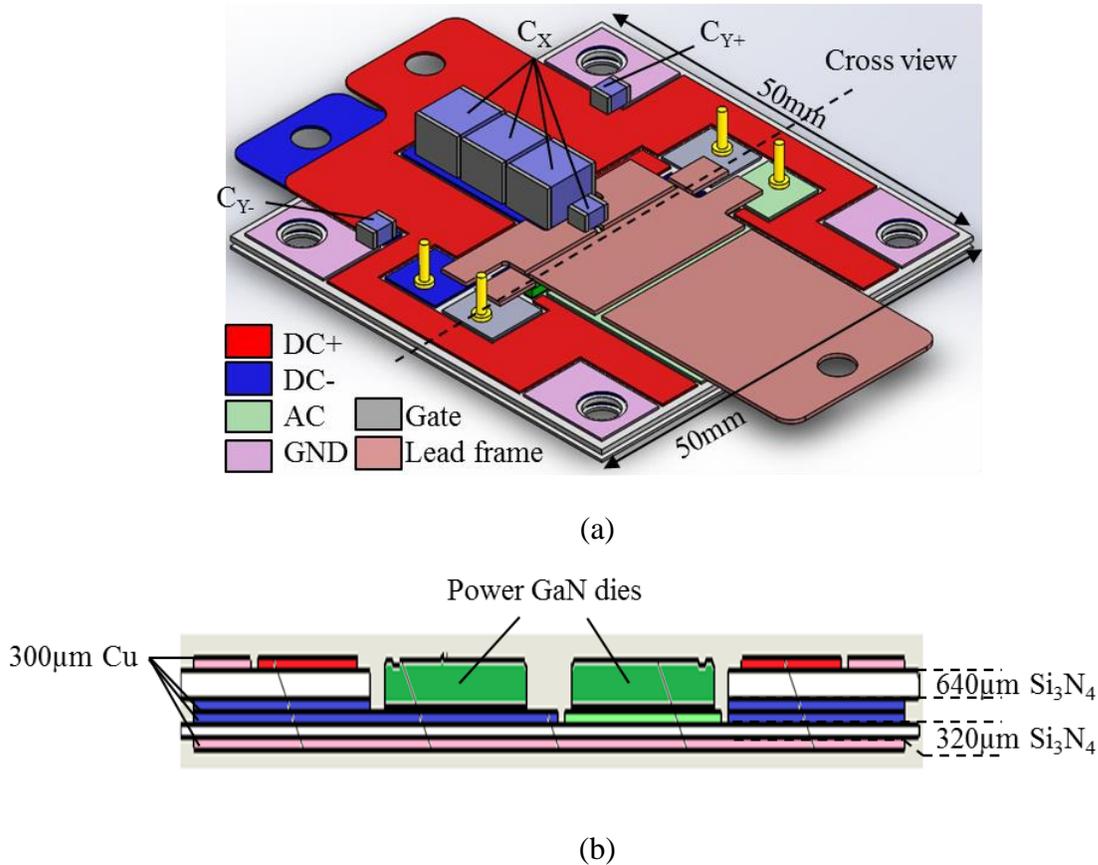


Fig. 2-11: 3D drawing (a) and cross view (b) of Gen 3 power module

It should be noted that this module design results in parasitic capacitances between the different potentials. **Fig. 2-12** shows the main capacitances whose values are calculated from Q3D modeling. They influence the electrical performance of the module in different ways:

- C_{MD} : 122pF, contributed to the DC link capacitance, thus good one.
- C_{MA} : 13pF, as discussed previously it should be as small as possible.

- C_{MOSSL} : 56pF, in parallel with the capacitance C_{DS} of the low-side transistor; comparable to the capacitance C_{DS} of some GaN HEMT (e.g. $C_{DS_GS66508@400V}=65pF$); it increases the C_{OSS} related switching loss (which can be quantified by $1/2 \cdot C_{OSS} \cdot V_{DS}^2$).
- C_{M-} : 480pF, it creates a huge imbalance referring to GND since there is no C_{M+} , resulting in EMI mode transformation without using ceramic capacitors as C_Y ; However, using large value of capacitor C_Y such as 10nF will solve this imbalance problem (reduce imbalance rate to 5%).

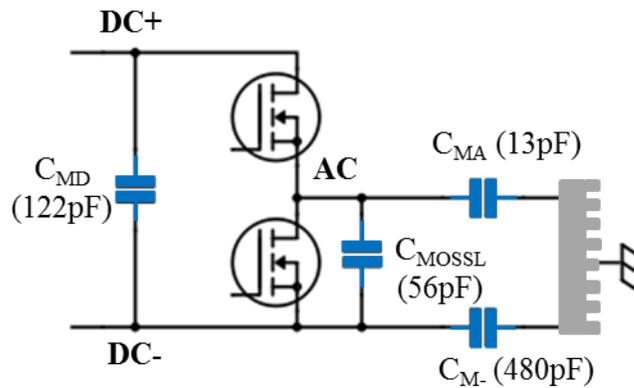


Fig. 2-12: Main parasitic capacitances in Gen3 module

It is also noted that the two C_Y capacitors are placed relatively far from the transistors compared with the C_X capacitors. The loop between the two transistors, C_{Y+} , C_{Y-} and the backside (GND) results in a parasitic inductance. Its value is calculated by Q3D modeling as 6nH and could be distributed equally as 3nH to the two DC sides as shown in Fig. 2-13.

As in traditional power module configuration, the gate driver board will be installed right above the module as shown in Fig. 2-14. The gate pillars could be replaced by spring loaded connectors for test debugging. The gate driver ICs will be placed on the board as near as possible to the pinouts to reduce the gate loop.

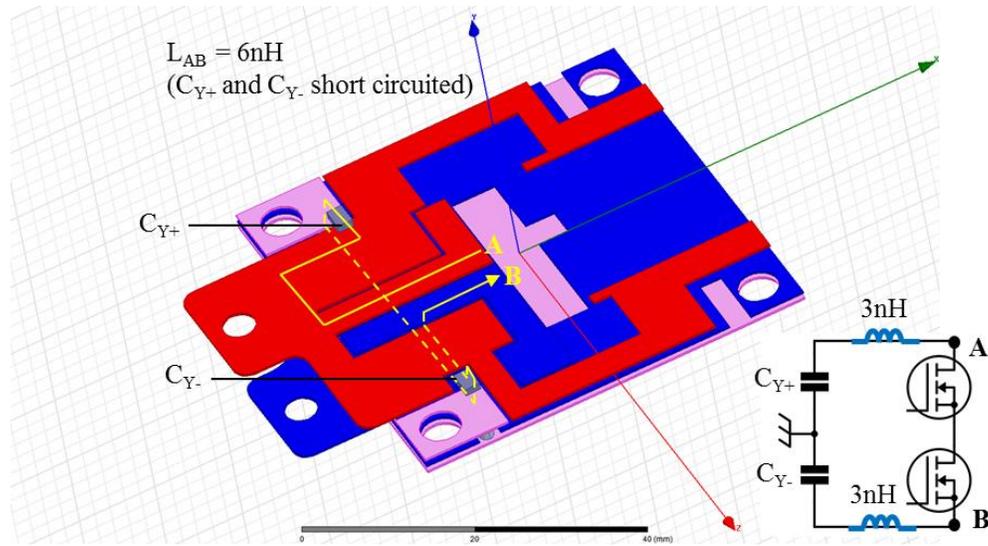


Fig. 2-13: Parasitic inductance in C_Y filtering loop in Gen3 module

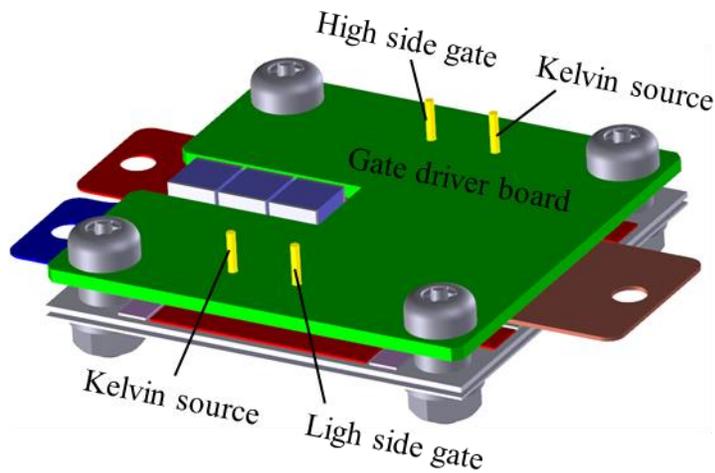


Fig. 2-14: Gate driver board configuration of Gen3 module

2.2.1.2 Gen2+ power module

An alternative design “Gen2+” which is less complicated is shown in **Fig. 2-15**. This module involves using 600V/60A GaN HEMT (GS66516T) from GaN Systems and similar design as shown in **Fig. 2-6b**. One layer ceramic substrate is used. The interconnection between the GaN devices and the top copper of the ceramic substrate is realized by lead frames as in Gen3 module. The gate driver board configuration is the same as in the previous one. In this

module, only C_X capacitors are used. The parasitic capacitances between the DC sides and GND (C_{M+} and C_{M-}) are relatively balanced, thus no EMI mode transformation will occur.

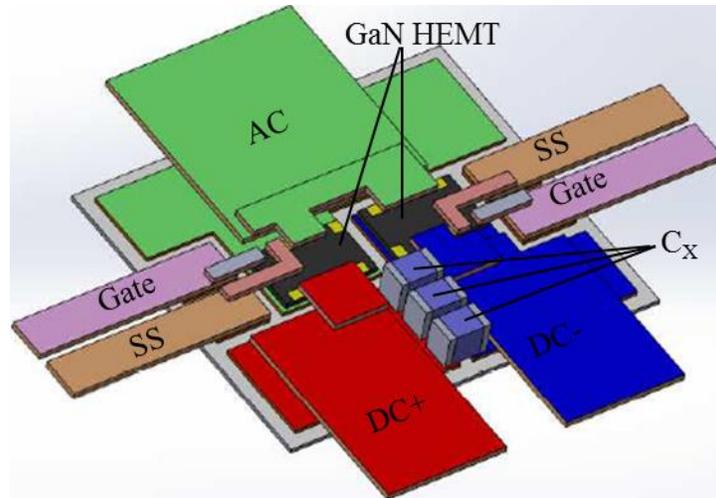


Fig. 2-15: 3D drawing of Gen2+ power module

2.2.2 SATIE power module design

2.2.2.1 *Power module design*

In this dissertation it is intended to investigate in the methodology of EMI study in GaN based power module (Gen3 or Gen2+ liked), therefore:

- The prototype module should have similar size and layout as the modules of the MEGAN project so that it has similar parasitics;
- It should use simple and low-cost technology to manufacture in order to test and debug repeatedly;
- It should use existing commercial GaN HEMTs.

Based on the previous precautions, the proposed power module uses two-layer PCB and 600V/30A GaN HEMT from GaN Systems (GS66508P), as shown in **Fig. 2-16**.

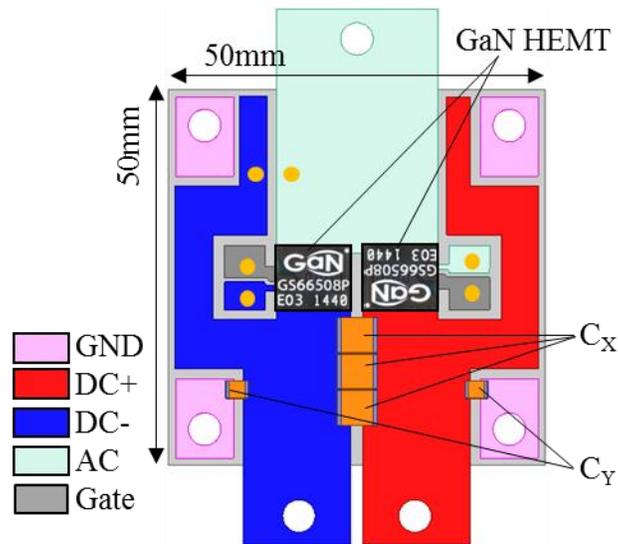


Fig. 2-16: Top view of the SATIE power module

The GS66508P's package has been discussed in 1.1.2.5 and it makes the GaN chips connected to the top surface of the module by planar lead frame. The 50mm×50mm PCB has the same size as the Gen3 and Gen2+ power module. The top copper of the PCB serves as DC, AC and gate terminals; the layout and the locations of the GaN chips and MLCCs are quite similar as those of the Gen3 module. The bottom copper of the PCB serves as the backside of any other power module to be attached to grounded heatsink. The insulation epoxy layer of the PCB has 0.8mm of thickness, which is similar to the first layer of the Gen3 module so that they have similar values ($\times 10\text{pF}$) of parasitic capacitances. All through-holes are for 4mm screws. The orange color points in **Fig. 2-16** are the contact points to the gate driver board – including the gate and kelvin source connections and the low-side GaN device's drain-source voltage monitoring (between AC and DC-).

This PCB module has limited power dissipation capability since the thick epoxy layer presents a very high thermal resistance. However, the module design can be scaled to a two-layer insulated metal substrate (IMS) with aluminum substrate to make a more thermally efficient power module.

The layout of the module results in some stray capacitances between the top layer elements and the bottom layer (GND). They are indicated in **Fig. 2-17**.

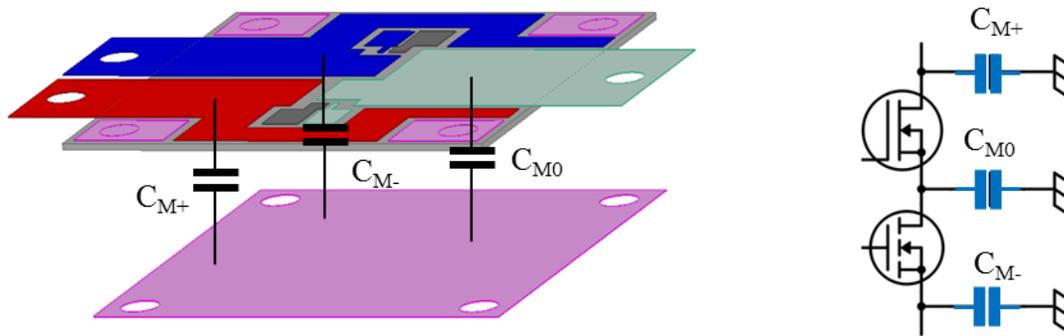


Fig. 2-17: Parasitic capacitances in SATIE module

A fabricated sample of SATIE module without soldering C_X or X_Y is shown in **Fig. 2-18**. All components can be soldered easily to the module. The module is fixed to a heatsink underneath the module by four 4mm screws.

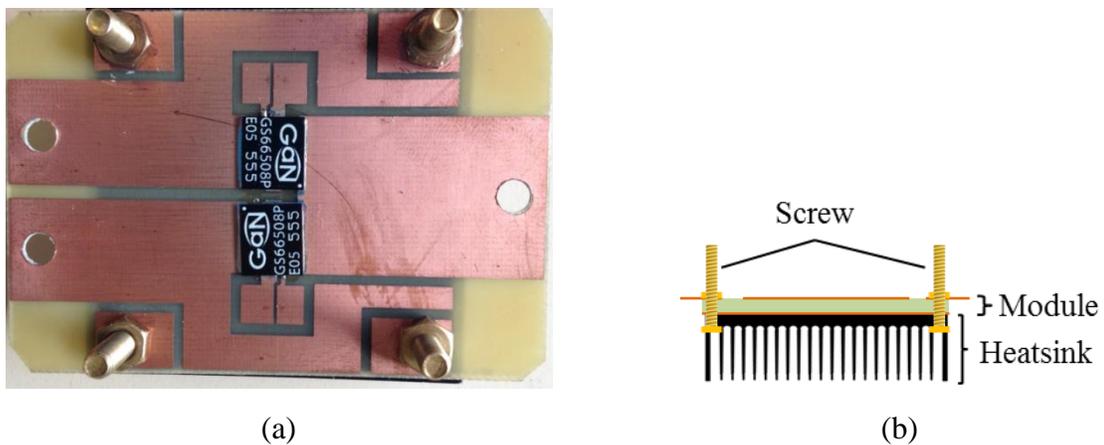


Fig. 2-18: Top view (a) and side view (b) of the fabricated SATIE module

2.2.2.2 Gate driver board design

Gate driver for cascode GaN device is similar as for the conventional Si MOSFETs since the input of the cascode device is a low-voltage MOSFET. Gate drivers for e-mode GaN devices have some specific requirements comparing to their Si counterparts. These requirements are due to the ultra-fast switching and the voltage rating of the gate terminal.

- The V_{TH} of an e-mode GaN device is typically 1~2V and since the negative driving voltage is not desirable (due to the increase of the reverse switching loss), it is recommended to turn off the GaN device at 0V. Of course, this makes the driving circuit less complex than a negative voltage driving capable one. For turning on, it is recommended gate driving voltage is 5~6V which is very close to its maximum rating (e.g. for EPC $V_{GS_on}=5V$ and $V_{GS_max}=6V$; for GaN Systems $V_{GS_on}=6V$ and $V_{GS_max}=10V$). This requires a gate drive design with minimum voltage overshoot to avoid gate rupture which is a well-known issue with e-mode GaN devices. Some gate driver integrated circuit (IC) dedicated to GaN device are available in the market, such as UCC27511 of TI and PE29100 of Peregrine Semiconductor; they have miniature packaging to reduce the gate loop inductance significantly and a voltage regulator integrated in the IC. A special driving case is for GaN device from Panasonic which requires -5V~3V (5V max) gate driving voltage. A specific passive circuit has been developed to supply a negative driving voltage instead of using a second power supply for the driver [**Umegami 14**] and this has been recently included in a commercial driver IC design [**Panasonic 16**].
- The isolation in both signal transfer and power delivery in the gate drive circuit is supposed to provide superior common-mode transient immunity (CMTI). Insufficient CMTI may cause spurious switching events when dV/dt exceeds its maximum rating and EMI problems. This CMTI relies on the parasitic capacitance between the primary and the secondary side of the isolation in the signal transfer and/or power delivery unit. The SI827x gate driver IC of Siliconlab has a state-of-the-art CMTI of 200kV/ μ s minimum thanks to their optoelectronic technology (0.5 pF isolation capacitance), compared with the conventional solution of 50~100kV/ μ s. The NXJ1series isolated DC-DC power supply from MURATA POWER has a 2pF input-output capacitance, which minimizes the common mode EMI problem. In a half bridge, an alternative way is to cascode the high-side power supply after the low-side one [**NGUYEN 17**].
- The Miller turn-on, also known as cross talk, is a phenomenon that in a half bridge one device is unintentionally turned on by the injection of the gate current due to dV/dt on Miller capacitance (C_{gd}) of this device when the complementary device is turned on [**Zhang 14**]. This phenomenon may result in a DC current shoot through or at least an

increased switching loss. The method to mitigate this cross-talk is to divert the injecting current due to $C_{GD} \cdot dV/dt$ rather from C_{gs} but to elsewhere such as an additional gate capacitor or a zero impedance turn-off path. The former method is easy to implant but it compromises the switching losses since it slows down the switching; the latter one is the basis that the state-of-the-art commercial gate driver IC dedicated to solve the cross talk problem – the turn-off path is separated from the turn-on. In addition, the gate loop inductance especially the turn-off loop one must be minimized to reduce the path impedance. Smallest possible turn-off external resistance is recommended.

- Since the drive IC is recommended to be placed as close as possible to the power device, the thermal issue occurs since the IC is close to a heat source. Therefore, in specific applications, the driver IC's thermal capacity will be a challenge.

In conclusion, the gate driver design for GaN HEMT must satisfy the specific requirement such as voltage ratings and CMTI; in addition, placing the driver as close as possible to the GaN device and careful use of external gate resistances are crucial.

In the dissertation's case, for driving GS66508P GaN HEMT, the gate voltage is set between 0V and 5V. The commercial DC-DC power blocks and gate driver ICs are used. The circuit of the gate drive board is presented in **Fig. 2-19** and the layout/3D drawing are shown in **Fig. 2-20**.

The blocks Dr1 and Dr2 are two isolated gate driver ICs; the blocks P1 and P2 are and two isolated DC-DC converters powering these drivers – which means the isolation appears both between high-side and low-side and between the signal input and the driver output. Therefore, three “ground” potentials present on the board (**Fig. 2-20b**): 1) GND_S as the signal ground and also for the input of both DC-DC converter blocks; 2) GND_H as the ground of the high-side driver which will be connected to the kelvin source of the corresponding GaN HEMT SS_H ; 3) GND_L as the ground of the low-side driver which will be connected to the kelvin source of corresponding GaN HEMT SS_L .

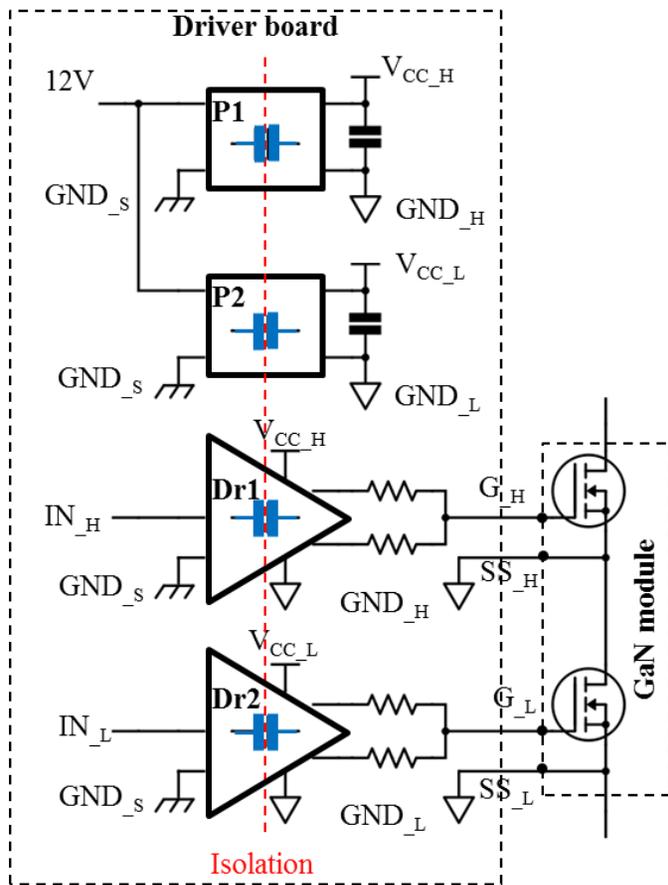


Fig. 2-19: Circuit of the gate drive board for SATIE module

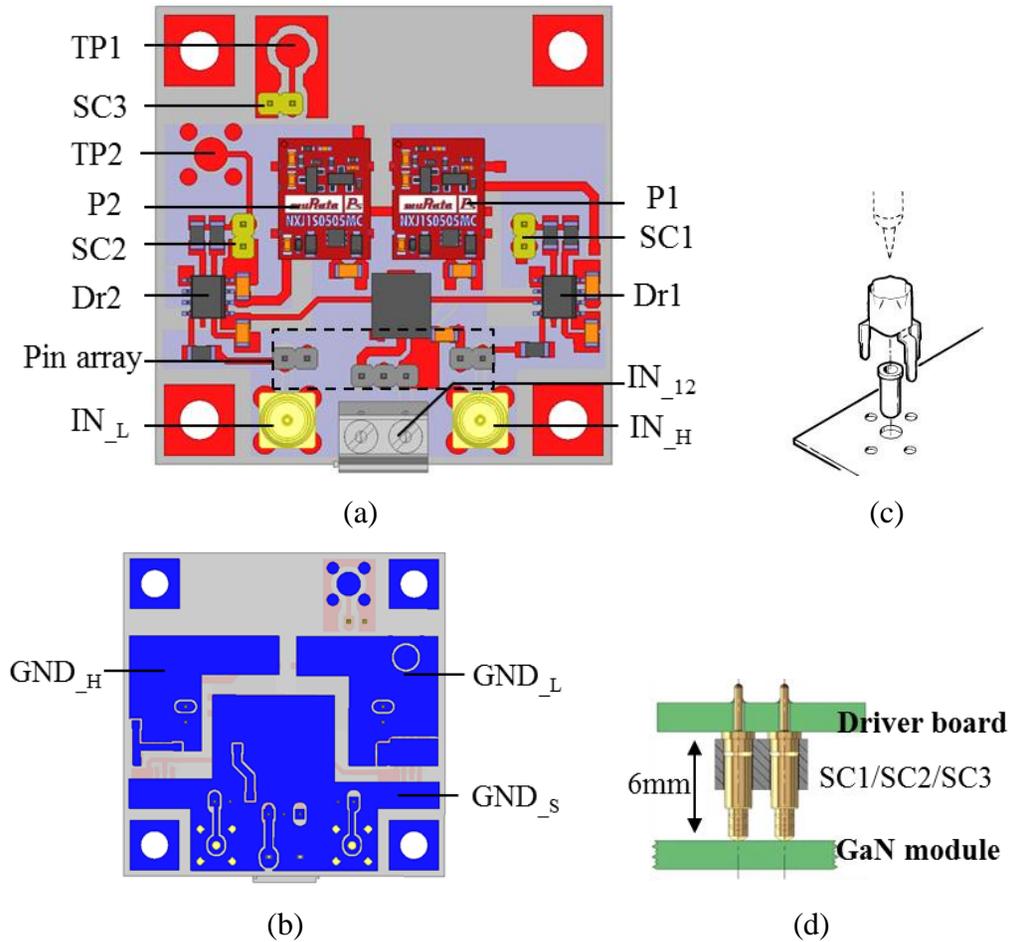


Fig. 2-20: Top (a) and bottom view (b) of the drive board ; the probe-tip adapter (c) and the spring loaded connector (d)

The driver IC, SI8271 from Silicon Lab, provides separated output for turn-on and turn-off, with 2.7Ω of R_{OH} and 1.0Ω of R_{OL} resulting in peak output current 1.8A of I_{OH} and 4.0A of I_{OL} . Approximately 40ns of propagation delay and 10ns of rise/fall time make this IC has a speed fast enough. It also has a 0.5pF isolation capacitance between input and output thanks to their semiconductor based isolation technologies; which allows a common mode transient immunity (CMTI) as high as 400kV/ μ s. All decoupling capacitors are placed as close as possible to the input sides of these ICs.

The isolated 1W DC-DC converter, NXJ1S1205 from MURATA POWER, provides directly 5V from 12V to the gate driver IC to turn on the power device. Its isolation capacitance is typically 2.5pF. It should be noted that the isolation capacitances of both gate drivers IC and the converter block are essential to reduce the common mode current flowing from the power module to the driver board.

The gate driver board will be fixed right above the power module by four screws. The G_{HL} and SS_{HL} pads on the power module are connected to the driver board via SC1 and SC2 – 2.54mm spring loaded connectors from Preci-dip (**Fig. 2-20d**) which has $10m\Omega$ of static contact resistance. Another connector SC3 is used to monitor the drain source voltage of the low-side GaN HEMT (V_{DS_L}). The distance between the driver board and the power module is at minimum 6mm, according to the size of the spring connector.

TP1 and TP2 are passive voltage probe tip adapters (**Fig. 2-20c**), respectively for the measurement of V_{DS_L} and V_{GS_L} . IN_L/IN_H are two SMB connectors for signal input of high/low-side gate driver IC and IN_{12} is a Phoenix connector providing 12V input of the two DC-DC blocks. Three pin head arrays are placed in parallel with each of them which allows the probable connection to an auxiliary board above (such as dead-time generation etc).

A prototype gate driver board is fixed above the SATIE power module and its top and side views are shown in **Fig. 2-21**.

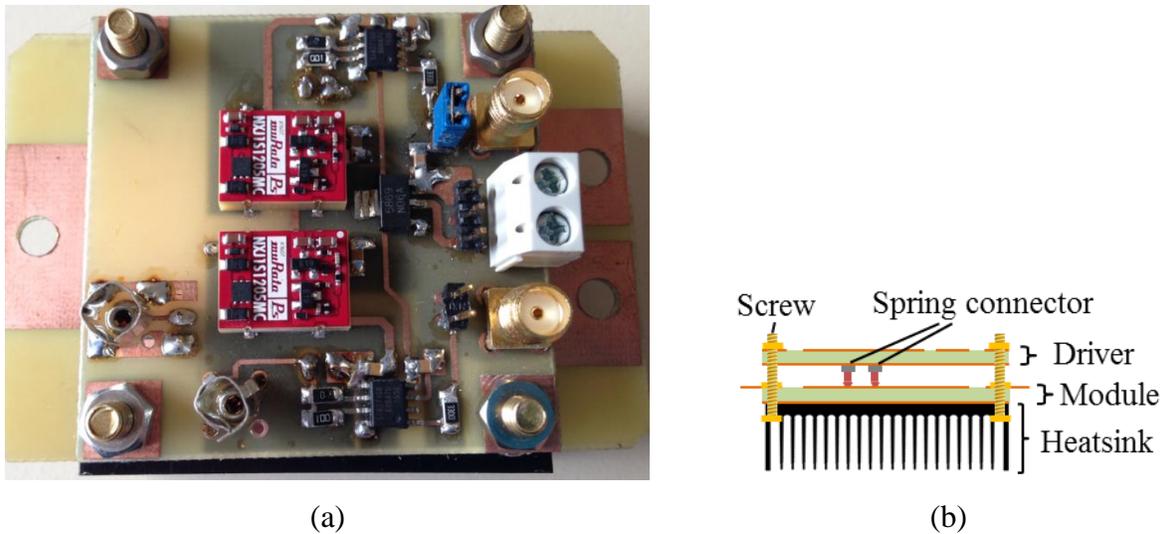


Fig. 2-21: Top view (a) and side view (b) of the gate driver board

2.3 SATIE module modeling

As discussed previously, the power module’s modeling is for the purpose of predicting the switching loss and EMI noises. A power module’s modeling includes not only the module itself but also the associated DC link capacitor and its gate driver circuit. The bare module (without in-module capacitor) system is illustrated as in **Fig. 2-22**.

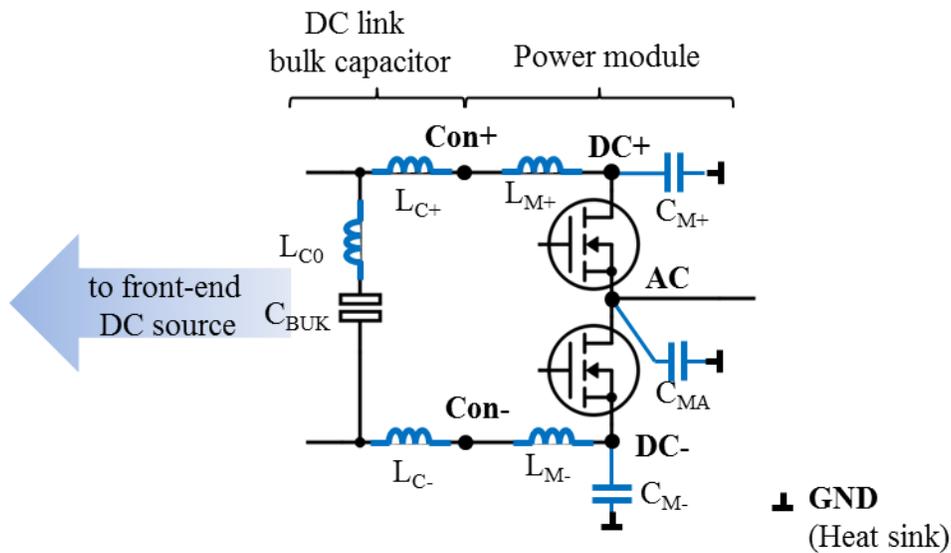


Fig. 2-22: Model illustration of a bare module (without in-module capacitors)

As discussed in 2.1.1, $L_{C0}/L_{C+}/L_{C-}$ are different parasitic inductances of a large value DC link capacitor (C_{BUK}). In this dissertation, one 4-pin metallized polypropylene film capacitor of $30\mu\text{F}/800\text{V}$ (EZPE80306MTA from Panasonic) has been used.

This capacitor's pinouts are quite often not compatible to the DC terminals of the power module. Therefore, a supporting PCB board is necessary to be the interface connecting the capacitor (C_{BUK}) and the power module (**Fig. 2-23**). Two M4 screws are used to connect the supporting PCB and the power module; this results in 4mm distance between the module and the supporting PCB. Therefore, L_{M+}/L_{M-} are in fact the partial parasitic inductances forming the power loop $\text{Con+} \rightarrow \text{DC+} \rightarrow \text{DC-} \rightarrow \text{Con-}$; their values are due to not only the power module but also the DC link capacitor's supporting PCB.

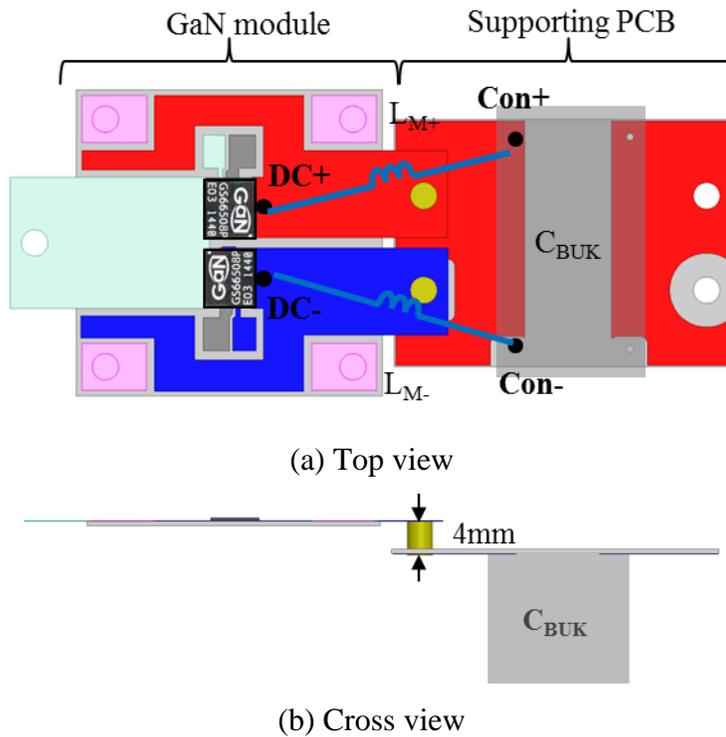


Fig. 2-23: Illustration of the $L_{M+}+L_{M-}$ loop

The parasitic capacitances of the power module $C_{MA}/C_{M+}/C_{M-}$ have been illustrated in **Fig. 2-17**. At last, the in-module ceramic capacitors' model will be integrated in the complete model, together with the gate drive's model.

2.3.1 DC link bulk capacitor (C_{BUK}) modeling

A 4-pin capacitor can be treated as a two-port network and its behavioral model is shown in **Fig. 2-24**. C_0 is the nominal value of the capacitor and Z_M is the equivalent series impedance. Z_M is essentially resistive and inductive due to the internal ESR and ESL of the capacitor. Z_L is mostly inductive due to the pinout connections. Z_M is essential for the voltage insertion gain of the filtering effect of this capacitor; Z_M+Z_L contribute to the total stray inductance of the power transfer path. Comparing with the L_{C+} , L_{C-} and L_{C0} from **Fig. 2-22**, L_{C0} inductive part of Z_M and L_{C+}/L_{C-} can be treated as half of the inductive value of Z_L respectively.

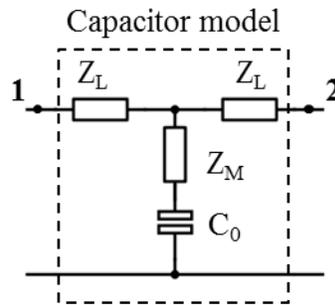


Fig. 2-24: Model of 4-pin DC link bulk capacitor

The Z_M and Z_L can only be found out by impedance measurement since it is too difficult to model a capacitor by numerical approach. The measurement equipment used in this dissertation is a vector network analyzer E5061B which enables the impedance measurement up to hundreds of MHz by different measurement ports (gain-phase or S-parameter). For DC link capacitor's modeling, the gain-phase ports will be used for impedance measurement up to 30MHz which is sufficient for the precision of the research in this dissertation.

2.3.1.1 Impedance measurement - Z_M

Z_M measurement is configured as in **Fig. 2-25**. The LF port provides a source voltage in relevant frequency range into terminal 1 of the capacitor. The current of this loop I_1 is measured by a wide band (up to 200MHz) transformer type current sensor (ref: CT2 from Tektronix) and this sensor is connected to Port R, terminated with 50Ω . Port T, terminated with $1M\Omega$, is connected to the terminal 2 of the capacitor to measure the voltage V_2 . Therefore T/R, equaling

V_2/I_1 while I_2 is nearly zero in relevant frequency range (since the T input impedance is $1M\Omega$), indicates the impedance of the sum of Z_M and C_0 . This method is able to eliminate the parasitic effect of Z_L and thus make the Z_M measurable.

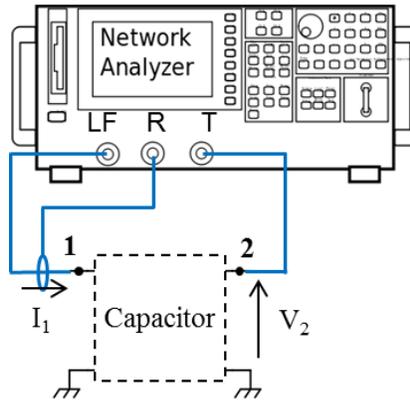


Fig. 2-25: Configuration of the Z_M measurement

At first a correction should be done. The terminal 1 and 2 are short-circuited and a 50Ω resistor is inserted between the terminals and GND. Therefore:

$$\frac{V_2}{I_1} = \frac{T}{R} = \frac{V_{LF} \frac{50}{50+50}}{V_{LF} \frac{1}{50+50}} = 50$$

However, the measured impedance is not perfectly 50Ω in magnitude and 0° in phase at the whole frequency range from 10kHz to 30MHz as shown in **Fig. 2-26a**. There are two distortions observed – one from 10kHz to 50kHz and the other from 1MHz to 30MHz. The former is due to the low bandwidth limit of the CT2 current sensor; the latter is due to the stray capacitive effect in the current sensor and the coaxial cable. In order to correct this error, “THRU” response calibration is done and this pulls the phase to 0° and the magnitude to 1 at the whole frequency range, as shown in **Fig. 2-26b**. With this correction, the future phase measurement can be trusted but the magnitude should be multiplied by 50.

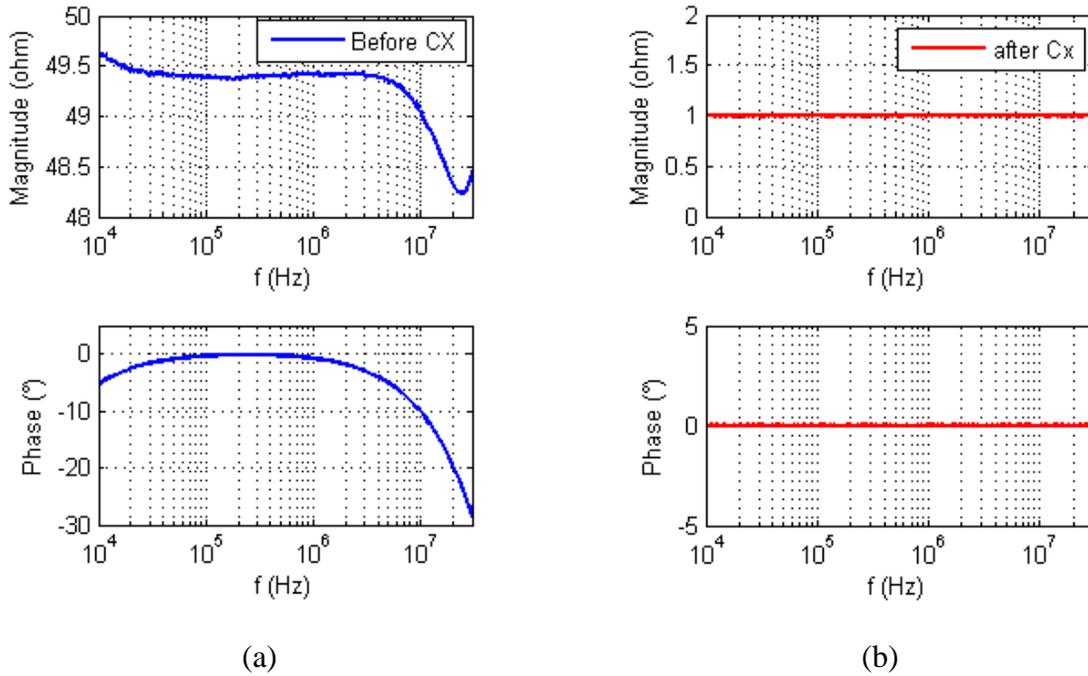
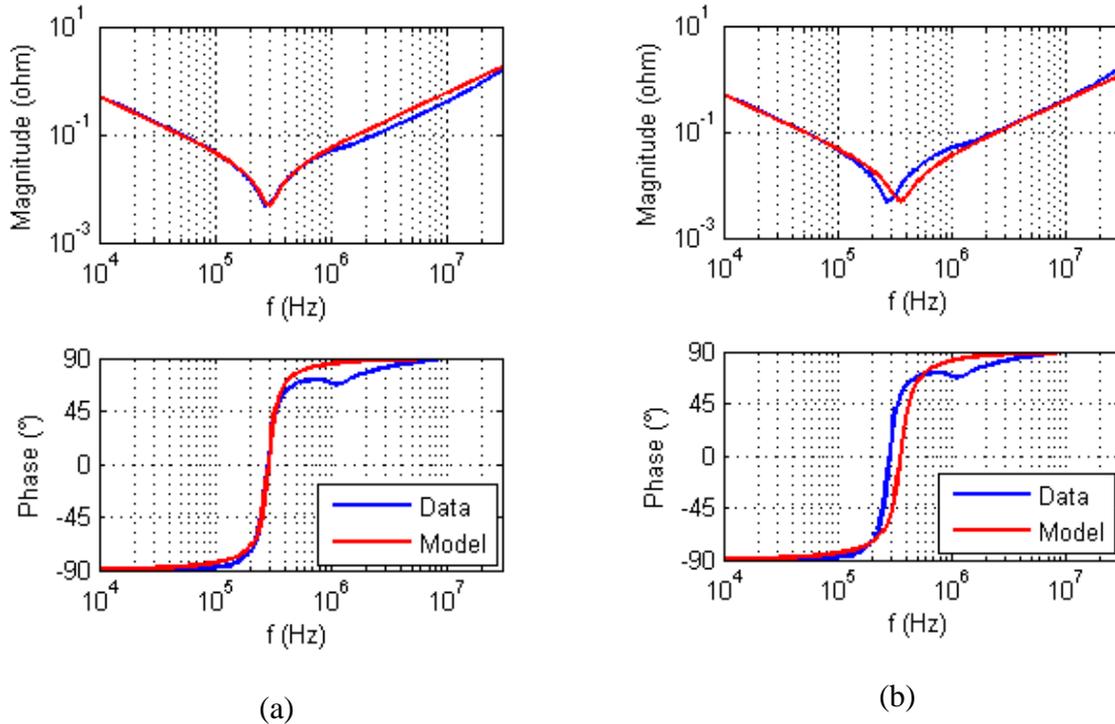


Fig. 2-26: Before (a) and after (b) the correction of the CT2's transfer function

The measurement result is shown with blue lines in **Fig. 2-27a**.



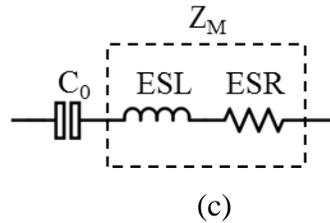


Fig. 2-27: Comparison between the measured impedance and its model (c) with different coefficients' values: $C_0=30\mu\text{F}$, $\text{ESL}=10.5\text{nH}$ (a); $C_0=30\mu\text{F}$, $\text{ESL}=6.5\text{nH}$ (b)

Firstly a basic model of Z_M – an ESR in series with an ESL (**Fig. 2-27c**) – is used. Comparisons between fitted model and measurement shows that a single ESL cannot model the impedance above the resonance frequency. In fact, the ESL value falls from 10nH to 6.5nH at around 400kHz~500kHz. This effect is due to current distribution inside the capacitor which modifies the ESL' value [**Seguin 97**]. This fall of this ESL's value can be modeled by dividing ESL with L_0 and L_1 as shown in **Fig. 2-28a**.

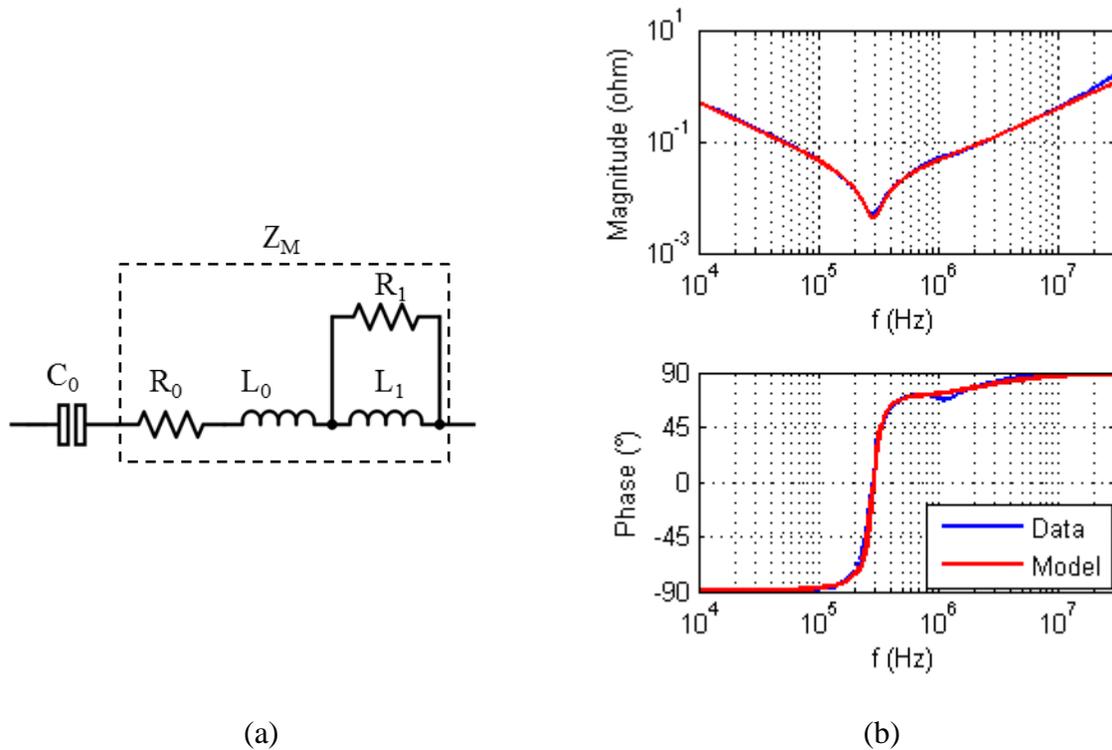


Fig. 2-28: Comparison between the measured impedance and its model (a) with coefficients as $C_0=30\mu\text{F}$, $R_0=2\text{m}\Omega$, $L_0=6.5\text{nH}$, $R_1=20\text{m}\Omega$, $L_1=4\text{nH}$ (b)

The sum of L_0 and L_1 represents ESL right after the resonance; L_0 represents the ESL at higher frequency. R_0 and R_1 represent the ESR of the capacitor. The final modeling results are shown in **Fig. 2-28b**.

2.3.1.2 Impedance measurement - Z_L

Since Z_M and C_0 are already known, Z_L can be deduced by the measurement of the sum of $Z_L+Z_M+C_0$. This impedance can be measured through a test fixture 16047E of the VNA on which the capacitor is inserted in the compensation interface (**Fig. 2-29b**). Impedance measurement method is set to “GP shunt” since it results a good precision for small impedance in relevant frequency range [p9, Keysight 17]. The cable configuration is shown in **Fig. 2-29a**. O/S/L calibration should be done at the end of the T adaptor. Then connecting this adaptor to the HIGH of the test fixture and short-circuit the LOW with the GND potential. At last, SHORT/OPEN compensation should be done at the contact interface of the test fixture to eliminate extra stray inductance in the dispositive (**Fig. 2-29b**).

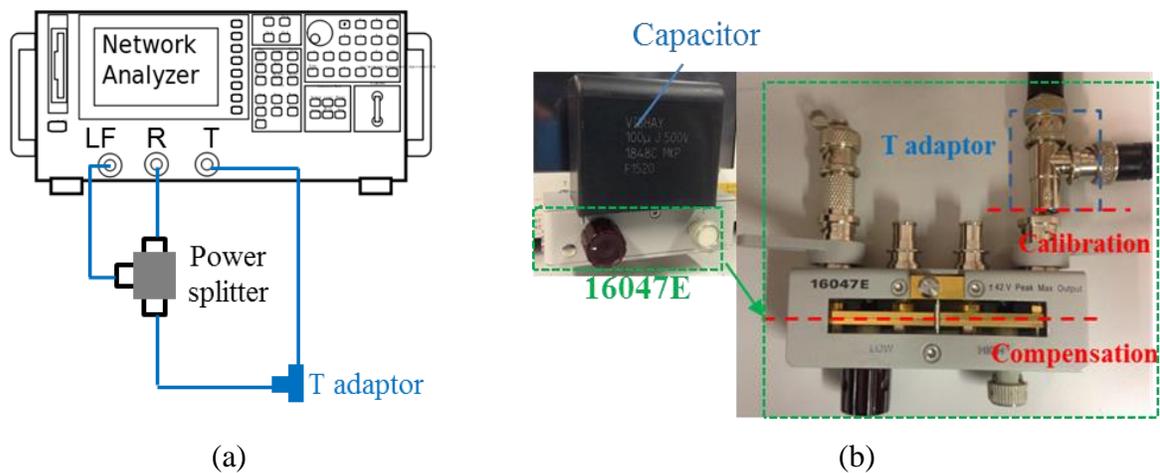


Fig. 2-29: Configuration of Z_L measurement (a) and the indication of the calibration and compensation plane (b)

The measured result is shown with blue lines in **Fig. 2-30a**. Z_L impedance is modeled simply as a series of an inductance L_2 and a resistance R_2 whose values are shown in **Fig. 2-30**. Therefore, $L_{C+} = L_{C-} = 1/2 \cdot L_2 = 15nH$.

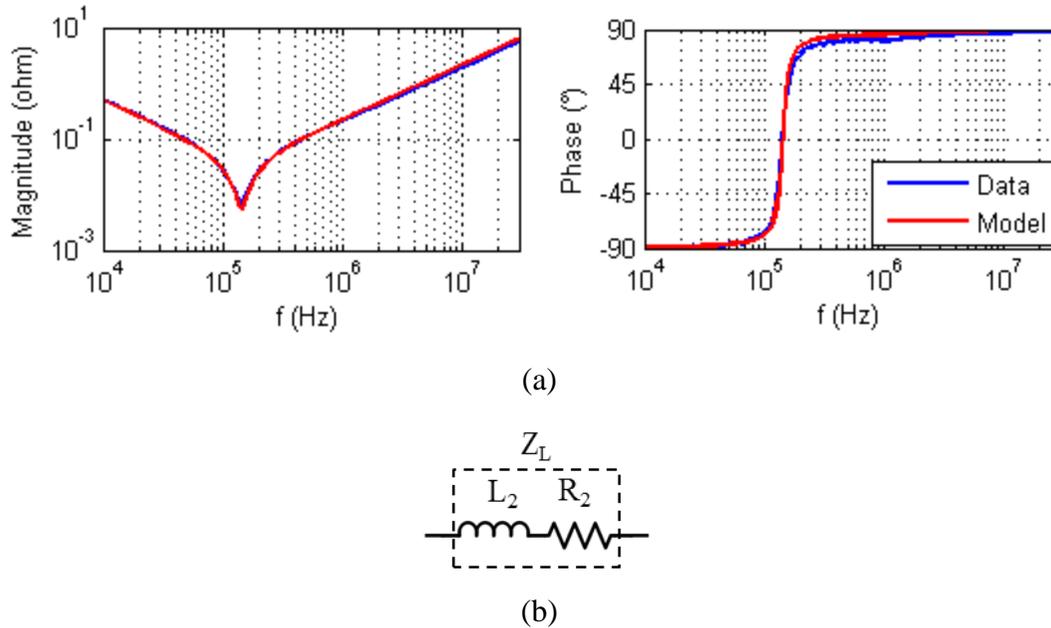


Fig. 2-30: Comparison (a) between the measured impedance $Z_L+Z_M+C_0$ and its model (b) with coefficients as $L_2=30\text{nH}$, $R_2=3\text{m}\Omega$

2.3.1.3 Final model of the DC link bulk capacitor

The final model of the DC link capacitor (EZPE80306MTA $30\mu\text{F}$) is shown in **Fig. 2-31**. The right side (Con+ and Con-) will be connected to the supporting PCB.

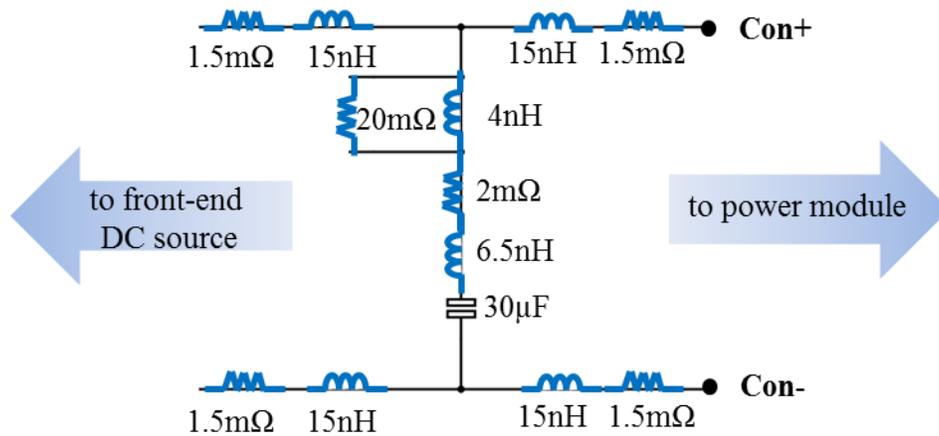


Fig. 2-31: Final model of the DC link bulk capacitor

2.3.2 Bare module modeling

In order to complete the modeling process, a bare SATIE module, with neither in-module MLCC capacitors nor semiconductor devices, is modeled as the circuit in **Fig. 2-32**. C_{M+} , C_{M-} and C_{MA} as main parasitic capacitances and L_{M+} , L_{M-} as power loop parasitic inductances.

The parasitic elements can be either calculated by a numerical approach such as Q3D (c. f. 2.3.2.1-A) or be measured directly by an impedance analyzer with proper protocol. It should be noted that both methods lead to some error. However, eventual results-matching between the two methods make a tendency to a good estimation. Last but not the least, their values will finally be evaluated by comparison between circuit simulation and measurement in real test bench.

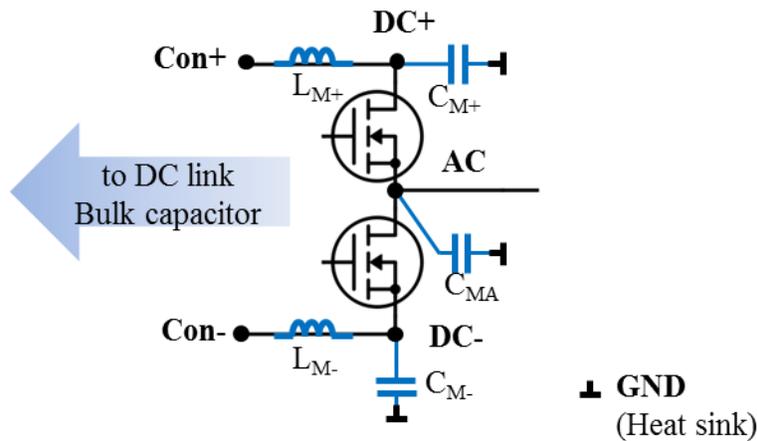


Fig. 2-32: Parasitic model of a bare SATIE module

2.3.2.1 Parasitic capacitances calculation – C_{M+} , C_{M-} and C_{MA}

A. By Q3D extraction

ANSYS Q3D Extractor takes into account the 2D or 3D structure of electronic packaging or PCB and the related insulation materials' properties, uses method of moments (MoM) and finite element method (FEM), to compute the partial inductive (partial self-inductance and mutual one) and capacitive elements. The module's layout can be imported from PCB design software EagleCAD to ANSYS Q3D in proper way. The relative permittivity ϵ_r of FR4 epoxy is calculated by the measurement of capacitance of a PCB with a known surface and its value is

estimated as 5.6 for the prototype module. **Fig. 2-33** shows all parasitic capacitances to be extracted in Q3D and their values

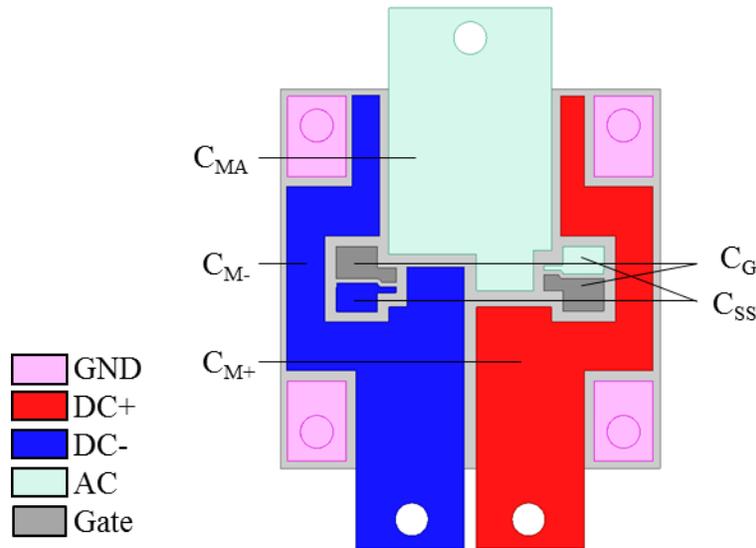


Fig. 2-33: Capacitances to be calculated in Q3D

are shown in **Tab. 2-2**. The capacitances between different copper pads on top layer are too tiny and therefore they are ignored. It should be noted that C_{SS} (capacitance between the kelvin source pad and GND) should be added with C_{M-} and C_{MA} respectively since they are connected inside the power device's package.

Tab. 2-2: Q3D extraction of parasitic capacitances in bare SATIE module

$C_{M+}=38.2\text{pF}$	$C_{M-}=41.7\text{pF}$	$C_{MA}=34.9\text{pF}$	$C_G=2.5\text{pF}$	$C_{SS}=2.0\text{pF}$
------------------------	------------------------	------------------------	--------------------	-----------------------

B. By impedance measurement

The parasitic capacitances can be directly measured one by one in a bare module without any semiconductor power chip. However, the bare module (only layout and interconnections, no semiconductors) is not often achievable. The measurement approach below provides the capability to measure parasitic capacitances directly in a completed module including semiconductors. In a first place the two GaN devices should be short-circuited between gate and

kelvin source so that each device is equivalent to a capacitance between drain and source with a value of C_{OSS} ($C_{DS}+C_{GD}$) at low V_{DS} voltage ($\sim 500\text{pF}$ for GS66508P). Therefore there are 5 unknown (C_{M+} , C_{M-} and C_{MA}) or roughly known (C_{OSS} of high-side and low-side devices) capacitances between the DC+, DC-, AC and GND potentials (**Fig. 2-34**).

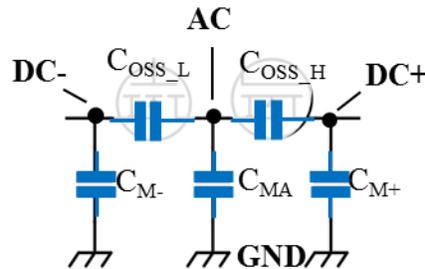


Fig. 2-34: Capacitances between different terminals

Since the error of several pF between the C_{OSS} of high-side device and the low-side one (mostly due to the manufacturing process, etc) can make a difference compared to the values of C_{M+} , C_{M-} and C_{MA} (according to the Q3D calculations), it is advised for precision purpose to treat the two C_{OSS} as two unknown coefficients – C_{OSS_H} and C_{OSS_L} . Finally 5 capacitance measurements with proper short or open-circuit operations should be done in order to determine the 5 unknown capacitances between terminals, as discussed hereafter.

In order to measure the capacitances of the module mentioned above without any soldering, 2×1 spring loaded connector arrays, as used in gate drive board, are used to take contacts on different terminal areas on the top layer. Each pair of those connectors allows to measure or short-circuit the capacitance between two terminals. All contact points are shown in **Fig. 2-35a**. Each pair of the spring loaded connectors is in parallel with a SMB adaptor for impedance measurement and a 2×1 pin array for short-circuits convenience by a jumper. All the connectors are configured in a PCB which is fixed above the power module via four screws (**Fig. 2-35b**). It should be noted that COM contact points (**Fig. 2-35a**) are for the measurement of the stray capacitance in the spring loaded connector together with the SMB connector, which should be compensated (subtracted) from the measurement results.

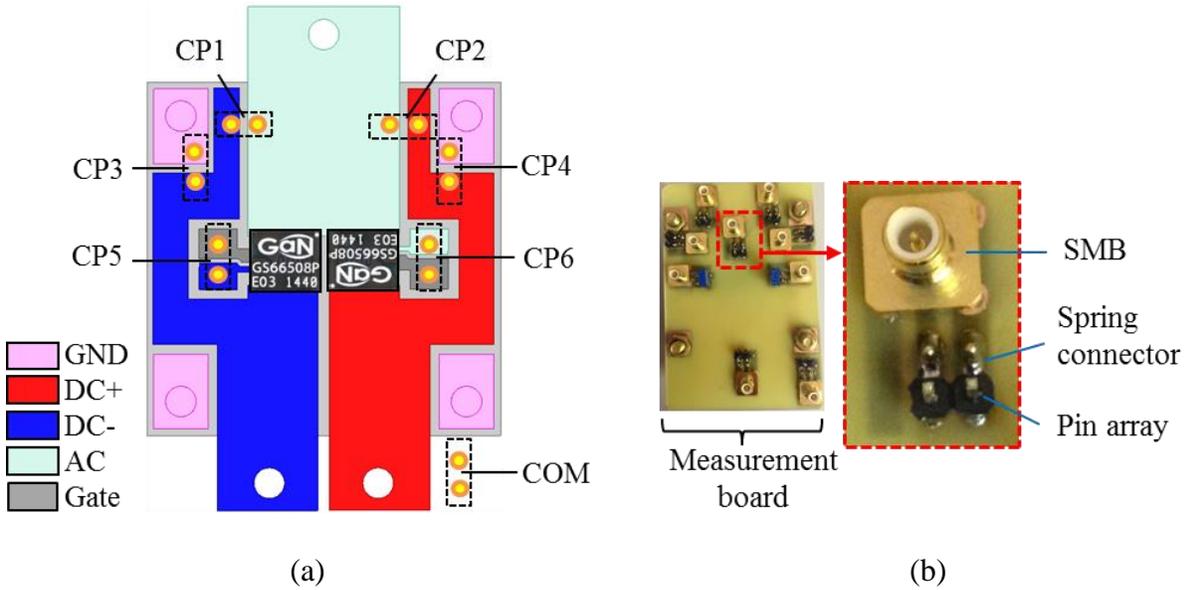


Fig. 2-35: Contact points for capacitances' measurement (a) and measurement board (b)

The measurement procedure is presented below:

- Preparation & Measurement method choosing

The contact points CP5 (gate and kelvin source for low-side GaN device) and CP6 (gate and kelvin source for high-side GaN device) are short-circuited before all measurement; in addition, since the “to be measured” capacitances' value is hundreds of pF, corresponding to very high impedance at the frequency range up to 30MHz, “GP series” impedance measurement configuration (Gain-phase with series-through) will be used [p9, Keysight 17].

- Calibration & Compensation:

After O/S/L calibration to the end of the cable, at least an “OPEN” compensation should be done at the COM contact point, in order to eliminate the test fixture stray capacitance between two spring connectors and the SMB connector. The value is measured as 2.0pF.

- Measurement 1:

Short-circuiting CP1 (DC- to AC) and CP2 (DC+ to AC); measuring capacitance of CP3 or CP4 (DC+ to GND or DC- to GND).

$$C_{M+} + C_{M-} + C_{MA} = 126.0 pF \quad \text{Eq 2-2}$$

- Measurement 2:

Short-circuiting CP2 (DC+ to AC) and CP3 (DC- to GND); measuring capacitance of CP4 (DC+ to GND).

$$C_{OSS_L} + C_{MA} + C_{M+} = 565.4 pF \quad \text{Eq 2-3}$$

- Measurement 3:

Short-circuiting CP1 (DC- to AC) and CP4 (DC+ to GND); measuring capacitance of CP3 (DC- to GND).

$$C_{OSS_H} + C_{MA} + C_{M-} = 571.2 pF \quad \text{Eq 2-4}$$

- Measurement 4:

Short-circuiting CP1 (DC- to AC) and CP3 (DC- to GND); measuring capacitance of CP4 (DC+ to GND).

$$C_{OSS_H} + C_{M+} = 525.9 pF \quad \text{Eq 2-5}$$

- Measurement 5:

Short-circuiting CP2 (DC+ to AC) and CP4 (DC+ to GND); measuring capacitance of CP3 (DC- to GND).

$$C_{OSS_L} + C_{M-} = 534.4 pF \quad \text{Eq 2-6}$$

Solving Eq 2-2 to Eq 2-6, the results are shown in **Tab. 2-3**.

Tab. 2-3: Measured parasitic capacitances in SATIE module

$C_{M+}=40.3pF$	$C_{M-}=47.5pF$	$C_{MA}=38.2pF$	$C_{OSS_H}=485.6pF$	$C_{OSS_L}=486.9pF$
-----------------	-----------------	-----------------	----------------------	----------------------

It should be noted that the measured results of C_{M-} and C_{MA} have included not only the C_{SS} but also the C_G mentioned in Q3D modeling part. Therefore, their values should be compared with the sum of C_{M-}/C_{MA} , C_G and C_{SS} calculated in Q3D. **Tab. 2-4** shows the comparison results. The errors are totally acceptable.

Tab. 2-4: Comparison of module parasitic capacitances by Q3D and by measurements

	$C_{M-}+C_G+C_{SS}$	$C_{MA}+C_G+C_{SS}$	C_{M+}
Q3D extraction	46.2pF	39.4pF	38.2pF
Measured	47.5pF	38.2pF	40.3pF

2.3.2.2 Parasitic inductances calculation – L_{M+} and L_{M-}

A. By Q3D extraction

The partial inductances L_{M+} and L_{M-} are illustrated in **Fig. 2-23** and its value can be calculated in Q3D as 11nH for each.

Tab. 2-5: Q3D calculated L_{M+} and L_{M-} values

$L_{M+}=11\text{nH}$	$L_{M-}=11\text{nH}$
----------------------	----------------------

B. By impedance measurement

There is no easy way to measure directly the aforementioned inductances. However, L_{M+} and L_{M-} 's values can be verified indirectly. Two test points are set as TP+ and TP- as shown in **Fig. 2-36a**. The impedance between the two test points should be the paralleling of the impedance on the left side and the one on the right side, thus $L_{P1}+C_{OSS}/2$ in parallel with $L_{P2}+L_{C+}+L_{C-}+L_{C0}+C_{BUK}$ as shown in **Fig. 2-36b**, where $L_{P1}+L_{P2}=L_{M+}+L_{M-}$. Since $L_{C+}+L_{C-}+L_{C0}+C_{BUK}$ and C_{OSS} are already known, $L_{P1}+L_{P2}$ should be able to be deduced.

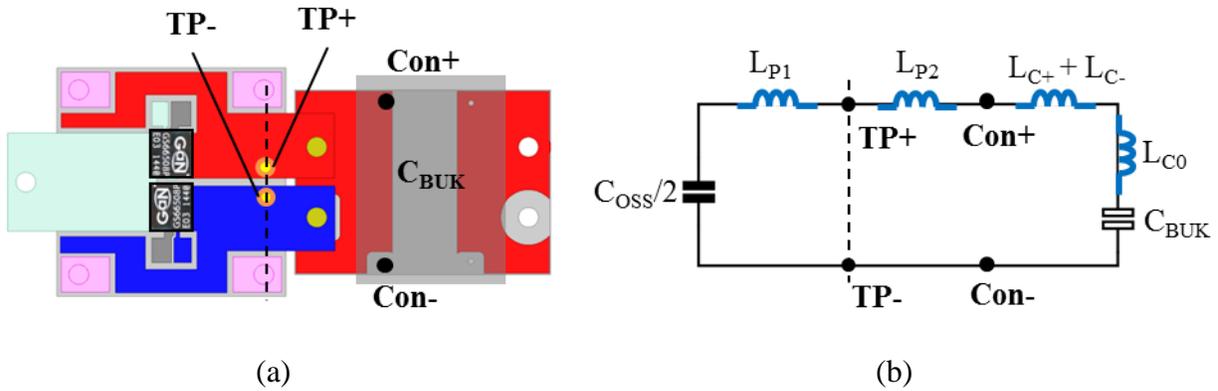


Fig. 2-36: L_{M+}/L_{M-} measurement test points setup (a) and the equivalent circuit (b)

The measurement result and the fitted model are shown in **Fig. 2-37**. The first magnitude valley is due to the resonance between the C_{BUK} ($30\mu\text{F}$) and the $L_{C+}+L_{C-}+L_{C0}+L_{P2}$; the second one is due to the resonance between the $C_{OSS}/2$ (30pF) and the L_{P1} .

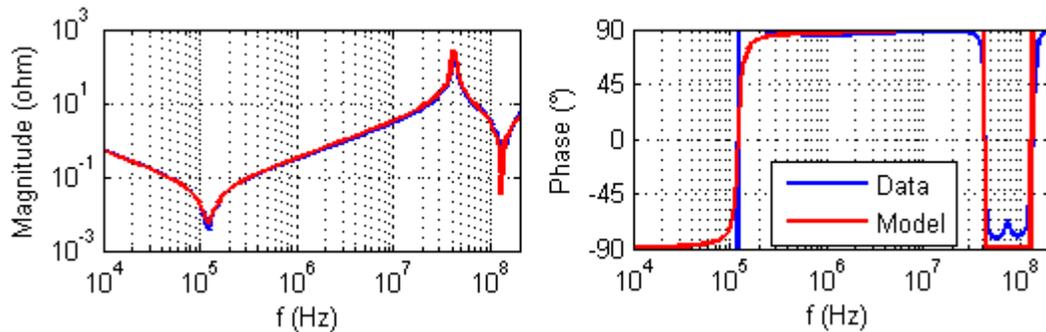


Fig. 2-37: Comparison between the fitted model and impedance measurement between TP+ and TP-

L_{P1} and L_{P2} are found as 6nH and 15nH respectively. The sum of these two measured inductances (21nH) is compared with the Q3D calculated ones, as show in **Tab. 2-6**.

Tab. 2-6: Comparison of calculated and measured $L_{M+}+L_{M-}$

	Q3D extraction	Measurement
$L_{M+}+L_{M-}$	22nH	21nH

2.3.2.3 Final model of the bare module with DC link bulk capacitor

The final module's model together with the DC link capacitor is presented in **Fig. 2-38**. There is an extremely large power loop inductance (over 60nH) in which the bulk capacitor and the power module terminals (including the capacitor supporting PCB board and the interconnection screws) contribute respectively around 35~40nH and 22nH.

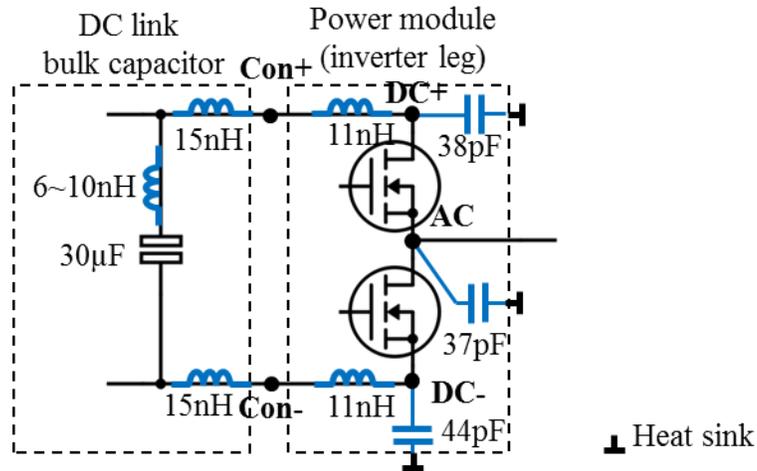


Fig. 2-38: Values of main parasitic elements in bare SATIE module with the DC link capacitor

2.3.3 In-module capacitors modeling

As shown in **Fig. 2-16**, three C_X capacitors in 2220 package are in parallel while one C_Y capacitor in 1206 package on each DC side.

2.3.3.1 Capacitors C_X

Three C_X capacitors – C_{X1} , C_{X2} and C_{X3} – and the GaN devices are modeled in Q3D as shown in **Fig. 2-39a**. The GaN devices are short-circuited. The parasitic inductances between A+ and A-/B+ and B-/C+ and C- are calculated as 2.5nH, 3.4nH and 4.3nH. The three values should be added with the GS66508P GaN devices' package parasitic inductance which is 0.5nH. Therefore, the three power loops can be modeled as distributed partial inductances as shown in

Fig. 2-39b. ESL is the equivalent series inductance of the 2220 package of the C_X capacitor. According to [AVX] it can be estimated reasonably as 0.5nH.

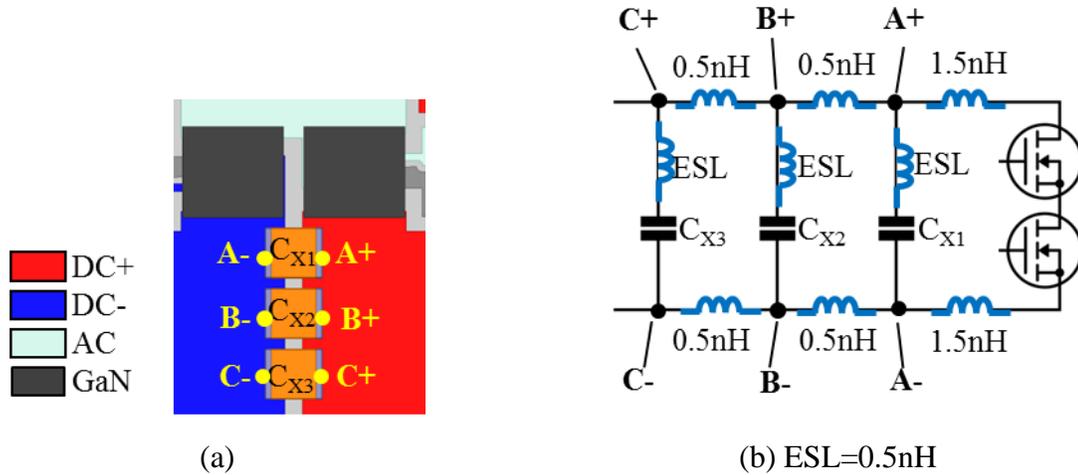


Fig. 2-39: Power loop for different C_X capacitors (a) and the equivalent circuit (b)

2.3.3.2 Capacitors C_Y

The loop inductance formed by the two C_Y capacitors and the GaN devices and the backside of the power module (GND) is illustrated in **Fig. 2-40**. This loop (in yellow dashed line) inductance is calculated by Q3D as 5.5nH. Being added with 0.5nH from the two GS66508P packages and with 2nH [AVX] from the 1206 package of two C_Y capacitors, the total loop inductance is 8nH. Therefore, each C_Y capacitor's partial inductance is distributed equally as 4nF as shown in **Fig. 2-41**.

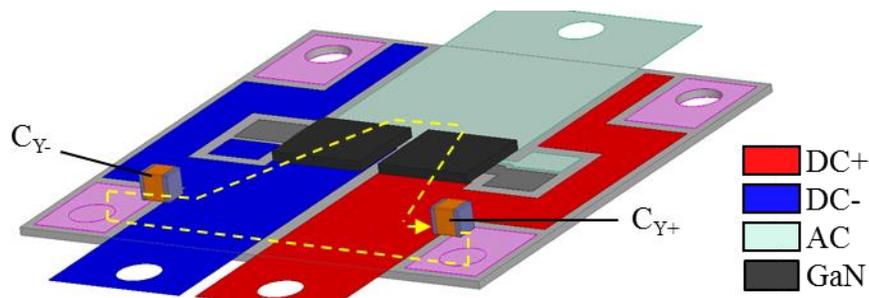


Fig. 2-40: Illustration of the inductive loop of C_{Y+}/C_{Y-} capacitors

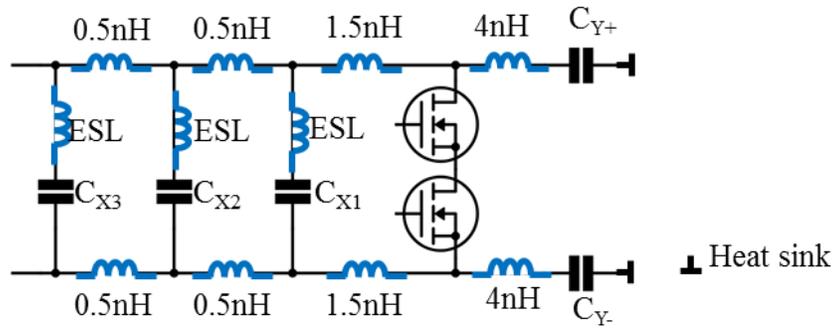


Fig. 2-41: Parasitic inductance with C_X and C_Y in SATIE module

2.3.3.3 Final model of the SATIE module with in-module capacitors

The full circuit model of the SATIE module including C_X and C_Y capacitors with DC link bulk capacitor is shown in Fig. 2-42, with parasitic elements in blue color and discrete components in black color.

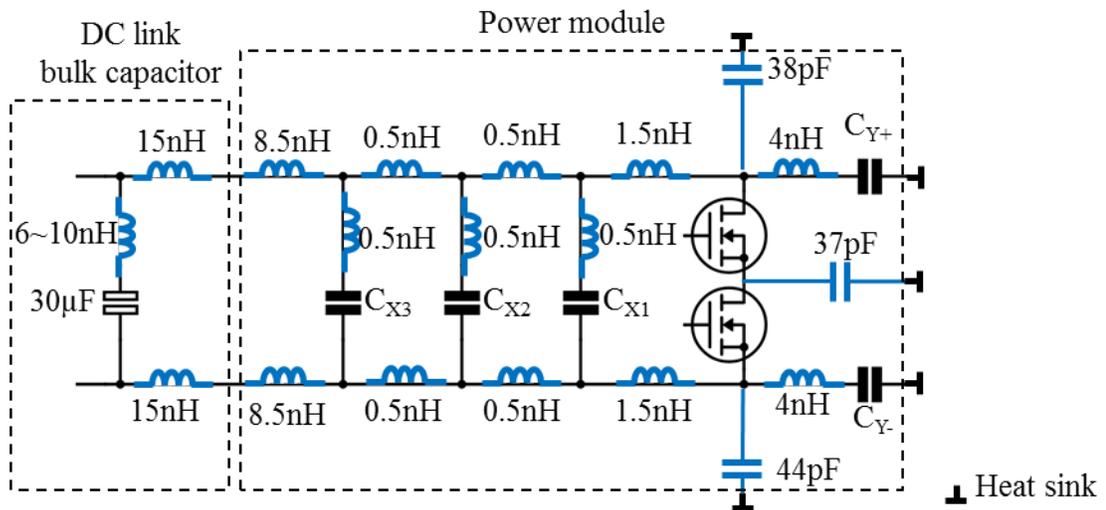


Fig. 2-42: Full model of SATIE module with in-module capacitors

2.3.4 Gate driver modeling

The model of gate driver does not consider the gate loop inductance since it does not change the voltage or current switching waveform [Wang 13] and thus does not influence the

EMI performance. Therefore, only the turn-on and turn-off loop resistance have been taken into account. R_{G_ON} includes the discrete SMD resistor (10Ω) and the internal R_{OH} of gate driver (2.7Ω) and R_{G_OFF} includes the discrete SMD turn-off resistor (0Ω) and the internal R_{OL} of the gate driver (1Ω). The contact resistance of the spring load connector can be ignored. V_{GG} is the model of the output voltage of the gate driver IC. It is modeled as a trapezoidal waveform with T_R and T_F which are measurement of V_{GS} without turning on the DC power.

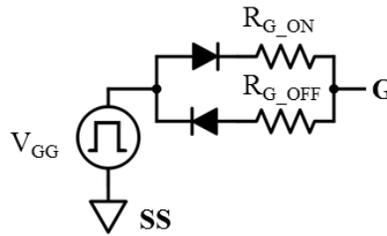


Fig. 2-43: Model of the gate driver: $R_{G_ON}=12.7\Omega$, $R_{G_OFF}=1\Omega$, $T_R=10ns$ and $T_F=10ns$

2.4 Conclusions

Main parasitic elements influencing the switching waveforms and the EMI propagation path are reviewed in the first part of this chapter. Based on these elements, the state-of-the-art low inductive power module technologies for WBG devices are reviewed.

Based on the power module designs in the MEGAN project, a SATIE module is designed and manufactured for the research purpose in this dissertation. This module is modeled with lumped impedances which are identified by either numerical calculation or impedance measurement or both. The coherence between the impedance measurement and the numerical calculation justifies the precision of the developed model.

CHAPTER 3

SWITCHING WAVEFORMS ANALYSIS

The GaN semiconductor device and the power module including the DC link capacitor have been studied and modeled in the previous chapters. The full package of the aforementioned models will be verified by the switching waveforms in this chapter.

The switching waveforms (voltage and current) in a switching cell are not only crucial for the switching loss evaluation but also are the source of the conducted EMI noises in both differential and common modes. These waveforms, especially the transients (dV/dt and dI/dt) are due to both the intrinsic properties of the power device and the relevant parasitic elements in the switching environment. Therefore, the switching waveforms' test is an efficient way to evaluate the power device model together with parasitic elements in power loop.

In the first part of this chapter, the switching test setup is presented, including the load resistor and inductor's modeling and the precautions for voltage and current measurements;

In the second part, the measured switching voltages in different working points, without and with in-module C_X capacitors, will be compared with the simulations;

In the final part, a parametric study for the switching voltage overshoot minimization is presented.

3.1 Test setup

The switching waveforms can be evaluated typically by adding a resistor and an inductor as load between the AC terminal and one DC terminal of an inverter leg and switching the power devices permanently. This method accumulates switching energy loss in the power devices and heats them up significantly. In order to evaluate the switching waveforms without heating the power device, the double-pulse test will be executed.

A double-pulse test's configuration is shown in **Fig. 3-1a**. The high value C_{BUK} capacitor is powered to a desired DC voltage. A load inductor L_{LOAD} is connected between the DC+ and the AC terminal, thus in parallel with the high-side transistor. This transistor, named GaN_{SYN} , is short-circuited at gate terminal so that it is permanently at off state and it can be reversely conductive when there is freewheeling current. The low-side transistor GaN_{SW} , which is the device to be tested, is switched with gate bias as shown in V_{GS} of **Fig. 3-1b**. The first pulse is to establish the desired current in the inductor load under a desired DC voltage. Therefore, the end of the first pulse can be used as the turn-off switching characterization and the beginning of the second pulse can be used for the turn-on one. This approach allows the switching evaluation under room temperature since only a couple of switching does not accumulate power loss thus the transistors will not be heated.

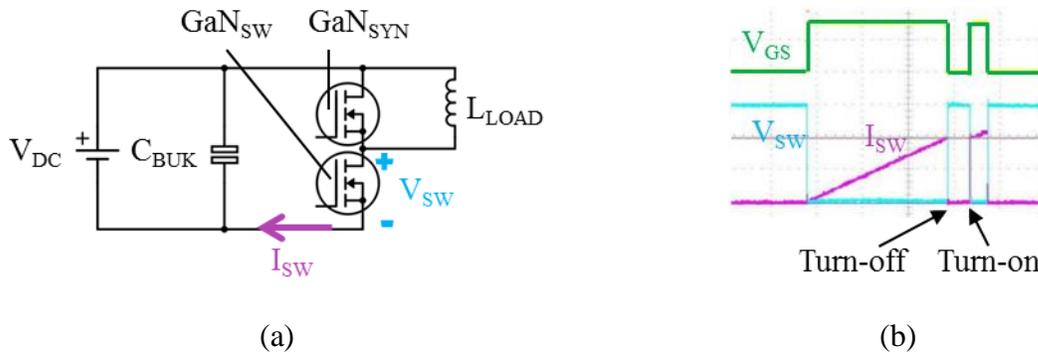


Fig. 3-1: Double pulse test circuit presentation (a) and typical waveforms (b)

Since both permanent switching and double-pulse switching will be tested, the load resistor and inductor will be modeled at first. Then the voltage and current measurement

precautions will be discussed. Finally the test bench with all measurement equipment will be presented.

3.1.1 Load modeling

Briefly saying, the resistor (R) load value determines the average load current value in steady state and the inductor (L) load value should be large enough to maintain this current during a switching period. However, in HF some stray elements will influence the switching and the EMI performance.

- Considering switching, the inter-winding capacitance of power RL load, which are often modeled as in parallel with RL, will influence the switching characteristics of the power device. This is because the stray capacitance is also in parallel with the output capacitance (C_{oss}) of the power device and when its value is comparable or even much bigger than C_{oss} , the switching voltage variation will be modified [Zhang 15].
- Considering EMI 1) as is well known that the voltage at the mid-point of the half bridge is the CM EMI noise source; this voltage is potentially modified by the stray capacitance of RL load as discussed above; 2) since the RL load is often attached to a grounded heatsink which will cause a large value capacitance between the RL load and the ground, this results in a CM EMI propagation path in addition to the famous mid-point capacitance in half bridge.

Therefore, for switching and EMI studies, the relevant HF stray elements should be carefully measured and modeled. The RL loads used below are chosen purposely with simple impedance characteristics so that all the parasitic elements can be precisely modeled. In general, either R or L can be treated as two-port network as shown in **Fig. 3-2**. A and B are the two terminals while C is the ground connection. Therefore, R or L load can be modeled as three impedances Z_{AB} , Z_{AC} and A_{BC} .

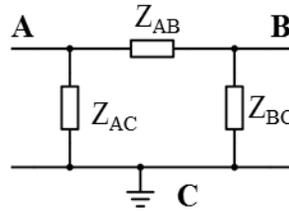


Fig. 3-2: Two-port network model for R or/and L load

3.1.1.1 Resistor modeling

A power resistor of 47Ω from Vishay (**Fig. 3-3**) is attached to a ventilated grounded heatsink via a layer of thermal grease, which results in a high value stray capacitance between R and the ground. A and B are two terminals of this power resistor; C are the contacts of the grounded heatsink. Two SMB terminals are connected temporarily between A and C, B and C, allowing the impedance measurement. Supposing this resistor has a good symmetry, $Z_{AC}=Z_{BC}$; they represent the stray capacitance between the resistance and the grounded heatsink. Z_{AB} is the resistive part around 47Ω and probably with some HF effect.

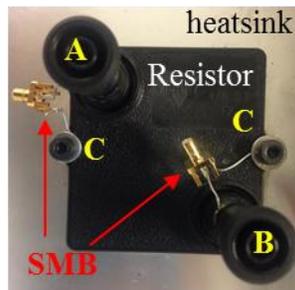


Fig. 3-3: Resistor load used in this dissertation

Two measurements have been done: 1) Measuring impedance Z_1 between A/B and C with A and B short-circuited; 2) Measuring impedance Z_2 between A and C with B and C short-circuited. Therefore:

$$Z_1 = Z_{AC} // Z_{BC} \quad \text{Eq 3-1}$$

$$Z_2 = Z_{AB} // Z_{AC} \quad \text{Eq 3-2}$$

Since $Z_{AC}=Z_{BC}$, **Eq 3-1** can be rewritten as:

$$Z_{AC} = Z_{BC} = 2 \cdot Z_1 \quad \text{Eq 3-3}$$

Z_{AB} and Z_{AC} (Z_{BC}) can be deduced from **Eq 3-2** and **Eq 3-3** with the measurement of Z_1 and Z_2 , as shown in **Fig. 3-4**:

Z_{AC} (Z_{BC}) is simply modeled as a capacitance by fitting its impedance. Z_{AB} looks like a series of a resistance and an inductance at first glance, however; however, with a physical respect of skin effect and impedance fitting matter, it is modeled with an additional one-deep Ladder model [**Kundert 06**]. The completed model is shown in **Fig. 3-5**. R_0 and L_0 represent the physical values of the resistor and the stray inductance inside the resistor; R_1 and L_1 are used to model the AC resistance due to skin effect; C_0 represents the distributed stray capacitance between the resistor and the grounded heatsink.

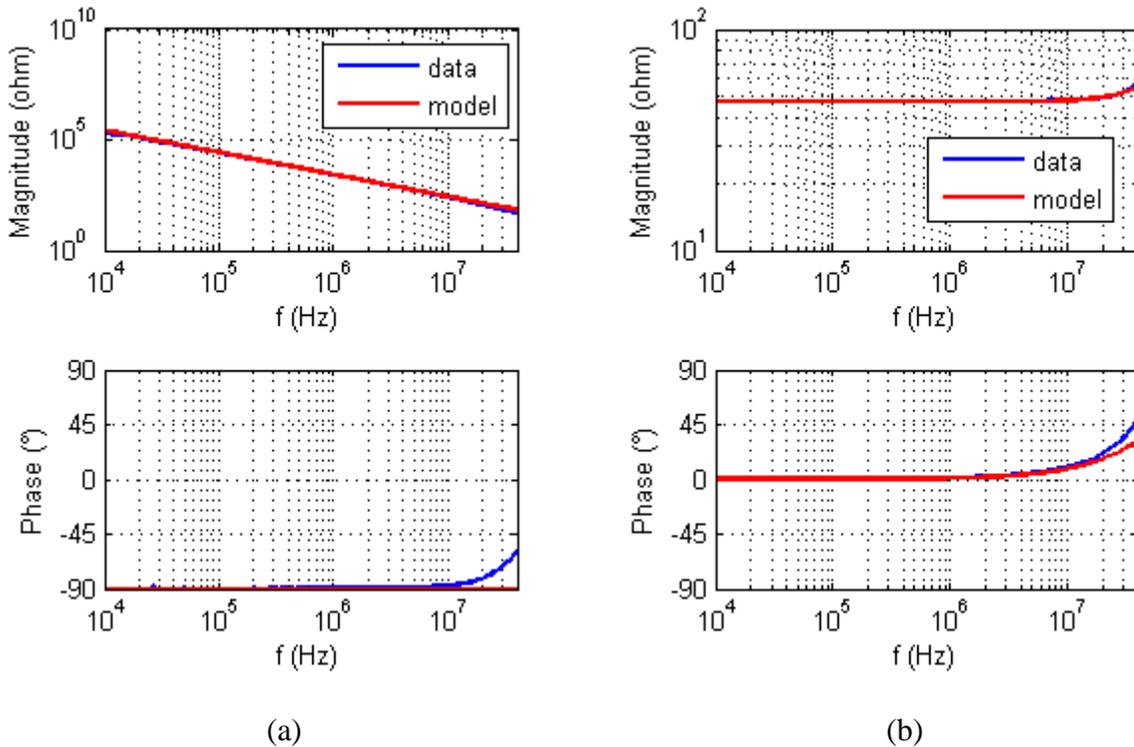


Fig. 3-4: Measurement and modeling of Z_{AC} / Z_{BC} (a) and Z_{AB} (b) of the resistor load

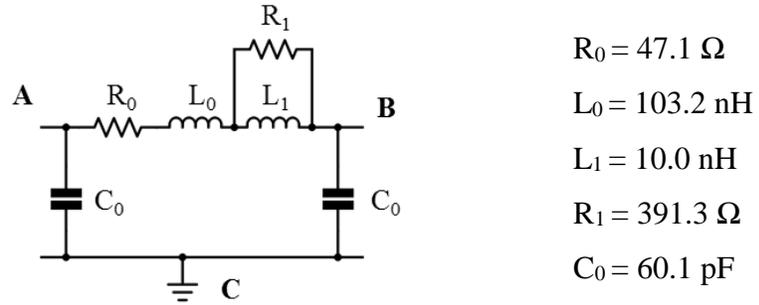
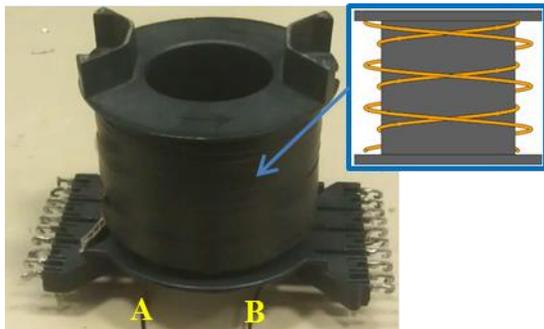


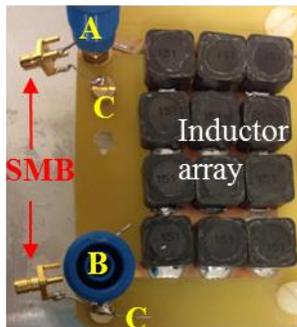
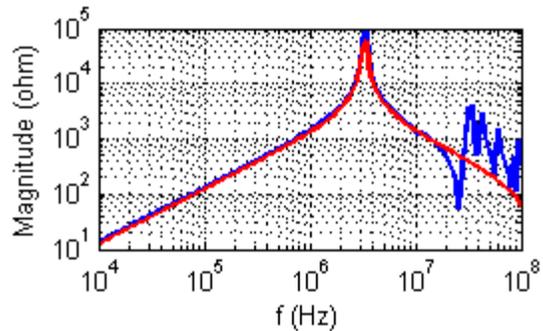
Fig. 3-5: Model of the resistor load

3.1.1.2 Inductor modeling

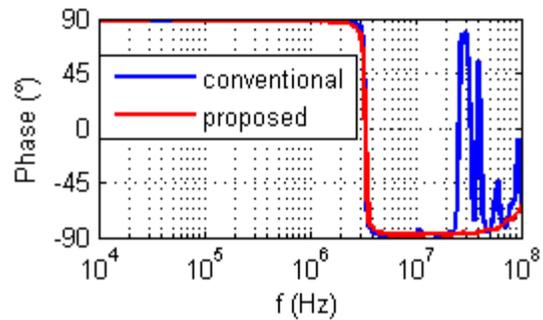
A conventional power inductor is often wound around an air core in certain way to minimize the inter-winding capacitance, as shown in Fig. 3-6a. The impedance Z_{AB} without ground plane is shown with blue line in Fig. 3-6c.



(a) Conventional load inductor



(b) Proposed load inductor



(c) Impedance between A and B

Fig. 3-6: Load inductors and their measured impedances

There are several distributed resonances from 10MHz to 100MHz (blue line) due to the propagation effect in the winding which will result into a complicated model and thus increasing the volume of calculation in simulation. Besides, the distribution of stray capacitances between the inductor and the grounded heatsink becomes complicated as well. Therefore, an array (3x4) of SMD power inductors (SRR1280-151K of Bourn) is used as the proposed one (**Fig. 3-6b**). It has simple impedance in a wide frequency range (red line) and meanwhile a sufficient saturation current rating (5.7A). In addition, it has been fixed high enough from the heatsink to reduce the CM capacitance.

The modeling method is the same as in R modeling. The measurement and modeling results are shown in **Fig. 3-7**. The complete model is shown in **Fig. 3-8**. L_0 represents the physical value of the power inductor, EPC represents the inter-winding capacitance and C_0 represents the distributed CM capacitance.

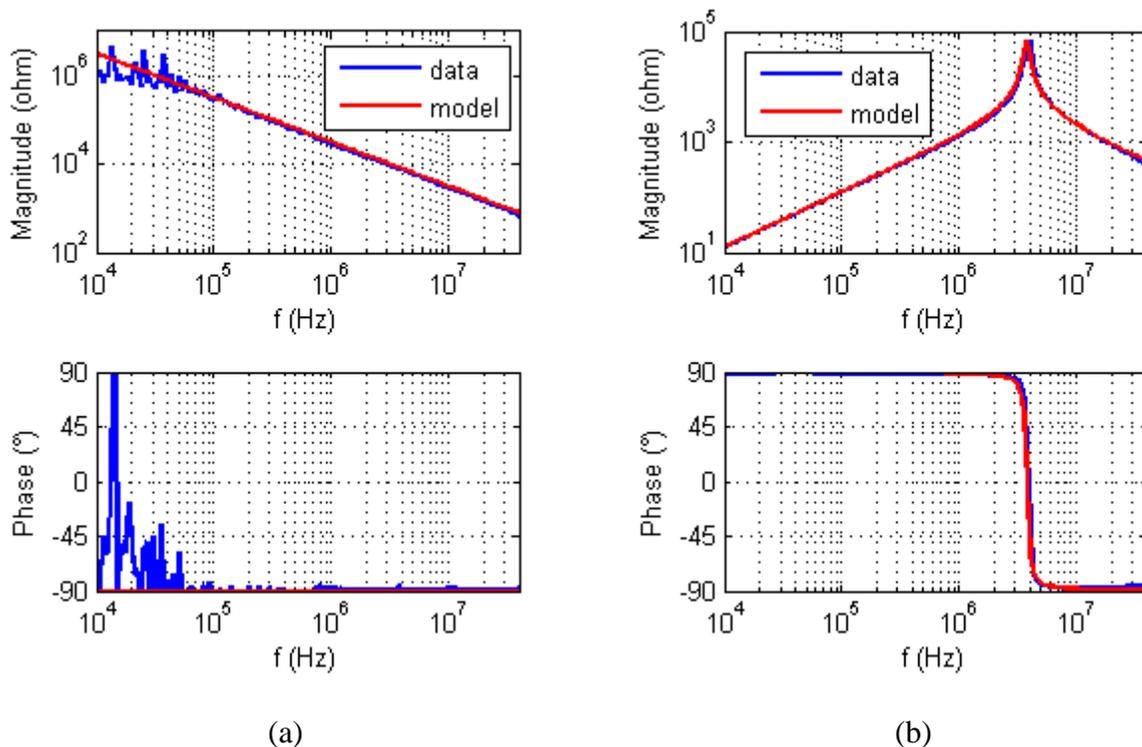


Fig. 3-7: Measurement and modeling of Z_{AC}/Z_{BC} (a) and Z_{AB} (b) of the inductor load

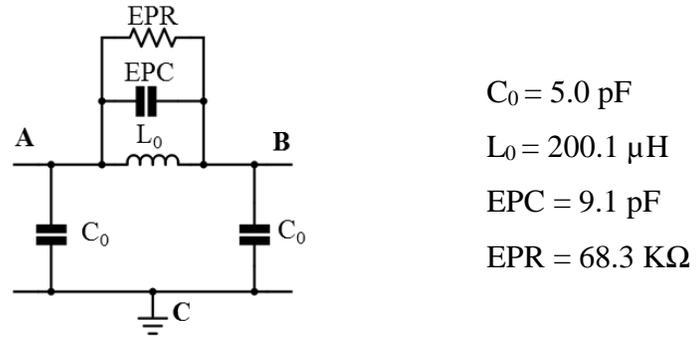


Fig. 3-8: Model of the inductor load

3.1.1.3 Final model

The final RL model is a series of R and L model, as in **Fig. 3-9**. A is the terminal of the resistor side and B is the one of the inductor side, with C the ground. Well matched comparisons between impedance measurements and model are shown in **Fig. 3-10**.

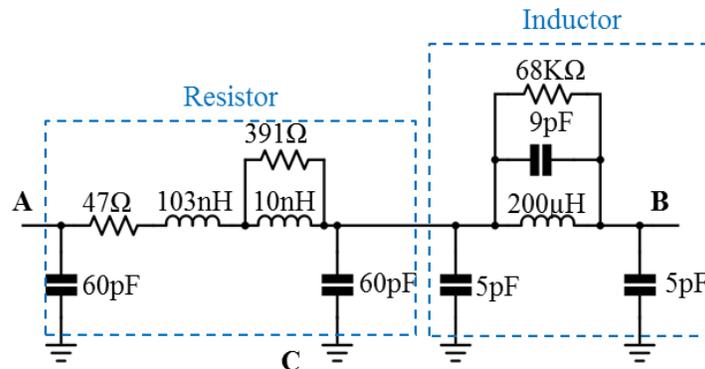


Fig. 3-9: Full model of R and L loads

It should be noted that, the CM capacitances' values in the RL model indicate that the resistor side ($60\text{pF}+60\text{pF}+5\text{pF}$) provides much larger CM EMI path than the inductor side (5pF). Therefore, connecting L or R to the AC terminal of the inverter leg will cause difference in CM noise magnitude and the noise mode transformation. These effects will be discussed in chapter 4.

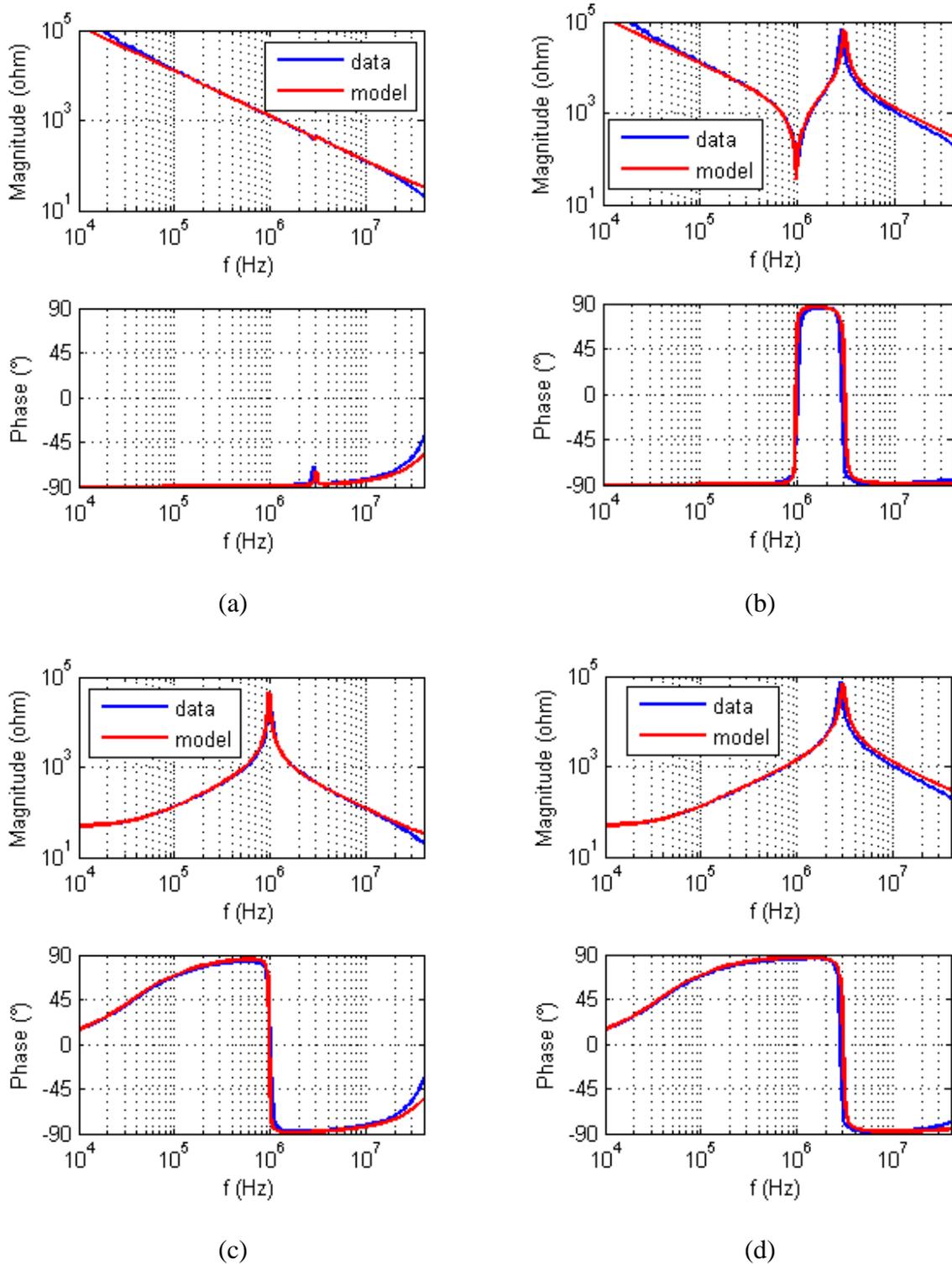


Fig. 3-10: Measurement and model – Z_{AC} with B and C opened (a); Z_{BC} with A and C opened (b); Z_{AC} with B and C shorted (c); Z_{BC} with A and C shorted (d)

3.1.2 Measurement precautions

The most obvious advantages of GaN devices, comparing to their Si counterparts, are much faster switching and higher intensity integration capability. Both of them result in challenges for voltage and especially current measurement in a switching cell.

3.1.2.1 *Current measurement*

Current measurement in a switching cell is up to now a contradictory issue: the high bandwidth and high current rating require a voluminous sensor which increases the parasitic inductance in power loop and degrades the electric performance, which is contradictory to the requirement of “clean switching” [Bayerer 10]. Therefore, either relatively precise current measurement or the most proper switching will be achieved. Generally speaking, current measurement in a switching cell is for:

- 1) Short-circuit protection;
- 2) Characterizing the switching transient.

The former is essential in industrial level product. However, current sensor is not the only solution for short-circuit protection – the drain source voltage detection inspired by typical IGBT power circuit [Li 16] or dI/dt detection on parasitic inductance [Kawase 15] have proved their feasibility in GaN or SiC based low-inductive power inverters.

The latter is often for academic research purpose. The state-of-the-art current sensing technologies will be discussed below:

- The most adapted method is the technology of mirror transistor in parallel of the main power device which will divert a tiny portion of the channel current and reflect the total one by its drain-source voltage. This small transistor could be monolithically integrated with the main power GaN device in the same substrate. However, this solution is yet to come into the market or even sample, the method is only tested with discrete GaN devices [Biglarbegian 17].
- Coaxial shunt [Billmann] is widely used thanks to its large frequency bandwidth (up to 2GHz). In fact it is the reference high-frequency current sensor for fast switching WBG devices in most of the publications. However, it inserts also a relatively large parasitic

inductance in the measurement loop due to its voluminous body which degrades the switching performance.

- Transformer type current sensors provide galvanic isolation for current sensing. In addition, proper design integrates the transformer coil directly in the PCB to make the current sensor low profile [Li 15] [Wang 15]. The bandwidth is the main limiting factor, for which a typical Rogowski sensor has a bandwidth up to $\sim 30\text{MHz}$ while a typical Pearson sensor has a bandwidth up to $\sim 200\text{MHz}$. It should be noted that the maximal current measuring capability is always contradict to the frequency bandwidth for these transformer based current sensors.
- A more advanced design based on Rogowski transformer (**Fig. 3-11**), which allows to measure up to 80A with a frequency bandwidth $300\text{ kHz} \sim 500\text{ MHz}$. The U type coil inserts only less than 1nH inductance. However, the large receiver unit takes space so that the switching loop is enlarged as well as a coaxial shunt.

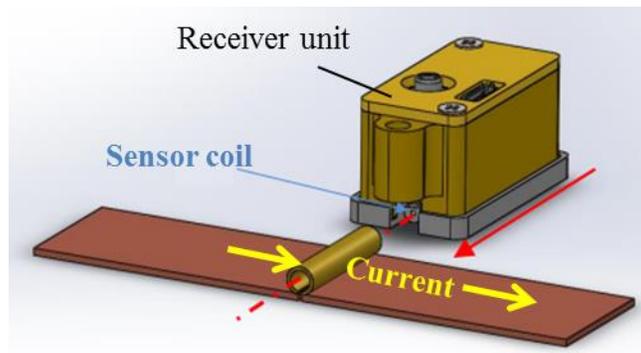


Fig. 3-11: IZM Rogowski current sensor [IZM]

Nevertheless, not any current sensor mentioned above is capable to measure the HF current in a switching loop formed by two GaN chips and ceramic capacitor nearby as shown in SATIE module. Since the current sensing is not the main issue in this dissertation, the following study will not include any switching current sensing. But this issue remains of interest for future researches.

3.1.2.2 Voltage measurement

The voltage measurement is less complicated than current measurement. Nevertheless, a high-frequency bandwidth is required for measuring the high slew rate of switching voltage. In addition, the influence of the parasitic inductances to measurement errors should be understood.

According to the latest reports of the GaN devices' manufacturers, the edge time (rise or fall time) of voltage between the drain and source terminals is around 300ps for low-voltage GaN HEMT [**Lidow 15**] and 5ns for high-voltage one [**GaN Systems 16**]. Supposing they are the real edge time (T_{edge}) of the GaN devices, the measured edge time ($T_{measure}$) shown in a scope via a voltage probe is [**Sandler 15**]:

$$T_{measure} = \sqrt{T_{scope}^2 + T_{probe}^2 + T_{edge}^2} \quad \text{Eq 3-4}$$

Where T_{scope} and T_{probe} are respectively the edge time of the scope and the voltage probe. If an accuracy of 5% for the measured edge time is required:

$$T_{measure} = (1 + 5\%) \cdot T_{edge} \quad \text{Eq 3-5}$$

Giving that the corresponding frequency bandwidth (BW) of an edge time is:

$$BW = \frac{1}{\pi \cdot T_{edge}} \quad \text{Eq 3-6}$$

Solving the **Eq 3-4** ~ **Eq 3-6**, the probable combination of scope and probe with sufficient frequency bandwidth are:

- 6GHz scope with >5.2GHz probe for low-voltage GaN device;
- 1GHz scope with 300MHz probe for high-voltage GaN device.

Since only high-voltage (600V) GaN devices will be studied, the latter combination of scope and voltage probe will be the standard requirement for all measurement equipment for the following studies – a 1 GHz scope (TPO7104 from Tektronix) and a 500 MHz passive voltage probe (P6139B from Tektronix) will be used in this dissertation.

3.1.2.3 Influence of parasitic inductances

A. Voltage measurement

The drain-source voltage V_{DS} measurement is taken as an example, as shown in **Fig. 3-12a**. This voltage V_{DS} is measured by a typical passive probe which is represented by an input capacitance C_{IN} and a paralleled $1M\Omega$ resistor.

L_{p1} is the parasitic inductance introduced by the grounding lead of a typical passive voltage probe. It will oscillate with the input capacitance (C_{IN}) of the voltage probe and introduce measurement error. Therefore, it is recommended to shorten this grounding lead or use probe-tip adaptor.

L_{p2} is the parasitic inductance adding in series with the output capacitance (C_{OSS}) of the power chip, which is due to the power device package and the relevant PCB trace. Therefore, the voltage between the test point TP and the ground is naturally more damped than the voltage across the C_{OSS} which is the real drain source voltage of the power chip as shown in **Fig. 3-12b**, in which an example of the comparison between the simulated voltage at C_{OSS} (1nF) and the one at C_{OSS} (1nF) + L_{p2} (1nH) with 1ns as the voltage rising time, the voltage difference is as high as 100V. This means the real drain source voltage overshoot might be much higher than the measured one, especially when the voltage slew rate is significantly high. The higher the value of L_{p2} is, the larger the difference between the measured V_{DS} voltage and the real one is. Therefore, it is recommended to put the test points close to the power chip.

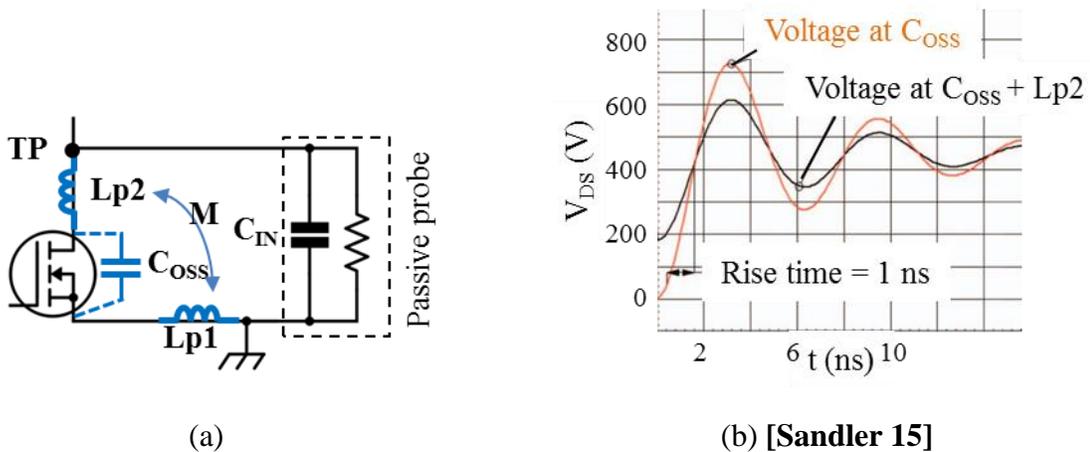


Fig. 3-12: Parasitic inductances in voltage measurement (a) and their influences (b)

B. Current measurement

The measurement of the switching current I_{DS} with a shunt resistor R is taken as an example as shown in **Fig. 3-13a**.

L_{p1} is the parasitic inductance introduced by the voltage probe's test tip. L_{p2} is the parasitic inductance in common between the current path and the voltage measurement. In addition, a mutual inductance M exists between L_{p1} and L_{p2} ; eventually a positive M inductance will increase the effect of the L_{p2} .

With a very high slew rate of the switching current, which is the case of a GaN HEMT, the measured current (voltage on $R+L_{p2}$) is amplified significantly from the real one (voltage on R). **Fig. 3-13b** shows the measured current (blue line) by a paralleled array of 0603 packaging film resistors and the simulated current (red line). The difference of the two currents allows determining the value of the inductance L_{p2} , which is only 0.15nH. This value is reasonable considering the tiny resistors and the PCB layout. However, its influence onto the current measurement is quite significant. Therefore, both the minimizing of the $L_{p2}+M$ inductances and the correction of the measured current are recommended for future work.

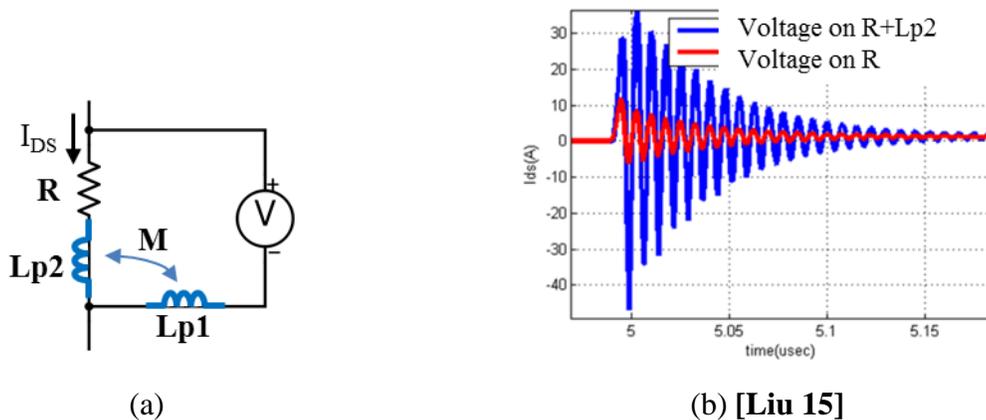


Fig. 3-13: Parasitic inductances in current measurement (a) and their influences (b)

3.1.3 Test setup

The complete double pulse or permanent switching test setup is shown in **Fig. 3-14**. V_{DC} is a 600V/20A lab power supply; it provides the desired DC voltage to the DC link capacitor C_{BUK} (see 2.3.1) to create a voltage source close to the GaN inverter leg, where the synchronous

GaN HEMT (GaN_{SYN}) is short-circuited at gate terminal and the switching GaN HEMT (GaN_{SW}) is controlled at gate by double pulse from signal generator.

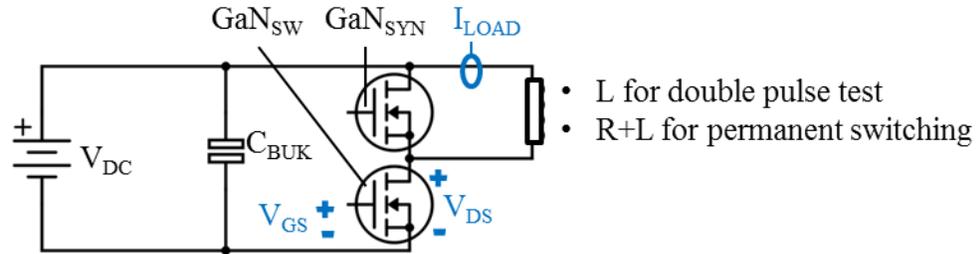


Fig. 3-14: Double pulse test and measurement set up

Tab. 3-1 shows a resume of the main measurement staffs.

Tab. 3-1: Resume of double pulse/permanent switching test setup measurement equipment

Measuring	Reference	Characteristics
Scope	DPO7104	8 bit; 1 GHz
V_{DS}	P6139B	300 V; 500 MHz
V_{GS}	TPP0200	200 V; 200 MHz
I_{LOAD}	TCP0030	30 A; DC to 120 MHz

It should be noted that the load current measurement is just for monitoring and it should be inserted at the DC+ side rather than the AC side. This is for the reason that common mode EMI noise will be coupled to the transformer type current sensor via the stray capacitance between them. **Fig. 3-15** shows the distortion of the current measurement with different locations (DC+ or AC side) of the load current sensor; the measurement in AC side is apparently with more distortion.

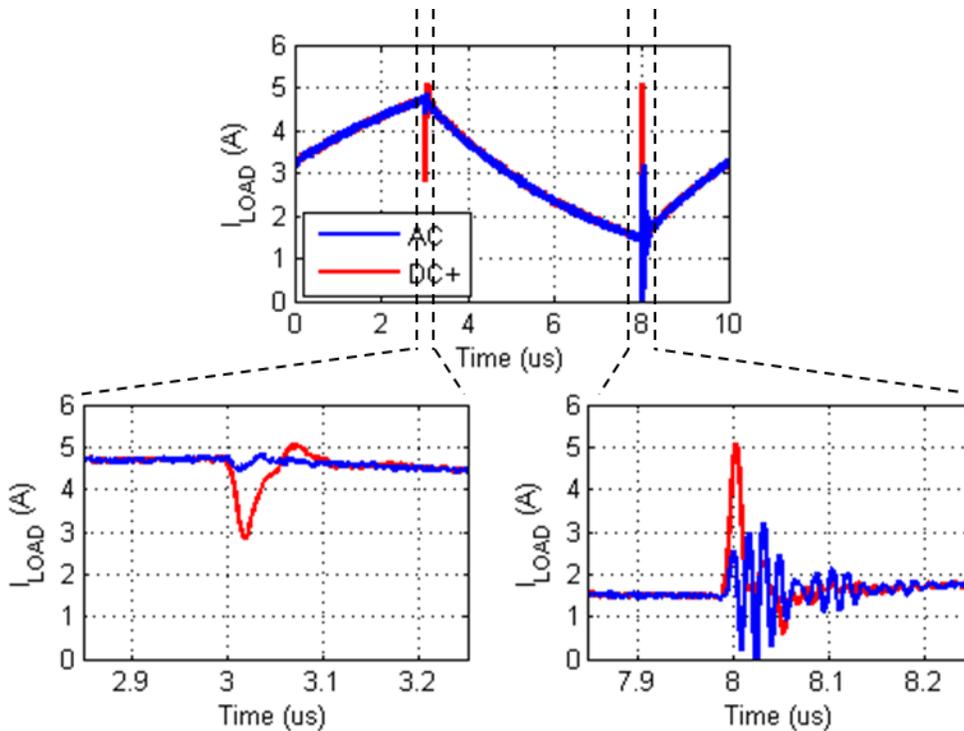


Fig. 3-15: Distortion of the load current measurement for different locations of the current sensor.

Meanwhile, all passive voltage probes should be added with common mode choke in case that CM EMI noise result in measurement errors or even dysfunctionality of any unit in the setup.

Followed by the double pulse test, permanent switching at 100kHz will also be tested with loading the GaN inverter leg with a series of resistor and inductor. This will heat up the two GaN HEMTs and thus their chip temperature should be monitored. Two glass fiber temperature sensors are attached to the top surface of the GaN chips by high temperature Kapton polyimide film tape (**Fig. 3-16a**). The temperature sensors are connected to PID temperature regulators to show the temperature on screen. **Fig. 3-16b** shows that switching at 300V, the switched GaN (GaN_{SW}) is measured at about 60°C and the synchronized one (GaN_{SYN}) is measured at about 80°C . An alternative way to monitor the temperature is to dig holes at the gate driver board above the power module; an infrared thermometer or a thermal camera can detect the temperature of the GaN chip through the holes above them.



Fig. 3-16: Temperature sensor location (a) and PID regulator screen (b)

3.2 Switching with bare module

In this section the GaN module will be tested without any in-module capacitor. Two switching modes will be considered:

- The GaN_{SW} switches on double pulse mode with a single inductor load at 150V and 300V; thus the GaN HEMT's model at room temperature 25°C could be validated. (see 3.2.1)
- Then it switches permanently with resistor and inductor load at 300V, 100kHz and duty circle 0.5; thus the GaN HEMT's model at a higher temperature (~60°C) could be validated. (see 3.2.2)

3.2.1 Double pulse test

The measured and simulated switching voltages V_{DS} and V_{GS} at 300V 15A are compared in **Fig. 3-17**. A huge difference is observed at the turn-on waveforms. The oscillations at V_{GS} and the voltage V_{DS} drop imply the value of the common parasitic inductance L_m between the power loop and the gate loop as shown in **Fig. 1-31** (c.f. 1.2.3). Reminding that L_m includes the physical common parasitic inductance and the mutual one between the two loops. 1nH is chosen as a reasonable value for L_m to fit the simulated turn-on waveform to the measured one. **Fig. 3-18** shows the comparison and apparently the coherence verifies the value of L_m .

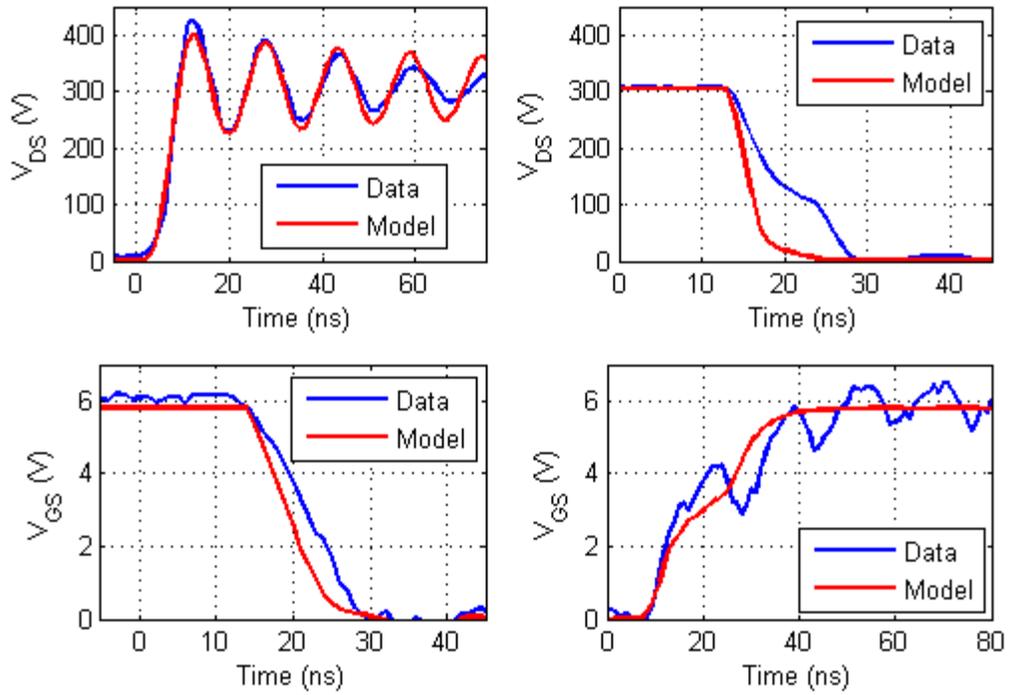


Fig. 3-17: Measured (data) and simulated (model) V_{DS} and V_{GS} at 300V/15A

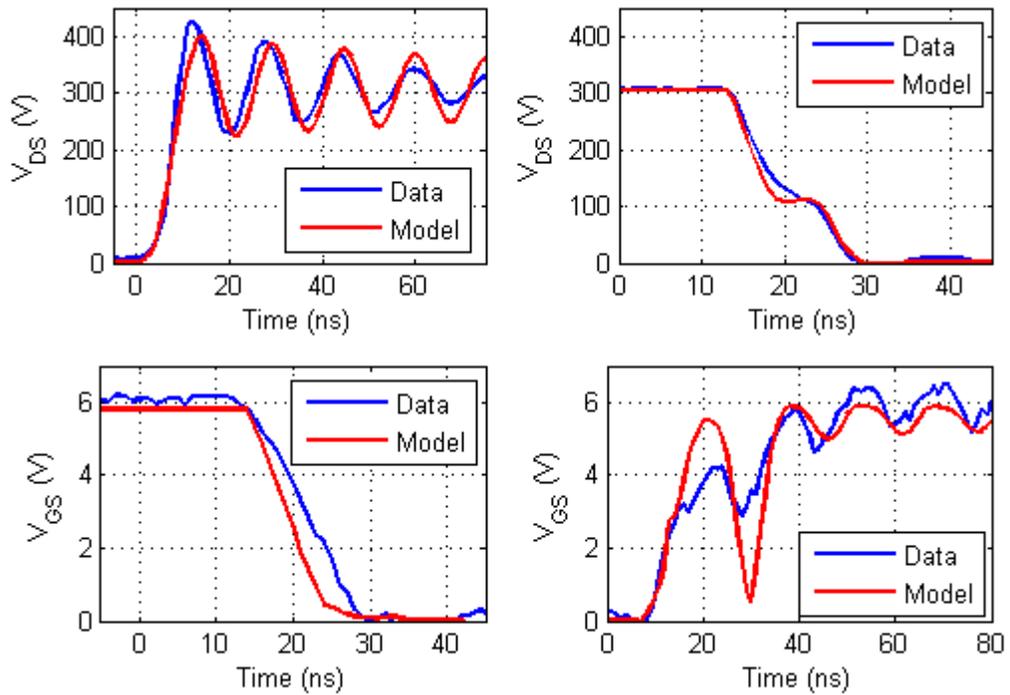
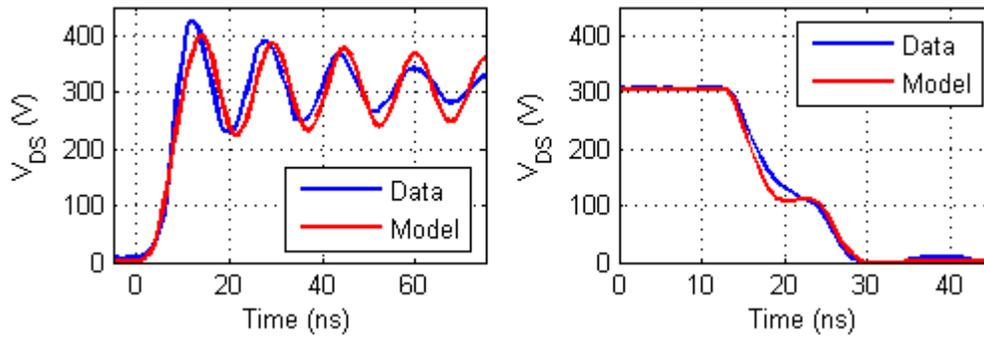


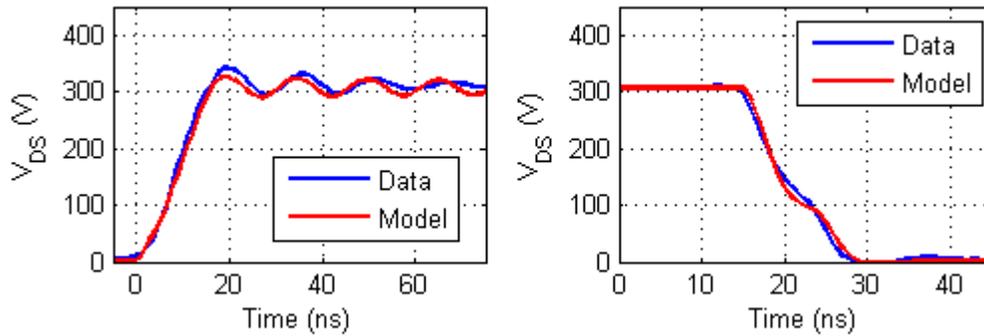
Fig. 3-18: Measured (data) and simulated (model) V_{DS} and V_{GS} at 300V/15A with $L_m=1\text{nH}$

More comparisons are found in **Fig. 3-19** (300V) and **Fig. 3-20** (150V).

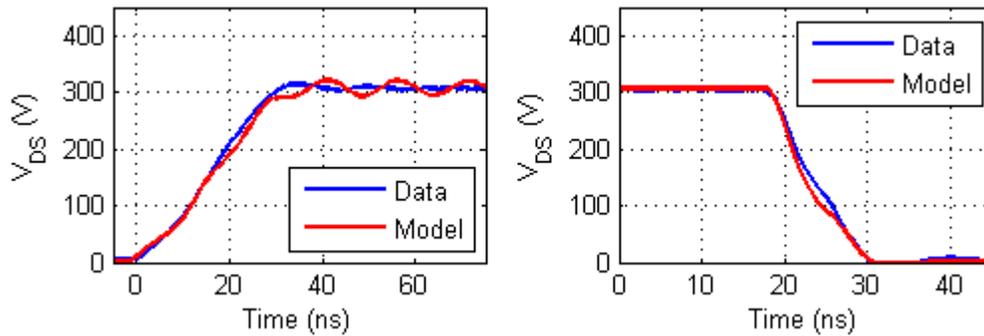
At 300V (**Fig. 3-19**) the V_{DS} variations during the turn-on and turn-off (84MHz oscillation) are coherent in simulation and in measurement; this means a correct modeling of the GaN HEMT at room temperature and of the main parasitic inductances including L_m .



(a) 300V / 15A



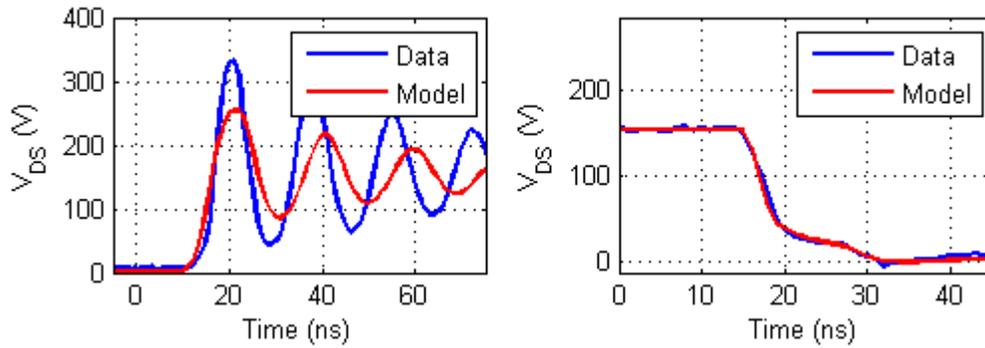
(b) 300V / 7A



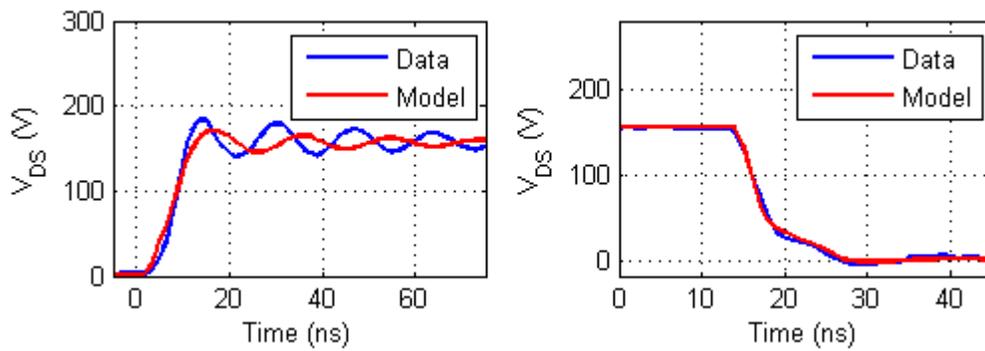
(c) 300V / 3A

Fig. 3-19: Measured (data) and simulated (model) V_{DS} at 300V

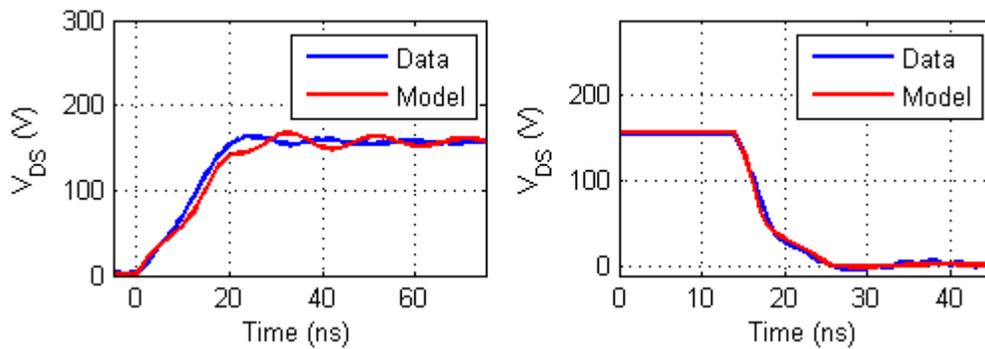
However, at 150V (**Fig. 3-20**), the simulated voltage V_{DS} 's oscillation is not well matched with the measured one; this means that the C_{OSS} capacitance's model at low voltage around 150V is lack of precision.



(a) 150V / 15A



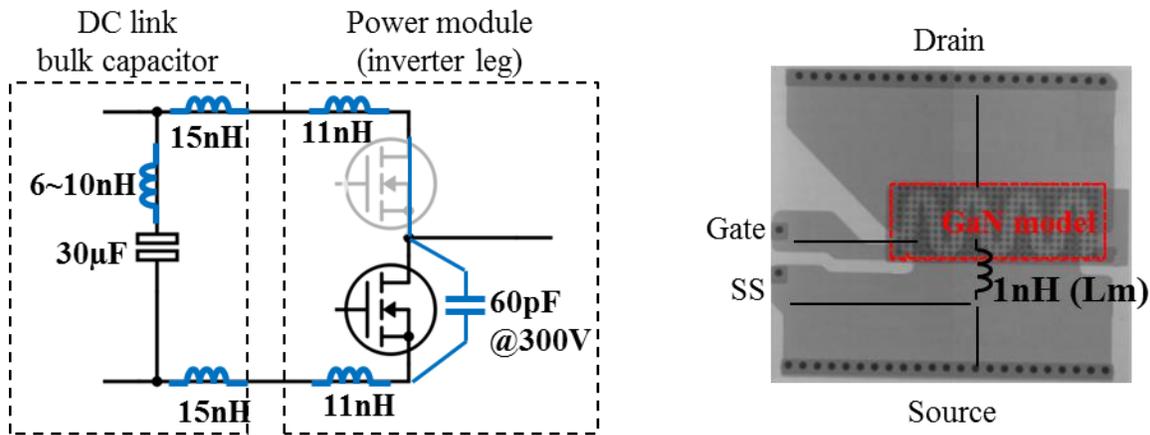
(b) 150V / 7A



(c) 150V / 3A

Fig. 3-20: Measured (data) and simulated (model) V_{DS} at 150V

Fig. 3-21 illustrates the relevant parasitic elements forming the switching waveforms. The parasitic inductances and capacitance in **Fig. 3-21a** lead to the 84MHz oscillation which is observed in **Fig. 3-19** ($V_{DS}=300V$). The tiny 1nH of L_m inductance in common between the power loop and the gate one, results in significant effect in V_{DS} 's falling edge, as shown in **Fig. 3-18**.



(a) Power loop parasitic elements resulting in V_{DS} oscillation (b) Common parasitic inductance between the power loop and the gate loop

Fig. 3-21: Parasitic elements forming switching waveforms

3.2.2 Permanent switching test

The GaN_{SW} switches at 300V, 100kHz with a duty circle of 0.5. Therefore the average load current is about 3A as shown in **Fig. 3-22**.

The two GaN HEMTs are measured at 60°C (GaN_{SW}) and at 80°C (GaN_{SYN}). Setting the temperature input of the GaN HEMT model equaling to the measured data (60°C for GaN_{SW} and 80°C for GaN_{SYN}) and comparing the measured and simulated V_{DS} , the results are shown in **Fig. 3-23**. The V_{DS} variations in permanent switching have been correctly predicted as in double pulse test.

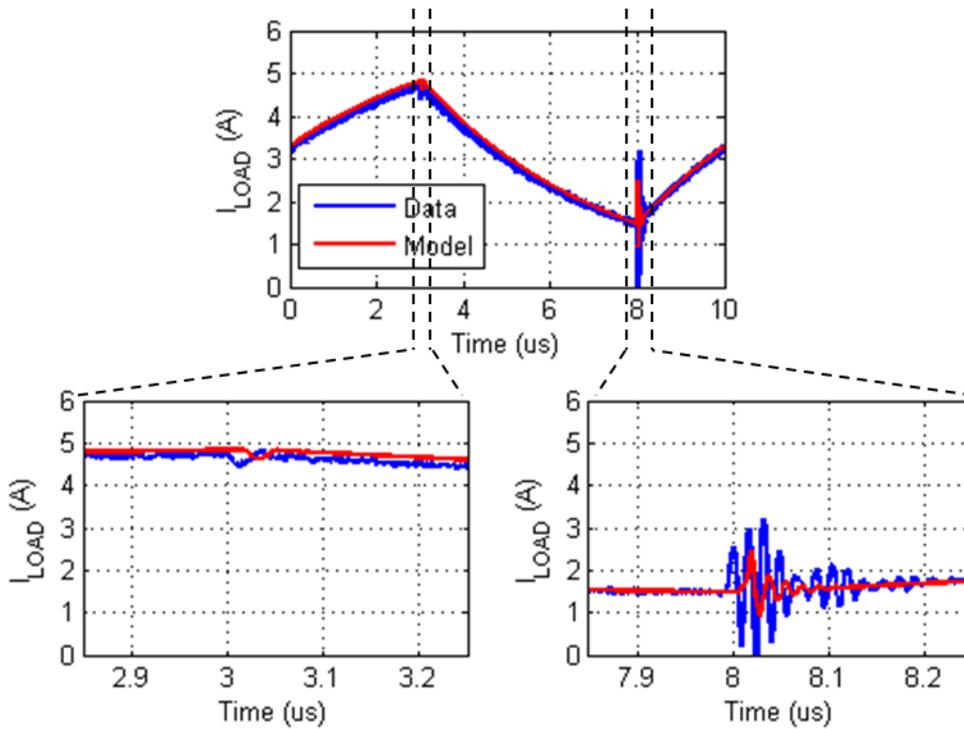


Fig. 3-22: Measured (data) and simulated (model) load current

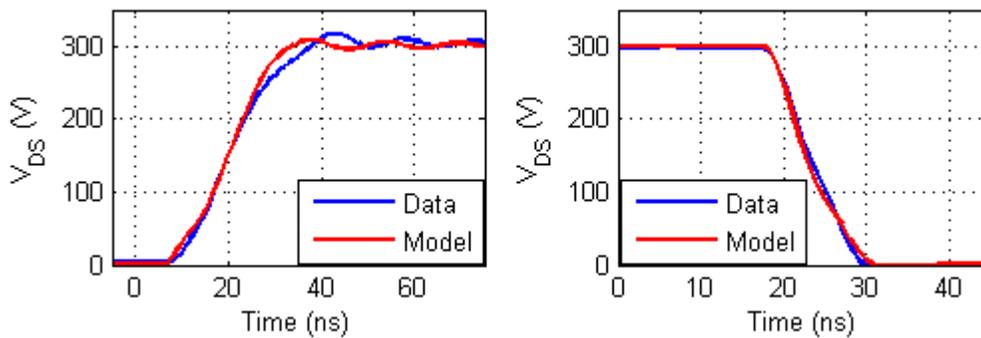


Fig. 3-23: Measured (data) and simulated (model) V_{DS} at 300V, 0.5 duty circle and 100kHz, 60°C for GaN_{SW} and 80°C for GaN_{SYN}

Since the V_{DS} variation at 300V 3A has already been validated at room temperature in double pulse test. **Fig. 3-24** shows the comparison between the simulated switching V_{DS} at room temperature and at 80°C.

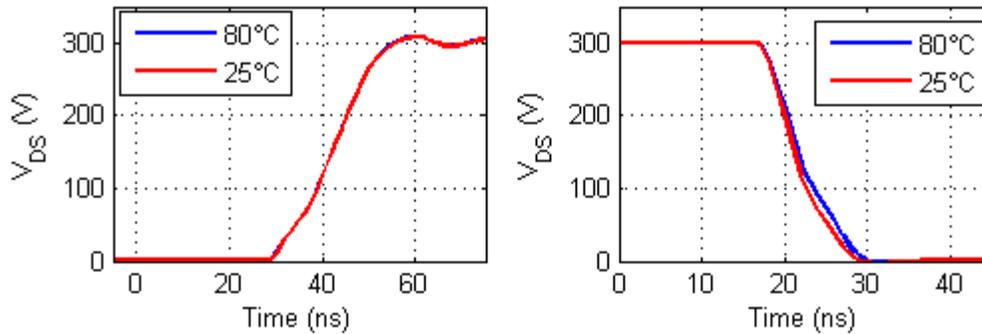


Fig. 3-24: Simulated V_{DS} transients at different temperature

Only a tiny difference is observed in turn-on transient. Unlike traditional Si MOSFET with temperature dependent reverse current characteristics, GaN HEMT has zero reverse recovery charge. Therefore the only temperature dependent element which might change the switching voltage transient is the trans-conductance of the transistor. However, this element does not modify significantly the voltage transient and thus has ignorable effects sur the EMI noise sources.

3.3 Switching with in-module C_X capacitors

The high voltage overshoot during oscillation (e.g. in **Fig. 3-19a**) induced by the large power loop inductance is intolerable. It increases the switching loss and degrades the device reliability. Low profile low ESL ceramic capacitor, being placed as close as possible to the fast switching WBG power semiconductor devices, becomes mandatory for the purpose of minimizing the voltage overshoot. The C_X capacitors, as discussed in 2.3.3.1, are used to minimize this V_{DS} overshoot.

3.3.1 Permanent switching test

Compared with the power loop in bare module (**Fig. 3-25a**), the one with in-module C_X capacitors is presented in **Fig. 3-25b**. The voltage V_{DS} of the low-side GaN HEMT starts to oscillate only after surpassing the DC voltage, then the high-side GaN HEMT is reversely conducting. Therefore the high-side GaN HEMT is short-circuited in the power loop analysis. It should be noted that the circuit model in **Fig. 3-25b** is different from the one in **Fig. 2-39** (c.f. 2.3.3.1): this model has been simplified by combing three C_X capacitors as one. In reality as the

three capacitors in parallel are soldered together, the three capacitors' total impedance acts just as one capacitor.

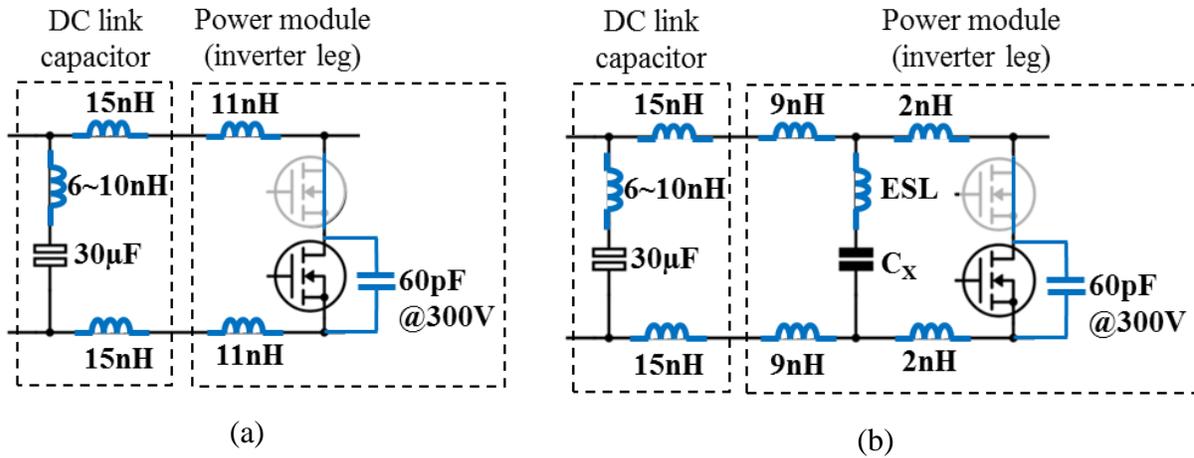
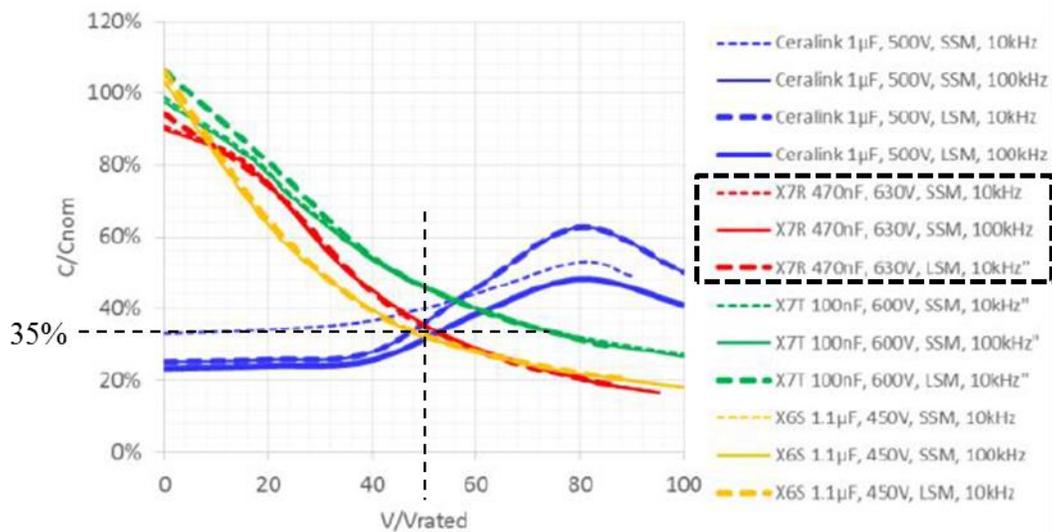
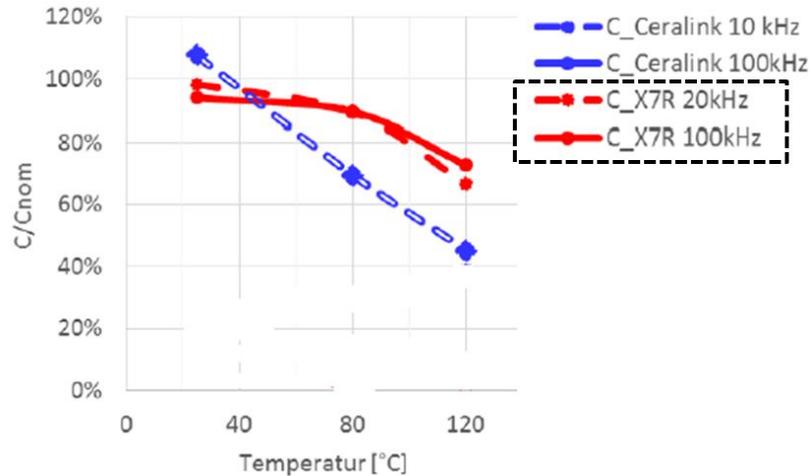


Fig. 3-25: Power loops in bare module (a) and in module with C_x capacitors (b)

The 300V/3A permanent switching is tested as in 3.2.2 with three C_x capacitors rated 150nF/630V each (450nF in total). As using the MLCC capacitors, a well-known issue is that its capacitance value decreases with the voltage bias due to a degradation of the permeability. The higher the capacitance value is, the more significant this effect is. The voltage dependent capacitance's evolutions for a bunch of MLCC capacitors are shown in **Fig. 3-26a**.



(a)



(b)

Fig. 3-26: Voltage (a) and temperature (b) dependency of capacitance value for different ceramic capacitors' technologies [Klein 17]

From the voltage dependencies in **Fig. 3-26a**, the used C_X capacitors' value is estimated as 35% of its nominated value (150nF) as applying the voltage bias 50% (300V) of its rated one (630V), which is around 50nF.

Besides the voltage, the capacitance value drops further with the temperature (**Fig. 3-26b**).

The measured and simulated V_{DS} (300V/3A) results are shown in **Fig. 3-27**. Besides the obvious V_{DS} overshoot decreasing (from 23V to 15V), it is observed that an evident low frequency (~ 2 MHz) oscillation has occurred. There is a small difference between the measured voltage overshoot and the simulated one; this may be due to that the high-frequency (over 300MHz) oscillation is close to the limit of the voltage probe (500MHz). The turn-on and turn-off V_{DS} variations are correctly matched and this is essential for predicting the EMI noises.

3.3.2 Analysis of the voltage V_{DS} 's oscillations at turn-off

The circuit model in **Fig. 3-25b** can be simplified as shown in **Fig. 3-28a**. The ESL of the DC link capacitor (6~10nH) is replaced by its average value 8nH. The ESL (0.5nH/3) of C_X can be distributed into the left and right part of the circuit. L_X is the parasitic inductance due to the power loop formed by the two GaN HEMTs and the nearby in-module C_X capacitors. L_{DC} is the parasitic inductance due to the DC bus and the bulk capacitor's ESL.

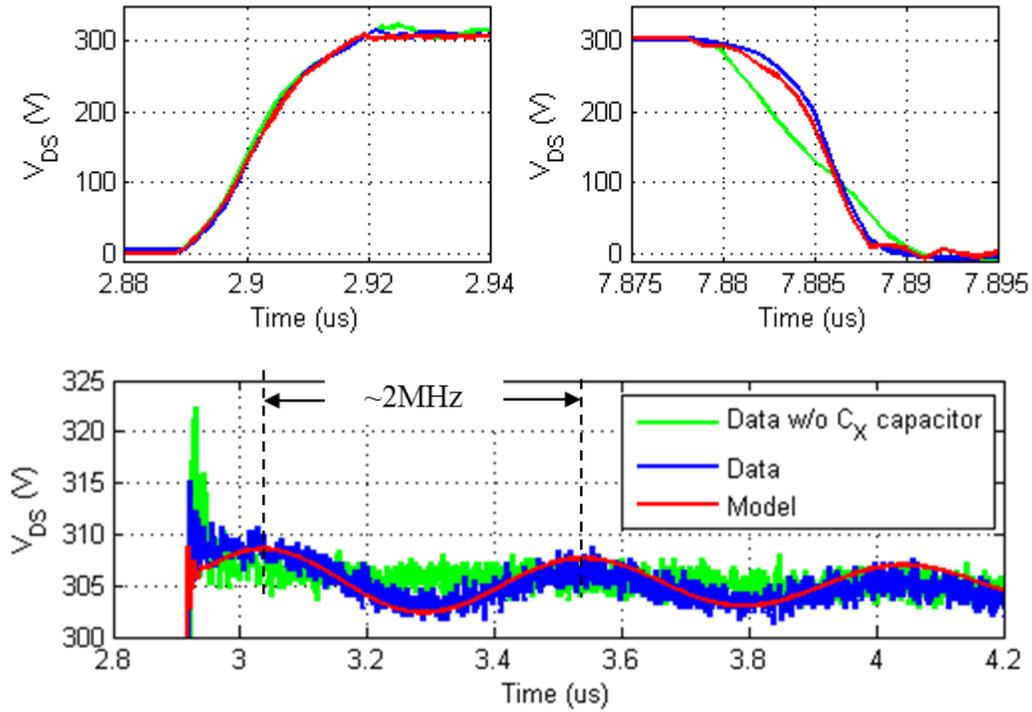


Fig. 3-27: Measured (data) and simulated (model) V_{DS} with in module C_X capacitors

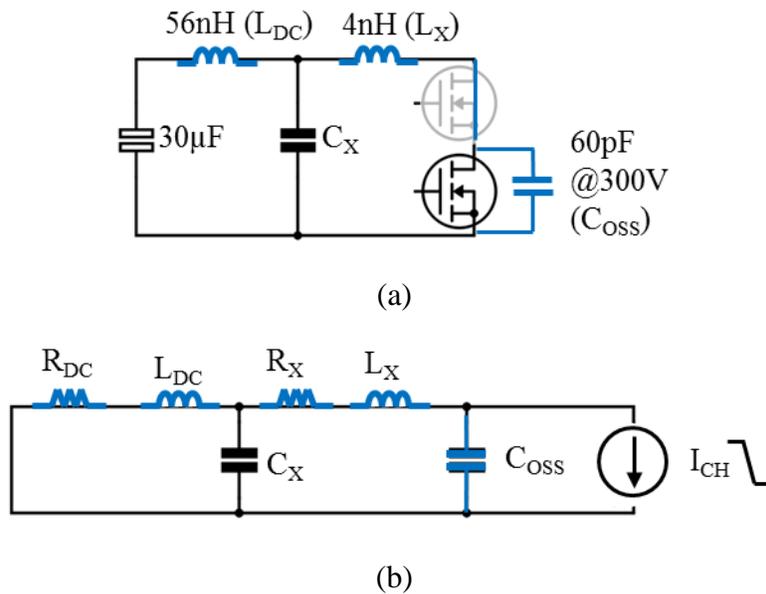


Fig. 3-28: Simplified power loop circuit (a) and the oscillation origin (b)

In small signal analysis, the $30\mu\text{F}$ capacitance is treated as a short-circuit. The low-side GaN HEMT is replaced as a step down current source I_{CH} representing the current drop during the turn-off transient. **Fig. 3-28b** shows the small signal model of the simplified power loop, completed by the resistive elements: R_{X} is constituted by the equivalent resistance when the high-side GaN HEMT is in reverse conduction and the ESR of the C_{X} capacitors; R_{DC} is mainly constituted by the ESR of the bulk capacitor and the relevant parasitic resistances in the DC bus.

Since $C_{\text{X}} \gg C_{\text{OSS}}$, C_{X} could be treated as short-circuit in front of C_{OSS} and C_{OSS} could be treated as an open-circuit regarding to C_{X} . Therefore, the V_{DS} , voltage across the C_{OSS} , oscillates at frequencies of two paralleled LC resonances formed by $L_{\text{X}} // C_{\text{OSS}}$ and by $L_{\text{DC}} // C_{\text{X}}$. These two oscillations are observed in simulated voltage V_{DS} waveforms, as shown in **Fig. 3-29** with different C_{X} values (10nF and 100nF) at 300V/10A.

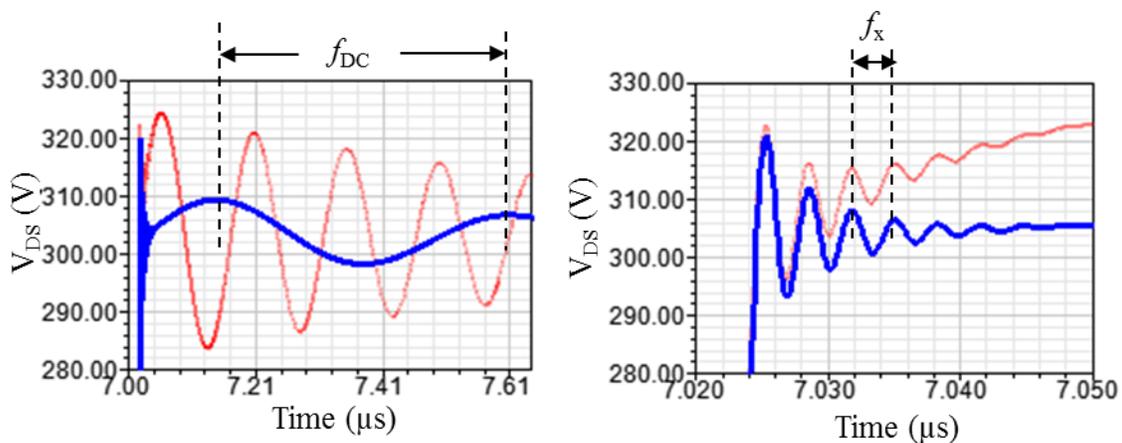


Fig. 3-29: Simulated V_{DS} oscillations at 300V/15A with $C_{\text{X}} = 10\text{nF}$ (red) and 100nF (blue)

f_{DC} and f_{X} are respectively oscillation frequency of $L_{\text{DC}} // C_{\text{X}}$ and $L_{\text{X}} // C_{\text{OSS}}$. For either 10nF or 100nF C_{X} capacitance, f_{X} is calculated as 333MHz. As with 10nF of C_{X} capacitance, f_{DC} is 6.8MHz; as with 100nF of C_{X} capacitance, f_{DC} is 2.2MHz. All these resonance frequencies' calculations are coherent with the L_{DC} , C_{X} and C_{OSS} values.

It is stated in previous study [Liu 07] that making one oscillation frequency ($L_{\text{X}} // C_{\text{OSS}}$) significantly higher than the other ($L_{\text{DC}} // C_{\text{X}}$) will assure a minimum V_{DS} overshoot. However, in both cases shown in **Fig. 3-29**, f_{X} is significantly higher (more than ten times) than f_{DC} , which is why the first peak value of V_{DS} is determined only by the high-frequency oscillation (due to

L_X and C_{OSS}). However, when C_X 's value is as low as 10nF, the low frequency oscillation's (due to L_{DC} and C_X) magnitude is even higher than the high-frequency one. Therefore, C_X 's value should be high enough to make the peak value of the low-frequency oscillation lower than the peak value of the high-frequency one. It is obvious that the higher is L_{DC} the higher in need is C_X since the damping factor is proportional to $\sqrt{C_X / L_{DC}}$.

With traditional slow switching power semiconductor device such as IGBT, the voltage overshoot can be approximated with **Eq 3-7** [Semikron 08].

$$\Delta V_{DS} = L_X \cdot \frac{\Delta I_{DS}}{\Delta T_F} \quad \text{Eq 3-7}$$

This is true in slow switching (up to hundreds of ns) as shown in **Fig. 3-30a**. The L_X is increased exaggeratedly to over 40nH and R_{G_OFF} is set to 500 Ω to significantly slow down the current cutoff. In this case, it is observed that the main current drop occurs quasi linearly right after the voltage V_{DS} reaches its DC value (300V); the voltage V_{DS} starts to fall after the current I_{DS} turning to zero. The measured $L_X \cdot \Delta I_{DS} / \Delta T_F$ (40nH \times 10A/34ns=12V) is close to the measured ΔV_{DS} (15V).

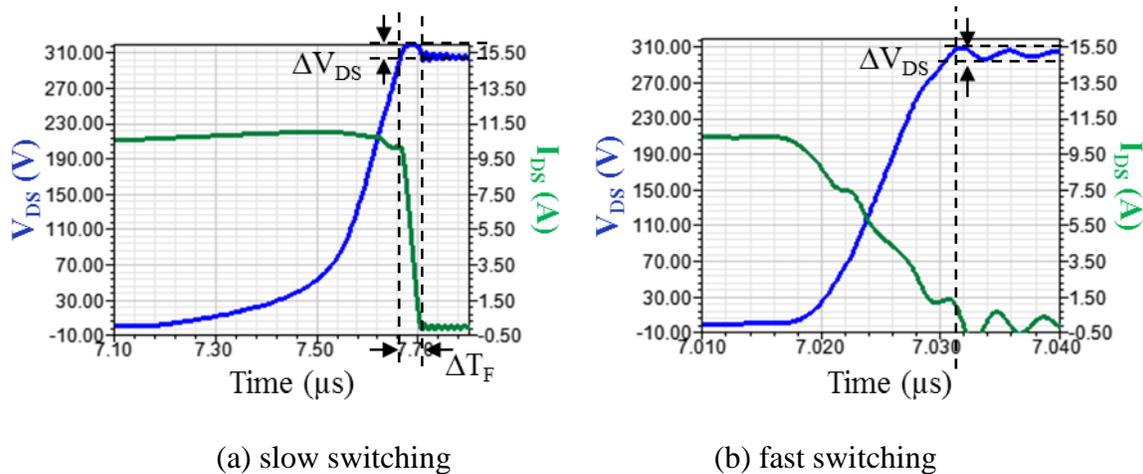


Fig. 3-30: Simulated switching waveforms

However, in fast switching GaN device, current drops simultaneously with the voltage rising happen within 10ns. The mechanism can no longer be explained as in **Eq 3-7**. As shown in **Fig. 3-30b**, even before the voltage V_{DS} reaching its DC voltage the current I_{DS} has already

fallen to zero. Therefore, it is difficult to describe this transient by a simple analytic equation as Eq 3-7.

3.3.3 Parametric analysis of the voltage V_{DS} 's overshoot

From the discussion in the last section, it can be concluded that V_{DS} overshoot is determined by L_{DC} , L_X , C_X , C_{OSS} and the I_{CH} drop. It is noted that I_{CH} drop slew rate is determined mainly by the turn-off gate resistance (R_{G_OFF}). Therefore, in a fixed design, e.g. in this dissertation $L_{DC}=56\text{nH}/L_X=4\text{nH}/C_{OSS}=60\text{pF}/R_{G_OFF}=1\Omega$, the V_{DS} overshoot decreases with the increasing C_X . In order to study this evolution, simulations with the complete model are executed with different C_X values in 400V/20A (**Fig. 3-31**).

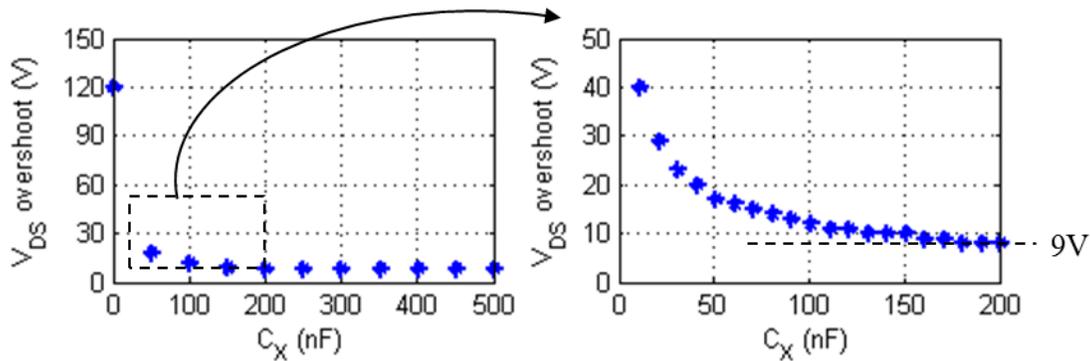


Fig. 3-31: V_{DS} overshoot vs C_X in 400V/20A

It is observed that for C_X around 150nF assures the minimum V_{DS} overshoot of 9V; above this C_X capacitance value, no further V_{DS} overshoot reduction is observed.

More V_{DS} overshoot evolutions with C_X capacitance in different conditions ($L_{DC}/L_X/C_{OSS}/R_{G_OFF}$) are shown in **Fig. 3-32**.

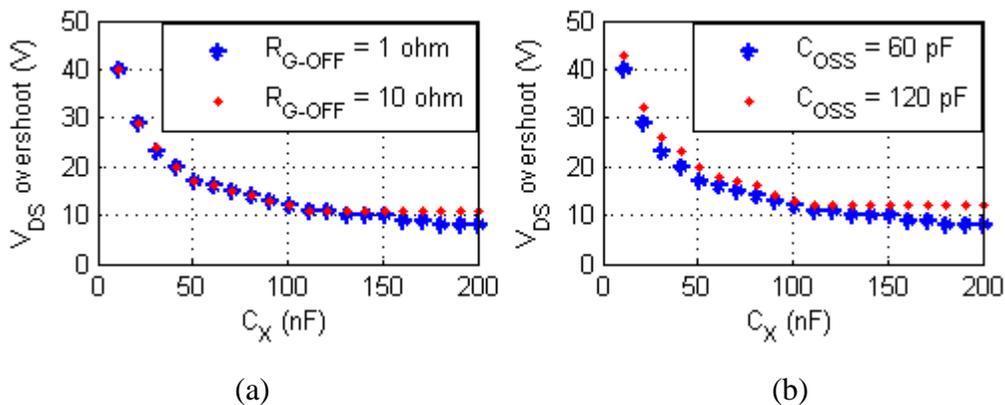
R_{G_OFF} is supposed to be minimized in order to avoid CdV/dt turn-on when the gate turn-off voltage is close to its threshold. A resistance of 10Ω is taken as an exaggerate example to show R_{G_OFF} 's impact on V_{DS} overshoot (**Fig. 3-32a**). It is observed that $R_{G_OFF}=10\Omega$, compared to $R_{G_OFF}=1\Omega$, increases the minimum V_{DS} overshoot from 9V to 11V; besides, the C_X capacitance in need to assure this V_{DS} minimum overshoot decreases from around 150nF to 100nF.

C_{OSS} is intrinsic capacitance of the power semiconductor device. However, in some design (e.g. Gen3 module) the module layout might double the C_{OSS} value by paralleling a stray capacitance. **Fig. 3-32b** shows that two times higher C_{OSS} value increases the minimum V_{DS} overshoot value from 9V to 12V. However, the C_X value in need to maintain this minimum V_{DS} overshoot has been decreased from 150nF to 100nF.

L_X is a critical element for HF oscillation peak which is also the minimum V_{DS} overshoot as discussed previously. In fact the V_{DS} overshoot is somehow proportional to the value of L_X as long as the switching current slew rate is given. This is the reason why the minimum V_{DS} overshoot has been increased from 9V to 16V as increasing L_X value from 4nH to 8nH (**Fig. 3-32c**). However, as decreasing L_X value from 4nH to 2nH, no further minimum V_{DS} overshoot decreasing is ever found.

L_{DC} value can be decreased from a rough design (56nH) to an improved one (e.g. 26nH) by using low ESL capacitor and optimized DC busbar connection. **Fig. 3-32d** shows that different L_{DC} leads to the same minimum V_{DS} overshoot. However, the C_X capacitance in need to maintain this minimum V_{DS} overshoot has been decreased. This can be explained by the resonating energy between C_X and L_{DC} ($C_X \cdot \Delta V_{DS}^2 = L_{DC} \cdot \Delta I^2$): the higher the L_{DC} is, the larger C_X is needed to maintain the same V_{DS} overshoot (ΔV_{DS}).

The load current value, I_{LOAD} , is also an element influencing the V_{DS} overshoot. Its influence is similar to L_{DC} which means that different I_{LOAD} leads to the same minimum V_{DS} overshoot but the C_X capacitance needed to maintain this minimum V_{DS} overshoot is decreased (**Fig. 3-32e**).



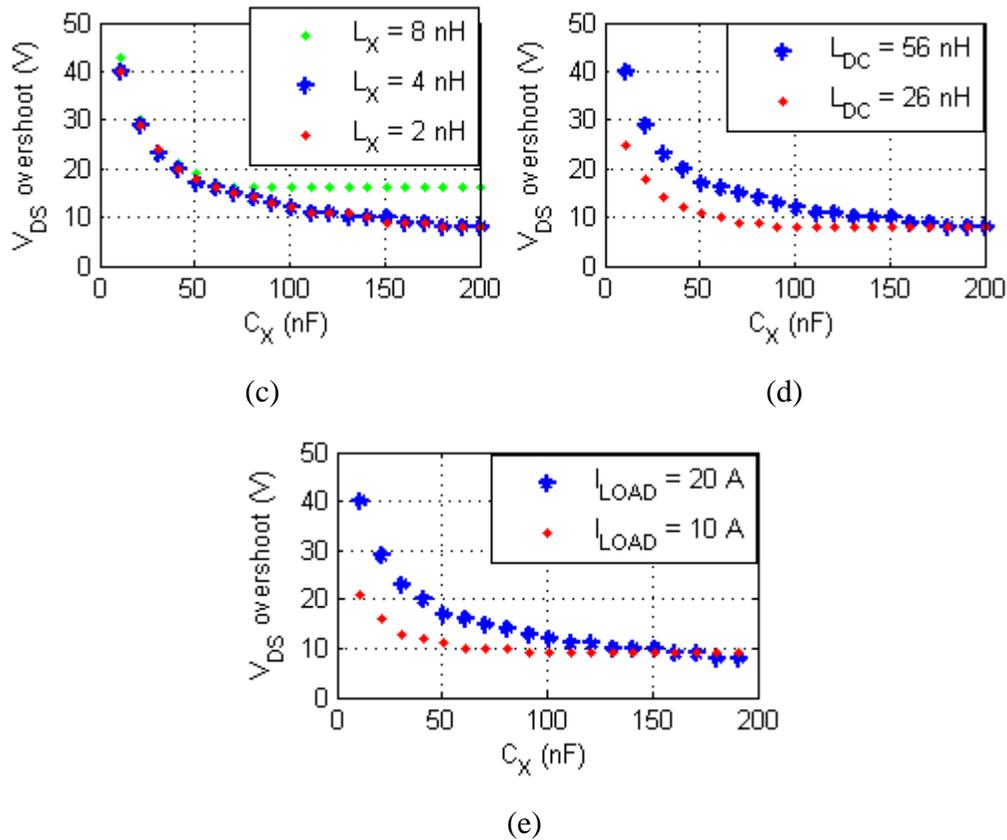


Fig. 3-32: Simulated V_{DS} overshoot vs C_X in 400V/20A with different R_{G_OFF} (a), C_{OSS} (b), L_X (c), L_{DC} (d) and I_{LOAD} (e)

3.4 Conclusions

In this chapter, the models of the GaN HEMT and the power module developed in the two previous chapters have been verified to predict the switching waveforms, which is essential for the switching loss estimation and EMI noises sources.

In the experimental part, the test setup has been presented and modeled. The precautions for voltage and current measurement have been discussed.

Double pulse and permanent switching test have been executed and the measured switching waveforms' are well matched with the simulated ones.

Finally the switching voltage's oscillation under the use of the in-module capacitor has been discussed. The methodology to find the capacitor's value to minimize the switching voltage overshoot under different parasitic elements has been given.

CHAPTER 4

EMI ANALYSIS & MITIGATION TECHNIQUES

After the modeling of the GaN power device and the power module in the chapters one and two, the full aforementioned model package is verified with the switching waveforms in experimental tests in chapter three. Based on the developed model, the in-module C_X capacitor minimizing the switching voltage overshoot has been discussed.

In this chapter, the developed model package will be challenged in conducted electromagnetic interference (EMI) test, in forms of common mode (CM) and differential mode (DM) currents measurements. This allows the verification of all the relevant parasitic elements which constitute the EMI noises' propagation paths in both DM and CM as well as the mode transformation.

The test setup including the measurement methods and equipment are presented, including the line-impedance-stabilized-network (LISN)'s modeling. Then the EMI measurement on bare power module with different resistor-inductor load connection configurations is discussed and compared with the model. The EMI noises are also characterized on power module with in-module capacitors by measurement and simulation. Finally, based on the developed model, the effects and value recommendations of the in-module capacitors are presented by simulated study.

4.1 Test setup

In a typical conducted EMI test setup, two Line-Impedance-Stabilization-Networks (LISN), each being connected between a DC power line and the ground potential, are inserted between the DC voltage source (V_{DC}) and the device under test (DUT) which is constituted by the DC link capacitor, an inverter leg and the resistor-inductor load as shown in **Fig. 4-1**.

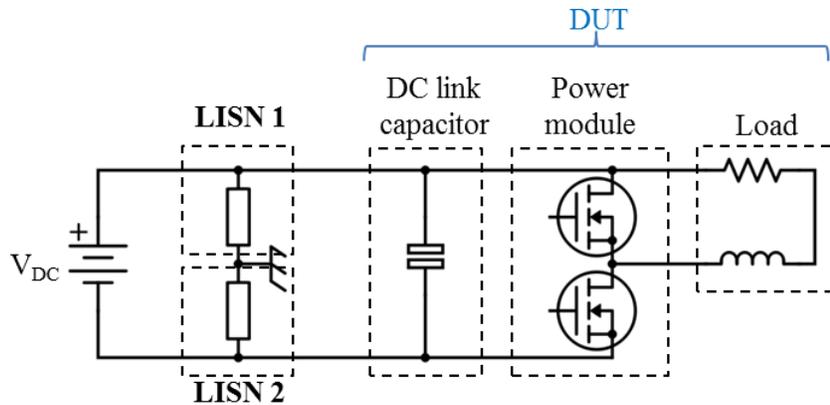


Fig. 4-1: EMI measurement with LISNs

A LISN is a device used for standard or pre-compliance conducted EMI emission test. It has two basic functionalities: 1) isolating of the RF noise from the power source and 2) providing precise impedance (50Ω) to the input of the DUT in relevant frequency range in order to get a repeatable conducted emission measurement. In this dissertation, two identical LISNs (ref 9403-5-BP-10-BNC) from Solar Electronics are used (**Fig. 4-2a**).

4.1.1 LISN modeling

A LISN is basically a two-port network (**Fig. 4-2b**), in which one port (A - G) is connected to the DC voltage source V_{DC} and the other (B - G) is connected to the DUT; in addition, there is a measurement port C - G which will be connected to a 50Ω terminated measurement equipment such as a spectrum analyzer. Basic passive components in a LISN are also shown in **Fig. 4-2b**: Looking into the terminal A, C_1 ($\sim 10\mu\text{F}$, added at the input of LISN) and L_1 ($\sim 5\mu\text{H}$) form a low pass filter in order to isolate the RF noise from the DC power source; Looking into the terminal B, C_2 ($\sim 0.1\mu\text{F}$) is essentially shorted in $150\text{ kHz} \sim 30\text{ MHz}$ while L_1 is nearly an open-circuit, so that the conducted emission pass entirely through the R_0 (50Ω) resistor

of the spectrum analyzer which will be connected via terminal C (BNC adapter) in parallel with an internal isolation resistor R_2 (over $10k\Omega$) of the LISN.

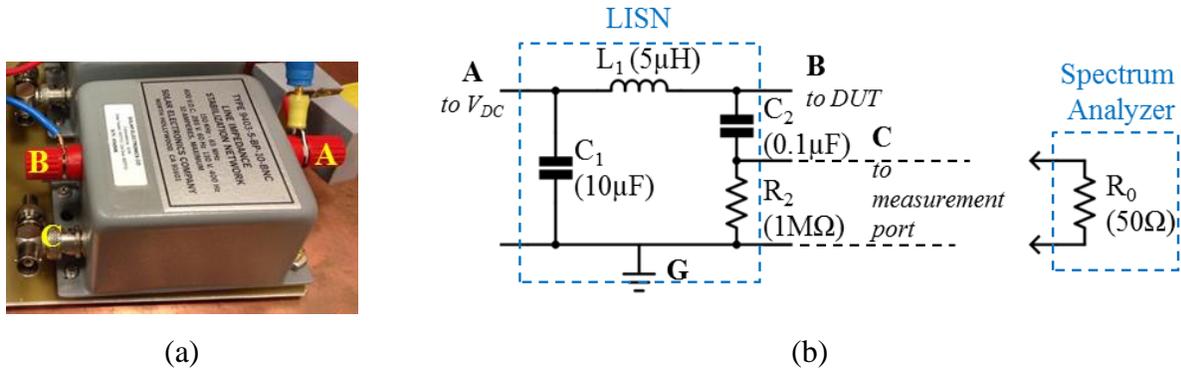


Fig. 4-2: Mono phase LISN (a) and the equivalent circuit (b)

In order to obtain the precise model of this LISN, two impedances are measured: Z_{BG} without and with R_0 (50Ω) terminated, as shown in **Fig. 4-3a** and **Fig. 4-3b**.

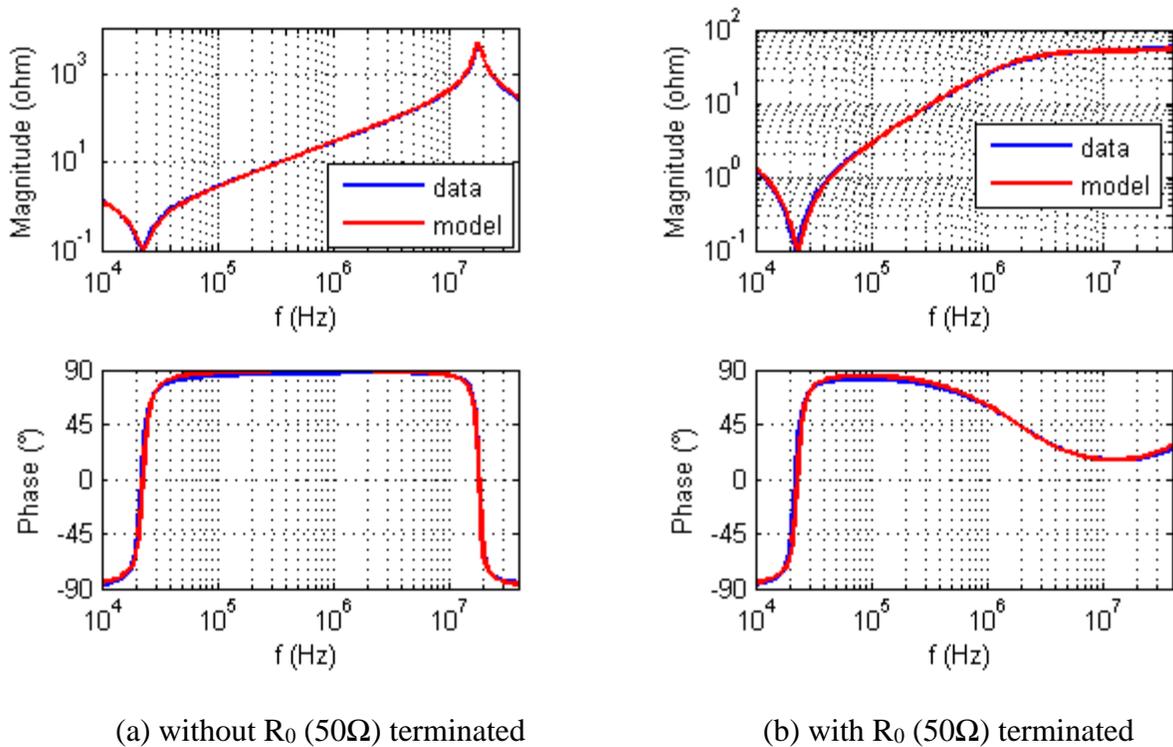


Fig. 4-3: Measured (data) and simulated (model) Z_{BG} impedance

In **Fig. 4-3a**, the values of the filter inductor L_1 and the capacitor C_1 together with an equivalent series resistance (ESR_1) in series can be deduced from the first resonance valley since the series of the capacitor C_2 and the resistor R_2 is essentially open; the second resonance peak quantifies the existence of an equivalent parallel capacitance (EPC_1) and resistance (EPR_1) of L_1 . In **Fig. 4-3b**, the value of the capacitor C_2 and the resistor R_0 can be added in parallel with the aforementioned impedance network. It should be noted that the R_0 is found a little larger than 50Ω ; this is because the extra resistance is due to the equivalent series resistance (ESR_2) of the capacitor C_2 .

The complete model is shown in **Fig. 4-4**. L_2 is the stray inductance of the wire outside the LISN. R_2 is removed since it nearly does not change the value of R_0 . Some stray elements of the components, such as ESL of the capacitors C_1 and C_2 , are ignored since they do not change the total impedance.

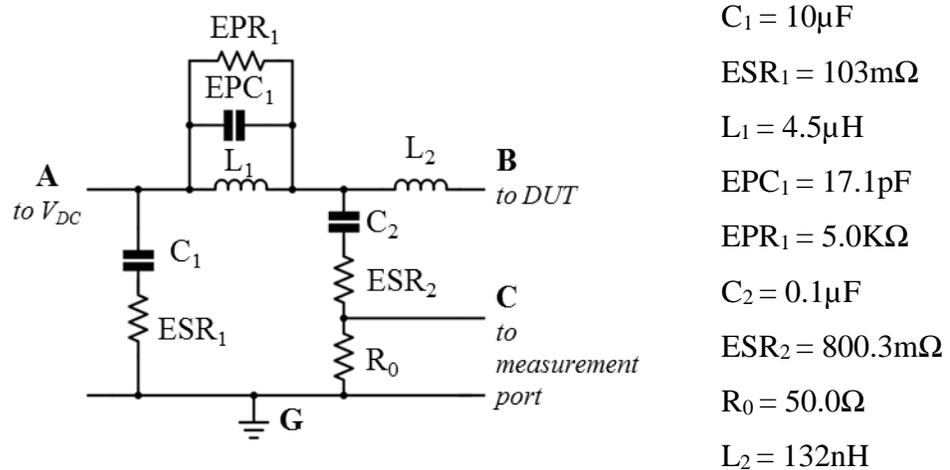


Fig. 4-4: Model of one LISN

In order to verify the modeling of the LISN, the impedance between the C and G with 50Ω (R_0) terminated is measured and compared to the model (**Fig. 4-5**).

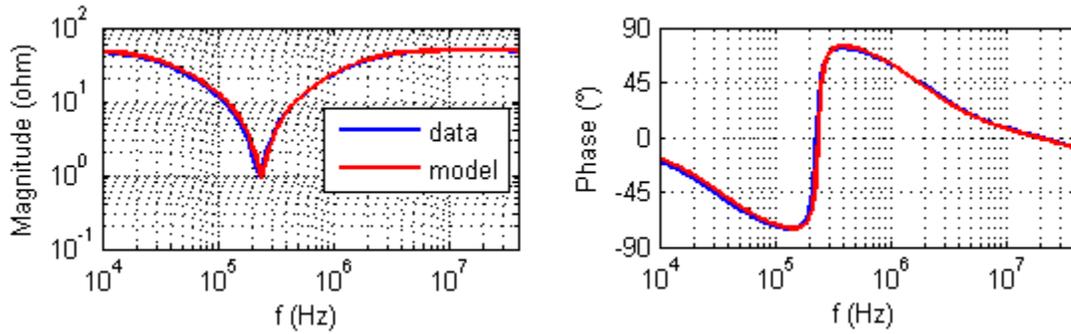


Fig. 4-5: Measured (data) and simulated (model) Z_{CG} impedance with 50Ω terminated

In conducted EMI measurement, current from port B to G (I_{BG}) can be measured by an AC current sensor; this current is the one circuiting in the DC buses. For purpose of EMC normative measurement, the current passing R0 (I_{CG}) is often measured to compare with the EMC standard. The transfer function of I_{BG}/I_{CG} can be deduced with the precise LISN model and is shown in **Fig. 4-6**. Large difference appears until 5MHz; the lower the frequency is, the larger the difference is. This difference is due to the $L_1 + C_1$ sharing current with I_{CG} from the total I_{BG} in low frequency range.

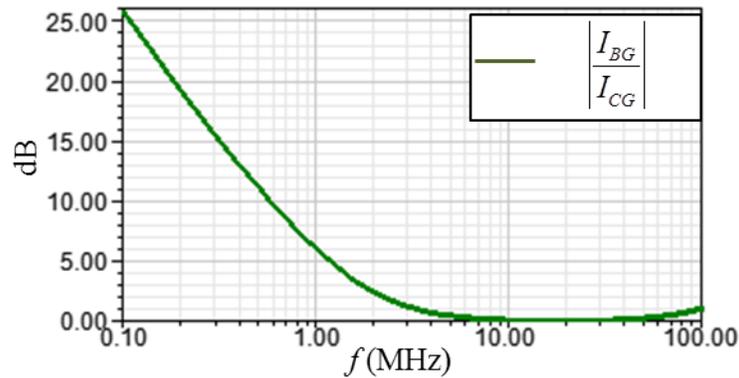


Fig. 4-6: Transfer function of I_{BG}/I_{CG}

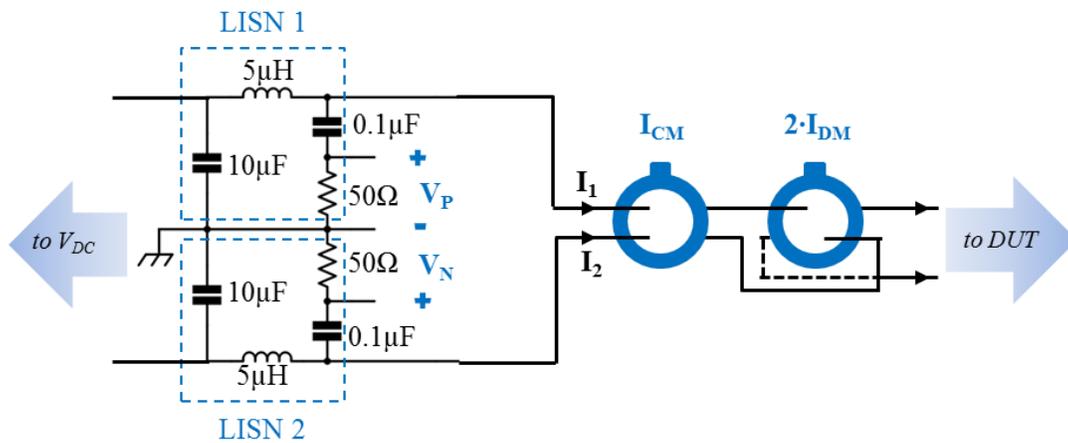
4.1.2 EMI noises measurements

The EMI noises measurements are illustrated with equivalent circuit in **Fig. 4-7a**.

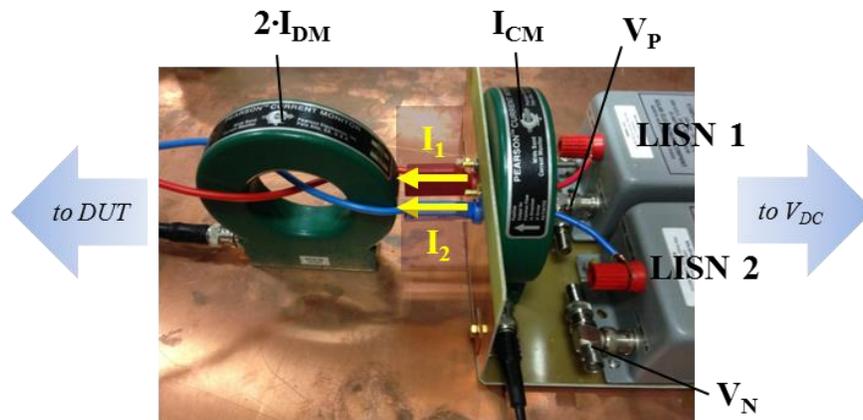
The voltages (noted as V_P and V_N) or currents (noted as I_P and I_N) passing through the 50Ω resistors in parallel with the LISNs are often measured in spectrum and compared with the EMC standard. The equations below define the relations between these voltages and currents.

$$I_P = \frac{V_P}{50} \quad \text{Eq 4-1}$$

$$I_N = \frac{V_N}{50} \quad \text{Eq 4-2}$$



(a)



(b)

Fig. 4-7: EMI noises' measurements: V_P , V_N , I_{CM} and I_{DM}

For EMI filter design purpose, the noise currents are studied in forms of common mode (CM) current I_{CM} and differential mode (DM) one I_{DM} . The I_{CM} and I_{DM} are defined as below with I_1 and I_2 the currents flowing in the DC sides:

$$I_{CM} = I_1 + I_2 \quad \text{Eq 4-3}$$

$$I_{DM} = \frac{I_1 - I_2}{2} \quad \text{Eq 4-4}$$

The voltages V_P , V_N and currents I_{CM} , I_{DM} can be measured directly as shown in **Fig. 4-7b**:

- AC voltages V_P and V_N can be measured by two $\times 10$ passive voltage probes (TPP0200, DC ~ 200MHz);
- AC currents I_{CM} and $2 \cdot I_{DM}$ can be measured by two AC current sensors (Pearson 6595, 100Hz ~ 150MHz as -3dB cutoff frequency, $V/A=0.25$ with 50Ω terminal resistance); it is reasonable to treat the 0dB measurement in a frequency range of 1kHz ~ 30MHz.

It should be noted that in some analytic circuit model for EMI analysis, a LISN is simplified as a single 50Ω resistor thus $I_P=I_1$, $I_N=I_2$. However, as shown in **Fig. 4-7a**, the current I_1 includes not only the current passing 50Ω resistor (I_P) but also the one passing the low-pass filter $5\mu H + 10\mu F$.

4.1.2.1 Common mode current measurement

As discussed previously, there are two ways to measure the CM noise:

- I_{CM} : The one measured directly by an AC current sensor;
- I_P+I_N : The one defined by **Eq 4-1** and **Eq 4-2** where V_P and V_N are measured by passive voltage probes.

Fig. 4-8 shows the comparison of measured CM currents between the two aforementioned approaches. Supposing that the AC current sensor's transfer function in relevant frequency range is always 0dB, the difference between I_{CM} and I_P+I_N up to 5MHz is due to the difference between I_{BG} and I_{CG} (**Fig. 4-6**); above 5MHz, I_{CM} can be treated as equaling I_P+I_N .

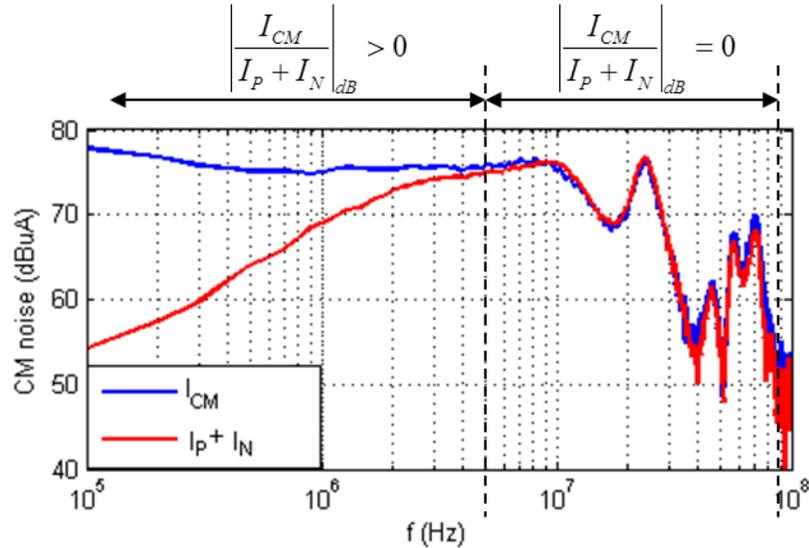


Fig. 4-8: Different approaches of CM noise measurement

4.1.2.2 Differential mode current measurement

As discussed previously, there are two ways to measure the DM noise:

- I_{DM} : The one measured directly by an AC current sensor;
- $I_P - I_N$: The one defined by **Eq 4-1** and **Eq 4-2** where V_P and V_N are measured by passive voltage probes.

Fig. 4-9 shows the comparison of measured DM currents between the two aforementioned approaches. As in CM measurement, the difference between $2 \cdot I_{DM}$ and $I_P - I_N$ up to 5MHz is due to the difference between I_{BG} and I_{CG} (**Fig. 4-6**). Above 5MHz, $2 \cdot I_{DM}$ is supposed to be treated as equaling $I_P - I_N$ according to previous analysis. However, DM currents' magnitude show waveforms just like the CM noise, especially the one measured by the AC current sensor (blue line). This is because the AC current sensor has a very large loop (**Fig. 4-7b**) which will capture the radiated emission induced by CM current in DC power line; it can also be explained as the mode transformation from CM to DM. Even with another current sensor with smaller loop, this error can be reduced but can never be eliminated. Therefore, the most suitable way to evaluate the DM noise is $I_P - I_N$ even though the CM's influence exists still (due to the ground return path of oscilloscope).

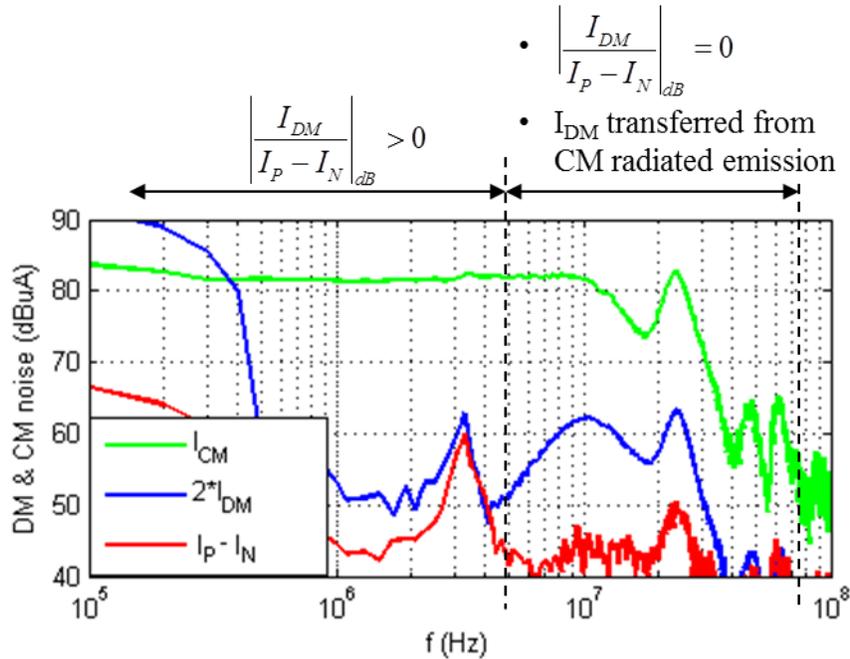


Fig. 4-9: Different approaches of DM noise measurement

4.1.2.3 Data processing

The EMI noises can be captured by oscilloscope in time domain followed by Fast Fourier transformation (FFT) or by a spectrum analyzer in frequency domain. It should be noted that the time domain measurement with a 8-bit oscilloscope results in a dynamic range of $(1/2^8)_{dB}$ thus 48dB in frequency domain. This is far less than the dynamic range of a typical spectrum analyzer which is around 120dB. However, in order to investigate the EMI noise in time and frequency domain at the same time, the latter method is used in this dissertation: FFT with rectangular window is used to process the time domain EMI noise measurement by an oscilloscope or simulation to obtain the corresponding frequency domain EMI noise level. Either in measurement or simulation, only one period of signal in permanent state is acquired and processed with FFT followed by envelop detecting as shown in **Fig. 4-10**. The resolution of the time domain signal is 1point/1ns at $1\mu s$'s switching period and thus the 500MHz in frequency domain.

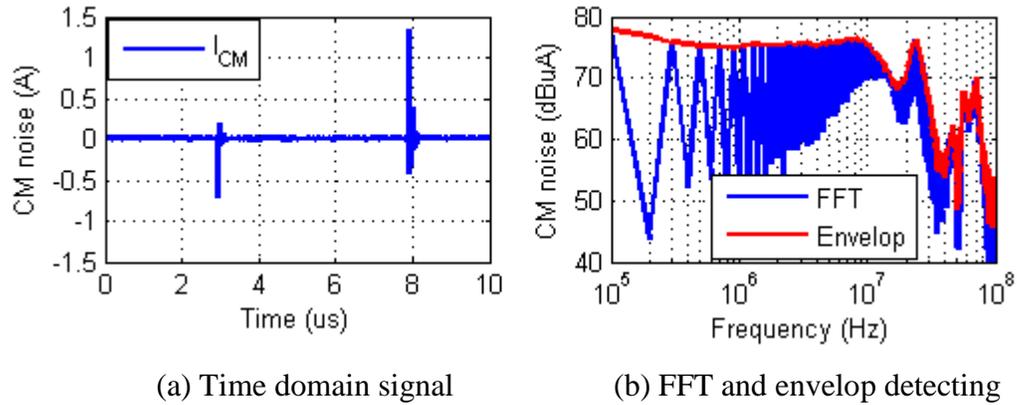


Fig. 4-10: Data processing example

4.1.3 Experimental setup

The experimental setup is presented in **Fig. 4-11**. The LISN, power module (including DC link capacitor) and load are grounded at the copper plate beneath (GND).

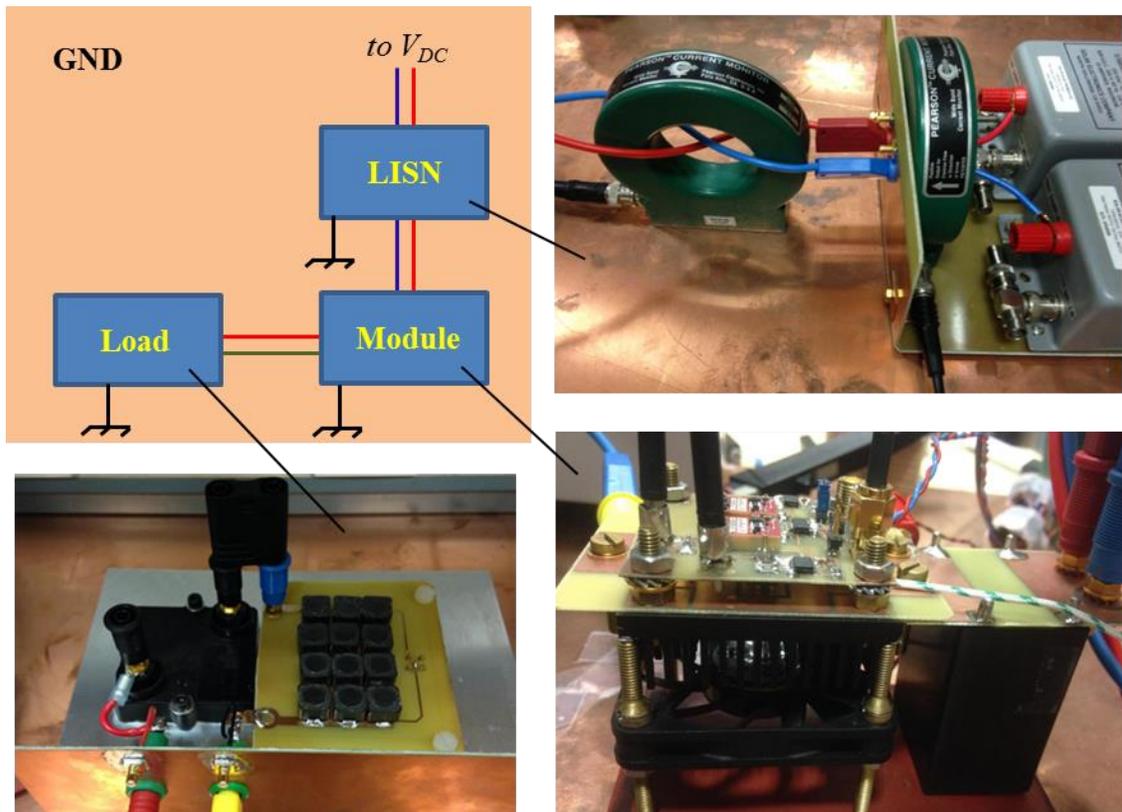


Fig. 4-11: Experimental setup (300V, 100kHz, $\alpha=0.5$) for EMI analysis

The switching condition of the power module is set to 300V, 100kHz with duty circle as 0.5. This choice is a compromise of the module's thermal dissipation ability. It should be noted that as the EMI noises are being measured, no other voltage monitoring probes should be presented. This is for the purpose of restricting the complexity of several ground potential which will couple CM noise in measurement of others. The EMI noises will be measured and analyzed with the bare power module at first and then with in-module capacitors of different values.

The full simulation circuit is shown in **Fig. 4-12**. The different model blocks have been developed respectively in 4.1.1 (LISN), 2.3.1 (DC link capacitor), 2.3.2 & 2.3.4 (Power module + Gate driver) and 3.1.1 (load). The inductances between different blocks are the estimated wire parasitics. It should be noted that the ground return parasitic inductances from the module (L_{Module}) and the load (L_{Load}) are treated differently since physically the distance between the power module and the ground connection of the LISNs is much closer than the other thus $L_{Module} < L_{LOAD}$. Their values are undetermined and will be discussed in section 4.2.1.

It should be noted that the DC voltage source is not modeled in the full simulation circuit. The simulation can be launched by setting the initial voltage at the C_{BUK} as desired one (~300V).

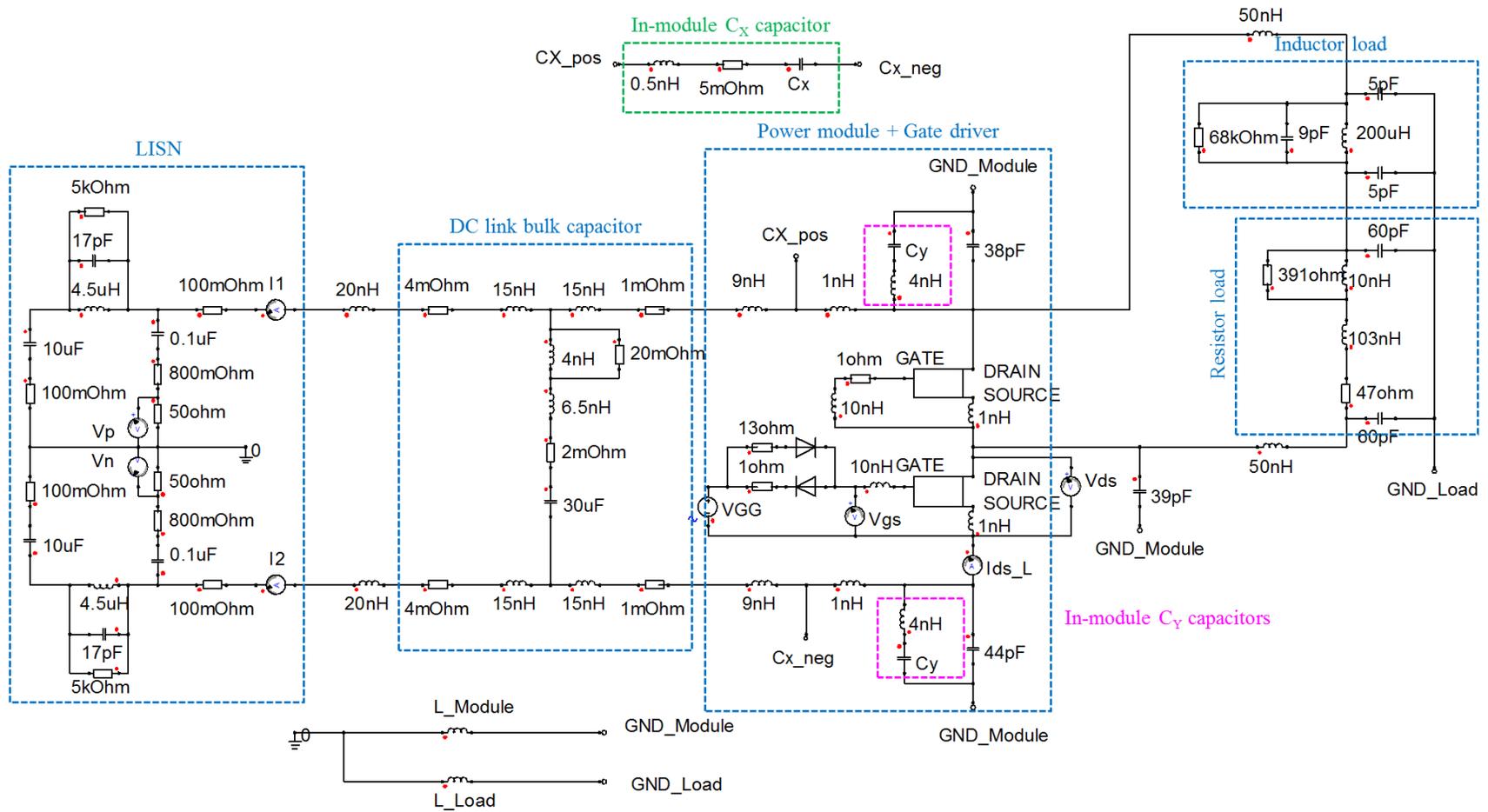


Fig. 4-12: Full simulation circuit for EMI analysis

4.1.4 Influences of different load connecting configurations

The load is constituted by a resistor and an inductor in which the common mode stray capacitance of the resistor is much more significant than the one of the inductor. Therefore, connecting the resistor to the AC terminal or the DC terminal of the power module would make a difference regarding the CM EMI noise propagation path and the noise transformation from one mode to the other. **Fig. 4-13** shows the two load connecting configurations with a bare module – “AC-R” by connecting the resistor load to the AC terminal and “AC-L” by connecting the inductor load to the AC terminal. It should be noted that in the following circuit the GND_{Module} and GND_{Load} are simplified as one GND.

Even though the load in general cases is different from the one used in this dissertation. The imbalanced distribution of the CM capacitances in this load is representative of the general case load which suffers from the same problem.

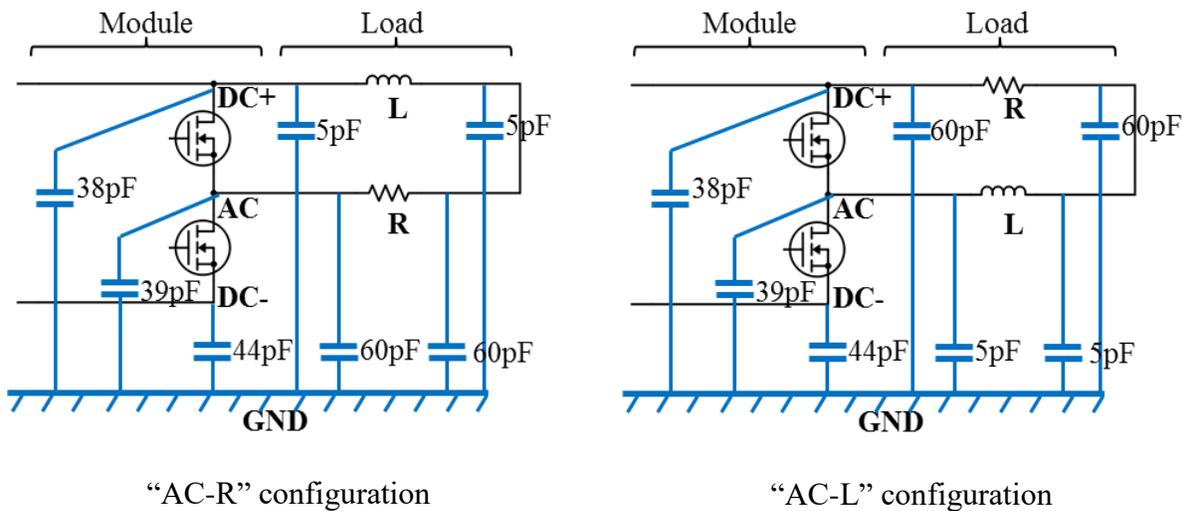


Fig. 4-13: Common mode impedances by connecting RL load in different ways

- The “AC-R” configuration results in more stray capacitance ($60\text{pF}+60\text{pF}+5\text{pF}$) in parallel with the AC-to-GND one (39pF) of the module which means higher CM noise in low frequency; however, the stray capacitances of the two DC sides ($38\text{pF}+5\text{pF}$ in DC+ and 44pF in DC-) are relatively balanced therefore little mode transformation happens.

- In the contrary, “AC-L” configuration introduces less stray capacitance (5pF) to the AC-to-GND one (39pF) of the module which results in lower CM noise in low frequency; however, the stray capacitances of the two DC sides (38pF+60pF+60pF+5pF in DC+ and 44pF in DC-) are quite imbalanced and thus significant mode transformation would occur.

Fig. 4-14a shows the measured CM current I_{CM} and the DM one I_{DM} in both load configurations with the bare power module. It is observed that the currents I_{DM} in both configurations are little different and thus only one I_{DM} is shown in figure. However, the currents I_{CM} are quite different from one load configuration to the other:

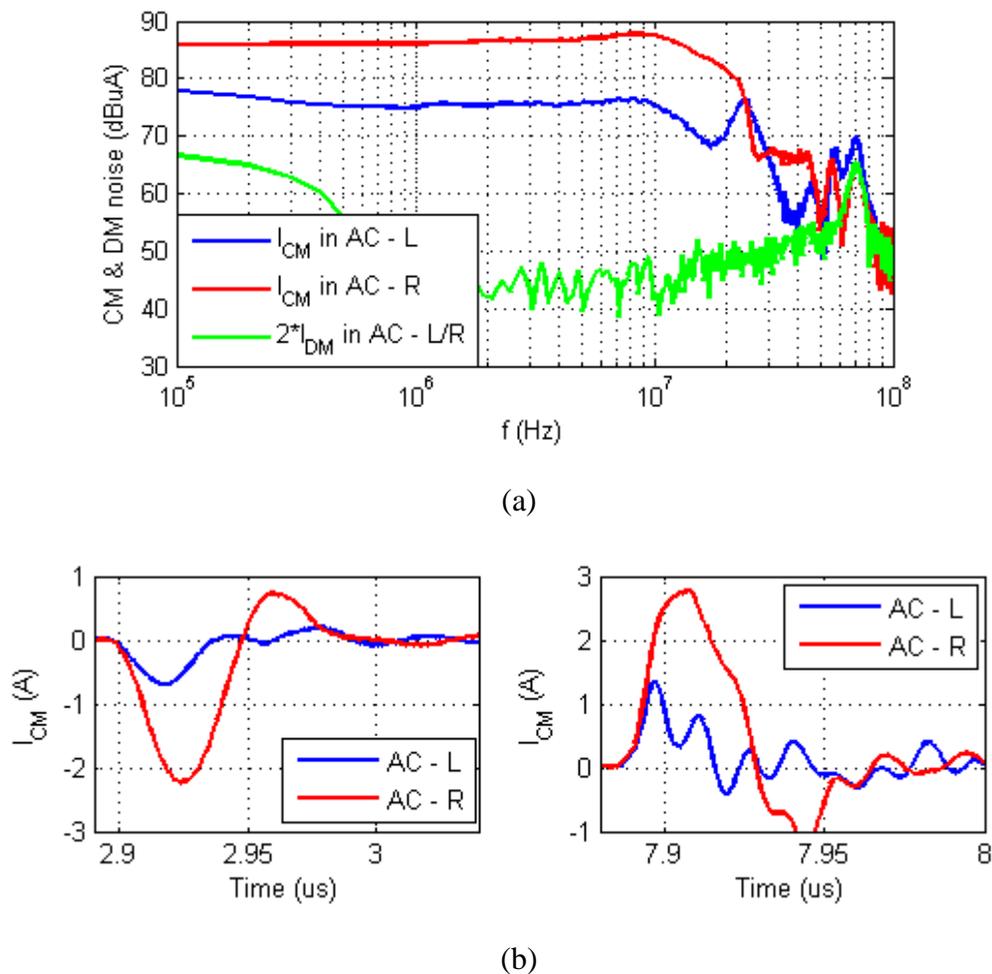


Fig. 4-14: Time (b) and frequency (a) domain comparison of measured I_{CM} and I_{DM} in different load configurations with the bare power module

- The “AC-R” configuration induces much higher magnitude CM current than “AC-L” in time domain (**Fig. 4-14b**) as well as in frequency domain. This verifies the aforementioned common mode impedance analysis. Detail analysis will be given in 4.2;
- In “AC-L” configuration, the global magnitude of CM noise is lower but there is a peak value of I_{CM} at around 25MHz, which is approved to be due to mode transformation from DM noise (analyzed in detail in 0).

Another comparison between the switching voltages V_{DS} in both load configurations are shown in **Fig. 4-15**.

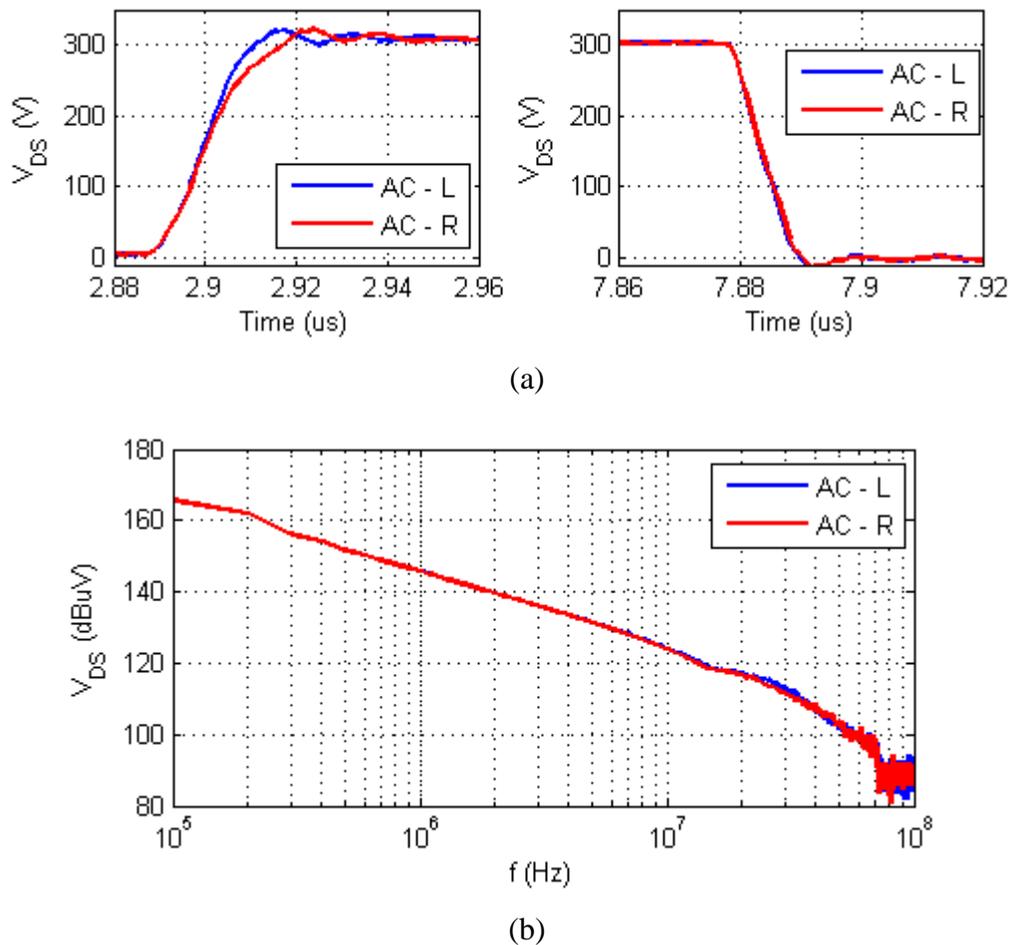


Fig. 4-15: Time (a) and frequency domain (b) comparison of measured V_{DS} in different load configurations

In time domain, “AC-R” configuration slows down slightly the V_{DS} rising edge compared to the “AC-L”, which is due to the large value stray capacitances from the load resistor in parallel with the C_{OSS} of GaN HEMT. This will increase the switching loss apparently. However, in frequency domain this effect does not change anything in V_{DS} 's spectra up to 100MHz, which means that the EMI noise propagation path is the only reason for the I_{CM} 's difference.

4.1.5 Test procedures

The EMI noises in DM and CM are measured with the bare power module as well as the one with in-module capacitors, with resistor load connected to the AC terminal and DC terminal.

The measured results and their analysis are presented sequentially as below:

- 1) CM current (I_{CM}) with resistor load connected to AC terminal, respectively with the bare power module (**Fig. 4-16a**), the module with only C_X capacitor (**Fig. 4-16b**) and with only C_Y capacitor (**Fig. 4-16c**), finally the module with both capacitors (**Fig. 4-16d**); (section 4.2)
- 2) CM current (I_{CM}) with resistor load connected to DC terminal, same procedure as above; (section 4.3)
- 3) DM current (I_{DM}), same procedure as above. (section 4.4)

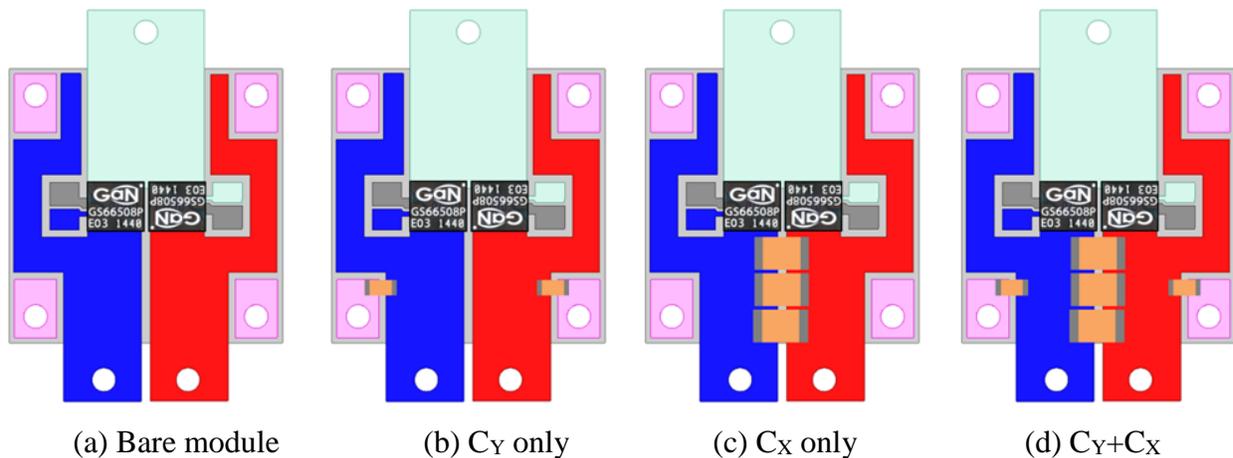


Fig. 4-16: Evaluation procedure for in-module capacitors

4.2 Common mode current I_{CM} with resistor connected to AC terminal

4.2.1 With the bare module

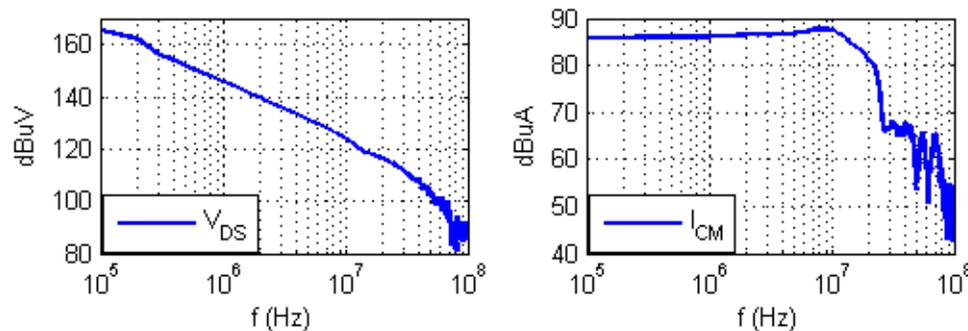
The “AC – R” configuration is studied in this section. As discussed previously, in this configuration the DC sides are relatively balanced and thus little mode transformation should occur. Therefore, the CM current I_{CM} can be considered being generated only by the CM noise source V_{DS} , where Z_{CM} is the CM noise propagation impedance (Eq 4-5 and Eq 4-6).

$$I_{CM}(f) = \frac{V_{DS}(f)}{Z_{CM}(f)} \quad \text{Eq 4-5}$$

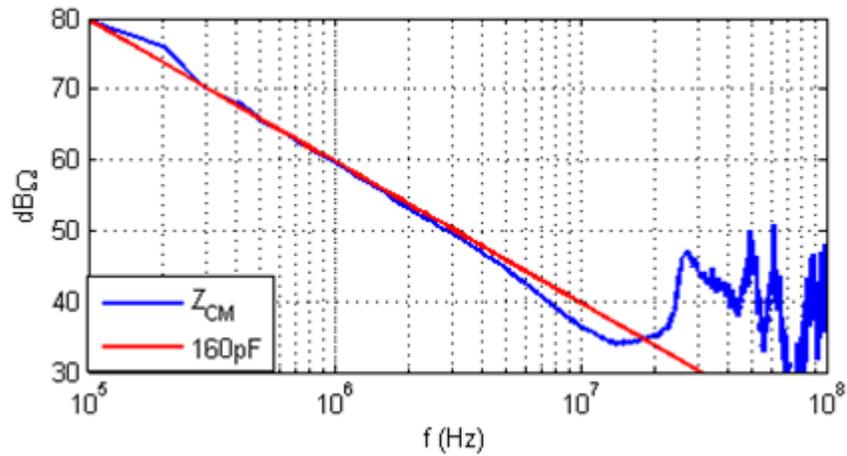
$$|I_{CM}(f)|_{dB} = |V_{DS}(f)|_{dB} - |Z_{CM}(f)|_{dB} \quad \text{Eq 4-6}$$

Since I_{CM} and V_{DS} are already found by measurement (Fig. 4-17a), the Z_{CM} can be deduced by applying these data in dB to Eq 4-6. The deduced Z_{CM} is shown in Fig. 4-17b and the downward slope signifies that this Z_{CM} is contributed mainly by a stray capacitance which is obvious the one between the AC and the GND potential. As discussed previously, this stray capacitance is contributed mainly by 39pF from the module and 60pF+60pF from the resistor load. The total 160pF’s impedance is compared with the Z_{CM} (Fig. 4-17b) and the result shows a correct modeling of these stray capacitances.

The stray capacitances’ impedance fit the measured Z_{CM} only up to 5MHz since the complete Z_{CM} is constituted by not only the capacitances but also the ground return parasitic inductances – L_{module} and L_{Load} – as shown by the simplified circuit in Fig. 4-18.



(a) Measured V_{DS} and I_{CM} in spectra



(b) Deduced Z_{CM}

Fig. 4-17: Definition of the CM noise propagation impedance Z_{CM}

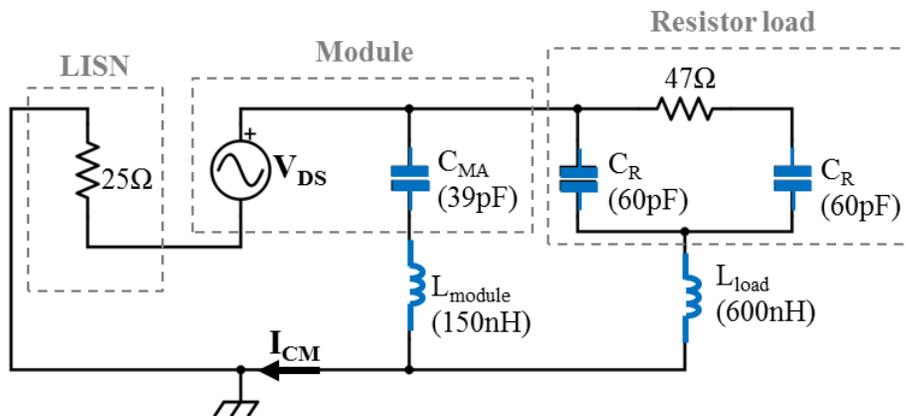


Fig. 4-18: Simplified model of Z_{CM}

The values of L_{Module} and L_{Load} are difficult to give a precise estimation since they are related to the geometries of the module/load and the grounding wire’s locations, etc. However, they can be defined by fitting the total Z_{CM} impedance model to the previously deduced one (**Fig. 4-17b**).

As observing the circuit model in **Fig. 4-18** and the measured Z_{CM} in **Fig. 4-17b**, the first resonance valley should be determined by $2 \cdot C_R$ (120pF) and L_{Load} , while the second one is supposed to be determined by C_{MA} (39pF) and L_{Module} . Therefore the former is approximated as 600nH and the latter 150nH. The modeled Z_{CM} is compared with the measured one as shown in

Fig. 4-19. It is concluded that the CM current goes mainly through the resistor load at frequency 100kHz~30MHz and mainly through the power module at frequency range above 30MHz.

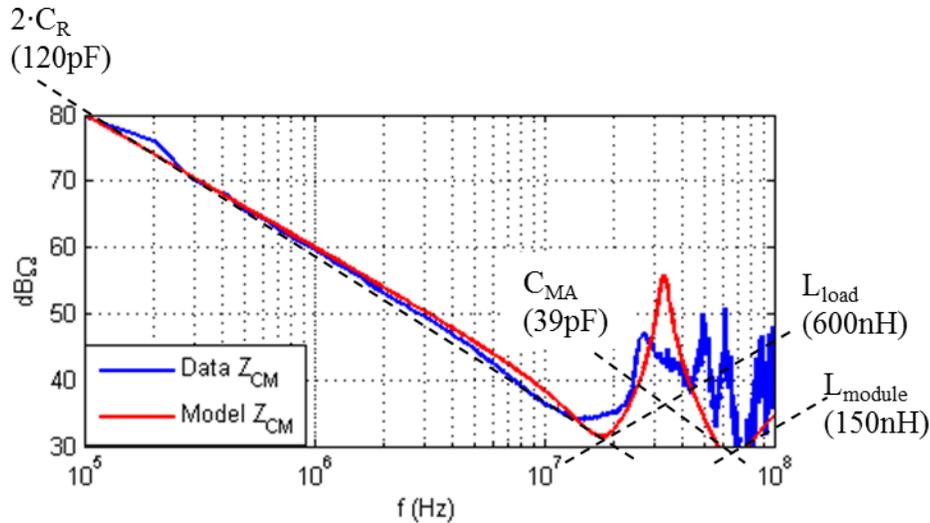
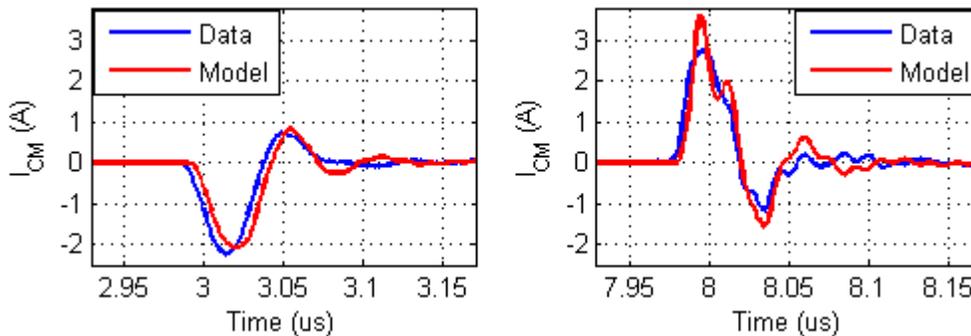
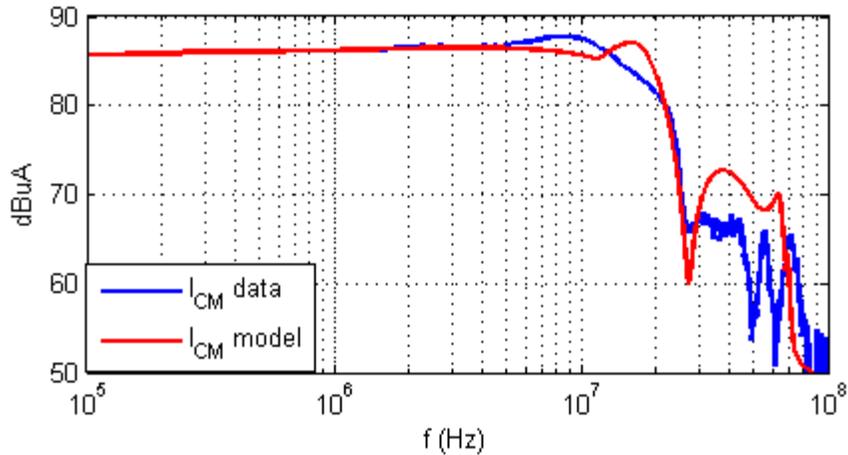


Fig. 4-19: Measured (data) and simulated (model) Z_{CM}

Completing the full simulation model in **Fig. 4-12** with values of L_{module} and L_{Load} , the final simulated (with circuit model in **Fig. 4-12**) and measured I_{CM} are shown in **Fig. 4-20**. The two results match each other with a good precision up to 30MHz. Above 30MHz, the tendency is correctly found within 5dB's error; however, the high-frequency resonances are failed to reconstruct. This is reasonable since the majority of the models are built up to 30MHz.



(a) Time domain



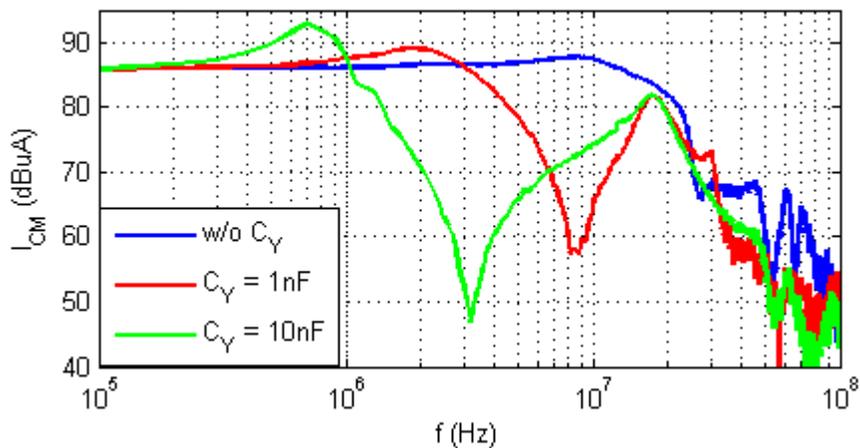
(b) Frequency domain

Fig. 4-20: Comparison of measured (data) and simulated (model) I_{CM} with bare module

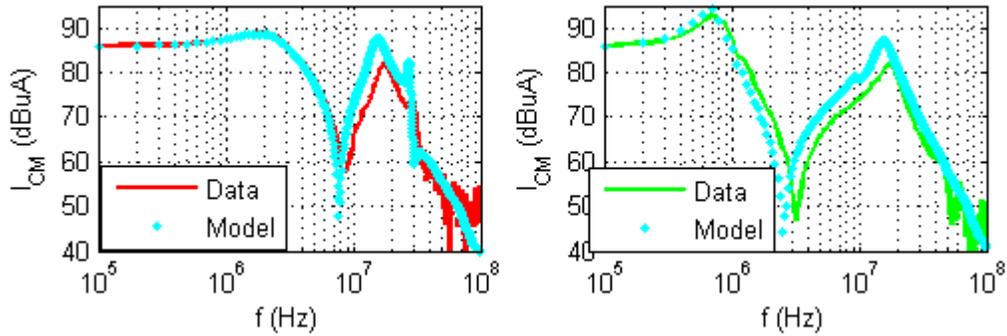
4.2.2 With C_Y capacitors

MLCC capacitors of 1nF/1KV and 10nF/1KV are used as test values for C_Y capacitor. **Fig. 4-21** shows the simulated and measured common mode EMI noise with C_Y capacitors of different values in AC – R load configuration.

It is observed that the CM noise starts to be attenuated according to the value of the C_Y capacitors, then reaches a valley bottom (at 3MHz with $C_Y=10$ nF and at 9MHz with $C_Y=1$ nF); then increases at a peak value (at 18MHz for both $C_Y=10$ nF and $C_Y=1$ nF).



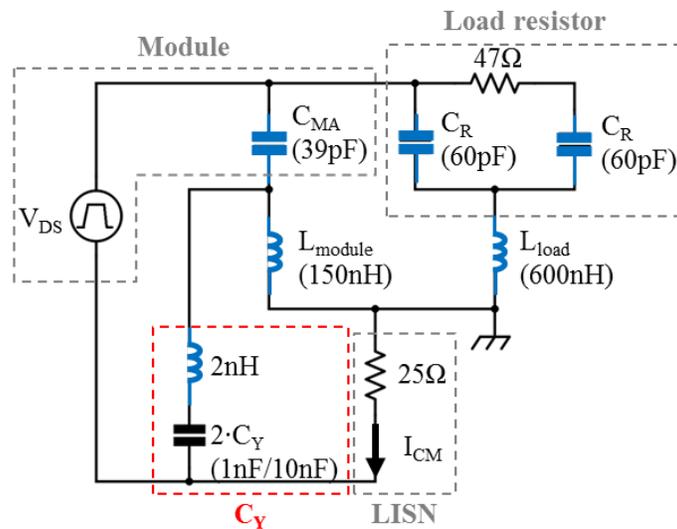
(a) Measured I_{CM} with different C_Y values



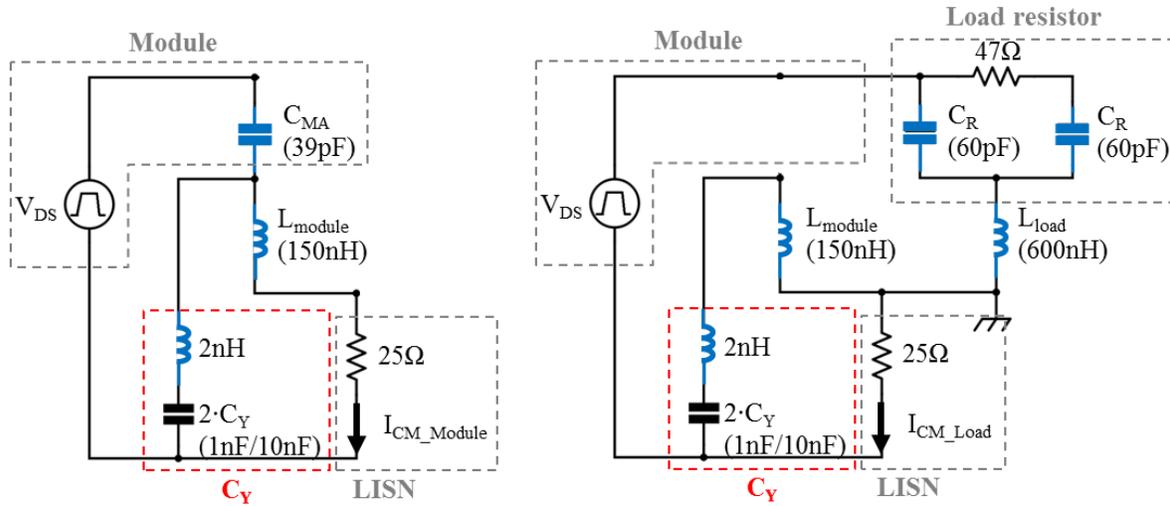
(b) Measured (data) vs simulated (model) I_{CM} with C_Y of 0.7nF (red) and 7nF (green)

Fig. 4-21: Comparison of measured (data) and simulated (model) I_{CM} with C_Y capacitors

These CM noise valley and peak values are analyzed in **Fig. 4-22**. shows the origin of this parasitic inductance. **Fig. 4-22a** shows the simplified CM noise propagation path (c.f.) including the C_Y capacitors. The noise source – mid-point voltage V_{DS} – creates two CM currents through respectively stray capacitances of the power module C_{MA} (39pF) and of the load resistor $2 \cdot C_R$ (60pF \times 2). Then the two currents pass through respectively their ground parasitic inductance being seen from the power module (150nH) and the load resistor (600nH) and go back to the LISN resistance, simplified as 25 Ω . The two aforementioned CM currents are named I_{CM_Module} and I_{CM_Load} and their impedance paths are shown in **Fig. 4-22b** and **Fig. 4-22c**.



(a)



(b) above 30MHz

(c) under 30MHz

Fig. 4-22: Common mode noise propagation path

- In **Fig. 4-22b**, as discussed in 4.2.1, the CM noise propagation path $C_{MA} + L_{Module}$ involves in the frequency range above 30MHz. In addition, the C_Y capacitors represent low impedance in a wide frequency range thanks to its small associated parasitic inductance (2nH); thus the CM current generated by V_{DS} on C_{MA} flows mostly through C_Y capacitors other than the LISN. Therefore, C_Y capacitors have a well attenuation effect on the CM current generated within the power module.
- In **Fig. 4-22c**, as discussed in 4.2.1, the CM noise propagation path $2 \cdot C_R + L_{Load}$ involves in the frequency range under 30MHz, where occur the aforementioned noise valley (3MHz / 9MHz) and peak values (18MHz). This CM noise propagation path – Z_{CM} – can be represented as below:

$$Z_{CM} = Z_{2 \cdot C_R} + Z_{L_{Load}} + (Z_{2 \cdot C_Y} + Z_{L_{Module}}) // Z_{25\Omega} \quad \text{Eq 4-7}$$

Putting **Eq 4-7** into **Eq 4-5**, the CM current can be defined as :

$$I_{CM} = V_{DS} \cdot (Z_{2 \cdot C_R} + Z_{L_{Load}} + (Z_{2 \cdot C_Y} + Z_{L_{Module}}) // Z_{25\Omega})^{-1} \quad \text{Eq 4-8}$$

This equation can explain the valley and peak values in CM noise above: 1) the peak value of I_{CM} occurs when $Z_{2 \cdot C_R} + Z_{L_{Load}}$ reaches its minimum value at the resonance frequency determined by $2 \cdot C_R$ and L_{Load} ; 2) the valley value of I_{CM} occurs when $Z_{2 \cdot C_Y} + Z_{L_{Module}}$ reaches its minimum value at the resonance frequency determined by $2 \cdot C_Y$ and L_{Module} . These calculated resonance frequencies match well with the observed frequencies. These resonance frequencies are illustrated in **Fig. 4-23**.

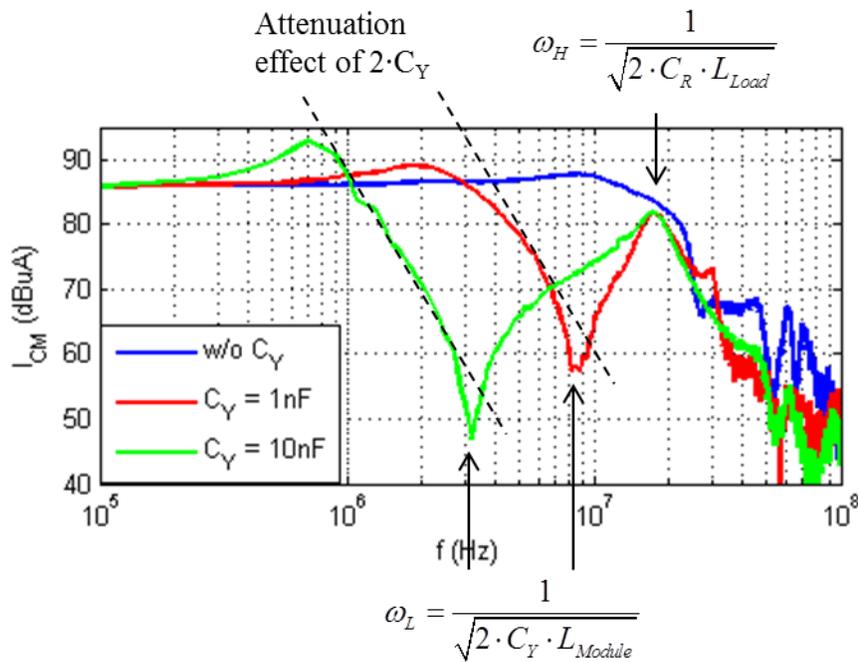


Fig. 4-23: Attenuation effect of C_Y capacitors and relevant resonance frequencies

With fixed value of C_Y (CM filter capacitance according the EMC norm) and C_R (parasitic of load resistor) capacitances, it is recommended to: 1) increase the L_{Load} value in order to pull the frequency ω_H towards the low frequency so that the peak value is decreased; 2) decrease the L_{Module} in order to push the frequency ω_L towards the high frequency so that the attenuation effect of C_Y capacitors can be extended.

4.2.3 With C_X capacitors

The CM noises, however, are little influenced by C_X capacitors up to 30MHz, as shown in **Fig. 4-24**. Above 30MHz, C_X capacitors result in suppression of the high frequency peak values observed at 60MHz and 70MHz. This “to be verified” phenomenon can be explained by the fact that C_X capacitance recycles the high frequency DM noise being transformed into CM one. Since the model’s precision is limited at 30MHz, this phenomenon has not been found in simulation.

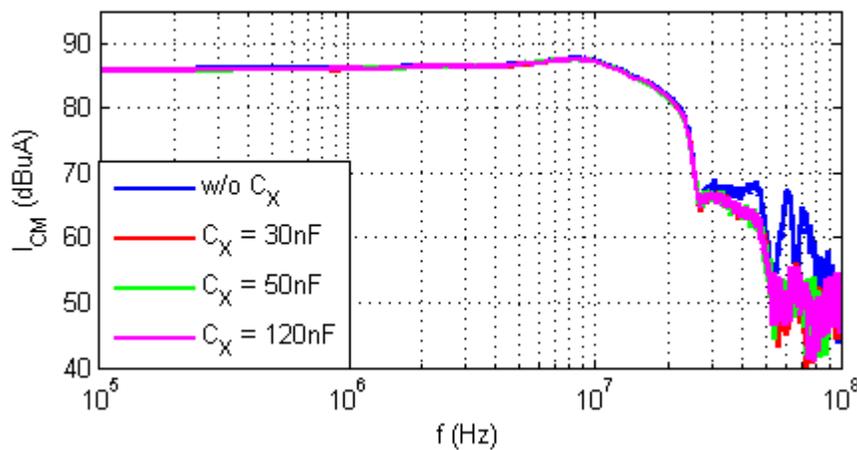


Fig. 4-24: Measured I_{CM} with C_X capacitors

4.2.4 With both C_X and C_Y capacitors

The measured CM noises, with the bare power module and with 120nF as C_X capacitor and 10nF as C_Y capacitors, are compared in **Fig. 4-25**. The main attenuation effects occur :

- At mid frequency range (1MHz ~ 20MHz), C_Y capacitors attenuate the CM noise but this attenuation effect is compromised by the ground return parasitic inductances L_{Module} and L_{Load} ;
- At high frequency range (above 30MHz), either C_X capacitors or the two C_Y capacitors in series (which serve as small value C_X capacitors) can reduce the CM noise which is transformed from the DM one.

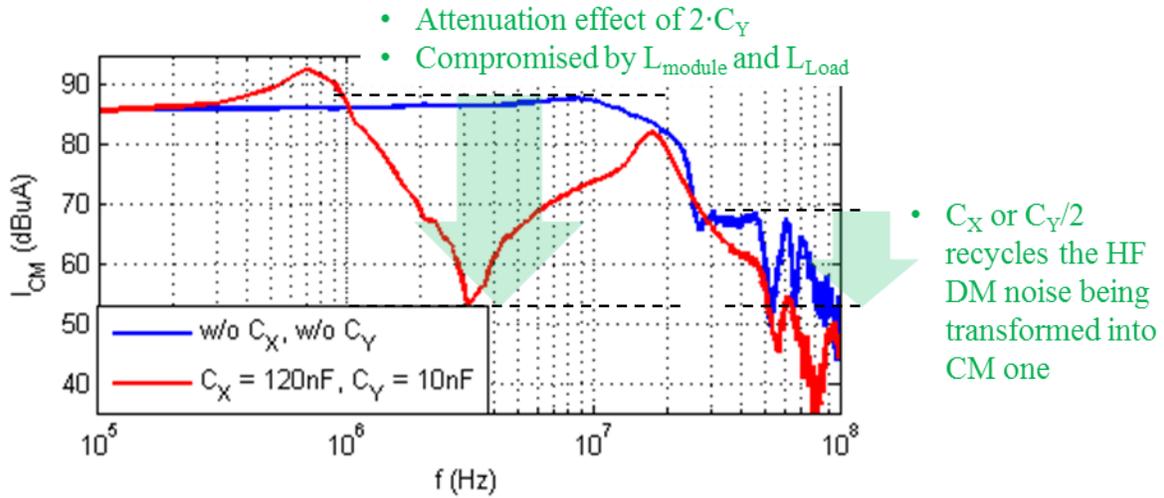
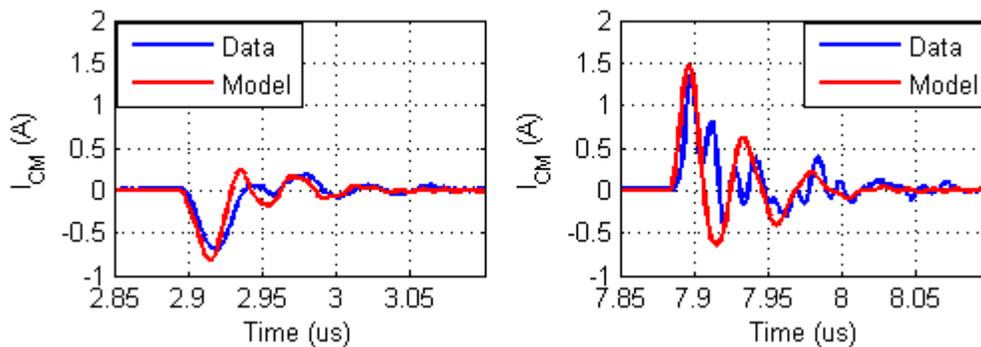


Fig. 4-25: CM current with bare module and with both C_X and C_Y capacitors

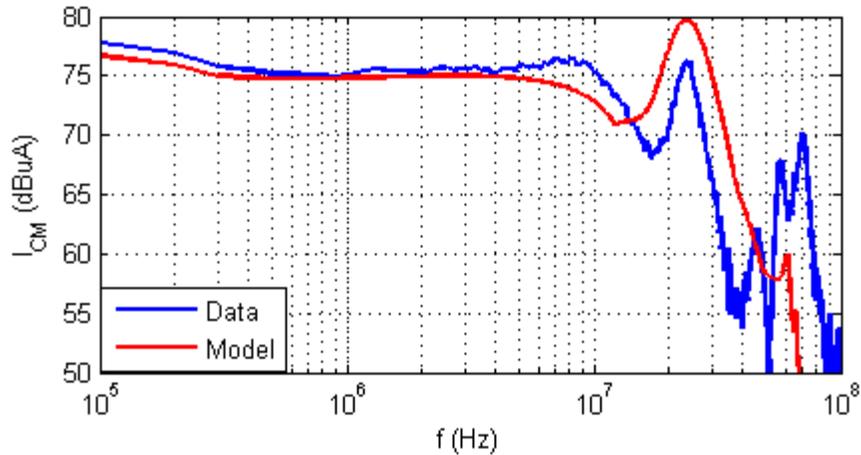
4.3 Common mode current I_{CM} with resistor load connected to DC terminal

4.3.1 With the bare module

As discussed previously, with the resistor load connected to the DC terminal, the DC sides are highly imbalanced and thus mode transformation would occur. The simulated (with the circuit in Fig. 4-12) and measured I_{CM} are shown in Fig. 4-26.



(a) Time domain



(b) Frequency domain

Fig. 4-26: Measured (data) and simulated (model) I_{CM} with resistor connected to DC terminal

In this load configuration, the mid-point stray capacitance is relatively smaller ($39\text{pF} + 5\text{pF}$); however, the DC+ side stray capacitance ($38\text{pF} + 60\text{pF} + 60\text{pF} + 5\text{pF}$) is much larger than the DC- one (44pF), which causes a mode transformation from the DM noise source I_{DS} to the CM noise I_{CM} . This mode transformation can be explained as in **Fig. 4-27**, which involves the relevant impedances extracted from the simulation circuit in **Fig. 4-12**. I_{CMDS} represents the CM current transferred from the DM noise source I_{DS} and it can be defined as in **Eq 4-9**. Detail calculation can be found in Appendix B.

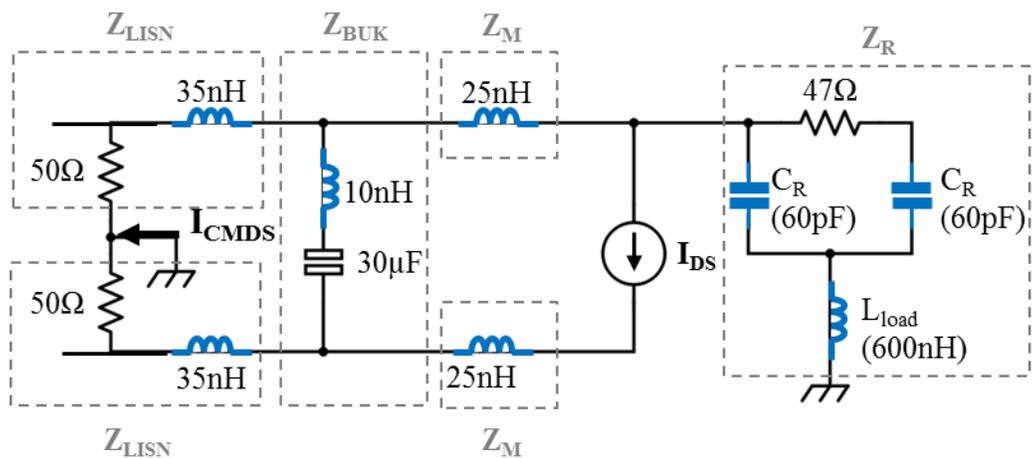


Fig. 4-27: Relevant impedance resulting in mode transformation from DM to CM

$$k(f) = \frac{I_{CMDS}(f)}{I_{DS}(f)} = \frac{1}{1 + \frac{Z_R + Z_{LISN} / 2}{Z_M + Z_{BUK} / 2}} \quad \text{Eq 4-9}$$

This transformation coefficient k has its maximal value with

$$f_{\max} = \frac{1}{2\pi \sqrt{2 \cdot C_R \cdot L_{Load}}}$$

Then I_{CMDS} is compared with the total CM one I_{CM} in **Fig. 4-28c**.

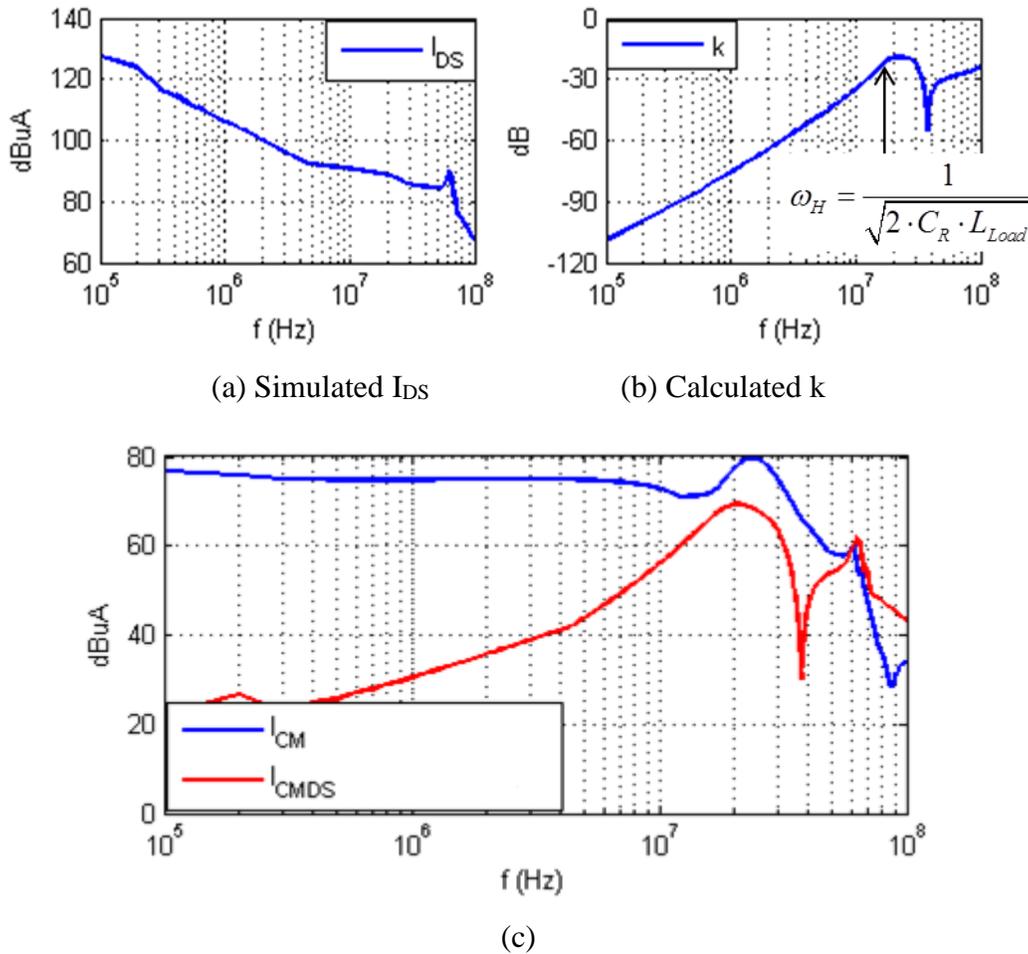
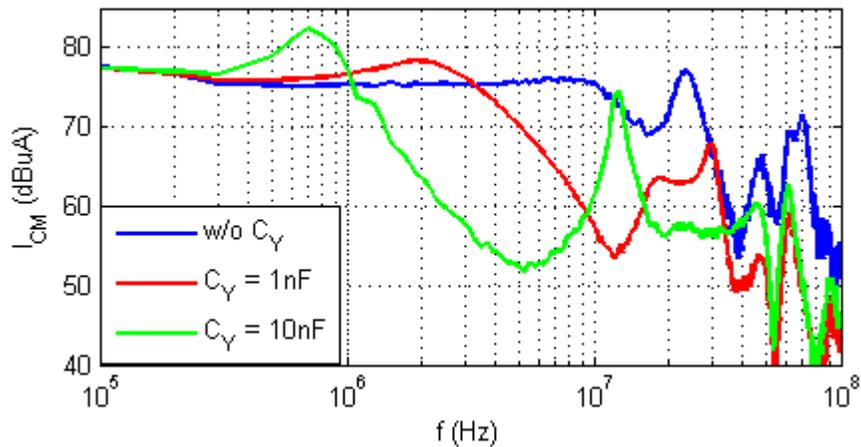


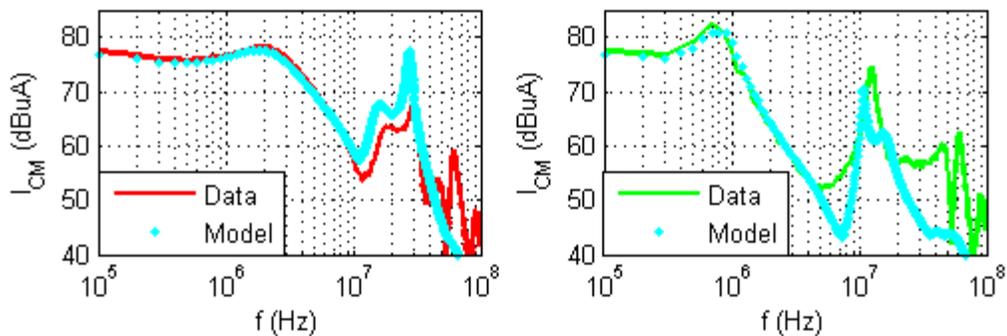
Fig. 4-28: The DM EMI noise source I_{DS} (a), the transformation coefficient k from DM to CM (b) and the deduced I_{CM} transformed from I_{DS} (c)

4.3.2 With C_Y capacitors

Fig. 4-29 shows the CM EMI noise with C_Y capacitors of different values in AC – L load configuration.



(a) Measured I_{CM} with different C_Y values



(b) Measured (data) vs simulated (model) I_{CM} with C_Y of 1nF (red) and 10nF (green)

Fig. 4-29: Comparison of measured (data) and simulated (model) I_{CM} with C_Y capacitors

C_Y capacitors' attenuations are observed as in previous analysis. However, undesired peak values appear at different frequencies with different values of C_Y capacitors. These peak values can be explained by circuit in **Fig. 4-22**, which is the impedances relevant for mode transformation from DM to CM. I_{CMDS} represents the CM current transferred from the DM noise source I_{DS} and it can be defined as in **Eq 4-10**. Detail calculation can be found in Appendix B.

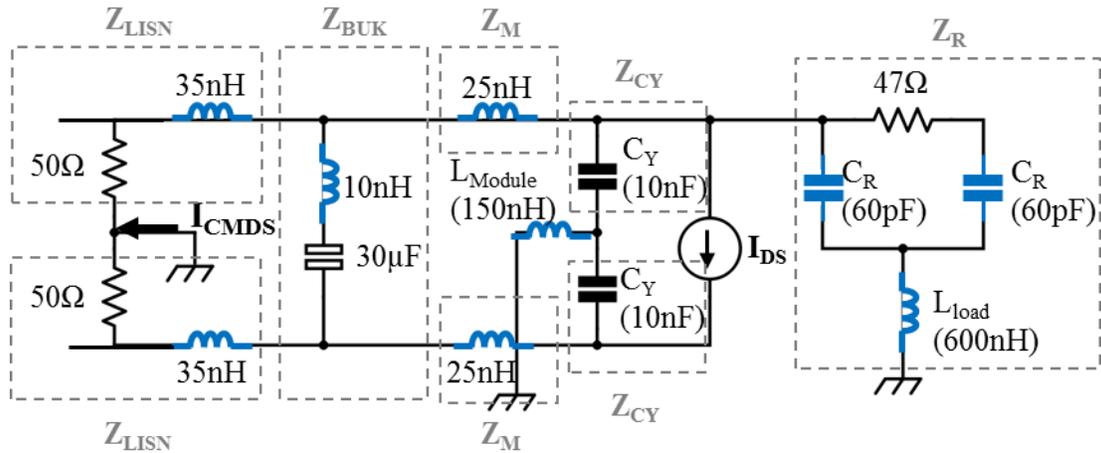


Fig. 4-30: Relevant impedance resulting in mode transformation from DM to CM

$$k(f) = \frac{I_{CMDS}(f)}{I_{DS}(f)} = \frac{\left(\frac{1}{1 + \frac{1}{1 + \frac{1}{Z_{CY} + Z_R + Z_{LM}}}} - \frac{1}{2} \right) \left(\frac{1}{Z_{LM} + \frac{Z_{LISN}}{2}} \right)}{\left(\frac{1}{2 \cdot Z_M + Z_{CX}} + \frac{1}{2 \cdot Z_{CY}} \right)} \quad \text{Eq 4-10}$$

The denominator of the equation above implicates that the k has a peak value at the frequency determined by $2 \cdot Z_M + Z_{CX} + 2 \cdot Z_{CY}$, which is defined in equation below:

$$f_{\max} = \frac{1}{2\pi \sqrt{2 \cdot C_Y \cdot \left(L_M + \frac{L_{C0}}{2} \right)}}$$

Where L_M is the DC bus parasitic inductance of the power module and L_{C0} the ESL of the bulk capacitor.

In **Fig. 4-31a**, it is noted that the magnitude peak of I_{DS} at high frequency disappears thanks to the “ C_X ” capacitors. **Fig. 4-31c** shows the CM noise transformed from the DM noise source.

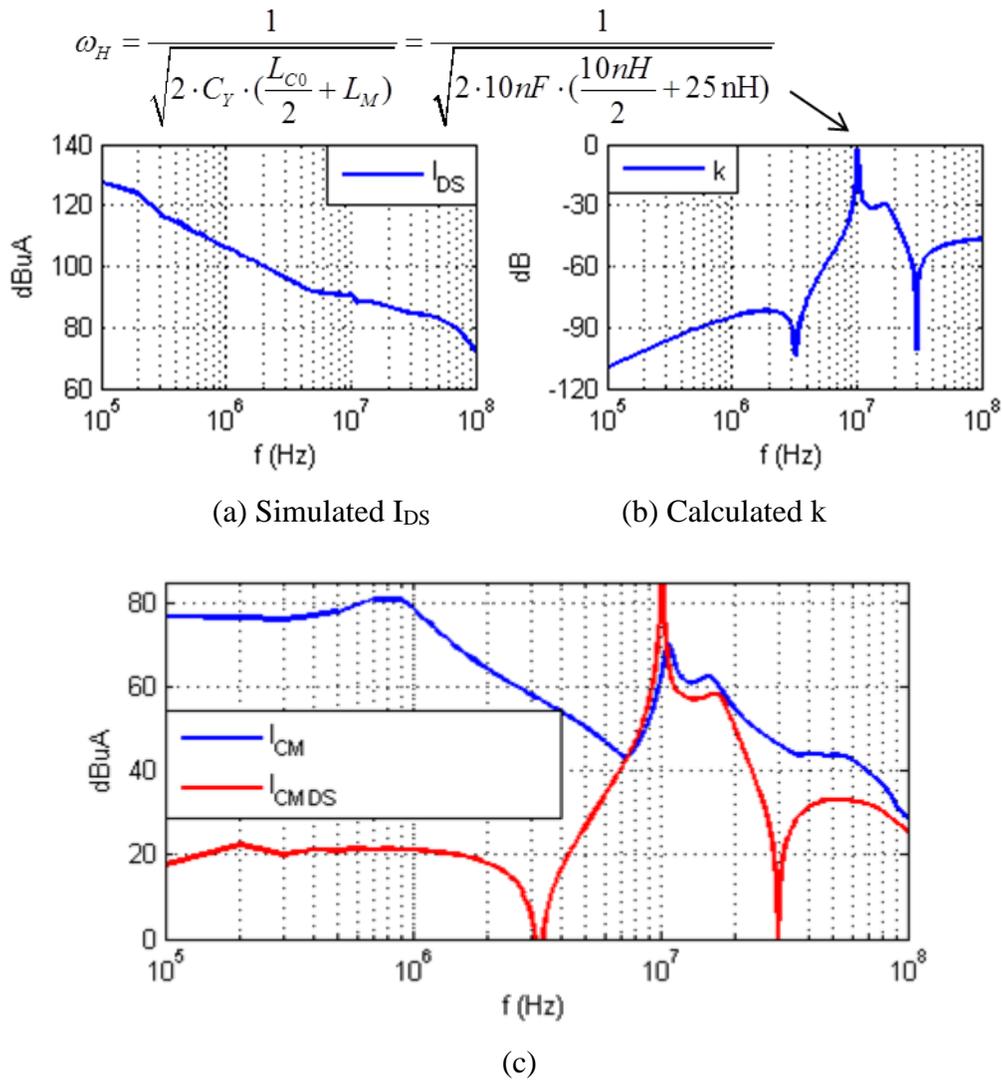


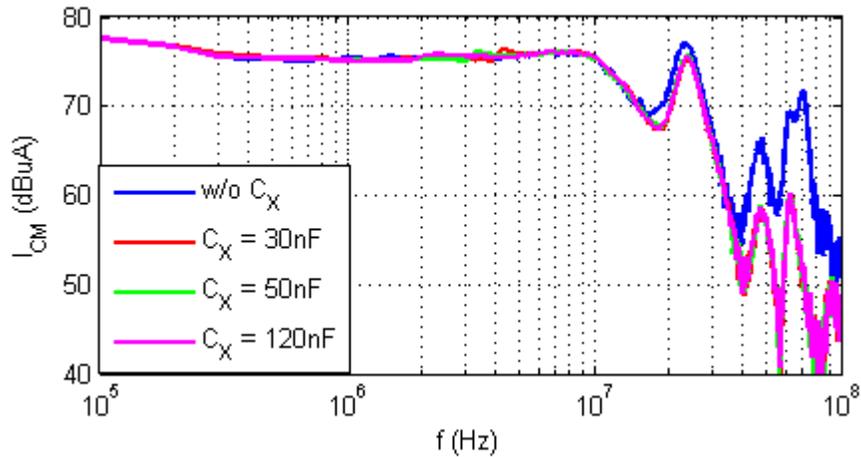
Fig. 4-31: The DM EMI noise source I_{DS} (a), the transformation coefficient k from DM to CM (b) and the deduced I_{CM} transformed from I_{DS} (c)

Since the I_{CM} noise peak at 12MHz is transformed from I_{DS} , a C_X capacitor close to the source I_{DS} will be efficient to recycle its high-frequency component thus reduce the I_{CM} noise at relevant frequency band. This will be approved in section 0.

4.3.3 With C_X capacitors

The CM noises, however, are little influenced by C_X capacitors up to 30MHz, as shown in **Fig. 4-32**. Above 30MHz, C_X capacitors result in suppression of the high frequency peak

values observed at 60MHz and 70MHz. This “to be verified” phenomenon can be explained by the fact that C_X capacitance recycles the high frequency DM noise being transformed into CM one. Since the model’s precision is limited at 30MHz, this phenomenon has not been found in simulation.



(b) AC – L load configuration

Fig. 4-32: Measured I_{CM} with different C_X values

4.3.4 With both C_X and C_Y capacitors

The measured CM noises, with the bare power module and with 120nF as C_X capacitor and 10nF as C_Y capacitors, are compared in **Fig. 4-33**.

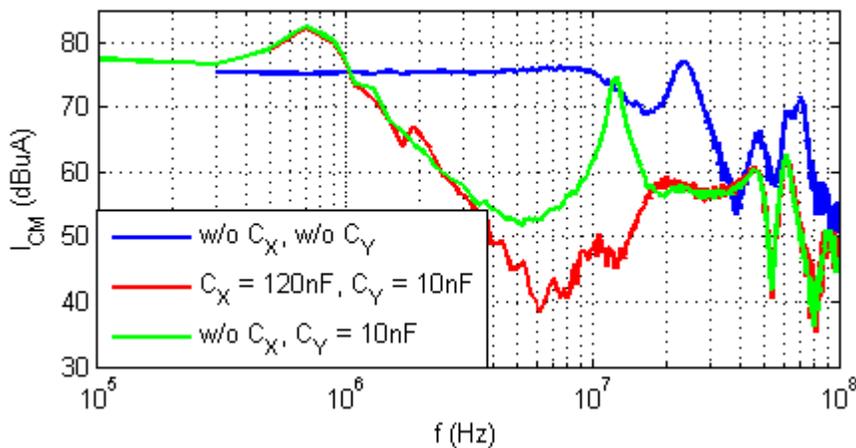


Fig. 4-33: CM current with bare module and with both C_X and C_Y capacitors

- From bare module to only using C_Y capacitors, a peak value appears due to the mode transformation from DM noise source IDS, as discussed in 4.3.2;
- In order to suppress this peak, placing C_X capacitors is an efficient way as shown in the figure; this is because the existence of C_X capacitors modifies the transformation coefficient k .

4.4 Differential mode current I_{DM} in both load connecting configurations

4.4.1 With the bare module

The differential mode currents I_{DM} in both load connecting configurations are the same. This means that there is little impact from the common mode noise source to the differential one, even when there is a significant imbalance between the DC sides. The measured result, shown in **Fig. 4-34** and well matched with the simulated one.

This DM noise starts from the switching frequency 100kHz and decreases due to the filter effect of the bulk DC link capacitor. This attenuation ends very soon at around 300kHz due to the ESL (10nH) of the capacitor. The other noise peak at around 70MHz is due to the oscillation resonance in switching current which is determined by the C_{OSS} capacitance of the power device and the total parasitic inductance in power loop.

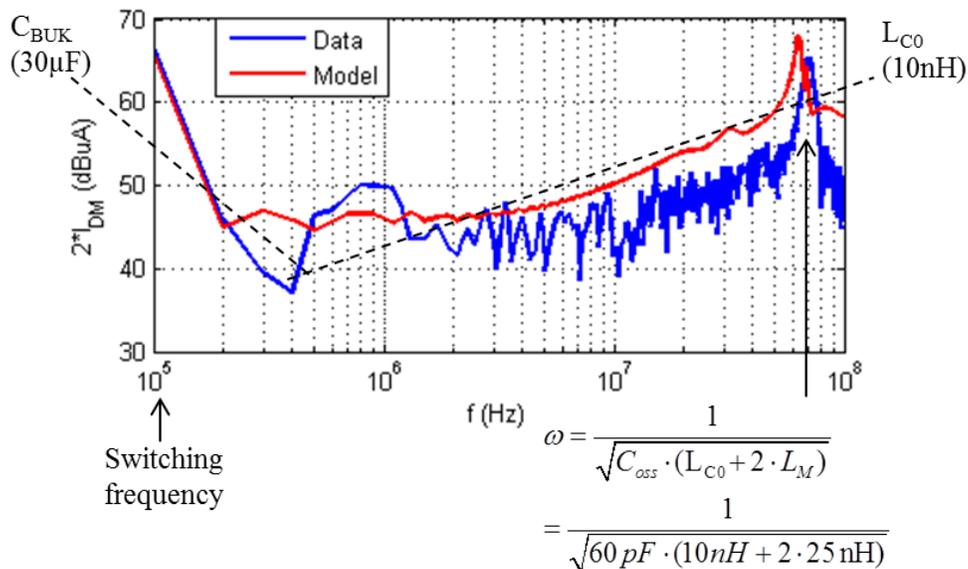
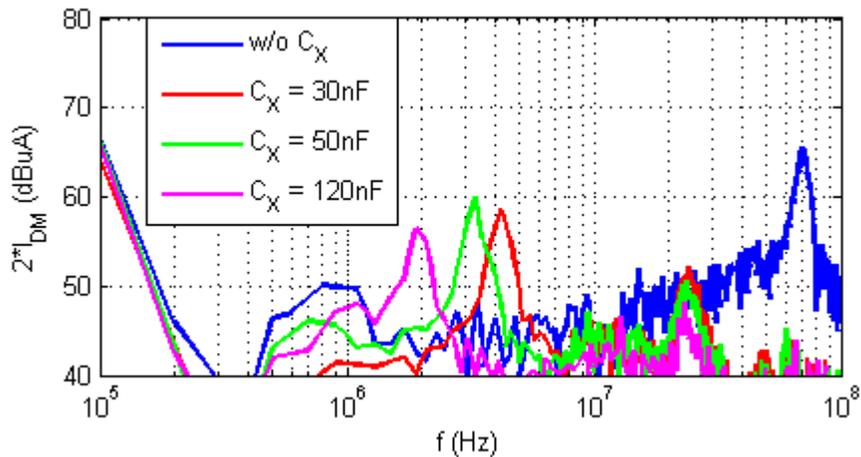


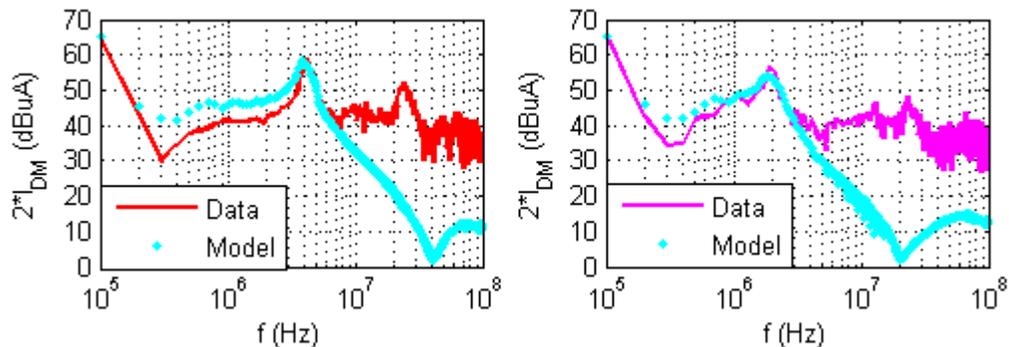
Fig. 4-34: Frequency domain comparison of measured (data) and simulated (model) $2 \cdot I_{DM}$

4.4.2 With C_X capacitors

MLCC capacitors of 47nF/1kV, 150nF/630V and 450nF/630V are used as test values for C_X capacitor. As discussed in 3.3.1, their capacitance values decrease as voltage increases and are estimated as 30nF, 50nF and 120nF. The measured DM noises with these C_X capacitors are shown in **Fig. 4-35a**.



(a) Measured $2 \cdot I_{DM}$ with different C_X values



(b) Measured (data) vs simulated (model) $2 \cdot I_{DM}$ with C_X of 30nF (red) and 120nF (purple)

Fig. 4-35: Differential mode noise comparisons in AC – R/L configuration

Compared with the simulated results in **Fig. 4-35b**, C_X capacitors attenuate the high-frequency DM noise; however, a resonance peak appears at the frequency due to C_X and the parasitic inductance (L_{DC} in **Fig. 3-28**) between DC link capacitor and the C_X capacitor. Above ~MHz, the significant difference between the simulated and measured I_{DM} is due to the

measurement sensibility of the scope precision, where the noise floor level is about 35dB μ A. In addition, mode transformation from CM to DM is observed at the noise floor.

Another effect of C_X capacitor is that it increases the mid-point voltage V_{DS} 's slew rate (Fig. 4-36a) and this will increase the magnitude of the V_{DS} in high-frequency. The FFT of these time domain voltages V_{DS} are shown in Fig. 4-36b. It is observed that the spectra's difference is not apparent until to 80MHz.

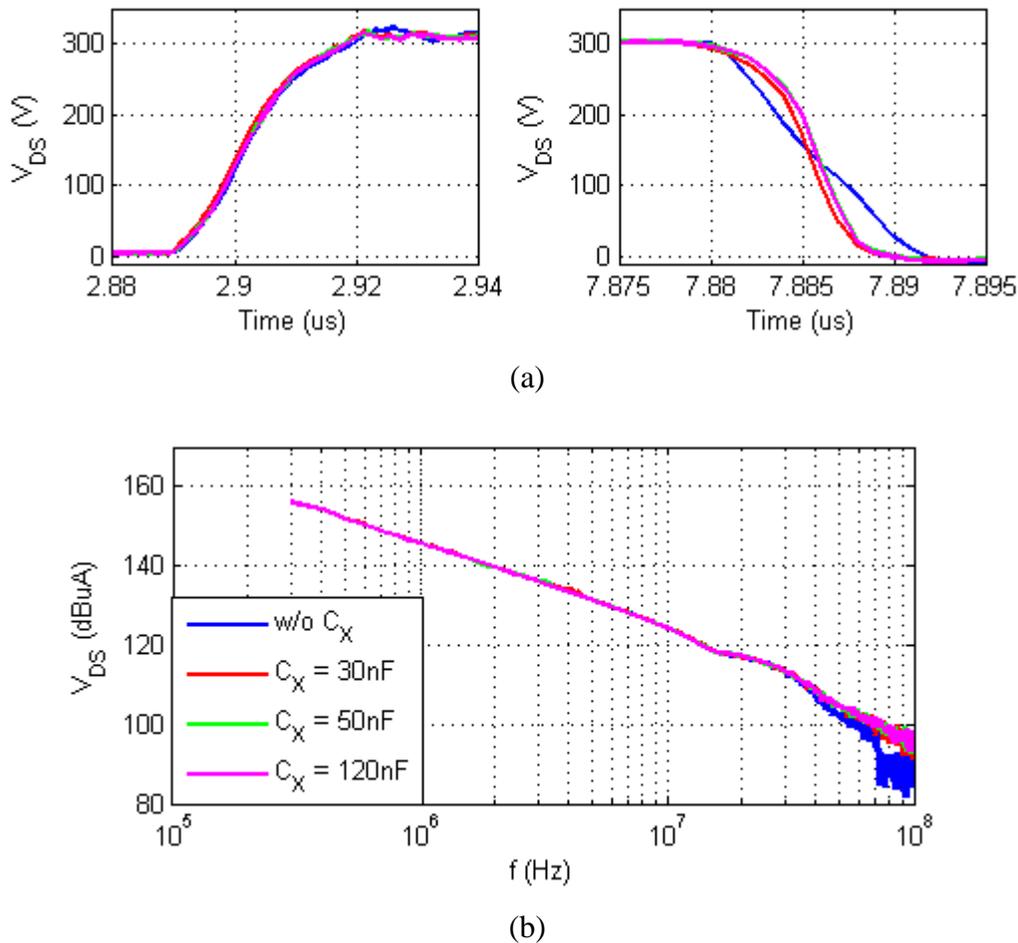
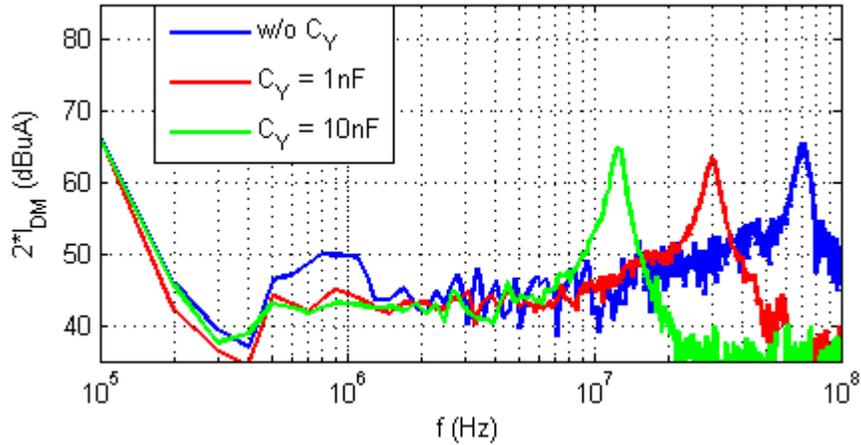


Fig. 4-36: Variation of V_{DS} with different C_X values in time (a) and frequency (b) domain

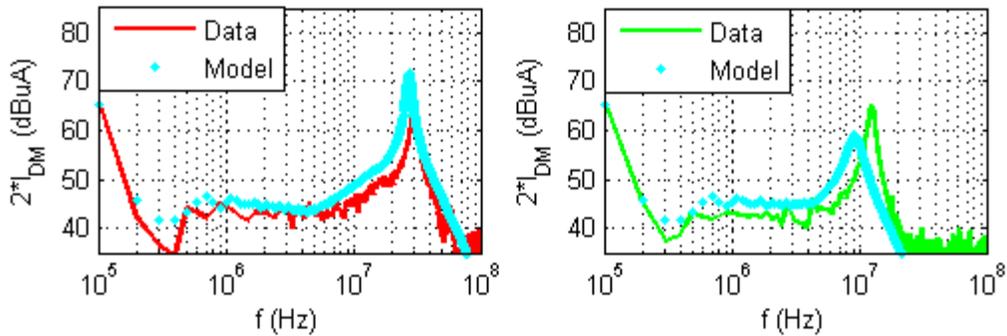
4.4.3 With C_Y capacitors

MLCC capacitors of 1nF/1kV and 10nF/1kV are used as test values for C_Y capacitor. As discussed in 3.3.1, their capacitance values decrease as voltage increases and are estimated as

0.8nF and 7nF. The measured DM noises with these C_Y capacitors are shown in **Fig. 4-37a**. The results are similar to the previous analysis with C_X capacitors. The two C_Y capacitors in series serve as one equivalent “ C_X ” capacitor.



(a) Measured $2 \cdot I_{DM}$ with different C_Y values



(b) Measured (data) vs simulated (model) $2 \cdot I_{DM}$ with C_Y of 1nF (red) and 10nF (green)

Fig. 4-37: Differential mode noise comparisons in AC – R/L configuration

4.4.4 With both C_X and C_Y capacitors

The measured DM noises, with the bare power module and with 120nF as C_X capacitor and 10nF as C_Y capacitors, are compared in **Fig. 4-38**.

- From bare module to only using C_X capacitors, the peak value at 70MHz is suppressed; however another peak appears at lower frequency with lower magnitude.

- Using C_Y capacitors can make DM noise lower between 3MHz and 30MHz; this is probably thanks to the C_Y capacitors attenuating the CM noise being supposed to transfer to the DM one, but this is to be verified.

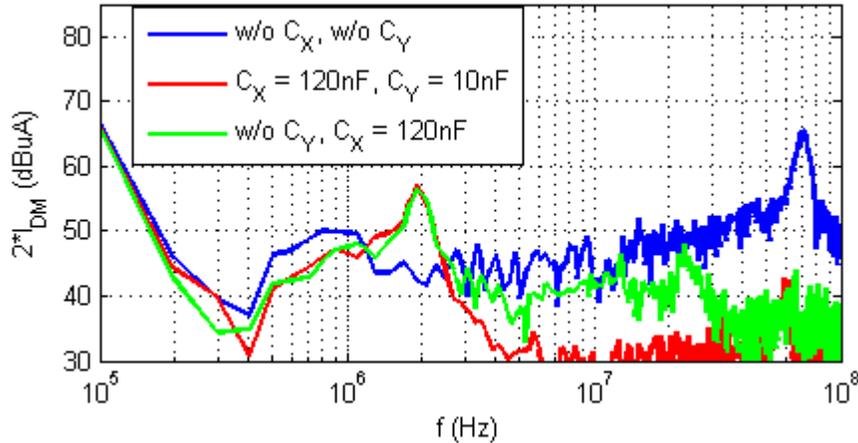


Fig. 4-38: DM current with bare module and with both C_X and C_Y capacitors

4.5 Discussion on common mode filter

The previous studies have validated the efficiency and precision of the whole power module system's modeling in terms of switching and EMI characteristics. The in-module C_X and C_Y capacitors' influences on EMI noises have been evaluated in different load connection configurations. However, in-module capacitors cannot stand alone to attenuate the EMI noises down to the required level; the input filter is a must for the adjusting of the total EMI performance. In case of the CM filter, C_Y capacitors' value is limited by the maximally allowed ground leakage current, say 20nF for one side C_Y capacitance. An issue would be discussed: Should the total 20nF be inserted in the power module (C_{Y_IN}) or be applied to the input filter (C_{Y_EX}) as shown in **Fig. 4-39**? Or is there an optimal distribution between the C_{Y_IN} and the C_{Y_EX} ?

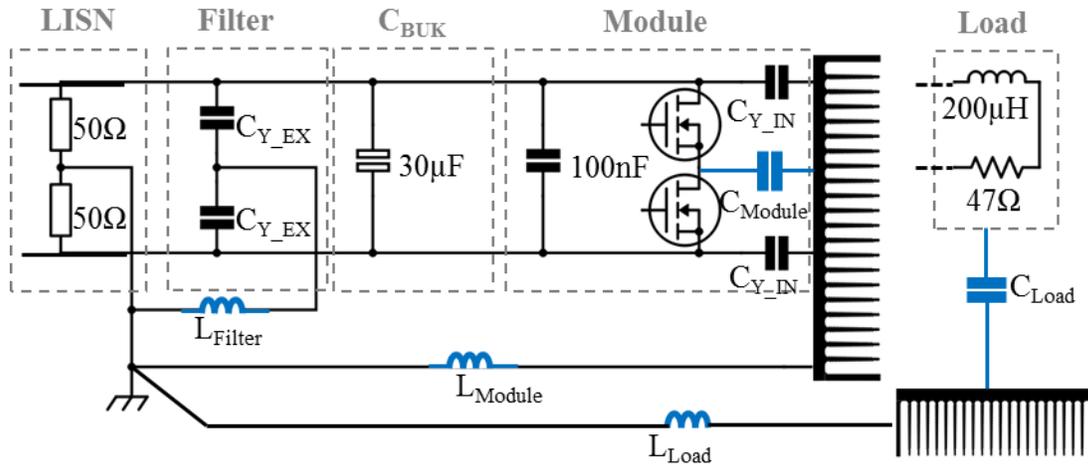


Fig. 4-39: CY capacitors in input filter (C_{Y_EX}) and in the power module (C_{Y_IN})

In this section, the distribution of C_{Y_IN} and C_{Y_EX} is studied via the simulation of the previously developed model. As shown in **Fig. 4-39**, the same MLCC capacitors are inserted in the place for input filter (C_{Y_EX}) and in the power module (C_{Y_IN}). It should be noted that L_{Filter} is the ground return parasitic inductance of the input filter and it is estimated as 50nH. Similarly, L_{Module} and L_{Load} are calculated as 150nH and 600nH in previous study. The in-module C_X capacitor is set as 100nF to minimize the switching voltage overshoot and filter the high-frequency DM noise.

Fig. 4-40 shows the simulated CM noises with different distributed values of C_{Y_EX} and C_{Y_IN} .

- In **Fig. 4-40a**, the CM noises I_{CM} are compared in two extreme combinations of C_{Y_EX} and C_{Y_IN} . – either 20nF only in C_{Y_IN} (blue) or only in C_{Y_EX} (red). It is observed that the latter has a better attenuation effect than the former at the range of 1MHz to 30MHz; above 30MHz, the situation is inverted. Is it possible to keep the better attenuation effects in both frequency ranges?
- In **Fig. 4-40b**, a larger portion of the total C_Y capacitance is inserted into the power module ($C_{Y_IN}=16nF$) and the rest portion is inserted into the input filter ($C_{Y_EX}=4nF$). It is observed that an undesired noise peak occurs at 4MHz.

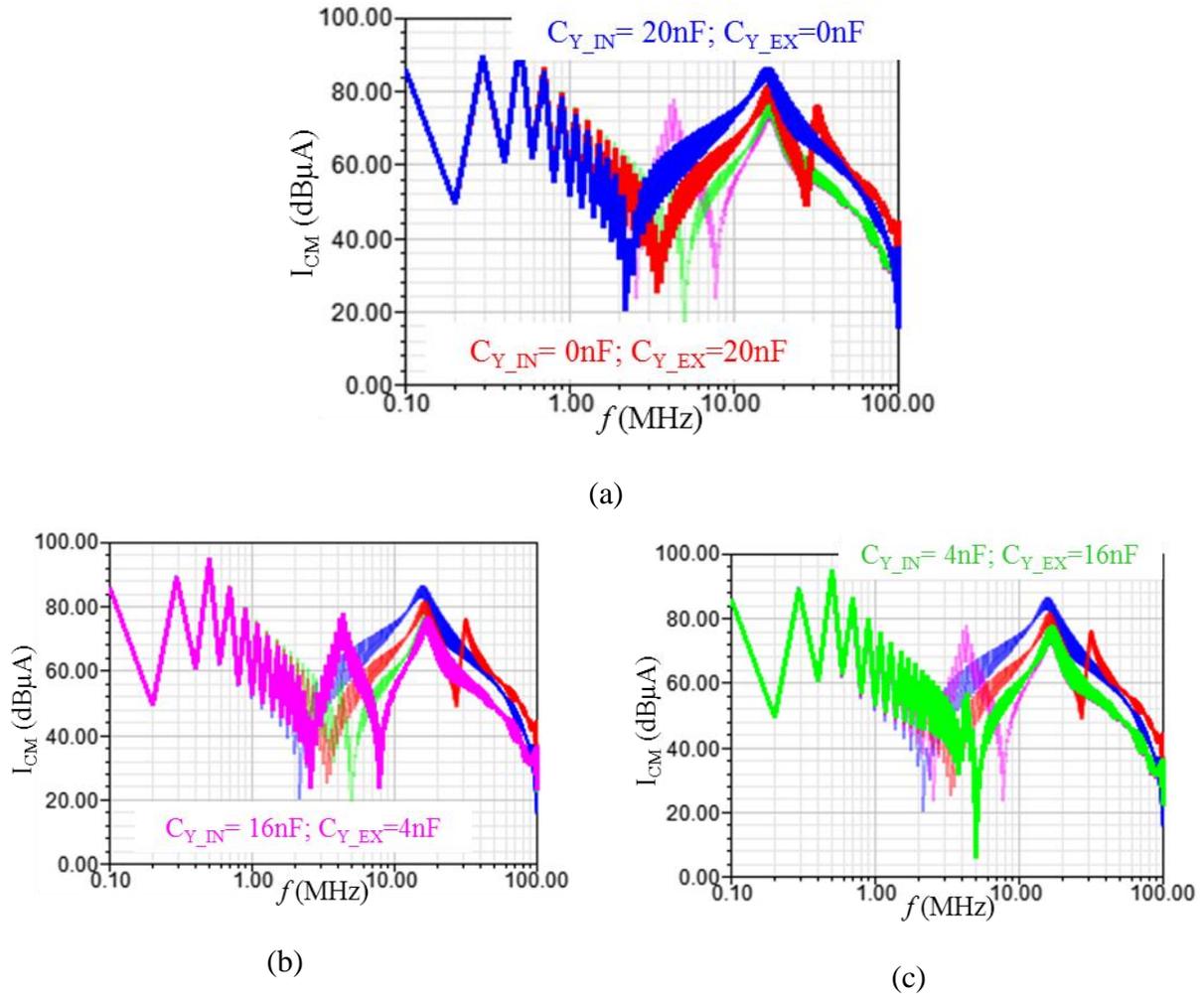


Fig. 4-40: Parametric study of C_{Y_EX} and C_{Y_IN} by simulation

- In **Fig. 4-40c**, a larger portion of the total C_Y capacitance is inserted into the input filter ($C_{Y_EX}=16\text{nF}$) and the rest portion is inserted into power module ($C_{Y_IN}=4\text{nF}$). In this case, a best attenuation among the three configurations has been given.

This parametric study above indicates that there is an optimal distribution of C_{Y_EX} and C_{Y_IN} exists to have a best CM attenuation effect. In general, C_{Y_EX} should take the most of the C_Y capacitance value and the C_{Y_IN} only need a small value. This can be explained by that 1) C_{Y_IN} is only efficient for recycling the CM noise generated from the power module as explained in **Fig. 4-22**; 2) C_{Y_EX} is effective for attenuation of global CM noise (generated from the module and the load) but the high-frequency attenuation effect is limited.

4.6 Conclusions

In this chapter, the GaN power module has been tested in switching with the resistor-inductor load and the common mode and differential mode EMI noises are measured and compared with the simulated ones with previously developed models, where the results are correctly matched. It has been observed that different load connecting configuration leads to significant different common mode noises. The reasons have been analyzed that the complicated common mode propagation path constituted by the resistor load either increases the common mode noise magnitude (by connecting the resistor load to AC terminal) or generates the mode transformation from the differential mode noise source to the common mode noise (by connecting the inductor load to AC terminal). Based on the correct modeling of the in-module capacitors, a parametric study on the distribution of the in-module C_Y capacitor and the ones in the input filter has been executed by simulation. It has been concluded that an optimal distribution exists for a best attenuation effect at all frequency range.

The using of C_X and C_Y in-module capacitors is concluded below:

- C_X capacitor's value should be large enough 1) to assure a minimum switching voltage overshoot and 2) to attenuate the high-frequency (above ~MHz) DM noise to desired level (EMC standard) or to avoid mode transformation to CM noise. The 1) is in priority since it reduces significantly the power device's stress and switching losses; the value in 2) is often lower than the one in 1). 100nF is a minimum C_X capacitance value for the SATIE GaN module in this dissertation.
- C_Y capacitor's value should be large enough to recycle the CM noise generated within the module, not anywhere else (e.g. from the load). An optimal distribution of C_Y capacitances in module and in EMI filter exists and requires an analysis at the global converter. 4nF is an optimal in-module C_Y capacitance for the SATIE GaN module in this dissertation.

Compared with traditional power module using IGBT or MOSFET, modules using GaN technologies result in 1) smaller size and 2) faster switching. The 1) makes the module itself no longer the essential EMI noise propagation path; in this dissertation, the load resistor contributes much more significantly to CM noise propagation path than the module. The 2) results in higher

dV/dt and dI/dt , thus -20dB/dec in noise sources' spectra up to over hundreds of MHz; in the IGBT's case, which switch at $\sim 200\text{ns}$'s dV/dt , the -20dB/dec in noise source's spectra ends up at around 2MHz and followed by -40dB/dec .

GENERAL CONCLUSIONS AND PERSPECTIVES

In order to understand EMI phenomenon concerning the GaN device based power module and thus to find recommendations for design optimization, modeling / experimental / parametric analysis have been studied during the three years' research. The main achieved results are reviewed as the realized work below:

Realized work

- Technologies of the GaN power devices – from the material properties to the device structures – have been reviewed; State-of-the-art low inductive power module designs have been presented and the EMI relevant parasitic elements have been resumed.
- A compact modeling methodology for all e-mode GaN HEMT has been developed. This has been demonstrated by modeling a commercial 600V GaN HEMT based on the static and dynamic characteristics in datasheet.
- A power module, adapted for the commercial GaN HEMT mentioned above and insertion of in-module MLCC C_X and C_Y capacitors, has been designed and manufactured, together with a gate driver board and the DC link capacitor connection. All these units have been modeled by extraction of lumped impedances calculated numerically with ANSYS Q3D software and/or by impedance measurement with a VNA E5061B.
- In order to verify the full model of GaN device and power module in experimental switching test, a test bench has been set up. The precautions for various measurements (voltage / current / EMI noises ...) have been presented. The test units other than power module have been modeled with the aforementioned modeling method as well.
- The switching waveforms in double-pulse test are compared between the simulated ones and the measured ones where they are correctly matched. Specially, the switching voltage V_{DS} 's oscillation has been analyzed and the minimization of its overshoot by in-module C_X capacitors have been studied.
- The CM and DM EMI noises are compared between the simulated ones and the measured ones where they are correctly matched. The influences on CM current of the way the load

resistor connecting have been analyzed – As load resistor connecting to AC terminal, the CM current's magnitude has been increased significantly by the load resistor's CM impedance; As the load resistor connecting to DC terminal, its CM impedance contribute to the noise mode transformation from the DM to the CM. Finally, a parametric study shows an optimal distribution exists between the C_Y capacitor in the power module and in the input filter.

The above realized work lead to a deep understanding the EMI phenomenon within a WBG device based power module. Nevertheless, many aspects can be pursuit for the future research:

Perspectives

- All the methodologies of device modeling and impedance measurement should be scaled to the GaN devices developed by CEA-Leti and the power module of MEGAN project as soon as they are available in samples.
- Switching current measurement. Whether for switching characterization or for overcurrent protection, a current sensor, with both large bandwidth (up to at least ~500MHz in order to measure ~ns dI/dt) and little influence on the miniature power loop (under several nH), is worthy of an reflection on the method of sensing other than electromagnetic way.
- In terms of switching loss characterization, the dynamic on-state resistance of the GaN device has to be taken into account. An extension of the classic device model with this dynamic $R_{DS(on)}$ should be developed.
- The near field radiation by the power loop is to be characterized in case that it results in the dysfunctions of the gate driver above.
- Since the stray capacitance between the power module and the device gate becomes comparable to the C_{GD} of the device, the influence to the switching / EMI noises / robustness of the gate driver are to be evaluated.

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APPENDIX A

SPICE MODEL OF GS66508X

This SPICE model is coded from the mathematical equations in 1.2.1.5 (static part) and in 1.2.2.1 ~ 1.2.2.3 (dynamic part).

```
* GS66508X chip model
.SUBCKT  GS66508X  gate  drain  source

* Coefficient definition
.param  g0=45.2          g1=-0.353          g2=942.9e-6          rdd25=50e-3
        rdd150=150e-3  Temp=25
+      vth=1.7          b=0.15          a1=4.2          a2=4.1
+      acgs0=249e-12
+      acgd0=2e-12     acgd1=309e-12     acgd2=-38     acgd3=24
+      acds0=69e-12     acds1=101e-12     acds2=173     acds3=38
+      acds4=251e-12    acds5=65          acds6=7

* Rdd and Rgg definition
R_dd    drain    dd          {rdd25+(rdd150-rdd25)/(150-25)*(Temp-25)}
R_gg    gate     gg          {1.5}

* Ich definition
G_ICH   dd       source      Value {if (v(dd,source)>0,
+      (log(1.0+exp((g0+g1*Temp+g2*Temp*Temp)*(v(gg,source)-
vth)/(1.0+b*v(gg,source))))*a1*v(dd,source)/(1.0+a2*v(dd,source))),
+      (-log(1.0+exp((g0+g1*Temp+g2*Temp*Temp)*(v(gg,dd)-
vth)/(1.0+b*v(gg,dd))))*a1*v(source,dd)/(1.0+a2*v(source,dd)))) }

```

* Convergence resistance definition

```
R_CDSCONV    dd      source {100Meg}
R_CGSCONV    gg      source {100Meg}
R_CGDCONV    gg      dd      {100Meg}
```

* Cgs definition

```
C_GS      gg      source {acgs0}
```

* Cgd definition

```
C_DG      dd      gg      {acgd0}
E_IDG     d_idg    a_idg    Value={acgd1*acgd3*log(1+exp((-v(dd,gg)+acgd2)/acgd3))}
V_IDG     a_idg    b_idg    0.0
C_IDG     b_idg    c_idg    {1.0e-6}
R_IDG1    c_idg    d_idg    {1e-3}
F_IDG     dd      gg      V_IDG 1.0e6
R_IDG2    a_idg    dd      100Meg
```

* Cds definition

```
C_DS      dd      source {acds0}
E_IDS     d_ids    a_ids    Value={acds1*acds3*log(1+exp((-v(dd,source)+acds2)/acds3))+acds4*acds6*log(1+exp((-v(dd,source)+acds5)/acds6))}
V_IDS     a_ids    b_ids    0.0
C_IDS     b_ids    c_ids    {1.0e-6}
R_IDS1    c_ids    d_ids    {1e-3}
F_IDS     dd      source V_IDS 1.0e6
R_IDS2    a_ids    dd      100Meg
```

.ENDS

Fig. A-1 shows the netlists for the modeling of non-linear capacitance C_{DS} .

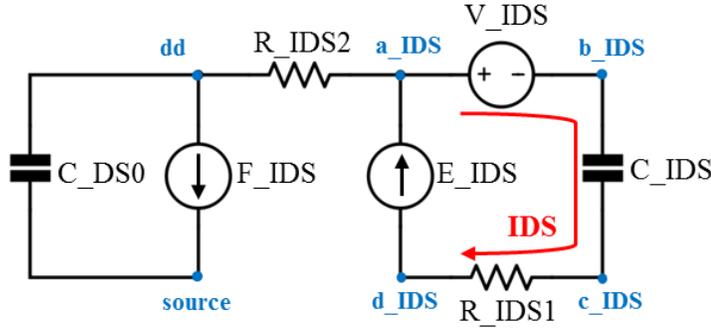


Fig. A-1 : Illustration of netlists of C_{DS} model

The capacitance C_{DS0} represents the initial value of the capacitance C_{DS} ;

A current-controlled current source F_{IDS} is used to model the non-linear capacitive characteristic between dd and $source$. The current passing from dd to $source$ F_{IDS} equals the current passing the voltage source V_{IDS} (from $+$ to $-$) multiplied by $1e6$. The aforementioned current is the current IDS (red arrow in **Fig. A-1**) circling in the loop of $a_{IDS} - b_{IDS} - c_{IDS} - d_{IDS}$. Therefore:

$$F_{IDS} = 1e6 \cdot IDS$$

E_{IDS} is a voltage controlled voltage source and it is applied on the $1\mu F$ capacitance C_{IDS} . Therefore the current passing this capacitance IDS is determined as below:

$$IDS = C_{IDS} \cdot \frac{dE_{IDS}}{dt} = (1e-6) \cdot \frac{dE_{IDS}}{dt}$$

Deducing from the two equations above, the current F_{IDS} can be defined as:

$$F_{IDS} = \frac{dE_{IDS}}{dt}$$

This is the current/charge equation between dd and $source$.

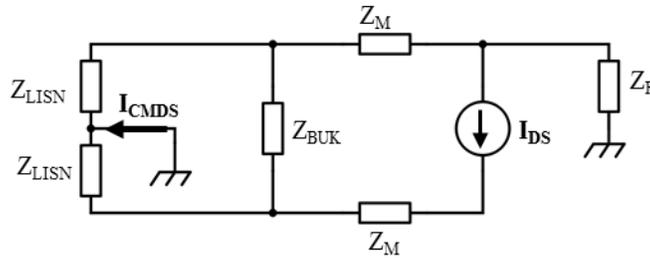
It should be noted that R_{IDS2} is a large resistance ($100M\Omega$) to decouple the two networks; R_{IDS1} is a tiny resistance ($1m\Omega$) to avoid the divergence problem.

APPENDIX B

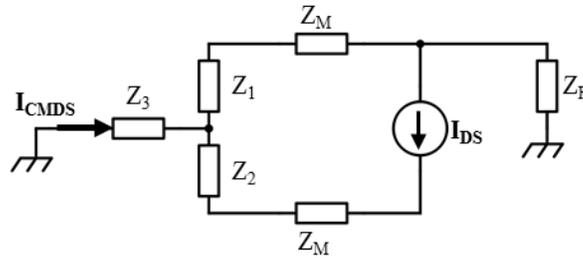
COEFFICIENT CALCULATION OF MODE TRANSFORMATION FROM DM TO CM

With the bare module (c.f. section 4.3.1)

The impedances with the bare SATIE power module resulting in mode transformation from DM noise source to CM noise are shown below (c.f. **Fig. 4-27**).



Transforming the triangle network of Z_{LISN} - Z_{LISN} - Z_{BUK} to a star one, as shown below.



$$Z_1 = Z_2 = \frac{Z_{LISN} \cdot Z_{BUK}}{2 \cdot Z_{LISN} + Z_{BUK}} = \frac{Z_{BUK}}{2 + \frac{Z_{BUK}}{Z_{LISN}}}$$

$$Z_3 = \frac{Z_{LISN}^2}{2 \cdot Z_{LISN} + Z_{BUK}} = \frac{Z_{LISN}}{2 + \frac{Z_{BUK}}{Z_{LISN}}}$$

Since $Z_{LISN} \gg Z_{BUK}$, $Z_{BUK}/Z_{LISN} \approx 0$. Therefore,

$$Z_1 = Z_2 = \frac{Z_{BUK}}{2}$$

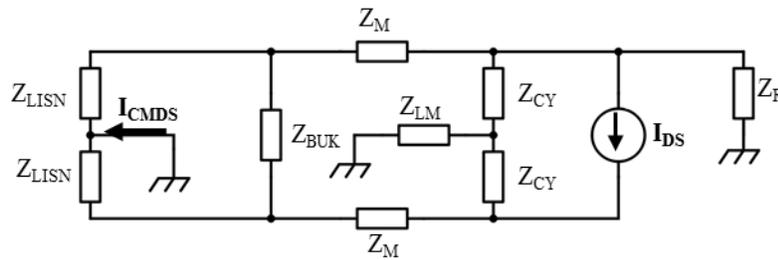
$$Z_3 = \frac{Z_{LISN}}{2}$$

The transformation coefficient k is defined below,

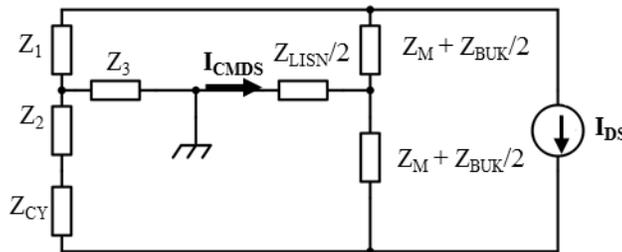
$$k = \frac{I_{CMDS}}{I_{DS}} = \frac{Z_M + \frac{Z_{BUK}}{2}}{Z_R + \frac{Z_{LISN}}{2} + \frac{Z_{BUK}}{2} + Z_M} = \frac{1}{1 + \frac{Z_R + \frac{Z_{LISN}}{2}}{Z_M + \frac{Z_{BUK}}{2}}}$$

With the C_Y capacitors (c.f. section 4.3.2)

The impedances with the SATIE power module with in-module C_Y capacitors resulting in mode transformation from DM noise source to CM noise are shown below (c.f. **Fig. 4-30**). Z_{LM} is the impedance of the module's ground return inductance L_{Module}.



Transforming the triangle networks of Z_{LISN}-Z_{LINS}-Z_{BUK} and Z_{CY}-Z_{LM}-Z_R to star ones. The former has been calculated previously and the latter one is represented as Z₁ to Z₃, as shown below.



$$Z_1 = \frac{Z_{CY} \cdot Z_R}{Z_{CY} + Z_R + Z_{LM}}$$

$$Z_2 = \frac{Z_{CY} \cdot Z_{LM}}{Z_{CY} + Z_R + Z_{LM}}$$

$$Z_3 = \frac{Z_{LM} \cdot Z_R}{Z_{CY} + Z_R + Z_{LM}}$$

Making V the voltage drop of the current source I_{DS} ,

$$V \left(\frac{1}{2 \cdot Z_M + Z_{BUK}} + \frac{1}{2 \cdot Z_{CY}} \right) = I_{DS}$$

$$V \left(\frac{Z_1 + Z_2}{Z_1 + Z_2 + Z_{CY}} - \frac{1}{2} \right) \left(\frac{1}{Z_3 + \frac{Z_{LISN}}{2}} \right) = I_{CMDS}$$

From all equations above, the transformation coefficient k is defined as below:

$$k = \frac{I_{CMDS}}{I_{DS}} = \frac{\left(\frac{1}{1 + \frac{1}{1 + \frac{Z_{LM}}{Z_{CY} + Z_R + Z_{LM}}}} - \frac{1}{2} \right) \left(\frac{1}{Z_{LM} + \frac{Z_{LISN}}{2}} \right)}{\left(\frac{1}{2 \cdot Z_M + Z_{CX}} + \frac{1}{2 \cdot Z_{CY}} \right)}$$