Superconducting silicon on insulator and silicide-based superconducting MOSFET for quantum technologies

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A Roman.

La folie, c'est de faire toujours la même chose et de s'attendre à un résultat différent.

Albert Einstein

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Abstract

Superconducting transport through a silicon MOSFET can open up many new possibilities ranging from fundamental research to industrial applications. In this thesis, we investigate the electric transport properties of a MOSFET built with superconducting source and drain contacts. Due to their advantages in terms of scalability and reproducibility, we want to integrate superconducting materials compatible with CMOS technology, thus exploiting the reliable and mature silicon technology. The idea is to realize a new type of superconducting circuits in a transistor geometry in which a non-dissipative supercurrent flowing through the device from source to drain will be modulated by a gate: a JOFET (Josephson Field Effect Transistor). One important outcome is the realization of superconducting qubits in a perfectly reproducible and mature technology. However, at low temperature and with the reduction of the size of the devices, two antagonistic phenomena appear. The dissipation-free transport of Cooper pairs competes with lossy single-particle processes due to Coulomb interactions. The goal is to understand how these two conflicting properties manifest in such hybrid devices. In this thesis, I studied two different ways of introducing superconductivity in the devices. We deployed a high boron doping and a laser annealing provided by well-controlled out-of-equilibrium doping techniques to make the silicon superconducting. Although highly boron-doped silicon has been known to be superconducting since 2006, superconductivity of SOI, the basic brick of some transistors, was never tested before. We aim at adapting those doping techniques on SOI in order to make it superconducting and to integrate it in transistor-like devices. In a second project, we study source and drain contacts fabricated with superconducting silicides such as PtSi. Such Schottky barrier MOSFETs with superconducting PtSi contacts are elaborated at the CEA/LETI. Measurements at very low temperature revealed the competition between superconductivity and Coulomb interactions and moreover, have brought evidence of superconductivity in PtSi based silicon Schottky barrier MOSFET.

Résumé

L'introduction de la supraconductivité dans des structures de type MOSFET en silicium ouvre de nouvelles perspectives dans la recherche en nanophysique. Dans cette thèse, on s'intéresse aux propriétés de transport électronique au sein d'un MOSFET fabriqué avec des sources et drains supraconducteurs. Afin de garantir la reproductibilité de ces dispositifs, il est important d'intégrer des matériaux supraconducteurs compatibles avec la technologie CMOS exploitant la technologie silicium qui a pour énorme avantage d'être véritablement fiable et mature. L'idée fondamentale est de réaliser un nouveau type de circuit supraconducteur avec une géométrie de type transistor dans lequel un supercourant non dissipatif circulant au sein du dispositif, de la source vers le drain, serait modulé par une tension de grille : un JOFET (Josephson Field Effect Transistor). Une perspective importante est la réalisation d'un qubit supraconducteur grâce à une technologie parfaitement reproductible et mature. Cependant, à très basse température et avec la diminution de la taille des dispositifs, deux phénomènes a priori antagonistes entrent en compétition, à savoir la supraconductivité qui implique un grand nombre d'électrons condensés dans le même état quantique macroscopique et l'interaction Coulombienne qui décrit des processus de transport à une particule. L'intérêt de l'étude est donc de réaliser de tels transistors afin de mieux comprendre comment ce genre de dispositif hybride peut s'adapter à des propriétés opposées. Dans cette thèse, j'ai étudié deux façons d'introduire la supraconductivité dans nos dispositifs. La première option est de réaliser des sources et drains en silicium rendus supraconducteurs par dopage en bore et recuit laser effectué grâce à des techniques de dopage hors-équilibre robustes et bien maîtrisées. Même si la supraconductivité du silicium très fortement dopé en bore est connue depuis 2006 et son état supraconducteur a été très bien caractérisé sur des couches bidimensionnelles, la supraconductivité du SOI, qui est le substrat initial à la base de certains transistors, n'a jamais encore été testée et étudiée. L'objectif est de pouvoir adapter ces techniques de dopage au SOI afin de le rendre supraconducteur et de pouvoir l'intégrer par la suite dans des dispositifs de type MOSFET. La seconde option considérée est la réalisation de source et drain à base de siliciures supraconducteurs tel que le PtSi. Ce siliciure est intéressant du point de vue de sa température critique relativement haute de 1K. D'un point de vue technologique, les MOSFETs à barrière Schottky présentant des contacts en PtSi supraconducteur ont été élaborés au CEA/LETI. Les mesures à très basse température au sein d'un cryostat à dilution ont mis en évidence cette compétition entre la supraconductivité et les effets d'interaction Coulombienne et ont également révélé la supraconductivité dans le MOSFET comportant des contacts en PtSi grâce notamment à l'observation du gap induit dans le dispositif.

Introduction

Context

Quantum computing is a key area of modern research. In a quantum computer, the classical bit is replaced by its quantum counterpart, the qubit. It still contains the 0 and 1 states, but in the quantum realm, these states can be coherently superimposed, and entangled. These trademark quantum traits can massively increase the computational speed for several problems where classical computers remain inefficient. Qubits can be realized with various different types of two-state quantum systems. One of the prime candidates are superconducting qubits. They are attractive since they offer a good scalability, are integrable in existing electric circuits and because their parameters are highly tunable [1], [2]. Moreover, due to continued progress, their coherence time has risen to a level where it is no longer a limiting factor. The most promising among the various superconducting qubits is the transmon, first studied at Yale in 2007 [3], which uses traditional tunnel Josephson junctions with a sufficiently small charging energy. However, in such transmon devices, the control of the qubit energy is obtained by using a magnetic flux threading a superconducting loop containing two tunnel Josephson junctions. Recent experiments at Delft and Copenhagen in 2015 have shown superconducting transmon qubits including a semiconductor nanowire-based Josephson junction [4], [5]. These hybrid devices are referred to as gatemons. They use field effect tunability characteristic for semiconductors to allow qubit control by simply modifying the applied gate voltage and require only one Josephson junction.

In fact, thanks to their specific tunability, semiconductors are one of the key elements in microelectronics. Silicon in particular, ranks as the number one semiconductor element used in virtually all technologies, as it is abundant on earth, and generates low fabrication costs. It is most notably the ingredient of choice for the CMOS technology that allows to make integrated circuits. This technology is reliable and mature, and has been successfully adapted to the modern demands of miniaturization and performance. Since the rise of the CMOS technology in the 1960's, silicon has played an integral role in it. Much more recent is the realization that highly boron-doped silicon is superconducting [6]. This was achieved for the first time in 2006 in Orsay, by the use of controlled out-of-equilibrium doping techniques through laser annealing. The major advantage of superconducting silicon is to combine the interesting properties of silicon and superconductivity in the same device

[7], e.g., to study all silicon superconductor-normal metal (SN) bilayers or SNS junctions [8]. Moreover, this offers the tempting perspective to fabricate all silicon superconducting-semiconductor hybrid devices with transparent interfaces.

The main goal of this thesis is to fabricate and study a new type of superconducting circuit where a dissipationless supercurrent modulated by a gate can flow from source to drain through a transistor, a so-called JOFET. To this end, we want to integrate superconducting materials compatible with the CMOS technology to benefit from its reproducibility. We follow two possible tracks. In one of them, we introduce superconducting silicon in those nanodevices. Here, the key step is to test superconductivity of Silicon On Insulator (SOI) - the standard building block of some transistors - by extending the doping techniques that are established on bulk silicon, to SOI. This work has been done in close collaboration with the CEA/LETI and the IEF (now C2N) in Orsay. The second option is to fabricate source and drain from superconducting silicides such as PtSi [9], [10]. Here, we use Schottky barrier MOSFETs that are manufactured at CEA/LETI, and study their transport properties at very low temperature. In the future, the circuits studied in this thesis could be integrated into a resonator as a gatemon, to read-out and control qubit states.

Contents

This manuscript is divided into four chapters.

The first chapter is dedicated to the theoretical aspects of quantum transport that are relevant for this thesis. After a short review of the history of superconductivity, I introduce in particular Josephson junctions and the role of the interface in hybrid nanostructures. I furthermore introduce the transport physics in a regime where Coulomb interaction is of importance. This second part ranges from Single Electron Transistors (SET) in the Coulomb blockade regime to superconducting circuits with a non-negligible charging energy. This chapter will be used as a basis for the rest of this thesis's manuscript.

In Chapter 2, I present all experimental techniques. I require very low temperature (in order to reach the superconducting phase of the materials used), for which I deploy either a ^{3}He-^{4}He dilution refrigerator or an Oxford PPMS (Physical Properties Measurement System). The fabrication of the contacts in cleanroom will be also described in details. Moreover, I will introduce an important technique used to analyse and characterize the crystalline structures of my samples: the X-ray diffraction.

In the third chapter, I present the experimental results obtained on superconducting boron-doped Silicon-On-Insulator (SOI:B). I start with introducing the two doping techniques which allow to fabricate boron-doped silicon layers, GILD (Gas Immersion Laser Doping) and PLIE (Pulsed Laser Induced Epitaxy). The previous experimental results obtained on Si:B will be afterwards reviewed. In my work, the laser doping techniques will have to be adapted to the SOI. Here, the thin thickness of the top silicon layer of SOI represents the real challenge. At the end of the chapter, two superconducting SOI:B devices in a SQUID and a Hall bar geometry are presented.

In the last chapter, I first want to better understand the fabrication conditions of the PtSi silicide, which is superconducting at low temperature. In this thesis, I study a new superconducting circuit which relies on the traditional MOSFET architecture. In fact, I want to conceive a MOSFET with superconducting PtSi source and drain, which would behave as a Josephson junction with gate voltage tunable properties: a JOFET. The measurements at very low temperature of Schottky barrier MOSFETs with superconducting source and drain will be presented.

Chapter 1

Theoretical background

Contents

1.1 Superconductivity

In this chapter, I want to describe theoretically superconductivity and electronic transport through a quantum dot, since these two effects coexist at very low temperature in the devices I want to fabricate and study.

In general, conduction electrons in a metal experience a Coulomb interaction that is not necessarily weak (in particular because it is long range), invalidating the treatment of electrons as independent particles. However, a single particle picture still holds in the presence of interactions, as was first sketched by Landau [11]. In the Landau-Fermi liquid theory, the electrons of a non-interacting Fermi gas can be mapped to quasiparticles (in a simplified picture "screened" electrons) in the interacting system. Such quasiparticles still retain many of the electron properties, such as, e.g., charge, spin, and momentum. For simplicity, we will therefore refer to them as electrons (and holes, respectively) in the remainder of this thesis.

The conducting properties of the metal arise because of the finite density of states at the chemical potential, which can be computed by the single particle band structure. There are two main contributions to electrical resistance. The first one corresponds to the vibrations of the lattice atoms around their equilibrium positions. This electron-phonon interaction gives rise to a finite electrical resistance even in pure metals. The second is due to the impurities and defects in the lattice, which contribute to create disorder and scattering, causing additional resistance. Finally, we note that in general there is still a residual (screened) electron-electron interaction which may contribute significantly to the resistance at low temperature [12].

When certain metals are cooled at very low temperature, they become superconducting. Superconductivity is a remarkable phenomenon: superconductors can transport electric current without any resistance and thus without any losses. They also behave like a perfect diamagnet, which means that any magnetic field is expelled from the superconductor when the material is in its superconducting state. Explaining superconductivity was without doubt one of the most important achievements of solid state theory of the 20^{th} century. Crucially, the resulting theory allows again for a description in terms of effective single particle excitations. This provides a simple, intuitive access to the physics of superconductivity.

1.1.1 History of superconductivity

The discovery of superconductivity goes back to the Dutch physicist and Nobel laureate Kamerlingh Onnes in 1911 [13]. He discovered that the mercury electrical resistance abruptly vanishes below a certain critical temperature (see Fig.1.1).

Moreover, superconductors are also perfectly diamagnetic. It means that when we apply an external magnetic field, below a certain critical temperature, the superconductor will produce itself a magnetic field counteracting this external field. This property was discovered by Meissner and Ochsenfeld in 1933 and is known as the Meissner effect [14].

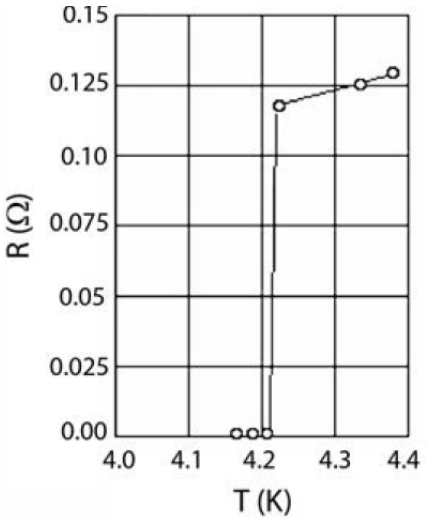


Figure 1.1: Resistance of mercury as a function of temperature exhibiting a superconducting transition at $T_c = 4.2K$, shown by K. Onnes [13].

Theoretically, finding the keys to elucidate the superconductivity was a huge challenge. During decades, physicists failed to develop a theoretical understanding of superconductivity. We will now describe some early phenomenological models trying to explain superconductivity.

In 1935, F. London and H. London gave the first phenomenological theory which was able to describe the two fundamental properties related to superconductivity, the perfect conductivity and diamagnetism [15]. The two London equations are

$$\frac{\partial \vec{J_S}}{\partial t} = \frac{n_S e^2}{m} \vec{E} \tag{1.1}$$

$$\vec{\nabla} \times \vec{J_S} = -\frac{n_S e^2}{m} \vec{B} \ . \tag{1.2}$$

The first London equation is derivated using the equation of motion applied on a density of superconducting electrons n_S, assuming that they are moving without friction. Here, we define $\vec{J_S} = n_S e \vec{v_S}$ the current density per unit of surface, proportionnal to the charge e, the number density n_S and the velocity of superconducting electrons $\vec{v_S}$. This first equation describes the effect of an electrical field on a superconductor. Concerning the second London equation, it can be obtained using Maxwell equations.

By inserting Ampere's law $\vec{\nabla} \times \vec{B} = \mu_0 \vec{J_S}$ into Eq.(1.2), we obtain after some algebra

$$\nabla^2 \vec{B} = -\frac{1}{\lambda_L^2} \vec{B} \ . \tag{1.3}$$

where

$$\lambda_L = \sqrt{\frac{m}{\mu_0 n_S e^2}} \tag{1.4}$$

As a simple example, we consider a one-dimensional geometry, where the superconductor starts at $x = 0$. The solution to Eq.(1.3) is then of the form $\vec{B}(x) = \vec{B}(0)\exp(-x/\lambda_L)$, where $\vec{B}(0)$ is the magnetic field at the boundary, and λ_L is the so called London penetration depth. It describes how far the magnetic field can penetrate into the superconducting material.

The London penetration depth depends on the properties of the superconducting material through the superconducting density n_S. Finally, we note that London's result indicates, that the expulsion of the magnetic field and zero resistance are not two independent phenomena, but that the former is a direct consequence of the latter.

However, it turns out that the London theory was not enough to capture all experimental findings. Most importantly, experiments indicated that the length scale over which $\vec{J}_S$ decayed, did not correspond to the penetration depth λ_L as London predicted. In order to resolve this, Pippard initiated the idea that the local relation between $\vec{J}s$ and $\vec{B}$ of Eq.(1.2) should be replaced by a non-local one [16]. The non-locality enters through a finite coherence length ξ, corresponding to the length scale over which the supercurrent changes, in a spatially varying magnetic field. The coherence length may be estimated by means of the Heisenberg uncertainty principle, $\xi_0 \sim \Delta x \geq \frac{1}{\Delta k}$. Only the electrons with an energy of the order of $k_B T_c$ from the Fermi energy will contribute, since they are the only ones relevant around T_c. Consequently, the wave vector uncertainty of a superconducting wave function can be written as

$$\Delta k \approx \frac{k_B T_c}{\hbar v_F} \tag{1.5}$$

leading to

$$\xi_0 \approx \frac{\hbar v_F}{k_B T_c} \tag{1.6}$$

where ξ_0 is the Pippard coherence length at zero temperature.

In 1950, Ginzburg and Landau (GL) proposed the first macroscopic theory capable of a detailed analysis of superconducting properties, strikingly, again based on phenomenological arguments [17]. The theory is based on the fact that the normal metal-superconductor transition represents a second order phase transition, with an order parameter related to density of superconducting electrons. Ginzburg and Landau provided a form for the free energy that is able to describe this transition,

$$f = \alpha|\psi|^2 + \frac{1}{2}\beta|\psi|^4 + \frac{1}{2m}\left|(-i\hbar\nabla - 2e\vec{A})\psi\right|^2 + \frac{h^2}{8\pi} \tag{1.7}$$

where the constants α and β are to be determined from experiment and dependent on the temperature, m is the mass of the electrons, e is the electron charge, $\vec{A}$ is the vector

potential and $\vec{B}$ is the magnetic field. The order parameter ψ is chosen such that its square amplitude gives the superconducting density, i.e., $\psi = \sqrt{n_S}e^{i\phi}$. The above free energy formula is expanded up to fourth order in ψ, justified for small ψ and $\nabla\psi$. The phase transition occurs at the temperature T_c above (below) which f is minimized by $\psi = 0$ (ψ finite).

Moreover, the GL theory gives rise to the same two characteristic lengths as introduced before, the GL coherence length ξ_{GL} and the penetration depth λ written as follows

$$\xi_{GL} = \frac{\hbar}{\sqrt{2m|\alpha|}} \tag{1.8}$$

and

$$\lambda = \sqrt{\frac{m\beta}{4e^2\mu_0|\alpha|}} \ . \tag{1.9}$$

We have to emphasize though that Pippard's coherence length ξ_0 coincides with the above only for pure superconductors at temperatures far below T_c, since the underlying assumptions of GL are much more general.

Importantly, Abrikosov pointed out in 1957, that the GL theory predicts two types of superconductors, depending on the ratio between ξ_{GL} and λ [18]. We note the ratio κ the Ginzburg-Landau parameter $\kappa = \lambda/\xi_{GL}$ distinguishing the two types. For $\kappa < \frac{1}{\sqrt{2}}$, the superconductor is a type I. And for $\kappa > \frac{1}{\sqrt{2}}$, the superconductor is a type II.

These two types exhibit a very different behavior with respect to the magnetic field, as shown in Fig.1.2. We can state that when the magnetic field becomes strong enough, there is a point at which the superconductor is no longer capable to produce a counteracting magnetic field and this will indeed induce the penetration of the external field in the superconducting material.

Firstly, when the applied field rises above a certain critical value H_c, a type I superconductor sees his superconductivity abruptly destroyed and experiences a complete penetration of the external magnetic field. A type II superconductor, on the other hand, exhibits a intermediary state in which the external field penetrates the superconductor in shape of vortices, appearing above a certain critical field H_{c1}. No superconducting state exists in the vortices, but only outside. Above a higher critical field H_{c2}, superconductivity is destroyed and the material becomes normal.

Up to now, we have described general features of superconductors thanks to the first phenomenological theories dedicated to them. In 1950, Fröhlich made a first step towards a microscopic theory, through the observation that the vibrations of the crystalline lattice, that is to say the electron-phonon interaction, may create an attraction between electrons, and could be for this reason the cause of superconductivity [19]. Few years later, in 1956, Cooper pointed out that as soon as there is a tiny attraction between electrons, the Fermi

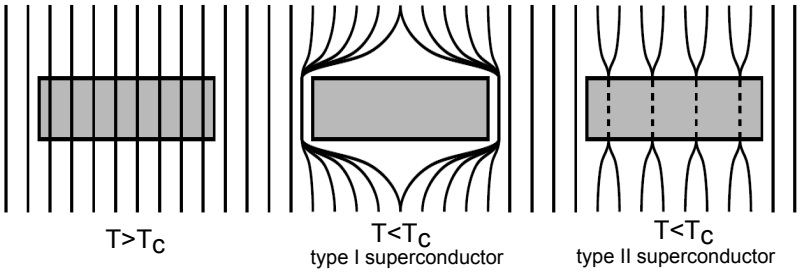


Figure 1.2: Sketch of magnetic flux lines through a normal metal at $T > T_c$, a type I superconductor at $T < T_c$ and a type-II superconductor at $T < T_c$. The dashed lines inside the superconductor represent the vortices.

sea exhibits an instability [20]. This culminated into the seminal microscopic theory of Bardeen, Cooper and Schrieffer (BCS) in 1957, who were awarded with the Nobel Prize in 1972 [21]. In the following, we reiterate in more detail the cornerstones of this theory.

Usually, the interaction between electrons is repulsive, due to the Coulomb interaction between two negative charges. In fact, the interaction between two electrons via the exchange of a phonon, can lead to an attractive interaction. The idea is that a first electron leads to a deformation of the positively charged ions in its surroundings, to which a subsequent electron is attracted, see Fig.1.3. The two electrons with opposite momentum and spin (in the conventional theory) form a so called Cooper pair.

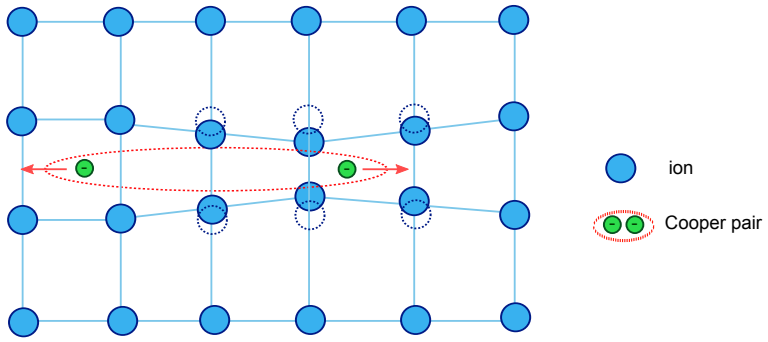


Figure 1.3: Illustration of the formation of a Cooper pair. The Cooper pair, composed of two electrons of opposite spins, is joined by a phonon.

Because the energy of a Cooper pair is lower than that of two separated electrons, the Fermi sea becomes unstable. Instead, the new ground state consists of a condensate of Cooper pairs - a macroscopic, many-body quantum state, with a phase φ. The formation of the condensate goes hand in hand with the emergence of an energy gap. The energy gap corresponds to the minimum amount of energy that is needed to excite the superconductor. Within the framework of the BCS theory, one can understand in a simplified picture, why the supercurrent, carried by Cooper pairs, is dissipation-free. Once in the condensate, the

electrons have - thanks to the energy gap - no states available, into which they can be scattered, allowing for a current without losses.

Twice the energy gap Δ is precisely the energy required to break a Cooper pair. The BCS theory gives the relation between the gap at zero temperature $\Delta(0)$ and the critical temperature T_c

$$\Delta(0) = 1.76 k_B T_c \tag{1.10}$$

where k_B is the Boltzmann constant.

The BCS theory is the first to predict the precise temperature dependence of the superconducting gap for all temperatures, as it is shown in Fig.1.4. For temperatures close to the critical one T_c, it can be described by the formula

$$\frac{\Delta(T)}{\Delta(0)} \approx 1.74\sqrt{1 - \frac{T}{T_c}} \, . \tag{1.11}$$

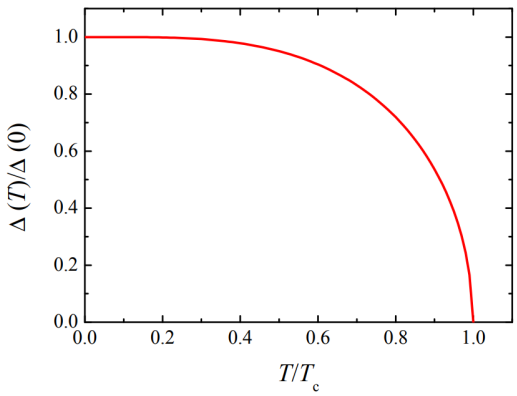


Figure 1.4: Temperature dependence of the normalised BCS gap $\Delta(T)/\Delta(0)$.

Rigorously speaking, this result is only valid in the weak coupling regime, but it gives a good approximation in many cases. In fact, the result coincides with experimental measurements for typical superconductors such as lead, tin and indium [22].

Finally, within the BCS theory, the coherence length corresponds to the Cooper pairs' characteristic size. At zero temperature, it is given by [23]

$$\xi = \frac{\hbar v_F}{\pi \Delta(0)} \tag{1.12}$$

where v_F is the electron velocity at the Fermi level. With the above relation Eq.(1.10) between $\Delta(0)$ and T_c, we can easily see that the BCS coherence length coincides with Pippard's estimate for temperatures much below T_c.

In the next sections of this manuscript, some important characteristics of superconducting materials will be used and their notations are specified here. These essential parameters

are the superconducting gap Δ, the critical temperature T_c, the critical magnetic field H_c, or H_{c1} and H_{c2} (whether we consider a type I superconductor or a type II), the coherence length ξ corresponding to the characteristic size of a Cooper pair and the London penetration depth λ_L denoting the distance up to which a magnetic field can penetrate a superconductor.

1.2 Hybrid Nanostructures

1.2.1 Andreev reflection and proximity effect

1.2.1.1 Andreev reflection and coherence

The study of the interplay of a superconductor with a non-superconducting material (for instance a metal) is a central topics of modern research. The recent considerable development of nanofabrication technologies allowing to create hybrid nanostructures, added to the importance of the involved quantum effects, have created a huge interest and have also permitted major advances [24], [25], [26]. There remain however some highly relevant open questions. For instance, the study of superconductor/ferromagnet hybrid structures open new points related to the competition and the coexistance of the two phenomena superconductivity and ferromagnetism [27], [28].

Let's consider an interface between a superconductor S and a normal metal N. Within the superconductor, there are no available single particle states at energies below the gap Δ. This fact can be seen in the BCS density of states,

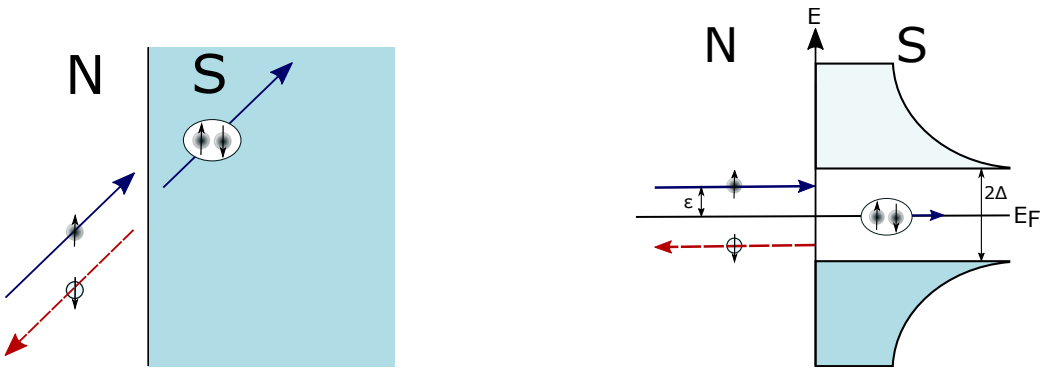
$$\rho_S = \rho_N \left[\frac{\varepsilon}{\sqrt{\varepsilon^2 - \Delta^2}} \right] \tag{1.13}$$

with $\varepsilon > 0$ and ρ_N the density of states in the normal state at the Fermi energy.

It is nonzero, only for $\varepsilon > \Delta$. This means that an electron of energy $|\varepsilon| < \Delta$ (with $|\varepsilon| = E - E_F$ the excitation energy) coming from the normal metal, cannot enter the superconductor. Subgap charge transport can nonetheless occur, when considering second order processes.

The basic coherent mechanism providing electronic transport below the gap at SN interfaces is the Andreev reflection. In 1956, Andreev showed that within this process, an incoming electron from the normal metal can flow through the superconductor by forming a Cooper pair with a second electron extracted from the metal. The missing charge $-e$ is retro-reflected as a hole in the metal, see Fig.1.5 [29]. Thus, it means that the Andreev reflection has the peculiar feature to allow, in a coherent way, the conversion of a dissipative electrical current held by electrons in the normal metal to a dissipationless supercurrent carried by Cooper pairs in the superconductor.

Let's now be more specific about the characteristics of the incident electron and the reflected hole in this process. For clarity, we introduce now the indices e and h corresponding



(a) (b)

Figure 1.5: Sketch of the Andreev reflection in the normal metal-superconductor interface in real space (a), and the corresponding energy diagram (b)

respectively to the incident electron and the reflected hole. We denote that the reflected hole is the perfect time-reversed partner of the incident electron within this process.
Consequently, an incoming electron from the normal metal with a energy $E_e = \varepsilon + E_F$, a momentum $k_e = k_F + \frac{\delta k}{2}$ and a spin $S = \sigma$ is retro-reflected as a hole with opposite momentum and spin, that is to say $k_h = k_F - \frac{\delta k}{2}$ and $S = -\sigma$ at the energy $E_h = -\varepsilon + E_F$. This leads to the generation of a Cooper pair in the superconductor. In this process, the involved energies respect the energy conservation principle.
Without any surprise, the Andreev reflection is of course time-reversible, meaning that the inverse process is also possible. When a hole reaches the SN interface, a Cooper pair is removed from the superconductor, and an electron is retro-reflected.

The difference between the wave vectors of the electron and hole is

$$\delta k = k_e - k_h = \frac{2\varepsilon}{\hbar v_F} \tag{1.14}$$

where $v_F = \frac{\hbar k_F}{m}$ corresponds to the Fermi velocity.

In addition, the reflection induces a phase change to the reflected hole

$$\phi_i = \varphi - \arccos\left(\frac{\varepsilon}{\Delta}\right) \ . \tag{1.15}$$

As mentioned above, φ corresponds to the macroscopic superconducting phase and ε is the energy of the incoming electron above the Fermi level. Depending on the value of ε, we can now distinguish two different cases.

For $\varepsilon = 0$, the retro-reflection is perfect, in the sense that both electron and hole have exactly the same wave vector. Thus, the reflected hole tracks the very same path of the incident electron. As a result, there is no dephasing induced by the propagation in

the material, the global phase difference $\delta\phi = \phi_i$ remains constant in time. In this case, electron and hole form a so called Andreev pair, whose coherence is only limited by the individual phase coherence length L_φ.

For $\varepsilon \neq 0$, the two wave vectors are no longer the same and as we move away from the SN interface, a phase-shift induced by the propagation ϕ_p appears. After a time τ_ε, the propagation-induced phase-shift ϕ_P is equal to

$$\phi_p = \frac{2\varepsilon\tau_\varepsilon}{\hbar} \ . \tag{1.16}$$

Consequently, during an Andreev reflection process, the phase-shift between the incident electron and the retro-reflected hole $\delta\phi = \phi_i + \phi_p$ is due to two distinct contributions: the first one is induced directly by the Andreev reflection and the second involves the propagation and exhibits an important dependence on the material properties (ballistic or diffusive material).

In the diffusive case, the diffusion constant of the normal metal D_N has to be taken into account. Hence, in a disordered metal, the coherence of the Andreev pairs is limited by the length

$$L_\varepsilon = \sqrt{D_N\tau_\varepsilon} = \sqrt{\frac{\hbar D_N}{\varepsilon}} \ . \tag{1.17}$$

We deduce that the coherence of the Andreev pairs can be easily weakened by multiple parameters, such as the applied voltage ($\varepsilon = eV$) or the temperature ($\varepsilon = 2\pi k_B T$). Following Eq.(1.17) and substituting ε by $2\pi k_B T$, one obtains the thermal length in the diffusive limit

$$L_T = \sqrt{\frac{\hbar D_N}{2\pi k_B T}} \ . \tag{1.18}$$

If we now consider a sample of length L, it is possible to define the energy window within which an Andreev pair keeps its coherence in the overall sample, using Eq.(1.17). This energy window is the so called Thouless energy and is given by

$$E_{Th} = \frac{\hbar D}{L^2} \ . \tag{1.19}$$

Finally, the ultimate limite for the coherence length of Andreev pairs is defined by the electronic phase coherence length L_φ. It corresponds to the length travelled by the electron before its initial phase turns out to be randomized. Experimental studies in diffusive metal nanostructures provide estimations for the phase coherence length, it can vary between tens of nanometers up to micrometers, depending on the material purity and the temperature.

1.2.1.2 Proximity effect

Until now, we have considered that the SN interface was ideal and that the mechanism of Andreev reflection was occuring precisely at the interface between the superconductor and

the metal. However, these assumptions are not always adequate with real systems. Actually, an electrical contact between a normal metal attached through a highly transparent interface to a superconductor brings major changes in the transport properties of the two materials.

If a superconductor is in contact with a normal metal, an Andreev reflection can generate an Andreev pair in the metal, which can keep its coherence over a length L_ε in the latter, as it has been explained before. It is precisely this coherence which modifies the normal properties of the metal by inducing superconductivity into it. This phenomenon is called the proximity effect.

The formation of Cooper pairs is even possible in the normal metal within a short distance from the interface $\xi_N = \sqrt{\frac{\hbar D_N}{\Delta}}$, which corresponds to the penetration length of the Cooper pairs in metal.

In the same way, the superconducting properties are modified in proximity of the metal. The superconducting gap is weakened and electrons can penetrate the superconductor within the distance $\xi_S = \sqrt{\frac{\hbar D_S}{\Delta}}$, leading to the phenomenon of inverse proximity effect.

Theoretically, the Bogoliubov-de Gennes equations are used to describe the quasiparticle excitations in a superconductor and to determine their wavefunctions throughout the travelled structure [30]. An interesting feature of the Bogoliubov-de Gennes equations is that they suit for the description of systems with a spatially varying gap, including SN junctions since a normal metal can be easily described by setting Δ to 0.

Writing the Schrödinger equations for an electron and hole excitation as one matrix equation, we obtain the Bogoliubov-de Gennes equations

$$\begin{pmatrix} H_0 & \Delta(x) \\ \Delta(x)^* & -H_0^* \end{pmatrix} \quad \begin{pmatrix} \psi_e(x) \\ \psi_h(x) \end{pmatrix} = \varepsilon \begin{pmatrix} \psi_e(x) \\ \psi_h(x) \end{pmatrix} \tag{1.20}$$

where $\varepsilon = E - E_F$ is the excitation energy of the quasiparticle (electron (hole) above (below) the Fermi energy E_F) and H_0 is the single particle Hamiltonian, written as

$$H_0 = \frac{p^2}{2m_{eff}} + V(x) - E_F \tag{1.21}$$

with V(x) an additional confining potential.

The wave-functions consist of two components corresponding to the electron part $\psi_e(x)$ and the hole part $\psi_h(x)$ of the excitations of the superconductor. $\Delta(x)$ is called the pair potential, giving the coupling between the electron and hole wave-function $(\psi_e(x), \psi_h(x))$.

Directly from the Bogoliubov-de Gennes equations, it is obvious to state that for $\Delta(x) = 0$, the equations decouple and quasiparticles are only described as in a normal metal. We can deduce that the coupling between electron-like and hole-like excitations, which is characteristic for superconductivity, only occurs when $\Delta(x)$ is finite.

Summarizing, the coherence length of an Andreev pair L_ε is found to have two limits, the electronic phase coherence length L_φ as it was mentioned before, and the penetration length of Cooper pairs in metal ξ_N exhibiting the proximity effect. We report the characteristic lengths and their corresponding energies in Fig.1.6.

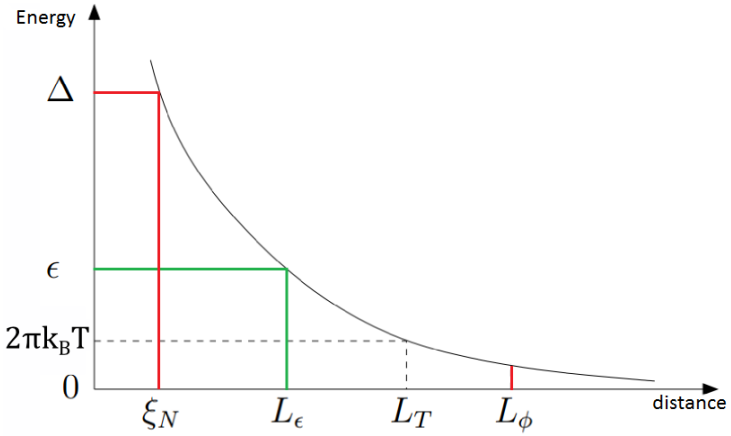


Figure 1.6: Relation between characteristical lengths and energies. x gives the distance to the superconducting material. The two boundary lengths are L_φ and ξ_N. The thermal length L_T gives the pairs penetration at finite temperature.

1.2.2 Role of the SN interface

The quality and the transparency of the interface between a normal metal and a superconductor has a significant influence on the Andreev reflection. So far, the SN interface has been considered as ideal and the Andreev reflection was considered to be the only mechanism for an incoming electron with $\varepsilon < \Delta$ at the interface. Nevertheless, in reality, the interface is never perfectly clean and scattering is induced by any defects or impurities. In fact, other mechanisms are also possible at the SN interface, depending on the energy of the incident electron and the transparency of the interface, see Fig.1.7(a):

- A- Andreev reflection, which corresponds to a retro-reflection of an electron as a hole, with a probability A
- B- Specular reflection, which is a simple reflection of an electron as an electron, with a probability B
- C- Transmission, corresponding to the transfer of an electron as an electron-like quasiparticle, with a probability C
- D- Andreev transmission, the transfer of an electron as a hole-like quasiparticle, with a probability D.

The effect of the interface transparency on the electronic transport through a SN junction has been discussed first by Blonder, Tinkham and Klapwijk (BTK) in 1982 [31]. Solving the Bogoliubov-de Gennes equations, they calculated the conductance of a simplified ballistic single-channel SN system with an arbitrary interface transparency considering the above elementary processes.

In this BTK model, the parameter Z describes the height of the barrier at the interface, the barrier can be also expressed as a repulsive potential U. This two parameters are simply connected by the relation $Z = U/\hbar v_F$. The transparency of the barrier is then given by $T = 1/(1+Z^2)$. Consequently, we can deduce that for $Z = 0$, the barrier is fully transparent and the interface is perfect. On the other hand, $Z >> 1$ is associated to the tunnel limit of an SIN interface. The probabilities of the four processes occuring at the interface are closely depending on the barrier height Z, as it is represented in Fig.1.7(b).
Due to probability conservation, the sum of the probabilities equals to 1 : $A+B+C+D = 1$.

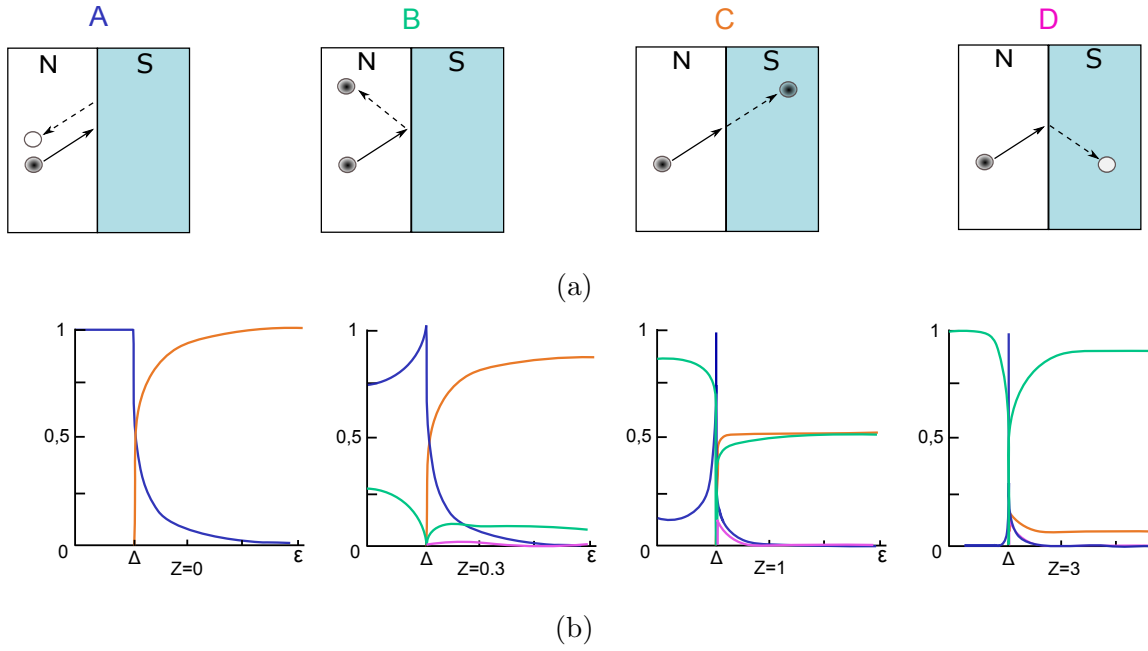


Figure 1.7: (a) Schemes of the four mechanisms coming into play at the SN boundary, (b) the probability of each of them is strongly correlated to the parameter Z corresponding to the barrier height.

The total current flowing from the normal metal to the superconductor with a finite bias V reads

$$I_{NS} = \frac{G_0}{e}\int_{-\infty}^{+\infty}[1 + A(\varepsilon,Z) - B(\varepsilon,Z)][f_0(\varepsilon - eV) - f_0(\varepsilon)]\mathrm{d}\varepsilon \tag{1.22}$$

where $A(\varepsilon,Z)$ and $B(\varepsilon,Z)$ are the probabilities for Andreev reflection and simple reflection, respectively. The Fermi-Dirac distribution functions in the superconductor and the metal are given as $f_0(\varepsilon)$ and $f_0(\varepsilon - eV)$. We will define G_0 shortly.

From Eq.1.22, we can compute the differential conductance through a SN interface :

$$\frac{\partial I_{NS}}{\partial V} = \frac{G_0}{e}\int_{-\infty}^{+\infty}[1 + A(\varepsilon,Z) - B(\varepsilon,Z)]\frac{\partial f_0}{\partial V}(\varepsilon - eV)\mathrm{d}\varepsilon \ . \tag{1.23}$$

Since $\frac{\partial f_0}{\partial V}(\varepsilon - eV) = -e\frac{\partial f_0}{\partial \varepsilon}(\varepsilon - eV)$, we obtain

$$G_{NS} = \frac{\partial I_{NS}}{\partial V} = G_0\int_{-\infty}^{+\infty}[1 + A(\varepsilon,Z) - B(\varepsilon,Z)]\left(\frac{-\partial f_0}{\partial \varepsilon}(\varepsilon - eV)\right)\mathrm{d}\varepsilon \ . \tag{1.24}$$

We now specify the prefactor G_0. Replacing the superconductor by a normal metal

$$I_{NN} = I_{NS}(\Delta \to 0) \tag{1.25}$$

we reveive,

$$I_{NN} = \frac{G_0}{e}T\int_{-\infty}^{+\infty}(f_0(\varepsilon - eV) - f_0(\varepsilon))\mathrm{d}\varepsilon = G_0TV \tag{1.26}$$

because $A \to 0$ and $B \to 1 - T$ for $\Delta \to 0$.

Hence, we get immediately the differential conductance G_{NN},

$$G_{NN} = \frac{\partial I_{NN}}{\partial V} = G_0T \ . \tag{1.27}$$

Finally, we can deduce the prefactor G_0

$$G_0 = \frac{G_{NN}}{T} = G_{NN}(1 + Z^2) \ . \tag{1.28}$$

By reporting the Eq.1.28 in Eq.1.24, we obtain the final expression for the differential conductance through a SN junction

$$G_{NS} = G_{NN}(1 + Z^2)\int_{-\infty}^{+\infty}[1 + A(\varepsilon,Z) - B(\varepsilon,Z)]\left(\frac{-\partial f_0}{\partial \varepsilon}(\varepsilon - eV)\right)\mathrm{d}\varepsilon \ . \tag{1.29}$$

It appears that the differential conductance of the SN junction is proportional to $[1 + A(\varepsilon,Z) - B(\varepsilon,Z)]$. This relation allows to understand the evolution of the interface behavior mainly as a function of the barrier height Z.

Without any barrier ($Z = 0$), the barrier transparency is ideal and $A = 1$ for $\varepsilon < \Delta$: the injected electron can only be Andreev reflected as a hole and the simple reflection vanishes, $B = 0$. It means that the Andreev reflection process doubles the charge transfer in the SN junction as compared to a normal system, that is to say $(1 + A(\varepsilon) - B(\varepsilon)) = 2$ for $\varepsilon < \Delta$, see Fig.1.8

For non-transparent interfaces ($Z > 0$), there is a probability that electrons are Andreev reflected but due to the presence of the barrier at the interface, electrons can now undergo

simple reflection. In the subgap regime, since an electron is either Andreev reflected or simply reflected, $A + B = 1$ has to be respected. Hence, an increase of simple reflection induces a decrease of the Andreev reflection.

When $Z >> 1$, the transparency of the barrier becomes very poor and almost no transport occurs at $\varepsilon < \Delta$, $A \approx 0$ and $B \approx 1$. Above the gap on the other hand, $\varepsilon > \Delta$, the one-particle processes are the only ones to survive, $A \approx 0$ and $B \approx 1 - \frac{1}{Z^2}\frac{\varepsilon}{\sqrt{\varepsilon^2-\Delta^2}}$, where B has been expanded up to first order in $1/Z^2$. Inserting this into Eq.(1.29), we see that the conductance is now proportionnal to the density of states of the superconductor.

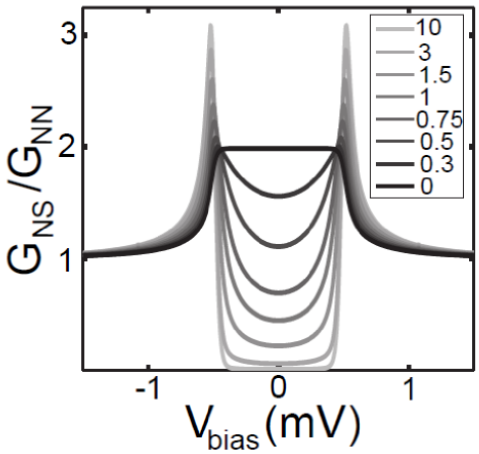


Figure 1.8: Typical conductance-voltage characteristic as a function of the parameter Z. For $Z = 0$ ($T = 1$), the conductance is doubled under the gap. For $Z >> 1$ ($T << 1$), the tunnel limit is reached. The parameters here are $\Delta = 500\mu$eV and $T = 200$mK (reproduced from [32]).

1.3 Josephson effect

1.3.1 Josephson equations

Tunneling of particles through classically forbidden regions is one of the most remarkable features of quantum mechanics. Even if tunneling is a purely quantum mechanical effect, it can be observed at a macroscopic scale in certain systems.

Josephson predicted in 1962 that a supercurrent can flow through a thin insulating barrier connected to two superconducting reservoirs [33]. This is called the Josephson effect and refers to the macroscopic tunneling of Cooper pairs. While the original prediction was based on the assumption of a weakly transmitting barrier, it has later been pointed out that the Josephson effect persists when using small but highly transparent interface [34]. This effect actually occurs whenever two superconducting electrodes are separated by a so

called weak link. This weak link was initially an insulator, but it can also be a normal metal, a semiconductor or a physical constriction as well, see Fig.1.9.

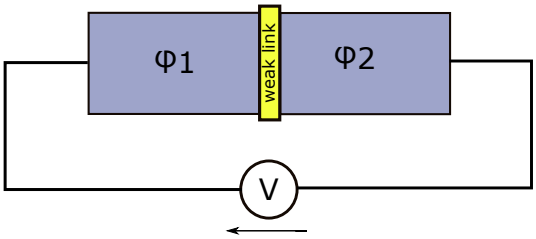


Figure 1.9: Schematic diagram of a Josephson junction composed of two superconducting reservoirs separeted by a weak link, connected to a DC bias voltage V.

Theoretical calculations based on the existence of macroscopic wavefunctions result in two main equations, corresponding to the so called DC and AC Josephson effects. The first Josephson equation provides a simple relation between the supercurrent flowing through the junction I_s and the phase difference between the two superconductors $\Phi = \varphi_1 - \varphi_2$, at zero applied voltage,

$$I_s = I_c \sin(\Phi) \tag{1.30}$$

where I_c is the critical current of the junction. It is affected by temperature and represents the maximum current that can be carried by the supercurrent.

For tunnel junctions, the precise temperature dependence of the critical current is given by the Ambegaokar-Baratoff formula [35]. Using the BCS theory, they derived a relation between the critical current and the BCS gap. For $T = 0$, this can be written as follows,

$$I_c = \frac{\pi \Delta(0)}{2eR_N} \tag{1.31}$$

with $\Delta(0)$ the BCS gap at zero temperature and R_N the normal state resistance.

Importantly, we note that the critical current of a Josephson junction strongly depends on its geometry since the resistance of a barrier is inversely proportional to its cross section S, i.e., $R_N \sim 1/S$.

The second Josephson equation states that a DC voltage V applied across the junction leads to a time-dependent phase difference. This is the AC Josephson equation,

$$\frac{d\Phi}{dt} = \frac{2eV}{\hbar} \ . \tag{1.32}$$

Combining Eq.(1.30) and Eq.(1.32), one deduces that a non-zero potential V induces an alternating supercurrent flowing through the junction

$$I_s = I_c \sin(2\pi f_J t + \Phi(0)) \tag{1.33}$$

of frequency $f_J = \frac{2eV}{h} = 483.6.10^{12} V(Hz)$. This voltage-dependent frequency is called the Josephson frequency.

Josephson was awarded with the Nobel Prize in 1973 for his work on the Josephson effect. The DC Josephson effect was demonstrated experimentally for the very first time in 1963 by Anderson and Rowell [36].

1.3.2 The Josephson energy

Theoretically, the Josephson effect can be described by a simple effective Hamiltonian. To show this, we have to determine an energy associated with the exchange of Cooper pairs across the junction.

Using the results we presented before for the voltage V and the current I_s flowing through a Josephson junction (Eq.(1.30) and Eq.(1.32)), we can derive an expression for the total energy of a Josephson junction

$$E(t) = \int_0^t V I_s dt = \frac{\phi_0}{2\pi} \int_0^t I_c \sin(\Phi) d\Phi = \frac{\phi_0 I_c}{2\pi}(1 - \cos\Phi) \tag{1.34}$$

where $\phi_0 = h/2e$ is the flux quantum.

Finally, we obtain

$$E(t) = -E_J \cos\Phi + K \tag{1.35}$$

where K is a constant that we can set to zero and E_J is the so called Josephson energy $E_J = \frac{\phi_0 I_c}{2\pi}$, giving the coupling of the system.

Since the Josephson junction is a link between two superconductor, it also acts as a capacitor with an intrinsic capacitance C_J. The inductance of the junction is given by

$$L_J = \frac{\phi_0}{2\pi I_c \cos\Phi} \ . \tag{1.36}$$

The capacitance added to the nonlinear inductance make the junction a nonlinear LC oscillator.

1.3.3 The RCSJ-Model

So far, we have considered ideal Josephson junctions either in the absence or presence of a voltage, allowing a supercurrent of Cooper pairs to flow through them. However, in general both quasiparticles and Cooper pairs can tunnel through a barrier of a Josephson junction.

Actually, a model capable of describing real Josephson junctions should take into account the capacitance between the two superconducting reservoirs. Moreover, thermally excited quasiparticles in the reservoirs can propagate across the barrier resulting in a quasiparticle resistance.

In order to describe this, Stewart [37] and McCumber [38] introduced the Resistivity and Capacitively Shunted Junction model, shortly called the RCSJ-model in 1968. It models the real Josephson junction as three parallel circuits: a capacitance C to simulate the

geometrically induced capacitance between the reservoirs of the junction, a quasiparticle resistance R and the Josephson junction itself in its ideal version. Within this approach, the equivalent circuit of a real Josephson junction in the framework of the RCSJ-model is schematically illustrated in Fig.1.10.

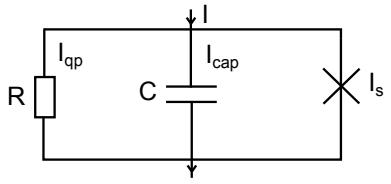


Figure 1.10: Equivalent circuit of the RCSJ-model. The real Josephson junction is modeled as an ideal Josephson junction in parallel to a capacitance C formed by the reservoirs and a resistance R describing the dissipation due to the quasiparticle tunneling.

According to Kirchhoff's law, the total current flowing through the circuit is the sum of the currents flowing through the three branches, that is to say, the supercurrent $I_s = I_c \sin(\Phi)$, the quasiparticle tunneling current $I_{qp} = V/R$ and the current taking into account the capacitance of the Josephson junction $I_{cap} = C\frac{dV}{dt}$.

Hence, the total current across the junction reads

$$I = I_c \sin(\Phi) + \frac{V}{R} + C\frac{dV}{dt} \ . \tag{1.37}$$

By substituting the voltage V across the junction using the second Josephson equation (Eq.(1.32)), one obtains

$$I = I_c \sin(\Phi) + \frac{1}{R}\left(\frac{\phi_0}{2\pi}\right)\frac{d\Phi}{dt} + C\left(\frac{\phi_0}{2\pi}\right)\frac{d^2\Phi}{dt^2} \ . \tag{1.38}$$

By defining the plasma frequency of the junction $\omega_p = \sqrt{2eI_c/\hbar C}$, the reduced time $\tau = \omega_p t$, the quality factor $Q = \omega_p RC$ and the Stewart-McCumber parameter $\beta_c = Q^2$, we get the dimensionless equation

$$\frac{I}{I_c} = \sin(\Phi) + \frac{1}{Q}\frac{d\Phi}{d\tau} + \frac{d^2\Phi}{d\tau^2} \ . \tag{1.39}$$

We directly note the analogy between this equation and the one associated to the movement of a classical particle with a mass $\left(\frac{\hbar}{2e}\right)^2 C$ in a potential $U(\Phi) = -E_J \cos(\Phi) - \left(\frac{\phi_0}{2\pi}\right) I\Phi$, where E_J is the Josephson energy.

Results and discussion

The periodic term of the potential U may lead to the presence of a hysteresis in the I(V) characteristics. By considering the analogy with the classical particle motion, depending on its velocity, the particle can be retained or not in the low-potential valleys of the potential,

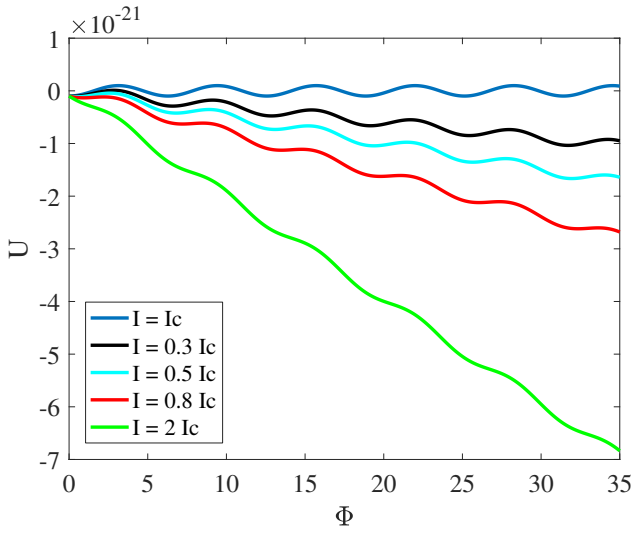


Figure 1.11: Potential U plotted as a function of the phase difference Φ for different currents I.

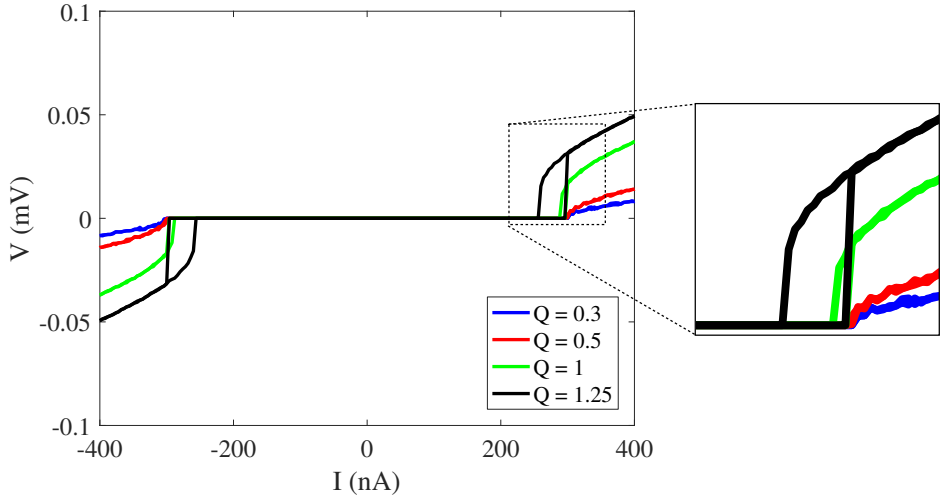


Figure 1.12: Numerical simulations of the RCSJ model realized with Matlab for a junction with a critical current I_c of 300 nA, a resistance R of 200Ω and a capacitance of 1.10^{-13}F. The I(V) curves have been plotted for different values of the quality factor Q, showing two different behaviors: the absence or presence of a hysteresis. The code of the program used to generate the curves is presented in Appendix A.

as seen in Fig.1.11. The particle getting stuck in a local minimum corresponds to the situation where the DC Josephson junction is operated. The AC Josephson effect will occur otherwise.

In the case of $I > I_c$, as observed on Fig.1.11 with the green curve, the particle is

not blocked inside a low-potential valley, in fact it will "fall". By reducing I, this particle might keep falling even if I gets smaller than I_c: this is the origin of the hysteresis visible on Fig.1.12.

The value of the quality factor Q allows to determine the shape of the current-voltage curves around the critical current I_c, i.e., the presence or absence of an hysteresis. Two regimes are possible depending on Q. For $Q < \frac{1}{2}$, no hysteresis is observed in the I(V) characteristics meaning that the transition between the superconducting state and the normal one is smooth; the junction is overdamped. On the other hand, for $Q > \frac{1}{2}$, the transition is abrupt and a hysteresis is to be noticed; the junction is underdamped.

1.3.4 Application of the Josephson effect: DC SQUID

The discovery of the Josephson effect opened not only a new major chapter of physics but also offers rich perspectives for a wide variety of applications [39]. We focus now on new effects appearing when a magnetic flux is applied on a Josephson junction. The new system that we consider is made of a superconducting ring interrupted by two Josephson junctions set in parallel; it is called a Superconducting Quantum Interference Device (SQUID). The scheme of a SQUID is presented in Fig.1.13. SQUIDs are usually used for very sensitive magnetic flux measurements [40].

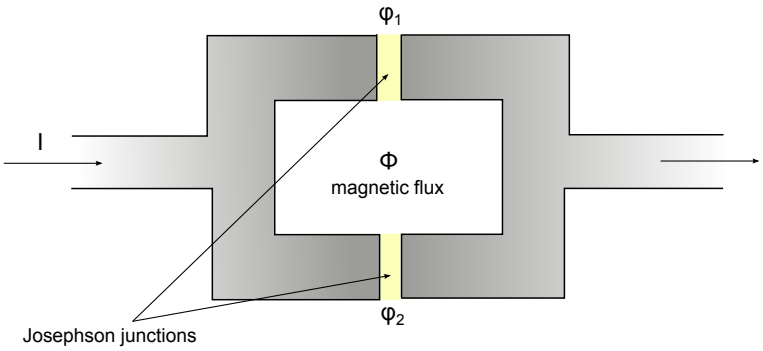


Figure 1.13: A schematic figure of a SQUID: two Josephson junctions in parallel forming a loop.

The principle of a SQUID is based both on the Josephson effect and on the quantization of the magnetic flux through a superconducting loop. All the Cooper pairs inside the loop have the same wave function, and the phase difference Φ through a closed loop is defined modulo 2π.

In 1959, Aharonov and Bohm [41] predicted that this phase difference Φ is proportional to the magnetic flux ϕ crossing the closed loop. Hence, we get

$$\Phi = \frac{2\pi\phi}{\phi_0} = 2n\pi \tag{1.40}$$

with ϕ_0 the flux quantum and n a integer.

We deduce directly from Eq.(1.40) the quantization of the magnetic flux through a superconducting loop

$$\phi = n\phi_0 \tag{1.41}$$

We now aim at deriving the maximum current I_c that can flow across a SQUID and determining its dependence with the applied magnetic flux.

The total current across the SQUID depends on the phase difference of each Josephson junction Φ_1 and Φ_2 and can be written as the sum of the currents flowing through the two junctions,

$$I = I_1 + I_2 = I_{c1}\sin(\Phi_1) + I_{c2}\sin(\Phi_2)\ . \tag{1.42}$$

To simplify the calculations, we here consider a SQUID with two identical Josephson junctions, i.e., $I_{c1} = I_{c2} = I_{c0}$, one obtains

$$I = 2I_{c0}\cos\left(\frac{\Phi_1 - \Phi_2}{2}\right)\sin\left(\frac{\Phi_1 + \Phi_2}{2}\right)\ . \tag{1.43}$$

By neglecting the inductance of the superconducting loop, the magnetic flux circulating through the loop ϕ equals to the applied magnetic flux ϕ_{ext}.

Consequently, it comes

$$\Phi = \frac{2\pi\phi}{\phi_0} = \frac{2\pi\phi_{ext}}{\phi_0} = \Phi_1 - \Phi_2\ . \tag{1.44}$$

By reinjecting this result in Eq.(1.43), the total current I flowing through the SQUID reads

$$I = 2I_{c0}\cos\left(\frac{\pi\phi_{ext}}{\phi_0}\right)\sin\left(\frac{\Phi_1 + \Phi_2}{2}\right)\ . \tag{1.45}$$

Finally, the critical current of the SQUID I_c is obtained by maximising the total current I, it comes

$$I_c = 2I_{c0}\left|\cos\left(\frac{\pi\phi_{ext}}{\phi_0}\right)\right|\ . \tag{1.46}$$

This equation shows that the critical current of a SQUID is a periodic function of ϕ, with a period equal to ϕ_0. The function is represented in Fig.1.14. This allows to measure the flux crossing the loop with a higher resolution than ϕ_0.

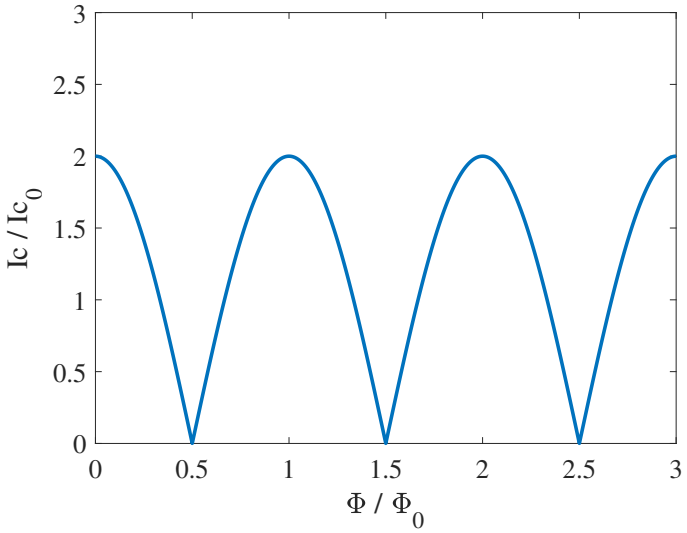


Figure 1.14: Dependence of the critical current with the external flux.

1.4 Electronic transport through a charged island

The quantization of electric charges was discovered by Millikan, more than a hundred years ago, in 1913 [42]. Electrons carry the elementary charge usually denoted as $e \simeq 1.602.10^{-19}$C. Despite being incredibly fundamental, this discovery did not have a huge impact in common electronics since the discreteness of the charge is not seen in most of electronic circuits and devices.

In order to observe charge quantization effects, it is first essential to be able to isolate a few electrons in tiny regions of space, roughly on the nanometer scale. Progress in fabrication techniques, especially in nanolithography, has opened up the possibility to confine electrons in sub-micron regions, allowing for the experimental observation of single electron physics.

However, this observation is only possible if the energy scale of the temperature is lower than the one associated with charging the device, referred to as the charging energy.

Among all the single-electron devices, the simplest system showing charging effects is the single-electron transistor (SET) consisting of a small island coupled to two leads. Thanks to the Coulomb repulsion, an electron cannot penetrate the island if the latter is already occupied with another one. Therefore, electrons are transferred through the SET one by one, in a sequential transport. Furthermore, the island is capacitively coupled to a gate. Depending on the applied gate voltage, the phenomenon of Coulomb blockade emerges, where the electric transport is completely blocked.

In this chapter, we will introduce the basic ingredients for single charge tunneling and present the single-electron transistor. I will also discuss how the Coulomb blockade can be explained within the basic concept of the charging energy.

1.4.1 The single electron transistor

1.4.1.1 Charging energy

The single-electron transistor consists of a small conducting region, typically called the island, coupled to two leads by tunnel junctions. These two leads (or electrodes) are commonly named source and drain of the transistor. An applied voltage between the source S and the drain D, i.e., $V_{DS} = V_S - V_D$ allows to drive a current through the transistor. The electronic levels of each electrode are filled up to their respective electrochemical potentials, μ_S and μ_D. The difference between the electrochemical potentials is determined by the applied voltage V_{DS}, such that $\mu_S - \mu_D = |e|V_{DS}$. Moreover, the island is also capacitively coupled to a gate G, meaning that its electrochemical potential can be tuned by the gate voltage V_G. The SET is schematically presented with its associated equivalent electric circuit in Fig.1.15.

The island is characterized by the so called charging energy which is defined as the energy required to add one additional electron to the island

$$E_c = \frac{e^2}{2C_\Sigma} \tag{1.47}$$

where C_Σ is the sum of the capacitances of the island, $C_\Sigma = C_S + C_D + C_G$.

1.4.1.2 Coulomb blockade

By applying a voltage V_G on the island, the total charge Q_{tot} of the island can be written as

$$Q_{tot} = Ne - C_S V_S - C_D V_D - C_G V_G \tag{1.48}$$

where N is the integer number of electrons on the island.

We can deduce the electrostatic energy of the island,

$$E_{el}(N) = \frac{Q_{tot}^2}{2C_\Sigma} = \frac{(Ne - C_S V_S - C_D V_D - C_G V_G)^2}{2C_\Sigma} \tag{1.49}$$

As the electron number of the island changes due to the tunneling, the electrostatic energy of the island is modified. In order to describe the charge transport, it is more convenient to refer to the electrochemical potential μ_N which is, by definition, the energy difference between two subsequent charge states and also the minimal energy required for adding the $(N+1)^{th}$ electron to the dot, it is given by

$$\mu_N = E_{el}(N+1) - E_{el}(N) = \left(N - \frac{1}{2}\right)\frac{e^2}{C_\Sigma} - \frac{eQ_{tot}}{C_\Sigma} \tag{1.50}$$

For zero applied voltage between the source and the drain, $V_{DS} = V_S = V_D = 0$, we deduce directly from the Eq.(1.49) and Eq.(1.50) the following expressions for the electrostatic energy and the electrochemical potential,

$$E_{el}(N) = \frac{(Ne - C_G V_G)^2}{2C_\Sigma} = E_c(N - n_G)^2 \tag{1.51}$$

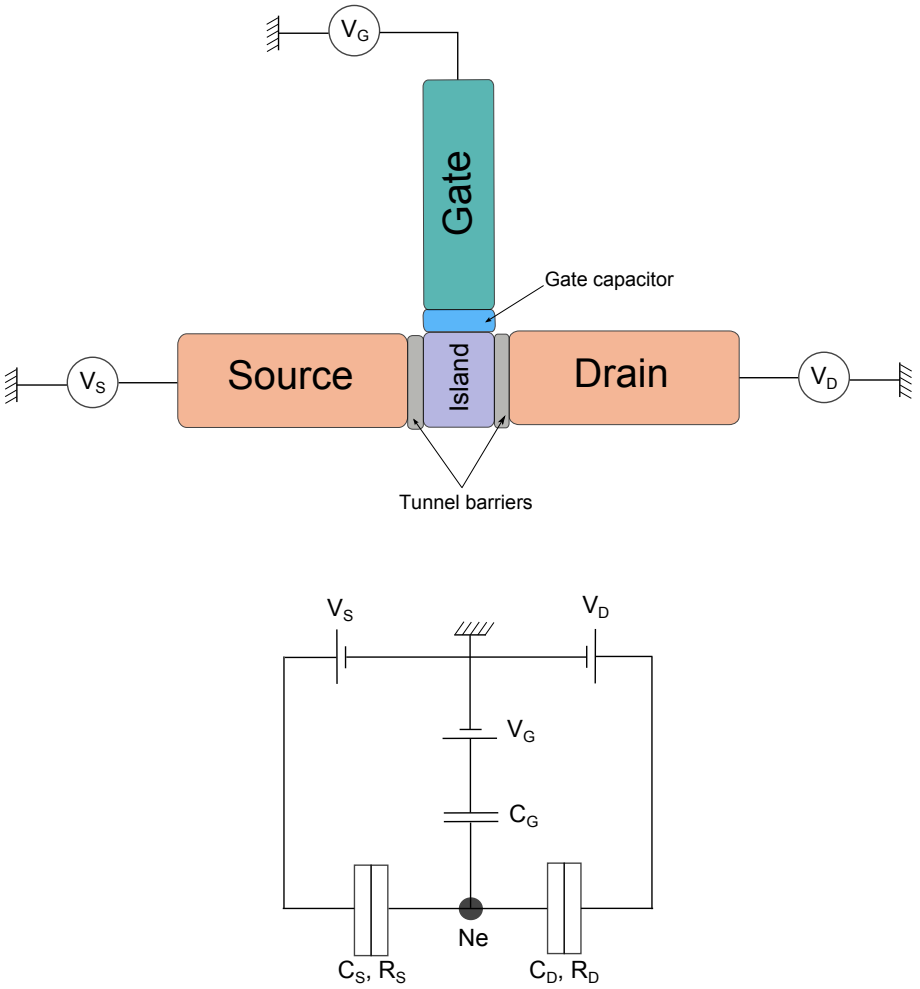


Figure 1.15: Schematic of a single-electron transistor and its equivalent electric circuit. The two tunnel junctions associated to the source and drain are characterized by a capacitance $C_{S,D}$ and a resistance $R_{S,D}$. The island with a certain integer amount of electrons N with a charge e, is coupled to the gate via the capacitance C_G.

where E_c is the charge energy, n_G is the density of induced charges added through the gate capacitor $n_G = \frac{C_G V_G}{e}$, and

$$\mu_N = \left(N - \frac{1}{2}\right)\frac{e^2}{C_\Sigma} - \frac{eC_G V_G}{C_\Sigma} \tag{1.52}$$

Eq.(1.51) exhibits a quadratic dependence of the electrostatic energy with the applied gate charge n_G. The different number of electrons N on the island gives energy levels which are a series of shifted parabolas as a function of the gate charge that cross at the half-integer charge degeneracy points, see in Fig.1.16. Precisely at these charge degeneracy points, we will get a conductance peak.

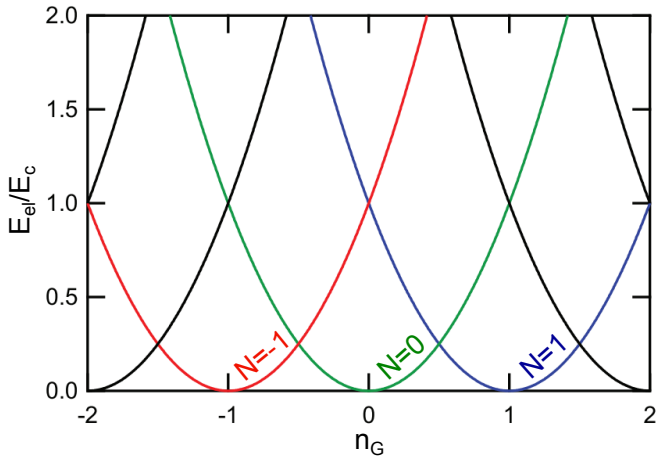


Figure 1.16: Energy levels of the SET. The electrostatic energy is plotted as a function of the applied gate charge n_G, for different number N of additional charges induced on the island by V_G. The points where these energy parabolas cross correspond to the charge degeneracy points, at which the charge on the island will increment by one electron, in order to remain in the ground state.

In order to find the gate voltage V_G corresponding to the intersection point between the $E_{el}(N)$ and $E_{el}(N+1)$ parabolas, i.e. when $E_{el}(N) = E_{el}(N+1)$, we set Eq.(1.52) to zero, giving the following condition for V_G,

$$V_G(N) = \frac{(N - \frac{1}{2})e}{C_G} \ . \tag{1.53}$$

In a SET, the current is established by sequential transport of electrons, meaning that electrons are transferred one by one through the transistor. Whether the transport is possible or not depends on the electrochemical potential on the island which can be tuned by the gate voltage. As a function of the applied gate voltage, the conductance shows a series of peaks, which corresponds to the Coulomb oscillations. In between the peaks, the transport is blocked; this is the Coulomb blockade.

The conductance peaks oscillate as a function of the gate voltage V_G, each peak corresponding to a change of one electron, as represented in Fig.1.17. The period ΔV_G is given by

$$\Delta V_G = V_G(N+1) - V_G(N) = \frac{e}{C_G} \tag{1.54}$$

We can deduce that the spacing between these half-integer conductance peaks is an integer. Adding one electron in the island requires the voltage $\Delta V_G = e/C_G$.

Let us summarize now the different scenarios for the transport through a SET that can occur depending on the applied bias voltage V_{DS} and the gate voltage V_G, with the sketches presented in Fig.1.18.

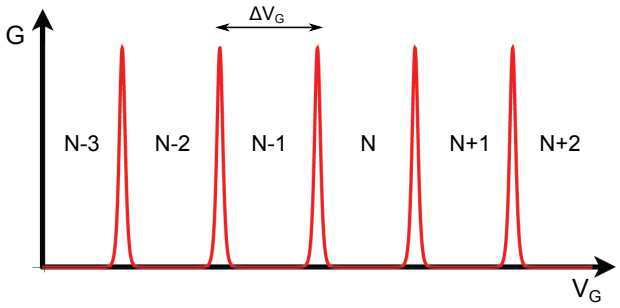


Figure 1.17: Conductance through a SET as a function of the gate voltage with a fixed bias voltage $V_{DS} = 0$. The conductance peaks are spaced with ΔV_G.

We assume in a first case that there is no applied voltage between the S and D leads and no gate voltage. In Fig.1.18(a), the sketched grey bars depict all the energies that are already occupied with an electron, up to the Fermi energy. In this case, electrons will not have enough energy to tunnel through the island and no current will flow across the transistor. Hence, the system is in a Coulomb blockade regime.

We consider now the case where a finite voltage is applied between the two leads. It means that the Fermi energy of the two reservoirs is different for a finite V_{DS}. We explain now two different possibilities, indicated with a purple or green star in Fig.1.18. The first situation is shown in Fig.1.18(b), where the energy levels of the island are tuned with the gate voltage such that no energy level exists between μ_S and μ_D. Consequently, no current can flow through the transistor (Coulomb blockade, purple star in Fig.1.18). However, as presented in Fig.1.18(c), if the energy levels are tuned such that a charge transition is energetically available, then the electrical transport is possible (single electron tunnelling, green star in Fig.1.18).

In Fig.1.18(e), the no-current areas and well-defined charge states display rhombohedral regions along V_{DS} =0, drawing the so called Coulomb diamonds. The numbers written inside the diamonds correspond to the number of charges in the island. Each time the charge on the island is incremented by one, we measure a finite conductance peak (Fig.1.18(d)).

Experimentally, the Coulomb diamonds allow us to estimate the charging energy of a system, as it is presented in Fig.1.19.

To observe the Coulomb blockade experimentally, several conditions are necessary. Firstly, the charging energy E_c needs to exceed the thermal energy k_BT, in order to avoid a thermal excitation of an extra electron that could get into the island instead of being blocked. To respect this first condition at room temperature, the capacitance C of the island has to be inferior to $3.09.10^{-18}$F, meaning that the radius R of the spheric metallic island has to be lower than 28nm, if we consider that the self-capacitance of a metallic sphere is proportional to is radius, such that $C = 4\pi\varepsilon_0 R$. That's why it is really important to work with extremly small islands. The other option to consider to respect this condition is to work at low temperature. It has become in fact possible to fabricate metallic islands

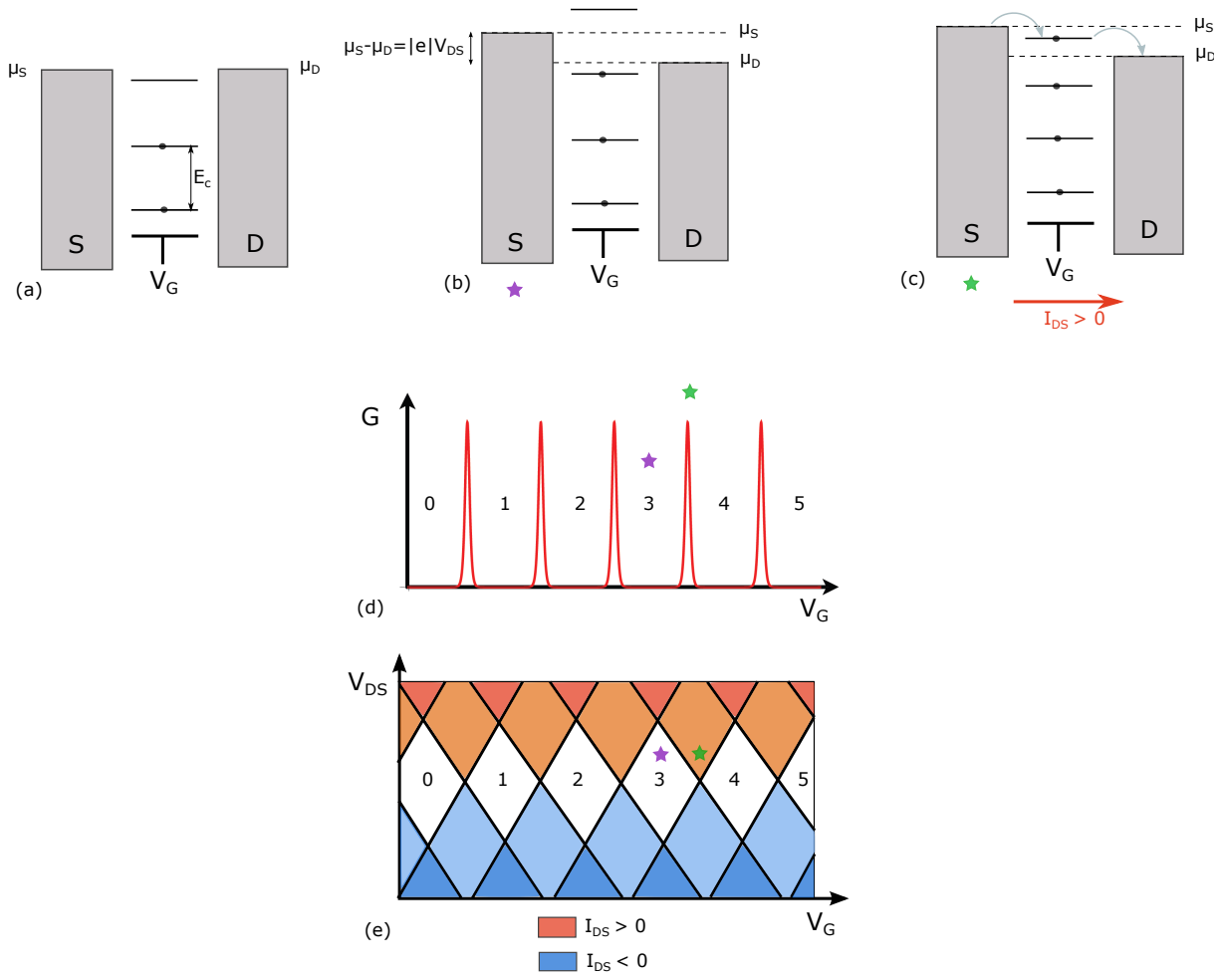


Figure 1.18: (a) Energy diagrams for a SET. The energy levels of the island are sketched with the central horizontal lines, spaced with the charging energy E_c. The grew bars correspond to the filled bands of the leads. With no finite bias applied, the transport is blocked. (b) No energy level exists within the bias window $\mu_S - \mu_D$: Coulomb blockade. (c) A charge transition is available within the bias window, allowing an electric transport. (d) Conductance as a function of the gate voltage showing conductance peaks. (e) Plot of the applied voltage with respect to the gate voltage, showing Coulomb diamonds.

with capacitances in the range of 10^{-15}F in a controlled way. The associated temperature scale E_c/k_B would be of the order of 1K, which is experimentally accessible.

The second condition refers to the life time $\Delta t = RC$ of an electron on the island. Indeed, it needs to be long to allow the corresponding energy uncertainty $\Delta E = h/\Delta t = h/RC$ to be weaker than the charging energy. That leads to a condition for the tunnel resistance between the island and the source and drain reservoirs written as $R_{tun} >> h/e^2 \simeq 26k\Omega$.

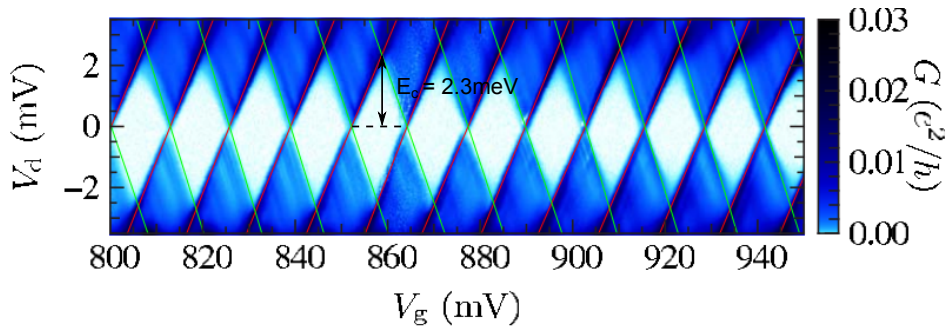


Figure 1.19: Graph of the differential conductance G as a function of the bias voltage (y-axis) and the gate voltage (x-axis). The Coulomb diamonds show the regions where the current is supressed by Coulomb blockade. Extracted from [43].

1.4.2 Superconducting Quantum Circuits

We will now proceed by considering transport in superconducting circuits. Such circuits are amongst the prime candidates to realize quantum bits (qubits), the core building blocks of quantum computers. Just like its classical counter part, the qubit stores information in a $|0\rangle$ or $|1\rangle$ state. Crucially though, while the classical bit provides information by being precisely in the $|0\rangle$ or $|1\rangle$ state, the qubit can be in any quantum superposition of these two states. Physically, the qubit is implemented as a quantum two-level system.

In principle, already a simple superconducting LC resonator could make up a coherent quantum system with discrete states, in the form of a quantum harmonic oscillator. However, as I will show in the following, the use of a non-linear element is essential since it will induce a non-equal spacing of the energy levels of the quantized oscillator and thus makes the circuit suitable as a two-level system.

Providing the non-linearity with its inductance, the Josephson junction represents a fundamental element used to fabricate superconducting quantum circuits. Importantly, there will be two energy scales, whose competition is essential when considering superconducting qubits. Apart from the Josephson energy E_J, there will also emerge a charging energy E_c associated with the tunneling of Cooper pairs, in analogy to the charging effects of the SET introduced above. By varying the E_J/E_C ratio, we can in fact obtain devices operating in different regimes, from Cooper-pair boxes to transmon qubits.

In this section, the basic concepts of superconducting qubits such as Cooper pair box, transmon and gatemon qubits will be presented. I will begin with the simple LC circuit, with an inductance and a capacitance in parallel, behaving as a harmonic oscillator.

1.4.2.1 The LC circuit

The LC resonator is composed of an inductance L and a capacitance C in parallel as introduced in Fig.1.20. We denote two energies associated to the LC oscillator. A capacitive energy $Q^2/2C$ represents the energy that can be stored in the capacitor, where Q is the

charge on each capacitor plate. There is also an inductive energy $\phi^2/2L$, where ϕ is the flux through the inductor.

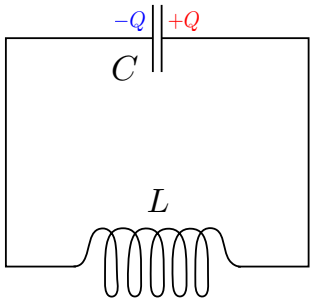


Figure 1.20: LC circuit.

By quantizing Q and ϕ, according to the quantization prescription $[Q,\phi] = i\hbar$, we obtain the effective Hamiltonian of the LC circuit

$$\hat{H} = \frac{\hat{Q}^2}{2C} + \frac{\hat{\phi}^2}{2L} \ . \tag{1.55}$$

We recognize here the Hamiltonian of a harmonic oscillator, with a resonance frequency $\omega_0 = 1/\sqrt{LC}$. The energy spectrum of the quantized harmonic oscillator in Fig.1.21 shows an equidistant spacing between the levels.

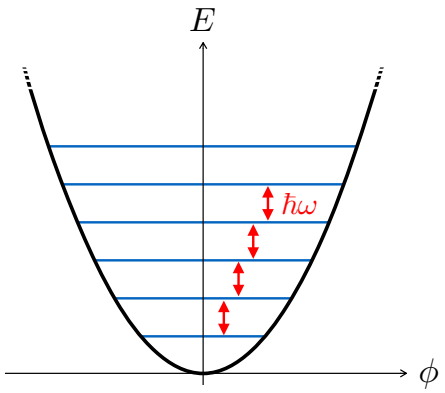


Figure 1.21: Energy spectrum showing equidistant energy levels separated by the transition frequency.

However, it is impossible to implement a superconducting qubit using such a linear LC circuit because the associated transition frequencies between all the adjacent energy levels are strictly equal, which prevent us to manipulate the two lowest states of the qubit without exciting higher energy states. Therefore, in order to realize a qubit, we need to introduce a non-linear element in the circuit. One possible solution is to substitute the linear inductance of the LC oscillator with a non-linear one, provided by a Josephson junction.

1.4.2.2 Cooper Pair Box (CPB)

The Cooper pair box (CPB) consists of a superconducting reservoir and a superconducting island, connected by one or two Josephson junctions, where Cooper pairs and quasiparticles can tunnel. In its simplest version presented in Fig.1.22, a single Josephson junction with capacitance C_J and Josephson energy $E_J = \frac{\phi_0 I_c}{2\pi}$ is used. The superconducting CPB island is also capacitively coupled to a gate voltage V_G, in serie with a capacitance C_G.

In addition to the Josephson energy, the island has a second characteristic energy, the charging energy E_c, required to transfer one Cooper pair through the junction. This is given by

$$E_c = \frac{(2e)^2}{2C_\Sigma} \tag{1.56}$$

where C_Σ is the total capacitance of the island, written as the sum $C_\Sigma = C_J + C_G$, and $2e$ is the corresponding charge of a Cooper pair.

Taking into account these two energies, we can now derive the effective Hamiltonian of the system as

$$\hat{H} = 4E_c(\hat{N} - n_G)^2 - E_J \cos(\hat{\Phi}) \tag{1.57}$$

where $\hat{N}$ is the Cooper pair number operator, $\hat{\Phi}$ is the phase difference operator and n_G is the gate charge measured in units of the Cooper pair charge $2e$, that can be written as

$$n_G = \frac{C_G V_G}{2e} + \frac{Q_{env}}{2e} \tag{1.58}$$

where Q_{env} denotes the environment-induced offset charge.

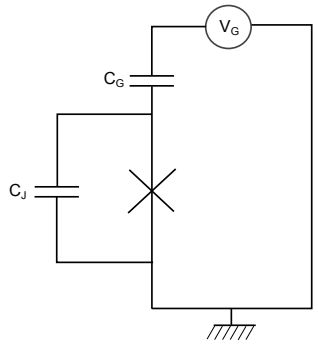


Figure 1.22: Scheme of the electric circuit of a Cooper Pair Box. It consists of a Josephson junction with Josephson energy E_J and a capacitance C_J, capacitively coupled to a gate voltage V_G through a gate capacitor C_G.

In Fig.1.23 the energy levels of the Hamiltonian of the Eq.(1.57) are represented as a function of the gate charge n_G for different values of E_J/E_c. A CPB is operated in the regime where $E_J << E_c$. When $E_J = E_C$ (Fig.1.23(a)), the CPB regime still dominates.

In fact, we can clearly see the relation between the CPB energy spectrum in Fig.1.23 and the charging energy diagram of the SET (Fig.1.16). The coherent Cooper pair tunneling

provides an anticrossing of the energy lines, with an energy gap scaling with the Josephson energy E_J. This is typical for a quantum coherent coupling of two states, in this case two charge states differing by $2e$.

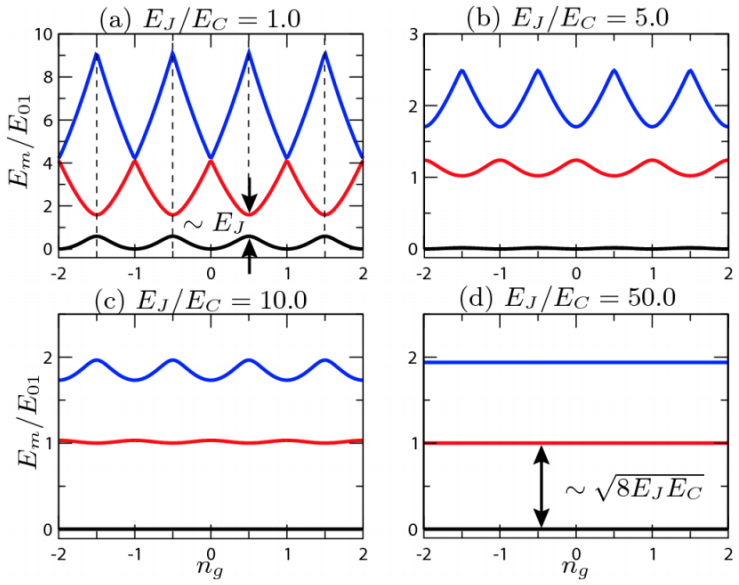


Figure 1.23: First three energy levels of the Hamiltonian of the Cooper pair box as a function of the gate charge n_G, for E_J/E_C ratios equal to 1, 5, 10 and 50. As can be observed on (d), for $E_J >> E_C$, the charge-dispersion curve becomes completely flat. Extracted from [3].

1.4.2.3 Transmon qubit

Because of its small size, the CPB is very sensitive to charge noise. As a matter of fact, one can elegantly accomplish a protection against charge noise by tweaking the system parameters, such that $E_J >> E_c$. A qubit operating in this regime is called a transmon, first developped by Schoelkopf [44], [3]. The strongly reduced charging energy can be obtained by setting a large capacitance C_J in parallel to the Josephson junction.

Two parameters are essential in the operation of a transmon qubit, the charge dispersion of the energy levels and the anharmonicity. Fig.1.23 shows that an increase of the ratio E_J/E_c directly leads to a decrease in the charge dispersion, and consequently reduces significantly the sensitivity towards charge noise. In fact, we notice that the levels become more and more flat as the ratio rises. More precisely, it has been derived that the charge dispersion flattens exponentially with E_J/E_c [3].

While increasing the ratio E_J/E_c lowers the charge noise sensitivity and thus enhances the transmon qubit performance, it reduces at the same time the energy level anharmonicity, allowing the system to become nearly a harmonic oscillator. However, keeping the

anharmonicity is crucial to be able to isolate the two lowest states of the perturbed harmonic oscillator of the qubit.

We can easily quantify the anharmonicity by considering the Hamiltonian (Eq.(1.57)) in the transmon regime. In the limit of $E_J/E_c \to \infty$, we recover the linear, harmonic oscillator, where all energy levels are equally separated by the plasma frequency, i.e.,

$$\omega = \frac{1}{\sqrt{L_J C}} \sim \frac{1}{\hbar}\sqrt{8E_J E_c} \ . \tag{1.59}$$

For a finite but still large ratio of E_J/E_c, the energy levels receive the following corrections. The transition energy from ground to first excited state is approximated as $E_{01} = \sqrt{8E_J E_c} - E_c$ and from first to second excited state, $E_{12} = \sqrt{8E_J E_c} - 2E_c$. Thus, for $E_J >> E_c$, the anharmonicity of the transmon qubit is derived as

$$\alpha = E_{12} - E_{01} \simeq -E_c \ . \tag{1.60}$$

We see that while the charge dispersion diminishes exponentially, the anharmonicity vanishes only linearly. For this reason, it is still possible to find a regime $E_J >> E_c$ where the system is essentially insensitive to charge fluctuations and the amount of anharmonicity required for the control of a qubit is still large enough to allow for the isolation of the first two states. Consequently, the transmon qubit remains controllable.

1.4.2.4 Gatemon

Based on the principle of the transmon qubit and operating in the same regime, a new device called gatemon was introduced [4], [5]. This new type of transmon-like device is based on semiconductor nanowires. It uses a S-Sm-S (Superconductor-Semiconductor-Superconductor) Josephson junction capacitively coupled to a gate. Actually, the gate voltage allows to control the Josephson energy, by modulating the density of charges in the semiconductor nanowire.

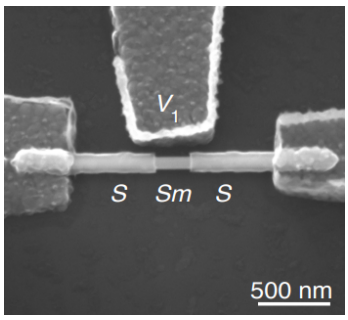


Figure 1.24: Scanning electron micrograph of the S-Sm-S Josephson junction connected with high transparency epitaxial Al contacts. The gate voltage V_1 is used to modify the critical current of the InAs nanowire and hence to control the Josephson energy. Extracted from [4].

The first operating gatemon was realized by the team of Marcus in Copenhagen [4] and DiCarlo in Delft [5]. The device presented in Fig.1.24 is based on a InAs semiconductor nanowire with an epitaxially grown Al superconducting layer to realize the highly transparent contacts. A nearby gate voltage is added in order to be able to tune the Josephson energy of the junction.

Almost all transmons are fabricated with SIS tunnel junctions associated to many low transmitting channels. However, a gatemon is based on a semiconductor nanowire which has only a few highly transmitting channels. Consequently, the first Josephson equation is modified and Beenakker has shown that the Josephson potential of a nanowire based Josephson junction is written as follows [34]

$$V(\hat{\Phi}) = -\Delta \sum_{i=0} \sqrt{1 - T_i \sin^2(\hat{\Phi}/2)} \tag{1.61}$$

where $\hat{\Phi}$ is the phase difference operator, i is the number of conducting channels and T_i is the transmission of the i^{th} channel.

Considering a gatemon working in the transmon regime and hence neglecting the offset charge of the island, the effective Hamiltonian becomes

$$\hat{H} = 4E_c\hat{N}^2 + V(\hat{\Phi}) \tag{1.62}$$

where $\hat{N}$ is the Cooper pair number operator.

We plot the Josephson potential normalized by the Josephson energy with respect to the phase difference for two limiting cases, T_i=1 and $T_i \to 0$ in Fig.1.25. A harmonic potential is also depicted for comparison. For the first case of fully transmitting channels (T_i=1), the potential resembles the harmonic potential. For $T_i \to 0$, the shape of the potential is different, as it is now proportionnal to $-\cos(\Phi)$, corresponding to the well-known SIS junction with low transmitting channels.

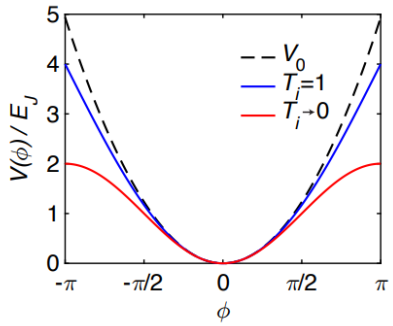


Figure 1.25: Normalized Josephson potential as a function of the phase difference, for two different limits of T_i (blue and red lines). A harmonic potential V_0 is also plotted (dashed black line). Extracted from [4].

Studying these two different limiting cases allows us to establish a relation between the anharmonicity α and the transmitting channels. As we mentioned before, for a transmon based on a SIS junction, i.e., in the limiting case $T_i \to 0$, $\alpha = -E_c$. For T_i=1, $\alpha = -E_c/4$. Experiments realized recently have managed to measure the anharmonicity in a gatemon qubit. As a result, the anharmonicity obtained for nanowire based Josephson junctions is between these two limits [45].

1.4.3 Josephson Field Effect Transistor (JOFET)

So far, we have mainly considered the transport properties through a metallic or superconducting island in the different hybrid structures presented before. We will now focus on hybrid superconductor (S)-quantum dot (QD) systems. The major advances in nanofabrication techniques have made it possible to couple quantum dots to superconducting leads. Hybrid devices with quantum dots open the possibility to control single electrons (quantum dots) in the presence of a macroscopic quantum phenomenon involving large numbers of electrons (superconductivity). This naturally leads to a competition between superconductivty and Coulomb blockade.

The first experimental evidence of superconducting properties in transport through a hybrid superconductor-quantum dot device has been obtained in 1995 [46]. In fact, the signature of the superconducting gap was revealed and the quasiparticle density of states close to the superconducting gap was modified. However, the measurement of the supercurrent remained a hard task since it was only possible in a transport regime where the tunneling of quasiparticles was the dominant transport mechanism. More precisely, this problem was based on fabrication aspects. For example, because of the presence of Schottky barriers at the interface between the superconducting leads and the semiconductor, the tunneling of Cooper pairs was impossible.

Nevertheless, by including new materials for quantum dots, such as carbon nanotubes [47], [48], [49], [50] or InAs semiconducting nanowire [51], as presented in Fig.1.26, the evidence of a supercurrent became accessible due to a higher transparency of the barrier and thus, to a better coupling.

We want to focus now on the Josephson Field Effect Transistor (JOFET), which is also a hybrid superconductor- gate-controlled quantum dot device. This device is based on a semiconductor, which allows the control of the charge carrier concentration by simply applying an electric field. More precisely, the Field Effect Transistor (FET) consists of a semiconductor connected to a source and a drain, and capacitively connected to a gate and additional backgate. The current through the FET is related to the number of charge carriers. Hence, by applying a gate voltage, one can control the conductance of the semiconductor.

If the source and drain are superconducting, the FET becomes a JOFET, that can be understood as a SINIS junction where the role of the normal metal is played by a doped

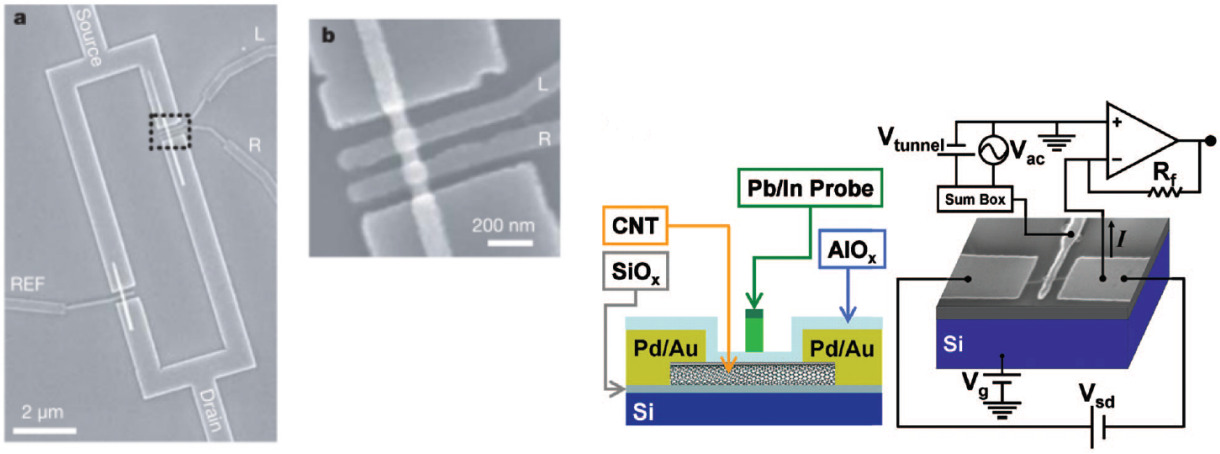


Figure 1.26: On left: SEM image of a quantum dot coupled to Al superconducting leads. The device is a Ti/Al SQUID whose two arms contain a break bridged by an InAs nanowire. A pair of Al gates (L, R) is used to define the quantum dot for one of the nanowires. Figures reproduced from [51]. On right: sketch of the carbon nanotube device geometry, and SEM image of the carbon nanotube quantum dot, with the measurement circuit. Extracted from [47].

semiconductor. The critical current of such tunable Josephson junction can be modified by the applied gate voltage.

When studying the transport properties through a JOFET, we observe a zero conductance gap region with a width of 2Δ, which splits the Coulomb diamonds into two parts, as shown in Fig.1.27(a). This zero conductance gap is due to the energy gap induced in the semiconductor by the superconducting proximity effect. The standard "closed" Coulomb diamond pattern can be obtained as soon as the superconductors of the device are made normal by applying a sufficient magnetic field.

Fig.1.27(b) indicates the condition to avoid the suppression of current due to the induced superconducting gap; the applied bias voltage between source and drain has to be $V > 2\Delta/e$.

1.4.3.1 Weak/strong coupling regime

Depending on the relative values of distinct characteristic energies, we can distinguish three different regimes for such devices, inducing a direct competition between superconductivity and Coulomb blockade [52]. These energies are the superconducting gap Δ, the charging energy E_c and the width of the quantum dot energy levels Γ, the latter being associated with the tunneling rate of the electrons across the barrier. All of these energy scales are indicated on the energy diagram in Fig.1.28. As we are now considering a quantum dot and not an island in the device, we have now to take into account the spacing ε between two consecutive energy levels in the quantum dot.

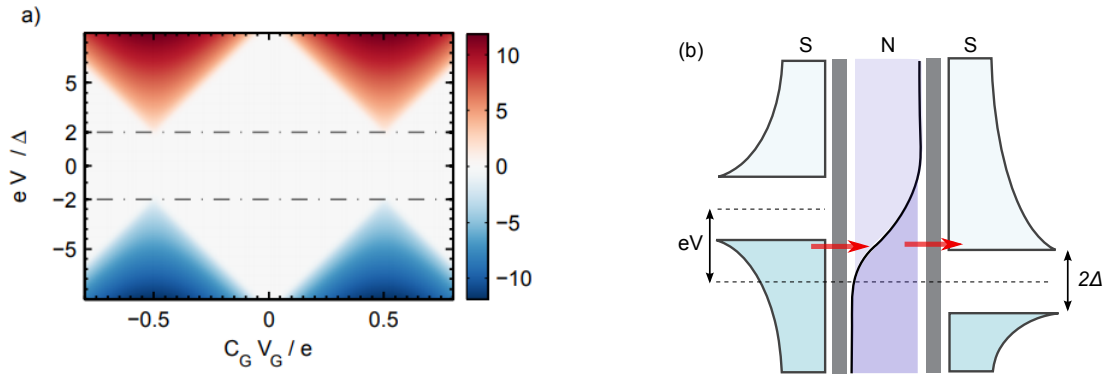


Figure 1.27: (a) Zero conductance gap in the Coulomb diamond pattern of a SINIS junction for an applied bias voltage $V < 2\Delta/e$. (b) Sketch of the energy density for a SINIS junction showing that the current is supressed if $V < 2\Delta/e$.

The three regimes for a quantum dot are defined as follows. Firstly, the strong-coupling regime appears when $\Gamma >> \Delta, E_c$. In this regime, the value of the charging energy is not high enough for a Coulomb blockade to emerge. Consequently, the Cooper pairs can tunnel through the junction leading to a supercurrent flowing across the quantum dot (Fig.1.29(a)). In fact, in its essence, this regime is comparable to the gatemon physics discussed above.

Secondly, if $\Gamma << \Delta, E_c$, we have a weakly coupled quantum dot. The high charging energy prevents the Cooper pairs to tunnel through the quantum dot. Thus, no supercurrent can flow in this regime. However, single-particle tunneling is still possible. As explained in the section of the single electron transistor, depending on the bias voltage and the gate voltage applied, the device will experience either a Coulomb blockade or a flowing current (Fig.1.29(b)). Overall, in this regime the transport results in the splitted Coulomb diamonds, shown in Fig.1.27(a).

Finally, in the intermediate-coupling regime, all the energy scales are comparable, i.e., $\Gamma \sim \Delta \sim E_c$. This regime is definitely the most complex one, where the competition between superconductivty and single-particle process is the most apparent.

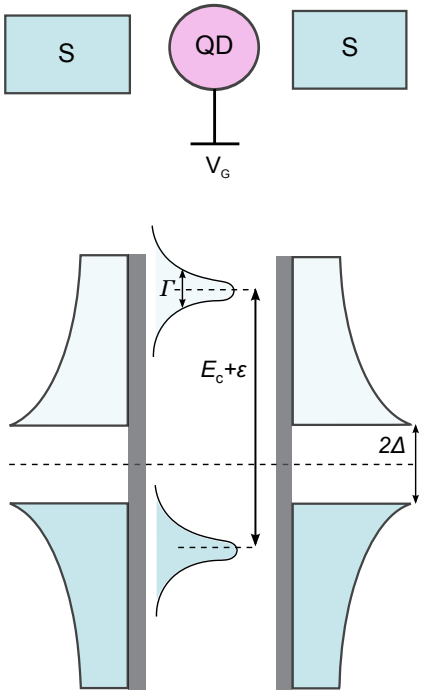


Figure 1.28: Energy diagram for a hybrid superconductor-quantum dot device. The energy required to add a single charge in the quantum dot is the charging energy E_c (the spacing between two energy levels in the QD is ε), Δ is the superconducting gap and Γ is the width of the quantum dot energy levels.

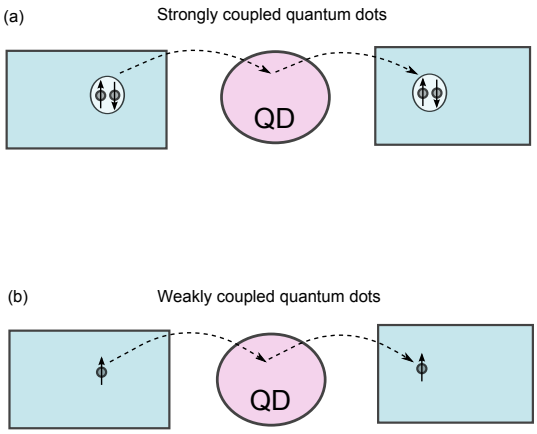


Figure 1.29: (a) Supercurrent is the dominant transport mechanism in the strong coupling regime ($\Gamma >> \Delta, E_c$). (b) Single electrons can tunnel from source to drain if a minimum bias voltage $V > 2\Delta/e$ is applied in the weak coupling regime ($\Gamma << \Delta, E_c$). Cooper pairs cannot tunnel due to the strong charging energy.

Chapter 2

Experimental techniques

Contents

2.1 Cryogenics

2.1.1 Dilution refrigerator

Up to the 1950s, the only technnique to obtain temperatures below 1K was based on magnetic refrigeration using adiabatic demagnetization of paramagnetic salts in crystal or tablet form [53]. This method was then replaced by the ^{3}He-refrigerator. However, the use of the latter, by only pumping a ^{3}He-bath, makes possible to achieve temperatures at best of the order of 0.3K.

The dilution refrigerator principle was suggested by London in 1952. Ten years later, based on this promising and original idea, Clarke, Mendoza and London himself proposed a prototype of the continuous refrigerator with liquid helium to lower temperatures. In comparison to ^{3}He-refrigerators exploiting the latent heat of evaporation for cooling, the new approach was to use the heat of mixing of the two helium isotopes to obtain very low temperatures. The first continuous refrigerator using this new principle was built in 1964, in the Kamerlingh Onnes Laboratorium, at Leiden University, and they managed to reach the low temperature of 0.22K, never got before by any refrigerator systems [54]. Rapidly after, in 1966, Neganov et al. in Dubna and Hall et al. in Manchester went below the temperature of 100mK with an improved design of the ^{3}He-^{4}He dilution refrigerator. With these improvements combined to the efficiency of the system, the Dubna refrigerator soon reached the extreme low temperature of 25mK.

In this chapter, I will present in detail the ^{3}He-^{4}He dilution refrigeration system. This tool offers the only continuous refrigeration method for temperatures below 0.3K. ^{3}He-^{4}He dilution refrigerators are nowadays among the most important equipment for condensed-matter physics since many properties of matter have to be studied at temperatures well-below 1K to understand their peculiar behavior. In addition, another not negligible point is that the magnetic field, often needed in low-temperature experiments, has negligible effects on the refrigerator performance. However, even if its thermodynamics is now well established, building such a system needs substantial experience and a lot of time.

The operation of a dilution refrigerator requires the use of the two helium isotopes mixing : ^{3}He and ^{4}He, and is based on the fundamental properties of the ^{3}He-^{4}He phase diagram. In the chapter, we note x the concentration of ^{3}He in the mixture of the two helium isotopes. By definition, the ^{3}He concentration is written as

$$x = \frac{n_{^3\mathrm{He}}}{n_{^3\mathrm{He}} + n_{^4\mathrm{He}}} \tag{2.1}$$

where $n_{^3\mathrm{He}}$ and $n_{^4\mathrm{He}}$ are the number of ^{3}He and ^{4}He atoms respectively. Hence, the ^{4}He concentration equals to 1-x.

The phase diagram (x,T) of the ^{3}He-^{4}He mixture at saturated vapour pressure is illustrated on Fig.2.1. This figure shows several of the remarkable features of the isotopic liquid mixture. On this diagram, the tri-critical point located at a temperature of 0.87K and at

a ^{3}He concentration close to 70%, separates the three possible phases of the mixture. We dinstinguish the superfluid phase, the normalfluid phase and the two-phase region.

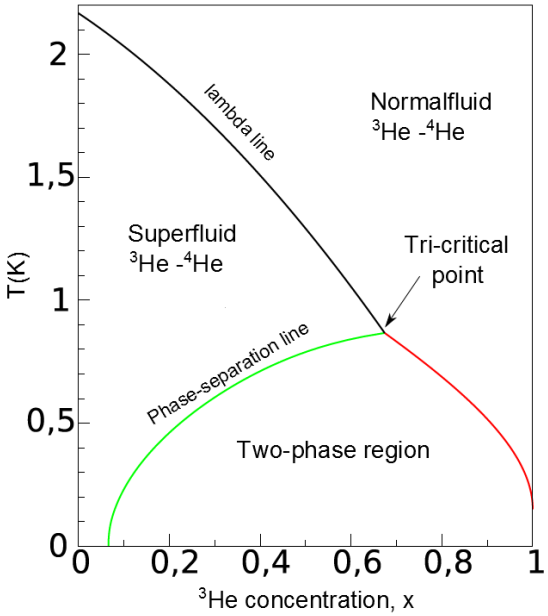


Figure 2.1: Phase diagram of the ^{3}He-^{4}He mixture at saturated vapour pressure. The diagram depicts the lambda line, which distinguishes the superfluid phase from the normalfluid one, and also the phase separation line, separating the superfluid phase and the two-phase region.

Let's now focus on the pure liquids. The diagram shows that liquid ^{4}He becomes superfluid at a temperature of 2.17K. Superfluidity is the characteristic property of a fluid with zero viscosity, and concerns here only ^{4}He at very low temperature. In this present mixture case, referring to the diagram, the superfluid phase is revealed for temperatures under the so called lambda line.

As we can observe in Fig.2.1, the ^{3}He and ^{4}He mixture is perfectly miscible for temperatures above 0.87K. But, then, if we cool this helium mixture (with $x > 6\%$) to temperatures below 0.87K, the solution becomes instable; the liquid will finally separate into two distinct phases, one rich in ^{3}He and the other rich in ^{4}He. Because of its lower density, the ^{3}He-rich liquid floats on top of the ^{4}He-rich liquid. The ^{3}He-rich phase is called the concentrated phase and the ^{4}He-rich phase is the dilute phase. In the latter, a few atoms of ^{3}He, surrounded by superfluid ^{4}He, behave as a gaz and the associated pressure is the osmotic pressure.

The process of cooling in a ^{3}He-^{4}He dilution refrigerator is achieved by transferring ^{3}He atoms from the "liquid" concentrated phase to the "gaseous" dilute one. The principle of a dilution refrigerator can be easier understood if we compare its cooling process to the cooling happening when a liquid is evaporated. However, despite this simple analogy, we

do not forget that the physics involved in these two cooling processes differs. In fact, in a classical evaporation, the heat of evaporation is used for cooling; whereas for a dilution refrigerator, the enthalpy of mixing of two liquids is involved [55], [56].

The four main components of a dilution refrigerator are the following : the 1K bath, the still, the heat exchangers and the mixing chamber. All of these elements are immersed in a ^{4}He bath (T=4.2K) allowing a precooling. The sketch of the ^{3}He-^{4}He dilution refrigerator is presented in Fig.2.2.

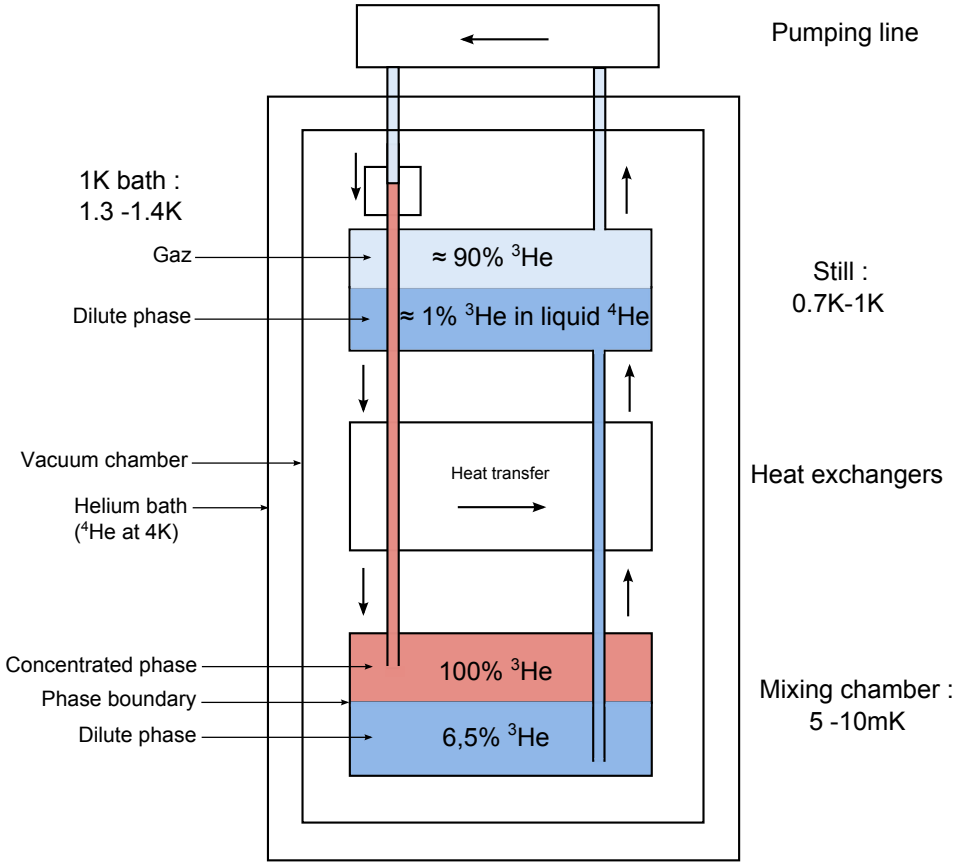


Figure 2.2: Schematic ^{3}He-^{4}He dilution refrigerator.

At first, the outside ^{3}He gas coming from the exit of a pump at room temperature is precooled by the liquid ^{4}He bath. ^{3}He is then condensed in the ^{4}He pumped bath at about 1.3K. A flow impedance is used to ensure sufficient pressure in order to make the ^{3}He condense. The liquid ^{3}He can now circulate through a first heat exchanger, which is in thermal contact with the still, at a temperature around 0.7K. Afterwards, a second flow impedence allows to keep ^{3}He liquid and prevent from any evaporation. And for the second time, the liquid ^{3}He can flow through one or a serie of heat exchangers, used to lower its temperature enough until it can penetrate into the mixing chamber.

We remind that a certain quantity of ^{3}He is continously evaporated in the still. Because of the concentration difference, a small part of ^{3}He will migrate from the mixing chamber

to the still. This will result in a depletion of ^{3}He in the dilute phase, and consequently, the thermodynamic equilibrium will be no longer satisfied. In order to maintain the ^{3}He-^{4}He ration, ^{3}He atoms of the concentrated phase will evaporate to the dilute phase of the mixing chamber. This migrant flux absorbs a certain energy quantity, generating a cooling.

2.1.2 PPMS

To measure the samples at very low temperature, an additional system of cooling was largely used. The PPMS (Physical Properties Measurement System) is an automated measurement plateform produced by Quantum Design and installed in Pheliqs, in CEA. This cryostat allows the temperature to range from 300K to 2K in almost two hours thanks to a continuous ^{4}He pumping. Fig.2.3 shows a cross-sectional view of the PPMS.

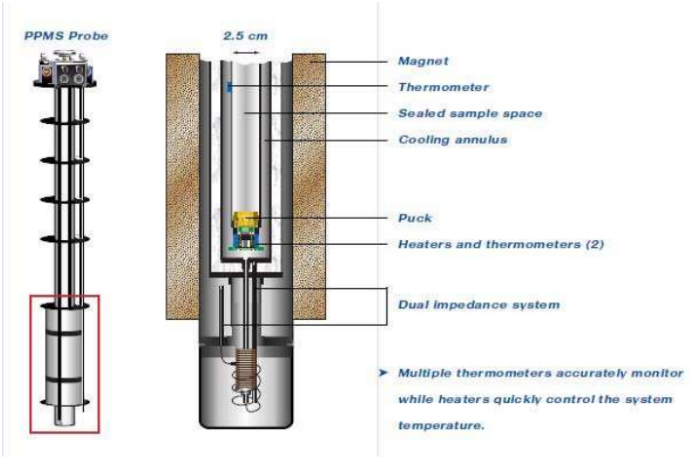


Figure 2.3: Cross-sectional view of the PPMS.

The sample holder (also called puck) contains a superconducting coil permitting to generate a magnetic field up to 9T. It can welcome two samples and a thermometer, allowing to perform three different measurements in parallel. In my case, I only used the PPMS to measure the resistivity of my samples. In order to observe certain superconducting transitions, it was necessary to reach temperatures well-below 2K. The idea is to use the process of adiabatic demagnetization compatible with the PPMS. The temperature can indeed be lowered from 2K to 50mK in a few minutes. The cooling process is composed of several steps, I will describe them briefly.

Firstly, the sample-holder is placed inside the PPMS and cooled at 2K in a high vacuum atmosphere. A magnetic field of 4T is applied afterwards, leading to an alignment between the magnetic moments of the paramagnetic salts and the field. The sample-holder is in equilibrium at 2K. Then, the sample-holder is thermally decoupled from the external environment thanks to a secondary pumping. The magnetic field is then removed, causing a misalignment of the magnetic moments. The puck is this time isolated; and the total

entropy of the system has to remain constant. For this reason, the temperature will start to decrease, until reaching its minimum at around 50mK. Finally, the sample-holder will warm up slowly since the thermal insulation is not perfect. The transport measurements can be performed during this warming. Usually, it takes almost one hour to reach again 2K.

2.2 Measurement techniques

2.2.1 Fabrication of the contacts

The electrical resistances of our Si:B and SOI:B layers were measured at room temperature using the 4-wire sensing. Its principle is very simple: by passing a current through two outer probes and measuring the voltage through the inner probes, we manage to determine the sample resistivity. This involves the fabrication of 4 contacts pads at the surface of our samples in cleanroom, whose steps will be specified below.
1) PPMA (Poly(methyl methacrylate)) resin deposit on all the surface of the sample (spreading: 6000 rpm during 50s, annealing: 180°C during 4min, thickness: 200nm).
2) Drawing of the contacts on KLayout (on left of Fig.2.4) and optical lithography to define the shapes of the contacts.
3) Development MIBK + IPA (Methyl isobutyl ketone + isopropanol), rinse with IPA.
4) HF cleaning to remove the native SiO_2 oxide.
5) Evaporation of Ti(10nm)/Au(70nm).
6) Lift off (acetone).

This process ensures the fabrication of clean and well-defined contacts with small contact resistances (in comparison with the resistances of our layers), as it can be seen in Fig.2.4(right).

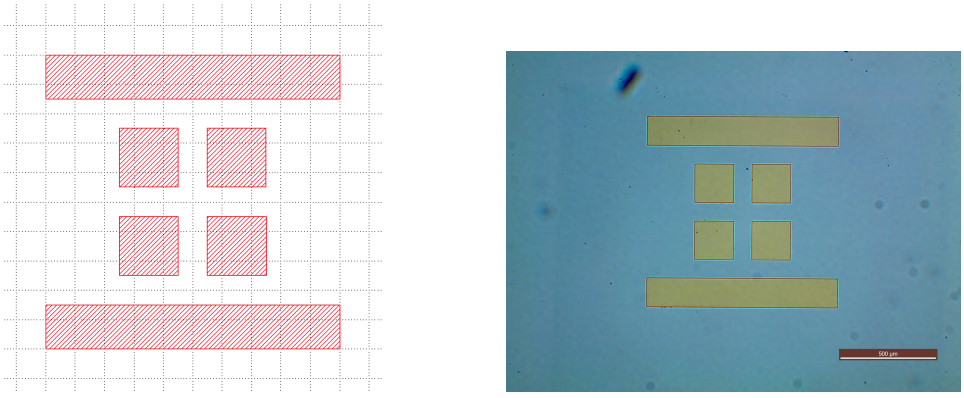


Figure 2.4: On left: drawing of the contacts shapes with the software KLayout. On right: optical microscope image showing the Ti/Au contacts on the Si:B layer, after lift-off. We can also distinguish the Si:B layer from the Si substrate with the slight color change.

2.3 Analysis techniques

2.3.1 X-ray diffraction (XRD)

In addition to the very low temperature measurements realized both with the PPMS and the dilution refrigerator, we also used X-ray diffraction (XRD) to characterize the crystalline structure of our samples. I will now explain the principle of this non-destructive technique. In fact, XRD provides information on various elements such as the crystalline structure, the preferred crystal orientation (also known as the texture), and other structural parameters, such as the average grain size, the presence of strain and crystal defects. A sketch explaining the principle of the XRD measurement is presented in Fig.2.5. The angle ω is defined as the angle between the position of the X-ray source and the surface of the measured sample. 2θ refers to the angle between the position of the X-ray source and the position of the detector.

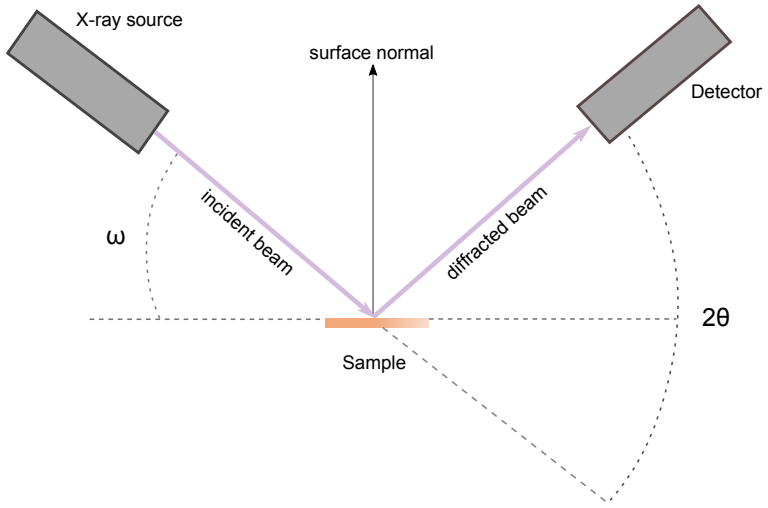


Figure 2.5: Sketch showing the principle of XRD measurement.

The fundamental and powerful equation in XRD studies is the Bragg's law, which allows to determine the different crystal lattice plane spacings and thus also the lattice parameters. As the atoms in a crystal are arranged in lattice plane layers, the X-rays can be assumed as being scattered by the lattice planes themselves. The derivation of the Bragg's law can in fact be done by simple geometry analysis, using Fig.2.6. The lattice planes with h, k and l Miller indices are separeted by a distance d_{hkl}.

As it can be seen in Fig.2.6, the incident X-ray beam gets scattered by the two lattice planes. However, since there is a finite distance between these planes, there will be a path difference between the two beams when they coincide at infinity. The total path difference is S1+S2. We note that the paths S1 and S2 can be written as a function of d_{hkl} and θ, such as S1+S2 $= 2d_{hkl} \sin\theta$. By combining this with the condition for constructive interference, we can obtain the Bragg's law

$$2d_{hkl} \sin\theta = n\lambda \tag{2.2}$$

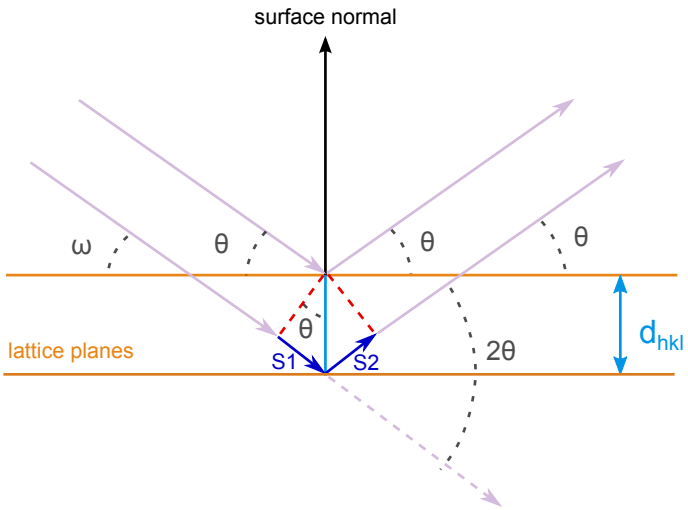


Figure 2.6: Scattering of X-rays against two adjacent lattice plane layers.

where λ is the wavelength of the incident beam and n an integer.

Performing XRD measurements, we will register intensity peaks whenever Eq.(2.2) is verified. Consequently, XRD peaks are produced by constructive interference of a X-ray beam diffracted at specific angles from each set of lattice planes in a sample. We deduce that the X-ray diffraction pattern giving the intensity peaks with respect to the angle 2θ, is the fingerprint of the periodic atomic arrangements of a sample.

With XRD, we can determine if our Si:B layers obtained on top of bulk silicon substrate or SOI substrate are crystalline. In the case of highly boron-doped silicon or SOI obtained by GILD or PLIE, boron is introduced in the substitutional sites of the silicon layer, inducing a weak contraction of the epitaxial layer. This will result in a higher diffraction angle for the doped layer than for the silicon one, according to the Bragg's law. These XRD measurements could also allow us determining the thickness of the boron-doped silicon layer with the presence of interference fringes.

Chapter 3

Superconducting boron-doped Silicon on Insulator (SOI:B)

Contents

Introduction

As mentioned above, the Josephson effect is indeed the basic component concerning superconducting electronics. More precisely, we want to fabricate nanotransistors with superconducting source and drain, leading to the creation of a Josephson Field Effect Transistor (JOFET), allowing a non-dissipative current to flow through it. The superconducting material used to realize the source and drain contacts of the transistor has to be compatible with the silicon technology. It is for reproducibility and scalability reasons that we want to focus on nanodevices using a silicon technology. The first road to introduce superconductivity in transistors that we consider involves a superconducting semiconductor: the superconducting silicon.

The possibility of observing superconductivity in semiconductors has long been studied over the years, but firstly theoretically. In 1964, with his correct theoretical prediction, Cohen opened the road of new superconductors, the superconducting semiconductors [57]. The same year, semiconductors such as GeTe and $SrTiO_3$ were shown to exhibit superconductivity at low temperature [58], [59]. Despite these considerable discoveries, the critical temperatures associated to these superconductors remained rather weak and did not exceed 100mK.

After this breakthrough, much interest has been given to the issue of superconductivity in semiconductors leading to a significant rise of the number of superconducting semiconductors discovered. In this context, in 2004, superconductivity has been found in boron-doped diamond (C:B) for the first time by Ekimov [60]. In highly doped diamond, the critical temperatures measured so far reaches 10K, for a boron concentration of the order of 0.5at.%.

Naturally, the discovery of superconducting highly boron-doped cubic silicon (Si:B) in 2006 was induced by the superconducting boron-doped diamond one. Considering that silicon crystallizes in the same pattern as diamond, the study of the superconducting silicon was the logical next step. Boron-doped silicon is superconducting below a critical temperature of 0.35K, with a critical field of about 0.4T and for a boron concentration rate of 5at.% [6]. The previous study of superconducting diamond gave precious indications concerning the dopant concentration rate to explore in order to fabricate superconducting silicon. In fact, it is necessary to dope the silicon layers with boron well above its solubility limit, which is around 1.2at.% ($6.10^{20}cm^{-3}$). Using dopant concentrations which overcome this limit imposes to consider not conventional out-of-equilibrium doping techniques which suit with this constraint. The challenge for these techniques is twofold : firstly, the doping methods performed have to highly dope silicon and secondly, they have to produce superconductivity in silicon. This was achieved by using two out-of-equilibrium laser doping techniques, the Gas Immersion Laser Doping (GILD) and the Pulsed Laser Induced Epitaxy (PLIE). The GILD has shown excellent performances in terms of homogeneous dopant concentration and activation. The first superconducting boron-doped silicon samples fabricated by the Institut d'Electronique Fondamentale (IEF, now C2N) of

Orsay and measured in 2006 as mentioned before, were obtained with the GILD.

In this chapter, I will first introduce the fabrication of the Si:B samples including the doping techniques by laser, followed by a short overview of the previous experimental results obtained on Si:B. Then, the general experimental characteristics of the fabricated Si:B SQUID will be presented. However, basic nanodevices such as nanotransistors start their fabrication from simple Silicon on Insulator (SOI) and not from bulk silicon. That is the reason why we are interested in making superconducting SOI, it is this same SOI which could be integrating in future nanotransistors. The laser doping technique will have to be adapted to the SOI, and then to a transistor structure-like. I will precise the limitations emerging. Afterwards, the SOI:B experimental measurements at very low temperature will be presented and discussed. Furthermore, X-Ray Diffraction (XRD) measurements were used to obtain complementary informations on SOI:B epilayers, I will specify the results brought by the use of this technique, which allows to probe precisely the crystallinity of the layers. Finally, the last part of this chapter will be dedicated to the first two SOI:B devices realized, the SQUID and the Hall bar.

3.1 Si:B superconductivity

3.1.1 Si:B epilayers fabrication and doping techniques

The well-known semiconductor silicon has been without doubt the basic element for the microelectronics since the last decades. It is actually a promising candidate for a large amount of new applications, as it inherits its potential from the highly developed silicon technology. The interesting properties of silicon, such as its relatively low price in comparison to other materials like gallium (Ga) or arsenide (As), its abundance on earth (silicon represents the second element in earth crust after oxygen), its good crystallisation and the native presence of a good oxide SiO_2, can explain its success and why it has been chosen by the microelectronics industry as the standard material.

The basic brick in microelectronics is the Metal Oxide Semiconductor (MOS) transistor, whose gate length can be used as a reference to define the level reached by the microelectronics technology. Silicon can be an appropriate candidate for quantum nanoelectronics, at the price of work in term of devices size reduction to go from the classical regimes to the quantum ones. Moreover, doping is an important ingredient of microelectronics and more generally of all the semiconductor physics. In fact, semiconductor highly doping appears definitely as a critical step for the future CMOS technologies and is widely studied. The realization of ultra-shallow and highly doped junctions with abrupt profile is a major challenge to extend the miniaturization of microelectronic devices. The reduction of the MOS transistor size requires techniques which allows to create these described junctions between the source and the drain. Importantly, the thinner the junction is, the higher the doping rate has to be to allow a good conduction in the device.

In this technological context, in order to overcome the solubility limit of boron in silicon by managing to substitute a very high silicon atoms rate with boron atoms, was developped an out-of-equilibrium laser doping technique in Orsay, the Gas Immersion Laser Doping (GILD) [61]. In 1999, at the IEF of Orsay, Boulmer used this doping technique to elaborate boron-doped silicon layers, well-beyond the boron solubility limit, and for different thicknesses going from 10nm to 80nm as presented in Fig.3.1 [62].

Naturally, we understand that with these measurements came the superconductivity of boron-doped silicon as an unexpected result, even if it was predicted. We will now focus on describing firstly the laser doping principle, and secondly the two doping methods performed to fabricate the superconducting silicon layers.

3.1.1.1 Laser doping principle

Conventional doping techniques reach their limits for the fabrication of ultra-shallow (10nm) and highly doped junctions (doping up to 10^{21}cm^{-3}) with abrupt profile. In comparison, we point out that laser doping techniques offer interesting solutions.

Laser doping is used to anneal layers with dopants introduced before (PLIE) or during the laser pulses (GILD). This corresponds to one of the most relevant differences between

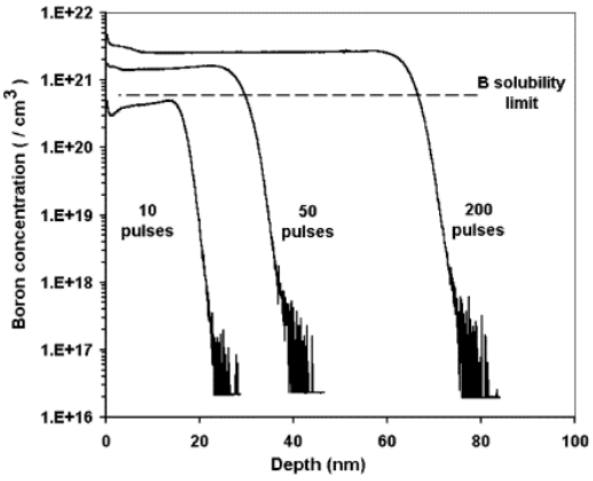


Figure 3.1: Boron concentration profile for three layers with different laser pulses number. The boron solubility limit is already reached for 10 laser pulses. [61]

the two doping methods. Unlike a classical annealing which heats the entire material volume, the laser annealing induces an increase of the material temperature but only locally at the surface. The used lasers have commonly a short pulse duration (usually equals to tens of ns) and generally emit UV radiation. We note that these properties will allow to realize cycles of fusion and recrystallisation on depths of the order of tens of nanometers in the material.

It is important to specify that the spatial repartition of the dopants at the end of the process will be on average homogeneous and will have a perfectly random distribution without boron aggregate. Another essential point to clarify is that the doped layer corresponds to the annealed layer, which means that the thickness of the doped layer is equivalent to the thickness of the melted layer.

3.1.1.2 GILD

GILD experiments were operated exclusively at IEF of Orsay. All the laser-doped samples were fabricated on p-type (001)-oriented silicon wafers with an initial doping rate of the order of 10^{15}cm^{-2}. I now specify the different steps occuring during the process of GILD.

GILD is an out-of-equilibrium doping technique. Before each doping experiment with GILD, the silicon sample undergoes a meticulous cleaning in a hydrofluoric acid solution (HF) in order to remove carefully the native oxide at the surface of the sample. The silicon layers doping runs in a ultra high vaccum chamber, at a pressure of 10^{-9}mbar, in order to avoid any sample contamination by impurities. The precursor gas BCl_3 is introduced in the chamber by a pulse valve at the surface of the silicon sample. One part of the gas molecules allows to saturate the chemisorption sites of the silicon wafer, the other one is pumped. After a short delay of 10ms, the first laser pulse is sent at the surface of the silicon wafer.

Laser-induced doping was performed with a 308nm wavelength pulsed excimer XeCl laser with an extremely short pulse duration of 25ns. During a laser pulse, the silicon melts over a thickness and a time that depend on the energy density of the laser. Boron atoms diffuse very rapidly into the melted phase. Finally, at the end of the laser pulse, boron atoms are incorporated in silicon substitutional sites during the recrystallisation. The principle of the doping is summarized and depicted in Fig.3.2.

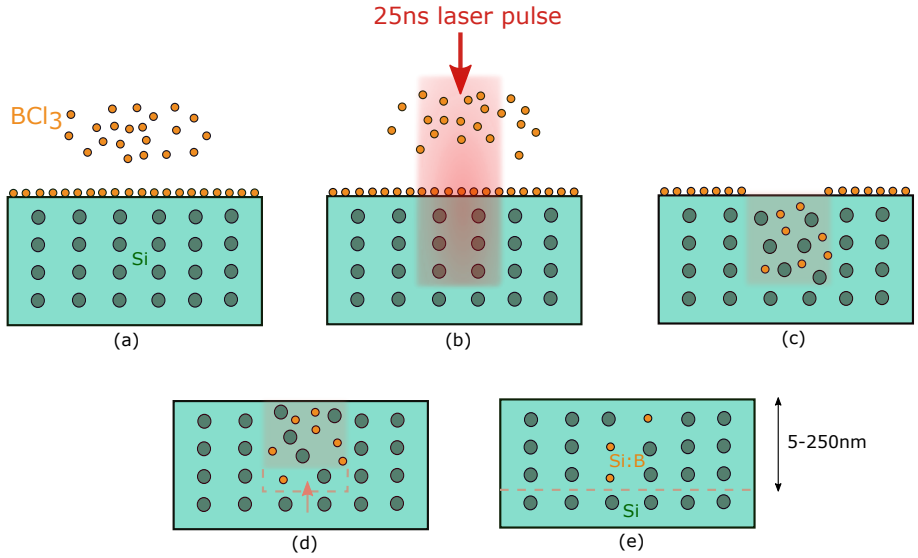


Figure 3.2: Principles of the Gas Immersion Laser Doping (GILD). (a) Introduction of the precursor gas at the surface of the Si wafer. (b) Melting of the silicon sample due to a laser shot, on a certain thickness ranging from tens to hundreds of nanometers. (c) Diffusion of the dopants. (d-e) Recrystallisation of the melted silicon. Trapping of boron atoms in substitutional sites of silicon. Formation of two different layers : Si:B layer on top and Si.

In this doping technique, we note the importance of two distinct parameters, the number of laser shots and the fusion time. With every new laser shot, boron atoms are incorporated. We can reasonably deduce that the number of laser shots defines simply the doping rate. Concerning the fusion time, it determines the thickness of the doped layer. These parameters are clearly decorrelated with the GILD.

Interestingly, the GILD process can be performed and cyclically repeated until the dopant concentration required is reached and this can go up to 10at.% of active boron atoms in silicon. Consequently, one major advantage of this doping technique is to be cumulative, allowing to reach the highest doping rates so far. Nevertheless, the efficiency of the technique is also dependent on certain doping atoms properties. For instance, the high mobility of boron atoms in melted liquid silicon is a crucial point, leading to a homogeneous repartition of the boron dopants in the final silicon epilayer.

Furthermore, the GILD finds its attractivity in the way that this method is well-controlled and reproducible. More precisely, the number of boron atoms introduced at

each laser pulse is always the same; it corresponds to $1.2.10^{14}cm^{-2}$. At the end of the high doping process, two other advantages of GILD have to be highlighted: firstly, the sharp Si:B/Si substrate interface and then, the complete absence of aggregates in the bilayer, revealed by Atom Probe Tomography as shown in Fig.3.3 [63]. The combination of these results allows to describe the Si:B layer performed with GILD technique as a well-defined random substitutional alloy, with promising superconducting properties. A photo of the global technical installation performing GILD is shown in Fig.3.4.

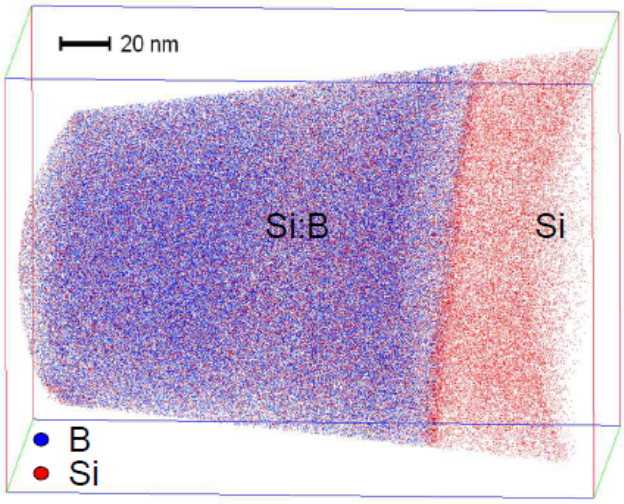


Figure 3.3: Atom Probe Tomography image revealing the sharp interface between the boron-doped silicon layer and the Si substrate. No cluster or precipitate is noticed in the bilayer material [63].

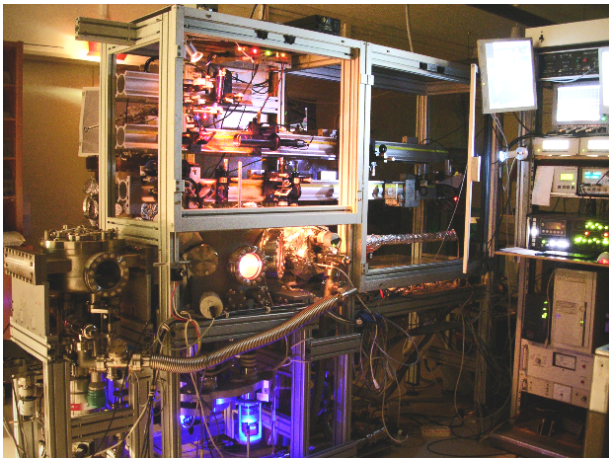


Figure 3.4: View of the technical installation performing GILD at IEF, Orsay. The installation regroups the high-vacuum chamber, the XeCl excimer laser, the doping gas, the optical arrangement with lens and mirrors, and the monitoring computer system.

Fine control over the doped layer: Experimental conditions

As we mentioned before, laser doping is realized in a ultra high vaccum chamber with a pulse excimer laser. The installed high vaccum is vital to avoid any contamination by other atoms which could be incorporated in the silicon during the melting of the material. The precursor gas BCl_3 introduced in the chamber has been chosen for its convenient property : in fact, during the crystallization, unlike boron atoms which will be incorporated in the silicon layer, chlorine will be rejected at the surface.

Moreover, excimer lasers are quite well adapted to surface treatments, and in our case to layers doping, for several reasons. First of all, the laser beam is very weakly coherent, limiting interferential and diffractive effects which would lead to an inhomogeneous and non-uniform treatment for a surface layer. Secondly, excimer laser appears as the only laser source which can deliver medium powers and considerable energies in the ultraviolet region. Typically, the excimer XeCl laser used offers an energy of 180mJ per impulsion. Finally, energy profiles for the laser impulsions of square shape are rather homogeneous on a surface of the order of cm^2.

The size of each doped layer on the Si wafer corresponds to the size of the laser beam; in Orsay, it is $2 \times 2mm^2$. The homogeneity of the laser beam is optimized, using the cutting of the beam in multiple sub-beams with an optical device of lens and mirrors. In a second step, the sub-beams are superimposed on the area to dope. The spatial uniformity and homogeneity of the energy density deposited by a laser shot is registered and controlled by an analysis system, here a CCD camera. The Fig.3.5 shows the squared spatial repartition of the energy density after homogenization by the optical device. In the central part of the square, we observe a good homogeneity of the energy density. However, a small divergence appears at the edges, which are less sharp.

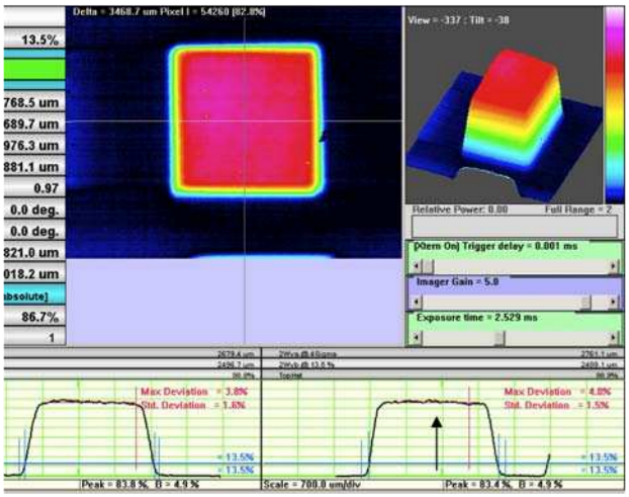


Figure 3.5: Photography of the square shape spatial repartition of the density energy for an laser shot. Taken from [64].

In-situ control of transient reflectometry

In order to control the steps of fusion and recrystallisation of the silicon, it is necessary to add an in-situ and temporally-resolved characterization tool, which helps to better understand involved phenomena during the laser annealing. The system should have a temporal resolution in the order of the nanosecond or less since the timescales we are working with are in the order of several nanoseconds. The transient reflectometry measurement is a technique well-adapted to the laser doping. It allows to measure the surface state of a material, as well as the thickness of a liquid layer, in our case the melted silicon, as presented in Fig.3.6.

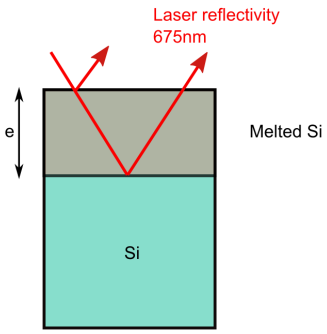


Figure 3.6: Scheme of the laser reflectivity principle.

This useful tool has its principle firstly based on the indice variation of the silicon, that is to say if the silicon is in its solid or liquid phase, allowing to evaluate the fusion, and secondly on the different doping rates, permitting to follow closely the silicon doping during the annealing process. The optical excitation of the silicon surface to study with a continuous laser gives rise to a partial reflection at the surface. The reflected signal is then collected and analysed with a photodiode. The wavelength of this continuous laser has to be chosen regarding the silicon properties and depending on the material depth we want to work with. The laser used for the in-situ control has a power of several mW at the wavelength of 675nm, with a temporal resolution of 1ns, which perfectly fits with the considerations explained above.

The thickness of the electrical activated layer is equal to the thickness of the melted layer, because in the doping process, the dopants diffusion happens only in liquid phase and thus, the melted depth can be assimilated to the doping depth. The melting time, measured by transient reflectivity, can be correlated to the doping depth for each laser impulsion.

Fig.3.7 presents several curves of transient reflectivity at 675nm measured for different laser energies, going from 600mJ/cm^2 to 950mJ/cm^2. The brutal variation of the reflectivity registered is clearly caused by the melting of the silicon layer. The transient reflectivity doubles, when a sufficient silicon thickness of 20nm is melted, and then saturates.

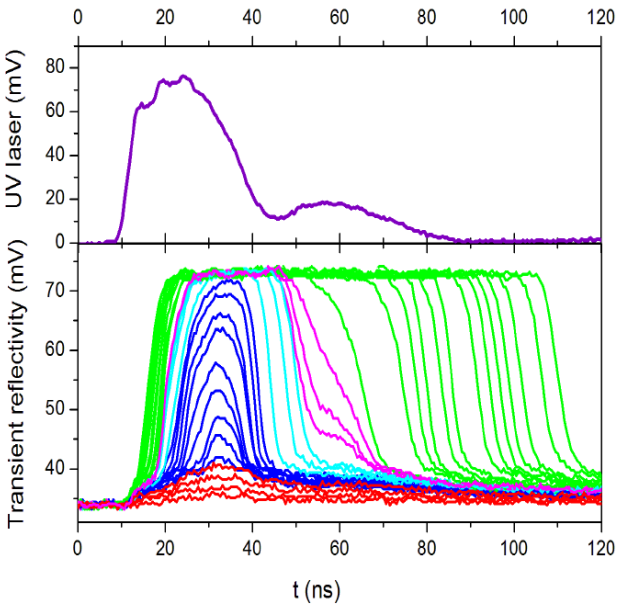


Figure 3.7: Transient reflectivity evolution at 675nm for several laser energies. The variation of the transient reflectivity indicates the beginning of the melting. For higher laser energies, the transient reflectivity increases and saturates for a melted layer thickness of 20nm.

The melting time, monitored by transient reflectivity, allows to calculate indirectly the doping depth. The doping depth increases linearly with the melting time, as we noticed in Fig.3.8.

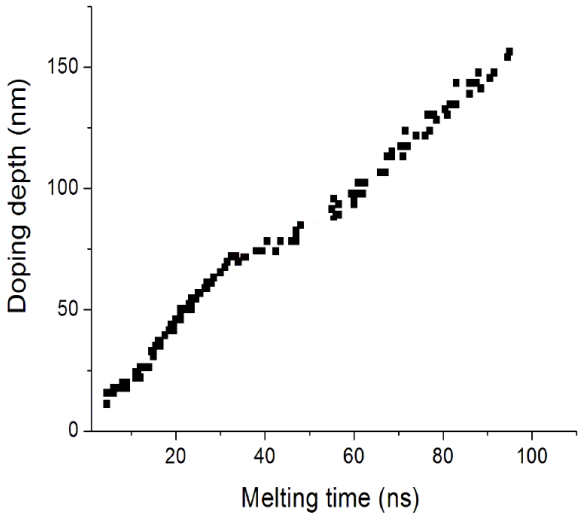


Figure 3.8: Doping depth as a function of the melting time, regardless of the doping rate.

Conclusion

The first out-of-equilibrium laser doping technique GILD described in this manuscript generates boron-doped silicon layers, at a doping rate well beyond the boron solubility limit, making them superconducting. This cumulative and reproducible method presents many advantages and allows to control with a high precision the doping and the thickness of the annealed layer.

3.1.1.3 PLIE

The second out-of-equilibrium doping method used to dope silicon layers with boron atoms is PLIE. In this case, the layers are initially preimplanted with dopants. It is actually this initial preimplantation dose which allows to determine the final achievable concentration. Consequently, a very few number of laser shots (usually one or two) are necessary in this doping technique, in comparison to the GILD requiring repeated cycles of chimisorption, fusion, diffusion of dopants and recrystallisation, with a large number of laser shots (up to $\simeq$ 200-300 in our studies). The laser shots are here useful to redistribute the boron dopants on a certain thickness and to recrystallize the doped layer. With the PLIE, the doped thickness and the final concentration are closely correlated. The principle of the PLIE is summarized on Fig.3.9.

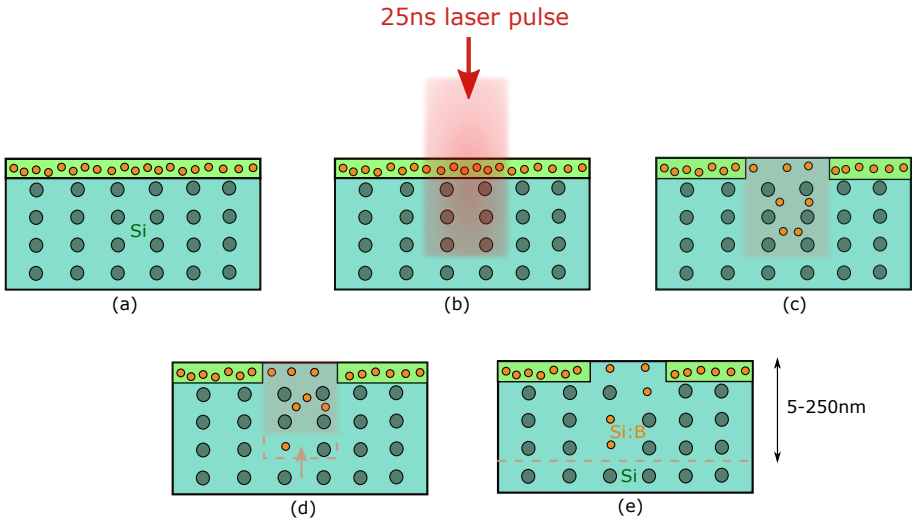


Figure 3.9: Sketch explaining the principle of the PLIE (Pulse Laser Induced Epitaxy). (a) Preimplantation of the dopants. (b) Melting of the preimplanted silicon sample. (c) Diffusion of boron atomes. (d-e) Recrystallisation of the liquid silicon.

3.1.2 Overview of the previous experimental results

Before the beginning of this thesis, series of GILD and PLIE samples were realized, mostly during Audrey Grockowiak's thesis [64], who studied the properties of very highly doped

silicon layers on bulk silicon wafers. The principal aim of this work was to investigate the different parameters affecting superconductivity of highly doped silicon, such as the dopant concentration, the doped layers thickness and also the doping technique. The work was focused on boron-doped silicon, as the tests with other dopants like phosphorus, aluminum, gallium and arsenic were unsuccessful.

This section will regroup major results obtained before my thesis.

GILD samples: Dependence of the critical temperature T_c with the doping rate n_B

The dopant concentration and the thickness of the doped layer are two crucial parameters. Firstly, for GILD Si:B samples, I present the evolution of the critical temperature as a function of the boron concentration, at a fixed Si:B thickness of 50nm. The curves associated are shown in Fig.3.10. This graph considers five layers of boron doped silicon with different doping rates, from 1.5at.% to 12at.%. For each doping rate, the resistance normalized with the normal resistance as a function of the temperature is plotted. We can notice that the superconducting transitions appear at different critical temperatures. We observe that the higher the doping rate, the higher the critical temperature.

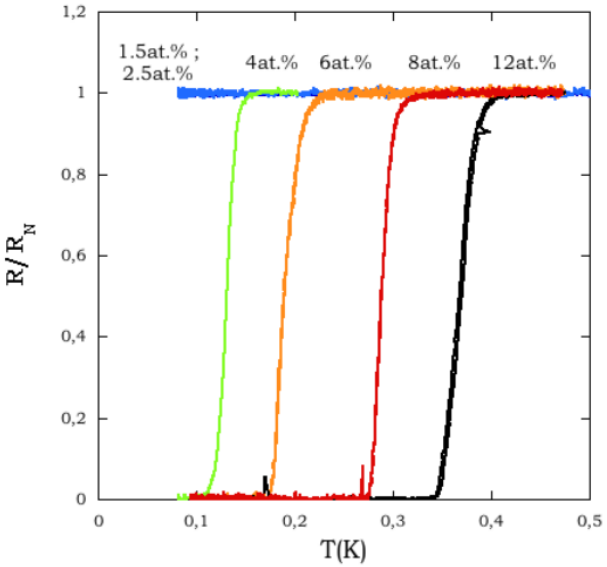


Figure 3.10: Resistance normalized with the normal state resistance as a function of the temperature for different layers of boron-doped silicon with thickness of 50nm. Extracted from [64].

GILD samples: Dependence of the critical temperature T_c with the thickness of the doped layer d

Fig.3.11 presents the critical temperature of different Si:B samples as a function of the boron concentration, and for different thicknesses of the doped layer, varying from 20nm

to 200nm. First of all, the global shape of the T_c as a function of the doping rate obtained on samples at 23ns/50nm, is confirmed for all the various measured thicknesses. From this figure, we can clearly deduce that the T_c depends on the boron concentration n_B, but also on the thickness d. In fact, for fixed concentration, the critical temperature increases undoubtedly with the thickness.

Secondly, superconductivity seems to appear only above a certain critical concentration of boron atoms $n_{B,c}$. We observe also a strong rise of the T_c with the boron concentration, for rather weak n_B. For larger n_B, the critical temperatures continue to increase before starting to saturate. The maximal critical temperature obtained is close to 0.7K.

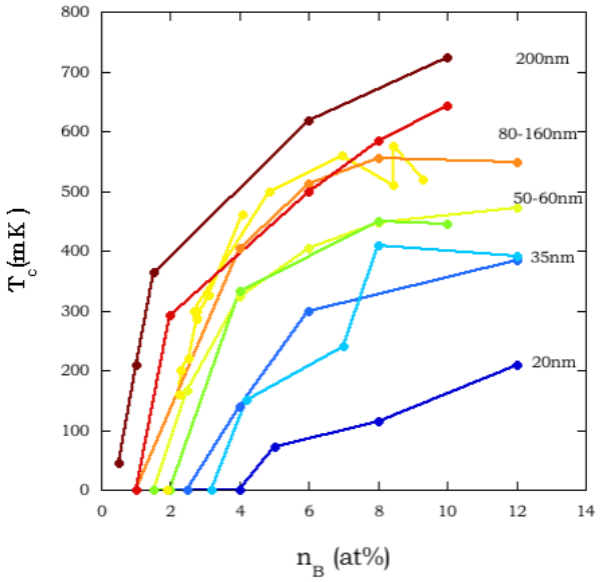


Figure 3.11: Critical temperature as a function of the boron concentration, for different thicknesses, ranging from 20nm to 200nm. Extracted from [64].

PLIE and GILD samples: Dependence of the critical temperature T_c with n_B and d

PLIE Si:B samples were also realized and measured. We note B+ Si:B samples preimplanted with a boron dose of $2.5.10^{16}$cm^{-2} and B++ those with a larger boron preimplantation of 5.10^{16}cm^{-2}, all fabricated with an implantation energy of 3keV.

As we can notice from Fig.3.12, while the T_c of GILD samples sharply increase with the boron concentration until the saturation at large n_B, the T_c of PLIE samples appear to remain constant. We remind here that for PLIE doping, the thickness and the doping rate are closely correlated, as explained before in the description of the PLIE technique. More precisely, for B+ samples, the corresponding T_c are close to 200mK, and for B++ samples, T_c is in the order of 300mK. It proves that the T_c is only defined by the boron dose.

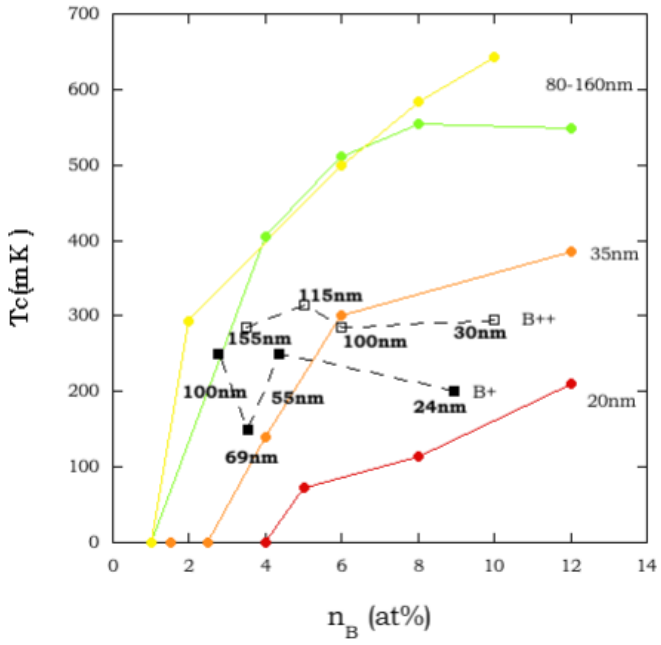


Figure 3.12: Critical temperature as a function of the boron concentration, for GILD samples at different d, and for PLIE samples preimplanted with different doses. GILD samples are presented with circular points and PLIE samples with squared points. Extracted from [64].

Conclusion

Boron-doped silicon samples have already been realized with the two laser doping techniques and characterized to extract the different parameters affecting superconductivity. Both doping methods (GILD and PLIE) allow to fabricate superconducting Si:B layers. All the results obtained before my thesis represent a solid basis for my work. As I am interested in making superconducting SOI, initial brick of nanodevices such as MOSFETs, I had to consider these doping techniques and adapt them. Moreover, a small number of PLIE Si:B samples realized with only two different doses has shown that the T_c was only dependent on the boron dose. This is an important result, which has to be confirmed with additional PLIE Si:B samples.

3.1.3 First device integrating Si:B: SQUID

Silicon technology offers great advantages such as reliability and maturity [7]. Moreover, as shown before, preparation conditions of superconducting silicon layers have been both improved and optimized with GILD especially. Superconducting boron-doped silicon samples can be now fabricated in a very precise and reproducible way. In this context, the first

chosen application of superconducting Si:B is the realization of SQUIDs (Superconducting QUantum Interference Devices), made entirely of silicon.

The samples presented in this section are the first superconducting Si:B SQUIDs. The experimental results obtained on one silicon SQUID have been recently published [65].

Fabrication

A SQUID is a very sensitive magnetometer used to measure extremely low magnetic flux. The device is simply based on superconducting loops containing two weak links in parallel acting as two Josephson junctions. During my thesis, we have fabricated a SQUID from a single layer of superconducting silicon. This superconducting film was obtained by heavily doping the silicon layer with boron atoms using GILD. The doping method has been precisely described above.

The initial superconducting silicon layer used in the present study was fabricated at the IEF of Orsay. It was made with 200 laser pulses and a melting time of 47ns, giving a final Si:B thickness equals to 80nm and a boron doping of the order of 5at.%, which corresponds to a boron dose of $2.4.10^{16}$cm^{-2}.

Starting from this superconducting film, several SQUIDs were realized; all of them have the rigourous same loop area, only the weak links dimensions were different. More precisely, the dimensions of the weak links range from 80nm to 200nm in width and from 100nm to 500nm in length. In the article published and in this section, I present the results obtained on a SQUID with weak links of 100nm by 100nm. The dimensions of the studied SQUID are indicated on the SEM image presented in Fig.3.13.

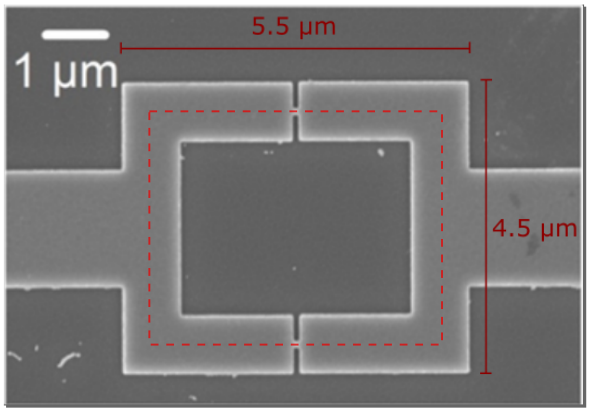


Figure 3.13: SEM image of the Si SQUID composed of two weak links of 100nm by 100nm.

The realization of the SQUID geometry requires several steps, executed in cleanroom at the PTA, in the CEA, in Grenoble. As a first step, an electron beam lithography is performed in order to define the shapes of the wanted device, that is to say the loops, the weak links and the contacts. Then, a 20nm-thick aluminum (Al) hard mask is deposited by lift-off to protect the silicon. The unprotected silicon (with a thickness roughly equal

to 100nm) is afterwards etched away by Reactive Ion Etching (RIE). The Al hard mask can now be entirely removed by wet etching. Finally, contacts pads are defined by optical lithography and, titanium (Ti) and gold (Au) are evaporated, after a short HF cleaning to remove the native SiO_2 oxide.

Experimental results

The superconducting silicon SQUID has been then measured at very low temperature in a dilution cryostat. The curve of the resistance as the function of the temperature is shown in Fig.3.14. We note a critical temperature of 260mK, which is consistent with our expectations for such a Si:B layer with this precise thickness and doping rate. Moreover, we clearly observe an abrupt and complete superconducting transition for the SQUID, meaning that the entire structure exhibits superconductivity at 260mK.

At higher temperature, the resistance of the device shows a clear metallic behavior, as presented in Fig.3.15.

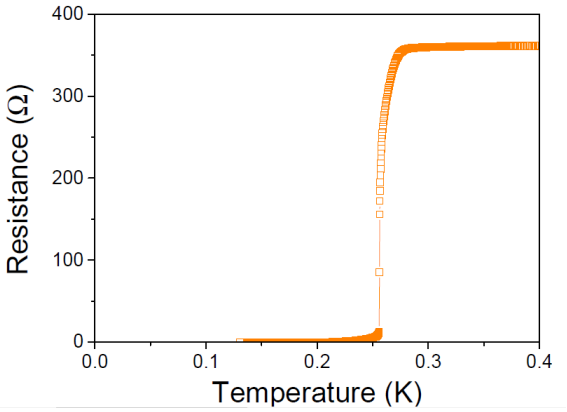


Figure 3.14: Resistance of the device as a function of the temperature : complete superconducting transition of the Si:B SQUID.

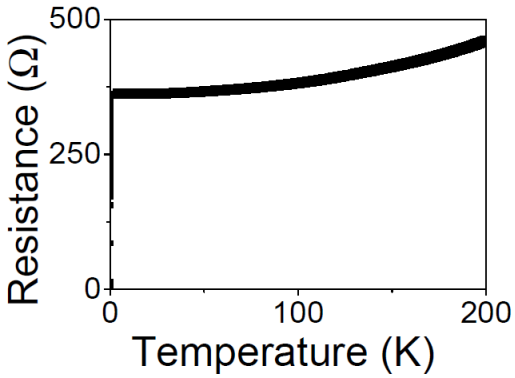


Figure 3.15: SQUID metallic behavior at higher temperature.

I-V characteristics (see Fig.3.16) obtained at 100mK allows us to identify the SQUID critical current I_c of 4μA and the re-trapping current I_r, even if the latter is fairly weak. Below the critical temperature, the I-V characteristics presents a strongly hysteretic response. Furthermore, for current larger than I_c, the slope of the I-V curve, that is to say the resistance of the device, equals 360Ω, which corresponds exactly to its resistance at 4K, well above the critical temperature. Therefore, when the current reaches the critical current, the entire structure of the SQUID becomes normal. This can be easily explained by the fact that a heating process happens and propagates from the two junctions to the rest of the structure.

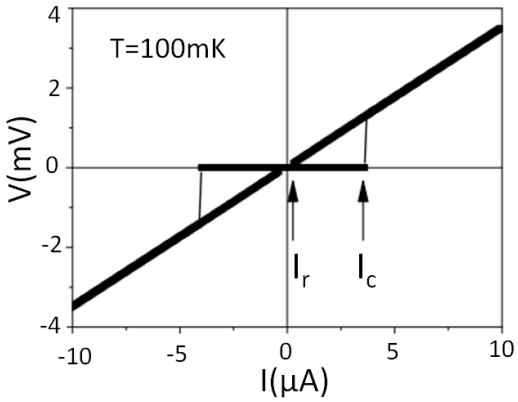


Figure 3.16: I-V characteristics measured at 100mK. I_c corresponds to the critical current and I_r shows the re-trapping current.

Now we aim at estimating the product $R_N I_{c,wl}$ and comparing to the value of Δ/e. Here, R_N is the normal state resistance of one junction composing the SQUID and $I_{c,wl}$ corresponds to the critical current of this junction.

As explained before, the normal state resistance of the SQUID is 360Ω. Considering the geometry of the SQUID, we can deduce the sheet resistance starting from the normal state resistance of the device. Given the square shape of one weak link corresponding to one junction, it directly comes that the normal state resistance of one junction R_N equals to the sheet resistance, approximately equals to 14Ω. Furthermore, for symmetrical reasons, we can directly calculate the critical current of one junction, we obtain $I_{c,wl} = I_c/2 = 2\mu$A, giving straightforward the product $R_N I_{c,wl} \simeq 28\mu$V.

Concerning the superconducting gap at zero temperature, it can be estimated using the BCS relationship [66]

$$\Delta(0) = 1.76 k_B T_c \ . \tag{3.1}$$

Considering the critical temperature of 0.26K, we easily obtain $\Delta/e \simeq 40\mu$V. Hence, we conclude that $R_N I_{c,wl} = \alpha\Delta/e$, with $\alpha = 0.7$, which is consistent with previous calculations [23], [25], since in our case the nanobridge length is larger than the zero temperature coherence length.

Another essential study in devices such as SQUID especially, is the effect of the magnetic field. The dependence of the critical current with the magnetic field was also investigated, for several various temperatures, ranging from 100mK to 260mK, the latter corresponding to the critical temperature of the device. In our case, the magnetic field is applied perpendicular to the studied sample. For a SQUID, one would expect that its critical current is periodically modulated with a period Φ_0 as a function of the magnetic flux.

We clearly observe this interesting effect, plotted in Fig.3.17. The curves presented here have all been obtained by ramping the magnetic field from -5G to 5G, with steps of 0.1G. The curves express a highly regular oscillation of the critical current as a function of the applied magnetic flux, with a measured period ΔB of 1G. This value coincides with one flux quantum $\Phi_0 = h/2e = 2.10^{15}$Wb in a surface area of $20\mu m^2$, which corresponds to the surface of the SQUID loop of 4μm by 5μm (dashed line in Fig.3.13).

When increasing the temperature, the oscillations gradually decrease and start to vanish when approaching the critical temperature.

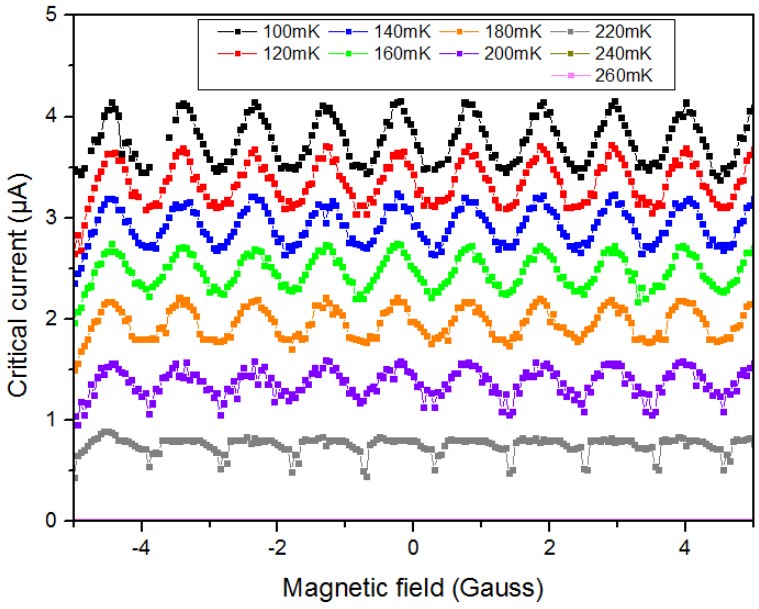


Figure 3.17: Evolution of the critical current as a function of the magnetic field, for different temperatures, from 100mK to the critical temperature of 260mK.

The weakness of the modulation amplitudes observed can be reasonably explained either with SQUID asymmetry reasons or either with the kinetic inductance of the SQUID. The modulation rate of the critical current amplitudes $\Delta I_c/I_c$ depends on the so-called screening parameter β_L, given by

$$\beta_L = \frac{2\pi L I_c}{\Phi_0} \ . \tag{3.2}$$

It is shown that for a fixed I_c, the modulation decreases when increasing β_L [67], [68]. The global inductance L can be expressed as the sum of the geometric inductance L_g and the

kinetic inductance L_k,

$$L = L_g + L_k \ . \tag{3.3}$$

In a superconducting material, L_k comes from the motion of the Cooper pairs. The kinetic inductance can be defined as follows [69],

$$L_{k,sq} = \frac{R_{sq}h}{2\pi^2\Delta} \frac{1}{\tanh\left(\frac{\Delta}{2k_BT_c}\right)} \tag{3.4}$$

with R_{sq} the sheet resistance in the non-superconducting state, k_B the Boltzmann constant, Δ the superconducting gap and T_c the critical temperature of Si:B.

We can derive the geometric and kinetic inductance of the device. Taking into account the dimensions of the SQUID, it comes $L_g = 2.5$pH and $L_k \sim 340$pH. We deduce that the geometric inductance is negligible compared with the kinetic inductance. From these values, we estimate the screening parameter $\beta_L \sim 2$. Following [68] and Fig.4 therein, we see that it predicts an amplitude modulation of 20-30% which is very consistent with our findings. We then conclude that the rather weak amplitude of modulation is mostly due to the kinetic inductance.

For superconducting weak links, the amplitude of the critical current strongly depends on the length of the bridge compared to the superconducting Ginzburg-Landau (GL) coherence length ξ. Considering the formulas written above, it is clear to deduce that if the length of the nanobridge increases, the amplitude of the critical current decreases. The modulation depth is reduced as soon as the coherence length becomes shorter than the bridge length.

Consequently, to provide a Josephson effect and a good modulation, the length of the bridge has to be smaller than the coherence length of the material. For example, typical values for the coherence length of aluminum range from 100nm to 1μm, according to the purity of the material. Concerning niobium, its coherence length is fairly close to 10nm. Even if niobium has the major advantage to benefit from higher critical temperatures than aluminum, it appears that Al junctions are more suitable to preserve a good modulation of the critical current.

In the case of superconducting silicon, we can derive its coherence length using the dirty limit. In this limit, the coherence length ξ equals to $\sqrt{\xi_0 l_0}$ where ξ_0 corresponds to the BCS coherence length and l_0 is the elastic mean free path [23]. Taking into account the doping rate of the present superconducting silicon, we estimate $\xi_0 \simeq 1\mu$m and $l_0 \simeq 2-3$nm, resulting to a zero temperature coherence length $\xi(0) \simeq 40-50$nm. The Si:B coherence length is smaller than the nanobridge length of 100nm; hence, it confirms the weakness of the critical current amplitude.

Furthermore, a simulation of the Ginzburg-Landau equations has been operated starting from a code developped by Hasselbach et al. [70] to find and confirm the critical current evolution as a function of the temperature and the magnetic field. The GL equations have

been solved numerically in 2D. At the beginning of the calculations, we assume that a macroscopic superconducting wave function can be defined as

$$\psi(r) = f(r)\psi_\infty e^{i\phi(r)} \tag{3.5}$$

with the parameters f and ϕ depending on the position and ψ_∞ constant.

For the simulation, we chose to fix $f = 1$ at both left (L) and right (R) sides of the device, as sketched on Fig.3.18(a). In addition, we assume a certain phase ϕ_L and ϕ_R at the left and right sides of the SQUID, generally $\phi_L = -\phi_R$. Finally, we get the amplitude f and the phase ϕ everywhere along the device.

The Fig.3.18(b) presents a color plot of the local superconducting phase ϕ for a total phase difference $\Delta\phi = \phi_L - \phi_R \simeq 3\pi/2$. It appears that the phase evolves locally and drops exactly at the junction bridges. Repeating the same operation for several phase differences allows us to determine at the end the current-phase relationship, and consequently, the evolution of the critical current as a function of the magnetic field.

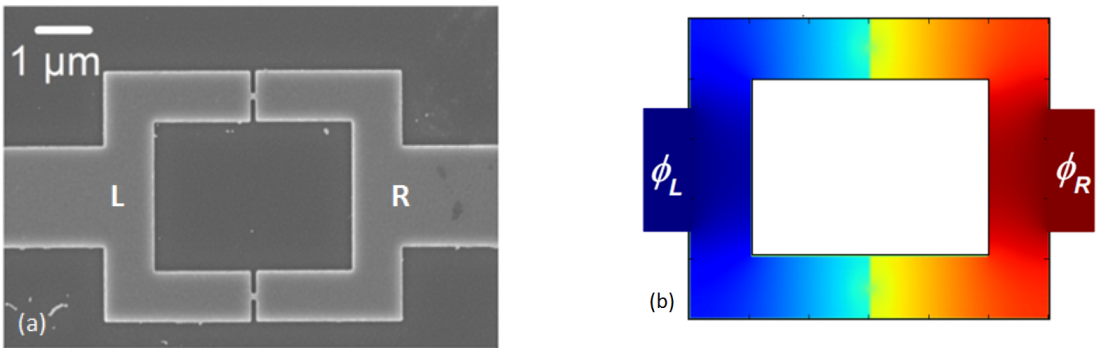


Figure 3.18: (a) SEM image of the studied SQUID with explained L (left) and R (right) positions. (b) Color plot of the superconducting phase for a total phase difference $\Delta\phi \simeq 3\pi/2$. This phase drops at the junction nanobridges of the SQUID.

The simulation gives both the magnetic field dependence and the temperature dependence of the critical current, see Fig.3.19. The last one is obtained by taking into account the temperature dependence of the GL coherence length. The simulations are in really good agreement with experimental results.

Conclusion

We have fabricated our first superconducting full silicon working device, which will act as a stepping stone for future nanofabrication and measurements. One important point to remind is that the superconducting silicon SQUID offers the high advantage to use the silicon technology, which is CMOS compatible. We measured periodic oscillations of the critical current of the device as a function of the magnetic flux, which correspond to the signature of the expected SQUID effect. The magnetic field and the temperature

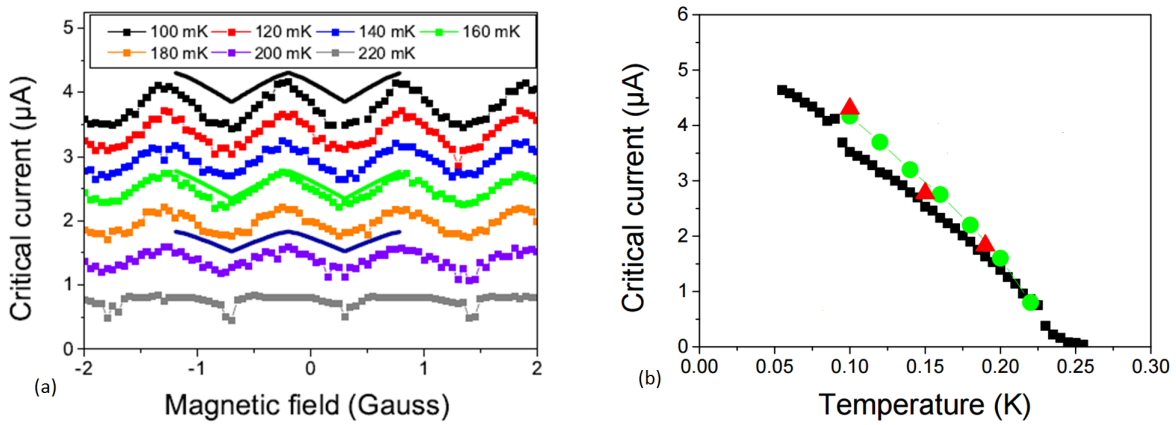


Figure 3.19: (a) Critical current of the device as a function of the magnetic field, for different temperatures. The solid lines correspond to the simulations, made for various temperatures: 100mK, 150mK and 190mK. (b) Critical current evolution as a function of the temperature (black squared points). The critical current disappears when reaching the critical temperature. The maximum critical current obtained by measuring the magnetic flux modulation is also plotted as a function of the temperature (green circles). Finally, the red triangles come from the derivation of the Ginzburg-Landau equations.

dependence of the critical current can be simulated by resolving numerically the Ginzburg-Laudau equations and the obtained simulations have shown great accordance with the experimental measurements.

I chose here to present the results obtained on one Si:B SQUID with one weak links size and one doping rate. However, the measured features are totally reproducible for devices with various bridge dimensions and fabricated from different Si:B films. All of these promising results highlight the fact that superconductivity in silicon can be described by a macroscopic wave function.

3.2 SOI:B superconductivity

We want to conceive and fabricate a non dissipative Josephson Field Effect Transistor (JOFET) with superconducting source and drain contacts. The idea is to build a new type of superconducting qubit based on the Josephson effect. However, the realisation of such a nanotransistor is not straightforward, mainly due to the major difficulty of avoiding the Schottky barrier usually present at the interface between the contacts (metallic superconductor) and the channel (semiconductor), which prevents Cooper pairs to leak into the channel for the Josephson effect. Moreover, the superconducting material composing the source and drain, will have to be compatible with the silicon technology. From fundamental point of view, the interplay between Coulomb blockade and superconductivity is here crucial and will be deeply studied.

In the present thesis, we have considered two ways to incorporate superconductivity in nanodevices such as nanotransistors. The first road as I explained before, is to use superconducting silicon. The good quality of superconducting doped silicon layers is based on the many advantages of the laser doping techniques, especially the GILD. Standard fabrication processes, well-optimised for silicon, could be adapted and employed to SOI (Silicon On Insulator) firstly, and then to more complex nanostructures like MOSFETs. Furthermore, creating a superconducting silicon/silicon junctions at the location of the source and drain contacts during the doping process, would have the great advantage to form an extremely clean and transparent interface. The second way to introduce superconductivity in nanotransitors is related to superconducting silicides, in our case PtSi. The latter will be discussed further in my thesis and will be the main subject of the next chapter.

Laser doping methods allow to fabricate superconducting silicon layers with well controlled concentration and doping depth. We now aim to extend these fabrication techniques to SOI, in order to make it superconducting. Realizing superconducting SOI is a really difficult exercise due to the thin thickness of the silicon layer above the buried oxyde (BOX). In fact, during the doping, one single laser shot sent too deeply in the SOI, will touch the SiO_2 and will literally destroyed the structure by preventing any recrystallisation.

For the fabrication process, we have worked with the IEF of Orsay to perform both GILD and PLIE SOI:B samples. Si:B samples were also fabricated in order to trace back the previous results of Audrey Grockowiak.

We have also collaborated in a second step with the LETI and the LASSE company (now SPLEEN) to make PLIE SOI:B samples and start testing possible integration. If superconductivity was obtained for SOI, with the laser doping expertise, the LETI could afterwards realize the entire process of fabrication for superconducting transistor as they are already now building transistors.

We have measured the transport properties of GILD and PLIE samples at very low temperature either in the PPMS (Physical Properties Measurement System) or in a He^3/He^4 dilution refrigerator. I will present these results. X-ray diffraction measurements were also made on these samples; we will examine the accordance with the low temperature results.

Finally, I will present the two first fabricated superconducting SOI:B devices, the SQUID and the Hall bar.

3.2.1 Superconducting SOI:B with GILD

We want to take advantage of the well-known silicon technology and the superconductivity to make nanoMOSFETs with source and drain which are superconducting thanks to the laser doping and laser annealing. As we control well the fabrication of superconducting silicon, we now have a huge interest of making superconducting SOI.

At the LETI of Grenoble, before the start of my thesis, laser annealing has already been made on nanodevices, and more precisely on PMOS transistors presenting a 30nm thick SiN cap layer on top [71]. Fig.3.20 shows two TEM images of PMOS planar Fully Depleted Silicium On Insulator (FDSOI) devices before and after the laser annealing.

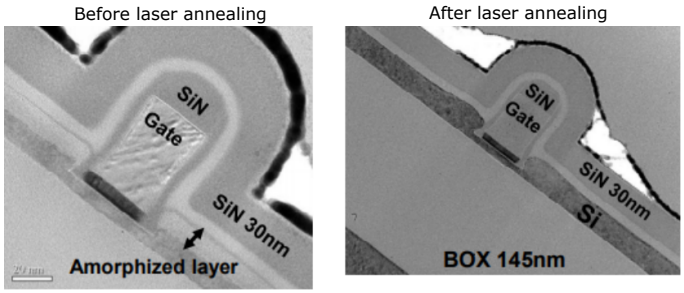


Figure 3.20: TEM images of a PMOS FDSOI device before and after the laser annealing with BF_2 (boron and fluorine) Lightly Doped Drain (LDD) implantation [71].

This result suggests that the whole structure of the PMOS device was not damaged by the laser shot of the laser annealing. The source and drain silicon film seems to have recrystallised without any gate morphological degradation. This promising observation corresponds exactly to the starting point, which let us think that we could repeat the same operation with our transistors and dope the silicon of the source and drain enough to make it superconducting, without detroying the initial structures.

Before realizing such transistors with superconducting source and drain, we first need to examine the superconductivity of Silicon On Insulator. Full sheet SOI corresponds to a well-known substrate composed of three layers, widely used in microelectronics fabrication, see Fig.3.21. The silicon layer on top is single-crystalline and sits on an insulating material, the silicon dioxide SiO_2. For GILD, we have chosen a thickness of 23nm for the Si active layer as it corresponds to what could be done in a real device. The whole structure rests on a mechanical substrate, the silicon. The oxide layer between the active top silicon layer and the mechanical silicon substrate is called the buried oxide (BOX).

In comparison to bulk silicon, due to the thin thickness (23nm) of the top Si layer of the substrate, making superconducting SOI is a different challenge. Indeed, the demanding task with laser annealing is really difficult because the laser pulses sent at the surface of

the SOI substrate should never reach the BOX, even a single time, otherwise the following recrystallisation would be impossible; as no recrystallisation exists over SiO_2. Moreover, during the doping procedure at Orsay, another issue is added, it is related to the difficult control of the doped thickness, caused by interferences present in the transient reflectivity, as we can see in Fig.3.22.

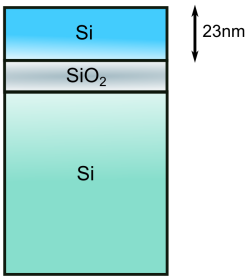


Figure 3.21: Sketch of the SOI substrate used for this study.

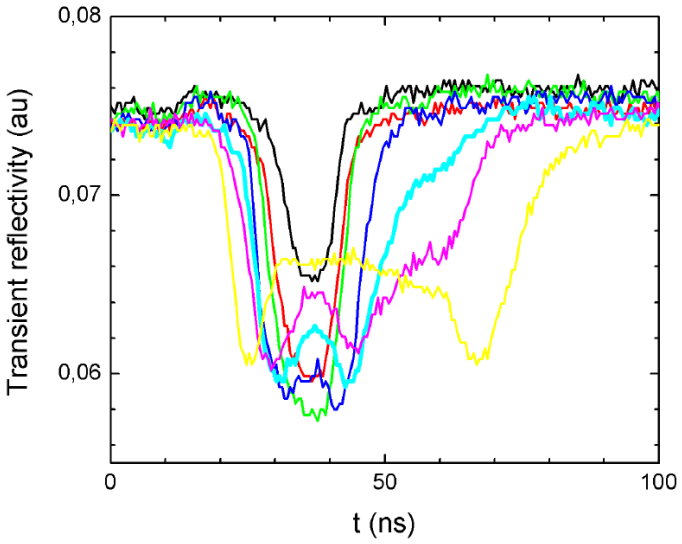


Figure 3.22: Transient reflectivity curves for different laser energies, showing interferences. Curves realized on SOI substrate at IEF, Orsay.

First tests on 23nm Full Sheet SOI with a boron concentration of 10^{21}cm^{-3} were performed to find the good laser conditions to melt the silicon layer. Fig.3.23 shows the sheet resistances R_{sq} of SOI:B samples as a function of the laser energies E, and for different number of laser shots. It indicates that an increased number of laser shots promotes a homogeneous dopant distribution and decreases the overall resistance. Furthermore, increasing the laser energies leads to lower the sheet resistances, until we reach the damage threshold. At this point, R_{sq} suddently diverge, meaning that the BOX has been touched

by at least one or several laser shots. These curves give the range of laser energies to use in order to avoid to destroy our samples during the doping process.

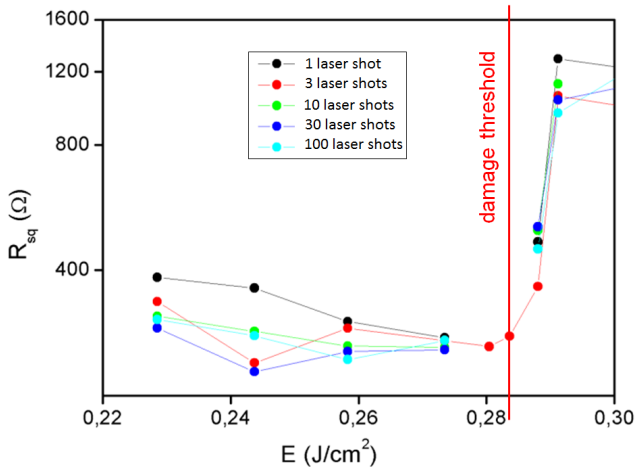


Figure 3.23: Sheet resistance of the SOI:B samples as a function of laser energies, for different number of laser pulses.

At first, we decided to fabricate our first boron-doped SOI samples with GILD technique at the IEF of Orsay, as it is presented in Fig.3.24. We remind here that the initial boron dose of the top Si layer is 1.10^{15}cm^{-2}, and each laser shot adds $1.2.10^{14}$cm^{-2} for the final boron dose. All in all, we realized ten samples of SOI:B with different number of laser shots and with different adapted laser energies.

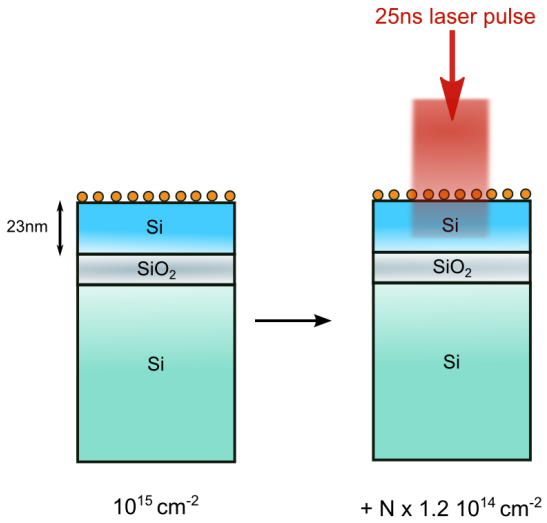


Figure 3.24: Sketches of GILD process with full sheet SOI samples. The initial dose of the silicon is 1.10^{15}cm^{-2}. Each laser shot N adds $1.2.10^{14}$cm^{-2} for the final boron dose.

Afterwards, the samples have all been measured at very low temperature in a dilution cryostat, in order to enlight their transport properties. We present these SOI:B samples with their associated properties such as their normal resistances at 4K R_N, their resistances at 300K R_{300K}, their boron doses n_B and their critical temperatures T_c in Tab.3.1. The sample names give the date of fabrication.

Sample name	Laser shots	E (mJ/cm^2)	T_c(mK)	$R_N(\Omega)$	$R_{300K}(\Omega)$	n_B(cm$^{-2)}$	n_B(at.%)
20160915-1	100	236	150	6.98	9.89	$1.3.10^{16}$	11.3
20160915-2	100	241	160	6	8.7	$1.3.10^{16}$	11.3
20160915-3	150	225	170	7.2	9.9	$1.9.10^{16}$	16.5
20160915-4	150	230	230	8.1	10.9	$1.9.10^{16}$	16.5
20160915-5	200	209	125	8	11.6	$2.5.10^{16}$	21.7
20160915-6	200	214	135	14.7	17.58	$2.5.10^{16}$	21.7
20160915-7	200	219	185	8.5	11.7	$2.5.10^{16}$	21.7
20160915-8	250	193	125	15.5	18.6	$3.1.10^{16}$	26.9
20160915-9	250	209	120	16.7	20.7	$3.1.10^{16}$	26.9
20160915-10	300	193	<48	15.5	19.5	$4.6.10^{16}$	40

Table 3.1: GILD samples fabricated in Orsay

We can notice that nine out of ten GILD SOI:B samples are superconducting, which is a promising result. Fig.3.25 presents the resistance normalized by the normal resistance at 4K as a function of the temperature for four SOI:B samples with different boron concentration, ranging from 11.3at.% to 26.9at.%. The superconducting transitions are all complete. However, critical temperatures are rather weak in comparison to those associated to superconducting bulk silicon; it ranges from 120mK to 230mK. From these measurements, we cannot deduce a clear dependence of the critical temperature with the boron concentration, as it was established for the boron-doped bulk silicon samples.

Importantly, I want here to specify that the boron concentrations n_B in at.% are theoretical and have been calculated by considering a top boron-doped silicon layer of 20nm (lower than 23nm). Given the very high concentrations ($n_B > 10\%$), it is likely that all the boron atoms are not active.

Conclusion

Despite the major difficulty of operating laser annealing on SOI substrate, superconductivity was observed on almost all the highly doped SOI (23nm) samples obtained with GILD technique at Orsay. Boron doses associated to superconducting SOI:B samples vary from $1.3.10^{16}$cm^{-2} to $3.1.10^{16}$cm^{-2}. Even if the measured critical temperatures are relatively low, these results show great potential.

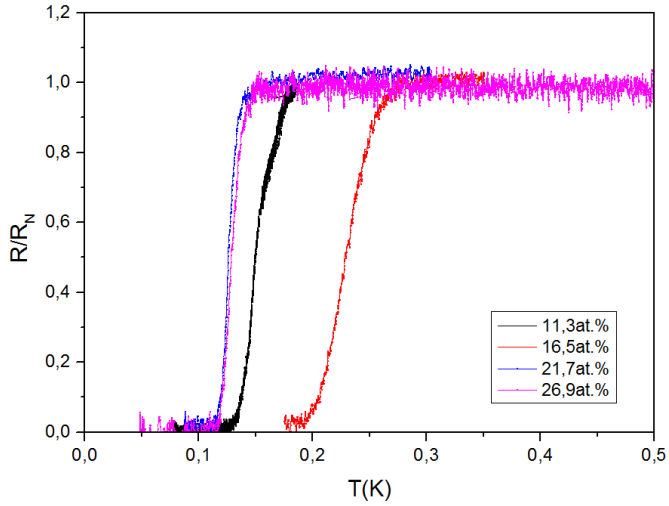


Figure 3.25: Evolution of the resistance normalized by normal resistance as a function of temperature for four SOI:B samples with different boron concentration, showing complete superconducting transitions.

3.2.2 Superconducting SOI:B on nanodevices

Superconducting SOI:B samples have been obtained with GILD. We remind that we aim at observing superconductivity effects on electric transport of a silicon field effect transistor at very low temperature.

For this reason, we have performed laser annealing on predefined nanostructures for which the fabrication process was stopped after the transistor was defined but before the RTA (Rapid Thermal Annealing). The annealing allows the recrystallisation of the structure and the activation of the dopants. These non-annealed nanostructures were just LDD preimplanted with boron atoms (1.10^{15}cm^{-2}). Moreover, the gates of the nanotransistors were covered by a SiN oxide, but not the source and drain. The objective of these tests was to determine if the nanostructures can survive to laser shots performed at IEF.

We realized in Orsay four series of laser shots with different conditions on four different samples with predefined nanostructures from the LETI, called SUNI1. The conditions are summarized in Tab.3.2. The laser annealing was realized with a different number of laser shots, and was done after a HF cleaning or without one. HF is used here to remove native silicon dioxide from wafers.

SUNI1-1	SUNI1-2	SUNI1-3	SUNI1-4
HF	HF	HF	no HF
1-3 laser shots	100 laser shots	0 laser shot	1-3 laser shots

Table 3.2: Laser annealing tests on SUNI1 samples with different conditions.

SEM observation followed the laser annealing of these nanostructures, in order to observe if they were damaged. For the nanostructures annealed of the samples SUNI1-1 and SUNI1-2, they are severely damaged, even more for the smallest structures. The surprising fact is that there is no significant difference between the SEM images of the nanostructures annealed of these two samples. We can also assume that the first laser shots are determinant.

SUNI1-3 and SUNI1-4 samples show non deteriorated nanostructures when observing with SEM. Although this result is obvious for SUNI1-3 as no laser shot has been sent, it is rather surprising for the SUNI1-4 sample. On the latter, HF cleaning was not performed before the laser annealing. Consequently, we can suppose that native oxide could protect the silicon from damages during the annealing.

Here we present in Fig.3.26 SEM images of two MOSFETs of the sample SUNI1-1, before and after the laser annealing executing in Orsay. As a result, while the smaller structure on the left of Fig.3.26 has been badly damaged by the laser annealing, the interesting point to observe is that the larger structure on the right of Fig.3.26 has been entirely preserved. We can reasonably attribute these different behaviors to the different sizes of the predefined structures.

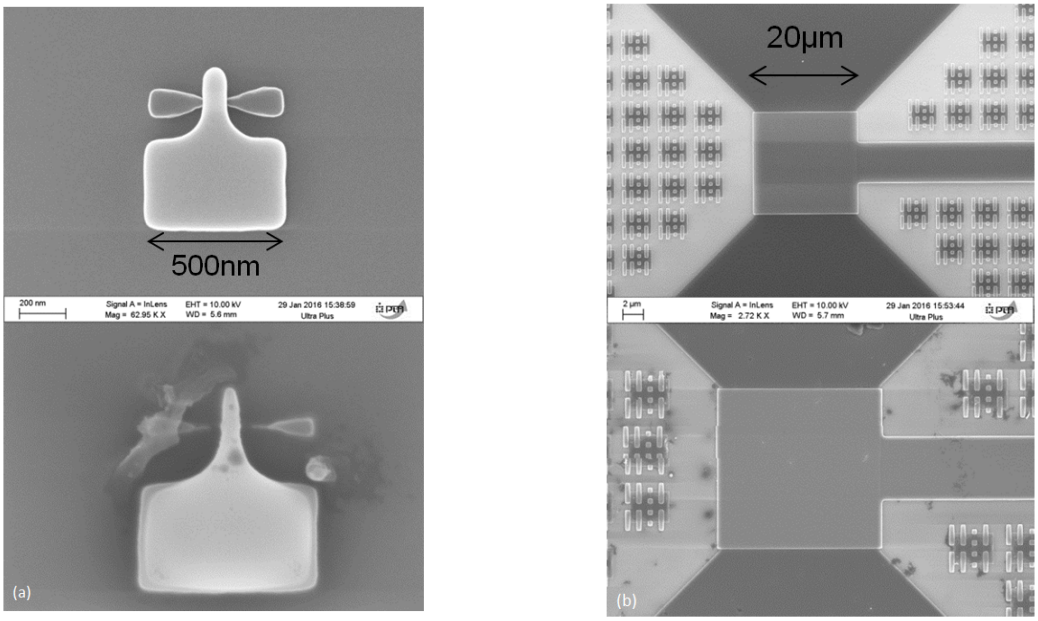


Figure 3.26: SEM images of two boron preimplanted MOSFETs before and after laser annealing.

However, even if transistors of micrometric size seem to survive to laser shots, it is also necessary to check if the recrystallisation was achieved and the dopants are activated. The simple way to realize this operation is to perform electrical tests at room temperature, in order to register any field effect.

Before the realization of electrical tests, the SiN oxide present on all the gates of transistors had to be removed by a wet-etching with phosphoric acid (H_3PO_4) in cleanroom. In order to isolate the gates of transistors and also protect the rest of the structures (mainly the spacers made of SiN), a high precise electron-beam lithography was made, taking the advantage that H_3PO_4 will not destroy the remaining PMMA resin during the etching. Unfortunately, according to thickness measurements realized at the Dektak profilometer in cleanroom, wet-etching appears to be not sufficient to remove entirely the SiN on top of the gates. The profilometer is an instrument used to measure the vertical profile of samples and thin film thickness. We consequently decided to try another option with an etching made with the Oxford installation. And this time, two characterisation methods, both profilometer and SEM/EDX acquisitions confirmed the entire removal of the oxide.

Afterwards, I have tested electrically the structures already contacted, as shown for example on the right of Fig.3.26. Despite the care brought to the SiN layer removal, electrical tests were not successful. In fact, no field effect was measured, we registered either gate leakage current or no current at all flowing through the transistors.

We can assume different reasons to explain the result. Firstly, even if the larger transistors seem to have suffered from no major degradation, it is possible that the gates could have been weakened, leading to the leakage currents. On the other hand, obtaining no current flowing through several transistors could demonstrate that the annealing has not properly worked. Finally, we could also think that some of the nanotransistors were already broken before the step of laser annealing.

Conclusion

We made laser annealing tests on several preimplanted nanostructures. The two important points to keep in mind in that despite the severe damages induced by laser annealing seen on SEM images, larger micrometric devices survived to the laser shots. Moreover, the SiN oxide seems to have a crucial role here, because it protects the silicon layer below during the annealing. Hence, it would be highly interesting to perform other laser annealing tests on preimplanted non-annealed devices covered by SiN (and not only on the gates).

In any case, we need to continue to explore laser annealing on LETI nanodevices, in order to find the well-adapted power conditions, especially for the first laser shots, to ensure the non-degradation of the devices. We probably will have to use weaker power for the laser shots.

We now want to focus on realizing superconducting SOI:B with PLIE technique. It seems to be the most adapted method because a very few number of laser shots are necessary to activate the dopants and recrystallise the Si layer. Even if the first laser shots sent are determinant for the devices, we can reasonably think that the nanostructures still have greater chance to survive if they experiment less laser shots.

3.2.3 Superconducting SOI:B with PLIE

We want now to examine superconductivity of SOI:B samples with the second laser doping technique PLIE. As mentioned before, due to the initial boron preimplantation and to the very small number of laser shots needed for the recrystallisation, PLIE appears as the best candidate to make superconducting SOI, if we want to integrate the latter in a transitor-like nanostructure.

We first fabricated PLIE boron-doped SOI with the LETI. All the PLIE samples are presented with their characteristics in Tab.3.3.

We started from two 23nm thick SOI wafers from the LETI, already preimplanted with a boron dose of 1.10^{15}cm^{-2}. We chose the thickness of 23nm for the top silicon layer of SOI since it is the basic thickness used at LETI. These SOI wafers have been then preimplanted at the LETI, with a dose of $2.5.10^{16}$cm^{-2} for the first one named Slot22 and with a dose of 5.10^{16}cm^{-2} for the second named Slot23. The choice for these two preimplanted doses refers to the results obtained by Audrey Grockowiak during her thesis. She actually managed to obtain superconducting bulk Si:B with PLIE with those preimplantation doses. The doping realized here is made only with boron atoms. The implantation energy of 2keV has been chosen rather weak because of the thin thickness of the top silicon layer of SOI.

In our study, we also chose to add two other SOI wafers from the LETI, but with a different silicon top layer thickness. Considering the major difficulty to dope 23nm thick SOI without touching the BOX, we decided to slightly increase the thickness of SOI to 33nm. These two 33nm thick SOI wafers have been afterwards preimplanted at the LETI. Slot24 is associated with the boron dose of $2.5.10^{16}$cm^{-2}, while a dose of 5.10^{16}cm^{-2} was preimplanted in Slot25. For this larger thickness of top silicon, the implantation energy can be also increased to 3keV.

Finally, we performed PLIE doping on three bulk silicon wafers, initially preimplanted at the same dose of 1.10^{15}cm^{-2}. In the following, the bulk silicon wafers are named Slot1, Slot2 and Slot3 and the boron doses preimplanted are similar to those associated to the other samples : either $2.5.10^{16}$cm^{-2} or 5.10^{16}cm^{-2}. This will allow us recovering the previous results of Audrey Grockowiak on PLIE bulk Si:B samples or maybe revealing unexpected different behaviors.

During the PLIE laser annealing, one, two or five laser shots have been sent on different sites of the wafers, with different energy densities. A sketch of the PLIE process on a SOI wafer is presented in Fig.3.27.

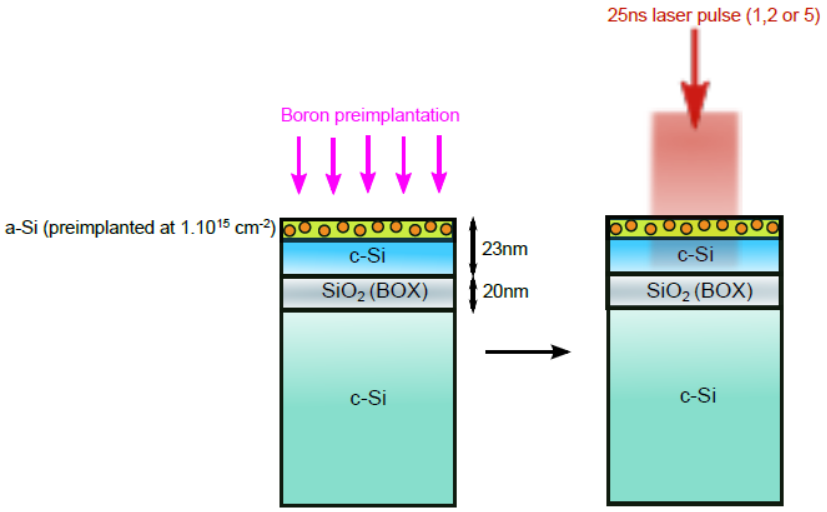


Figure 3.27: Sketch of PLIE doping on SOI wafer (LotID: T16S0926).

Slot number	Material	Dopant	Preimplanted dose (cm^{-2})	Implantation energy (keV)
1	Bulk Si	B+	$2.5.10^{16}$	3
2	Bulk Si	B+	$2.5.10^{16}$	4
3	Bulk Si	B+	5.10^{16}	4
22	SOI 23nm	B+	$2.5.10^{16}$	2
23	SOI 23nm	B+	5.10^{16}	2
24	SOI 33nm	B+	$2.5.10^{16}$	3
25	SOI 33nm	B+	5.10^{16}	3

Table 3.3: PLIE samples.

The laser annealing has been done at the LASSE company. The laser used operates at 308nm, the laser shots are 160ns long and cover an area of $18 \times 18mm^2$ each. This is much larger than in Orsay, where areas of $2 \times 2mm^2$ are annealed. These areas are called sites in the following of the thesis. The mapping of the sites distribution on a full sheet 300mm SOI wafer is represented in Fig.3.28.

The mapping can be explained as follows. From the site 1 to 45, one single pulse has been performed. Then, multi pulse has been experimented. Two laser pulses have been sent to the site 46 to 58. And finally, from the site 59 to 71, five laser shots have been realized. The energy density increases for each new annealed site.

The other half of the presented SOI wafer was not used in a first place; it was later sent to Orsay, in order to realize the same kind of laser annealing with the same number of laser shots. The main idea is actually to compare the samples annealed at Orsay and at LASSE. In fact, the different conditions used by Orsay and LASSE could generate samples of various qualities and properties. The two main differences between the two

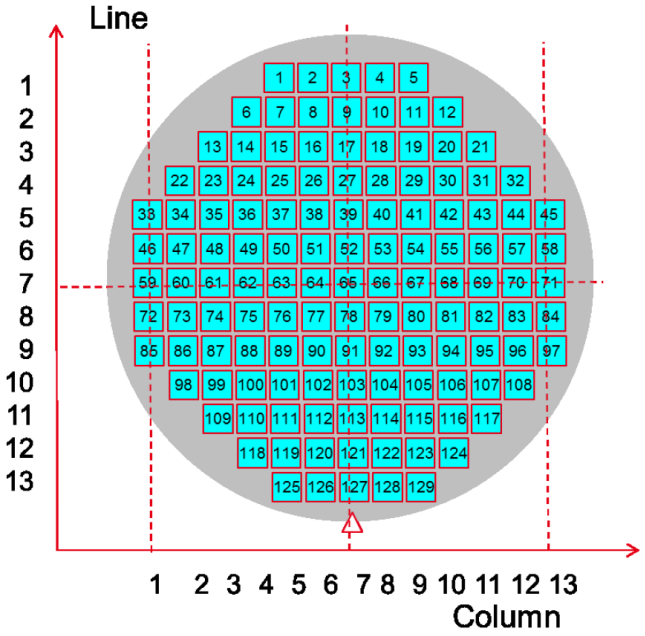


Figure 3.28: Mapping showing the sites distribution on a SOI wafer realized at LASSE. Each site of $18 \times 18\text{mm}^2$ corresponds to one laser annealing at one laser energy and for a specific number of laser pulses.

institutes are related to the high vacuum chamber and the duration of the laser pulse. In fact, as mentioned before, in Orsay, a high vacuum chamber protects the samples for any contamination and the laser shot duration is extremly short, equals to 25ns. On the other hand, LASSE uses no high vacuum chamber but a N_2 atmosphere during the doping process and the laser shot duration is really longer, this is actually 160ns. Importantly, we want to check if these two experimental parameters could have a determinant role to play in SOI:B superconductivity.

Experimental results on 23nm SOI:B (Slot22 and 23)

After laser annealing, the first experimental observations have been made using an optical microscope. Fig.3.29 shows several microscope images of different sites of the Slot22, which have been fabricated at different laser energies and also with a different number of laser shots: 1, 2 or 5.

For one laser pulse and for an energy density $E = 0.65\text{J/cm}^2$, a first surface color change is detected. On the microscope image, we can actually well distinguish the right edge of the annealed site which has received the laser pulse, from the initial surface. While increasing the energy density, the sites become progressively darker. Moreover, at $E = 0.99\text{J/cm}^2$, we notice an edge color change, it is darker than the middle part of the site. This change of color becomes even more stronger by increasing E. The exact same behaviour and color changes appear by observing different sites of the Slot23 at the microscope.

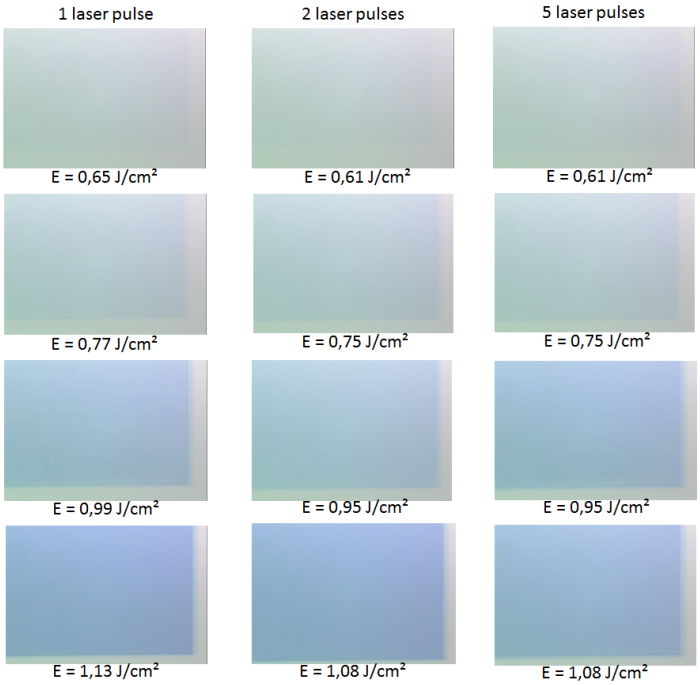


Figure 3.29: Optical microscope images of 12 sites of Slot22. These sites of PLIE SOI:B have been realized at different laser energy and with different number of laser shots.

In order to explain these color changes observed at the optical microscope, we measured the sheet resistance as a function of the energy density for all the single-pulse sites of the Slot22 and Slot23. The results can be observed in Fig.3.30.

As operated in Orsay, LASSE uses transient reflectivity in order to control the process of PLIE. As explained at the beginning of this chapter, a change in transient reflectivity indicates the Si melting start. We can see in Fig.3.30 that the energy density threshold associated to the silicon melting point which induces an abrupt variation of the transient reflectivity, is very similar to the one where a color change threshold has been noticed on a microscope image. Therefore, we can reasonably suppose that the color change threshold indicates the silicon melting.

Furthermore, for the Slot23, at higher energy densities close to $E = 1 J/cm^2$, we can observe a suddenly dramatic decrease of the sheet resistance, followed by an increase. This could be the potential sign that all the silicon is now melted, preventing a good recrystallisation.

Fig.3.31 allows to compare the sheet resistance as a function of the energy density for single-pulse sites (1-45) with multi-pulse ones (46-71). We can immediately note that the curves all have the same shape and that the sheet resistance behavior is identical for single and multi-pulses. However, to study it completely, it would have been interesting to continue the sheet resistance measurements for multi-pulses at higher energy densities.

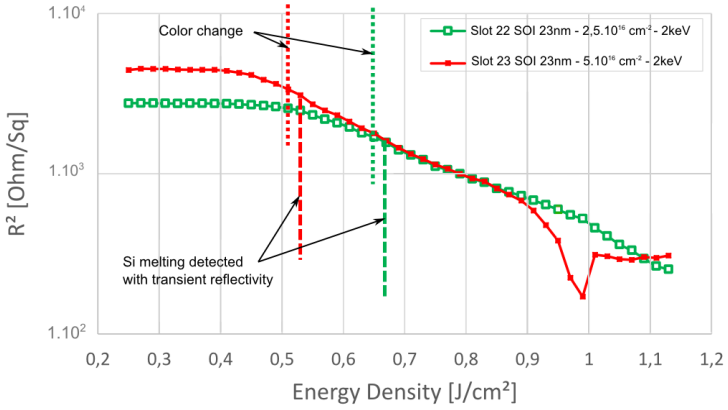


Figure 3.30: Sheet resistance from the site 1 to 45 as a function of the energy density (with one laser pulse). The energy density of the silicon melting start is really close to the energy density where a color change is seen. For Slot 22: $E = 0.68 J/cm^2$ and for Slot 23: $E = 0.53 J/cm^2$ (reflectivity)

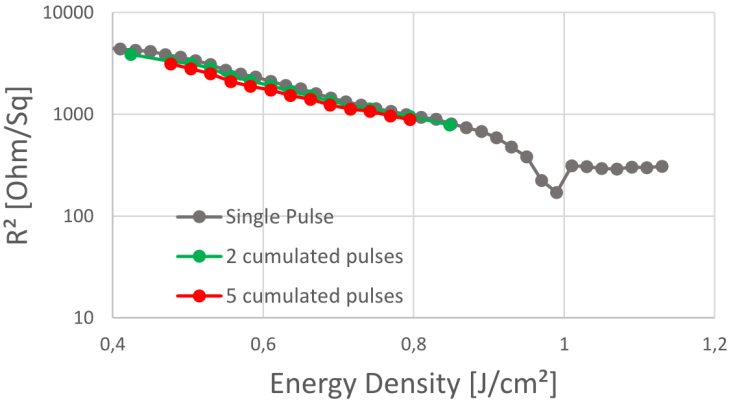


Figure 3.31: Sheet resistance evolution with the energy density for the Slot23, to compare single and multi-pulse.

After the first experimental results obtained at room temperature, electrical resistance measurements were realized at very low temperature using the Physical Properties Measurements System (PPMS). We firstly focused on low temperature measurements on PLIE SOI:B Slot22, which has a boron dose of $2.5.10^{16} cm^{-2}$.

I began with the sites 45 and 57 of the Slot22. The first one has received one laser shot, whereas two laser shots were sent on the site 57. The choice of these two sites refers to their associated high energy densities, giving the lowest sheet resistances, before the damage threshold where the BOX is reached by one or several laser pulses. We measured them with the PPMS, but only a metallic behavior was observed, without any sign of superconductivity.

Then, assuming that the energy densities associated to the two first sites were too high, we were interested in considering sites with lower density energies. All in all, I measured the sites 22, 30, 34 and 47 at very low temperature; however, as in the previous case, no superconductivity was detected.

I present all the properties associated to the studied Slot22 sites in Tab.3.4, that is to say the number of laser shots, the sheet resistance R and the energy density E.

Site number of Slot22	Number of laser shots	R (Ω)	E (J/cm^2)	Superconductivity
45	1	253.1	1.13	no
57	2	392.8	1.02	no
22	1	1602	0.67	no
30	1	808.5	0.85	no
34	1	639	0.93	no
47	2	1911.4	0.61	no

Table 3.4: PLIE Slot22 samples

In order to complete the electrical resistance measurements performed at low temperature with the PPMS and offer a better understanding of these results, high-resolution X-ray diffraction (XRD) analysis of all these sites from the Slot22 was realized around the (004) Bragg reflection at room temperature in CEA, in collaboration with Stéphane Lequien. XRD measurements could also allow us extracting the real thickness of the doped silicon layer. In fact, we can only assume now that this thickness has to be lower than 23nm, otherwise the BOX is touched and the entire structure of SOI is damaged.

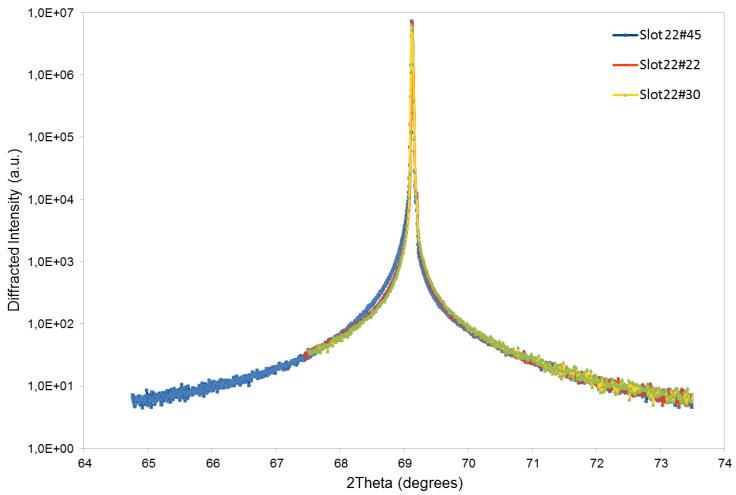


Figure 3.32: XRD measurements of the sites 45, 22 and 30 of the Slot 22, around the (004) Bragg reflection. The Bragg angle associated to the only one diffraction peak corresponding to the silicon substrate is $\theta = 34.575°$.

For all the sites of the Slot22, the results obtained indicate the same behavior. As presented in Fig.3.32, we can clearly see one diffraction peak appearing at the Bragg angle $2\theta = 69{,}15°$, corresponding to the Si substrate. Nevertheless, we also note the absence of a diffraction peak corresponding to a Si:B layer on top of the SOI substrate. This reveals that no Si:B layer with a single crystal character has been formed during the PLIE process.

Conclusion

Unfortunately, our first PLIE SOI:B samples were not superconducting at very low temperature. High-resolution X-ray diffraction has confirmed the absence of a Si:B crystalline layer on top of the SOI substrate. Before extending the work dedicated on SOI:B samples obtained with PLIE, we have focused on PLIE bulk Si:B, since superconductivity has already been measured in bulk silicon doped with PLIE before my thesis work.

Experimental results on PLIE Si:B (Slot1)

We now consider the wafer named Slot1 which corresponds to bulk silicon preimplanted with boron at $2.5.10^{16}\text{cm}^{-2}$ and annealed with PLIE as explained above.

As preliminary experiments, we performed also optical microscope observation and electrical sheet resistance measurement as a function of the energy density at room temperature. It is the first step allowing us finding the good laser conditions to melt the silicon.

At first, I chose to work on the sites 44 and 56 of the Slot1, with low sheet resistances of the order of tens of Ω. The high energy densities associated are respectively 1.96J/cm^2 and 1.938J/cm^2. Moreover, the site 44 has been performed with a single laser pulse during PLIE, while the site 56 has received two laser shots. These two sites are metallic at very low temperature.

Due to the same reasons as explained above, we chose also to work on the site 2 of the Slot1 with a weaker energy density of 1.1J/cm^2, and with a sheet resistance equals to 153Ω. Finally, the low-temperature measurements gave the same result, no superconductivity has been observed.

The measured sites and their principal characteristics are presented in Tab.3.5.

Site number of Slot1	Number of laser shots	R (Ω)	E (J/cm^2)	Superconductivity
2	1	153	1.1	no
44	1	13.5	1.96	no
56	2	20	1.938	no

Table 3.5: PLIE Slot1 samples

Afterwards, XRD analysis was performed of these three samples. Interestingly, the sites 44 and 56 reveal a different behavior from the site 2 of the Slot1. As shown in Fig.3.33 corresponding to the diffractogram of the site 56, we can see the expected diffraction peak of

the silicon substrate for the Bragg angle $2\theta = 69.15°$, but also two other diffraction peaks separated from the first one, appearing for the following Bragg angles $2\theta = 70.87°$ and $71.72°$. The XRD results let us assume that these two broad diffraction peaks would correspond to two different Si:B layers with different boron concentrations. However, one can not extract the thickness of these Si:B layers, because no interference fringes are observed.

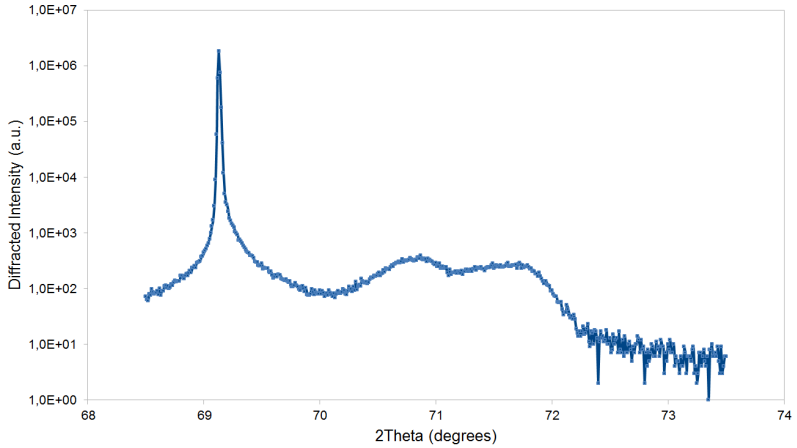


Figure 3.33: XRD measurements of the site 56 of the Slot 1, around the (004) Bragg reflection.

The XRD results performed on the site 2 of the Slot1 are depicted in Fig.3.34. In comparison to the two previous samples, we only observe one diffraction peak assigned to the silicon substrate. This supports the absence of a single crystalline Si:B layer on this sample.

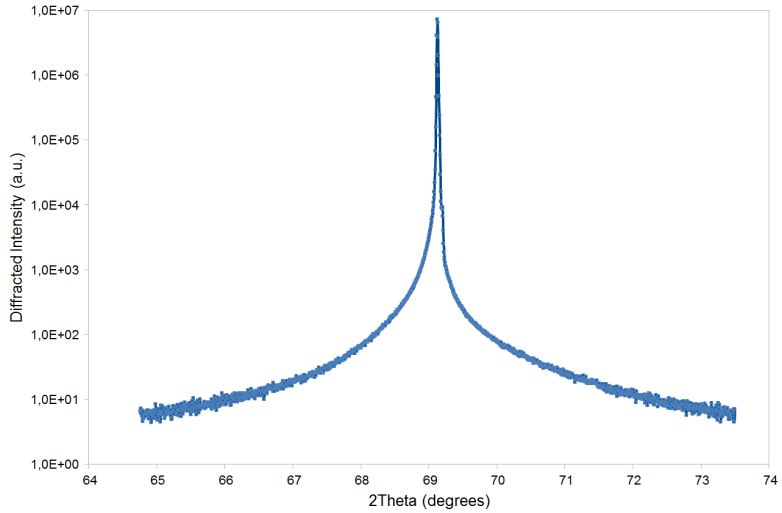


Figure 3.34: XRD measurements of the site 2 of the Slot 1, around the (004) Bragg reflection.

The X-ray measurements of these three Si:B samples obtained with PLIE are in very good agreement with the low temperature resistance results realized with the PPMS. These results are not consistent with the ones obtained by Audrey Grockowiak during her thesis work. As mentioned before, her PLIE Si:B samples were superconducting at very low temperature. Furthermore, when she measured them with XRD, we could notice two separated sharp peaks: one corresponding to the silicon substrate and the other one to the top Si:B layer.

Conclusion

Unfortunately, we did not manage to fabricate superconducting boron-doped bulk silicon and boron-doped SOI with PLIE technique, using the laser annealing facility of the LASSE company. Considering the difficulty of the demanding task, the fact that we obtained no superconducting PLIE Si:B and SOI:B samples at LASSE is not totally surprising. However, it is also not prohibitive, as the laser energies targeting at LASSE was not optimal. This work would have to be extended to become successful.

Before the start of my thesis, Audrey Grockowiak observed superconductivity on highly boron-doped bulk silicon obtained with PLIE and operated at IEF. Therefore, it is likely that the different process conditions between IEF and LASSE play a determinant role in the fabricated samples superconductivity. For this reason, the other halves of all the bulk silicon and SOI wafers have been sent to IEF, in order to realize PLIE and obtain superconductivity.

Experimental results with PLIE samples realized at IEF, Orsay

PLIE Si:B (Slot1)

We started with the Slot1, corresponding to the bulk silicon wafer preimplanted with a boron dose of $2.5.10^{16}$cm^{-2}. The laser annealing was this time executed in IEF; we fabricated several highly boron-doped bulk silicon samples with different number of laser shots and various energy densities. The main goal was to recover the results obtained by Audrey Grockowiak on PLIE Si:B superconductivity.

All the samples measured at very low temperature with the PPMS are presented with their characteristics in Tab.3.6, they are all superconducting. Fig.3.35 shows the complete superconducting transitions of the Si:B samples.

Sample name	Laser shots	E (mJ/cm^2)	R_{4K} (Ω)	Superconductivity	T_c (K)
20170511-1	5	600	16.3	yes	0.2
20170511-2	2	680	7.08	yes	0.37
20170511-3	5	680	21.9	yes	0.22
20170511-4	2	760	6.9	yes	0.36
20170511-5	5	760	25.5	yes	0.22

Table 3.6: PLIE Si:B samples (Slot1, IEF)

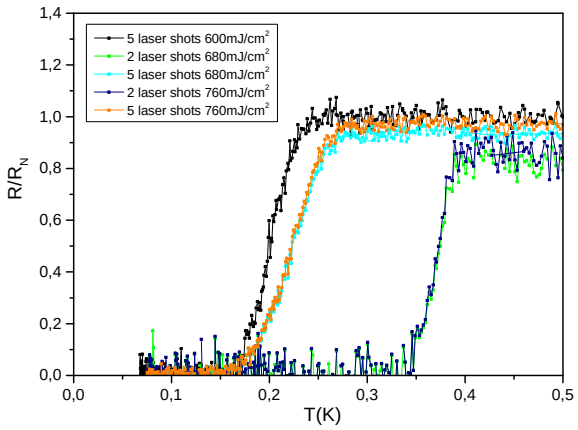


Figure 3.35: Evolution of the resistance normalized by normal resistance with respect to the temperature for five Si:B samples obtained at different energy densites and for different number of laser shots. The superconducting transitions are all complete. The correlation between the sample resistance and the critical temperature is clear: the annealed Si:B samples having the lowest disorder, that is to say the weakest resistances, exhibit the highest critical temperatures, up to 0.37K.

From these measurements, we would expect that an increased number of laser shots would decrease the resistance of the sample. Moreover, the overall resistance should decrease with a higher energy density, because the thickness of the melted silicon layer would become larger. However, from these results, we cannot extract any correlation between the sample resistance and the energy density associated to the doped Si thickness.

Nevertheless, the correlation between the resistance and the critical temperature seems to be more robust. We observe that the Si:B samples with the higher critical temperatures, here up to 0.37K, have also the lowest resistances. Higher resistances seem to be the signature of an increased disorder in the Si:B layers. During her thesis, Audrey Grockowiak obtained superconducting PLIE Si:B samples with associated critical temperatures of the order of 200mK. She assumed that the T_c of PLIE samples was only dependent on the initial preimplanted boron dose. It seems that the present results weaken this assumption, since for two Si:B samples, we measured higher critical temperatures. A careful and intensive study will be needed before it is possible to conclude.

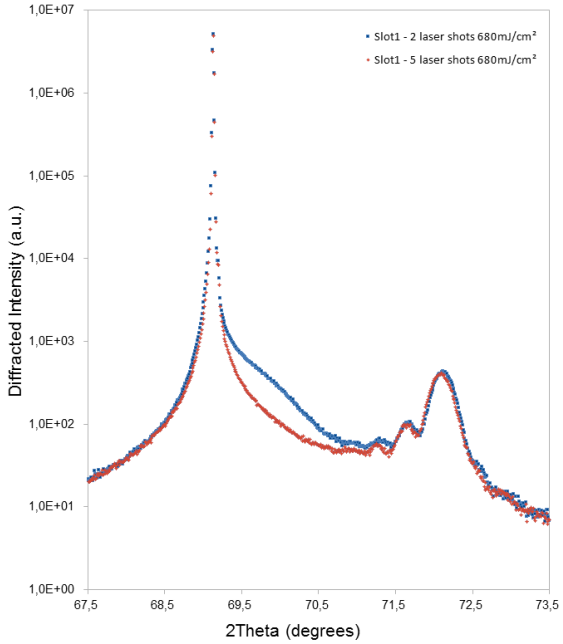


Figure 3.36: XRD measurements realized on two superconducting Si:B samples fabricated at the same energy density of 680mJ/cm^2, and with either two or five laser shots. The first diffraction peak appearing at the Bragg angle $2\theta = 69.1°$, corresponds to the silicon substrate, for each sample. The second peak at the higher angle $2\theta = 72.2°$ reveals the presence of a crystalline Si:B layer in each sample.

After low temperature measurements, XRD was also performed on two superconducting Si:B samples (see Fig.3.36). The bulk silicon substrate peak is observed at $2\theta = 69.1°$, for each measured sample. We also notice an additional diffraction peak at $2\theta = 72.2°$, corresponding to the Si:B layer. It confirms that the PLIE fabricated Si:B layer is crystalline. Moreover, it shows that the laser annealing was performed successfully and that

the recrystallisation was fast enough, without introducing too many defects or permitting a too large boron diffusion in the silicon.

These two samples were annealed with either two or five laser shots, and XRD analysis has shown that the Si:B layers were crystalline. In future XRD measurements, it would be interesting to consider a Si:B layer annealed with only one laser shot and check if the latter is sufficient to make the layer crystalline.

We have managed to fabricate superconducting highly boron-doped bulk silicon with the PLIE technique at IEF. Both very low temperature measurements and XRD analysis reveal the presence of a superconducting crystalline Si:B layer on top of the silicon substrates. It shows that the experimental conditions during the initial preimplantation and the laser annealing are well-controlled and reproducible. However, as the correlations between the different parameters are not always well-understood, an extended study on superconducting Si:B samples will have to be realized. The next step is to fabricate superconducting SOI:B samples with the PLIE technique.

PLIE 33nm SOI:B (Slot24)

We consider now the Slot24, corresponding to the 33nm thick SOI wafer preimplanted with a boron dose of $2.5.10^{16}\text{cm}^{-2}$. The PLIE laser annealing was performed with either one, two or five laser pulses, for different energy densities. For all the fabricated SOI:B samples, the sheet resistance as a function of the energy density is plotted in Fig.3.37.

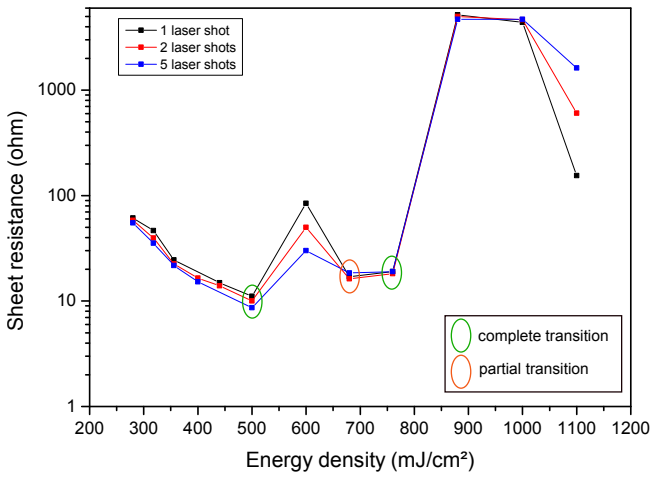


Figure 3.37: Sheet resistance of SOI:B samples from the Slot24 with respect to the energy density, for either 1, 2 or 5 laser shots.

For low energy densities, between 250 and 500mJ/cm^2, we observe a decrease of the sheet resistance of the measured samples when the energy density increases. In this range

of energy density, we also notice that an increased number of laser shots contributes to slightly reduce the resistance. This behavior is in good agreement with our expectations. Then, for energy densities higher than 500mJ/cm^2, appears an area with a sudden rise of the sheet resistance. This dispersion in the resistance underlines the rise of disorder in the Si:B layer of the SOI samples. The appearance of increased disorder is confirmed by the noticeable unhomogeneous aspect of the fabricated SOI:B samples. Finally, the energy threshold at 880mJ/cm^2, supported by an abrupt increase in resistance, is reached, meaning that the BOX has been touched.

All of the annealed samples which have been measured at very low temperature are summarized in Tab.3.7.

Sample name	Laser shots	E (mJ/cm^2)	R_{300K} (Ω)	R_{4K} (Ω)	Superconductivity	T_c (K)
33nm20170515-1	2	356	48.9	44.5	no	/
33nm20170515-2	2	400	27	24.08	no	/
33nm20170515-3	2	440	24.8	21.32	no	/
33nm20170515-4a	1	500	22.09	18.57	yes	0.23
33nm20170515-4b	2	500	15.39	13.06	yes	0.2
33nm20170515-4c	5	500	15.09	12.13	yes	0.2
33nm20170515-5	2	600	252	318	no	/
33nm20170515-6a	1	680	39.2	36.8	partial transition	/
33nm20170515-6b	2	680	33.15	30.8	no	/
33nm20170515-6c	5	680	40.3	38.8	partial transition	/
33nm20170515-7a	1	760	27	24.08	multiple transition	/
33nm20170515-7b	2	760	27.1	24.2	muliple transition	/
33nm20170515-7c	5	760	48.9	44.5	multiple transition	/
33nm20170515-8	2	880	774	/	no	/

Table 3.7: PLIE 33nm SOI:B samples (Slot24, IEF)

The resistance with respect to the temperature for a series of eight SOI:B samples annealed with two laser shots and for different energy densities, is shown in Fig.3.38(top, left). One complete superconducting transition is to be noticed for the SOI:B sample annealed at the energy density of 500mJ/cm^2. At the same energy density but with a different number of laser shots (one and five), we also measure complete superconducting transitions, see Fig.3.38(top, right). The critical temperatures of these SOI:B samples are of the order of 200mK. Once again, it seems that the correlation between the resistance and the critical temperature is robust. In fact, the three superconducting SOI:B samples annealed at the same energy density of 500mJ/cm^2 have the lowest measured resistances, ensuring less disorder.

Furthermore, we also register sign of superconductivity in other SOI:B samples. For instance, at 680mJ/cm^2, we observe partial superconducting transitions (Fig.3.38(bottom, left)). Additionnally, multiple superconducting transitions are obtained for SOI:B samples

fabricated at 760mJ/cm^2, as presented in Fig.3.38(bottom, right). The other samples show metallic behaviors.

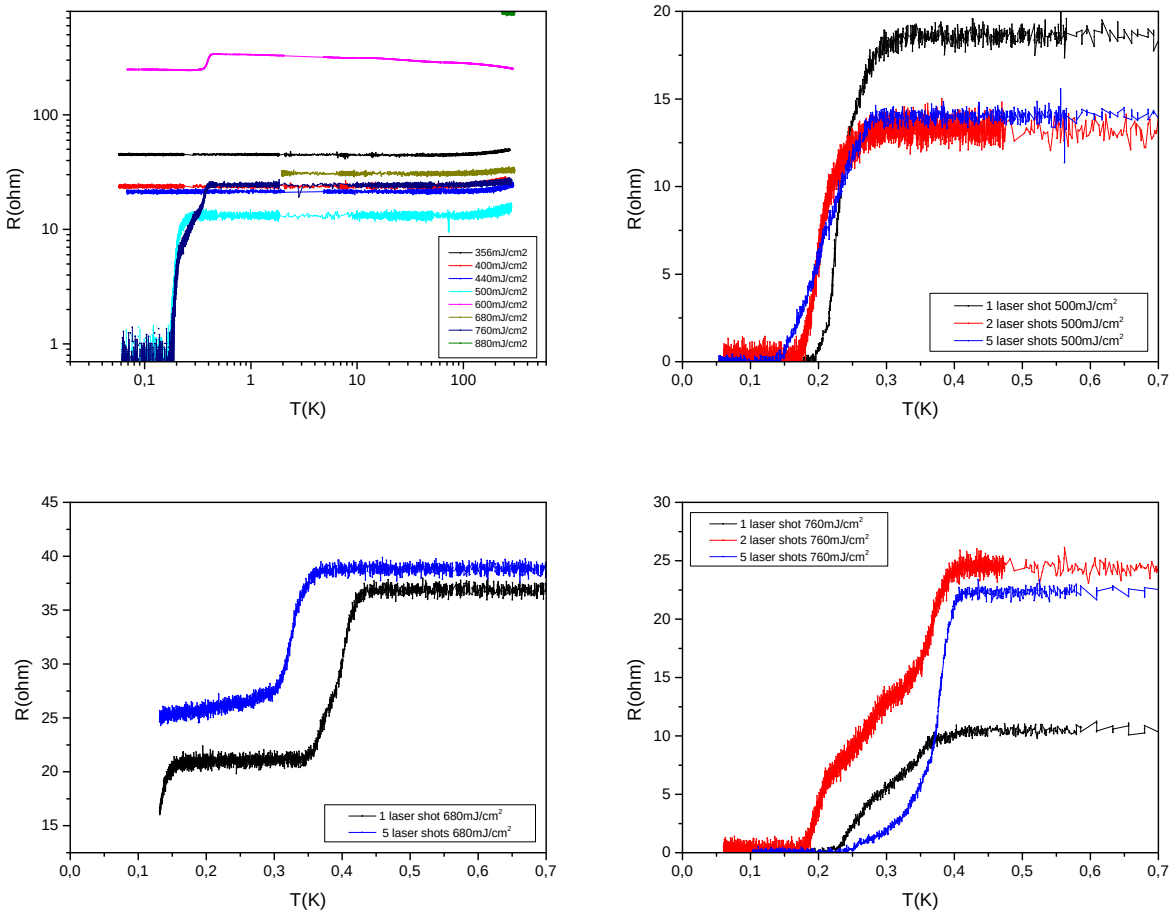


Figure 3.38: (Top, left) Resistance as a function of the temperature for eight SOI:B samples annealed with two laser shots and for different energy densities. One superconducting transition is complete (500mJ/cm^2). (Top, right) Complete superconducting transitions for SOI:B samples annealed at 500mJ/cm^2, for 1, 2 or 5 laser shots. (Bottom, left) Partial superconducting transitions for SOI:B samples annealed at 680mJ/cm^2, for 1, 2 or 5 laser shots. (Bottom, right) Multiple superconducting transitions for SOI:B samples annealed at 760mJ/cm^2, for 1, 2 or 5 laser shots.

We have then performed XRD measurements on two different SOI:B samples, one showing a complete superconducting transition (500mJ/cm^2) and the other exhibiting a metallic behavior (440mJ/cm^2). Both SOI:B samples have been annealed with two laser shots. The goal was to test if the XRD analysis could reveal a distinction between these two SOI:B samples, having a different electrical transport behavior. The two diffractograms I(2θ) are displayed in Fig.3.39. In fact, we observe a clear difference in the X-ray diffraction scans,

which could explain the resistance measurements. The silicon substrate peak appears for both SOI:B samples, as expected. However, the superconducting SOI:B sample presents an additionnal diffraction peak around the angle of $2\theta = 72°$, while no peak is to be noticed for the metallic SOI:B sample. The presence of this additionnal peak for the superconducting SOI:B sample means that a crystalline Si:B layer has been fabricated on top of the SOI substrate. It seems that the XRD measurements are in very good agreement with the low temperature results.

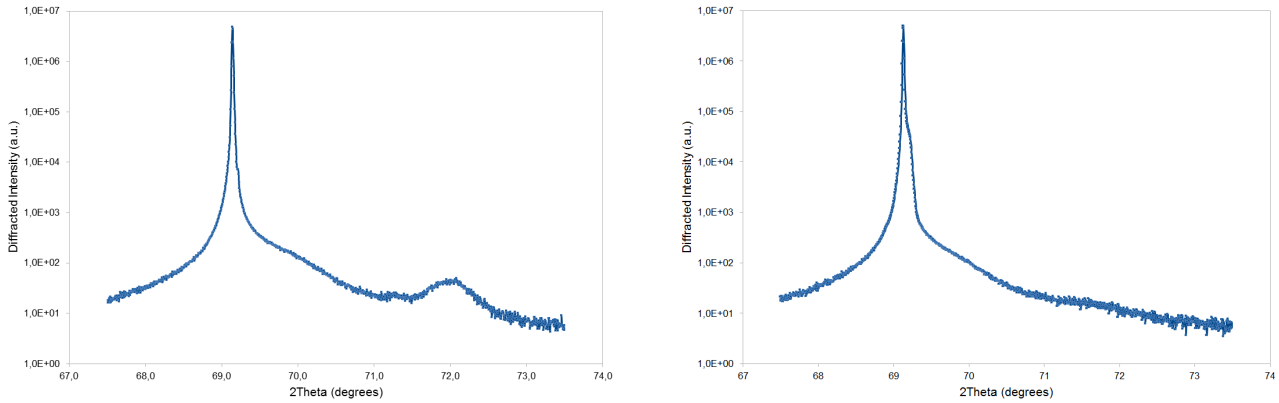


Figure 3.39: (Left) XRD measurements showing a diffraction peak around $2\theta = 72°$ for the SOI:B sample annealed at 500mJ/cm^2, corresponding to the crystalline Si:B layer on top of the SOI substrate. (Right) No peak corresponding to a Si:B layer has been measured for the SOI:B sample annealed at 440mJ/cm^2.

For the first time, we have fabricated superconducting SOI:B samples with the PLIE technique at the IEF. This is one major result of this thesis work. This reveals that the preimplantation of dopants is well-controlled and that the laser expertise permitting to send laser shots at the surface of a SOI sample without touching the BOX is achieved. We have now to determine if superconductivity can be obtained in 23nm thick SOI:B, this thickness is actually the one standard at the LETI.

PLIE 23nm SOI:B (Slot22)

We focus now on 23nm thick SOI:B samples from the Slot22, preimplanted with a boron dose of $2.5.10^{16}$cm^{-2}, and annealed with PLIE technique with either 1, 2 or 5 laser pulses.

The overall aspect of the graph presenting the sheet resistances of the fabricated SOI:B samples as a function of the energy density is the same than in the previous case of 33nm thick SOI:B from Slot24 (see Fig.3.40).

All of the SOI:B samples measured at very low temperature are presented with their characteristics in Tab.3.8. The resistance normalized by the normal resistance as a function of the temperature is presented in Fig.3.41. We observed one partial superconducting transition for a SOI:B sample annealed at 440mJ/cm^2, with two laser shots. The other SOI:B samples are clearly metallic.

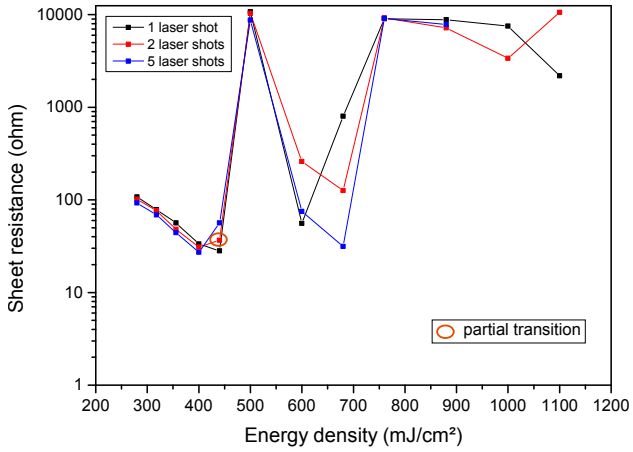


Figure 3.40: Sheet resistance with respect to the energy density for the 23nm SOI:B samples from the Slot22.

Sample name	Laser shots	Energy density (mJ/cm^2)	R_{4K} (Ω)	Superconductivity
23nm20170515-1	2	318	160.7	no
23nm20170515-2	2	356	109.7	no
23nm20170515-3	2	400	54.8	no
23nm20170515-4	2	440	31.7	partial transition

Table 3.8: PLIE 23nm SOI:B samples (Slot22, IEF)

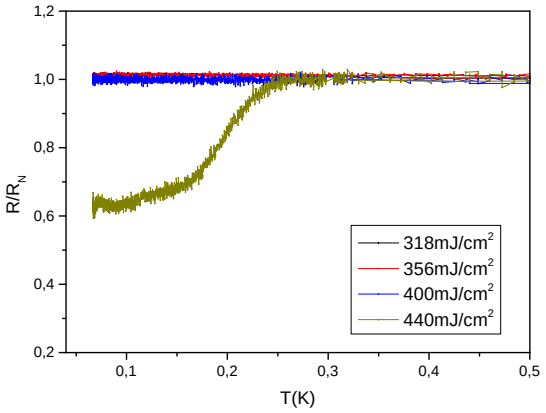


Figure 3.41: Resistance normalized by the normal resistance as a function of the temperature, showing one partial superconducting transition for a SOI:B sample annealed at the energy density of 440mJ/cm^2, with two laser shots. The other SOI:B samples are metallic.

The measurement of this first partial superconducting transition for a 23nm SOI:B sample is a very promising result. Thus, it would be highly interesting to extend this work by fabricating other 23nm SOI:B samples with the PLIE technique, with a laser annealing with energy densities in the range between 440 and 500mJ/cm^2. In fact, as we can observe in Fig.3.40, this corresponds precisely to the energy range where the sheet resistances are the lowest, providing the less disorder, and offering the best chances for superconductivity to emerge.

To conclude, we have successfully fabricated superconducting Si:B and SOI:B samples with the PLIE technique, at IEF. Due to a highly-controlled laser expertise, we are now able to perform superconducting SOI:B layers with both doping techniques, GILD and PLIE at IEF. We can deduce that the experimental conditions operated at IEF, more precisely concerning the high-vaccum chamber and the short duration of the laser pulse, are determinant to obtain superconductivity.

After this breakthrough, the idea would be to take advantage of the superconductivity of SOI:B and thus introduce it in nanodevices, such as MOSFETs. Before trying to inject SOI:B in transistor-like devices which would be a highly difficult task, we have first decided to fabricate two simple superconducting SOI:B devices: a SQUID and a Hall bar.

3.2.4 First SOI:B devices

3.2.4.1 SQUID and Hall bar

Starting from a single superconducting SOI:B layer obtained with GILD technique using 200 laser shots (final boron dose of $2.5.10^{16}$cm^{-2}), we have fabricated a SOI:B Hall bar and two SOI:B SQUIDs. The Ti/Au contacts are already present on the SOI:B layer since they were realized as a first step in order to perform electrical transport measurements at very low temperature. Taking into account the location of these contacts, the realignment of the pattern composed of the Hall bar and the SQUIDs during the nanolithography process, was made in a second step. The drawing of the pattern with all the notified dimensions is presented in Fig.3.42.

The different steps of the realization of the devices are summarized here.
1) Electron beam lithography to define the shapes of the wanted global device, that is to say the SQUIDs and the Hall bar.
2) 20nm Al hard mask lift off to protect the top Si:B layer on the SOI substrate.
3) Etching of unprotected Si:B by RIE.
4) Al hard mask wet etching.

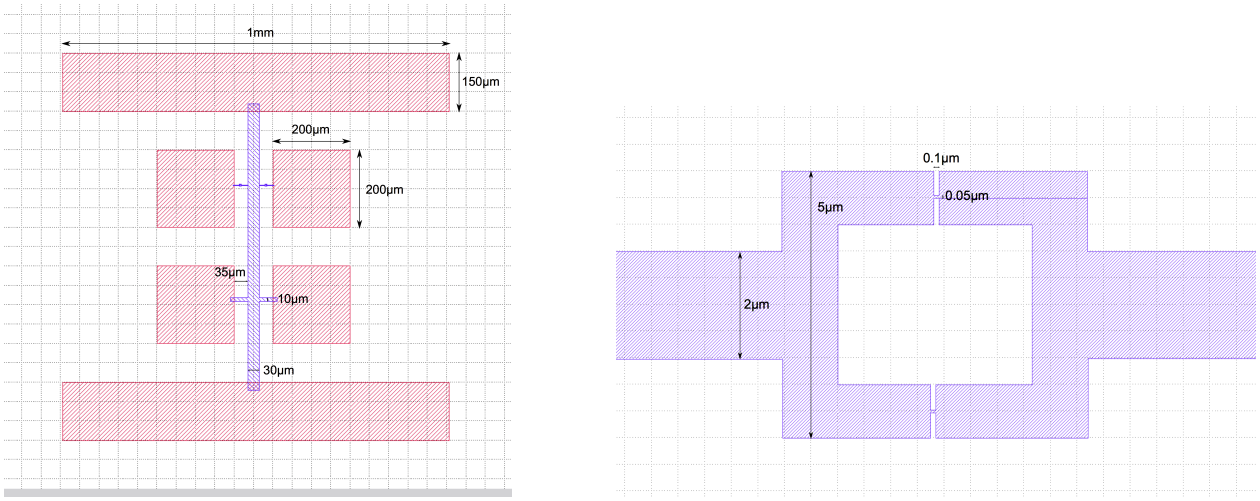


Figure 3.42: (Left) Drawing of the pattern containing the SQUIDs and the Hall bar, realized with KLayout. (Right) Drawing of one of the two identical SQUIDs.

Microscope and SEM images of the global device taken during the fabrication process are depicted in Fig.3.43. The sample has then been measured at very low temperature using a dilution cryostat. The expected critical temperature for this SOI:B device is of the order of 120mK.

At very low temperature, unfortunately, the SQUID on the left position of the central bar was broken; so we decided to focus on the measurements of the central bar and the right SQUID. The first results show that both geometries of central bar and SQUID are not

perfectly superconducting. The resistance as a function of the temperature is presented in Fig.3.44, for each geometry. We can clearly see two uncomplete superconducting transitions. Moreover, we observe multiple transitions for these two geometries, which means that the overall structure does not show a single transition at the same temperature. For instance, in the SQUID geometry, because of their small sizes, it is likely that the two weak links exhibit a transition before the rest of the SQUID loop.

In any case, this result is quite surprising since the initial SOI:B layer without any fabricated device was superconducting. However, we can assume here that the different steps needed for the fabrication of both Hall bar and SQUIDs have probably deteriorated the quality of the SOI:B layer, and thus would explain this result. Moreover, I also want to point out that these measurements at very low temperature are extremly sensible to external noise; it was necessary to add a large number of filters in serie to eliminate the maximum of noise that we could.

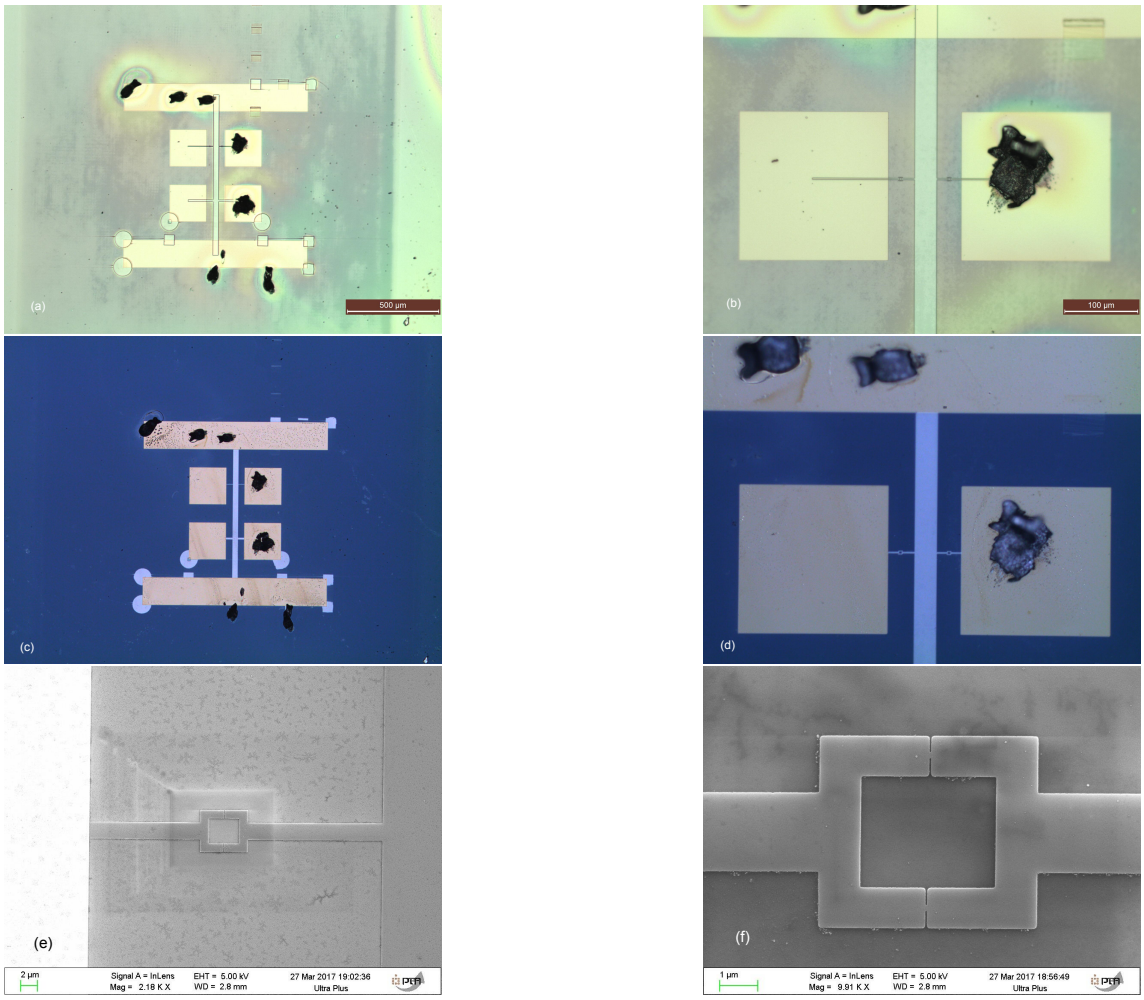


Figure 3.43: Microscope images of the device during the process: (a-b) After lift-off. (c-d) After wet etching. SEM images at the end of the process: (e-f) SOI:B SQUID.

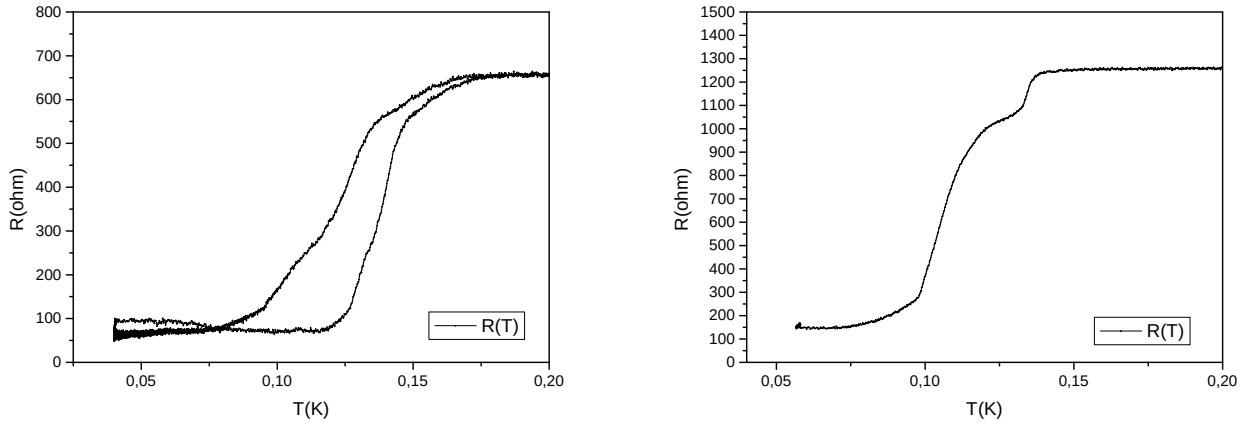


Figure 3.44: (Left) Uncomplete superconducting transition for the central bar geometry. (Right) Uncomplete and multiple superconducting transition for the SQUID geometry.

Even if the realized structures were not totally superconducting, I-V characteristics obtained at 50mK were realized, see Fig.3.45. Nevertheless, we cannot extract a precise critical current from these graphs.

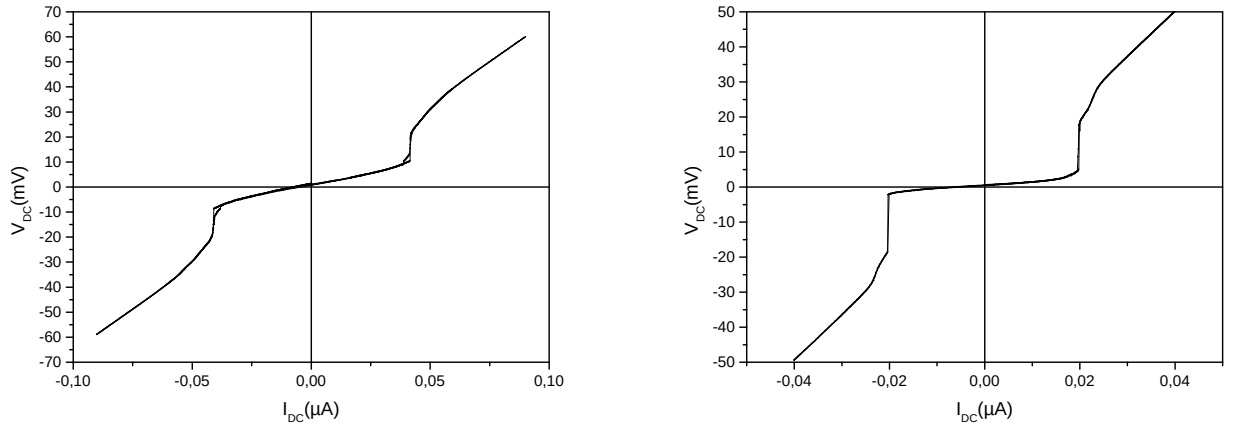


Figure 3.45: I-V characteristics measured at 50mK: (left) for the central bar structure, (right) for the SQUID geometry.

Concerning the SOI:B SQUID, the next step was to apply a magnetic flux to analyse the critical current behavior as a function of the applied magnetic flux. We remind here that the critical current would be periodically modulated with a period ϕ_0 as a function of the magnetic flux. Moreover, ϕ_0 should coincide with one flux quantum in a surface area equal to the surface of the SQUID loop.

Unfortunately, the SQUID effect was not observed since the expected evolution of the critical current with the magnetic flux was not measured. Despite the fact that we did not manage to fabricate a superconducting SOI:B SQUID presenting a SQUID effect, these first results are in any case extremely encouraging. The nanofabrication is a difficult task and the crucial step of etching will have to be improved, for example by adjusting the etching recipe, to avoid causing damage to the SOI:B layer.

At room temperature, we can use the Hall effect to determine the carrier density in the highly doped SOI:B Hall bar. Using the results from the Hall effect calculations, we define the potential difference across the device, the Hall voltage V_H, which is related to the Hall field, by

$$V_H = \left(\frac{1}{ne}\right) IB \tag{3.6}$$

where I is the current flowing through the bar, B is the magnetic field applied perpendicular to the sample and n is the charge carrier number density.

The term in parenthesis is known as the Hall coefficient R_H, defined as

$$R_H = \frac{1}{ne} \ . \tag{3.7}$$

The Hall coefficient is positive if the charge carriers are positive, and negative in the other case. Here, the boron dopants correspond to a P-type doping. When mixed into the silicon lattice, they form holes, consequently the sign of R_H will be positive.

Experimentally, we measured $R_H = 0.1\Omega/\mathrm{T}$, leading to a charge carrier density $n = 6.25.10^{15}\mathrm{cm}^{-2}$, which is slightly lower than the expected value of $2.5.10^{16}\mathrm{cm}^{-2}$. As mentioned before, due to the very high boron concentrations in the top silicon layer which create strong disorder, we can assume that all the boron dopants are not active, thus explaining this result.

Chapter 4

Schottky barrier MOSFETs with superconducting source and drain

Contents

Introduction

We want to build a new type of superconducting qubit involving a Josephson junction whose critical current can be modulated with a gate. More precisely, we aim at fabricating a Josephson Field Effect Transistor (JOFET) with high quality interface, allowing a dissipationless supercurrent to flow through it. The Josephson junction (tunnel, SNS) is the basic brick in nanoelectronics and is used in many common devices such as SQUIDs or qubits. However, to provide a control with a gate, the use of a semiconductor material is needed. The idea is therefore to conceive a nanotransistor with a semiconductor silicon channel coupled to two superconducting source and drain contacts. The superconducting material used to realize these contacts has to be compatible with the silicon technology, for reproducibility and scalability reasons. Moreover, the quality of the interface between the source (drain) and the channel has to be transparent enough to allow a supercurrent to flow through the transistor. For nanodevices, it will emerge an interplay between two conflicting phenomena; the Coulomb blockade, which is a single-particle process, and superconductivity, involving a large number of electrons condensing in a macroscopic quantum state. The interest of this study is thus to realize such nanodevices in order to better understand how this kind of hybrid transistor can adapt itself to these two different behaviors. Moreover, by varying the charging energy, for example by modifying the size of the quantum dot, it will be possible to switch from one behavior to the other one, with one single technology.

Two independent groups have demonstrated so far a new transmon qubit scheme, consisting of two superconductors bridged by a indium-arsenide (InAs) semiconductor nanowire. The nanowire replaces one of the basic elements of a superconducting qubit, that is to say the insulating barrier between two superconducting materials that forms a Josephson junction. In fact, InAs nanowires appear to be ideal candidates for this purpose because they are relatively easy to grow as single crystals. To contact the nanowire, Di Carlo's group uses NbTiN [5], while Marcus' group uses epitaxially grown Al [72]. Nevertheless, it seems rather difficult to integrate easily a nanowire into a superconducting circuit, and even more to reproduce it successfully. That is the reason why we are interested to fabricate a superconducting qubit which is compatible with the silicon technology.

We offer in this thesis two different ways to introduce superconductivity in transistors. The first promising way using superconducting silicon has already been developed in a previous section. The second road is to include superconducting silicides that are fully CMOS compatible. Some of them have already been used in the past such as PtSi [73] or $CoSi_2$ [74]. Both are superconducting with critical temperatures around 1K and 3K respectively. The silicides are commonly used in silicon technology to provide electrical contact between the silicon source and drain and the metallic connecting pads. Some ten years ago, silicide contacts were studied in detail at LETI and elsewhere to fabricate what is called the Schottky barrier MOSFET. The idea was to implement the silicide as close as possible to the active channel of the transistor with the hope to reduce the access resistance. The results obtained demonstrated rather low Schottky resistance ($\sim 10^{-8}\Omega.\mathrm{cm}^2$) but was not significantly lower than for the traditional geometry. Therefore, this technique was

more or less abandoned. However, some wafers from the LETI, processed in 2009, were still available and never studied in detail at low temperature.

I will present in the first part of this chapter the experimental conditions to obtain superconducting PtSi at the LETI. Then, I will study a first structure called Kelvin cross device composing of PtSi to check the superconducting continuity in the nanodevice. Finally, I will measure at very low temperature two transistors with different channel size and with superconducting PtSi source and drain contacts. I will explain the transport properties in such hybrid structures, in which the competition between superconductivity and Coulomb blockade is essential.

4.1 Fabrication of superconducting PtSi silicide

The first goal was to determine the experimental conditions to realize superconducting PtSi silicide on full sheet wafers. For this reason, we have fabricated eight PtSi wafers with different conditions of annealing temperature and time, at the LETI. The sheet resistances of these wafers have been afterwards measured at room temperature and also their critical temperatures using the PPMS. All the characteristics of these wafers are summarized in Tab.4.1.

Wafer number	1	2	3	4	5	6	7	8
Annealing temperature (°C)	350	400	450	500	350	400	450	500
Annealing time (s)	30	30	30	30	60	60	60	60
Critical temperature (K)	0.24	0.26	0.66	0.64	0.27	0.25	0.67	0.66
Sheet resistance (Ω)	224.35	220.72	45.32	46.68	224.35	217.55	43.96	45.32

Table 4.1: PtSi samples realized at LETI.

We observe that all these samples are superconducting, but with very distinct critical temperatures ranging from 0.24K for the lowest to 0.67K for the highest ones. In fact, the expected critical temperature for PtSi films is close to 1K. The superconducting wafers with the highest T_c are the ones corresponding to the superconducting PtSi phase that we were looking for. We can assume that the wafers revealing critical temperatures of the order of 0.25K correspond to another phase, most likely to the Pt_2Si, which would explain why the T_c were so different from the expected value.

We can also deduce from Table.4.1 that the annealing temperature is a determinant factor to obtain superconducting PtSi; in fact, this is observed for an annealing temperature at least equal to 450°C. However, it seems that the annealing time does not play a role in the fabrication of the superconducting silicide. For wafers 3, 4, 7 and 8 with good experimental conditions, the superconducting transitions are complete and abrupt, with a critical temperature close to 0.65K, as shown in Fig.4.1.

In order to better understand the dependence of the critical temperature of our samples with the annealing temperature, X-ray diffraction measurements were performed at LETI.

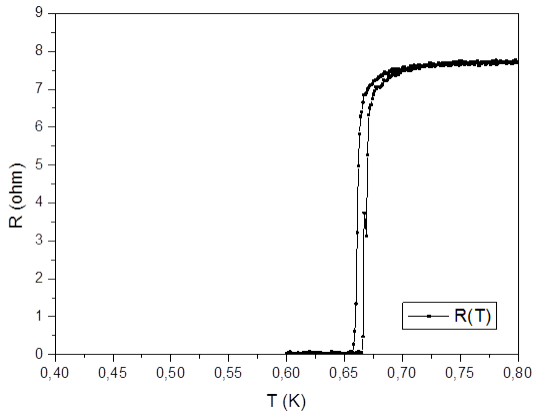


Figure 4.1: Complete and abrupt superconducting transition of PtSi wafer 8, fabricated with an annealing temperature of 500°C and an annealing time of 60s.

The XRD characterizations in the in-plane configuration, for the first four samples annealed during 30s, are presented in Fig.4.2. The XRD spectra obtained for the sample 3 and 4 show a similar behavior with peaks of equal intensities and present at the same angle. However, the spectra of the sample 1 and 2 denote an absence of peak. We aim at comparing the XRD peaks obtained for the sample 3 and 4, i.e., their intensities and their associated angles, with the PtSi JCPDS card, which groups all the peaks in the 2θ spectra associated with the PtSi phase. It was actually possible to assign all the spectra peaks of sample 3 and 4 to the PtSi phase. Thus, it reveals that the obtained phase for these two samples is PtSi and moreover, this phase is crystalline. Nevertheless, it is important to specify that a certain number of peaks in the PtSi JCPDS card was not identified in the in-plane configuration spectra. We can assume that the crystalline PtSi may have some planes with an out-of-plane orientation, which are not detectable with these measurements, thus explaining the missing peaks.

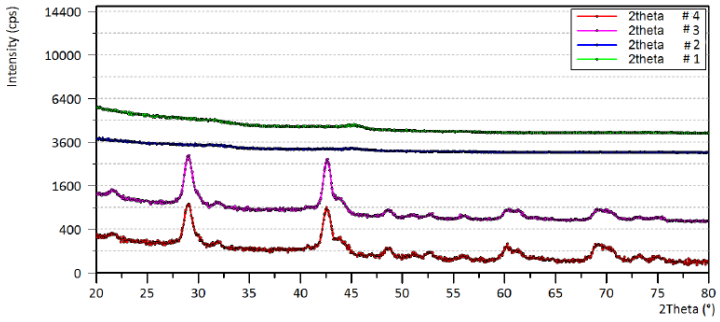


Figure 4.2: In-plane X-ray diffraction for the samples 1, 2, 3 and 4. The XRD spectra of samples 1 and 2 are very similar, such as the behaviors of samples 3 and 4. The presented spectra are here shifted for more clarity.

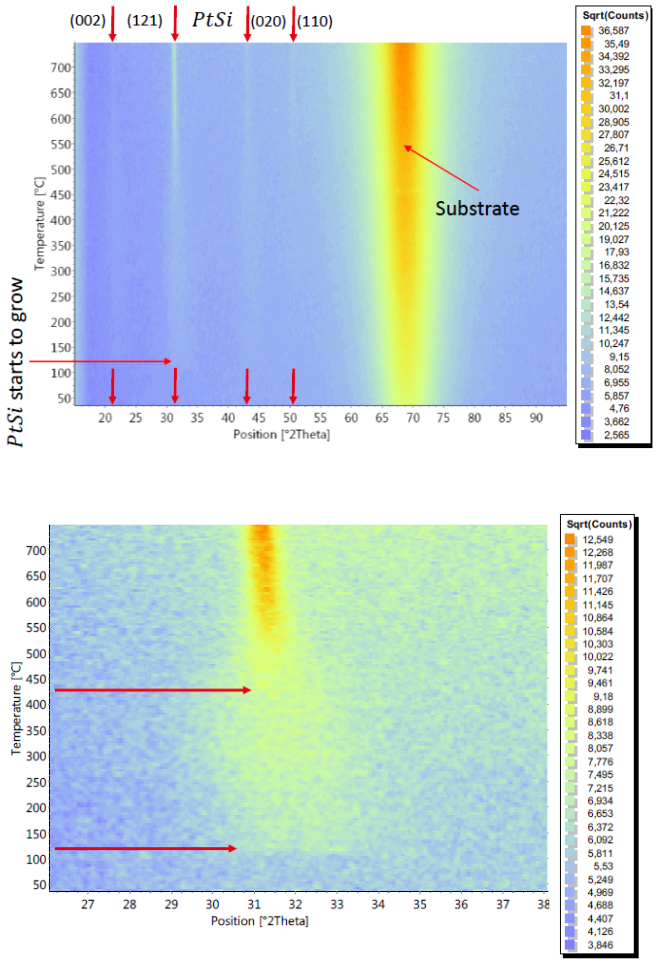


Figure 4.3: In-plane XRD measurements performed when the sample 2 was re-annealed, presenting the diffracted intensity with respect to the annealing temperature and the angle. The large peak on the right of the first spectrum corresponds to the substrate. The four peaks are assigned to the PtSi phase. The second spectrum is a zoom on the peak at 31.5°, revealing more precisely at which temperature the PtSi starts to grow and when its growth rate begins to rise drastically. (Internship Antonio LACERDA, CEA, 2017)

The sample 2 was afterwards re-annealed and in-plane XRD measurements were realized. Fig.4.3 presents the diffracted intensity for the sample 2 as a function of the annealed temperature and the angle 2θ. The re-annealing was performed starting from the temperature of 50°C to 700°C. We observe the large substrate peak on the right of the spectrum, and also four thinner and weaker peaks for 2θ equal to 21.6°, 31.5°, 43° and 50.5°. Furthermore, these four peaks are appearing for an annealing temperature around 120°C. If we zoom on the peak at 31.5°, we clearly see that its intensity begins to increase slightly around 450°C, and then it strongly rises when increasing the annealing temperature, until 700°C. By using the PtSi JCPDS card, it is possible to attribute each of the four peaks, confirming the PtSi phase. The strong intensity increase noticeable around 450°C on the

XRD spectrum is probably the sign of the drastic rise in the PtSi growth rate. This is in very good agreement with our preliminary results, where the phase obtained for an annealing temperature higher than 450°C, was crystalline PtSi and no in-plane Pt_2Si. Interestingly, it means that for temperatures which do not exceed 450°C, the Pt_2Si is still present for an annealing time of 30s.

Finally, the XRD measurements confirm the results obtained on the PtSi samples fabricated at LETI. The annealing temperature has a major influence on the critical temperature of the samples. The XRD spectra have shown that the PtSi begins to form at a temperature around 120°C and its growth rate considerably increases from 450°C. We can deduce that below 450°C, the Pt_2Si phase has not been entirely consumed, explaining the low critical temperatures. However, above this temperature, the single phase is crystalline PtSi.

4.2 Superconducting PtSi on devices

4.2.1 Kelvin cross

We remind here that we aim at studying electric transport in silicon MOSFETs with superconducting PtSi source and drain contacts. After investigating, we have found such devices in P834 Mina wafers fabricated in LETI in 2009.

Before considering the MOSFETs, we first want to study a simplest device using the same PtSi to test its superconductivity at low temperature. Thus, we examined on the same Mina wafers a structure called Kelvin cross, which is used to contact the transistors. The Kelvin cross is composed of several layers, as it is presented in Fig.4.4. The lower electrode of the Kelvin cross corresponds to the PtSi layer. The PtSi silicide has been fabricated with an annealing temperature of 550°C; consequently, according to our preliminary study, it should be superconducting. On top of it, the via composed of a W/TiN/Ti stack has been deposited. Importantly, it has been shown that the most significant decrease in the access resistance is obtained by replacing the TiN layer by a TiN/Ti bilayer [75]. In this case, the contact resistivity is of the order of $0.6\Omega.\mu m^2$, instead of almost $8\Omega.\mu m^2$ [10]. Finally, the upper electrode also named metal 1 is a bilayer composed of 10nm of TiN and 200nm of Cu.

The interesting configuration of the Kelvin cross offers the advantage to measure separetely the upper electrode, the via and the PtSi layer. The resistances of the three main components were measured using the 4-wire sensing. In particular, by applying a current between the contacts 1 and 3, and measuring the voltage between the contacts 2 and 4 (see the positions of the contacts in Fig.4.4(left)), we only register the contribution of the upper electrode. In the same way, the contribution of the via is obtained by applying a current between I_+,I_-=1,5 and measuring the voltage between V_+,V_-=3,7. For the lower electrode, we use I_+,I_-=5,7 and V_+,V_-=6,8. In fact, we want to check if the lower electrode is superconducting at low temperature and if the superconducting continuity is allowed in

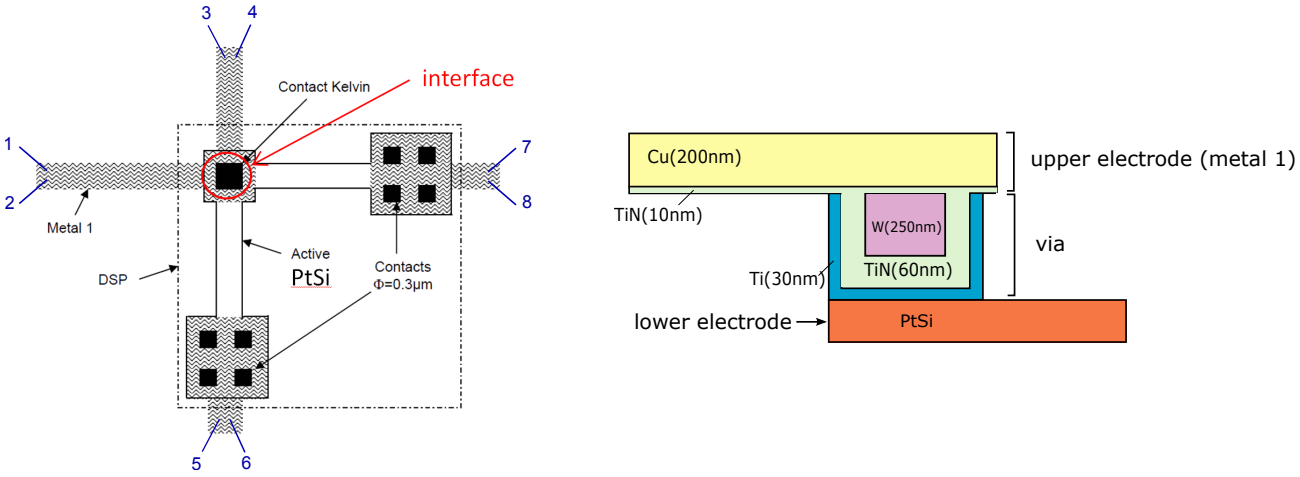


Figure 4.4: Kelvin cross geometry

the entire structure of the Kelvin cross contact. The resistance normalized by the normal resistance as a function of the temperature for the three main components of the Kelvin cross is presented in Fig.4.5.

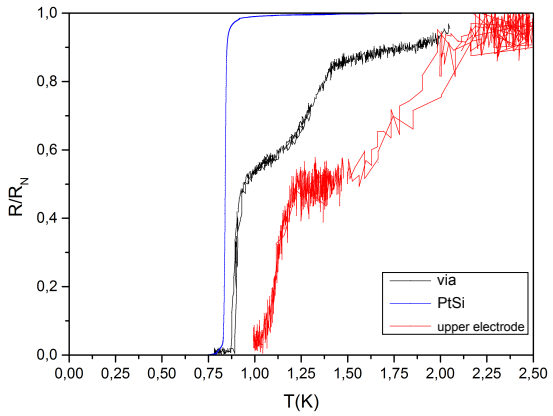


Figure 4.5: Resistance normalized by the normal resistance at 4K with respect to the temperature for the different components of the Kelvin cross, showing superconducting transitions.

We observe that the superconducting transition of the PtSi layer is abrupt and complete. The critical temperature is close to 0.84K, which is in very good agreement with our expectations. Hence, the superconductivity of PtSi is confirmed. Concerning the via (interface) of the Kelvin cross, its transition is superconducting and complete. However, this transition is multiple. We know that TiN is superconducting. Thus, we can assign the first transition around 1.25K to the bilayer TiN(60nm)/Ti. In fact, the thickest layer of TiN will show a superconducting transition in a first place, and the Ti layer of 30nm becomes su-

perconducting by proximity effect. The metallic tungsten layer is completely shunted. The second transition around 0.89K corresponds to the thinnest layer of TiN(10nm). Finally, the upper electrode (metal 1) also shows a complete superconducting transition because of the 10nm TiN layer. This transition is very noisy since the normal state resistance of the upper electrode is very low.

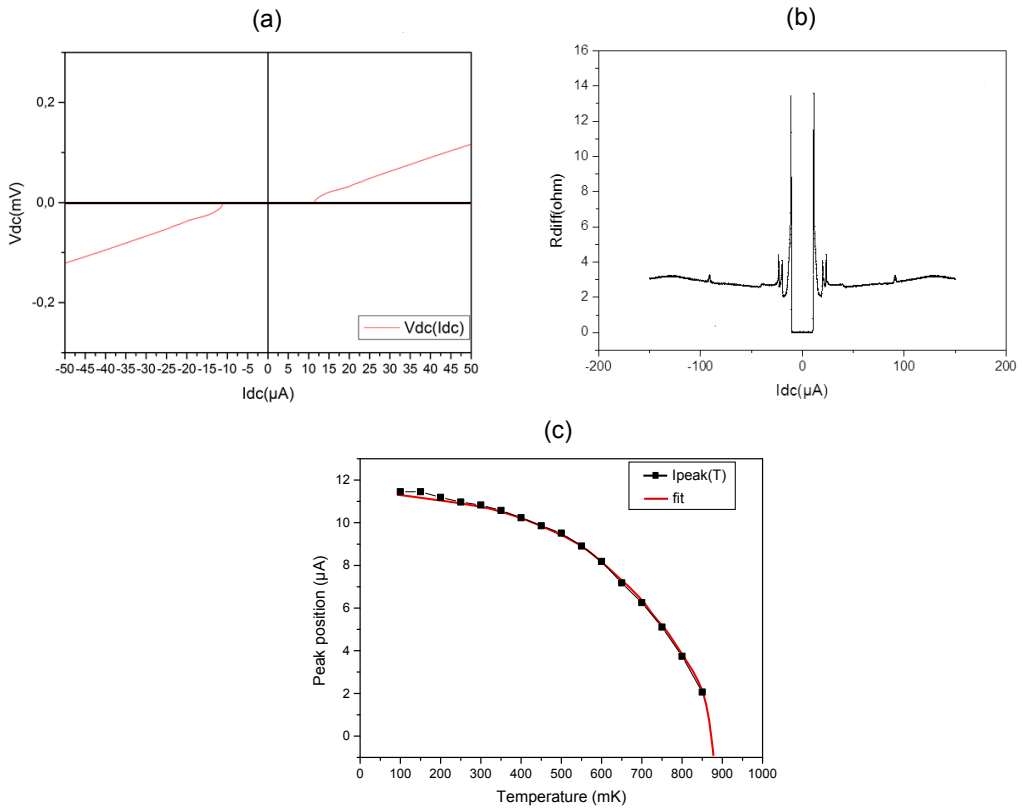


Figure 4.6: (a) I-V characteristics for the via (interface) at 100mK. (b) Differential resistance as a function of the DC current for the via at 100mK. (c) DC current peaks positions in the differential resistance with respect to the temperature. The current decreases when increasing the temperature and vanishes at the T_c of the via.

Moreover, I-V characteristics for the via (see Fig.4.6(a)) obtained at 100mK allows us to identify the critical current of 11.4μA. Measurements of differential resistance as a function of the DC current were also performed for the via at 100mK (see Fig.4.6(b)) and also for different temperatures ranging from 150mK to 850mK. Fig.4.6(c) presents the dependence of the peak position of DC current with the temperature. It slightly decreases when rising the temperature and vanishes when reaching the critical temperature. This behavior respects the BCS theory (see fit in Fig.4.6(c)).

To conclude, we have tested at low temperature Kelvin cross structures present on P834 wafers. These devices allowing to contact the transistors, are very interesting since they allow us to test independently the different constituents. The measurements performed

reveal the PtSi superconductivity and moreover, the superconducting continuity in the Kelvin cross. The next step is therefore to study the MOSFET itself.

4.2.2 Schottky barrier MOSFETs with superconducting PtSi source and drain

4.2.2.1 Introduction to Schottky barrier MOSFET

The standard MOSFET device fabricated at LETI presents metallic contacts made of an alloy of Si and metal called silicide, in the source and drain region. Nowadays, the LETI uses the NiPtSi silicide which is not superconducting at very low temperature. The layer of NiPtSi is rather thin and sits on doped silicon. In comparison, the Schottky barrier MOSFET (SbMOSFET) adopts a PtSi silicide for the source and drain contacts. This silicide has slightly diffused under the spacers and is really close to the active silicon channel. The SbMOSFET also forms Schottky contacts at the interface between the PtSi metallic silicide at room temperature and the silicon channel. The sketches of the two devices are illustrated in Fig.4.7.

The Schottky barrier MOSFET offers several advantages in comparison to usual MOSFET. In fact, it provides a high thermal stability and reduces the parasitic source/drain resistances. For instance, in general, the silicide has a much lower specific sheet resistance than highly doped silicon. Due to its benefits, the SbMOSFETs have been proposed as an alternative to usual MOSFETs and have received an increasing interest in the recent years. Despite these advantages, it is nevertheless important to mention several issues appearing with SbMOSFETs. Firstly, the drive current I_{ON} is limited by the Schottky barrier height. Consequently, the SbMOSFETs still do not reach the best $I_{ON} - I_{OFF}$ performance achievable with MOSFETs. Secondly, the SbMOSFET has a higher leakage current than the conventional MOSFET due to the tunneling current between the silicon substrate and the silicide.

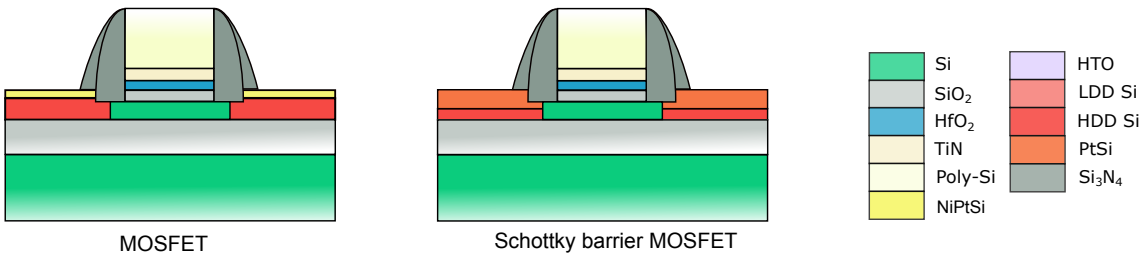


Figure 4.7: Comparison between the MOSFET device with metallic contacts fabricated with NiPtSi silicide (not superconducting) and the Schottky barrier MOSFET with metallic contacts made of PtSi silicide (superconducting), which has slightly diffused under the spacers. The PtSi silicide is really close to the silicon channel. Both devices are fabricated at LETI.

4.2.2.2 Description of our devices

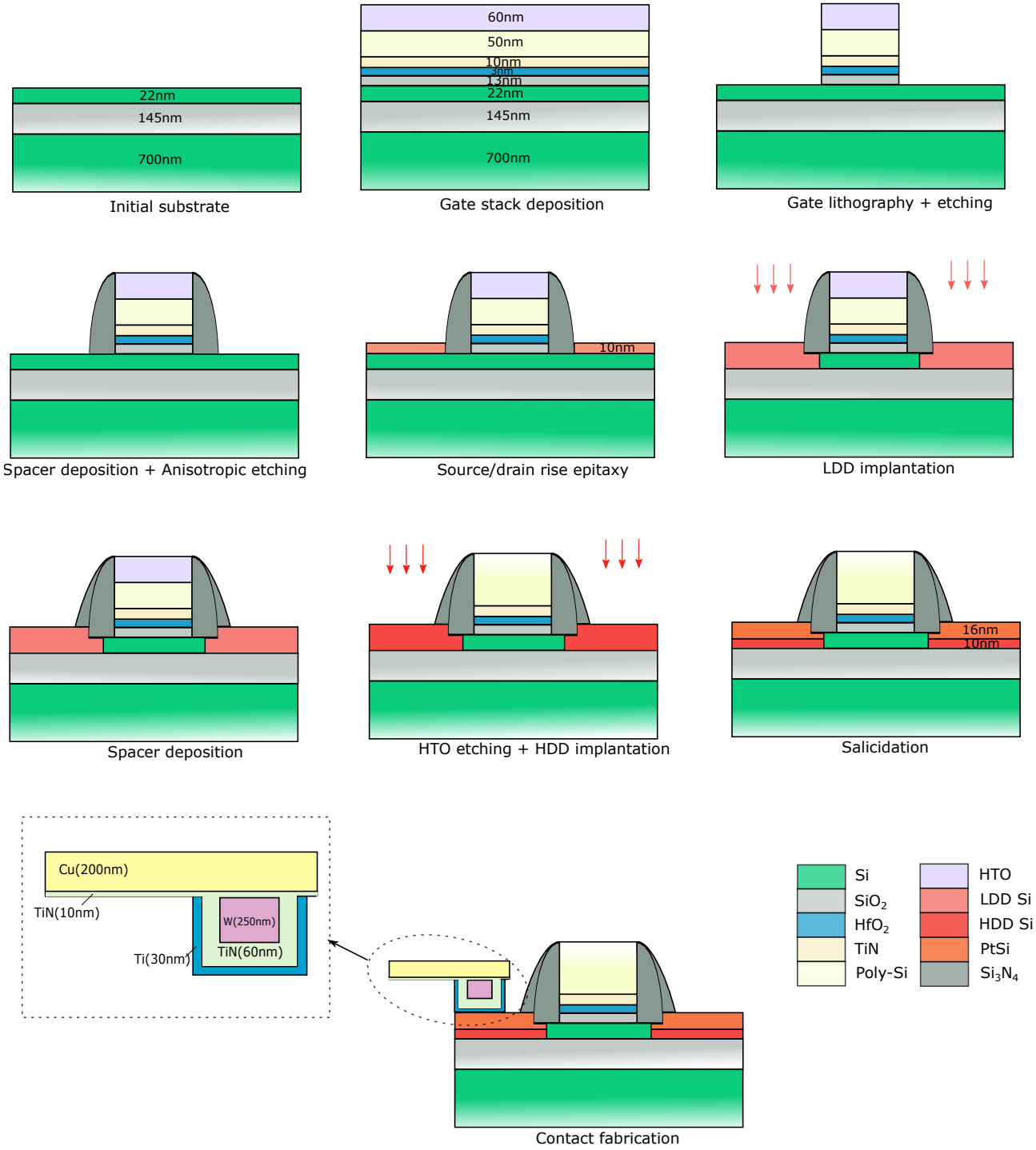


Figure 4.8: Fabrication of the Schottky barrier MOSFET with PtSi source and drain.

The different steps of the Schottky barrier MOSFET fabrication are explained here (see

Fig.4.8). Samples fabrication takes advantage of the established and mature Complementary Metal-Oxide-Semiconductor (CMOS) technology and start from a SOI substrate from the LETI. On top of the BOX which is a 145nm thick layer of silicon dioxide, lies a 22nm layer of high-quality silicon.

The first step of the fabrication process defines the silicon channel. The gate stack deposition is afterwards realized. The gate stack is composed of several layers, including an insulating layer and metallic layers above the latter. The insulator is a 3nm thick layer of hafnium-based oxide HfO_2, which is a high-κ oxide, whose dielectric constant is larger than in the silicon dioxide [76] (ε_κ = 22-25 and ε_{SiO_2} = 3.9). However, the interface between the silicon and the high-κ oxide HfO_2 is not optimal, inducing additional noise at low temperature [77]. To solve this problem, a thin layer of thermally grown SiO_2 (13nm) is added between the two materials, creating a better interface. The metallic layers are composed of a 10nm thick layer of TiN and about 50nm of poly-silicon. On top of these layers acts the 60nm of HTO as hard mask. The lithography allows to define the shape and size of the wanted gate and the gate etching is afterwards performed. Considering the small sizes of our devices, the e-beam lithography is needed.

Since the presence of gates is not sufficient to completely protect the active area, self-aligned sidewall spacers are deposited (LPCVD) on both sides of the gates. They are made with the Si_3N_4 oxide and they are 10nm long.

In order to lower the access resistance and facilitate the future dopants implantation, the thickness of the exposed silicon forming the source and drain contacts is increased by 10nm with a selective rise epitaxy. We note that the top of the poly-silicon gate is still protected by the HTO layer. The dopant implantation can be now perfomed in two steps, i.e., a first low-dose implantation called Low-Doped-Drain (LDD), followed by a high-dose one named High-Doped-Drain (HDD). Between the two dopant implantations, a second spacer deposition is done. The HTO layer can be removed after this spacer deposition.

The final fabrication step is the metallization of the source and drain. In our case, the alloy formed is the 16nm thick PtSi silicide. Afterwards, the contacts will be deposited on the PtSi. The different layers composing the Kelvin cross contact and their dimensions are reminded in Fig.4.8.

4.2.2.3 Experimental results

Here we present the results of our measurements in order to characterize the devices. The studied devices come from the wafer P834W06. The working Schottky barrier MOSFETs exhibiting a field effect at room temperature were selected using the probe station (Fig.4.9), installed at the CEA-Pheliqs. It allows to choose the best candidates for future very low temperature measurements. A constant bias voltage V_{DS} between the source and drain of 10mV is applied. By sweeping the gate voltage V_G from -1V to 1V, we measure the current I_{DS} flowing between the source and the drain.

Unfortunately, as these samples are extremely fragile, we found many MOSFETs of this wafer broken at room temperature. Some of them presented a gate leakage current, in others the PtSi silicide had so much diffused under the spacers that a shunted transistor has been created. This new configuration can be however useful to measure the critical temperature of the PtSi silicide. A very small number of operating MOSFETs was measured at the probe station.

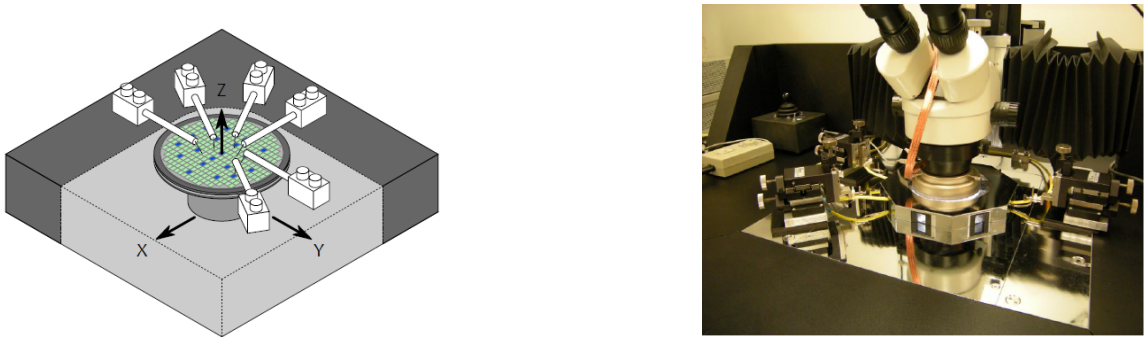


Figure 4.9: Probe station sketch and photo.

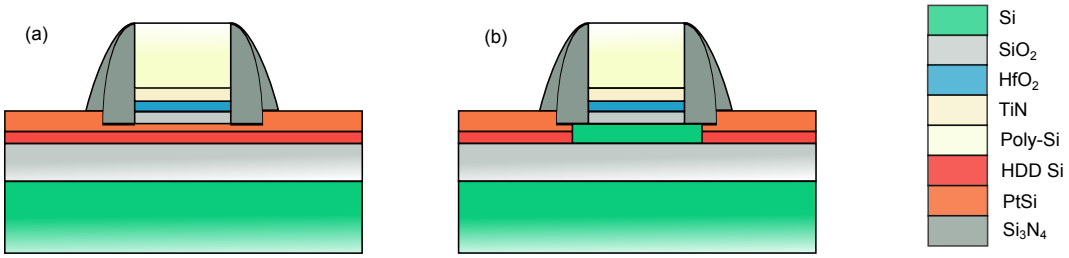


Figure 4.10: (a) Shunted transistor: the PtSi silicide has spread too far under the spacers, (b) Schottky barrier MOSFET

We decided to measure in a dilution cryostat one shunted transistor and one Schottky barrier MOSFET, as shown in Fig.4.10.

Shunted transistor FD3N03-4 (L = 0.03μm and W = 10μm)

The studied shunted device named FD3N03-4 has the following dimensions for the silicon channel : L(length) = 0.03μm and W(width) = 10μm. Its resistance at 300K R_{300K} is 353.4Ω and at 4K, R_{4K} = 268Ω. These results are consistent with a metallic behavior.

At very low temperature, the resistance with respect to the temperature is measured, showing an abrupt and complete superconducting transition (see Fig.4.11). The critical temperature of the PtSi link, part of the shunted transistor, is of the order of 0.88K, which roughly corresponds to the expected value for the T_c of PtSi.

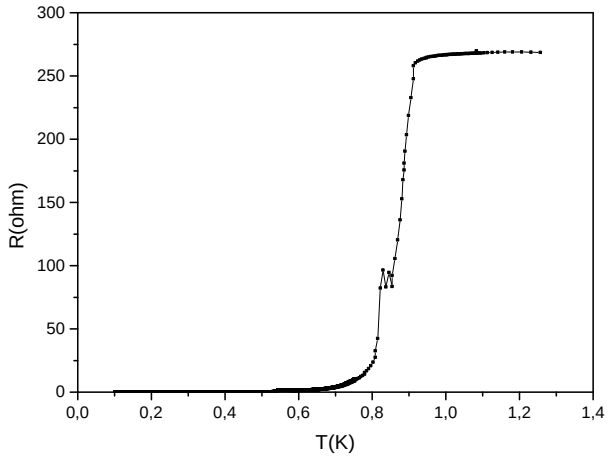


Figure 4.11: Superconducting transition of the PtSi link of the shunted transistor FD3N03-4 (L=30nm × W=10μm)

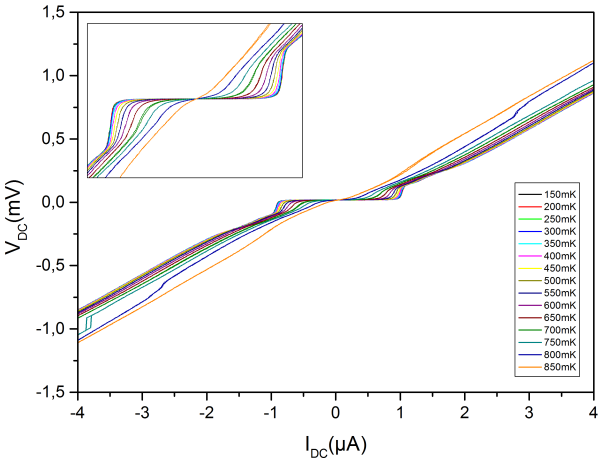


Figure 4.12: V-I characteristics at different temperatures showing hysteresis below the critical temperature.

V-I characteristics were also performed for various temperatures, ranging from 150mK to 850mK, approaching to the T_c (see Fig.4.12). It allows us to identify the critical current I_c of 1μA of the PtSi link. Below the critical temperature, we observe that the V-I characteristics present a strongly hysteretic response.

The critical current decreases when increasing the temperature and vanishes when reaching the critical temperature. A simulation shows that the evolution of I_c with the temperature is in very good agreement with the BCS theory (see Fig.4.13).

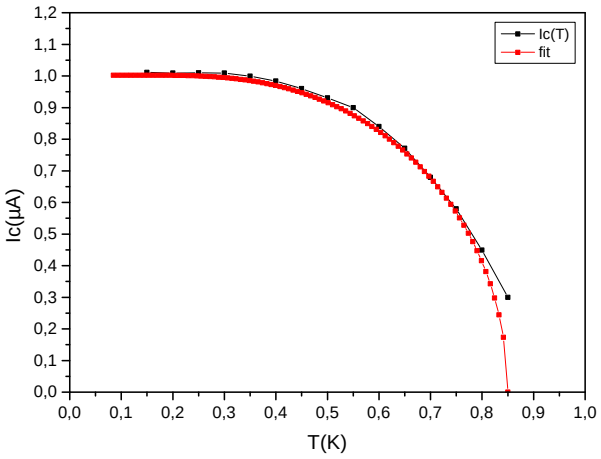


Figure 4.13: Evolution of the critical current I_c with the temperature. I_c diminishes with the increasing temperature, until it disappears at T=T_c. This evolution is perfectly consistent with the BCS theory, as the simulation proves it.

Results on the Schottky barrier MOSFET PTL50RSUB1-2 (L = 50nm × W = 50nm)

After considering a PtSi shunted transistor, we aim at measuring a Schottky barrier MOSFET at very low temperature to study its electronic transport. The first measured Schottky barrier MOSFET named PTL50RSUB1-2 has a extremely small silicon channel with dimensions L = 50nm × W = 50nm. This MOSFET comes from the die 10 of the wafer P834W06.

At 4K, we measure Coulomb oscillations. At 200mK, the current flowing between the source and the drain I_{DS} as a function of the bias voltage V_{DS} and the gate voltage V_G shows very sharp Coulomb diamonds, as seen in Fig.4.14. The noticeable symmetry of the Coulomb diamonds suggests equivalent tunnel coupling to the source and drain leads. Importantly, by zooming on the map, we observe that the Coulomb diamonds are separeted by an energy gap corresponding to the superconducting gap of the PtSi silicide $2\Delta/e \simeq$ 0.3mV, where there is no current flowing through the device. This gap can be in fact derived using the formula of the BCS theory, $\Delta = 1.76 k_B T_c$, with $T_c = 0.88$K. From the Coulomb diamonds pattern, we can also extract the charging energy roughly equal to 1.25meV. We measure here the "standard" S-QD-S transistor behavior.

At 200mK, the next step was to add a magnetic field higher than the critical magnetic field of the superconducting PtSi to "kill" superconductivity and recover the normal state. The interesting point would have been to check if the conventional closed Coulomb diamonds would appear. This would have been the final compelling evidence of the superconductivity effect in the Schottky barrier MOSFET device. Unfortunately, the SbMOSFET broke during the measurements without letting us the chance to complete it.

Results on the Schottky barrier MOSFET FD3N10-4 (L = 0.06μm and W = 0.8μm)

The second measured Schottky barrier MOSFET called FD3N10-4 has the following channel dimensions : L = 0.06μm and W = 0.8μm. In comparison to the first measured MOSFET, the latter presents a larger conducting silicon channel. Importantly, I want to specify that a FDSOI transistor is in a backgated configuration due to the presence of the buried oxide. In fact, the so-called top gate is known as the principal usual gate and the substrate acts itself as the backgate. At low temperature, the silicon underneath the BOX is not conducting. In order to use it as a backgate, we have implemented a LED at low temperature allowing charge transfer at the down part of the BOX.

At room temperature, we first want to measure the current flowing between source and drain and also the differential conductance as a function of the gate voltage. Actually, we performed a lock-in measurement with our device. In this lock-in measurement, we combined a DC source/drain voltage with a smaller AC voltage. By measuring the change in current in response to the AC voltage, we can directly extract the differential conductance ∂I/∂V. The typical characteristics at 300K of this SbMOSFET are shown in Fig.4.15. These characteristics present the source/drain current and the differential conductance

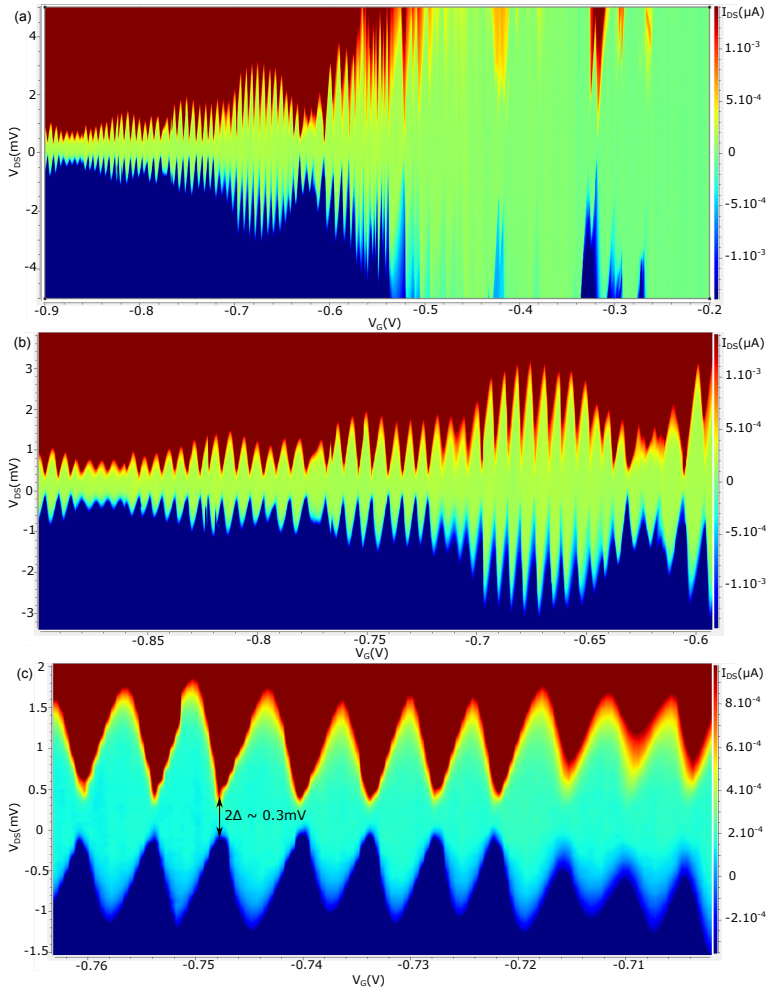


Figure 4.14: (a) D/S current map of rather symmetrical sharp Coulomb diamonds at T = 200mK, with an applied gate voltage ranging from -0.9V to 0.2V. The diamonds regions coincide with a current I_{DS} equal to zero. Each diamond corresponds to a fixed number of electrons within the quantum dot. (b,c) By zooming, the Coulomb diamonds are more and more visible and sharp. On (c): an energy gap separating the Coulomb diamonds in two parts is noticeable and corresponds to the superconducting gap of the PtSi 2Δ.

G_{diff} as a function of the gate voltage V_G, for a constant bias voltage V_{DS} equal to 100μV and an AC voltage of 100μV, and for various applied backgate voltages V_{BG} ranging from 0V to 30V.

The saturation regime of the $I_{DS} - V_G$ curve shows a rather small drive current I_{ON} around 10nA, in comparison to the one that we could expect for a traditional MOSFET device. Depending on V_G and V_{DS}, the operational regions of a SbMOSFET can be divided into three parts: the sub-threshold regime, the sub-linear regime and the saturation one. Ideally, the sub-thresold regime is dominated by the transport at the Schottky barrier (which limits the current flowing into the silicon channel), and the ON-state of a SbMOS-

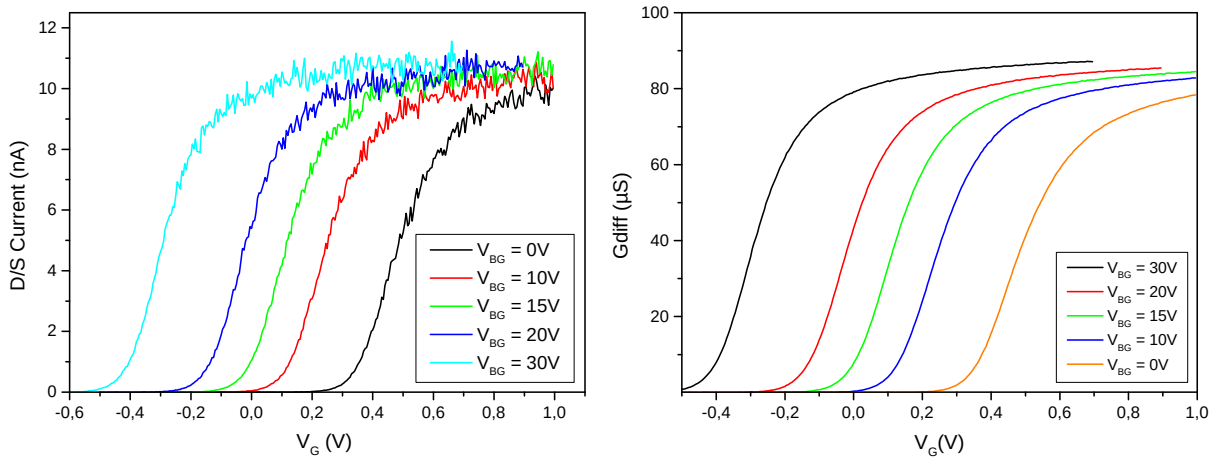


Figure 4.15: Characteristics of the SbMOSFET at T = 300K, for $V_{DS} = 100\mu$V, $V_{AC} = 100\mu$V and for various values of backgate voltages. In the saturation regime, I_{ON} is close to 10nA and the differential conductance roughly equals to 80μS.

FET is determined by the drift-diffusion transport in the channel. However, the Schottky barrier at the interface between the silicide contacts and the channel is not sufficiently transparent to allow the transport to be only limited by the channel resistance during the ON-state. Thus, it explains the low value of the drive current of the Schottky barrier MOSFET.

According to our measurements, the applied backgate voltage has a small influence on the drive current I_{ON} in the saturation regime. It seems that increasing the backgate voltage contributes to slightly rise I_{ON}. We deduce that the gate and backgate voltages affect only moderately the barrier height and also the carrier density in the conducting channel.

The threshold voltage V_t is defined as the inflection point in the $I_{DS} - V_G$ or $G_{diff} - V_G$ curves. The threshold voltage depends also on the applied backgate voltage, and is obtained by taking the position of the maximum in the derivative of the differential conductance with respect to the gate voltage, see Fig.4.16.

The sub-threshold region usually characterizes the switching behavior of a transitor-like device. The required gate voltage which is needed to change the source/drain current by one order of magnitude is called the inverse sub-threshold slope S. It is given by [78]

$$S = \ln 10 \left(\frac{\partial \ln I_{DS}}{\partial V_G} \right)^{-1} \simeq \ln 10 \frac{k_B T}{e} \left(1 + \frac{C_d}{C_{ox}} \right) \tag{4.1}$$

with C_d the maximal depletion layer capacitance and C_{ox} the gate oxide capacitance.

If $C_d \ll C_{ox}$, S is usually fixed at $\ln 10 \frac{k_B T}{e}$, i.e., 60mV/decade at room temperature. For our studied SbMOSFET, we obtain 92mV/decade, corresponding to 60mV/decade

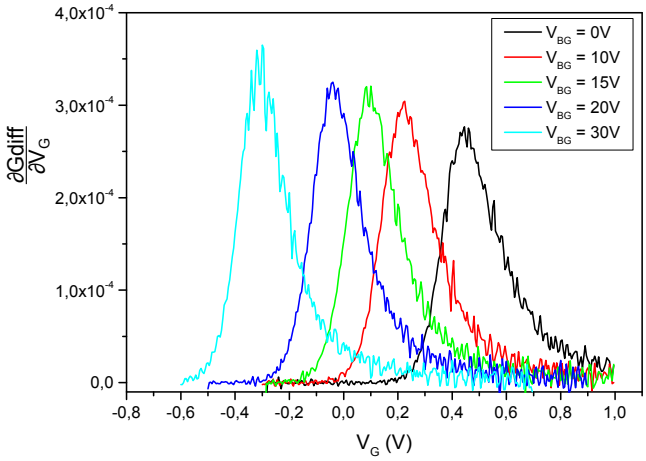


Figure 4.16: Derivative of the differential conductance with respect to the gate voltage, allowing to extract the different threshold voltages for various applied backgate voltages at T = 300K.

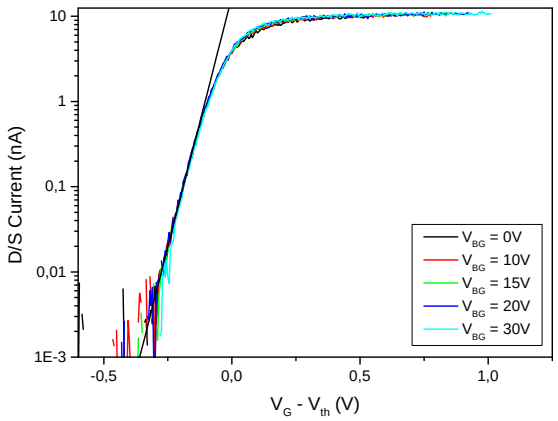


Figure 4.17: Logarithmic dependence of the source/drain current I_{DS} with $V_G - V_{th}$ at T = 300K and for $V_{DS} = 100\mu$V, showing a good scaling. The inverse sub-threshold slope S is equal to 93mV/decade, i.e., 60mV/decade $\times\frac{1}{\alpha}$ with $\alpha = 0.65$.

$\times\frac{1}{\alpha}$, with the level-arm parameter α equal to 0.65, as shows Fig.4.17. We conclude that we measure the "standard" CMOS transistor behavior at 300mK.

At 4K, the characteristics of the SbMOSFET giving the current flowing between the source and drain, and the differential conductance as a function of the gate voltage and for various backgate voltages are presented in Fig.4.18. The V_{BG} are still ranging from 0V to 30V. During these measurements at 4K, the bias voltage is fixed at 100μV and the AC

voltage equals to 100μV. We observe a moderate decrease of the drive current I_{ON} to 6nA. This demonstrates that the transport through the Schottky barrier is not only thermally activated but involves tunnel effect.

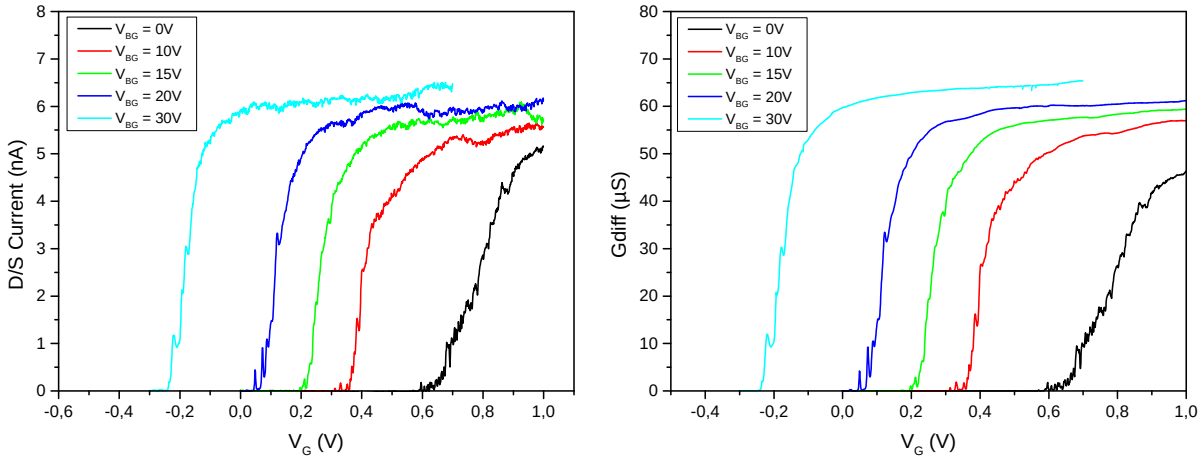


Figure 4.18: Characteristics of the SbMOSFET at T = 4K, for V_{DS}= 100μV and V_{AC} = 100μV. We note a small decrease at 4K of the drive current $I_{ON} \simeq$ 6nA and of the differential conductance Gdiff $\simeq$ 60μS.

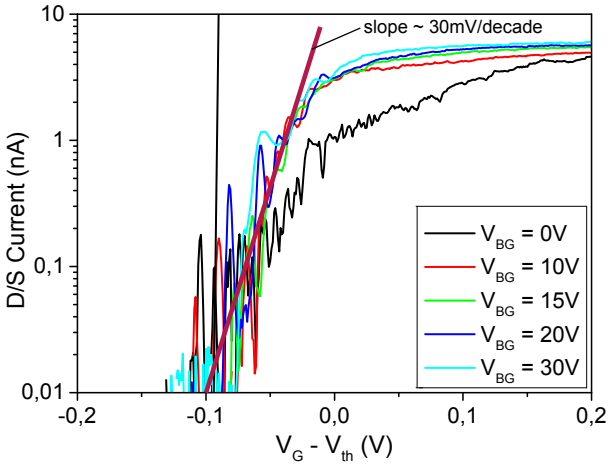


Figure 4.19: Logarithmic dependence of the source/drain current I_{DS} with $V_G - V_{th}$ at T = 4K and for V_{DS} = 100μV, showing a less obvious scaling. The slope of these curves can be estimated to be equal to 30mV/decade.

Furthermore, at 4K, the scaling is not as obvious as at 300K, as it is depicted in Fig.4.19. However, one can estimate a sub-threshold slope which equals to $\sim$ 30mV/decade. This

value is much larger than what is expected if only considering the temperature decrease. Indeed, one should find a slope of 92mV/decade $\times \frac{4K}{300K} \simeq 0.12$. This confirms that the transport is not only thermally activated. Moreover, the curves at 4K in Fig.4.18 seem to present more oscillations than at 300K. This effect seems to be nevertheless less visible when increasing the backgate voltage to 30V.

At $V_{BG} = 10V$, regular oscillations appear in S/D current and differential conductance. In order to test whether these oscillations come from Coulomb blockade, we have measured the S/D current as a function of both the gate voltage and the bias voltage. The S/D current with respect to the bias voltage and the gate voltage is plotted in Fig.4.20(a-b). The applied backgate voltage is 10V. We can distinguish two regimes in these patterns depending on the applied gate voltage.
- For small V_G and more precisely for $V_G < 0.4$V, a series of Coulomb diamonds with different sizes is considered as the potential result of Coulomb blockade on one or several impurity traps in the channel. This is confirmed by the large value of the charging energy, which cannot be the one associated to the size of the channel.
- For $V_G > 0.4$V, the differential conductance shows a large zero bias anomaly which is symmetrical below $V_{DS} = \pm 4$mV (see Fig.4.20(c) for an applied gate voltage of 0.5V). This non-linear behavior is probably associated to dynamical Coulomb blockade arising in mesoscopic system when the access conductance per channel is smaller than the quantum of conductance. Considering the width of our device (800nm) and assuming a Fermi wavelength in silicon of 10nm, one has 80 channels in parallel. As the transport is limited by the barriers, the conductance per channel at each interface is $\sim 2 \times 60\mu S \times \frac{1}{N_{ch}} \simeq 1.5\mu$S, which is much lower than G_Q. At bias voltages above $\pm$ 4mV, the differential conductance curve is highly non-symmetrical. This is a signature of Schottky barrier and appears because the two barriers are not perfectly equal.

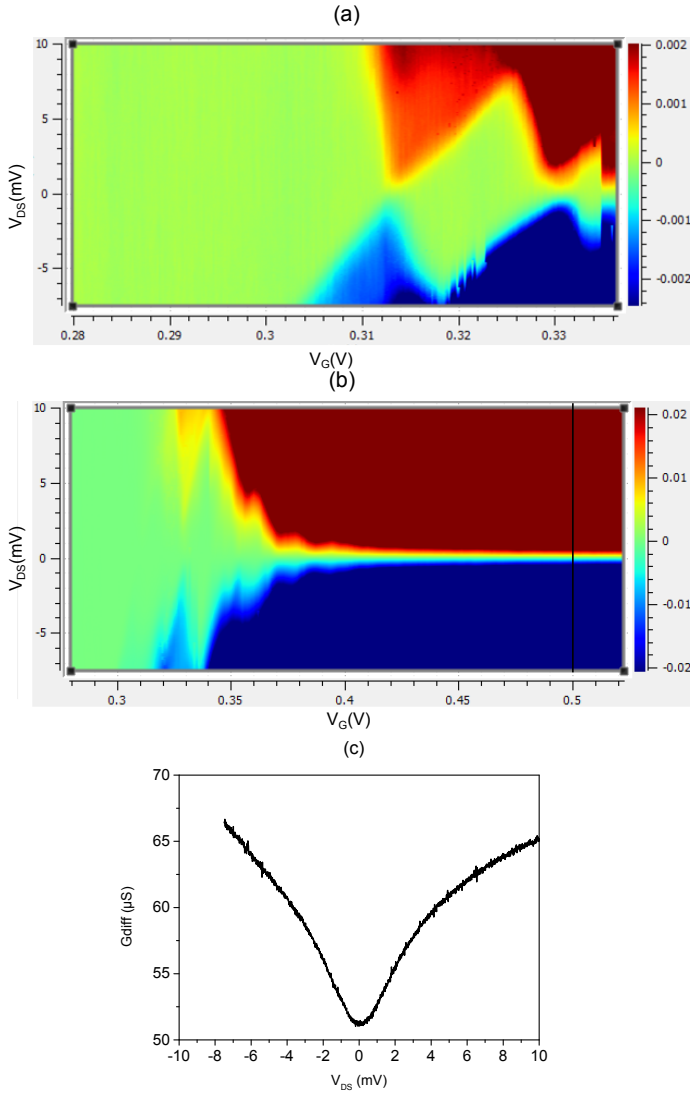


Figure 4.20: SbMOSFET electric transport at 4K, for $V_{BG} = 10$V : (a-b) S/D current as a function of the bias voltage and the gate voltage. We distinguish two regimes depending on the applied gate voltage. (c) Differential conductance anomaly for $V_G = 0.5$V.

At the very low temperature of 200mK, the S/D current and the differential conductance are measured with respect to the bias voltage and gate voltage, for $V_{AC} = 2\mu$V and for $V_{BG} = 30$V. The 2D-graphs are presented in Fig.4.21(A-B). For the differential conductance graph, we note the appearance of two horizontal lines at $\pm$ 0.16mV.

The differential conductance as a function of the bias voltage, at 150mK, for $V_{BG} =$ 30V, and for three different applied gate voltages, $V_G = 0$V, $V_G =$ -0.2V and $V_G =$ -0.22V is plotted in Fig.4.22.
- For $V_G = 0$V, we observe clear coherence peaks at $V_{DS} \sim \pm 160\mu$V and also a large decrease of the differential conductance around zero bias voltage. This behavior looks like

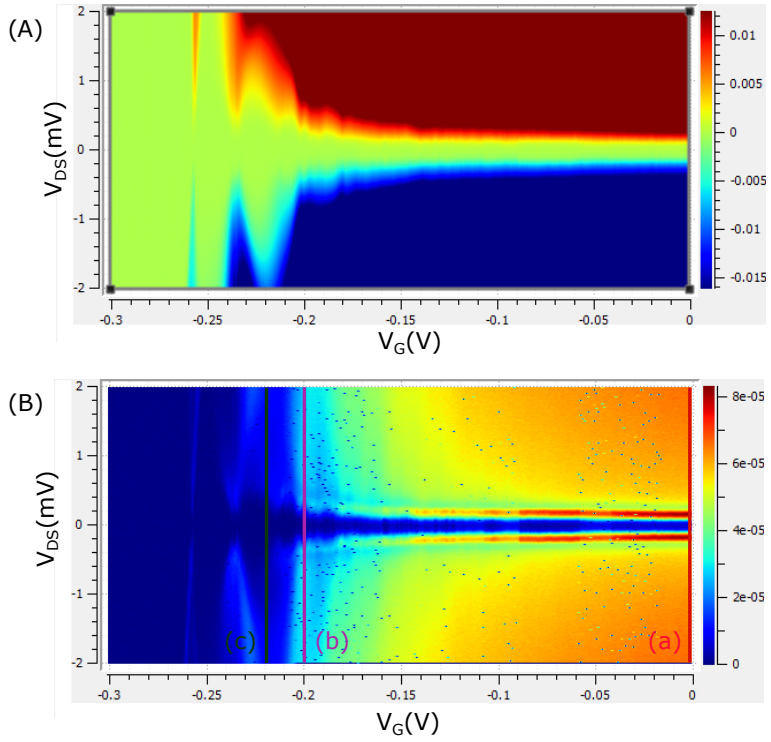


Figure 4.21: (A) S/D current with respect to the bias voltage and gate voltage at 200mK, for V_{BG} = 30V. (B) Differential conductance as a function of the bias voltage and gate voltage, at 200mK, for V_{BG} = 30V and for an applied AC voltage of 2μV.

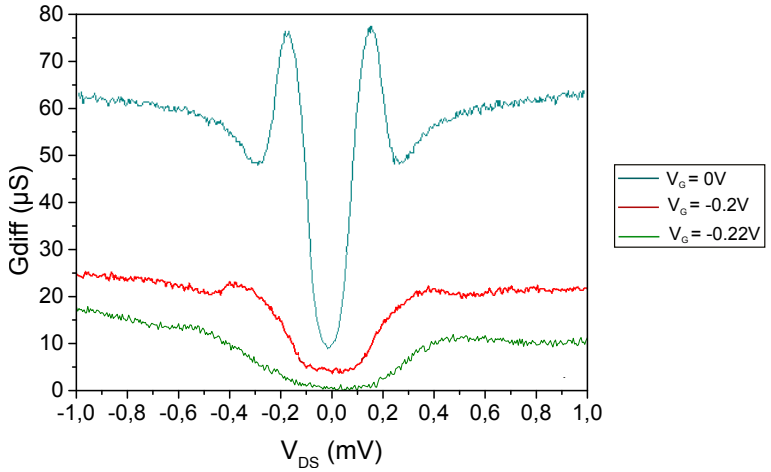


Figure 4.22: Differential conductance as a function of the bias voltage at 150mK, for V_{BG} = 30V and for V_G = 0V (a), V_G = -0.2V (b) and V_G = -0.22V (c).

the electronic response of an SN interface where the peak reflects the discontinuity in the density of states at the superconducting gap.

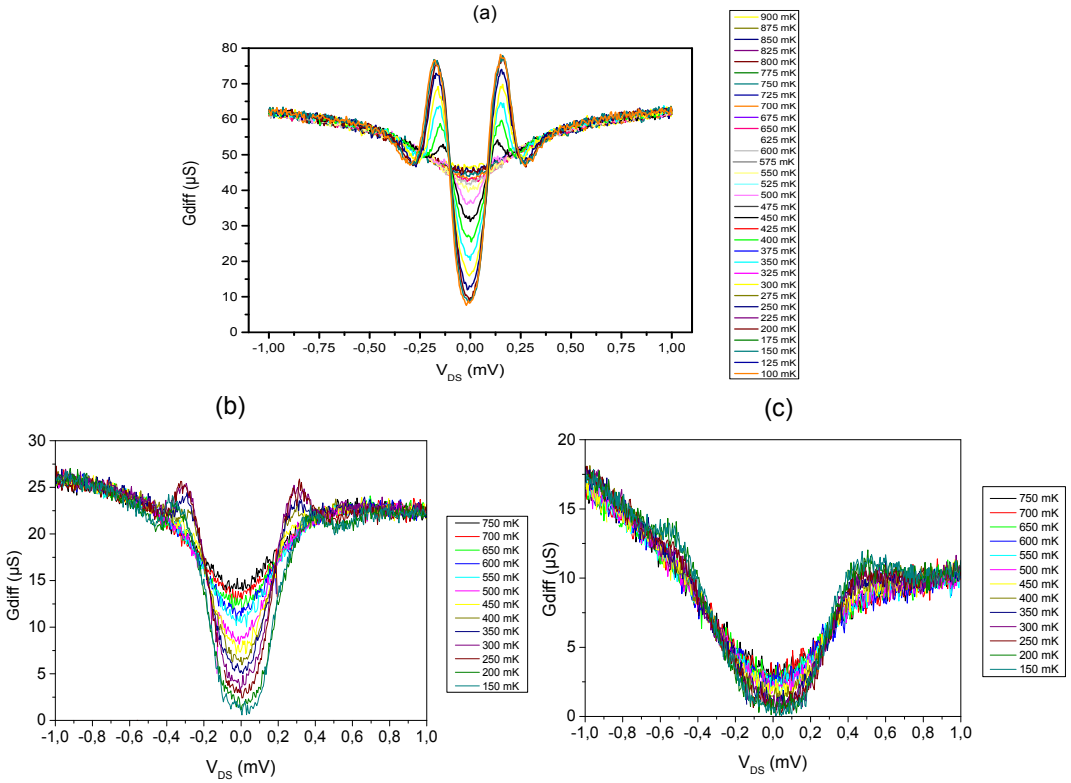


Figure 4.23: Temperature dependence of the differential conductance as a function of the bias voltage, for V_{BG} = 30V and for V_G = 0V (a), V_G = -0.2V (b) and V_G = -0.22V (c).

- For $V_G \neq$ 0V (-0.2V and -0.22V), the coherence peaks are less and less visible and we note a decrease of the overall conductance level. The noticeable asymmetry is due to the Schottky barriers.

Fig.4.23 shows the temperature dependence of the differential conductance with respect to the bias voltage, for V_{BG} = 30V and for V_G = 0V (a), V_G = -0.2V (b) and V_G = -0.22V (c).
- For V_G = 0V, the coherence peaks vanish close to the temperature of 500mK and the differential conductance at zero bias voltage saturates around 750mK. If one plot the bias voltage peak position as a function of the temperature, the dependence is exactly the one of a superconducting BCS gap with T_c = 0.66K (see Fig.4.24). However, the coherence peaks appear at $V_{peak} \simeq 160\mu$V. Using the result of the BCS theory and considering a critical temperature of 0.66K, we obtain a BCS superconducting gap $\Delta_{BCS} = 1.76 k_B T_c = 100\mu$V. Because of the geometry, V_{peak} should be equal to $2\Delta_{BCS} = 200\mu$V. We conclude that the observed superconducting gap is slightly weakened. We can formulate two assumptions to explain this result. Firstly, it is possible that the PtSi which has diffused under the spacers and stands very close to the channel is different from the rest of PtSi silicide. Secondly, we can also imagine that instead of probing the wanted PtSi gap, we probe an induced gap in some remaining silicon close to the PtSi somewhere below the spacers. Both assumptions

would result in a smaller induced gap.

Another interesting point to notice here is the presence of a finite differential conductance at zero bias voltage, for $V_G = 0$V, suggesting a moderate Schottky barrier interface (with a transparency not too low) which has to be determined. Indeed, as seen in Fig.4.25(d), the zero bias conductance is almost zero as soon as the transparency is lower than 0.01.

In Fig.4.23(a), we note the presence of a small dip right after the coherence peak and observe a differential conductance which is not constant at larger bias voltages. This behavior is not usually observed for standard SN interface, and could be the sign of a superconducting effect or a normal effect. To answer this question, in order to recover the normal state, we have applied a magnetic field of 4kG, larger than the critical magnetic field of PtSi (see Fig.4.25). When applying a magnetic field, we observe a series of curves at different temperatures ranging from 150mK to 850mK, presenting the similar behavior than the one obtained at 4K. In fact, the coherence peaks have disappeared and the gap in differential conductance broadens when the temperature increases. We deduce that the presence of the dip is not related to superconductivity. By comparing the differential conductance with respect to the bias voltage, at different temperatures, with and withtout a magnetic field (see Fig.4.25(c)), we see a perfect matching of the differential conductance above the coherence peak. We can deduce that the dip is really due to the interplay between superconductivity and Coulomb interaction.

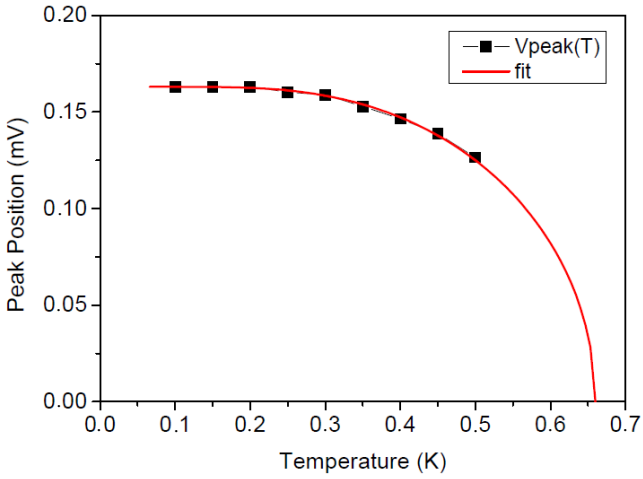


Figure 4.24: Peaks positions in the differential conductance indicating the induced gap as a function of the temperature. As the amplitude of the peaks becomes weaker when increasing the temperature, we were not able to add experimental data above the temperature of 0.5K. However, the first results show a good agreement with the BCS theory.

We want to estimate the transparency of the Schottky barrier of our device. We start

from the conductance at a SN interface in the BTK framework, at T = 0K,

$$G_{NS} = G_Q \sum \frac{2T^2}{(2-T)^2} \tag{4.2}$$

where G_Q is the conductance quantum $\frac{2e^2}{e}$ and T is the transparency per channel.

The conductance at the interface between two metals is given by $G_{NN} = G_Q \sum T$. Thus, we obtain

$$\frac{G_{NS}}{G_{NN}} = \frac{\sum \frac{2T^2}{(2-T)^2}}{\sum T} \simeq \frac{2\Gamma}{(2-\Gamma)^2} \tag{4.3}$$

Considering Fig.4.25(a-b), we can estimate the ratio $\frac{G_{NS}}{G_{NN}} \simeq \frac{10\mu S}{27\mu S} \simeq 0.37$. We get the transparency of the barrier $\Gamma \sim 0.44$. This Schottky barrier of moderate transparency explains the finite differential conductance obtained for zero bias voltage and is in good agreement with the BTK results (see Fig.4.25(d)).

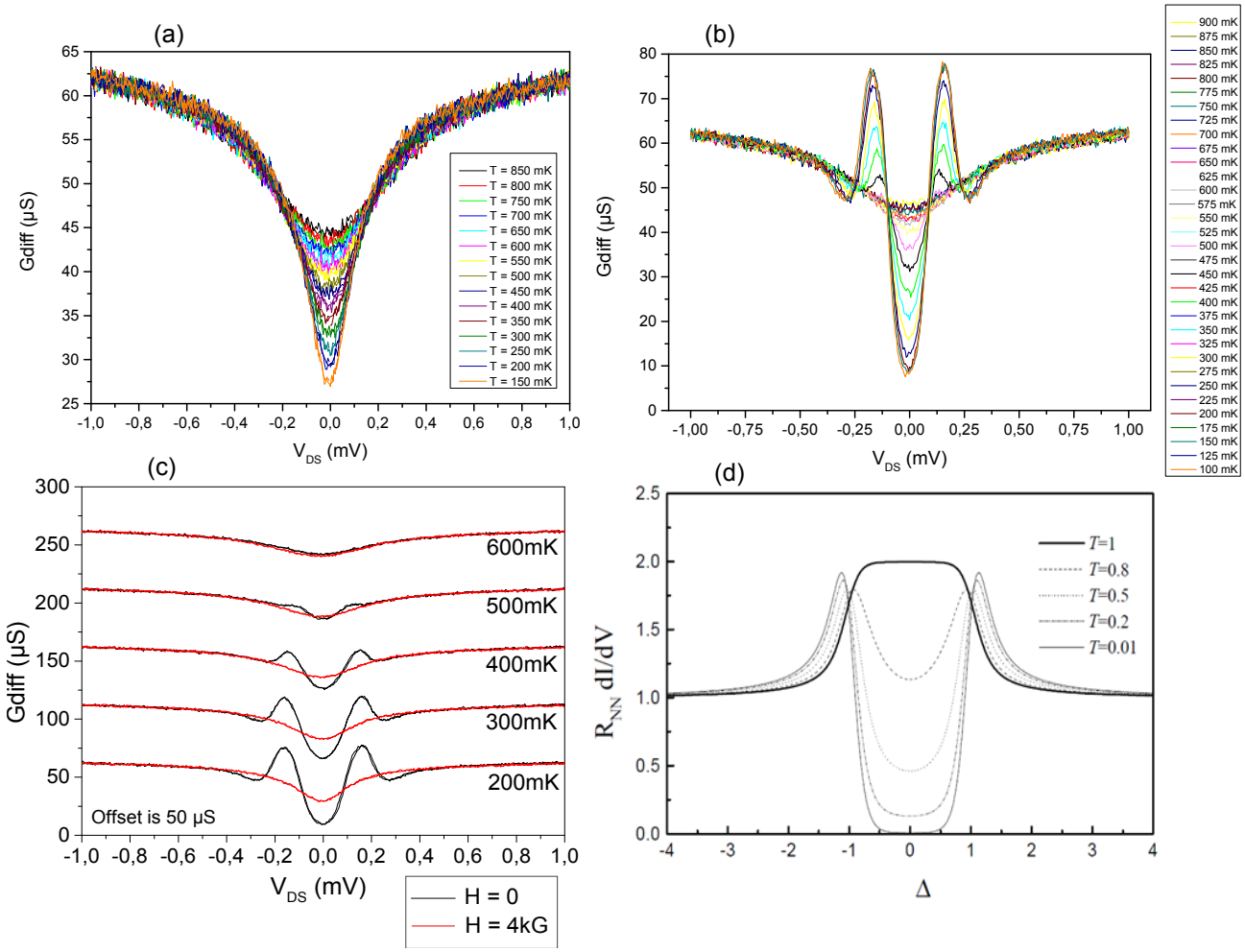


Figure 4.25: (a) Temperature dependence of the induced gap with an applied external magnetic field of 4kG (b) Temperature dependence of the induced gap with no external magnetic field (c) Magnetic field and temperature dependence of the induced gap. An offset of 50μS has been applied between the curves for different temperatures (d) Differential conductance as a function of the bias voltage, in the BTK framework, for different barrier transparency T. For an ideal transparent barrier (T=1), under the gap Δ, the Andreev reflection is the dominant mechanism and thus, we observe a doubled conductance corresponding to the Cooper pairs transport. In order to get a normal state conductance, we need to apply a source/drain voltage larger than $2\Delta/e$. As the barrier transparency decreases, the Andreev reflection is less and less made possible, leading to a lower conductance under the gap until it vanishes.

Conclusion

We have characterized the electric transport properties of our PtSi based silicon Sb-MOSFET and we have also achieved measuring evidence of superconductivity via the presence of a superconducting induced gap in our device. This gap matches with the BCS

theory for the temperature dependence but is slightly weakened. The disappearance of the induced gap in the measured differential conductance when applying a strong magnetic field of 4kG compellingly confirms the superconductivity in the PtSi based SbMOSFET. Moreover, the presence of a finite conductance at very low temperature for zero bias voltage supports the idea of a Schottky barrier interface with a moderate quality and transparency which has been estimated.

PtSi based silicon MOSFET appears to be a promising candidate for allowing a supercurrent to tunnel through the device. That is the reason why the improvement of the barrier interface quality is necessary. One of the first requirements would be to have a better control of the salicidation during the SbMOSFET fabrication process. Another perspective would be to use a different silicide with high critical temperatures such as $CoSi_2$ [74] or V_3Si [79], [80], [81], [82]. Finally, using superconducting highly boron-doped silicon for the source and drain contacts and adding on top the superconducting silicide may be the ideal choice for our contacts. Combining the superconducting properties of these two materials could strengthen the resulting superconductivity in a first place and secondly, the choice of these materials could enhance the quality of the interface with the semiconductor channel.

Conclusion and Perspectives

During this thesis, I have studied superconducting transport through silicon MOSFET and investigated two main roads to introduce superconductivity in our nanodevices. The major goal was to realize a JOFET in a MOSFET geometry, including superconducting materials compatible with the highly mature and reproducible CMOS technology. Importantly, it is worth mentioning that the experimental work conducted in the course of this thesis is of highly explorative character.

On the first part, I have extended the work of Audrey Grockowiak on superconducting boron-doped silicon layers. The difficult challenge was to adapt the laser doping techniques used to make superconducting silicon to SOI, the basic building block of some transistors. I first have recovered the previous results obtained on bulk silicon and then, I have successfully fabricated superconducting boron-doped SOI with the two doping methods at Orsay. This has been confirmed by XRD measurements. Moreover, I have elaborated two full superconducting SOI devices, a SQUID and a Hall bar. The work on superconducting SOI:B has to be continued, especially for the PLIE technique, to be able to determine with precision the most suitable preimplantation dose and also the most promising range of laser energy densities to consider, in order to bring superconductivity.

On the second part, I have studied superconducting silicides, in particular PtSi, which is compatible with the CMOS technology. I have investigated several aspects of the low temperature transport in nanoscale FDSOI- Schottky barrier MOSFETs with superconducting PtSi source and drain fabricated at LETI. At very low temperature, I have evidenced superconductivity in the PtSi based silicon SbMOSFET due to the measurement of the PtSi induced gap in the device. I have also revealed the presence of a finite conductance for zero bias voltage, leading to a Schottky barrier with moderate transparency, that I have estimated. Moreover, the interplay between the two antagonistic phenomena of superconductivity and Coulomb blockade has been manifested itself via the presence of a small dip close to the coherence peaks in the differential conductance at low temperature, which is not ordinarily noticeable for traditional SN interface.

It is however important to keep in mind that the nanodevices used in this research were in fact originally conceived for an entirely different purpose, and have now for the first time been studied in the context of quantum transport. To improve the results for future studies, it is imperative to conceive new device designs, which are able to capture the parameter regime in which the sought-after effects can occur. In particular, in order to capture true

transmon/gatemon physics, the tunneling interface needs to be made more transparent. Two future directions are worth considering: firstly, the superconducting PtSi silicide could be replaced by other silicides, such as V_3Si or $CoSi_2$, both of which are CMOS compatible and very interesting due to their high critical temperatures. This could probably offer interface of higher quality. Secondly, the idea to combine both superconducting PtSi and superconducting silicon to realize the source and drain contacts of a transistor is certainly very challenging but could also strenghten superconductivity and open doors towards a gatemon by offering interface of higher transparency.

Appendix A

```
close all
clear

%% V plotted against I for different values of Q

Imax = 2000*10^(-9);

x = 0:2000;
Itab = zeros(length(x),1);

for idx = 1:2001
    Itab(idx)= -Imax+x(idx)*Imax / 500;
end

for idx= 1001:2001
    Itab(idx)=Imax-(x(idx)-1000)*Imax / 500;
end

nmax = 10^(6);
nlast = nmax/10;
delta = 0.001;


h = 6.63*10^(-34);
e = 1.6*10^(-19);
hb = h/(2*pi);
C = 10^(-13);

Ic = 300*10^(-9);

wp=sqrt(2*e*Ic/ (hb*C)) ;

Q = [0.3,0.5,1,2];

colors = {'b','r','g','k'};
```

```
for k = 1:length(Q)

    phin = 0;
    phinp1 = 0;

    voltage = zeros(length(x),1);

    for idx = 1:2001


        Inorm = Itab(idx)/Ic;
        total = 0;
        ntotal = 0;
        average = 0;

        for i = 1:nmax
            phinm1=phin ;
            phin=phinp1;
            phinp1=(Inorm-sin(phin))*delta*delta-(1/Q(k))*(phin-phinm1)...
                delta+2*phin-phinm1;

            if i>nmax-nlast
                average =  (average*ntotal + (phin-phinm1)/(delta))/...
                    (ntotal+1) ;
                ntotal = ntotal+1;
            end
        end

        voltage(idx) = wp* average*hb/(2*e) ;
    end


    if k == 1
        figure,
    end
```

```
    plot(Itab*10^(9),voltage*10^3,'linewidth',2,'color',colors{k})
    xlim([-0.4,0.4]*10^(-6)*10^(9))
    ylim([-1,1]*10^(-4)*10^(3))
    ylabel('V (mV)','fontname','times','fontsize',15)
    xlabel('I (nA)','fontname','times','fontsize',15)
    set(gca,'fontname','times','fontsize',15)
    set(gcf,'color','white')
    hold on

end

legend('Q = 0.3', 'Q = 0.5', 'Q = 1','Q = 2','location','northwest')



%% U plotted against phi for different values of I

phi = 0:0.01:35;
U = zeros(length(phi),1);

colors = {'b','k','cyan','r','g'};

I = [0,0.3,0.5,0.8,2].*Ic;

figure,
for i = 1:length(I)
    for idx = 1:length(phi)
        U(idx) = -hb*Ic/(2*e)*cos(phi(idx))-hb*I(i)/(2*e)*phi(idx);
    end
    plot(phi,U,colors{i},'linewidth',2)
    hold on
end

legend('I = 0','I = 0.3 Ic','I = 0.5 Ic','I = 0.8 Ic','I = 2 Ic',...
    'location','southwest')
ylabel('U','fontname','times','fontsize',15)
xlabel('\Phi','fontname','times','fontsize',15)
set(gca,'fontname','times','fontsize',15)
set(gcf,'color','white')

%% Ic/Ic_0 plotted against Phi/Phi_0

phi_ext_over_phi0 =linspace(0,3,10000);

IoverIC = zeros(length(phi_ext_over_phi0),1);
```

```
for idx = 1:length(phi_ext_over_phi0)
    IoverIC(idx) =2*abs(cos(pi*phi_ext_over_phi0(idx)))/Ic;
end

figure, plot(phi_ext_over_phi0,Ic*IoverIC,'linewidth',2)
ylim([0,3])
ylabel('Ic / Ic_{0}','fontname','times','fontsize',15)
xlabel('\Phi / \Phi_{0}','fontname','times','fontsize',15)
set(gca,'fontname','times','fontsize',15)
set(gcf,'color','white')
```

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