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# Modelling, characterisation and optimization of substrate losses in RF switch IC design for WLAN applications

Fadoua Gacim

► **To cite this version:**

Fadoua Gacim. Modelling, characterisation and optimization of substrate losses in RF switch IC design for WLAN applications. Electromagnetism. Normandie Université, 2017. English. NNT : 2017NORMC268 . tel-01743712

**HAL Id: tel-01743712**

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Normandie Université

**THESE**

**Pour obtenir le diplôme de doctorat**

**Spécialité Electronique, Microélectronique, Optique et Lasers, Optoélectroniques,  
Microondes**

**Préparée au sein de l'ENSICAEN et de l'UNICAEN**

**Modelling, Characterisation and optimization of substrate losses  
in RF switch IC design for WLAN application**

**Présentée et soutenue  
par  
Fadoua GACIM**

**Thèse soutenue publiquement le (19 Décembre 2017)  
devant le jury composé de**

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# Acknowledgements

During my PhD work I met wonderful people who gave real fundamental contributions to my personal and professional growth. I do not know if I will be able to really thank all of them.

This CIFRE thesis was realized through a collaboration between NXP Semiconductors-Caen and the University of Caen Normandy.

First of all, my special and deep appreciation is for my advisor at NXP, Dr-HDR Olivier Tesson. For his continuous support of my PhD study and related research. For his patience, motivation, and immense knowledge. For all the time of research reviewing this thesis and almost all the papers I published, I owe him immense gratitude.

Beside my supervisor I would like to thank my co-advisor at NXP, Mrs. Nathalie Jourdan for advices she gave me with her always optimistic attitude, always believing in my abilities. Many thanks to Prof. Philippe Descamps, my supervisor from the University of Caen Normandy, for the many advices and recommendations he gave me. And also his administrative efforts to ensure that the defense took place in a satisfactory manner.

I would like to thank Prof. Jean-Baptiste Begueret and Dr-HDR Emeric de Foucault who have kindly reported this thesis and gave their favorable opinion so that I can defend my work and obtain the title of Doctor of the University of Caen. I also thank all the members of my jury who agreed to give some of their time to take an interest in my work. Dr-HDR Patrice Gamand, Prof. dr. ir. Domine Leenaerts and Hans van Walderveen for their valuable comments, recommendations and careful review of my manuscript.

I would to express my deep gratitude to Mrs. Dominique Lohy manager of the PDK team in NXP-Caen, who was able to make this CIFRE thesis possible in a cross collaboration between the PDK team and the design team (BL-SAS). She made me feel very welcome in the team and has been a source of love and energy ever since.

Special thanks for the people who helped me technically. A big thank to Hans van Walderveen from NXP-Eindhoven, Dr.ir. Peter Magnée from NXP-Nijmegen, Dr. Cristian Andrei from NXP-Caen, Sylvie Parmantier from Cadence, Dr-HDR Sidina Wane and of course Dr-HDR Olivier Tesson from SAS-Caen.

Many thanks to Dominique Lesenechal for his help to make all my measurements possible. I would like to also thank Samuel Mabire and Olivier Minchin for helping me in ‘tool-fighting’. Mrs. Carole Aubey and Melina for their efficiency and kindness, many things could not have been done without their interventions.

I also would like to thank Cees van Dinther and ir Michel Groenewegen for having received me in the SAS team at NXP-Nijmegen. Many thanks to ir Michel Groenewegen who took the time and made a special trip to be present at my thesis defense.

In my daily work I have been blessed with a friendly and cheerful group, Dominique Lohy, Nathalie Jourdan, Didier Leroux, Jean-Francois Aupee, Sylvie-anne Leverd, Jean-Yves Queignec, Christophe Lecoutre, Didier Depreeuw, Hubert Furdyna, Christele Biard and Emmanuel Grenados. Thank you for all your support and good cheers! I love you all and I could not express in a few lines my gratitude for you.

Thanks to my supervisor of my final year internship Manohiana Ranaivoniarivo who provided me an opportunity to join her team as intern at NXP Semiconductors.

I finish with the most basic source of my life energy: my family, my parents: mom Hasna Hammouka and dad Jilali GACIM. My brother Salah-Eddine, my sister Safaa and my little nephew Adam. I have an amazing family; their support has been unconditional all these years; they have given up many things for me; they have cherished with me every great moment and supported me whenever I needed it. And I want to thank them now: MERCI!!!

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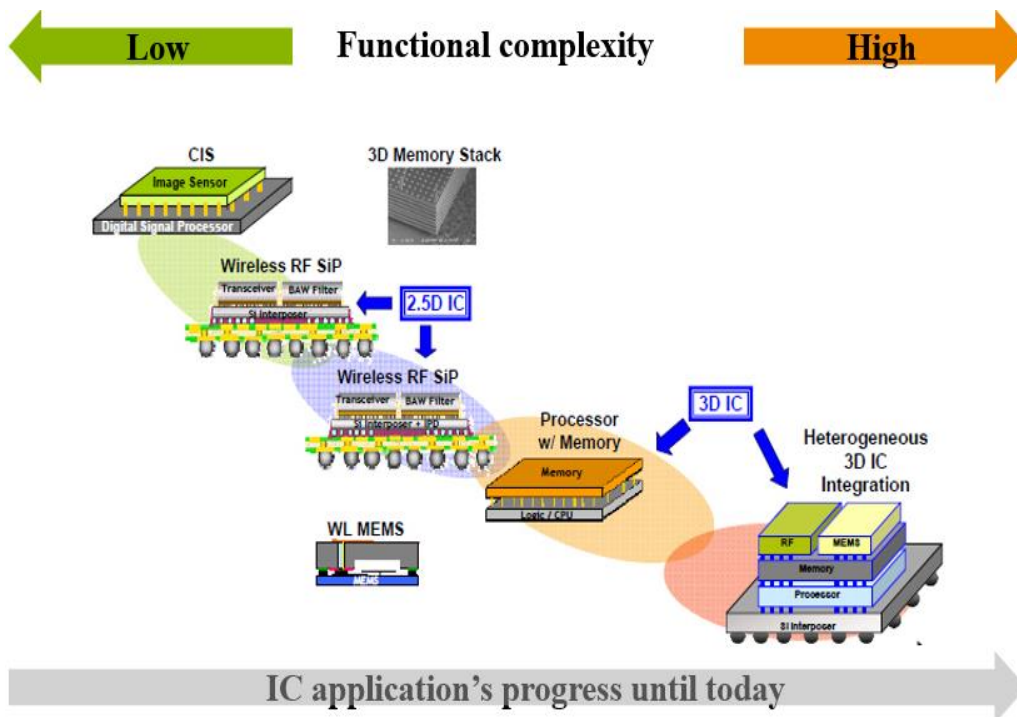
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## General Introduction

The evolution and the development of high performance wireless communication systems like the cellular system, Bluetooth, the wireless local area network (WLAN), etc., involve ever-increasing complex Radio Frequency Integrated Circuits (RFICs) to support this growth.

The wireless revolution where different devices are connected simultaneously makes it possible to communicate anywhere at any time. Recent developments in wireless networking using different standards exhibit several challenges. The most critical challenges are: Low cost/Low power/High integration in a small form factor for RF functions and Multi-mode/Multi-band operations. In addition, the decreased feature size of the integration technologies leads to higher complexity as it is required for highly integrated transceivers for mobile communication and wireless networking. This requires choosing an optimized technology as well as the development of new design strategies.



*Figure 1.1. IC application's road map*

For high-frequency and high-power integrated solutions, a good choice of semiconductor substrate technology can provide a strategic advantage by achieving better performance without additional design cost. A material such as gallium arsenide (GaAs) has traditionally been the substrate of choice for RF applications [1-12]. However, the large scale of commercial RF applications requires a substrate that is low cost, like silicon, and also present low losses.

Due to the high operating speed of state-of-the-art bipolar transistors, combined with high-density CMOS in BiCMOS technologies (for example BiCMOS- from NXP), it becomes possible to realize integrated circuits for very challenging applications.

RF circuit designs have tight requirements on power consumption and noise figure (NF). The accuracy of circuit simulation and its related predictability is very crucial in meeting those

requirements. This is highly linked to the accuracy of the models with their intrinsic and extrinsic effects. Therefore, for successful design of such circuits, it is mandatory to consider accurately parasitic effects, including the influence of the substrate, as early as possible during circuit design to reduce the number of design iterations and thus reduce ‘time to market’.

The substrate impedance is therefore an important extrinsic element in the performance of the circuits. It then needs to be accurately modelled for predictable simulations.

This thesis deals with substrate characterization and optimization in RFIC’s, and the development of an efficient methodology for parasitic extraction of inhomogeneous substrates, offering a challenging trade-off between required accuracy and fast simulation.

The interest in developing a substrate extraction technique is twofold. First, it will allow a deeper physical understanding of the different coupling mechanisms in the silicon substrate. Secondly, in addition to the development of reduction techniques of the substrate effect, it is important to define simple and fast simulation methods to handle the substrate coupling effects in complex circuits.

### **This manuscript consists of the following chapters:**

**Chapter 1** presents the context and state of the art of coupling effects in Integrated Circuits, to define clearly the circuit environment, and to initiate discussions on the root cause of the mismatch between measurements and simulation. This is key to identify the areas that should be explored in more detail. The purpose of chapter 1 is to give a global background of modelling techniques and the position of this thesis in that context.

**Chapter 2** presents the predictable substrate modelling technique that has been developed in this PhD program. The accuracy and sensitivity of the proposed methodology have been verified on a single test case with different layout variants of Deep Trench Isolation. From measurements analysis, we will be able to get more knowledge about isolation strategy (especially in relation to DTI).

**Chapter 3** focuses on the role of substrate isolation techniques on nMOS switch performances, Design recommendations on isolation techniques (from a layout point of view) at device level are also presented in this chapter. The proposed method has been validated using measurement results and EM simulations (both 2.5D and 3D FEM) for accuracy and flow usability.

**Chapter 4** will propose the ad-hoc approach one step further considering a full IP (SP2T and SP8T circuits) This IP has been developed in-house using an NXP BiCMOS technology. RF measurements are presented to support theoretical investigations. A comparison between simulations and experimental data is also presented and discussed in view of the criteria accuracy and development-time.

**Chapter 5** demonstrates how to use the proposed methodology in the development of a full SP3T switch embedded in a commercial product for WLAN related applications. This switch will be described in detail in this chapter. It includes the series and parallel switches but also the ESD protection (which are known to couple with the substrate and thus leading to additional losses). A bias block together with a decoder are also included in this topology. In this chapter, challenges

related to database partitioning will be presented. We will highlight the way we have succeeded to solve these issues by adopting a new methodology. Results are then compared to both measurements and the prior methodology.

Finally, we will draw some conclusions inherent to the methodology itself and the way we can also minimize losses related to substrate coupling. Layout recommendations will be provided based on the available data.



# Chapter I: Context and state of the art of modelling techniques for RFIC's

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## **Introduction**

Chapter I presents the motivation and the objective of the thesis. This chapter is organized as follows: The first section describes the main parasitic effects in Integrated Circuits. The physical behaviour of the silicon and the contribution of the substrate losses are highlighted. In the second section, we discuss the modelling techniques with the advantages and limitations of each approach. The third section presents the predictive methodology proposed in this thesis. The mechanism and the implementation in NXP of this methodology in the design flow are described. The fourth section presents the design consideration in Front End Integrated Circuits. Then we will discuss the thesis motivation and the challenges to meet. Finally, the last paragraph concludes this chapter.

## I.1. Types of parasitic coupling in Integrated Circuits

In the introduction of this book it is shown how trends towards greater complexity, increasing performance and reducing size makes the timely prediction of coupling mechanisms more and more important. In-circuit disturbances, can limit the circuit performance, so they should be considered in all stages of the design process. The main mechanisms of electric coupling in IC's are presented in the following paragraph. More generally, there are thousands of couplings in IC's, but most of them compensate each other. In the following parts of this section we will discuss main coupling contributors and the way they can be anticipated at design phase (extraction).

### I.1.1. Crosstalk effects in integrated circuits

Crosstalk can be defined, as an unwanted interference caused by the electric and magnetic fields of one circuit (aggressor) affecting another one (victim) [I-23]. From this general definition, it can be deduced that any mechanism that creates such type of interference falls into the crosstalk definition. In the case of high-frequency ICs, coupling through the substrate – the so-called substrate crosstalk – is one of the main sources of interference. It is recognized as one of the most limiting factors in the performance of RF ICs [I-16] [I-17]. Many techniques have been developed to reduce this loss of performance, one of the possibility is to use a (so-called) less lossy substrate like: GaAs, Silicon-On-Isolator (SOI), Silicon-On-Sapphire (SOS), high-resistive silicon (HRS), Glass, quartz, or to etch the substrate away under the device (macro mechanical system - MEMS) [I-49]. But the mechanical stability, process ability and packaging of such structures should be taken in consideration.

Better electrical characteristics than using normal Si substrate can be achieved by applying glass or quartz substrates, but one of the major difficulties is the low thermal conductivity of these materials that may severely limit the maximum dissipated power of the package. SOS combines several of the benefits in term of cross talk reduction and thermal conductivity, but it has a poor mechanical stability, which, is excellent for bulk silicon [I-50].

To address these issues more favourably, other materials that have a higher thermal conductivity and allow for high-density through-wafer interconnects should be considered. High-resistive silicon meets most of these requirements.

Crosstalk in silicon substrates is caused by three different mechanisms: injection into the substrate, the propagation of the noise signal through the substrate and the sensitivity of an adjacent circuit to pick up this noise signal. Various isolation strategies which are layout dependent have been made to reduce crosstalk. In general, crosstalk reduction strategies fall into two different categories: One is to attempt to block crosstalk signals and the other is to drain the crosstalk signal to ground.

Crosstalk is expressed in dB as follows:

$$Crosstalk (dB) = 20 \log\left(\frac{coupled\ voltage\ at\ receiver}{signal\ voltage\ in\ source}\right) \quad (I-1)$$

In integrated circuits, there are generally: electric field coupling, magnetic field coupling and substrate coupling.

### Electric field coupling:

This kind of coupling occurs when electric field lines originate from one conductor and terminate to another. This can be represented schematically by a parasitic capacitance between two conductors. This capacitive coupling (or electric field coupling) between interconnect (isolated by oxide), has been studied in [I-18], [I-10]. The electric field coupling induces a current in the victim conductor (or circuit) that is proportional to the time derivative of the source signal ( $i = C \cdot dV/dt$ ). The larger the capacitance the larger the coupling, which means it increases for closer, longer interconnects and increases with frequency.

In modern technologies the lateral (intra-layer) dimensions are smaller than the vertical (inter-layer) dimensions. Therefore the lateral capacitances are dominant over the vertical capacitances (Figure I.2).

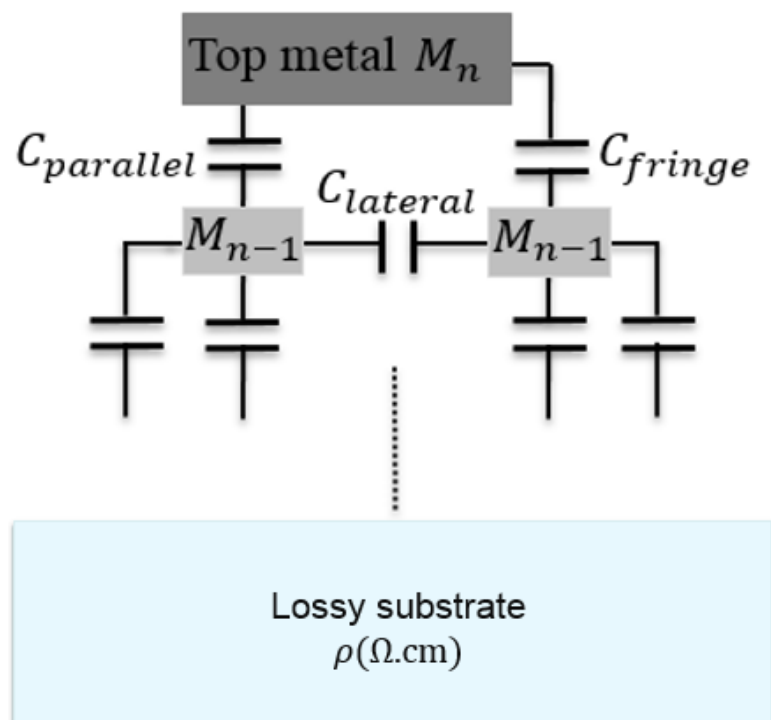


Figure I. 2. Capacitive coupling between wires in a multi-layered interconnect system

### Magnetic field coupling:

Magnetic field coupling or inductive coupling can also be a significant source of crosstalk in Integrated Circuits.

A magnetic field induces a current and its variation generates a voltage in the victim device (or circuit) that is proportional to the derivative of the signal current in the source device (or circuit) [I-18] ( $V = L \cdot di/dt$ )

#### I.1.2. Passive elements and metal losses

Passive elements include resistors, capacitors and inductors. In BiCMOS technology, resistors and most capacitors are library components and the available modelling is accurate. When

frequency is increasing, modelling is of particular importance as series resistance and inductance can jeopardize capacitor performance. This requires a proper extraction strategy. Inductors are critical components that need to be accurately modelled and optimized for their particular purpose in the design. The right trade-off between Q-factor and chip area is crucial for chip performance and having the smallest area. When current flows through a spiral, a magnetic field that penetrates the substrate induces eddy currents which flow in the opposite direction (Lenz' Law). This results in a severe loss of the quality factor (Q) of the inductor. If the substrate is sufficiently resistive ( $\sim \text{Ohm}\cdot\text{cm}$ ), this type of loss is small.

The substrate loss consists of two parts: finite resistance due to electrically induced conductive and displacement currents, and magnetically induced eddy current resistance. These losses are known as capacitive and magnetic, respectively.

One of the difficulties in designing integrated RF circuits is the low Q-factor of on-chip inductors and transmission lines. This is mainly due to the mentioned eddy current in the substrate and the DC resistance of the inductor wires.

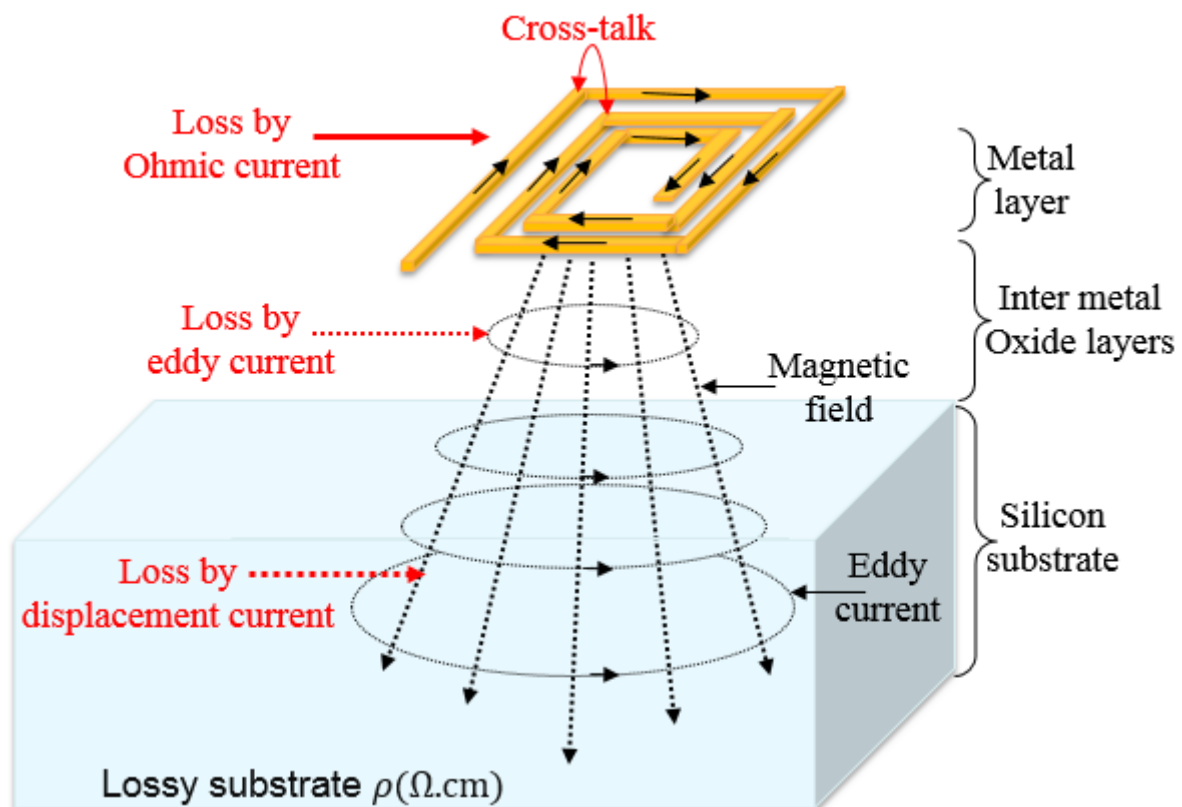


Figure I. 3. Integrated coil related losses

To reduce electromagnetic (EM) couplings and to improve the Q-factor of on-chip inductors, different strategies in [I-6] are applied. These strategies are all targeted at improving the inductor's intrinsic resistance (by using a thick metal layer or stacked inductors...), modifying its architecture, optimizing the substrate stack (removing low-Ohmic buried layers, using Deep Trench Isolation [I-22]), or using a metal shield to decrease the vertical electric field penetrating into the substrate. These include metal ground shield (MGS), polysilicon ground shield (PGS) and n+ ground shield (NGS) [I-39]. Solid ground shields result in a very large capacitance between the trace and the

ground plane, in a lower inductance and SRF (self-resonance frequency). Therefore, a patterned shield (Figure I.4) provides isolation from the substrate and thus no eddy currents will be induced in the substrate, which leads to an improvement of the Q-factor. However, that can reduce the SRF.

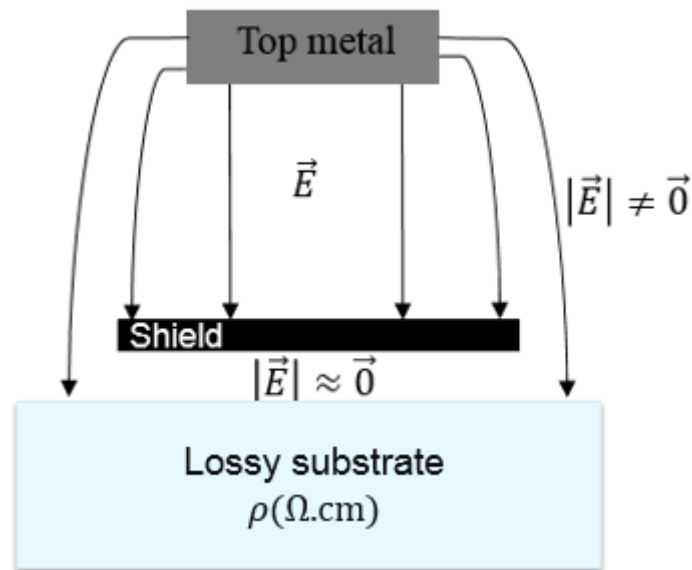


Figure I. 4. Electrical field suppression using MGS or PGS

Another technique is based on the use of a Via-hole connection and a Faraday cage (Figure I.5) to shield it from high frequency paths[I-51].

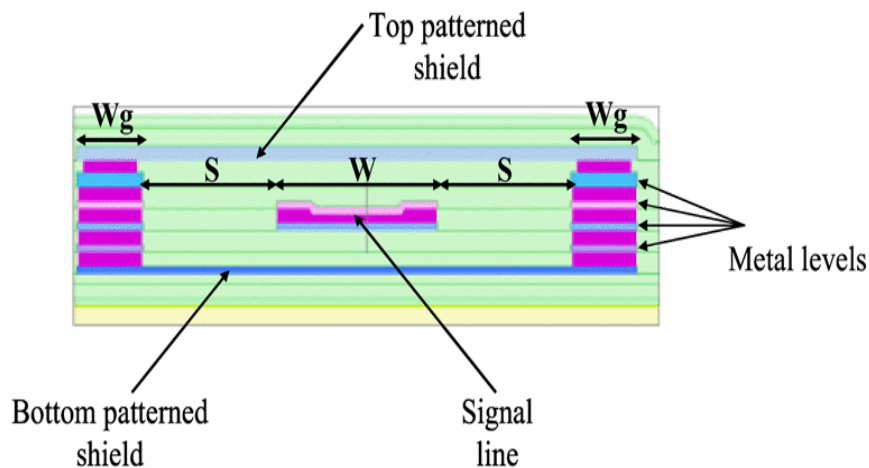


Figure I. 5. Cross section representation of Iline configuration embedded in a metal cage

This technique offers a higher density of integration and allows proper grounding connection leading to a higher flexibility of routing. Although this technique is applicable to SiP application using TSV (Through Silicon Via). However, it can include spurious resonant modes, and requires properly designed grounding strategies to avoid floating configurations.

### I.1.3. Substrate effects in integrated circuits:

Substrate coupling in IC's is the process whereby a parasitic current flow in the substrate creates an electrical coupling between devices and/or circuits due to the presence of conductive and capacitive paths in the silicon substrate.

Current is injected into the substrate through various mechanisms. Physically large passive devices such as inductors, capacitors, interconnect and bond-pads inject displacement current in the substrate. These currents flow vertically and horizontally to points of low potential in the substrate, such as substrate taps and the back-plane. These currents couple to other large passive structures in a similar manner [I-19].

Active devices also inject current into the substrate. For this reason, a lot of effort has been put into isolating active devices from the substrate by either reverse-biased PN junctions, Faraday cage, SOI or other isolation techniques [I-40] [I-41] [I-42] [I-43].

The current can also be injected into the substrate by means of the hot electron effect. In a short-channel MOS transistor, for instance. There the electron-hole pair mechanism takes place in the high-field pinch-off region near the drain due to collisions. The electric field lines lead one set of the carriers into the substrate.

Another mechanism, by which parasitic currents can be injected into the substrate, is capacitive coupling. This can be caused by the interaction of bipolar NPN transistors and the substrate through the N-type collector (BN) to the n/p-substrate junction. This capacitive coupling can also be caused by a MOS transistor through the source-substrate and drain-substrate junction capacitances. Figure 1.6 summarizes the capacitive coupling mechanisms.

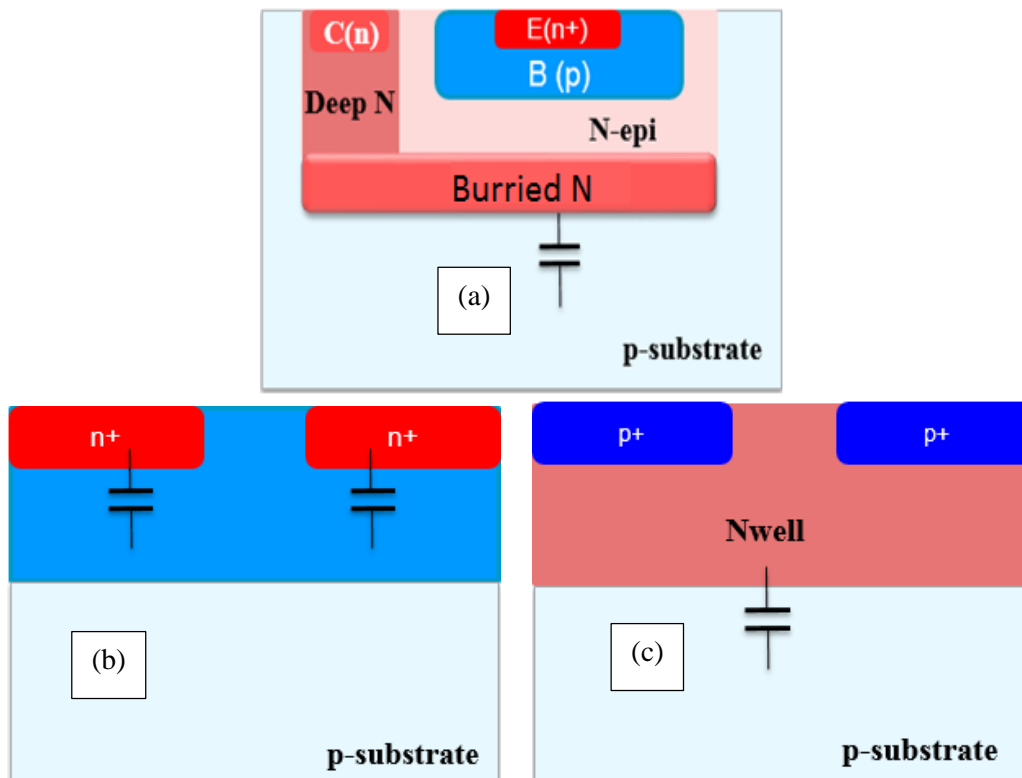


Figure 1.6 Capacitive coupling to the substrate through PN junction: (a) in NPN transistor (b) in nMOS transistor, (c) in pMOS transistor

Those capacitances give a path for the current to propagate into the substrate. Its values depend on the doping profile levels as well as the bias level.

Furthermore, in an integrated circuit, the coupling between different portions of the chip can be very problematic. Although careful layout techniques and isolation strategies can minimize them, these effects can never be eliminated or ignored in ICs. Substrate coupling is treated extensively in [I-23].

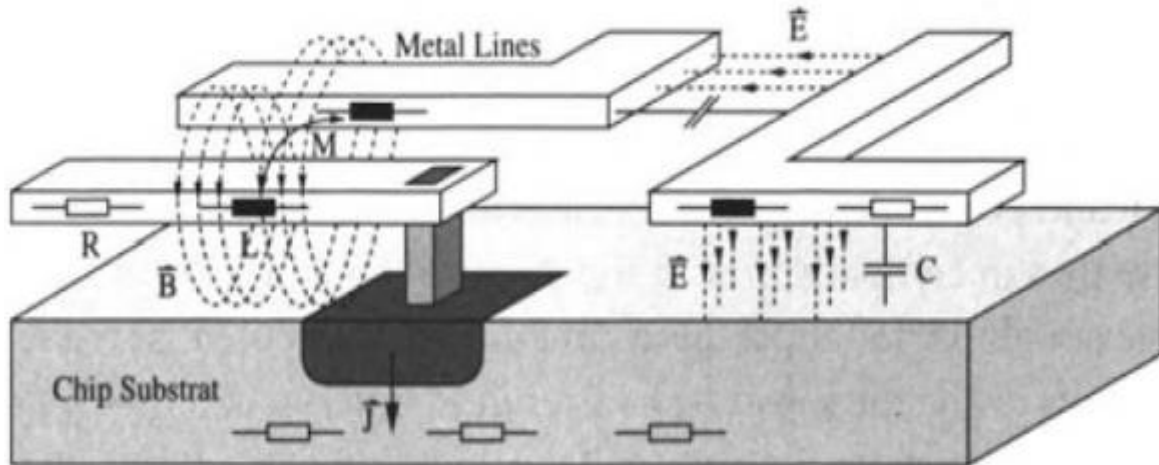


Figure I. 7 Parasitic effect to be considered during design simulation

The substrate is a major source of loss and limitation of high-frequency signals, which is a direct consequence of the conductive nature of Si as opposed to the insulating nature of GaAs. The Si substrate resistivity varies from some  $k\Omega\cdot\text{cm}$  for lightly doped Si to few  $m\Omega\cdot\text{cm}$  for heavily doped Si.

The Si-substrate influences the behaviour of the integrated circuit design in a negative manner. The capacitance between interconnect (wires) and the substrate delays the signal through the interconnection. The current flowing to ground through the substrate causes a voltage drop, which affects the device operation in a negative manner. In addition, the substrate is not a perfect isolation between devices, leading to unwanted “cross-talk” through the substrate. Figure 1.7 illustrates coupling phenomena to be considered in addition.

In fact, to tackle these substrates induced losses, some papers [I-56] already propose different isolation techniques.

In this thesis, we develop a predictable modelling methodology which can handle accurately the considered isolation technique by the designer and thus help on the minimization of the substrate related losses.

- **Substrate physical equivalent model:**

It is essential to know how the signal propagates from one device to another or from one circuit to another. Therefore, it is necessary to understand the mechanism and the physics of the substrate to be able to model accurately the substrate.

The current density for a silicon substrate with losses takes the expression [I-23]:



$$\vec{j} = (\sigma + j\omega\epsilon)\vec{E} \quad (I-2)$$

where  $j$  is the current density in the substrate ( $A/cm^2$ ),  $\sigma$  the conductivity,  $\epsilon$  the dielectric permittivity of the silicon,  $\omega$  the angular frequency and  $\vec{E}$  the electric field strength (V/cm). Ohm's law consists of a real part and an imaginary part, describing the conductive behaviour and capacitive behaviour, respectively.

- **Particular case regarding Silicon**

Silicon, as any semiconductor material, exhibits both conductive and dielectric characteristics, which can be translated into a resistive and a capacitive effect, respectively. Inside a doped semiconductor, the conductivity is given by:

$$\sigma = q(\mu_p p + \mu_n n) \quad (I-3)$$

Where  $q$  is the electron charge,  $\mu_n$  and  $\mu_p$  represent the mobility of the electrons and holes carriers, and  $n$  and  $p$  stand for the respective carrier densities. The  $\mu_n$  and  $\mu_p$  parameters vary as function of the total semiconductor doping and temperature.

At low frequencies, silicon can be considered as ohmic for signal below of the frequency  $f_c$  and the associated capacitive effect can be neglected. As the frequency increases, the capacitive effect rises to become equal to the resistive effect at the cut-off frequency defined by[I-36]:

$$\frac{1}{R_s} = \omega_c C_s = 2\pi f_c C_s ; f_c = \frac{q(\mu_p p + \mu_n n)}{2\pi\epsilon_0\epsilon_{rsi}} \quad (I-4)$$

Resistive effect:

The substrate can be modelled as mainly resistive for frequencies from DC up to a cut-off frequency [I-36], which is defined as:

$$f_c = \frac{1}{2\pi \rho_{sub} \epsilon_{sub}} \quad (I-5)$$

Where  $\rho_{sub}$  and  $\epsilon_{sub}$  are the resistivity and the permittivity of silicon, respectively.

In the case of the BiCMOS technology that is used to support this study, the resistivity of the substrate is 200  $\Omega\text{cm}$ . According to (I-5), the behaviour of the substrate is mainly resistive for frequencies up to 760 MHz.

Capacitive effect:

At frequencies above the cut-off frequency, the dielectric behaviour of the semiconductor can no longer be neglected, thus the substrate must be modelled as an RC (resistive and capacitive) network as shown in Figure I.8.

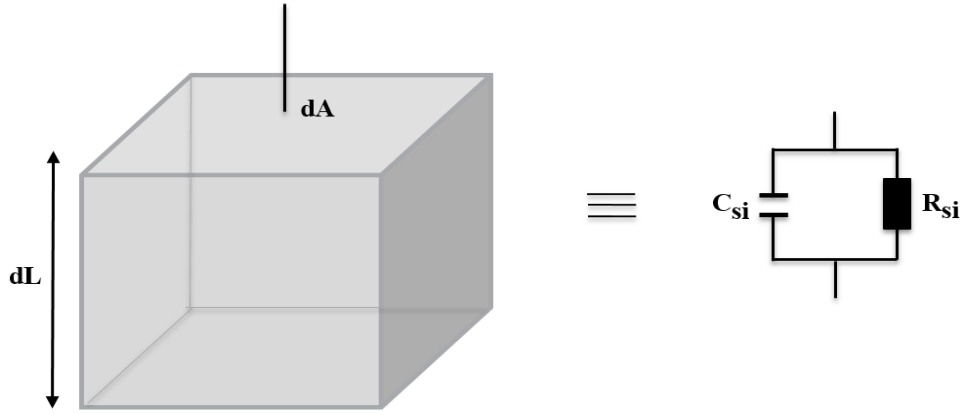


Figure I. 8. RC model of a piece of substrate

Figure I.9 represents the lumped element equivalent circuit used to describe the crosstalk effects between two devices in silicon substrate. The two capacitors and resistors  $C_{si}$ ,  $R_{si}$  represent the coupling effect between the bottom of each device and the back-side of the wafer [I-34] [I-35]. These capacitors and resistors are defined by:

$$R_{si} = \frac{t_{si}}{\sigma_{si}A_{device}} (\Omega) \quad , \quad C_{si} = \frac{\epsilon_0\epsilon_{rsi}A_{device}}{t_{si}} \quad (I-6)$$

With  $\epsilon_{rsi}$  and  $t_{si}$  being the permittivity and the thickness of the silicon, respectively, and  $A_{device}$  the area considered at terminals 1 and 2.

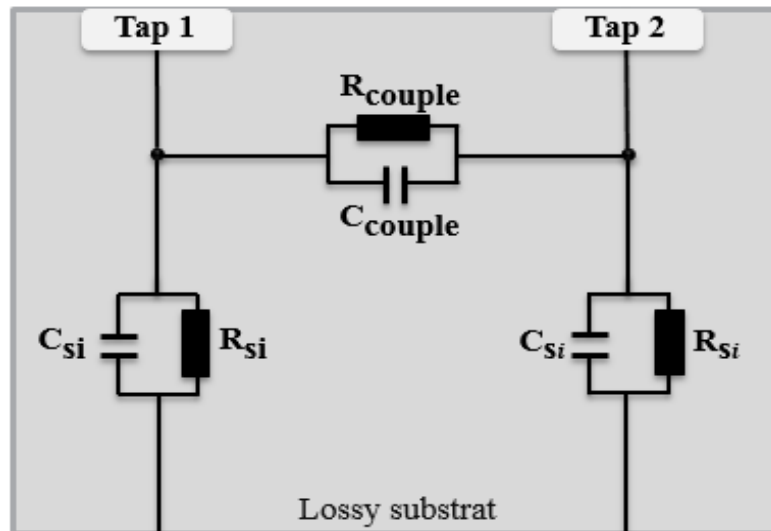


Figure I. 9. Lumped equivalent R-C model substrate crosstalk in the case of BiCMOS substrate

When two devices are close enough, a portion of the signal present at one device is transferred to the second device by coupling. This coupling effect is modelled by the parameters  $R_{couple}$  and  $C_{couple}$ .

## I.2. Circuit parasitic modelling

Parasitic effects are becoming more critical with increasing requirements on performance, density, complexity, and levels of integration in RFIC designs. For radio frequency (RF) designs, parasitic effects such as IC package pin leakage and substrate coupling are now widely seen. This leads to the need to model the parasitic networks in the areas of chip-package and substrate.

This section is organized as follows. A brief survey and the description of the various techniques used in resistance, capacitance and inductance extraction are presented. In terms of solution methods, both the domain methods that solve differential Maxwell equations such as finite difference (FD) [I-26] and finite element (FE) [I-24] methods, as well as integral equation approaches such as method of moments (MoM) [I-28] are discussed. From the accuracy standpoint, two-dimensional (2-D), quasi-3-D (or 2.5-D), 3-D, and quasi-static techniques are covered.

### I.2.1. RLCK extraction method

This technique is a quasi-static analysis performed by EDA commercial tools (Assura, Calibre, ...) design environments and is based on an approximate segmentation technique to compute quickly the couplings between interconnection of components. It is fast and accurate enough RF applications [I-2].

The tool extracts resistance (R), capacitance (C), self (L) and mutual (k) inductance parameter extractions as shown in figure 1-10.

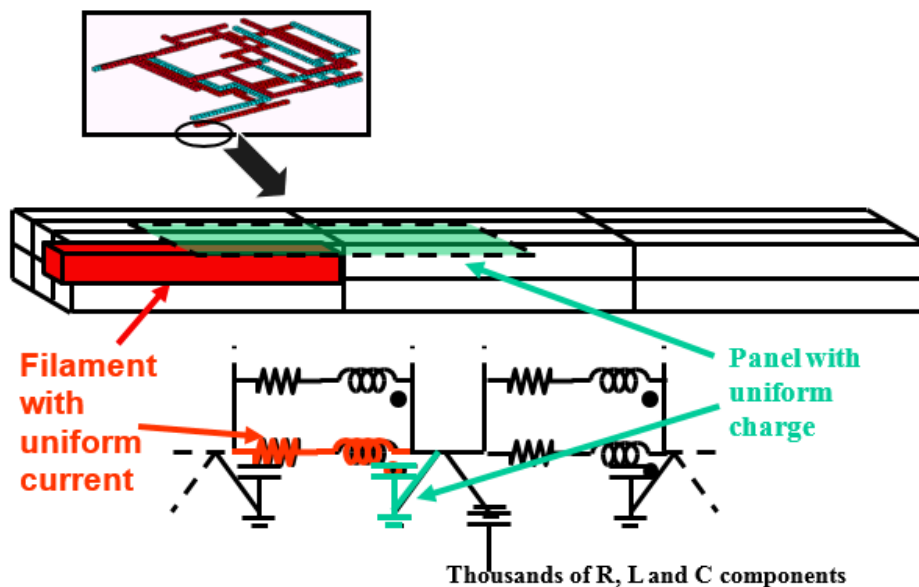


Figure I. 10. Illustrative multi-line conductors model extraction using PEX

This technique makes it possible to relate the RLCK model (parasitic netlist) with the intrinsic device implicitly, which leads to a simple post-layout simulation for the user. Also, time and frequency domain simulation are both possible. However, the real challenge with this technique is the local ground references and the return path of the inductive currents. All the substrate taps are assumed to be at the same potential. therefore, a near or a far substrate tap will be all shorted to

the same (global) ground. This model presents a limitation regarding the substrate behaviour and limits its use at backend interconnect parasitic.

### I.2.2. Compact model

In this method, components in design kit libraries are described by lumped element behavioural models, obtained from measurement and characterization for limited geometries and layout topologies. In addition, these models do not include the full substrate model and even if in the future will support the substrate network it will be strongly layout and technology dependent. Therefore, it is not able to give more freedom for designers. However, it is not possible to capture the substrate coupling effect between blocks [I-3]. The most well-known models available on the market are [I-52] [I-53] [I-54] [I-55]:

- MOS: PSP, bsim
- Bipolar: Mextram, HICUM
- Passive devices: TLIM, LSIM

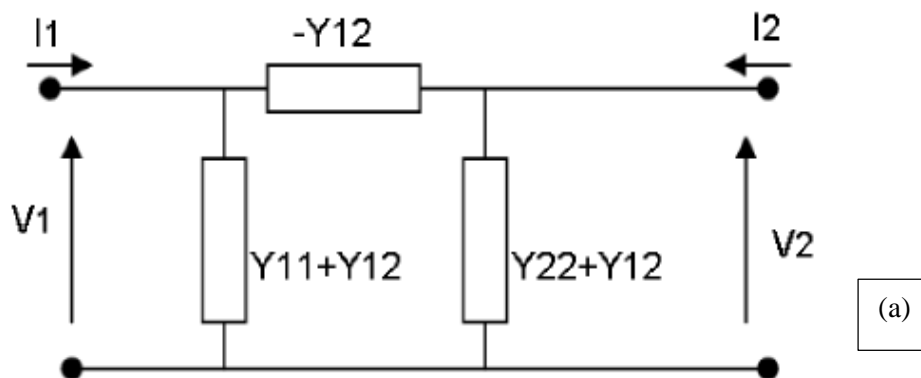
### I.2.3. Macro-modelling based techniques

In this part, we explore a methodology to extract, from EM simulation results and measurement data, equivalent circuits for passive circuits. This approach is oriented around fitting techniques to find the best matching models representations. Many efforts have been addressed to the macro-modelling approaches to reduce the complexity while maintaining an acceptable accuracy.

- **Extraction of equivalent Circuits for Passive Circuits (lumped-element model)**

An RLCG equivalent circuit is derived from Z or Y-parameters (Figure I.11). Y-parameters are convenient if we want to model our circuit under test with elements in a pi topology (one component across, and two in shunt). Z-parameters are convenient when we want to model the circuit with a T type of topology (two components in series with a shunt element between them) [I-31].

Each branch of the  $\pi$  or T equivalent topology is represented by an admittance or by an impedance, noted in  $Y_{parameters}$  or  $Z_{parameters}$  respectively. The series and parallel branches are composed of RLCG.



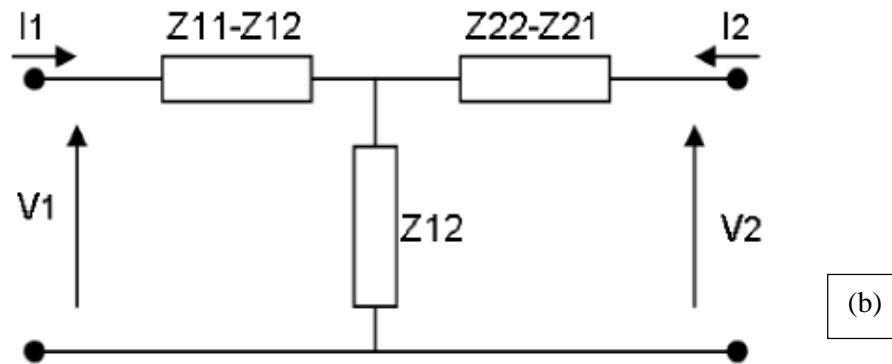


Figure I. 11. PI equivalent topology (a), and T equivalent topology (b)

This model is based on analytical calculations. It represents simply and physically the studied structure. Time domain analysis is also possible. However, it is narrow band and not accurate enough for more complex system. In addition, the difficulty is to find the appropriate equivalent model [I-4].

- **Black-Box (or S-parameters) model**

The Black-Box model contains the measured data or the EM simulated results in S-parameters. This model is frequency dependent. However, this model is only valid in the frequency domain and it presents some limitations in term of causality and time domain analysis. Also, it has some limitations regarding its ability to have predictive simulation.

#### I.2.4. Finite Element Method -FEM

Resolution by integral equations is only possible if the structure is homogeneous in the resolution area; the later means that  $\epsilon$  and  $\mu$  are constant. If  $\epsilon$  or  $\mu$  are variable, which corresponds to a non-homogeneous structure we must use a finite element formulation [I-24] [I-25].

The finite elements method (FEM) is widely used in mechanics. It was introduced by P. SILVESTER and MVK CHARI at the beginning of the seventies in the electromagnetic domain to solve non-homogeneous problems and complex geometries. The finite element method is generally applicable in the spectral domain. What is interesting in this method is its inherent capacity to account for non-homogeneous structures.

The first step of the Finite Element Method is to divide the space to be modelled into small elements or pieces of arbitrary shapes, which may be smaller where geometry details require it. In each element, it is assumed that the variation of the field quantity is simple (generally linear). The field is therefore described by a set of linear functions.

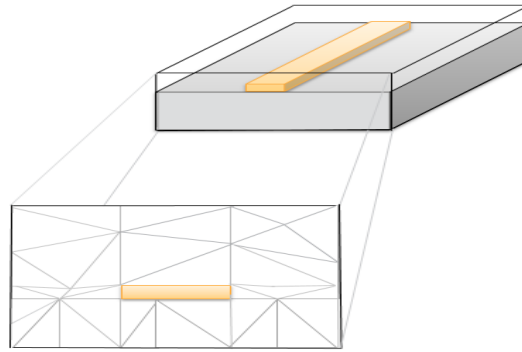


Figure I. 12. Finite Elements modelling example

Figure.I.12 shows an example of a finite element subdivision. The model contains information about geometry, material constants, excitations and boundary conditions. Each corner of an element is called a node. The goal of the finite element method is to determine the field at each node of the element:

$$[K]=[F][E]$$



The global system:

$$\begin{bmatrix} K_1 \\ \vdots \\ K_n \end{bmatrix} = \begin{bmatrix} F_{11} & \cdots & F_{1n} \\ \vdots & \ddots & \vdots \\ F_{n1} & \cdots & F_{nn} \end{bmatrix} \begin{bmatrix} E_1 \\ \vdots \\ E_n \end{bmatrix}$$

Where, E represents the unknown terms at each node which we are looking for, K represents the sources applied on the system. The F-matrix depends on boundary conditions and the geometry studied.

- **Advantages and disadvantages of the Finite Element Method-FEM**

The major advantage of the Finite Element Method over other methods is that in this method each element can have an electrical and geometrical characteristic independent of the other elements. This allows us to solve problems with many small elements in a complex geometry. Thus, it is possible to resolve complex geometrical cases having different properties relatively efficiently. The major disadvantage however of this method is the difficulty of modelling open systems (in the case where the field is unknown at any point of the study domain boundary). One of the big advantages of FEM is also because it includes a mesh algorithm based on refinement.

### I.2.5. Finite Differences Method in Time Domain-FDTD

The Finite difference method time domain (FDTD) [I-26] is a computational method using a grid based time domain numerical analysis for solving Maxwell's equations. The FDTD algorithm was first established by Yee as a three-dimensional solution of Maxwell's curl equations in 1966 [I-27].

The numerical resolution of Maxwell's equations by this method requires a Fine discretization spatio-temporal in squares or cubes with discretization steps  $\Delta x$ ,  $\Delta y$  and  $\Delta z$ . Space is thus divided into elementary parallelepipedal cells, within which the six electromagnetic field components (Ex,

$E_y$ ,  $E_z$  and  $H_x$ ,  $H_y$ ,  $H_z$ ) are calculated. The electric field is solved at a given instant, then the magnetic field is solved at the next instant (in time) and the procedure is repeated several times.

The method makes it possible to solve the Maxwell equations in time and space, by directly approximating the differential operations.

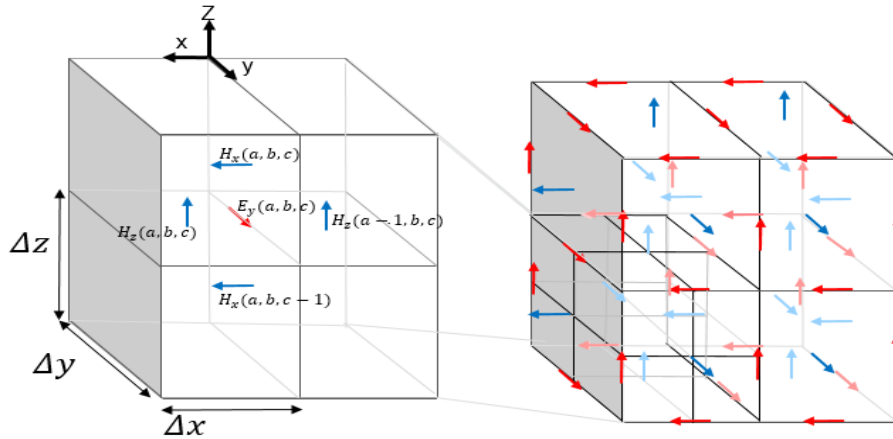


Figure I. 13. The Yee cell

• **Advantages and disadvantages of the Finite Differences Method in Time Domain-FDTD**

The main advantage of this method is that it allows a temporal resolution of the problem and therefore it allows to find the response of a wide frequency band in a single resolution. And its great flexibility to model electromagnetic problems with arbitrary signals propagating in complex configurations of conductors, dielectrics and lossy materials, nonlinear and anisotropic. It also makes it possible to obtain directly the E and H fields.

The major disadvantage however of this method is the compute time and memory requirements. The whole domain to be modelled must be subdivided into cubes and these cubes must be small, relative to the smallest wavelength. These cubes are all the smaller because the geometry is complex. To avoid the problems of dispersion and to obtain a wide frequency spectrum of radiation, it requires very small time steps. In addition, this method calculates only the propagated field; the other parameters such as current distribution are more difficult to calculate.

**I.2.6. Method of Moments-MoM**

The Method of Moment (MoM) [I-28] is a numerical technique aiming to solve Maxwell's equations in the frequency domain using their integral form. The electromagnetic field can then be expressed in the form of a surface integral. The decomposition of surface current into basic functions simplifies the resolution of the integral equations, which makes the method simple to implement [I-29] [I-30].

The method of moments (MOM) can be applied either in the spectral domain [I-44]-[I-45], or in the spatial domain [I-46]-[I-47]. The spatial domain approach has the advantage that, in this method, the integrands for the MoM matrix elements need to be evaluated only over the finite extension associated with the basis and testing functions, as opposed to over an infinite range required in its spectral domain counterpart [I-48]. In the conventional form of the spatial domain approach, the closed-form Green's function is involved.

In the case of the open-form Green's function (spectral domain), all dielectric layers are assumed to have infinite extension in the lateral plane. Therefore, it is not possible to have finite dielectric dimension. The fact that it is limited to homogenous layer stacks, decreases considerably the number of unknowns, and thus makes it possible to tackle complex geometry.

- **Advantages and disadvantages of the Method of Moments-MoM**

The method of moments has the advantage of modelling only the metallic structures and not all the surrounding space. Thus, it is best suited for modelling wires and homogenous structures. However, this method is more difficult to solve problems with dielectrics or inhomogeneous materials. MoM is a frequency domain method, so handling non-linear problems is impossible. Table 1.1 compares the different numerical methods.

*Table I. 1. Comparative table for different numerical methods*

| <b>Method</b>        | <b>Advantages</b>  | <b>Limitations</b>   |
|----------------------|--|--|
| <b>RLCk</b>          | <ul style="list-style-type: none"> <li>Integrated in the design flow</li> <li>Fast and easy to use</li> <li>Based on physical behaviour</li> </ul>   | <ul style="list-style-type: none"> <li>The substrate network</li> <li>Local substrate reference</li> </ul>   |
| <b>Macro-Model</b>   | <ul style="list-style-type: none"> <li>Fast simulation</li> <li>Simple and physical behavior</li> <li>Applicable at schematic level</li> </ul>   | <ul style="list-style-type: none"> <li>Difficult to find out the equivalent model</li> <li>Longer design iterations: based on measurements</li> <li>Not always reliable and not easily scalable</li> <li>Less parameters dependency (process, temperature, ...)</li> </ul> |
| <b>Compact Model</b> | <ul style="list-style-type: none"> <li>Based on physical behavior</li> <li>Frequency and temperature (and other parameters) dependent</li> <li>Response at schematic level</li> <li>Process variations</li> <li>Worldwide standards defined</li> </ul> | <ul style="list-style-type: none"> <li>Valid at a limited topology and geometry</li> <li>Limits the freedom to design new topologies</li> <li>No cross-talk effect</li> <li>Long development time</li> </ul>   |
| <b>MoM</b>           | <ul style="list-style-type: none"> <li>Good for metallic structure</li> </ul>  | <ul style="list-style-type: none"> <li>Difficult to resolve dielectric problem</li> </ul>  |



|             |  |   |
|-------------|--|---|
|             | Closed form has the possibility to use finite die extension  | Open form: Impossible to define finite dimension. And cannot handle inhomogeneous layers such as DTI.<br><br>Closed form: is based on 2.5D EM model (not fully 3D). |
| <b>FDTD</b> | One resolution gives a response for a wide band<br>Flexibility to model EM problems in conductor, dielectric and others materials with anisotropies structures<br>Good approach for antennas | Large memory requirements<br>Regular cube discretization<br>Only propagated field   |
| <b>FEM</b>  | Very flexible in discretization: each element has electrical and geometrical property independent of other elements.<br>Can define a finite extension (for die, package and PCB stacks)      | Difficult for open systems.<br>Complex to use.<br>CPU intensive<br>Only for part of the design, not possible for the complete design.                               |

## I.3. Substrate Network Analysis Methodology

### I.3.1. Substrate network analysis integration in NXP's design flow

The use of numerical solvers aiming at simulating the behaviour of different isolation schemes is impractical when applied to actual circuit situation, such as design analysis since this is a CPU-intensive procedure. Circuit parasitic extraction is better suited for this purpose.

The standard PEX (Parasitic EXtraction) solution considers the substrate as an ideal ground node. This in spite of the fact that the distributed nature of the coupling to substrate in the RF domain, requires a connection to a substrate mesh.

An extraction is the process by which an electrical equivalent model of the substrate, possibly including resistance and/or capacitance is determined. This approach has been preferred to other solutions because of its ability to model complex 3D structures such as wells, contacts, substrate taps, deep trenches, diffusions etc.

Once the extraction is completed, circuit simulation can be performed on the design including the three-dimensional extracted RC network for the substrate. If a circuit-level simulation is performed with substrate extraction, the time should be short and not limit this approach only for analysing small components [I-32] [I-33]. The following figure (1-14) summarizes the design flow.

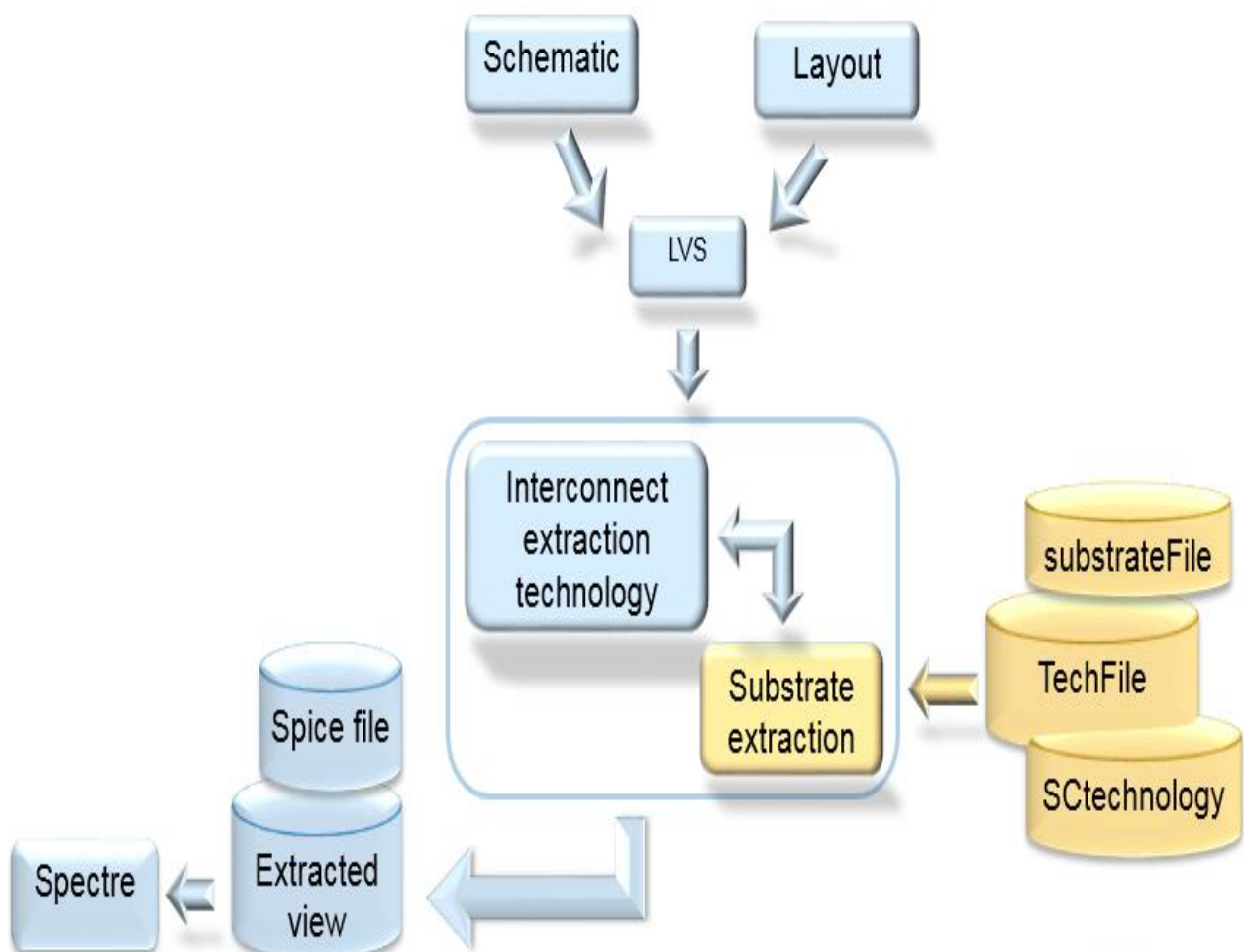


Figure I. 14 Flowchart of PEX including substrate extraction.

- **Substrate Extraction implementation**

Parasitic extraction starts with PDK (Process Design Kit) technology files. To enable substrate extraction, additional rules, describing the substrate parameters are added to the PDK. This allows for a smooth flow going from schematic capture, layout, LVS and finally the creation of an extracted parasitic netlist which is used for re-simulation (Post layout simulation). To properly characterize a semiconductor technology for substrate parasitic extraction, technology details such as substrate doping-profiles are needed. The substrate extractor requires cross-sections of the carrier doping concentration from the top of junctions down to the backside of the wafer. Each different region in the process technology needs its own cross-section.

- **Technology File**

To model the substrate effect, doping information is required to be able to calculate the conductivity at any point (x, y, z) in the substrate. Doping profiles are obtained from TCAD simulations and represent net carrier concentration of the different doping configurations. For every process technology, there are many doping profiles needed for different parts of the fabricated devices. The doping concentration of each layer is the mean of the non-uniform doping profile within this layer. This process is named profile discretization.

Figure I.15 shows that there are several regions to consider. The regions and their boundaries are determined by the levels and by the types of doping present in them. The substrate technology file can be created by using the process doping profiles as input to the substrate extractor.

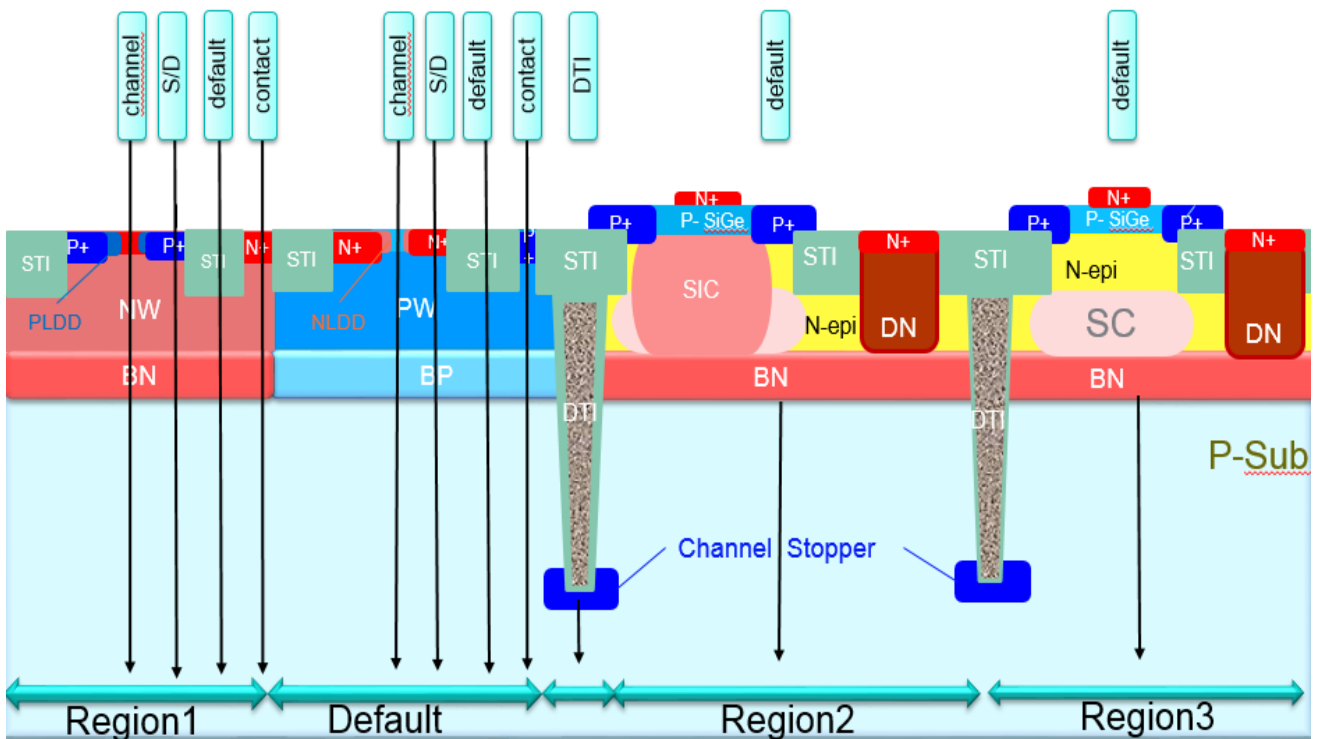


Figure I. 15.Regions and cross-sections in BiCMOS technology

### I.3.2. Substrate extraction

The substrate extraction procedure splits the layout area into multiple regions.

It is important to make the substrate extraction user friendly and integrate it into the standard design flow.

All the mathematical methods for substrate extraction depend on the same inputs:

- Layout information,
- Substrate description (technology)
- Electrical information (net names)

The areas that interact with the substrate are marked as substrate ports.

The substrate model must be based on the three dimensions of the substrate. The substrate extraction uses doping profile information to find equations that describe the substrate. The different layers of the substrate have different doping levels. For this reason, the substrate is divided into many smaller elements, each element has a resistivity and a permittivity. The equations are then solved so that a model of an element is achieved.

The resulting model is shown in figure I.16(b), where each impedance from a surface to the middle node a, is modelled as a resistor in parallel with a capacitor with the values of R and C, respectively. When the substrate is segmented into many cubic elements (figure I.16), the substrate mesh is obtained.

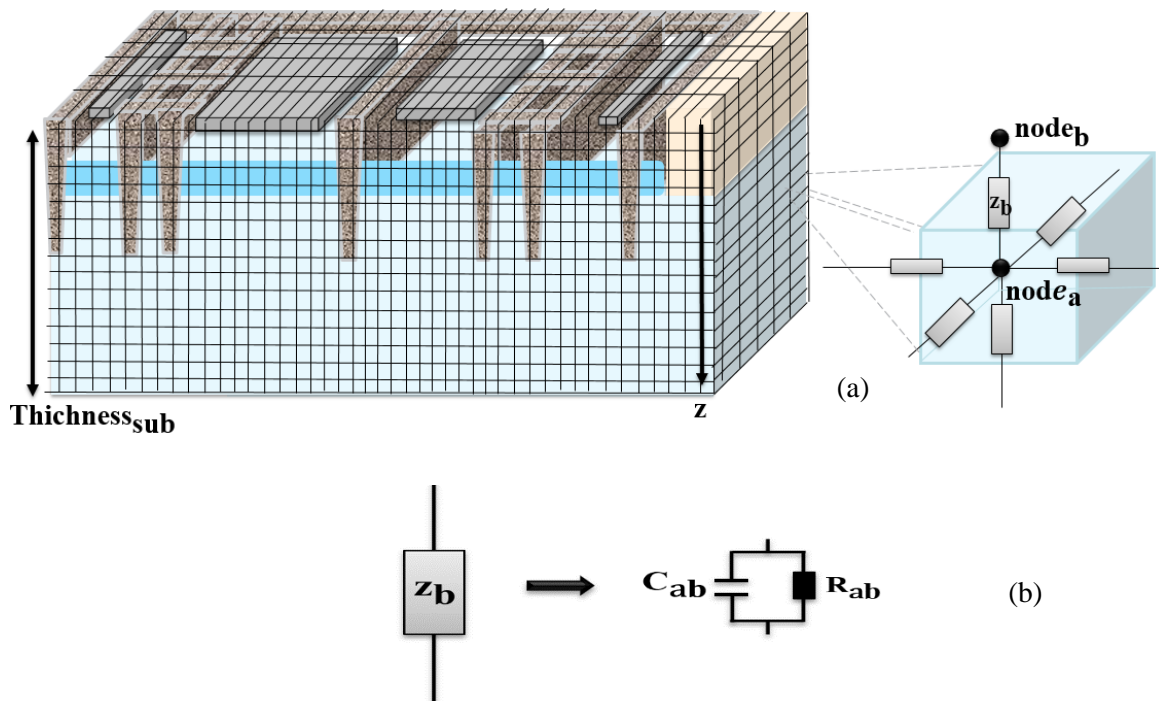


Figure I. 16. Capacitances and Resistances around a mesh node in the electrical substrate mesh

There are two main fields of application where substrate analysis is required:

- To investigate substrate coupling depending on the technology used,
- To find the optimal solution to tackle substrate losses. Like DTI, guard rings, substrate contacts position, triple well, or any combination...

### I.3.3. Align device model and substrate extraction

It should be noted that sometimes, the substrate resistors and/or capacitors are already included in the device model to take the behaviour of the substrate itself into account. These built-in components can be used for a first approximation of the substrate loading. However, if accurate substrate modelling is required it is suggested to disable them and to use an external substrate circuit instead.

In addition, it is not possible in practice to model the substrate inside the device, the coupling between the neighbour components, neither to offer a substrate model that account also for the design context. Because of this, it is necessary to turn off the substrate model at post-layout simulation and keep the extraction using the proposal methodology which offers a tread-off between accuracy and design freedom.

Aligning device model and parasitic extraction consists of making sure that:

1. The plug-in substrate model is activated at schematic level (PEX run without substrate extraction).
2. The plug-in substrate model is disconnected when running post-layout simulation
3. There is no overlap between the backend PEX model and the extracted substrate model

These three conditions can be handled by means of a model-parameter. This model-parameter is used to control whether or not the internal substrate model of the device model is enabled or not. Below we explain the case of the pMOS device as described figure 1-17, two scenarios are discussed:

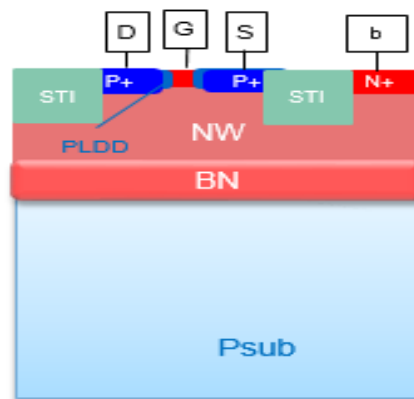


Figure I. 17.pMOS cross section

**Scenario 1:** Consider the complete Nwell (NW) impedance during substrate extraction. In that case, we will have a double capacitance counting:

1. BN/ Psub parasitic diode model is accounted for at post layout simulation
2. Substrate extraction will create, for this same junction, a distributed capacitance network at a given reverse bias.

**Scenario 2:** we extract only the psub below the pMOS (starts right below the bottom of the Buried N).

We have chosen the second scenario: keep the parasitic diode in the compact model because it is reserves bias and temperature dependent.

This strategy of alignment between model and substrate extraction were discussed for all BiCMOS devices such as bipolar transistors, resistors, ESD diodes...

## **I.4. Front-end RFIC design and general consideration**

The challenges for the next generation wireless circuits will increase even further, when designs will need to meet multi-standards. Evaluations of various integration strategies will need to be performed to verify the feasibility of the proposed integration approach, these evaluations must also consider issues such as performance and cost. The requirements of the various communication standards differ over a very wide range in terms of linearity, noise figure, isolation, bandwidth, etc. This will have an impact on all radio front-end building blocks, and require comprehensive trade-off analysis to select the best appropriate architecture and derive the individual circuit block requirements.

In this section, we will discuss the most important design considerations when specifying the requirements of all the components in the system.

### **I.4.1. Receiver architecture**

The RF front-end is a key block in wireless systems. It typically consists of a power amplifier (PA) in transmit mode and a low-noise amplifier (LNA) in reception mode. [I-38]. The first stage after the antenna and the RF filter in the receiver chain is typically an LNA. Since every stage in the receiver chain adds noise to the signal, very weak signals will be included in this noise and be lost. The main function of the LNA is to provide high enough gain to overcome the noise of subsequent stages (mixer etc.), while adding as little noise as possible. At the same time, it should be linear enough to handle strong interferers without introducing intermodulation distortion. The topology of an RF transceiver is shown in figure I.18.

An essential component of the RFIC architecture is the RF switch [I-1]. The power handling capability of the RF switch limits the amount of power that can be transmitted through the system. Moreover, the insertion loss of the switch also adds to the noise-figure of the receiver, and the LNA has a direct impact on the receiver signal-to-noise ratio (SNR) and thus can restrict the maximum data rate, receiver sensitivity, and other receiver parameters. For wireless receivers, the SNR limits the minimum detectable signal and therefore limits the receiver dynamic range.

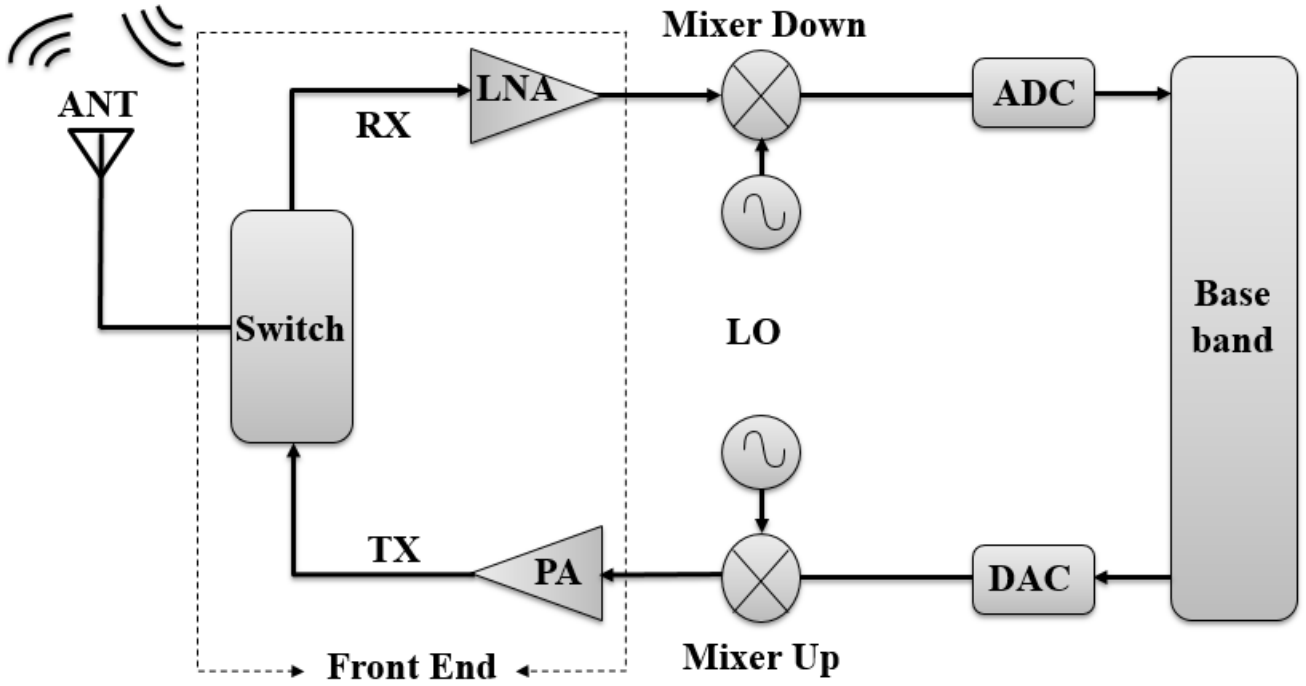


Figure I. 18. Block diagram of a simple RF transceiver architecture

#### I.4.2. Design Considerations

Due to the very different operating conditions of a transceiver and depending on the surrounding environment several requirements can be specified.

- a. **Noise figure and sensitivity:** Sensitivity is the key specification for a receiver. Receiver sensitivity means, the ability to handle the minimum signal level with the acceptable signal-to-noise ratio. There is no such measurement standard for measuring the sensitivity. However, we can measure the sensitivity with the help of the noise figure. The noise figure is a measure of how much the SNR (Signal to Noise Ratio) degrades as the received signal passes through a receiver [I-9]. Noise Figure can be defined in several ways. The most common definition of noise factor is:

$$N_{factor} = \frac{SNR_{in}}{SNR_{out}} \quad (I-7)$$

The noise figure NF is defined as the noise factor in dB.

The required noise figure (NF) of the front-end is calculated from the following formula:

$$NF(dB) = P_{in}(dBm) - P_{nf}(dBm) - SNR_{out}(dB) - 10\log(BW) \quad (I-8)$$

where  $P_{in}$  is the sensitivity level,  $P_{nf}$  is the thermal noise floor equal to  $10\log(kT)$ .  $SNR_{out}$  is the minimal output signal to noise ratio of the designed Front-End. BW is the bandwidth of interest.

For a cascade of n-stages, the total noise figure ( $NF_{total}$ ) can be obtained in terms of noise figure and gain of each stage. This known as Friis equation [I-10] [I-11].

$$NF_{total} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \dots + \frac{NF_n - 1}{G_1 G_2 \dots G_{n-1}} \quad (I-9)$$

where  $NF_{total}$  is the cumulative noise figure of n-stages referring to the input of the first stage,  $NF_i$  is the noise figure of the i-th stage,  $G_i$  is the gain or attenuation of the i-th stage.

- b. Selectivity:** Selectivity is the ability to reject all unwanted signals which enter through the antenna interface. Therefore, at least two characteristics have to be considered simultaneously for selectivity. On the one hand, the selective components should be sharp enough and on the other hand they should be broad enough to pass the highest side band frequencies with acceptable distortion in amplitude and phase. Filters are very vital elements for Rx performance, because they have a role for both sensitivity and selectivity issues. However, different architectures and different frequency plan have different filtering problems. Therefore, better selection of receiver architecture and frequency plan will bring better selectivity [I-13].
- c. Power handling capability:** Interfering RF signals together with receiver nonlinearities can generate intermodulation products that fall into the channel of interest resulting in the reduction of the system dynamic range. The receiver linearity is usually specified through the IIP3 and 1-dB compression point ( $P_{1dB}$ ). For the given interferers at  $f_1$  and  $f_2$  close to the desired signal, the third-order intermodulation products (IM3) appear at  $2f_1 - f_2$  and  $2f_2 - f_1$ . When the magnitude of the interferers gets large, the magnitude of the third-order intermodulation products also gets large and distorts the desired signal. The input-referred third-order intercept point (IIP3) is considered a measure of how linear the circuit is [I-11]. Thus, IIP3 of each stage should be sufficiently high to avoid corruption of the desired signal by the third-order intermodulation products (IM3) [I-10].

$$IIP3 = P_{int} + \frac{P_{int} - P_s + SNR_{req} + M}{2} \quad (I-10)$$

where  $P_{int}$  is the power of the interferer,  $P_s$  is the power of the desired signal,  $SNR_{req}$  is the required SNR, and  $M$  is the circuit margin.

- d. Dynamic range:** In analog circuits, such as amplifiers, the dynamic range is defined by both the signal-to-noise ratio (SNR) and the spurious free dynamic range (SFDR). The SFDR is the maximum relative level of interferences that a receiver can tolerate while producing an acceptable quality from a low input level. The lower end of the dynamic range is defined by the sensitivity of the receiver. The upper end of the dynamic range is defined by the maximum input level that the system can tolerate without distorting the signal [I-11].
- e. Insertion loss:** is defined as the signal power loss introduced by the RF switch between the input port and the output port in its on-state. The main contributing factors include on resistance and substrate loss [I-14]. It is measured by:
- $$IL(dB) = -20 \log_{10} |S_{21}| \quad (I-11)$$
- f. Isolation:** It refers to the RF isolation between the input and the output of the circuit and to how well the RF switch is able to prevent power leakage from the input. It is measured by  $S_{21}$  of the switch in the Off-state [I-15]. The main contributing factor is the capacitive coupling.



- g. Power consumption:** Low power consumption is usually required. The previous three requirements should not be solved at the expense of severely increased power consumption.
- h. Switching time:** between On-state and Off-state is also of particular interest

Thus, RFIC designers face several important challenges. Considering a large IC, such as a wireless transceiver, high-speed requirements make circuits extremely sensitive to parasitic elements. This includes passive modelling, interconnect parasitic and substrate behaviour. Thus, the essence of the RFIC flow is the ability to manage, replicate and control post-layout simulations and effects, and effectively use this information at timely points throughout the design process

## **I.5. Context and challenges brought out**

### **I.5.1. Motivation**

During design phase, modelling active devices (nMOS, ESD diode...) and passive devices (inductors, MIM capacitors. TL.) in order to have a first approximation of circuit behavioural where coupling effects and substrate losses must be considered remains very challenging for available simulation tools. In addition, for available modelling techniques, there is the lack of missing substrate network modelling under active devices. The coupling between neighbouring devices through the substrate is also not easy to deal with.

The available methodologies that have been proposed and investigated to reduce substrate coupling in FEICs (Front-End Integrated Circuits), are related to device optimization (resistive body floating technique...), design techniques (by parallel resonant circuits connected to the bulk, shield...) [I-7] and process-technology itself [I-8] like Silicon on Isolator (SOI). However, the considered solutions must not jeopardize other performances related to frontend IC's (NF for LNA, linearity for PA ...). So, optimizing the process and the performances for all these parameters is a classical trade-off that every designer has to face. So, in view of reducing time to market, having design tools that are able to reduce design iterations is key.

The use of Deep Trench Isolation (DTI) exhibits interesting isolation capabilities [I-5] [I-6]. This kind of isolation is commonly used under inductors and other passive devices [I-6]. Nevertheless, its use still depends too often on empirical approaches and the literature is rather silent as to its optimal use in a complex design. This technique is also helpful to isolate the different active blocks from each-other in an RF switch, LNA and PA. Here again, there is no common practice published about its best implementation in terms of layout topology.

Although, the presence of DTI leads to inhomogeneous structures in the substrate layer stack. This requires an EM analysis in the space domain coupled to a very thin mesh and therefore results in excessive compute time (Finite Element Method-FEM). 2.5D MoM method (Method of Moments) can also be used, but shows strong limitations when an anisotropic substrate (like DTI) must be addressed.

The available library component models today can offer a substrate model. However, it is limited to handling the substrate effect under a device. The interaction between devices and the design context cannot be captured in this way.

The necessity appears for developing a methodology that is fully integrated in the design flow, to accurately predict substrate losses that can impact circuits performances, prior to device experimental evaluation

### **I.5.2. The proposed methodology to account for substrate effects**

We have seen that one of the major limitations to achieve the high performances requirements in the RF Font-End IC's is strongly linked to substrate losses [5] [6], and predictability of circuit behaviour prior to processing. Lower substrate impedance leads to higher insertion loss and thus higher Noise Figure (NF). For that reason, we propose different layout variants at device and circuit level to explain the DTI use model for circuit performance improvements.

In addition, evaluating substrate loss and EM (Electromagnetic) coupling mechanisms on the circuit performance with its high complex architecture (active, passive components and the related interconnections) is key to reduce design iterations. Therefore, the methodology must be able to deal with buried structures, including substrate contacts, DTI and all other non-uniform layers.

To analyse the substrate related losses in FE IC's, we propose circuit level design, characterization and modelling analysis of the specified parameters (Insertion loss, Isolation, Linearity, Noise Figure...) that includes substrate effects and Electromagnetic coupling mechanism.

The proposed modelling methodology combines the benefits two principal approaches: quasi-static approach developed for inhomogeneous substrate, and a 2.5D EM analysis that properly handle the different EM phenomena (eddy current losses, skin effect...)

### **I.5.3. The challenges**

To develop the proposed methodology for substrate modelling, some challenges must be underlined:

- The predictability of the methodology: to ensure the first-time right silicon, the methodology must be able to predict the adequate circuit behaviour before having measurement results.
- The accuracy: the required parameters mainly, noise figure, losses, linearity and isolation quality must be compliant with the requirement specifications
- The flow integration: the proposed methodology must be fully integrated in the design environment and easy to use.

## **I.6. Synthesis and concluding remarks: necessity of developing a methodology for modelling RF switches**

In this chapter, we set out the different existing methods and techniques of analysis for FEIC modelling purpose. The various methods cannot deal with all integrated circuit issues, like substrate losses and backend parasitic.

We proposed a methodology for substrate modelling that includes substrate effects in the device itself as well as substrate coupling between neighbouring devices that affect considerably the circuits performance. The modelling methodology at circuit level combines full wave analysis and substrate analysis.

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# Chapter II: Evaluation, characterization, modelling and analysis of single isolation structures

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# Introduction

This chapter will focus on test-structure definition, extraction and modelling to be placed on Silicon and then characterized. From measurements analysis, we will be able to get more knowledge about isolation strategy (especially in link with DTI) and thus give recommendations from design point of view at layout step.

After a first description of the considered process used to perform this study, I will provide details about the test-structures issued.

- Latter structures are related to passive elements such as coils
- Former ones are related to switch devices for which coupling phenomenon are known to degrade a lot performance (Insertion losses and thus Noise Figure)

In order to support theoretical investigations, these test-structures will be measured against frequency in the laboratory. Typical parameters such as  $Q_{factor}$ , Insertion losses, Isolation and Noise Figure will be compared for different layout variants.

Then we will make a state of art regarding the modelling strategies that can be considered for this type of substrate isolations. In fact, literature is quite mute on this kind of modelling. This is particularly key on our side as we have really tight requirements in terms of losses, Noise Figure and switching times. Modelling must be accurate enough to be able to tackle losses for a predictable simulation in a wide frequency range. This can be achieved only with a proper partitioning of the layout and good knowledge of loss mechanism occurring in the substrate.

The use of DTI (Deep Trenches Isolation) exhibits interesting isolation capabilities however it leads to an anisotropic structure in the substrate. This requires an analysis in a finite layer dimension.

To our knowledge, this is the first time, that such tool is developed and presented within a typical EDA commercial flow.

## II.1. Technology description

### II.1.1. BiCMOS process description

In a BiCMOS process bipolar transistors have been added to a CMOS technology. Adding bipolar, high-frequency devices, is needed for RF circuits because CMOS is not fast enough and can be limited when dealing with “high” power applications (PA, ...). Thus, it is possible to integrate RF circuits together with digital parts, for which CMOS is the only reasonable choice.

Modern BiCMOS processes use SiGe bipolar transistors. A graded Germanium profile within the base reduces the base transit time, thus improving  $f_T$ . BiCMOS technologies usually use a substrate with higher resistivity, compared to high-performance CMOS technologies, because of that is better suited for integration of High-Q passive components [II-15].

The ability of fabricating both SiGe bipolar and CMOS technologies on a single wafer, has created many opportunities for mixed-signal ICs. The SiGe technology offers high speed and gain, which is needed for many RF and analog applications.

The technology used for this study is a SiGe BiCMOS technology of NXP. It is an advanced high-speed BiCMOS technology, offering up to 6 layers of metal interconnect, 0.25 $\mu\text{m}$  nMOS and pMOS transistors, vertical NPN transistors (both high speed and high voltage versions), mono- and polysilicon resistors, diodes, and capacitors (including a high density MIM capacitor). Isolated (short channel) NMOS transistors, a vertical PNP transistor, and a SiGe thin film resistor are optionally available. Table II.1 represent the main NXP technology parameters:

Table II. 1 The used NXP BiCMOS manufacturing technology

| Parameters                                  | technology           |
|---|----------------------|
| BJT/HBT base                                | SiGe:C               |
| Lithography $_{min}$ of emitter             | 0.3 $\mu\text{m}$    |
| NPN $NF_{min}$ @ 2 GHz                      | < 0.4 dB             |
| NPN $NF_{min}$ @ 10 GHz                     | < 0.6 dB             |
| NPN $f_T/f_{max}$                           | 180 GHz/180 GHz      |
| nMOS figure of merit ( $R_{on} * C_{off}$ ) | 300 fs               |
| nMOS $f_T/f_{max}$                          | 45 / 80 GHz          |
| Substrate isolation                         | STI/DTI              |
| Capacitor (fF/ $\mu\text{m}^2$ )            | 5                    |
| MIM capacitor Q-factor                      | >100 up to 20-30 GHz |
| Inductor Q-factor (L=0.5 nH)                | > 20 at 20 GHz       |

FigureII.1 (a) Shows the  $f_T$  function of maximum Breakdown voltage in various generation of NXP BiCMOS technology vs IBM, ST and Infineon technologies.

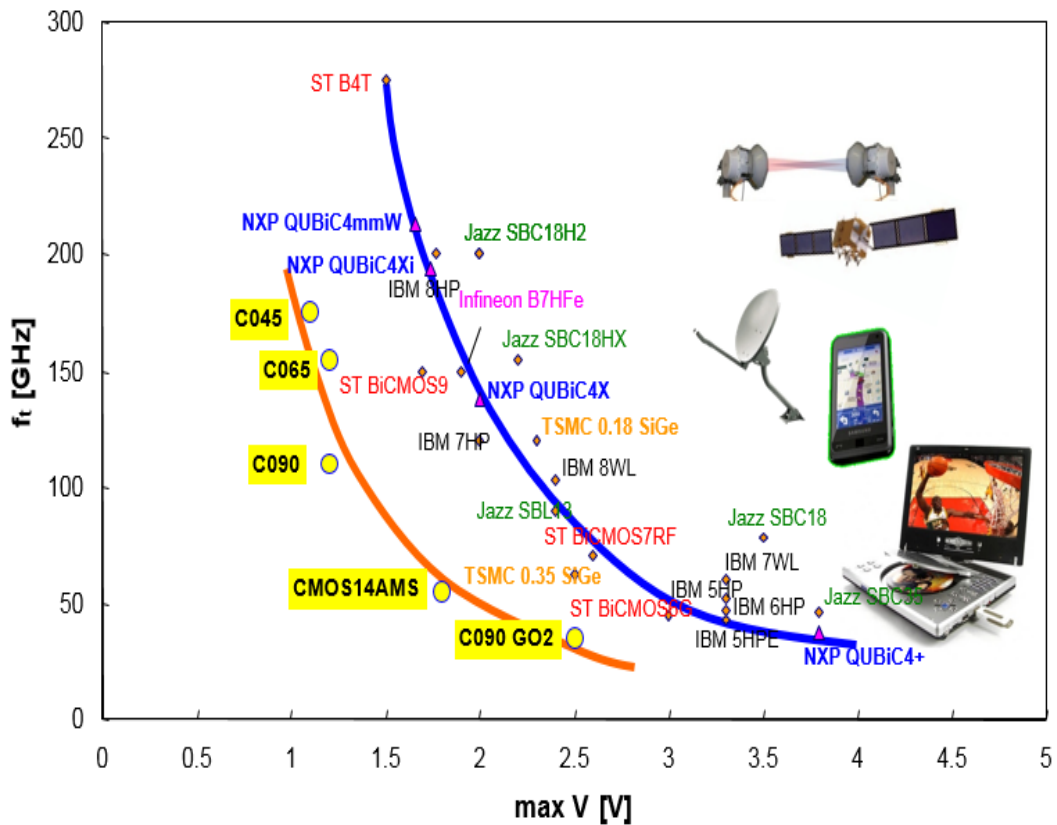


Figure II. 1.(a)  $f_t$  versus max  $BV_{ceo}$  for RF technologies

The figure.II.1 (b) illustrates a cross-section of the typical NXP in house BiCMOS 0.25  $\mu\text{m}$  process. Bulk silicon resistivity is 200 Ohm.cm. The buried P-Layer, acting as low resistivity lossy conductor, can be broken by Deep Trench Isolation-DTI for local high impedance conditions. The backplane of the substrate region can be grounded or left floating depending on the final application (WLCSP or QFN type of package).

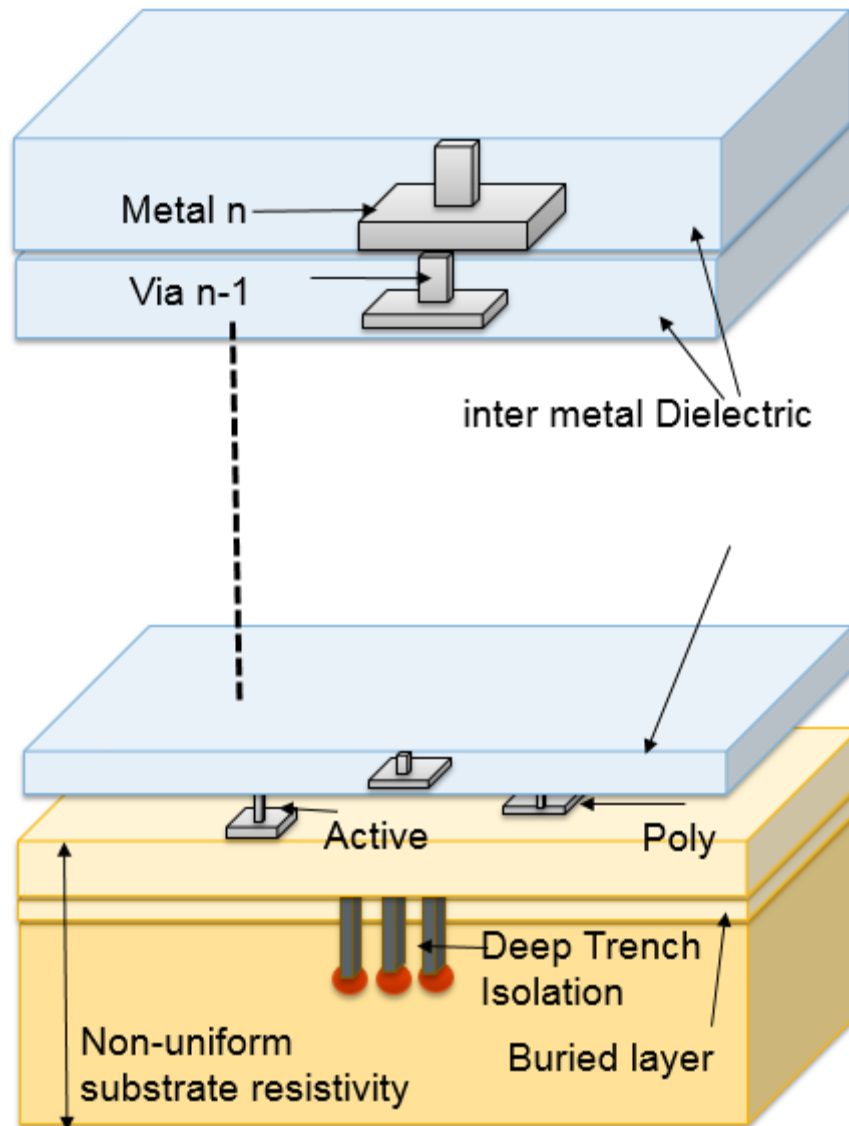


Figure II.1.(b) BiCMOS layers stack

Inductors are implemented thanks to the thicker top-level metal layers of the interconnect stack, to minimize the resistive loss, as well as the capacitive and magnetic losses to the dissipative silicon substrate. The Q-factor is limited by the metal series resistance at low frequencies, while at high frequencies the substrate resistivity is the limiting factor.

The metal layers M5 and M6 are 3 $\mu$ m thick, and the whole backend is in total 10  $\mu$ m thick. These dimensions make it challenging to design high quality passive devices. [I-5].

### II.1.2. Deep Trench Isolation-DTI in BiCMOS technology

DTI (Deep Trench Isolation) is a layer in the SiGe BiCMOS technology that can be used in two ways:

1. Create an area on the die that has a much lower capacitance to the substrate (Vertical isolation), using a kind-of honeycomb structure of DTI.

In figure, an example of a single RF PAD. The DTI impact on the coupling capacitance has been evaluated:

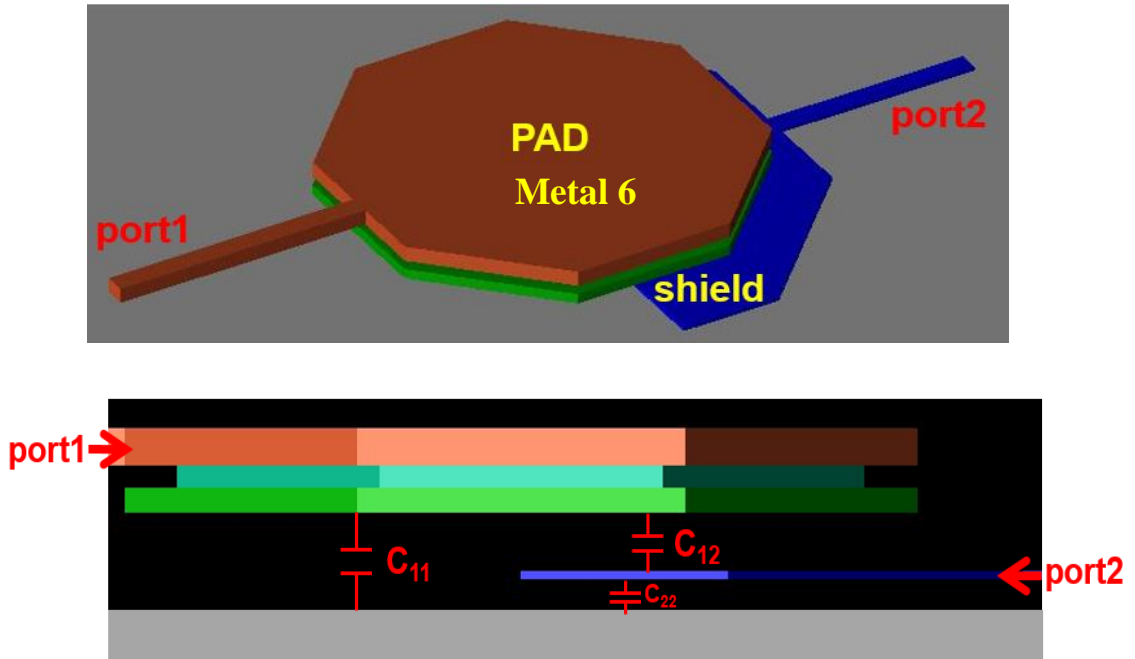


Figure II.2. Top view and cross section of the RF pad using DTI shield

$C_{11}$  is the coupling capacitor between port1 and the ground reference,  $C_{22}$  is the coupling capacitor between port2 and the ground reference, and  $C_{12}$  the coupling capacitor between port1 and port2.

By Applying the formula:  $C_{vertical} = \frac{\epsilon_0 \epsilon_r \cdot Area}{Distance}$  (II-1), increasing the distance to substrate leads to decreasing the vertical capacitance

Measurement were performed on two test cases:

- The RF PAD implemented with DTI shield:  $C_{22} = 42.54$  fF
  - Without DTI:  $C_{22DTI} = 20.53$  fF
- ⇒ A reduction is of substrate coupling capacitance is about 51.7 % with DTI

2. Create an area in the silicon that has less conductivity to the area on the other side of the DTI (lateral isolation). This is done by creating a polygon shape using a wall of DTI.

The trench has a liner of oxide along the entire trench, so both on the side-walls and the bottom, with the remainder of the trench filled with poly-silicon (figure II.4), with a relative dielectric constant of 11.9.

The effective capacitance of DTI is:

$$C_{DTI} = \left[ \frac{1}{C_{ox}} + \frac{1}{C_{poly}} + \frac{1}{C_{ox}} \right]^{-1} \quad (II-2)$$

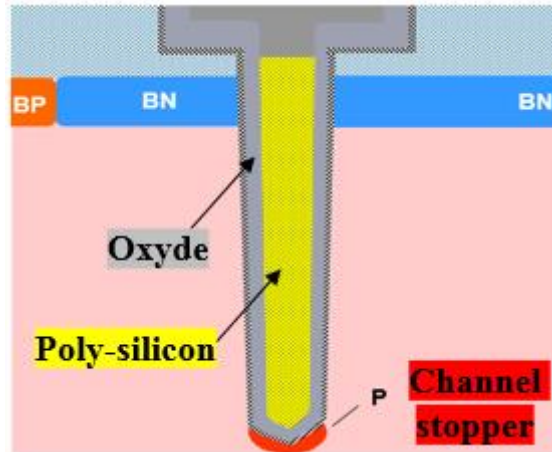


Figure II.3. DTI cross section in BiCMOS technology

Even better substrate isolation can be achieved by using SOS (Silicon On Sapphire) or SOI (Silicon On Isolator) substrates, but one of major difficulty is the low thermal conductivity of that materials, the mechanical stability and process ability [I-49].

Furthermore, current SiGe heterojunction bipolar transistor (HBT) technology offers  $f_T$  competitive with GaAs, the first real microwave IC technology, although GaAs still offers better quality for the passives and better power-handling capability. When high frequency operation with very good noise performance, mixed-signal capability, and low cost/high volume manufacturing are required SiGe is often the process of choice.

## II.2. Main substrate isolation techniques

In a bulk technology, parasitic signals propagate both in the heavily doped layers as well as in the P-substrate. Earlier it was described that the substrate coupling can really degrade the overall circuit performances. Therefore, the substrate coupling must be blocked or reduced so that it does not jeopardize device performances. The selection and implementation of the right isolation technique, becomes one of the key factors that allows silicon to be used for RF applications.

A variety of techniques to decrease the impact of the substrate have been proposed and studied. These techniques include choices of manufacturing technology, substrate thickness and resistivity, the physical separation between devices, the placement of substrate contacts, guard rings, triple wells, shield, via hole connection and Faraday cage [I-51] [II-3]. The most known and straightforward way to deal with substrate coupling and improve device isolation are described below:

### II.2.1. Guard Ring

A common technique to reduce substrate coupling by placing guard rings around the sensitive block. These guard ring consist of substrate contacts (Ptaps or Ntaps). A typical layout of guard bands is shown in figure.II.5. The guard ring acts as a low impedance path, filtering the current within the substrate. The efficiency of conventional guard rings, however, is limited due to the vertical current propagation paths throughout the substrate. A portion of the current can flow deeper into the substrate, thereby bypassing the guard ring, making the isolation less effective.

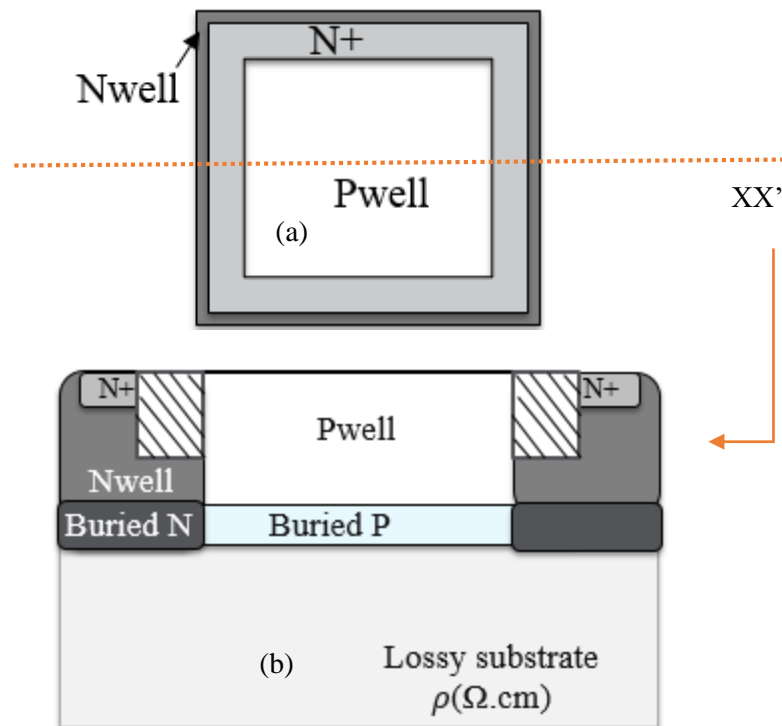


Figure II.4. Top view (a) and cross section (b) of N-type guard ring



## II.2.2. Buried layers

The horizontal isolation is possible by using wells separating the devices, it is possible to introduce under a block a deep N-doped layer called "Deep Nwell" (DNW), a few microns from the surface. Triple well or buried layer technologies provide the possibility to have double series PN-junctions. with increased impedance and Pwell isolation [II-2]. However, this configuration leads to high parasitic capacitances which limit its functionality at high frequency (Figure II.6).

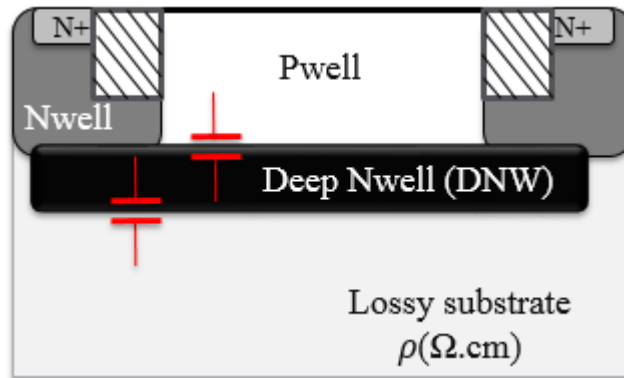


Figure II.5. Cross section a Deep Nwell isolation and the related capacitive coupling

## II.2.3. Pwell block and Buried P block layers

This allows for serial isolation with high impedance: on a localized zone, the Pwell and the buried P can be blocked and then an n-epitaxial layer appears with higher resistivity. It can be integrated between two blocks, or under passives blocks (Inductors, Transmission lines...) (Figure II.7) to improve the Q factor and reduce the parallel substrate resistance [II-27].

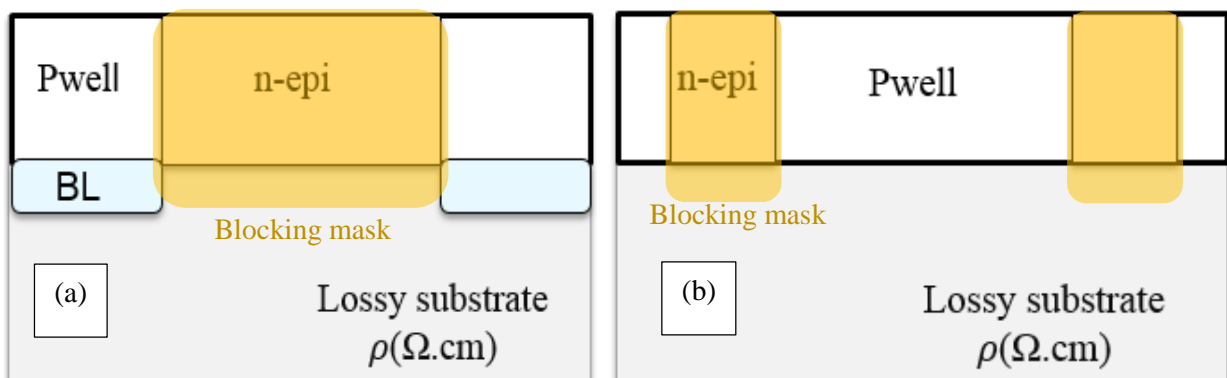


Figure II.6. Pwell block layer: (a) under bloc (b) between two blocks

## II.2.4. Deep-Trench-Isolation

A further improvement in isolation can be achieved using a deep trench isolation placed around the device [I-5]. It acts as lateral isolation based on the concept of applying a vertical trench to the substrate coupling path. The trench interrupts the undesired propagation path and forces the disturbance to penetrate deep into the more resistive substrate.

The Deep Trench Isolation-DTI is used to have a “floating” body in MOS devices and to assess new isolation strategy to increase the impedance path of undesired coupling, thus improve the circuit performances. In addition, the use of Deep Trench isolation is extended to passive devices such as inductors for which for Q-factor improvement and substrate coupling reduction can be achieved. The DTI is introduced underneath the inductor to interrupt the BL (Buried Layer) and part of the lossy silicon substrate. However, the main drawbacks of the DTI are the high conductivity of the channel stopper under DTI, and the mechanical stress for grinded wafer.

## II.3. Substrate isolation influence on passive elements

### II.4.1 The influence of Deep Trench Isolation on coils

The main purpose of the passive devices presented in this section is to serve as inductive elements in ESD protection, matching network, pads and bridge distance between devices. However, on-chip inductors available in BiCMOS process technology, exhibit relatively a poor Q factor due to the losses in silicon substrate and Ohmic loss of thin metal layer [III-3].

Inductor's loss depends on the geometry of the inductor, metal conductivity, substrate resistivity, and frequency of operation. Metal losses dominate at low frequencies, whereas substrate losses are critical at high frequencies.

The conductor loss is proportional to the series resistance of the inductance. At low frequencies, the series resistance can be calculated from the know equation: ( $R_{dc} = \rho \frac{l}{w.t}$  (II-3) where w is the width, t is the thickness, l is the total length of the conductor strip in the coil, and  $\rho$  is the resistivity of the conductor material).

However, at higher frequencies, the series resistance becomes a complex function due to the skin effect and eddy currents. The series resistance increases significantly at higher frequencies due to eddy currents (magnetically induced currents). It thus reduces the overall quality factor.

The substrate loss consists of two parts: finite resistance due to electrically induced conductive and displacement currents, and magnetically induced eddy current resistance. These losses are known as capacitive and magnetic, respectively.

Capacitive loss can be minimized by either using very high resistivity substrates or by placing a shield between the oxide layer and the substrate. However, due to the low resistivity of Si substrates, currents induced by the penetration of the magnetic fields of the inductor into the substrate cause extra resistive loss.

In order to improve inductor Q-factor, different techniques regrouped into four principal categories in [II-16]:

- Layout optimization (differential configuration, vertical inductors, variable line width) [II-217]:
- The metal parameters (thicker, high conductivity) [II-18]
- The use of high resistivity substrate (High resistivity material, low dielectric material, Si on Sapphire, or Glass or Isolator, ...) [II-19] [II-20]
- The use of a substrate shield (Metal or Poly Ground Shield, DTI shield, ...) [II-21]

In this study, we investigate the impact of various shielding strategies. The effects metallic shield, the DTI and BL (Buried Layer) on substrate coupling is compared.

The Buried layer has a high conductivity (~1200 S/m) which leads to a low impedance path of the eddy current. To increase this impedance, we investigate two techniques: removing the buried layer underneath the inductor, or using the DTI to break the community of the buried layer.

The test case considered is a 6.6nH octagonal inductor with various shielding strategies (figure II.8)

- Metal 1 shield
- Poly shield
- DTI mesh
- DTI mesh with removing the buried layer
- Blocking only the buried layer

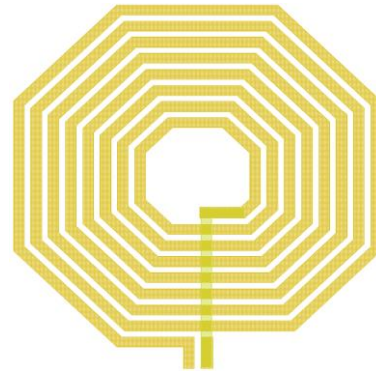


Figure II. 7. octagonal inductor under test

Table II. 2. Shielding techniques with the corresponding cross section

| Metal 1 shield | Poly Shield | DTI | DTI noBP | noBP |
|----------------|-------------|-----|----------|------|
|                |             |     |          |      |

For this evaluation, two ports measurements were performed from 100 MHz to 20GHz, with an Open, Short, Load structures for De-embedding purposes.

## II.4.2 Modelling of inductors in circuit simulation

To accurately consider the behaviour of the inductors in circuit simulation, we need to use an equivalent circuit consisting of magnetic and electric storage elements as well as loss elements. A commonly accepted equivalent circuit is the  $\pi$  mode shown in figure.II.8 accounts for the effect of dielectric layer between the inductor and the substrate (Si), and for the inductive and capacitive losses. The magnetic field generated by the current on the spiral induces current in the substrate, which has the opposite polarity, giving rise to a parallel parasitic inductor as shown in figure II.9.

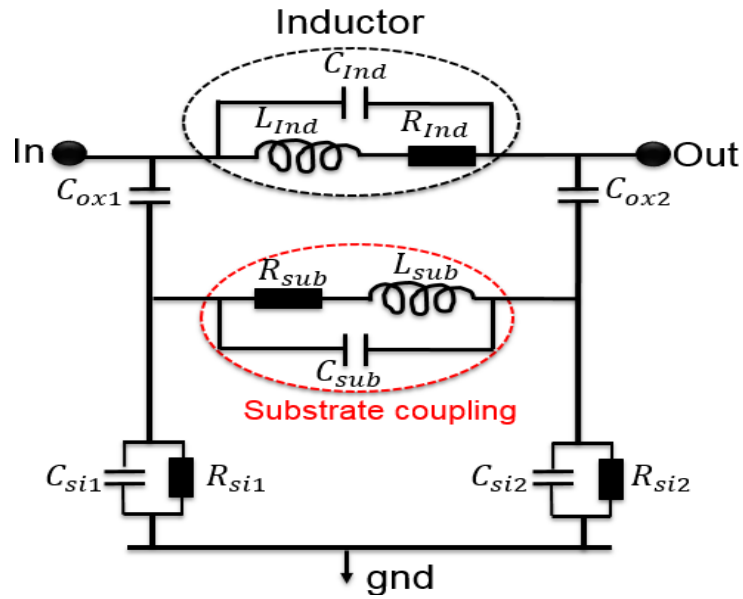


Figure II.8. Equivalent circuit of on-chip inductor

Where:

$L_{ind}$ : Total inductance

$C_{ind}$ : Fringing capacitance between the inductor windings

$R_{ind}$ : series resistance of the inductor metal

$C_{ox}$ : Shunt capacitances of the oxide layer

$R_{si}$  and  $C_{si}$ : Silicon resistance and capacitance due to substrate losses

$L_{sub}$ ,  $R_{sub}$  and  $C_{sub}$ : Parallel inductance, resistance and capacitance due to eddy current loss in the substrate.

The inductance value and its quality factor should be determined with accuracy. Here,  $\pi$  type equivalent circuit is introduced for simple two-port inductors (Figure II.10), and the derivation of inductance, quality factor, the parallel parasitic resistance and the coupling capacitance to the substrate is presented.

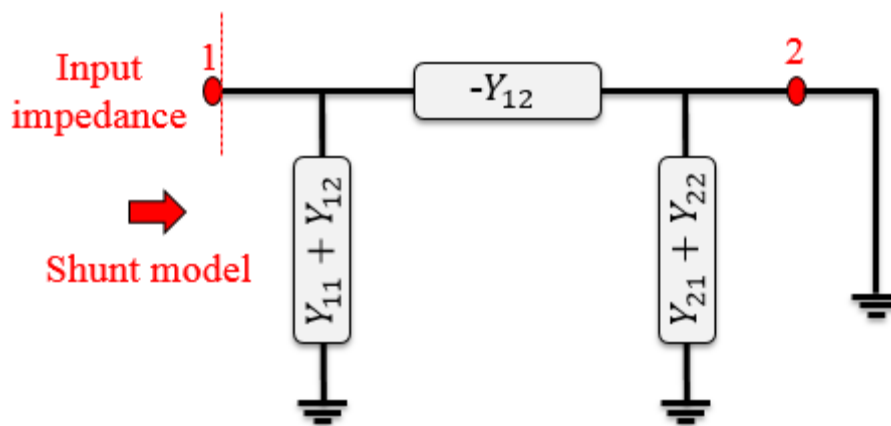


Figure II.9. Shunt model

In this case, input impedance of the inductor in the single-ended mode can be calculated by  $1/Y_{11}$ :

$$L = \frac{\text{imag}(1/Y_{11})}{\omega} \quad (II-4)$$

$$Q = \frac{\text{imag}(1/Y_{11})}{\text{real}(1/Y_{11})} \quad (II-5)$$

$$R_{sub} = 1/\text{real}(Y_{11}) \quad (II-6)$$

$$C_{sub1} = \frac{\text{imag}(Y_{11}+Y_{12})}{\omega} \quad (II-7)$$

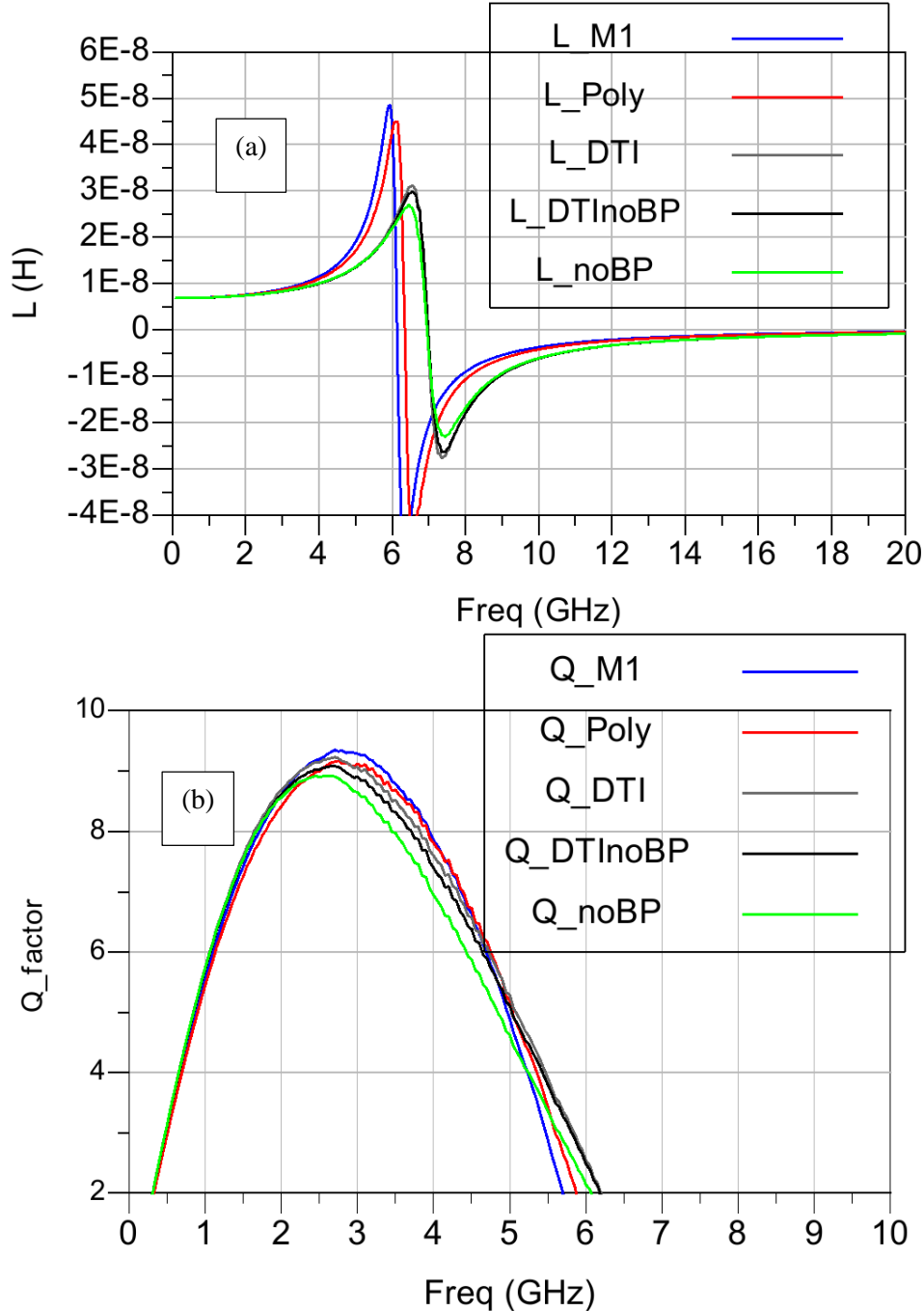


Figure II. 10. Comparison between measurements of the shield strategies applied to the inductor (Metal shield, Poly Shield, DTI, DTI without BP and noBP) (a): Inductance value, (b): Q-factor

At lower frequencies ( $<2.4$ GHz), difference between Q-factor as function of the shield-type (Metal shield, Poly shield) or the substrate optimization (DTI, DTI noBP or noBP) is marginal.

At frequencies above 2.4GHz, the metal shield reaches the highest Q-factor.

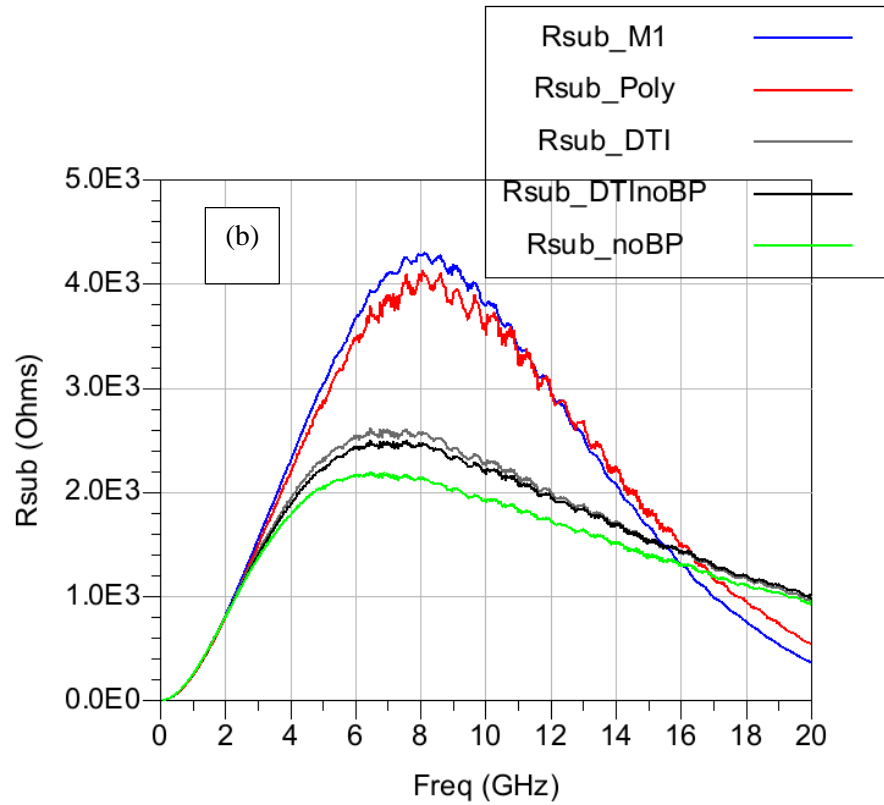
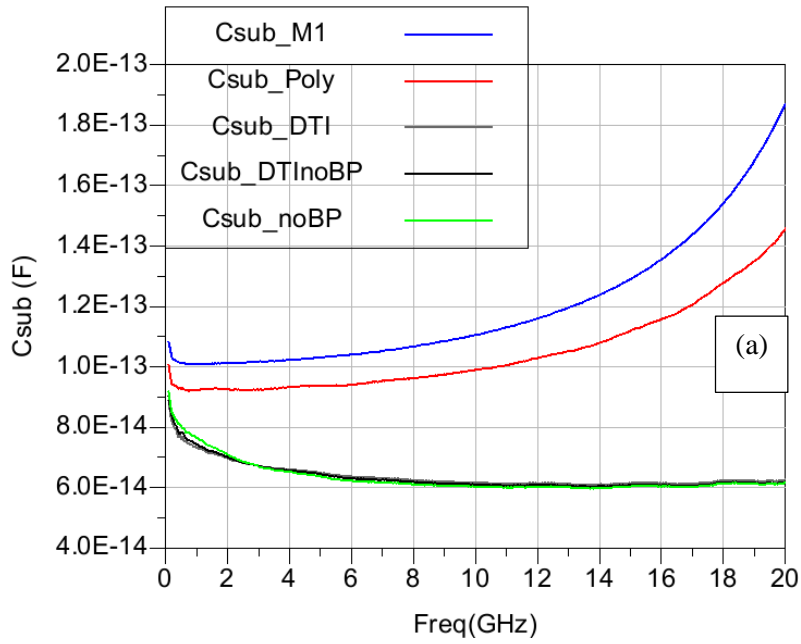


Figure II.11 Comparison between the shielding strategies applied to the inductor (Metal1 shield, Poly Shield, DTI, DTI without BP and noBP) (a): Coupling capacitance value, (b) parallel substrate resistance.

The coupling capacitance to the shield metal or to the substrate decreases with increased distance to shield or to the substrate. The lowest capacitance is reached with the use of the DTI, or by removing the buried layer.

Table II.3. Inductor performances function of different shield (a) at 2.4GHz, and (b) at 5.8GHz

| Shield strategy | $C_{sub}$ (fF)<br>At 2.4GHz | $R_{sub}$ (K $\Omega$ )<br>at 2.4GHz | L (nH)<br>at 2.4GHz | Q-factor<br>at 2.4GHz |
|-----------------|-----------------------------|--------------------------------------|---------------------|-----------------------|
|-----------------|-----------------------------|--------------------------------------|---------------------|-----------------------|

(a)

|                       |     |     |     |     |
|-----------------------|-----|-----|-----|-----|
| <b>Metal 1 shield</b> | 101 | 1.1 | 7.8 | 9.1 |
| <b>Poly shield</b>    | 92  | 1   | 7.8 | 9   |
| <b>DTI</b>            | 68  | 1   | 7.7 | 9   |
| <b>DTI noBP</b>       | 68  | 1   | 7.7 | 8.9 |
| <b>NoBP</b>           | 68  | 1   | 7.7 | 8.8 |

| Shield strategy<br>(b) | $C_{sub}$ (fF)<br>At 5.8GHz | $R_{sub}$ (K $\Omega$ )<br>at 5.8GHz | L (nH)<br>at 5.8GHz | Q-factor<br>at 5.8GHz |
|------------------------|-----------------------------|--------------------------------------|---------------------|-----------------------|
| <b>Metal 1 shield</b>  | 103                         | 3                                    | 17                  | 4.9                   |
| <b>Poly shield</b>     | 94                          | 2.9                                  | 1                   | 5.2                   |
| <b>DTI</b>             | 65                          | 2.34                                 | 13                  | 5.2                   |
| <b>DTI noBP</b>        | 64                          | 2.2                                  | 13                  | 5.1                   |
| <b>noBP</b>            | 63                          | 2                                    | 13                  | 4.6                   |

From the measurements results, Metal shield is the best option to reach high Q-factor; it is recommended to use metallic shields at higher frequencies. However, the substrate related losses are also higher this is due to the penetration of magnetic field to the substrate.

The Q factor formulation is proper for inductors when serving as shunt elements. However, inductors are also used frequently as series elements in many applications and their performance is lower than predicted by one-port formulation in these cases.

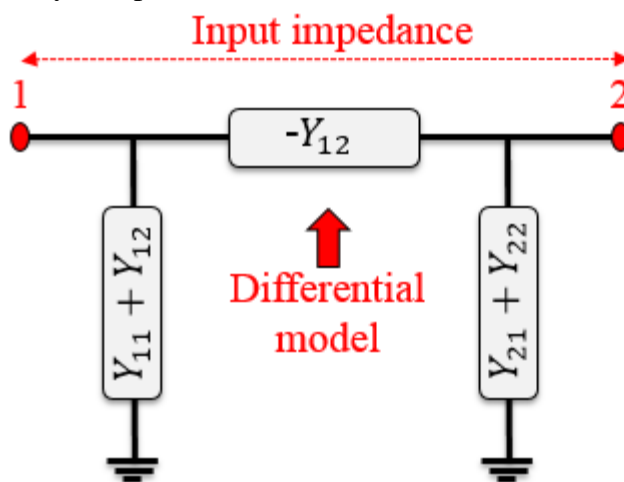


Figure II.12. Differential model

To calculate differential Q factor from 2-port simulations, we need a different equation which measures differentially between port 1 and 2 (figure II.13).

- $Z_{dd} = Z(1,1) + Z(2,2) - Z(1,2) - Z(2,1)$  (II-8)
- $Y_{cc} = Y(1,1) + Y(2,2) + Y(1,2) + Y(2,1)$  (II-9)
- represents the common mode admittance. Quantifies the max Noise that can be generated by the device [II-22]

We define the inductance differential L and Q-factor value from the differential model (Figure II.13) as following:



$$L_{dd} = \frac{\text{imag}(Z_{dd})}{2\pi f} \quad (II-10)$$

$$Q_{dd} = \frac{\text{imag}(Z_{dd})}{\text{real}(Z_{dd})} \quad (II-11)$$

$$C_{sub} = \frac{\text{imag}(Y_{cc})}{2\pi f} \quad (II-12)$$

For a two ports inductor, the single ended Q factor is lower than the differential Q factor, because the substrate impact is minimized.

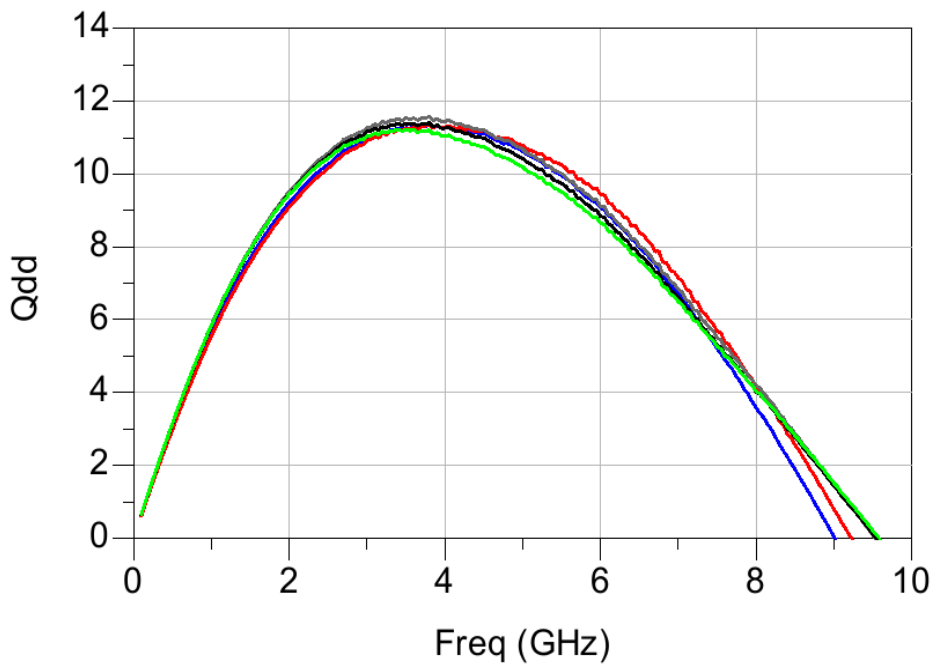


Figure II.13 Differential Q-factor ( $Q_{dd}$ ) of inductor with different shield

At lower frequencies <2.4GHz, the shield metallic gives a good trade-off between High Q-factor and low losses. However, at frequencies >2.4GHz, in common mode, the capacitance is significantly lower without ground shield (compared to Metal 1 and poly-silicon ground shields), if DTI mesh is added or if the Buried-P layer is removed underneath the inductor. In order to ensure a good trade-off between higher Q-factor, lower substrate loss and footprint, the use of DTI or removal of the Buried-P layer is recommended in combination with layout optimisation (stacked inductor for example or the inductor architecture modification).

## II.4. Substrate extraction between two substrate taps

### II.4.1. Substrate taps

By default, each nMOS switch does not contain a substrate pin. The fourth port of the MOS device is bulk substrate, which connects to the pwell and further via a contact to Metall1. The designers define the number of substrate contacts for the topology of their block. Figure.II.15 shows the cross section of substrate tap.

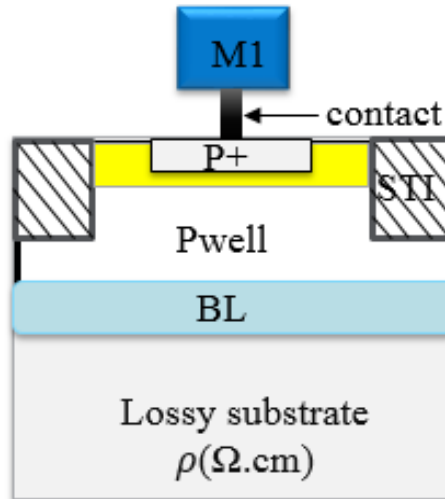


Figure II.14. Cross section of the substrate tap in BiCMOS technology

In the silicon substrate, a substrate tap is often used as a single ptap or guard rings of ptaps for circuit protection. Those ptaps are connected to certain potential to ensure that the substrate is at the required potential (most likely 0V). If the ptap is not placed properly, these regions can also participate on the substrate perturbation. In some configurations keeping the substrate floating leads to best performances.

### II.4.2. Substrate network extraction & analysis

In the past, the lack of fast simulation capability has restricted the study of substrate coupling to limited case studies. The substrate simulation strategy shown in this work, allows studying the dependence of substrate isolation and substrate model on various variables such as the conductivity of the substrate and substrate contact placement.

In the frequencies less than the substrate cut of frequency of the BiCMOS technology, the substrate can be modeled by a resistive network, but after this cut of frequency the capacitive behavior of the substrate appears.

By integrating the resistivity of the P-sub layer on the volume containing the major current flow, we estimated the equivalent resistance between the P-sub nodes of the two blocks. In a first step, we draw the equivalent lines in which the current lines lie that go from one block to the other; we simplified this volume by associating a parallelepiped (figure II.17).

The main limitation of available parasitic extractor for backend metallization, is the reference ground. All the substrate taps are assumed to be equipotential. To address this problem, full-wave simulation based methodology is required to properly account for substrate effect.

### II.4.3. Substrate network extraction without DTI

This analysis deals with understanding the behavior of the substrate resistance as function of doping profile. This analysis helps us to evaluate the accuracy and the sensitivity of the extracted substrate resistance based on different circuit topologies. Figure.II.16 represents the layer information of the structures to be used for the analysis.

The substrate resistance extracted between two Ptaps is compared to EM simulation and hand calculation.

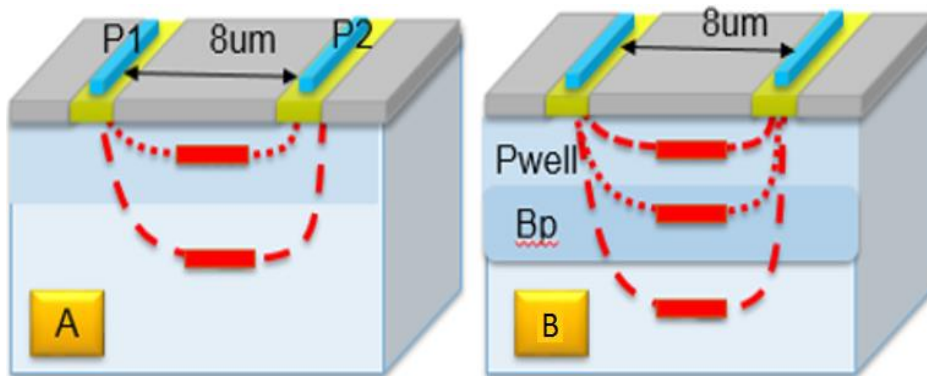


Figure II.15. Two contacts for substrate resistance extraction

- Topology **A**: this case allows us to extract the substrate resistance between P1 (port1) and P2 (port2) with a relatively high resistive substrate, the buried layer is removed.
- Topology **B**: due to the presence of the buried-p layer (buried-p has a better conductivity than pwell: 666 – 1200 S/m versus 333 S/m), using the buried-p layer results in a lower impedance between P1 and P2.

Table II.4 resume of the test cases under evaluation.

Table II.4. test case descriptions

| Structures description:  | Substrate description of the test cases |   |
|--|---|---|
| <ul style="list-style-type: none"> <li>• 2 Ptaps</li> <li>• Dimension(WxL) = 0.5<math>\mu</math>m x 10<math>\mu</math>m</li> <li>• Distance between 2Ptap = 8 <math>\mu</math>m</li> <li>• No DTI</li> </ul> | Test case <b>B</b>                      | <ul style="list-style-type: none"> <li>• With Pwell</li> <li>• With Buried layer</li> </ul>   |
|  |   | <ul style="list-style-type: none"> <li>• With Pwell</li> <li>• Without Buried layer</li> </ul>  |
|  | Test case <b>A</b>                      | <ul style="list-style-type: none"> <li>• With Pwell:<br/>Pwell resistivity (<math>\rho</math>) *2</li> <li>• With Buried layer</li> </ul> |

The major part of the signal propagates near the surface, and a small part flows deeper within the substrate. The deeper path resistance is then higher than the one close to the surface.

The signal path is approximated with a half-ellipse as illustrated in figure.II.17 the resistance of the path is calculated based on the perimeter of the ellipse.

Based on the approximation of [II-4], the perimeter can be calculated as the following:

$$p = \pi \left[ 3(x + y) - \sqrt{(3x + y)(x + 3y)} \right] \quad (II-13)$$

With x being the length of the semi-major axis and y being the measure of the semi-minor axis of the ellipse.

In our case, x represents the distance (d/2) between the two contacts, and y represents the depth; it varies based on the depth of the signal. The half-ellipse perimeter  $P_i$  is given by:

$$P_i = \frac{\pi}{2} \left[ 3 \left( \frac{d}{2} + h_i \right) - \sqrt{(1.5d + h_i)(1.5d + 3h_i)} \right] \quad (II-14)$$

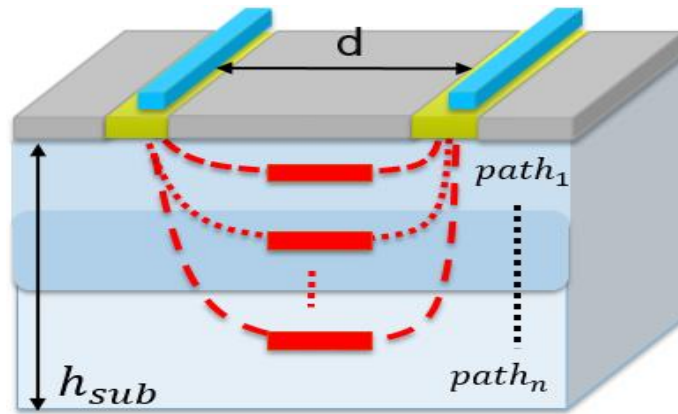


Figure II.16. Signal propagation between two ports within a silicon doped substrate based on the approximation of the half-ellipse model

The resistance  $R_i$  of each path is estimated by:

$$R_i = \rho \frac{P_i}{w \cdot h_i} \quad \text{where} \quad h_i = \frac{h_{sub}}{n} \quad (II-15)$$

in which  $\rho$  is the electrical resistivity of the substrate, w is the width of the port.  $h_{sub}$  is the thickness and the n is the approximate number of substrate paths.

The effective resistance between two contacts is the sum of the parallel resistors:

$$R_{eff} = \left[ \sum_{i=1}^n \frac{1}{R_i} \right]^{-1} \quad (II-16)$$

This methodology is not robust enough and the resistance value depends on the port's width.

The substrate based extraction methodology is then used and compared to full wave simulation in figure II.18. To evaluate the extraction accuracy and sensitivity to doping profile.

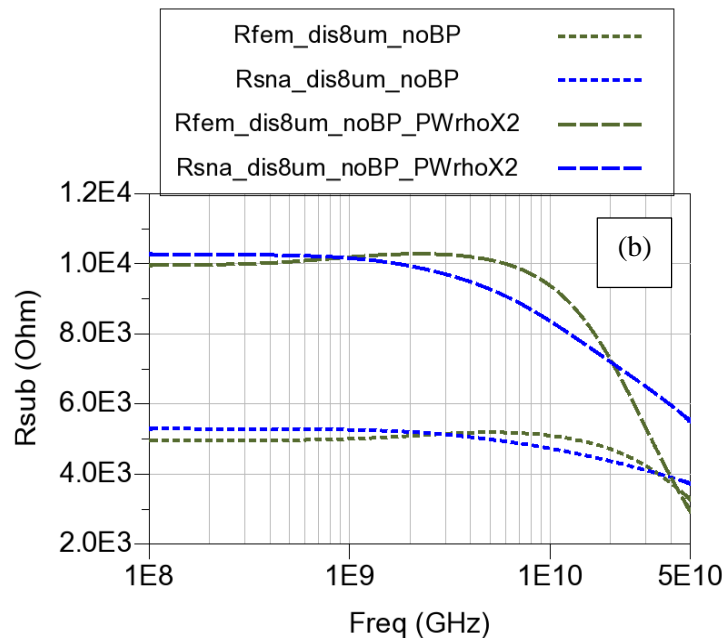
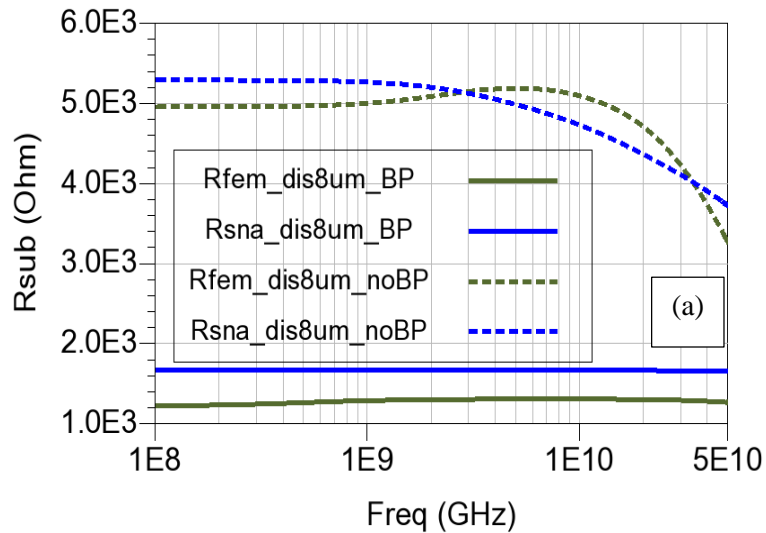


Figure II.17. Substrate resistances sensitivity evaluation : (a) impact of Buried layer (b) impact of the Pwell conductivity

In figure II.17 (a), the substrate resistance is extracted as function of the buried layer. The substrate resistance is  $\sim 2\text{K}\Omega$  in the case of the buried p vs a resistance  $\sim 5\text{K}\Omega$  without the buried layer. This is because of the higher conductivity of the buried layer.

In figure II.17 (b), we compare the substrate resistance function of the resistivity of the Pwell in order to evaluate the sensitivity of the extraction based methodology.

The Pwell conductivity were multiplied by 2 in the substrate extractor (we changed the doping profile information) and in EM layer stack.

The resistance is increased as expected and correlation with the full wave simulations is satisfying. The resistance significantly increases when the Buried layer is removed (figure II.16 (A)).

## II.4.4. Increasing the substrate impedance between ports

In this section, the impact of various isolation strategies is discussed. For simplicity reasons, substrate taps were chosen for this investigation.

Figure II.18 shows the structures that are designed using a BiCMOS technology. Each structure consists of two Ptap. One Ptap is the signal port and the other is grounded. This arrangement will give us a two port model which is very easy to understand. Furthermore, the effects on the substrate impedance of the number of rings of the deep trenches to break up Buried P layer on the can be investigated.

Table II.5 describes the test case under investigation in this section:

*Table II.5. Test case description*

|   |   |
|---|---|
| <b>Structure description:</b>             | 2 Ptap: <ul style="list-style-type: none"><li>• 1 Ptap inside the DTI → Signal port</li><li>• 1 Ptap place outside DTI → Ground</li></ul>                                     |
| <b>Active area (W x L)</b>                | 2 active areas are evaluated: <ul style="list-style-type: none"><li>• 20<math>\mu</math>m x 20<math>\mu</math>m</li><li>• 40<math>\mu</math>m x 40<math>\mu</math>m</li></ul> |
| <b>number of DTI rings between 2 Ptap</b> | 4 rings   |
| <b>Space between rings</b>                | 3 $\mu$ m   |
| <b>Measurement setup</b>                  | One-port test structure   |
| <b>Frequency</b>                          | 100MHz – 50GHz  |

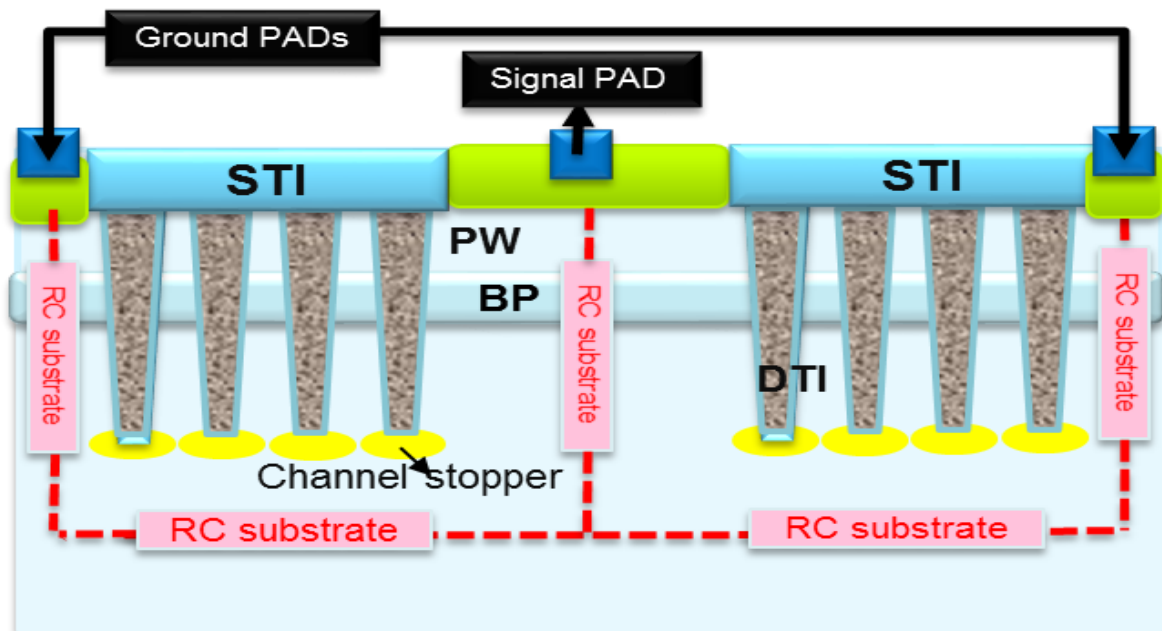
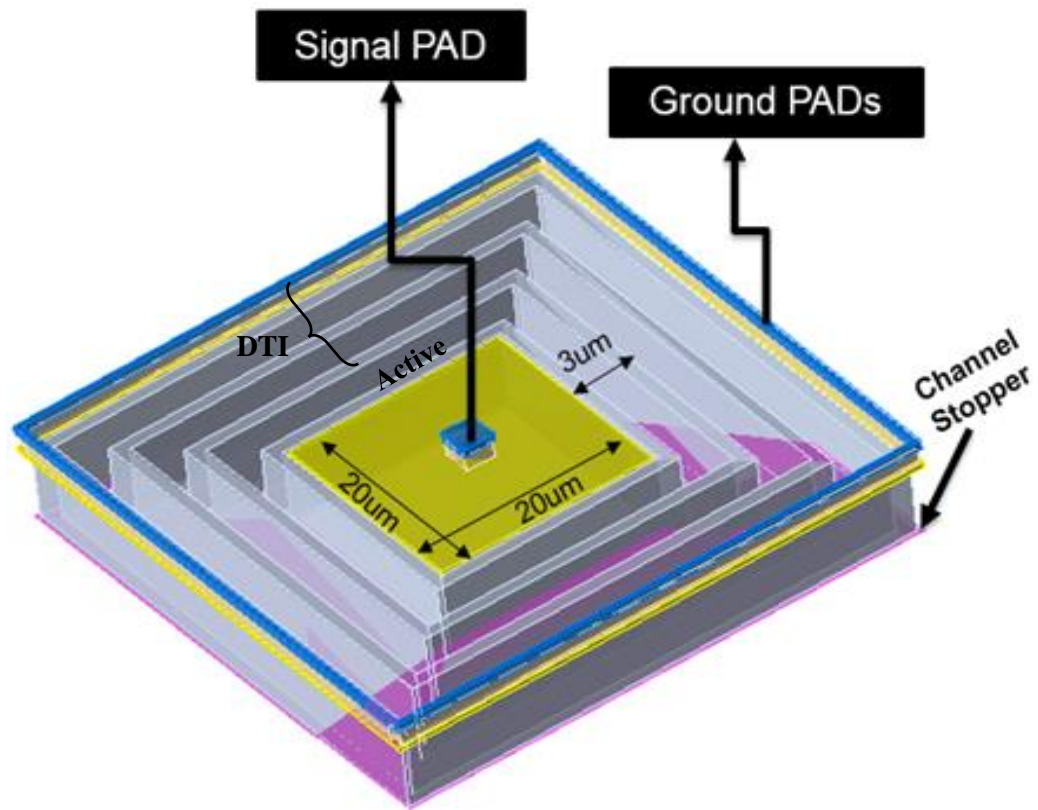


Figure II.18. Cross-section and top view of the example test structure: It has one PTAP placed inside the DTI rings and a second PTAP outside the DTI.

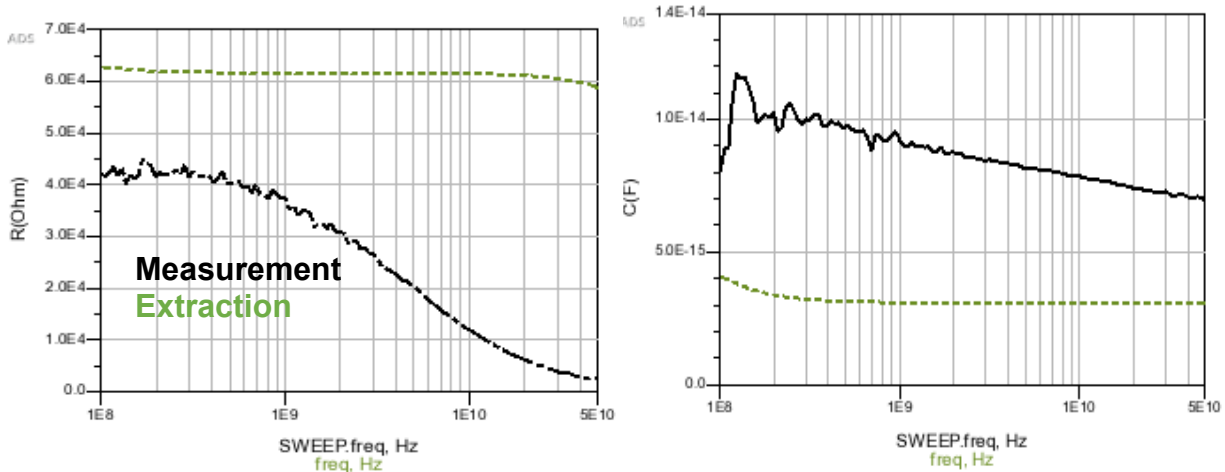


Figure II.19. Extracted (with SNA) substrate resistance and capacitance vs measured results

The first isolation introduced here is the Deep Trench Isolation. Those trenches create a silicon pieces that are completely separated. The formation of isolated trench that divides the silicon pieces between the signal ports and ground port, leads to a significant improvement in low frequency isolation (Figure II.20). However, at frequencies above 10 GHz, the level of isolation decreases due to the capacitive coupling across the trench.

The observed mismatch between extracted results and measurements for this simple structure, is due to the lack of lateral capacitance extraction through the DTI and the channel stopper effect (below DTI) in the substrate model (figure II.20 (b)).

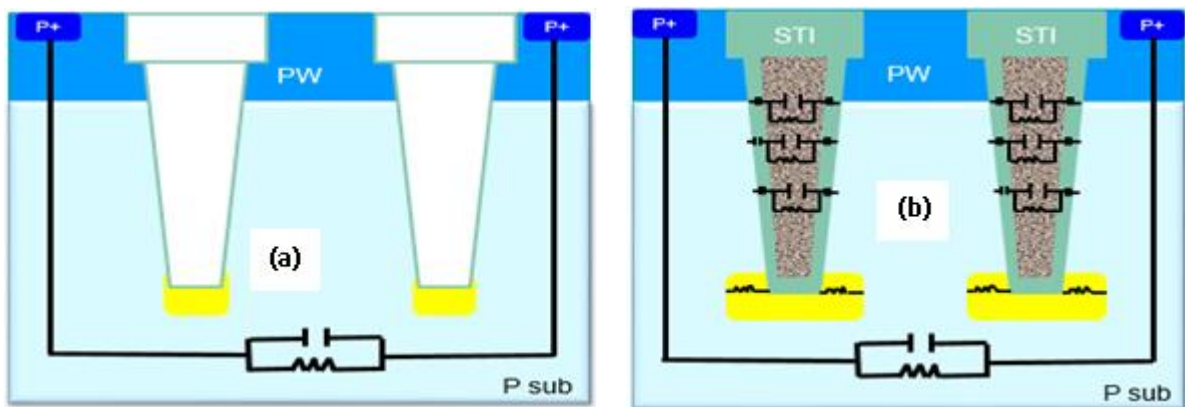


Figure II.20. Cross section of current DTI model (a) vs the accurate DTI model (b)

Based on these results, we worked with the tool vendor to validate improved modeling regarding the lateral capacitance of DTI.

#### a. Substrate extraction with the improved DTI model

After getting the updated model, a re-evaluation of different simple structures was studied. This shows that the improved modelling account correctly for the lateral capacitance through the DTI. The accuracy of this updated model is verified against silicon measurement. The evaluation was done in a first step on the same test case used in Figure II.19, and then extended to 3 layout variants structures varying the number of DTI rings (Table II.6).



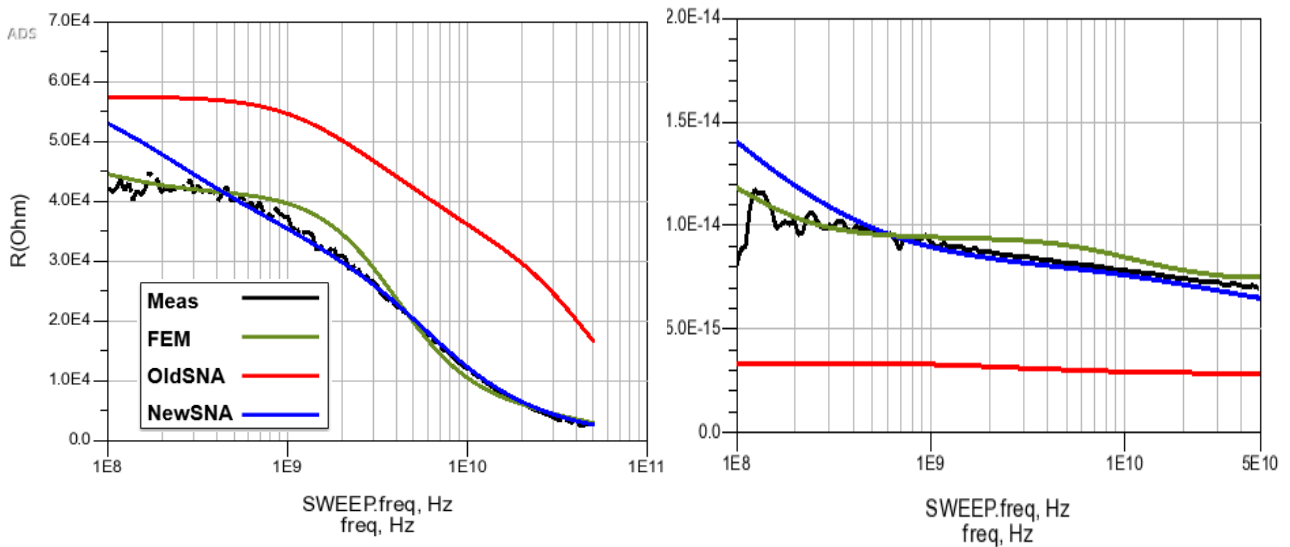


Figure II.21. substrate resistance and capacitance function of Area, extracted vs measured values:

area 20x20  $\mu\text{m}^2$

The extracted substrate capacitance and resistance is compared with measurement data, with EM simulation using Finite Element Method and previously extracted network. From available data obtained from updated extraction algorithm a good correlation with measurements can be proven.

**b. Impact of the number of DTI rings**

Three layout topologies were studied. We took the opportunity to vary the number of DTI rings which were positioned between the inner and the outer substrate:

- 2 rings between 2 ptaps
- 4 rings between 2 ptaps
- 6 rings between 2 ptaps

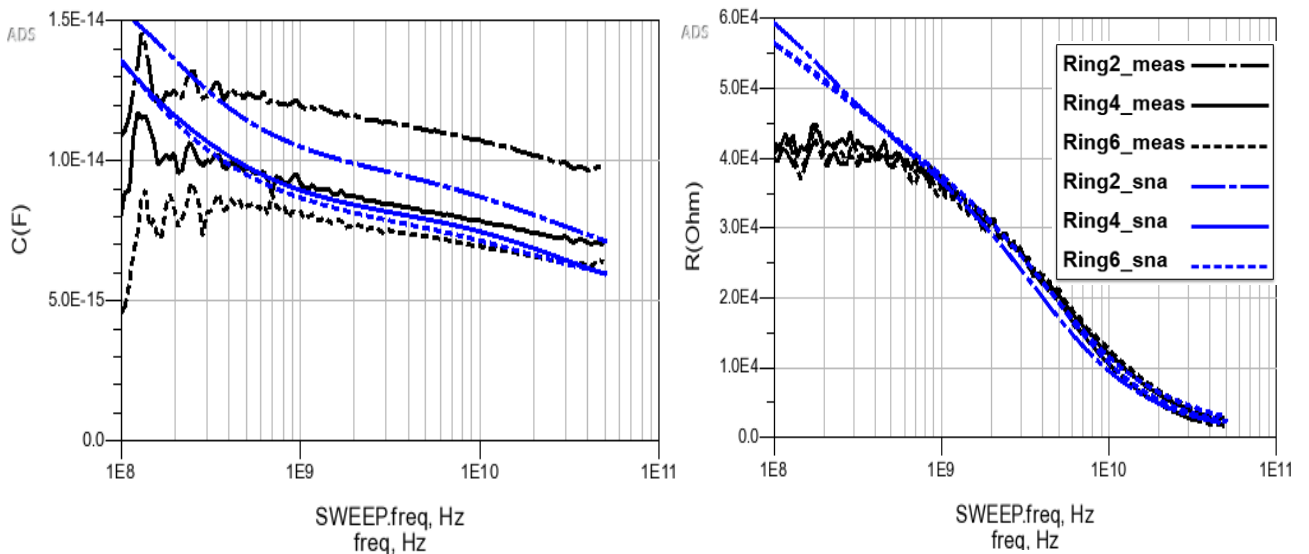


Figure II.22. substrate resistance and as capacitance function of the number of rings: extracted values vs measurements

The extracted substrate impedance as function of the number of rings was compared to measurements results (Figure II.23). The extracted impedance changes with the number of rings as expected

from measurements. The lower substrate capacitance is reached with the higher number of rings. However, the difference between 4 rings and 6 rings is weak.

The table II.6 presents the substrate resistance and capacitance values function of number of rings.

*Table II. 1. test case description as function of the number of rings*

| Structure description:  | number of DTI rings between 2 Ptaps<br>(Space between rings 3 $\mu$ m) | R(K $\Omega$ ) | C(fF) |
|---|--|----------------|-------|
| 2 Ptaps: <ul style="list-style-type: none"> <li>• 1 Ptap inside the DTI <math>\rightarrow</math> Signal port</li> <li>• 1 Ptap place outside DTI <math>\rightarrow</math> Ground</li> <li>• Active area: 20<math>\mu</math>m x 20<math>\mu</math>m</li> </ul> | 2 rings  | 12             | 10    |
|   | 4 rings  | 12             | 7.8   |
|   | 6 rings  | 12.6           | 7     |

From the obtained results it can be concluded that the substrate capacitance decreases when the number rings increases. The impact of the number of rings on the substrate resistance proved to be minor.

## Conclusions

In the previous section, various methods to reduce substrate coupling and to predict its behavior in the modelling phase have been proposed. The main criteria from the above discussions are to prevent substrate coupling and find out the best isolation strategy.

The measurement results of different topologies of a single test structure are presented. The test structures have different substrate isolation based on Deep Trench Isolation. The goal of this structures is twofold: the first one is to validate the substrate network extractor that was integrated in the design flow and second one is to compare the isolation structures based on Deep Trench Isolation and learn what isolation structures are most efficient for substrate coupling reduction as well as the design parameters involved, RF characterization procedures and de-embedding technique.

A good correlation is obtained between RF measurements and the developed methodology for inhomogenous substrate extraction. This methodology shows a predictable result at a single test cases (substrate contacts). In the next chapter, we will extend this evaluation at component level.

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# CHAPTER III: Applying isolation and modelling related techniques to nMOS switch device

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## Introduction

In this chapter, the role of Deep Trench Isolation on substrate coupling and consequently on the nMOS switch performance is analyzed. To support this investigation different layouts are analyzed.

The modelling methodology, based on the quasi-static approach developed in the previous chapter, will be investigated on component level. First the validity of this methodology is verified by comparing its results with a standard numerical method based on FEM (Finite Element Method). Subsequently all results are correlated with measurements.

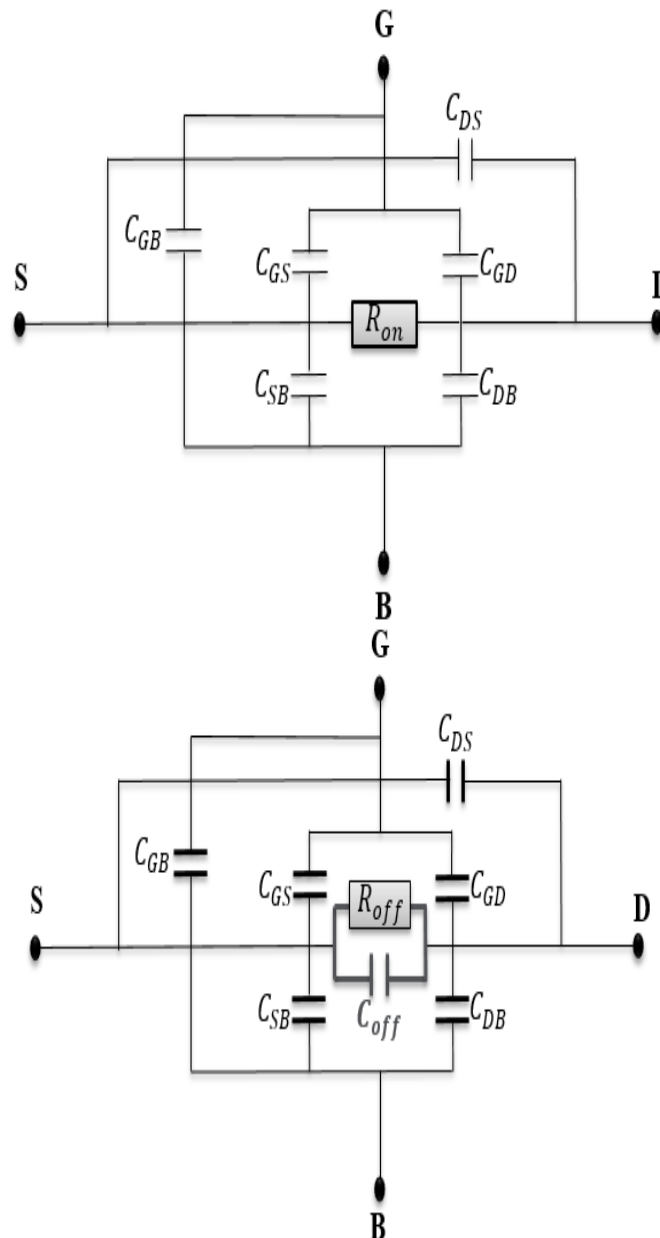
The substrate is usually described by means of RC networks. This approach is suitable for low frequency operation (for which the substrate impedance does not influence device performance). With increasing operating frequency, the substrate impedance becomes more and more frequency dependent and the Figure of Merit (FOM), which is for example  $R_{on} * C_{off}$  for a switch, must be adjusted to deal with substrate coupling. For mmWave operation, for instance, this mechanism can cause more than half of the loss in a switch[III-7].

On top of that coupling between different active devices can also jeopardize performance. This is typically a domain where compact models are not accurate anymore, as they don't take the layout environment of the actual device into account. There are of course several techniques to improve isolation (they will be discussed later in this chapter), but most important here is correct substrate layout extraction during the design phase. Often it relies on complex techniques such as FEM analysis. This modeling technique though is very time consuming and requires very often a high level of expertise. This chapter will focus also on the extraction methodology that we developed in order to speed-up extraction and ease of use.

Substrate isolation can also play a significant role in device linearity. As an example, consider ESD diodes on an RF input: these devices present a parasitic diode to the bulk substrate. If the substrate isolation strategy is not applied, it is really common to observe a strong degradation of the 1 dB compression point. This is again a typical case that we need to take care off during parasitic substrate extraction.

### III.1. The nMOS switch device

The basic function of the transistor is to control the current that flows between the drain and source by applying a voltage on the gate terminal. The gate is isolated from the p-doped substrate by a thin layer of an insulating material, usually  $\text{SiO}_2$ . When the gate voltage is increased above a certain threshold voltage,  $V_{th}$ , a conducting channel of electrons is formed in the p-doped area under the gate. This allows a current to flow between the highly negatively doped drain and source. This on-off model is an oversimplified view of the threshold voltage. The channel is built up gradually and a subthreshold current is flowing even below  $V_{th}$ . For proper operation, a voltage also must be applied to the substrate (bulk) to have a well-defined potential. A symbol of an nMOS transistor is shown in figure III.1.



(a) On-state equivalent model

(b) Off-state equivalent model

Figure III. 1 Schematic of a nMOS switch and its simplified small-signal circuit model of On (a) and Off (b) states



Figure III.1 (a) A simplified equivalent circuit of an nMOS transistor. The nMOS transistor is a four-port device.  $C_{js}$  and  $C_{jd}$  are junction capacitances of the source and drain junction diodes, and  $C_{gs}$  and  $C_{gd}$  are parasitic capacitances between the gate on one side and the source and the drain on the other side. There is a substrate-related impedance between the source/drain junction and the body node. This substrate network includes the vertical and the horizontal impedances (resistance and capacitance).

Ideally when the transistor is in its off state, no RF signals propagate from one terminal to the other (input to output). This is typically the case for low frequency signals. But at higher frequencies signals will leak from one terminal to the other due to the capacitive behavior of the P/N junctions of source and drain, and also due to the lossy behaviour of the silicon substrate. [II-1] (as shown in figure III.2).

Figure III.2 (a) shows the potential RF leakage paths (highlighted in red dashed lines) for an nMOS.

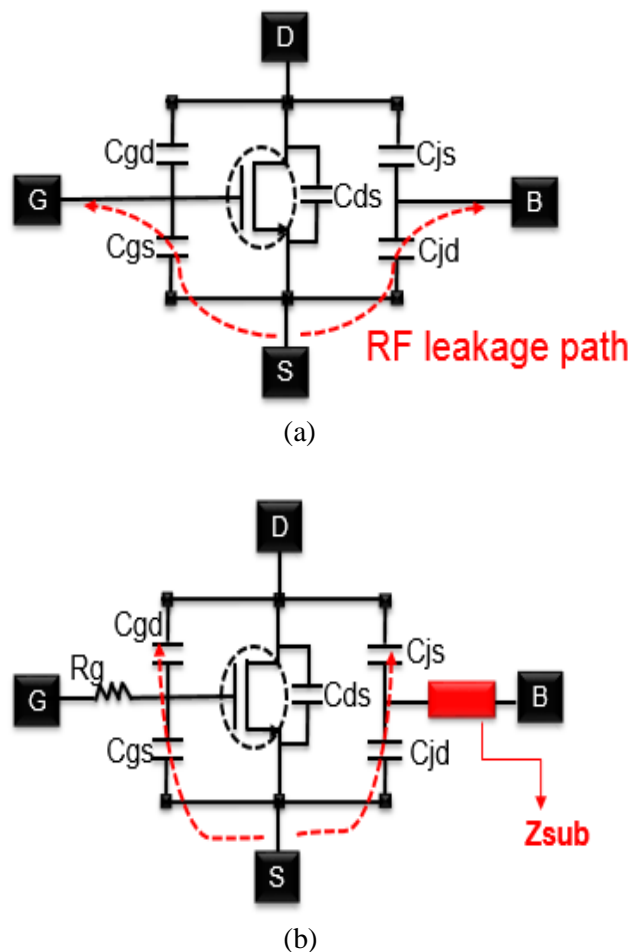


Figure III.2 nMOS transistor diagrams highlighting the parasitic devices and RF leakage paths for (a) nMOS device and (b) isolated nMOS with high substrate impedance

This type of structure (Figure III.2 (b)) provides added substrate isolation and body bias control through the PTAP. Because of this added isolation the substrate impedance increases, and the parasitic losses of the transistor are reduced. This minimizes the amount of RF leakage through the substrate, which in turn improves the insertion loss of the switch [III-1]. The purpose of  $R_g$  and

$Z_{sub}$ , shown in figure.III.2(b), is to minimize the fluctuations of  $V_{gs}$ , and  $V_{gd}$  at the source and drain terminals. In other words: the device robustness is increased by improving gate bias isolation [III-1] [III-2].

The nMOS compact model (PSP) available in the library is partitioned into the intrinsic model and the substrate model:

- The intrinsic MOS model. This models the equivalent circuit presented in figure III.2 ((a) and (b)).

The device has an accurate description of the off-state capacitance which is determined by the junction capacitance and the overlap capacitance.

- The isolation: the substrate model is based on a fixed configuration (DTI used in a ring structure) with 2 variables: the number of rings and the spacing between the rings.

The substrate effect inside the compact model predicts the device behaviour at schematic level.

The main drawbacks of this compact model with its substrate circuit are: the fixed isolation strategy (DTI ring) and the lack of taking coupling to other devices into account. In other words: the model does not know the environment of the nMOS switch in the layout.

The necessity of a methodology to predict the substrate behaviour at device, IP and chip level appears whatever the isolation technique applied.

### III.1.1. Substrate body tuning technique in BiCMOS switches

Compared to the GaAs process, Si-technology has a critical disadvantage in terms of the power-handling capability. When the peak-to-peak value of a small signal voltage swing is smaller than the threshold voltage of the junction diodes, the existence of the junction diodes doesn't affect the power-handling capability of the switch. However, once the level of the input voltage swing exceeds this threshold voltage, the input signal starts to be distorted. This can limit the power handling capability of the switch. Without resolving this issue, the BiCMOS switch cannot be used for high power applications.

Figure III.3 shows configurations of the body floating technique [I-7] [II-5]. As can be seen in figure III.3 (b), an RC circuit is connected at the substrate bulk port in the nMOS device. This RC circuit provides a very high impedance to the bulk port. This ensures that the portion of the impedance of the junction diode and the junction capacitor becomes relatively small in the overall impedance between the source port and ground. When the voltage swing of the applied signal to the switch exceeds the turn-on voltage of the junction diode, the voltage level between the source or the drain and the bulk port is divided by the ratio of the impedance between the RC network and the junction capacitors. Consequently, only a smaller portion of the voltage swing is applied to the junction diode, so that the junction diode does not turn on even at a large signal negative voltage swing.

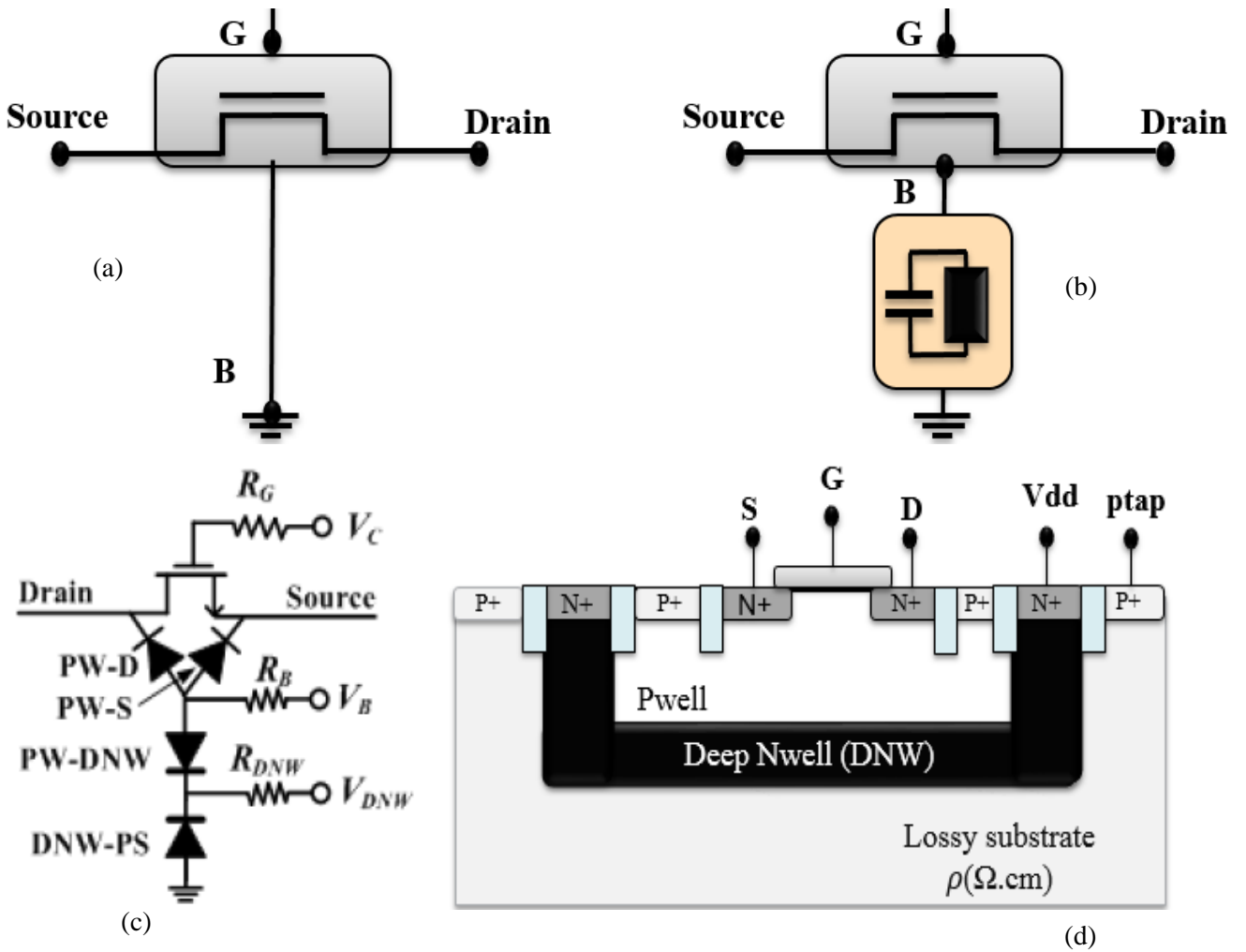


Figure III. 3 (a) Standard switch. (b) switch with body floating using RC network (c) switch using body floating technique using Deep N-well process and (d) Cross section

The body floating technique is implemented in the triple-well nMOS device [II-17] [II-18]. The triple-well nMOS devices can provide perfect isolation between the substrate body of one device and another device[II-6] [III-1]. However, the high parasitic capacitances limit its functionality at mmWave frequencies. The schematic configuration of the body floating technique, as implemented in the triple-well nMOS device, is shown in figure III.3 (c)

### III.1.2. Test case descriptions

In this section we explore RF nMOS switch designs in a commercially available 0.25  $\mu\text{m}$  SiGe BiCMOS technology. The focus of this work is to design high isolation, low-loss switches for integration between the antenna and the PA and LNA in wireless front-end applications. The challenge consists of designing a low loss switch using a longer channel length technology (0.25  $\mu\text{m}$ ), while maintaining adequate isolation, and pushing for higher linearity.

The nMOS switches were designed using the topology highlighted in figure.III.4. To improve insertion loss, an isolated nMOS device is surrounded by Deep Trenches. The isolated p-well is achieved by floating the bulk of the nMOS device, reducing parasitic losses by increasing the effective substrate impedance in the body of the device.

The optimization of switches for a specific application involves appropriate selection of device geometry. The geometry selection provides a balance in trade-offs between the on-state device resistance ( $R_{on}$ ) and the off-state parasitic capacitances ( $C_{off}$ ).  $R_{on} \cdot C_{off}$  is the Figure of Merit for nMOS switch designs. The devices were sized to maximize isolation and to provide lower insertion loss at the bandwidth of interest (100 MHz to 20 GHz). The transistors width was selected to be 300  $\mu\text{m}$  using the minimum gate length of 0.25 $\mu\text{m}$ . The source and drain of the devices were biased in a deep-off mode. Table III.1 shows the applied bias conditions:

Table III. 1.nMOS switch bias configuration

| nMOS switch | Vg (V) | Vs (V) | Vd (V) | Vb (V) |
|-------------|--------|--------|--------|--------|
| On          | 2.5    | 0      | 0      | 0      |
| Off         | 0      | 2.5    | 2.5    | 0      |

The gates of the transistors are RF-floating by the use of a high resistors value 80 k $\Omega$  [II-2]. This technique is applied to isolate the gate nodes from RF ground, thus improving the insertion loss of the switch and this helps to improve dc bias isolation. The gates were controlled using 2.5V source to turn-on or off the switch.

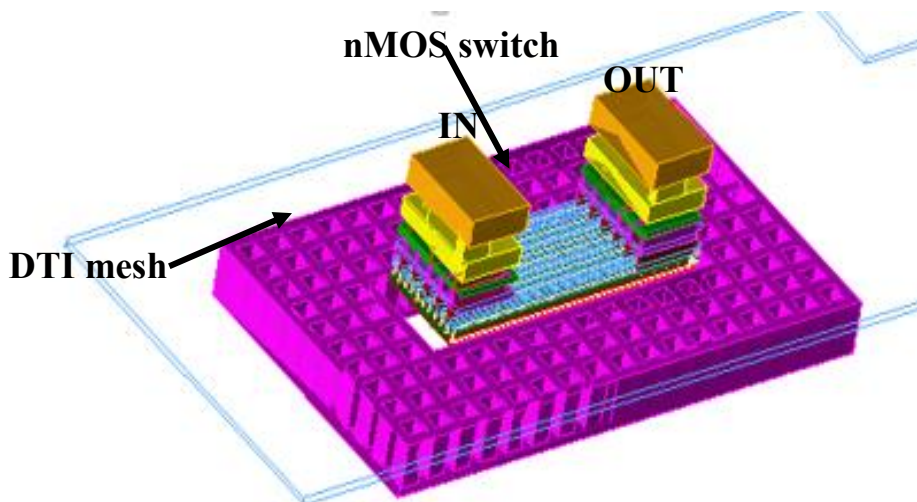


Figure III.4. Top view of nMOS switch with DTI mesh

The scattering parameters of the two-port measurements are performed over a frequency range of 100 MHz-10 GHz., This was done using an RF probe station and vector network analyzer (VNA) (Figure III.5) [II-3].

Calibration has been done to remove the errors coming from wires and RF connectors of VNA. In order to remove the wafer probing parasitic, an Open-Short-Load de-embedding technique was done.

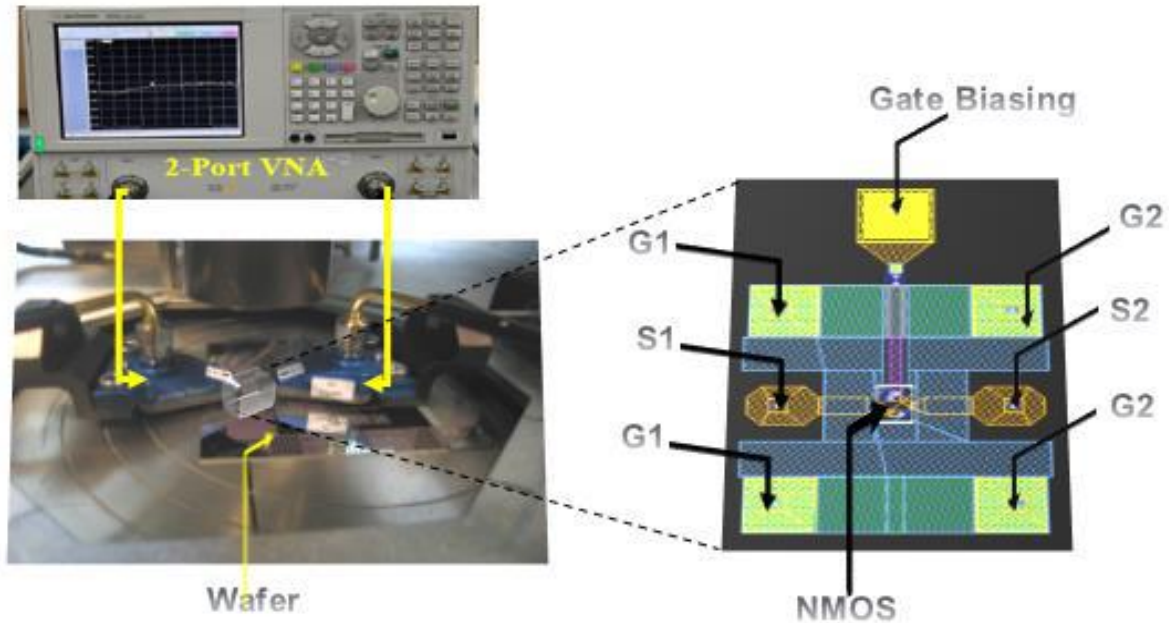


Figure III.5. Measurement set-up of nMOS switch

#### III.1.4. RF measurements results and Discussions

To illustrate the impact on an isolated nMOS switch. A comparison between post layout simulation of an nMOS and measurement results was done and is presented in Figure III.6 and table III.2. The behavior of the intrinsic transistor part is controlled by the device model, and the layout environment is captured using a Parasitic Extraction tool (PEX). The nMOS is biased either in on-mode or in deep-off mode ( $V_g=0V$ ,  $V_d = V_s = 2.5V$ ).

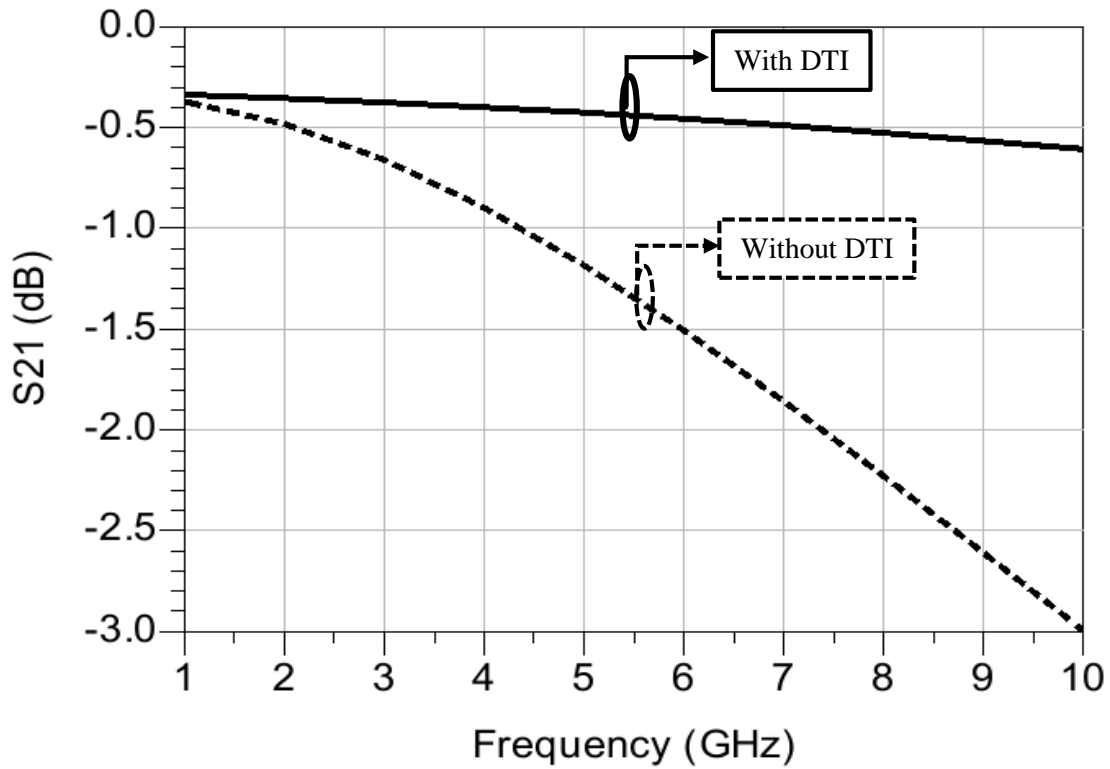


Figure III. 6. Insertion loss of nMOS structure with DTI vs without DTI

Promising results are obtained for the modeled nMOS with DTI. The Insertion Loss from the model with DTI is 0.43 dB, whereas the model without DTI predicts 1.2 dB.

In table III.2, below, comparison results at 5GHz are shown.

Table III.2. Measurement with DTI vs without DTI

| At 5GHz                | Measurements | Model_DTI | Model_noDTI |
|------------------------|--------------|-----------|-------------|
| Insertion Loss (dB)    | -0.42        | -0.43     | -1.2        |
| Input Return Loss(dB)  | -22.5        | -22.8     | -9.8        |
| Phase IRL (°)          | -73          | -75       | -109        |
| Output Return Loss(dB) | -22.4        | -22.8     | -9.8        |
| Phase ORL (°)          | -72          | -75       | -109        |
| Ron ( $\Omega$ )       | 3.7          | 3.7       | 3.89        |
| Coff (fF)              | 122          | 120       | 70          |

### III.1.5. FEM modelling to account for substrate effect

The measurement results are corrected using Thru-Open-Short de-embedding. Therefore, in simulation, the same method must be applied to be able to compare the results

To validate the substrate layer stack properties and the accuracy of EM simulation, we first start with a passive structure. The Open structures used for de-embedding was used for this analysis.

Simulation ports must be defined as close as the GSG configuration used in measurement (Figure III.7).

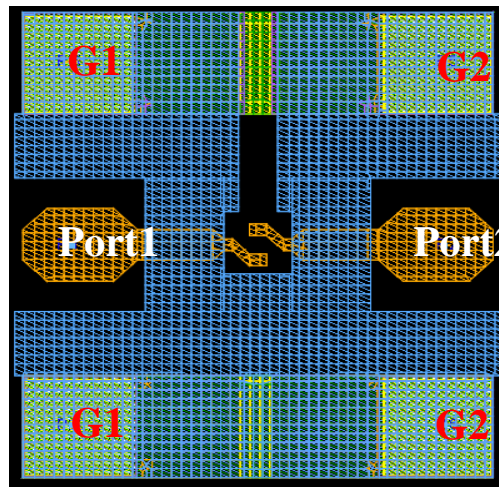


Figure III.7. Open structure simulated with momentum

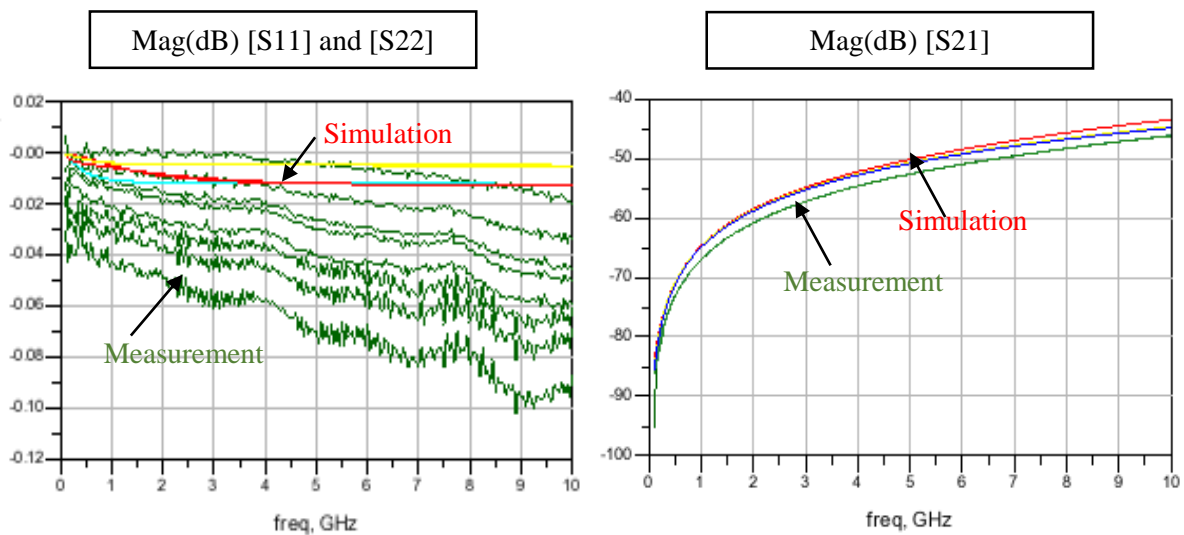


Figure III.8. Measurement vs simulation  $S_{xx}$  and  $S_{21}$

The results of  $S_{xx}$  obtained by EM simulation are compared with different measurements (Figure III.8). There is uncertainty on measurements. It seems that the positions of Probes can indeed lead to significant discrepancies.

After the validation of the EM simulation results obtained in the Open-Short test structures, now we need to include the intrinsic device using a partitioning methodology.

The proposed partitioning methodology is applied to accurately capture all the extrinsic passive parasitics. This strategy is described in Figure III.9. It combines two main tools RC extraction and Electromagnetic (EM) simulations. The nMOS switch was designed in a commercial layout environment and then transferred to an Electromagnetic solver to obtain S-parameters. Once these simulation results are obtained, re-simulation in a commercial circuit simulator can be done, but only in the frequency domain of EM analysis.

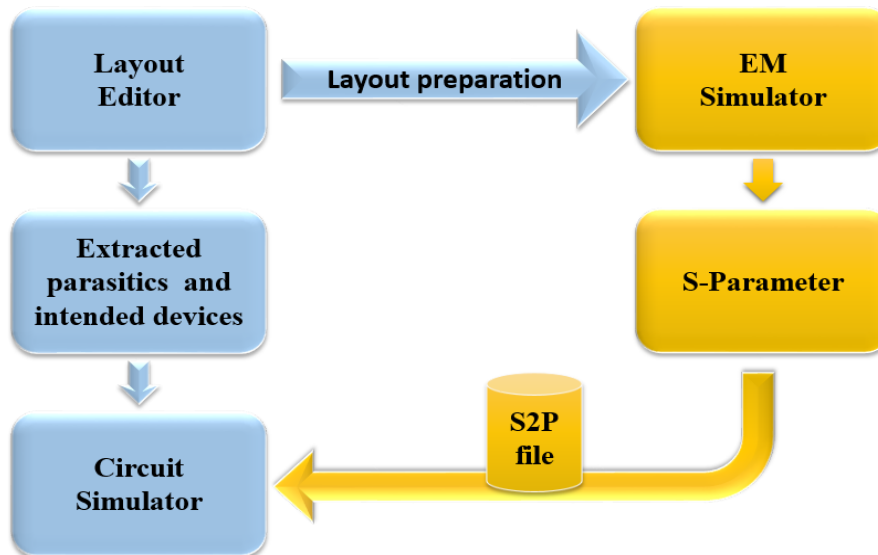


Figure III.9. Synoptic figure of the considered extraction flow

The following phases are required to achieve the adequate results. First, the structure is subdivided into two blocks:

- **RC block:** The extraction procedure needs to have a good understanding of the device model boundaries, in order to capture all the interconnect parasitic missing in the device model without any double counting parasitic effects that are already accounted for in the device model.

**EM block:** This part models the substrate impedance with high accuracy taking into account the frequency dependency. Before transferring the layout from the layout editor to the EM solver, some simplifications have to be done to make sure that only the substrate network which is missing in both device model and parasitic extraction tool (PEX) is taken into account. All backend metallization layers from metal 2 up to metal 6 were removed, except the metal1 that is part of the substrate pin (P-TAP).

A strong awareness and precision are required to define the substrate layer stack for Electromagnetic simulation, taking into account Deep Trench Isolation, channel stopper, buried layer and substrate pin position. On top of that, the non-uniform substrate resistivity profile through the whole thickness of the substrate (650  $\mu\text{m}$ ) is considered.

Two ports of excitations were used: one port was applied to substrate pin (P-TAP) which is connected to the ground. The second port was connected to the bulk of the mos. Thus, the accurate parallel resistance and capacitance are derived from the S-parameters.

Then, it is mandatory to combine the resulting EM simulation with the RC block to obtain the global response of the structure, as described in Figure III.10.



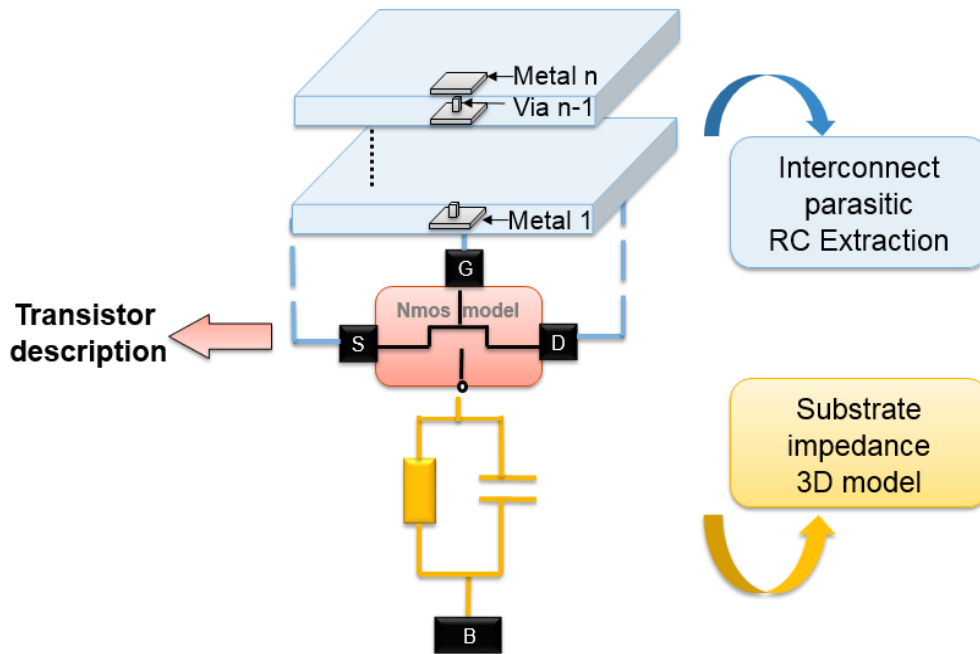


Figure III.10. Partitioning technique and reconstitution of sub-blocks

### III.1.6. Measurement/simulation correlations

This section is dedicated to the comparison of S-parameters obtained using the proposed partitioning methodology with the measurements results of three samples

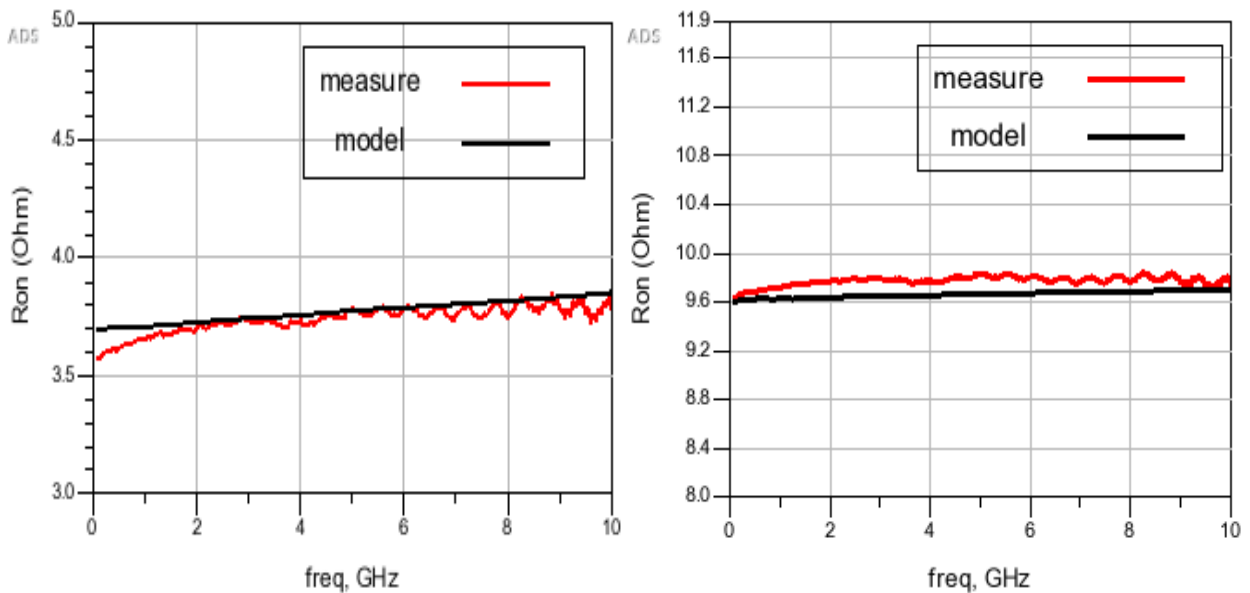


Figure III.11. Measured vs. simulated Ron: a)  $W=300 \mu\text{m}$ , b)  $W=107 \mu\text{m}$

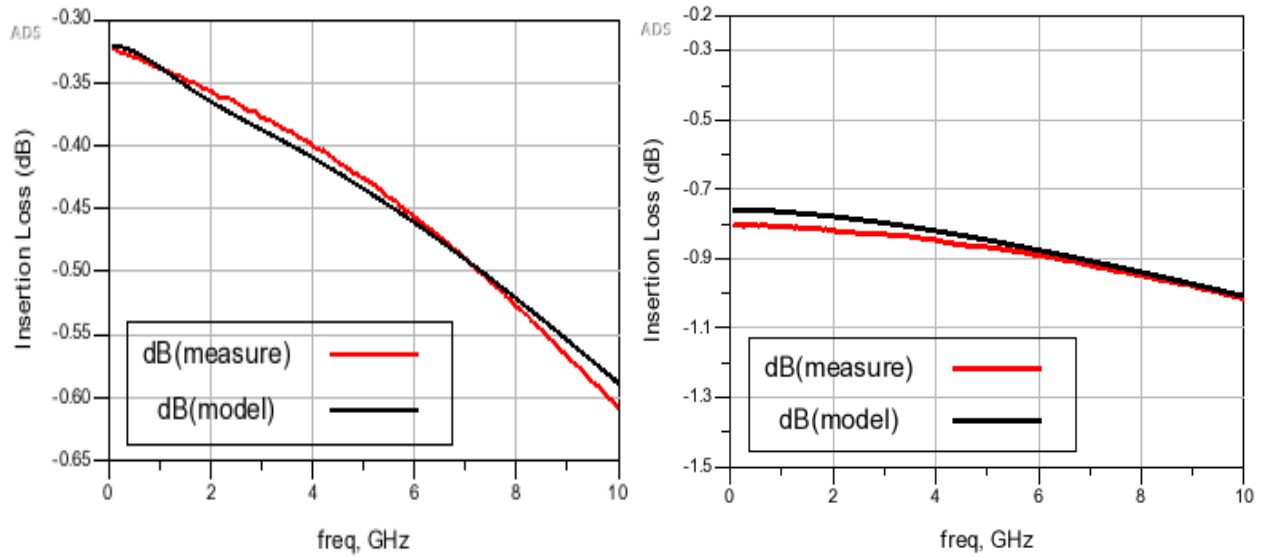


Figure III.12. Measured vs. simulated IL as a function of frequency: a)  $W=300 \mu\text{m}$ , b)  $W=107 \mu\text{m}$

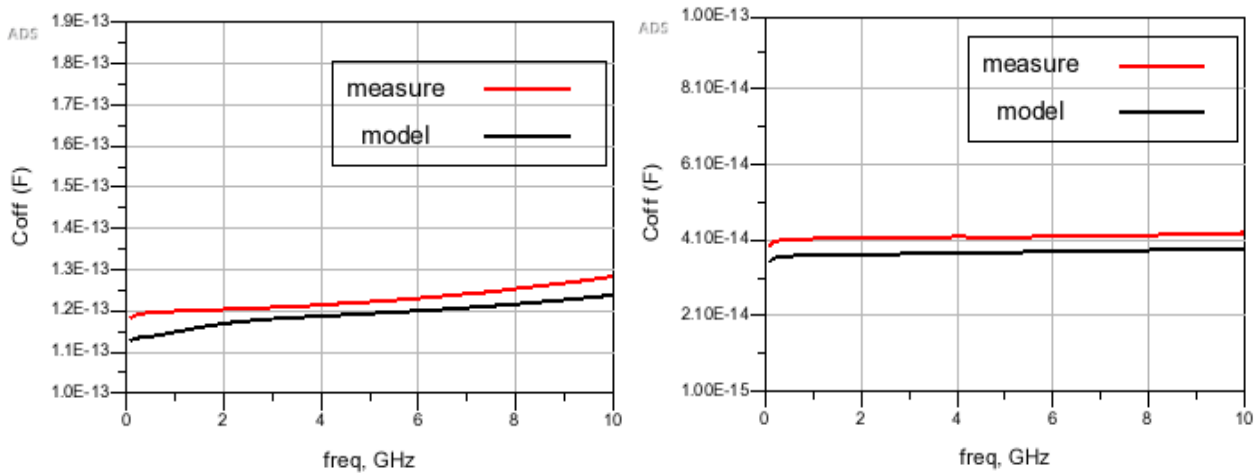


Figure III.13. Measured vs. simulated Coff as a function of frequency: a)  $W=300 \mu\text{m}$ , b)  $W=107 \mu\text{m}$

Promising results are obtained for both geometries, less than 20 m dB of difference is guaranteed for the Insertion Loss. Concerning the isolation, the Coff is in good agreement with measurement. In the table below, a comparison between the resulting partitioning methodology and the measurements is illustrated respectively at 2.4 GHz and 5.8 GHz

Table III.3. Simulation vs measurement of nMOS switch at 2.4GHz

| 2.4 GHz              | MOS width=300 $\mu$ m |        |            | MOS width=107 $\mu$ m |       |            |
|----------------------|-----------------------|--------|------------|-----------------------|-------|------------|
|                      | measure               | Model  | $\epsilon$ | measure               | Model | $\epsilon$ |
| IL (dB)              | -0.36                 | -0.37  | 0.01       | -0.82                 | 0.82  | 0.01       |
| Phase ( $^{\circ}$ ) | -3.6                  | -3.6   | 0          | -3.1                  | -2.9  | 0.2        |
| In.RL (dB)           | -26 dB                | -26 dB | 0.4        | -20.7                 | -21   | 0.4        |
| Phase ( $^{\circ}$ ) | -48                   | -53    | 4.6        | -18.6                 | -24   | 5.4        |
| Out.RL (dB)          | -26                   | -26    | 0.5        | -20.7                 | -21   | 0.4        |
| Phase ( $^{\circ}$ ) | -77                   | -79    | 2.1        | -19.5                 | -24   | 4.8        |
| Ron ( $\Omega$ )     | 3.7                   | 3.7    | 0          | 9.825                 | 9.645 | 0.18       |
| Coff (fF)            | 120                   | 118    | 2          | 42                    | 44    | 2          |

Table III.4. Simulation vs measurement of nMOS switch at 5.8GHz

| 5.8 GHz              | MOS width=300 $\mu$ m |       |            | MOS width=107 $\mu$ m |       |            |
|----------------------|-----------------------|-------|------------|-----------------------|-------|------------|
|                      | measure               | Model | $\epsilon$ | measure               | model | $\epsilon$ |
| IL(dB)               | -0.45                 | -0.45 | 0.004      | -0.88                 | -0.88 | 0.01       |
| Phase:               | -8.3                  | -8.2  | 0.1        | -7.5                  | -6.8  | 0.7        |
| In.RL (dB)           | -21.5                 | -21.8 | 0.3        | -19.7                 | -19.4 | 0.3        |
| Phase ( $^{\circ}$ ) | -78.0                 | -79.8 | 1.8        | -44.0                 | -50.9 | 6          |
| OutRL (dB)           | -21.5                 | -21.8 | 0.3        | -20.7                 | -21.1 | 0.4        |
| Phase ( $^{\circ}$ ) | -77.8                 | -80   | 2.2        | -43.9                 | -50.9 | 7          |
| Ron ( $\Omega$ )     | 3.7                   | 3.7   | 0          | 9.837                 | 9.671 | 0.166      |
| Coff (fF)            | 122                   | 120   | 2          | 42                    | 45    | 3          |

Measurements results and the partitioning methodology simulation leads to good agreement with modeling.

A predictable extraction methodology based on a Full wave approach, in order to predict the influence of substrate coupling of RF nMOS switch was discussed. The modelling methodology of the RF nMOS switch exhibits a good agreement between measured and simulated results. A difference of 0.01 dB on insertion loss and a difference in Coff less than 3fF for two different geometries have been obtained.

The available computed results confirmed the hypothesis that the main issue for this circuit is coming from the lack of substrate modeling. However, its computation is not user friendly due the fact that is not well embedded in current design flow and requires expertise.

## III.2. DTI effect on nMOS switch performances

### III.2.1. Design description

The use of Deep Trench Isolation (DTI) exhibits interesting isolation capabilities [I-6] [I-5]. This kind of isolation is commonly used under inductors and other passive devices [I-6]. Nevertheless, its implementation still depends too often on empirical approaches and the literature is rather silent as to its optimal use in the design. This technique is also helpful to isolate, in one hand the bulk of the nMOS from the substrate tap, and on the other hand the different transistors from one to each other in RF switch, LNA and PA's. Here again, there is no widespread practice published about its best implementation in terms of layout topology.

Notwithstanding, the presence of the DTI leads to inhomogeneous structures in the substrate layer stack. This requires an EM analysis in the space domain coupled to a very thin mesh and therefore excessively computing time (Finite Element Method-FEM). 2.5D MoM methods (Method of the Moment) can be also used but show strong limitations when anisotropic substrate like DTI must be addressed.

In this section, we present different layout variant of a nMOS switch to demystify the DTI use model for insertion loss, noise reduction and isolation improvement. These different test-cases are then evaluated with the help of the new quasi-static tool presented in the previous section. I examine various nMOS design and layout optimizations for the nMOS device, to determine its effectiveness and impact on the nMOS switch performance. These design and layout changes attempt to significantly increase or decrease the substrate impedance ( $Z_{sub}$ ) by incorporating on-chip polysilicon-based resistors, additional substrate contacts, and deep-trench isolation structures in the switch design. The nMOS switch consists of the same core design with a width of 1 mm.

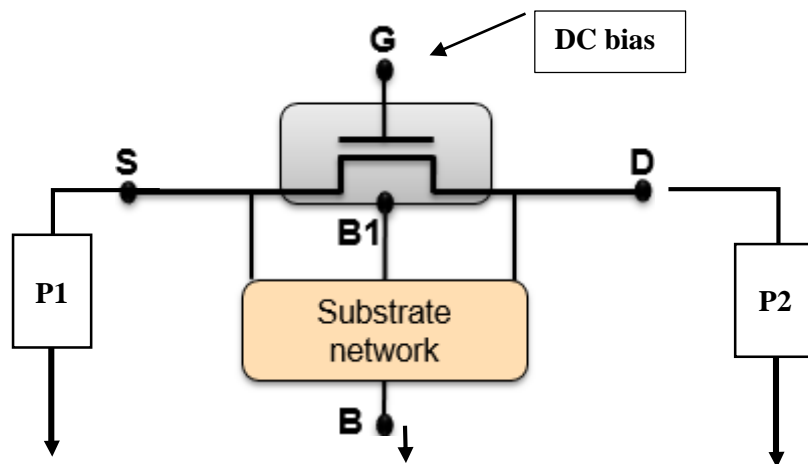


Figure III. 14. Schematic of isolated nMOS switch

The nMOS device is essentially 4 terminals, 2-port device. For our purpose, the source and drain terminals form the input and output ports, respectively. The gate of the nMOS is RF-floating by adding a very large resistor (80 K $\Omega$ ) to avoid the gate breakdown due to the large RF signal swing.

The bulk terminal is connected to a high substrate network (Bootstrapping technique) as illustrated in Figure III.14 so that the gate and bulk nodes of the nMOS are RF-floating (bootstrap technique).

To investigate the effects of the deep trench isolation performances in substrate coupling reduction, the test case structures shown in Figure III.15 are extracted using the proposed methodology based on a Quasi-static approach. Goal of layout variant is put in obviousness the impact of different substrate impedance on the total losses of the device.

In the first test case structure of Figure III.15 (a), the nMOS switches with the associated substrate tap are not isolated. This structure is used for reference purpose. The second test case in Figure III.15 (b, c and d) represents an isolated nMOS switch using DTI rings (1, 2 and 3)

The options without DTI correspond to the reference structures with the BL (assuming the nominal values for the conductivity (1000 S/m) and thickness (1  $\mu\text{m}$ )).

The last test case evaluated in Figure III.15 (a) is without DTI and without the buried layer under the active area, and with an additional option without the Pwell around the active area.

Table III.5 presents the overall test cases under evaluation with the corresponding isolation technique.

*Table III.5. Test cases description*

| Structure description                    | Isolation technique  |                  |
|--|--|------------------|
| Reference structure                      | No isolation   | FigureIII.15 (a) |
| Isolation without DTI                    | A Ring of Buried p and Pwell mask block<br>→ The Buried p and the Pwell are removed around the device. | FigureIII.16     |
| Isolation using various DTI rings number | 1 ring   | FigureIII.15(b)  |
|  | 2rings   | FigureIII.15 (c) |
|  | 3 rings  | FigureIII.15(d)  |
| Structure using 2 rings DTI              | 2 $\mu\text{m}$  | FigureIII.19(a)  |
|  | 5 $\mu\text{m}$  | FigureIII.19(b)  |

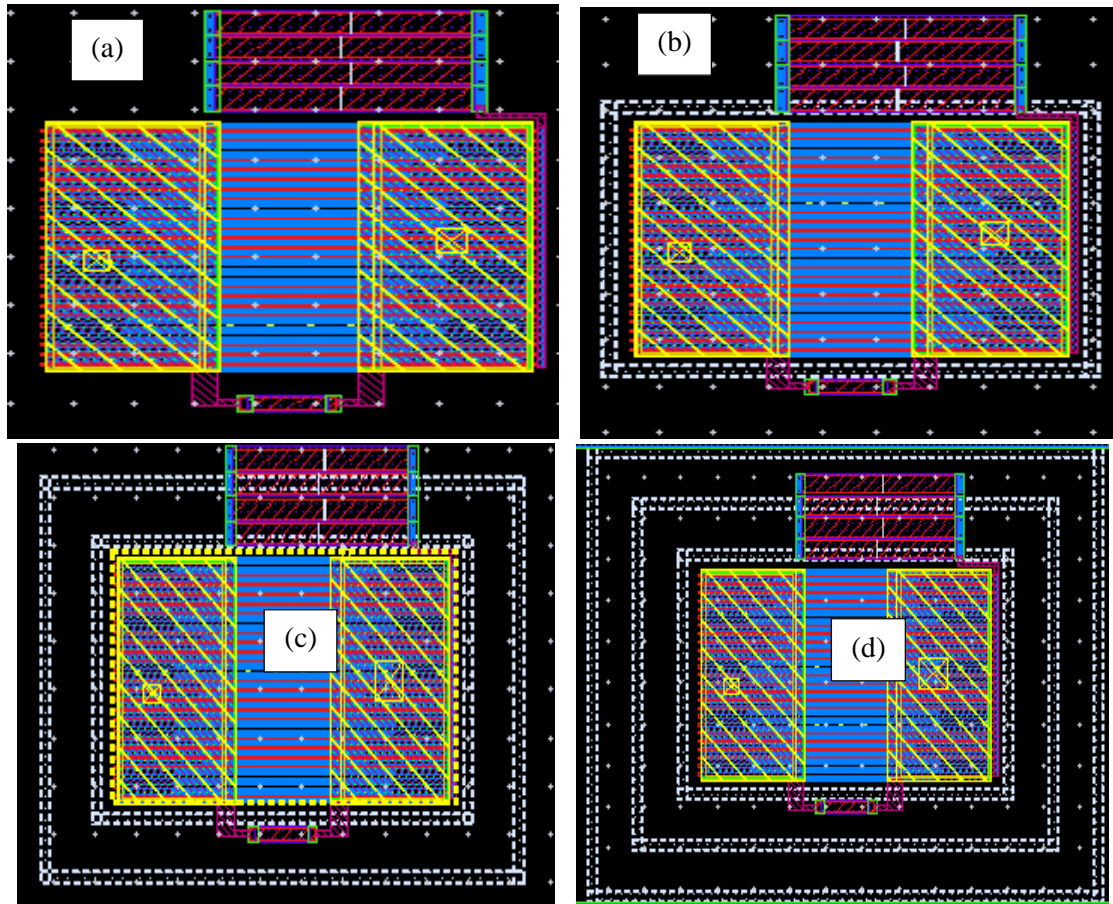


Figure III.15. Top view of the isolated nMOS function of number of DTI rings(b,c,d) and the reference structure without DTI (a)

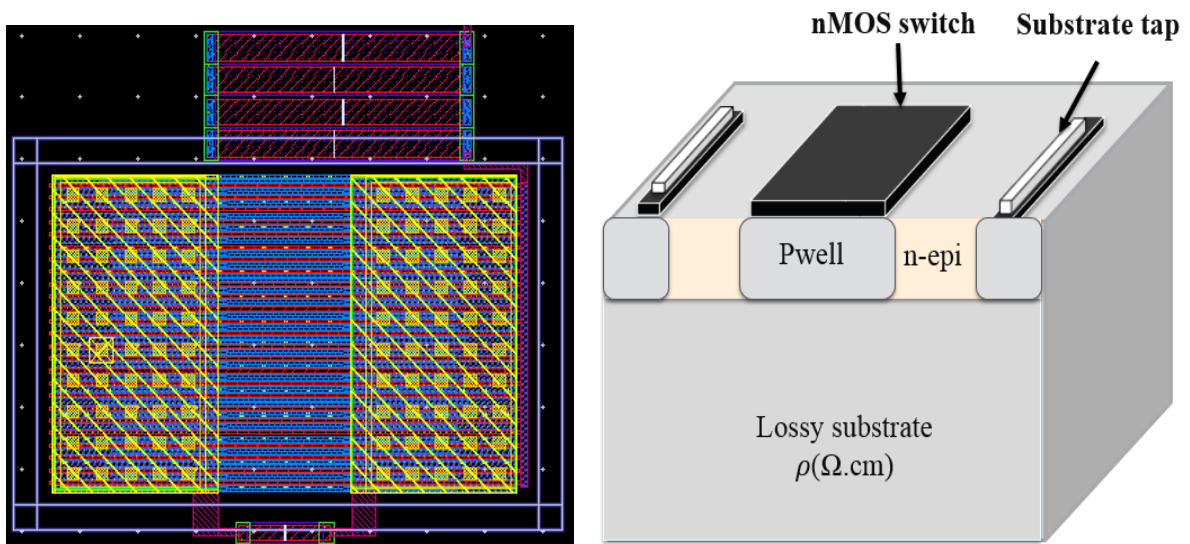


Figure III.16. Top view of the isolated nMOS without DTI and without BP/Pwell (a) and top view (b)

### III.2.2. Measured Results for the nMOS Devices

#### a. DTI influence on nMOS device

The S-parameters of the series nMOS device were measured at wafer level, with the pad parasitic de-embedded using standard open-short de-embedding.

The  $S_{21}$  of the device can be seen in Figure.III.15 (a), with the gate-source voltage (VGS) biased at 0V and 2.5V to evaluate their transmission and isolation capabilities.

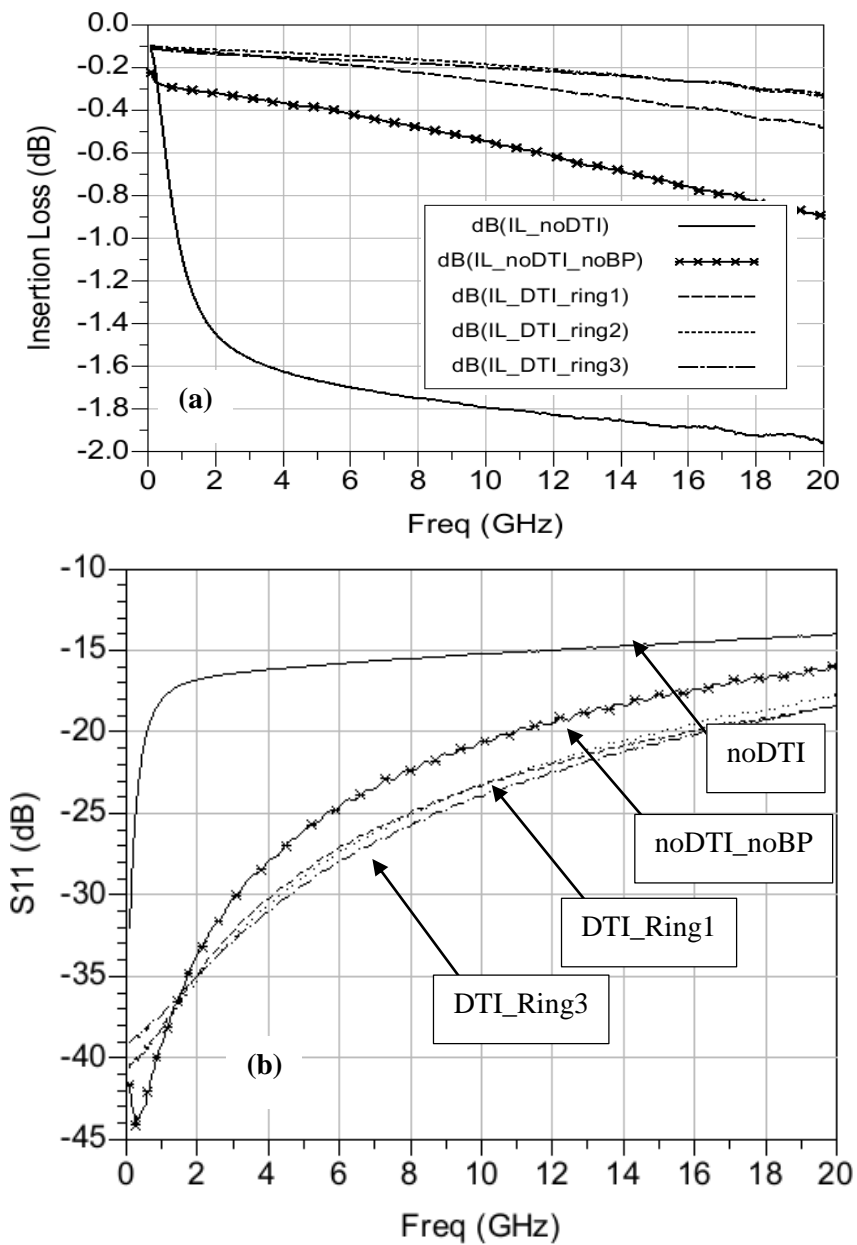


Figure III.17. Measured variations against frequency of  $S_{21}$ (a) and  $S_{11}$  (b) in on-state

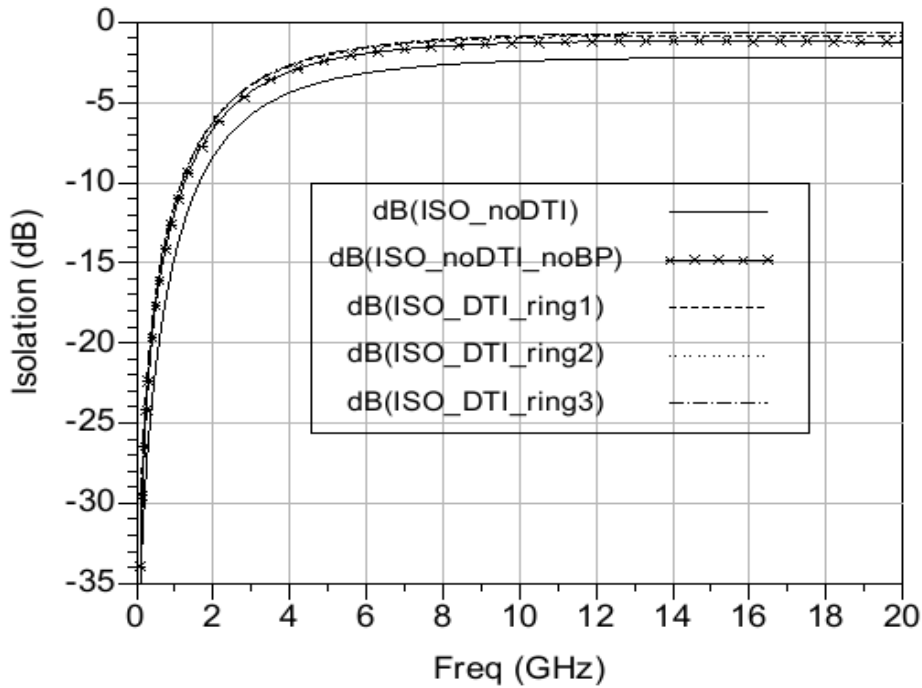


Figure III.18. Measured variations against frequency of isolation in off-state

The impact of a deep trench isolation on the insertion loss, input/output return loss and isolation against frequency is presented in figure III.17 and III.18 in reference to deep trench rings options shown in Figure III.15 (b, c, d), without BP/Pwell (Figure.III.16) and in comparison, with a reference structure without deep trench patterning (Figure.III.15 (a)).

These results highlight the impact of the deep-trench isolation ring on the high-substrate devices. The interruption of the BL and part of the silicon substrate by DTI leads to better isolation performances.

In addition, this DTI ring around the nMOS increases the substrate impedance, minimizing the loading effects of the parasitic drain-substrate and source-substrate capacitances in loading the device. but adding more than 2 DTI rings has a marginal impact on overall performances.

For WLAN applications [2.4GHz – 5.8GHz], the use of 1 ring seems to be sufficient. From the obtained results, at 2.4GHz, the difference between insertion loss with the increased number of rings is weak. This can help to have a satisfactory performance and footprint layout

#### b. DTI ring's space impact on nMOS device

We have seen that by increasing the number of rings we improve the switch performances; it has been observed that the use of DTI with 3 rings has more usability.

In this section, we evaluated the impact of the deep trench ring spacing. Two options are shown in Figure III.19:

- DTI 3rings with a space of 2 $\mu$ m between rings
- DTI 3rings with a space of 5 $\mu$ m between rings



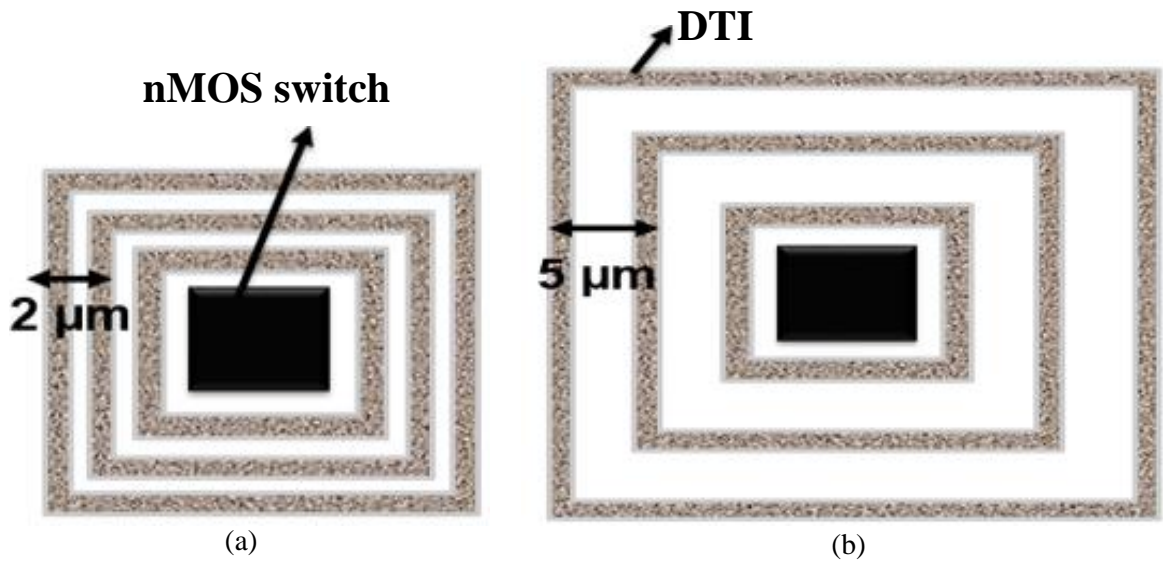


Figure III.19. Top view of the isolated nMOS function of DTI ring space

The Figure III.19 illustrate the separation of 5um between 2 rings versus 2μm.

The measurement result showing the influence of DTI ring spacing on nMOS performance against frequency are presented in Figure III.20.

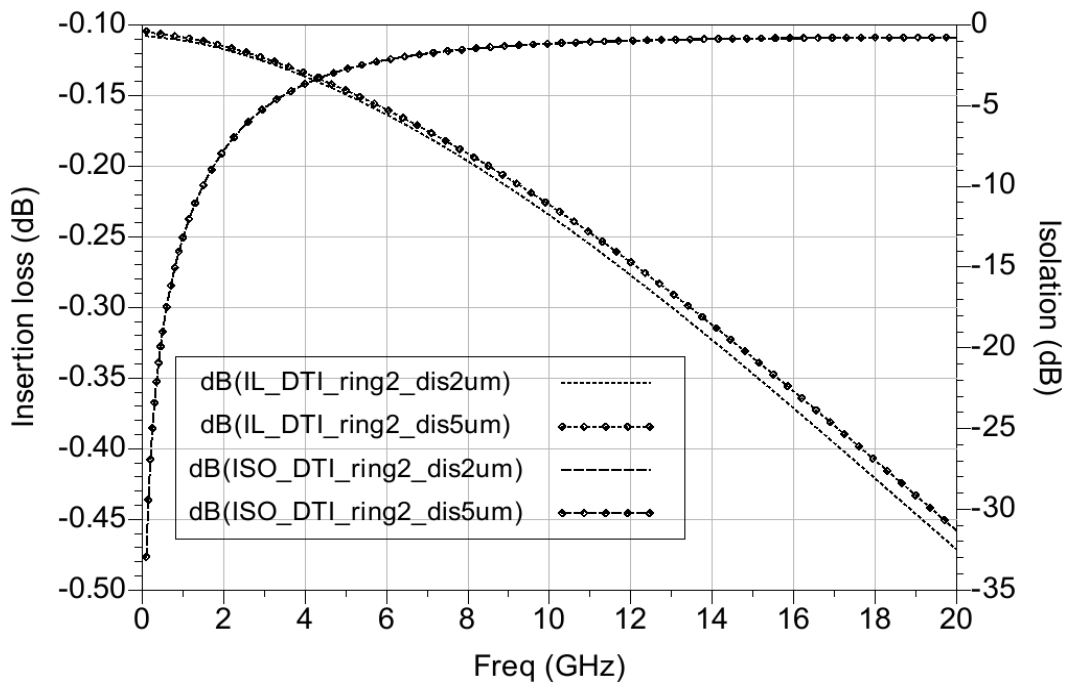


Figure III.20. Measured space variations against frequency of insertion loss and isolation

It has been observed that the DTI ring with a space of 5um has a marginal impact on nMOS switch performances. This is due to the presence of the channel stopper below DTI (Figure III.21) which behaves as a conductor in the case of a minimum separation between ring thus leads to path of undesired RF leakage.

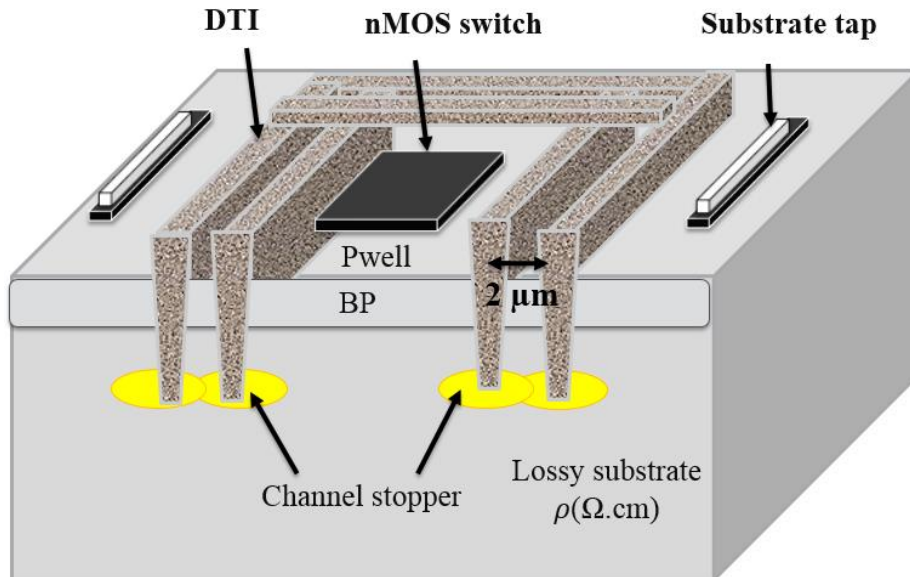


Figure III.21. Cross section of the isolated nMOS with DTI: space of 2 μm and the impact of channel stopper

### III.2.3. Modelling technique and comparison with measurements

Based on the obtained results and the concluding remarks in the previous sections, we examine the accuracy of the proposed methodology at block level.

The test case used is the nMOS switch isolated by 2 DTI rings with a space of 5 μm (Figure III.22). The total channel width is 1000 μm.

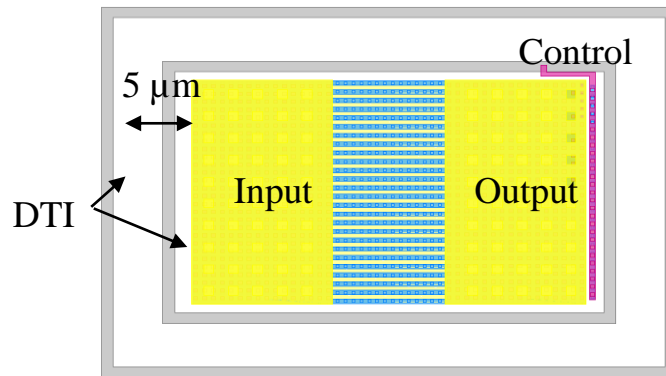


Figure III. 22. Top view of the isolated nMOS fusing 2 rings of DTI with 5 μm of spacing between rings

As discussed before, this isolated configuration poses some difficulties to standard 2.5-D EM design tools. The principal difficulties concern the accurate simulation of the boundary conditions at the limits of the BL (Buried Layer) domain bounded by the isolation trench ring.

The substrate network is extracted and then associated to the compact model of the nMOS device. Several parameters were evaluated, principally the insertion loss, the input return loss (magnitude and phase) (Figure III.23) and III.24) the  $R_{on}$  and the isolation (Figure III.25).

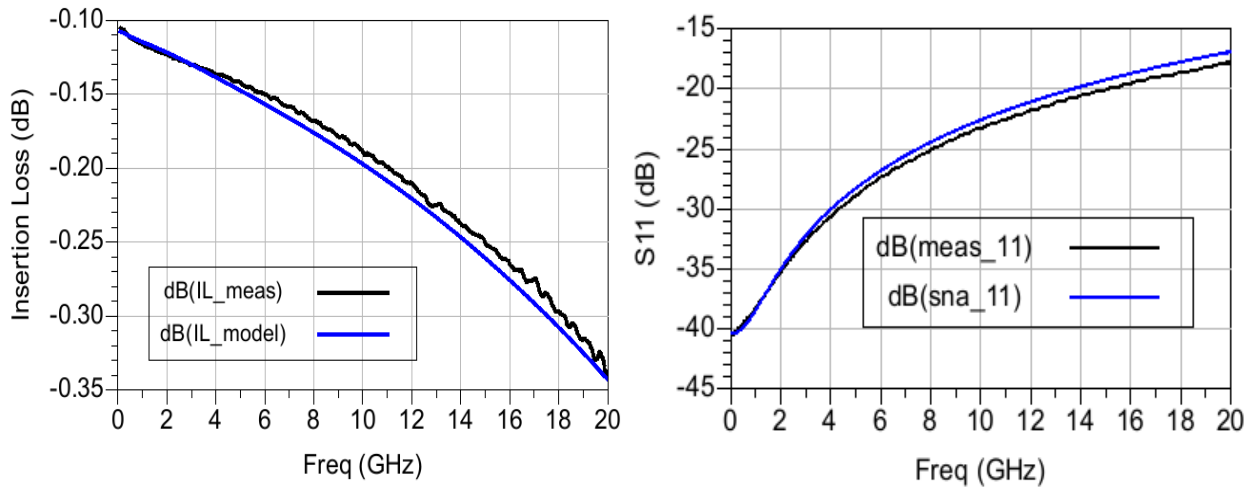


Figure III.23. Magnitude of  $S_{11}$  and insertion loss  $S_{21}$  against frequency: predicted simulation vs measurements result

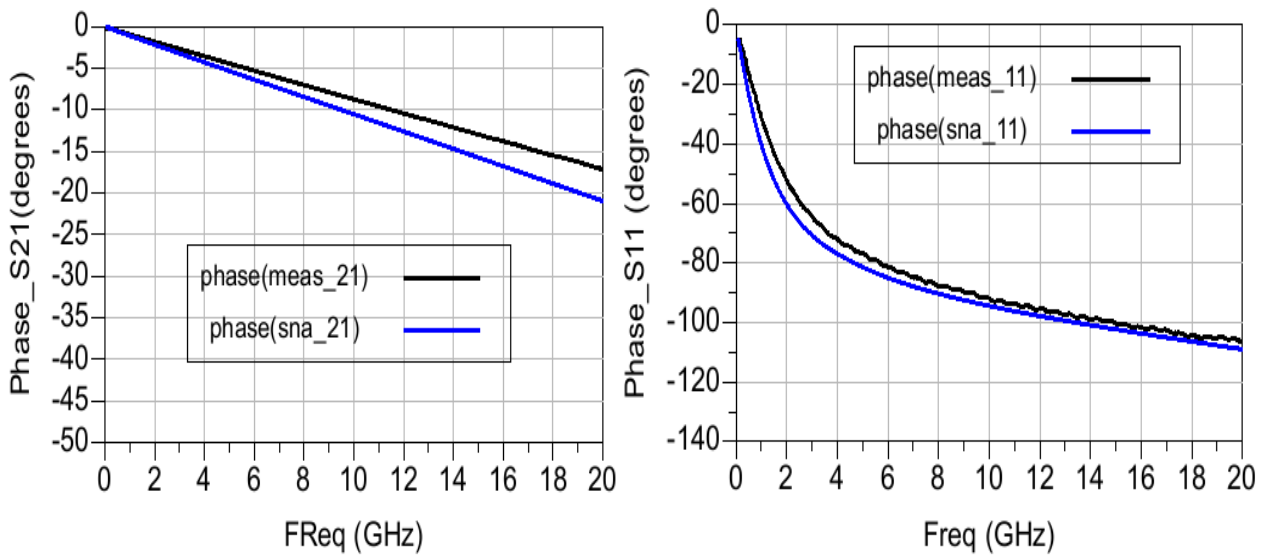


Figure III.24. Phase of  $S_{11}$  and  $S_{21}$  against frequency: predicted simulation vs measurements

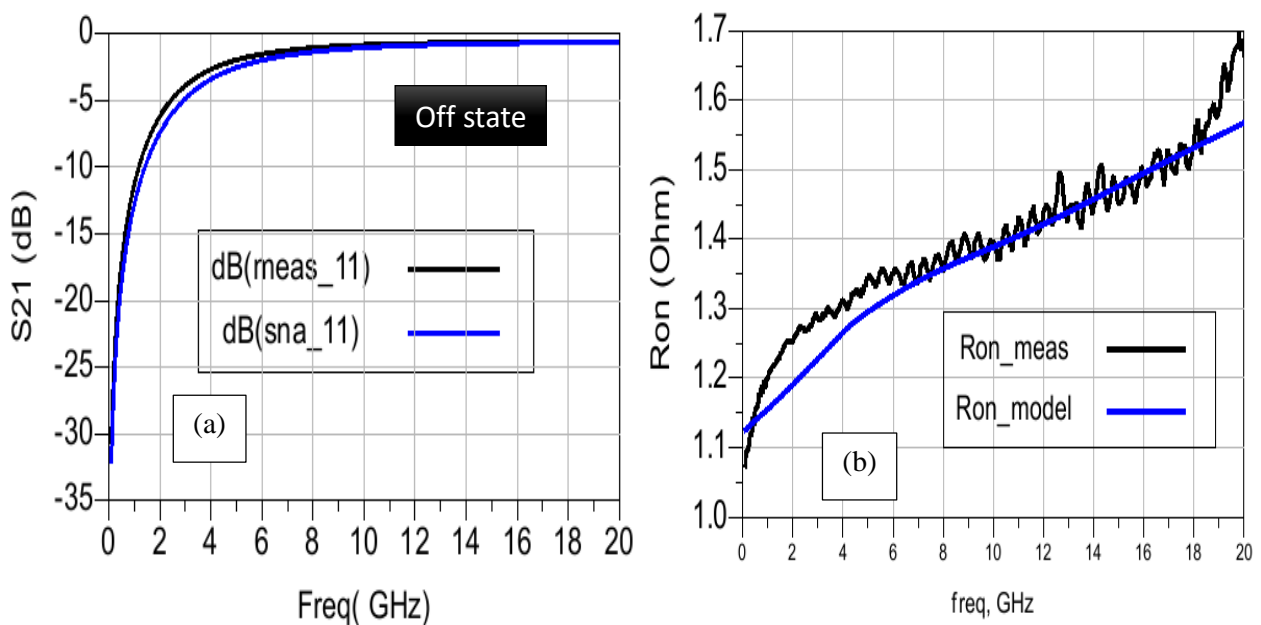


Figure III.25. Isolation (a) and  $R_{on}$  (b) against frequency: predicted simulation vs measurements

Post layout simulation (backend parasitic + substrate extraction) and RF measurement are compared for the isolated nMOS switch with DTI 2 rings with 5  $\mu\text{m}$ . Pas mal du tout la corrélation

*Table III.6. Simulated switch performances vs measurements at 2.4 GHz*

| <b>Frequency = 2.4 GHz</b>    | <b>Insertion Loss (dB)</b> | <b>Isolation (dB)</b> | <b>Input return loss (dB)</b> | <b>Ron (<math>\Omega</math>)</b> |
|-------------------------------|----------------------------|-----------------------|-------------------------------|----------------------------------|
| <b>Post layout simulation</b> | 0.12                       | 5                     | 34                            | 1.27                             |
| <b>RF measurements</b>        | 0.12                       | 6.2                   | 34                            | 1.2                              |

*Table III.7. Simulated switch performances vs measurements at 20 GHz*

| <b>Frequency = 20 GHz</b>     | <b>Insertion Loss (dB)</b> | <b>Isolation (dB)</b> | <b>Input return loss (dB)</b> | <b>Ron (<math>\Omega</math>)</b> |
|-------------------------------|----------------------------|-----------------------|-------------------------------|----------------------------------|
| <b>Post layout simulation</b> | 0.34                       | 0.6                   | 18                            | 1.66                             |
| <b>RF measurements</b>        | 0.34                       | 0.6                   | 17                            | 1.56                             |

Very good agreement observed between post layout simulations and measurements for the insertion loss and input/output return loss in mag & phase over the frequency range.

### III.3. Substrate Isolation's recommendations using DTI

From the measurement results done on the various structures of the nMOS device used in switch application and on coils. we define the following recommendations for a best isolation:

- DTI with 1 ring configuration has a better isolation than removing the Burried P and Pwell around the active area. Indeed, this technique improves the isolation comparing to the default case (without DTI, without any isolation technique) but not enough to achieve the requested specification.
- The DTI rings versus DTI mesh shows almost the same isolation when the number of rings is more than 2. For this reason, we recommend to use a DTI configuration with rings instead of a mesh, to save area and reduce the extraction run time.
- The DTI with 3 rings didn't show a significant isolation improvement versus DTI with 2 rings, in that sense the use of 2 rings is good enough to improve the nMOS isolation
- The use of 2 DTI rings with a spacing of  $5\mu\text{m}$  between rings has the better isolation than 2 rings with a spacing of  $2\mu\text{m}$ . From the obtained results in Figure III.20, it is preferable to use a space  $5\mu\text{m}$  for lower losses.
- The use of a single Ptap out the DTI instead a ring of Ptaps, this has no impact on the performances provided that Ptap is outside the DTI ring
- The interruption of the Buried-P underneath the passive element instead of the DTI mesh has a significant gain in the run time of EM simulation for the same accuracy.

In addition, a particular care must be paid also to the layout itself to reduce the occupied active area and thus reduce the substrate impact [III-6]. Figure III.26 illustrate a new topology of an optimized nMOS switch. From the published results in [III-6] the figure of merit of the switch is improved because of a significant reduction of the substrate impact.

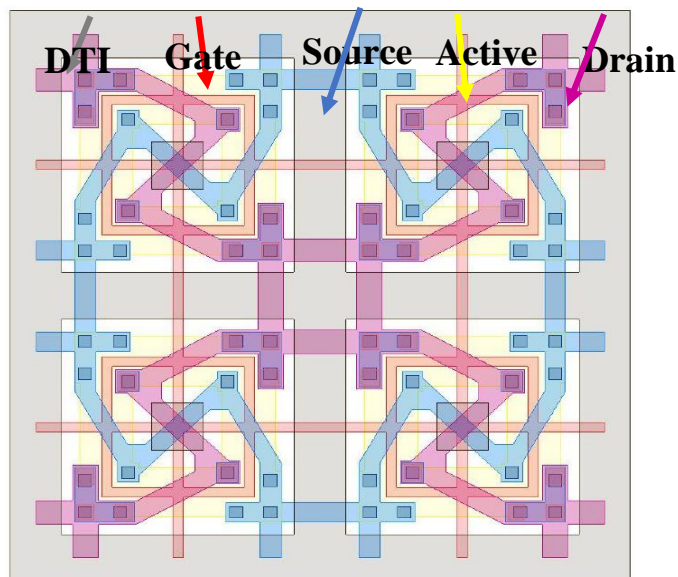


Figure III.26. A new layout of an optimized nMOS switch



## Conclusions

This chapter discusses various methods to reduce substrate coupling in the nMOS switch using Deep Trench Isolation. The role of the number of rings, the space between rings and Ptap placement on the figure of merit of the nMOS switch were investigated.

The main objective of this study is to find out the best isolation strategy and define a list of recommendations for the design community to improve the switch performance.

The accuracy of the modelling methodology developed in the previous chapter was evaluated at component level. The obtained results using substrate extraction, are compared with measurement data and an accuracy of 50 mdB is obtained overall the frequency range used (100MHz -20GHz). Both experiments and simulations, showed that the use of two rings of DTI with a spacing of 5 $\mu$ m has better substrate coupling prevention capability than 2 rings with 2  $\mu$ m and 1 ring. But isolation with 3 rings of DTI did not reduce significantly insertion loss.

The efficient usage of isolation structures is validated at device level. The validation of the proposed isolation strategy is extended to be done at IP level, and that will be presented in the next chapter.

Using the proposed methodology shows that all stringent requirements of today's wireless applications can be met. This paves the way for implementing a fully integrated TX/RX switch in a BiCMOS technology.

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# Chapter IV: Modelling methodology for predictive analysis of substrate effects in an RF Switch

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## Introduction

The previous chapters have clarified the advantage of substrate isolation and the role of the Deep Trench Isolation (DTI) on substrate coupling and the necessity to have a predictable methodology to handle DTI accurately in a shorter time. A methodology was proposed based on a quasi-static approach for layout extraction.

We have studied previously the modelling and isolation strategy on dedicated single structures. We propose to move forward in this chapter and apply the proposed methodology to a full SPDT switch for LTE applications.

The accuracy of the proposed methodology was evaluated in comparison with numerical method and measurement data. This allows us to validate, on one hand the impact of substrate isolation on the device performance, and on the other hand the correctness and predictability of the considered methodology.

This chapter will explore two variants of an RF switch based on a 0.25  $\mu\text{m}$  SiGe BiCMOS technology. This switch is a key element in Front-End IC's (Integrated Circuits) for WLAN, LTE and mmWave applications. In this chapter, we will extend the previously defined methodology to a more complete circuit design. Several options of an SP3T switch will be presented allowing to investigate bulk and doped regions absolute biasing. We will draw some conclusions with respect to this aspect. On top of that we will elaborate on the isolation strategies that have been considered. Then, we will evaluate the accuracy of the developed modelling approach at IP level by a comparison with the Finite Element Method simulation results and measurement data. The tight requirements imposed by communication standards require a proper modelling of this kind of IP in their real environment to account for predictability on Insertion Losses as well as NF (Noise Figure) [III-1]. On top of that, to extend the methodology, an SP8T switch has been used also as a test vehicle.

## IV.1. LTE SPxT switch

In this section, we explore RF Single-pole Double throw (SP2T) switch design using in house NXP 0.25  $\mu\text{m}$  BiCMOS technology. The focus of this work is to design a high performances switch in term of insertion loss and noise figure for cellular applications (Long Term Evolution).

The use of BiCMOS nMOS transistors for front-end blocks of RF switches raises issues to nMOS substrate loss due to the lossy nature of the silicon. RF single-pole, double throw SPDT switch designs are explored for their power handling capability and isolation [IV-2]. The standard series-shunt switch utilizes nMOS transistors acting as pass-gates and shunt terminations. Most of the switch performance is determined by the electrical characteristics and parasitics associated with the series (or on-state) device.

The SPDT switch was designed using the topology highlighted in Figure.IV.1. The topology was chosen to meet the tight specifications. The goal is to design a switch with a minimum insertion loss ( $<1$  dB) and a high isolation.

To improve insertion loss, an isolated nMOS device is used as a series switch. This isolation is achieved using 3 DTI rings, reducing parasitic losses by increasing the substrate impedance of the device. The shunt nMOS devices lead to increased isolation while degrading the insertion loss.

Three test cases are evaluated, 2 test cases represent the SP2T and the third one is an SP8T:

- **SP2T:** Single Pole Double Throw, it is based on two design variants:
  - Case A: Asymmetrical bias: only the drain is biased in the case A (the drain is floating)
  - Case B: Symmetrical bias: both source and drain of the device are biased at the same dc potential. This option requires the use of DC blocking capacitors. These capacitors must be carefully chosen and a trade-off must be done between capacitor area (value) and related losses. It has the advantage to turn some nMOS in deep-off state and thus reduces Coff and improves isolation. For mmWave applications, series inductance of the capacitor can be also a concern when designing the switch.
- **SP8T:** multiple throw switch: This configuration is like the SPDT A. asymmetrical bias is considered  
These switches were initially designed by the ADT team from NXP NL and placed on a MPW (Multi Project Wafer).

### IV.1.1. SPDT test cases description

The first two test cases (A and B) in are shown in Figure IV.1. The switching control is provided by a DC signal. When  $v_{on}$  is high, M1 is on and M2, M3 and M4 are off, allowing the RF signal to pass from IN to OUT1. Similarly, the signal flows from IN2 to OUT when  $v_{off}$  is high.

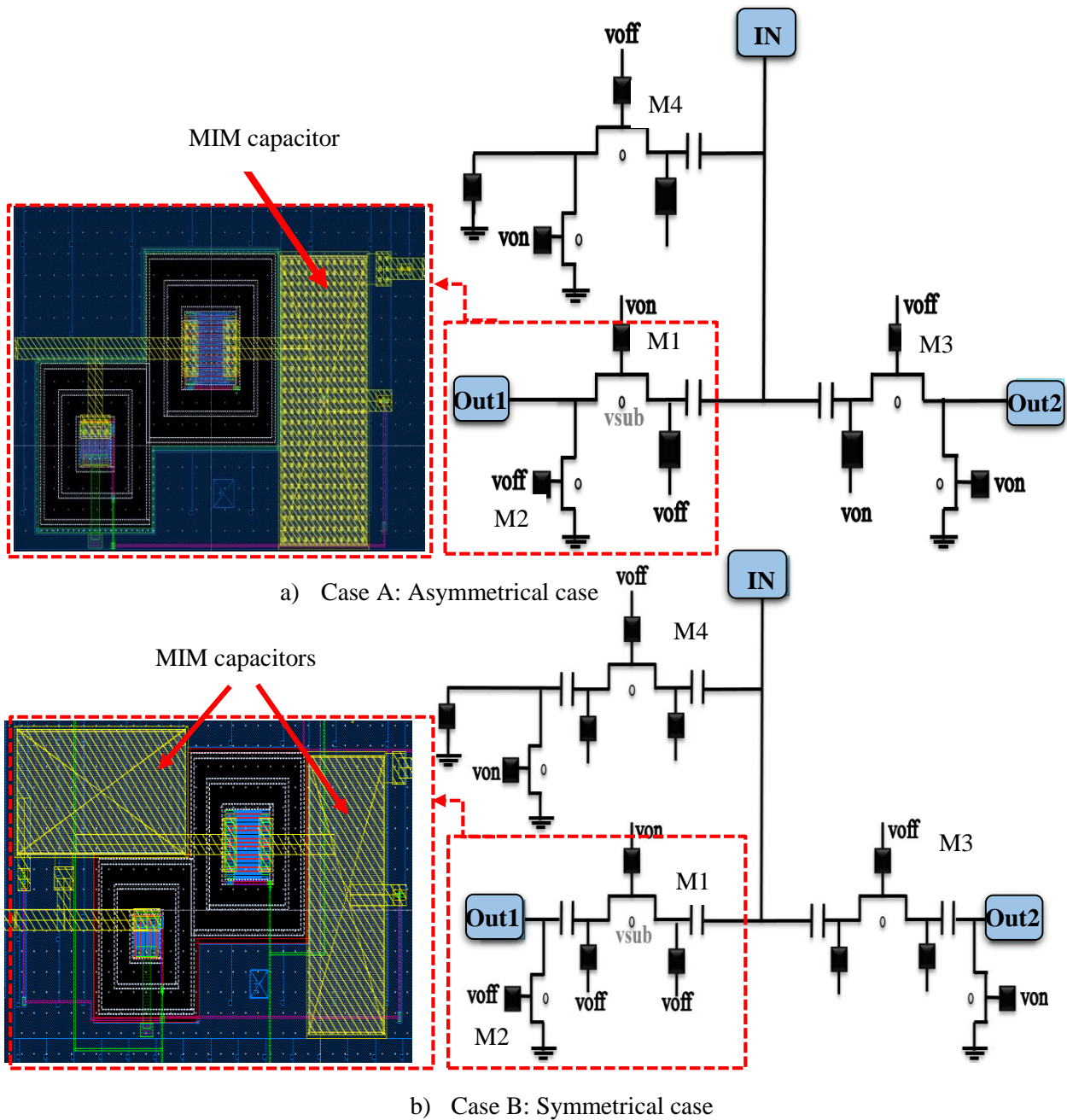


Figure IV. 1. Schematic of the SPDT switch: a) Only the drain is biased, b) Both the source and drain are biased

The gate of the device is isolated using a  $50\text{K}\Omega$  poly resistor [II-20] to isolate the gate from the RF signal leakage. The bulk of each nMOS device is connected to a DC signal:  $v_{\text{sub}}$ .  $v_{\text{sub}}$  value will be swept during the experiment. We will elaborate later on that specific feature.

The case A: when M1 is in its on-state ( $V_{\text{on}}$ ), the drain is biased to  $V_{\text{off}}$  voltage through a  $100\text{K}\Omega$  resistor. The source of the nMOS device is float. In this configuration, only one MIM capacitor is connected to the drain for DC block.

The case B: when the control voltage  $V_{\text{on}}=2.8\text{V}$ , the voltage  $V_{\text{off}}=0\text{V}$  provides the bias to both of the source and the drain of the transistor through resistor of  $100\text{K}\Omega$  which play the role of RF choke. In this configuration, two MIM capacitors connected to etch side (source/drain).

Table IV. 1. Description of the design configurations

| Design | Description  | Bias → IN-OUT1 active branch |        |        |        |
|--------|--------------|------------------------------|--------|--------|--------|
|        |              | Vg (V)                       | Vs (V) | Vd (V) | Vb (V) |
| SPDT-A | Asymmetrical | Von                          | Float  | Voff   | 0      |
| SPDT-B | Symmetrical  | Von                          | Voff   | Voff   | 0      |
| SP8T   | Asymmetrical | Von                          | Float  | Voff   | 0      |

The optimization of those switch for the LTE band requires appropriate selection of device geometry which involves a trade-off between the On-state ( $R_{on}$  device on resistance) and the Off-state (device capacitances). As the nMOS switch operates in the linear region, the on-resistance can be given by the equation:

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})}$$

In other words, the on-resistance is inversely proportional to the total width of the transistor, a larger width will provide a smaller  $R_{on}$ , but will also increase overlap and S/D to body capacitances, thus impacting the overall switch performances. This includes the linearity which is also dominated by the device parasitic capacitances. Consequently, it is necessary to pay attention to the layout of the MOS to minimize the losses.

In the current design, the switches were realized to achieve an optimum insertion loss at 1.8GHz. The optimal gate widths for the series and shunt devices were chosen as 200 $\mu$ m and 100 $\mu$ m, respectively. The insertion of the series switch is defined as follows:

$$IL_{serie} \text{ (dB)} = 20 \log \left( 1 + \frac{R_{on}}{Z_0} \right)$$

In the real case, this on-resistance corresponds to the DC  $R_{on}$ . The effective on-resistance then also includes the contribution of the admittance to ground, which is formed by the parallel connection of gate and bulk impedances.

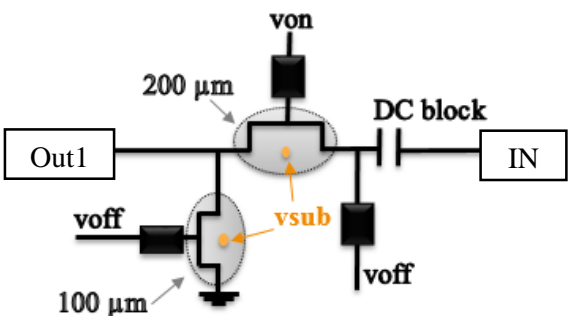
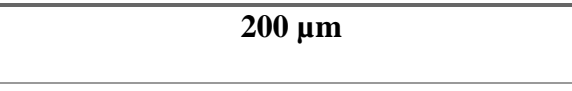
Furthermore, the insertion loss of the shunt switch which is defined by the following formula, these losses will be added to the total insertion losses of the On-branch (series losses):

$$IL_{shunt} \text{ (dB)} = 10 \log \left( 1 + (\pi f \cdot C_{off} \cdot Z_0)^2 \right)$$

The on-resistance is technology dependent. In 0.25 $\mu$ m BiCMOS technology, for a transistor with a total channel width of 200 $\mu$ m, of which the gate and Source/Drain are respectively biased at 2.8V and 0V, the on-resistance is 5.5 $\Omega$ .

The following table represents the on-resistance and the off-capacitance together with the calculated insertion losses at 1.8 GHz:

Table IV. 2.SPDT switch performances

| Switch sizes  | $R_{on}$ ( $\Omega$ ) | $C_{off}$ (fF) | IL (dB) |
|---|-----------------------|----------------|---------|
|  | 5.5                   | 111            | 0.47    |
|  | 10.8                  | 57             | 0.9     |

#### IV.1.2. RF Measurement set-up of SPDT and SP8T

Figure.IV.2 describes the test bench for RF characterization using a two-port Vector Network Analyser (VNA) and G-S-G RF probes of the SPDT switch. The SP8T switch follows the same measurement procedure.

Measurements were performed from 100 MHz to 25 GHz.

The calibration at 90° was performed prior to measurements.

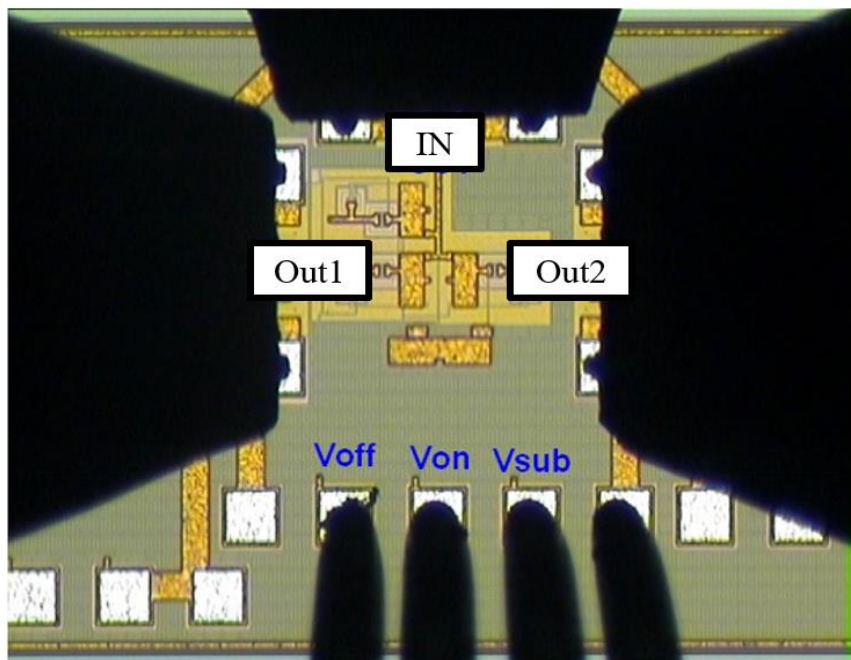


Figure IV. 2.Schematic of the SPDT switch A and B versions using different bias configurations

### IV.1.3. SPDT Measurement Results

To define the best design methodology, a comparison between configurations A and B was performed based on the measurements results.

When nMOS device (M1) is on, we evaluate the insertion loss between IN and OUT1, and the isolation between OUT1 and OUT2 (Figure IV.3: a) and b) respectively).

When M1 is in disable mode, we evaluated the isolation between the IN and OUT1. This needs to be high enough to prevent the RF signal leakage to the other side of the switch (between IN and OUT2).

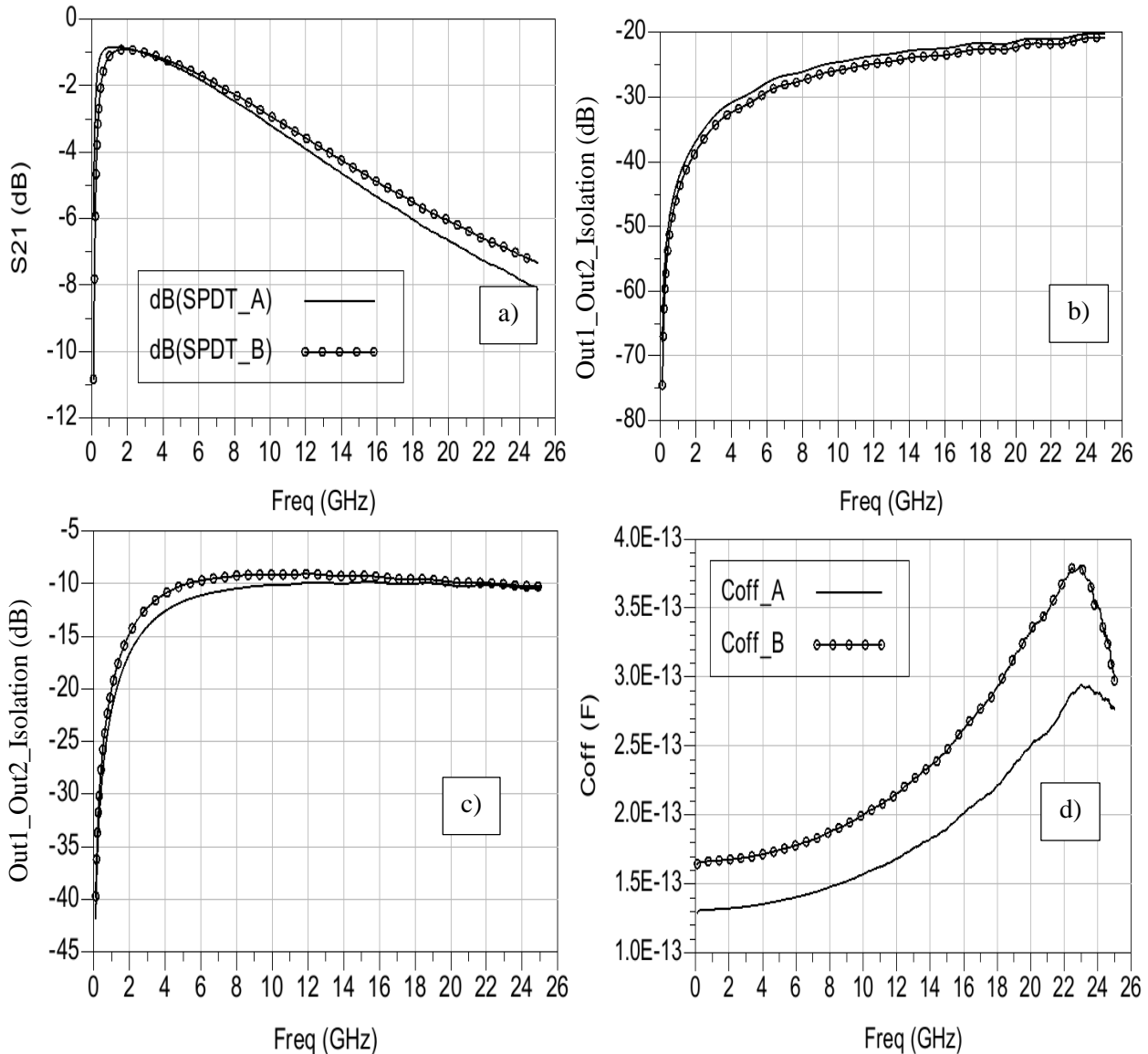


Figure IV. 3. Symmetrical switch vs asymmetrical switch comparison: a) the insertion loss between IN and OUT1, b) the isolation between OUT1 and OUT2, c) the isolation between IN and OUT1 and d) Coff

From the obtained result, at 1.8GHz the insertion loss of the case A vs the case B is 0.86dB vs 0.9dB respectively.

The isolation is slightly higher in the configuration A (asymmetrical). The Coff obtained in case A is lower than the Coff of case B. The isolation of case A is thus best.

In that sense, the asymmetrical configuration offers a good trade-off between switch performance and layout compactness with the use of one MIM capacitor instead of two for each side of the switch.

#### IV.1.4. SPDT modelling methodology and comparison with measurements

##### c. Modelling methodology

The EM analysis of the complete design, including substrate effects, passive elements losses etc, does not converge very well within a reasonable run time, using the available commercial EM tools. It needs several hours, and the data base (partitioned layout) is very complicated. So, a methodology is developed to reach the required trade-off between accuracy and computational resources. This methodology is based on a partitioning S-parameters model issued from EM simulation and layout based parasitic extraction technique to account for the substrate with its anisotropic structures (DTI). In few minutes, we can achieve the required extraction level for accurate simulations.

In the previous chapter, we have presented the layout parasitic extraction methodology to predict the substrate impact in the nMOS device with various isolations techniques. The accuracy of this methodology was validated in comparison with the measurements results for different parameters.

In this section, we will investigate the predictability of this proposed methodology at IP level. The switch designed in this study includes several nMOS devices isolated by the DTI, these trenches serve to increase the substrate impedance between each device's body connection and substrate tap and between the neighbor devices. In this aspect, even if the undesired coupling between the nMOS devices is reduced thanks to the DTI, it should be accounted accurately in addition to the substrate network of the device itself. (Figure IV.4).

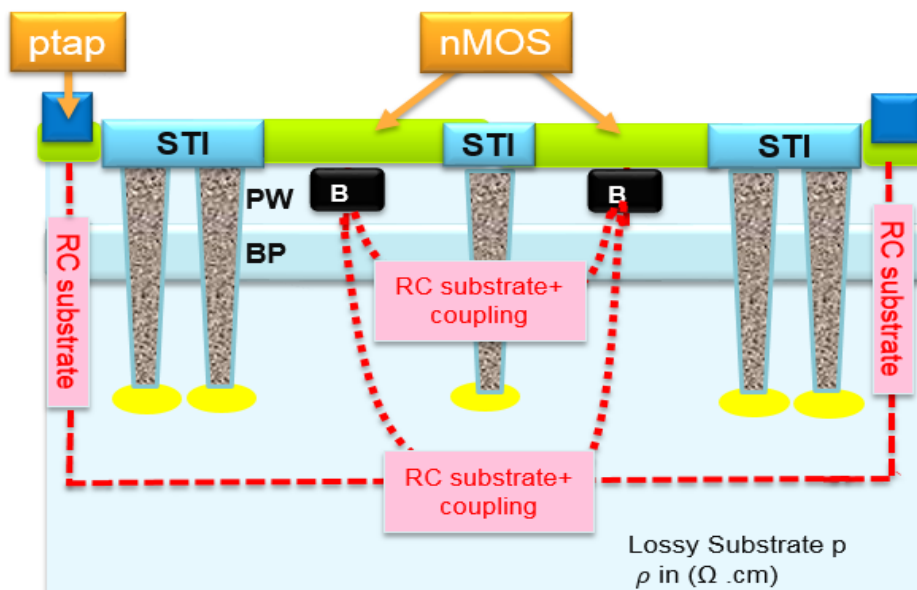


Figure IV. 4. Cross-section of 2 nMOS isolated by DTI



The simulation of the complete design needs to be segmented into partitioned sub-blocks. Two approaches are compared in terms of accuracy and complexity. To support theoretical investigations, correlations with silicon measurement are proposed. These methodologies based on a partitioning technique of lumped RLCK model extraction with the S-parameters models in the first approach and with the based layout extraction in the approach.

The first analysis, figures-out the equivalent substrate impedance as localized  $Z_{sub}$  from the S-parameter instead of the distributed R-C network currently used to denote the impedance between the bodies of the transistors as shown in figure IV.4.

The second approach is based on a quasi-static approach to extract the distributed substrate network

- Model based on full wave simulation for substrate analysis: in that case, the substrate impedance is derived from S-parameter obtained from 3D EM simulation. The body of each nMOS is connected to the  $Z_{subV}$ . The interaction between the neighbor devices is represented by the lateral contribution  $Z_{subL}$  (Figure IV.5).

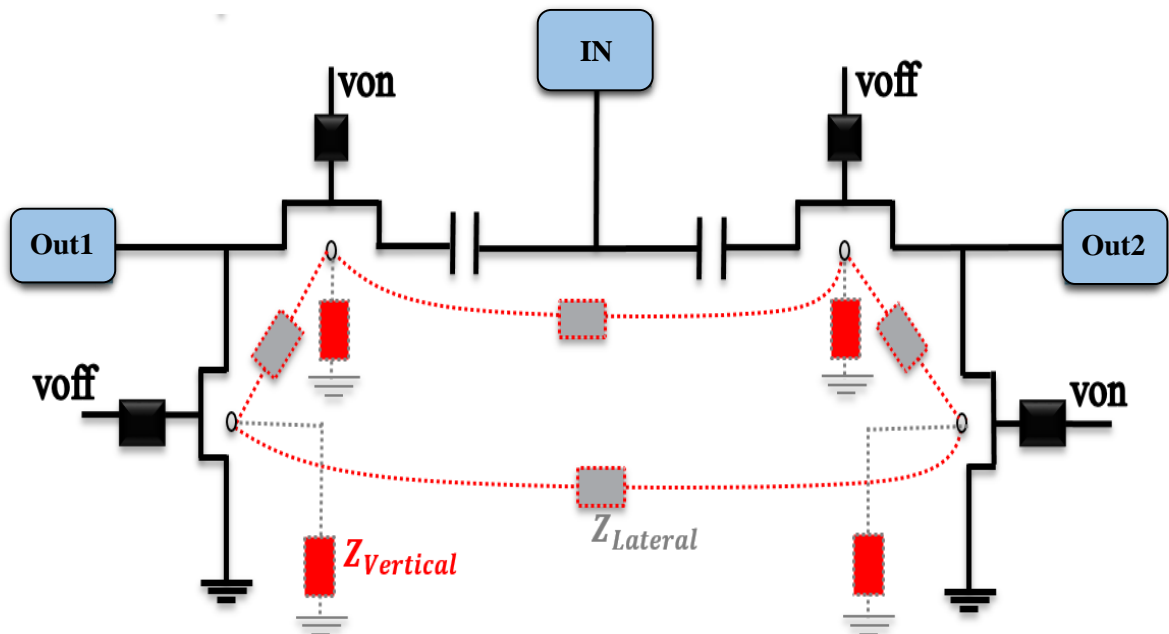


Figure IV. 5. The circuit schematic of the SPDT switch including the derived substrate lumped-element from 3D EM simulation

- Model based on quasi-static for layout extraction: A distributed RC network is extracted and implicitly connected to the components (Figure IV.6).

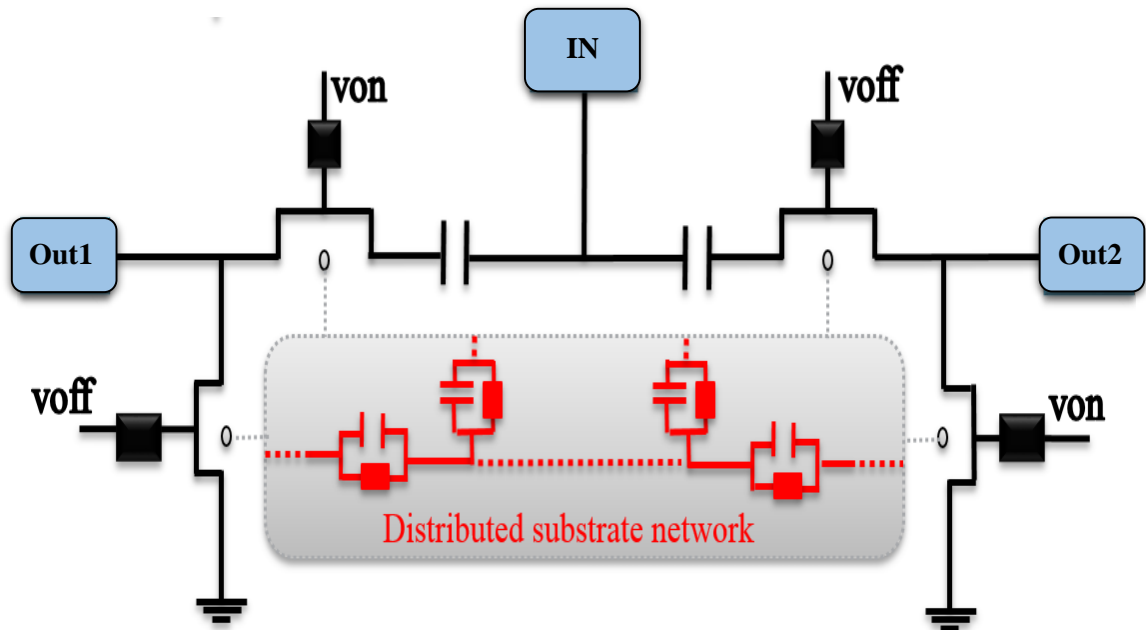


Figure IV. 6. The circuit schematic of the SPDT switch including the distributed substrate network

Table IV. 3. Advantage and limitations of the proposed modelling approaches

| Methodology                                    | Advantage   | Limitation   | Proposal   |
|--|---|--|--|
| <b>Backend + substrate extraction</b>          | Fully integrated in the flow<br>Tradeoff between accuracy versus usability<br>Fast run simulation (few minutes)           | Coupling between passives elements and the substrate   | Partitioning methodology with 2.5D EM simulation to account for EM behavior of passive elements              |
| <b>Backend + Lumped-element (S-parameters)</b> | Coupling between backend and substrate included in the analysis<br>Use of lumped-element representation from S-parameters | Complexity: requires 3D approach to account for anisotropic structures<br>Difficult to find out the corresponding model<br>Excessive run time stimulation (1h).<br>Requires first S-parameter simulation | Partitioning methodology between 2.5D/3D approaches: cascade approach between passive elements and substrate |

#### d. Correlation with measurements results

Figures IV.7 and IV.8 shows the measured insertion loss and the return loss of the SPDT-A, the insertion loss at 1.8GHz=0.7dB from predicted simulation using both methodologies vs 0.8dB and measurements.

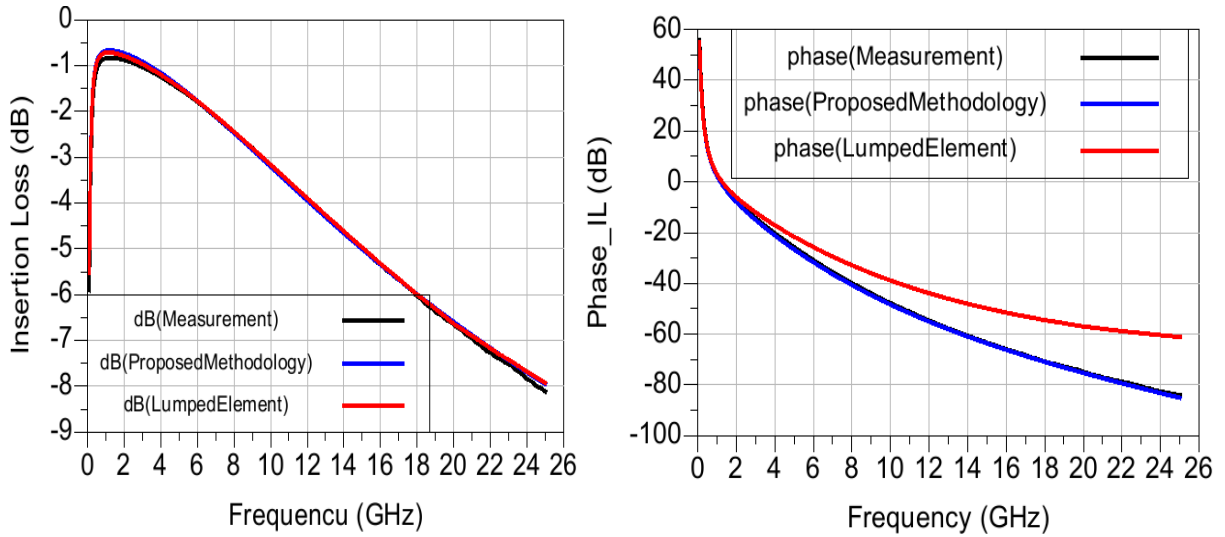


Figure IV. 7. Measurement vs proposed model:  $S_{21}$  and  $S_{11}$  phases

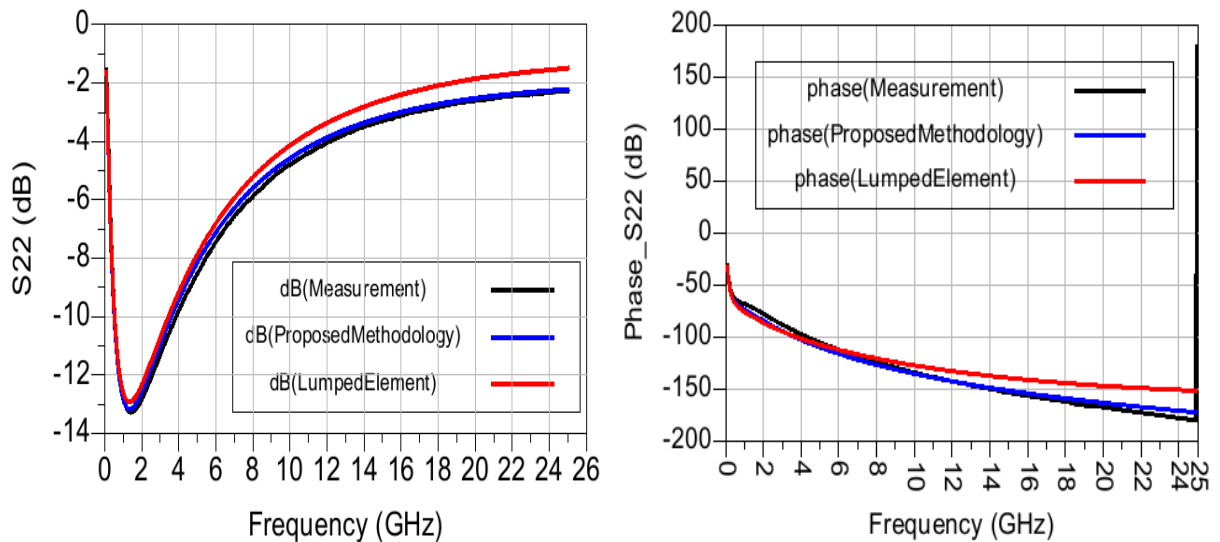


Figure IV. 8. Measurement of asymmetrical SPDT switch vs proposed model:  $S_{21}$  and  $S_{11}$  mag

A very good agreement between simulation and measurement for insertion and return loss (mag & phase) using the based layout extraction.

The approach based on the lumped-element is presenting an accurate result in comparison to measurements results and the based layout extraction methodology.

#### e. RF switch performance as function of the substrate bias

Each nMOS device in the SPDT switch has its own substrate tap located outside the DTI rings. These substrate taps are connected to a dc voltage  $v_{sub}$ .

To investigate the substrate bias impact on the switch parameters, mainly the insertion loss, and the isolation between IN and OUT1 (figure.IV.4), three variants  $v_{sub}$  values were measured at a fixed  $v_{g1}=2.8V$ :

- $v_{sub} = 0V$
- $v_{sub} = -1.5V$
- $v_{sub} = -2.5V$

In a second test, we change the gate voltage value from 2.8V ( $v_{g1}$ ) to 1.5V ( $v_{g2}$ ) and keeping the same substrate bias  $v_{sub}$  variation (0V, -1.5V and -2.5V)

The use of body-biasing technique allows to control the leakage current. The body  $V_b$  of the nMOS device biased to a voltage lower than ground increases the threshold voltage of the nMOS device, and consequently the leakage current is reduced. The following equation shows that when  $V_b$  reduced,  $V_{th}$  increases. However, in the active mode, the increased  $V_{th}$  impact the delay.

$$V_{th} = V_{th_0} + \gamma(\sqrt{|-2\phi_F + V_b|} - \sqrt{|-2\phi_F|})$$

Where  $V_{th_0}$  is the threshold voltage for  $V_b = 0$ ,  $V_b$  is the body voltage,  $\phi_F$  is the fermi potential and  $\gamma$  is the body effect coefficient which is function of the substrate doping, silicon permittivity, and oxide capacitance.

In addition, the NMOS transistors bodies are biased with a negative dc voltage, and thus it reduces the parasitic capacitance of the nMOS transistors between drain and source. Assuming that the dc biases of both drain and source are set to 0 V, the diodes ( $D_{sb}$  and  $D_{db}$ ) are turned off when the body bias of the transistor is lower than  $\sim 0.7$  V. The junction capacitances of the  $D_{sb}$  and  $D_{db}$  can be expressed as:

$$C_{sb,db} = \left( \frac{C_{bot_0}}{\sqrt{(1-(V_b/\phi_{bot}))^{m_{bot}}}} \right) \cdot Area + \left( \frac{C_{sw_0}}{\sqrt{(1-(V_b/\phi_{sw}))^{m_{sw}}}} \right) \cdot Perimeter$$

where  $C_{bt_0}$  ( $C_{sw_0}$ ) is the value of capacitance at zero voltage,  $V_b$  is the body bias voltage,  $m_{bot}$  ( $m_{sw}$ ) are the process dependent, and  $\phi_{bot}$  ( $\phi_{sw}$ ) is the junction potential. As can be observed, the nonlinear junction capacitances will be reduced when the body is biased with negative voltage. In figure IV.9 we present the comparison between the 3-varied substrate bias at a given gate voltage.

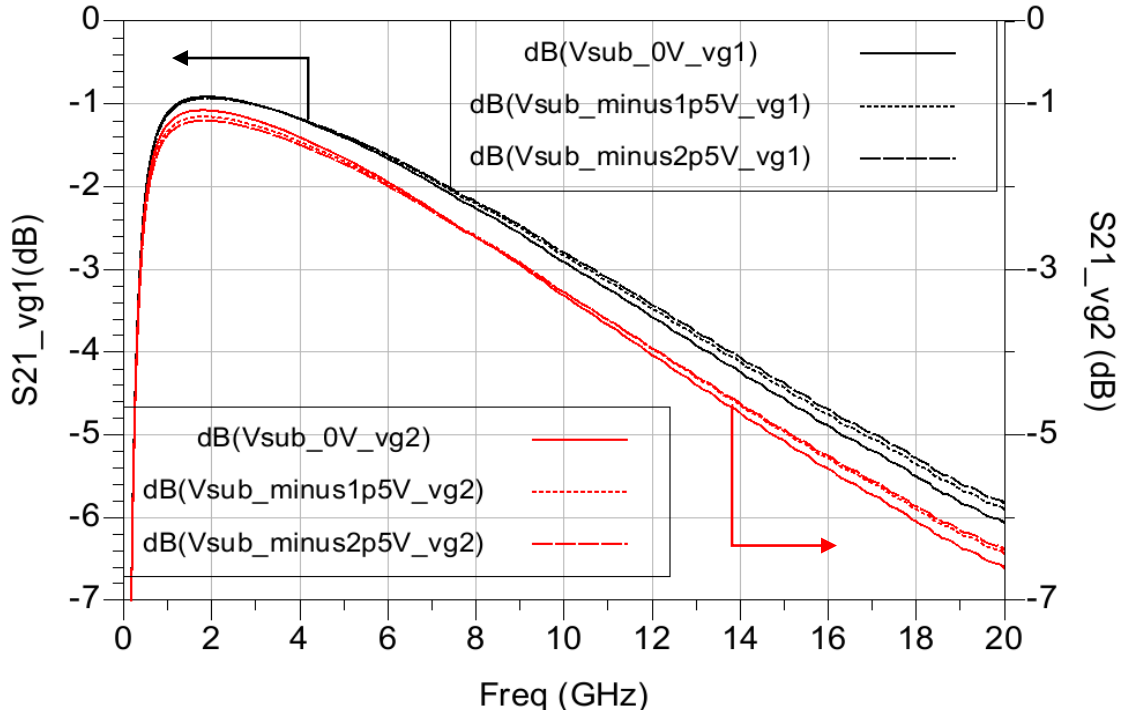


Figure IV. 9. Measured insertion loss of the SPDT\_B switch function of the substrate bias at a given gate voltage:  $vg1(2.8V)$  and  $vg2(1.5V)$

From the obtained measurements results, we observe that at low frequency, no influence of the substrate bias on the insertion loss. But with the increased frequency increases, the 0V is presenting a worst result than -1.5V and -2.5V (figure.IV.9).

The achieved improvement is minimal regarding the difficulties that this technique presents. To control the threshold voltage, the substrate bias voltage need to be dynamically varied in order to reduce the leakage current in the standby mode, and to attain the normally low  $V_{th}$  in the active mode, thus minimizing the delay variation. This technique has two major drawbacks: the threshold voltage is proportional to the square root of the substrate voltage which requires a large change in the substrate voltage to change  $V_{th}$  by effective value, and a charge pump circuit to bias the substrate is required.

The gate control was also varied between 2 values:  $v_{g1}=2.8V$  and  $v_{g2}=1.5V$ . In the case of the symmetrical switch SPDT\_B, decreasing the gate value degrades the insertion loss.

#### **f. Substrate thickness impact on RF switch**

The back-plane of the substrate may or may not be grounded (case of Flip-chip applications or on the other side QFN based package with exposed die paddle). Depending on the final application and on the packaging.

In flip-Chip packaging, the dies are grinded to be at 180um, an evaluation of the circuit performances function of substrate thickness and the backside connection: floating versus grounded has to be done.

In this part, we investigate the impact of the substrate thickness on the insertion loss and isolation of the switch.

Two thickness were measured and simulated:

- The default thickness: 700  $\mu\text{m}$
- The grinded substrate: 80  $\mu\text{m}$  (for thin HVQFN package)

Here, the chuck of the wafer prober was connected to ground via the grounding port of the network analyser. The results are shown in figure.IV.10.

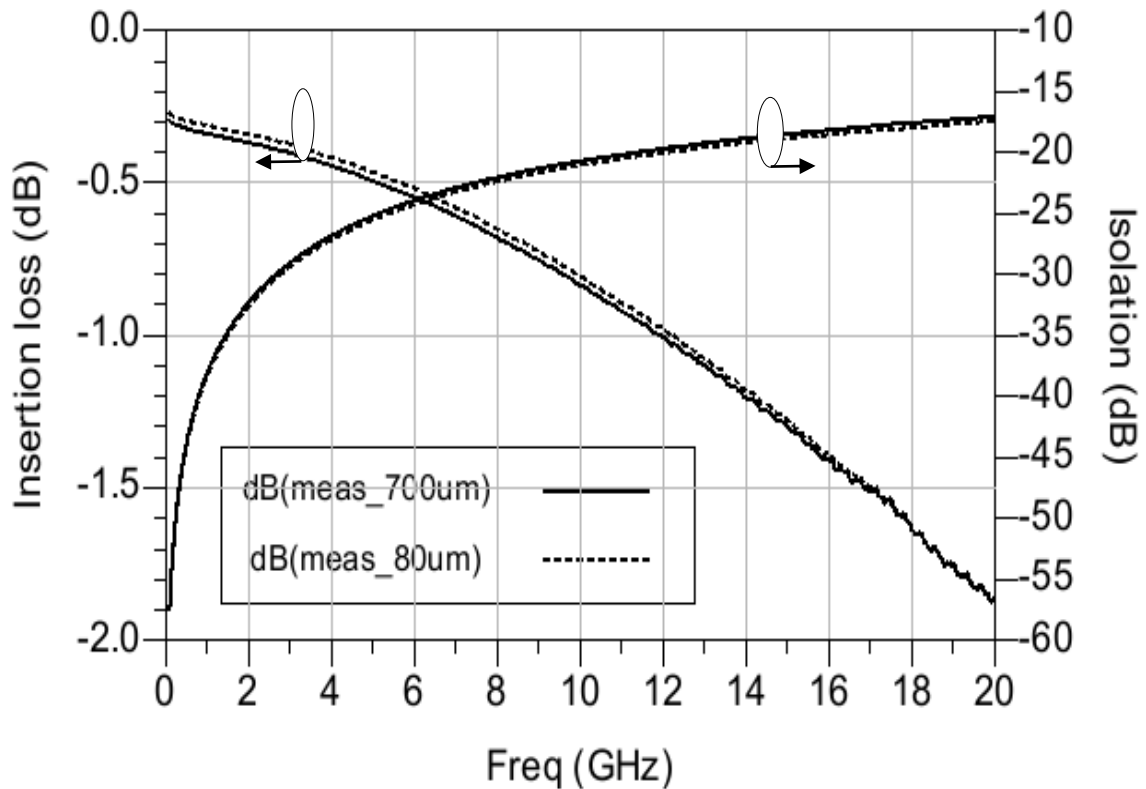


Figure IV. 10. Measured insertion loss and isolation of the SPDT switch as function of the substrate thickness

The impact of silicon substrate thickness on the insertion losses between IN and OUT1 is evaluated.

The substrate cross talk isolation for varying substrate thickness (700  $\mu\text{m}$  vs 80  $\mu\text{m}$ ) with the substrate tap (ptap) located at the frontside is shown in figure.IV.5. From measurement results, decreasing wafer thickness has a marginal impact on switch performances. This because the RF signal leakage does not flow deeply into the silicon substrate when ground nodes are located in the frontside.

The layout parasitic based methodology account for the backside connection. It can handle a backside grounded or floating. The substrate network is calculated assuming the following condition of limits:

- If the backside is connected the ground: it is modelled by the extractor tool as  $V=0$
- If the backside is float: In that case the current=0

## IV.2. SP8T design description

The SP8T switch, 8 inputs sent to one output. The design methodology is the same used in the SPDT-A asymmetrical topology, the control voltage is determined to be 2.8V for the gate of the nMOS device in the On-state and 0V in the Off state. The eight RF inputs ports are distributed into two sections. Each section is constructed by connecting through an intermediate series switch branch to the antenna port (OUT). Figure IV.11 shows the corresponding schematic of the SP8T.

Each branch is designed using the SPST switch highlighted in Figure IV.11. To improve the isolation and the insertion loss, the series and the shunt nMOS devices are isolated from the substrate tap and from each other by the use of 3 DTI rings. The use of the DTI rings around each nMOS device reduce the substrate losses by increasing the substrate impedance in the body of the device. The shunt device increases the isolation with a degradation of the insertion losses. The source is floating and the drain was held at a dc potential. The gate is isolated from RF leakage by 50K $\Omega$  resistor. However, the isolation is degraded due to the additional DTI parasitic capacitance.

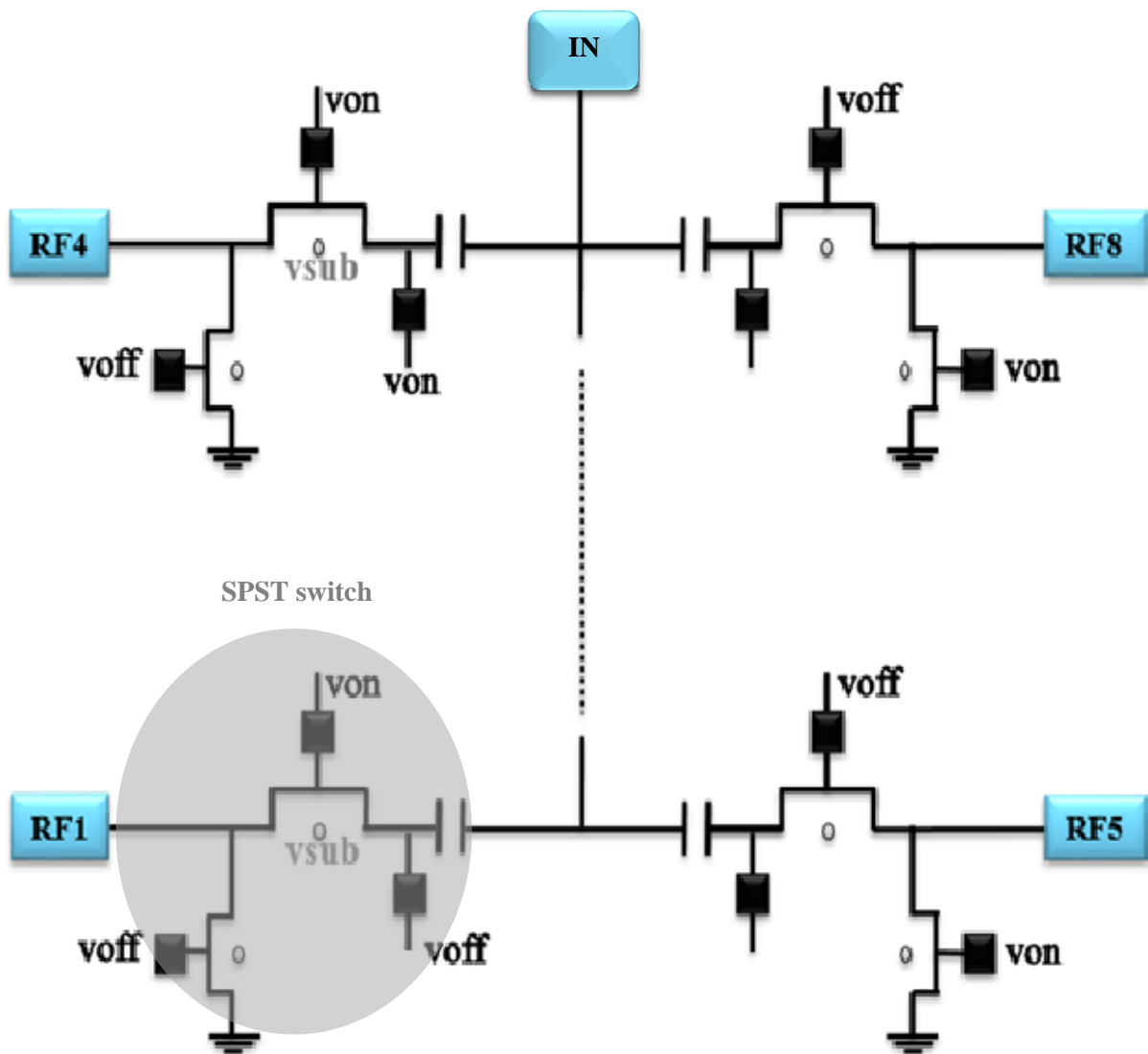


Figure IV. 11.SP8T switch schematic(a)

The optimization of the switch performances involves appropriate selection of device geometry to ensure a trade-off between the On-state and the Off-state. The figure of merit is mainly the product  $R_{on} \cdot C_{off}$ . The smaller width provides the smaller  $R_{on}$  but will increase the capacitances (overlap and source/drain to body capacitances). The switch in this work were designed to improve the insertion loss and thus Noise Figure.

The DC blocking capacitors “C\_block” in Figure IV. 1 were used in series with the series transistors. These blocking capacitors prevent DC current from flowing through the series arms when the FETs are turned On. The capacitors were sized to act as an electrical short for the RF signal over the desired operating frequency range.

### IV.2.1. SP8T modelling methodology

We have seen that the RF switches with 2 inputs to one inputs are sensitive to various coupling mechanisms (substrate coupling, electromagnetic interferences...) and needs a methodology to account for the overall parasitics and predict the accurate behavior of the switch in early phase in the design. In the case of SP8T with 8 inputs to one output, the unwanted couplings are higher and each side of the switch will contribute to the degradation of the “On” branch. In addition, various MIM capacitors are used but will also add resistive losses that need to be modeled accurately.

To analyze the multi-throw switches, we propose a modelling methodology where interaction and influences of, metal parasitics and the substrate are taken into account. To accurately account for substrate effect, this methodology is done in two ways:

#### a. The First approach: based on the proposed layout extraction methodology

The first methodology introduces internally the bulk pin and then extracts the substrate network between this pin and the external Ptap (Figure IV.12). This helps to save design time and simplify the flow.

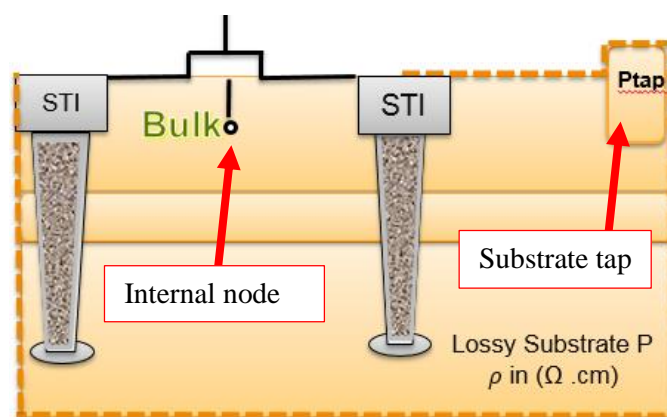


Figure IV. 12. Cross section of a nMOS device with the fourth pin (bulk) and the substrate tap

The proposed modelling methodology at IP-level combines EM simulation to basic layout. Extraction. The flow simplicity appears as shown in figure IV.13. the substrate network with its inhomogeneous substrate is accounted implicitly with backend parasitic.



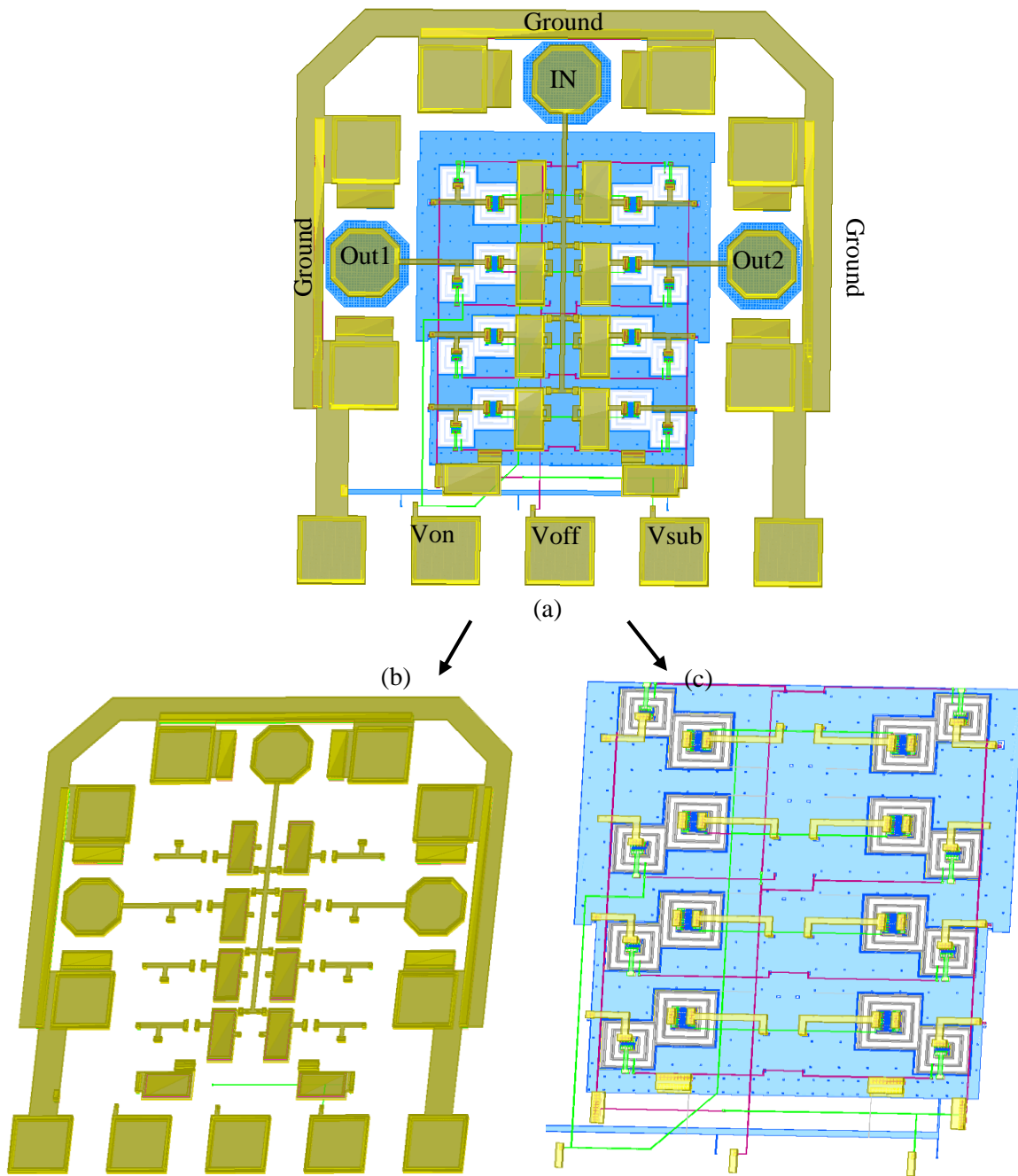


Figure IV. 13. From the initial layout of the RF switch (a) to the passive blocks analyzed by EM (b), and the active blocks including the DTI (c)

**b. The second approach: based on EM simulation (Finite Elements Method)**

The second methodology based on EM simulation, requires a layout modification to obtain a clean LVS (Layout Versus Schematic). We need to introduce a fourth pin for the nMOS device, this is needed to connect the obtained model from S-parameters between the bulk pin (the back-gate of the nMOS) and the Ptap located outside the DTI (Figure IV.14).

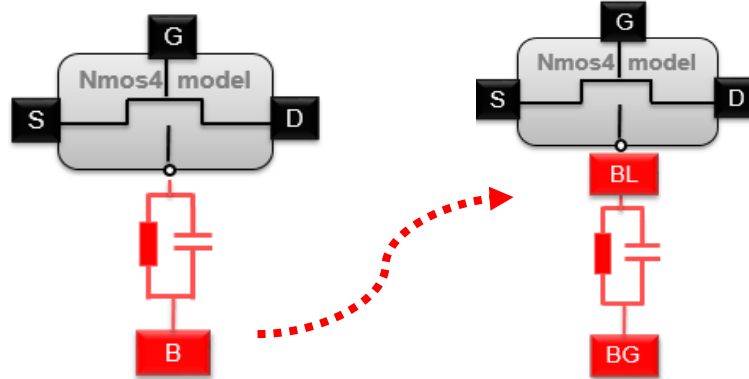


Figure IV. 14. Symbol of nMOS device: (a) without the external bulk, (b) the updated device to connect the 3D substrate model

This methodology, in contrast of the developed methodology previously required an additional step to account for substrate effect. The partitioning is then done on three steps:

- RC sub-block: represents the RCLK parasitic of backend interconnect metallization.
- EM sub-block: based on full wave simulation to handle accurately the various interaction between the Pads, the upper metal layer access and the MIM capacitors. The MIM capacitors need to be modelled with care due the thin dielectric used to make the capacitance and the losses induced in the substrate.
- 3D model: based on Finite Elements method to model the substrate impedance under the various component (MOS, resistors and diode) with the corresponding isolation technique(DTI). The main challenge is to define the boundary between the backend of the device (interconnect metallisation) and the frontend (substrate) to avoid a double parasitic counting. Also, the local body connection and the global ground are one of particular attention.
- 

Figure IV.15 (c) shows the additional step for substrate modelling; it requires more ports together with a layout simplification to speed up the run time simulation without impacting the accuracy.

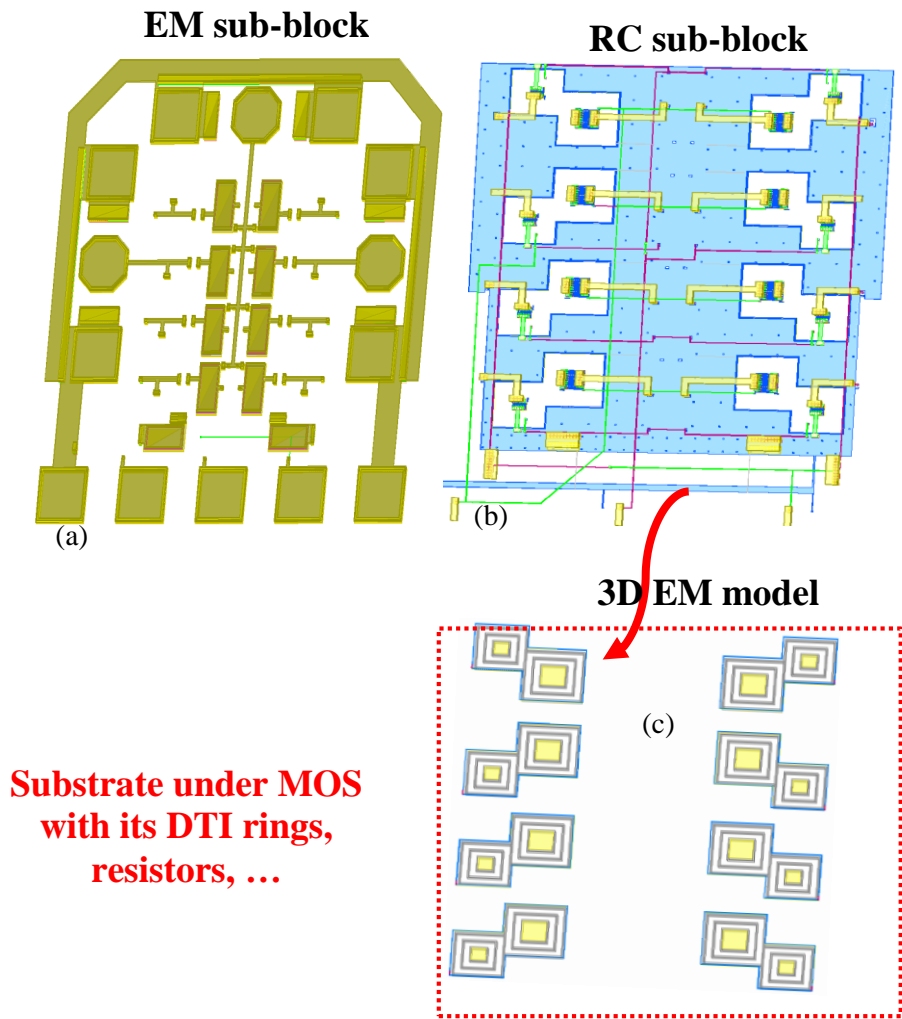


Figure IV. 15. From the initial layout of the RF switch (Figure.IV.12-a) to the passive blocks analyzed by EM (a), the active blocks with its backend parasitics (b), and the corresponding 3D substrate model (c)

The comparison between the two considered methods is performed upon accuracy and simulation run time. Then a correlation with measurements up to 20GHz is shown in Figure IV.16 The test bench of the overall design is describing the use of the he proposed layout based extraction methodology in comparison with the full wave methodology.

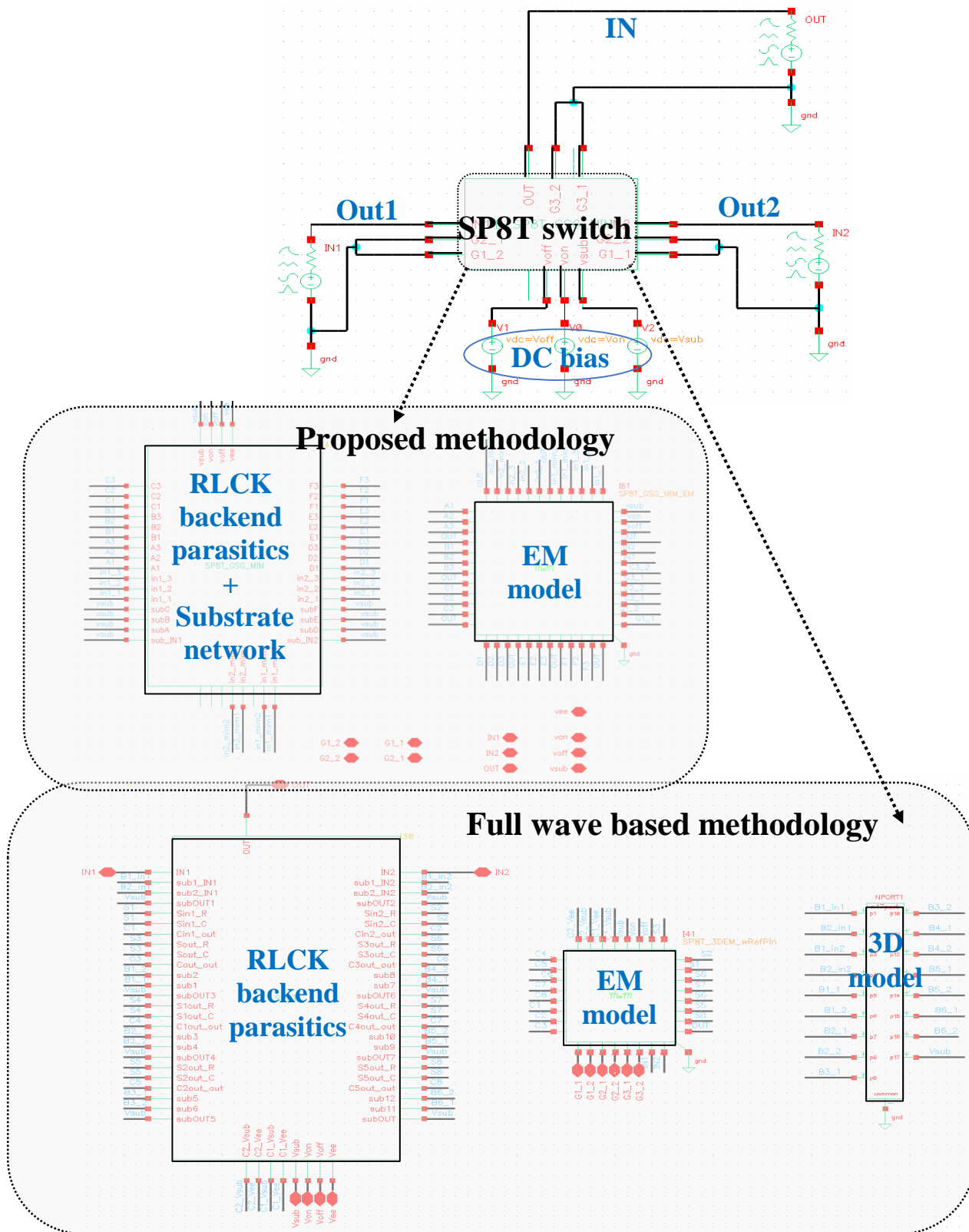


Figure IV. 16.SP8T switch test-bench (a)

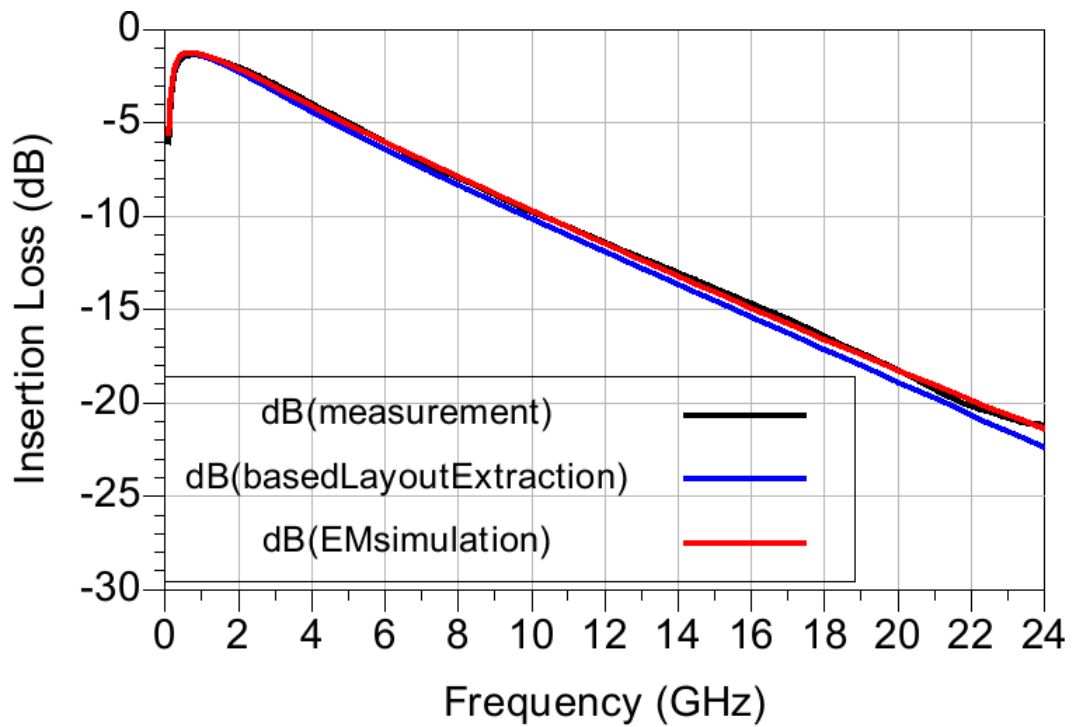


Figure IV. 17. Measured insertion loss of the SP8T switch in comparison with the proposed methodology and EM simulation (3D)

Table IV. 4. Comparative table between measurement, Layout based extraction and EM simulation

| @ 1.8 GHz      | IL(dB) | ISO (dB) | Run time   |
|----------------|--------|----------|--|
| Measurement    | 1.7    | 20       | Not applicable                                     |
| 3D model       | 1.7    | 18       | 2h30   |
| Proposed model | 1.7    | 18       | 33 min of extraction + 2 min of circuit simulation |

The proposed methodology, offers a considerable gain in run time with the required accuracy. In the overall frequency range, a good correlation between measurement and the predicted simulation based on both techniques developed above. In one hand, the based layout extraction methodology reproduces an equivalent accuracy to full wave simulation for the studied design, and on another hand this accuracy is validated by silicon measurement.

Thanks to the fact that the proposed methodology offers a good predictably up to 25 GHz, it can be extended to 5G application in the up to Ka band.

#### IV.2.2. Comparison of switch performances in various technologies

The table below represents a comparison between the SPDT switch performances in BiCMOS technology used in this study, with other switches' s performances obtained in different technologies (CMOS, SOI, CMOS on SOI and lower channel length in BiCMOS).

*Table IV. 5.Comparison of switches*

| Technology                                       | 0.18 $\mu\text{m}$ Bulk CMOS  | 0.18 $\mu\text{m}$ SOI CMOS        | 0.13 $\mu\text{m}$ SiGe BiCMOS | 0.25 $\mu\text{m}$ SiGe BiCMOS |       |
|--|-------------------------------|------------------------------------|--------------------------------|--------------------------------|-------|
| Substrate resistivity ( $\Omega\cdot\text{cm}$ ) | 11–16                         | 1000                               | 8 – 10                         | 200                            |       |
| Type   | SP3T                          | SPDT                               | SPDT                           | SPDTA                          | SPDTB |
| Frequency(GHz)                                   | 2.4                           | DC-40                              | DC-20                          | 2.4                            |       |
| Insertion Loss (dB)                              | 1.3                           | < 1                                | < 2                            | 0.9                            | 0.9   |
| Isolation (dB)                                   | 28                            | > 17                               | > 15                           | 15                             | 13    |
| Control voltage (V)                              | 3.3                           | 2.5                                | 2.5                            | 2.8                            |       |
| Topology   | Serie-shunt, with triple well | Serie-shunt, with matching network | Serie-shunt, with DTI          | Serie-shunt, with DTI          |       |
| Reference  | [IV.4]                        | [IV.5]                             | [IV.6]                         | This work                      |       |

The lower insertion loss is obtained using the SOI technology (Silicon On Isolator), this technology offers a fully isolated nMOS device thanks to buried oxide (BOX). It of course exhibits better isolation than SiGe, but minimizing IL involves a trade-off with other switch performance metrics such as isolation, bandwidth and signal handling capability and with low cost applications. Although the SOI has a temperature conductivity lower than BiCMOS which leads to some difficulties in high power devices.

In the presented SPDT switch, we could improve the insertion loss without changing the technology itself, thanks to the use of DTI. But the layout routing and the design topology need to be improved. Indeed, the insertion loss is very sensitive to the substrate losses but the design topology has also a marginal impact on parasitic optimization.



## Conclusions

This chapter presents the design methodology of the SPDT switch for which RF performances are extracted from S-parameters measurements. It has been shown that the asymmetrical case can give a comparable performance to the symmetrical switch in both On and Off states, this can help to give a good trade-off between the required accuracy and the footprint.

Several parameters were investigated, the substrate bias, the gate control and the substrate thickness: from the obtained results, neither impact of the substrate bias on the insertion loss nor on the isolation have been observed.

In addition, the substrate thickness impact was investigated. The switch was measured with two substrate thicknesses: 700  $\mu\text{m}$  and 80  $\mu\text{m}$ . In both cases a substrate tap (ptap) was located at the frontside.

We found that the position of the ground reference plan at the backside of the wafer has a marginal impact on performances in the studied range.

Then, a predictable and accurate methodology to simplify the modelling/simulation phase has been investigated. The proposed methodology offers a trade-off between the accuracy and ease of use, together with integration in the standard design flow. The simulation results demonstrate a satisfactory correlation with measurements results for all the various switches used (double and multi-throw). This methodology, integrated into the design flow could be a reference to study new strategies of insulation and can help saving a huge amount of time during layout optimization.

In the next chapter, we will focus on describing a highly linear, highly isolated and low loss RF switch including Bluetooth.

In order to achieve the best performances of the RF SP3T switch that will be described later, we need to take advantage from the substrate isolation strategies that we developed in the chapter II and with the design technique in order to ensure the trade-offs between the key parameters of the switch (linearity, Noise figure, fast switching time, low loss, high isolation).



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# Chapter V: Modelling methodology for a predictive analysis of substrate effects in RFIC design

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## Introduction

In this last chapter, we will present different layout variants of a RF switch to demystify the DTI use model for insertion loss, noise reduction and isolation improvement. These different test-cases are then evaluated with the help of the new quasi-static tool presented in the previous chapter.

In the first part, we will describe the SP3T used to support our investigations. The second part will be devoted to the analysis of results obtained with the different DTI implementations considered. In the third part, the modelling method is addressed, including both substrate extraction and the way the database partitioning was considered between backend and frontend. A comparison between simulations and measurements is performed in the last part.

## V.1. RF switch architectures and specifications

### V.1.1. Design description

The SP3T considered for this study is presented in Figure V.1. This RF switch is designed using NXP in-house 0.25um BiCMOS process [I-5].

The SP3T switch is designed in a series-shunt configuration. The series arms provide a low resistance path for the “On” branch, and shunt arms are used to improve the isolation of the switch by grounding RF signals on the “Off” side. A bypass mode is incorporated into the WLAN receiver to increase the dynamic range and to avoid distortion of the LNA [V-7].

The SP3T switch is capable of switching between WLAN receive, WLAN transmit and Bluetooth, as illustrated in Figure V.1.

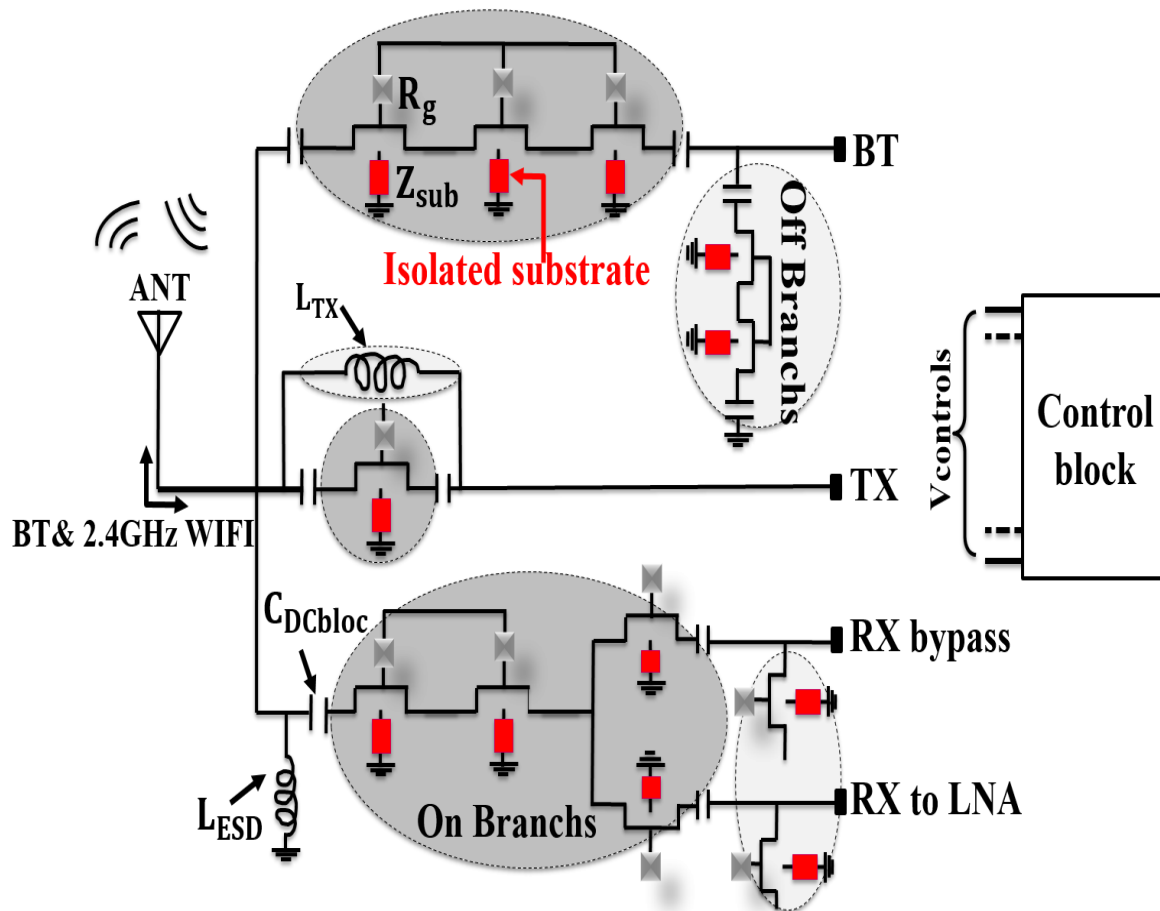


Figure V. 1. Schematic of the SP3T switch using series/shunt configuration and TX coil

When the transmit, mode is ON, the signal from the PA is fed into the transmit of the switch which is turned on. This allows the signal to be switched and propagated through to the antenna. In view of this architecture, one of the most critical specifications for the transmit and Bluetooth switch is the insertion loss. The maximum transmitted power of the system is reduced by the insertion loss of the transmit switch. Similarly, on the receive side, the insertion loss of the switch adds directly to the noise figure of the receiver.

The SP3T switch is controlled by a logic decoder with two inputs and three modes, as shown in Table V.1. When the RX mode is enabled, Vgtx is set to high since the switches are turned on when both Vg\_off\_bt and Vb\_off\_rx are high. The bypass mode is turned on when Vc2 is high and Von is low. The SP3T is matched on-chip and all necessary paths are dc blocked with MIM caps. The values of series dc blocking MIM caps are chosen to provide an optimal match at the frequency of interest.

*Table V. 1 Controller logic for FEIC operation*

| Control signal |      | Mode of operation |        |        |     | Mode name                 |
|----------------|------|-------------------|--------|--------|-----|---------------------------|
| C0             | C1   | Switch            |        |        | LNA |                           |
|                |      | ANT-RX            | ANT-TX | ANT-BT |     |                           |
| <b>Low</b>     | Low  | Off               | Off    | On     | Off | <b>ANT BT mode</b>        |
| <b>Low</b>     | High | Off               | On     | Off    | Off | <b>ANT TX mode</b>        |
| <b>High</b>    | Low  | On                | Off    | Off    | Off | <b>ANT RX bypass mode</b> |
| <b>High</b>    | High | On                | Off    | Off    | On  | <b>ANT RX gain mode</b>   |

### V.1.2. Design methodology

The number of shunt devices and series devices are critical to meet the isolation specification. The maximum power-handling capability of a switch depends on the maximum voltage swing that can be safely applied to the OFF-state switch at an antenna port as well as the maximum current flow limit in the ON-state switch. The latter can be easily solved by increasing the width of the device in the ON-state path, which is, however, accompanied by degraded isolation performance. The former becomes the main issue in designing high-power switches. There have been three different kinds of methods to improve high power-handling capability: in our case, we used stacked FET transistors.

At high frequency, the power handling of nMOS switches is limited by the voltage swing in the OFF-state and by current saturation in the ON state.

The off-state nMOS switches should support more than 30dBm which is equivalent to 10V across 50Ω. As the breakdown voltage of an nMOS device in BiCMOS technology is about 5V, then, the power handling capability is improved by stacking three FETs as shown in Figure V.3.

In other process technologies (CMOS) the number of the stacked nMOS switches can be increased due to the low breakdown voltage comparing to BiCMOS SiGe technology limiting then the voltage swing [V-15].

By stacking transistors at the OFF-state path, the RF voltage swing at the OFF-state path can be evenly divided within the stacked FETs, so that the voltage handling capability increases approximately by 3 times.

As the number of stacked transistors increases, the power-handling capability can be improved [V-5] [V-6] [V-7]. However, the stacked FETs switch will create higher insertion loss than a single FET switch. Thus, the increased power handling typically comes at the cost of higher insertion loss.

Insertion losses in RF switches is generally attributed to three factors:

- The finite resistance of the series devices,
- VSWR losses due to the mismatch at the terminals of the switch,
- Passive elements (inductors, transmission lines, conductors...) due to the parallel substrate resistance.

The straightforward method to minimize the insertion loss is enlarging the size of the switch. However, the parasitic capacitances also increase, resulting in high substrate coupling. Otherwise, the large nMOS is not desirable from the perspective of power-handling capability, as well. The enlarged junction diodes can provide a low-impedance path by forward-biasing when a large signal flows, deteriorating the power performance, eventually

Therefore, the size of the FETs has to be defined with care, and some new design techniques and isolation strategies are needed.

#### **a. LC resonator in TX mode**

When Tx mode is in operation, shunt FETs at the Rx and BT mode needs to be ON state to bypass leaking power to ground to protect the receiver/Bluetooth blocks. The location of the shunt device in each configuration can vary to obtain the best performance in terms of improving isolation as well as insertion loss at each Rx/BT path.

The correct balance between on-resistance and parasitic capacitance requirements must be established to size the devices correctly. Smaller device has higher OFF-state impedance than a larger device; in other words, a smaller device has a better isolation performance a than larger device. While a wider device allows lower on-resistance and thus lower insertion loss, it also has higher capacitance in off-state, leading to a higher insertion loss for other 'on' switch paths (Bluetooth and receive) in the SP3T.

We summarize the relationship between the device size and the substrate impact in Table V.2 Table V.2 represents the relationship between the nMOS size and the substrate coupling.

Table V.2. Substrate impact as function of the nMOS size

| W (μm) | Frequency(GHz) = 2.4  |          |                  | Frequency(GHz) = 5.8  |          |                  | R <sub>on</sub> (Ω) | C <sub>off</sub> (fF) |
|--------|-----------------------|----------|------------------|-----------------------|----------|------------------|---------------------|-----------------------|
|        | R <sub>sub</sub> (KΩ) | FOM (fs) | Substrate impact | R <sub>sub</sub> (KΩ) | FOM (fs) | Substrate impact |                     |                       |
| 100    | 1.9 e+4               | 305      | 1.6 %            | 1.28 e+4              | 305      | 2.4 %            | 10                  | 30                    |
| 200    | 1.34 e+4              | 314      | 4.7 %            | 9.05 e+3              | 321      | 6.9 %            | 5                   | 60                    |
| 300    | 1.10 e+4              | 326      | 8.6 %            | 7.39 e+3              | 338      | 12.7 %           | 3.33                | 90                    |
| 400    | 9.49 e+3              | 340      | 13.2 %           | 6.40 e+3              | 359      | 19.5 %           | 2.5                 | 120                   |
| 500    | 8.49 e+3              | 355      | 18.4%            | 5.72 e+3              | 382      | 27.3 %           | 2                   | 150                   |
| 600    | 7.75 e+3              | 373      | 24.2%            | 5.22 e+3              | 408      | 35.9 %           | 1.67                | 180                   |
| 700    | 7.17 e+3              | 392      | 30.5 %           | 4.83 e+3              | 436      | 45.2 %           | 1.43                | 210                   |
| 800    | 6.71 e+3              | 412      | 37.3%            | 4.52 e+3              | 466      | 55.3 %           | 1.25                | 240                   |
| 900    | 6.32 e+3              | 433      | 44.5 %           | 4.26 e+3              | 498      | 66.0 %           | 1.11                | 270                   |
| 1000   | 6 e+3                 | 456      | 52.1 %           | 4.05 e+3              | 532      | 77.3 %           | 1                   | 300                   |

The transmit path of the switch (TX) is constructed with a single nMOS device (width = 1mm).

To support the TX port operating under higher power, three transistors are placed in the receive path and the Bluetooth path.

As the lower insertion loss reached by a wider device comes at the cost of higher insertion loss, we opted for a resonator coil to increase the transmitter's isolation and bridge this gap. The TX coil is designed to resonate at 2.4 GHz in parallel with C<sub>off</sub> of the TX path [V-11]:

$$f = \frac{1}{2\pi\sqrt{L C_{off}}} \quad (V-1)$$

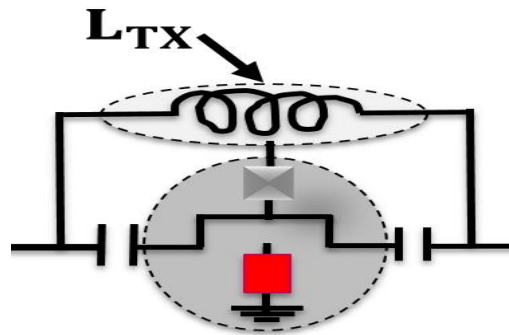


Figure V. 2. Schematic of the Transmit mode using TX resonator coil

A single nMOS switch has ~ 0.1 dB loss at 2.4GHz, in the series-shunt configuration, it will be added to this loss the contribution of the off paths (BT and RX), the shunt elements, and the parallel substrate loss due to the ESD diode and TX coil. An insertion loss of 0.7 dB in the TX path with an isolation

superior than 20 dB, a return loss less than 10 dB and a CP1 superior than 30dBm are then expected. The substrate plays a significant role on the figure of merit of switch, it is mandatory to anticipate the substrate loss and to prevent its damage in order to maintain the expected performances.

Furthermore, the transmit path needs to handle more than one-watt (30 dBm) of RF power while maintaining minimal insertion loss. Which is equivalent to 10V.

To fix the adequate number of the stacked devices in the off-paths (RX and BT). It is mandatory to define the maximum voltage produced by the power in the TX path under the VSWR (Voltage Swing Wave Ratio).

$$V_{max} = V_p \left(1 + \frac{VSWR-1}{VSWR+1}\right) \quad \text{with } V_p = \sqrt{2 \times P(\text{watt}) \times Z_0} \quad (V-2)$$

### **b. Multi-Stacked FETs in RX and BT branches**

The voltage swings 10 V peak-to-peak when a signal of 30 dBm is transmitted into 50  $\Omega$  on the transmit throw. The power-handling capability of the RF switches is dominated by the maximum voltage swing over the off-switch devices. The channels and junction diodes of the off-state devices, is influenced not only by the device characteristic (threshold voltage) but also by the lossy silicon substrate (junction diode turn-on voltage). The voltage swings to carry the 30dBm in TX path is too large to be sustained by a single nMOS device, resulting in not only device breakdown but also leakages through the switch device and the substrate. Therefore, the most important design consideration in designing RF switches is to relieve the voltage swings over off-switch devices to secure the linear power transmission.

Thus, the BT switch in “off” state should be able to tolerate this voltage swing without any of the series FETs turning “on”. A stack of three series FETs is used in the Bluetooth (Or Receive) throw to withstand the high transmit voltage swing, as shown in Figure V.3. Additionally, it should not dissipate significant signal power and should maintain good isolation between transmit and Bluetooth (or Receive) ports. The transmit throw also needs to have a good isolation in the BT (or RX) mode so as not to draw power from the antenna (ANT), which would increase insertion loss.

The Receiver has two modes of operation: high-gain and bypass mode.



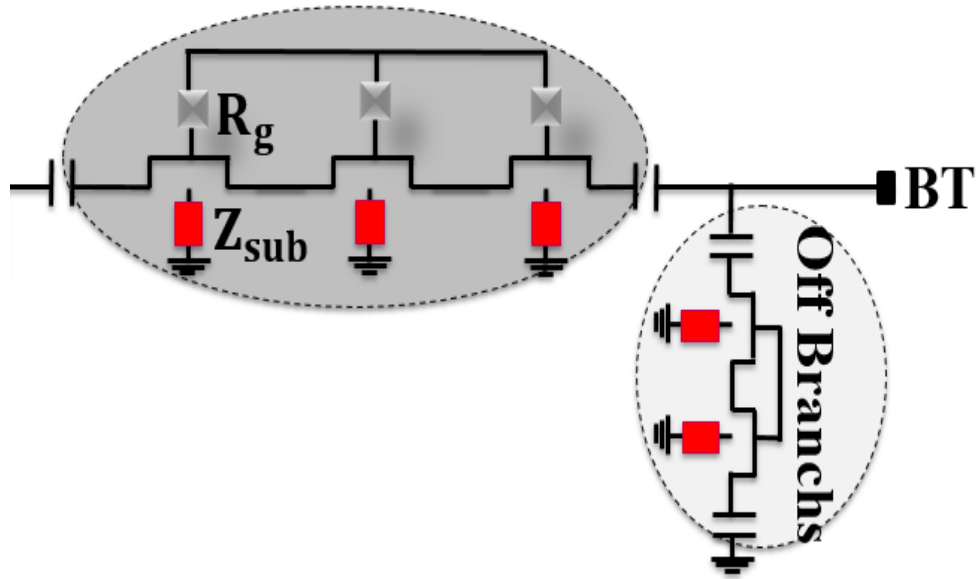


Figure V. 3. Schematic of the Bluetooth mode using multi-stacked nMOS

For a transistor with a total channel width of  $1000\ \mu\text{m}$ , of which the gate and source (drain) are biased at  $2.5\text{V}$  and  $0\text{V}$  respectively, the simulation-derived on-resistance  $R_{on}$  is about  $1\ \Omega$  and a  $C_{off}$  is about  $300\text{fF}$ . Referring to table V.2, this wider device has a lower  $R_{on}$ , but it suffers from higher substrate losses.

The shunt leakage via the substrate and the parallel substrate coupling from the coil and the access paths will be added to the series losses.

To this it will be added the losses of the shunt path, the off paths and the contribution of parallel losses from the inductors. The Bluetooth mode should maintain then an insertion loss around  $0.9\ \text{dB}$ .

Since the transistors used have parasitic and the silicon based technology is limited by the lossy characteristics of the substrate, we must avoid connecting the body of the nMOS transistors to a low impedance node in order to get rid of leaky paths through the substrate (Figure V.4). This can lead higher insertion loss of the “On” branch and thus higher Noise Figure (NF). A trade-off must be then found on the device size. The wider transistor the lower losses at low frequencies, but higher interaction with substrate. DC blocking capacitors are also added on each series and shunt branches to allow a deep-off biasing of nMOS when set to “Off” state.

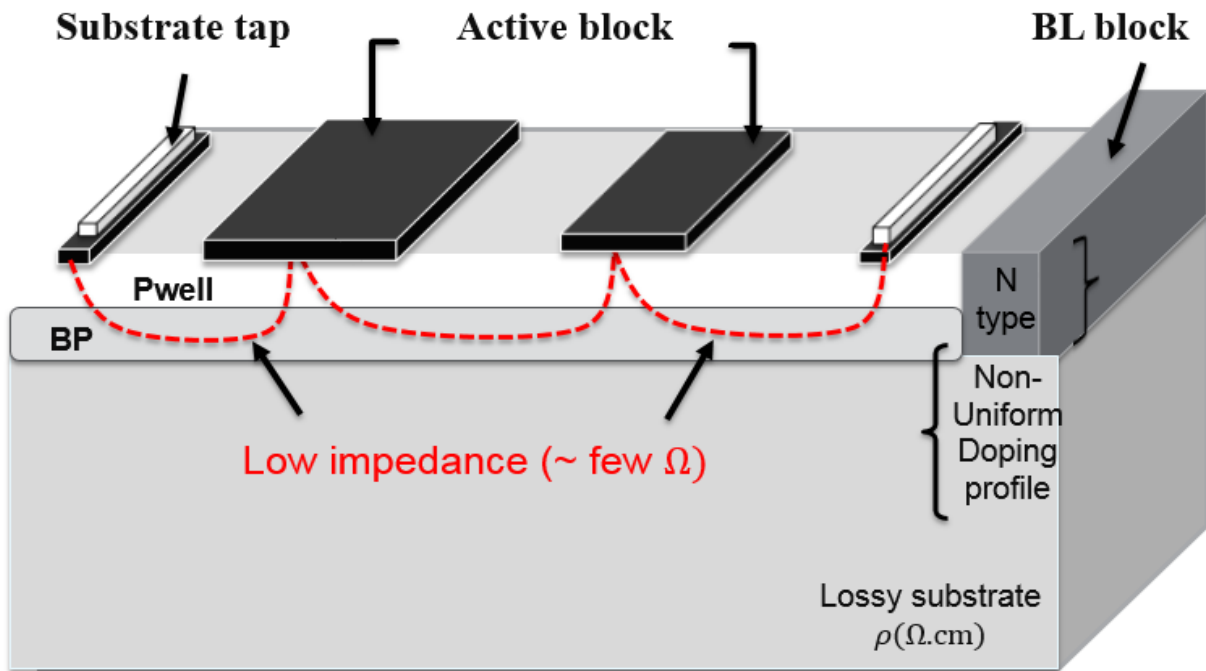


Figure V. 4. Substrate coupling of non-isolated nMOS switches

To increase the impedance path of undesired coupling, an isolation technique based on DTI is used to break both epitaxial and buried layers. Its thickness is around 6  $\mu m$ . It is already widely used below passive devices to reduce parasitic capacitances and substrate related losses (Figure V.5) [V-16]. The buried layer (BL) is indeed more conductive than the bulk substrate and so provides lowest impedance paths to coupling paths.

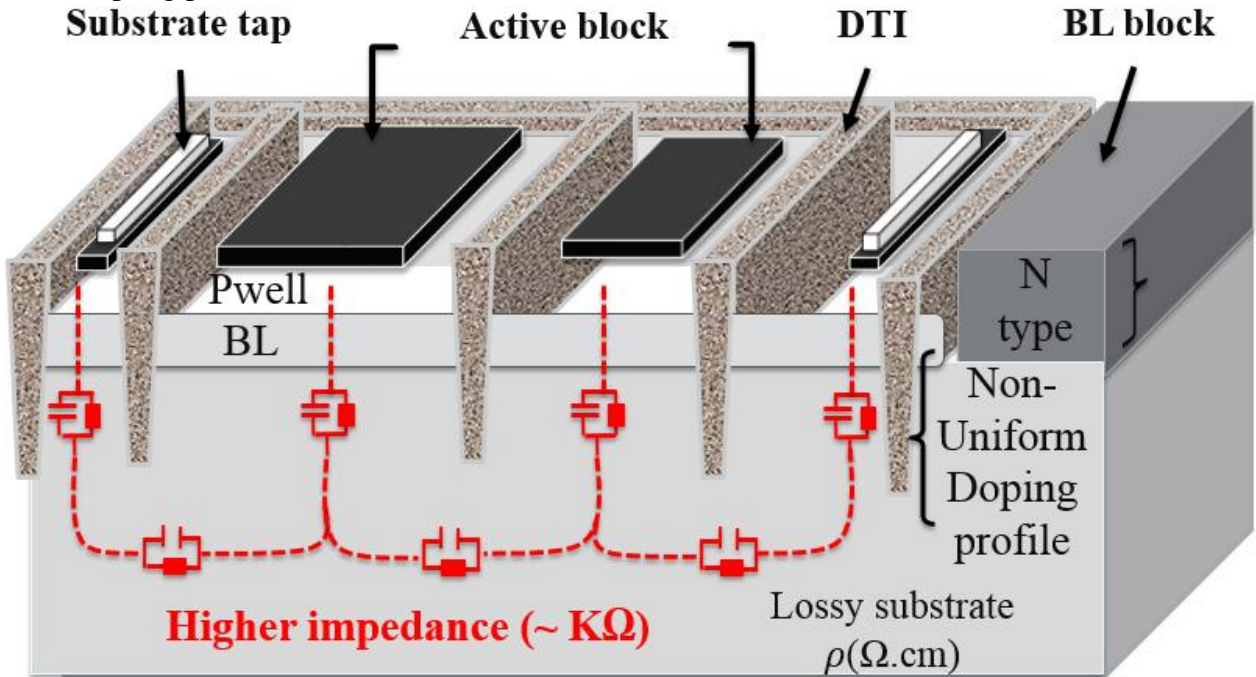


Figure V.5. Influence on the substrate impedance of introducing Deep Trench Isolation-DTI

### c. ESD protection design consideration

The design requirement imposes constraints for ESD design of an RF switch. In order to provide enough immunity against ESD stresses, ESD protection circuits must be provided to all Input/Outputs pads in the ICs as shown in Figure V.6.

However, the parasitic capacitance in the ESD protection circuit degrades the circuit performances [V-12]. The negative impacts of ESD protection circuits on the design performances had been investigated [V-1].

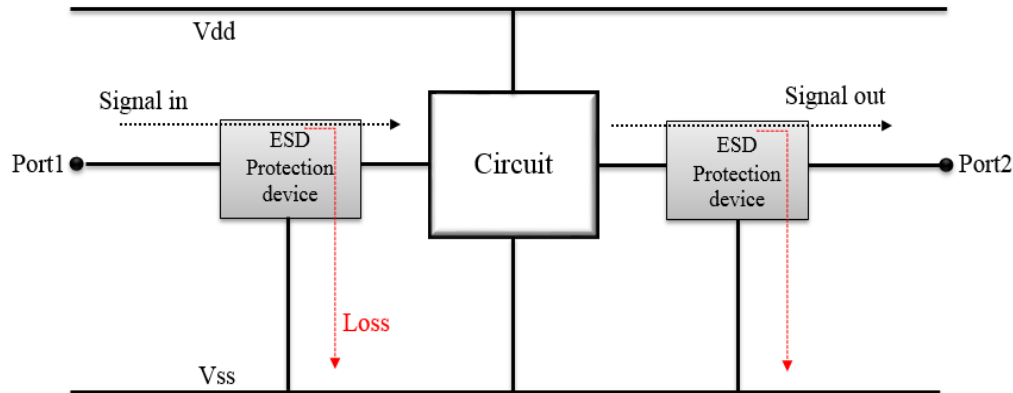


Figure V.6. Signal loss at input and output pads of RFIC with ESD protection devices

The Parasitic capacitance is one of the most important design consideration for RFICs. The ESD protection devices with large dimensions have the parasitic capacitance which is too large. Moreover, for the RF circuits, the parasitic capacitance of ESD protection devices causes signal losses from the pad to ground, as shown in Figure.V.6. Furthermore, it causes RF performances degradation on several aspects: noise figure, power gain and input matching.

In this design, we will use an ESD coil. The difficulty of this technique is related to the parallel substrate resistance. The goal is to create an impedance which is low enough to act as a short at DC, but high enough to act as open at operating frequency.

Noise figure is one of the most important merits of the RF circuit. Since the RF switch is a cascade of several stages, the overall noise figure of the RF receiver can be obtained in terms of the noise figure and power gain of each stage in the receiver. With the ESD protection circuit added at the input pad to protect the RF switch against ESD damage, the ESD protection circuit becomes the first stage in the RF switch.

To provide ESD protection, and reduce the performances degradation due to ESD protection devices, circuit design techniques had been used in order to reduce the parasitic capacitance from ESD protection circuit.

- **Typical ESD protection scheme**

The typical ESD protection circuit scheme is based on a double diode at I/O pad, as illustrated in Figure V.7 can directly shunt the positive and negative stress pulses to the grounded power pulse vdd or vss [V-14].

In the optimization of the ESD diodes, the diode size should be large enough to have a small on resistance to shunt the ESD current but small enough to meet the low capacitance requirement for RF applications.

As the diode size becomes larger, the increased substrate parasitic capacitance  $C_{sub}$ [V-2] is responsible to the increased loss of the diode at high frequencies, which creates a low-impedance signal path to the substrate.

In order to reduce the performances degradation caused by the parasitic capacitance from ESD diodes at I/O pad, stacked diodes in series can be used to replace the diodes in Figure V.7 to obtain lower (total) capacitance. The price is the increased voltage drop across the diodes as well as a large silicon area.

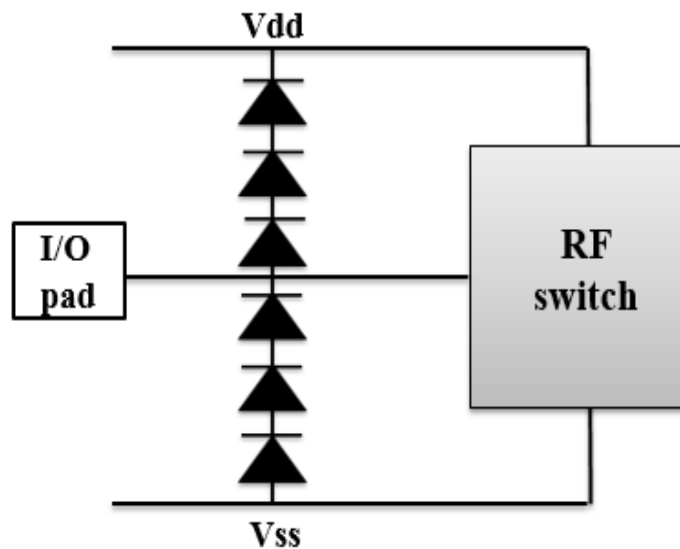


Figure V.7. Typical ESD protection scheme with stacked diodes

From equation (V-2), the power in the TX paths may produce a voltage superior to 10 V at which requires more than 7 diodes to protect the circuit from the negative swing and 5 diodes for the positive swing. These stacked diodes for ESD protection will be placed to each input/output pad (ANT, TX, RX, BT), which leads to larger area.

In addition, Power handling capability is assumed to be limited by the maximum voltages that the well junction diodes can sustain. The voltage of the junction diodes DNW-Pwell and DNW must not exceed 0.7V and -9V to avoid forward biasing and reverse breakdown, respectively.

The former degrades linearity of the switch while the latter damages the junction diode.

The systematic circuit characterization suggests that full-design ESD protection must be thoroughly examined by checking all critical circuit specifications, not just the ESD leakage behaviours, and different circuit parameters may be affected by ESD differently. The linearity is a key challenge that may only be addressed by if high ESD protection is required. which is one of the main focus of this section.

In this work, differing from the diode-based approach, we proposed using a shunt inductor (Figure V.8) [V-13] for ESD current to realize a robust ESD protection while maintaining a low noise figure and high linearity.

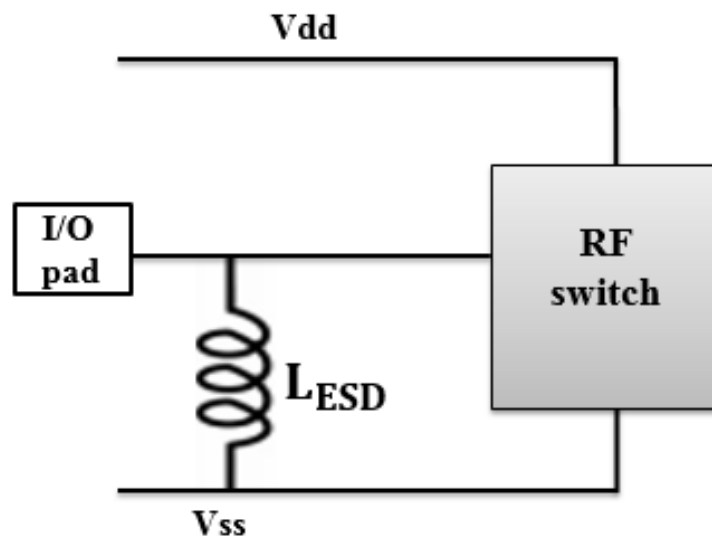


Figure V.8. ESD protection scheme with shunt inductor

The ESD diode suffers from a parasitic substrate diode. This parasitic diode needs to be isolated by a high substrate impedance (Figure V.9). However, this needs accurate substrate modelling to define the equivalent substrate network. In addition, this substrate effect plays a marginal role in the linearity of the switch.

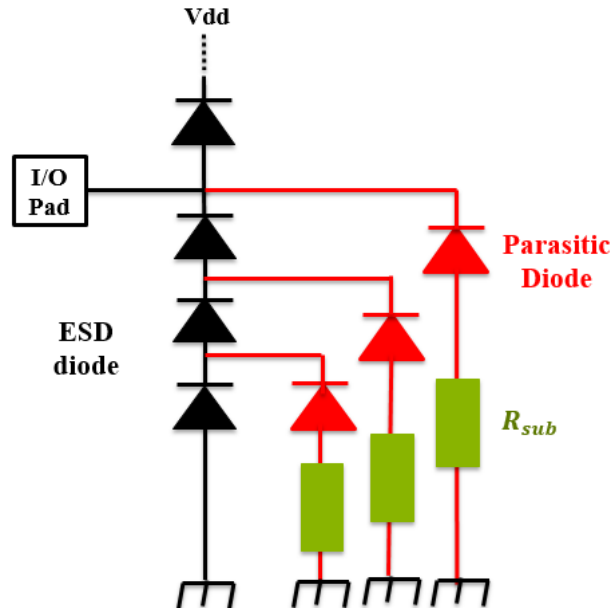


Figure V. 9. ESD diode with its corresponding parasitic diode

Three techniques of ESD protection in the SP3T switch were evaluated in respect of the switch linearity:

- ESD coil: a shunt coil is designed for ESD protection.
- ESD stacked diodes with a substrate pin connected to the global ground
- ESD stacked diode isolated by a high substrate impedance (figure V.9)

The three test cases were simulated and compared in table V.3. The higher 1dB compression point is obtained using the ESD coil. The stacked diode suffers from the substrate effect. And the worst CPI is obtained with a non-isolated diode.

Figure V.10 presents simulated SP8T linearity, showing severe degradation caused by ESD protection using the stacked diodes, which is reduced to only 1 dB after coil ESD concurrent design.

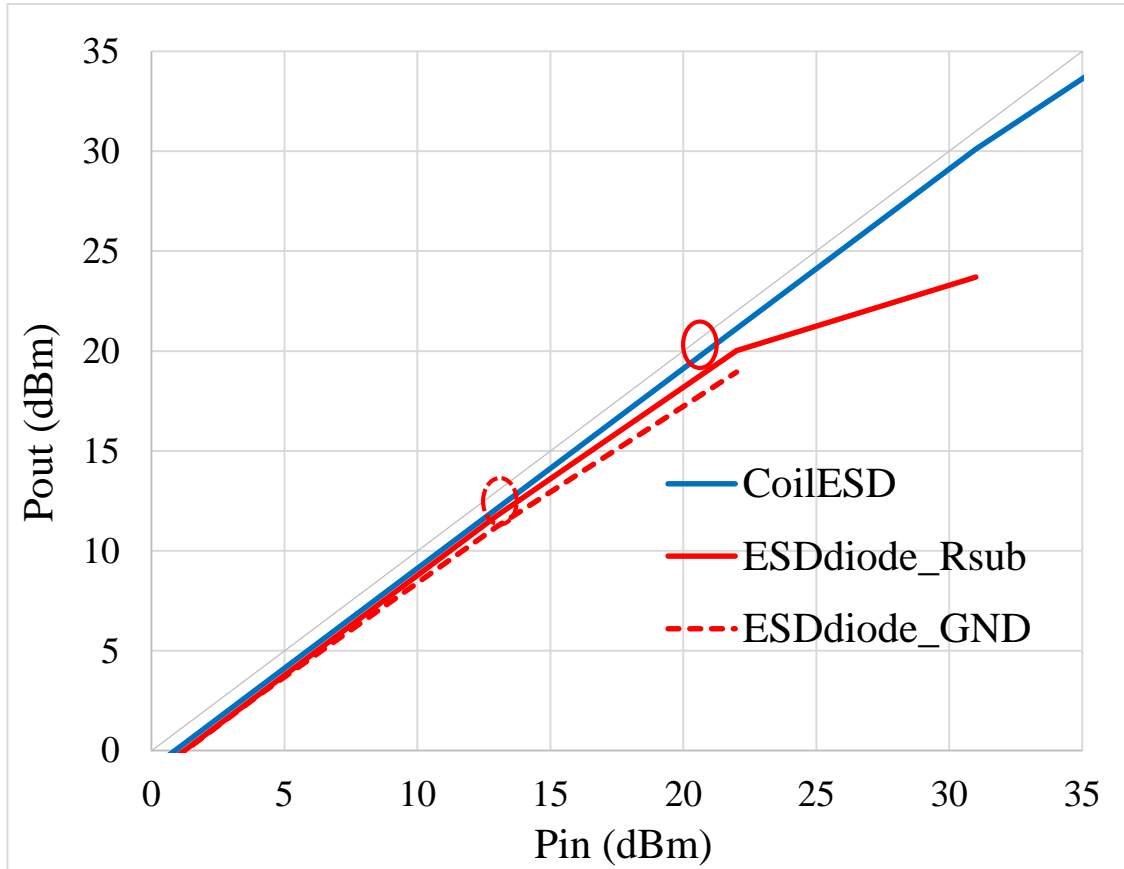


Figure V.10. ESD protection using ESD coil vs ESD diode with and without substrate resistance, show ESD impacts on switch linearity

Table V.33. Compression point 1dB function of the ESD protection technique

| ESD protection  | CP1 (dB) |
|---|----------|
| ESD coil  | 32       |
| ESD diode connected to the ground                                     | 14       |
| ESD diode connected to a high substrate resistance ( $\sim K\Omega$ ) | 20       |

Since the frequency component of ESD current is much lower than that of the RF signal, the inductor-based protection can thus exhibit high impedance at normal states and low impedance during ESD

events. The inductor can bypass the discharge current directly to the ground via  $L_{ESD}$  during an ESD event, and further blocks the ESD current by  $C_{DCBLOCK}$  to protect the internal circuit.

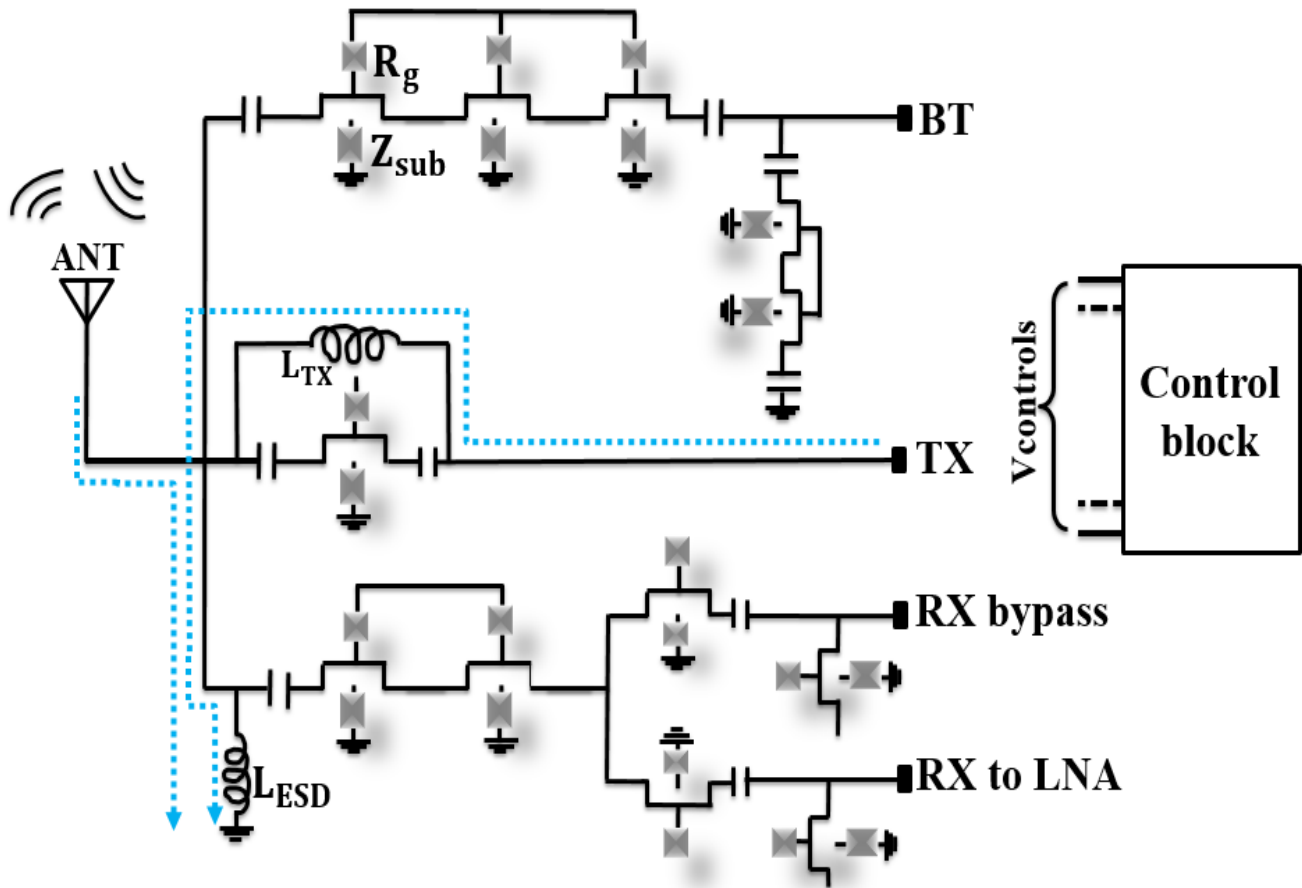


Figure V.11. ESD evacuation path of Antenna and the TX

However, this inductor will participate to losses mechanism for every mode (BT, TX and RX). Special care must be paid-off to its implementation regarding parallel losses. In that sense, coupling with substrate must be minimized as much as possible to be transparent for RF.

### V.1.3. Test Case Descriptions

In order to investigate the effect of the Deep Trench Isolation performances and its capability to reduce substrate coupling, the four test cases of SP3T shown in Figure V.12 have been implemented on Silicon and then measured against frequency (on-wafer measurements up to 10 GHz). The active block represents all the nMOS switches used in series and shunt arms of the SP3T switch.



In the first structure, nMOS switches bulks are connected to substrate taps without any isolation. This structure is used as a reference for comparison purpose. For all other structures, different isolation strategies have been considered (either base on one or more DTI rings or DTI mesh).

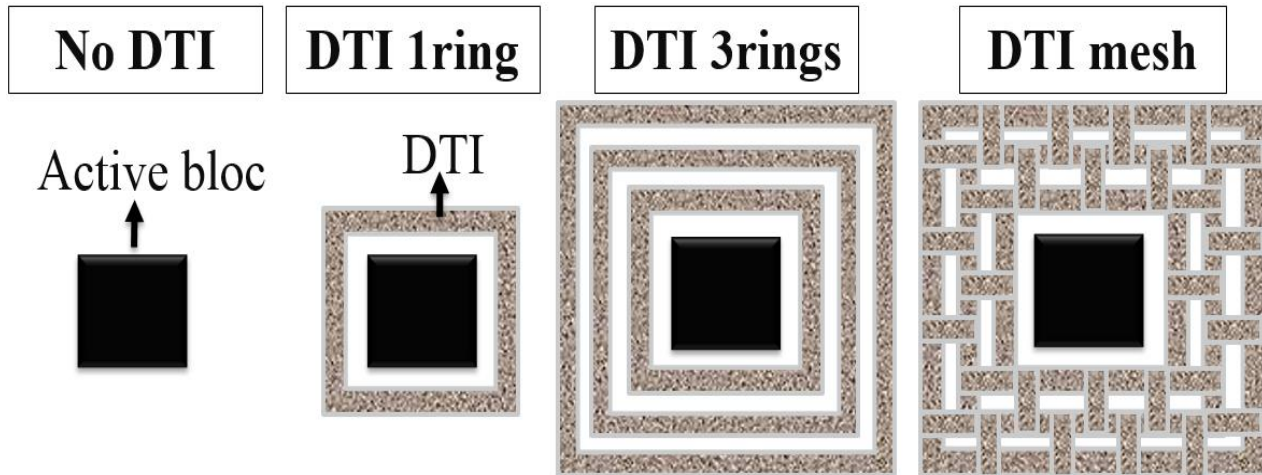


Figure V.12. Top view of different configuration of DTI and reference structure without isolation

#### a. RF Characterisation Strategy

The designed test-cases SP3T were fabricated using NXP 0.25  $\mu\text{m}$  BiCMOS process technology with silicon substrate resistivity of 200  $\Omega\cdot\text{cm}$  and a thickness of 700  $\mu\text{m}$ . The active devices used in this design are nMOS transistors with DTI isolation.

A microscopograph of the fabricated die is shown in Figure V.13. The chip dimensions are 0.98 mm x 0.6 mm<sup>2</sup> including dc blocking MIM capacitors and signals Pads.

The SP3T structures were measured using network analyser (VNA). Four-port (GSGSG) S-parameter measurements were performed for each structure in the frequency range [100 MHz - 8 GHz] with a grounded wafer backside. Prior to measurements, SOLT calibration has been performed on a separate cal-kit from 1 to 8 GHz.

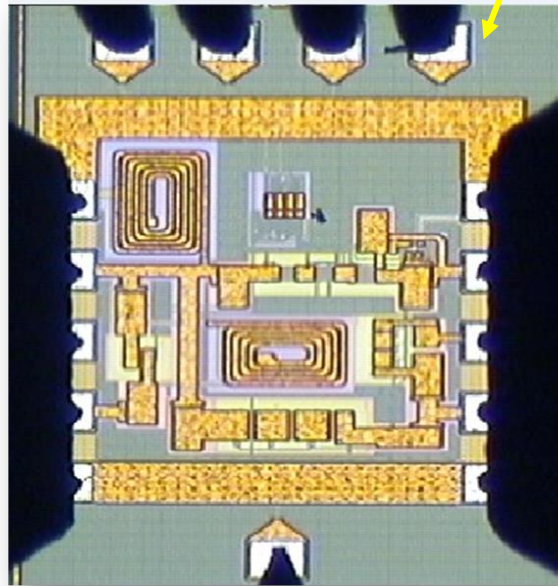
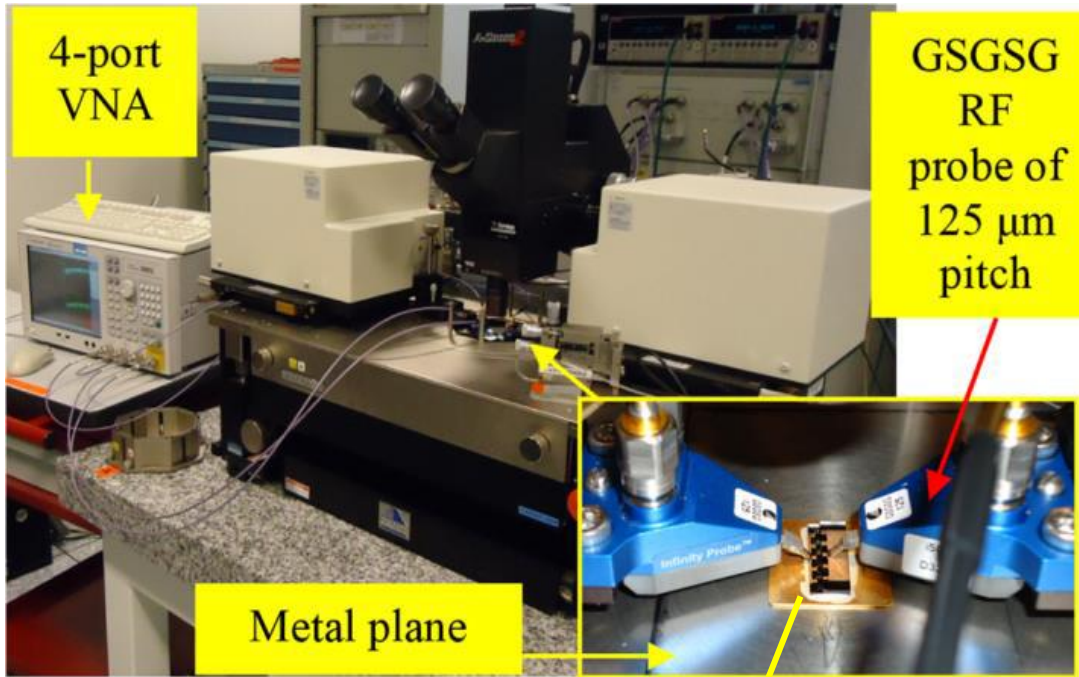


Figure V. 13. Measurement set-up of SP3T switch

## b. RF Characterisation Results

The SP3T switch has four ports ANT, RX, TX and BT as shown in Figure V.1. The propagation of the signal between the antenna and the BT, TX or RX port is commanded by a control block. The impact on insertion loss, isolation in TX mode together with input return losses of different layout options of Deep Trench Isolation is presented in Figure V.14, Figure V.15 in comparison with a reference structure without DTI.

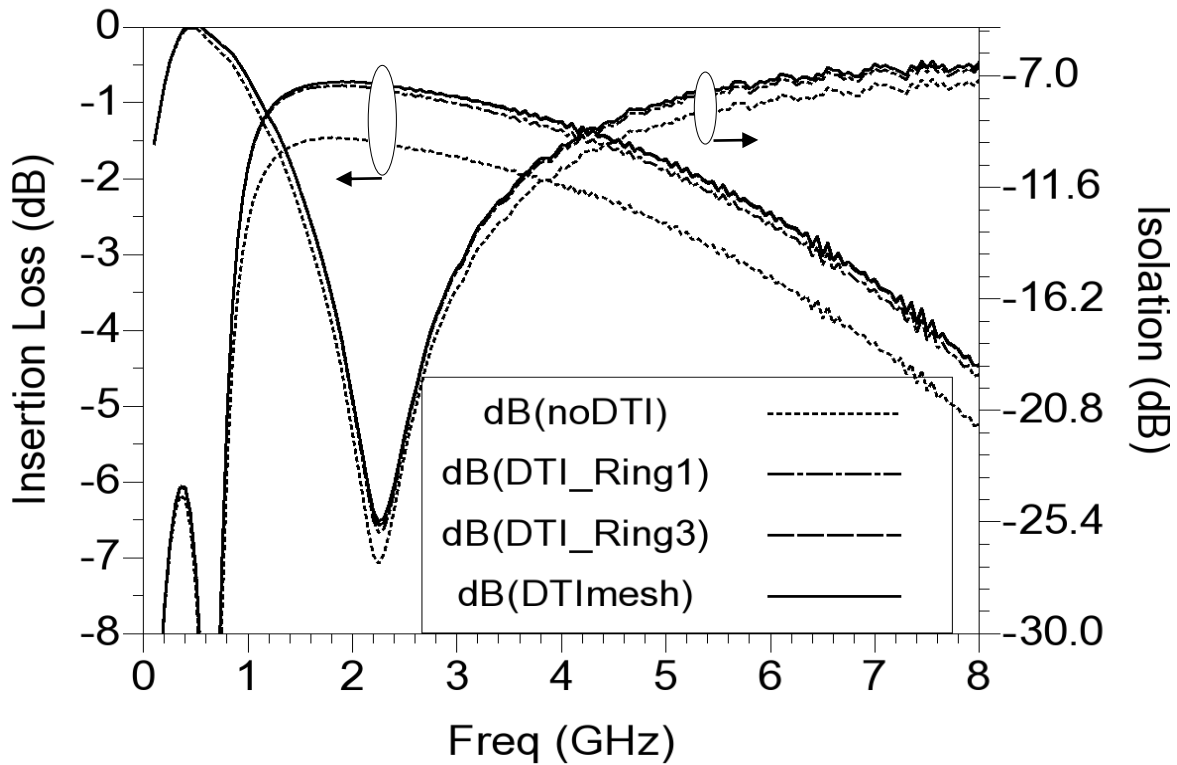


Figure V.234. Measured variations against frequency of insertion loss and isolation in TX mode

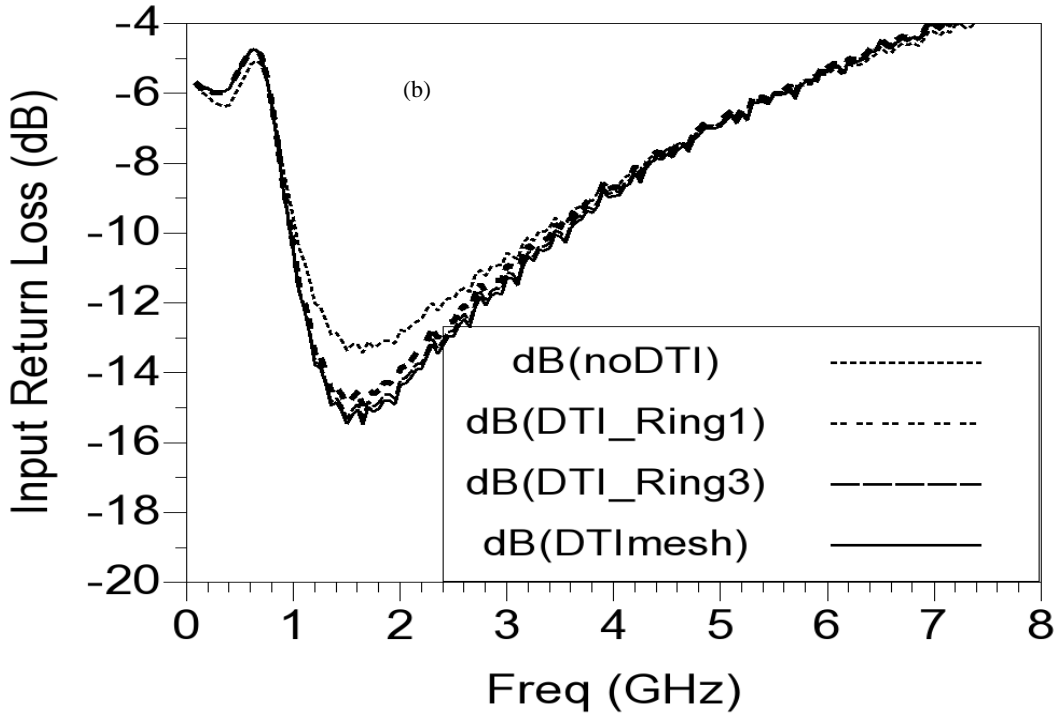


Figure V.15. Measured variations against frequency of and return loss and isolation in TX mode

Comparison between various DTI options from measured TX modes are reported in the table V.4.

Table V.4. Comparison of Different Measured Configurations

| Isolation strategy | TX mode at 2.4GHz |         |         |
|--------------------|-------------------|---------|---------|
|                    | IL(dB)            | ISO(dB) | IRL(dB) |
| No DTI             | 1.57              | 24      | 12      |
| DTI_1ring          | 0.86              | 24      | 13      |
| DTI_3ring          | 0.79              | 24      | 13      |
| DTI_mesh           | 0.79              | 23      | 13      |

Couplings dependence against DTI configurations is evaluated in Figure V.15 and table V.4.

The Deep Trench Isolation improves the SP3T performances in comparison with reference SP3T structure without DTI. Increasing the number of DTI rings improve performances but adding more than 3 DTI rings has a marginal impact on overall performances. The case of SP3T switch with DTI mesh

option has no significant impact versus version with 3 rings options meaning that breaking the buried layer with a perpendicular DTI has the major impact on the coupling reduction. This point is of particular relevance as footprint can be reached based on the implementation done with 2, 3 rings.

#### **V.1.4. Modelling Methodology**

In RF switch cases, the integrated circuit comprises several inductors as, transmission lines and other loop as the seal/guard ring. Lets' consider the example on Figure V.16: interactions between the different components are necessary to analyse, however currently, no EM tool using any kind of numerical method could afford to analyse electromagnetically an entire IC because of its complexity. The analysis should then define a partitioning strategy in order to highlight the function blocks, the components or metallization to be investigated and remove all the other elements from the layout to be analysed.

- **Modelling Strategy**

Evaluating EM (ElectroMagnetic) coupling effects on the SP3T switch performances with its highly complex architecture (active, passive components and the related interconnections) is key to reduce design iterations. Then, it must be able to deal with buried structures, including substrate contacts, DTI and all other anisotropic layers.

3D FEM based simulators are indeed the most efficient ones to tackle this kind of issues (provided that coupling phenomenon are EM related and not solid-state physics – in that case a different simulator must be considered). On the other side, these 3D FEM tools are quite complex to setup and requires huge memory and computation time. According to our knowledge, only Maxwell simulator [x] is able to deal with both Boltzmann and Maxwell equations.

A partitioning methodology is proposed for modelling and analysis of the SP3T switch. This partitioning methodology is developed based on two different strategies and have been applied using 3D and 2.5D electromagnetic solutions. The accuracy of proposed partitioning methodology is compared to full wave simulation results and measurement.

The objective of partitioning strategies is to segment a complex circuit into sub-blocks to analyse separately and then combine, later on, for global performances analysis. Although the partitioning strategies help to speed up the simulation run time.

To apply the proposed partitioning methodology (illustrated in Figure V.17 and V.18) the test cases in Figure V.16 are considered. The proposed strategy is investigated based on the following steps:

The first step is the partitioning of the physical layout topology into sub-blocks to analysis separately.

The second step is combining the extracted S-parameters multi-ports with the appropriate connections in the circuit analysis environment to synthesize the global response of the whole structure).

The last step consists of a comparison between both methodologies: Full-wave simulation technique and the based layout extraction and then, a correlation with measurements results is performed.

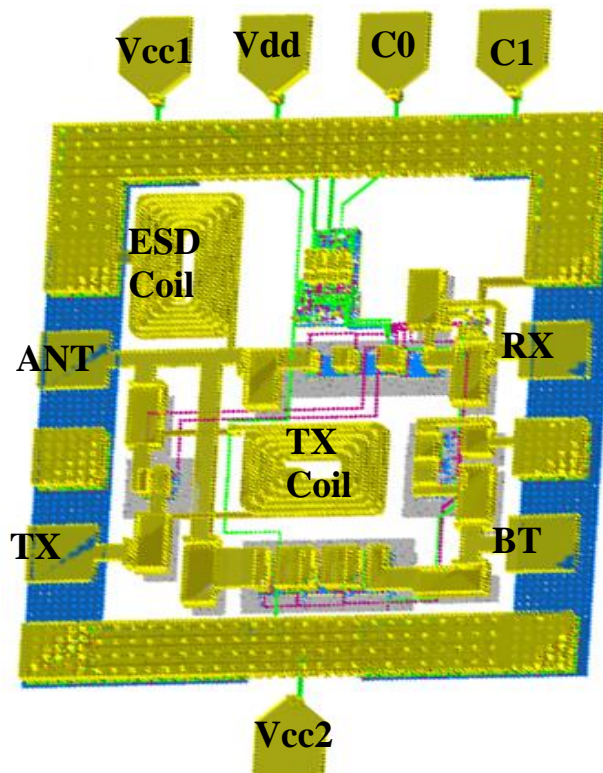


Figure V.16. Topology of SP3T switch

This starting step requires proper analysis and expertise of the specific structures in order to define appropriate sub-blocks frontiers. Once the sub-blocks are defined, the associated S-parameter models are extracted. The resulting sub-blocks are derived in terms of multi-port elements; the size of the multi-ports being determined by the number of used port excitations. Trade-offs between low run time, straightforward flow and accuracy over the overall frequency response impose optimal partitioning strategy.

Two different partitioning strategies for the SP3T are described below:

➤ **Strategy I: Full wave simulation**

This methodology couple properly the backend parasitic extraction to full wave simulation (2.5D analysis together with 3D analysis):

The quasi-static backend parasitic extraction deals with parasitic capacitance, inductance and resistances of backend metallization.

Full wave simulation is represented by a hybrid solution 2.5D / 3D: the various interactions of passive elements are modelled using 2.5D analysis, and the substrate including the introduction of the DTI needs a resolution in special domain. A 3D analysis is then applied for substrate modelling.

Figure V.17 illustrate the full wave based methodology applied to the SP3T switch.

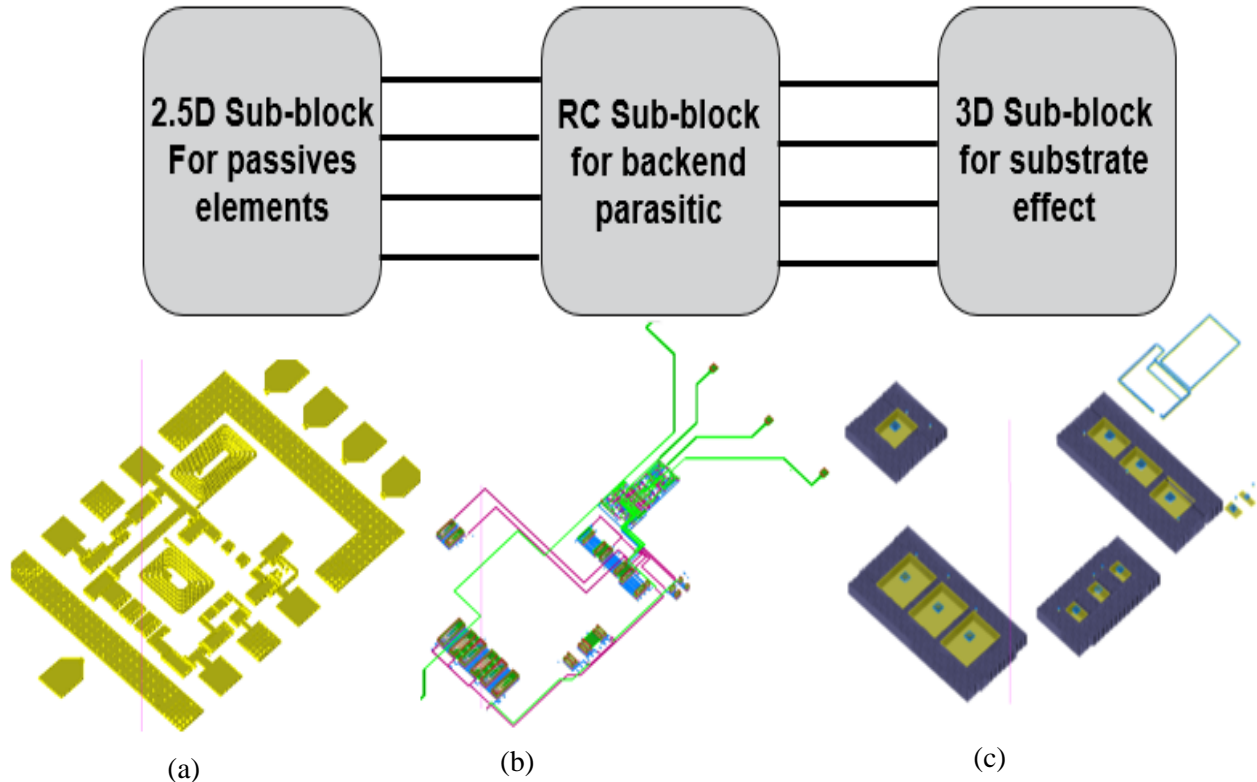


Figure V.17. The initial layout of the RF switch (Figure V.16) is fragmented based on strategy I, to the passive blocks analyzed by EM (c), by taking into account the active blocks with its DC access (b) and the substrate coupling (c)

➤ **Strategy II: Layout based extraction for inhomogeneous substrate extraction**

The proposed methodology combines the benefits of 2.5D EM analysis that properly handle the different EM behaviour (eddy current losses, skin effect...) with the advantage of layout based parasitic extraction technique to account for interconnect parasitic metallization and inhomogeneous substrate. This methodology extracts the distributed RC substrate network using a 3D description: conductivity at any point (x, y, z) based on the doping profile information.

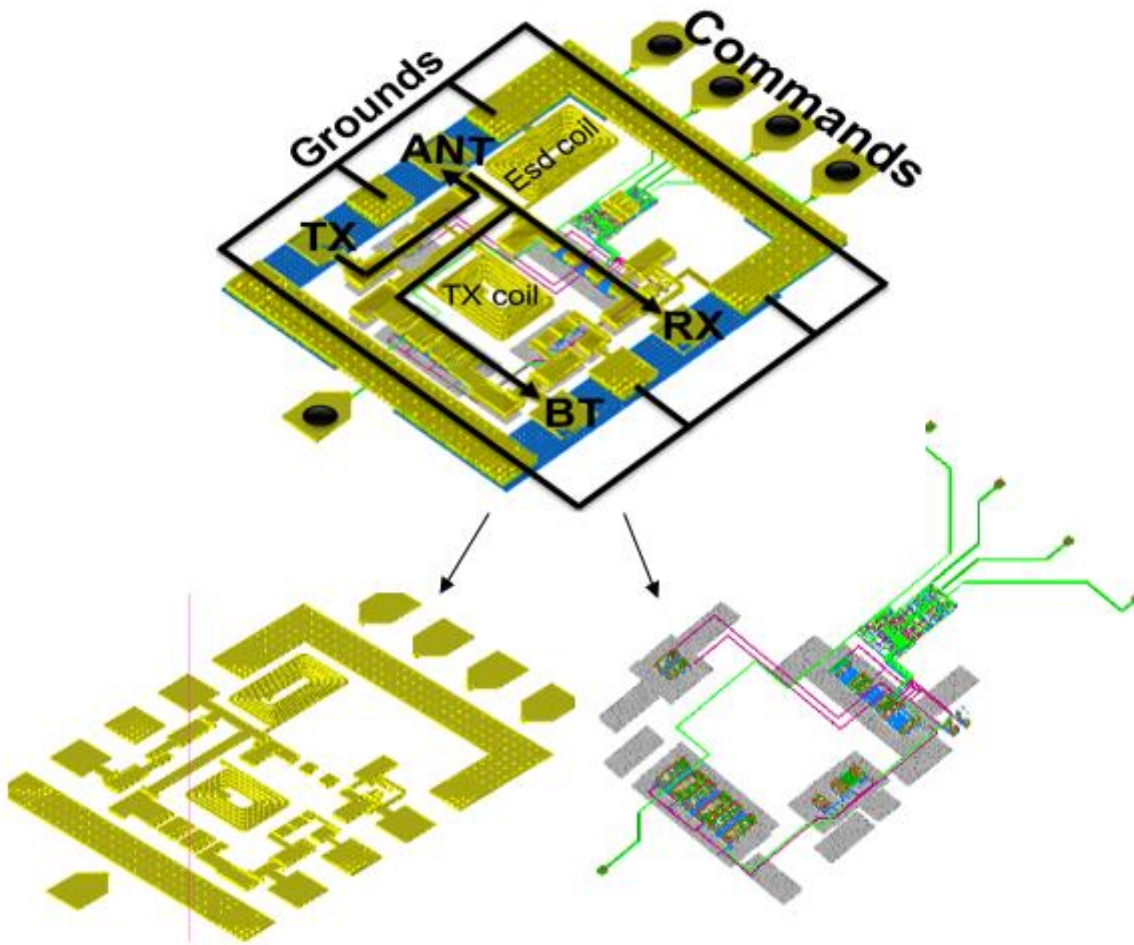


Figure V.18. Configuration of SP3T switch fragmented into 2 main sub-block based on strategy II: (a) Interaction of passives elements (b) and Backend parasitic extraction with related substrate effect

From the described partitioning strategies (Layout based extraction (strategy I) and Full wave simulation (strategy II)). A significant improvement in the flow usability is achieved using the based layout extraction. Indeed, for physical verification DRC (Design Rule Check) and LVS (Layout Vs Schematic) are much easier because of the simplicity of the partitioned database.

### V.1.5. Correlation with FEM Analysis and Measurements

In order to evaluate the accuracy of the proposed technique, the SP3T switch with DTI mesh option is examined. Table V.5 represents a comparison between measurement results, the previous model based on 3D substrate modelling (FEM), and the proposed model in this study. This offers a good accuracy with less than 0.06 dB for the insertion losses (Figure V.19) over the band together with lower computation time.



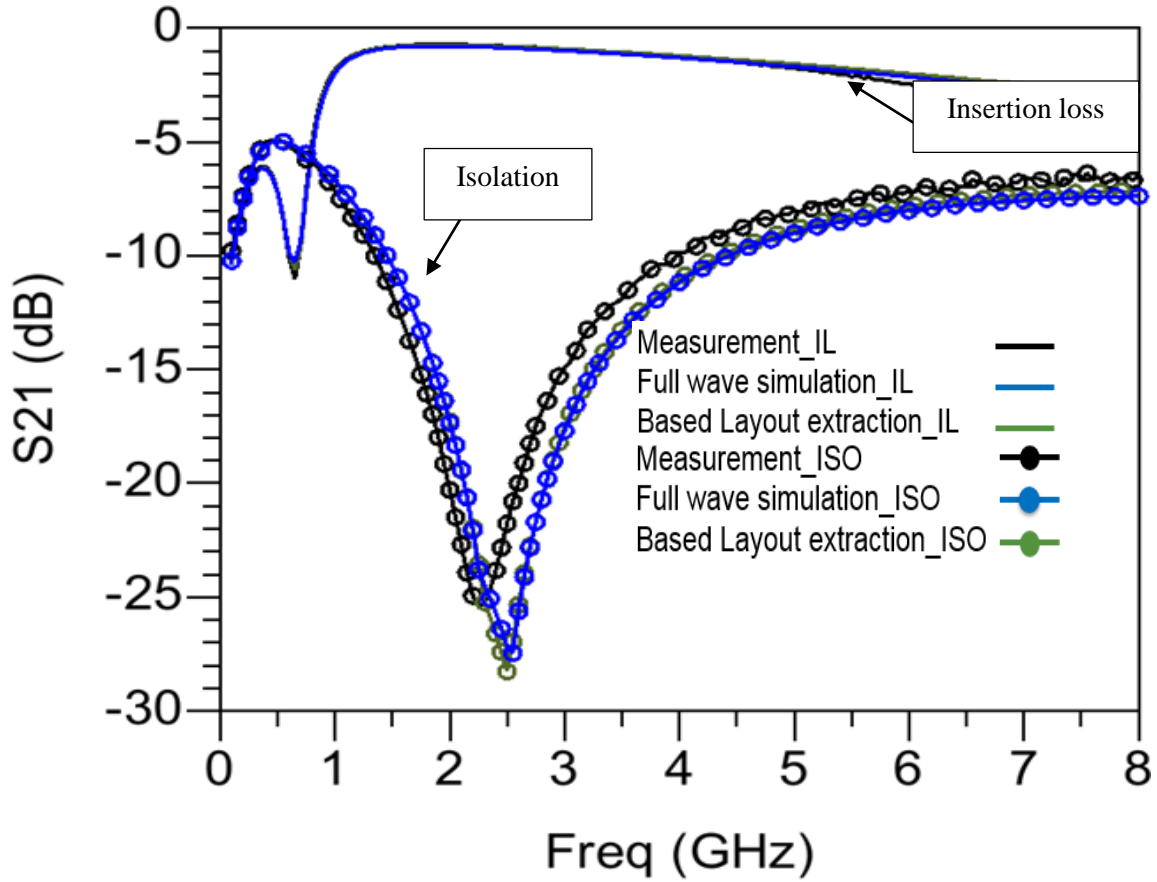


Figure V.19. Insertion loss and isolation of the transmitter: Measurement vs proposed model using both strategies: full wave simulation and based layout extraction

Table V.5. Comparison between measurements, 3D model and proposal model of TX mode

| @ 2.4GHz       | IL (dB) | ISO (dB) | S11(dB) | S22(dB) | CPU time   |
|----------------|---------|----------|---------|---------|------------|
| Measurements   | 0.8     | 23.5     | 13      | 13      |            |
| 3D model       | 0.8     | 26.6     | 13      | 13      | 3h         |
| Proposed model | 0.85    | 25.6     | 13      | 13      | 30 minutes |

The curves in Figure V.20 illustrate SP3T switch performances using DTI mesh option. The proposed model based on layout extraction shows good agreement with 3D (Finite Element Method) model obtained with full wave simulation and with measurement results.

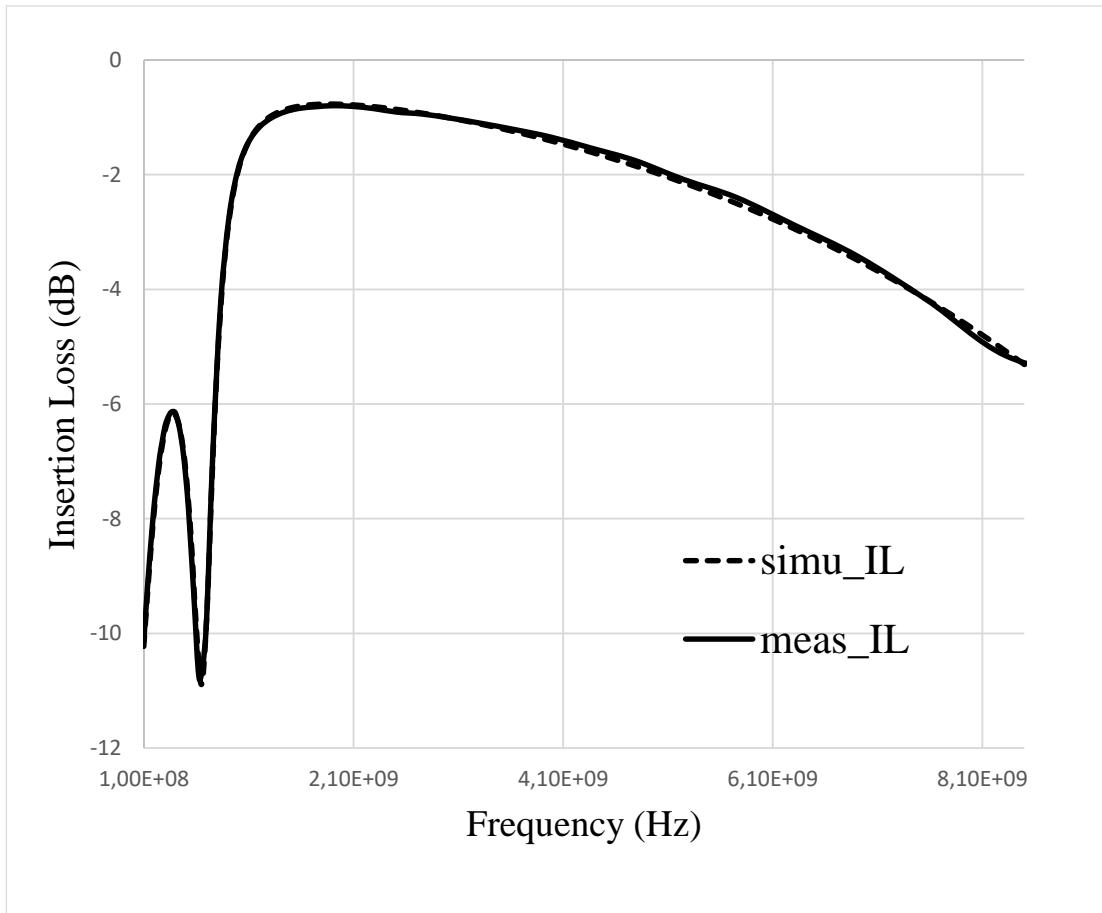


Figure V.20. Insertion loss of the transmitter: Measurement vs proposed model using DTI mesh option

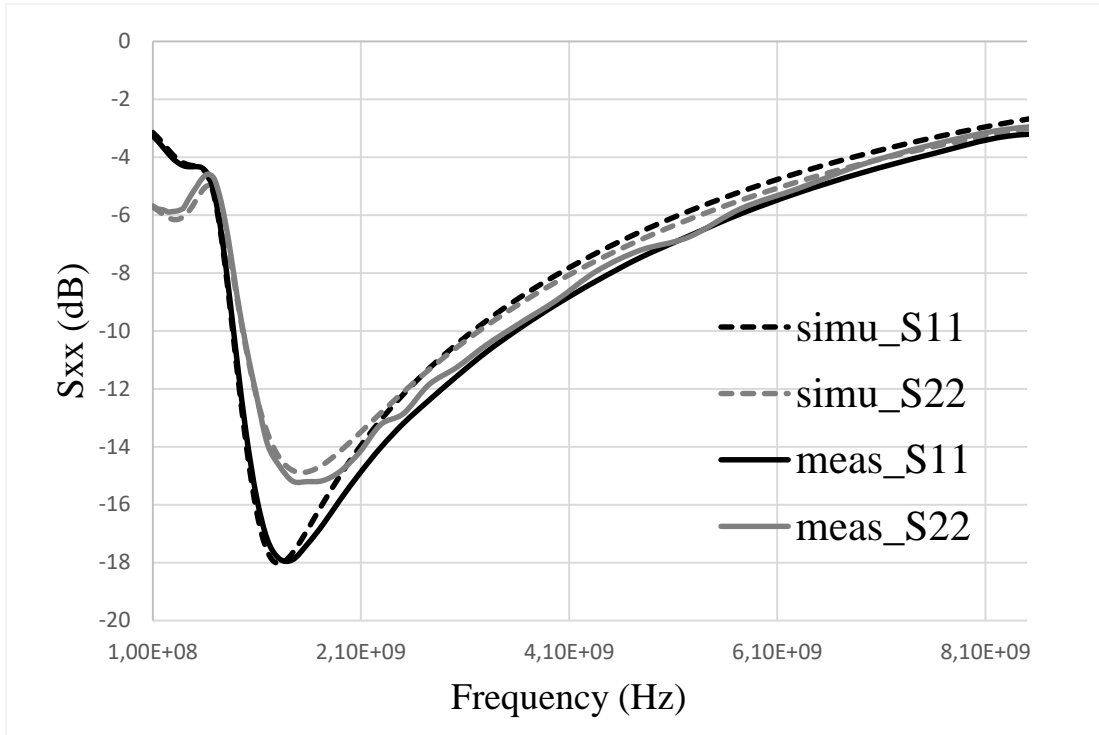


Figure V.21. Input and output return losses of the transmitter; Measurement vs proposed model using DTI mesh option

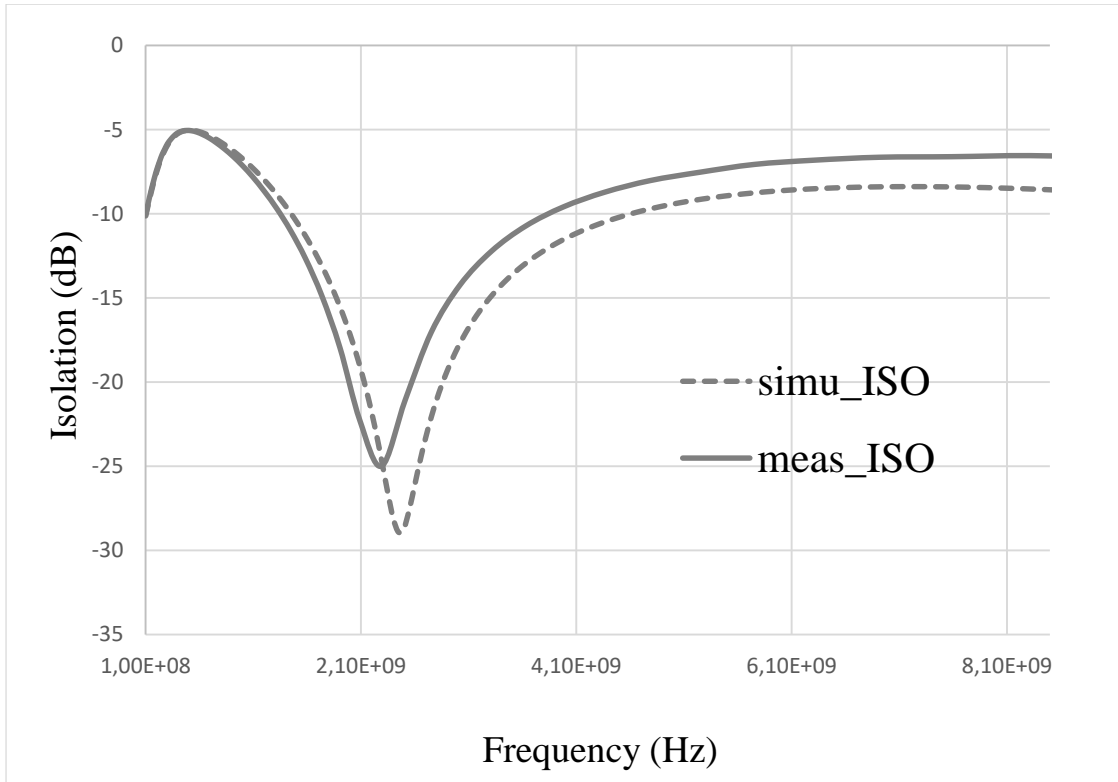


Figure V. 22. Isolation of the transmitter: Measurement vs proposed model using DTI mesh option

In order to validate the proposed methodology, the SP3T switch performances in function of DTI number of rings has been analysed. The table V.6 compares insertion losses of TX mode with isolation of RX and BT modes. The substrate RC network including the DTI capacitance effect is accurately captured.

Promising modelling is achieved. Based on available data, an average difference of 0.06 dB is observed between simulation and measurements for insertion loss. Isolation together with input and output and output return losses are also well predicted by the proposed methodology (whatever the layout variant considered).

Table V.6. Comparison between Simulation and Measurements of SP3T Switch Performances in Function of Number of rings

| @ 2.4 GHz         | 1 ring      |             | 3rings      |             |
|-------------------|-------------|-------------|-------------|-------------|
|                   | measurement | simulation  | Measurement | simulation  |
| <b>IL_TX (dB)</b> | <b>0.86</b> | <b>0.93</b> | <b>0.79</b> | <b>0.84</b> |
| <b>IRL_TX(dB)</b> | <b>12</b>   | <b>12</b>   | <b>13</b>   | <b>13</b>   |
| <b>ISO_RX(dB)</b> | <b>23</b>   | <b>24</b>   | <b>23</b>   | <b>24</b>   |
| <b>ISO_BT(dB)</b> | <b>45</b>   | <b>44</b>   | <b>43</b>   | <b>43</b>   |

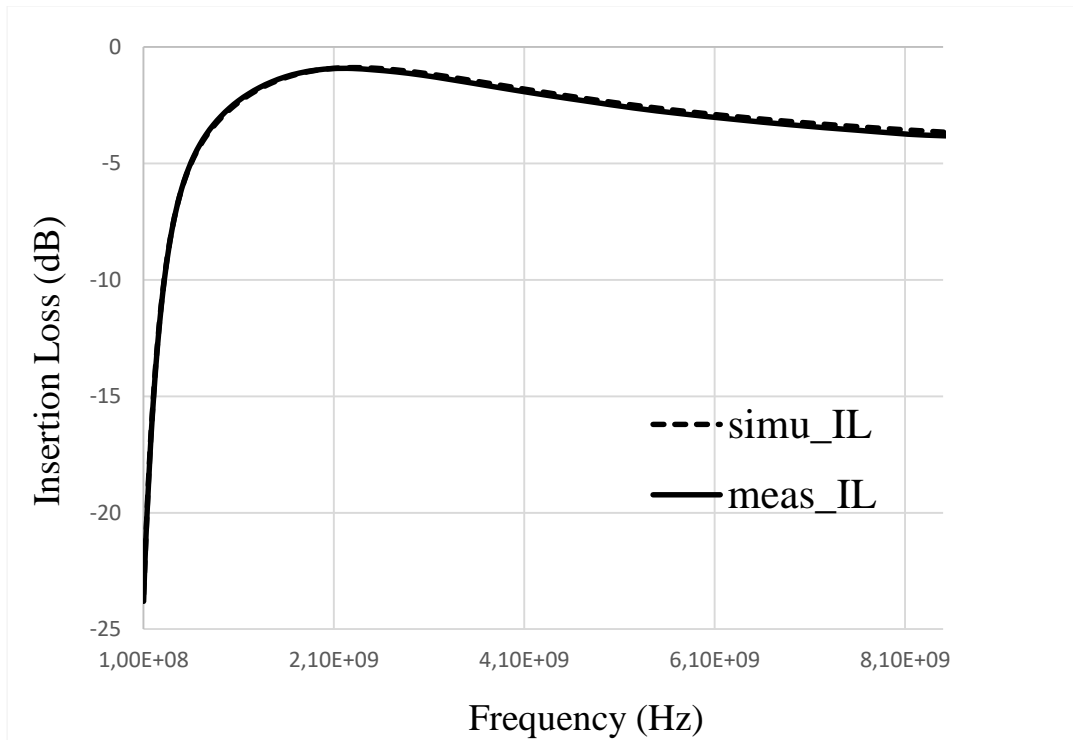


Figure V. 23. Insertion Loss of Bluetooth mode: Measurement vs proposed model using DTI mesh option

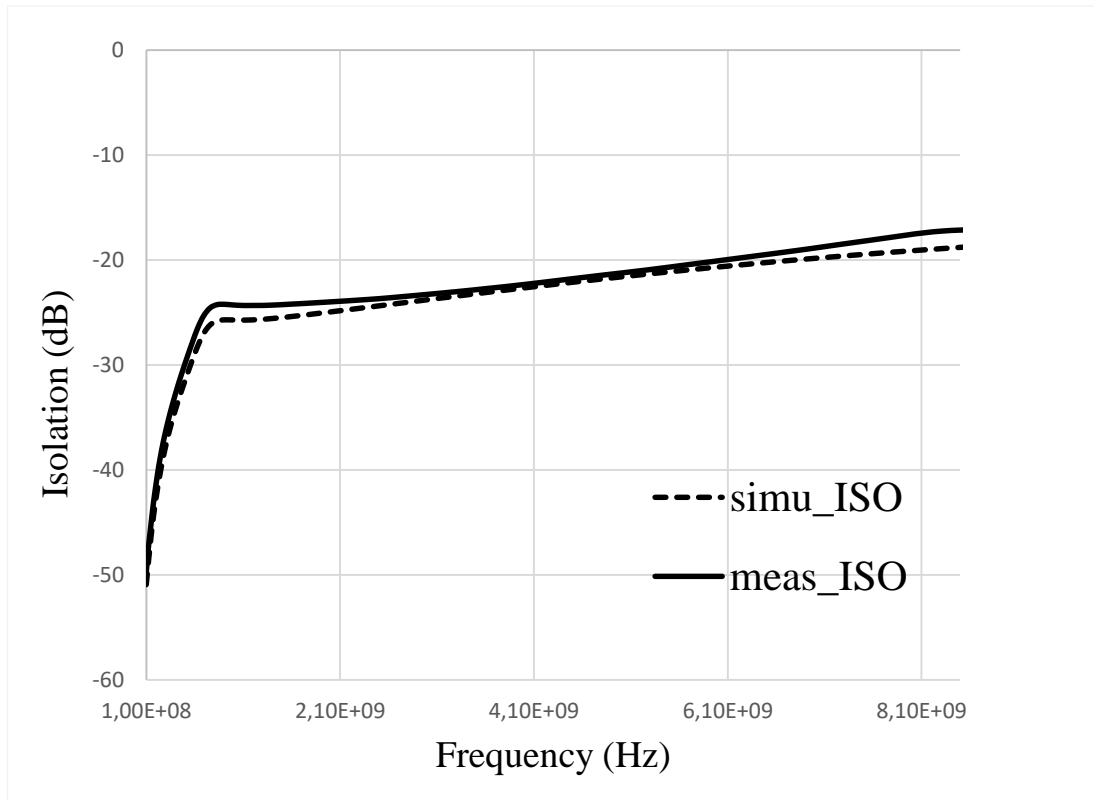


Figure V.24. Measurement vs proposed model using DTI mesh option: Isolation

The measured insertion loss between the Antenna port and Bluetooth port is 0.9 dB at 2.4 GHz, while between the Transmit port and the Antenna is 0.79dB. The return loss is about 18 dB in both cases. Thus, the higher insertion loss for the Bluetooth throw can be attributed to the extra series transistor in the Bluetooth path. Indeed, they are three nMOS switches stacked in BT path versus one nMOS in the TX paths.

## Conclusions

This chapter presents the influence of Deep Trench Isolation on SPDT switch performance. Impact of the number of rings in substrate coupling has been evaluated and discussed. It has been observed that the use of Deep Trench Isolation using ring configurations is clearly efficient to tackle substrate coupling related issues. It shows as good or better results than DTI mesh for which mechanical stress can be an issue.

Next a predictable and accurate methodology to simplify the modelling/simulation phase has been investigated. The proposed methodology offers a trade-off between accuracy and ease of use, as well as being well integrated into a standard design flow. The simulation results demonstrate a satisfactory correlation with measurements results for all the test structures evaluated. This methodology can thus serve as a reference to study new strategies of isolation and can help saving a huge amount of time during layout optimization.

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## General conclusions

This thesis focuses on one hand on the substrate loss optimization in RF switch IC design done in the 0.25 $\mu$ m BiCMOS SiGe NXP process for cellular/WLAN applications, and on the other hand on the development of an efficient methodology for parasitic extraction of inhomogeneous substrates offering a challenging trade-off between required accuracy and fast simulation.

One of the major limitations to achieve the required performance in RF front-end IC's is strongly linked to substrate coupling, due to the lossy nature of silicon.

This thesis is devoted to both a deeper physical understanding of the different coupling mechanisms in the silicon substrate, as well as to the development of substrate effect reduction techniques, as it is important to define simple and fast simulation approaches to handle the substrate coupling effects in a complex circuit.

The main contributions of this thesis are summarized as follows:

❖ **Investigate on the optimum isolation strategy to improve circuit performances:**

- The role of Deep Trench Isolation on nMOS switch performance with different layout variants. Some design (layout point of view) recommendations at device level were also presented to demystify the use of DTI (trade-off between substrate coupling reduction and footprint)
- The impact of DTI and Buried layer on passive elements for substrate coupling reduction.
- Analysis of the influence of DTI on the performance of RF switches.

It has been observed that the use of Deep Trench Isolation with rings is very efficient to tackle substrate coupling related issues.

Combination of DTI with layout topological optimization in passive elements has demonstrated high Q-factors. Removing the buried-p layer underneath the device reduces the parallel resistive losses, and exhibits a similar performance as the DTI mesh for which mechanical stress can be an issue.

❖ **Developing a predictable modelling methodology to reduce time to market:**

A predictable and an accurate methodology to simplify the modelling/simulation phase has been investigated.

- Flow integration: the proposed methodology is fully integrated in the design flow and easy to use.
- The accuracy of the proposed methodology was first verified on a single test case in comparison with RF measurements and full-wave simulations.

- Apply the proposed methodology to a full SPDT switch for LTE applications, then apply it to an SP3T switch for WLAN applications: the required parameters, mainly noise figure, losses, and isolation, must be compliant with requirement specifications.
- Both the impact of substrate thickness and the substrate bias on switch performance have been investigated using the proposed methodology and validated using RF silicon measurements.

This methodology focuses on the extraction tool to tackle the coupling between different active devices which can also jeopardize circuit performance. This is typically a domain in which a compact model is not sufficiently accurate as it does not take into account the layout environment of the device. Most of the time modelling techniques rely on complex techniques such as FEM analysis. But FEM analysis is very time consuming and requires most of the time a considerable expertise.

The simulation results obtained from the proposed methodology in this thesis demonstrate a satisfactory correlation with measurement results for all the test structures evaluated in this thesis.

## Perspectives

This thesis gives rise to some perspectives in short and long term:

- The impact of substrate effects of ESD protection components on the linearity of the switch is under investigation. RF Measurements will be performed for comparison purposes. This study will concern the SPDT switch for the LTE band and the SP3T input LNA for WLAN applications. The obtained results will be presented in the thesis defence.
- We also planned to perform Noise Figure measurements of the RF switch. This work will also be presented in the thesis defence.
- Extension of the proposed methodology to 5G applications
- Developing a low loss, high isolation and high linearity wideband RF switch for 5G applications.
- Extension of the proposed methodology to SOI technology for 5G applications.

## Annex

### Validate PDK (Process Design Kit) Backend stack against silicon:

The objective is to validate the correctness of backend stack modelling for PEX (Parasitic Extraction) tool against silicon measurements.

The foundry translates electrical measurements on backend\*-stack to geometrical dimensions present in the Design Rule Manual (DRM). Then, the PDK team uses these geometrical dimensions to model the back-end stack for the supported PEX tool.

Closing the loop will validate the correctness and the correlation of the modelled stack against silicon measurements. The accuracy of a backend stack is correct when:

- The sheet resistance of all metal layers and vias extracted by the PEX-tool correlate well with measurements data.
- The plate and coupling capacitances extracted by the PEX-tool correlates with silicon measurements.

#### ➤ Sheet Resistance:

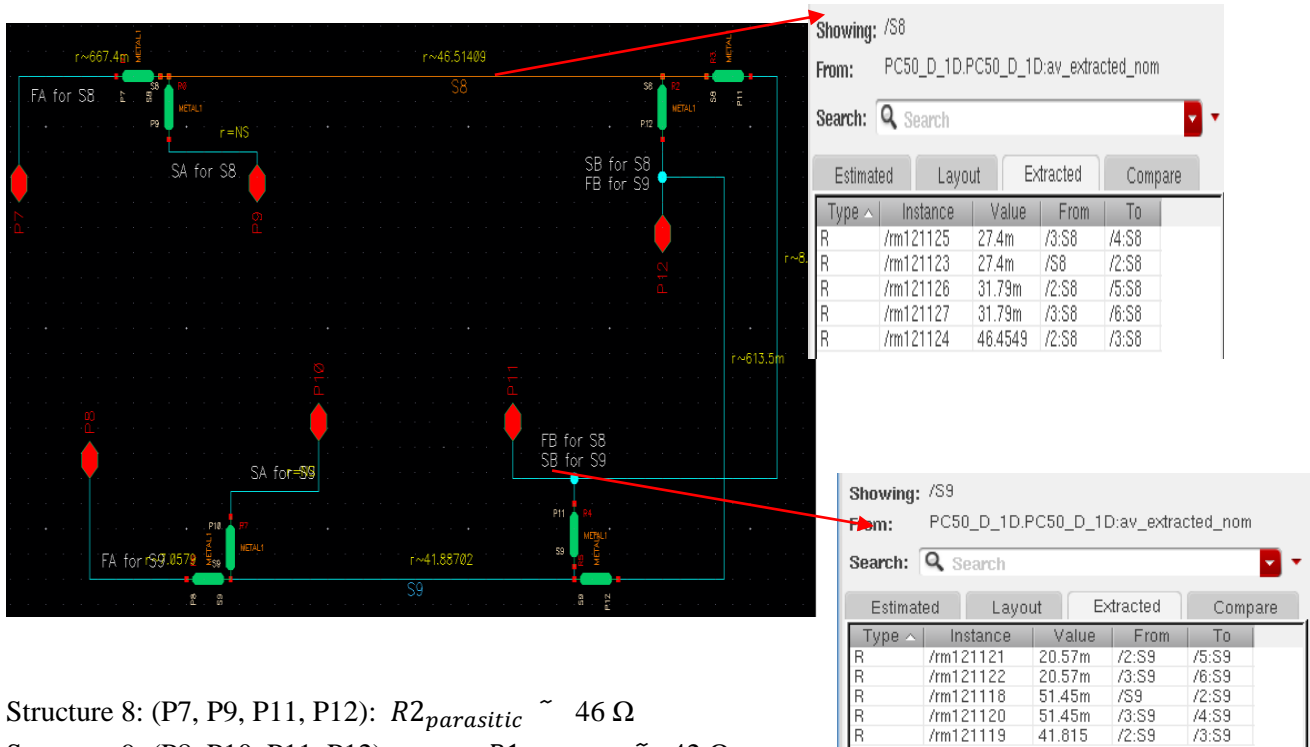
The  $R_{\square}$  of Metal1 is evaluated as illustrated below. The corresponding PCM (Process Control Module) structures were defined in collaboration with the process team.

Two geometries are considered:

| # | contents                              | dimensions                  |
|---|---------------------------------------|-----------------------------|
| 1 | diode p+ ACTIVE to NWELL              | ACTIVE W×L = 79.1×83.6      |
| 2 | METAL3 isolation on topo              | METAL3 teeth per comb = 41  |
| 3 | chain METAL1 to p+ unsilicided ACTIVE | #CONTACT = 39×2×31×2 = 4836 |
| 4 | chain METAL6 to MIM                   | #VIA5 = 10×15+8 = 158       |
| - |                                       |                             |
| - |                                       |                             |
| - |                                       |                             |
| 8 | res METAL1                            | L/W = 871.0/0.8 = 1088.75   |
| 9 | res METAL1                            | L/W = 435.5/0.4 = 1088.75   |

Table.1. M1 structure considered for closing the loop

Resistances extraction and test bench: After Layout extraction, below the test bench is showing the of structure 8 (R2) and structure 9 (R1)



Structure 8: (P7, P9, P11, P12):  $R_{2_{parasitic}} \sim 46 \Omega$

Structure 9: (P8, P10, P11, P12):  $R_{1_{parasitic}} \sim 42 \Omega$

| Structure ID  | Dimensions<br>L/W (um) | extraction corners |           |           |
|---------------|------------------------|--------------------|-----------|-----------|
|               |                        | $R_{nom}$          | $R_{min}$ | $R_{max}$ |
| EAL00060 (R2) | 871/0,8= 1088,75       | 46,51409           | 29,38204  | 64,3934   |
| EAL00061 (R1) | 435,5/0,4=1088,75      | 41,88702           | 23,12798  | 64,43168  |

Table.2. Extracted resistance in different corners

**Parasitic extraction Vs PCM measurement Data:**

| Data file     | Variable | Obs    | Mean     | Std. Dev. | Min    | Max    | parameter name     |
|---------------|----------|--------|----------|-----------|--------|--------|--------------------|
| PQ050PFC_2014 | EAL00060 | 680    | 46.87145 | 1.216283  | 42.996 | 50.479 | R_M1_871/0.8_R4p   |
| PQ050PFH_2014 | EAL00060 | 2004   | 45.70528 | 1.778762  | 41.673 | 51.081 | R_M1_871/0.8_R4p   |
| PQ050PFL_2014 | EAL00060 | 10353  | 47.60458 | 1.459665  | 44.021 | 54.408 | R_M1_871/0.8_R4p   |
| PQ050PFT_2014 | EAL00060 | 54540  | 44.70679 | 1.473302  | 39.861 | 52.138 | R_M1_871/0.8_R4p   |
| PQ050WAA_2014 | EWL24040 | 440    | 45.12322 | 1.315415  | 42.02  | 49.088 | R_M1_871/0.8_R4p   |
| PQ050W_2014   | EWL24040 | 1190   | 43.2561  | 1.173684  | 40.373 | 48.211 | R_M1_871/0.8_R4p   |
| PQ050XI_2014  | EAL00060 | R2 460 | 44.89743 | 1.347873  | 42.15  | 49.545 | R_M1_871/0.8_R4p   |
| PQ050X_2014   | EAL00060 | 2178   | 46.39529 | 1.239178  | 40.78  | 52.002 | R_M1_871/0.8_R4p   |
| PQ050PFC_2014 | EAL00061 | 680    | 41.6695  | 1.480726  | 37.763 | 46.352 | R_M1_435.5/0.4_R4p |
| PQ050PFH_2014 | EAL00061 | 2004   | 41.18315 | 2.781579  | 35.478 | 50.278 | R_M1_435.5/0.4_R4p |
| PQ050PFL_2014 | EAL00061 | 10354  | 44.6707  | 2.140718  | 39.958 | 54.109 | R_M1_435.5/0.4_R4p |
| PQ050PFT_2014 | EAL00061 | 54541  | 39.8802  | 1.931056  | 33.942 | 51.948 | R_M1_435.5/0.4_R4p |
| PQ050WAA_2014 | EWL24041 | 440    | 40.4217  | 1.595843  | 37.062 | 44.807 | R_M1_435.5/0.4_R4p |
| PQ050W_2014   | EWL24041 | 1190   | 38.35718 | 1.356694  | 34.978 | 43.925 | R_M1_435.5/0.4_R4p |
| PQ050XI_2014  | EAL00061 | R1 460 | 40.52926 | 2.170182  | 36.475 | 48.758 | R_M1_435.5/0.4_R4p |
| PQ050X_2014   | EAL00061 | 2178   | 43.28727 | 1.904453  | 37.292 | 50.076 | R_M1_435.5/0.4_R4p |

Table.3. PCM measurement data of M1 sheet resistance (S8 and S9)

$$\Delta\sigma = \frac{R2(meas) - R2(QRC)}{std.dev} = 1,2$$

$$\Delta\sigma = \frac{R1(meas) - R1(QRC)}{std.dev} = 0,62$$

The same manner is applied to the other metal layer for layer stack validation.

➤ **Plate capacitors:**

The second parameter to be validated is the vertical capacitance. The same steps have been followed: Collaboration with process team to get the corresponding PCM data, then extraction and finally comparison with measurements data and hand calculation.

$$C(F) = \frac{Area * \epsilon_0 \epsilon_r}{thickness\ of\ the\ dielectric} \Rightarrow C(aF/um^2) = \frac{C(F)}{Area(um^2)}$$

The worst and the best capacitances are not statistical values, they are related to the upper- and lower spec limits (LSL and USL) of the process.

Below a correlation between PCM data (630 samples) and extracted plate capacitor between Metal1 and metal2 is shown:

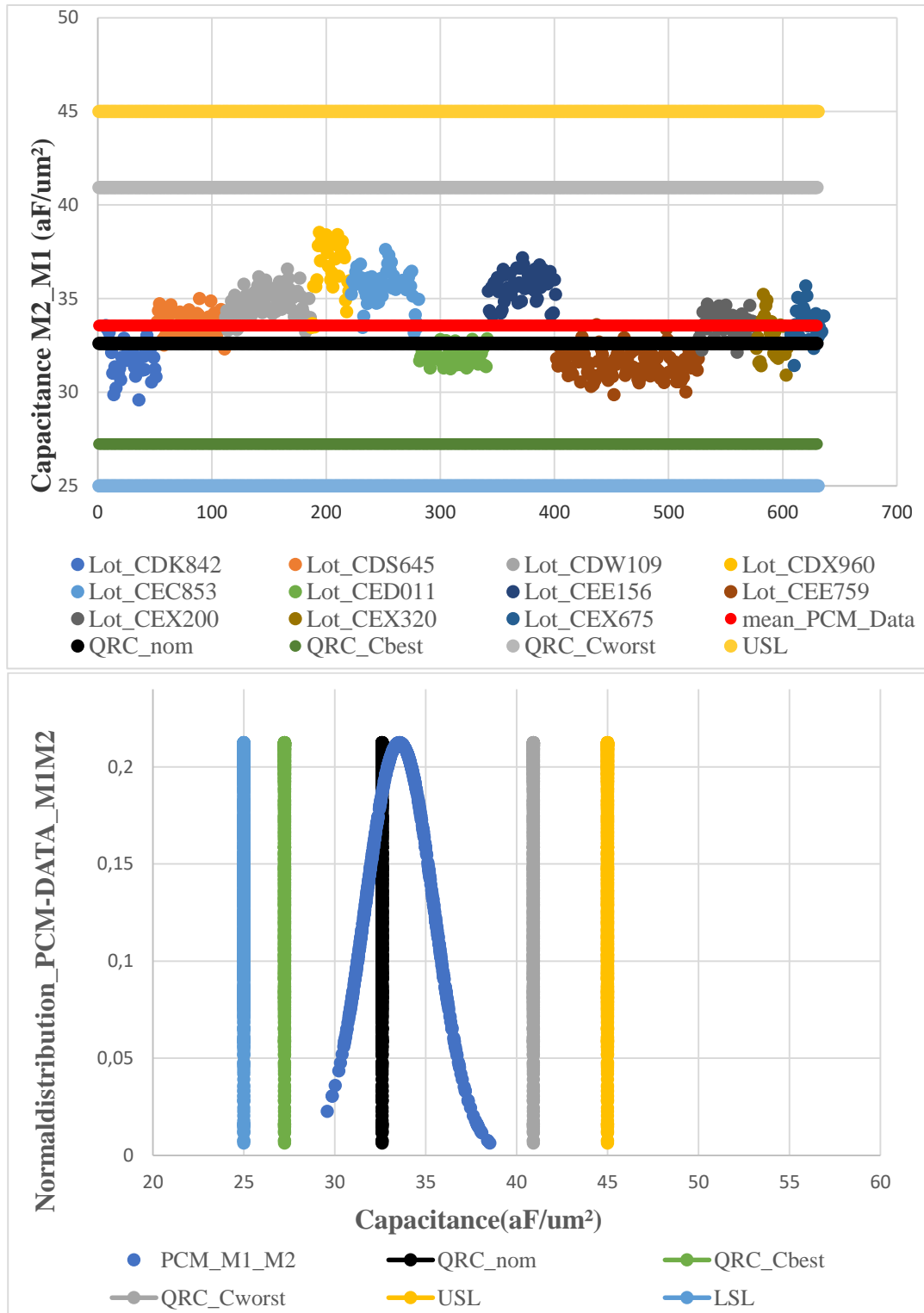


Figure.1 measurement data of 630 sample vs extracted corners (nominal, Cbest and Cworst)

$$\frac{\Delta_{nom}}{std.dev} = \frac{C_{mean(meas)} - C_{nom}(QRC)}{std.dev} = \frac{33.56 - 32.60}{1.87} = 0,51$$

$$\frac{\Delta_{\text{best}}}{\text{std.dev}} = \frac{\Delta_{\text{best}}}{\text{std.dev}} = \frac{C_{\text{best}}(\text{QRC}) - C_{\text{LSL}}(\text{meas})}{\text{std.dev}} = \frac{27,23 - 25}{1,87} = 1,2$$

$$\frac{\Delta_{\text{Worst}}}{\text{std.dev}} = \frac{C_{\text{USL}}(\text{meas}) - C_{\text{Worst}}(\text{QRC})}{\text{std.dev}} = \frac{45 - 41}{1,87} = 2,13$$

The validation was done for all plate capacitors up to metal 6. The table below represents the comparison for all metal layers.

| Cap/area<br>[aF/<br>um <sup>2</sup> um <sup>2</sup> ] | Calculated<br>nom | PEX<br>nom | PCM<br>mean | PEX<br>Cbest | PCM<br>LSL | PEX<br>Cworst | PCM<br>USL |
|---|-------------------|------------|-------------|--------------|------------|---------------|------------|
| Poly_(N+)   | 95,67             | 96,74      | 95.74805    | 85,303       | 65         | 111,72        | 125        |
| M1_to_Poly  | 57,19             | 57,45      | 52.69902    | 47,1807      | 42         | 73,91         | 65         |
| M2_to_M1  | 32,29             | 32,60      | 33.56036    | 27,2365      | 25         | 40,9271       | 45         |
| M3_to_M2  | 32,30             | 32,65      | 33.71042    | 27,2649      | 25         | 40,9838       | 45         |
| M5_to_M3  | 32,30             | 32,69      | 36.50669    | 27,3247      | 26         | 41,0951       | 49         |
| M6_to_M5  | 20,64             | 21,17      | 22.22109    | 17,6255      | 17         | 26,4678       | 29         |

Table.4. Comparison between Extraction (PEX), PCM data and hand calculation



## Calibration and De-Embedding for RF Measurements

- Calibration Techniques

RF measurements involve a Vector Network Analyzer to evaluate the characteristics of the device under test (DUT) through its S-parameters. Calibration is an essential step in the measurement process that removes the parasitic capacitances, inductances and resistances due to the Network Analyzer, cables, probe station, and probes. Without calibration, the measurements do not provide the correct S-parameters. To compute, determine and remove these unknown error terms from the measurement results, a calibration procedure, called vector error correction, is required using known standards.

Figure.II.18 illustrates the block diagram of the DUT cascaded between two errors boxes.

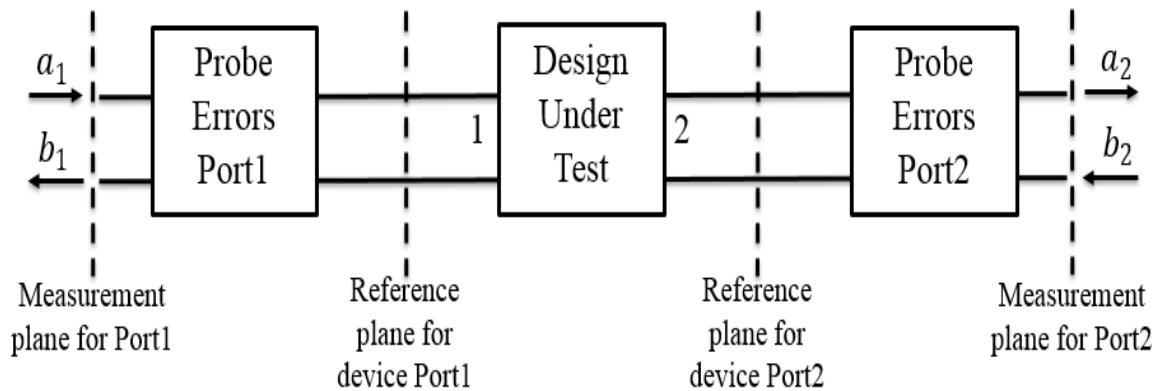


Figure.1. Reference planes for calibration purpose

The T-parameters of the T-matrix are defined as:

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} a_2 \\ b_2 \end{bmatrix}$$

The procedure consists of finding the S-parameters or the T-parameters of the error Port 1/2 matrices of figure.II.18 through the measurements of standards.

As the T-parameters of the un-calibrated device can be written as:

$$T_{meas} = T_1 T_{DUT} T_2$$

where  $T_{meas}$  represents the total T-matrix measured,  $T_{DUT}$  the actual T-matrix of the DUT.  $T_1$  and  $T_2$  are the virtual error T-matrices. Once the T-parameters of the virtual error matrices are determined, the next step of the calibration consists of removing the error matrices as:

$$T_{DUT} = T_1^{-1} T_{meas} T_2^{-1}$$

The calibration method allows moving the reference plane at the end of the probe tips. This calibration uses standards made on a substrate. These standards are certified, and allow measurements up to 50GHz and 110GHz depending on the VNA and probe tips used. The most common calibration methods that allow the correction are:

- SOLT (Short-Open-Load-Thru) [II-7]
- TRL (Thru-Reflect-Line) [II-8]
- LRM (Line-Reflect-Load) [II-9]
- LRMM (Line-Reflect-Reflect-Match) [II-10].

In our study, on-wafer LRMM/SOLT calibration methods are used. The calibration standards are made on alumina substrate (ISS Impedance Substrate Standard).

**SOLT (Short-Open-Load-Thru):** The SOLT calibration is the most commonly used calibration technique. It utilizes three impedances and one transmission standard to define the calibrated reference plane. These standards, a Short, an Open, Load and a Thru make up the SOLT calibration kit. The SOLT calibration method is shown in figure.II.19

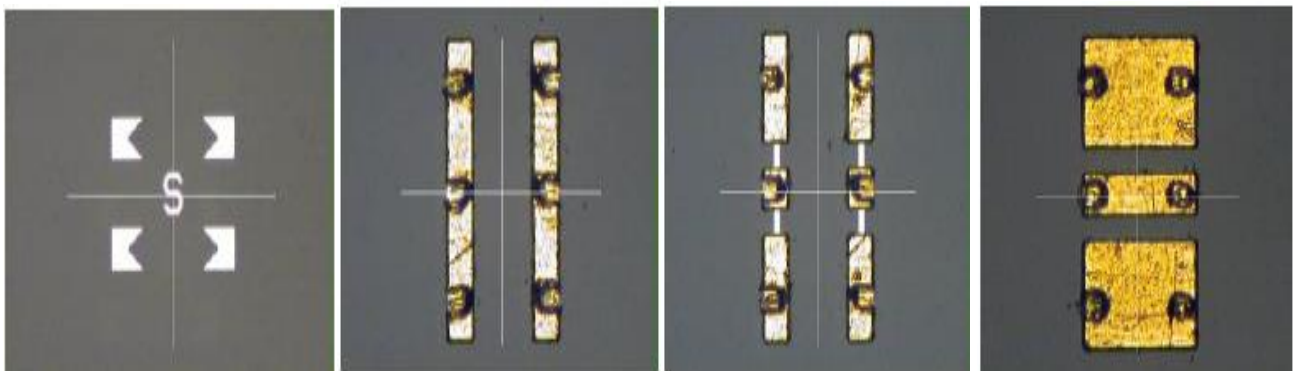


Figure 2: Layout of calibration standard for SOLT calibration: Open (a), Short (b) Load (c), and Thru (d)

This method of calibration [II-7] considers standards as ideal:

- The short circuit reflects all the energy received by inverting the phase,
- The open circuit reflects all the energy received without modifying the phase,
- The load absorbs all the energy received,
- The line transmits all the energy.

Thus, we obtain the matrices of parameters S and T following (see equations below)

- De-embedding technique

Once the calibration has been carried out, so that all the interference introduced by the analyzer and the cables are included in the error terms seen previously.

To return the reference plane to the intrinsic component, the interference brought by the pads and the interconnection lines must be eliminated. For this, we use a correction technique called de-embedding after the component measurement.

This technique consists to subtract parasitic of interconnections between measurement probes and DUT (Design Under Test).

In order to get the DUT response from measurements, the parasitic must be removed. For that, the dummy patterns are fabricated on the same wafer and should be carefully designed to reproduce and subtract the extrinsic parasitic of a fixture device.

**The Open-Short De-embedding method:** De-embedding technique allows to remove the parasitic of the probe pads and metallization from the measured S-parameters in order to extract the intrinsic device behavior.

Several de-embedding techniques have been described in the literature [II-12] [II-13] [II-14]. In the Open-Short defined by Koolen et al [II-11] where the interconnections lead to 2 main contributions:

- Parallel (capacitive => PI circuit), determination of  $Y_1$ ,  $Y_2$ , and  $Y_3$  using an Open dummy
- Series (inductive and resistive =>T circuit), determination  $Z_1$ ,  $Z_2$ , and  $Z_3$  using a Short dummy

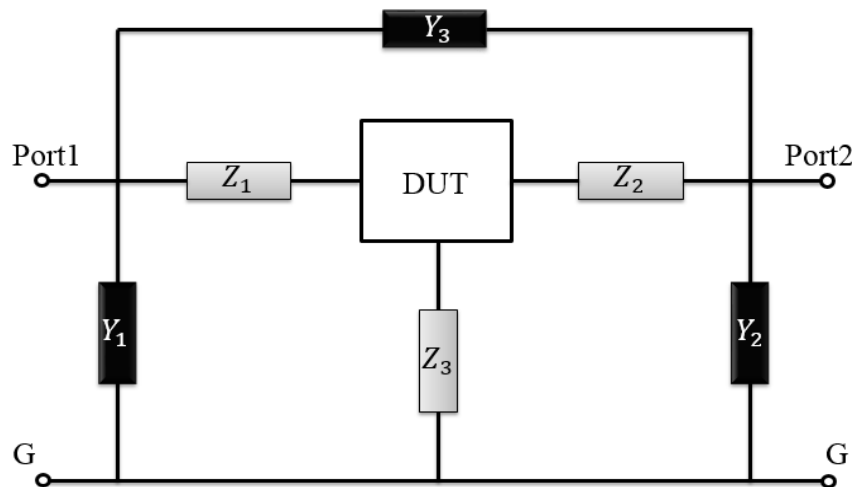


Figure 3. Equivalent circuit with parasitic admittances and impedances

The DUT own Y-parameters are then obtained from the open and short structure, respectively as follows:

$$Y_{OpenShort} = ((Y_{DUT} - Y_{Open})^{-1} - (Y_{DUT} - Y_{Open})^{-1})^{-1}$$

$Y_{\text{open}}$  denotes the two-port admittance parameters measured on the “open” dummy structure.  
 $Y_{\text{short}}$  denotes the two-port impedance parameters measured on the “short” dummy structure.