3D integration of single electron transistors in the back-end-of-line of 28 nm CMOS technology for the development of ultra-low power sensors

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N°d'ordre NNT : 2016LYSEI155

THÈSE de DOCTORAT DE L'UNIVERSITÉ DE LYON
opérée au sein de
Institut National des Sciences Appliquées de Lyon
et délivré en partenariat international avec
Université de Sherbrooke

École Doctorale N° :EDA160
École Doctorale Électronique, Électrotechnique, Automatique de Lyon

Spécialité de doctorat : Électronique, micro et nanoélectronique, optique et laser

Soutenue publiquement le 16/12/2016, par :
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3D INTEGRATION OF SINGLE ELECTRON TRANSISTORS IN THE BACK-END-OF-LINE OF 28 nm CMOS TECHNOLOGY FOR THE DEVELOPMENT OF ULTRA-LOW POWER SENSORS

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Dedicated to my parents

Acknowledgments

First, I would like to express my deepest sense of gratitude to my supervisors Prof. Dominique Drouin and Prof. Abdelkader Souifi for providing me the opportunity to undertake such exciting and challenging Ph.D. research project in such a fascinating field of nanoelectronics. My deepest thanks also go to associate Prof. Serge Ecoffey for supervising the research project work. I am grateful to all of them for the encouragement, support, guidance, advices, and enriching discussions. I owe to them all I have learned throughout this "adventure". A Special thanks to my supervisor Prof. Dominique Drouin for believing in me and giving me the chance to go further in my research project.

I would like to thank all the nanoelectronics research group members for the support, the collaborative and constructive work, being helpful and providing a lovely and friendly ambiance, which made it more convenient to carry out the research project. In particular, Bruno Lee Sang and Gabriel Droulers for all the help rendered in various ways and the enriching discussions. I acknowledge the help from Jean-Philippe Richard, Fréderic Bourque and Marc Guilmain. A special thanks to Pascal Lemieux for helping with the development of the FD-SOI FET simulator. His amazing skills in programming and keen interest account for a big part of the developed simulator.

I am grateful to all the collaborators and project partners, Jean-Pierre Cloarec, Stéphane Monfray, Adranik Sarkissian, Andreas Rudiger, Bertrand Vilquin and Jonathan Genest who generously shared their insights and expertize. Their valuable and meticulous criticism and suggestions were very helpful and constructive, and account for a big part of the achieved work.

I would like to thank the entire 3IT-LNN, 3IT-LCSM and IMDQ technical and research staff for their support and being always ready to give a hand, in particular Pierre Langlois, Marie-José Gour, Étienne Paradis, Carolyn Roy, Denis Pellé, Daniel Blackburn, René Labrecque, Christian Sara-Bournet and Michael Lacerte for their tremendous help, favours and moral support.

I would like to thank all the INL members for the great time spent with them. A special thanks to Annie Suslec, Yvan Doyeux, Nicolas Baboux, Lama Rahal, Francis Calmon Daniel Barbier,

Brice Gautier and Christian Gontrand for their kindness, all kinds of support, the coffee breaks, and the very special discussions and jokes!

I would like to thank all the 3IT members, for taking part of this project and all the moments shared together. A special thanks to Osvaldo Arenas and Martine Parent for the moral support, and Arnaud Samson for the help with LabView programming.

I am so grateful to La Fondation Force for the support and making this project go to his end.

I owe everything to my parents who never kept sacrificing and dedicating themselves to my accomplishment so trustworthy and humbly and without any expectation whatever. A mere “thank you” to acknowledge their sacrifice can hardly do justice to the immerse gratitude I feel. I hope my accomplishments can make them proud. Last, I am so grateful to all the people who took part in this “adventure”, inspired me, supported me and fed me with food, compassion and love. I owe to them a LOT. I could not have made it this far without their constant moral support and encouragement. I am grateful to Sylvie Jacques, Hatem Laabidi, Véronique Thibaut, Tina Merz, Frances Alvo, Samuel Paquette, Simon Stankovich, Joanna Bateman, Dany Loubier, Philippe Demers, Dominique Boiverts, Julia Goolia, Geneviève Kiliko, Rafael Soler Hernandez, Maricarmen Soler Hernandez, Matteo Vignetti and Daniel Thomas for all what they have done for me.

Abstract

The need of integration of new functionalities on mobile and autonomous electronic systems has to take into account all the problematic of heterogeneity together with energy consumption and thermal dissipation. In this context, all the sensing or memory components added to the CMOS (Complementary Metal Oxide Semiconductor) processing units have to respect drastic supply energy requirements.

Smart mobile systems already incorporate a large number of embedded sensing components such as accelerometers, temperature sensors and infrared detectors. However, up to now, chemical sensors have not been fully integrated in compact systems on chips. Integration of gas sensors is limited since most used and reliable gas sensors, semiconducting metal oxide resistors and catalytic metal oxide semiconductor- field effect transistors (MOSFETs), are generally operated at high temperatures, 200–500 °C and 140–200° C, respectively.

The suspended gate-field effect transistor (SG-FET)-based gas sensors offer advantages of detecting chemisorbed, as well as physisorbed gas molecules and to operate at room temperature or slightly above it. However they present integration limitations due to the implementation of a suspended gate electrode and augmented channel width in order to overcome poor transconductance due to the very low capacitance across the airgap.

Double gate-transistors are of great interest for FET-based gas sensing since one functionalized gate would be dedicated for capacitively coupling of gas induced charges and the other one is used to bias the transistor, without need of airgap structure. This work discusses the integration of double gate-transistors with CMOS devices for highly sensitive and ultra-low power gas sensing applications.

The use of single electron transistors (SETs) is of great interest for gas sensing applications because of their key properties, which are its ultra-high charge sensitivity and the ultra-low power consumption and dissipation, inherent to the fundamental of their operation based on the transport of a reduced number of charges.

Therefore, the work presented in this thesis is focused on the proof of concept of 3D monolithic integration of SETs on CMOS technology for high sensitivity and ultra-low power gas sensing functionality. The proposed approach is to integrate metallic double gate-single electron

transistors (DG-SETs) in the Back-End-Of-Line (BEOL) of CMOS circuits (within the CMOS interconnect layers) using the *nanodamascene* process. We take advantage of the hyper sensitivity of the SET to electric charges as well from CMOS circuits for high-speed signal processing.

Fully depleted-silicon on insulator (FD-SOI) MOSFETs are very attractive devices for gas sensing due to their amplification capability when operated in the sub-threshold regime which is the strongest asset of these devices with respect to the FET-based gas sensor technology. In addition these devices are of a high interest in terms of integration density due to their small size. Moreover FD-SOI FETs is a mature and well-modelled technology. We focus on the functionalization of the front gate of a FD-SOI MOSFET as a demonstration of the DG-transistor-based gas sensor.

Kelvin probe has been the privileged technique for the investigation of FET-based gas sensors' sensitive material via measuring the work function variation induced by gas species adsorption. In this work an alternative technique to investigate gas sensitivity of materials suitable for implementation in DG-FET-based gas sensors, based on measurement of the surface charge induced by gas species adsorption is discussed.

In order to increase the specific surface of the sensing electrode, a novel concept of functionalized gate surface texturing suitable for FET-based gas sensors are presented. It is based on the spray coating of a multi-walled-carbon nanotubes (MW-CNTs) suspension to deposit a MW-CNT porous network as a conducting frame for the sensing material.

The main objective of this Ph.D. thesis can be divided into 4 parts: (1) modelling and simulation of a DG-SET and a FD-SOI MOSFET-based gas sensor response, and estimation of the sensitivity as well as the power consumption; (2) investigation of Pt sensitivity to hydrogen by surface charge measurement technique and development of the sensing electrode surface texturing process with CNT networks; (3) development and optimization of the DG-SET integration process in the BEOL of a CMOS substrate, and (4) FD-SOI MOSFET functionalization with Pt for H_2 sensing.

Keywords: Single electron transistors, 3D monolithic integration, FET-based gas sensors, Gas sensing, Hydrogen detection, Sensing layer texturing, MW-CNT networks, Ultra-low power, FDSOI.

Résumé

La forte demande et le besoin d'intégration hétérogène de nouvelles fonctionnalités dans les systèmes mobiles et autonomes, tels que les mémoires, capteurs, et interfaces de communication doit prendre en compte les problématiques d'hétérogénéité, de consommation d'énergie et de dissipation de chaleur.

Les systèmes mobiles intelligents sont déjà dotés de plusieurs composants de type capteur comme les accéléromètres, les thermomètres et les détecteurs infrarouge. Cependant, jusqu'à aujourd'hui l'intégration de capteurs chimiques dans des systèmes compacts sur puce reste limitée pour des raisons de consommation d'énergie et dissipation de chaleur principalement. La technologie actuelle et fiable des capteurs de gaz, les résistors à base d'oxyde métallique et les MOSFETs (Metal Oxide Semiconductor- Field Effect Transistors) catalytiques sont opérés à de hautes températures de 200–500 °C et 140–200 °C, respectivement.

Les transistors à effet de champ à grille suspendu (SG-FETs pour Suspended Gate-Field Effect Transistors) offrent l'avantage d'être sensibles aux molécules gazeuses adsorbées aussi bien par chemisorption que par physisorption, et sont opérés à température ambiante ou légèrement au-dessus. Cependant l'intégration de ce type de composant est problématique due au besoin d'implémenter une grille suspendue et l'élargissement de la largeur du canal pour compenser la détérioration de la transconductance due à la faible capacité à travers le gap d'air.

Les transistors à double grilles sont d'un grand intérêt pour les applications de détection de gaz, car une des deux grilles est fonctionnalisée et permet de coupler capacitivement au canal les charges induites par l'adsorption des molécules gazeuses cibles, et l'autre grille est utilisée pour le contrôle du point d'opération du transistor sans avoir besoin d'une structure suspendue.

Les transistors monoélectroniques (les SETs pour Single Electron Transistors) présentent une solution très prometteuse grâce à leur faible puissance liée à leur principe de fonctionnement basé sur le transport d'un nombre réduit d'électrons et leur faible niveau de courant.

Le travail présenté dans cette thèse fut donc concentré sur la démonstration de l'intégration 3D monolithique de SETs sur un substrat de technologie CMOS (Complementary Metal Oxide Semiconductor) pour la réalisation de la fonction capteurs de gaz très sensible et ultra basse consommation d'énergie. L'approche proposée consiste à l'intégration de SETs métalliques à

double grilles dans l'unité de fabrication finale BEOL (Back-End-Of-Line) d'une technologie CMOS à l'aide du procédé *nanodamascene*. Le système sur puce profitera de la très élevée sensibilité à la charge électrique du transistor monoélectronique, ainsi que le traitement de signal et des données à haute vitesse en utilisant une technologie de pointe CMOS disponible.

Les MOSFETs issus de la technologie FD-SOI (Fully Depleted-Silicon On Insulator) sont une solution très attractive à cause de leur pouvoir d'amplification du signal quand ils sont opérés dans le régime sous-le-seuil. Ces dispositifs permettent une très haute densité d'intégration due à leurs dimensions nanométriques et sont une technologie bien mature et modélisée. Ce travail se concentre sur le développement d'un procédé de fonctionnalisation d'un MOSFET FD-SOI comme démonstration du concept du capteur de gaz à base de transistor à double grilles.

La sonde Kelvin a été la technique privilégiée pour la caractérisation des matériaux sensibles par le biais de mesure de la variation du travail de sortie induite par l'adsorption de molécules de gaz. Dans ce travail, une technique de caractérisation des matériaux sensibles alternative basée sur la mesure de la charge de surface est discutée.

Pour augmenter la surface spécifique de l'électrode sensible, un nouveau concept de texturation de surface est présenté. Le procédé est basé sur le dépôt de réseaux de nanotubes de carbone multi-parois par pulvérisation d'une suspension de ces nanotubes. Les réseaux déposés servent de «squelettes» pour le matériau sensible.

L'objectif principal de cette thèse de doctorat peut être divisé en 4 parties : (1) la modélisation et simulation de la réponse d'un capteur de gaz à base de SET à double grilles ou d'un MOSFET FD-SOI, et l'estimation de la sensibilité ainsi que la puissance consommée; (2) la caractérisation de la sensibilité du Pt comme couche sensible pour la détection du H_2 par la technique de mesure de charge de surface, et le développement du procédé de texturation de surface de la grille fonctionnalisée avec les réseaux de nanotubes de carbone; (3) le développement et l'optimisation du procédé de fabrication des SETs à double grilles dans l'entité BEOL d'un substrat CMOS; et (4) la fonctionnalisation d'un MOSFET FD-SOI avec du Pt pour réaliser la fonction de capteur de H_2.

Mots-clès : Transistors monoélectroniques, Intégration 3D monolithique, Capteur de gaz à base de FET, Capteur de gaz, Détection du dihydrogène, Texturation de surface de la couche sensible, Réseaux de MW-CNTs, Ultra-basse consommation, FDSOI.

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List of Acronyms

AC	Alternating Current
ADC	Analogue-to-Digital Converter
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
BEOL	Back-End-Of-Line
BOX	Buried Oxide
CCP	Capacitively Coupled Plasma
CLM	Channel Length Modulation
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Planarization
CNT	Carbon NanoTube
CNT-FET	Carbon NanoTube-Field Effect Transistor
CPD	Contact Potential Difference
CVD	Chemical Vapour Deposition
DAQ	Data acquisition
DC	Direct Current
DG-SET	Double Gate-Single Electron Transistor
DIBL	Drain Induced Barrier Lowering

DMM	DMM
EBL	E-Beam Lithography
EL	Ethyl L-lactate
EPR	Electron Paramagnetic Resonance
FD-SOI	Fully Depleted-Silicon On Insulator
FET	Field Effect Transistor
FIB	Focused Ion Beam
FTIR	Fourier Transform InfraRed
GPIB	General Purpose Interface Bus
IC	Integrated Circuit
ICP	Intrinsically Conducting Polymer
ICP	Inductively Coupled Plasma
ILD	Inter Layer Dielectric
IR	Infrared
ITRS	International Technology Roadmap for Semiconductors
KP	Kelvin Probe
MFC	Mass Flow Controller
MIM	Metal Insulator Metal
MOSFET	Metal Oxide Semiconductor- Field Effect Transistor

MOX	Metal Oxide
MW-CNT	Multi Walled-Carbon NanoTube
NMP	1-methyl-2-pyrrolidinone
NW	NanoWire
NWFET	Nanowire Field Effect Transistor
PEI	Poly(-ethyleneimine)
PID	Proportional-Integral-Derivative
PMMA	Poly(methyl methacrylate)
PolFET	Polymer Field Effect Transistor
PVD	Physical Vapour Deposition
QCA	Quantum Cellular Automata
QMB	Quartz MicroBalance
RF	Radio Frequency
RH	Relative Humidity
RIE	Reactive Ion Etching
RT	Room Temperature
SAW	Surface Acoustic Waves
SCPI	Standard Commands for Programmable Instruments
SEM	Single Electron Memory

SEM	Scanning Electron Microscope
SET	Single Electron Transistor
SG-FET	Suspended Gate-Field Effect Transistor
SH	Self Heating
SoC	System On Chip
SW-CNT	Single Walled-Carbon Nanotube
TEOS	TetraEthyl OrthoSilicate
TFET	Tunnel Field Effect Transistor
TPD	Temperature Programmed Desorption
TTL	Transistor-Transistor Logic
UTBB	Ultrathin body and BOX
UV	UltraViolet
VO	Velocity Overshoot
VOC	Volatile Organic Compound

List of Symbols

e	The elementary electric charge
μ_{dipole}	Dipolar moment of a dipole
d_{dipole}	Distance separating the barycentres of the opposite charges of a dipole
Q_{dipole}	Charge of dipole layer capacitor model
$\Delta\Phi$	Work function variation
N_{max}	Maximum number of adsorption sites
Θ	Coverage rate
E_C	Conduction band energy level
E_V	Valence band energy level
E_F	Fermi energy level
Λ_{air}	Thickness of the space charge layer caused by O_2 chemisorption on an n-type metal oxide surface
$eV_{surface}$	Energy barrier height of the surface band bending caused by O_2 chemisorption on an n-type metal oxide surface
λ_D	Debye length
Z_0	Thickness of the depleted surface layer of a sensing metal oxide layer
Z_g	Thickness of a sensing metal oxide layer
qV_s	Energy barrier height of the surface band bending of a compact sensing metal oxide layer

X_g	Grain size of a porous sensing metal oxide layer
ΔE_A	Activation barrier
ΔH_{chem}	Heat of chemisorption
K_b	Boltzmann constant
T	Temperature
ΔV_i	Potential change of the metal surface (gate metal)
V_g	Gate voltage of a FET (MOSFET or CNT-FET)
I_{ds}	Drain-to-source current of a FET (MOSFET or CNT-FET)
V_{th}	Threshold voltage of a FET (MOSFET or CNT-FET)
Δn	Charge carrier concentration variation of graphene
N_i	Concentration of adsorption induced impurities in graphene
C_S	Island-to-source tunnel junction capacitance
R_S	Island-to-source tunnel junction resistance
C_D	Island-to-drain tunnel junction capacitance
R_D	Island-to-drain tunnel junction resistance
q_1	Charge accumulated at the source
q_2	Charge accumulated at the drain
C_Σ	Total island capacitance of a single-island, double tunnel junction system or an a SET

U	Electrostatic energy
V_{DS}	Drain-to-source voltage of a single-island, double tunnel junction system or a SET
E_c	Charging energy of a single electron
$\Delta E_{S\to I}$	The electrostatic energy barrier seen by an electron reaching the island from the source
$\Delta E_{I\to D}$	The electrostatic energy barrier seen by an electron leaving the island to the drain
N	number of electrons charging the island
Q	Island net charge
I_{DS}	Drain-to-source current of a single-island, double tunnel junction system or a SET
V_C	Coulomb blockade voltage
t	Lifetime of the charging
h	Planck's constant
R_t	Tunnelling junction resistance
C_t	Tunnelling junction capacitance
R_q	Quantum resistance
V_{GS}	Gate to source voltage of a SET
V_{GS}^{th}	Threshold gate voltage of a SET
C_G	Gate-to-island capacitance

Q_0	Island background charge
Γ	Tunnelling rate
F	Helmholtz's free energy
R_t	Tunnel junction resistance
P_i	Occupation probability of state *i*
$\Gamma_{i\to j}$	Tunnelling rate from state *i* to state *j*
W	FET channel width
L	FET channel length
C_{eq}	equivalent gate capacitance of a SG-FET
g	Transistor transconductance
μ	FET channel mobility
S	Sensitivity of a SG-FET-based gas sensor
C_B	Bias gate capacitance of the DG-SET-based gas sensor
C_G	Functionalized gate capacitance of the DG-SET-based gas sensor
V_B	Bias gate voltage of the DG-SET-based gas sensor
V_G	Functionalized gate potential of the DG-SET-based gas sensor
I^0	Operation current of the DG-SET-based gas sensor
Q^0	The functionalized gate surface charge of the DG-SET-based gas sensor under background gas

V_{shift}	Voltage applied to the bias gate
${Q_{gf}}^0$	Functionalized gate (front gate) surface charge of a FD-SOI-based gas sensor under background gas
Q_{gf}	Functionalized gate (front gate) surface charge of a FD-SOI-based gas sensor, also referred to as front gate charge
V_{gf}	Functionalized gate potential of a FD-SOI-based gas sensor
V_{gb}	Back gate bias of a FD-SOI-based gas sensor
C_S	Island-to-source capacitance of the DG-SET-based gas sensor
C_D	Island-to-drain capacitance of the DG-SET-based gas sensor
C_B	Island-to-side gate capacitance of the DG-SET-based gas sensor
C_G	Island-to-top gate capacitance of the DG-SET-based gas sensor
C_3	Functionalized gate-to-side gate of the DG-SET-based gas sensor
C_1	Functionalized gate-to-source of the DG-SET-based gas sensor
C_2	Functionalized gate-to-drain of the DG-SET-based gas sensor
C_4	Bias gate-to- source of the DG-SET-based gas sensor
C_5	Bias gate-to-drain of the DG-SET-based gas sensor
I_{DS}	Drain-to-source current of the DG-SET-based gas sensor
V_{DS}	Drain-to-source voltage of the DG-SET-based gas sensor
$W_{Side\ gate}$	Side gate width
$D_{Side\ gate}$	Side gate-to-island distance

W_I	Island width
L_I	Island length
$t_{Dielectric}$	Tunnel junction dielectric thickness
t_{CMP}	Structure thickness
$D_{Top\ gate}$	Top gate-to-island distance
A	Top gate side length
K	Top gate dielectric permittivity
R	Top gate-to-island capacitance-to-top gate total parasitic capacitance ratio
α	Coefficient expressing how much times the charging energy is larger than the thermal energy
V_{BS}	Bias gate-to-source voltage of a DG-SET-based gas sensor
V_{DS}	Drain-to-source voltage of a DG-SET-based gas sensor
I_{DS}	Drain-to-source current of a DG-SET-based gas sensor
C_{oxf}	Front gate capacitance of an FD-SOI MOSFET
$\varphi(x,y)$	2D potential distribution along the channel of an UTBB FD-SOI MOSFET
V_{bi}	The built in potential across the source/drain-channel junctions
V_{ds}	The drain voltage
x and y	Si channel coordinates of an UTBB FD-SOI MOSFET
$\lambda(x)$	The natural length at any position x along the channel

t_{oxf}	The front gate oxide thickness
t_{oxb}	The back gate oxide thickness
ε_{Si}	The dielectric permittivity of silicon
ε_{ox}	The dielectric permittivity of the oxide
t_{Si}	Si body thickness
V_{fbf}	Flat band voltage of the front gate
V_{fbb}	Flat band voltage of the back gate
V_{gf}	Front gate potential
V_{gb}	Back gate potential
x_c	The effective conductive path position
V_{thf}	The front gate threshold voltage
Q_{thf}	Threshold charge carrier sheet density at the effective path
λ_f	the natural length of the front gate
n_i	carrier concentration of the Si channel
L_{eff}	The effective length due to the CLM effect
W	The channel width
C_{oxf}	The front gate oxide capacitance per unit area
η_f	The front interface ideality factor
μ_{eff}	The effective carrier mobility

v_{sat}	The saturation velocity
Q_{inv}	Inversion charge carrier density
Q_{gf}	The front gate charge (front gate surface charge)
θ_1 and θ_2	mobility attenuation factors
R_{sd}	Series resistance
ΔL	Length shortening
V_{dsat}	The saturation drain voltage
V_E	Fitting parameter
$v_{sat,\ VO}$	Velocity overshoot modified saturation velocity
λ_w	Energy relaxation length
τ_w	Energy relaxation time constant
N_A	The doping concentration of the silicon channel
N_{SD}	The doping concentration of the source/drain contacts
R_{th}	Silicon thermal resistance
K_{Si}	The thermal conductivity of silicon
K_{ox}	The thermal conductivity of silicon dioxide
$\mu_{eff,\ SH}$	Self-heating modified effective mobility
$\mu_\circ$	Low field mobility
r	The mobility temperature exponent

V_c	Counter sweeping voltage applied between Kelvin probe and the material
E_{vacuum}	Vacuum energy level
C_F	Reference capacitance
C_S	Source capacitance
Q	Charge to me measured by an electrometer
A	Open loop gain of the operational amplifier
V_S	The potential associated to the charge to be measured
Z_F	The feedback impedance in a coulombmeter
Z_S	Source impedance
C_{IN}	Input capacitance of the electrometer
$Q_{response}$	Charge reading signal after reaching the steady state
$Q_{baseline}$	Charge reading signal in absence of target gas
ΔQ	Charge reading variation
K_{ads}	adsorption reaction constant
K_{des}	Desorption reaction constant
Θ	Coverage rate of H_a
υ	Coverage rate of OH_a
φ	Coverage rate of NH_a
ψ	Coverage rate of NH_{2a}

$[S_t]$	Density of available surface sites for chemisorption, occupied or unoccupied
P_{H_2}	Partial pressure of H_2 in the gas phase
P_{O_2}	Partial pressure of O_2 in the gas phase
P_{N_2}	Partial pressure of N_2 in the gas phase
ΔQ_{max}	Maximum charge variation due to chemisorption of hydrogen on all adsorption sites.

CHAPTER 1 Introduction

1.1 General

Nowadays, the society enjoys emerging integration technology, thanks to the beginning of nanoelectronics era, enabling system miniaturization with increased computational power together with diversified functionalities. This has led among others, to the emergence of nomadic battery powered wireless systems such as portable consumer electronic devices (smartphones, activity trackers…), wireless sensor systems, ambient intelligence devices and more. It is impacting not only society lifestyle but also industrial monitoring applications, defense and healthcare devices.

The need of integration of new functionalities on systems on chips (SoCs) has to take into account all the problematic of heterogeneity together with energy consumption and thermal power dissipation. In this context, all memories, sensing components and other functionalities added to the CMOS (Complementary Metal Oxide Semiconductor) have to respect drastic supply energy requirements, especially for autonomous electronic system applications.

Autonomous electronic systems can be defined as "an electronic system that has been designed to operate and/or communicate as long as possible in known/unknown environments providing, elaborating and storing information without being connected to a power grid" [33]. From the energy point of view autonomous sensor systems should be able to operate with less than hundreds of μW of power within less than some cubic centimeter [33]. Autonomous sensor systems do not escape from this stringent requirement.

Nowadays, smart mobile systems already incorporate a large number of embedded sensing components such as accelerometers, temperature sensors, infrared (IR) detectors, etc., but up to now gas sensors cannot be fully integrated in compact SoCs mainly for power consumption considerations.

1.2 Gas sensor integration challenges

The integration of gas sensors is limited since most used and reliable gas sensors, semiconducting metal oxide (MOX) resistors and catalytic MOSFETs (metal oxide

semiconductor field effect transistors) are generally operated at high temperatures, 200–500 °C [2, 4, 5, 13] and 140–200 °C [15, 34, 35] respectively.

The need of a high operating temperature induces an important energy cost for conventional MOX gas sensors and catalytic MOSFETs. The total power consumption of a gas sensor system includes 3 main contributions: the transducer device, the heating element and the associated electronics including read-out, analogue-to-digital converter (ADC) and logic processing circuits. Typical power consumption of MOX gas sensors, which are the widely available commercial sensors, is in the range of 200 mW to 1 W [4, 15], which is too much for battery-powered applications.

The heater is largely the main contributor to the total power consumption. The energy supply demands of these types of gas sensors are in conflict with the drastic requirement for portable integrated sensor systems (mobile systems). Moreover full integration of such gas sensors with electronics (for signal processing) on the same substrate is problematic not only for power consumption concern but also because such high operating temperature is not compatible with CMOS operation.

Gas sensor integration within standard microelectronics technologies has been extensively developed and lead to the use of micromachined silicon substrate. The gas sensor components are embedded in a thin dielectric suspended membrane of low thermal conductivity which provides good thermal isolation between substrate and the heated gas-sensitive region. This technology has lowered the power consumption to the 30–150 mW range [4] and allowed the integration of signal-processing electronics on the same substrate.

1.3 Emergence of low power transistors

The exponential increase of transistor integration density, the more and more complex integrated circuits (ICs) and its increasing speed have led to a “power crisis” in advanced CMOS technology. The power density in microprocessors is already above 100 W/cm^2.

Power consumption and heat dissipation in electronic devices are becoming a critical issue for the future ICs technology. “The carbon footprint of only the internet is higher than that of the worldwide air traffic” [36]. In 2014, the US data centres consumed 2% of the country’s total US

energy consumption [37]. Energy consumption requirement is even more critical for mobile electronic systems such as mobile phones, tablets, PCs, embedded systems, etc.

At the moment, CMOS device scaling allows to decrease the transistor power consumption following the International Technology Roadmap for Semiconductors (ITRS) roadmap. New ultra-low power electronic devices are coming more and more into focus as the ongoing miniaturization in IC technology demands new innovative solutions or new paradigms to keep pace with Moore's Law, while meeting the stringent power consumption requirement. Such "green devices" are tunnelling FETs (TFETs), multi-gate FETs, nanowire FETs (NWFETs) and single electron transistors (SETs). These devices offer a great decrease in the operation voltage and drive current.

1.4 Open questions and research project objectives

The use of a SET as a transducer is of great interest for several reasons. Its greatest advantage is its ultra-high electric charge sensitivity. SETs are known to be hyper electrometers [38]. In addition their small size (few tens of nanometres) is very valuable from the integration density point of view. Moreover, SETs are ultra-low power devices inherent to the fundamental of their operation based on the transport of reduced number of electrons.

Integration of SETs with advanced low power CMOS for applications not requiring high speed is presenting valuable advantages such as a high integration density without facing the problematic power consumption. Hybrid SET-CMOS technology has a great potential for heterogeneous integration of memories, sensors, etc. In particular, the 3D integration of SETs on CMOS technology for gas sensing functionality, illustrated in Fig. 1.1, is of great interest. It presents the advantage of an ultra-low power application. The integration on a CMOS substrates allows to benefit from CMOS circuits for the read-out and signal processing and to give new functionalities to CMOS chips.

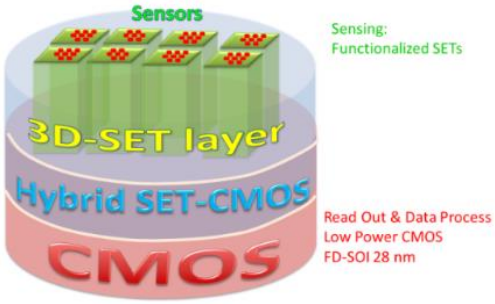

Figure 1.1 Concept of 3D SET-CMOS Integrated Circuits and Sensors [1].

In this context, the proposed research project is focused on the proof of concept of 3D monolithic integration of a SET-based gas sensor, on CMOS technology. The proposed approach relies on 3D integration of SET-based gas sensors in the Back-End-Of-Line (BEOL) of advanced FD-SOI (fully depleted-silicon on insulator) CMOS circuits. Integration of ultra-sensitive sensors in the BEOL unit of CMOS technology is in line with the "More than Moore" roadmap paving the way to future high value products in the world of smart and mobile electronics. We also aim to take advantage of the SET sensitivity down to the single electric charge to achieve a decrease in the heating of the sensing material. The hyper sensitivity of the SET would compensate for reduced "chemical signal" resulting from the reduced temperature.

These last years, several research teams have explored various designs and concepts for the demonstration of CMOS compatible SETs operating at room temperature and fabricated with a reproducible fabrication process. In 2007, the group of D. Drouin from Université de Sherbrooke has published the fabrication of Metallic SETs operating at up to 430K [39] by the so-called "*nanodamascene*" process. This fabrication process, co-invented by D. Drouin, is a new approach for the fabrication of metallic single electron devices. The process relies on thinning embedded metallic structures in a dielectric layer by chemical mechanical planarization (CMP) in a similar way to interconnects fabrication processes in ICs. A schematic of the device structure is shown in Fig. 1.2. This breakthrough has been recognized by the industry as a significant proof of room temperature SET operation, and is referenced in the 2009 ITRS. In 2011, the integration of operational metallic SETs in the BEOL of advanced CMOS circuits has

been demonstrated by Jouvet et al. [29], within a collaboration between Université de Sherbrooke, CNRS and [2]STMicroelectronics.

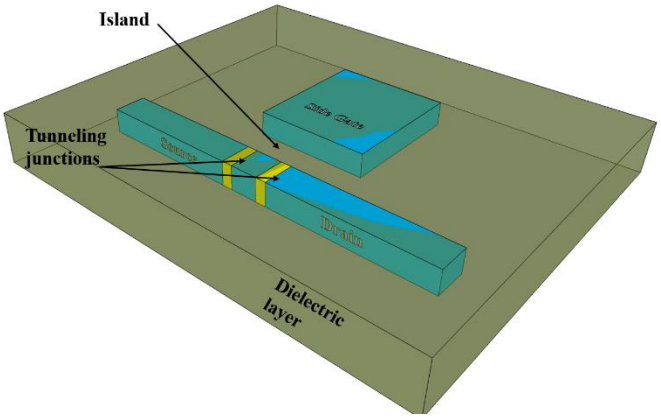

Figure 1.2 3D schematic representation of a SET embedded in a dielectric layer fabricated by the *nanodamascene* process.

The technological know-how of SET integration in the BEOL of advanced CMOS circuits is the first building block towards the implementation of a fully integrated gas sensor. The proposed architecture is shown in Fig. 1.3.

The general concept is to incorporate a functionalized top gate with a dedicated gas-sensitive material in addition to the side gate. The functionalized gate is kept floating with the sensing layer exposed to the gas to be detected, while the side gate is biased to control the operation point of the transistor. The functionalized top gate potential variations induced by target gas molecule adsorption gate the transistor.

[2] CNRS stands for The *Centre National de la Recherche Scientifique* (National Center for Scientific Research), which is a public organization under the responsibility of the French Ministry of Education and Research.

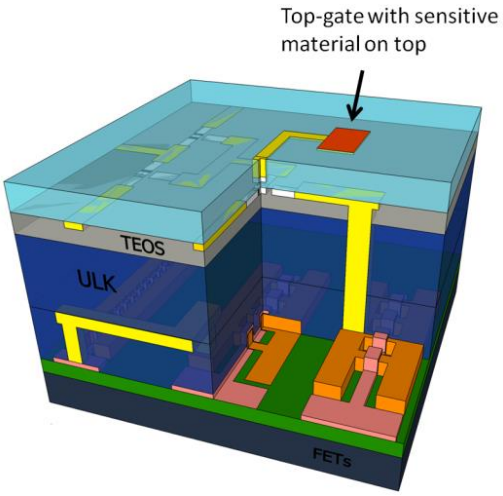

Figure 1.3 3D schematic representation of the proposed concept of a fully integrated metallic SET gas sensor on a CMOS substrate.

The double gate approach can be applied also to any FET that allows the channel gating by two separate gates. Such configuration of double-gated FET is possible with FD-SOI MOSFETs. In addition to the front gate, the substrate bulk Si can be used for back biasing of the transistor channel through the buried oxide (BOX). Such a device is very promising for gas sensing applications due to their amplification capability when operated in the sub-threshold regime, which is the strongest asset of these devices with respect to the FET-based gas sensor technology. In addition the small size of these devices is also of a high interest in terms of integration density. FD-SOI FETs are a mature technology and well modelled.

1.5 Outline of this thesis

The thesis manuscript is organized as follows:

Chapter 2 reviews integrated gas sensor technology with a focus on conductivity and FET type gas sensors. An overview of different gas sensor technologies as well as different sensing material types is presented. The sensing mechanism of MOX resistors as well as FET-based gas sensors is described. A brief overview of gas adsorption/desorption on solids is given.

In chapter 3 both the double gate-SET (DG-SET) and the FD-SOI MOSFET-based gas sensors concepts and expected sensitivities are presented. The SET operation principle is presented and detailed. A brief overview of the Orthodox theory is given. Modelling and design of the proposed DG-SET-based gas sensor together with a simulated response is discussed. A FD-SOI

MOSFET-based gas sensor simulation model is given and the impact of the channel length and back gate bias on the sensor sensitivity is studied.

In Chapter 4, a new technique for material sensitivity evaluation based on measurement of material surface charge/potential variation induced by gas molecules adsorption is presented. A new sensing electrode surface texturing process is presented. The sensitivity to hydrogen of Pt layers have been investigated with the surface charge measurement technique. Obtained experimental data are analyzed and discussed.

In chapter 5, a brief introduction and evolution history of the nanodamascene process is given. The developed fabrication process, based on the "*nanodamascene*" process, is presented and different steps as well as the lithography patterns are detailed. Major fabrication process issues and proposed solutions are discussed. A FD-SOI FET functionalization process with Pt for H_2 sensing is presented. Electrical characterizations are discussed.

Chapter 6 presents a summary of the obtained results and the project original contributions. Some perspectives and outlooks are discussed as well as some of the possible implementations of the DG-transistor-based gas sensors.

CHAPTER 2 Literature review on integrated gas sensors

2.1 Introduction

A very broad range of technologies has been investigated for gas molecules detection. Some of these technologies have been already commercialized. Mainly, the gas sensor development aims at improving the "3S" performance parameters: sensitivity, selectivity and stability. Gas sensor development aims at other demands such as short response time, good reversibility, low cost, small size and low power consumption.

A gas sensor is a chemical sensor operated in the vapour phase. It consists of two parts: (i) gas-sensitive material and (ii) transducer. Gas species interact with the sensitive material by adsorption, desorption, absorption or chemical reactions at the surface and/or the bulk of the material. These interactions give rise to reversible changes in one or more of the sensing material physicochemical properties such as its mass, conductivity, work function or optical properties. These variations, containing the chemical information, are converted, by the means of the transducer, into an electrical signal such as frequency, current, or voltage, which is then subjected to further data treatment and processing.

Variations in sensitive material physical properties might be measured by different transducer principles depending on the physical property to be monitored, which gives rise to several types of gas sensors, as illustrated in Fig. 2.1. Several detection principles can be employed for a specific gas sensing, depending on the required characteristics for the sensor, such as the sensitivity, selectivity, linearity, and response time, and sensing concentration range. Table 2.1 summarizes the most common physical properties of gas-sensitive material giving different transduction principles.

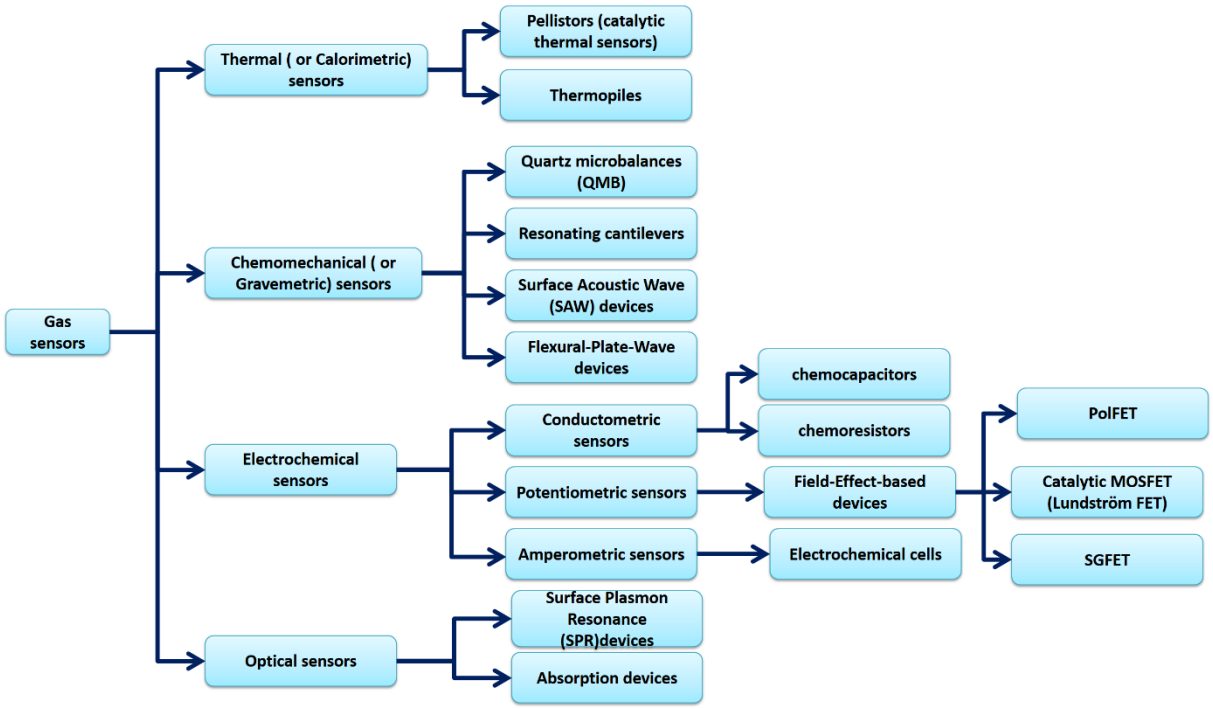

Figure 2.1 Different types of gas sensors.

Table 2.1 Physical changes in the gas-sensitive material and corresponding sensor device type.

Gas induced physical property change in the sensitive material	**Type of gas sensors**
Mass	Gravimetric sensors (Resonating cantilever, QMB, SAW sensors)
Conductivity	Chemoresistors (metal oxide resistor, polymer resistor)
Work function	Filed-Effect-based gas sensors (Catalytic MOSFET, SG-FET, PolFET)
Optical absorption	Absorption devices (CO_2 IR sensor)
Temperature	Calorimetric sensors (thermopiles, pellistors)

Most common integrated gas sensor devices are based on semiconducting metal oxides (MOXs), intrinsically conducting polymers (ICPs), conducting polymer composites, catalytic metals, in combination with chemoresistors (or conductivity gas sensors), FET-based gas sensors (catalytic MOSFETs, suspended gate-FETs (SG-FETs)), quartz microbalances (QMB) and surface acoustic wave (SAW) devices.

2.2 Sensing materials

Gas sensitive material is a key part in the sensing mechanism. Interactions behind the gas molecules recognition involve adsorption (chemisorption and/or physisorption), absorption, surface reactions, diffusion, etc. Characteristics of the sensitive material, such as sensitivity and selectivity, are often tuned by adding dopants, modifying microstructure or varying the operating temperature. Three classes of materials have been widely used as gas sensitive materials in integrated gas sensors: (i) Semiconducting metal oxides (ii) polymers and (iii) catalytic metals (table 2.2).

A gas sensitive material can be applied to different transducer devices. So the selection of the optimal sensing material becomes a key point and will depend on the desired requirements and the operation parameters. Operation parameters, which depend on the gas sensor application, involve: operating temperature, sensing chemical environment (interfering gases, humidity, etc.), and analyte concentration range. Performance related requirements are sensitivity, selectivity, stability, and time response. Integration related requirements are size, power consumption, fabrication process complexity, cost, etc.

Hydrogen or hydrogen containing molecules are known to be adsorbed on catalytic metals, such as Pd, Pt, Ir, Ag, and Au, and be dissolved. This is the key property behind of their use in combination with either MOSFET [13–15, 35, 40] or SG-FET [16, 32, 41, 42] devices. Semiconducting metal oxides such as SnO_2, TiO_2, WO_3, ZnO and In_2O_3, have been used mostly as chemoresistors [43, 44] but also with SG-FETs [32, 45]. Intrinsically conducting polymers (ICP) and conducting polymer composites are the two types of polymers used as sensing layers in gas sensors. ICPs are π electron conjugated polymers that can be doped as semiconductors or conductors. Conducting polymer composites consist of conducting particles, mainly polypyrrole or carbon black dispersed in an insulating polymer matrix. Polymers have served as sensing

layers mostly in chemoresistors (conductivity gas sensors) [2] and FET-based gas sensors such as PolFET [46].

Table 2.2 Typical gas sensitive materials used in integrated gas sensors.

Class of material	**Examples**
Catalytic metals	Pd, Pt, Ir, Ag, Au
Metal oxides	Cr_2O_3, Mn_2O3, Co_3O_4, NiO, CuO, SrO, In_2O_3, WO_3, TiO_2, V_2O_3, Fe_2O_3, GeO_2, Nb_2O_5, MoO_3, Ta_2O_5, La_2O_3, CeO_2, Nd_2O_3,…
Polymers	polypyrrole, polytiophene, polyaniline, poly(dodecylthiophene), polyindole, Trans-polyacetylene, polyphenylene, carbon black composite, polypyrrole particle composite

2.3 Gas adsorption/desorption on solids

Gas adsorption on solids can take two forms: either by physisorption, or chemisorption. For the former, gas species are bound only by Van der Waals forces (without any chemical interaction taking place). Therefore adsorbed gas molecules are not chemically altered during adsorption process and the binding is very weak (below 100meV) [12]. Thus, physisorption is always reversible and adsorbates can be easily desorbed by heating or even at room temperature. Physisorption has low optimum temperature and leads only to a surface dipole layer which causes a surface potential variation/surface charge variation [12, 42].

In case of chemisorption, gas species are adsorbed via strong chemical bindings (ionic binding, covalent binding) and thus they are chemically modified as adsorbates. For instance, they can dissociate and adsorb on the surface of the solid in form of charged sub-molecules or single atoms, as it is the case in dissociative chemisorption. Therefore chemisorption is not always reversible. During chemisorption, a partial electron transfer from or to the solid conduction band occurs depending on adsorbate electronegativity and temperature [12]. Chemisorbed species

create a layer of dipoles. This layer induces a change in surface charge (surface charge accumulation or net surface charge) variation and thus a surface potential variation.

Physisorption is associated to a neutral state of adsorbate, while chemisorption to a charged one [43]. But both types of adsorption lead to the formation of surface dipole layer. This local dipole layer causes a potential shift (surface potential variation), which is much stronger in the case of chemisorption than in the case of physisorption.

The chemisorbed species and the underlying atom(s) of the solid can be seen as an electric dipole carrying a dipolar moment μ_{dipole}. The dipolar moment is either pointing away or to the surface and has an amount depending on the polarization of the chemical bond (s) within the formed adsorption chemical complex. Either the positive or negative end pointing away from the surface depends on the difference in electron affinity of the adsorbate and the solid atom(s). The formed surface dipole layer can be modelled by a plate capacitor carrying $+Q_{dipole}$ and $-Q_{dipole}$ as opposite charges separated by the distance d_{dipole}. The induced work function change $\Delta\Phi$ is obtained by the Helmholtz equation [47]:

$$\Delta\Phi = 4\pi\ \Theta\ N_{max}\ \mu_{dipole}\ \ f^*\ ;\ f^* = 4\pi/\epsilon_0 \qquad (2.1)$$

where N_{max} is the maximum number of adsorption sites per unit area, and Θ is the coverage rate, and is ϵ_0 the permittivity of vacuum.

It is assumed that the plane of electroneutrality, defined with respect to the image charge plane within the substrate surface, is within the adsorbate layer. An emerging electron must work only against half of the adlayer potential.

Adsorbed atoms or molecules to the surface of a sensitive material either by chemisorption or physisorption, induce a work function variation. This work function variation depends on surface coverage rate of gas atoms or molecules. Since the surface coverage rate is dependent on gas species concentration (partial pressure). Measuring this work function variation can be used as an indicator for gas species and their corresponding concentrations [12, 42].

2.4 Conductivity gas sensors

Conductivity gas sensors also named chemoresistors, work on the principle that interactions of the sensing layer with gas molecules lead to resistance (conductance) change. The most commonly used sensing material classes are semiconducting metal oxides, ICP and conducting polymer composites [2]. The mechanisms behind the change in resistance of the sensing layer are different for each material type. However, the structure and layout of conductivity gas sensors are mainly the same for the 3 classes of material.

Conductivity gas sensors consist of a gas sensitive layer deployed on an insulating substrate between two interdigitated or parallel metallic electrodes, which form the electrical connections through which the relative resistance change is measured. A schematic of a typical conductivity gas sensor design is shown in Fig. 2.2. The insulating substrate, which could be made of glass, alumina, or other ceramics, is heated in case a semiconducting metal oxide is used as a sensing layer.

For effective sensing semiconducting metal oxide conductivity gas sensors need to operate at high temperature, typically 200–500 °C [2, 5, 13]. However polymer-based conductivity gas sensors operate at room temperature [2].

The semiconducting Metal oxide gas sensors have been applied for the sensing of a wide range of gases including NH_3, nitrous oxides (NO_2 or NO), CO, CO_2, H_2S, SO_2, H_2, O_2, O_3, CH_4, and some VOCs [2, 5, 7, 13, 43], while polymer-based resistors were employed generally dedicated to VOCs sensing (ethanol, CH_4, $CHCl_3$) [2, 13].

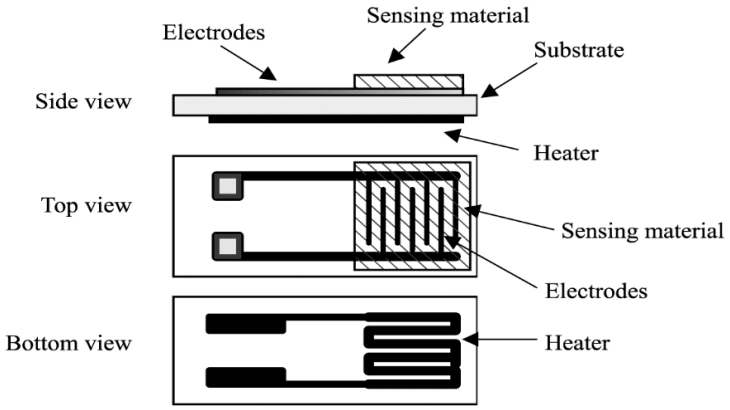

Figure 2.2 Typical structure of a conductivity gas sensor. Reproduced from [2].

Polymer composite sensing layers are usually deposited by spin coating, dip coating, spray coating or screen printing, with film thickness ranging in the few tens of nm to 1 µm. ICPs are generally deposited onto the substrate, using electrochemical techniques or by chemical polymerization carried out directly to the substrate [2, 13]. Metal oxide can be deposited as a thick or thin film layer. A broad range of techniques are used for semiconducting metal oxide deposition including physical vapour deposition (PVD) techniques (evaporation or sputtering), chemical vapour deposition (CVD) techniques, so-gel techniques and screen printing which is most widely used technique in industry [7]. Film thickness ranges from 10 to 300µm for thick films and 6–1000 nm for thin films [2].

Conducting polymer composite resistors change in resistance is due to diffusion of gas species into the polymer film. Permeated gas molecules into the polymer composite film make the polymer expand. Polymer expansion reduces the number of conducting pathways for charge carriers [48]. Conducting polymer composite resistors exhibit a highly linear response to a wide range of gases [48] with a detection limit $\leq$ 0.1-5 ppm (parts per million) [2] and response times ranging from seconds to minutes [48]. They are relatively inexpensive and operate at ambient temperature, which is an important advantage relevant to mobile autonomous systems. Polymer composite-based conductivity sensors suffer from aging which leads to drift in response signal [2] and high sensitivity to humidity.

The sensing mechanism of ICP-based conductivity sensors is poorly understood. Generally, vapour diffusion into the sensing polymer film causes swelling and therefore alters the conductivity [34]. According to several authors, three types of conductivity are altered by the vapour sorption [2]:

- (1) The intra-chain conductivity i. e. the conductivity along the backbone;
- (2) The intermolecular conductivity which is due to electrons hopping to different chains because of analyte absorption; and
- (3) The ionic conductivity which is affected by protons tunnelling induced by hydrogen bond interaction at the backbone and also by ion migration through the polymer.

ICP resistors respond to a wide range of VOCs, especially polar analytes, with sensitivities in the 0.1-100 ppm range and response times generally varying from seconds to minutes [2, 13].

They are inexpensive and operate at ambient temperature, but they suffer from a high sensitivity to humidity [34] and sensor response drift due to oxidation of the polymers over time [2, 13].

Several interaction mechanisms cause changes in the conductivity of the semiconducting metal oxide depending on the morphology and the microstructure. These mechanisms will be detailed in the next section. In thick film technology a heater is integrated on the back side of the substrate, as shown in Fig 2.3. In thin film technology, the electronic devices are mostly thermally isolated by their integration onto micro-hotplates using silicon micromachining (bulk & surface micromachining) and thin film deposition (Fig 2.4). This technology shows lower power consumption compared to the thick sensors. Metal oxide gas sensors exhibit fast response and recovery times. The main drawback of this type of sensor is the need for high temperature, typically 200–500 °C, for the operation, which results in a high power consumption not suitable for portable applications. A comparison of the 3 types of conductometric gas sensors is presented in table 2.3. In the following, emphasis will be on metal oxide gas sensors as they are of high interest to our research project. The sensing mechanism of metal oxide gas sensors will be detailed and recent advances in the field will be presented.

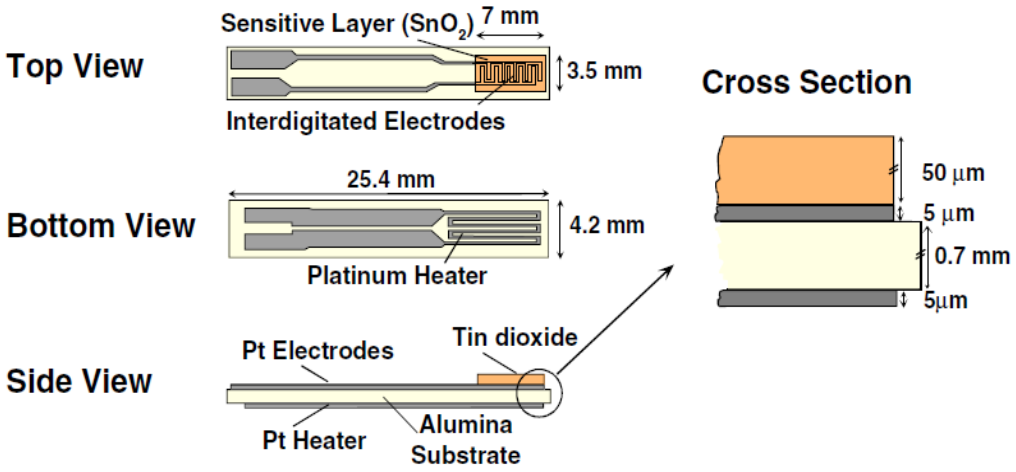

Figure 2.3 Typical Structure of a metal oxide gas sensor. Reproduced from [3].

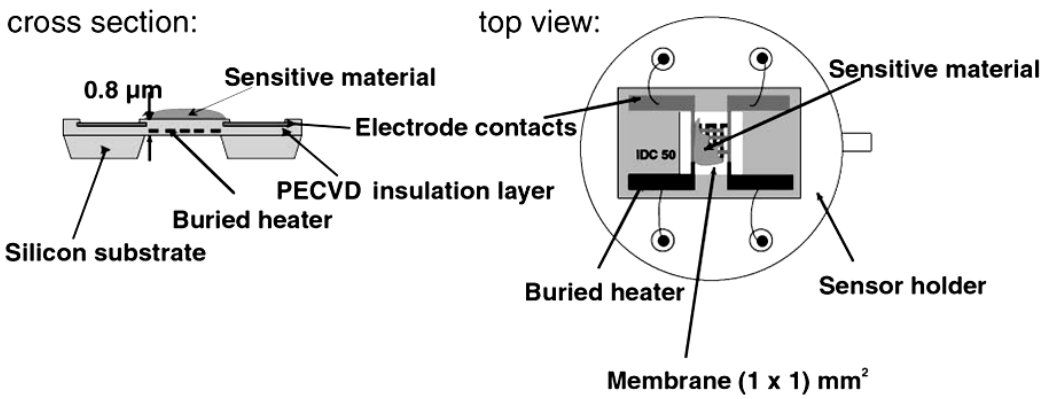

Figure 2.4 Metal oxide gas sensor based on a micromachined hotplate on a Si substrate. Reproduced from [4].

Table 2.3 Comparison of the 3 conductometric gas sensor types.

	Conducting polymer composite	**Intrinsically conducting polymer**	**Semiconducting metal oxides**
Operating Temperature	Room Temperature	Room Temperature	200–500°C
Detection limit range	0.1–100 ppm	0.1–100 ppm	5–500ppm
Advantages	Low cost; Low energy consumption.	Low cost; Low energy consumption; Good response time.	Low cost; Short response time; Long life time.
Disadvantages	Highly sensitive to humidity; Response drift with time (aging).	Highly sensitive to humidity; Response drift with time (aging).	Sensitive to environmental factors ; High energy consumption.

2.5 Metal oxide gas sensors

Metal oxide gas sensors have attracted much interest and are currently in large-scale use since they offer low cost, a wide range of target gases, simplicity in fabrication and high sensitivity. These advantages have worked in their favour over other technologies as a wide use technology for gas sensing.

Despite the working principle of metal oxide chemoresistors, the gas sensing mechanism is complex and still controversial, but essentially trapping of electrons at adsorbed molecules and band bending induced by these charged molecules are responsible for a change in conductivity [5].

Interactions taking place at the metal oxide surface involve reduction/oxidation of the semiconductor, adsorption of the gas molecules directly on the semiconductor and/or by reaction with surface states associated with pre-adsorbed ambient oxygen, electronic transfer of delocalized conduction-band electrons to localized surface states and vice versa, catalytic effects and in general complex surface chemical reactions between the different adsorbed chemical species [43].

2.5.1 Sensing mechanism

It is generally accepted that ambient oxygen plays a fundamental role in the interactions on which is based the gas-sensing mechanism of metal oxide chemoresistors. As shown in Fig. 2.5, when O_2 molecules adsorb (chemisorption) on the surface of an n-type metal oxide, they would extract electrons from the conduction band and trap the electrons at the surface in the form of ions species: O_2^-, O^- or O^{2-} [3, 5, 6]. The negative charge accumulation on the surface causes a band bending and an electron depleted region (space-charge-layer), the thickness of which is the length of the band bending region. O^- is believed to be dominant at the temperature range of 300–450 °C, which corresponds to the operating temperature range for most metal oxide gas sensors [5]. The reaction of these oxygen species with reducing gases such as H_2, CH_4, CO, C_2H_5 H_2S, etc., or a competitive adsorption and replacement of the adsorbed oxygen by other molecules releases an electron to the bulk and decreases the bend bending and thickness of the depletion layer, resulting in an increased conductivity. In the presence of oxidizing gas

molecules, such as NO_2, Cl_2, etc., the inverse occurs: the number of adsorbed oxygen increases and thus the conductance decreases as it removes electrons.

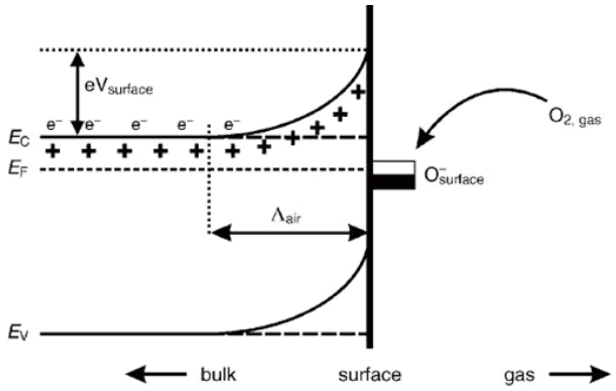

Figure 2.5 Diagram of band bending after chemisorption of charged species (here the ionosorption of oxygen) E_C, E_V, and E_F denote the energy of the conduction band, valence band, and the Fermi level, respectively, while Λ_{air} denotes the thickness of the space-charge layer, and $eV_{surface}$ denotes the potential barrier. Reproduced from [5].

Metal oxides of n- and p-type have inverse direction of conductivity changes for interaction with the same gases, which is a very important fact for their application [2, 7, 43, 44]. Table 2.4 summarizes the response of reducing and oxidizing gases on both types for semiconducting metal oxides.

Table 2.4 Signs of resistance change (increase or decrease) as a response to a change in gaseous atmosphere.

	n-type metal oxide	**p-type metal oxides**
Examples	MgO, CaO, TiO_2, ZrO_2, V_2O_5, Nb_2O_5, Ta_2O_5, MoO3, WO_3, ZnO, Al_2O_3, Ga_2O_3, In_2O_3, SnO_2	Y_2O_3, La_2O_3, CeO_2, Mn_2O_3, Co_3O_4, NiO, PdO, Ag_2O, Bi_2O_3, Sb2O3, TeO_2
Response to reducing gas	Resistance decreases with reducing gas	Resistance increases with reducing gases
Response to oxidizing gas	Resistance increases with oxidizing gases	Resistance decreases with oxidizing gases

N. Bârsan and U. Weimar have provided a frame model in Ref. [6] to describe phenomena involved in the detection process using a basic research approach to the greatest possible extent and dealing with all contributions to the conduction mechanism.

Depending on deposition techniques, compact layers or porous layers of metal oxide can be obtained. This is a fundamental distinction to make in order to describe phenomena behind metal oxide responses to gas. In compact layers, the interaction with gases is taking place only at the geometric surface. In porous layers, gases cannot penetrate into the sensitive layer and the gas interaction is taking place at the surface of individual grains, at grain-grain boundaries and at the interface between grains and electrodes. In the following, the latter contribution is neglected for simplicity purpose. For details see Ref. [6, 49].

In case of compact layers, depending on the ratio between layer thickness and Debye length λ_D, the metal oxide layer can be fully or partially depleted, as shown in Fig. 2.6. Partially depleted layers correspond to the case where the surface reaction with gas molecules does not influence the entire layer and thus the layer thickness is greater than the thickness of the depleted surface layer. Therefore the conduction process takes place in the bulk region (of thickness $Z_0 - Z_g$, much more conductive than the surface depleted layer). Formally two resistances occur in parallel, one influenced by surface reactions and the other not; the conduction is parallel to the surface, and this explains the limited sensitivity. In such a case, the influence of surface phenomena will consist in the modulation of the thickness of this conducting channel (conductive layer with a reaction-dependent thickness).

For the case of completely depleted layers in the absence of reducing gases, it is possible that exposure to reducing gases acts as a switch to the partly depleted layer case (due to the injection of additional free charge carriers). It is also possible that exposure to oxidizing gases acts as a switch between partly depleted and completely depleted layer cases.

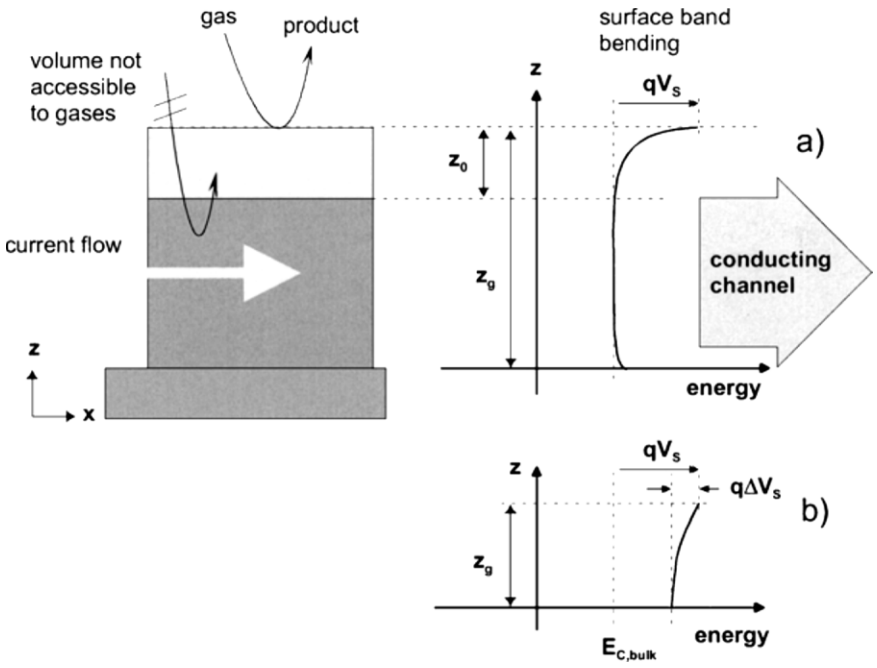

Figure 2.6 Schematic of a compact sensing layer with geometry and energy band diagrams; Z_0 is the thickness of the depleted surface layer; Z_g is the layer thickness and qV_s the band bending energy barrier height. a) Represents a partly depleted compact layer ("thicker"), and b) represents a completely depleted layer ("thinner"). Reproduced from [6].

In case of a porous layer, depending on the size grains and necks, we can distinguish three cases:

Case a) in this case the contact region between grains is large enough ($Z_n \gg \lambda_D$) to permit the existence of a region unaffected by surface phenomena (open necks Fig. 2.7.a). This case corresponds to large grains sintered with large necks (neck diameter is greater than depletion layer thickness) where the necks are partly depleted. Conduction in this case is similar to a compact layer thicker than λ_D.

Case b) in which the contact region between grains is large but entirely influenced by surface phenomena (closed necks, Fig. 2.7.b, Z_n comparable to λ_D). This case corresponds to large grains not sintered together, with necks fully depleted. The electron flow through grain boundaries has to deal with a potential barrier between grains. That means that the electrons passing from one grain to the other will face different values of the barrier height depending on their *z* position (see Fig. 2.7.b). One can treat this by considering an effective value of the potential barrier V_s, whose height is surface phenomena dependent, illustrated in Fig 2.8. The

response is therefore the result of the modulation of the height of the energy barrier qV_s, as illustrated in Fig 2.8.

Case c) in this case corresponds to small grains and small necks. The grains are fully depleted. The contact region between grains is small enough ($Z_n \ll \lambda_D$) so the charge carriers will see only one value of V_s when moving from one grain to the other, as shown in Fig. 2.8. It is also possible that exposure to oxidizing gases acts as a switch between partly depleted and completely depleted layer cases. For small grains and narrow necks, when the mean free path of free charge carriers becomes comparable to the dimension of the grains, a surface influence on mobility should be taken into consideration. This happens because the number of collisions experienced by the free charge carriers in the bulk of the grain becomes comparable to the number of surface collisions; the latter may be influenced by adsorbed species acting as additional scattering centres [6].

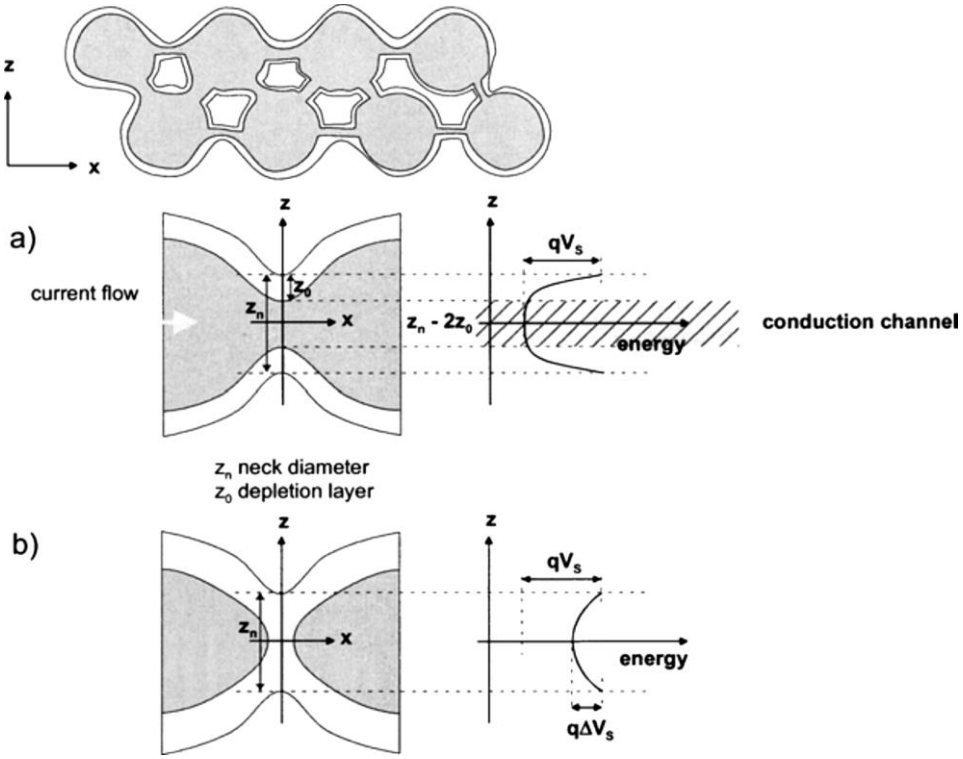

Figure 2.7 Schematic representation of a porous sensing layer with geometry and surface energy band-case with necks between grains. Z_n is the neck diameter; Z_0 is the thickness of the depletion layer. a) Represents the case of only partially depleted necks whereas b) represents large grains where the neck contact is completely depleted. Reproduced from [6].

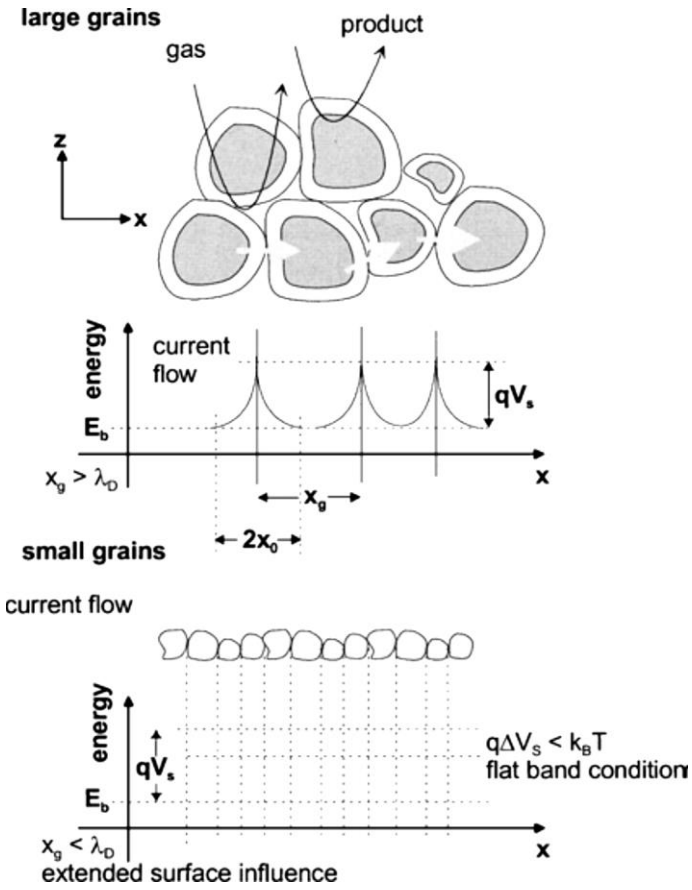

Figure 2.8 Schematic representation of a porous sensing layer with geometry and energy band. λ_D is the Debye length and X_g is the grain size. Reproduced from [6].

With respect to their conductivity, the most efficient gas sensors are those which are based on n-type metal oxides, such as SnO_2, TiO_2, WO_3, ZnO and In_2O_3, providing the opportunity of oxygen chemisorption [43]. In general, all n-oxides are known to be thermally stable and work at lower oxygen partial pressure in comparison to well-known p-type oxides. Interaction of n-type metal oxides with reducing gases is a decrease in resistance which is the preferred direction of resistance change for gas sensing. Many p-type oxides are relatively unstable because of the tendency to exchange lattice oxygen easily with air [43], which limits their use.

Sensor selectivity and sensitivity over a wide range can be tuned by varying the metal oxide microstructure (morphology, grain size and porosity), adding dopants (e.g., catalytic metals), varying operating temperature or heating mode (cycling heating or constant heating), etc. Metal oxide sensing layers are usually implemented as polycrystalline films.

2.5.2 Sensing influencing factors

Conductometric MOX gas sensors are one of the most extensively investigated groups of sensors. This type of sensor has been of great interest due to the flexibility and simplicity in fabrication and the broad range of target gases possible to detect.

A lot of effort has been made to enhance the sensitivity, and thus to decrease the detection limit, and to decrease the operating temperature. Investigated influencing factors have been mainly: chemical composition, surface modification or decoration –mainly with catalytic metals, such as Pd or Pt, microstructure (phase, surface morphology, grain size) and operating temperature. All these factors have been investigated to enhance the sensing reactions and to increase the available specific surface, and thus to increase the collected chemical signal.

2.5.2.a Microstructure

The microstructure properties involve surface morphology, shape and size of grains, crystallographic orientations, and porosity. All of these parameters have been found to strongly impact the sensitivity and the dynamics of the sensor (response and recovery times). Conductometric gas sensors prepared with amorphous state, glass-state, nanocrystalline state, polycrystalline state, and single crystal state MOX have been reported [43], in thin or thick layer, or as one-dimensional nanostructures [50]. However, in literature, nano- and polycrystalline materials have attracted much attention in the field of gas sensors [43].

Several reports have observed that the sensitivity of MOX resistors significantly increases when the grain size is decreased, as shown in Fig. 2.9. Lu *et al*. [8] have fabricated SnO_2gas sensors with different particle size from nanosized SnO_2 powder. The authors have observed that sensitivity of nanosized SnO_2 increases drastically with the reduction of particle size below 10 nm, and sensors with particle size of 8–10 nm could both respond and recover quickly. However sensors with particle size smaller than 20 nm, drift more or less. For instance, a sensor with 2 nm particle size had 40% drift during the 30-day test. It is due, first, to the increase of the specific surface by the decrease of grain size.

Second, for small grains with either narrow or large necks, when the grain size is comparable to the thickness of surface charge layer, the grain is fully depleted. Then exposure to reducing gases acts as a switch to the partially depleted grains. If these small grains are connected with

narrow necks, a double-Schottky barrier model or "neck" model can be applied [6], as detailed in the section 2.5.1. Also, in this case, the mean free path of free charge carriers becomes comparable to the dimension of the grains, so that a surface influence on mobility should be taken into consideration. This happens because the number of collisions experienced by the free charge carriers in the bulk of the grain becomes comparable to the number of surface collisions; the latter may be influenced by adsorbed species acting as additional scattering centres [6].

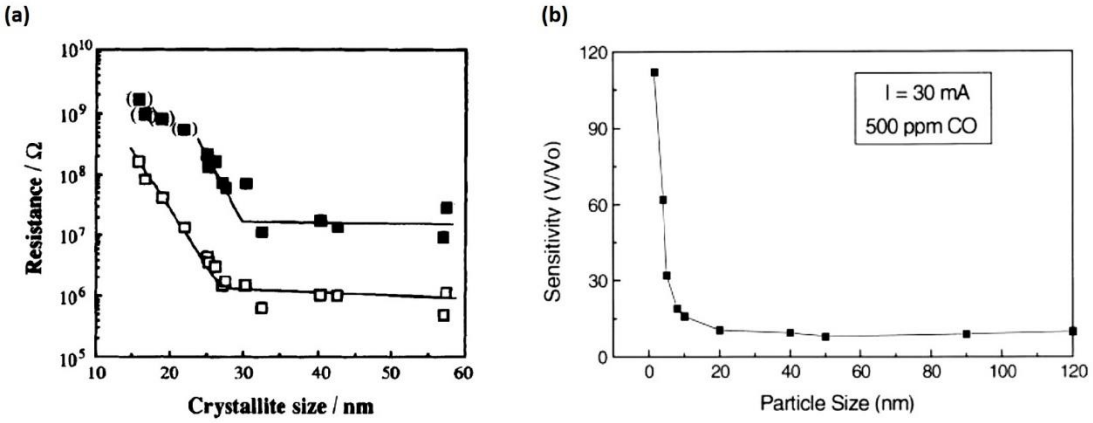

Figure 2.9 a) Resistance variation as a function of WO_3 crystallite size for; □ air and ■ 5ppm NO_2 at 300 °C. Reproduced from [7]. b) Sensitivity *versus* grain size of a SnO_2 nanocrystals-based sensor under exposure to 500 ppm. Reproduced from [8].

2.5.2.b Operating temperature

Commonly observed response *versus* operating temperature curve has a "bell" shape. The response increases and reaches their maxima at a certain temperature, and then decreases with increasing the temperature. Fig 2.10 and Fig. 2.11 present typical MOX resistor gas sensors responses with respect to operating temperature.

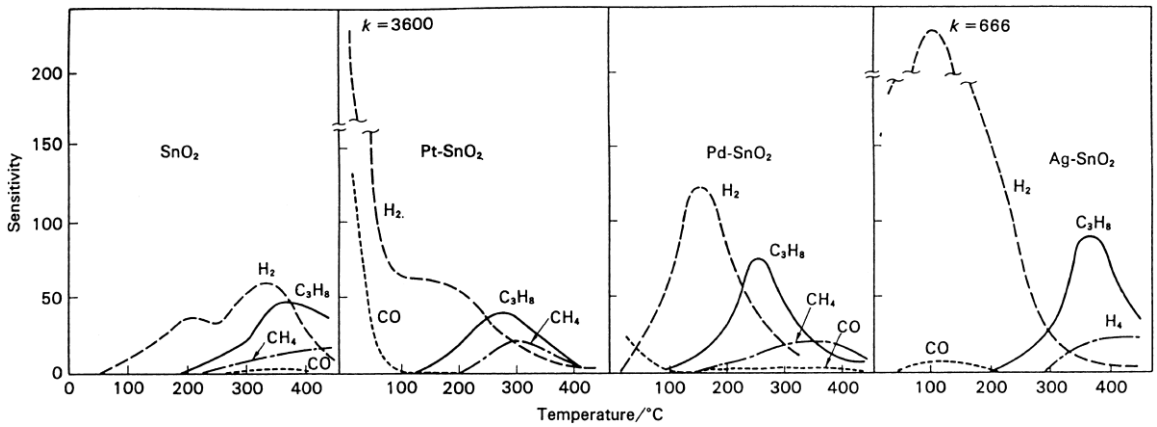

Figure 2.10 Sensitivity- temperature profile of chemoresistors with undoped, Pt-doped, Pd-doped and Ag-doped SnO_2 to 0.8% of H_2, 0.5% of CH_4 , 0.2% of C_3H_8 and 0.02% of CO in air. The sensitivity is defined as the ratio of sensor conductance in the presence of a target gas to the conductance in air (mixture of O_2 and N_2). Reproduced from [9].

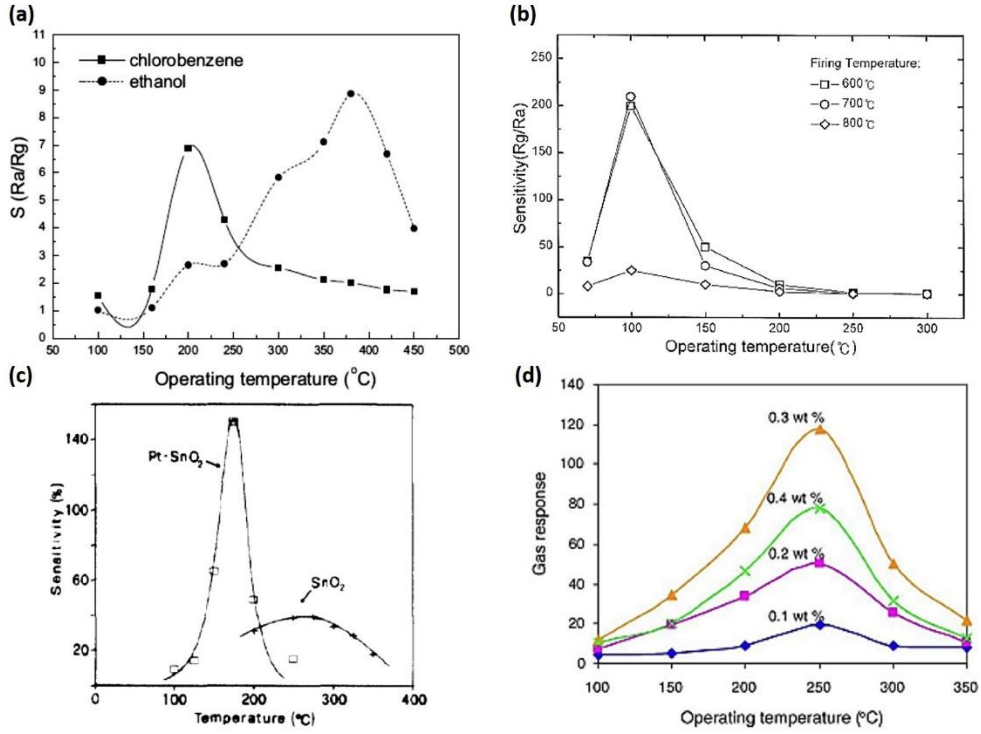

Figure 2.11 Sensitivity-operating temperature profile of a) ZnO nanoplate-based chemoresistor at 100 ppm of ethanol and chlorobenzene. Reproduced from [5]. b) Screen printed WO_3 thick layer resistor sintered at different temperatures at 100 ppm of NO_2.Reproduced from [10]. c) Undoped and Pt-doped SnO_2 thin layer chemoresistor at 180 ppm of CO. Reproduced from [11]. d) Screen printed ZnO thick film with different RuO_2 doping percentage. Reproduced from [7].

First heating is needed in MOX conductometric gas sensors to yield enough charge carrier density for reasonable conductance measurement. Then thermal energy is also required to activate grain boundary diffusion of gas species [42].

In addition, the sensitivity dependence on the operating temperature can be explained by the fact that the coverage rate (or chemisorption rate) $\frac{d\Theta}{dt}$ is determined by an activation barrier between a physisorbed state and the chemisorbed state and an activation barrier of desorption according to Lennard-Jones model. According to this model, the rate of chemisorption is expressed as follows [51]:

$$\frac{d\Theta}{dt} = K_{ads} \exp\left(-\frac{\Delta E_A}{K_b T}\right) - K_{des}\, \Theta \exp\left(-\frac{\Delta E_A + \Delta H_{chem}}{K_b T}\right) \quad (2.2)$$

where ΔE_A is the activation barrier that a physisorbed molecule has to overcome in order to reach the chemisorbed state, ΔH_{chem} is the heat of chemisorption, K_b is Boltzmann constant, and T is the temperature.

At equilibrium state: $\frac{d\Theta}{dt} = 0$, which means that the rate of adsorption is equal to the rate of desorption, and assuming that ΔH_{chem} is independent of the coverage, the coverage rate is then expressed as follows [51]:

$$\Theta = \frac{K_{ads}}{K_{des}} \exp\left(\frac{\Delta H_{chem}}{K_b T}\right) \quad (2.3)$$

Thus the coverage rate is dependent on temperature and the heat of chemisorption, which is a material-gas molecule specific quantity. Thus generally the coverage will decrease with increasing temperature. At low temperatures the molecules are, however, trapped in a physisorbed state and cannot overcome the activation barrier ΔE_A. This results in a maximum coverage at a certain optimal temperature. Heat of chemisorption ΔH_{chem} is a chemisorption form dependent. For instance, different chemisorbed oxygen forms (O_2^-, O^- and O^{2-}) have different ΔH_{chem}. Thereby, chemisorption of each adsorbed oxygen form has a different optimal temperature. N. Barsan and U. Weimar [6] provided a literature survey of oxygen species detected at different temperatures at SnO_2 surfaces with different chemical spectroscopy techniques, as it is shown in Fig 2.12. Oxygen can be ionosorbed in the molecular form of O^{2-}

or in the atomic form of O^- or O^{2-} (dissociative ionosorption). It has been proven by TPD (temperature programmed desorption), FTIR (Fourier transform infrared) analysis and EPR (electron paramagnetic resonance) that below 150 °C the molecular form dominates and above this temperature the ionic species dominate [6].

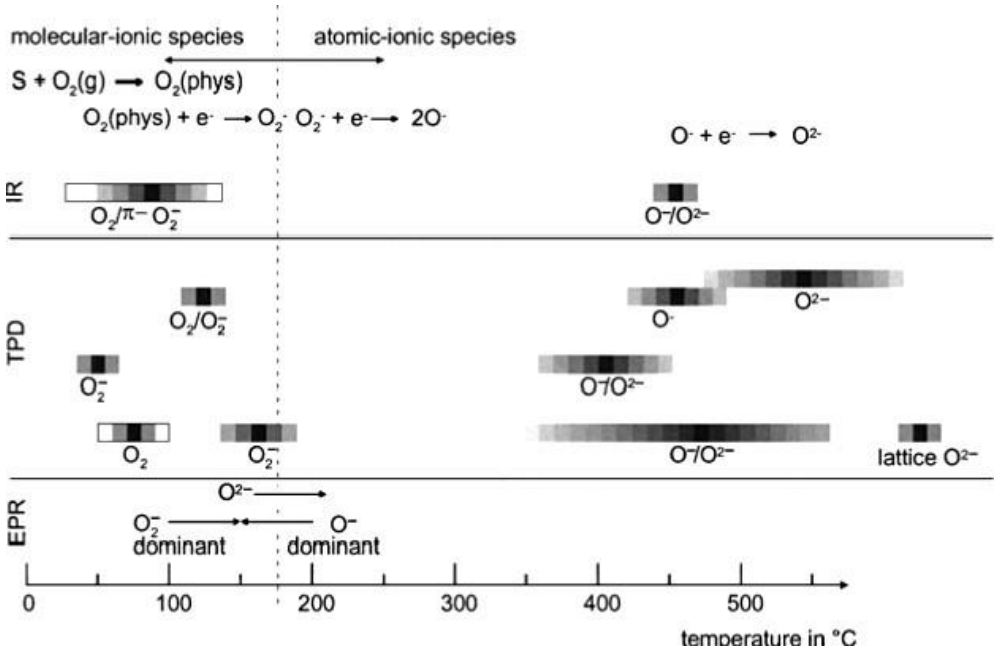

Figure 2.12 Literature survey of oxygen species detected at different temperatures at SnO2 surfaces with IR analysis, TPD and EPR (electron paramagnetic resonance). Reproduced from [6].

The sensing mechanism is ruled by the reaction of these oxygen species with reducing gases or a competitive adsorption and replacement of the adsorbed oxygen by other molecules as explained in the section 2.5.1. Therefore, depending on the involved in (or preferred) ionosorbed oxygen form for the sensing mechanism, the sensitivity will be strongly temperature dependant.

2.6 Field effect transistor-based gas sensors

One promising gas-sensing concept with high flexibility regarding sensing performances and materials is the detection via field effect transistors well suited for the measurement of potential variations. Both forms of gas molecules adsorption on solids, chemisorption run by ionic bonds and physisorption run by Van Der Walls interactions, induce modification of the surface charge and thus the surface potential. The effect is stronger in case of chemisorption compared to physisorption, since a charge exchange occurs and adsorbates are in a charged state. This leads

to a material work function variation (a surface potential variation) [12, 42] as explained in section 2.3. If the inner surface of the transistor gate is accessible to gas species, the induced voltage shift associated to the work function variation acts as an artificial voltage, which is added to an externally applied gate voltage and affects the conductance of the transistor channel [12, 42].

Overall, two different FETs have been used for this concept: MOSFETs and SG-FETs. In the former concept, the sensitive layer is the gate material itself. For the latter the gas sensitive layer is placed on the inner surface of suspended gate at a certain distance above the transistor channel. Both transducer concepts are illustrated in Fig 213. Historically MOSFET gas sensors have first introduced in 1975 [14]. Later, SG-FETs have been developed for gas detection.

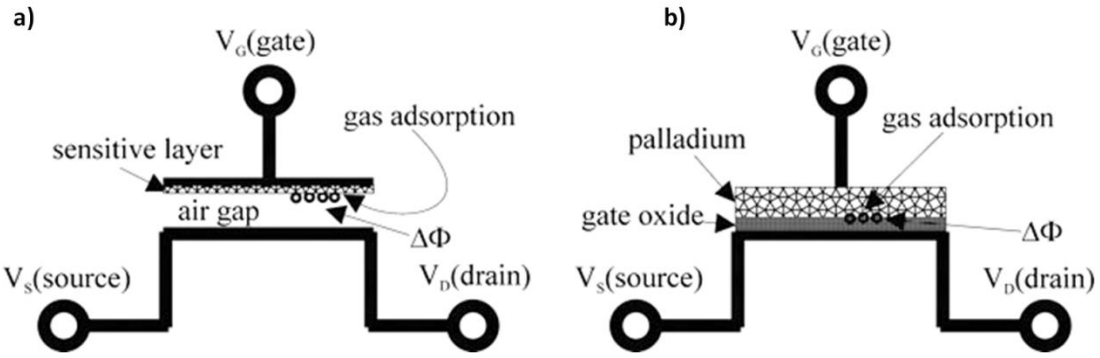

Figure 2.13 Schematic view of a) a SG-FET, b) a Pd-MOSFET. Reproduced from [12].

In principle, any gas adsorption leads to an individual work function. Therefore measurement of work function changes can be used as an indicator for the surface coverage of impinging gas species and their corresponding concentrations.

Therefore, for a successful sensor concept, it is necessary to develop a suitable surface for each specific gas.

2.6.1 MOSFET gas sensors (Catalytic MOSFETs)

MOSFET-based gas sensors, also referred to as catalytic MOSFETs or Lundström MOSFETs, are based on a conventional MOSFET where a catalytic metal, such as Pd, Pt or Ir, is usually used as a thin layer (sub-100 nm) to form the gate electrode [13, 52]. MOSFET-based gas

sensors are usually operated at a temperature in the range of 100°-200 °C [34, 35, 53]. Fig. 2.14 shows a cross-sectional structure of an n-channel MOSFET gas sensor.

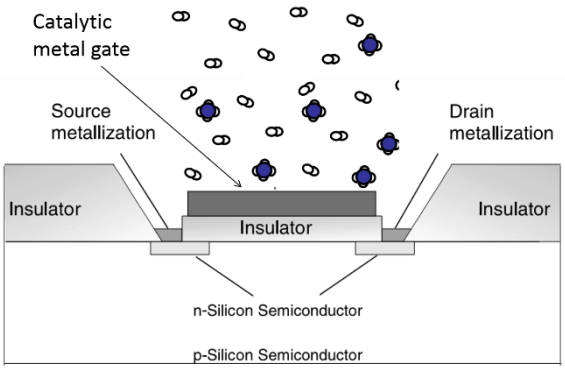

Figure 2.14 Cross sectional schematic of an n-channel MOSFET gas sensor structure with a catalytic metal gate electrode. Adapted from [13].

MOSFET as a gas sensor for H_2 was demonstrated first by Lundström *et al.* in 1975 [14, 54]. This group has demonstrated hydrogen sensitive Pd-MOSFET with detection capabilities down to 40 ppm of H_2 gas molecules in synthetic air (mixture of 20% oxygen and 80% nitrogen) with a response time of less than 2 min at 150 °C. The demonstrated device was an n-channel Si MOSFET with 10 nm-thick SiO_2 layer as a gate dielectric and 10 nm-thick e-beam evaporated Pd gate electrode. They reported a decrease in threshold voltage V_{th} in the presence of hydrogen and much a longer response time – for both "charging" and "relaxing"- at lower temperature. Fig. 2.15 shows the change in threshold voltage with time for two different H_2 concentrations at a temperature of 150 °C.

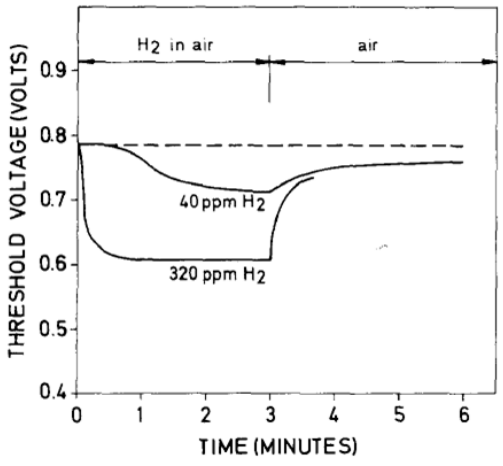

Figure 2.15 Change in threshold voltage with time in two different gas mixtures at a temperature of 150 °C. Reproduced from [14].

The proposed sensing mechanism is as follows: When the catalytic MOSFET gate is exposed to H_2, gas molecules adsorb by dissociative chemisorption on the outer gate metal surface, as shown in Fig. 2.16.b. Some of the atoms diffuse rapidly through the gate metal down to the inner metal surface and are trapped (adsorbed) at the metal/oxide interface, which gives rise to a local dipole layer in equilibrium with the outer layer of chemisorbed hydrogen and the gas phase [35]. The dipole layer induces a potential distribution in the structure, as illustrated in Fig.2.16.b. The induced voltage drop (or the potential shift) ΔV_i that appears at the interface is added to the externally applied voltage V_g, which results in an increase of the channel conductance and in consequence an increase in source-drain current I_{ds}. Thereby the I_{ds}-V_g curve is shifted towards lower voltages by ΔV_i (Fig. 2.16.a) [12, 53].

In other words, the generated dipole layer of adsorbed hydrogen atoms at the metal-gate oxide interface makes the work function of inner gate metal surface decreases by $\Delta\Phi$, and therefore changes the work-function difference between the metal and the semiconductor which results in a shift of the threshold voltage V_{th} of the MOS transistor [14, 55] by shifting the flatband voltage of the MOS structure.

The shift in the catalytic MOSFET I_{ds}-V_g curve, referred to as the threshold voltage shift ΔV_{th}, is the output signal.

In sensor configuration, the catalytic MOSFET is operated at constant source-drain current by applying a counter gate voltage, which constitutes the sensor signal (change in gate voltage required to keep the drain current constant at a pre-selected value) [12, 13, 53].

The potential shift ΔV_i is proportional to the number of hydrogen atoms absorbed per unit area at the metal/oxide interface, and is used to monitor the hydrogen concentration in the ambient environment [52]. When the hydrogen gas is not anymore present in the ambient, the hydrogen atoms at the metal-air interface recombine into molecules (or water if oxygen is present), and the metal/oxide interface, which is in equilibrium with the outer interface, is emptied. This shift in the I_{ds}-V_g curve is therefore reversible [35].

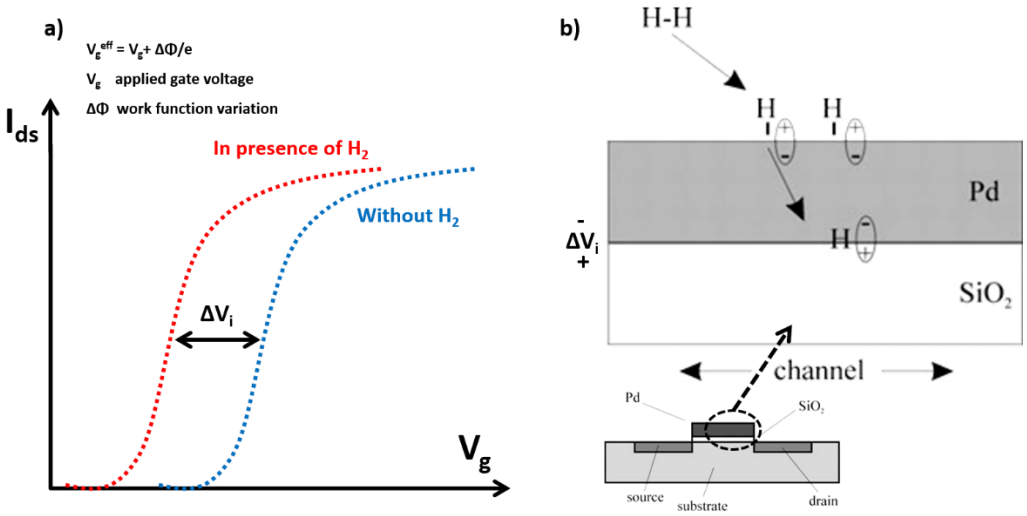

Figure 2.16 Transduction principle in catalytic MOSFET. a) I_{ds} *versus* V_g curve under and without exposure to H_2. b) Schematic illustrating the work function change of the inner Pd surface due to the trapped hydrogen atom at the Pd-SiO_2 interface.

In addition to H_2, the so-called Lundström MOSFETs were found sensitive to hydrogen containing gases, such as hydrogen sulphide [56], ethanol, acetone, ethylene [54] and ammonia [15, 35, 54], since they can be adsorbed and dehydrogenated on the surface of the catalytic metals mainly Pd, Pt and Ir, so that hydrogen atoms are released and diffuse through the metal layer, which acts as a hydrogen filter, to the metal/oxide interface. The detection limit for catalytic MOSFETs is generally about a few ppm.

It has been shown that the sensor sensitivity depends not only on the nature of the catalytic metal, but also on the structure of the metal film and the operating temperature [35, 54]. For instance, it has been observed that a thin layer of Pt on top of a Pd-gate increases the sensitivity towards ethanol at the time as it decreases the hydrogen sensitivity [54]. Large sensitivity toward ammonia has been achieved only when the catalytic metal gate is made so thin that it is porous. The sensing mechanism of porous catalytic metal films is detailed in [35, 54]. Brian *et al.* claimed that thin discontinuous Ir films have larger sensitivity toward H_2 and ammonia and reduced recovery time than thin discontinuous Pt film [35].

Lundström *et al.* have demonstrated the sensitivity towards molecules like hydrogen, ammonia, ethanol and ethylene using catalytic metal gates [54]. They discussed how the selectivity depends on the choice and structure of catalytic metals and the operating temperature.

MOSFET gas sensors are fabricated using standard silicon technology microelectronic processes on silicon. Both n and p channel MOSFETSs are used for gas sensing [13]. The gate material is removed and replaced by a catalytic metal film. Both thick (100–300 nm) and thin (3–30 nm) films have been used for the gate material [2].

It is also possible to tune the selectivity of a catalytic MOSFET, and therefore detect different molecules, by varying the operating temperature since target gas molecules have different optimal reacting temperatures. However, the operating temperature is limited by the silicon technology to a value not higher than 200–225 °C, due to leakage currents at p-n junctions increasing with temperature.

The catalytic gate requires high temperature and therefore to reduce the power consumption it is desirable to thermally isolate the sensor from the IC area. MOSFET gas sensors realized using a standard silicon processing have power consumption of about 0.5–1.0 W [15]. Much work has been carried out to reduce the power consumption of these devices. The main concept is to isolate the electronic components (sensor MOSFET, heating resistor, temperature sensor), on an insulating membrane using micromachining and thin film technology. This membrane can be formed by removing the silicon substrate using a variety of bulk-etching techniques. The membrane is usually formed by an insulating layer (thermal silicon oxide or silicon nitride) [57].

Briand *et al*. reported the fabrication of an array of four MOSFET gas sensors based on Si low power MOSFET with 8 nm-thick Pt, Pd or Ir gate electrode, for H_2 and ammonia sensing [15]. Using Silicon Bulk Micromachining, the MOSFET sensor, heating resistor and temperature sensor diode, as seen in Fig. 2.17, were fabricated within a silicon island isolated from the chip and suspended by a dielectric membrane formed by two deposited nitride layers (low pressure CVD and plasma enhanced CVD deposited). The thermal mass and, therefore, the power consumption of the sensor, are minimized by the design. The power consumption was lowered to 90 mW at an operating temperature of 170 °C.

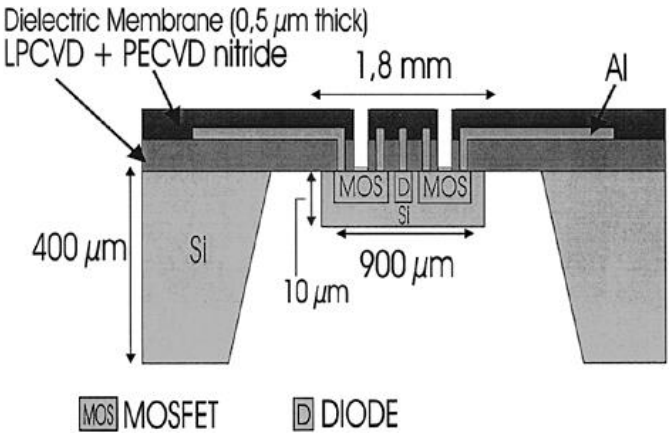

Figure 2.17 Schematic cross-sectional view of the low-power MOSFET array gas sensor. The electronic components are located in a silicon island isolated from the silicon chip frame by a dielectric membrane made of two nitride layers**.** Reproduced from [15]**.**

2.6.2 SG-FET-based gas sensors

The need of a permeable gate for target gas molecules has been a hard limitation of possibly detected gases for Lundström MOSFETs. In addition to a limited range of target gases, the required high operating temperature (above 100 °C) is one of the main limitations of this type of sensor.

Another promising gas sensing concept via FET devices is the use of SG-FET as a transducer. In principle, these devices can be used for the sensing of a wide range of gas species, and provide a real flexibility in integration of the sensitive layer.

As depicted in Fig. 2.18, SG-FETs are similar to MOSFETs, but have an air gap between the gate dielectric and the gate electrode. At the inner surface of the suspended gate, a gas sensitive layer is deposited. The target gas molecules diffuse through the air gap and adsorb on the surface of the sensitive layer. As previously explained, this induces a work function shift of the sensitive layer. The potential shift is added to applied gate voltage V_g, and consequently, the I_{ds}-V_g curve is shifted. The air gap height must be at least 1 µm, in order to keep gas diffusion to the sensitive layer fast enough [12].

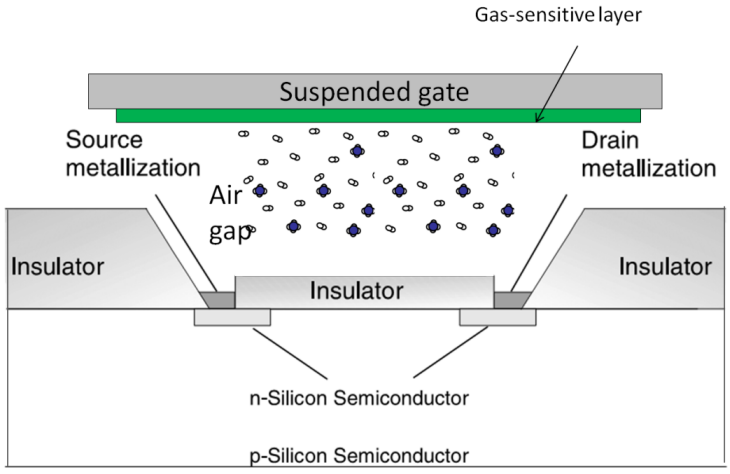

Figure 2.18 Cross sectional schematic of n-channel SGSFET gas sensor. Adapted from [13].

The main advantages of SG-FET gas sensors are room temperature (RT) operation or slightly above and a large choice of sensitive materials. The sensitive material has to be conductive or very thin. A wide range of sensitive materials have been demonstrated in combination with SG-FET such as: Pt [16], Ir oxide [32], etc. Table 2.5, reported from [12], shows some examples of sensitive materials deployed in a SG-FET gas sensor.

Table 2.5 Known combinations of detectable gas species and associated sensitive material integrated with a SG-FET. Reproduced from [12].

Sensitive material	**Target gas**
Platinum	H_2
Palladium	H_2
Titanium nitride	NH_3
Copper–phthalocyanine	NO, NO_2
Polysiloxanes	CO_2
Tin dioxide	CO, NO_2, O_3
Silver oxide	H_2S
Cobalt oxide	NO_2, NH_3
Chromium titanium oxide	H_2S, NH_3, Cl_2
Gold	Cl_2
Potassium iodide	O_3
Germanium	C_2H_5OH

The first SG-FET gas sensor was the monolithically integrated SG-FET, patented by Janata [45, 58]. Sensitive materials have been integrated by electrochemical deposition.

Later, Eisele *et al*. [59] have developed the Hybrid SG-FET (HSG-EFT). In contrast to the monolithic SG-FETs, a suspended gate electrode is mounted to a separated MOSFET transducer via flip-chip bonding. The hybrid design allows a wide spectrum of deposition techniques for the sensitive material since it is no longer dependent on the transistor fabrication.

Wilbertz *et al*. have integrated a Lundström MOSFET and a SG-FET gas sensors within the same chip [16]. The device is illustrated in Fig. 2.15.a. Pt and Pd were used as a sensitive material for the SG-FET and Lundström MOSFET respectively; and the response to H_2 of the paired sensor was investigated. While the Lundström -FET already gives a distinct response at a low H_2 concentration of 5 ppm, the SG-FET needs about one order of magnitude higher concentration for a clear signal, as it can be seen in Fig 2.15.b. However the two sensors give opposite response to CO (Fig 2.19.c). Thus the combination of both signals may be useful to reduce the cross sensitivity to interfering gases. At room temperature both devices demonstrate gas sensitivity and response times lying in the 10 s range. However at 100 °C response time is reduced to 1s in the case of Pd-MOSFET.

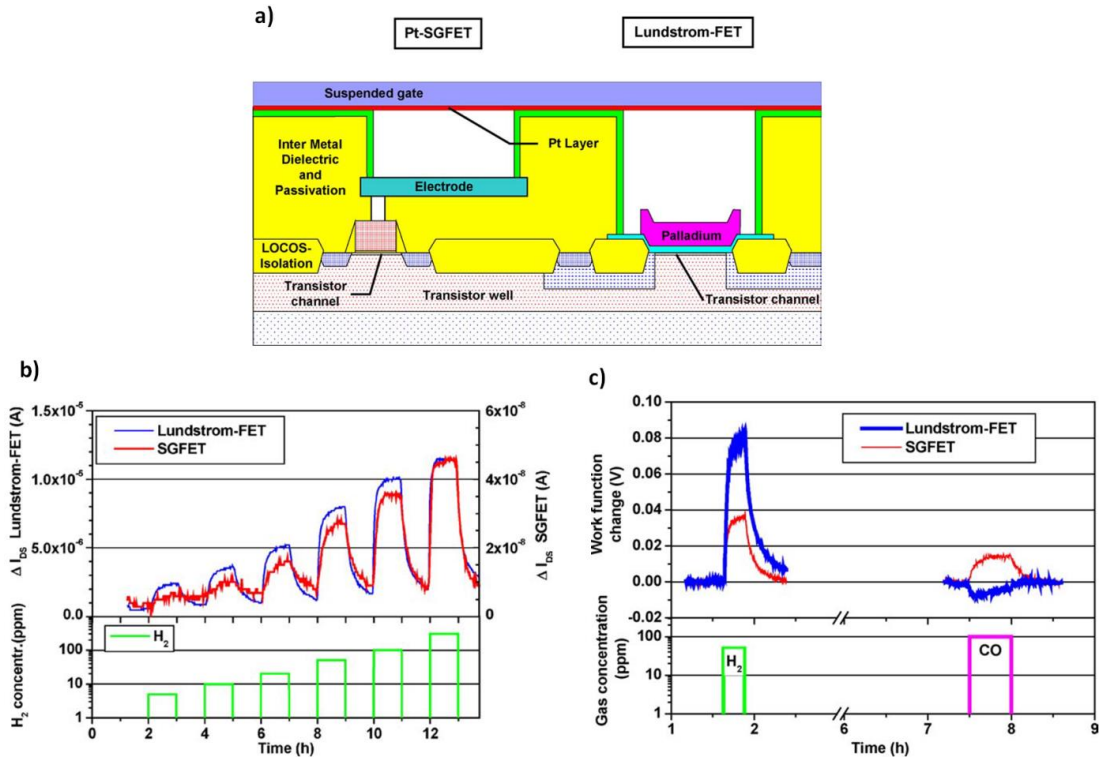

Figure 2.19 a) Schematic representation of Lundström -FET/SG-FET double sensor in CMOS technology. b) Different hydrogen sensitivity of Lundström -FET and SG-FET with Pt gate at low H_2 concentrations. c) Cross sensitivity of the double sensor system to a 100 ppm CO pulse, compared to the system's reaction to a 50 ppm hydrogen flow. Calibrated work function change at the sensing layer is shown. Reproduced from [16].

2.7 CNT and graphene-based gas sensors

Carbon nanotubes are one-dimension molecular-scale cylinder with high mechanical stiffness and strength. When they are in the form of a single walled-carbon nanotube (SW-CNT), they can be metallic, semiconducting, or semi-metallic, depending on their chirality [19]. Since their discovery in 1991, CNTs have attracted considerable interest for a broad range of applications (e.g., transistors, field emission devices and chemical sensors).

Recently, gas sensors based on graphene or CNTs have been demonstrated with an impressive sensitivity compared to existing technologies. As observed in the literature, CNT-based sensors clearly show the most sensitive sensors in the range of few ppb (parts per billion) to a few tens of ppm. Many studies have been carried out on CNT-based gas sensors for the sensing of gases such as H_2, CH_4, CO, H_2S and some VOCs. The research has essentially focused on CNT-FETs as gas sensors with individual SW-CNTs.

The main advantages for CNT-FET-based gas sensors, compared to existing technologies, are room temperature operation with low power consumption, fast response and recovery time and sensitivity to very low concentration down to the ppb range. Meanwhile, the physical interpretation of sensing mechanism has not been yet clarified and is still controversial.

One of the reasons for unreached detection resolution of individual atoms or molecules by any detection technique is the fluctuations due to thermal motion of charges and defects, which lead to intrinsic noise exceeding the sought-after signal from individual molecules, usually by orders of magnitude.

Graphene has been reported to be a strictly two-dimensional material highly conductive and with low Johnson noise. It also has few defects, which ensures a low level of 1/f noise caused by their thermal switching. In addition, graphene allows metal contacts that are ohmic and with low resistance. All of these features maximize the signal-to-noise ratio to a level sufficient for detecting changes in a local concentration by less than one electron charge at room temperature and makes it a promising candidate for chemical sensors.

Schedin *et al.* [17] have investigated the capability of graphene devices to detect gas molecules. The device was elaborated by micromechanical cleavage of graphene on an oxidized Si substrate and e-beam Lithography to define Au/Ti contacts. Sensitivity to NO_2, NH_3, H_2O and CO gas

molecules diluted in N_2 was reported in concentration of 1 ppm. Large detectable change in resistivity has been observed, as seen in Fig. 2.20, immediately for NO_2 and within 1 min of exposure for the other gases. They performed Hall measurements, which revealed that NO_2 and H_2O act as acceptors and NH_3 and CO as donors. The same measurements have allowed the estimation of charge carrier concentration variation (Δn) which was found to linearly depend on the concentration of an examined chemical.

Although chemical doping by gas molecules adsorption induced impurities in graphene in concentrations $N_i = \Delta n$, Schedin *et al.* have found that these extra scatterers do not induce a notable changes in the mobility even for N_i exceeding 10^{12} cm^{-2}.

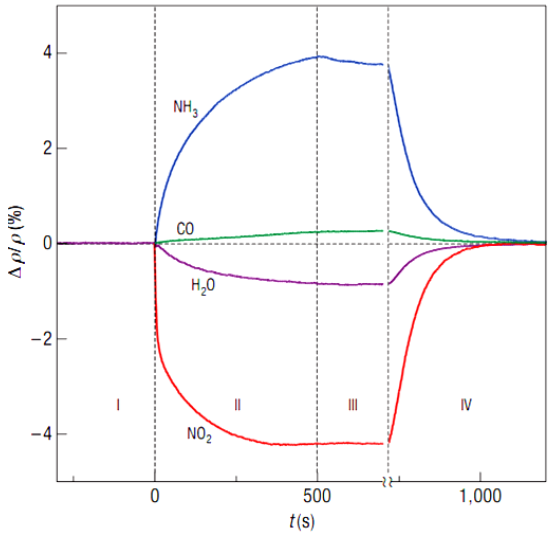

Figure 2.20 Changes in resistivity caused by graphene exposure to various gases diluted in concentration to 1 ppm. The positive (negative) sign of changes is chosen here to indicate electron (hole) doping. Region I: the device is in a vacuum before its exposure; II: exposure to a 5 l volume of a diluted chemical; III: evacuation of the experimental set-up; and IV: annealing at 150 °C. Reproduced from [17].

Typical CNT-FET-based gas sensors are designed as follows. CVD grown CNTs are contacted to drain and source metal contacts on a Si substrate with a dielectric layer on top. A schematic of a typical device is shown in Fig. 2.21. The Si substrate is used as a back gate.

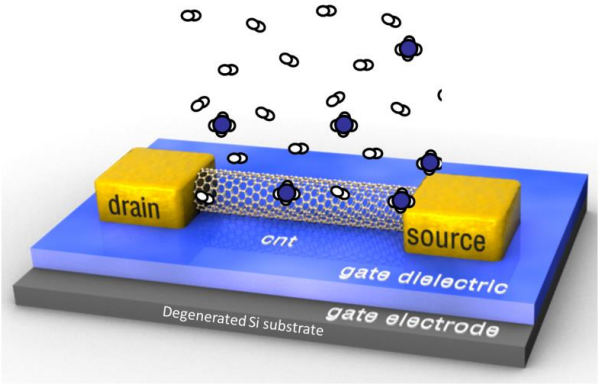

Figure 2.21 Schematic of a typical CNT-FET structure. The Si substrate acts as a back gate. Adapted from [18].

Kong *et al.* [19] demonstrated the first gas sensor based on CNT elaborated by a CVD growth technique, in 2000. They reported the realization of individual semiconducting SW-CNT (S-SW-CNT) FET-based chemical sensors capable of detecting small concentrations of NO_2 or NH_3 gas molecules. Reported S-SW-CNT devices were found to behave as p-channel MOSFET, as seen in Fig. 2.22. These S-SW-CNTs are p-type semiconductors and present substantial hole charge carriers. After exposure to gas molecules, the conductance of these devices exhibited 100 fold decrease for NH_3 gas with time response of 1 to 2 min (measurement for 1% concentration of NH_3 at $V_g = 0$ V) and 3 orders of magnitude increase for NO_2 gas with response time in the range of 2 to 10 s (measurement for 200 ppm concentration of NO_2 at $V_g = +4$ V). I_{ds} -V_g curves of these devices, recorded before and after exposure for the same device and successively after sample recovery by heating, are shown in Fig 2.22, where a shift of -4V is observed upon exposure to NH_3 and a shift of +4V upon exposure to NO_2.

The adsorption of NH_3 was found to induce a hole depletion which reduced the conductance. In contrast, adsorption of NO_2 caused enriched hole carriers in the CNT, which enhanced its conductance. These results showed that upon adsorption of NO_2, a charge transfer is likely to occur from the S-SW-CNT to NO_2 because of the electron-withdrawing of the NO_2 molecules. In contrast, NH_3, which is a Lewis base, is found to be a donor. This effect has been assimilated to a sort of "molecular gating" of the carbon nanotube, due to the gas molecules adsorption [60].

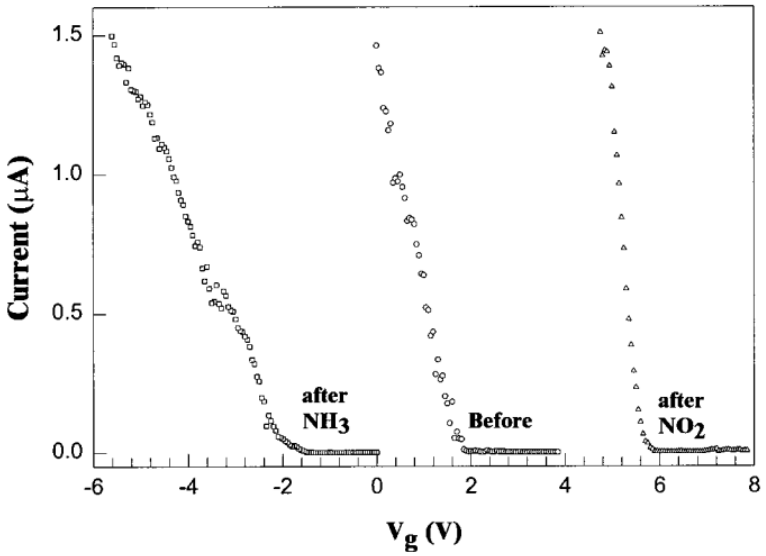

Figure 2.22 Chemical gating effects to the semiconducting SWNT. Current *versus* gate voltage curves before NO_2, after NO_2 and after NH_3 exposures. The measurements were carried out successively after sample recovery and with exposure to NH_3 (0.1–1%) and NO_2 (2–200 ppm) in an air flow rate of 700 ml/min. The channel length was around 5μm. Reproduced from [19].

Liu *et al*. [20] investigated the response of a single SW-CNT as CNT-FET channel, exposed to concentrations varying from 0 to 4 ppm of NO_2 and from 0 to 400 ppm of NH_3, covering alternatively the metal/SW-CNT contacts and the centre of the channel, with poly(methyl methacrylate) (PMMA) resist, as illustrated in Fig. 2.23. They revealed that NO_2 shifts the threshold voltage positively, while NH_3 shifts it negatively for both centre-exposed and contact-exposed devices (Fig. 2.24).

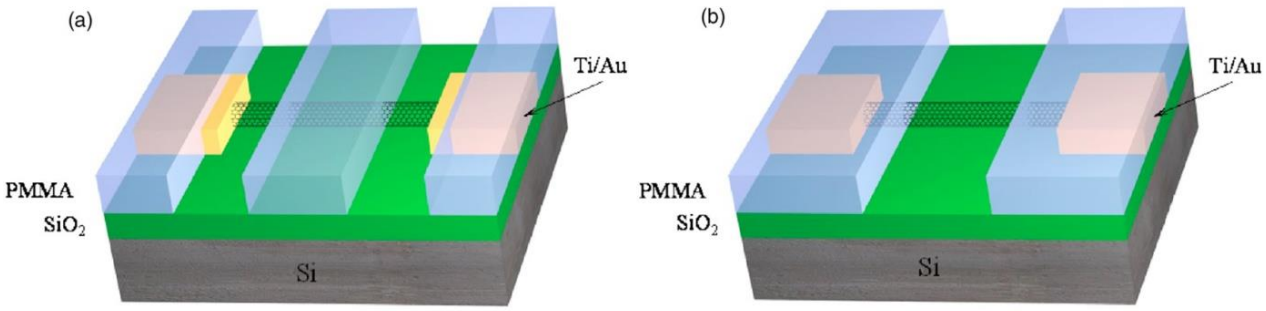

Figure 2.23 Schematics of the two CNT-FET structures used by Liu *et al*.. (a) Contact exposed device. (b) Centre exposed device. Reproduced from [20].

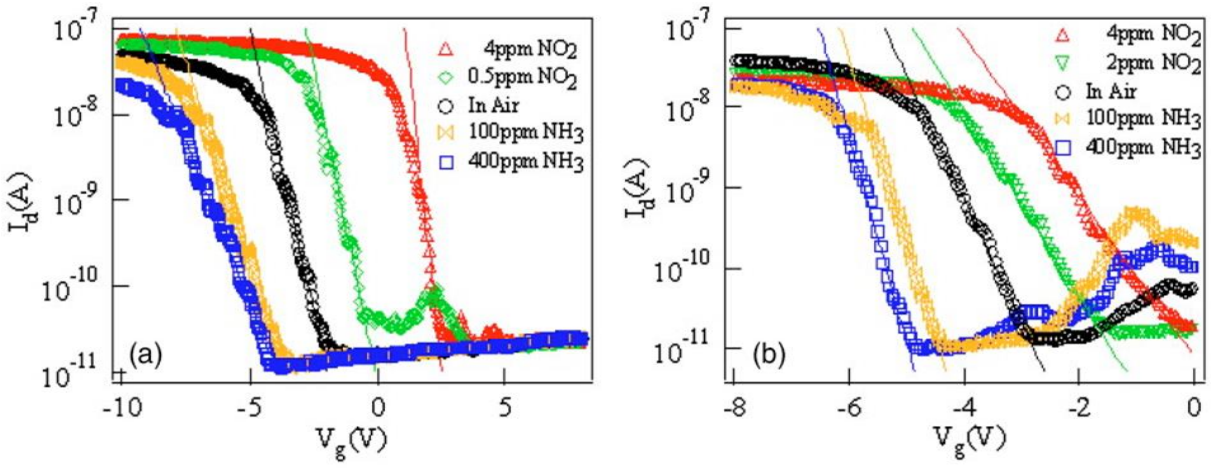

Figure 2.24 I_{ds}-V_g curves of a) a contact-exposed device and b) a centre-exposed device under exposure to different concentrations of NO_2 and NH_3. Reproduced from [20].

Several scientific teams have focused their studies on finding whether the response signals of CNT-FETs gas sensors result from charge transfer between adsorbed gas molecules and the body of the CNT or/and from the gas species induced Schottky barrier modulation at the CNT/metal contacts.

Using passivated and non-passivated CNT/metal contacts with thermally evaporated SiO_2, Bradley *et al*. [61] have investigated the mechanism behind the sensitivity of CNT-FETs to NH_3 gas. They found a good sensitivity to NH_3 and suggested that sensing occurs through charge-transfer doping of the CNT channel rather than through modifying Schottky barrier induced by the interaction between gas species with the metal/CNT interface.

In contrast to results by Liu *et al*. [20] who have employed PMMA as a passivation layer and observed changes in the transfer characteristics upon exposure to NH_3 and NO_2 for both contact-passivated and channel-passivated devices, Zhang *et al*. [62] reported that when PMMA was applied to protect the CNT/metal contacts from NO_2 exposure, their devices became insensitive after contact passivation. They argued that when the passivation length was comparable to the depletion length in the CNT, the contacts could be indirectly affected.

The obvious ambiguity in those reports could arise from the permeable passivation materials used. Moreover, as the experiments were carried out at room temperature and air ambient only, exclusive identification of the sensing mechanisms is not possible.

To differentiate the sensing mechanisms, Peng *et al*. [63] have employed three CNT-FET structures: (i) the entire CNT channel and CNT/electrode contacts are accessible to NH_3 gas (ii) the CNT/electrode contacts are passivated with a Si_3N_4 thin film, leaving the CNT channel open to the gas and (ii) the CNT channel is covered with the film, while the contacts are open to the gas. They suggest that the Schottky barrier modulation at the contacts is the dominant mechanism from room temperature to 150 °C. At higher temperatures, the charge transfer process contributes to the response signals.

CNT-FET-based CO_2 sensors have been reported by Star *et al.* [64]. Specific sensitivity to CO_2 has been achieved by employing recognition layers that induce chemical reactions that modify the CNT-FET device characteristics. This group has used a mixture of poly(-ethyleneimine) (PEI) and starch polymers as a CO_2 selective recognition layer, coating the CNT channel. The mechanism of sensing involves adsorption of CO_2 molecules in the coating polymer and chemical reactions between the CO_2 molecules with primary and secondary amino groups which lower the pH of the polymer layer and alter the charge transfer to the CNT channel. The response to CO_2 gas was fast and reproducible over a wide range of concentration from 500 ppm to 10% in air.

2.8 Single electron transistor-based gas sensor

Until now, only one group from the Michigan Technological University has demonstrated a SET-based gas sensor. Karre *et al*. [21] have demonstrated the possibility of NO_2 sensing using SET devices as a sensitive electrometer at room temperature. The reported device is a multiple island SET, where the gate pad was used as the sensing element. The device was fabricated over a silicon substrate with 300 nm-thick Al_2O_3 layer on top. Tungsten 10 nm nanoparticles - as islands - were deposited randomly followed by the fabrication of W gate drain and source connecting leads and pads by focused ion beam (FIB) deposition. Then nano-islands and leads were oxidized in paracetic acid (combination of H_2O_2 and acetic acid). Approximately 10 conducting islands were formed between the source and drain terminals. A 30nm-thick passivating Al_2O_3 layer was deposited over the device to isolate and stabilize the tunnel junction behaviour of the device. The passivating oxide was removed from the pad regions by FIB etching.

The sensing characteristics of the device were investigated by varying the concentration of NO_2 in N_2 gas from 36% to 100% at atmospheric pressure. Under exposure to 41% concentration NO_2 gas, the drain current decreased by an order of magnitude. Different concentrations of the NO_2 resulted in variation of the decrease in the source-drain current I_{ds}. The lowest concentration of NO_2 that was detected with this device was 36%. Fig 2.25.a shows variations in the I_{ds} current that occurred under switching the NO_2 gas injection in the flow cell. The I_{ds} current relaxes to the base value after decreasing which results in a peak.

Karre *et al.* reported that ionosorption of NO_2 molecules to native W oxide (WO) present at the top surface of the gate electrode (exposed gate pad to gas flow), illustrated in Fig. 2.26, is behind the observed response of the device. The presence of gas molecules on the gate electrode surface will modulate charges available on the gate terminal, acting as an additional bias, which affects the tunnelling characteristics.

Electron transfer can be from or to the gate terminal depending on the incoming gas molecules and surface states. Electron transfer to the gate induces a negative bias (potential) on the gate proportional to the number of gas molecules adsorbed to the gate terminal and *vice versa.* The adsorption of NO_2 molecules corresponds to an electron transfer. The gas molecules adsorbed on the gate terminal create extra charges proportional to the number of gas molecules adsorbed and thus modulating the tunnelling properties.

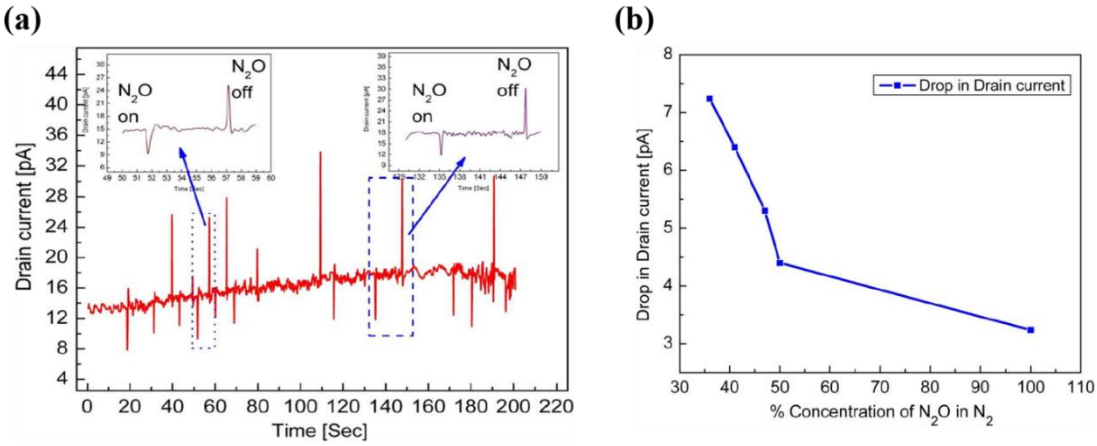

Figure 2.25 a) Time response of SET-based gas sensor to the injection of the mixture of gases into the flow cell. The NO_2 concentration is 41% in N_2. b) Variation of the drop in drain current in function of concentration of NO_2 in N_2. Reproduced from [21].

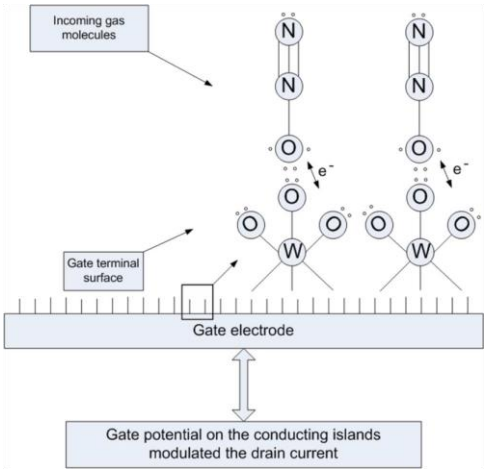

Figure 2.26 Proposed ionosorption mechanism resulting in charge transfer in the SET gas sensor. Reproduced from [21].

The reduction in the drain current of the SET device decreases with the increase in the concentration of gas. For lower concentrations of the sensing species, the SET device is more sensitive and for higher concentrations the sensitivity of the SET sensor decreases, as shown in Fig. 2.25.b. [21].

2.9 Conclusion

In MOX resistor gas sensors heating is needed to yield enough charge carrier density for reasonable conductance measurement, and to activate grain boundary diffusion of gas species. Moreover, this type of sensor is sensitive only to chemisorbed species, whom optimum temperature is usually at very elevated temperature.

The high operating temperature of MOX resistors is the main limitation toward integration with CMOS in a SoC. First it is incompatible with CMOS transistor operation. Second, from a power consumption point of view, these devices are incompatible with a battery powered mobile systems. A lot of efforts have been made to decrease the power consumption by integrating the sensors within a suspended membrane isolated from the substrate in order to decrease thermal mass. One dimensional nanostructured MOX have attracted a lot of interest in recent years because of their high surface-to-volume ratio as well as their good thermal stability and tunable surface state and texture. A broad range of nanostructured MOX resistors such as nanowires, nanofibers, nanorods, nanobelts, etc., have been reported. A complete review of the mechanism and the performances of this type of sensors can be found in [50]. The main aim of

nanostructuring the sensing material is to decrease the operating temperature by increasing the "chemical signal" and thus improving the signal-to-noise ratio.

SG-FET gas sensors have been demonstrated at RT or slightly above thanks to their sensitivity to both of chemisorbed and physisorbed species. The latter have their optimum at low temperature. In addition, the transistor gain improves the sensitivity and compensate for the lack of the "chemical signal" at low temperature. In hybrid SG-FET, the sensing layer could be very large, thus increasing the collected chemical signal. CNT-FET-based gas sensors, have shown a very promising capability of sensing to achieve very sensitive sensors operated at RT. However, from a fabrication point of view, the CNT assembly and alignment technique are not yet compatible with mass production IC technology, or do not yield reproducible results.

Up to now, only one demonstration of a SET as a gas sensor has been reported. The very limited amount of experimental data and the proposed sensing mechanism raise more questions than give clear demonstration about the sensing mechanisms. For example, the current relaxation to its base value after decreasing as a response to N_2O presence is not yet understood. In that perspective there is still a lot to be done in gas sensing using SET transducers.

CHAPTER 3 Device design, modelling and simulation

3.1 Introduction

For appropriate geometry design and sizing, device modelling and numerical simulations are needed. The goal of simulation is to estimate the expected sensor sensitivity, sensitivity range, and detection limit. The latter is strongly dependent on the transducer signal-to-noise ratio.

SET current-voltage characteristics are very dependent on the island capacitances. From a design point of view, placing four electrodes close to the island with minimum parasitic capacitances, while keeping the island total capacitance below the limit for room temperature operations, is very challenging and needs prior calculations and optimization. Therefore the impact of functionalized gate geometrical parameters on the different device capacitances has been studied. Sensor response simulation also allows optimization of drain to source polarization voltage with regard to device performance, especially in terms of power consumption.

FD-SOI FETs are very promising candidates for gas sensing applications because they allow the channel gating by two separate gates: the front gate and the substrate bulk Si. In addition, their amplification capability when operated in the sub-threshold regime as well as low drive current is very interesting for sensing applications. Moreover, the small size of these devices is also of a high interest in terms of integration density.

In this chapter, a brief background on the Coulomb blockade effect and single electron transistors is first presented. An overview of the Orthodox theory, which is the background theory for most single electronics simulators, is then given. Afterwards, the concept of double-gate transistor-based gas sensors is introduced. DG-SET capacitance optimization as well as their impact on the SET operation is discussed. DG-SET-based sensor sensitivity in terms of the current variation per charge change is estimated. Then, the concept of a DG-FET is introduced. The sensitivity of a DG-FET-based gas sensor using a FD-SOI MOSFET is estimated using a compact analytical model. The impacts of the substrate bias, channel dimensions and temperature have been studied.

3.2 SET theory

Single electron devices, such as SETs, operation principle is based on single electron charging effects, also known as Coulomb blockade effect. Single-electron charging effects provide a means to control the transfer of electrons between small conducting structures at the level of one electron [38, 65]. These effects are observed only under some conditions detailed below. In the following the concept of single electron phenomena and Coulomb blockade effect are explained by referring to single-island, double tunnel junction system. The SET operation principle is then presented and detailed. A brief overview of the *Orthodox theory* is given afterwards.

3.2.1 Coulomb blockade effect

To understand the theory behind the SET operation principle, first the Coulomb blockade principle has to be introduced. We consider a nanoscaled metallic structure, referred to as *the island*, placed very close to two other metallic electrodes referred to as *drain* and *source*, as illustrated in Fig. 3.1. The gaps between the island and the two metallic electrodes are filled with a dielectric, and are so thin that they form leaky capacitors. That means that the island is connected to the two terminals through tunnel junctions. This forms what is known as the single-island, double tunnel junction system [65]. We assume that the island has a null net charge, when both electrodes are grounded. For the following we assume that if a bias is applied to an electrode with the other being considered as voltage reference, electrons can only flow from or to the island by tunnelling effect.

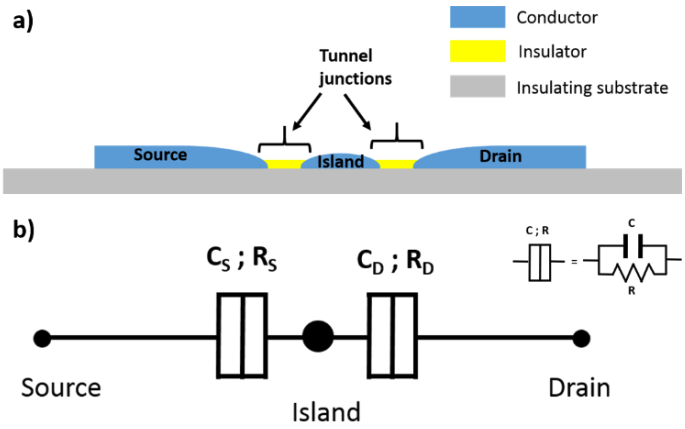

Figure 3.1 The single-island, double tunnel junction system. a) Schematic structure of single-island, double tunnel junction system showing an isolated nano-sized metallic island placed close to two metallic electrodes: drain and source. b) Circuit diagram of a single-island, double tunnel junction system. C_S and R_S are respectively island-to-source tunnel junction capacitance and resistance. C_D and R_D are respectively island-to-drain capacitance and resistance.

Let us assume that a single electron is transferred to the island so that it has a net electric charge equal to – e, where $e \approx 1.6\ 10^{-19}$ C is the elementary charge. If the potential difference between drain and source V_{DS} is null (e.g. drain and source are electrically connected), equivalent positive charges, q_1 and q_2 are accumulated at respectively source and drain electrodes, as depicted in Fig. 3.2.a as a result of neutrality principle, with $q_1 + q_2 - e = 0$. Similarly, if an electron is withdrawn from the island, compensating negative charges appear at these terminals.

The system is equivalent to a capacitor with a total capacitance C_Σ equivalent to the two tunnel junction capacitors in parallel, as shown in Fig. 3.2.b ($C_\Sigma = C_D + C_S$, where C_D and C_S are respectively island-to-drain and island-to-source capacitances). The electrostatic energy U stored in the system equals:

$$U = \frac{e^2}{2\ C_\Sigma} \qquad (3.1)$$

This energy stands as an electrostatic energy barrier toward adding another electron/withdrawing an electron to/from the island initially. This quantity is known as the charging energy of a single electron and noted E_c [65]. For $V_{DS} = 0$ V, no more charge can tunnel onto the island because of this electrostatic energy barrier.

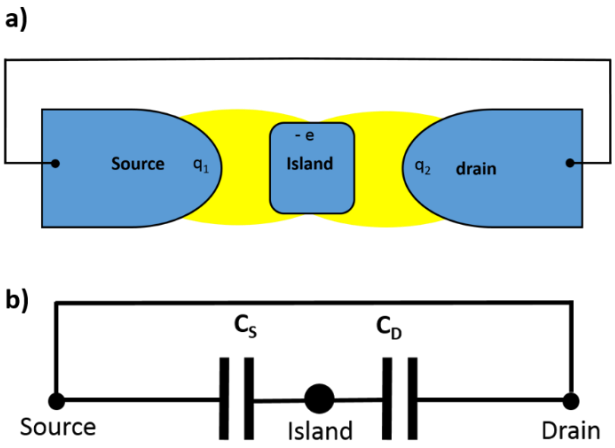

Figure 3.2 a) Schematic representation of the single-island, double tunnel junction system with drain and source electrically connected. b) Circuit diagram of the single-island, double tunnel junction system with drain and source electrically connected.

If a voltage is applied to drain with respect to the source, as illustrated in Fig. 3.3, so that potential difference $V_{DS} > 0$, a potential difference between the intermediate island and each of the two electrodes is created. The electrostatic energy barrier seen by an electron reaching the island from the source is then:

$$\Delta E_{S\to I} = \frac{e^2}{2\,C_\Sigma} - e\,\frac{C_D}{C_\Sigma}\,V_{DS} \tag{3.2}$$

and the electrostatic energy barrier seen by an electron leaving the island to the drain is:

$$\Delta E_{I\to D} = \frac{e^2}{2\,C_\Sigma} - e\,\frac{C_S}{C_\Sigma}\,V_{DS} \tag{3.3}$$

One can notice through the terms $-e\,\frac{C_D}{C_\Sigma}\,V_{DS}$ and $-e\,\frac{C_S}{C_\Sigma}\,V_{DS}$ that the applied voltage V_{DS} is lowering the electrostatic energy barrier seen by an electron flowing from source to island or from island to drain. For a small positive value of V_{DS}, the potential difference between the higher energy source electrode and the island is not enough to overcome the energy barrier $\frac{e^2}{2\,C_\Sigma}$. Therefore, electrons on this electrode cannot tunnel onto the island. However, if V_{DS} is increased such that $\frac{e^2}{2\,C_\Sigma}$ is overcome, an electron can tunnel onto the island. Then this electron can tunnel

off the island to the lower energy positively biased drain electrode. Another electron can then tunnel immediately onto the island, repeating the process. A current begins then to flow across the system. This effect is known as the Coulomb blockade. Note that the Coulomb blockade prevents from adding more than one electron to the island at once. Because once the electron reaches the island the electrostatic energy is increased by $\frac{e^2}{2\,C_\Sigma}$. The island net charge is increased only by one electron. The current flow is produced by "a caravan" of electrons charging and discharging subsequently the island one after the other. Eq. 3.2 and Eq. 3.3, show that the current I_{DS} begins to flow for:

$$|V_{DS}| \geq V_C = \min\left(\frac{e}{2C_S}; \frac{e}{2C_D}\right) \tag{3.4}$$

If V_{DS} is increased enough to overcome the electrostatic barrier of $2 \times \frac{e^2}{2\,C_\Sigma}$, then a second electron can tunnel into the island and on average, the island is charged by two extra electrons. With further increase in V_{DS}, the number of electrons charging the island increases one-by-one. We recall that the island average charge Q is non-continuous but rather discrete with only values of $N \times e$, where N is an integer. The electrostatic energy is increased by $\frac{e^2}{2\,C_\Sigma}$ per additional single electron charging the island. Therefore allowed energy levels in the island are then discrete levels linearly spaced by a constant gap $\frac{e^2}{C_\Sigma}$, as illustrated in Fig. 3.4.

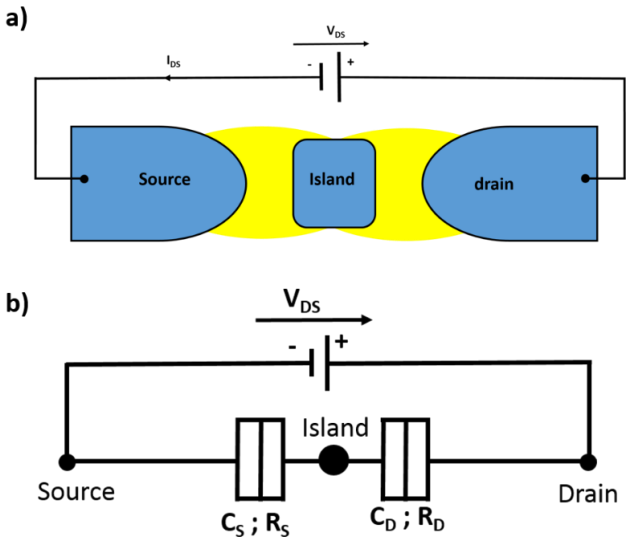

Figure 3.3 a) Schematic representation of the single-island, double tunnel junction system where a voltage V_{DS} is applied between drain and source. b) Circuit diagram of the single-island, double tunnel junction system where a voltage V_{DS} is applied between source and drain.

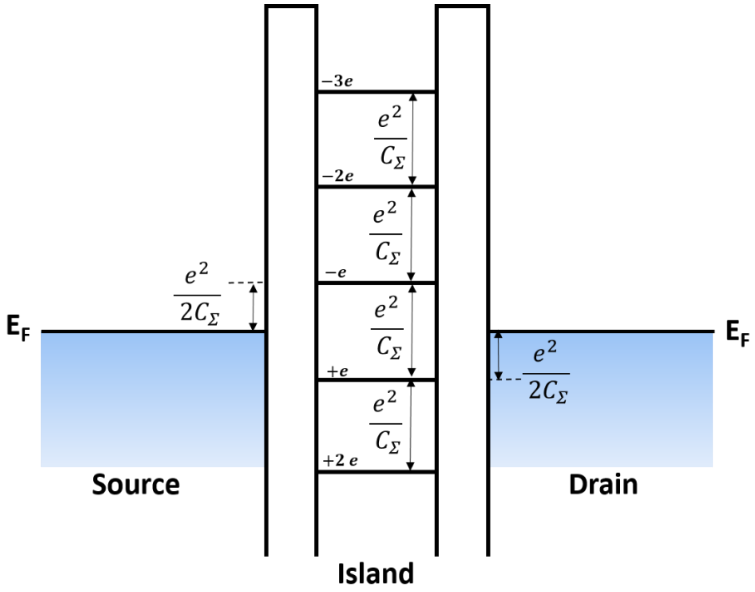

Figure 3.4 Energy band diagram of a single-island, double tunnel junction system when V_{DS} is null, showing possible island discrete levels relative to the island and drain Fermi levels corresponding to the island net charge $Q = N \times e$, where e is the elementary charge and N is an integer.

If we consider that the single-island, double tunnel junction system is symmetrical, i.e., C_S and C_D are equal, then the potential drops between the intermediate island and each of the two

terminals are equal. The I_{DS}-V_{DS} curve, along with the energy band diagrams of such a case with respect to three distinct V_{DS} voltages are presented in Fig. 3.5. Represented island discrete upper and lower energy levels correspond to the island charge of respectively $-e$ and e. Since the tunnel junctions are symmetrical, these levels are at the same gap from the Fermi level corresponding to neutral island charge. At $V_{DS} = 0$ V the energy barrier seen by an electron to tunnel to the island is $\frac{e^2}{2\,C_\Sigma}$, as illustrated in Fig. 3.5. For low values of V_{DS}, electrons cannot overcome this barrier. The I_{DS}-V_{DS} curve exhibit a nonlinear behaviour with a zero current region, known as the Coulomb gap, for $|V_{DS}| \geq V_C = \frac{e}{C_\Sigma}$, where V_C is known as the Coulomb blockade voltage. $|V_{DS}|$ has to be increased to at least $V_C = \frac{e}{C_\Sigma}$ to let electrons flow through the island.

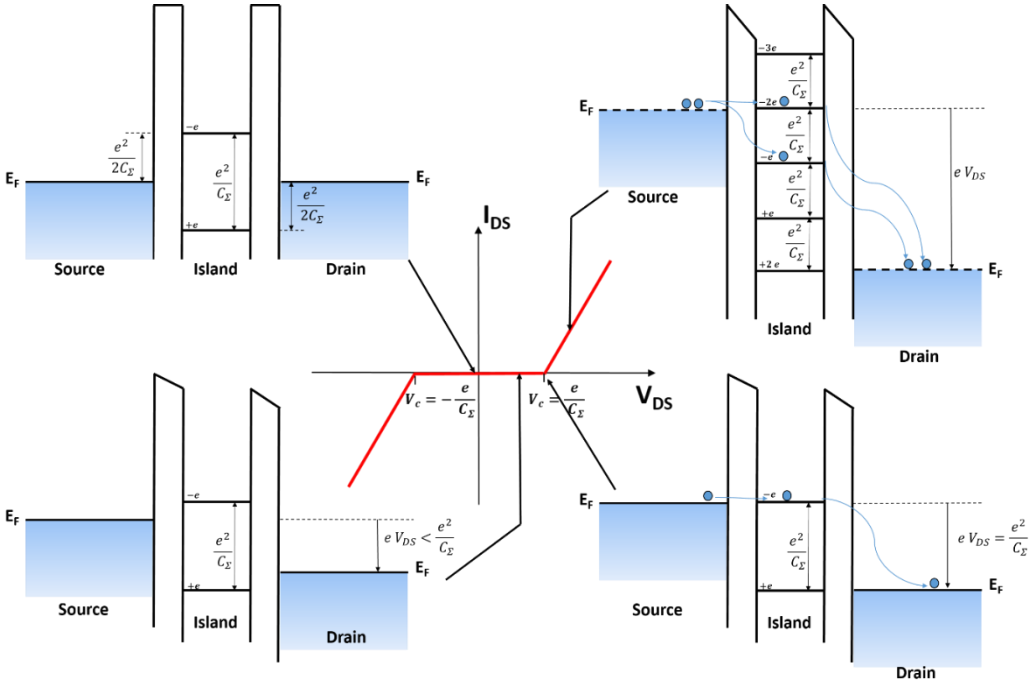

Figure 3.5 I_{DS}-V_{DS} characteristics corresponding to a symmetrical single-island, double tunnel junction system, with energy band diagrams corresponding to distinct values of V_{DS}. Represented island discrete energy levels correspond to the island net charge $Q = N \times e$, where e is the elementary charge and N is an integer. Since the tunnel junctions are symmetrical, these levels are at the same gap from the island Fermi level corresponding to neutral island charge.

In literature, because needed voltage to overcome the Coulomb blockade is $\frac{e}{C_\Sigma}$ when tunnel junctions are symmetrical, the charging energy E_c is often expressed as:

$$E_c = \frac{e^2}{C_\Sigma} \tag{3.5}$$

as a more adequate measure of the strength of these effects. In the following, we consider the expression given in Eq. 3.1. The charging energy $\frac{e^2}{2\,C_\Sigma}$ is behind blocking the injection/ejection of a single charge into/from the island. Coulomb blockade is observed when the charging energy of a single electron is much larger than the thermal energy $K_B T$, where K_B is Boltzmann constant and T is the temperature, to prevent thermally activated tunnel current. This condition is known as the capacitance condition and is expressed as:

$$E_c = \frac{e^2}{2\,C_\Sigma} \gg K_B\,T \tag{3.6}$$

At 300 k, this gives:

$$C_\Sigma \ll 3 \text{ aF} \tag{3.7}$$

It is necessary to have a nanometre-scale island (~100 nm or less in size), to have C_Σ in the aF range.

Another condition needed to observe the Coulomb blockade effect, known as the opacity condition, is to have the charge well localized on the island. This is to suppress quantum fluctuations in the number of electrons in the island. If the tunnel barriers are not sufficiently resistive, the electron wave function may extend strongly across the tunnel barriers into the electrodes, then the charging electrons cannot be localized on the island. Heisenberg uncertainty principle is expressed as:

$$\Delta U\,\Delta t > h \tag{3.8}$$

where ΔU is the electrostatic energy, Δt is the lifetime of the charging, and h is Planck's constant. ΔU is proportional to $e^2/\,C_t$. Δt equals $R_t\,C_t$, where R_t is the tunnelling resistance and C_t is the tunnelling junction capacitance. The uncertainty inequality reduces to:

$$R_t > \frac{h}{e^2} = R_q \approx 25.8\ \text{K}\Omega \tag{3.9}$$

R_q is known as the quantum resistance. As a result, to satisfy the opacity condition, one must have the tunnelling resistance larger than the quantum resistance R_q. Furthermore, it is necessary that the tunnel barrier height does exceed $K_B T$, in order to prevent hot electrons from flowing to the island over the potential barrier (thermionic emission current).

3.2.2 Single electron transistor

A SET is a three terminal device. It is formed by an island separated from drain and source by leaky capacitors (tunnel junctions), to which a gate electrode is added. The gate electrode is electrostatically coupled to the island through an ideal infinite-resistance capacitor. The schematic structure and circuit diagram of a SET with the source taken as common voltage reference for gate and drain polarization are shown in Fig. 3.6. The gate bias is capacitively coupled to the island and allows shifting its electrostatic potential. The gate voltage V_{GS} may be used to control the Fermi level of the island, and to overcome or impose a Coulomb blockade.

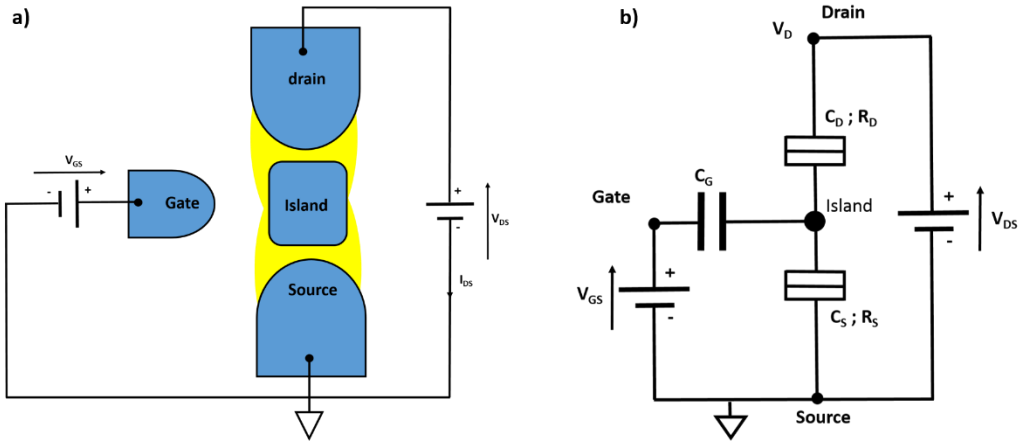

Figure 3.6 a) Schematic structure of a single electron transistor. b) Circuit diagram of a single electron transistor. The source is considered as common voltage reference for gate and drain polarization. C_G denotes the gate-to-island capacitance.

Let us consider the island initially neutral. The corresponding energy band diagram is shown in Fig. 3.7.c. By applying a positive V_{GS}, the island Fermi level is shifted down to compensate the electrostatic energy barrier. The electrostatic energy barrier seen by an electron reaching the island from the source, under a gate bias is expressed as:

$$\Delta E_{S\to I} = \frac{e^2}{2\,C_\Sigma} - e\,\frac{C_G}{C_\Sigma}\,V_{GS} \neq 0 \tag{3.10}$$

where C_Σ, the island total capacitance is nothing but the sum of the three capacitance: C_S, C_D and C_G. Eq 3.10 leads to a threshold gate voltageV_{GS}^{th}, needed to overcome this barrier, which equals:

$$V_{GS}^{th} = \frac{e}{2\,C_G} \tag{3.11}$$

If a non-null small V_{DS} is applied, a current flows from drain to source across the island. The island is then charged with a single electron. This situation is illustrated in Fig. 3.7.d. Increasing the gate voltage V_{GS} further but still below $2 \times V_{GS}^{th} = \frac{e}{C_G}$ makes the Fermi level corresponding to single charged electron decreases to a point where electron transfer from the island to the drain is energetically non favourable because the island Fermi level is below drain Fermi level (Fig. 3.7.e), then the current is suppressed and the island has a net charge of one electron. If V_{GS} is increased to twice V_{GS}^{th} so that the energy barrier associated with addition of a second electron to the island is overcome, a second electron flows from the island to the drain and the island is now charged with two electrons, as illustrated n Fig. 3.7.f. Further increase in V_{GS} causes I_{DS} to oscillate periodically, as can be seen in Fig. 3.7.b with a constant period equal to $\frac{e}{C_G}$, each current peak corresponding to a change in the island net charge by only one electron (Fig. 3.7.b). With increasing V_{GS} the island net charge is increased one by one.

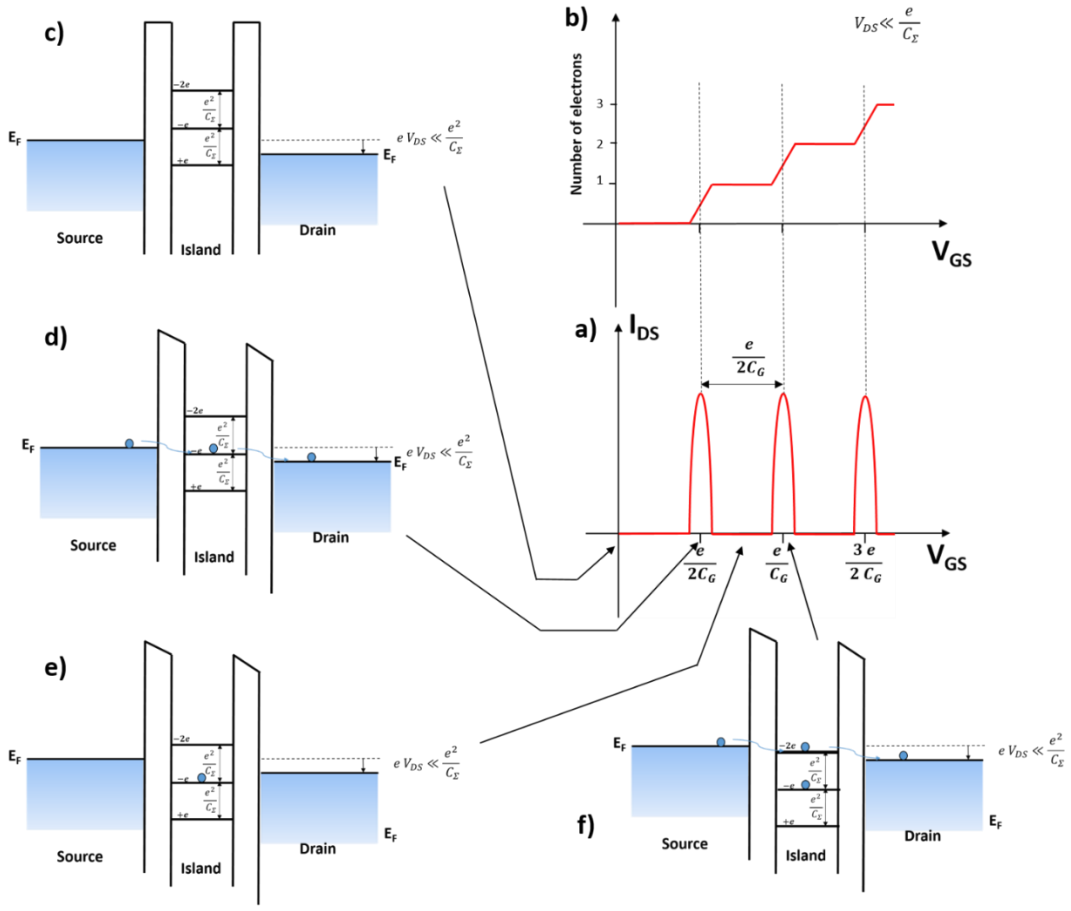

Figure 3.7 a) I_{DS}-V_{GS} characteristics at a small V_{DS}, known as Coulomb oscillations. b) Number of electrons accumulated in the island as a function of V_{GS}. c-f) Energy band diagrams corresponding to distinct values of V_{GS} at a small V_{DS} for $V_{GS} = 0\ V$, $V_{GS} = \frac{e}{2\ C_G}$, $\frac{e}{2\ C_G} < V_{GS} < \frac{e}{C_G}$ and $V_{GS} = \frac{e}{C_G}$.

The gate bias can be used to shift the island potential down to make the island Fermi level enclosed between source and drain Fermi levels. In other words, increasing V_{GS} make the discrete energy levels "scroll down" which leads to I_{DS}-V_{GS} characteristics known as Coulomb oscillations, shown in Fig. 3.7.a. The gap between the energy levels corresponding to the distinct island net charge $Q = N \times e$, where N is an integer, is $\frac{e}{C_\Sigma}$. A variation in the gate voltage ΔV_{GS} leads to variation in the island potential as much as $\frac{C_G}{C_\Sigma}\Delta V_{GS}$. The needed ΔV_{GS} variation to shift the island Fermi level by $\frac{e}{C_\Sigma}$ is obtained from:

$$\frac{C_G}{C_\Sigma}\Delta V_{GS} = \frac{e}{C_\Sigma} \quad (3.12)$$

Which reduces to:

$$\Delta V_{GS} = \frac{e}{C_G} \quad (3.13)$$

Therefore Coulomb peaks are distanced by $\frac{e}{C_G}$.

In Fig. 3.7.a and 3.7.b, represented V_{GS} values corresponding to oscillation peaks are valid if the island has no background charge Q_0. These values are shifted if the island has a non-null background charge. However Coulomb oscillations peaks always have a period of $\frac{e}{C_G}$.

If V_{DS} is increased, this will allow a multi-level conduction through the island but I_{DS}-V_{GS} characteristics still exhibit Coulomb oscillations with a DC offset corresponding to conduction levels below the upper one. The SET can then be considered as a switch device controlled by the gate bias. Adjusting V_{GS} to a voltage corresponding to an oscillation peak leads to the suppressing of the Coulomb blockade and the transistor is in an ON "state". When V_{GS} is set to 0 (or elsewhere than values corresponding to Coulomb oscillations), the transistor is in an "OFF" state, as illustrated in Fig. 3.8.

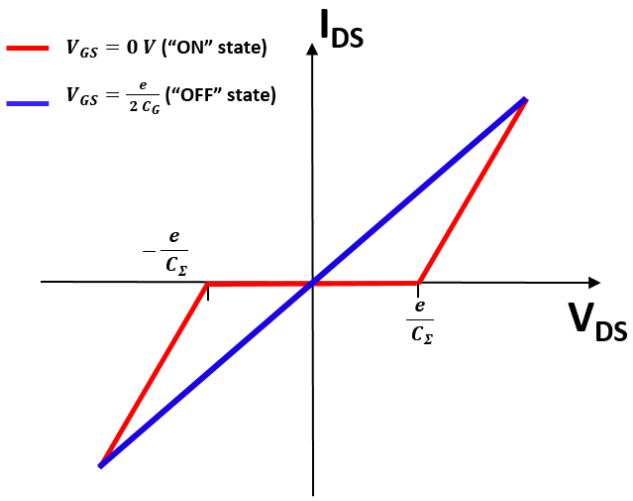

Figure 3.8 I_{DS}-V_{DS} characteristics of a SET in the "ON" and "OFF" states. (This characteristic corresponds to symmetrical tunnel junction SET, symmetrical V_{DS} polarization, and a null background island charge).

Coulomb blockade regions for different combinations of V_{DS} and V_{GS} may be presented within the same 2D plot: the stability diagram, shown in Fig 3.9. A colour scale is used to represent the current level. A Stability diagram could also be presented in terms of conductance. Due to its typical shape this diagram is commonly known as the Coulomb diamond. Inside the diamonds the island has a stable number of electrons. The frontiers between the diamonds define the limit of the Coulomb blockade regions for tunnelling across the tunnel junctions. Slopes of these borders are expressed as:

$$\frac{dV_{GS}}{dV_{DS}}|\Delta E_{S\to I} = -\frac{C_D}{C_G} \tag{3.14}$$

$$\frac{dV_{GS}}{dV_{DS}}|\Delta E_{I\to D} = \frac{C_G + C_S}{C_G} \tag{3.15}$$

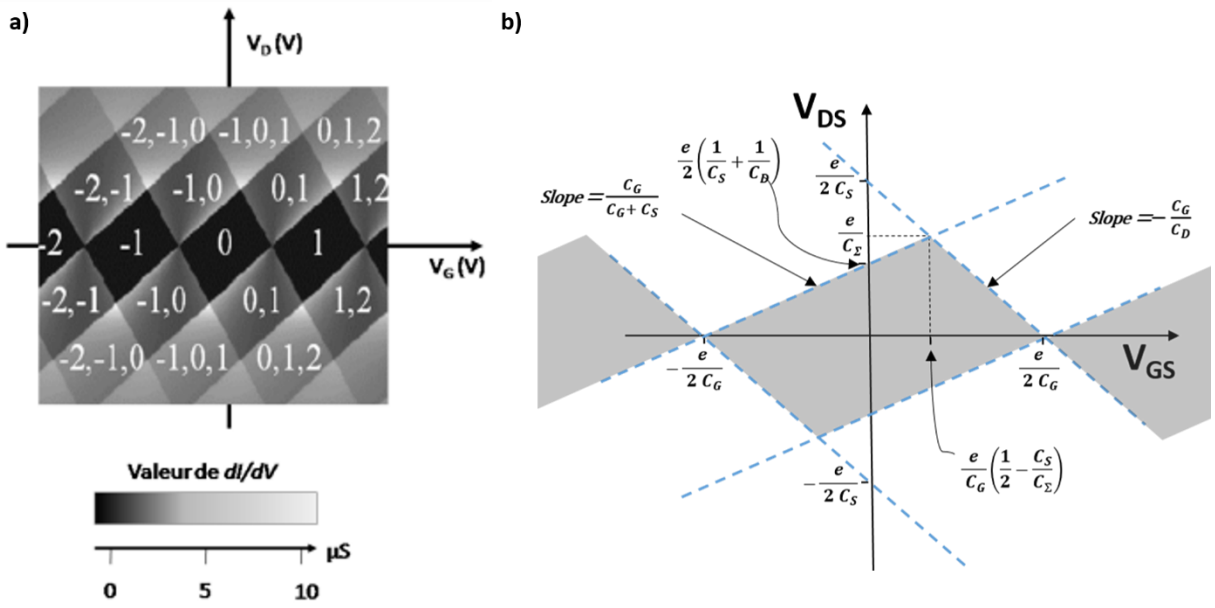

Figure 3.9 Coulomb diamonds of an SET. a) Conduction stability diagram. Numbers separated by commas represent the possible states in terms of the number of electrons charging the island. Black coloured regions are Coulomb blockade zones [22]. b) Illustration of SET parameters defining the shape of the Coulomb diamonds.

3.2.3 The Orthodox theory

Throughout the history of single electronics, major models describing the operation of single electron devices or systems have been based on the so-called "Orthodox theory". Developed first by I.O Kulik and R.I Shekhter [66] and generalized later by Averin and Likharev [67].

The theory gives the rules running the tunnelling events and the system state time evolution. The theory makes the following major assumptions [38]:

- The electron energy quantization in the island is ignored, and the electron energy spectrum is considered continuous.
- The time of tunnelling through the barrier is assumed to be negligible in comparison with other time scales (including the interval between subsequent tunnelling events)
- Coherent quantum processes consisting of several simultaneous tunnelling events ("co-tunnelling") are ignored. This assumption is valid if the resistance of all the tunnel barriers of the system is much higher than the quantum resistance R_q.

Within the Orthodox theory, the system can be seen as an ensemble of conductors connected either by tunnel junctions or capacitors and the rate (i.e., probability per unit time) of a tunnel event is a function of the variation in Helmholtz free energy as a result of the tunnelling [38] and is given by:

$$\Gamma(\Delta F) = \frac{\Delta F}{e^2 R_t \left(1 - e^{-\frac{\Delta F}{K_B T}}\right)} \tag{3.16}$$

where ΔF is variation in Helmholtz's free energy, and R_t is the tunnel junction resistance. Helmholtz free energy is defined by the difference in electrostatic energy stored in the circuit and the work done by the voltage sources. We should note that the tunnelling rate depends on the tunnel junction resistance and temperature. The state probabilities are solutions of the master equations [38] given by:

$$\frac{dP_i}{dt} = \sum_j \Gamma_{j\to i} P_j - \Gamma_{i\to j} P_i \tag{3.17}$$

where $\Gamma_{j\to i}$ and $\Gamma_{i\to j}$ are the tunnelling rates respectively from state *j* to state *i* and from state *i* to state *j*, P_i is the occupation probability of state *i*, and the system is assumed to evaluate in a discrete manner at random time steps [68]. Several simulators [69, 70] have been developed within the framework of the Orthodox theory.

3.3 Double gate transistor-based gas sensor

SG-FET-based gas sensors offer advantages of detecting chemisorbed, as well as physisorbed gas molecules [42] but also to benefit from the transistor gain to amplify the chemical signal. They have been demonstrated to operate at room temperature or slightly above it, and sensitive to a broad range of gases [12, 41, 42] such as CO [45, 71], H_2 [16, 24, 72, 73], alcohols [74], O_3 [75], NH_3 [31] and NO_2 [41] thanks to real flexibility in sensitive layer choice and integration in comparison to catalytic MOSFETs and PolFETs.

However, integration of these sensors is complex from a fabrication point of view because of the necessity to implement a suspended gate electrode with the sensitive material deposited on the back side. The sensing layer has to be deposited on the back side of the gate electrode otherwise the adsorption induced material work function change (change in surface potential) would be screened by the gate electrode because it is biased [74, 76].

In addition, the transistor channel width to channel length ratio W/L has to be increased to overcome poor transconductance due to the very low capacitance across the airgap [41, 42]. To have a high signal to noise ratio the transconductance has to be as high as possible.

In the linear regime of the $I_{ds} - V_{ds}$ characteristic, the transistor transconductance g can be written as:

$$g = \frac{dI_{DS}}{dV_G} = \mu \frac{W}{L} C_{eq} V_{ds} \tag{3.18}$$

Where μ is the inversion charge carrier mobility, C_{eq} is the equivalent gate capacitance defined as a series of insulator and airgap capacitances, and V_G is the gate voltage. The sensor sensitivity can thus be defined as [73]:

$$S = {}^{g}/_{V_{ds}} = \mu \frac{W}{L} C_{eq} \quad (3.19)$$

S can be increased by increasing ${}^{W}/_{L}$ ratio and C_{eq}. However increasing C_{eq} by increasing the capacitance across the airgap is limited by the minimum of ~0.8 µm airgap needed to ensure fast gas species diffusion [73]. Meanwhile, increasing ${}^{W}/_{L}$ ratio is a limiting factor toward miniaturization and high density integration.

If the transistor channel can be controlled by two different gate electrodes, a suspended gate is no longer needed because one gate would be used to bias the transducer at the aimed operation point, and the second gate would be functionalized with a dedicated gas-sensitive material. The sensitive material is directly deposited on top of the functionalized gate electrode, which is floating (not biased) and used to capacitively couple surface charge at the outer sensing layer surface to the transistor channel.

Sensing layer surface charge is the result of, in addition to dandling bonds and surface defects, the partial charge transfer from/to the material during the gas species adsorption process (as detailed in section 2.2). An equal and opposite to the surface charge, charge accumulation exists in the close vicinity of the material surface. If the sensing material is a metal, the surface charge accumulation is located at the surface. If the material is semiconducting the charge accumulation is distributed over a space charge zone (depletion layer). This is illustrated for H_2 chemisorption on Pt (metallic sensing material) and O_2 chemisorption on SnO_2 (semiconducting sensing material) respectively in Fig 3.10.a and Fig. 3.10.b.

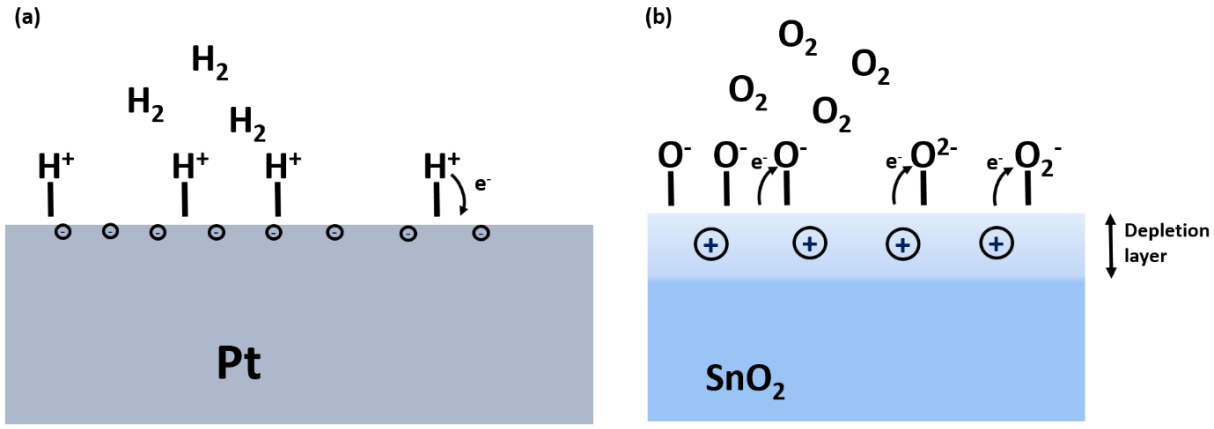

Figure 3.10 Schematic representation of gas molecules chemisorption on a sensing layer surface showing the partial charge transfer. a) H_2 chemisorption on Pt surface showing the partial electron transfer. b) O_2 chemisorption on SnO_2 surface showing the partial electron withdrawing.

Double gate–single electron transistors (DG-SETs) are of great interest because they offer the possibility to incorporate two different gate electrodes without any need for an airgap structure: a functionalized gate with a dedicated gas-sensitive material on top of it and a bias gate to control the operation point of the transistor, as depicted in Fig. 3.11b. Implementation of this concept is carried out as shown in Fig. 3.11.a. The sensing layer is deposited over a metallic pad and the ensemble forms what is referred to as the sensing pad. The sensing pad is integrated above the device and electrically connected to the DG-SET top gate which plays the role of a functionalized gate. The equivalent circuit diagram is shown in Fig. 3.11.b.

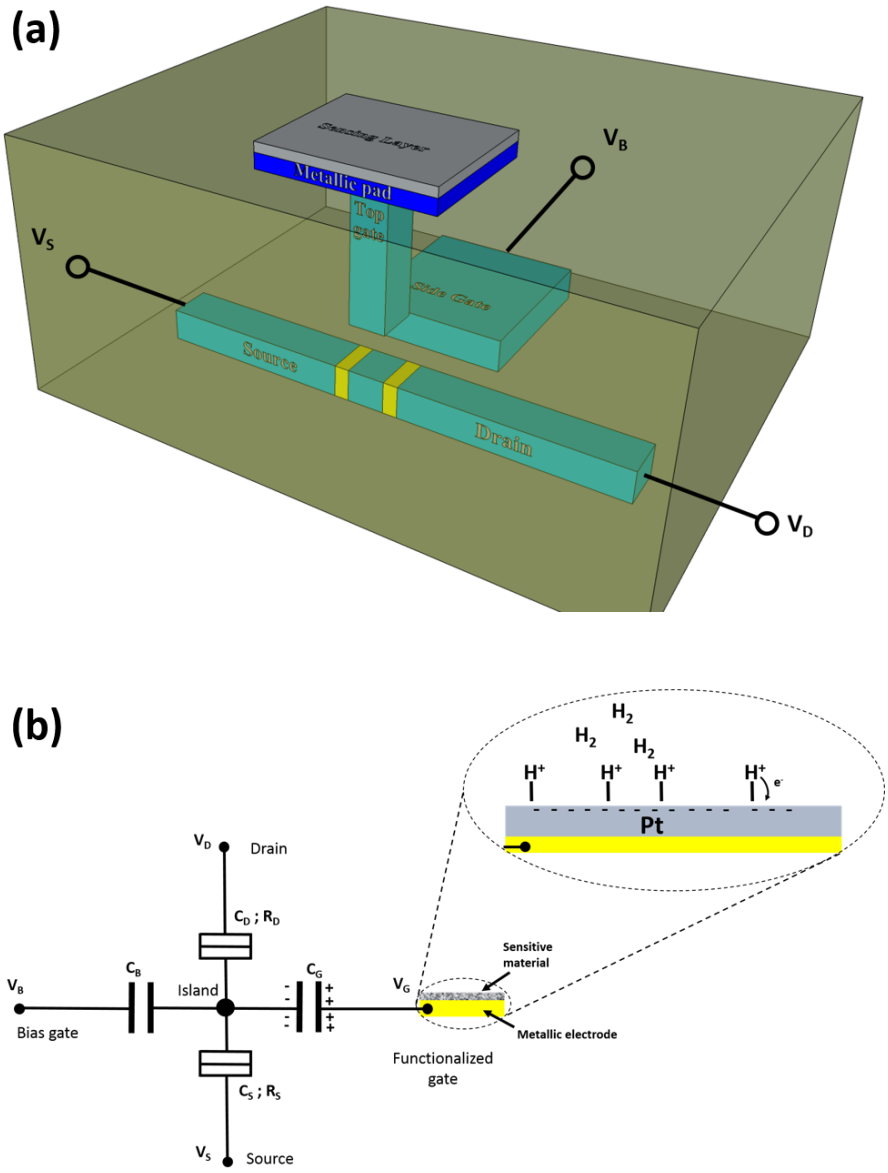

Figure 3.11 a) 3D schematic of the DG-SET-based gas sensor concept showing the top gate connected to the sensing pad and playing the role of the functionalized gate and the side gate serving as a bias gate. b) Circuit diagram of the DG-SET-based gas sensor showing the island capacitively coupled to two different gate electrodes: a functionalized gate and a bias gate. C_G and C_B denote respectively functionalized gate and bias gate capacitances. Only the bias gate is polarized by the voltage source V_B.

Functionalized gate and bias gate capacitances are referred to as respectively C_G and C_B. Only the bias gate is polarized by a voltage source V_B. It should be noted that V_G is nota result of polarization by a voltage source, which has an infinite reservoir of electrons, but of polarization

by the finite sensing material surface charge. This charge is capacitively coupled to the SET island through C_G. Charge variation induces a variation in the sensor output signal: I_{DS}. Coulomb oscillations with respect to the functionalized gate charge, spaced by $\frac{e}{C_G}$, for $V_B = 0$ V and $V_B = V_{shift}$ are shown in Fig. 3.12. The linear part of a Coulomb peak, delimited in Fig. 3.12, is the operation range of interest. The operation current I^0 is nothing but the current at the midway of the Coulomb peak linear region of interest. The sensor sensitivity is defined by the Coulomb peak slope. Surface charge variation is then coupled to the transistor island and yields current variations around the operation current I^0.

In an absence of the target gas (under background gas) the functionalized gate surface charge is not null and is equal to a charge amount Q^0. When applying a voltage V_{shift} to the bias gate, the Coulomb oscillations at varying functionalized gate voltage, or charge are shifted, as illustrated in Fig. 3.12. The bias gate voltage V_B is used to make Q^0 corresponds to the operation current I^0. $Q^0$and I^0 are the sensor operation point parameters. The V_{Shift} satisfies the following relation:

$$C_B(V_{shift} - V_{Island}(V_B = V_{Shift}) = C_G(V_G - V_{Island}(V_B = 0) - (-Q^0) \qquad (3.20)$$

At $V_B = V_{shift}$, the functionalized gate surface charge variation around Q^0: $Q^0 \pm \Delta Q$ yields a proportional current variation $I^0 \pm \Delta I$.

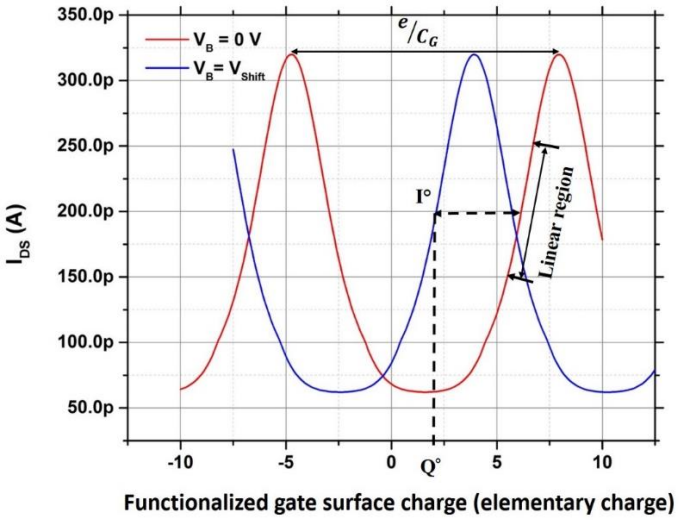

Figure 3.12 Coulomb oscillations with respect to the functionalized gate charge for $V_B = 0$ V and $V_B = V_{shift}$.

Such a configuration of double-gate transistor is also possible with FD-SOI MOSFETs. In addition to the front gate, the substrate bulk Si can be used for back biasing of the transistor channel through the buried oxide. Such a device is attractive for gas sensing applications due to their amplification capability when operated in the sub-threshold regime. Ideal subthreshold swing and high transconductance levels have been achieved thanks to thin Si film on buried oxide [77], which is the strongest asset of these devices with respect to the FET-based gas sensor technology. In addition, the small size of these devices is also of a high interest in terms of integration density. FD-SOI FETs are a mature technology and well modelled.

Ultrathin body and BOX (UTBB) FD-SOI MOSFETs are considered as the most promising devices for sensing applications. The thin buried oxide (BOX) has allowed the enhancement of the technology scalability, ideal subthreshold swing and a control of the threshold voltage with the back gate bias (substrate biasing) without the need of using different channel doping concentrations and thus lower variability due random dopant fluctuations [78, 79]. Thanks to the back-to-front gate coupling factor obtained with the UTBB FD-SOI FETs, the threshold voltage can be shifted and a nearly ideal subthreshold slope can be obtained without the need for excessive substrate bias (back gate bias) [77].

Similar to the concept presented above the sensing pad is connected to the front gate which is kept floating (not biased) plays the role of the functionalized gate. We take advantage of the back gate, which is used as a control gate, to bias the transistor at the aimed operation point (see Fig. 3.13).

In an absence of the target gas (under background gas) the functionalized gate surface charge, referred to as ${Q_{gf}}^0$, is not null, and equal but opposite in signs to the charge present at the outer surface of the front gate. It is equal to the charge lying at the front gate inner surface/front gate oxide interface. The functionalized gate (front gate) charge varies in the range ${Q_{gf}}^0 \pm \Delta Q_{gf}$, where ΔQ_{fg} is the target gas induced surface charge variation.

In UTBB MOSFETs, the back gate biasing has the capability of shifting the front gate subthreshold voltage, without excessive voltages. Typical transfer characteristics $I_{ds}\ versus\ V_{gf}$ of an n-type FD-SOI MOSFET for various back gate bias V_{gb} are presented in Fig 3.14. The drain –to-source current I_{ds} variation as a function of the front gate charge Q_{gf}

follows the same variation as well as a function of the corresponding voltage V_{gf}, as illustrated in Fig 3.14.

The back gate is used to shift the I_{DS} $versus$ Q_{gf} curve so that the linear region corresponds to the variation range of the front gate charge ${Q_{gf}}^{0} \pm \Delta Q_{gf}$.

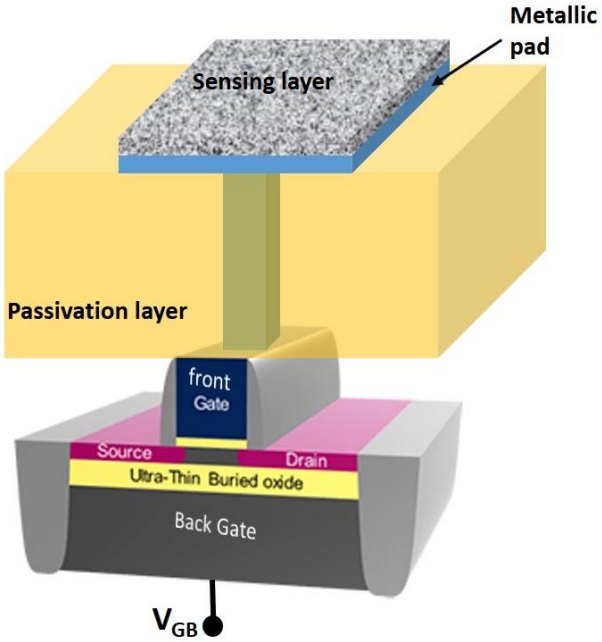

Figure 3.13 3D schematic representation of the FD-SOI MOSFET-based gas sensor concept showing the front gate connected to the sensing pad and playing the role of the functionalized gate and the substrate serving as a control gate.

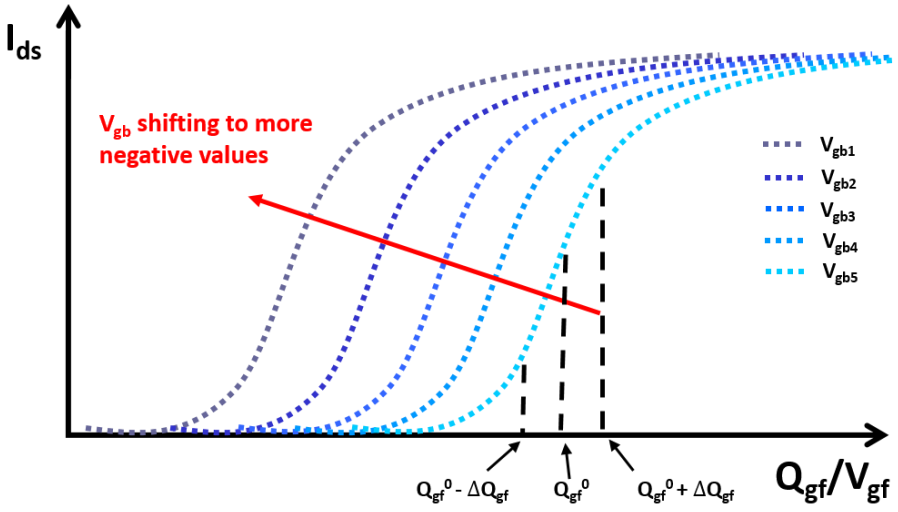

Figure 3.14 Typical characteristics I_{ds} $versus$ V_{gf}/Q_{gf} at various V_{gb} of an n-type FD-SOI MOSFET showing the shifting effect of the back biasing.

3.4 DG-SET-based gas sensor design, modelling and simulation

Incorporating an additional gate electrode to the SET comes at the expense of the island total capacitance and hence the operating temperature. The geometrical design has to take into consideration not only the functionalized gate-to-island capacitance, but also all the parasitic capacitive coupling between the functionalized gate and the surrounding electrodes (drain, source, bias gate). A Circuit diagram of the DG-SET showing the functionalized gate parasitic capacitive coupling with drain, source and bias gate, is presented in Fig. 3.15. All the device capacitances are summarized in table 3.1. C_1, C_2 and C_3 are respectively the functionalized gate-to-source, the functionalized gate-to-drain and the functionalized gate-to-bias gate capacitances. C_4 and C_5 are respectively the bias gate-to-source and the bias gate-to-drain capacitances. In fact, the parasitic capacitances C_1, C_2, C_3, C_4 and C_5 increase the effective capacitive coupling between the island and all the other terminals: source, drain, bias gate and functionalized gate and hence the effective island total capacitance.

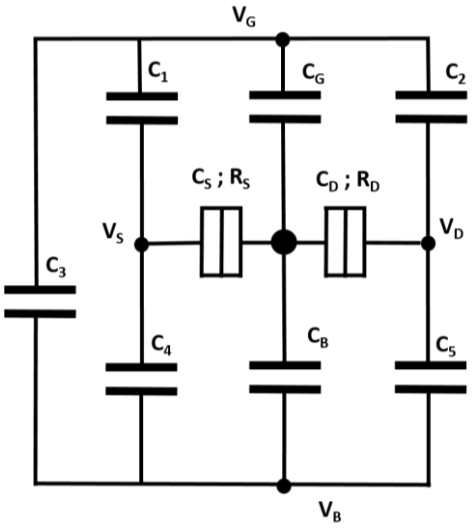

Figure 3.15 Circuit diagram of a DG –SET showing the functionalized gate parasitic capacitances C_1, C_2 and C_3, and bias gate parasitic capacitances C_4 and C_5.

Table 3.1 Capacitances into play in the DG-SET-based gas sensor operation.

Capacitance	**Symbol**
Island-to-source capacitance	C_S
Island-to-drain capacitance	C_D
Island-to-side gate capacitance	C_B
Island-to-top gate capacitance	C_G
Functionalized gate-to-side gate	C_3
Functionalized gate-to-source	C_1
Functionalized gate-to-drain	C_2
Bias gate-to- source	C_4
Bias gate-to-drain	C_5

In the following, first the functionalized gate geometrical parameters have been optimized with regard to the island total capacitance as well as the C_G-to-the functionalized gate total parasitic capacitance ratio (referred to below as R). Capacitances C_G, C_1, C_2 and C_3 have been calculated with respect to geometrical parameters, using COMSOL Multiphysics software (finite element simulations).

The DG-SET sensitivity is defined by Coulomb oscillations peaks slope ($I_{DS} - V_G$) and thus by C_G and V_{DS} but also depends on the parasitic capacitances. The sensor output signal has been simulated using a Monte Carlo single electronics simulator, with all device capacitances prior extracted from COMSOL simulations, in order to estimate the sensor sensitivity.

3.4.1 Functionalized Gate Capacitances Calculation

All the device capacitances have been calculated with respect to real geometry using COMSOL Multiphysics software. The software allows solving Maxwell's equations in the entire implemented geometry using the finite element method. As illustrated in Fig. 3.16, the

functionalized gate is implemented as a top gate and the bias gate is as a side gate.

The device is encapsulated in a TEOS (TetraEthyl OrthoSilicate) layer, with dielectric constant of 4.2, which defines the side gate dielectric material. Calculations under COMSOL were carried out to study the impact of the functionalized gate geometry parameters on the functionalized gate parasitic capacitances. For all the calculations, several geometry parameters, summarized in table 3.2, are set to reasonable constant values within reach of the developed fabrication process, detailed in Chapter 5. TiO_2 with dielectric constant of 3.5 was considered as the tunnel junction dielectric material.

Table 3.2 Geometry parameters, symbols and considered values for the COMSOL model.

Geometry Parameters	**Symbol**	**Considered value for COMSOL calculations**
Side gate width (nm)	$W_{Side\ gate}$	120
Side gate-to-island distance (nm)	$D_{Side\ gate}$	100
Island width (nm)	W_I	20
Island length (nm)	L_I	20
Tunnel junction dielectric thickness (nm)	$t_{Dielectric}$	8
Structure thickness (nm)	t_{CMP}	5

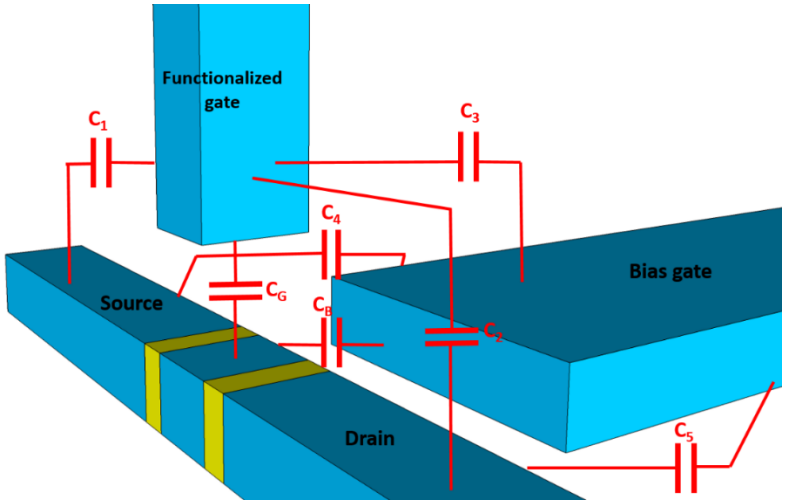

Figure 3.16 Functionalized gate 3D scheme showing all the capacitances at play in the DG-SET characteristics. The functionalized gate is implemented as a top-gate, and the bias gate as a side-gate.

As illustrated in Fig. 3.17, the functionalized gate is implemented as a top gate with a side length A and perfectly aligned on the island. The top gate is at a distance from the island of $D_{Top\ gate}$. Top gate parameters are summarized in table 3.3.

Table 3.3 Top gate parameters for the COMSOL model.

Top gate parameter	**Symbol**
Top gate-to-island distance	$D_{Top\ gate}$
Top gate side length	A
Top gate dielectric permittivity	K

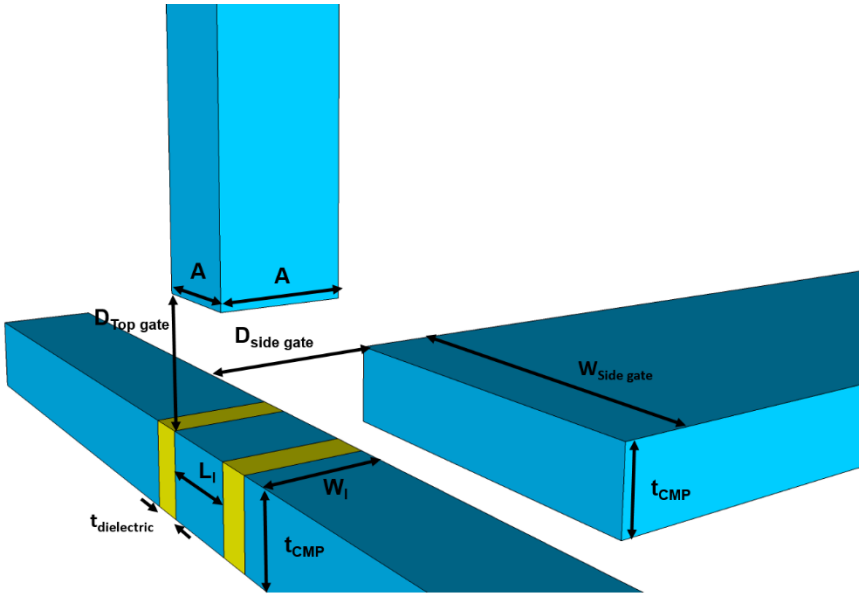

Figure 3.17 3D Schematic of the simulated DG-DET showing the geometrical parameters.

First, all the device capacitances have been calculated for geometry and material parameters values listed in table 3.2, $A = 20$ nm, $D_{Top\ gate} = 50$ nm, and TEOS ($K = 4.2$) as a top gate dielectric material. Obtained island capacitances are presented in table 3.4. Side gate-to-drain and side gate-to-source capacitances were found to be equal to 2.4 aF.

Table 3.4 Island capacitances calculated with COMSOL for geometry and material parameters values listed in table 3.2, $A = 20$ nm, $D_{Top\ gate} = 50$ nm, and $K = 4.2$.

Island capacitance	**Value (aF)**
Island-to-source capacitance (C_S)	1.82
Island-to-drain capacitance (C_D)	1.82
Island-to-side gate capacitance (C_B)	0.37
Island-to-top gate capacitance (C_G)	0.31
Island total capacitance (C_Σ)	4.34

The top gate design has to be optimized to increase the top gate-to-island capacitance (C_G) and minimize all the top gate parasitic capacitance (C_1, C_2 and C_3). This is to increase the top gate-to-island capacitance to top gate total parasitic capacitance ratio R, expressed as:

$$R = \frac{C_G}{C_1 + C_2 + C_3} \tag{3.21}$$

Both of the ratio R and top gate lever C_G/C_Σ impact the transducer sensitivity. The ratio R translates the fraction the functionalized gate charge that is coupled to the island rather than to the other surrounding electrodes (drain, source and site gate electrodes). Larger is R, greater is the DG-SET-based gas sensor sensitivity. Larger is C_G, greater is the sensitivity. Since the geometry is symmetrical around the side gate axis, the top gate-to-drain and top gate-to-source capacitances are equal. In the following, only the top gate-to-source capacitance is represented in figures for sake of clarity.

First, the impact of the top gate side length on top gate capacitances has been studied for $D_{Top\ gate} = 50$ nm. Fig. 3.18 presents calculated top gate capacitances and ratio R at varying side length A. All the top gate capacitances increase with increasing the side length. For A greater than 30 nm the parasitic top gate capacitances increase strongly more than the top gate-to-island capacitance. The ratio curve has a bell shape around $A = 30$ nm. The maximum ratio at $A = 30\ nm$ is 0.14. The optimum value of 30 nm is considered for the following step of capacitance calculation at varying $D_{Top\ gate}$.

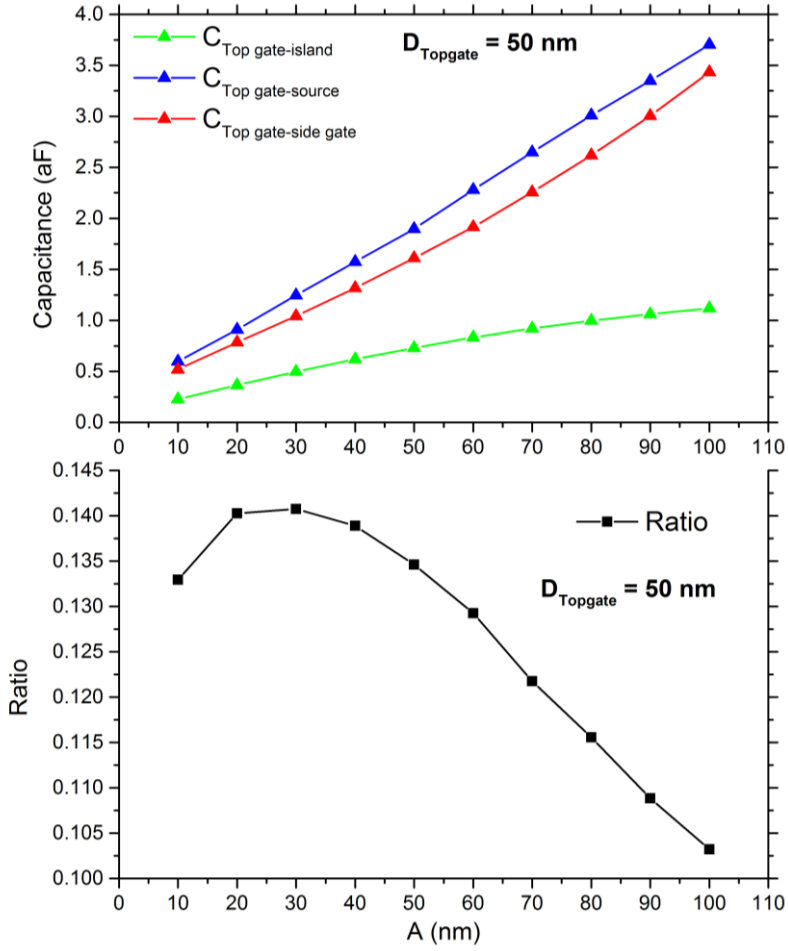

Figure 3.18 Impact of top gate side length on top gate capacitances. a) Top gate capacitances versus side length for $D_{Top\ gate} = 50$ nm. b) R *versus* side length for $D_{Top\ gate} = 50$ nm.

Fig. 3.19 presents calculated top gate capacitances and ratio R at varying $D_{Top\ gate}$. C_G is found more impacted by varying $D_{Top\ gate}$ than the parasitic capacitances C_1, C_2 and C_3. The closer the top gate is to the island, the greater the top gate-to-island capacitance C_G is. With decreasing $D_{Top\ gate}$ below 30 nm, C_G increases strongly and hence the ratio R strongly increases as well. Decreasing $D_{Top\ gate}$ improves greatly the capacitive coupling of top gate charge to the island and hence the top gate lever (C_G/C_Σ), which yields more abrupt Coulomb peak slope, as well as the ratio R. But at the same time it increases the island total capacitance and thus comes at the expense of operating temperature.

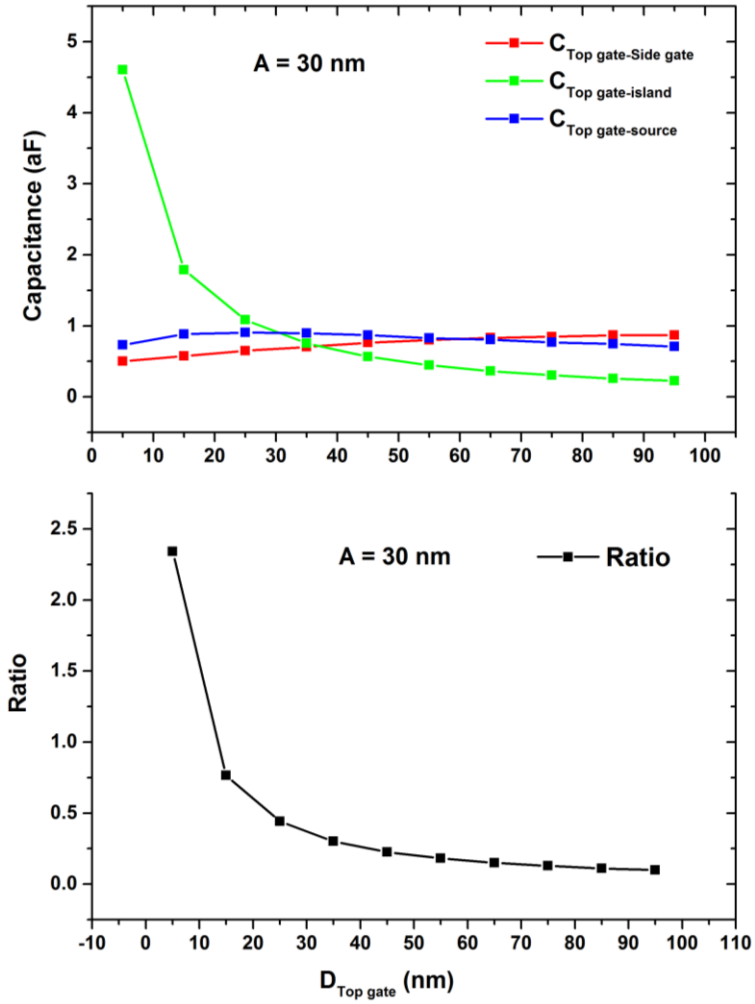

Figure 3.19 Impact of top gate distance on top gate capacitances. a) Top gate capacitances *versus* top gate distance for $A = 30$ nm. b) R *versus* top gate distance for $A = 30$ nm.

For appropriate operation and to benefit from Coulomb peaks slope, it is preferable to have the charging energy few times larger than the thermal energy. This condition can be expressed as:

$$\frac{e^2}{2\,C_\Sigma} > \alpha\, K_B T \qquad (3.22)$$

where α is a coefficient. Table 3.5 gives maximum island total capacitance with respect to the target operating temperature of 25 and 60 °C, with α = 10.

Table 3.5 Maximum island total capacitance with respect to target operating temperature.

Operating temperature (°C)	Maximum island total capacitance (aF)
25	0.3
60	0.27

The island total capacitance is the limiting factor for the top gate design. It is better to have lower top gate-to-island capacitance at the expense of the Coulomb peak slope and the ratio, and hence the sensor sensitivity. Moreover, having a smaller slope increases the sensitivity range (excursion range). Meanwhile, lowering C_G by increasing $D_{Top\ gate}$, increases very slightly the parasitic capacitances C_1, C_2 and C_3, as can be seen in Fig 3.19. These parasitic capacitances increase the effective island total capacitance. Therefore, a compromise has to be found for the top gate distance. Monte Carlo simulations presented below have allowed to set the acceptable island total capacitance that allows to have Coulomb oscillations and thus a functional device at room temperature.

For each considered $D_{Top\ gate}$, optimization of the top gate side length A again has to be done. In the following we consider $D_{Top\ gate} = 15nm$. The impact of the side length on R is presented in Fig. 3.20. The obtained optimum side length is 20 nm, for a maximum ratio at 0.76.

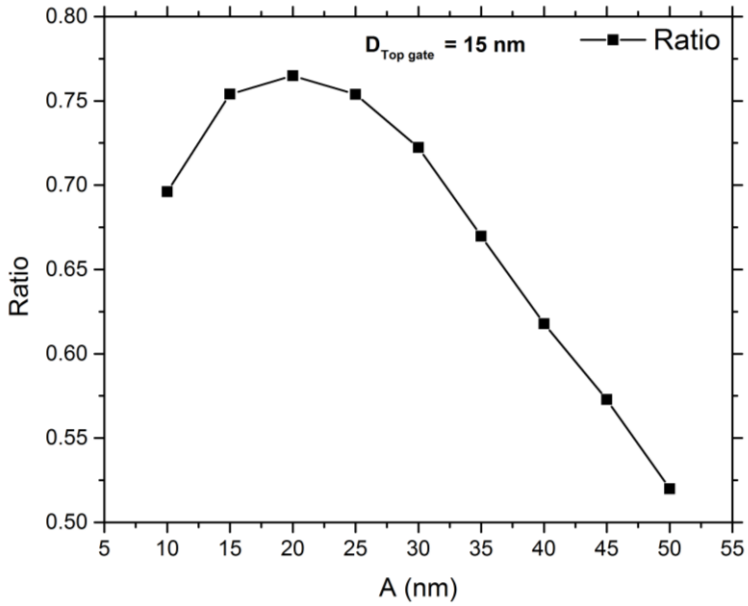

Figure 3.20 The ratio R as a function of side length for $D_{Top\ gate} = 15$ nm.

Calculations have shown that that for each $D_{Top\ gate}$ an optimal top gate side length A, that maximizes the ratio R, is found and is mainly equal to the island dimension. However, the top gate-to-island distance is the main impacting parameter on the transducer. The impact of decreasing the top gate-to-island distance ($D_{Top\ gate}$) on the top gate total parasitic capacitance ($C_2 + C_1 + C_3$), the top gate-to-island capacitance (C_G), the ratio (R) and the island total capacitance (C_Σ) is summarized in table 3.6.

Table 3.6 Impact of decreasing the distance $D_{Top\ gate}$ on the top gate total parasitic capacitance ($C_2 + C_1 + C_3$), the top gate-to-island capacitance (C_G), the ratio (R) and the island total capacitance (C_Σ).

	Decreasing $D_{Top\ gate}$
$\boldsymbol{C_2 + C_1 + C_3}$	Decreased slightly
$\boldsymbol{C_G}$ **or** $\boldsymbol{C_G/C_\Sigma}$	Increased
$\boldsymbol{R}$	Increased
$\boldsymbol{C_\Sigma}$	Increased
Sensitivity	Increased
Operating temperature	Decreased

Placing the top gate close to the island in order to increase C_G (or C_G/C_Σ) and R and thus the sensitivity, increases C_Σ and hence comes at the expense of the device operating temperature.

The island total capacitance is the main limiting factor in the implementation of a functionalized gate as a top gate. C_G cannot be tuned independently of C_1, C_2 and C_3. The top gate has to be placed not too close to the island, at the expense of the ratio R and Coulomb peak slope (the sensitivity), because it yields an enormous C_G, and not too far because the ratio R and the yielded sensitivity are decreased as a result of a decreased C_G (and also increased top gate parasitic capacitances C_1, C_2 and C_3 with decreasing the distance).. Therefore, a compromise has to be found for the top gate design. $D_{Top\ gate}$ has to be increased as low as possible to maximize the ratio and the top gate lever while keeping C_Σ small enough to allow the operation at room temperature. Lowering C_G and R will not impact the sensor a lot, since the DG-SET estimated sensitivity is sufficient for gas sensing applications.

The e-beam lithography tool in the *nanodamascene* fabrication process has a maximum alignment error within the ±50 nm range. Considering the top gate side length and top gate-to-island distance equal to respectively 20 nm and 15 nm, and TEOS as a dielectric, the

misalignment impact on top gate capacitances has also been studied within the mentioned range along XX' and YY' axis, as illustrated in Fig. 3.21. The top gate total parasitic capacitance together with the top gate-to-island capacitance, as well as the ratio as a function of the misalignment ΔY and the misalignment ΔX are shown in Fig. 3.22 and 3.23 respectively.

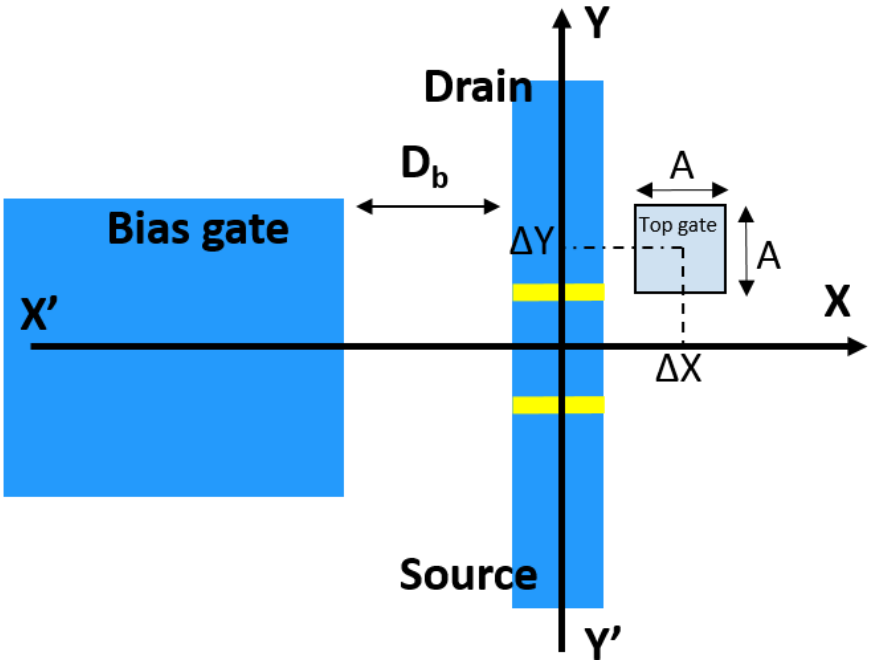

Figure 3.21 Top gate misalignment along XX' and YY' axis. Δ*X* and Δ*Y* denote the top gate deviation respectively along XX' and YY' axis.

Top gate fabrication misalignment has a strong impact on the yielded capacitance. For a misalignment of 50 nm along XX' or YY' axis, the ratio is reduced below 0.2. However, misalignment errors in the ±10 nm range does not take off more than 10% of the ratio. This means that if the misalignment error has to be kept below 10 nm otherwise it may lead to a reduced sensitivity and a strong device variability, which is easily possible with industrial UV lithography technology which has the overlay within few nm. This is due to the fact that the island is very closely located to the three other terminals (drain, source and gate electrodes).

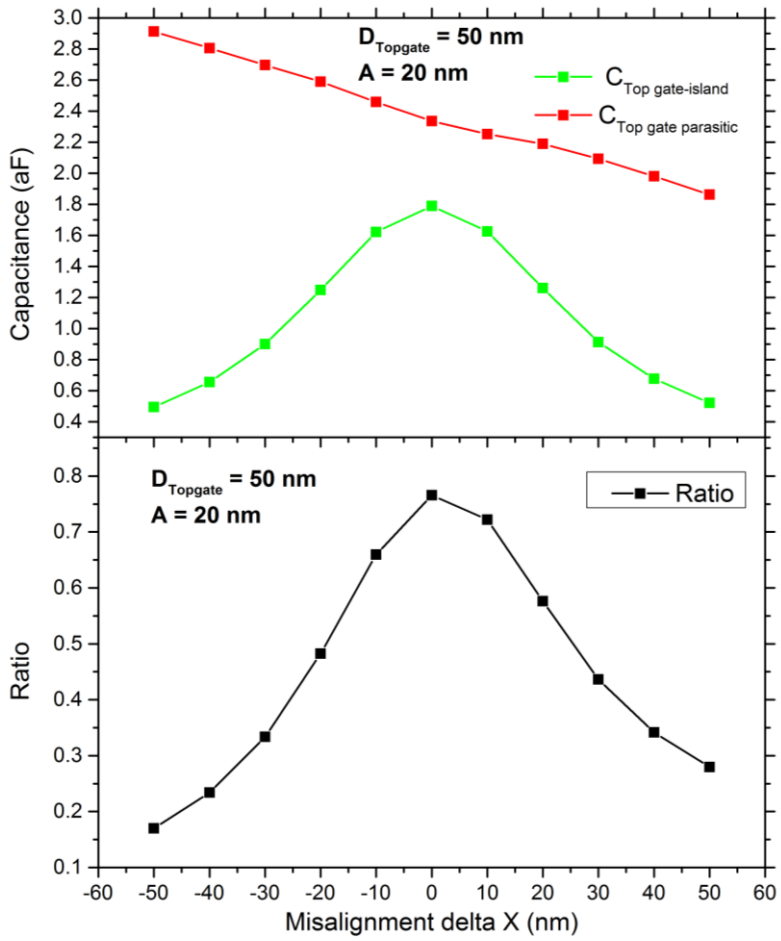

Figure 3.22 Impact of misalignment along XX' on top gate capacitances for $D_{Top\ gate} = 15$ nm and $A = 20$ nm. a) Top gate-to-island and top gate total parasitic capacitances *versus* misalignment along XX' axis. b) *R versus* misalignment along XX axis'.

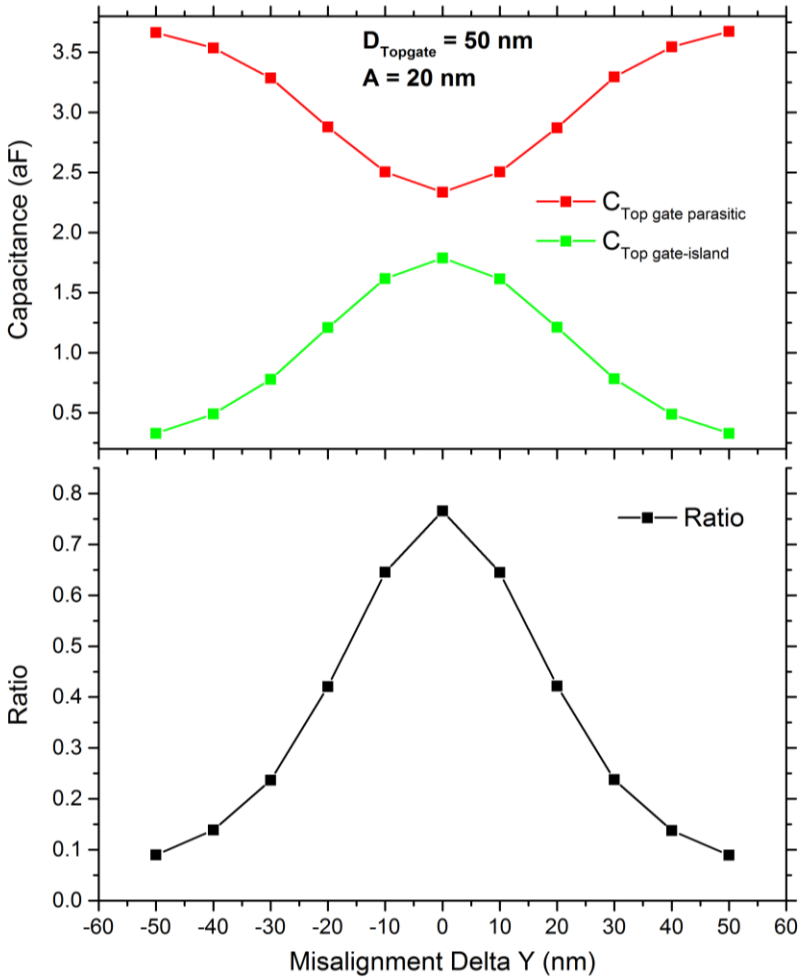

Figure 3.23 Impact of misalignment along YY' on top gate capacitances for $D_{Top\ gate} = 15$ nm and $A = 20$ nm. a) Top gate-to-island and top gate total parasitic capacitances *versus* misalignment along YY' axis. b) R *versus* misalignment along YY' axis.

Considering the calculated capacitances, listed in table 3.4, for parameter values listed in table 3.2, Coulomb oscillations at room temperature won't be observed, because the charging energy is smaller than the thermal energy $K_B T$. Island total capacitance can be reduced by thinning the structure more and downsizing the side gate width. From a fabrication point of view, for the former, this means that a very precise control over the CMP is needed. For the latter, it means that the alignment error of the island deposition process has to be greatly reduced.

3.4.2 DG-SET-based gas sensor response simulation

DC stationary simulations using a Monte Carlo simulator have been carried out in order to estimate the DG-SET based sensor sensitivity. SIMON [69], a single-electron tunnel devices and circuit simulator, based on Monte Carlo method has been chosen for the DG-SET current simulation because it allows easy and quick implementation of a compact model of the system composed by tunnel junctions, capacitors and voltage sources, using a graphic interface. SIMON also allows simulation of rare processes such as co-tunnelling by combining Monte Carlo and master equation methods. Although, the SIMON simulator does not take into account either thermionic emission currents or tunnel resistance variations with the voltage drop across it, it allows an analysis with sufficient quality to extract device sensitivity.

For Monte Carlo simulations, the considered values for C_S, C_D and C_B capacitances are different from those calculated in section 3.5.1 and listed in table 3.4. These values, obtained for the parameters listed in table 3.2, are above the limit of 3 aF for the island total capacitance. Simulations under SIMON have shown that no Coulomb oscillations can be distinguishable for these values.

For the following, these capacitances have been reduced to values, listed in table 3.7, that allow RT operation. For functionalized gate (top gate) capacitances (C_G, C_1, C_2 and C_3), those values corresponding to $D_{Top\ gate} = 55$ nm are considered because below this value the island total capacitance is increased too much to allow the operation at RT.

Table 3.7 Considered capacitances for Monte Carlo simulations.

Capacitance	Value (aF)
C_S	0.2
C_D	0.2
C_B	0.04
C_G	0.48
C_Σ	0.89
C_1	0.83
C_2	0.83
C_3	0.79
C_4	0.26
C_5	0.266

In SIMON, the functionalized gate is implemented as a "non-volatile node" with a background charge, which can be set to different values. Drain and source tunnel resistance have been set to 4.5 $10^7\Omega$ [22]. The source is taken as a common voltage reference for bias gate and drain polarization.

First, the Coulomb diamonds of a DG-SET model without parasitic capacitances, presented in Fig. 3.24, have been simulated at operating temperature of 10 K and for a null charge on the functionalized gate and presented in Fig. 3.253.a. The extracted traces at $V_{BS} = 0$ V and $V_{DS} = 330$ mV are shown respectively in Fig 3.25.b and Fig. 3.25.c. Extracted island total capacitance from Coulomb diamonds is equal to 0.43 aF. Coulomb oscillations are spaced by a period of 3.84 V, which in agreement with C_B. The noise seen in obtained characteristics comes for Monte Carlo method.

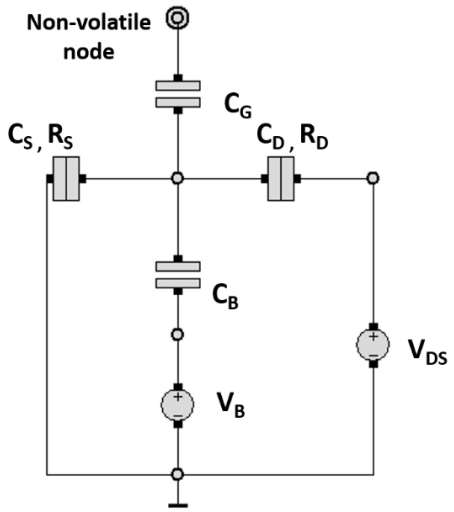

Figure 3.24 Circuit diagram of simulated DG-SET model without parasitic capacitances. The functionalized gate electrode is a "non-volatile node" with a pre-set background charge. The source is taken as a common voltage reference for bias gate and drain polarization.

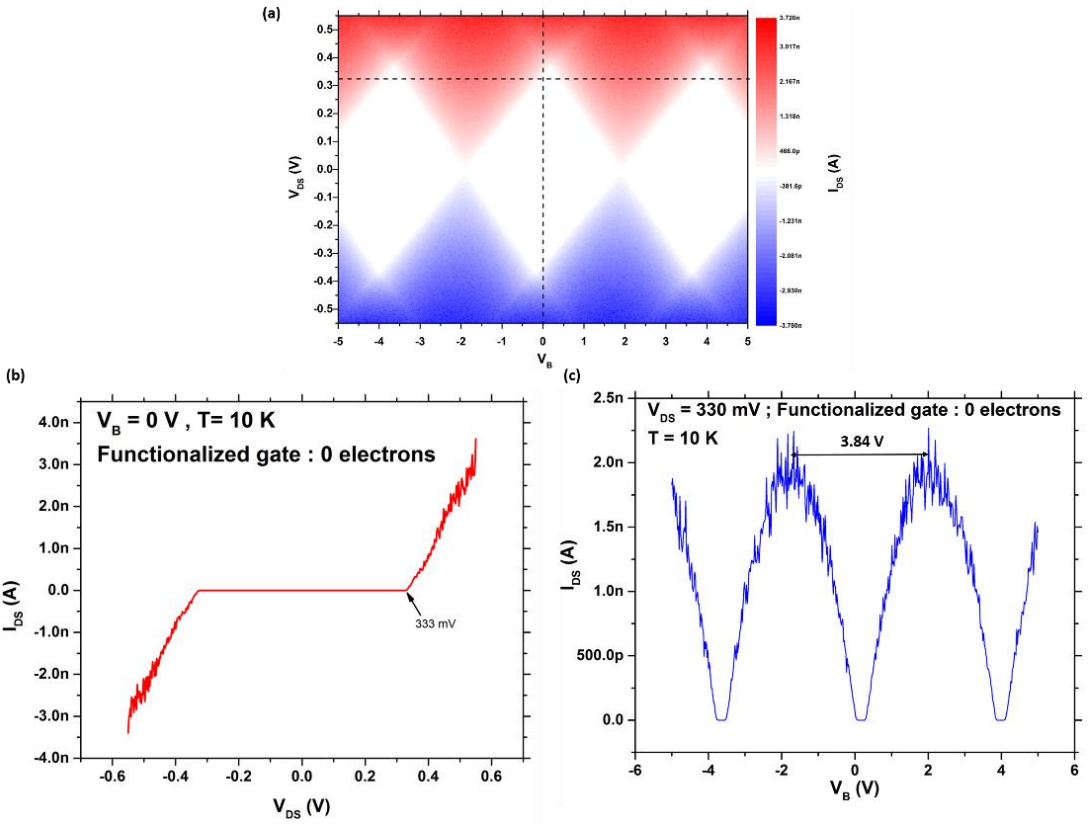

Figure 3.25 a) Simulated Coulomb diamonds of the DG-SET model without parasitic capacitances at 10 K and for null charge on the functionalized gate, from which line traces in b) and c) were extracted.

Simulation of the same model at 300 K has exhibited Coulomb oscillations, as can be seen in Fig. 3.26. At 300 K, the I_{DS} *versus* V_{BS} trace, shown in Fig. 3.26.b, exhibits a current offset, of nearly 600 pA, compared to Coulomb oscillations simulation at 10 K, which is due to more thermally activated tunnel current. The tunnel rate is increased by increasing temperature as can be seen through Eq. 3.16.

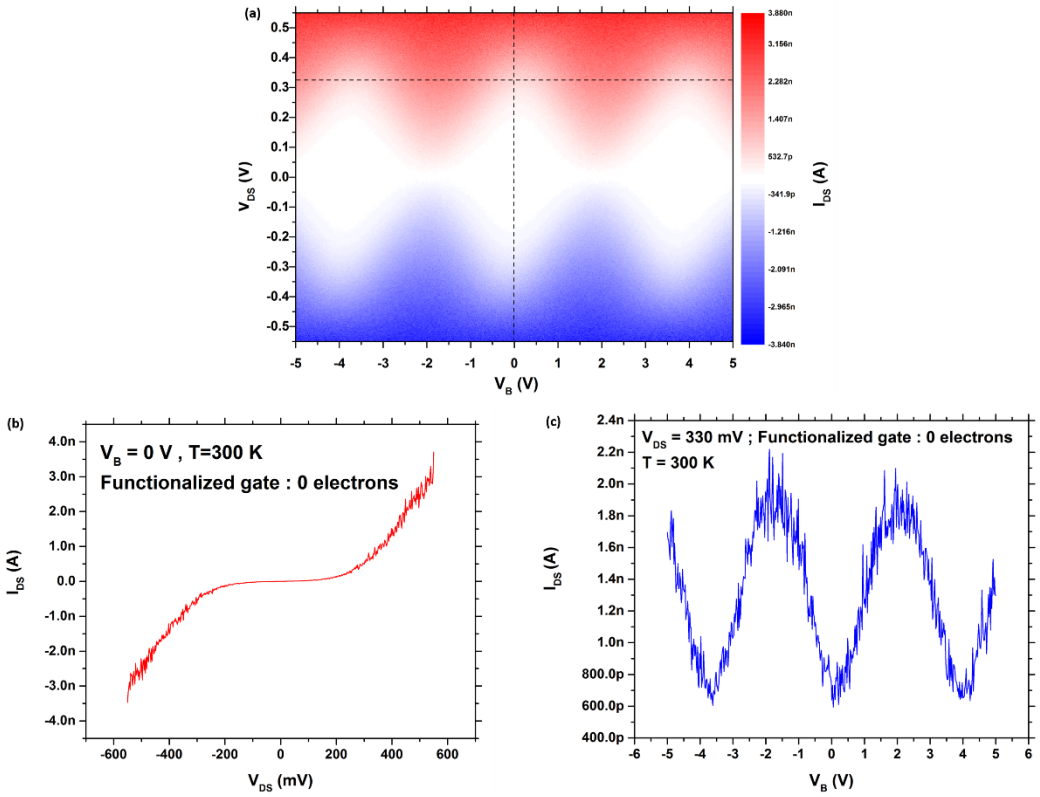

Figure 3.26 a) Simulated Coulomb diamonds of the DG-SET model without parasitic capacitances at 300 K and for null charge on the functionalized gate, from which line traces in b) and c) were extracted.

Coulomb diamonds of the DG-SET model with all the parasitic capacitances, C_1, C_2, C_3, C_4 and C_5, shown in Fig. 3.27, have been simulated at operating temperature of 10 K as well as 300 K, and are presented in Fig. 3.28 and Fig. 3.29.

As can be seen in line trace extracted at $V_{BS} = 0\ V$ from simulated Coulomb diamonds at 10 K, shown in Fig. 3.28.b, the voltage threshold for Coulomb blockade is reduced to 160 mV, compared to 330 mV for the DG-SET model without parasitic capacitances. This is due the increased island total capacitance. The effective island total capacitance extracted from the Coulomb diamonds, shown in Fig. 3.28.a, is equal to 0.8 aF. As can be seen in Fig. 3.28.c, the

impact of V_{DS} on Coulomb peaks slope is negligible. As V_{DS} increases the Coulomb peaks are widened and the maximum current is increased.

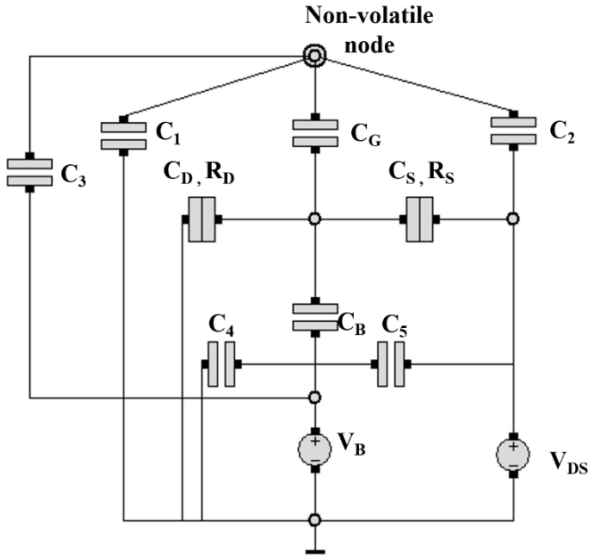

Figure 3.27 Circuit diagram of simulated DG-SET model with all the parasitic capacitances. The functionalized gate electrode is a "non-volatile node" with a pre-set background charge. The source is taken as a common voltage reference for bias gate and drain polarization.

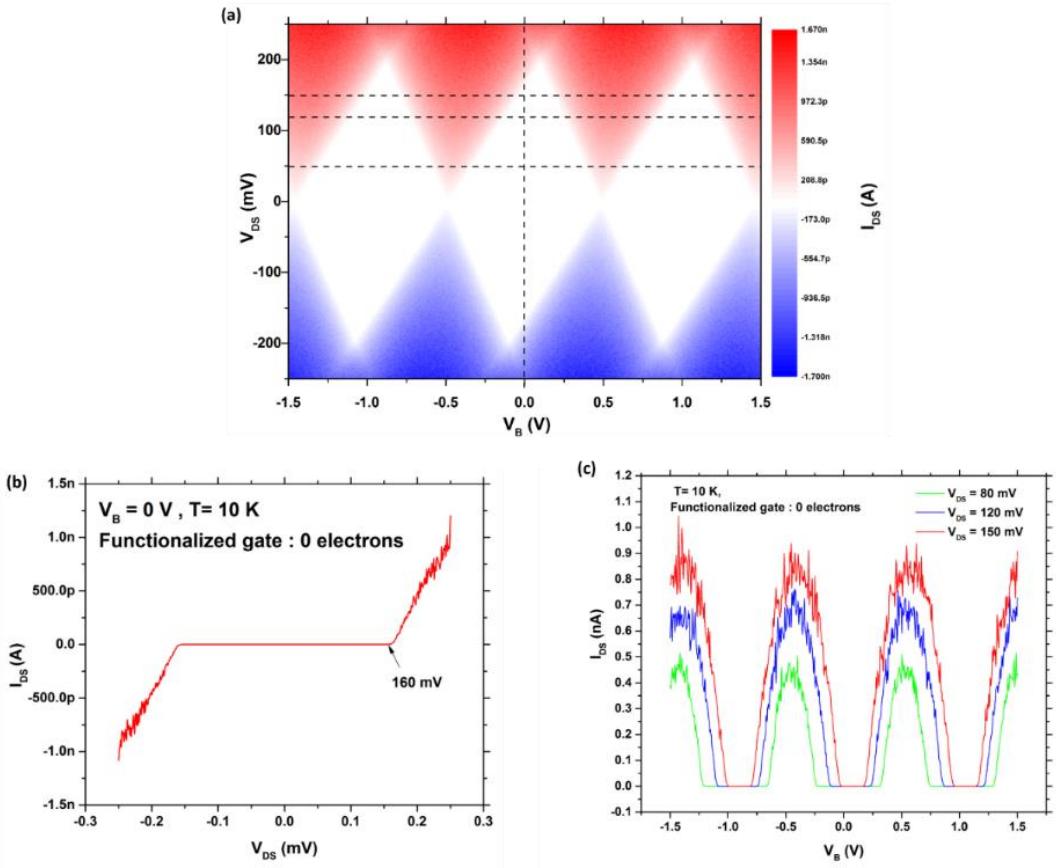

Figure 3.28 a) Simulated Coulomb diamonds of the DG-SET model with all the parasitic capacitances at 10 K and for a null charge on the functionalized gate, from which traces in b) and c) were extracted.

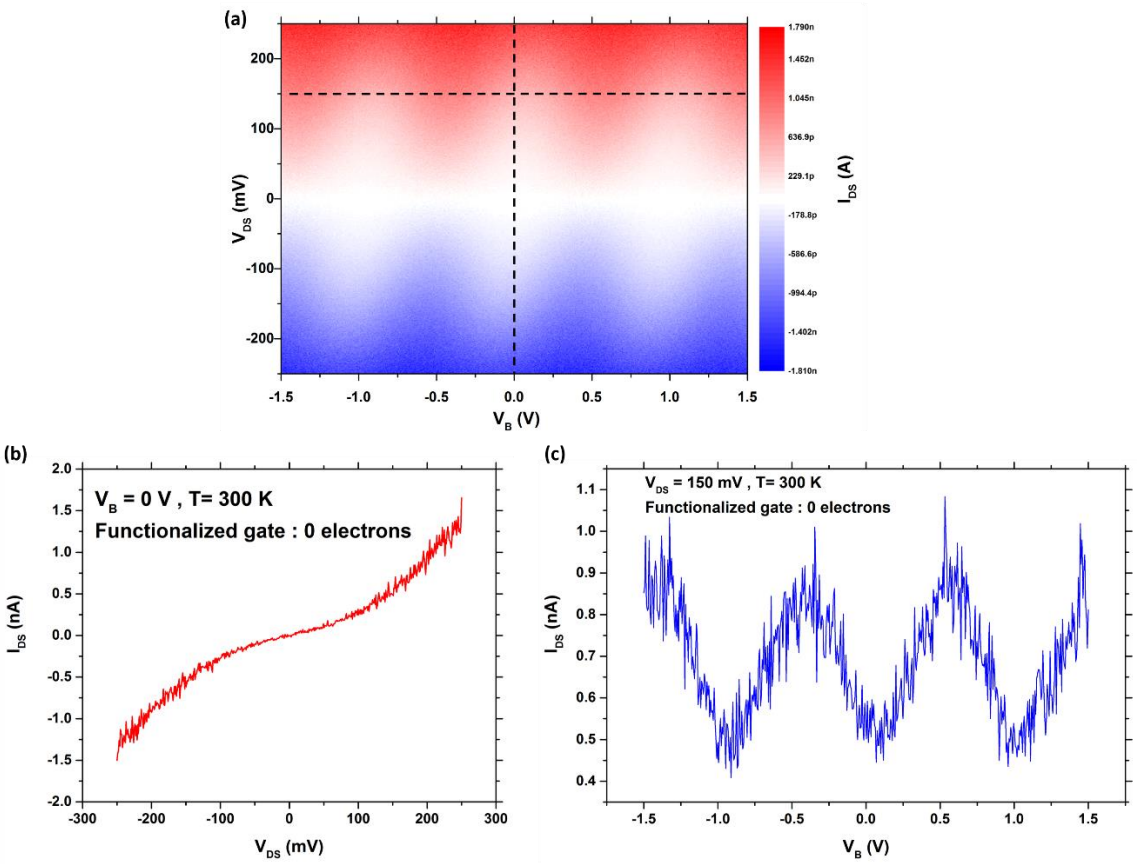

Figure 3.29 a) Simulated Coulomb diamonds of the DG-SET model with all the parasitic capacitances at 300 K, and for a null charge on the functionalized gate, from which traces in b) and c) were extracted.

Simulation of the DG-SET with all the parasitic capacitances at 300 K exhibited Coulomb blockade as shown in Fig 3.29. I_{DS} *versus* V_{BS} exhibits Coulomb oscillations with some current DC offset. The DG-SET with all the parasitic capacitances still can be operated at room temperature as a chemical sensor with captured charge coupled the island via the functionalized gate capacitance.

For sensing operation the DG-SET is polarized with a V_{DS} voltage slightly below the voltage threshold (threshold voltage of I_{DS} *versus* V_{DS} curve at $V_{BS} = 0$ V) to have only one electron flowing at the same time through the island from the source to the drain, which corresponds to the possible island charge states of 0 or 1 electron. Thus Coulomb oscillations will have the lowest DC offset current (corresponding to available energy levels compromised between source and drain Fermi levels), and the highest peak current level which is advantageous for the signal to noise ratio and read-out circuitry.

For sensitivity estimation, simulations of the DG-SET model with all the parasitic capacitances at 300 K for different values of the functionalized gate charge have been carried out. The drain is polarized below the Coulomb voltage (200 mV extracted from Fig. 3.28.a) at 155 mV. Each simulation is repeated ten times and the mean value of obtained current response is considered. Obtained data is presented in Fig. 3.30. I_{DS} at varying functionalized gate charge exhibits Coulomb oscillations. The sensitivity (current variation per aC unit of charge) is extracted from the Coulomb peak slope and is estimated to be about 900 ±25 pA/aC (145±4 pA/single electron). The standby state is defined as the transducer state in absence of the target gas to be detected. If we consider the standby period current level as the current corresponding to the bottom edge of the Coulomb peak slope (gas sensing configuration), the power consumption is equal to 86 pW (heating power is not taken into account). If the transducer is configured as an electrometer (the functionalized gate charge may vary in both directions), the transistor has to be polarized at the midway of the Coulomb peak slope. The power consumption corresponding to this configuration is equal to 110 pW

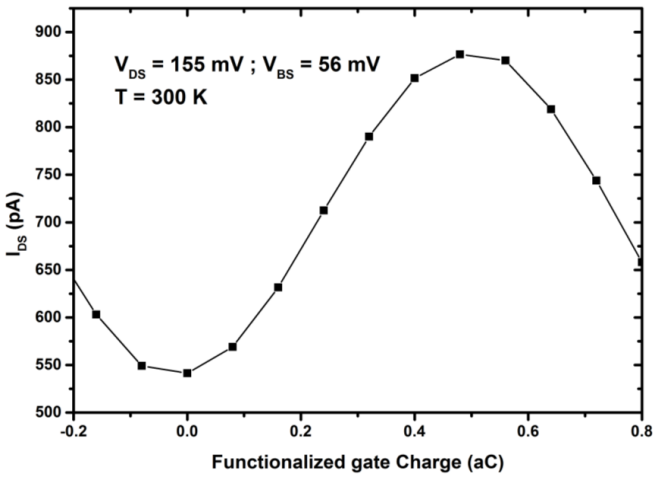

Figure 3.30 I_{DS} at varying functionalized gate charge simulated for the DG-SET model with all the parasitic capacitances at 300 K.

3.5 FD-SOI MOSFET-based gas sensor modelling and simulation

For the sake of simplicity, in the discussed model we suppose that the sensing material is conductive and neglect any capacitance through this layer. This case corresponds to the use of platinum as a sensing material for H_2 sensing, detailed in chapters 4 and 5. The floating functionalized gate surface charge/ potential, induced by gas adsorption, is coupled to the thin

Si FET channel through the front gate capacitance C_{oxf}. Variations in the sensing material surface charge will gate the transistor channel and yield variations in the current I_{DS}. The current variations are regarded as the sensor output. The substrate bias is used to operate the transistor in the sub-threshold regime when ${Q_{fg}}^0$ charge is present on the front gate in absence of the target gas. In other words, the back gate bias is adjusting the transistor transfer characteristics with respect to the functionalized gate potential so that the charge variation range ${Q_{fg}}^0 \pm \Delta Q_{fg}$, induced by gas molecules adsorption, corresponds to the linear regime of this characteristic.

For the case where the gas to be detected induces a negative charge supply to the sensing material surface, which corresponds to a positive charge change at the inner side of the front gate $(\Delta Q_{fg} > 0)$ e. g. H_2 detection by Pt, an n-type MOSFET is preferred, because detection events will correspond to an increase in the current I_{DS}. In absence of the gas to be detected, the transistor is operated at the bottom edge of the linear regime of the characteristics $I_{DS} - Q_{gf}$ to have the lowest possible current level, and thus the lowest power consumption during the standby period (absence of the gas to be detected).

The back gate bias does not only shift the front gate threshold voltage, but also may affect the subthreshold slope. In the following we carry out simulations according to the above presented model of the FD-SOI MOSFET-based gas sensor. The objective is to investigate the impact of the back gate bias, transistor channel dimensions and temperature on sensor sensitivity.

3.5.1 UTBB FD-SOI MOSFET model

Simulations are based on an analytical compact current model for a lightly doped short channel n-type UTBB FD-SOI MOSFET taken from [78, 79] and adapted to carry out drain current calculations with respect to the front gate charge. A simulator based on this adapted model has been implemented in Matlab and allows drain current calculations with respect to various variables such as temperature, channel width and length, silicon body thickness, back gate voltage, front gate voltage, drain voltage and front gate charge.

The implemented current model is an analytical compact charge-based, which is valid in all regions of the operation with back gate control and takes into consideration the effects of drain induced barrier lowering (DIBL), channel length modulation (CLM), saturation velocity, mobility degradation, quantum confinement, velocity overshoot (VO) and self-heating (SH)

effects. The detailed model can be found in [79]. The implemented analytical compact model is described in Appendix A.

3.5.2 UTBB FD-SOI MOSFET-based gas sensor response simulation

For the following simulations we considered a device with characteristics of an n-type FD-SOI MOSFET with back plane issued from 28 nm FD-SOI CMOS technology, fabricated by STMicroelectronics [80]. Simulated device characteristics are detailed in Appendix A. In the following, the impact of the channel length (L) and width (W), the back-gating bias (V_{gb}) and the temperature (T) are studied. V_{ds}, I_{ds}, ${Q_{fg}}^{0}$ and Q_{gf} stand for the drain voltage, the drain current, the front gate charge in absence of the target gas and the front gate charge (${Q_{fg}}^{0} \pm \Delta Q_{fg}$). The source is taken as a common voltage reference for back gate and drain polarization.

Simulated I_{ds} *versus* Q_{gf} curves for $V_{ds} = 0.1\ V$, $L = 30\ nm$ and $W = 0.5\ \mu m$, with back bias voltages V_{gb} varying from -3 to +3 V is presented in Fig. 3.31. As predicted, the back gate voltage allows to shift the obtained characteristics and adjust them as a function of ${Q_{fg}}^{0}$. The estimated Q_{gf} excursion window for sweeping the back gate bias from -3 to +3V is about 125 aC.

The sensor sensitivity is defined as the current variation per unit of front gate charge variation:

$$S = \frac{\mathrm{d}\, I_{ds}}{\mathrm{d}\, Q_{gf}} \tag{3.23}$$

Extracted sensitivities from data presented in Fig. 3.31 for V_{gb} varying from -3 to +3 V are quasi constant at varying V_{gb} from -3 to +3 V. Obtained sensitivities mean value over all characteristics equals to 1.8± 0.1 µA/aC.

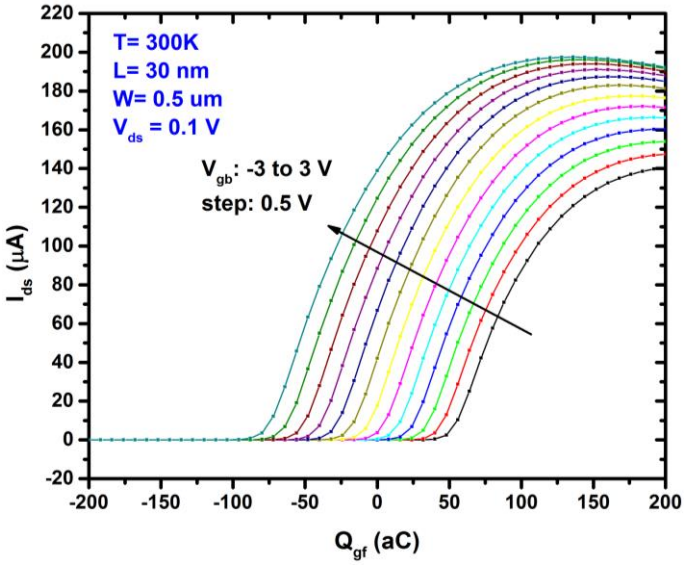

Figure 3.31 Simulated $I_{ds}\ versus\ Q_{gf}$ for $V_{ds} = 0.1$ V, $L = 30$ nm and $W = 0.5$ µm, with back bias voltages V_{gb} varying from -3 to +3 V.

If we consider arbitrarily that ${Q_{fg}}^0 = -25$ aC, the back gate has to be biased at 2 V to make the linear region of $I_{ds}\ versus\ Q_{gf}$ curve correspond to the front gate charge variations within the range -25 aC $\pm\ \Delta Q_{fg}$. Simulated $I_{ds}\ versus\ Q_{gf}$ curves for $V_{ds} = 0.1$ V, $V_{gb} = 2$ V, and $W = 0.5$ µm with varying channel length L from 20 to 40 nm are presented in Fig. 3.32.

With decreasing channel length the curve slope increases. As a consequence the sensor sensitivity increases, which is coherent. At the same time the current levels increase with decreasing channel length. Increased sensitivity by decreasing the length also comes with a shrinking of the excursion window of Q_{gf} (sensitivity range ${Q_{fg}}^0 \pm \Delta Q_{fg}$). Extracted sensitivities at varying length are presented in Fig. 3.33 and are in the µA/aC range. Considering these values, the channel length can be relaxed to obtain a wider sensitivity range, lower current levels with still appreciable current change for the front gate charge variations.

Considering the standby current level corresponding to the bottom edge of the slope (gas sensing configuration) and a device with $L = 30$ nm and $W = 0.5$ µm, biased at $V_{ds} = 0.1$ V and $V_{gb} = 2$ V , and ${Q_{fg}}^0 = -25$ aC, the power consumption is estimated to be 1.23 µW (heating power is not taken into account). If the device is configured as an electrometer, the power consumption is estimated to be 6.43 µW.

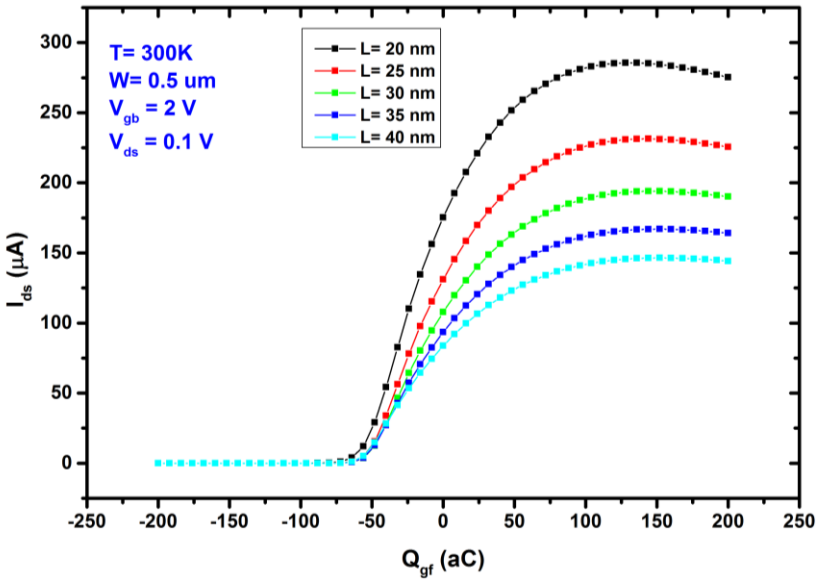

Figure 3.32 Simulated I_{ds} $versus$ Q_{gf} curves for $V_{ds} = 0.1$ V, $V_{gb} = 2$ V, and $W = 0.5$ µm with varying the channel length L from 20 to 40 nm.

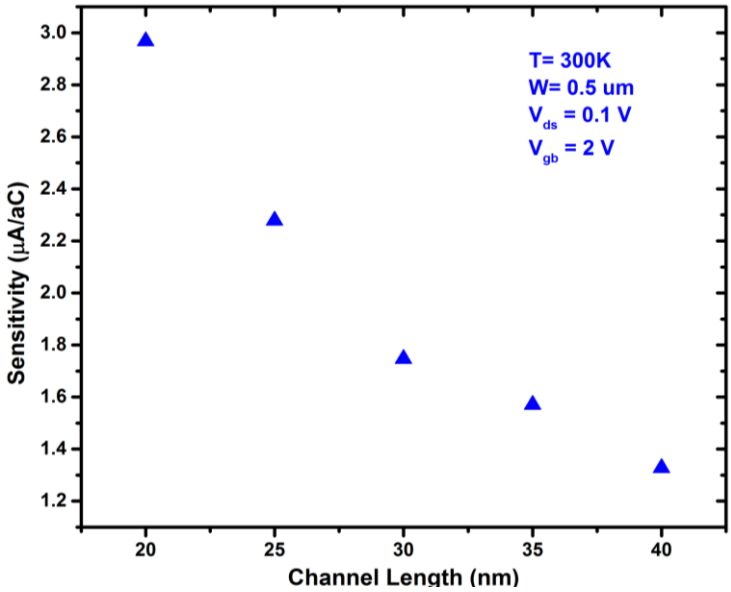

Figure 3.33 Extracted sensitivities at varying channel length for $V_{ds} = 0.1$ V, $V_{gb} = 2$ V, and $W = 0.5$ µm.

To investigate the impact of the channel width the current I_{ds} as a function of Q_{gf} has been simulated for $V_{ds} = 0.1$ V, $V_{gb} = 2$ V, and $L = 30$ nm with channel width W varying from 100 to 500 nm. Obtained I_{ds} $versus$ Q_{gf} are presented in Fig. 3.34. Extracted sensitivities are quasi constant, with a mean value equal to 1.8 ± 0.1 µA/aC. The sensitivity is not affected by varying

the channel width. However, with decreasing channel width the current decreases and the saturation of the curve is obtained faster which shrinks the excursion window of Q_{gf} (sensitivity range ${Q_{fg}}^{0} \pm \Delta Q_{fg}$). The targeted current levels and excursion window have to be taken into consideration in the channel width tuning, but still the latter parameter seems to have the most important impact.

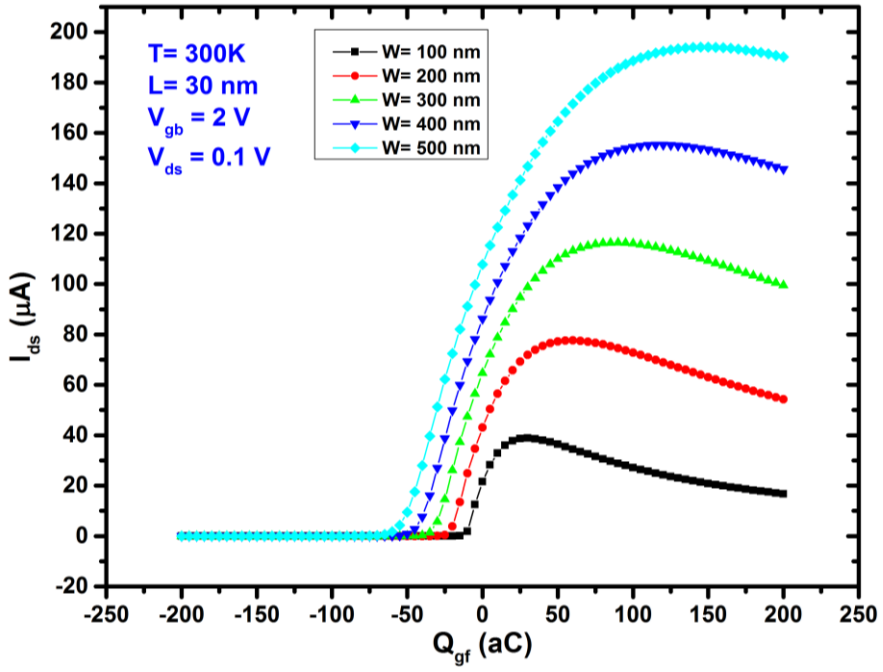

Figure 3.34 Simulated I_{ds} $versus$ Q_{gf} curves for $V_{ds} = 0.1$ V, $V_{gb} = 2$ V, and $L = 30$ nm with varying the channel length W from 100 to 500 nm.

The impact of the operating temperature has been investigated. The sensor response at varying temperature has been simulated for $V_{ds} = 0.1$ V, $V_{gb} = 2$ V, and channel parameters $L =$ 30 nm, $W = 0.5$ µm, with varying temperature and obtained I_{ds} $versus$ Q_{gf} are presented in Fig. 3.35. With increasing temperature I_{ds} $versus$ Q_{gf} are very slightly shifted toward negative Q_{gf} with a negligible impact on curves slopes (sensitivities).

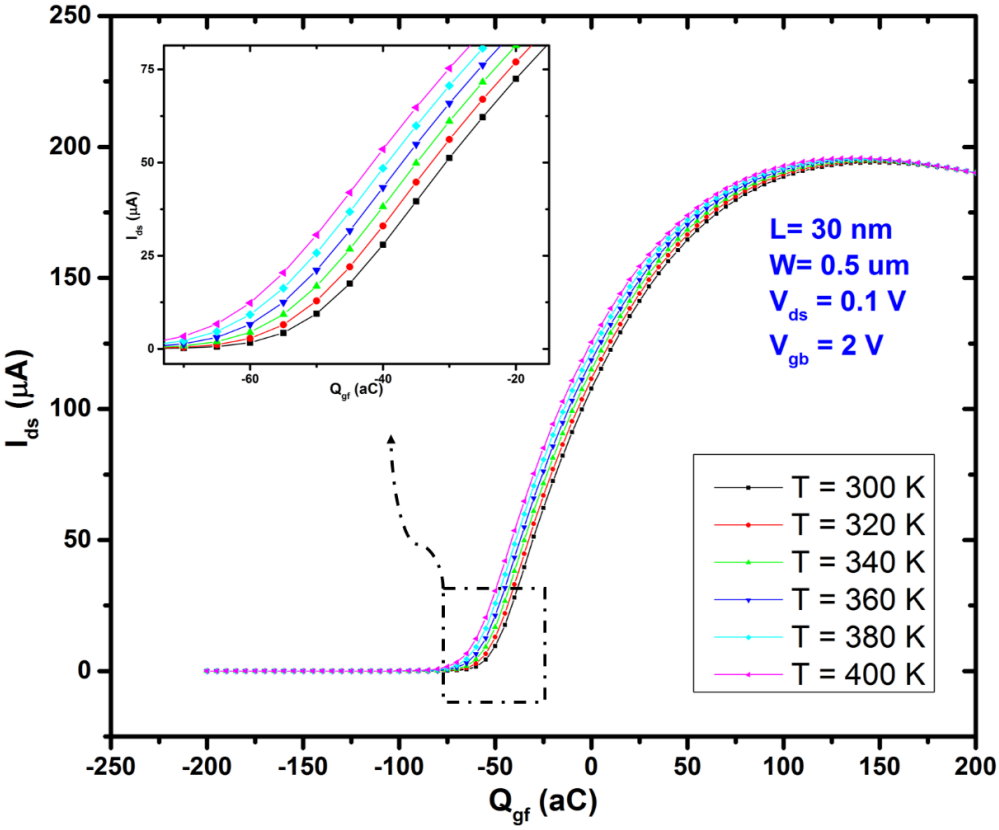

Figure 3.35 Simulated I_{ds} $versus$ Q_{gf} curves for $V_{ds} = 0.1$ V, $V_{gb} = 2$ V, and channel parameters $L = 30$ nm, $W = 0.5$ µm, with varying operating temperature.

3.6 Conclusion

Double gate–transistors are of great interest because they offer the possibility to incorporate two different gate electrodes without any need for an airgap structure. The introduced concept opens the door not only to gas sensors but also to biochemical sensing applications.

DG-SETs are very attractive because of their small size and their hyper-sensitivity down to the single electric charge. For the studied DG-SET-based gas sensor, the functionalized gate capacitance C_G, as well as all the parasitic capacitances increase the island total capacitance at the expense of the operating temperature. All of them impact the DG-SET sensitivity since it depends on the functionalized gate lever C_G/C_Σ and the ratio R.

Calculations have shown that that for each $D_{Top\,gate}$ an optimal top gate side length A, that maximizes the ratio R, is found and is mainly equal to the island dimension. However, the top gate-to-island distance is the main impacting parameter on the transducer.

Therefore, a compromise has to be found for the top gate design. $D_{Top\ gate}$ has to be increased as low as possible to maximize the ratio and the top gate lever while keeping C_{Σ} small enough to allow the operation at room temperature. Lowering C_G and R will not impact the sensor a lot, since the DG-SET estimated sensitivity is sufficient for gas sensing applications.

The impact of the top gate misalignment error was found critical because it dramatically increases the top gate parasitic capacitances. But with industrial lithography tools, the error can be kept low enough (10 nm) to obtain acceptable ratio R and not to degrade the sensitivity. The sensitivity calculation allows optimal sizing of the sensing material surface area, and estimation of sensitivity as output current per unit of concentration.

Extracted sensitivity and power consumption for a DG-SET-based gas sensor with optimized top gate geometry parameters (see section 3.4.1) are 900 pC/aC and 86 pW respectively.

FD-SOI MOSFETs are also very promising for implementation as a gas sensor. FD-SOI CMOS is a mature technology with almost ideal subthreshold slope especially with UTBB devices. The expected sensitivity of such device has been simulated and estimated values for the modelled device parameters are within few µA per aC of charge variation which is more than sufficient for sensing knowing the high signal-to-noise ratio of these types of transistor. The device channel width and length have to be tuned with regards to the desired sensitivity, sensitivity range (excursion window) and current levels (power consumption). Extracted sensitivity and power consumption for a FD-SOI MOSFET-based gas sensor with $L = 30$ nm and $W = 0.5$ µm, and biased at $V_{ds} = 0.1$ V (see section 3.5.2) are 1.8 µC/aC and 1.23 µW respectively.

Extracted sensitivities and power consumption values for both of the simulated DG-FET and DG-SET are summarized in table 3.8. From energy budget point of view, the DG-SET has about 4 orders of magnitude lower power consumption that the DG-FET, thanks to the ultra-low current levels driving the SETs, inherent to the fundamental of their operation based on the transport of reduced number of electrons. However, from sensitivity point of view, the DG-FET (FD-SOI FET) was found 3 orders of magnitude more sensitive than the DG-SET thanks to the ideal sub-threshold slope. The DG-SET was disabled in term of sensitivity because of the top gate-to-island distance trade-off made to allow RT operation at the expense of the top gate-to-island capacitance and ratio R. The implementation of a top gate with pushing the sensitivity to

its maximum while having a RT operation is challenging because of the contribution of C_G and all the parasitic capacitances to the total effective island capacitance.

The estimated DG-SET power consumption is unmatched in the state-of-the-art of FET gas sensor technology. However, the fabrication technology has to be optimized to achieve RT operated devices.

Table 3.8 Comparison between simulated DG-SET and DG-FET in terms of sensitivity and power consumption.

	FD-SOI FET	**DG-SET**
Sensitivity (µA/aC)	1.8	$9\ 10^{-4}$
Power consumption (µW)	1.23	$8.6\ 10^{-5}$

Catalytic MOSFETs and SG-FETs have power consumption (transducer only) typically ranging from few tens to 100 µW [15, 35, 55, 71, 73]. Estimated FD-SOI FET power consumption is one order of magnitude lower than the state of the art in FET-based gas sensor technology. The transducer power consumption, with FD-SOI FETs, is reduced at least one order of magnitude in comparison to typical catalytic MOSFETs and SG-FETs-based gas sensors. The estimated FD-SOI MOSFET-based gas sensor power consumption is for a device with a channel width of 500 nm. It can be reduced by a factor of 5 if the channel width is reduced down to 100 nm ($L/W = 5$). The FD-SOI FETs are very promising for integration as a gas sensor for both of sensitivity and transducer power consumption motivations. Moreover, the high sensitivity of such devices may lead to a reduction in the needed sensing material area. In consequence, the needed power for heating the sensing material is reduced.

CHAPTER 4 Top-gate functionalization

4.1 Introduction

Both forms of gas molecules adsorption on solids, chemisorption run by ionic bonds and physisorption run by Van der Waals interactions, induce modifications of surface charge and thus a change in surface potential (can also be seen as a material work function variation). The effect is stronger in case of chemisorption compared to physisorption, since a partial charge transfer occurs and adsorbates are in a charged state. This potential change induced by gas molecules adsorption or desorption, if capacitively coupled to a transistor channel, affects the channel conductance and yields a current variation.

This has been achieved by making the inner surface of field-effect transistor (FET) gate accessible to gas species by either a permeable-to-hydrogen-atoms gate electrode made of catalytic metals, in so-called "Lundström" MOSFETs (catalytic MOSFETs) or by a suspended gate with a sensitive layer deposited on the outer surface, in suspended gate-FET (SG-FET)-based gas sensors [12, 42] (see section 2.5). In both cases the induced potential shift acts as an artificial voltage which is added to potentially applied gate voltage (external voltage source) and affects the conductance of the transistor channel [12, 42].

Catalytic MOSFETs are usually operated at temperatures in the range of 100–200 °C [15], and limited to detection of H_2 and hydrogen containing gases, such as ammonia, hydrogen sulphide, ethylene and ethanol [54, 56], since these molecules can be adsorbed and dissociated on the surface of catalytic metals. In contrast, SG-FET-based gas sensors have been demonstrated to detect a broad range of gases [12, 42] such as CO [45, 71], H_2 [16, 24, 72, 73], thanks to flexibility in sensitive layer choice and integration, and operate at RT or slightly above.

However, the integration of these sensors is complex mainly because of the necessity to implement a suspended gate electrode with the sensitive material deposited on the back side. The transistor channel width to length ratio has to be increased to overcome the poor transconductance due to the very low capacitance across the airgap [41, 42], which is a limitation towards high integration density.

As discussed in section 3.3, an alternative to these limitations is the use a double gate-FET (DG-FET) as a transducer. The general concept is to incorporate a functionalized gate with a dedicated gas-sensitive material and a control gate. The control gate is biased in order to control the operation point of the transistor, while the functionalized gate is a floating gate electrode with a dedicated sensitive material deposited on top of it. Such a configuration of the functionalized gate allows a better transconductance which yields a larger current variation for functionalized gate potential variations when the transistor is biased to operate in the linear region of the transfer characteristics. This configuration is illustrated in Fig. 4.1 for a FD-SOI MOSFET where the functionalized gate is the front gate electrode covered with the sensing layer and left floating (no biasing), and the back gate plays the role of the control gate. Knowing the surface charge variation of the floating functionalized gate of a DG-FET or a DG-SET, the channel conductance variation can be estimated.

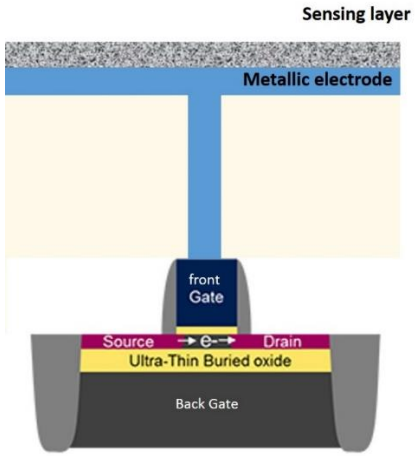

Figure 4.1 Cross section schematic of a DG-FET-based gas sensor realized with an FD-SOI MOSFET showing the sensing pad connected directly to the front gate of the transistor. Adapted from [23].

Very recently, Han *et al.* reported a chemically gated FET gas sensor, based on a normally off FET with a floating SnO_2 gate for NO and O_2 sensing. The authors used a honeycomb like structured Si channel with a conformal 2D tin oxide film on top, as a floating gate electrode. The transistor channel is patterned as a honeycomb to increase the specific sensing surface of the overlying SnO_2 layer [81]. Owing to their high surface to volume ratio, 2-D or 1-D nanostructured materials have been heavily used in gas sensing devices mainly as chemoresistors [50], as an effective way to increase the specific sensing surface. This allowed

enhancing the sensitivity and reducing the operating temperature, since the collected chemical signal is increased.

In this chapter, a novel concept to increase the specific surface of the sensing layer, useful for implementation with FET-based sensors, is presented. We propose a gate electrode surface texturing process by the deposition of Multi Wall-Carbon Nano Tube (MW-CNT) networks using spray coating of CNTs suspension.

A new technique to investigate gas sensitivity of materials based on measurement of material surface charge/potential variation induced by gas molecules adsorption is also presented. The technique gives the material surface charge. Surface charge measurement has been applied to investigate Pt sensitivity to hydrogen.

Pt as a dense thin layer as well as in combination with MW-CNT networks has been used as a sensitive material for hydrogen sensing. The sensitivity of Pt layers deposited on bare metallic electrodes has been investigated with the surface charge measurement technique. Estimated Pt sensitivity to hydrogen was used for the sizing of a sensing pad suitable for implementation with either a DG-SET or a DF-FET.

4.2 H_2 sensing with Pt

4.2.1 Pt interactions with hydrogen and oxygen

A well-known property of hydrogen molecules is its ability to dissociate into H atoms at the contact of platinum surface. The single H atoms interacts quite strongly with the Pt surface leading to the process of dissociative chemisorption with typical binding energies ranging between 50 and ~150 kJ/mol [47].

However, two possible types of hydrogen adatom chemisorption on Pt surfaces have been observed distinguishable by their impact on Pt work function and conductivity called the r-type adsorption and s-type adsorption [82]. The former increases the work function and the resistance. While the latter decreases the work function and the resistance. Same observations have been obtained for Ni and Pd.

The chemisorbed H adatom by r-type adsorption is slightly negatively polarized by 0.02 in units of elementary charge, hence the r-type adsorption increases the work function. The r-adatom

stands in an equilibrium right above a Pt ion at a distance evaluated at 1 Å outside the electronic surface [82].

The s-adatom is positively charged and always associated with a dipole moment of the order of 0.06 D. The s-type adsorption is interstitial and standing in an equilibrium position 0.5 Å inside the electronic surface [82]. This form of adsorption, leading to a decrease in the work function has been reported as the mechanism behind the detection of hydrogen by catalytic MOSFETs as well as Pt SG-FETs [16, 24, 55, 83]. This means that the chemisorption of H atoms at the Pt surfaces or the Pt/SiO_2 interface is an s-type adsorption in the temperature range of detection.

These adatoms are strongly electropositive therefore their electrons are partially transferred to the Pt, i.e. the chemical binding between the hydrogen and platinum atoms is polarized due to the electronegativity difference and thus the electrons forming the bond are attracted more to the Pt atom. Hydrogen chemisorption on Pt gives rise to a decrease in Pt work function (potential shift) [12, 24, 84]. Similarly to hydrogen, oxygen molecules adsorb dissociatively on Pt surfaces in the form of single isolated atoms. Since the oxygen atoms are strongly electronegative, the partial electron transfer occurs from Pt to the oxygen adatoms. Oxygen chemisorption gives rise to an increase of Pt work function (potential shift) [12]. Hydrogen and oxygen adsorption on Pt, illustrated in Fig 4.2, have opposite effects.

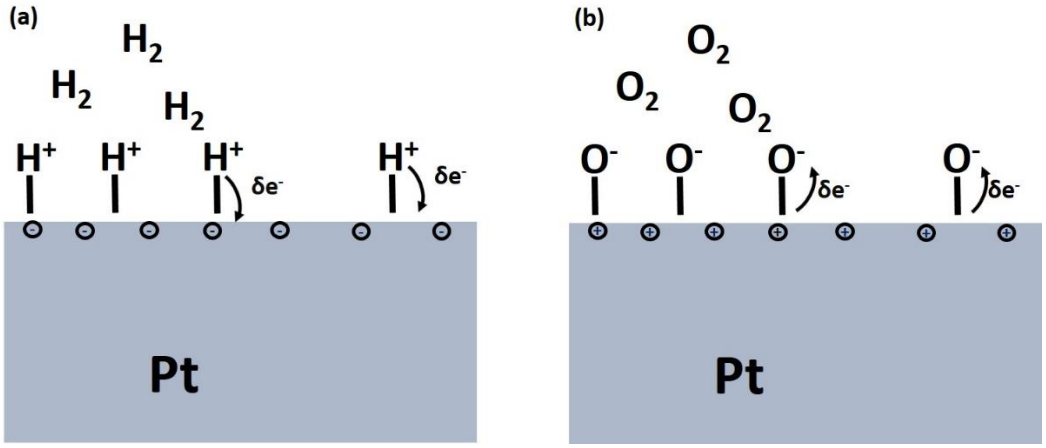

Figure 4.2 Schematic representation of hydrogen and oxygen molecules adsorption on Pt surfaces showing a partial charge transfer. a) H_2 dissociative chemisorption on Pt surface showing a partial electron transfer. b) O_2 dissociative chemisorption on Pt surface showing a partial electron withdrawing.

Another noteworthy property of adsorbed hydrogen atoms is their ability to be dissolved by Ti, V, Zr, Nb, Hf, Ta, and, "most notably, Pd" [47]. The H adatoms migrate through the topmost surface layer of catalytic metals such Pt and Pd, and accommodate in subsurface and bulk sites.

4.2.2 Pt as a sensing layer for H_2

Pd has been shown highly sensitive to H_2 and is widely used in catalytic MOSFET hydrogen sensors. However it has been shown that under high concentration of hydrogen, it exhibits blister formation and response degradation and long-term stability issues [24, 42]. Pd blistering is a result of lattice expansion and mechanical stresses induced by hydrogen molecules phase transition into an absorbed hydrogen atom taking place at the surface [85, 86].

Pt has a lower sensitivity to H_2 than Pd [54, 85, 87], but it is stable and does not exhibit blister formation even at 10% H_2 gas at 150 °C [85].

Pt has a larger H_2 sensitivity and shorter response and recovery times than Ir [24]. Schnargal et al. and Wilbertz *et al.* reported Pt response times (the time for reaching 90% of the steady state signal) to be below the 10 s at RT [16, 24].

The presence of humidity is reported shortening the recovery time of Pt but to decrease its response [24]. Platinum has been used to detect hydrogen in combination either with catalytic MOSFETs [15, 40, 54] or SG-FETS [16, 24, 72, 73]. With the latter, reliable sensitivity to hydrogen at temperatures down to RT have been demonstrated. For instance, Scharnagl *et al.* has reported a Pt SG-FET operated at 30 °C and 0% RH (relative humidity) [24], whom response signal to 0.1% H_2 and dependence on concentration from 50 ppm to 2% are shown in Fig. 4.3.

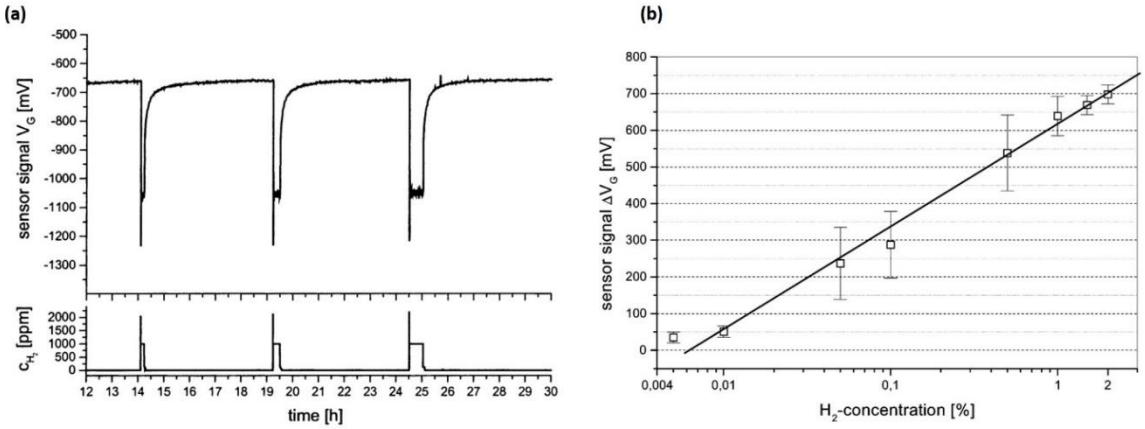

Figure 4.3 Pt-SG-FET sensitivity to H_2 at 30 °C. a) Pt-SG-FET response signal to 0.1% H_2 at 30 °C and 0% RH. b) H_2 concentration dependence of the Pt-SG-FET response at 30 °C and 0% RH. Reproduced from [24].

Wilbertz *et al.* reported the integration of a Pd-catalytic MOSFET with a Pt-SG-FET on a single chip in CMOS technology [16]. A cross section schematic of the paired sensor system as well as response to varying H_2 concentrations at 100 °C are shown in Fig. 4.4. The Pd Lundström FET sensitivity starts saturating at high hydrogen concentrations around 0.5% while the Pt-SG-FET sensitivity stays linear up to 2% (the highest measured concentration reported by the authors), as can be seen in Fig 4.4.c.

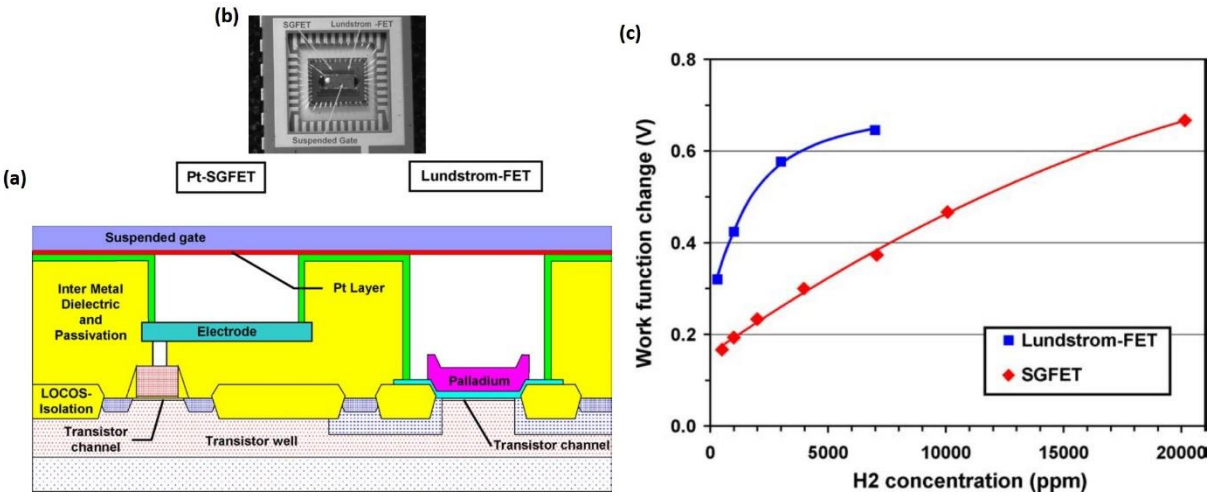

Figure 4.4 a) Response as a function of hydrogen concentration at 100 °C in synthetic air of the Pd Lundström-FET and the Pt-SG-FET. b) Cross section schematic of the combined Pd Lundström-FET/ Pt-SG-FET sensor system. c) Top view image of the sensor chip with the combined Pd Lundström-FET/ Pt-SG-FET devices. Reproduced from [16].

Several authors reported a linear Pt response to the logarithm of the hydrogen gas concentration as either a SG-FET [12, 24] or a catalytic MOSFET [84, 88]. Some authors reported that Pt response to H_2 starts to saturate for concentration above 2% [12, 24].

However, it has been observed that Pt exhibits unstable response to hydrogen for temperatures above about 60 °C [12, 72]. The Pt surface work function signal, under exposure to hydrogen, drifts strongly to its original baseline for temperatures above about 60 °C, as can be seen in Fig. 4.5. It is also known that after the first exposure of Pt to hydrogen, a baseline drift is observed. Afterwards a stable baseline is observed [24]. A baseline drift is also observed when Pt is exposed to high H_2 concentrations [16].

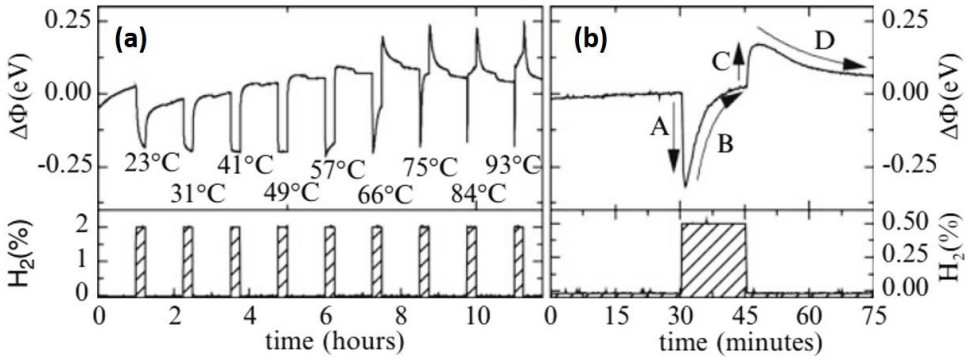

Figure 4.5 a) Pt surface work function change under exposure to 2% H_2 in synthetic air at 30% RH and different temperatures. b) The drift behaviour of Pt work function in hydrogen containing air with 30% RH at 75 °C. Reproduced from [12].

4.3 Sensing electrode surface texturing with CNT networks

Since their discovery in 1991, CNTs have found widespread interest either for their electrical or mechanical properties. These 1-D nanomaterial made up entirely of carbon is obtained by bending one or more sheets of single-atom-thick (called graphene sheets), into a cylindrical shape, as illustrated in Fig. 4.6. So they exist as single-walled nanotubes (SW-CNTs) or multi-walled nanotubes (MW-CNTs). Depending on the chirality along the single carbon thick sheet, SW-CNTs may have metallic or semiconducting behaviour. In contrast, MW-CNTs are metallic.

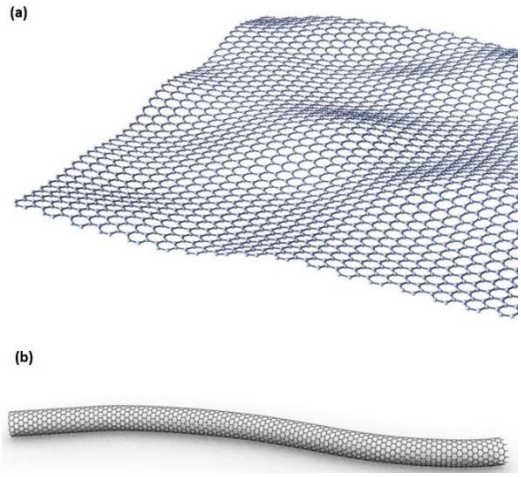

Figure 4.6 3D schematic representations of carbon nanomaterials. a) A sheet of graphene. Reproduced from [25]. b) A single-walled CNT. Reproduced from [26].

CNT-FET-based gas sensors, where a single SW-CNT is contacted between two metallic electrodes, on a dielectric/Si substrate acting as a bottom gate, have been extensively studied (see section 2.6). However, fabrication techniques for single SW-CNT positioning as well variability in fabricated transistors are limitations towards sensors mass production. Recently, random SW-CNT networks, have been used as a transistor channel for gas sensing applications. By controlling the areal densities, a global semiconducting behaviour can be achieved. More details can be found in [60].

A CNT network can be regarded as a thin film of randomly distributed CNTs laid horizontally on the surface of the substrate. Deposition of CNT networks, also referred to as "CNT mats", has been achieved by a solution based film coating techniques such as drop coating, ink jet printing and spray coating [60, 89, 90]. It allows to uniformly lay down the CNT dispersion on the substrate. A solution-based deposition is advantageous because it is low temperature process, allows the deposition on arbitrary substrates, does not need a high-vacuum system, which reduces costs significantly, and has a high deposition rate [91]. In this work, MW-CNT mats have been used for the electrode surface texturing concept. MW-CNT networks have served as a conducting electrode frame for functionalization.

4.3.1 Surface texturing using MW-CNTs concept

The intuitive approach for functionalized gate implementation is to have a metallic pad with the sensing layer overlying as a dense film. An alternative approach is to use a surface texturing technique to increase the specific sensing surface. We propose a gate electrode pad surface texturing process by the deposition of Multi Wall-Carbon Nano Tube (MW-CNT) networks using spray coating of CNTs suspension. The sensing material is deposited on top of the MW CNTs porous film overlying on the metallic pad. We take advantage of the conducting behaviour and the high surface to volume ratio of the MW-CNTs.

The texturing process starts with MW-CNT suspension preparation. Then, the suspension is sprayed over the metallic pad. Afterwards, the gas- sensitive material can be deposited. Pt has been evaporated on top of the textured metallic pad to yield a Pt covered MW-CNT porous film. In the following, the suspension preparation and developed spray coating process are detailed. Then, obtained textured sensing layers are presented.

4.3.2 MW-CNTs dispersion

CNTs are naturally grouped in bundles by Van der Waal forces. The most challenging issues to overcome by the dispersion process is to “break” these bundles to obtain a bundle free, and long-term-stable CNT suspension. A good wettability of the metallic surface by the CNT solution is also preferred for spray coating purposes.

NMP (1-methyl-2-pyrrolidinone) has been widely used and yields stable CNTs suspension even without a need of surfactants [92]. Water is a good polar solvent but it has a bad wettability of Au because of its hydrophobic behaviour. It also needs surfactants to yield stable and bundle free CNT suspensions. Methanol is the most polar over the commonly used organic solvents such as isopropanol, ethanol, acetone. It also exhibits good miscibility with water and wettability of Au. Both of methanol:H_2O and NMP have been investigated for CNT suspension preparation using commercially available pristine MW-CNT powder from Cheap Tubes Inc.. Properties of the MW-CNT powder are summarized in table 4.1.

Table 4.1 Properties of commercially available CNTs used in suspension preparations.

Property	Value
CNT type	Pristine Multiwalled-CNTs
CNT length (µm)	0.5-2
CNT diameter (nm)	13–18
Purity (%)	≥99

In a first step, MW-CNT powder with a very precise weight is added to the solvent (or solvent with surfactants) in a falcon tube (see Fig. 4.7.a). In a second step, the solution is sonicated using a sonicator probe for 5 min. The falcon tube is placed into a water bath with ice cubes to allow cooling during sonicating (see Fig. 4.7.b). A homogenous dark solution is obtained (see Fig. 4.7.c).

Methanol and methanol:H_2O, with SDS surfactants, yielded unstable suspension over time and the CNTs quickly agglomerate and sediment inside the falcon tube. Stable suspension has been obtained only for methanol:H_2O ratio of 1:1 with SDS and at concentration as low as 0.006 mg/ml, which is not convenient for the deposition because a more CNT-loaded solution is desired. However, with NMP, a stable suspension has been achieved for concentration below 0.05 mg/ml without the need of dispersion aids. For these reasons, this dispersion solution has been considered for the following CNTs deposition by spray coating because it avoids the need of rinsing off the surfactant and further cleaning process after coating.

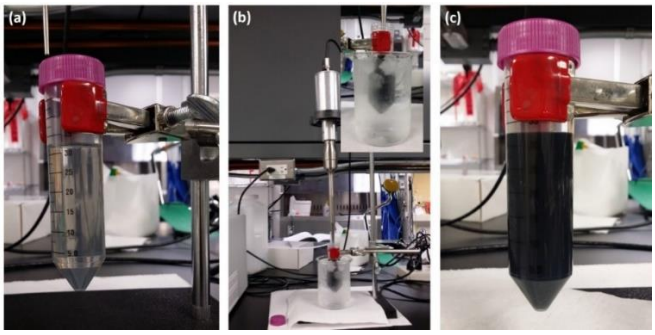

Figure 4.7 CNT dispersion process. a) CNT powder is added to the solvent in a falcon tube. b) The dispersion is sonicated using a sonicator probe. Inset: a close up of the sonicator probe into the CNT solution c) A homogenous suspension is obtained after sonicating.

4.3.3 MW-CNT Spray coating process

The MW-CNT suspension (described above) has been sprayed over the samples using a spray coating system (Prism BT from Ultrasonic Systems, Inc), shown in Fig. 4.8.a. The spray coating systems uses an ultrasonic spray head, show in Fig. 4.8.b, composed of an ultrasonic generator, a spray-forming tip, a liquid delivery system and air directors. The solution is applied directly to the spray forming tip which atomizes the liquid by ultrasonic energy. The Formed spray is shaped and directed down to the substrate with low pressure air directors. The ultrasonically–produced spray can be expanded to a wide rectangular pattern by the air directors system. The spray head has an X-Y-Z motion and positioning system that allows to create dots, single lines, lines or serpentine lines coating patterns. The liquid delivery flow rate is controlled by a pump. The substrate can be heated to a set-point temperature during coating. A visualization of the coating process is illustrated in Fig. 4.8.c. Coating “recipes” can be fully programmed via a graphic interface. Main spray coating process parameters are listed in table 4.2.

Table 4.2 Main spray coating process parameters.

Parameter	Description
Coating type	Type of the coating pattern: dot; lines; area to fill with lines distanced by a specified pitch; area to fill with serpentine lines distanced by a specified pitch
Substrate temperature	Hotplate temperature on top of which the substrate is placed.
Flow rate (ml/s)	Flow rate of liquid coating material delivery to the spray head
Speed (mm/s)	The running speed of the spray head while coating
Height (mm)	The height in millimetres of the spray head above the substrate while coating
Pressure (psi)	Pressure of the N_2 steam used to direct down the spray against the substrate
Number of iterations	Number of times the coating pattern is subsequently repeated

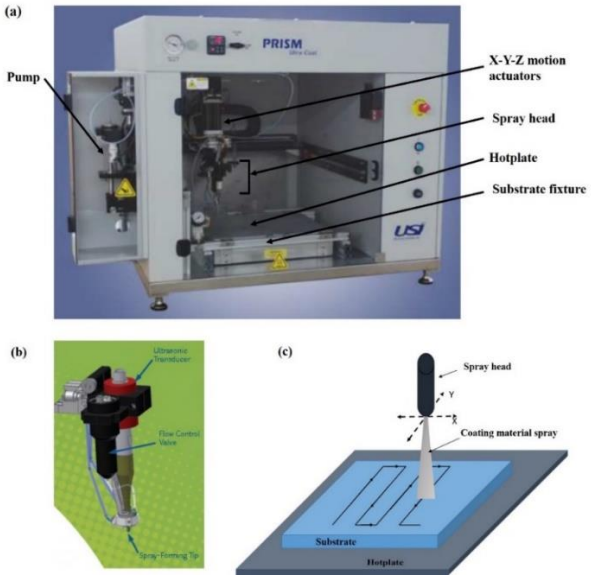

Figure 4.8 Spray coating system. a) A photograph of the model Prism BT spray coating system from Ultrasonic Systems, Inc [27]. b) 3D schematic of the ultrasonic spray head [27]. c) 3D schematic of the spray coating process.

In the following, substrates are 1x1 cm^2 sized Si/SiO_2 with a top 5 nm/50 nm-thick bi-layer of Cr/Au deposited by e-beam evaporation. For spray coating process development, CNT suspensions prepared with pristine MW-CNTs (with properties listed in table 4.1) and NMP (without use of any surfactant) have been used.

Spray coating is carried out while the substrate is heated to allow evaporation of the solvent. The wettability of the substrate by the solvent, thermal flow current in the liquid droplets deposited on the substrate have been one of the main hindrances to coating process development. Both cause what it is known as the "coffee-ring effect" [90, 93]. It has been observed that, for low temperature deposition, the sprayed CNT-loaded liquid forms droplets on the substrate surface. The CNTs initially dispersed over the entire drop, after evaporation become concentrated into a tiny circumference liner, as can be seen in Fig. 4.9.a and 4.9.b. In consequence coating uniformity over the whole surface is hard to achieve. This effect is shown, in Fig. 4.9, for spraying a 0.07 mg/ml-concentrated MW-CNT dispersion in NMP at 40 mm/s speed, 0.2 ml/min flow rate and alternated perpendicular lines coating pattern repeated subsequently 16 times. If the liquid deposition rate is relatively high as a result of high flow rate (≥0.5 ml/min) and/or low speed (≤ 40 mm/s), combined with low temperature, deposited droplets merge together and form larger droplets. Evaporation of these droplets leads to the same non-homogenous CNT mats due to the "coffee-ring effect", as can be seen in Fig. 4.10. In consequence higher temperature and lower flow rate and higher speed are preferable to overcome this issue.

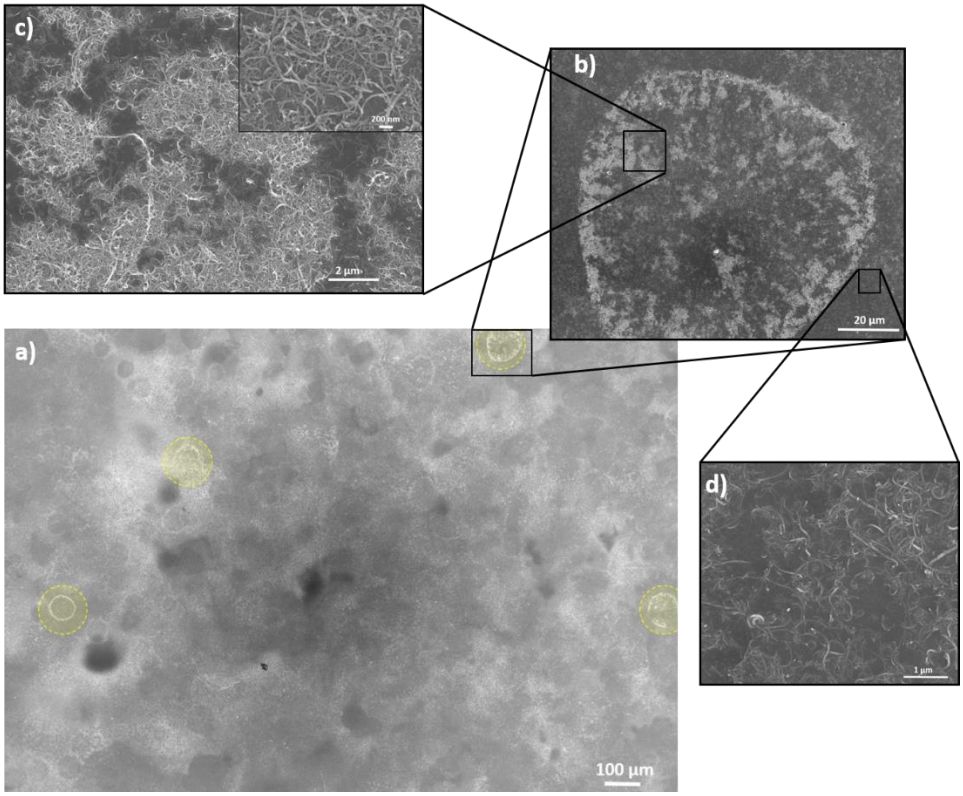

Figure 4.9 The "coffee-ring effect". a) SEM image of MW-CNTs coating on a 5 nm/50 nm-thick Cr/Au bilayer showing the concentrated CNTs in ring-shaped regions highlighted in yellow. b) A close-up of the "coffee-ring effect". c) A close-up of the region inside the "ring". Inset: a close-up of the deposited MW-CNT networks. d) A close-up of the region outside the "ring" showing the lack of CNT-network deposition (see text for coating details).

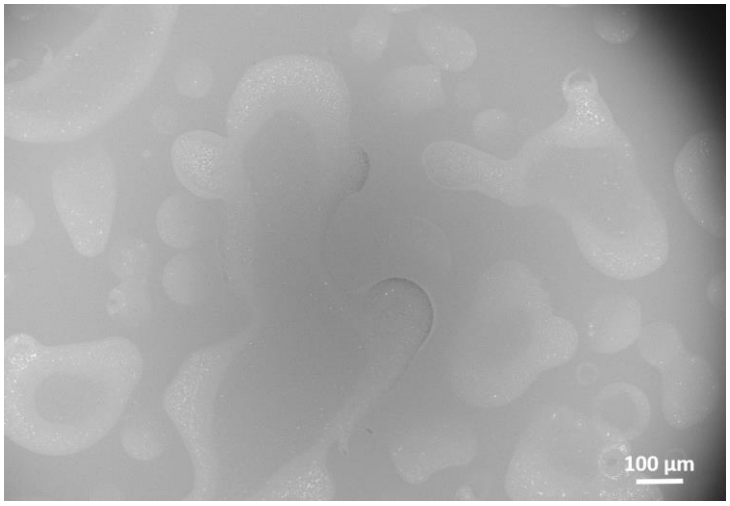

Figure 4.10 SEM image of CNT deposition by a single line pattern spray coating of a 0.1 mg/ml-concentrated MW-CNT dispersion in NMP at 40 mm/s of speed, 0.5 ml/min of flow rate and temperature of 70 °C.

The “coffee-ring effect” can be suppressed by increasing the coating temperature over the boiling point of the NMP (202 °C). The solvent is instantly evaporated at the contact with the substrate surface without forming large droplets. A uniform CNT deposition over the whole substrate surface can then be achieved. Fig. 4.11 shows a comparison between two CNT coatings at 150 and 230 °C. At a coating temperature of 230 °C the “coffee-ring effect” is strongly reduced yielding a uniform distribution of deposited CNTs over the sample surface, as can be seen in Fig. 4.11.b.

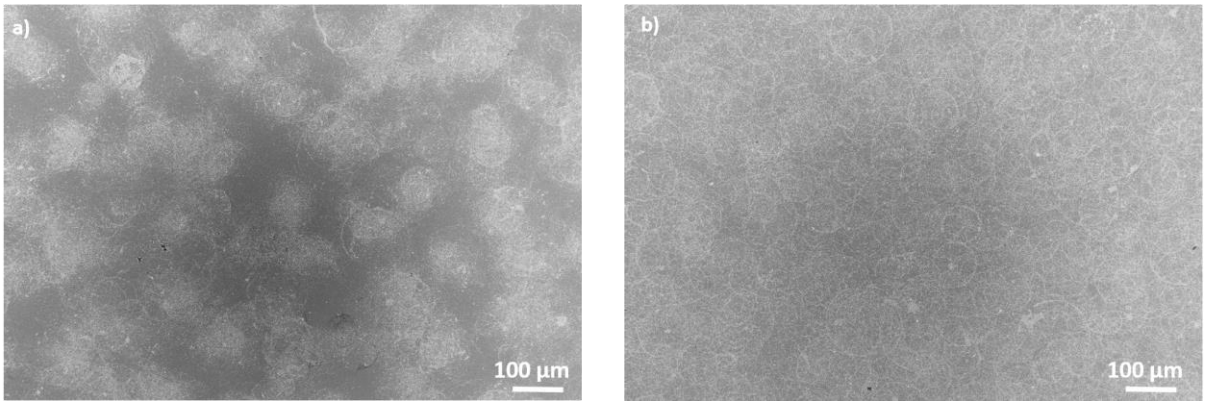

Figure 4.11 SEM images of CNT deposition by alternated perpendicular lines coating pattern repeated subsequently 20 times using a 0.05 mg/ml-concentrated MW-CNT dispersion in NMP at 40 mm/s of speed, 0.25 ml/min of flow rate and temperature of (a) 150 °C and (b) 230 °C.

It is desirable to obtain a homogenous CNT networks layer over large surface with full-surface coverage and controlled thickness. To address the global uniformity of CNT deposition, coating parameters have been optimized and set at the listed values in table 4.3. Coating type and temperature have been found as main parameters impacting the coating uniformity over the entire substrate surface.

Table 4.3 Optimized CNT spray coating process parameters.

Parameter	**Optimized value**
Coating type	Area filled with serpentine lines distanced by a 1 mm pitch
Substrate temperature (°C)	220
Flow rate (ml/s)	0.25
Speed (mm/s)	80
Height (mm)	65
Pressure (psi)	25
CNT suspension concentration (mg/ml)	0.05

Spraying of a CNT dispersion allows randomly deposition of CNT. For a full-surface coverage, multiple coating patterns have to be carried out subsequently. The CNT mats thickness can be tuned by varying the number of subsequently repeated coating pattern (number of iteration).

Five different coatings have been carried out at the optimized parameters (listed in table 4.3) for different iteration number 10, 20, 50, 150 and 300 times. Obtained CNT layers morphology was studied using SEM and AFM observations.

A globally uniform distribution of deposited CNT over the entire substrate surface has been achieved at the optimized coating parameters over the five different number of iterations, as can be seen in Fig. 4.12. However, SEM and AFM observations have shown that a fully covered substrate surface is achieved only for coatings at 50 iterations or above, as can be seen in Fig. 4.13. Spray coatings at 50, 150 and 300 iterations yielded globally uniform and homogenous porous MW-CNTs layers (see Fig. 4.13.c, 4.13.d and 4.13.e). Obtained layer porosity is very relevant to gas sensing (see Fig. 4.14 and 4.15).

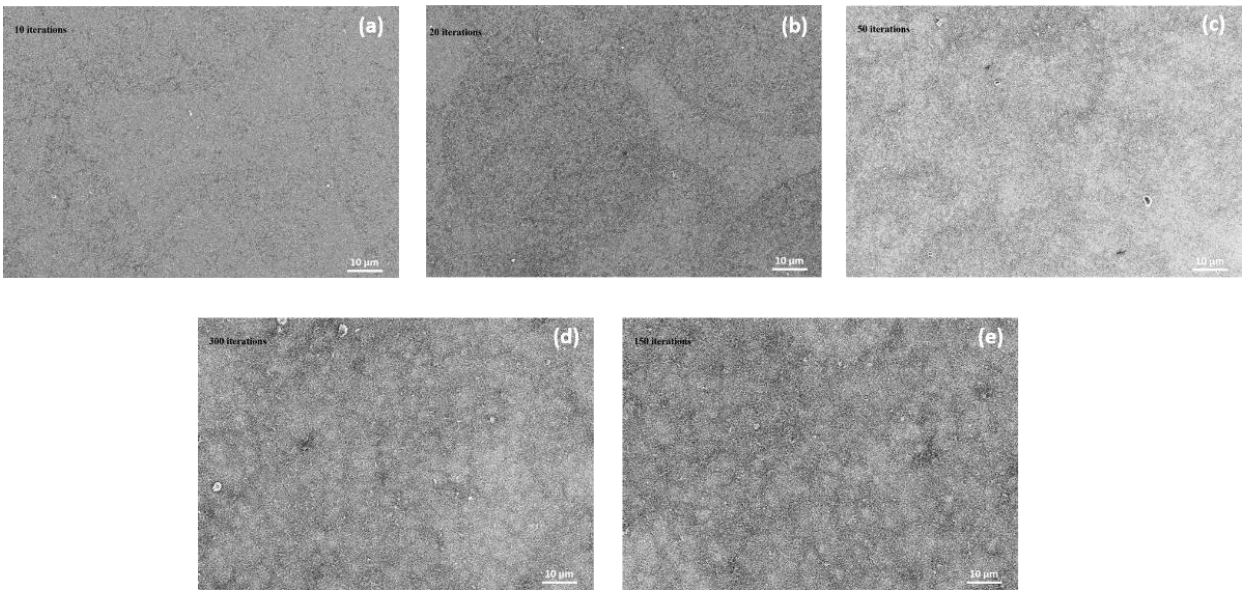

Figure 4.12 SEM images of MW-CNT networks layers obtained by spray coating at the optimized parameters for a) 10, b) 20, c) 50, d) 150 and 300 iterations, showing uniform distribution of CNT deposition.

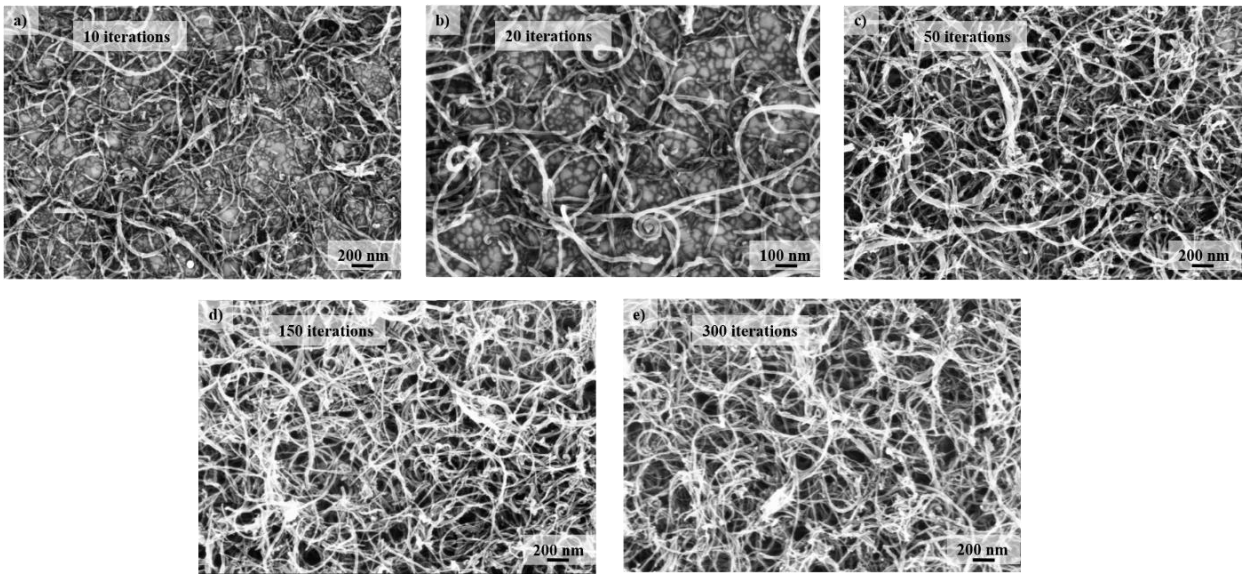

Figure 4.13 SEM images of MW-CNT networks layers obtained by spray coating at the optimized parameters for a) 10, b) 20, c) 50, d) 150 and 300 iterations, showing surface coverage.

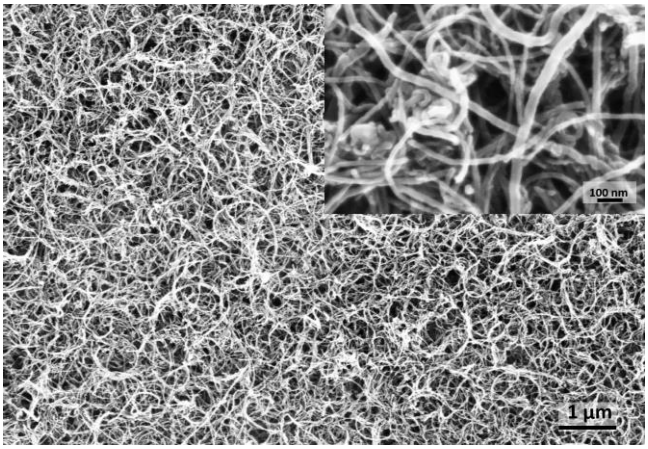

Figure 4.14 SEM image of porous CNT networks layer obtained by spray coating at the optimized parameters for 150 iterations. Inset: a close up of the CNT mat showing CNTs overlapped yielding a porous layer.

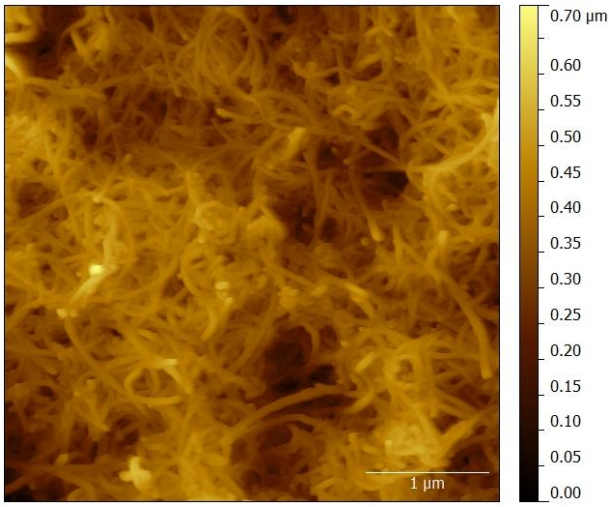

Figure 4.15 Topography scan of a porous CNT layer obtained by spray coating for 300 iterations.

CNT layer thicknesses have been determined from profilometer traces over samples coated with masked substrate regions, as illustrated in Fig. 4.16. The thickness mean value over 5 samples of each coating batch is given in table. 4.4. CNT networks layer thickness can be increased with increasing the number of iterations. The thickness dependence on the number of iterations is not linear. For the first iterations, the material is deposited on a bare surface or a thin porous CNT layer, thus the deposited layer grows faster as a function of the number of iterations. Further than 150 iterations, the CNT layer seems to grow slowly, because the material is deposited on top of the already grown porous layer, and the CNTs are more likely to be incorporated in the

layer porosity. The thickness standard deviations estimated over the 5 samples of each sample batch is within 10%. This means that the coating process is reproducible.

We have been able to achieve globally uniform and porous CNT networks layers on large surfaces, making the CNT spray coating process suitable for large area applications and mass production. CNT deposition with a substrate temperature above the boiling point of the solvent allowed circumvent of all the issues related to substrate wettability by the dispersing media as well as the "coffee-ring effect". Moreover, the low process temperature below CMOS technology thermal budget makes it of great interest for integration with CMOS in term of compatibility.

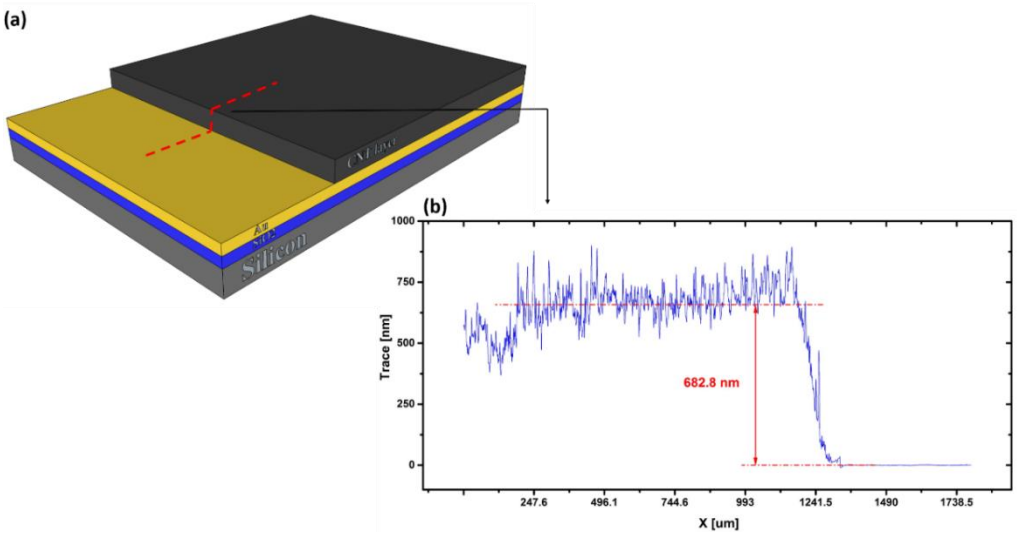

Figure 4.16 a) Schematic illustration of profilometer line trace of the step obtained by spray coating a sample with a masked region, offering a reliable estimation of the CNT layer thickness. b) Profilometer trace of the step of a sample from batch E (coating at 300 iterations). Levelling is done on the Au trace.

Table 4.4 Characteristics of MW-CNT networks layers obtained at the optimized spray coating parameters for different number of iterations.

Coating batch	# of iterations	Surface coverage	CNT layer thickness mean value (nm)
A	10	partial	-
B	20	partial	-
C	50	Full	135 ± 11
D	150	Full	529 ± 50
E	300	Full	664 ± 41

4.3.4 Pt-coated MW-CNT networks

50 nm and 5 nm –thick Pt layers have been evaporated on CNT layers of coating batches A, B, C, D and E. SEM observations have shown that Pt evaporation yielded conformal coatings on the nanotubes, as can be seen in Fig. 4.17. Pt exhibited good wettability over the CNTs which plays in favour of good contact resistance between Pt and the MW-CNTs, thanks to enhanced contact area.

The evaporation of 5 nm-thick Pt layer yielded almost fully Pt-coated CNTs, as can be seen in Fig. 4.18.b. In both evaporated Pt thicknesses, the CNT layers porosity has been preserved (see Fig. 4.18).

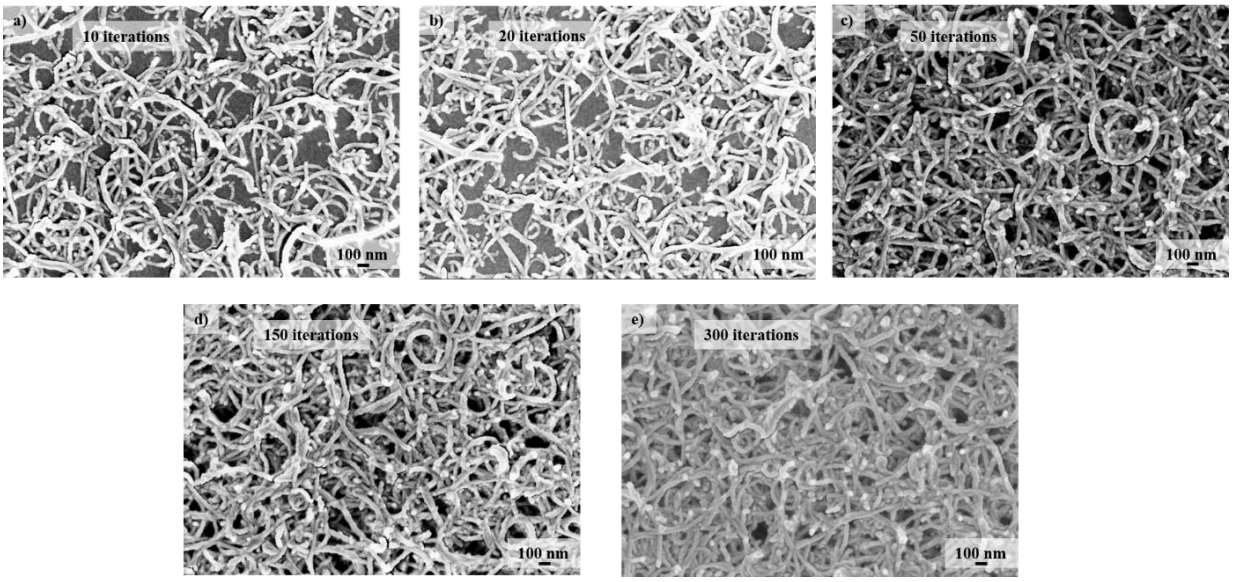

Figure 4.17 SEM images of MW-CNT networks layers obtained by spray coating at the optimized parameters for a) 10, b) 20, c) 50, d) 150 and 300 iterations, after 50 nm-thick Pt layer evaporation, showing conformal coating of the nanotubes.

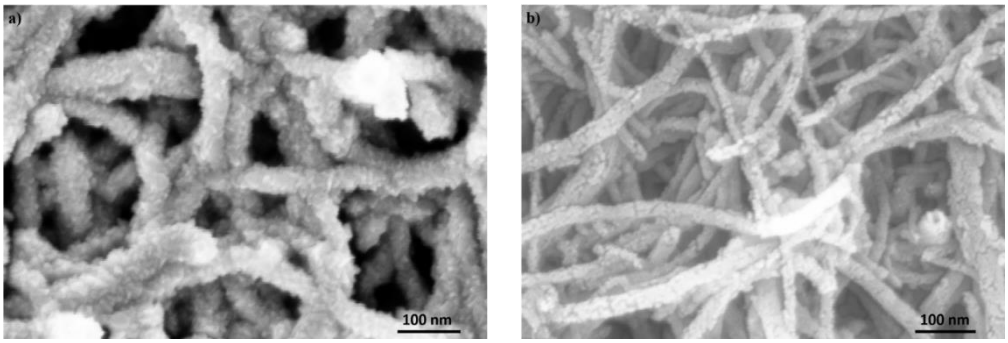

Figure 4.18 SEM images of MW-CNT networks layers obtained by spray coating at the optimized parameters for 150 iterations, after (a) 50 nm and (b) 5 nm -thick Pt layer evaporation showing the good wettability of the MW-CNTs by Pt.

4.4 Material sensitivity characterization

4.4.1 Kelvin probe technique

Kelvin probe (KP) has been the preferred technique for the investigation of sensing material deployed in FET-based gas sensors. Material sensitivity is given in term of work function variation induced by gas species adsorption. The work function is the energy difference between the vacuum level and the Fermi level [94] and can be seen as the least amount of energy needed to withdraw an electron from a material surface atom to the vacuum level. KP belongs to

scanning probe microscopy techniques. It gives the work function difference between the scanning probe tip and the sample. It consists of a non-contact, non-destructive vibrating capacitor used to measure the work function via equilibrium and not via extracting electrons. The Kelvin probe measurement principle is described in Appendix C.

The tip has to be made of a material with very well-known absolute work function value so the work function of the sample can be deduced. Usually the tip is gold made. KP measurements are very reliable under vacuum conditions. In sensing material investigations, the objective is not to obtain the absolute work function value but the variation of this quantity under presence of target gas concentration.

From a technical point of view, KP for sensing material characterization is challenging because the gas chamber has to be large enough to hold not only the sample but also the whole probe. Controlling gas diffusion homogeneity and turbulence is more challenging to control in larger gas chamber. In addition, the work function of the reference material (tip material) may be sensitive to the target gas and contribute to the obtained signal (CPD). This could be a source of error. One needs a reference probe which is not affected by the target. Ostrick *et al*. [31] use a gold grid in KP measurements for work function variations of a sensing layer as response to NH_3. The authors made reference measurements to compensate the gold reaction. Reference measurements were made using Si_3N_4 film as a reference sample.

4.4.2 Surface charge measurement technique

We propose a new technique to investigate material sensitivity, based on measurement of material surface charge variation (surface potential variation) induced by adsorption of gas molecules. The charge measurement is carried out with an electrometer with feedback amplifier configuration, in Coulombs mode (see Appendix B).

4.4.2.a Surface charge measurement principle

Charge measurement is carried out with an electrometer with feedback amplifier configuration, in Coulombs mode. The sensitive layer (metallic or semiconducting) is deposited on top of a metal electrode that is connected to the electrometer high input. The low input is connected to the substrate backside. An electrometer in Coulombs mode is equivalent to two capacitors in parallel: (i) an input capacitance C_{IN} of 10 pF, and (ii) an amplifier input capacitance of $A \times C_F$,

where C_F is the electrometer reference feedback capacitance (capacitor which provides the feedback path around the operational amplifier) of 1000 pF and A is the open loop gain of the operation amplifier. The surface charge measurement configuration and equivalent circuit diagram of the electrometer in Coulombs mode is depicted in Fig. 4.20. Since A is large enough ($A = 55 \times 10^6$), $A \times C_F$ dominates all other capacitances C_S and C_{IN}, and the charge to be measured is completely transferred the coulombmeter input capacitor $A \times C_F$. The electrometer with feedback amplifier configuration allows charge measurements independent of the source capacitance C_S.

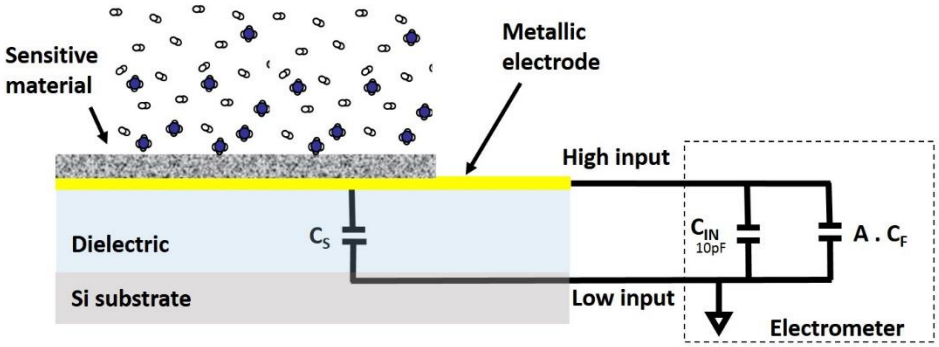

Figure 4.20 Schematic representation of surface charge measurement configuration and equivalent circuit diagram of the electrometer with feedback amplifier in Coulombs mode. C_{IN}, C_S and C_F are respectively the input capacitance, the source capacitance and the electrometer reference feedback capacitance. A is the open loop gain of the electrometer operation amplifier.

The method can be applied to conducting materials. Neglecting the source and electrometer input capacitance, the equivalent system is depicted in Fig. 4.21 for hydrogen and oxygen detection with Pt as well as for CO detection with SnO_2. Charges at the both sides of the electrometer capacitance, are illustrated in green or red when they appear or disappear respectively, as a result of a single adsorption event. In both cases of hydrogen sensing with Pt and CO sensing with SnO_2, a detection event yields a negative charge transfer to the material, which translates into a negative variation in the electrometer charge reading, as illustrated in Fig. 4.21.e, which is equal but opposite in the sign to the surface charge variation. In contrast, the detection of oxygen by Pt yields a negative charge transfer from the material, which induces a positive change in the electrometer charge reading, as illustrated in Fig. 4.21.d.

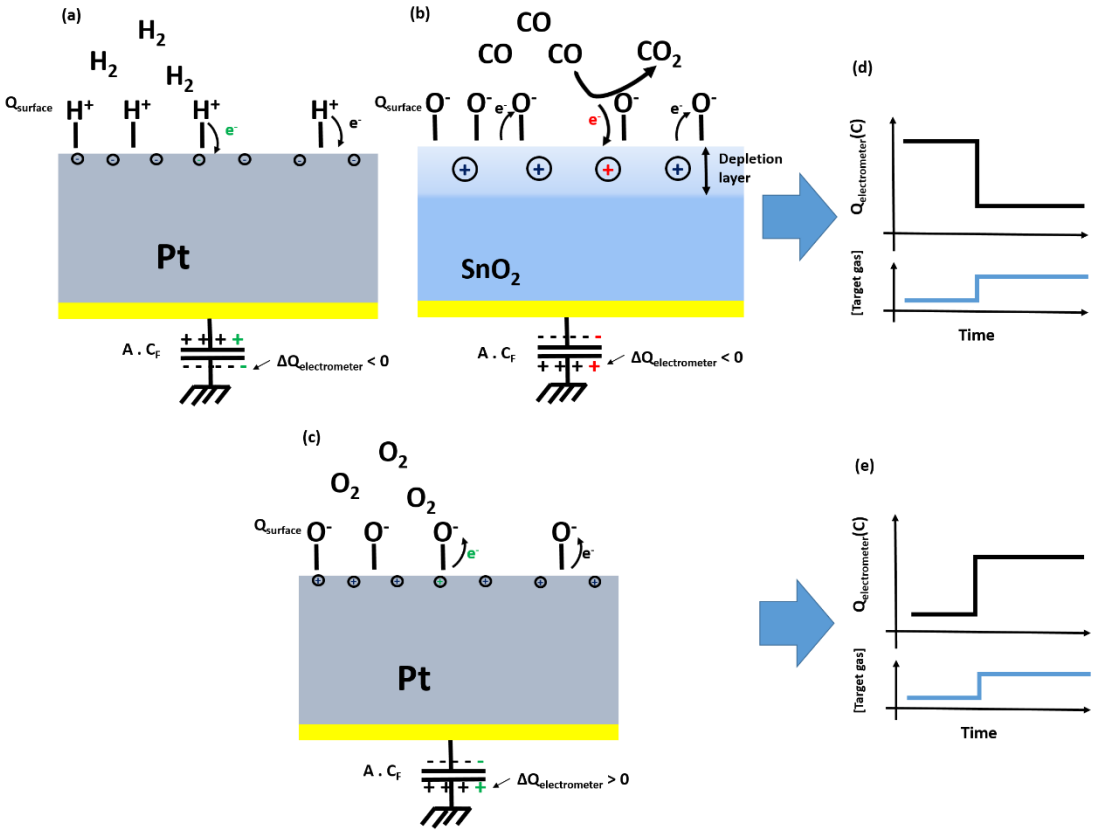

Figure 4.21 Schematic of equivalent system of a sensing layer connected to an electrometer (with feedback amplifier) in Coulombs mode in surface charge measurement configuration illustrated for a) H_2 detection with Pt, b) CO detection with SnO_2, c) and oxygen detection with Pt, and yielded charge reading change shown in d) and e). Charges in green or red are meant to respectively appear or disappear as a result of the detection event.

4.4.2.b Experimental set-up and measurement conditions

An experimental set-up, show in Fig. 4.22, has been built to carry out surface charge measurement. Gas sensing characterizations were carried out inside a metallic gas chamber with controlled atmosphere. The gas chamber, shown in Fig. 4.23, is made of aluminium and has a volume of about 160 ml. It has 4 electrical feedthroughs and gas inlet and outlet placed respectively at the bottom and top of the chamber. Three of the electrical feedthroughs are equipped with a 3-lug female triax bulkhead connectors (Keithley model CS-630 connector) for connection with measurement instruments. The other electrical feedthrough allows the heater DC voltage supply. The chamber has been designed that no turbulence is generated at a flow rate up to 1 L/min. The experimental set-up is described in Appendix B.

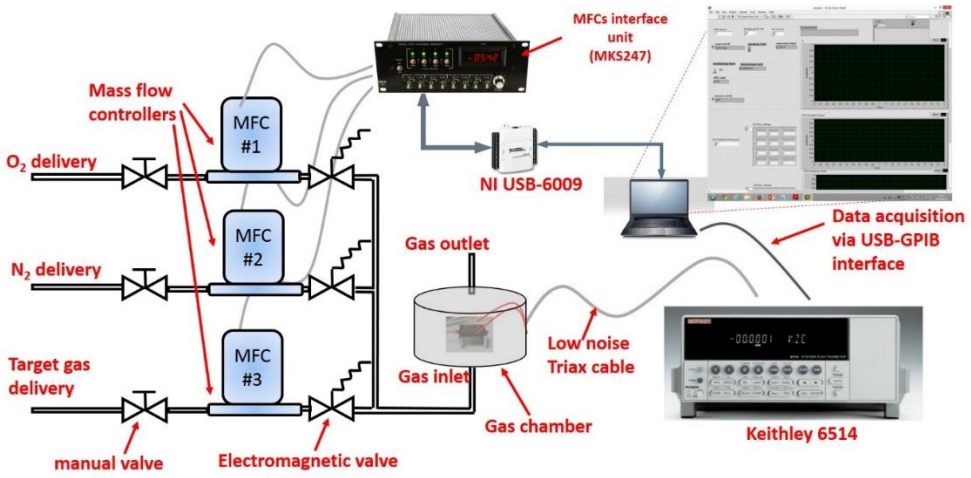

Figure 4.22 Schematic representation of the experimental set-up used in surface charge measurements.

The samples were wirebonded to a chip carrier with a flexible heater underneath of it (see Fig. 4.23.b and 4.23.c). The ensemble of sample, heater, chip carrier and socket is mounted on a "homemade" metallic holder and placed inside the metallic gas chamber with the sample facing the gas inlet, as shown in Fig. 4.23.a. Measurements were carried out at a total flow rate of 1 L/min. An Omega model KHLV-0502/10 heater has been used to heat the sample. The Polyimide film insulated heater is rated up to 200 °C with excellent out-gazing properties and has a thickness of 2.54 mm. The flexible heater was wrapped in an aluminium foil.

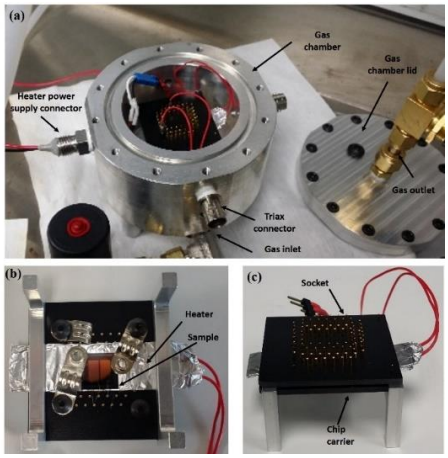

Figure 4.23 A view of the gas chamber and the sample holder. a) Photograph of the metallic chamber with the sample placed inside. b) Bottom view photograph of a sample wirebonded to a chip carrier and mounted on the sample holder with the flexible heater. c) Top view photograph of a sample mounted on a chip holder with the flexible heater.

Measurements were carried out with common and the chassis-ground of the electrometer connected (brought to the same potential by installing the ground link between the common and Chassis-ground binding posts). The metallic chamber was connected to electrometer chassis-ground to act as a metal noise shield. The Keithley model 6514 was operated at an integration time of 16.64 ms. At this reading rate the noise reading is at its minimum level, as suggested by the instrument manufacturer. Charge measurement was sampled at sampling period of 1s, which is enough low compared to time constant of response signals.

4.4.2.c Sample design and fabrication process

Fig. 4.24.a and 4.24.b illustrate respectively a top-view and a cross-section structure of a typical sample used in gas-sensitive material characterization using surface charge measurement technique. The fabrication process is based on two UV lithography steps (UV#1 and UV#2) followed by material deposition and a lift-off process. The second lithography is aligned on marks patterned by the first one. Two photomasks (mask UV#1 and mask UV#2) have been designed so that processing of a 4 inch wafer yields 4 samples. The UV lithography layout (UV#1 and UV#2) is shown in Fig. 4.25.

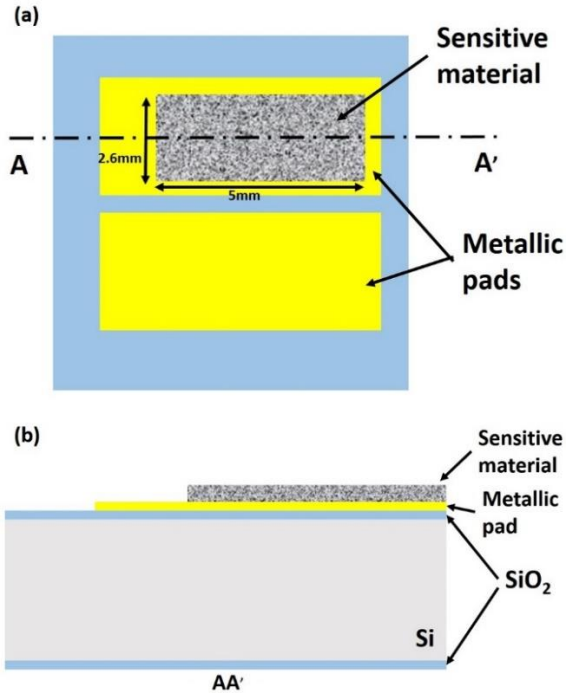

Figure 4.24 Sample design used in gas-sensitive material characterization using surface charge measurement technique. a) Top view and b) cross-section schematic representation of sample structure.

Starting substrates are boron doped Si wafer (6 Ω.cm) with 150 nm-thick layer of thermally grown SiO_2. Prior to processing, substrates are ultrasonicated in acetone for 5 min, then dipped in isopropanol for 5 min, and rinsed with deionized water, to remove organic and inorganic contaminants. The wet cleaning step is followed by exposure to a capacitively coupled O_2 plasma produced by 150 W radio frequency (RF) power at 300 mTorr for 5 min in a barrel etcher.

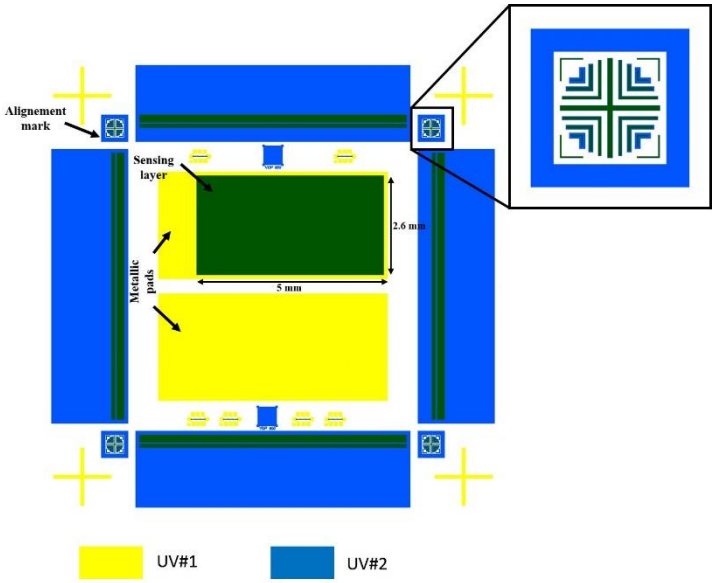

Figure 4.25 UV lithography layout of a cell. Right: a close-up of an alignment mark.

Fig. 4.26 shows an overview of the fabrication process flow of samples without CNT surface texturing. In a first step, a bilayer resist of LOR3A/S1805 was spun onto the sample. Both resists were spun at 5000 rpm for 5 min. S1805, a positive UV resist, is baked at 115 °C for 60 s. LOR3A, a lift-off resist, is baked at 150 °C for 5 min. The S1805 resist is exposed using the mask UV#1 to pattern the two metallic pads. After puddle resist development in AZ MIF319 (2 x 30 s), samples are exposed to capacitively coupled O_2 plasma at 100W and 300mTorr for 60 s in a barrel etcher, to remove residual resist waste.

Then, the two metallic electrodes are formed by e-beam evaporation of a 5 nm-thick Ti layer followed by a lift-off process. At this step the wafer could be diced into 4 different 1x1 cm^2 samples, which could be processed individually.

In a second step, UV lithography aligned on marks (see Fig. 4.26) patterned during first UV lithography is carried out to define the area of sensitive material. The sensing layer is deposited by either e-beam evaporation or sputtering, followed by a lift-off process. A bilayer resist LOR/S1805 is used for sensitive material patterning. Resist spinning, baking and development are the same as in the first step. A post-development O_2 plasma process was carried out as described above. Only the lift-off resist layer thickness has to be tuned with respect to desired material layer thickness. It should exceed 3 times the thickness of the material to be deposited for reliable lift-off. Table 4.5, gives an overview of the lift-off resist deposition process and yielded thickness (data given by the resist supplier). The sensitive material is deposited only on top of only one over the two patterned Ti electrodes. The second bare Au electrode serves as a reference to check the Au electrode to the target gas. The formed sensitive material layer has a surface area about 13 mm^2 (see Fig. 4.25). Ti electrodes are wire-bonded to a chip carrier. Samples with 50 nm-thick Pt layer as a sensing layer, deposited by e-beam evaporation at a rate of 0.5nm/s, have been fabricated for H_2 sensing.

Table 4.5 Lift-off resist spin coating process and yielded layer thickness.

Lift-off resist	Spin coating speed (rpm)	Duration of spinning (s)	Baking temperature (°C)	Duration of baking (min)	Yielded thickness (nm)
LOR3A	5000	30	150	5	250
LOR5A	5000	30	150	5	400
LOR5A	3000	30	150	5	550

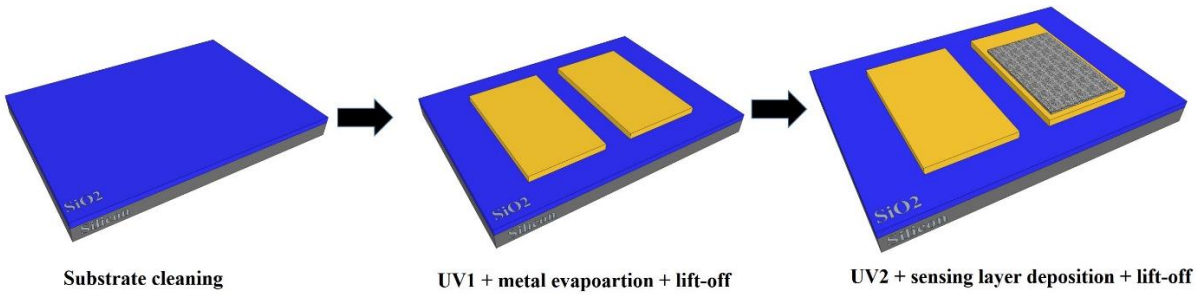

Figure 4.26 Schematic of sample fabrication process flow.

Fabrication process flow of samples with CNT surface texturing, similar to the process described above, is shown in Fig. 4.27. Just after forming the two metallic electrodes, a blanket MW-CNT layer is deposited by spray coating over the whole sample surface followed by a wet cleaning process, as detailed in section 4.6.3. A subsequent UV lithography (UV2) is carried out using a negative resist and mask UV#2 to define the CNT mat area. AZ NLOF 2020, a negative resist, is spun onto the sample at 3000 rpm for 5 min, thermally cured on a hotplate at 110 °C for 60 s to yield a 2 µm-thick resist layer. The resist is exposed and a post exposure bake is carried out at the same conditions as the soft bake. Afterwards, the resist is developed by puddling AZ MIF319 developer 3 times for 30s.

In the next step, the exposed CNT networks layer is etched down by reactive ion etching process (RIE) using only oxygen in a RF powered CCP (capacitively coupled plasma) system. A CNT plasma etching process has been developed and optimized. Optimized parameters and obtained etch rate are summarized in table 4.6. The etching duration has to be tuned with respect to the CNT mat layer thickness. Through the resist stripping, exposure to the O_2 plasma is avoided as well as the sonication due to the fragility of the CNT networks.

Table 4.6 Optimized CNT networks layer CCP etching process and corresponding etch rate.

Parameter	**Value**
Gas	O_2
Pressure (mTorr)	300
Power (W)	100
Etch rate (nm/min)	70 ± 7

In the last step, a Pt layer is deposited on top of the already patterned CNT mat by an aligned UV lithography (UV#3) and lift-off process. UV#3 is carried out using mask UV#2 and a bilayer resist LOR5A/S1805. Resist spinning, baking and development are the same as described above.

In contrast, no exposure to O_2 plasma is carried out after resist development. The CNT mat is Pt-coated by evaporation of a 50 nm-thick layer with a deposition rate of 0.5 nm/s.

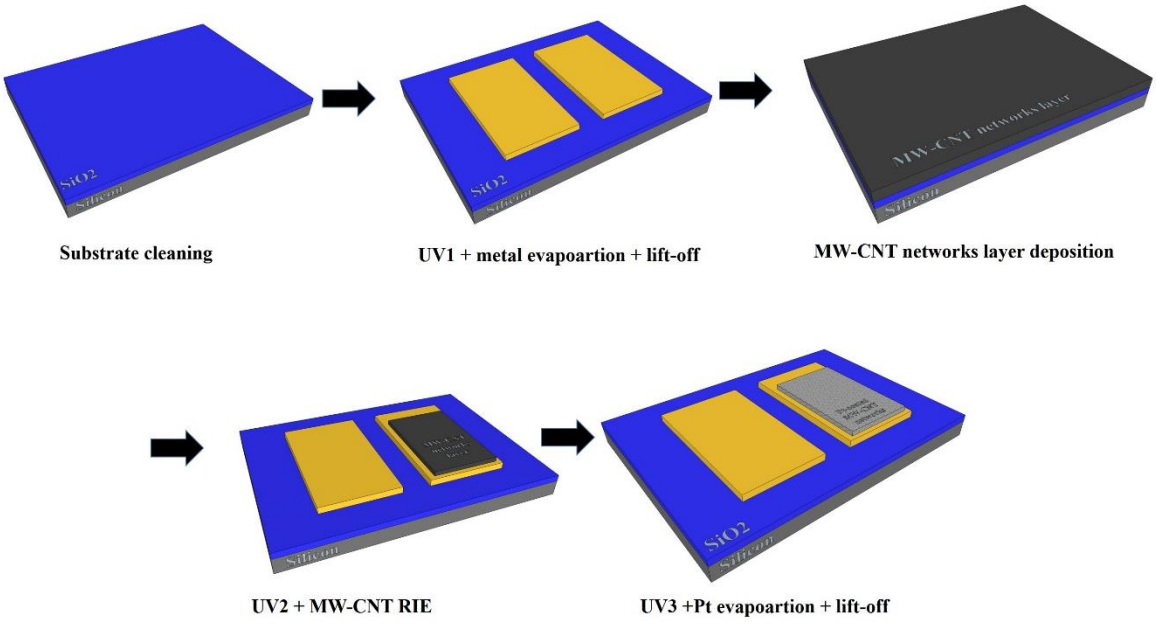

Figure 4.27 Schematic of CNT-textured sample fabrication process flow.

4.5 Platinum sensitivity to H_2

Platinum sensitivity to hydrogen diluted in synthetic air (80% N_2 and 20% O_2) has been investigated by the surface charge measurement technique. For this purpose, samples with 50 nm-thick Pt layer as a sensing layer, deposited by e-beam evaporation at a rate of 0.5 nm/s, on a 5 nm-thick Ti layer have been fabricated and wirebonded to the chip carrier with Al wires.

In the following, experimental data are mean values of Pt response over 5 subsequent repeated measurements. Mean values and standard deviations, represented by bar errors, have been estimated by statistical analysis over the 5 repeated measurements.

During each recording measurement, the sample is first soaked in background gas flow for 1000 s, to acquire the baseline signal $Q_{baseline}$, before injecting H_2 at the desired concentration during 1000 s to acquire the response signal after reaching the steady state $Q_{response}$. Then, H_2 feeding is switched off and the sample is again under background gas flow for 1000 s. The charge reading variation $\Delta Q_{electrometer}$ is the difference between the two acquired values:

$$\Delta Q_{electrometer} = Q_{response} - Q_{baseline} \quad (4.1)$$

First, the sensitivity of bare Ti pad to H_2 has been checked. The Ti pad exhibited no response to the hydrogen injection over the temperature range RT-190 °C. This means that neither the Ti layer nor the wiring system inside the gas chamber is responding to hydrogen and thus not contributing to the measured signals.

The Pt response to the oxygen injection in pure N_2 has been investigated over the temperature range RT-190 °C and is shown in Fig 4.28. A typical response of Pt to the injection of 20% oxygen in pure N_2 at 130 °C is shown in Fig. 4.29. In the presence of O_2 the electrometer charge reading exhibited a positive variation as a response to the O_2 injection over the whole investigated temperature range, which in agreement with the theory (as described in section 4.2.1).

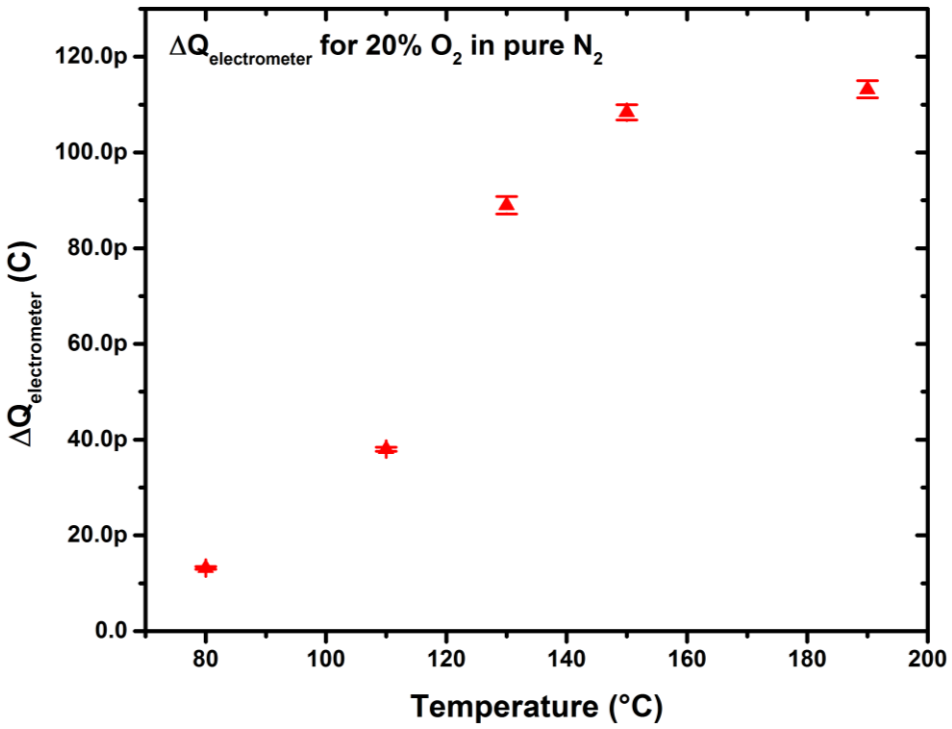

Figure 4.28 Pt layer charge variation response at varying temperature from 80 to 190 °C to oxygen concentration of 20% in pure nitrogen.

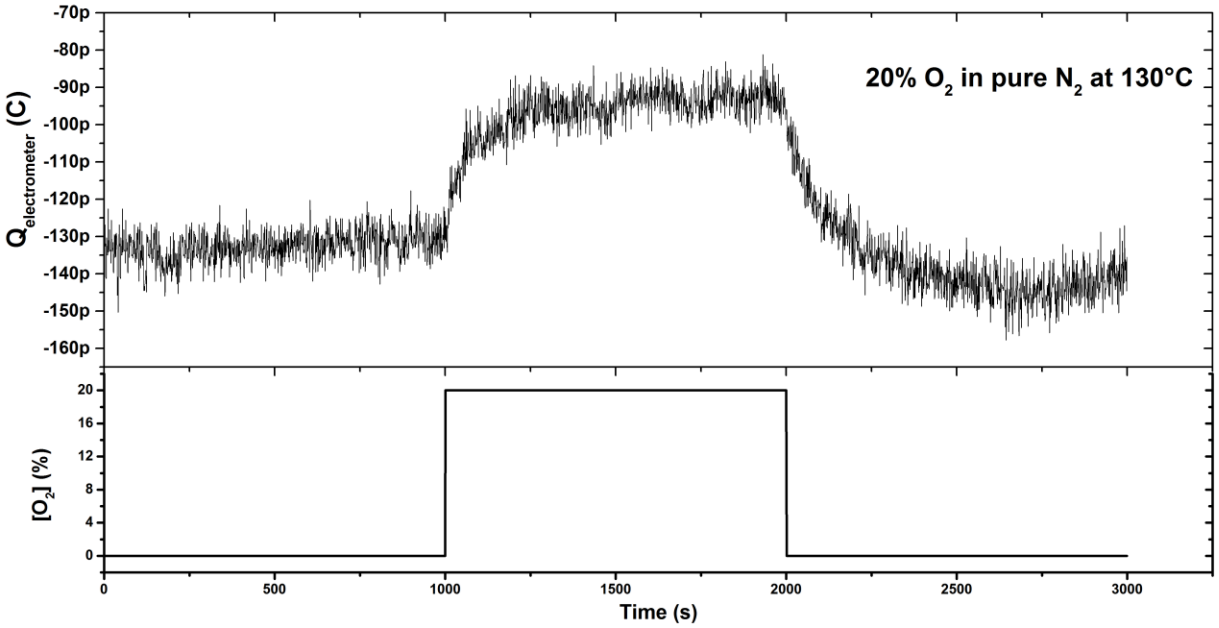

Figure 4.29 Time response of platinum layer to the injection of 20% O_2 in pure N_2 at 130 °C.

The Pt response to 4% H_2 in synthetic air (80% N_2 and 20% O_2) has been investigated over the temperature range of RT to 190 °C. Experimental data are given in table 4.7. Two different types of Pt response (in term of the electrometer charge reading) have been observed: a positive variation for operating temperature above 80 °C (see Fig. 4.30) and a negative variation below this temperature (see Fig. 4.31) have been observed. Pt charge variation dependence on H_2 concentration has been studied for both regimes. Charge measurements were carried out for different concentrations ranging from 0.5 to 5% and from 0.5 to 4% at temperatures of 60 and 130 °C respectively.

Table 4.7 Pt response to the 4% H_2 injection in synthetic air for various operating temperatures in term of the electrometer charge reading.

Temperature (°C)	**ΔQ (C)**	**Standard deviation (C)**
50	-11.84 10^{-12}	0.2 10^{-12}
60	-14.5 10^{-12}	1.8 10^{-12}
80	+31.7 10^{-12}	1.4 10^{-12}
110	+2.25 10^{-9}	0.122 10^{-9}
130	+4.916 10^{-9}	0.183 10^{-9}
150	+8.84 10^{-9}	0.176 10^{-9}
190	+23.363 10^{-9}	0.880 10^{-9}

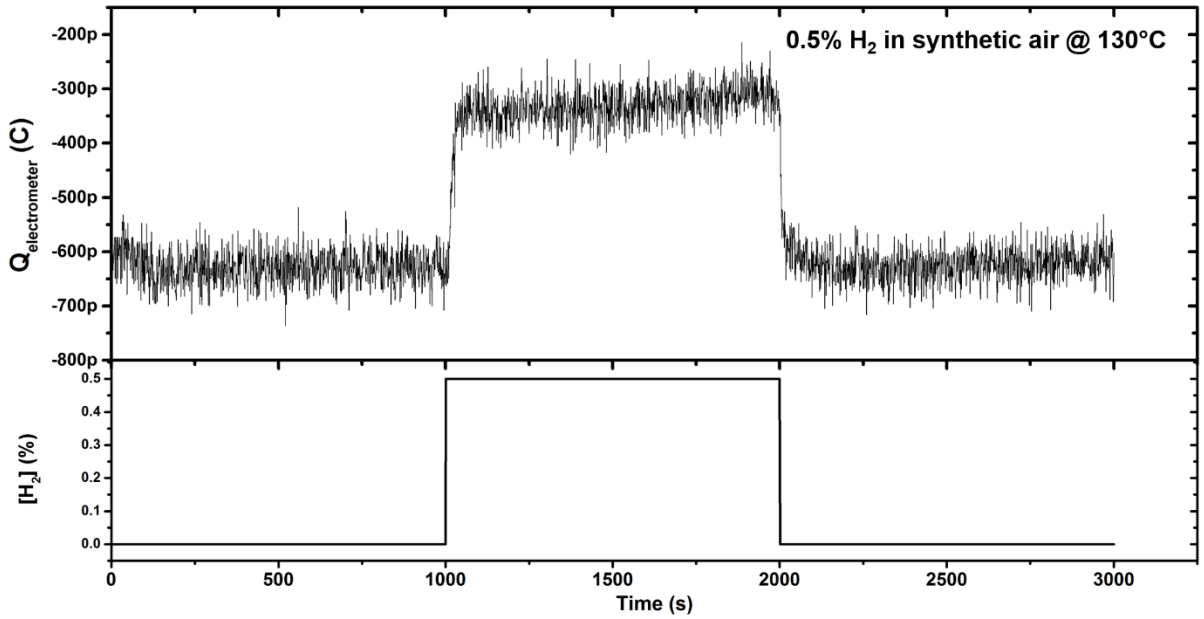

Figure 4.30 Time response of a platinum layer to the injection of 0.5% H_2 in synthetic air at 130 °C.

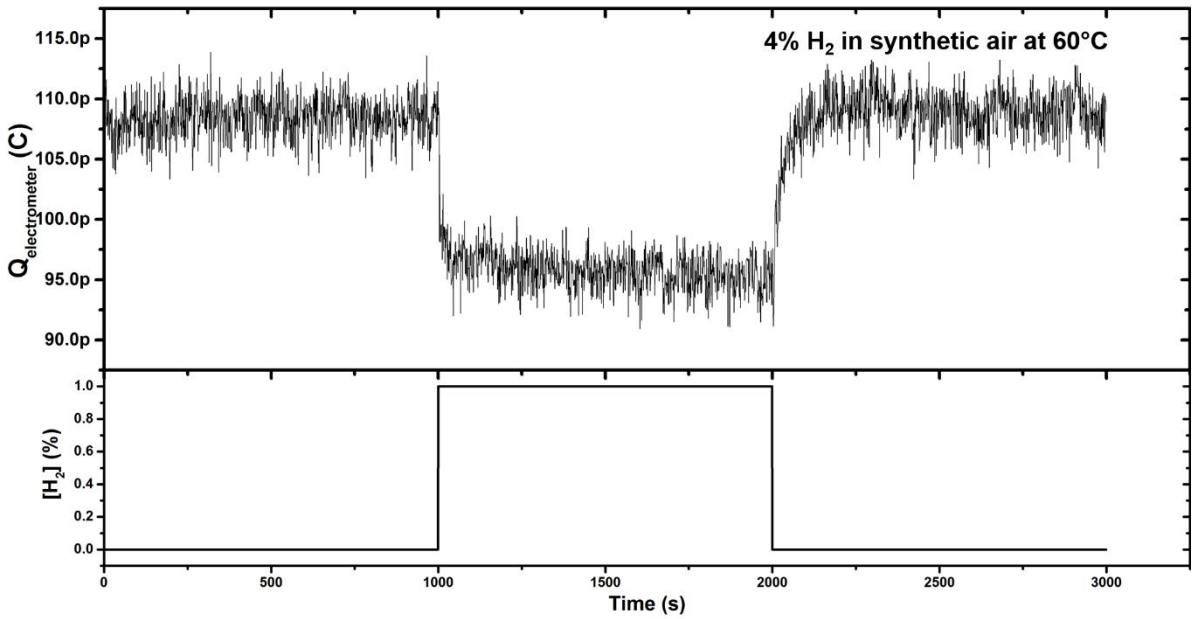

Figure 4.31 Time response of platinum layer to the injection of 4% H_2 in synthetic air at 60 °C.

Data for temperature below 80 °C is in agreement with the theory: the hydrogen atoms adsorption gives rise to a positive variation in surface charge and hence a decrease in Pt work function (a decrease in the Pt potential) [12, 24, 87], which translates into a negative variation in the electrometer charge reading, as explained in section 4.2.2.b. Induced charge reading variations ΔQ at varying hydrogen concentration at 60 °C are presented in Fig. 4.32.

A good linear material response to the logarithm of H_2 concentration from 0.5 to 3% has been obtained with a sensitivity of -13.4 pC/decade. The same observation has been reported in literature [12, 24, 84, 88]. As can be seen in Fig. 4.32.a with increasing H_2 concentration above 3% $|\Delta Q|$ decreases exhibiting a tendency toward saturation. The sensitivity of the sensing layer per surface area is estimated to be equal to -0.8 pC/decade per mm^2. The time response at this temperature is within 5s.

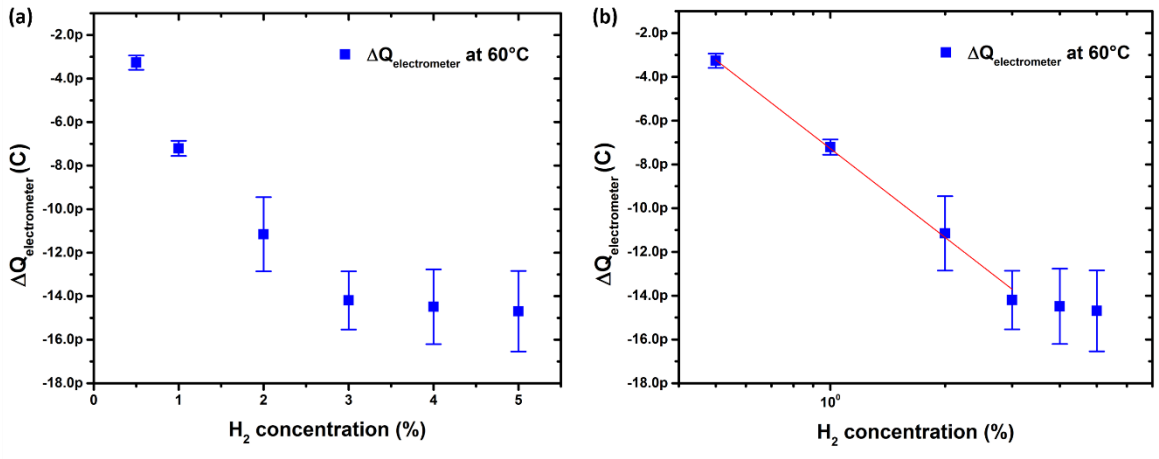

Figure 4.32 Hydrogen concentration dependence of platinum layer response in term of charge reading variation at 60 °C in the linear (a) and semi-logarithmic scale (b).

The induced charge reading variation - and thus surface charge variation- can be described by the following model.

It is assumed that the density of adsorbed hydrogen is proportional to the hydrogen partial pressure (It means that the heat of adsorption is considered constant and independent of the surface coverage rate). The equation describing the hydrogen chemisorption at the surface of Pt can be written as:

$$H_{2gas} \rightleftharpoons 2\,H_a \tag{4.2}$$

In presence of oxygen, we assume that adsorbed hydrogen and oxygen atoms may react and form H_2O. This interaction is given by the following equations:

$$O_{2gas} + 2\,H_a \overset{C_1}{\rightarrow} 2\,OH_a \tag{4.3}$$

$$OH_a + H_a \overset{C_2}{\rightarrow} H_2O_{gas} \tag{4.4}$$

where index *gas* refers to gas phase species and *a* to atomic adsorbed species; K_{ads} and K_{des} stand for respectively adsorption reaction and desorption reaction constants of hydrogen chemisorption on platinum (Eq. 4.2). C_1 and C_2 denote reaction constants of Eq. 4.3 and 4.4

respectively. Back reactions of Eq. 4.3 and 4.4 are neglected owing to the large enthalpy of forward reactions.

Possible other reactions that can take place at the Pt surface between nitrogen and adsorbed hydrogen adatom can be described by the following equations:

$$N_{2gas} + 2\,H_a \overset{K_1}{\rightarrow} 2\,NH_a \tag{4.5}$$

$$2NH_a + H_a \overset{K_2}{\rightarrow} NH_{2a} \tag{4.6}$$

$$NH_{2a} + H_a \overset{K_3}{\rightarrow} NH_{3gas} \tag{4.7}$$

where all back reactions of Eq. 4.5, 4.6 and 4.7 have been neglected;. K_1, K_2 and K_3 denote reaction constants of respectively Eq. 4.5, 4.6 and 4.7.

The surface coverage rate Θ is defined as the ratio of adsorbed hydrogen concentration $[H_a]$ by the total density (concentration) of available surface sites for chemisorption, occupied or unoccupied, $[S_t]$:

$$\Theta = \frac{[H_a]}{[S_t]} \tag{4.8}$$

Similarly , φ and ψ denote surface fractional coverage of OH_a, NH_a and NH_{2a} respectively, assuming the number of adsorption sites to be the same. Using equation of H_2 chemisorption and coverage rate definition, the rate equation for H_2 chemisorption will be:

$$\frac{d\Theta}{dt} = K_{ads}\,P_{H_2}\,(1-\Theta)^2 - K_{des}\,\Theta^2 - C_1\,P_{O_2}\,\Theta^2\,(1-\upsilon)^2 - C_2\,\Theta\,\upsilon - K_1\,P_{N_2}\,\Theta^2(1-\varphi)^2 - K_2\,\Theta\,\varphi^2\,(1-\psi) - K_3\,\Theta\,\psi \tag{4.9}$$

$$\frac{d\upsilon}{dt} = C_1\,P_{O_2}\,\Theta^2\,(1-\upsilon)^2 - C_2\,\Theta\,\upsilon \tag{4.10}$$

$$\frac{d\varphi}{dt} = K_1\,P_{N_2}\,\Theta^2\,(1-\varphi)^2 - K_2\,\Theta\,\varphi^2\,(1-\psi) \tag{4.11}$$

$$\frac{d\psi}{dt} = K_2\,\Theta\,\varphi^2\,(1-\psi) - K_3\,\Theta\,\psi \tag{4.12}$$

where P_{H_2}, P_{O_2} and P_{N_2} are partial pressure of hydrogen, oxygen and nitrogen. Factors like $(1-\Theta)^2$ and Θ^2 arise from the fact that two adsorption sites are involved in adsorption-desorption reaction of Eq 4.2. At equilibrium (steady state) $\frac{d\Theta}{dt} = 0$, $\frac{d\upsilon}{dt} = 0$, $\frac{d\varphi}{dt} = 0$ and $\frac{d\psi}{dt} = 0$ and assuming that $\upsilon \ll 1$ and $\varphi \ll 1$, the steady-state coverage rate is given by:

$$\frac{\Theta}{1-\Theta} = \left(\frac{K_{ads}\,P_{H_2}}{2\,C_1\,P_{O_2} + 3\,K_1\,P_{N_2} + K_{des}}\right)^{1/2} \tag{4.13}$$

The charge variation ΔQ is assumed to be proportional to coverage rate Θ. Assuming that $\Theta = 1$, where all adsorption sites are occupied, corresponds to the maximum variation in charge of Pt and using Eq. 4.13 we have:

$$\frac{1}{\Delta Q} = \frac{1}{\Delta Q_{max}}\left(\frac{2\,C_1\,P_{O_2} + 3\,K_1\,P_{N_2} + K_{des}}{K_{ads}\,P_{H_2}}\right)^{1/2} + \frac{1}{\Delta Q_{max}} \tag{4.14}$$

where ΔQ_{max} stands for maximum charge variation due to chemisorption of hydrogen on all adsorption sites. Equation (9) implies that $^1/_{\Delta Q}$ is proportional to $(P_{H_2})^{-1/2}$. A plot of $^1/_{\Delta Q}$ *versus* $(P_{H_2})^{-1/2}$ at 60 °C is presented in Fig. 4.33.

From the intercept of a linear fit of experimental data corresponding to the saturation region (data for H_2 concentration of 3–5%) of $^1/_{\Delta Q}$ *versus* $(P_{H_2})^{-1/2}$ plot ΔQ_{max} could be estimated. We obtained $\Delta Q_{max} = -16.7$ pC.

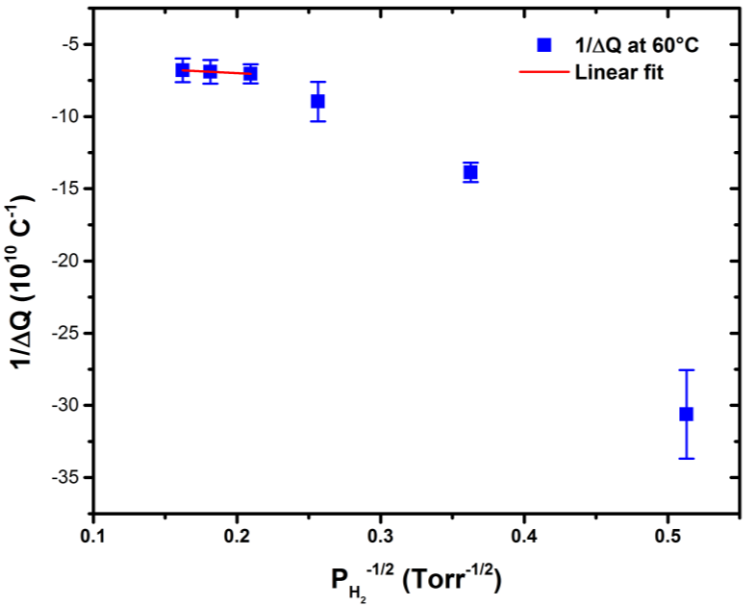

Figure 4.33 Plot of $1/\Delta Q$ *versus* $P_{H_2}{}^{-1/2}$ at 60 °C.

The platinum response to H_2 in synthetic air for temperature above 80 °C surprisingly exhibited a positive variation in charge reading and hence an increase in the work function (increase in the potential). It is known that for temperature above 100 °C, adsorbed hydrogen atoms at the outer surface diffuse rapidly through the Pt film due to the high solubility and diffusivity of hydrogen in catalytic metals [14, 35, 52, 55, 87]. For this reason catalytic MOSFETs are generally operated in relatively high temperature range of 100–200 °C [35]. It is believed that hydrogen atoms diffuse through the 50 nm-thick Pt layer and adsorb at the Pt/Ti or Pt/TiO_x interface with an r-type adsorption mechanism giving rise to an increase of the work function.

The Pt charge variation with respect to operating temperature for H_2 concentration of 4% is shown in Fig. 4.34, and appears to increase strongly above 120 °C. Pt layer response in terms of charge variation as a function of hydrogen concentration at 130 °C is presented in Fig. 4.35. Pt exhibited a linear concentration dependence between 0.5 and 4%, without any saturation tendency in the studied range. Absolute values of obtained charge variations at temperature above 80 °C are more than two folds larger than values below this temperature. The observed signal is of great interest because it can be used to gate a FET, but also it did not exhibit any tendency toward saturation up to the highest studied concentration of 4%. In contrast to the s-type chemisorption at the Pt/SiO_2 interface and the Pt surface, the resulted signals start to saturate at respectively 1.5% [12, 16] and 2% [16, 24]. However the operating temperature is a

limit. At the operating temperature of 130 °C, the response time was about 30 s, larger than at 60 °C. This can be explained by the need of hydrogen diffusion through the Pt layer.

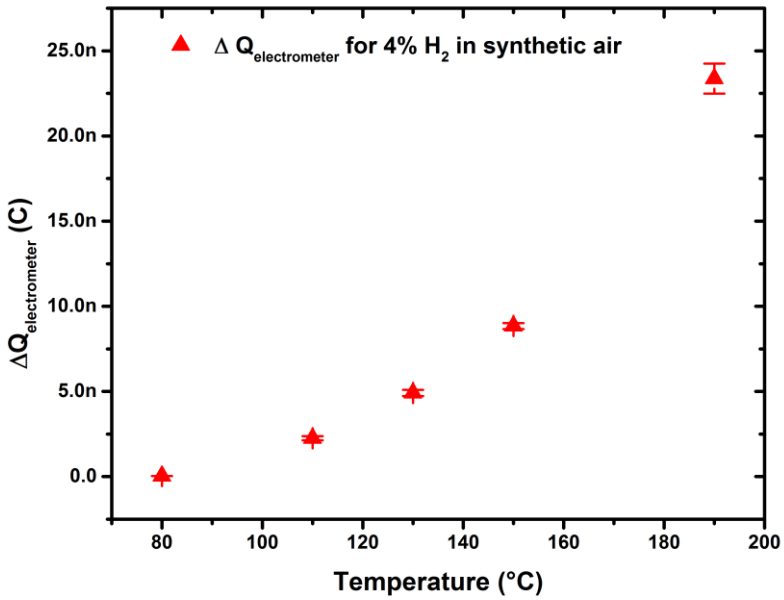

Figure 4.34 Pt layer charge variation response at varying temperature from 80 to 190 °C to hydrogen concentration of 4% in synthetic air.

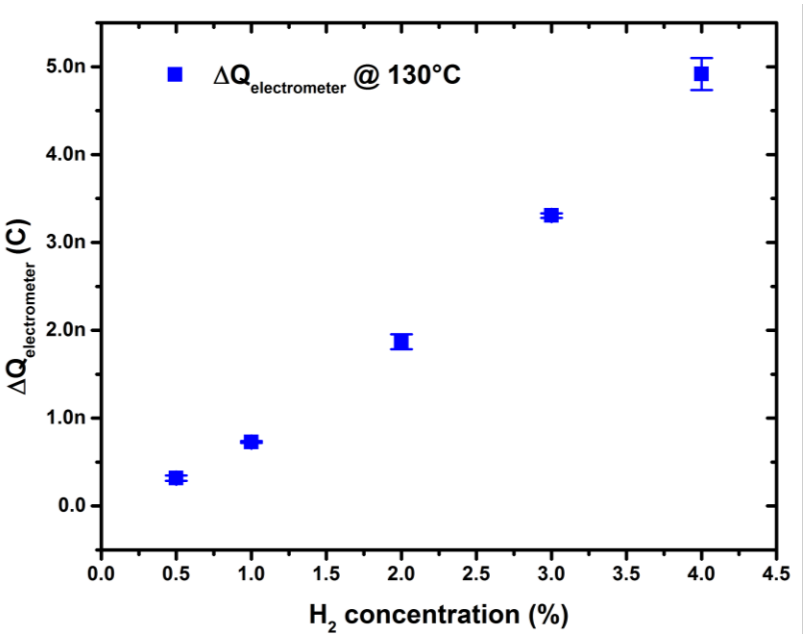

Figure 4.35 Hydrogen concentration dependence of platinum layer response in term of charge reading variation at 130 °C in synthetic air.

The proposed technique is based on measuring the material surface charge/potential variation induced by gas molecules adsorption. Knowing the surface charge variation of the floating functionalized gate of a DG-FET, the channel conductance variation can be estimated. The estimated material sensitivity is used for sensing layers sizing with regard to the transistor transfer function and target concentration range.

The proposed technique is easy to implement. Only the sample has to be placed inside a controlled atmosphere cell. In contrast to kP technique, the gas chamber has to be large enough to hold the entire probe set-up. A small cell makes it easy to control gas diffusion homogeneity and turbulences in comparison to larger gas chambers. In addition, In KP technique, the work function of the reference probe may be sensitive to the target gas and be a source of error by contributing to the obtained signal.

4.6 H_2 Sensing surface sizing for integration with a DG-transistor

The estimated Pt sensitivity to H_2 at 60 °C (see section 4.5) is used for sizing the needed sensing area for integration with both of the DG-SET and DG-FET based H_2 sensors. The Pt sensing pad is sized to ensure hydrogen detection at the concentration ranging from 0 to 4%. The sensor response is calculated to different concentrations and the sensor sensitivity is extracted.

4.6.1 H_2 Sensing with a DG-SET

A DG-SET, with the same parameters as considered in section 3.4.2, is considered for H_2 sensor response simulation. Considering the extracted Pt sensitivity to H_2 at 60 °C, the sensing area heated at 60 °C needed to detect hydrogen at concentration ranging from 0 to 4% is 0.36 µm^2. DG-SET hydrogen sensor response is shown in Fig. 4.36. The DG-SET is biased at $V_{Ds} = 155$ mV. The control gate bias is adjusted as for a gas sensor configuration. Extracted sensitivity from the linear region of 0–3% is 100 pA/%H_2. The ultra-reduced sensing area is a result of the large Coulomb peak slope and the reduced excursion window (see section 3.4.2).

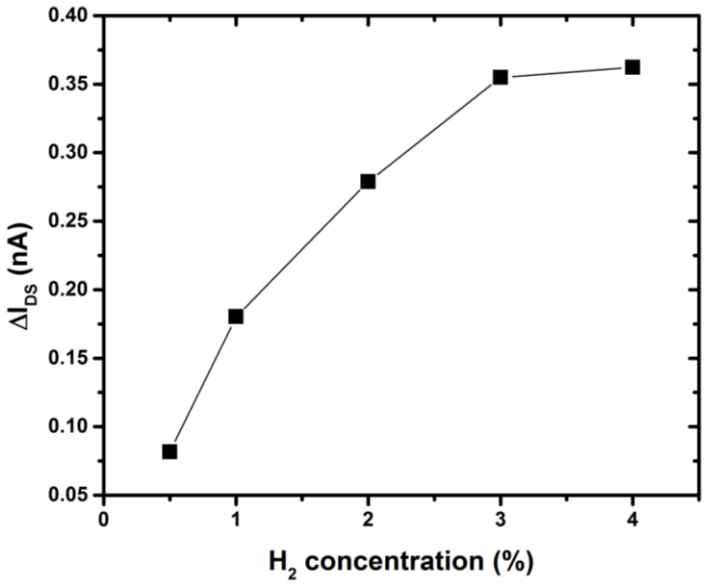

Figure 4.36 Pt-functionalized DG-SET-based H_2 sensor response to varying concentration.

4.6.2 H_2 Sensing with a DG-FET

An n-type UTBB FD-SOI MOSFET with the same parameters as considered in section 3.5.2 is considered for H_2 sensor response simulation. The sensor response is estimated for a device with $L = 30$ nm and $W = 0.5$ µm, and biased at $V_{ds} = 0.1$ V. The sensing Pt area needed to detect hydrogen at 60 °C and at concentration ranging from 0 to 4% is 60 µm^2. ${Q_{fg}}^0$ The charge present on the front gate in absence of the target gas ${Q_{fg}}^0$ is equal to + 486 aC. Fig. 4.37 shows the simulated FD-SOI FET hydrogen sensor response to varying hydrogen as current variation per unit hydrogen concentration. The extracted sensitivity from simulated response is 41 µA/%H_2. For 1 ppm H_2, the DG-FET sensor response is 4.1 nA, which is a noticeable current easily read, thanks to the high signal-to-noise ratio of such devices. The device power consumption is 1.23 µW.

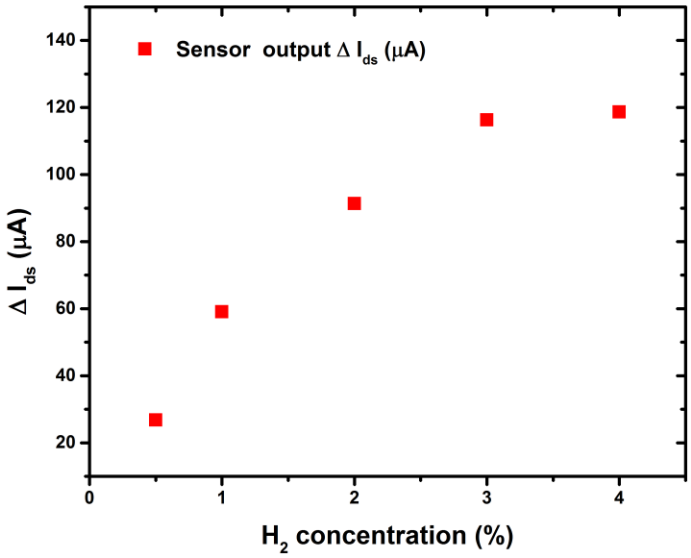

Figure 4.37 Pt-functionalized DG-FET-based H_2 sensor response to varying H_2 concentration.

The device is biased at $V_{gb} = -26$ V. This is due to the fact that ${Q_{fg}}^0$ is too large that it biases the transistor in the saturation regime. The large back gate bias is applied to bring the transistor operation point to the bottom edge of $I_{ds}\ versus\ Q_{gf}$ curve linear region slope (see section 3.5.2). If the ${Q_{fg}}^0$ is too large that a very large back biasing voltage is needed to set the transistor operation point in the linear region of the $I_{ds}\ versus\ Q_{gf}$ curve, it may be problematic because such large voltage is not used in integrated circuits. As an alternative, the DG-FET drain-source current is maintained constant by applying a counter back gate voltage. The transistor is controlled to be constant by a control circuit. The variation in the controlling back gate voltage constitutes the sensor signal. In such configuration, the choice of the operating constant drain-source current is imposed by the available range of back gate voltages (from -1 to 1 V in ICs). Simulated $I_{ds}\ versus\ V_{gb}$ curves for the same device as mentioned above and functionalized with a 60 μm^2-wide Pt sensing pad, with varying the H_2 concentration from 0 to 4%, are shown in Fig. 4.38. For response read at V_{gb} varying within the -1 – 1 V range (compatible with ICs employed voltages), the constant I_{ds} is set at 120 µA. The DG-FET H_2 sensor response, in such configuration has been simulated and is shown in Fig. 4.39. The extracted sensitivity from simulated response is 750 mV/%H_2. Thanks to a large coupling factor between the UTBB FD-SOI MOSFET front gate and back gate, the estimated H_2 sensor sensitivity is 3 fold larger than

SG-FET and Lundström FET-based hydrogen sensor sensitivities [16, 83, 84], typically ranging from 70 to 200 mV/%H_2 (in the few % concentration range). Such high sensitivity allows pushing down the detection limit. For 10 ppm H_2, the response ΔV_{gb} is estimated to be 0.75 mV, which is a noticeable signal easily detected with read-out electronics.

In such configuration the power consumption is increased up to 12 µW because of the drain-source current in the order of 120 µA (imposed by the back gate voltage range used for response read-out).

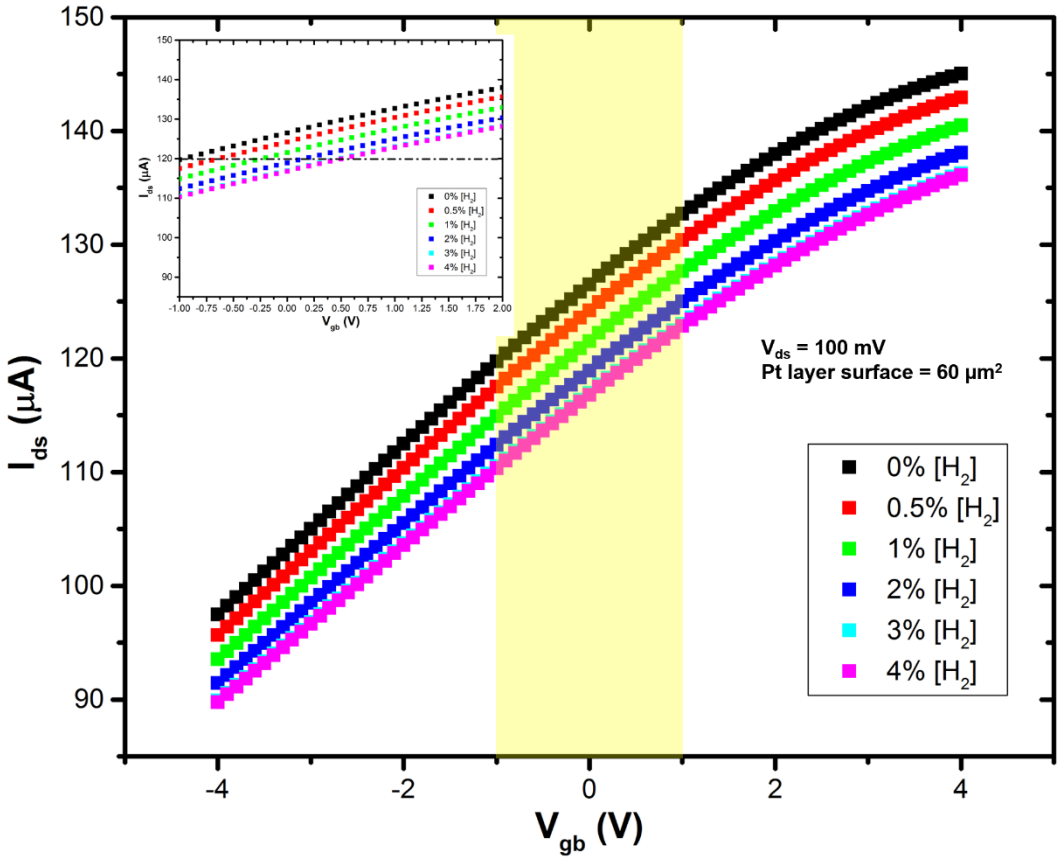

Figure 4.38 Simulated I_{ds} *versus* V_{gb} curves for $V_{ds} = 0.1$ V, a 60 µm^2-wide Pt sensing pad and channel parameters $L = 30$ nm, $W = 0.5$ µm, with varying the H_2 concentration from 0 to 4%. The V_{gb} range of interest in response read out is highlighted in yellow. Inset: a close up of curves for V_{gb} from -1 to 1 V.

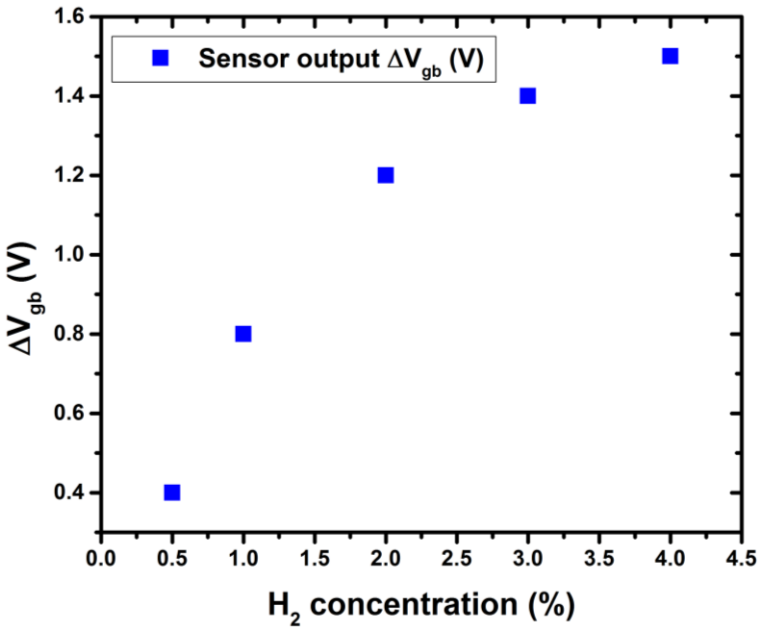

Figure 4.39 Pt-functionalized DG-FET-based H_2 sensor response, as a variation in V_{gb}, to varying H_2 concentration.

4.7 Conclusion

Sensitivity investigations by surface charge measurement can be applied to any type of sensing material where chemisorption or physisorption induce a surface charge variation. This technique allows for the estimation of the maximum surface charge variation which corresponds to the saturation of all possible adsorption sites. Also, sensitivity can be estimated and used for sensing layer design and sizing with regard to the transducer transfer function and target concentration range.

The experimental data for temperatures below 80 °C are in good agreement with literature and relevant to Pt integration with a DG-FET or DG-SET-type transducers. Hydrogen chemisorption at the Pt/Ti interface is interesting is terms of signal amplitude and linearity over the studied concentration range of 0.5-4%. Extensive investigation of H adsorption at Pt/Ti interface is needed.

The high sensitivity of studied DG-FET or DG-SET has allowed downscaling of the needed sensing surface. The Pt layer needed for integration with a DG-SET or a DG-FET (UTBB FD-SOI MOSFET), for H_2 detection in the 0–4%range was estimated to be 0.36 and 60 μm^2 respectively. The ultra-reduced Pt sensing area is unmatched in the FET gas sensors state of art.

Typical sensing areas in SG-FETs and Lundström MOSFETs are ranging from few hundreds of μm^2 to few mm^2. In gas sensors, heating the sensing layer is contributing the most to the gas sensor power consumption. The yielded reduced sensing layer is one of the main advantages of DG-transistor-based gas sensors because smaller surfaces will have less energy cost in term of heating and allow higher integration density very relevant to integrated sensor systems and e-nose applications.

Thanks to the amplification capability of UTBB FD-SOI MOSFET, the estimated H_2 DG-FET sensor sensitivity of 750 mv/%H_2 is large beyond reported sensitivities for Pt-MOSFETs and Pt-SG-FETs in literature. The high DG-FETs sensitivity is their strongest asset with respect to the FET-based gas sensor technology. Moreover, the estimated transducer power consumption of 12 µW is very relevant to ultra-low power gas sensing applications.

CHAPTER 5 Gas sensor integration and electrical characterization

5.1 Introduction

Over the past, several research teams have explored various designs and concepts for the demonstration of CMOS compatible SETs operating at room temperature and fabricated with a reproducible fabrication process. The so-called "*nanodamascene*" process has been one of the most promising routes toward realization of RT-operated SETs. In this chapter, a brief introduction and the evolution history of the *nanodamascene* process are given. The fabrication process, based on the "*nanodamascene*" process, is presented and different lithography patterns are described. Major fabrication issues and proposed solutions are discussed. For gas sensor integration, we opted for the FD-SOI FETs because they are a mature technology and well modelled. FDSOI MOSFETs are functionalized with Pt as a sensing layer for H_2 sensing. A developed functionalization process is presented.

5.2 DG-SET integration

5.2.1 The *nanodamascene* process

In 2007, the group of Pr D. Drouin from Université de Sherbrooke has demonstrated the fabrication of metallic SET operating at temperature up to 430 K [39] by the so-called "*nanodamascene*" process. The demonstrated SET consists in a 2–3 nm-thick by 10 nm-wide Ti nanowire interspersed by few-nm-spaced tunnel junctions formed by 8 nm-thick amorphous plasma grown TiO_x. The device was back-gated by the Si substrate. The SET charging energy was estimated at 457 meV- more than 12 times the value of thermal fluctuations at 433 K. The reported operating temperature of 430 K is below the upper temperature limit of conventional Si-FETs, "opening the door to hybrid designs" [39]. This fabrication process is a new approach for the fabrication of metallic SETs with total capacitance in the sub-atto farad range [28, 39]. This breakthrough has been recognized by the industry as a significant proof of the room temperature SET operation, and is referenced in the ITRS 2009 roadmap [95].

The *nanodamascene* process consists in combining e-beam lithography (EBL) and chemical mechanical planarization (CMP) to form a nanometre sized Ti island separated from drain and source by two very thin tunnel junctions, all of them embedded in Si oxide. The main process steps are presented in Fig 5.1. First, a narrow trench -few nanometres in width- is formed in a SiO_2 layer thermally grown on a silicon wafer, as shown in Fig. 5.1.a. The trench is patterned by a resistless first EBL (EBL#1) process. The SiO_2 layer is directly irradiated with low energy electron beam, modifying its density, and thus, its etch rate in a buffered hydrofluoric acid (BHF) solution. The depth and width are controlled by the EBL exposure dose and less than 15 nm-wide trench can be achieved. In a second step, a Ti perpendicular-to-trench line is defined by a second EBL (EBL#2) and deposited by lift-off process, as shown in Fig. 5.1.b. The Ti line is subsequently oxidized in pure oxygen to grow TiO_x on its sidewalls, creating the tunnel junction dielectric. In the next step, a Ti layer is deposited over the entire sample surface, as shown in Fig. 5.1.c. Then the sample is polished with a CMP process down to the SiO_2 surface to expose the buried structures. Patterned structures placed next to the device with depth of few nanometres less than the trench depth were used as a CMP end point detection technique. Polishing is stopped once these features started to disappear [28]. The device is a nanowire embedded in the silicon oxide with two tunnel junctions forming a SET island, with thickness down to 2 nm, thanks to CMP, as can be seen in Fig. 5.1.d.

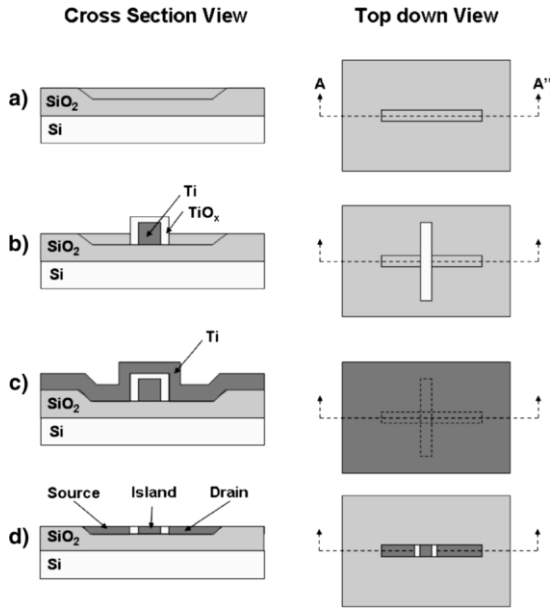

Figure 5.1 *Nanodamascene* fabrication process reported by Dubuc *et al.* [28]. The left side of each part of the figure is the cross section along the AA" axis.

The process has been modified and optimized to allow building a self-aligned side gate [28, 96] in order to address each transistor individually.

Two other main modifications have been made to improve the *nanodamascene* process [96]: (i) prior to EBL#1, electrical contact pads and leads for the source, drain and gate (micrometric structures) are patterned by UV lithography and transferred to the Si oxide by a dry etch; (ii) EBL#1 is carried out using an e-beam resist (PMMA[3]) and aligned to already UV lithography patterned structures. The EBL#1 pattern is designed to overlap already patterned source, drain and gate electrodes, and transferred to the substrate by a dry etch step. The use of PMMA resist was motivated by the fact it has a lower exposure dose than SiO_2, which allowed a great gain in writing time.

The self-aligned gate *nanodamascene* process has pathed the way toward multiple applications. The design has been modified to allow fabrication of devices as metallic nanowire (NW), metal insulator metal structure (MIM), single electron memory (SEM) [98], SET for charge detection [99], quantum cellular automata (QCA) [100] and tunnelling field effect transistors [101]. The process steps such as oxide plasma etch and CMP have been developed and optimized [98, 102, 103].

Because it is a low thermal budget processes (below 200 °C) and combines conventional fabrication techniques (UV lithography, EBL, CMP), the *nanodamascene* process is CMOS BEOL technology compatible, and with variations still enable SETs to be operated within a temperature range similar to other conventional Si-FETs [28, 39, 104]. This has motivated studies of logic SET-only circuit design as well as [105] and hybrid SET-CMOS circuit design [29, 105–108].

In 2011, based on *nanodamascene* process, the integration of metallic SETs in the Back-End-Of-Line of advanced CMOS technology has been demonstrated by Jouvet *et al*. [29], within collaboration between of University of Sherbrooke, CNRS[4] and STmicroelectronics. It is a proof of concept of possible 3D monolithic integration of single electron devices to add new and advanced functionalities to CMOS circuits, such as single electron memories, SET logic circuits,

[3] Polymethyl methacrylate (PMMA) is the standard high-resolution polymer E-beam resist [97].
[4] CNRS stands for The *Centre National de la Recherche Scientifique* (National Center for Scientific Research), which is a public organization under the responsibility of the French Ministry of Education and Research

sensors and SET-CMOS hybrid circuit for logic and memories [106]. The devices have been integrated within the inter layer dielectric (ILD) of CMOS circuit, as illustrated in Fig. 5.2, with preserving the functionality of underlying transistor layer.

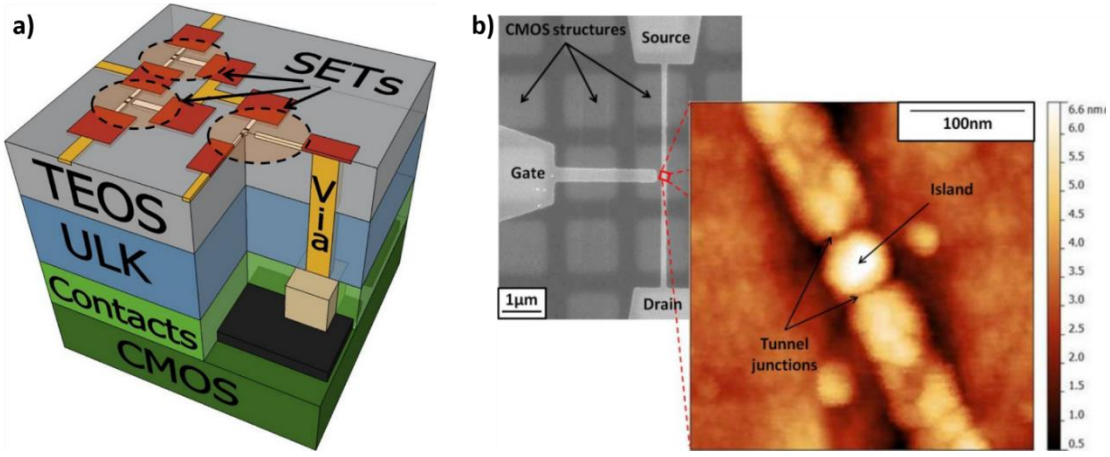

Figure 5.2 a) Schematic representation of a 3D hybrid SET-CMOS circuit with single SET level fabricated on a CMOS substrate. b) Left: SEM image of a SET fabricated on a CMOS substrate, right: AFM topography scan of integrated SET in the TEOS layer on top of the CMOS substrate. Reproduced from [29].

5.2.2 Fabrication process

Integration of metallic DG-SET, as a sensor transducer, on advanced CMOS substrate has been based on the *nanodamascene* process. The main process is still the same as reported in [106], but several steps have been optimized and lithography layouts have been adapted. The *nanodamascene* process is a versatile process which allows the fabrication at the same time of SETs, NW and MIM devices [98]. In the following we describe the (initial) fabrication process for a DG-SET. Process improvements and optimization are discussed in the section 5.2.3. The fabrication process is illustrated only for DG-SETs in Fig. 5.5. For NW and MIM devices, only EBL processes layout differs from SET ones. The EBL pattern design is presented in section 5.2.2.b.

Starting substrates were 28 nm-CMOS technology substrates [109] from STmicroelectronics with only the first metal interconnect level implemented. The substrates have a top layer stack of SiCN/SiOC/TEOS as illustrated in Fig. 5.3. A top view optical and SEM images of a CMOS

substrate are shown in Fig. 5.4. The SET were integrated within the 100 nm-thick TEOS[5] top layer.

Prior to processing, substrates are dipped in a piranha solution (1:4 H_2O:H_2SO_4) for 5 min, then rinsed with deionized water and dried under nitrogen, to remove organic and inorganic contaminants. The wet cleaning step is followed by exposure to a capacitively coupled O_2 plasma produced by 150 W RF power at 300mTorr for 5 min.

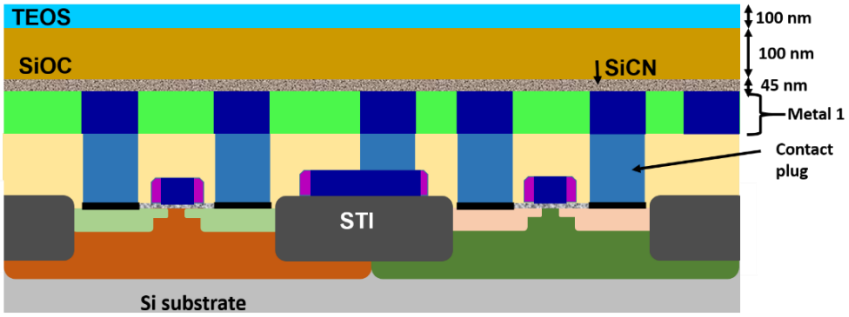

Figure 5.3 Schematic of CMOS substrates with the top layer stack of SiCN/SiOC/TEOS.

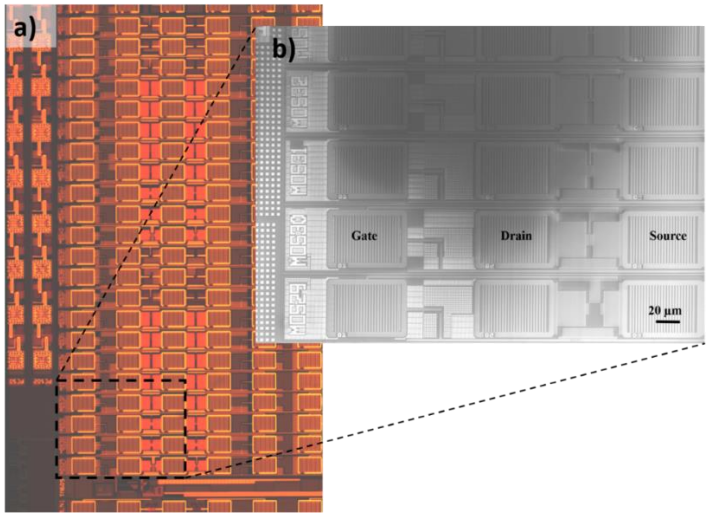

Figure 5.4 CMOS substrate with only the first metal interconnect level implemented. a) Optical image of a CMOS zone showing a matrix Cu stripped contact pads. b) An SEM image of the area delimited by dashed lines in a) showing the Cu structures beneath the SiCN/SiOC/TEOS stack.

[5] TEOS stands for TetraEthOxySilane: Si $(C_2H_5O)_4$, which is a silicate commonly used in IC interconnect technology as a dielectric material.

Similar to the process describes previously, UV lithography and EBLs are carried out subsequently to define the device structure. All these lithographic processes have been modified to be aligned to CMOS structures.

In the first step, micrometric contact electrodes, pads and leads, and CMP sacrificial structures (dummies) are patterned by a first UV lithography (UV1) and transferred to the substrate by plasma etching, as illustrated in step #1 of Fig. 5.5. The optical lithography is aligned on CMOS structures beneath the SiCN/SiOC/TEOS layer stack. A positive photoresist (S1805) is deposited on the samples by spin-coating at 5000 rpm for 5 min and thermally cured on a hotplate at 115 °C for 60 s. After UV optical lithography, the photoresist layer is developed by puddling AZ MIF319 developer twice for 15 s.

Afterwards, UV1 patterned contact electrodes and dummies are dry etched into the TEOS layer by RIE process using a CF_4 based etching chemistry. The system used is a Multiplex Advanced Oxide Etch (AOE) inductively coupled plasma (ICP) system from Surface Technology Systems with an electrostatic chuck. A CF_4/H_2/He gas mixture is used at a flow rate of respectively 12, 14, 140 sccm, and at a total pressure of 4 mTorr. CF_4 yield both ions and radicals. Both of the coil and the platen are RF powered at 13.56 MHz. The platen temperature is controlled by helium flow and kept constant at -20°C.

The micrometric pattern has been etched down either 60 nm or 40 nm with vertical or 70°-angled sidewalls. Vertical and 70°-angled sidewall TEOS RIE processes have been developed within the research group and are detailed respectively in [103] and [110]. Table 5.1 gives an overview of both processes parameters.

Table 5.1 TEOS RIE process parameters.

	Vertical sidewall TEOS RIE process	**70°-angled sidewall TEOS RIE process**
Pressure (mTorr)	4	4
CF_4 flow rate (sccm)	12	12
H_2 flow rate (sccm)	14	14
He flow rate (sccm)	140	140
Coil power (W)	100	100
Platen power (W)	50	10
Platen temperature (°)	-20	-20

In the second step, a first EBL (EBL1) is used to define the 20 nm-wide transistor channel and the gate box along with contact leads in an electroresist using a modified scanning electron microscope (SEM) at 20 kV. Samples are spin-coated with ZEP520A, a positive e-beam resist, diluted in anisole with a ratio of 2.4:1, at 5000 rpm for 30 s. Then, the resist is baked on a hotplate at 180 °C for 5 min. Resist deposition process yields 80 nm-thick layer, which is, with regard to the resist etching selectivity, sufficient for the subsequent plasma etching of 20 nm-deep nanometric structures. After e-beam writing, resist is developed by dipping in O-xylene at room temperature for 75 s and rinsed in MIBK[6] for 15 s followed by drying under N_2. A post bake is carried out for 3 min at 115 °C to improve resist etch resistance and reduce line edge roughness, as reported in [103]. The nanoscaled pattern is etched 20 nm-deep into the TEOS layer, as illustrated in step #2 of Fig. 5.5, using the same plasma etching process described previously.

[6] Méthyl-4 pentanone-2

In the next step, the island is deposited through a second EBL (EBL2) and lift-off metallization. The patterning process has been developed within Marc Guilmain Ph.D. research project and is detailed in [98]. A bilayer resist stack of MMA/ZEP520A is used to obtain the undercut structure needed for the lift-off process. MMA[7], a copolymer, diluted in Ethyl L-lactate (EL) with a ratio of 2:1, is first spun at 5000 rpm for 30 s and baked at 180 °C for 5 min. Thereafter, ZEP520A diluted in anisole with a ratio of 4.2:1, is spun at 5000 rpm for 30 s and baked at 180 °C for 5 min, to yield a very thin layer and have better resolution.

A narrow line with the target width of 20 nm is defined, by EBL, perpendicular to the etched source/drain channel trench and across the gate box, as shown in step #3 of Fig. 5.5. The e-beam resist is also patterned to deposit metal rectangle overlapping the gate box by the same lift-off process, as shown in step #3 of Fig. 5.5.

The ZEP520A is developed by dipping in O-xylene for 75 s. The 2:1 MMA:EL is developed by dipping subsequently in a 4:1 IPA[8]:H_2O solution for 2 min at 20°C. The sample is dried under N_2 and the development process is followed by exposure to capacitively coupled O_2 plasma at 50W, and 800mTorr for 12 s, to remove residual resist waste in the openings without enlargement of the patterned narrow line. Afterwards, a 25 nm-thick Ti layer is deposited by e-beam evaporation at a deposition rate of 5 A/s. Finally, lift-off is used to remove the resist from the sample and leave Ti in the defined region. Details on the lift-off metallization and its development can be found in [98].

Once the deposition of the SET island is carried out, the tunnel junction dielectric can then be deposited. Initially few nanometres grown TiO_x by oxidation in pure O_2 plasma was used. The use of dielectric materials deposited by atomic layer deposition (ALD) such as Al_2O_3 has been also considered and applied. The motivation of such is the instability of the Ti/TiO_x junction system and oxygen diffusion, discussed in section 5.2.3.a.

In the next step, etched structures into the TEOS layer are filled by the deposition of a 150 nm-thick Ti blanket layer, as illustrated in step #5 of Fig. 5.5. Ti layer deposition is done by RF magnetron sputtering of a Ti target with Ar ions using SPT320 sputter deposition system from

[7] Methyl methacrylate
[8] Isopropanol

Plasmionique. The choice of sputtering technique over thermal evaporation is discussed and detailed in [111]. Alternatively a bilayer of TiN/Ti 5 nm/150 nm is used instead of the 150 nm Ti layer to address the instability of the Ti/TiO_x junction system and oxygen diffusion. The bilayer is deposited in-situ by same technique (see section 5.2.3.a).

Finally, CMP is processed to remove the excess of Ti on top of the TEOS layer surface leaving embedded metal structures. Further CMP iterations are carried out to thin more the obtained devices only few nm. Both of SEM and atomic force microscopy (AFM) observations, in addition to NW resistivity measurement are used to control the planarization process. 1x1 cm^2 samples area polished using an Alpsitec E460 system, an H_2O-based 50 nm-sized silica slurry and a polishing pad made of rigid micro-porous polyurethane material (model IC1000). The slurry solution is diluted with IPA at 1:1 and has a pH of 9.5.

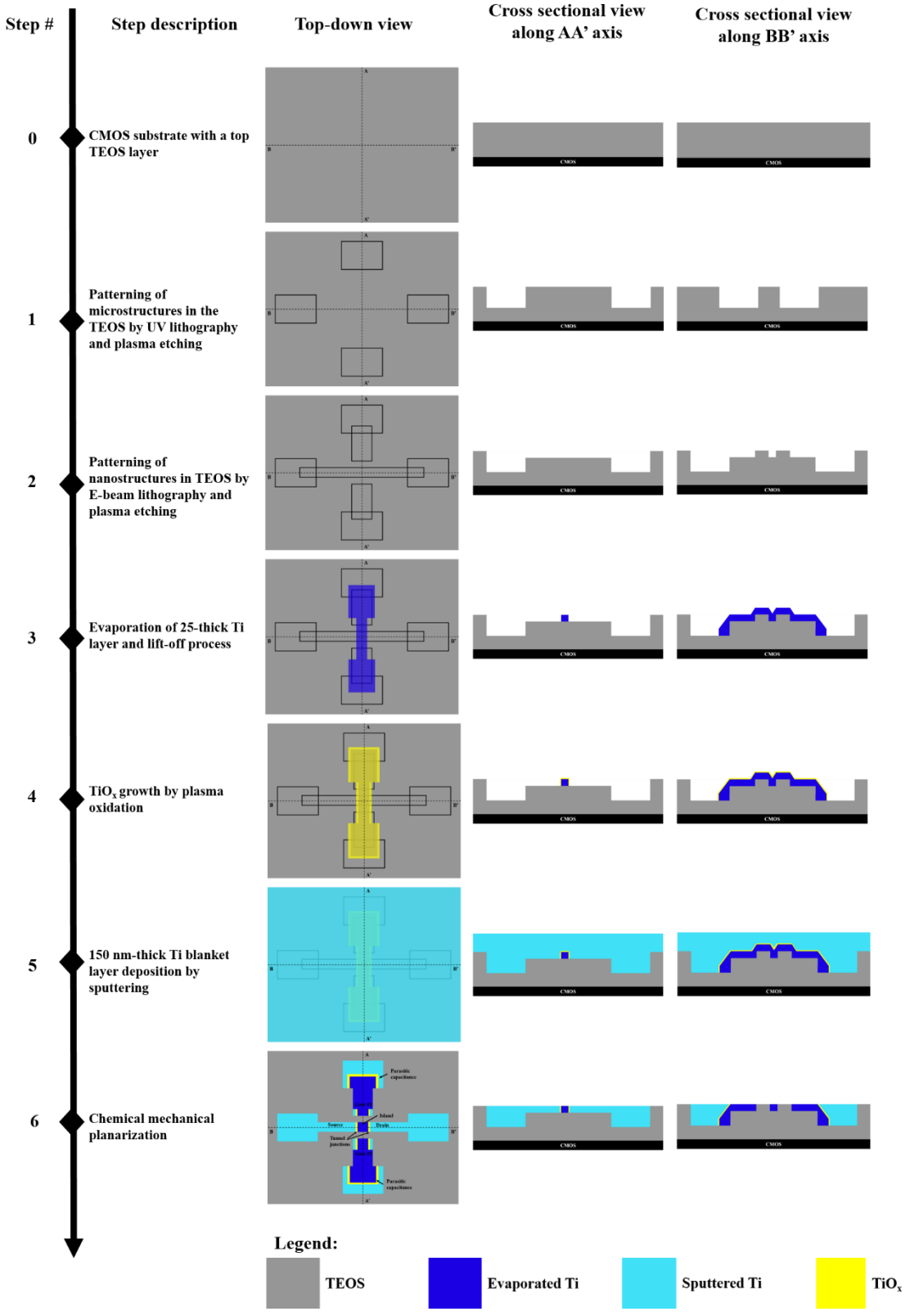

Figure 5.5 DG-SET fabrication process flow.

5.2.2.a UV lithography layout

As detailed above, the first optical lithography (UV1) is used to pattern microstructures, with dimensions equal or larger than 2 µm, into the TEOS layer. This step allows formation of contact leads and pads along with sacrificial structures for CMP (dummies). The optical lithography mask layout can be found in Appendix D. The mask has been designed with regard to 6 CMOS zones identified within the 31.94 mm width by 51.64 mm length CMOS substrate. Six dies were designed and placed superposed over the CMOS zones (see Fig. D.1). In each die centre is placed a matrix of identical cells with size of 360 by 520 μm^2 (highlighted in yellow in Fig. D.1). The optical lithography pattern is aligned on Cu structures beneath the TEOS layer, shown in Fig. 5.6. After etching down the features and resist stripping (see Fig. 5.10), the CMOS substrate is diced into 6 1x1 cm^2 sized samples. The layout of a cell is presented in Fig. 5.7 with a close up of the central region. In each cell, there are four electrode triplets. EBL zones highlighted in blue in Fig. 5.7 are located between the electrode triplets (for source, drain and gate). As can be seen in Fig. 5.7 and 5.8, contact leads and pads are designed to be stripped with 2 µm-wide lines.

The microstructure layout is important and has a strong impact on planarization uniformity. In the following, the pattern density is defined as the ratio of Ti surface by the total surface (Ti + TEOS). It has been found that increasing pattern density and decreasing line width decrease dishing of SiO_2 surface because it is faster polishing than Ti and due to "the transition from a dishing (isolated lines) to an erosion regime (array of lines)" [111]. TEOS and SiO_2 have very close removal rates.

To optimize planarization uniformity, minimize dishing and low contact resistance, all the micrometric features are kept in the 2 µm-range with a pattern density of 50% (Fig. 5.7). Large area with no active feature over the sample surface is paved with 2 µm-square-shaped-dummy structures, as can be seen in Fig. 5.7. This is to have the optimum 50% density with increased Ti structure circumference to surface ratio. Because polishing of Ti structure is an "edge first", increasing Ti structure edge circumference increases the removal rate and thus improves the global planarization.

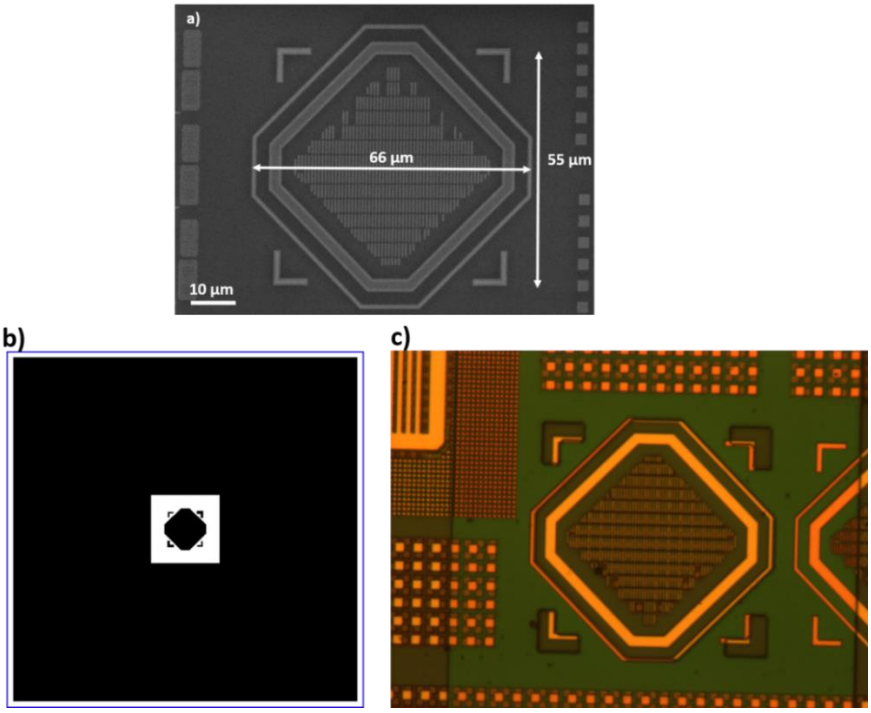

Figure 5.6 UV1 alignment mark and feature. a) SEM image of typical Cu alignment mark used for UV1. b) Alignment feature design from the UV lithography mask. c) Optical image of the Cu alignment mark taken after resist development.

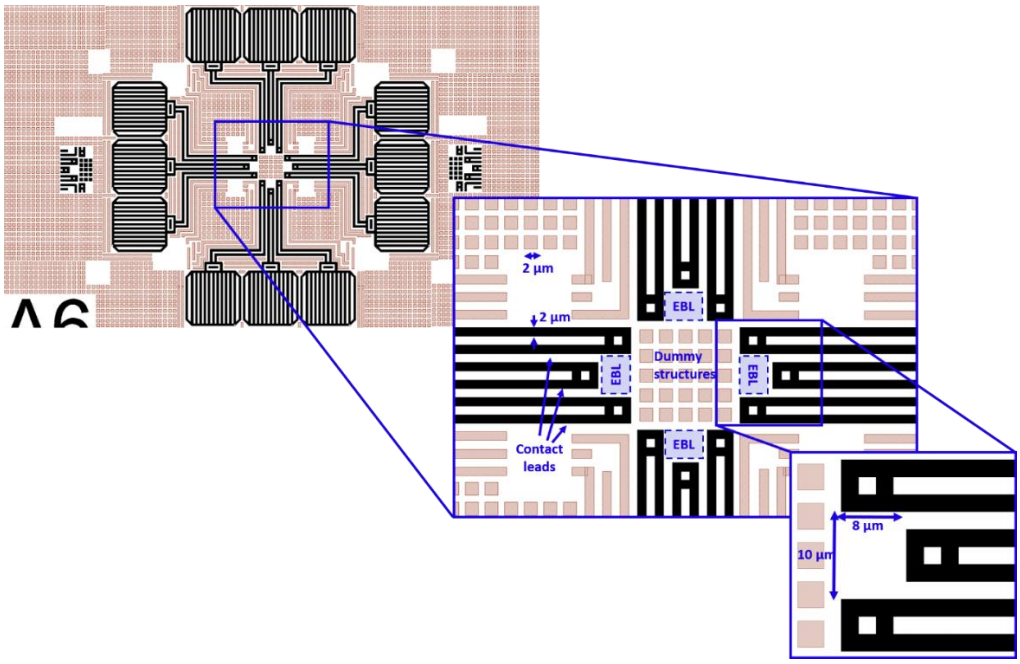

Figure 5.7 a UV1 cell layout. Middle: a close up the central zone with the four electrode triplets. EBL zones are highlighted in blue. Right: a close up of the EBL zone with area of 8 by 10 µm^2.

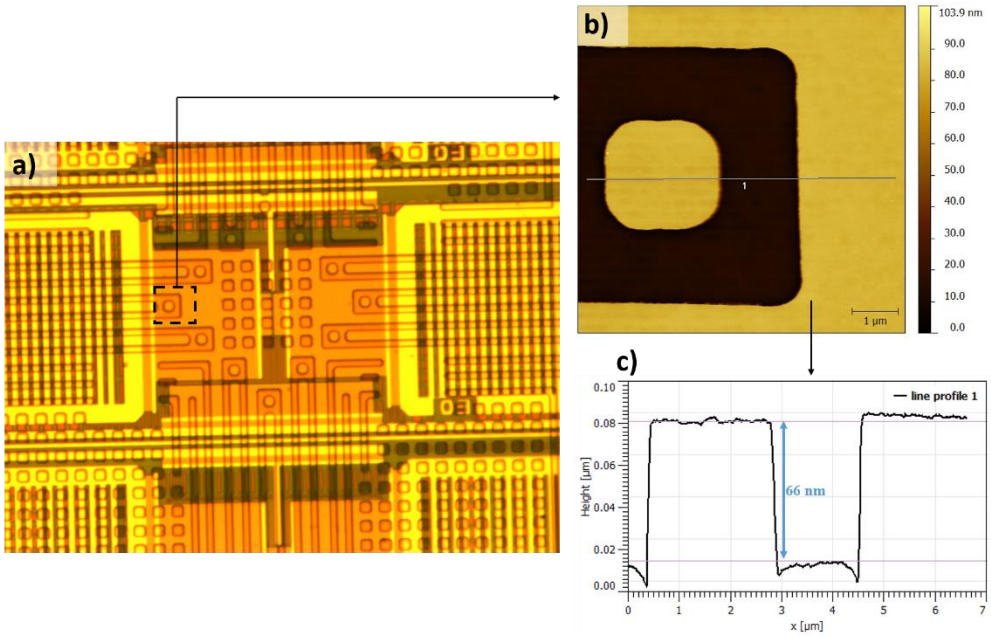

Figure 5.8 Optical image of a cell after resist development. b) AFM scan of the area delimited by dashed lines in a) after UV1 pattern plasma etching 60 nm-deep into the TEOS layer and resist stripping, showing the line profile extracted in c).

5.2.2.b E-beam lithography layout

Both of EBL1 and EBL2 processes are critical since they strongly affect final device dimensions and yielded capacitances. In addition, through the EBL1 process nanoscaled dummies are patterned in close vicinity of the active device (transistor channel and contacts), strongly affect the CMP process.

E-beam lithography processes, EBL1 and EBL2, have been carried with a SEM modified with a Nabity NPGS pattern generator software. The layout of the EBL pattern has been designed using DesignCAD LT 2000 software. EBL1 and EBL2 patterning processes are both aligned on CMOS structures beneath the TEOS layer. The alignment error is within the ±50 nm range. It is mainly due to the SEM stage drift over time, SEM scan pixel size and temperature variations, in addition to charging effect.

The EBL1 pattern design in shown in Fig. 5.9. In addition to SET, NW and MIM devices have been fabricated. In each cell two SETs, a MIM and a NW have been designed within the four EBL zones, as can be seen in Fig. 5.9. The EBL1 pattern is the same for the three device types. In Fig 5.10, the EBL1 pattern with “fan”-type design is shown. EBL1 patterned contact leads

(source, drain and gate), drawn in blue in Fig. 5.10, are designed to overlap with patterned UV1 contacts with respect to the maximum alignment error. In the close proximity of the NW trench (transistor channel trench), drawn in red in Fig.5.10.b, a line array is designed. These lines, drawn in pink in Fig. 5.10.b, serve as line dummies. Large area around are paved with square-shaped dummies. Line dummies width and pitch have been designed to respect the pattern density rule of 50%. Another EBL1 pattern with "comb" design, illustrated in Fig. 5.11, has been also used for the EBL1 process. The EBL1 pattern is transferred to the TEOS layer by RIE. The features are etched down 20 nm deep and obtained structure is shown in Fig. 5.12.

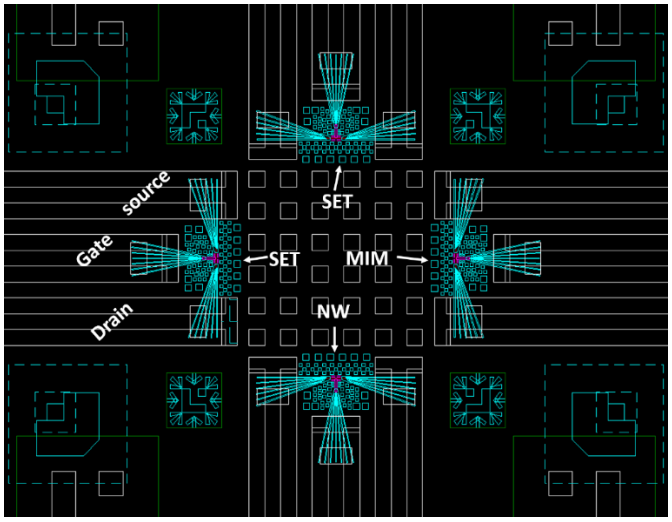

Figure 5.9 EBL1 layout. Nanometric contact leads, the NW trench, gate box and dummies are patterned by the EBL1 process.

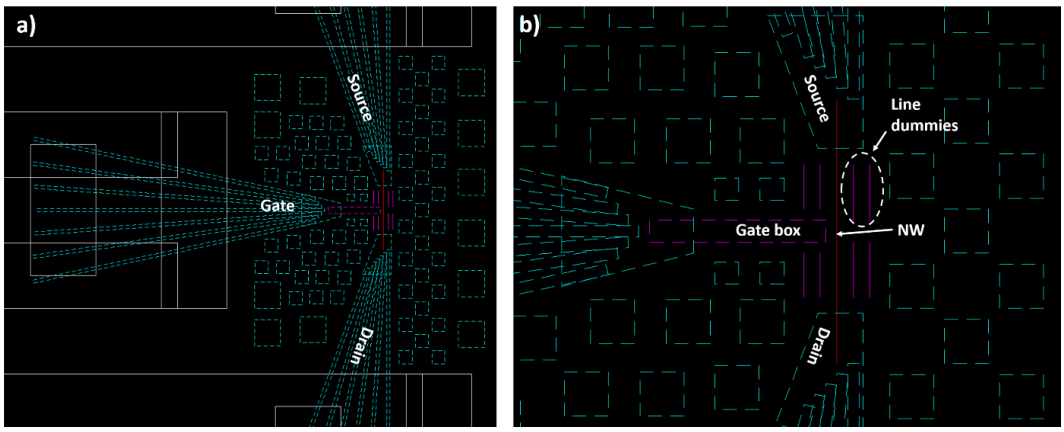

Figure 5.10 EBL1 layout of a SET with "fan"-type design. a) EBL1 pattern showing the overlap between UV1 patterned leads and EBL patterned leads. b) A close up of the EBL1 layout showing the EBL patterned line and square-shaped dummies, contact leads and the NW (the channel trench).

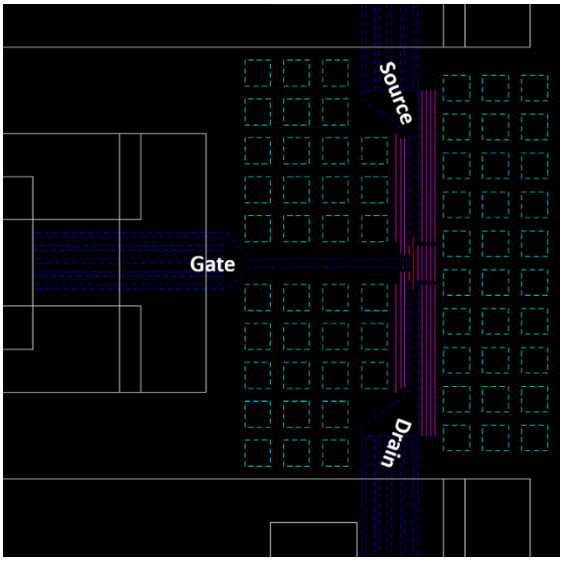

Figure 5.11 EBL1 layout of a SET with “comb”-like design.

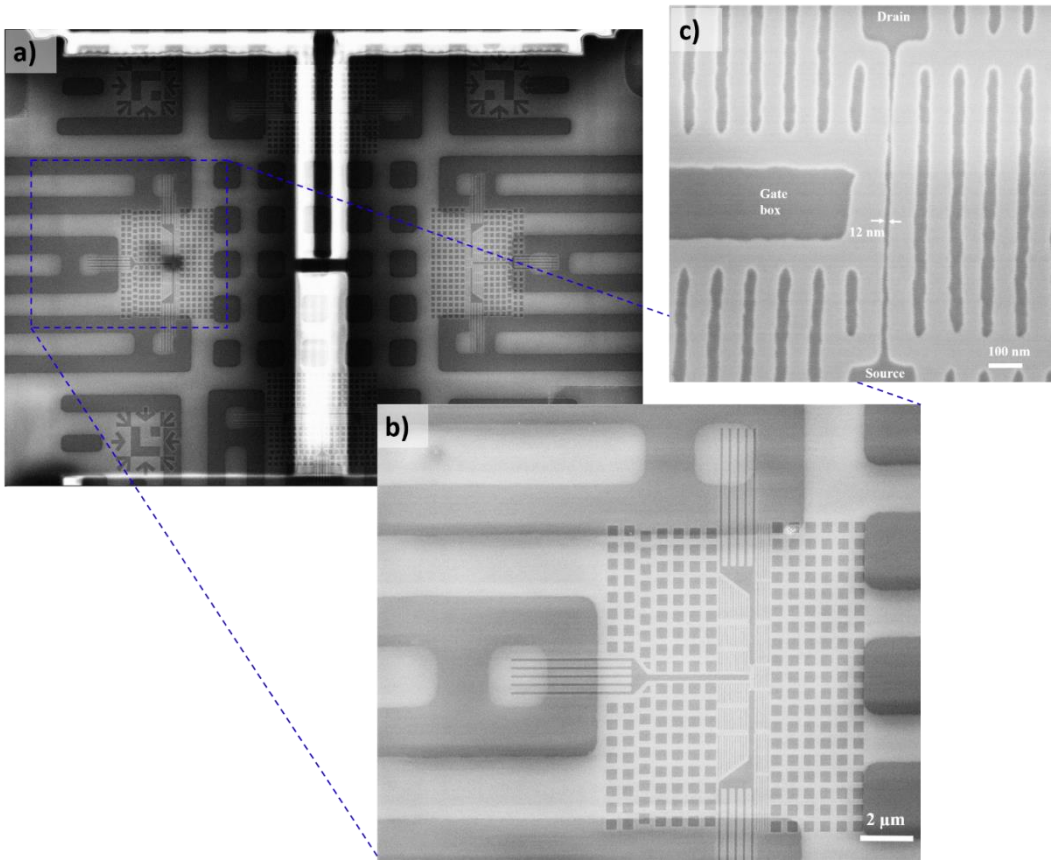

Figure 5.12 Structure after etching down 20 mn deep the EBL1 pattern (comb type) into the TEOS layer. a) SEM image of a cell. b) A close up of a device EBL zone. c) A close up of the gate box and the NW trench.

Only the SET and MIM devices are concerned by the EBL2 process since there is no need to form a tunnel junction for the NW. The EBL2 pattern corresponding to "fan"-type design is presented in Fig. 5.13 for both device types. For the SET, a Ti polygon is designed to cover the whole EBL1 gate lead pattern and be overlapping with the gate box, as shown in Fig. 5.13.a and Fig.5.13.b. The interface between this EBL2 patterned polygons and the UV patterned electrode corresponds to a parasitic capacitance in series with the gate capacitance. A Ti line overlapping with the rectangle is designed to be perpendicular to the trench (NW), as shown in Fig. 5.13.b. For the MIM device, a Ti polygon is designed superposed over only one EBL1 patterned contact lead, as can be seen in Fig. 5.13.c and Fig. 5.13.d. Similar to the SET gate, the interface between this EBL2 patterned polygons and the UV patterned electrode corresponds to a parasitic capacitance in series with the MIM capacitance. The Ti features are deposited by 20 nm-thick Ti layer evaporation and lift-off process. The structure is shown for a SET device in Fig. 5.14.

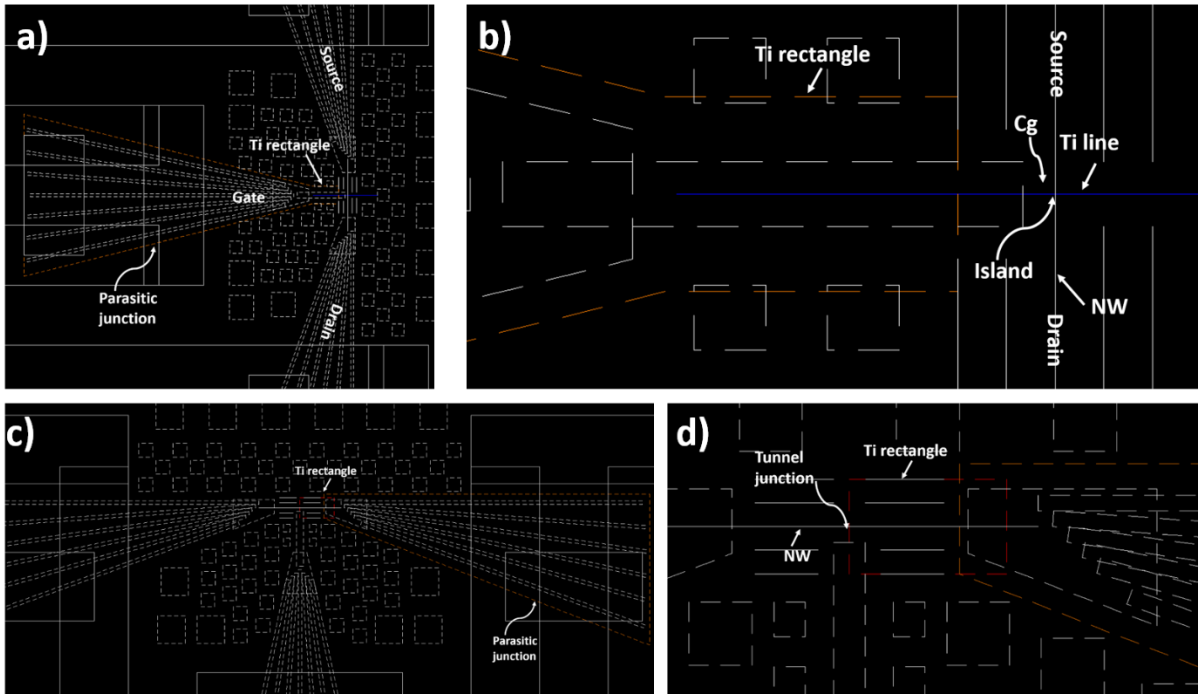

Figure 5.13 EBL2 layout SET and MIM devices. a) EBL2 pattern of a SET. b) A close up showing the overlap between the Ti rectangle and the gate box. c) EBL2 pattern of a MIM structure. d) A close up showing the overlap between the Ti rectangle and the EBL1 patterned electrode.

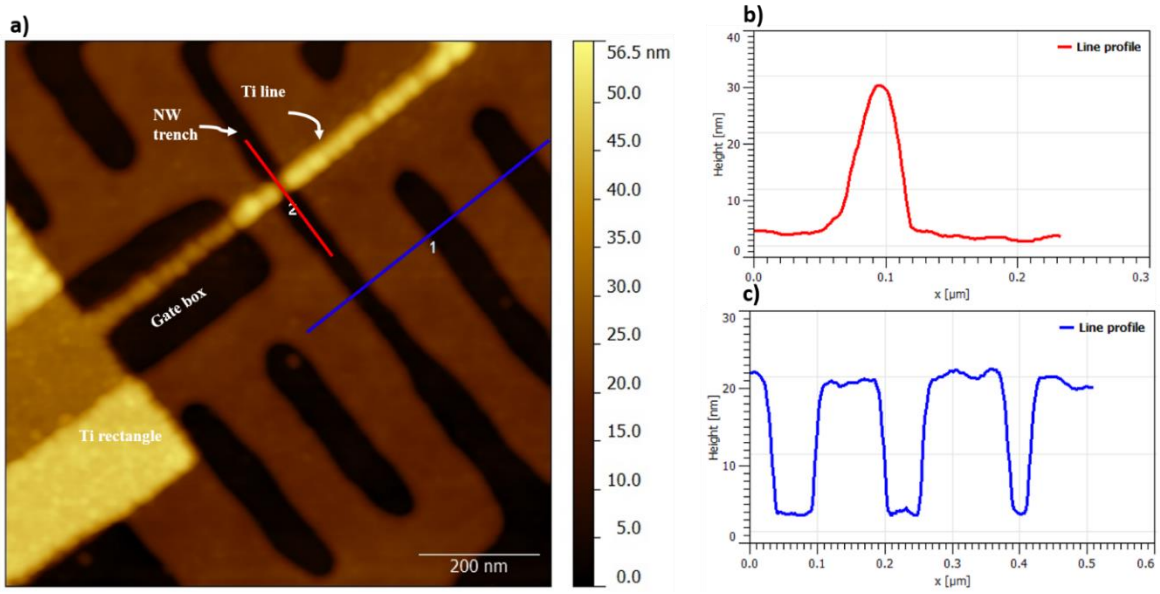

Figure. 5.14 Structure of a SET device after EBL lift-off process. a) AFM scan of a SET device EBL zone showing line profiles extracted in b) and c).

5.2.3 Fabrication process optimization

5.2.3.a Tunnel junction dielectric

It has been reported that Ti/TiO_2 as junction material system is not stable over because of oxygen diffusion from TiO_x into Ti. $Ti/TiO_2/Ti$ MIM devices have exhibited critical aging behaviour and degradation of electrical characterization. This due to the fact that the oxide barrier is degraded to a point where the junction is short-circuited. The potential barrier is physically deformed [112]. Two strategies have been considered to overcome this issue: (i) implementation of a diffusion barrier and (ii) Replacing the tunnel junction dielectric with a stable material. TiN has been implemented as a diffusion barrier.

Prior to Ti blanket deposition (just after TiO_x growth), the island is capped with a 5 nm-thick TiN layer deposited on samples by RF magnetron sputtering. The deposited thin TiN layer is conformal and prevents diffusion of oxygen from the TiO_2 into the Ti electrode.

Replacing the TiO_2 by ALD-deposited Al_2O_3, as a more stable material, with still TiN as a diffusion barrier has been also considered. A batch of samples with different Al_2O_3 thicknesses have been fabricated. After Ti lift-off process, a few nm-thick Al_2O_3 film (1–3 nm) is deposited by ALD followed by an in-situ deposition of 25 nm-thick TiN layer.

5.2.3.b Chemical mechanical planarization process

CMP step is very critical because it has to be controlled in the nanometre range to obtain devices with the desired thickness. Meanwhile it has been very challenging to achieve such goal, since on top of the sample surface both microstructures and nanostructures are present. In addition several materials may be present also such as TEOS, tunnel junction dielectric (Al_2O_3 or TiO_x), sputtered titanium, evaporated Ti, ALD deposited TiN or sputtered TiN. In the following, CMP related issues, adopted solutions and results are detailed.

Chemical mechanical planarization observations

SEM observations of devices after CMP iterations have revealed two major anomalies:

- A non-homogenous planarization over devices of the same cell.
- A non-homogenous planarization over all sample cells.

Fig. 5.15, presents SEM observations of the same cell through the CMP process (UV and EBL1 features are etched with vertical sidewalls, the UV features are 60 nm-deep, the junction dielectric is an in-situ plasma grown TiO_x). SEM observations have shown that first UV patterned structures are released from the Ti blanket layer while the EBL patterned structures are still encapsulated. After further CMP iterations upper SET and MIM devices are still encapsulated in the Ti layer while the two other devices are already released, as can be seen in Fig. 5.15.c.

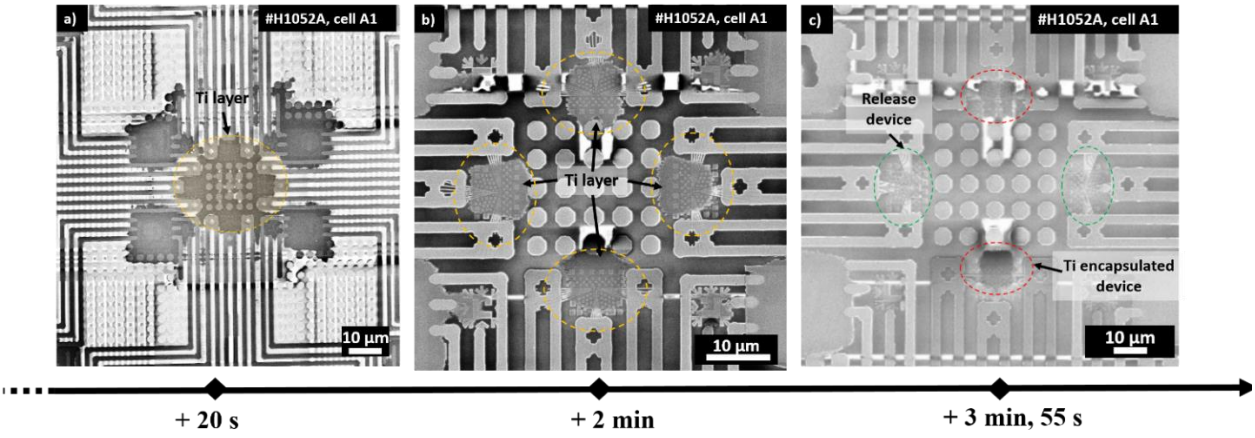

Figure 5.15 SEM images of the same cell of a sample through the CMP process. a) After several CMP iterations b) After further few CMP iterations (2 min more of total processing). c) After further few CMP iterations (3 min and 45 s more of total processing).

Fig. 5.16, presents SEM observations of different cells of the same sample over the last CMP steps (UV and EBL1 features are etched with vertical sidewalls, the UV features are 60 nm-deep, the junction dielectric is an in-situ plasma grown TiO_x, TiN/Ti bi layer blanket is deposited to fill the etched features). The CMP is stopped because processing further steps may lead to the device overpolishing and it has been preferred to carry out electrical characterization on already released devices. A comparison between several cells (A1, B1, C1 and D1) of the same sample after several CMP steps has pointed out a non-homogenous planarization. As can be seen in Fig. 5.16, in cells B1 and C1 all the devices, not only have been released from the Ti blanket layer but have also been overpolished and EBL patterned contact leads have been cut off leading to open circuit devices. Cell A1 and D1 exhibited the same behaviour through the CMP process: upper SET and MIM devices are still encapsulated in the Ti layer while the two other devices are already released. This observation has been made for several other samples (see Fig. 5.15.c and 5.16.a. Taking into consideration that Cu structures under the EBL zones beneath the TEOS layer are the same for cell A1 and D1 as well as for cells B1 and C1, the hypothesis that the TEOS topography is the cause behind the obtained planarization issues, has been investigated. AFM topography scans of the EBL zones have confirmed the expressed hypothesis. Fig. 5.17 shows AFM scans of two EBL zones of cell A1. TEOS layer topography exhibits variations in the 5 nm range.

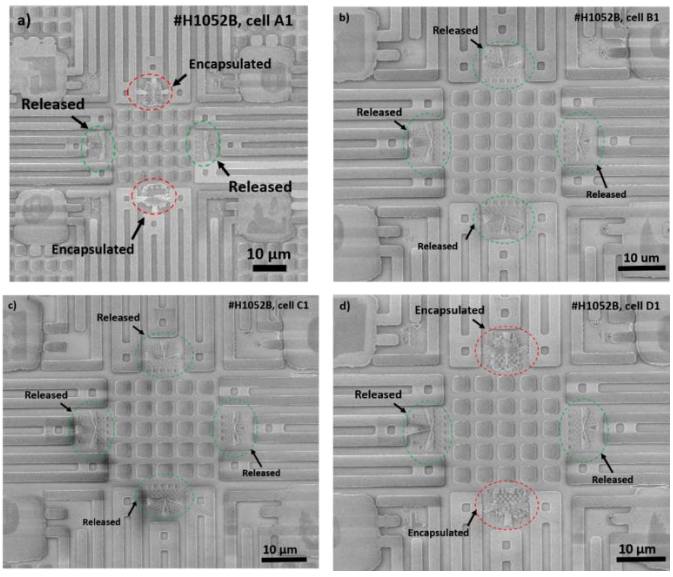

Figure 5.16 Comparison between different cells of a same sample after several CMP iterations. a) SEM image of cell A1. b) SEM image of cell B1. c) SEM image of cell C1. d) SEM image of cell D1.

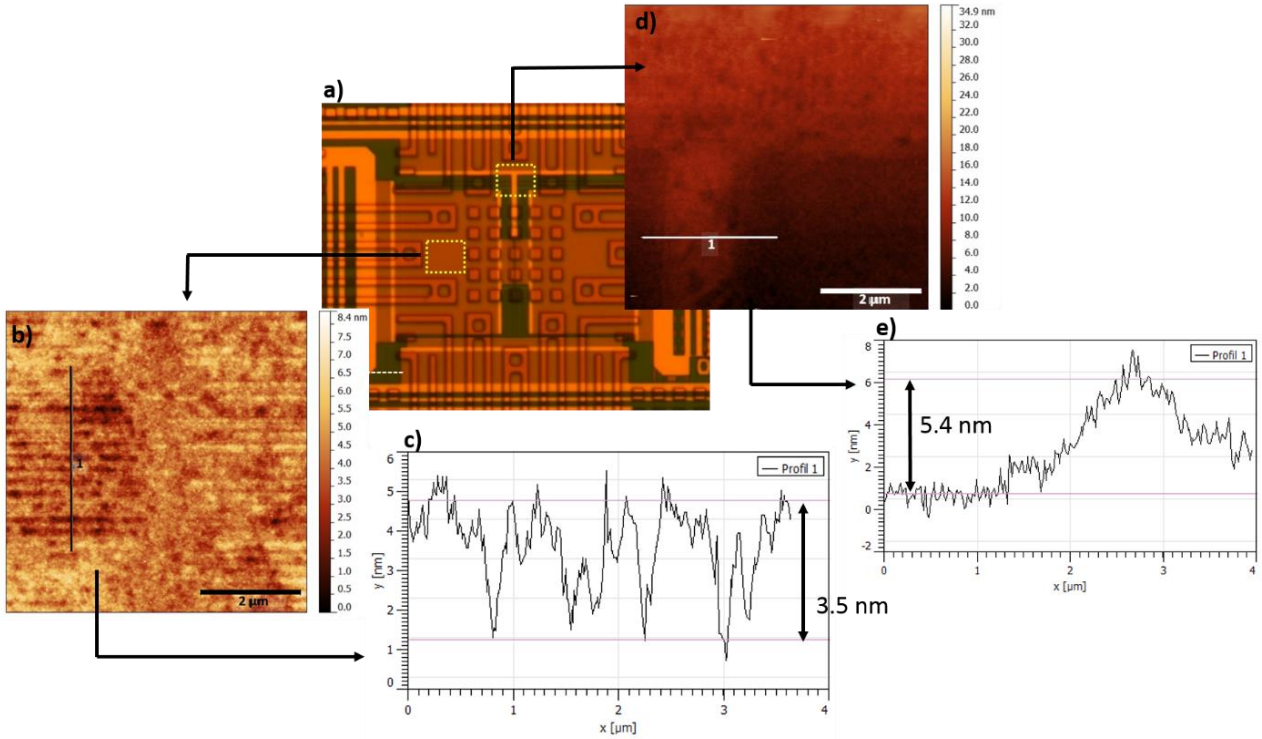

Figure 5.17 EBL zones topography characterization. a) Optical image of cell A1 taken after UV1 process development showing AFM scanned areas shown in d) and d). b) AFM topographic scan of the left SET EBL zone showing the line profile extracted in c). d) AFM topographic scan of the upper SET EBL zone showing the line profile extracted in e).

Due to non-homogenous planarization, processing further CMP iterations to release encapsulated devices from the Ti blanket layer has been at the expense of already released devices. AFM scans, presented in Fig. 5.18, 5.19 and 5.20, show devices overpolishing. EBL patterned contact lead combs cut off in the region close to the UV features (Fig. 5.18, 5.19 and 5.20) has been observed. It is due to the fact that these EBL features are in the close vicinity of micrometric features (UV patterned). In addition, both types of features have different depths. Initially, EBL patterned and UV patterned features are 20 and 60 nm deep respectively. Cavities and voids have been observed in the Ti transistor channels or nanowires, as can be seen in Fig. 5.19 (highlighted in green), and at the EBL patterned leads and UV patterned electrodes interface, as can be seen in Fig.5.20. It is due to an inappropriate filling of trenches during the Ti blanket layer deposition. The circumvent of this issue is discussed below.

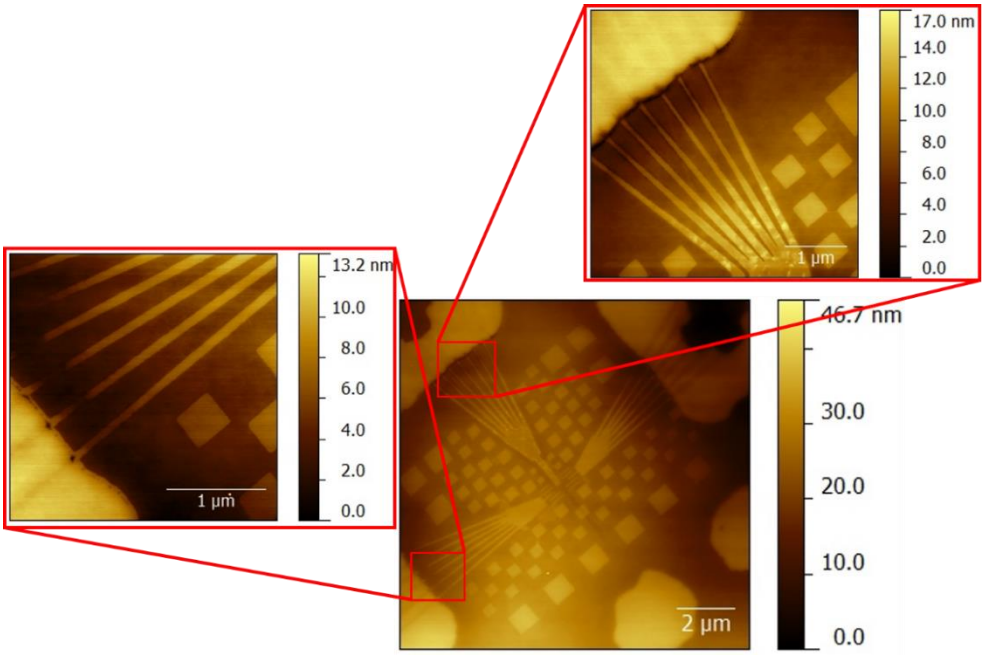

Figure 5.18 AFM scan of a SET device. Left: a close up of the overlap between the EBL patterned source/drain leads and the UV patterned electrodes showing the "erosion" of the former. Right: a close up of the overlap between the EBL patterned gate lead and the UV patterned electrodes showing no "erosion".

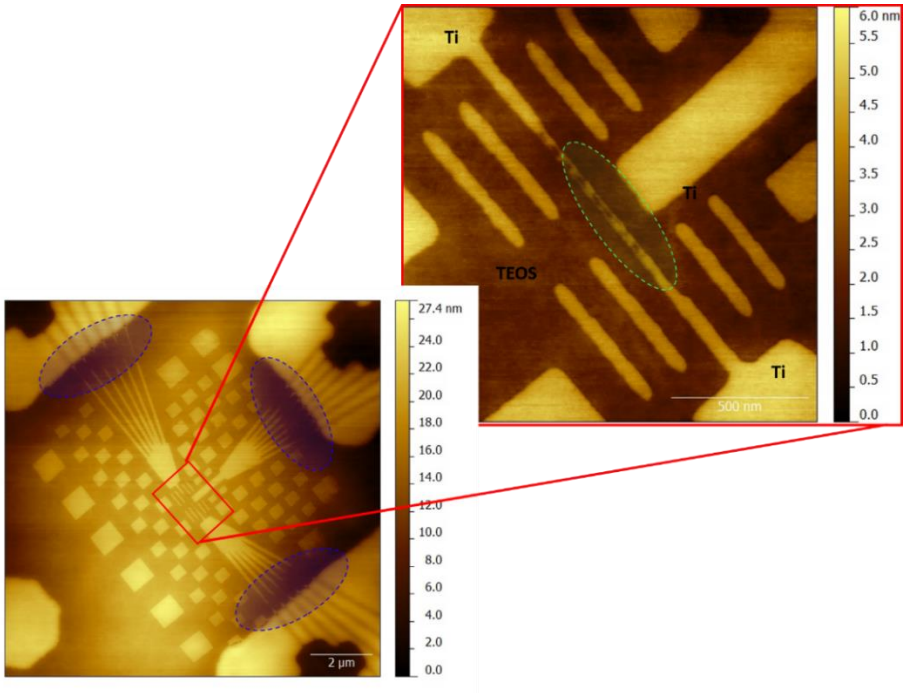

Figure 5.19 AFM scan of a NW device. Cut off EBL contact leads are highlighted in green. Right: a close up showing the cavities in the 20 nm wide Ti NW.

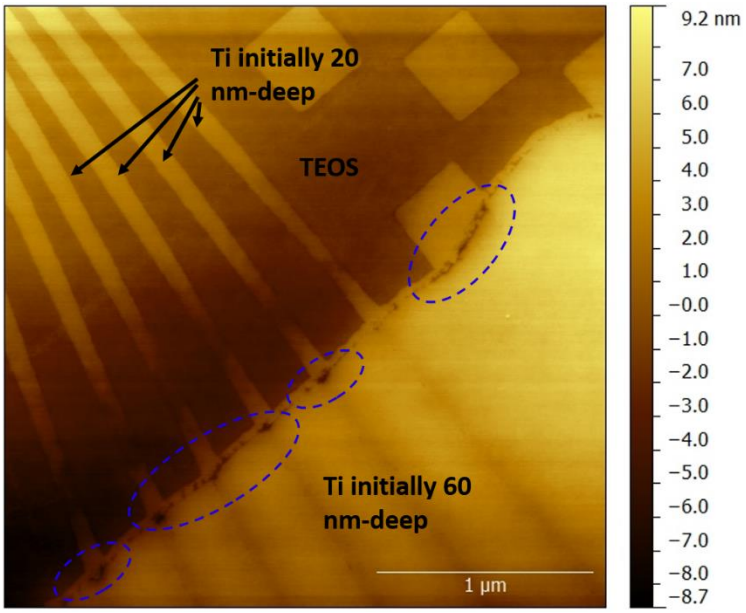

Figure 5.20 AFM scan of the overlap between the EBL patterned contact lead and the UV patterned electrode. Cavities at the interface are highlighted with blue dashed circles.

UV lithography mask and E-beam lithography layout optimization

Taking into consideration the observed issues with CMP, a new optimized optical lithography mask has been designed. The new UV mask layout is presented in Fig. 5.21. Cells matrix has been wisely placed so that the EBL zones are located on regions where the TEOS layer topography exhibits very slight variations and relative uniformity. Each cell provides ten electrodes, as illustrated in Fig. 5.21.b. They have been designed to have source to drain or drain/source to gate distances equal to 2 µm, as shown in Fig. 5.21.c. The aim is to reduce EBL zone surface and improve planarization.

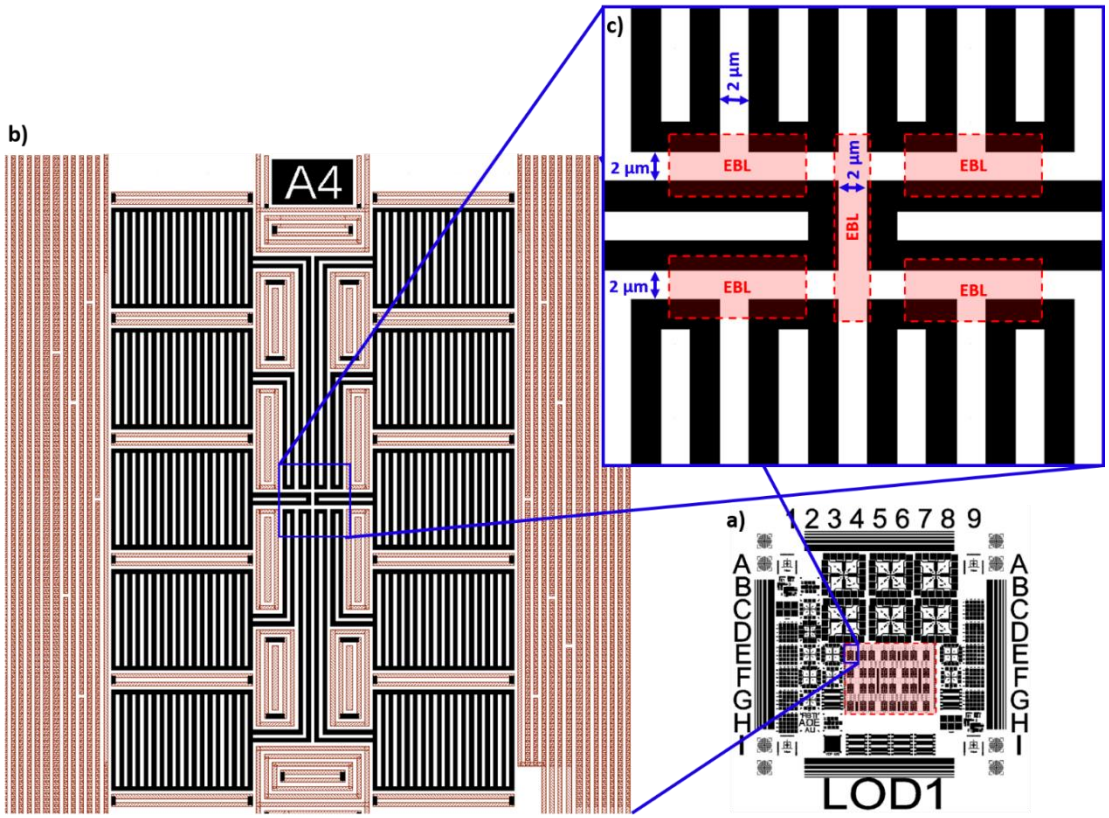

Figure 5.21 New UV lithography layout. a) Die layout with cell array highlighted in red. Dummies have been removed for clarity. b) A cell layout showing line dummies paving regions between contact pads and leads. c) A close up of a cell centre region showing EBL zones highlighted in red.

New EBL patterns have been designed. EBL1 and EBL2 layout for SET, MIM and DG-SET devices are presented in Fig. 5.22, Fig. 5.25 and Fig. 5.28 respectively. Contact leads have larger comb fingers than the previous layout with a width of 400 nm. With respect to the 50% pattern density rule and to avoid overpolishing, only line dummies have been used for paving the area around the devices because they have been found to yield better and faster planarization compared to square shaped ones. For SETs, the Ti polygon overlapping the gate box was abandoned and kept only for the MIM device. For MIM devices it is preferred to have a greater parasitic capacitance in series with the tunnel junction capacitance otherwise both capacitances will be comparable. For the SET the parasitic capacitance in series with the gate capacitance is not dramatic (SETs are characterized in the DC regime).

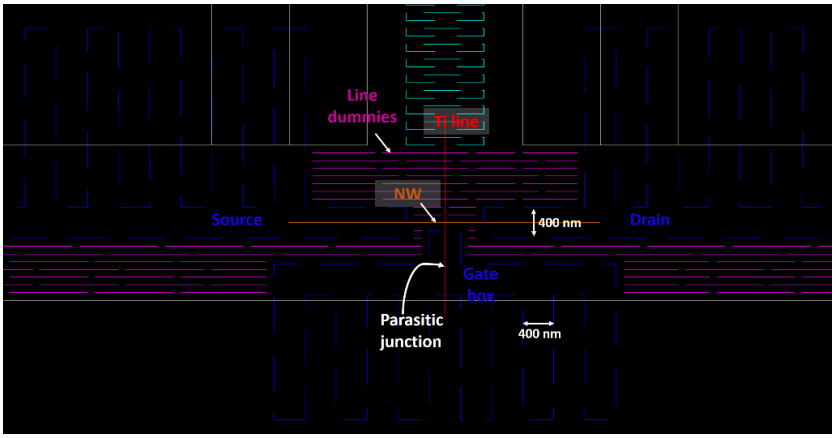

Figure 5.22 EBL1 and EBL2 layouts of a SET.

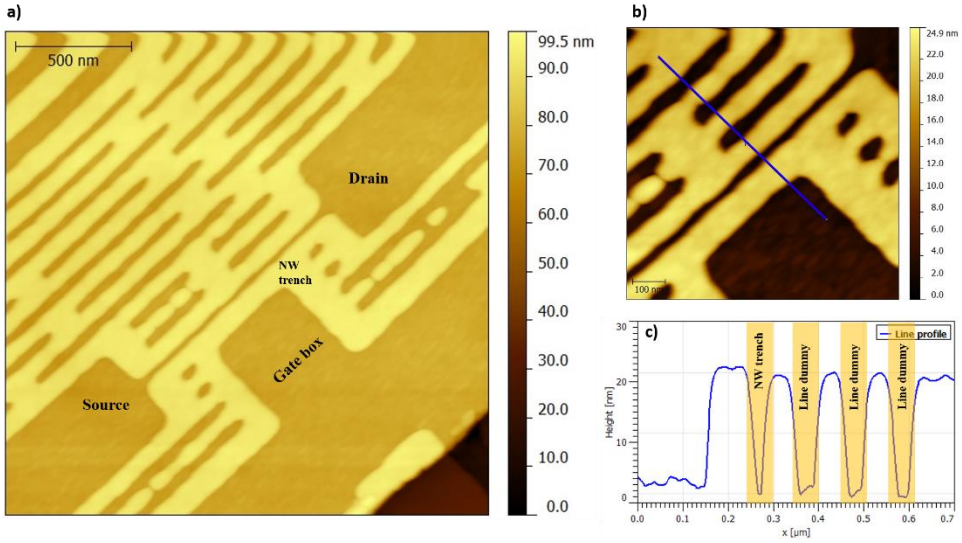

Figure. 5.23 Structure of a SET device after etching down 20 nm deep the EBL1 pattern into the TEOS layer. a) AFM scan of a SET device EBL zone. b) A close up of the NW trench and the gate box showing the line profile extracted in c).

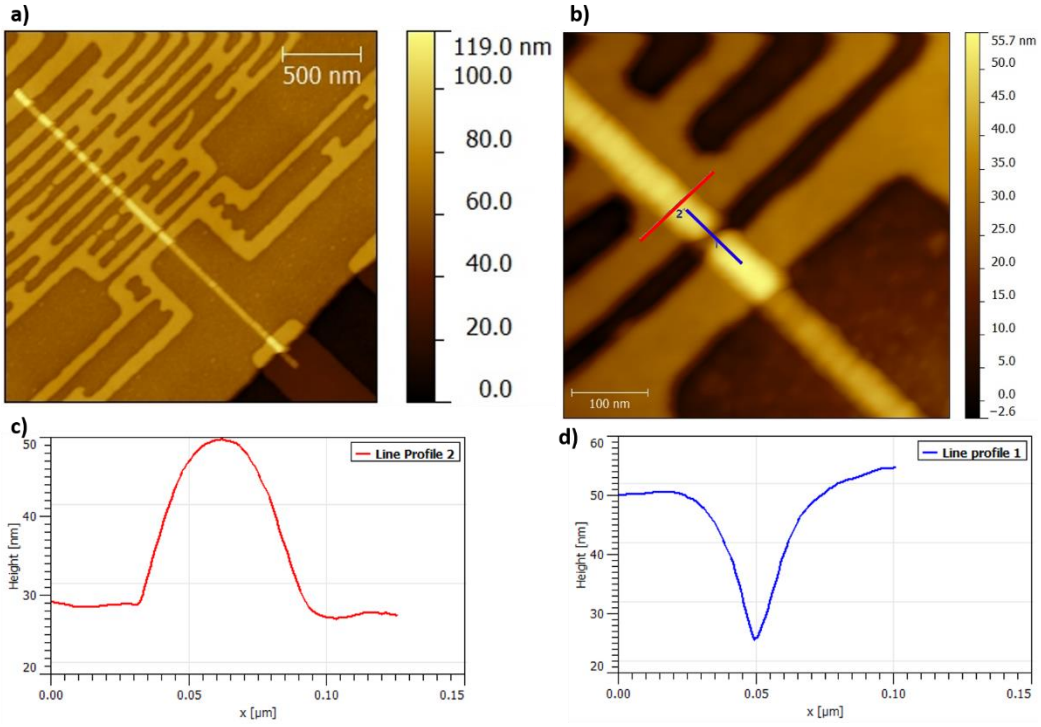

Figure. 5.24 Structure of a SET device after EBL lift-off process. a) AFM scan of a SET device EBL zone. b) A close up of the NW trench and the gate box showing line profiles extracted in c) and d).

The structures for the SET and the DG-SET devices with the new optimized after EBL1 plasma etching are shown in Fig. 5.23 and 5.24 respectively. The structures for the SET and the DG-SET devices after EBL1 plasma etching are shown in Fig. 5.26 and 5.27 respectively.

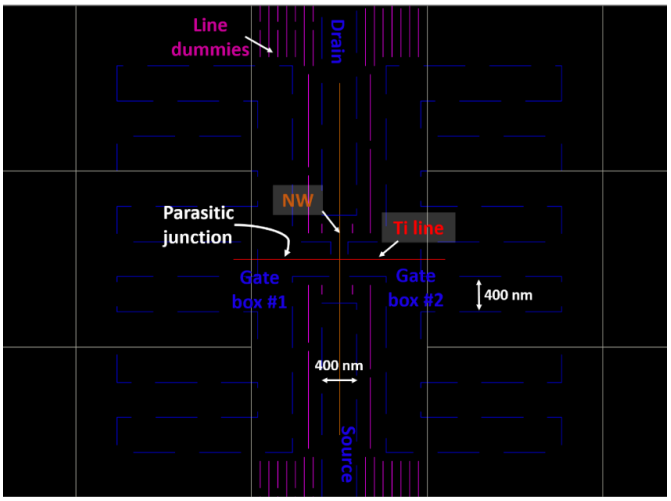

Figure 5.25 EBL1 and EBL2 layouts of a DG-SET.

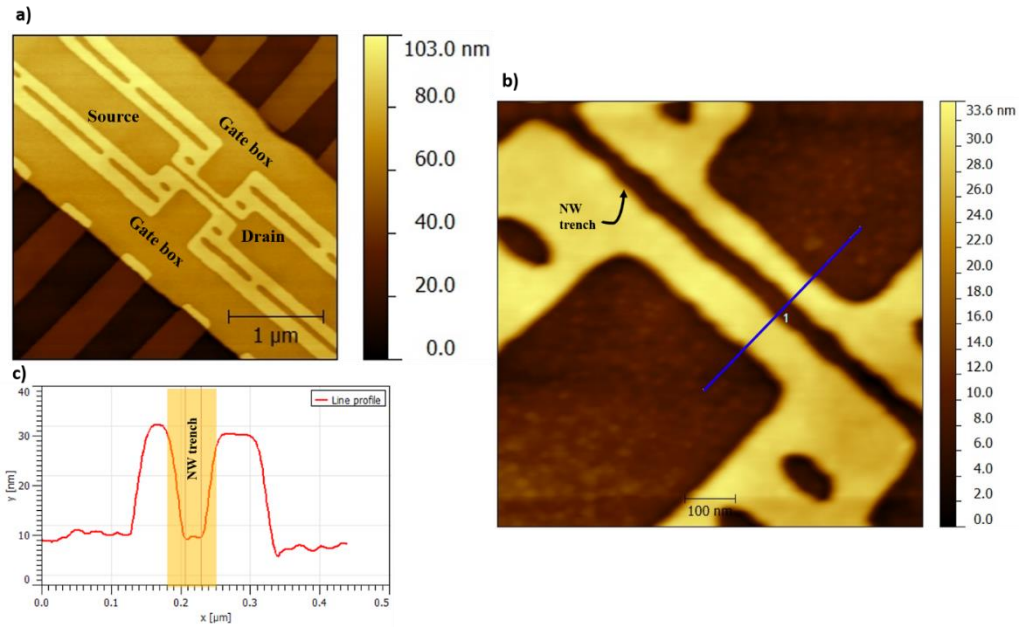

Figure. 5.26 Structure of a DG-SET device after etching down 20 nm deep the EBL1 pattern into the TEOS layer. a) AFM scan of a DG-SET device EBL zone. b) A close up of the NW trench and the two gate boxes showing the line profile extracted in c).

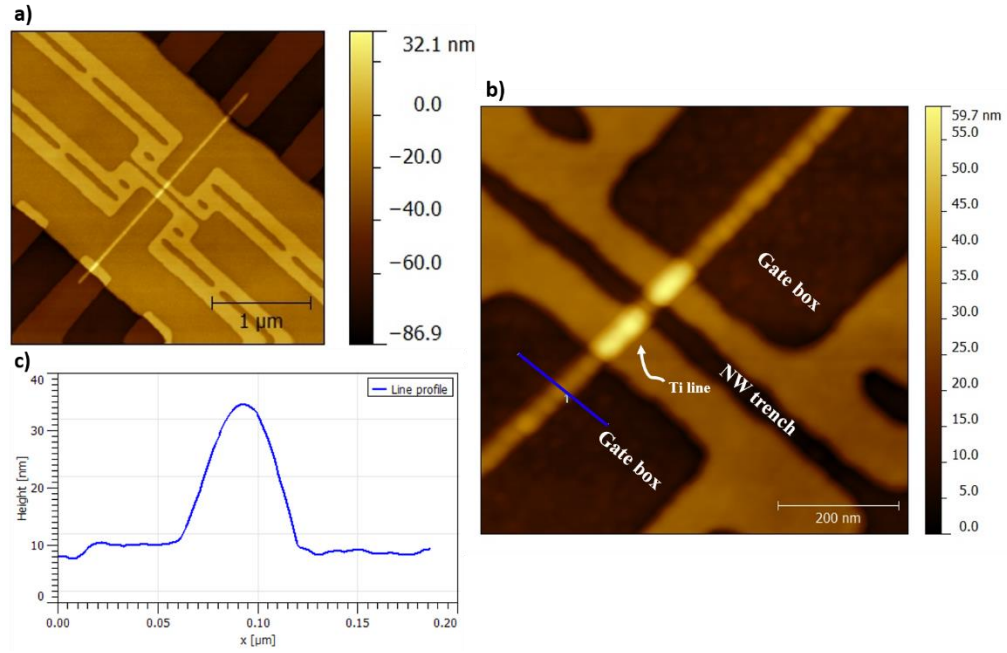

Figure. 5.27 Structure of a DG-SET device after EBL lift-off process. a) AFM scan of a DG-SET device EBL zone. b) A close up of the NW trench and the two gate boxes showing line profile extracted in c).

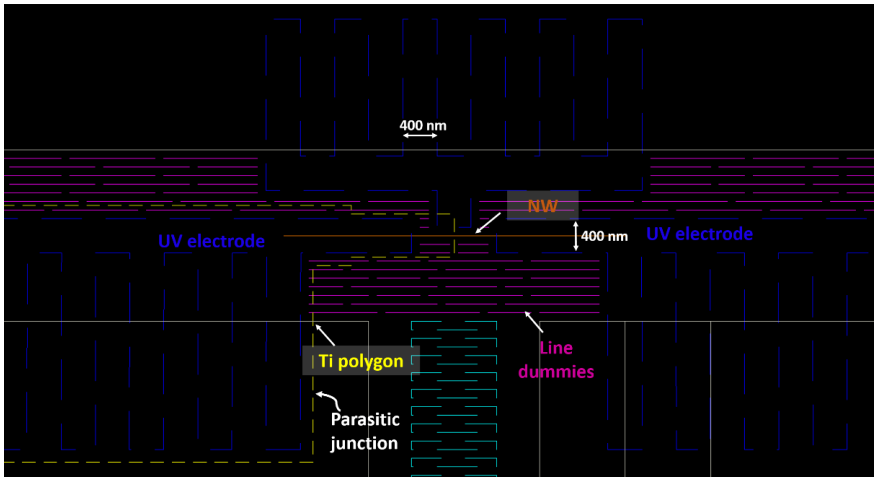

Figure 5.28 EBL1 and EBL2 layouts of a MIM device.

Trench filling optimization

Both TEOS plasma etching steps have been modified in order to improve the trench filling with Ti. Initially, UV lithography and EBL patterned structures are etched into the TEOS layer with nearly vertical sidewalls. The plasma etching process yielding 70°-angled sidewalls has been adopted to improve grains growth on the trench sidewall in order to limit the formation of cavities and porosity in the metallic structures. In addition, the deposition rate of the first 30 nm-thick Ti blanket layer has been reduced to about 0.4 nm/min, to allow better adatoms mobility and enhance grains growth on the trench sidewall. The remaining 120 nm-thick Ti layer is deposited at a rate of 1.6 nm/min.

Chemical mechanical planarization results

SEM observations of the same cell of a sample over the last CMP steps are presented in Fig. 5.30. The UV features are 40 nm-deep and all the features are 70°-angled sidewall etched. A 1 nm-thick Al_2O_3 layer has been deposited by ALD as a junction dielectric after lifting-off the Ti line. The Al_2O_3 deposition is followed by an in-situ deposition of 25 nm-thick TiN layer to fill the EBL1 features. A schematic illustration of the corresponding structure is given in Fig. 5.29.

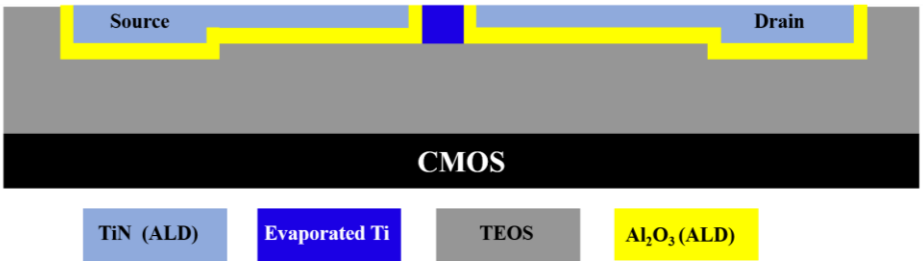

Figure 5.29 Schematic representation of cross-sectional structure of a DG-SET integrated in the TEOS layer on top of a CMOS substrate.

As can be seen in Fig. 5.30, UV and EBL patterned structures are released from the Ti blanket layer at the same time. A homogenous planarization over devices of the same cell as well as over all cells of a sample has been obtained. Similar results have been obtained for four other samples (with different Al_2O_3 junction thickness from 1 to 3 nm). An AFM scan of a DG-SET device of the same sample is shown in Fig. 5.31. Topography variations over the NW trench, line dummies and the TEOS layer are in the few Å range. This is because the CMP removal rates of TEOS and TiN are very close, 60 and 45 nm/min respectively.

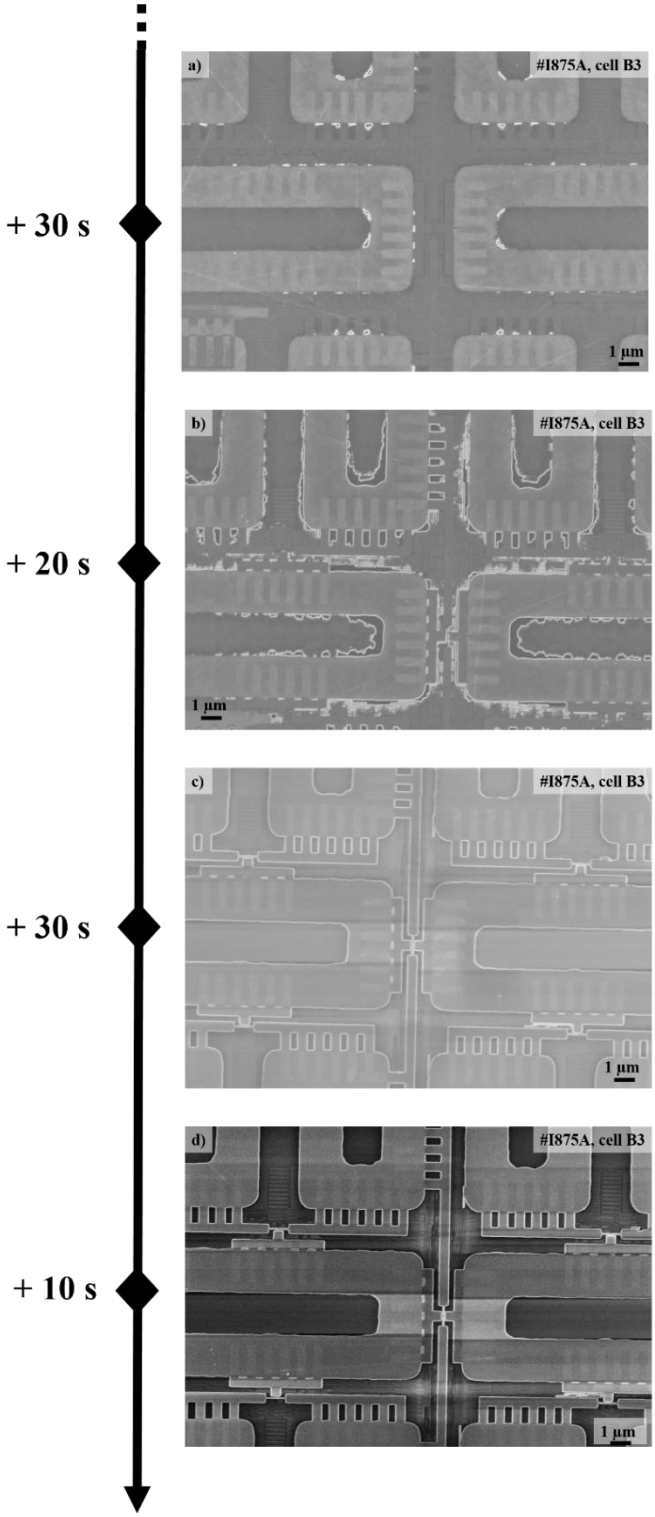

Figure 5.30 SEM images of the same cell of a sample through the CMP process. a) After several CMP iterations. b) After 20 s more of CMP. c) After 30 s more of CMP. d) After 10 s more of CMP.

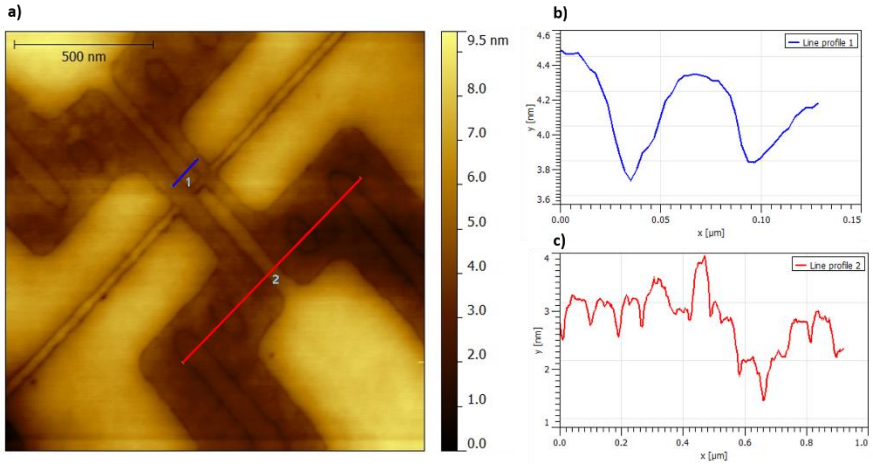

Figure 5.31 AFM scan of a DG-SET obtained after CMP processing showing line profiles extracted in b) and c).

5.3 FD-SOI MOSFET gate functionalization

Front gates of 28 nm FD-SOI MOSFETs have been functionalized with Pt as a sensing layer for H_2 sensing. A functionalization process has been developed. Starting substrates were 28 nm-FD-SOI technology substrates from STmicroelectronics with only the first metal interconnect level implemented. Fig 5.32 illustrates the devices structure. The substrates are top coated with a dielectric layer (passivation layer).

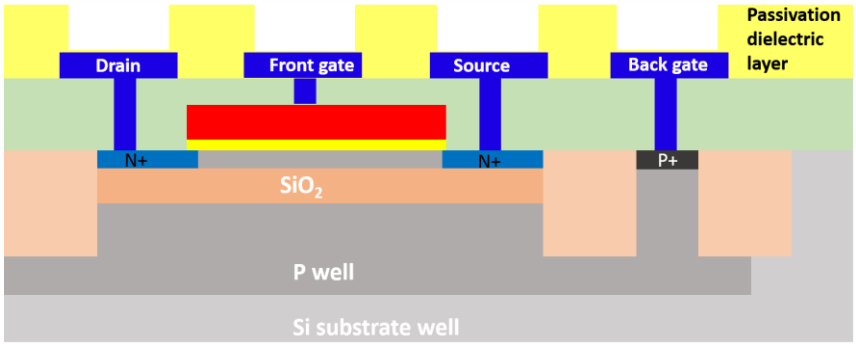

Figure 5.32 Cross sectional schematic of the FD-SOI substrates.

A top view optical image of the FD-SOI substrates is presented in Fig. 5.35 showing Cu contact pads matrix of a CMOS zone. The contact pads (drain, source, front gate and back gate) are exposed (accessible) through already formed 1.1 µm-deep openings in the passivation layer as illustrated by the profilometre trace in Fig. 5.33.c. A Cu contact pad has length and wide of

90 x 60 µm^2.Openings on top of the Cu contacts are smaller than the pads in length and wide and dimensions of 75 x 45 µm^2, as can be seen in Fig. 5.33 and 5.34.

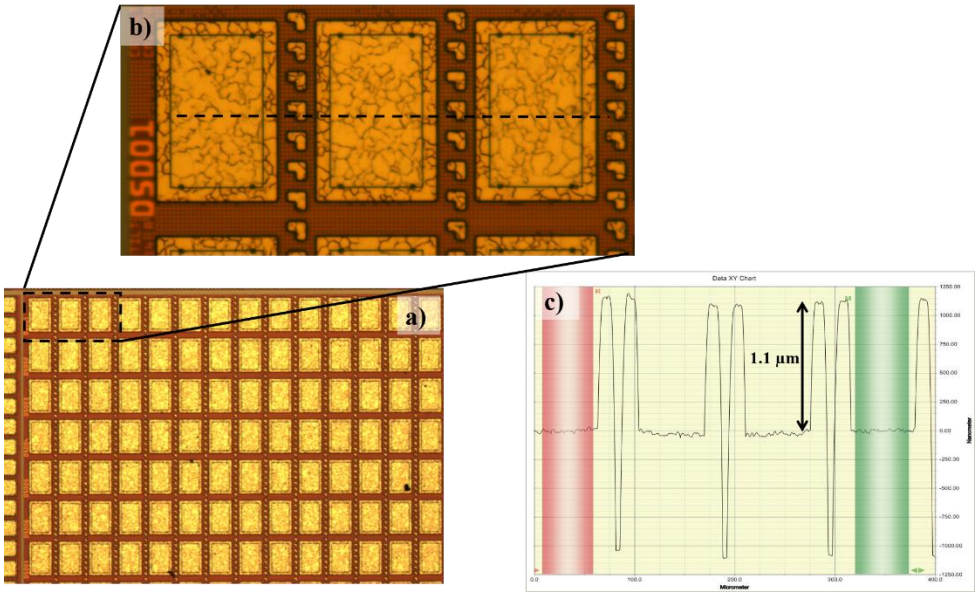

Figure 5.33 FD-SOI technology substrate. a) Optical image of contact pads matrix of a CMOS zone. b) A close-up of few contact pads showing the profilometer trace given in c).

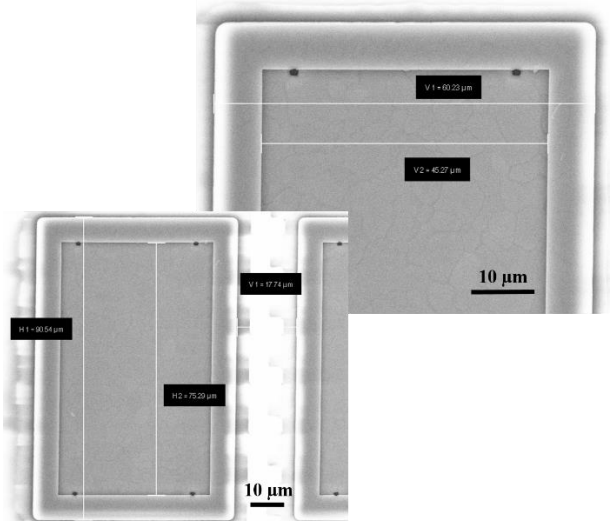

Figure 5.34 SEM image of a Cu contact pad. Right: a close up of the upper part of the contact pad.

We took advantage of already present pads to form the sensing pads (as detailed in section 3.3 and 4.1). Transistors are arranged into lines forming an array of devices. Each line has 9 devices with different channel width and length. The corresponding contact pads are similarly arranged

into any array, as shown in Fig. 5.33 and Fig. 5.35. The back gate contact, referred to as the well, is a common contact to all the 9 devices of a line.

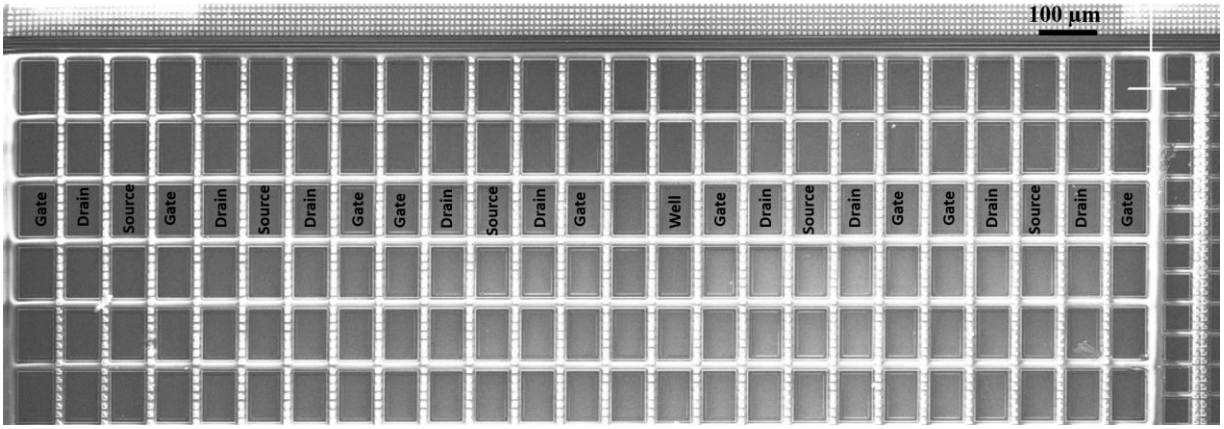

Figure 5.35 SEM image of a contact pads array of a CMOS zone.

Figure 5.36 gives an overview of the functionalization process. The Pt layer on top of the front gate pad is patterned by a UV lift-off process using a bilayer resist of LOR5A/S1805. The LOR5A, lift-off resist, is spun first at 1000 rpm for 5 min and baked at 150 °C for 5 min on a hotplate to yield nearly 1 µm-thick layer. The thick LOR5A layer helped filling the openings and reducing the topography variations due the already formed openings in the passivation layer. Then, S1805, a positive UV resist, is spun at 5000 rpm for 30 s and baked 115 °C for 60 s on a hotplate. The S1805 resist is exposed using a UV mask to define the openings on front gates pads. A UV mask has been designed. The UV lithography is aligned on CMOS structures. The UV lithography layout is designed to deposit Pt over the whole exposed surface of the front gate Cu pad (75 x 45 μm^2). After puddle development of the bilayer resist in AZ MIF319 (2 x 30 s), the sample is dipped in a copper oxide remover solution (PBS-172) for 5 min at ambient temperature and rinsed in deionized water for 15 s. Subsequently, a 50 nm-thick Pt layer as a sensing layer, is deposited by e-beam evaporation at a rate of 0.5 nm/s and followed by a lift-off process. A 5 nm-thick Ti layer is evaporated before in-situ as an adhesion layer. The sample is wirebonded to a chip carrier for electrical characterization under controlled atmosphere.

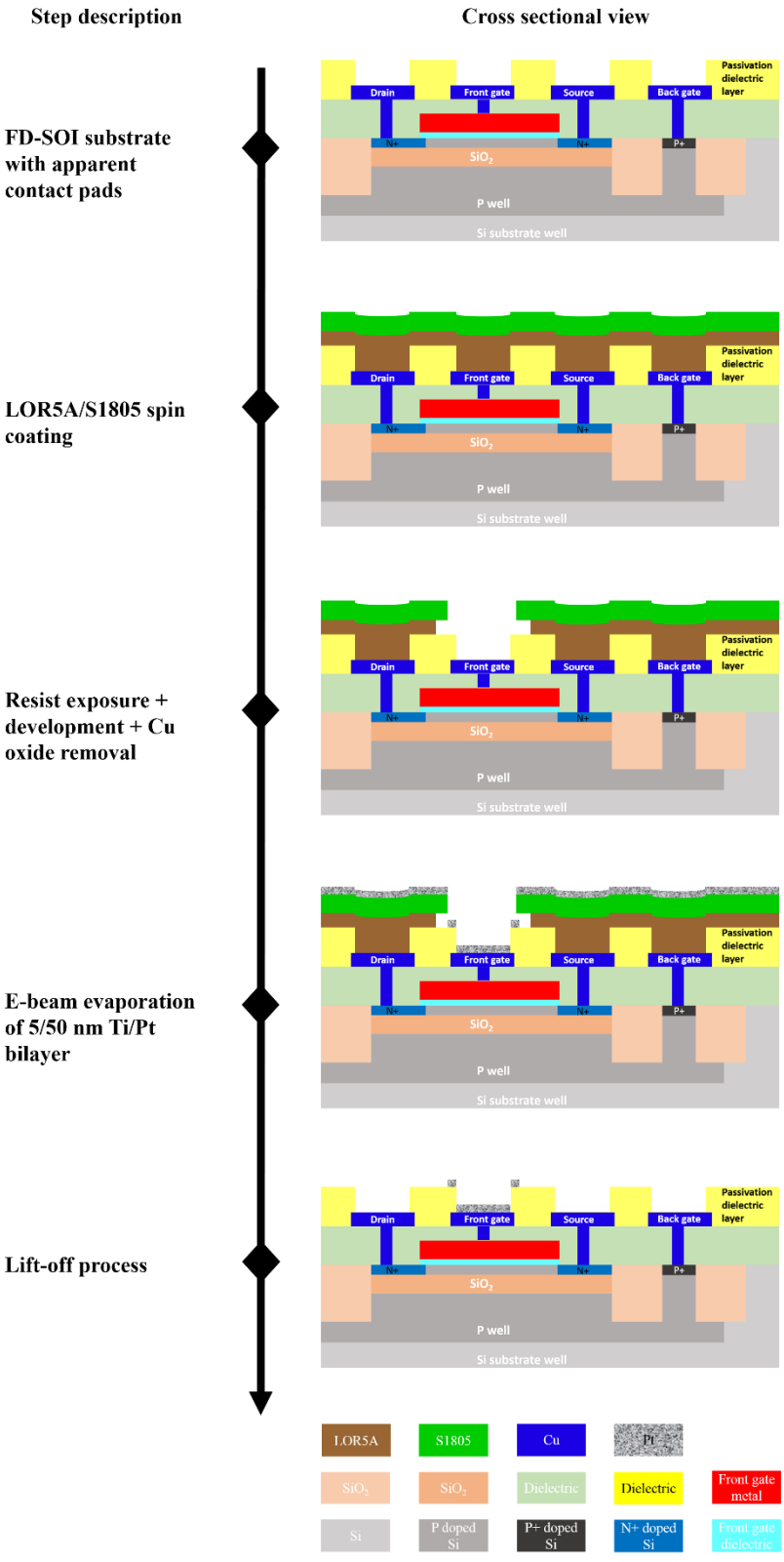

Figure 5.36 Front gate functionalization process flow.

5.4 Nano device electrical characterization

The nanowires placed next to the SETs are characterized in order to estimate the obtained nano devices thickness. The electrical characterization MIM devices placed next to the SETs are carried out in order to extract the tunnelling junction dielectric parameters such as the barrier height, the effective mass, and the thickness. MIM, NW and SET devices with the old UV and EBL layouts have been fabricated and characterized.

A typical NW I-V, obtained by four-point probe measurement technique is shown in Fig. 5.38. It corresponds to a Ti 20 nm-wide NW with structure presented in Fig. 5.37. The resistance is extracted from the NW linear I-V curve, and used the estimated the Ti NW resistivity by subtracting the UV and EBL patterned leads resistance. The NW thickness is extracted using an abacus representing the titanium resistivity as a function of its thickness. The method developed by Guilmain *et al.* to control the thickness of metallic lines fabricated by the *nanodamascene* process in the nanometre range [111]. The NW resistivity measurement is then used as an end-point detection technique for planarization.

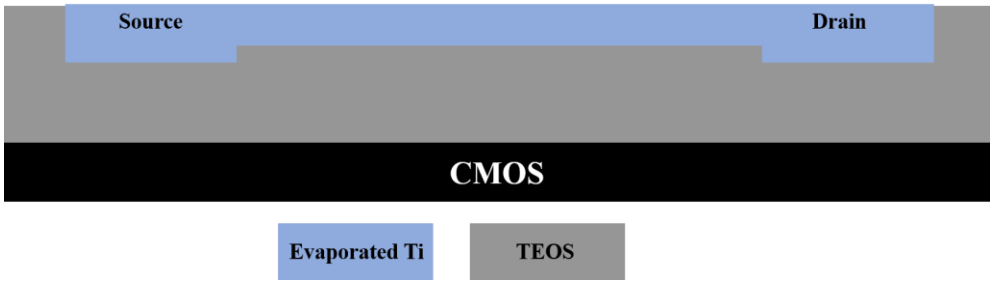

Figure 5.37 Schematic representation of cross-sectional structure of a Ti NW integrated in the TEOS layer on top of a CMOS substrate.

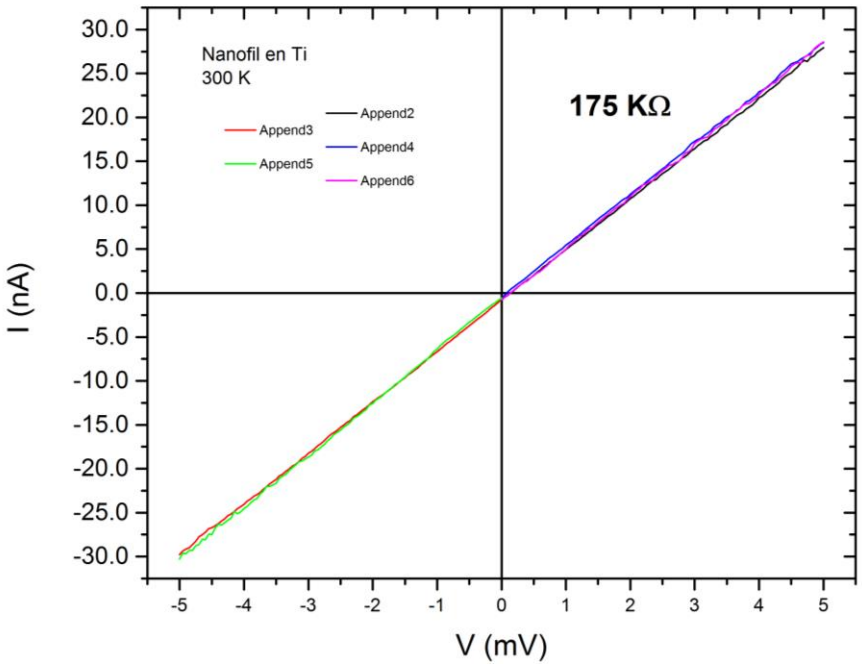

Figure 5.38 Typical 20 nm-wide NW I-V curve at 300 K.

Typical MIM I-V characteristics of a device, illustrated in Fig. 5.39, with a tunnelling material of 4 nm-thick plasma grown TiO_x (measured by ellipsometry) is presented in Fig. 5.40. Knowing the junction dimensions (width, height and tunnelling junction dielectric thickness), the effective mass, the dielectric constant and the barrier height are extracted by fitting the I-V curve to a MIM junction current model, developed by Droulers *et al.*[112]. The current model takes into consideration the conduction mechanism of the thermionic emission conduction, the direct tunnelling and the Fowler-Nordheim emission. The model accounts for the potential barrier deformation by the image force.

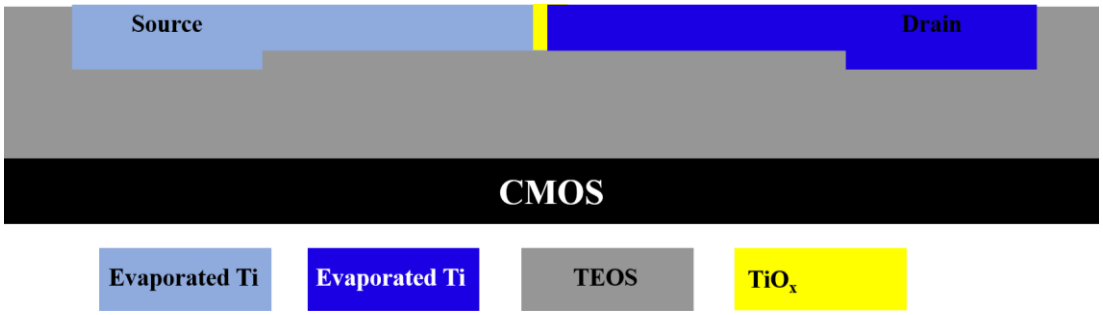

Figure 5.39 Schematic of cross-sectional structure of a MIM nano device with TiO_x as a tunnelling dielectric integrated in the TEOS layer on top of a CMOS substrate.

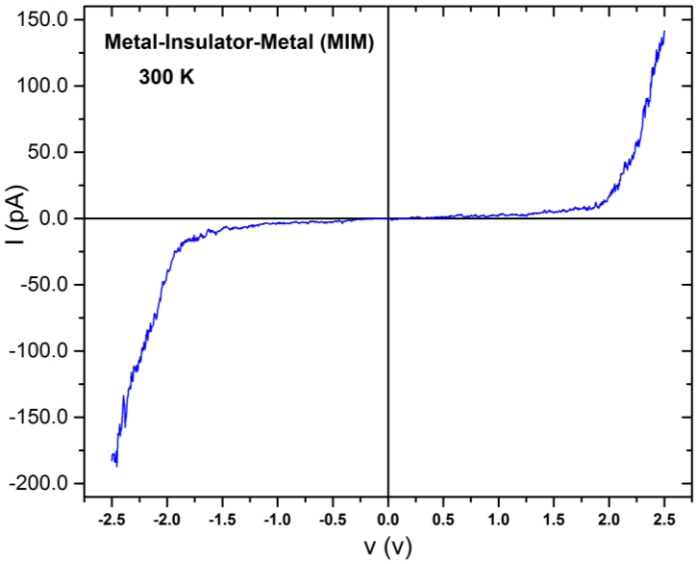

Figure 5.40 Typical MIM $I-V$ curve at 300 K.

About 40 SET devices over 5 samples with the old non-optimized UV lithography and EBL layouts have been fabricated and electrically characterized. 20% of the devices exhibited a Coulomb blockade behaviour in the I_{ds} $versus$ V_{ds} curves, as can be seen in Fig. 5.41. However, at varying V_{gs} no gate control on the transistor conductance has been observed. The rest of the devices were found to be either open circuits or short circuits (see Fig. 5.42), as a consequence of the non-homogenous planarization and overpolishing due to the non-optimized lithography layout.

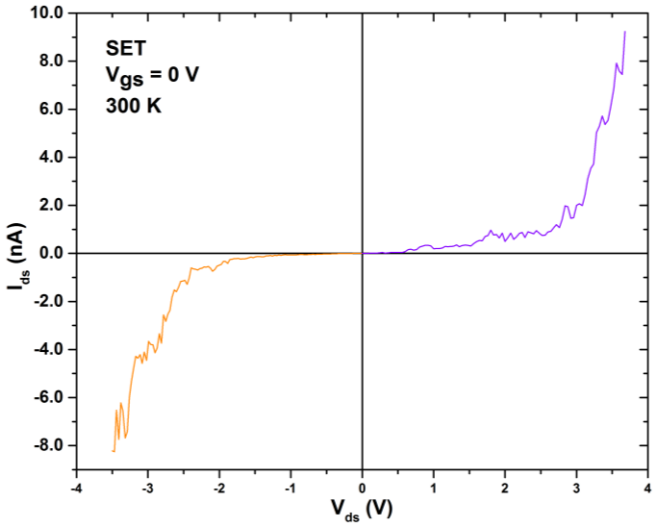

Figure 5.41 SET $I_{ds}-V_{ds}$ curve at $V_{gs}=0$ V and 300 K showing a threshold voltage.

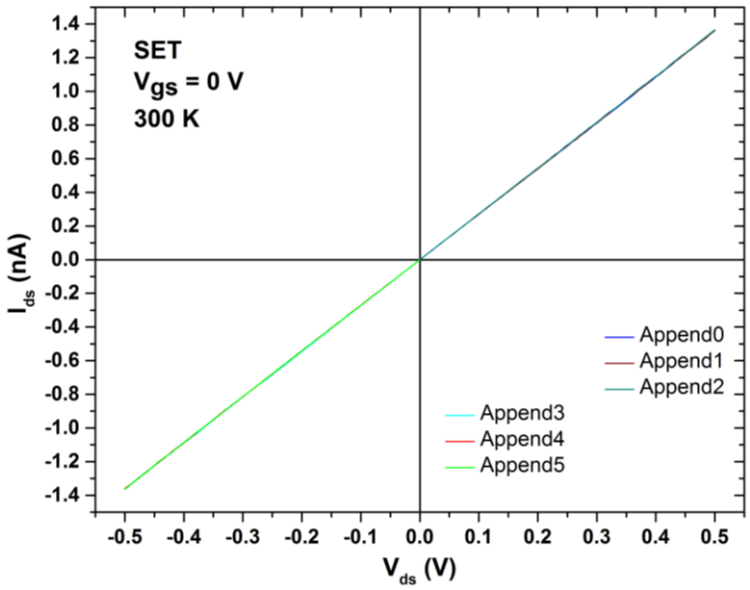

Figure 5.42 SET I_{ds} *versus* V_{ds} curve at $V_{gs} = 0$ V and 300 K showing a resistance behaviour.

Fabricated devices with the optimized lithography layouts, exhibited good results in term of planarization, as discussed in section 5.2.3. However, unfortunately this sample batch was damaged and could not be characterized due to an issue with the passivation layer deposition and contact pad formation.

5.5 Conclusion

The fabrication process has been optimized with regards to the CMP processing as well as the tunneling junction stability. The UV lithography layout, as well as the EBL layout have been optimized in order to improve the CMP processing and achieve a homogenous planarization over the whole sample. The trench filling has been optimized by adopting the angled sidewalls etched structures and reducing the deposition rate of the blanket Ti layer. In order to circumvent the issue of tunnelling junction aging due to oxygen diffusion, Ti has been replaced by TiN (deposited either by ALD or sputtering) for the source and drain electrodes formation.

Achieving a reliable SET fabrication process is challenging because homogenous planarization as well as material properties have to be taken into consideration. Stable materials without diffusion are highly needed especially to obtain stable junctions. CMP processing is strongly dependent on not only present structures but also on all the present different materials. This may

need tremendous efforts because planarization of a material may strongly depend on whether it is nanostructured or not and also on all the neighbouring materials.

In order to achieve a thickness controlled- CMP processing, the use of a stop layer, such as Si_3N_4, is desirable. It allows the control of the yielded embedded structures. In order to comply with industrial IC fabrication processes, the EBL patterning can by replaced by the immersion UV lithography tool combined with the double or quadruple patterning technique. This would also lead to reducing of the alignment error down to few nanometres and thus reducing the gate box width. In consequence, the contribution of the side gate to the island total capacitance (side gate capacitance and parasitic capacitances) can be reduced. Moreover, in term of design, the both side gates can be replaced by a bottom and a top gate, in order to achieve more freedom in gate-to-island distance sizing.

Integration of SETs operating at room temperature or above is the most important milestone toward integration of SET-based gas sensors. Meanwhile, FD-SOI technology offers a very attractive platform for integration of DG-FET-based gas sensors with a high integration density compared to actual technology.

CHAPTER 6 Conclusions and perspectives

6.1 Summary and conclusions

The DG-transistor-based gas sensor is a novel approach in the field of FET gas sensing. Thanks to the dual control of the transistor conductance by two independent gates, an air gap structure or permeable gate electrode made of a catalytic metal is no longer needed. The transistor operation point is set by the control gate. The functionalized gate is “chemically biased” and allows the capacitively coupling of the surface charge to the transistor channel yielding fluctuations around the operation point. These fluctuations are used to monitor the target gas concentration. Both of the DG-SET or DG-FET devices as a gas sensor have been modelled and simulated.

DC stationary simulations of a DG-SET compact model using a Monte Carlo simulator have been carried out. Model parameters are extracted from capacitance calculations by finite elements simulations of a *nanodamascene* metallic SET with the functionalized gate implemented as a top gate. Both of the transducer sensitivity and power consumption have been estimated.

The effective total island capacitance (including all the parasitic capacitances) was found as the dominating limiting factor in the design of functionalized gate, because of its strong impact on operating temperature and the quality of Coulomb peaks. Lowering the functionalized gate capacitance and the all the engendered parasitic capacitances, at the expense of the sensitivity, is desirable as much as possible. The design of the functionalized gate has to be done in order to minimize as much as possible the engendered increase in the effective total island capacitance.

The extensive and reliable available analytical models for UTBB FD-SOI FETs have been combined and modified to allow the simulation of the drain-source current with respect to the front gate charge. Simulation of a device with characteristics of an n-type FD-SOI MOSFET with a back plane issued from 28 nm FD-SOI CMOS technology has been carried out in order to estimate the sensitivity as well as the power consumption.

Extracted sensitivity for a DG-SET-based gas sensor and a DG-FET-based gas sensor ($L = 30$ nm and $W = 0.5$ µm, $V_{ds} = 0.1$ V) are 900 pA/aC and 1.8 µA/aC respectively. Extracted sensitivity and power consumption for a DG-SET-based gas sensor with optimized top gate geometry parameters are 900 pC/aC and 86 pW respectively. In term of sensitivity, the DG-FET was found superior to the DG SET by 3 orders of magnitude. However, in term of power consumption, the DG-SET is 4 orders of magnitude less energy consuming thanks to its ultra-low driving current based on the transport of reduced number of charges. The DG-SET was disabled in term of sensitivity because of the top gate-to-island distance trade-off made to allow RT operation at the expense of the top gate-to-island capacitive coupling. The DG-FET power consumption is found below the lowest values reported in literature for SG-FETs and Lundström MOSFETs (few tens of µW), and thus very relevant to ultra-low power gas sensing applications especially battery powered mobile systems. The device channel width and length have to be tuned with regard to the desired sensitivity, sensitivity range (excursion window) and current levels (power consumption).

A novel technique of material sensitivity investigation, based on measurement of the surface charge variation induced by gas species adsorption, has been proposed and implemented. Sensitivity investigation by surface charge measurement can be applied to any type of sensing material where chemisorption or physisorption induce a surface charge variation. Platinum sensitivity to hydrogen diluted in synthetic air (80% N_2 and 20% O_2) has been investigated by the surface charge measurement technique over the temperature range of RT to 190 °C. Two types of response to H_2 injection have been observed for a 50 nm-thick Pt film: a positive variation in surface charge due hydrogen adsorption at the outer surface at temperature below 80 °C, and thus a decrease in the Pt potential, and a negative variation in surface charge due to hydrogen adsorption at the Pt/Ti or Pt/TiO_2 interface at temperature above 80 °C. Pt charge variation dependence on H_2 concentration has been studied for both regimes. Extensive investigation of H adsorption at Pt/Ti or Pt/TiO_2 interface is needed. The experimental data for temperature below 80 °C are in good agreement with literature and relevant to Pt integration with a DG-FET.

Extracted sensitivity from experimental data has been used for sensing layer sizing with regards to the transducer transfer function and target concentration range.

The estimated Pt sensitivity to H_2 at 60 °C has been used for sizing the needed sensing area for integration with both of the DG-SET and DG-FET based H_2 sensors. The Pt sensing pad has been sized in order to ensure hydrogen detection at the concentration ranging from 0 to 4%. The sensor response to different H_2 concentrations has been simulated and the sensor sensitivity is extracted. The Pt layer needed for integration with a DG-SET or a DG-FET (UTBB FD-SOI MOSFET), for H_2 detection in the 0–4%range was estimated to be 0.36 and 60 μm^2. The sensing layer heating accounts for almost the whole gas sensor power consumption.

The high sensitivity of studied DG-FET or DG-SET has allowed downscaling of the needed sensing surface and thus reducing the heating energy cost. Moreover, the high sensitivity may lead to pushing down of the temperature. The "chemical signal" yielded by either chemisorption or physisorption at low temperature is very low to be detected by conventional transducers, but, thanks to the amplification capability of FD-SOI MOSFETs when operated in sub-threshold regime or SETs, it can be transformed into a reliable response signal.

Thanks to the amplification capability of UTBB FD-SOI MOSFETs, the estimated H_2 DG-FET sensor sensitivity of 750 mV/%H_2 is largely beyond reported sensitivities for Pt-MOSFETs and Pt-SG-FETs in literature. The high DG-FETs sensitivity is their strongest asset with respect to the FET-based gas sensor technology. Moreover, the estimated transducer power consumption of 12 µW is very relevant to ultra-low power gas sensing applications. A fabrication process for integration of SETs in the BEOL entity of a CMOS chip (within the CMOS interconnect layers) aligned on underlying CMOS structures has been developed. The CMP processing is very critical because it has to be controlled in the nanometre range to obtain few nanometre thin devices. Meanwhile it has been very challenging to achieve such goal, since on top of the sample surface both microstructures and nanostructures are present. In addition several materials may be present also such TEOS, tunnel junction dielectric (Al_2O_3 or TiO_x), sputtered Ti, evaporated Ti, ALD deposited TiN or sputtered TiN. Optimized UV lithography and e-beam lithography, together with the trench filling optimization improved the CMP processing as discussed in Chapter 5. Obtained devices are very promising and electrical characterization are undergoing.

6.2 Perspectives

FD-SOI technology offers a very attractive platform for integration of DG-FET-based gas sensors with a high integration density compared to actual technology. Functionalization of the

front gate of an n-type FD-SOI MOSFET with Pt for H_2 sensing as a demonstration of the DG-transistor-approach is a first step toward detecting various target gas species or biochemical species in a liquid phase.

Integration of SETs with CMOS devices for gas sensing presents valuable advantages: a high integration density, an ultra-low power integrated sensor system and use of CMOS for signal processing and hybrid SET-CMOS circuits for the read-out. Integration of SETs operating at room temperature or above is the most important milestone toward integration of SET-based gas sensors. Achieving devices operating at RT or above is strongly related to dimensions downscaling. The transistor design with regards to device dimensions and capacitances has to be carried out prior to fabrication. The geometrical design has a strong impact on the yielded effective total island capacitance, as discussed in Chapter 3.

However, FD-SOI CMOS technology is an available mature technology, well modelled and largely deployed in ICs. For gas sensing applications, they present the following valuable advantages:

- Advanced FD-SOI FETs are ultra-low power consumption transducers.
- Thanks to their amplification capability when biased in sub-threshold regime, FD-SOI FETs are ultra-sensitive charge detector if operated as a DG-FET-based gas sensor (as seen in Chapters 3 and 4).
- Thanks to their enhanced sensitivity, the sensing temperature and the sensing layer surface can be considerably reduced yielding a considerable reduction in the sensor power consumption
- In term of integration density, advanced FD-SOI technology allows very high integration density.
- FD-SOI FETs allow integration of gas sensors with CMOS circuits, which results into adding innovative sensing applications to CMOS chips.

All of these benefits, make the DG-FET-based gas sensors a strong candidate for future gas sensing applications in terms of sensitivity and power consumption. Ultra-low power DG-FETs sensors, integrated with CMOS circuits is with very high interest for mobile or autonomous electronic systems. This kind of systems, powered by batteries and potentially energy

harvesting, have drastic power consumption requirements. The DG-FET-based gas sensors may find application in wireless or mobile integrated sensor systems, portable consumer electronic devices, ambient intelligence devices and more. For instance, smartphones already incorporate cameras, microphones, accelerometers, gyroscopes, etc. Gas sensors may be the next step in functionalities diversifying.

The high integration density of FD-SOI technology may find application in on chip e-nose systems. Integration of sensors matrix with CMOS logic circuits in the same chip is possible with the FD-SOI FET technology. This may also be relevant to the field of bio-mimic. The On chip e-nose systems are the premise of the artificial olfaction. FD-SOI FET gas sensors may make this evolution faster.

APPENDIX A Simulated FD-SOI MOSFET model

The implemented current model is an analytical compact charge-based valid for lightly doped short channel transistors. The model is functional in all regions of operation with back gate control and takes into consideration the effects of drain induced barrier lowering (DIBL), channel length modulation (CLM), saturation velocity, mobility degradation, quantum confinement, velocity overshoot (VO) and self-heating (SH) effects. The detailed model can be found in [79]. In the following, the model is described.

A.1 UTBB FD-SOI MOSFET model

For an UTBB FD-SOI MOSFET with lightly doped channel and large width, the 2D potential distribution $\varphi(x,y)$ along the channel can be expressed as follows [78]:

$$\varphi(x,y) = A + \frac{1}{e^{\frac{2L}{\lambda(x)}} - 1}\left[(V_{bi} + V_{ds} - A)\left(e^{\frac{L+y}{\lambda(x)}} - e^{\frac{L-y}{\lambda(x)}}\right) + (V_{bi} - A)\left(e^{\frac{2L-y}{\lambda(x)}} - e^{\frac{y}{\lambda(x)}}\right)\right] \quad (.A.1)$$

where V_{bi} is the built in potential across source/drain-channel junctions, V_{ds} is the drain voltage, x and y are Si channel coordinates according to the coordinates system and geometrical definitions presented in Fig. A.1, L is the channel length and $\lambda(x)$ is the natural length at any position x along the channel.

The parameter A has the dimension of an electric potential and is expressed as:

$$A = \alpha(x)\, V'_{gf} + \beta(x)\, V'_{gb} \quad (A.2)$$

where $\alpha(x)$ and $\beta(x)$ are x-dependent parameters expressed as follows:

$$\alpha(x) = \frac{\varepsilon_{Si}\, t_{oxb} + \varepsilon_{ox}\,(t_{Si} - x)}{\varepsilon_{Si}\,(t_{oxf} + t_{oxb}) + \varepsilon_{ox}\, t_{Si}} \quad (A.3.a)$$

$$\beta(x) = \frac{\varepsilon_{Si}\, t_{oxb} + \varepsilon_{ox}\, x}{\varepsilon_{Si}\left(t_{oxf} + t_{oxb}\right) + \varepsilon_{ox}\, t_{Si}} \qquad \text{(A.3.b)}$$

where t_{oxf} and t_{oxb} are respectively the front gate oxide thickness and the back gate oxide thickness, ε_{Si} and ε_{ox} are respectively the dielectric permittivity of silicon and the dielectric permittivity of the oxide, and t_{Si} is the Si body thickness.

V'_{gi} is the gate voltage reduced by the flat band voltage V_{fbi} where the index i denotes either front or back gate. V'_{gf} and V'_{gb} are then expresses as:

$$V'_{gf} = V_{gf} - V_{fbf} \qquad \text{(A.4.a)}$$

$$V'_{gb} = V_{gb} - V_{fbb} \qquad \text{(A.4.b)}$$

where V_{gf} and V_{gb} are respectively the front gate potential and the back gate potential.

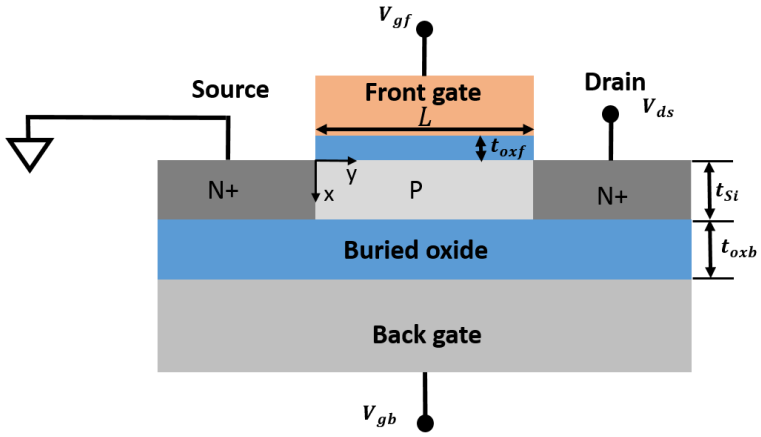

Figure A.1 Cross section schematic representation of simulated UTBB FD-SOI MOSFET structure.

The natural length is a function of the position x along the Si body thickness and is given by [78]:

$$\lambda(x) = \sqrt{\left(\frac{\varepsilon_{Si}\, t_{oxf}\, t_{Si}}{2\varepsilon_{ox}}\right)\left(\frac{2\,\varepsilon_{Si}\, t_{oxb} + \varepsilon_{ox}\, t_{Si}}{\varepsilon_{Si}\left(t_{oxf} + t_{oxb}\right) + \varepsilon_{ox}\, t_{Si}}\left(1 + \frac{\varepsilon_{ox}}{\varepsilon_{Si}\, t_{oxf}}\, x\right) - \frac{\varepsilon_{ox}}{\varepsilon_{Si}\, t_{oxf}\, t_{Si}}\, x^2\right)} \quad \text{(A.5)}$$

The effective conductive path position x_c is back gate bias-dependent and obtained from the empirical relations [79]:

$$\frac{x_c}{t_{si}} = \begin{cases} A_c\, e^{\frac{V_{gb}}{B_c}}, & V_{gb} \leq 0 \\ A_c + 0.04\, V_{gb}, & V_{gb} > 0 \end{cases} \quad \text{(A.6)}$$

where A_c and B_c constants are model parameters.

In UTBB FD-SOI MOSFETs, the threshold V_{thf} voltage is defined quantitatively as the front gate voltage needed to make the minimum carrier charge sheet density Q_{inv} at the effective conductive path reaches an adequate value Q_{thf} to switch on the transistor.

For devices with geometrical parameters within the ranges: $L = 20 - 90\ nm$, $t_{Si} = 10 - 20\ nm$, $t_{oxf} = 1 - 2\ nm$ and $t_{oxb} = 5 - 30\ nm$, Q_{thf} as a function of V_{ds} has been modelled as [78]:

$$Q_{thf} = 7 \times 10^{10}\left(1 + 8\, V_{ds}\, \frac{\lambda_f}{L} + 4\, \frac{t_{oxf}}{t_{oxb}}\right) \quad \text{(A.7)}$$

where λ_f is the natural length of the front gate. λ_f is obtained from Eq. A.5 for $x = x_c$.

The front gate threshold voltage can be expressed in terms of V_{fbf}, V'_{gb} and Q_{thf} in a simple and explicit way as [78]:

$$V_{thf} = V_{fbf} + A_f \frac{K_B T}{e} ln\left(\frac{Q_{thf}\, N_A}{n_i^2\, t_{si}}\right) - B_f \sqrt{\left(V_{bi} - \frac{K_B T}{e}\, ln\left(\frac{Q_{thf}\, N_A}{n_i^2\, t_{si}}\right)\right)\left(V_{bi} + V_{ds} - \frac{K_B T}{e} ln\left(\frac{Q_{thf}\, N_A}{n_i^2\, t_{si}}\right)\right)} - C_f\, (2\, V_{bi} + V_{ds} + \beta_f\, V'_{gb}\left(cosh\left(\frac{L}{\lambda_f}\right) - 1\right) \quad \text{(A.8)}$$

where n_i is the intrinsic carrier concentration of the Si channel, K_B is Boltzmann constant, T is the temperature and A_f, B_f and C_f are parameters given by the following expressions:

$$A_f = 8e^{\frac{2L}{\lambda_f}} \sinh^2\left(\frac{L}{2\lambda_f}\right)\left[1 + \cosh\left(\frac{L}{\lambda_f}\right)\right] \Big/ \alpha_f \left(e^{\frac{L}{\lambda_f}} - 1\right)^4 \quad \text{(A.9.a)}$$

$$B_f = \frac{2e^{\frac{2L}{\lambda_f}}\left(e^{\frac{L}{\lambda_f}} + 1\right)}{\alpha_f \left(e^{\frac{L}{\lambda_f}} - 1\right)^2} \quad \text{(A.9.b)}$$

$$C_f = \frac{8e^{\frac{2L}{\lambda_f}} \sinh^2\left(\frac{L}{2\lambda_f}\right)}{\alpha_f \left(e^{\frac{L}{\lambda_f}} - 1\right)^4} \quad \text{(A.9.c)}$$

α_f and β_f are defined as:

$$\alpha_f = \alpha(x_c) \quad \text{(A.10.a)}$$

$$\beta_f = \beta(x_c) \quad \text{(A.10.b)}$$

We recall that x_c is the distance of the effective conductive path from the front gate interface.

Based on the drift-diffusion transport and integrated from source to drain, the drain current expression in terms of normalized charge at the source and drain is given by [79]:

$$I_{ds} = \frac{W\ \mu_{eff}\ C_{oxf}\ \frac{K_B T}{e}}{L_{eff} + \frac{\mu_{eff}\ \frac{K_B T}{e}}{\upsilon_{sat}}} \left[(q_s - q_d) + \frac{1}{2\eta_f}\ (q_s^2 - q_d^2) \right] \quad (A.11)$$

where, W is the channel width, L_{eff} is the effective length due to the CLM effect, C_{oxf} is the front gate oxide capacitance per unit area, η_f is the front interface ideality factor, μ_{eff} is the effective carrier mobility, and υ_{sat} is the saturation velocity. q_s and q_d are the normalized charge at the source and drain derived the from inversion charge density Q_{inv} expressed by an interpolating function as a single expression valid in both strong and weak inversion as follows [79]:

$$Q_{inv} = \eta_f\ C_{oxf}\ K_B T \ln\left(1 + e^{\frac{V_{gf} - V_{thf} - \eta_f V_y}{\eta_f \frac{K_B T}{e}}}\right) \quad (A.12.a)$$

$$q_{inv} = \frac{Q_{inv}}{C_{oxf}\ \frac{K_B T}{e}} \quad (A.12.b)$$

where V_y is the quasi Fermi level potential in the channel and equals 0 at source and V_{ds} at drain.

The front gate potential V_{gf} is obtained from the front gate charge Q_{gf} by the following equation [113]:

$$Q_{gf} = W C_{oxf} \int_0^L \left(V_{gf} - V_{fbf} - \varphi(0,y)\right) dy \quad (A.13)$$

The front interface ideality factor η_f is estimated from the following expression:

$$n_f = \frac{1}{\alpha_f{}'} \left[1 - K_f \frac{\left(2\ V_{bi} - 2\ A_{fc} + V_{ds}\right) e^{\frac{L}{2\lambda_f'}} \left(e^{\frac{L}{2\lambda_f'}} - 1 \right)}{\left(e^{\frac{L}{2\lambda_f'}} + 1 \right) \left[\left(V_{bi} - A_{fc}\right) \left(e^{\frac{L}{2\lambda_f'}} - 1 \right) - V_{ds} \right]} \right]^{-1} \quad (A.14)$$

where

$$A_{fc} = \alpha'_f \, V_{thf} + \beta'_f \, V'_{gb} \tag{A.15}$$

and

$$K_f = \sqrt{\frac{\left(V_{bi} - A_{fc}\right)\left(e^{\frac{L}{\lambda'_f}} - 1\right) - V_{ds}}{\left(V_{bi} - A_{fc}\right)\left(e^{\frac{L}{\lambda'_f}} - 1\right) + V_{ds}\, e^{\frac{L}{\lambda'_f}}}} \tag{A.16}$$

α'_f, β'_f and λ'_f are calculated from respectively Eq. A.10.a, Eq. A.10.b and Eq. A.5 by replacing the front gate oxide thickness t_{oxf} and the silicon body thickness t_{si} by respectively the equivalent front gate oxide thickness t_{oxf}^{eq} and the equivalent silicon body thickness t_{si}^{eq} defined as a function of the effective path depth x_c as follows:

$$t_{oxf}^{eq} = t_{oxf} + \frac{\varepsilon_{ox}}{\varepsilon_{Si}} x_c \tag{A.17.a}$$

$$t_{si}^{eq} = t_{Si} - \frac{\varepsilon_{ox}}{\varepsilon_{Si}} x_c \tag{A.17.b}$$

where ε_{ox} and ε_{Si} are oxide relative permittivity and silicon relative permittivity respectively.

The effective carrier mobility, as a result of the degradation due to the vertical gate field, is expressed in terms of q_s as [79]:

$$\mu_{eff} = \frac{\mu_\circ}{1 + \theta_1 \frac{K_B T}{e} q_s + \theta_2 (\frac{K_B T}{e} q_s)^2} \tag{A.18}$$

where $\mu_\circ$ is the low field mobility and θ_1 and θ_2 are mobility attenuation factors. The former is correlated to phonon scattering and Coulomb scattering, while the latter is correlated to the surface roughness scattering. To take into account the series resistance R_{sd}, in Eq. A.18 θ_1 has to be substituted by $\theta_{1,R_{sd}}$ expressed as [79]:

$$\theta_{1,R_{sd}} = \theta_1 + {}^{W}/_{L} \, \mu_\circ \, R_{sd} \, C_{oxf} \tag{A.19}$$

The effective length is given by:

$$L_{eff} = L - \Delta L \tag{A.20}$$

where ΔL is the channel length shortening in saturation regime due to the CLM effect, modelled as [79]:

$$\Delta L = \lambda_f \ln\left[1 + \frac{(V_{ds} - V_{dsat} + 0.05)\tanh(V_{ds}/V_{dsat})^3}{V_E}\right] \tag{A.21}$$

where V_{dsat} is the saturation drain voltage and V_E is a fitting parameter. V_{dsat} is approximated as follows [79]:

$$V_{dsat} = \sqrt{\left(\frac{\upsilon_{sat}\, L}{\mu_{eff}}\right)^2 + \frac{2\, q_s \frac{K_B T}{e}\, \upsilon_{sat}\, L}{\mu_{eff}}} - \frac{\upsilon_{sat}\, L}{\mu_{eff}} + \frac{q_s \frac{K_B T}{e}}{\eta_f} - q_s \frac{K_B T}{e} \tag{A.22}$$

Taking into account the velocity overshoot phenomenon in short channel transistor, the saturation velocity is modified a length-dependent factor as follows [79]:

$$\upsilon_{sat,\ VO} = \upsilon_{sat}\left(1 + \frac{2\,\lambda_w}{L}\right) \tag{A.23}$$

where λ_w is the energy relaxation length given by:

$$\lambda_w = 2\,\upsilon_{sat}\,\tau_w \tag{A.24}$$

where $\tau_w$is the energy relaxation time constant.

The built in potential V_{bi} is given by [78]:

$$V_{bi} = \frac{K_B T}{e} ln\left(\frac{N_A\, N_{SD}}{n_i^2}\right) \tag{A.25}$$

where N_A the doping concentration of the silicon channel and N_{SD} is the doping concentration of the source/drain contacts.

The functional dependence of the silicon intrinsic carrier concentration n_i on temperature from 275 to 375 K is modelled by the following polynomial expression [114]:

$$n_i = 9.15 \times 10^{19} \left(\frac{T}{300}\right)^2 e^{\left(-\frac{6880}{T}\right)} \quad \text{(A.26)}$$

The SH effect is taken in account by estimation of the temperature rise given by:

$$T - T_\circ = R_{th} V_{ds} I_{ds\circ} \quad \text{(A.27)}$$

where R_{th} is the thermal resistance given by [79]:

$$R_{th} = \frac{1}{2\,W} \sqrt{\frac{t_{oxb}}{K_{ox}\, K_{Si}\, t_{Si}}} \quad \text{(A.28)}$$

where K_{Si} is the thermal conductivity of silicon. Once T is obtained, V_{thf} and μ_{eff} have to be recalculated to refine the drain current calculation in Eq. A.11.

The decrease of the effective carrier mobility due to the SH effect is approximated in terms of T and μ_{eff} as [79]:

$$\mu_{eff,\ SH} \approx \frac{\mu_{eff}}{1 + \frac{r\, R_{th}\, V_{ds}\, I_{ds}}{T}} \quad \text{(A.29)}$$

where r is the mobility temperature exponent.

A.2 Simulated UTBB FD-SOI MOSFET characteristics

For simulations, presented in section 3.5, we considered a device with characteristics of an n-type FD-SOI MOSFET with back plane issued from 28 nm FD-SOI CMOS technology, fabricated by STMicroelectronics [80]. The simulated device characteristics are listed in table A.1.

For V_{fbf}, V_{fbb}, A_c and B_c, we considered values extracted from experimental data of the above mentioned FD-SOI technology [79]. From experimental data presented in [79], $\mu_\circ$, $\theta_{1,R_{sd}}$ and

θ_2 have been modelled by a polynomial expression as a function of V_{gb} as follows for values ranging in -3 to 3 V:

$$\mu_{\circ} = 0.131\,{V_{gb}}^2 + 0.0357\,V_{gb} + 94.167 \quad \text{(A.30.a)}$$

$$\theta_{1,R_{sd}} = 0.0154\,{V_{gb}}^2 - 0.0511\,V_{gb} + 0.42 \quad \text{(A.30.b)}$$

$$\theta_2 = -0.0432\,V_{gb} + 0.5371 \quad \text{(A.30.c)}$$

Hereon the model constant parameters can be found in table A.2.

Table A.1 Simulated device characteristics.

Model parameter	**Value**	**Units**
N_A	10^{15}	cm^{-3}
N_{SD}	10^{20}	cm^{-3}
t_{Si}	7	nm
t_{oxb}	25	nm
t_{oxf}	1.55	nm
V_{fbf}	-0.37	V
V_{fbb}	-0.17	V
A_c	0.2	
B_c	3.1	

Table A.2 Simulated model constant parameters.

Model constant parameter	**Value**	**Units**
K_B	1,38064852 10^{-23}	J/K
ε_{Si}	1,03416913 10^{-10}	F/m
ε_{ox}	3,45313325 10^{-11}	F/m
K_{Si}	1,4	W/m K
K_{ox}	63	
$\mu_{\circ}$	≈ 93,5	$cm^2/(V\ s)$
υ_{sat}	≈ 2 10^7	cm/s
V_E	0,5	
r	0,5	

APPENDIX B Surface charge measurement technique

The surface charge measurement is carried out with an electrometer with feedback amplifier configuration, in Coulombs mode. In the following,

B.1 Measurement instrument

An electrometer is capable of making charge measurements. The coulombmeter function allows to measure electrical charge that has been stored in a capacitor or that might be produced by some charge generating process such as net surface charge generated by molecules adsorption on a material surface. It has special input characteristics and high sensitivity that allow it to perform current, resistance and charge measurements far beyond the capabilities of a conventional DMM. Electrometer designed for low level measurements usually use circuits based amplifier configurations [30].

An electrometer with coulombmeter function uses a reference capacitor to which the charge to be measured is transferred. Electrometers may have either shunt or feedback amplifier configuration, as shown in Fig B.1.a and B.1.b. In the former, the reference capacitor C_F is used in a shunt mode; and in the latter, it provides the feedback around the operational amplifier. The output voltage of the amplifier gives a measure of the charge. In the shunt arrangement, output voltage is given by the following expression:

$$V_{output} = \frac{R_1 + R_2}{R_2} \frac{Q}{C_S + C_F} \quad \text{(B.1)}$$

where C_S is the source capacitance and Q is the charge to be measured. Note that in the shunt configuration, the dependence of the measurement on C_S, which needs to be known for accurate measurement. Increasing the reference capacitance to a point where it should dominate total capacitance comes with reducing the output voltage and the measurement becomes more difficult. The dependence of the shunt configuration on C_S is one of the main limitation of this mode. Indeed, any leakage current into the input of the operational amplifier through the reference capacitance will be integrated within the measurement.

For accurate charge measurement of low charge levels, feedback amplifier configuration is commonly used. In this mode, the input capacitance is equivalent to $A.C_F$, where A is open loop gain of the operational amplifier. In the feedback configuration, the output voltage is given by the following expression:

$$V_{output} = \frac{A.Q}{C_S + A.C_F} \quad \text{(B.2)}$$

where C_S is the source capacitance and Q is the charge to be measured. The gain A of the amplifier is very large, a minimum of 10^4 to 10^5 and often 10^6 [30], making the coulombmeter input capacitance $A.C_F$ very large compared to source capacitance C_S. Thus the charge to be measured is completely transferred the input capacitance of the coulombmeter and the charge measurement is independent of source capacitance.

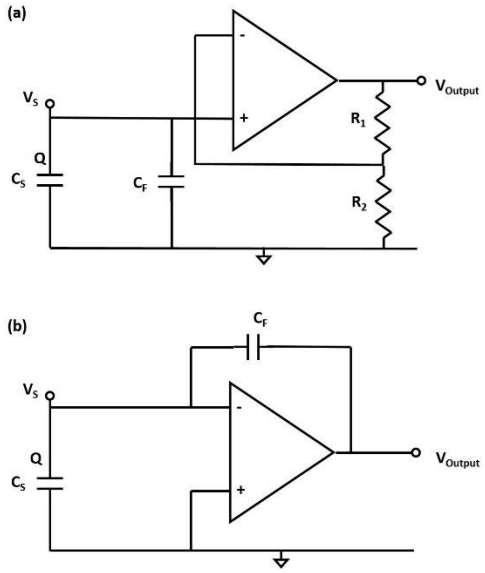

Figure B.1 Circuit diagrams of both coulombmeter configurations. a) Shunt amplifier configuration. b) Feedback amplifier configuration. In both circuits, C_F and C_S are respectively the reference capacitance and source capacitance, V_S is the potential associated to the charge to be measured.

Surface charge measurements have been performed using a Keithley model 6514 electrometer. This model is a digital electrometer with amplifier feedback configuration. Fig. B.2 shows the block diagram of a typical digital electrometer. The coulombmeter function of the electrometer measures charge by integrating the input current. An integrating capacitor is placed in the feedback loop of the input stage.

An electrometer preamplifier is used at the input to increase sensitivity and raise input resistance [30]. It is capable of charge measurement from 10 fC to 2.1 μC, with resolution and accuracy down to respectively 10 fC and 0.4%, with the lowest range (20 nC). Complete instrument specification can be found in [115].

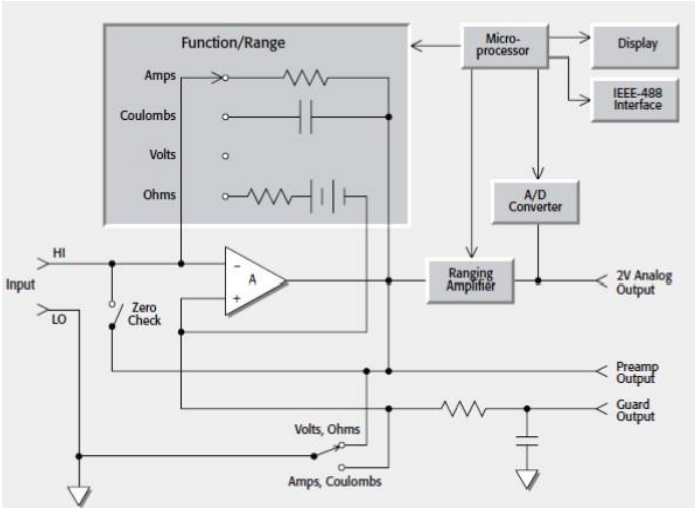

Figure B.2 Block diagram of a typical digital electrometer with feedback amplifier configuration (for ammeter and coulombmeter functions) [30].

Some considerations for making proper and accurate charge measurement have to be taken into account. First, the integrating amplifier has an input current bias, which is integrated along with the input signal. Over long measurement period, integrated offset current will lead to a long-term drift in the charge reading. Keithley 6514 has a typical input current bias of 4 fA for Coulombs function at 20 °C. This input offset translates into a charge offset of 4 fC per second at 20 °C [116]. This value must be subtracted from the final reading to obtain the correct value.

Another consideration is to properly reset the integrating amplifier by enabling the "Zero check" feature. When the "Zero check" is enabled, the input amplifier is configured to shunt through a 10 MΩ resistor, as shown in Fig. B.2. Charge stored in the reference capacitor is then dissipated and the charge reading is reset to zero. Therefore the sample is disconnected from the electrometer input before enabling the "zero check" feature, otherwise stored charge in the sample will dissipate through the "zero check" impedance (10 MΩ). Then the zero check feature is disabled before connecting the sample to electrometer input. Switching off the zero check feature produces a sudden change in charge reading known as "zero check hop". To eliminate this reading offset, a charge reading has to be done just after disabling the zero check and

subtract this reading from all subsequent reading. The "relative" feature, if enabled immediately after disabling the zero check feature, nulls out the charge reading caused by hop in charge.

The voltage burden is the voltage drop caused by adding of instrument input stage resistance to the test circuit load. The voltage burden of an amplifier feedback electrometer in Coulombs mode is generally lower than 100 μV [30]. If the source voltage is at least 10mV, the typical electrometer in Coulombs mode will integrate the current accurately. If the source voltage is much lower, the voltage burden may become a problem, and the input stage noise will be amplified so much that making accurate charge readings becomes problematic.

In coulombmeter, the noise gain depends on the feedback impedance as well as the source impedance. The feedback impedance in a coulombmeter is the reference capacitor. The output noise as a function of the input noise is given by the following equation:

$$Output\ noise = input\ noise\ (1 + \frac{Z_F}{Z_S}) \tag{B.3}$$

B.2 Experimental set-up

The gas mixture feeding system is composed of three analogue mass flow controllers (MFCs), different gas deliveries (ex. N_2, O_2, CO, H_2, etc.), a MFCs interface (MKS model 247D) and appropriate pipes and fittings. The three MFCs are Tylan model FC260 with 3 different maximum flow rate capability of 10, 200 and 1000 sccm (square centimetre square per minute). The used MFC model has analogue command signal (MFC flow rate input signal) and output signal (MFC feedback signal) within the range 0–5 VDC for full scale, and a proportional-integral-derivative (PID) regulator integrated within its electronics. The MFC interface provides the power supply (±15VDC), command signal (MFC flow input signal), and receives the output signal (MFC feedback signal) for each MFC. The MFCs interface unit is connected to MFCs by appropriate interface cables and connectors (DB15 type connectors). The interface unit can be operated manually via the front panel controls or through remote control (external control). In our experimental set-up, we used the remote control mode of the 247 unit.

Communication to and from the 247 unit occurs through an external control interface connector (DB 25 connector). Remote control is accomplished by applying set-point signals and flow ON/OFF signals to the interface connector in the form of respectively analogue DC voltage and

TTL (transistor-transistor logic) logic signal. The desired flow rate is determined by the magnitude of the set point signal with +5 V corresponding to full scale flow rate. Returned MFC feedback signal is also transferred by the 247 unit via the external control interface connector. A computer with a LabView program and National Instrument (NI) multifunction data acquisition (DAQ) hardware are used for gas feeding system control and data acquisition. The NI model USB-6009 hardware is used to generate the appropriate set-point signals (247 unit set-point input) and flow ON/OFF signals (247 unit flow ON/OFF input) and acquire the output flow signal. The NI hardware has analogue input and output lines with respectively 14-bits and 12-bits resolution, and software or external triggering. It has digital input/output lines with TTL logic level compatibility. The NI model USB-6009, is connected to the computer via USB bus, which also provide the power supply. The USB-6009 is digitally triggered. Then, due to the USB bus speed, sampling period below 500 ms was problematic. For measurement acquisition and the electrometer control, GPIB (General Purpose Interface Bus) communication bus, SCPI (Standard Commands for Programmable Instruments) language and the LabView program were used. The LabView program ensures to properly configure the electrometer, generate adequate signals for MFCs control, acquisition and “real time” display of charge measurement signal and all the MFC feedback signals.

The triboelectric effect should be taken into account. It can be seen as the static charge imbalance created between the conductor and the insulation jacket of due to friction caused by cable movement. A low noise-type triax cable (Keithley Model 7078-TRX triax cable) was used, which minimizes the unwanted triboelectric effects. Triax cable centre conductor, inner shell conductor and outer shield conductor are respectively high input, low input and chassis-ground of the electrometer input.

APPENDIX C Sensing material characterization by work function measurements

The material sensitivity is given in term of work function variation induced by gas species adsorption. The work function is the energy difference between the vacuum level and the Fermi level [94] and can be seen as the least amount of energy needed to withdraw an electron from a material surface atom to the vacuum level'. Kelvin probe (KP) has been the preferred technique for the investigation of sensing material deployed in FET-based gas sensors by measuring the work function variation induced by target gas species adsorption. KP belongs to scanning probe microscopy techniques.

C.1 Kelvin probe measurement principle

The Fermi levels of two conducting materials (a metal or a semiconductor) in separated systems align at the vacuum level at energies corresponding to the respective work functions Φ_1 and Φ_2. This is illustrated in energy band diagram of two metallic materials show in Fig. C.1.a. If they are electrically connected, for example by an external conducting wire, electrons will flow from the material with the smallest work functions to the material with the larger work function till a thermal equilibrium is established as a single system (Fermi levels alignment), as illustrated in Fig. C.1.b for two conducting materials. This charge leads to the former and the latter to charge respectively positively and negatively. The two surfaces become equally and oppositely charged. The charge is built up at the surface or within the charge space zone whether the material is a metal or a semiconductor respectively. A surface potential difference gradient associated with an electric field is established between surfaces of both materials to compensate for work functions difference. This potential difference associated with the electric field is called contact potential difference (CPD) and equals the work function difference:

$$CPD = \Phi_1 - \Phi_2 \qquad (C.1)$$

At equilibrium, the Fermi level in the material with the smaller work function is lowered by an amount equal the difference between the two work functions, as can be seen in Fig. C.1.b where the two materials are metallic.

If a sweeping counter voltage V_c is applied between both materials, as illustrated in Fig. C.1.c, and current flow is recorded, the zero charge flow point can be determined. The counter voltage corresponding to this state of zero charge flow point is exactly –CPD.

In KP, one of the materials is the sample, and the other one is the probe tip, and a counter voltage is applied between them. The tip is vibrating in a close proximity to sample surface at a certain frequency. Generated oscillating current is monitored. Gradual sweeping of the counter voltage and finding zero AC current allows to determine CPD. Since small currents are difficult to detect, usually a current *versus* counter voltage curve is measured and the null current point is found through a curve fit. Since the CPD equals the work function difference, the tip has to be made of a material with very well-known absolute work function value so the work function of the sample can be deduced. Usually the tip is gold made. KP measurements are very reliable under vacuum conditions.

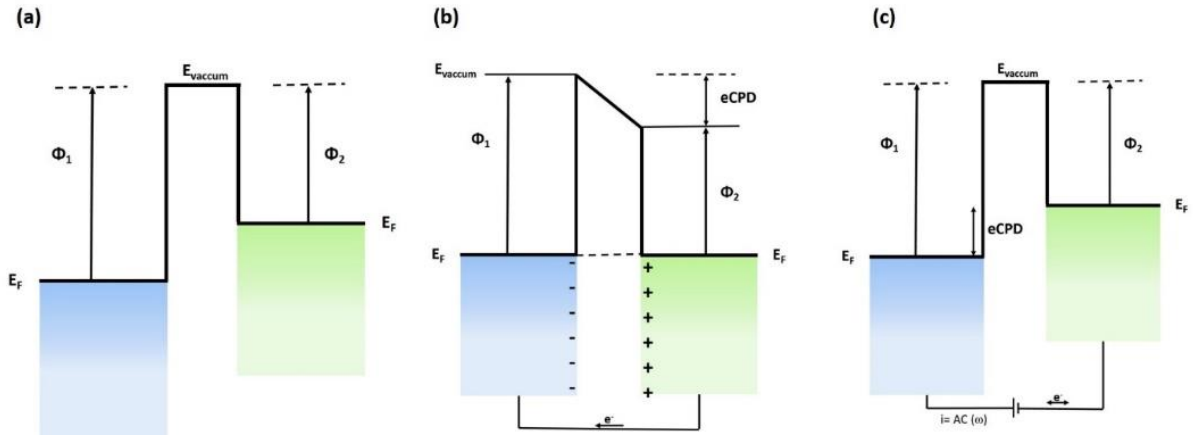

Figure C.1 Energy band diagram of two metallic materials (a) in separated systems, (b) connected into one system, (c) with a voltage biasing V_c. Φ_2 and Φ_2 denote work function of respectively material 1 and material 2, E_F and E_{vacuum} denote respectively Fermi and vacuum energy levels and CPD stands for contact potential difference.

C.2 Sensing material work function change measurements

For a first evaluation, work function measurements carried out by means of KP under controlled gas atmosphere have been widely used. Scharnagl *et al.* [24] applied KP to investigate work function change of a 100 nm-thick layer of Pt due to H_2 adsorption. The work function change response (Kelvin probe signal) to exposure to 1% H_2 in dry air or with 30% RH at 30 °C is

shown in Fig. C.2.a. Fig. C.2.b shows work function response recorded over time, to different H_2 concentrations in dry air at 30 °C.

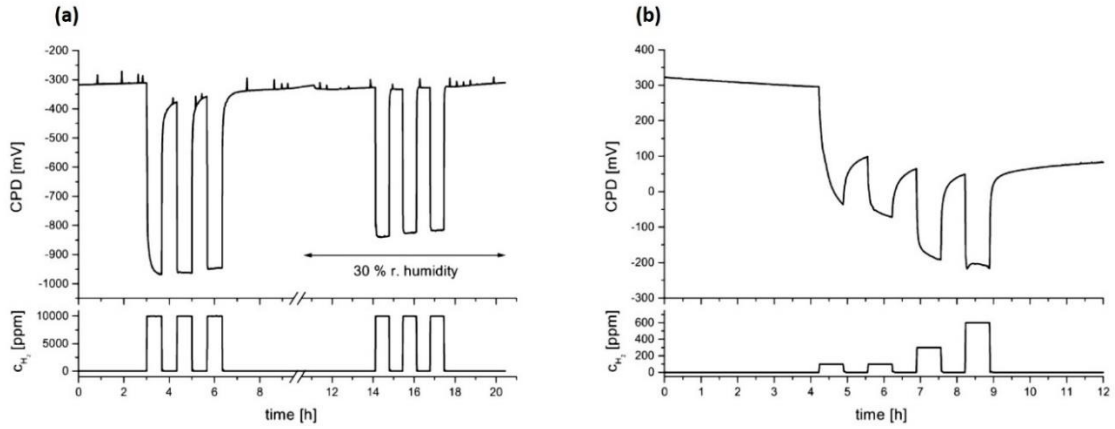

Figure C.2 Kelvin probe signal of a 100 nm-thick layer of Pt for a) 1% H_2 in dry air (left) and with 30% RH (right) at 30 °C; b) for 100, 300, 600 ppm H_2 at 0% RH and 30 °C. Reproduced from [24].

Ostrick *et al.* [31] have used Kelvin probe method to investigate sensitivity and stability of TiN as a sensitive material for ammonia sensing in work function type sensors as well as the dependence of the sensitivity on RH. KP output signal *versus* NH_3 concentration curves, for sputtered TiN, screen printed TiN and screen printed TiO_2 layers are shown in Fig. C.3.a. Fig. C.3.b shows a comparison between the 3 different materials in term of RH impact on the sensitivity (as work function change per NH_3 concentration decade).

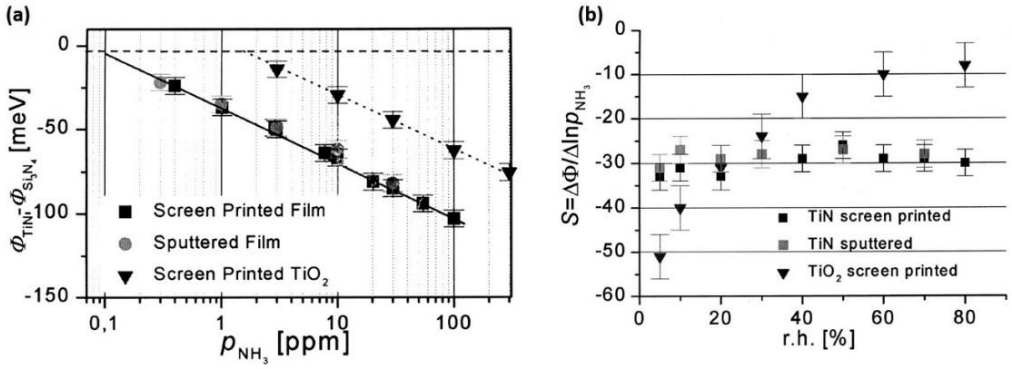

Figure C.3 a) Kelvin probe signal at varying concentration of ammonia for sputtered TiN, screen printed TiN and screen printed TiO_2 at 23 °C and 40% RH. Si_3N_4 was used as a reference material since its work function is not altered by ammonia gas molecules. b) Sensitivity, as work function changes per NH_3 concentration decade, at RT, at different RH between 0% and 80%, for sputtered TiN, screen printed TiN and screen printed TiO_2. Reproduced from [31].

Using KP, Karthigeyan *et al.* [32] have investigated the sensitivity of 20 nm-thick Ir oxide layers to gases such as CO, SO_2, NO_2, Cl_2 and H_2 under dry and humid conditions at RT. Ir oxide has been found selectively sensitive to ammonia with negligible cross response to other investigated gages. Kelvin probe signal (CPD), in Fig. C.4.a shows no response of Ir oxide layer to exposure of 2000 ppm H_2. Such a layer exhibits reversible response to NH_3, as can be seen in Fig. C.4.b, due to work function change of the film.

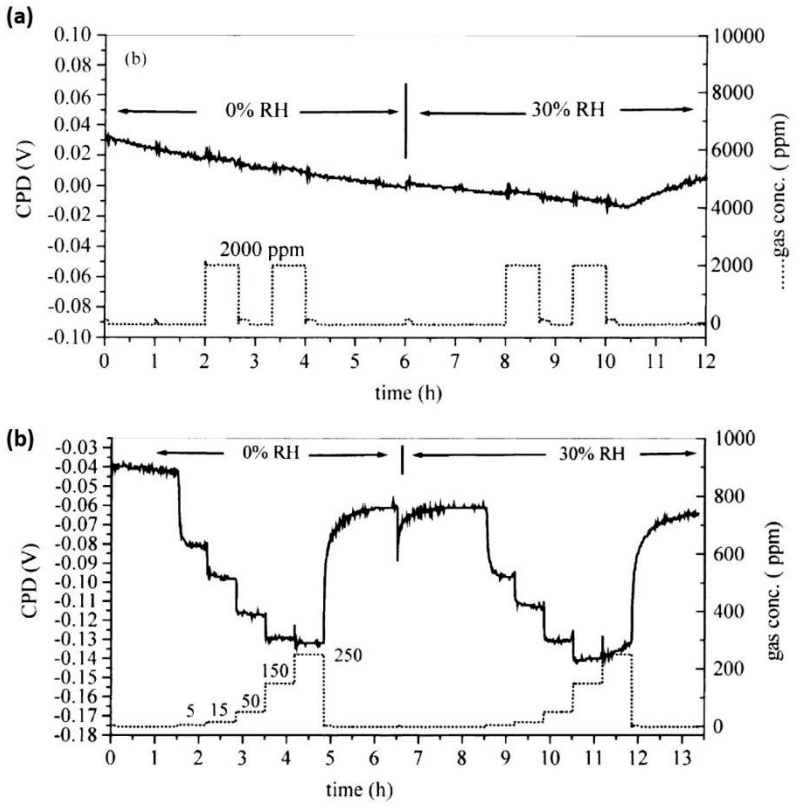

Figure C.4 CPD response of an Ir oxide layer to a) 2000 ppm H_2 under dry and humid air at 30 °C. b) Varying NH_3 concentration at 30 °C under dry and humid conditions. Reproduced from [32].

APPENDIX D UV lithography layout of nanodamascene SETs

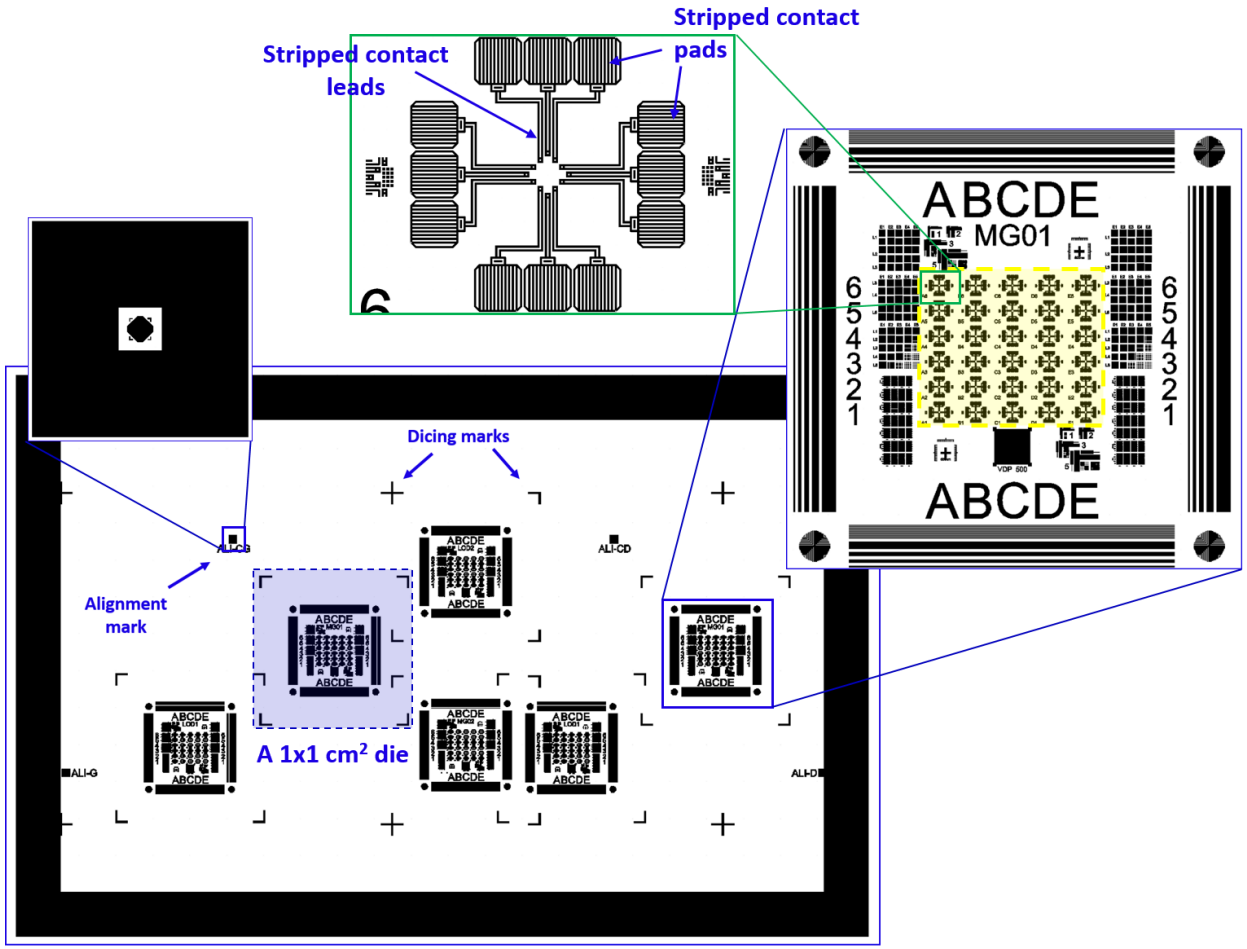

Figure D.1 UV lithography mask layout with a die highlighted in blue. Dummies have been removed for clarity. Right: a close up of a die with the cells matrix highlighted in yellow. Top: a close up of a cell. Left: a close up of an alignment feature.

APPENDIX E Résumé étendu

E.1 Introduction

E.1.1 Mise en contexte

La forte demande et le besoin d'intégration hétérogène de nouvelles fonctionnalités dans les systèmes mobiles et autonomes, tels que les mémoires, capteurs, et interfaces de communication doit prendre en compte les problématiques d'hétérogénéité, de consommation d'énergie et de dissipation de chaleur.

Les systèmes mobiles intelligents sont déjà dotés de plusieurs composants de type capteur comme les accéléromètres, les thermomètres et les détecteurs infrarouge. Cependant, jusqu'à aujourd'hui l'intégration de capteurs chimiques dans des systèmes compacts sur puce reste limitée pour des raisons de consommation d'énergie et dissipation de chaleur principalement. La technologie actuelle et fiable des capteurs de gaz, les résistors à base d'oxyde métallique (les capteurs de gaz MOX) et les MOSFETs (Metal Oxide Semiconductor- Field Effect Transistors) catalytiques sont opérés à de hautes températures de 200–500 °C et 140–200 °C, respectivement. Les derniers sont limités à la détection des molécules décomposables à la surface d'un métal catalytique tel que le H_2, NH_3 ou H_2S.

La haute température d'opération constitue un important coût énergétique pour les MOX et les MOSFET catalytiques. La puissance consommée d'un capteur de gaz est constituée de trois contributions : le transducteur, le dispositif de chauffage du matériau sensible et l'électronique de « read-out », conditionnement du signal et du convertisseur analogique/numérique. La puissance consommée typique des capteurs de gaz de type MOX varie de 200 mW a 1 W [4, 15], incompatible avec les systèmes alimentés sur batterie.

L'élément chauffant constitue la contribution majeure dans la puissance consommé (plus de 80%). La consommation d'énergie de ce type de capteur est en conflit avec les exigences drastiques des systèmes de capteurs intégrés mobiles. L'intégration de ce type de capteur avec de l'électronique intégré sur un même substrat est problématique car la gamme de températures d'opération élevés est incompatible avec l'opération des entités électroniques de traitement analogique ou numérique.

La technologie de micro-machinage a permis l'intégration des composants de détection de gaz dans des membranes diélectriques minces suspendus et ayant une faible conductivité thermique ce qui assure une isolation thermique avec le substrat. Cette technologie a permis de réduire la puissance consommé à la gamme 30–150 mW [4].

Les transistors à effet de champ à grille suspendu (SG-FETs pour Suspended Gate-Field Effect Transistors) offrent l'avantage d'être sensibles aux molécules gazeuses adsorbées aussi bien par chemisorption que par physisorption, et sont opérés à température ambiante ou légèrement au-dessus. Cependant l'intégration de ce type de composant est problématique due au besoin d'implémenter une grille suspendue et l'augmentation du ratio largeur/longueur du canal pour compenser la détérioration de la transconductance due à la faible capacité à travers le gap d'air.

E.1.2 Question de recherche et objectives

Les transistors à double grilles comme transducteur sont d'un grand intérêt pour les applications de détection de gaz, car une des deux grilles est fonctionnalisée et permet de coupler capacitivement au canal les charges induites par l'adsorption des molécules gazeuses cibles, et l'autre grille est utilisée pour le contrôle du point d'opération du transistor sans avoir besoin d'une structure suspendue.

Les transistors monoélectroniques (les SET pour Single Electron Transistors) présentent un candidat de transducteur de capteur de gaz très attractif du à leurs ultra sensibilité de l'ordre de la charge électrique unique [38], mais également à leurs faibles niveaux de courant liée à leur principe de fonctionnement basé sur le transport d'un nombre réduit d'électrons. Les SET sont également attractifs de par leurs dimensions nanométriques.

L'intégration 3D de SET avec la technologie CMOS (Complementary Metal Oxide Semiconductor) avancé basse consommation est d'un grand intérêt pour l'intégration de la fonction détection de gaz et rajouter de nouvelles fonctionnalités au CMOS. L'intégration sur puce CMOS de capteur de gaz à base de SET, illustrée dans la figure E.1, permet de bénéficier des circuits CMOS basse consommation pour le « read-out », le traitement de signal et de données.

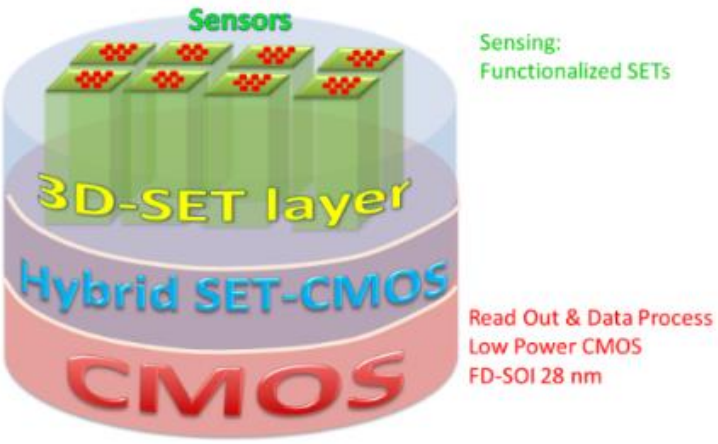

Figure E.1 Concept de l'intégration 3D de circuits hybrides SET-CMOS et capteurs chimique à base de SET [1].

Les MOSFET issus de la technologie FD-SOI (Fully Depleted-Silicon On Insulator) sont une solution très attractive à cause de leur pouvoir d'amplification du signal quand ils sont opérés dans le régime sous-le-seuil. Ces dispositifs permettent une très haute densité d'intégration due à leurs dimensions nanométriques et sont une technologie bien mature et modélisée.

Le travail présenté dans cette thèse fut donc concentré sur la conception et la démonstration de l'intégration 3D monolithique de SET sur un substrat de technologie CMOS pour la réalisation de la fonction capteurs de gaz très sensible et ultra-basse consommation d'énergie. L'approche proposée consiste à l'intégration de SET métalliques à double grilles dans l'unité de fabrication finale BEOL (Back-End-Of-Line) d'une technologie CMOS à l'aide du procédé *nanodamascene*. Le système sur puce profitera de la très élevée sensibilité à la charge électrique du transistor monoélectronique, ainsi que le traitement de signal et des données à haute vitesse en utilisant une technologie de pointe CMOS disponible.

Ce travail a également pour objectif la conception et le développement d'un capteur de gaz à base d'un MOSFET FD-SOI comme transducteur de type transistor à double grilles.

E.2 Conception, modélisation et simulation

Le concept d'utiliser un transistor à double grilles comme l'élément transducteur du capteur de gaz repose sur le principe de découplage des fonctions de polarisation du transistor (ou « read-out ») et détection du signal chimique. Si la conductance du transistor est contrôlée par

deux électrodes de grille indépendantes (par effet de champ), la structure gap d'air n'est plus nécessaire. Une grille de polarisation (ou de contrôle), polarisée par une source de tension, permet de fixer le point d'opération du transistor. Une grille fonctionnalisée avec le matériau sensible adéquat, laissée flottante, permet le couplage de ses variations de charge de surface au canal du transistor induisant des fluctuations de courant autour du point d'opération. Ces fluctuations permettent la détection.

L'implémentation de cette configuration est possible avec les transistors monoélectroniques et les transistors MOSFET issues de la filière FD-SOI. Ces deux types de transistor ont été considérés pour l'implémentation d'un capteur de gaz à base d'un transistor à double grille.

Le matériau sensible est déposé directement sur un plot métallique formant ainsi le plot sensible connecté à l'électrode de grille. L'ensemble forme la grille fonctionnalisée.

E.2.1 Capteur de gaz à base d'un DG-SET

Le transistor monoélectronique *nanodamascene* forme la brique de base du capteur de gaz à base d'un SET à double grilles (DG-SET). La grille fonctionnalisée est implémenté comme une grille supérieure. La grille latérale joue le rôle de la grille de polarisation (ou de contrôle). La structure du capteur de gaz à base d'un DG-SET est représentée dans la figure. E.2. La pente d'un pic de coulomb est la région d'opération d'intérêt qui permettra la transduction des variations de la charge de surface du matériau sensible en variation de courant. La polarisation de la grille de contrôle V_B permet de faire correspondre le point d'opération voulu à la charge de surface Q^0 présente en absence du gaz cible, tel qu'illustré dans la figure E.3.

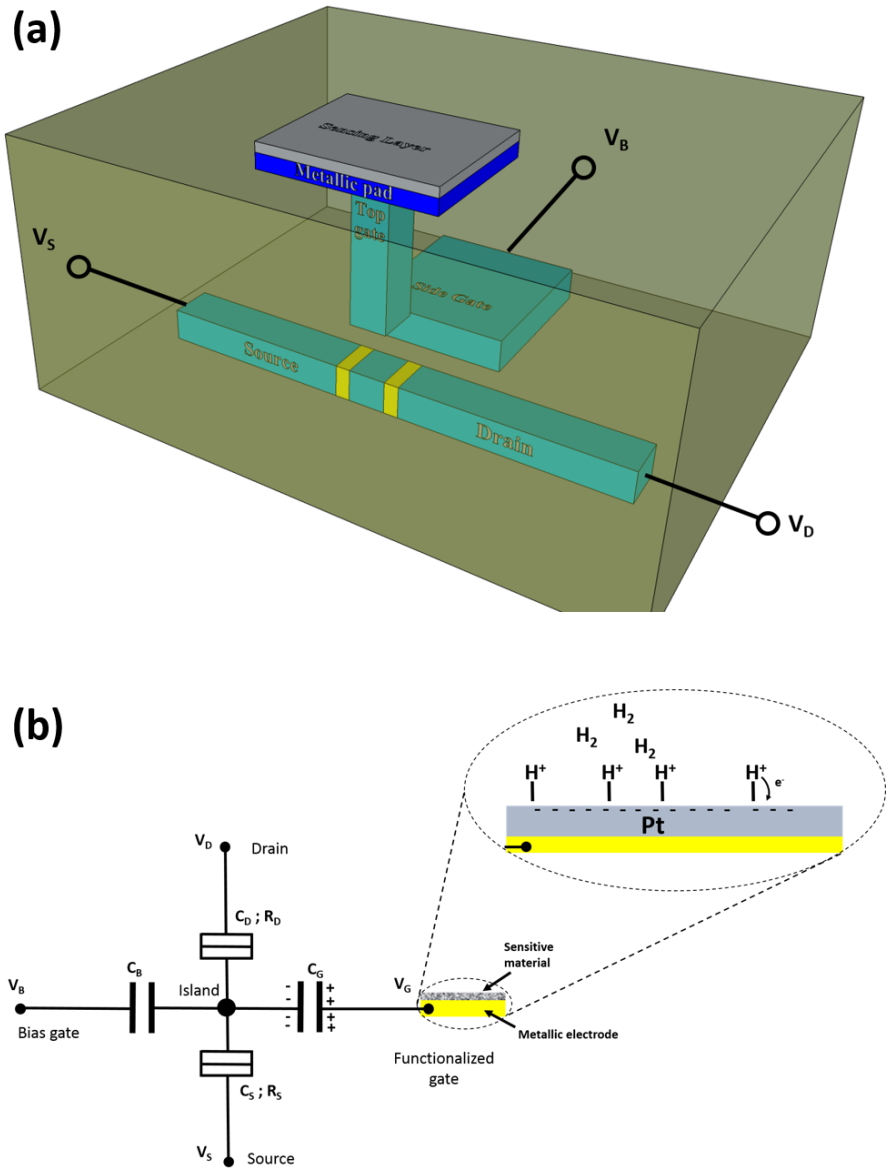

Figure E.2 a) Schéma 3D du concept d'un capteur de gaz à base d'un DG-SET *nanodamascene* montrant le plot sensible connecté à la grille supérieure jouant le rôle de la grille fonctionnalisée et la grille latérale servant de grille de polarisation. b) Circuit équivalent du capteur de gaz à base d'un DG-SET montrant l'îlot capacitivement couplé à deux électrodes de grille : la grille fonctionnalisée et la grille de polarisation. C_G et C_B représentent respectivement la capacité de la grille fonctionnalisée et la capacité de la grille de polarisation. Seule la grille de polarisation est polarisée par la source de voltage V_B.

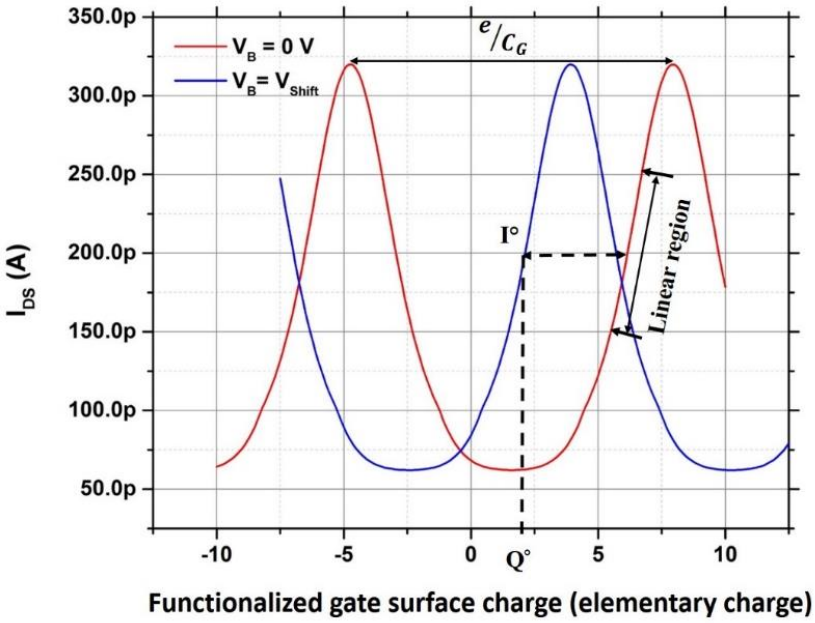

Figure E.3 Oscillations de Coulomb en fonction de la charge de surface de la grille fonctionnalisée pour une polarisation de la grille de contôle $V_B = 0$ V et $V_B = V_{shift}$.

L'incorporation d'une grille supplémentaire augment la capacité totale de l'îlot au dépend de la température d'opération. La conception géométrique de la grille supérieure doit prendre en compte non seulement la capacité de couplage de l'électrode de grille avec l'ilot mais également toutes les autres capacités parasites avec les autres terminaux avoisinants à savoir source drain grille latérale. Ces capacités parasites contribuent à la capacité totale de l'îlot. Le digramme de circuit électrique du dispositif est donné à la figure E.4. Le tableau E.4 rapporte l'ensemble des capacités mises en jeu.

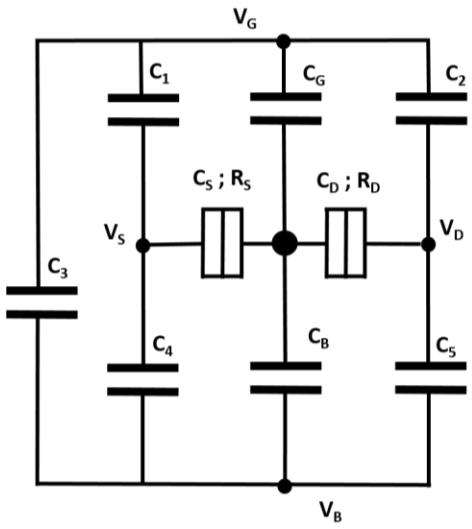

Figure E.4 Circuit du DG–SET montrant les capacités parasites de la grille fonctionnalisée C_1, C_2 et C_3, et celles de la grille de polarisation C_4 et C_5.

Tableau E.1 Ensemble des capacités mises en jeu dans l'opération d'un capteur de gaz à base d'un DG-SET.

Capacité	**Symbol**
îlot-source	C_S
îlot-drain	C_D
îlot-grille de polarisation	C_B
îlot-grille fonctionnalisée	C_G
Grille fonctionnalisée-grille de polarisation	C_3
Grille fonctionnalisée-source	C_1
Grille fonctionnalisée-drain	C_2
Grille de polarisation-source	C_4
Grille de polarisation-drain	C_5

L'ensemble des capacités de la structure, schématisée à la figure E.5, a été calculé pas la méthode d'éléments finis. Les paramètres géométriques de la grille supérieure ont été optimisée en fonction du ratio R définie tel que :

$$R = \frac{C_G}{C_1 + C_2 + C_3} \tag{E.1}$$

La sensibilité du transducteur SET est directement impactée par le ratio R ainsi que le levier de grille C_G/C_Σ.

La structure DG-SET simulée est représentée dans la figure E.5. La longueur de coté A et la distance entre la grille supérieure et l'ilot $D_{Top\ gate}$ sont les seuls paramètres à optimiser.

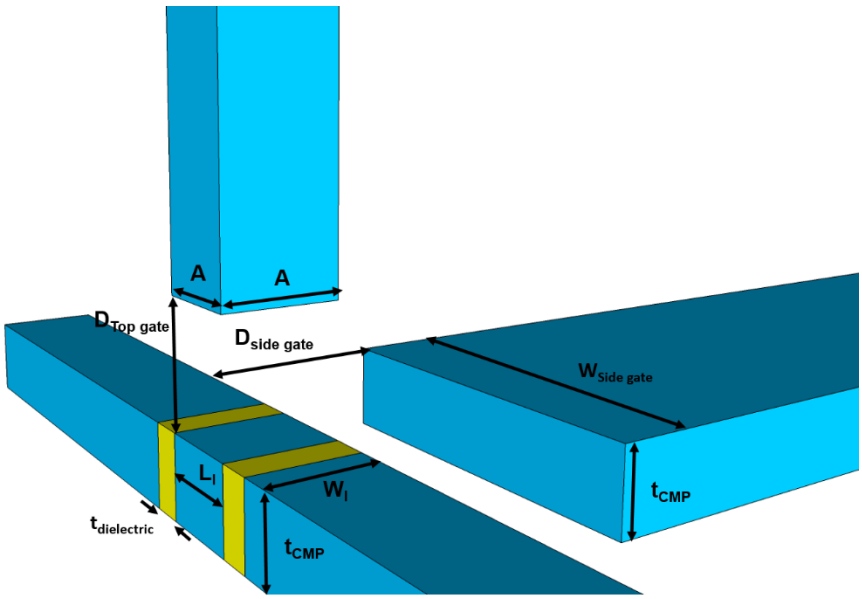

Figure E.5 Schéma 3D du dispositif DG-SET simulé montrant les paramètres géométriques.

Il existe une longueur optimal A qui permet de maximiser le ratio R pour chaque distance $D_{Top\ gate}$. Généralement le choix de A est optimal s'il est égal aux dimensions de l'îlot. Par contre la distance $D_{Top\ gate}$ est le facteur le plus influant sur les caractéristiques du transducteur DG-SET et le paramètre le plus limitant dans le dimensionnement de la grille supérieure car la capacité C_G ne peut pas être affiner indépendamment des capacités parasites C_1, C_2 et C_3. La figure E.6 présente l'impact du paramètre géométrique $D_{Top\ gate}$ sur les capacités de la grille supérieure et le ratio R pour $A = 30$ nm.

L'impact de la réduction de la distance $D_{Top\ gate}$ sur les capacités parasitiques de la grille frontale ($C_2 + C_1 + C_3$), la capacité de la grille frontale (C_G), le ratio R et la capacité totale (C_Σ) de l'ilot, est synthétisé dans le tableau E.2.

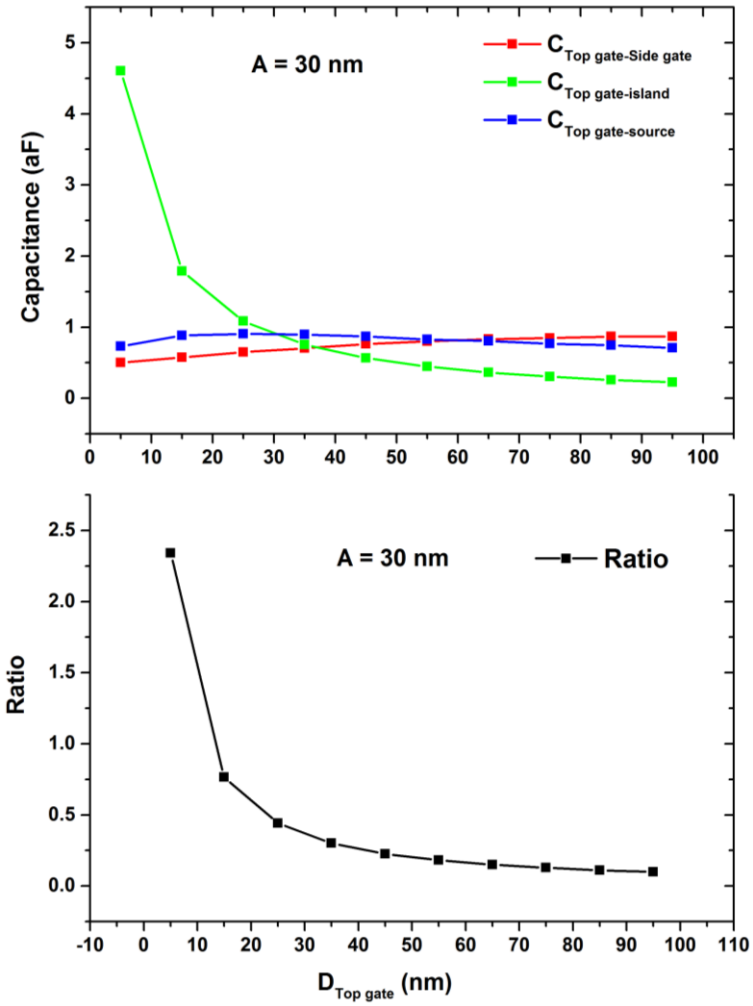

Figure E.6 Impact de la distance $D_{Top\ gate}$ sur les capacités de la grille supérieure. a) Capacités de la grille supérieure *versus* $D_{Top\ gate}$ pour $A = 30$ nm. b) R *versus* $D_{Top\ gate}$ pour $A = 30$ nm.

Tableau E.2 Impact de la réduction de la distance grille supérieure-îlot $D_{Top\ gate}$ sur le total des capacités parasites de la grille supérieure ($C_2 + C_1 + C_3$), la capacité grille supérieure-îlot (C_G), le ratio (R) et la capacité totale de l'îlot (C_Σ).

	Réduction de $D_{Top\ gate}$
$\boldsymbol{C_2 + C_1 + C_3}$	Légèrement réduite
$\boldsymbol{C_G}$ **or** $\boldsymbol{C_G/C_\Sigma}$	Augmenté
$\boldsymbol{R}$	Augmenté
$\boldsymbol{C_\Sigma}$	Augmenté
Sensibilité	Augmentée
Temperature d'opération	Réduite

Placer la grille frontale proche de l'ilot pour augmenter C_G (ou C_G/C_Σ) et R et donc la sensibilité, viendrais au dépende la capacité totale et donc au dépende de la température d'opération. La grille ne devrait pas être placé très proche de l'ilot car, au dépende de R et de la sensibilité, car ceci augmente fortement C_G et par conséquent C_Σ. Placer la grille frontale loin de l'ilot car R est réduite a cause de la réduction de C_Σ et l'augmentation des capacités parasites C_1, C_2 et C_3. Par conséquent, le dimensionnement de $D_{Top\ gate}$ est un compromis entre la sensibilité et la température d'opération.

Les simulations Monte Carlo, ont permis de situer la limite du paramètre $D_{Top\ gate}$, permettant le meilleur couplage tout en permettant un fonctionnement à température ambiante, à 55 nm. Le jeu de capacités correspondant a été retenu pour la simulation de la réponse d'un DG-SET comme transducteur d'un capteur de gaz.

L'impact du désalignement de la grille frontale selon l'axe longitudinal XX' et transversale YY'(voir figure. E.7) sur C_G, $C_2 + C_1 + C_3$, et le ratio R, a été étudiée dans la plage ±50 nm, et présenté dans les figures. E.8 et E.9. Pour un désalignement de ±50 nm R est fortement réduit à 0.2. Le désalignement est donc très critique pour l'obtention de la sensibilité du transducteur

SET voulue. Cependant une erreur dans la limite du ±10 nm, ne réduit *R* que d'au maximum 10%. Cette erreur de désalignement est largement dans la portée des outils de lithographie optique industriels.

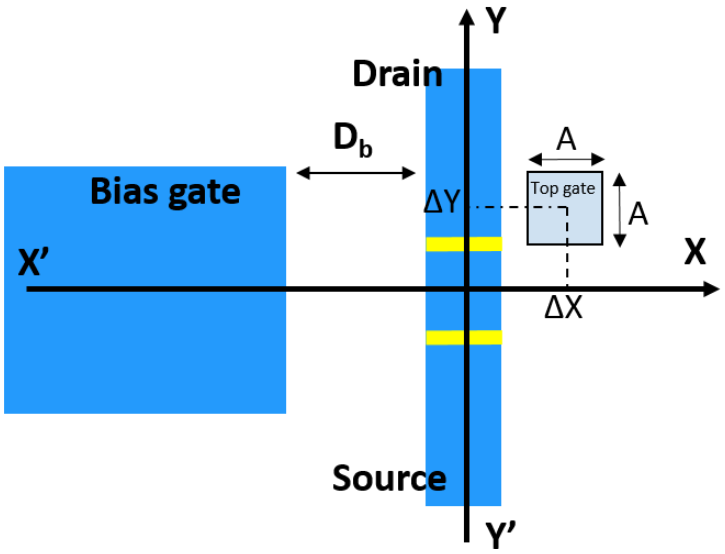

Figure E.7 Illustration schématique de désalignement de la grille supérieure selon les axes XX' et YY' axis. Δ*X* et Δ*Y* représentent la déviation de la position de la grille supérieure selon respectivement l'axe XX' et l'axe YY'.

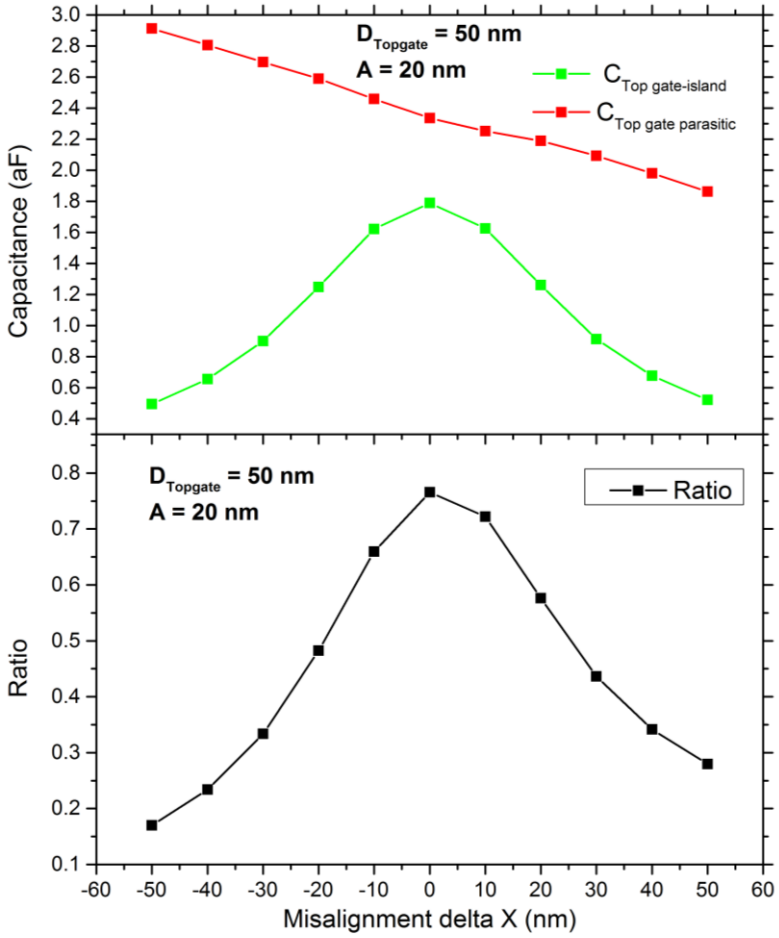

Figure E.8 Impact du désalignement selon l'axe XX' sur les capacités de la grille supérieure pour $D_{Top\ gate} = 15$ nm et $A = 20$ nm. a) Capacités de la grille supérieure *versus* ΔX. b) R *versus* ΔX.

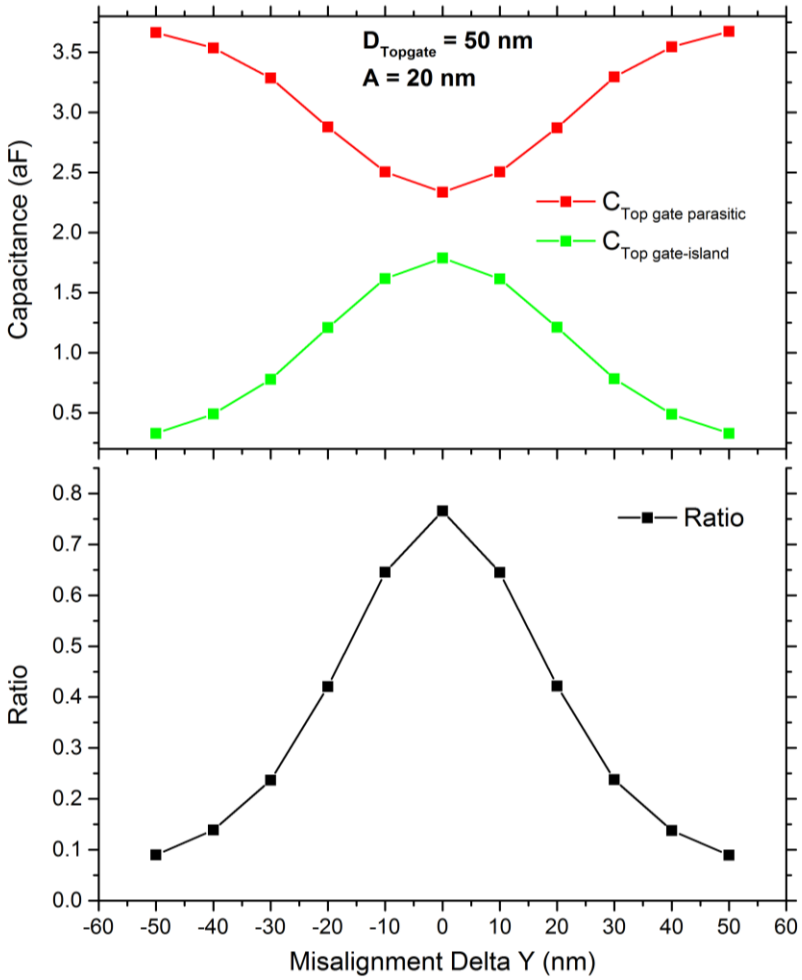

Figure E.9 Impact du désalignement selon l'axe YY' sur les capacités de la grille supérieure pour $D_{Top\ gate} = 15$ nm et $A = 20$ nm. a) Capacités de la grille supérieure *versus* ΔY. b) R *versus* ΔY.

Le modèle du DG-SET avec les capacité parasites a été simulée à l'aide d'un simulateur de type Monte Carlo (SIMON [1]). La grille fonctionnalisée est implémentée comme un nœud non volatile avec une charge fixé. Les résistance des jonctions tunnels ont été fixé à 4.5 $10^7\Omega$, valeur expérimentale estimée dans [2].

La simulation du diamant de Coulomb du modèle du DG-SET avec les capacité parasites à 300 K a permis d'estimer la tension seuil du blocage de Coulomb est de s'assurer que le jeu de capacité retenu correspondant à $D_{Top\ gate} = 55$ nm (voir tableau E.3) permet un fonctionnement adéquat à cette température.

Des simulations du courant en régime stationnaire du transducteur DG-SET avec le jeu de capacité retenu, à 300 K ont été effectuées pour plusieurs valeurs de charge de la grille fonctionnalisée.

Tableau E.3 Valeurs des capacités considérées pour les simulations Monte Carlo.

Capacité	**Value (aF)**
C_S	0.2
C_D	0.2
C_B	0.04
C_G	0.48
C_Σ	0.89
C_1	0.83
C_2	0.83
C_3	0.79
C_4	0.26
C_5	0.266

Le DG-SET est polarisé avec une tension drain-source V_{DS} légèrement inférieure à la tension de blocage de Coulomb à 155 mV.

La caractéristique I_{DS} en fonction de la charge de la grille fonctionnalisée obtenue est montrée sur la figure E.10. La caractéristique exprime des oscillations de Coulomb. À partir de la pente d'un pic de Coulomb, la sensibilité a été extraite et estimée à 900 ±25 pA/aC

(145±4 pA/électron). La puissance consommée du transducteur DG-SET simulé a été estimée à 86 pW, si le point d'opération est pris à la limite inférieure de la pente du pic de Coulomb.

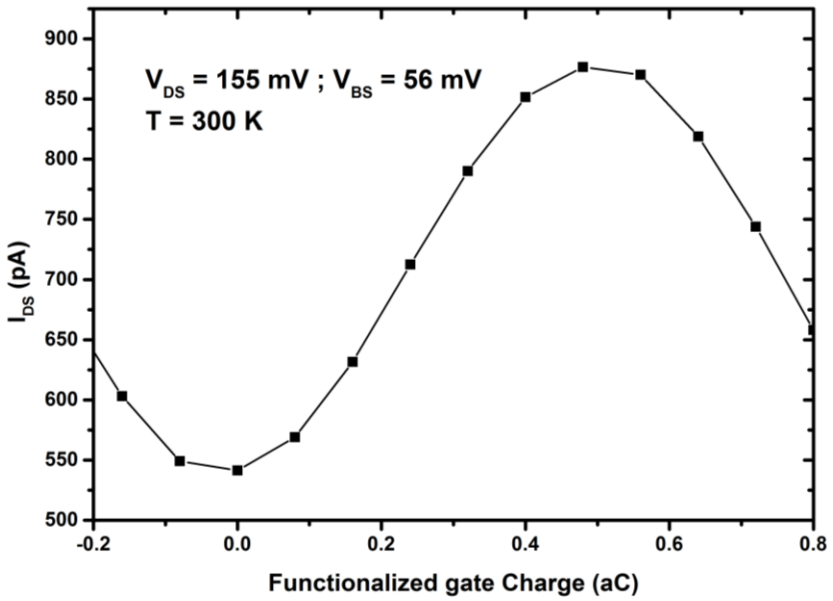

Figure E.10 Caractéristique I_{DS} *versus* la charge de la grille fonctionnalisée simulée pour le modèle du DG-SET avec toutes les capacités parasites à 300 K.

E.2.2 Capteur de gaz à base d'un DG-FET

La configuration capteur de gaz à base d'un transistor à double grille est réalisable avec les MOSFET issue de la filière FD-SOI. Ce type de FET (Fiels Effect Transistor) en plus de la grille frontale, peut être contrôlé par une polarisation de la grille arrière (substrat). La grille frontale joue le rôle de la grille fonctionnalisée. La grille arrière est utilisée comme une grille de polarisation (contrôle). La structure d'un capteur de gaz à base d'un MOSFET FD-SOI est représentée dans la figure E.11. Le plot sensible est connecté à l'électrode de grille frontale. L'ensemble forme la grille fonctionnalisée. La grille arrière dans les MOSFET FD-SOI a le pouvoir de décaler la caractéristique I_{ds} $versus$ V_{gf}/Q_{gf} (potentiel/charge de la grille frontale), tel qu'illustré dans la figure E.12.

La polarisation de la grille de contrôle permet de faire correspondre le point d'opération voulu à la charge de surface Q^0 présente en absence du gaz cible, tel qu'illustré dans la figure E.12.

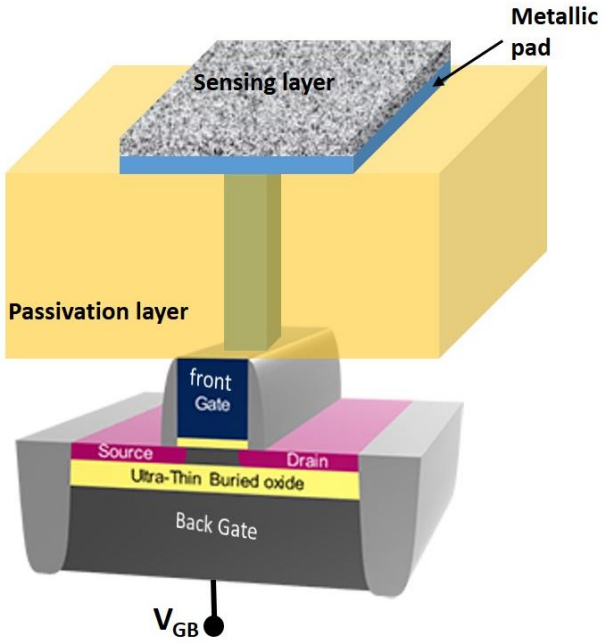

Figure E.11 Illustration schématique du concept de capteur de gaz à base d'un MOSFET FD-SOI montrant la grille frontale connecté au plot sensible et jouant le rôle de la grille fonctionnalisée. Le substrat (grille arrière) joue le rôle de la grille de contrôle.

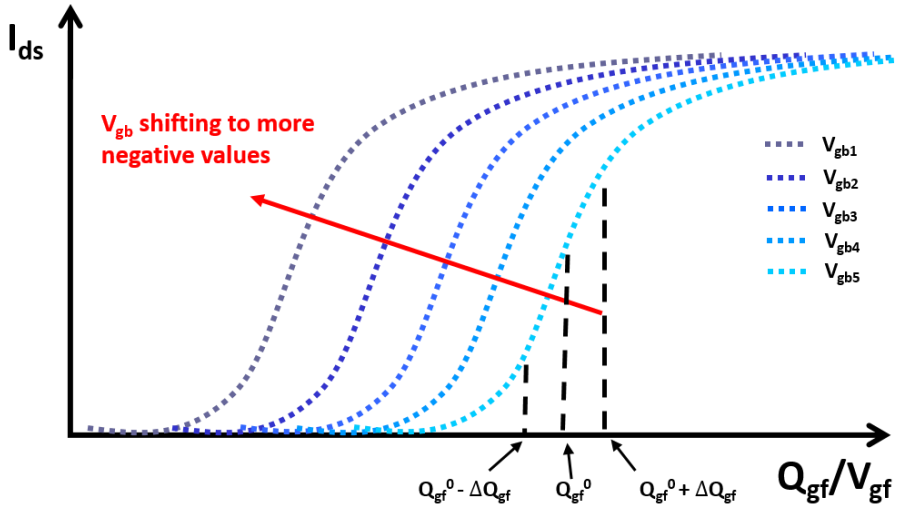

Figure E.12 Caractéristiques typiques $I_{ds}\ versus\ V_{gf}/Q_{gf}$ d'un MOSFET FD-SOI de type n pour différentes polarisation de la grille arrière V_{gb}.

La réponse d'un FET FD-SOI a été simulé grâce un simulateur développé et basé sur un modèle analytique compacte [3, 4]. Le modèle choisi est un modèle d'un MOSFET FD-SOI à canal court, légèrement dopé .de type n et valide aussi bien en régime linéaire qu'en régime de

saturation. Le modèle a été adapté pour permettre de calculer le courant drain-source en fonction de la charge de la grille fonctionnalisée. Les simulations effectués ont permis d'étudier l'impact des dimensions du canal, la polarisation de la grille arrière et la température sur la sensibilité du transducteur de type FET à double grilles (DG-FET). Les caractéristique d'un MOSFET FD-SOI de type n issue de la technologie 28 nm de STMicroelectronics [5]. Les caractéristiques du dispositif simulé sont déraillé dans l'annexe A.

La polarisation de la grille arrière V_{gb} permet le décalage des courbes I_{ds} *versus* Q_{gf} dans une fenêtre d'excursion de largeur 125 aC pour une plage de polarisation de -3 à 3 V. La sensibilité estimée est quasi constante en fonction de la polarisation de la grille arrière et égale à 1.8± 0.1 µA/aC pour $V_{ds} = 0.1$ V, $L = 30$ nm et $W = 0.5$ µm ou L et W représentent respectivement la longueur et la largeur du canal.

La réduction de la longueur du canal augmente la sensibilité tout en réduisant la plage de sensibilité (plage de la pente sous seuil). Également le raccourcissent du canal augmente les niveaux de courant I_{ds}. La variation de la sensibilité en fonction de la longueur de grille est montrée sur la figure. E.13. pour $V_{ds} = 0.1$ V, $V_{gb} = 2$ V, et $W = 0.5$ µm.

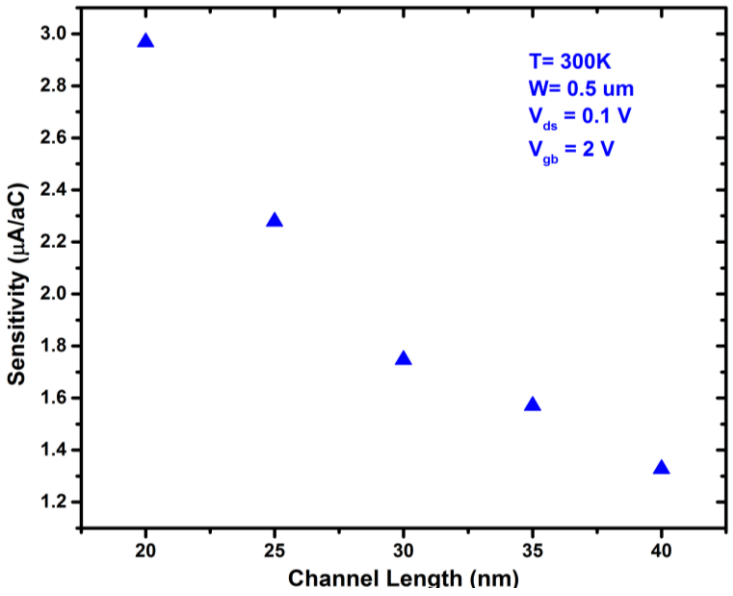

Figure E.13 Sensibilité extraite en fonction de la longueur du canal pour $V_{ds} = 0.1$ V, $V_{gb} = 2$ V, et $W = 0.5$ µm

La sensibilité est quasi constante en fonction de largeur de grille et égale en moyenne à 1.8 ± 0.1 µA/aC pour $V_{ds} = 0.1$ V, $V_{gb} = 2$ V, et $L = 30\ nm$. Le rétrécissement de la largeur du

canal permet de réduire les niveaux de courant et par conséquent la puissance consommée, mais aussi la plage de sensibilité. La variation de la température entre 300 et 400 K a un effet négligeable sur la sensibilité. L'augmentation de la température décale les caractéristiques I_{ds} *versus* Q_{gf} vers les valeurs négatives. La puissance consommé par un transducteur de type MOSFET FD-SOI, avec $L = 30$ nm et $W = 0.5$ µm et polarisé par $V_{ds} = 0.1$ V et $V_{gb} = 2$ V, est estimé à 1.23 µW.

E.2.3 Comparaison des performances du DG-FET et le DG-SET

Les sensibilités et la puissance consommée des deux type de transducteurs considérés est rapporté dans le tableau E.4.

De point de vue puissance consommée, le DG-SET est 4 ordres de grandeurs moins énergivore que le DG-FET, dû à ses très faibles niveaux de courant résultant de son principe de fonctionnement basé sur le transport d'un nombre réduit d'électrons. La puissance consommée estimée du DG-SET comme transducteur d'un capteur de gaz est largement au-delà de l'état de l'art des capteurs de gaz à base de FET. La puissance consommée du transducteur dans les capteurs de gaz de type MOSFET catalytiques et SG-FET s'étends entre quelques dizaines à 100 µW [6–10]. Cependant la technologie de fabrication des SET opérant à température ambiante pose encore défi et reste à être optimisé.

En revanche, le FET FD-SOI est 3 ordres de grandeur plus sensible que le DG-SET *nanodamascene*. La sensibilité obtenus de quelque µA/aC est largement suffisante pour la fonction de détection vu le haut ratio signal à bruit de ce type de transducteur (dû à leur énorme pouvoir d'amplification si polarisé dans le régime sous-le-seuil). La sensibilité du DG-SET a été pénalisée par le compromis fait dans le dimensionnement de la grille frontale entre couplage et capacité totale de l'îlot.

La puissance consommée du MOSFET FD-SOI comme transducteur d'un capteur de gaz est au moins 1 ordre de grandeur plus faible que l'état de l'art des capteurs de gaz à base de FET. Cette puissance a été estimé pour un dispositif avec $L = 30$ nm et $W = 0.5$ µ et peut être divisé par 5 si la largeur du canal est réduite à 100 nm ($L/W = 5$).

Tableau E.4 Comparaison des performances des transducteurs DG-SET et DG-FET étudiés

	DG-FET	DG-SET
Sensibilité (µA/aC)	1.8	$9\ 10^{-4}$
Puissance consommée (µW)	1.23	$8.6\ 10^{-5}$

L'intégration des MOSFET FD-SOI comme capteur de gaz et très prometteuse en raison de la grande sensibilité et la puissance consommé très réduite. En plus la grande sensibilité de ce type de transducteur permettrait la réduction de la surface sensible et par conséquent la réduction de l'apport énergétique nécessaire pour le chauffage du matériau sensible.

Les MOSFET sont une solution très attractive de point de vue densité d'intégration. due à leurs dimensions nanométriques et maturité de la technologie.

E.3 Fonctionnalisation de la grille sensible

La deuxième brique du projet de recherche est la fonctionnalisation de la grille sensible. Le choix sur le matériau sensible fut porté sur le Pt pour la détection du H_2. Préalablement au dimensionnement de la surface du plot sensible à intégrer avec un DG-SET ou un DG-FET, la sensibilité du Pt à l'hydrogène a été caractérisée par une nouvelle technique de mesure de charge de surface.

Cette technique de caractérisation de la sensibilité du matériau est alternative à la sonde Kelvin, largement utilisé pour la caractérisation de matériaux convenables à l'intégration avec des transducteurs de type FET.

E.3.1 Mesure de la charge de surface

La sonde Kelvin a été la technique privilégiée pour la caractérisation des matériaux sensibles par le biais de mesure de la variation du travail de sortie induite par l'adsorption de molécules de gaz. Dans ce travail, une technique de caractérisation des matériaux sensibles alternative basée sur la mesure de la charge de surface est discutée.

Une nouvelle technique de caractérisation de la sensibilité du matériau sensible basé sur la mesure de variation de charge de surface induite par l'adsorption des molécules cible, est

proposée. La technique permet la mesure de la charge de surface d'un matériau, contrairement à la méthode de la sonde Kelvin qui évalue le travail de sorti du matériau. La mesure de charge est réalisée à l'aide d'un électromètre en mode coulombmètre avec un amplificateur en configuration boucle fermée. La sensibilité du matériau est estimé en terme variation de charge par unité de surface par unité de concentration du gaz cible. La variation de la charge de surface est égale en amplitude mais de signe opposé à la variation de la lecture donné par l'électromètre.

E.3.2 Caractérisation de la sensibilité du platine au H_2

La technique de mesure de charge de surface a été appliquée pour la détection de l'hydrogène avec un film de Pt de 50 nm d'épaisseur et d'une surface de 13 mm^2 déposé sur une couche de Ti. .Préalablement la sensibilité du Pt à la variation de la concentration de l'oxygène dans du N_2 pur a été caractérisé. L'injection de l'oxygène dans de l'azote pur induit une variation positive dans la lecture de l'électromètre pour plage de température de 80-190 °C. La réponse du Pt en termes de variation de charge à l'injection de 20% d'O2 en fonction de la température est donnée à la figure. E.14. La réponse du plot sensible de surface de 13 mm^2 en Pt à l'injection de 20% d'oxygène à 80°C est égale à 13pC. Par conséquent une variation de quelques % de la teneur de l'atmosphère en oxygène induirait une variation négligeable par rapport au signal d détection de l'hydrogène.

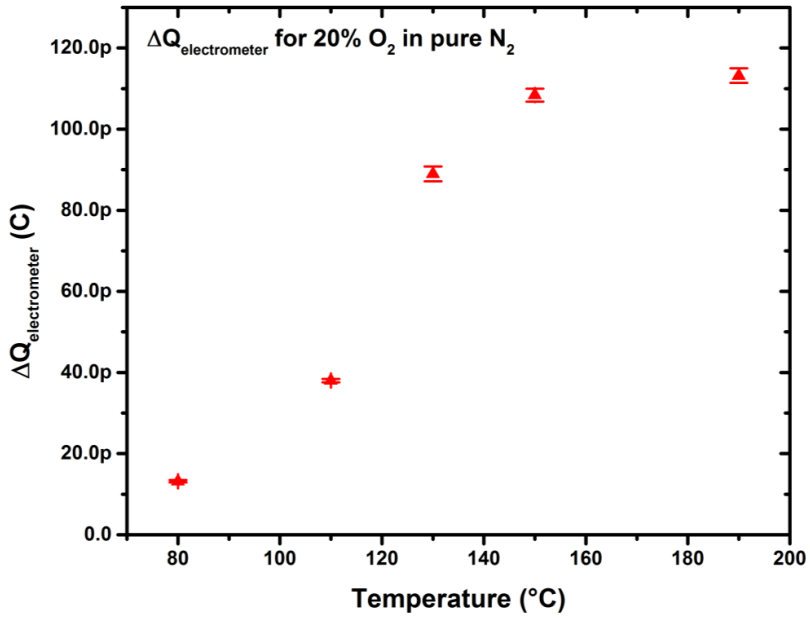

Figure E.14 Réponse de la couche de Pt en variation de charge à l'injection de 20% d'oxygène dans l'azote pur en fonction de la température de 80 à 190 °C.

La sensibilité du Pt à l'hydrogène dans l'air synthétique (80% N_2 et 20% O_2) a été caractérisée pour l'intervalle de température 50-190 °C. À une température de 80 °C ou au-dessus, le Pt exhibe une variation positive de la lecture de charge. En dessous de cette température, la réponse du Pt est variation négative, qui correspond à une variation positive de la charge de surface cohérente avec la littérature. Les signaux réponse du Pt en termes de lecture de charge de l'électromètre à l'injection de 0.5% d'hydrogène à 130 °C et l'injection de 4% d'hydrogène à 60 °C sont montrés respectivement sur les figures. E.15 et E.16.

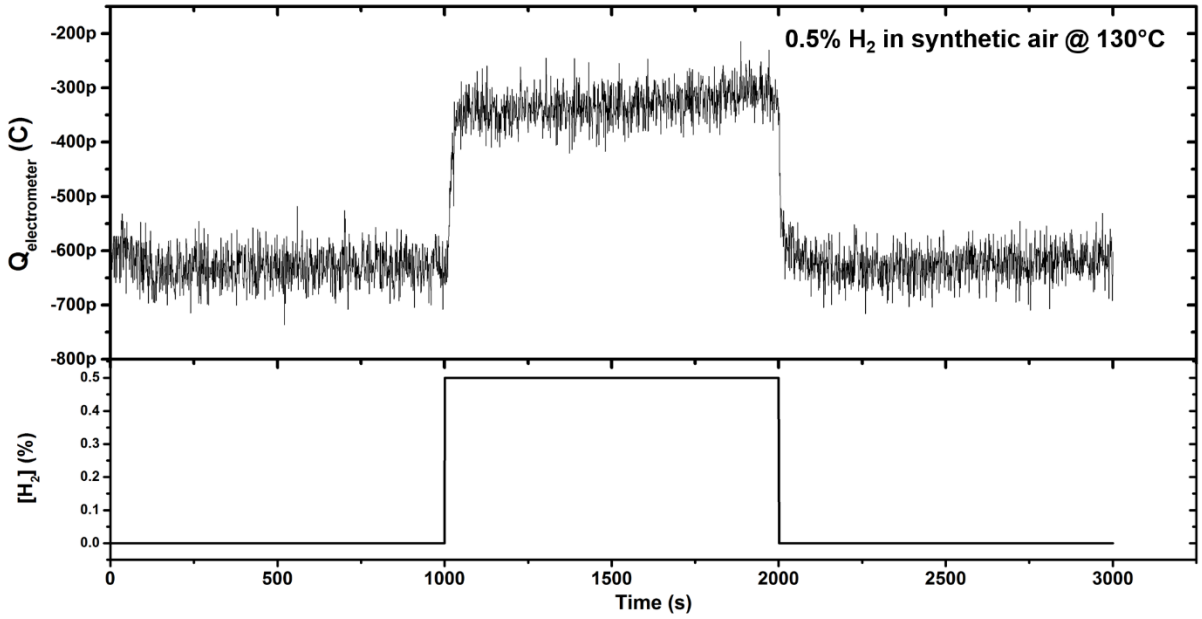

Figure E.15 Signal réponse de la couche de Pt en termes de lecture de charge de l'électromètre à l'injection de 0.5% d'hydrogène dans l'air synthétique à 130 °C.

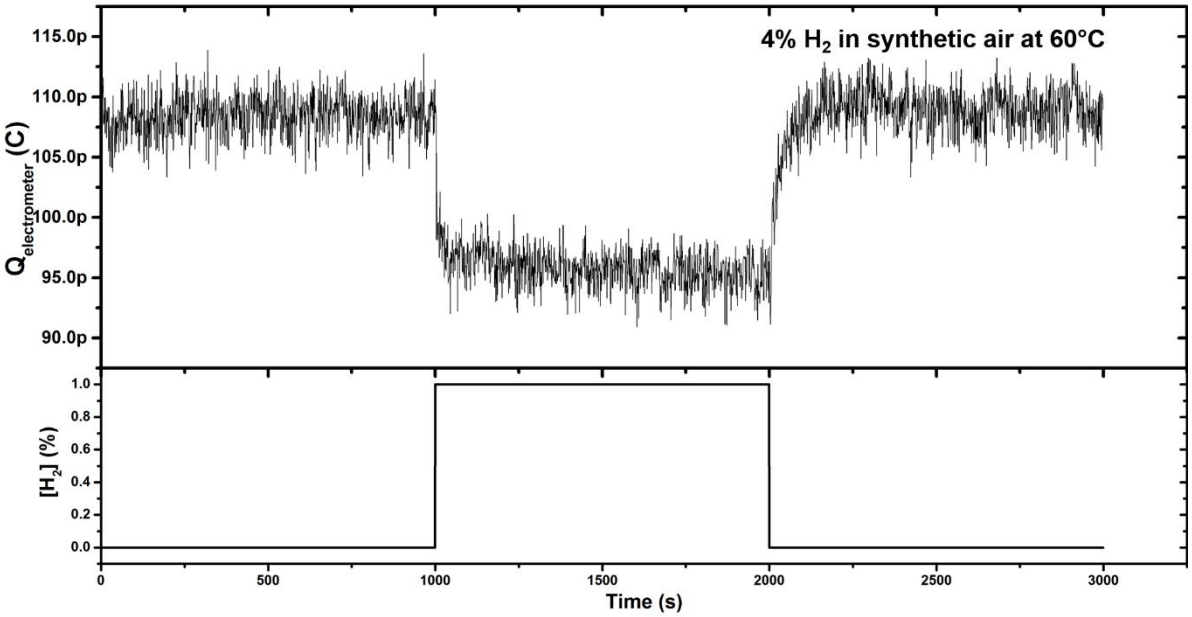

Figure E.16 Signal réponse de la couche de Pt en termes de lecture de charge de l'électromètre à l'injection de 4% d'hydrogène dans l'air synthétique à 60 °C.

La réponse du Pt à l'hydrogène a été investiguée dans l'intervalle de concentration 0.5-5% à 60 °C et est montré sur la figure E.17. une linéarité de la réponse du Pt au logarithme de la concentration du hydrogène a été obtenue, en cohérence avec la littérature [11–14]. Au-dessus de la concentration de 3%, la réponse du Pt exhibe une tendance à la saturation. La sensibilité extraite de la couche de Pt à 60°C a été estimé à -0.8 pC/decade par mm^2.

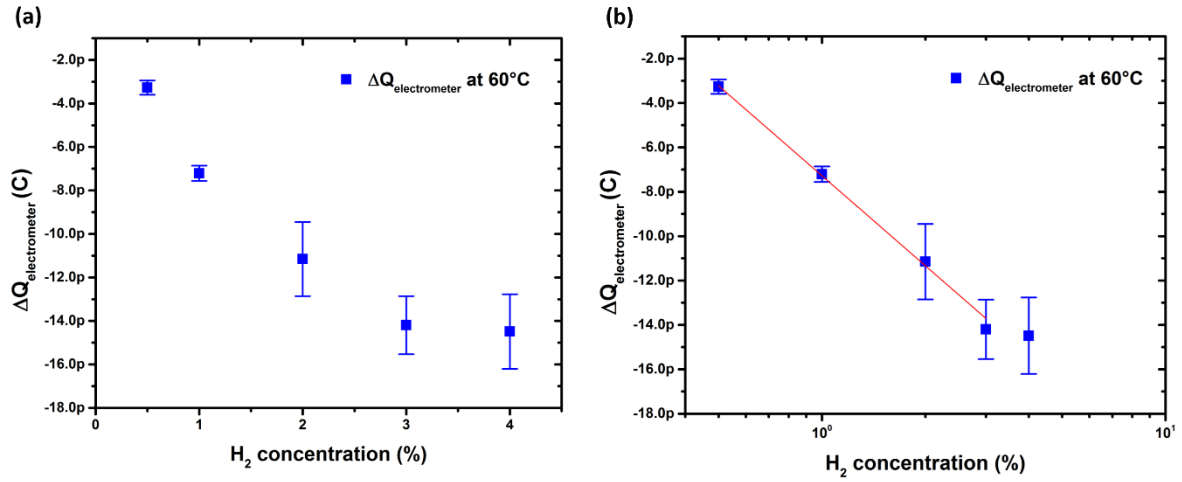

Figure E.17 Réponse de la couche de Pt en variation de charge en fonction de la concentration de H_2 dans l'air synthétique à 60 °C à l'échelle linéaire (a) et l'échelle semi-logarithmique (b).

La réponse positive en terme de variation de la lecture de charge, qui correspond à une variation négative de la charge de surface, observé au-dessus de 80 °C est synonyme d'une augmentation du travail sortie. Cette réponse est, probablement, dû à la diffusion de l'hydrogène atomique à travers de la couche de la platine et l'adsorption à l'interface Pt/Ti ou Pt/TiO_x par le mécanisme d'adsorption de type r. Une investigation plus approfondie de ce type de réponse est nécessaire. La réponse du Pt à l'injection de 4% d'hydrogène en fonction de la température allant de 80 à 190 °C est montrée sur la figure. E.18. La réponse du Pt au H_2 a été investiguée dans l'intervalle de concentration 0.5-4% à 130 °C, et est montré sur la figure. E.19.

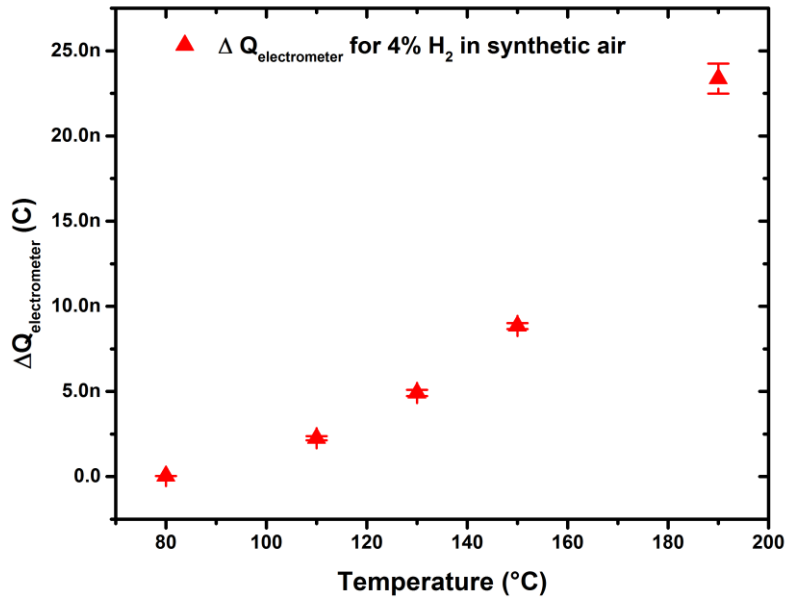

Figure E.18 Réponse de la couche de Pt en variation de charge à l'injection de 4% d'hydrogène dans l'air synthétique en fonction de la température de 80 à 190 °C.

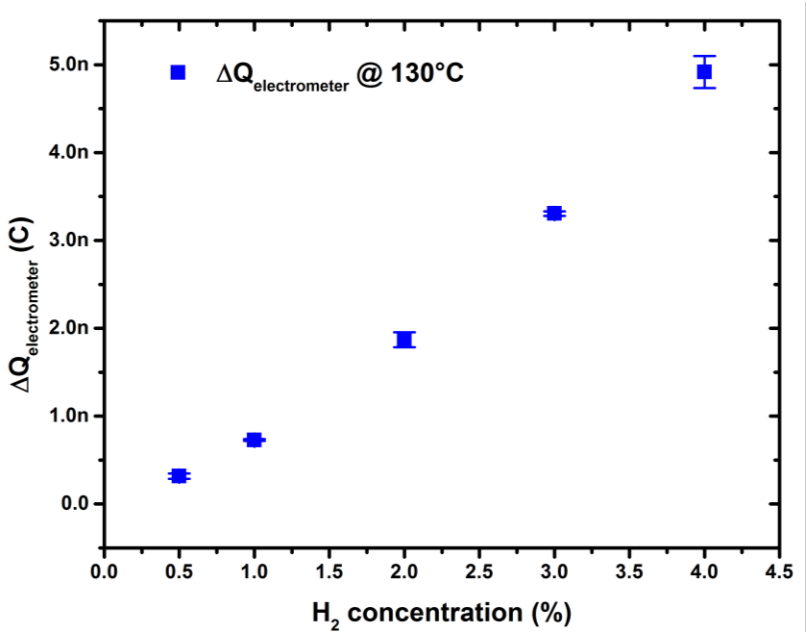

Figure E.19 Réponse de la couche de Pt en variation de charge en fonction de la concentration de H_2 à 130 °C.

E.3.3 Dimensionnement de la surface sensible

La sensibilité extraite du Pt à l'hydrogène à 60 °C a été utilisée pour le dimensionnement de la surface du plot sensible en Pt à intégrer en combinaison avec un DG-FET ou un DG-SET pour la détection d'hydrogène dans l'intervalle de concentration 0-4%. La réponse du capteur de gaz conçu a été simulée et la sensibilité a été extraite.

Considérant le même dispositif DG-SET utilisé pour les précédentes simulations et polarisé dans les mêmes conditions, la surface de platine nécessaire est de 0.36 μm^2. La réponse en termes de variation du courant drain-source du capteur d'hydrogène à base d'un DG-SET en fonction de la concentration d'hydrogène est montrée sur la figure E.20. La sensibilité extraite de la pente de la région linéaire s'étalant de 0 à 3% est de 100 pA/%H_2. La surface ultra-réduite de platine est une conséquence de l'énorme pente du pic de Coulomb et de la fenêtre d'excursion réduite de la charge de la grille fonctionnalisée.

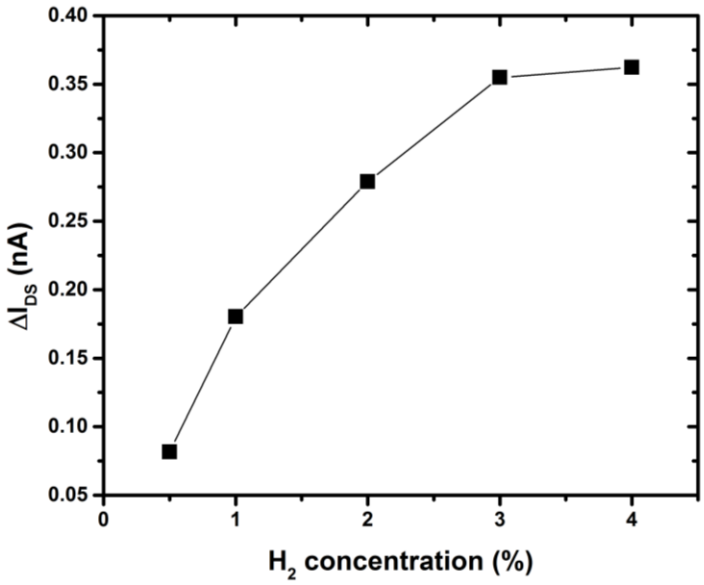

Figure E.20 Réponse simulée du capteur d'hydrogène à base d'un DG-SET fonctionnalisé avec du Pt en fonction de la concentration de H_2 dans l'air synthétique.

Pour l'intégration du Pt comme matériau sensible pour la détection de l'hydrogène avec un DG-FET, un dispositif de type MOSFET FD-SOI, de type n ayant les caractéristiques $L =$ 30 nm et $W = 0.5$ µm et polarisé à $V_{ds} = 0.1$ V, a été considéré. La surface nécessaire en platine pour la détection de l'hydrogène de 0 à 4% est de 60 µm^2.

La réponse du capteur conçu en termes de variation du courant drain-source est présentée dans la figure E.21. La sensibilité extraite sur la plage de concentration 0-3% est égale à 41 µA/%H_2. Cette sensibilité élevée permet de pousser la limite de détection jusqu'à l'ordre de quelque ppm. Pour une injection de 1 ppm d'hydrogène la variation du courant est estimée à 4.1 nA, qui constitue un signal considérable facilement lu par un circuit de « read-out ». La puissance consommée est estimée à 1.23 µW.

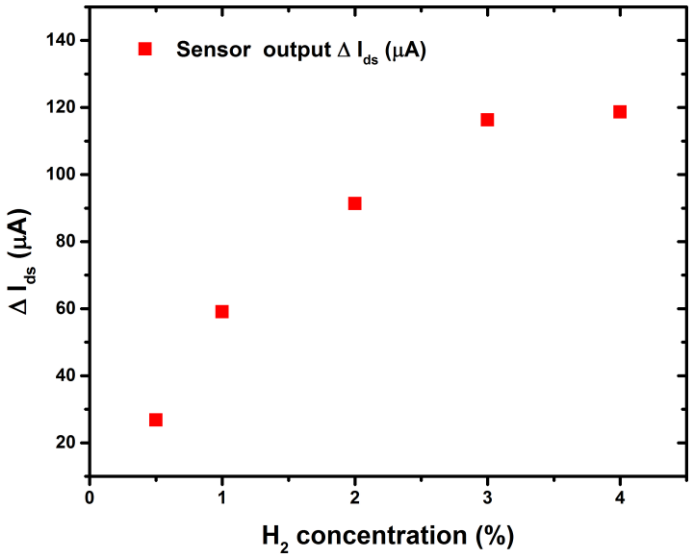

Figure E.21 Réponse simulée du capteur d'hydrogène à base d'un DG-FET fonctionnalisé avec du Pt en fonction de la concentration de H_2 dans l'air synthétique.

Cependant, pour opérer le capteur d'hydrogène DG-FET de la sorte, la grille arrière a été polarisé à -26 V, ce qui constitue une polarisation non commode dans les circuits intégrés. Le capteur DG-FET peut être opérer à courant constant par asservissement en boucle fermée de la polarisation de la grille arrière. Dans ce cas, la variation du voltage d'asservissement appliqué à la grille arrière en réaction à la détection d'hydrogène constitue le signal de réponse. Les caractéristiques $I_{ds}\ versus\ V_{gb}$ du dispositif considéré à différentes concentration d'hydrogène sont présentées dans la figure. E.22. Le choix du niveau de courant drain-source d'opération est imposé par la plage de variation de la polarisation de la grille arrière. Pour une plage de -1 à 1 V, niveaux de tensions compatible avec les circuits intégré, le courant drain-source est pris à 120 µA. Ceci a conduit à une augmentation de la puissance consommée jusqu'à 12 µW. La réponse simulée en termes de variation du voltage de la grille arrière en fonction de la concentration de H_2 dans l'air synthétique est donné à la figure E.23. La sensibilité extraite est égale à 750 mV/%H_2. La sensibilité des capteurs d'hydrogène à base de MOSFET catalytiques ou de SG-FET fonctionnalisés avec du platine varie de 70 à 200 mV/%H_2 [13, 15, 16]. La sensibilité estimé du DG-FET est 3 fois plus large que celles relates dans l'état de l'art de la détection d'hydrogène avec des FET. Cette large sensibilité est due à l'important facteur de couplage entre les deux grilles du MOSFET FD-SOI étudié.

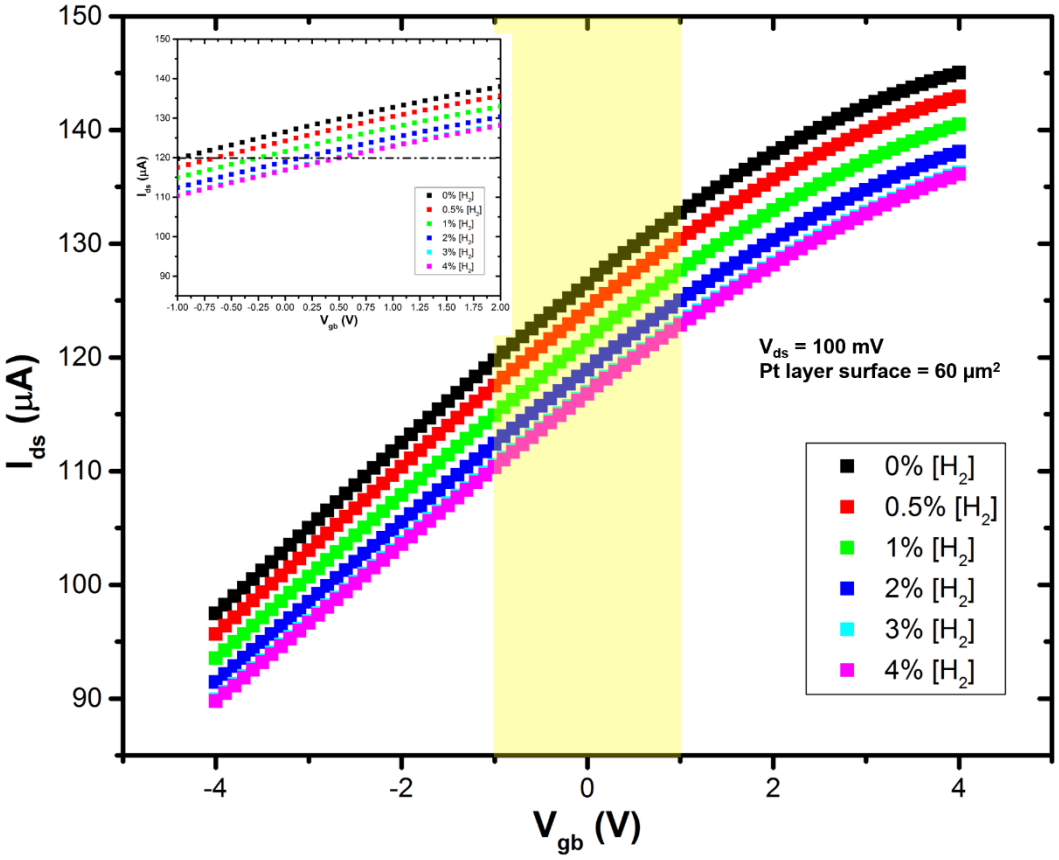

Figure E.22 Caractéristiques I_{ds} *versus* V_{gb} simulées du capteur de H_2 à base d'un DG-FET fonctionnalisé avec du Pt à différentes concentrations d'hydrogène de 0 à 4%.

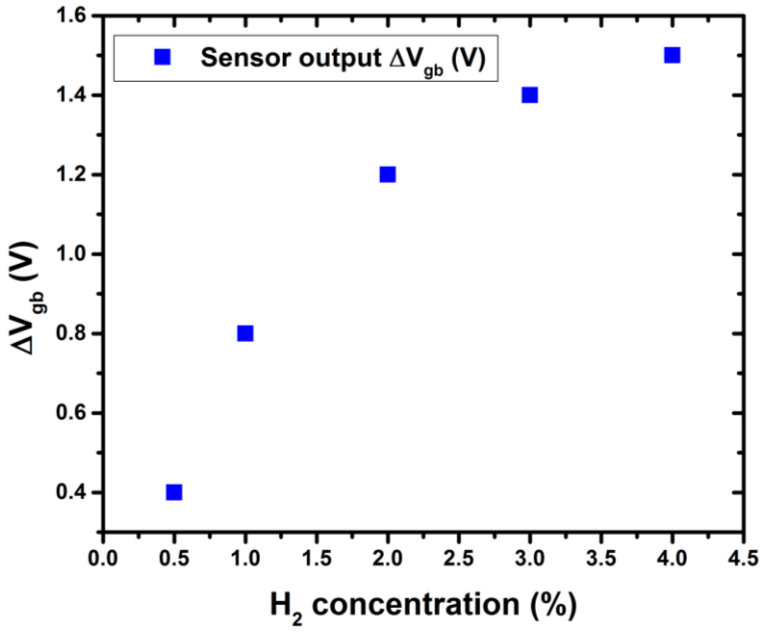

Figure E.23 Réponse simulée en terme de voltage de la grille arrière du capteur d'hydrogène à base d'un DG-FET fonctionnalisé avec du Pt en fonction de la concentration de H_2 dans l'air synthétique.

La surface ultra réduite de Pt nécessaire pour réaliser le capteur d'hydrogène à base d'un MOSFET FD-SOI est atout majeur en faveur de ce type de transducteur ultra-sensible, comparé à l'état de l'art de la technologie de capteur de gaz à base de FET. Généralement la surface sensible dans les MOSFET catalytique et SG-FET varie de quelques centaines de μm^2 à quelques mm^2. La réduction de la surface sensible permet une haute densité d'intégration mais surtout la réduction considérable de la puissance de chauffage et par conséquent la puissance de chauffage.

E.4 Intégration de dispositifs SET sur CMOS

E.4.1 Optimisation du procédé de fabrication

Depuis la 1ère démonstration de transistors monoélectroniques métalliques réalisés par le procédé *nanodamascene* opérant à température ambiante par Dubuc *et al.* [17], ce procédé de fabrication a été développé et optimisé jusqu'à la démonstration d'intégration de SET métalliques dans l'unité de fabrication finale (BEOL pour Back-End-Of-Line) d'une

technologie CMOS par N. Jouvet [18]. Cette intégration réussite de SET constitue la brique de départ pour l'intégration de SET métalliques à double grilles sur puce CMOS encastré dans une couche diélectrique d'interconnexion pour la réalisation de la fonction détection chimique.

Le procédé *nanodamascene* utilisé dans ce projet de recherche a été optimisé pour permette la fabrication de SET métalliques alignés sur les structures de la couche CMOS. Le procédé de fabrication, détaillé à la figure E.24, combine lithographies optiques, lithographie électroniques et planarisation mécano-chimique pour fabriquer des structures métalliques planaires encastrées dans la couche diélectrique supérieure du substrat CMOS. La planarisation mécano-chimique, étape clé du procède, permet d'amincir les structures planaires pour obtenir des jonctions tunnel avec de très faibles sections et par conséquent de très faibles capacités permettant l'opération à température ambiante.

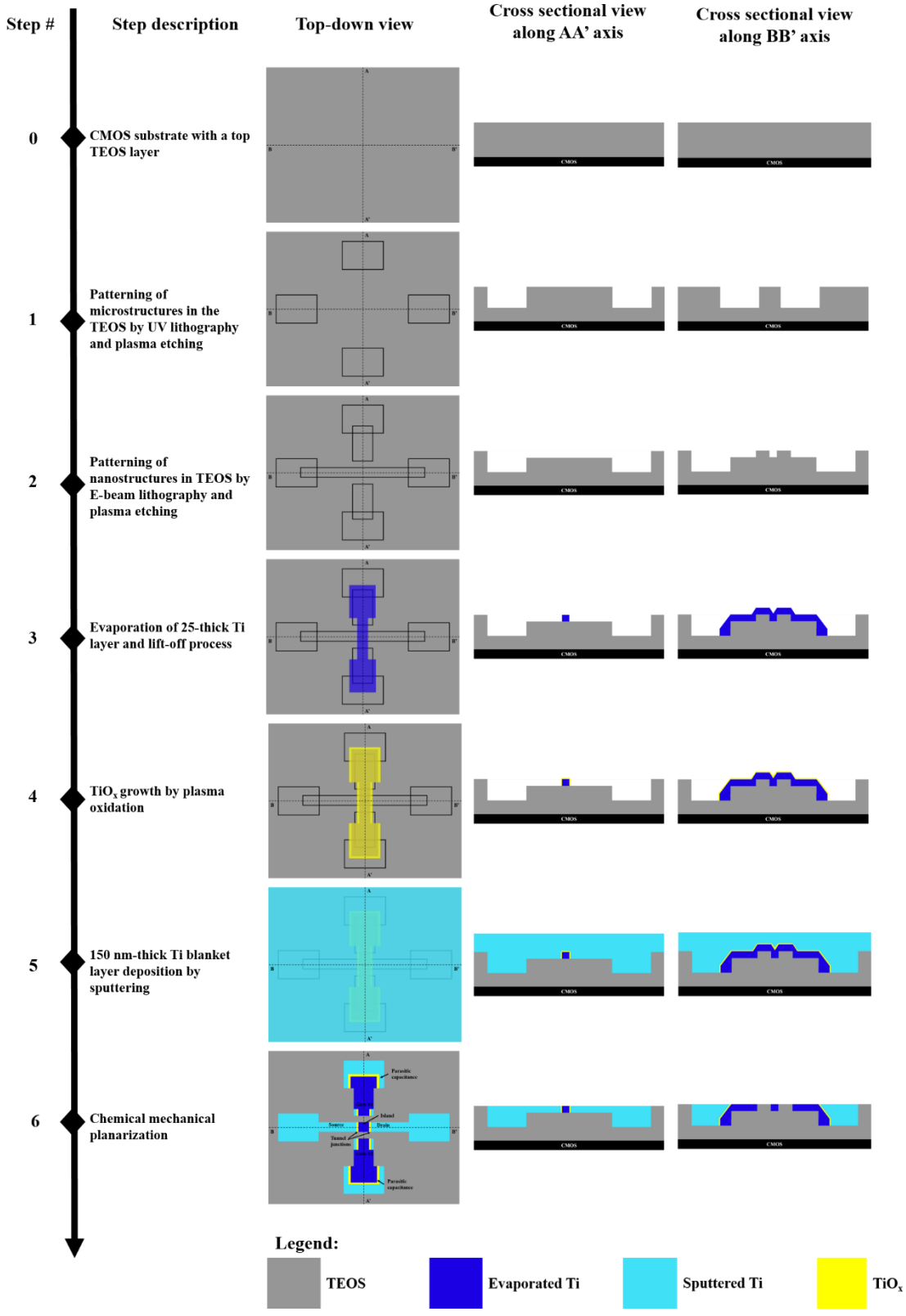

Figure E.24 Procédé *nanodamascene* de fabrication de DG-SET.

L'intégration sur CMOS de SET *nanodamascene* pose un défi à cause des contraintes suivantes :

- Alignement des lithographies sur les structures CMOS
- La nano-topographie de la couche diélectrique supérieure du substrat CMOS, surtout si l'épaisseur cible des structures désirées et de 5 nm.
- L'empilement des couches diélectriques ULK (pour Ultra Low K)
- Juxtaposition de structures micrométriques et nanométriques.
- Présence à la même surface de différent matériaux ex. du Ti déposé par évaporation, du Ti déposé par pulvérisation cathodique, des diélectriques comme le Al_2O_3 ou le TiO_x.

Avec la version initiale des masques de lithographie optique et électronique, une planarisation non homogène mais également un problème de remplissage des tranchées ont été observés, tel que vu sur les figure E.25, E.26 et E.27.

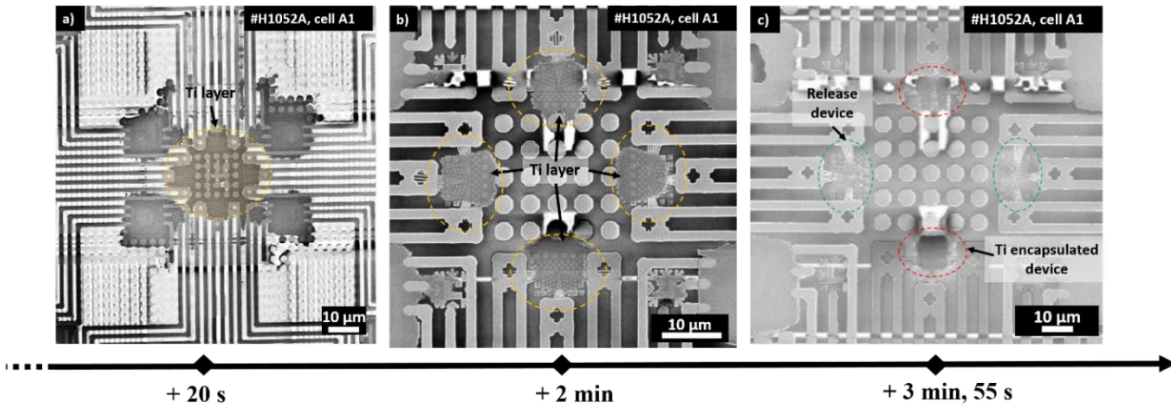

Figure E.25 Observation SEM d'une même cellule le long du procédé de planarisation.

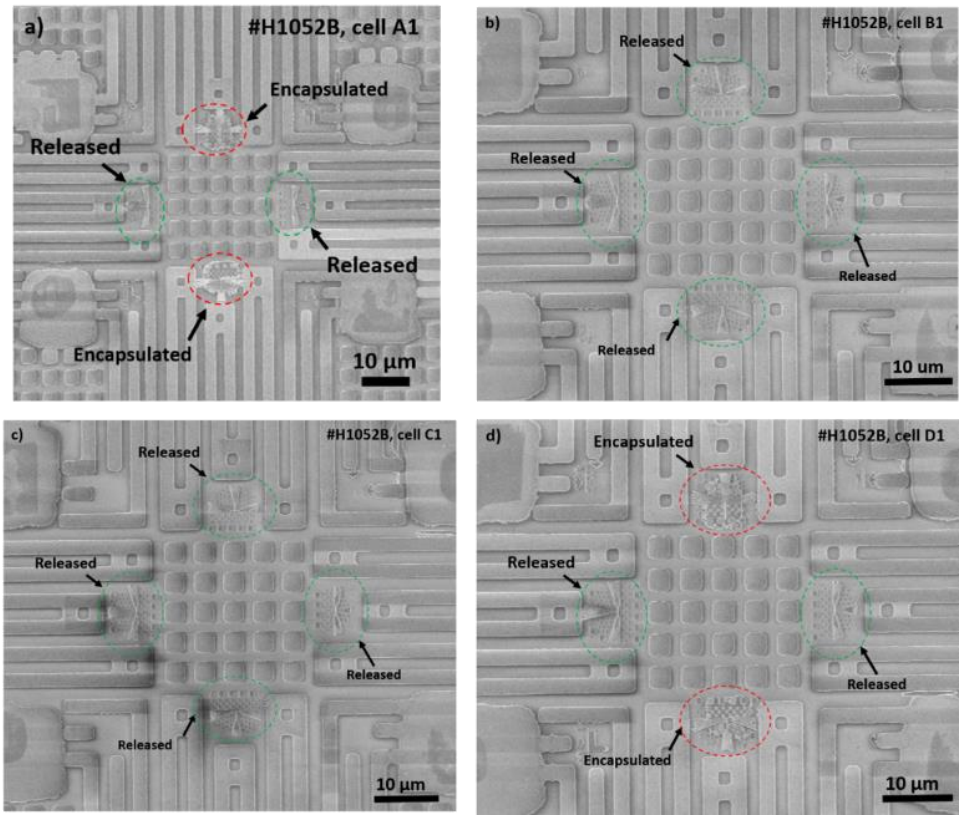

Figure E.26 Comparaison entre différentes cellules d'un même échantillon après le procédé de planarisation. a) Image SEM de la cellule A1. b) Image SEM de la cellule B1. c) Image SEM de la cellule C1. d) Image SEM de la cellule D1.

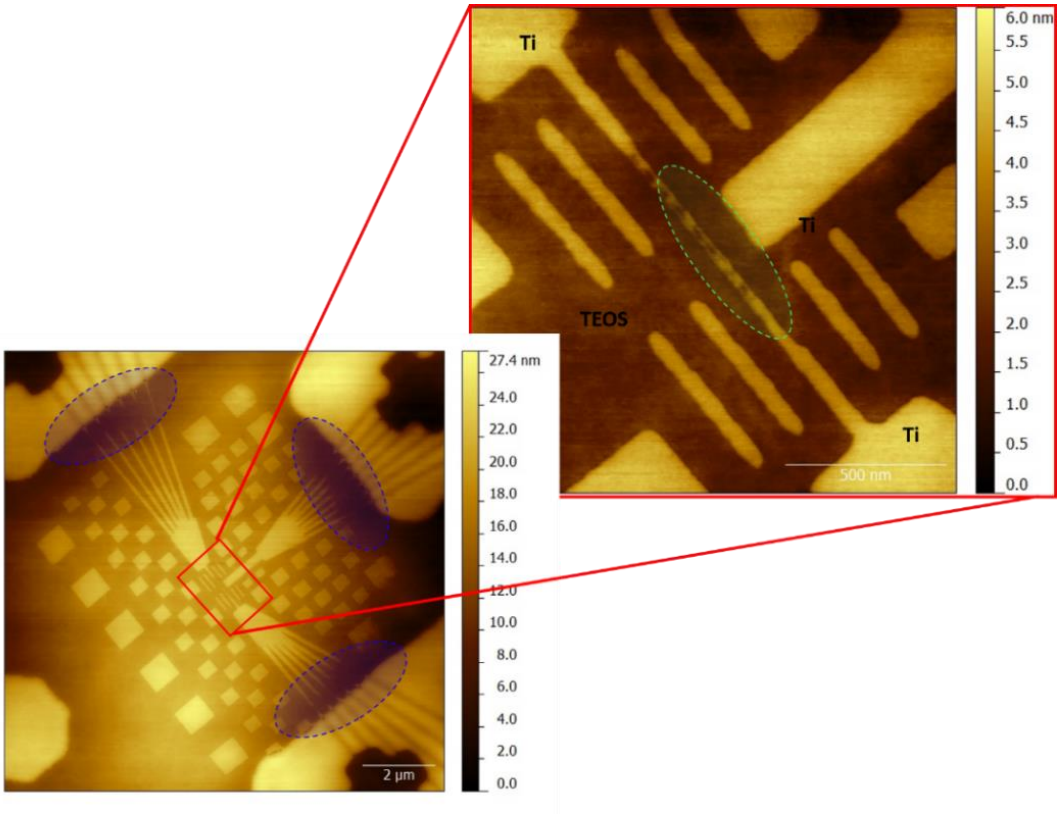

Figure E.27 Observation AFM d'un dispositif naofil. Les chemins d'amené nanométriques sont sur-polis conduisant à une perte de contact électrique. Des cavités sont observées au niveau du canal du nanodispostif.

Les masques de lithographie optique et électronique ont été optimisés pour optimiser l'étape de planarisation mécano-chimique et principalement les modifications suivantes ont été apportées :

- Rapprochement des électrodes micrométriques à 2µm de distance,
- Optimisation des structures sacrificielles nanométriques pour optimiser la planarisation,
- Optimisation de l'emplacement des dispositifs nanométriques (choix de régions ou la topographie initiale de la couche diélectrique supérieure du substrat CMOS est la plus planaire).

Le remplissage des tranchés a été optimisé en optant pour des tranchés gravés à flancs inclinés et en réduisant le taux de dépôt à 0.4 nm/min des premier 25 nm de la couche de titane plein plaque déposé par pulvérisation.

Les optimisations apportées au procédé ont permis d'obtenir une planarisation homogène des dispositifs, tel que vu sur la figure E.28 et E.29.

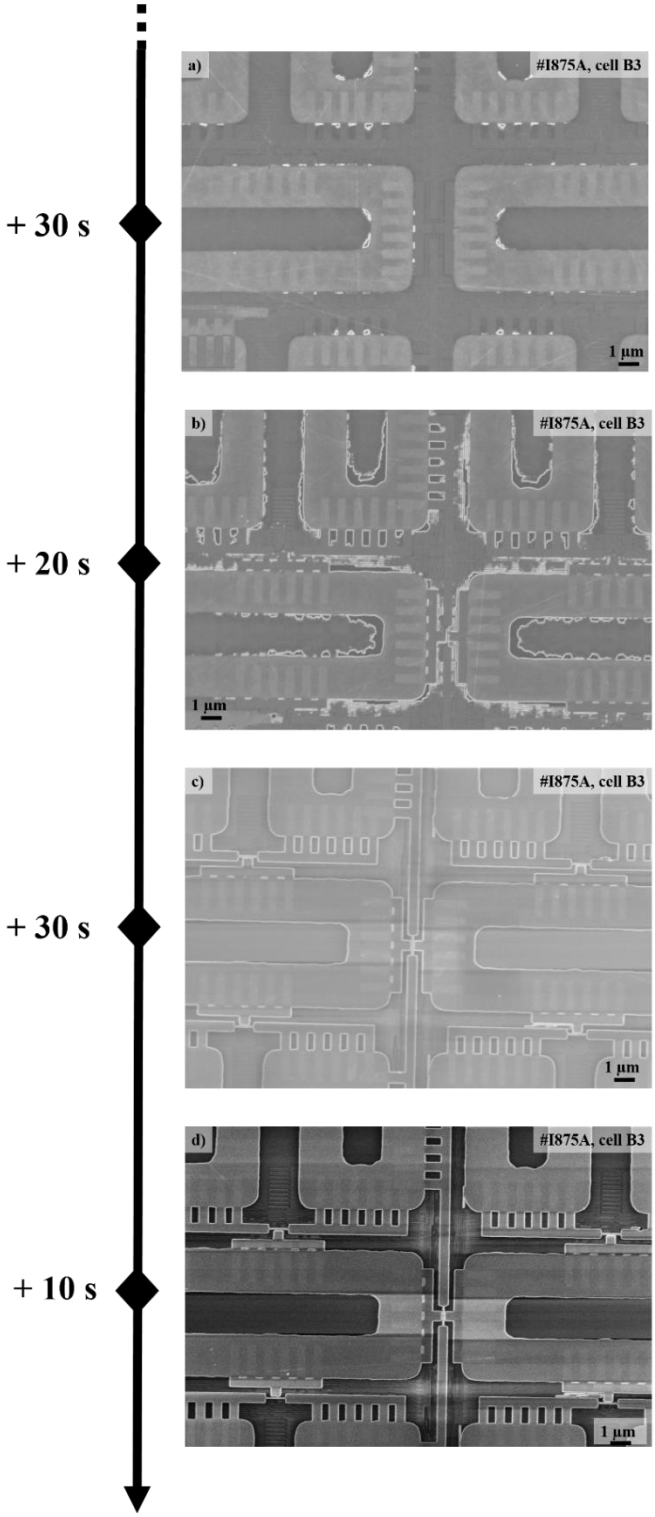

Figure E.28 Observation SEM d'une même cellule d'un échantillon structuré avec les masques de lithographie optimisés le long du procédé de planarisation.

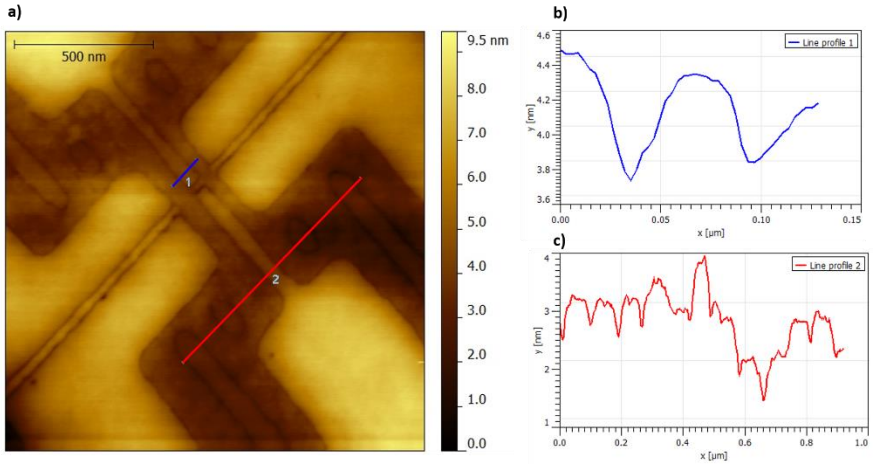

Figure E.29 a) Observation AFM d'un dispositif DG-SET, montrant les tracés extrait dans b) et c)

Le control du procédé de la planarisation et donc de l'épaisseur des structures planaires obtenues, pourrait être amélioré en optant pour l'incorporation de couches d'arrêt diélectrique comme le Si_3N_4. Il a été observé un vieillissement des jonctions tunnel en TiOx dû à la diffusion de l'oxygène de l'oxyde de Ti vers les terminaux de drain et source en Ti. Le Ti a été remplacé par le TiN déposé par ALD (pour Atomic Layer Deposition) comme métal pour la formation des électrodes de drain et source.

Les étapes de lithographie électroniques pourrait être remplacé par de la lithographie UV par immersion. Les outils de lithographie UV industriel permettent un alignement avec une erreur de quelque nm. Ceci permettrait de réduire la largeur de la grille latérale et par conséquent réduire considérablement sa contribution à la capacité totale de l'îlot. En termes de conception, la grille latérale (grille de contrôle) pourrait être remplacée par une grille inférieure ce qui permettrait une liberté dans le dimensionnement de la distance qui la sépare de l'îlot.

E.4.2 Caractérisation électrique des nanodispositfs

Des dispositifs de type nanofil et MIM (pour Metal Insulator Metal) en Ti encastrés dans la couche diélectrique placés à côté des dispositifs SET, dont la structure est illustrée dans les figures E.30 et E.31, avec la version initiale des masques de lithographie, ont été électriquement caractérisés pour estimer l'épaisseur des structures planaires fabriqués.

Figure E.30 Représentation schématique de la structure vue en coupe d'un nanofil en Ti encastré dans la couche diélectrique supérieure du substrat CMOS.

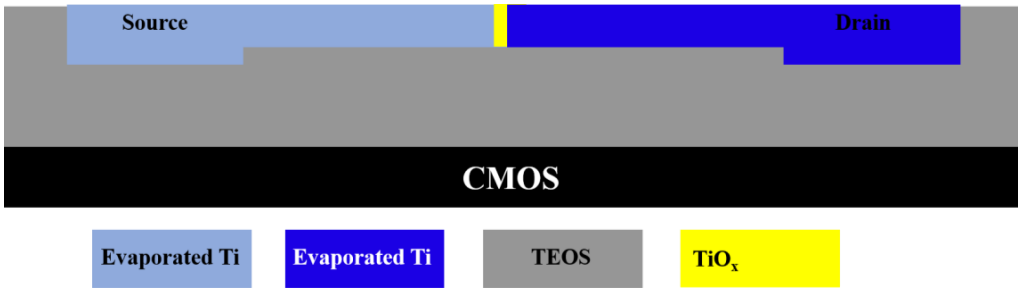

Figure E.31 Représentation schématique de la structure vue en coupe d'une avec une jonction tunnel en TiO_x encastré dans la couche diélectrique supérieure du substrat CMOS.

Une caractéristique $I-V$ typique réalisée en 4 points d'un nanofil de 20 nm de largeur est montré sur la figure E.32. La résistance extraite permet après soustraction des résistances des chemins d'amené micrométriques et nanométriques, d'estimer la résistivité du nanofil. L'épaisseur du nanofil est estimée à partir d'un abaque qui représente la résistivité en fonction de l'épaisseur. Cette méthode a été développée par Guilmain *et al* pour le control de l'épaisseur de nanofils métalliques réalisés par *nanodamascene*. La mesure de résistivité des nanofils est utilisée comme méthode de control du procédé de planarisation mécano-chimique.

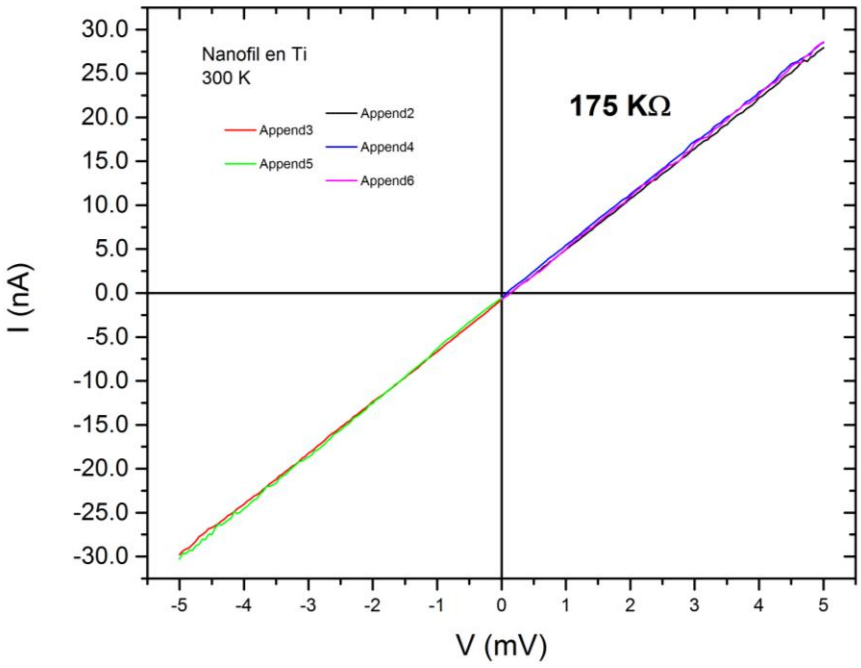

Figure E.32 Caractéristique $I-V$ typique d'un nanofil en Ti de 20 nm de largeur à 300 K.

La caractérisation électrique $I-V$ des dispositifs MIM permettent l'extraction des paramètres des jonctions tunnel tel que la hauteur de barrière, la masse effective et l'épaisseur. Une caractérisation $I-V$ typique d'une MIM, dont la structure est représentée dans la figure E.31 et ayant 4 nm de TiO_x comme diélectrique de jonction tunnel, est montré sur la figure E.33.

Connaissant les dimensions de la jonction tunnel (largeur, longueur et épaisseur), la masse effective, la constante diélectrique ainsi que la hauteur de barrière sont extraite en faisant concorder les caractéristiques $I-V$ simulées d'un modèle de MIM avec les courbes expérimentales. Le modèle prend en considération les mécanismes de conduction par émission thermoïonique, tunnel direct et tunnel de type Fowler-Nordheim. Le modèle développé par Droulers *et al.*[112], prend en compte l'effet de la déformation de la barrière par la force image.

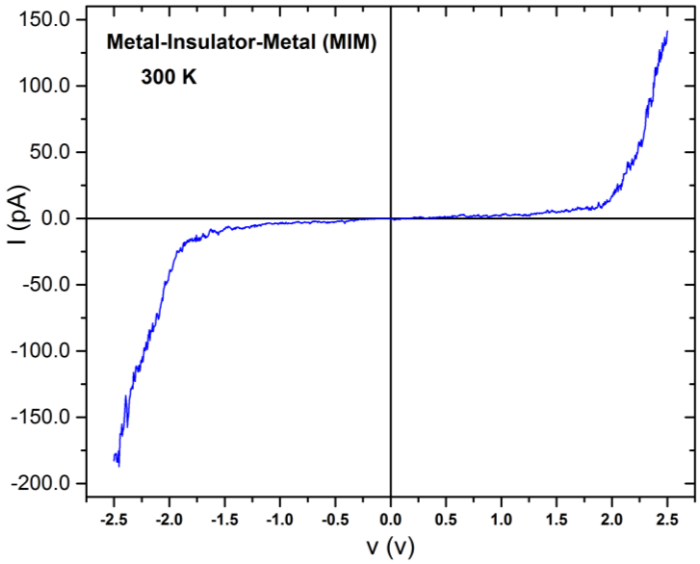

Figure E.33 Caractéristique $I-V$ typique d'une MIM ayant 4 nm de TiO_x comme diélectrique de jonction tunnel à 300 K.

Plus de 40 dispositifs SET ont été fabriqués avec la version initiale des masques de lithographie le et caractérisés électriquement. 20% seulement des dispositifs ont exhibé un une tension seuil de blocage de Coulomb (voir figure E.34) à 300 K. Cependant, il n'a été possible d'observer un effet de grille au niveau des caractérisations $I_{ds}\ versus\ V_{gs}$. Le reste des dispositifs correspond à des circuits ouverts ou des court-circuits (caractéristique $I_{ds}\ versus\ V_{ds}$ linéaire) tel que vu sur la figure E.35. Ceci est dû conséquence de la planarisation non homogène.

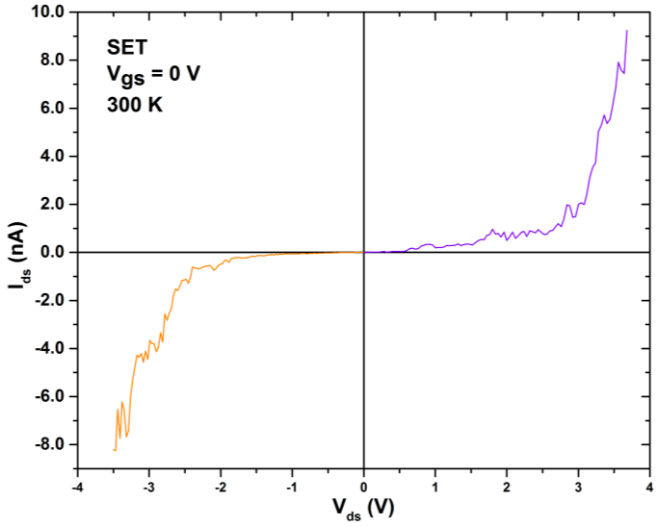

Figure E.34 Caractéristique $I_{ds}-V_{ds}$ d'un SET à $V_{gs}=0$ V et 300 K, montrant la tension seuil du blocage de Coulomb.

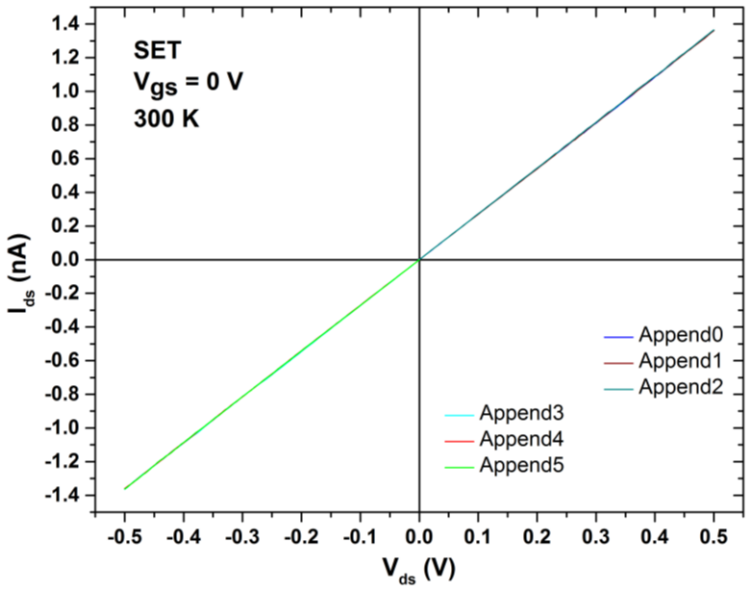

Figure E.35 Caractéristique $I_{ds} - V_{ds}$ d'un SET à $V_{gs} = 0$ V et 300 K ayant un comportement d'une résistance.

Les dispositifs fabriqués avec le jeu de masques de lithographie optique et électronique optimisés, ont permis d'obtenir des résultats très encourageant au niveau de la planarisation. Cependant il n'a été possible de procéder à la caractérisation électrique, car les échantillons ont été endommagés pendant les étapes de fabrication de passivation et formation des plots de contacts électriques.

E.5 Perspectives

La technologie FD-SOI est une plateforme très attractive pour l'intégration de capteurs de gaz, avec une haute densité d'intégration en comparaison à l'état de l'art actuel. La démonstration expérimentale de la détection de l'hydrogène avec un MOSFET FD-SOI fonctionnalisée avec du Pt serait le premier pas vers la détection de différents molécules en phase gazeuse ou même des molécules biochimique en phase liquide.

La technologie FD-SOI est une technologie mature et massivement déployé dans l'industrie des circuits intégrés. Ce type de transistors offre les avantages suivants :

- Les transistors issus de la technologie FD-SOI avancée sont des dispositifs ultra-basse consommation.

- L’énorme pouvoir amplification de ces transistors quand ils sont opérés en régime sous-le-seuil, fait d’eux des transducteurs ultrasensibles en configuration capteur de gaz à base d’un FET à double grilles
- La sensibilité accrue estimée des transducteurs de type MOSFET FD-SOI, permet la réduction de la température de chauffage du matériau sensible nécessaire à l’obtention du signal chimique, mais également la surface spécifique, permettant ainsi une réduction considérable du budget énergétique
- La technologie FD-SOI permet une très haute densité d’intégration.
- La plateforme FD-SOI permet l’intégration de capteurs de gaz avec des circuits CMOS, et par conséquent l’ajout de nouvelles fonctionnalités au puces CMOS

Tous ces avantages font des capteurs de gaz à base des DG-FET un candidat très attractif pour la future de la technologie de détection de gaz en termes de densité d’intégration, sensibilité et puissance consommée. Des capteurs de gaz à base de DG-FET ultra basse consommation intégré avec des circuits CMOS est d’un grand potentiel pour les systèmes électronique mobiles ou autonome. Ce type de systèmes, alimenté sur batterie ou potentiellement par récupération d’énergie présentent des exigences drastiques en terme de consommation d’énergie. Les DG-FET seraient bien placés pour trouver applications dans les systèmes de capteurs intégrés sans fil ou mobiles, l’électronique grand public, la domotique, etc. Par exemple les cellulaires intelligents incorpore déjà des caméras, des microphones, des accéléromètres, des gyroscopes, etc. l’intégration de capteur de gaz est sans doute la prochaine étape dans la diversification des fonctionnalités.

La haute densité d’intégration de la technologie FD-SOI pourrait trouver application dans les systèmes de nez électronique sur puce. L’intégration de matrices de capteurs de gaz avec les circuits logiques CMOS sur la même puce est possible avec la technologie FD-SOI

The high integration density of FD-SOI technology may find application in on chip e-nose systems. Integration of sensors matrix with CMOS logic circuits in the same chip is possible with the FD-SOI FET technology. Ceci est pertinent dans le domaine de la bio mimique. Les nez électroniques sur puce seraient les prémices de l’odorat artificiel. La technologie des capteurs de gaz à base des transistors FD-SOI pourrait accélérer cette révolution.

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FOLIO ADMINISTRATIF

THESE DE L'UNIVERSITE DE LYON OPEREE AU SEIN DE L'INSA LYON

NOM : Ayadi LA DATE de SOUTENANCE : 16/12/2016

Prénom : Yosri

TITRE : INTÉGRATION 3D DE DISPOSITIFS SET DANS LE BACK-END-OF-LINE EN TECHNOLOGIES CMOS 28 nm POUR LE DÉVELOPPEMENT DE CAPTEURS ULTRA BASSE CONSOMMATION

3D INTEGRATION OF SINGLE ELECRTON TRANSISTORS IN THE BACK-END-OF-LINE OF 28 nm CMOS TECHNOOGY FOR THE DEVELOPMENT OF ULTRA-LOW POWER SENSORS

NATURE : Doctorat Numéro d'ordre : 2016LYSEI155

Ecole doctorale : Électronique, électrotechnique, Automatique de Lyon

Spécialité : Électronique, micro et nanoélectronique, optique et laser

RESUME :

La forte demande et le besoin d'intégration hétérogène de nouvelles fonctionnalités dans les systèmes mobiles et autonomes, tels que les mémoires, capteurs, et interfaces de communication doit prendre en compte les problématiques d'hétérogénéité, de consommation d'énergie et de dissipation de chaleur.
Les systèmes mobiles intelligents sont déjà dotés de plusieurs composants de type capteur comme les accéléromètres, les thermomètres et les détecteurs infrarouge. Cependant, jusqu'à aujourd'hui l'intégration de capteurs chimiques dans des systèmes compacts sur puce reste limitée pour des raisons de consommation d'énergie et dissipation de chaleur principalement. La technologie actuelle et fiable des capteurs de gaz, les résistors à base d'oxyde métallique et les MOSFETs (Metal Oxide Semiconductor- Field Effect Transistors) catalytiques sont opérés à de hautes températures de 200–500 °C et 140–200 °C, respectivement.
Les transistors à effet de champ à grille suspendu (SG-FETs pour Suspended Gate-Field Effect Transistors) offrent l'avantage d'être sensibles aux molécules gazeuses adsorbées aussi bien par chemisorption que par physisorption, et sont opérés à température ambiante ou légèrement au-dessus. Cependant l'intégration de ce type de composant est problématique due au besoin d'implémenter une grille suspendue et l'élargissement de la largeur du canal pour compenser la détérioration de la transconductance due à la faible capacité à travers le gap d'air.
Les transistors à double grilles sont d'un grand intérêt pour les applications de détection de gaz, car une des deux grilles est fonctionnalisée et permet de coupler capacitivement au canal les charges induites par l'adsorption des molécules gazeuses cibles, et l'autre grille est utilisée pour le contrôle du point d'opération du transistor sans avoir besoin d'une structure suspendue.
Les transistors monoélectroniques (les SETs pour Single Electron Transistors) présentent une solution très prometteuse grâce à leur faible puissance liée à leur principe de fonctionnement basé sur le transport d'un nombre réduit d'électrons et leur faible niveau de courant.
Le travail présenté dans cette thèse fut donc concentré sur la démonstration de l'intégration 3D monolithique de SETs sur un substrat de technologie CMOS (Complementary Metal Oxide Semiconductor) pour la réalisation de la fonction capteurs de gaz très sensible et ultra basse consommation d'énergie. L'approche proposée consiste à l'intégration de SETs métalliques à double grilles dans l'unité de fabrication finale BEOL (Back-End-Of-Line) d'une technologie CMOS à l'aide du procédé nanodamascene. Le système sur puce profitera de la très élevée sensibilité à la charge électrique du transistor monoélectronique, ainsi que le traitement de signal et des données à haute vitesse en utilisant une technologie de pointe CMOS disponible.
Les MOSFETs issus de la technologie FD-SOI (Fully Depleted-Silicon On Insulator) sont une solution très attractive à cause de leur pouvoir d'amplification du signal quand ils sont opérés dans le régime sous-le-seuil. Ces dispositifs permettent une très haute densité d'intégration due à leurs dimensions nanométriques et sont une technologie bien

mature et modélisée. Ce travail se concentre sur le développement d'un procédé de fonctionnalisation d'un MOSFET FD-SOI comme démonstration du concept du capteur de gaz à base de transistor à double grilles.
La sonde Kelvin a été la technique privilégiée pour la caractérisation des matériaux sensibles par le biais de mesure de la variation du travail de sortie induite par l'adsorption de molécules de gaz. Dans ce travail, une technique de caractérisation des matériaux sensibles alternative basée sur la mesure de la charge de surface est discutée.
Pour augmenter la surface spécifique de l'électrode sensible, un nouveau concept de texturation de surface est présenté. Le procédé est basé sur le dépôt de réseaux de nanotubes de carbone multi-parois par pulvérisation d'une suspension de ces nanotubes. Les réseaux déposés servent de «squelettes» pour le matériau sensible.
L'objectif principal de cette thèse de doctorat peut être divisé en 4 parties : (1) la modélisation et simulation de la réponse d'un capteur de gaz à base de SET à double grilles ou d'un MOSFET FD-SOI, et l'estimation de la sensibilité ainsi que la puissance consommée; (2) la caractérisation de la sensibilité du Pt comme couche sensible pour la détection du H2 par la technique de mesure de charge de surface, et le développement du procédé de texturation de surface de la grille fonctionnalisée avec les réseaux de nanotubes de carbone; (3) le développement et l'optimisation du procédé de fabrication des SETs à double grilles dans l'entité BEOL d'un substrat CMOS; et (4) la fonctionnalisation d'un MOSFET FD-SOI avec du Pt pour réaliser la fonction de capteur de H2.

MOTS-CLÉS :

Transistors monoélectroniques, Intégration 3D monolithique, Capteur de gaz à base de FET, Capteur de gaz, Détection du dihydrogène, Texturation de surface de la couche sensible, Réseaux de MW-CNTs, Ultra-basse consommation, FDSOI.

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Composition du jury :

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M. Abdelghani, Adnane	Pr des universités	INSAT	Rapporteur
M. Monfray, Stéphane	Ing. Recherche	STmicroelectronics	Examinateur
Mme Ionica, Irina	Maître de Conférences	Université Grenoble Alpes	Examinatrice
M. Ecoffey, Serge	Pr Associé	Université de Sherbrooke	Invité
M. Souifi, Abdelkader	Pr des universités	INSA de Lyon	Co-directeur de thèse
M. Drouin, Dominique	Pr des universités	Université de Sherbrooke	Co-directeur de thèse