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Hadhemi Lakhdhar

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POUR OBTENIR LE GRADE DE

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L'UNIVERSITÉ DE BORDEAUX

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Par Hadhemi LAKHDHAR

**Reliability assessment of GaN HEMTs on Si substrate with ultra-short gate
dedicated to power applications at frequency above 40 GHz**

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Soutenue le 20/12/2017

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Abstract : Step-stress experiments are performed to investigate reliability assessment of ultra-short gate AlGaIn/GaN high electron mobility transistor (HEMT) on Si substrate. A methodology based on a sequence of step stress tests has been defined for in-situ diagnosis of a permanent degradation and of a degradation which is identified by a drain current transient occurring during each step of the aging sequence. The same stress conditions were applied on HEMTs with different geometries. It is found no evolution of the drain current during non-stressful steps. The value of the critical degradation voltage beyond which the stress drain current starts to decrease significantly is also found dependent on the stress bias conditions, the gate-drain distance and the gate length. Moreover, the safe operating area of this technology has been determined.

Keywords : AlGaIn/GaN HEMT, ultra-short gate, step stress, robustness, degradation, safe operating area (SOA)

Résumé : Des tests de vieillissement accéléré ont été effectués pour évaluer la robustesse des transistors HEMTs en AlGaIn/GaN à grille ultra-courte sur Si. Une méthodologie basée sur une séquence d'essais de vieillissement a été définie pour établir le diagnostic in-situ d'une dégradation statique et permanente et d'une dégradation qui se traduit par un transitoire de courant de drain au cours du chaque palier de la séquence de vieillissement. La valeur de la tension critique de dégradation à partir de laquelle le courant de drain commence à diminuer de façon significative dépend des conditions de polarisation du vieillissement, de la distance grille-drain et de la longueur de grille. De plus, l'aire de sécurité de fonctionnement de cette technologie a été déterminée.

Mots clés : HEMT AlGaIn / GaN, grille ultra-courte, vieillissement accéléré, robustesse, dégradation, aire de sécurité de fonctionnement (SOA)

Dedicated to my parents, my sister, my beloved husband and my angel 'Layane' for their love and constant support. May they find the sign of my deepest gratitude and limitless acknowledgement to their love and support that made my sun shine.

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Introduction

The last century has seen a tremendous evolution in the fields of science and technology linked to all aspects of our lives such as telecommunications, automotive, entertainment, medical matters, comfort and safety, through the revolution of micro- and nano-electronic devices. In particular, a quasi-exponential semiconductor progression and an associated miniaturization were observed.

One of the key technologies making this evolution possible was the Gallium Nitride (GaN) based High Electron Mobility Transistor (HEMT), which was first demonstrated in 1993 by Khan, exhibiting impressive attributes and outstanding potentials and performances, compared with counterparts based on other materials, in term of high power, high frequency and high voltage operation in microwave and millimeter wave range.

This is due to the extraordinary material properties of GaN material such as large band gap (3.4 eV at room temperature), high breakdown field (3.3 MV/cm), high saturation electron velocity (2.7×10^7 cm/s), high electron mobility (900 cm²/V.s), high melting point, relatively low dielectric constant and the interesting features of the AlGaN/GaN heterostructure such as high density of the two dimensional electron gas (2-DEG). However, HEMT reliability is still under investigation, partly due to the continuous evolution of the process and technologies, and partly due to the lack of technological solutions of failure. Hence, before large-scale commercialization of GaN HEMTs, reliability has to be fully demonstrated and more investigation is needed to improve device technology, epitaxy, design and other performance limiting factors.

Different types of semiconductor substrates have been considered for their thermal properties, large area availability and cost effectiveness. In this frame, the successful growth of GaN on Silicon (Si) attracts the industry because of the availability of large high resistive silicon wafers at low cost.

Over the last several years, was observed a continuous trend to increase power density and minimize the footprints of the device. In particular, improved frequency performance of GaN HEMTs is achieved through downscaling of the gate length to sub-100 nm in conjunction with state-of-the-art technologies.

In this context, this thesis will focus on reliability assessment of GaN HEMTs on Si (III) substrate

with ultra-short gate dedicated to power applications at frequency above 40 GHz. This work was carried out between the Integration of Materials to Systems (IMS) laboratory, University of Bordeaux and the Institute of Electronics, Microelectronics and Nanotechnology (IEMN), University of Lille.

This manuscript is shared into three chapters as follows:

Chapter 1 provides a background description about GaN HEMTs. The crystal structure and the basic physical properties of GaN are reviewed. Then, the basic concepts and the operation principles of GaN based HEMTs are presented followed by a review of the applications well suited for GaN based devices. The reliability issues of GaN based devices including indicators, methods and tools of reliability assessment are discussed. Then, degradation mechanisms and trapping effects are reviewed. Finally, a state of the art of the reliability of HEMT with ultra-short gate is presented.

Chapter 2 summarizes the first contribution of this work. Devices grown by metal organic chemical vapor deposition (MOCVD) and devices grown using Molecular Beam Epitaxy (MBE) technique are introduced as well as their technological process steps. Then, an electrical characterization campaign is performed including DC characterization, RF characterization and parameters extraction. A particular attention is given to the impact of device geometry on static and microwave performances for both technologies and to the on-wafer dispersion of their electrical parameters.

Chapter 3 summarizes the second contribution of this work. In order to perform a robustness assessment of short gate MOCVD GaN HEMTs on Si (III) substrate, a methodology is defined for in-situ diagnosis of permanent degradation. This study aims at defining the safe operating DC conditions. Then, the results of DC step stress aging tests carried out on HEMTs are detailed and discussed, including the identification of degradation signatures and the determination of the maximum values of DC bias voltages that devices can withstand. A critical degradation drain-source voltage is defined and its variation with the device geometry is studied. The last part of this chapter is devoted to the analysis of TLMs after aging tests, in order to give an insight about the physical impact of the electrical stress.

Finally, conclusions for all the topics presented in this thesis are drawn, and a discussion of several possible ways for future work is presented.

Chapter 1

Gallium–Nitride HEMTs

1.1 Introduction

This chapter describes a background information about AlGaN / GaN high electron mobility transistors (HEMTs).

Section 1.2 outlines the crystal structure and the basic physical properties of Gallium Nitride (GaN) as a semiconductor material, its use in the design of high electron mobility transistors and deals with its polarization properties that play an important role in the formation of the two dimensional electron gas (2DEG) at the AlGaN/GaN interface. Section 1.3 introduces the basic concepts and the operation principles of HEMTs based on AlGaN/GaN heterostructure. This will be followed by a review of the applications well suited for GaN based devices in section 1.4. Section 1.5 discusses the reliability issues of GaN based devices including indicators, methods and tools of reliability assessment. Then, degradation mechanisms and trapping effects are detailed in section 1.6. A particular attention will be given to the GaN HEMT with ultra-short gate.

1.2 GaN: material system

Gallium Nitride wide bandgap semiconductors have attracted a great level of attention for many years, thanks to their several material properties making them ideally suited for high power, high frequency applications. These properties include:

- Energy gap of 3.4 eV [1] over three times that of Si. This large energy gap gives it the ability to withstand high electric fields (GaN has a breakdown electric field of 3.3 MV/cm), high operating temperatures, and enables high power density applications extensively covering both commercial and military markets [2-4].
- High electron mobility ($900 \text{ cm}^2/\text{V.s}$ in GaN) coupled with the ability to withstand high

voltages permits reaching for higher saturation velocities (2.7×10^7 cm/s) and higher operating frequency [1].

- High mechanical/thermal stability combined with good thermal conductivity for dissipating heat essentially for devices on SiC substrate, so devices can operate at higher temperature and power.

Table 1.1 compares the basic material properties of GaN with other well-known semiconductors.

Table 1.1: Physical properties of different semiconductors (GaN and other competitors) considered for high-voltage applications [1]

Material properties	Si	6H-SiC	GaAs	GaN
Bandgap energy (eV)	1.1	3.0	1.43	3.4
Electron mobility ($cm^2V^{-1}s^{-1}$)	1400	400	8500	900
Saturated (peak) drift velocity (10^7 cm/s)	1.0	2.0	2.1	2.7
Breakdown electric field (MV/cm)	0.3	2.4	0.4	3.3
Thermal conductivity ($Wcm^{-1}K^{-1}$)	1.5	4.5	0.5	1.3
Relative dielectric constant	11.8	9.7 (static) 6.7 (HF)	12.9 (static) 10.9 (HF)	9.5 (static) 5.3 (HF)

Figure 1.1 shows a comparison between GaN, Si and GaAs advantages for RF and power supply circuits. It can be shown that GaN is the key material for the next generation of high-frequency, high-power, high-voltage, high-temperature and low-loss operating specifications transistors [1] and thus an adequate and outstanding candidate for high performance HEMT.

There are two important figures of merit leading to rate the performance of devices made of different materials:

- Johnson's figure of merit (JFOM), which describes a device ability to operate at both a high power and high frequency. It is determined by the product of electric field breakdown (E_C) and electron saturation velocity (V_S) as shown in the following formula [6].

$$JFOM = \frac{E_C V_S}{2\pi} \quad (1.1)$$

- Baliga's figure of merit (BFOM), which describes the resistive losses of a device [7] It is given by:

$$BFOM = \epsilon\mu E_C^3 \quad (1.2)$$

Here, ϵ is the dielectric constant of the material, μ is the carrier mobility and E_C is the critical breakdown field of the semiconductor.

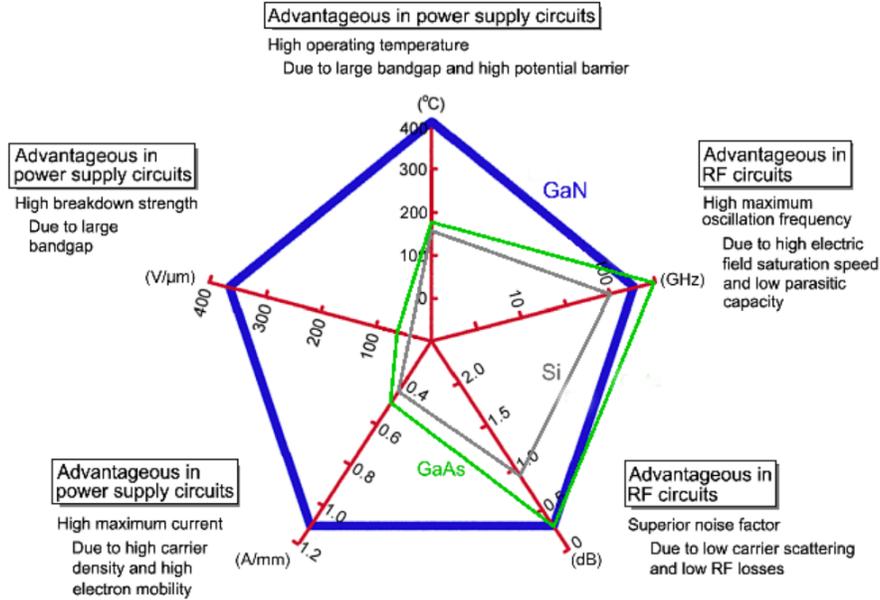


Figure 1.1: GaN material compared to Si and GaAs [5]

Table 1.2 shows a comparison of GaN with conventional semiconductor materials. The figures of merit are normalized in reference to those calculated for silicon (Si) material. The highest values possible are desirable.

Table 1.2: Comparison of Johnson and Baliga figures of merit for Si, GaAs and GaN materials [8]

Material	$\frac{JFOM}{JFOM(Si)}$	$\frac{BFOM}{BFOM(Si)}$
Si	1	1
GaAs	1.8	14.8
GaN	215.1	186.7

1.2.1 Crystal structure

The group of III-nitride (AlN, GaN and InN), can crystallize depending on the growth conditions and crystallographic orientation of the substrate in three crystal structures: wurtzite (WZ) according to a hexagonal Bravais lattice [9], zinc-blende (ZB) with a cubic shaped lattice and rock-salt (RS) crystal structures [10]. The main focus of our work is based on GaN, which usually tends to synthesized in the hexagonal wurtzite crystal structure.

The ZB structure has several advantages for device applications, such as smaller band-gap and higher carrier mobility [11]. It can be used for applications that need high cut-off frequency and

this is due to the higher electron drift mobility ($1300 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at 300 K) and lower effective mass compared to WZ structure [12]. Although, it is the thermodynamically metastable polytype of GaN.

Regarding the wurtzite structure, it is the most stable structure at ambient temperature and pressure [13,14] with the lowest energy in the stress-free state [15,16]. In addition to piezoelectric effects that have a large impact on the charge density and electric field distribution within the material [17,18], wurtzite structure also possess a very large spontaneous polarization field due to the ionicity of the covalent bonds and the low inversion symmetry of wurtzites (the highly electronegative nitrogen atoms and the less electronegative gallium atoms) which can be exploited in creating high-density 2DEG (two dimensional electron gas) at III-N heterointerfaces [19]. The polarization effects and the 2DEG formation will be discussed in details in the following sections.

Since polarization is a bulk property [20], the polarity of the crystal does not depend on the surface layer but only on the position of the bonds along the $[0001]$ axis. Depending on the growth method the polarity of GaN crystal may be either a Ga-face polarity (correspond to (0001) crystalline face) when the N-Ga bond points from the substrate to the surface or an N-face polarity (correspond to $(000\bar{1})$ crystalline faces) when the N-Ga bond points from the surface to the substrate [21] as shown in Figure 1.2. This determines the polarity of the spontaneous electric field and affect both device technology and performance [22].

N-face crystals are chemically active which enables wet-chemical etching of the material. They suffer from a very rough surface morphology and high background doping concentration.

Ga-face crystals have much smoother surface morphology, lower background doping concentration, higher electron transport properties and are preferred for device operation [23].

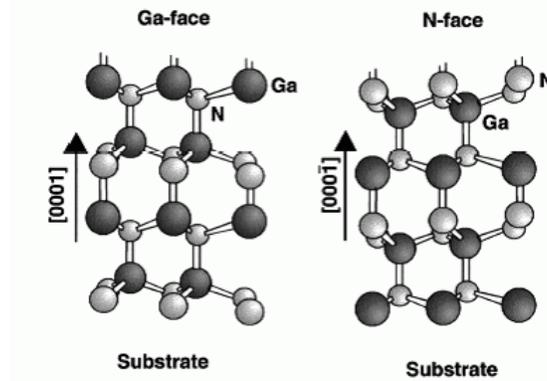


Figure 1.2: Hexagonal wurtzite crystal GaN: Ga-face polarity (left) and N-face polarity (right)

Sufficiently high hydrostatic pressure may cause the WZ structure to collapse into a denser rock salt (RS) phase [24-26]. A phase transition from WZ to a body-centered-tetragonal structure

phase (TS) has been shown to occur in [0001] oriented GaN nanowires during tensile loading [27,28]. It was reported that the competition between phonon and elastic instabilities plays an important role in the reconstructive phase transition from WZ to RS structure [29]. The RS structure is typical of ionic bonds [30] and presents less interest for device applications.

1.2.2 Polarization effect

The crystal structure of III-nitrides results in spontaneous polarization (P_{SP}) which appears in both layers [31,32]. This is due to the strong electro negativity difference from the nitrogen and the gallium.

The second polarization field so-called strain-induced or piezoelectric polarization (P_{PE}) appears on GaN, AlN or AlGaN when the material is strained.

The total polarization is therefore the sum of two contributions; the spontaneous polarization existing at equilibrium and the piezoelectric polarization existing under external constraint, as illustrated in 1.3.

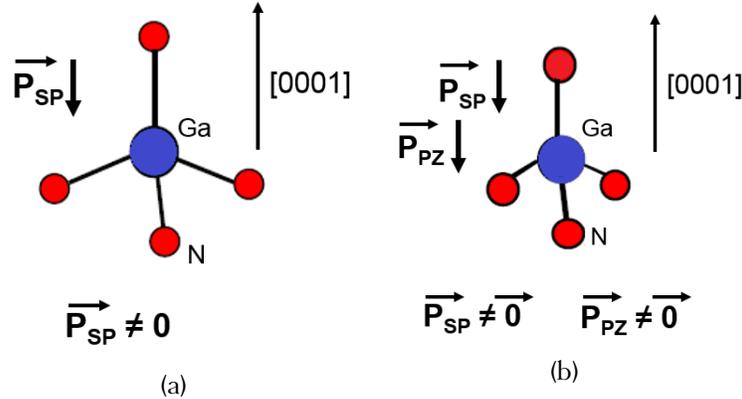


Figure 1.3: (a) Spontaneous polarization: GaN wurtzite structure at equilibrium, (b) piezoelectric polarization: GaN wurtzite structure under external constraint

The piezoelectric polarization P_{PE} can be expressed as follows [21]:

$$P_{PE} = 2 \left(\frac{a - a_0}{a_0} \right) \left(e_{13} - e_{33} \frac{C_{13}}{C_{33}} \right) \quad (1.3)$$

Where $\frac{a - a_0}{a_0}$ term represents the in-plane strain,

a is the resulted lattice constant induced by the applied strain,

a_0 is the intrinsic lattice constant of the material,

e_{13} , e_{33} are the piezoelectric coefficients, and

C_{13} and C_{33} are elastic constants.

The direction of the piezoelectric polarization depends on the sign of $(a - a_0)$. P_{PE} is always negative for layers under tensile stress ($a > a_0$) and positive for layers under compressive stress ($a < a_0$). Spontaneous and piezoelectric polarizations are parallel to each other for layers under tensile stress, and are anti-parallel for layers under compressive stress.

Spontaneous and piezoelectric polarization effects are used to increase carrier concentration of GaN-based HEMTs.

1.3 GaN High Electron Mobility Transistors

The high electron mobility transistor (HEMT) is a field effect transistor incorporating a junction between two materials having different band-gap energies. Its invention is attributed to Takashi Mimura at Fujitsu laboratories in Japan in 1980 [33] using an AlGaAs/GaAs device. Alongside Fujitsu a number of other research facilities joined on the further development of the new structures: Bell Labs, Thomson CSF in France, Honeywell and IBM [34].

The GaN material demonstrated more advantages over GaAs material. The first reported GaN HEMT dates back to 1993 by Kahn [35] but these devices did not reach the commercial market until 2006 [36]. Developments have been going on, mainly driven by a growing demand for high power communication systems at microwave frequencies.

Based on wide bandgap material, GaN-based high-electron-mobility transistors (HEMTs) are getting in the focus of research activities in the recent years and are one of the most promising devices for high frequency and high power applications.

1.3.1 Epitaxial structure

Figure 1.4 shows a cross section of AlGaIn/GaN HEMT. Similar to a traditional FET, it comprised the drain and the source contacts to achieve ohmic contacts and a gate to generate the Schottky barrier.

In the following section, we review the structure of AlGaIn/GaN HEMT based on multiple epilayers grown onto each other:

- Substrate: it is used as the base for the growing process. HEMTs are usually grown on Silicon [37, 38], sapphire [39, 40] or Silicon Carbide [41]. As for GaN substrate, it is very pricey and very difficult to synthesize (GaN is naturally n-type then it is indeed necessary to perform a p-type doping, difficult to perform on GaN, in order to make the substrate resistive). The choice of the substrate depends on the available size, cost, thermal conductivity, lattice mismatch constant, heat expansion and application of the GaN based device. Figure 1.5 shows a comparison between these substrates [42]. The successful growth of GaN on Silicon attracts the industry because of the

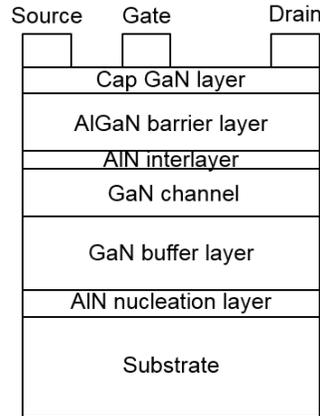


Figure 1.4: Cross section of AlGaN/GaN HEMT

availability of large high resistive silicon wafers at low cost. Currently the best results, which are obtained on SiC substrates, are likely reproduced by using Silicon substrates.

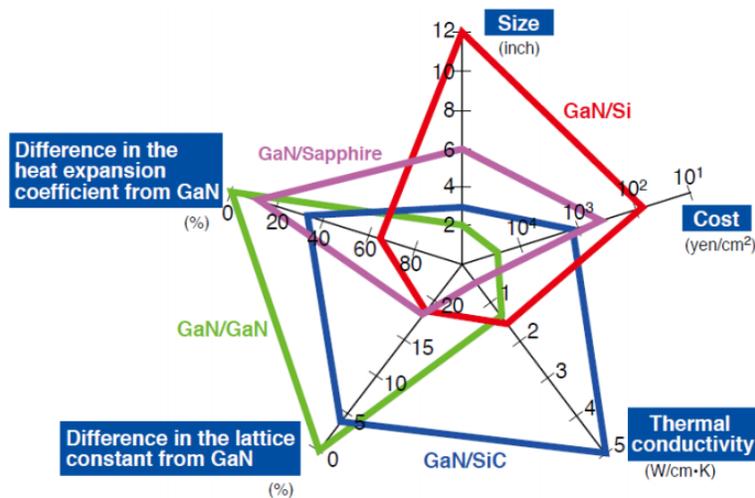


Figure 1.5: Comparison between different substrates on which GaN can be grown [42]

- GaN buffer layer: it is unintentionally doped and composed of the wide band-gap material. The material quality of this layer is very crucial especially because of traps and deep levels that degrade the device RF performance. It can be improved by the incorporation of acceptor type dopant such as iron or carbon to compensate for the residual N-type doping of gallium nitride [43]. The piezoelectric polarization is not present in the GaN buffer layer due to its relaxed state and thickness (0.5 to 4 μm).

- AlGaN barrier: it is an unintentionally doped layer formed by the $Al_xGa_{1-x}N$ wide bandgap material, where x is the aluminum mole fraction. This layer forms the Schottky contact with the gate metal contact and supplies the electrons for current conduction in the channel. The thickness (3 to 30 nm) and alloy composition of this layer are crucial to determine the mechanical stress and hence the piezoelectric polarization in the structure.

AlGaN/GaN HEMT may be subject to parasitic phenomena that will prevent it from functioning under optimal conditions. Thus, the following layers are generally added to the previously described structure.

- Nucleation layer: it is an intermediate layer between the GaN layer and the substrate. It permits to reduce the tensile strain of GaN due to the lattice mismatch that favors the cracks formation.

- AlN interlayer: so-called AlN spacer layer is used to enhance and improve the 2DEG density, the mobility and the drain current [44].

- GaN cap layer: permits to protect the active layer, and to reduce the contact and channel resistance in order to limit the leakage current.

The different epilayers growth is principally achieved via one of two different methods, Metal-organic Chemical Vapor Deposition (MOCVD) or Molecular Beam Epitaxy (MBE). In this section, the growth techniques are discussed in order to understand the differences in the fabricated samples that were used in the experiments within the framework of this thesis (AlGaN/GaN MOCVD and MBE technologies), and also to compare them in terms of reliability.

MOCVD growth of Gallium Nitride based materials involves a dynamic flow in which gaseous reactants pass over a heated substrate and react chemically to form a semiconductor layer. It is fast, at a rate of a few micrometers per hour, with multi-wafer capability easy to integrate, and performed at much higher temperatures (>1000 °C) than MBE growth (700 °C) and has a higher growth rate than MBE [45]. The growth rate of III-N MBE is $0.5 \sim 1\mu/h$ [46].

Figure 1.6 shows Schematic view of the MOCVD system.

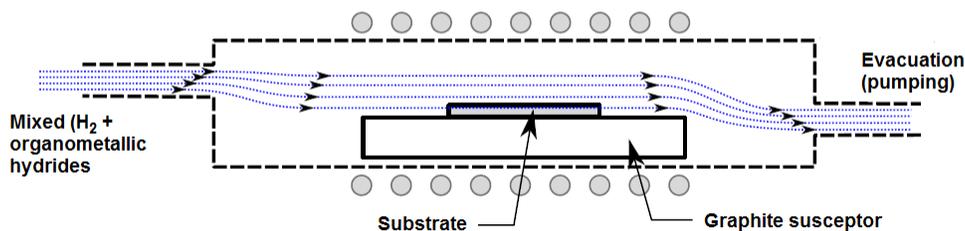


Figure 1.6: Schematic view of the MOCVD system [47]

MBE is another attractive growth method which occurs via reactions between thermal-energy molecular, atomic, or ionized beams of the constituent elements on a heated substrate in an ultrahigh vacuum. MBE allows precise definition of interfaces, the increased polarity of the interfaces, low point defect concentration, very low carbon and hydrogen impurity concentrations and better transport properties compared to MOCVD growth. Figure 1.7 shows a schematic view of the MBE system.

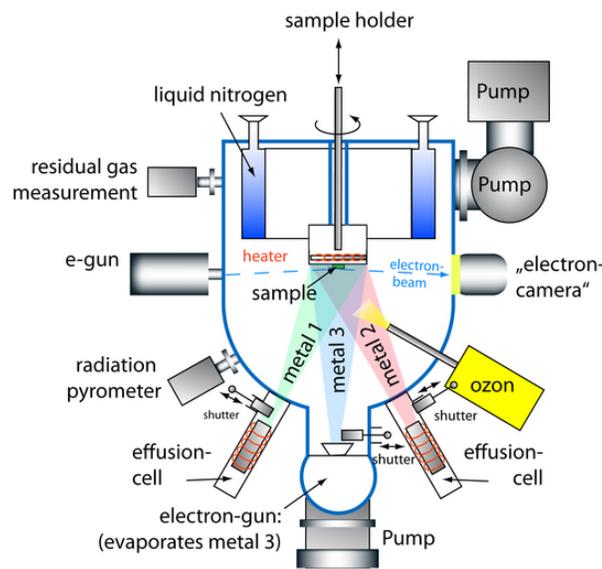


Figure 1.7: Schematic view of the MBE system [48]

Table 1.3 shows a comparison between MOCVD and MBE growth

1.3.2 AlGa_N / Ga_N heterostructure

AlGa_N / Ga_N heterostructure is a junction between AlGa_N and Ga_N layers having different energy band gap. In Ga-face heterostructure with AlGa_N layer under tensile strain, the piezoelectric polarization of AlGa_N layer is of the same polarity as the spontaneous polarization as shown in Figure 1.8.

The AlGa_N/Ga_N interface polarization $P_{(AlGa_N/Ga_N)}$ is given by the following equation:

$$P_{AlGa_N/Ga_N} = P_{SP(AlGa_N)} + P_{PE(AlGa_N)} + P_{SP(Ga_N)} \quad (1.4)$$

The AlGa_N/Ga_N heterostructure at thermodynamic equilibrium must have constant Fermi level. The difference of the two materials electron affinities and the continuity of the vacuum level induce discontinuities of conduction and valence bands at the interface between the two materials.

Table 1.3: Comparison between MOCVD and MBE growth

Growth techniques	Strengths	Weaknesses
MOCVD	High growth rate for bulk layers / Most flexible / Large scale production / Abrupt interface simple reactor / High purity / Selective in-situ monitoring / High grown layer quality / High throughput	High Process temperature / Complicated process / H pollution / Possible roughness at interfaces
MBE	Simple Process / Uniform / Free of an oxide layer / Good control of layer thickness and composition / Abrupt interface In-situ monitoring / substrate temperature is not high	Expensive / Low growth rate / Epitaxial growth under ultra-high vacuum conditions / Low throughput

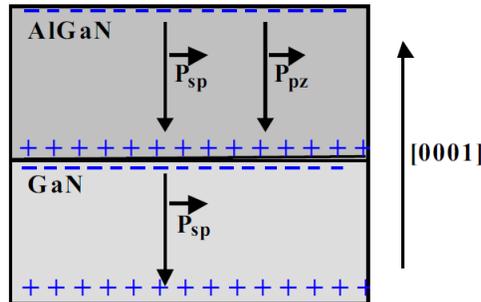


Figure 1.8: Spontaneous and piezoelectric polarizations and charges distribution in the AlGaIn/GaN heterostructure Ga-face

Electrons are confined in the triangular potential in discrete quantum state, which constitutes a conduction channel. The two-dimensional channel ensuring the conduction of the current, by means of the effect of an electric field induced by an excitation voltage. The confinement of electrons in a quantum well confers them a high mobility, because of their separation from fixed charges resulting from piezoelectric and spontaneous polarizations. The heterostructures described above are provided with two ohmic, drain and source contacts and a Schottky contact, the gate,

whose role is to modulate the drain-source current flowing in the channel. The gate contact of the AlGaN/GaN HEMT is a Schottky contact formed by a junction between a metal stack and AlGaN layer. The epitaxial growth is carried out on a substrate which can be a source of impurities that can affect the active layer. These impurities are due to the lattice mismatch with the upper layer, responsible for dislocations, which can spread to the channel.

The mechanical strain in the heterostructure depends on the thickness of the $Al_xGa_{1-x}N$ layer and the Al mole fraction.

Figure 1.9 shows the conduction energy band diagram and charges distribution in the AlGaN/GaN heterostructure. Where σ_{P1} is the charge due to spontaneous and piezoelectric polarizations induced at the AlGaN layer interfaces, σ_{P2} is the charge due solely to spontaneous polarization induced at the GaN layer interfaces, and the resulting positive charge $\sigma_{P1}-\sigma_{P2}$ induces the formation of a two-dimensional electronic gas ($-\sigma_n$) at the AlGaN / GaN interface to satisfy the electrical neutrality condition. The charge σ_n is therefore proportional to bias charge ($\sigma_{P1} - \sigma_{P2}$), minus the depletion charge due to the electric field in the AlGaN barrier layer coupled with the C_{AlGaN} capacitance and in the GaN layer coupled to the C_{GaN} capacitance. The proposed model takes into account surface defects that result in a surface charge, $+\sigma_{S1}$, and interface defects that result in a charge at the GaN / substrate interface, $-\sigma_{S2}$.

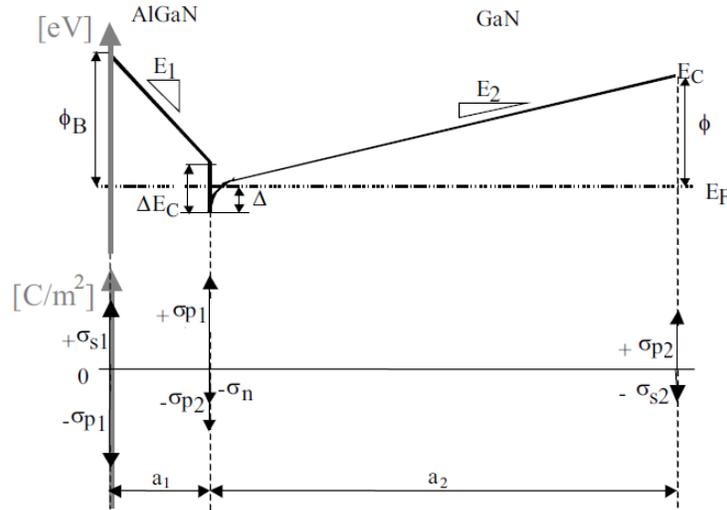


Figure 1.9: Conduction energy band diagram and charges distribution in the AlGaN/GaN heterostructure [49]

The dotted line is the position of the Fermi level in the semiconductor. ϕ_B is the height of the potential barrier at the surface, ϕ is the height of the potential barrier between the GaN layer and the substrate. E_F is the Fermi level and E_V is the valence level. E_1 and E_2 are the electric

field intensity in the AlGa N and the Ga N layers respectively, ΔE_C is the conduction band offset between $Al_xGa_{1-x}N$ and Ga N , Δ is the penetration of the conduction band edge below the Fermi level at the AlGa N /Ga N interface, $+\sigma_{S1}$ is a positive surface charge that participates in the $-\sigma_{P1}$ charge compensation, and $-\sigma_{S2}$ is a negative charge located on the lower face of the Ga N layer that participates in the compensation of the $+\sigma_{P2}$ charge.

The electrons transfer from AlGa N into Ga N and get confined in the triangular quantum well. The charge density is called two dimensional electron gas (2-DEG) due to the two-dimensional distribution of electrons in the channel.

By applying the Gaussian law to the three interfaces of the AlGa N / Ga N HEMT structure:

$$\sigma_{S1} - \sigma_{P1} = -\epsilon_1 E_1 \quad (1.5)$$

$$\sigma_{P1} - \sigma_{P2} - \sigma_n = \epsilon_1 E_1 + \epsilon_2 E_2 \quad (1.6)$$

$$\sigma_{P2} - \sigma_{S2} = -\epsilon_2 E_2 \quad (1.7)$$

Where ϵ_1 and ϵ_2 are the dielectric permittivities of the AlGa N and the Ga N layers respectively. To satisfy the neutrality condition, we deduce from equations 1.5, 1.6 and 1.7

$$\sigma_n = \sigma_{S1} - \sigma_{S2} \quad (1.8)$$

Considering that the majority of electrons occupy the first energy subband, the 2-DEG carrier density is governed by the following equation:

$$n_{2D} = \int_0^\infty D(E)f(E)dE = \left(\frac{m^*}{\phi^2 q} \right) \frac{\Delta}{q} \quad (1.9)$$

Where h is the Planck constant,

m^* is the electronic effective mass,

$f(E)$ is the Fermi-Dirac distribution function,

$D(E)$ is the energy density of states.

Writing σ as a function to n2D:

$$\frac{\phi_B}{q} - E_1 a_1 - \frac{\Delta E_C}{q} + \frac{\Delta}{q} = 0 \quad (1.10)$$

$$E_1 = \frac{\Delta - \Delta E_C + \phi_B}{q a_1} \quad (1.11)$$

The 2DEG thickness is much lower than GaN layer thickness, we deduce then:

$$\frac{\phi}{q} \approx E_2 a_2 \quad (1.12)$$

Using equation 1.6 and the expressions of E_1 and E_2 given in equations 1.11 and 1.12, it follows that:

$$\sigma_n = \frac{\sigma_{P1} - \sigma_{P2} - \frac{\epsilon_2 \phi}{a_2 q} - \epsilon_1 \left(\frac{\phi_B - \Delta E_C}{a_1 q} \right)}{1 + \frac{\epsilon_1 \pi \hbar^2}{a_1 q^2 m^*}} \quad (1.13)$$

Taking into account the V_{GS} polarization effects on σ_n :

$$\sigma_n = \frac{\sigma_{P1} - \sigma_{P2} - \frac{\epsilon_2 \phi}{a_2 q} - \frac{\epsilon_1}{a_1} \left(\frac{\phi_B}{q} - \frac{\Delta E_C}{q} - V_{GS} \right)}{1 + \frac{\epsilon_1 \pi \hbar^2}{a_1 q^2 m^*}} = \frac{\sigma_{P1} - \sigma_{P2} - C_2 \frac{\phi}{q} - \frac{\epsilon_1}{a_1} \left(\frac{\phi_B}{q} - \frac{\Delta E_C}{q} - V_{GS} \right)}{1 + C_1 \frac{\pi \hbar^2}{q^2 m^*}} \quad (1.14)$$

Where $C_1 = C_{AlGaN}$ and, $C_2 = C_{GaN}$

If the AlGa_N layer is completely deserted, the threshold voltage of the HEMT, is defined as the bias voltage to be applied to the gate to bring the GaN surface to the inversion threshold. From Equation 1.14, it follows the expression of the threshold voltage V_{TH} of a classical AlGa_N / GaN hetero-structure without taken into account the doping effects of the AlGa_N layer:

$$V_{TH} = \frac{\phi_B}{q} - \frac{\Delta E_C}{q} - \frac{\sigma_{P1} - \sigma_{P2}}{C_1} + \frac{C_2 \phi}{C_1 q} \quad (1.15)$$

1.4 Applications of AlGa_N/Ga_N HEMTs

Thanks to the excellent physical properties of Gallium Nitride, HEMTs have tremendous success in penetrating the consumer market for a wide range of applications, which include cell phones, radar, mixers, oscillators, surveillance, reconnaissance, TV broadcasting, communication satellite, base stations, sitcom, space, digital radios and attenuators in both commercial and military applications [4]. GaN HEMTs have found use in wireless infrastructures and high power electronics due their high efficiency, high frequency operation and high operating voltages [4]. Figure 1.10 shows the characteristics and applications areas of AlGa_N/Ga_N HEMT.

AlGa_N/Ga_N high electron mobility transistors (HEMTs) have attracted a lot of attention for Radio Frequency (RF) and Power Switching Application [51, 52], which will be presented and discussed in the following sections.

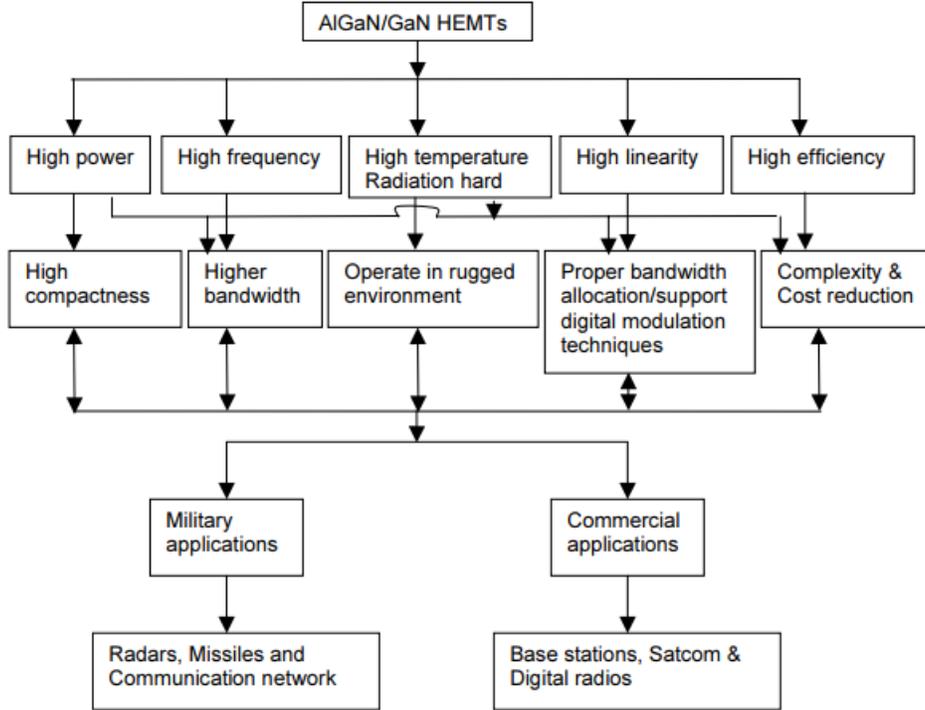


Figure 1.10: Characteristics and applications areas of AlGaIn/GaN HEMT [50]

1.4.1 RF Power Applications

RF performance of GaN devices have been widely reported in literature, with optimum performances concerning the maximum power capabilities (approximately one order of magnitude better than GaAs technology), and comparable maximum operating frequency. One of the best power performances of GaN on Si substrate with ultra-short gate at 40 GHz, have been demonstrated by Marti et al. [53], with a $P_{OUT} = 2 \text{ W/mm}$ (Table 1.4). According to equation 1.16, high values of transconductance (G_M), high values of the saturation velocity and low gate capacitances, enable to reach high intrinsic cut-off frequency values.

$$f_T = \frac{G_M}{2\pi C_G} = \frac{V_S}{2\pi L_G} \quad (1.16)$$

Where G_M is the transconductance,

C_G is the gate capacitance,

V_S the carrier velocity, and

L_G is the effective gate length.

Moreover, the device scaling will theoretically allow higher f_T and therefore f_{MAX} , due to

the inverse correlation with the gate length L_G , keeping a high aspect ratio between the gate length and the gate-to-channel distance. Reducing the gate length is crucial for increasing high-frequency performance; however, it becomes more and more difficult to fabricate ultra-short gate length devices. One of the smallest transistor gate reported in the literature for a GaN-HEMT is 20 nm [54]. Table 1.4 summarizes the recent research progress in GaN-based HEMTs with ultra-short gate (20-160 nm) for high power RF applications.

Table 1.4: Recent research progress in GaN-based HEMTs for high power RF applications (2010-2017)

L_G (nm)	I_{DSS} (A/mm)	f_T (GHz)	f_{MAX} (GHz)	f (GHz)	P_{OUT} (W/mm)	Substrate	References
20	>4	342	518			SiC	[55]
20		454	444			SiC	[56]
30	1.57	245	13			SiC	[57]
30	1.8	300	33			SiC	[58]
30	1.5	370	30			SiC	[59]
30	1.9	400	33			SiC	[60]
50	2.1	221	290			SiC	[61]
60	2.1	210	55			SiC	[61]
60	1.65	183	191	38	2.7	SiC	[62]
70	1.65	162	176			SiC	[63]
75	1.05	152	149	40	2	Si	[53]
75	0.8	170	210			SiC	[64]
80	1.1	114	230	40	1.25	SiC	[65]
80		176	70			Si	[66]
90	1.25	113	160	35	4.18	SiC	[67]
100	1.74	103	162			Si	[68]
100	1.65	80	200			SiC	[69]
100	1.13	115	150			Si	[66]
160	1.19	79	113.8			SiC	[70]
160	2	85	103			Si	[71]

As shown in Table 1.4, a downscaling of the gate length to sub-100 nm regime in conjunction with state-of-the-art technologies allows to improve the frequency performances. The highest f_T of 454 GHz with a simultaneous f_{MAX} of 444 GHz is obtained for 20 nm self-aligned gate HEMTs. With an off-state breakdown voltage of 10 V, the Johnson figure of this device reaches 4.5 THz - V [56].

1.4.2 Power Switching Applications

In addition to RF applications, the unique properties of GaN-based HEMTs have also attracted great interest in high-voltage power-switching applications, where the transistors are switching between their off and on states.

Power switching devices are used for power conversion applications that involve transforming a DC voltage to a lower value (buck converter) or to a higher value (boost converter). This may also be extended to converting a power source from AC to DC and vice versa or any other power switching circuit. Three important parameters of a power-switching transistor are the breakdown voltage ($V_{Breakdown}$), on-state resistance (R_{ON}) and gate capacitance (C_G). Kanamura et al. [72] have reported an off-state breakdown voltage of 320 V in E-mode MISHEMT with a triple cap layer with recessed-gate structure leading to a threshold voltage of +3 V. Finally, Srivastava et al. [73] have reported a breakdown voltage of 2.2 kV for HEMT with gate drain distances of 20 μm fabricated on Si by a new local Si substrate removal technology.

1.4.3 Future applications

Optimized AlGaIn/GaN HEMTs are well suited to play a pivotal role in next generation market demand. The past decade has witnessed tremendous progress in the development of III-nitride based light emitting diodes (LEDs) for lighting and high electron mobility transistors (HEMTs) for power applications.

Integration of InGaIn/GaN light-emitting diodes (LEDs) and AlGaIn/GaN high-electron-mobility transistors (HEMTs) on a common material platform is attracting increasing interest due to its advantages in reducing device footprint, enhancing system reliability, and minimizing interconnect-related parasitic [74]. Monolithic integration of HEMTs and LEDs aims to reduce undesirable parasitics and greatly improve the system stability as well as reliability. However, there are limited reports on the monolithic integration of the two kinds of devices, probably due to the huge difference in material requirements for LEDs and transistors as well as the complexity of device fabrication. A monolithic integrated HEMT-LED device with comparable performance to stand-alone devices has been recently fabricated and the breakdown voltage was enhanced, without degradation of the HEMT DC performance [75]. It shows a potential applications such as solid-state lighting, displays, and visible light communications. Figure 1.11 shows a cross-sectional schematic of the finished HEMT-LED on sapphire substrate. The inset shows the equivalent circuit diagram of the device [5].

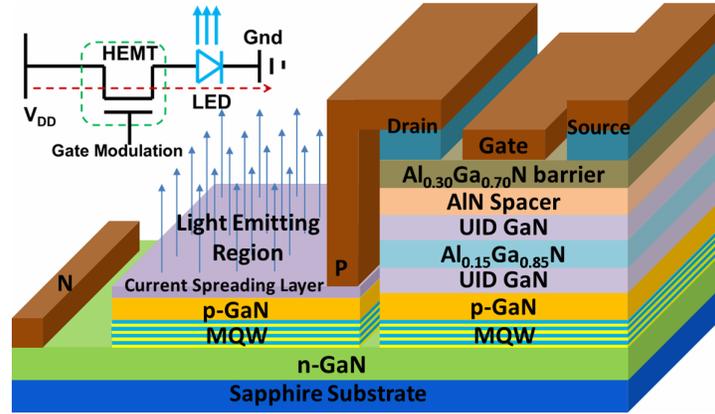


Figure 1.11: Cross-sectional schematic of the finished HEMT-LED on sapphire substrate. The inset shows the equivalent circuit diagram of the device [5]

1.5 GaN Reliability issues

Despite the very good material properties, the device design that have become matured with intensive studies and large effort spent in recent years and the excellent device performances for both RF and high power switching applications, there are still some issues that limit the device practical applications. Indeed, reliability has still to be fully demonstrated.

1.5.1 Reliability indicators

This section is mathematically oriented to an introduction to some of the main reliability notions and approaches. Reliability is one of the most important parameter before marketing a product. It is defined as the ability of a component, circuit or system to perform an intended or required function or mission without failure or degradation. The mission profile is defined in terms of specified operating and environmental conditions (such as temperature, voltage, current, etc.) and of given time duration [76].

Mathematically, the reliability function $R(t)$ is the probability that a component, circuit or system survives beyond any given specified time denoted by:

$$R(t) = P(T > t) \quad t \geq 0 \quad (1.17)$$

Where T is a random variable denoting the time-To-Failure or the Failure Time.

Robustness is the ability that its performances are not affected by the uncertain inputs or environment conditions.

Meanwhile, the unreliability $F(t)$, or the probability of failure, is defined as the probability that a component, circuit or system will not perform the required function under the operating

conditions encountered for a stated period of time t .

$$F(t) = 1 - R(t) = P(T \leq t) \quad t \geq 0 \quad (1.18)$$

Another reliability parameter related to $F(t)$ is the probability density function of failures, $f(t)$ defined as its derivative:

$$f(t) = \frac{dF(t)}{dt} = P(t < x < t + dt) \quad (1.19)$$

It represents the probability of an item failing in the time interval dt at time t , when the item was operating at $t = 0$.

The failure rate λ is expressed as the ratio of the total number of failures to the total operating time: $\lambda = K/T$, where K is the number of failures and T is the total operating time.

Two important parameters defined to describe the statistical distribution are the Mean Time To Failure ($MTTF$) and the Median Lifetime (MTF or t_m). The Mean Time To Failure is calculated as the mean value of a distribution:

$$MTTF = \int_0^{+\infty} t f(t) dt \quad (1.20)$$

In the case of $\lambda = Cst$, $MTTF$ is the reciprocal of the failure rate $1/\lambda$. It is used to describe the expected time to failure for non-repairable devices once they fail. The Median Lifetime t_m expresses the "average" value of a statistical lifetime distribution and it is defined as the time to 50% failures

$$t_m = MTF = \{t : Q(t) = 50\%\} \quad (1.21)$$

The reliability of semiconductor devices is associated to the failure rate $\lambda(t)$ over time described by the known "bathtub" curve. This latter is divided into three regions as shown in figure 1.12. Zone 1 is the infant mortality period characterized by an initially high failure rate due to the latent defects in the device, which falls off till time t_{infant} . Early failures can be eliminated by a "burn in" period during which time the equipment is operated at stress levels closely approximating the intended actual operating conditions in order to eliminate the external reasons causing defects. In zone 2, the device enters into a stable stage "useful life" with a constant failure rate. For high reliability applications, this constant failure rate λ should be extremely small. Finally, in zone 3 after time $t_{operation}$, the failure rate will increase sharply due to "wear-out" and the device comes to the end of its lifetime.

To understand and characterize reliability, data should be analyzed by a lifetime distribution

which models the lifetime of GaN based HEMTs during the stress and provides an insight into characteristics of failure times. There are many different lifetime distributions that can be used to model reliability data. The most widely applicable distributions for life data analysis, used for electronic and electrical components and systems, are the exponential, Weibull, normal and lognormal distributions and each one of them has a predefined form of $F(t)$.

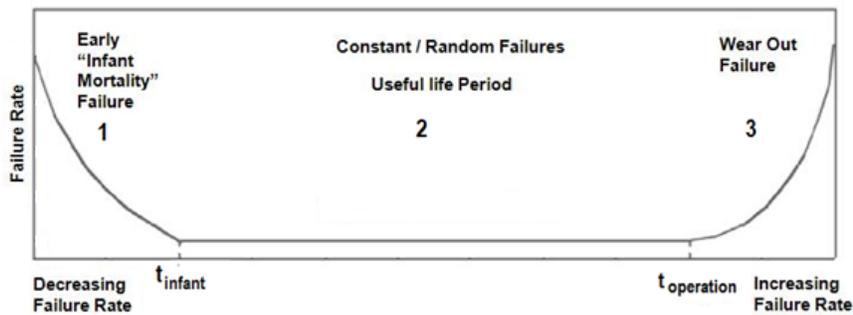


Figure 1.12: The bathtub curve of failure rate

The reliability assessment must begin with a survey of known conditions under which the device will operate. This may include a wide variety of factors for a semiconductor device. These conditions, which can induce different failures, or accelerate degradations localized in different areas of the device, hence reducing the lifetime, will be further discussed in the next sections.

1.5.2 Methods and tools for reliability assessment

1.5.2.1 Life test for reliability evaluation

Accelerated Stress Testing can be simply defined as: using higher-than-normal stress, and then failure can be induced earlier than usual. Hence much attention must be given to the stress conditions.

Accelerated Stress Testing consists of exposing a group of products to one or more stressing environments. In this section we will present some of the commonly used environments that can include electrical Stress, thermal cycling, thermal shock, mechanical stress, humidity, radiation, vibration and others.

- Electrical Stress: is used to test a product near or at its electrical limits. There are two basic types of electrical stress tests: Power Cycling and Voltage Margining.

We can distinguish four bias states (Figure 1.13) that are defined by different bias conditions. First a high-power State; biased at high current and high voltage. Second, an ON-state; biased to saturation with high current and low voltage. Third, an OFF-state; biased at very small current

and high voltage. Finally, $V_{DS} = 0$ state with the source and drain shorted at $V_D = V_S = 0$.

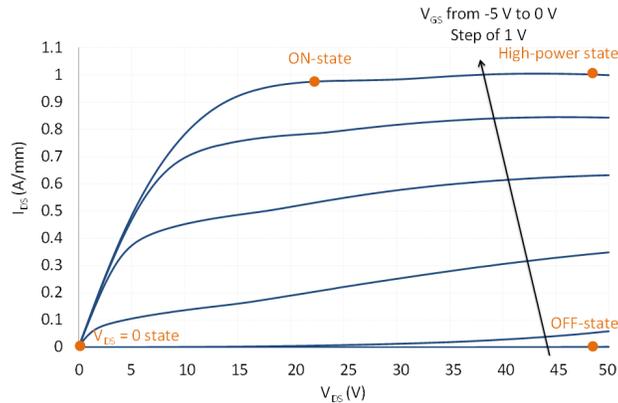


Figure 1.13: The four bias states for DUT aging have distinct stress conditions

- Thermal stress: Two types of thermal stresses can be carried out. Thermal cycling or thermal shock. Thermal cycling exposes products to alternating low and high air temperatures to accelerate failures caused by repeated temperature variations during normal use conditions. The transition between temperature extremes occurs very rapidly during thermal shock testing while temperature cycle testing uses slower rates of change between high and low temperatures.

- Mechanical stress: (or mechanical shock) such as vibration which involves stimulating a product with a pre-determined force over a frequency spectrum.

- Humidity testing is typically performed in a chamber that can precisely control wet and dry bulb temperatures. Exposing products to humidity stress precipitates corrosion and contamination defects in products. Humidity can penetrate porous materials, cause leakage between electrical conductors, and is also an important stress when evaluating coatings and seals.

- Radiation: study of radiation effects on AlGaIn/GaN HEMTs by X rays, protons, neutrons, and/or heavy ion irradiations is crucial for space applications in radiative environments [77].

- Combined environments: depending on product complexity, cost, and other reliability specifications, multiple environmental screens may be used simultaneously. For example, Thermal Cycling and Vibration are often combined in an Accelerated Stress Test program.

- High temperature Operating Life test (HTOL)

The devices are biased at predicted normal condition and stored at different temperatures (three to six temperatures generally between 175 °C and 310 °C). This enables to study the combined effects of thermal and electrical stresses and to assess the wear-out mechanism. HTOL is used for process qualification before the product release and manufacturing for commercialization. A short duration HTOL test known as "burn-in" is used for screening devices with high early failure and

infant mortality rate. HTOL permits extracting t_{50} (the time when 50 % of the devices is failed) that is often used instead of MTTF.

- High temperature Reverse Bias test (HTRB)

The gate Schottky diode is reverse biased close to breakdown voltage at high temperature. This permits to study the combined effects of high electric fields and temperature. As the devices under HTRB test are under pinch-off condition, the channel temperature is about the same as the case temperature.

- I_{DQ} (Quiescent Drain current test)

Another accelerated test used is the quiescent drain current test I_{DQ} which has a definition very close to HTOL. In this test, the device is biased at moderate drain current, high drain-source voltage and at different temperatures.

Figure 1.14 shows the typical bias points for HTOL, HTRB and I_{DQ} tests.

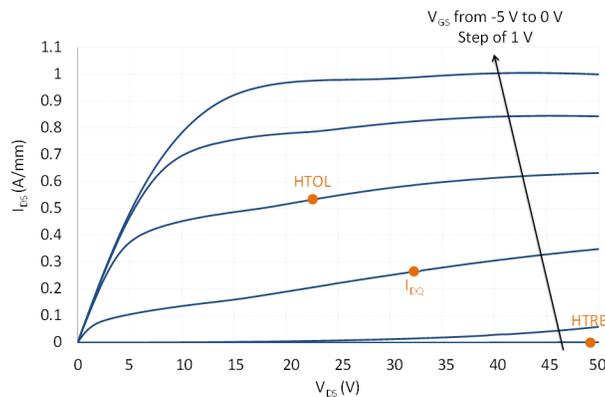


Figure 1.14: $I_{DS} - V_{DS}$ characteristics with possible bias points of ageing tests HTOL, HTRB and I_{DQ}

- Step Stress

The step stress test is performed at a fixed temperature, while voltages, currents or RF power applied during the stress are increased step by step with time either monotonically or with a recovery time period between each condition [78]. As the duration of the test can be short, it allows to obtain quickly information on the robustness of the technology. In particular, the maximum values of electrical conditions that can sustain the device can be determined. It is very useful for determining the safe operating area of the technology. Moreover, step stress tests can be

performed before long term aging tests. In this case, these tests allow to efficiently determine the aging electrical conditions applied during the long term aging test.

Three approaches to perform step stress tests are illustrated in Figure 1.15: the first one and the simplest consists in increasing the electrical stress step by step over time until the degradation observation. The second one called "cycling stress" consists in alternatively applying stress conditions and unstress conditions for a specified time. This latter period corresponds to a recovery period. Finally, the third one called "step-stress-recovery" is a combination of the previous tests. In this test, the electrical conditions are increased step by step but each aging step is followed by a recovery period.

The cyclic stress includes periods of recovery and Step-stress-recovery are particularly useful when trapping-detrapping mechanisms are involved.

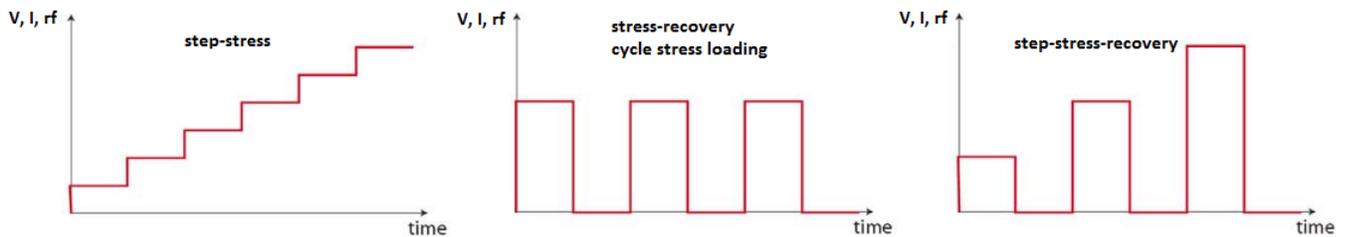


Figure 1.15: Three alternatives to a continuous DC stress. (left) Step-stress incrementally increases the stress conditions. (middle) The cyclic stress includes periods of recovery. (right) Step-stress-recovery is a combination of the other two

Step-stress experiments will be performed in the framework of this thesis in order to investigate reliability assessment of ultra-short gate AlGaIn/GaN HEMT on Si substrate.

1.6 Degradation mechanisms and trapping effects

Although impressive results were published for GaN-based transistors in a large frequency range, the performance and the reliability demonstration is still limited by a number of mechanisms and conflicting mean time to failure (MTTF) data on existing device designs which are a very important subject of concern [79].

Recent researches have presented deeper insight into the origins of device degradation which are addressed in the following sections.

1.6.1 Degradation mechanisms

Degradation mechanisms are the processes that occur in the device structure during an accelerated life test or operational life. They penalize the electrical performances and the reliability, and thus the lifetime of devices. Over the years, several failure mechanisms that limited device lifetime have been addressed.

In the figure 1.16 are reported a summary of the main failure mechanisms plaguing the GaN HEMT performances and reducing the device reliability.

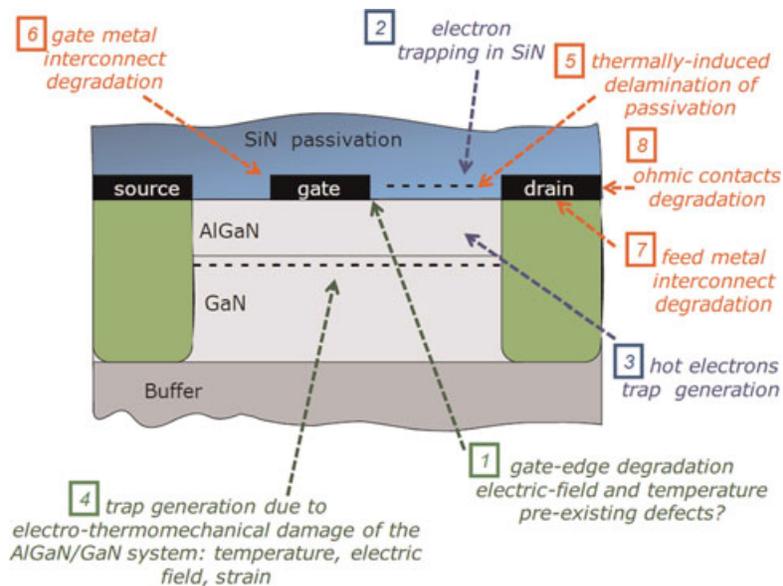


Figure 1.16: Failure mechanisms identified on GaN based HEMTs.

Red: Thermally-activated mechanisms/ Blue: mechanisms related to the presence of hot electrons (trapping effects)/ Green: mechanisms due to the polar and piezoelectric nature of the semiconductor material [80]

Failure mechanisms identified in red (5, 6, 7 and 8) refer to thermally activated degradation mechanisms, which have been previously observed in devices processed in other semiconductor systems such as Si, GaAs, InP, SiC, etc., and hence these failure mechanisms are more inherent to the metallization scheme rather than to the GaN material itself. Temperature has been identified as an accelerating factor for passivation stability and for contacts degradation.

Failure mechanisms identified in blue (2 and 3) are related to the presence of hot electrons, which are common to all high-voltage field-effect-transistors. Also hot-electrons related degradation has been largely reported in all the other semiconductor devices such as Si, GaAs, InP, etc.; hence, also these failure mechanisms are more inherent to the hot-electrons effects itself, rather than to the GaN material. Hot-electrons have been associated to trapping effects on the surface or

within the semiconductor layers.

Finally, failure mechanisms identified in green (1 and 4) are peculiar to GaN devices due to the polar and piezoelectric nature of this semiconductor material. This opens a new window in the reliability physics study, since these mechanisms have never been clearly identified in the other semiconductors. They have been correlated with the gate-edge degradation or with bulk-trap generations.

In the following, degradation mechanisms typical of GaN materials are described with reference to the various technologies.

1.6.1.1 Hot-electrons degradation effect

One well-known failure mechanism of early GaAs-based devices was hot electron-induced degradation [81]. It has been observed too in AlGaIn/GaN HEMTs and is typically prominent at very high drain voltages, where electrons may be trapped on the device surface, in the AlGaIn barrier layer or in the GaN buffer layer giving rise to reversible degradation of drain saturation current I_{DSS} and transconductance G_M [82, 83] and to an increase in drain resistance and a shift in threshold voltage [84].

The hot electrons can create defects or dangling bonds which may act as deep levels or traps. For these reasons, hot electron can be the origin of degradation processes and trapping phenomena within the passivation or GaN layers, as described in Figure 1.17.

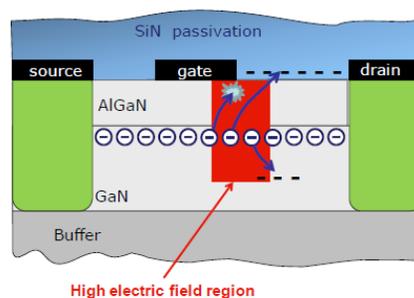


Figure 1.17: Cross section of AlGaIn/ GaN HEMT, identifying electrons achieving high energy and becoming "hot" [80]

Luminescence in HEMT is usually due to intra-band transitions of highly energetic electrons. In GaN devices, it can be due to band-to-band recombination typically associated with hot-electrons accelerated by the high longitudinal electric field in the channel, which scatters with charged centers releasing the energy in the form of photons [85, 86].

Hot-electron degradation has been proposed as the dominant failure mechanism on GaN based

HEMTs: Meneghesso et al. [81] have shown stronger performance reduction on semi-ON state stress with respect to ON-state (higher channel temperature) and OFF-state (higher electric field) stress, followed by a remarkable slow-trapping phenomena especially at the highest current tests. Coffie et al. [87] have presented a RF-power degradation with a negative activation energy, typical of hot-electron induced degradation. To avoid degradation by hot-electrons caused by the presence of high electric field in the gate-drain region, proper solutions are needed such as by adopting surface passivation and by realizing an extension of the gate metal to the region between the gate and the drain [4, 88, 89] so-called field plate.

1.6.1.2 Inverse piezoelectric effect

Because of the piezoelectric nature of AlGaN and GaN, the lattice mismatch between the material interfaces results in significant tensile strain. Exceeding a critical voltage, leads to layer relaxation through crystallographic defect formation. It is possible that the defects could be electrically active and induce device degradation [90]. The inverse piezoelectric effect is a consequence of the application of high electric field to piezoelectric GaN and the resulting additional mechanical strain in the semiconductor can lead, in certain bias and temperature conditions, and in the presence of nucleation defects, to lattice damage and further defects formation [91]. In addition, induced piezoelectric strain/stress in gate-drain region under different bias conditions was evaluated by micro-Raman measurement [92]. Under high drain bias, a large electric field appears around the drain-side of the gate edge across barrier layer which induces a large amount of mechanical stress, and thus promotes the formation of crystallographic defects and relaxation of the strain when the electric field reaches a certain value. Cross sectional transmission electron microscope (TEM) results revealed the formation of pits or cracks in the AlGaN barrier layer close to the drain side. Energy dispersive X-ray (EDX) measurement found that the cavity formed during degradation was filled with SiN_x passivation material. The fact that the passivation layer flowed into the cavity and oxidation occurred implies that high temperature by joule heating is involved in this failure. Only the presence of a vertical crack can be supported by the inverse piezoelectric effect [93].

1.6.1.3 Runaway effect

A new electric parasitic effect so called "electrical runaway mechanism" has been identified and characterized [94]. It is manifesting by an anomalous behavior of the gate current evolution as a function of V_{GD} on I_D (V_{DS}) output characteristics and I_D (V_{GS}) transfer characteristics in DC measurement. It consists of an important drop of output power correlated with a large negative increase of gate current with input power level in RF power measurement. As it can be observed in Figure 1.18, runaway mechanism takes place (red line) when the gate bias increases toward positive

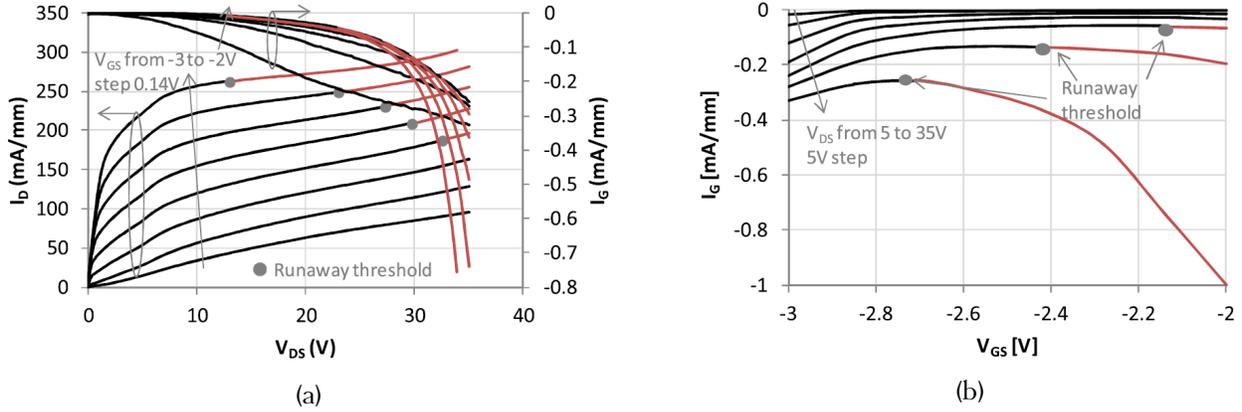


Figure 1.18: (a) I_D - V_{DS} characteristics at 125 °C, (b) I_G - V_{GS} characteristic at 125 °C, (GH50-10) Black: out of runaway operation/ Red: runaway operation/ Grey dots: runaway threshold [94]

value as the absolute gate current value increases too. Furthermore, the more the channel is open, the lower the V_{DS} runaway threshold voltage is.

The runaway mechanism has been correlated with tunnel effect conduction, since the increase rate of the gate current (dI_G/dV_{DS}) versus V_{DS} has been found to not depend on temperature but on electric field distribution in the gate to drain spacing of the device [95]. Since runaway mechanism can be observed on non-aged devices, it might be attributed to the presence of inherent defects in the AlGaIn layer [96]. Considering the deep insight electrical and optoelectrical measurement results, the physical mechanism inducing this new electrical parasitic effect is assumed to be uniformly distributed under the gate fingers area [97]. The runaway mechanism is strongly dependent on the quality of the Schottky contact and AlGaIn barrier layer. Indeed, it has been found amplified during reliability aging test where Schottky contact degradation and defects creation in AlGaIn barrier layer can be observed [96, 97]. In fact, it has been found to worsen throughout reliability aging test during which it can be observed a Schottky contact degradation and defects creation in AlGaIn layer.

1.6.2 Trapping effects

The trapping effects are the undesirable effects that appear on the I-V characteristics of fresh devices which may or not impact the lifetime of the device. They are induced by electron trapping at different locations of the device structure such as at the surface of the AlGaIn layer near the gate edges or at the metal/AlGaIn interface, inside the AlGaIn or GaN layers or at the AlGaIn/GaN interface. These effects are responsible for the degradation of electrical performances and have not been fully understood. Trapping-detrapping mechanisms induce electrical parasitic effects such as

current collapse or power slump, kink effect, belly shape...

Recently, intensive studies have been carried out to understand and mitigate the trapping effects in AlGaN/GaN HEMTs and several different techniques have been used, including current-mode Deep Level Transient Spectroscopy (DLTS), [98,99], conductance deep level transient spectroscopy (CDLTS) [100], transient drain current [101], gate leakage current [102] and threshold voltage [103] measurements at different temperatures as well as frequency dispersion in capacitance and conductance analysis [104].

1.6.2.1 The kink effect

The kink effect is an anomalous increase in the drain current I_{DS} at a relatively low drain source voltage V_{DS} as shown in Figure 1.19, resulting from the shift in threshold voltage.

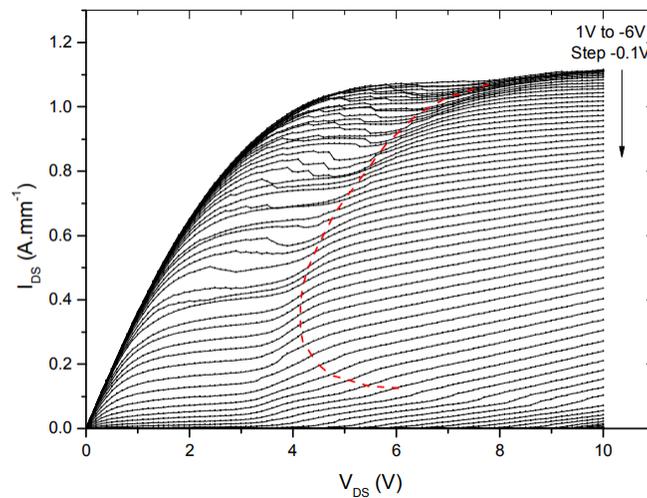


Figure 1.19: Forward I-V characteristics of a $2 \times 25 \times 0.1 \mu\text{m}^2$ HEMT [105]

The mechanisms of kink effect are classified from three viewpoints and have been clearly summarized in [106]:

- channel impact-ionization and subsequent hole accumulation, leading to change of surface or channel/substrate interface potential [107]. Altuntas et al. [105] showed that kink effect takes origin from impact ionization of shallow levels in the vicinity of the gate, - field-dependent trapping/de-trapping in deep levels [108],
- a combined effect of impact ionization and deep levels, thereby generating holes and modifying the occupation state of the surface, and the bulk or channel/substrate interface deep levels [109].

Meneghesso et al. [110] suggested that the kink effect could be induced by interband impact ionization of electrons by slow traps in the epitaxial layers under the gate, possibly in the GaN

buffer. Xu et al. [111] have reported that kink effect in AlGaN/GaN HEMTs can be decreased by using Al_2O_3 passivation replacing Si_3N_4 .

1.6.2.2 The current collapse phenomena

Another important parameter in the evaluation of device reliability is current collapse or also named dispersion, current compression, power slump which is the reduction of drain current after the application of high voltage. This effect limits the performance of HEMTs in high power and high frequency applications.

The origin of current collapse was attributed to surface trapping, in the AlGaN barrier layer, or buffer trapping, in the GaN buffer layer. Kawanago et al. [112] studied the gate metal contribution to the current collapse in the AlGaN/GaN HEMTs. They suggested the involvement of electron trapping on the defects in the AlGaN layer, particularly at the gate edge on the drain side. Also, the nitrogen vacancies in the AlGaN layer were pointed out to be responsible for electron trapping in AlGaN layer. To determine a detailed degradation mechanism, it is very important to understand the trapping behavior, such as the physical locations, energy levels and trapping/detrapping time constants. Various trap characterization methods, such as deep-level transient spectroscopy (DLTS) [113, 114], low-temperature Constant-Capacitance Deep-Level Transient Fourier Spectroscopy (CC-DLTFs) [115], frequency dependent capacitance and conductance measurements [104], and capacitance-voltage (C-V) measurements were employed to study trapping effects.

Possible mechanisms of the suppression of trapping effects by SiN_x passivation are:

- Passivation prevents the electrons from tunneling from the gate metal and the trap state density [116]
- Replacement of surface donors by the incorporation of passivation between Si and surface states [117].

An alternative Al_2O_3 dielectric layer deposited by atomic layer deposition technique is shown to improve pulsed I-V and RF power performance over PECVD SiN [118].

Optimized surface field plate structure is effective for the suppression of the current collapse phenomena due to the relaxation of the electric field peak at the gate edge [119]. It was proven that the use of dual-FP approach is effective to achieve almost collapse free operation for multi-fingered AlGaN/GaN MOS-HEMTs with a total gate width of 10 μm [120].

1.6.2.3 The Belly-Shape

Belly-shape (BS) is an electrical parasitic effect detected on the gate-source and gate-drain diodes forward current-voltage characteristics. The belly shape effect is characterized by higher gate current observed at low V_{GS} values on devices which have been submitted to HTRB [121] aging

test or HTOL aging test [122]. As shown in Figure 1.20, the belly shape effect induced by a HTOL test is assumed to be a transient effect attributed to trapping mechanisms located beneath the gate in the gate/cap GaN interface or at the gate edges [122]. In addition, Brunel et al. [121] detected the "belly shape" effect on GaN based HEMTs that were stressed by HTRB aging test carried out at 175 °C up to 4000 hours. It has been attributed to lateral surface conduction and correlated with electroluminescence signature under diode forward biasing conditions but not under transistor pinch-off biasing conditions. The physical analyses have pointed out the formation and growing over time of pits and cracks, at the gate foot edge on the drain side, attributed to the inverse piezoelectric effect.

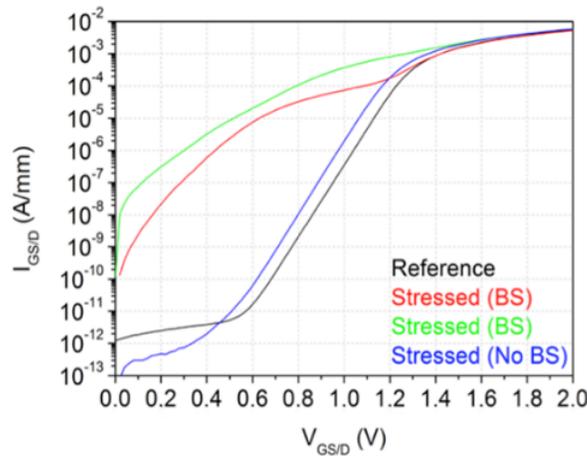


Figure 1.20: Forward gate current characteristics at $V_{DS} = 0$ V for a reference device, one stressed device without Belly Shape and 2 stressed devices with Belly Shape [122]

1.7 Reliability of HEMT with ultra-short gate

Gate length downscaling is one of the most effective methods to increase the static and the microwave performances in most semiconductor technologies, while keeping high aspect ratio. As the gate length scales down, the gate capacitance decreases and the electron velocity increases.

Up to now, only few papers have investigated on reliability assessment of ultra-short gate AlGaIn/GaN HEMTs on Si substrate. AlN/GaN-on-Si HFETs with 100 and 200 nm gate lengths have been tested in off-state stress test [123]. A 100 nm gate length GaN HEMT suitable for applications up to W-band frequencies has been investigated by on and off-state DC-stress tests. A life time higher than 10^5 hours was extrapolated using the constant current stress test at a base plate temperature of 125 °C [124]. A 150 nm T-gate length AlGaIn/GaN HEMTs stressed in air failed faster

and at a lower junction temperature than those stressed in nitrogen atmosphere due to an oxide formation. The observed oxide formation for devices stressed in air was underneath the gate for T-gate devices, but at the drain edge of the gate between the gate foot and the field plate dielectric for field plate devices. When stressed in dry nitrogen gate sinking mechanism has been observed only in T gate devices [125]. In ref [126], GaN HEMT robustness was also evaluated by voltage step-stress tests showing that electrical stress degradation in the gate and drain currents is electric field driven.

The optimized heterostructure with gate length scaling and efficient process technique can provide improved DC and RF performances. In 2015, Jatal et al. demonstrated 80 nm gate length on Si substrate with f_T of 176 GHz and f_{MAX} of 70 GHz [66].

The classical approach of reducing sizes of current technologies seems to reach limits and leads to difficult and complex problems such as short channel effect, interconnections, tunnel effect, etc. Therefore, the features of nanodevices appear to be the key solutions facing the goal of more integration and more complexity.

1.8 Conclusion chapter 1

In this chapter, to illustrate the advantages of GaN-based semiconductors over its predecessors, the physical properties induced by the wurtzite GaN and group-III-nitride compound semiconductors have been discussed. These properties are important for the operation of devices fabricated from this class of materials and exhibit high levels of spontaneous and piezoelectric polarizations.

Then, the structure of GaN based HEMT and its operating principles have been explained. The reduction of the defect density and the improvement of GaN epitaxial techniques constitute a major challenge for the development of HEMTs. Applications and a state of the art of GaN based HEMT performance are then presented.

AlGaIn/GaN HEMT is at the forefront of semiconductor research because of its excellent material properties and the presence of a high-mobility two-dimensional electron gas (2DEG) at the hetero-interface. It has demonstrated excellent high power and high frequency performance compared with counterparts based on other materials. However, HEMT reliability is still under investigation, due to the continuous evolution of the process and technologies, and the the lack of technological solutions of failure. Hence, before tremendous commercialization of GaN HEMTs, reliability has to be fully demonstrated and more investigation is needed to improve device technology, epitaxy, design and other performance limiting factors.

Not yet mature, GaN-based HEMTs are subject, in addition to the degradation mechanisms traditionally observed, to additional degradation mechanisms due to the physical properties of the materials constituting them. Indeed, the presence of traps located on the surface and in the GaN

buffer causes the appearance of parasitic effects which greatly degrade the electrical performance of HEMTs. In addition, the piezoelectric nature of the materials used, coupled with strong polarizations between the gate and the drain, cause the formation of crystalline defects which can also affect the electrical performance of HEMTs.

Thus, the final part of this chapter was devoted to reliability issues; accelerated life testing, and GaN HEMT recoverable (trapping effects) and non-recoverable (degradation mechanisms) degradations, that are prominent in the literature, were reviewed. A particular attention will be given to the GaN HEMT with ultra-short gate.

Following chapters summarize the targets of the thesis and the main results obtained.

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Chapter 2

Device description and electrical characterization before aging tests

2.1 Introduction

AlGaIn/GaN HEMTs were processed at IEMN Lille, France (Epitaxy provided by CHREA). Two technologies were provided; devices grown by metal organic chemical vapor deposition (MOCVD) and devices grown using Molecular Beam Epitaxy (MBE).

In this chapter, the technology of the devices under test is described and then, the electrical characterization is detailed. The results of the MOCVD and MBE grown HEMTs, which have been used for experiments in this thesis, are discussed.

A characterization campaign is performed on the devices of both technologies with a measurement protocol established in the framework of this work. It comprises:

- DC characterization: The drain output characteristics $I_{DS}(V_{DS})$, the transfer and transconductance characteristics $I_{DS}-G_M(V_{GS})$ are measured. The quality of the Schottky contact is evaluated by measuring the gate Schottky diode characteristic $I_{GS}(V_{GS})$.

- RF characterization to determine the frequency performances of the components: The cut-off frequency f_T and the maximum oscillation frequency f_{MAX} are extracted.

We also got interested in the impact of the topology in terms of gate length, gate-drain distance and gate-source distance, on static and microwave performances. Electrical characterization of AlGaIn/GaN HEMT devices in this chapter will give information about the electrical performances of both technologies under test and will provide a basis for the selection of devices to be stressed.

2.2 Devices under test

IEMN Lille has developed two GaN fabrication processes based on epitaxy of GaN and AlGaN layers grown by MOCVD or MBE on Si substrate. There are differences of epitaxial layers and geometry between both processes.

Figure 2.1 shows AlGaN/GaN MOCVD HEMT wafer and AlGaN/GaN MBE HEMT wafer.

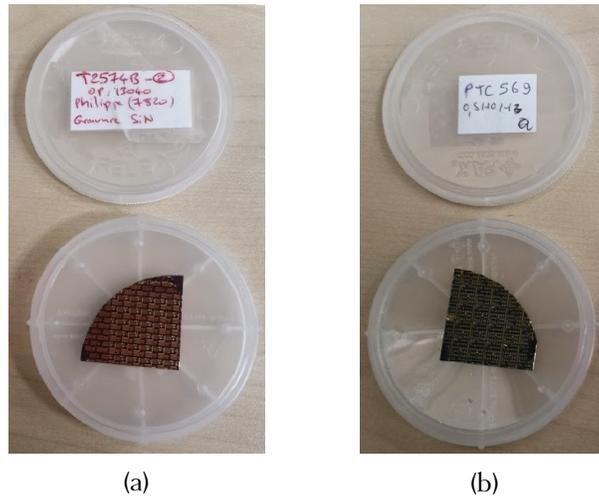


Figure 2.1: AlGaN/GaN HEMT wafers (a) grown by MOCVD, (b) grown by MBE

The epitaxial structure of the AlGaN/GaN MOCVD HEMTs under test is grown on silicon (III) substrate. A $0.2 \mu\text{m}$ thick AlN nucleation layer was grown directly on the substrate, followed by a $0.7 \mu\text{m}$ thick NID GaN buffer layer, a 1 nm thick AlN interlayer, a 15 nm $\text{Al}_{0.31}\text{Ga}_{0.69}\text{N}$ barrier layer and a 4 nm thick SiN cap layer. The use of the AlN interlayer included between the AlGaN barrier and GaN bulk aims improving the electron confinement and the electron mobility in the 2DEG channel [1]. The 2DEG charge density N_S is $1 \times 10^{13} \text{ cm}^{-2}$ and the electron mobility is evaluated to $1540 \text{ cm}^2/\text{V.s}$ by means of HALL measurement. Devices were processed at IEMN with Ti/Al/Ni/Au ohmic contact and Ni/Au metallization for Schottky contact. Devices were passivated by PECVD with 50 nm SiN/ 100 nm SiO_2 . Devices with two gate fingers are patterned with different gate lengths $L_G = 75, 100, 150 \text{ nm}$ and a total gate development of $2 \times 25 \mu\text{m}$. The gate-source distance is 600 nm for all devices and the drain-source distance is varying from 1.5 to $5.5 \mu\text{m}$.

Figure 2.2 shows the cross section of GaN HEMTs epitaxial structure grown by MOCVD.

The MBE-grown devices are fabricated on silicon (III) substrate. A 44 nm thick AlN layer was grown directly on the substrate, followed by a 250 nm thick $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ layer and a $0.13 \mu\text{m}$ thick AlN layer. Next, a $1.73 \mu\text{m}$ thick GaN channel layer was grown followed by 1 nm thick AlN interlayer. Finally, a 10 nm thick $\text{Al}_{0.29}\text{Ga}_{0.71}\text{N}$ barrier was grown and capped by a 0.5 nm thick

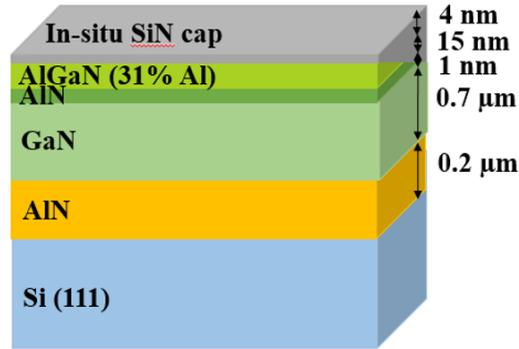


Figure 2.2: Epitaxial structure of GaN HEMTs grown by MOCVD

GaN layer. The devices were also processed at IEMN. The HEMTs are of $2 \times 50 \mu\text{m}$ wide, with a gate length of 75, 100 and 150 nm. The source-drain distance is $2.65 \mu\text{m}$ for all devices and the source-gate distance is ranging from 1.13 to $1.23 \mu\text{m}$

The epitaxial structure of the GaN HEMTs grown by MBE is shown in Figure 2.3.

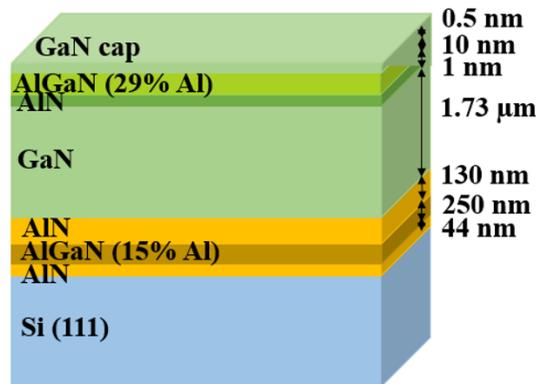


Figure 2.3: Epitaxial structure of GaN HEMTs grown by MBE

The distribution of the electric field in the channel is non-homogeneous in the HEMTs [2]. When the transistor is polarized by a drain-source voltage, the electric field in the gate-drain region registers a drastic increase with a peak at the gate exit drain side [3]. This sudden increase of the electric field at the output of the gate may cause electrical parasitic effects which can lead to the deterioration of the component. Therefore, the increase in the gate-drain distance becomes necessary in order to reduce the peak at the output of the gate thanks to a better distribution of the electric field. The reduction of the gate-source distance leads to the reduction of the source resistance and thus allows the improvement of component performances. Indeed, the parasitic

resistance of the source R_S is given by the following equation:

$$R_S = \frac{R_C}{W} + \frac{R_{\square} L_{GS}}{W} \quad (2.1)$$

Where R_C , W , R_{\square} and L_{GS} represent the contact resistance, the development of the transistor (or gate width), the sheet resistance and the gate-source distance respectively.

The widening of the gate-drain distance favors the interaction of the surface states with the bidimensional electron gas and the decrease of the electric field on the drain side, which leads to a higher breakdown voltage. Therefore, a compromise must be reached to combine better electric field in the channel with low parasitic capacitances.

In order to reduce the electric field, a reduction of current collapse phenomena due to surface traps [4,5], have to be made by using surface passivation as is the case of devices under test.

The technology under study in this thesis does not use field plate because the goal was to develop transistors operating at high frequency, even though this specific technique may have some advantages in terms of field spreading. It is consisting of an extension of the gate metal to the region between the gate and the drain [6-8], it has been used to suppress gate breakdown, and permits high bias voltages to be applied [9]. As described by Karmalkar et al. [10], field plates act to smoothen the electric field across the device channel and reduce the electric field peak at the gate exit. This means that the electric field distribution is improved [11,12].

Field-plated HEMTs when biased at $V_{DS} = 120 V$ have produced over $30 W/mm$ RF power density in S-band [13], and over $5 W/mm$ at $30 GHz$ with a drain bias of $V_{DS} = 30 V$ [14,15]. However, field plates connected to the source and gate contacts introduce an additional capacitance, which lead to increased switching times and reduced bandwidth for broadband amplifiers, and also reduce the transconductance of the transistor. Therefore degradation in frequency performances occurs. For this reason, a minimum field-plate length must be employed [16].

2.3 Technology

In this part, we will briefly focus on the different steps of the fabrication process of the HEMTs. In particular, we will highlight the optimization done for some processing steps which helped producing transistors having sub micrometric gates and then reaching low leakage current and high breakdown voltage.

These technologies, developed for applications in the millimeter wave range (frequency range from $30 GHz$ to $300 GHz$), include technological specificities such as a gate length of $150 nm$ and below. In such conditions, it can be shown that the barrier layer thickness must be less than $10 nm$ in order to respect the transistor aspect ratio (gate length L_G over barrier thickness ratio t_{bar}) coupled with a good carrier density N_s in the channel. The aspect ratio between the gate

length and the AlGa_N barrier thickness should ideally be greater than 15 for the AlGa_N / Ga_N HEMT in order to prevent short channel effects while improving the static and microwave performances of the component [2]. Indeed, such short gate lengths, are accompanied by the appearance of parasitic electrostatic effect, known as "the short channel", which heavily affect both the DC and the RF performances of the device [17-19]. This effect disturbs the good control by the voltage V_{GS} of the conductivity between the source and the drain, which contributes to the degradation of the transconductance. Additionally, it contributes to the increase of the output conductance, limiting the performance in terms of cut-off frequencies. Respecting the aspect ratio quantity improves the gate control on the channel and considerably reduces the transistor output conductance. Electron-beam lithography enables processing patterns with a resolution around ten nanometers.

The HEMTs studied in the framework of this thesis have a standard topology with two gate fingers, two source contacts and a drain contact.

Figure 2.4 shows the schematic representation of a coplanar transistor.

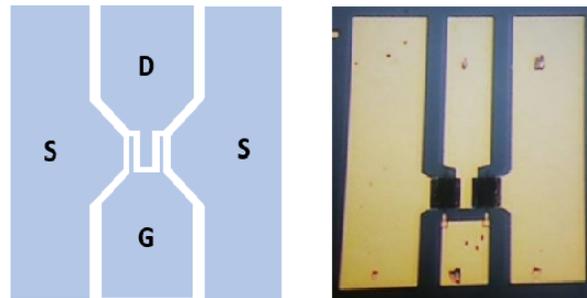


Figure 2.4: Schematic representation of a coplanar transistor

The main technological steps are chronologically described in the following.

2.3.1 Alignment marks

The alignment marks correspond to reference points on the sample in order to position the electron beam and consequently align and write the different mask levels with a theoretical resolution of 5 nm.

The electro sensitive resin bilayer used leads to obtain a cap-shaped profile after chemical revelation, which promotes the lift-off operation after metallization by evaporation of a metal stack of Molybdenum / Nickel / Molybdenum (20 / 40 / 70 nm). The composition of this stack of metals is imposed by the fact that Molybdenum (Mo) is a highly constrained refractory metal, which has a melting point of 2617 °C. Thus, a thin layer of Nickel (Ni), which has a melting temperature of 1450 °C, is inserted between two layers of Molybdenum (Mo) in order to moderate the Mo layer inner strain. The thickness of the each metal layer is chosen so as to obtain a sufficiently high

contrast between the masker and the semiconductor surface.

However, after the ohmic contacts annealing at a temperature above 850 °C, the surface of the Mo-based marks becomes very rough and the contrast of the mask with the semiconductor surface is deteriorated. This makes the research phase of the marks very complex especially when in the case of aligning the gate between the drain and the source contacts.

In order to solve this penalizing contrast problem, a thin layer of 10 nm Gold (Au) was added to the Molybdenum based stack during evaporation. The new gate metal stack is thus composed of Mo / Ni / Mo / Au.

2.3.2 Ohmic contact formation

An ohmic contact is a metal / semiconductor contact having a linear and symmetric current-voltage characteristic. In order to achieve power and frequency performances, it is necessary to reduce the resistivity of these contacts, surface roughness and steep sides.

As for the alignment marks, an electron-beam lithography was carried out to fabricate the ohmic contacts.

The sample is introduced into the vacuum metallization room where an in-situ IBE (Ion Beam Etching) is performed. This technique allows to carry out a soft in-situ physical etching in the metallization system, ensuring the maintenance of the sample in a clean environment throughout the metallization process duration.

An optimum contact resistance is obtained when around 75 % of the barrier is etched [20]. The etching step is necessary in order to bring the metal stack closer to the nearest conduction channel 2D without degrading the GaN layer. Then, a metallization Ti / Al / Ni / Au (12 / 200 / 40 / 100 nm) is deposited by evaporation.

The titanium (Ti), the first deposited metal, also acting as a bonding layer, is at the origin of the formation of TiN alloy after annealing at the interface between the metal contact and the semiconductor. This alloy has a lower electron work function than that of the nitride barrier. Then, the TiN formation generates nitrogen vacancies in the barrier that act as donor centers. A local n-type "pseudo-doping" of the barrier layer then appears. However, the donor concentration is inversely proportional to the barrier effective thickness. Consequently, since the barrier thickness decreases under the doping effect, the electrons passage is favored by tunneling effect, thus resulting in a low contact resistance.

The aluminum (Al) layer allows to form a Ti-Al alloy at the interface with the titanium. This alloy reduces the reactivity between titanium and GaN, and thus prevents the formation of vacancies at the interface due to the migration of gallium [21].

The nickel (Ni) avoids the formation of compounds between gold and aluminum which is crucial to avoid the purple plague. It acts as a diffusion barrier. The surface layer is made of gold (Au) in

order to distribute the current homogeneously over the entire surface of the contact and benefit from its excellent electrical conductivity. The ohmic contact was then rapid thermal annealed (RTA) in the temperature range of 800-900 °C for 30 s.

2.3.3 Device isolation

The purpose of the isolation is to delimit the operating area of each transistor. This isolation can be carried out in two different ways: by physico-chemical etching (mesa technology) or by ion implantation (planar technology). Within the framework of this work planar technology was used.

The choice of the ions to be implanted depends on the material nature. In the case of AlGaIn/GaN heterostructures, the elements mostly used are argon, helium, nitrogen or oxygen [22-24]. This process leads to break the crystalline continuity of the implanted material and to make the semiconductor amorphous in order to eliminate any parasitic conduction. The ion implantations were initially carried out by implantation of He^{2+} ions and then in order to reduce the costs, the helium implantation was replaced by nitrogen. Optimization of energies and implantation doses was developed internally at IEMN. The choice of optical lithography is justified by the low resolution required by this step.

2.3.4 Gate formation

In our case, the surface layer consists of AlGaIn unintentionally doped (n-type). It is therefore necessary that the metal constituting the Schottky contact has an electron work function higher than the electron affinity of the semiconductor at the surface.

The necessity of reducing the gate length for the component frequency rise leads to an increase in the gate resistance and consequently reduces the component performances, in particular the cutoff frequency (f_T), the maximum oscillation frequency (f_{MAX}) and the power gain. To alleviate this problem, a modification of the gate shape is necessary [25]

The use of electron-beam lithography, associated with specific resists bilayers, enabled to obtain T-shape gate (Figure 2.5). A Schottky Ni / Au metal stack was used.

Achieving gate lengths of less than 100 nm required optimization of the technological process which is composed of two steps: The first one consists in writing the gate cap to the electronic mask followed by a double development of resins PMMA 3 % 450 K and PMMA (MAA 33%). The second step involves a second writing in order to define the gate foot followed by a last development enabling the foot opening. Figure 2.5 shows a SEM image of T-shape gate of a device under test.

The next step of the gate contact metallization is a crucial step in the technological process of the HEMTs, which must combine a high Schottky barrier height with the lowest possible reverse leakage current associated with low resistance.

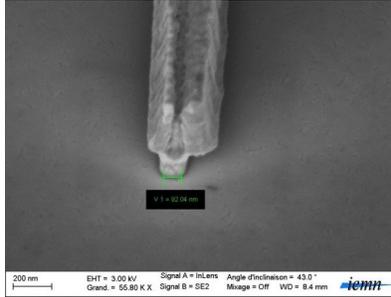


Figure 2.5: SEM image of T-shape gate with a gate foot of 100 nm [26]

For HEMT structures presented in this work, Ni / Au metal stack was used (40 nm / 300 nm). Nickel is used as a Schottky contact with a work function of the order of 5.15 eV [27], ensuring a reasonable Schottky barrier height and the gold is deposited to ensure a good electrical contact and reduce the gate resistance. The T-shape gate is finally obtained by lift-off.

Figure 2.6 shows the descriptive diagram of the technological realization of T-gate.

The current development of gate technologies dedicated to HEMT components is increasingly focusing on “self-aligned” gate technology. This has the advantage of considerably reducing the distance between the source and the drain contacts and a fortiori the gate-source distance in order to increase the microwave performances of the components. This technology consists in first realizing the gate electrodes and then in a second step in aligning the source and drain contacts with the gate. This technological process, combined with the production of regrowth ohmic contacts, which can drastically reduce contact resistance and surface roughness, has been demonstrated by several research groups [28,29]. With this technology, gate-source distances of the order of 50 nm can therefore be realized, associated with gate lengths of 20 nm, leading to extremely high cut-off frequencies (f_T/f_{MAX} : 454/444 GHz) [30].

2.3.5 Passivation

The improvement of the devices leads to a mandatory step of surface passivation by a dielectric layer. Then, an additional step of dielectric etching follows to access the contacts. However, the choice of the dielectric must meet many parameters; a high resistivity, a high breakdown electric field for a rise in frequency, satisfactory electrical permittivity for a better homogeneity of the field. Therefore, numerous studies have been carried out on the III-N semiconductors to find a suitable insulator [31,32], such as the SiO_2 for silicon.

Devices were passivated in this work with PECVD with 50 nm Si_3N_4 / 100 nm SiO_2 at 340 °C with a plasma pretreatment. These two materials permit to reduce the impact of the surface traps on the transistor. Si_3N_4 is used to passivate the semiconductor surface by essentially

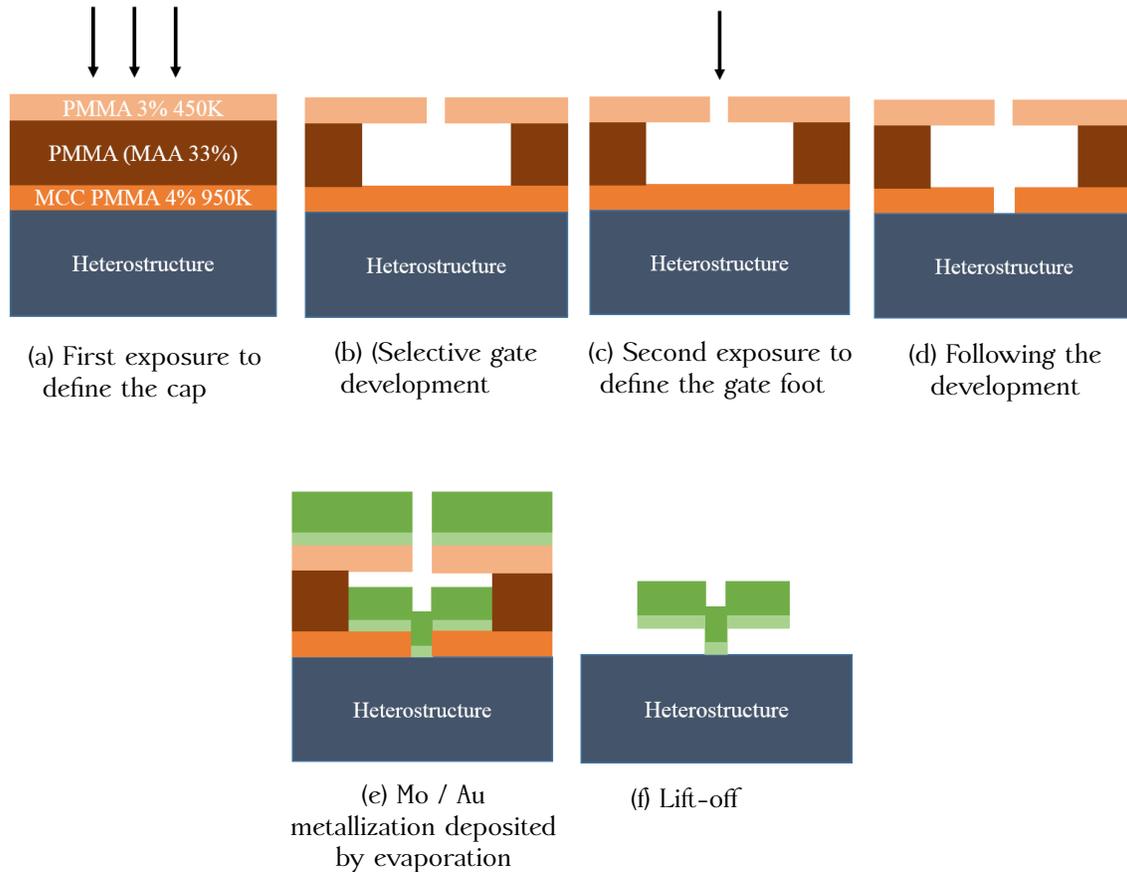


Figure 2.6: Descriptive diagram of the technological realization of T-gate with the different steps; electronic writing, selective development, metallization and lift-off

reducing nitrogen vacancies. SiO_2 is used in order to prevent tension strain generated by Si_3N_4 .

2.3.6 Pads thickening

The pads thickening step permits to connect the two gate fingers and makes source and drain easily accessible. The production of these pads is carried out by optical lithography using a bilayer of photosensitive resins in two steps. A metallization Ti / Au is then deposited by evaporation, followed by a lift-off step. Figure 2.8 summarizes the main technological steps of HEMT transistor.

Figure 2.8 summarizes the main technological steps of HEMT transistor.

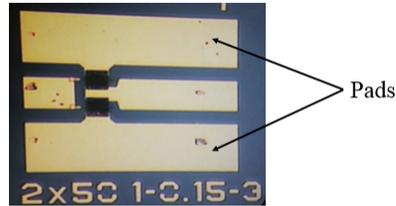


Figure 2.7: summarizes the main technological steps of HEMT transistor

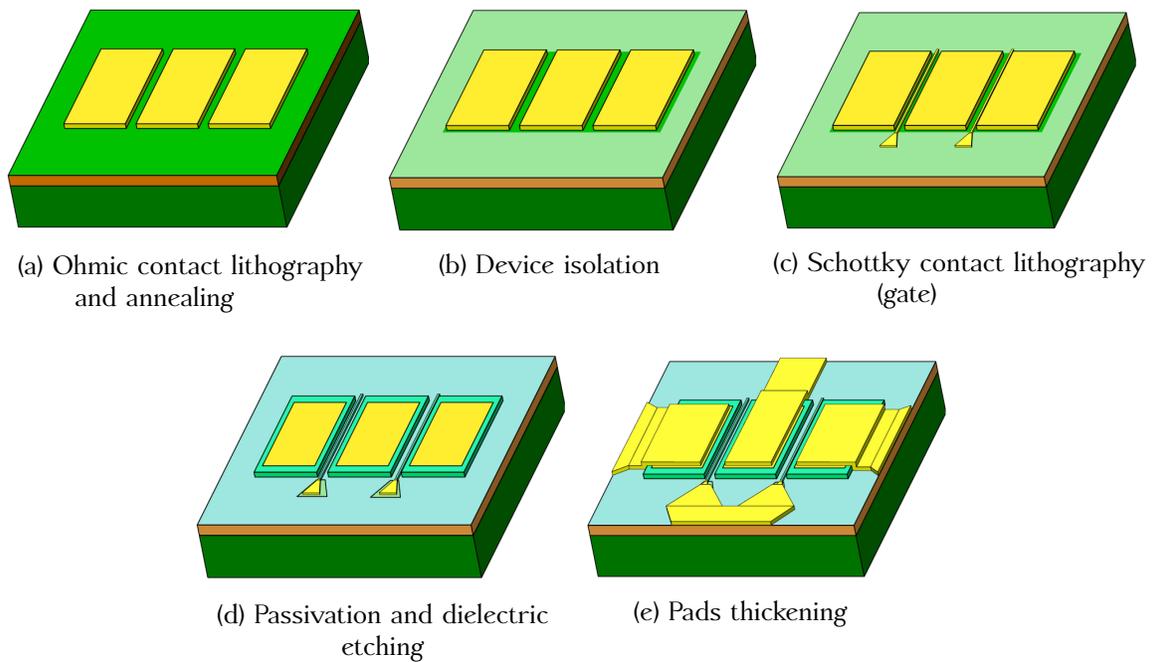


Figure 2.8: Descriptive diagram of the technological realization of T-gate with the different stages; electronic writing, selective development, metallization and lift-off [33]

2.4 DC characterization

Static measurement is usually the first step in the electrical characterization of the device. This section is dedicated to the DC characterization of AlGaIn/GaN MOCVD and AlGaIn/GaN MBE HEMT technologies under study. The objectives are the analysis of the static performances of the devices and the identification of the undesirable effects which can be at the origin of electrical anomalies such as short channel effects.

2.4.1 Experimental procedure for I-V characterization

2.4.1.1 Experimental setup

The DC measurements are carried out by a HP 4142B semiconductor parameter analyzer using ICCAP KEYSIGHT software. The measurements are performed by using TTPX Lakeshore cryogenic probe station with a temperature range from 80 K to 475 K [34].

In the context of this research study, the fabricated devices are "normally on", i.e., since the source / drain channel is conducting while the HEMT is at equilibrium.

Figure 2.9 (a) shows the cryogenic probe station and (b) shows RF and DC probes located on a transistor during DC measurement.

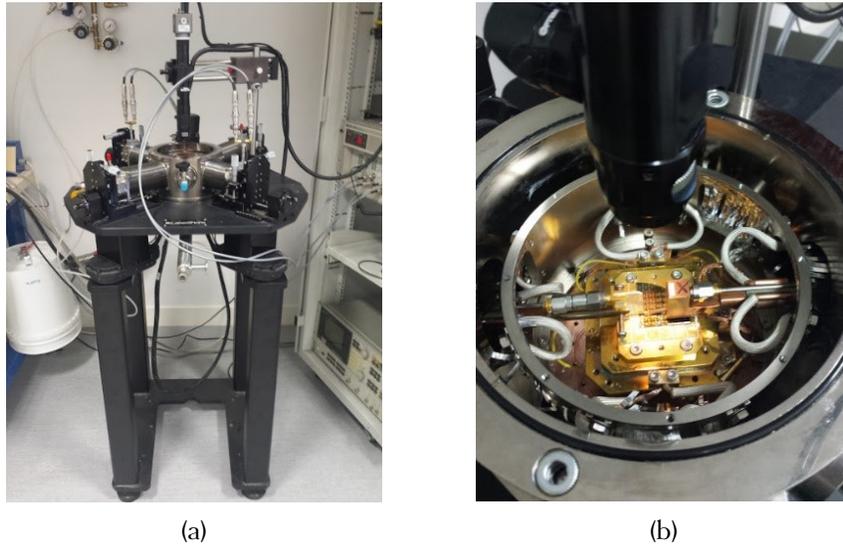


Figure 2.9: (a) TTPX Lakeshore cryogenic probe station, (b) AlGaIn/GaN HEMT wafer under electrical testing

DC measurements were carried out in both research laboratories, IMS Bordeaux and IEMN Lille. The comparison of the DC data extracted in both laboratories from the same samples, have allowed to highlight the influence of few parasitic effects depending on the experimental setup.

2.4.1.2 AlGaIn / GaN HEMT characterization

The main electrical measurements address the drain and gate currents which are expressed as a function of the gate or drain voltages.

From I-V characteristics; gate Schottky diode characteristics $I_{GS}(V_{GS})$ and drain output characteristics $I_{DS}(V_{DS})$ are measured permitting to deduce the transfer and transconductance characteristics $I_{DS} - G_M(V_{GS})$ and various parameters such as the drain current saturation, I_{DSS} , the

Schottky gate barrier height, ϕ_B , its ideality factor, η , the reverse gate current I_{GINV} , the HEMT threshold voltage, V_{TH} , the ohmic contact resistance, R_C , the HEMT resistance, R_{DS} in ohmic regime. This analysis, presenting performance indicators, provide also insight into components parameter dispersion.

- Gate Schottky diode characteristics $I_{GS}(V_{GS})$ (Input characteristic)

The study of the gate current via the $I_{GS}(V_{DS}, V_{GS})$ characteristic is the best way to evaluate the quality of the Schottky gate contact.

In the diode configuration (at $V_{DS} = 0$), a V_{GS} voltage is applied in both direct ($V_{GS} > 0$) and reverse bias conditions ($V_{GS} < 0$). In such condition, and considering that the current raises from a thermionic process, the gate current of the Schottky diode can be expressed by [35]:

$$I_G = I_S \left\{ \exp \left[\frac{q(V_{GS} - R_S I_G)}{\eta k_B T} \right] - 1 \right\} \quad (2.2)$$

The equation 2.2 can be reduced to the following equation, if $V_{GS} \gg R_S I_G$,

$$I_G = I_S \left(e^{\frac{qV_{GS}}{\eta k_B T}} - 1 \right) \quad (2.3)$$

Where V_{GS} is the applied voltage, η is the ideality factor of the diode, T is the temperature in K , k_B is the Boltzmann constant ($1.38 \times 10^{-23} \text{ J/Ks}^2$), q is the elementary electric charge ($1.602 \times 10^{-19} \text{ C}$) and I_S is the reverse saturation current derived from the straight line intercept of the current at zero bias given by equation (2.2)

$$I_S = S A^* T^2 e^{\frac{-q\phi_B}{k_B T}} \quad (2.4)$$

Where S is the Schottky contact area and A^* is the effective Richardson constant ($31.27 \text{ Acm}^{-2} \text{ K}^{-2}$ for $Al_{0.3l}Ga_{0.69}N$ and $30.95 \text{ A.cm}^{-2} \text{ .K}^{-2}$ for $Al_{0.29}Ga_{0.71}N$) that can be written as:

$$A^* = 4\pi q m_e^* m_0 k_B^2 h^{-3} \quad (2.5)$$

Where m_e^* is the effective mass, $m_0 = 9.1 \times 10^{-31} \text{ kg}$ and h is the Planck's constant, $h = 6.62 \times 10^{-34} \text{ Js}$.

The electron effective mass depends on Al mole fraction and is calculated by the following formula [36]:

$$m_{e,AlGaN}^*(x) = (0.22 + 0.13x)m_0 \quad (2.6)$$

A logarithmic representation of the characteristic $I_G(V_{GS})$ enables a linear extrapolation of

the linear coefficient, α , and the intercept at the origin, β , permit to get the barrier height, ϕ_B , and the ideality factor, η , following the equations (2.7) and (2.8):

$$\phi_B = \frac{k_B T}{q} \ln \left(\frac{S A^* T^2}{\beta} \right) \quad (2.7)$$

$$\eta = \frac{1}{\ln(10) \alpha \frac{k_B T}{q}} \quad (2.8)$$

Another parameter, which can be extracted from $I_{GS}-V_{GS}$ characteristic in reverse mode is the gate leakage current I_{GINV} as illustrated in Figure 2.10.

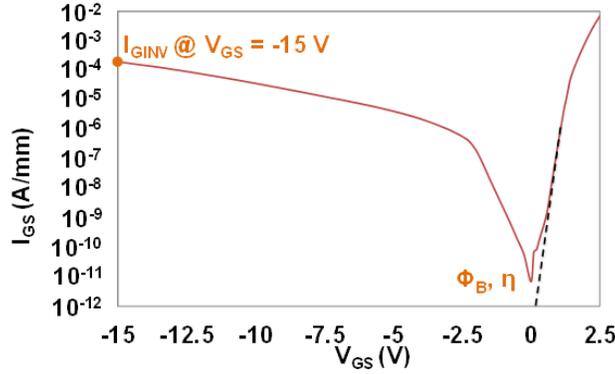


Figure 2.10: Typical I_{GS} (V_{GS}) characteristic of GaN HEMT

- Drain output characteristics I_{DS} (V_{DS})

Figure 2.11 shows a typical I_{DS} (V_{DS}) characteristic of a HEMT under test. There are thus two operating regions: the linear region for which the drain current is proportional to the drain-source voltage and the saturation region for which the current I_{DS} remains quasi-independent of the voltage V_{DS} . It is used to determine graphically the saturation drain current I_{DSS} and the drain-source resistance R_{DS} .

The saturation current I_{DSS} is the drain current measured at $V_{GS} = 0$ and at V_{DS} such as the device operates in saturation regime (at $V_{DS} = 10$ V in Figure 2.11). The resistance R_{DS} is given by the following equation:

$$R_{DS} = \left(\frac{\Delta V_{DS}}{\Delta I_{DS}} \right)_{V_{GS}=0, V_{DS} \rightarrow 0} \quad (2.9)$$

- Transfer and transconductance characteristics $I_{DS}-G_M$ (V_{GS})

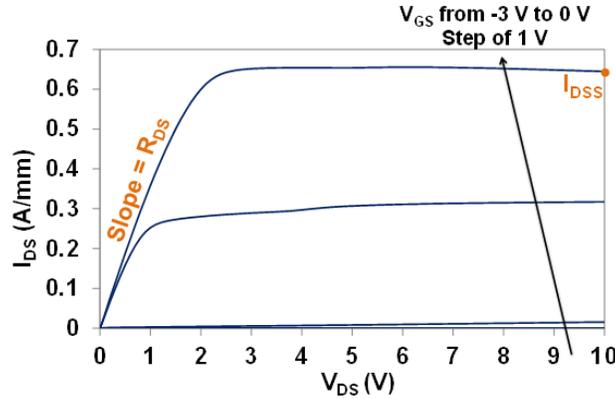


Figure 2.11: Typical I_{DS} (V_{DS}) characteristic of GaN HEMT

From the measurement of the transfer characteristics I_{DS} (V_{GS}) the threshold voltage (V_{TH}) can be graphically extracted.

There are several methods for determining the threshold voltage:

- Tangent extrapolation method: considering the quasi-linear part of the characteristic I_{DS} (V_{GS}), the intersection of the tangent and the abscissa axis gives the value of the threshold voltage.
- Quadratic extrapolation method: is also called as "Linear Extrapolation in Saturation Region". The I_{DS} for linear region is proportional to $(V_{GS} - V_{TH})$. Similarly, I_{DS} in saturation region is proportional to $(V_{GS} - V_{TH})^2$. Hence V_{TH} can be extracted by extrapolating the curve $\sqrt{I_{DS}}$ versus V_{GS} at the inflexion point of the curve.
- Current extrapolation method: The threshold voltage value is the V_{GS} value corresponding at $I_{DS} = 1\%$ of I_{DSS} . This method is mainly used by designers.

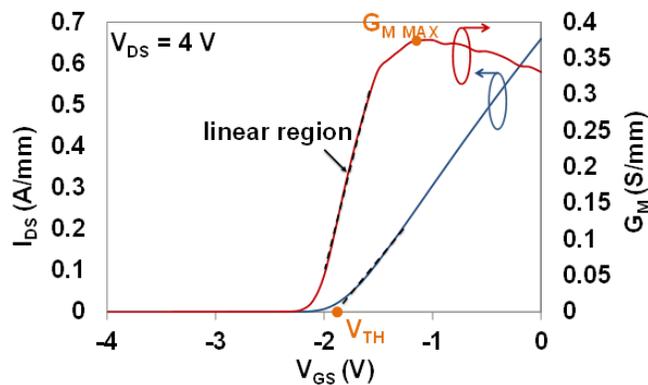


Figure 2.12: Typical I_{DS} - G_M (V_{GS}) characteristic of GaN HEMT

It is also possible to obtain the transconductance G_M by derivative of the characteristic I_{DS}

(V_{GS}). Its expression is therefore of the following form:

$$G_M = \left(\frac{\Delta I_{DS}}{\Delta V_{GS}} \right)_{V_{DS}=Cste} \quad (2.10)$$

The transconductance can be expressed in linear region as a function of the transistor parameters according to the following expression.

$$G_M = \frac{W\mu}{L_G}(V_{GS} - V_{TH}) \quad (2.11)$$

Where W is the gate width, μ is the mobility in the channel and L_G is the gate length.

The transistor output conductance is expressed according to the following equation:

$$G_{DS} = \frac{1}{R_{DS}} = \left(\frac{\Delta I_{DS}}{\Delta V_{DS}} \right)_{V_{GS}=Cste} \quad (2.12)$$

The plotting of the transfer function of the component G_M as a function of the voltage V_{GS} for a fixed value V_{DS} shows three operating zones to appear:

For $V_{GS} < V_{TH}$, the carrier density in the channel is negligible (deserted channel) and the component is considered as turn-off.

When $V_{GS} > V_{TH}$, the carrier density in the channel increases and the drain current increases with the gate voltage to the optimum operating point which corresponds to the value of V_{GS} for which the transconductance is maximum G_{MMAX} , as illustrated in Figure 2.12.

Beyond the gate voltage corresponding to G_{MMAX} , the thermal effect, the presence of the defects as well as the increase of the source and the drain resistances [37], with drain current [38] lead to a decrease of G_M when V_{GS} approaches to 0 V. Therefore, it is possible from this characteristic to determine the polarization point (V_{GS} , V_{DS}) for which the transconductance is maximum G_{MMAX} .

Another interesting characteristic to be exploited is the variation of the drain current I_{DS} in logarithmic scale as a function of the gate voltage V_{GS} (2.13). Therefore, we can deduce the ON-OFF ratio of the transistor. It corresponds to the ratio between the on state drain current and the off state drain current. It is the figure of merit for having high performance (enhancement of I_{ON}) and low leakage power (reduction of I_{OFF}) for transistors. Typically, increased control of the gate over the channel causes very high ON-OFF ratios.

- TLM characterization

Each sub-reticle of the wafer parts contained several test devices including transmission line modules (TLMs).

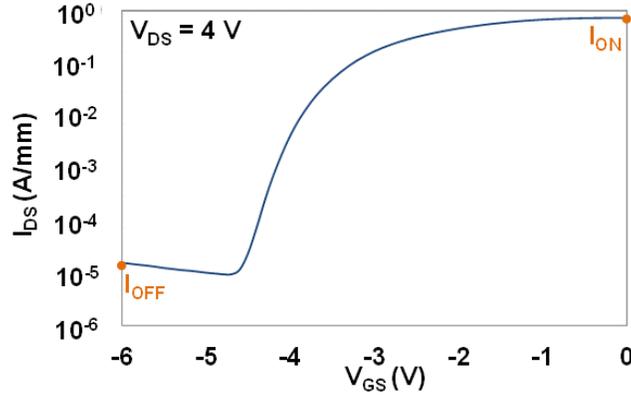


Figure 2.13: Logarithmic plot of a typical I_{DS} (V_{GS}) characteristic of GaN HEMT

There are several ways to measure the ohmic contact resistance at the metal/semiconductor interface, the most commonly technique consists of measuring the transmission line model (TLM) [39,40]. The TLM test structure consists of several electrodes fabricated on the epitaxial structure. These electrodes exhibit the same length (L) and width (W) separated by different semiconductor lengths d .

The TLM structure is described in Figure 2.14.

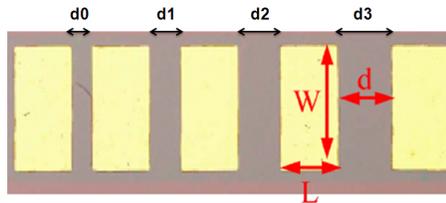


Figure 2.14: A Transmission Line Method (TLM) test structure

The I-V measurements are performed between two adjacent electrical contacts while the spacing between the electrodes (d) is varied.

The total resistance is given as [41]:

$$R_T = \frac{V}{I} = 2\frac{R_C}{W} + \frac{R_{\square}}{W}d \quad (2.13)$$

Where W is the width of the contacts, R_C is the contact resistance and R_{\square} is the sheet resistance between contacts.

In Figure 2.15, the measured resistances are plotted as a function of the distance of the electrode spacing d . Fitting Eq. 2.13, the values of the sheet resistance (R_{\square}) and the contact resistance (R_C) can be obtained.

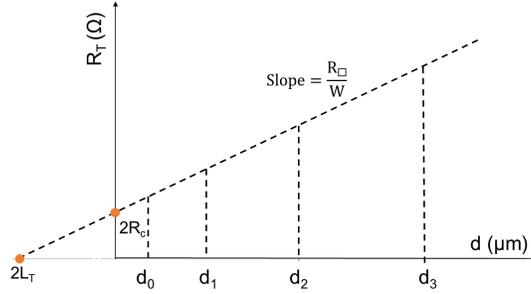


Figure 2.15: Plot of total resistance versus contact spacing to explain the TLM measurement technique

The specific contact resistance (ρ_C) is given by:

$$\rho_C = \frac{R_C^2}{R_\square} \quad (2.14)$$

The current transfer length (L_T) (also known as effective contact length), is the average distance that an electron (or hole) travels in the semiconductor beneath the contact before it flows up into the contact [42]. It is as follows:

$$L_T = \frac{R_C}{R_\square} \quad (2.15)$$

The optimization of ohmic contacts by reducing the contact resistance is one of the key points to optimize the performances of GaN-based devices

Table 2.1 summarizes previous described parameters and their extraction conditions which will be used to evaluate the dispersion and as initial values to follow their evolution during aging tests.

R_{DS} was defined as the resistance between source and drain at $V_{GS} = 0$, and V_{DS} of 0.5 V was chosen unrelated to potential applications.

Table 2.1: Electrical parameters and their extraction conditions

Parameters	Extraction conditions
I_{DSS}	$V_{DS} = 0 \text{ V}, V_{GS} = 10 \text{ V}$
R_{DS}	$V_{GS} = 0 \text{ V}, V_{DS} \rightarrow 0$
I_{GINV}	$V_{GS} = -15 \text{ V}$
G_{MMAX}	$V_{DS} = 4 \text{ V}$
V_{TH}	$V_{DS} = 4 \text{ V}$

2.4.2 AlGaIn/GaN MOCVD technology

2.4.2.1 Analysis of the dispersion of electrical characterization

Around one hundred devices and five TLM patterns from MOCVD growth have been characterized and will be presented in forthcoming paragraphs for the purpose of studying the electrical behavior and the dispersion of the electrical parameters of transistors under test. Table 2.2 presents the number of characterized devices per geometry.

Table 2.2: Number of characterized devices per geometry

Device geometry		N° of characterized devices
L_G (nm)	L_{DS} (μm)	
75	1.5	12
	2.5	7
	3.5	7
	4.5	7
	5.5	7
100	2.5	7
	3.5	7
	4.5	7
	5.5	7
150	2.5	7
	3.5	7
	4.5	7
	5.5	7

The wafer map that corresponding to AlGaIn/GaN MOCVD technology is shown in Figure 2.16.

The transistors under study have a total width of $2 \times 25 \mu m$, a gate-source distance of $600 nm$, a drain-source distance ranging from $1.5 \mu m$ to $5.5 \mu m$ and a gate length of 75 or 100 or $150 nm$.

- Gate Schottky diode characteristics $I_{GS}(V_{GS})$ (Input characteristic)

Figure 2.17 (a) shows $I_{GS}-V_{GS}$ characteristic of transistors with different geometry (different L_G and L_{DS}) at $V_{DS} = 0 V$ while V_{GS} was swept from $-15 V$ to $2.5 V$, while Figure 2.17 (b) shows $I_{GS}-V_{GS}$ characteristic of seven typical transistors with the same geometry ($L_G = 75 nm$, $L_{DS} = 5.5 \mu m$) in the same conditions.

Based on Figure 2.17 (a), the effective barrier height obtained according to equation (2.7), the ideality factor was deduced using equation (2.8) and the gate current I_{GINV} are given in Table 2.3.

The ideality factor is a significant indicator of the Schottky contact quality and / or the existence of conduction modes other than pure thermionic. If the thermionic effect is the main transport mechanism, the ideality factor is equal to 1 and in this case the contact is considered to be

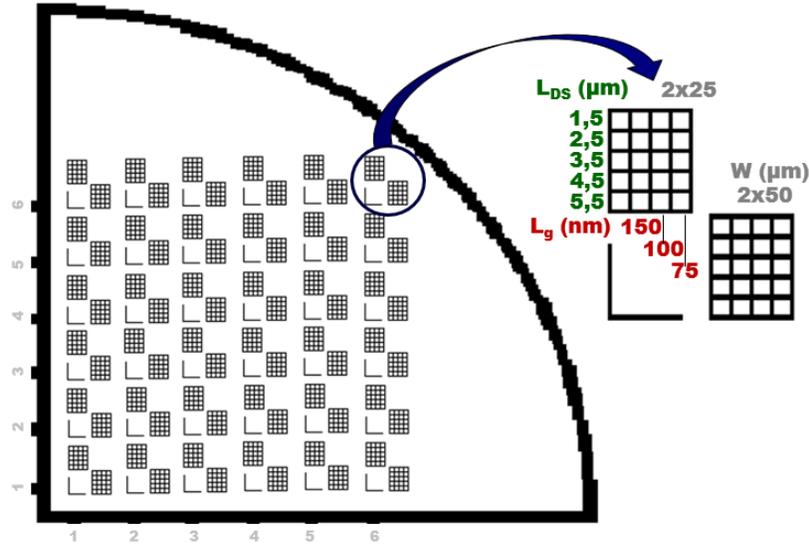
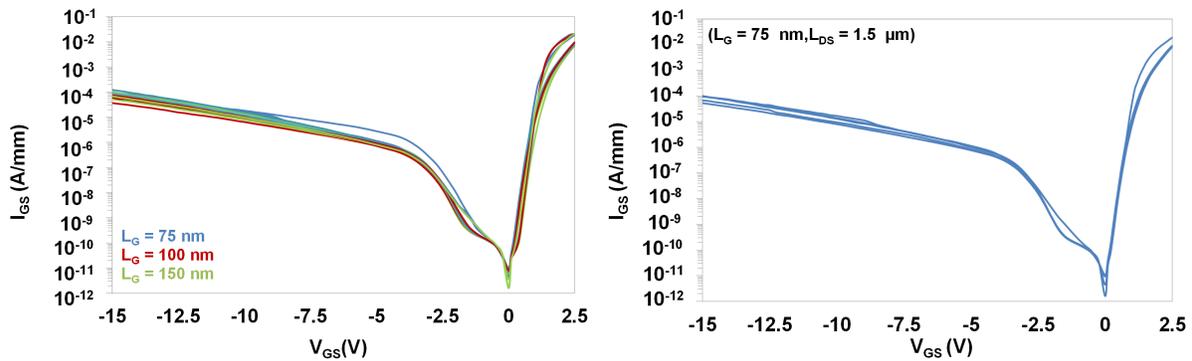


Figure 2.16: Wafer map of AlGaN/GaN MOCVD technology

Figure 2.17: I_{GS} - V_{GS} characteristics of different MOCVD HEMTs (a) and seven $5.5 \mu\text{m}$ drain-source distance and 75 nm gate length MOCVD HEMTs (b)

"ideal", which means theoretically without roughness and interface defects. The obtained ideality factor greater than 1, can be explained by the presence of defects and several other transport mechanisms including trapping / de-trapping mechanisms.

Figure 2.17 (a) shows that the input characteristics of samples with the same geometry ($L_G = 75 \text{ nm}$, $L_{DS} = 5.5 \mu\text{m}$) are not superimposed for $V_{DS} = 0 \text{ V}$. Therefore, a small dispersion is noticed.

- Drain output characteristics I_{DS} (V_{DS})

Figure 2.18 shows I_{DS} versus V_{DS} (a) for transistors with different geometry (different L_G and L_{DS}) and (b) for seven typical transistors with the same geometry ($L_G = 75 \text{ nm}$, $L_{DS} = 5.5 \mu\text{m}$),

Table 2.3: Barrier height ϕ_B , ideality factor η and gate current I_{GINV} of AlGaIn/GaN MOCVD technology

Parameters	AlGaIn/GaN MOCVD technology
ϕ_B (eV)	0.68 ± 0.025
η	2.54 ± 0.25
I_{GINV} (A/mm) @ $V_{GS} = -15$ V	$8 \times 10^{-5} \pm 5 \times 10^{-5}$

at gate voltage V_{GS} ranging from -5 V to 0 V and up to drain voltage $V_{DS} = 10$ V. It indicates that for a V_{GS} close to the pinch off, in saturation region, there is an increase in drain current as a function of drain-source electric field. This phenomenon is attributed to short channel effects. These latter are mainly attributable to low aspect ratios. Indeed, according to Jessen et al. [43], the short channel effects start to appear for aspect ratios lower than 15 and are considered modest up to aspect ratios of about 10.

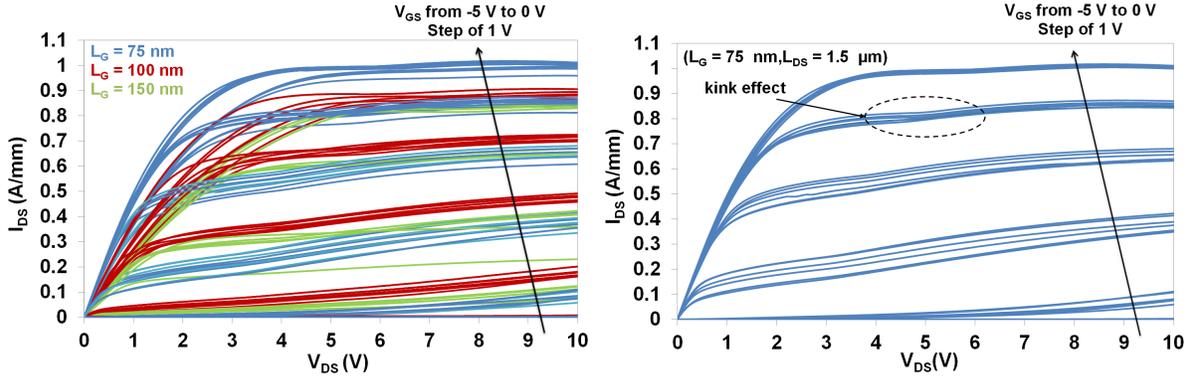


Figure 2.18: I_{DS} - V_{DS} characteristics (a) of different MOCVD HEMTs and (b) of seven $5.5 \mu\text{m}$ drain-source distance and 75 nm gate length MOCVD HEMTs

Using figure 2.18 (a), the resulting parameters value (I_{DSS} and R_{DS} and L_G/t_{bar}) are illustrated in table 2.4.

Table 2.4: Saturation current, R_{DS} resistance and aspect ratio of AlGaIn/GaN MOCVD technology

Parameters	AlGaIn/GaN MOCVD technology		
L_G (nm)	75	100	150
I_{DSS} @ $V_{GS} = 0$ V	0.96 ± 0.04	0.9 ± 0.02	0.83 ± 0.03
R_{DS} ($\Omega \cdot \text{mm}$)	1.86 ± 0.5	3.13 ± 0.3	3.6 ± 0.3
Aspect ratio L_G/t_{bar}	5	6.6	10

Figure 2.18 (b) illustrates the appearance of a small kink effect at $V_{GS} = -1$ V and $V_{DS} = 6$ V for gate voltages close to the threshold voltage. This is manifested with an increase of the drain

current.

Several works [44–47] have attributed this physical phenomenon to trapping and de-trapping processes associated with increasing drain current. It is noticed too that the output characteristics up to $V_{DS} = 10\text{ V}$ are not superimposed and then a small dispersion is noticed by a variation of I_{DSS} and R_{DS} . From the table 2.4, we can deduce that the short channel effects are low for HEMTs with L_G of 150 nm and more present for HEMTs with L_G of 75 and 100 nm.

- Transfer and transconductance characteristics $I_{DS}-G_M (V_{GS})$

The $I_D (V_{GS})$ and $G_M (V_{GS})$ characteristics of devices with different geometry are shown in Figure 2.19 (a) and of those of seven devices with the same geometry are shown in Figure 2.19 (b). V_{GS} is varying from -6 V to 0 V at a fixed V_{DS} voltage of 4 V .

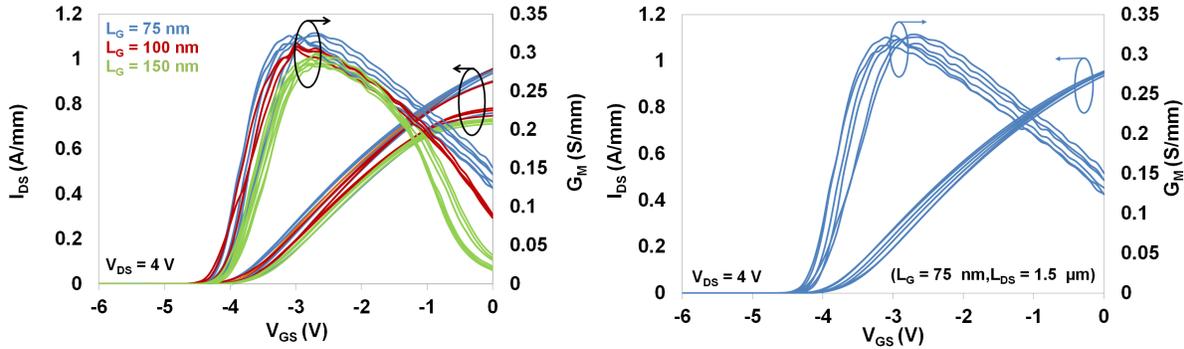


Figure 2.19: $I_{DS}-G_M (V_{GS})$ characteristics (a) of different MOCVD HEMTs and (b) seven $5.5\ \mu\text{m}$ drain-source distance and $75\ \text{nm}$ gate length MOCVD HEMTs

The ON and OFF drain current (a) of devices with different geometry and (b) of the seven aforementioned devices with the same geometry are plotted between drain current, in log scale in figure 2.20.

The transfer characteristic exhibited a peak G_{MMAX} at the bias point $(V_{GS}, V_{DS}) = (-2.9 \pm 0.2\text{ V}, 4\text{ V})$, which should deliver the best microwave performances, a threshold voltage V_{TH} , obtained using the tangent extrapolation method and ON-OFF ratio and their values are reported in Table 2.5.

Figure 2.20 (b) shows $I_{DS}-G_M$ versus V_{GS} characteristics of previous mentioned samples showing that for $V_{DS} = 4\text{ V}$ are not superimposed. all the DC characteristics of the $5.5\ \mu\text{m}$ drain source distance and the $75\ \text{nm}$ gate length samples are not superimposed. The same results were depicted for samples of other geometry. Therefore, dispersion of about 2 to 3 % is noticed for the devices with the same geometry.

The 55 devices having the most homogenous behavior were selected for RF measurements and accelerated aging tests.

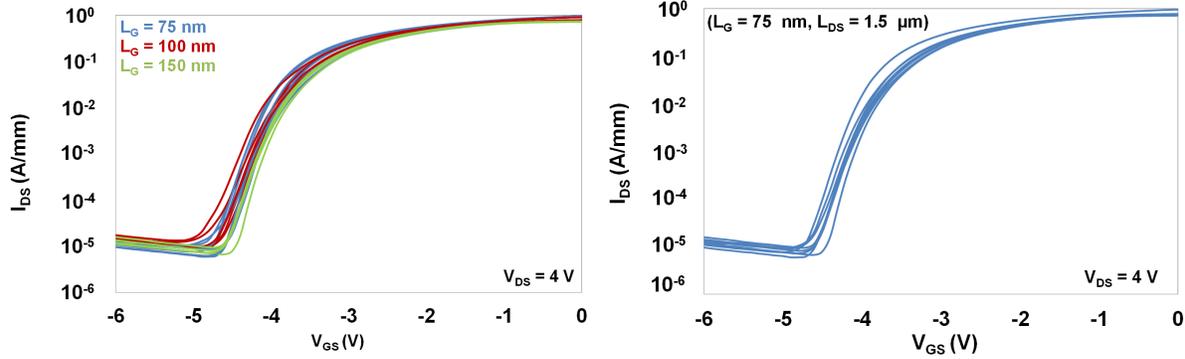


Figure 2.20: Logarithmic scale of I_{DS} (V_{GS}) characteristics (a) of different MOCVD HEMTs and (b) of seven $5.5 \mu\text{m}$ drain-source distance and 75 nm gate length MOCVD HEMTs

Table 2.5: Maximum transconductance, threshold voltage and ON-OFF ratio of AlGaN/GaN MOCVD technology

Parameters	AlGaN/GaN MOCVD technology		
L_G (nm)	75	100	150
G_{MMAX} (mS/mm) @ $V_{DS} = 6 \text{ V}$	0.31 ± 0.02	0.29 ± 0.01	0.27 ± 0.01
V_{TH} (V) @ $V_{DS} = 6 \text{ V}$	-3.9 ± 0.05	-3.8 ± 0.04	-3.7 ± 0.05
I_{ON}/I_{OFF}	$10^{4.9} \pm 10^{0.3}$		

- TLM characterization

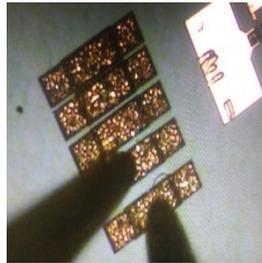


Figure 2.21: An optical picture of a TLM mask of MOCVD technology

A typical transfer length method (TLM) structure with contact separations of 2, 5, 10 and $20 \mu\text{m}$ and a total width W of $100 \mu\text{m}$ (Figure 2.21) has been characterized by varying the voltage from 0 to 4 V. Figure 2.22 presents the DC characteristic of a TLM structure.

The total resistance has been measured in ohmic regime at $V_{DS} = 0.5 \text{ V}$. Figure 2.23 shows the evolution of the total resistance as a function of the inter electrode distance d .

According to equations (2.14) and (2.15), the contact resistance, R_C , the sheet resistance, R_{\square} , and

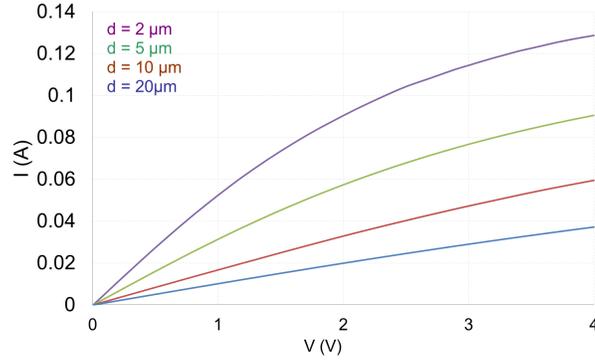


Figure 2.22: I-V characteristic of TLM structure

the transfer length, L_T , have been extracted and the typical values are reported in Table 2.6.

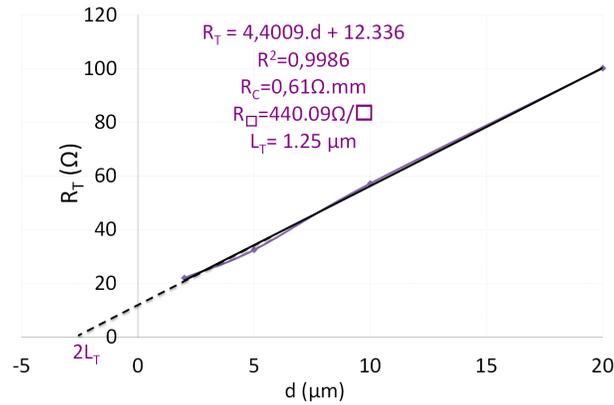


Figure 2.23: Resistance versus gap spacing and extraction of contact and sheet resistances from TLM patterns with spacing of 2, 5, 10 and 20 μm

The low value of ohmic contact resistance R_C is a good result for an alloyed ohmic contact and an indicator of the maturity of the technological process. A sheet resistance (R_\square) of 440 Ω/\square is a typical result reflecting the good quality of the epitaxial layers.

2.4.2.2 Impact of device geometry on static performances

In order to analyze the effect of the gate length, the drain-source distance and the gate-source distance on the component performances, we carried out a measurement campaign of on HEMTs of different topology. This section illustrates the impact of device geometry especially on the drain current saturation, I_{DSS} , the maximum transconductance, G_{MMAX} , the resistance R_{DS} and the threshold voltage, V_{TH} .

Table 2.6: Contact and sheet resistances of AlGaIn/GaN MOCVD technology

Parameters	AlGaIn/GaN MOCVD technology
R_C ($\Omega.mm$)	0.61
R_{\square} (Ω/\square)	440
L_T (μm)	1.25

The comparison of the results obtained as a function of the topology of the transistors presented in Figure 2.24 and 2.25 shows that the gate length, the drain-source distance and the gate-drain distance have a non-negligible impact on the static characteristics. As it can be seen, decreasing the gate length increases the drain current and consequently the transconductance peak value, and decreases the R_{DS} resistance and the threshold voltage leading to an improvement of the device performances. In particular, we can notice:

- At a fixed value of the gate length, the drain current and the extrinsic transconductance increases when the drain-source distance is decreasing. For instance, at $L_G = 75$ nm, when L_{DS} varies from 5.5 to 1.5 μm , the drain current saturation changes from 0.86 to 1 A/mm, and the extrinsic transconductance changes from 0.29 to 0.34 S/mm which represent an increase of 16 % and 17 % respectively.

- At a fixed the drain-source distance (varying as L_{GD}), the drain current and the extrinsic transconductance increases when the gate length is decreasing. For instance, at $L_{DS} = 5.5$ μm , when L_G varies from 150 to 75 nm, the drain current saturation changes from 0.81 to 0.9 A/mm, and the extrinsic transconductance changes from 0.26 to 0.3 S/mm, which represents an increase of 11 % and 15 % respectively.

- The drain current saturation I_{DSS} and the transconductance G_M are all the more high as the gate is close to the drain ($L_{GS} = Cst$). It is therefore necessary to reduce the distance between the source and the drain contacts in order to benefit of the maximum current density, while minimizing the transit times of the carriers.

Shorter L_G reduces the size of transistor and then increases the current density. Moreover, the path length traversed by the electrons decreased. It provides less resistance and lower surface-roughness scattering which leads to a higher transconductance and mobility. As the gate length will decrease, the performance will be better.

2.4.3 AlGaIn/GaN MBE technology

2.4.3.1 Analysis of the dispersion of electrical characterization

Twenty three devices and four TLMs grown by MBE have been characterized and will be presented in the next subsections. There are few devices available compared to the first technology owing

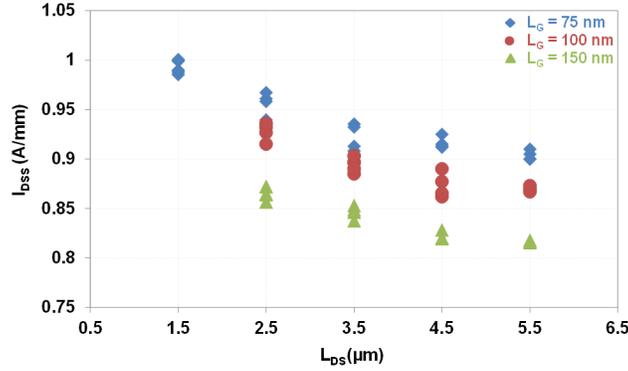


Figure 2.24: Impact of device geometry on drain current saturation of AlGaIn/GaN MOCVD technology

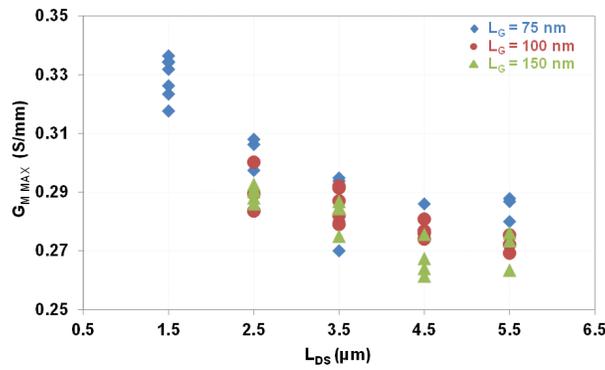


Figure 2.25: Impact of device geometry on maximum transconductance of AlGaIn/GaN MOCVD technology

to the manufacturing efficiencies and many technical problems encountered during measurement. These measurements were carried out in order to study the electrical behavior and the dispersion of the electrical parameters of the studied transistors along the wafer. Table 2.7 summarizes the number of characterized devices per geometry.

The wafer map of AlGaIn/GaN MBE technology is shown in Figure 2.26.

The transistors under tests have a total width of $2 \times 50 \mu\text{m}$, a drain-source distance of $2.65 \mu\text{m}$, a gate-source distance ranging from 1.13 to $1.23 \mu\text{m}$ and a gate length of 75 or 100 or 150 nm .

- Gate Schottky diode characteristics

Figure 2.27 (a) shows the transistor gate current as a function of the gate-source voltage V_{GS} of transistors with different geometry (different L_G and L_{GS}) at a drain-source voltage V_{DS} of 0 V while V_{GS} was swept from -15 V to 2.5 V , while Figure 2.27 (b) shows $I_{GS} - V_{GS}$ characteristic

Table 2.7: Number of characterized devices per geometry

Device geometry		N° of characterized devices
L_G (nm)	L_{GS} (μm)	
75	1.18	2
	1.23	4
100	1.15	2
	1.2	5
150	1.13	3
	1.18	7

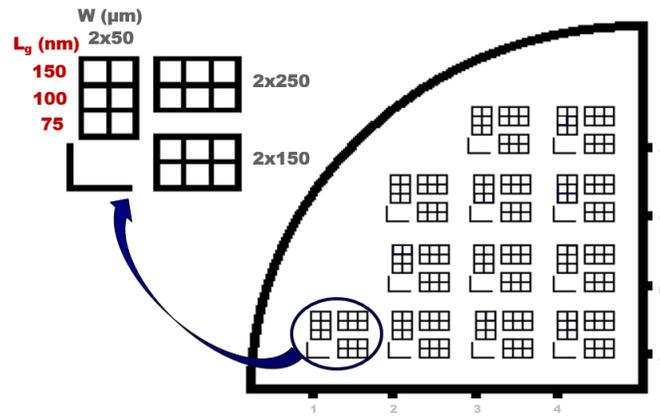
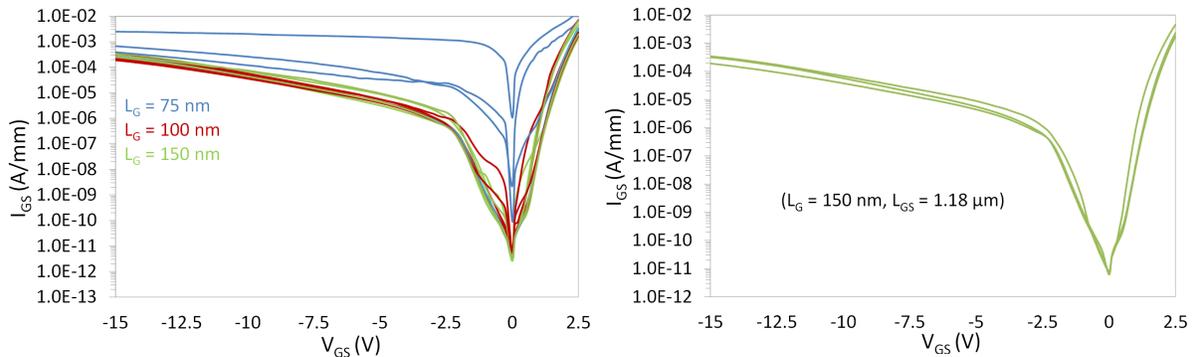


Figure 2.26: Wafer map of AlGaN/GaN MBE technology

of three typical transistors having the same geometry ($L_G = 150 \text{ nm}$, $L_{GS} = 1.18 \mu\text{m}$) in the same conditions.

Figure 2.27: I_{GS} - V_{GS} characteristics of (a) MBE transistors with different geometry (left), and (b) three $1.18 \mu\text{m}$ gate-source distance and 150 nm gate length MBE HEMTs

The resulting value of the effective barrier height and the ideality factor obtained according

to equations (2.7) and (2.8), and the gate leakage current I_{GINV} are reported in Table 2.8.

Table 2.8: Barrier height, ideality factor and I_{GINV} of AlGaIn/GaN MBE technology

Parameters	AlGaIn/GaN MBE technology
ϕ_B (eV)	0.55 ± 0.15
η	4.54 ± 1
I_{GINV} (A/mm) @ $V_{GS} = -15$ V	$126 \times 10^{-4} \pm 123 \times 10^{-4}$

Figure 2.27 (b) shows that a small dispersion is noticed for the three samples of the same geometry.

- Drain output characteristics

I_{DS} versus V_{DS} for transistors with different geometry at V_{GS} ranging from -5 V to 0 V is shown in figure 2.28 (a), and three samples with the same geometry ($L_G = 150$ nm, $L_{GS} = 1.18$ μ m) is shown in figure 2.28 (b).

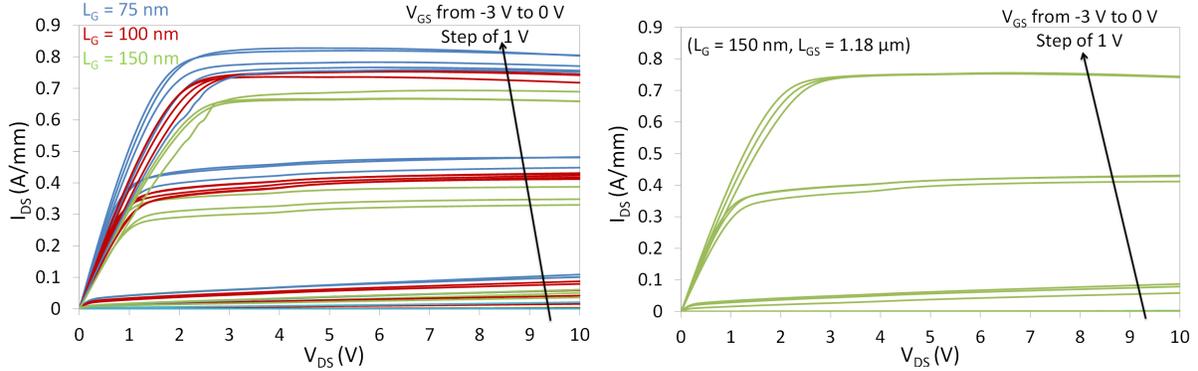


Figure 2.28: I_{DS} - V_{DS} characteristics of MBE transistors with different geometry (a), and three 1.18 μ m gate-source distance and 150 nm gate length MBE HEMTs (b)

Using figure 2.28 (a), the drain current saturation I_{DSS} , R_{DS} resistance and aspect ratio are given in Table 2.9.

Table 2.9: Barrier height, ideality factor and aspect ratio of AlGaIn/GaN MBE technology

Parameters	AlGaIn/GaN MBE technology		
L_G (nm)	75	100	150
I_{DSS} @ $V_{GS} = 0$ V	0.82 ± 0.03	0.72 ± 0.04	0.62 ± 0.04
R_{DS} (Ω .mm)	1.6 ± 0.4	2.87 ± 0.3	3.8 ± 0.5
Aspect ratio L_G/t_{bar}	7.5	10	15

Figure 2.28 (b) shows that the output characteristics of the aforementioned three samples are not superposed for V_{GS} from $-5 V$ to $0 V$. A small dispersion is noticed.

From the table 2.9, we can deduce that the short channel effects are negligible for HEMTs with L_G of $150 nm$, low for HEMTs with L_G of $100 nm$ and more present for HEMTs with L_G of $75 nm$.

- Transfer and transconductance characteristics

The measured current and transconductance characteristics of devices with different geometry are shown in Figure 2.29 (a) and of those of three aforementioned devices with the same geometry are shown in figure 2.29 (b). V_{GS} is varying from $-6 V$ to $0 V$ at a fixed V_{DS} voltage of $4 V$. The transfer characteristic exhibited a peak G_{MMAX} of $0.38 \pm 0.03 S/mm$ at the bias point ($-1.2 V$, $4 V$) and a threshold voltage V_{TH} of $-1.95 \pm 0.15 V$.

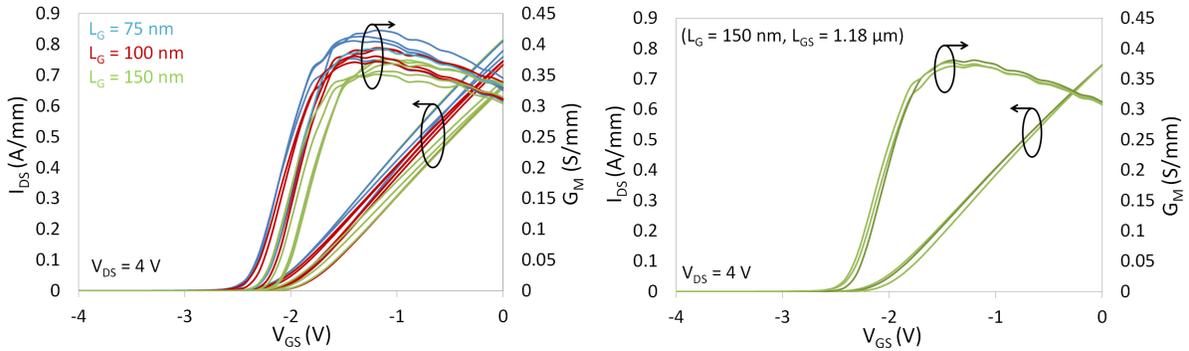


Figure 2.29: $I_{DS} - G_M (V_{GS})$ characteristics of (a) MBE transistors with different geometry, and (b) three $1.18 \mu m$ gate-source distance and $150 nm$ gate length MBE HEMTs

The ON and OFF drain currents (a) of devices with different geometry and (b) of the three aforementioned devices with the same geometry are plotted between drain current, in log scale in 2.30.

The resulting parameters value from the figure 2.29 (b): G_{MMAX} at the bias point V_{GS} ($-1.1 \pm 0.2 V$, $4 V$), the threshold voltage V_{TH} ON-OFF ratio are reported in Table 2.10.

Figure 2.29 (b) shows $I_{DS}-G_M$ versus V_{GS} characteristics for $V_{DS} = 4 V$ of previous mentioned samples that are not superimposed.

All the DC characteristics of the $1.18 \mu m$ gate source distance and the $150 nm$ gate length samples are not superimposed. The same results were depicted for samples of other geometry. Therefore, a dispersion of about 1 to 3 % is noticed.

The most homogenous 14 devices were selected for RF measurements and next accelerated aging tests.

- TLM characterization

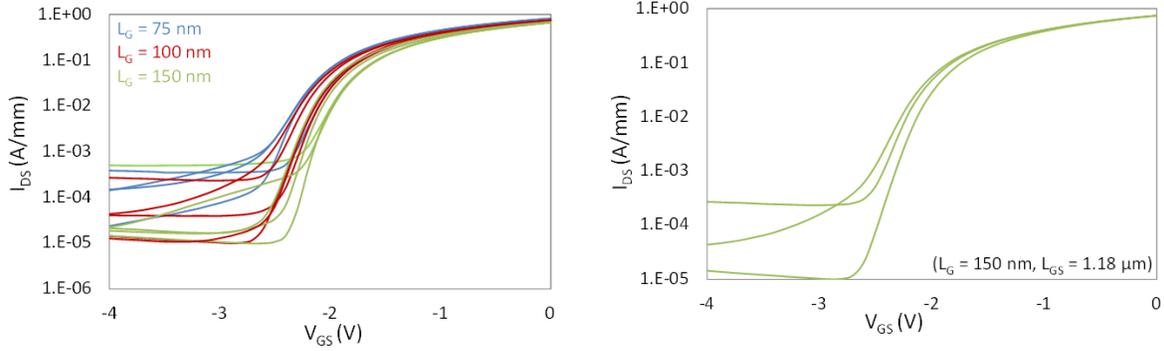


Figure 2.30: Logarithmic plot of I_{DS} -Gm (V_{GS}) characteristics (a) of MBE transistors with different geometry, and (b) three 1.18 μm gate-source distance and 150 nm gate length MBE HEMTs

Table 2.10: Maximum transconductance, threshold voltage and ON-OFF ratio of AlGaIn/GaN MBE technology

Parameters	AlGaIn/GaN MBE technology		
L_G (nm)	75	100	150
G_{MMAX} (mS/mm) @ $V_{DS} = 6$ V	0.4 ± 0.01	0.38 ± 0.02	0.32 ± 0.03
V_{TH} (V) @ $V_{DS} = 6$ V	-2.05 ± 0.05	-1.9 ± 0.05	-1.8 ± 0.05
I_{ON}/I_{OFF}	$10^{4.1} \pm 10^{0.7}$		

Transfer length method (TLM) structure with contact separations of 2, 5, 10 and 20 μm , total width of 100 μm and layout similar to HEMT grown by MBE was characterized (Figure 2.31).

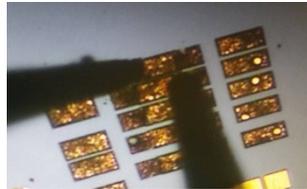


Figure 2.31: An optical image of TLM mask of MBE technology

Figure 2.32 presents DC characteristic of a TLM structure.

It can be seen that the ohmic regime occurs especially for short lengths, that is why we have extracted the parameters of the TLM resistance at $V_{DS} = 0.5$ V.

A typical TLM extraction which gave an average value of contact resistance, R_C , of 0.67 $\Omega\cdot\text{mm}$, a sheet resistance, R_{\square} , of 237 Ω/\square , of and transfer length, L_T , of 2.75 μm , according to equations (2.14) and (2.15) is depicted in Figure 2.33 and Table 2.11. Measured ohmic contact resistance (R_C)

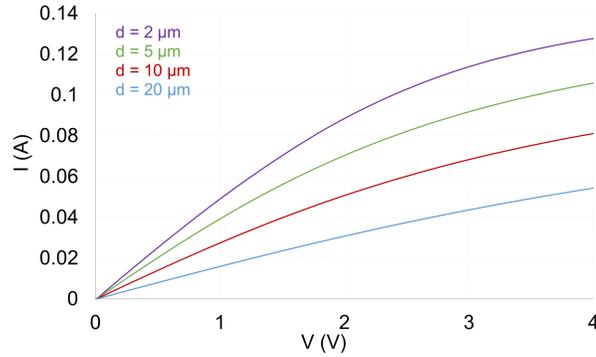
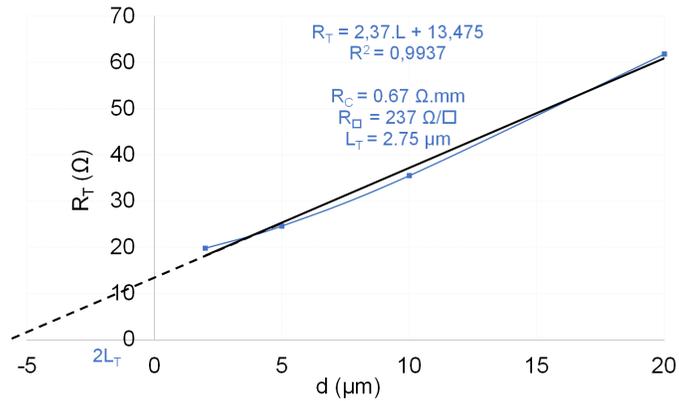


Figure 2.32: I-V characteristic of TLM structure

and sheet resistance (R_{\square}) are found good.

Figure 2.33: Measured resistance versus gap spacing and extraction of contact and sheet resistances from TLM patterns with the spacing of 2, 5, 10 and 20 μm

2.4.3.2 Impact of device geometry on static performances

Figure 2.34, figure 2.35, figure 2.36 and 2.37 show the results of the drain current saturation, I_{DSS} , the maximum transconductance, G_{MMAX} , the resistance R_{DS} and the threshold voltage, V_{TH} respectively. They are obtained as a function of the topologies of the transistors.

It's clear that the gate length, the gate-source distance and the gate-drain distance have a non-negligible impact on the static characteristics.

As it can be seen, decreasing the gate length increases the drain current and consequently the transconductance peak value, decreases the resistance R_{DS} and leads to a negative shift of the threshold voltage. In particular, we can notice:

Table 2.11: Contact and sheet resistances of AlGaIn/GaN MBE technology

Parameters	AlGaIn/GaN MBE technology
R_C ($\Omega.mm$)	0.67
R_{\square} (Ω/\square)	237
L_T (μm)	2.75

- At a fixed value of the gate length, the drain current and the transconductance increases with the gate-source distance increasing. For instance, at $L_G = 75$ nm, when L_{GS} varies from 1.13 to 1.18 μm , the drain current saturation changes from 0.65 to 0.8 A/mm, and the extrinsic transconductance changes from 0.37 to 0.42 S/mm, representing increase of 23 % and 13 % respectively.

- At a fixed value of the gate-source distance (varying inversely as L_{GD}), the drain current and the transconductance increases with the gate length decreasing. For instance, at $L_{GS} = 1.18$ μm , when L_G varies from 150 to 75 nm, the drain current saturation changes from 0.65 to 0.8 A/mm, and the extrinsic transconductance changes from 0.36 to 0.42 S/mm, which represents a decrease of 23 % and 16 % respectively.

- The drain current saturation I_{DSS} and the transconductance G_M are all the more high as the gate is close to the drain for a fixed L_{DS} . It is why it is necessary to reduce the gate-source distance and the drain-source distance to achieve maximum current density, while minimizing the transit times of the carriers.

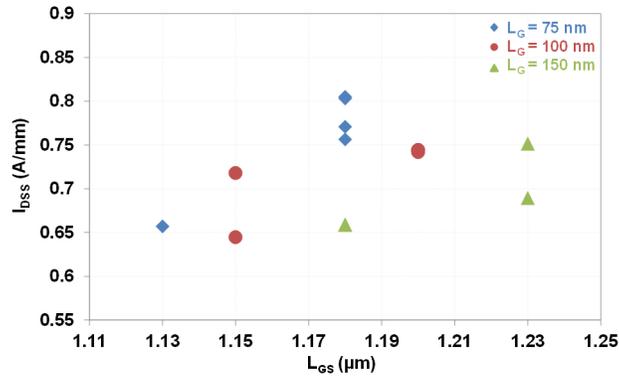


Figure 2.34: Impact of device geometry on drain current saturation of AlGaIn/GaN MBE technology

2.4.4 Comparison between both technologies

Table 2.12 summarizes key parameters comparison between both technologies reported in this study.

To give complementary insights, Figure 2.38 shows input characteristics of both technologies.

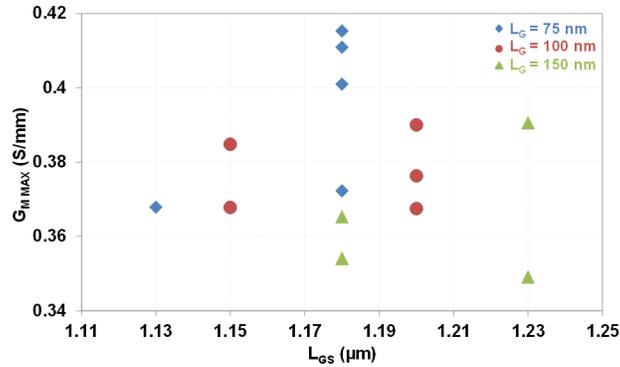


Figure 2.35: Impact of device geometry on maximum transconductance of AlGaIn/GaN MBE technology

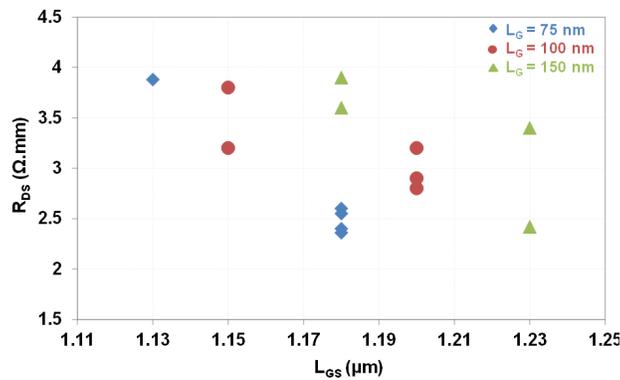


Figure 2.36: Impact of device geometry on on-resistance R_{DS} of AlGaIn/GaN MBE technology

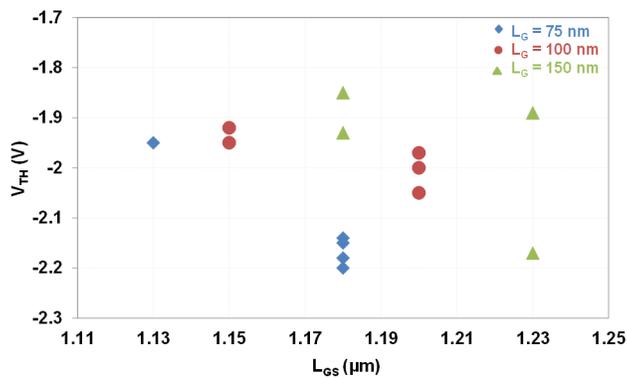


Figure 2.37: Impact of device geometry on threshold voltage of AlGaIn/GaN MBE technology

Figure 2.39 shows output characteristics of both technologies, the I_{DS} characteristic of the MBE technology is found very flat in saturation regime even though its current I_{DS} (A/mm) is

Table 2.12: Main electrical parameters extracted of AlGaIn/GaN MOCVD and MBE technologies

Parameters	AlGaIn/GaN MOCVD technology			AlGaIn/GaN MBE technology		
W (μm)	2 × 25			2 × 50		
L_{DS} (μm)	1.5/2.5/3./4.5/5.5			2.65		
L_{GS} (μm)	0.6			1.13/1.15/1.18/1.2/1.23		
L_G (nm)	75	100	150	75	100	150
I_{DSS} (A/mm) @ $V_{GS} = 0$ V	0.96 ± 0.04	0.9 ± 0.02	0.83 ± 0.03	0.82 ± 0.03	0.72 ± 0.04	0.62 ± 0.04
R_{DS} ($\Omega.mm$)	1.86 ± 0.5	3.13 ± 0.3	3.6 ± 0.3	1.6 ± 0.4	2.87 ± 0.3	3.8 ± 0.5
G_{MMAX} (mS/mm) @ $V_{DS} = 6$ V	0.31 ± 0.02	0.29 ± 0.01	0.27 ± 0.01	0.4± 0.01	0.38 ± 0.02	0.32 ± 0.03
V_{TH} (V) @ $V_{DS} = 6$ V	-3.9 ± 0.05	-3.8 ± 0.04	-3.7 ± 0.05	-2.05 ± 0.05	-1.9 ± 0.05	-1.8 ± 0.05
ϕ_B (eV)	0.68 ± 0.025			0.55 ± 0.15		
η	2.54 ± 0.25			4.54 ± 1		
I_{GINV} (A/mm) @ $V_{GS} = -15$ V	$8 \times 10^{-5} \pm 5 \times 10^{-5}$			$126 \times 10^{-4} \pm 123 \times 10^{-4}$		
R_C ($\Omega.mm$)	0.6 ± 0.1			0.6 ± 0.1		
R_{\square} (Ω/\square)	435 ± 6			240 ± 20		
L_T (μm)	1.25 ± 0.15			2.75 ± 0.2		

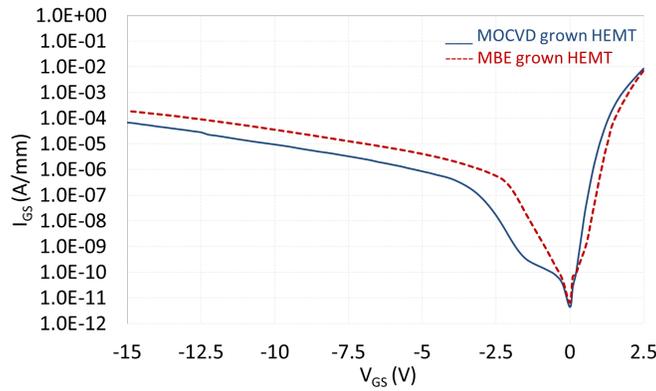


Figure 2.38: Comparison of I_{GS} - V_{GS} characteristics of MOCVD grown HEMT ($L_G = 75$ nm, $L_{GS} = 0.6$ μm , $L_{DS} = 1.5$ μm) and MBE grown HEMT ($L_G = 100$ nm, $L_{GS} = 1.15$ μm , $L_{DS} = 2.65$ μm)

lower. Furthermore, for MOCVD technology we can distinguish a small kink effect.

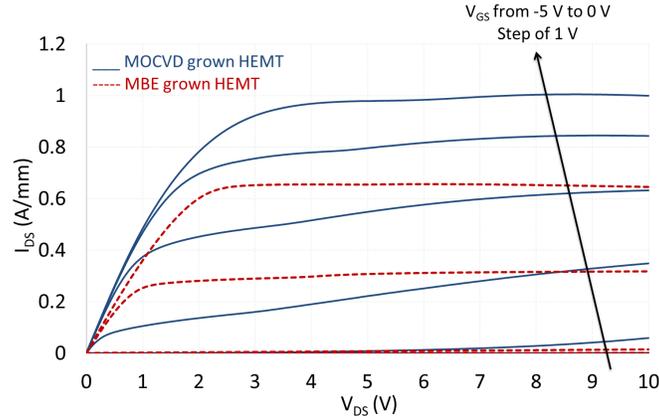


Figure 2.39: Comparison of I_{DS} - V_{DS} characteristics of MOCVD grown HEMT ($L_G = 75$ nm, $L_{GS} = 0.6$ μ m, $L_{DS} = 1.5$ μ m) and MBE grown HEMT ($L_G = 100$ nm, $L_{GS} = 1.15$ μ m, $L_{DS} = 2.65$ μ m)

Figure 2.40 shows the drain current and the transconductance characteristics for both technologies. The peak value of the transconductance is found higher for MBE-grown HEMT and the threshold voltage V_{TH} is found lower for MOCVD devices.

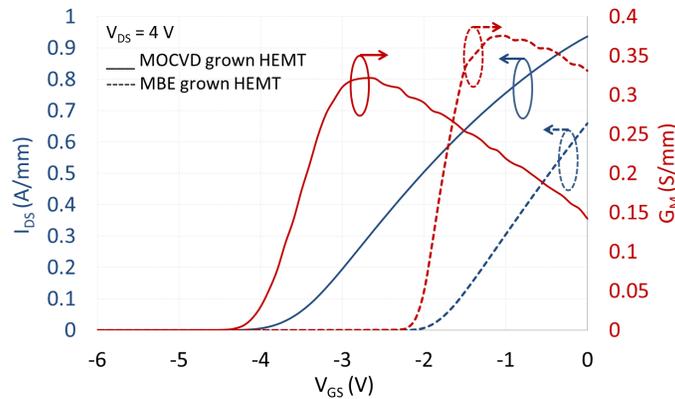


Figure 2.40: Comparison of I_{DS} - G_M (V_{GS}) characteristics of MOCVD grown HEMT ($L_G = 75$ nm, $L_{GS} = 0.6$ μ m, $L_{DS} = 1.5$ μ m) and MBE grown HEMT ($L_G = 100$ nm, $L_{GS} = 1.15$ μ m, $L_{DS} = 2.65$ μ m)

As previously shown, the ohmic contact resistance (R_C) and the sheet resistance (R_{\square}) are found excellent for both technologies. As reported in Table 2.12, ohmic contacts of MBE devices present a comparable contact resistance, R_C , and lower resistance, R_{\square} , than that of MOCVD devices. Thus, MBE technology provides HEMTs with best epitaxial quality and best conduction property [48].

2.5 RF characterization and parameter extraction

The small signal microwave characteristics were evaluated at IEMN Lille using a Keysight vector network analyzer (E8361A). To assess the high frequency performances of GaN HEMTs, microwave S-parameter measurements were performed from 500 MHz to 67 GHz.

It is possible to model the device by a linear quadripole or by a S_{IJ} parameter matrix. The electrical modeling of a HEMT device is obtained through the elaboration of an equivalent circuit model as shown in Figure 2.41.

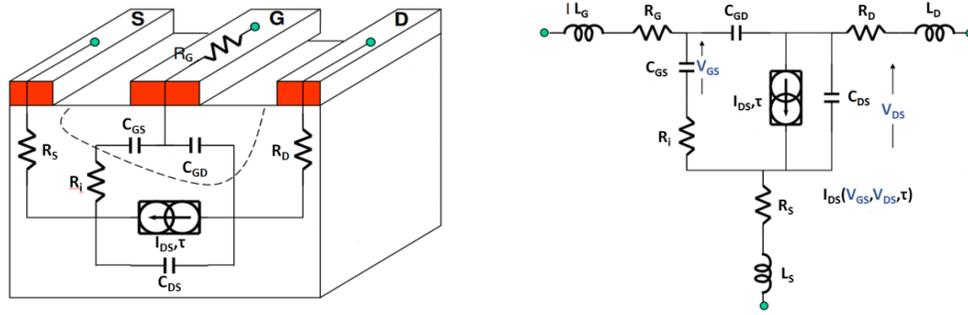


Figure 2.41: Small signal equivalent circuit model of the HEMT

R_S and L_S are the source access resistance and the source inductance respectively. Similarly, R_D , R_G , L_D and L_G correspond to the resistances and inductances of the drain and gate electrodes. The elements C_{GS} , C_{GD} and C_{DS} represent the capacitance between gate-source, gate-drain and drain-source respectively.

The high-frequency performances of any microwave transistor are usually assessed by two small-signal figures-of-merit, which are the maximum oscillation frequency f_{MAX} and the current gain cutoff frequency f_T . The current gain cutoff frequency (f_T) is defined at the frequency where the current gain $|H_{21}|$ is equal to 0 dB. Several couples of polarization points (V_{GS} , V_{DS}) have been investigated so as to be positioned around the maximum of transconductance (optimum polarization point previously defined during the static measurements) for detecting the maximum cut-off frequency and the maximum oscillation frequency of the component.

The transmission hybrid parameter (H_{21}) is:

$$H_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \quad (2.16)$$

$$H_{21} = \frac{I_{out}}{I_{in}} \quad (2.17)$$

From the various intrinsic and extrinsic elements of the equivalent circuit model, the expres-

sion of the cutoff frequency of the current gain is governed by equation:

$$W_R = 2\pi f_T = \frac{G_M}{C_G} = \frac{G_M}{C_{GS} + C_{BG} + C_{GD}} \quad (2.18)$$

The maximum oscillation frequency (f_{MAX}) is the highest operating frequency beyond which a transistor is not able to amplify power, it is derived as:

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi R_G C_{GD}}} \quad (2.19)$$

It is defined as the frequency at which the unilateral power gain $|U|$ is unity or 0 dB. Consequently, f_{MAX} is an important figure-of-merit to assess potentialities for high-frequency analog applications.

Where unilateral gain (U) is expressed as [49]:

$$U = \frac{1}{2} \frac{|S_{21} - 1|^2}{k \frac{S_{21}}{S_{12}} - Re\left(\frac{S_{21}}{S_{12}}\right)} \quad (2.20)$$

Calibration of the measurement system is necessary to determine systematic errors through a series of measurements on a calibration structure. In this case, an LRRM (Line-Reflect-Reflect-Match) calibration is performed [50]. Thus calibration permits to correct the errors introduced by the interconnection elements between the measured device and the end of the measurement probes. After calibration, the reference plane is found at the level of the measurement pads. In turn, the de-embedding operation consists in shifting the electrical reference planes closer to the device under test in order to subtract unwanted contributions.

The Open-Short de-embedding technique consists in measuring on wafer the S parameters of the components under test as well as those of the Open and Short patterns with the same topology. An Open structure is an open circuit allowing to characterize the capacitive effects of all the accesses while a Short structure allows to take into consideration the capacitive, resistive and inductive effects of these same access lines.

The Open Short method was chosen to implement de-embedding. This procedure consists in eliminating the contribution of certain parasitic measured elements, namely the access lines and the contact pads, by applying a so-called peeling method.

After the de-embedding procedure, the frequencies f_T and f_{MAX} were evaluated from the extrapolation by a slope of -20 dB/dec [49] of the gain of current $|H_{21}|$ and of unilateral gain of Mason $|U|$. Noting that there is another definition for f_T by using the Gummel method [51], where f_T is extracted from the inverse of the low frequency slope of $\frac{1}{H_{21}}$.

Through these equations (f_T and f_{MAX}), the improvement of the components performances

requires, among other things, the reduction of the parasitics, namely the parasitic access resistances, the output conductance $\frac{1}{R_{DS}}$ likely to contribute to the drastic drop of frequency performances as well as parasitic capacitances C_{GS} and C_{GD} .

Microwave power measurements will not be carried out on these technologies due to the excessive losses observed in the epitaxial structure which essentially limit the performances indicators such as power gain and energy efficiency (PAE). Estimated output power ($P_{out,max}$) can be determined using the following equation:

$$P_{out,max} = \frac{\Delta I_D \Delta I_V}{8} = \frac{I_{MAX}(V_{breakdown} - V_{knee})}{8} \quad (2.21)$$

A "load line" is drawn on figure 2.42 between the two extreme points I_{MAX} and $V_{breakdown}$. For both technologies under study, $V_{breakdown}$ is of the order of 70 V.

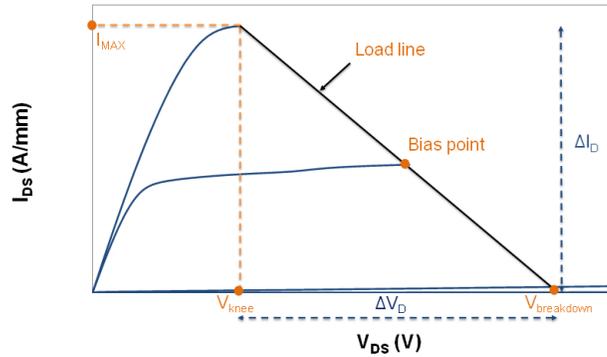


Figure 2.42: Output characteristic I_{DS} (V_{DS}) of a Class A power amplifier and load line

2.5.1 AlGaN/GaN MOCVD technology

Figure 2.43 shows the evolution of the current Gain $|H_{21}|$ and the unilateral power gain $|U|$ versus frequency of a typical sample which has a total width of $2 \times 25 \mu m$, a gate-source distance of 600 nm, a drain-source distance of 5.5 μm and a gate length of 100 nm, at the bias point corresponding to the maximum of transconductance previously determined. The extrapolation by a slope of -20 dB/dec leads to evaluate the cutoff gain frequency and the maximum oscillation, f_T and f_{MAX} which are 50 GHz and 75 GHz respectively at $V_{GS} = 2.6 V$ and $V_{DS} = 4 V$. The output power is estimated using equation 2.21 to be 8.12 W/mm (26 dBm).

2.5.1.1 Impact of device geometry on RF performances

As for the analysis of the static performances of the components, a study of the microwave performances evolution with the different gate lengths, gate-source distances and gate-drain distances

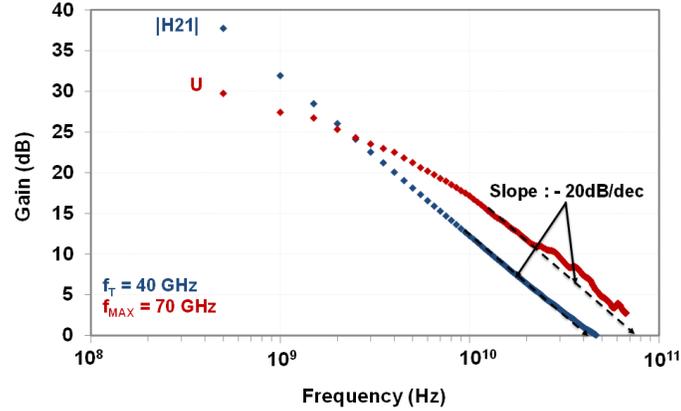


Figure 2.43: The evolution of the current Gain $|H_{21}|$ and unilateral power gain $|U|$ versus frequency of a typical MOCVD HEMT ($L_G = 100 \text{ nm}$, $L_{DS} = 5.5 \text{ }\mu\text{m}$)

was carried out. The table 2.13 summarizes the main results obtained: the current gain cutoff and the maximum oscillation frequencies for different geometries of AlGaIn/GaN MOCVD technology.

The extraction of f_T and f_{MAX} from HEMTs of different geometry shows that the decrease of the gate length is accompanied by an increase of f_T and f_{MAX} . This means that the cut-off frequency scales almost linearly with the inverse of the gate length down to $L_G = 75 \text{ nm}$.

Improving the power-frequency performances of transistors does not depend only on technological improvements (such as reduction of gate length, passivation, etc.). An additional and crucial point is to reduce the thickness of the barrier separating the gate of the channel as the gate length decreases in order to reduce the transit time of the electrons under the gate and thus to reach higher operating frequencies. This must be done while maintaining an efficient control of the carriers under the gate, in which case there appear phenomena such as the "short channel effect" or, "punch through", which cause rapid increase of the subthreshold drain leakage current and it is often interpreted as the device breakdown voltage [52,53], due to the low back confinement of the electrons in the channel.

From Table 2.13, it can be noted that for a L_{DS} distance of $5.5 \text{ }\mu\text{m}$, the cut-off frequency f_T varies from 40 GHz when $L_G = 150 \text{ nm}$ to 55 GHz when $L_G = 75 \text{ nm}$ which is an increase of 37 % and the maximum oscillation frequency varies from 54 GHz when $L_G = 150 \text{ nm}$ to 78 GHz when $L_G = 75 \text{ nm}$ which is an increase of 44 %.

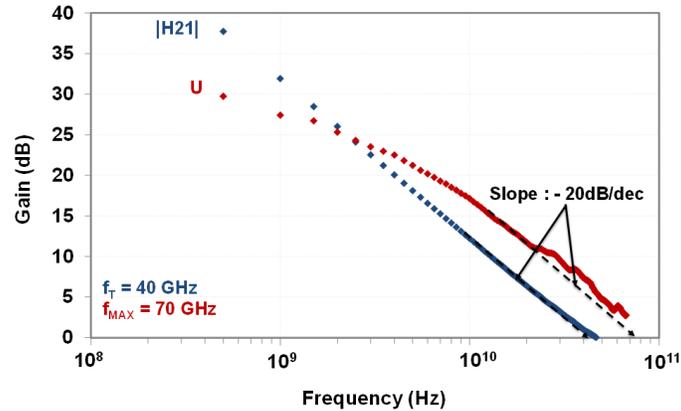
Considering the obtained results, the reduction of the gate length L_G and the drain source distance L_{DS} have allowed a significant improvement in the current gain cut-off frequency and the maximum oscillation frequency due to the decreasing capacitive effects as expected [54,55].

Table 2.13: The cutoff frequency and the maximum oscillation for AlGaN/GaN MOCVD HEMTs of different geometry

W (μm)	L_G (nm)	L_{DS} (μm)	f_T (GHz)	f_{MAX} (GHz)
2×25	75	1.5	80	100
		2.5	68	92
		3.5	60	84
		4.5	57	81
		5.5	55	78
	100	2.5	63	82
		3.5	58	78
		4.5	54	70
		5.5	50	75
	150	2.5	48	64
		3.5	47	62
		4.5	44	59
5.5		40	54	

2.5.2 AlGaN/GaN MBE technology

Figure 2.44 shows the evolution of the current Gain $|H_{21}|$ and unilateral power gain $|U|$ versus frequency of a typical device which has a total width of $2 \times 50 \mu m$, a gate-source distance of $1.15 \mu m$, a drain-source distance of $2.65 \mu m$ and a gate length of $100 nm$ at the bias point corresponding to the maximum of the transconductance previously determined. A value of f_T of $40 GHz$ and a value of f_{MAX} of $70 GHz$ were obtained at $V_{DS} = 4 V$ and $V_{GS} = -1.2 V$. The output power is estimated to be $7.11 W/mm$ ($28.52 dBm$).

Figure 2.44: The evolution of the current Gain $|H_{21}|$ and unilateral power gain $|U|$ versus frequency of a typical MBE HEMT ($L_{GS} = 1.15 \mu m$, $L_G = 100 nm$)

2.5.2.1 Impact of device geometry on RF performances

The Table 2.14 summarizes the main results obtained of cut-off frequency and maximum oscillation frequency for devices with different geometry.

Table 2.14: The cutoff and the maximum oscillation frequencies for AlGaIn/GaN MBE HEMTs of different geometry

W (μm)	L_G (nm)	L_{DS} (μm)	f_T (GHz)	f_{MAX} (GHz)
2×50	75	1.18	52	78
		1.23	55	80
	100	1.15	40	70
		1.2	53	79
	150	1.13	38	60
		1.18	40	65

Measurements of S parameters were made up to 67 GHz. The current gain modulus and the unilateral gain of Mason (U) were measured as a function of the frequency on the different transistors. A cut-off frequency f_T of 50 GHz and a maximum oscillation frequency f_{MAX} of 78 GHz were obtained on the smallest gate length of 75 nm and a gate-source spacing of 1.23 μm . Reducing the gate length L_G allowed an improvement in the cut-off frequency and the maximum oscillation frequency.

2.6 Conclusion chapter 2

In the first part of this chapter, a description of the devices under test and the key technological steps has been discussed. Another part of this chapter presents the electrical characteristics of HEMT components issued from AlGaIn/GaN HEMT MOCVD technology and AlGaIn/GaN HEMT MBE technology. The measurements consisted of the standard DC and RF measurements. The DC characteristics were carried out in order to study the electrical behavior and the dispersion of the electrical parameters of the studied transistors. Then, RF characterization was carried out in order to assess high frequency performances.

This study allows to evaluate the impact of the geometry on the component performances so as to determine the optimum topology in terms of gate length, gate-source distance and drain-source distance and finally to obtain the best performances in both static mode and in terms of cut-off frequencies.

HEMT grown by MOCVD were compared with HEMT grown by MBE. Results indicated that devices grown by MOCVD exhibit larger saturation drain current, I_{DSS} , cut-off frequency, f_T and maximum oscillation frequency, f_{MAX} , especially at shorter gate lengths, primarily because the

improved carrier confinement reduces short channel effects. The 2D electron gas density increases with the aluminum content, the addition of a very thin layer AlN (1nm) between the channel and the barrier layer [56] and the addition of a cap layer to the surface of AlGaN layer [57].

The measurements described in this chapter aimed to check the DC and dynamic electrical behavior of the devices and the performance homogeneity of the transistors within the wafers. A reliability campaign to test the devices will be investigated in the following chapter.

References Chapter 2

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Chapter 3

SOA evaluation by "step stress" accelerated aging tests

3.1 Introduction

After the measurements dedicated to characterize the DC and dynamic electrical behavior of the devices and to evaluate the performance homogeneity of the transistors within the wafers, it has been possible to assess the reliability of the devices by performing DC step stresses.

This chapter presents a reliability study as a function of the drain and gate bias conditions for different geometries of AlGaIn/GaN HEMTs. It focuses on the Safe Operating Area (SOA) of the HEMT technology by experimentally determining the boundary of the maximum voltage and conduction current sustained by the HEMT when biased in DC conditions.

At the beginning of this chapter, the methodologies used for evaluating the SOA of GaN HEMTs on silicon substrate are presented. Then, DC accelerated aging tests results are detailed and discussed, including the identification of degradation signatures and the determination of the maximum values of DC bias voltages. Then, the critical degradation voltage variation with device geometry is studied. The last part of this chapter is devoted to the analysis of TLMs after aging tests.

3.2 "Step Stress" aging on AlGaIn/GaN MOCVD technology

The "step stress" aging on AlGaIn/GaN HEMTs consists in carrying out DC aging sequences under gate-source voltage bias in "on-state" (at $V_{GS} = 0 / -1 / -2 / -3$ V) or "off state" (at $V_{GS} = -4$ V) conditions while V_{DS} is stepped up from 5 V to a higher voltage increasing by 5 V step.

During this experiment, difficulties encountered were mainly technical problems such as os-

cillations of devices manufactured on MBE technology. Many experiments have been done in order to stabilize currents such as adding bias tees on the gate and drain sides or a ferrite but without any result. For this reason, the reliability study only focuses on the MOCVD technology.

3.2.1 Test bench

The electrical characterizations before and after aging tests are carried out by HP 4142B modular DC monitor. The experimental setup used for aging tests under DC electrical constraints is based on a BILT system BE100 providing electrical polarization to the transistors transferred on the test base station. This test bench is controlled by a PC using the "EASY STRESS" software as shown in 3.1.

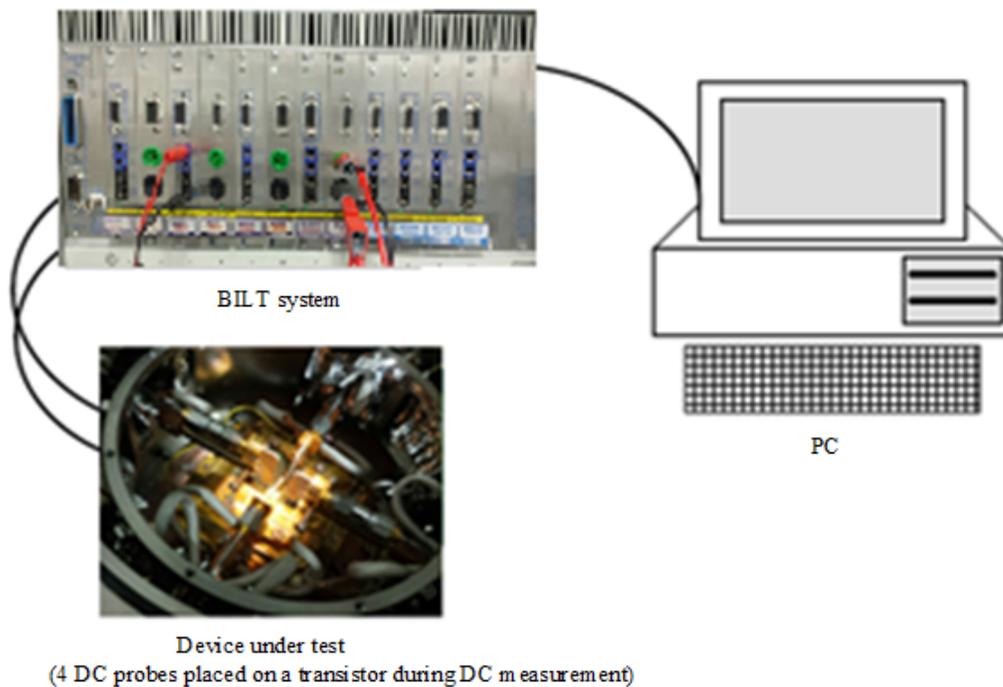


Figure 3.1: Accelerated aging test bench

BILT is a modular test system, which primary purpose is the generation of high quality of programmable power source for test benches. The management of the bench is ensured by different hardware and software entities (Figure 3.2). The BILT system makes it possible to polarize at most five transistors at the same time with different polarization conditions. In our case, as the accelerated aging test is directly performed on wafer, it is possible to polarize with contact probes only one transistor at a time.

- The "Easy Stress" PC software allows to control the BILT chassis for the aging tests
- The Figure 3.2 illustrated the BILT system description.

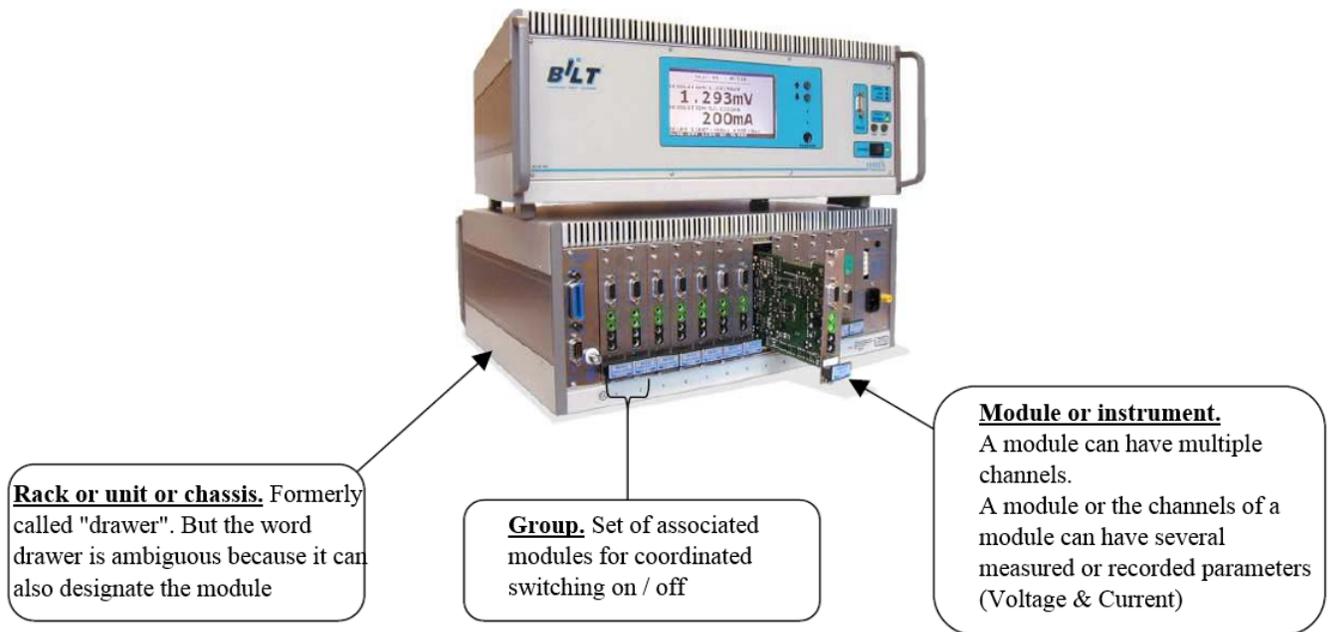


Figure 3.2: BILT System Description

Easy Stress is a software for controlling a BILT chassis network for accelerated aging tests of electronic components in static continuous operation. Once the test is launched, the chassis is autonomous. It manages a time counter, the measurement traces, the monitoring of the thresholds on the measurements, and so on.

BILT DC sources performances are achieved thanks to the following choice of ranges; e.g:

- For the BE515 module that polarizes the transistor gate, 8 current ranges from $6.25 \mu A$ to $200 mA$ full scale, and 4 voltage ranges from 5 to 40 V.
- For the BE525 module that polarizes the drain transistor, 8 current ranges from 10 to 2 A full scale, and a $\pm 60 V$ voltage range.

The measurement resolution and precision for current ranges of the BE515 module are reported in table 3.1.

3.2.2 Description of the 1st methodology

The methodology consists in carrying out DC aging sequences under voltage bias. Each aging sequence is defined by a couple of polarization points (V_{GS} , V_{DS}). An aging sequence is composed

Table 3.1: Summary of parameter extraction results of TLMs

Ranges	± 6.25 μA	± 25 μA	± 125 μA	± 500 μA	± 2.5 $m A$	± 10 $m A$	± 50 $m A$	± 0.2 A
Resolution	1.6 $n A$	6.6 $n A$	33 $n A$	131 $n A$	0.66 μA	2.6 μA	13 μA	53 μA
Precision	19 $n A$	78 $n A$	375 $n A$	1.5 μA	7.5 μA	30 μA	150 μA	600 μA

of several aging steps: V_{DS} is stepped up from 5 V to a higher voltage increasing by 5 V step while maintaining the V_{GS} voltage constant. Each step is held for 5 or 15 minutes at a fixed drain voltage and the drain and gate currents are recorded during the whole aging sequence. The sampling frequency is 1 kHz. The device DC characteristics are measured before and after the aging sequence. Some components are submitted to the DC aging sequences until a significant degradation occurs in order to define their maximum operating conditions and the associated degradation criterion. For the rest of this chapter, let us note the aging conditions as shown in the following table.

Table 3.2: Step-stress V_{GS} aging conditions and their notations

Notation Aging	conditions
A	$V_{GS} = 0$ V
B	$V_{GS} = -1$ V
C	$V_{GS} = -2$ V
D	$V_{GS} = -3$ V
E	$V_{GS} = -4$ V

3.2.2.1 On-state step stress tests

On-state degradation tests are carried out by means of the step stress strategy in condition A (at $V_{GS} = 0$ V), increasing drain voltages until device failure is reached. Figure 3.3 shows a representative result of the evolution of I_{DS} and I_{GS} currents measured during the aging sequence of a 75 nm gate length and 4.5 μm drain-source distance HEMT, with the drain voltage increased from 5 V to 25 V by step of 5 V every 5 minutes.

It is noted that a decrease of I_{DS} and I_{GS} currents is associated with the increase of the bias condition V_{DS} from one step to another. If this decrease of I_{DS} is considered as a degradation, it means that the drain current should increase according to the I_{DS} - V_{DS} characteristic except if its decrease is due to thermal effects at high V_{DS} . Then, it is not possible to conclude on the I_{DS} degradation without comparing the I_{DS} - V_{DS} characteristic up to 25 V measured before and after the stress sequence but these measurements could possibly induce degradation in the device

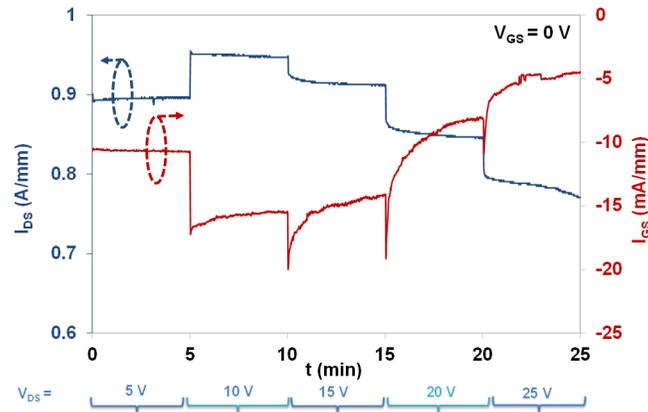


Figure 3.3: Results of a step-stress experiment carried out on a HEMT with a gate length of 75 nm and a drain-source distance of $4.5 \text{ }\mu\text{m}$. The gate voltage is fixed in condition A (at $V_{GS} = 0 \text{ V}$), while the drain voltage is increased by 5 V every 5 minutes.

under test.

The gradual evolution of I_{DS} and I_{GS} is observed as a function of the aging time until a significant decrease of the gate and drain currents is recorded during the step at $V_{DS} = 25 \text{ V}$. There are also oscillations of the gate current during the last step at $V_{DS} = 25 \text{ V}$. Then, a catastrophic degradation occurred for $V_{DS} > 25 \text{ V}$ as shown in figure 3.4.



Figure 3.4: Optical image of a device before stress and after a catastrophic degradation

3.2.2.2 Off-state step stress tests

Off-state degradation tests are carried out by means of the step stress strategy with $V_{GS} = -4 \text{ V}$. Increasing drain voltages are applied to the devices, until failure is reached. Figure 3.5 shows a representative result of the gate and the drain currents evolution during the aging sequence of a 150 nm gate length and $2.5 \text{ }\mu\text{m}$ drain source distance HEMT, when the drain voltage is increased from 5 V to 60 V by step of 5 V every 5 minutes. As expected, increasing the V_{DS} bias voltage involves the increase of the gate and drain currents.

As illustrated in 3.5, in off-state mode in condition E (at $V_{GS} = -4 V$), we can reach $V_{DS} = 60 V$ (which is the voltage range limit of the BE525 module) without any degradation for this typical device.

The recording of the gate current is noisy: this is due to the resolution of the measurement which is of the same order of magnitude of the gate current. In this case, the gate current of the device was low enough to consider that its evolution is not significant.

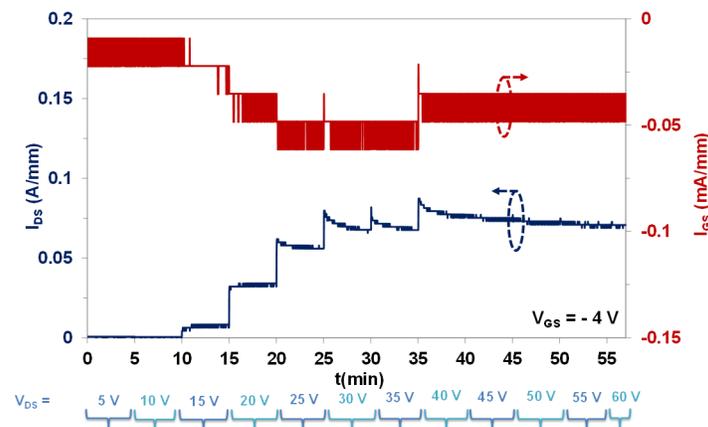


Figure 3.5: Results of a step-stress experiment carried out on a HEMT with a gate length of $150 nm$ and a drain-source distance of $2.5 \mu m$. The gate voltage is fixed in condition E (at $V_{GS} = -4 V$), while the drain voltage increases by $5 V$ every 5 minutes

We have shown the results of aging tests, which have been carried out by sweeping up the drain-source voltage of the device, until a sudden decrease in drain current is detected. However, this method can be destructive and its major disadvantage is that it is difficult to analyze the gradual degradation of the device and to conclude except in the case of catastrophic failure.

Another method chosen to define the maximum values of DC bias voltages will be described in the following section.

3.2.3 Description of the 2nd methodology

The second methodology, based on two steps, has been defined for in-situ diagnosis of permanent degradation of the HEMT DC characteristics. It consists in performing:

i) A burn-in in nominal conditions ($V_{GS} = 0$, $V_{DS} = 5 V$) for 30 minutes in order to stabilize the gate and drain currents. As shown in figure 3.6 for a typical component, after 10 minutes the currents stabilize.

ii) A sequence of step stress tests applied until a degradation criterion is reached. It is composed of a stressful biasing for 5 or 15 minutes followed by a non-stressful biasing for 5 or 15

minutes in nominal conditions. Then, the former sequence is repeated several times with more severe drain-source bias conditions. The figure 3.7 shows the accelerated test profile. A typical result of such accelerated test profile is shown in figure 3.8 for a 75 nm gate length and 5.5 μm drain-source distance HEMT.

The bias conditions for the non-stressful steps, here $V_{GS} = 0$, $V_{DS} = 5$ V, are chosen not to induce any permanent degradation. This is checked during the burn-in of the devices, where bias conditions are generally the same as the one applied for non-stressful steps.

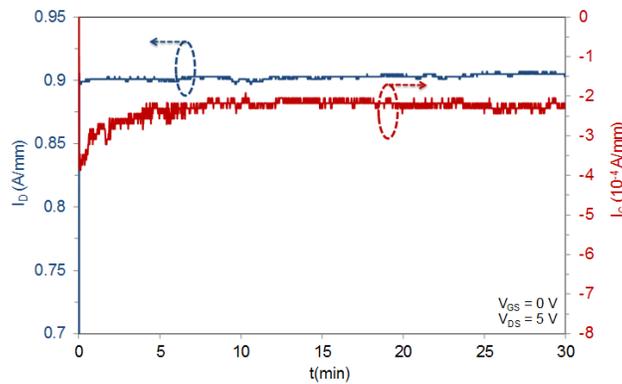


Figure 3.6: Example of burn-in in nominal conditions ($V_{GS} = 0$, $V_{DS} = 5$ V) for 30 minutes of a 75 nm gate length and 5.5 μm drain-source distance HEMT

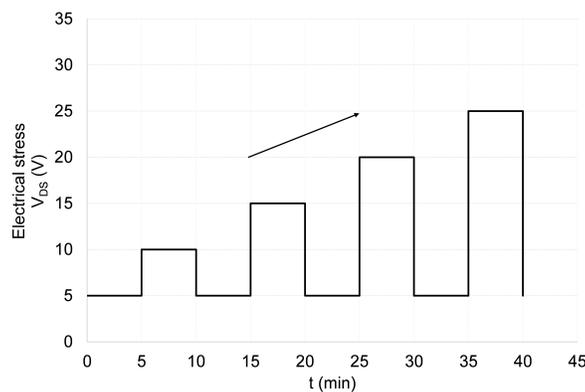


Figure 3.7: Accelerated life test profile with a step duration of 5 min

We have defined the critical V_{DS} degradation voltage such that the drain current decreases by 10%. This criterion is chosen judiciously when the degradation is beginning. It is justified in order to be able to make the degradation diagnosis before a catastrophic failure occurs. On the other hand, the degradation criterion must be significant compared to the initial

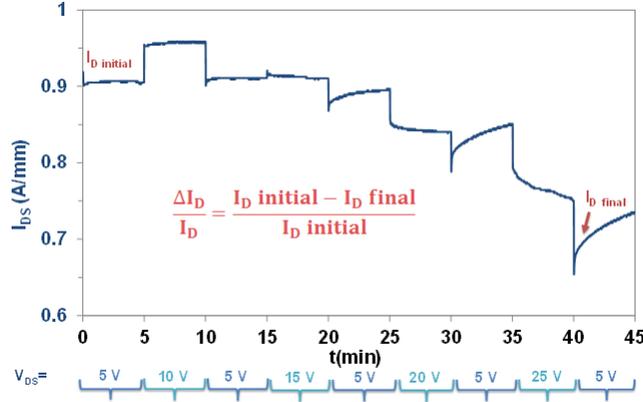


Figure 3.8: Example of drain current evolution versus time of a 75 nm gate length and $5.5 \mu\text{m}$ drain-source distance HEMT during the step stress sequence in condition A (at $V_{GS} = 0 \text{ V}$) with $V_{DS} = 5 \text{ V}; 10; 5; 15; 5; 20; 5; 25; 5 \text{ V}$

dispersion of electrical parameters. As shown in chapter 2, the dispersion of the drain current is about 3 %. The drain current degradation after an aging sequence is calculated with I_{DS} value recorded at the beginning of initial and final non-stressful 5 V steps. It is defined as:

$$\frac{\Delta I_D}{I_D} = \frac{I_{D\text{initial}} - I_{D\text{final}}}{I_{D\text{initial}}} \quad (3.1)$$

Where I_D initial and I_D final are the drain current of the first 5 V step and the drain current of the last 5 V step respectively when increasing the bias conditions (as shown in figure 3.8). Figure 3.9 shows the flow diagram of this methodology.

3.3 Aging test results

During the step stress sequence, several parameters such as the drain current decrease, the drain current transient at $V_{DS} = 5 \text{ V}$ and its amplitude, are identified. The evolution of these parameters defines the “signature” of degradation mechanisms.

The purpose of this section is to analyze the effect of accelerated aging tests performed in “on-state” and “off-state” regimes on the static electrical characteristics of the technology under test and the associated physical mechanisms. Three to five devices per geometry were investigated; thus more than 40 devices were submitted to aging tests.

The first part of this section is devoted to the identification of the degradation signatures. Then, the static and permanent degradation is studied, through the analysis of I-V characteristics evolution. The third part is devoted to the analysis of the transient degradation by determining the time constant and the amplitude of the drain current transient.

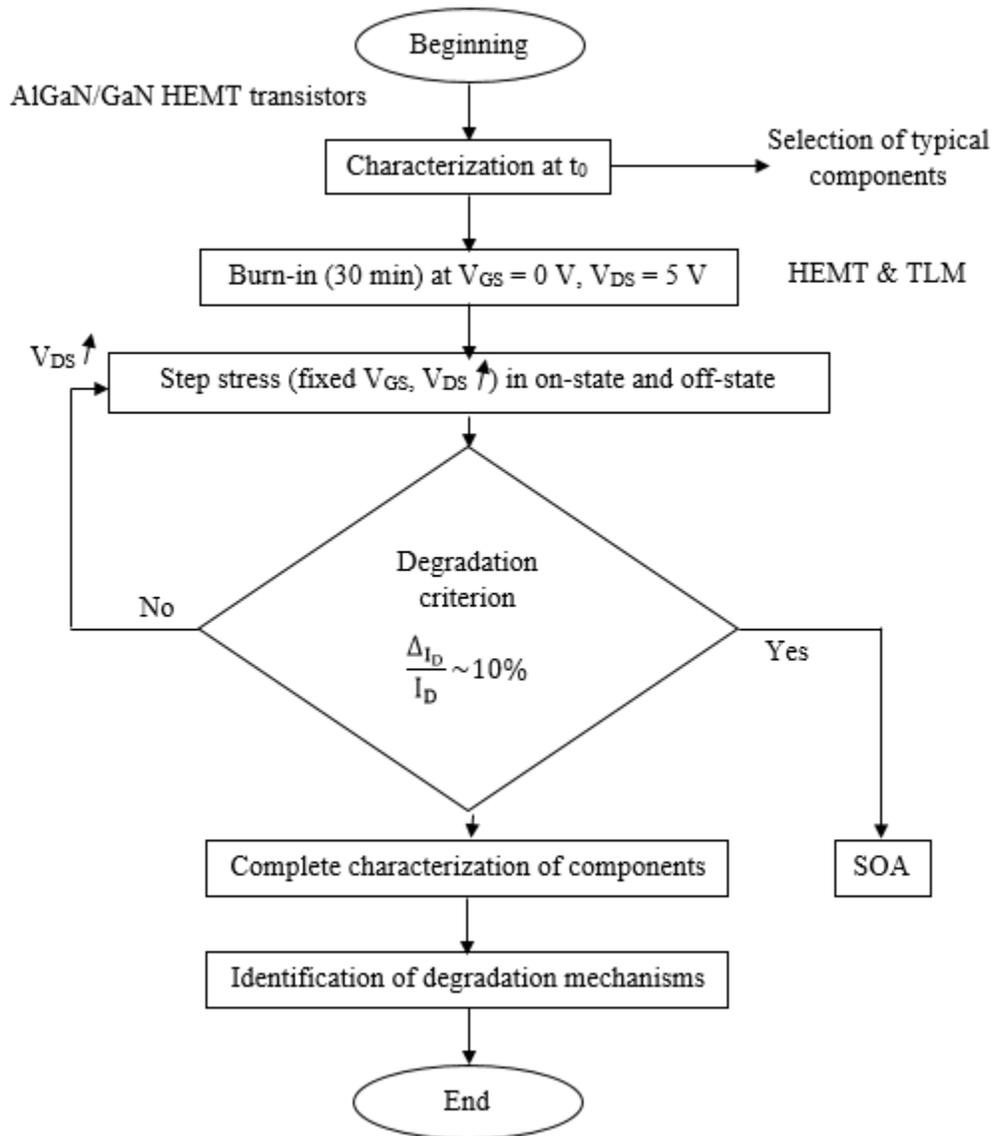


Figure 3.9: Flow diagram of the methodology defined for in-situ diagnosis of the permanent degradation during DC step aging tests

3.3.1 Identification of degradation signatures

3.3.1.1 On-state step stress tests

In the following, two typical examples are presented in on-state conditions. Figure 3.10 shows the drain current versus time of a 75 nm gate length and 5.5 μm drain-source distance HEMT with V_{DS} bias swept from 10 to 25 V by step of 5 V in condition A (at $V_{GS} = 0$ V) with a step duration

of 5 minutes. Figure 3.11 shows the drain current versus time of another GaN HEMT of the same geometry aged with V_{DS} bias swept from 10 to 30 V by step of 5 V in condition B (at $V_{GS} = -1$ V) with a step duration of 5 minutes. These two devices present a low gate current before stress (in the range of 4 μ A). Then, with respect to the performances of the BILT module, the record of the gate current was not significant even at the end of the stress sequence. Consequently, we will focus on the drain current evolution during aging sequences.

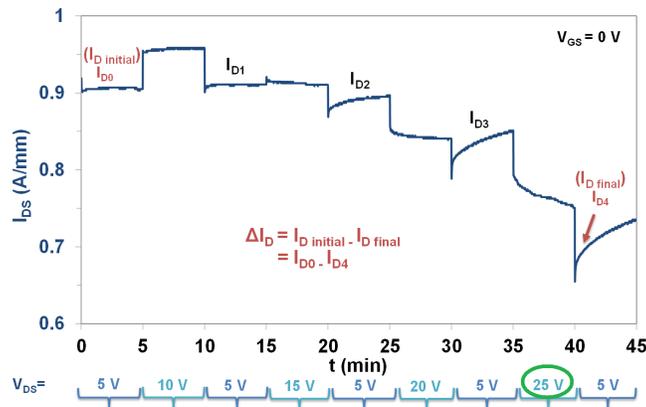


Figure 3.10: Drain current evolution versus time of a 75 nm gate length and 5.5 μ m drain-source distance HEMT during the step stress sequence in condition A (at $V_{GS} = 0$ V)

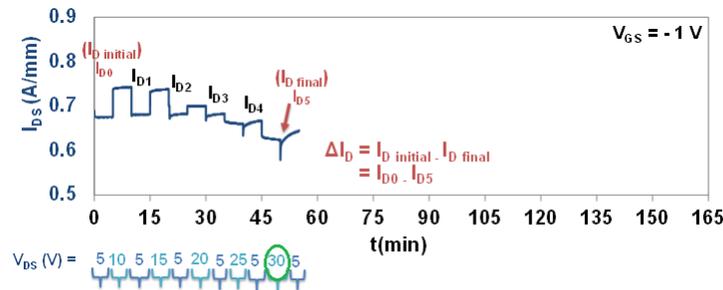


Figure 3.11: Drain current evolution versus time of a 75 nm gate length and 5.5 μ m drain-source distance HEMT during the step stress sequence in condition B (at $V_{GS} = -1$ V)

Figure 3.10 shows that drain current I_{DS} at $V_{DS} = 5$ V decreases by 12 % on the step at a drain source voltage of 25 V in condition A (at $V_{GS} = 0$). As for figure 3.10, figure 3.11 shows a decrease of the drain current I_{DS} at $V_{DS} = 5$ V by 11 % on the step at a drain-source voltage of 30 V in condition B (at $V_{GS} = -1$ V).

The same sequences have been carried out with step duration of 15 minutes as in the case of the figure 3.12. It shows the drain current evolution versus time of a 75 nm gate length and 5.5 μ m drain-source distance HEMT during the step stress sequence in condition B (at $V_{GS} = -1$ V).

Comparing the results shown in figure 3.11 (step of 5 minutes) and figure 3.12 (step of 15 minutes), I_{DS} decreases by 11 % after a drain source voltage of 30 V in both cases. Therefore, the same results were reproduced.

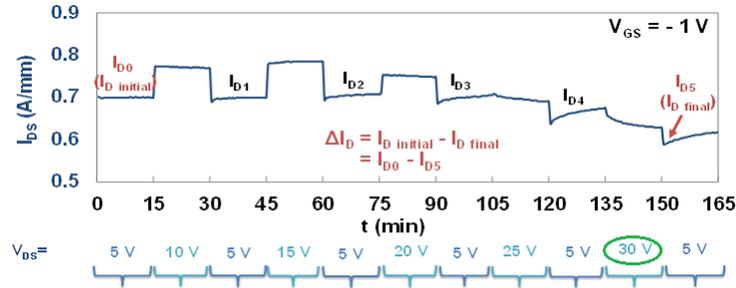


Figure 3.12: Drain current evolution versus time of a 75 nm gate length and 5.5 μm drain-source distance HEMT during the step stress sequence in condition B (at $V_{GS} = -1$ V)
The step duration is 15 minutes.

The advantage of this second aging test method proposed is the possibility to diagnose permanent degradation without removing the device under test from the test bench and without performing complete electrical characterization.

As shown in figures 3.10, 3.11 and 3.12 two degradation signatures can be identified:

i) Static and permanent degradation identified by the decrease of the drain current on successive 5 V non-stressful steps. Drain current does not change at $V_{DS} = 5$ V until the critical value of V_{DS} voltage is applied (25 V in condition A and 30 V in condition B) from which the drain current decreases sharply; I_{DS} decreases by 12 % in condition A (at $V_{GS} = 0$) and 11 % in condition B (at $V_{GS} = -1$ V).

ii) Intra-step degradation identified by a drain current transient on the unstressed step which amplitude often increases when the critical value of V_{DS} voltage is reached. Many experiments have been done to prove that this transient does not stem from the test bench. These drain current transients reflect trapping-detrapping phenomena which enhance during the aging sequence.

These degradations signatures will be detailed in sections 3.3.2 and 3.3.3.

3.3.1.2 Off-state step stress tests

Figure 3.13 shows the drain and gate currents evolution versus time of a 75 nm gate length and 3.5 μm drain-source distance HEMT during a step stress sequence performed in off-state conditions in condition E (at $V_{GS} = -4$ V).

At the end of the sequence carried out in condition E (at $V_{GS} = -4$ V) and V_{DS} up to 60 V, which is the limit of stress test setup, no degradation was detected. Indeed, the values of the

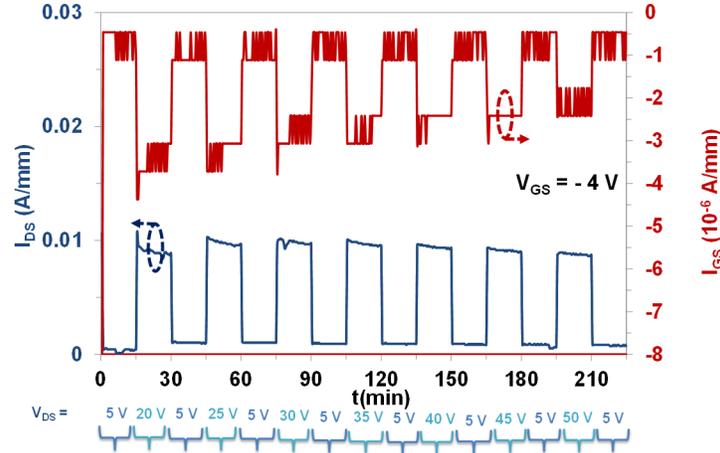


Figure 3.13: Drain and gate currents evolution versus time of a 75 nm gate length and 3.5 μm drain-source distance HEMT during the step stress sequence in condition E (at $V_{GS} = -4$ V) with step duration of 15 min and $V_{DS} = 5$ V; 20; 5 V; 25; 5 V; 30; 5 V; 35; 5 V; 45; 5 V; 50; 5 V

gate and drain currents measured during the non-stressful steps at $V_{DS} = 5$ V do not significantly change.

3.3.1.3 Influence of V_{GS} polarization

Other devices were stressed in conditions C and D, i.e. at V_{GS} of -2 V and -3 V. The results are summarized in table 3.3 and compared with results obtained in conditions A and B.

Table 3.3: Relationship between the critical V_{DS} degradation voltage and the gate source voltage at which devices are aged

Aging conditions	V_{GS} (V)	L_G (nm)	L_{DS} (μm)	% I_{DS} decrease at $V_{DS} = 5$ V	V_{DSdeg} (V)
A	0	75	5.5	12 ± 3	25
B	-1	75	5.5	11 ± 1	30
C	-2	75	5.5	10 ± 1	40
D	-3	75	5.5	10 ± 2	50

These results consolidate the fact that V_{DS} degradation voltage at which the static and permanent degradation occurs, increases with V_{GS} becoming more negative.

Drain current versus time of two HEMTs with the same topology ($L_G = 75$ nm, $L_{DS} = 5.5$ μm) during the step stress sequences A (at $V_{GS} = 0$) and B (at $V_{GS} = -1$ V) is shown in figure 3.14.

As noticed in figure 3.14 the critical degradation voltage is all the more important as the voltage V_{GS} is negative; indeed, we assume that it is not only the electric field that leads to the degradation but rather more a combination of high current density and electric field. Moreover, a

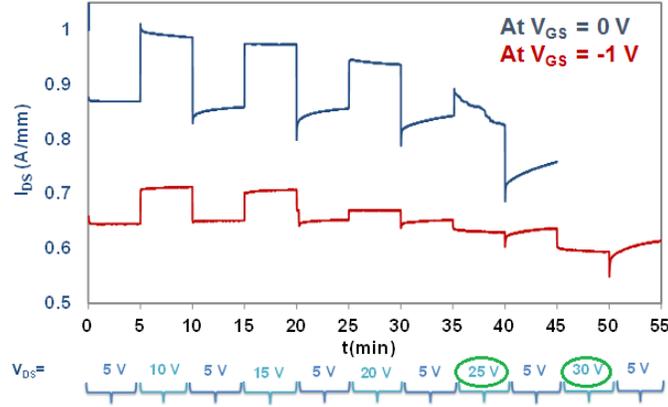


Figure 3.14: Drain current evolution versus time of HEMTs ($L_G = 75$ nm, $L_{DS} = 5.5$ μ m) during the step stress sequences in condition A (at $V_{GS} = 0$ V) and B (at $V_{GS} = -1$ V)

high current density leads to an increase in temperature. Therefore, self-heating should contribute as a degradation factor.

3.3.1.4 Cumulative effect during the step stress sequence

During the step stress sequences shown before, the amplitude of intra-step transients of the unstressed step (5 V step) usually increases when a degradation is observed. It can be due to the amplification of trapping effects. A further study was carried out by performing decreasing step stress sequences and comparing them with increasing ones applied under the same conditions.

Figure 3.15 and figure 3.16 show the drain and gate currents evolution versus time of two typical transistors having the same geometry ($L_G = 100$ nm, $L_{DS} = 2.5$ μ m) during the step stress sequence in condition A (at $V_{GS} = 0$ V). The drain-source voltage is increased from 5 V to 25 V (Figure 3.15) and in another sequence decreased from 25 V to 5 V (Figure 3.16). The comparison of these two aging sequences leads to ensure if there is or not any cumulative effect during aging sequence and then if there is an amplification of trapping effects.

As shown in figure 3.15, when the drain voltage of stressful step is increased up to 25 V, the drain current value at 5 V steps decreases and the transient amplitude increases. The critical V_{DS} degradation value is observed at 25 V, at which the drain current decreases approximately by 11 %. Figure 3.16 shows that the critical V_{DS} degradation value is observed at the first stressful step of 25 V, at which the drain current decreases sharply by 13 %. Then, in the V_{DS} decreasing sequence, the drain current value at 5 V steps increases and the transient amplitude decreases. Comparing the aforementioned figures, we can notice that there is no cumulative effect during aging sequence due to the relaxation during the 5 V steps.

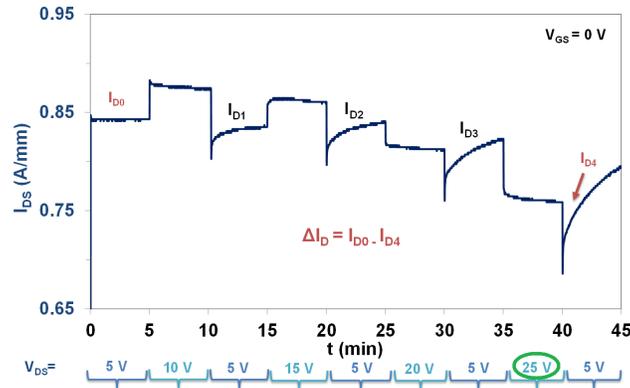


Figure 3.15: Drain and gate current evolution versus time of a 100 nm gate length and 2.5 μm drain-source distance HEMT during the step stress sequence. The gate voltage is fixed in condition A (at $V_{GS} = 0\text{ V}$), while the drain voltage is increased from 5 to 25 V by step of 5 V every 5 minutes)

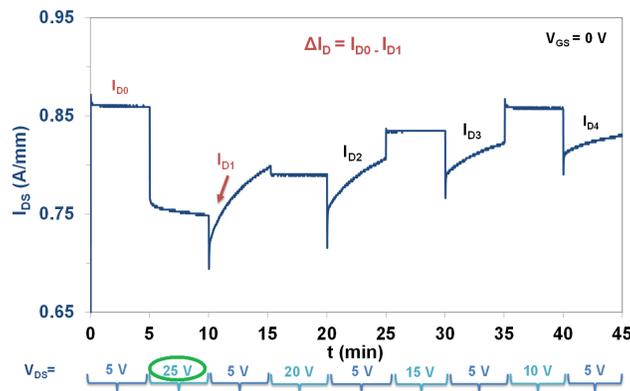


Figure 3.16: Drain and gate current evolution versus time of a 100 nm gate length and 2.5 μm drain-source distance HEMT during the step stress sequence. The gate voltage is fixed in condition A (at $V_{GS} = 0\text{ V}$), while the drain voltage is decreased from 25 V to 5 V by step of 5 V every 5 minutes)

3.3.2 Static and permanent degradation

3.3.2.1 On-state step stress tests

In this section, we report representative results, obtained on a device with the shortest gate length $L_G = 75\text{ nm}$ and $L_{DS} = 5.5\ \mu\text{m}$. Figure 3.17 shows a typical evolution of $I_{DS}(I_{GS})-V_{DS}$ characteristics before and after the stress sequence performed under condition A (at $V_{GS} = 0$) (see Figure 3.10) where the drain current at $V_{DS} = 5\text{ V}$ decreases by 12 % during the stress sequence. In attempt to identify the degradation mechanisms, we compare these characteristics with the ones

measured after a storage at room temperature during 24 hours.

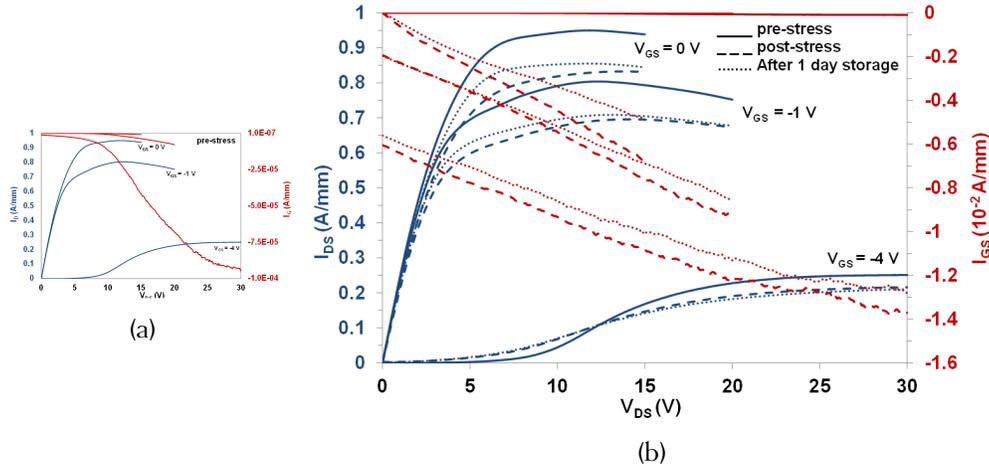


Figure 3.17: I_{DS} (I_{GS})- V_{DS} characteristics of a $5.5 \mu\text{m}$ drain-source distance and 75 nm gate length HEMT aged in condition A (at $V_{GS} = 0$) before and after stress and after 1 day storage. I_{DS} (I_{GS})- V_{DS} characteristics before stress on the top left

In figure 3.17, the observed shift of the I_{DS} (I_{GS})- V_{DS} characteristics reflects the permanent degradation of the gate and drain currents. Partial recovery of the drain and gate currents after one-day storage indicates that the degradation is also caused by trapping and detrapping mechanisms.

Electrons trapped by both the AlGaIn barrier traps and the surface states under stress lead to the partial recovery of device parameters when the stress is removed [1]. Chang et al. suggested that the degradation and the recovery process is closely related to the states of native traps [2]. The degradation under on-state conditions and its partial recovery indicates that reducing the initial trap concentration by proper processing technology is crucial in order to improve long term stability. 3.17 shows a decrease of the drain current from 0.9 to 0.8 A/mm at $V_{GS} = 0$ and $V_{DS} = 15 \text{ V}$, this is often attributed to crack formation [3], or electron trapping [4]. The gate current increases by 4 order of magnitude from -8.4×10^{-7} to $-5 \times 10^{-3} \text{ A/mm}$ at $V_{GS} = 0 \text{ V}$ and $V_{DS} = 15 \text{ V}$.

The decrease of I_{DS} is associated to the increase of R_{DS} by 5 % from 4.2 to $4.4 \Omega \cdot \text{mm}$ which is not significant compared to the dispersion of 3 % on virgin devices. R_{DS} was defined as the resistance between source and drain at $V_{GS} = 0$ and $V_{DS} = 0.5 \text{ V}$. In addition, the decrease of I_{DS} is correlated with an increase of I_{GS} as shown in figure 3.17. It indicates that the change of I_{DS} and I_{GS} may have the same origin.

Figure 3.18 shows a typical evolution of I_{DS} (G_M)- V_{GS} and I_{DS} - V_{GS} characteristics before and after the stress sequence in condition A.

Furthermore, the threshold voltage V_{TH} was extracted before and after stress using tangent

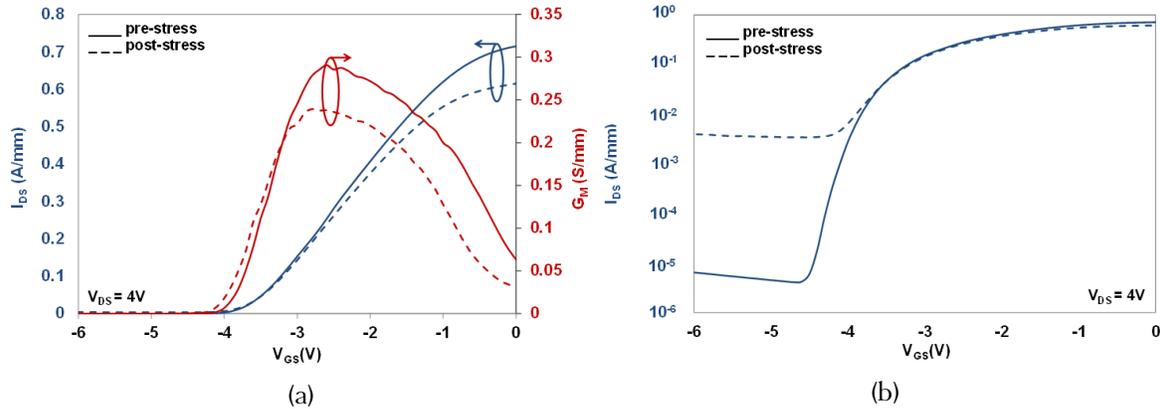


Figure 3.18: I_{DS} (G_M)- V_{GS} characteristic of a 75 nm gate length and 5.5 μm drain-source distance HEMT aged in condition A (at $V_{GS} = 0$) before and after stress in (a) linear scale and (b) log scale

method extrapolation. It is very slightly affected. Indeed, a slight shift is observed in the negative direction of about 2 %, which is not significant compared to the dispersion of 1.5 % on virgin devices. The saturation drain current I_{DSS} decreases by 16 %. The peak position of the transconductance curve is very slightly shifted while its maximum G_{MMAX} decreases by 20 % at $V_{DS} = 4$ V which could be mainly related to mobility degradation and/or source resistance increase [5]. In addition, the current below the threshold increases from 6.5×10^{-6} to 4×10^{-3} A/mm as shown in figure 3.18 (b). In other studies, it has been reported that defects located in the gate-drain access region are strongly affecting the transconductance but only weakly the threshold voltage [6,7]. Figure 3.19 shows a typical evolution of $I_{GS} - V_{GS}$ characteristic before and after the stress sequence carried out in condition A.

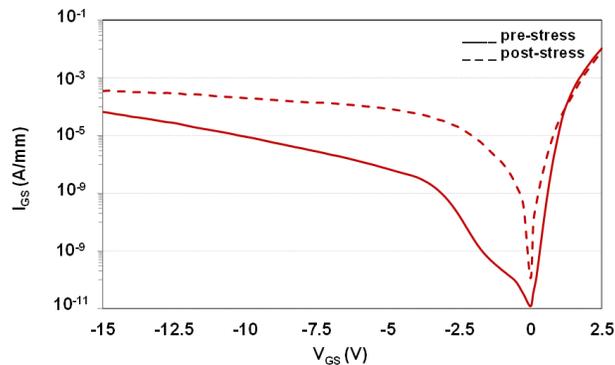


Figure 3.19: $I_{GS} - V_{GS}$ characteristic of a 75 nm gate length and 5.5 μm drain-source distance HEMT aged in condition A (at $V_{GS} = 0$) before and after stress

As shown in figure 3.19, the gate leakage has increased; I_{GINV} at $V_{GS} = -15$ V increases from

7×10^{-5} to 2×10^{-4} A. Furthermore, the Schottky barrier height ϕ_B and the ideality factor η are extracted to analyze the reason for the increase of the gate leakage current. It appears a lower barrier height and a higher ideality factor. This is probably due to the fact that some gate leakage mechanisms other than the thermionic emission mechanism become dominant with the stress (as the drain-source voltage rises). The ideality factor η increases by 80 % from 2.33 to 4.21 and the Schottky barrier height has reduced by 30 % from 0.66 eV to 0.47 eV after the stress sequence. Thus, a degradation of the Schottky contact is observed. Del Alamo et al. have shown under high voltage electrical stress that the drain current reduces, R_{DS} increases, the gate leakage current increases, and suggested that this was due to defects generated in AlGaN barrier [8]. This may also be due to inverse piezoelectric effect as a result of applied high electric field [8-10], a defect generation and the percolation process [11,12], or to electrochemical reactions occurring at the surface [13], In addition, several authors [12,14] indicated that the most important failure mode is the increase in the gate leakage current, which can be particularly detrimental in power applications, where leakage must be kept as low as possible to limit power losses. More detailed investigations are needed to identify the degradation mechanisms and modes, to understand if failure is due to the process or epitaxy related problems.

3.3.2.2 Off-state step stress tests

Representative results, obtained on a device with the shortest gate length $L_G = 75$ nm and $L_{DS} = 3.5$ μm is reported in the following figures. Figure 3.20 shows a typical evolution of $I_{DS}(I_{GS})-V_{DS}$ characteristics before and after the stress sequence performed under condition E (at $V_{GS} = -4$ V) (see figure 3.13).

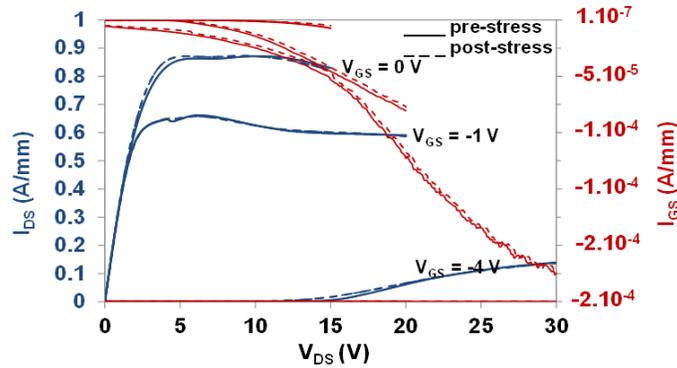


Figure 3.20: $I_{DS}(I_{GS})-V_{DS}$ characteristics of a 75 nm gate length and 3.5 μm drain-source distance HEMT aged in condition E (at $V_{GS} = -4$ V) before and after stress

Figure 3.21 shows a typical evolution of $I_{GS} - V_{GS}$ characteristics before and after the stress sequence performed under condition E (at $V_{GS} = -4$ V).

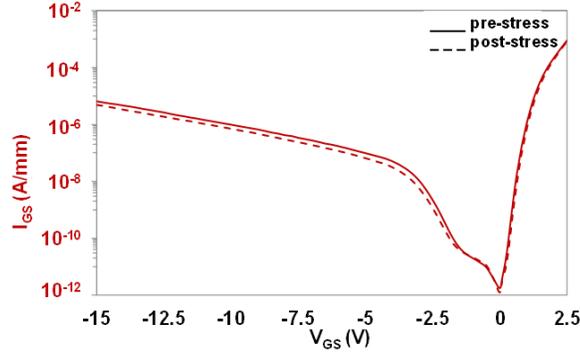


Figure 3.21: $I_{GS} - V_{GS}$ characteristic of a 75 nm gate length and 3.5 μm drain-source distance HEMT aged in condition E (at $V_{GS} = -4$ V) before (solid lines) and after stress (dashed lines)

Figure 3.22 shows a typical evolution of $I_{DS} (G_M) - V_{GS}$ and $I_{DS} - V_{GS}$ characteristics before and after the stress sequence performed under condition E (at $V_{GS} = -4$ V).

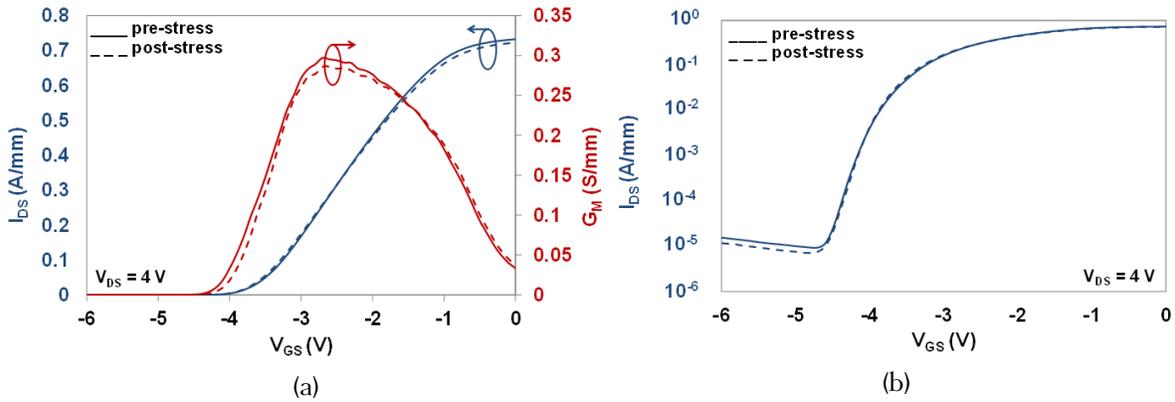


Figure 3.22: $I_{DS} (G_M) - V_{GS}$ characteristic of a 75 nm gate length and 3.5 μm drain-source distance HEMT aged in condition E (at $V_{GS} = -4$ V) before (solid lines) and after stress (dashed lines) in (a) linear scale and (b) log scale

The $I_{DS} (G_M) - V_{GS}$ and $I_{DS} - V_{GS}$ characteristic evolution before and after stress indicates that devices can withstand a V_{DS} voltage of 60 V without showing any degradation. Therefore, no piezo electrical influence is noticed. Among all 40 components submitted to aging tests, those submitted to off-state step stress tests undergo the smallest influence of aging sequence.

3.3.2.3 Electrical parameters evolution after on-state step stress tests

One to three HEMTs per geometry available were submitted to step stress sequence with the gate voltage fixed in condition A (at $V_{GS} = 0$ V) and the drain voltage increased by step of 5 V every 5

minutes until a decrease of the drain current of about 10 % is reached.

Main static parameters such as the saturation drain current, I_{DSS} , the transconductance peak, G_{MMAX} , the threshold voltage, V_{TH} , the Schottky barrier height, ϕ_B , and the ideality factor, η , were extracted before and after stress in order to identify and quantify the main performances of the technology and to better understand degradation signatures and root cause of failure mechanisms. The following tables show the electrical parameters evolution before and after stress.

Extraction conditions of the aforementioned parameters have been discussed in chapter 2 in section 2.4.1.2.

Table 3.4: Drain current saturation I_{DSS} , resistance R_{DS} , maximum transconductance G_{MMAX} and threshold voltage V_{TH} , evolution of typical devices before and after stress

Device geometry		I_{DSS} (A/mm)		R_{DS} (Ω mm)		G_{MMAX} (S/mm) at $V_{DS} = 4$ V	
L_{DS} (μ m)	L_G (nm)	Before stress	After stress	Before stress	After stress	Before stress	After stress
1.5	75	1.01	0.89	3.9	4.1	0.33	0.26
2.5	75	1	0.87	3.89	4.2	0.32	0.26
	100	0.9	0.85	3.15	3.3	0.29	0.25
	150	0.8	0.79	2.34	2.9	0.27	0.21
3.5	75	0.99	0.9	3.87	4.1	0.3	0.26
	100	0.9	0.77	3.13	3.3	0.29	0.23
	150	0.82	0.7	2.33	2.5	0.27	0.22
4.5	75	0.99	0.89	3.9	4.1	0.29	0.23
	100	0.91	0.8	3.14	3	0.28	0.23
	150	0.8	0.72	2.35	2.5	0.27	0.21
5.5	75	0.98	0.91	2.9	2.38	0.29	0.23
	100	0.93	0.81	3.12	3.3	0.28	0.22
	150	0.84	0.77	2.34	2.5	0.26	0.21

Table 3.5: Schottky barrier height ϕ_B , ideality factor η and inverse gate current I_{GINV} evolution of typical devices before and after stress

Device geometry		ϕ_B		η		I_{GINV} at $V_{GS} = -15$ V	
L_{DS} (μ m)	L_G (nm)	Before stress	After stress	Before stress	After stress	Before stress	After stress
1.5	75	0.70	0.49	2.4	4.3	-2.9	-86
2.5	75	0.68	0.49	2.3	4.2	-4.8	-2.10 ³
	100	0.69	0.47	2.5	4.5	-3.2	-106
	150	0.71	0.60	2.7	4.3	-3.8	-110
3.5	75	0.71	0.53	2.8	4.2	-3.2	-125
	100	0.67	0.45	2.4	4.3	-2.4	-2.10 ³
	150	0.70	0.50	2.3	4.2	-4.1	-1192
4.5	75	0.69	0.48	2.5	4.1	-3.8	-150
	100	0.70	0.52	2.8	4.6	-3.7	-103
	150	0.70	0.51	2.3	4.1	-2.9	-97
5.5	75	0.66	0.47	2.3	4.2	-4.1	-112
	100	0.71	0.51	2.3	4.1	-3.6	-88
	150	0.71	0.52	2.4	4.3	-2.7	-20

The results reported in table 3.4 show that the saturation drain current I_{DSS} decreases by 9 to 14 %, the maximum transconductance G_M decreases by 15 to 20 % and the threshold voltage. Table 3.5 shows a decrease of the Schottky barrier height ϕ_B by 20 % to 30 % and an increase of the ideality factor η by 70 % to 80 % after stress. We can conclude that the Schottky diode is degraded after stress.

3.3.2.4 Discussion on the degradation signatures on the basis of electrical parameters evolution in on-state conditions

The investigations carried out in the previous paragraphs show several trends: The saturation drain current decreased by approximately 10 % (which is the failure criterion), the drain-source resistance increased by 6 ± 2 %. This is usually attributed to hot electrons. Moreover, The Schottky contact suffered degradation, with almost a two to three order of magnitude increase in the reverse gate leakage current. Maximum transconductance presents a decrease by 17.5 ± 2.5 % while the threshold voltage is relatively unaffected. It has been reported in other studies that defects located in the gate-drain access region are strongly affecting the transconductance but only weakly the threshold voltage [6,7]. It was found too that V_{DS} degradation voltage at which the static and permanent degradation occurs, increases with V_{GS} becoming more negative.

We conclude that it is not only the electric field that leads to the degradation but rather more a combination of high current density, electric field and self-heating.

Previous studies indicated that HEMTs may present either:

- localized trapping processes [15,16], in which electrons are mainly trapped at the edge of the gate on the drain side due to high peak electric field [17]. This mechanism has a strong impact in RF devices, and usually decreases with increasing L_{GD} , since the peak electric field decreases for larger gate-drain distances [18].

- non-localized trapping processes [19,20], in which electrons are trapped in the whole gate-drain access region due to surface trapping [20-22], or non-localized hot electron trapping [19,23]. Trapping processes can play an important role in limiting the power devices performance.

3.3.3 Transient degradation

During the step stress sequences performed in on-state conditions to identify the critical degradation voltage, a drain current transient occurs at $V_{DS} = 5$ V as shown in figure 3.10 for a 75 nm gate length and 5.5 μm drain-source distance HEMT. The calculation of the time constants of intra-step drain current transients is necessary to provide information of the kinetic of trapping/detrapping mechanisms. There are different methods for the evaluation of time constants. It has been performed in this work using the fitting of the data by the stretched multi-exponential function given

by the following equation:

$$I_{DS}(t) = I_{DSf} + \sum_i^{\infty} a_i e^{-\frac{t}{\tau_i}} \quad (3.2)$$

Where the fitting parameters a_i , τ_i and N are, respectively, the magnitude of the trapping (detrapping) transients, the associated time constants τ_i , and the number of exponential components corresponding to the trapping/detrapping kinetics. N typically ranges between 2 and 4 depending on the analyzed devices. Positive values of a_i correspond to electron trapping processes while negative values correspond to electron detrapping processes. I_{DSf} is the current value at the end of the transient step. The I_{DS} current transients measured during step stress sequences were fitted by a sum of only two exponential components ($N = 2$), according to the aforementioned equation. Intra-step time constants of the drain current transients are extracted from the last two non-stressful steps at 5 V after the steps at 20V and 25V ($I_{DSfinal-1}$ and $I_{DSfinal}$). In Figure 3.23, an example of the drain current transients extracted from Figure 3.10 is shown for a typical device with 75 nm gate length and 5.5 μm drain-source distance during the step stress sequence performed in condition A (at $V_{GS} = 0$ V).

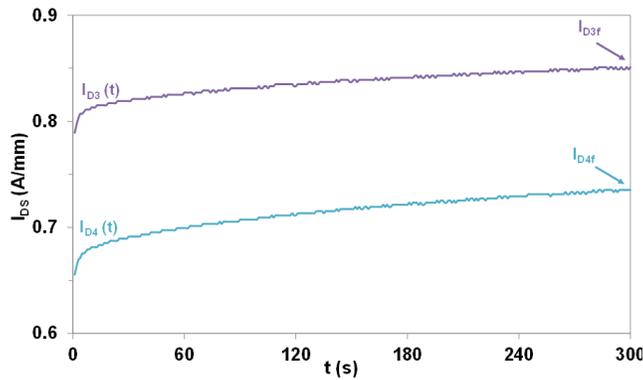


Figure 3.23: Current transients evolution to $V_{DS} = 5$ V versus time during the 2 last non-stressful aging steps at $V_{DS} = 5$ V in condition A (at $V_{GS} = 0$ V), of a 75 nm gate length and 5.5 μm drain-source distance HEMT (I_{D3} et I_{D4} extracted from figure 3.10)

As shown in Figure 3.23, the amplitude of the current transient $I_{D4}(t)$ obtained after a step stress at V_{DS} of 25 V is higher than the amplitude of the current transient $I_{D3}(t)$ obtained after a step stress at V_{DS} of 20 V. Figure 3.24 presents the modelling of $I_{D4}(t)$ transient using the above equation.

Two preminent time constants are extracted: τ_1 in the range of 2 to 4 minutes and τ_2 in the range of several seconds which are of the same order of magnitude for all drain current transients. Therefore, trapping-detrapping mechanisms are induced by similar traps in all devices and are

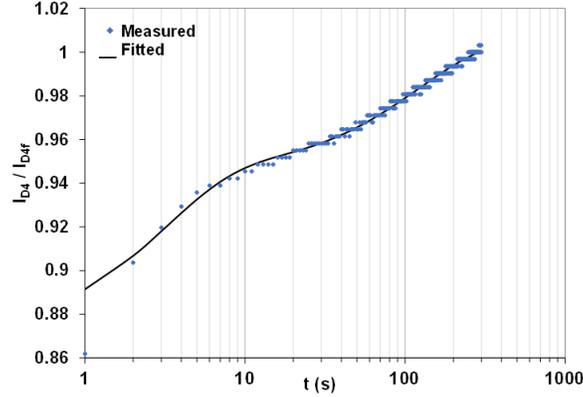


Figure 3.24: Fitting of I_{D4} transient in condition A (at $V_{GS} = 0$ V) at $V_{DS} = 5$ V by the stretched multi-exponential function of a 75 nm gate length and 5.5 μm drain-source distance HEMT)

Table 3.6: Time constants and dispersion of IDS transients recorded during the last two non-stressful steps for devices aged in conditions A (at $V_{GS} = 0$ V) and B (at $V_{GS} = -1$ V)

Aging conditions	$\tau_1(s)$	$\tau_2(s)$
A $I_{DS}^{final-1}$	143 ± 11	2 ± 1
A I_{DS}^{final}	214 ± 23	3 ± 1
B $I_{DS}^{final-1}$	131 ± 19	4 ± 1
B I_{DS}^{final}	146 ± 17	4 ± 2

enhanced by the stress tests (high value of V_{DS} voltage). These rather high values of the trap time constants indicates that traps could have high activation energy; their signature should be completed by I_{DS} transient measurements as a function of temperature.

3.4 Safe Operating Area (SOA)

3.4.1 Principle of determination of the SOA

One of the criteria to address reliability concern in HEMT devices is its Safe Operating Area (SOA), which means the domain of operating conditions without self-damage. On the basis of the results described above and regarding the critical degradation voltage, the operating area without degradation was determined for HEMTs of each geometry.

Figure 3.25 shows the DC safe operating area for GaN HEMT with a gate length of 75 nm and a drain-source distance of 1.5 μm . The dashed line presents the boundary of the operating zone without degradation. Operation of the transistor out of this limit leads to catastrophic degradation.

For every stress conditions, several samples were stressed. The results of these experiments

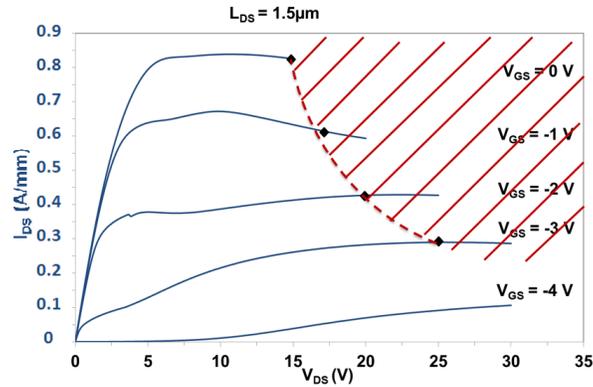


Figure 3.25: SOA of HEMTs ($L_G = 75 \text{ nm}$, $L_{DS} = 1.5 \mu\text{m}$) The rhombuses correspond to the critical degradation voltage V_{DS} causing an I_{DS} decrease of about 10 %

are reported in table 3.7 for devices with $L_G = 75 \text{ nm}$. The devices were stressed with increasing V_{DS} voltages until they failed. In this study, the safe operating area is defined for failure criteria of about 10 % drop in the drain source current I_{DS} and consequently, is determined through the evolution of the critical degradation voltage V_{DSdeg} as a function of V_{GS} .

Table 3.7: Critical degradation voltage of 75 nm gate length HEMTs with drain source distance ranging from 1.5 to 5.5 μm while V_{GS} was kept constant to 0, -1, -2 or -3 V

L_{DS} (μm)	V_{DSdeg} (V)			
	Condition A (at $V_{GS} = 0$ V)	Condition B (at $V_{GS} = -1$ V)	Condition C (at $V_{GS} = -2$ V)	Condition D (at $V_{GS} = -3$ V)
1.5	15	15/20	20	25
2.5	20	20	25	30
3.5	20	20	25	30
4.5	25	25	30	40
5.5	25	30	40	50

It is important to point out that the former results were obtained at room temperature and for short aging test duration. So, more or less severe stress conditions such as ambient temperature higher than 300 K and long term aging tests could lead to a shift to the left or the right of the contour delimiting the transistor safe operating area.

Figure 3.26 shows the On-operating areas of a typical transistor ($L_G = 75 \text{ nm}$, $L_{DS} = 1.5 \mu\text{m}$).

From the results analysis of the aging tests, in "on-state" mode, it is possible to define three operating zones not involving the same risk as regards the appearance of degradation:

- A safe operating zone of the transistor where the drift of the drain current at $V_{DS} = 5 \text{ V}$ during the aging sequence is much lower than the failure criterion, i.e. 10 %. In this case, it is the

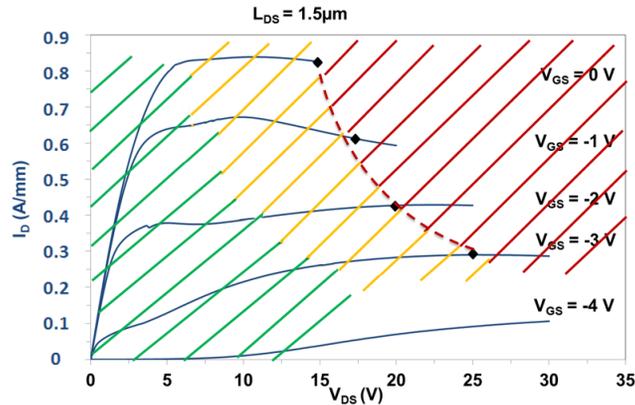


Figure 3.26: On-operating areas of a typical transistor HEMTs ($L_G = 75$ nm, $L_{DS} = 1.5$ μm)

safe operating area defined by the green region.

- A permissible operating zone of the transistor where the drift of the drain current at $V_{DS} = 5\text{V}$ during the aging sequence is lower than the failure criterion. In this case, it is the operation area corresponding to the yellow region, which will be used for future long term reliability tests.

- A forbidden operating zone where the drift of the drain current at $V_{DS} = 5\text{V}$ during the aging sequence exceeds the failure criterion. This area corresponds to the operating area defined by the red region.

Dissipated power in stressing conditions were also determined and results are depicted in figure 3.27 for two HEMT geometries ($L_G = 75$ nm, $L_{DS} = 1.5$ μm) and ($L_G = 75$ nm, $L_{DS} = 5.5$ μm). We can note that dissipated power is constant in stressing conditions expect in off-state conditions. Then, it suggests that it is not only the electric field that leads to the degradation but rather more a combination of high current density, electric field and self-heating.

3.4.2 Critical degradation voltage variation with device geometry

To assess the relation between the critical degradation voltage and the device geometry, similar step stresses were applied for different gate lengths and different drain-source distances while V_{GS} was kept constant to 0, -1, -2 or -3 V. The gate-source distance is 600 nm for all devices as previously mentioned. Four devices, of each available geometry, were aged and the results are reported in figure 3.28 and figure 3.30 for the step stress sequence A, i.e. at $V_{GS} = 0$ V and in figure 3.29 and figure 3.31 for the step stress sequence B, i.e. at $V_{GS} = -1$ V. The critical V_{DS} degradation voltage is defined, as previously described, such as the drain current decreases approximately by 10 % at $V_{DS} = 5\text{V}$.

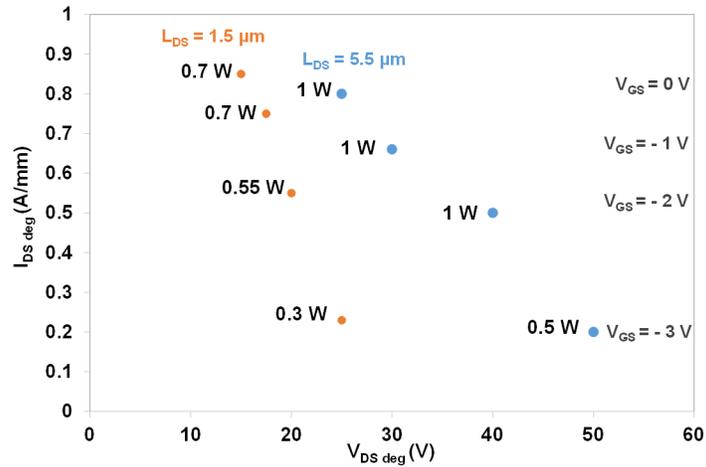


Figure 3.27: Dissipated power in stressing conditions for HEMTs under test of two geometries ($L_G = 75\ nm$, $L_{DS} = 1.5\ \mu m$) and ($L_G = 75\ nm$, $L_{DS} = 5.5\ \mu m$)

3.4.2.1 Critical degradation voltage variation with the gate length L_G

Figure 3.28 and Figure 3.29 show the relation between the critical degradation voltage and the gate length for devices having a drain-source distance of $2.5\ \mu m$ in condition A and of $5.5\ \mu m$ in condition B, respectively. Shorter L_G results in an increase of the electric field at the gate edge towards the drain [24]. Consequently, the V_{DS} degradation voltage, at which degradation occurs, increases with the gate length.

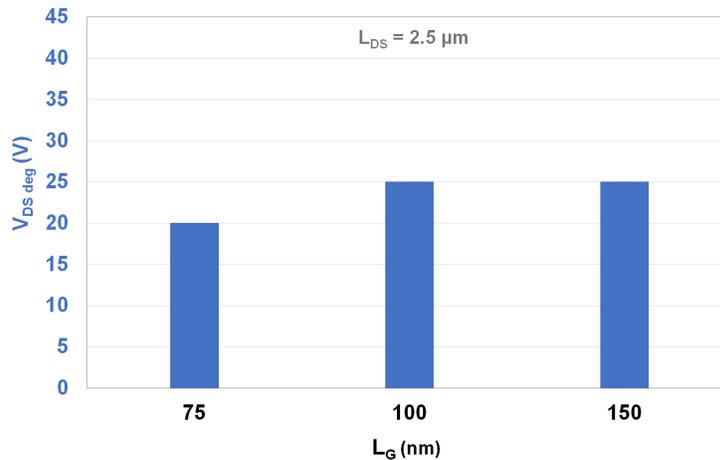


Figure 3.28: Relation between the critical degradation voltage and the gate length in condition A (at $V_{GS} = 0\ V$)

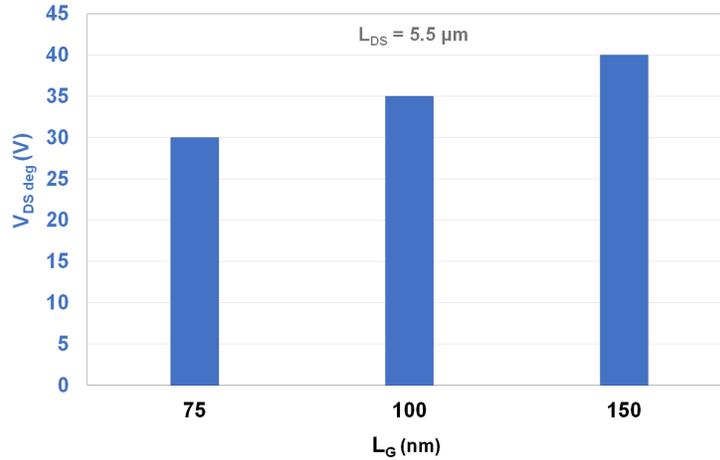


Figure 3.29: Relation between the critical degradation voltage and the gate length in condition B (at $V_{GS} = -1$ V)

3.4.2.2 Critical drain source voltage variation with the gate-drain distance L_{GD}

Figure 3.30 and figure 3.31 show the relation between the critical degradation voltage and the drain-source distance (varying as L_{GD}) for devices a gate length of 75 nm in condition A and of 100 nm in condition B, respectively.

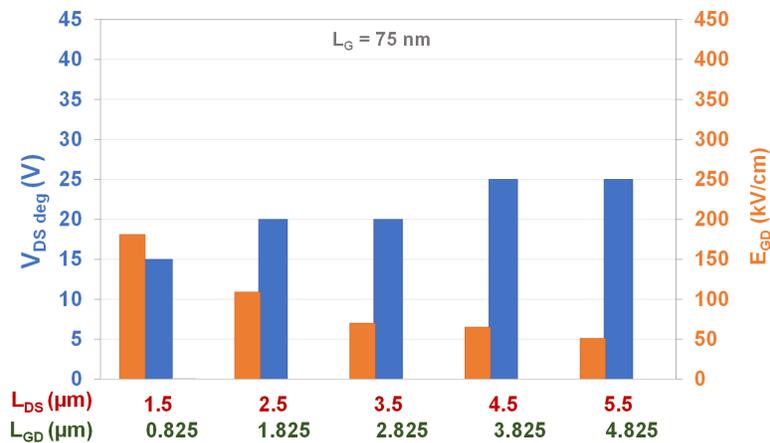


Figure 3.30: Relations between the critical degradation voltage, the electric field E_{GD} and the drain-source distance L_{DS} (varying as L_{GD}) in condition A (at $V_{GS} = 0$ V)

High drain-source voltage generates a substantial increase in the electric field, which is maximal at the gate edge on the drain side of the device. The maximum electric field is lower for longer gate-drain distance. As a consequence, the V_{DS} degradation voltage at which the degradation oc-

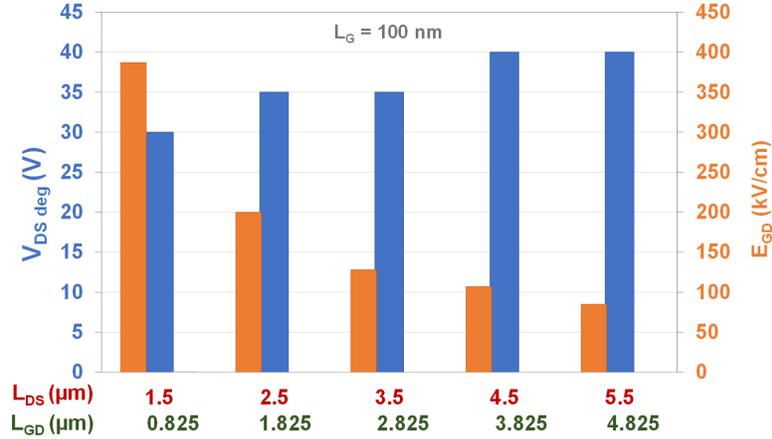


Figure 3.31: Relations between the critical degradation voltage, the electric field E_{GD} and the drain-source distance L_{DS} (varying as L_{GD}) in condition B (at $V_{GS} = -1$ V)

curs, increases with the drain-source distance L_{DS} and L_{GD} . The degradation under conditions of high electric field between the gate and the drain has been reported to be caused by hot electrons [25].

To better understand the origin of degradation, we have compared the key parameters evolution: critical degradation voltage, $V_{DS \text{ deg}}$, electric field, E_{GD} , and dissipated power, P , in stressing conditions as a function of V_{GS} voltage for HEMTs with the same geometry, $L_G = 75$ nm, $L_{DS} = 5.5$ μm .

Table 3.8: Critical degradation voltage, electric field and dissipated power of 75 nm gate length and a 5.5 μm drain source-distance HEMTs for step stress sequences A ($V_{GS} = 0$ V), B ($V_{GS} = -1$ V), C ($V_{GS} = -2$ V) and D ($V_{GS} = -3$ V)

Aging conditions	V_{DEdeg} (V)	E_{GD} (kV/cm)	P (W)
Condition A (at $V_{GS} = 0$ V)	25	51	1
Condition B (at $V_{GS} = -1$ V)	30	64	1
Condition C (at $V_{GS} = -2$ V)	40	87	1
Condition D (at $V_{GS} = -3$ V)	50	109	0.5

As shown in table 3.8, for a devices with $L_G = 75$ nm and $L_{DS} = 5.5$ μm , the critical degradation voltage and the electric field increase when V_{GS} becomes more negative while the DC dissipated power is of about 1 W, in stressing conditions in conditions A, B and C. and decreased

by 50 % in condition D ($V_{GS} = -3$ V).

In conditions A, B and C, under the assumption that device self-heating is proportional to the dissipated power, the junction temperature in these experiments should be relatively unchanged. When V_{GS} becomes more negative, the degradation is greatly reduced due to the reduction of electron density in the channel. This leads to a higher critical degradation voltage. In this case, the electric field is the preminent degradation factor. In condition D, both electric field and thermal effects lead to the degradation.

3.4.2.3 SOA assessment as a function of the device geometry

For determining the SOA as a function of the geometry, step stress sequences A ($V_{GS} = 0$ V), B ($V_{GS} = -1$ V), C ($V_{GS} = -2$ V) and D ($V_{GS} = -3$ V) have been applied on devices of 75 nm gate length HEMTs with drain-source distance ranging from 1.5 to 5.5 μm . The critical degradation drain voltage has been determined for each aging sequence and each geometry. The results are already shown in table 3.7. Using the table 3.7, the SOA boundary of HEMTs with different geometries can be determined. Figure 3.32 presents the SOA for 75 nm gate length and 1.5 or 5.5 μm drain source distance HEMTs.

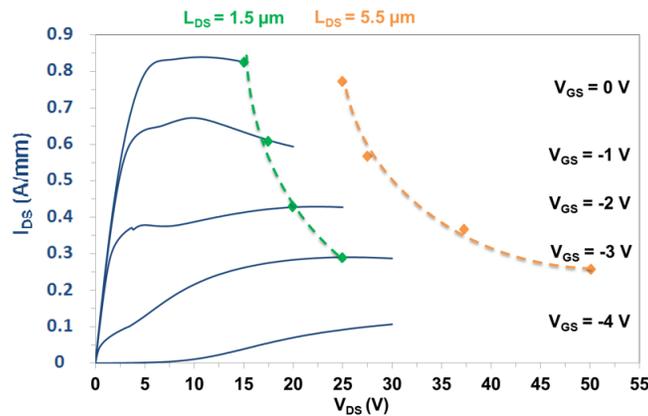


Figure 3.32: SOA of 75 nm gate length HEMTs with drain source distance of 1.5 and 5.5 μm . The rhombuses correspond to critical degradation voltage V_{DS} inducing a drift of I_{DS} around 10 %

The dashed line presents the SOA boundary

In summary, as shown in figure 3.32, as the V_{DS} degradation voltage at which degradation occurs increases with the drain-source distance L_{DS} , the SOA is shifted towards the high values of V_{DS} as the drain-source distance increases. It means that devices with large drain-source spacing are more robust.

3.5 Analysis of TLMS after aging tests

The TLM is the most employed method to determine the experimental parameters of ohmic contact (contact resistance, sheet resistance and specific contact resistance). These structures which are essentially HEMT without gate, provides the opportunity to understand and investigate the source-drain conduction path. At least 4 TLM structures per inter-electrode distance were investigated.

More than 12 TLM structures with contact distances of 2, 5, 10 and 20 μm and a total width of 100 μm were also stressed in order to eliminate the effect of the gate on the device and locate degradations stemming from the channel and the contacts respectively. The same methodology as HEMTs was investigated: a sequence of step stress tests has been applied until a degradation criterion is reached. It is composed of a stressful biasing for 5 minutes followed by a non-stressful biasing for 5 minutes in nominal conditions. Then, the former sequence is repeated several times with more severe bias conditions.

Figure 3.33 shows a representative result of the current evolution versus time of different TLMS as a function of the spacing, when the voltage is increased by step of 5 V every 5 minutes. The degradation criterion of TLM is found to be about 6 to 7 %. Exceeding this percentage, a catastrophic degradation occurs as shown in the top of figure 3.33.

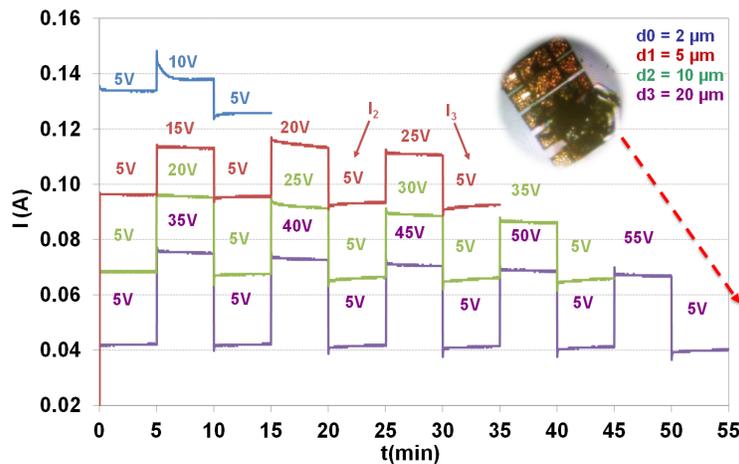


Figure 3.33: Current evolution versus time of 2, 5, 10 and 20 μm TLM spacing. On the top right, image of TLM after a catastrophic degradation occurring at voltage of 60 V for a 20 μm TLM spacing.

Figure 3.34 shows a representative result of the current evolution versus time of 5 μm TLM spacing.

Figure 3.35 shows a typical evolution of I-V characteristics before and after the stress sequence of a 5 μm TLM spacing. In attempt to identify the degradation mechanisms, we compare these

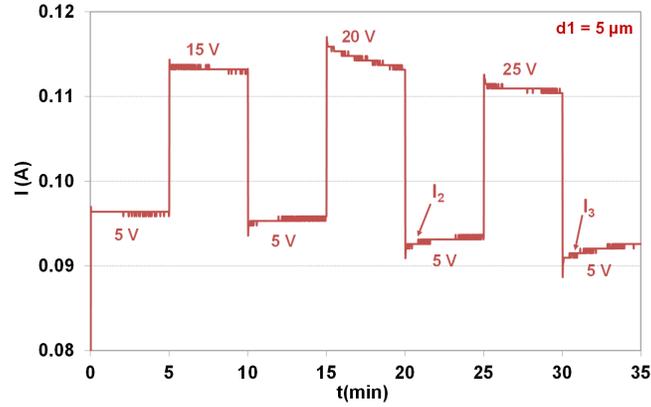


Figure 3.34: Current evolution versus time of $5 \mu m$ TLM spacing

characteristics with the ones measured after a storage at room temperature during 24 hours.

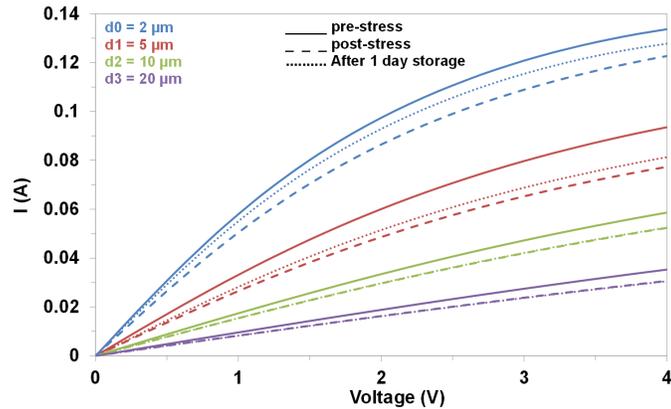


Figure 3.35: Current evolution versus time of $5 \mu m$ TLM spacing

In figure 3.35, the observed shift of the I-V characteristics shows that only a fraction of the degradation of the current is permanent. Partial recovery after one-day storage indicates that trapping and de-trapping mechanisms can contribute to the degradation.

A typical TLM extraction which gave an average value and its dispersion of contact resistance R_C and sheet resistance R_{\square} specific contact resistance ρ_C and transfer length L_T before and after stress is depicted in table 3.9.

As can be seen in table 3.9, the device resistance increase was dominated by change of the sheet resistance R_{\square} and not of the contact resistance because the increase of R_C and ρ_C is not significant compared to the dispersion. Therefore, degradation is probably located in the channel which means a degradation of 2DEG density (n_s) and/or the mobility.

During the step stress sequences, a current transient occurs during the step performed at

Table 3.9: TLM parameters extracted before and after stress

TLM parameters	Before stress	After stress
R_C ($\Omega\cdot\text{mm}$)	0.6 ± 0.05	0.7 ± 0.05
R_{\square} (Ω/\square)	435 ± 6	465 ± 5
L_T (μm)	1.25 ± 0.15	1.4 ± 0.1
ρ_C (Ωcm^2)	$8 \times 10^{-6} \pm 10^{-6}$	$11 \times 10^{-6} \pm 10^{-6}$

$V = 5$ V. In figure 3.36, an example of the current transients extracted from figure 3.34 is shown for a typical $5 \mu\text{m}$ TLM.

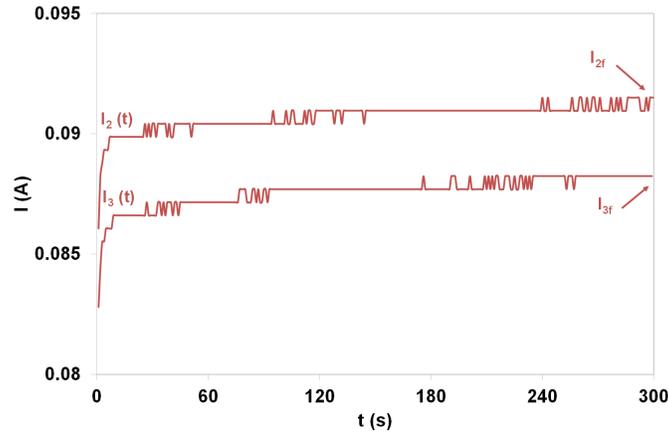


Figure 3.36: Current transients evolution versus time during the last two non-stressful aging steps at $V = 5$ V, for $5 \mu\text{m}$ TLM (extracted from figure 3.36)

Different TLM spacing were tested and then compared, by terms of degradation criterion, critical degradation voltage and time constants of current transients, to HEMTs with close value of drain-source distance L_{DS} . Table 3.11 and table 3.10 summarize the details of parameter extraction results of TLM patterns of $5 \mu\text{m}$ length and $5.5 \mu\text{m}$ drain-source distance HEMTs. The results clearly show that the critical degradation voltage is similar and about 25 V for both TLM patterns of $5 \mu\text{m}$ length and $5.5 \mu\text{m}$ drain-source distance ($4.825 \mu\text{m}$ gate-drain distance) HEMTs.

All current transients exhibit two preminent time constants τ_1 in the range of several minutes and τ_2 in the range of several seconds, which are of the same order of magnitude for all stress sequences in TLMs as well as in HEMTs. Therefore, trapping-detrapping phenomena are induced by similar traps in all devices and are enhanced by the stress tests.

In summary, comparing results of TLM spacing and HEMTs with close value of drain source distance L_{DS} , their critical degradation voltage and electric field are similar. In addition, the signature of the degradation is similar for HEMTs and TLM in term of transient evolution and permanent current decrease. Therefore, the origin of the observed degradations in HEMTs and TLMs struc-

Table 3.10: Summary of parameter extraction results of TLMs

Samples	d (μm)	V_{deg} (V)	E (kV/cm)	τ (s) $I_{final-1}$	τ (s) I_{final}
TLM 1	5	25	50	$\tau_1=50.14$ $\tau_2=1$	$\tau_1=270.74$ $\tau_2=1$
TLM 2				$\tau_1=55.25$ $\tau_2=1$	$\tau_1=84.6$ $\tau_2=1.63$
TLM 3				$\tau_1=87.65$ $\tau_2=1.81$	$\tau_1=87.17$ $\tau_2=1.86$
TLM 4				$\tau_1=193.39$ $\tau_2=1.34$	$\tau_1=144.5$ $\tau_2=1.32$

Table 3.11: Summary of parameter extraction results of HEMTs

Samples	L_G (nm)	L_{DS} (μm)	L_{GD} (μm)	V_{DSdeg} (V)	E_{GD} (kV/cm)	τ (s) $I_{final-1}$	τ (s) I_{final}
HEMT 1	75	5.5	4.825	25	51	$\tau_1=132.24$ $\tau_2=1.81$	$\tau_1=205$ $\tau_2=1.82$
HEMT 2						$\tau_1=138.74$ $\tau_2=2.66$	$\tau_1=187.24$ $\tau_2=2.4$
HEMT 3						$\tau_1=139.83$ $\tau_2=2.3$	$\tau_1=141.46$ $\tau_2=2.41$
HEMT 4						$\tau_1=154.34$ $\tau_2=2.19$	$\tau_1=267.88$ $\tau_2=2.92$

tures seems to be same and could stem from modification of electron transport mechanisms in the channel.

Chou [25] reported a similar outcome as a result of accelerated stressing and suggested that the gate metal is probably not the origin of the degradation. We agree with this assertion, based on results involving TLM stress testing, since it appears that the gate is indeed not responsible for the degradation. Since the TLM structures are on the same wafer, with the same ohmic contact metals as the HEMTs, we can conclude that the channel, the source-drain conduction path, are the origin of degradation of the HEMTs. The observed degradation appears not to be related to the interaction of the gate with the channel.

3.6 Conclusion chapter 3

In this study, the objective was to perform a robustness assessment of short gate MOCVD GaN HEMTs on Si substrate. For that, a methodology has been defined for in-situ diagnosis of permanent

degradation. This study aims at defining safe operating DC conditions by on-state aging sequences comprising stressful steps and non-stressful steps.

One set of devices per geometry was submitted to stress sequence in order to induce progressive degradation mechanisms for HEMTs featuring gate lengths ranging from 75 to 150 nm. Two degradation signatures were identified:

i) Static and permanent degradation which is quantified by the decrease of the drain current on successive 5 V non-stressful steps. It is found that V_{DS} degradation voltage, at which static and permanent degradation occurs, increases with V_{GS} aging condition becoming more negative. The V_{DS} degradation voltage is also found lower for the shortest gate length L_G devices and gate-drain distance L_{GD} devices.

ii) Intra-step degradation identified by a drain current transient occurring during each step of the aging sequence. These drain current transients reflect trapping-detrapping phenomena. Furthermore, the analysis of I_{DS} transients recorded during the stress sequence has shown that the amplitude of the transient mechanisms increases when the V_{DS} degradation voltage is reached. All I_{DS} transients exhibit two preeminent time constants τ_1 in the range of 2 to 4 minutes and τ_2 in the range of several seconds, which are of the same order of magnitude for all stress sequences. Therefore, trapping-detrapping phenomena are induced by similar traps in all devices and are enhanced by the stress tests.

In this study an investigation of the SOA of ultra-short gate AlGaN/GaN HEMT devices is presented. It is based on the determination of the maximum values of DC bias voltages. HEMTs grown by MOCVD were studied and failure points were measured at different bias conditions. The methodology consists in applying accelerated DC step stresses until a failure criterion was observed. It was found that the SOA is shifted toward the high values of V_{DS} as the drain-source distance increases.

Finally, an analysis of TLM is presented. It suggests that traps responsible for currents transients occurring as well in HEMTs as in TLMs are rather more located in the channel. Based on the values of the associated time constants, it is likely that these traps are characterized by significant activation energies.

Step stress test is considered as an effective method for evaluating the device robustness. The next step will investigate the long term reliability tests and degradation mechanisms to better understand degradation signatures and root cause failure mechanisms.

References Chapter 3

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Conclusion

In this research study, the objective was to perform a reliability study of ultra-short gate AlGaIn/GaN high electron mobility transistor (HEMT) on silicon substrate dedicated to microwave power applications. This work was carried out within IMS Bordeaux and IEMN Lille laboratories.

The unique physical properties of III-nitride compound semiconductors, in particular the Gallium Nitride (GaN), were presented in chapter 1. The structure of GaN based HEMT, its operating principle and its applications have been detailed. AlGaIn/GaN HEMT has demonstrated excellent high power and high frequency performance compared with counterparts based on other materials. However, there are still some issues limiting the device operating applications impeding the way to commercialization. Indeed, reliability has still to be fully demonstrated due to the continuous evolution of the material and technological process. The final part of this chapter was devoted to reliability issues, accelerated life testing, GaN HEMT trapping effects and degradation mechanisms. They were reviewed and a particular attention was given to the GaN HEMT with ultra-short gate of 75, 100 and 150 nm.

In chapter 2, a description of the devices under test and the key technological steps was discussed. Another part of this chapter presents the electrical characteristics of HEMT components issued from AlGaIn/GaN HEMT MOCVD technology and AlGaIn/GaN HEMT MBE technology and fabricated at IEMN. The measurements consisted in standard DC and RF characterizations. The DC characterization was carried out in order to study the electrical behavior and the dispersion of the electrical parameters of the studied transistors. Then, the RF characterization was carried out in order to assess high frequency performance. This study permits to evaluate the impact of the geometry on the component performance so as to determine the optimum topology in terms of gate length, gate-source distance and drain-source distance and finally to obtain the best performances in static mode and in terms of cut-off frequencies. For the studied devices, results indicated that devices grown by MOCVD exhibit larger drain current saturation, I_{DSS} , cut-off frequency, f_T and maximum oscillation frequency, f_{MAX} , especially for short gate lengths. Through DC and dynamic electrical behavior of the transistors and their performance homogeneity within the wafers, a set of 40 transistors of the AlGaIn/GaN MOCVD technology and 14 transistors of the AlGaIn/GaN MBE

technology of different geometries has been chosen to be submitted to the aging tests.

Chapter 3 presents a reliability campaign. 40 devices per geometry were submitted to different step stress sequences in order to induce a progressive degradation for electrical parameters for HEMTs featuring gate lengths ranging from 75 to 150 nm. A new methodology based on a sequence of step stress tests was defined. The advantage of this method is the possibility to diagnose permanent degradation without removing the device under test from the test bench and without performing complete electrical characterization.

Two degradation signatures were identified:

i) Static and permanent degradation which is quantified by the decrease of the drain current on successive 5 V non-stressful steps. It is found that V_{DS} degradation voltage, at which static and permanent degradation occurs, increases with V_{GS} becoming more negative. The V_{DS} degradation voltage is also found lower for the shortest gate length L_G devices and gate-drain distance L_{GD} devices. We suggest that both self-heating and the electrical field magnitude contribute to the degradation of the electrical performance of the devices under tests.

ii) Intra-step degradation identified by a drain current transient occurring during each step of the aging sequence. These drain current transients reflect trapping-detrapping phenomena. Furthermore, the analysis of I_{DS} transients recorded during the stress sequence has shown that the amplitude of the transient mechanisms increases when the V_{DS} degradation voltage is reached. All I_{DS} transients exhibit two preeminent time constants τ_1 in the range of 2 to 4 minutes and τ_2 in the range of several seconds, which are of the same order of magnitude for all stress sequences. Therefore, trapping-detrapping phenomena are induced by similar traps in all devices and are enhanced by the stress tests.

In this study an investigation of the safe operating area (SOA) of ultra-short gate AlGaIn/GaN HEMT devices is presented. It is based on the determination of the maximum values of DC bias voltages. It was found that the SOA is shifted toward the high values of V_{DS} as the drain-source distance increases. Finally, an analysis of TLM is presented. It suggests that traps responsible for currents transients occurring as well in HEMTs as in TLMs are rather more located in the channel.

By means of short-term on wafer tests, well-defined degradation signatures and safe operating condition limits were determined.

Future work

Short-term tests are useful in this study for identifying early failures during technology development, in order to improve material, process and device design intrinsic and extrinsic weaknesses. To stabilize processes, extremely accelerated conditions can be used, in order to obtain information concerning possible failure mode and mechanisms. Degradation signatures of the MOCVD

technology under study were defined, but this do not provide any information on degradation kinetics, activation energies, mean time to failures and their extrapolation models. In order to get confidence on the reliability of the technology under study in this thesis, long-term tests are required, increasing significantly the complexity of the reliability evaluation process. Thus, it will be possible to highlight activation energy by reiterating these studies as a function of temperature and / or use other techniques or models such as the variation of the slope below the threshold or the modeling of the Schottky contact.

The long-term accelerated aging test bench adequate to device on package was already developed. A long-term reliability campaign for GaN-based devices will be performed. The choice of conditions for DC long-term life tests will take into consideration the combination of the main accelerating factors: hot electrons, electric field, and thermal effects, as suggested by the results of short-term tests in this work.

The work carried out in this thesis is a starting point for many possible works. There are many ways to pursue this topic further using packaged devices mainly the low frequency noise measurements in order to characterize the parasitic effects and to study phenomena related to traps and interface states, the low frequency noise measurements versus temperature to study the trapping/detrapping phenomena and determine the activation energy of traps in the epitaxial structure. Besides, the long-term accelerated aging tests under electrical and thermal conditions (HTOL and HTRB) in order to model the temporal drifts of the characteristic parameters as a function of the activation factors, for example thermal storage tests at three temperatures will be carried out, with the aim of studying purely thermally activated failure mechanisms and to extract their activation energy, or submitting the devices under 2 bias points, 2 temperatures conditions in order to study the effect of combined electric field, current, temperature and as as consequence to identify the electrical parasitic effects and the degradation mechanisms.

Résumé

Le matériau GaN ou arséniure de gallium, connu dès le début du 20^{ème} siècle, n'a pu être synthétisé avec des propriétés physiques et électriques utiles pour les composants semi-conducteurs que beaucoup plus tard. Ce n'est en effet qu'en 1991, que la démonstration d'un gaz bidimensionnel d'électrons à l'interface d'une hétérojonction AlGa_N/Ga_N sur substrat saphir a pu être réalisée.

Ces travaux ont permis la fabrication du transistor à haute mobilité électronique (HEMT) issu de la filière de Nitrure de Gallium (Ga_N). Ce dernier a démontré des performances impressionnantes en puissance hyperfréquence et est perçu dans de nombreuses applications comme le composant du futur. Ceci est dû principalement aux propriétés du matériau Ga_N, telles qu'une large bande interdite directe (3,4 eV à température ambiante), un champ de claquage élevé (3,3 MV/cm), une vitesse de saturation des électrons élevée ($2,7 \times 10^7$ cm/s), une haute mobilité électronique (900 cm²/Vs), un point de fusion élevé, une constante diélectrique relativement faible.

Cependant, ces composants à base de Ga_N sont sujets à divers effets, inhérents à la qualité de l'hétérostructure AlGa_N/Ga_N fabriquée sur différents substrats, et qui sont susceptibles de dégrader leurs performances électriques, et leur fiabilité. Par conséquent, la fiabilité des HEMTs Ga_N doit être pleinement démontrée avant leur intégration dans les systèmes et davantage d'investigations sont nécessaires pour améliorer la technologie des dispositifs, l'épitaxie, la conception et d'autres facteurs limitant leurs performances.

Différents types de substrats semi-conducteurs ont été considérés pour le HEMT à base de Ga_N, en raison de leurs propriétés thermiques, leur disponibilité et leur coût. En particulier, le silicium, disponible en wafer de grande taille, sa maturité technologique et son faible coût en font un substrat très attrayant.

Au cours des dernières années, on a observé une tendance continue, d'une part à augmenter la densité de puissance et d'autre part à minimiser les empreintes des composants. En particulier, l'amélioration de la performance en fréquence des HEMTs Ga_N est obtenue grâce à la réduction de la longueur de la grille (< à 100 nm) tout en respectant la limitation du rapport d'aspect, rapport entre longueur de grille et épaisseur de couche barrière AlGa_N.

Dans ce contexte, cette thèse porte sur l'évaluation de la fiabilité des HEMTs GaN sur substrat Si (III) à grille ultra-courte, dédiés aux applications de puissance à fréquence supérieure à 40 GHz.

Ce travail a été réalisé en collaboration entre le laboratoire d'Intégration du Matériau au Système (IMS), Université de Bordeaux et l'Institut d'Electronique, de Microélectronique et de Nanotechnologie (IEMN), Université de Lille I.

Dans le cadre de ces travaux, on a étudié deux technologies fournies par l'IEMN et dont l'épitaxie est réalisée par le CHREA-CNRS, soit par croissance MOCVD soit par croissance MBE.

Les dispositifs sous test ainsi que les étapes technologiques clés ont été décrits. Ensuite, une caractérisation DC a été réalisée afin d'étudier le comportement électrique et la dispersion des paramètres électriques des transistors étudiés. Puis, une caractérisation RF a été réalisée afin d'évaluer les performances à haute fréquence. Cette étude a permis d'évaluer l'impact de la géométrie sur les performances statiques et fréquentielles des composants afin de déterminer la topologie optimale en termes de longueur de grille, de distance grille-source et de distance drain-source. Ces caractérisations visaient aussi à vérifier le comportement électrique statique et dynamique des dispositifs et l'homogénéité des performances des transistors issus du même wafer.

Après avoir caractérisé les composants, analysé l'influence de la géométrie, la dispersion et identifié les effets parasites de fonctionnement, des tests de vieillissement accéléré sous contraintes échelonnées ont été effectués pour évaluer la robustesse des transistors HEMTs obtenus par croissance MOCVD.

Une méthodologie a été définie pour le diagnostic in-situ de la dégradation permanente. Elle consiste à effectuer des séquences de paliers de vieillissement sous tension de polarisation. La tension V_{DS} est augmentée par palier de 5 V tout en maintenant la tension V_{GS} constante. Chaque séquence de paliers de vieillissement est appliquée jusqu'à ce qu'un critère de dégradation soit atteint. Chaque palier comprend une phase de 5 ou 15 minutes sous conditions de vieillissement et une autre phase de 5 ou 15 minutes sous conditions de polarisation nominales. Ces séquences de tests de vieillissement ont été réalisées en condition de polarisation « on-state » i.e. à $V_{GS} = 0$, -1, -2, -3 V ou « off-state » à $V_{GS} = -4$ V.

Un ensemble de dispositifs de géométrie différente a été soumis à des séquences de vieillissement afin d'induire des mécanismes de dégradation progressifs pour des HEMTs de longueur de grille de 75, 100 ou 150 nm.

Deux types de dégradation ont été identifiés:

i) Une dégradation statique et permanente quantifiée par la diminution du courant de drain observée sur les paliers successifs effectués en conditions nominales à $V_{DS} = 5$ V.

La valeur de la tension critique de dégradation à partir de laquelle le courant de drain commence

à diminuer de façon significative dépend des conditions de polarisation du vieillissement, de la distance grille-drain et de la longueur de grille; elle est d'autant plus importante que la tension V_{GS} est plus négative. La tension critique de dégradation V_{DS} est également trouvée plus faible pour les transistors ayant des longueurs de grille L_G et des distances grille-drain L_{GD} plus courtes. Il a été démontré que le champ électrique et la puissance dissipée sont des facteurs d'accélération de la dégradation.

ii) Une dégradation transitoire observée au cours des paliers; il s'agit d'un transitoire de courant de drain, se produisant à chaque palier de la séquence de vieillissement.

Ces transitoires de courant de drain reflètent des phénomènes de piégeage et de dé-piégeage des porteurs. Tous les transitoires de courant de drain I_D présentent deux constantes de temps prédominantes; τ_1 d'environ 2 à 4 minutes et τ_2 d'environ plusieurs secondes, qui sont du même ordre de grandeur pour toutes les séquences de vieillissement. Par conséquent, les mécanismes de piégeage et dé-piégeage sont induits par des pièges similaires dans tous les dispositifs et sont renforcés par les essais de vieillissement accéléré sous polarisation.

Par ailleurs, l'aire de sécurité de fonctionnement (SOA) de cette technologie a été déterminée et sera une base pour définir les conditions de polarisation des futurs tests de vieillissement de longue durée. L'étude de la SOA est basée sur la détermination des valeurs maximales des tensions de polarisation DC qui permettent un fonctionnement des transistors sans dégradation. Les HEMTs obtenus par croissance MOCVD ont été étudiés et les tensions critiques de dégradation ont été déterminées sous plusieurs conditions de polarisation.

Il a été constaté que la frontière de la SOA est décalée vers les valeurs de V_{DS} plus élevées lorsque la distance drain-source augmente.

Enfin, afin de localiser l'origine des dégradations, des séquences de vieillissement accéléré sous contraintes échelonnées ont été effectuées sur des structures de test de type TLM d'espacements différents.

La tension critique de dégradation est trouvée plus faible pour la distance inter électrode la plus courte. Deux constantes de temps prédominantes sont extraites: τ_1 de l'ordre de 1 à 3 minutes et τ_2 de l'ordre de plusieurs secondes. Elles sont du même ordre de grandeur pour tous les transitoires de courant. De ce fait, on peut en déduire que les mécanismes de piégeage et dé-piégeage sont induits par des pièges similaires dans tous les dispositifs, TLM et HEMT, et sont renforcés par les essais de vieillissement accéléré.

L'étude des TLMs a permis de déterminer des valeurs de tension critique de dégradation et des signatures de dégradation analogues à celles relevées sur des HEMTs de géométrie proche. Par conséquent, les pièges responsables des transitoires de courant qui se produisent aussi bien dans les HEMTs que dans les TLMs sont plutôt localisés dans le canal que dans la région de la grille.

Le vieillissement accéléré sous contraintes échelonnées associé à la méthodologie mise au point pour effectuer le diagnostic in situ des dégradations du courant de drain se sont montrés efficaces pour évaluer la robustesse du HEMT GaN à grille ultra-courte.

List of publications

- **Journals**

Hadhemi Lakhdhar, Nathalie Labat, Arnaud Curutchet, Nicolas Defrance, Marie Lesecq, Jean-Claude De Jaeger, Nathalie Malbert, "Reliability assessment of ultra-short gate length AlGaIn/GaN HEMTs on Si substrate by on-state step stress", *Microelectronics Reliability*, 2016

- **International conferences**

Hadhemi Lakhdhar, Nathalie Labat, Arnaud Curutchet, Nicolas Defrance, Marie Lesecq, Jean-Claude De Jaeger, Nathalie Malbert, "Reliability assessment of ultra-short gate length AlGaIn/GaN HEMTs on Si substrate by on-state step stress", *27th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis*, Halle (Germany), 2016

- **National conferences**

Hadhemi Lakhdhar, Nathalie Labat, Arnaud Curutchet, Nicolas Defrance, Marie Lesecq, Jean-Claude De Jaeger, Nathalie Malbert, "Évaluation de la fiabilité des composants HEMTs AlGaIn / GaN à grille nanométrique sur substrat de silicium par des essais de vieillissement accéléré "on-state"", *20emes Journées Nationales Micro-Ondes*, Saint-Malo (France), 2017

- **Oral presentations**

Hadhemi Lakhdhar "Reliability assessment of GaN HEMTs on Si substrate with ultra-short gate dedicated to power applications at frequency above 40 GHz", GaNex meeting 2015 / 2016 / 2017