



**HAL**  
open science

# Fabrication and Characterization of Gate-All-Around Stacked-Nanowire/Nanosheet MOS transistors realized by a Gate-Last approach for sub-7 nm technology nodes.

Loic Gaben

► **To cite this version:**

Loic Gaben. Fabrication and Characterization of Gate-All-Around Stacked-Nanowire/Nanosheet MOS transistors realized by a Gate-Last approach for sub-7 nm technology nodes.. Micro and nanotechnologies/Microelectronics. Université Grenoble Alpes, 2017. English. NNT : 2017GREAT095 . tel-01780190

**HAL Id: tel-01780190**

**<https://theses.hal.science/tel-01780190>**

Submitted on 27 Apr 2018

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



## THÈSE

Pour obtenir le grade de

## DOCTEUR DE LA COMMUNAUTÉ UNIVERSITÉ GRENOBLE ALPES

Spécialité : NANO ELECTRONIQUE ET NANO TECHNOLOGIES

Arrêté ministériel : 25 mai 2016

Présentée par

**Loïc GABEN**

Thèse dirigée par **Francis BALESTRA** , , , et  
codirigée par **Thomas SKOTNICKI**

préparée au sein du **Laboratoire Institut de Microélectronique,  
Electromagnétisme et Photonique - Laboratoire  
d'hyperfréquences et de caractérisation**  
dans l'**École Doctorale Electronique, Electrotechnique,  
Automatique, Traitement du Signal (EEATS)**

**Fabrication et caractérisation de transistors  
MOS à base de nanofils de silicium empilés  
et à grille enrobante réalisés par approche  
Gate-Last pour les noeuds technologiques  
sub-7 nm.**

**Fabrication and Characterization of Gate-All-  
Around Stacked-Nanowire/Nanosheet MOS  
transistors realized by a Gate-Last approach  
for sub-7 nm technology nodes.**

Thèse soutenue publiquement le **19 octobre 2017**,  
devant le jury composé de :

**Monsieur Francis BALESTRA**

Directeur de Recherche, CNRS Délégation Alpes, Directeur de thèse

**Monsieur Gérard GHIBAUDO**

Directeur de Recherche, CNRS Délégation Alpes, Président

**Monsieur Emmanuel DUBOIS**

Directeur de Recherche, IEMN, Rapporteur

**Monsieur Brice GAUTIER**

Professeur, INSA Lyon, Rapporteur

## Introduction: stacked nanowire FETs for the sub-7 nm node technologies.

Metal oxide semiconductor field effect transistor (MOSFET) may be the most impressive achievement of the last century. Studied since the early 20s [Lilienfield 1925 US1745175], the work of Shockley, Bardeen, Parson and Brattain in the 40s' led to the germanium bipolar transistor in 1947 and to the first MOS transistor of I. Ross in 1955 embedding a ferroelectric dielectric gate oxide. In 1960 Kahng and Attala presented the first MOS transistor with a silicon dioxide gate oxide which was realized for the first time during an experiment in the summer of 1957 in Bell labs. The concept of integrated circuit was proposed by J. Kilby in 1958 and followed in 1967 by the complementary MOS (CMOS) of F. Wanlass. The first Intel 4004 chip made it real in 1971: the very first stage of a fierce fight for miniaturization and performance improvements.

Gordon Moore's predictions of 1965 turned into an industry roadmap sustained by exponential revenues to finally become the self-fulfilled prophecy known as Moore's law. In the last 60 years, solid-state-circuits industry has grown into one of the largest in the world and no other device seems to have drawn so much attention, research and developments. The need for boosting computational power was eventually shadowed by the necessity for energy efficient circuits both during calculations and during standby mode. This latest trend has emerged as a result of the increasing popularity of mobile devices made possible by the modern ULSI circuits that pack billions of transistors in a very small surface.

Even though the scaling rules proposed by R. Dennard et al. in 1967 had been valid for years during the "happy scaling" era, several issues were not anticipated at that time. Short channel effects, mobility degradation, variability and quantum tunneling leakage presented major challenges as device dimensions reached and ultimately broke the sub-100nm barrier in the last decades. As sub-32nm node planar technologies on bulk were facing severe loss of gate control over the channel, device engineers were forced to consider multi-gates devices such as Fully Depleted Silicon On Insulator (FDSOI), based on the full depletion of the Si channel, and 3D FinFET architectures.

However, this change of architecture has raised integration complexity. For the first time, the last node generations employing FinFETs have presented a slowdown in the decrease of the cost per transistor which has been one of the main motivations during the miniaturization era. This has likely caused the decrease in the number of competitors having advanced node technologies in mass production.

Even though, the ever-present need for ultra-low power systems for always-on-standby smart devices such as smartphones, Internet of Things (IoT), Augmented and Virtual Reality (AR / VR) has kept some of the industry fighting its way towards better and smaller transistors. Subsequently, the cost per functionality still seems to be a motivation to develop the 10 nm and 7 nm nodes although Intel has already announced a slowdown of their two-year tick-tock roadmap opting for a three-years development scheme. On their side, TSMC and Globalfoundries also have a FinFET roadmap including 16 nm, 14 nm and 10 nm technologies while Samsung recently announced a 4 nm node roadmap.

In parallel, STMicroelectronics has developed its 28 nm FDSOI technology in collaboration with CEA LETI and Grenoble Minattec research laboratories such as IMEP-LAHC. In 2016, Globalfoundries and Samsung have also started working on this technology giving promising perspectives for the development of the FDSOI ecosystem.

Today, the question of FinFET and FDSOI downscaling is still open and more than ever alternatives to CMOS transistors are being investigated such as tunnel FETs (TFETs) [Mayer 2008], [Ionescu 2011 Nature], [Avci 2015] and 2D materials [Wu 2013]. A change of logic paradigm is also researched in neuromorphic computing [Burr 2016]. However, none of these options managed to find their way to mass production yet remaining labeled as “Beyond-Moore” or “More-than-Moore” solutions. Hence, it seems the industry will rely on “More-Moore” as far as the down-scaling will remain possible.

Similarly as with the introduction of a second gate in FDSOI and FinFET, adding one or two additional gates to realize trigate,  $\Omega$ -gate or gate-all-around (GAA) nanowire (NW) transistors (NWFETs) might be the ultimate solution to keep electrostatics under control in ultra-scaled channels. Hereafter, stacking vertically these NW channels could be at the utmost of conventional CMOS scaling.

This is the question the present thesis will try to answer: are FinFET and FDSOI intended to be the last silicon based conventional CMOS architectures or nanowire and stacked nanowire FETs (SNWFETs) can help to keep the downscaling era alive, along with the ambitious perspective of further expanding CMOS in the third dimension?

*No exponential is forever: but “forever” can be delayed” G. Moore [Moore 2003].*

## Contents

Introduction: stacked nanowire FETs for the sub-7 nm node technologies.....	1
1. Need of 3D-channels in CMOS technology .....	5
1.1. Physics of multi-gate devices: scaling length volume inversion & mobility.....	6
1.1.1. CMOS scaling.....	6
1.1.2. Double gate device physics: volume inversion.....	8
1.1.3. Multi-gate device physics: carrier transport in thin films.....	10
1.1.4. Conclusion .....	11
1.2. Double-gate devices: from FDSOI and FinFET to nanowires.....	12
1.2.1. FDSOI .....	12
1.2.2. Horizontal Double-gate devices .....	13
1.2.3. Silicon-On-Nothing (SON).....	15
1.2.4. Vertical double-gate: towards FinFET .....	16
1.2.5. Conclusions.....	18
1.3. The nanowire technology: down to the end of the roadmap? .....	19
1.3.1. Tri-Gates, $\pi$ -gate, $\Omega$ -gate and gate-all-around (GAA) nanowire FETs .....	19
1.3.2. Technology boosters: channel orientation and strain in trigate nanowire FETs.....	21
1.3.3. Technology boosters: the case of Sidewall Image Transfer (SIT) .....	26
1.3.4. Stacked NWS.....	29
1.3.5. Conclusion and thesis proposal.....	33
2. Benchmarking Stacked Nanowires Technologies with FinFET .....	35
2.1. TCAD Model: Simulation Parameters and Extraction .....	35
2.1.1. TCAD model.....	36
2.1.2. Intrinsic delay approximation.....	39
2.1.3. Parasitic capacitances – inverter equivalent capacitance.....	40
2.2. Electrostatics of 3D-architectures .....	42
2.2.1. Subthreshold behavior .....	42
2.2.2. Parasitic capacitances.....	46
2.2.3. Conclusion .....	47
2.3. Constant footprint and height comparison using TCAD simulation.....	48
2.3.1. Comparison guidelines .....	48
2.3.2. Results and discussion.....	49
2.3.3. Towards stacked nanosheets? .....	52
2.4. Internal spacer and gate alignment is key to reduce parasitic capacitances.....	53
2.5. Discussions .....	55
2.6. Conclusion .....	56

3.	Stacked nanowire FETs: integration challenges and process optimization.	57
3.1.	Gate last integration flows of stacked nanowires	57
3.1.1.	NW Last: polysilicon sacrificial gate	58
3.1.2.	NW First: HSQ sacrificial gate	62
3.1.3.	Alternatives?	64
3.1.4.	Conclusion	66
3.2.	Si/SiGe superlattice	67
3.3.	Si/SiGe fins patterning	72
3.4.	SiGe selective removal	74
3.5.	Source and drains (S/D) and internal spacers fabrication	81
3.5.1.	Surface preparation	81
3.5.2.	Selective epitaxial growth (SEG)	83
3.5.3.	S/D in a NW last approach with aligned internal spacers.	83
3.5.4.	S/D in a NW first approach with self-aligned internal spacers	85
3.6.	Electron beam lithography of HSQ	88
3.6.1.	Conditions	88
3.6.2.	Layouts description	88
3.6.3.	Resist developing	91
3.6.4.	Observations	93
3.6.5.	Limitation and perspectives	95
3.7.	Chemical mechanical planarization (CMP)	96
3.7.1.	Introduction to CMP	96
3.7.2.	Polysilicon sacrificial gate CMP (NW Last approach)	97
3.7.3.	Sacrificial gate opening CMP	101
3.7.4.	Metal CMP (NW Last & NW First)	105
3.8.	Conclusion	108
4.	Achieved integrations and optimization perspectives	110
4.1.	Electrical characterization of SNWFETs fabricated in a NW last approach	110
4.1.1.	Device fabrication	110
4.1.2.	Electrical measurements	113
4.2.	3D SAC and STI: HSQ the ultimate resist?	116
4.2.1.	SNWFETs fabricated in a NW first approach	116
4.2.2.	Alternative approach with HSQ sacrificial gates and lateral insulation	121
	General Conclusion	126

# 1. Need of 3D-channels in CMOS technology

The purpose of this chapter is to assess the cumulated benefits of nanowire-based architectures through the evolution of their elders. Their apparition and current methods of fabrication are introduced through a detailed explanation of the historical context. Through the years, many different devices, processes and integrations were investigated. Observing how and when these development efforts helped in the adoption of new technologies is expected to provide some perspectives and a better comprehension of the choices made today.

In the following first subchapter, scaling needs are seen as the main drivers for technology and device physics research (§1.1). nanowire and stacked-nanowire FETs history and fabrication methods are intimately linked to double-gate (DG) and multi-gate (MG), fully-depleted transistors on silicon-on-insulator (FDSOI) and silicon-on-nothing (SON) technologies. Figure 1.1 therefore maps several of these architectures picturing the stacked nanowires FETs (SNWFETs) as a potential outcome of CMOS downscaling.

With the ambition of introducing SNWFETs as a new alternative, the second sub-chapter intends to provide some insights on how both major substitutes to bulk that are FDSOI and FinFET managed to find their way to mass production and how the other technologies helped or will help new ones to emerge (§1.2).

The status of the next 7 nm and 5 nm technologies nodes remain uncertain: even if FinFETs have good chances to be part of 7 nm [WuSY 2016 IEDM], [XieR 2016 IEDM], there is still some room and time for a new architecture to be inserted. With this standpoint, the third and last sub-chapter sets the nanowire-based technology as a good candidate for substituting to FinFET (§1.3).

This initial revision concludes on SNWFET development perspectives along with the thesis objectives.

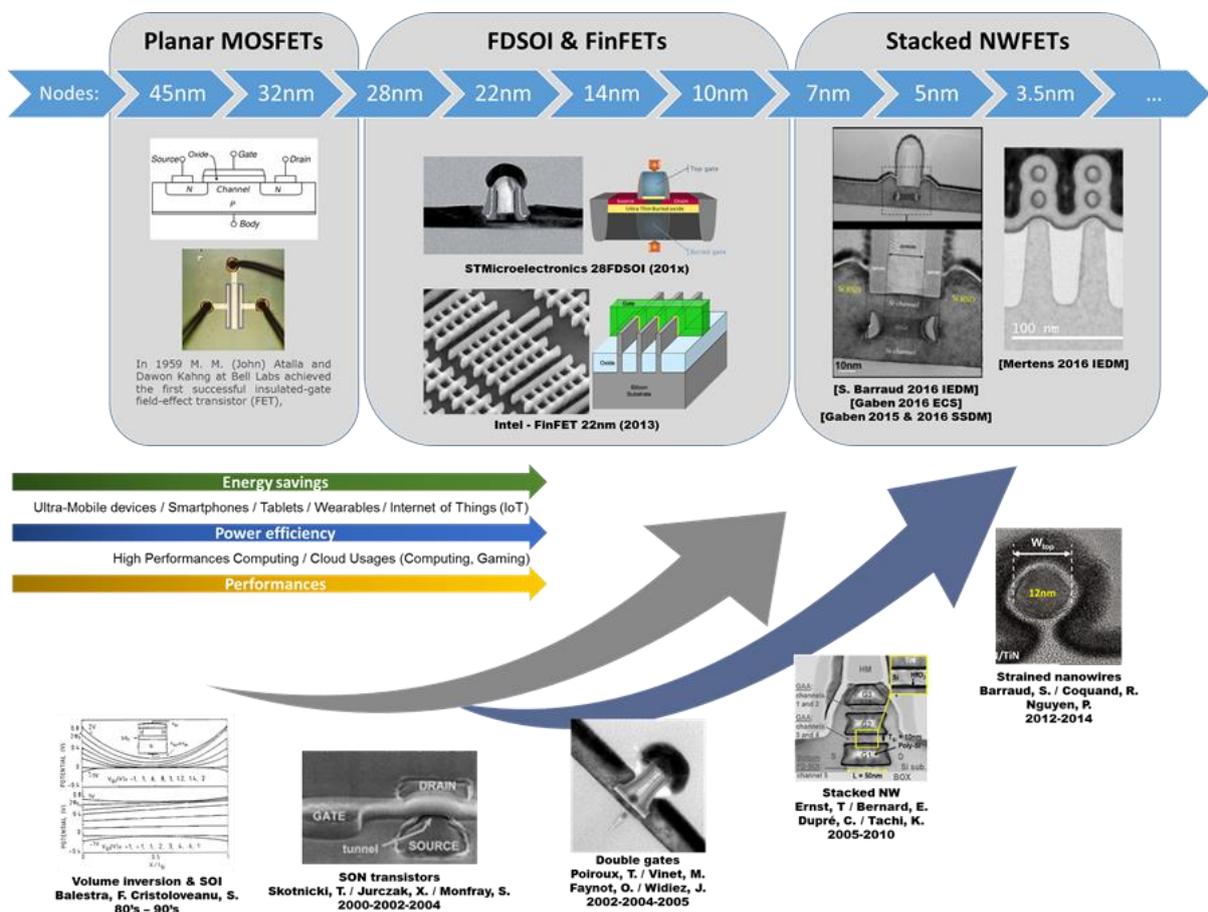


Figure 1.1 Expected timeline for the emergence of new technologies: from bulk to FinFET, FDSOI and stacked NW.

## 1.1. Physics of multi-gate devices: scaling length volume inversion & mobility.

In this section, the physics and historical apparition of multi-gate architectures are explained in order to understand the reasons why the addition of one or several gates had been the most promising concept for an ultimate scaling of transistors. The first section concerns electrostatics and scaling lengths (§1.1.1). The second section discusses the advantages of DG devices through the finding of volume inversion (§1.1.2). In the last section, the preempted enhancements in carrier mobility due to the additional gates are finally introduced (§1.1.3).

### 1.1.1. CMOS scaling.

The understanding of the underlying physical phenomena taking place during downscaling has never stopped to grow. Dennard et al. [Dennard 1974] introduced scaling rules for MOSFET suggesting that if devices dimensions and applied potentials are scaled down by a common factor  $1/k < 1$  while impurity concentration is increased by  $k$ , the shape of the electric field should remain constant. This was believed to provide a steady increase of performance with constant power consumption. However, short channel effects (SCE) and mobility degradation with the increase of channel doping were not addressed yet. In 1980, Brews et al. [Brews 1980] improved this scaling law to offer more flexibility in the geometry and to set some room for new architectures. In 1984, Dennard and his team added the impact of finite inversion layer, mobility degradation effects, drift velocity saturation and source and drain (SD) contact resistances [Baccarani 1984]. For sub-micrometer technologies, the previous scaling rules led to excessively high doping requirements causing mobility degradation and increased junction capacitances. By introducing a natural length, [Yan 1992] defined a new and unique criterion for the scaling of both SOI and bulk devices. A year later, [Suzuki 1993] defined another natural length to unify this value for different gate lengths across different architectures including undoped channels and SOI transistors with back-gate control. It was concluded that the SOI thickness needs to be decreased along with the gate length and the gate oxide to preserve the performances. A dependence in permittivity was added in [Frank 1998] to take into account the apparition of high- $k$  gate insulators. As gate-all-around (GAA) devices were attracting the attention, [Auth 1997] adapted the scaling length found in [Suzuki 93] for vertical surrounding gate (SGT). In 2009 and 2010, Bangsaruntip et al, showed the universality of SCE in GAA-FETs, FinFET and FDSOI [Bangsaruntip 2009 IEDM], [Bangsaruntip 2010 EDL]. Interestingly, this last scaling length can also be used to extract the effective channel length.

The voltage doping transformation (VDT) suggested that the potential barrier height is physically equivalent to and can be replaced by a reduction in channel doping concentration derived from the Poisson equation in a simple function of channel length, source to drain bias and source to bulk bias [Skotnicki 1988]. The VDT model was later introduced in the Model for Analog and digital Simulation of mos TrAnsistoRs (MASTAR) in 1994 [Skotnicki 1994] and used to compute the impact of scaling since the International Technology Roadmap for Semiconductors of 2005 (ITRS).

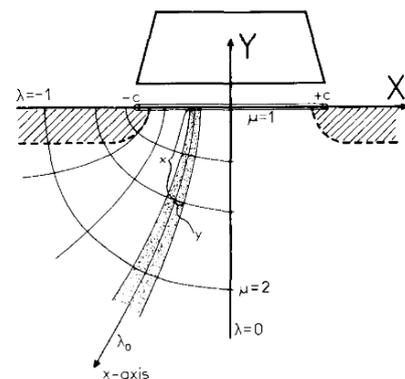


Figure 1.2 - Electric field illustration in a bulk device annotated for VDT transformation model as in [Skotnicki 1988].

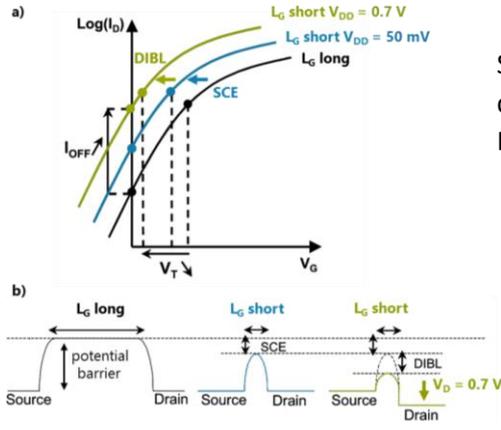


Figure 1.3 – DIBL and SCE displayed on (a) a transistor I-V characteristic and (b) on a band diagram.

SCE and drain induced barrier lowering (DIBL) can be computed in various devices geometry by introducing the Electrostatic Integrity factor (EI):

$$SCE \sim 0.64 \frac{\epsilon_{Si}}{\epsilon_{ox}} \cdot EI \cdot V_{bi} \quad (Eq. 1-1)$$

$$DIBL \sim 0.80 \frac{\epsilon_{Si}}{\epsilon_{ox}} \cdot EI \cdot V_{DS} \quad (Eq. 1-2)$$

with  $V_{bi}$  the source to drain built-in potential and  $V_{DS}$  the source to drain potential.

This gives the threshold voltage roll-off in between a long channel device ( $V_{th\infty}$ ) and its short channel counterpart ( $V_{th}$ ):

$$V_{th} = V_{th\infty} - SCE - DIBL \quad (Eq. 1-3)$$

In turn, the EI factor depends on the architecture so that its characteristic equation for either a bulk, FDSOI or double gate architecture is given in equations (1-4) to (1-6). The electric field lines propagation can hereby be controlled by adding a buried oxide layer under the channel or one or several gates impacting the EI factor:

$$EI_{bulk} = \left( 1 + \frac{x_j^2}{L_{el}^2} \right) \cdot \frac{t_{ox}}{L_{el}} \cdot \frac{t_{dep}}{L_{el}} \quad (Eq. 1-4)$$

$$EI_{FDSOI} = \left( 1 + \frac{t_{Si}^2}{L_{el}^2} \right) \cdot \frac{t_{ox}}{L_{el}} \cdot \frac{t_{Si} + \lambda t_{BOX}}{L_{el}} \quad (Eq. 1-5)$$

$$EI_{double\ gate} = \frac{1}{2} \left( 1 + \frac{t_{Si}^2}{L_{el}^2} \right) \cdot \frac{t_{ox}}{L_{el}} \cdot \frac{t_{Si}}{L_{el}} \quad (Eq. 1-6)$$

If EI can be reduced in a bulk device by shrinking the junction depth  $x_j$  and the depletion depth  $t_{dep}$ , one need to downsize the silicon film  $t_{Si}$  and BOX  $t_{BOX}$  thicknesses in a fully depleted SOI device. The double gate (DG) MOSFET brings another significant improvement in DIBL as displayed in Figure 1.4 and according to (Eq. 1-6), channel thickness must be reduced to limit SCE and DIBL. In a sense, this graph was a prelude to the introduction of FDSOI and double gate devices constrained by the difficulty or the impossibility to scale down usual bulk devices under the 32-nm node technology without suffering of severe degradations in subthreshold behavior.

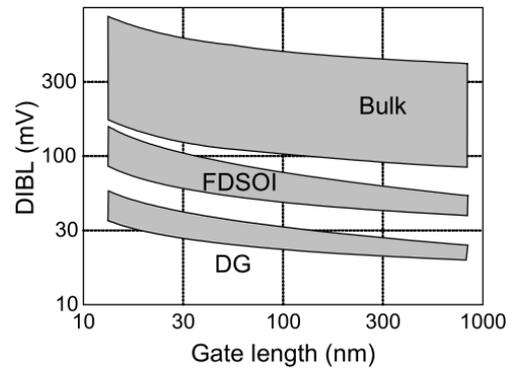


Figure 1.4 - Impact of the architecture on DIBL as predicted by MASTAR [Colinge 2008].

Although electrostatic integrity of the device is of big concern, carrier transport must be at least preserved or improved after each generation of transistor. In the following, the discovery of volume inversion is revised and used as a base to analyze electron and hole mobility in multi gate devices.

### 1.1.2. Double gate device physics: volume inversion.

Interest for transistors on SOI was growing in the 80s and several groups started to use the silicon back side to control the electric field in the channel. By using the buried oxide (BOX) as a gate oxide and the silicon substrate as a back gate, the silicon channel surface in contact with the BOX could be designed as a back channel to achieve accumulation, depletion and inversion at this interface. Front and back gates coupling were studied in [Lim 1983] evidencing a front and back channel conduction and a threshold voltage  $V_T$  affected by the biasing of the two gates. This effect turned out to be a great advantage of FDSOI transistors (§1.2.1), [Fenouillet-Beranger 2009], [Planes 2012].

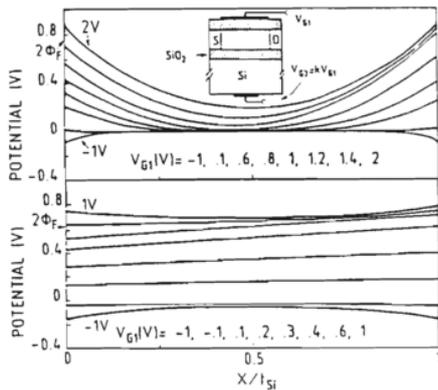


Figure 1.5 - Potential profiles inside the 300 nm silicon film [Balestra 1987]

Playing with low doped SOI MOSFETs and biasing voltages, Balestra, Cristoloveanu et al, first introduced the concept of volume inversion (VI-MOSFET) [Balestra 1987] (Figure 1.5). The VI concept induces the best electrostatic control of the channel by the gates and allow 2G, 3G and 4G MOSFETs to be scaled down in the sub-10nm gate length range. While in bulk silicon MOSFETs the minority carriers are confined in a very narrow triangular potential well at the gate oxide and channel interface, instead, the potential becomes parabolic and sometimes flat in SOI MOSFETs, allowing the minority carriers to spread into the film volume [Cristoloveanu 1990]. Promises were a current flow at least doubled compared to single gate (SG) MOSFETs. A mobility enhancement is expected due to

a reduced influence of the interfacial defects on the minority carriers that are no longer confined in the vicinity of the oxide interface [Balestra 1987], [Colinge 1990]. Tanaka et al in 1991 proposed a model to fit their 60 nm thin un-doped channels [Tanaka 1991]. Since on a range of high gate voltages the potential does not change at the center of the silicon channel, and while it is bent at the insulator-channel interface, they divided the drain current in two parts: one part is constant at the center and dominant in between the subthreshold and saturation regimes and the second is a surface current which varies with the gate voltage as soon as the difference of potential between the interface and the center causes the band to bend.

[Venkatesan 1992] confirmed the existence of volume inversion measuring a slight transconductance boost – below 10% – around threshold in 100 nm double gate structure ( $T_{ox} = 20$  nm). However, their simulation claimed that the enhancement is strictly restricted to the near threshold operation. By comparing the drain currents at constant  $V_G - V_T$  in DG and SG transistors on SOI, they could not find more than twice the current in the DG, which is also the gain in effective width compared to a SG. According to the authors, this proves that surface inversion layers shield bulk inversion charges under high gate biases and therefore that carrier density does no longer increase with gate voltage. They also found the electron concentration in the center of the film to be the third of the one in both surface channels at high voltage.

Baie and Colinge studied the behavior of inversion layers in 40 nm thin DG channels as a function of gate voltage and related it to energy band diagrams [Baie 1998]. For low voltages, only one permitted energy level is being populated (Figure 1.6.A.a) and most of the free electrons are located at the center of the silicon film illustrating the concept of VI (Figure 1.6.B.a). As the transverse electric field is increased, a second permitted level is being populated (Figure 1.6.A.b). Finally, the two first levels tends to pair up with  $V_G > V_T$  as they become degenerated into a single energy level (Figure 1.6.A.c). One wave function is symmetric while the second is antisymmetric leading to the formation of two inversion channels next to the Si/SiO<sub>2</sub> interfaces (Figure 1.6.B.b and B.c). Figure 1.6.C reports the considerations of Figure 1.6.B on a single electron concentration scale.

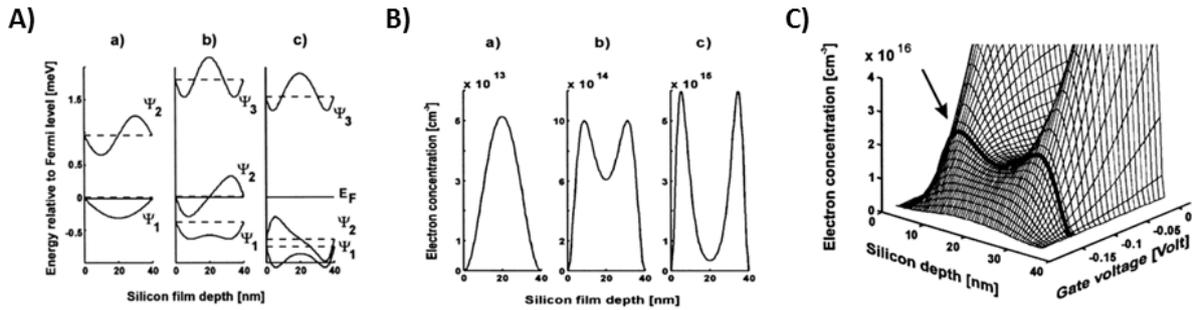


Figure 1.6 – (A) Evolution of the first wave functions and their respective energy levels and (B) electron concentration as a function of gate voltage: (a) low voltage, (b) moderate inversion (c) above  $V_r$ . (C) Electron concentration as a function of silicon thickness and gate voltage as published in [Baie 1998]

Considering that in such device, the impact of VI seems to be relatively limited to low gate voltage, one can think that the claimed benefits of VI are limited to low and moderate inversion. However, Gamiz and Fischetti completed the understanding of VI layers by studying the impact of channel thickness [Gamiz 2001]. If the film thickness is higher than the sum of the two depletion layers, the device operation is similar to two conventional MOSFETs in parallel (as in the case of [Baie 1998]). However, if the silicon slab is thin enough, VI can be maintained over a large range of effective electric fields (Figure 1.7.A and B). Similarly to SG SOI devices and consistently with [Baie 1998], Figure 1.7C shows the population of non-primed sub-bands with lower conduction effective masses ( $m_{c,primed} > m_{c,non-primed}$ ) is increased as silicon thickness is reduced. As a result, the global effective mass is reduced and the electron mobility is therefore increased.

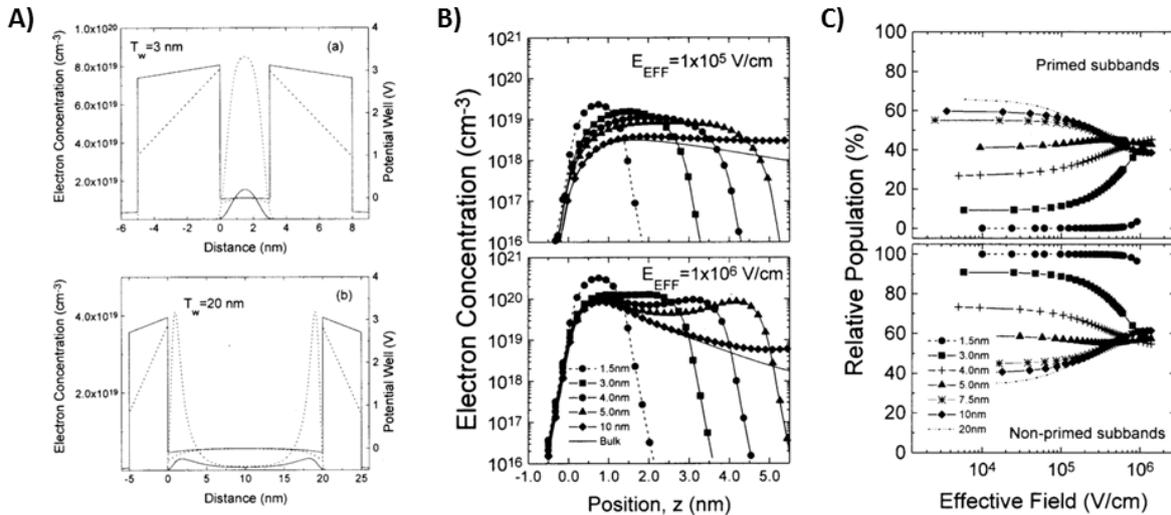


Figure 1.7 – (A) Potential well and electron distribution in a DGSOI for  $N_{inv} = 1.3 \times 10^{12} \text{ cm}^{-2}$  (solid line) and  $N_{inv} = 8.5 \times 10^{12} \text{ cm}^{-2}$  (dashed). (B) Electron distribution for different thicknesses and electric effective field. (C) Sub-band relative population [Gamiz 2001].

Consequently, the thinnest channels should be advantaged in terms of electron distribution. However, in such highly confined structures, a significant part of the electron distribution extends into the oxide. This raises the question of carrier scattering intensity in such devices including surface roughness and Coulomb scattering due to trapped charges into the oxide. This may balance the advantages of VI as initially expected.

### 1.1.3. Multi-gate device physics: carrier transport in thin films.

#### Electron-phonon scattering

Gamiz and Fischetti used the form factor defined in [Price 1981] which links phonon scattering rates with the transversal envelope of the electron wave function. A greater confinement enhances the overlapping of the electron wave function so as the scattering rate. Figure 1.8 compares DG and SG on SOI devices as a function of effective transverse field and silicon thickness. For thick channels, the two inversion layers behave almost independently as seen in §1.1.2, so that the form factor and the phonon limited mobility is near the one in SG on SOI. For thinner channels, VI occurs and the dispersion of electron throughout the whole channel reveals its advantage in terms of phonon scattering. However, as confinement is increased this advantage is quickly lost and no longer depends on the electric field but only on geometric considerations. A peak clearly appears in the 3 nm to 4 nm region (Figure 1.8b) and can be explained by the behavior of conduction effective mass. In this region, the reduction of conduction effective mass dominates over the increase of phonon scattering rate. As the silicon thickness is reduced, the reverse happens and therefore the mobility drops.

#### Surface roughness scattering

Surface roughness scattering comes from a perturbation of the potential well perpendicularly to the interface caused by a variation of that interface from an ideal plane. In Figure 1.9 the peak in the 3 to 4 nm range is now wiped out as surface scattering limits the mobility in such thin channels. Only remains an improved mobility in the range 3 to 15 nm – modulated by effective electric field intensity – due to VI which keeps a significant amount of electrons apart from the interfaces (Figure 1.9).

#### Coulomb scattering

Coulomb scattering is due to charges trapped at the Si-SiO<sub>2</sub> interfaces affecting the low inversion mobility (at the High-k-metal interface as well in modern technologies). As the effective field is increased, electrons become to screen these charges and this effect no longer limits electron mobility. Figure 1.10 reveals that the screening effect is more effective for thinner channels as the mobility increases faster for these confirming one more time the role of VI. Figure 1.10 emphasizes even more the advantage of DG and VI with low transverse field mobility plot – low enough to prevent any screening effect.

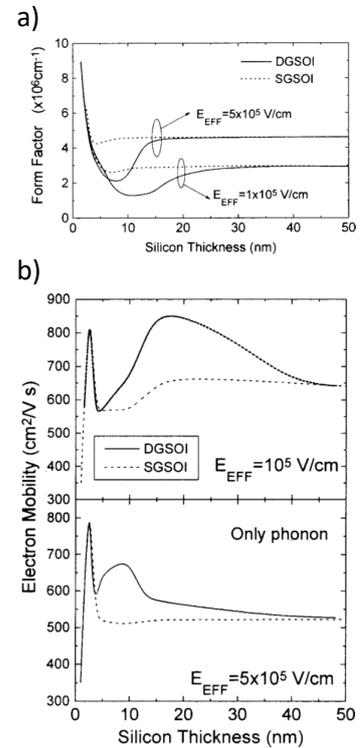


Figure 1.8 – (a) Form factor evolution for the ground sub-band and (b) Phonon-limited mobility as a function of silicon thickness.

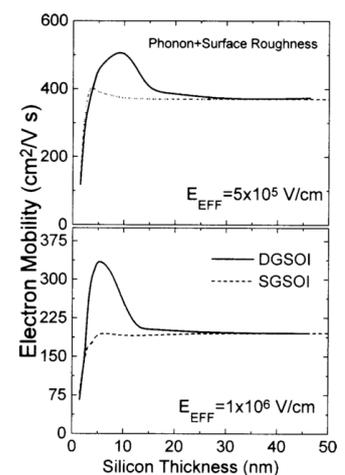


Figure 1.9 - Electron mobility as a function of silicon thickness: influence of phonon and surface roughness only [Gamiz 2001].

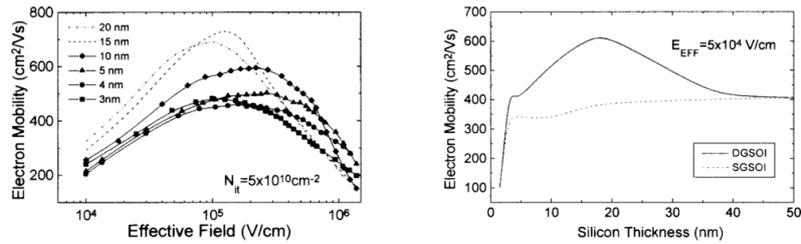


Figure 1.10 - Electron mobility curves in a DGSOI with phonon, surface roughness and Coulomb scattering included: (a) as a function of transverse effective field and (b) as a function of silicon thickness [Gamiz 2001].

DG are one-dimensional confined structures but carrier transport in trigate and  $\Omega$ -gate constrained by a two-dimensional confinement can be studied similarly. For example, in [Niquet 2012 ULIS], [Niquet 2012 Nano Lett.] and [Niquet 2012 TED], Non-Equilibrium Green's Functions (NEGF) band structure calculations are realized for various silicon nanowires with different size and crystallographic orientations for the channel. This will be more discussed in trigate NWFETs in the last sub-chapter §1.3.2.

#### 1.1.4. Conclusion

Finally, this sub-chapter presented the multi-gates architectures as the only option to keep scaling down silicon CMOS devices while preserving electrostatic integrity (§1.1.1). In thin double-gate devices, electrons extend throughout the entire channel under threshold and near threshold. Yet if the channel is thin enough, this volume inversion can be maintained over a wide range of effective electric fields hoping for an enhanced carrier mobility (§1.1.2). However, with such confined structures, the impact on mobility can be significant and may limit the advantages of VI (§1.1.3). Even though, this comprehension had been a motivation for fabricating ultrathin channels and ultimately the nanowires devices described in the two next sub-chapters.

## 1.2. Double-gate devices: from FDSOI and FinFET to nanowires

In an attempt to study and to eventually benefit from the precited advantages of adding extra gates around the channel, double-gate (DG) devices have been realized from many ways. Recent FDSOI technologies with back-biasing abilities consist in a first family of asymmetric DG presented in the first section (§1.2.1). The symmetric DG kind is then analyzed: starting with horizontal DG devices obtained from wafer bonding (§1.2.2) or from Silicon-On-Nothing (SON) fabrication processes (§1.2.3). Finally, a last family of vertical symmetric DG well known as FinFETs is presented in §1.2.4.

### 1.2.1. FDSOI

Fabrication of CMOS transistors on wafers including a buried oxide (BOX) was studied since the 60s. SOI MOSFET was first recognized for its improved resistance to radiation [Davis 1985]. By the end of the 80's several publications have shown their advantages over bulk CMOS in terms of short channel threshold voltage scalability [Colinge 1987], subthreshold slope [Colinge 1986], hot electron immunity [Colinge 1986] and drive current [Sturm 1988]. However, and as summarized in [Colinge 1989], these advantages could not be implemented until the extra wafer cost became lower than the added processing cost for improving bulk. If the first SOI wafers were silicon on sapphire (SOS), they were rapidly replaced by more traditional and cheaper silicon wafers with the apparition of techniques such as Separation by IMplantation of OXYgen (SIMOX) [Smith 1956], [Watanabe 1966], [Izumi 1978], [Bruehl 1985] and Bond and Etch back SOI (BESOI). A significant achievement towards the democratization of SOI, was the publication of the Smart-cut process to produce Unibond wafers [Bruehl 1995]. FDSOI first appearance on ITRS roadmap was in 2001, about 25 years after the first fully depleted MOSFET named the "deep depleted" with undoped SOS films [Balestra 1985 SSE] and the first demonstration of an ideal subthreshold slope (SS) of 60mV/dec by numerical simulation [Balestra 1985 PhD thesis], [Balestra 2015 Wiley].

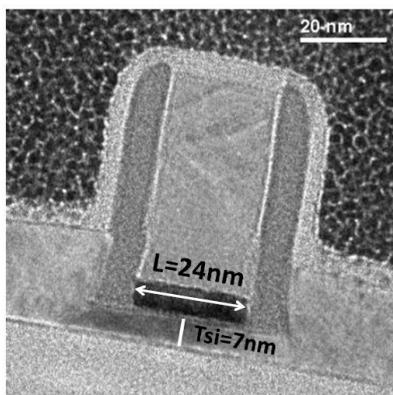


Figure 1.11 - Cross sectional TEM image of 28 nm FDSOI with  $L_G = 25 \text{ nm}$  and  $T_{Si} = 7 \text{ nm}$  [Planes 2012].

The first STMicroelectronics full platform using FDSOI was presented in 2012 [Planes 2012]. This 28 nm FDSOI technology is fully compatible with Adaptive Voltage Scaling (AVS) and Adaptive Body-Bias (ABB) advantaged by the use of the back gate [LiuQ 2011], [Weber 2010]. Multi- $V_T$  approach is realized through Ultra-Thin (UTBOX) and appropriate ground plane (GP) as explained in [Fenouillet 2009], [Noël 2011 TED], [Grenouillet 2012 IEDM]. Un-doped channels improve stochastic mismatch so that random  $V_T$  variations are mostly coming from dipoles in the high-k and local TiN metal gate workfunction variations [Weber 2008]. Weber and al. showed a negligible impact of local variations of  $T_{Si}$  and that its scaling compensates  $L_G$  variations contributing to a better matching. The process being simpler than bulk FinFET, this compensates for extra cost due to SOI substrates. FDSOI is qualified of "low-cost" process by STMicroelectronics and Globalfoundries compared to FinFET.

FDSOI scaling would require thinner  $T_{Si}$  to overcome SCE increase with  $L_G$  reduction for 14 nm and 10 nm nodes. However, quantum confinement effects will dominate  $V_T$  as  $T_{Si}$  reaches 3 nm. FDSOI technology scaling then consists in scaling the BOX and integrating boosters such as SiGe channels formed by Ge condensation [Cheng 2012], raised source and drain (RSD), strained SOI [Andrieu 2010], [Fenouillet-Beranger 2012 VLSI], [LiuQ 2013 IEDM]. In 2014, a 0.55x area scaling and 30% speed boost

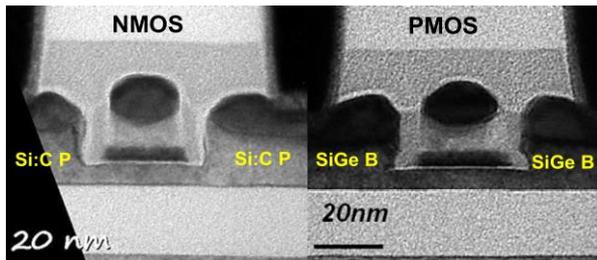


Figure 1.12 – 14 nm FDSOI transistors featuring strained channels thanks to Si:C and SiGe:B in situ doped RSD [Weber 2014].

was obtained to improve 28FDSOI [Weber 2014]. The introduction of SiCBN low-k spacer allowed STMicroelectronics, LETI and IBM to present an upgraded FDSOI with effective width normalized currents highly competitive with FinFETs [Weber 2015 VLSI]. The efficiency of the back-side biasing technique is no longer to demonstrate, [Arnaud 2012] presented for example -30% CPU power consumption at constant frequency with +80% switching

efficiency when carefully choosing the forward body bias. [LiuQ 2014 IEDM] proposed a dual strained channel integration by using tensile sSOI substrates for NFETs and 35% Ge enriched areas to reverse the strain into a compressively SGOI PFETs. The mobility improvement and the proposed scaling was claimed to make this integration suitable for a 10 nm node technology.

During the year 2016, few research groups have been predicting a scaling down to the 7 and 5 nm node technologies [VLSI 2016 panel sessions]. In 2016, FDSOI ecosystem has seen GlobalFoundries and Samsung joining the effort. AMD announced a partnership with GlobalFoundries on their 12FDX technology for 2019 which is planned to succeed to their previous 22FDX.

### 1.2.2. Horizontal Double-gate devices

Scaling requirements for high electrostatic control and later the interest in volume inversion devices had likely set up the research efforts toward highly confined structures such as double gate devices. In 1984, Sekigawa and Hayashi presented one of the first concept of DG structure suitable for 3D integrated circuits (IC). The so-called XMOS transistor was supposed to benefit from reduced channel thickness and lower doping since the channel length is decreased as required by the industry roadmap [Sekigawa 1984]. In the 80's, most of the first planar DG transistors were realized on a single SOI wafer using the BOX as a back-gate oxide. This is the reason why DG transistors were also referring at this time to SG transistors on SOI with a back-gate control over the channel.

Unfortunately, the BOX thickness was a parameter hardly scalable: even if it was possible to balance the front and back biasing voltages to compensate a thicker back-gate oxide [Balestra 1987], it seemed impossible to comply with extremely thin oxide layers within the nanometric range required for the most advanced nodes gate stacks [ITRS 2001]. Consequently, new techniques using wafer bonding were developed in order to form separately the front and back gates [Tanaka 1991]. One of the best performances of the year 1994 on 0.19  $\mu\text{m}$  gate lengths was obtained with these devices due to low  $V_T$  and steep subthreshold slope (SS) at low voltages [Tanaka 1994].

Whereas traditional bulk or FDSOI MOSFETs featured a self-aligned gate and junctions, front and back gates alignment issue arose in the specific case of DG; especially when realized after wafer bonding. This was discussed in [Wong 1994], [Allibert 2001] and [Yin 2003] where the use of an oversized back gate was recommended to reduce the constraints on the alignment despite of an increased device delay. [Lolivier 2004], [Widiez 2004], [Widiez 2005] and [Vinet 2005] presented promising results for these devices realized with a bonding process in comparison with bulk and single gate devices with back biasing (Figure 1.13). Many alternatives to wafer bonding were suggested using selective epitaxial growth (SEG) and epitaxial lateral overgrowth (ELO) [Denton 1996]. To solve the misalignment issue, [Wong 1997] proposed a self-aligned DG using a sacrificial amorphous silicon channel. An aperture is realized into the BOX in order to use the bulk Si underneath as a seed for SEG/ELO to build the drain,

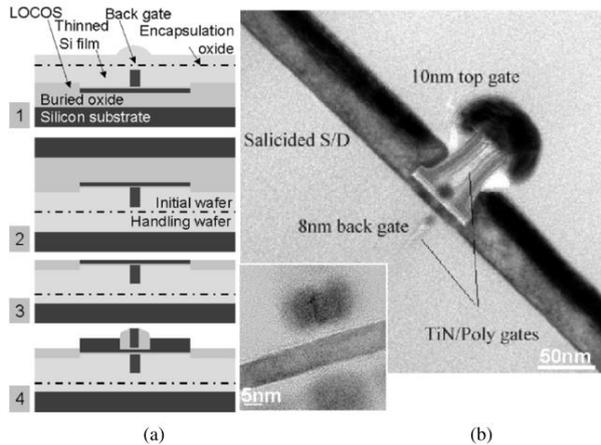


Figure 1.13 - (a) Process description: 1) top gate patterning and oxide encapsulation, 2) bonding, 3) initial substrate and BOX removal and 4) back gate patterning. (b) TEM cross section of a 10 nm gate length device with 10 nm channel thickness, raised nickel silicided source and drain and poly-TiN gate [Vinet 2005].

However, this technique requires a specific SOI substrate made of Si/SiN/SiO<sub>2</sub> BOX/bulk instead of SOI. [LiuH 2002] presented a derivative using lateral phase solid epitaxy (LSPE). [Zhang 2004] also derived this concept of multilayers with sacrificial gate to propose a monolithic integration of stacked DG to realize an inverter.

#### PlaneFET

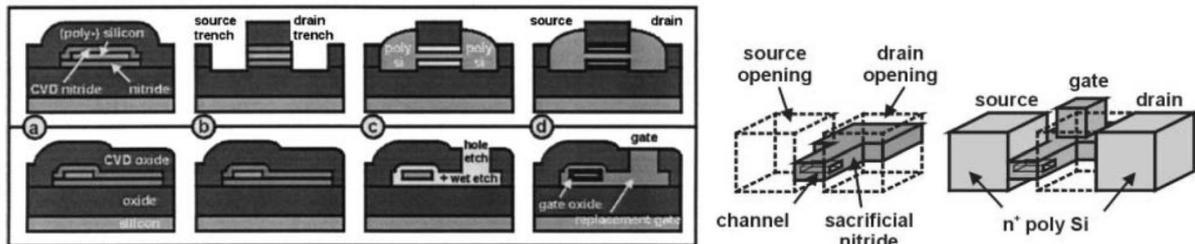


Figure 1.14 – Plane FET concept as proposed in [Schulz 2002].

It was claimed that these devices were good candidates for low power applications thanks to a lower  $V_T$  and a better SS so the results had sustained many developments. Frank et al. predicted a scalability of double-gate MOSFETs down to 30 nm gate length at least but warned about the need of a precise control of the channel thickness (5 nm in the simulation), dual gate alignment, abrupt doping profiles, and gate work function control so as a new heat extraction technique [Frank 1992].

Finally, DG transistors on SOI at that time had to compose either with misalignment due to wafer bonding or with complex integrations [Poiroux 2006], [Poiroux 2009]. Although improved integrations with aligned DG were later proposed [Vinet 2009], the introduction of Silicon-On-Nothing (SON) concept in the beginning of the 00's was a prelude to the fabrication of self-aligned features.

### 1.2.3. Silicon-On-Nothing (SON)

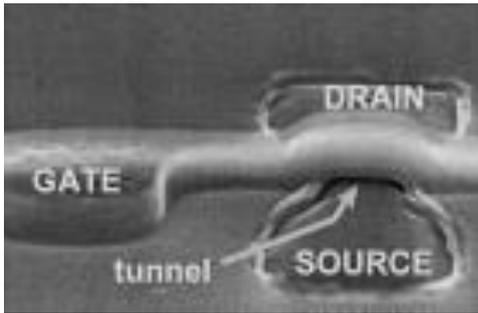


Figure 1.15 - SEM image of a SON suspended channel after SiGe selective removal [Jurczak 2000].

Silicon-On-Nothing (SON) evolved from the SilicON Cut-off junction (SONCTION) [Skotnicki 1999] to become an alternative to FDSOI. The process, as first described in [Jurczak 1999] and [Jurczak 2000], features a selective epitaxy of SiGe on STI patterned active area followed by a non-selective epitaxy of silicon. SiGe allows the crystalline continuity of the lattice for the epitaxy of the silicon channel and also acts as a sacrificial layer. Once the SiGe is selectively removed, the silicon membrane remains suspended being attached to the gate which is itself attached on both ends to the STI oxide. The cavity is then filled with an oxide and the S/D regions are formed (Figure 1.15). The same advantages

as with FDSOI are found in this device, and besides, this local SOI no longer requires expensive SOI substrates. A co-integration with bulk devices is also permitted [Huguenin 2010 VLSI]. Additionally, insulation and channel thicknesses are defined by epitaxy which allows to perform extremely thin BOX and channel down to 20 nm and 5 nm with a good controllability as reported in [Jurczak 2000]. This turned out to be an advantage when decreasing the BOX and SOI thicknesses remained a significant challenge on commercial SOI substrates [Fenuillet-Beranger 2003]. Self-heating was also believed to be less important than for FDSOI since only the channel area is insulated from the substrate [Jurczak 2000]. The technology was further developed in [Monfray 2001] which presented for the first time 80 nm gate length transistors with promising projections for advanced nodes, with 9 nm thick channel [Monfray 2002 SOI] and fully operational SRAM [Monfray 2004]. A review of this architecture was realized in [Skotnicki 2006].

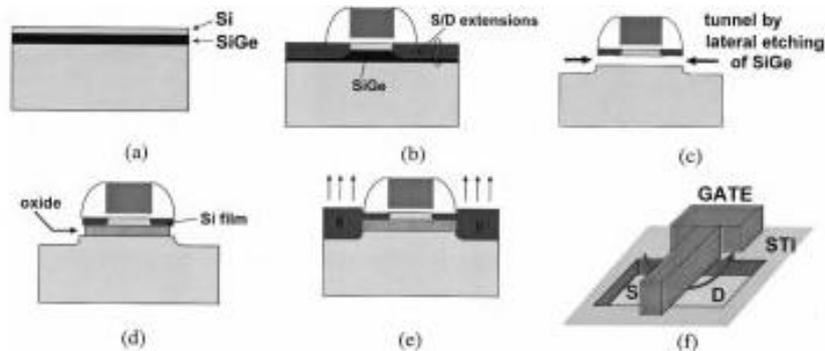


Figure 1.16 - SON transistor fabrication steps up to the sacrificial SiGe removing as presented in [Monfray 2002].

The derivation of the SON process to realize DG FETs is interesting in the framework of this thesis: the bottom local insulation was replaced by gate material in both [Monfray 2002 VLSI] and [Harrison 2003] reporting the first variants with top  $L_G$  and  $T_{Si}$  down to 40 nm and 15 nm respectively. Yet the bottom gate remains defined by the shallow trench isolation (STI) and therefore are in the micrometric range (Figure 1.17a). It was later improved using a near-damascene process named “Poly Replacement Through Contact Hole (PRETCH)” in order to introduce a high-k and a metal gate stack (Figure 1.17a), [Harrison 2004], [Coronel 2004], [Cerutti 2005]. This process naturally led to self-aligned DG and, because SiGe/Si epitaxies can be repeated several times to produce a super-lattice alternating multiple channels and sacrificial layers, to multi-channel devices (Figure 1.17c), [Shenoy 2004], [Hartmann 2005]. Stacked channel devices will be discussed in the next sub chapter (§1.3.4). Nevertheless, the first attempts were reported in [KimSM 2004], [LeeSY 2004], [Yoon 2004] and [Ernst 2006]

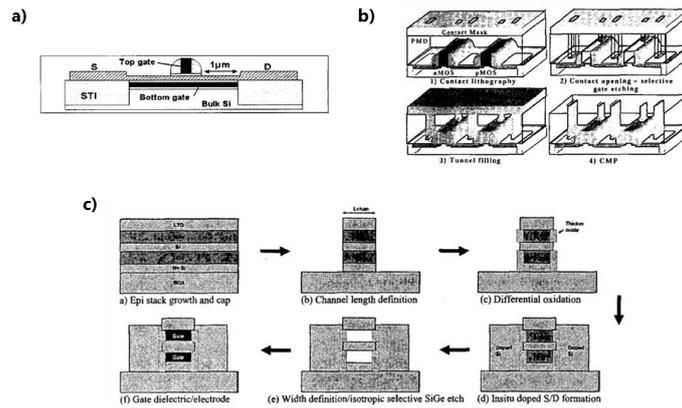


Figure 1.17 - (a) SON process where the local insulation is replaced by gate material to realize a back gate [Monfray 2002 VLSI]. (b) PRETCH concept as proposed in [Harison 2004]. (c) Stacked DG FETs fabrication as presented in [Shenoy 2004]

### 1.2.4. Vertical double-gate: towards FinFET

Along with the development of horizontal planar DG, vertical channels – with still horizontal conduction – were researched. One advantage over planar DG is to propose an increased channel width with limited wafer area occupation. Although tridimensional devices increased the process flow complexity, the FinFET architecture met mass production requirements in 2010 [Yeh 2010 IEDM].

A novel structure named fully depleted lean channel transistor (known as DELTA) was proposed to take advantage of volume inversion [Hisamoto 1989] [Hisamoto 1991]. In this assembly, a vertical silicon fin is realized and SIMOX isolation is replaced by selective oxidation of the silicon substrate. However, this was accused to generate too much defects at the edges of the field oxides ( $W = 200 \text{ nm}$ ,  $L_{\text{eff}} = 150 \text{ nm}$ ,  $T_{\text{ox}} = 8.5 \text{ nm}$ ,  $SS = 62 \text{ mV/dec}$ ). A new device was realized on SOI with a gate last process but without using a sacrificial gate and named Folded Channel MOSFET [Hisamoto 1998]. Low DIBL was experimentally measured along with a reduction of SS as fin width is decreased down to 15 nm for a minimal gate length of 30nm. The terminology finFET appeared for the first time in 1999 when Huang et al, presented a gate-last process to realize P-MOSFET devices with gate length down to 18 nm, fin width down to 15 nm with excellent performances ( $288\mu\text{A}/\mu\text{m}$  to  $410\mu\text{A}/\mu\text{m}$  with channel effective width normalization) [Huang 1999], [Hisamoto 2000], (Figure 1.18). Multi-fins devices where linked together with SiGe pads, their spacer patterning process removed the SiN from the fin sidewalls and their data and projections for 7 nm node fins turned out to be relatively good predictions [Hashemi 2016 VLSI], [WuSY 2016 IEDM], [XieR 2016 IEDM]. Sacrificial oxidation can improve the fin sidewalls surface and enhance carrier mobility [Lindert 2001].

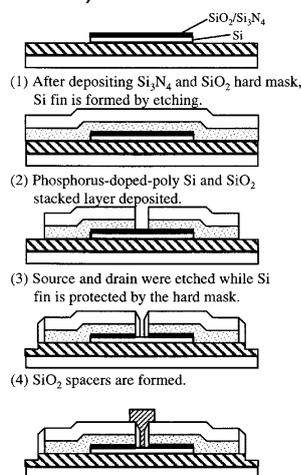


Figure 1.18 - First FinFET process [Hisamoto 2000]

Obtaining narrow fins with a very good control of the width and shape associated with a very low dispersion is essential for this technology. The angle of the fin sidewalls due to lithography and patterning limitations will restrict the maximum height achievable from an electrostatic point of view [WuX 2005]. For example, Liu et al. obtained high A/R fins ( $H_{\text{fin}} = 80 \text{ nm}$   $W = 8.5 \text{ nm}$ ) thanks to wet anisotropic etching [LiuYX 2003], [LiuY 2004], (Figure 1.19). Record fin A/R were obtained in [Van Dal 2007] with 5 nm width and 65 nm tall fins. Similarly to

FDSOI devices, their simulations also showed that the main source of  $V_T$  variation comes from  $L_G$  variations more than from the fin width – respectively, the SOI thickness in FDSOI.

Although Lindert et al. fins were doped, the use of intrinsic channel improves reliability as for planar DG and FDSOI devices and also increases carrier mobility with the reduction of channel transverse effective field. In this case,  $V_T$  may be then adjusted by using appropriate gate material: either with usual heavily doped polysilicon gates or with an asymmetric polysilicon doping of the two gates [Kedzierski 2001], or else, by using metal gate to avoid any poly-depletion issue with fully salicided gates and dopant segregation [Kedzierski 2004], or even metallic gates [Ha 2004], [Mistry 2007], [Auth 2012].

When proceeding with the CMP supposed to remove the gate material on top of the fin – often covered by an insulating hard mask – both gates can be isolated to make them working independently [LiuYX 2003]. In the same idea, a four gates transistor (4T-FinFET) was also proposed to enhance  $V_T$  control [LiuY 2004].

In order to increase devices drive current, several fins can be grouped into a single transistor. Spacer patterning was therefore introduced to double the lithography pitch and reduce the device footprint [Choi 2001], (§1.3.2). Channel stress is also being used as a performance booster [Maitra 2011 EDL], (§1.3.2).

FinFET was qualified in [Poiroux 2009] as the most studied and the most mature of the multiple gate technologies as IBM was presenting their 22 nm technology [Kawasaki 2009 IEDM]. Still, it was only more than two years later that TSMC announced the firsts FinFETs fabricated on an industrial scale in December 2010 [Yeh 2010 IEDM] followed by Intel in May 2011 featuring strained silicon channels enabled by  $\text{Si}_{0.5}\text{Ge}_{0.5}$  RSD and enhanced by a gate-last process [Auth 2012]. This was the third version of their High-k metal gate process which also featured self-aligned contacts (SAC). The fin width was 8 nm and gate length was scaled down to 30 nm. The transistors were called trigates to emphasize the fact that the top of the fin was also conducting. In 2014, the second generation of FinFET had improved fin patterning and doping techniques dividing by two the  $V_T$  dispersion while a 0.7x device scaling was achieved with 8 nm fin width and 42 nm fin height channels [Natarajan 2014]. Fin design is always a trade-off between manufacturability (fin height and width), parasitic capacitances and access resistances. To limit current loss in the bulk substrate, the IBM, SOITEC and STMicroelectronics alliance also presented FinFETs on SOI [Khakifirooz 2013 S3S].

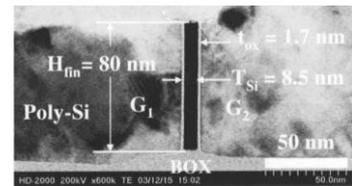


Figure 1.19 – 80 nm / 8.5 nm fin realized by anisotropic wet etching [LiuY 2004].

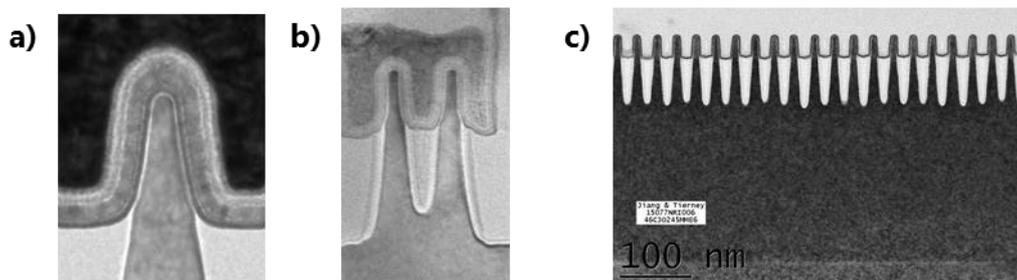


Figure 1.20 - (a) Intel 22 nm FinFET [Auth 2012], (b) Intel 14 nm FinFET [Auth 2014] and (c) IBM 7 nm node FinFET [XieR 2016 IEDM].

If FinFET scaling was recommended to be executed with maintaining an aspect-ratio of  $\sim 2.5$  [Kawasaki 2009 IEDM], Chang et al. pointed out that fin width reduction will be ultimately limited by quantum confinement [Chang 2011]. Their 4 nm narrow fins presented increased  $V_T$  due to band splitting and reduced mobility which cannot be solely attributed to an increased influence of interface states ( $D_{it}$ ). This is one of the reasons why some of the recent developments concerning FinFET are

focused on new channel materials with potentially higher carrier mobility such as germanium rich fins [Hashemi 2016 VLSI], and III-V [Czornomaz 2016 VLSI]. One of the main challenge with these materials remain the interface trap density which limits the actual mobility [Hiblot 2016 PhD]. The 10 nm FinFET technologies are a combination of state-of-the-art patterning, advanced gate stack engineering with multi- $V_T$  abilities [Cho 2016 VLSI] and S/D doping engineering especially concerning the suppression of the bottom fin conduction [Kikuchi 2016 IEDM]. By the end of 2016, the race for the 7 nm has been started with several related publications. Among them, TSMC achieved a 256 Mb  $0.027\mu\text{m}^2$  6-T SRAM by optimizing its DUV immersion lithography process [WuSY 2016 IEDM] while the IBM - GF - Samsung alliance substantiate EUV with a 7 nm process featuring 44 nm contacted poly-pitch (CPP) and 36 nm metallization pitch with dual strained channels for current enhancement and trench epitaxy to reduce access resistances [XieR 2016 IEDM]. An interesting comparison with FDSOI is detailed in [Weber 2015 VLSI] which results came to challenge state-of-the-art 14 nm FinFETs showing similar performances when normalized by the devices effective width. Although FinFET provides large drive current per footprint unit, this is balanced by a larger gate and parasitic capacitance. More than competing technologies, FinFET and FDSOI may actually address different and complementary markets: “Instead of FinFET versus FDSOI, let’s talk about FinFET and FDSOI” [Andrieu 2016].

### 1.2.5. Conclusions

Currently, manufactured horizontal double gate technologies consist in FDSOI (§1.2.1). The main advantage is the asymmetric back gate polarization which can be used dynamically to boost either the performances (forward back bias) or to lower the power consumption (reverse back bias). Fabrication process being closer from planar bulk technologies is another benefit for the cost of FDSOI.

Driven by the potential of volume inversion, many other advances were achieved concerning the fabrication of symmetric double-gate devices (§1.2.2) and SON (§1.2.3). Although none of them reached an industrial maturity, the experience accumulated during these developments provides information about the processes and feasibility. To illustrate this point within this thesis framework, the selective removal of SiGe developed for SON technology can be adapted for the critical step of forming the suspended silicon nanowire channels in SNWFETs as it will be observed in the next and last subchapter (§1.3.4).

Vertical double gate or FinFET technology (§1.2.4) on the other hand offers the best device compacity at the price of increased access resistance and parasitic capacitances. At the beginning of 2017, FinFET scaling remain crucial for the sub 7 nm nodes technologies.

With one or two additional gates, the nanowire geometry can be considered as a new step forward in transistor scaling. The following sub-chapter states the actual positioning of NWFETs and SNWFETs before concluding on the thesis objectives.

### 1.3. The nanowire technology: down to the end of the roadmap?

By using tri-gates,  $\Omega$ -gates or ultimately gate-all-around (GAA) configurations, NW channels benefit from increased electrostatic control of the gate over the channel. The first section describes the state-of-the-art of NWFET technology (§1.3.1). This is followed by several studies of NWFETs confirming their compatibility with usual technology improvements. The impact of channel strain and channel orientation optimization are first measured in §1.3.2. To improve integration density and transistor performance, advanced double patterning techniques are also investigated in §1.3.3. The following section is then dedicated to the possibility of increasing the drive current of such devices at no cost in device footprint – wafer area occupation – by vertically stacking several NW channels (§1.3.4). This sub-chapter concludes with the thesis objectives, setting SNWFETs as a potential evolution of FinFET technology by means of a performance evaluation and device fabrication processes as close as possible from the existent (§1.3.5).

#### 1.3.1. Tri-Gates, $\pi$ -gate, $\Omega$ -gate and gate-all-around (GAA) nanowire FETs

In the 80's, trench isolation was investigated to remove the bird's-beak shape due to selective oxidation in structures such as DELTA [Hisamoto 1989]. In the process named BOX for buried oxide [Kurosawa 1981], the gate was also in contact with the sidewall of the silicon channels creating two extra vertical "parasitic" channels along with the horizontal one. A double hump in the I-V characteristics of devices revealed the presence of the two different channels having their own different threshold voltages. This was attributed to the sharp corners where the electric field is higher, lowering  $V_T$  locally [Iizuka 1981]. First considered as parasitic, it was suppressed by using lateral doping. These gate extensions were finally found to be interesting to increase controllability over the channel especially when the sidewalls are brought close enough to merge the depletion regions [Hieda 1987]. Improvements were reported in [Hieda 1989] where sidewall gates were then used to control sidewall channels. This was one of the first tri-gate transistor which was named at that time trench-isolated transistor using sidewall gates (TIS). Subthreshold swing was improved by 30 mV/decade over LOCOS insulation MOSFET. The double hump in the I-V characteristics was also found to be reduced with channel width. This was confirmed in the devices fabricated by Doyle et al. (30 nm to 60 nm thick bodies under  $L_G = 30$  nm tri-gates) [Doyle 2003]. Their simulations preconize the use of rounded corner edges to limit the  $V_T$  lowering. Besides, [Yang 2004] presented a 10 nm diameter NW with 5 nm gate length named the "nanowire FinFET". As channel dimensions were reduced, the trigate transistor became a nanowire FET only differentiated from a FinFET by an aspect-ratio (A/R) close to one. The absence of remaining hard mask on top of the fin makes the top of the fin also conducting and FinFETs are sometimes called trigates.

Similarly to FinFETs and other 3D architectures, current in tri-gate NW FETs is often normalized by the effective width  $W_{\text{eff}} = 2xH + W$  (Figure 1.21a). The NWs must be arranged in multi-finger arrays of pitch smaller than  $W+H/2$  for competing with single gate devices in terms of effective width (Figure 1.21b).

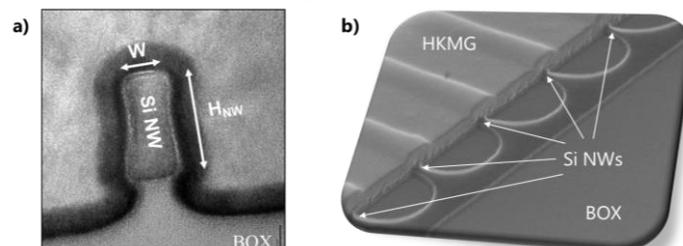


Figure 1.21 - (a) cross-section of a trigate NW channel (TEM) and (b) trigate NW array (SEM).

Although tall fins present higher  $W_{\text{eff}}$ , electrostatic control is found to be better in near-to-one aspect-ratio tri-gates NWs (§1.1.1) which can additionally benefit from body effect for  $V_T$  control when fabricated on SOI [Coquand 2013], [Hiblot 2015]. To increase even more the electrostatic control in such NW, Park et al. proposed the  $\pi$ -gate concept where the gate enters in the BOX to increase its control over the channel [Park 2001]. This concept goes even further with the  $\Omega$ -gate where an isotropic etch of the BOX offers some space under the channel for the gate stack to be deposited [Jahan 2005]. The process must then feature an isotropic step during which the gate stack is etched away from under the nanowire in the extension regions. Instead of BOX over etch, the rounded nanowire can also be obtained from a square shape tri-gate NW using hydrogen annealing [Hashemi 2010]. This technique had also been previously employed to improve channel mobility by smoothing the channel surface [Dornel 2007 APL]. Rounding the sharp corners again prevents  $V_T$  and SS lowering [Ritzenthaler 2005].

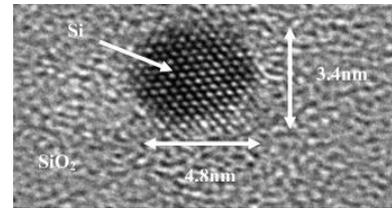


Figure 1.22 - Cross section of a silicon nanowire obtained by a self-limited oxidation to achieve a sub-5nm channel [Hubert 2008 ECST]

From an electrostatic point of view, the ultimate nanowire device would be the gate-all-around (GAA) structure. It was realized for the first time from a BOX over etch [Colinge 1990]. Samsung in 2005 announced one of the first NW MOSFET with a “highly manufacturable” process, proposing their “parallel Twins Silicon NW (TSNWFET)” [Suk 2005]. The 10 nm diameter n and p-FETs presented extremely low DIBL (31 mV/V NMOS and 15 mV/V PMOS), high SS (71 mV/dec NMOS and 66 mV/dec PMOS) at 30 nm gate length and impressive ON/OFF currents (2.64 mA/ $\mu\text{m}$  / 3.1 nA – diameter normalized). The NW FETs fabricated in the recent years confirm these interesting properties [Tachi 2010 IEDM], [Bangsaruntip 2009 IEDM], [Saitoh 2010 VLSI], [Barraud 2012 EDL], [Bangsaruntip 2013 IEDM]. Similarly to planar architectures, their compatibility with high-k metal gate [Barraud 2013 VLSI], strain engineering [Coquand 2012 VLSI], Ge channels [Suh 2011 APL], [WanCC 2016 SSDM] or SiGe channels [Woo 2012 APL], [Hashemi 2013 VLSI], [Nguyen 2014 IEDM] have been studied with aggressively scaled NW width and gate length down to 10 nm and 15 nm respectively or with surrounding gates (GAA) [Chen 2008], [Chen 2010].

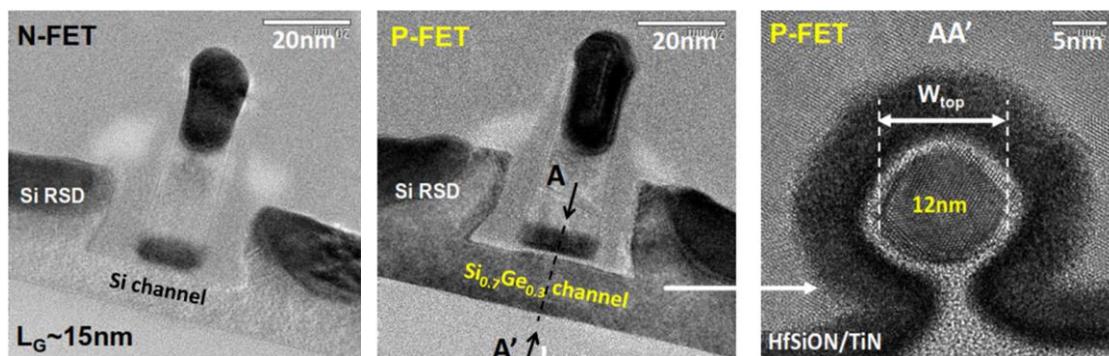


Figure 1.23 - NFET and PFET with Si and SiGe NW channels and  $\Omega$ -gate successfully co-integrated [Nguyen 2014 IEDM].

However, the GAA configurations and in a certain way the  $\Omega$ -gate ones involves an overetch of the gate. The resulting trimming of the gate may ultimately limit the scaling of such devices as the gate length is shrunk.

### 1.3.2. Technology boosters: channel orientation and strain in trigate nanowire FETs.

During the design and fabrication of such devices, the transistor channels can be orientated in diverse ways to benefit from the anisotropy of the carrier mobility in silicon. Strain can also be introduced into the channel to modify the band structure and the effective masses and thereby improve carrier mobility. Although these effects are now well known in bulk silicon, the quantum confinement induced by the nanowire geometry may alter the usual conclusions. This section revises the current knowledge on such matters and brings several updates concerning hole transport with measurements realized on PMOS devices.

#### Channel orientation

Industry commonly use (001) surface silicon wafers. The fabricated devices are typically oriented in the <110> direction but the <100> direction is accessible by a 45° rotation (Figure 1.24). Device properties and more specifically carrier mobility will strongly depend on these crystallographic planes and orientations [Yang 2003], [Andrieu 2007], [Bidal 2008], [BenAkkez 2012]. [Chen 2008] proposed a fully proportional relationship between (110) and (100) mobilities (Eq. 1-7).

$$\mu_{eff, trigate} = \frac{W}{W + 2H} \mu_{100} + \frac{2H}{W + 2H} \mu_{110} \quad (Eq. 1-7)$$

This relation was successfully applied in [Chen 2010], [Coquand 2012 ULIS], [Coquand 2013 SSE] and [Coquand 2013 TED] to confirm the advantage of (110) sidewalls for the transport of holes and the (001) top surface for the transport of electrons (Figure 1.24). As a consequence, electron effective mobility is found to be decreased with decreasing NW width as the relative contribution of the top channel is also decreased. The opposite is observed in the case of hole transport.

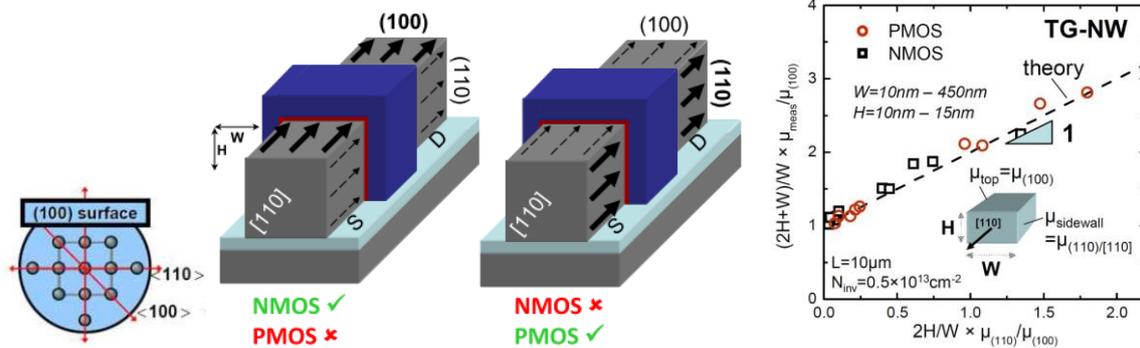


Figure 1.24 - Trigate NW interfaces orientations and proportionality of the sidewall mobility [Coquand 2012 ULIS].

Another example is measured in [Gaben 2015 EUROSIOI-ULIS]. Split C-V measurements [2004 Romanjek EDL] on arrays of 50 NWs having 10 μm gate lengths confirmed an improvement of the hole effective mobility as the NW width is reduced and as the NW height is increased (Figure 1.25). Up to +38% had been obtained when increasing the vertical sidewall contribution by switching from a large channel to a 10 nm narrow by 24 nm tall NW. This points out again the advantage of the (110) sidewalls for the transport of holes.

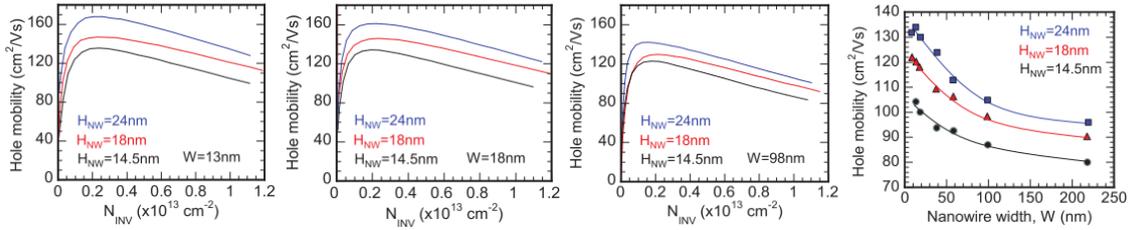


Figure 1.25 - Effective mobility as a function of  $N_{INV}$  for different NW width and height [Gaben 2015].

For a given  $H_{NW} = 11$  nm, Figure 1.26 summarizes the impact of channel width on electron and hole mobility from measurements realized in [Coquand 2012], [Barraud 2013 VLSI] and [Gaben 2015].

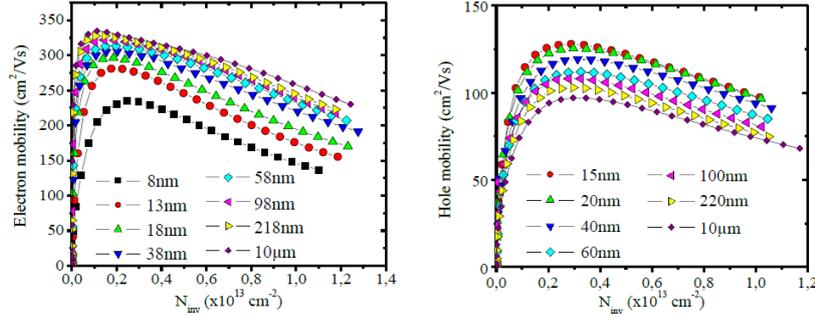


Figure 1.26 – (a) Electron and (b) hole effective mobility as a function of  $N_{INV}$  for different NW widths and for  $H_{NW} = 11$  nm as synthesized in [Barraud 2017 TED].

Let's consider devices oriented along the [100] direction instead. Supposing a facet-dominated transport model, a constant carrier mobility would be expected when reducing NW width since this time both sidewalls and top surface are {100} planes. However, when decreasing the width below 25 nm, an electron mobility degradation is observed (Figure 1.27a). Although it is slightly less important than in the [110]-oriented channel, this invites reconsidering the facet dominated transport model in narrow devices. This is also confirmed by the small hole mobility degradation observed in the narrowest [100]-oriented channels (Figure 1.27b).

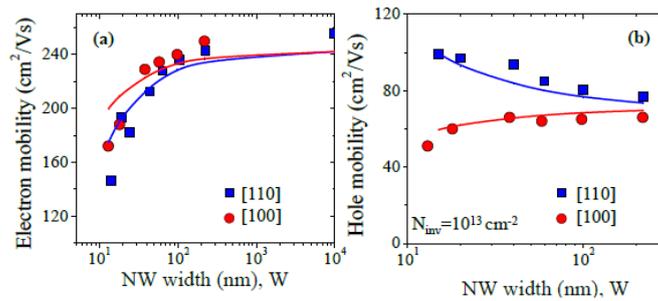


Figure 1.27 – (a) Electron and (b) hole effective mobility as a function of nanowire width at  $N_{inv} = 10^{13} \text{ cm}^{-2}$  for [110] and [100] channels ( $H_{NW} = 11$  nm and  $L_G = 10 \mu\text{m}$ ). Solid line represents NEGF calculation.

Non-Equilibrium Green's Functions (NEGF) calculations in cylindrical and square Si NWs provide further insights into the dependence of hole mobility on NW width [Niquet 2012 ULIS], [Niquet 2012 Nano Lett.], [Niquet 2012 TED]. The valence bands are degenerated – brought together – in  $\langle 100 \rangle$  Si NWs and presents heavy effective masses while in  $\langle 110 \rangle$  oriented channels, light holes sub-bands gets separated from heavier ones due to quantum confinement. As a result, hole mobility is considerably degraded by the enhancement of electron-phonon and surface roughness scattering in small  $\langle 100 \rangle$  Si NWs, while it continues to increase down to very small sizes in  $\langle 110 \rangle$  Si NWs. In other words, the anisotropy in hole mobility is explained by the difference in effective masses which are impacted differently by structural confinement according to the transport direction. Confinement in Si NWs

enhances carrier-phonon and surface roughness interaction when decreasing NW width or height [Niquet 2012 ULIS], [Neophytou 2011], [JinS 2007]. Low temperature measurements of Figure 1.28 confirm this stronger surface roughness scattering in the narrowest NWs consistently with [JinS 2007]. At the same time, the phonon-limited mobility extracted from Matthiessen's rule and temperature dependent measurements of mobility, is invariant regardless of NW width (Figure 1.28b) consistently with [Fischetti 1996] and [Niquet 2012 TED]. This suggest the mobility in smallest NWs to be surface-roughness limited.

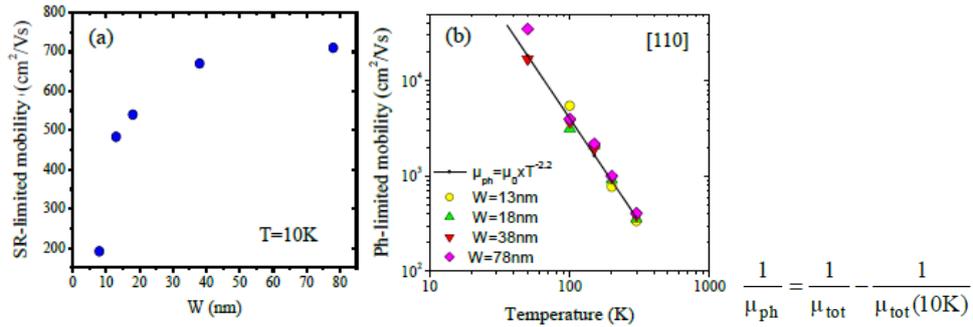


Figure 1.28 – (a) Surface-roughness limited mobility ( $N_{inv} = 10^{13} \text{ cm}^{-2}$ ) as a function of NW width at  $T = 10 \text{ K}$  and (b) phonon-limited mobility as a function of temperature at  $N_{inv} = 10^{13} \text{ cm}^{-2}$  for different NW widths.

Channel orientation was also studied in [Saitoh 2010]. By opting for <100> over <110> channels +25% and +14% increase of  $I_{ON}$  was achieved in N and P-FETs respectively. Noticing the  $\sim 8\%$   $T_{inv}$  reduction in <100> is not sufficient to increase  $I_{ON}$  by itself, they conclude on a carrier velocity improvement in their short channel devices. The decrease of  $\mu_e$  with  $W_{NW}$  shrinking is also found on long channel devices and despite of the (110) side channels, the  $I_{ON}$  for the PFETs is much lower than for the NFETs. They also found a deviation from the linear relationship they attributed to an additional scattering in narrow PFETs. They extracted from charge pumping, the density of interface defects ( $D_{it}$ ) and isolated each contribution with Mathiessen rule and they concluded that surface roughness is the main contribution to the carrier mobility degradation in NWs. Accessorily, higher  $D_{it}$  was found for the side channels due to RIE patterning. The contribution of gate induced stress was also studied. Transverse compressive and vertical tensile strain on the side channel largely decrease  $\mu_e$  of <110> NFETs and moreover, NFETs seem to be more sensitive to stress than PFETs.

## Channel stress

The benefits of strained channels were briefly presented in the section concerning FDSOI [Andrieu 2010], [Fenouillet-Beranger 2012 VLSI], [LiuQ 2013], [Weber 2014], (§1.2.1). With SON technology (§1.2.3), leaving the SiGe layer under the channel as a stressor [Chanemougame 2005] has been investigated. SiGe raised source and drain (RSD) were introduced to boost the performances of 90 nm node silicon bulk devices [Ghani 2003], [Mistry 2007]. They are still used on FinFET with enhanced effects due to the gate-last process [Auth 2012], [Natarajan 2014], (§1.2.4). Other techniques are available to introduce some stress in the channel such as the strain memorization technique [Chen 2004] or the use of a contact etch stop layer (CESL) [Thompson 2002]. A gate-last process is also known to enhance strain [Morvan 2013 IEDM].

The introduction of biaxial or uniaxial strain in the silicon channel modifies its band structure (splitting and/or degeneracy) which impacts electron and hole transport consequently [Skotnicki 2008]. Quantum confinement also adds up to the equation which makes the behavior of NW based devices extremely complex. Fully atomistic semi-empirical calculation of [Niquet 2012 ULIS] and [Neophytou 2011] have shown uniaxial tensile strain lowers the ground state valleys respectively towards the heavier ones. The proportion of fast electrons is increased and inter-valley scattering is

reduced which translate into a higher  $\mu_e$ . Concerning hole transport, biaxial tensile strain removes the degeneracy of the valence bands increasing the number of light holes so as the mobility. Moreover, as the NW width is reduced, the strain becomes uniaxial which was found in [Niquet 2012 TED] to lift upwards the heavy holes sub-bands resulting in a degradation of the mobility. The transition biaxial towards uniaxial can be observed experimentally in  $V_T$  measurements of [Coquand 2013 TED] and was predicted in [LimJS 2004 EDL]. On the contrary, uniaxial compressive strain seems preferable to improve hole transport in narrow channels.

Uniaxial tensile-strained  $\Omega$ -gate strained SOI (sSOI) n-FET NWs down to 10nm gate length were realized [Barraud 2013 VLSI] as well as high-performance  $\Omega$ -gate p-FETs on compressively-strained-SiGeOI substrates obtained by Ge enrichment [Nguyen 2014 S3S]. These were later successfully co-integrated to offer -50% delay reduction in fan-out 3 ring oscillators [Nguyen 2014 IEDM]. No electron mobility degradation due to co-integration was noticed but +135% in hole mobility was obtained in strained SiGe narrow channels benefiting from uniaxial stress – only +60% in the largest devices embedding biaxial stress.

[Coquand 2012 VLSI] measured +40% increase in saturation current for  $L_G = 45$  nm long and 11 nm large uniaxially stressed channels of NMOS NWFETs. Capacitive measurements on devices realized with strained-SOI substrates showed +70% electron effective mobility improvement over standard SOI devices. This enhancement drops down to +55% on 10 nm narrow NWs as the biaxial strain becomes uniaxial. This was confirmed on 45 nm short channel with +40% drive current improvement.

Another way to bring compressive stress into the NW channels is to proceed with a selective epitaxial growth (SEG) of the RSD. The impact of  $\text{Si}_{0.7}\text{Ge}_{0.3}$  RSD thickness on P-type trigate NW FETs has been reported at the beginning of this thesis [Gaben 2015]. In this work, various SOI thicknesses from 11 nm to 24 nm were patterned into NWs in between 10 nm and 10  $\mu\text{m}$  large. This was followed by the process already used for previous publications of the group: high-k/metal gate (HfSiON/TiN) was patterned in a gate-first process and, after the etching of a 10 nm large spacer, a SEG of either 20 nm or 30 nm of  $\text{Si}_{0.7}\text{Ge}_{0.3}$  Boron in situ doped was realized to form the RSDs. A high dose doping (HDD) implant, an activation spike annealing and a NiPt salicidation followed before the back-end. Figure 1.29 summarizes the key process steps along with a cross-section TEM and Energy Dispersive X-ray spectroscopy (EDX) images of a 25 nm tall and 10 nm narrow device.

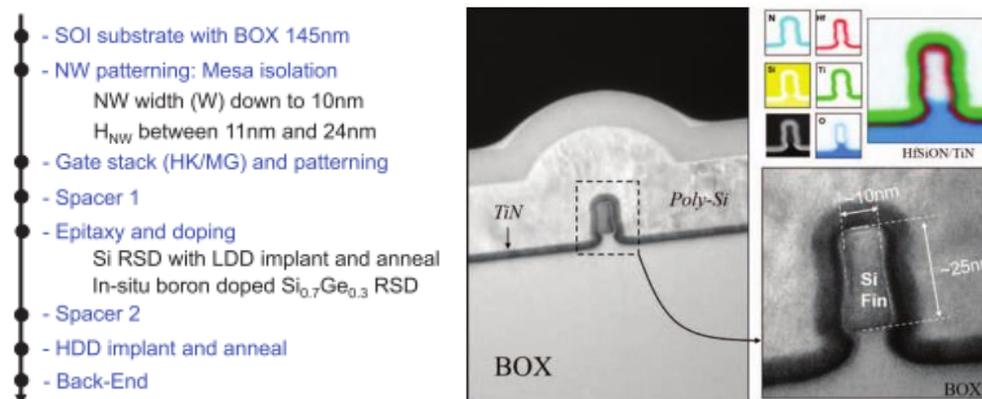


Figure 1.29 - Main process flow steps and TEM/EDX images of a 10 nm narrow and 25 nm tall NW channel [Gaben 2015].

The effect of  $\text{Si}_{0.7}\text{Ge}_{0.3}$  RSD is evaluated in Figure 1.30 for gate lengths down to 25 nm – the effect on long gate lengths is negligible. Up to +86% improvement in drive current is obtained for the introduction of SiGe RSD on the smallest 12 nm NWs. This advantage drops at +58% only for the 24 nm tall NWs. Influence of strain induced by SiGe RSD can be further improved by increasing the RSD SEG thickness: +36% is obtained by increasing the epitaxy from 20 nm to 30 nm (Figure 1.30.a).

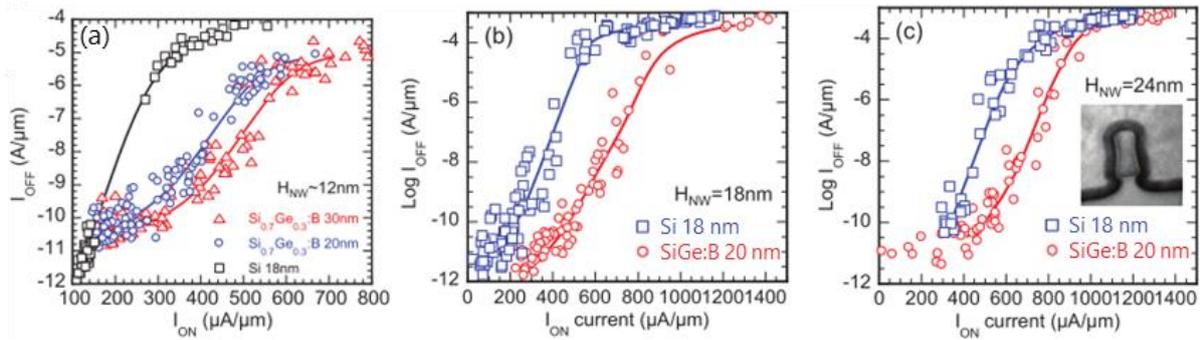


Figure 1.30 -  $I_{ON}$ - $I_{OFF}$  curves at  $V_G = V_{DD} = 0.9\text{V}$  for different RSD nature and thicknesses for three NW thicknesses: (a) 12 nm, (b) 18 nm and (c) 24 nm [Gaben 2015].

SiGe RSDs are confirmed to be an effective way to increase channel compressive strain and to enhance hole mobility. Although it seems to be more efficient on the smallest NWs, an increase in the epitaxy thickness is expected to bring more stress in the tallest NWs. A rise in the Ge portion is also likely a way to transfer more stress into the channel [Auth 2012], [Natarajan 2014]. SiGe SD stressors may compensate for the hole mobility loss due to the use of a sSOI substrate which usually embeds tensile stress to boost the NMOS devices. The effect of SiGe RSDs is enhanced when the NW extensions are first recessed before to proceed with the SEG [Barraud 2013 VLSI]. Similarly, SiC RSD can be introduced to induce tensile strain [Ang 2005], [Liow 2007], [Togo 2012]. Since these electron and hole mobility improvements are due to uniaxial stress which results in a change in effective mass instead of a scattering mechanism reduction, this effect is believed to be preserved when scaling the gate length [Thomson 2004].

Co-integration of local strain engineering techniques is currently under study for making PMOS and NMOS independently benefit from stress. These techniques named Strained Silicon by Top Recrystallization of Amorphized SiGe on SOI (STRASS) and BOX creep, are illustrated in Figure 1.31 [Bonnevialle 2016]. After the Shallow Trench Isolation (STI) module, it is possible to induce or to relax stress by carefully optimizing epitaxy and annealing steps. Design co-optimization is also extremely important for a platform technology to fully benefit from each introduced booster [Berthelon 2016 VLSI], [Berthelon 2017 EUROSIOI]. Therefore, according to our results, such developments are also of primary interest for enhancing performances of NW technologies.

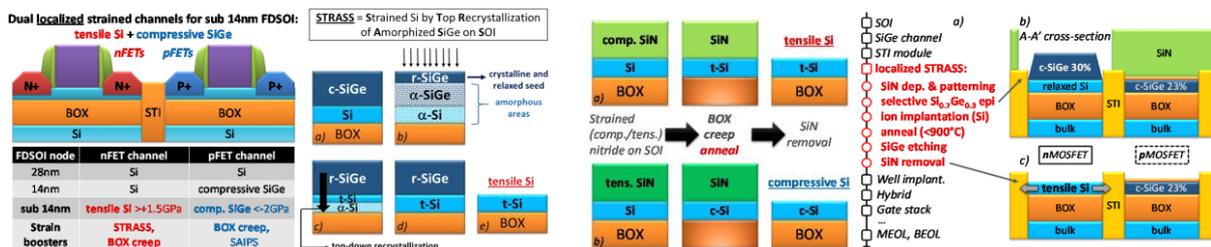


Figure 1.31 – (a) Need of strained channels for sub-14 nm node FDSOI. (b) Principle of Strained Silicon by Top Recrystallization of Amorphized SiGe on SOI (STRASS) and (c) BOX Creep. (d) Dual strained channel can be co-integrated using proper masking [Bonnevialle 2016].

### 1.3.3. Technology boosters: the case of Sidewall Image Transfer (SIT)

The multiple patterning technique was proposed for the first time in [Choi 2001], [Choi 2002 SSE], [Choi 2002 TED] in order to deal with lithography limitations and still divide by two or four the minimum pitch. An interesting derivation of the STI patterning was also used to divide an active area into two silicon fins avoiding the use of core material in [KimSM 2004]. Techniques such as Sidewall Image Transfer (SIT) or Self-Aligned Double or Quadruple Patterning (SADP / SAQP) alleviates any misalignment issues introduced by multiple exposures as explained in Figure 1.32 drawings. These techniques were first industrialized for the first metal layers in back end of line (BEOL) [Hwang 2009 ESSDERC] and are now used in 14 nm node processes to decrease the fin pitch in the active layer [Yamashita 2011], [Auth 2012 VLSI], [Natarajan 2014 IEDM]. Introduction of SIT for Samsung is planned for the 10 nm node [Cho 2016 VLSI] while IBM presented devices with a 30 nm fin pitch for their 7 nm node FinFET using EUV lithography [XieR 2016 IEDM]. Pitch was limited to 40 nm when using DUV lithography [Basker 2010 VLSI].

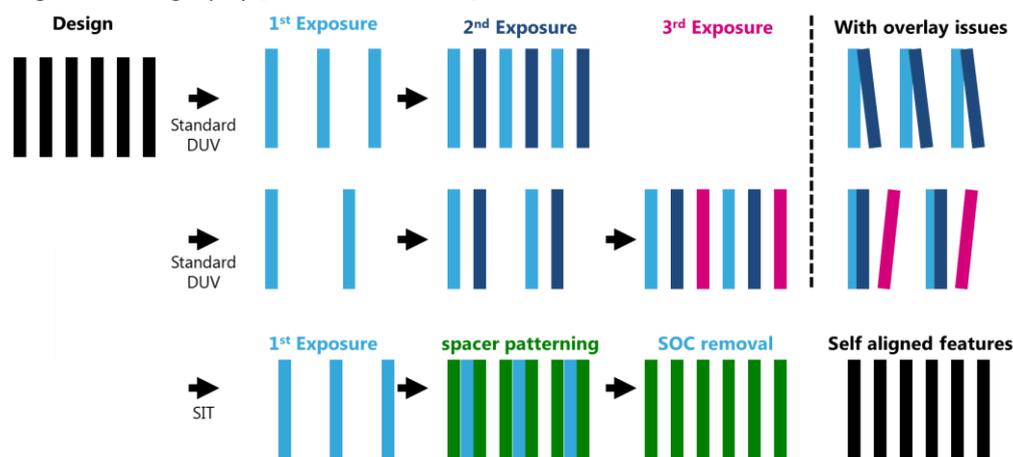


Figure 1.32 – Top view illustrations for the need of self-aligned patterning (SIT).

The process developed in CEA-LETI for the patterning of silicon nanowires has been described in [Barnola 2014 SPIE]. It was used to produce 35 nm pitch silicon NWs  $\Omega$ -FETs for which performances were reported at the beginning of this thesis in [Gaben 2015 SSDM]. Figure 1.33 provides an overview of the overall process flow. Starting from 300 mm SOI substrates with a 145 nm buried oxide (BOX), initial silicon thickness was thinned down to 8 nm and 5 nm. Then, a 15 nm thick Titanium Nitride (TiN) layer was deposited. This buffer layer served at the end as a hard mask for the patterning of silicon NWs. It was found to reduce NW width distortion caused by both micro-loading effects due to spacer asymmetry and by silicon consumption during Si-rich anti-reflective coating (Si-ARC) removal and spacer patterning. Then, a spin-on-carbon (SOC) layer and a Si-ARC were deposited for the initial lithography. High end DUV immersion lithography tools can reach 70 nm pitch, however the available Nikon SR1 is limited to 180 nm. Electron beam (e-beam) lithography was required to pattern the 70 nm features in photoresist and SOC aiming for a 35 nm pitch after the SIT process. The resist patterns were trimmed with  $\text{Cl}_2/\text{O}_2$  before to transfer them into the Si-Arc and SOC layers using respectively  $\text{CH}_2\text{F}_2/\text{CF}_4/\text{He}$  and  $\text{HBr}/\text{O}_2$  chemistries. Si-ARC was removed in order to only leave the SOC mandrel. The next step involved conformal deposition of a SiN layer in a process optimized to be highly uniform and controllable. This SiN spacer material was anisotropically etched with  $\text{CH}_2\text{F}_2/\text{O}_2/\text{CF}_4$  plasma, so that it was completely removed everywhere excepted along the sidewalls of the previously patterned sacrificial material (SOC). A sub-network of hard-mask spacers was left with a spatial frequency two times smaller than obtained with the first lithography (35 nm). Finally, the SOC mandrels were selectively removed using  $\text{O}_2$  plasma allowing the transfer of the remaining spacers into the TiN and into the silicon layers using TiN as a masking layer.

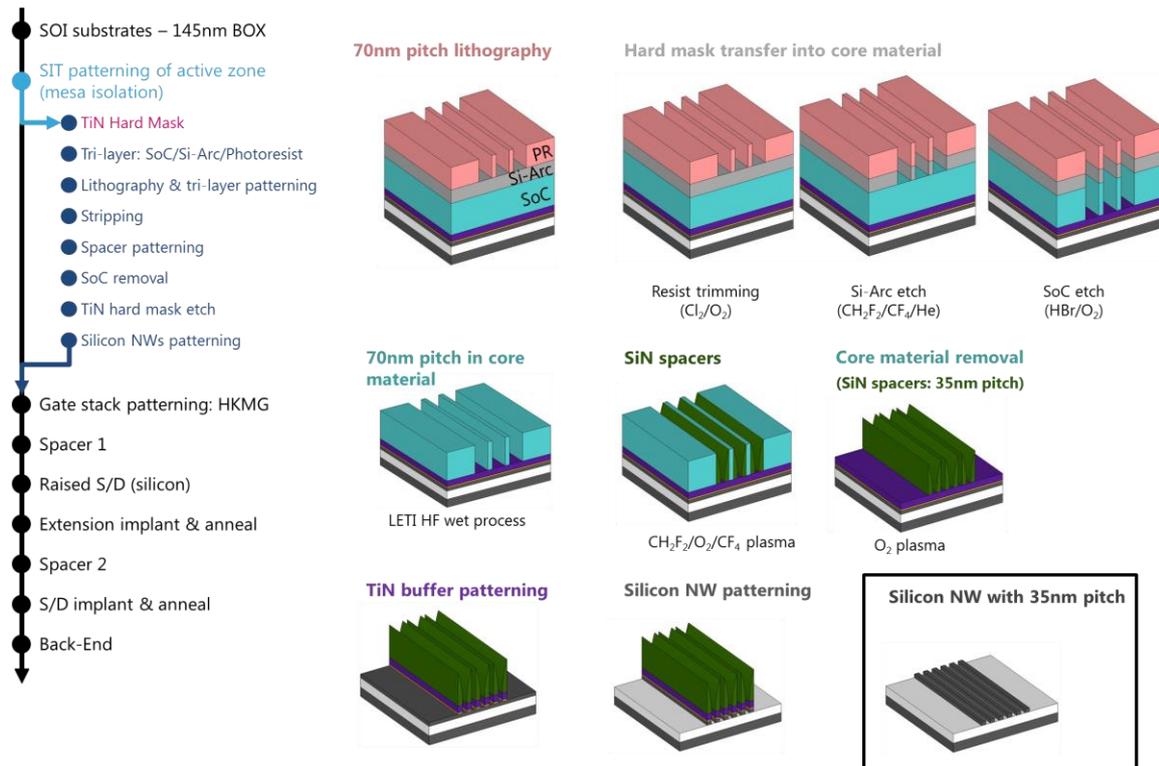


Figure 1.33 – CEA-LETI SIT process flow [Barnola 2014 SPIE], [Gaben 2015 SSDM].

Two types of devices with 6 or 250 parallel NWs were realized. The TEM images of Figure 1.34 report NW widths down to 12 nm and NW thicknesses down to 5 nm. Our typical gate-first process was then used to build the transistors (§1.3.2). The high- $\kappa$  metal gate stack consisted in 1.9 nm chemical vapor deposition (CVD) of HfSiON, 5 nm atomic layer deposition (ALD) of TiN and 50 nm polysilicon (EOT = 1.3 nm). After patterning, gate lengths as small as 16 nm were obtained as shown in Figure 1.34. A 10 nm thick SiN layer was then deposited and etched to form a first spacer on the sidewalls of the gate. 20 nm-thick Si raised source and drain (SD) were selectively grown at 750°C, 20 Torr prior to the SD extension implantation and activation annealing. At this step, a second offset spacer consisting of a tetraethyl orthosilicate (TEOS) liner and a nitride layer was fabricated before the SD implantations, activation spike anneal and silicidation (NiPtSi silicide), in order to lower the contact resistance. Finally, tungsten contacts and standard Cu back-end-of-the-line process were performed.

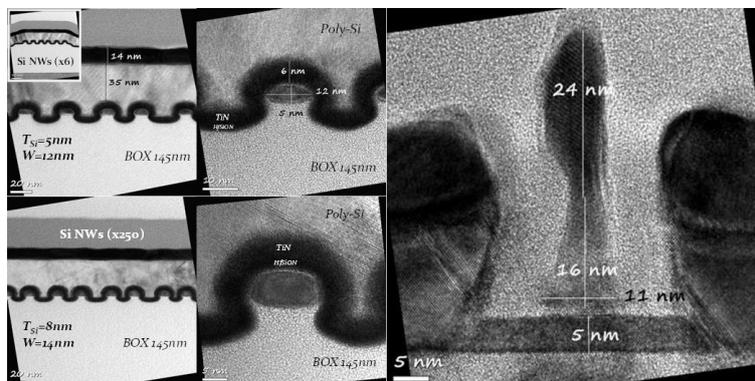


Figure 1.34 – Cross-section TEM into 6 and 250 parallel NWs realized through SIT and longitudinal section TEM of a 16 nm gate.

Measurements on 250 NWs (Figure 1.35 a and b) reported good  $I_{ON}$ - $I_{OFF}$  currents for such NW based structures without any strain engineering yet ( $I_{ON,NMOS} = 650 \mu A/\mu m$  and  $I_{ON,PMOS} = 290 \mu A/\mu m$  at  $I_{OFF} = 100 nA/\mu m$ ). Mobility measurements are in accordance with previous work with isolated devices (Figure 1.35 c & d), [Barraud 2012 EDL], [Gaben 2015 ULIS] which testifies that the SIT process did not impact the channel surface quality. Differences in between 6 and 250 NW channel NMOS devices are related to the smaller channel height of the 6 NW devices (insets of Figure 1.35c). The higher NWs also evidence higher DIBL in Figure 1.35e. Dopant diffusion is likely reducing the channel effective length translating into higher than expected DIBL measurements (cf. simulations in §2).

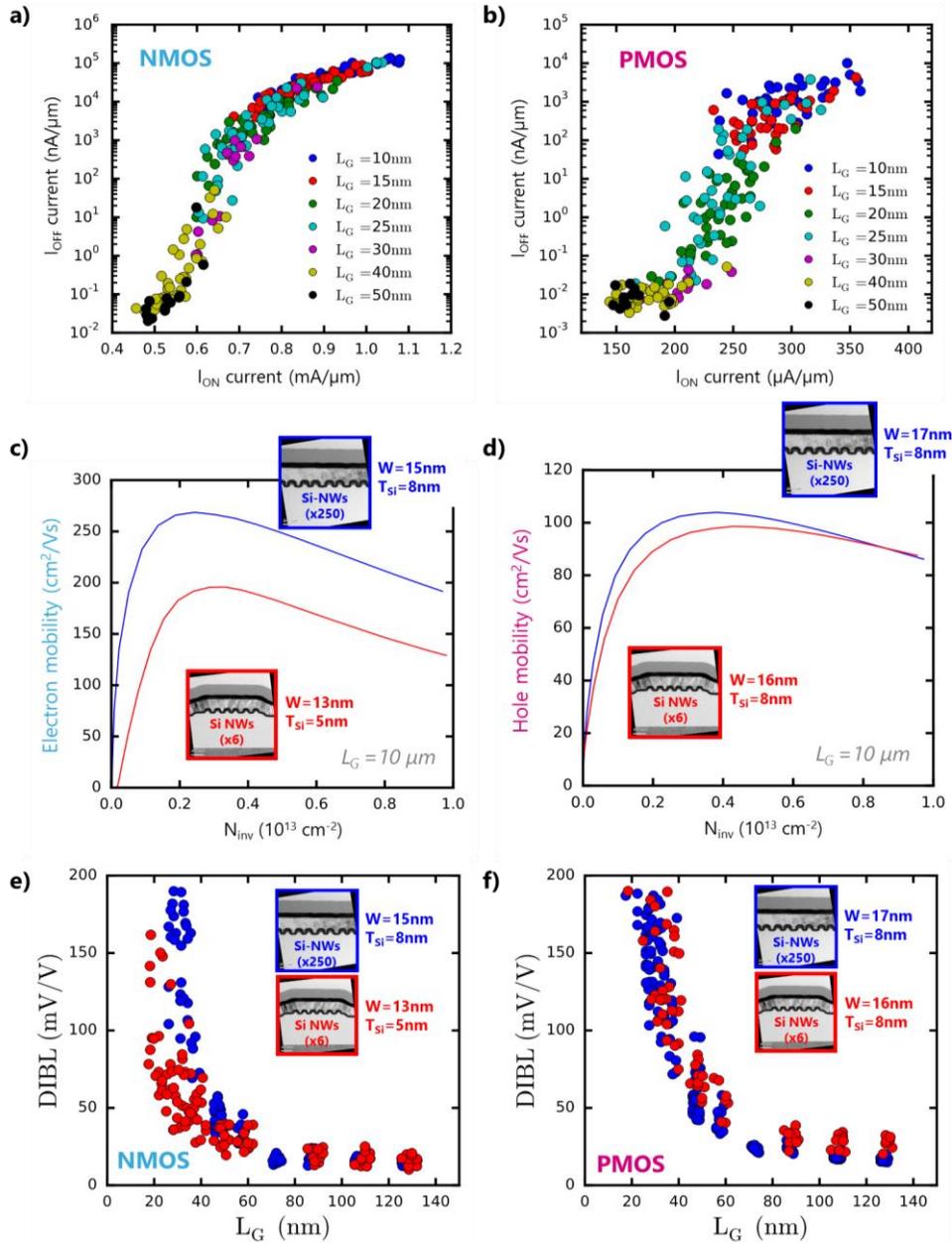


Figure 1.35 - (a) and (b)  $I$ - $V$  characteristics for 250 NW NMOS and PMOS devices, (c) and (d) mobility measurements, (e) and (f) DIBL for all devices ( $V_{DD} = 0.9 V$ ).

Recent improvements of this SIT process led to the fabrication of Si/SiGe fins for the realization of stacked NWs (§3.3). Other SADP techniques concerns pillar duplication for symmetric and antisymmetric standard cells such as memories [HongJ 2016 SSDM]. Self-assembly of polymers is also a promising technique to push forward the limitations of DUV [TsaiH 2014 ACS Nano]. TSMC recently managed to extend the use of DUV lithography to 7 nm node [WuSY 2016 IEDM].

### 1.3.4. Stacked NWs

#### History and known advantages

SON process described in §1.2.3 involves a SiGe sacrificial layer. Derivations of this process naturally led to multi-channel devices (MCFETs) as the SiGe/Si epitaxies can be repeated several times to produce a super-lattice alternating several channels and sacrificial layers [Hartmann 2005]. The first devices were reported by Samsung in [LeeSY 2003], [Yoon 2004], [LeeSY 2004] featuring a damascene process [OhCW 2003], [Yun 2006] where SiGe acts as a sacrificial gate material. A first SRAM was presented in [KimMS 2006 VLSI].

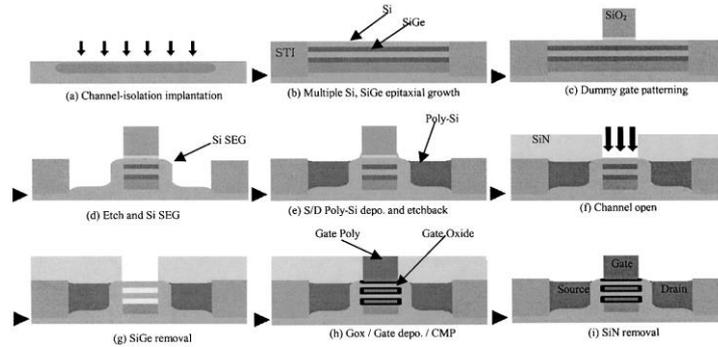


Figure 1.36 – MCFETs realized with sacrificial SiGe in a damascene process [LeeSY 2003].

The adoption of a novel architecture such as stacked-NW FETs (SNWFETs) would be obviously facilitated if the process fabrication could remain as close as possible from the main stream development efforts. A “FinFET-like process” is used in [Ernst 2006] to stack three or four NWs (Figure 1.37). The 70 nm large and 15 nm high suspended NWs were wrapped in HfO<sub>2</sub> and TiN high-k metal gates. The gates were either self-aligned in between the SD pads or either defined by an anisotropic etch followed by an isotropic etch in order to remove the material from in between the NWs. As a consequence, the gate is also trimmed. Figure 1.37 c and d illustrates two issues encountered with this integration: beam buckling and void creation during the gate stack deposition. This was subsequently improved in [Bernard 2008 SSE].

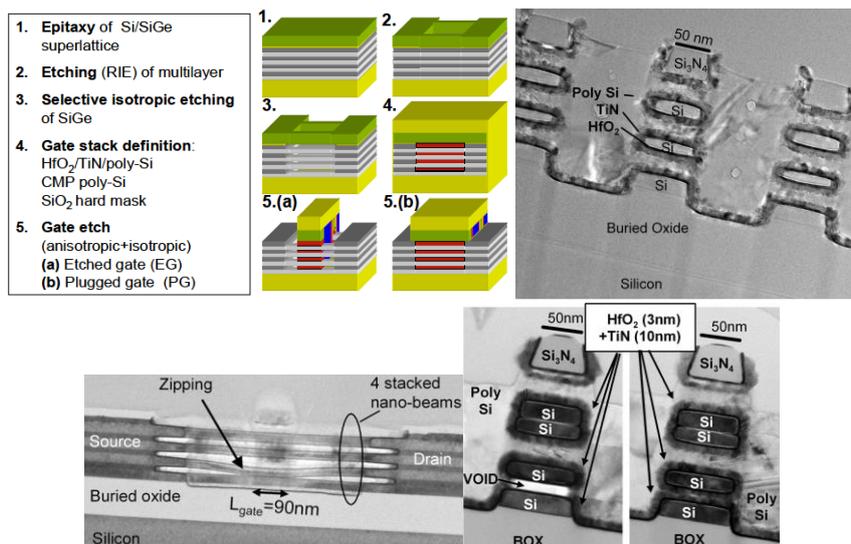


Figure 1.37 – (a) FinFET-like adapted process for stacked NWs as in [Ernst 2006], (b) TEM cross-section after gate stack deposition. (c) Illustration of beam buckling risk attributed to wet process for surface cleaning before High-k deposition and (d) TEM cross-section of such effect and also for the illustration of the risk of void apparition if the deposition is not conformal enough.

The process was later improved to produce 10 nm thin channels showing  $I_{ON}$  currents of 2.27 mA/ $\mu\text{m}$  and 1.32 mA/ $\mu\text{m}$  for N and PMOS respectively and  $I_{OFF} = 16.5$  pA/ $\mu\text{m}$  [Bernard 2008 VLSI]. The process no longer use suspended channels as the sacrificial SiGe is removed after the SD epitaxy. This however requires additional lithography steps as pictured in Figure 1.38. The bottom channel of the stack can be seen as a common FDSOI transistor, yet it can be turned off by applying proper back bias ( $V_T$  increase) since this channel features an increased access resistance and poorer performances as compared to the above GAA channels [Dupré 2008 ESSDERC].

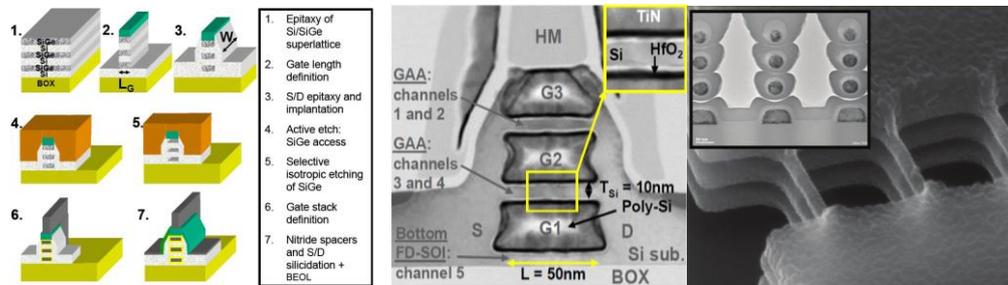


Figure 1.38 – (a) New process for stacked NW and (b) TEM cross-section after gate stack deposition [Bernard 2008]. (c) 3D stacked nanowires rounded by hydrogen annealing [Dornel 2007 APL].

In order to increase drive current in FinFETs, one or several parallel channels must be added. This discrete layout limitation is alleviated in SNWFETs by simply tuning NW width [Ernst 2008 ICICDT] or by adding more NWs in the stack (Figure 1.39a). A concept of memory using a common control gate and each layer as a bit lines was early mentioned in [Ernst 2008 IEDM] (Figure 1.39b&c). It was sustained by the idea that the number of vertically stacked channels is almost unlimited [Hartmann 2008 ECS] (Figure 1.39d). By using selective epitaxy growth (SEG) and appropriate lithography masks, the number of vertically stacked channels can be locally tuned – and therefore the device drive current – bringing even more flexibility in the SRAM stability and density is therefore improved according to [Thomas 2008]. Concerning the variability, the use of intrinsic channels removes any random dopant fluctuation issues and channel thickness is precisely controlled by epitaxy.

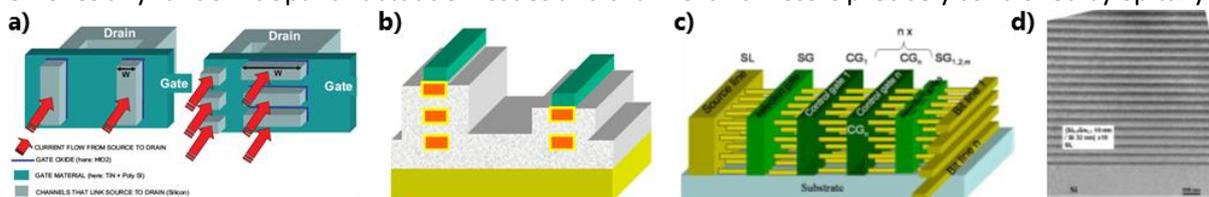


Figure 1.39 – (a) FinFET design limitations are not present in stacked NWs since NW width is tunable [Ernst 2008 ICICDT] so as the number of vertically stacked channels [Thomas 2008] (b). (c) A concept of stacked NW matrix for memory in [Ernst 2008 IEDM] and (d) TEM cross-section of 19 period of 19 nm thick SiGe and 32 nm Si layers [Hartmann 2008].

## Internal spacers

The volume of spacer material in between the stacked NWs is referred to as internal spacers (Figure 1.40). They were found necessary to decrease parasitic capacitances in [LimT 2009] and in [Huguenin 2011 ESSDERC]. Inner spacers were realized in [Shenoy 2004] by SiGe selective oxidation occurring faster than the Si one and by playing with anisotropic etch of SiN spacers in [Bernard 2009 EDL] (Figure 1.40). In the former, after the patterning of the active area, a partial selective etch of SiGe is realized. The cavities formed are then filled when depositing a conformal layer of SiN spacer. An “optimized anisotropic/isotropic etch sequence” of the SiN is then realized so the aforementioned cavities remain filled while the channels edges remain accessible for a merging epitaxy

of the S/D. An AFM 3D technique was developed to monitor the cavity depth [Foucher 2008 SPIE] which also defines the internal spacer thickness. Remote plasma (RP) and in situ inductively coupled plasma (ICP) processes were compared for controlling the SiGe recess [Barnola 2008 ECS]. RP process was sensitive to loading effects leading to unequal etch rate depending on the distance from the substrate and ICP was finally preferable.

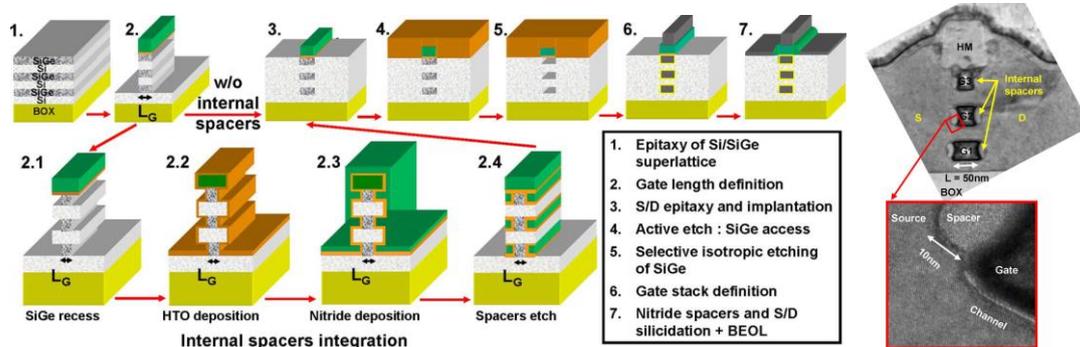


Figure 1.40 – MCFET fabrication process featuring internal SiN spacers [Bernard 2009 EDL].

The introduction of the SiN spacer resulted in -32% reduction in gate-to-drain capacitance (Figure 1.41a) and in a decrease of -39% in the intrinsic CV/I delay (Figure 1.41b). Although, the series resistances were increased due to lightly doped drain (LDD) resistivity under the internal spacers [LimT 2009], the devices presented a drive current of 2.33 mA/ $\mu\text{m}$  (NMOS) / 1.52 mA/ $\mu\text{m}$  (PMOS) and ultralow  $I_{\text{OFF}}$  currents compatible with LSTP ITRS requirements: 27 pA/ $\mu\text{m}$  (NMOS) / 38 pA/ $\mu\text{m}$  (PMOS). The resistance could still be improved by further junction engineering.

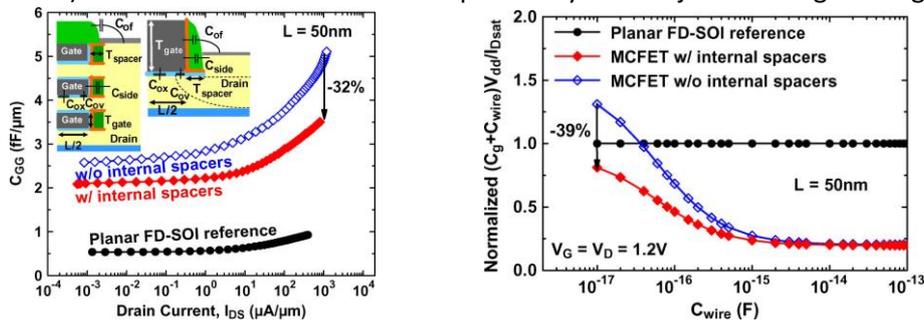


Figure 1.41 – (a) Reduction in gate-to-drain parasitic capacitance ( $C_{GG}$ ) due to the introduction of internal spacers and (b) the effects on intrinsic CV/I delay with  $C_{\text{wire}}$  the interconnection capacitance.

## Hydrogen Silsesquioxane (HSQ)

Flowable oxides such as hydrogen silsesquioxane (HSQ) can be used as negative tone photoresists. Once exposed to an electron beam (ebeam) or an extreme ultraviolet light (EUV), the “cage-like” structure changes into a “network-like” structure forming an oxide  $\text{SiO}_x$  [LiouHC 1998]. Unexposed resist can be developed using TMAH solution. A thermal treatment may also be applied to enhance the densification of the remaining oxide. One of the most interesting properties of ebeam and EUV is that silicon is transparent for these sources. Consequently, the resist can be used to realize self-aligned features through silicon layers such as stacked NWs or nanosheets as pictured in Figure 1.42. It is therefore possible to realize either oxide trenches for a damascene process, or sacrificial gates for a damascene and gate-last integration. This idea was patented [US20050037603] and used for the fabrication of self-aligned localized SOI devices and self-aligned DG [Wacquez 2006 SSDM]. TEM images reproduced in Figure 1.42 show 5 nm thin silicon nanoplate channels with self-aligned oxide trenches [Monfray 2010 IEDM], [Coquand 2013 ECST], [Coquand 2013 VLSI] or sacrificial gates.

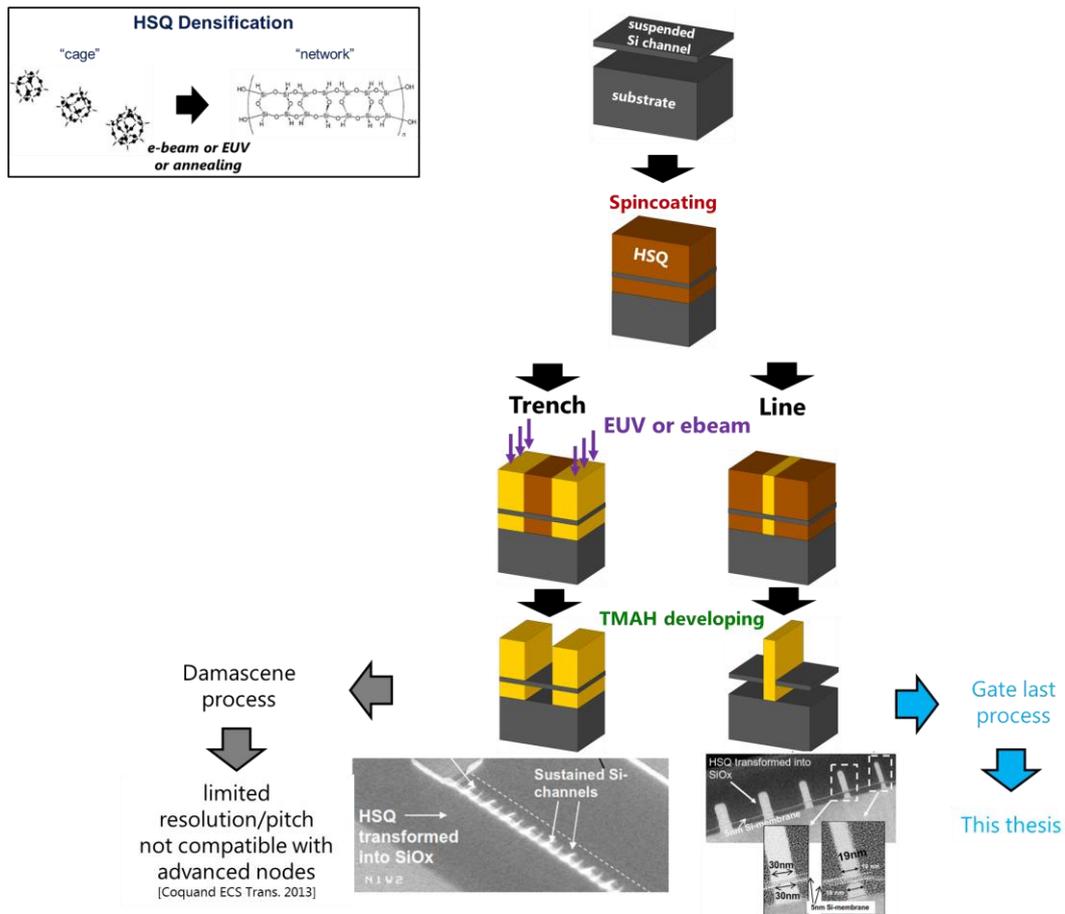


Figure 1.42 - HSQ self-aligned features exposed through silicon.

First GAA NWFETs realized from HSQ trenches were reported in [Coquand 2013 VLSI]. Process flow and structural images are provided in Figure 1.43. Once the trench is realized, the HKMG stack is deposited and cleared by CMP. The HSQ oxide around the self-aligned gate is then removed so the spacers and SD can be built around. Yet the gate length is limited by the trench minimal CD achievable which is 30 nm [Coquand 2013 ECS]. Even if gate trimming can be performed, this would prevent to meet the requirements in terms of patterning density. This is the reason why this thesis work focuses on the patterning of HSQ sacrificial gates for a gate-last integration (§3.1.2, §3.6, §0).

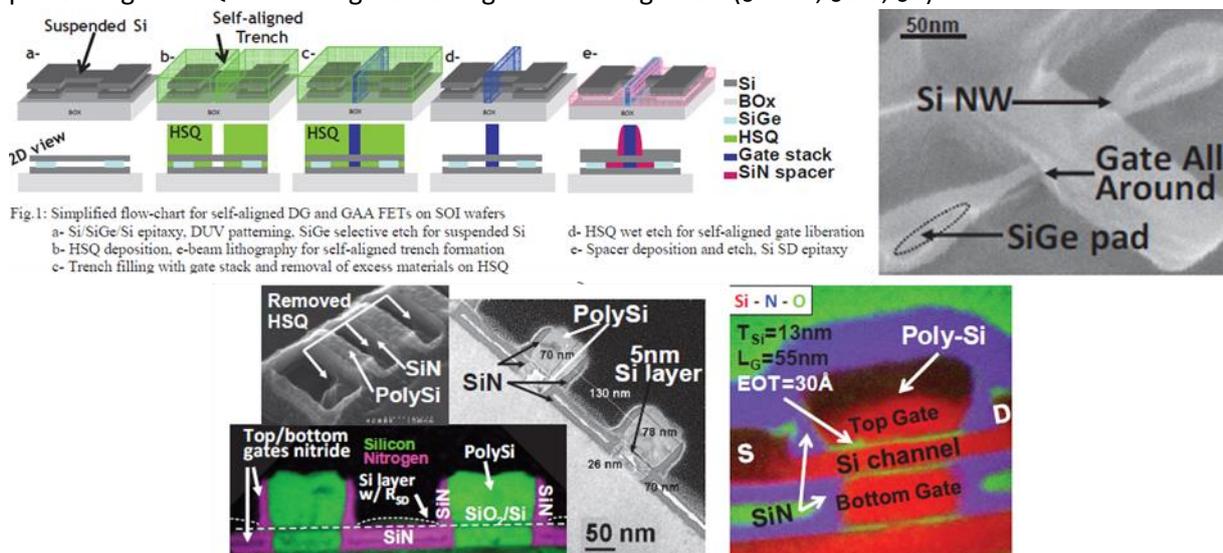


Figure 1.43 – GAA NW FET process featuring the use of HSQ trenches issued from [Coquand 2013 VLSI].

### 1.3.5. Conclusion and thesis proposal

#### Conclusions

The first part of this chapter (§1.1) consisted in providing an insight of multi-gate device physics. Original expectations in adding one or several gates to conventional CMOS were first introduced to improve electrostatic control (§1.1.1). With the apparition of the first double gates, device physics research got interested in volume inversion expecting an increase of carrier mobility in confined structures (§1.1.2). However, carrier transport in multi-gate FETs turned out to be much more complex than in typical bulk and volume inversion does not hinder completely the effect of surface interactions (§1.1.3).

Currently, manufactured horizontal double gate technologies consist of FDSOI (§1.2.1). The main advantage is the asymmetric back gate polarization which can be used to dynamically boost either the performances (forward back bias) or to lower the power consumption (reverse back bias). Moreover, FDSOI announced low cost process flow contributes to its attractiveness, as compared to the significantly more complex one of FinFET.

Driven by the electrostatics improvements and the potential of volume inversion, many other advances were achieved concerning the fabrication of symmetric double gate devices (§1.2.2) and SON (§1.2.3). Although none of them reached an industrial maturity, the experience accumulated during these developments provides a useful roadmap on the viability of each technology. For example, the selective removal of SiGe process developed for SON technology can be adapted for the critical step of forming the suspended silicon nanowire channels in SNWFETs (§1.3.4).

Vertical double-gate or FinFET technology (§1.2.4) on the other hand offers the best device compactness at the price of increased access resistance and parasitic capacitances. In the beginning of 2017, the question of FinFET scaling remains crucial for the sub-7 nm node technologies and below.

Ultimately, trigate,  $\Omega$ -gate and gate-all-around devices have been considered as the optimal multi-gate architecture that may substitute to current FinFETs for the end of the CMOS roadmap in terms of electrostatic control and because of their similar fabrication process (§1.3.1).

Tri-gates nanowire devices with various dimensions down to 5 nm were fabricated in order to study carrier transport in such devices. The impact of channel orientations and channel strain – which was induced by raised source and drain – on carrier mobility and consequently on device performances was measured (§1.3.2). It was shown that the usual surface conduction model is no longer reliable once the NW dimensions are reduced in the 10 nm range and below. Hence, the influence of quantum confinement must be taken into account.

Similarly as with FinFET technology, NWFET output current can be improved by adding several channels in parallel per transistor. As device compacity is of great concern, a multiple patterning technique was developed to increase the number of parallel nanowires (§1.3.2). The obtained  $\Omega$ -gate nanowire devices had 35 nm channel pitch and presented with good subthreshold behavior as expected in such a structure along with good performances considering the absence of strain engineering on this batch.

In the same spirit, transistor output current can be further increased by stacking several nanowires in the vertical direction. As compared to the horizontal multi-finger devices, this improvement does not cost any extra wafer surface. As a result, SNWFETs combine both great advantages of having excellent performances inherited from nanowire geometry and of being extremely compact. The various integrations considered in the past (§1.3.4) revealed common points in the fabrication of SNWFETs such as the use of sacrificial silicon germanium (SiGe) layers to build the NW stacks. The need for an internal spacer between the vertically stacked nanowires to isolate the gate from the source and drain

has been identified. Some techniques consisted in using sacrificial oxidation of SiGe, while others introduced with cavities carved into sacrificial SiGe or simply relied on gate oxide and high-k to perform the insulation function. An interesting alternative involving Hydrogen Silsesquioxane (HSQ) non-organic EUV photoresist and electron beam (ebeam) resist was also investigated. Since the silicon from which are made the stacked NW channels does not hinder EUV wavelengths, this material was used to realize vertical self-aligned features in damascene integrations of SON devices and of SNWFETs. The fact that HSQ can be crosslinked with electron beam lithography is an important advantage as this allows working with more commonly available tools other than EUV steppers.

## Thesis proposal

Although SNWFETs have been successfully demonstrated in the past, modern technologies require the use of high-k metal gate (HKMG). Processes involving the use of high-k such as HfO<sub>2</sub> are not compatible with the thermal budget of source and drain fabrication. The risk of equivalent oxide thickness (EOT) regrowth due to oxygen scavenging is significant even in the presence of a good barrier. The need of a gate-last integration approach has therefore risen. Polysilicon sacrificial gate is usually patterned and replaced in the final stages – after the source and drain epitaxy and the dopant activation anneal – with the final HKMG. Even if low temperature processes are currently developed especially for monolithic applications such as LETI Coolcube™ technology [2015 Pasini VLSI], [2016 Brunet VLSI], a gate-last integration approach provides several other advantages such as enhancing the impact of stressors (the contact etch stop layers (CESL) and the raised source and drains) and allows threshold voltage tuning by varying device gate workfunctions [Veloso 2008], [Veloso 2011].

Subsequently, this thesis intends to provide some insight into modern SNWFET technology. The following chapter presents TCAD simulations performed to evaluate the potential of SNWFETs (§2). After describing the models used in this work (§2.1), a benchmark of SNWFET against FinFET technology is presented (§2.2). The objective is to determine the conditions for which the NW based transistors are able to compete with FinFETs. The last part of this chapter shows the necessity of implementing internal spacers to reduce parasitic capacitances (§2.3).

In the light of these results, and based on previous knowledge developed on 200 mm tools in LETI, SNWFET-specific adaptations to LETI gate-last integration of FinFETs in 300 mm line were made. The first part of the third chapter (§3) consists in evaluating the different options available and their feasibility (§3.1). Two approaches were finally selected: a first one for its close proximity with existing FinFET integration process and the possible implementation of aligned internal spacers (§3.1.1) and a second one based on HSQ sacrificial gates providing self-aligned gates and self-aligned internal spacers (§3.1.2). The chapter therefore enumerates the main process developments realized for one or both integration routes with performance evaluation and perspectives (§3.2 to §3.7).

Finally, the fourth chapter provides electrical results obtained on SNWFETs (§4.1). A comparison of the two alternative integrations based on polysilicon sacrificial gate or based on HSQ is done (§4.2). This last chapter concludes with various proposals of new integration concepts and perspectives for the stacked nanowire technology (§4.3).

*Although it is impossible to predict what kind of electronic gadgets we will be carrying with us in 20 years, we can be sure that the transistors in them will be tiny multigate nanowire devices.  
– Isabelle Ferain, Cynthia Colinge, Jean Pierre Colinge, (Nature 2011)*

## 2. Benchmarking Stacked Nanowires Technologies with FinFET

The advantages of multi-gate architectures such as nanowire FETs (NWFETs) and stacked nanowire FETs (SNWFETs) have been developed in Chapter §1. However, the capability of SNWFETs to overcome FinFETs performance in the specific context of advanced CMOS technologies still need to be verified. Subsequently in this second chapter, preliminary to any cleanroom development of devices, simulations are performed with 7 nm node design rules. Technology Computer Aided Design (TCAD) is used for the optimization of NW geometries in terms of electrical characteristics and process flow. After describing the models used in this work (§2.1), this chapter assesses the electrostatics of various FinFETs and SNWFETs (§2.2). A comparison of SNWFETs against FinFET technology is then made (§2.3). Finally, the need for internal spacers in between the stacked nanowires is described in the last section (§2.4). Hence, the purpose of the present chapter is to justify and to provide guidelines for the fabrication of stacked nanowire/nanosheet devices.

### 2.1. TCAD Model: Simulation Parameters and Extraction

Several levels of precision cohabit in microelectronic simulations (Figure 2.1). Advanced simulations target specific phenomena using highly precise approach such as band structure computation. A level of precision lower, the components and the technological processes simulations help predicting the devices performance with simplified algorithms and faster computation times. Finally, the compact modeling are dedicated to circuit evaluations involving a significantly higher number of devices. All of these domains complement each other, not to mention experimental characterization which is essential to build a global comprehension of the physics behind the devices and complex architectures. TCAD Sentaurus SDE tool [Sentaurus 2013] is therefore the most efficient way to set up an exhaustive analysis of FinFET and SNWFET. In the following, the key design rules and devices models that fits projections for the 7 nm node technology are first presented (§2.1.1). Transistor intrinsic delay is then defined in §2.1.2 as this value can be used to compare performances in between the different devices. The definition includes an equivalent capacitance model which is therefore simplified in the third section (§2.1.3).

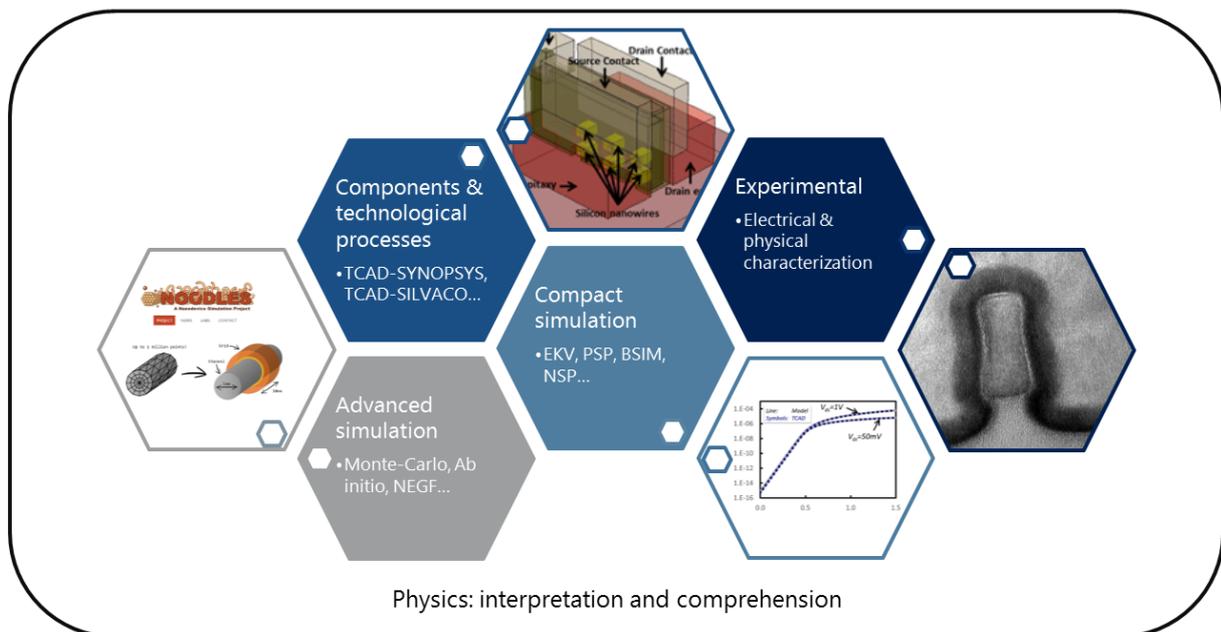
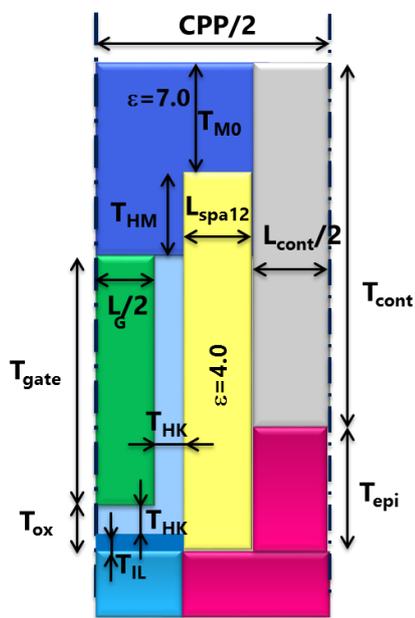


Figure 2.1 - Simulation in microelectronics.

### 2.1.1. TCAD model

#### Geometric parameters

Main geometric parameters are reported in Figure 2.2 in a cross section along with a table. The prediction has been defined in CEA-LETI and based on internal knowledge and state-of-the-art material and patterning abilities according also to the 10nm-node definition from ITRS 2013, [Lacord 2012 TED]. The contacted polysilicon pitch (CPP) defines the pitch between two neighboring gates and  $L_G$  is the gate length. The equivalent oxide thickness (EOT) is calculated from the formulae recalled in the inset and considers the presence of a high-k layer –  $\text{HfO}_2$  for instance – above the chemically oxidized inter layer (IL): their thickness and dielectric permittivity are respectively  $T_{\text{HK}}$ ,  $\epsilon_{\text{HK}}$ ,  $T_{\text{IL}}$  and  $\epsilon_{\text{IL}}$ . The gate spacers are  $L_{\text{spa}12}$  large and isolate the gate over its entire height  $T_{\text{gate}}$ . The raised source and drain (RSD) thickness is  $T_{\text{epi}}$  and the width and height of the contact above are respectively  $L_{\text{cont}}$  and  $T_{\text{cont}}$ . Finally, a hard mask (HM) isolating the gate from the source and drain contacts which thickness is  $T_{\text{M}0}$ .



	nfet	pfet
CPP	46nm	
$L_G$	16nm	
EOT	0.67nm	0.67nm
$T_{\text{HK}}, \epsilon_{\text{HK}}$	1.8nm, 25	1.8nm, 25
$T_{\text{IL}}, \epsilon_{\text{IL}}$	0.4nm, 4	0.4nm, 4
$L_{\text{spa}12}$	4.2nm	4.2nm
$T_{\text{gate}}$	25nm	
$T_{\text{epi}}$	20nm	20nm
$L_{\text{cont}}$	18nm	
$T_{\text{cont}}$	50nm	
$T_{\text{M}0}$	20nm	

$$T_{\text{ox}} = T_{\text{HK}} + T_{\text{IL}}$$

$$T_{\text{HM}} = T_{\text{cont}} + T_{\text{epi}} - T_{\text{M}0} - T_{\text{gate}} - T_{\text{ox}}$$

Figure 2.2 - 7nm-node device description as defined by LETI.

Figure 2.3 represents an example of FinFET with three parallel fins. The number of parallel fins is tunable as well as their dimensions ( $H_{\text{Fin}}$  and  $W$  the height and width respectively) and the fin pitch (FP).

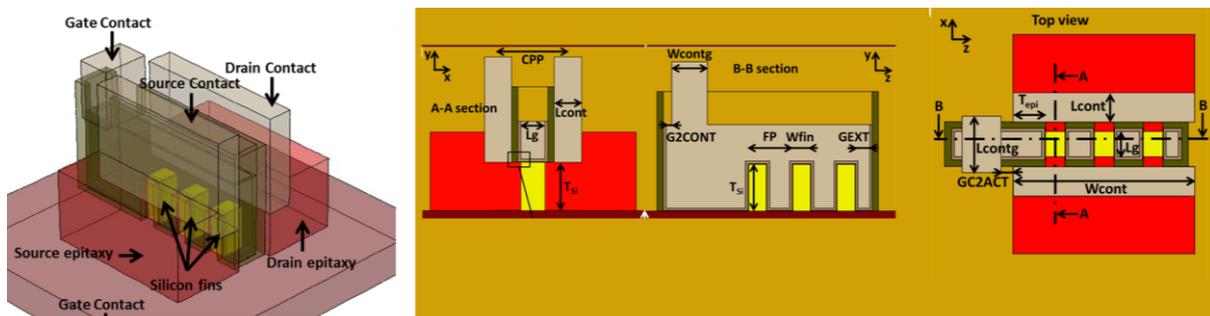


Figure 2.3 - TCAD device description for FinFET architecture [Lacord 2016 TED].

Figure 2.4 represents a SNWFET featuring three stacks of NWs with a specific “mixed” configuration with one gate-all-around (GAA) suspended NW on top of a trigate NW laying on the buried oxide (BOX). The number of parallel stacks is tunable as well as the number of NW in each stack. The gate configuration can be either fully composed of GAA or alternatively composed of a trigate and one or several GAAs. A vertical space  $H_{\text{space}} = 8 \text{ nm}$  is kept constant in between the NWs unless mentioned otherwise. The value is in accordance with cleanroom developments and the thickness of the HKMG layers (§3).

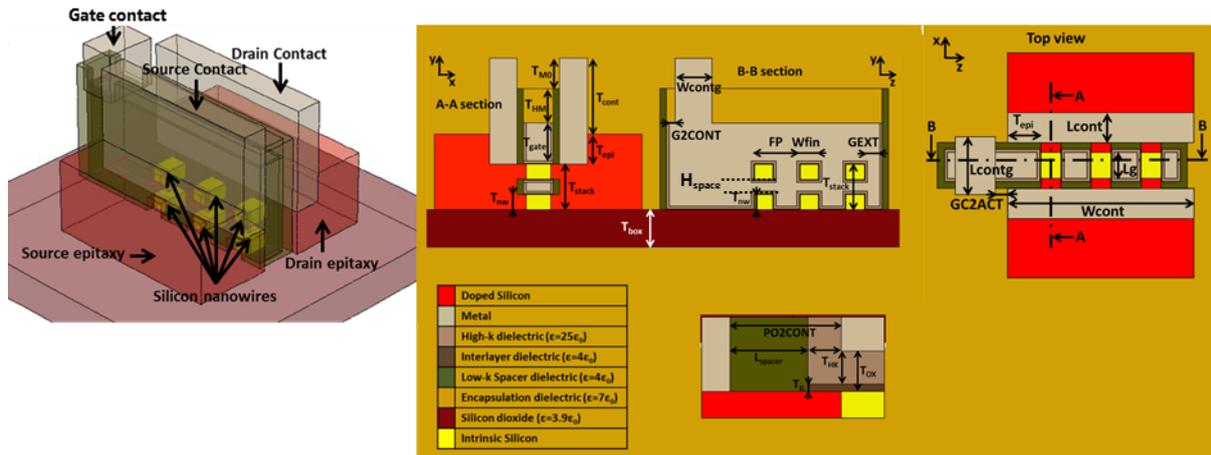


Figure 2.4 - TCAD device description for stacked-NWs architecture [Lacord 2016 TED].

## Doping levels

Concerning the doping levels, intrinsic silicon channels only are used for the simulations. Source and drain are heavily doped with  $10^{23} \text{ atoms/cm}^3$  and can be considered metallic – low access resistance – which emphasizes the junction and channel intrinsic resistances. Vertical junction lines are located under the spacer at  $L_{\text{spacer}}/2$ . As explained in the third chapter (§3), RSD are in-situ doped. The activation anneal that follows distributes the dopants from the RSD uniform reservoirs to the intrinsic channel following the Gaussian distribution pictured in Figure 2.5 according to Fick’s diffusion law.

GAA structure confines the electric field within the channel: there is no need to simulate more than one NW in this configuration and the total output current can be obtained by multiplying by the number of channels. In other words, the normalized current does not depend on the number of channels, only on their geometry. This effect was verified with a few experiments on trigate devices and FinFETs. This helps saving precious simulation time. This is a consequence of having uniform and very high doping of the S/D region, allowing to neglect the problematic of S/D access resistance and to focus on the intrinsic architectures themselves. In future work, models including doping non-uniformity and more realistic concentrations will have to be added. However, it is possible to imagine that SNWFET technology could benefit from the same state-of-the-art than FinFETs as their fabrication process and their dimensions are very close (§3).

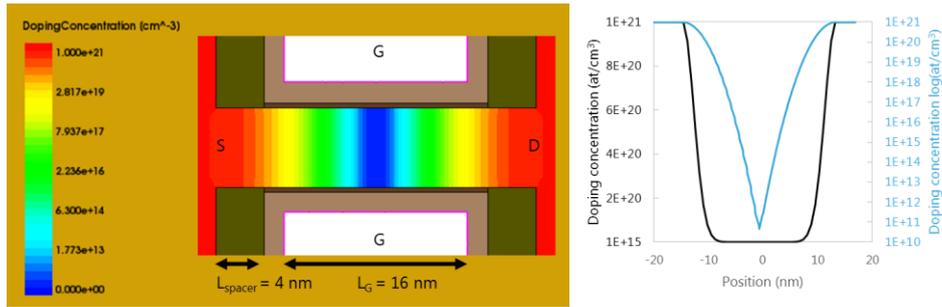


Figure 2.5 - Gaussian distribution of dopants in the channel: source-drain longitudinal-section of a GAA nanowire device with  $L_G = 16$  nm and  $L_{Spacer} = 4.2$  nm.

## Electrostatic and carrier transport models

The present chapter focuses on the electrostatic behavior of FinFETs and SNWFETs which dominates their performance. Carrier transport is described with a Drift-Diffusion model based on Boltzmann semi-classical transport. A constant mobility of  $100 \text{ cm}^2/\text{V}\cdot\text{s}$  and a saturation velocity of  $1.07 \times 10^7 \text{ cm/s}$  are set along with a supply voltage  $V_{DD} = 0.7 \text{ V}$ . As a consequence of this carrier transport model, no quantitative projection can be realized, especially concerning the above threshold current. Subsequently, the results presented in this chapter evidence mostly the differences in electrostatics under threshold.

Quantum confinement effects in such narrow structures must be considered. The density-gradient model proposed by [Ancona 1989] includes this effect inside a Drift-Diffusion approach thanks to a calibration of the parameters previously obtained in [Pons 2013]. The computation of Poisson-Shrodinger is then avoided and quantum effects are simulated through the charge density thanks to a correction of the potential. In the present conditions, Pons et al. calibration is valid down to  $W = H_{NW} = 6 \text{ nm}$ . Consequently, the simulated channels have been restricted to fin widths larger than  $7 \text{ nm}$  and NW thicknesses higher than  $6.33 \text{ nm}$ . A channel cross-section is presented in Figure 2.6 where the difference in between a classical model and a density gradient model can be observed. The quantum correction shifts the pic of carrier concentration from the interface by a distance so called the dark space (DS).

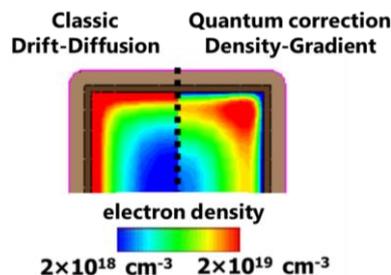


Figure 2.6 - Improvements brought by density-gradient correction: the electron density peak is no longer at the interface channel-insulator.

### 2.1.2. Intrinsic delay approximation

The intrinsic delay can be approximated using the effective current  $I_{eff}$  in the expression (Eq. 2-1) according to [Wei 2011 TED].  $I_{eff}$  is defined by equations (Eq. 2-2) to (Eq. 2-4). In the present case, the extraction is realized at  $+V_{DD} = 0.7$  V from the gate voltage  $V_{G0}$  required to reach the fixed off state current  $I_{OFF} = 100$  nA/ $\mu$ m (for high performance applications: this value has been defined in ITRS 2013). This is intended to suppress the effect of threshold voltage variation in between the different architectures in comparison with an extraction at fixed gate voltage.

$$\tau = \frac{C_{eq} \cdot V_{DD}}{I_{eff}} \quad (\text{Eq. 2-1})$$

$$I_{eff} = \frac{I_H + I_L}{2} \quad (\text{Eq. 2-2})$$

$$I_H = I_{DS}(V_G = V_{DD} + V_{G0}, V_D = \frac{V_{DD}}{2}) \quad (\text{Eq. 2-3})$$

$$I_L = I_{DS}(V_G = \frac{V_{DD}}{2} + V_{G0}, V_D = V_{DD}) \quad (\text{Eq. 2-4})$$

Figure 2.7 illustrates the extraction of  $I_{eff}$  according to the equations (Eq. 2-2) to (Eq. 2-4).  $V_{G0}$  is extracted on the  $I_D$ - $V_G$  curve at  $V_D = V_{DD} = 0.7$  V, and consequently, the off current  $I_{OFF, VD=VDD/2}$  considered for the extraction of  $I_H$  in the  $I_D$ - $V_G$  plot at  $V_D = V_{DD}/2$  is lower than 100 nA/ $\mu$ m depending on DIBL.

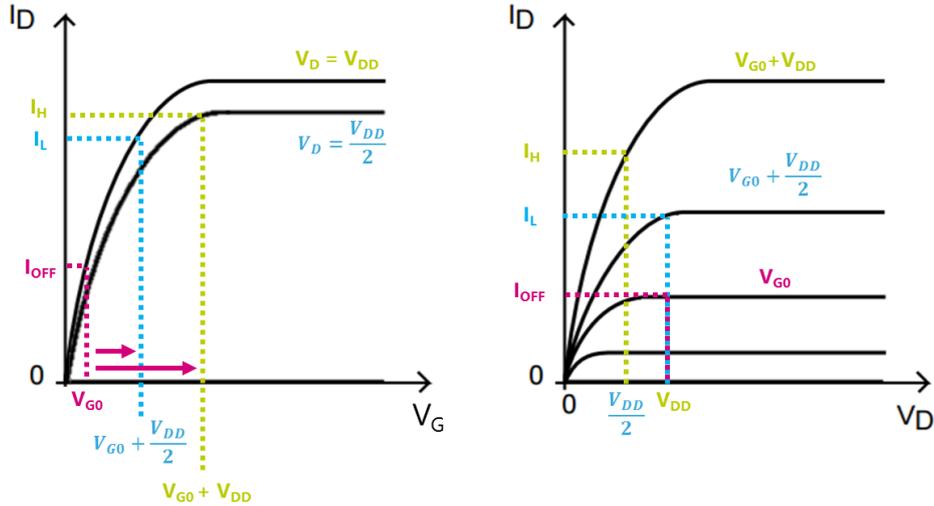


Figure 2.7 -  $I_D$ - $V_G$  plots illustrating effective current extraction.

### 2.1.3. Parasitic capacitances – inverter equivalent capacitance

The equivalent capacitance  $C_{eq}$  for an inverter as defined in [Wei 2011 TED] is reported in equations (Eq. 2-5) to (Eq. 2-7) with  $M = 2$  the Miller Effect in an inverter and  $FO = 3$  the fan-out number. Therefore,  $C_{eq}$  is a combination of all the parasitic capacitances illustrated in Figure 2.8.

$$C_{eq} = M \cdot C_{gd0} + C_j + \left( \frac{1}{4} C_{goff} + \frac{3}{4} \cdot C_{gon} \right) \cdot FO \quad (Eq. 2-5)$$

$$C_{goff} = C_{gboff} + 2 \cdot C_{ov} + 2 \cdot C_{if} + 2 \cdot C_{of} + 2 \cdot C_{pcca} + 2 \cdot C_{corner} \quad (Eq. 2-6)$$

$$C_{gon} = C_{gc} + 2 \cdot C_{ov} + 2 \cdot C_{of} + 2 \cdot C_{pcca} + 2 \cdot C_{corner} \quad (Eq. 2-7)$$

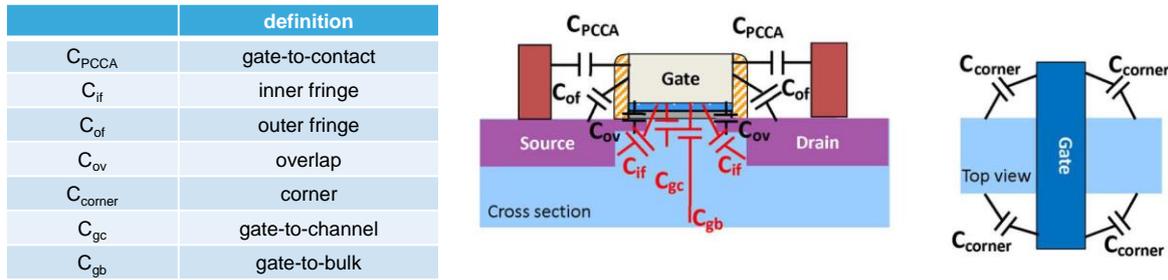


Figure 2.8 - Illustration of the different parasitic capacitances present in a planar bulk transistor

Gate-to-source  $C_{gs0}$  and gate-to-drain  $C_{gd0}$  capacitances being dominants in the off state capacitances, the approximation of (Eq. 2-8) for an underlapped channel ( $C_{ov} = 0$  fF) is justified.

$$C_{goff} = C_{gg0} \approx 2 \cdot C_{gd0} \quad (Eq. 2-8)$$

Once the transistor is on, the inversion capacitance noted  $C_{inv}$  or  $C_{gc}$  and gate-to-source  $C_{gs}$  and drain  $C_{gd}$  capacitances dominate as the inner-fringe capacitances become shielded by the charge of the inversion layer. As a result, and if the inversion capacitance is approximated by a planar capacitor, the expression of the  $C_{g, on}$  capacitance is used (Eq. 2-9).

$$C_{gon} = C_{gc} = C_{inv} = \frac{\epsilon_{SiO_2} \cdot S}{t_{inv}} = \frac{\epsilon_{SiO_2} \cdot L_g \cdot W_{eff}}{t_{inv}} \quad (Eq. 2-9)$$

The inversion layer thickness  $t_{inv}$  includes the equivalent oxide thickness (EOT) and the dark space (DS) and its expression is given in (Eq. 2-10). In first approximation for  $t_{inv}$ , the DS can remain constant: 0.4nm for NMOS and 0.6nm for PMOS.

$$t_{inv} = EOT + \frac{\epsilon_{SiO_2}}{\epsilon_{Si}} \cdot DS \quad (Eq. 2-10)$$

Finally,  $C_{eq}$  can be defined as:

$$C_{eq} = (M + 2 \times FO) \times C_{gd0} + \frac{3}{4} \times \frac{\epsilon_{SiO_2} L_g W_{eff}}{t_{inv}} \times FO + \frac{C_{BE}}{2} \quad (Eq. 2-11)$$

with  $M = 2$  the coefficient for Miller effect,  $FO = 3$  the electric fan-out,  $W_{\text{eff}}$  the effective width – or device perimeter –  $t_{\text{inv}}$  the inversion layer thickness and  $C_{\text{gd}0}$  the gate-to-drain parasitic capacitance extracted at  $V_G = 0 \text{ V}$  and  $V_D = 0 \text{ V}$ . Another capacitance is added to take into account the effect of the back-end:  $C_{\text{BE}} = 2 \text{ fF}$  is a common value used internally for the back-end capacitance.

This derivation simplifies the computation of the intrinsic delay since only the  $0 \text{ V}$  gate-to-drain parasitic capacitance needs to be extracted from the simulation and not the entire C-V plot. This is in accordance with the level of precision needed for this preliminary study as well as with the basic mobility model employed.

## 2.2. Electrostatics of 3D-architectures

One way to increase the drive current is to increase transistor effective width. This translates for FinFETs and SNWFETs by an increase of channel height or width. Subsequently in the following subchapter, electrostatic behavior of FinFET and NW devices having different channel geometries and configurations is analyzed.

### 2.2.1. Subthreshold behavior

As discussed in §1.1, the main interests of 3D architectures is the gain in electric width – or effective width  $W_{\text{Eff}}$  – per device area – or footprint – which translates in much more compact designs [WuSY 2016 IEDM]. Besides, multi-gates devices also bring a substantial improvement in the electrostatic control over the channel – which justifies all the developments from bulk transistors up to FDSOI, FinFET and stacked NWs revised in the first chapter. This is evidenced through the values of the subthreshold slope (SS), the short channel effects (SCE) and the drain induced barrier lowering (DIBL). The effective width  $W_{\text{Eff}}$  can be enlarged by increasing the channel height and width. This is not without consequences on electrostatic control and the following subchapter intends to expose the impact of increasing  $W_{\text{Eff}}$  on electrostatic control and parasitic capacitances when playing with fin and NW dimensions.

Figure 2.9 shows the dependence of DIBL on fin height  $H_{\text{Fin}}$  for different gate lengths  $L_G$  and different fin widths  $W$ . In each case, the lowest DIBL is obtained for a tri-gate with near-to-one aspect-ratio ( $A/R$ ). As the fin height is increased,  $A/R$  increases so as DIBL. Once the  $A/R$  reach approximately three, the device exhibits a double gate behavior and DIBL is no longer increased with  $H_{\text{Fin}}$ . However, fin height is ultimately limited by the patterning capability (§1.2.4, §1.3.3). As expected, an increase of the gate length also provides a better electrostatic control. Targeting a DIBL of 60 mV/V at  $L_G = 16$  nm for the 7 nm-node, Figure 2.9 suggests the use of a fin narrower than 8 nm. This is in accordance with recent demonstrations of 10 nm and 7 nm node technologies based on FinFET [Hashemi 2016 VLSI], [WuSY 2016 IEDM], [XieR 2016 IEDM].

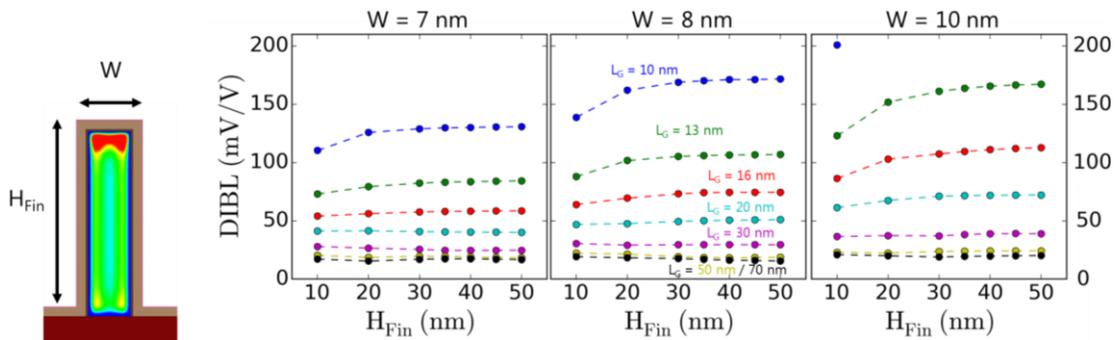


Figure 2.9 – DIBL in FinFETs as a function of fin height  $H_{\text{Fin}}$  for different gate lengths  $L_G$  and fin widths  $W$ .

Figure 2.10 shows the DIBL dependence of gate-all-around NW devices on NW width  $W$  for different gate lengths and NW thicknesses  $H_{\text{NW}}$ . DIBL increases with NW width and a saturation is reached once the sidewall gates – or more precisely the effect of corners (§1.3.1) – no longer have a significant impact on the overall current, the device being close from a double gate. Considering the target  $L_G = 16$  nm for the 7 nm node specifications and a DIBL of 60 mV/V, NW width is not limited as long as the NW thickness is kept below  $H_{\text{NW}} = 8$  nm.

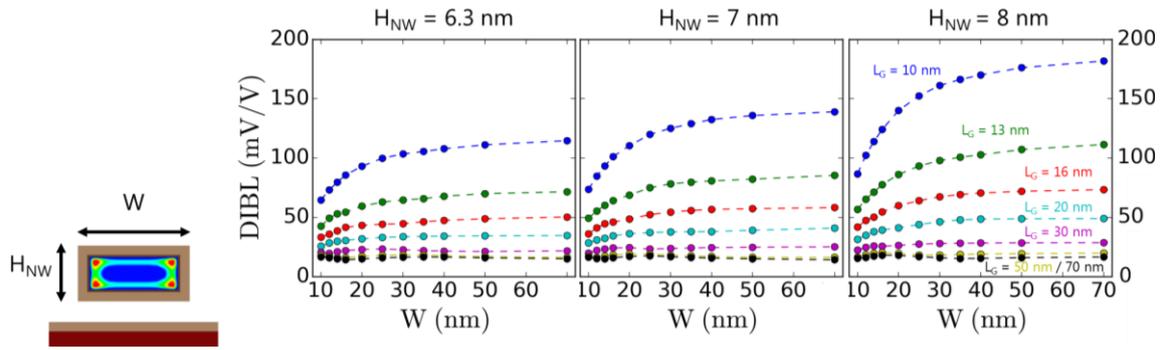


Figure 2.10 - DIBL as a function of NW width for different gate lengths and NW thicknesses for a single GAA structure.

For fabrication purposes, the mixed configurations of Figure 2.11 including a trigate may be required, the bottom NW laying on the BOX serving as a seed for S/D epitaxy (§3). In this case, DIBL increases significantly as NW width  $W$  is increased. This effect can be attenuated similarly as with FDSOI devices by decreasing the channel thickness. Adding GAA NW channels balances the impact of the trigate channel. Considering  $L_G = 16$  nm, and aiming a DIBL of 60 mV/V, NW width is therefore limited at  $W = 16$  nm in the case of the thinnest channel ( $H_{NW} = 6.3$  nm).

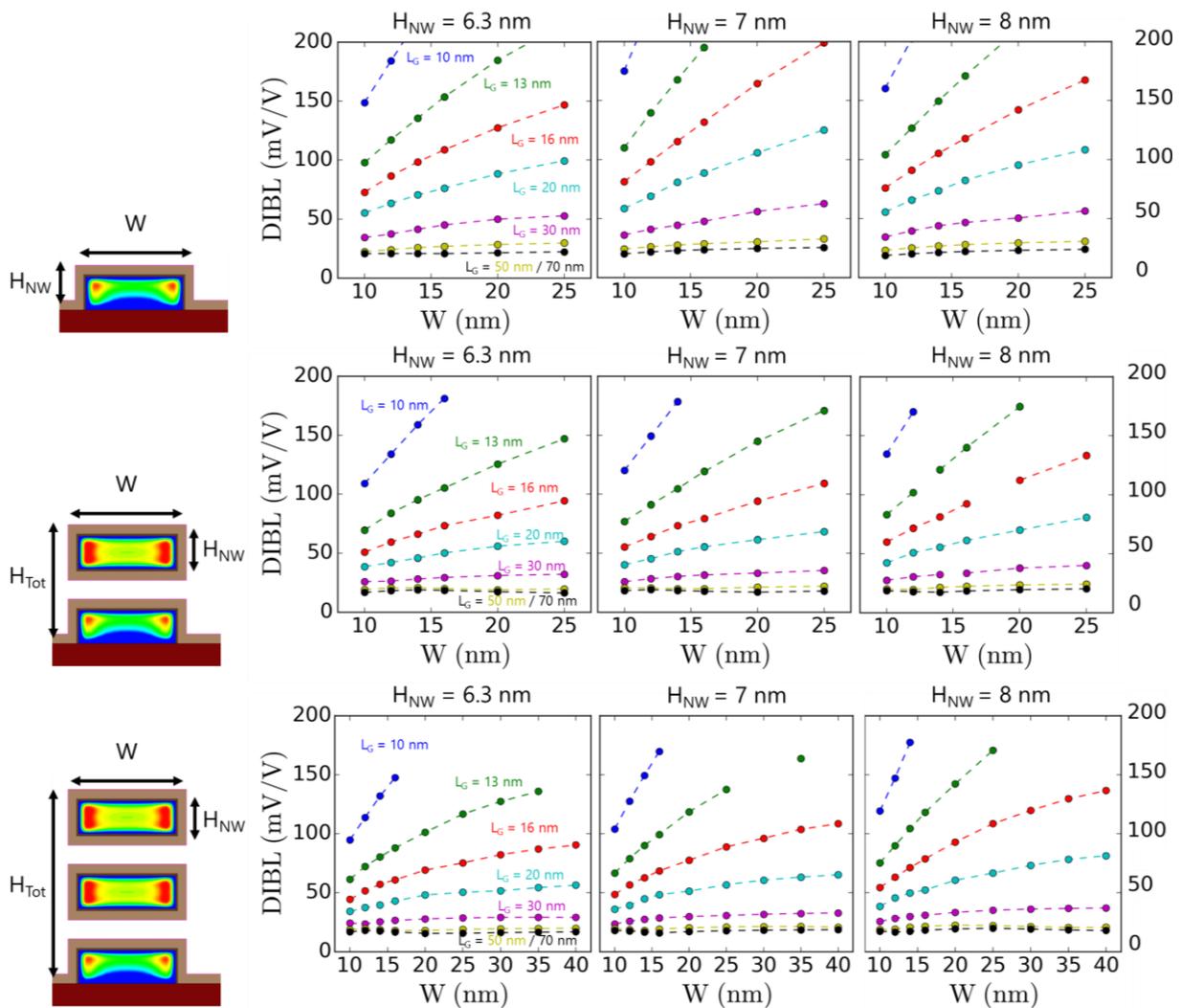


Figure 2.11 - DIBL as a function of NW width for different gate lengths and NW thicknesses: (a)  $H_{NW} = 6.3$  nm, (b)  $H_{NW} = 7$  nm and (c)  $H_{NW} = 8$  nm

For optimizing the bottom tri-gate behavior, a BOX over etch can be performed in order to obtain an  $\Omega$ -gate (§1.3.1). Figure 2.12 displays the advantages of such structure for different recess depths. However, as NW width is increased, the influence of the omega gate is less and less beneficial as the gate loses its control over the center part of the NW.

Besides, etch depth is limited on the longitudinal direction by the spacer width: by carving too deep under the NW, the risk is to shortcut the gate with the source and drain under the spacer – or even a lift-off of the whole structure (§3, §4.2). Another option is an increase of the doping concentration of this specific channel in order to deactivate it by an increase of its threshold voltage.

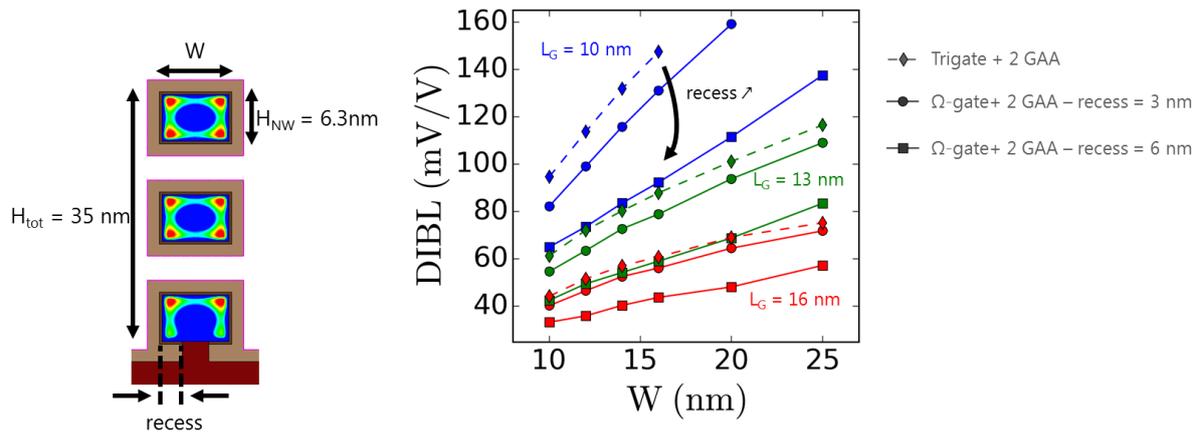


Figure 2.12 – Improvement of electrostatic control by the introduction of an  $\Omega$ -gate for the bottom tri-gate which translates into a decrease of DIBL.

Figure 2.13 compares the DIBL and the subthreshold slope of different MOSFET architectures. The potential of full GAA over the other architectures is confirmed even with large NWs. Besides, Figure 2.13c interestingly reveals the possibility to tune the threshold voltage  $V_T$  by varying the NW width. Only full GAA devices can entirely benefit from this effect since their subthreshold performances are moderately impacted by the variation of channel width.

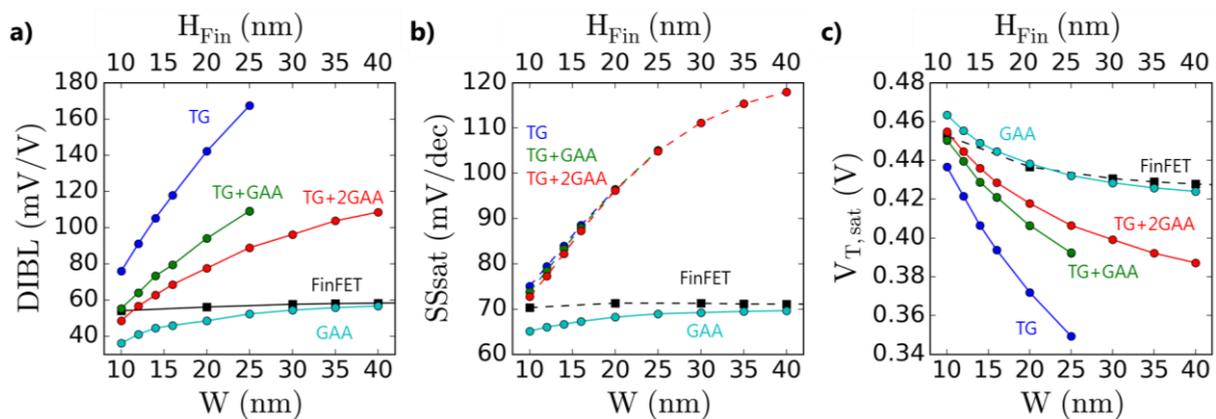


Figure 2.13 – (a) DIBL, (b) subthreshold slope and (c) threshold voltage comparison of FinFETs with only an increase of fin height  $H_{Fin}$  (top horizontal axis) and SNWFETs with only an increase of NW width  $W$  (bottom horizontal axis) at  $L_G = 16\text{nm}$  but with same critical dimensions ( $W_{Fin} = H_{NW} = 7\text{nm}$ ).

Figure 2.14 provides the effective width of FinFET and SNWFETs as a function of device footprint for a given technology ( $W_{\text{Fin}} = 7 \text{ nm}$  and fin pitch = 30nm). FinFET devices (square points on the graph) features one, two or three parallel fins with heights varying from 20 to 60 nm. They are compared with large NW devices or nanosheet (NS) having their width equal to their footprint (a single NW stack per device). The effective width of one, two or three suspended NW or NS is plotted as a function of  $W_{\text{NW}}$ . The Figure 2.14 gives the effective width enhancement that can be expected when switching from fins to NS within a given device footprint.

Considering the example of a space of 8 nm in between the different NW vertically stacked, the total height of a structure including three 7 nm thick NS is 45 nm. In a FinFET device composed of two 45 nm tall fins this would grant a +36% advantage in effective width to the SNWFET technology for the same footprint.

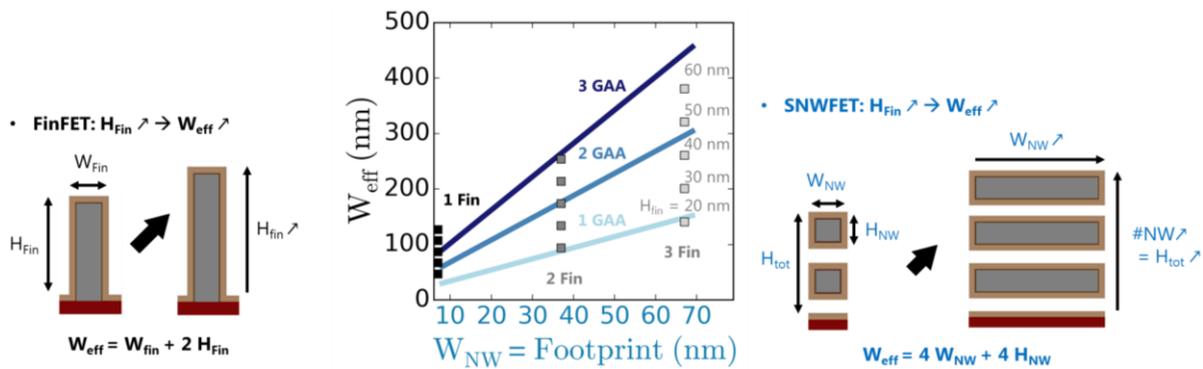


Figure 2.14 – The different ways to increase the effective width  $W_{\text{eff}}$  for SNWFETs and multi-fingers FinFETs for different fin heights and 1 to 3 NWs per stack (with  $H_{\text{NW}} = W_{\text{Fin}} = 7 \text{ nm}$  and 30 nm fin pitch patterning technology).

Thus, increasing NW width or fin height to enlarge effective width is an interesting option. However, the impact of parasitic capacitances still needs to be evaluated with the risk of cancelling any potential benefits of the  $W_{\text{eff}}$  increase.

### 2.2.2. Parasitic capacitances

As explained in the previous sub-chapter, gate-to-drain capacitance ( $C_{gd0}$ ) is the dominant parasitic capacitance involved in the transistor switching delay. The following part is focused on the impact of the geometry on parasitic capacitances.

If the entire  $I_D$ - $V_G$  plot was required for the previous extractions, the extraction of  $C_{gd0}$  only requires the simulations of the first step of the C-V plot which decrease significantly the computation time. The whole structures are always simulated with all the stacks and all the channels unlike in the previous section since the geometries and the surfaces at play have a real impact on parasitic capacitances.

Figure 2.15 displays the variation of  $C_{gd0}$  normalized by  $W_{eff}$  for every architecture. An increase of  $W_{eff}$  through  $H_{Fin}$  or  $W$  for FinFET and stacked NW respectively, reduces the normalized capacitance. Consequently,  $C_{gd0}$  can be expected to weight less in the intrinsic delay.

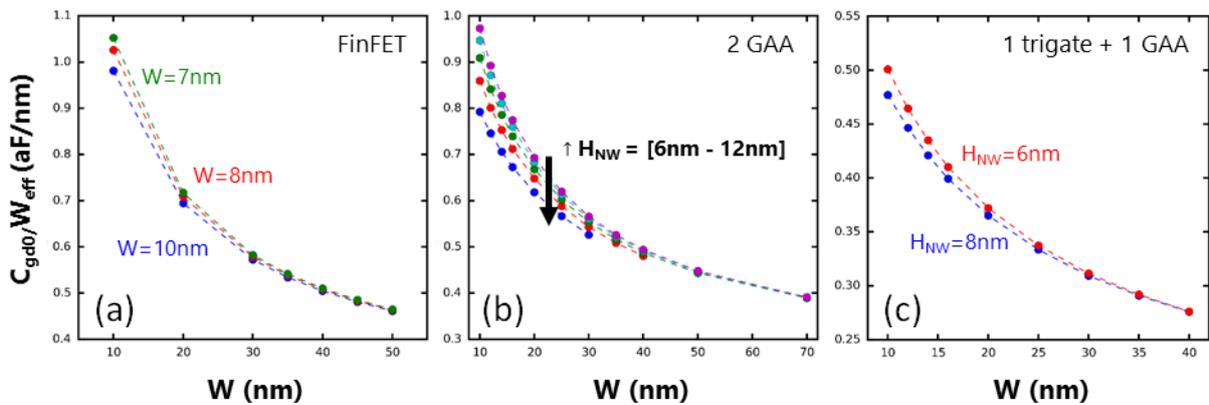


Figure 2.15 - Normalized gate-to-drain parasitic capacitance for (a) FinFET, (b) GAA NWFET and (c) mixed trigate and GAA NWFET as a function of fin width and height or NW width and thickness for  $L_G = 16$  nm.

Gate-to-drain capacitances of GAA NWFET have a linear behavior on a large panel of NW width as revealed in the example of Figure 2.16a. Hence, the values of the capacitances for more than three vertically stacked channels can be easily extrapolated. Figure 2.16b reveals that increasing the number of vertically stacked channels increases  $W_{eff}$  and likely contributes in reducing the impact of  $C_{gd0}$  on the intrinsic delay.

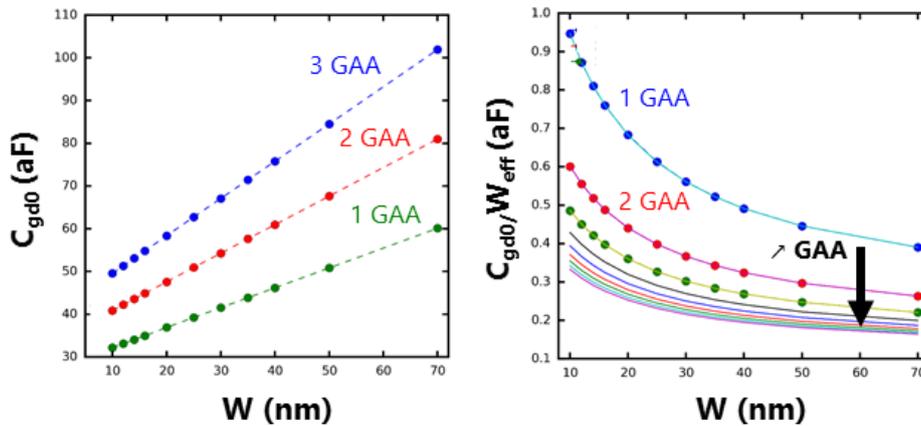


Figure 2.16 - (a) Linear curve fit of parasitic capacitances and (b) normalized parasitic capacitances with extrapolation more than three stacked GAA.

### 2.2.3. Conclusion

Finally, increasing the effective width  $W_{\text{eff}}$  for improving the drive current must be realized by an increase of fin height in the case of FinFET or by adding several parallel fins per transistor with a fin pitch FP. Indeed, increasing the fin width is not an option due to the degradation of the electrostatics. Similarly, in the case of SNWETs, the increase of  $W_{\text{eff}}$  is expected from enlarging  $W_{\text{NW}}$  and not from increasing  $H_{\text{NW}}$  in order to maintain a good immunity to SCE. Likewise, adding several channels in the stack or adding several stacks in parallel per transistor is also possible. In the special case of a mixed configuration of SNWFET including a tri-gate or an  $\Omega$ -gate laying on the BOX, the width is limited by the NW thickness.

Concerning the parasitic capacitances, all the architectures seem to benefit from the increase of  $W_{\text{eff}}$ .

Ultimately, large and thin stacked NWs or stacked nanosheets (SNSFETs) is the most interesting geometry when considering a replacement for the FinFET. They have the advantage of an excellent double gate-like electrostatic control and a higher effective width per footprint.

On this basis, the following sub-chapter suggests a set of recommendations for a proper benchmarking of both FinFET and SNWFET technologies.

### 2.3.Constant footprint and height comparison using TCAD simulation

If SNWFETs are considered as the main alternative to FinFET technology, it remains unclear if using the same technology constraints as for FinFET fabrication, the stacked NW architecture is able to overcome FinFET performances in the context of the 7 nm technology node and beyond. Besides, on one hand, the occupied space on the wafer – or footprint – is of great concern for the designers. On the other hand, the previous sub-chapter (§2.2) has shown stacked nanosheets (SNS) to provide a significant improvement of channel effective width; subsequently at the expense of a loss in device footprint. In the following, guidelines for accurate benchmarking of stacked NW and FinFET architectures are suggested including restrictions on device footprint (§2.3.1). Parasitic capacitances and effective current are extracted from TCAD simulations for both architectures to estimate the NMOS switching delay (§2.3.2). The last section concludes on the advantages of SNSFETs as presented in [Gaben 2015 SSDM.b].

#### 2.3.1. Comparison guidelines

Significant advances have been made in recent years in advanced patterning of FinFET (§1.2.4). Multiple patterning techniques has led to 40nm fin pitch (FP) with DUV [Basker 2010 VLSI] for FinFET and down to 35 nm NW pitch for NWs [Barnola 2014 SPIE], [Gaben 2015 SSDM2] (§1.3.2). Recently, several demonstrations of sub-30 nm fin pitch were realized with quadruple patterning for 7 nm technology [XieR IEDM 2016].

In the case of gate last integration of SNWFETs presented in this thesis (§3), silicon fins of the FinFET technology are replaced by Si/SiGe fins as illustrated in Figure 2.17a. The suspended silicon channels are then obtained after a selective etch of the SiGe sacrificial layers. Besides, an adaptation to the SNWFETs of the SIT technique presented in [Barnola 2014 SPIE] has led to 60 nm tall Si/SiGe fins in a FP = 40 nm pitch array (Figure 2.17b). Consequently, the fabrication of SNW can be reasonably expected to benefit from the same patterning advances as FinFET enabling SNW architectures having a total height  $H_{stack} = H_{Fin}$  and with a space between the stacks  $W_s = FP - W_{Fin}$  equal to the one in FinFETs.

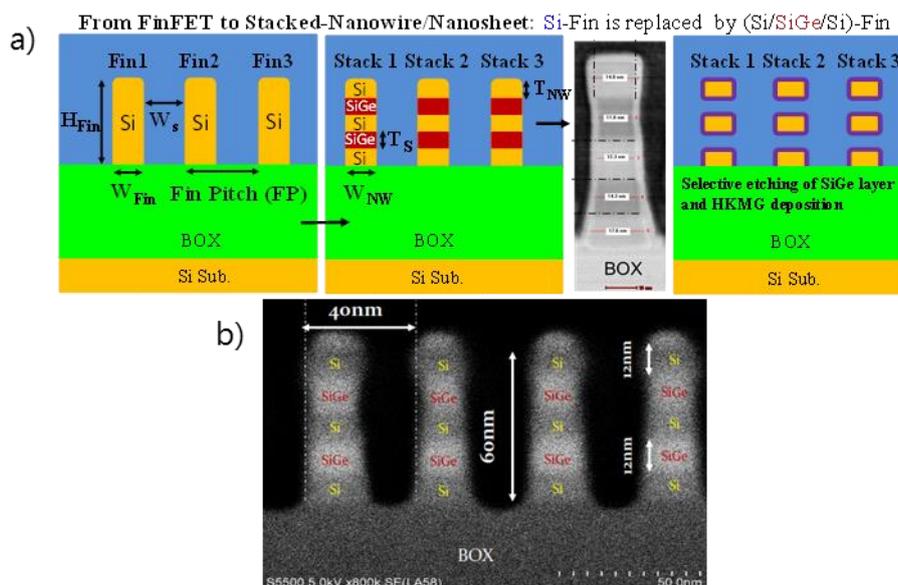


Figure 2.17 – (a) Process adapted from FinFET fabrication for stacked-NW patterning: Si Fins are replaced by (Si/SiGe/Si/SiGe/Si) Fins. SiGe is then selectively etched leaving suspended Si-channels. (b) TEM cross section of such Si/SiGe fin patterned with an adaptation of the SIT process presented in §1.3.3: 40 nm pitch array is obtained with a 60 nm high stack of three NWs [Gaben 2015a].

As device footprint is also decisive in the selection of a technology, any benchmarking must be done within a constant footprint. In other words, two FinFETs or SNWFETs should always be compared when having the same envelope or cross section as pictured in the example of Figure 2.18.

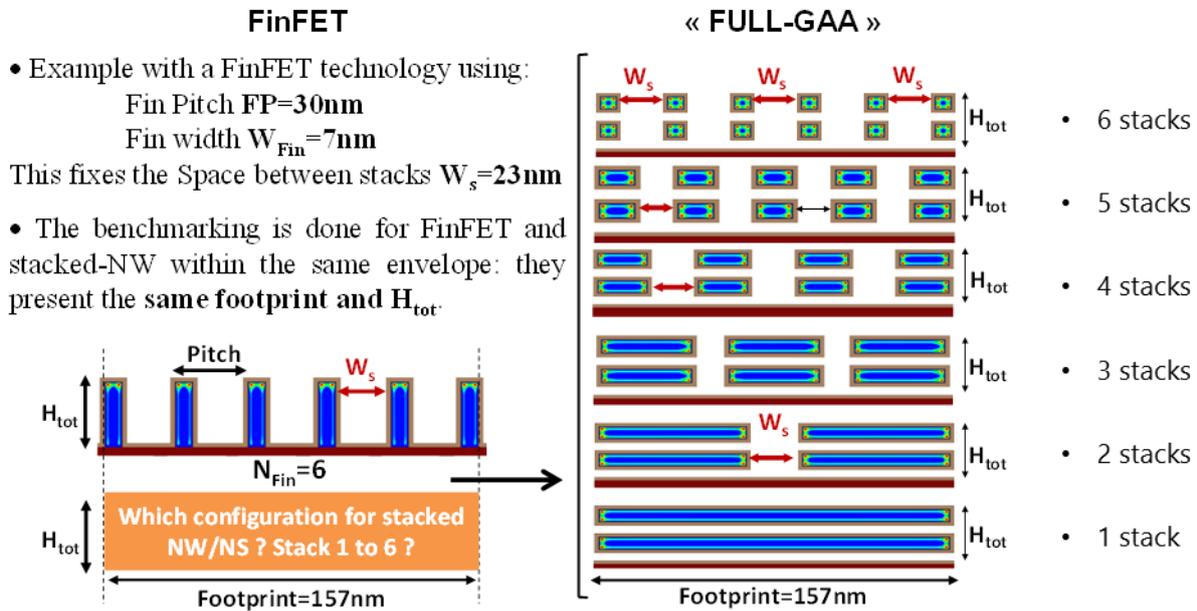


Figure 2.18 - Guideline for benchmarking FinFET and stacked-NW architectures. Several stacked-NW configurations match the envelope defined by the FinFET configuration. In this example labeled “FULL-GAA” with two GAA vertically stacked, several NW width ( $W_{\text{NW}}$ ) meet the condition Footprint = 157 nm for  $H_{\text{tot}} = H_{\text{Fin}}$ .

### 2.3.2. Results and discussion

Assuming a FinFET technology characterized by  $W_{\text{Fin}} = 7\text{ nm}$  and  $FP = 30\text{ nm}$ , with a supply voltage  $V_{\text{DD}} = 0.7\text{ V}$  and a minimum gate length fixed at  $L_G = 16\text{ nm}$ . A 157 nm footprint which corresponds to 6 silicon fins was used as an example. The electrostatic control is investigated for FinFETs and two types of SNWFETs. Figure 2.19 shows that in a full GAA configuration, more than 46% wider effective width  $W_{\text{eff}}$  can be obtained within the same transistor section while keeping the same DIBL as the FinFET. The mixed configuration presents only 15% improvement in  $W_{\text{eff}}$  at constant DIBL due to the impact of this bottom tri-gate NW even if  $H_{\text{NW}}$  is thinned down to 6.3 nm (§2.2).

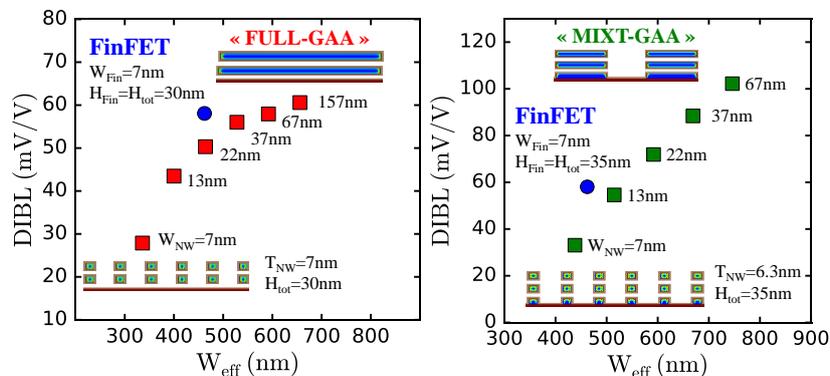


Figure 2.19 – DIBL as a function of effective width  $W_{\text{eff}}$  in the case of footprint = 157 nm: several  $W_{\text{NW}}$  are allowed increasing  $W_{\text{eff}}$  over the reference FinFET configuration ( $L_G = 16\text{ nm}$ ).

Similarly as in (§2.2.2), parasitic capacitances are extracted but for several multi-fins and multi-stacks configurations. With a 157 nm footprint example, Figure 2.20 shows that normalized gate-to-drain capacitance  $C_{gd0}$  grows slower than  $W_{eff}$ . As a result, switching delay might not be penalized when trying to increase the drive current by an increase of  $W_{eff}$  through  $H_{Fin}$  or  $W_{NW}$  for FinFET and stacked NW respectively. Figure 2.20b also shows a similar trend when stacking one or more NWs: in other words,  $W_{eff}$  increases more than  $C_{gd0}$  as  $H_{tot}$  is increased.

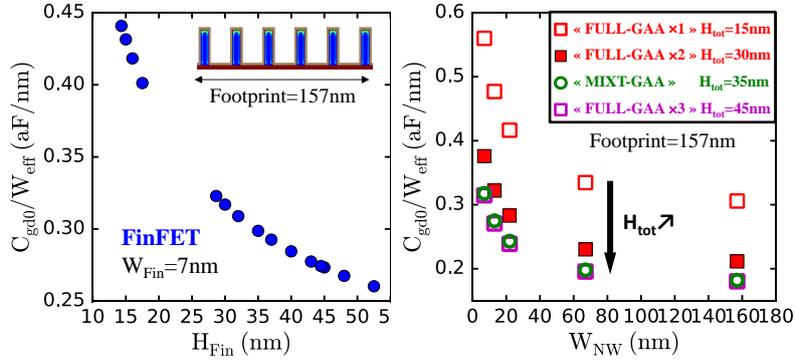


Figure 2.20 - Normalized gate-to-drain capacitance as a function of  $H_{Fin}$  and  $W_{NW}$  within a 157 nm footprint for (a) FinFET and (b) stacked-NW architectures.

Various FinFET and SNWFET configurations are therefore compared using the intrinsic delay (Eq. 2-1). The effective current  $I_{Eff}$  is extracted from the simulations and the expression of  $C_{eq}$  is calculated from  $C_{gd0}$  also extracted from C-V simulations as explained in §2.2. The precision of the transport model is limited to relative comparisons in between the various devices and architectures. Consequently, the advantage of SNWFET architecture over FinFET will be characterized by using the delay reduction formulae of (Eq. 2-12).

$$Delay\ reduction = \frac{\tau_{FinFET}(footprint, H_{tot}) - \tau_{GAA}(footprint, H_{tot})}{\tau_{FinFET}(footprint, H_{tot})} \quad (Eq. 2-12)$$

Figure 2.21 shows the delay reduction obtained by switching for a full GAA NW technology with two NWs per stack as a function of the footprint. Each SNWFET configuration is compared to FinFETs having the same  $H_{Fin} = H_{tot}$  and the same footprint as well. In this example, the FinFET devices have the following characteristics:  $W_{Fin} = 7$  nm,  $H_{Fin} = 30$  nm and fin pitch  $FP = 30$  nm inducing a space between two fins or between two NWs of  $W_S = 23$  nm. NW thickness is  $H_{NW} = 7$  nm and vertical space between two NWs is  $H_{space} = 8$  nm for a total height  $H_{tot} = H_{Fin} = 30$  nm. NW width takes incremental values in between 7 nm and 157 nm to match at the same time the footprint of the FinFET devices and  $W_S = 23$  nm.

Highest improvements are obtained for the largest nanowires confirming the advantages of nanosheets in terms of effective width improvement. This advantage is increased as larger footprints are considered. Up to -44% delay time could be saved by preferring the configurations where  $W_{NW} = Footprint$ .

Additionally, delay reduction seems to depend only on NW width  $W_{NW}$ . For example, the three configurations embedding  $W_{NW} = 37$  nm large NWs present a delay reduction of -26%, -25% and -24% for 37 nm, 97 nm and 157 nm footprints respectively.

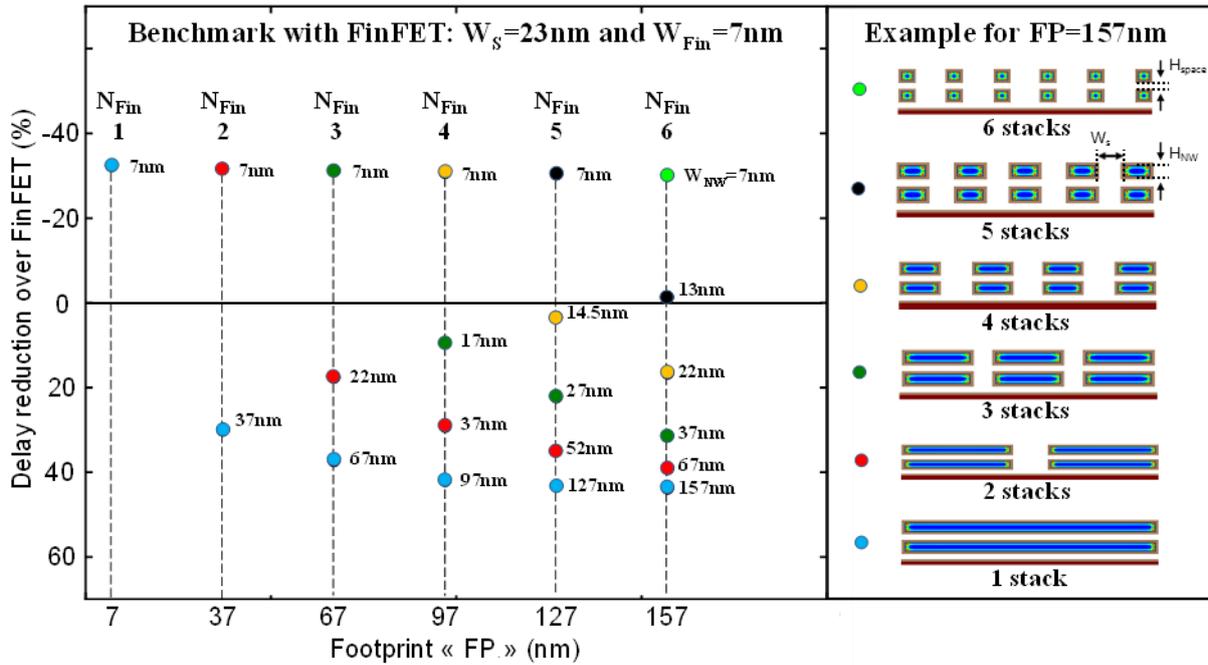


Figure 2.21 - Delay reduction over FinFET technology for different footprint and  $W_{\text{NW}}$ .

Therefore, Figure 2.22 displays in red squares the same data points of the previous graph (Figure 2.21) as a function of NW width instead of footprint. An alternative configuration with three vertically stacked GAA NW channels per stack with  $H_{\text{tot}}' = H_{\text{Fin}}' = 45\text{nm}$  is also presented in blue circles. Again, all configuration having identical NW width matches a similar delay reduction.

As a result, even in case of an improvement of the patterning technology allowing taller fins to be fabricated, taller NW stacks can also be performed (§2.3.1) and therefore the advantage of SNWFET technology is preserved depending only on NW width.

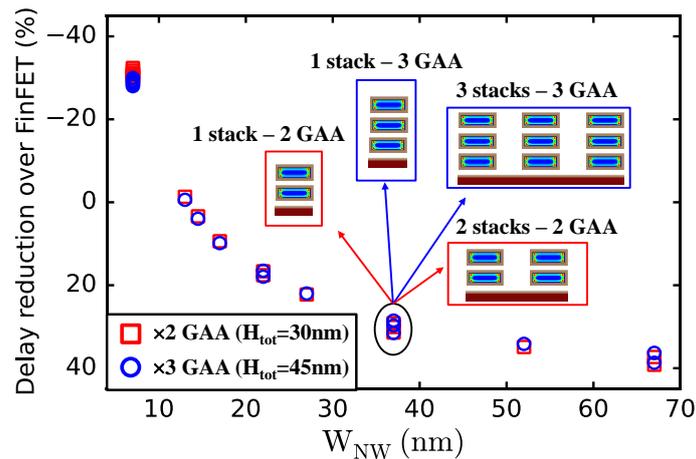


Figure 2.22 - Delay reduction over FinFET technology for different  $W_{\text{NW}}$  independently of the number of stacked GAA channels or footprint: delay reduction depends mainly on  $W_{\text{NW}}$

Subsequently, this plot can be used as a figure of merit in order to evaluate the other main technology parameters. Figure 2.23 shows the influence of the fin pitch which also determines the space  $W_s$  in between two fins or two stacks of NWs (§2.3.1).

For  $W_s = 18$  nm (FP = 25 nm) the delay reduction over FinFET technology is less significant due to a lower gain in effective width: in other words, the ratio  $W_{\text{eff\_FinFET}}/W_{\text{eff\_NW}}$  decreases.

By using thinner NWs ( $H_{\text{NW}} = 6$  nm), the performance gap is enlarged in favor of SNWFETs thanks to better electrostatic control of the gate (reduced DIBL) when comparing with the same 7 nm large fins.

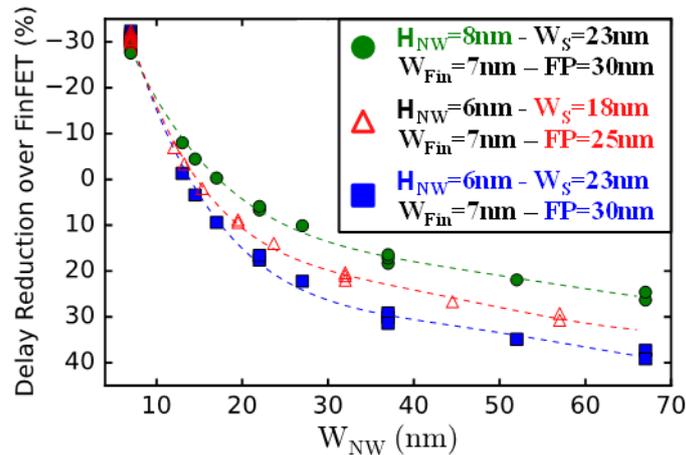


Figure 2.23 - Figure of merit: delay reduction over FinFET technology for two different FinFET technology fin pitch (FP = 25 nm and FP = 30 nm) and for two different stacked NW channel thicknesses ( $H_{\text{NW}} = 6$  nm and  $H_{\text{NW}} = 8$  nm).

### 2.3.3. Towards stacked nanosheets?

The benchmark methodology developed in this sub-chapter compares FinFET and SNWFET technologies having identical footprint and total height. This appeared to be one of the best solution to take into account all the fabrication advances that both architectures would benefit in the near future (§2.3.1).

Large and thin stacked NWs or stacked nanosheets (SNS) present increased effective width per footprint unit and limited parasitic capacitances providing them with a significant advantage over FinFETs. This advantage is mostly related to the NW widths no matter the number of stacks nor the total height of the stacks.

In order to increase FinFET output current, several fins per transistor need to be added. Consequently, current, performances and therefore footprint are quantified in FinFET [2012 Lacord SSDM]. In opposition, SNWFET technology is more flexible as drive current can be easily tuned by changing the NW width.

Besides, the performance advantage of SNWFET for a given footprint can be turned to lower the transistor footprints with identical performances. Both performances and footprint can also be balanced through appropriate NW width.

## 2.4. Internal spacer and gate alignment is key to reduce parasitic capacitances

Most of the fabrication steps of stacked-NW devices can be derived from the gate-last fabrication of FinFETs (§3.1). The main differences reside in the release of the suspended silicon channels and the fabrication of internal spacers in between the NWs of the stack (§3.4). Figure 2.24 illustrates a two GAA SNWFET with internal spacers located under the main spacer isolating the HKMG from the S/D. In the later, SNWFETs were simulated with aligned internal spacers having the same thickness and dielectric constant as the main spacers. However, when following the standard gate-last integration process flow of FinFETs, only the 1.8 nm thin layer of gate dielectric isolates the metallic gate from the S/D epitaxies which may result in increased gate-to-drain parasitic capacitances.

This subchapter evaluates the negative impact on SNWFET performances of removing these low-k internal spacers in order to justify the development of this SNWFET-specific integration module in the following chapter.

No specific fabrication knowledge is needed for the understanding of the following section. Thus, insights into these architectures are provided in the following next chapter (§3.1) and [Gaben 2016 ECS].

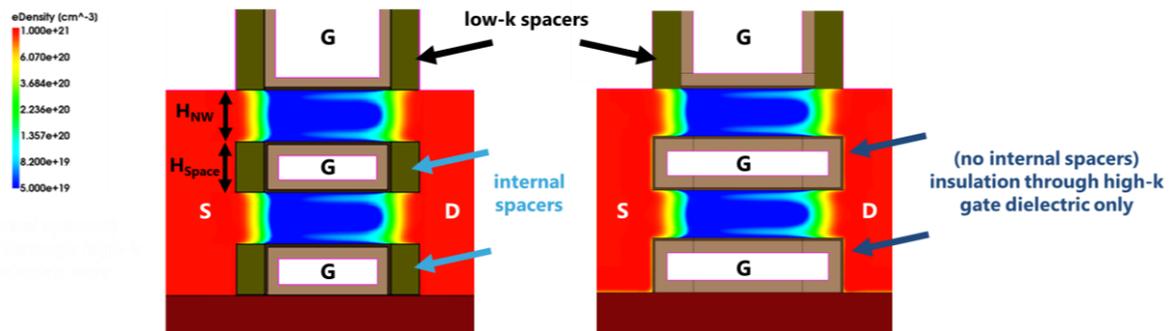


Figure 2.24 - Adaptation of the original deck: inner spacers are removed.

Figure 2.25 shows the increase of gate-to-drain parasitic capacitance  $C_{gd0}$  as internal spacers are removed. Difference is even increased as the NW width is enlarged which is particularly detrimental when considering nanosheets. A decrease of the vertical space  $H_{space}$  in between the NWs of the stack also contributes in reducing  $C_{gd0}$  as a consequence of the proportionality of the capacitances with the surfaces at play.

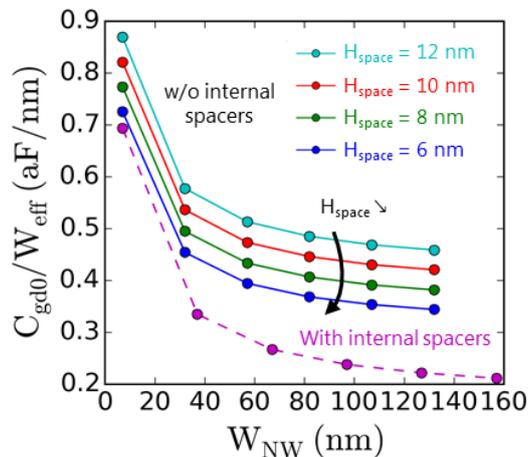


Figure 2.25 – Impact on parasitic capacitances of removing the internal spacers.

Similarly to the previous subchapter (§2.3), these values can be wrapped up in the delay reduction. Figure 2.26, shows from -15 % to -20 % of advantage over FinFET can be lost if internal spacers are removed, up to the point that there is no longer any advantages to use SNWFET.

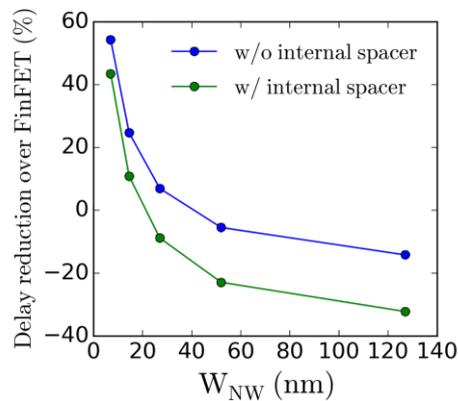


Figure 2.26 - Impact on delay of removing the internal spacers.

Adding internal spacers is therefore essential. The alignment of these internal spacers also deserves some attention. The source or drain side of the internal spacers is limited by the fabrication process involving an anisotropic etch removing precisely any material outside the internal spacer cavities. Only the etch depth under the NWs can vary (§3.1). Figure 2.27 illustrates the internal spacers thickness in case of under etch and in case of over etch. Main spacers are 4.2 nm thick (§2.1.1).

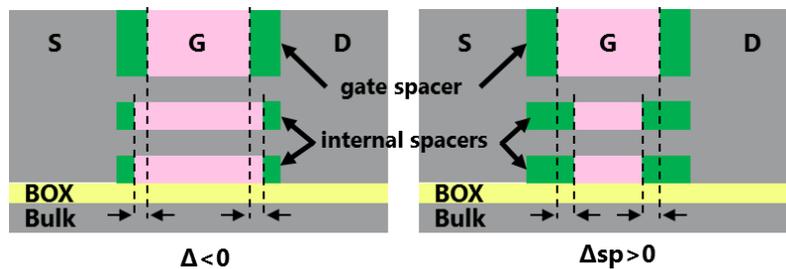


Figure 2.27 – Spacer alignment issue for a dual GAA SNWFET: (left) under etch case and (right) overetch case.

Figure 2.28 presents the impact of misalignment on SNWFET performances for several NW widths. Although a thicker spacer reduces the parasitic coupling between the gates and the S/D (Figure 2.28b), this is counter balanced by the reduction of the gate surface in contact with the channel and DIBL increases (Figure 2.28c). On the contrary, reduction or absence of internal spacers improves the electrostatic control as several of the gates extend slightly more over the channel. This points out the existence of an optimum for the thickness and for the location of the internal spacer to maximize performances (Figure 2.28d). Taking into account some variability in the fabrication process, this optimum might not be the “aligned” position considering the higher slope on the side of a too thick spacer. However, considering the precision of the models used here, it is not possible to draw a general conclusion outside of this perspective.

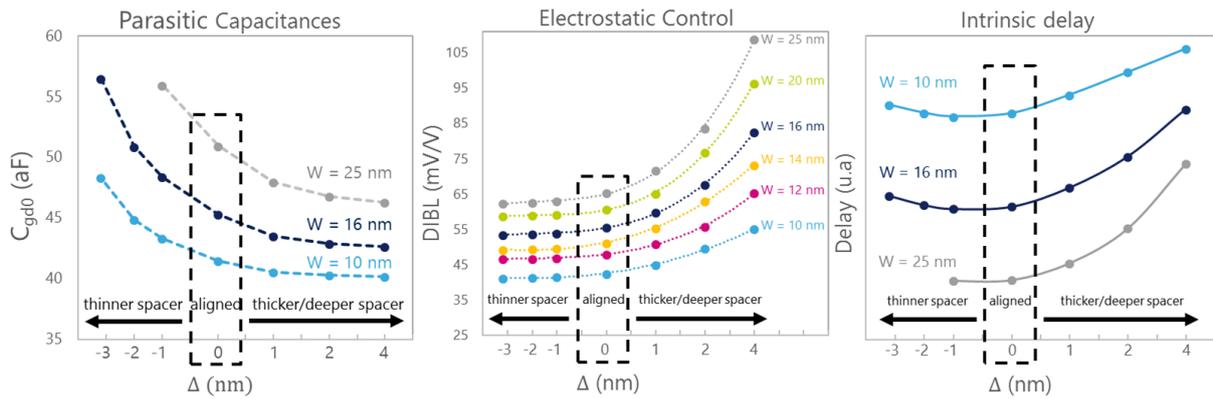


Figure 2.28 – (a) Spacer alignment issue for a dual GAA SNFET and its impact on (b) the parasitic capacitances, (c) on the electrostatic control and (d) on the intrinsic delay.

Finally, adding internal spacers is necessary to at least preserve and increase the advantage of SNWFETs over FinFETs estimated in (§2.3). Even if the space between the vertically stacked NWs is reduced, parasitic capacitance reduction induced by the low-k material remains significant enough to justify the added fabrication steps described in the next chapter (§3.1). The alignment of these internal spacers was shown to be important. Although self-aligned spacers are preferable, simulations suggest the existence of a sweet point when considering a non-self-aligned fabrication process with some intrinsic variability.

## 2.5. Discussions

The current chapter is focused on electrostatic behavior of FinFETs and stacked-NW FETs which is known to dominate their performances. As revised in (§1.1.2) and as studied in (§1.3.2), confinement may have a significant impact on transport properties and computing the band structures of each different confined geometry can improve the benchmark accuracy.

In the previous section, only the NMOS were simulated with a constant mobility model ( $\mu_e = 100 \text{ cm}^2/\text{V}\cdot\text{s}$ ). This strong simplification restricted the study to relative comparisons in between the two architectures, especially concerning the intrinsic delay. Again, as observed in (§1.1.2) and in (§1.3.2), the mobility strongly depends on transverse electric field and is also influenced by channel geometry and orientation, surface roughness, gate stack (EOT,  $D_{it}$ ...), residual stress and confinement which are all technology dependent. Implementing an improved mobility model would bring significant improvements; although actual devices are required for accurate parameter calibration of any advanced model and were not available at the time of this preliminary study.

As noticed in (§1.3.2), transport of holes in PMOS seems advantaged along (110) vertical sidewalls of trigate NW transistors while electron transport is fastened in (100) horizontal planes when considering standard  $\langle 100 \rangle$  oriented channels. Since the inverter delay – often used for device benchmarking along with ring oscillators – is an average of the NFET and PFET delays, an evaluation of the weight of each surface channel contribution would be interesting. Although the facet dominated transport model seems significantly impacted by quantum confinement in such narrow NWs and fins, a hybrid integration may worth consideration. In such concept, stacked nanosheet technology would be likely

preferable for building NFETs whereas vertical FinFETs may provide improved mobility for the realization of PFETs. The previous simulations also do not account for channel strain introduced by SiGe RSD and enhanced by the gate-last process, nor SiGe channels strained on SOI after epitaxy as measured in the later fabricated devices (§4), [Barraud 2016 IEDM].

In the present simulations, S/D were considered uniformly and highly doped. However, as already observed in FinFET technology, access resistance may be different from the bottom of the fin to the top: an accurate model taking this effect into account is likely needed to study the impact of the integration flow chosen for the S/D. In this thesis, the in-situ doping realized after a vertical recess of the NW extensions provides a configuration very close from the simulated case and only junction abruptness may need attention in the model likely with calibrations (§3.1). Hopefully, strong similarities with FinFET fabrication process let expect that SNWFET technologies will benefit from recent developments on FinFET [Kikuchi 2016 IEDM].

## 2.6. Conclusion

The present chapter presents simulation studies that were realized with the objective of identifying the most promising structures with better chances to compete with FinFET and eventually to replace this architecture for the 7 nm node technologies and beyond.

Although a basic transport model has been used, the conclusions were mostly drawn from subthreshold behavior of the transistors which itself relies on a calibrated quantum confinement model. Moreover, the results are also consistent with other data published by IBM [KimSD 2015 S3S].

Thin and large vertically stacked nanowires or nanosheets seem to provide better performances as compared to FinFET devices while having an equivalent or smaller overall footprint. Subsequently, this study has pointed out the flexibility of such NW based structure since device footprint can be fine-tuned through NW width while FinFET technology must deal with discrete values of the footprint depending on how many parallel fins are used.

Finally, the interest of building internal spacers in between the vertically stacked-NWs have been evaluated. The risk of wiping out any performance advantage of SNWFETs over FinFETs has been identified and is specifically attributed to the increase of parasitic capacitances when removing these internal spacers.

As a result, in this work, efforts have been put into proposing devices that will decrease parasitic capacitances by employing internal spacers. This will be described in the following next chapter (§3).

### 3. Stacked nanowire FETs: integration challenges and process optimization.

As discussed in the first chapter (§1), SNWFETs must be fabricated within a gate last integration flow. Therefore, and despite of the similarities, the typical FinFET integration must be adapted to the specificities of stacked channels and more specifically, internal spacers must be fabricated as concluded in the simulation of the second chapter (§2). In a first part of this chapter, two main alternatives for the integration of SNWFETs with internal spacers and regarding a gate last process are first described (§3.1). A brief comparison with few other discarded alternatives is made to understand the advantages of these two selected ones. Afterwards, the following subchapters focus on five major process developments: the Si/SiGe superlattice epitaxy (§3.2), the Si/SiGe fin patterning (§3.3) and the selective etching of SiGe (§3.4) are first discussed, which then introduces the S/D module fabrication with internal spacers (§3.5). Another subchapter is dedicated to the lithography of HSQ sacrificial gates (§3.6). Finally, the last subchapter points out the challenges of such gate last approaches for chemical mechanical planarization processes (§3.7). Thanks to this insight on these specific processes and their cross-dependency, SNWFET technologies can be built with selected options such as the two examples that are provided in the chapter 4.

#### 3.1. Gate last integration flows of stacked nanowires

As show in Figure 3.1, and as already introduced in §1.3.4, top-down fabrication of NW stacks is usually starting from a superlattice epitaxy of Si and SiGe (Figure 3.1a). Then the Si/SiGe fins are patterned using a process derived from silicon fin patterning (Figure 3.1b). Finally, the sacrificial SiGe is removed selectively towards Si leaving the silicon NW channels suspended. However, this etching can be carried out at different step of the integration: if the Si NW are released prior to the sacrificial gate patterning, the approach is named “NW first” (Figure 3.1c-d). If the Si/SiGe fins are kept for remaining as close as possible from a FinFET integration, this option is referred to as “NW last” (Figure 3.1c-d) since the NWs are then suspended only after the sacrificial gate removal. A polysilicon sacrificial gate is preferred for NW last integration to rely on a FinFET integration base while an HSQ sacrificial gate is definitely preferred for the NW first approach to benefit from self-aligned lithography as introduced in §1.3.4. Hence the present subchapter presents these two alternatives and their specificities. The last third section explains the reasons for the abandon of the other combinations.

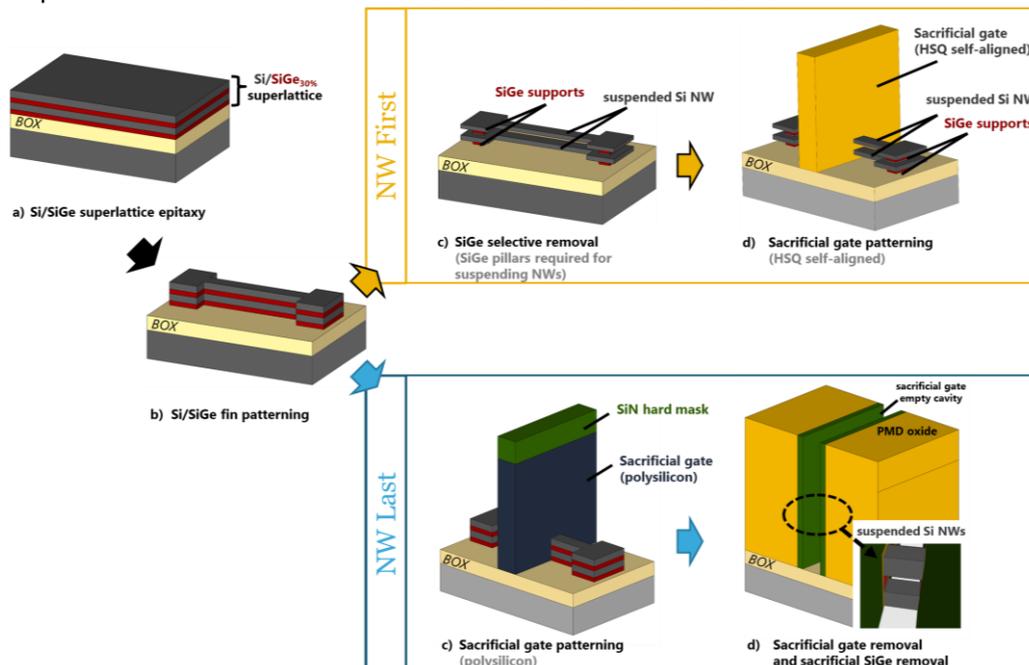


Figure 3.1 – NW first and NW last integration schemes [Gaben 2016 ECS].

### 3.1.1. NW Last: polysilicon sacrificial gate

The NW last approach can be considered as the “mainstream” option due to high similarities with FinFET integration since the silicon fins are here replaced by Si/SiGe ones [Mertens 2016 VLSI], [Barraud 2016 IEDM]. As highlighted in dark blue in Figure 3.2, only four key process steps are specific to the SNWFETs as compared to FinFET technology: the superlattice epitaxy, the fabrication of the Si/SiGe fins, the internal spacers fabrication during the RS/D epitaxy and the sacrificial SiGe selective removal (within the removed gate cavity after the sacrificial gate etching). The following sub-section describes one possible integration following this approach with a specific focus on the internal spacer fabrication and the self-aligned contacts (SAC).

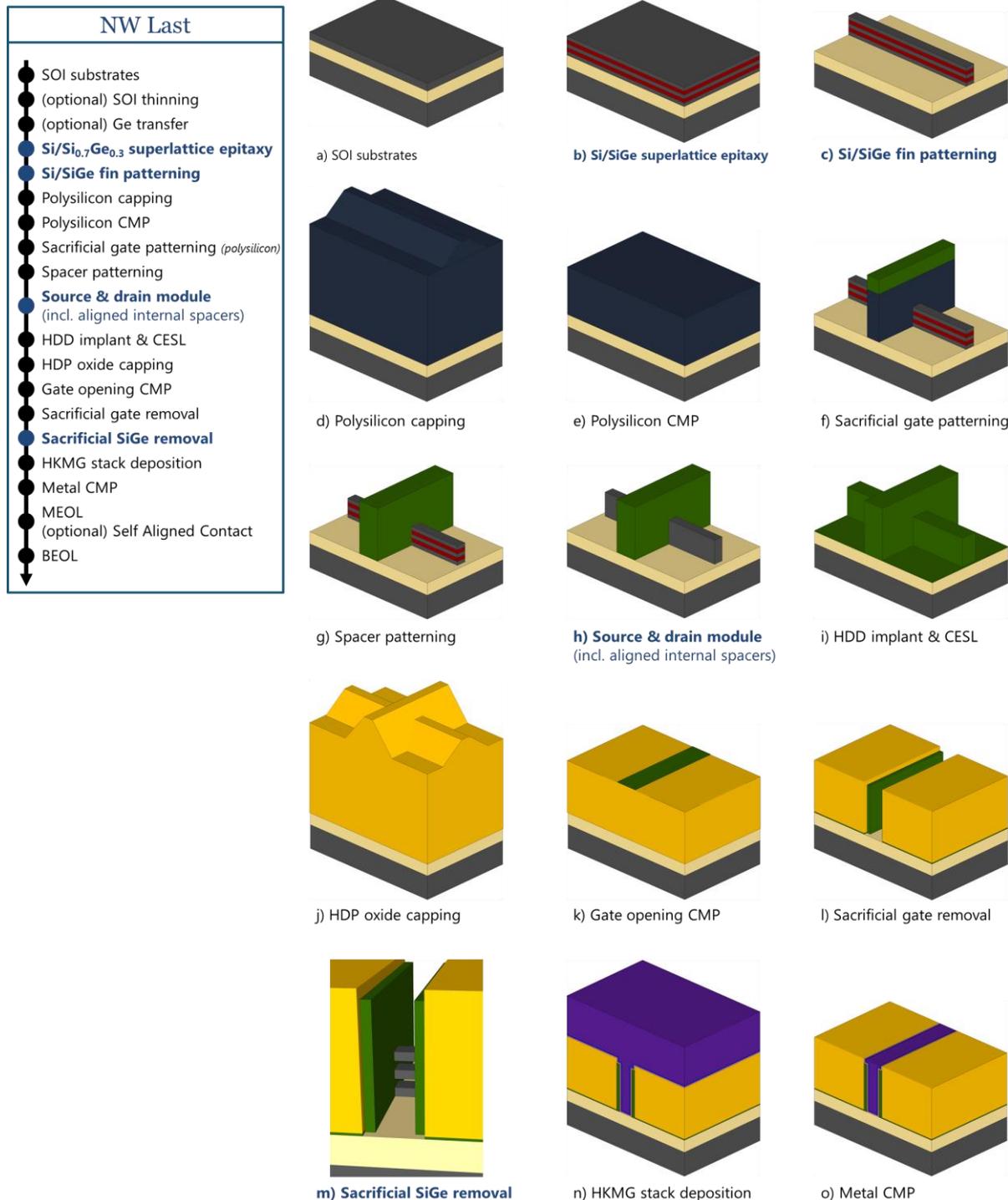


Figure 3.2 - Gate last NW last integration of stacked NWs with polysilicon sacrificial gate and SAC.

## Initiation

As explained previously, the NW last integration starts with the superlattice epitaxy of Si/SiGe following the process described in (§3.2). To achieve different order and thickness of NW stacks, optional steps of Ge condensation and SOI thinning can be introduced. Si/SiGe fins are then patterned (§3.3) prior the deposition and the planarization of a conformal layer of polysilicon. A SiN hard mask and a tri-layer optimized for the DUV lithography are then deposited prior to the patterning of the sacrificial gates. SiN gate spacers are finally deposited and patterned along the gate with an anisotropic etch.

## Source and drain (S/D) fabrication with aligned internal spacers

As concluded from simulations in the previous chapter (§2.4), the addition of internal spacers contributes in reducing parasitic capacitances. Figure 3.3 shows schematics of a source-to-drain longitudinal section presenting the S/D fabrication steps including these internal spacers. The process flow relies on the selective etching of SiGe for carving cavities in between the Si NWs. The first step consists in a vertical anisotropic etch of the Si/SiGe extensions (Figure 3.3a-b). If the transistors are fabricated on SOI substrates, a nanometric seed layer of silicon must be left at the bottom of the stack on the BOX for the later in-situ doped selective epitaxy growth (SEG) of the S/D. The isotropic partial etch of SiGe is then carried out selectively towards the Si NW channels leaving small cavities aligned under the first gate spacers (Figure 3.3c). Selectivity is therefore extremely important to preserve the entrance of the channel. A second conformal deposition of SiN fills these cavities as shown on Figure 3.3d. Another anisotropic etching similar to the spacer patterning is then performed. A small isotropic component is maintained in order to reveal the silicon channels entrances (Figure 3.3e). A phosphorus in-situ doped Si or a boron in-situ doped SiGe SEG is finally performed from the bottom epitaxy seed layer to the top NWs for merging the stacked channels around the internal SiN spacers (Figure 3.3f). As observed in Figure 3.3g, the SiN internal spacers serve also as a etch-stop during the sacrificial SiGe removal.

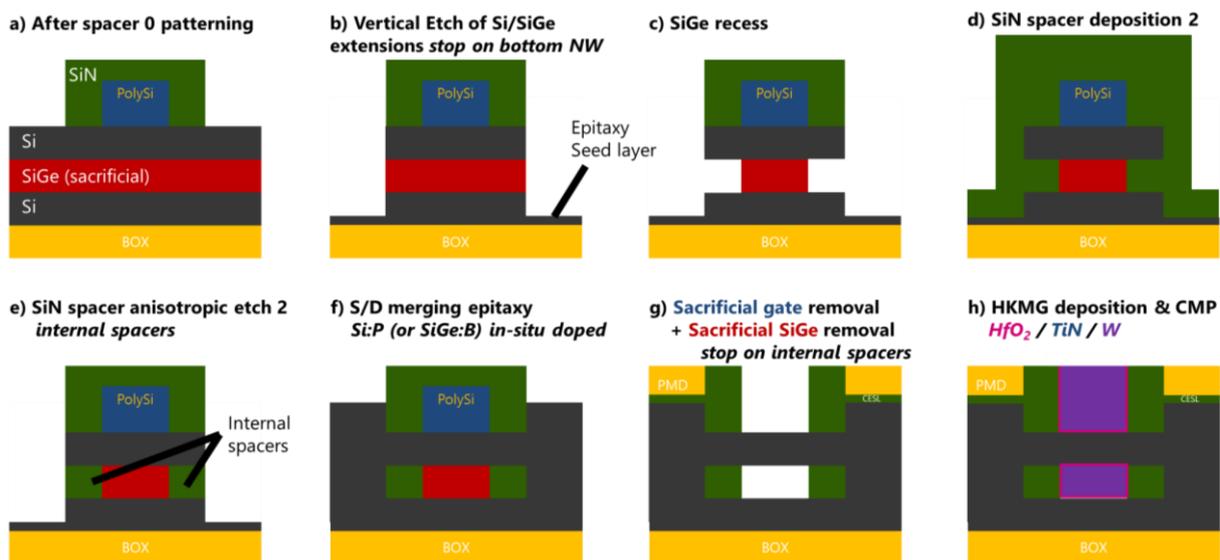


Figure 3.3 - Internal spacers fabrication steps, sacrificial gate removal and stacked NW release.

## Sacrificial gate removal and NW stack release

Next to the S/D fabrication, a protective contact-etch-stop layer (CESL) and an oxide capping are deposited right above as described in Figure 3.3g. This oxide pre-metal dielectric (PMD) consists in a first oxide atomic layer deposition (ALD) ensuring a slow but conformal deposition on these high aspect-ratio features before finishing the encapsulation with a high-density plasma (HDP) oxide with higher deposition rate. A CMP is then performed to reach the top of the polysilicon sacrificial gate stopping selectively on the remaining SiN hard mask above it. Once the SiN material and the polysilicon gate are etched away with a peroxide and a hot TMAH solutions respectively, the sacrificial SiGe can therefore be selectively removed to leave the suspended Si channels (Figure 3.3g).

## HKMG

Finally, the surface of the channels is chemically oxidized in preparation for a 2 nm HfO<sub>2</sub> ALD. A nitridation can additionally stabilize the high-k prior to a 3 nm deposition of a TiN barrier. Tungsten is deposited to achieve the gate contact. Then, a metal CMP selective to the PMD oxide is performed to remove any gate stack material from outside of the gate cavity (Figure 3.3h).

## Self-aligned contacts

A self-aligned contact (SAC) module can be implemented following the steps of Figure 3.6. SACs are used to reduce misalignment issues during contact patterning thanks to a protective SiN stopper above the gate [Niebojewski 2014 SSE]. Access resistance is also improved since the contacts are patterned as close as possible from the channel entrance. However, one side-effect is the increase of the gate-to-contact parasitic capacitances.

First step consists in recessing the tungsten gate contact as shown in Figure 3.4a. A conformal SiN is then deposited inside the remaining cavity (Figure 3.4b) and a CMP stopping on the oxide filling is performed. Therefore, the SiN stopper only remains to protect the top of the HKMG (Figure 3.4c). As shown in Figure 3.4d, the negative of the active level lithography mask is used for patterning the S/D SAC contacts. Hence, a portion of the gate is exposed during the etch and needs the stopper protection.

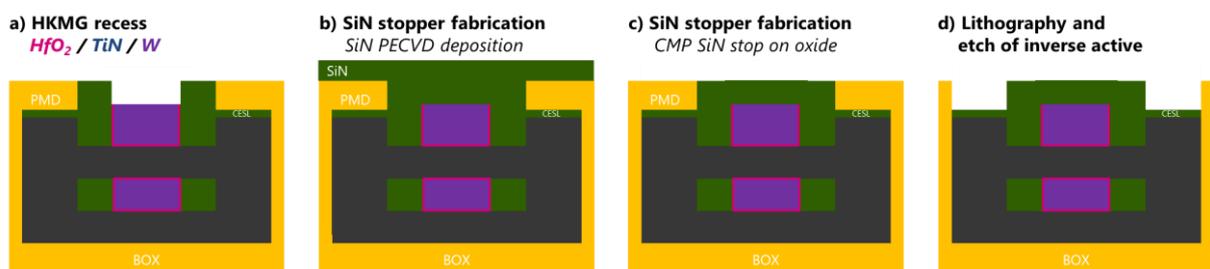


Figure 3.4 - Self-align contact (SAC) module: inverse active patterning.

As shown in Figure 3.5a, the CESL is then removed to open an access for the top of the S/D and allows the NiPtSi silicidation to be performed (Figure 3.5b-c). Again, the SiN stopper protects the HKMG during the removal of the unreacted NiPt (Figure 3.5d).

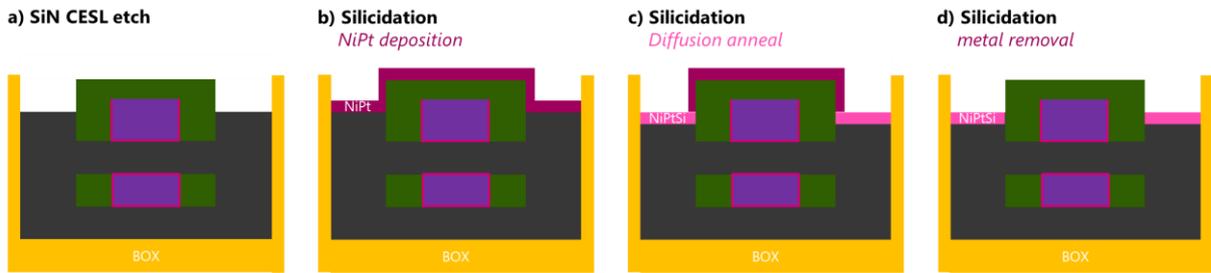


Figure 3.5 – Self-align contact (SAC) module: silicidation.

Finally, tungsten is deposited (Figure 3.6a) and after a last metal CMP stopping on oxide and SiN (Figure 3.6b) the source and drains are finally disconnected. The contacts are finally etched into another layer of HDP oxide (Figure 3.6c-d) and a new deposition of tungsten is carried out to fill the contacts holes (Figure 3.6e) with a last CMP for clearing the metal from the oxide surface (Figure 3.6f). Figure 3.6f illustrates the interest of SAC in case of lithography misalignment: SAC allows to relax the requirements in overlay on very aggressively scaled layouts such as in SRAMs.

Other techniques such as self-assembly of copolymer blocs seem also promising for contact patterning however the technology is not mature enough to be considered in the framework of this thesis. Hence only the CMP of tungsten will be described in the last subchapter (§3.7).

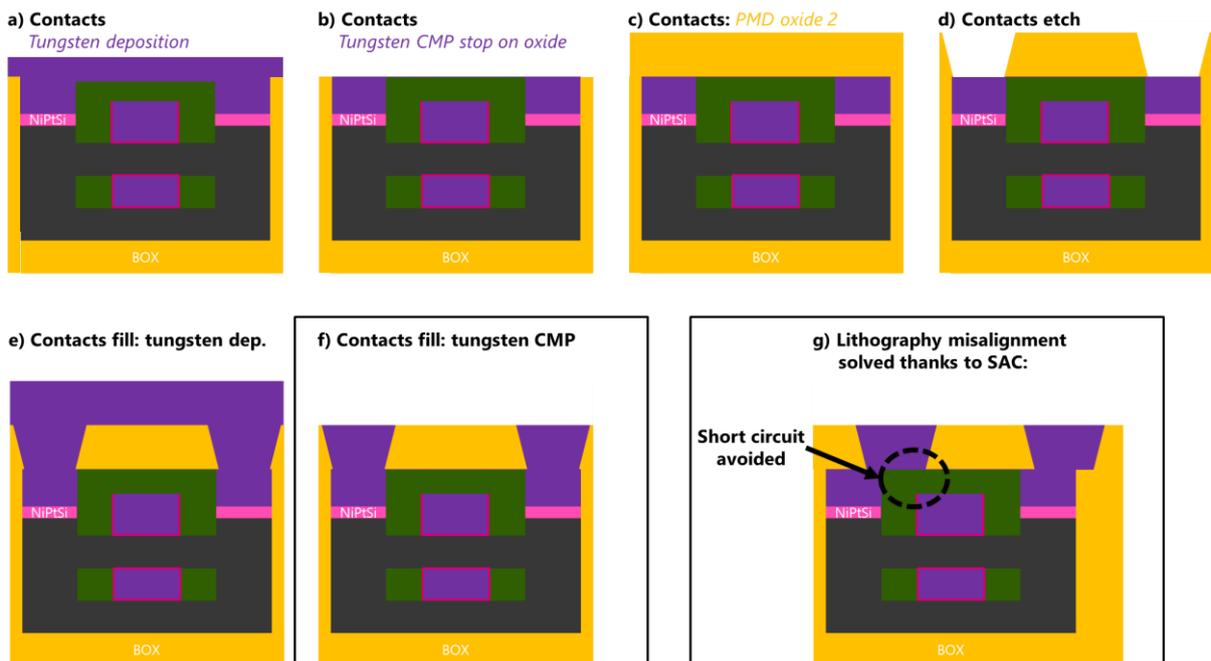


Figure 3.6 – Self-align contact (SAC) module: contact patterning.

### 3.1.2. NW First: HSQ sacrificial gate

As explained in the first chapter (§1.3.4), hydrogen silsesquioxane (HSQ) is a non-organic resist which is turned into a silicon oxide when exposed to an electron beam (ebeam) or an EUV light. Silicon being transparent to such sources, HSQ can be therefore used for building self-aligned features through the suspended silicon nanowires. Besides, the fabrication of sacrificial gates with HSQ appears relevant since the presence and the alignment of internal spacers have significant impacts on SNWFET performances according to the conclusion of the previous chapter (§2.4). The integration presented in Figure 3.7 features HSQ sacrificial gates replacing the typical polysilicon material. The integration scheme corresponds to a “NW first” approach since the suspended NW channels are obtained before the sacrificial gate patterning.

#### Initiation

As for the NW last approach, the integration starts with the superlattice epitaxy of Si/SiGe (Figure 3.7a) with optional steps of Ge condensation and SOI thinning. After the Si/SiGe fin patterning (Figure 3.7b), the sacrificial SiGe is selectively removed leaving suspended NWs (Figure 3.7c). Unlike with the NW last approach, anchor points are required on both ends of the NW stacks. Hence, SiGe etching depth must be optimized according to the NW width and relatively to the width of the anchors so enough SiGe will remain within the anchors to maintain the structure. Mechanical resistance of these stacks will be discussed in (§3.4).

#### Sacrificial gate patterning

HSQ is then spincoated with adjusted viscosity and spinning speed to obtain the desired film thickness which is also the height of the future sacrificial gates (Figure 3.7d). An ebeam or an EUV exposure is then performed (Figure 3.7e) and the HSQ oxide sacrificial gates remain after developing in TMAH without requiring any etching or stripping step since the non-organic polymer resist turns itself into the desired oxide features (Figure 3.7f). Since Si does not hinder ebeam exposure, the HSQ gates are vertically self-aligned through the NWs of the stack.

#### S/D fabrication with self-aligned internal spacers

Afterwards, the first SiN spacer is patterned along the sides of the HSQ gates (Figure 3.7g). Since this highly conformal layer also fills the space in between the suspended silicon NWs, self-aligned internal spacers are formed at the same time. Several vertical anisotropic etchings are then performed to recess the S/D extensions composed with several layers of Si and SiN (Figure 3.7h). A nanometric seed layer of silicon is left of the bottom NW so a Si:P or a SiGe:B in-situ doped SEG of the S/D can be performed to reconnect the silicon NW channels around the self-aligned internal spacers (Figure 3.7i).

#### HKMG

Therefore, the S/D are capped with a SiN CESL layer and a polysilicon layer (instead of oxide in the NW last approach). CMP of the polysilicon is then performed to open an access to the HSQ sacrificial gates (Figure 3.7j). HSQ oxide is then removed with hydrofluoric acid (HF) selectively towards polysilicon capping and SiN spacers (Figure 3.7k). The sacrificial SiGe had already been removed before HSQ lithography, the suspended NWs are directly covered with 2 nm of HfO<sub>2</sub> high-k dielectric ALD after surface preparation. A nitridation can additionally stabilize the high-k prior to a 3 nm deposition of a

TiN barrier. Tungsten is then deposited to make the gate contact and a metal CMP selective to polysilicon is performed to remove any gate material from outside of the gate cavity.

## Contacts

Polysilicon can be removed with TMAH and finally, a SAC module can be implemented similarly as described for the NW last integration (§3.1.1).

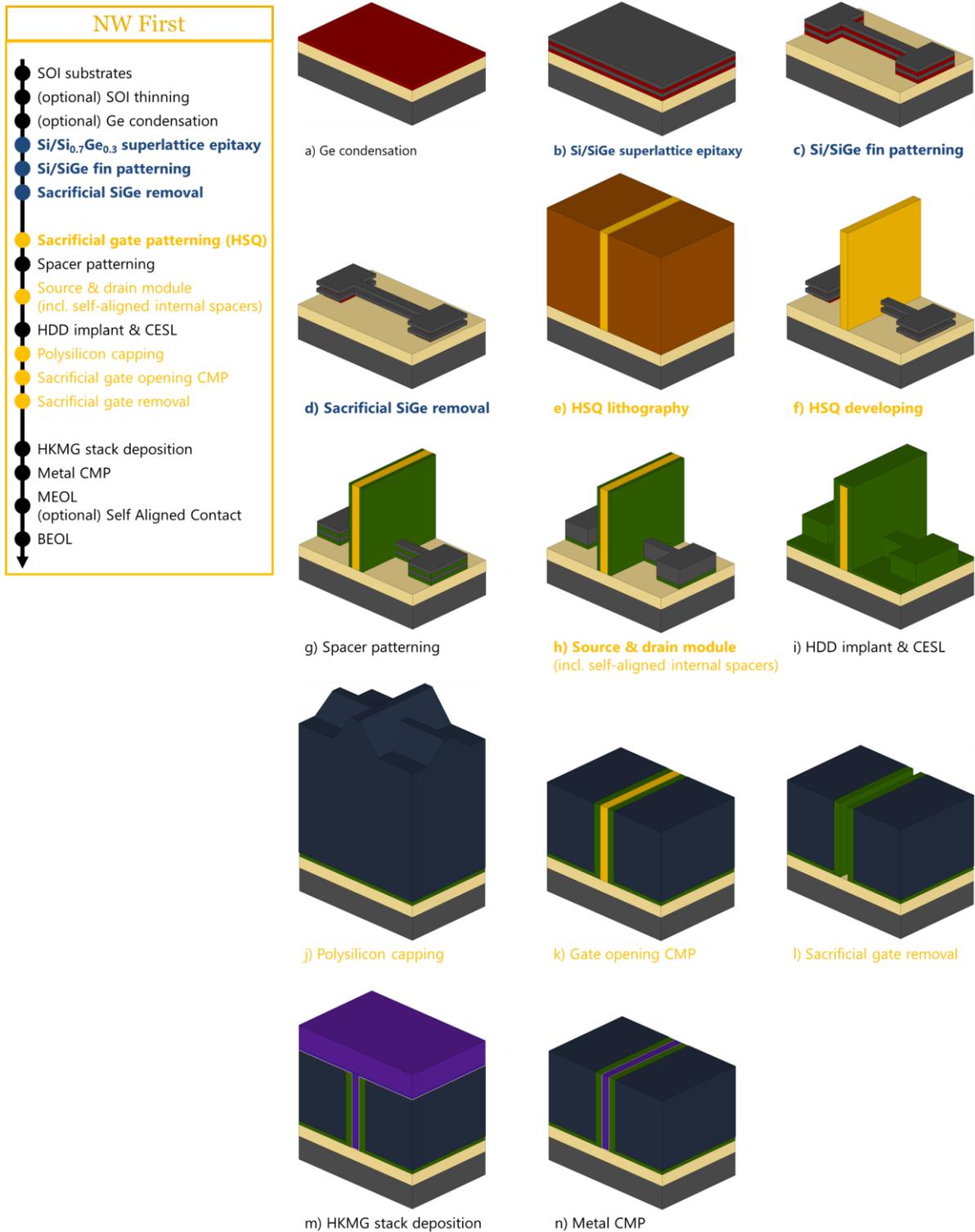


Figure 3.7 - Gate last NW first integration of stacked NWs with HSQ sacrificial gate and SAC.

### 3.1.3. Alternatives?

The objective of this section is to provide a better understanding of the two integration flows that were retained in the last two sections through the examples of the combinations of NW last/first approaches and polysilicon/HSQ that were rejected for cleanroom developments.

#### NW last without internal spacers

Although the advantages of internal spacers in terms of parasitic capacitance reduction was demonstrated in (§2.4), one may want to avoid the increased complexity of such process (§3.1.1). Therefore, few limitations appear in the gate last and nanowire last configuration when removing the sacrificial SiGe. As imaged in Figure 3.8, the absence of internal spacers also implies the absence of etch-stop layers in between the NWs. If large NWs or nanosheets are used following the simulation conclusions of the previous chapter (§2), the etch front cannot be uniform since the SiGe is accessed and etched longer at the edges than in the center of the nanosheet. Ultimately, the isotropic etch occurs deep under the SiN spacer and even into the S/D. Thicker spacers would be required to compensate, however, this is in opposition with the recommendations for the 7 nm node design.

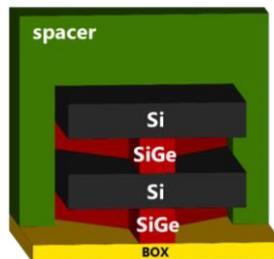


Figure 3.8 - Non parallel SiGe etch front is problematic in case of the absence of an etch stop layer [Gaben 2016 ECST].

A solution to this issue [Mertens 2016 VLSI] is to etch vertically the extensions and to proceed with a merging Si SEG (Figure 3.9a-c). Once the sacrificial gate is taken away (Figure 3.9d), the sacrificial SiGe can be removed selectively towards the Si RS/D with a safe over-etch margin (Figure 3.9e). Finally, the HKMG is isolated from the doped RS/D by the high-k layer (Figure 3.9f). However, this approach prevents the use of SiGe RS/D for inducing compressive strain advantageous for PMOS. Thus, reversing the etch selectivity and combining locally SiGe channels and SiGe S/D for PMOS is a solution to explore.

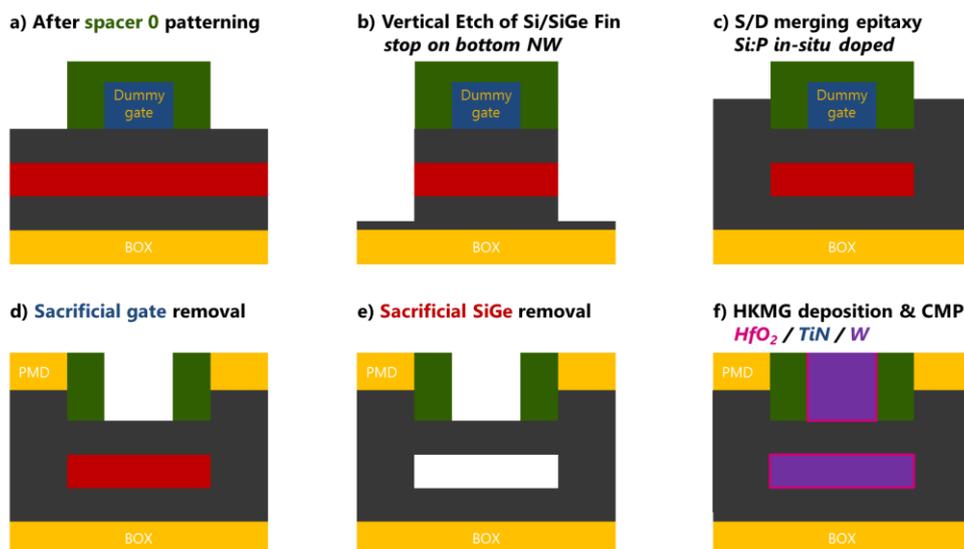


Figure 3.9 - Silicon S/D can be used as an etch stop layer during SiGe removal.

### NW last with HSQ sacrificial gate

Using HSQ in a NW last approach is also possible (Figure 3.10). However, the internal spacers then have to be built in the exact same way as with using a polysilicon sacrificial gate as revealed by Figure 3.10. Besides, the advantage of using HSQ for building self-aligned gate is lost in this case and thus, this approach presents less interest. Moreover, an integration based on HSQ introduces much larger differences with typical gate last integrations of FinFET. Consequently, increasing the complexity of the previously described NW last approach, by introducing HSQ sacrificial gates, was not justified at the beginning of this thesis project. Nevertheless, the modules independently developed for each integration can be assembled together in order to achieve this option. This will be discussed along with several other concepts in the following next chapter (§4.2).

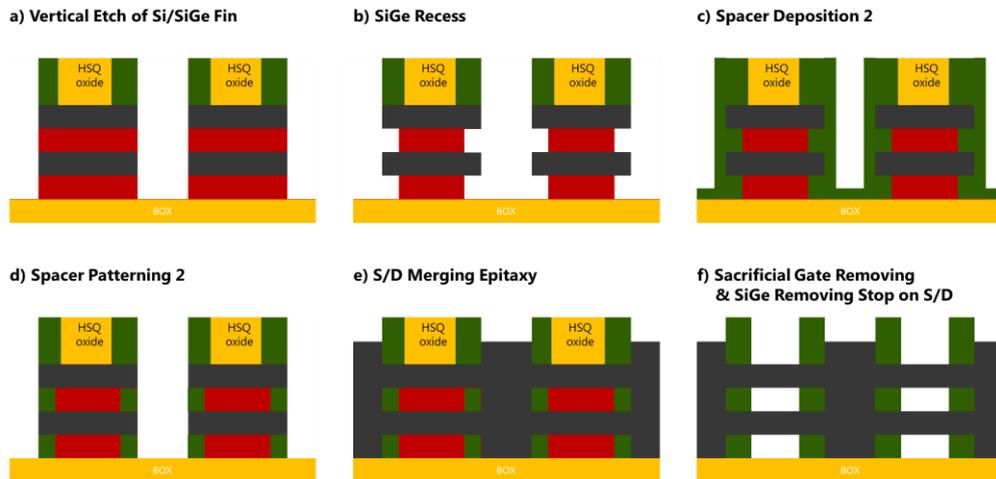


Figure 3.10 - NW Last option with HSQ sacrificial gates.

### NW first with polysilicon sacrificial gate

Two reasons prevent to combine polysilicon sacrificial gates with NW first option. First, in this configuration the polysilicon replaces the SiGe in between the suspended Si NWs resulting in a “NW last-like” structure. Thus, internal spacers fabrication remains similar to the NW last approach presented in §3.1.1. Secondly, the realization of suspended NWs in a NW first approach requires anchors on both sides of the NWs with extra cost in wafer surface occupation. Consequently, this combination seems non-optimized due to an increased complexity without any additional advantages such as self-aligned gates and internal spacers.

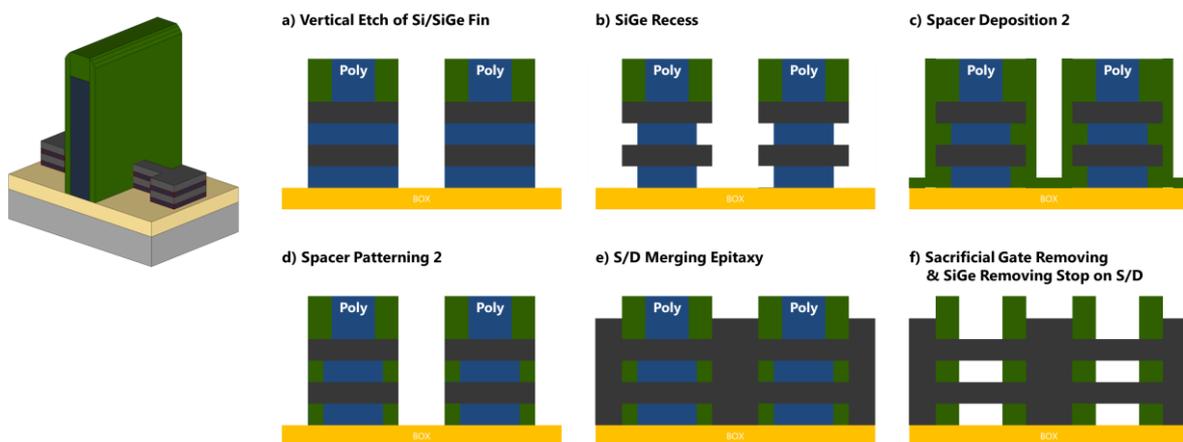


Figure 3.11 - NW First option with polysilicon sacrificial gate: polysilicon fills the space in between the NWs.

### 3.1.4. Conclusion

In summary, the two integrations recalled in Figure 3.12 remains interesting to develop. On one hand, the NW last approach due to its close proximity with a FinFET process flow has only four modules specific to SNWFETs (in blue on Figure 3.12). The NW first approach on the other hand, benefits from self-aligned gate and spacers, however at the price of one major additional development concerning the HSQ lithography (bold yellow on Figure 3.12). The other main developments are inherited from the NW last approach (blue) along with other minor adaptations from FinFET process flow (light yellow). Yet, the development of the HSQ lithography has offered to build several promising concepts to be developed in the last chapter (§4.2).

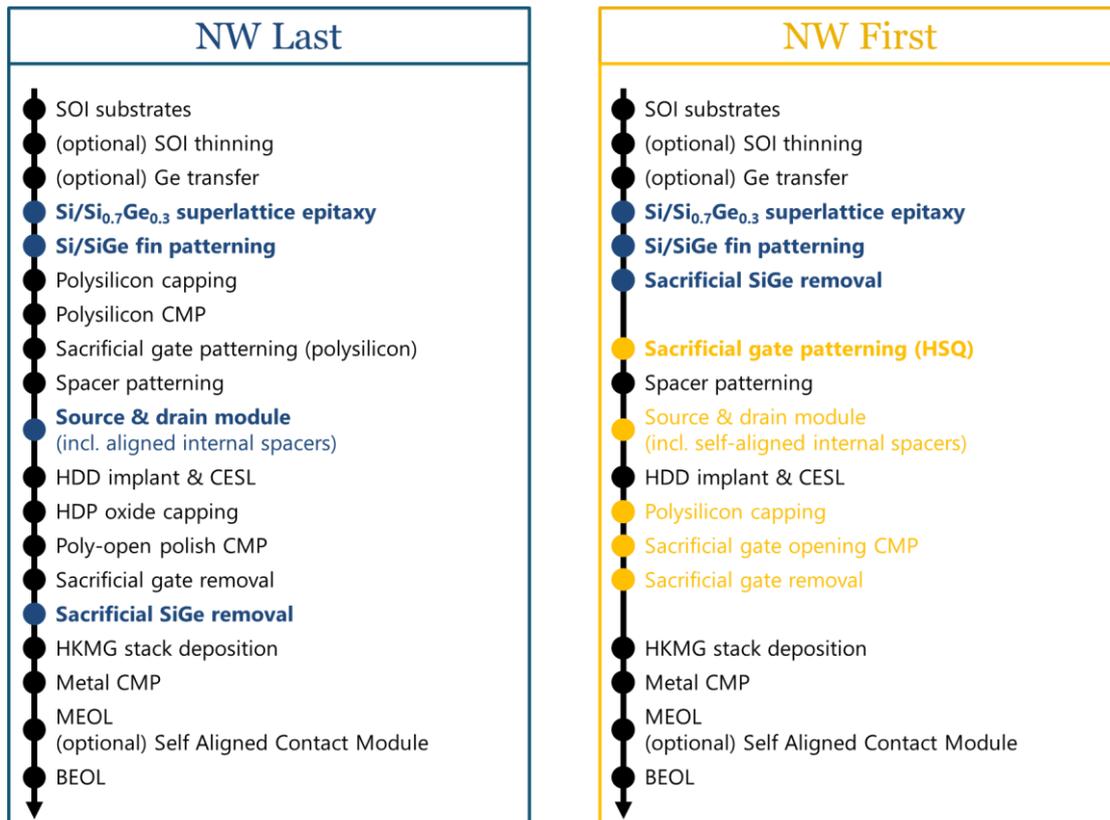


Figure 3.12 - NW last and NW first process flows. In blue the four major developments specific to the SNWFETs integration and in yellow the additional variation introduced by the NW first alternative.

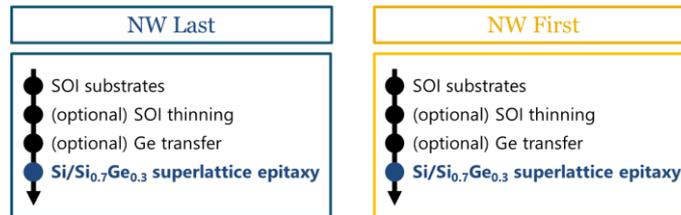
The following subchapters focus on five major process developments:

- first, the Si/SiGe superlattice epitaxy is provided in (§3.2) followed by
- Si/SiGe fin patterning (§3.3) both used in the two approaches (Figure 3.12)
- SiGe selective etching is described in (§3.4). Although the process is used in both alternatives (Figure 3.12), the selective removal of SiGe happens two times in NW last: first during the internal spacers fabrication and then for suspending the Si NWs within the gate cavity. Concerning the NW first, SiGe etching is usually performed only once and before the HSQ sacrificial gate patterning.
- the S/D with internal spacers for the NW last approach combining both epitaxy and sacrificial SiGe etching concerns is explained in (§3.5).
- the development of HSQ lithography to achieve self-aligned sacrificial gates and internal spacers is then presented in (§3.6).

Finally, the last subchapter is pointing out the specificities of the various CMPs for gate last integration, even though these are not specific to SNWFET (§3.7).

### 3.2. Si/SiGe superlattice

As observed in the introduction to SNWFETs (§1.3.4), silicon (Si) and silicon germanium (SiGe) materials are essential for the fabrication of stacked nanowires channels. On one hand Si and SiGe have similar lattice parameters allowing the heteroepitaxy of one above the other. On the other hand, a good etching selectivity can be achieved in between the two materials allowing SiGe to be used as a sacrificial layer for later forming the suspended Si NWs. In the following sub-chapter, Si/SiGe superlattice fabrication is related. However, to achieve on SOI the different “full GAA” and “mixed GAA” configurations proposed in the previous simulation chapter (§2), additional steps of SOI thinning and Ge condensation may be required first.



SOI substrates with a 145 nm BOX and 16 nm thick silicon layer are used. If the first layer of silicon is intended to be used in order to create the SNWFET bottom channel (trigate or  $\Omega$ -gate), the Si layer must be thinned down below 10 nm to obtain the performances required by the simulation of Chapter 2. Therefore, a cycle of thermal oxidation and of HF etching is performed.

The ellipsometry measurements in Figure 3.13 shows the 10 nm target was reached with a thickness variation below 1 nm. Although the impact of channel thickness variability still needs to be fully evaluated on SNWFETs electrical performances, the present variation should have very limited impact on performances as compared to other processes variability. Also, few wafers increase the range of the batch since 3 over 25 are slightly below 9 nm. This might be due to a tool ramping up effect (for reaching a stable temperature) or due to a slight non-uniformity of the temperature in the furnace affecting differently the wafers depending on their position in the holder. Finally, although SOI wafers with thin BOX and thin SOI layer are already available for manufacturing, the higher cost of these substrates is not relevant for the present demonstrations.

Layer	Mean (25 wafers)	3 $\sigma$	Range	Min	Max
BOX (oxide)	145.7 nm	0.7 nm	1.5 nm	144.8 nm	146.3 nm
SOI (silicon)	9.9 nm	0.7 nm	2.1 nm	8.5 nm	10.5 nm

Mean range per wafer (25 wafers)	3 $\sigma$	Layer
0.5 nm	0.2 nm	BOX (oxide)
0.7 nm	0.3 nm	SOI (silicon)

Figure 3.13 - Effect of SOI thinning on an entire lot of 25 wafers: initial SOI was 16 nm and target was 10 nm.

Once the SOI has been thinned to the proper dimension, the successive epitaxies of Si<sub>0.7</sub>Ge<sub>0.3</sub> can be carried out on top. As shown in Figure 3.14, the number of Si layers also determines the final number of NWs in the stacks once the sacrificial SiGe is etched away. As discussed in §1.3.4 and in §1.2.3, the epitaxy of such superlattice have been previously studied in LETI for the fabrication of MCBFETs [Ernst 2006], and SON [Skotnicki 1999]. These processes have been successfully transferred on the recent 300 mm tool available in LETI (Centura 300).

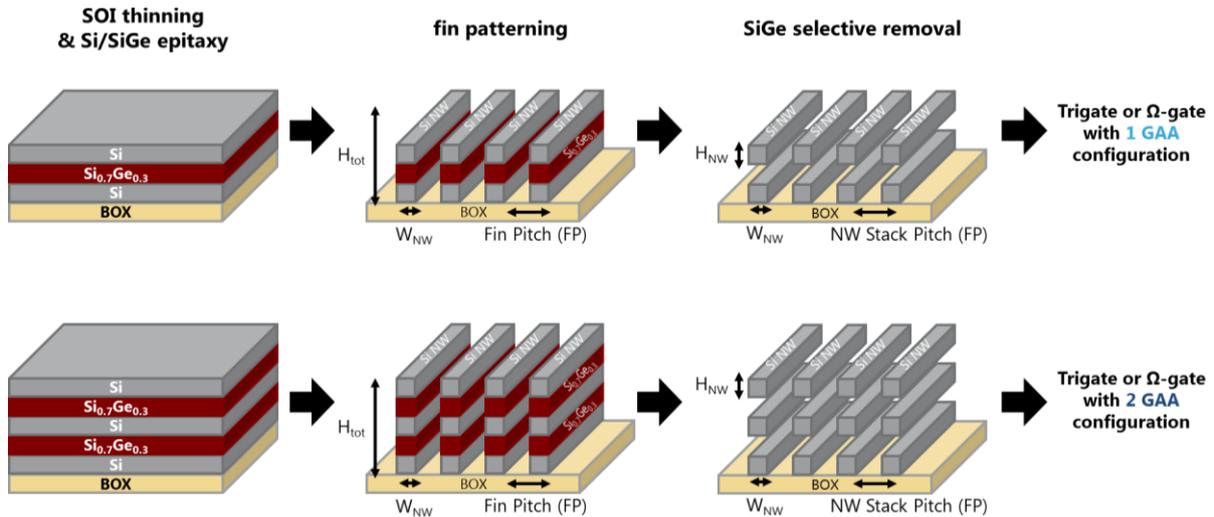


Figure 3.14 – Schematic of mixt trigate and 1 or 2 GAA configurations formed from thin SOI layer (In the case of gate last integration of SNWFET, sacrificial removal is not necessarily performed just after Si/SiGe fin patterning).

Epitaxy process consists in the deposition of a single-crystalline layer onto another crystalline structure. Hence, the new layer is forced to take the exact same lattice parameter as the one underneath. Consequently, in the case of heteroepitaxy, for example when growing SiGe on Si, the naturally higher lattice parameter of SiGe induces a compressive stress into the SiGe when adapting to the relaxed crystalline Si as shown in Figure 3.15. As observed on trigate NWFETs in §1.3.2, inducing stress into the channel highly improve carrier mobility. This is the reason why strain mappings are closely monitored in this thesis especially concerning the compressive strain for PMOS improvement.

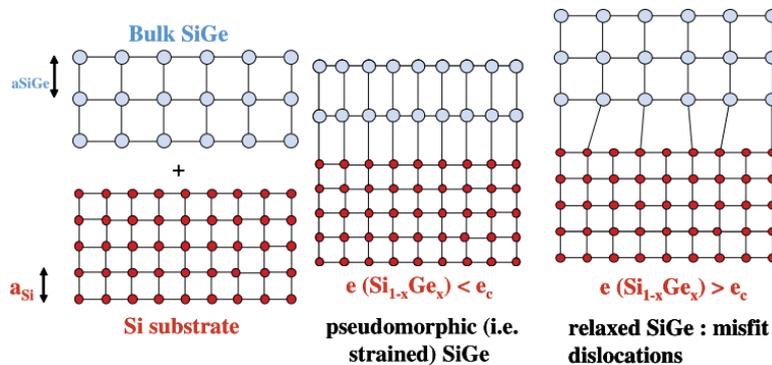


Figure 3.15 - Heteroepitaxy of SiGe on Si: lattice mismatch, strain and misfit dislocations introduced once the elastic energy of SiGe is higher than the critical energy  $e_c$  [Hartmann 2016].

A downside is the plastic relaxation effect that happens once the apparition of misfit dislocations becomes energetically favorable to minimize the elastic energy introduced by the lattice mismatch [Hartmann 2016]. Therefore, this can be a limitation to the maximal thickness of the epitaxy and to the number of channel that is possible to stack [Hartmann 2008 ECST]. In the framework of this thesis, the Si and SiGe layers are in between 7 nm and 12 nm stacked up to 5 levels with no significant defects.

As shown in Figure 3.14, the release of the stacked NW channels is carried out by removing the sacrificial SiGe. As it will be observed in the following next section, SiGe versus Si etching selectivity can be enhanced by increasing the Ge content in the SiGe alloy (§3.4). However, increasing Ge

concentration may also generate crystalline defects due to high lattice mismatch and therefore this limits the number and the total thickness of the NW stacks. Thus, the Ge percentage becomes a trade-off in between etching selectivity and epitaxy quality. Consequently, the Ge content was restrained to  $\text{Si}_{0.7}\text{Ge}_{0.3}$  and  $\text{Si}_{0.5}\text{Ge}_{0.5}$  and total epitaxy thickness limited to 60 nm to fit under a given gate height.

In this thesis project, we remind that SOI substrates are used. Bulk wafers could also be used but the absence of BOX must be taken into account as both the epitaxy growth speed and the internal strain are then influenced. Although intrinsic channels are preferred according to Chapter 1, in-situ doping with boron, phosphorus or carbon can also be performed to obtain doped channels [Hartmann 2005 jCG], [Hartmann 2008 ECST]. Finally, one can notice that the epitaxy process is influenced by partial pressures, temperature, precursors, doping precursors in case of in-situ doping and by the nature of the substrate and of the surfaces.

Since SOI substrates are used, and since according to the simulations of Chapter 2 the most favorable gate configuration is the full GAA, then the superlattice epitaxy must be started from a SiGe layer as shown in Figure 3.16. To this purpose, a Ge condensation technique can be performed prior to the Si/SiGe superlattice epitaxy. A first epitaxy of  $\text{Si}_{0.7}\text{Ge}_{0.3}$  is carried out on top of the thinned SOI. An annealing is then performed so the atoms of Ge are pushed into the Si underneath as the Si is preferentially oxidized. A final HF-based process removes the created  $\text{SiO}_2$  layer above the new SiGe layer and then only the superlattice epitaxy is performed on top of the SGOI.

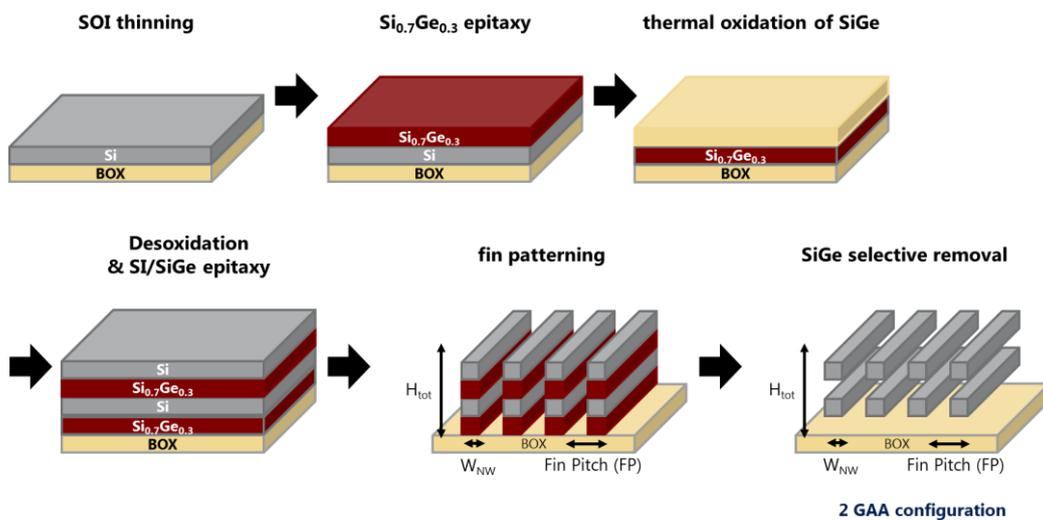


Figure 3.16 – Schematic of Ge condensation process followed by Si/SiGe/Si epitaxies to form a dual GAA configuration (in the case of gate last integration of SNWFET, SiGe sacrificial removal is not necessarily performed just after Si/SiGe fin patterning).

For all these epitaxy process, the growth chemistry involves  $\text{SiH}_2\text{Cl}_2 + \text{GeH}_4$  for the SiGe layers and  $\text{SiH}_4$  for the Si ones at 20 Torr and  $650^\circ\text{C}$  [Hartmann 2012 TSF]. Figure 3.17 reports the statistical results of a full batch of 25 wafers used in the fabrication of dual GAA devices after Ge condensation and successive epitaxies of Si/SiGe/Si. The Ge condensation process increased the thickness variation over the wafer to 1.4 nm. The wafer to wafer variability is similar to what was obtained after the SOI thinning step. Due to extra consumption of silicon during thermal oxidation for Ge condensation, the final SGOI layer is 8 nm thick while the SOI was initially 10 nm thick (Figure 3.13). As shown in the TEM image of the inset in Figure 3.17, 14 nm Si, 8 nm SiGe and 15 nm Si have been epitaxied on top of the 8 nm SGOI seed layer. The thicker than required by simulation Si layers were intended to endure a low

selectivity process of sacrificial etching. Figure 3.17 presents a 45 nm thick Si/SiGe stack with a thickness range increased to 5 nm as compared as SGOI thickness variation. Monitoring measurements were realized with ellipsometry for process control of 14 to 49 points per wafer. Although the precision of such method is lower than the X-ray diffraction (XRD) technique, ellipsometry is also much faster. XRD is therefore reserved for epitaxy tool process calibration.

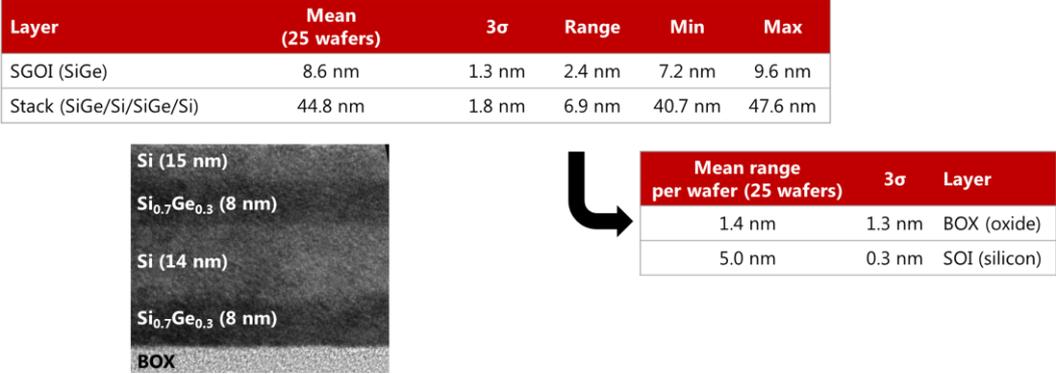


Figure 3.17 – Effect of Ge condensation into a 10 nm thick SOI aiming for a 8 nm SGOI and after the epitaxy of the Si/SiGe/Si layers for a targeted total height of 45 nm.

The Ge condensation technique have been commonly used in the fabrication of 14 nm technology devices on SOI with SiGe channels for PMOS [Cheng 2012] as well as for building trigate NWFETs [Nguyen 2014 S3S]. By masking selected areas of the wafer and using selective epitaxial growth (SEG), various combination of Si and SiGe devices can be cointegrated. For example, trigate NWFETs have been fabricated in such a way with no penalty on the electrical performances [Nguyen 2014 IEDM]. Therefore, this technique can be safely used for an industrialization of SNWFETs.

As previously shown in Figure 3.15, the lattice mismatch in between Si and Si<sub>x</sub>Ge<sub>1-x</sub> layers induces stress. As measured and discussed in the first chapter with non-stacked NWFETs (§1.3.2), appropriate strain improves carrier transport in NW channels. Based on this idea, multiple combinations can be obtained favorizing either tensile Si for NMOS channels when starting from strained SOI (sSOI) substrate (Figure 3.18a) or else compressive SiGe channels for PMOS after Ge enrichment of the SOI layer (Figure 3.18b). As previously written, no defects are visible in the layers.

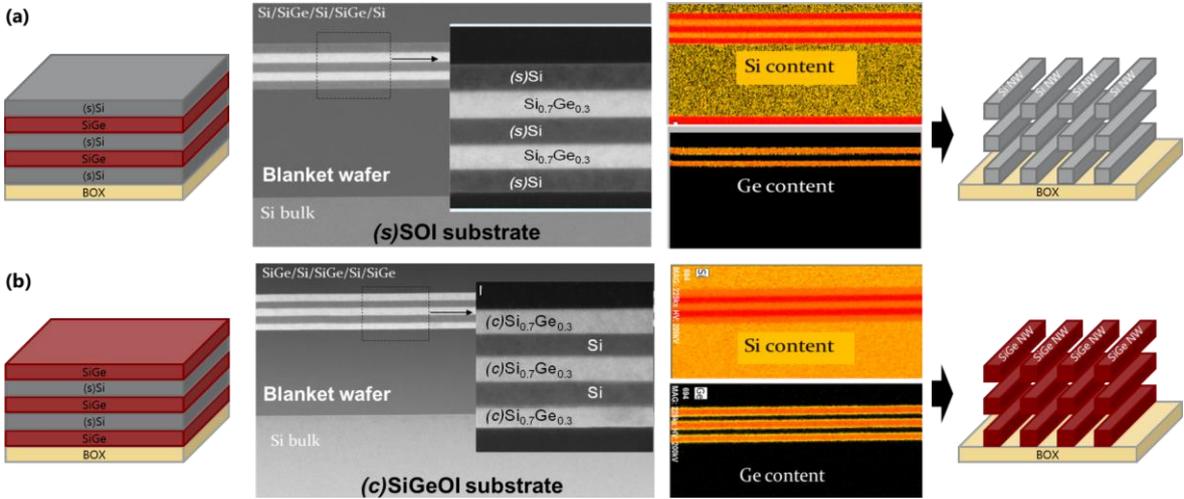


Figure 3.18 - TEM and Energy Dispersive X-ray spectroscopy mappings of Si/SiGe superlattices with (a) three levels of tensile strained Si layers and (b) three levels of compressive strain SiGe layers [Barraud 2016 IEDM].

For verification, strain mappings can be extracted by precession electron diffraction (PED) on a TEM. A 3D finite element method (FEM) was developed in order to fit the Ge fractions and to take into account the lamellae thicknesses, some elastic relaxation in between the different layers and the influence of free surfaces at the edges of the samples [Reboh 2013 APLM], [Lubk 2014]. Figure 3.19 presents the results for the configuration of Figure 3.18a starting from sSOI substrate. Si layers all present -0.4% vertical stress and a 0.8% in-plane deformation. The measurements show a complete report of the lattice parameter and of the strain throughout the identical layers in the entire superlattice.

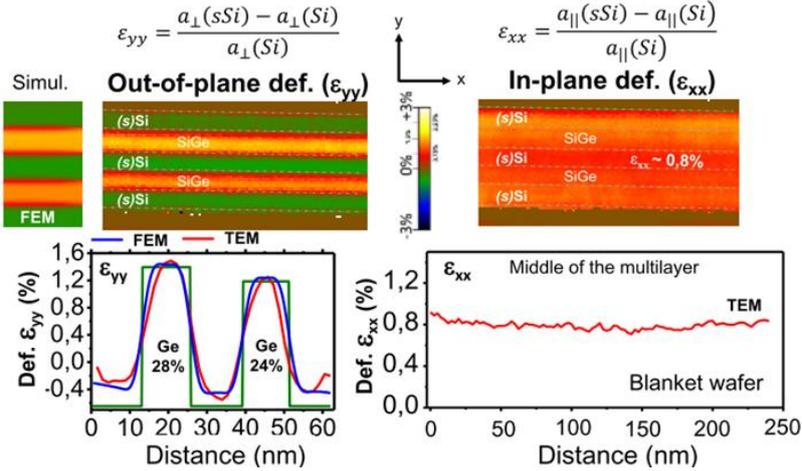


Figure 3.19 - In and out of plane deformation maps of Si/SiGe stacks on full 300 mm wafers starting from 1.4GPa sSOI substrates. The extracted and simulated values also show good correlation [Barraud 2016 IEDM].

Hence, these results are promising for the SNWFET technology but only if the strain is not fully relaxed during the integration, especially after the Si/SiGe fin patterning and SiGe sacrificial removal. Therefore, the following next subchapter focuses on the etching of the Si/SiGe fins.

### 3.3. Si/SiGe fins patterning

The Si/SiGe fin patterning process has been developed in [Barnola 2008]. The developed resist must be trimmed in  $\text{Cl}_2/\text{O}_2$  plasma prior to HBr curing in order to bypass the 80-nm minimal feature limitation of the tool. The nitride-oxide hard-mask (HM) is then opened using  $\text{CF}_4/\text{CH}_2/\text{F}_2/\text{O}_2/\text{He}$  plasma. Once the top of the Si/SiGe superlattice is reached, the stack is patterned using  $\text{Cl}_2/\text{HBr}/\text{O}_2$ .

The etching process can be monitored following the emission ray of germanium in Ge-based reaction byproducts (265 nm wavelength). Figure 3.20 shows the strong delimitation of each Si-SiGe layer interface. This figure also underlines the importance of epitaxy uniformity. Epitaxy process “A” presents a 20-nm wafer range which contributes to enlarge the Ge emission lines respectively to the process “B” having a 3-nm range. Failure in detecting the bottom of the Si/SiGe superlattice may result in a significant BOX over etch. Any range and variability is detrimental as it is cumulated through the future process steps such as CMP and gate patterning.

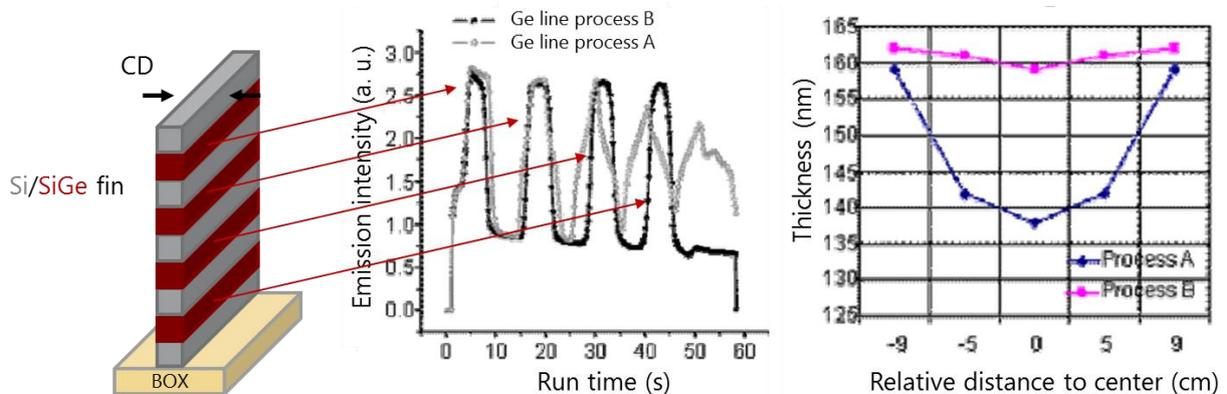


Figure 3.20 - Ge emission lines and superlattice thicknesses for a good uniformity in the epitaxy thickness (process B) and a bad uniformity (process A) as in [Barnola 2008].

To limit BOX consumption, a two-step process was evaluated in [Barnola 2008]. The main etch step is stopped during the etch of the bottom Si layer and a “soft landing” step is added to stop on the  $\text{SiO}_2$  underneath. However, this approach led to Si/SiGe fin profiles resulting in a difference of 8 nm in between the top and the bottom NW CDs. In order to obtain vertical etching profiles, the main etch was applied all the way down to the BOX sacrificing a few nanometers of  $\text{SiO}_2$ . Therefore, this was turned into an advantage for turning the bottom trigate channel into an  $\Omega$ -gate as recommended by simulations for improving gate control over this channel.

As also mentioned in chapter 2, device footprint is critical in SNWFET technology. In order to overcome the performances of FinFETs, the NW stacks must be arranged as closely as possible. Hence, an adaptation of the process developed in [Barnola 2014 SPIE] and already used to perform the 35-nm pitch  $\Omega$ -gate NWFETs presented in §1.3.3 has been conducted. The TEM images of Figure 3.21 show 60 nm high Si/SiGe fins with 3 level of Si NWs organized in arrays of 40 nm pitch.

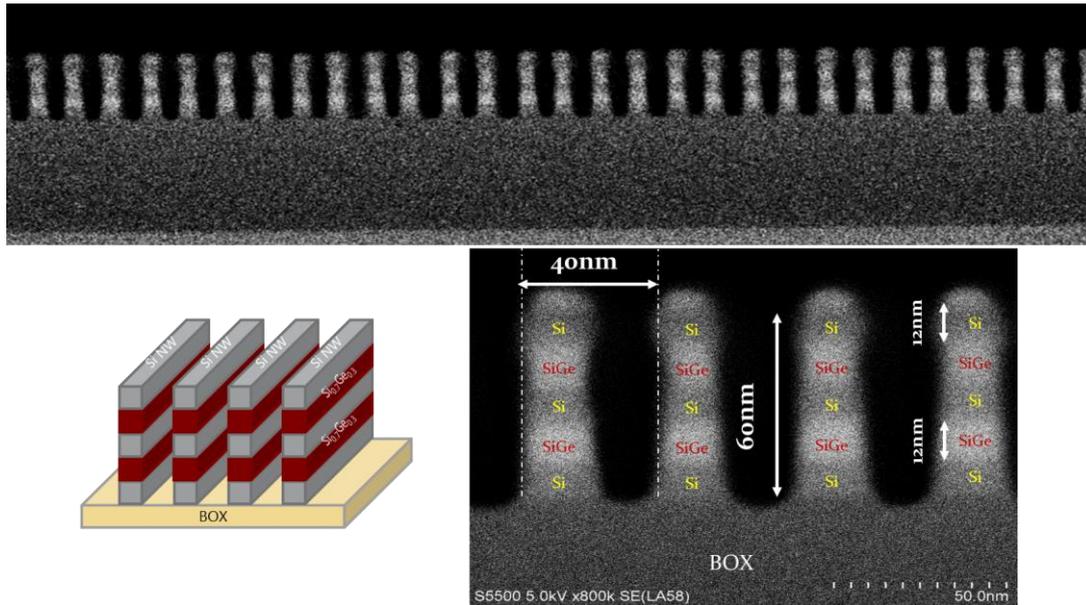


Figure 3.21 – Cross-sectional TEM images of 60 nm high fins of Si/SiGe/Si/SiGe/Si patterned in arrays of 40 nm pitch using SIT process [Gaben 2015 SSDM].

Figure 3.22 shows the Precession Electron Diffraction (PED) deformation mappings of a Si/SiGe/Si/SiGe/Si fin post etching. A deformation of 0.8% (1.4 GPa stress) is still observed in the strained Si layers (a strained SOI substrate has been used for this demonstration). Even if relaxation is observed in the cross section (Figure 3.22.right) due to free edges, the longitudinal strain is maintained after fin patterning according to Figure 3.22.left. This result is promising for SNWFET technology which is likely able to benefit from stress engineering to enhance carrier mobility.

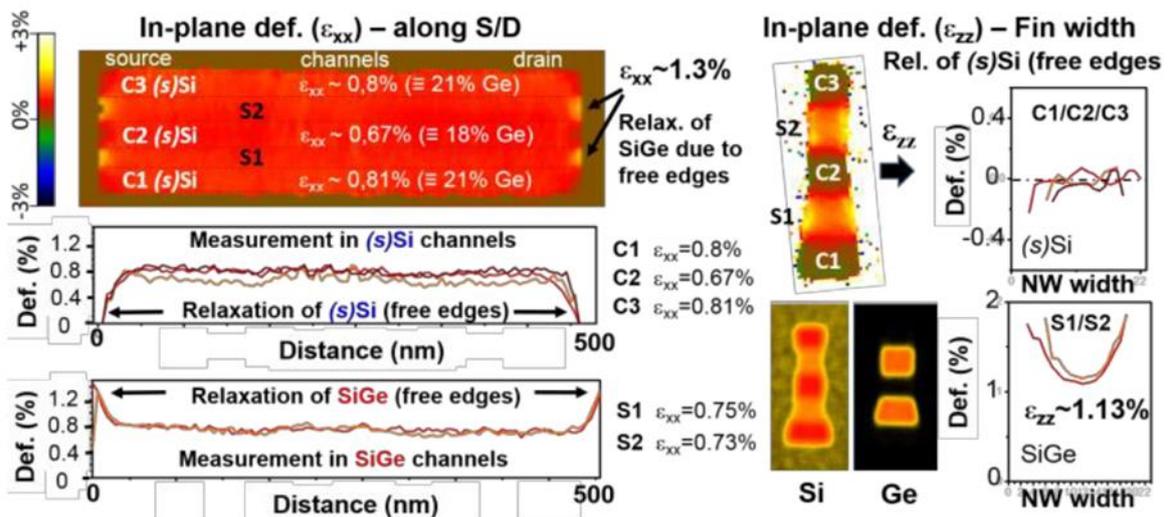


Figure 3.22 – (left) In-plane ( $\epsilon_{xx}$ ) PED deformation maps of Si/SiGe/Si/SiGe/Si fins post etching. A deformation of 0.8% in the sSi layers is maintained (1.4 GPa stress) and (right) Deformation mappings and profile for ( $\epsilon_{zz}$ ). Strain relaxation effects are observed in this direction due to free edges [Barraud 2016 IEDM].

Finally, various Si/SiGe fin dimensions were obtained from 15 nm to 100 nm large and from 100 nm to 1  $\mu\text{m}$  long as designed on the lithography mask. However, SiGe remain sacrificial and the question of its selective etch remain crucial for both NW first and NW last approaches.

### 3.4. SiGe selective removal

As recalled in Figure 3.23, the selective etching of SiGe is performed in different steps of the two investigated integrations: to suspend the Si NWs in both NW first and NW last approaches as well as inside the NW last S/D module in the NW last integration. In the latter, cavities are etched into the Si/SiGe stacks for placing the internal spacers (see next subchapter §3.5). Hence, the selective etching of sacrificial SiGe towards Si must be investigated.



Figure 3.23 – Steps involving SiGe selective removal in NW first and in NW last approaches (red color).

Etching selectivity in such superlattices is crucial and tunnel enlargement may result in Si channel thickness variation as shown in Figure 3.24 due to the tunnel entrance enlargement. For process characterization purposes, only large pads of Si/SiGe superlattice are observed under SEM and TEM cross sections. The etching from can also be observed by transparency on top view SEM images.

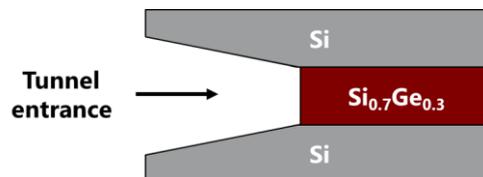


Figure 3.24 – Tunnel entrance enlargement in Si/SiGe superlattice.

The present section provides an overview of the three different approaches for the selective etching of SiGe that have been developed in LETI during the past decade. Plasma and wet etching are then experimented on the actual NW stacks. The performance of optimized process is then observed for both NW last and NW first integration schemes.

#### Dry etch of SiGe: plasma etching

After a wet pre-treatment for removing native oxide, Si/SiGe stacks are placed in a remote plasma chamber. Active species are brought into the etching chamber without any ion bombardment (anisotropic etching) and isotropic etching can take place. Using pure  $\text{CF}_4$ , Si and Ge atoms are etched from the surface forming  $\text{SiF}_x$  and  $\text{GeF}_y$  volatile products [Borel 2004]. Since Si-Si binding energy is higher than Si-Ge one (2.31 eV and 2.12 eV respectively), Ge atoms are preferentially removed. Etch rate is therefore increased with Ge content quadrupling when opting from 25% instead of 15% Ge. However, SiGe etch rate slows down and saturates above a concentration of 30%.

The selective c-Si<sub>1-x</sub>Ge<sub>x</sub> alloy etching is piloted by the  $\text{CF}_4$  flow, the chamber pressure and the plasma source power. The optimized process presented in [Salvetat 2008 ECST] also showed with AFM measurements that this process does not introduce any additional roughness. Besides, etch rate is also confirmed to be poorly dependent on Ge concentration above 20% concentration up

to 40% (Figure 3.25a). Finally, selectivity depends on etching time since the tunnel entrance is not enlarged as much as the tunnel depth is increased once a permanent regime is reached. Besides, the etch is not affected by the crystallographic plane orientation according to the SEM image of Figure 3.25b.

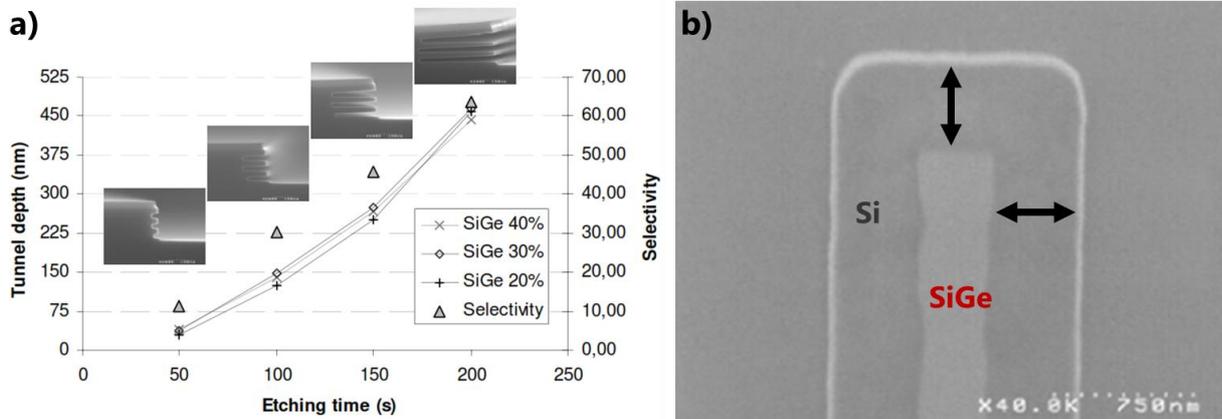


Figure 3.25 - (a) Tunnel depth and selectivity as a function of etching time and Ge content for a bulk Si/SiGe 20 nm/Si 40nm/SiGe 20nm/Si 40nm/SiGe 20nm/Si 40nm superlattice. (b) top view SEM showing a uniform etch front by transparency (isotropic etch) [Salvetat 2008 ECST].

### Dry etch of SiGe: gaseous HCl etching

Gaseous HCl etching can be performed in-situ with the epitaxy tool [Salvetat 2008 ECST]. The selectivity is obtained thanks to the differences of chemical activity in between Si and SiGe depending on the pressure and temperature conditions [Destefanis 2008 ECST]. Ge fraction or increasing temperature both improve the Si and SiGe etch rate. However, the extracted activation energies evidence a decrease of the selectivity with increasing the temperature. Concerning the Ge percentage, 20% appears too low to achieve the required selectivity for carving 300 nm deep cavities. In contrast, 30% (40%) concentration provide a selectivity of 100 (150 respectively) much higher than with plasma etching (60). This is the opposite of the etch rate which falls from 100 nm/min with plasma down to 10 to 30 nm/min with HCl.

In Figure 3.26a, the cross-sectional SEM image evidences a slight bottom-up effect: deeper cavities are obtained at the bottom of the stack as the opposite top-down effect was obtained with plasma etching. Moreover, the process evidence a strong anisotropy regarding crystalline orientation: the  $\langle 100 \rangle$  directions are etched about 10 times faster than the  $\langle 110 \rangle$  directions (Figure 3.26b).

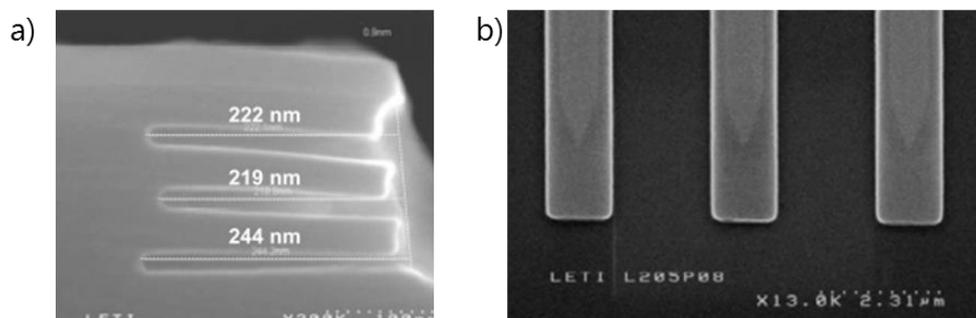


Figure 3.26 - bulk Si/SiGe30% 20 nm/Si 40nm/SiGe30% 20nm/Si 40nm/SiGe30% 20nm/Si 40nm superlattice after HCl etching of SiGe: (a) cross-sectional SEM image showing the bottom tunnel is deeper than the upper ones and (b) a top view SEM image in which the cavities carved into SiGe are visible by transparency through the top silicon layer [Salvetat 2008 ECST].

## Wet etch of SiGe

Selectivity is based on the different oxidation and etching kinetics of SiGe and Si [Salvetat 2008 ECST]. Therefore, the mixture must contain at least one etch agent such as HF and one oxidant agent such as  $H_2O_2$  or  $HNO_3$ . Adding an organic acid such as acetic acid increases both the etch rate and the selectivity [Carns 1995]. Increasing the dilution in deionized water improves the selectivity. After an optimum point, the etching of Si and SiGe decrease again until totally stopped [Salvetat 2008 ECST]. A bottom-up effect has been also observed with about 20% higher etch rate for the bottom cavity. Two specific points require investigation when working in wet chemistry. Firstly, the etch rate neither the selectivity are significantly affected by bath aging even after 26 days. Secondly, capillarity forces seem too weak to cause collapsing of the 40 nm thick silicon slabs even with 450 nm tunnel depths.

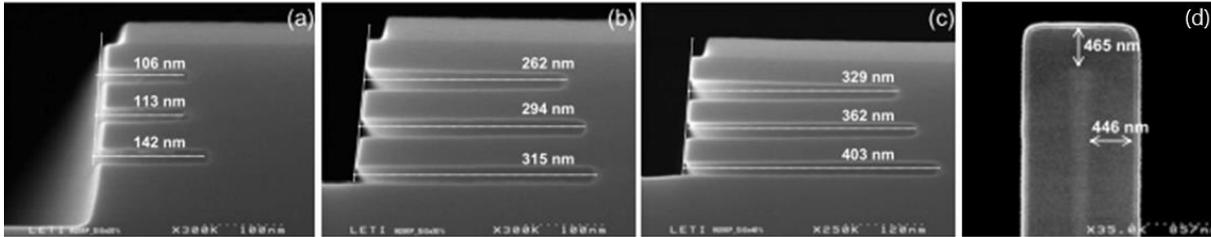


Figure 3.27 - Cross section SEM images after 2 min wet etching of SiGe in a bulk Si/SiGe 20 nm/Si 40nm/SiGe 20nm/Si 40nm/SiGe 20nm/Si 40nm superlattice with (a) 20%, (b) 30% and (c) 40% of Ge fraction. (d) top view SEM image showing the isotropy of this process.

## Updated results

The previous results obtained for hundreds of nanometers deep cavities are good indications for the potential of each process. Nevertheless, switching for large and thin nanosheets requires further investigation. Indeed, for such thin NWs ( $H_{NW} = 6 \text{ nm}$  to  $12 \text{ nm}$ ), the tunnel entrance enlargement (Figure 3.24) becomes of the order of magnitude of the Si NW thickness. Moreover, the processes must be adapted to 300 mm tools. Silicon NW release was studied in dry and wet chemistry on NW stacks with the following thicknesses: Si 14 nm/SiGe 8 nm/Si 14 nm/SiGe 8 nm/BOX 145nm. Thicker than required silicon layers were epitaxied (7 to 8 nm thick channels are recommended by the simulations of chapter 2) in anticipation for some unwanted silicon consumption. A Lam Versys tool was used with  $CF_4$  chemistry and optimized conditions after removing the native oxide in a 1% HF solution. TEM images of Figure 3.28 after 8s and 10s of main etch show that the bottom NW thicknesses are reduced from 14 nm down to 7 nm and 6 nm respectively. Etching rate also seems slightly slower for the top SiGe layer than for the bottom one in opposition with the observations of [Salvetat 2008 ECST] for plasma etching likely due to the presence of the BOX.

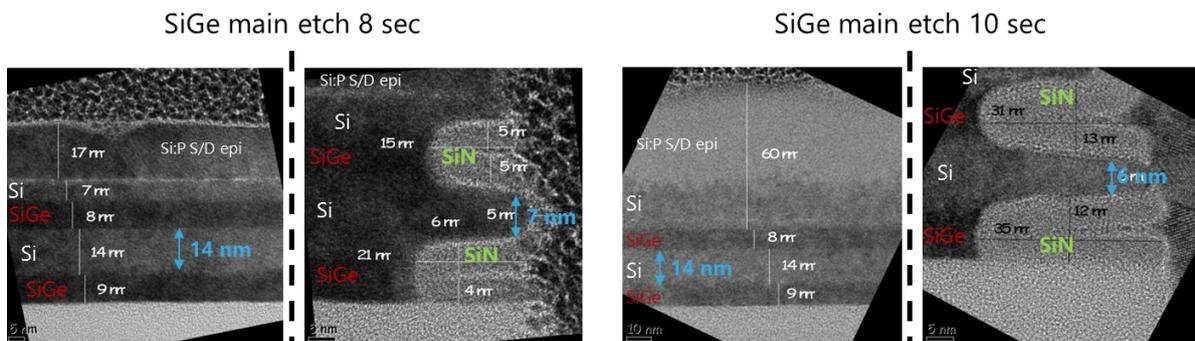


Figure 3.28 - TEM images of Si/SiGe stack inside the anchor (left) and at the edge of the stack (right) after 8 sec and 10 sec of main etch. (For demonstration purposes, SiN spacer was also deposited and anisotropically etched away from the top NW and a Si:P SEG epitaxy was performed)

In parallel, a wet chemistry was proposed with a new mixture optimized from accumulated experience on related structures (see previous subsections). Wafers are manually dipped into the mixture, rinsed in deionized water and dried in neutral atmosphere. 30% and 45% Ge concentrations were studied in Si 7 nm/Si<sub>1-x</sub>Ge<sub>x</sub> 8 nm/Si 7 nm/Si<sub>1-x</sub>Ge<sub>x</sub> 8 nm/Si 7 nm/BOX 145 nm superlattices. Etch rates are reported in Figure 3.29 along with a cross-sectional SEM image. In accordance with previous work [Salvetat 2008 ECST], SiGe etch rate is increased with Ge content.

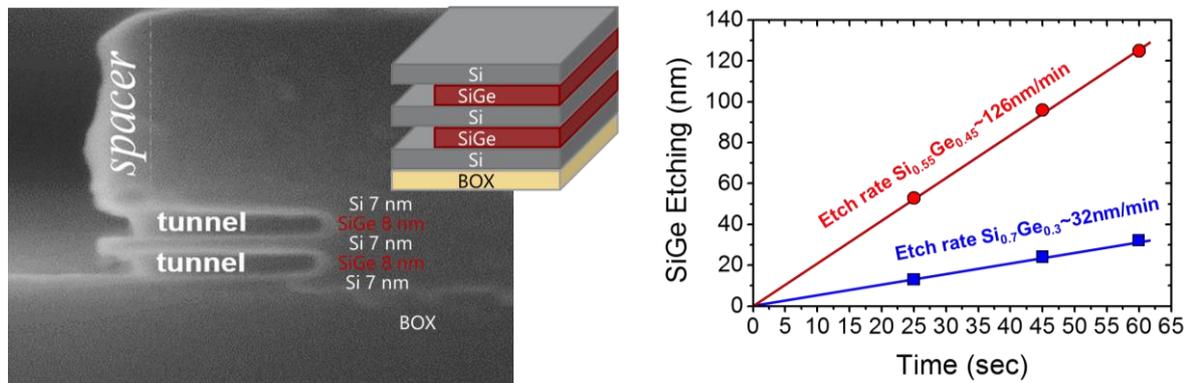


Figure 3.29 - SiGe selective etching: SEM cross-sectional image of a superlattice after SiGe etching (left). Etch rate as a function of Ge content in SiGe layer (right). The stack is made of Si 7 nm/Si<sub>1-x</sub>Ge<sub>x</sub> 8 nm/Si 7 nm/Si<sub>1-x</sub>Ge<sub>x</sub> 8 nm/Si 7 nm/BOX 145 nm layers.

The etching depth is usually measured with top view SEM imaging since the SiGe etch front is visible through the top silicon layer as shown on Figure 3.30. In this example, the stack is Si 14 nm/Si<sub>0.7</sub>Ge<sub>0.3</sub> 8 nm/Si 14 nm/Si<sub>0.7</sub>Ge<sub>0.3</sub> 8 nm /BOX 145 nm. Hence, measurements shows that the wet etch rate is slightly affected when switching for different layer thicknesses since 39 nm/min has been observed on the structure of Figure 3.30.

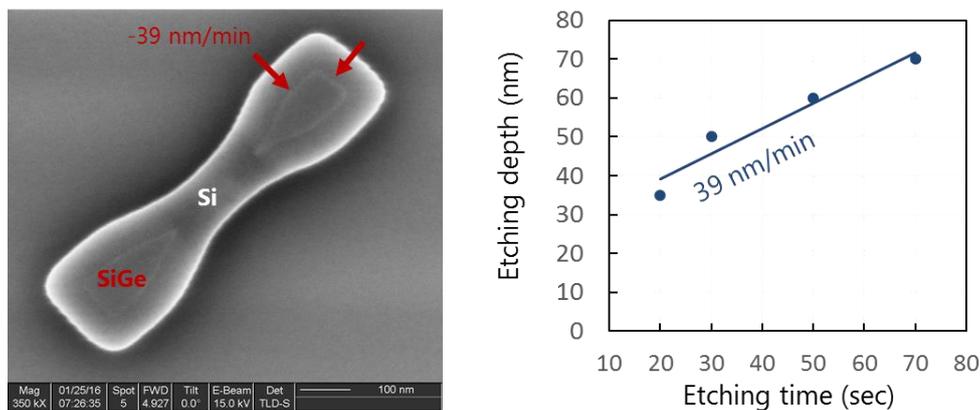


Figure 3.30 - SiGe selective etching: SEM top view of a NW stack (left) and measured etch rate (right). The 70 nm large stack is made of Si 14 nm/Si<sub>0.7</sub>Ge<sub>0.3</sub> 8 nm/Si 14 nm/Si<sub>0.7</sub>Ge<sub>0.3</sub> 8 nm /BOX 145 nm.

Subsequently, the question of the collapsing arises: what is the influence of the NW geometry and environment on the stacks integrity?

### Structural integrity of the NW stacks

Collapsing may be a limitation in such architectures featuring suspended features. The NW first approach is obviously more sensitive to this effect as the length of the suspended NWs is longer than in the NW last approach. Indeed, the maximal length in NW last alternative where the NW are suspended corresponds to the gate length (§3.1.1). Within the NW first approach, hundreds of nanometer long NWs are released in the early stages of the integration, suspended in between SiGe lateral anchors. To minimize the wafer area lost for these anchors, the NW must be as long as possible (see chapter 4). Figure 3.31 show SEM images of 150 nm and 800 nm long stacked channels.

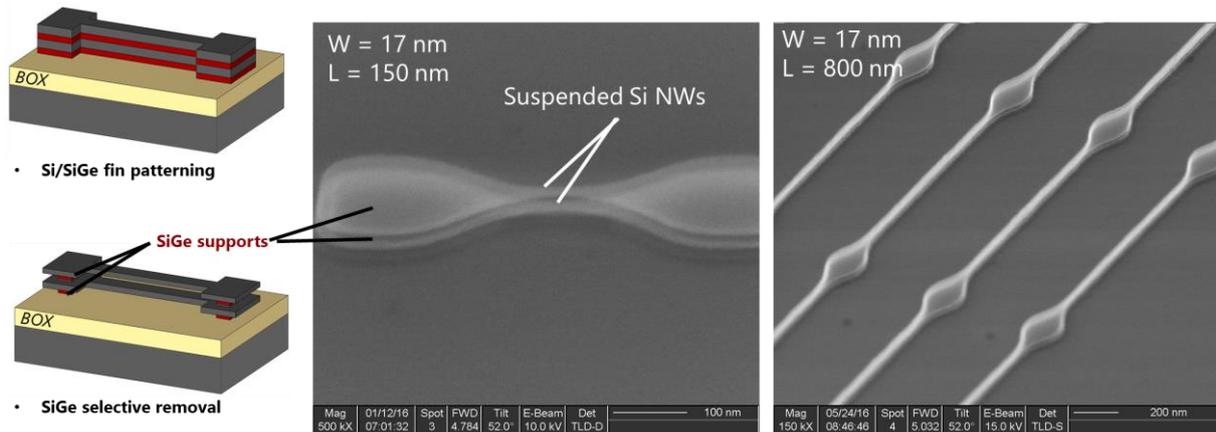


Figure 3.31 – SEM images of arrays of stacked NW: 800 nm long dual channels maintained by Si/SiGe anchors.

Nevertheless, the results of the observations are often affected by SEM charging which occurs during image acquisition with elevated acceleration voltages causing pattern collapsing. A complete study with TEM images is therefore required for an extended comprehension of the collapsing mechanisms.

In the meantime, an analytic model was used to describe the behavior of these stacked silicon slabs by means of the non-linear Euler equation (Eq. 3-1), [Gaben 2016 SNW].

$$\frac{H_{NW}^2}{12} \cdot \frac{d^2w}{dx^2} + \left( \frac{\sigma_{NW}}{E_{NW}} - \frac{1}{2 \cdot L_{NW}} \cdot \int_0^L \left( \frac{dw}{dx} \right)^2 dx \right) \cdot w = 0 \quad (Eq. 3-1)$$

The structure is described by clamped-clamped NWs (Figure 3.32), with  $H_{NW}$ ,  $L_{NW}$  the NW height and length respectively,  $L_{SiGe}$  the initial support length,  $E_{NW}$  the Young modulus,  $\sigma_{NW}$  the in-plane compressive stress and  $w(x)$  the vertical deformation of the beam as a function of the position  $x$ .

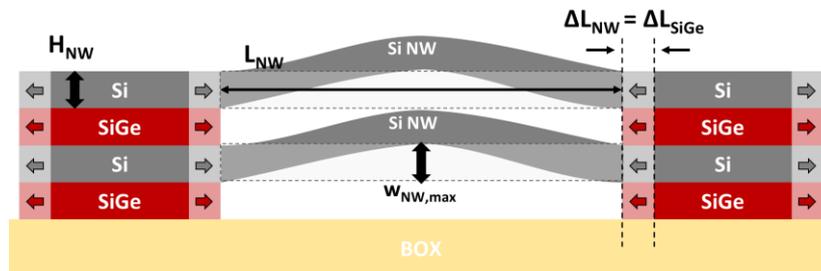


Figure 3.32 - Suspended NW channels modeled as clamped-clamped beams. The SiGe relaxation can induce the deformation of the beams.

The NWs remain straight as long as  $\sigma_{NW}$  stays below the critical value, known as the first Euler load  $\sigma_{Euler}$  (Eq. 3-2), corresponding to the eigenvalue of (Eq. 3-1).

$$\sigma_{NW} \leq \sigma_{Euler} = \frac{E_{NW} \cdot \pi^2}{3} \frac{H_{NW}^2}{L_{NW}^2} \quad (Eq. 3-2)$$

Assuming the NW stress is induced by SiGe stress relaxation, we have the following relation (Eq. 3-3):

$$\Delta L_{NW} = \Delta L_{NW} \Leftrightarrow \varepsilon_{SiGe} \cdot L_{SiGe} = \varepsilon_{NW} \cdot L_{NW} \quad (Eq. 3-3)$$

Hence, it comes the following condition on SiGe stress (Eq. 3-4):

$$\sigma_{SiGe} \leq \frac{E_{SiGe} \cdot \pi^2}{3} \frac{H_{NW}^2}{L_{NW} \cdot L_{SiGe}} \quad (Eq. 3-4)$$

Once  $\sigma_{SiGe}$  exceeds this critical value, the deflexion of the buckled nanowire is given by the following equation:

$$w_{NW,max}^2 = \frac{L_{NW}^2}{E_{NW} \cdot \pi^2} (\sigma_{NW} - \sigma_{Euler}) \quad (Eq. 3-5)$$

This shows that NWs can buckle in two opposite directions once the critical stress is reached [Fang 1999], as illustrated in Figure 3.33.

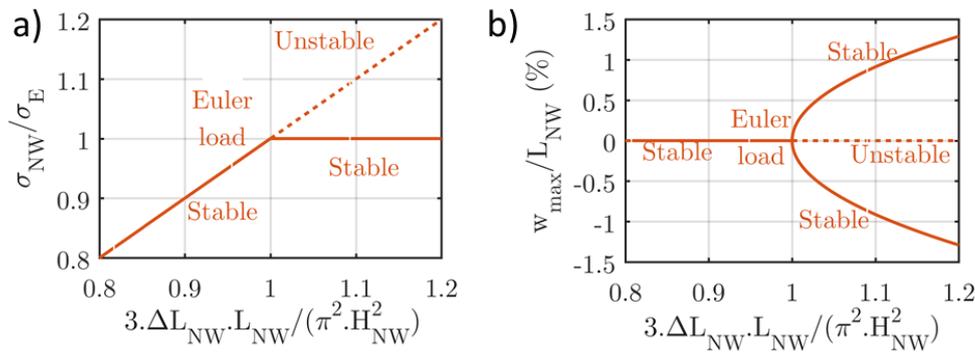


Figure 3.33 - Evolution (a) of compressive stress and (b) of deflexion as a function of strain and geometry [Gaben 2016 SNW].

Consequently, Figure 3.34 can be plotted evidencing the maximum stress accepted by the NWs before buckling: the longer and the thinner the NWs, the more sensible they become to residual stress.

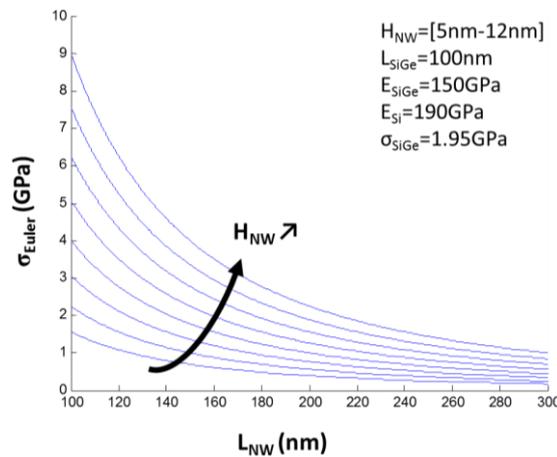


Figure 3.34 – Euler load as a function of  $L_{NW}$  and  $H_{NW}$ : example for a given SiGe anchor.

Besides, several other trade-offs can be evidenced from this model and hence from the 3D-plots presented in Figure 3.35:

- In the case of dense layout integration, the number of SiGe supports has to be minimized in order to maximize the number of gate and devices in between. In other words, the ratio  $L_{NW}/L_{SiGe}$  must be increased. However, increasing  $L_{NW}$  also decreases  $\sigma_{Euler}$  and increase the sensitivity to internal stress according to Figure 3.34 and Figure 3.35a.
- $L_{SiGe}$  can also be reduced in order to decrease  $\sigma_{SiGe}$ . Considering that NW width need to be maximized for performance optimization (§2), the low limit of  $L_{SiGe}$  is therefore fixed by the NW width since SiGe etching also occurs within the lateral anchors.
- A thicker  $H_{NW}$  can improve the NW resistance to buckling, however, a negative impact on electrostatics and performances has been demonstrated by simulations (§2).
- Alternatively, a lower concentration of Ge can reduce  $\sigma_{SiGe}$  and  $\sigma_{NW}$  but at the expense of a lower  $Si_{1-x}Ge_x$  etching selectivity towards Si.

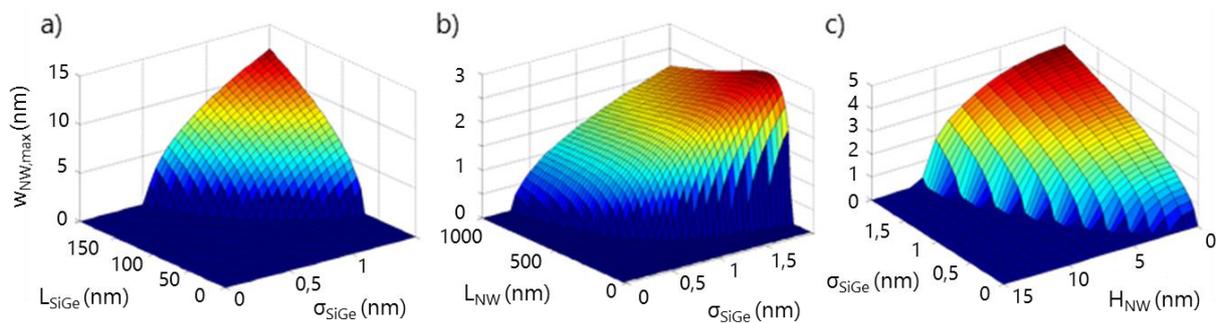


Figure 3.35 - NW maximum deflexion as a function of structure geometry for different SiGe residual stresses. The plans  $w_{NW,max} = 0$  correspond to acceptable straight stable positions

Finally, in both NW last and NW first approaches, the NW channel end up suspended once the sacrificial gates are removed and prior to the HKMG stack deposition. As noticed in simulations [Reboh 2016], highly compressive stress can be introduced by means of SiGe RS/D. Consequently, the longest channels in the longest gate length cavities may be affected by buckling issues. The strain level will be evaluated in the following next section concerning the SEG of S/D.

## Conclusion

Among the three techniques available for the selective etch of SiGe versus Si, the wet chemistry is the more promising in terms of selectivity. Even if the edges of the silicon NW channels are consumed by a few nanometers, their overall thickness remains uniform as compared with tunnel enlargement resulting from plasma etching. At least  $W = 70$  nm large suspended nanosheets – as required to enhance SNWFET performances – were obtained. Besides, the process is sufficiently controlled to carve nanometric cavities in between the NWs for placing the internal spacers in the alignment of the principal gate spacers for a NW last approach. The good selectivity therefore preserves the shape of the NW channel cuts.

Subsequently, pattern collapse has been identified as an important risk when working with suspended features. Residual stress due to SiGe anchors (NW first) and due to SiGe RS/D (NW last and NW first) is the main cause of NW buckling. If at least few hundreds of nanometers long 7 nm thick suspended NWs were observed, an extended study is required with TEM imaging to avoid any twisted conclusion about collapsing due to SEM-induced surface charging.

### 3.5. Source and drains (S/D) and internal spacers fabrication

Epitaxy must be often selective, targeting a growth onto crystalline materials without any deposition on surroundings dielectrics. This is the case for the S/D epitaxy where Si or SiGe often in-situ doped with phosphorus, boron or carbon must grow from a Si or SiGe seed and not on the sidewall of the gate spacers or onto the insulation (BOX or shallow trench insulation). On top of the first epitaxy parameters precited in §3.2, surface preparation prior to the epitaxy has also a significant importance in determining the epitaxy quality and therefore the electric performances. This is especially true as the fabrication of SNWFETs with internal spacers – as required to minimize the parasitic capacitances (§2) and to serve as an etch stop layer (§3.1) – requires several steps of etching that might damage the surface.

This sub-chapter starts with the recent improvements made in surface preparation and selective epitaxy growth (SEG) on SOI devices. Then, optimized results are presented for SNWFETs having internal spacers formed with both NW last and NW first approaches. Finally, SiGe S/D are evaluated to induce compressive channel stress in order to improve hole mobility as already observed in trigate NWFETs (§1.3.2).

#### 3.5.1. Surface preparation

The presence on the surface of amorphous silicon oxide layers, polymers or etching residues has a strong impact on the epitaxy quality. Typically, high temperature bake must be applied under hydrogen flow to desorbs the contaminants and to passivate the surface. However, the minimum required of 1050°C is often not compatible with usual patterned wafers, thin SOI layers or ion implanted materials, causing thin film islanding, shape change and dopant migration. In order to avoid high thermal budgets, a combination of “HF-last” wet cleaning and in-situ H<sub>2</sub> can be used [Abbadie 2004]. The wafers are dipped in HF diluted in deionized and deoxygenated water (typically between 0.2% and 1%) to remove the native SiO<sub>2</sub> prior rinsing, in deionized and deoxygenated water, and drying. The wafers must be then loaded as quickly as possible in an inert atmosphere (N<sub>2</sub>) to preserve the surface passivation. 85% of the silicon dangling bonds are occupied by hydrogen atoms according to [Hartmann 2016] and the last 15% that are bound to oxygen, fluorine and carbon must be removed with the H<sub>2</sub> in-situ annealing. Nevertheless, Y. Bogumilowicz et al. results reported in [Hartmann 2016] show a correlation of baking temperature increase and surface contamination decrease and therefore the significant impact on epitaxy quality (Figure 3.36). The number of defects is reduced by nearly two orders of magnitude when increasing the temperature from 775°C to 825°C.

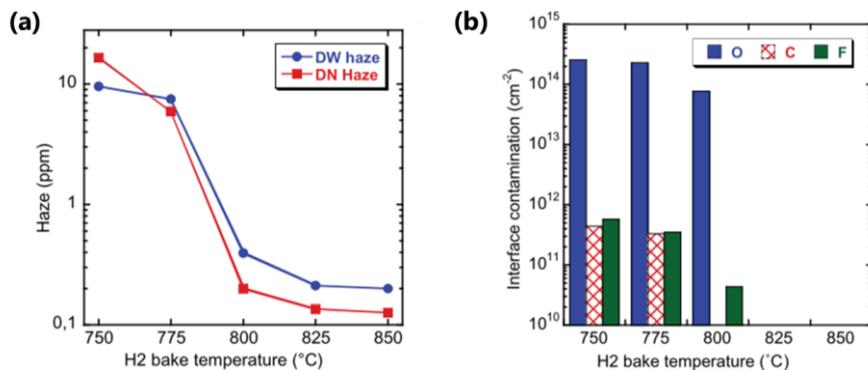


Figure 3.36 – Effect of H<sub>2</sub> in-situ baking temperature (2 minutes) on (a) haze (surface roughness) after 100 nm epitaxy of Si and (b) corelation with interface contaminants [Hartmann 2016].

However,  $>800^{\circ}\text{C}$  remains too high for the targeted applications since, for example, the NWs are rounded after 2 min at  $750^{\circ}\text{C}$  [Dornel 2007 APL]. NWs can also be pinched at their base and even detach. In ion implanted devices, an elevated temperature can cause the migration of the dopants. In gate first integration schemes, a detrimental oxide regrowth in between the channel and the gate high-k dielectric occurs. Consequently, innovative surface preparation schemes had to be investigated to obtain high crystalline quality epitaxial layers with lower thermal budgets. On thin SOI (3 nm typically),  $\text{H}_2$  bake is typically carried out at  $650^{\circ}\text{C}$  and 20 Torr for 2 min prior to the SEG of Si RS/D [Jahan 2005]. The impact of such a low temperature appears limited on (001) surfaces [Destefanis 2008 SST] and electrical performances of FDSOI devices with dual channels [Le Royer 2011 IEDM] with Si [Andrieu 2007 VLSI] or SiGe:B [Baudot 2010 EDL] RS/D are excellent. However, epitaxy of (110) contaminated surfaces is catastrophic [Destefanis 2008 SST].

Four different surface preparation strategies are compared in Figure 3.37 [Lu 2016] starting from a simple “HF-last” process (Figure 3.37a). In Figure 3.37b, a “Siconi” process is partially performed: etchants are generated in a remote plasma cavity ( $\text{NH}_3 + \text{NF}_3 \rightarrow \text{NH}_4\text{F} + \text{NH}_4\text{F}\cdot\text{HF}$ ) and  $\text{SiO}_2$  is then transformed into a salt at  $30^{\circ}\text{C}$ . The salts are then sublimated in the epitaxy chamber prior to the epitaxy. In Figure 3.37c, a “HF-Last” wet cleaning is performed before and in the last SEM of Figure 3.37d, the full Siconi process is performed including the last salt sublimation in the Siconi chamber before an HF-last cleaning and the epitaxy.

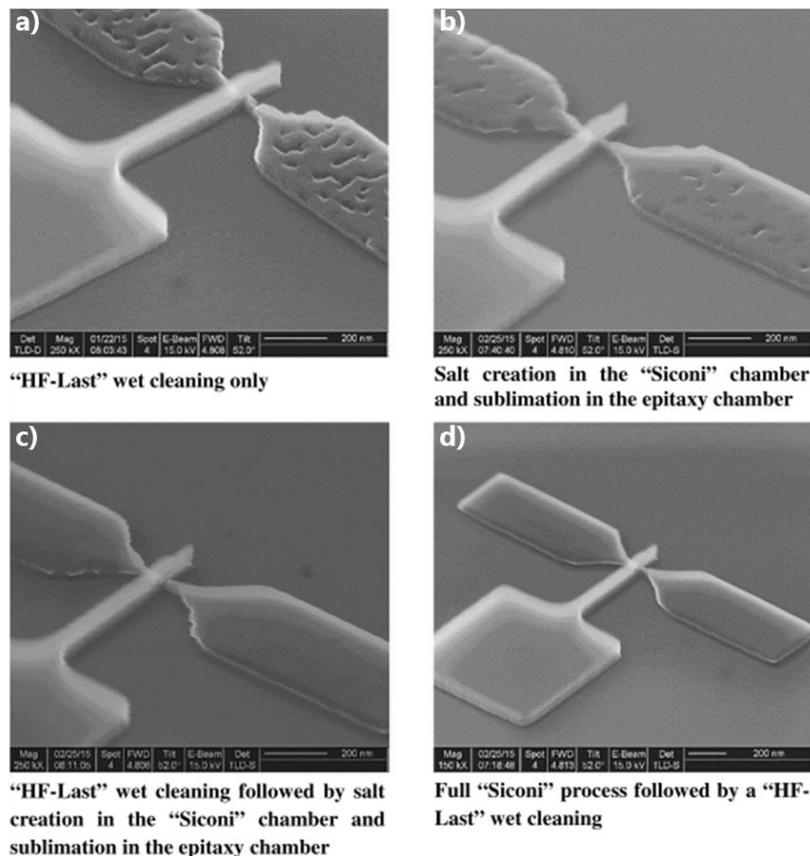


Figure 3.37 - Effect of different surface preparation on 18 nm thick  $\text{Si}_{0.7}\text{Ge}_{0.3}\text{:B}$  S/D epitaxy quality [Lu 2016].

No matter the order, combining HF-last and Siconi leads to significant improvement of the epitaxy quality. In any case, specific care must be taken during lithography and the following etch steps to remove all polymers and other residues especially in the case of NW last and NW first integrations where the epitaxy of S/D is performed after several deep reactive ion etching (DRIE) steps.

### 3.5.2. Selective epitaxial growth (SEG)

SEG is obtained from dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) precursor with  $\text{SiO}_2$  and  $\text{SiN}$  masking layers. Si and SiGe:B RS/D have been successfully realized in the past [Hartmann 2011 JCG], [Barraud 2013] as well as SiGe/Si bilayers [Monfray 2010]. Besides, patterned wafers are affected by loading effects: a variation of the growth rate and of the Ge concentration is observed with an amplitude related to the mask opening [Hartmann 2016]. The growth rate itself depends on surface orientation and increase exponentially with the temperature while Ge content increases linearly with the  $\text{GeH}_4$  flow.

Although, the Si precursor dichlorosilane has a low growth rate at low temperature [Hartmann 2007], low temperature SEG ( $650^\circ\text{C}$ ) have been achieved on 3 nm-thin FDSOI transistors [Le Royer 2011 IEDM] and trigate NWFETs [Barraud 2014]: a simple HF-last and in-situ  $\text{H}_2$  bake at  $650^\circ\text{C}$  and 20 Torr for 2 min has been used prior the epitaxy of  $2 \times 10^{20} \text{ cm}^{-3}$  in-situ doped of SiGe:B RS/D at  $650^\circ\text{C}$  with  $\text{SiH}_2\text{Cl}_2 + \text{GeH}_4 + \text{HCl} + \text{B}_2\text{H}_6$  chemistry. State-of-the-art electric performances were measured, advantaged by reduced access resistances (high doping concentration) and increased hole mobility due to compressive channel stress. The same process is therefore used for the S/D SEG of SNWFETs fabricated in this thesis.

Otherwise, low growing rate issues can be addressed by using silane and disilane having higher rates at low temperature ( $650^\circ\text{C}$  and lower). Their use has been developed especially for monolithic 3D application requiring very low thermal budget [Lu 2016], [Hartmann 2016]. However, those gases are not selective towards dielectrics and therefore require the use of the Cyclic Deposition/Etch (CDE) technique [Bauer 2006], [Bauer 2007]. As described in [Hartmann 2016], few nanometers of Si or SiGe are deposited: single crystalline layers are arranged on silicon active areas (the S/D surface) while dielectrics (BOX, STI,  $\text{SiN}$  spacers) are covered with amorphous or polycrystalline material. A selective etch is therefore performed with chlorine chemistry in order to remove any non-crystalline material. Besides, low temperature process allows SiGe:B layers for instance to remain fully compressively strained [He 2012]. Subsequently, even if CDE have not been used for NWFET and SNWFET fabrication in this thesis project, this technique remains promising for further improvements of SNWFET.

### 3.5.3. S/D in a NW last approach with aligned internal spacers.

As recalled in Figure 3.38, in the NW last approach for making internal spacers before the S/D epitaxy, the NW extensions are first etched down to the bottom NW (Figure 3.38b). During this etch an isotropic and selective etch of the sacrificial SiGe is realized in-situ for carving cavities aligned under the gate spacers (Figure 3.38c, §3.4). Highly conformal  $\text{SiN}$  spacer material is deposited filling the cavities (Figure 3.38d). A last optimized anisotropic / isotropic etch removes  $\text{SiN}$  from the NW cuts (Figure 3.38e) allowing the Si or SiGe merging SEG in-situ doped with phosphorus or boron (Figure 3.38f).

Source-drain longitudinal TEM images of Figure 3.38g display a mixt configuration with a trigate and a single GAA channel. The internal spacers present a good alignment with the main gate spacers and the merging SEG of the RS/D does not exhibit any significant lattice defect.

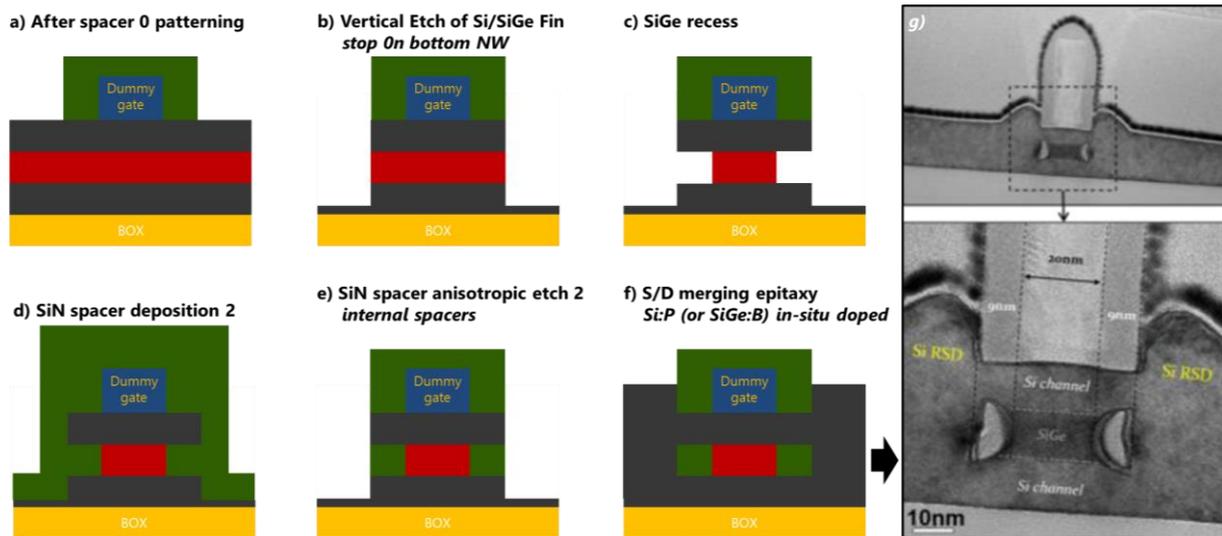


Figure 3.38 – (left) NW last integration scheme for the fabrication of the aligned internal spacers. (right) TEM longitudinal section images of a phosphorus in-situ doped SD with internal spacers.

Similarly, SEG of SiGe:B was also performed. The SEM images of Figure 3.39 of both SiGe:B and Si:P S/D do not present any noticeable defects.

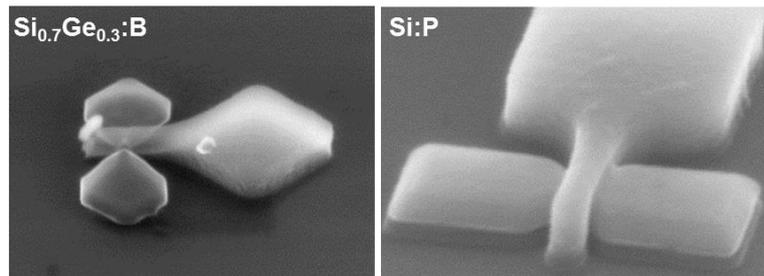


Figure 3.39 - SEM of single transistors after RS/D epitaxy of SiGe:B and Si:P.

Figure 3.40 presents in and out of plane deformations associated with Si and SiGe:B RS/D epitaxy. If PED mappings reveal that no residual stress is present in the Si S/D (NMOS), in contrary SiGe:B RS/D injects significant amount of compressive strain into the Si NW channels with near to -1% in-plane deformation (PMOS). As a result, SNWFET technology is compatible with this usual strain management technique in order to improve hole transport in PMOSFETs. This will be confirmed by the electrical measurements provided in the following next chapter (§4.1).

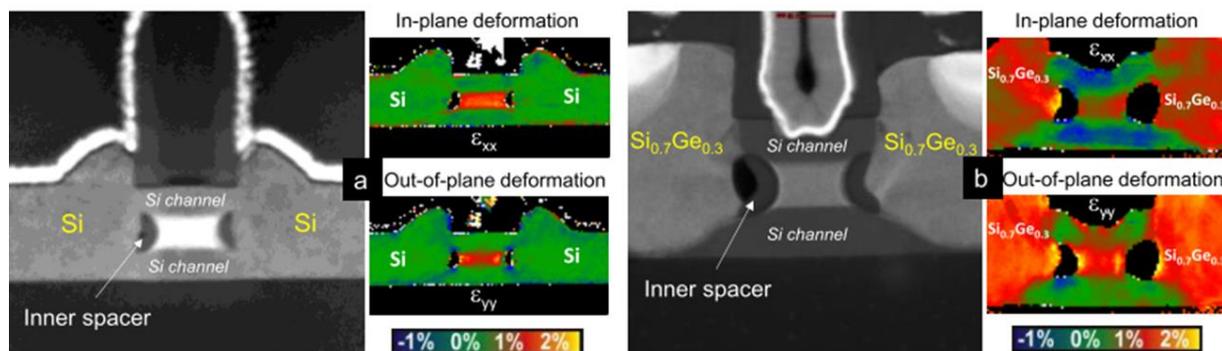


Figure 3.40 - HAADF STEM images along with in and out of plane deformations maps acquired by PED after Si and SiGe:B RS/D epitaxies.

### 3.5.4. S/D in a NW first approach with self-aligned internal spacers

The case of NW first approach with HSQ lithography is recalled in Figure 3.41 for two suspended NWs (dual GAA configuration). After exposure and developing of the HSQ self-aligned sacrificial gates (Figure 3.41a), a conformal layer of SiN is deposited (Figure 3.41b) and anisotropically etched in order to let emerge the NW stack (Figure 3.41c). In this case, SiN occupies the space in between the NWs. Then, the Si NW extension anisotropic etching is combined with a SiN anisotropic spacer etching in order to recess the Si/SiN stack and to stop into the bottom NW (Figure 3.41d). Si:P and SiGe:B merging SEG are then performed from the remaining nanometric layer of Si (Figure 3.41e). Consequently, self-aligned spacers are obtained and the process can be continued up to the sacrificial gate replacement with no subsequent SiGe selective etch (Figure 3.41f-g) leading to self-aligned HKMG (Figure 3.41h).

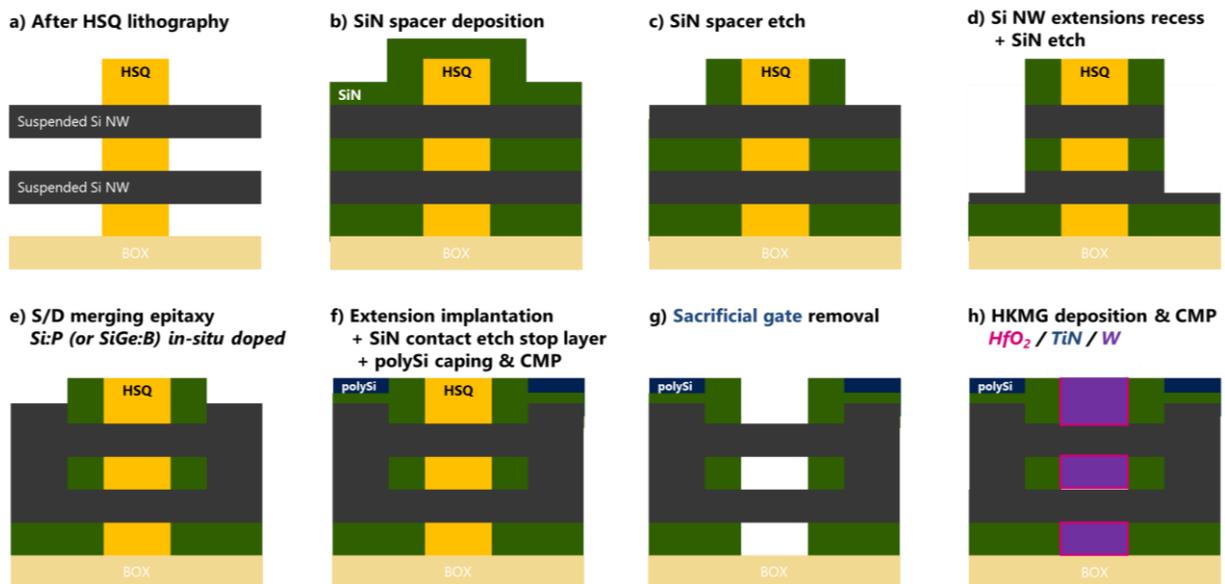


Figure 3.41 - NW First integration scheme for the fabrication of the self-aligned internal spacers.

The absence of a protective SiN stopper on top of the HSQ gate is a potential issue as compared to the NW last integration flow. In the later, a SiN hard-mask remains after the polysilicon gate patterning. Therefore, HSQ oxide is directly exposed during the S/D extension etchings and the HF-based pre-epitaxy surface cleaning. Hence, the impact of plasma deep reactive ion etching (DRIE) needs to be evaluated. According to SEM and TEM images of Figure 3.42, no HSQ recess is observed in between the SiN spacers implying that HSQ is removed at the same speed than SiN. Consequently, the sacrificial gate height is shortened by the thickness of the SiN spacer that needs to be removed around the Si NW stack. In Figure 3.42, an over etch margin has been applied to remove the SiN all the way down to the BOX: SiN is absent on the side of the active areas according to the SEM image and thus, SiN remains only in between the Si NWs. As a side note, the schematic of Figure 3.42 evidence the SiGe lateral anchors required to suspend the NWs while the Figure 3.41 relates a general case where several gates are patterned in parallel on the same NW stack and where the SiGe anchors are “far” on the edges of the active area. This will be further discussed in the following next chapter (§4.2).

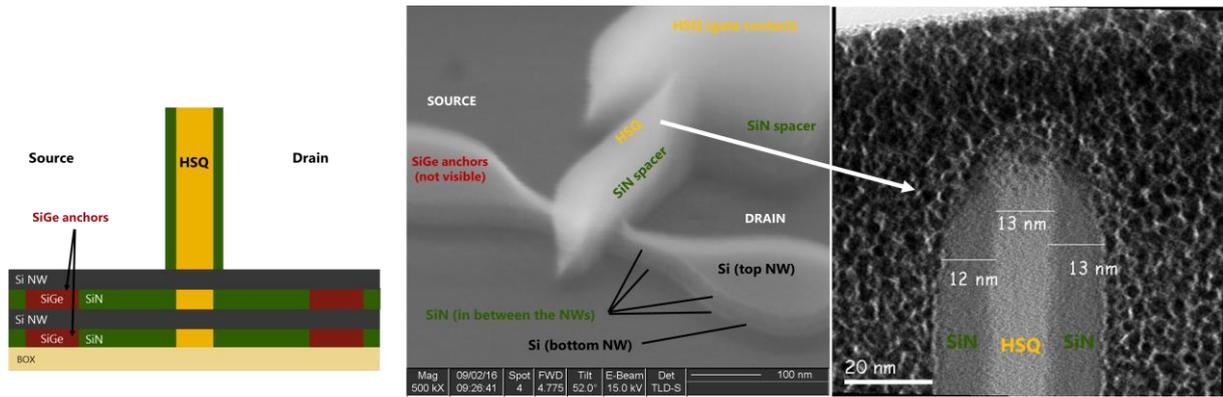


Figure 3.42 - SEM and TEM images of a single gate transistor with HSQ sacrificial gate after spacer patterning in a NW first integration scheme.

Then, the NW extensions must be etched down to the bottom NW prior to proceed with the merging SEG of the S/D. Figure 3.43 presents the result of this sequence with HF wet cleaning and H<sub>2</sub> in-situ bake at 650°C prior to perform the epitaxy of a Si:P S/D. No significant recess of the HSQ gate was revealed by AFM, however, the SEM image of Figure 3.43 presents a S/D epitaxy with an important rugosity.

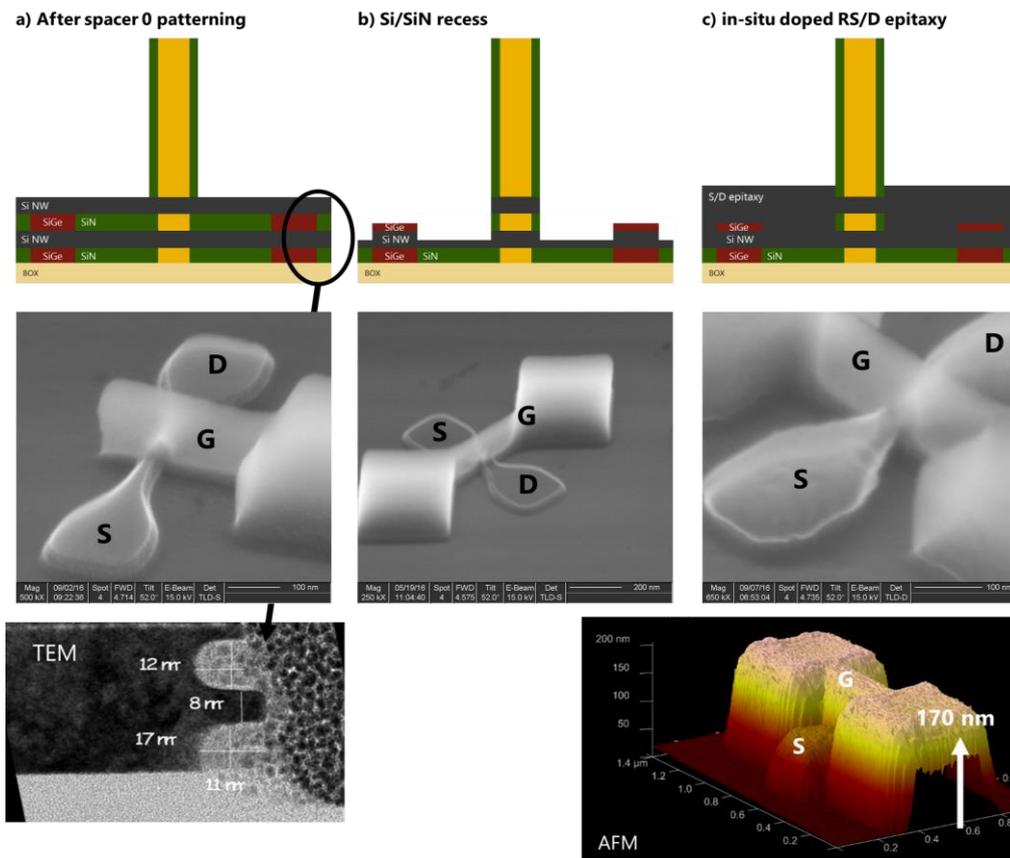


Figure 3.43 – (a) Spacer patterning with SEM and TEM showing the SiN present in between the NWs, (b) the extensions recess and (c) the S/D merging SEG: no significant recess of the HSQ is observed on SEM and AFM images after the epitaxy and the sacrificial gate remain 170 nm high.

Besides, the alternative surface preparation schemes proposed in a previous subsection to improve the epitaxy quality have been experimented with a focus on the impact on HSQ. Figure 3.44 presents a combination of SEM and TEM images with AFM measurements evaluating the HSQ consumption in between the spacers during a partial and a complete Siconi. The Siconi consumes “only” 10 nm of HSQ and slightly improve epitaxy quality.

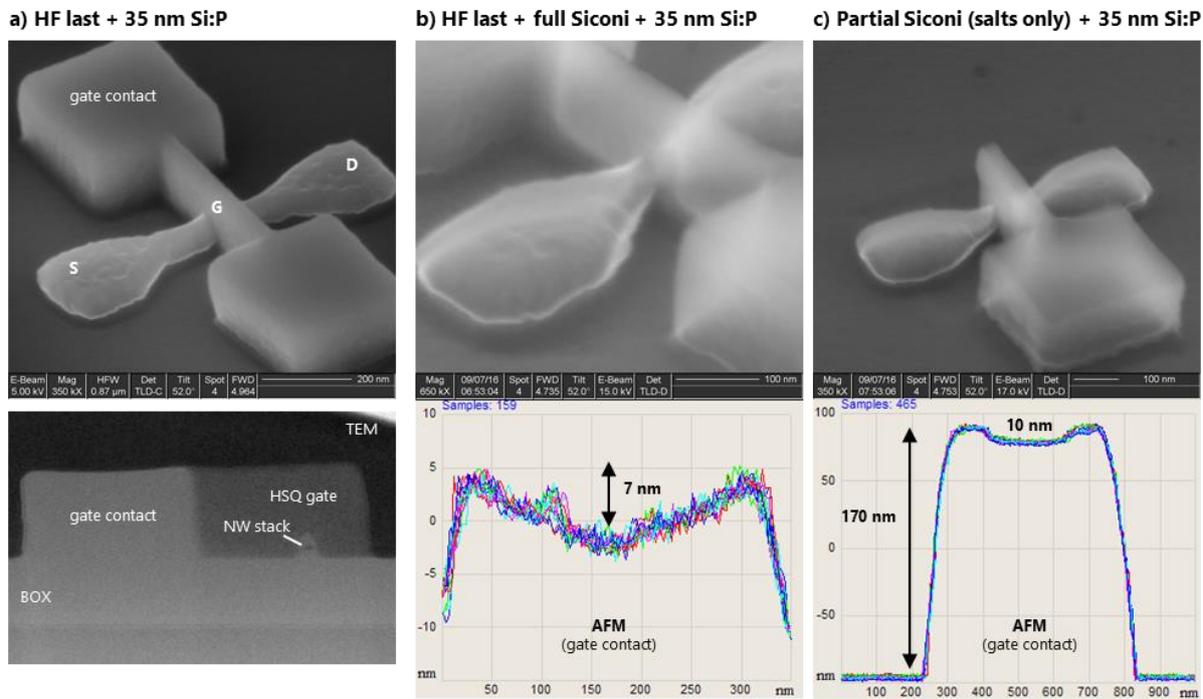


Figure 3.44 - Comparison of various pre-epitaxy surface preparations and their impact on HSQ.

Since the HSQ sacrificial gate remains 170 nm high after spacer patterning and S/D recess, losing ~10 nm of HSQ over the 125 nm remaining above the 35 nm high stack of NWs is then acceptable. Besides, no impact of such a small recess on the following steps have been noticed. Indeed, a step of non-selective CMP is performed to reach the buried HSQ surrounded by SiN spacers as observed in the dedicated subchapter (§3.7).

Finally, after these tests, the remaining wafers of the NW first dedicated batch were processed with standard HF-last pre-epitaxy cleaning prior to Si:P and SiGe:B merging SEGs: this standard process appears to be simpler and therefore faster. This is in accordance with the objectives of this specific batch dedicated for the development and the demonstration of the NW first approach.

### 3.6. Electron beam lithography of HSQ

HSQ resist has been used as a sacrificial gate material itself in the NW First integration (§3.1.2) as this inorganic resist can be turned into a dense oxide. HSQ appears as an interesting alternative to polysilicon for the fabrication of sacrificial gates for its ability to be exposed by EUV or electron beam through silicon leading to self-aligned gates and spacers through the suspended silicon NW channels. In the following, the deployed efforts in finding the proper conditions for lithography and developing of HSQ are detailed. Figuring what is the minimum gate pitch achievable and prospecting scaling potential is essential to determine if HSQ material can replace the typical polysilicon sacrificial gates.

#### 3.6.1. Conditions

EUV stepper being not available in LETI at the time of this project, a SB3054 electron beam from VISTEC has been used. The shaped beam tool is able to model rectangular beams with dimensions from 30 nm and up to 1600 nm with an acceleration energy of 50 keV. Spin coating and developing were realized in a DNS RF3 tool. A XR-1541 (also labelled as “FOX 13”) was provided by Dow Corning whose datasheet is reproduced in Figure 3.45a: contaminants level is compatible with front end of line (FEOL) specifications. Figure 3.45b shows for this dilution of HSQ that up to 212 nm thick layers can be obtained leading to features having the same height after developing. Although the spin coating was realized manually, wafer uniformity was in the 5% range. Those resists have a shelf time of 6 months and are known to crystalize quickly after the first use. To minimize this impact, experiments were conducted within few days after the first opening and the resist was preserved at 5°C. Spincoating itself is done at room temperature (the cleanroom is stabilized at 21°C). Few defects may randomly appear during manual spincoating (Figure 3.45c) but wafers can be recycled with TMAH developer.

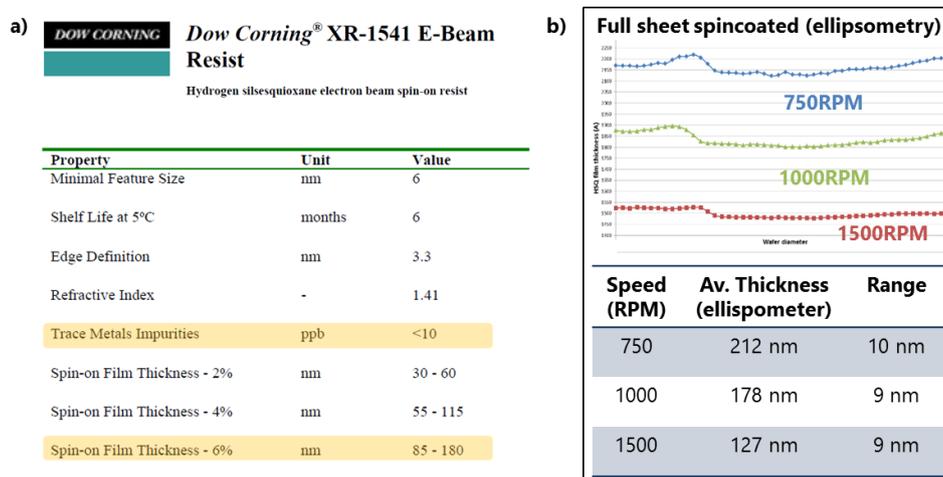


Figure 3.45 - (a) XR-1541 datasheet (HSQ), (b) spincoated layer uniformity over 300 mm diameter wafer.

#### 3.6.2. Layouts description

A new layout was designed specifically for the investigation of HSQ properties. Single and arrays of lines were placed and separated from one to another by 50 μm to avoid any proximity effect. Critical dimensions (CD) – or linewidth – were targeted in between 6 nm and 30 nm. Various line array pitches were included such as 46 nm and 64 nm, the 7 nm and 10 nm nodes technology predicted specifications, and up to 100 nm pitch. Different geometries were considered to improve the

mechanical resistance of such high aspect-ratio (A/R) lines. Adding one or two lateral anchors as illustrated in Figure 3.46 is expected to reduce collapsing.

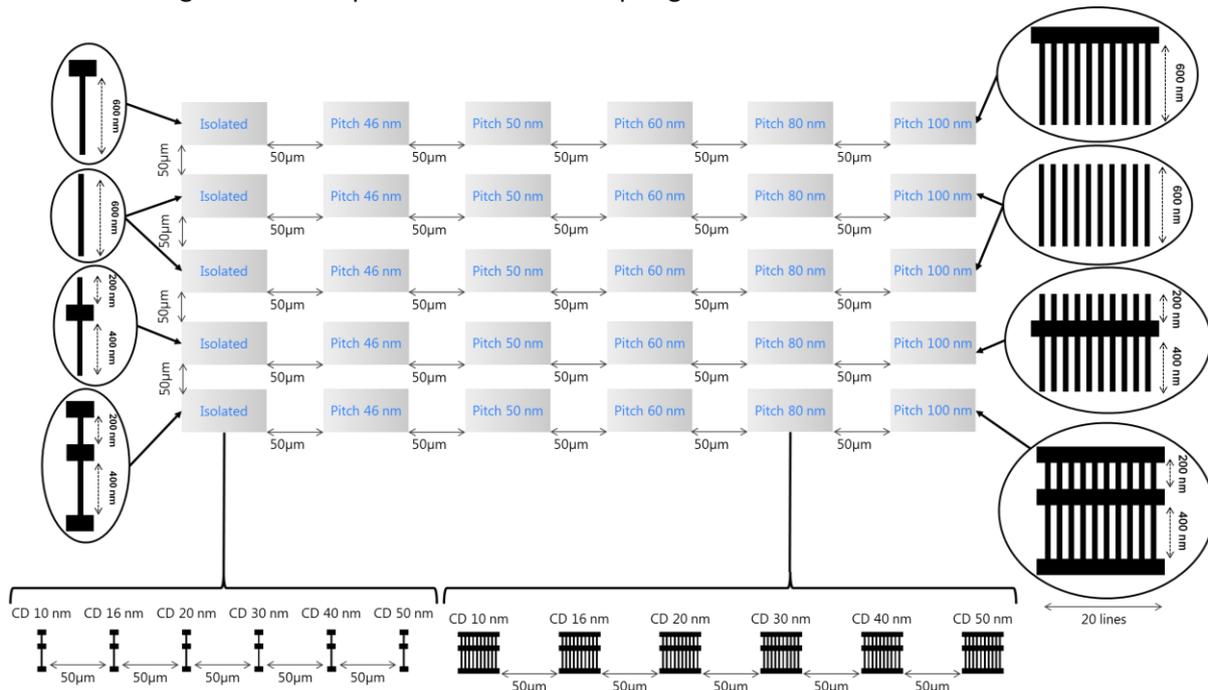


Figure 3.46 - Layout "HSQGABEN" for studying HSQ properties.

Typical lithography mask set used in LETI for advanced devices is codenamed "SNO2". Figure 3.47 shows two types of devices with single stack of NWS (Figure 3.47c) and with 10 to 50 parallel NW stacks (Figure 3.47d). For layout uniformization purpose (see the subchapter related to CMP: §3.7), dummies features for active and gate level are often placed as visible on Figure 3.47a-b.

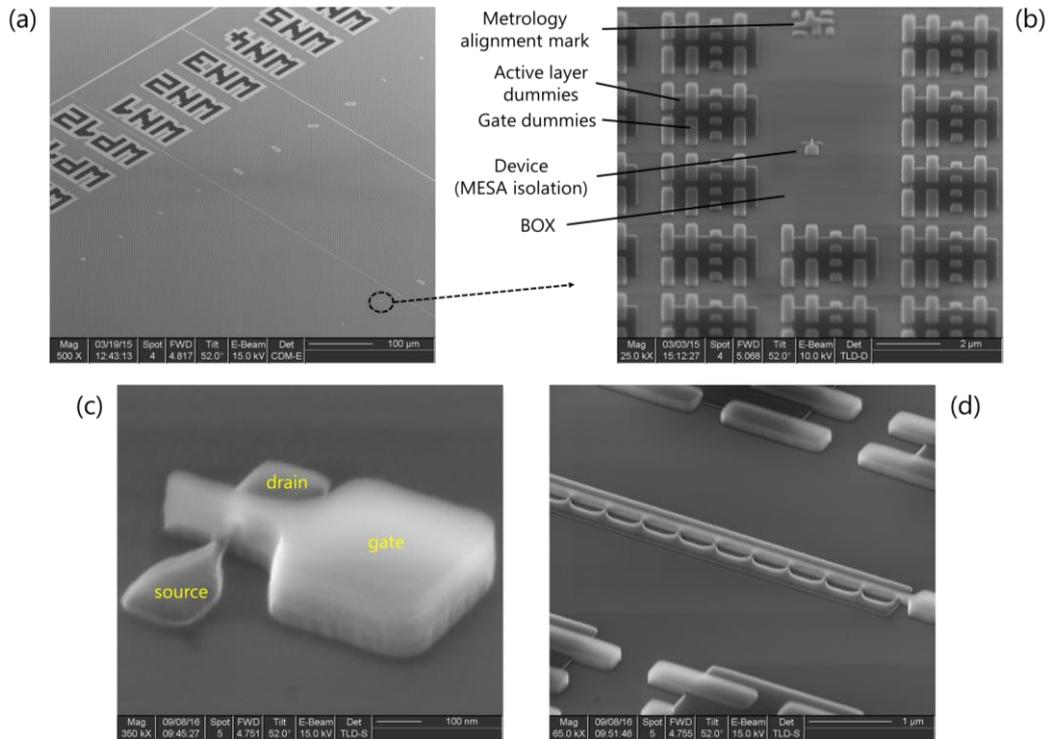


Figure 3.47 - SEM images of the wafer with active and gate level patterns: (a) and (b) low zooming (micrometric scale), (c) single stack transistor and (d) parallel stacks transistor (multi-fingers device).

A variant of this layout is presented in Figure 3.48 featuring most of the usual single gate devices used for transistor tests in a large variety of gate length from 6 nm up to 10 μm placed on active areas (the NW stacks) having widths and length from 10 nm up to 10 μm. Few modifications on these devices were introduced: several gate lengths were scaled from 15 nm down to 6 nm and attached on both end to prevent collapsing (Figure 3.48 left). For dense integration demonstration purpose, “multigate” devices were added to mimic aggressively scaled devices (Figure 3.48 right). They are not electrically functional as they share the same gate contact. But major change was to remove the gate dummies usually covering the majority of the chip in order to significantly reduce the exposure time. The active layer dummies (SiGe/Si/SiGe/Si) exposed with DUV lithography still remain.

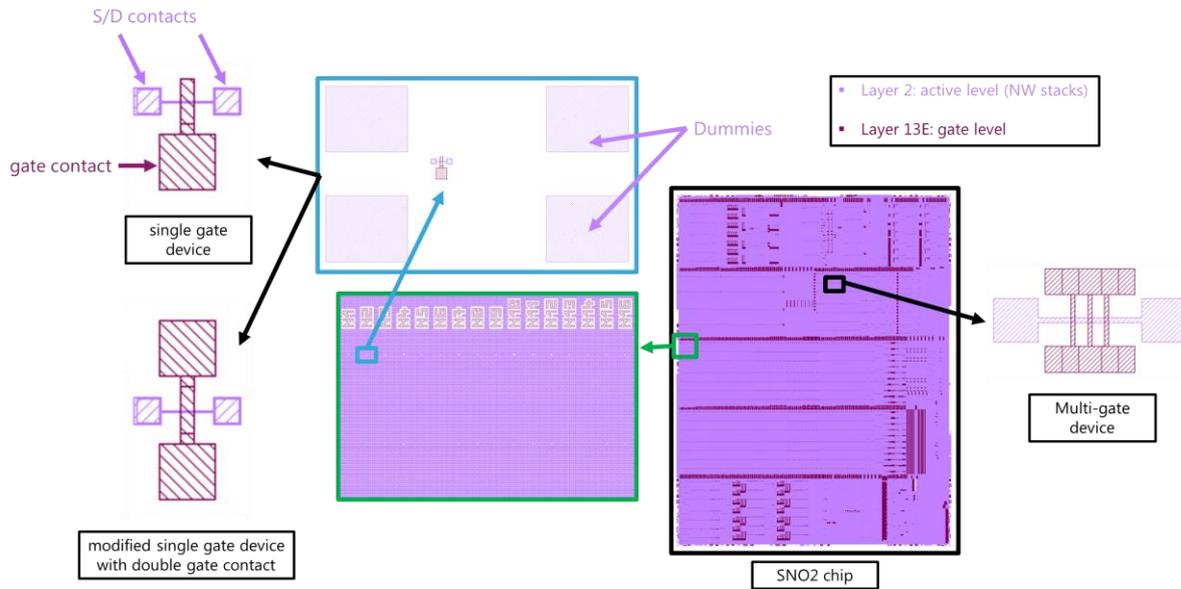


Figure 3.48 - SNO2HSQLG layout with modifications to include ultra-scaled gate lengths down to 6 nm and multigate devices. Gate dummies were removed in order to lower the exposure time.

### 3.6.3. Resist developing

Tetramethylammonium hydroxide (TMAH) is the usual developer for HSQ. Even though 25% concentration provides the best contrast [Coquand ECS 2013], [Monfray 2010 IEDM], regulations have recently limited it at 2.38%. Analysis of such various and numerous structures was conducted on a Hitachi automated critical dimension scanning electron microscope (CD SEM) Hitachi CG4000. Since the resist once developed seemed not sensitive to electron beam anymore (no CD contraction), voltage was set to 800 V with a current of 8 pA for maximum contrast and resolution. First statement is that single isolated devices are easily resolved. Figure 3.49a shows the slight dependence of CD with exposure dose. Besides, CD does not depend on developing time: when turned into a dense oxide, HSQ becomes entirely selective towards the TMAH developer and no resist trimming effect is observed even if the puddle time is doubled (Figure 3.49a). Gate lengths down to 6 nm were achieved with 200 nm high HSQ line and 400 nm long maintained at the extremities by two gate contacts as proved in SEM and TEM inset of Figure 3.49b. Finally, the variability on a 300 mm wafer is within the 2 nm range over the whole wafer and for all the devices (Figure 3.49c). The value is limited by tool precision.

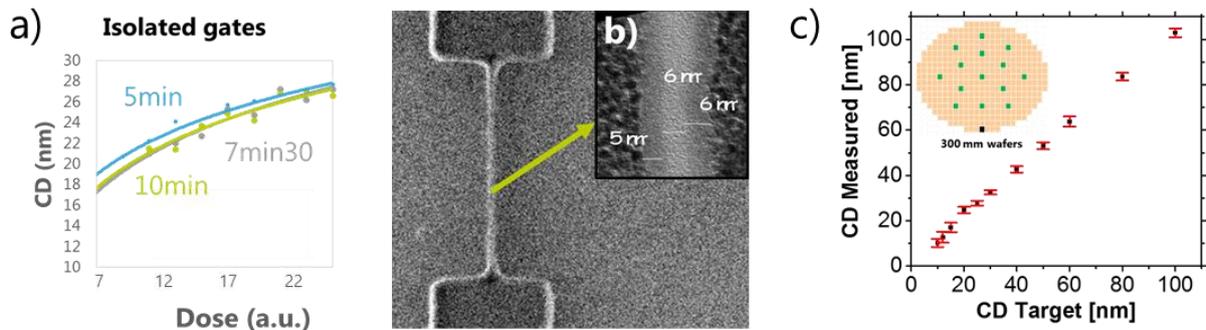


Figure 3.49 – (a) CD dependence on exposure dose and puddle time during developing in TMAH. (b) SEM top view and (inset) TEM cross section of one the best scaled gate: 200nm high and 6nm large. (c) CD uniformity measured on 14 chips over a 300 mm wafer.

The case of arrays of gates is more complex. Exposure-dose experiments analysis revealed that very specific conditions of dose, gate CD, gate pitch and gate height were required in order to a proper restitution of the targeted layout. Figure 3.50 shows the effect of exposure dose on a 64 nm pitch array of 200 nm and 400 nm long lines. If the dose is too small, transformation of the resist is not sufficient for the narrow features to remain. As the dose is increased, the CD is enlarged and 200 nm long lines can be resolved. 400 nm long lines needs a higher dose and CD in order to prevent collapsing – either due to capillarity forces and/or centrifuge acceleration.

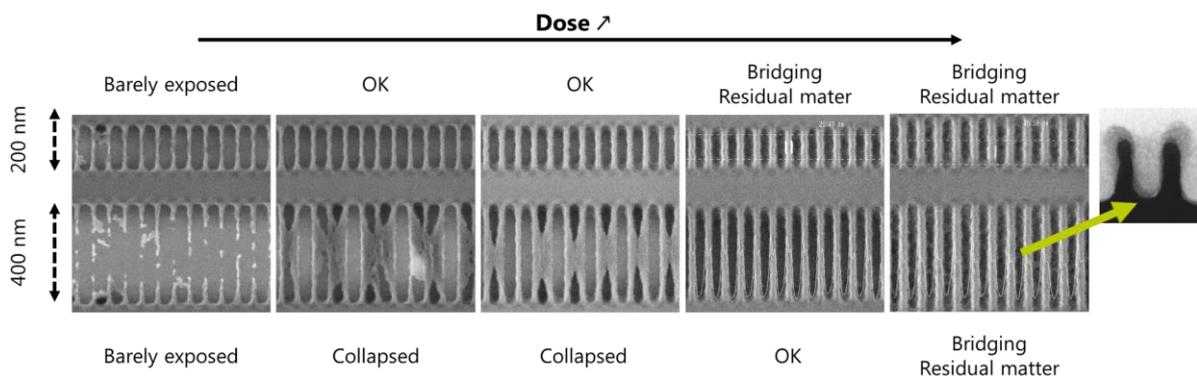


Figure 3.50 - Exposure dose results on silicon bulk substrates for a 64 nm pitch array.

Spincoated resist in this example was 200 nm thick but similarly, a study on 120 nm thick resist shown an improved mechanical resistance, allowing narrower CD and pitch. In each case, when the dose becomes too high, some residual material remains at the bottom in between the lines. Finally, a process window of  $400 \mu\text{C}/\text{cm}^2$  was found centered on  $1200 \mu\text{C}/\text{cm}^2$ .

The experimental protocol of Figure 3.51 was set up to improve pattern resolution and investigate HSQ minimal pitch achievable within the LETI cleanroom context. Two tools were available at the time of the study. The DNS RF3 dispenses the TMAH developer and remain still during the puddle time needed to dissolve the unexposed resist. In an attempt to remove more of the residues at the feet of the lines, puddle time was first increased, then two consecutives developing where evaluated and a Sokudo Duo tool was used with its spin-on dispenser which may improve reactants extraction from the cavities.

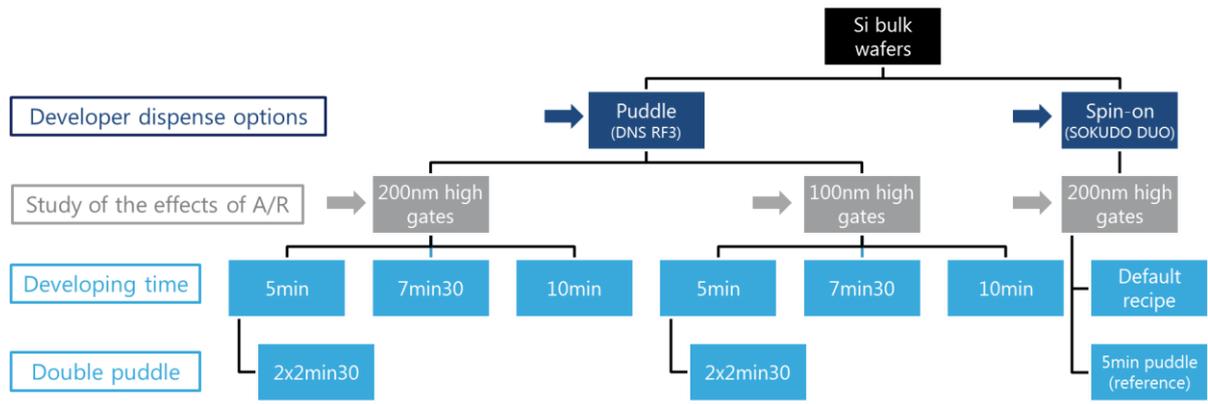


Figure 3.51 - Experiment plan for HSQ developing optimization.

Results on 60 nm pitch array and 16 nm large lines are displayed in Figure 3.52 showing that a higher developing time very slightly increases resolution. Since the exposed HSQ is selective towards TMAH, nothing prevents to increase as much as needed the puddle time. Conversely, the use of spin-on developer tool or double developing has not significant impact on the result.

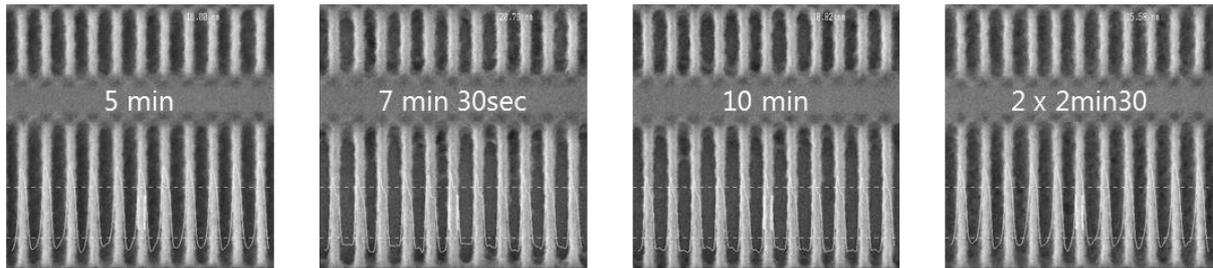


Figure 3.52 - Effect of puddle time during developing on 60 nm pitch and 16 nm CD line arrays.

### 3.6.4. Observations

Top view SEM images of Figure 3.53 show 60 nm pitch with 18 nm gate length for 200 nm high line arrays – measured with AFM – and 46 nm pitch with 8 nm CD when decreasing the feature height down to 120 nm high. The TEM images realized later on, revealed that resolution is a matter of space between two features independently of the line pitch and the line CD: 35 nm in the TEM image of Figure 3.53d was observed several times and seem to be the minimum achievable within the conditions employed in this thesis framework.

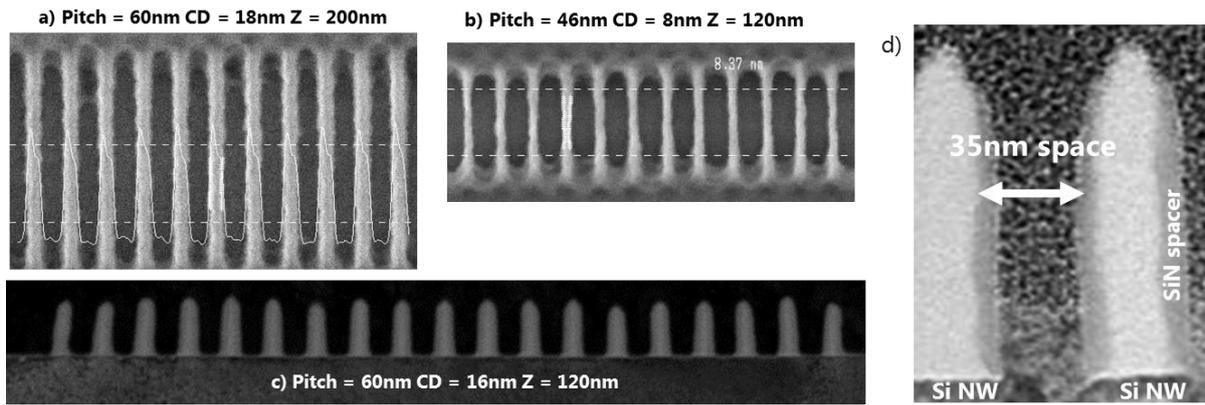


Figure 3.53 - a) and b) top view SEM images of best scaled devices. TEM images post spacer patterning of c) 60 nm pitch and 8 nm CD line array and d) 35 nm space in between 16 nm large and 200 nm high lines.

Once the HSQ lithography of sacrificial HSQ gates is performed above the two NW stacks, the previous results remain unchanged. Since silicon does not hinder the ebeam exposure, HSQ is transformed through the two suspended silicon NWs leading to self-aligned sacrificial gates as proven by SEM and TEM images of Figure 3.54 where the 200 nm high oxide line remain vertical and perfectly aligned.

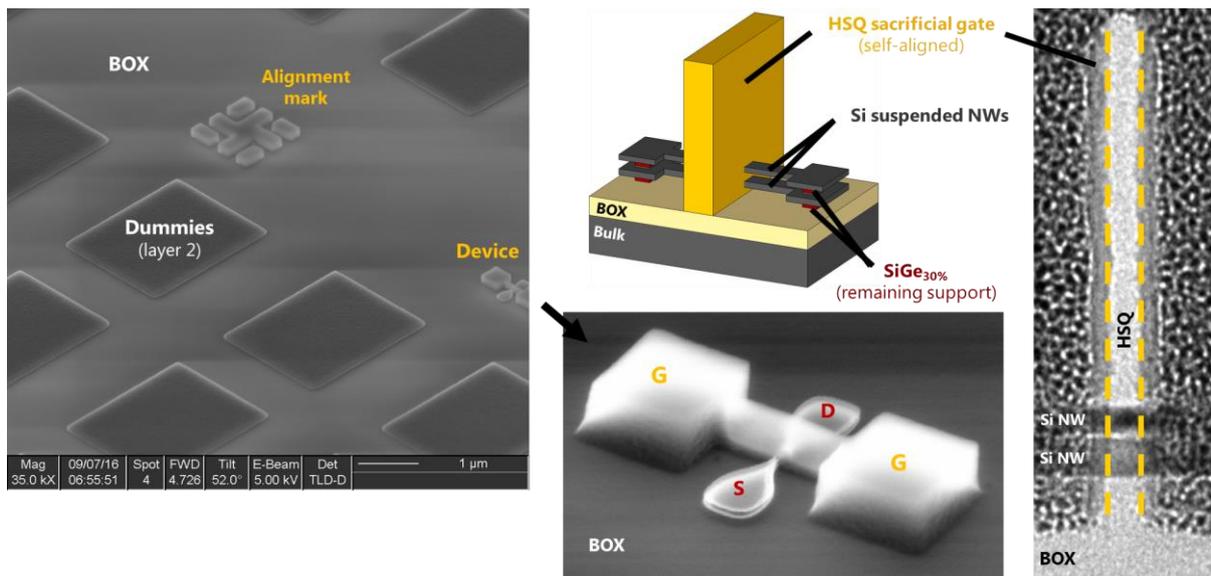


Figure 3.54 - HSQ lithography of self-aligned sacrificial gates. TEM image shows the perfect alignment through the two suspended silicon NWs [Gaben 2016 SSDM]. Si NWs are  $W = 15$  nm large and  $H_{NW} = 8$  nm thick, HSQ sacrificial gate is 200 nm high and 16 nm large after 4 nm SiN spacer patterning in the 35 nm thick TEM lamellae.

Previously shown results are likely dependent on the specific conditions available for the tests and different tools, resist or environment conditions may result in slightly improved or altered outcomes. However, it is safe to expect that the enumerated trends remain valid.

### 3.6.5. Limitation and perspectives

The 35 nm minimal space in between two features may be seen as a first limitation when considering the use of HSQ sacrificial gates. However, when two HSQ features are brought close enough, only the bottom of the line start to enlarge and to merge as imaged in Figure 3.55. Three options are conceivable to remove the oxide feet. First an isotropic trimming using HF solution or plasma etching can be considered at the expense of some gate length reduction – which can be anticipated in the layout design. Secondly, an anisotropic plasma etch can preserve the features width, however the oxide height will be reduced as it is not protected by a hard mask. Last option is based on the hypothesis that bridging appears due to a proximity effect: energy level for cross-linking is reached only because of the superposition of the background level of the close HSQ gates. By optimizing the exposure ordering or by realizing two successive exposure and developing steps it may be possible to get rid of this bottom oxide. Conversely, instead of being an issue, this effect may be turned into a local insulation when considering a bulk integration: the suspended NWs need to be raised higher above the bottom oxide [Gaben patent number 1658042].

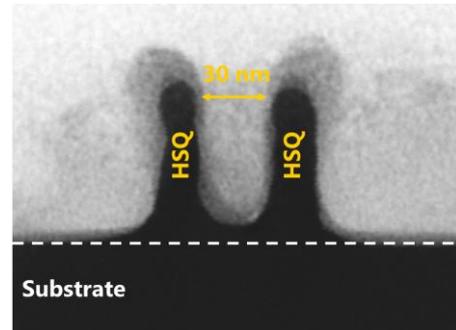


Figure 3.55 - TEM image of two HSQ lines close enough to evidence bottom bridging

Such high aspect ratio (A/R) features, are found to be extremely fragile. In order to prevent collapsing of the most scaled features, lateral anchors may need to be added. In our SNO<sub>2</sub>HSQLG ebeam layout, the lines below 15 nm CD were supported on both end by larges blocs of HSQ later used as gate contacts. This may first seem to appear as a waste of wafer area as compared with usual layouts, yet these anchors can be turned into a lateral device insulation (Figure 3.56), [Gaben 0693FR01].

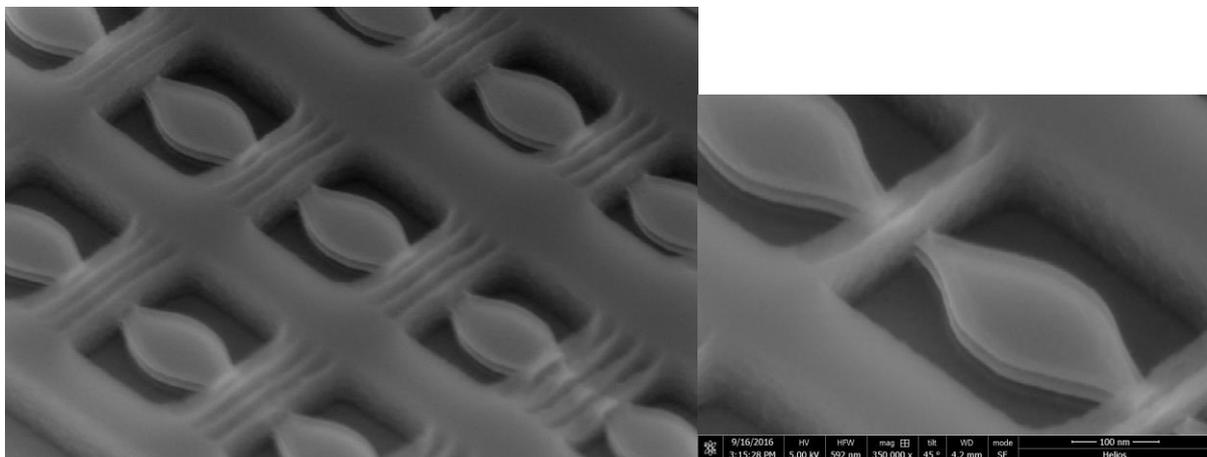


Figure 3.56 - HSQ sacrificial gates anchors used as lateral device insulation for the separation of S/D.

HSQ lithography requires, ebeam or EUV lithography which have significant costs in processing time and in investment respectively. An extended discussion of pros and cons for the use of both techniques will be developed in the next chapter once the complete picture will be drawn, including the mainstream NW last integration.

### 3.7. Chemical mechanical planarization (CMP)

Gate last integration flows requires several steps of Chemical Mechanical Planarization (CMP) and both NW last and NW first approaches for the fabrication of SNWFETs confirms this statement (§3.1). In the present subchapter, the main challenges of CMP are first introduced (§3.7.1) prior to relate some major results. Observations are linked to the process performances of the other modules, revealing the key elements of these integrations. First of all, the polysilicon CMP in preparation of the sacrificial gate patterning in NW last approach is presented (§3.7.2). Then, the sacrificial gate opening CMPs for both NW last and NW first alternatives are described (§3.7.3). Finally, the metal CMPs for HKMG fabrication and self-aligned contacts are shown (§3.7.4).

#### 3.7.1. Introduction to CMP

Chemical mechanical planarization, [IBM Patent US4944836 1990] was first introduced to solve back-end alignment issues due to the multiplication of interconnecting metal layers. When patterning new interconnections into a capping oxide which is too conformal, – not planar enough – all the topological variations are cumulated in the top layer (Figure 3.57a). This may cause defects in lithography steps limiting the interconnection density and any efforts for scaling the transistors could be lost. Introduction of CMP for copper interconnects enables designs with up to 11 metal layers as in the 28FDSOI chip of Figure 3.57b. Ever since, CMP has evolved to tackle numerous challenges from the original back end of line (BEOL) down to the front end of line (FEOL) [Zantye 2004], [Dysard 2010 ECST], [Balan SSDM 2016]. Shallow trench isolation (STI), gate last based integrations (Figure 3.57c), [Mistry 2007], [Dysard 2010 ECST], self-aligned contact (SAC) (Figure 3.57d), [Niebojewski 2014 SSE] all needed in sub-7nm nodes technologies require state-of-the-art CMP processes with nanometric precision and ranges not only across the chip but also all across the whole 300 mm diameter wafer. The two gate last processes developed in this thesis framework are not an exception and the success of these integrations considerably relies on CMP quality level as shown in the present subchapter.

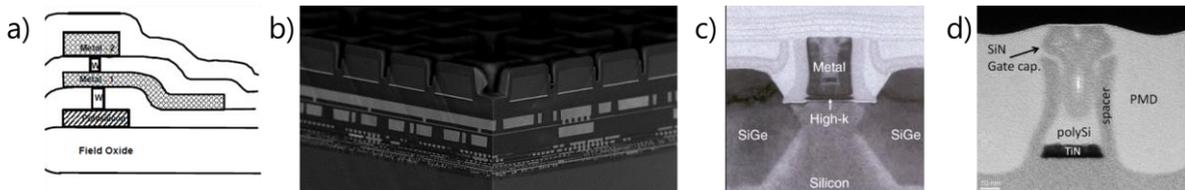


Figure 3.57 - (a) Illustration of non-planar multilevel metal interconnects. (b) SEM image of a STMicroelectronics 28 nm FDSOI chip cut with its 11 interconnect layers. (c) First replacement metal gate process in Intel 45 nm technology [Mistry 2007]. (d) Demonstration of first step of SAC module on 14 nm FDSOI technology (SiN stopper above polysilicon gates).

CMP consists in a double action of a polymer pad in collaboration with a chemical slurry (Figure 3.58). Optimizations reside first in the chemical composition of the slurry which selectivity is tuned towards designed materials by playing on a chemical additive. Sometimes, abrasive nanoparticles are added to enhance mechanical interaction with the wafer surface. The pad is optimized with different stripes and geometries to facilitate the intake of slurry and the evacuation of byproducts. Precise control of the mechanical pressure, rotation speed and temperature

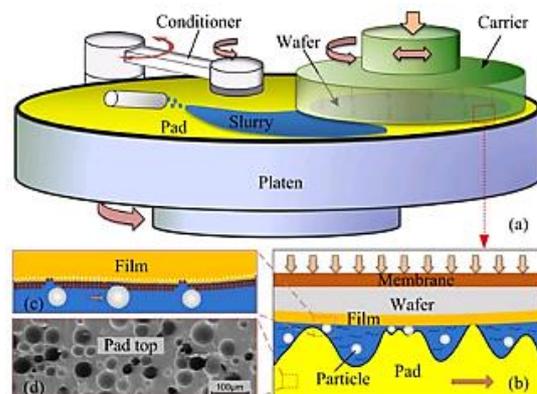


Figure 3.58 - Principle of CMP: (a) set-up schematics, (b) wafer/pad interaction, (c & d) zoom-in [ZhaoD 2013].

are vital as well as the uniformity of these parameters throughout the wafer surface. Yet the removal rate  $R$  is proportional to the applied pressure  $P$  as related in Preston equation (Eq. 3-6) with  $K$  the Preston constant and  $V$  the relative speed:

$$R = K \times P \times V \quad (\text{Eq. 3-6})$$

This may be an issue as pictured in Figure 3.59 when designs involve different patterns density. The smaller the patterns, the lower the contact surface with the pad and the higher the pressure so as the removal rate. This is the source of residues or over-erosion if an over polishing (OP) is applied to remove these. Consequences for the subsequent CMP steps are short-circuits and non-connected vias in case of arcing. Erosion is a physical effect related to pressure while dishing is a selectivity issue encountered when polished material is removed faster than its counterparts.

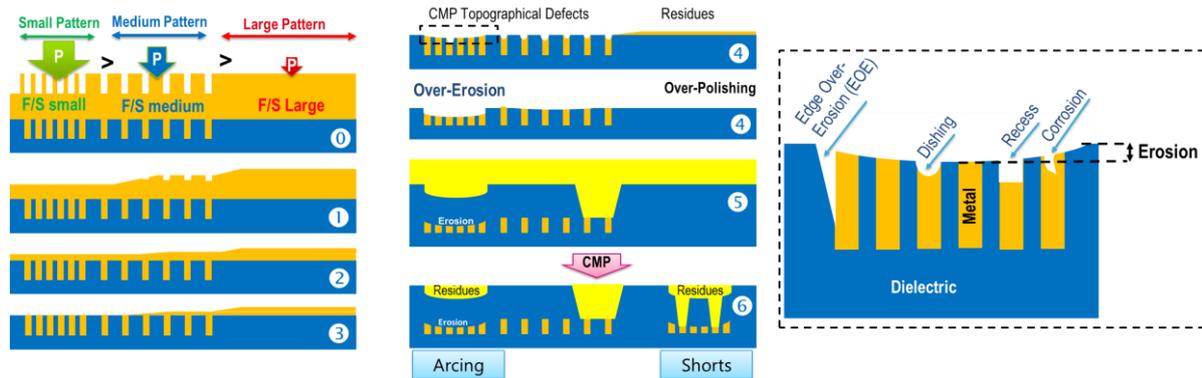
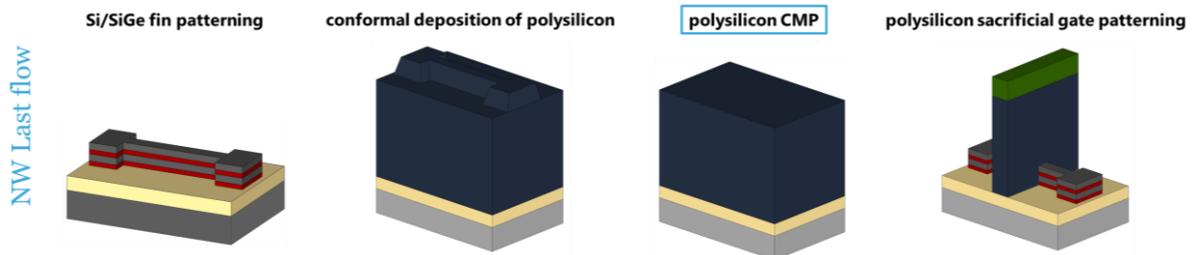


Figure 3.59 - CMP topographical defects: related sources and issues.

### 3.7.2. Polysilicon sacrificial gate CMP (NW Last approach)



In the NW last approach, the active layer consists in 35 nm tall Si/SiGe fins and dummies. As observed in the previous section, most of the defects in CMP process result from the lack of uniformity in the subsequent patterns. As the present layout is composed with many single and isolated devices, most of the chip layout is therefore covered with dummy patterns as shown by the SEM image of Figure 3.60. In order to pattern the sacrificial gates, a 189 nm thick polysilicon conformal layer is deposited. Hence, the objective of the following CMP is to planarize the polysilicon surface in preparation for the sacrificial gate lithography. Figure 3.60 includes cartographies of the whole wafer surface before and after CMP showing a wafer range below 5 nm. AFM measurement of Figure 3.60 was performed after CMP on a  $10 \mu\text{m} \times 10 \mu\text{m}$  surface centered in the exact same area than for the SEM image. The step due to the conformal deposition of polysilicon above 35 nm active areas and dummies is properly planarized. Local range is about 5 nm with a rugosity of 0.6 nm (RMS).

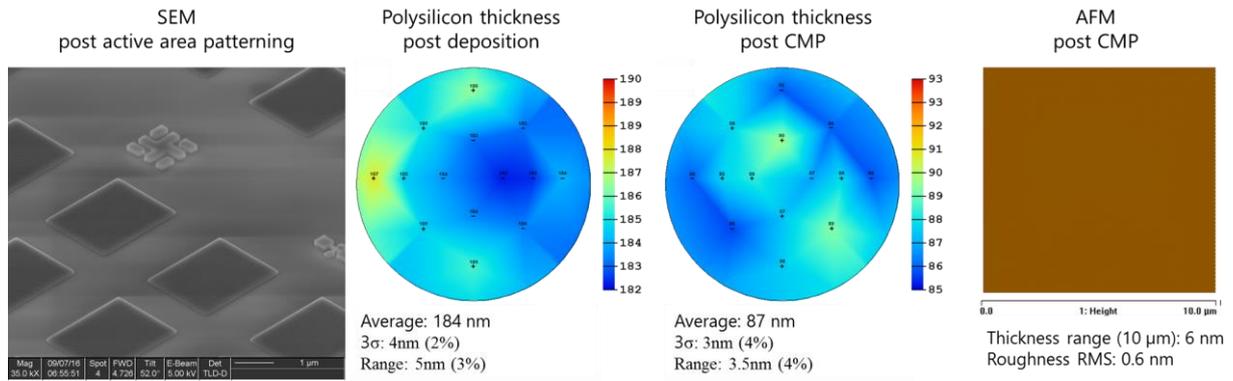


Figure 3.60 - Results of polysilicon CMP erasing an active layer to BOX step height of 35 nm.

Figure 3.61 shows the wafer to wafer derivation obtained on a single batch of 25 wafers. Process variation in CMP can be due to pad self-heating or pad and chemistry aging. In order to prevent the first, several dummy wafers are first processed for warming up the pad (pad conditioning). In the present demonstration, the slight variation is not of a big concern however, this would need to be corrected for matching production requirements.

Polysilicon CMP was performed with a constant time per wafer which can also be very precisely controlled by the number of pad rotations at a given speed. Therefore, any process parameter derivation is likely causing a variation of the removal rate (RR) and thus, a variation of the final thickness as observed in Figure 3.61.

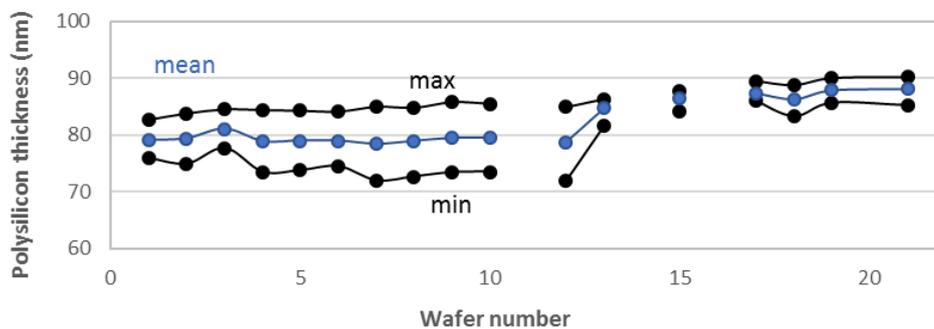


Figure 3.61 - Process derivation with constant time: average thickness is increased by 5 nm in between the first and the last wafer processed.

For improving process robustness, several feedbacks can be implemented on a CMP tool to follow the material removal rate. Directly on the pad, pressure and resistance to rotation can be monitored. In the case of metallic material, Foucault currents can be measured (see §3.7.4). If the CMP is selective towards one or several materials, the pad can stop onto specific features (§3.7.3, §3.7.4).

Unfortunately, the development test layout used in this thesis have several areas empty of dummies such as the peripheral parts needed for metrology purposes presenting either positive or negative topography as shown on Figure 3.62a-b. Thus, the SEM images of Figure 3.62c and d show two sections of the same 2 cm wide chip distant from 1.6 mm: a variation of the polysilicon thickness of 26 nm is observed. Since, polysilicon thickness is monitored by ellipsometry in dedicated metrology boxes, the on-chip thickness variation cannot be properly quantified and such cross-section SEMs are required.

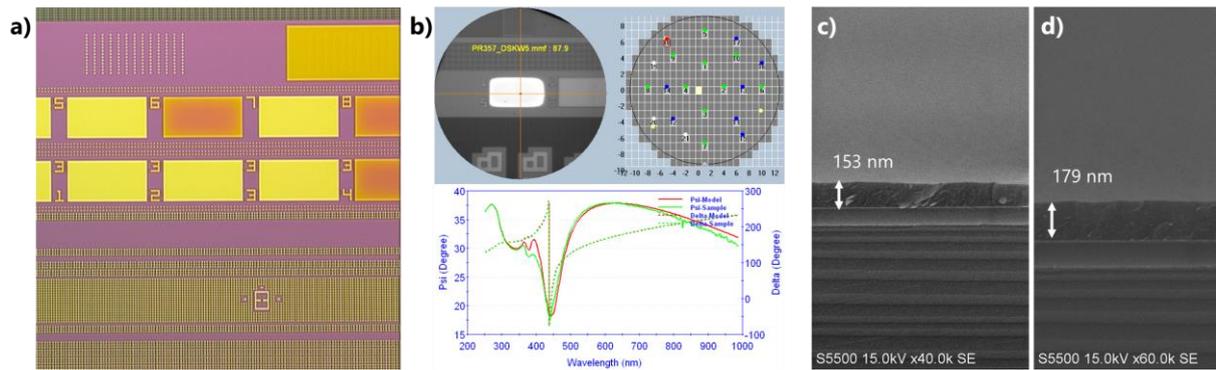


Figure 3.62 - (a) Optical photograph of the chip surface showing the peripheral part with metrology boxes. (b) Nanometrics eplisometer measurement windows with the optical view centered on a measurement box, the chip selectors on a wafer map and the correlation graph. (c) and (d) are two SEM cross-sectional images of two points distant from 1.6 mm showing a difference of 26 nm in the polysilicon thickness.

The lithography and etch of these polysilicon features requires only few comments in the framework of this thesis. First of all, the higher the gate the more space is available in the vertical direction to endure the numerous CMP and overpolishing, while keeping a safe margin above the NW stack for placing a SiN stopper in a SAC approach. However, the higher the gate the more sensitive the process is to collapse due to high aspect ratios. Keeping a vertical profile on higher gates is also more difficult. Therefore, the polysilicon sacrificial gates were etched into a 105 nm thick polysilicon layer with a 35 nm thick SiN hard mask. The SEM image of Figure 3.63 shows a 70 nm tall polysilicon sacrificial gate above a NW stack with a minimal length of 25 nm.

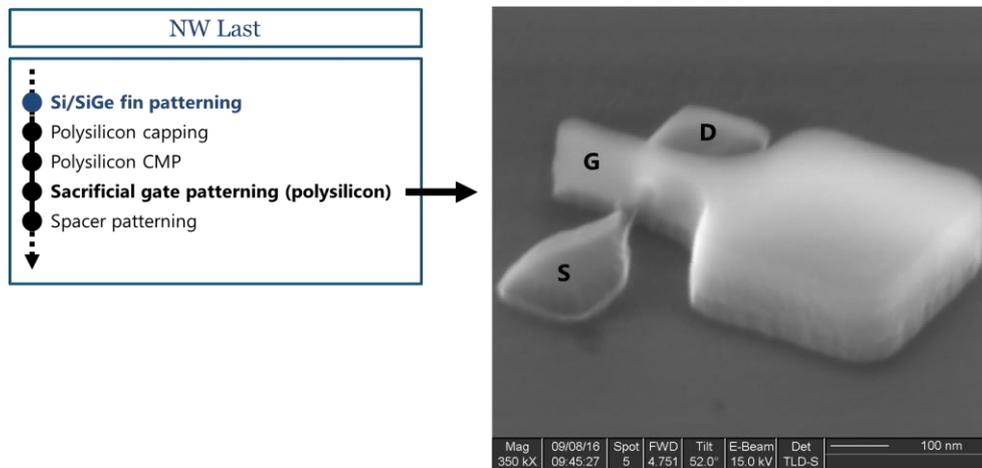


Figure 3.63 - SEM image of a 70 nm tall sacrificial polysilicon gate after etch.

The polysilicon layer uniformity, and thus of the polysilicon CMP, must be excellent to prevent any issue during lithography and etch. The SEM image of Figure 3.64a is an example of an active area that have been damaged due to a too long exposition to ion bombardment and etching. Indeed, while the polysilicon in this area was completely consumed, other areas were still not entirely etched down to the BOX. This can be monitored by following the emissive ray intensity specific to one chemical specie associated to the etched layer and/or reaction byproducts concentration. Figure 3.64b is a schematic that compares the signal provided by different wafers: the transition for a very uniform layer is much

faster than a non-uniform layer which signal extend longer. In conclusion, significant efforts must also be deployed concerning the CMP as explained later in the last subchapter (§3.7).

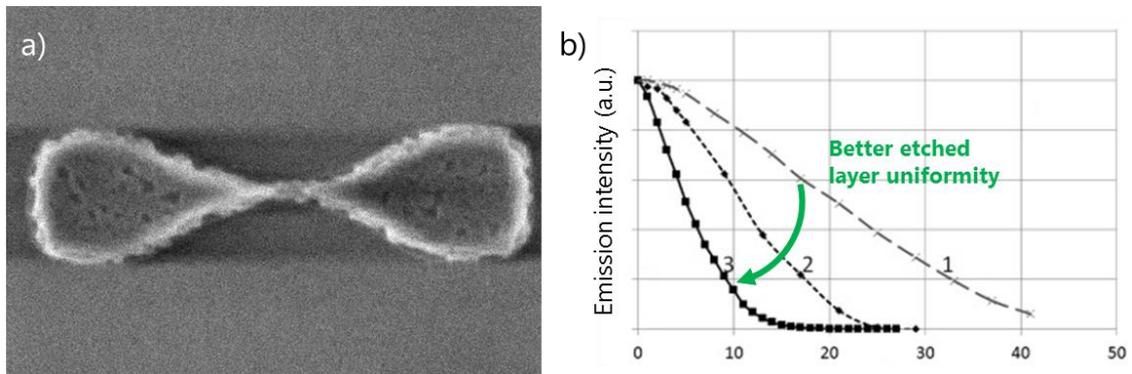


Figure 3.64 - (a) SEM image of an active area damaged by a too long plasma etching: this will cause important defects in the following S/D epitaxy. (b) Schematic of an emissive ray signal obtained during plasma etching of different wafers: the better the thickness uniformity of the etched layer, the faster the transition

Up to 40 nm difference has been found in between low areas principally within the edges of the chips and the devices located in the middle. One way to tackle this issue is to insert a new patterning step prior the CMP. By means of a new lithography mask, the polysilicon in high areas is etched down in order to regain uniformity and to facilitate CMP (Figure 3.65).

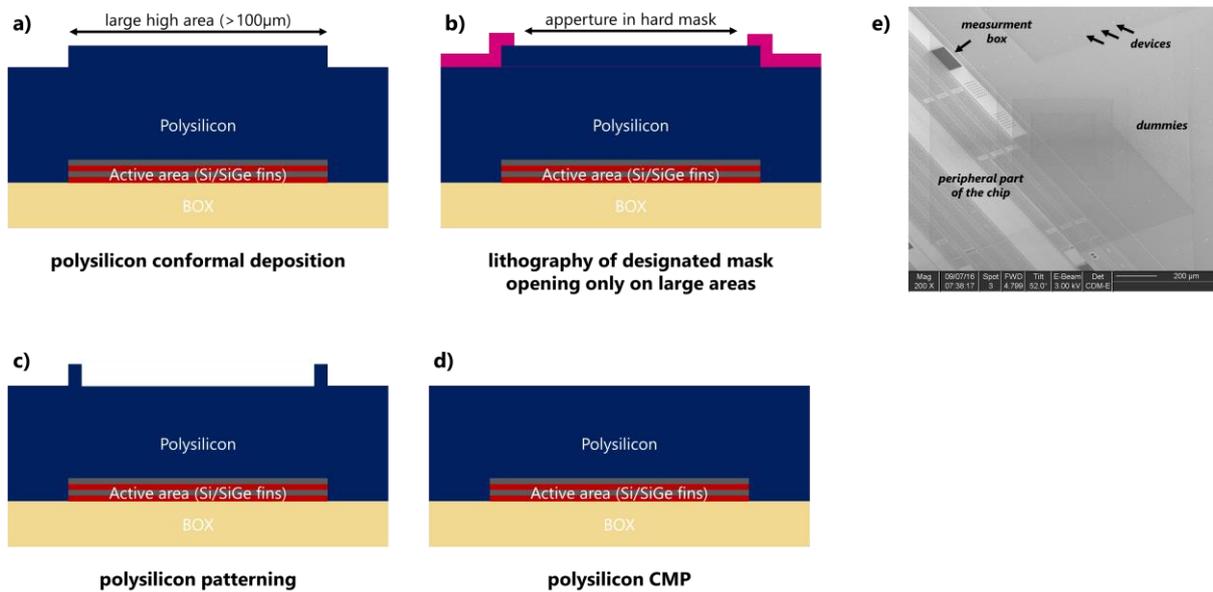
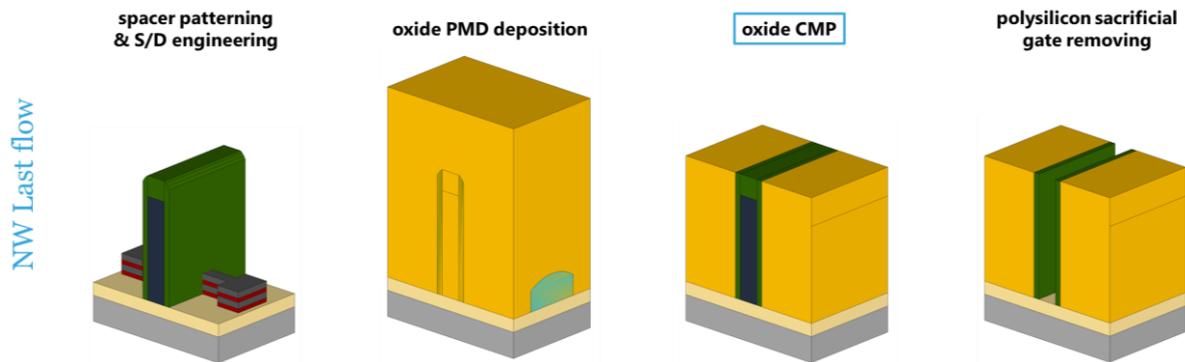


Figure 3.65 – (a-d) Principle of high area patterning in order to facilitate CMP. (e) SEM top view of one of the chip.

### 3.7.3. Sacrificial gate opening CMP

**Poly-Open-Polish: gate last CMP of the oxide capping for the NW Last approach.**



Usual gate last processes feature a step of high density plasma (HDP) oxide pre-metal dielectric (PMD) CMP. Once the transistors S/Ds are built around the sacrificial gates, a protective CESL is deposited above as well as an oxide capping. Therefore, the objective of this CMP – next to planarizing the PMD for the latter patterning of the contacts – is to reach the polysilicon sacrificial gates buried under so they can be removed and replaced by an HKMG. A high selectivity towards SiN is required to have both a complete stop on the top of the gates and a uniform gate height across the chip. Nitride polish rates are adjusted through the pH which govern kinetics of the hydrolysis of the nitride film [Dysar 2010 ECST]. High silicon nitrides removal rates might be required in gate last processes to also get rid of the nitride hard mask (HM) and of the spacers along with tunable selectivity on oxide. However, in the present case, for the integration of SNWFET within a NW last approach, the whole height of the SiN HM needs to be preserved as this space will be later required for building the final SiN stopper above the HKMG.

The SEM images of Figure 3.66 show a single device surrounded by active and gate levels dummies before the oxide capping and after a successful CMP: the SiN HM have been reached and no additional wafer range have been introduced according to ellipsometry measurements of the PMD oxide thickness. The excellent selectivity of the process allowed the application of an overpolishing for decreasing the chances of failure in opening the gates.

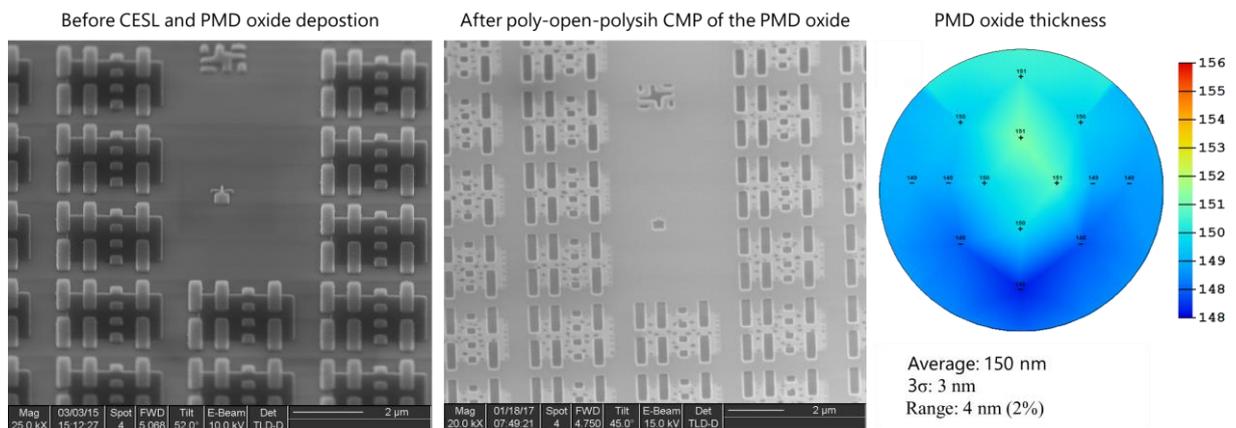
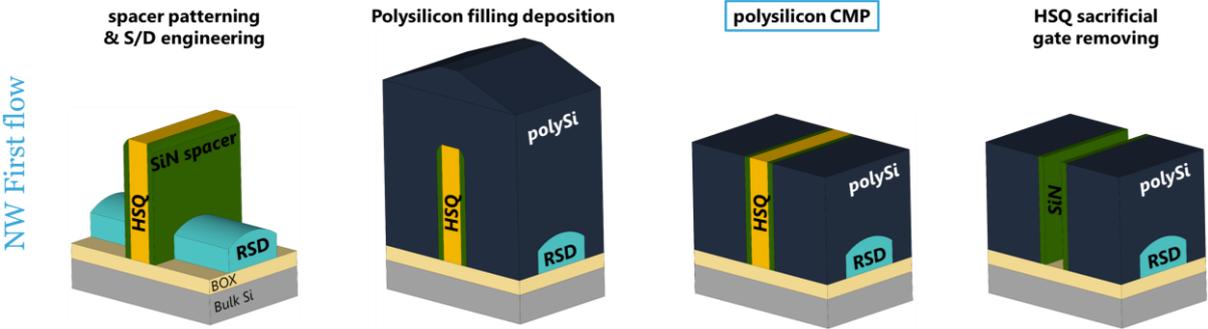


Figure 3.66 - SEM images before and after CMP of the PMD oxide

Finally, for accessing the gate, an optimized step of SiN etching needs to be performed. Thereafter, the sacrificial polysilicon gate can be removed with a TMAH solution.

**NW First alternative with HSQ oxide sacrificial gate and polysilicon filling.**



Unlike with the NW Last option, the NW First approach with HSQ sacrificial gates is not compatible with an oxide capping. Indeed, to remove HSQ oxide with a significant selectivity, the material used for filling cannot be also an oxide no matter the relative densities. To overcome this issue, flowable oxide such as HSQ (non-conformal) was suggested for obtaining an as-deposited planar oxide filling [Coquand USXXXXXX] prior to the addition of a SiN conformal capping intended to protect the oxide during the removal of the HSQ sacrificial gate (Figure 3.67).

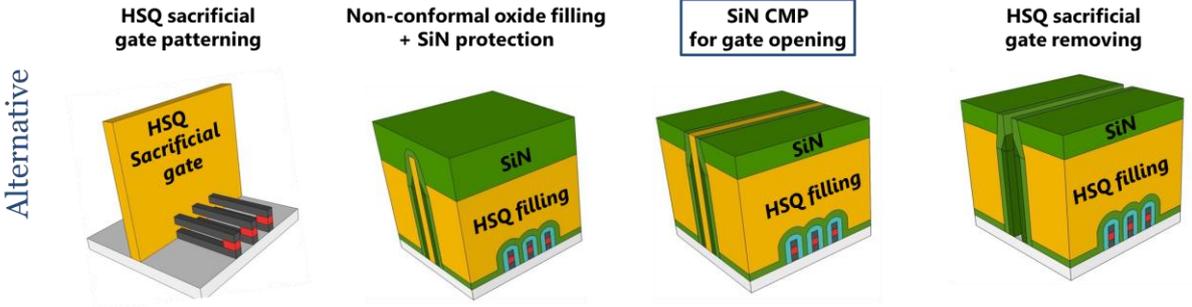


Figure 3.67 - Alternative to polysilicon filling with flowable oxide and SiN protection for oxide sacrificial gate selective removal.

Instead, another option was proposed and tested in the framework of this thesis: by using only polysilicon for the capping, the HSQ oxide can be selectively removed with some HF. This avoids developing the complex capping with the two layers suggested above. Besides, the polysilicon CMP process as previously described in §3.7.2 can be adapted which avoids developing and maintaining an additional specific process for the NW first approach.

Figure 3.68 shows the layout configuration, with SEM images of the devices and of the dummies. An AFM mapping also shows the topography of a single transistor with S/D and a double contact pads HSQ gate which remains 170 nm tall. The epitaxy of the S/D has already been made adding in between 45 nm to 65 nm to the original 35 nm thick active layer. Besides, as the HSQ sacrificial gates are made patterned with ebeam lithography, the gate level dummies have been removed from the layout to drastically reduce the exposure time. Hence, the oxide sacrificial gates are extremely rare on a chip which makes the CMP process almost insensitive to their presence.

AFM shows the actives dummies have been raised by 45 nm and 65 nm by the Si:P or SiGe:B epitaxies respectively as compared with NW last approach. Therefore, this extra step height must be anticipated for the CMP by depositing a thicker polysilicon capping: instead of 189 nm for planarizing a 35 nm step and targeting a 90 nm final thickness above the BOX, in the present case, 180 nm + 165 nm = 345 nm of polysilicon have been deposited, 180 nm being the targeted thickness above the top of the sacrificial gate while 165 nm are consumed during the planarization process.

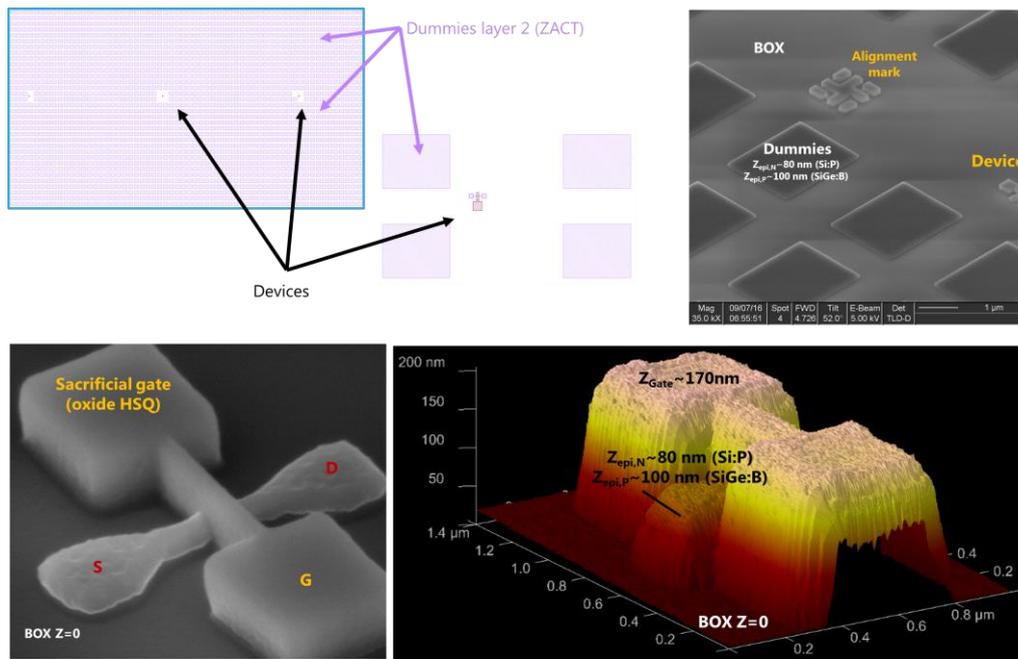


Figure 3.68 - (a) Chip surface (SEM) with active layer dummies and an isolated device after S/D epitaxy, (b) zoom-in of the device and (c) three dimensional build of an AFM measurement.

Unfortunately, the pad/chemistry system used for this planarization is highly selective to both SiN and oxide. Hence, as shown on Figure 3.69, the first polysilicon CMP planarization step must be stopped in the gate vicinity ( $\sim 180\text{nm}$ ) to avoid dishing once the pad is stopped onto SiN and oxide. Afterwards, the slurry is replaced by a non-selective one and the CMP is performed in the last 10 to 15 nm. The switch must be carefully adjusted: if the selective step is pushed too far down, erosion would alter the uniformity. On contrary, if the CMP is stopped too far above the gates, the slow non-selective CMP becomes too long and generates non-uniformity.

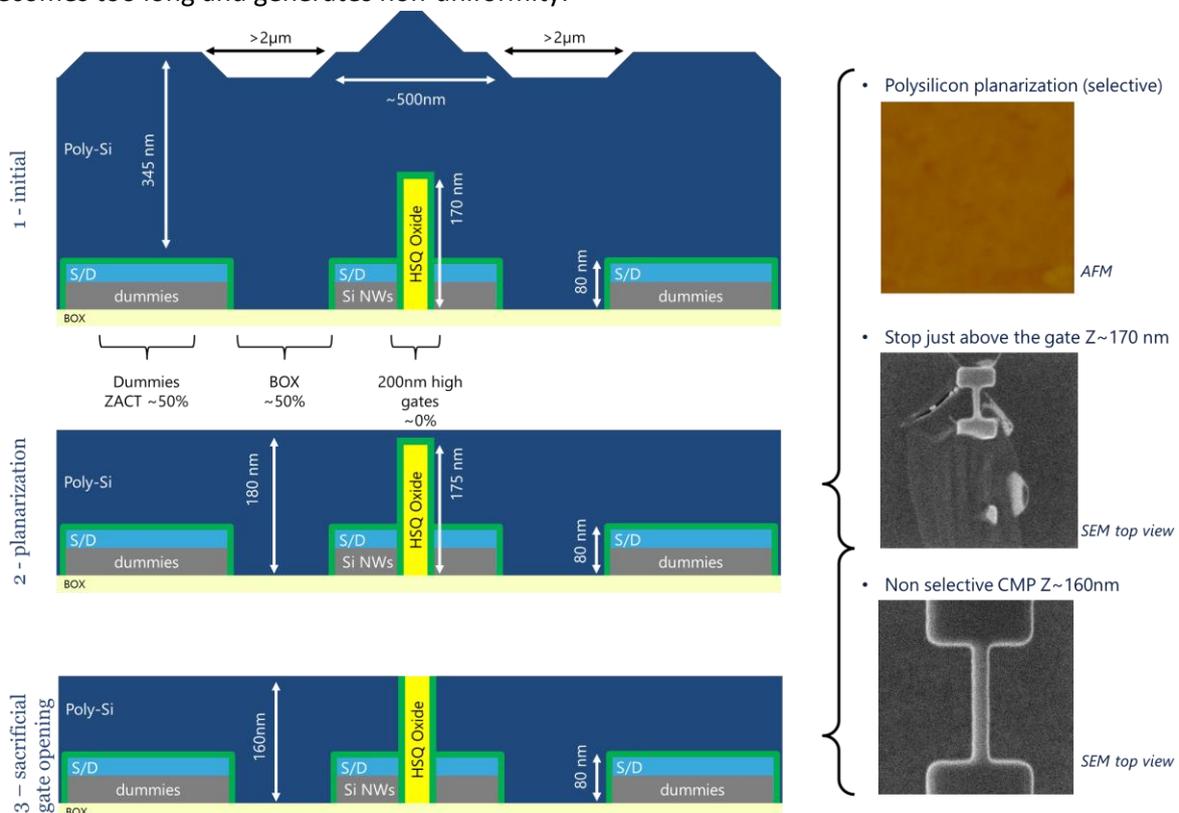


Figure 3.69 - Polysilicon CMP for HSQ oxide sacrificial gate opening.

The two-steps CMP process presents excellent thickness uniformity across the 300 mm wafers according to Figure 3.70. Moreover, the CMP also manages to reduce the range inherited from the HSQ manual spincoating. The first cartography has been obtained out of AFM measurements performed on HSQ sacrificial gates just after developing and presents a range of 11 nm in HSQ feature height. The second cartography shows that the presence of HSQ gates does not modify the performance of CMP as compared with previous results in NW last approach. The third one shows that the last non-selective gate opening CMP does not introduce additional range. And finally, the AFM measurement performed on a 10 μm by 10 μm surface presents a surface roughness of 0.6 nm RMS and no trace of the dummies neither of the devices underneath: planarisation range is therefore excellent and undetectable which makes this solution suitable for very low density layouts (often encountered when using ebeam lithography for exposure time management purposes)

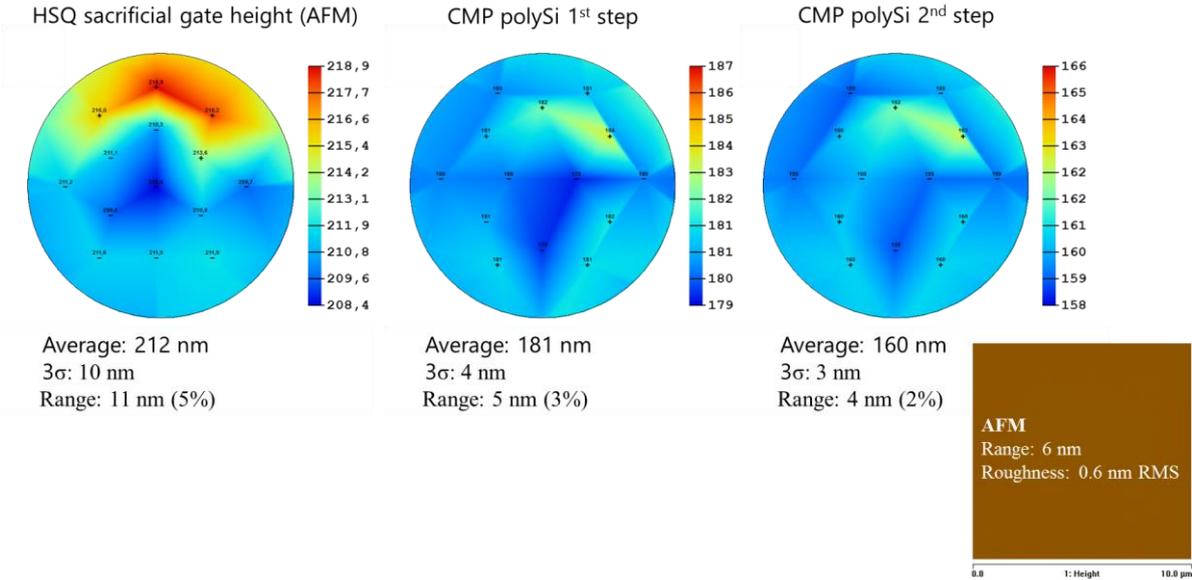


Figure 3.70 – 300 mm wafer thickness uniformity post HSQ lithography and developing (sacrificial gate height measured by AFM) and post the two-steps polysilicon CMP. AFM measurement performed on a 10 μm by 10 μm surface shows a surface roughness of 0.6 nm RMS and no trace of the dummies neither of the devices underneath.

### 3.7.4. Metal CMP (NW Last & NW First)

#### HKMG CMP

Once the polysilicon or the HSQ oxide sacrificial gate are selectively removed, the HKMG can be installed in the empty cavities. A first layer of HfO<sub>2</sub> is deposited and stabilized eventually with a nitridation step followed by a titanium and a titanium nitride barrier. Finally, the gate cavity is filled during the 200 nm deposition of tungsten. The HKMG CMP consists in clearing the gate stack material from outside the gate cavities stopping either on oxide or polysilicon filling as shown on Figure 3.71.

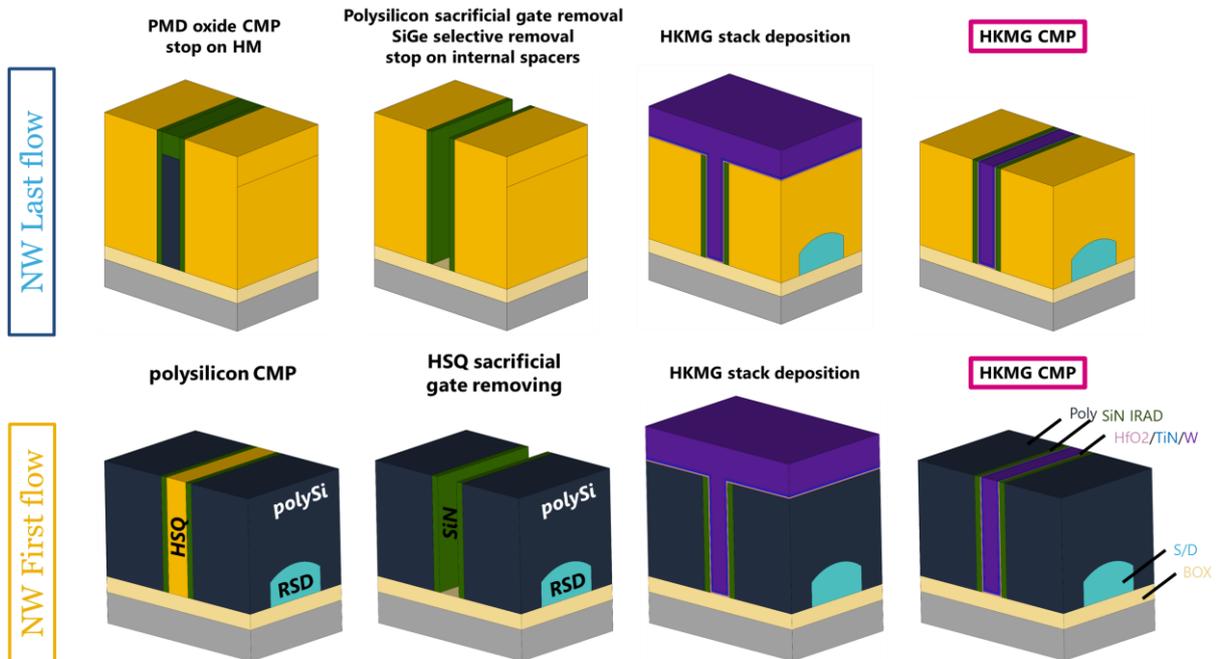


Figure 3.71 - HKMG CMP in NW last and NW first approaches.

Metal CMP process is often followed by measuring the Foucault induced currents. A first planarization step is stopped in the vicinity of the metal/polysilicon or metal/oxide interfaces involving a first hard pad in order to quickly remove most of the 200 nm thick tungsten layer. In a second step, a soft pad is used for improving the surface quality and land selectively on the interface.

A large over polishing time is applied to remove any residues of HfO<sub>2</sub> taking advantage of the slurry excellent selectivity towards oxide and polysilicon. Consequently, a limited degradation of the planarization range has been observed according to Figure 3.72. The degree of planarization remains excellent.

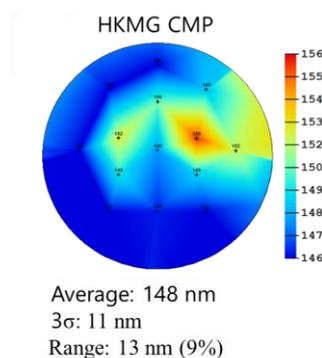


Figure 3.72 – Polysilicon thickness uniformity after HKMG CMP selectively stopped on polysilicon.

The risk of such an important over polishing time is to cause a significant dishing in large features and metal erosion in dense and narrow areas. The images of Figure 3.73 are obtained after the HKMG CMP process stopping on polysilicon (NW first approach) and after TMAH removal of the polysilicon. In the present case, no SiN protective stopper has been built above the HKMG. The TEM cross-sections present a limited dishing of 5 nm. The EDX mapping also shows the good conformality of the deposited layers as well as the absence of voids in the tungsten contact in cavities as narrow as 16 nm with a 160 nm / 16 nm = 10 aspect-ratio.

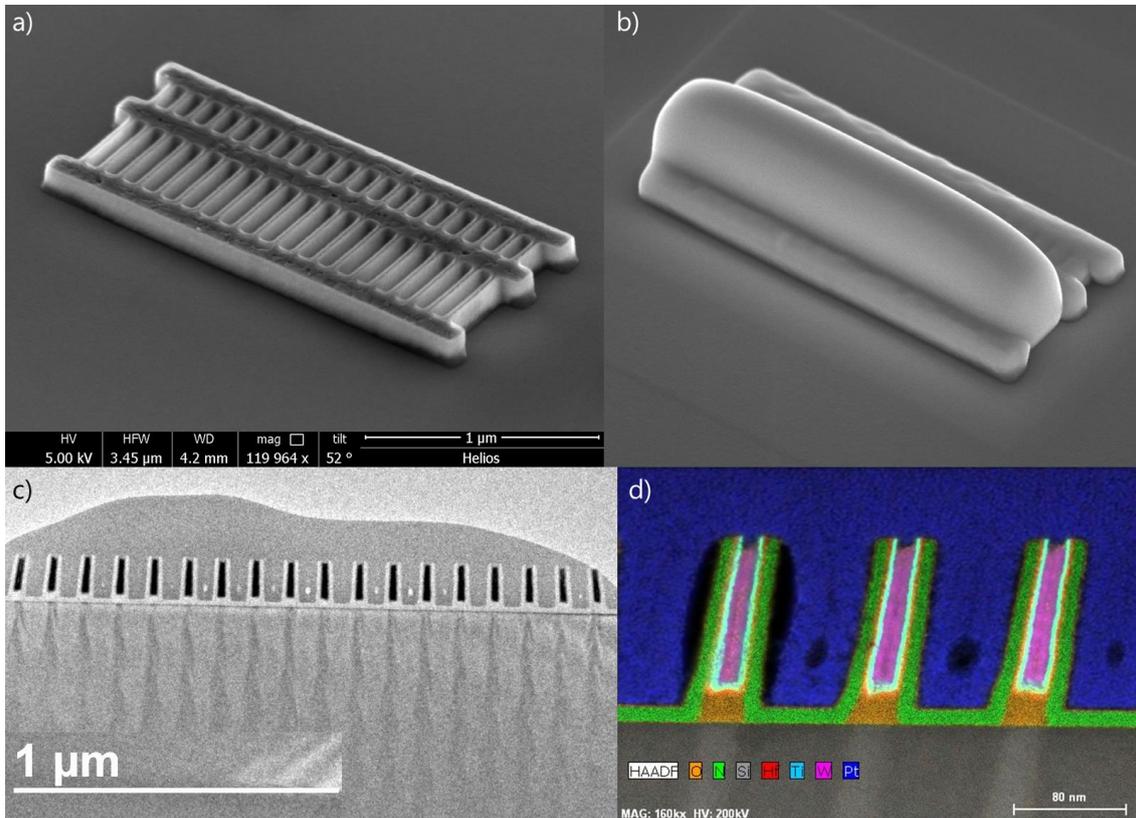


Figure 3.73 - 100 nm pitch array of 16 nm large HKMG after polysilicon CMP. For demonstration purposes, polysilicon filling (NW First approach) has been removed with TMAH and the stacked and suspended NWs are not present. The gates inclination in the EDX mapping is intrinsic to the characterisation technique. (a) SEM image before TEM lamellae preparation (b) with Pt deposition. (c) Cross-sectional TEM image and (d) EDX mapping showing the excellent conformality of the HKMG stack in between the SiN spacers.

The case of NW last approach with HDP oxide filling instead of polysilicon is shown in Figure 3.74 with again almost no dishing.

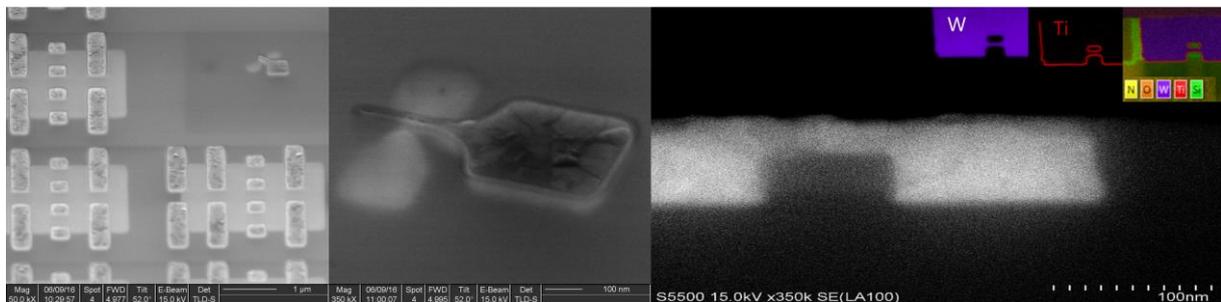


Figure 3.74 – SEM of single isolated device and gate dummies filled with HKMG stack after CMP stopping on PMD oxide (case NW last). The RS/D and active layer dummies are visible by transparency through the oxide. The SEM along a longitudinal section of the HKMG shows the active area crossing the metallic gate (inset: EDX mappings).

### Self-aligned-contact (SAC) CMP (NW Last & NW First options)

As introduced in §3.1, SAC is required for the most advanced and compact integration approaches to prevent misalignment issue during contact patterning which could cause the short-circuit of the gate with the S/D contacts. In both NW last and NW first approaches, a SiN stopper is required on top of the HKMG.

Figure 3.75 presents two TEM cross-section images after a recess of the tungsten in between the gate spacers and after the deposition of a conformal SiN layer (left) and after the SiN CMP stopping on HDP oxide leaving a small amount of SiN above the HKMG (right). The thickness of the HKMG and therefore of the initial sacrificial gate relatively to the stack of NW is crucial. Indeed, the remaining space above the NW stack and the tungsten gate contact is limiting the amount of SiN that can fit in the cavity. Thus, the sacrificial gates (HSQ or polysilicon) must be built initially tall enough to endure all the CMPs and to absorb any range created during these successive CMPs.

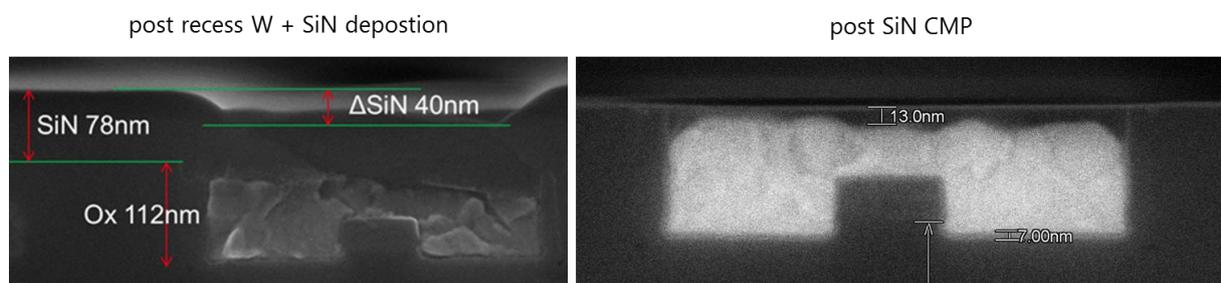


Figure 3.75 – Cross-sectional TEM images before and after the SiN stopper CMP.

A similar CMP process can be implemented in the case of a NW first process flow and a polysilicon filling (§3.1.2) since the selectivity in between SiN and polysilicon has already been demonstrated to be tunable [Dysar 2010 ECST]. However, this could not be developed in this thesis project timeframe and the SAC patterning had to be performed without SiN stopper as shown in the SEM images of Figure 3.76. Since the contact patterning pitch is relaxed, no short circuit is therefore expected. The process flow starts with the patterning of the negative mask of the active layer into a SiO<sub>2</sub> hard mask (Figure 3.76a). The polysilicon is then removed with a hot TMAH solution with an adjusted time to limit material recess under the HM edges (Figure 3.76b). The previous Figure 3.73 represents a configuration closer from a real layout as suggested in the next chapter (§4.2). In that case, polysilicon can be removed with a usual over etch since the etching is stopped in between the array of features. And finally, contact salicidation is performed prior to the tungsten deposition and CMP (Figure 3.76d).

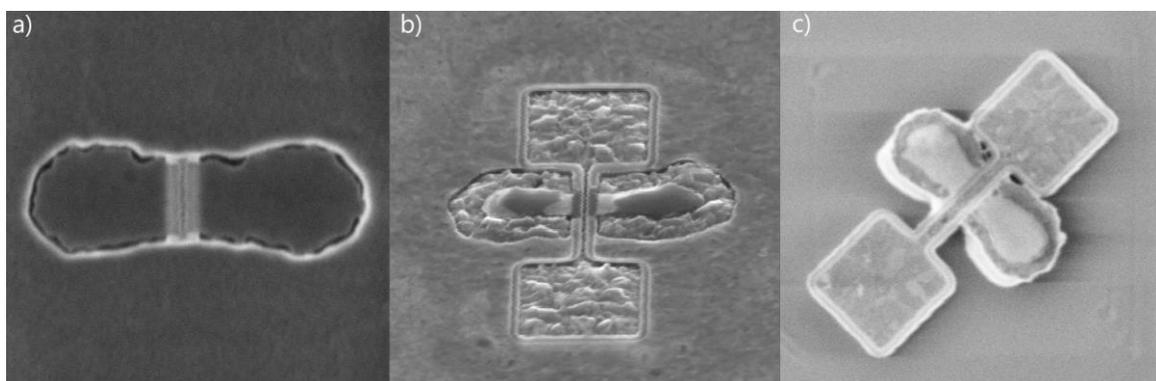


Figure 3.76 - SEM images of a single transistor in a SAC process flow: (a) HM patterning and TMAH removal of polysilicon, (b) HKMG CMP and (c) complete removal of polysilicon prior to contact patterning.

### 3.8. Conclusion

The present chapter has been focused in providing information about specific building blocks of SNWFET technology. In comparison with the gate first integrations of NWFET and SNWFETs fabricated in the past (§1.3), a gate last approach requires several adaptations. Besides, although FinFET technologies are already in production with such an integration mode, opting for NW stacks instead of fins also imposes several specific steps. This was recalled in the first subchapter (§3.1) where two options were proposed to fit the technology requirements pointed out by simulations (§2):

- In the NW last approach, Si/SiGe fins replace usual silicon fins in a FinFET integration. Only four steps differ from FinFET: the epitaxy of the Si/SiGe superlattice, the patterning of the Si/SiGe hybrid fins, the S/D fabrication with internal spacers and the sacrificial SiGe removal for suspending the NW channels (§3.1.1).
- In the NW first approach, the sacrificial SiGe selective removal for suspending the NW channels is performed before the sacrificial gate patterning (§3.1.2). By using a HSQ flowable oxide sensitive to electron beam lithography, oxide sacrificial gates can be obtained. With this non-organic resist, no etching is required since the exposed material crosslinks into an oxide  $\text{SiO}_x$ . Since silicon does not hinder ebeam, HSQ sacrificial gates are self-aligned through the NWs of the stack and subsequently so as the internal spacers.

A few other alternatives and combinations were also described, however, their interest in terms of integration complexity and cost was found limited (§3.1.3).

The second part of this chapter described five essential process developments that were achieved specifically for building SNWFETs:

- SiGe is used as a sacrificial layer for suspending the Si NW channels for several reasons. First, the Si and SiGe lattice parameters are close enough so the epitaxy of Si/SiGe superlattices is possible (§3.2). Secondly, some strain resulting from this lattice mismatch has been observed into the Si and SiGe layers. This could be used to improve mobility in NMOS (tensile) or in PMOS (compressive) transistors. Optionally, when using SOI substrates, the first Si layer can be thinned and doped with Ge allowing to begin the superlattice with SGOI layer (SiGe on insulator). This way, the bottom channel ends up fully suspended to achieve a GAA configuration.
- Si fin patterning has been successfully adapted to pattern Si/SiGe hybrid fins. The SIT process developed previously for non-stacked NW devices can be adapted to achieve 60 nm tall and 20 nm large Si/SiGe fins in 40 nm pitch arrays (§3.3). This enables the fabrication of multi-fingers devices as proposed in the simulation chapter (§2.3) but also makes the SNWFET technology suitable for the very high density of integration required in advanced nodes. Moreover, the stress mappings performed on these structures have shown a full report of the longitudinal stress throughout the entire superlattice after fin patterning. This seems promising to enable channel strain optimization and carrier mobility enhancement in the stacked channels.
- Since the Si-Ge chemical bond is different enough from the Si-Si one, several approaches can be implemented to etch selectively the SiGe regarding to the Si NWs. In §3.4, the wet chemistry was found to provide the best selectivity. Hence, this process was preferred for both carving the internal spacers cavities in between the Si NW channels and for suspending the NWs either in NW first or NW last approach. However, the model developed in the last part of §3.4 raised the attention on the risk of NW buckling which is mainly driven by internal stress.

- In §3.5, the S/D fabrication with internal spacers was explained. In both NW last and NW first approaches, the NW extensions must be first recessed. Therefore, the surface preparation becomes essential for obtaining defect-free S/D epitaxy. Low thermal budget techniques inherited from monolithic application developments have been observed to be compatible with SNWFET integration and to improve the quality of the epitaxy. A low temperature process preserves the NWs from deformation and prevents the stressed materials to relax. SiGe in-situ doped epitaxy of the RS/D was shown to introduce significant channel stress and let expect electrical performance improvement. Regarding the case of a NW first approach, the self-aligned internal spacers are already present when the epitaxy is performed. In a NW last integration, additional steps are added in order to selectively etch cavities in the SiGe in between the Si NWs and a cycle of SiN conformal deposition and etching is performed to achieve the internal spacers.
- The ebeam lithography of HSQ flowable oxide has been evaluated in §3.6 for the fabrication of self-aligned sacrificial gates. Significantly high aspect-ratio have been obtained with 6 nm linewidth for 200 nm height. Sub-60 nm pitch arrays have been achieved and the spacing was found limited to 35 nm in the present conditions. However, promising suggestions have been proposed to either surpass this restriction or to take advantage of it.

The last part of this chapters (§3.7), has shown that the success of these two gate last integrations relies significantly on CMP:

- Since the thickness uniformity is known to affect patterning performances, the polysilicon CMP prior to the sacrificial gate patterning needs to be carefully optimized. In the present case, a specific lithography mask and a patterning step had to be introduced to deal with a non-optimized layout embedding significantly non-uniformities (large areas without any dummies features for example).
- Excellent performances have been obtained for the gate opening CMPs for both NW last and NW first approaches with a wafer range of 4 nm and a nanometric degree of planarization locally. Concerning the later, an innovative approach with polysilicon capping instead of HDP oxide has been proposed: by re-using the polysilicon planarization and adding a non-selective step, the HSQ oxide sacrificial gates could be opened and removed selectively towards the polysilicon fill.
- Once the sacrificial gates are removed and the HKMG stack is deposited, a metal CMP is performed to remove all this material from outside the gate cavity. This CMP must stop either onto polysilicon (NW first approach) or onto PMD oxide (NW last approach). Similar CMP is again performed for the fabrication of self-aligned contacts. However, a SiN stopper must be introduced first by slightly recessing the HKMG and by depositing SiN into this cavity prior to clear out SiN from outside the cavity with another SiN CMP.

In summary, since the available space for the final gate around and above the NW stack is slightly consumed during all the successive CMP, optimizing their performances is imperative: any additional range and selectivity loss adds up and can significantly affects the integration flow.

The present chapter has provided a toolset of techniques for fabricating SNWFETs along with many warnings about the principal variables affecting the processes, the modules and the overall integration flow. By picking and assembling several of these building blocks, SNWFETs have been successfully fabricated. Their electrical performances are analyzed in the following next chapter (§4).

## 4. Achieved integrations and optimization perspectives

The first chapter has given a motivational context behind the development of new SNWFET technologies adapted from existing gate last FinFET process flow and gate first SNWFET. The second chapter has shown the importance of internal spacers for maintaining superior performances above FinFET while the third chapter has provided a toolbox for the fabrication of SNWFETs. Finally, the present chapter is wrapping up this knowledge to analyze electrical performances of a batch of SNWFETs and to suggest improvements for the future of the architecture.

In a first part, electrical measurements performed on gate last and NW last SNWFETs are related to physical considerations relying on previous chapters (§4.1). The second section is dedicated to the less-advanced results obtained with the NW first process flow. At the light of several observations and concerns raised during the experiments and the process developments, several ideas and projections are proposed regarding the potential of HSQ material (§4.2).

### 4.1. Electrical characterization of SNWFETs fabricated in a NW last approach

The present section reports the fabrication of PMOS SNWFETs obtained with a NW last approach assembled from the modules described in the previous chapter. Since this very first electric lot is also a route opener, the integration slightly differs from the optimized one proposed in the beginning of chapter 3 (§3.1.1). The first part thereby consists in providing a detailed process flow along with the related physical characterization results (§4.1.1). The second part focusses on the electrical characterization of these functional devices (§4.1.2). Thus, the results are linked to the process performances with the help of simulations and of previous NWFET characterizations already related in chapter 1.

#### 4.1.1. Device fabrication

The overall process flow of the very first lot of SNWFET is presented in Figure 4.1 to Figure 4.6. This lot is a route opener and does not embed all the parallel learning contained in the chapters 2 and 3. The transistors have been built on 300 mm SOI substrates. The SOI layer was first thinned from 16 nm down to 12 nm (§3.2) prior to perform an epitaxial growth of 12 nm of  $\text{Si}_{0.7}\text{Ge}_{0.3}$  and of 12 nm of Si. A tri-layer hard mask was then deposited prior to the DUV exposure of the usual “SNO2” lithography mask without multiple patterning. Etching was performed in a LAM VERSYS following the process explained in (§3.3). A slight over etch was applied to obtain vertical profiles and therefore identical NW width with a wafer range of about 3 nm as shown in Figure 4.1. A slight isotropic etching of the BOX was applied for forming an  $\Omega$ -gate around the bottom NW as recommended by the simulations performed in §2.2. A broad range of NW width was achieved in between 17 nm and 70 nm to also have nanosheets.

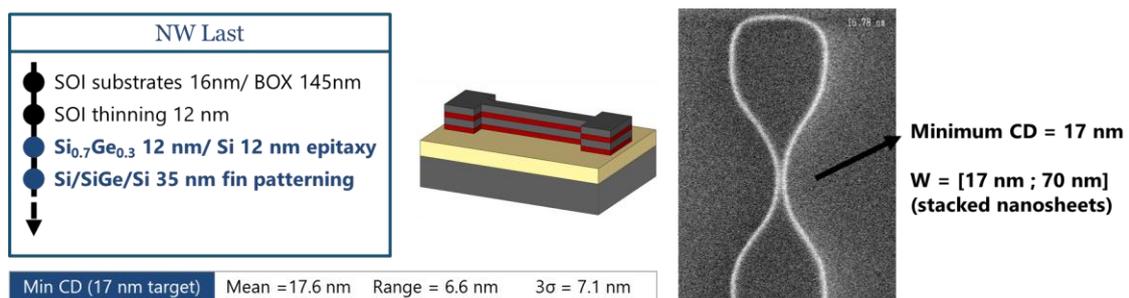


Figure 4.1 – Active area patterning: 36 nm high Si 12nm/SiGe 12nm/Si 12nm fins are obtained.

The (Si/SiGe/Si) fins were then capped with 189 nm of polysilicon. The 35 nm step height due to the presence of the stacks was then planarized aiming for 105 nm above the BOX (§3.7.2). A 40 nm SiN and 27 nm oxide hard mask were deposited prior to the usual tri-layer for DUV patterning of the sacrificial gates. As shown in Figure 4.2, a minimal CD of 26 nm has been achieved.

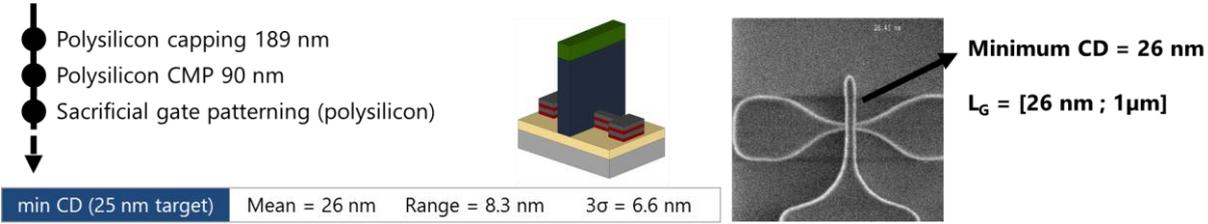


Figure 4.2 – Polysilicon sacrificial gate patterning: 90 nm high polysilicon and 35 nm high hard mask.

The 11.5 nm thick SiN gate spacers were then patterned alongside the sacrificial gate. Some spacer material was also left on the sidewalls of the (Si/SiGe/Si) fins in order to preserve the SiN HM on top of the gates. The NW last approach described in (§3.5) was then conducted for fabricating the S/D with aligned internal spacers. As shown in Figure 4.3, the NW extensions were anisotropically etched down to the bottom NW. The etching was monitored in order to only leave a thin crystalline silicon layer of the bottom NWs which has been used later as an epitaxial seed. The wet process described in §3.4 was then performed for recessing the SiGe in between the Si NW channels. Another 6 nm thick SiN layer was then deposited to fill these cavities and a second anisotropic etch of SiN was performed to clear the silicon NW channels entrances. Finally, a HF last cleaning was performed prior to the selective epitaxial growth of 40 nm of Si<sub>0.7</sub>Ge<sub>0.3</sub> boron in-situ doped ( $2 \times 10^{20} \text{ cm}^{-3}$ ). After patterning the second spacers (15 nm large), doping was improved with an additional implantation of boron followed by a 1050°C activation spike annealing.

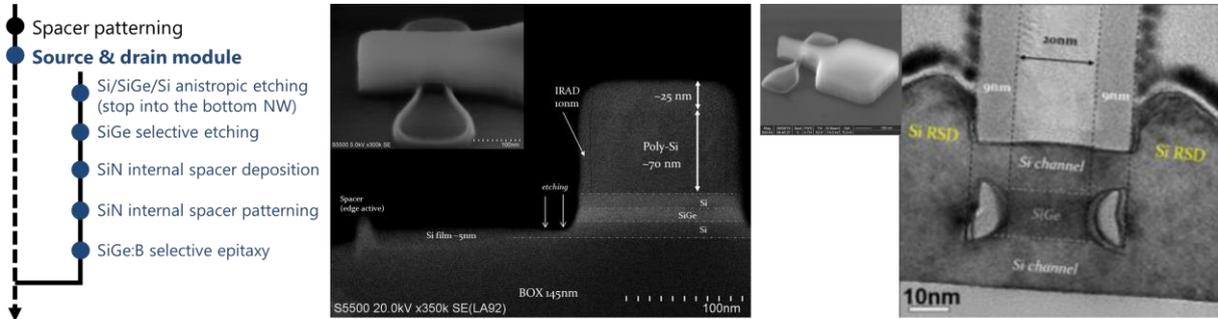


Figure 4.3 – NW extension recess (SEM image on the left) and internal spacer fabrication followed by S/D epitaxy (TEM image on the right and inset SEM image).

For this first lot, a silicide first approach was chosen for improving access resistance without having to develop a SAC module as proposed in §3.7.4. This consisted in the salicidation process described in Figure 4.4. After a Siconi surface preparation, a first layer of NiPt was deposited. An annealing diffused the metal into the SiGe S/D. The BOX as well as the SiN spacers were slightly affected by the cleaning which has a high selectivity towards these materials. SiN prevented the polysilicon gates to be also silicided. Finally, a 15 nm CESL layer was deposited prior to the PMD oxide capping (350 nm of HDP). Since metallic contamination was now embedded on the wafers, a serious care has been taken when using FEOL tools and processes. Dedicated chemical batches were prepared outside of the usual FEOL cleaning equipment and tool qualifications had to be carried out after processing these wafers before authorizing again a normal operating.

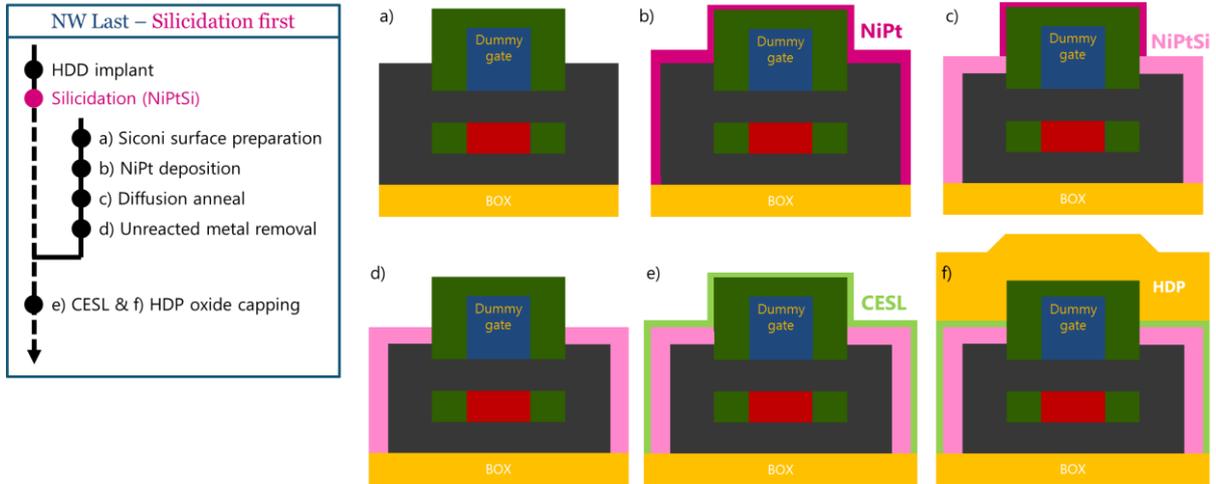


Figure 4.4 – S/D silicidation first module.

The sacrificial gate opening CMP of the oxide capping as described in (§3.7.3) was then performed, stopping selectively onto the SiN HM. The SiN HM was then removed with a chemical wet process for accessing the polysilicon sacrificial gate (Figure 4.5). The difficulty has resided in controlling the etching when having two distinct types of SiN material in presence: the two SiN IRAD spacers fabricated at 650°C and the PECVD HM deposited at 400°C may be etched differently. After engineering the etching process, the integrity of the spacers could be successfully preserved while removing the HM as shown on the cross section TEMs of Figure 4.5.

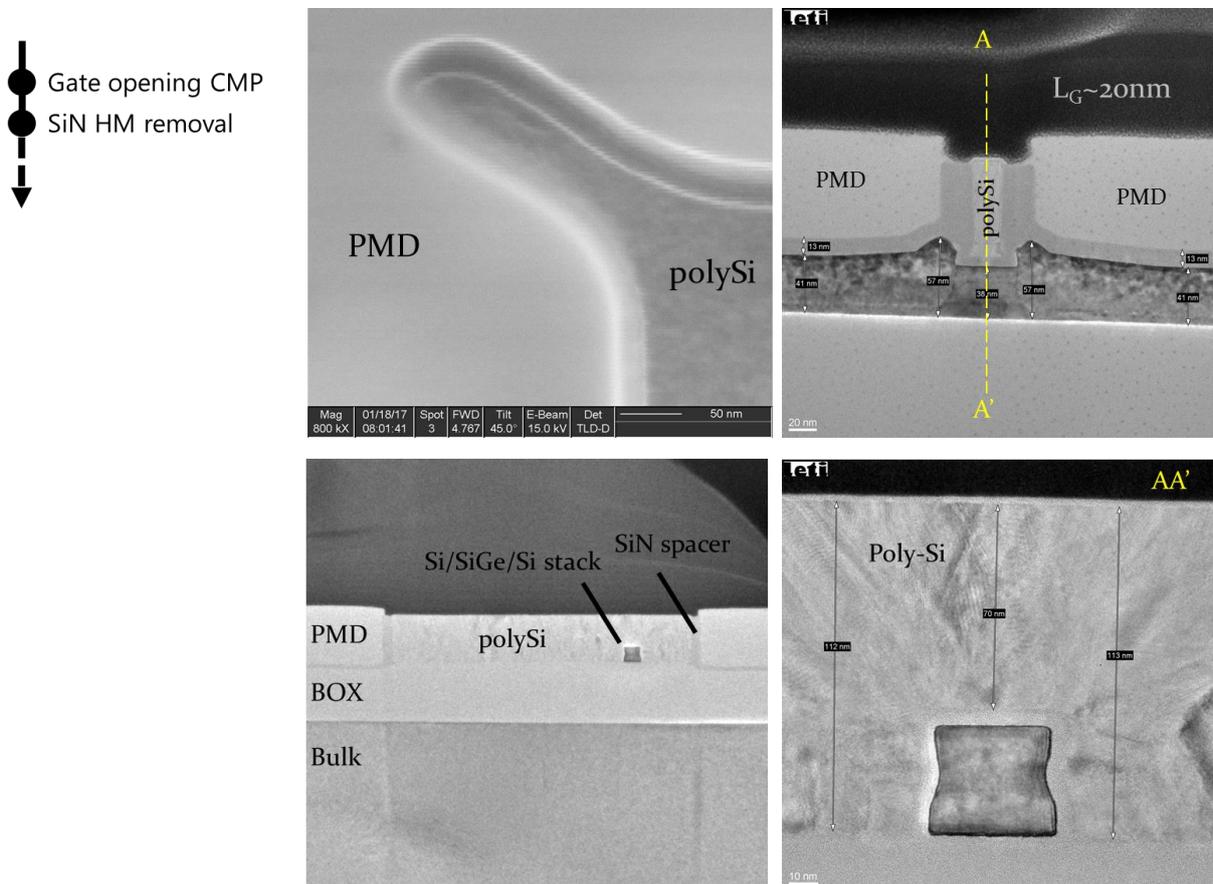
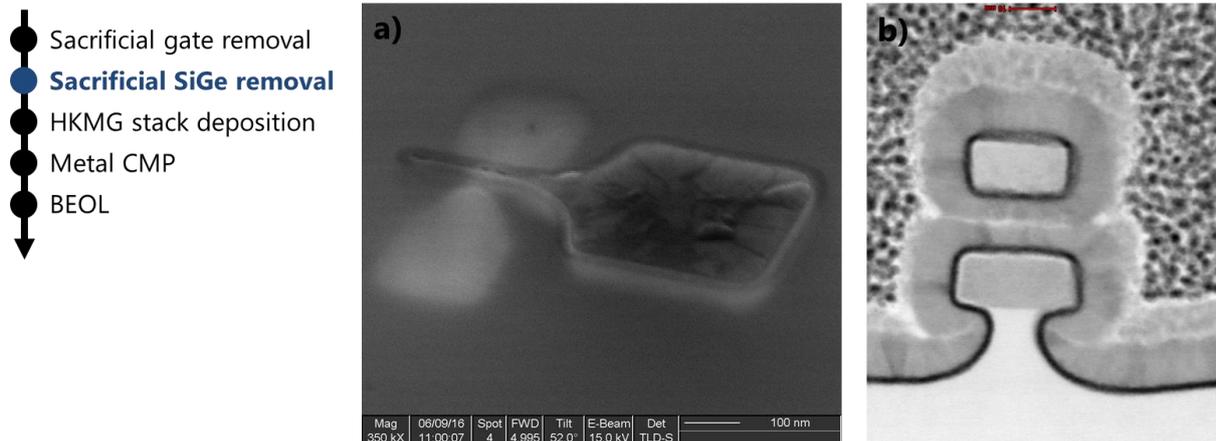


Figure 4.5 – SEM and TEM images post poly-open-polish CMP and SiN hard mask removal.

A solution of TMAH was then used to etch away the polysilicon sacrificial gate selectively towards the PMD oxide, the SiN spacers and internal spacers. Sacrificial SiGe was then removed selectively towards Si NW channels, internal spacers and spacers using the same wet process already described in (§3.4). The two NW channels were then wrapped into HfO<sub>2</sub> and TiN prior to fill the gate cavity with tungsten. The metal CMP was performed as described in (§3.7.4) but was not followed by a SAC module which could not be developed at that time. Figure 4.6 shows that the HKMG material has been cleared out of the HDP oxide and also that the deposition was conformal around the NWs within the gate cavity.



Standard 65 nm process for contact patterning was realized by STMicroelectronics Crolles at the exception of the etching step. Indeed, a specific care had to be taken when etching the PMD and opening on tungsten gate contact and NiPtSi silicided RS/D. In other words, the Ni and Pt contamination level were not appropriate for the middle end of line (MEOL) etching tools in this specific production environment. Finally, back-end of line (BEOL) consisted in a single layer of metal and the copper pads. No additional metal lines have been needed since no complex circuit was designed on this mask set.

#### 4.1.2. Electrical measurements

A collection of PMOS SNWFETs was electrically characterized through capacitive C-V and current I-V measurements. These transistors were made of one or several parallel stacks of two NWs with one suspended GAA NW channel above one  $\Omega$ -gate NW channel laying on the BOX. NW width was in between  $W = 25$  and  $45$  nm and gate length was in the range of  $L_G = 25$  to  $500$  nm.

Figure 4.7 provides the gate to source capacitance dependence on NW width. The measurement was performed on devices having 30 parallel gates and 120 parallel stacks of NWs which therefore averaged the variations. Figure 4.7c shows that the normalized capacitance does not depend on NW width. This extraction made at  $-1$  V allows to extract an EOT of  $1.8$  nm.

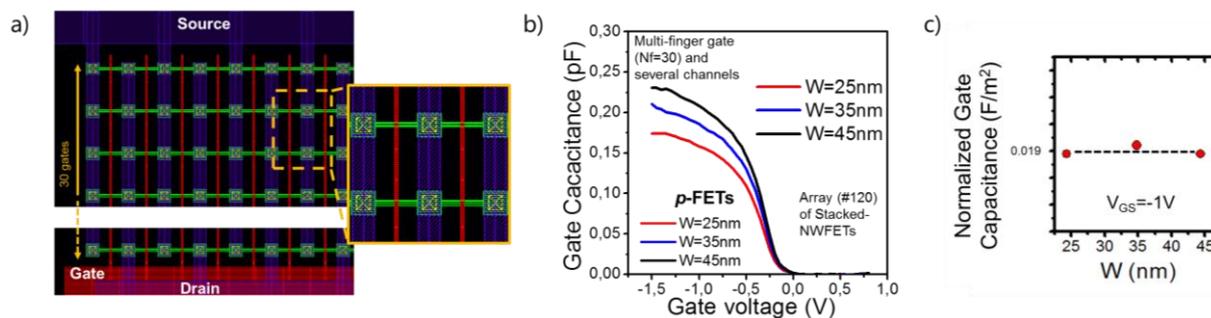


Figure 4.7 - (a) device layout for the (b) C-V measurements for  $W = 25, 35$  and  $45\text{nm}$  stacked NWs. (c) Normalized gate to channel capacitance at  $-1\text{V}$  as a function of NW width. Gate length is  $L_G = 500\text{nm}$ , the array is constituted of 120 parallel NWs and 30 parallel gates.

In Figure 4.8a, the saturation current, measured at  $V_D = V_{DD} = 0.9\text{V}$  for gate lengths in the 25 nm to 70 nm range, evolves linearly with the saturation threshold voltage  $V_{T,\text{sat}}$  indicating the apparition of short channel effects. As expected, Figure 4.8b shows an absolute increase of  $V_{T,\text{sat}}$  with decreasing channel width. Low values of  $V_{T,\text{sat}}$  result from channel under compressive strain due to SiGe S/D (§3.5). The variation is in accordance with simulation of chapter 2.

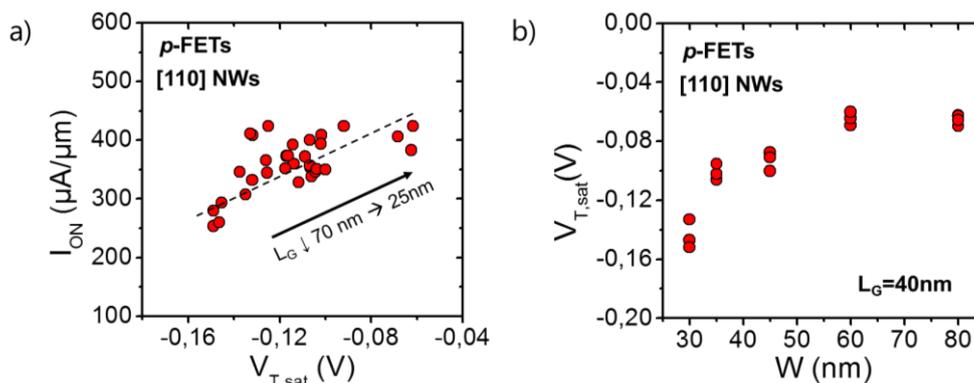


Figure 4.8 – (a) Linear evolution of the on current (normalized by channels perimeter) with the saturation threshold voltage and (b) saturation voltage roll-off with  $W$ .

The DIBL and the subthreshold slope  $SS_{\text{sat}}$  are provided in Figure 4.9 and show the impact of decreasing NW width and gate length on electrostatic control. With a 25 nm gate length, DIBL and  $SS_{\text{sat}}$  are limited to 60 mV/V and 88 mV/dec in average. The results are in accordance with the simulations of chapter 2. Thus, significant improvements can be expected after reducing the thickness of the NW channels and by opting for full GAA devices. As expected from the NW stack and from the sacrificial gate patterning processes variabilities observed in §4.1, a significant spread of the values is noticeable on Figure 4.9.

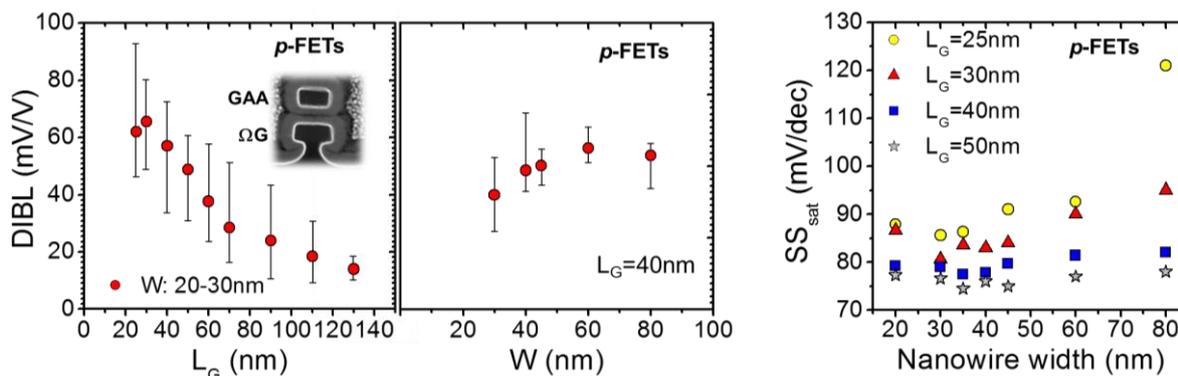


Figure 4.9 - DIBL and  $SS_{\text{SAT}}$  as a function of gate length and NW width.

$I_{ON}$ - $I_{OFF}$  trade-off is also reported in Figure 4.10 for [100] and [110] oriented channels compared to results from [Mertens 2016 VLSI] and [Dupré 2008 IEDM]. As previously observed in trigate NWFETs (§1.3.2), hole transport is favored in (110) surfaces. Since the [110]-oriented devices present four (100) channel surfaces and three (110) ones while the [100] devices have all the seven surfaces in the (110) family of plans, this explains the 130% increase in drive current at constant off-state current observed when orienting the PMOS channels in the [110] direction. Figure 4.10 shows the normalized current is increased by approximately 56% over the devices of [Dupré 2008 IEDM]. A significant part of this performance improvement is likely coming from the compressive strain induced by the SiGe S/D, according to observations on trigate NWs (§1.3.2).

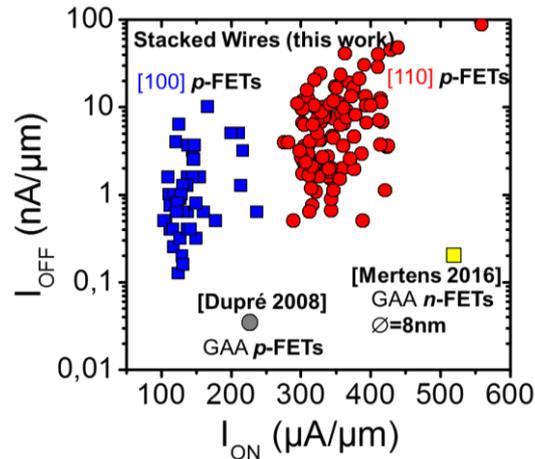


Figure 4.10 -  $I_{ON}$ - $I_{OFF}$  trade-off for [100] and [110] P-type SNWFETs [Barraud 2016] compared to devices reported in [Dupré 2008] and [Mertens 2016] (channels perimeter-normalized).

To summarize these characterizations, a single SNWFET with  $L_G = 25$  nm and  $W = 30$  nm has been selected and its current-voltage characteristic has been plotted in Figure 4.11. A good  $SS_{sat}$  of 80 mV/dec and an excellent DIBL of 50 mV/V are measured along with a 400  $\mu A/\mu m$  effective width-normalized on current at  $V_{DD} = 0.9$  V.

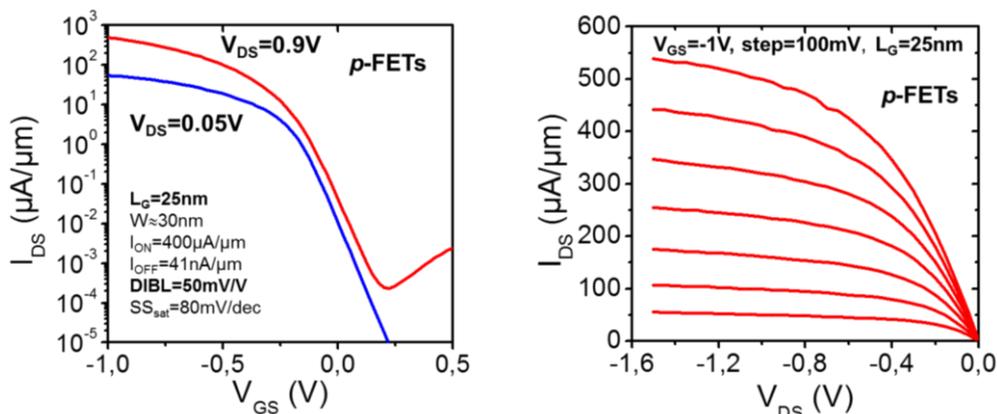


Figure 4.11 -  $I$ - $V$  characteristics of a 30 nm large P-type SNWFET with one  $\Omega$ -gate and one GAA stack NW channels. Gate length is  $L_G = 25$  nm and  $V_{DD} = 0.9$  V.

## 4.2. 3D SAC and STI: HSQ the ultimate resist?

Although a complete electrical characterization could not be performed at the time of writing this thesis, a NW first integration with HSQ sacrificial gates has been carried out up to the contact patterning. Thus, these fabrication steps along with the related physical characterizations are first described (§4.2.1). Based on the observations made during fabrication of these experimental devices, several concepts and innovative approaches are proposed in the second part (§4.2.2).

### 4.2.1. SNWFETs fabricated in a NW first approach

In parallel of the NW last approach, a NW first process flow was conducted. Starting from 8 nm SGOI after SOI thinning and Ge condensation, a 12 nm Si / 8 nm Si<sub>0.7</sub>Ge<sub>0.3</sub> / 12 nm Si superlattice epitaxy was performed following the processes described in §3.2. The LETI SNO2 lithography mask was exposed for patterning the SiGe/Si fins as described in §3.3 without performing multiple patterning. A selective etch of the sacrificial SiGe was conducted with the available dry plasma process described in §3.4. Figure 4.12 shows two 10 nm large and 300 nm long stacked NWs suspended on both ends by the Si/SiGe anchors.

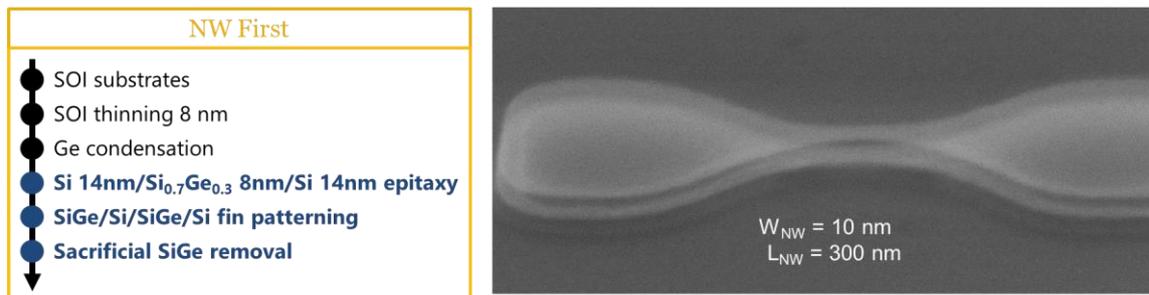


Figure 4.12 – SEM image of two suspended NWs after sacrificial SiGe removal.

The suspended two-NW stacks were then covered with HSQ. The spincoating speed was 2000 RPM leading to 180 nm thick resist. The adaptation of the SNO2 layout described in §3.6 was then exposed with a VISTEC SB3054 ebeam. A slight dose correction on the smallest gate widths (6 to 12 nm) was applied as these small features required a higher than nominal dose to be achieved. After developing, the self-aligned gates remained 212 nm tall in average according to AFM measurements (Figure 4.13). Minimal CD was measured at 6 nm.

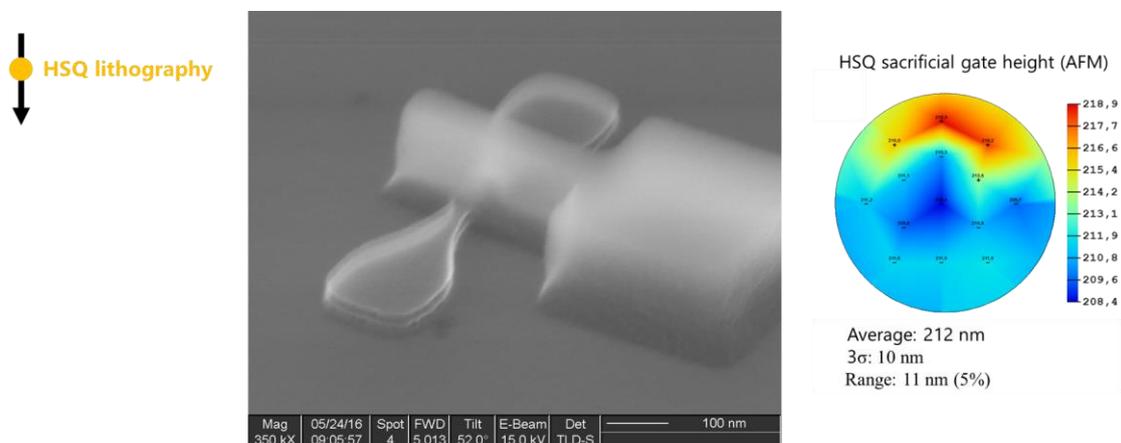


Figure 4.13 – SEM image of an HSQ sacrificial gate onto two suspended NWs and wafer mapping of gate height measured by AFM.

9 nm thick SiN spacers were then deposited and patterned along the HSQ gates. The NW extensions were then recessed by performing successive anisotropic etching of Si and SiN as explained in (§3.5). Only a thin layer of Si in the bottom NW was left as an epitaxy seed. The internal spacers were already patterned and self-aligned with the principal gate spacers so that only an in-situ doped epitaxy of Si:P or SiGe:B was required for reconnecting both suspended NW channel cuts. A second 15 nm thick SiN spacer was patterned for protecting the channel entrances from salicidation. A doping implantation of either boron or phosphorus was performed for decreasing the access resistance. AFM measurements showed a limited vertical consumption of the sacrificial gate height which remained 175 nm high (Figure 4.14).

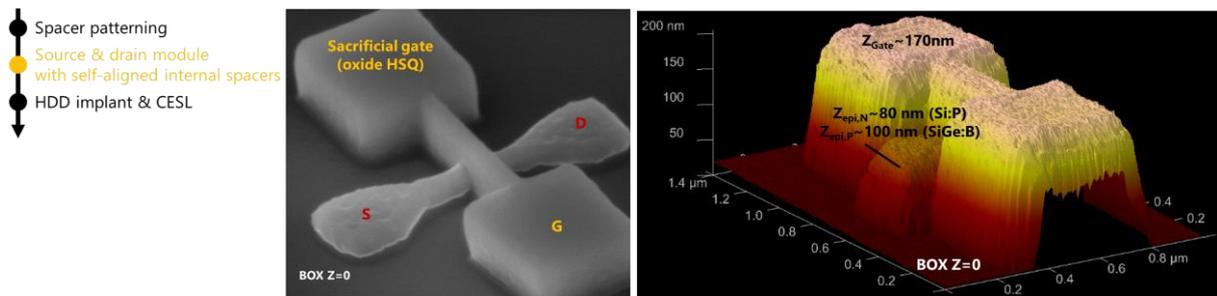


Figure 4.14 – SEM and AFM images of the device after spacer patterning, and S/D fabrication.

A SiN CESL layer of 2 nm was deposited prior capping with 345 nm of polysilicon. The polysilicon CMP as described in (§3.7.3) was then performed: a first planarization step brought the layer down to 180 nm before to switch for a non-selective slurry able to equally remove polysilicon, SiN and HSQ oxide. Unfortunately, even if excellent wafer uniformity was obtained (5 nm range when according to the measurements performed in dedicated metrology boxes), the on-chip variation of the polysilicon suffered from the layout uniformity issues described in (§3.7.2). Although 20 to 30 nm variations were observed, and considering the absence of alternatives at that time, the entire batch has been processed without the improvement described in (§3.7.2).

The sacrificial HSQ removal was then performed in 2% diluted HF. However, a variation of the etching speed depending on gate CD was observed. Besides, a beneficial use of this effect is presented in the next part. However, the selectivity towards the BOX was not high enough to absorb both the difference in between the etching speed in all the different gates and at the same time the additional amount of HSQ to etch due to gate height variation because of the on-chip CMP non-uniformity. Figure 4.15 (top) shows SEM cross sectional images of gate cavities at distinct stages of the HF etch: several gates in the chip center were not opened by the polysilicon CMP while other shorter gates in the edge of the chip had HF etch occurring. The BOX over etch is visible in Figure 4.15 (bottom): this proves that a robust integration of SNWFET using HSQ sacrificial gates requires silicon bulk substrates instead of SOI to have an etch stop layer.

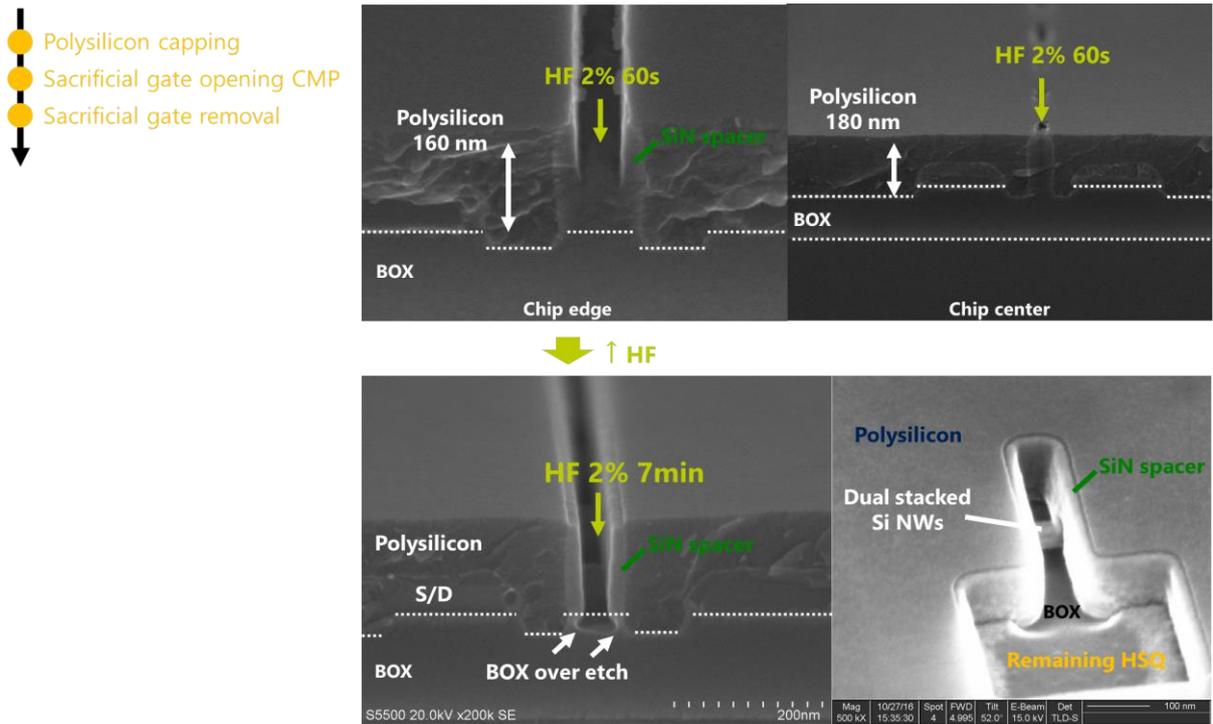


Figure 4.15 – SEM images of HSQ sacrificial gates removal.

The channel surface was then prepared by chemically growing a thin oxide interlayer prior to the deposition of 2 nm of  $\text{HfO}_2$ . The gate stack was completed by a layer of Ti (5 nm) before to fill the cavity with tungsten. All these materials were then polished away from the surface outside of the gate (Figure 4.16).

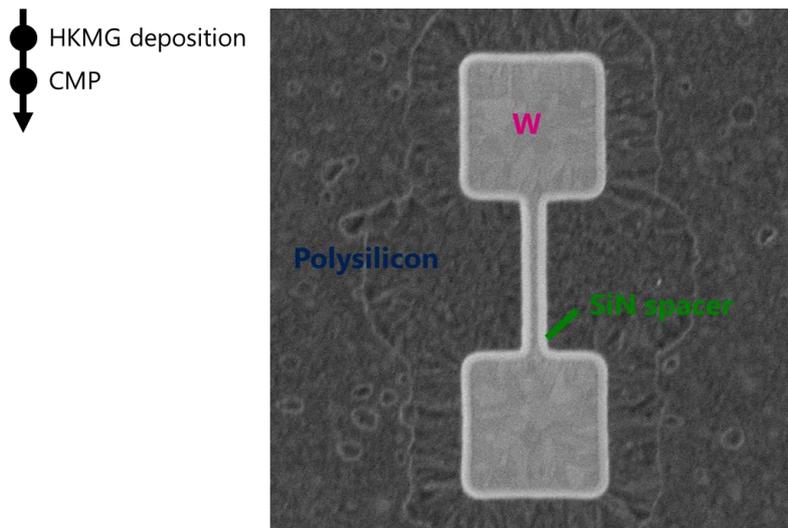


Figure 4.16 – Top view SEM image of a HSQ sacrificial gate replaced by HKMG after CMP stopping onto polysilicon filling.

In order to reach the S/D and to make the contacts, a 45 nm oxide hard mask was deposited above the polysilicon filling and was patterned using the inverse of the active area lithography mask. A hot TMAH wet etch was then performed with a controlled time to remove the polysilicon above the S/D. Although the etching direction cannot be controlled in such polycrystalline material (etch rates can vary from 1 to 100 ratio depending on the grain orientation), the double gate contact design prevented any future short circuit by the top of the gate with enough margin.

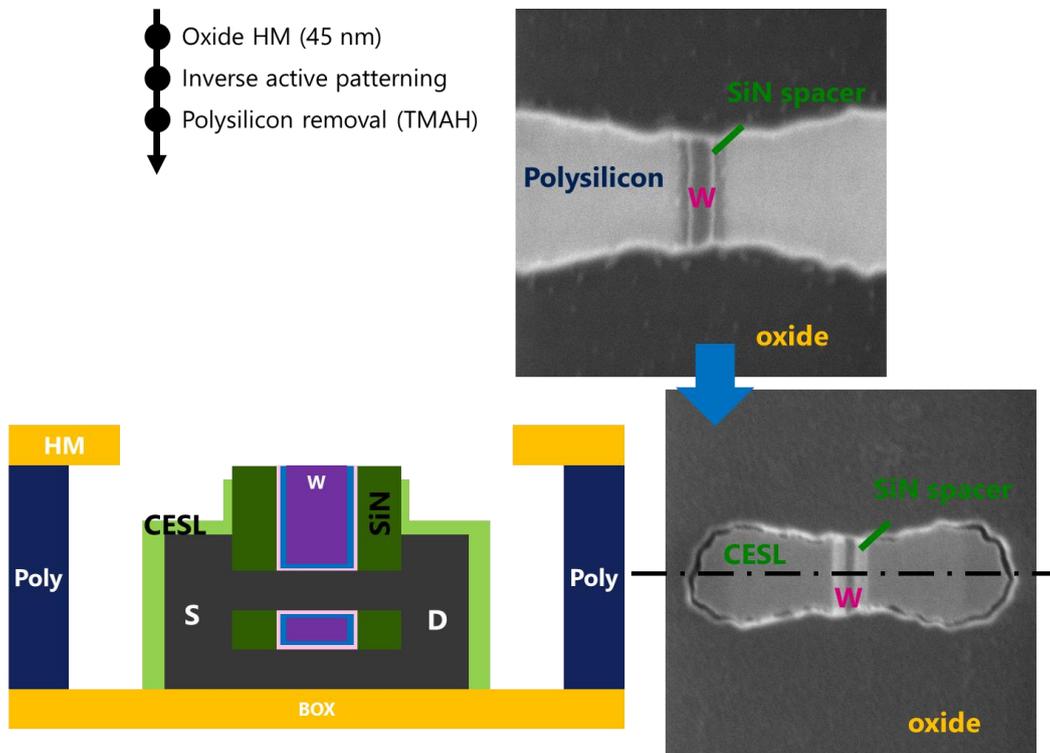


Figure 4.17 – Contact opening in a self-aligned like process.

This palliative approach is not suitable in an industrial process with a high device pitch: a realistic self-aligned contact process would require to recess the HKMG and to place a SiN stopper on top by means of an additional SiN CMP (§3.7.4). This SiN stopper is intended to isolate and to protect the HKMG during the anisotropic plasma etching after the inverse active mask lithography and during the S/D salicidation.

In order to finalize the contacts, S/D salicidation must be performed. However, since no SiN stopper was implemented, the usual wet cleaning of the unreacted metal residues could not be performed with the risk to empty the metal gate. An alternative approach relying on metal CMP was preferred: in this case, the NiPt layer is expected to be entirely transformed into NiPtSi near the Si or SiGe S/D while the unreacted metal is left on the side of the SiN spacers. Then, tungsten was deposited to fill the cavity and another metal CMP was performed to clear the NiPt and the tungsten from outside the contact cavities (Figure 4.18). Finally, a TMAH wet etch was used to clear the polysilicon off the wafer and a usual BEOL process have been performed starting by the deposition of a HDP oxide PMD.

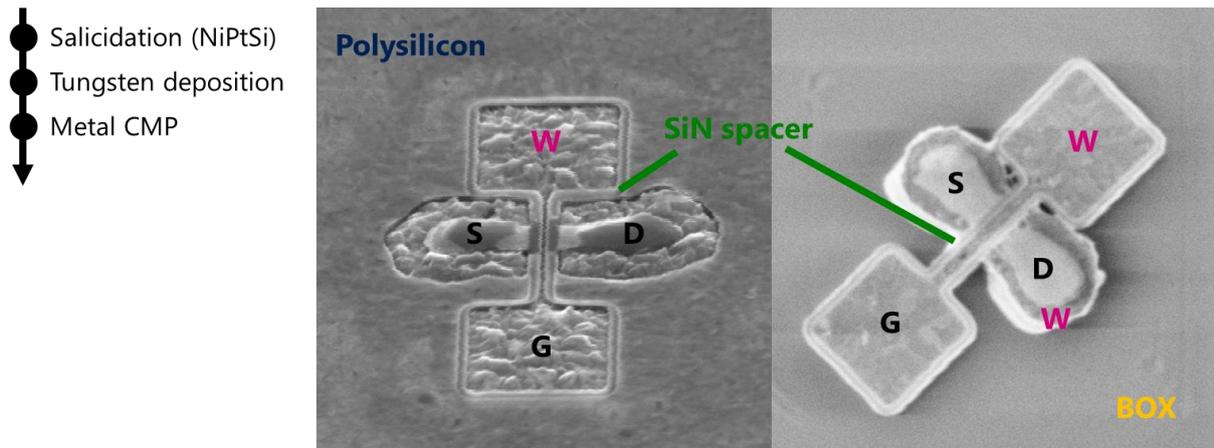


Figure 4.18 – Silicidation and tungsten contact filling in a self-aligned-like process.

Finally, SNWFETs were obtained with a NW first approach and with HSQ sacrificial gates. However, BEOL could not be performed at the time of writing these lines. Usually, millimetric sized copper pads are fabricated for linking the transistors metal interconnects with usual probing tools. Performing characterization when this step is not feasible or when targeting specific devices, the nanoprobeing technique can be used. Such method allows to approach nanometric electrical probes onto transistors with no back-end (or after digging an access into the metal interconnects). This technique guided under SEM imaging has been conducted on a few samples during this thesis as shown in Figure 4.19.

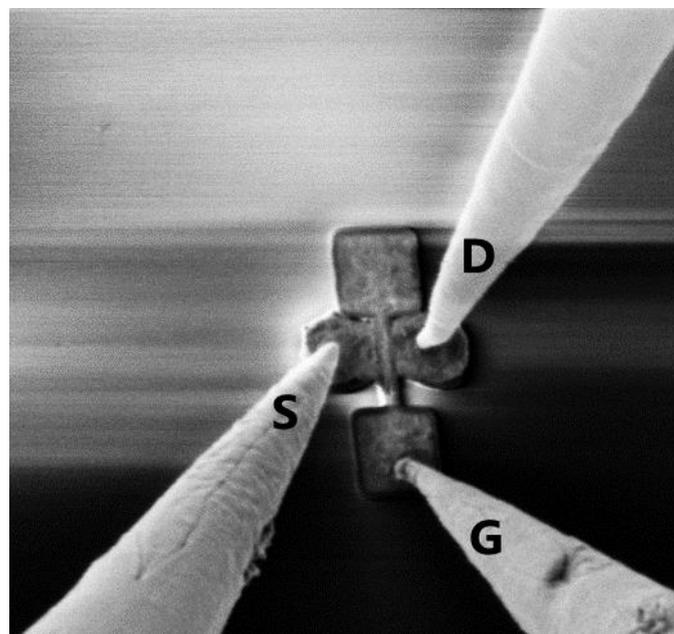


Figure 4.19 –Nanoprobeing of a SNWFET: device approach is realized under SEM imaging.

Unfortunately, the available devices at the time of the measurement were in short-circuit likely due to the BOX over etch observed previously (Figure 4.15). By realizing this integration on bulk substrates, this issue could be solved and functional devices could be fabricated following an identical process flow.

#### 4.2.2. Alternative approach with HSQ sacrificial gates and lateral insulation

HSQ has proved in the last part to be able to replace polysilicon sacrificial gates of typical gate last integration processes. In a NW first approach however, one downside is the loss in layout due to the lateral anchors required for suspending the NWs. The need of EUV for the lithography of HSQ or the a priori slower electron beam lithography raises also some question of the cost effectiveness of this approach. Therefore, several propositions and concepts are suggested in the following subchapter to provide further perspectives for HSQ and to balance with these concerns. Although no devices could be fabricated following these concepts, most of them have been submitted for patenting.

##### Lateral insulation and SAC

A similar process as the one described in (§3.1.2) and followed in (§4.2.1) is proposed in Figure 4.20. As shown in §1.3.3 and in §3.3, sidewall image transfer can be used to etch arrays of Si/SiGe fins as shown in Figure 4.20a-b. Following a NW first integration approach, the sacrificial SiGe is removed before the sacrificial gate patterning (Figure 4.20c). Anchors must be therefore included in the matrix to maintain the NWs suspended on both ends. The frequency of these anchors depends on NW thickness and Ge concentration in SiGe as pointed out in §3.4.

These suspended NWs are then immersed into a first HSQ resist layer whose thickness  $t_1$  depends on both spincoating speed and solvent viscosity. Ebeam through-silicon exposure is then performed as described in §3.6 to define the self-aligned sacrificial gates (Figure 4.20d). No conventional etching or stripping is needed since the exposed and developed material becomes an oxide used as a sacrificial gate. As shown in Figure 4.20d, several gates can be placed on the same silicon rod. This is a way to avoid separating physically the devices from one another. Consequently, this approach requires less lateral anchors.

Let's now use one of the HSQ property demonstrated in §3.6: HSQ is entirely selective to its developer (TMAH) once exposed. Therefore, a second layer of HSQ with a thickness  $t_2 < t_1$  can be spincoated, exposed and developed. A second population of HSQ features is obtained smaller than the first group of dummy gates (Figure 4.20e). This second population of HSQ structures features smaller sacrificial gates ( $t = t_2$ ) parallel to the first ones in addition of HSQ walls in between and parallel to the NW stacks (Figure 4.20e). These walls will serve as a lateral separation and isolation for the sources and drains of the adjacent devices. As shown in §3.6, the pitch of such features is of the order of magnitude of the NW stack array pitch realized by SIT (§3.3) and sub 40 nm device pitch can be expected.

At this point, the local insulation principle determined in §3.6 and Figure 3.55 could be used. By diverting the bridging effect observed during lithography and developing when two HSQ features are brought too closely, the device pitch could be further decreased while offering a complete insulation from the bulk.

The process described in §3.1.2 and demonstrated in §4.2.1 can be followed: the gate lateral spacers are patterned on the side of all HSQ features. The S/D are then fabricated following the process proposed in §3.5, before to implant and to encapsulate the devices into a SiN CESL and into polysilicon (Figure 4.20f).

The CMP of the polysilicon capping described in §3.7.3 is then performed and stopped selectively onto the highest HSQ oxide sacrificial gates. Subsequently, the second population of smaller HSQ features remain encapsulated under polysilicon. The HSQ in the as opened sacrificial gates is then etched away (Figure 4.20g) and replaced with the high-k metal gate stack. The extra metal is then polished away from the top of the polysilicon fill (Figure 4.20h, §3.7.4) prior to be itself removed by a hot TMAH solution (Figure 4.20i).

Eventually, SiN stoppers can be inserted to encapsulate the HKMG: this involves a metal etch-back and another CMP of SiN with a stop onto polysilicon as described in §3.7.4 for SAC module process flow.

Finally, salicidation is made within the S/D contact cavities which are therefore filled with tungsten. A last metal CMP is performed stopping onto the buried HSQ oxide features. SACs are then achieved through the separation by the SiN spacers and the HSQ features isolating the devices from one another (Figure 4.20j).

As shown in Figure 4.20k, some HSQ oxide may be left at the bottom of the gate cavity, under the suspended silicon NW channels, in order to suppress the bulk parasitic channel with this localized insulation.

State of the art MEOL and BEOL can now be applied to interconnect the devices and to finally build a complete chip.

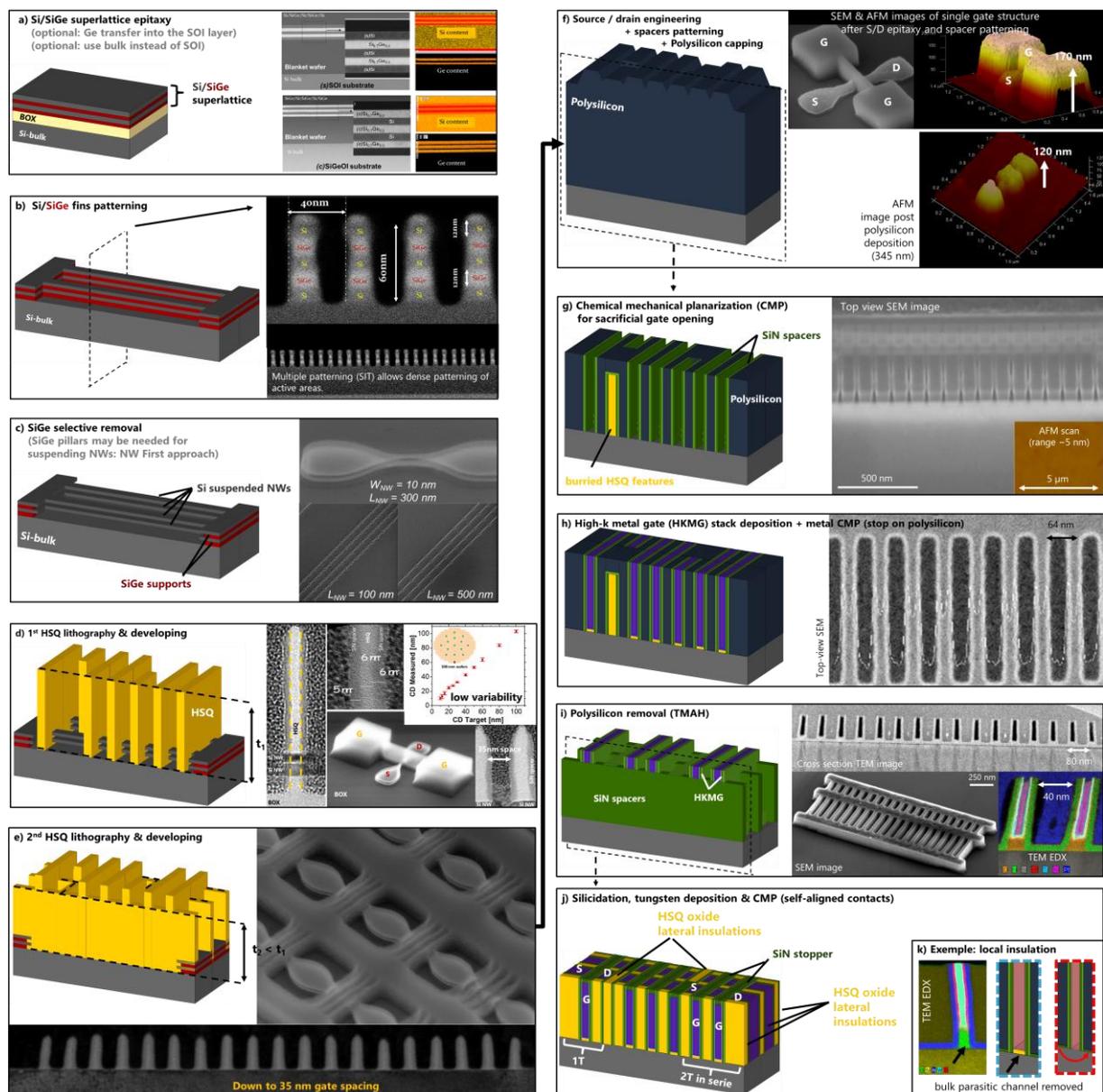


Figure 4.20 –Proposal for a HSQ based process flow for the fabrication of SNWFETs.

## Multi- $V_T$ approach

In the previous example, the second population of HSQ oxide sacrificial gates could also be replaced by an alternative HKMG stack with adjusted workfunction in order to realize a multi-threshold design ( $V_T$  flavoring). The polysilicon and HKMG CMPs can be cycled in order to reach several populations of buried HSQ features with different heights as shown in Figure 4.21. Subsequently, a third population of HSQ sacrificial features with a height  $t_3 < t_2 < t_1$  is preredquired to finally isolate the devices after the SAC CMP (Figure 4.21k).

As shown in Figure 4.21l, the last remaining HSQ can also be removed to access and to cut the NW extensions for suppressing any current leakage through this channel. Alternatively, a third gate stack can be deposited to maintain a near zero leakage current by shifting the  $V_T$ .

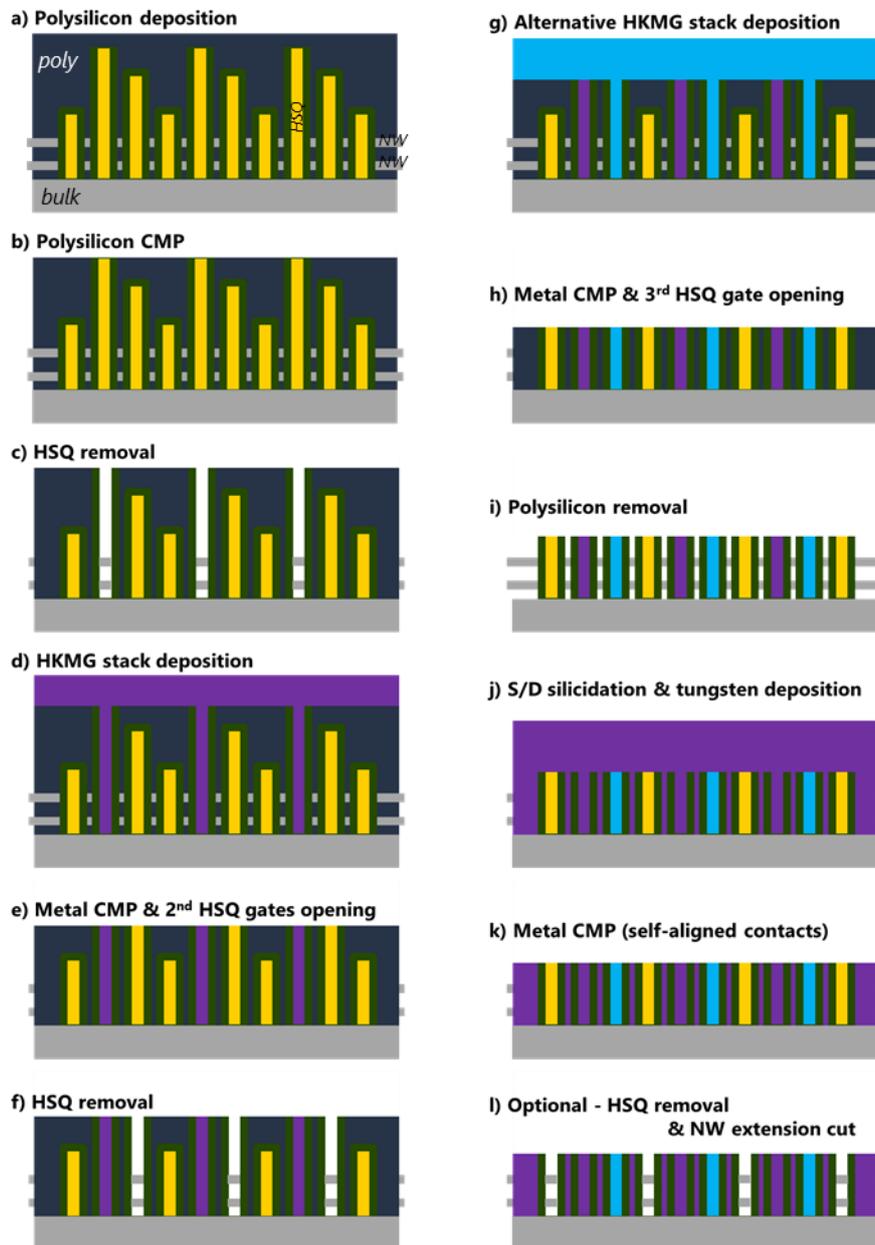


Figure 4.21 - Longitudinal cut along suspended NW channels: three different population of sacrificial HSQ gate heights are represented and used to fabricate transistors with two different gate stack and isolate the three groups of two transistors in series by leaving HSQ dummy gates (a-k). Options to remove any leakage current are either to remove the NW extensions or to place a third gate stack to shift the parasitic channels  $V_{th}$  once the last HSQ material is removed (j).

## Nearest contact bridging

Similarly, after the multi- $V_T$  option, the device lateral insulation is also tunable in a sort of “3D-STI” and “3D-SAC”. As show in Figure 4.21e, smaller HSQ lines parallel to the NW channels can be implemented. By tuning locally the height of these insulation features, the first connections stage in between the nearest devices can be achieved without requiring additional patterning step (Figure 4.22).

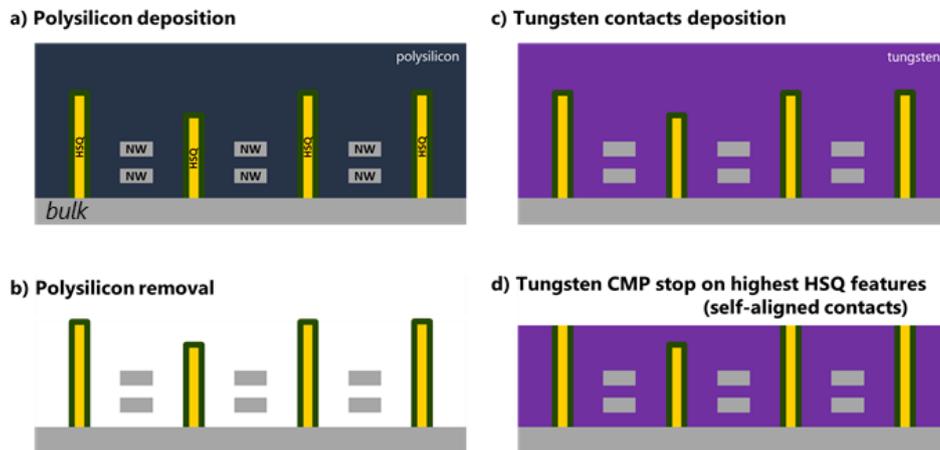


Figure 4.22 - Concept of 3D-STI and 3D-SAC: cross-sectional view into the source and drain regions (NW extensions). With two populations of insulator heights, 3D SAC allows to connect two neighboring devices and to isolate the others.

## 3D lithography concept

Although such approaches pave the way for building ultra-compact tri-dimensional devices, in the former descriptions the various populations of sacrificial feature heights are obtained through multiple lithography and developing cycle steps. When considering the use of EUV exposure tool, several lithography masks must be designed. Even if the number of masks is similar to what can be expected in a FinFET technology, this approach does not have the flexibility of an electron beam tool. By contrast, the electron beam lithography has a much lower throughput as each feature have to be written one by one. Following the approaches previously proposed, if several HSQ lithography steps are considered, processing time is tremendously increased and the alternative is not time and cost competitive.

The SEM cross section of Figure 4.23 reveal another property of HSQ oxide: the HF etch speed is highly dependent on crosslinking and exposure conditions. The images of Figure 4.23 were obtained after polysilicon CMP for HSQ sacrificial gate opening. On this wafer, identical exposure dose was applied to obtain all the HSQ patterns. A partial HF etch has been applied to measure HSQ etch speed and the results features a higher etch rate in narrower features. This can be attributed to the electron beam energy diffusion: the larger the structures, the more energy is absorbed and the denser is the oxide.

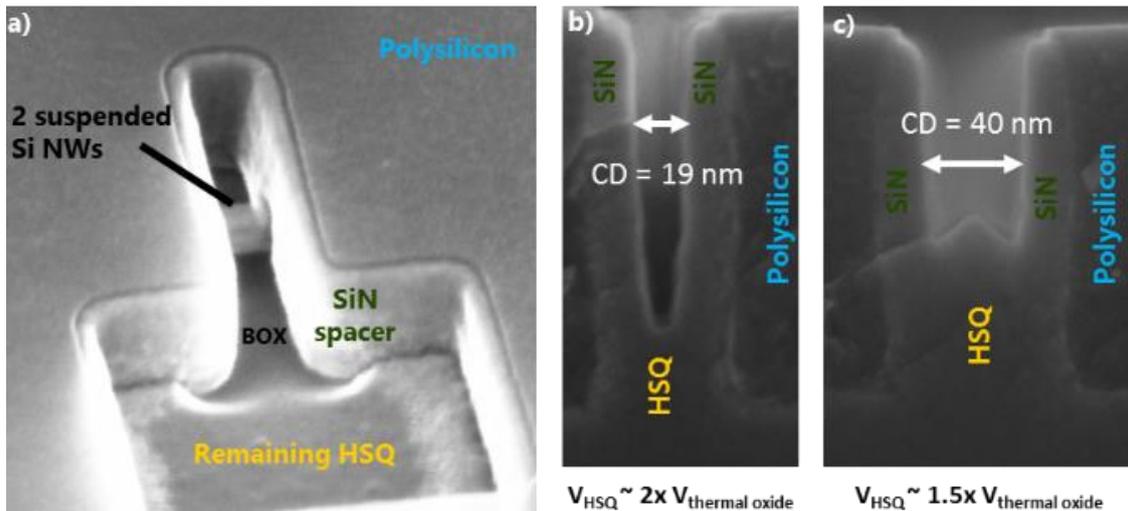


Figure 4.23 – (a) SEM image after HSQ sacrificial gate removal and (b) SEM cross-sections images during HSQ sacrificial gate removal showing the etch rate dependence on gate CD.

If several annealing techniques could be used to uniformize the curing of the HSQ features, this effect can be derived for building the tri-dimensional sacrificial HSQ structures previously presented. The latter results show the possibility to play on exposure dose to modify the HSQ density locally. Subsequently, for a unique spincoated layer of HSQ, the post-developing feature size and density of oxide can be tuned in a way that after a HF trimming, various heights can be obtained to reproduce the conditions of Figure 4.20 to Figure 4.22. Moreover, the aforementioned results of Figure 4.23 show that the difference of etch rate is maintained even after exposed HSQ has endured the whole FEOL thermal budget (including S/D epitaxy, SiN and polysilicon deposition steps). Consequently, if the selectivity is high enough a selected group of sacrificial gates could alternatively or complementarily be replaced by HKMG while the rest remains available for lateral insulation without performing the CMP cycles described in Figure 4.20 and Figure 4.21.

### Compatibility with NW last approach and FinFET technology

Finally, nothing intrinsically prevents to use HSQ and these concepts with FinFETs and SNWFETs with a NW last approach to replace polysilicon sacrificial gates. Additionally, using HSQ and “3D-STI” and “3D-SAC” concepts, the use of a specific mask to remove the Si or SiGe channel extensions would no longer be required for isolating the devices from one another.

### Conclusion

Subsequently, these observations suggest that a single exposure with precise control of the dose and an adapted design may be adequate to realize multi-level features including sacrificial gates, lateral device separation, SAC and several of the first interconnects. By skipping several patterning steps, these concepts could provide a definitive advantage of using multi electron beam lithography for innovative VLSI technology and sub 7 nm nodes platforms.

## General Conclusion

As of today, the question of FinFET and FDSOI downscaling is still open and SNWFET is a potential candidate for the next generation of CMOS. In the first chapter, the addition of one or several gates per channel is observed to improve electrostatic control over the channel. This became a requirement to counter the effect of decreasing the gate length in the most advanced technology nodes. After the double gates such as FinFET and FDSOI, the NW channels with three (trigate) or four (GAA) gates is likely the ultimate solution in terms of electrostatic optimization.

Although these properties were verified in the past, trigate NWFETs were fabricated in a gate first approach with different channel orientations and with raised source and drain. Measurements have shown that a compressive stress brings a significant improvement of hole mobility and performances. The observations of a large variety of channels size and orientation, has also shown that carrier transport in multigate FETs turns out to be deeply affected by quantum confinement and devices dimensions. Consequently, in addition of all the benefits in terms of electrostatic control, increased drive current and compactness, the complexity of performance prediction and of compact modeling is likely increased for NW architectures.

The NW channels with multiple gates folded around is another significant advantage of the NWFET technology. The high device effective width per unit footprint translates into a high drive current. To further improve device compactness and current density, an optimized sidewall image transfer patterning was developed for producing multi-finger devices. A slight BOX overetch during NW patterning was applied to obtain  $\Omega$ -gate NWFETs with a 35 nm channel pitch and excellent performances. However, ultimately the GAA configuration remains the optimal configuration.

Nevertheless, the NW channels must be ultimately stacked on top of each other for fully competing with FinFET technology in terms of effective width and current drivability. As a prelude to any cleanroom developments, a technology benchmarking has been performed in the second chapter. FinFET architecture is therefore the base for comparison with SNWFET. Using TCAD simulation, large and thin NW channels or nanosheets have been found to overcome FinFET performances when comparing devices with similar footprints and total heights in both technologies. Besides, the SNWFET or SNSFET technologies introduce more design flexibility since the NW width can be tuned to obtain either more current or lower footprint than its FinFET counterpart.

Since the benefits of SNWFETs was verified, the second part of this chapter has focused on one particularity of this technology. The source and drain-to-gate spacer is the low-k dielectric insulation ensuring a proper functioning of the MOSFET. When fabricating SNWFET in a gate last approach, the surface of the gate between the NWs may not be covered by such a material. Therefore, the electric insulation is only achieved by the high-k dielectric. The simulations performed on dual GAA SNWFETs have shown first a significant reduction of the gate-to-source and drain parasitic capacitances when internal spacers are introduced. Furthermore, the position of these internal spacers under the gate presents an optimum when considering process variability. Consequently, two process flows including aligned and self-aligned internal spacers have been suggested.

Even though SNWFETs were produced in the past, the fabrication flow must be adapted for state-of-the-art gate stacks and their limited acceptable thermal budget. Therefore, two gate last integrations derived from FinFET technology are suggested in the first part of the third chapter.

The so-called NW last approach relies on Si/SiGe fins instead of silicon fins. The sacrificial SiGe is only removed within the gate cavity after the sacrificial polysilicon gate is etched away. The internal spacers are obtained during the recessed and raised source and drain module, by carving cavities into the sacrificial SiGe aligned under the main gate spacer. Two steps of SiN conformal deposition and of anisotropic etch is then performed to place the SiN material into these cavities.

In the second process flow, the sacrificial SiGe is removed before the patterning of the sacrificial gate. Hence this approach is referred as NW first. Since the silicon NW channels are suspended, the use of an innovative sacrificial gate material is proposed to replace polysilicon: HSQ flowable oxide is spincoated and transformed into silicon dioxide features under an electron beam. No etching nor stripping are required by using this patterning technique as the resist material is turned into the final structure. Since silicon does not hinder such exposure source, the sacrificial gates are self-aligned through the channels. Once the SiN conformal deposition is performed, self-aligned internal spacers are therefore obtained.

These integrations rely on several key processes such as the heteroepitaxy of Si and SiGe materials, the patterning of the NW stacks, the selective etching of the sacrificial SiGe and the patterning of the sacrificial gates. Hence the second part of chapter 3 provides details about these processes developed specifically for SNWFET integration.

Si and SiGe heteroepitaxy of one above the other is permitted either for the fabrication of the superlattices leading to the Si/SiGe fins after patterning or for the Si or SiGe in-situ doped sources and drains. Moreover, strain mappings have shown that the stress of the under layers can be transferred to the upper layers throughout the superlattice. Subsequently, optimized channels under tensile or compressive stress can be expected when starting respectively from a strained SOI substrate or from SiGe on insulator substrates obtained by (localized) Ge condensation. Although the same mappings after Si/SiGe fin patterning have shown that the longitudinal strain is preserved, the risk of relaxation due to the free edges have also been pointed out.

The selective removal of SiGe leading to the suspended channels has been investigated through different wet and dry approaches. Even though the  $\text{CF}_4$  plasma and chlorine chemistries were good enough in the past, their intrinsic selectivities are no longer compatible with current NW dimensions. Indeed, as shown by TCAD simulations, the 6 to 8 nm thick channels must be fully preserved. Therefore, a  $\text{H}_2\text{O}_2/\text{HNO}_3$  wet chemistry has been successfully optimized to obtain up to 70 nm wide suspended nanosheets.

However, when considering suspended silicon channels, the question of mechanical robustness becomes crucial. An analytical model has been used to show that NW buckling is dominated by internal stress which is itself induced by the relaxation of the SiGe in the Si/SiGe lateral anchors maintaining the suspended NWs. Therefore, several trade-offs have been identified in between NW widths, thicknesses and anchor lengths and with Ge concentration and SiGe etch depth and selectivity.

Concerning the sources and drains, boron and phosphorus in-situ doped epitaxies were successfully performed after the anisotropic plasma etch for recessing the NW extensions. The epitaxy quality on a surface damaged and contaminated by the etching and by the reaction byproducts was improved by a Siconi surface preparation instead of usual HF last cleaning. A specific process has been developed to insert aligned internal spacers in a NW last approach for reducing the parasitic capacitances and for providing an etch stop layer when removing the sacrificial SiGe in between the suspended NWs. Additionally, significant compressive strain induced by SiGe source and drain has been measured.

Lithography of HSQ flowable oxide has been studied for patterning sacrificial gates in a NW first approach. Since EUV lithography was not available, an electron beam lithography has been calibrated to achieve self-aligned gates through two suspended Si NWs with gate lengths down to only 6 nm. In the provided conditions, minimum spacing in between HSQ features have been measured at 35 nm in sub-60nm pitch arrays.

The last part of this third chapter showed that the control and uniformity of FEOL CMPs are crucial. Layout and design integration co-optimization importance has been demonstrated with the polysilicon CMP. Since large areas of the test chips were not covered in dummies while some other large positive features were present, significant on-chip thickness variation was observed post planarization although the wafer uniformity and local planarization range was excellent. By using an additional lithography mask to etch away the highest features, the dishing of the lowest areas has been avoided. The selectivity in between silicon, oxide, silicon nitride and metal is also important in such gate last integrations. The gate opening CMP of the HDP oxide capping stopping onto the SiN hard mask on top of the polysilicon sacrificial gates have been successfully performed. In the case of a NW first approach, the selectivities have also been effectively reversed to planarize the polysilicon capping and to land into the HSQ oxide sacrificial gates. The last CMPs concerned the HKMG stack and the SACs. The latter case underlines the importance of nanometric precision in all the previous CMP. Indeed, the cumulated planarization range may result in a detrimental reduction of the gate height leaving not sufficient space for inserting a SiN stopper to protect and isolate the gate during the SAC module.

In the final chapter, this toolset of processes and knowledge was successfully assembled to achieve SNW PMOSFETs within a gate last and NW last approach. Electrical characterization presented excellent performances in accordance with the TCAD simulations, with the process conditions and with several previous references. The introduction of SiGe raised source and drain induced significant compressive stress also enhanced by the gate last integration model for promising improvement of hole transport in stacked NW technology.

The integration of SNWFETs based on a NW first approach and HSQ sacrificial gates was also conducted up to the SAC module. Although electrical characterizations using nanoprobeing were not conclusive and although the BEOL could not be performed on time, the proof of concept and the accumulated learning allows to draw stimulating perspectives for this technology. Based on the observation that transformed HSQ is entirely selective to its developer (TMAH), several HSQ feature heights can be obtained by multiple spincoating, exposure and developing cycles. Such oxide structures can be turned into sacrificial gates and lateral isolation for separating the adjacent devices and perform a "3D-SAC". Furthermore, by adding one or several cycles of CMP, multi- $V_T$  and nearest transistor contact bridging concepts could be suggested. Although these concepts are promising for further shrinks of SRAMs and other standard cells, the question of low throughput of electron beam lithography and therefore of its cost effectiveness arises. Even if HSQ could also be exposed with an EUV equipment, this material presents another interesting property: its etch rate under HF varies according to the exposure dose. Subsequently, by using multi-electron beam lithography and adjusting the exposure doses the 3D-lithography previously described could be achieved in one single and mask-less lithography step. Therefore, the design flexibility, the decreased number masks and of patterning steps could make this alternative competitive as compared to the polysilicon sacrificial gate. Besides, HSQ is also compatible with SNWFET fabrication within a NW last approach and FinFET integrations.

In the light of this work, the SNWFET technology is foreseen as an evolution of FinFET. Indeed, in following the NW last approach, very few process steps are introduced in comparison with recent gate last integrations of FinFETs. Besides, both simulations and device measurements gives promising perspectives in outperforming FinFETs. Furthermore, observations on trigate NWFETs and SNWFETs have shown NW channels to benefit from carrier transport strain enhancement techniques by means of strain report in the superlattice and by the raised SiGe source and drain. Opting for large and thin stacked nanosheets provide an additional advantage over FinFET technology in terms of device effective width per footprint unit. While FinFET is intrinsically limited by fin patterning and consequently a quantified device footprint, TCAD has shown that NW width can be tuned to advantage device compactness and performances. This is sustained by advanced process engineering by providing highly selective sacrificial SiGe removal.

However, electrical measurement and TCAD have also confirmed that the bottom NW is limiting the overall device performances. Even though an  $\Omega$ -gate can slightly improve the electrostatic control of this bottom NW, enlargement of NW width will still be limited for optimizing the immunity to short channel effects. From this statement two options remain: either the integration must focus on GAA square cross-section NWs or the devices must be integrated on bulk substrates. In the latter, the bottom channel must be “killed” by using proper doping to shift the threshold voltage of the parasitic channel.

The question of NW buckling is essential for both NW last and NW first approaches as the process repeatability and stability relies on the robustness of the integration, and hence, in the present case, on mechanical resistance of the suspended NWs. NW last is less impacted by such issue due to shorter NW length corresponding only to the gate length inside the gate cavity. State-of-the-art characterization tools such as 3D-CD SEMs are intended to provide a metrology for such concerns but were not operational during the realization of this thesis work.

Finally, the SNWFET technology as derived from FinFET appears close to a possible industrialization. Besides, further advanced simulations and device characterizations can still provide a better understanding of the transport properties in such confined channels. Subsequently, further optimizations can be expected for several node generations of SNWFETs.



# BIBLIOGRAPHIE

- Abbadie, A., J. M. Hartmann, P. Holliger, M. N. Séméria, P. Besson, and P. Gentile2004 Low thermal budget surface preparation of Si and SiGe, *Applied Surface Science*, 225 (1–4) (March), 256–266. doi:10.1016/j.apsusc.2003.10.018.
- Ben Akkez, I., C. Fenouillet-Beranger, A. Cros, P. Perreau, S. Haendler, O. Weber, F. Andrieu, et al.2012 Impact of substrate orientation on Ultra Thin BOX Fully Depleted SOI electrical performances, *2012 13th International Conference on Ultimate Integration on Silicon (ULIS)*, IEEE, March, 177–180. doi:10.1109/ULIS.2012.6193386.
- Allibert, F., A. Zaslavsky, J. Pretet, and S. Cristoloveanu2001 Double-Gate MOSFETs: Is Gate Alignment Mandatory?, *31st European Solid-State Device Research Conference*, IEEE, 1,267–270. doi:10.1109/ESSDERC.2001.195252.
- Ancona, M. G., and G. J. Iafrate1989 Quantum correction to the equation of state of an electron gas in a semiconductor, *Physical Review B*, 39 (13) (May 1), 9536–9540. doi:10.1103/PhysRevB.39.9536.
- Andrieu, F., O. Faynot, F. Rochette, J.-C. Barbe, C. Buj, Y. Bogumilowicz, F. Allain, et al.2007 Impact of Mobility Boosters (XsSOI, CESL, TiN gate) on the Performance of  $100\text{nm}$  or  $110\text{nm}$  oriented FDSOI cMOSFETs for the 32nm Node, *2007 IEEE Symposium on VLSI Technology*, IEEE, June, 50–51. doi:10.1109/VLSIT.2007.4339723.
- Andrieu, F., O. Weber, S. Baudot, C. Fenouillet-Beranger, O. Rozeau, J. Mazurier, P. Perreau, J. Eymery, and O. Faynot2010 Fully depleted Silicon-On-Insulator with back bias and strain for low power and high performance applications, *2010 IEEE International Conference on Integrated Circuit Design and Technology*, IEEE, June, 59–62. doi:10.1109/ICICDT.2010.5510295.
- Anon.2013 Sentaurus
- Arnaud, F., N. Planes, O. Weber, V. Barral, S. Haendler, P. Flatresse, and F. Nyer2012 Switching energy efficiency optimization for advanced CPU thanks to UTBB technology, *Technical Digest - International Electron Devices Meeting, IEDM*, 48–51. doi:10.1109/IEDM.2012.6478970.
- Auth, C., C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, et al.2012 A 22nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors , Self-Aligned Contacts and High Density MIM Capacitors IDSAT (  $A / \mu\text{m}$  ) VGS (  $V$  ) m (2003), 131–132
- Auth, C. P., and J. D. Plummer1997 Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's, *IEEE Electron Device Letters*, 18 (2) (February), 74–76. doi:10.1109/55.553049.
- Avci, U. E., D. H. Morris, and I. A. Young2015 Tunnel Field-Effect Transistors: Prospects and Challenges, *IEEE Journal of the Electron Devices Society*, 3 (3) (May), 88–95. doi:10.1109/JEDS.2015.2390591.
- Baccarani, G., M. R. Wordeman, and R. H. Dennard1984 Generalized scaling theory and its application to a  $1.8\mu\text{m}$  micrometer MOSFET design, *IEEE Transactions on Electron Devices*, 31 (4) (April), 452–462. doi:10.1109/T-ED.1984.21550.
- Baie, X., and J. P. Colinge1998 Two-dimensional confinement effects in gate-all-around (GAA) MOSFETs, *Solid-State Electronics*, 42 (4) (April), 499–504. doi:10.1016/S0038-1101(98)00061-6.
- Balan, V.2016 CMP – Stack Trek, *SSDM*,
- Balestra, F., J. Brini, and P. Gentil1985 Deep depleted SOI MOSFETs with back potential control: A numerical simulation, *Solid-State Electronics*, 28 (10) (October), 1031–1037. doi:10.1016/0038-1101(85)90035-8.

- Balestra, F., S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa 1987 Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance, *IEEE Electron Device Letters*, 8 (9) (September), 410–412. doi:10.1109/EDL.1987.26677.
- Balestra, F., G. Ghibaudo, and J. Jomaah 2015 Modeling of low-frequency noise in advanced CMOS devices, *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, 28 (6) (November), 613–627. doi:10.1002/jnm.2052.
- Bangsaruntip, S., K. Balakrishnan, S. L. Cheng, J. Chang, M. Brink, I. Lauer, R. L. Bruce, et al. 2013 Density scaling with gate-all-around silicon nanowire MOSFETs for the 10 nm node and beyond, *Technical Digest - International Electron Devices Meeting, IEDM*, 526–529. doi:10.1109/IEDM.2013.6724667.
- Bangsaruntip, S., G. M. Cohen, A. Majumdar, and J. W. Sleight 2010 Universality of Short-Channel Effects in Undoped-Body Silicon Nanowire MOSFETs, *IEEE Electron Device Letters*, 31 (9) (September), 903–905. doi:10.1109/LED.2010.2052231.
- Bangsaruntip, S., G. M. Cohen, A. Majumdar, Y. Zhang, S. U. Engelmann, N. C. M. Fuller, L. M. Gignac, et al. 2009 High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling, *2009 IEEE International Electron Devices Meeting (IEDM)*, IEEE, December, 1–4. doi:10.1109/IEDM.2009.5424364.
- Barnola, S., P. Pimenta Barros, C. Arvet, C. Vizioz, N. Posseme, A. Gharbi, M. Argoud, et al. 2014 Plasma etching and integration challenges using alternative patterning techniques for 11nm node and beyond, in G. S. Oehrlein, Q. Lin, and Y. Zhang (eds.), *Proc. of SPIE*, March 28, 9054,90540E. doi:10.1117/12.2046251.
- Barnola, S., C. Vizioz, N. Vulliet, C. Dupré, T. Ernst, P. Gautier, C. Arvet, et al. 2008 Dry Etch Challenges in Gate All Around Devices for sub 32 nm Applications, *ECS Transactions*, ECS, 16,923–934. doi:10.1149/1.2986854.
- Barraud, S., R. Coquand, M. Casse, M. Koyama, J. M. Hartmann, V. Maffini-Alvaro, C. Comboroure, et al. 2012 Performance of omega-shaped-gate silicon nanowire MOSFET with diameter down to 8 nm, *IEEE Electron Device Letters*, 33 (11), 1526–1528. doi:10.1109/LED.2012.2212691.
- Barraud, S., R. Coquand, V. Maffini-Alvaro, M.-P. Samson, J.-M. Hartmann, L. Tosti, M. Cassé, et al. 2013 Scaling of  $\Omega$ -Gate SOI Nanowire N- and P-FET down to 10nm Gate Length: Size- and Orientation-Dependent Strain Effects, *2013 Symposium on VLSI Circuits (VLSI)*, 230–231
- Barraud, S., V. Lapras, M. P. Samson, L. Gaben, L. Grenouillet, Y. Morand, and J. Daranlot 2016 Vertically Stacked-NanoWires MOSFETs in a Replacement Metal Gate Process with Inner Spacer and SiGe Source / Drain, *IEDM*, 1–4
- Barraud, S., R. Lavieville, C. Tabone, F. Allain, M. Casse, M.-P. Samson, V. Maffini-Alvarro, and M. Vinet 2014 Strained Silicon Directly on Insulator N- and P-FET nanowire transistors, *2014 15th International Conference on Ultimate Integration on Silicon (ULIS)*, IEEE, April, 65–68. doi:10.1109/ULIS.2014.6813907.
- Basker, V. S., T. Standaert, H. Kawasaki, C.-C. Yeh, K. Maitra, T. Yamashita, J. Faltermeier, et al. 2010 A 0.063  $\mu\text{m}^2$  FinFET SRAM cell demonstration with conventional lithography using a novel integration scheme with aggressively scaled fin and gate pitch, *2010 Symposium on VLSI Technology*, IEEE, June, 50,19–20. doi:10.1109/VLSIT.2010.5556135.
- Baudot, S., F. Andrieu, O. Weber, P. Perreau, J.-F. Damlencourt, S. Barnola, T. Salvétat, et al. 2010 Fully Depleted Strained Silicon-on-Insulator p-MOSFETs With Recessed and Embedded Silicon&#x2013;Germanium Source/Drain, *IEEE Electron Device Letters*, 31 (10) (October), 1074–1076. doi:10.1109/LED.2010.2057500.
- Bauer, M. 2006 SEPARATE INJECTION OF REACTIVE SPECIES IN SELECTIVE FORMATION OF FILMS
- Bauer, M., V. Machkaoutsan, and C. Arena 2007 Highly tensile strained silicon–carbon alloys epitaxially grown into recessed source drain areas of NMOS devices, *Semiconductor Science and Technology*, 22 (1) (January 1), S183–S187. doi:10.1088/0268-1242/22/1/S43.

- Bernard, E., T. Ernst, B. Guillaumot, N. Vulliet, V. Barral, V. Maffini-Alvaro, F. Andrieu, et al.2008 Novel integration process and performances analysis of Low STandby Power (LSTP) 3D multi-channel CMOSFET (MCFET) on SOI with metal / high-K gate stack, *2008 Symposium on VLSI Technology*, IEEE, June, 5,16–17. doi:10.1109/VLSIT.2008.4588546.
- Bernard, E., T. Ernst, B. Guillaumot, N. Vulliet, X. Garros, V. Maffini-Alvaro, P. Coronel, T. Skotnicki, and S. Deleonibus2008 Impact of the gate stack on the electrical performances of 3D multi-channel MOSFET (MCFET) on SOI, *Solid-State Electronics*, 52 (9), 1297–1302. doi:10.1016/j.sse.2008.04.014.
- Bernard, E., T. Ernst, B. Guillaumot, N. Vulliet, T. C. Lim, O. Rozeau, F. Danneville, et al.2009 First internal spacers' introduction in record high ION /IOFFTiN/HfO2 gate multichannel MOSFET satisfying both high-performance and low standby power requirements, *IEEE Electron Device Letters*, 30 (2), 148–151. doi:10.1109/LED.2008.2009008.
- Berthelon, R., F. Andrieu, B. Mathieu, D. Dutartre, C. Le Royer, M. Vinet, and A. Claverie2017 Mechanical simulations of BOX creep for strained FDSOI, *2017 Joint International EUROSIOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSIOI-ULIS)*, IEEE, April, 91–94. doi:10.1109/ULIS.2017.7962609.
- Bidal, G., F. Boeuf, S. Denorme, N. Loubet, C. Laviron, F. Leverd, S. Barnola, et al.2008 Planar Bulk+ technology using TiN/Hf-based gate stack for low power applications, *2008 Symposium on VLSI Technology*, IEEE, June, 33,146–147. doi:10.1109/VLSIT.2008.4588596.
- Boeuf, F., G. Hiblot, G. Ghibaudo, and Q. Rafhay2014 Analytical relationship between subthreshold swing of thermionic and tunnelling currents, *Electronics Letters*, 50 (23), 1745–1747. doi:10.1049/el.2014.3206.
- Bonnevialle, A., C. Le Royer, Y. Morand, S. Reboh, C. Plantier, N. Rambal, J. Pédini, et al.2016 Smart Solutions for Efficient Dual Strain Integration for Future FDSOI Generations, *Vlsi 2016*, 392 (2014), 132–133
- BOREL, S.2004 Isotropic etching of SiGe alloys with high selectivity to similar materials, *Microelectronic Engineering*, 73–74 (June), 301–305. doi:10.1016/j.mee.2004.02.057.
- Brews, J. R., W. Fichtner, E. H. Nicollian, and S. M. Sze1980 Generalized guide for MOSFET miniaturization, *IEEE Electron Device Letters*, 1 (1) (January), 2–4. doi:10.1109/EDL.1980.25205.
- Bruel, M., B. Aspar, B. Charlet, C. Maleville, T. Poumeyrol, A. Soubie, A. J. Auberton-Herve, et al.1995 'Smart cut': a promising new SOI material technology, *1995 IEEE International SOI Conference Proceedings*, IEEE, 178–179. doi:10.1109/SOI.1995.526518.
- Bruel, M., J. Margail, J. Stoemenos, P. Martin, and C. Jaussaud1985 Formation of buried insulating layers by high dose oxygen implantation under controlled temperature conditions, *Vacuum*, 35 (12) (December), 589–593. doi:10.1016/0042-207X(85)90321-5.
- Brunet, L., P. Batude, C. Fenouillet-Beranger, P. Besombes, L. Hortemel, F. Ponthenier, B. Previtali, et al.2016 First demonstration of a CMOS over CMOS 3D VLSI CoolCube™ integration on 300mm wafers, *2016 IEEE Symposium on VLSI Technology*, IEEE, June, 1–2. doi:10.1109/VLSIT.2016.7573428.
- Burr, G. W., R. M. Shelby, A. Sebastian, S. Kim, S. Kim, S. Sidler, K. Virwani, et al.2017 Neuromorphic computing using non-volatile memory, *Advances in Physics: X*, 2 (1), 89–124. doi:10.1080/23746149.2016.1259585.
- Cams, T. K.1995 Chemical Etching of Si[<sub>1-x</sub>]Ge[<sub>x</sub>] in HF:H[<sub>2</sub>]O[<sub>2</sub>]:CH[<sub>3</sub>]COOH, *Journal of The Electrochemical Society*, 142 (4), 1260. doi:10.1149/1.2044161.
- Cerutti, R., P. Coronel, and S. Harrison2005 Metal gate-all-around CMOS integration using poly-gate replacement through contact hole (PRETCH), *Integrated Circuit ...*, 203–206
- Chanemougame, D.2005 Conception et fabrication de nouvelles architectures CMOS et étude du transport dans les canaux de conduction ultra minces obtenus avec la technologie SON, 38926–38926

Chang-Woo Oh, Sung-Ho Kim, Chang-Sub Lee, Jeong-Dong Choe, Shin-Ae Lee, Sung-Young Lee, Kyung-Hwan Yeo, et al.2003 Highly manufacturable sub-50 nm high performance CMOSFET using real damascene gate process, *2003 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.03CH37407)*, Japan Soc. Applied Phys, 147–148. doi:10.1109/VLSIT.2003.1221128.

Chang, J. B., M. Guillorn, P. M. Solomon, C.-H. Lin, S. U. Engelmann, a. Pyzyna, J. a. Ott, and W. . Haensch2011 Scaling of SOI FinFETs down to fin width of 4 nm for the 10nm technology node, *2011 Symposium on VLSI Technology - Digest of Technical Papers*, 12–13

Chen, J., T. Saraya, and T. Hiramoto2010 Mobility enhancement over universal mobility in (100) silicon nanowire gate-all-around MOSFETs with width and height of less than 10nm range, *Digest of Technical Papers - Symposium on VLSI Technology*, (100), 175–176. doi:10.1109/VLSIT.2010.5556217.

Chen, J., T. Saraya, K. Miyaji, K. Shimizu, and T. Hiramoto2008 Experimental study of mobility in [110]- and [100]-directed multiple silicon nanowire GAA MOSFETs on (100) SOI, *Digest of Technical Papers - Symposium on VLSI Technology*, (100), 32–33. doi:10.1109/VLSIT.2008.4588552.

Cheng, K., A. Khakifirooz, N. Loubet, S. Luning, T. Nagumo, M. Vinet, Q. Liu, et al.2012 High performance extremely thin SOI (ETSOI) hybrid CMOS with Si channel NFET and strained SiGe channel PFET, *2012 International Electron Devices Meeting*, IEEE, December, 18.1.1-18.1.4. doi:10.1109/IEDM.2012.6479063.

Chi-Chun Chen, V. S. Chang, Y. Jin, C.-H. Chen, T.-L. Lee, S.-C. Chen, and M.-S. Liang2004 Extended scaling of ultrathin gate oxynitride toward sub-65nm CMOS by optimization of UV photo-oxidation, soft plasma/thermal nitridation & stress enhancement, *Digest of Technical Papers. 2004 Symposium on VLSI Technology, 2004.*, IEEE, 176–177. doi:10.1109/VLSIT.2004.1345464.

Chih-Chieh Yeh, Chih-Sheng Chang, Hong-Nien Lin, Wei-Hsiung Tseng, Li-Shyue Lai, Tsu-Hsiu Perng, Tsung-Lin Lee, et al.2010 A low operating power FinFET transistor module featuring scaled gate stack and strain engineering for 32/28nm SoC technology, *2010 International Electron Devices Meeting*, IEEE, December, 34.1.1-34.1.4. doi:10.1109/IEDM.2010.5703473.

Cho, H.-J., H. S. Oh, K. J. Nam, Y. H. Kim, K. H. Yeo, W. D. Kim, Y. S. Chung, et al.2016 Si FinFET based 10nm technology with multi Vt gate stack for low power and high performance applications, *2016 IEEE Symposium on VLSI Technology*, IEEE, June, 1–2. doi:10.1109/VLSIT.2016.7573359.

Choi, Y.-K., T.-J. King, and C. Hu2002 Spacer FinFET: nanoscale double-gate CMOS technology for the terabit era, *Solid-State Electronics*, 46 (10) (October), 1595–1601. doi:10.1016/S0038-1101(02)00111-9.

Chunshan Yin, P. C. H. Chan, and V. W. C. Chan2003 Fabrication of raised S/D gate-all-around transistor and gate misalignment analysis, *IEEE Electron Device Letters*, 24 (10) (October), 658–660. doi:10.1109/LED.2003.817367.

Colinge, J.-P.1986 Subthreshold slope of thin-film SOI MOSFET's, *IEEE Electron Device Letters*, 7 (4) (April), 244–246. doi:10.1109/EDL.1986.26359.

1987 Some properties of thin-film SOI MOSFETs, *IEEE Circuits and Devices Magazine*, 3 (6) (November), 16–20. doi:10.1109/MCD.1987.6323175.

1988 Reduction of kink effect in thin-film SOI MOSFETs, *IEEE Electron Device Letters*, 9 (2) (February), 97–99. doi:10.1109/55.2052.

1989 Thin-film SOI technology: the solution to many submicron CMOS problems, *International Technical Digest on Electron Devices Meeting*, IEEE, 817–820. doi:10.1109/IEDM.1989.74178.

Colinge, J. P., and A. Chandrakasan2008 *FinFETs and Other Multi-Gate Transistors*,. Ed. J.-P. Colinge, *FinFETs and Other Multi-Gate Transistors*, Boston, MA: Springer US. doi:10.1007/978-0-387-71752-4.

Colinge, J. P., M. H. Gao, A. Romano-Rodriguez, H. Maes, and C. Claeys1990 Silicon-on-insulator 'gate-all-around device', *International Technical Digest on Electron Devices*, IEEE, 595–598. doi:10.1109/IEDM.1990.237128.

Coquand, R.2013 Démonstration de l'intérêt des alignées pour les nœuds sub-10nm Plan de l'exposé

Coquand, R., S. Barraud, M. Casse, P. Leroux, C. Vizioz, C. Comboroure, P. Perreau, et al.2012 Scaling of high-k/metal-gate Trigate SOI nanowire transistors down to 10nm width, *2012 13th International Conference on Ultimate Integration on Silicon (ULIS)*, IEEE, March, 1,37–40. doi:10.1109/ULIS.2012.6193351.

Coquand, R., S. Barraud, M. Cassé, P. Leroux, C. Vizioz, C. Comboroure, P. Perreau, et al.2013 Scaling of high-κ/metal-gate TriGate SOI nanowire transistors down to 10nm width, *Solid-State Electronics*, 88 (100) (October), 32–36. doi:10.1016/j.sse.2013.04.006.

Coquand, R., M. Casse, S. Barraud, P. Leroux, D. Cooper, C. Vizioz, C. Comboroure, et al.2012 Strain-induced performance enhancement of tri-gate and omega-gate nanowire FETs scaled down to 10nm Width, *2012 Symposium on VLSI Technology (VLSIT)*, IEEE, June, 60,13–14. doi:10.1109/VLSIT.2012.6242437.

Coquand, R., and S. Monfray2013 Innovative through-Si 3D lithography for ultimate self-aligned planar Double-Gate and Gate-All-Around nanowire transistors, ... *2013 Symposium on*, 226–227

Coquand, R., S. Monfray, J. Pradelles, L. Martin, M.-P. Samson, J. Bustos, S. Barraud, et al.2013 On the Optimization of Ebeam Lithography Using Hydrogen Silsesquioxane (HSQ) for Innovative Self-Aligned CMOS Process, *ECS Transactions*, 53 (3) (May 3), 177–184. doi:10.1149/05303.0177ecst.

Coronel, P., S. Harrison, R. Cerutti, S. Monfray, and S. Skotnicki2004 Highly performant double gate MOSFET realized with SON process: how we address the design and process for the GAA SON challenges ?, *2004 International Conference on Integrated Circuit Design and Technology (IEEE Cat. No.04EX866)*, IEEE, 81–89. doi:10.1109/ICICDT.2004.1309913.

Cristoloveanu, S., and D. E. Ioannou1990 Adjustable confinement of the electron gas in dual-gate silicon-on-insulator mosfet's, *Superlattices and Microstructures*, 8 (1) (January), 131–135. doi:10.1016/0749-6036(90)90290-N.

Czornomaz, L., V. Djara, V. Deshpande, E. O'Connor, M. Sousa, D. Caimi, K. Cheng, and J. Fompeyrine2016 First demonstration of InGaAs/SiGe CMOS inverters and dense SRAM arrays on Si using selective epitaxy and standard FEOL processes, *2016 IEEE Symposium on VLSI Technology*, IEEE, June, 2016–Septe,1–2. doi:10.1109/VLSIT.2016.7573391.

van Dal, M. J. H., N. Collaert, G. Doornbos, G. Vellianitis, G. Curatola, B. J. Pawlak, R. Duffy, et al.2007 Highly manufacturable FinFETs with sub-10nm fin width and high aspect ratio fabricated with immersion lithography, *2007 IEEE Symposium on VLSI Technology*, IEEE, June, 80,110–111. doi:10.1109/VLSIT.2007.4339747.

Davis, G. E., L. R. Hite, T. G. W. Blake, C. Chen, H. W. Lam, and R. DeMoyer1985 Transient Radiation Effects in SOI Memories, *Transaction on Nuclear Science*, 4431–4437. doi:10.1109/TNS.1985.4334137.

Dennard, R. H., F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc1974 Design of ion-implanted MOSFET's with very small physical dimensions, *IEEE Journal of Solid-State Circuits*, 9 (5) (October), 256–268. doi:10.1109/JSSC.1974.1050511.

Denton, J. P., and G. W. Neudeck1996 Fully depleted dual-gated thin-film SOI P-MOSFETs fabricated in SOI islands with an isolated buried polysilicon backgate, *IEEE Electron Device Letters*, 17 (11) (November), 509–511. doi:10.1109/55.541764.

Destefanis, V., J.-M. Hartmann, F. Hüe, and D. Bensahel2008 HCl Selective Etching of Si<sub>1-x</sub>Ge<sub>x</sub> versus Si for Silicon On Nothing and Multi Gate Devices, *ECS Transactions*, ECS, 16,427–438. doi:10.1149/1.2986800.

Destefanis, V., J. M. Hartmann, M. Hopstaken, V. Delaye, and D. Bensahel2008 Low-thermal surface preparation, HCl etch and Si/SiGe selective epitaxy on (1 1 0) silicon surfaces, *Semiconductor Science and Technology*, 23 (10) (October 1), 105018. doi:10.1088/0268-1242/23/10/105018.

Dornel, E., T. Ernst, J. C. Barbé, J. M. Hartmann, V. Delaye, F. Aussenac, C. Vizioz, et al.2007 Hydrogen annealing of

arrays of planar and vertically stacked Si nanowires, *Applied Physics Letters*, 91 (23), 233502. doi:10.1063/1.2818678.

Doyle, B., B. Boyanov, S. Datta, M. Doczy, S. Harelund, B. Jin, J. Kavalieros, T. Linton, R. Rios, and R. Chau2003 Tri-Gate fully-depleted CMOS transistors: fabrication, design and layout, *2003 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.03CH37407)*, Japan Soc. Applied Phys, 49,133–134. doi:10.1109/VLSIT.2003.1221121.

Dupre, C., T. Ernst, E. Bernard, B. Guillaumot, N. Vulliet, P. Coronel, T. Skotnicki, S. Cristoloveanu, G. Ghibaudo, and S. Deleonibus2008 A mobility extraction method for 3D multichannel devices, *ESSDERC 2008 - 38th European Solid-State Device Research Conference*, 230–233. doi:10.1109/ESSDERC.2008.4681740.

Dupre, C., A. Hubert, S. Becu, M. Jublot, V. Maffini-Alvaro, C. Vizios, F. Aussenac, et al.2008 15nm-diameter 3D stacked nanowires with independent gates operation: &#x03A6;FET, *2008 IEEE International Electron Devices Meeting*, IEEE, December, 35,1–4. doi:10.1109/IEDM.2008.4796805.

Dysard, J. M., V. Brusica, P. Feeney, S. Grumbine, K. Moeggenborg, G. Whitener, W. Ward, G. Burns, and K. Choi2010 CMP Solutions for the Integration of High-K Metal Gate Technologies, *ECS Transactions*, 33,77–89. doi:10.1149/1.3489048.

Ernst, T., F. Andrieu, and O. Weber2006 High Mobility Nano-Scaled CMOS: Some Opportunities and Challenges, *SiGe Technology and Device Meeting, 2006. ISTDM 2006. Third International*, 17–18

Ernst, T., E. Bernard, C. Dupre, A. Hubert, S. Becu, B. Guillaumot, O. Rozeau, et al.2008 3D Multichannels and stacked nanowires technologies for new design opportunities in nanoelectronics, *2008 IEEE International Conference on Integrated Circuit Design and Technology, Proceedings*, 265–268. doi:10.1109/Icicdt.2008.4567292.

Ernst, T., C. Dupre, C. Isheden, E. Bernard, R. Ritzenthaler, V. Maffini-Alvaro, J.-C. Barbe, et al.2006 Novel 3D integration process for highly scalable Nano-Beam stacked-channels GAA (NBG) FinFETs with HfO<sub>2</sub>/TiN gate stack, *2006 International Electron Devices Meeting*, IEEE, 1–4. doi:10.1109/IEDM.2006.346955.

Ernst, T., L. Duraffourg, C. Dupre, E. Bernard, P. Andreucci, S. Becu, E. Ollier, et al.2008 Novel Si-based nanowire devices: Will they serve ultimate MOSFETs scaling or ultimate hybrid integration?, *2008 IEEE International Electron Devices Meeting*, IEEE, December, 1–4. doi:10.1109/IEDM.2008.4796804.

Eun-Jung Yoon, Sung-Young Lee, Sung-Min Kim, Min-Sang Kim, Sung Hwan Kim, Li Ming, Sungdae Suk, et al.2004 Sub 30 nm multi-bridge-channel MOSFET(MBCFET) with metal gate electrode for ultra high performance application, *IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004.*, IEEE, 627–630. doi:10.1109/IEDM.2004.1419244.

Fang, W., and J. a Wickert1999 Post buckling of micromachined beams, *Journal of Micromechanics and Microengineering*, 4, 116–122. doi:10.1088/0960-1317/4/3/004.

Fenouillet-Beranger, C., P. Perreau, S. Denorme, L. Tosti, F. Andrieu, O. Weber, and C. Arvet2009 Impact of a 10nm Ultra-Thin BOX (UTBOX) and Ground Plane on FDSOI devices for 32nm node and below, *ESSCIRC*, (I), 4–7

Fenouillet-Beranger, C., P. Perreau, O. Weber, I. Ben-Akkez, A. Cros, A. Bajolet, S. Haendler, et al.2012 Enhancement of Devices Performance of hybrid FDSOI/Bulk Technology by using UTBOX sSOI substrates, *Symposium on VLSI Technology*, 115–116. doi:10.1109/VLSIT.2012.6242488.

Fenouillet-Beranger, Skotnicki, Monfray, Carriere, and Boeuf2003 Requirements for ultra-thin-film devices and new materials on CMOS roadmap, *2003 IEEE International Conference on Robotics and Automation (Cat No 03CH37422) SOI-03*, IEEE, 0,145–146. doi:10.1109/SOI.2003.1242930.

Fischetti, M. V., and S. E. Laux1996 Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys, *Journal of Applied Physics*, 80 (4), 2234. doi:10.1063/1.363052.

Foucher, J., E. Pargon, M. Martin, S. Reyne, and C. Dupré2008 Paving the way for multiple applications for the 3D-AFM technique in the semiconductor industry 6922, 1–9. doi:10.1117/12.772675.

- Frank, D. J., Y. Taur, and H.-S. P. Wong 1998 Generalized scale length for two-dimensional effects in MOSFETs, *IEEE Electron Device Letters*, 19 (10) (October), 385–387. doi:10.1109/55.720194.
- Frank, Laux, and Fischetti 1992 Monte Carlo simulation of a 30 nm dual-gate MOSFET: how short can Si go?, *International Technical Digest on Electron Devices Meeting*, IEEE, 553–556. doi:10.1109/IEDM.1992.307422.
- Fu-Liang Yang, Di-Hong Lee, Hou-Yu Chen, Chang-Yun Chang, Sheng-Da Liu, Cheng-Chuan Huang, Tang-Xuan Chung, et al. 2004 5nm-gate nanowire FinFET, *Digest of Technical Papers. 2004 Symposium on VLSI Technology, 2004.*, IEEE, 196–197. doi:10.1109/VLSIT.2004.1345476.
- Gaben, L., A. Arnaud, M. Barlas, M. P. Samson, C. Arvet, C. Vizioz, J.-M. Hartmann, et al. 2016 Stacked Nanowires FETs: Mechanical robustness evaluation for sub-7nm nodes, *2016 IEEE Silicon Nanoelectronics Workshop (SNW)*, IEEE, June, 136–137. doi:10.1109/SNW.2016.7578020.
- Gaben, L., S. Barraud, M. Jaud, S. Martinie, O. Rozeau, J. Lacord, G. Hibelot, et al. 2015 Stacked-Nanowire and FinFET Transistors : Guidelines for the 7nm node, *SSDM*, 1006–1007
- Gaben, L., S. Barraud, M.-P. Samson, J.-M. Hartmann, C. Vizioz, F. Aussenac, F. Allain, et al. 2015 P-type trigate nano wires: Impact of nano wire thickness and Si $\langle$ 0.7 $\rangle$ /Ge $\langle$ 0.3 $\rangle$  source-drain epitaxy, *EUROSOI-ULIS 2015: 2015 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon*, IEEE, January, 13–16. doi:10.1109/ULIS.2015.7063761.
- Gaben, L., S. Barraud, M.-P. Samson, M.-A. Jaud, S. Martinie, O. Rozeau, J. Lacord, et al. 2016 (Invited) Evaluation of Stacked Nanowires Transistors for CMOS: Performance and Technology Opportunities, *ECS Transactions*, 72 (4) (May 19), 43–54. doi:10.1149/07204.0043ecst.
- Gamiz, F., and M. V. Fischetti 2001 Monte Carlo simulation of double-gate silicon-on-insulator inversion layers: The role of volume inversion, *Journal of Applied Physics*, 89 (10), 5478. doi:10.1063/1.1358321.
- Ghani, T., M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, et al. A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors, *IEEE International Electron Devices Meeting 2003*, IEEE, M, 11.6.1-11.6.3. doi:10.1109/IEDM.2003.1269442.
- Grenouillet, L., M. Vinet, J. Gimbert, B. Giraud, J. P. Noel, Q. Liu, P. Khare, et al. 2012 UTBB FDSOI transistors with dual STI for a multi-V<sub>t</sub> strategy at 20nm node and below, *Technical Digest - International Electron Devices Meeting, IEDM*, 4–7. doi:10.1109/IEDM.2012.6478974.
- Guarini, K. W., P. M. Solomon, Y. Zhang, K. K. Chan, E. C. Jones, G. M. Cohen, M. Ronay, et al. 2001 Triple-Self-Aligned , Planar Double-Gate MOSFETs : Devices and Circuits, *IEDM*, 425–428
- Ha, D., H. Takeuchi, Y.-K. Choi, T.-J. King, W. P. Baim, D.-L. Kwongo, A. Agarwal, and M. Ameen 2004 Molybdenum-gate HfO<sub>2</sub>/CMOS FinFET technology, *IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004.*, IEEE, 28, 643–646. doi:10.1109/IEDM.2004.1419248.
- Harrison, S., P. Coronel, A. Cros, R. Cerutti, F. Leverd, A. Beverina, R. Wacquez, et al. 2004 Poly-gate replacement through contact hole (PRETCH): a new method for high-K/metal gate and multi-oxide implementation on chip, *IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004.*, IEEE, 2, 291–294. doi:10.1109/IEDM.2004.1419136.
- Harrison, S., P. Coronel, F. Leverd, R. Cerutti, R. Palla, D. Delille, S. Borel, et al. 2003 Highly performant double gate MOSFET realized with SON process, *IEEE International Electron Devices Meeting 2003*, IEEE, 18.6.1-18.6.4. doi:10.1109/IEDM.2003.1269319.
- Hartmann, J.-M., A.-M. Papon, J.-P. Colonna, T. Ernst, and T. Billon 2008 Growth and Thermal Stability of SiGe/Si Superlattices on Bulk Si Wafers, *ECS Transactions*, ECS, 16, 341–351. doi:10.1149/1.2986792.

- Hartmann, J. M. 2007 Low temperature growth kinetics of high Ge content SiGe in reduced pressure-chemical vapor deposition, *Journal of Crystal Growth*, 305 (1) (July), 113–121. doi:10.1016/j.jcrysgro.2007.03.051.
- Hartmann, J. M. 2016 Si, SiGe, and Si(1-y)Cy on Si: Epitaxy of Group-IV Semiconductors for Nanoelectronics, *World Scientific*, . Vol. 1 IEEE, June
- Hartmann, J. M., V. Benevent, J. F. Damlencourt, and T. Billon 2012 A benchmarking of silane, disilane and dichlorosilane for the low temperature growth of group IV layers, *Thin Solid Films*, 520 (8), 3185–3189. doi:10.1016/j.tsf.2011.10.164.
- Hartmann, J. M., P. Holliger, F. Laugier, G. Rolland, A. Suhm, T. Ernst, T. Billon, and N. Vulliet 2005 Growth of SiGe/Si superlattices on silicon-on-insulator substrates for multi-bridge channel field effect transistors, *Journal of Crystal Growth*, 283 (1–2) (September), 57–67. doi:10.1016/j.jcrysgro.2005.05.068.
- Hartmann, J. M., M. Py, J. P. Barnes, B. Prévitali, P. Batude, and T. Billon 2011 Low temperature boron and phosphorous doped SiGe for recessed and raised sources and drains, *Journal of Crystal Growth*, 327 (1) (July), 68–77. doi:10.1016/j.jcrysgro.2011.05.009.
- Hashemi, P., T. Ando, K. Balakrishnan, E. Cartier, M. Lofaro, J. A. Ott, J. Bruley, et al. 2016 Replacement high-K/metal-gate High-Ge-content strained SiGe FinFETs with high hole mobility and excellent SS and reliability at aggressive EOT 7A and scaled dimensions down to sub-4nm fin widths, *Digest of Technical Papers - Symposium on VLSI Technology*, 2016–Sept, 96–97. doi:10.1109/VLSIT.2016.7573392.
- Hashemi, P., and M. Kobayashi 2013 High-performance Si 1– x Ge x channel on insulator trigate PFETs featuring an implant-free process and aggressively-scaled fin and gate dimensions, *VLSI Circuits (VLSIC ...)*, 18–19
- Hashemi, P., J. T. Teherani, and J. L. Hoyt 2010 Investigation of hole mobility in gate-all-around Si nanowire p-MOSFETs with high-k/metal-gate: Effects of hydrogen thermal annealing and nanowire shape, *2010 International Electron Devices Meeting*, IEEE, December, 34.5.1–34.5.4. doi:10.1109/IEDM.2010.5703477.
- He, H., P. Brabant, K. Chung, M. Shinriki, T. Adam, A. Reznicek, D. Sadana, S. Hasaka, and T. Francis 2012 High strain embedded-SiGe via low temperature reduced pressure chemical vapor deposition, *Thin Solid Films*, 520 (8) (February), 3175–3178. doi:10.1016/j.tsf.2011.10.082.
- Hiblot, G. 2015 Compact modeling of MOSFET transistors with III-V
- Hiblot, G., Q. Rafhay, L. Gaben, G. Ghibaudo, and F. Boeuf 2015 Optimization of Trigate-On-Insulator MOSFET aspect ratio with MASTAR, *2015 45th European Solid State Device Research Conference (ESSDERC)*, IEEE, September, 2015–Novem, 242–245. doi:10.1109/ESSDERC.2015.7324759.
- Hieda, K., F. Horigu, H. Watanabe, K. Sunouchi, I. Inoue, and T. Hamamoto 1987 New effects of trench isolated transistor using side-wall gates, *1987 International Electron Devices Meeting*, IRE, 736–739. doi:10.1109/IEDM.1987.191536.
- Hieda, K., F. Horiguchi, H. Watanabe, K. Sunouchi, I. Inoue, and T. Hamamoto 1989 Effects of a new trench-isolated transistor using sidewall gates, *IEEE Transactions on Electron Devices*, 36 (9), 1615–1619. doi:10.1109/16.34221.
- Hisamoto, D., T. Kaga, Y. Kawamoto, and E. Takeda 1989 A fully depleted lean-channel transistor (DELTA)-a novel vertical ultra thin SOI MOSFET, *International Technical Digest on Electron Devices Meeting*, IEEE, 833–836. doi:10.1109/IEDM.1989.74182.
- Hisamoto, D., T. Kaga, and E. Takeda 1991 Impact of the vertical SOI “DELTA” structure on planar device technology, *IEEE Transactions on Electron Devices*, 38 (6) (June), 1419–1424. doi:10.1109/16.81634.
- Hisamoto, D., W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu 2000

FinFET-a self-aligned double-gate MOSFET scalable to 20 nm, *IEEE Transactions on Electron Devices*, 47 (12), 2320–2325. doi:10.1109/16.887014.

Hisamoto, D., Wen-Chin Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, Tsu-Jae King, J. Bokor, and Chenming Hu1998 A folded-channel MOSFET for deep-sub-tenth micron era, *International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217)*, IEEE, 38,1032–1034. doi:10.1109/IEDM.1998.746531.

Hon-Sum Wong, D. J. Frank, Yuan Taur, and J. M. C. Stork1994 Design and performance considerations for sub-0.1  $\mu\text{m}$  double-gate SOI MOSFET'S, *Proceedings of 1994 IEEE International Electron Devices Meeting*, IEEE, 747–750. doi:10.1109/IEDM.1994.383315.

Hubert, A., J.-P. Colonna, S. Bécu, C. Dupré, V. Maffini-Alvaro, J.-M. Hartmann, S. Pauliac, et al.2008 Oxidation of Suspended Stacked Silicon Nanowire for Sub-10nm Cross-Section Shape Optimization, *ECS Transactions*, ECS, 13,195–199. doi:10.1149/1.2911500.

Huguenin, J.-L., J. Lacord, S. Monfray, R. Coquand, T. Skotnicki, G. Ghibaudo, and F. Boeuf2011 Comparative study of circuit perspectives for multi-gate structures at sub-10nm node, *2011 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, IEEE, September, 107–110. doi:10.1109/ESSDERC.2011.6044223.

Huguenin, J.-L., S. Monfray, G. Bidal, S. Denorme, P. Perreau, S. Barnola, M.-P. Samson, et al.2010 Hybrid Localized SOI/bulk technology for low power system-on-chip, *2010 Symposium on VLSI Technology*, 59–60. doi:10.1109/VLSIT.2010.5556119.

Hwang, B., J. Han, M. Kim, S. Jung, N. Lim, S. Jin, Y. Yim, et al.2009 Comparison of double patterning technologies in NAND flash memory with sub-30nm node, *2009 Proceedings of the European Solid State Device Research Conference*, IEEE, September, 269–271. doi:10.1109/ESSDERC.2009.5331401.

Hyung-Kyu Lim, and J. G. Fossum1983 Threshold voltage of thin-film Silicon-on-insulator (SOI) MOSFET's, *IEEE Transactions on Electron Devices*, 30 (10) (October), 1244–1251. doi:10.1109/T-ED.1983.21282.

Iizuka, T., K. Y. Chiu, and J. L. Moll1981 Double threshold MOSFETs in bird's-beak free structures, *1981 International Electron Devices Meeting*, IRE, 380–383. doi:10.1109/IEDM.1981.190093.

Ionescu, A. M., and H. Riel2011 Tunnel field-effect transistors as energy-efficient electronic switches., *Nature*, 479 (7373), 329–37. doi:10.1038/nature10679.

Izumi, K., M. Doken, and H. Ariyoshi1978 C.M.O.S. devices fabricated on buried SiO<sub>2</sub> layers formed by oxygen implantation into silicon, *Electronics Letters*, 14 (18), 593. doi:10.1049/el:19780397.

Jahan, C., O. Faynot, M. Casse, R. Ritzenthaler, L. Brevard, L. Tosti, X. Garros, et al.2005  $\Omega$ FETs transistors with tin metal gate and HfO<sub>2</sub> down to 10nm, *Digest of Technical Papers. 2005 Symposium on VLSI Technology, 2005.*, IEEE, 2005,112–113. doi:10.1109/.2005.1469233.

Jin, S., M. V. Fischetti, and T. W. Tang2007 Modeling of electron mobility in gated silicon nanowires at room temperature: Surface roughness scattering, dielectric screening, and band nonparabolicity, *Journal of Applied Physics*, 102 (8). doi:10.1063/1.2802586.

Jurczak, M., T. Skotnicki, M. Paoli, B. Tormen, J. Martins, J. L. Regolini, D. Dutartre, et al.2000 Silicon-on-Nothing (SON)-an innovative process for advanced CMOS, *IEEE Transactions on Electron Devices*, 47 (11), 2179–2187. doi:10.1109/16.877181.

Jurczak, M., T. Skotnicki, M. Paoli, B. Tormen, J.-L. Regolini, C. Morin, A. Schiltz, J. Martins, R. Pantel, and J. Galvier1999 SON (silicon on nothing)-a new device architecture for the ULSI era, *1999 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.99CH36325)*, Japan Soc. Appl. Phys, 33,29–30. doi:10.1109/VLSIT.1999.799324.

Kah-Wee Ang, King-Jien Chui, V. Bliznetsov, Yihua Wang, Lai-Yin Wong, Chih-Hang Tung, N. Balasubramanian, Ming-Fu

- Li, G. Samudra, and Yee-Chia Yeo 2005 Thin body silicon-on-insulator N-MOSFET with silicon-carbon source/drain regions for performance enhancement, *IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest.*, IEEE, 0,497–500. doi:10.1109/IEDM.2005.1609390.
- Kawasaki, H., V. S. Basker, T. Yamashita, C.-H. Lin, Y. Zhu, J. Faltermeier, S. Schmitz, et al. 2009 Challenges and solutions of FinFET integration in an SRAM cell and a logic circuit for 22 nm node and beyond, *2009 IEEE International Electron Devices Meeting (IEDM)*, IEEE, December, 1–4. doi:10.1109/IEDM.2009.5424366.
- Kedzierski, J., D. M. Fried, E. J. Nowak, T. Kanarsky, J. H. Rankin, H. Hanafi, W. Natzle, et al. 2001 High-performance symmetric-gate and CMOS-compatible V/sub t/ asymmetric-gate FinFET devices, *International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224)*, IEEE, 19.5.1-19.5.4. doi:10.1109/IEDM.2001.979530.
- Kedzierski, J., M. Jeong, T. Kanarsky, Y. Zhang, and H.-S. P. Wong 2004 Fabrication of Metal Gated FinFETs Through Complete Gate Silicidation With Ni, *IEEE Transactions on Electron Devices*, 51 (12) (December), 2115–2120. doi:10.1109/TED.2004.838448.
- Khakifirooz, A., R. Sreenivasan, B. N. Taber, F. Allibert, P. Hashemi, W. Chern, N. Xu, et al. 2013 Aggressively scaled strained silicon directly on insulator (SSDOI) FinFETs, *2013 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, IEEE, October, 1–2. doi:10.1109/S3S.2013.6716520.
- Kikuchi, Y., T. Hopf, G. Mannaert, Z. Tao, A. Waite, J. Cournoyer, J. Borniquel, et al. 2016 Improvement of the CMOS characteristics of bulk Si FinFETs by high temperature ion implantation, *2016 IEEE International Electron Devices Meeting (IEDM)*, IEEE, December, 17.5.1-17.5.4. doi:10.1109/IEDM.2016.7838440.
- Kim, M., S.-Y. Lee, E.-J. Yoon, S. Kim, J. Lian, K.-H. Lee, N. Cho, et al. 2006 122 Mb High Speed SRAM Cell with 25 nm Gate Length Multi-Bridge-Channel MOSFET (MBCFET) on Bulk Si Substrate, *2006 Symposium on VLSI Technology, 2006. Digest of Technical Papers.*, IEEE, 3,68–69. doi:10.1109/VLSIT.2006.1705220.
- Kim, S.-D., M. Guillorn, I. Lauer, P. Oldiges, T. Hook, and M.-H. Na 2015 Performance trade-offs in FinFET and gate-all-around device architectures for 7nm-node and beyond, *2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, IEEE, October, 1–3. doi:10.1109/S3S.2015.7333521.
- Kurosawa, K., T. Shibata, and H. Iizuka 1981 A new bird's-beak free field isolation technology for VLSI devices, *1981 International Electron Devices Meeting*, IRE, 384–387. doi:10.1109/IEDM.1981.190094.
- Lacord, J., G. Ghibaudo, and F. Boeuf 2012a Comprehensive and accurate parasitic capacitance models for two- and three-dimensional CMOS device structures, *IEEE Transactions on Electron Devices*, 59 (5), 1332–1344. doi:10.1109/TED.2012.2187454.
- Lacord, J., G. Ghibaudo, and F. Boeuf 2012b A Comparative Study of Minimal Supply Voltage of 6T-SRAM at the 16nm node using MASTAR into a Conventional CAD Environment, *SSDM*, 33 (4), 2–3
- Lacord, J., S. Martinie, O. Rozeau, M. A. Jaud, S. Barraud, and J. C. Barbé 2016 Parasitic capacitance analytical model for sub-7-nm multigate devices, *IEEE Transactions on Electron Devices*, 63 (2), 781–786. doi:10.1109/TED.2015.2506781.
- Lim, J. S., S. E. Thompson, and J. G. Fossum 2004 Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs, *IEEE Electron Device Letters*, 25 (11), 731–733. doi:10.1109/LED.2004.837581.
- Lim, T. C., E. Bernard, O. Rozeau, T. Ernst, B. Guillaumot, N. Vulliet, C. Buj-Dufournet, et al. 2009 Analog/RF performance of multichannel SOI MOSFET, *IEEE Transactions on Electron Devices*, 56 (7), 1473–1482. doi:10.1109/TED.2009.2021438.
- Lin, X., C. Feng, S. Zhang, W.-H. Ho, and M. Chan 2004 Characterization of double gate MOSFETs fabricated by a simple method on a recrystallized silicon film, *Solid-State Electronics*, 48 (12) (December), 2315–2319. doi:10.1016/j.sse.2004.04.015.

Lindert, N., L. Chang, Yang-Kyu Choi, E. H. Anderson, Wen-Chin Lee, Tsu-Jae King, J. Bokor, and Chenming Hu 2001 Sub-60-nm quasi-planar FinFETs fabricated using a simplified process, *IEEE Electron Device Letters*, 22 (10) (October), 487–489. doi:10.1109/55.954920.

Liou, H.-C., and J. Pretzer 1998 Effect of curing temperature on the mechanical properties of hydrogen silsesquioxane thin films, *Thin Solid Films*, 335 (1–2), 186–191. doi:10.1016/S0040-6090(98)00881-5.

Liow, T., K. Tan, R. T. P. Lee, C. Tung, G. S. Samudra, N. Balasubramanian, and Y. Yeo 2007 N-Channel (110)-Sidewall Strained FinFETs With Silicon-Carbon Source and Drain Stressors and Tensile Capping Layer, *IEEE Electron Device Letters*, 28 (11) (November), 1014–1017. doi:10.1109/LED.2007.908495.

Liu, H., Z. Xiong, P. Xuan, J. Bokor, C. W. Bay, and H. Kong 2002 High Performance Double-Gate SOI MOSFET Using Lateral Solid Phase Epitaxy, 110–111

Liu, Q., B. DeSalvo, P. Morin, N. Loubet, S. Pilorget, F. Chafik, S. Maitrejean, et al. 2014 FDSOI CMOS devices featuring dual strained channel and thin BOX extendable to the 10nm node, *2014 IEEE International Electron Devices Meeting*, IEEE, December, 9.1.1-9.1.4. doi:10.1109/IEDM.2014.7047014.

Liu, Q., F. Monsieur, a. Kumar, T. Yamamoto, a. Yagishita, P. Kulkarni, S. Ponoth, et al. 2011 Impact of back bias on ultra-thin body and BOX (UTBB) devices, *2011 Symposium on VLSI Technology - Digest of Technical Papers*, 160–161

Liu, Q., M. Vinet, J. Gimbert, N. Loubet, R. Wacquez, L. Grenouillet, Y. Le Tiec, et al. 2013 High performance UTBB FDSOI devices featuring 20nm gate length for 14nm node and beyond, *2013 IEEE International Electron Devices Meeting*, IEEE, December, 9.2.1-9.2.4. doi:10.1109/IEDM.2013.6724592.

Liu, Y., M. Masahara, K. Ishii, T. Sekigawa, H. Takashima, H. Yamauchi, E. Suzuki, H. Takashima, H. Yamauchi, and E. Suzuki 2004 A Highly Threshold Voltage-Controllable 4T FinFET with an 8.5-nm-Thick Si-Fin Channel, *IEEE Electron Device Letters*, 25 (7) (July), 510–512. doi:10.1109/LED.2004.831205.

Liu, Y. X., K. Ishii, T. Tsutsumi, M. Masahara, H. Takashima, and E. Suzuki 2003 Ultra-narrow rectangular cross-section Si-Fin channel double-gate MOSFETs fabricated by using orientation-dependent wet etching, *61st Device Research Conference. Conference Digest (Cat. No.03TH8663)*, IEEE, 2003–Janua, 31–32. doi:10.1109/DRC.2003.1226857.

Lolivier, J., J. Widiez, A. Vinet, T. Poiroux, F. Dauge, B. Previtali, A. Mouis, J. Jommah, F. Balestra, and S. Deleonibus 2004 Experimental comparison between double gate, ground plane, and single gate SOI CMOSFETs, *Proceedings of the 30th European Solid-State Circuits Conference (IEEE Cat. No.04EX850)*, IEEE, 77–80. doi:10.1109/ESSDER.2004.1356492.

Lu, C.-M. V., C. Fenouillet-Beranger, J.-M. Hartmann, P. Rodriguez, V. Benevent, M.-P. Samson, B. Previtali, et al. 2016 Integration of Low Temperature SiGe:B Raised Sources and Drains in p-Type FDSOI Field Effect Transistors, *ECS Transactions*, 75 (8) (September 23), 51–58. doi:10.1149/07508.0051ecst.

Lubk, A., E. Javon, N. Cherkashin, S. Reboh, C. Gatel, and M. Hÿtch 2014 Dynamic scattering theory for dark-field electron holography of 3D strain fields, *Ultramicroscopy*, 136, 42–49. doi:10.1016/j.ultramicro.2013.07.007.

Maitra, K., A. Khakifirooz, P. Kulkarni, V. S. Basker, J. Faltermeier, H. Jagannathan, H. Adhikari, et al. 2011 Aggressively Scaled Strained-Silicon-on-Insulator Undoped-Body High- $\kappa$ /Metal-Gate nFinFETs for High-Performance Logic Applications, *IEEE Electron Device Letters*, 32 (6) (June), 713–715. doi:10.1109/LED.2011.2126556.

Mayer, F., C. Le Royer, J. F. Damlencourt, K. Romanjek, F. Andrieu, C. Tabone, B. Previtali, and S. Deleonibus 2008 Impact of SOI, Si<sub>1-x</sub>Ge<sub>x</sub>OI and GeOI substrates on CMOS compatible tunnel FET performance, *Technical Digest - International Electron Devices Meeting, IEDM*, 4, 9–13. doi:10.1109/IEDM.2008.4796641.

Mertens, H., R. Ritzenthaler, A. Hikavy, M. S. Kim, Z. Tao, K. Wostyn, S. A. Chew, et al. 2016 Gate-All-Around MOSFETs based on Vertically Stacked Horizontal Si Nanowires in a Replacement Metal Gate Process on Bulk Si Substrates, *VLSI*

- Mistry, K., C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, et al.2007 A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging, *2007 IEEE International Electron Devices Meeting*, IEEE, 247–250. doi:10.1109/IEDM.2007.4418914.
- Monfray, S., D. Chanemougame, S. Borel, A. Talbot, F. Loverd, N. Planes, D. Delille, et al.2004 SON (silicon-on-nothing) technological CMOS platform: highly performant devices and SRAM cells, *IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004.*, IEEE, 4,635–638. doi:10.1109/IEDM.2004.1419246.
- Monfray, S., J.-L. Huguenin, M. Martin, M.-P. Samson, C. Borowiak, C. Arvet, J. Dalemcourt, et al.2010 A solution for an ideal planar multi-gates process for ultimate CMOS?, *2010 International Electron Devices Meeting*, IEEE, December, 11.2.1-11.2.4. doi:10.1109/IEDM.2010.5703339.
- Monfray, S., T. Skotnicki, Y. Morand, S. Descombes, P. Coronel, P. Mazoyer, S. Harrison, et al.2002 50 nm-Gate All Around (GAA)-Silicon On Nothing (SON)-devices: a simple way to co-integration of GAA transistors within bulk MOSFET process, *2002 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.01CH37303)*, IEEE, 108–109. doi:10.1109/VLSIT.2002.1015411.
- Monfray, S., T. Skotnicki, Y. Morand, S. Descombes, M. Paoli, P. Ribot, A. Talbot, et al.2001 First 80 nm SON (Silicon-On-Nothing) MOSFETs with perfect morphology and high electrical performance, *International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224)*, IEEE, 29.7.1-29.7.4. doi:10.1109/IEDM.2001.979591.
- Monfray, Skotnicki, Morand, Descombes, Talbot, Dutartre, Leverd, et al.2002 Highly-performant 38 nm SON (silicon-on-nothing) P-MOSFETs with 9 nm-thick channels, *IEEE International SOI Conference SOI-02*, IEEE, 20–22. doi:10.1109/SOI.2002.1044400.
- Moore, G. E.2003 No exponential is forever: But ‘forever’ can be delayed!, *Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International*, 20–23 vol.1. doi:10.1109/ISSCC.2003.1234194.
- Morvan, S., C. Le Royer, F. Andrieu, P. Perreau, Y. Morand, D. Cooper, M. Casse, et al.2013 Gate-last integration on planar FDSOI MOSFET: Impact of mechanical boosters and channel orientations, *Technical Digest - International Electron Devices Meeting, IEDM,*. doi:10.1109/IEDM.2013.6724668.
- Natarajan, S., M. Agostinelli, S. Akbar, M. Bost, A. Bowonder, V. Chikarmane, S. Chouksey, et al.2014 A 14nm logic technology featuring 2<sup>nd</sup>-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 &#x00B5;m<sup>2</sup> SRAM cell size, *2014 IEEE International Electron Devices Meeting*, IEEE, December, 3.7.1-3.7.3. doi:10.1109/IEDM.2014.7046976.
- Neophytou, N., and H. Kosina2011 Atomistic simulations of low-field mobility in Si nanowires: Influence of confinement and orientation, *Physical Review B*, 84 (8) (August 23), 85313. doi:10.1103/PhysRevB.84.085313.
- Nguyen, P., S. Barraud, M. Koyama, M. Casse, F. Andrieu, C. Tabone, F. Glowacki, et al.2014 High mobility w-gate nanowire P-FET on cSGOI substrates obtained by Ge enrichment technique, *2014 SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, IEEE, October, 1–2. doi:10.1109/S3S.2014.7028187.
- Nguyen, P., S. Barraud, C. Tabone, L. Gaben, M. Casse, F. Glowacki, J.-M. Hartmann, et al.2014 Dual-channel CMOS co-integration with Si NFET and strained-SiGe PFET in nanowire device architecture featuring sub-15nm gate length, *2014 IEEE International Electron Devices Meeting*, IEEE, December, 16.2.1-16.2.4. doi:10.1109/IEDM.2014.7047062.
- Niebojewski, H.2014 Contacts auto-alignés ( SAC ) pour la technologie CMOS 10nm FDSOI
- Niquet, Y.-M., C. Delerue, and C. Krzeminski2012 Effects of Strain on the Carrier Mobility in Silicon Nanowires, *Nano Letters*, 12 (7) (July 11), 3545–3550. doi:10.1021/nl3010995.
- Niquet, Y., C. Delerue, D. Rideau, and B. Videau2012 Fully Atomistic Simulations of Phonon-Limited Mobility of

- Electrons and Holes in  $\langle 100 \rangle$ -,  $\langle 110 \rangle$ -,  $\langle 111 \rangle$ -silicon, *IEEE Transactions on Electron Devices*, 59 (5) (May), 1480–1487. doi:10.1109/TED.2012.2187788.
- Niquet, Y. M., C. Delerue, and D. Rideau 2012 Orientational and strain dependence of the mobility in silicon nanowires, *2012 13th International Conference on Ultimate Integration on Silicon (ULIS)*, IEEE, March, 49–52. doi:10.1109/ULIS.2012.6193354.
- Noel, J. P., O. Thomas, M. A. Jaud, O. Weber, T. Poiroux, C. Fenouillet-Beranger, P. Rivallin, et al. 2011 Multi-VT UTBB FDSOI device architectures for low-power CMOS circuit, *IEEE Transactions on Electron Devices*, 58 (8), 2473–2482. doi:10.1109/TED.2011.2155658.
- Park, J. T., J. P. Colinge, and C. H. Diaz 2001 Pi-gate SOI MOSFET, *IEEE Electron Device Letters*, 22 (8), 405–406. doi:10.1109/55.936358.
- Pasini, L., P. Batude, M. Casse, B. Mathieu, B. Sklenard, F. P. Luce, S. Reboh, et al. 2015 High performance low temperature activated devices and optimization guidelines for 3D VLSI integration of FD, TriGate, FinFET on insulator, *2015 Symposium on VLSI Technology (VLSI Technology)*, IEEE, June, T50–T51. doi:10.1109/VLSIT.2015.7223699.
- Planes, N., O. Weber, V. Barral, S. Haendler, D. Noblet, D. Croain, M. Bocat, et al. 2012 28nm FDSOI technology platform for high-speed low-voltage digital applications, *2012 Symposium on VLSI Technology (VLSIT)*, IEEE, June, 33,133–134. doi:10.1109/VLSIT.2012.6242497.
- Poiroux, T., M. Vinet, and S. Deleonibus 2009 Multiple Gate Technologies, *Planar Double-Gate Transistor*, Dordrecht: Springer Netherlands, 3–25. doi:10.1007/978-1-4020-9341-8\_2.
- Poiroux, T., M. Vinet, O. Faynot, J. Widiez, J. Lolivier, B. Previtali, T. Ernst, and S. Deleonibus 2006 Multigate silicon MOSFETs for 45nm node and beyond, *Solid-State Electronics*, 50 (1) (January), 18–23. doi:10.1016/j.sse.2005.10.049.
- Pons, N., F. Triozon, M.-A. Jaud, R. Coquand, S. Martinie, O. Rozeau, Y.-M. Niquet, V.-H. Nguyen, A. I.-E. Oudrhiri, and S. Barraud 2013 Density Gradient calibration for 2D quantum confinement: Tri-Gate SOI transistor application, *2013 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, IEEE, September, 184–187. doi:10.1109/SISPAD.2013.6650605.
- Price, P. .1981 Two-dimensional electron transport in semiconductor layers. I. Phonon scattering, *Annals of Physics*, 133 (2) (May), 217–239. doi:10.1016/0003-4916(81)90250-5.
- Reboh, S., R. Coquand, E. Augendre, S. Barraud, S. Maitrejean, M. Vinet, O. Faynot, et al. 2016 An analysis of stress evolution in stacked GAA transistors, *2016 IEEE Silicon Nanoelectronics Workshop (SNW)*, IEEE, June 1, 795,206–207. doi:10.1109/SNW.2016.7578053.
- Reboh, S., P. Morin, M. J. Hÿtch, F. Houdellier, and A. Claverie 2013 Mechanics of silicon nitride thin-film stressors on a transistor-like geometry, *APL Materials*, 1 (4) (October), 42117. doi:10.1063/1.4826545.
- Ritzenthaler, R., O. Faynot, and C. Jahan 2005 Corner and Coupling Effects in Triple-Gate FETs, *ECS Transactions*,
- Romanjek, K., F. Andrieu, T. Ernst, and G. Ghibaudo 2004 Improved Split C–V Method for Effective Mobility Extraction in sub-0.1- $\mu\text{m}$  Si MOSFETs, *IEEE Electron Device Letters*, 25 (8) (August), 583–585. doi:10.1109/LED.2004.832786.
- Le Royer, C., A. Villalon, M. Casse, D. Cooper, J. Mazurier, B. Previtali, C. Tabone, et al. 2011 First demonstration of ultrathin body c-SiGe channel FDSOI pMOSFETs combined with SiGe(:B) RSD: Drastic improvement of electrostatics ( $V_{th}$  tuning, DIBL) and transport ( $I_{on}$ ,  $I_{off}$ ) properties down to 23nm gate length, *2011 International Electron Devices Meeting*, IEEE, December, 16.5.1-16.5.4. doi:10.1109/IEDM.2011.6131567.
- Saitoh, M., Y. Nakabayashi, H. Itokawa, M. Murano, I. Mizushima, K. Uchida, and T. Numata 2010 Short-channel

performance and mobility analysis of <110>- and <100>-oriented tri-gate nanowire MOSFETs with raised source/drain extensions, *2010 Symposium on VLSI Technology*, IEEE, June, 169–170. doi:10.1109/VLSIT.2010.5556214.

Salvetat, T., V. Destefanis, S. Borel, J.-M. Hartmann, O. Kermarrec, and Y. Campidelli2008 Comparison Between Three Si1-xGex versus Si Selective Etching Processes, *ECS Transactions*, ECS, 16,439–449. doi:10.1149/1.2986801.

Schulz, T., W. Rösner, E. Landgraf, L. Risch, and U. Langmann2002 Planar and vertical double gate concepts, *Solid-State Electronics*, 46 (7) (July), 985–989. doi:10.1016/S0038-1101(02)00031-X.

Sekigawa, T., and Y. Hayashi1984 Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate, *Solid-State Electronics*, 27 (8–9) (August), 827–828. doi:10.1016/0038-1101(84)90036-4.

Shengdong Zhang, Xinnan Lin, Ru Huang, Ruqi Han, and Mansun Chan2003 A self-aligned, electrically separable double-gate mos transistor technology for dynamic threshold voltage application, *IEEE Transactions on Electron Devices*, 50 (11) (November), 2297–2300. doi:10.1109/TED.2003.818598.

Shenoy, R. S., and K. C. Saraswat2004 Novel process for fully self-aligned planar ultrathin body Double-Gate FET, *2004 IEEE International SOI Conference (IEEE Cat. No.04CH37573)*, IEEE, 190–191. doi:10.1109/SOI.2004.1391611.

Skotnicki, T., C. Denat, P. Senn, G. Merckel, and B. Hennion1994 A new analog/digital CAD model for sub-halfmicron MOSFETs, *Proceedings of 1994 IEEE International Electron Devices Meeting*, IEEE, 165–168. doi:10.1109/IEDM.1994.383439.

Skotnicki, T., C. Fenouillet-Beranger, C. Gallon, F. Boeuf, S. Monfray, F. Payet, A. Pouydebasque, et al.2008 Innovative Materials, Devices, and CMOS Technologies for Low-Power Mobile Multimedia, *IEEE Transactions on Electron Devices*, 55 (1) (January), 96–130. doi:10.1109/TED.2007.911338.

Skotnicki, T., M. Jrczak, R. Gwoziecki, D. Lenoble, P. Ribot, M. Paoli, J. Martins, et al.1999 Heavily doped and extremely shallow junctions on insulator by SONCTION (SilicON Cut-off junctionION) process, *International Electron Devices Meeting 1999. Technical Digest (Cat. No.99CH36318)*, IEEE, 0,513–516. doi:10.1109/IEDM.1999.824205.

Skotnicki, T., G. Merckel, and T. Pedron1988 The Voltage-Doping Transformation: A New Approach to the Modeling of MOSFET Short-Channel Effects, *IEEE Electron Device Letters*, 9 (3), 109–112. doi:10.1109/55.2058.

Skotnicki, T., and S. Monfray2006 Silicon-on-nothing (SON) technology, *2006 8th International Conference on Solid-State and Integrated Circuit Technology Proceedings*, IEEE, 11–14. doi:10.1109/ICSICT.2006.306043.

Smith, M. L.1956 *Electromagnetically Enriched Isotopes and Mass Spectroscopy*, London: Butterworth

Sturm, J. C., K. Tokunaga, and J.-P. Colinge1988 Increased drain saturation current in ultra-thin silicon-on-insulator (SOI) MOS transistors, *IEEE Electron Device Letters*, 9 (9) (September), 460–463. doi:10.1109/55.6945.

Suh, J., R. Nakane, N. Taoka, M. Takenaka, and S. Takagi2011 Highly strained-SiGe-on-insulator p-channel metal-oxide-semiconductor field-effective transistors fabricated by applying Ge condensation technique to strained-Si-on-insulator substrates, *Applied Physics Letters*, 99 (14). doi:10.1063/1.3647631.

Sung-Young Lee, Eun-Jung Yoon, Sung-Min Kim, Chang Woo Oh, Ming Li, Jeong-Dong Choi, Kyoung-Hwan Yeo, et al.2004 A novel sub-50 nm multi-bridge-channel MOSFET (MBCFET) with extremely high performance, *Digest of Technical Papers. 2004 Symposium on VLSI Technology, 2004.*, IEEE, 200–201. doi:10.1109/VLSIT.2004.1345478.

Sung-Young Lee, Sung-Min Kim, Eun-Jung Yoon, Chang-Woo Oh, Ilsub Chung, Donggun Park, and Kinam Kim2003 A novel multibrige-channel MOSFET (MBCFET): fabrication technologies and characteristics, *IEEE Transactions On Nanotechnology*, 2 (4) (December), 253–257. doi:10.1109/TNANO.2003.820777.

Sung Dae Suk, Sung-Young Lee, Sung-Min Kim, Eun-Jung Yoon, Min-Sang Kim, Ming Li, Chang Woo Oh, et al.2005 High performance 5nm radius Twin Silicon Nanowire MOSFET (TSNWFET) : fabrication on bulk si wafer, characteristics, and

reliability, *IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest.*, IEEE, 0,717–720. doi:10.1109/IEDM.2005.1609453.

Sung Min Kim, Eun Jung Yoon, Hye Jin Jo, Ming Li, Chang Woo Oh, Sung Young Lee, Kyoung Hwan Yeo, et al.2004 A novel multi-channel field effect transistor (McFET) on bulk Si for high performance sub-80nm application, *IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004.*, IEEE, 639–642. doi:10.1109/IEDM.2004.1419247.

Suzuki, K., T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto1993 Scaling theory for double-gate SOI MOSFET's, *IEEE Transactions on Electron Devices*, 40 (12), 2326–2329. doi:10.1109/16.249482.

Tachi, K., M. Cassé, S. Barraud, C. Dupré, a. Hubert, N. Vulliet, M. E. Faivre, et al.2010 Experimental study on carrier transport limiting phenomena in 10 nm width nanowire CMOS transistors, *Technical Digest - International Electron Devices Meeting, IEDM, (c)*, 784–787. doi:10.1109/IEDM.2010.5703476.

Tanaka, T., H. Horie, S. Ando, and S. Hijiya1991 Analysis of p/sup +/- poly Si double-gate thin-film SOI MOSFETs, *International Electron Devices Meeting 1991 [Technical Digest]*, IEEE, 1991–Janua,683–686. doi:10.1109/IEDM.1991.235330.

Tanaka, T., K. Suzuki, H. Horie, and T. Sugii1994 Ultrafast low-power operation of p/sup +/-n/sup +/- double-gate SOI MOSFETs, *Proceedings of 1994 VLSI Technology Symposium*, IEEE, 595,11–12. doi:10.1109/VLSIT.1994.324402.

Thomas, O., B. Guillaumot, T. Ernst, B. Cousin, and O. Rozeau2008 A power-efficient improved-stability 6T SRAM cell in 45nm multi-channel FET technology, *ESSDERC 2008 - Proceedings of the 38th European Solid-State Device Research Conference*, 150–153. doi:10.1109/ESSDERC.2008.4681721.

Thompson, S., N. Anand, M. Armstrong, C. Auth, B. Arcot, M. Alavi, P. Bai, et al.A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low k ILD, and 1  $\mu\text{m}^2$  SRAM cell, *Digest. International Electron Devices Meeting*, IEEE, 61–64. doi:10.1109/IEDM.2002.1175779.

Thompson, S. E., G. Sun, K. Wu, J. Lim, and T. Nishida2004 Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs, *IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004.*, IEEE, 221–224. doi:10.1109/IEDM.2004.1419114.

Togo, M., J. W. Lee, L. Pantisano, T. Chiarella, R. Ritzenthaler, R. Krom, A. Hikavy, et al.2012 Phosphorus doped SiC Source Drain and SiGe channel for scaled bulk FinFETs, *2012 International Electron Devices Meeting*, IEEE, December, 18.2.1-18.2.4. doi:10.1109/IEDM.2012.6479064.

Tsai, H., J. W. Pitera, H. Miyazoe, S. Bangsaruntip, S. U. Engelmann, C.-C. Liu, J. Y. Cheng, et al.2014 Two-Dimensional Pattern Formation Using Graphoepitaxy of PS- b -PMMA Block Copolymers for Advanced FinFET Device and Circuit Fabrication, *ACS Nano*, 8 (5) (May 27), 5227–5232. doi:10.1021/nn501300b.

Veloso, A., L.-A. Ragnarsson, M. J. Cho, K. Devriendt, K. Kellens, F. Sebaai, S. Suhard, et al.2011 Gate-last vs. gate-first technology for aggressively scaled EOT logic/RF CMOS, *2011 Symposium on VLSI Technology - Digest of Technical Papers*, 2011, 34–35

Veloso, A., L. Witters, M. Demand, I. Ferain, N. J. Son, B. Kaczer, P. J. Roussel, et al.2008 Flexible and robust capping-metal gate integration technology enabling multiple-VT CMOS in MuGFETs, *2008 Symposium on VLSI Technology*, IEEE, June, 2008,14–15. doi:10.1109/VLSIT.2008.4588545.

Venkatesan, S., G. W. Neudeck, and R. F. Pierret1992 Dual-gate operation and volume inversion in n-channel SOI MOSFET's, *IEEE Electron Device Letters*, 13 (1) (January), 44–46. doi:10.1109/55.144946.

Vinet, M., T. Poiroux, C. Licitra, J. Widiez, J. Bhandari, B. Previtali, C. Vizioz, et al.2009 Self-Aligned Planar Double-Gate MOSFETs by Bonding for 22-nm Node, With Metal Gates, High- $\kappa$  Dielectrics, and Metallic Source/Drain, *IEEE Electron Device Letters*, 30 (7) (July), 748–750. doi:10.1109/LED.2009.2020614.

- Vinet, M., T. Poiroux, J. Widiez, J. Lolivier, B. Previtali, C. Vizios, B. Guillaumot, et al. 2005 Bonded planar double-metal-gate NMOS transistors down to 10 nm, *IEEE Electron Device Letters*, 26 (5) (May), 317–319. doi:10.1109/LED.2005.846580.
- Wacquez, R., P. Coronel, M. P. Samson, D. Delille, J. Bustos, and J. P. Gouy 2006 A Novel 3D Lithography : Self Aligned Patterning Through Thin Layers, *EIPBN*, 3 (7), 534–535
- Wan, C., C. Su, S. Hsu, G. Luo, T. Hou, W. Wu, and W. Yeh 2016 Suspended Ge GateAllAround Nanowire FETs with Selective Etching Technique, *SSDM*,
- Watanabe, M., and A. Tooi 1966 Formation of SiO<sub>2</sub> Films by Oxygen-Ion Bombardment, *Japanese Journal of Applied Physics*, 5 (8) (August), 737–738. doi:10.1143/JJAP.5.737.
- Weber, O., F. Andrieu, J. Mazurier, M. Casse, X. Garros, C. Leroux, F. Martin, et al. 2010 Work-function engineering in gate first technology for multi-V<sub>T</sub> dual-gate FDSOI CMOS on UTBOX, *2010 International Electron Devices Meeting*, IEEE, December, 3.4.1-3.4.4. doi:10.1109/IEDM.2010.5703289.
- Weber, O., E. Josse, F. Andrieu, A. Cros, E. Richard, P. Perreau, E. Baylac, et al. 2014 14nm FDSOI technology for high speed and energy efficient applications, *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers*, IEEE, June, 1–2. doi:10.1109/VLSIT.2014.6894343.
- Weber, O., E. Josse, J. Mazurier, N. Degors, S. Chhun, P. Maury, S. Lagrasta, D. Barge, J.-P. Manceau, and M. Haond 2015 14nm FDSOI Upgraded Device Performance for Ultra-Low Voltage Operation, *Symposium on VLSI Technology*, T168–T169. doi:10.1109/VLSIT.2015.7223664.
- Weber, O., and S. Takagi 2008 Experimental Examination and Physical Understanding of the Coulomb Scattering Mobility in Strained-Si nMOSFETs, *IEEE Transactions on Electron Devices*, 55 (9) (September), 2386–2396. doi:10.1109/TED.2008.927388.
- Wei, L., F. Boeuf, T. Skotnicki, and H. S. P. Wong 2011 Parasitic capacitances: Analytical models and impact on circuit-level performance, *IEEE Transactions on Electron Devices*, 58 (5), 1361–1370. doi:10.1109/TED.2011.2121912.
- Widiez, J., F. Dauge, M. Vinet, T. Poiroux, B. Previtali, M. Mouis, and S. Deleonibus 2004 Experimental gate misalignment analysis on double gate SOI MOSFETs, *2004 IEEE International SOI Conference (IEEE Cat. No.04CH37573)*, IEEE, 185–186. doi:10.1109/SOI.2004.1391609.
- Widiez, J., M. Vinet, T. Poiroux, P. Holliger, B. Previtali, P. Grosgeorges, M. Mouis, and S. Deleonibus 2005 TiN metal gate thickness influence on Fully Depleted SOI MOSFETs physical and electrical properties, *2005 IEEE International SOI Conference*, 30–31. doi:10.1109/SOI.2005.1563523.
- Wong, H.-S. P., K. K. Chan, and Y. Taur 1997 Self-aligned (top and bottom) double-gate MOSFET with a 25 nm thick silicon channel, *International Electron Devices Meeting. IEDM Technical Digest*, IEEE, 427–430. doi:10.1109/IEDM.1997.650416.
- Woo Lee, J., D. Jang, M. Mouis, K. Tachi, G. Tae Kim, T. Ernst, and G. Ghibaudo 2012 Short channel mobility analysis of SiGe nanowire p-type field effect transistors: Origins of the strain induced performance improvement, *Applied Physics Letters*, 101 (14), 1–5. doi:10.1063/1.4756910.
- Wu, C., X. Lu, L. Peng, K. Xu, X. Peng, J. Huang, G. Yu, and Y. Xie 2013 Two-dimensional vanadyl phosphate ultrathin nanosheets for high energy density and flexible pseudocapacitors, *Nature Communications*, 4 (September 12), 2431. doi:10.1038/ncomms3431.
- Wu, S.-Y., C. Y. Lin, M. C. Chiang, J. J. Liaw, J. Y. Cheng, S. H. Yang, C. H. Tsai, et al. 2016 A 7nm CMOS platform technology featuring 4 th generation FinFET transistors with a 0.027um<sup>2</sup> high density 6-T SRAM cell for mobile SoC applications, *2016 IEEE International Electron Devices Meeting (IEDM)*, IEEE, December, 2.6.1-2.6.4.

doi:10.1109/IEDM.2016.7838333.

Wu, X., P. C. H. Chan, and M. Chan2005 Impacts of Nonrectangular Fin Cross Section on the Electrical Characteristics of FinFET, *IEEE Transactions on Electron Devices*, 52 (1) (January), 63–68. doi:10.1109/TED.2004.841334.

Xie, R., P. Montanini, K. Akarvardar, N. Tripathi, B. Haran, S. Johnson, T. Hook, et al.2016 A 7nm FinFET technology featuring EUV patterning and dual strained high mobility channels, *2016 IEEE International Electron Devices Meeting (IEDM)*, IEEE, December, 12,2.7.1-2.7.4. doi:10.1109/IEDM.2016.7838334.

Xuejue Huang, Wen-Chin Lee, Charles Kuo, D. Hisamoto, Leland Chang, J. Kedzierski, E. Anderson, et al.1999 Sub 50-nm FinFET: PMOS, *International Electron Devices Meeting 1999. Technical Digest (Cat. No.99CH36318)*, IEEE, 67–70. doi:10.1109/IEDM.1999.823848.

Yamashita, T., V. S. Basker, T. Standaert, C.-C. Yeh, T. Yamamoto, K. Maitra, C.-H. Lin, et al.2011 Sub-25nm FinFET with advanced fin formation and short channel effect engineering, *2011 Symposium on VLSI Technology - Digest of Technical Papers*, 14–15

Yan, R.-H., A. Ourmazd, and K. F. Lee1992 Scaling the Si MOSFET: from bulk to SOI to bulk, *IEEE Transactions on Electron Devices*, 39 (7) (July), 1704–1710. doi:10.1109/16.141237.

Yang-Kyu Choi, N. Lindert, Peiqi Xuan, S. Tang, Daewon Ha, E. Anderson, Tsu-Jae King, J. Bokor, and Chenming Hu2001 Sub-20 nm CMOS FinFET technologies, *International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224)*, 19.1.1-19.1.4. doi:10.1109/IEDM.2001.979526.

Yang-Kyu Choi, Tsu-Jae King, and Chenming Hu2002 A spacer patterning technology for nanoscale CMOS, *IEEE Transactions on Electron Devices*, 49 (3) (March), 436–441. doi:10.1109/16.987114.

Yang, M., M. leong, L. Shi, K. Chan, V. Chan, A. Chou, E. Gusev, et al.2003 High performance CMOS fabricated on hybrid substrate with different crystal orientations, *IEEE International Electron Devices Meeting 2003*, IEEE, 18.7.1-18.7.4. doi:10.1109/IEDM.2003.1269320.

Yun, E., M. Kim, S. Kim, S. Lee, D. Kim, and D. Park2006 Characteristics of MBCFET (Multi-Bridge-Channel MOSFET) with Tall-Embedded-Gate (TEG), *2006 8th International Conference on Solid-State and Integrated Circuit Technology Proceedings*, IEEE, 3,81–83. doi:10.1109/ICSICT.2006.306083.

Zantye, P. B., A. Kumar, and A. K. Sikder2004 Chemical mechanical planarization for microelectronics applications, *Materials Science and Engineering R: Reports*, 45 (3–6), 89–220. doi:10.1016/j.msere.2004.06.002.

Zhang, S., R. Han, X. Lin, X. Wu, and M. Chan2004 A Stacked CMOS Technology on SOI Substrate, *IEEE Electron Device Letters*, 25 (9) (September), 661–663. doi:10.1109/LED.2004.834735.

Zhao, D., T. Wang, Y. He, and X. Lu2013 Kinematic Optimization for Chemical Mechanical Polishing Based On Statistical Analysis of Particle Trajectories, *IEEE Transactions on Semiconductor Manufacturing*, 26 (4) (November), 556–563. doi:10.1109/TSM.2013.2281218.