Characterization and design of high-switching speed capability of GaN power devices in a 3-phase inverter

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Characterization and Design of High-Switching Speed Capability of GaN Power Devices in a 3-Phase Inverter

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« *Ce n'est pas parce que les choses sont difficiles que nous n'osons pas, c'est parce que nous n'osons pas que les choses sont difficiles.* » (Sénèque)

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List of Acronyms

AMR Anisotropic Magnetoresistance.

CTE Coeffcient of Thermal Expension.

DPT Double Pulse Test.
DSP Digital Signal Processor.

ESL Equivalent Series Inductance.
ESR Equivalent Series Resistance.

FEA Finite Element Analysis.
FoM Figure of Merit.

GaN Gallium Nitride.
GMR Giant Magnetoresistance.

HEMT High Electron Mobility Transistor.
HFET High Field Efect Transistor.

IC Integrated Circuit.

MLCC Multi-Layer Ceramic Capacitor.
MR Magnetoresistance.

OCP Over-Current Protection.

PEEC Partial Element Equivalent Circuit.

POL Point Of Load.

PPO Polyphenylene Oxide.

PTFE Polytetrafluoroethylene.

SMPS Switched-Mode Power Supply.

SOI Silicon On Insulator.

TCR Thermal Coeffcient of Resistance.

Tg Glass Transition Temperature.

TMR Tunnel Magnetoresistance.

WBG Wide Band Gap.

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Dissemination

The presented work has been disseminated through various conference and journal publications, as well as miscellaneous contributions to workshops, conferences, etc. All the disseminated work is listed in the following sections.

Conferences

- R. Perrin, D. Bergogne, B.Allard, C. Martin "GaN Power Module with High Temperature Gate Driver and Insulated Power Supply", in *High Temperature Electronics Conference(HiTEC)*, **2014**

- R. Perrin, N. Quentin, B. Allard, C. Buttay, R. Burgos, W. Zhang, D. Boroyevic, P. Preciat, D. Martineau, "2 MHz High-Density Integrated Power Supply for Gate Driver in High-Temperature Applications", in the *Applied Power Electronics Conference (APEC)*, **2016**

- R. Perrin, C. Buttay, B. Allard, C. Martin, "Integrated High-Temperature Isolation barrier with Coreless Transformer", in *Conference on Integrated Power Electronics Systems (CIPS)*, **2016**

- R. Perrin, B. Sun, C. Buttay, B. Allard, N. Quentin, M. Ali, R. Burgos, D. Boroyevich, "Two Comparison-Alternative High Temperature PCB-Embedded Transformer Designs for a 2 W Gate Driver Power Supply", in *Energy Conversion Congress and Expo (ECCE)*, **2016**

- R. Perrin, N. Quentin, C. Martin, C. Joubert, L. Grimaud, B. Lacombe, R. Cellier, "A Single Switch Resonant and Quasi-Resonant Converter Suitable for Low Power Applications", in *Annual Conference on IEEE Industrial Electronics Society (IECON)*, **2016**

Journals

- R. Perrin, B.Allard, C. Martin, M. Ali, “High Temperature GaN Active-Clamp Flyback Converter with Resonant Operation Mode” in the *IEEE Transaction in Power Electronics*, **2016**

- R. Perrin, J. Alles, B. Allard, M. Ali, “High Temperature Current Sensor Solution based on Tunnel Magnetoresistance Effect”, in *Electric Power Systems Research* [accepted]

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- R. Perrin, B. Allard, D. Bergogne, C. Martin, “High-Temperature SOI Driver for GaN Power Module”, in the *European PhD School: Power Electronics, Electrical Machines, Energy Control and Power Systems*, **2014**[Poster]

- B. Allard, G. Clerc, R. Perrin, E. Dumitrescu, R. German, A. Lievre, M. Makdessi, E. Niel, R. Ouaida, “Reliability and Safety Monitoring for more Electrical Transportation”, in the *Automotive Power Electronics Conference (APE)*, **2015**

- B. Allard, R. Perrin, R. Riva, C. Buttay, C. Martin, H. Morel, “Considerations for High Temperature Power Electronics”, in the *18th International Symposium Power Electronics*, **2015**

- N. Quentin, C. Martin, R. Perrin, C. Joubert, “GaN Active-Clamp Flyback converter with resonant operation over a wide input voltage range”, in the *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM)* **2016**

- N. Quentin, C. Martin, R. Perrin, C. Joubert, “A large input voltage range 1 MHz full converter with 95% peak efficiency for aircraft applications”, in the *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM)* **2016**

Abstract

The french industrial project MEGaN targets the development of power module based on GaN HEMT transistors. One of the industrial applications is the aeronautics field with a high-constraint on the galvanic isolation (>100 kV/μs) and ambient temperature (200°C). The intent of this work is the power module block (3 phases inverter 650 V 30 A). The goal is to obtain a small footprint module, 30 cm^2, with necessary functions such as gate driver, gate driver power supply, bulk capacitor and current phase sensor. This goal implies high efficiency as well as respect of the constraint of galvanic isolation with an optimized volume.

This dissertation, besides the state of the art of power modules and especially the GaN HEMT ones, addressed a control signal isolation solution based on coreless transformers. Different prototypes based on coreless transformers were characterized and verified over 3000 hours in order to evaluate their robustness.

The different studies realized the characterization of the different market available GaN HEMTs in order to mature a circuit simulation model for various converter topologies. In the collaborative work of the project, our contribution did not focus on the gate driver chip design even if experimental evaluation work was made, but a gate driver power supply strategy.

The first gate driver isolated power supply design proposition focused on the low-voltage GaN HEMT conversion. The active-clamp Flyback topology allows to have the best trade-off between the GaN transistors and the isolation constraint of the transformer. Different transformer topolgies were experimentally performed and a novel PCB embedded transformer process was proposed with high-temperature capability. A lamination process was proposed for its cost-efficiency and for the reliability of the prototype (1000 H cycling test between - 55; + 200°C), with 88 % intrinsic efficiency. However, the transformer isolation capacitance was drastically reduced compared to the previous prototypes. 2 high-integrated gate driver power supply prototypes were designed

with: GaN transistors (2.4 MHz, 2 W, 74 %, 6 cm^2), and with a CMOS SOI dedicated chip (1.2 MHz, 2 W, 77 %, 8.5 cm^2).
In the last chapter, this dissertation presents an easily integrated solution for a phase current sensor based on the magnetoresistance component. The comparison between shunt resistor and magnetoresistance is experimentally performed. Finally, two inverter prototypes are presented, with one multi-level gate driver dedicated for GaN HEMT showing small switching loss performance.

Résumé

Le projet industriel français MEGaN vise le développement de module de puissance à base de compostant HEMT en GaN. Une des application industrielle concerne l'aéronautique avec une forte contrainte en isolation galvanique (>100 kV/μs) et en température ambiante (200°C). Le travail de thèse a été concentré sur une brique module de puissance (bras d'onduleur 650 V 30 A). L'objectif est d'atteindre un prototype de facteur de forme peu épais, 30 cm^2 et embarquant l'ensemble des fonctions driver, alimentation de driver, la capacité de bus et capteur de courant phase. Cet objectif implique un fort rendement énergétique, et le respect de l'isolation galvanique alors que la contrainte en surface est forte.

Le manuscrit, outre l'état de l'art relatif au module de puissance et notamment celui à base de transistor GaN HEMT, aborde une solution d'isolation de signaux de commande à base de micro-transformateur. Des prototypes de micro-transformateur ont été caractérisés et vieillis pendant 3000 H pour évaluer la robustesse de la solution.

Les travaux ont contribué à la caractérisation de plusieurs composants GaN afin de mûrir des modèles pour la simulation circuit de topologie de convertisseur. Au sein du travail collaboratif MEGaN, notre contribution ne concernait pas la conception du circuit intégré (driver de grille), tout en ayant participé à la validation des spécifications, mais une stratégie d'alimentation du driver de grille.

Une première proposition d'alimentation isolée pour le driver de grille a privilégié l'utilisation de composants GaN basse-tension. La topologie Flyback résonante avec clamp permet de tirer le meilleur parti de ces composants GaN mais pose la contrainte du transformateur de puissance. Plusieurs technologies pour la réalisation du transformateur ont été validées expérimentalement et notamment une proposition originale enfouissement du composant magnétique au sein d'un substrat polymère haute-température. En particulier, un procédé de fabrication peu onéreux permet d'obtenir un dispositif fiable (1000

H de cyclage entre - 55 ; + 200°C), avec un rendement intrinsèque de 88 % pour 2 W transférés. La capacité parasite d'isolation est réduite par rapport aux prototypes précédent. Deux prototypes d'alimentations à forte intégration utilisent soit les transistors GaN basse tension (2.4 MHz, 2 W, 74 %, 6 cm^2), soit un circuit intégré dédié en technologie CMOS SOI, conçu pour l'application (1.2 MHz, 2 W, 77 %, 8.5 cm^2).
Le manuscrit propose par la suite une solution intégrable de mesure de courant de phase du bras de pont, basé sur une magnétorésistance. La comparaison expérimentale vis à vis d'une solution à résistance de shunt. Enfin, deux prototypes de convertisseur sont décrit, dont une a pu faire l'objet d'une validation expérimentale démontrant des pertes en commutation réduites.

Résumé étendu en Français

Introduction

L'avion plus électrique est une des solutions envisagées pour contribuer à la réduction de la consommation des énergies fossiles, de l'empreinte énergétique et des émissions de CO_2. Le remplacement des actionneurs mécaniques ou pneumatiques par des actionneurs électrique type HMA-EMA a permis une réduction de la masse de l'avion ainsi qu'une maintenance facilité. La **??** permet de voir l'augmentation de la puissance électrique embarquée au sein de différents avions. La progression est notable ses derniers années du au fait de l'augmentation du prix du pétrole et de la demande de plus en plus forte pour des transports moins polluants.

Dans cet objectif les composants à grand gap tel que les MOSFET SIC ou les HEMT GaN trouvent une place de choix. Leurs caractéristiques statiques et dynamiques ont permis et vont permettre une réduction du volume des convertisseurs avec une plus grande étendue de fonctionnement en température. Les convertisseurs que se soit pour la commande moteur ou le transfert d'énergie, se concentrent autour de bus 1200 V. Les transistors en GaN avec des caractéristiques intrinsèques dépassant les meilleurs composants de puissance du marché sont une solution très attractive.

Le projet français MEGaN a pour objectif la création d'une filière industrielle autour des composants GaN de la création du composant à sont utilisation finale dans des systèmes de conversion. Il rassemble autour de ce projet commun, industrielles et laboratoire académique avec une forte interaction entre les différents partenaires pour arriver un produit optimal.

Ma thèse se rattache à deux Work-Package, WP3 et WP6 qui correspondent au développement d'un composant de commande de grille adapté aux composants GaN. Mon objectif a été de participer aux spécifications du composant mais surtout de crée le circuit qui allait l'accueillir. Une caractérisation des composants GaN HEMT produit par le CEA-Leti a permis de spécifier au mieux le composant de commande. La vitesse de commutation élevée des composants GaN et son impact sur le circuit a été étudié afin de proposer des solutions innovantes et adapté. Notamment un travail particulier a été fournis avec pour objectif l'immunité aux rapides dV/dt générés par les GaN HEMT. Le manuscrit de thèse s'organise en 5 chapitres comme détaillé ci-dessous et reflète la vision globale de ces travaux sur la conversion de puissance basé sur les composants grand gap en GaN.

Le chapitre 1 décrit les caractéristiques statiques et dynamiques du transistor à hétéro-jonction en matériau GaN. Une modélisation du comportement est décrite pour alimenter des simulations circuit. Le chapitre 2 décrit une solution d'isolation galvanique de signaux de commande bas-niveau. Le transformateur sans matériau magnétique est caractérisé notamment en température et l'immunité aux dV/dt évaluée expérimentalement à l'aide d'un générateur construit dans ce but. Le chapitre 3 concerne l'alimentation électrique du circuit de commande de grille du transistor de puissance. Le verrou principal concerne l'immunité aux dV/dt avec la proposition d'un transformateur à matériau magnétique enfoui. Le chapitre 4 détaille d'autres verrous concernant la mesure de courant ou une topologie de commande locale de grille à 4 niveaux de tension. Une commande locale de grille de transistor est proposée sur circuit imprimé haute température. Le chapitre 5 résume les contributions de la thèse et discute les principales perspectives.

Chapitre 1: Composants en Nitrure de Gallium

Comme démontré dans la Figure 1.1 les composants en Nitrure de Gallium possèdent des caractéristiques intrinsèques supérieures aux composants en Silicium. Notamment ils présentent un bon comportement en haute-tension et à haute-fréquence, essentiel pour un meilleur rendement des convertisseurs. Les figures de mérites ou FoM montrés dans la Table 1.2 mettent exergues ces deux caractéristiques face aux autres matériaux du marché.

Cependant le GaN étant un composant en développement et présentant une maturité faible, sa présence sur le marché des composants de puissance reste faible. Il est dont intéressant de regarder comment ce nouveau matériau est entrain de s'insérer dans le marché actuel. La Figure 1.6 montre que le GaN est actuellement présent sur une catégorie que nous pouvons appeler basse-tension, un second marché plus haute tension (600 V) est entrain d'émerger, c'est ce que vise le projet MEGaN.

Afin d'avoir une meilleure connaissance de ces nouveaux composants, il a été nécessaire de réaliser à la fois des caractéristiques statiques et dynamiques sur des composants du projet et des échantillons commerciaux. Deux types de composants GaN existent, les composants de type cascodé et de type "enhancement". Les deux structures se différencient par des modes et des structures différentes qui sont décris dans ce manuscrit. Nous avons donc sélectionnés des solutions existantes du marché avec ces deux types de structure pour réaliser les différentes caractérisations. La résistance à l'état passant et la tension de seuil ont été deux point essentiels, mesurés entre 25 et 200°C en mode statique.

Pour la caractérisation dynamique un banc de type double impulsions a été réalisé comme montré en Figure 1.25. L'évaluation des pertes en commutations pour différentes tensions et courant de drain a été réalisée entre 25 et 200°C. Les composants de types cascodés, ils présentes une résistance à l'état passant plus élevés mais ont une grande stabilité des pertes en commutation en température. Quant aux composants de types "enhancement", ils présentent une grande stabilité de la tension de seuil en température avec une résistance à l'état passant plus faible. Leur comportement en commutations se caractérise par une augmentation des pertes en température.

Dans le but d'une amélioration des modèles de simulation de composant existant, des pistes sont proposées. Notamment, le comportement des composants de types "enhancement" lors de la commutation à l'état On a été étudié et la mise en équation du comportement a permis d'améliorer le modèle existant. Figure 1.38 et Figure 1.39 montrent après correction du modèle une bonne correspondance entre simulation et expérimentation.

Chapitre 2: Isolation à base de transformateur à air

L'isolation des signaux de commande est un enjeu propre aux solutions de conversion isolées comme le montre la Figure 2.2. L'isolation doit permettre de transmettre les signaux de commande vers le circuit de commande de grille. Dans cette optique, le laboratoire Ampère a développé une solution de transformateur à air sur un substrat de verre en partenariat avec ST Microéléctronique comme montré en Figure 2.12. Ses faibles dimensions en font une solution attractive pour l'intégration dans un système à faible volume. De plus le substrat de verre lui confère une tenue en température élevée se qui correspond au besoin des application aéronautique.

Une première étape a été la caractérisation de la solution d'isolation en température. Un premier test de vieillissement a été réalisé pendant 3000 H. Ce premier test a montré un problème d'oxydation de la structure des enroulements du transformateur. Cependant une solution avec une couche de Parylène déposé en surface du transformateur a permis de réduire les interactions entre l'air et la structure. La stabilité de la structure a été démontrée durant 3000 H avec une couche de Parylene en mesurant la variation de la

capacité entre primaire et secondaire comme montré en Figure 2.16.
Dans un second temps, la solution a été testée dans un système complet montré en Figure 2.18, composé d'un émetteur pour la modulation de la trame à 25 MHz afin d'envoyer la donnée à travers le transformateur et d'un récepteur pour démoduler la trame. La solution développée, avait pour objectif une application à 200°C, il a été donc forcé d'utiliser des émetteurs/récepteurs en technologie SOI CMOS de chez EasiiC XREL avec une tenue en température maximum de 250°C. La solution a été également testée durant 600 H pour vérifier que les caractéristiques du transformateur n'affectaient pas la stabilité du transfert du signal. Les résultats ont montrés une remarquable stabilité et validé le composant.
Comme nous l'avons vu les composants de puissance en GaN sont capables de vitesse de commutation 4 fois supérieur au Silicium. De ce fait, l'immunité de la solution d'isolation a du être caractérisé en dynamique. Un générateur de dV/dt a été construit basé sur un composant bien connu, un tube à éclateur à gaz en Figure 2.21. Le système est capable de délivrer des vitesses de commutation à haute-tension entre 20 $kV/\mu s$ et 150 $kV/\mu s$ grâce à une résistance variable. Le système a été connecté à différent systèmes d'isolation du commerce comme l'opto-coupleur et avec la solution coreless afin de définir des limites maximum d'utilisation en dV/dt. La solution coreless a pu être caractérisée avec une limite en dV/dt à 65 $kV/\mu s$ se qui en fait une solution viable pour des systèmes de conversion en GaN.
En Figure 2.32 une modélisation simple d'une structure d'isolation de signaux a été proposée basé sur les résultats expérimentaux du générateurs de dV/dt et montre une bonne corrélation avec l'expérimental.

Chapitre 3: Alimentation électrique du circuit de commande de grille

L'isolation galvanique ne se limite pas uniquement aux signaux de commande mais également à l'alimentation du composant de commande de grille. Des problématiques similaires s'appliquent à l'isolation de l'alimentation de puissance. Dans un convertisseur isolé, la puissance est transmise à travers un transformateur.
Dans cette thèse, le travail a été axé sur la réduction du volume du convertisseur. Afin d'avoir un grande immunité aux dV/dt une géométrie de transformateur originale a été proposée en Figure 3.34. La géométrie appelée transformateur coplanaire donne une solution avec une capacité parasite la plus faible du marché avec une valeur de 0.9 pF. Cependant cette structure présente une grande inductance de fuite non compatible avec certaines topolo-

gies de convertisseur.

La montée en fréquence de commutation est aussi un point important pour la réduction de la taille des passifs tel que le transformateur comme montré en Figure 3.2. Une topologie basée sur une Flyback à clamp actif est proposée avec un mode résonant, ce qui lui permet de réaliser une commutation à zéro de tension et de courant sur les éléments actifs, celle-ci est détaillée en Figure 3.19. Les pertes en commutations se retrouvent quasi nulle et permettent des fréquences de commutation de l'ordre de 2 MHz dans notre cas. La forte inductance de fuite est utilisée dans la résonance avec la capacité de clamp et permet l'utilisation de ce type de transformateur sans contrainte. Un premier prototype discret en Figure 3.53, a été réalisé basé sur des transistors GaN et a démontré un rendement de 74% à 3 W et 800 kHz. Ce prototype a démontré une réduction de volume par 4 par rapport a un prototype Flyback équivalent commutant à 200 kHz.

Dans un deuxième temps, un travail a été axé sur l'intégration du transformateur pour une réduction plus forte du volume. L'étude bibliographique a démontré l'avantage du matériau PCB comme substrat pour son faible prix et sa forte diversité dans le monde industriel en Table 3.6. Une première étape a été la mise au point d'un procédé de lamination du PCB avec des éléments magnétiques en son sein détaillé en Figure 3.40. Le procédé a été mis au point avec un PCB Panasonic présentant une très faible déformation mécanique en température pour réduire le stress mécanique sur les ferrites. Un premier prototype avec un transformateur pour une solution de convertisseur à 2.2 MHz a été réalisé avec succès. Un vieillissement comparatif, par cyclage thermique entre -55 et 200°C, entre le PCB Panasonic et le FR4 a été réalisé et a démontré la grande stabilité du PCB Panasonic en température durant 1000 cycles en Figure 3.51. Un convertisseur complet a été réalisé basé sur des GaN EPC avec un rendement de 65% à 2.2 MHz et 3 W comme montré en Figure 3.63.

La dernière étape de cette étude a été la spécification d'une puce en SOI CMOS pour intégré la partie active du convertisseur et avoir un fonction capable de tenir les 200°C. Ce travail a été réalisé conjointement avec EasiiC Xrel. La fonction intègre le contrôleur PWM, des fonctions de sécurité comme une fonction de soft-start et de limitation en courant, les deux composants de commande de grille ainsi que les deux MOSFET SOI. Un dernier prototype 3 W avec puce SOI en surface et une fréquence de découpage de 1.2 MHz a démontré un rendement de 76% et une grande stabilité de la tension de sortie comme montré en Figure 3.63.

Enfin un prototype de convertisseur Buck isolé détaillé en Figure 3.67, a été réalisé pour démontrer l'avantage d'avoir un fonction de régulation pour avoir une stabilité de la tension de sortie en température et en fonction de la charge.

Chapitre 4: Problématique d'intégration dans un module de puissance

Dans ce dernier chapitre est abordé la problématique d'intégration des différents éléments d'un convertisseur dans un module de puissance. En effet, la possibilité offerte par les composants grand-gap comme le GaN permet d'avoir des architectures et des assemblages de plus en plus complexe pour avoir un faible volume.

Dans cette optique, une solution de mesure de courant, essentiel pour le contrôle du convertisseur, basé sur une magnétorésistance a été démontrée en **??**. La mesure de courant est l'un des éléments les plus difficilement intégrable, du fait des solutions du marché isolé ou shunt qui ont des volumes important. La magnétorésistance tunnel a l'avantage de proposer une mesure du champ électrique de façon isolé avec la taille d'un composant CMS.

Une étude de différentes solutions du marché a été faite pour identifier les meilleures caractéristiques. Une TMR a été sélectionnée et une étude en température et en courant a permis d'identifier les différents coefficients de variation de la puce. Le comportement très linéaire de la magnétorésistance pour chaque point de température est très encourageant comme montré en Figure 4.15. La solution complète a été implémenté dans une mesure de courant pic à 30 A dans le bras du convertisseur et a démontré de bonne performance.

Afin de traiter la problématique des composants en GaN au niveau du composant de commande, une méthode de commande de grille multi-niveaux a été proposée en Figure 4.25. La commande multi-niveaux a l'avantage de tirer le meilleur parti des composants GaN HEMT en accélérant les vitesses de commutations et en réduisant l'effet de "crosstalk" dans le bras. L'accélération des temps de commutation se fait par une injection de courant de grille plus important afin de charger et décharger plus rapidement la capacité de grille. Comme montré en Figure 4.27, les pertes en commutations s'en trouvent réduites de 30%.

L'effet dit "crosstalk" dans un bras d'onduleur peut causer la reconduction des transistors et court-circuiter le bras. Afin d'éliminer cet effet, la commande multi-niveaux appliques une tension négative sur la grille. Cependant les pertes en conduction sont augmentées mais le bilan des pertes globales restes amélioré.

Un modèle de perte simple est proposé afin d'évaluer les avantages de la solution pour différentes puissances. En Figure 4.39, le modèle donne une bonne correspondance avec la réalité expérimentale.

Conclusions et Perspectives

Cette thèse c'est concentré sur l'étude de l'impact de la monter en fréquence d'un convertisseur de type onduleur avec des composants de type GaN HEMT. Différentes solutions ont été proposés pour résoudre les problématiques rencontrés.

La caractérisation des composants GaN a été réalisée en dynamique et en statique jusqu'à 200°C. Les résultats pour chaque type de structure ont été discutés.

Une solution d'isolation des signaux de commandes haute-température basée sur une technologie de transformateur à air sur substrat de verre. Un traitement au Parylène a permis de valider cette solution sur le long terme. L'immunité au dV/dt a pu être étudié expérimentalement avec un générateur de dV/dt et un modèle simple a été proposé.

Une convertisseur de type POL 3 W a destination de l'alimentation du composant de commande a été proposé. Il se démarque par son faible volume, sa puce SOI CMOS pour un fonctionnement jusqu'à 200°C et son immunité au fort dV/dt. Pour cela un procédé d'assemblage a été développé pour l'intégration du transformateur dans un substrat PCB. Une puce SOI CMOS intégrant les fonctions de protections de commandes et de puissance a été spécifiée et testée avec succès. Pour finir une topologie de type Flyback à clamp actif avec un mode résonant a permis une monté en fréquence jusqu'à 2.2 MHz.

Enfin le composant de commande et son module de puissance ont été étudiés et une solution de mesure de courant à base de magnétorésistance a été proposée. Cette solution de mesure de courant de type isolé permet de solutionner les solutions existantes trop volumineuses pour être intégrable. Un type de commande de grille multi-niveaux a permis également de proposer une solution intermédiaire entre pertes en commutations et rapide fréquence de commutations.

De ce travail ressort une vue globale de l'optimisation en volume d'un convertisseur de type onduleur. Les différentes approches pour la réduction du volume, que se soit de l'assemblage, sur la topologie circuit ou le choix de commande a permis une optimisation globale. L'immunité aux dV/dt a été particulièrement traitée ainsi que le développement de modèle simples pour l'amélioration de la simulation. Cependant, pour les composants en GaN, deux points sont a améliorés pour avoir des modèles précis. La modélisation des effets de résistance passante dynamique et le comportement à l'état bloqué sont a étudiés et a modélisés.

L'augmentation des vitesses de commutation va également de paire avec une augmentation du bruit électrique CEM. Ce point n'a pas été traité dans cette thèse et devra faire le cas d'une attention particulière dans le développent de convertisseurs en GaN. Pour finir afin d'adresser au mieux le GaN HEMT en température une solution de puce en SOI CMOS au plus proche du composant de puissance permettra de profiter pleinement des avantages de ce matériau.

Chapter 1

Characterization and Modeling of 600 V E-GaN HEMTs

Contents

This chapter presents a comparative overview of Wide Band Gap (WBG) devices with a focus on the Gallium Nitride (GaN) based devices. A static and a dynamic characterization of the two main types of GaN devices is performed with a focus on their high-temperature capability. The analysis of the switching behavior of the enhancement device is made and a specific model is developed for modeling the Miller effect. Both simulation and experimental results are presented and compared in order to improve the model.

1.1 Wide Bandgap semiconductors materials

Wide band gap power semiconductor devices have proven to be a milestone in the development of the power conversion field. In a semiconductor crystal if a covalent bond is broken and an electron is excited into the conduction band, it leaves behind a unbalanced charge (positive charge in ine the case of a hole). In Figure 1.2 a simplified energy band diagram is shown. The top band is called the conduction band E_c and the bottom one is called the valence band E_v. Between E_c and E_v is the forbidden band where no charge exist ideally. In order to move from the valence band to the conduction band, the electrons need an amount of energy proportional to $E_g = E_c - E_v$, where E_g is the bandgap.

One emerging WBG material, GaN, with the High Electron Mobility Transistor (HEMT) structure is a promising good candidate to achieve high-frequency and high power density conversion. As shown in Figure 1.1, WBG devices such as Silicon Carbide (SiC) or GaN present clear advantages compare to classic Silicon (Si) power devices..

To be considered as a WBG semiconductor the material has to have a band gap larger than the Si one, $1.12eV$. GaN and SiC have a bandgap 3 times larger than Si. According to Table 1.1, it is obvious than the diamond material is best one but the process does not allow the commercialization of

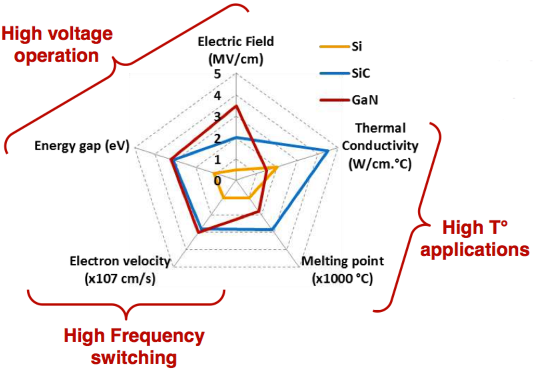


Figure 1.1 – Comparison of SiC and GaN devices against Si for Power applications [189].

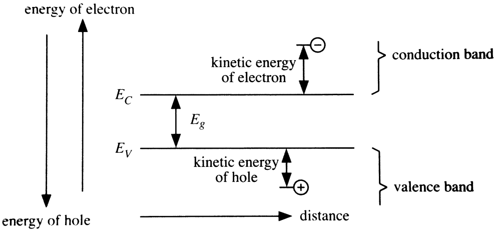


Figure 1.2 – Band diagram after an atom has been ionized [119].

this material yet. WBG materials in general and specifically GaN and SiC materials present better physical characteristics :

- WBG materials presents higher breakdown voltages because of their higher electric breakdown field (E_c), which means that for a similar thickness, the breakdown will be higher than for Si, this point is graphically represented in Figure 1.3;
- The combination of E_g and the thermal conductivity λ, increases the thermal capability of the components by increasing the heat transfer. From a system point of view this advantage helps to decrease cooling system and volume of conversion system, this point is graphically represented in Figure 1.4;
- The relative permittivity ϵ is smaller for the WBG materials and helps to realize smaller intrinsic capacitance as well as a bigger saturation velocity v_{SAT}. With a reduced capacitance , the switching speed can be increased and the conversion system volume decreases, as a consequence of the reduction of the passive components around;

Although WBG semiconductor presents undeniable advantages, the low maturity of those technology compare to Si, does not allow us to fully enjoy each points, due to accessibility and higher cost limitation.

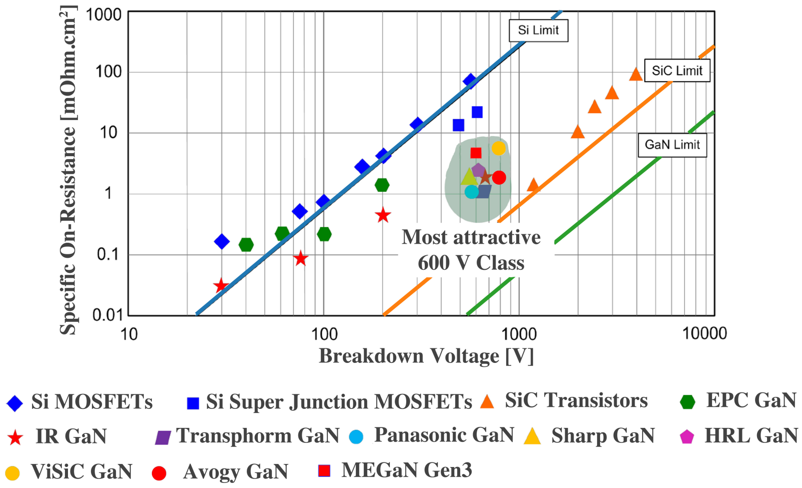


Figure 1.3 – Specific On-resistance vs. breakdown voltage for commercially SI, SiC and GaN devices [122]

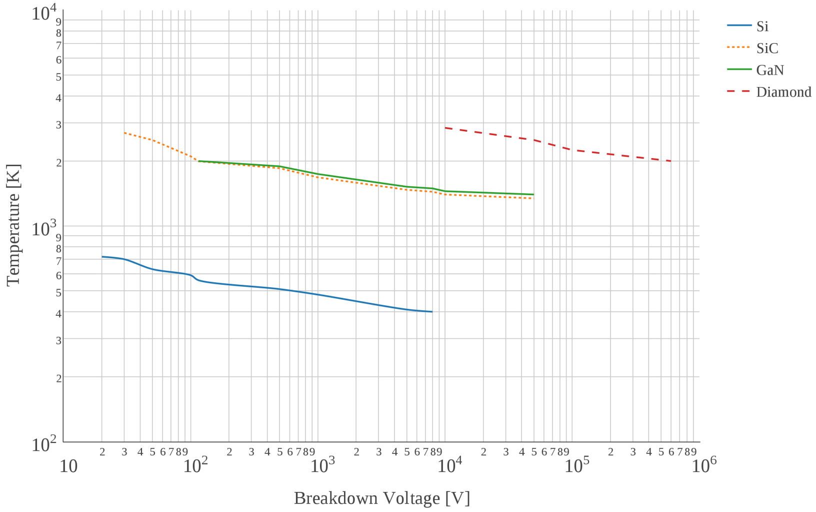


Figure 1.4 – Limited operation temperature for different semiconductor materials [177].

Table 1.1 – Physical properties of the principal semiconductor materials at 300 K.

	Eg	μ_n	μ_p	v_{SAT}	E_c	λ	ϵ
Si	1.12	1450	450	10^7	$3 * 10^5$	1.3	11.7
GaAs	1.4	8500	400	$2 * 10^7$	$5 * 10^5$	0.54	12.9
3C-SiC	2.3	1000	45	$2.5 * 10^7$	$2 * 10^5$	5	9.6
6H-SiC	2.9	415	90	$2 * 10^7$	$2.5 * 10^5$	5	9.7
4H-SiC	3.2	950	115	$2 * 10^7$	$3 * 10^5$	5	10
GaN	3.39	1000	150	$2 * 10^7$	$5 * 10^5$	1.3	8.9
GaP	2.26	250	100	$2 * 10^7$	10^7	1.1	11.1
C	5.6	2200	1800	$3 * 10^7$	$5.6 * 10^7$	20	5.7

It is also really interesting to take a look to the different Figure of Merit (FoM) in Table 1.2, which allows to have a comparative factor between the different semiconductor materials. The Baliga factor ($BFM_{Si/GaN} = 187$), shows the trade-off between on-state voltage and the maximum breakdown voltage. With a factor 187 times higher than the Si, we can conclude than

Variable	Unit	Variable	Unit
Eg	$[eV]$	E_c	$[V/cm]$
μ_n	$[cm^2/V.s]$	λ	$[W/cm.K^{-1}]$
μ_p	$[cm^2/V.s]$	ϵ	$[F.m^{-1}]$
v_{SAT}	$[cm/s]$	-	-

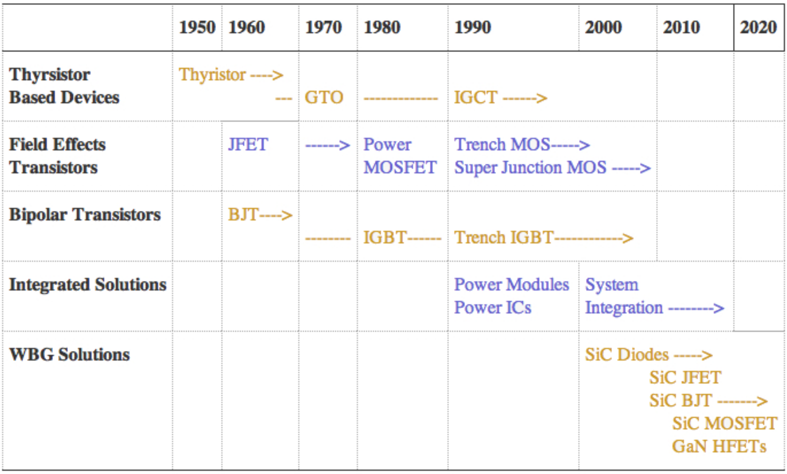
GaN will offer a better On-resistance for a same drain voltage, and a better heat transfer capability. To conclude Si and GaAs have quite poor performances, SiC and GaN with similar figures of merit, hence similar performances, offer strong capabilities, and diamond has at least 40 times better figures of merit than the other semiconductors.

Table 1.2 – Main figures of merit for WBG semiconductors [158].

	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Generic Criteria						
JFM	1	1.8	277.8	215.1	215.1	81000
BFM	1	14.8	125.3	223.1	186.7	25106
Unipolar Components Criteria						
FSFM	1	11.4	30.5	61.2	65	3595
FPFM	1	3.6	48.3	56	30.4	1476
FTFM	1	40.7	1470.5	3424.8	1973.6	5304459
Bipolar Components Criteria						
BSFM	1	1.6	13.1	12.9	52.5	2402
BPFM	1	0.9	57.3	35.4	10.7	594
BTFM	1	1.4	748.9	458.1	560.5	1426711

Commercialization of WBG power devices started with the SiC diodes in early 2000. Today 1200 V SiC MOSFETs are the common rated transistors, with a vertical structure as Si MOSFETs. Table Figure 1.5 shows the different steps of the semiconductor market evolution. The classic Thyristor was the first one in 1950's, and quickly replaced by the IGBT, MOSFET and JFET structures. Currently, WBG devices are the last introduced power devices with ever higher performances. Figure Figure 1.6 shows some ratings of commercial and labscale power devices. We can notice two tendencies, the first one is a clear interest for 10 kV SiC product. SiC was preliminary focus on 1200 V

JFM	Johnson's figure of merit, a measure of the ultimate high-frequency capability of the material.
BFM	Baliga's figure of merit, a measure of the specific on-resistance of the drift region of a vertical field effect transistor (FET)
FSFM	FET switching speed figure of merit
BSFM	Bipolar switching speed figure of merit
FPFM	FET power-handling-capacity figure of merit
FTFM	FET power-switching product
BPFM	Bipolar power handling capacity figure of merit
BTFM	Bipolar power switching product



	1950	1960	1970	1980	1990	2000	2010	2020
Thyristor Based Devices	Thyristor ---->	---	GTO	-------------	IGCT ------>			
Field Effects Transistors		JFET	------>	Power MOSFET	Trench MOS-----> Super Junction MOS ----->			
Bipolar Transistors		BJT---->	--------	IGBT------	Trench IGBT------------>			
Integrated Solutions					Power Modules Power ICs	System Integration -------->		
WBG Solutions						SiC Diodes ----->	SiC JFET SiC BJT -------> SiC MOSFET GaN HFETs	

Figure 1.5 – Timeline of the development of the power semiconductor [100].

and now a clear increase of the maximum voltage is requested. The second tendency acknowledges that GaN addresses a premature market, so it is staying on "low voltage" area between 600 V for the commercial products and with some research on 1200 V.

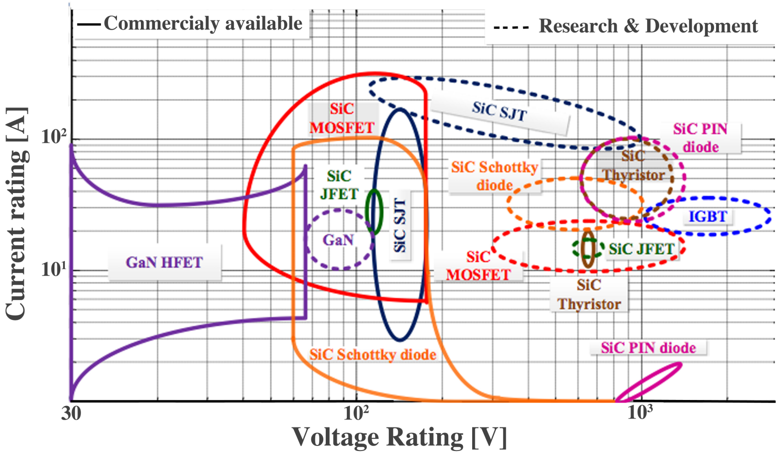


Figure 1.6 – Rating of selected research and commercial power devices [250].

1.2 GaN Power devices

To target competitive power electronics devices, GaN is grown on Si substrate in the majority of the commercial devices. Other more efficient substrate as SiC or Sapphire have been used too but with higher development cost [78]. To make GaN growth on 6 inch and 8 inch Si wafer [29] is a challenge, with a difficult trade-off to find between breakdown voltage, GaN thickness and current collapse, but that allows to use conventional Si fabrication structure. The reliability issues are not developed in this dissertation, but some works [105] have been already done on the different degradation mechanisms such as hot electron damage, inverse piezoelectric effect....

1.2.1 GaN Rectifier

Commonly, power device development starts with the tuning of the diode process. The reason is that the diode structure is the simplest one and allows to address the problems related to the new material. Diodes are also mandatory devices in converter topologies.

There is three main diode structures:

- The Schottky Barrier Diode (SBD) is presented in Figure 1.7(a). The SBD structure allows a really low On-state losses and fast switching by the simplicity of the two N^+ and N^- doped elements.

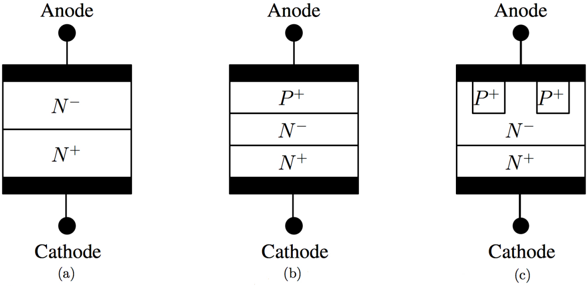


Figure 1.7 – Main diode structures.

- The PIN diode in Figure 1.7(b), is mainly used for high voltage application because of its high blocking voltage. The high reverse recovery phenomena in this diode is the main drawback.

- The Junction Barrier Schottky (JBS) in Figure 1.7(c), is a mix between the two previous structures in order to have the common advantage of those both structures.

The first GaN structures proposed in the literature were lateral or quasi vertical structures to avoid the poor electric conductivity of the GaN substrate [216]. The attractiveness of the GaN diodes comes from the Si and Sapphire substrate which enables development using standard microelectronics resources. More recently, some 4 kV vertical GaN PIN diode structures appeared in literature [152, 109]. Some important improvements are also made on the contact resistance to implement P-type GaN (requested in the PIN structure) as in [59] with a 2.6 kV bilayer PIN diode.

In Figure 1.8 the state of the art is presented for the best results for GaN diodes. From Figure 1.3, we can see that the different prototypes presented in this graphics are really close to the GaN theoretical limit. This maturity comes from the simplicity of the rectifier comparatively to a complex structure as a transistors.

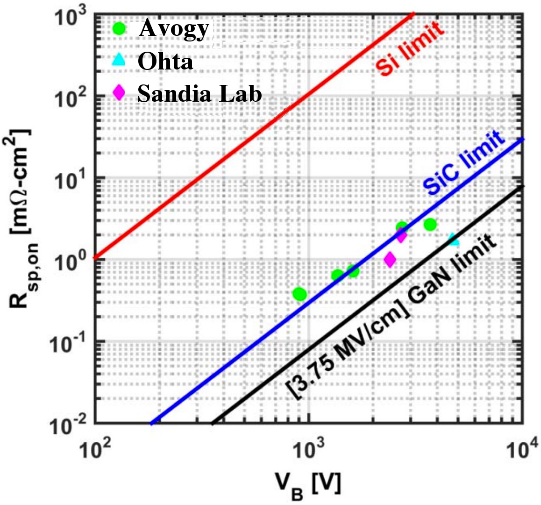


Figure 1.8 – Baliga figure of merit for GaN diodes state of the art (Sandia lab: [59]; Ohta: [152]; Avogy: [108]).

1.2.2 The lateral GaN power device

GaN power devices can be categorized in two modes, either Enhancement mode (E-Mode) or Depletion mode (D-Mode). The difference between structures is the positive threshold voltage for the E-mode and the negative voltage for the D-mode required for turning-Off the component. The structure used in this work is known as a HEMT or lateral High Field Efect Transistor (HFET). The common voltage rating is around 600-650 V and the only one commercialize currently.

Figure 1.9 shows a basic structure of a lateral GaN. The most important part is the interface AlGaN/GaN. A piezoelectric crystal strain created at this interfaceand a two-dimensional electron gas (2DEG) appears. It is this 2DEG channel which can be modulated by the gate.

The substrate, for a cost reason, is usually in Silicon but it can be in SiC or sapphire. On the top of the substrate a layer called buffer, made with different GaN based materials, allows the growth of the GaN layer on a compatible material layer.

One of the drawback of the 2DEG gas, is that the HEMT is intrinsically normally-On. Different structures have been proposed in order to have a normally-Off device.

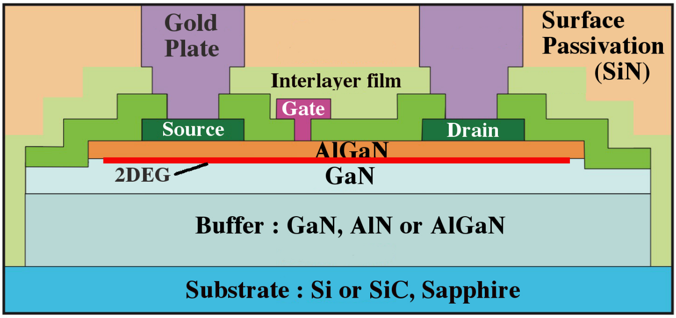


Figure 1.9 – Cross-section of a basic lateral GaN HEMT or HFET structure [91].

1.2.2.1 Depletion Mode GaN devices in a cascode structure

The cascode structure is illustrated in Figure 1.10 a), three components compose the structure. The power diode and the low-voltage Si MOSFET (30 V) are connected with the depletion-mode HEMT in a same package. The drain and source of the Si MOSFET are connected to the gate and source of the HEMT, thereby the MOSFET gate determines the gate maximum voltage through its drain voltage.

The wire bonding which connect the different chips inside the package also means that the switching performance of the device is really dependent of the parasitic inductance. The switching losses can be also affected drastically by the junction capacitance of each device. An interesting work about this issue resolves some tricky points [244]. An optimization of the parasitic inductance is made with a stack die assembly package and an external capacitor is added in the package to balance the junction capacitance between the HEMT and the MOSFET.

Table 1.3 – Commercial Cascode GaN Devices.

Manufacturer	$V_{GS_{Max}}$ [V]	$V_{ds_{Max}}$ [V]	$I_{ds_{Max}}$ [A]	R_{ds-On} [mΩ]	Q_g [nC]
Transphorm	±18	600	34	52	19
Infineon	±20	600	10	125	–
MicroGaN	–	600	–	320	–
RFMD	–	650	25	–	19

In order to have a view of the commercial available devices, Table 1.3

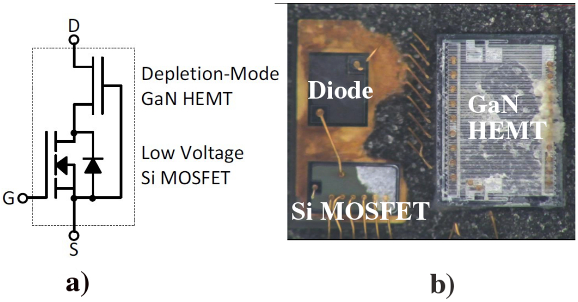


Figure 1.10 – Normally-Off Cascode structure a); Package view of a Transphorm TPH3002PS Cascode GaN, 600 V 17 A b) [22].

presents the current status. Company Transphorm is currently the only one which is selling devices online. As we can notice they are all rated around 600 V and use GaN on Si device with a chip in package assembly.

The comparison between the GaN cascode structure and a similar Si MOSFET, allows to see the improvement of the performances. Two devices with similar breakdown voltage and On-resistance are used to perform the comparison. Table 1.4 shows different static and dynamic parameters. The total gate charge Q_g is smaller with the GaN than with Si, which means smaller driving loss. Smaller E_{oss} means smaller switching loss for the turn-On, smaller Q_{oss} allows smaller resonant time and smaller RMS current in a converter. For the recovery charge Q_{rr}, the difference is huge due to the cascode structure, the depletion GaN HEMT does not have body diode, only the Si MOSFET is

Table 1.4 – Comparison between Cascode GaN vs. Mosfet Si.

Parameter	GaN HEMT	Si MOSFET	Factor
V_{ds}	600 V	600 V	–
R_{ds}	0.15 Ω	0.14 Ω	+6%
Q_g	6.2 nC	75 nC	−91%
Q_{gd}	2.2 nC	38 nC	−94%
E_{oss}	6 uJ	11 uJ	−45%
Q_{oss}	28 nC	130 nC	−78%
Q_{rr}	42 nC	8200 nC	−99%
t_{rr}	24 nC	460 nC	−94%

contributing to the reverse recovery charge.
Those characteristics seem to indicate that the cascode GaN is a good candidate for high-frequency conversion applications. In Figure 1.11 the conduction principle of the cascode GaN is explained and related with the Id-Vd characteristics. When 5 V gate drive voltage is applied, the Si MOSFET is fully enhanced. Since the on-resistance of the Si MOSFET is very small, the gate drive voltage applied on the depletion-mode GaN HEMT is close to zero and the GaN HEMT is fully turned on. In this conduction mode, the current flows through both the channel of the Si MOSFET and the channel of the GaN HEMT, so that the voltage drop equals to Equation (1.1). The current can be bidirectional and it is symmetric in the first quadrant and the third quadrant (as the red curve in Figure 1.11). In this condition, since the on-resistance of the Si MOSFET is much smaller than that of the 600 V GaN HEMT, the total voltage drop is dominaed by the GaN HEMT.

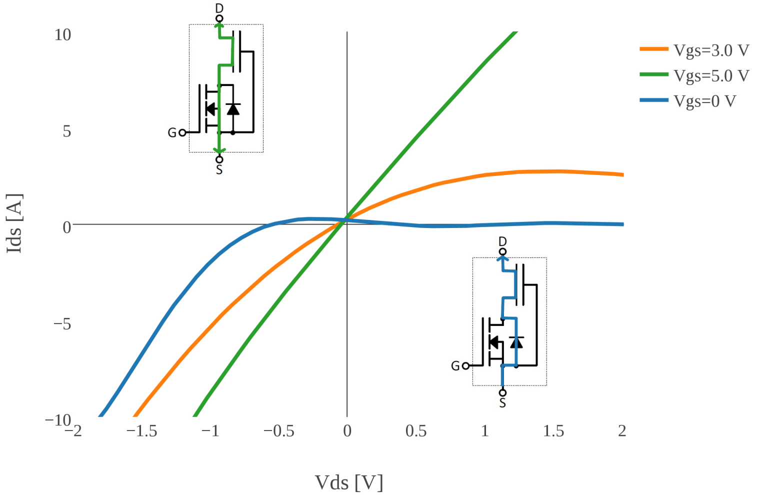


Figure 1.11 – Conduction principle of a cascode GaN HEMT and it is Vd-Id characteristics.

$$V_{ds} = I_{ds} * (R_{ds_{GaN}} + R_{ds_{Si}}) \tag{1.1}$$

When the Si MOSFET is turned off by applying 0 V driving voltage, the cascode GaN HEMT is blocking in the first quadrant while still conducting in the third quadrant. The current first goes through the body diode of the Si MOSFET. Then the gate-to-source voltage of the GaN HEMT equals to the forward voltage of the body diode what makes it turn on. So the current also goes through the channel of the GaN HEMT like shown in Figure 1.11. In reverse conduction mode, the voltage drop equals to Equation (1.2) and is corresponding to the blue curve in Figure 1.11.

$$V_{ds} = I_{sd} * R_{ds_{GaN}} + V_{bd} \tag{1.2}$$

1.2.2.2 Enhancement-Mode GaN devices

As already said before, the HEMT is naturally normally-On. However some modifications on the gate architecture can make the threshold voltage positive, and make a normally-Off device or also called enhancement GaN device.

Table 1.5 – Commercial Enhancement GaN device.

Manufacturer	Vgsmax	VDS	IDS	RdsON	Qg
EPC	6	30	60	1.3	20
		40		1.5	19
		60		2.2	16
		80		2.5	15
		100		3.2	13
		200	9	43	1.8
GaN Systems	10	650	22	73	4.6
			30	55	5.8
			60	27	12
Panasonic	600	12	15	65	11
			10	155	6
HRL	5	1200	10	500	–
		600	10	350	–
Exagan	5	1200	100	–	–
		600	16	–	–

Different technics have been used in industry to customize the gate. Most of the devices commercially available are listed in Table 1.5.

Usually there are three popular gate structures in industry to have normally-off devices: the recessed gate, implanted gate and pGaN gate.In Figure 1.12 figures (a) and (b) show two isolated structures. The first one creates a MISFET inversion layer under the gate in order to connect the 2DEG between the source/gate with the gate/drain one and modulate the channel. The structure (b) is an insulated recessed gate. The gate is etched in the AlGaN layer and an insulation layer is deposed on AlN to have a precise thickness. HRL [52] and now Navitas [2] are using this process in their lateral structures. The structures (a) or (b) can be used by GaN Systems since they are using an insulated gate structure.

Recessed gate is also used by Exagan in some architectures to find the trade-off between high threshold voltage, low On-resistance and no current collapse [29]. EPC GaN devices are using a p-doped GaN gate structure as shown in Figure 1.12 (c). The p-doped layer creates a diode characteristic and the threshold voltage is shifted by the diode voltage drop [116]. In the same way, Panasonic is using AlGaN p-doped gate structure in their Gate Injection Transistors (GITs) [206, 215, 137]. The difference in the materials is modifying the maximum gate voltage allowed: in the EPC case it is around 5 V and only 3 V for the Panasonic. This low gate voltage value is increasing the gate driver design complexity to not break the gate with overvoltage [33].

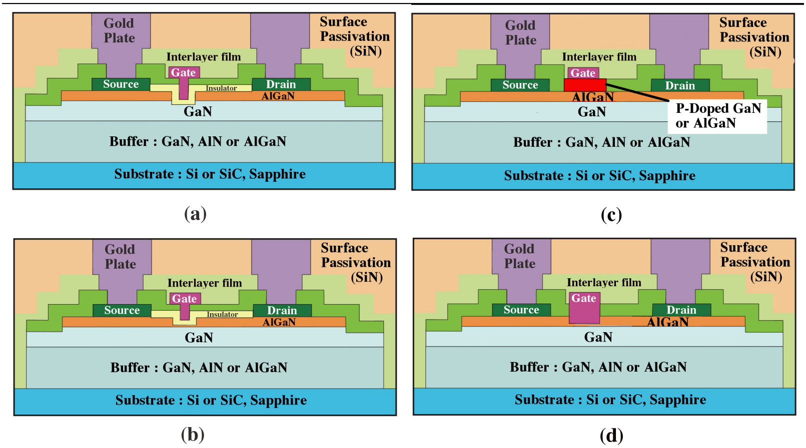


Figure 1.12 – Normally Off device gate structures, MIS-HFET (a), Insulated recessed gate (b), P-doped GaN or AlGaN (c), Recessed gate (d).

1.2.2.3 Dynamic $R_{ds_{On}}$

Among the technological challenges behind GaN transistors, current collapse is one of the most reported one. The current collapse is the name given to the phenomena which increases the On-resistance during the switching time as shown in Figure 1.14.

Two phenomena cause the current collapse. The first one illustrated Figure 1.13, is the trapping of the surface charges close to the gate terminal on the drain side during the off-state. Lateral structure and impurity of the material cause the trap of these charge. During the switching time between Off to On state, these charges are acting as a second gate until they are released. The second phenomenon illustrated in Figure 1.13 is called hot electrons phenomenon : the charges in the channel are trapped in the mismatch in the material structure and cause a degradation of the On-resistance [87]. These phenomena have been shown to be dependent with the junction temperature [20]. Some studies [20, 191] show a pulse method to measure the current

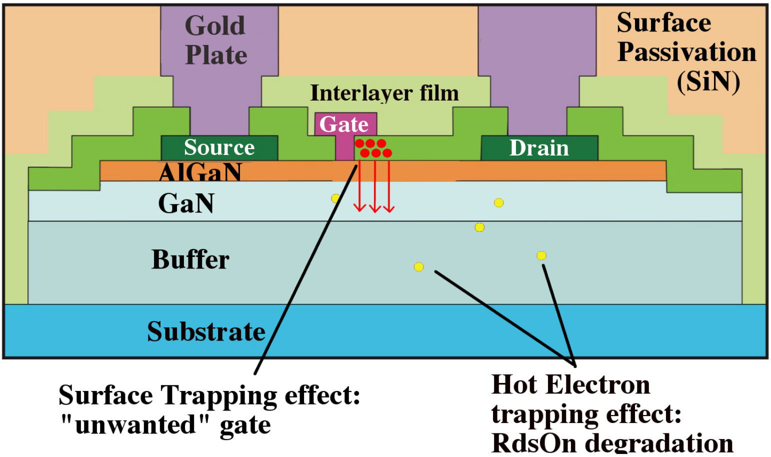


Figure 1.13 – Current collapse phenomena: surface charge trapping and hot electron trapping.

collapse. The difficulties is that the effect is visible during a short time after the switching. Therefore, the measurement system has to be fast and accurate on a large scale because the drain voltage variation is between hundred Volts and few millivolts during the current-collapse effect.

The circuit proposed is an active clamp on the output node of the GaN bridge. The system has to be robust against ringing because the switching with a clamp on the output node adds several parasitic elements. Temperature, drain voltage and current but also switching frequency and duty-cycle have a major influence on the current collapse and cause additional conduction and switching losses. As an example for a normally-Off device with the following characteristics, 600 V 150 $m\Omega$, the On-resistance can grow up to 400 $m\Omega$ during few hundred nanoseconds.

In order to resolve or limit this effect, manufacturers have proposed two main

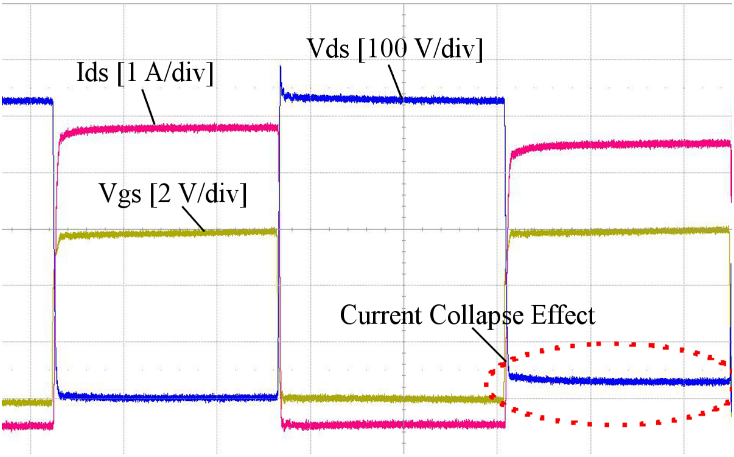


Figure 1.14 – Current collapse effect on drain voltage with a Normally-Off MEGaN HEMT.

architectures. The first one is called field plates as shown in Figure 1.15. Ssome extensions of the gate and the source plates in the device structure allow a better distribution of the field inside the channel. This system allows to remove trapped electrons in the structure by avoiding the usual field concentration on the drain side.

The second architecture is used in the Panasonic devices [102]. The prin-

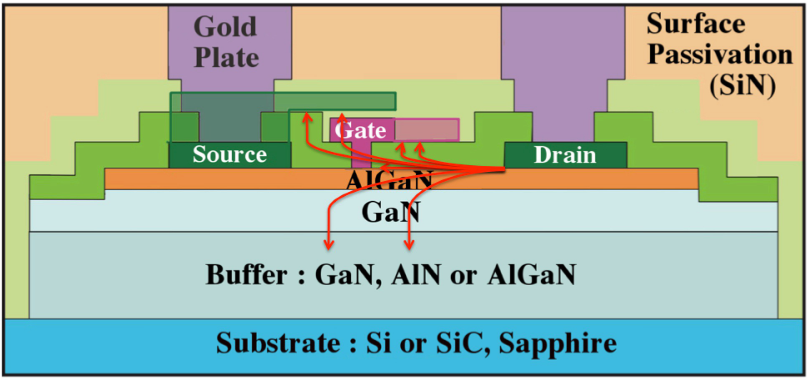


Figure 1.15 – Current collapse limitation by the field plates structure.

ciple of this one is to inject holes in the channel where trapped electrons are recombined. In order to do that an extra P-doped area is placed on the top of the AlGaN layer and connected with the drain. This techniques allow to limit the current collapse by a factor of 1.3 instead of 5 without.

1.2.2.4 Reverse Conduction Mode in GaN devices

GaN devices due to the lateral structure do not have intrinsic body-diode as the Si MOSFET structureHowever there is a reverse conduction capability for cascode and enhancement GaN devices.
In the cascode device case, as discussed before, the Si MOSFET body diode is turning On the channel of the GaN device. Thereby the cascode has a body diode behvior with a lower Q_{rr} than a similar Si MOSFET due to the low voltage Si MOSFET.
In the enhancement GaN device, the symmetry of the lateral structure allows the current to circulate in deletedthe both ways. This effect realizes a conduction in both waysas a body diode effect. When the gate source voltage is going up to the threshold voltage, the device is turned On, and when the drain gate voltage $V_{gd}th$ is reaching the reverse threshold voltage, the device is also turned on.
Equation (1.3) is giving the voltage drop , where $R_{sd}rev$ is the resistance of

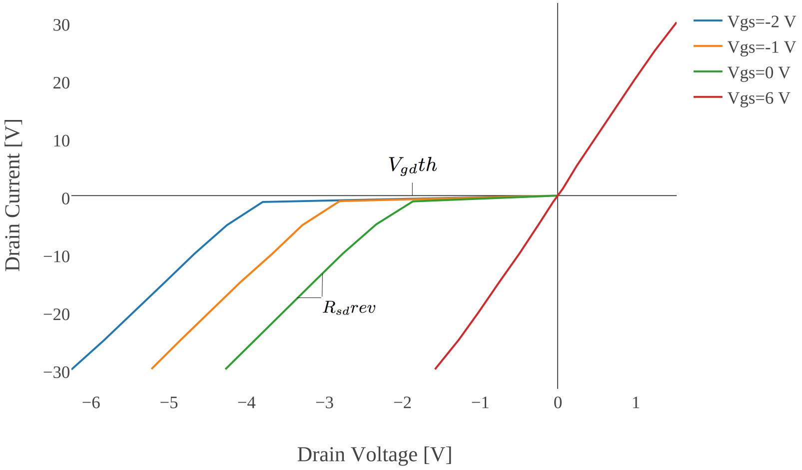


Figure 1.16 – Enhancement GaN device reverse conduction I-V characteristic.

the channel in reverse mode. This parameter depends on the junction temper-

ature, the drain current and the gate voltage. There is a limit for driving the transistor: a too negative gate voltage can saturate the device and dropping voltage can be important.
Figure 1.16 shows the typical behavior of the enhancement GaN in reverse conduction for V_{gs} between 0 to -2 V.

$$V_{sd} = V_{gd}th - V_{gs} + I_{ds} * R_{sd}rev \tag{1.3}$$

By comparison a Si MOSFET body-diode has a dropping voltage around 0.8

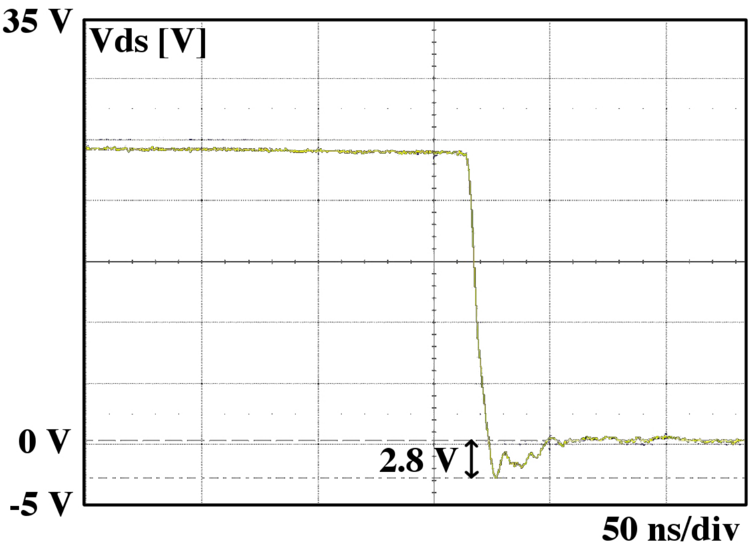


Figure 1.17 – Drain voltage drop of an enhancement GaN device, EPC2012.

V when the GaN device can be between -3 V and -5 V as in Figure 1.17. It appears that the GaN conduction losses become important due to the high voltage drop: it is important to keep as short as possible the dead time [163]. On the other hand, recovery losses does not exist because there is no diode: logically, ZVS switching gives a useful solution to fully take advantage of the enhancement GaN behavior.
If the application requires long dead-time or high current, it can be useful to use in parallel on the enhancement GaN device, a schottky diode to limit the conduction losses in detriment of the recovery loss and additional parasitic elements.

1.2.2.5 Commercial availability

GaN devices have been recently introduced on the WBG devices market. As shown in Figure 1.18, the first available products have been on the market since 2010. The problem of working with a recent technology is the low availability and the difficulty to have access to samples.

In order to consolidate the GaN market, industry is establishing partnerships like recently between Panasonic and Infineon [225] in 2015. Those new market movements will allow a larger production and an easier access in the next few years.

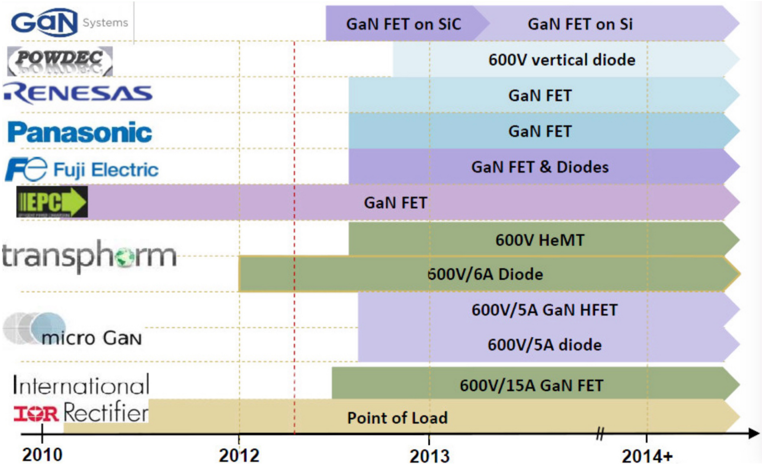


Figure 1.18 – GaN production roadmap, Yole [86].

1.2.2.6 Summary

This first section wished to give a landscape of the GaN devices, a description of the different structures was given for both cascode and enhancement transistors. The first part was more focused to show the capabilities of the GaN material in comparison with other WBG materials and the silicon. We have also seen the different specificities or challenges required by the GaN devices, like the current collapse or the reverse conduction.

We have discussed about the commercial availability of those devices to highlight the context of this study which is made on a pre-mature technology.

In the following section, in order to compare cascode and enhancement technologies, a characterization of each device was performed. According to the study context, high-temperature characterization is included in both static and dynamic results.

1.3 Characterization of an Enhancement and Cascode GaN Devices

Power semiconductor devices can be characterized in both static and dynamic ways. In this section both characterizations are performed and details are given on the different experimental setups used. Dynamic and static characterizations are both well described for Si and SiC in literature [61, 46, 251, 175]. However GaN presents some particularities due to the fast switching capability of the device. Some results on commercial or sample available devices such as IR, HRL, EPC or Transphorm have been already published [58, 161, 166, 80]. The goal of this section is to give a comparative study in a high-temperature application field ($+200°C$), between three representative GaN devices, for losses and switching performances. Also in the context of the MEGAN project, two different generations of GaN from CEA-Leti lab were characterized and the results will be presented in the same time. Those devices are under development and are not comparable to a mature product.
Two of the tested commercial devices testedave an enhancement mode, the EPC2012 from EPC and the GS66508 from GaN Systems, and one with a cascode mode, TPH3006LD, from Transphorm.
The EPC2012 was one of the first GaN available on the market, with rating 200 V, 3 A. The GS66508 is one of the first high voltage, high current device with 600 V, 30 A rating. However at the beginning of this PhD an incomplete datasheet was published. The cascode device is 600 V, 17 A device from Transphorm company. The Table 1.6 summarizes the main parameters of those three devices from each datasheets.

Table 1.6 – Summary of characterized devices

Device	Company	Size	V_{ds}	I_{ds}	R_{dsOn}	v_{gs}
EPC2012	EPC	1.7x0.9	200 V	3 A	0.1 Ω	+6 V
GS66508	GaN Systems	10x8.63	600 V	30 A	0.05 Ω	+10 V
TPH3006LD	Transphorm	8.1x7.3	600 V	17 A	0.15 Ω	+18 V
MEGAN Gen1	CEA-Leti	9x3.6	200 V	20 A	0.03 Ω	-7 V
MEGAN Gen2	CEA-Leti	4.7x2.4	600 V	30 A	0.08 Ω	+6 V

1.3.1 Static Characterization

1.3.1.0.1 Test setup The different tests were performed with a curve tracer (Tektronix 371A) which allows high current pulse up to 400 A. The devices were mounted on a PCB board in order to fit the different packages as shown in Figure 1.19. The board was heated for temperature test, by a hot plate and controlled by a thermocouple placed on the components' package: this ensures a discrepency on temperature less than $+2°C$.

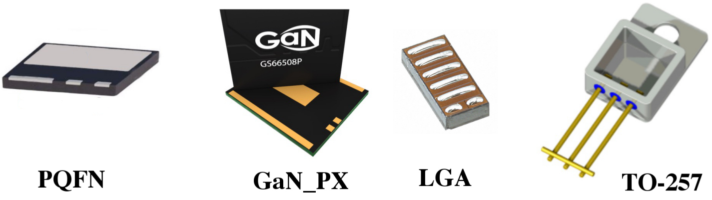


Figure 1.19 – Different packages for each GaN devices.

Presented results do not intend to cover a full datasheet for each components but to complete missing elements and give a high temperature capability view of those components. The final goal of this characterization study is to build an efficient and GaN custom gate driver, with requested parameters such as threshold voltage or gate leakage current.

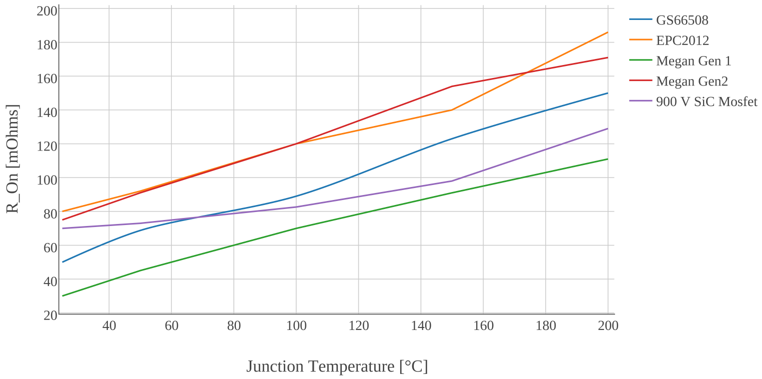


Figure 1.20 – Enhancement GaN devices and SiC MOSFET On resistance vs. temperature measured with the curve tracer.

1.3.1.0.2 On resistance In Figure 1.20, R_{On} is plotted as function of the temperature and exhibits a monotonously increasing trend from $25 - 200°C$ for all GaN enhancement devices. Each measurements were performed at 30% of the nominal current and at the datasheet advised gate voltage. According to Figure 1.22, the variation of the On-resistance at $200°C$ is within 2.5 and 3 times the ambient temperature value.

Comparatively, typical SiC MOSFET has a higher R_{On} value at ambient temperature but the increasein he resistance stays under 2 times the initial value in temperature.

Cascode device, due to the large R_{On}, is not included in Figure 1.20 but in a separate one in order to have an adapted scale for the enhancement mode device. According to Figure 1.21, cascode device has an On-resistance 2 times higher than an enhancement device but presents a similar variation in temperature. The higher On-resistance is mainly due to the Si MOSFET in serial with the GaN device which R_{On} value drastically degrades with temperature.

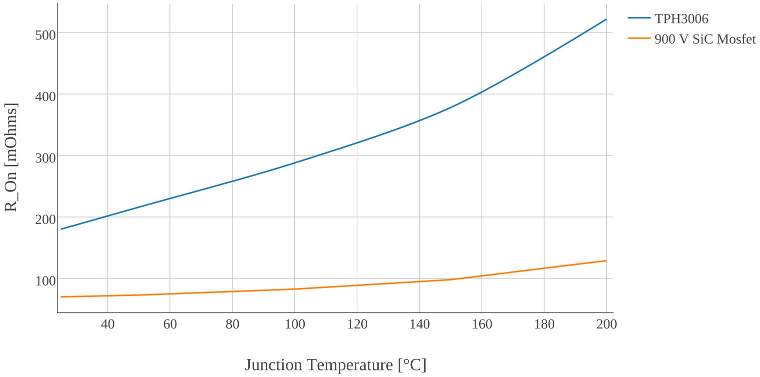


Figure 1.21 – Cascode device and SiC MOSFET device On resistance value vs. temperature measured with the curve tracer.

On-resistance value allows a good overview of the GaN devices as a compartive factor between the different structure.

1.3.1.0.3 Threshold voltage Threshold voltage measurement in temperature appeared as a key element for the gate driver design in order to determine the optimal gate driving voltage. Different measured threshold voltages vs. temperature are shown in Figure 1.23. The global tendency for enhancement GaN devices is a small decrease in the threshold voltage in temperature. The EPC device has an opposite behavior with an increase in the V_{th} up to $1.1V$ at

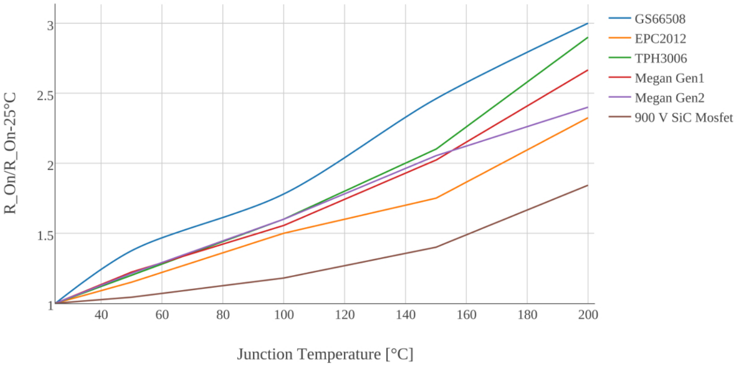


Figure 1.22 – Normalized On-resistances vs. temperature for GaN and SiC MOSFET devices measured with the curve tracer.

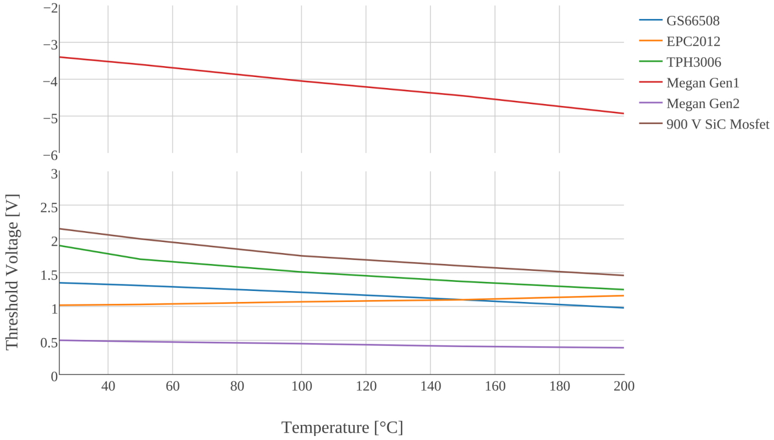


Figure 1.23 – Threshold Voltages vs. temperature for GaN and SiC MOSFET devices measured during switching and with curve tracer.

$200°C$. The cascode structure with a Si MOSFET presents a similar behavior as a classic Si device. The SiC MOSFET as comparison point, presents a higher V_{th} than GaN devices but the decrease in temperature is superior even if it stays higher to the ones of all GaN devices.
Stability of the GaN V_{th} is an interesting point for high-temperature application field, however, solution for increasing this value should be found to have a good dV/dt immunity. Moreover the high reverse dropping voltage of the

GaN does not allow too much negative driving voltage such as for SiC devices. Proper gate driver design has to be implemented to deliver arobust system against dV/dt.

1.3.2 Dynamic Characterization

Currently, Double Pulse Test (DPT) has become the standard to measure the switching performance of a power device. Two pulses are applied on the gate of the device with different times in a inductive clamp circuit as shown in Figure 1.24. Regulating the first pulse duration and the bus voltage, the switching current and voltage stress can be customized. The temperature raise of the junction is limited by the small number of switchings and allows temperature independent measurements. A DPT board was built with a particularly care about reducing parasitic elements as advised in [248]. All the environment is at ambient temperature, only the switching devices are heated by the hotplate. The device package temperature is measured with a thermocouple and at each temperature step a 30 min stabilization time is afforded, in order to ensure that the junction temperature is stable and as close as possible to the packaging one. Figure 1.25 shows the lab test setup. The TO-247 DUT package in this case, is mounted on an isolated pad with thermal greaseand the thermocouple is directly connected on the package with a Kapton tape.

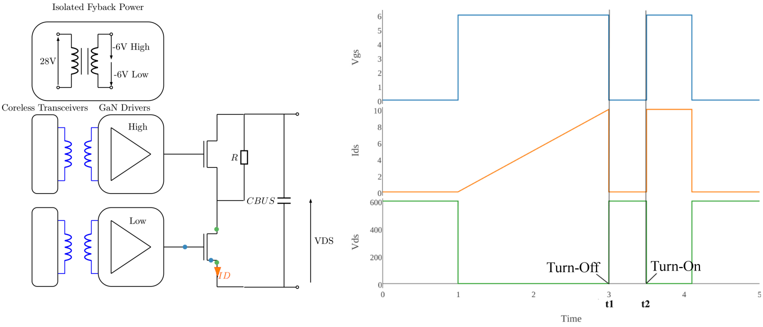


Figure 1.24 – Typical double pulse test circuit with the typical waveform.

The switching tests are performed under 600 V and varying load currents up to 30 A, and repeated for different temperatures with steps up to 200°C.The temperature gradient is limited by the DPT technique but will still be present during the measure with a small impact on results. For a precise measurement of the drain voltage, a high bandwidth and high dynamic range probe is required due the fast switching transient capability of GaN devices. Passive

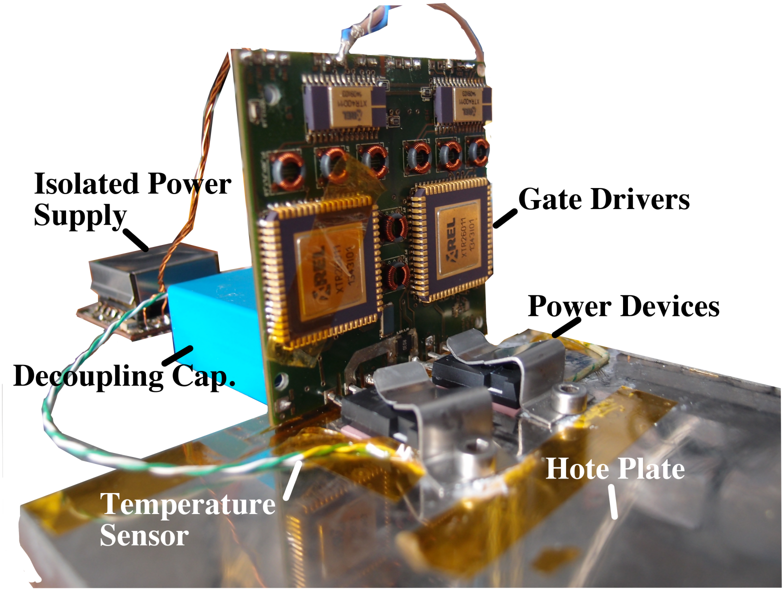


Figure 1.25 – Double pulse tester setup.

probes are preferred because they are presented the both parameters. The slope signal bandwidth can be determined as [46]:

$$f_{sw} = 0.35/(min_{[tr,tf]}) \tag{1.4}$$

Equation (1.4) can be used to determine also the fastest transient signal capability of the measurement system. For the current measurement, it is now well known [45] that coaxial shunt presents the best trade-off between bandwidth, fast rise-time and accuracy. All measurement results presented in this chapter were performed with passive voltage probe from Lecroy PP09 with 500 V for the dynamic range and 500 MHz bandwidth and a T&R current shunt SSDN-10 with a 2 GHz bandwidth and 0.1 Ω value.

However good probes could be useless without specific connectors, short connection pathes and low inductance connectors. DPT board has been implemented in order to reduce the ground loop of the probes and reduce the impact of the parasitic elements from the measurement system on the power switching loop. Figure 1.26 shows an optimized path between the power devices and the shunt in order to reduce parasitic inductance in the measurement loop. For the voltage path, a short wire closed to the ground pad, allows a low current flow in the measurement loop and the coaxial connector (Lecroy coaxial probe

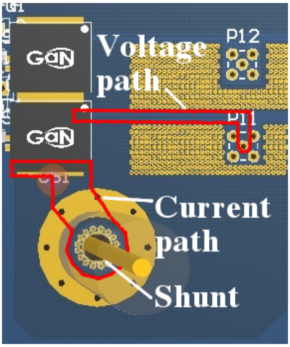


Figure 1.26 – Optimized voltage and current pathes for the GaN Systems GaN HEMT lab DPT board.

connector) keeps the ground loop as short as possible.
The last important issue towards an optimized measurement setup, is to limit the common-mode current in the ground path which is produced by the high dV/dt of the GaN devices phase leg. As shown in [227, 45], common-mode current is responsible of ringing on the drain current which can disturb the measurement of losses. In order to alleviate the issue, external common-mode chokes with high impedance at the common-mode ringing frequency can be employed at both main DC voltage source and probes coaxial cables. Also a specific gate driver power supply was designed with a very low primary-to-secondary capacitance transformer (few pF) in order to limit the current flow through it. This point will be developed in a next chapter.
In this part of the study, we focused the measurement on two components which were fitting the requirements exposed in the introduction. One is the cascode power device TPH3006 and the other one, the enhancement device GS66508. This allowed us to simplify the measurement of losses and the number of design for each DPT prototypes. In all this test, a gate resistor of 2 Ω is used in order to control the switching speed.

1.3.2.1 Enhancement Mode GaN Devices

Figure 1.27 shows 2 different temperature points of the switching behavior for the GS66508 device, with drain current, voltage and gate voltage. The gate voltage applies during this test is 0; 6 V. This value is determined according to the previous static characterization. Figure 1.27 shows that the enhancement GaN device is slowing down in high-temperature: the maximum dV/dt decreases by 45% at 20 A.

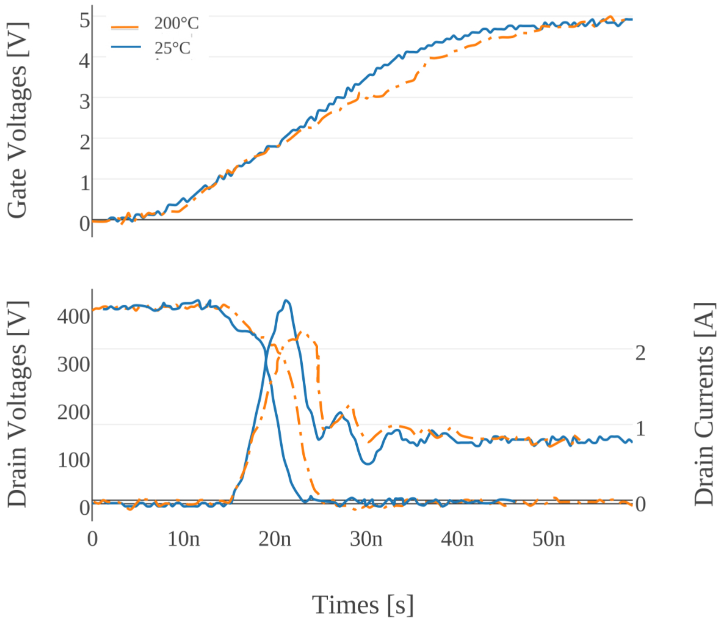


Figure 1.27 – Experimental turn On transient waveforms of the bottom device at 400 V and 1 A at 25 and 200°C from Figure 1.25.

The switching energies are calculated based on the experimental measurements, by doing the integral of the dissipated power $V_{ds} * Ids$. E_{On} and E_{Off} are defined as the turn-On and turn-Off energy dissipated during turn-On and turn-Off transition time as shown in Figure 1.28.

As shown in [248], a special care has to be taken about the alignment between drain current and drain voltage to reduce the mismatch in the loss calculation. In order to do that, the alignment is processed on the oscilloscope by superposing the two waveforms and ensures that current and voltage are switching at the same time. The deskew of the probes is realized directly on the oscilloscope and adjusted during the processing of the data. Figure 1.29 gives the results obtained with 2 Ω gate resistance.

The temperature dependence of the turn-On loss is mainly due to the decrease in the the transconductance [100, 58] in temperature for the GaN devices.The transconductance of the GaN device has the specificity to have a negative coefficient in temperature: in the case of the GS66508 device, the value is divided by 2 between 25 and 200°C. The resistance of the channel increases

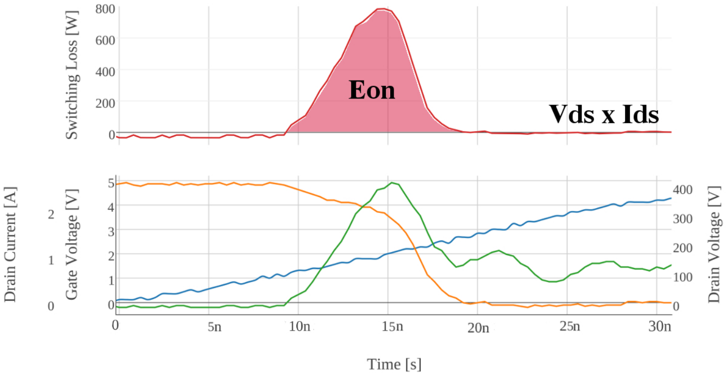


Figure 1.28 – Evaluation of turn-On energy.

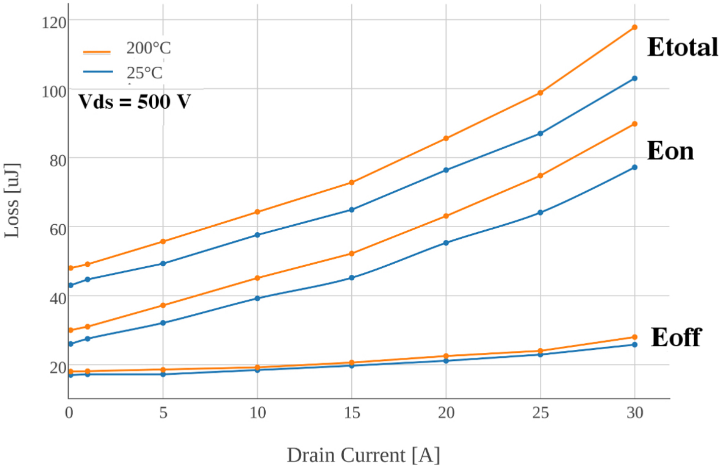


Figure 1.29 – Experimental turn-On and turn-Off losses at 25 and 200°C at $V_{ds} = 500V$ from Figure 1.25.

and saturates the device in high temperature: the result is an increase in the losses with the temperature up to 16% at 30 A. The turn-Off losses seem not really affected by the temperature.

The gate charge specification is a key parameter for the gate driver designer as it sets the power consumption of the gate driver for a given operating frequency. For this test the device is driven by a 6 V gate voltage and a 2 Ω gate resistor with a 200 V drain voltage.

The measured turn-On and turn-Off values of the gate voltage in Figure 1.30,

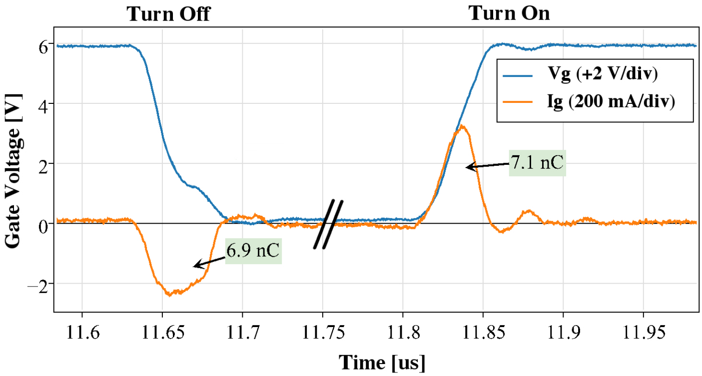


Figure 1.30 – Gate voltage and gate current during turn-On and turn-Off states.

shows the energy necessary to bias the HEMT gate. It is also an experimental technique to determine a mean value of the gate capacitance, a parameter used to design the gate driver. With this GaN device, the measured mean gate capacitance value is:

$$Q_g = \int_0^t I_g \, dt + Q_g(0) \tag{1.5}$$

$$C_{gs} = \Delta Q/\Delta V = 250pF \tag{1.6}$$

1.3.2.2 Cascode Mode GaN Device

The same method as previously detailed is used for the cascode device. The cascode device loss measurement is highly dependent on the package parasitic inductance as shown in [251, 235, 121]: for our test, we choose the PQFP package in order to reduce those parasitic elements. As shown in [235], a small switching loss variation in temperature is expected since the switching waveform shapes are quite similar in Figure 1.31. The cascode GaN exhibits a maximum dV/dt about 102 $V/\mu s$ with an external gate resistor of 2 Ω. However, during the test the gate leakage current increases up to 3 mA at $200°C$ and $V_{ds} = 500V$.

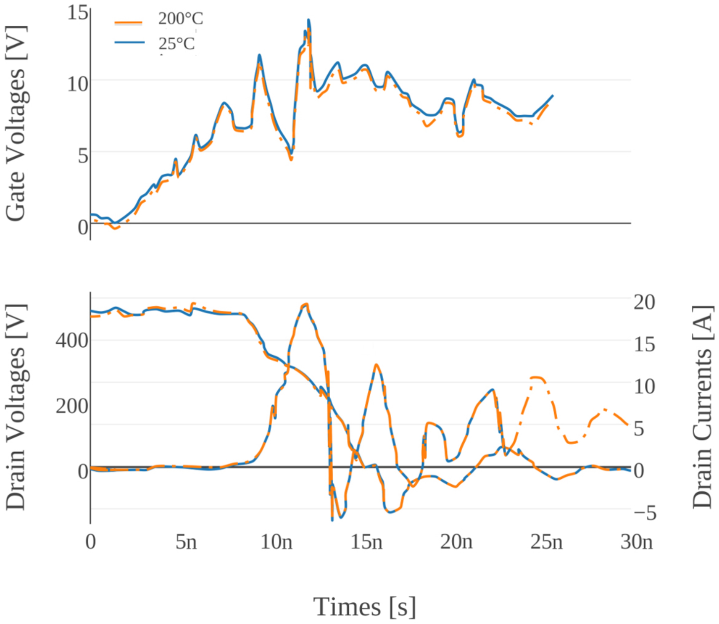


Figure 1.31 – Experimental turn-On transient waveforms of the bottom device on the board at 500 V and 5 A at 25 and 200$^{\circ}C$.

To performed the DPT, a gate voltage of 0; 10 V is applied since the gate resistor is limiting the di/dt: in the case of a 0 Ω gate resistor low inductance gate loop design should be done in order to avoid re-conduction fault. This fault has been mainly noticed with TO-220 package and not with the PQFN chosen.

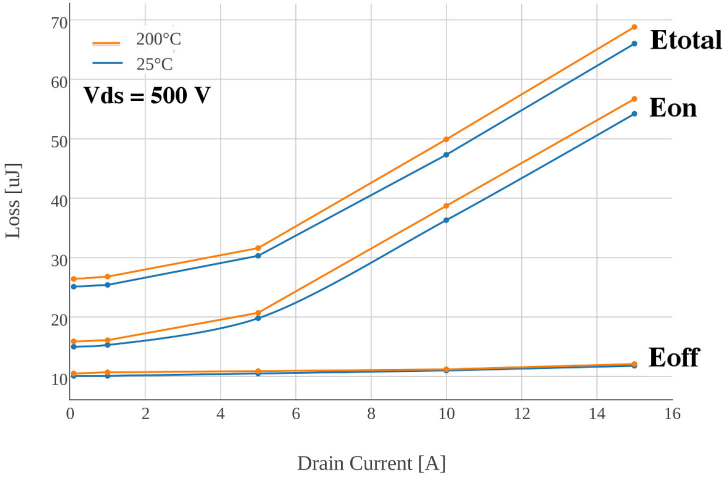


Figure 1.32 – Experimental turn-On and turn-Off losses for 25 and 200°C at $V_{ds} = 500V$.

1.4 Contribution to modeling of an Enhancement GaN device

This section does not present a full model developpment, however an existing SPICESimulation Program with Integrated Circuit Emphasis model is improved according to our own experiment results and characterization and a specific focus is made on the turn-On behaviour and a related modeling of the Miller effect in the GaN device.

1.4.1 SPICE Model Improvement

A SPICE based behavioral simulation model is initially provided by the device manufacturer, GaN Systems. LTspice software is used for the circuit simulation. In order to test the model in a real case, the device model is placed in a phase leg configuration. Figure 1.33 shows that simulation waveforms do not match with the experimental ones. In simulation, rising and falling times are longer than experimental ones. Also ringing and overvoltage do not match with the experimental results. It appears that the spice model provided by the manufacturer, does not allowed a good accuracy for the circuit prediction. A modification of the model seems a good approach to improve the accuracy without developing a full model of a GaN device.

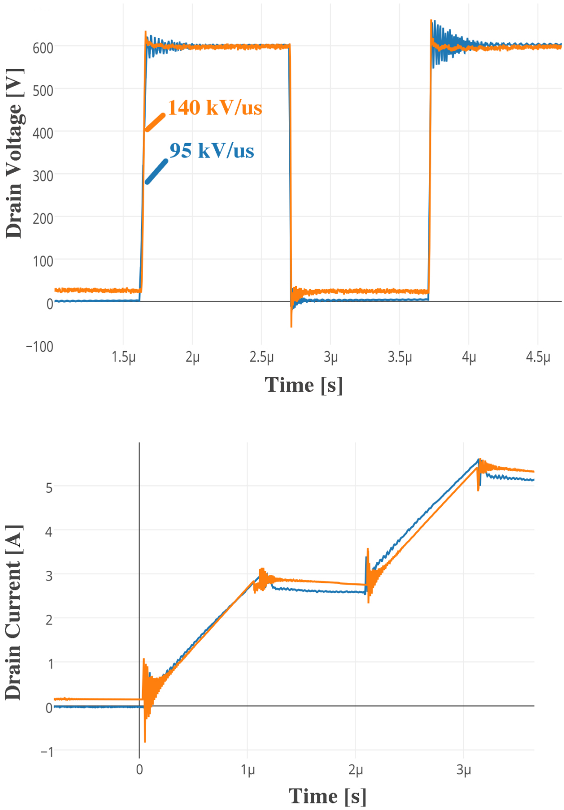


Figure 1.33 – Experimental (orange) and simulation (blue) comparative waveforms.

The modification of the model begins with the verification of the basics characteristics of the device.

Figure 1.34 shows the I-V characteristics of the GaN model device and the accuracy of this characteristics is verified.

The C-V characteristic is checked in order to validate the capacitance of the model as shown in Figure 1.35. Both C_{rss} and C_{oss} are fitting the datasheet values.

The first mismatch is found in the C_{iss} characteristic as shown in Figure 1.36 top, of the GaN device. After a proper modification of the non-linearity coefficient, the values are closer to the datasheet ones, modified model is given in

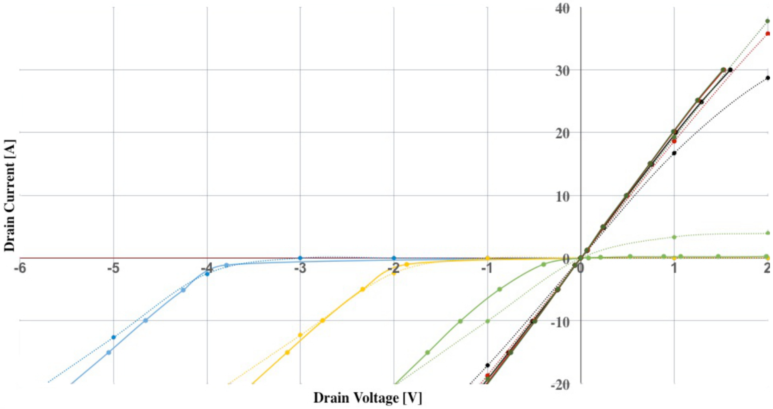


Figure 1.34 – Experimental (plain) and simulation (dashed) comparative drain voltage and current characteristic.

appendix .1. Also an experimental value from [100] allows a double comparison for the C_{oss} value.

A new equivalent circuit of the DPT setup was designed in Figure 1.37 and simulated with better curves' fitting between experiment and simulation as shown in Figure 1.38. The schematic was developed by following the work made in [82] with a shunt model, a decoupling capacitor model, a gate driver model and voltage probes' model. All the models used in this schematic will be detailed in the last chapter of this thesis.

Figure 1.38 shows a good matching between simulation and experimental waveforms, however the parasitic elements which influence the parasitic oscillation, does not fully matched. In order to improve the model, a specific Spice circuit model with parameters extracted from the FEM model of the board, is shown in the last chapter of this thesis.

Based on the switching energy calculation from the simulation waveforms, another comparison can be done between experimental and simulation data. Due to the PCB board parasitic elements the matching in high-drain current between experimental and simulated value are different for the E_{On} value. In this section a SPICE model was improved in parallel and an experimental DPT board was designed to validate simulation with experimental data. Both cascode and enhancement GaN devices were tested in current and in temperature and results were compared with simulation.

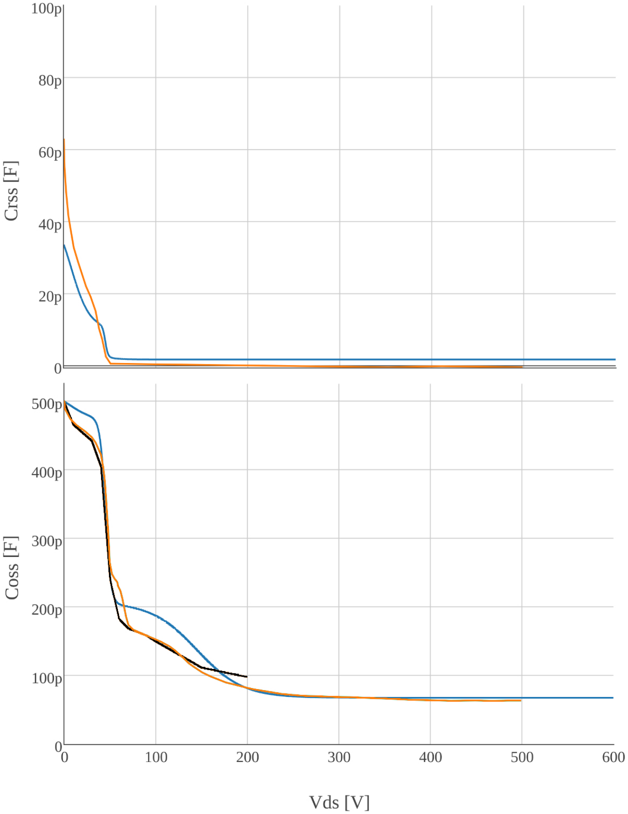


Figure 1.35 – GaN device C_{rss} and C_{oss} characteristic with datasheet (orange), simulation (blue) and experimental value (black) from [101].

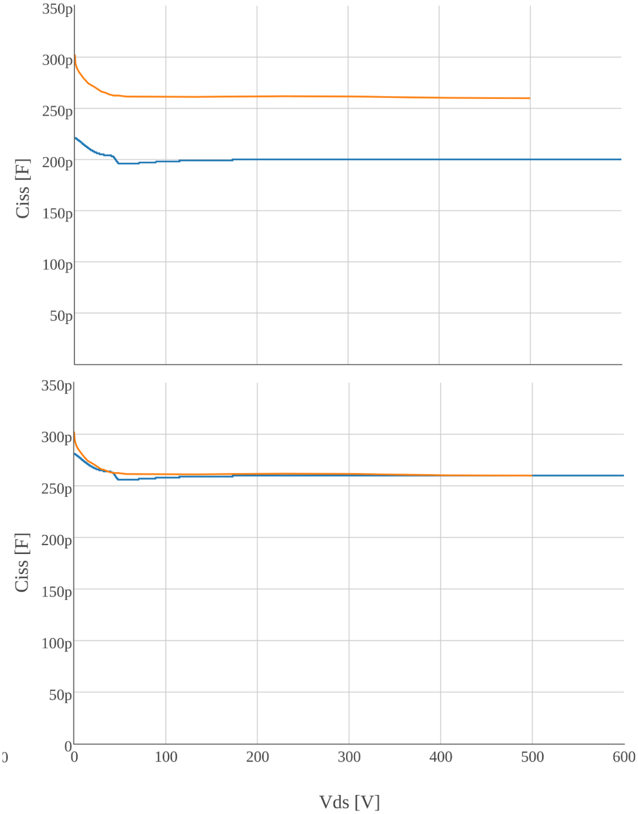


Figure 1.36 – GaN device C_{iss} capacitance datasheet (orange), simulation (blue) value before (top) and after modification (bottom).

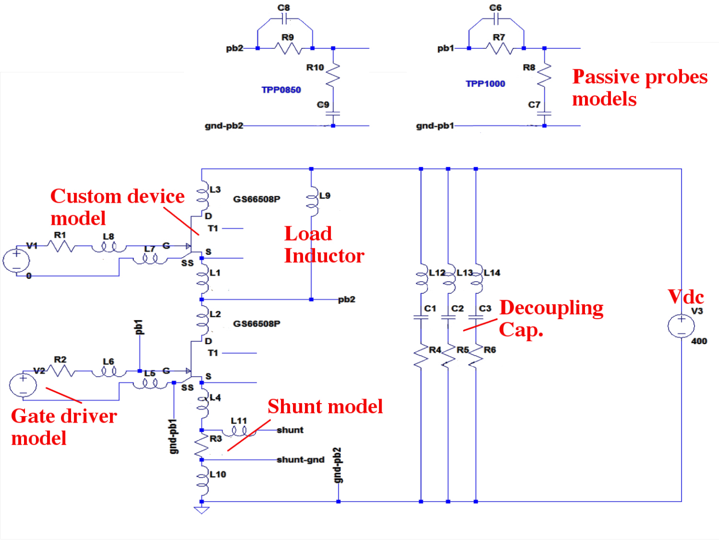


Figure 1.37 – Simulation circuit of the board in the double-pulse test configuration.

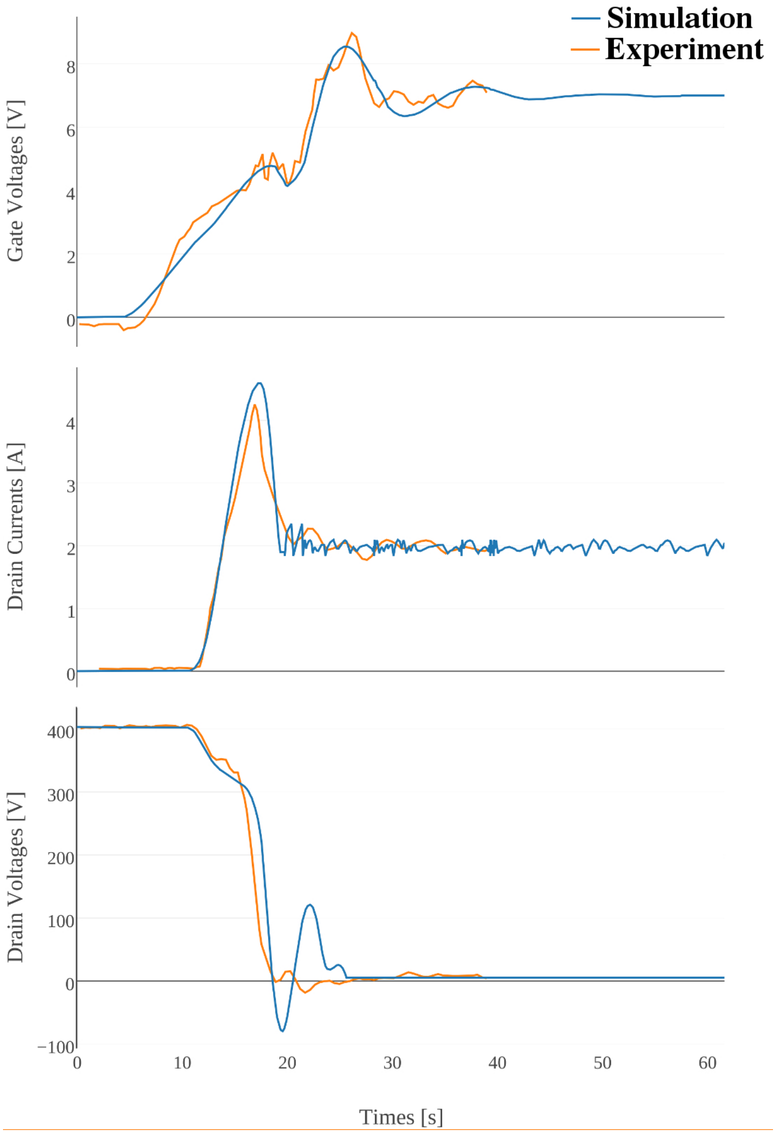


Figure 1.38 – Simulated and experimental turn-On switching waveforms of the bottom GaN device at 400 V, 2 A with $R_g = 0\ \Omega$.

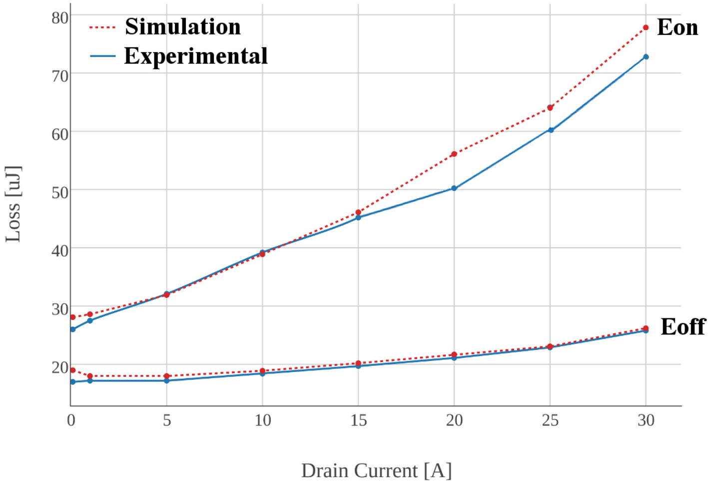


Figure 1.39 – Simulation and experimental E_{On} and E_{Off} losses from GS66508 modified model.

1.4.2 Turn-On transient behavior

This study is based on personal work but also on [100, 186]. A part of the study was made during my internship at Tennessee University in Knoxville, UTK. All works show that the classical Baliga formula [21] is no longer valid in the case of a high-speed switching devices, for describing the Miller effect. Actually, in the case of a gate resistor close to zero with a GaN device, the gate voltage is not dependent anymore on the driving voltage but only on the drain current I_d. In this case, the Plateau voltage $V_{plateau}$ does not exist. This paragraph describes the methodology of the turn-On behavior and the equation for the gate voltage transient and add some simulation results as a corroboration.

In order to analyze turn-On phenomena and improve the previous SPICE models, a simplified model was developed. Although, after checking and modifying the static characteristics of the model, it seemed interesting to study more carefully the dV/dt phenomena at turn-On transient time. Moreover the enhancement GaN device has a similar behavior as a Si MOSFET: that is why most of the model available currently are based on a MOSFET model. It is also interesting to develop a model in order to analyze carefully and understand experimental results.

Figure 1.40 shows the equivalent enhancement GaN model based on a classical MOSFET one. C_{ds}, C_{gd}, C_{gs} represent the parasitic capacitance between the three connections, R_{dsOn} is the equivalent resistance of the channel and the channel current is modeled with the current source $I_{channel}$. In the case of the GS66508 GaN device, the substrate is internally connected with the

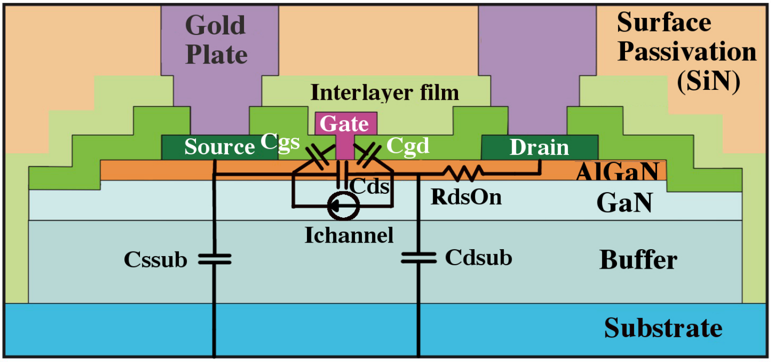


Figure 1.40 – Equivalent circuit model for an enhancement GaN device.

source, resulting in C_{ssub} to be negligeable. In the same way C_{dsub} can be serialized with C_{ds}. The typical turn-On transient for a phase leg with GaN

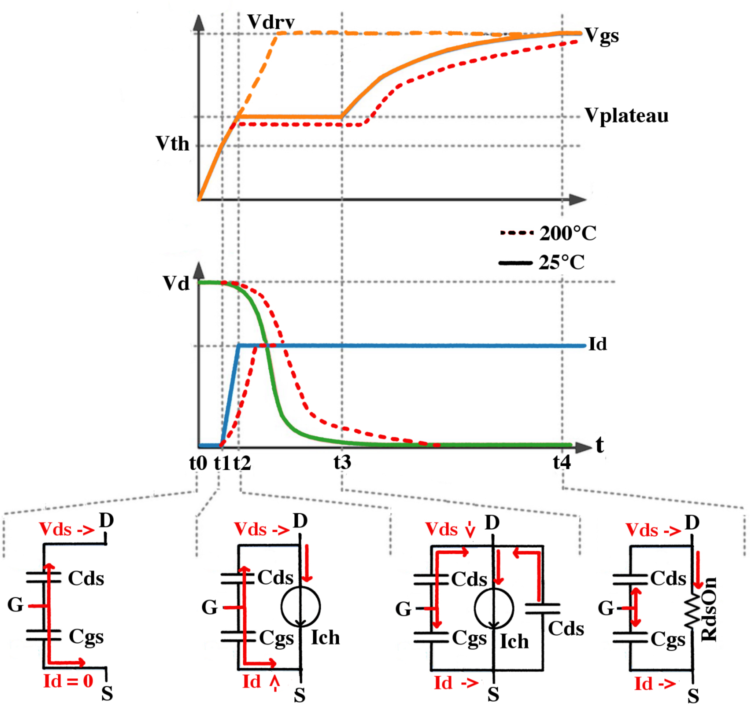


Figure 1.41 – Theoretical turn-On process of GaN HFET.

HFETs based on the MOSFET behavior is shown in Figure 1.40, with the current pathes for each subintervals shown with red arrows and the temperature specificity is shown with the hashed red line.

- In phase 1 ($t_0 < t < t_1$), the transistor is blocked and the gate current is starting to charge C_{gs} and C_{dg} through the reverse conduction mode of the top switch of the phase leg. According to [186] the current in the driving loop can be expressed as :

$$I_g = \frac{V_{drv}}{R_g} * exp(\frac{-t}{\tau_1}) \quad \text{with } \tau_1 = R_g * (C_{gs} + C_{gd}) \quad \text{or } \tau_1 = R_g * C_{iss} \tag{1.7}$$

According to Equation (1.7) the gate voltage exponentially grows up to the threshold voltage V_{th} and the duration of phase 1 can be expressed as follows:

$$t_1 - t_0 = R_g * C_{iss} * log\left(\frac{V_{drv_{On}} - V_{th}}{V_{drv_{On}} - V_{Plateau}}\right) \tag{1.8}$$

- In phase 2 ($t_1 < t < t_2$) the current I_g continues to grow exponentially following Equation (1.7) until $V_{Plateau}$.

  $$\frac{dI_d}{dt} = g_{fs} * \frac{dV_{gs}}{dt} \rightarrow \frac{dI_d}{dt} = g_{fs} * \frac{V_{drv} - V_{th}}{R_g * C_{iss}} \tag{1.9}$$

  The main point of this phase is the raise of the drain current which is dependent of the transconductance g_{fs} and the variation of the gate voltage V_{gs} as shown in Equation (1.9).
  At the end of phase 2the top switch "body-diode", after a fast recovery time, gest blocked. Then, the drain voltage V_{ds} can decrease.

- In phase 3 ($t_2 < t < t_3$) the GaN device is now in a conduction mode: the 2DEG is fully established. As shown in Figure 1.41 the drain current I_{ds} is the sum of three currents: the channel one I_{ch}, the current in C_{gd} and the current in C_{ds}. The drain current may be expressed as:

  $$I_{ds} = I_{ch} + C_{gd} * \frac{V_{drv} - V_{gs}}{R_g * C_{iss}} - C_{ds} * \frac{dV_{ds}}{dt} \tag{1.10}$$

  During this phase, the charge of C_{gs} is interrupted due to the high current called from C_{gd}.The gate voltage V_{gs} stays constant and equal to $V_{Plateau}$ even if the gate charge Q_g is still rising: this is the Miller effect.
  The $\frac{dV_{ds}}{dt}$ appears during this phase too and its non-linearity is mainly due to C_{gd} capacitance variation. However in the GaN case the value of the intrinsic capacitances are really low as shown in Table 1.7 and the Miller effect can be neglected in the case of a small gate resistance R_g and consequantly a high gate current. This case reduces the Miller effect time close to zero because of the really short charging time of those capacitances as shown in Figure 1.42.

Table 1.7 – Summary of intrinsic capacitance values for GaN, SiC and Si devices

Device	C_{rss}	C_{iss}	C_{oss}	V_{ds}	V_{gs}
Si 600 V	1.5 pF	2800 pF	100 pF	450 V	10 V
SiC 900 V	3.3 pF	700 pF	60 pF	600 V	15 V
GS66508	2 pF	260 pF	80 pF	450 V	6 V
TPH3006LD	5 pF	740 pF	133 pF	600 V	10 V
MEGAN Gen2	3 pF	600 pF	420 pF	650 V	5 V

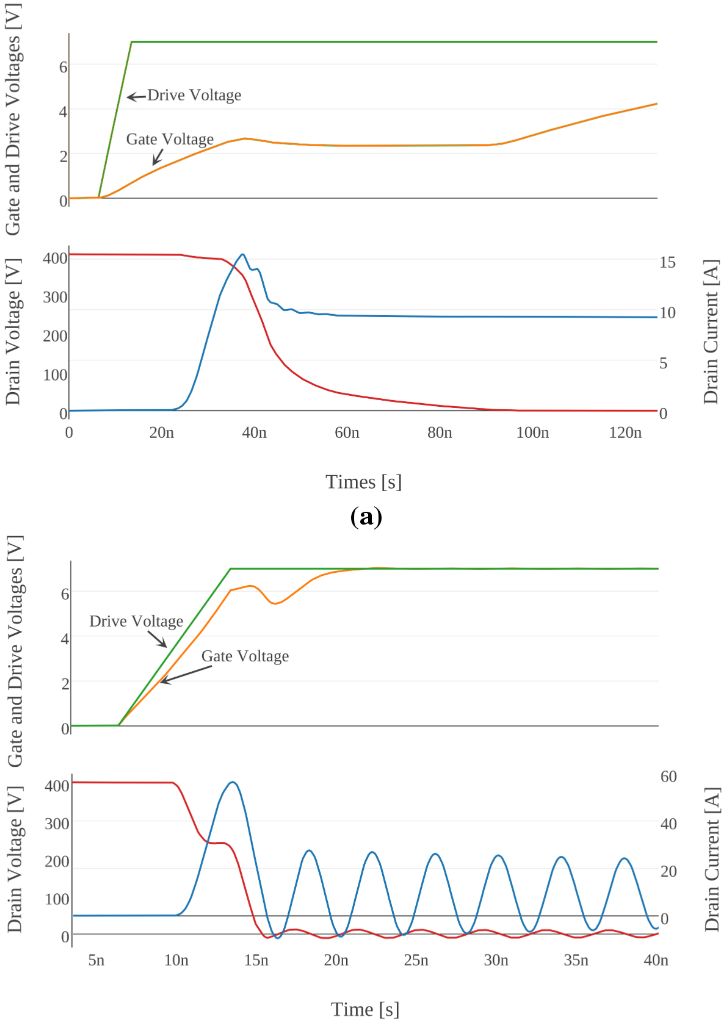
As demonstrated in [100], the Miller effect can be assimilated to a slope more than a plateau and be modeled with:

$$\frac{dV_{gs}}{dt} = \frac{V_{drv} - V_{gs}}{R_g * C_{iss}} - \left(\frac{C_{rss}/C_{iss}}{2 * C_{oss}}\right) * g_{fs} * (V_{gs} - V_{Plateau}) \qquad (1.11)$$

Equation (1.11) is divided in two parts: the first one is the voltage supplied by the gate driver and the second part is the feedback current from the Miller effect. Usually the second term is large enough to balance the gate driver voltage and produce the Miller plateau. But in the GaN case, as explained before, the second term is reduced due to the low parasitic capacitance values and the gate voltage V_{gs} continues to rise until the capacitance C_{rss} increases until avoltage below 50 V. During this short rise of C_{rss}, the second term of the equation is becoming larger and the gate voltage V_{gs} quickly falls just before the GaN device is going to the phase 4 as shown in Figure 1.42 b).
This point is at the base of the development of a custom gate driver with 3 voltage steps in order to obtain faster dV/dt. The driver is detailed in the last chapter of the thesis.

- In phase 4 ($t_3 < t < t_4$) , the $\frac{dV_{ds}}{dt}$ ends and the transistor is going into the ohmic region. The drain voltage V_{ds} is equal to $I_{ds} * R_{ds_{On}}$ and the gate voltage value is stable since both C_{gs} and C_{gd} are charged at the gate driver voltage V_{drv}.

The turn-Off is not detailed here, since it is acting symmetrically at the turn-On process. All the equations stay correct for this case too.
In order to conclude, Figure 1.43 shows the non-ideal switching trajectories for both turn-On and turn-Off and allows to see the 4 phases detailed before, replaced in the I-V characteristic.



(a)

(b)

Figure 1.42 – Spice Simulation of the turn-On waveforms with R_g =100 Ω (top) and R_g =1 Ω (bottom).

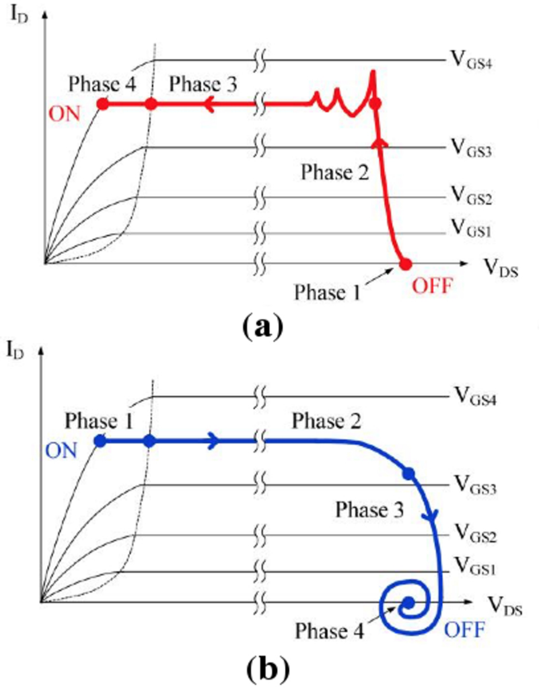


Figure 1.43 – Non-ideal switching trajectories for turn-On (a) and turn-Off (b) from [46].

1.5 Conclusion

In this section, the development of a primary GaN spice model shows a good matching with the most experimental experimental results. However a precise model of the turn-On transient seems interesting in order to customize a classic MOSFET spice model to adapt to a fast switching GaN device. The increase in the switching speed mainly due to smaller intrinsic capacitances in the GaN device case, includes new switching curve shapes not modelized in usual equations.

The PT boards have been developed to help have an overview of the switching losses in both cases of cascode and enhancement devices. The comparison with respect to temperature of those two types of device was also performed up to $200°C$. This section results are the base of the different designs presented in the next sections.

Chapter 2

Isolation of control signal using a Coreless transformer

Contents

This chapter details the different aspect of the dV/dt immunity in an inverter system. The high-temepraturе constraint is also present in this chapter with a specific coreless transformer presented in a custom modulation;demodulation chip-on-board system.
A simulation approach is applied to build a precise model of the dV/dt impact in a inverter system.
A dV/dt generator is also developped in order to corroborate the simulation model with experiment. Different isolation systems are tested in order to provide a comparative test.

2.1 Introduction

In Chapter 1 the different structures of GaN devices shows that the lateral structure is the most commonly used device currently. The different intrinsic

capacitances of the device are so small that it gives a very fast device with high dV/dt capability. The different measurements carried-out in the study, gave a maximum point at $210kV/\mu s$ at turn-Off for the GS66508 device and a dI/dt close to $10A/ns$.
Figure 2.1 shows the experimental values of the dV/dt at turn On and turn Off for different drain voltages and 2 Ω gate resistor. The comparison in Table 2.1 between Si, SiC and GaN device shows the new challenge dictated by the GaN device in the dV/dt immunity field.

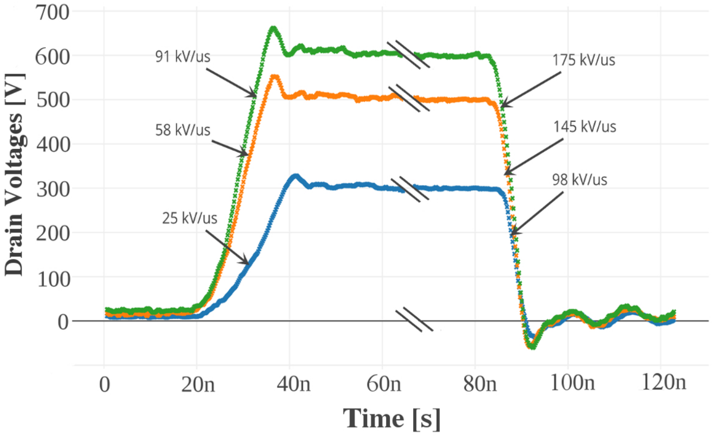


Figure 2.1 – Maximum experimental dV/dt for different drain voltages and a 2 Ω gate resistor.

Table 2.1 – Maximum experimental dV/dt for Si, SiC and GaN devices.

Device	Maximum dV/dt
GaN	$210\ kV/\mu s$
SiC	$90\ kV/\mu s$
Si	$50\ kV/\mu s$

In the context of an inverter composed of three phase legs, each one requests gate drivers, isolated power supply and control signal isolation. The isolation is requested by the floating high-side of the leg. In the case of dV/dt generated by the lower-side device a common-mode current is circulating through

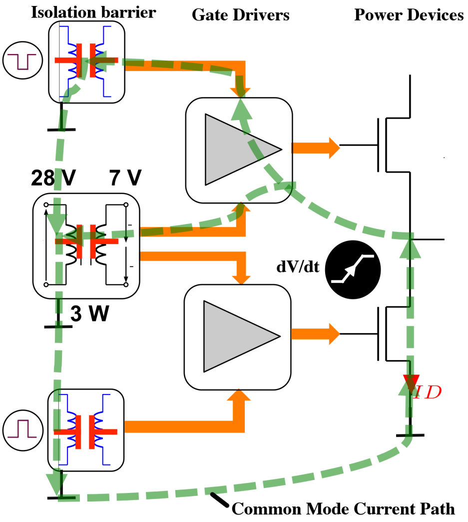


Figure 2.2 – Simplified schematic of the circulating common-mode current in an inverter phase leg.

the isolation capacitance of each power supplies and also through the control signal isolation, the current loop is closed by the coupling capacitance with ground as shown in Figure 2.2. If we are assuming that the isolation capacitance of each device is the dominant element for limiting the common-mode current [167], the current value can be estimated by:

$$I_{cm} = C_{iso} * \frac{dV_{ds}}{dt} \tag{2.1}$$

Based on Equation (2.1), it is easy to plot the current I_{cm} vs. dV/dt for different values of capacitance.

As presented before in the case of a GaN devices the dV/dt immunity has to reach 200 $kV/\mu s$, it is easy to see in Figure 2.3 that the isolation capacitance for each device has to be close to the order of magnitude of picofarad to have a limited circulating current.

As shown, the isolation function in the inverter system with WBG devices has to have the lowest capacitance to limit unwanted common-mode current circulation. High common-mode current generates unwanted logic level in the different logic buffers (FPGA or modulator) and can affect the power devices by generating short-circuits in the phase leg in the worst case.

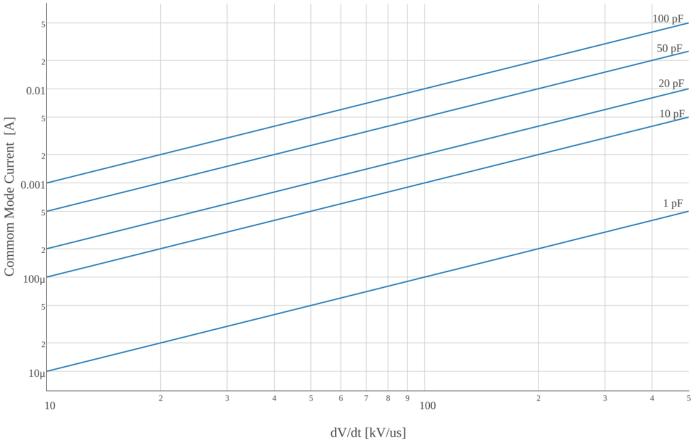


Figure 2.3 – Common-mode current for different isolation capacitances and dV/dt.

2.1.1 Galvanic Isolation Solutions

Different solutions exist for designing a galvanic isolation such as radiative coupling, capacitive coupling, or inductive coupling. Less common, such as the piezoelectric isolation or the radio frequency transmission can be found in specific products or lab demonstrators. A quick comparison is necessary to evaluate each one, moreover the high-temperature application field of this thesis needs specific requirement for the isolation capability.

2.1.1.0.1 Magnetic Core Transformer It is probably one of the most common solution for designing an isolation, especially in IGBT converting system with a good static isolation up to 5 kV [167].

As shown in Figure 2.4 commercially available products exist for this solution and in this case one transformer is dedicated for the power supply and the other one for the control signal isolation.

However this solution presents drawbacks: the first one is the volume of the magnetic core which is important and does not allow any integration of the solution. The second one is the high current requested by the windings of the transformer. And since the primary and the secondary windings of the transformer are superposed on the same substrate, the isolation capacitance is high.

However some laboratory solutions exist with some small toroidal ferrite which

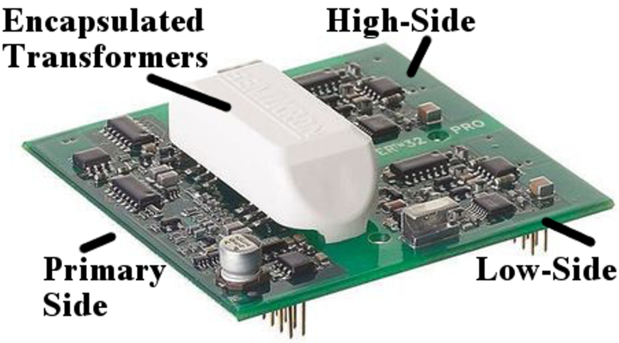


Figure 2.4 – Semikron IGBT gate driver with magnetic core isolation [1].

is offering a small discrete solution. Specific magnetic materials with high Curie temperature point are stable in high-temperature. Ampere lab developed a solution for a gate driver board [166] with discrete magnetic core

As shown in Figure 2.5, the gate driver board embeds 3 toroidal cores made with 4C65 magnetic material which has a Curie point at 280$^\circ C$ and a small volume. The solution was tested successfully up to 200$^\circ C$. However from a reliability point of view the mechanical stress applies by a temperature cycling can break the copper wire and an encapsulated solution would be more reliable.

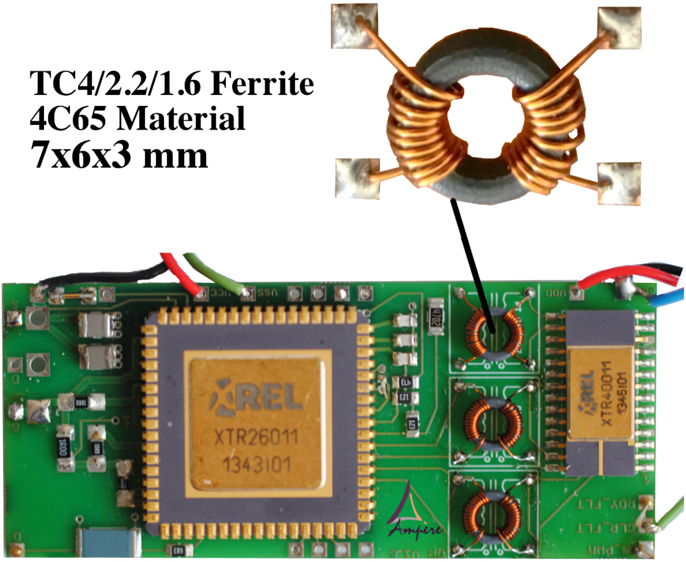


Figure 2.5 – High-temperature solution for a control signal isolation with a toroidal ferrite [166].

2.1.1.0.2 Coreless Transformer The coreless transformer does not have a magnetic core, in order to reduce the global volume and because of that it is widely integrated on Si chip. Generally, solutions present a signal modulation to transmit the data through it at few MHz to GHz: the result is a really small size which can be integrated in commercial available packages.
Current solutions propose static isolation between 2-3 kV with a dynamic isolation around 50 $kV/\mu s$ and operating temperature between -40 to $125°C$. Due to the high modulation frequency, the coreless transformer solution can be a source of EMI perturbation. As shown in Figure 2.6, the coreless transformer is a solution interesting for high-level integration products: however the requested dedicated modulation system is quite complex and the isolation capacitance is usually high, since the small size.
AMPERE lab proposed a high-temperature solution based on a coreless transformer [165], this solution will be detailed in this chapter.

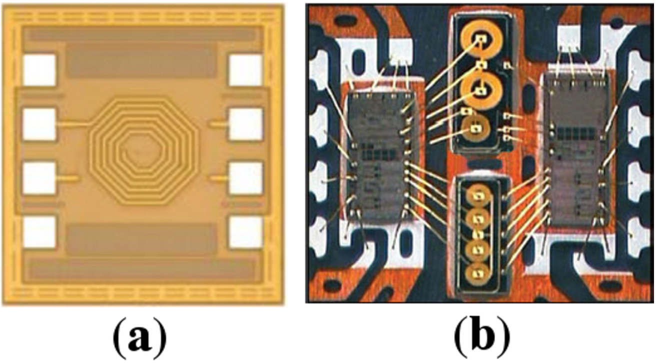


Figure 2.6 – Coreless transformer application, a) data isolation single transformer [147]; b) and a DC/DC converter with signal isolation in a iCoupler product [38].

2.1.1.0.3 Optical coupling Different solutions exist where the signal is transmited through an optic signal. The first one and the most commercialized one is the opto-coupler. The opto-coupler is using a LED to transmit the signal and a photo-transistor as the receiver. Due to the high isolation capacitance value of this solution and the high variation of the propagation delay about 10-40 ns, this solution is only used for slow and low-power converting system such as IGBT one.

Moreover, in a high-temperature point of view, the optical properties of the opto-coupler are no longer active beyond $125°C$ [226].

Another optical solution is the optical fiber which offers a perfect isolation barrier since the isolation capacitance is nearly equal to zero. The integration is limited by the high current requested by the laser diode and the optical connector.

A solution proposed by [76] shown in Figure 2.7, is using a 400 mW laser diode and a photovoltaic converter for the isolation of the signal and the power supply, coupled with a resonant driver to reduce by 10 the power of the system. The isolation system was implemented in a 1400 V 300 A IGBT converter.

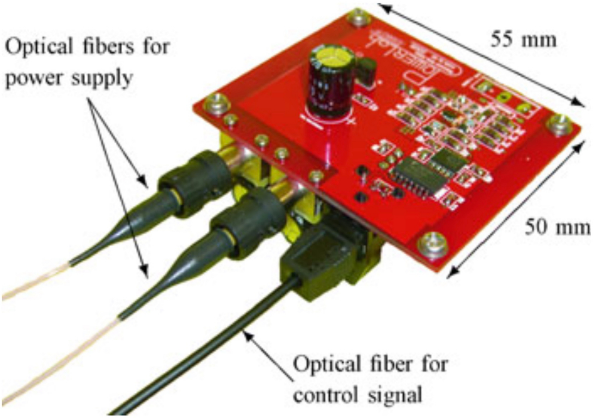


Figure 2.7 – Resonant gate driver optically isolated and supplied [76].

2.1.1.0.4 Capacitive coupling The isolation barrier offered by a capacitor or a dielectric can be also used in order to transmit signal. This solution is really attractive due to the high integration capability of the solution and because it is a really efficient one. However, the solution does not provide a good dV/dt immunity because the value of the capacitor has to be high enough to transmit the energy. The static isolation is limited by the width of the dielectric which limits this solution to applications below 500 V.

Figure 2.8 shows a PCB integrated capacitor isolated solution with a 400 V

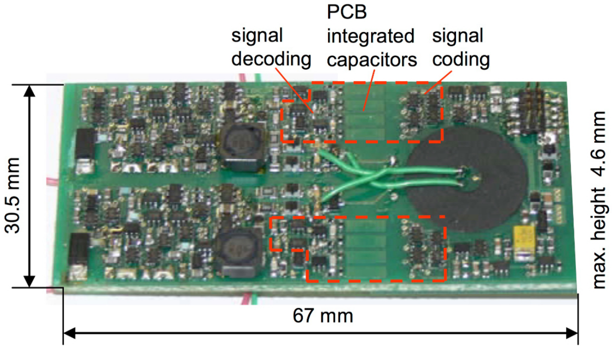


Figure 2.8 – Isolated gate driver solution with PCB integrated capacitor [242].

DC bus capability [242]. The capacitors are fabricated between two layers of

the PCB with a dedicated coding circuit. The large area dedictaed by the capacitor shows the limitation of this solution.
Another commercial solution is implemented in SiliconLabs products. No paper exists on the technology implemented in the products but it is interesting mention the isolation characteristics: one of the best capability in the market, Si827x gate driver [196] is credited of 200kV/us of immunity.
The solution as described in the datasheet is mentionning a silicon based isolation, probably capacitive, with a differential RF modulation/demodulation. It is probably this last point, with a 2-level modulation, that allows a good noise immunity.

2.1.1.0.5 RF solution Like optical solution, the idea is to propagate an electromagnetic signal between an emitter and a receiver without contact. In the radio-frequency domain, antennas are put in regard one to the other as in the pertinent solution with a butter coupler, named form its shape [145]. The solution is using the RF resonance with a modulation at 5.8 GHz. The antennas are placed face to face on a sapphire substrate as well as the gate driver.
The solution is integrated in a 1.7x1.8 mm area with a 2 pF isolation capacitance.
The solution shown in Figure 2.9 was implemented in a Panasonic GaN converter with a 80 V drain voltage. The gate driver supply power is less than a Watt and the estimated maximum dV/dt immunity is 25 kV/us according

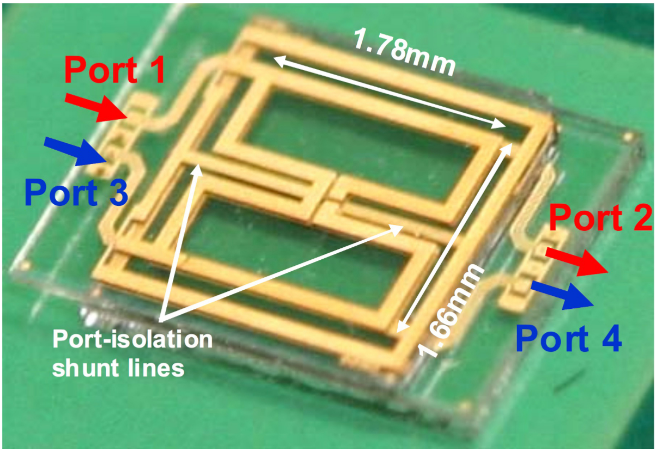


Figure 2.9 – Butterfly coupler on a sapphire substrate [145].

the author.

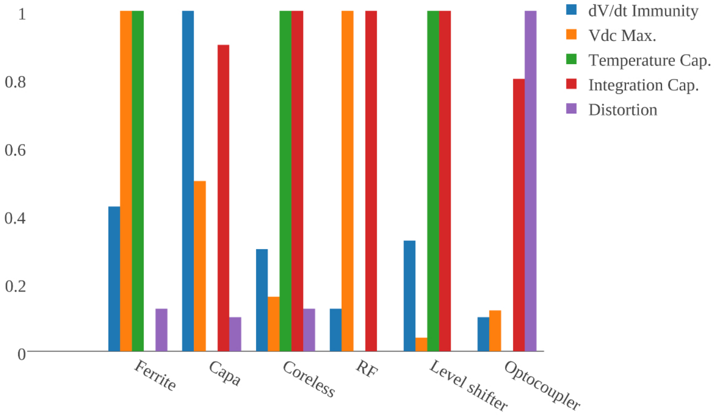


Figure 2.10 – Comparison of some isolation solutions previously presented.

The Figure 2.10 shows a comparison of each solutions presented before including also the level-shifter simple solution even if this low-voltage solution is not fitting our requirement. Values are normalized to the best figure for handy comparison.

2.2 High-Temperature Coreless Transformer Isolation Barrier

In this section, a coreless transformer component developed in the lab is presented. Its characterization and modeling are presentedas well.
An 1500 h aging test was performed in order to confirm and determine the best structure. Finally a demonstrator prototype was designed and tested up to 200°C.
The coreless choice as an isolation for the control signal was motivated by the recent advances which have brought to industrial level the coreless technology for integration in a chip of a driver [27, 211, 142].
There is an interest to develop a discrete coreless transformer. In fact, discrete components require less development efforts than fully integrated systems and permits flexibility in various applications and also a robust isolation.

2.2.1 Characterization and Modelization

Coreless transformer samples were developed in the lab in a previous project, FP7 Caterene THOR in collaboration with STMicroelectronics in Tours.

In Figure 2.11 coreless transformers are processed using Integrated Passive Device technology (IPD) from STMicroelectronics. It consists of a glass wafer onto which two layers of copper are deposited, insulated by a specific resin. It should be noted that the resin is a broad-band sensitive photopolymer named B-staged bisbenzocyclobutene (BCB).

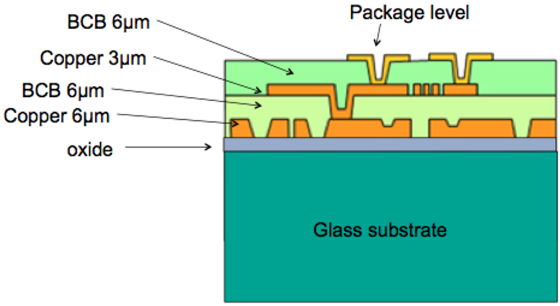


Figure 2.11 – Simplified cross-section of the technology used for the coreless transformer. With Courtesy of STMicroelectronics.

It is intended to be used as dielectrics in thin film microelecronics applications. This polymer was not specially developed for high temperature applications, however the process of reticulation that happens during the initial curing process leads to believe that an extension of the usual temperature limit (125 to $175°C$) is achievable.

Different coreless transformer structures have been fabricated to find the optimal winding and pads location structure as shown in Figure 2.12. The primary winding and the secondary winding are etched on the same metal level, while the second metal level is used to "bring back" the extremity of the coil from the center of the device to the side of the chip. For some applications it is necessary to have the contact pads at the corner of the chip, for improving insulation at package level for example.

This implementation is called "single layer" transformer and is noted "TRS", when double layers are noted "TRD".

For the purpose of verification the transformer is characterized using an impedance analyzer against the model in Figure 2.13. From a practical point

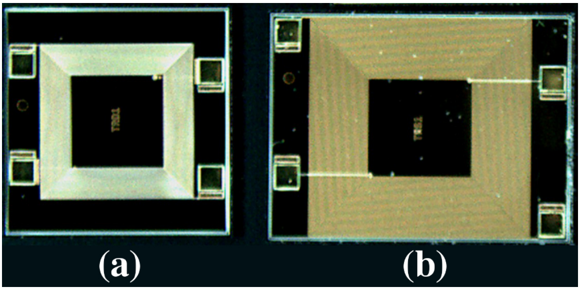
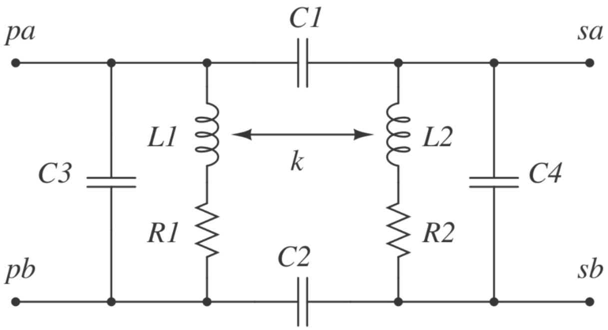


Figure 2.12 – Coreless transformer structures (a)TRD1 (3x3x0.2 mm) (b)TRS1 (4x3x0.2 mm).



	L1/L2 [uH]	R1 [Ohm]	R2 [Ohm]	k	Lf [uH]	C1/C2 [pF]
TRS1	0.966	47.753	46.654	0.923	0.142	14.6
TRD1	1.018	40.862	39.888	0.933	0.132	7.6

Figure 2.13 – Electrical model of the coreless-transformers in Figure 2.12 with identified parameters [30].

of view, there is no interest in reducing the operating frequency of the transformer.

On the contrary an increase in the carrier frequency is needed to reduce the coil driving current and to reduce the physical dimensions. The upper frequency limit for the transformer is set by the parasitic capacitances and the coil inductance what defines a self-resonant frequency. The other limiting factor toward the high-frequency is the ability of the transceiver to source and sink current. The coils are measured by an impedance analyzer Agilent 4294A as shown in Figure 2.14, and matched to a simple equivalent circuit model because it is well adapted to low frequency, lower than 100 MHz. The

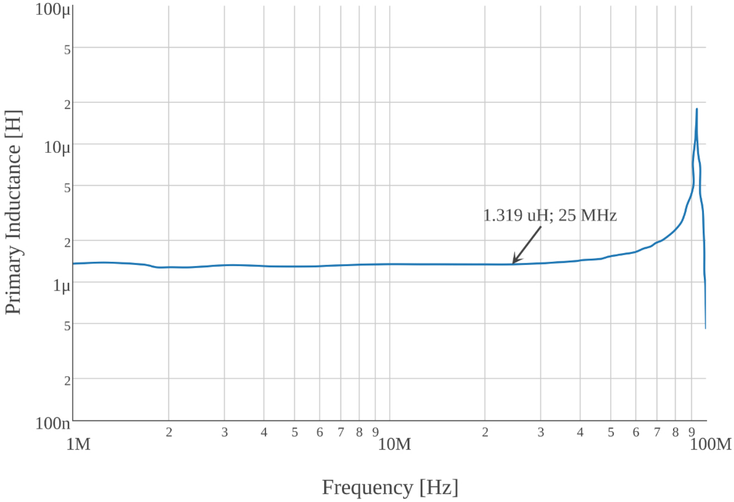


Figure 2.14 – Experimental primary inductance measurement.

full measurement protocol to identify each parameter is given in appendix .2. The main difference between double and simple layer is the isolation capacitance: this can be explained by the distance between primary and secondary windings. In the simple layer case, the windings are placed side by side, when in the double layer they are separated by an isolation layer.

2.2.2 Aging Test

As highlighted before, the isolation material in the structure (BCB) is not intended for an high-temperature application. The aging of this material is characterized by a loss in thickness (oxidation) [228]: the result is the increase in the isolation capacitance (C_1, C_2).
In order to stop this phenomenon, a chemical barrier made with a polymer,- the Parylene HT from SCS, was coated on the top of each coreless sample. Parylene reduced the oxygen impact as an aging accelerator, by making an isolation layer on the top of the sample [88].

6 samples of each coreless types are glued onto a ceramic substrate with a high-temperature glue (Duralco133) as shown in Figure 2.15(b). A Parylene coating is applied on all the area. In parallel a similar ceramic substrate with samples is fabricated to be used as a reference.

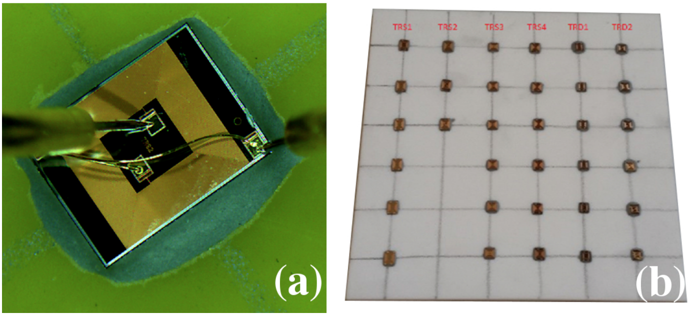


Figure 2.15 – 4 points probes for static measurement (a); Ceramic substrate and the 6 different coreless transformer types with Parylene coating (b).

To study the aging phenomena the samples are placed in a furnace with a constant temperature of 200°C. An initial reference measurement at ambient temperature was operated on all samples. Samples are measured with the same protocol. A rapid change appears at the beginning and measurements are operated every two-days, then a measurement point every week. A 4-point probe measurement with an impedance analyzer guarantees the repeatability of the measurement as shown in Figure 2.15(a)

Figure 2.16 shows the variation over 1500 h of the isolation capacitance for a

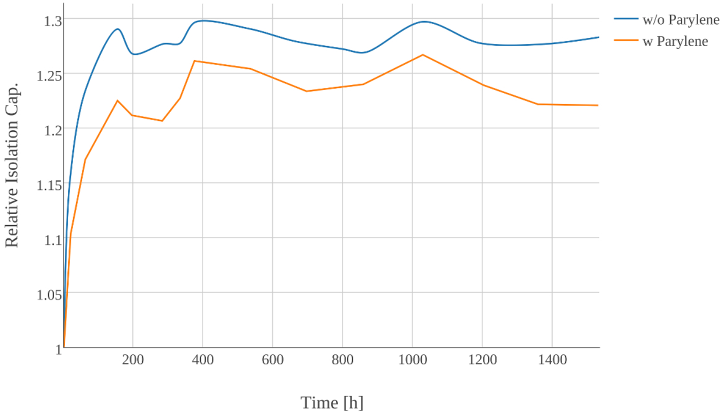


Figure 2.16 – TRS1 Isolation capacitance variation under 200°C with and without Parylene.

simple layer coreless transformer. The capacitance evolution is constant after a quick increase in the first 200 h. In the case of a single layer, Parylene does not seem to efficiently affect the aging process. The explanation for that is the fact that the both windings are on the same layer and the variation of the BCB layer barely affect the distance between them. The capacitance difference with and without Parylene can be attributed to the better dielectric strength of Parylene than air. Figure 2.17 shows the variation during 1500 h of the isolation capacitance of a double layer coreless transformer. In the case of a double layer coreless, Parylene makes a difference: the capacitance still increases after 1500 h without Parylene, when a stable value appears after 800 h with Parylene. In the case of a double layer, the BCB thickness variation doubles the capacitance value if a Parylene coating is not applied.

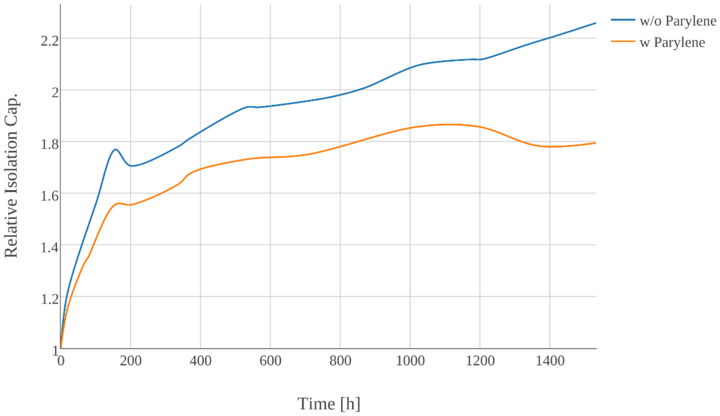


Figure 2.17 – TRD1 Isolation capacitance variation under 200°C with and without Parylene.

In comparison with the simple layer transformer coreless, the double layer shows a smaller capacitance value after 1500 h. However the stability of the single layer pushed us to choose this solution for the development of a demonstrator.

2.2.3 Design of a High-temperature Control Signal Isolation

Figure 2.18 shows the PCB board designed with a polymide 35N substrate with an ENPIG surface. Two coreless-transformers are glued to it with an high temperature glue (Duralco133), ball bonding are used to make the connection between board and chip.

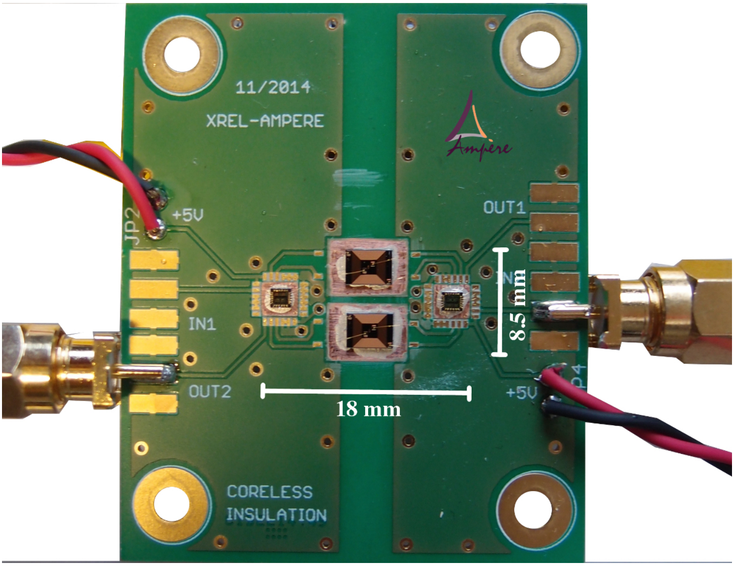


Figure 2.18 – Coreless-transformer Isolated board under testing.

Two XTR40010 SOI transceiver chips from EasiiC Xrel are used to transmit the control signal through the transformer. One NPO 100 nF decoupling capacitor is requested by those two chips. The total area for this two communication lines is about 153 mm^2. By comparison the solution with ferrite presented in the previous section needs an area of 200 mm^2.
In order to double check the Parylene effect, two boards were designed, one with Parylene one without but no difference were noticed since the single layer coreless-transformer was selected.

As shown in Figure 2.19, the signal is modulated with a basic frequency modulation (FM) and transmitted through the transformer. The modulation frequency is at 25 MHz and the maximum transmission delays measured is 90 ns at 200°C. The board was successfully tested between 25 to 200°C with a maximum supply power of 65 mW at 25°C.

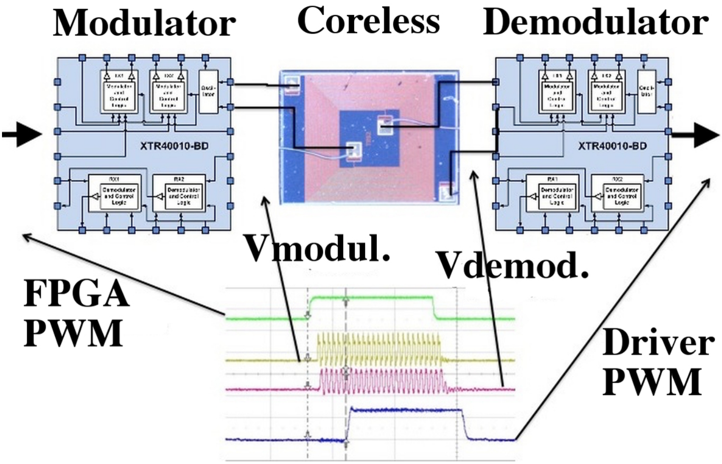


Figure 2.19 – Modulation and demodulation principle with two Xrel XTR40010 Transceiver.

2.2.4 Aging of the coreless-transformer board

In order to check if the coreless transformer structure variation does not have any impact on the final application, we repeated the same aging test as in previous section but for the full board during 600 h.

The difference in switching frequency between input and output has been used to see the impact of the coreless on the system robustness. An automatic measurement system tests every 30 minutes the input/output current and the input/output frequency. As shown in Figure 2.20, the error in percent for the frequency variation is less than 0.001 % during 600 h. The coreless transformer variation noticed if any has impact on the isolation function. The accuracy and the stability of the isolation function reach the required specifications.

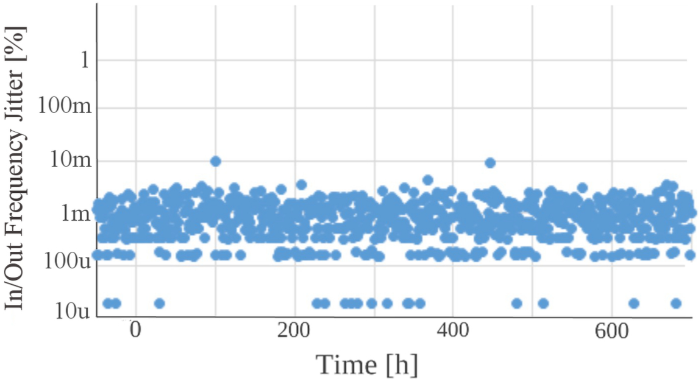


Figure 2.20 – Input/output frequency Jitter at 200°C.

2.3 A dV/dt Generator for an Accurate evaluation of Transient Impact

In the previous section, we described the isolation function for a high-temperature application. The coreless-transformer was characterized and implemented in a full operating prototype. The coreless-transformer showed a good reliability during the ageing test as good as the final PCB board.
In order to test the dV/dt immunity of this solution, a dV/dt generator was fabricated. Different isolation functions were characterized and a model of an inverter phase leg is proposed and discussed.

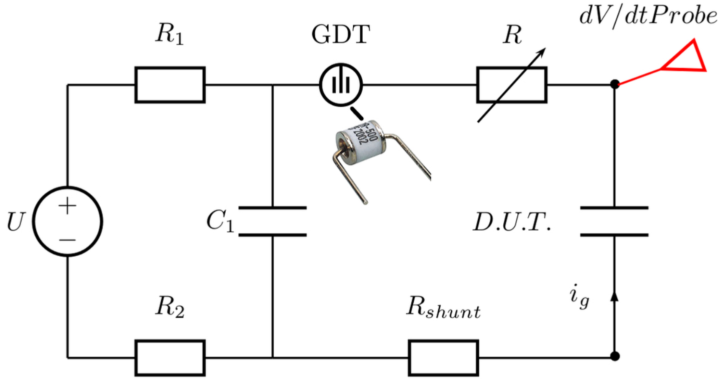
2.3.1 dV/dt Generator

dV/dt characterization is a poor topic, few papers are reporting issues about [219, 241] since the usual power conversion switching frequency stayed low enough to not be an issue. It is also interesting to see that there is no standard for the dynamic isolation testing of power electronic system: each company proposes its own test. With the WBG components and the increase in transient capability, isolation barriers have been more solicited.
More recently some testing material appeared on the market but the dV/dt capability of those stays below 50 $kV/\mu s$ [11]. This limitation is mainly due to the fact that IGBTs are used to switch the voltage. Another solution in literature gives faster transient (10 ns; 1000 V) by using parallel MOSFET transistor in an avalanche mode [133, 54]. This solution is limited by the capacitive value of the load.

2.3.1.0.1 Generator Schematic In order to have a cost-effective and easy solution for the dV/dt generation, a solution based on Gaz Surge Arrester (GSA) was developped. GSAs have a high dV/dt capability and no control signal or driver are requested. GSAs operate on the gas-physical principle of the highly effective arc discharge. From an electric point of view, surge arrester is acting as a voltage-dependent switch.

As soon as the voltage applied to the arrester exceeds the spark-over voltage, an arc is formed in the discharge region in few nanoseconds. The arc voltage is almost independent of the current thanks to a high surge current handling capability. The arc kills the overvoltage but provide a constant voltage transient independent of the load.

The circuit is presented in Figure 2.21. It is based on a Bourns-2087 Gaz Surge Arrester as a the dV/dt generator. The high voltage source includes a 4.5 uF capacitor bank, and it is decoupling from the DC source by two 1 kΩ resisitors. A resistor is put in series with the GSA for the dV/dt control. The resistor value allows decreasing the voltage slope by slowing down the di/dt. A high-voltage Lecroy ADP probe is used for the measurement of the dV/dt. The ground current is measured with a low parasitic inductance T&R shunt



$$R_1 = 1k\Omega \qquad R_{shunt} = 0.02546\Omega$$
$$R_2 = 1k\Omega \qquad GDT = Bourns - 2087$$
$$C_1 = 4.5\mu F \text{ (1.5 kV)}$$

Figure 2.21 – dV/dt generator based on a Gaz Surge Arrester.

resistor.

2.3.1.0.2 ***dV/dt* Generation** A 10 kV power supply is connected at the input of the generator and the input capacitor bank is charged until reaching the spark-over voltage of the GSA. In our case this voltage is 1.5 kV, since higher voltage means faster transient for a same GSA type.

The variable resistor is adjusted according to Table 2.2 in order to provide the requested transient voltage. As shown, the maximum dV/dt capability of our system was measured at 147 $kV/\mu s$ which is close to the GaN device capability (measured at 200 $kV/\mu s$ with the selected GaN device). As shown

Table 2.2 – Relation between serial resistor and dV/dt value for a Bourns-2087 GSA and a 100 pF load

Resistor [Ω]	dV/dt 10-90% [$kV/\mu s$]
1000	13
300	21
100	50
11	88
5	102
0	147

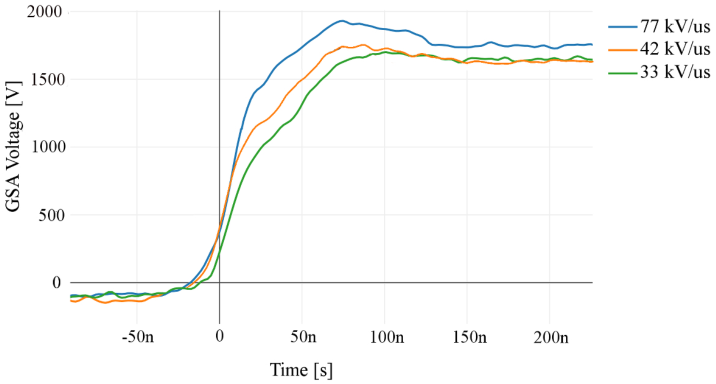


Figure 2.22 – Different dV/dt values generated by the Gaz Surge Arrester.

in Figure 2.22, the generator is able to generate transient with a constant shape, without noise or ringing. This advantage will help to have precise measurement and to cancel undesired noise.

2.3.2 Dynamic Characterization of Isolation Solutions

After the development and the test of the generator by itself, different isolation schemes were tested in order to provide a classification it with a normalized test. The goal is to determine the maximum dV/dt handled by the isolation components.
The test setup is composed by the dV/dt generator connected to the DUT, a special attention is taken to focus only on the signal isolation. In that perspective, all the power supplies are replaced by batteries and the PWM signal is generated through an optic fiber. The only way for the common-mode current generated by the transient to flow is by the isolation components under test. The DUT is connected following the schematic in Figure 2.23, the two capacitors represent the isolation barrier for the reference and the transmission line.

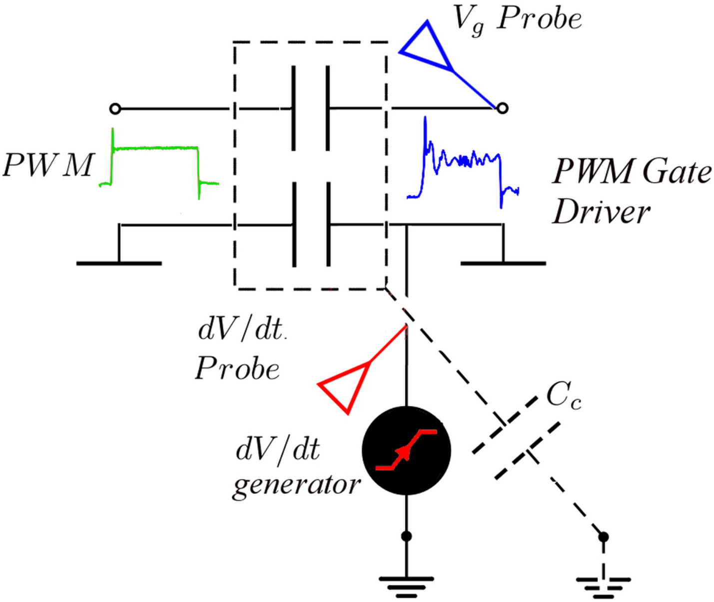


Figure 2.23 – Simplified equivalent circuit of the characterization setup with the parasitic capacitance of the DUT.

The capacitor C_c represents the coupling capacitor between the board and the ground, the common-mode current loop is closed by this point.
As shown in Figure 2.24, the generator is connected to the output node of the secondary side of the isolation in order to reproduce similar conditions as a dV/dt coming from the power device towards the driver. The transient is apply between the isolation secondary reference and the ground. This connecting point allows the generation of high-voltage transient (1.5 kV) without destroying the tested board, since references are different between them.
The dV/dt probe controls the slope of the transient and the V_g probe allows

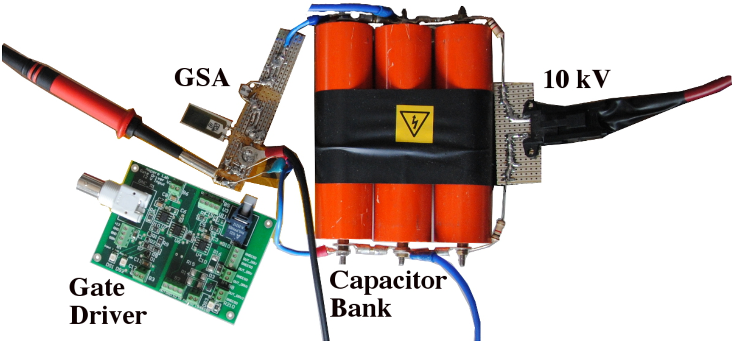


Figure 2.24 – Experimental setup.

to check the impact of the transient on the control signal. A shunt resistor is connected on the reference to measure the common-mode current generated. It is important to repeat that like for the DPT setup, measuring fast transient is only possible with high-bandwidth probes, a special care was taken in that perspective.
Logically, the test protocol consists in measuring how much current the isolation circuit is able to handle and stay stable under different dV/dt values and determine a maximum acceptance value.

2.3.2.0.1 Isolation characterization Three different types of isolation barrier are tested: an optocoupler from Vishay which represents the worst case, the coreless transformer presented in the last section and a capacitive isolation from the the market with a TI ISO721 digital isolator. All of them are implemented on the same gate driver board developed at the lab as a multi-purpose gate driver. Commercial products have a maximum dV/dt immunity given in the datasheet, with respectively 25 $kV/\mu s$ for the optocoupler and 50 $kV/\mu s$ for the TI digital isolator.

Tests have been performed, were realized with a positive dV/dt since negative and positive transient have the same effect on the logic signal according to our measurements.

As shown in Figure 2.25, the overvoltage generated by 45 $kV/\mu s$ dV/dt on the PWM signal is reaching 28 V for a 0;15 V logic signal, in the case of an optocoupler. In this case the dV/dt was destructive after few tests because the inputoutput logic buffer of the optocoupler are sensitive to overvoltage. In a similar manner, if the dV/dt happens during a low state of the logic signal, a reconduction phenomenon can be observed since the threshold voltage is over-passed. Figure 2.26 shows the common-mode current generated by a 100 $kV/\mu s$ in a capactive isolation with a measured 2 pF isolation capacitance. The maximum peak current is around 2 A and generates a 8 V peak voltage on the gate voltage.

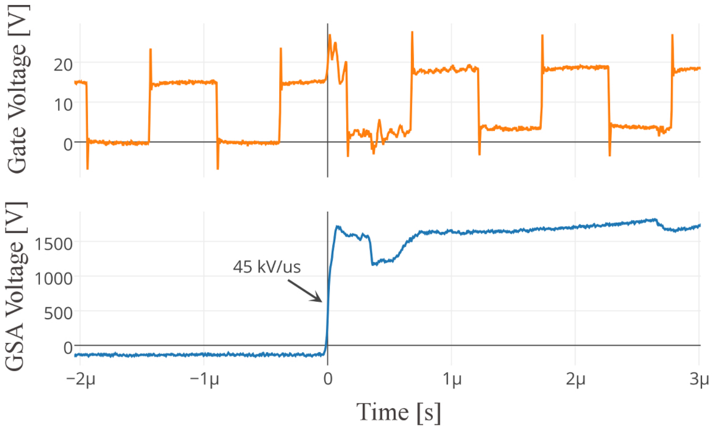


Figure 2.25 – 45 $kV/\mu s$ transient impact on an optocoupler barrier isolation logic signal.

The Figure 2.27 shows the different impacts on the gate voltage for different values of dV/dt in the case of a coreless-transformer isolation. It is interesting to see that the buffer circuit is handling the common-mode current until reaching a certain limit when it will modify the logic signal shape exponentially.

A specific issue appeared during the test: a capacitive discharge appears on the gate signal after the dV/dt, as shown in Figure 2.28. This coming from the capacitive charge between the oscilloscope connected to the board and the ground copper pad, it was resolved by a direct connection between oscilloscope

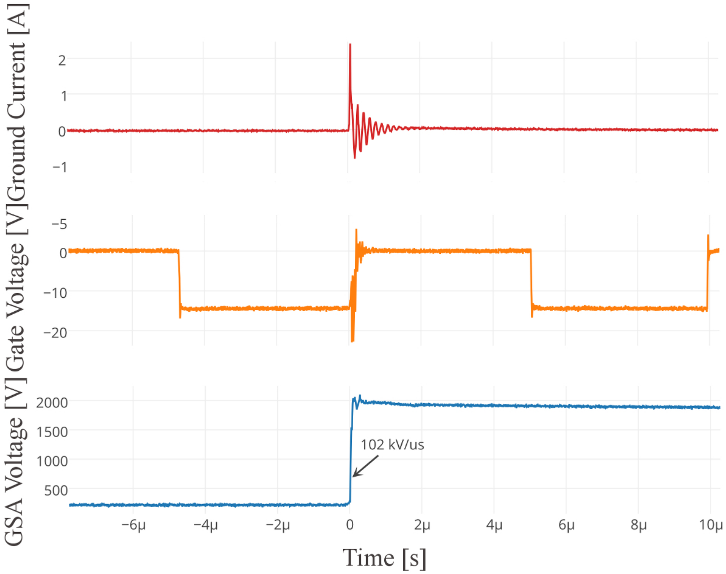


Figure 2.26 – 100 $kV/\mu s$ transient impact on an capacitive barrier isolation ISO721 logic signal and generated common mode current.

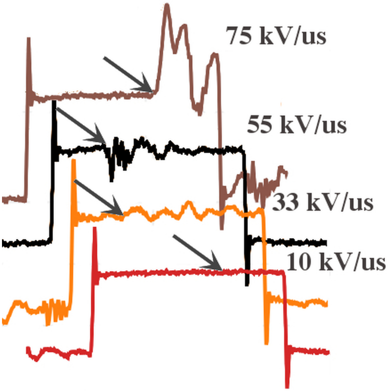


Figure 2.27 – Different dV/dt impact values on the gate voltage logic signal.

and pad in order to short circuit the coupling capacitor.

In order to summarize all the results, Table 2.3 presents the maximum dV/dt

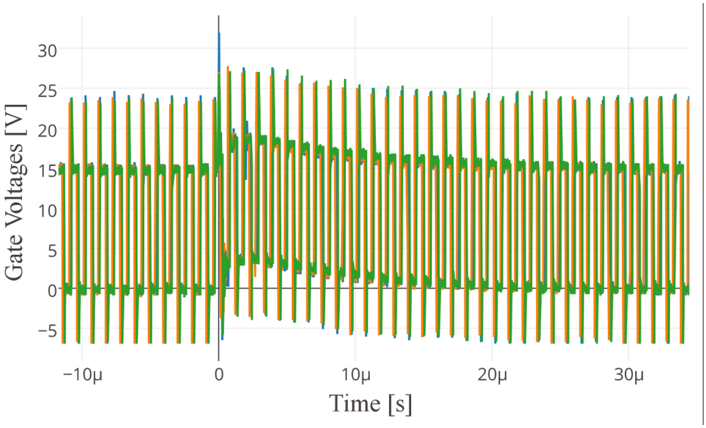


Figure 2.28 – Oscilloscope ground coupling capacitance discharging after a dV/dt.

and the measured isolation capacitance. In the case of the coreless transformer isolation, the buffer used in the transceiver has shown some trouble beyond 200 mA current peak, and a maximum current of 2.4 A destroyed the logic buffer for a dV/dt of 75 $kV/\mu s$. From the design point of view, the logic buffer used in an isolation system to transmit the signal through should accept high-peak current in order to increase the dV/dt immunity of the solution.

Table 2.3 – Summary of the maximum dV/dt acceptance for different isolation types.

Isolation Type	Max. dV/dt [$kV/\mu s$]	$C_{1/2}$ [pF]
Optocoupler	12	1.2
Coreless	65	12
Capacitive	43	2.1

According to the results, isolation capacitance is key for reducing the common-mode current since it is reducing the current path. But the immunity of the control signal can be also increased by using different modulation techniques as shown by the coreless-transformer solution.

2.3.2.0.2 Simplified Analytical Model In order to have an accurate estimation of the impact of the dV/dt on the gate voltage in a phase leg context, a first simplified approach consists to model the driver and the power device during a positive dV/dt as shown in Figure 2.29. It is assumed that the gate impedance is only formed by the internal gate resistor R_{drvOn} and an external gate resistor R_g, and the intrinsic capacitance of the GaN device C_{gd} and C_{gs} are constant under V_{gs} and V_{ds} (Section 1.3).

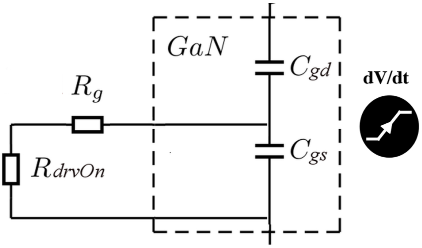


Figure 2.29 – Simplified model of the gate driver and the power device during a positive dV/dt.

$$V_{gs_{Max}} = (R_g + R_{drvOn}) * C_{gs} * \frac{dV_{ds}}{dt} * \left(1 - exp^{-\frac{dt}{(R_g+R_{drvOn})*(C_{gs}+C_{gd})}}\right) \tag{2.2}$$

Equation (2.2) presents the maximum value of V_{gs}: it can be seen that higher gate resistance value induces higher overshoot. However applying this equation to the real case does not provide a satisfying evaluation of the maximum value reached during experiment.
In [26], a small-signal analytical model of the gate voltage under high dV/dt is presented. In this model, the respective parasitic gate, drain and source inductances L_g, L_s and L_d are taken into account. The previous equation becomes :

$$V_{gs_{Max}} = \frac{dV_{ds}}{dt} * C_{gd} * (R_g + R_{drvOn}) + \frac{dV_{ds}}{dt} * C_{gd} * \left(\frac{1}{C_{gs}} - \frac{(R_g + R_{drvOn})^2}{4 * L_g}\right) * \sqrt{(L_s + L_d) * (C_{gs} + C_{gd})}$$
$$\text{with } L_g \geqslant (R_g + R_{drvOn})^2 * C_{gs} \tag{2.3}$$

From Equation (2.3), it can be noticed that the increase in the inductance value of the gate L_g induces a higher value of the spike. Moreover, the increase in the capacitor C_{gs} decreases the value of the voltage spike at the gate node. Two methods can be used to reduce such spikes. The first one is to increase the equivalent gate-to-source capacitance by adding another discrete capacitor in parallel to the gate and source terminals.

The second approach is to actively decrease the gate resistor by adding a switching device as close as possible to the gate terminal of the power device. However, in both equations, it is assumed that the intrinsic capacitances C_{gd} and C_{gs} do not vary with the applied voltage of the power device. In most devices, such as GaN HEMT, this assumption is not valid since intrinsic capacitances decreases as the applied voltage increases.

It appears, that it is more interesting to develop a global model of the converting system in order to accurately represent the different circuit interaction.

2.4 Modeling a Galvanic Isolation in a Power Stage

This section presents a simple model for the galvanic isolation in a power stage context, with a comparison between experiment and simulation. Some papers [242, 147, 82] are presenting some milestones to build a simulation model without showing a good matching between simulation and experiment. In this work some improvements of the schematic coupled with the dV/dt generator accuracy allowed a better understanding of the behavior.

In order to model the impact of the dV/dt on the isolation, a simplified schematic of the current loop in a power stage is proposed. As shown Figure 2.30, the coreless-transformer case is used in order to simulate the galvanic isolation efficiency. The schematic is presenting the high-side of a power stage isolation and the output capacitance of the driver C_{drv} is the first capacitance that the common-mode current I_{cm} is going through. The common mode current is assumed to flow from the source sense node of the power device since it is the lower impedance path (no gate resistor). The coreless is modeled by two isolation capacitance C_{iso} and the value of the transformer model are coming from Section 2.2.

The inductance L_3 is representing the connection to the transceiver, and C_{tr} the output of the transceiver buffer. L_1 and L_2 are the lead inductances representing the conduction path to the PWM logic signal. All the circuit is connect to the ground through two coupling capacitors: C_{c2} on the logic signal side and C_{c1} and C_{ds} on the power stage side. The drain-source capacitance will be neglected in the simulation since it does not impact the global circuit because $C_{ds} > C_{iso}$. The ground path is modeled by R_1 and L_4, in our case

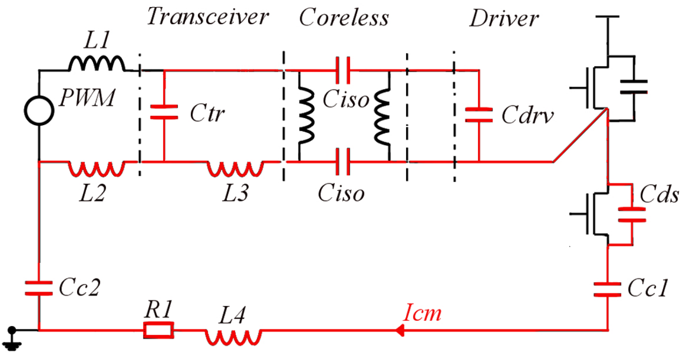


Figure 2.30 – Simplified model of a coreless-transformer isolation in a power stage configuration.

it is representing the copper plate on the bench.

2.4.1 SPICE Simulation

The previous schematic is implemented with LTspice software as shown in Figure 2.31: componenets values and impedances of the pathes were measured with an impedancemeter Agilent 4294A.
Figure 2.32 shows the simulation results for a 100 $kV/\mu s$ transient voltage

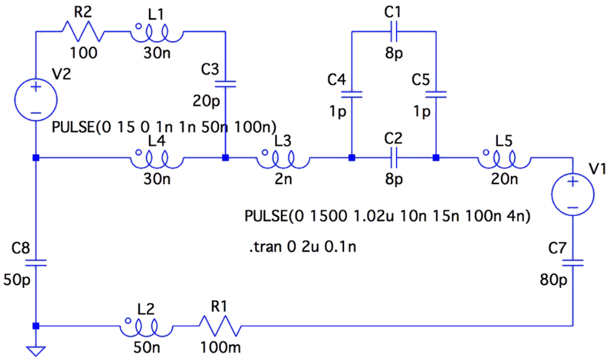


Figure 2.31 – LTspice circuit according to the schematic Figure 2.30.

for a coreless transformer galvanic isolation. The total isolation capacitance is around 15 pF and the average common mode current about 198 mA. The datasheet of the transceiver gives a maximum of 100 mA, this explain the maximum limit at 65 $kV/\mu s$.

In order to check the simulation results, Figure 2.33 is showing the experimental results from the dV/dt aggression of the coreless isolation PCB board. The results presents a really good fitting for the current curve with the same amplitude and frequency. For the gate voltage fitting between experiment and simulation, the amplitude is respected. This point is interesting for a good estimation of the maximum transient accepted. The amplitude allows to see if the threshold voltage of the power device is reached and if some improvement on the isolation has to be taken or the maximum dV/dt reduced.

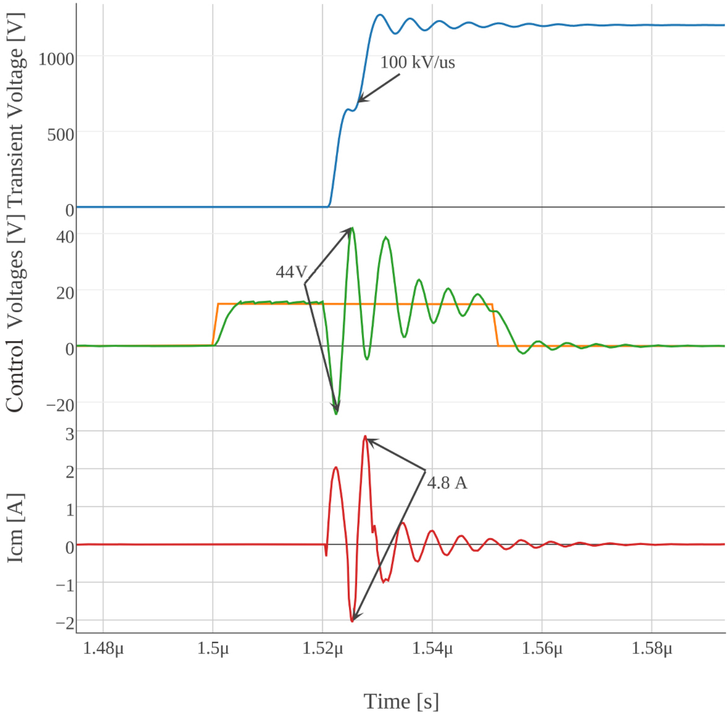


Figure 2.32 – Transient voltage, control signal voltages and common mode current.

Different simulation and experimental points were tested, and with a simple model of the common mode current path in a power stage, good fitting of the both was shown. On the range between 10 to 100 $kV/\mu s$ an maximum error

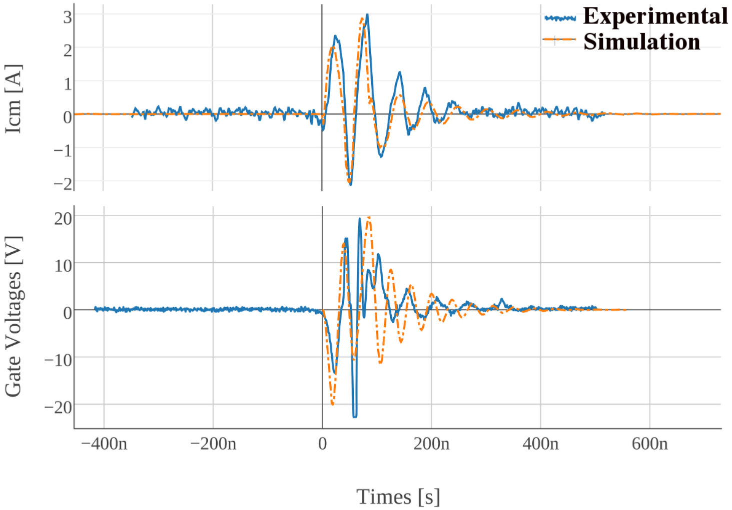


Figure 2.33 – Gate voltage and common-mode current experimental and simulatted waveforms for a 100 $kV/\mu s$.

on the voltage amplitude estimation was about 4 V. Good matching results are the result of an accurate model of the isolation component to have good results coupled with the dV/dt generator.

2.5 Conclusion

In this chapter an important work was made to develop a high-temperature coreless isolation barrier for control signal. Aging test and model development were performed in order to verify a good reliability and an accurate behavior prediction of the coreless component.

A PCB board with board on-chip assembly was performed in order to demonstrate the capability of the coreless transformer in a full control signal isolation system. In comparison with the radiative or the capacitive solutions, the coreless-transformer presents a good trade-off between isolation and high temperature capabilities.

A SPICE model of the coreless-transformer in a power stage context showed good matching results with experiment. A dV/dt generator was developed with a simple and efficient system: it was a key for the isolation barrier characterization.

However the command signal isolation is not the only one, in a power stage system, to stand the common-mode current transient. The gate driver power supply has also to benefit from good isolation capability in order to limit the common mode current path and complete the isolation barrier on the gate driver side.

Chapter 3

Gate Driver Power Supply dedicated for High-Switching Power Stage

Contents

This chapter focuses on the development of a gate driver power supply solution with the best trade-off between high-temperature capability, volume and efficiency. A solution with a SOI-chip and a PCB integrated transformer is proposed, with a decrease in volume from 195 to 6 cm^2 and a switching frequency increase from 0.2 to 2 MHz compared to the previously optimized solution.

Different locking points, such as magnetic material, assembly or integration are solved with innovative solutions.

3.1 SMPS dedicated for Gate Driver

This section gives an overview of the current power supply challenges for drivers.

The half-bridge topology is widely used in power converters and motor drives [127, 39]. The interest is motivated by the capability of the half bridge to provide efficient synchronous control of a PWM signal over a the bus voltage. However between the PWM controller and the power stage, gate drivers are required to provide fast switching and also isolation protection and function between control and power. When the bus voltage is higher than gate driver voltage, an isolated power supply is needed as shown in Figure 3.1. As shown in the previous chapter isolation barrier is a key point in fast switching converter and it was shown that parasitic inductances have an impact on the maximum common-mode current. It appears that to limit the common-mode current, the power supply has to be as close as possible to the power device for limiting the parasitic inductance and having a small isolation capacitance (<5 pF). The needs for integration seems obvious to provide an efficient solution against the increase of the switching frequency and thus fast transients.

The development of information technology is giving a tendency for slim and portable electronic appliances, what signifies the low profile, low power and high power density converters [75, 183, 162].

Increasing the switching frequency of the converter leads to a huge reduction in the size of passive elements such as magnetics (transformers, inductors) and capacitors. There is less requirement for energy storage per single switching cycle, thereby the size and cost of the converter gets reduced [85]. This enables the miniaturization of the passive components and hence the highly integrated converters [162, 154]. Apart from these advantages, increasing the switching frequency of converters enables fast dynamic response can be achieved to the rapid changes in line/load perturbations [104, 81].

According to Figure 3.2, the switching frequency is linearly proportional with the power density since for high switching frequency (> 1 MHz) there

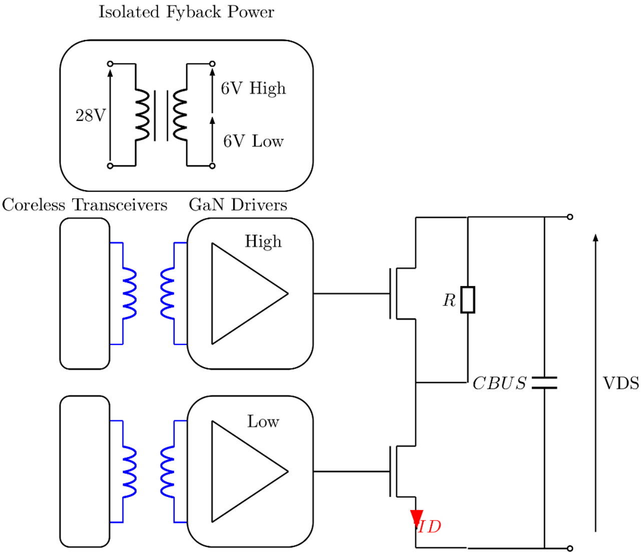


Figure 3.1 – A One-phase power stage block diagram.

is no low density point. However, it can be seen that with small switching frequency it is possible to achieve also high power density. It is manifest that another parameter different than switching frequency is affecting that.
By watching the product pictures on the graph, it can be noticed that they are using high level assembly architecture, with planar transformer or PCB embedded transformer with compact mechanical assembly.
In such low power supply application, it is obvious now, that the key to reduce the volume is not only switching frequency but also optimized assembly technics. By coupling both, it is possible to achieve high density converter in low power application.
Table 3.1 specifies the design target for the gate driver power supply and will give sense at each next section. The output voltage was fixed to address GaN Systems HEMT with a 6 V gate voltage. And the maximum power is coming from aeronautic company specification, partner of the project.

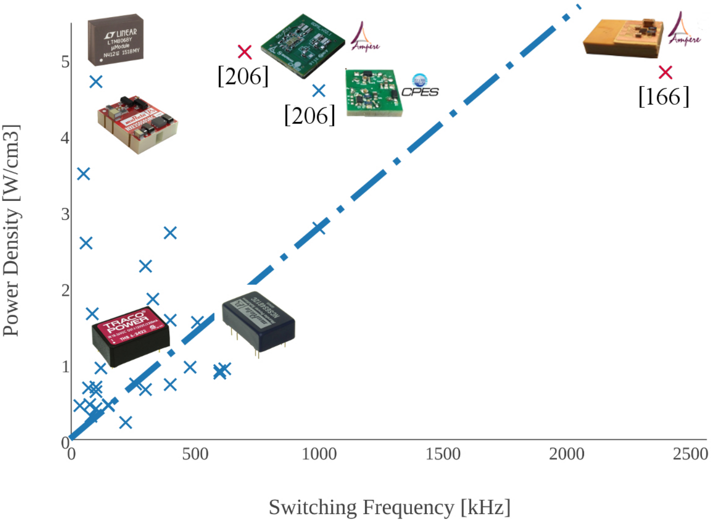


Figure 3.2 – Power density vs. switching frequency for commercial available low-power (< 5 W) converters and best lab-scale prototypes (including this work).

Table 3.1 – Specifications for an isolated gate-driver power supply dedicated to a GaN power stage for aeronautic applications.

Input Voltage	15 V (±1%)
Output Voltage	2 x 7 V
Power	2 W
Isolation Cap.	< 5 pF
Static Isolation	> 1.5 kV
Ambient Temperature	$-55; +200^{\circ}C$

3.1.1 Low Power and High-Temperature Soft-Switching topologies

As demonstrated, high-switching frequency is a good candidate for the reduction of the size of passive components at the penalty of additional switching losses in power devices. Alternatively soft-switching is an efficient technique to limit those power losses. The reduction in the current switched during transient allows a reduction of the EMI issues too [113].

The soft-switching technique, as sown in Figure 3.3, is forcing the switching at zero voltage (ZVS) or zero current (ZCS) and limit the switching losses. A resonant bank is usually associates with the power switch in order to have a spontaneous switching of the power device. This circuit can be of 4 different types, PRC, SRC, LLC or LCC by the association of capacitors and inductances. These inductances or capacitor can be discrete components on the board but also parasitic elements from existing components such as the leakage inductance of a transformer.

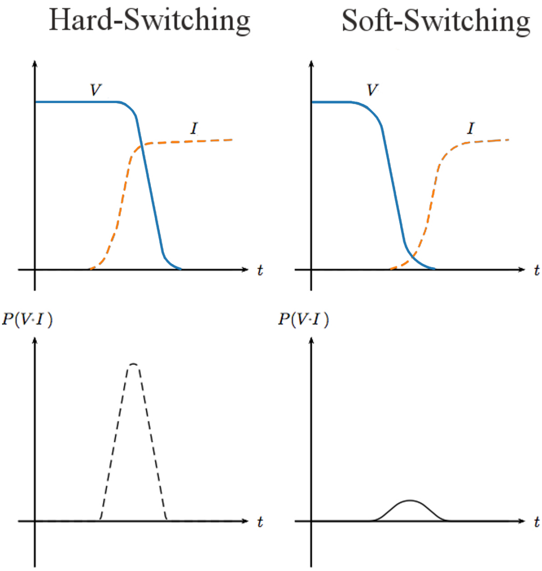


Figure 3.3 – Comparative hard and soft switching current and voltage waveforms.

The low power specification of a gate driver power supply and the small variation of the load current make specific constraint on the choice of topology. The low load variation is justified by the fact that the current requested during the switching is coming from the decoupling capacitors of the gate driver and not the power supply. The load current is mainly coming from the gate driver IC. As shown in Figure 3.4, low power converter design is mainly driven by the reduction in the number of active devices. The constraint of small components count is reinforced by the high-temperature, which increases the cost for each extra active components because of the specific assembly material and IC technology.

The most efficient DC-DC isolated power supply is then the one which offers trade-off between performances, complexity and number of components at low power. In industrial low-power applications, a suitable topology is the Flyback structure but this topology suffers from the inability to achieve high performances when the switching frequency increases due to hard-switching operation and the need for a snubber circuit to suppress the leakage inductance energy and EMI issues due to the diode reverse recovery effect.

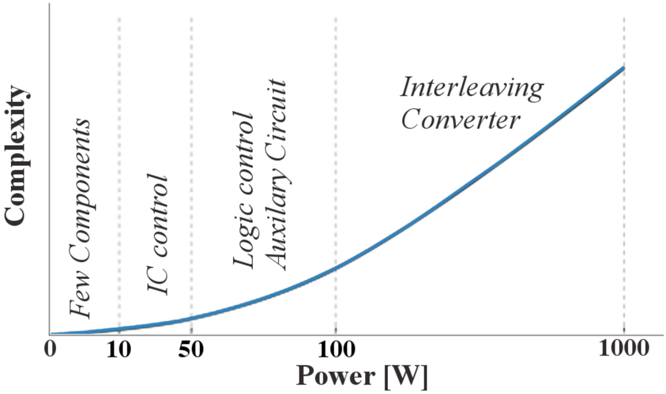


Figure 3.4 – Complexity of the power supply vs. power level.

Based on the flyback topology, a resonant active-clamp structure is performed in order to fit with the specified constraints. In the next paragraphs, pros and cons of each topology identified as a good candidate are discussed.

LLC topology As shown in Figure 3.5, one of the most popular isolated soft-switching converter is the LLC resonant converter [51, 74, 247, 236] that achieves Zero Voltage Switching (ZVS) at the primary side and Zero Current Switching (ZCS) at the secondary side. Moreover, at low input voltage, a low magnetizing inductance is needed to achieve ZVS operation.

In this condition, the magnetizing current has a significant value compared to the resonant current. This is an important impact on the conduction and magnetics losses. LLC resonant converter is therefore seldom considered at low-power and low voltage ($>$ 50 W, 100 V).

From temperature point of view, the number of active components is high due to the two rectifier by output. This affects the cost and the reliability of the power supply in harsh environment.

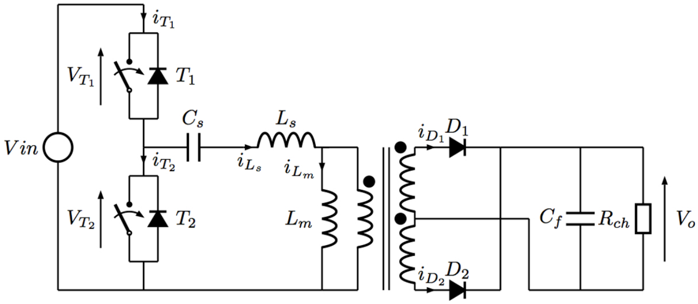


Figure 3.5 – LLC topology.

3.1.1.0.1 Quasi-Resonant Flyback topology The quasi-resonant Flyback shown in Figure 3.6 is similar to the classic Flyback [249, 195]. The difference is the discontinuous conduction mode coupled with no snubber in order to have a resonance between the leakage inductance of the transformer and the drain capacitance C_{ds} of the transistor, T_1.

This topology allows ZCS on the rectifier and ZVS on the transistor only

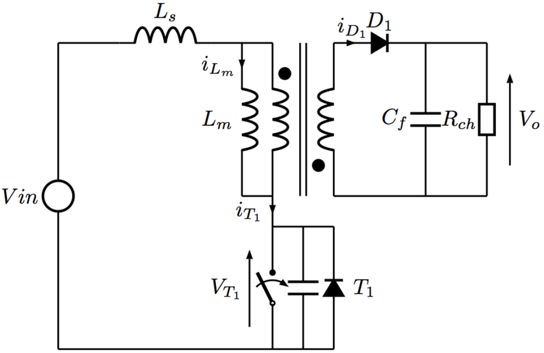


Figure 3.6 – Quasi-resonant Flyback topology.

during the turn-On transient. Turn-Off is operated in hard switching mode and the drain current spike can be twice the nominal value what adds more stress on the passive components.

$$\frac{V_{out}}{V_{in}} = \alpha * \sqrt{\frac{V_{out}}{2 * I_{out}} * L_m * f_{sw}} \tag{3.1}$$

According to the transfer function of the topology given in Equation (3.1), the stability of the topology is highly dependent on the output current I_{out}.

This means, in the case of a low power application, the stability and the resonance point will be difficult to keep. Moreover the current waveform in the transformer is not symmetric what oversizes the volume of magnetic material, key point in integration.

Active-clamp Flyback topology Initially the active-clamp technique was introduced in the Forward converter for the discharge of the transformer energy [98] and in the Flyback converter as a non-dissipative snubber [13, 103]. Moreover the active-clamp technique is a good candidate to achieve soft-switching conditions in both converters [64]. Literature covers the design of the Flyback active-clamp converter [224, 117, 118] to achieve ZVS on the transistors and at some operating point it is possible to achieve ZCS operation on the output diode to limit the reverse-recovery issues [17].

A variant of the Flyback converter with the addition of an active-clamp circuit is proposed in Figure 3.7. Here a specific design is detailed in accordance with the use of GaN transistors. This design allows the converter to operate in ZVS mode at the primary side using the transformer leakage inductance and a resonant capacitor. The specific design allows the output rectifier to be turned-Off under ZCS operation over the whole load range as in the case of a resonant converter but with less current stress on the resonant capacitor and switches. The full design procedure will be given in this chapter since this topology was selected as a good trade-off regarding the constraints of our targeted application.

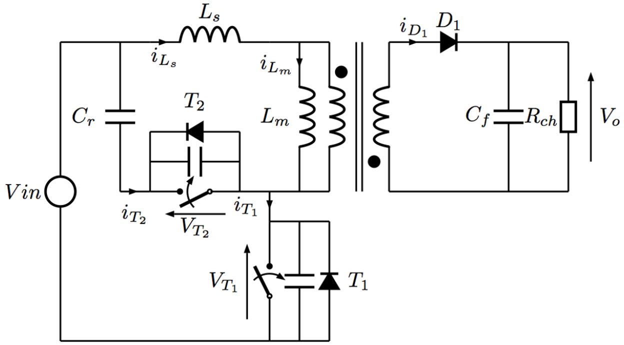


Figure 3.7 – Active-clamp Flyback topology.

Table 3.2 – *Summary of different soft-switching options*

Topology	**Benefits**	**Drawbacks**
LLC [51, 74, 247, 236]	-Soft-switching conditions for all power devices even at no load -Symmetrical and continuous operations of the transformer -Low $\frac{di}{dt}$ et $\frac{dv}{dt}$	-Oversizing of power devices -Complex control -Significant circulating power
Quasi-Resonant [160, 93, 194, 200, 151]	-Few components -No oversizing of power devices	-Soft-switching lost at light/variable load. -Complex control -[Flyback QR] Over-voltage during the turn-off.
Active-Clamp [114, 123]	-[Forward] Duty cycle higher than 0.5. -The leakage inductance energy is recycled.	-Higher voltage across the transistors.

3.1.2 Magnetic material for High-Temperature Application

Magnetic devices are an integral part of converter. It can be found as a transformer for an isolated topology or as an inductor for buck and boost converters. The role of the transformer is not limited to the basic isolation component. The design of the transformer has to take into count the isolation capabilities, the number of winding turns, the EMI constraints, parasitics such as the leakage inductance [28].
Magnetic materials are used for transformers because they can provide a good isolation and also transfer the energy with limited losses. The magnetic materials transfer the energy with a non-linear way following the $B - H$ characteristics as shown Figure 3.8(a).

Besides some special cases in a power conversion application such as current sensor, the magnetic material is used in the hysteresis cycle defined in the $B - H$ characteristics to avoid the saturation point of the cycle. In Figure 3.8(b) the $B - H$ loop with a large amplitude and DC component is

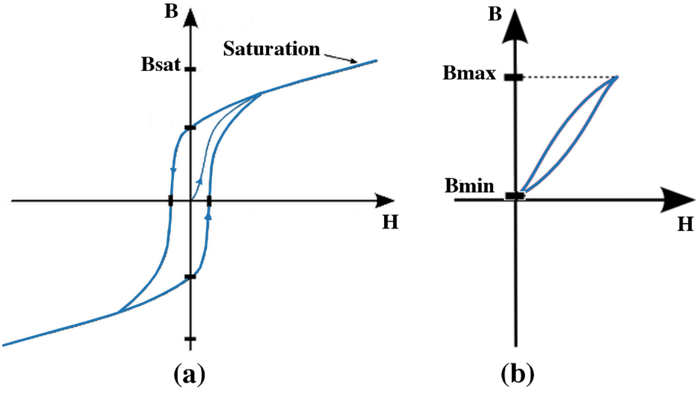


Figure 3.8 – $B - H$ characteristics [67].

specified for Forward or Flyback transformers. The energy transfer can be direct or indirect. Same kinds of transformers with less energy transfer capability is used in pulse transformer.
In all conversion applications the trade-off low losses (because of the large B-H loop) and high switching frequency (1 kHz to 10 MHz) is common. The permeability μ_r has to be kept on the frequency range too. For the temperature capability of the material, the Curie point T_c defines the maximum temperature beyond which the magnetic properties decline.

In Figure 3.9, the core losses allow a comparison between material but it is measured under sinusoidal excitation with no DC bias. This information is of limited help in power electronics applications, because the core losses depend on many aspects. DC bias [34, 141, 207], sinusoidal or square excitation [40, 41], temperature [14, 3] and AC frequency and amplitude [172] are affecting the core losses. Characterization is a key for complete and dedicated information about a magnetic material. Ampere laboratory has facilities to realize those measurement. In the power-supply application the saturation B field is a main point in order to transfer the energy through the transformer without core saturation. In Figure 3.10, presents the variation of B_{sat} versus temperature. As drawn on the figure a maximum B field can be identified in order to avoid saturation on all the temperature range.

A selection of magnetic material was performed in Table 3.3 according to their high-temperature capability. In our application, the 3F45 material for the high-frequency application (<1 MHz) and the 3C92 material for low-frequency application were used for the different prototypes. The commercial availability of those two materials was another motivation.

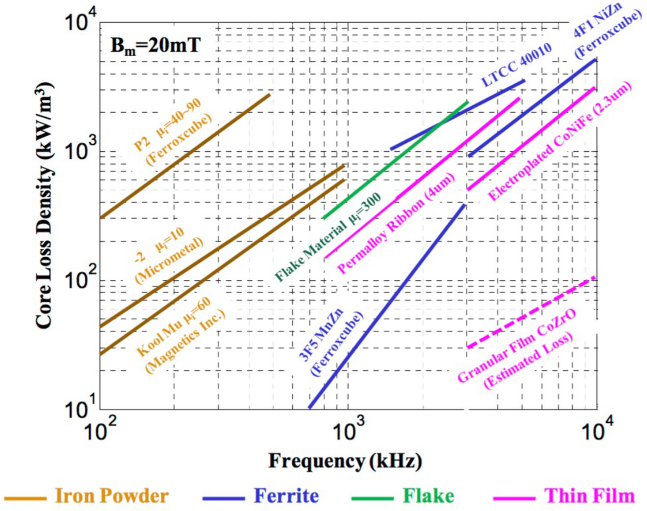


Figure 3.9 – Core loss chart for high frequency material [139].

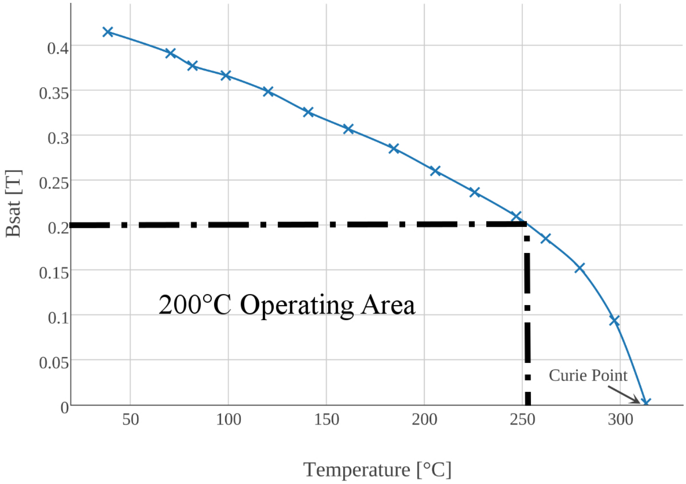


Figure 3.10 – Maximum B field in a 3F45 Ferroxcube Material vs. temperature.

Table 3.3 – Selection of High-Temperature and High-Frequency Magnetic Materials based on Figure 3.9.

Material	Tc	$\mu_{i@200°C}$	$B_{sat@25°C}$	F_{op}
Ferroxcube 3C92	280 °C	5500	540 mT	500 kHz
Ferroxcube 3C93	240 °C	5500	520 mT	1 MHz
Ferroxcube 3F45	300 °C	1250	420 mT	2 MHz
Ferroxcube 3F35	240 °C	2250	500 mT	1 MHz
Fair Rite 61	300 °C	125	NC	20 MHz
Magnetics L	300 °C	NC	NC	6 MHz

Transformer losses Transformer losses are an important part of the power-supply efficiency and the design of the transformer has to care about them. However the transformer losses are the results of physical effects, which are difficult to identifiy and estimate. An overview of the different contribution of losses and how estimate them is presented in this paragraph.
Copper losses are coming from the current circulating in the primary and secondary windings and the magnetic loss from the magnetic core.
The magnetic losses estimation is usually made based on the Steinmetz model. This model associates magnetic losses with switching frequency, temperature and a sinusoidal induction as defined in Equation (3.2) [71].

$$P_{fe} = V_{core} * f_{dec}^{\alpha} * (\Delta B)^{\beta} * (C_{T0} - C_{T1} * T_{amb} + C_{T2} * T_{amb}^{2}) \tag{3.2}$$

The coefficients $\Delta, \beta, C_{\times}$ are specific for each material and can be measured or are given by the manufacturer. As explained before, the sinusoidal excitation is not representative of the gate driver power supply application. In order to solve that issue it can be defined an equivalent frequency f_{eq} representative of the triangular excitation in a low power converter as shown in Equation (3.3) where α is the duty-cycle.

$$f_{eq} = \frac{2}{\pi^2} * \left(\frac{1}{\alpha} + \frac{1}{1-\alpha} \right) * f_{sw} \tag{3.3}$$

The copper losses are calculated with the resistivity of the copper windings. The resistance depends on the material (resistivity ρ) and the geometry of the winding (cross section A_w, wire length l_b) as shown in Equation (3.4). Also the proximity of the switching power devices can disturb the magnetic field and can reduce the effective current cross section and increase the resistivity of the material.

$$R = \rho * \frac{l_b}{A_w} \tag{3.4}$$

The skin and proximity effects are also two effects which can impact the resistivity of the winding. The skin effect is generated by Eddy currents inside the conductor which induce an opposite current in the center. The current in the winding becomes more important close to the surface. The current depth in the winding is definied in Equation (3.5).

$$\delta = \sqrt{\frac{\rho}{\pi * \mu_{cond} * f_{sw}}} \tag{3.5}$$

Equation (3.4) and Equation (3.5) give a good estimation if there are used correctly. The FEM software coupling with them allows a good 3D modeling of the different physical effects detailed before. Also in low power applications (<10 W) the Eddy current effects in copper are negligible and loss are dominated by copper and magnetic losses. The skin and proximity effects will be neglected.

Planar Transformer The classic transformer with a mechanical core in comparison with a planar transformer presents drawbacks. Especially with the emergence of the soft-switching power supply topologies, the reproducibility of the transformer in order to have constant parasitic elements (magnetizing and leakage inductances) has became an important point. This point can only be ensured with PCB windings of the planar transformer.
The volume optimization of the transformer with the increase of the switching frequency can be fully obtained with the planar transformer as demonstrated in [132] also shown in Figure 3.11. Another interesting point of the planar structure is the larger footprint area, which allowed a better thermal dissipation [173] up to 50% for a same volume. However this larger footprint is a penalty for the integration and 3D assembly are requested to minimize the volume.
Magnetic core for planar transformer are now well developed, and planar solutions are used in high-grade industry products.

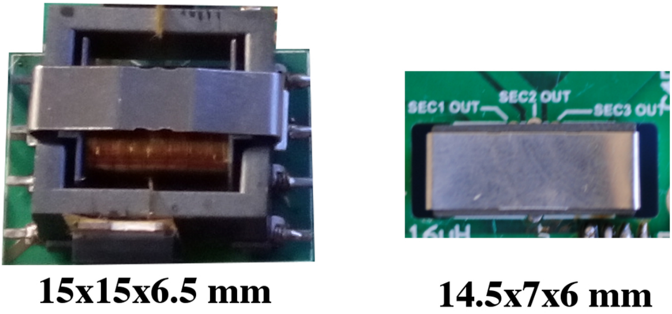


Figure 3.11 – EFD15 core transformer and ER14.5 core planar transformer for a 3 W, 200°C power supply.

As highlighted at the beginning of this section, the transformer has to respect EMI constraint. However EMI perturbations can be from different type and different standard can be applied. In the next section, the aeronautics standard is detailed due to the application field of this work.

3.1.3 EMI

Due to the context of the study, the aeronautics standards have to be respected. Aeronautic standards are ones of the most restrictive one to guaranty the reliability and safety in a plane. Moreover, the increase in the number of electrical systems in the aircraft is increasing the harmonic levels on the bus voltage [23].
In the civil aeronautic fields, the conduction eletromagnetic interference (EMI) standard is the DO160 [4] and it gives especially the maximum noise level allowed on a specific frequency range as shown in Figure 3.12.
EMI issue is a major concern in complex system or embedded system such as an aircraft or a car, and EMI filter design has became a challenge in high density converters to optimize the volume and the filtering capability. EMI interference between two equipments can be separated in two types: the conducted noise and the radiated noise and quantified by a frequency analysis of the converter input current signal.

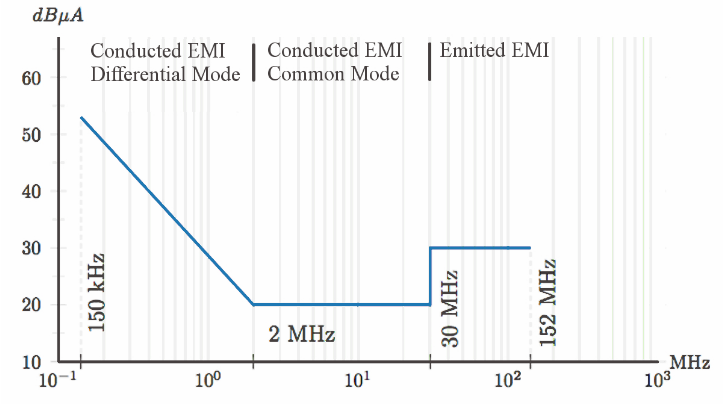


Figure 3.12 – Maximum EMI noise level from the DO160 standard [4].

As shown in Figure 3.12, the frequency range is expand between 150 kHz to 152 MHz and is not continuous on all the range. It can be separate in 3 different types as following detailed :

- 2 kHz to 2 MHz: A differential current comes from the power device switching. It is circulating between the two input wires. It can be reduced by L-C input filters (inductance and capacitor filter).

- 2 MHz to 30 MHz: The common-mode current, it is induced by fast dV/dt transients. A common-mode current is flowing to the ground and can be eliminated by a coupling capacitor between the transient point and ground and a coupling inductor placed at the system input.

- 30 MHz to 152 MHz: This perturbation is not conducted as a current but emitted and can be measured by antennas. The perturbation can be electric or magnetic and emitted by the converter all around it. The only solution to control it is a shield connected to ground of the converter such as a metal box or a copper plate.

It can be seen that power supplies are impacted by the three different types which makes it a really constrained system.
Another tricky point in the high-temperature converter is the selection of the passive elements and capacitors present a difficult part because of the low availability of efficient material with stable properties. This point is discussed in the next section.

3.1.4 High-Temperature Capacitor Selection

According to [182], for low voltage applications (< 50 V) and high-temperature ($200°C$) application, two types of capacitor are available: ceramic and silicon. The capacitance value is highly dependent temperature, the voltage and the frequency and requests characterization before using specific material in a high-temperature application.

Ceramic Capacitors

- X7R material shows high variation in its intrinsic proprieties with the temperature and voltage. The dielectric has a ferroelectric behavior, highly affected by temperature. For a 100 V voltage, the capacitance decreases by 10% and the capacitance can loose up to 60% of the initial value at $200°C$. The advantage of the material is that high value capacitor ($>$ 1 uF) are available even at $200°C$. An over-sizing of the capacitor has to be decided according to the application.

- BNT For this ceramic material sold by Novacap [149] is a new chemical compound including some Na in the dielectric and the result is an improvement of the stability in temperature. The capacitance decreases by 10% at $200°C$ and the ceramic still offers high capacitance value.

- NPO from SRT Microceramic [8], presents the best stability in temperature compared with the previous one with 2.5 % variation, as measured for our application [166]. However, the NPO ceramic material has a low volumic density: the result is low available capacitance value (below 200 nF) or for a custom capacitor, a large footprint package.

Figure 3.13 gives a summary of the relative capacitance value variation for 3 ceramic capacitor types.

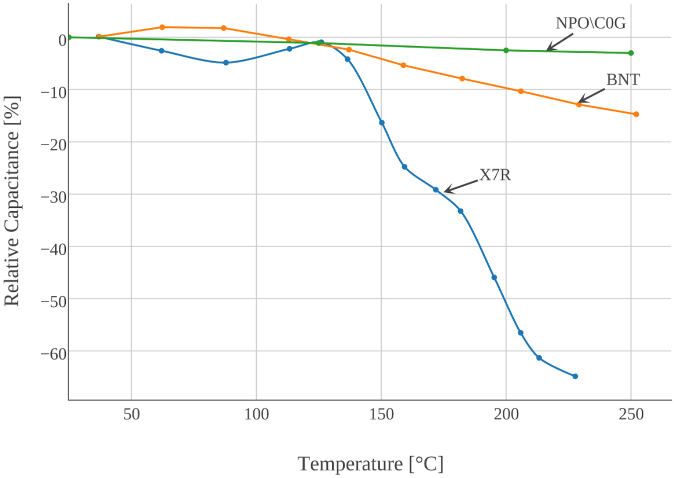


Figure 3.13 – Relative variation of the capacitance for a ceramic X7R (PCI-X7R), BNT and NPO at 10 kHz [182, 166, 8, 149].

IPDiA Silicon Capacitor has been developed to integrate large capacitance values in a CMOS process. They consist in deep trench in the dielectric material to increase the surface of the electrode. The high stability in temperature and the high integration capability [146] make an attractive solution for low voltage applications. In commercial available products the capacitance value does not exceed 100 nF and 30 V capability, but lab scale prototype shows higher rating [36, 218] up to 4.7 μF. As shown in Figure 3.14, IPDiA capacitors present a positive coefficient in temperature and the isolation resistance stays around 1 GΩ.

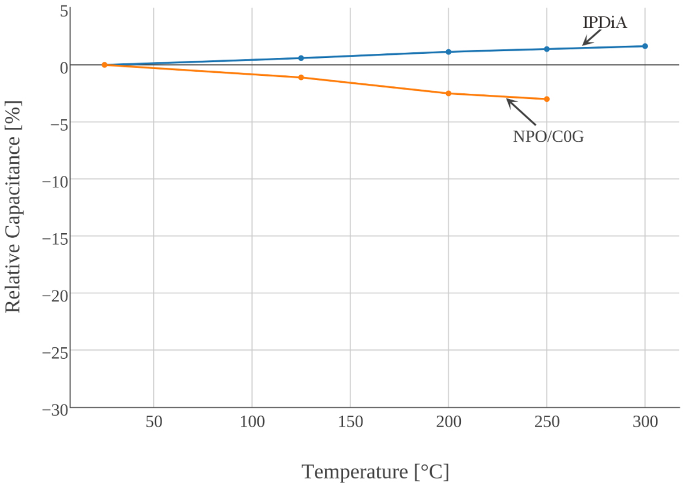


Figure 3.14 – Relative variation of the capacitance for a silicon IPDiA XTSC capacitor [36, 218] .

3.1.5 Power Supply Integration Challenges

The integration challenges are concerning different parts of the power supply. It can be the assembly or the passive components or the increase in the frequency like explained before. Different trends have been followed especially on the assembly side. It is interesting to take a look at them in order to focus the work.
Integration of passive components is a key enabler for high-power-density power supply [169, 170]. The low-cost printed circuit board (PCB) is the most widely used substrate material in electronic applications. The PCB material selected as the substrate material to embed a high power-density converter is mainly considered because of its capability for high-volume production using standard lamination process. The use of wide-band gap power transistors switched above 1 MHz in a soft-switching topology, is favorable to reduce the size of passive components and thus to make it possible to embed passives into PCB substrate [201, 18].
Two methods for fabrication of PCB embedded transformers have been reported in [125, 16, 44, 164, 144]. The first approach introduces the use of a toroidal-shape core inside a PCB. The conductive vias and traces used as windings are wrapped around the core formed by standard etching, drilling and plating processes.

However, the reliability of the assembly against temperature variation is compromised due to the large number of winding vias. Additionally this structure with the external windings generates a significant magnetic field emission, which cannot fit with the aeronautic standard.
The second method is to pot the soft magnetic composite materials around conductive winding for the transformer fabrication. The transformer is connected by pin connection in a PCB stack with the active layer. But the low operating temperature of this soft magnetic material makes it not suitable for high-temperature ($200°C$) applications.

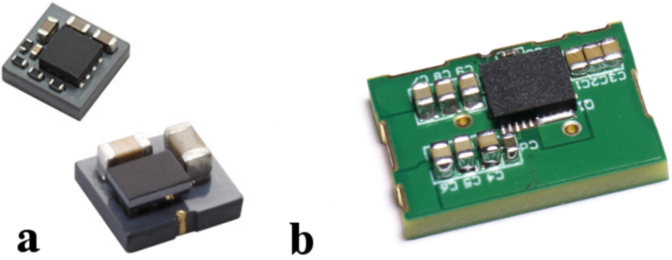


Figure 3.15 – Non-isolated LTCC inductor integrated POL converters a) Murata LTCC power supply [143]; b) CPES POL module with LTCC [245].

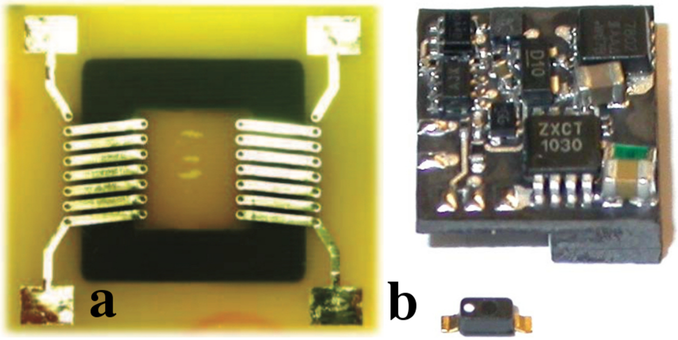


Figure 3.16 – a) PCB integrated EMI Filter with coupled inductor [16]; b) Integrated flyback dc-dc converter built using ferrite-based LTCC materials [184].

A series of studies have been performed on the realization of multi-megahertz integrated Point Of Load (POL) converter with LTCC planar inductor and

GaN devices [201, 245, 81]. Figure 3.15(a) presents the Murata's Micro DC-DC converts, which uses a LTCC inductor with a Flip-Chip IC on top [143] and Figure 3.15(b) shows a LTCC ferrite planar inductor and assembled POL module working at 5 MHz.

Nevertheless, a few papers deal with the integration of fully isolated converters. Figure 3.16(a) demonstrates a PCB integrated EMI filter with two coupled inductor with a toroidal core [16]. Figure 3.16(b) presents a LTCC transformer for a high-voltage Flyback application. The transformer allows a low frequency switching frequency and the measured isolation capacitance is around 30 pF [184, 185]. [131] presents a PCB integrated flyback transformer optimization for a 1 mm thin PFC rectifier without any experimental results.

Trends in Integration of Commercial Products According to Table 3.1, our application is low power and requires an isolation capacitance as small as possible. The volume of the gate driver power supply has to be optimized to reduce the global volume and limit the common-mode current in the converter system.

Figure 3.17 is giving the isolation capacitance of commercial and labs scale products and details the switching frequency and the maximum junction temperature in order to give a large overview about low power converter. It can be seen that there is really large (>100 pF) isolation capacitance converters due to the technology used where a coupling capacitor between primary and secondary is voluntary introduced such as Gaia converter [5].

Another category of products is characterized by a really low isolation capacitance but with a small power density. Usually it is power supply dedicated for medical application such as the Traco product [6]. And then, there is the last generation power supply such as the Linear Technology products [10] which are using an advance integration assembly with a very low capacitance.

In the following part, a focus is made on two selected commercial products, the LTM8068 and the Murata NXE2. They have respectively an isolation capacitance of 13 pF and 2.8 pF and one on the best power density of the market. The characteristics of the power supplies are given in Table 3.4.

Both converter are using an encapsulated package. Murata converter is using a tore integrated in the PCB as shown in Figure 3.18. The tore is not glued, so it can be assumed that the process is using a PCB mechanically etched where the tore is placed and the top circuit is laminated in order to close the PCB. On the other hand, the Linear Technology converter is using a wounded transformer with a central leg soldered on a laminate substrate and all in an encapsulated package using ball-bounding connection as shown in Figure 3.18. Both products are following the rules of simplicity applied in industry for low

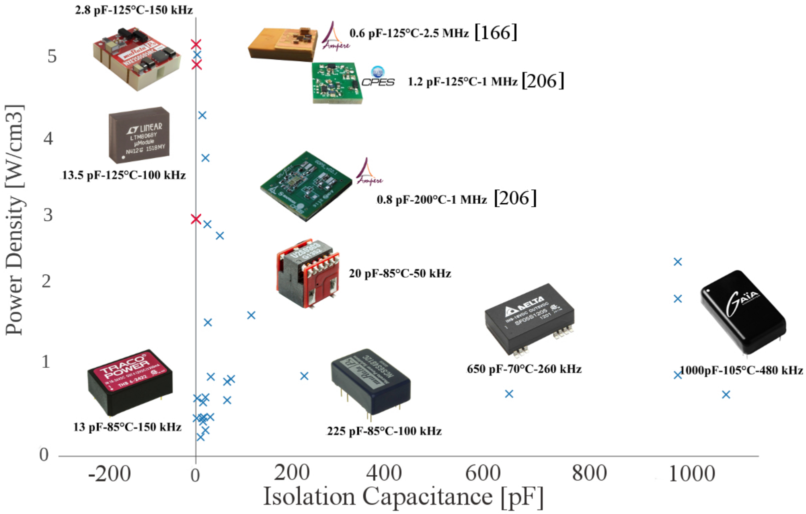


Figure 3.17 – Power density vs. isolation capacitance for commercial available low-power (< 5 W) converters and best lab scale prototypes (including this work); Isolation capacitance, max. junction temperature and switching frequency are given for each references.

Table 3.4 – LTM8068 and NXE2 power supply parameters from measurement and [9, 10].

	LTM8068	Murata NXE2
Power	2 W	2 W
Isolation Cap. (Meas.)	13.5 pF	2.8 pF
Efficiency Max. (Meas.)	70%	72%
Switching Freq.	250 kHz	130 kHz
Regulated	Yes	No
Output Var. (Meas.)	1.2%	11.5%
Protection (Meas.)	Yes (356 mA)	Yes (246 mA)
Size	11.35x9x4.92 mm	12.5x10.41x4.36 mm

power application. They are both using a flyback topology in order to limit the number of active devices and to reduce the footprint. The footprint is fixed by the size of the transformer.

Both products are providing one voltage output, what makes the products not suitable for a gate driver power supply in an inverter application with a high-side and a low-side. Besides the maximum junction temperature is given at 125°C and does not fit the temperature requirement.

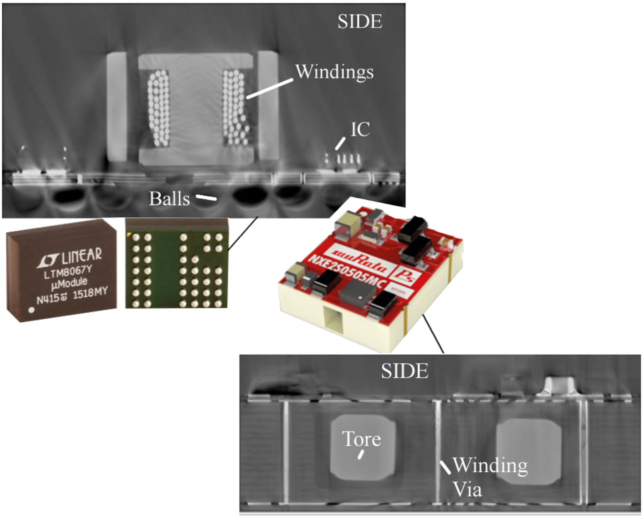


Figure 3.18 – Xray picture of the side and top cross-section of the LTM8068 and NXE2 power supplies.

3.1.6 Conclusion

In this first section, an overview of the different issues linked to the development of a gate driver power supply were presented. The integration challenges and especially the integration of the magnetic devices were detailed and the last advance packaging techniques explained.

The trends in high temperature and low power applications are not really addressed in literature, but the different techniques used for low temperature can be adapted. The active-clamp Flyback is identified as a good candidate is presented in the next section with a specific resonant mode. The design with a specific GaN transistors soft-switching process is detailed in the next section.

3.2 High-Temperature GaN Active-Clamp Flyback Converter with Resonant Operation interval

The general impression produced by this state of the art in the previous section is that there is no ideal topology. Currently it is difficult to reconcile, in a single topology, high efficiency and simplicity. To solve the low power and high efficiency problem, it is smart to combine the various types in order to accumulate their advantages.

The ideal converter achieves ZVS on the primary side and ZCS on the secondary side with a good use of the transformer where the power stored in the leakage inductance is recycled. All these features have to be summarize in a single topology that has a smaller number of components with a simple control.

Figure 3.19 shows the schematic circuit of the proposed converter. This topology is a variant of the Flyback converter with the addition of an active-clamp circuit composed of an auxiliary switch, T_{S2}. A clamp capacitor, C_r, acts as a resonant capacitor because it is associated with the leakage inductance of the transformer represented as L_r. This addition allows the converter to operate in ZVS using the transformer leakage inductance and the resonant capacitor.

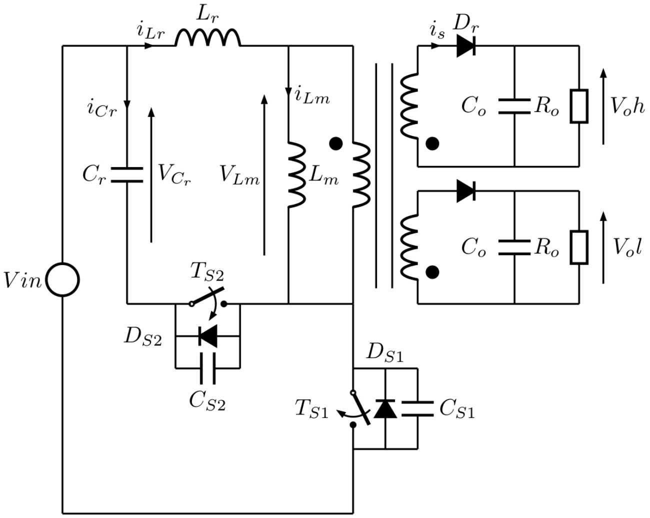


Figure 3.19 – Double-output Active-clamp flyback power supply.

One of the particularity of the resonant design as proposed, is a specific design which allows the output rectifier to be turned-Off softly in ZCS operation over the entire load range from 0 to 2 W.
In the next section the design of the resonant bank is given with a detail of each

3.2.1 Resonant interval of Operation

In this section, soft-switching conditions are presented to design the Active-clamp Flyback converter and to improve its efficiency. ZVS operation of the switches and the output rectifier ZCS conditions are derived using Equation (3.6) and Equation (3.12). This topology will be able to achieve soft-switching on T_{S1} and T_{S2} even at light load, what is a real benefit for a gate driver power supply.

3.2.1.1 Active-Clamp Flyback topology Operation

The steady-state operation of the converter includes 7 phases in one switching period, T. Figure 3.20 depicts the main waveforms and the operational intervals in the proposed active-clamp Flyback converter. Some assumptions are introduced:

- Dead-time is oversized between high-side and low-side power switch.
- The output capacitor value is large enough to neglect the voltage ripple.
- The resonant capacitor voltage, V_{C_r}, is equal to the magnetizing inductance voltage, V_{L_m}, because of $\frac{L_m}{L_m+L_r} \approx 1$. Which means that the resonance is dominated by the magnetizing current.

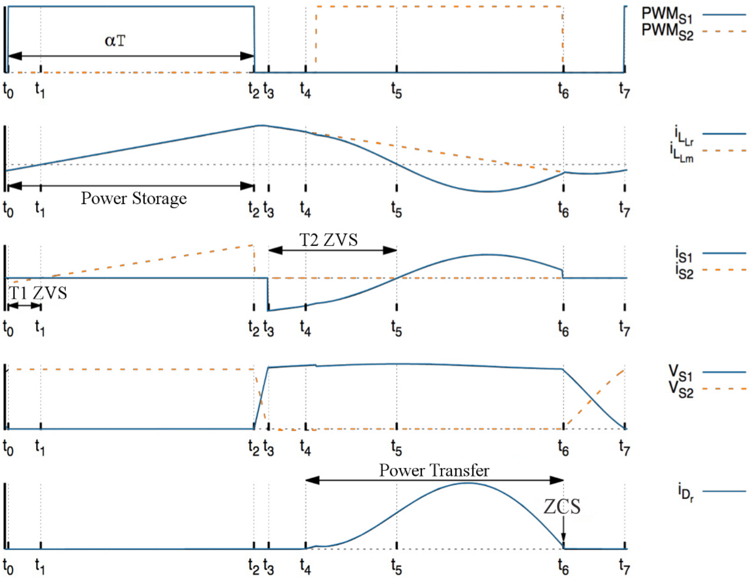


Figure 3.20 – Active-clamp Flyback main ideal waveforms in steady-state operation.

Interval 1: Inductance charging, $t_0 < t < t_1$
At t_0, the rectifier is blocked and the magnetizing current i_{L_m} is negative and will flow through the body diode of T_{S1}, resulting in a positive voltage across the magnetizing inductance, L_m. $i_{L_m}(t)$ is then approximated

$$i_{L_m}(t) = \frac{V_{in}\frac{L_m}{L_m+L_r}}{L_m}(t - t_0) + i_{L_m}(t_0) \tag{3.6}$$

ZVS condition is realized due to the body diode conduction of T_{S1}. The gate signal of T_{S1} should be applied during this interval 1.

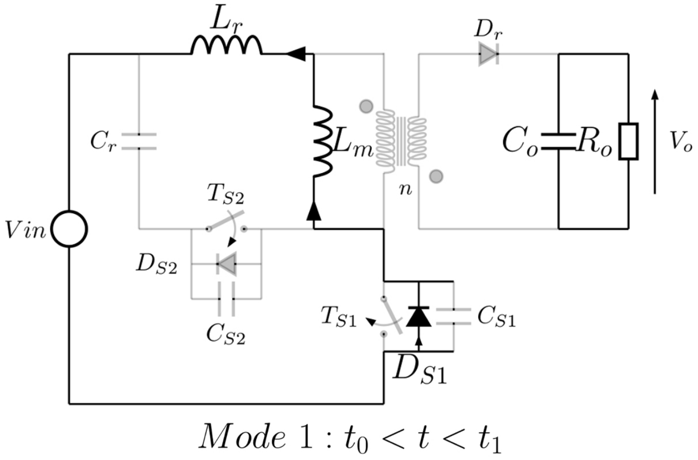


Figure 3.21 – Interval 1 of Active-Clamp Flyback topology operation.

Interval 2: Inductance charging, $t_1 < t < t_2$
At t_1, the magnetizing current reaches zero and T_{S1} is softly turned on. During this interval, the magnetizing current, i_{L_m}, still increases with the same slope as in interval 1.

This interval ends at t_2 when T_{S1} is turned Off. Hence, $t_2 - t_0 = \alpha T$.

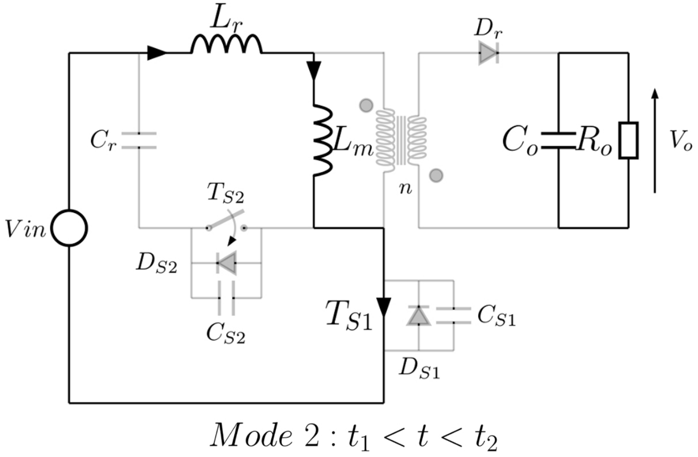


Figure 3.22 – Interval 2 of Active-Clamp Flyback topology operation.

Interval 3: Dead-time, $t_2 < t < t_3$
At t_2, T_{S1} is turned-Off. The magnetizing current, i_{L_m}, which is equal to the resonant current, i_{L_r}, acts as a constant current source because of a large L_m. Similarly C_r is large enough and acts as a constant voltage source, V_{cr}.

When T_{S1} is turned-Off, the drain-source parasitic capacitance of T_{S1} is charged to $-V_{Cr} + V_{in} \approx \frac{V_o}{n} + V_{in}$ and the drain-source parasitic capacitance of T_{S2} is discharged (0V). For part of the dead time duration, capacitances C_{S1} and C_{S2} will be respectively charged and discharged with the following currents and voltages

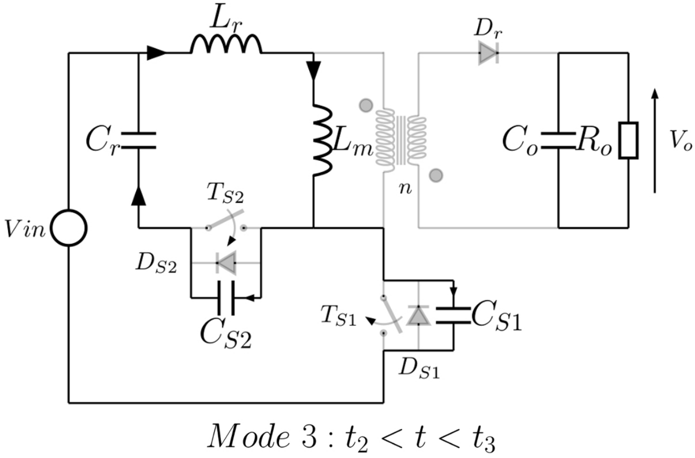


Figure 3.23 – Interval 3 Active-Clamp Flyback topology operation.

$$i_{C_{S1}} = i_{L_m} + i_{C_{S2}} \tag{3.7}$$

$$V_{S2} = (-V_{Cr} + V_{in}) - V_{S1} \tag{3.8}$$

Drain-source capacitances of T_{S1} and T_{S2} (C_{S1} and C_{S2}) are assumed to be equal ($C_{S1/2}$) despite the difference in voltages. $(-V_{Cr} + V_{in})$ is a constant voltage source over interval 3 thus $\frac{dV_{S1}}{dt} = -\frac{dV_{S2}}{dt}$. Therefore the duration of the charge of C_{S2} and discharge of C_{S1}:

$$t_{Ch_{C2}} = t_{Dis_{C1}} = \frac{-V_{Cr} + V_{in}}{i_{L_m}}(2C_{S1/2}) \approx \frac{\frac{V_o}{n} + V_{in}}{i_{L_m}}(2C_{S1/2}) \qquad (3.9)$$

This interval ends when the capacitances are fully charged or discharged.

Interval 4: Resonant phase, $t_3 < t < t_4$
At t_3, C_{S2} is fully discharged thus T_{S1} is in Off-state. Therefore, the inductor current, i_{L_r}, is flowing through the body diode D_{S2} thus $V_{L_m} \approx V_{C_r}$. During this interval, the voltage across the magnetizing inductance doesn't allow the transfer of power to the secondary side ($V_{C_r} > -\frac{V_o}{n}$). In other words the rectifier diode is blocked. L_m is thus free to participate to the resonance. It will form a resonant circuit where L_m is in series with L_r and both resonate with C_r. The voltage across the magnetizing inductance decreases and this interval ends when the rectifier is turned-On when $V_{L_m} \approx V_{C_r} \approx -V_o/n$.

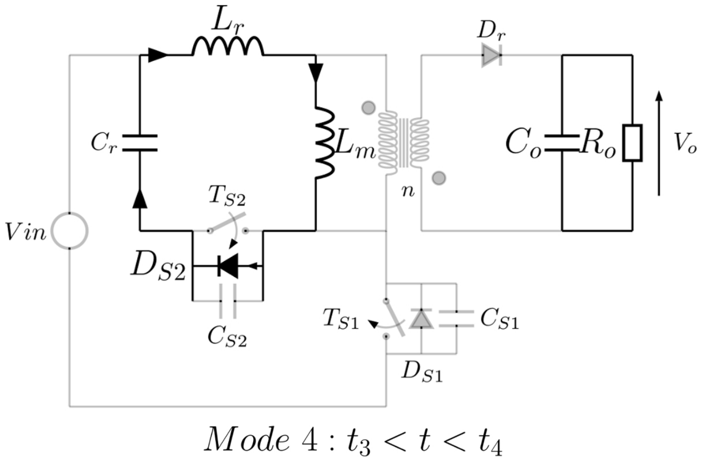


Figure 3.24 – Interval 4 Active-Clamp Flyback topology operation.

Interval 5: Power transfer, $t_4 < t < t_5$
At t_4, V_{L_m} reaches $-V_o/n$. The primary transformer voltage is clamped to $-\frac{V_o}{n}$. Therefore i_{L_m} linearly decreases because of the output voltage reflected to the primary side. As a consequence, L_m no longer participates to the

resonance. During this interval, the circuit operates like a series resonant converter with a resonance between L_r and C_r.

This new resonance will turn-On the secondary side diode, D_r, to conduct and the output current, i_s, begins to increase. It comes

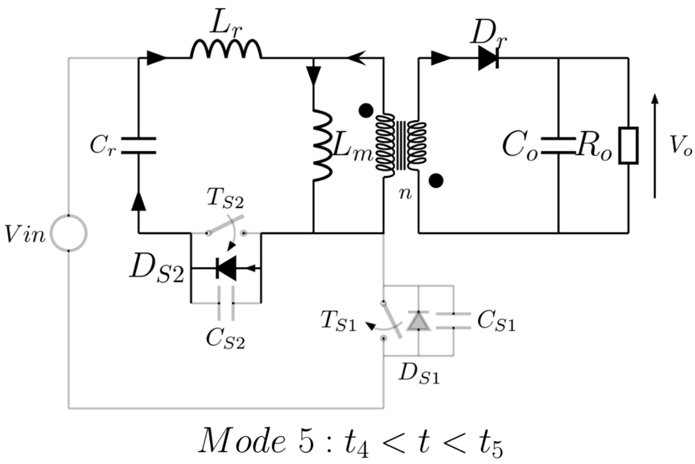


Figure 3.25 – Interval 5 Active-Clamp Flyback topology operation.

$$i_{L_m}(t) = \frac{-V_o}{nL_m}(t - t_4) + i_{L_r}(t_4) \tag{3.10}$$

$$i_{L_r}(t) \approx i_{L_r}(t_4)\cos((t - t_4)\omega_{M5}) \tag{3.11}$$

$$i_{D_r}(t) = \frac{i_{L_m}(t) - i_{L_r}(t)}{n} \tag{3.12}$$

Where $\omega_{M5} = \frac{1}{\sqrt{C_r L_r}}$ and n is the transformer ratio.

During interval 5 ZVS conditions are realized due to the conduction of the body diode of T_{S2}. And the gate signal of T_{S2} should be applied. This interval finishes when $i_{C_r} = i_{S2}$ reaches zero.

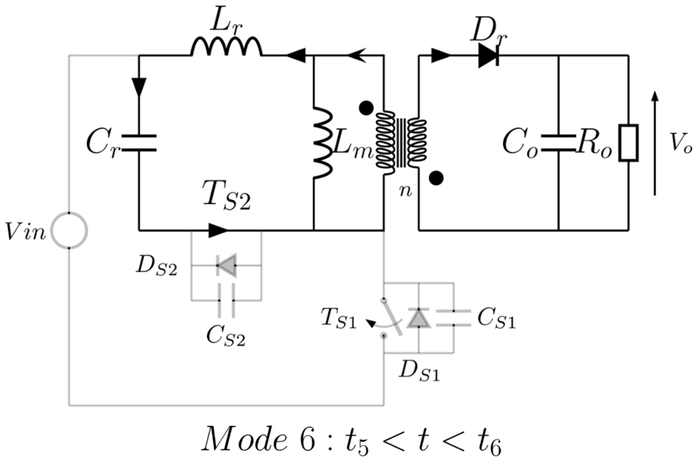


Figure 3.26 – Interval 6 Active-Clamp Flyback topology operation.

Interval 6: Power transfer, $t_5 < t < t_6$
At t_5, the current i_{C_r} reaches zero. T_{S2} is softly turned-On. During this interval, the state equations of interval 5 are still valid. interval 6 ends with the ZCS commutation of D_r, when the magnetizing current, i_{L_m}, is equal to the resonant current, i_{L_r}.

Interval 7: Dead time, $t_6 < t < t_7$
At t_6, T_{S2} is turned-Off. This interval is equivalent to interval 3 with different initial conditions on current levels.

The structure is named Flyback but as shown in Figure 3.21 to Figure 3.27 the waveforms are slightly different from the ones of a classical Flyback converter. The storage of power in interval 1 and interval 2 is the same as in a classical Flyback converter. As shown in Figure 3.25 and Figure 3.26, during $[t_4, t_6]$ (interval 5 and interval 6), the power is transferred in a different way compared to the case of the classical Flyback topology. The abovementioned analysis highlights that the classical Flyback current (i_{L_m}) is used only to achieve ZCS at the secondary side and the power is transferred directly to the load by L_rC_r resonance. This Offers the advantage of minimizing the power stored in the transformer what allows the use of a smaller transformer compared to the case of the classical Flyback converter.

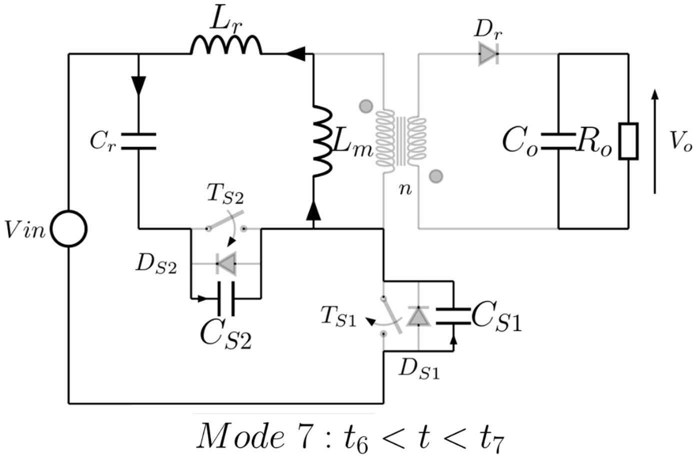


Figure 3.27 – Interval 7 Active-Clamp Flyback operation.

ZVS Condition for T_{S1}

T_{S1} turns-On in ZVS interval if the current, $i_{L_m} = i_{L_r}$, in interval 7 is high enough to discharge C_{S1} and charge C_{S2} during the dead-time . Then the body diode of T_{S1} becomes forward-biased.

$$\mid i_{L_r}(t_0) \mid \geq 2\ C_{S1/2} \frac{V_{in} + \frac{V_o}{n}}{t_{DT}} \tag{3.13}$$

where t_{DT} is the dead-time between the turn-Off and turn-On of the transistors.

It should be stressed that in contrary to the LLC converter, the magnetizing inductance is not constrained by the maximum step-up gain. Therefore it is possible to adjust the inital value, $i_{L_r}(t_0)$, by a proper choice of L_m what will optimally place the soft switching boundary. Assuming that the power is constant from input to output, the soft-switching condition of T_{S1} can be found averaging Equation (3.6) over $[0, \alpha T]$ because the average current $<i_{S1}>$ is equal to $\frac{1}{T}\int_0^{\alpha T} i_{L_m}(t)dt = \frac{P}{V_i}$ which is function of L_m. It comes:

$$L_m = \frac{V_i \frac{\alpha^2}{f^2} - 2L_r(\frac{P}{V_i f} + i_{L_r}(t_0)\frac{\alpha}{f})}{2(\frac{P}{V_i f} + i_{L_r}(t_0)\frac{\alpha}{f})} \tag{3.14}$$

Where f, α and P are respectively the switching frequency, the duty-cycle and the nominal output power.

ZVS Condition for T_{S2}

Similarly to T_{S1}, ZVS condition for T_{S2} is satisfied when the magnetizing current, $i_{L_m}(t_2)$, is large enough to discharge the drain-source parasitic capacitance of T_{S2} during interval 3. Given that the power flow is positive, the current $i_{L_m}(t_2)$ is always able to discharge C_{S2}. Therefore switching of T_{S2} is always soft.

ZCS Condition for D_r

ZCS condition for D_r is satisfied when the secondary side current, i_s, reaches zero before the end of the switching period, T. From the primary side, this condition occurs when the resonant current, i_{L_r}, reaches the magnetizing current, i_{L_m} at time t_6.

During $[t_4, t_6]$, according to Equation (3.11), the resonant current, i_{L_r}, has the form of a cosine with the period $2\pi\sqrt{L_r C_r}$. Because the magnetizing current has a negative slope, the time interval $[t_4, t_6]$ could be smaller than the period of the resonance. ZCS condition yields.

$$f_s \leq \frac{1-\alpha}{2\pi\sqrt{L_r C_r}} \tag{3.15}$$

L_r and C_r are designed according to Equation (3.15). Hence a wide set of solutions is possible. The general trend is to take into account the gate driver requirements what leads to minimize the inter-winding capacitance thus to maximize the leakage inductance of the transformer and so reduce the resonant capacitor.

Transformer Architecture

This section covers the theoretical design of an optimized transformer.

Gain of the converter The large-signal intervalling of the converter can be derived applying the principle of volt-seconds balance across the transformer magnetizing inductance [67]. Note that during this analysis, interval 3 can be neglected because $V_{L_m} \approx V_{C_r}$ rapidly converges to $\frac{-V_o}{n}$. The slope of V_{S1} and V_{S2} in interval 3 is the same as the one in interval 4 and interval 5. With these assumptions, the volt-second equation is

$$\alpha V_{in} \frac{L_m}{L_m + L_r} \approx (1-\alpha)\frac{V_o}{n} \tag{3.16}$$

It comes the relationship between the output voltage, V_0 and the DC input voltage, V_{in}:

$$\frac{V_o}{V_{in}} \approx \frac{n\alpha}{1-\alpha}\frac{L_m}{L_m + L_r} \tag{3.17}$$

The voltage relation Equation (3.17) is characteristic of an active-clamp converter, Forward or Flyback.

Transformer ratio The transformer turn-ratio should be chosen in order to fix the output voltage when the converter operates at the nominal input voltage, V_{in}. Equation (3.17) yields.

$$n = \frac{V_o(1-\alpha)}{\alpha V_{in}} \frac{L_m + L_r}{L_m} \tag{3.18}$$

Dead-time Optimization

In a high frequency soft-switching half-bridge, the dead-time control is a key point to reduce parasitic oscillations on the drain-source voltage responsible for EMI and switching losses [214, 163, 50].

In a GaN HEMT based half-bridge, it is not necessary to use external diode due to the available GaN reverse conduction. Nevertheless this reverse conduction has an important voltage drop (3.1 V) what leads to conduction losses. That is why an experimentally verified solution is proposed for a diode-less GaN half-bridge, to size precisely the dead-time duration.

During dead-times in interval 3 and 7, there is a capacitive transition in the half-bridge as shown in Figure 3.28, where the current is flowing through the drain-source parasitic capacitor. There is a relation between the magnetizing inductance and the required current to charge and discharge drain-source capacitors. Indeed by a proper choice of the dead-time in Equation (3.13) and the current amplitude during switching in Equation (3.14), the transistor losses can be even more reduced.

In this practical case, EPC2012 transistor are used in our first prototype. The HEMT has an equivalent drain-source capacitor of 0.22 nF for 30 V drain voltage. The drain-source capacitance is a non-linear function of voltage. The worst case of the problem at hand implies the maximum value of capacitance. The current, i_{L_r} in Equation (3.13), has to be more than 196 mA if the dead-time value is 20 ns. In these conditions the magnetizing inductance in Equation (3.14) has to be less than 5.8 μH.

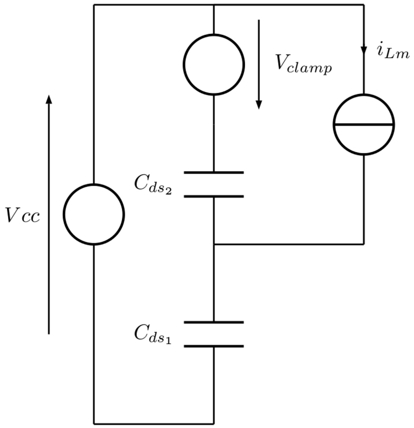


Figure 3.28 – Equivalent circuit of the GaN half-bridge during dead-time, interval 3.

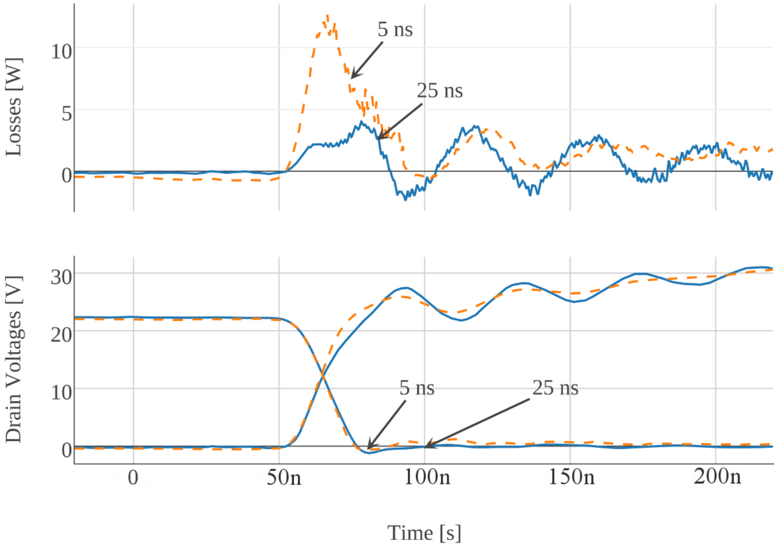


Figure 3.29 – Experimental losses and drain voltage across T_{S1} at turn-Off for different dead-time values (5 ns: dashed, 25 ns: solid).

Figure 3.29 shows the experimental waveforms for 2 different dead-times. It can be seen that a too short dead-time increases the switching losses. A trade-Off has to be found between switching losses and conduction losses because of the important voltage drop in the GaN transistor reverse conduction.

In order to summarize the different energies included during the transfer,

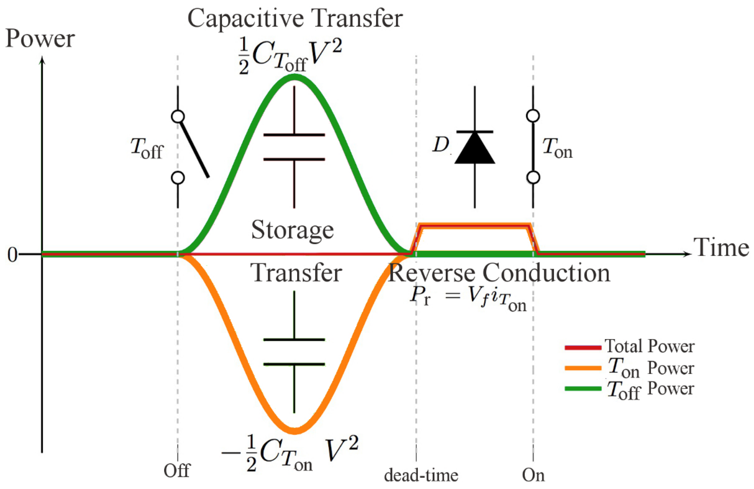


Figure 3.30 – Ideal power energy waveforms during dead-time in a GaN half-bridge

Figure 3.30 shows the capacitive transfer energy in the GaN half-bridge and the conduction losses P_r coming from the GaN reverse conduction. It can be seen that the symmetry in the half bridge between high and low-level transistors has to be respected in order to have zero switching losses during the capacitive transfer. That mean, carefully designed half-bridge and optimized parasitic inductance between the two transistors.

3.2.1.2 Conclusion

In this section, the different aspects of the new resonant-interval design were given. The different equations for the transformer sizing and the resonant bank were detailed.

A specific analysis of the dead-time optimization was made in order to reduce the switching losses and optimized the magnetizing inductance. The transformer volume is highly dependent of this inductance, and this accurate analysis allowed a good optimization of the footprint.

In the next section, the transformer design is detailed from isolation capability point of view.

3.3 Transformer Parasitic Capacitance Optmization

As shown in Section 2.2, isolation barriers are a key point for limiting the common-mode current in a half-bridge mode. The dV/dt immunity of a system can be increase by decreasing the isolation capacitance of each isolation barrier such as isolated gate driver power supply or control signal isolator.

The solution developed in this section is dedicated to the active-clamp flyback topology with a high-temperature capability and the specifications given in Table 3.1. The high-frequency switching allowed by the soft-switching mode will decrease the volume of the transformer. The challenge is to deal with a small transformer geometry but a low isolation capacitance. The reduction of the distance between primary and secondary windings due to the high frequency, will not help for a low capacitance.

In this section, a solution is proposed with a coplanar-winding transformer and different optimization solutions are presented.

3.3.1 Transformer Geometry Optimization

The first optimization and the easiest one is to work on the geometry of the transformer in order to reduce the capacitance. Different geometries were studied in order to realize a comparative work, each one were pushed as far as possible in order to obtain the lowest capacitance with the commercially available magnetic core.

Wounded Transformer The wounded transformer is the most common geometry in the industry for low-power converter, as shown in Figure 3.31.

Low manufacturing cost and the usage of the flyback topology makes this solution attractive and cost-efficient. The high-temperature constraints of our case makes difficult the material choice for the mechanical assembly and a manufacturer was chosen for the fabrication in order to have an industrial grade.

The transformer parameters are detailed in Table 3.5.

The transformer is using an ER14.5 ferrite core with a mechanical pot as shown in Figure 3.32 a). The solution to optimize the capacitance is to increase the distance between primary an secondary with a thicker Kapton layer and limiting the interleaving of the secondary with the primary side. The primary side is separated in two, in order to limit the leakage inductance, and both secondaries are sandwiched in the middle as shown in Figure 3.32 b).

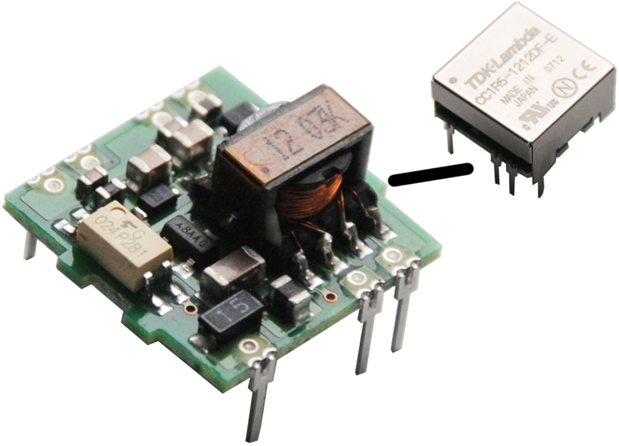


Figure 3.31 – Encapsulated wounded transformer of 3 W industrial power supply, TDKCC1R5 [208].

Table 3.5 – Wounded transformer specifications

Parameter	Value
Ferrite Core	ER14.5+pot
Isolation Cap.	< 20 pF
Ambient Temp. Max.	$200°C$
Wire type	Grade II
Isolation Material	Kapton
Volume	$1.458\ cm^3$

The result is a reduced contact area between primary and secondary and still keeping the advantage of an interleaving structure [222, 112, 157].
The measured isolation capacitance of this prototype is 12 pF when the TDK transformer in Figure 3.31 feature a 67 pF capacitance for the same output power but with a smaller volume.

Another method not detailed in this work, is to used a Faraday shield. The shield in a transformer is a copper layer between primary and secondary windings connected to ground in order to divide the coupling capacitance and force the common-mode current to ground.

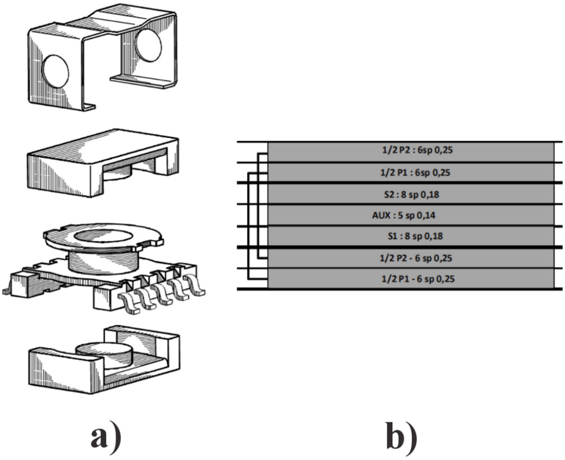


Figure 3.32 – a) ER14.5 Ferrite + Mechanical pot+ clip; b) P-S-S-P Interleaved transformer structure.

In [238, 237] good results were obtained with isolation capacitance around 2 pF and noticeable reduction of the common-mode current with a planar transformer version.
The drawbacks of this solution in the case of our application, is the extra-winding layer and the connection added by this solution which will limit the integreability of the solution.

Classical Planar Transformer Classical planar transformer design considers windings stacked on the middle leg of ferrite pots. One full prototype with the active-clamp flyback topology was designed as shown in Figure 3.33.
The same interleaved P-S-S-P structure is used for the windings in a 6 layers PCB with a ER14.5 core. A specific care was taken to shift primary and secondary in order to avoid a "face to face" between copper wire as shown in Figure 3.33, and reduce the isolation capacitance. The measured isolation capacitance is about 23 pF with a leakage inductance about 7% of the primary inductance, L_p . The capacitance dramatically increases due to the low distance between the PCB layer (254 μm) and the poor isolation quality of the prepreg material as a dielectric. The volume of the transformer is reduced to $1.050 cm^3$.

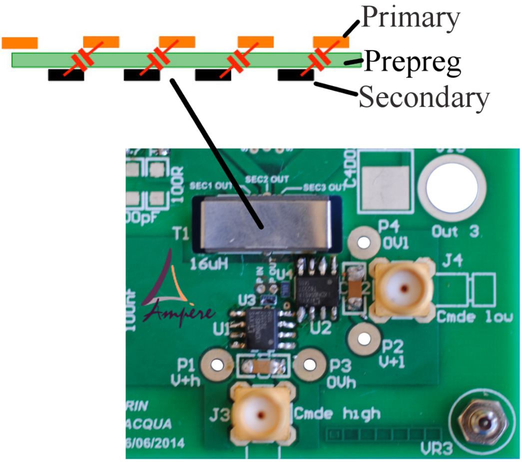


Figure 3.33 – Schematic of a classic planar transformer with simplified isolation capacitance between primary and secondary sides.

Coplanar-Winding Transformer The idea of the coplanar-winding transformer as a solution for reducing the isolation capacitance is coming from the active-filter design in [16] where a low capacitance and a high leakage inductance is requested too. Also different examples with a discrete toroidal core exist in the literature [246, 128, 130] but no planar transformer or high-integration level solutions are presented. Those solutions are usually reaching 1.5 to 2 pF isolation capacitance.

As shown in Figure 3.34, the windings of the primary and secondary side are not superposed but on the same plane. The ferrite core does not have middle leg anymore as shown in Figure 3.35. This two commercially available ferrite cores (ER 14.5, Ferroxcube) were machined to U- and I-shapes, respectively. A sectioning machine with diamond blade and a grinding/polishing table were used to reshape the ferrite cores. This custom shape allows also a reduction of the global transformer height.

The first drawbacks of this solution is the significant increase in the footprint since windings are not superposed in the middle but on the external legs of the U-ferrite. The global volume of the transformer is about 1.7 cm^3, the measured isolation capacitance is 2.3 pF with a leakage inductance about 31% of the primary inductance, L_p.

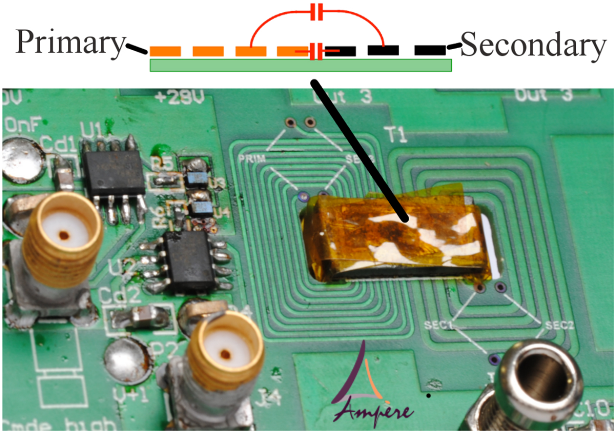


Figure 3.34 – Schematic of a coplanar-winding transformer with optimized isolation capacitance between primary and secondary sides.

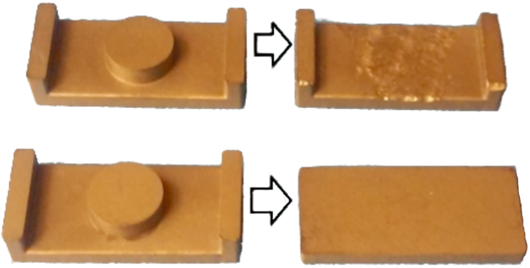


Figure 3.35 – Machined UI-shape ferrite core.

Summary In this section we have seen how to optimize an isolation capacitance in a planar transformer by working on the geometry by itself. A reduction up to 2.3 pF was performed with coplanar-winding transformer, however the increase of the transformer footprint is a drawback for the integration of the solution.

3.3.2 Transformer Optimization through FEM

As shown in [56], the isolation capacitance is divided in several physical capacitances as following:

- The turn-to-turn capacitance;
- Winding-to-magnetic core;
- Inter-winding interactions.

The complexity of the structure and the distribution of the different capacitances are highly dependent of the geometry. FEM simulation tools can provide an accurate model based on the 3D drawing even if it requires a cost of long simulation.

An accurate geometry model was drawn as shown in Figure 3.36. The picture shows the two main distances which affect the winding capacitance. The curve a) is related to the length between the winding and the magnetic core and the length between the primary and secondary windings. Curve b) is related to the length between the winding and the top of the magnetic core.

Maxwell software allows to make variable parameter in the model geometry, each length was defined as a parameter in order to find the optimal point for a precise design of the transformer (number of winding turns) and ER14.5 ferrite core as shown in Figure 3.37.

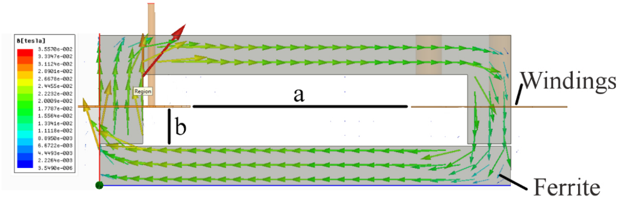


Figure 3.36 – 3D model of the transformer in FEM, with the B Field distribution and the distances which affect the isolation capacitance.

According to Figure 3.37, an optimal distance can be found around 2.5 mm for distance a) and 1 mm for distance b). It can be seen that the isolation capacitance between primary and secondary sides is dominant on the other two ones.

The transformer shown in Figure 3.34 was re-designed with the optimal parameters and implemented in the active-clamp flyback solution with a 0.8 pF

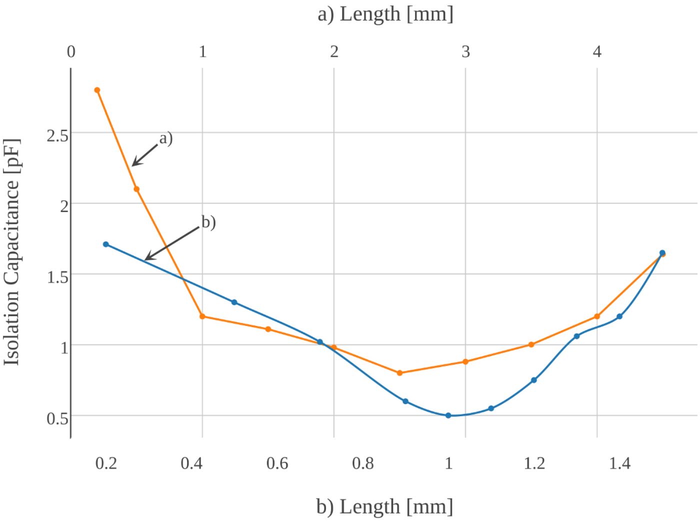


Figure 3.37 – Simulated Isolation capacitance vs. distances a) and b).

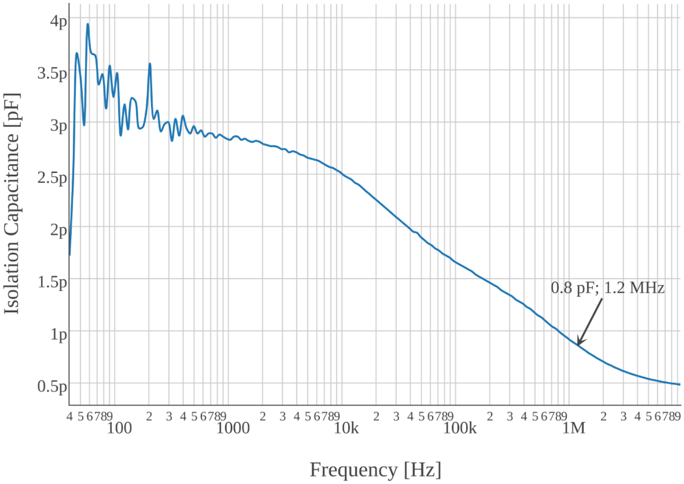


Figure 3.38 – Measured isolation capacitance in the optimized transformer.

isolation capacitance. The isolation was measured with an impedancemeter Agilent 4294A under probes. The accurate values provided by probe measurement are given in Figure 3.38.

The capacitance value was decreased from 2.3 to 0.8 pF after optimization and shows a results beyond the state-of-the-art.

3.3.3 Analytic Transformer Optimization

The analytic approach was widely used instead of FEM for two reasons: first, in order to point out the physical electrostatic relations of wounded components; second, to provide a simple and fast design tool [148, 124, 12, 56].
In this work, a focus is made on the collaboration work made at CPES lab on the transformer optimization. [203] is presenting the analytical solution for the transformer optimization. This study is based on a custom toroidal core with the same power supply specifications. All the volume parameters can be customized in order to reach the optimum design.
The optimization method is comparing the volume, the core losses and the isolation capacitance. The isolation capacitance model is relatively complex to build compared to the losses model. There are two parts in the isolation capacitance calculation extracted from [140]. One is total impedance of the equivalent capacitance from winding to core, in series with the resistance from primary side to secondary side on the core, and with the capacitance from core to the winding. This can be described with some analytical equations. The other part is the capacitance between the two windings without core, which is represented by a curve-fitting method based on the Q3D simulation results. However the error between the Q3D simulation and final measurements i up to 0.5 pF due to the model accuracy, which reduces the global accuracy of the whole optimization.

The specifity of this work is the used of the optimization software CADES. The models and the optimization process runs with two parameters (core losses and core volume) to draw a 3D Pareto surface between volume, losses, and isolation capacitance. Each point on the Figure 3.39 surface is an optimized result. One points is selected according to the requirement as 242 mW loss, 1 pF inter-capacitance with 242 mm^3 volume.
The cost of a full custom ferrite is expensive but allows an high improvement on the core loss and on integration of the transformer solution. The solution proposed, gives an efficient solution for the optimization of a magnetic core but is highly dependent of the accuracy of the different models used. However, the analytic model coupled with an optimization software to solve the different equations gives good results in a shorter time than FEM simulation, especially is different geometry have to be tested.

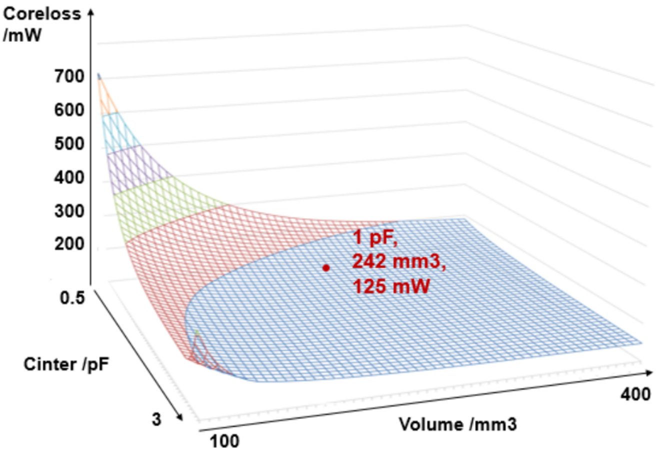


Figure 3.39 – Pareto surface of losses, isolation capacitance, and volume for the toroidal transformer design [203].

3.3.4 Conclusion

In order to optimize the isolation capacitance of a transformer, three decisive factors are considered :

- The dielectric constant of the insulating materials interposed between the conductors. This point is determined by the PCB material selection.
- The geometry of the winding like the diameter and dimension and the mutual spacing between wires and their distance to the screen or to the core. The optimum was reached after an FEM optimization.
- The winding arrangement and the strategy of connecting the different winding is affecting the isolation capacitance. The coplanar-winding structure is giving an optimal geometry for low isolation capacitance.

Different ways can be used to optimize the transformer. However FEM simulation seems a key point for accurate simulated value. In the next section a PCB embedded transformer prototype is designed based on a FEM optimization of the geometry.

3.4 PCB integration of a 2 W Power-Supply in High-Temperature Applications

This section details the PCB integration of the transformer in high-temperature applications. This part of the thesis was realized in CPES lab, Blacksburg, USA and 3DPhi, Toulouse, France. Fabrication took a lot of time to performed an efficient lamination process. Many test and failures were necessary in order to have good results. The size of the section is not representative of the allotted time.

The PCB embedding process presented in this work utilizes traditional Mn-Zn ferrite core and properly selected PCB materials with high glass-transition temperature (Glass Transition Temperature (Tg)) and low coefficient of thermal expansion (Coeffcient of Thermal Expension (CTE)) to develop a transformer with coplanar-winding structure for the highly integrated power supply used in harsh environment.

3.4.1 PCB Selection

Table 3.6 – High-Temperature PCB Materials.

Manufacturer	PCB	Tg [°C]	CTEz[10^{-6}]	CTEx[10^{-6}]	CTEy[10^{-6}]	Material
Arlon	35N	250	51	16	16	Polymide
Arlon	85N	260	50	16	16	Polymide
Panasonic	R1515E	250	22	9	9	PPO
Panasonic	R1515W	250	22	9	9	PPO
Hitachi	E700-G	250	20	8	10	PPO
Rogers	6202R	326	30	15	15	PTFE

Most commercially available PCB materials with high Tg have very high CTE ($> 30 \cdot 10^{-6}/\,^\circ$C) along z-direction, as listed in Table 3.6. The embedded Mn-Zn ferrite material has a CTE around 7 to $10 \cdot 10^{-6}/\,^\circ$C. Significant amount of thermal stresses could be applied on both ferrite cores and PCB laminates due to this dramatic CTE mismatch especially for high-temperature applications. Delamination on the multilayer PCB assembly and cracking in ferrite cores are the two most expected defects in the embedded structure, which would cause failure of the integrated power supply.

The Panasonic R-1515 PCB material is a Polyphenylene Oxide (PPO) epoxy resin and presents a low CTE of $22 \cdot 10^{-6}/\,^\circ$C in z-axis in Table 3.6 which is more compatible with that of ferrite materials. The reliability of embedded transformer would be improved accordingly. An embedded transformer prototype using traditional FR-4 material (epoxy resin with fiberglass) with higher CTEs ($60 \cdot 10^{-6}/\,^{\circ}$C in z-axis) was also manufactured as a reference. Thermal cycling tests have been used to evaluate the impact of different CTE mismatches on the integrity of the assemblies.

3.4.2 PCB Lamination Process

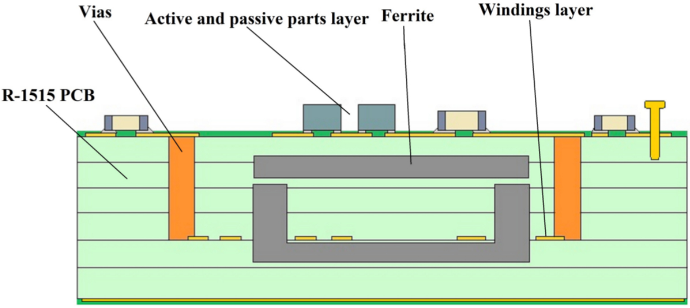


Figure 3.40 – Schematic of the power supply with PCB embedded transformer.

Figure 3.40 shows a cross-section of the PCB embedded transformer with different layers. The ferrite core and coplanar windings were embedded into the PCB (Panasonic R-1515W) to implement the transformer. All other components including active GaN devices, were mounted on the top surface of the PCB substrate.

The detailed information about the PCB embedding process of transformer is introduced below:

- Two commercially available ferrite cores (ER 14.5, Ferroxcube) were machined to U- and I-shapes, respectively as shown in Figure 3.41. This Mn-Zn ferrite core material was used due to its low core losses density at 1-2 MHz and high Curie temperature (300 °C). A sectioning machine with diamond blade and a grinding/polishing table were used to reshape the ferrite cores.

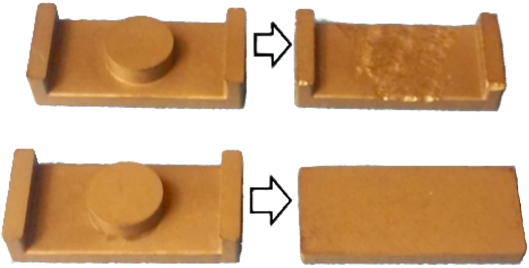


Figure 3.41 – Machined UI-shape ferrite core.

- Panels were cut in pre-preg using a CO_2 laser machine. Unneeded copper (Cu) on PCB panels was removed by ferric chloride etching solution as shown in Figure 3.42.

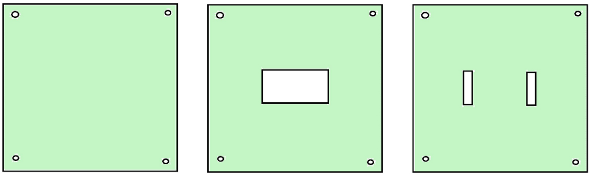


Figure 3.42 – C-stage after laser cutting.

- Two R-1515W laminate sheets with 1 oz. Cu were used for the preparation of embedded winding layer and the top active layer. The top Cu surfaces were patterned and etched to form the windings as shown in Figure 3.43 a) and the circuitry for the power supply as shown in Figure 3.43 b), respectively.

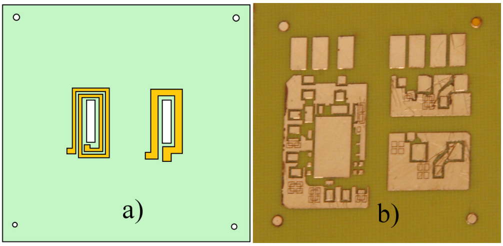


Figure 3.43 – Etched windings layer a); and top-circuit layer b).

- The PCB stack consisting of alternate c-stage laminates and b-stage prepregs was aligned with ferrite cores as shown in Figure 3.44.

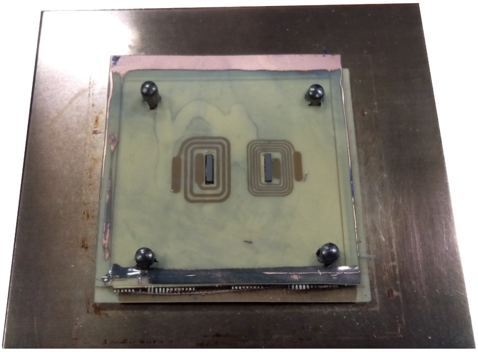


Figure 3.44 – PCB stack before lamination.

- The lamination process for the embedded transformer was divided into three steps as shown in Figure 3.46. The flat I-shape ferrite core with the top circuitry layer was laminated into one piece first following the pressure/temperature profile in Figure 3.45. Then, the U-shape core with the internal winding layer was embedded into the PCB multilayer substrate. The last lamination was performed to integrate the two parts of the previous steps. The customized air-gap distance can be adjusted using different thicknesses and/or numbers of the bonding prepreg layer. Figure 3.49 shows the picture of the final assembled passive substrate.

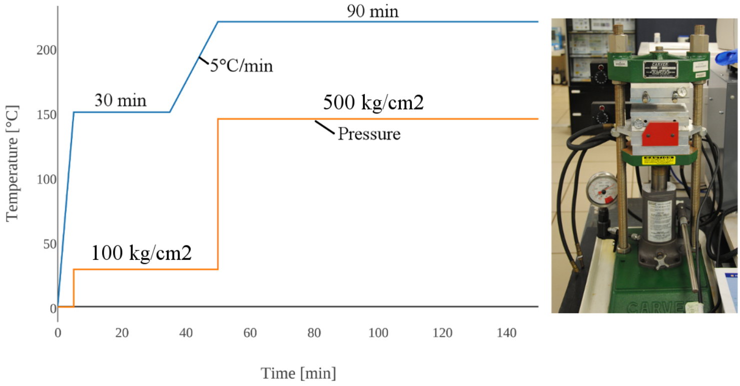


Figure 3.45 – Press condition for R-1515 process customized for PCB magnetic integration; 2112 Carvier press used for the lamination.

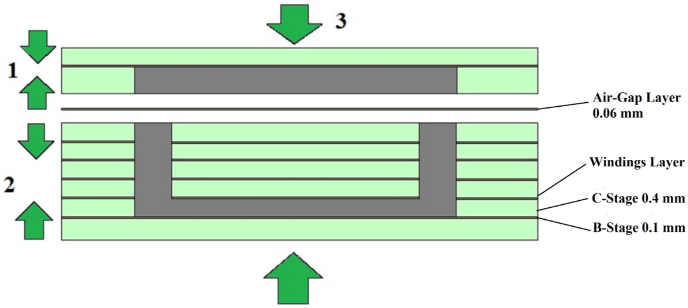


Figure 3.46 – 3 steps of the lamination process.

- Vias were drilled by a laser process, and the connections between the internal winding layer and the top circuitry were made with soldered Cu pins as shown in Figure 3.47.

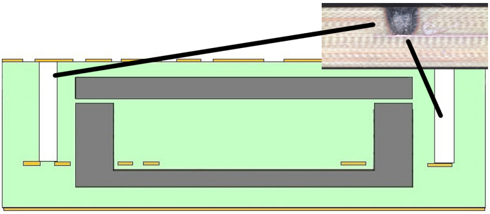


Figure 3.47 – Drilled vias in the laminated PCB.

The whole process flow for the power supply with PCB embedded transformer is given in Figure 3.48. The total thickness of the assembled passive

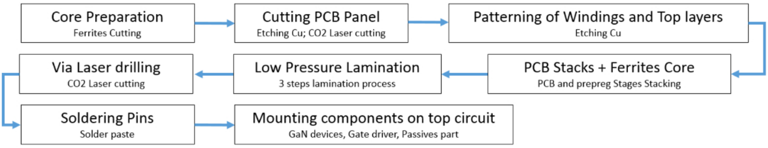


Figure 3.48 – Process flow for power supply with PCB embedded transformer.

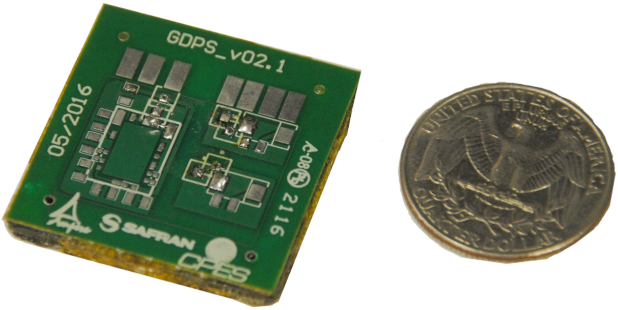


Figure 3.49 – Laminated PCB with embedded transformer.

substrate shown in Figure 3.49 is about 2.8 mm. In order to validate the lamination process measurement were realized on the main characteristics of the transformer such as leakage and primary inductance. Table 3.7, the small differences between simulation and experimental measurement values on the prototype shown in Figure 3.49, validate the process chosen for the magnetic integration. The lower experimental value for each parameter can be explain by the approximation on the air-gap length since the prepreg polymerization length during lamination shows a variation between 30 and 35 %. The complete converter prototype was built by soldering other components on top of the PCB.

Table 3.7 – Simulated and experimental PCB integrated transformer characteristics.

	Simulation	Experimental
Leak. Ind. (L_l)	2.5 uH	2.1 uH
Prim. Ind. (L_1)	6.1 uH	5.4 uH
Iso. Cap. ($C_{1/2}$)	0.7 pF	0.9 pF

3.4.3 Thermal Cycling of PCB Embedded Transformer

The reliability of the PCB with embedded ferrite core transformer was evaluated using a thermal cycling method. Due to the difference in CTEs between the ferrite and PCB substrate materials, major defects such as delamination at interfaces and cracking in ferrite core are expected. The cycling profile applied to the PCB samples follows the aeronautic constraint, with a temperature range from $-55\,^{\circ}\mathrm{C}$ to $200\,^{\circ}\mathrm{C}$ and the heating/cooling rate of $20\,^{\circ}\mathrm{C}/min$ and 20-min holding period at each plateau as shown in Figure 3.50. In order to make a comparative study, two specific samples were manufactured for this test using Panasonic's R-1515W and Isola's FR-406 PCB materials, respectively.

After 1000 cycles, no delamination and other major defects were observed on the sample using Panasonic's PCB materials, as shown in Figure 3.51 b). The color changing is coming from the contrast difference when the picture was taken. Serious delamination and ferrite crackings can be observed in Figure 3.51 d) on the PCB-embedded sample using FR-4 materials after only 150 cycles.

The R-1515 PCB material is identify as a good candidate so far for embedding ferrite in the PCB in high-temperature application.

Figure 3.50 – Thermal chamber for the cycling test.

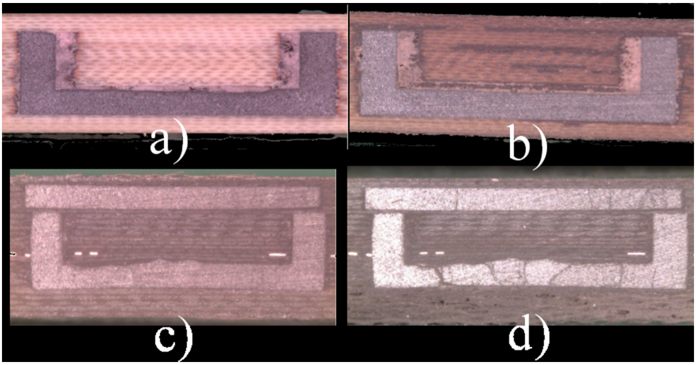


Figure 3.51 – Temperature cycling test: a) Panasonic R-1515 sample before cycling test; b) Panasonic R-1515 samples after 1000 temperature cycles; c) FR-4 samples before cycling test; d) FR-4 samples after 150 temperature cycles.

3.4.4 Conclusion

A new integration process for PCB embedded transformer has been proposed. In comparison with the conventional tools and know-how, this developed fabrication process allows the embedding of commercial ferrites with a good control of the air-gap. The high-temperature application requires the use of a PCB material with high Tg and suitable CTE compatible with embedded ferrite core material. The reliability of PCB embedded transformer fabricated in this study has been demonstrated using thermal cycling test.

3.5 Experimental results

This section details the different experimental results of the different designed gate driver power supplies designed. The decrease in the isolation capacitance and the integration of the power supply are the modification noticeable along this section.

3.5.1 High-Temperature Flyback Power Supply

Flyback converters are used in power supplies requiring low-to-medium output power on several output voltages. Due to the high cost of high-temperature components, the flyback converter has the advantage of a low count. This prototype will be used as a reference point for the next development.

The main switch is a N-MOSFET (ref : XTR2N0825 fro XREL) and the diodes are SiC diodes (ref : C3D02060E from CREE). The transformer is built using a low permeability nanocrystalline core from APERAM (ref : 095 045 B600), a high-temperature enameled copper wire and a high temperature polymer thermoplastic (PEEK) machined housing.

The regulation is based on quasi-regulation techniques by using a third dedicated winding on the transformer [129, 233]. This provides the insulation of the feedback regulation circuit at high temperature. The PWM controller (ref : XTR30014) is supplied by XREL. The power supply specifications are summarized in Table 3.9. The quasi-regulation of the output voltage reaches less than 16% discrepancy. We observed that the PWM controller adjusts correctly the duty-cycle ratio for different load change.

A high-temperature test is made at the nominal output current, (200mA), up to 200°C to plot the flyback output voltage variations. The performance is mainly determined by the PWM controller using the feedback loop. The test

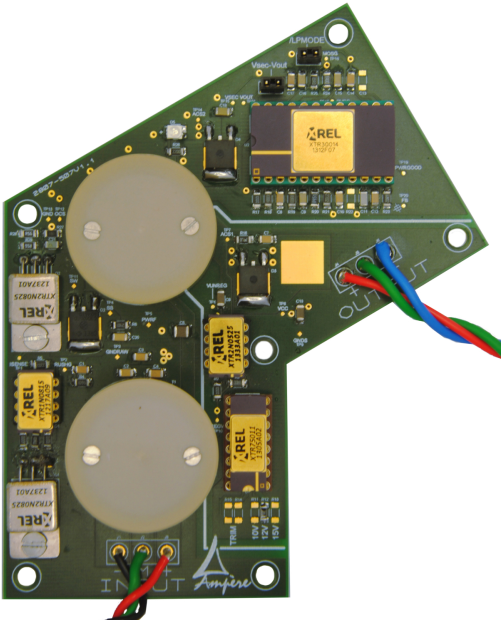


Figure 3.52 – Double output hard-switching flyback prototype with Xrel SOI MOSFET.

Item	Parameter
Type	Quasi-regulated Flyback
Input voltage	28 V
Output voltage	2 X 10 V
Load regulation	16%
Current output max	200 mA
Switching frequency	200 kHz
Insulation prim./sec.	1.5 kV
Temperature range	-60°C to +200°C
Isolation Cap.	4.5 pF
Footprint	560 cm^3

Table 3.8 – Hard-switching flyback converter specifications. A linear post regulator was used to provide a tighter tolerance, lower than 2%.

on the flyback converter shows an output voltage variation of about +1.8%.

3.5.2 High-Temperature Active-Clamp Flyback Power Supply

Figure 3.53 – Double output active-clamp flyback protoype with EPC GaN HEMT for high-temperature operation.

The half bridge is composed of two EPC2012 GaN transitors. Due to the high temperature requirement, it is necessary to use low side drivers with no external gate resistor, one of them isolated with a bootstrap system (diode and capacitor) for the power and a digital isolator for its PWM signal. A standard GaN dedicated driver LM5113 was not considered as the fixed dead-time values were not pertinent with the circuit.
The transformer is a planar shape designed with 3C92 Ferroxcube ER14.5 ferrites. All passives components are specified for high temperature (NPO-series capacitor SRT Ceramic, Kemet) and low temperature coefficient resistors (Vishay). A 5 A SiC Cree diode with a voltage drop of 0.7 V (@0 A 25°C) is selected as the rectifier diode. One output has a shunt resistor of value 1 Ohm, 3 W (Vishay Dale) for accurate current measurement.
The input voltage is fixed at 15 V and the output voltage are set to 6 V. A switching frequency of 800 kHz is chosen to fit the design with a duty-cycle of 0.5. The PCB is a four-layer Arlon 35N polymide PCB.

Figure 3.54 shows the experimental current waveforms at full-load (2 W). It allows to see how current flows through the transformer and the zero-current switching of the diode. The drain currents are measured with a Teledyne

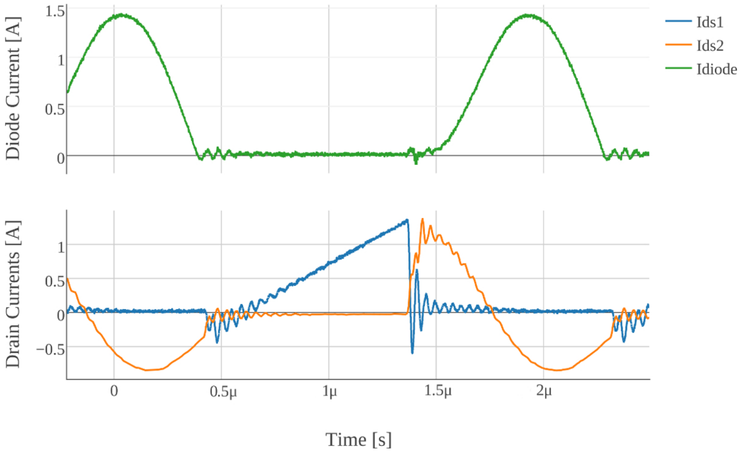


Figure 3.54 – Experimental drain current waveforms of GaN transistors and current in diode rectifier at 25 °C.

ADP032 current probe and the diode current is measured with the shunt resistor. These curves have to be compared to Figure 3.20. This allows to verify ZCS operation at the end of the diode conduction. Figure 3.54 illustrates that the soft-switching waveforms are relatively clean given that the converter operates at 800 kHz without any snubber.

A small linear decrease of 0.6 V (10%) is observed over 1 W range as it is the case in LLC resonant converter. The active-clamp topologies are intrinsically stable [65] regarding the load variation. This suggests to use the power supply without regulation system in order to gain in simplicity and reliability.

The targeted application is a driver power supply where the load is a GaN half bridge. From literature it is now well-known that the GaN transistor gate is very sensitive to overvoltage. The output voltage stability is thus a benefit for this kind of application.

Figure 3.55 shows the experimental efficiency of the converter. In this section the power-supply board is tested up to 200 °C using a hot furnace. The maximum value of 75% corresponds to literature values of this power range [97]. Both diodes with 0.7 V voltage drop create losses about 18% of the total losses. The other losses come from the magnetic material for 7% (149 mW losses).The IXDN604 loss is neglected and as shown in previous Section the switching losses are almost equal to zero.

The efficiency decrease is due to the increase in diode forward voltage with temperature (0.7 V at 25 °C, 1.6 V at 200 °C).

Item	Parameter
Type	Unregulated Active-Clamp Flyback
Input voltage	15 V
Output voltage	2 X 6 V
Load regulation	10%
Current output max	150 mA
Switching frequency	800 kHz
Temperature range	-60°C to +200°C
Isolation Cap.	2.3 pF
Footprint	31 cm^3

Table 3.9 – Insulated flyback converter specifications.

A linear post regulator was used to provide a tighter tolerance, lower than 2%.

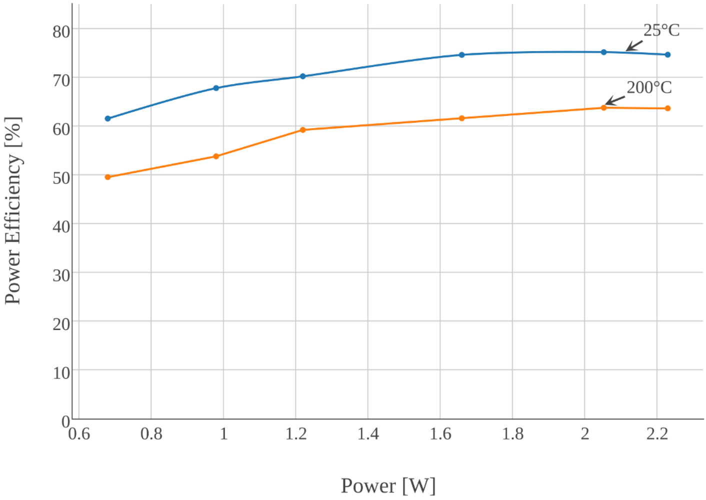


Figure 3.55 – Experimental efficiency vs. output power of the converter for different temperatures (800 kHz, $V_{in} = 15$ V, $V_{out} = 6$ V).

Diode Rectifier Optimization The diode rectifier has an importance on the global efficiency with 28% of the losses of the converter at 200 °C, due to the voltage drop on the output voltage and also the importance on the switching losses with the junction capacitance of the diode that causes extra ringing [77].

In this paragraph, a particular attention is given on the best diode type in order to optimize ZCS operation on the secondary side with the lowest voltage drop. The constraint on the diode for this prototype is an average current of 150 mA, a peak current of 1.1 A and 50 V maximum voltage. Three different SiC schottky diodes were tested, the detail of each is given in the Table 3.10.

Table 3.10 – High-frequency diode rectifier for high-temperature application.

Device	Drop. Voltage at 200 °C	Junction Cap. at 30 V	I_r at 200 °C
CREE C3D02060E [53]	1.6 V	25 pF	50 nA
Ampere Prototype [35]	1.4 V	250 pF	1 nA
GeneSiC GB02SHT01 [7]	1.55 V	35 pF	100 nA

SiC schottky diodes have a good reliability at high-temperature but suffer from high voltage drop at 200 °C. Also the diode package has an important role, since is impacting the diode junction capacitance by addition of parastics [174, 197].

As shown in Figure 3.56, for a similar operating point, the current waveform

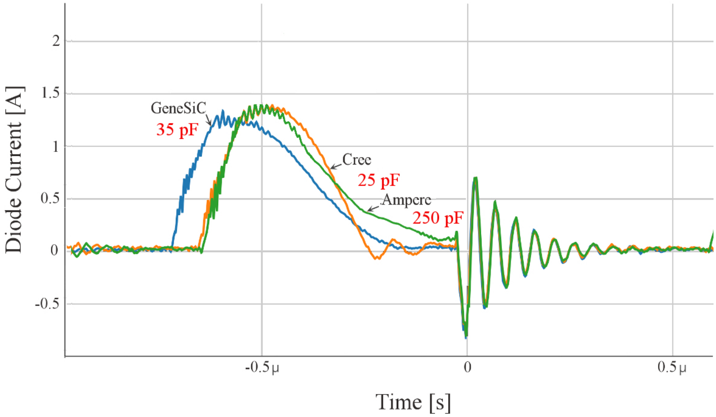


Figure 3.56 – Comparative diode current waveforms in an active-clamp flyback.

is modified by the junction capacitance value. The low junction capacitance coupled with a D2PaK package allows a fast transfer of the energy at the

secondary side of the converter through the diode. It can be also seen that a high junction capacitance value is slowing down the end of the resonant arch. After the diode rectifier optimization, the Cree diode was chosen for the optimized package and low junction capacitance. SOI diodes are also existing and present better characteristics at high-temperature [190] but the commercially available products are usually dedicated to low power application and were not fitting our maximum current requirement.
After this study, it appears that there is a market not addressed by the manufacturers for medium-power diode rectifier in SiC or SOI for low voltage application.

Synchronous Rectifier In order to offer an alternative solution to the dependence on the diode rectifier voltage drop, a synchronous rectifier was implemented at the secondary side of the power supply [83, 84]. GaN transistor has very low recovery losses Q_{rr} compared to SiC or Si devices due to the specific reverse conduction behavior. GaN transistor makes the synchronous rectifier solution really attractive for efficiency improvement [178].
However, if the efficiency of this solution for non-isolated converter topologies has been already demonstrated [96], the efficiency for isolated topologies makes only sense for high-power converters [243]. Indeed, the volume required for the synchronous control signal from the primary side to the secondary side and the specific gate driver for the synchronous transistor increase the footprint and the complexity of the solution.
The solution implemented in the active-clamp flyback increased the efficiency up to 85% with an EPC2007 GaN transistor and a LT8309 as the gate driver. The efficiency improvement comes with a penalty in the integration of the solution. It is also difficult to find GaN dedicated synchronous rectifier gate driver with high-frequency capability. This solution was not kept in the final prototype.

Specification of the Active-Clamp Flyback on 1 μm SOI-Chip

This section presents the development of a Silicon On Insulator (SOI) chip in order to integrate the active part of the active-clamp flyback. The design was realized in partnership with Easii IC XREL company. The specifications were provided according to the different confirmatory experiments performed with a discrete SOI devices.

Discrete Board The final SOI chip is made of the assembly of existing SOI devices in XREL catalog. Discrete components are in a first step implemented in a discrete prototype in order to address the possible issue before the design of the SOI chip.

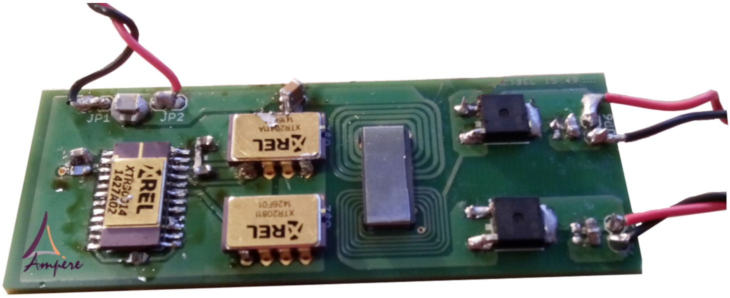


Figure 3.57 – 1 MHz discrete Active-clamp Flyback prototype for XREL components evaluation.

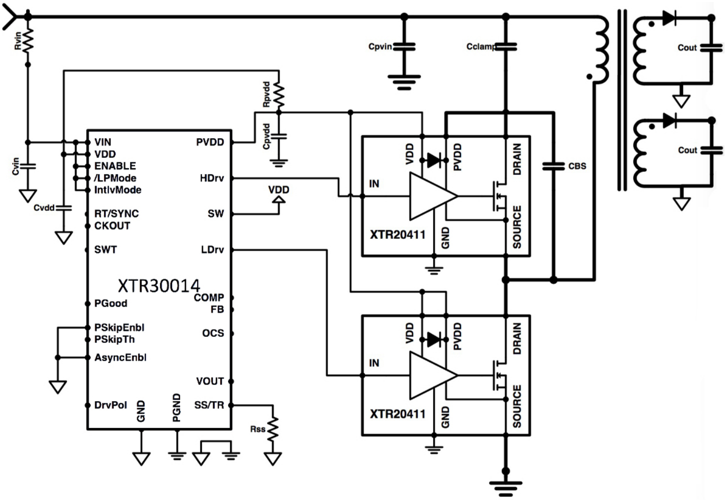


Figure 3.58 – 1 MHz discrete Active-clamp Flyback circuit schematic.

As shown in Figure 3.57 and Figure 3.58, the board is using an PWM controller XTR30010 generating a complementary 1 MHz signal with 0.5 duty-cycle. The high and low side transistors are using each one a XTR20411, which includes a bootstrap gate driver with a N-MOSFET. The bootstrap capacitor is a NPO 150 nF capacitor and the switching frequency is fixed

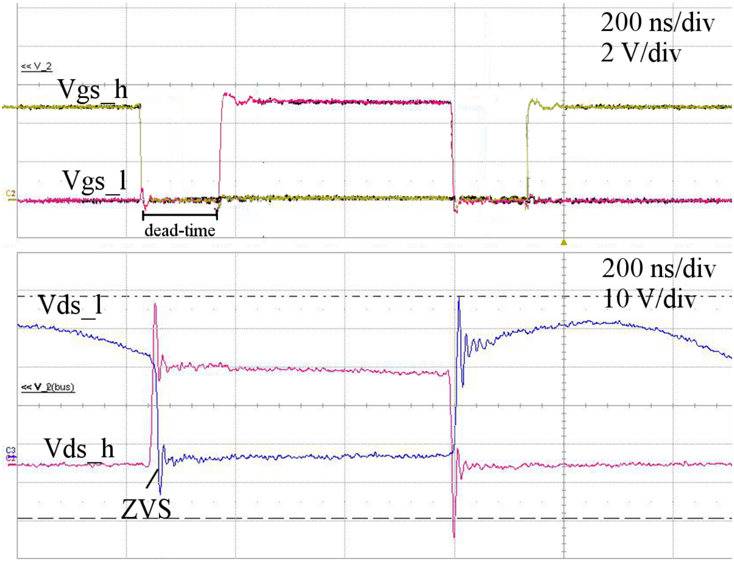


Figure 3.59 – High-side and low-side gate voltages and drain voltages at 25°C and 2 W.

through a 0.1% resistor. The coplanar-winding transformer is made with a 3F45 Ferroxcube customized U and I shapes and two C3D02060E diode rectifiers. The PWM controller is including a Over-Current Protection (OCP) and a soft-start function useful for gate driver power-supply.

A map of the losses for this prototype was done based on the experimental measurement realized in Figure 3.59. The voltage drop in the diode rectifier is the dominant as shown previously. The bar chart in Figure 3.60 shows the result. A bootstrap related issue was noticed in this first prototype. During the soft-start, the duty-cycle does not allow enough energy flowing through the bootstrap capacitor and the supply voltage for the high-side gate driver was not reaching the UVLO limit.

Figure 3.61 shows the optimal configuration in the phase-legs control signal for charging the bootstrap capacitor during the soft-start. The control command during the soft-start was adapted in the control chip circuit in order to have enough current flowing through the bootstrap capacitor by longer turn-On time of the transistor, T_1.

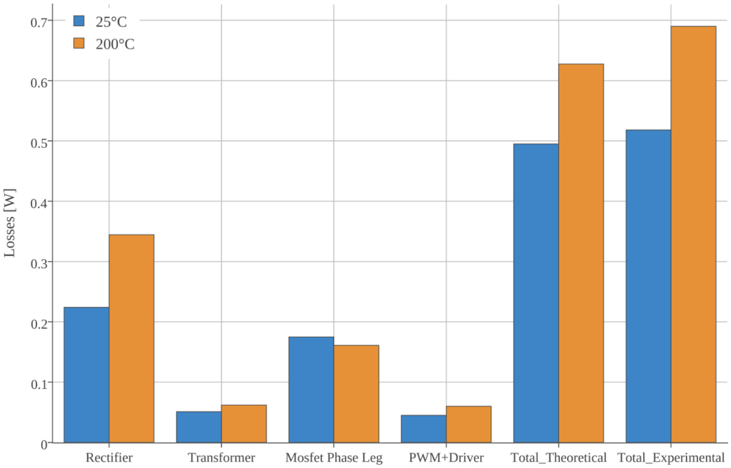


Figure 3.60 – Experimental losses map for 25°C and 200°C ambient temperature.

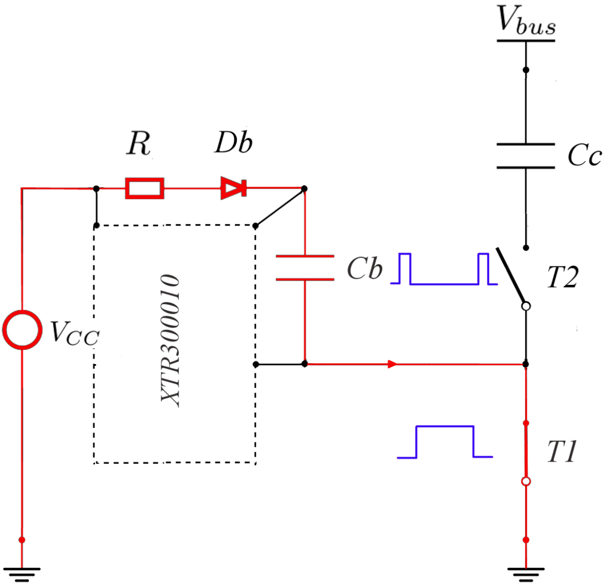


Figure 3.61 – Optimal soft-start control for charging the bootstrap capacitor.

3.5.2.1 Integrated Power Supply Solution

The integrated power supply solution is the assembly of the PCB embedded transformer and the SOI chip.

1 μm SOI-Chip The chip was designed with a SOI 1 μm technology from XFAB. The choice of this technology allows a good reliability at high-temperature [19, 55, 188]. However this technology is limiting the maximum switching frequency due to the MOSFET channel length, around 1 MHz. Another SOI technology such as 0.18 μm is less experienced in harsh environment but would allow higher switching frequency. The choice of the integration was motivated by the high-frequency switching and by the PCB embedded transformer process which allowed small footprint converter. Both points gives a tendency and new ways for the high-integrated power-supply.

The chip layout is detailed in Figure 3.62 and includes all the primary active parts of the power-supply accordign to the schematic in Figure 3.58. The soft-start function and the overcurrent protection are included in the PWM controller part. Switching frequency can be adjusted with a external resistor The maximum current of the protection is fixed also by an external resistor (3 A in our case) and the soft-start function is managed internally. The bootstrap, input and internal voltage decoupling capacitors are chosen accordingly from high-temperature application.

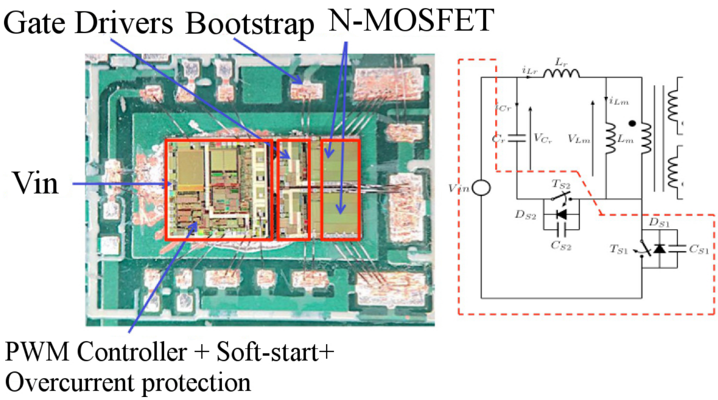


Figure 3.62 – SOI Chip with the active parts of the active-clamp flyback.

PCB Embedded Transformer Power Supply Two main prototypes were realized. The first one was realized based on EPC2012 GaN transistors with a 2.2 MHz switching frequency for ambient temperature Figure 3.63 a), since the GaN transistors and its associated gate driver were not able to reach 200 °C. The second prototype made with the SOI chip has high-temperature capability but lower switching frequency due to the SOI technology Figure 3.63 b). The SOI chip is bonded with high-temperature glue on top of the PCB and electrically connected by wire-bonding.

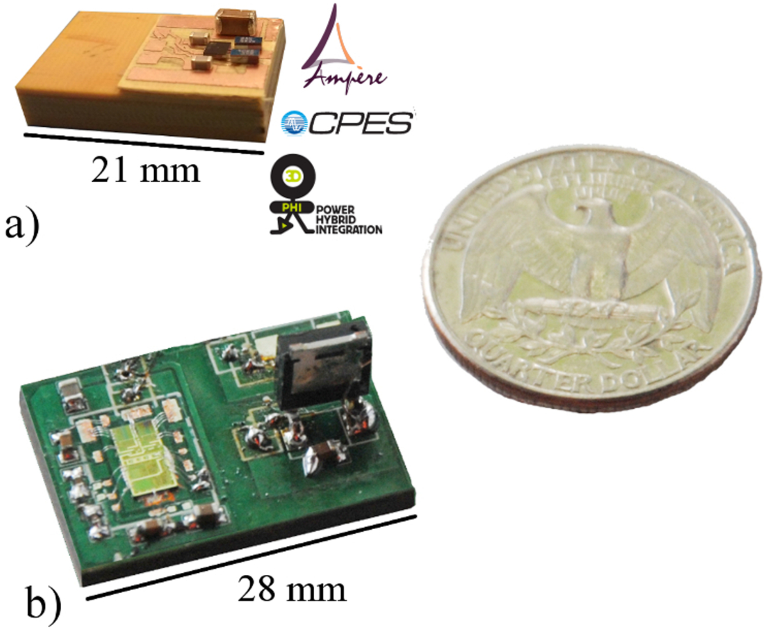


Figure 3.63 – a) 2.2 MHz prototype with GaN transistors and PCB integrated coplanar-windings transformer; b) 1 MHz prototype with SOI chip and PCB integrated coplanar-windings transformer.

A summary of the characteristics of each prototype is given in Table 3.11. The behavior in temperature of the prototype b) is better due to the SOI CMOS technology which ensures a good stability. The load regulation of the prototype b) allows an output voltage drop by 10% instead of 12% for the prototype a) due to the reduction of the parasitics which means less ringing during transient.

Table 3.11 – Characteristics for the integrated prototypes a) and b).

	Prototype a) (GaN)	Prototype b) (CMOS SOI)
Input voltage	15 V	15 to 36 V
Output voltage	2 X 6 V	2 X 6 V
Load regulation	12%	10%
Efficiency max.	68%	74%
Current output max	150 mA	150 mA
Meas. output ripple	51 mV	22 mV
Switching frequency	2.2 MHz	1.2 MHz
Temperature range	0 °C to +125 °C	−60 °C to +200 °C
Meas. Isolation Cap.	0.75 pF	0.9 pF
Footprint	0.7 cm^3	1.1 cm^3
Protection	None	Soft-start; OCP

In the Table 3.11, the efficiency difference is coming from the core loss of the 3F45 which is smaller at 1 than at 2 MHz. The isolation capacitance increase is due to the extra winding in the transformer structure due to the lower switching frequency. The SOI CMOS technology (1 μm xFAB) is limiting the maximum drain voltage to 40 V, the soft-start function allows for no over-voltage during the turn-On of the power supply as shown in Figure 3.64.

In order to limit the conduction losses of both switches and let enough time for the soft-switching to be completed, the dead-time was fixed to 100 ns which was also the minimum value that the 1 μm SOI CMOS technology

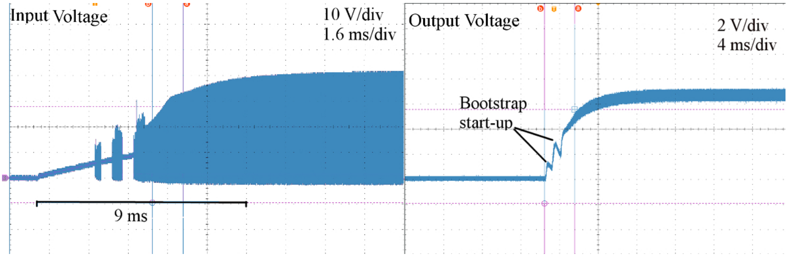


Figure 3.64 – Drain voltage and output voltage during soft-start in prototype b).

allows to implement in practice. The larger dead-time is also easily explained by the larger drain capacitance of the SOI MOSFET, given at 400 pF at 30 V.

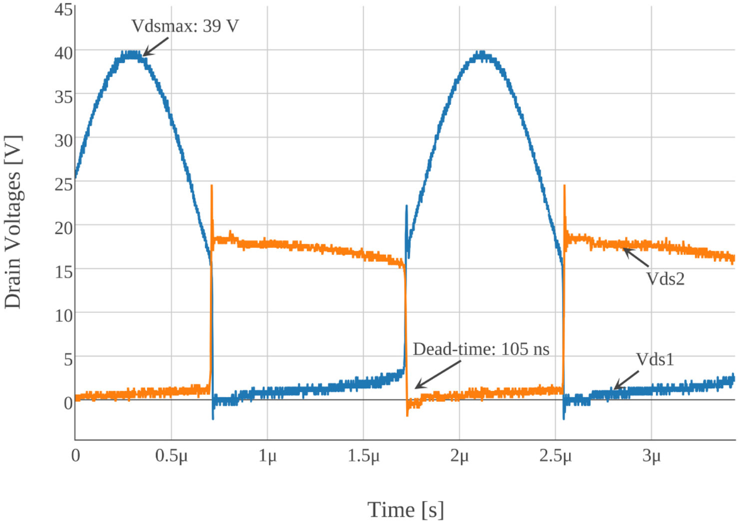


Figure 3.65 – T_{s1} and T_{s2} drain voltages at 200 °C.

Figure 3.65 shows the drain voltages for high and low-side transistors at 200 °C. The dead-time value is meeting the specifications The maximum drain voltage does not exceed 40 V and the switching frequency is 1.2 MHz. It can be also seen that soft-switching coupled with the chip-integration is allowing clean transient without ringing and with limited over-voltage.

Transistors selection In order to reduce as much as possible the size of the transformer, an optimization can be done on the phase leg transistor selection. As shown in Section 3.2, the magnetizing inductance of the transformer is dependent on the energy requested for charging and discharging the drain capacitance of the transistor, C_{ds}. In order to reduce the magnetizing inductance, the power transistor has to have the lowest drain capacitance value.

A selection of EPC GaN transistors with compatible rating is presented in Table 3.12, numbers in green are showing the best characteristic for each one. According to the Table 3.12, the transistor EPC8010 presents the best trade-off between drain-capacitance and On-resistance which affects the conduction losses. In Figure 3.66 simulated switching transient shows the improvement

Table 3.12 – EPC GaN transistors for optimized magnetizing inductance.

	EPC8010	EPC8003	EPC2012C
Vds [V]	100	100	200
Ids [A]	2.7	2.7	5
Ciss [pF]	43	38	100
Coss [pF]	25	18	65
Crss [pF]	0.3	0.2	0.4
RdsOn [mOhm]	160	300	100
Footprint [mm^2]	1.785	1.785	1.53

on the switching time. A shorter switching time means a better efficiency of the power supply to transfer the energy between primary side and secondary side. The low drain-capacitance increases the dV/dt and the area under the curve or the energy transfer is more important.

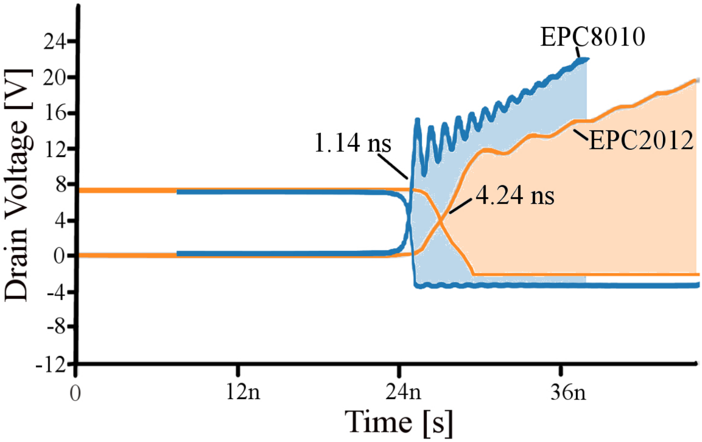


Figure 3.66 – SPICE simulated high and low drain voltages for EPC2012 and EPC8010 for the same power rating.

Measurements were performed with two different transistors and 2% efficiency point is linked to EPC8010. The conduction losses increase but the gain in the switching time is more important. Instead of increasing the efficiency, the size of the transformer can be reduced since the current in the magnetizing inductance can be lower. One winding turn was gain for the same efficiency and 1 mm on transformer footprint. This improvement was only possible with the GaN prototype since the SOI MOSFET capacitance value was given by the technology.

3.5.3 A High-Temperature Regulated Solution: Isolated Buck Power Supply

In order to demonstrate the possibility to have an efficient regulated gate driver power supply, a Flybuck prototype was designed. This prototype was built in partnership with V. Dessard from VDDconsult and is shown in Figure 3.67.

The Flybuck topology shown in Figure 3.68 is also known as the isolated buck converter, where the isolated output is generated by adding a coupled winding to the inductor of the buck [256, 69, 68]. The secondary side is looking like a flyback, but the primary side is a synchronous buck converter. The Flybuck can be regulated at the primary and makes the regulation circuit easy to design.

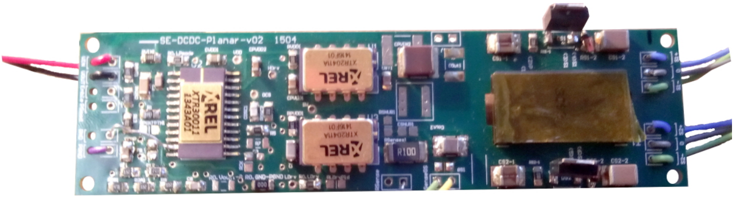


Figure 3.67 – 200 °C 3 W, 200 kHz Discrete FlyBuck Converter.

The goal is to achieve a better regulation than the one offers by the stable transfer function of the active-clamp flyback. The outputs of the flyback are set to 10 V and the load variation is realized between 0.1 to 3 W. The results on the output variation vs. the load is shown in Figure 3.69. The variation is about 7% at 25 °C and 3.6% at 200 °C. One of the advantage of the regulation at high-temperature with the SiC diode rectifier is the correction of the diode voltage drop in temperature.

The efficiency logically decreases in temperature since more energy is requested to correct the diode rectifier voltage drop as shown in Figure 3.70. The effect is not obvious under 1 W because diode voltage drop is dependent of the load current. The flyback prototype demonstrated better performances

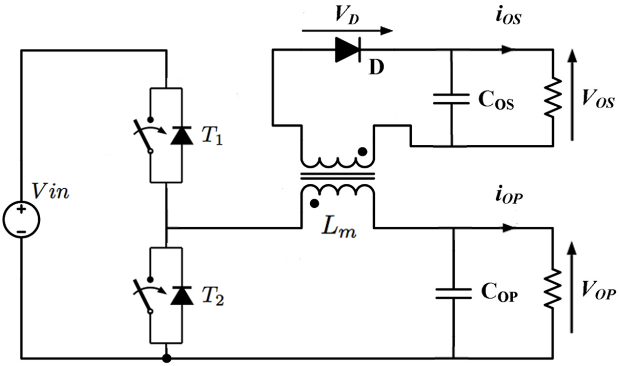


Figure 3.68 – FlyBuck converter topology.

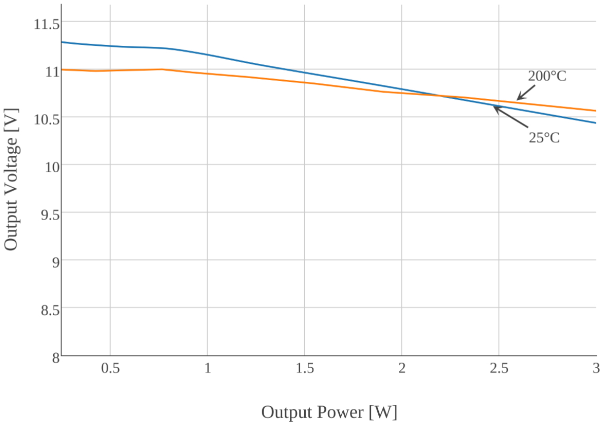


Figure 3.69 – FlyBuck output voltage variation vs. load power at 25 and 200 °C and [$V_{in} = 15V$, f_{sw}=200 kHz].

than the active-clamp flyback for its stability in temperature. However the transformer is designed like a flyback transformer where the leakage inductance has to be minimized in order to limit the current ringing on the MOSFET drain. That means a high-isolation capacitance value for the transformer and a low dV/dt immunity. The prototype transformer has an isolation capacitance about 26 pF, to be compared to the 0.7 pF in the best prototype of the active clamp flyback

The integration of this topology would be possible with an increase in the

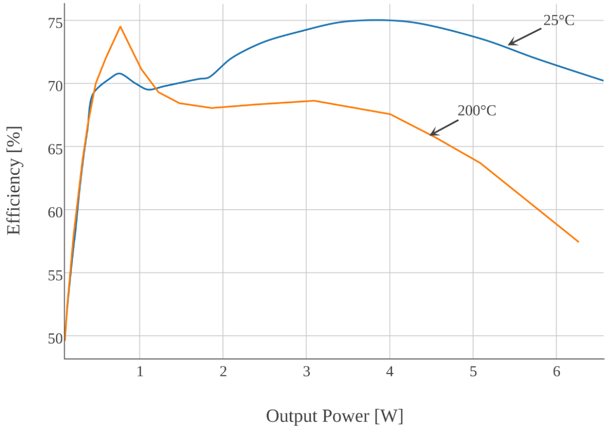


Figure 3.70 – FlyBuck efficiency vs. load power at 25 and 200 °C [$V_{in} = 15V$, f_{sw}=200 kHz].

switching-frequency for reducing the transformer size, however the isolation capacitance would still stay high.

3.6 Conclusion

In this chapter, are detailled the different approaches considered to address the miniaturization and high dV/dt immunity of a 2 W GaN gate driver power supply. The first contribution was to develop a soft-switching topology with few active components in order to have an easy integreability and a cost-effective topology for the high temperature application. The active-clamp flyback with a resonant mode was described and the design rules given.
Then as identified in the state-of-the-art, the assembly is a key point of the integration. A new concept of PCB transformer integration was performed and a high-temperature PCB selection was made. The process showed good results during the temperature cycling test and full power supply prototypes were designed. An SOI CMOS chip with protection and active devices for the active-clamp was specified and implemented on the top of the PCB with a coplanar-winding transformer.
The results show a 1 MHz active-clamp flyback SOI CMOS chip on PCB with 74% peak efficiency and 0.9 pF isolation capacitance.
As another way to address the gate driver power supply problematic, a regulated isolated buck converter was designed in order to show the advantage

of a regulation loop. The regulation loop decreased the variation of the output voltage versus the temperature. However the circuit complexity increased drastically and integration would be only possible with a chip integration and an increase of the switching frequency.
The next chapter will talk about the gate driver in the phase legs context and the gate driver power supply developed in this chapter will be implemented in a full-inverter system.

Chapter 4

Towards High-Temperature GaN Power Module Integration

Contents

This chapter focuses on the different improvements that can be made for the development of a GaN power module. Currently, only the power switches are included in commercial power module solutions. GaN and the increase in frequency call new challenges for the integration of the gate driver system. Different solutions are proposed in this perspective such as an integrated isolated current solution or a four-level gate driver for switching loss improvement. A final optimized phase-leg board included the different PhD developments, is under development. The development until the final design level will be detailed in this chapter.

4.1 Trends in WBG Gate Driver

In last chapters different parts of the power inverter module were addressed such as the gate driver power supply or the control signal isolation. In this chapter the gate driver by itself is studied and also the strategy of interconnection with the power devices.
The gate driver in the power module is a specific part for the design of power converting system. This first section will give an overview of the different challenges for the gate driver design as well as the power module since both are highly inter-dependent. The integration of the power module is a topic now highly addressed in literature [106, 24, 187]. The trends of integration includes the increased in the switching frequency, the use of WBG devices, new assembly technologies and sensing components. However even best state-of-the-art industrial solution such as the one presented in [110] with Semikron SKiN technology, does not integrate the different external solutions showed in Figure 4.1. The study presented in this chapter proposes demonstrators, solutions for a higher integration density in the power module.

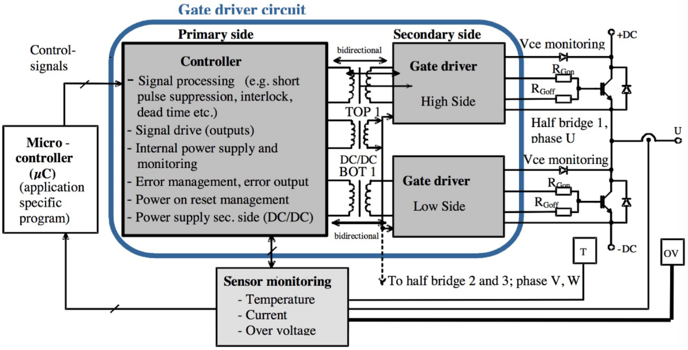


Figure 4.1 – Principle Functions in a Power Module.

4.1.1 High-temperature GaN Phase-leg Switching

High-temperature operation of gate drivers that also have high performance poses a significant challenge in both component and topology selections. The GaN devices have to be correctly addressed to fully enjoy their advantage as classical IGBT gate drivers do not provide sufficient capabilities. Has shown in Chapter 3, the SOI technology provides a good solution for high-temperature low-voltage application. Some companies such as Cissoid or XREL commercialize SOI gate driver with $250°C$ capabilities, and efficient high-temperature solution can be designed as shown in Figure 4.2.

However those commercial solutions have limitation due to the fact that they are using experienced integration technology with slow switching speed capability and large footprint package. This section will detail some improvement possible based on the current trend for GaN device.

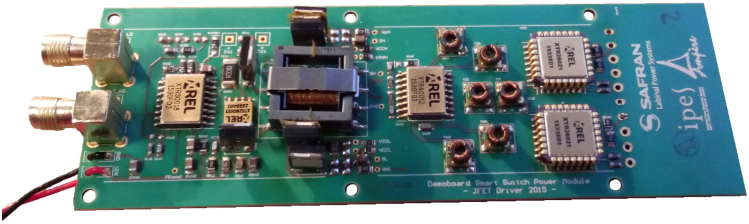


Figure 4.2 – High-temperature SiC gate driver developed at Ampere Lab with industrial partners.

4.1.1.0.1 High-Switching Frequency Gate Driver Usually there are two approaches for switching performance improvement. One is the gate driver, including active gate capabilities which senses the switching behavior such as di/dt or dV/dt, to tune gate driving strength or an intelligent gate driver which is based on the understanding of inherent characteristics of power devices to offline preset the gate drive output parameters under different switching states.The other one is the improvement of the design and the assembly of the power module in order to reduce the parasitic elements [255, 135, 209, 232, 47, 48].

The slow switching frequency of IGBT module allows the design of active gate driver to control the switching performance in order to reduce the switching losses, decrease the EMI noise or achieve fast-switching speed. The conventional gate driver can not offered the same adaptation of the switching performance [223]. The control of the dV/dt and di/dt can be performed in different way, the gate loop impedance can be modified or the gate current injection can be tuned [193, 213].

In close-loop system, a current sensor and a voltage sensor are implemented in the phase-leg in order to give a feedback on the voltage and current transient as shown in Figure 4.3. The Miller plateau can be also measured and used as a parameter to tune the dV/dt. The control loop is controlled by a

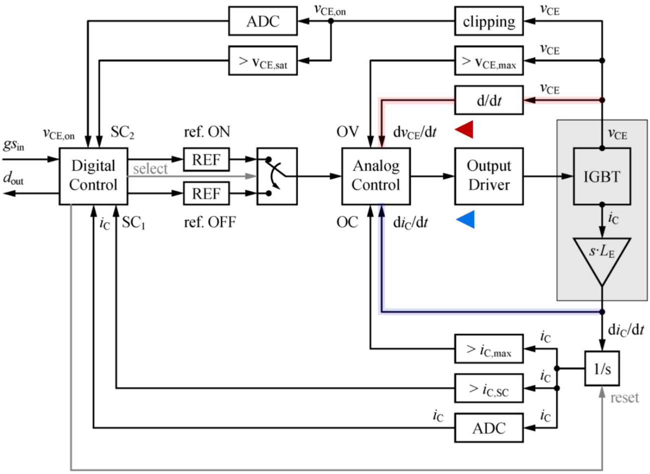


Figure 4.3 – Typical control loop for independent di/dt, dV/dt management [111].

logic digital block such as a FPGA with high-speed high-resolution D/A and A/D conversion [136, 57].
However WBG power devices with their few nanoseconds switching capability makes the control feedback loop not applicable since the control delay would be to long. To deal with this issue and improve the efficiency of power conversion, the development of a three-level driving method for GaN devices was proposed in a synchronous Buck converter which is capable of generating three different gate voltages under off-state, on-state and dead-time interval [205].
To address the GaN power device specificity, the market proposes few dedicated gate drivers. The LM5113 and LM5114 from TI are respectively dual and single gate driver presenting fast switching capabilities and a clamp system to deal with the low maximum gate voltage of GaN device [94]. The Panasonic GIT GaN device presents special characteristics with high-steady state current and a negative/positive gate voltage. In order to address those specifies Panasonic proposed a multi-stage gate driver currently includes in a IC chip [159]. [204] is presenting a dV/dt control for GaN System power device but with low dV/dt capability (60 $kV/\mu s$) by using various capacitors in parallel with the Miller capacitance C_{gd}.
The WBG devices are introducing new challenges to addressed safe driving circuit for low gate voltage, with fast switching capability. The control of the switching performance is possible but with simplified solution without close-

loop control.

The integration trends for power module is motivated by the increase in the switching frequency for the volume reduction. Fast switching frequency increases the parasitic effect in the gate and power loops of the power module. Ringing during transients are becoming a main issue and push new designs with optimized PCB parasitic inductances. Optimized layout between the gate driver and the power module is becoming something crucial to minimize parasitic elements.

Parasitics can be reduced by optimization of package such as a the combination of high and low-side device in a single module with a decoupling capacitor as show in Figure 4.4.

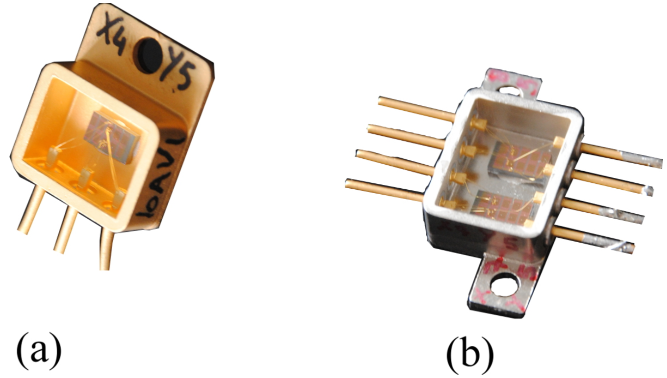


Figure 4.4 – MEGaN project discrete package optimization, a) single GaN power transistor; b) GaN phase legs in a single package.

The integration of the driver in the power module requests more effort but provides benefits: TI with the LMG5200 is the first commercially available GaN module built with EPC devices and rated at 80 V using this integration way [134, 126].

New developments are proposing also solution with GaN-based gate driver integrated in the power module package such as Navitas or GaN Systems company [107, 181]. Usually only the output buffer of the gate driver is GaN based and associated with silicon CMOS logic chip.

Another category of integrated module is using PCB as the embedded substrate for dice reported on DBC dissipation bottom substrate [240]. The PCB allows to reduce distance between power dice and gate drivers, but also to

solve the problem of wire-bond reliability. The first example is the one used it the Semikron SKiN technology with flex PCB as interconnection between power devices [110]. [60] gives an example of flex PCB interconnection with a gate driver on the flex. The European project Hi-level gives a 50 kW automotive inverter fully embedded in the PCB without any DBC [155]. Those examples do not concern the high-temperature application field but show that the PCB offers a good solution for reliable prototypes and proposes new 3D assembly with very low inductive interconnections.
As shown the high-frequency gate driver for a GaN transistor needs specific IC development to address the different challenges of this new technology such as high-frequency and low gate voltage. Integrated solutions are emerging with few commercially available products or advance multi-chip packaging assembly.

4.1.1.0.2 Crosstalk As the switching speed of power devices continuously increases, especially for WBG power devices, dv/dt induced spurious at turn-on in a phase-leg configuration is more and more common. The crosstalk effect also known as the cross-conduction effect is the interference between high and low side due to the Miller effect. The crosstalk can caused an unwanted tun-On due to the dV/dt on the drain-gate capacitance C_{dg} and possibly short-circuits the phase-leg. The phenomenon is described in Figure 4.5.

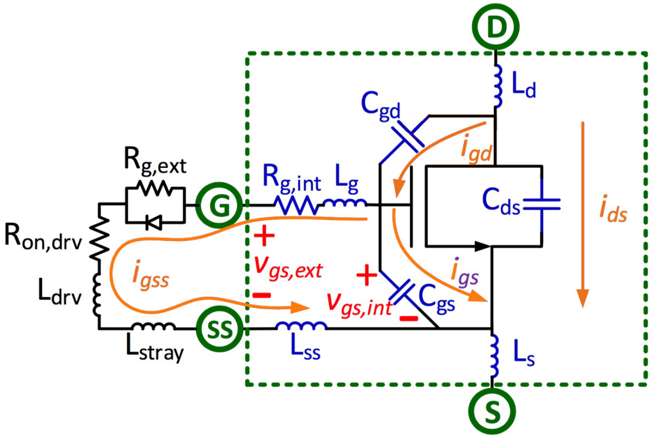


Figure 4.5 – Crosstalk effect on the high-side device of a phase leg [101].

Figure 4.5 shows the crosstalk effect for high-side power device with the

different parasitic elements. The current flows through the Miller capacitance C_{gd} to displace its charge. The same current will be split between the junction capacitance C_{gs} and the gate loop. If the gate current I_{gs} bring enough gate charge to raise V_{gs} to the threshold voltage value during low-side device turn-On, the high-side device will also turn-On and causes shoot-through losses.
Different techniques were proposed in literature to limit this phenomenon. The first one is directly on the package with the kelvin-source (SS) which limits the parasitic inductance and reduces the interaction with the power-loop [115]. Another solution consists to slow-down the dV/dt in order to limit the Miller effect. This can be achieved with different solutions, by adding an external capacitance in parallel with C_{gd} which will increase the global capacitance but increase the driving and overlap losses. Two different gate resistors can be used for tun-On and turn-Off to limit the dV/dt [229].
Another whole category of drivers called active drivers proposes solutions to control and adapt the dV/dt and di/dt in function of the load with open or close-loop as summarized in [111]. An efficient active gate drive solution with a negative voltage applied during the transient was demonstrated on SiC devices in [252] and shows good capability with few added components. In this thesis a solution will be proposed for GaN devices with a multi-level gate driver in order to deal with the crosstalk issue and decrease switching losses.

4.1.2 Current Sensors in the Power Module

The trend of electrification in Aerospace applications requires power modules to operate at very high ambient temperature, e.g. 200-250$^\circ C$. Package parasitics must be as low as possible and switching frequencies are expected in the 20kHz to 200kHz range [176, 166].

Figure 4.6 pictures an example of high-temperature module where the current sensor should take place.
In a phase leg configuration, a current measurement capability is necessary to enable a close-loop regulation; di/dt is expected to be actively controlled.
A direct measurement using a shunt resistor, or an inductor DC resistance. An indirect measurement includes current transformers, Rogowski coils and Hall effect devices such as summarize in Figure 4.7. Typically industrial applications use either shunts in high-temperature applications [150] or close-loop Hall sensors.
Close-loop sensors use magnetic core to concentrate the flux in a Hall effect device. The volume needed by the core is a limitation to integration in a power-module. Shunt-based sensors need a galvanic insulation of the

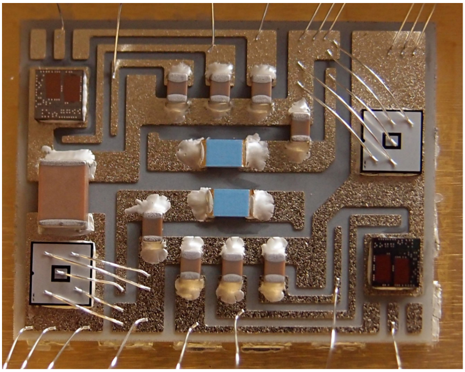


Figure 4.6 – A High Temperature Phase leg module by Ampere lab with two SiC transistors [180].

output [70]. Moreover high-temperature constraints prevent the use of a magnetic core and made all temperature-compensation system very expensive for a shunt current sensor.

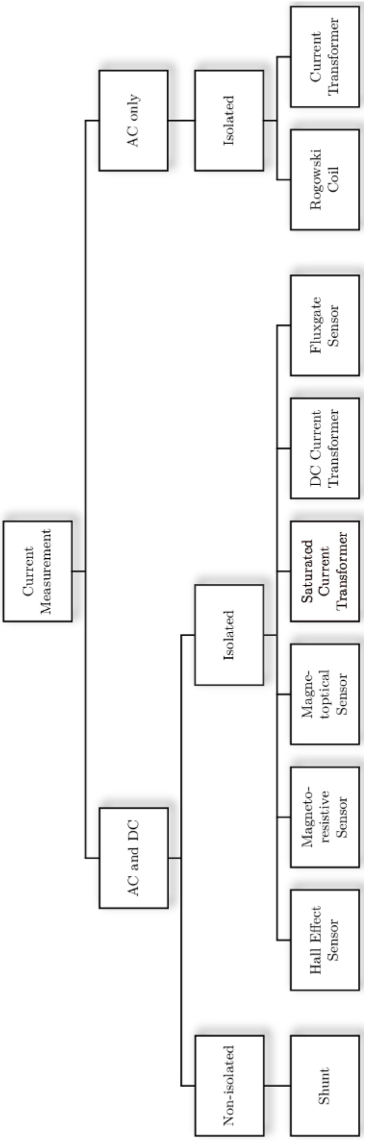


Figure 4.7 – Overview of the state of the art of different current measurement methods [230].

4.1.2.0.1 Shunt Resistor for High-Temperature The low-cost aspect is making this solution really attractive for industry. The high bandwidth and the really precise resistor value of the shunt resistor are the two advantages compared to other current sensing solutions. Ideally the shunt is a pure resistor, however all resistive material have a temperature coefficient which affects the accuracy of the resistance in a wide temperature range.
Also the size of the shunt increases with the current rating and can induce high parasitic inductance in the power loop. Another disadvantage of the shunt resistor is additional power losses and lack of galvanic isolation. The current flowing through the resistor always results in I^2R loss.

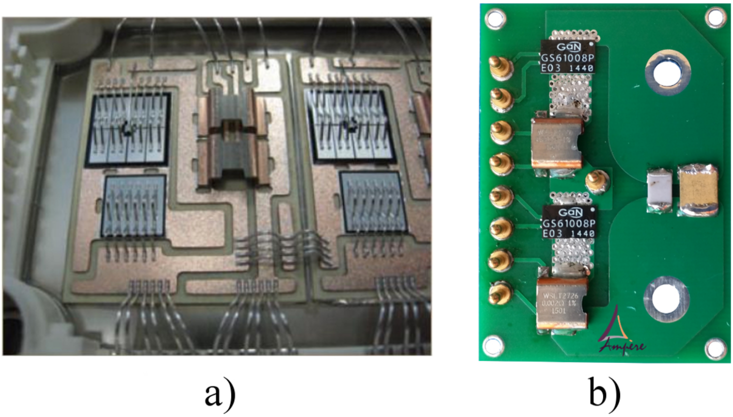


Figure 4.8 – (a) Shunt resistor in a commercial power module (Siemens SINAMICS G120); (b) Low temperature coefficient shunt resistor Vishay WSLT2726 for 200°C application.

Figure 4.8 shows a commercial power module with integrated shunt resistor and a lab protoype for high temperature evaluation of the WSLT2726 shunt resistor with low thermal coefficient. Different tests were performed for evaluating the shunt resistor as a sensor such as in Figure 4.8 (b). The parasitic added in the power loop with fast switching power devices, affect the drain current until the destruction of the power device.

4.1.2.0.2 Magnetoresistance Three main magnetoresistance types are commercially available, with Anisotropic Magnetoresistance (AMR), Giant Magnetoresistance (GMR) and Tunnel Magnetoresistance (TMR) products. Magnetoresistances are using the spin properties in the magnetic material.

The AMR effect was first described in 1857 by William Thomson [210]. Thomson observed that the resistivity of ferromagnetic materials depends on the angle between the direction of electric current and the orientation of magnetization. However the AMR presents a low stability in temperature and a short measurement field rate, which makes this sensor not suitable for current sensing [72, 95].

GMR is using the resistance of two thin ferromagnetic layers separated by a thin non-magnetic conducting layer can be altered by changing whether the moments of the ferromagnetic layers, parallel or antiparallel such as pictured in Figure 4.9 [37]. The bandwidth of the GMR is from DC to 1 MHz, and the operating temperature is from $-40°C$ to $200°C$. Both bandwidth and the operating temperature are superior to conventional magnetic-field sensing methods [106]. Different commercial products for current sensing are available on the market especially from the company Sensitec [198] and prove the capability of the GMR to address the current sensing market with an high integreability.

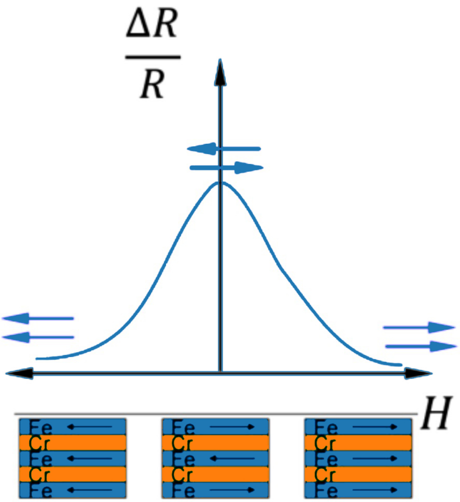


Figure 4.9 – Scattering from two different alignments of the magnetic moments in a GMR “sandwich” with two magnetic layers separated by a conducting non-magnetic layer [99].

The TMR is using a the same stack as a GMR but with an isolation layer.

This isolation layer is modulating the electrical resistance by regulating the current flow through it, as in function of an external field. This effect is called tunnel effect. In order to detect an external magnetic field using this effect, the device is configured keeping the magnetized direction of one ferromagnetic material layer (called fixed or pin layer) fixed and allowing the magnetized direction of the other ferromagnetic material layer (called free layer) to change depending on the external magnetic field.

Compared to GMR and AMR, the TMR has a better sensitivity with 20% (only 2% for AMR). It presents a really small volume and low-cost since it is also widely used in the hard disk read head or MRAM memory.

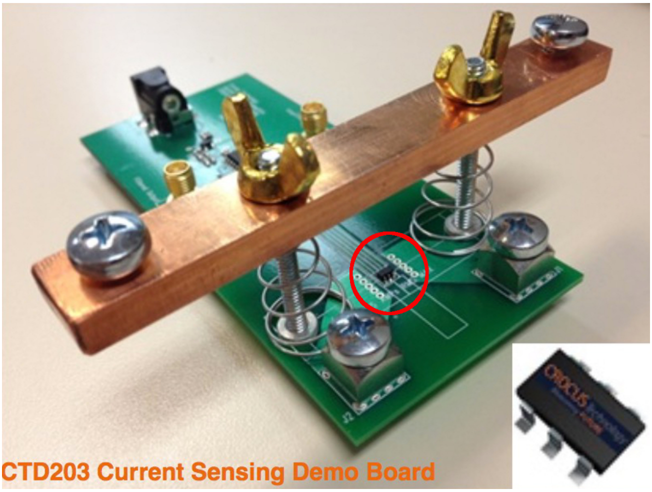


Figure 4.10 – CTD203 TMR Current Sensing Demo Board.

One company is commercializing a TMR based current sensor with a sensitivity of 86 mV/A [171]. The solution in Figure 4.10 showed good stability in low-temperature with a maximum test temperature at 85°C [202].

4.1.3 Physical Health Monitoring

This point is not developed in this thesis but an overview has to be given because of the important place of the gate driver in the reliability monitoring system. Indeed, the gate driver is the component directly connected to the power device and has to be able to sense and transmit the data.

It is also important to make the difference between reliability and health-monitoring. Health-monitoring is based on a model for the lifetime prediction of the power device or full system as shown in Figure 4.11. The reliability of power device is more focused on the identification of the failure mechanisms. For example, as shown in [192, 156], the reliability of SiC MOSFET is mainly dependent on the gate oxide aging. Different accelerated cycling tests showed a good lifetime prediction based on this parameter. Based on mathematic laws such as Gamma process or Weibull law, it is possible to give an estimation of the device lifetime.The IEC International Standards for semiconductor devices such as IEC 60747-34 and IEC 60747-9 [90, 89] define endurance and reliability test setups. However, the exact procedures are mostly adapted by the manufacturer for each product.

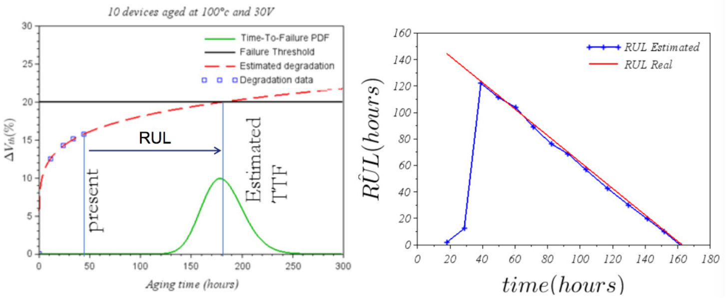


Figure 4.11 – Accurate Life time prediction for SiC MOSFET based on a stochastic approach [192].

The prognostic of the aging of a power module is therefore possible with the monitoring of identified variables such as gate leakage current or threshold voltage in the SiC MOSFET case. [66] shows that the monitoring of the VCE_{sat} compared to a minimum value allows an estimation of the power device aging. However, in the case of a power module, the assembly degradation mechanisms such as CTE issues or wire-bonding cracking, can not be predicted based on electrical measurements and make the reliability prediction more complex. However, a solution [42] based on the temperature measurement into the power device chip shows good results to estimate the assembly degradation with the solder join between the chip and the substrate.

It can be seen that the measured parameters requested for the life-time prediction are intrinsically situated in the power device. The role of the gate driver for the life-time prediction is to be the interface between the power device and the control board which is processing the data from the power device. It has to be taken into account in gate driver design to include sensors acquisition and communication lines for a better estimation of the power module life-time.

4.2 High Temperature Current Sensor Solution based on Tunnel Magnetoresistance Effect

Magnetoresistance with small size devices and insulated current measurements is a good candidate for current sensing in a integrated power module [153, 231, 199]. Literature is mostly addressing the high-temperature magnetoresistance behavior without real application as a sensor [92, 212]. The work presented in this chapter proposes a current sensor solution based on a magnetoresistance chip with a high-temperature characterization. The specifications required for a power module application are given. A comparative test is performed between different commercial magnetoresistance devices. One component is selected for high temperature test and experimental results are detailed and discussed.

Table 4.1 – Typical specifications for a current measurement in a high temperature power modules.

Parameter	Nominal
Type of transducer	Bidirectional Current Mes.
Bandwidth of transducer	0(DC) — 15 kHz
Dynamic Range	0 — 30 A
Nominal Current(min. error)	5 A
Max.Over Current	35 A
Temperature Range	-50°C — 250°C
Current Consumption	10 mA
Supply Voltage	5 V
Type of Output Signaling	Single ended(Non differential)
Resolution	0.01 A
Error at all range of temp.	3 %

In order to give a context to this study, Table 4.1 is giving the targeted specifications required for the integrated current sensor. In Magnetoresistance (MR), the measured parameter is the magnetic field produced by the current. The magnetic field can be determined over all the geometry of the power module if the current is known and the geometry constant. Ever the relation between the magnetic field and the current is complex and a finite-element approach is a necessary practical approach due to the high-complexity of the floor planning in a power module substrate.

An analysis is proposed on a set of a current traces taken as a vehicle and

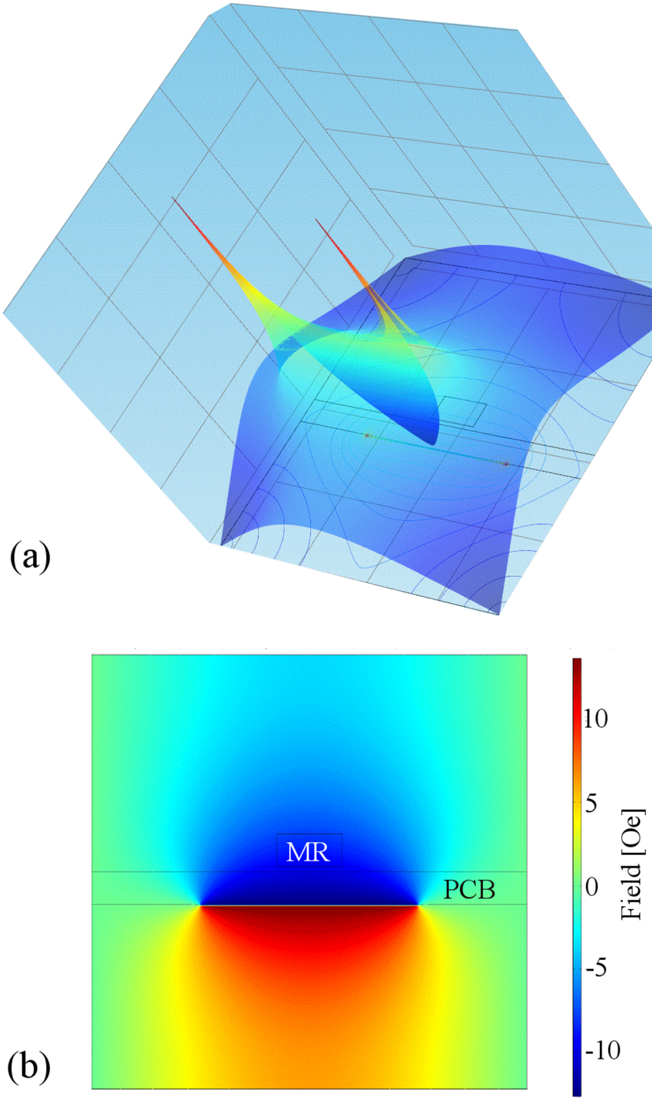


Figure 4.12 – FEM simulation of the current field repartition in a bus-bar a); and for the MR positioning b).

fabricated on a standard FR4 printed circuit board. FEM simulation evaluates the ampere-to-tesla relation [106] and the maximum current before MR saturation. The MR position on the bus bar impacts the current range allowable with respect to linearity range. The results of a FEM simulation for the positioning of the MR on the PCB shows that the current in the bus bar is not constant and actually concentrated at the edge as shown in Figure 4.12 (a). According to the FEM simulation in Figure 4.12 (b), a PCB test board is designed to perform a comparative test between commercial products.

4.2.1 TMR Selection and Evaluation

Four different MR devices are tested in order to validate previous simulations and check suitability: KMY20S (Sensitec Measurements), MMLP57F (Dowaytech MultiDimension) and AA005/AA002 (NVE Inc).

These devices present different MR architectures, MMLP57F is a TMR, but AA005 and AA002 are GMR devices. Due to limitations in temperature excursion that the PCB allows (FR-4), the devices have been tested at ambient temperature. The four different sensors are placed on a bus-bar with the exact same geometry conditions in order to have a precise comparison. The current is applied on the bus-bar and the created field is the same for each sensor. Criteria of linearity, hysteresis and measurement accuracy at ambient temperature are used to performed the comparison between each solutions.

Figure 4.13 shows the device behaviors at ambient temperature. This tests allows to check if MR device can achieve a bidirectional current sense. Device 1 features a poor sensitivity. Devices 3 and 4 are not suited for measurement of bipolar currents.

Device 2 (MMLP57F) is selected for the high-temperature test. The results indicate that the best suited device for the application is MMLP57F. The device sensitivity is 10.04 mV/A over ±30 A. Linearity is better than ±1%. We can explain this sensitivity by the TMR structure which offers a best variation of the resistance for the same current range. Nevertheless, TMR device allows to measure a current in two directions without post-treatment. All further testing and calculations will be realized only with device MMLP57F.

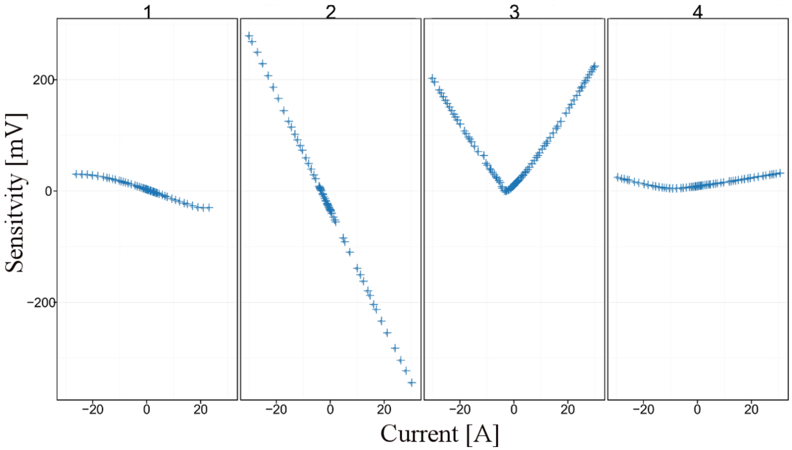


Figure 4.13 – Output voltage response vs. a 60 A current span at ambient temperature: (1)=KMY20S, (2)=MMLP57F, (3)=AA002 , (4)=AA005

4.2.2 TMR Current Sensor Design and Test

A PCB specified for high temperature is shown in Figure 4.14 based on a 35N polyamide substrate. It includes two TMR devices with different bus bar geometries and a PT1000 temperature sensor for a local control of the heat generated by the high-current bus-bar value.

Signals are captured from the oven environment thanks to dedicated coaxial-wires specified up to 250°C.

Table 4.2 – Table of conditions for measurements.

Parameter	Value
Device	MMLP57F
Temperature	-40 to 250°C
Supply	Constant Current: 0.015 mA
Apapratus	BKPRECISION + 2 X Keithley Multimeter
Shunt value	0.001035 Ohm

Tests are performed at constant voltage supply and constant current supply. The results are very similar in both cases but the output in the case of a current supply has a bigger range because of the Westhone bridge response.

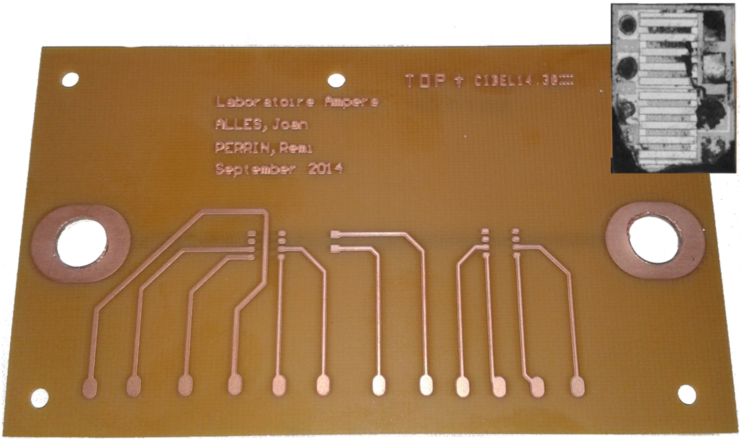


Figure 4.14 – Polyimide test vehicle and TMR chip devices obtained after the attack of the package by acid.

Measurements are performed at $-40, 0, 50, 100, 150, 200$ and $250°C$ Celsius degrees in order to obtain a model of the response using a linear regression.

The output is plotted versus the current for each temperature in Figure 4.15.

Figure 4.15 shows that the higher the temperature the smaller the slope decrease. The offset also varies between different temperatures.

Once the multivariate linear regression is performed and through the observation of the residuals and its distribution, its is possible to determine the resolution of the current sensor and the accuracy of the model. Figure 4.16 shows the results and allows to determine the resolution of the current sensor.

The error is about $\pm 0.1A$ in the range -30 A to 30 A (i.e a 0.33% of error). Maximum resolution with this prototype is therefore 0.2 A and makes this solution suitable as a current sensor in measurement or protection application. Equation (4.2) gives the relation between temperature T and the sensor output voltage V_{out} to have the current value. The equation is extracted from the experimental results in Figure 4.15.

$$
\begin{aligned}
I = 0.097 + 0.816V_{out} - 0.01458T + 0.00004985T^2 - 0.0001435V_{out}^2 + \quad (4.1)\\
+ 0.0044TV_{out} - V_{out}(0.00002T^2 - 0.0054T - 0.03) \quad (4.2)
\end{aligned}
$$

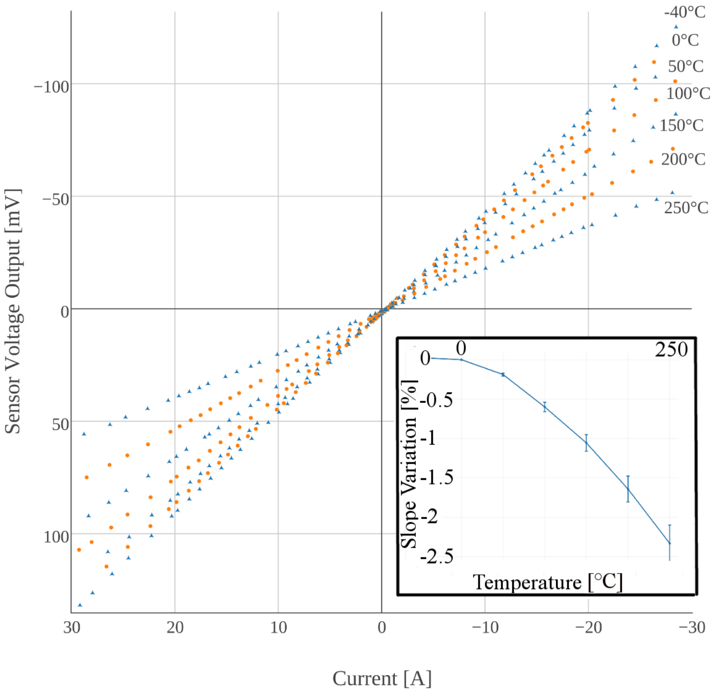


Figure 4.15 – Experimental response at constant current for different temperature steps between -40 to 250°C.

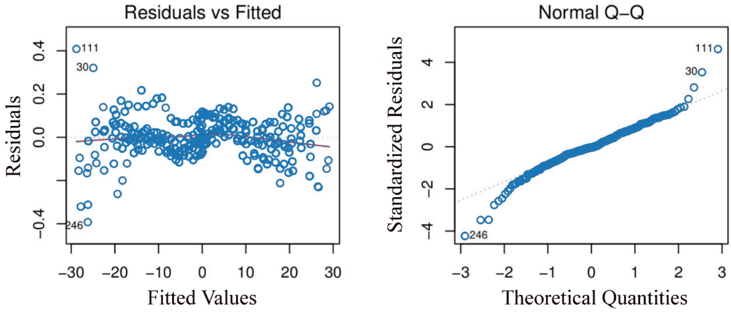


Figure 4.16 – Residuals vs fitted values and the test of normality.

4.2.3 TMR Current Sensor in a Overcurrent Protection Function

In Fig. 4.17, the polyimide prototype is placed in a phase of a power stage. The TMR current sensor is monitoring the load current. The inductive load (180 uH) is in parallel of the buck diode. Current protection limit is set to 40 A in the gate driver configuration, and the switching frequency is 20 kHz.

Figure 4.18, shows the measured waveforms on the test board. The TMR output voltage (green curve) is able to measure the overcurrent in the phase-leg and by using the gate driver XTR26020 from XREL, it is able to activate the protection mode. The TMR current sensor gives a good reproduction and a fast isolated picture of the load current.

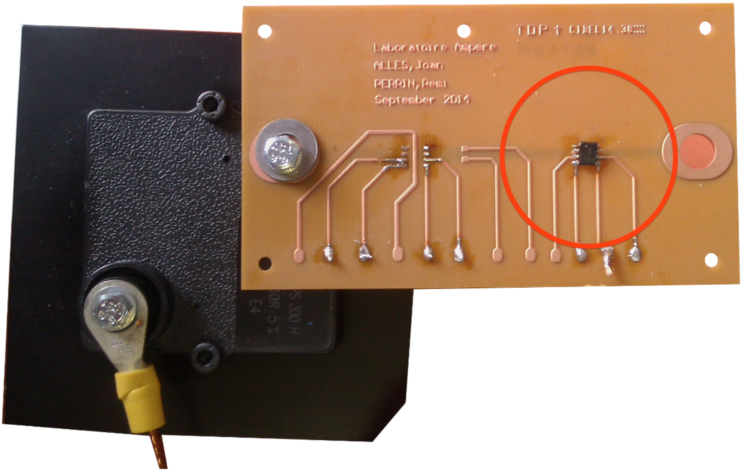


Figure 4.17 – TMR current sensor on the load circuit at 25°C.

The TMR-based current sensor showed good measurement capability and offer an integrated isolated solution for current protection in power-module. The temperature variation can be easily managed by measuring the temperature in the power module and compensate it at the control board level. The linearity of the TMR sensor allows a simple correction in temperature based on Equation (4.2).

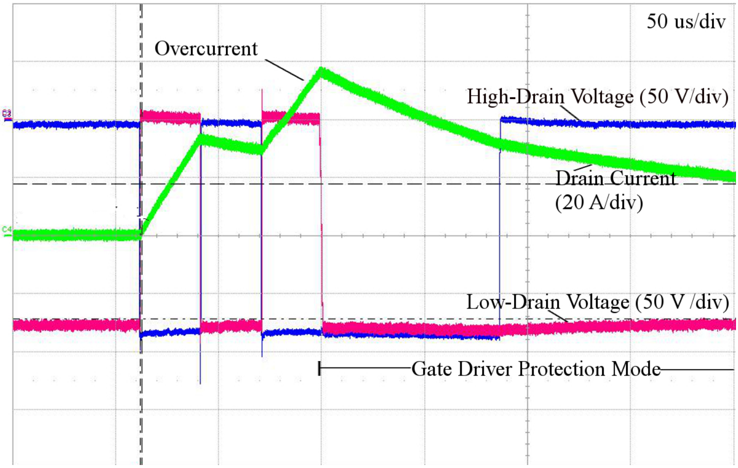


Figure 4.18 – TMR current sensor in an overcurrent protection application; drain voltages of the phase-leg (blue and red) and the load current (green).

4.3 Four-level Intelligent Gate Driver for E-mode GaN FETs

Multi-level gate driving has been demonstrated previously [252] for achieving better turn-On and turn-Off by reducing overlap losses and shoot-through losses. In this section, a four-level gate driver for GaN power stage is proposed based on a dual-isolated gate driver. Conventional gate driver controls the gate voltage while the source is fixed to a reference. The four-level gate driver proposes to control independently the gate and the source voltages with floating references and which allows four different levels of gate voltage.

A three-level driver for dead-time optimization in a 7 MHz GaN converter is presented in [205] but with a much higher circuit complexity. The challenge of this work is to increase the switching speed while keeping the gate voltage in the datasheet level for GaN devices which are sensitive to overvoltage [100].

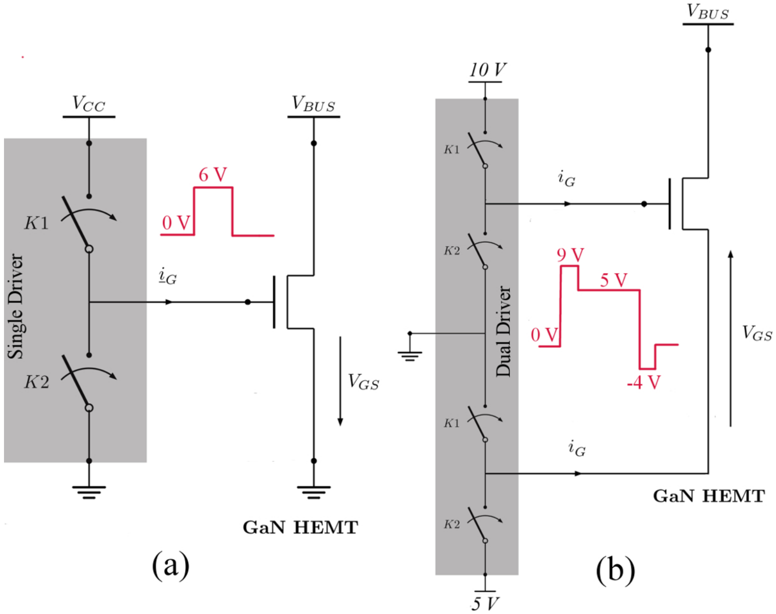


Figure 4.19 – Conventional single gate driver and intelligent gate driver with dual gate driver.

4.3.1 Principle of Operation of a Four-Level Driving Circuit for the eGaN FETs

The proposed intelligent gate driver circuit and the logic signals of its corresponding transistors are shown Figure 4.20 and Figure 4.21.

There are four switching intervals in one period as detailed below:

- Subinterval 1 $[t_0, t_1]$ The high-side power switch is driven with a 0 V gate voltage the device is Off. The low-side power switch is driven with a 5 V gate voltage, the device is On. No loss during this interval.

- Subinterval 2 $[t_1, t_2]$ The high-side switch stays at 0 but the low-side is switched to -4 V in order to absorb the crosstalk effect during the next inerval and to realize a ZVS during the turn-Off. This interval is part of the dead-time. Since the device is driven with a negative voltage, reverse conduction losses are present as well as turn-Off losses.

- Subinterval 3 $[t_2, t_3]$ This interval is the turn-On transient time. The gate voltage is maximize up to 9 V in order to have a higher gate-current

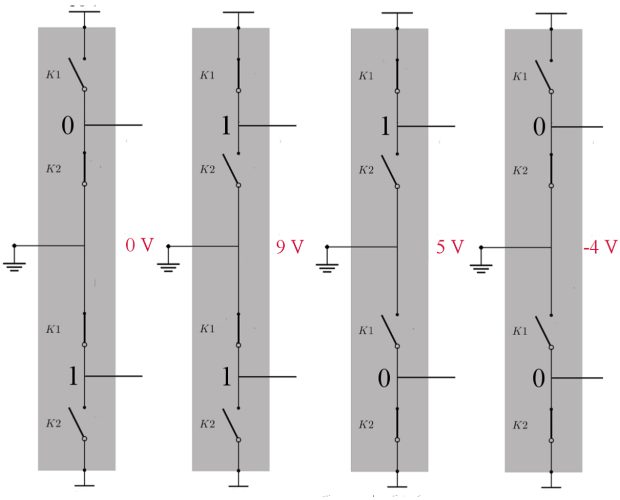


Figure 4.20 – Corresponding logic signals for high and low-side of the dual gate driver for the 4 different levels.

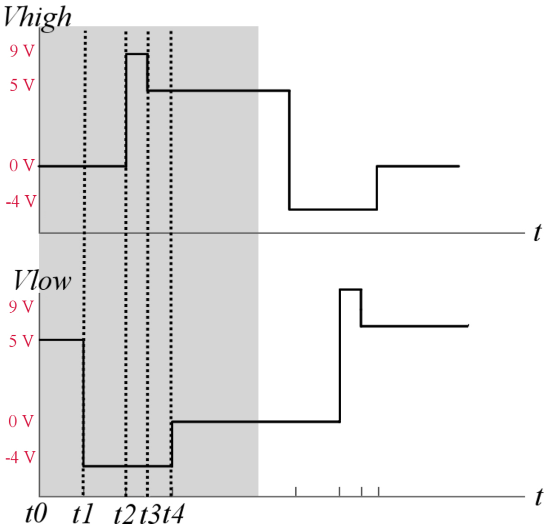


Figure 4.21 – Gate voltages for low and high-side of the phase-leg.

flowing through the gate capacitance C_{gs}. The transient speed is higher and switching losses reduced. During this interval, conduction losses and turn-On losses are present. This interval is part of the dead-time.

- Subinterval 4 $[t_3, t_4]$ The switching time is over, both high and low-side power switch have stable drain current and voltage. No loss during this interval.

As described the total switching loss are the sum of On and Off losses plus dead-time losses. Crosstalk losses are considered null since the -4 V negative voltage is applied during transient. The global switching losses can be estimated as given in Equation (4.3) and Equation (4.4).

$$E_{sw} = E_{on} + E_{off} + E_{dt} \tag{4.3}$$

$$E_{dt} = t_{dt}(V_{sd_{-4V}} I_{load} - R_{ds-on} I_{load}^2) + t_{dt}(V_{sd_{0V}} I_{load} - R_{ds-on} I_{load}^2) \tag{4.4}$$

Based on the loss evaluation model of [101, 100] and Equation (4.3), a global estimation of the switching losses is showed in Figure 4.22 for conventional and intelligent gate driver and for different temperatures.

A Spice simulation models was built based on the modified model from

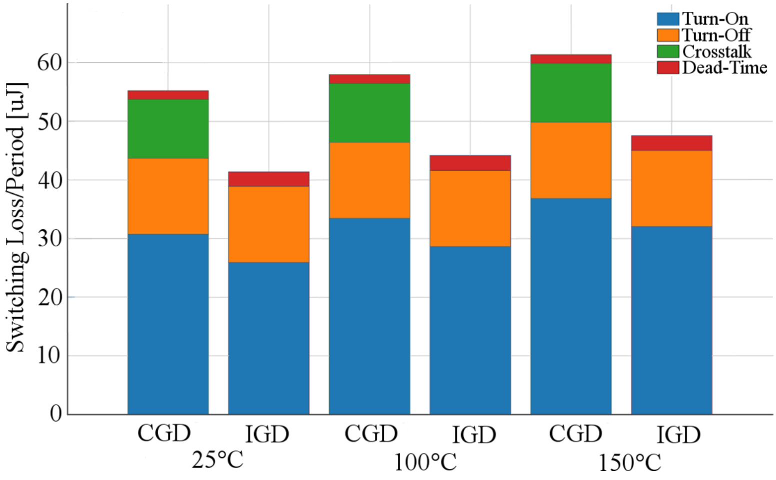


Figure 4.22 – Analytically estimation of the conventional (CGD) and intelligent gate driver (IGD) impact on the switching loss for one period at 400 V, 10 A and for different temperatures.

Section 1.4 in order to corroborate the previous analytic estimation as shown in Figure 4.23. In this model the different rise and fall times were taken into account such as Digital Signal Processor (DSP) delay of 5 ns and 10 ns for the gate driver used. The simulated switching loss difference between the two different gate driver is shown in Figure 4.24.

In Figure 4.24, the simulation results for the conventional gate driver slope is

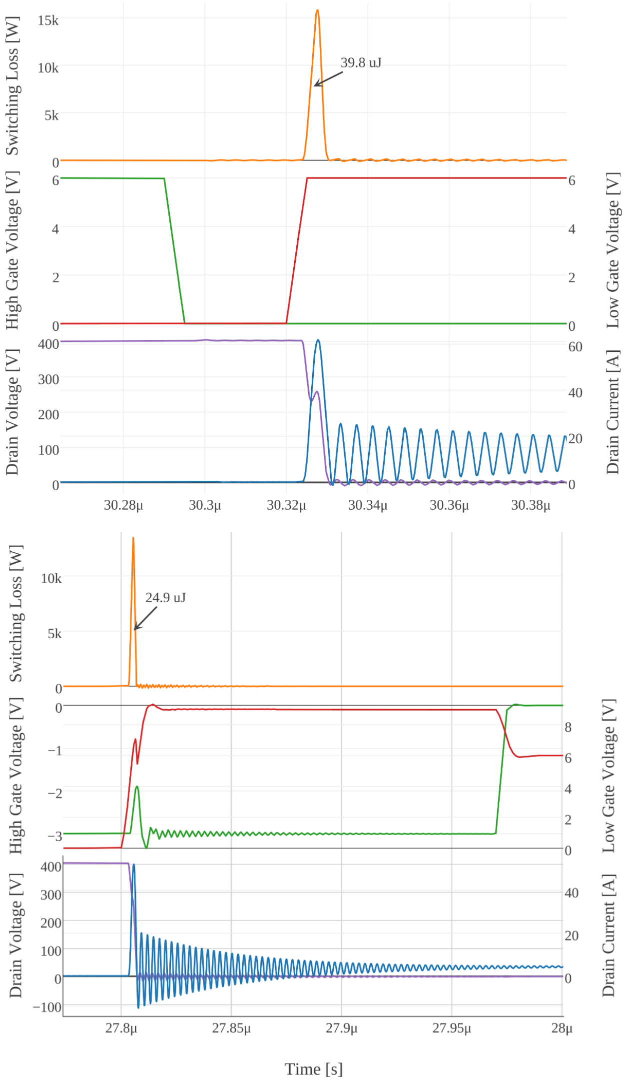


Figure 4.23 – Simulated switching loss for conventional and intelligent gate drive at 400 V, 15 A, 25°C.

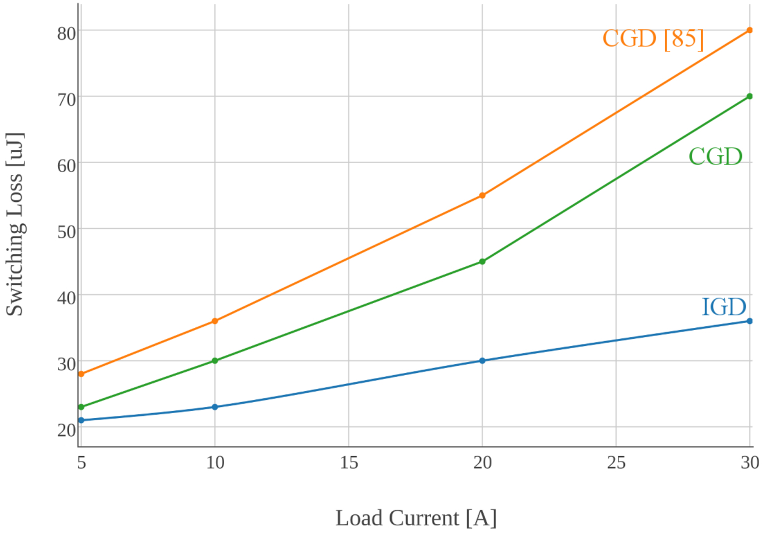


Figure 4.24 – Spice simulated switching losses for conventional and intelligent gate drive at 400 V, 25°C and experimental switching loss from [101].

following the same trend as the experimental values, but is shifted due to the difference in the parasitic model values. The validity of those results will be discussed with an experimental case in next section. However it can be seen that for a 400 V 30 A, a maximum switching loss point reduction of 50 % is showing the pertinence of the proposed solution.

4.3.2 Experimental Results and Analysis

A double pulse test with GS66508 GaN HEMT in a phase-leg configuration is established for experimental verification, as shown in Figure 4.25. The dual gate driver used for this board is the Si8275 from Silicon-Labs with a high dV/dt immunity specified up to $250kV/\mu s$. A specific care is taken to reduce the inductance loop between the gate driver and the power device. No external gate resistor is used besides the internal gate driver one.

The gate driver power supplies are two Murata NMS0505 with an isolation capacitance given at 2 pF in order to limit the common-mode current path. Two adjustable regulators allow to customize the gate voltage level.

Drain current and voltage measurement points are using coaxial shunt resistor and coaxial connector in order to reduce the measurement inductance loop and also the current level in the measurement loop. This board was designed and tested at Curent Lab Tennessee, USA, during my internship.

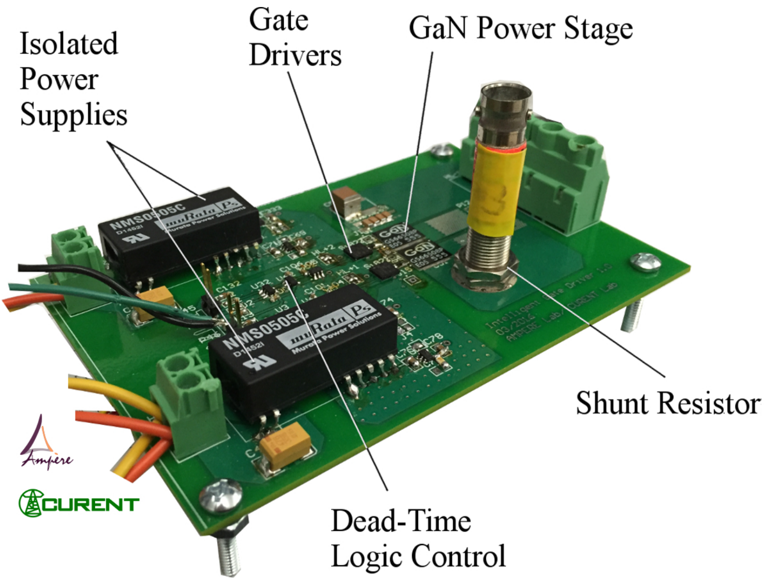


Figure 4.25 – DPT Intelligent Gate Driver Board in GaN phase-leg configuration with GS66508 HEMTs.

The board allows to switch between the two different gate driver modes (IGD and CGD), with the control signals. In order to prove the effectiveness of the solution, comparison experiments under different drain ratings were performed.

The testing conditions shown in Figure 4.26, keep the high-side switch short-circuited at 0 V and the low-side switch is controlled with the four-level gate signal. The 10 V pulse is kept as short as possible, 40 ns, in order to limit the overvoltage on the gate. The negative voltage step is a 4 μs pulse. The different levels are controlled by doing the difference of the two logic signals of the dual gate driver. The switching frequency is fixed at 20 kHz.

As the dV/dt speed impacts directly switching losses, a first measurement evaluation was to optimize the 10 V pulse. The duration was optimized in order to have the best spike. The first point is that the duration of the pulse does not impact the dV/dt speed. Therefore, the duration should be fixed as short as possible in order to reduce the stress on the gate. This parameter stays stable for different load current. In order to limit the overvoltage on the

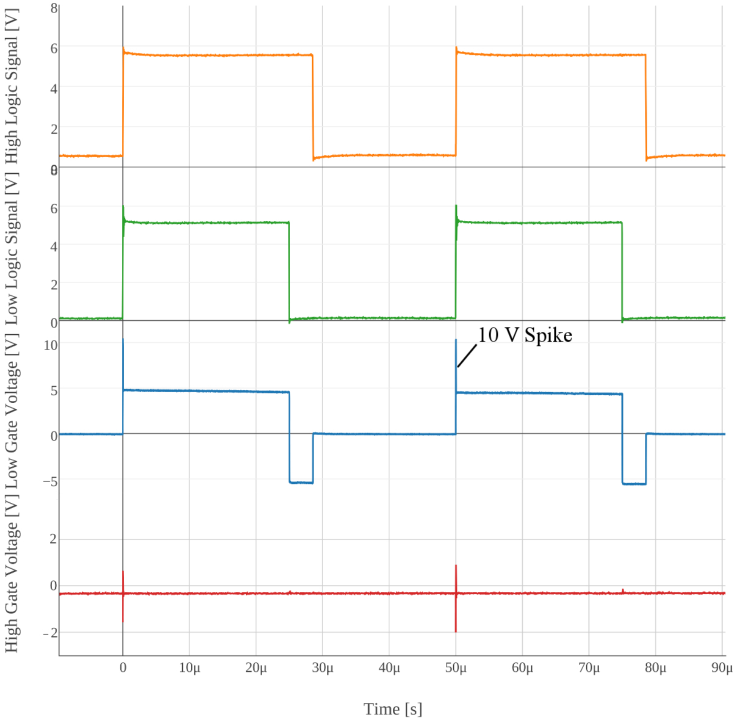


Figure 4.26 – Low-side control logic signals and high and low-side gate voltages for the DPT board.

gate, 9 V maximum gate voltage was chosen instead of 10 V.
The loss improvement evaluation was performed under different load current between 1 to 20 A and for 200 and 400 V with a 9; 5; 0; -4 V gate voltage. A comparison point with a conventional gate voltage 0; 5 V was made for each load current point too. The loss calculation is performed as shown in Figure 4.27. The dV/dt improvement is obvious even for small load current and low voltage. The switching losses are reduced due to the shorter switching time. The current peak is higher since the dV/dt is higher, but the drain ringing voltage stays limited.
The results are summarized in Figure 4.28. It can be seen that the maximum gain in switching losses is up to 26% at 400 V, 20 A and 22% at 200 V, 20 A.

The switching loss improvement is limited for small load current due to the low current requested by the gate capacitance. Therefore, the extra gate

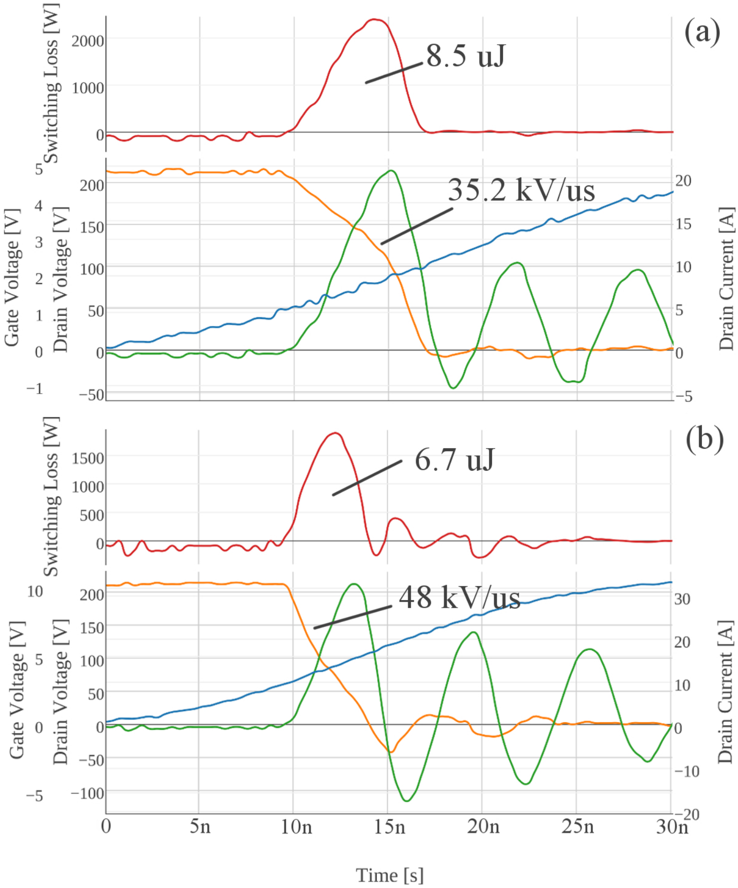


Figure 4.27 – Experimental switching loss calculation at 200 V, 5 A, a) for CGD; b) for IGD.

current proposed with the IGD does not have a strong effect on the switching speed.

The maximum dV/dt reached with IGD solution at 400 V, 20 A was about 203 $kV/\mu s$ against 172 $kV/\mu s$ for the CGD solution.

As a conclusion, the simulation model presented gives an over estimated value but gives the right gain between conventional and intelligent gate drivers. The switching loss improvement is important and the increased in the reverse conduction losses are not significant in comparison. Intelligent gate driver is

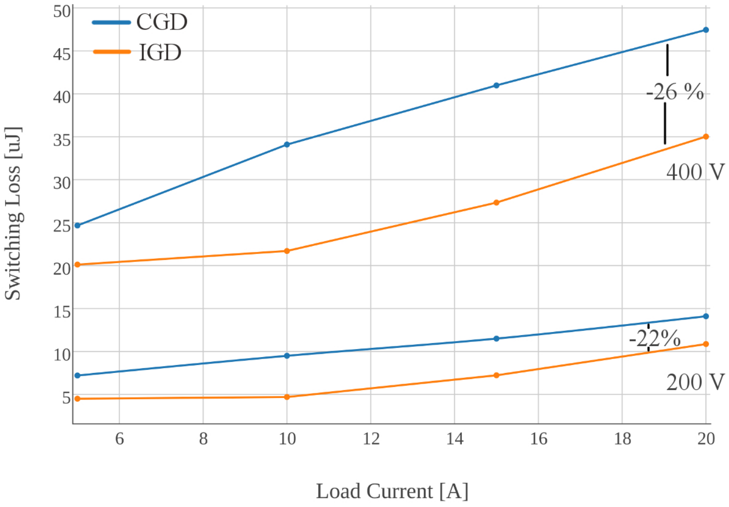


Figure 4.28 – CGD and IGD solution experimental switching loss at 200 V and 400 V for different load current at 25°C.

particularly suited to GaN HFETs, due to extremely low C_{gs} and high di_g/dt, and offers further improvement. Future test will target the temperature effect on this solution.

4.4 High-Temperature GaN Phase-leg Design

4.4.1 Selection and Modeling of External Circuit Components

The external circuit components in the phase-leg circuit are corresponding to the passive components such as DC capacitors but also current protection and gate driver Integrated Circuit (IC). These components also play very important roles in determining the fast switching behavior of the main switches, so it is necessary to consider all of them in order to have simulation results as close as possible to the real switching waveforms with detailed spikes and ringings. The following sections discuss the modeling of these components.

Gate Driver IC The gate driver IC used in the test is the XTR26020. The SPICE model of this chip is not available and has to be performed. However doing exact spice model of the full driver architecture is quite complicated and cannot be translated into SPICE template directly. So a simplified SPICE

model is built. The output totem-pole structure of the gate driver is using 40 V SOI MOSFET.
The parameters of this MOSFET are given by the manufacturer and can be included in a conventional SPICE MOSFET model (M_3, M_4). The logic requested by the totem-pole is done with conventional LTspice digital components as shown in Figure 4.29. The output resistance of the model is also adjusted to the datasheet rise and fall times (R_1, R_2).

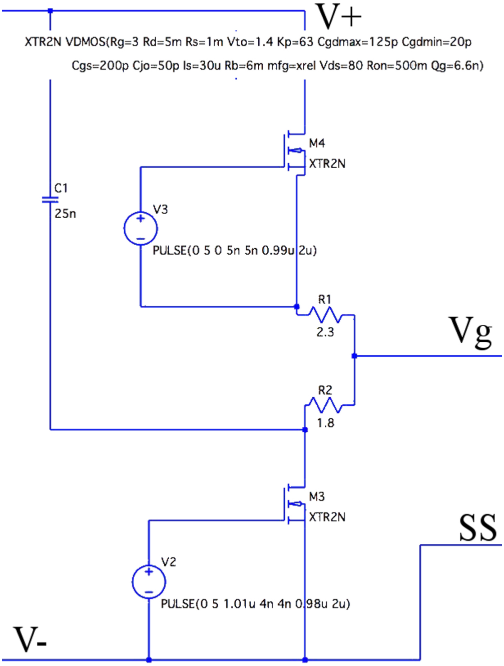


Figure 4.29 – XTR26020 Spice Model.

Current Protection An isolated TMR based current sensor was developed during this PhD, however the choice of the gate driver and the expensiveness of the SOI logic components for its implementation pushed us to use the shunt solution.
For this current protection, a Vishay WSLT2726 shunt resistor with 4 terminals and 0.003 Ω value is chosen. This shunt resistor has a low Thermal Coeffcient of Resistance (TCR) (<20 ppm/°C) which allows a maximum operating temperature of 275°C. In order to perform the model of the shunt,

parasitic inductances for the measurement and power sides are measured with an impedancemeter (Agilent 4294A).

As shown in Figure 4.30, the inductance for the power loop and the measurement loop are measured separately. The power inductance L_p is measured at 3.4 nH and the measurement inductance L_m at 5.2 nH. The inductance values does not change with temperature.

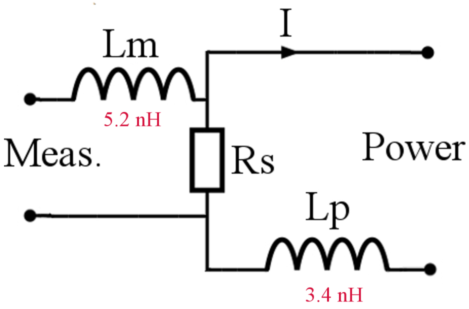


Figure 4.30 – WSLT2726 shunt resistor model.

Load Inductor In the test setup the inductor used is optimally designed to have a good frequency behavior with a high-frequency limit point. The inductance is not affecting the maximum switching frequency of the test setup. However as shown in [253] the target application of an inverter is a motor drive, and the impedance of the cable added with the motor inductance one are modifying the impedance of the power loop as shown in Figure 4.31. The lower impedance path increases the switching losses and decreases the maximum switching frequency of the system.

A solution with air-inductor filter on the motor-cable is proposed in [254] to limit the effect of the motor impedance on the phase-leg and also to reduce the dV/dt on the motor in the case of high-switching frequency power system.

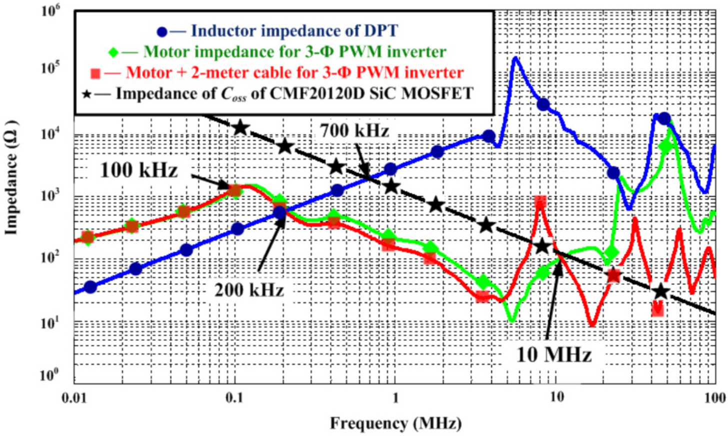


Figure 4.31 – Impedance comparison among different inductive loads [254].

Decoupling Capacitor The capacitors used in the phase-leg configuration, namely the DC bus bulk and decoupling capacitors, as well as the gate driver power supply capacitors, are also modeled. The parasitic Equivalent Series Resistance (ESR)s and Equivalent Series Inductance (ESL)s are taken into consideration in the capacitor modeling, as shown in Figure 4.32. These parameters affect the high-frequency ringing during the fast switching transients and have to be taken into account in the simulation.

The method to determine bus decoupling capacitors bank value is barely addressed in literature. However a rule of thumb is proposed in [49] based on the C_{oss} power switch capacitance value. The model establishes the relationship between the power switch parasitic ringing at turn-Off and the impedance seen by the device during this transient based on a small signal model. In order to limit the ringing on the DC-bus the ratio between the decoupling capacitor and the C_{oss} has to be higher than 50.

Figure 4.32 – Serial Capacitor Model.

However as reported in [120] the effect of the decoupling capacitor bank on the drain overvoltage is highly dependent on the parasitic elements in the circuit and the value of the bus decoupling capacitor has to be customized for each

design. In our prototype a C_{oss}/C_{dec} coefficient of 200 was used.
On the other hand the capacitor type has to be determined for high-temperature. The high-temperature capacitors selection was already presented in Section 3.1 for low-voltage application. However, in a phase-leg configuration, high-voltage capacitor are requested for the bus-decoupling capacitor bank. The first solution proposed on the market is to stack COG capacitors in order to increase the capacitance value for voltage breakdown up to 1 kV. This solution is called Multi-Layer Ceramic Capacitor (MLCC). However as shown in [221, 179, 25], in high-temperature cycling conditions, the capacitor stack shows insulation degradation and flex cracking due to the mechanical stress on the assembly.
Another capacitor technology called metallized dielectric film capacitors are preferred for high reliability applications due to their ability to self-heal [220, 31]. For many years Polytetrafluoroethylene (PTFE) has been used as a dielectric material for capacitors due to its stable electrical properties [217]. However, traditional sources of PTFE films have limited dielectric strength and a maximum operating temperature around 155°C [182].
Based on the PTFE material, Gore company has developed HBS PTFE film capacitors with extended characteristics [62, 63]. This new dielectric film presents a high-stability up to 250°C with a good impedance behavior in high-frequency. A 7 μF, 600 V sample shown in Figure 4.33, was tested at Ampere lab [15] up to 200°C. The measured impedance behavior at 0 V between 25 to 200°C shows a perfect stability of the capacitor, as shown in Figure 4.34 which corroborates the results of [62]. This capacitor was selected.

Figure 4.33 – 7 μF 600 V PTFE Gore Capacitor.

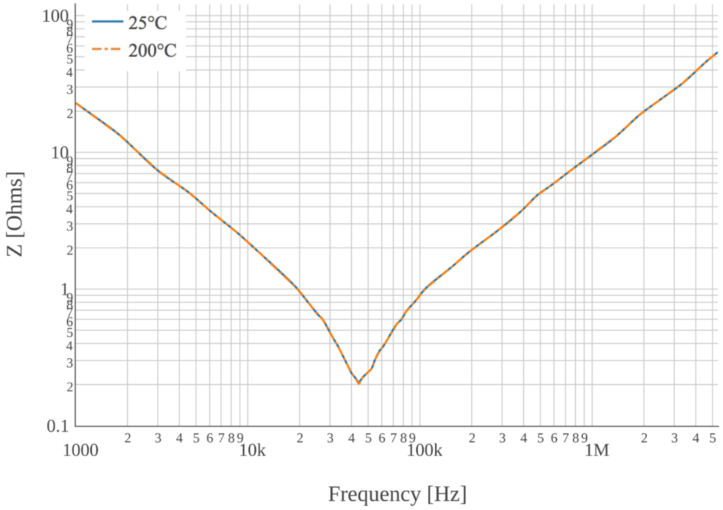


Figure 4.34 – 7 μF 600 V PTFE Gore Capacitor Impedance Evolution [15].

FEM PCB layout Parasitics Extraction Another method adopted in many works is the simulation-based method, which extracts the package parasitics using Finite Element Analysis (FEA) or Partial Element Equivalent Circuit (PEEC) methods. Electromagnetic analysis software such as INCA and Ansoft Q3D have been used in these works for the parasitics extraction [43, 234, 168].
The FEA method provides the value of any interconnection of the geometry and can be analyzed numerically. The separated interconnects without physically measurable inductance can also be evaluated based on the well-established concept of partial inductance, and the mutual terms can be taken care of automatically as well [239].
Moreover, some electromagnetic analysis software also provide interfaces for commonly-used circuit simulators such that the evaluation results can be directly used in circuit simulations to see the impacts of the parasitics. For the reasons stated above, this work adopts the simulation-based method to evaluate the PCB parastics. The software used in this work is Ansoft Quick 3D Extractor, coupled with LTspice to perform an accurate simulation of the inverter system. The modeling process of the PCB layout is illustrated in Figure 4.35.

Both gate and power loop inductances were optimized following the procedure in our design. The gate loop is situated between the gate driver and the

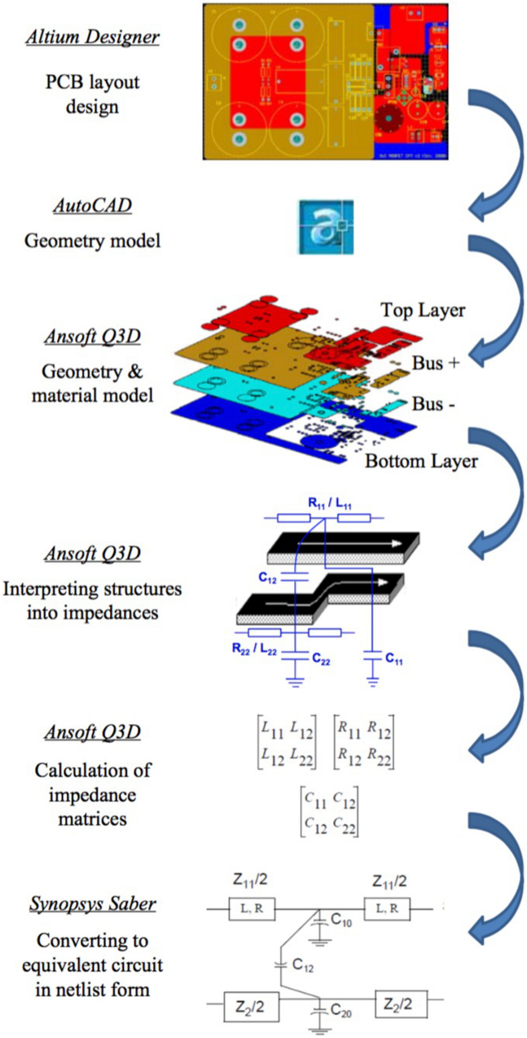


Figure 4.35 – PCB modeling procedure [46].

power switch and the power loop is located between the phase-leg and the decoupling capacitors.

As shown in Figure 4.36, the gate parasitic inductance is optimized by sizing the diameter of each via, the geometry of the gate driver pads as well as the

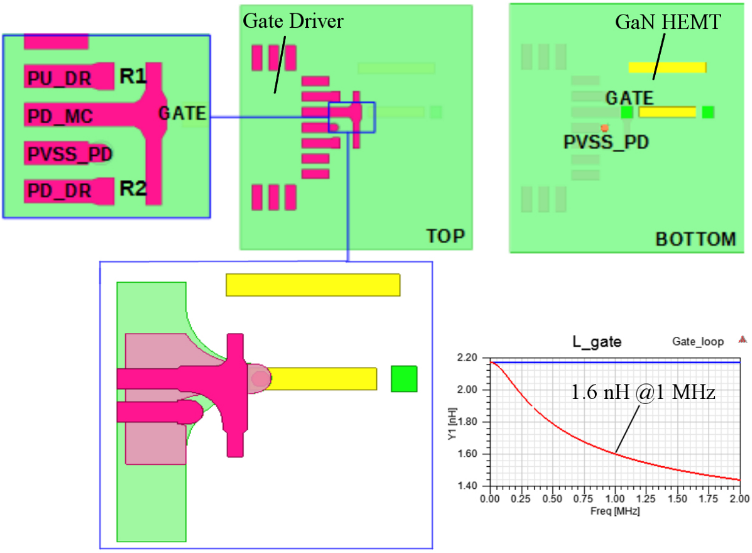


Figure 4.36 – PCB geometrical gate parasitic inductance optimization procedure.

thickness of each layer. The result shows a small gate inductance value of 1.58 nH, requested for fast switching capability.

4.4.2 SPICE Module Simulation

In order to start with a well known design, a SPICE model of the *GaN Systems* evaluation board GS66508T-EVBHB 650 V is realized. The different elements are modeled according to the detailed models. The circuit includes the *GaN Systems* transistors from the modified model in Section 1.4 and their respective package parasitics, the gate drive IC model, the PCB layout model, as well as passive component models. The coupling between the PCB board and the heat sink is also modeled.
A first step is made with the extraction of the PCB board parasitics with the design of a 3D model as shown in Figure 4.37.

The different layers and footprints are reproduced according to the real one and after extraction of the parasitics, the matrix is imported in LTspice as a sub-circuit model as shown in Figure 4.38.

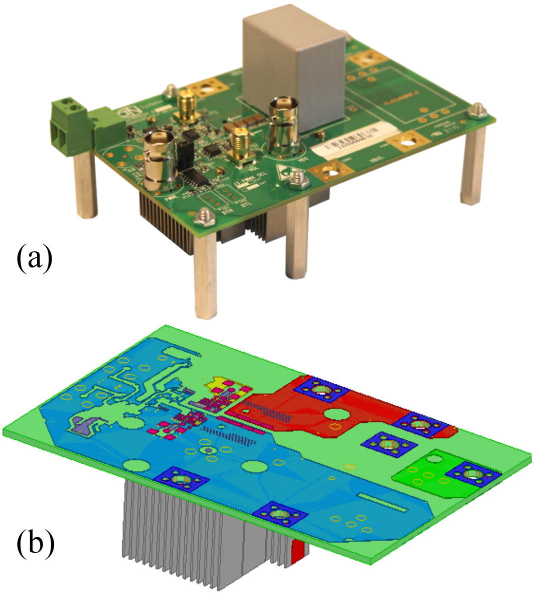


Figure 4.37 – PCB parasitics extraction. (a) GS66508T-EVBH evaluation board; (b) the Q3D evaluation board model.

The simulation analyses are in preliminary level, and the results shown in Figure 4.39 do not allow to draw any conclusions. However, the gate and drain voltage waveforms showed a good fitting between experiment and simulation.

High-Temperature GaN Phase-leg Board The objective is to design a 650 V, 30 A phase-leg prototype that summarizes the different works in this dissertation. The PCB board under design is shown in Figure 4.40. The power switches are two GaN System top-cooled 650 V, 60 A GaN HEMT, associated to two gate drivers (XREL XTR26020) chosen for their good capability at high-temperature. The isolation in ensured with coreless transformers for the control signals and by the PCB embedded transformer power supply for the gate driver.
The global dV/dt immunity is limited by the corless transformer isolation system at 65 $kV/\mu s$. The volume of one phase PCB board is 88 x 39 x 6 mm, in comparison, the first phase-leg prototype designed for the MEGaN project shows in appendix .6 without the gate driver power supply as well as no power switches had a volume of 60 x 39 x 4 mm.

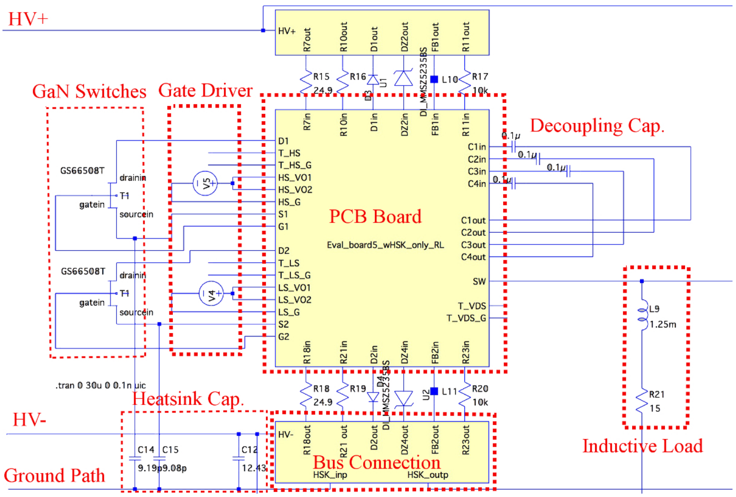


Figure 4.38 – Ltspice schematic of the PCB board with the extracted PCB board parasitics.

The 3 boards related to the 3 PCB boards will be plugged into a motherboard with the bulk capacitor. This assembly without connectors allows less parasitic elements as shown in Figure 4.41.

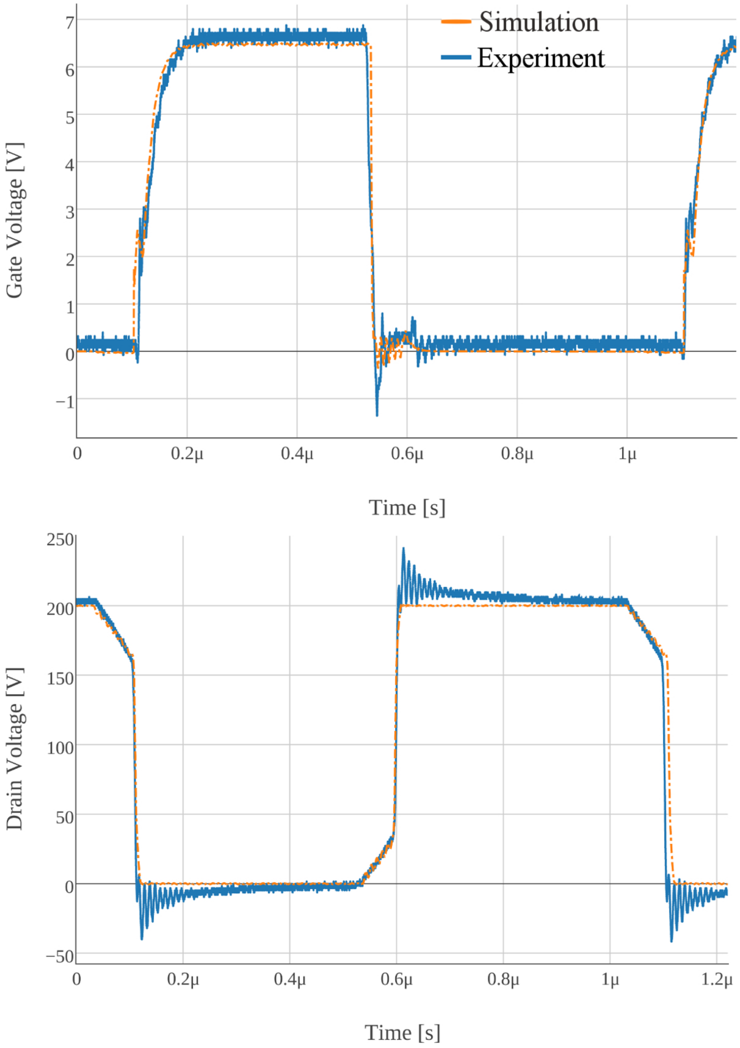


Figure 4.39 – Evaluation board experimental and simulated gate and drain voltage waveforms from the low-side switch at 200 V, 1 A.

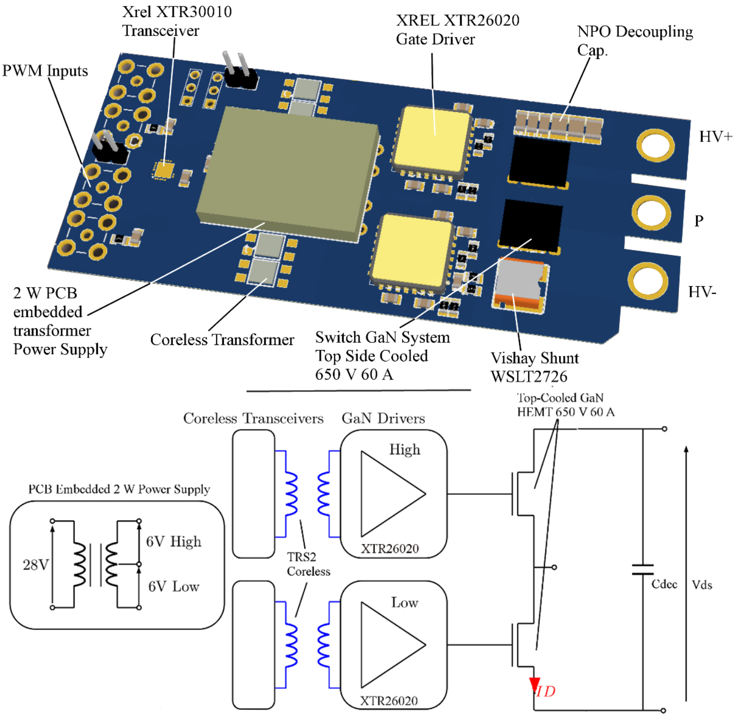


Figure 4.40 – 3D view of the 600 V high-temperature phase-leg prototype with its simplified schematic.

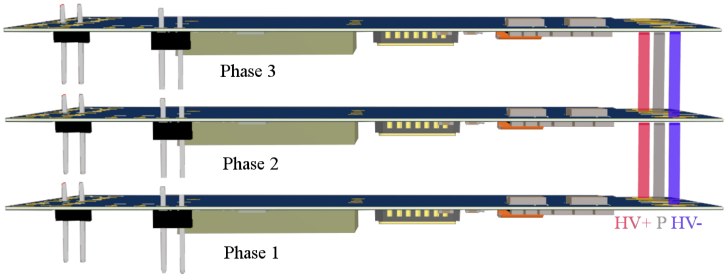


Figure 4.41 – 3D View of the 3 phases assembly.

4.5 Conclusion

The current sensor was identified as a key point in the ower module to increase the integration. A solution based on a TMR was proposed and characterized on the full temperature range. The current sensor was successfully implemented in a phase leg as a current protection.
In order to address faster switching time for lower losses in GaN devices, a four-level gate driver was proposed and designed for a phase leg. The solution presents a maximum improvement of 30 % for the switching losses, with a low complexity gate driver circuit.
In order to perform optimized layout of the GaN phase-leg, a PCB parasitic extraction matrix is implemented in a SPICE simulation model. The final high-temperature GaN phase-leg PCB board design is shown.

Chapter 5

General Conclusion

This work studied the impact of fast-switching in an inverter system and proposed solutions in order to deal with them. Characterization methods and procedures have been introduced for GaN HEMT devices at 200°C ambient temperature. The effect of temperature on the GaN HEMT structure has been discussed.
Based on characterization results device models have also been tuned.
A study about coreless transformers as a high-temperature control signal isolation barrier has been realized. Parylene coating showed good results in long-term temperature aging. Experimental characterization of the dynamic isolation of coreless-based solutions has been performed with a dV/dt generator.
A lamination process for high-temperature embedded PCB transformer with commercial magnetic ferrite was implemented for a gate driver power supply with ultra-low isolation capacitance. A transformer adapted resonant topology design was detailed as well as a SOI CMOS chip. The assembly of the SOI CMOS die plus the PCB embedded transformer gave an optimized volume solution as a low-power and high-isolation POL converter.
Finally, the gate driver itself was studied with the power module as a target. Solution for current sensor integration was proposed with magnetoresistance components. Full-temperature range characterization of the sensing solution has been performed and a compensation model was given.
Based on the GaN HEMT characterization in Chapter 1, a four-level gate driver was proposed in order to offer a trade-off between fast-switching and low switching losses dedicated for WBG power devices.

5.1 Summary of contributions

The proposed prototypes in this work address some key issues in the perspective of an integrated inverter system. Main contributions are the followings:

- The characterization at high temperature of commercially available GaN devices. Both cascode and enhancement GaN devices were tested in the full temperature range. The DPT method was used for this characterization and modeled in Chapter 1. Despite simple models, the experimental results proved agreement with simulations.

- The coreless transformer was identified as a good candidate for the control signal isolation in a high-temperature system with a top Parylene coating for reliability issues.
- The choice of converter topology compatible with low isolation capacitance transformer and high-switching frequency. The full design of a resonant converter was given and tested.
- An innovative lamination process for the integration of a magnetic material for a transformer into the PCB. The results showed an improvement of the global converter volume and the absence of degradation against temperature cycling test were observed so far.
- An original and simple solution for a dV/dt generator. The dV/dt generator allowed a characterization of the different isolation solutions with a simple setup.
- In order to address the fast-switching capability offered by GaN devices, a four-level gate driver was proposed. The solution showed good performance with faster transient up to 30 % and lower switching losses.
- An untested inverter solution was proposed with a PCB parasitic extraction for module layout optimization.

This strategy was to address high-frequency switching transients in an inverter system with a global approach. The global view allowed an optimization of the whole system and not only of one specific part, in order to take into count the interaction between each element.
However, the drawback of this approach, was to give many perspectives with each solution proposed without giving a complete development for each one.

5.2 Perspectives

The access to GaN devices from the CEA-Leti has limited this study for the development of a high-power GaN module prototype, and forced the development of the final inverter prototype at the end of this PhD. The GaN power devices are in a development time step but the improvement of the intrinsic characteristics are fast and proposed new challenges for each new available products. That is why this work may not be qualified as definitive and future works may be foreseen to address short-term issues. Based on the expectations of these near-future activities, the technological advances proposed in this work can be projected further in short-term and long-term activities.

5.2.1 Short-term Challenges

EMI Testing EMI issue is one of the main challenge reported for the WBG devices due to their fast-switching capability. Increasing the switching-frequency is coming with more EMI in the system [79, 32, 138].
The gate driver power supply is using soft-switching topology in order to have low-EMI level compared to a hard-switching topology. However, a characterization has to quantify this point as well as for the full inverter system.

High-temperature Testing of the Four-level Gate Driver A new test setup is needed to see the influence of temperature on the switching-speed of the GaN device under different gate voltage levels. The temperature influence would call for a compensation to be integrated in the control board to balance the effects.

GaN Reverse Conduction and Dynamic On-Resistance Modeling As shown in Chapter 1 modeling of the reverse conduction also called GaN "body-diode" is a key to perform a good accuracy for the loss prediction. However, this behavior in the GaN device structure is really different from the one of a MOSFET body-diode and requests a dedicated model [73]. Also the dynamic on-resistance effect is barely addressed in the current proposed models because difficult to quantify, however it has a large impact on the switching losses. The classical MOSFET spice model mostly implemented provides primary satisfying results regarding GaN device modeling, but does not include an accurate prediction for reverse-conduction losses and dynamic On-resistance.

5.2.2 Long-term Challenges

dV/dt control based on the four-level gate driver As demonstrated in Section 4.4 the applied peak gate voltage level has an influence on the switching speed. A control of the dV/dt can be implemented based on this idea. dV/dt control is directly related to the EMI impact of fast-switching device. In order to reduce the EMI footprint, dV/dt control is an efficient solution by adapting the switching speed as function of the load current.

SOI development of a GaN dedicated Gate Driver One major challenge to drive GaN power switch is to reduce the gate parasitics loop. The gate driver has to be placed as close as possible to the transistor. However high-temperature application for GaN device has to be addressed with high-temperature gate driver capability.
An SOI CMOS chip is a good candidate as demonstrated in Section 3.5. GaN-integrated gate drivers are now demonstrated in literature but the commercial offer (and the cost) will be delayed. So SOI CMOS is a competitive solution to address this issue. Moreover the integration of the gate driver allows to implement health-monitoring functions close to the power device as well as multi-level gate voltages. Based on the Texas Instrument product [134], it is possible to imagine a high-temperature GaN phase-leg for harsh environment application with intelligent functions integrated in the PCB package.

Advanced PCB embedded Power Module The 3D assembly approach discussed in this work for the gate driver power supply provides a nice framework to embed any additional passive components at a limited penalty in term of footprint, and still with a very acceptable reliability.

Appendices

.1 GaN HEMT GS66508 Modified Model

```
* Created in LTspice Version 4.13h                    *
*                                                      *
* GaN Systems Inc. Power Transistors                   *
* LTSpice Library for GaN Transistors                  *
* Version 1.27                            *
*                                    *
****************************************************************
*
****************************************************************
*
*                                    *
* Models provided by GaN Systems Inc. are not warranted by      *
* GaN Systems Inc. as                              *
* fully representing all of the specifications and operating    *
* characteristics of the semiconductor product to which the     *
* model relates. The model describe the characteristics of a    *
* typical device.                           *
* In all cases, the current data sheet information for a given  *
* device is the final design guideline and the only actual      *
* performance specification.                        *
* Altough models can be a useful tool in evaluating device      *
*  performance,  they  cannot  model  exact  device  performance
under *
* all conditions, nor are they intended to replace bread-       *
* boarding for final verification. GaN Systems Inc. therefore   *
* does not assume any liability arising from their use.         *
* GaN Systems Inc. reserves the right to change models without
*
* prior notice.                              *
*                                    *
* This library contains models of the following GaN Systems     *
* Inc. transistors:                          *
*                                    *
*   GS66508P    EO4 and EO5                         *
****************************************************************
*
*$
.subckt GS66508P gatein drainin sourcein source_S T1
*
.param conv_aide=1
.param Rth_CasetoAmbient=0
*
.param  aDi=0.25              cur={(1.3/3.6)*(0.069*75/80)*295/1}
slp=2.0   rpara=0.88
+     ITc=0.003           rTc=-0.0128                       x0_0=0.31
                    x0_1=0.255
+     di_gs1={7*4.3e-5}  di_gs2={2.6e-8}          di_gs3={100*0.8}
di_gs4={80*0.23}
```

```
+     Igs1=1.42e-10     Igs2={(3.0e-010)*(5.7)/20}      Igs3=4.9
Igs4=6.83e-01
+     Igs5=-7.85e-011    Igs6=-3.30                  Igs7=6.0
+     Igd1=5.49e-012              Igd2={2.6e-11*(7.5)/3}      Igd3=-
3.09       Igd4=12
+     Isd1=1.7e-013     Isd2=1e-12             Isd3=0           Isd4=2.5
+     Isd5=5e-013       Isd6=10                Isd7=4.5         of1=100
          of2=35
+          ff1=0.345                 ff2=1.2                         ff3=4.5
           ff4=0.5          ff5=8    ff6=0.14
*
Rth T0 T1 {(0.35*3.6)*(15/75*80*(1+0.005*(Temp-27)))/295}
Cth 0 T1 {(1/3.6)*(2.4e-5*75/80)*295}
Rth_pkg_brd T0 0 {0.43+Rth_CasetoAmbient}
Cth_pkg T0 0 {5e-3}
*
*
bdtemp 0 T1 I = (if(v(drain,source)>0,
+                                           (cur*(1-ITc*(V(T1)-0+Temp-
25))*log(1.0+exp(21*(v(gate,source)-7.9+6.1-0.000*(Temp-
25))/slp))*
+         v(drain,source)/(1                                            +
max(x0_0+x0_1*(v(gate,source)+9.1),0.2)*v(drain,source)))*
+         v(drainin,sourcein),
+         (cur*(1-ITc*(v(T1)-0+Temp-
25))*log(1.0+exp(21*(v(gate,drain)-7.9+6.1-0.000*(Temp-
25))/slp))*
+         v(source,drain)/(1                                            +
max(x0_0+x0_1*(v(gate,drain)+9.1),0.2)*1.0*v(source,drain)))*
+         v(sourcein,drainin)))
*
*Note: Internal inductors can be disabled by uncommenting the
following 4 lines and
*commenting out the next 8 lines.
*
*rd     drainin     drain     {(3.6/4)*(0.95*rpara*(1-0*rTC*(Temp-
25)))*18.2/295} tc=0.0128
*rs    sourcein    source    {(1*3.6)*(0.238*rpara*(1-0*rTc*(Temp-
25)))/295} tc=0.0128
*RSS source_S sourcein 0.0001
*rg gatein gate {0}
*
rd      drain3      drain      {(3.6/4)*(0.95*rpara*(1-0*rTC*(Temp-
25)))*18.2/295} tc=0.0135
ld drainin drain3 {2.0e-10} Rser=0
rs     source3     source     {(1*3.6)*(0.238*rpara*(1-0*rTc*(Temp-
25)))/295} tc=0.0135
Ls sourcein source3 {2.0e-10} Rser=0
LSS source_S source_S1 {1e-9} Rser=0
```

```
RSS source_S1 source3 {0.0001}
rg gatein gate1 {1.5}
Lg gate1 gate {1e-9} Rser=0
*
Rcsdconv drain source {1000Meg/aDi}
Rcgsconv gate source {1000Meg/aDi}
Rcgdconv gate drain {1000Meg/aDi}
*
bswitch drain2 source2 I = (if (v(drain2,source2)>0,
+       (cur*(1-ITc*(v(T1)-0+Temp-
25))*log(1.0+exp(21*(v(gate,source2)-7.9+6.1-0.00*(Temp-
25))/slp))*
+       v(drain2,source2)/(1                              +
max(x0_0+x0_1*(v(gate,source2)+9.1),0.2)*v(drain2,source2))),
+       (-cur*(1-ITc*(v(T1)-0+Temp-
25))*log(1.0+exp(21*(v(gate,drain2)-7.9+6.1-0.00*(Temp-
25))/slp))*
+       v(source2,drain2)/(1                              +
max(x0_0+x0_1*(v(gate,drain2)+9.1),0.2)*1.0*v(source2,drain2)
))) )
R_drain2 drain2 drain {(1e-4)}
R_source2 source2 source {(1e-4)}
*
**
bgsdiode1 gate source1 I = (if( v(gate,source)>100,
+
        (0.2*(1*conv_aide*10.5*aDi/1077*(di_gs1*(exp(16*(100.
0)/di_gs3)-1)+di_gs2*(exp(16*
+       (100.0)/di_gs4)-1)))*(1+0.005*(Temp-
27))*(1/3.6*295))*(1+0.09*exp(0.051*(Temp-27))),
+
        (0.2*(1*conv_aide*10.5*aDi/1077*(di_gs1*(exp(16*(v(ga
te,source1))/di_gs3)-1)+di_gs2*
+       (exp(16*(v(gate,source1))/di_gs4)-1)))*(1+0.005*(Temp-
27)))*(1/3.6*295))*(1+0.09*exp(0.051*(Temp-27))))
R_source1 source1 source {(14.47/380)}
*
**
bgddiode1 gate drain1 I = (if( v(gate,drain)>25,
+
        (conv_aide*4*(0.5*aDi/1077*(di_gs1*(exp(0.3*(25.0)/di_
gs3)-1)+di_gs2*(exp(0.3*
+       (25.0)/di_gs4)-1)))*(1+0.005*(Temp-
27))*(0.2/3.6*295)),
+
        (conv_aide*4*(0.5*aDi/1077*((di_gs1*1)*(exp(0.3*(v(gat
e,drain1))/(di_gs3*1))-1)
+       +(di_gs2*(1))*(exp(0.3*(v(gate,drain1))/(di_gs4*1))-
1)))*(1+0.005*(Temp-27))*(0.2/3.6*295))))
```

```
R_drain1 drain1 drain {14.47/380}
*
bdsdiode1 drain1 source1 I = (if( v(drain1,source1)>850,
+         (0.4e-
9*conv_aide*200*(0.5*aDi/1077*(di_gs1*(exp(5*(850.0-
630+((Temp-25)/1.75))/di_gs3)-1)+1*di_gs2*(exp(5*
+         (850.0-630+((Temp-25)/1.75))/di_gs4)-
1)))*(1+0.1*(Temp-27))*(0.2/3.6*295)),
+         (0.4e-
9*conv_aide*200*(0.5*aDi/1077*((di_gs1*1)*(exp(5*(v(drain1,s
ource1)-630+((Temp-25)/1.75))/(di_gs3*1))-1)
+         +1*(di_gs2*(1))*(exp(5*(v(drain1,source1)-630+((Temp-
25)/1.75))/(di_gs4*1))-1)))*(1+0.1*(Temp-
27))*(0.2/3.6*295))))
*
bdsdiode2 drain1 source1 I = (if( v(drain1,source1)>750,
+         (0.1e-
3*conv_aide*200*(0.5*aDi/1077*(di_gs1*(exp(0.5*(750.0-
670)/di_gs3))))
+         *(1+0.06*exp(0.1*(Temp-27)))*(0.2/3.6*295)),
+         (0.1e-
3*conv_aide*200*(0.5*aDi/1077*((di_gs1)*(exp(0.5*(v(drain,so
urce)-670)/(di_gs3)))))
+         *(1+0.09*exp(0.1*(Temp-27)))*(0.2/3.6*295))))
*
bgddiode2 gate drain1 I = (if( v(gate,drain1)>30,
+         (conv_aide*1e-12*((0.1*di_gs1*(exp(3*(30-
4)/1))+di_gs2*
+         (exp(3*(30-4)/1))))*(1+0.005*(Temp-25)))*(1/3.6*295),
+         (conv_aide*1e-12*((0.1*di_gs1*(exp(3*(v(gate,drain1)-
4)/1))+di_gs2*
+         (exp(3*(v(gate,drain1)-4)/1))))*(1+0.005*(Temp-
25)))*(1/3.6*295)))
****
*
C_GS    gate source   {(1.25/7*Igs1/120/2.18)*3.5*295+65e-12}
C_GS1        gate        source        Q        =
((1/7*10/120/2.18*1.5)*295*1.5*((0.5*Igs2*Igs4*log(1+exp(ff5
*0.5*(v(gate,source)-Igs3+
+                               4.6)/0.9933))-
Igs5*Igs7*log(1+exp(ff6*(v(source,drain)-Igs6)/Igs7)))))
*
C_GD   gate drain      {(0.8/17*Igd1/30/2.18)*1.5*295}
C_GD1          gate          drain          Q          =
((0.7/7*1/25/2.18*0.8)*295*((0.5*Igs2*Igs4*log(1+exp(ff1*6*(
v(gate,drain)-Igs3+of1-50)/
+
         (Igs4*ff3)))+Igd2*Igd4*log(1+exp(0.5*ff2*(v(gate,drain)-
Igd3+of2-30)/(Igd4
```

```
+                                       *ff4))))))
*
C_SD    source drain          {(2/7*Isd1/2.18)*10*295}
C_SD1            source            drain            Q            =
(1/7*1/2.18*18*295*(4*Isd2*Isd4*log(1+exp(0.1*(v(source,dra
in)-Isd3+145)/Isd4))+
+                        Isd5*Isd7*log(1+exp(1.5*(v(source,drain)-
Isd6+55)/Isd7))
+                                                   +5.7*0.0*(0.5*2.5e-
12*0.643*log(1+exp(v(source,drain)-4.68+80))/(0.643
+                                       *3.5))))
.ends
*$
```

.2 Coreless Isolation Capacitance Matlab Code

Extracted data from impedancemeter in mode R-X

```
function [y]=verif_Zcc()
syms Ceq;

% Variables modèle magnétique
m=0.923;
Lf=1.4250e-7;
Lm=9.66e-7;
Rs=47.75;
Rp=46.65;
%Variables modèle capacitif
R=92.1;
X=18;

Zmes=sqrt(R\textsuperscript{2}+X\textsuperscript{2});

Req=Rp+(Rs/m\textsuperscript{2});
w=2*pi*25.2*10e6;
Z1=Req+1i*Lf*w;
Z2=1i*Lm*w;
Z12=(Z2*Z1)/(Z1+Z2);
Z3=-1i/(Ceq*w);
Z123=(Z12*Z3)/(Z12+Z3);
x=solve(Zmes==abs(Z123),Ceq);
y=double(abs(x));
end
```

.3 XTR39020 SOI CMOS Chip Layout

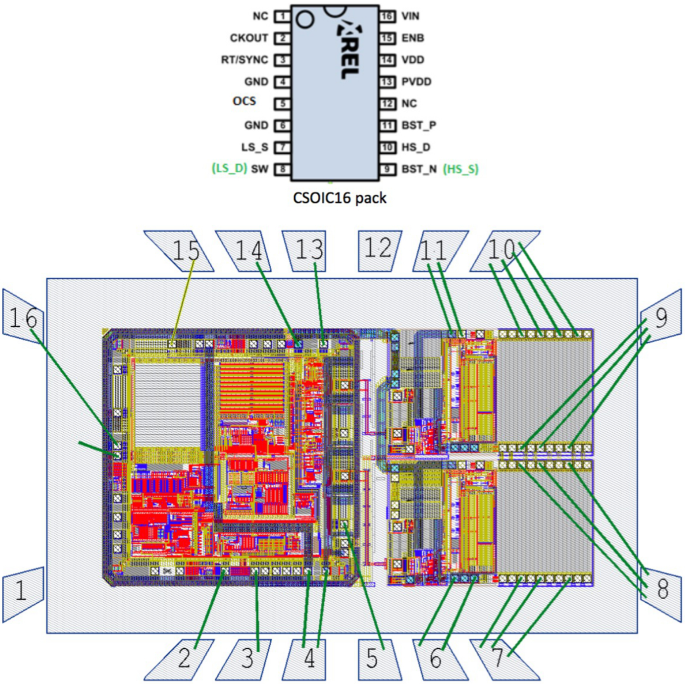
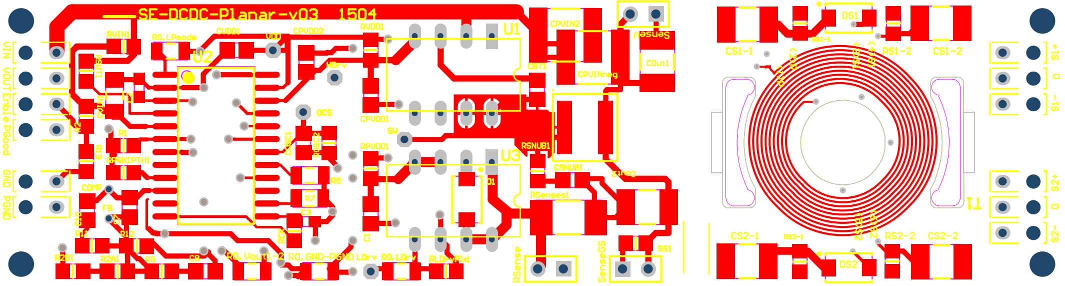


Figure 1 – XTR39020 SOI CMOS Chip Layout.

.4 Isolated Buck Converter Layout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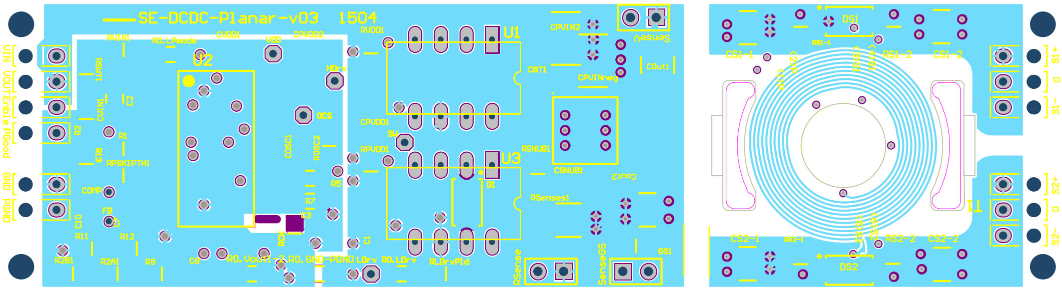
VIN
VOUT
Enable
PGood
GND
PGND
U1
U2
U3
T1
COut1
Sense
RSense
SenseGS
DS1
DS2
CS1-1
CS1-2
RS1-2
CS2-1
CS2-2
RS2-2
S1+
0
S1-
S2+
0
S2-
CPVIN2
CPVINneg
CBT1
RSNUB1
CSNUB1
RSense1
CVDD1
CPVDD2
RVDD1
CPVDD1
RPVDD1
HDrv
OCS
SW
D1
COMP
FB
LDrv
RLDrvHld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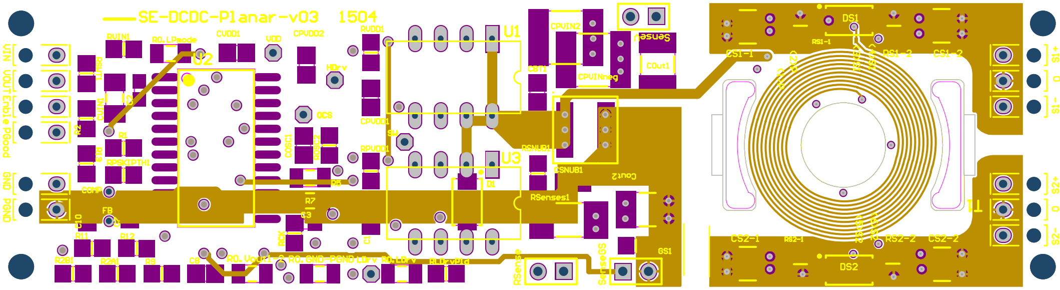
R0.LPmode
CVDD1
VDD
CPVDD2
RVDD1
U1
U2
U3
RSWT1
CVIN1
C2
R2
R1
R13
RPSKIPTH1
COMP
FB
C7
C10
R11
R12
R2B1
R2A1
R9
C8
R0.Vout1-2
R0.GND-PGND
LDrv
R0.LDrv
RLDrvPld
RCK
C3
R7
R5
C1
COSC1
ROSC2
OCS
HDrv
CPVDD1
SW
RPVDD1
D1
CPVIN2
CBT1
CPVINneg
SenseV
COut1
RSNUB1
CSNUB1
Cout2
RSenses1
RSense
SenseGS
GS1
VIN
VOUT
Enble
PGood
GND
PGND
DS1
DS2
RS1-1
RS1-2
CS1-1
CS1-2
RS2-1
RS2-2
CS2-1
CS2-2
(1)P
(2)P
(3)S1
(4)S1
(5)S2
(6)S2
T1
S1+
0
S1-
S2+
0
S2-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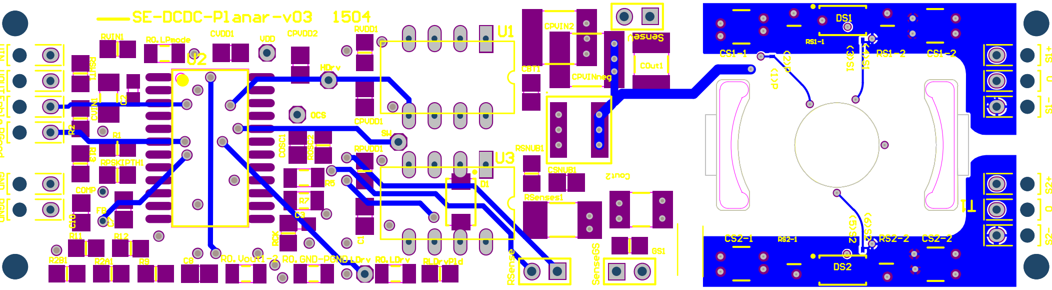
VOUT
Enable
PGood
GND
PGND
RVIN1
R0_LPmode
CVDD1
VDD
CPVDD2
RVDD1
U1
CPVIN2
Sense
COut1
U2
HDrv
OCS
CPVDD1
SW
RPVDD1
U3
CBT1
CPVINneg
RSNUB1
CSNUB1
RSenses1
Cout2
GS1
RSense
SenseGS
D1
R7
C3
R8
COMP
FB
RPSKIPTH1
R11
R12
R2B1
R2A1
R9
C8
R1
DS1
DS2
CS1-1
CS1-2
RS1-1
RS1-2
CS2-1
CS2-2
RS2-1
RS2-2
T1
S1+
0
S1-
S2+
0
S2-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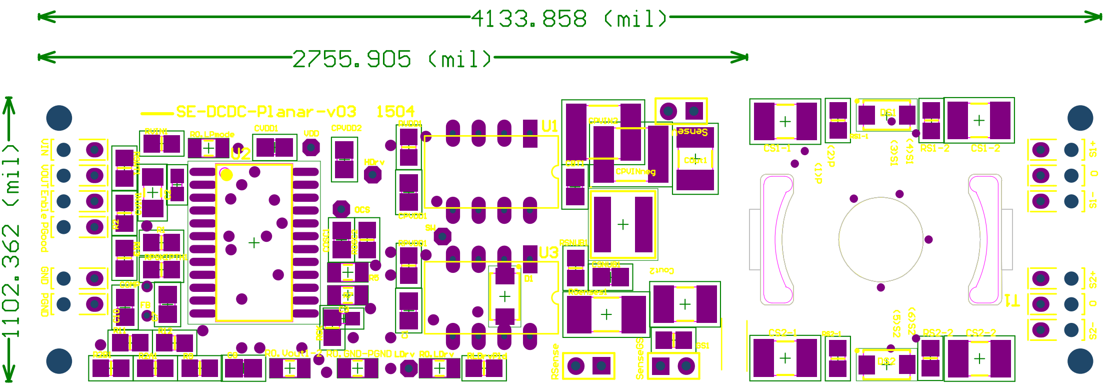
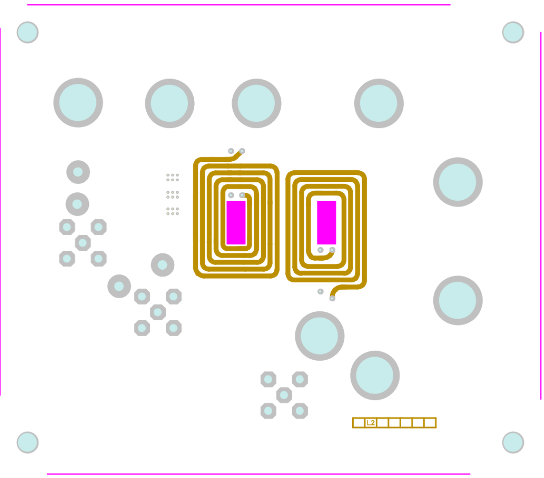
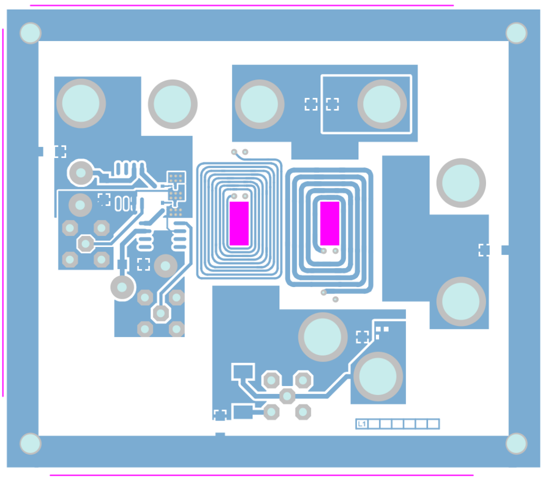
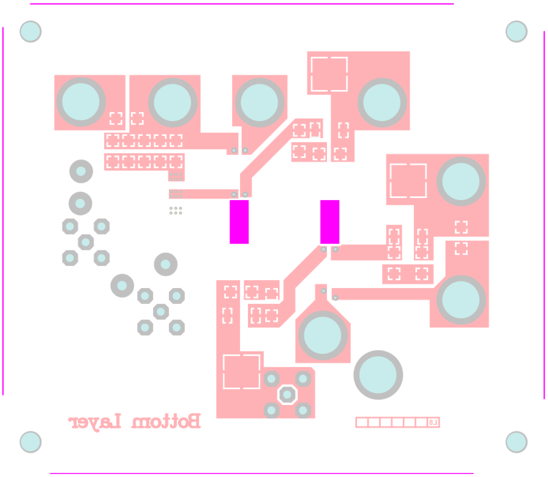
U2
U3
T1
DS1
DS2
VIN
VOUT
Enable
PGood
GND
PGND
S1+
0
S1-
S2+
0
S2-
CS1-1
CS1-2
CS2-1
CS2-2
RS1-1
RS1-2
RS2-1
RS2-2
Sense
SenseGS
RSense
COut1
COut2
CPVIN2
CPVINneg
CBT1
RSNUB1
CSNUB1
RSense1
HDrv
OCS
SW
VDD
CVDD1
CPVDD2
RVDD1
CPVDD1
RPVDD1
RVIN1
R0.LPmode
COMP
FB
RPSKIPTH1
R11
R12
R2B1
R2A1
R9
C8
R0.Vout1-2
R0.GND-PGND
LDrv
R0.LDrv
RLDrvPld
D1
R6
R7
C3
C1
GS1


4133.858 (mil)
2755.905 (mil)
1102.362 (mil)
SE-DCDC-Planar-v03 1504
U1
U2
U3
T1
VIN
VOUT
Enable
PGood
GND
PGND
Sense
RSense
SenseGS
CPVINreg
Cout2
CS1-1
CS1-2
RS1-2
CS2-1
CS2-2
RS2-2
S1+
0
S1-
S2+
0
S2-

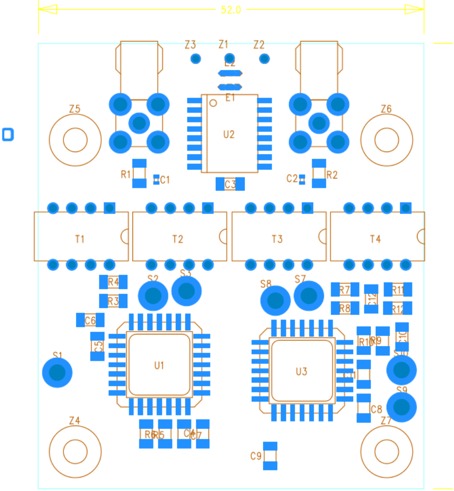
.5 800 kHz GaN Active Clamp Flyback Layout


L2


L1


Bottom Layer

.6 MEGaN Gate Driver Layout


52.0
Z3
Z1
Z2
E2
E1
U2
Z5
Z6
R1
C1
C3
C2
R2
T1
T2
T3
T4
R4
R3
S2
S3
S8
S7
R7
R8
R11
R12
C6
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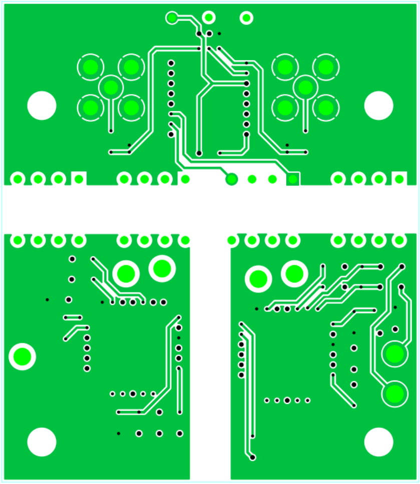
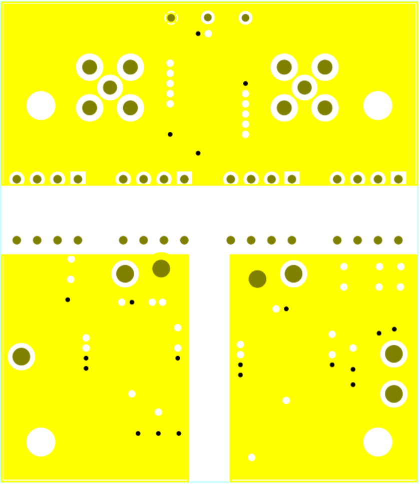
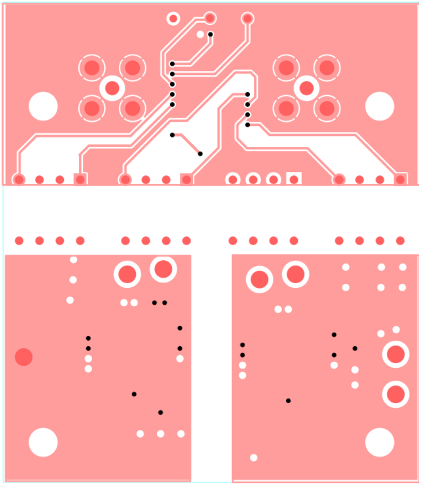
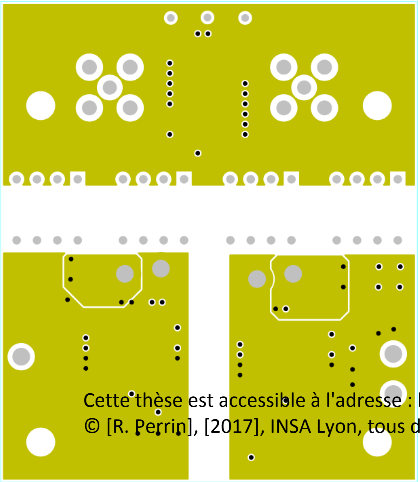
R6
R5
C4
C7
C9









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FOLIO ADMINISTRATIF

THESE DE L'UNIVERSITE DE LYON OPEREE AU SEIN DE L'INSA LYON

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Prénoms : Rémi

TITRE : Characterization and Design of High-Switching speed Capability of GaN Power Devices in a 3-Phase Inverter

NATURE : Doctorat Numéro d'ordre : 2017LYSEI**001**

Ecole doctorale : EEA 160

Spécialité : Génie Electrique

RESUME :

The french industrial project MEGaN targets the development of power module based on GaN HEMT transistors. One of the industrial applications is the aeronautics field with a high-constraint on the galvanic isolation (>100 kVµs) and ambient temperature (200°C). The intent of this work is the power module block (3 phases inverter 650 V 30 A). The goal is to obtain a small footprint module, 30 cm2, with necessary functions such as gate driver, gate driver power supply, bulk capacitor and current phase sensor. This goal implies high efficiency as well as respect of the constraint of galvanic isolation with an optimized volume.
This dissertation, besides the state of the art of power modules and especially the GaN HEMT ones, addressed a control signal isolation solution based on coreless transformers. Different prototypes based on coreless transformers were characterized and verified over 3000 hours in order to evaluate their robustness.
The different studies realized the characterization of the different market available GaN HEMTs in order to mature a circuit simulation model for various converter topologies. In the collaborative work of the project, our contribution did not focus on the gate driver chip design even if experimental evaluation work was made, but a gate driver power supply strategy.
The first gate driver isolated power supply design proposition focused on the low-voltage GaN HEMT conversion. The active-clamp Flyback topology allows to have the best trade-off between the GaN transistors and the isolation constraint of the transformer. Different transformer topolgies were experimentally performed and a novel PCB embedded transformer process was proposed with high-temperature capability. A lamination process was proposed for its cost-efficiency and for the reliability of the prototype (1000 H cycling test between - 55; + 200°C), with 88 % intrinsic efficiency. However, the transformer isolation capacitance was drastically reduced compared to the previous prototypes.
2 high-integrated gate driver power supply prototypes were designed with: GaN transistors (2.4 MHz, 2 W, 74 %, 6 cm2), and with a CMOS SOI dedicated chip (1.2 MHz, 2 W, 77 %, 8.5 cm2).
In the last chapter, this dissertation presents an easily integrated solution for a phase current sensor based on the magnetoresistance component. The comparison between shunt resistor and magnetoresistance is experimentally performed. Finally, two inverter prototypes are presented, with one multi-level gate driver dedicated for GaN HEMT showing small switching loss performance.

MOTS-CLÉS :
GaN HEMT, gate driver, embedded transformer, coreless transformer, harsh environment, current sensor

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