Detailed Investigation of Band Modulation Devices in 14 nm and 28 nm FDSOI Technologies

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To my parents and my brother …

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Contents

Abbreviations

Acronym	Nomination
1T-Bulk	**S**ingle **T**ransistor **Bulk**
1T-DRAM	**S**ingle **T**ransistor **DRAM**
1T-PDSOI	**S**ingle **T**ransistor **PDSOI**
1T-1C DRAM	**O**ne **T**ransistor **O**ne **C**apacitor **DRAM**
3D	**T**hree **D**imensional
3T	**T**hree **T**erminals
4T-SRAM	**F**our **T**ransistors **SRAM**
AlTiN	**Al**uminium **Ti**tanium **N**itride
ALWG	**A**rbitrary **L**inear **W**aveform **G**eneration
Al_2O_3	**Al**uminium **O**xide
ARAM	**A**dvanced **RAM**
A^2RAM	**A**dvanced **2 RAM**
B2B	**B**and **2 B**and
BBC-T	**B**ack **B**iased **C**ontrolled **T**hyristor
BeST	**B**BC-T **e**nhanced **ST**acked SCR
BET-FET	**B**ipolar-**E**nhanced **TFET**
BL	**B**it **L**ine
BTBT	**B**and **T**o **B**and **T**unneling
BOX	**B**uried **OX**ide
CC	**C**apacitive **C**oupling
CC-TLP	**C**apacitively **C**oupled **TLP**
CDM	**C**harge **D**evice **M**odel
CMOS	**C**omplementary **MOS**
D	**D**rain
DIBL	**D**rain-**I**nduced **B**arrier **L**owering
DRAM	**D**ynamic **R**andom **A**ccess **M**emory
DUT	**D**evice **U**nder **T**est
EHB-TFET	**E**lectron-**H**ole **B**ilayer **TFET**
eDRAM	**E**mbedded **DRAM**
ESD	**E**lectro-**S**tatic **D**ischarge
FBE	**F**loating **B**ody **E**ffects
FBJ	**F**orward **B**iased **J**unction
FDSOI	**F**ully **D**epleted **S**ilicon-**O**n-**I**nsulator
Fe-FET	**F**erroelectric **FET**
FED	**F**ield **E**ffect **D**iode
FET	**F**ield **E**ffect **T**ransistor
FN	**F**owler-**N**ordheim
G_b	**B**ack **G**ate
Ge	**Ge**rmanium
G_f	**F**ront **G**ate
GIDL	**G**ate-**I**nduced **D**rain **L**eakage

GP	**G**round **P**lane
GP-N	**N**-type **G**round **P**lane
GP-P	**P**-type **G**round **P**lane
GO1	**Thin G**ate **O**xide
GO2	**Thick G**ate **O**xide
GR	**G**eneration **R**ecombination
H_0	**H**old "**0**" operation
HBM	**H**uman **B**ody **M**odel
HfO_2	**Haf**nium **dio**xide
HKMG	**H**igh-**K M**etal **G**ate
H_{R0}	**H**old "**R0**"
HSG	**H**emi **S**pherical **G**rain
HV-ESD	**H**igh **V**oltage **ESD**
H_{W0}	**H**old "**W0**"
H_{W1}	**H**old "**W1**"
I/O	**I**nput/**O**utput
IC	**I**ntegrated **C**ircuit
IL	**I**nterface **L**ayer
IMOS	**I**mpact Ionization **MOS**
ITRS	**I**nternational **T**echnology **R**oadmap for **S**emiconductors
JEDEC78	**J**oint **E**lectron **D**evice **E**ngineering **C**ouncil
LDD	**L**ightly **D**oped **D**rain
LU	**L**atch **U**P
M_1	**First** level of **M**etal
M_2	**Second** level of **M**etal
MDC	**M**ulti **D**ual **C**ell
MM	**M**achine **M**odel
MOS	**M**etal **O**xide **S**emiconductor
MOSFET	**MOS F**ield **E**ffect **T**ransistor
MOX	**M**iddle **OX**ide
MRAM	**M**agnetic **RAM**
MSD	**M**eta **S**table **D**ip
MSDRAM	**M**eta **S**table **D**ip **R**andom **A**ccess **M**emory
NEMS	**N**ano-**E**lectro **M**echanical **S**ystem
nMOS	**n**-type **MOS**
NVM	**N**on **V**olatile **M**emories
NW	**N W**ell
ONO	**O**xide-**N**itride-**O**xynitride
P/E	**P**rogram/**E**rase
PCRAM	**P**hase **C**hange **RAM**
PD	**P**artially **D**epleted
PDSOI	**P**artially **D**epleted **S**ilicon-**O**n-**I**nsulator
PG	**P**ulse **G**enerator
PMOS	**P** type **MOS**
PW	**P W**ell
RAM	**R**andom **A**ccess **M**emory
RCA	**R**emoval of metallic and organic **C**ontaminations with surface **A**ctivation
ReRAM	**Re**sistive **RAM**

R_0, R_1	**R**ead "**0**" and "**1**" states
RPO	**R**esist **P**rotection **O**xide
RSU	**R**emote-Sense and **S**witch **U**nit
S	**S**ource
SA	**S**ense **A**mplifier
SCE	**S**hort **C**hannel **E**ffects
SCR	**S**ilicon **C**ontrolled **R**ectifier
Si	**Si**licon
SiGe	**Si**licon **Ge**rmanium
Si/SiGe HBT	**Si/SiGe H**eterojunction **B**ipolar **T**ransistor
SIMOX	**S**eparation by **IM**planted **OX**ygen
SL	**S**elect **L**ine
SiO_2	**Si**licon **Dio**xide
SOI	**S**ilicon-**O**n-**I**nsulator
SPICE	**S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis
SRAM	**S**tatic **RAM**
SRH	**S**hockley-**R**ead-**H**all
SS	**S**ubthreshold **S**lope
STI	**S**hallow **T**rench **I**solation
TCAD	Technology Computer-Aided Design
TDR	**T**ime **D**omain **R**eflectometry
TDRT	**T**ime **D**omain **R**eflectometry and **T**ransmission
TDT	**T**ime **D**omain **T**ransmission
TFET	**T**unnel **FET**
TiN	**Ti**tanium **N**itride
TLP	**T**ransmission **L**ine **P**ulse
ULP	**U**ltra-**L**ow **P**ower
URAM	**U**nified **RAM**
UTBB	**U**ltra-**T**hin **B**ody and **B**ox
UTSOI	Compact Model of MOSFET developed by CEA-Leti
VF-TLP	**V**ery **F**ast **TLP**
VLSI	**V**ery-**L**arge-**S**cale **I**ntegration
W_0	**W**rite "**0**"
W_1	**W**rite "**1**"
WGFMU	**W**aveform **G**enerator/**F**ast **M**easurement **U**nit
WL	**W**ord **L**ine
Z^2-FET	**Z**ero subthreshold slope and **Z**ero impact ionization **FET**
Z^2-FET SGP	**Z^2-FET S**ingle **G**round **P**lane
Z^2-FET DGP	**Z^2-FET D**ual **G**round **P**lane
Z^2-RAM	**Z^2**-FET **RAM**
Z^3-FET	**Z**ero SS, **Z**ero II and **Z**ero front-gate **FET**
ZeST	**Z^2**-FET **e**nhanced **ST**acked SCR

Symbols

Symbol	Description	Unit
$A_{Z^2\text{-FET}}$	Z^2-FET bit cell area	μm^2
C_b	Background capacitance	F
C_{box}	BOX capacitance	F
C_{ESD}	ESD capacitance	F
C_{inv}	Inversion capacitance	F
C_{ox}	Oxide capacitance	F
C_{Si}	Silicon film capacitance	F
C_{tot}	Total capacitance, $C_{inv} + C_{ox}$	F
D_{mm^2}	Integration density	mm^2
E_f, E_b	Electric field in gated/ungated parts of Z^2-FET	$V.cm^{-1}$
I_1, I_0	"1" and "0" states currents	A
I_A	Anode current	A
I_D	Drain current	A
I_{ESD}	ESD current	A
I_H	Holding current	A
I_{ON}, I_{OFF}	ON and OFF states currents	A
I_{R1}	Read "1" current	A
I_{t1}	Triggering current of ESD protection	A
I_{t2}	Second breakdown triggering current	A
I_{W1}	"1" writing current	A
L	Device length	nm
L_{ESD}	ESD inductance	H
L_G	Gate length	nm
L_{G1}, L_{G2}	FED first and second gate lengths	nm
L_{IN}	Intrinsic part length of Z^2-FET	nm
L_{int1}, L_{int2}	Intrinsic part lengths of BBC-T	nm
L_n	Gated part length of Z^2-FET	nm
L_p	Ungated part length of Z^2-FET	nm
$L_{n,\,p}$	Electron, holes diffusion lengths	nm
$L_{poly\text{-}contact}$	Distance between polysilicon and contact	nm
$L_{poly\text{-}RPO}$	Distance between polysilicon and RPO layer	nm
L_{RX}	Distance between two silicon active zones	nm
L_s	MOS selector gate length	nm
L_{source}	Source length	nm
N^+	N-type doping concentration	cm^{-3}
N_A, N_D	Concentration of ionized acceptors/donors	cm^{-3}
$N_{GP\text{-}P}$, $N_{A,GP\text{-}P}$	P-type ground plane concentration	cm^{-3}
N_{hk}	Fixed charge traps	cm^{-2}
n_i	Intrinsic carrier density	cm^{-3}
$N_{A,channel}$	Silicon channel doping concentration	cm^{-3}
P^+	P-type doping concentration	cm^{-3}

q	Electron charge	C
R_{6nm}	ON resistance of devices with t_{Si} = 6 nm	Ω/μm
R_{12nm}	ON resistance of devices with t_{Si} = 12 nm	Ω/μm
R_{ESD}	ESD resistance	Ω
R_{ON}	ON resistance	Ω/μm
RT	Rise time	s
t	Time	s
Δt	Time variation	s
T	Temperature	°C
ΔT	Temperature variation	°C
t_{BOX}	BOX thickness	nm
t_{epi}	Epitaxy layer thickness	nm
t_{ox}	Oxide thickness	nm
T_P	Programming time	s
t_{pulse}	Pulse duration	s
t_{PW}	Pulse width duration	s
t_{re}	Retention time	s
t_{Si}	Silicon thickness	nm
V_A	Anode voltage	v
$V_{A(W1)}$	Anode voltage for "1" writing	v
$V_{A(Reading)}$	Anode voltage for reading	v
V_B	Body potential	v
V_{BD}	Breakdown voltage	v
V_{bi}	Built in potential	v
V_{dd}	Supply voltage	v
V_{ddmax}	Max supply voltage	v
V_{DS}	Drain to source voltage	v
V_{DSAT}	Drain saturation voltage	v
V_{ESD}	ESD voltage	v
V_G	Gate voltage	v
V_{G1}, V_{G2}	First and second gate voltages in FED	v
V_{G1p}, V_{G1R}	Program and read voltages	v
V_{Gb}	Back-gate voltage	v
V_{GbN}	Ground plane N voltage	v
V_{GbP}	Ground plane P voltage	v
V_{Gf}	Front-gate voltage	v
ΔV_{Gf}	Front-gate voltage variation	v
V_{GP}	Ground plane voltage	v
V_{GS}	Gate to source voltage	v
V_H	Holding voltage	v
V_{in}	Internal node voltage	v
V_K	Cathode voltage	v
V_{ON}	Turn ON voltage	v
$V_{ON(DC)}$	DC turn ON voltage	v
ΔV_{ON}	Triggering voltage variation	v
V_T	Thermal voltage	v
V_{t1}	Triggering voltage	v
V_{t2}	Second breakdown voltage	v

V_{th}	Threshold voltage	v
W	Channel width	nm
W_{dep}	Depletion width	nm
WF_0	Gate workfunction	eV
Z_0	Impedance	Ω
λ_1, λ_2	Natural lengths in gated and ungated regions	nm
Φ	Potential	v
Φ_b	Initial ungated part potential of Z^2-FET	v
$\Phi_{b,final}$	Final ungated part potential of Z^2-FET	v
$\Phi_{b,sat}$	Saturated ungated part potential of Z^2-FET	v
$\Phi_{f,final}$	Final gated part potential of Z^2-FET	v
$\Phi_{f,sat}$	Saturated gated part potential of Z^2-FET	v
τ_{e-}	Electron lifetime	s
τ_{eff}	Effective carrier lifetime	s
τ_{max}	Maximum carrier lifetime	s

Introduction

The impressive development of microelectronic devices and circuits has enabled many new applications in several fields. Integrated circuits have become an integral part of our daily life as they can be found in the majority of electronic devices. Improving their performance and integration density requires a nonstop downscaling. However, nowadays they reach physical limitations, which implies searching for another concept. Proceeding from bulk to Silicon-On-Insulator (SOI) technology is one of the best solutions adopted by industrial companies. Thanks to Fully Depleted Silicon-On-Insulator (FDSOI), the Metal-Oxide Semiconductor FET (MOSFET) offers excellent features. Nonetheless, reducing its threshold voltage increases the leakage current and power consumption. As it is driven by the diffusion mechanism, the subthreshold slope is limited to 60 mV/dec. Hence, new software-hardware techniques from system to circuit level, dedicated to power saving, are a must. Different strategies have been proposed to reduce the supply voltage: channel engineering (Ge, III-IV, Graphene …), nanowire and nanotube FETs, circuits operate at low (cryogenic) temperatures. The study of structures achieving small swing switch is an attractive avenue that we have adopted. Band-modulation devices, which are the core of this thesis, offer not only a sharp switch but also very low leakage current, high current I_{ON}/I_{OFF} ratio, fast access time and adjustable triggering voltage. With these promising characteristics, the sharp-switching devices that have been developed can be used in many applications. We focus on Electro-Static Discharge protection (ESD), single Transistor Dynamic Random Access Memory (1T-DRAM) operation and logic switch.

Our goal is to explore band-modulation devices and verify whether they feature outstanding characteristics even at advanced 28 nm and 14 nm FDSOI technology nodes. The thesis was organized in four chapters, as described below.

An overview of sharp-switching devices is initially carried out in **Chapter 1**. Different variants with their operation principles are presented. The ESD physical mechanism, stress models and protection methods are highlighted. The last section is dedicated to 1T-DRAM application: the

state of the art of different structures in PDSOI, bulk and FDSOI technologies with their operation principle is described.

In **Chapter 2,** band-modulation devices fabricated with the most advanced FDSOI technologies (i.e. 28 nm and 14 nm) are presented. The band-modulation principle of Z^2-FET (Zero subthreshold slope and Zero impact ionization), which is unique for all variants, is investigated with Synopsis TCAD simulations. The advantage of implementing an N-type ground plane underneath the front-gate (Z^2-FET DGP) and operating with only back-gates (Z^3-FET with no front-gate) is explored.

The concept of modulating electrostatically the energy bands, proved with static DC electrical characterization, is further developed in **Chapter 3**. The dependency of device characteristics on anode, front and back-gates biases is highlighted for all-Si, SiGe and doped Z-FET structures. The ESD behavior and capability of sustaining high current is investigated using TLP characterization method. Finally, a model for the surface potential distribution in Z-FET structures is proposed.

The memory operation of sharp-switching devices is deeply analyzed with TCAD simulations, **in the fourth chapter,** and confirmed with systematic transient measurements. Operating as 1T-DRAM, Z-FET family devices feature high current margin and remarkable retention time. The feasibility of dense memory matrix is also discussed. A last section stands for the experimental proof of band-modulation devices as logic switches.

Finally, a conclusion recalls all the main achievements carried out in this thesis, and presents some perspectives to this work.

Chapter 1. Sharp-Switching Devices: State of the Art and Applications

SUMMARY

1.1. Introduction

The first chapter presents the context of topics developed during three years of PhD thesis work. First, we briefly introduce the history of MOSFET (Metal-Oxide Semiconductor FET) transistor and the trends of microelectronics. The unbreakable 60 mV/decade subthreshold slope of MOS transistor limits the reduction of power supply voltage even in FDSOI (Fully Depleted SOI) technology. This issue was the motivation of searching for sharp-switch devices described in the following. Devices with electrostatic modulation of energy bands attract attention nowadays. Thanks to their promising characteristics (sharp switch, low leakage current, adjustable triggering voltage), they can be used for many applications. In this chapter, we focus on ESD protection and single-transistor 1T-DRAM operation. The context and physical mechanisms of aggressive discharge current, stress models and ESD protection methods are highlighted. A review of several 1T-DRAM variants with different operation in PDSOI, bulk and FDSOI technologies is given to set the landmarks of my work.

1.2. MOSFET Transistor: State of Art and Trends

In 1930, J. Lilienfeld [1], the Polish-American physicist, was the first to provide the idea of three-electrode structure using copper-sulfide semiconductor material. Today this device is called a Field-Effect-Transistor (FET). Few years later, in 1948, the first device was fabricated at Bell laboratories by W. Shockley [2], J. Bardeen and W. Brattain [3] (Nobel Prize 1956) while the first Integrated Circuit (IC) was created by J. Kilby [4] (Nobel Prize 2000). These inventions have changed the human life and our society.

During the past decades, the CMOS technology [5] emerged as the dominant fabrication method for semiconductor integrated circuits where the MOS [6] (Metal-Oxide-Semiconductor transistor, Figure 1.1) was and still is the central component. Its function is similar to a switch. The role of a MOS is to let the current flow or block it by controlling the carrier channel (electrons or holes) with a transverse electric field created by the front gate polarization. On both sides of the channel are the source and the drain, which act as a tank of carriers.

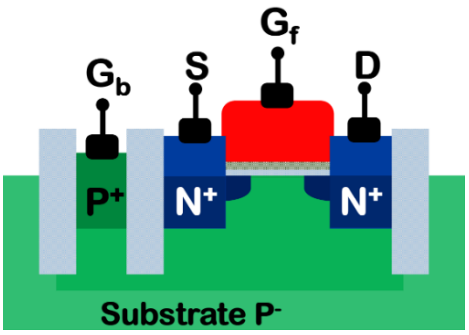

Figure 1.1. Schematic cross-section of N-type MOSFET transistor on 28 nm Bulk technology.

As CMOS technology is the driving force, the MOS transistor was almost exclusively fabricated on Bulk silicon substrate (type P for nMOS and type N for pMOS). The source and the drain are realized by implantation of donor/acceptor dopants next to the conduction channel. Considering the p-type silicon film, the source and the drain contacts are N^+ type. The gate is separated from the substrate by a dielectric layer. Generally, it is SiO_2 thanks to its very good compatibility with silicon. The Si active zone is detached from the rest of substrate by shallow trench isolation (STI). Thus, the space delimited determines the transistor geometry with a defined channel length L (distance between source and drain) and width W.

The transistor scaling down increases the on-chip transistor density. Nowadays, a chip can contain several hundred million, or even a few billion transistors. However, the fast downscaling puts almost an end to Moore's law. The cost of transistor is no longer decreasing while the equipment investment increases aggressively (Figure 1.2) [7]. Despite the challenge of enhancing its architecture (Metal Gate, LDD implant, Halo implant, …) and eliminating all unwanted parasitic effects, the bulk planar silicon MOSFET is facing severe problems when scaling beyond 28 nm node particularly with respect to power consumption [8-9]. Short channel effects [10] (SCE), such as threshold voltage roll-off, subthreshold slope (SS) degradation, mobility degradation and drain induced barrier lowering (DIBL) are some of these issues. When the device becomes smaller, the two depleted regions of source and drain can overlap affecting the channel electrostatic control induced by the gate bias. The potential distribution in the channel depends now on both transverse electric field (controlled by the gate) and longitudinal electric field (induced by the drain bias) which results in many forms of undesirable electrical behavior.

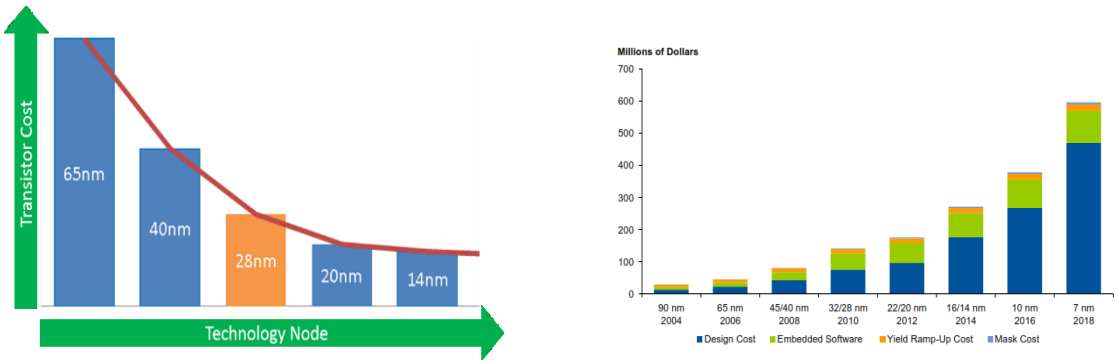

Figure 1.2. (a) Transistor manufacturing cost and (b) minimum scaling cost at recent technology nodes (GlobalFoundries 2015).

The MOS transistor implementation became more and more complex. In order to address this challenge and improve the device performance, adoption of new technologies, new materials and new architectures is required. One part of the biggest companies favored the transition into Fully-Depleted Silicon-On-Insulator (FDSOI) [11–13] planar technologies, while others decided to continue scaling with more complicated architectures such as FinFET [14, 15]. In this thesis we focus on FDSOI technology. In the next subsections a description of SOI, the benefits of this promising technology and its issues will be presented. Also we briefly define the MOS transistor in FDSOI technology.

1.3. Migration to FDSOI

1.3.1. SOI Technology

Unfortunately, existing solutions allowing the passage from the last node to next one are no longer sufficient to guarantee an optimal operation of MOSFET transistor (good current ratio I_{ON}/I_{OFF}). Thus, new technology architectures have been introduced to improve the electrostatic control of the channel by the gate. Among these, the Silicon-On-Insulator (SOI) took part as one of the best solutions [16]. The SOI substrate consists of undoped monocrystalline silicon film isolated from silicon substrate by a buried oxide (BOX). The active zone of transistor is defined on the upper silicon layer. Many techniques have been developed for producing a film of single-crystal silicon on top of insulator. However, SIMOX and UNIBOND seem to be the ideal candidates for VLSI CMOS applications [5]. SOITEC is the world's first SOI wafers provider using the SmartCut® technique (UNIBOND) [17]. The idea here is to realize:

1. An oxide layer on a silicon substrate (wafer A in Figure 1.3) followed by hydrogen ions implantation.
2. Hydrophilic bonding at room temperature of wafer A to a wafer B. Both wafers are previously cleaned using a modified RCA process.
3. Two-phase treatment of two wafers in order to split them into two parts at hydrogen ions level
4. In order to get a uniform and clean surface, a final touch of polish of SOI wafer is performed.

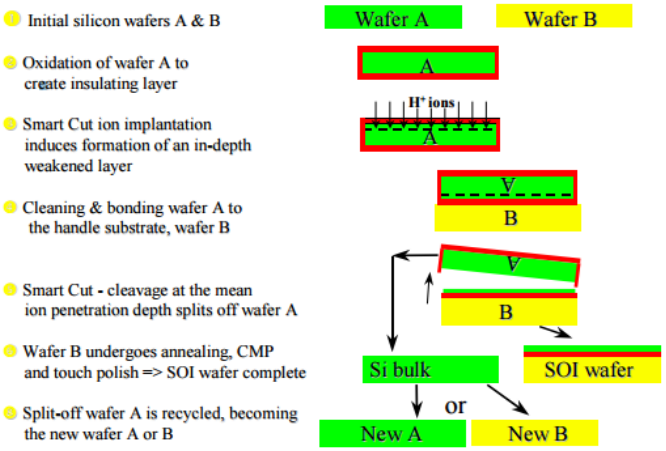

Figure 1.3. Schematic of SOI wafers fabrication using SmartCut® technique supported by SOITEC Company.

The SmartCut® CMOS approach features several outstanding advantages like better electrostatic control, reduction of parasitic capacitances between source/drain contacts and the substrate thanks to BOX presence, reduction of short-channel effects, improved device isolation and subthreshold swing enhanced, latch-up elimination, etc. In contrast, and like other technologies, SOI presents some drawbacks such as self-heating and floating body effects. However, the last issue (FBE) is useful for dynamic memory application as we will see later in section 1.6.

Two types of MOSFET transistors can be realized on SOI substrate. The first one is Partially Depleted Silicon-On-Insulator transistor (PDSOI [18]) where the depletion zone does not reach the BOX because of the important thickness of silicon film (t_{Si} > 50 nm). Conversely, with an ultra-thin silicon film the depletion zone reaches the buried oxide. Here we talk about Fully Depleted SOI transistors (FDSOI). In this thesis we focus on FDSOI devices and in the following subsection we describe the MOSFET transistor in Ultra-Thin Body and BOX (UTBB) FDSOI technology [16–18].

1.3.2. MOS Transistor in UTBB FDSOI Technology

Recently introduced by STMicroelectronics, the 28-nm UTBB FDSOI [12, 19] technology features a better electrostatic control and reduced undesirable parasitic effects. The process of MOS transistor starts from a SOI substrate with 25 nm of buried oxide (BOX) and 7 nm active silicon layer thicknesses. The thin buried oxide separates the undoped silicon film ($N_A \approx 10^{15}$ cm^{-3}) from a highly doped Ground Plane (with a concentration $N_{GP} > 10^{18}$ cm^{-3}) that prevents the substrate's deep depletion and acts as a back-gate. To access the GP and control the well potential, the BOX is locally etched. In 28 nm FDSOI process, a MOSFET can benefit from 2 types of ground planes (standard and flipped well, Figure 1.4). The undoped Si film is covered by a High-K dielectric and metal gate. This gate stack starts with a thermally grown oxide interface (SiO_2) covered by high-K material (HfO_2) and connected via a TiN or AlTiN metal layer. A silicon epitaxy is performed on the source and drain in order to reduce the access series resistances. After this step, Lightly Doped Drain implants (LDD) may be added at the source-channel and drain-channel junctions with the intention of reducing SCE and better controlling the transistor behavior. Finally, after the second gate spacer realization, the S/D are implanted (N_A, $N_D > 10^{20}$ cm^{-3}).

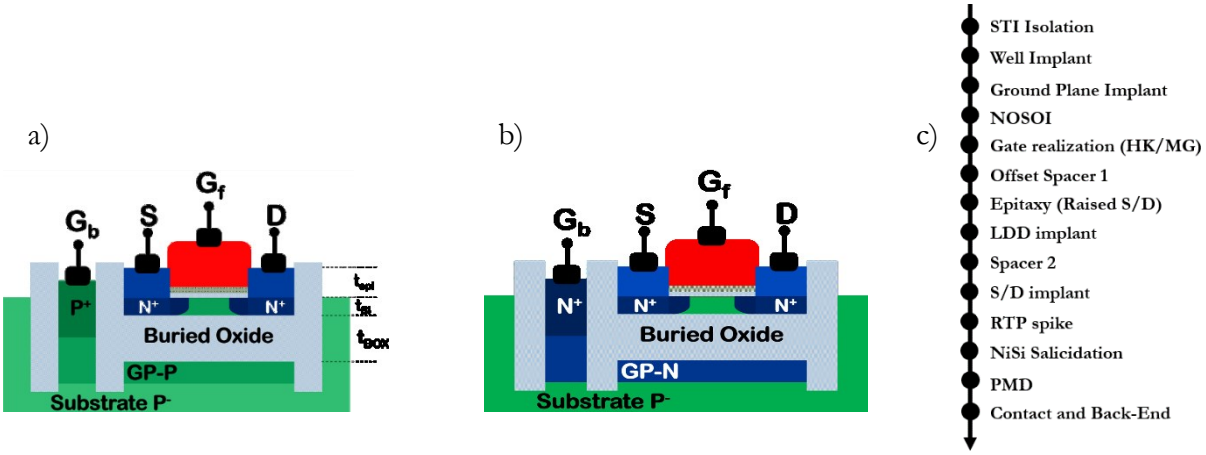

Figure 1.4. Schematic view of (a) standard and (b) flipped well MOSFET transistors in UTBB FDSOI technology. (c) 28FDSOI Front-End process flow.

Nonetheless, the outstanding UTBB technology with its numerous advantages motivated us to develop sharp switching devices that can break the 60 mV/decade subthreshold slope of MOS transistors. In the following section, innovative switches based on different physical mechanisms, such as band-modulation devices, which will be the core of this thesis, are described in details.

1.4. Sharp-Switching Devices

Lowering the "power consumption" is a big challenge especially after reaching CMOS downscaling limits. However, involving new semiconductor materials (Ge, III-V) into MOSFET's world is not yet a mainstream solution. The unbreakable 60 mV/decade subthreshold slope is a nightmare for a MOSFET transistor. Indeed, reducing the threshold voltage V_{th} with such a slope implies an off-state current (I_{OFF}) increase, and hence the static power consumption. In the hope of going below 60 mV/decade swing, several devices have been developed. We introduce these sharp-switch variants in the following subsections.

1.4.1. Tunnel Field Effect Transistor (TFET)

Due to its low subthreshold slope and good scalability, TFET is of great interest to replace or complement the MOSFET. Showed schematically in Figure 1.5-a, the Tunnel FET is essentially a gated P^+-I-N^+ diode [20] operating under reverse bias mode. Unlike the MOSFET which uses thermal carrier injection, the TFET utilizes band-to-band tunneling as a source for carrier injection mechanism. When there is no gate bias, the diode body is fully depleted and the band edges of N^+ and P^+ terminals are spaced out. There is no tunneling in this case and the TFET is in OFF-state. In contrast, increasing the gate voltage fills the channel with either electron or holes, depending on polarity ($V_G > 0$ V for N type and $V_G < 0$ V for P type), and alignment of energy band edges is observed. Now, the distance between the N^+ source and the P^+ channel is very short and the electrons can tunnel from the valence band of the P^+ region to the conduction band of the N+ region as shown in Figure 1.5-b.

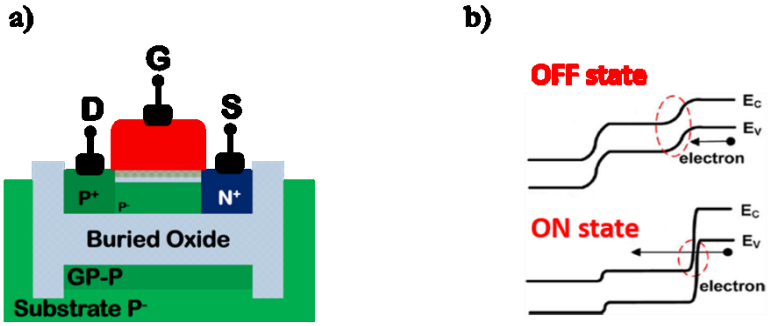

Figure 1.5. (a) Schematic view and (b) band diagram in ON/OFF states of planar all-Si TFET in silicon-on-insulator technology.

Figure 1.6 shows the transfer characteristics of N type all-Si TFET with a subthreshold SS = 52.8 mV/decade at low I_D current [21]. Despite the enhanced SS, all-Si TFET suffer from a poor current ratio I_{ON}/I_{OFF}. Even with a good SS achieved [21, 22], the best ON current is still low (46 µA/µm) in comparison with MOSFET [23]. For further I_{ON} improvement, many approaches can be considered such as lowering the bandgap by using alternative compounds like III-V [24], merging Si or replacing it totally with Germanium (Ge) [25]. Also, alternative geometries are of interest to enhance the I_{ON} current. For example, using a raised Ge electrode region permits a larger tunneling area and hence larger drain current could be obtained [S. H KIM and Schmidt] [26, 27]. Modifying the channel (EHB-TFET) [28] or combining a standard TFET with a Si/SiGe HBT in a single device (BET-FET) [29] are also proposed to achieve better I_{ON}/I_{OFF} current ratio. However, the TFET roadmap is still full of challenges and needs more convincing experimental validation.

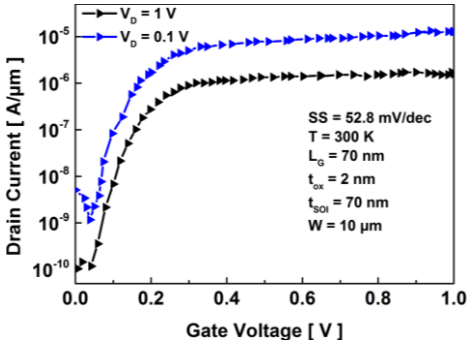

Figure 1.6. Room temperature experimental I_D-V_G characteristics of the first TFET showing SS < 60 mV/decade (adapted from W. Y. Choi et al. [21]).

1.4.2. Ferroelectric FET

A material is ferroelectric when it has two distinct polarization states, which can be maintained in the absence of an electric field and between which one can switch by applying an electric field. The main concept of Fe-FET [30], shown schematically in Figure 1.7, is replacing the gate dielectric by ferroelectric material. Polarizing the ferroelectric by applying a gate voltage modifies the conductivity of the semiconductor channel between source and drain. For example, a positive voltage directs the polarization along the semiconducting channel and results in a positive charge boosting the formation of an inversion electron layer. While switching the polarization to its other state, the ferroelectric charge becomes negative and the electrons close to the gate in the semiconductor get depleted. In this case, the Fe-FET is in OFF state with high threshold voltage V_{th} and low I_{OFF} leakage current.

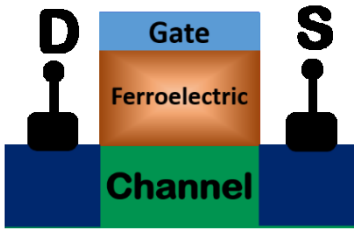

Figure 1.7. Schematic structure of a generic Ferroelectric FET.

Unfortunately, fabricated Fe-FET devices feature a high subthreshold slope (SS > 60 mV/decade). They suffer not only from reliability issues but also from technical problems such as Ferroelectric layer thickness, which should be ultrathin to prevent short channel effects induced by the drain fringing field. However, the technology of Fe-based negative capacitors is progressing [31, 32] and some solutions are proposed. For example, an external single-crystal $BiFeO_3$ capacitor is added in the series with the gate terminal leading to 8 mV/decade swing over 8 decades of current [33].

1.4.3. Nano-electro-mechanical FET

The concept of nanoelectromechanical FET [34, 35] consists in separating the gate from the channel by an empty cavity. More precisely, the gate electrode is anchored on two sides of the channel creating an air-gap between the channel and the gate (Figure 1.8). In the case of thick air-gap, the device operates with high gate voltage [34]. The gate is pulled up in OFF state with negative V_G and down in ON state with $V_G > 0$ V. However, the increased air-gap induces SCEs that limits the I_{OFF} current. In order to improve its operation, [36] proposed displacing the suspended gate in the opposite direction where the accumulation-mode channel is depleted when the gate is pulled down ($V_G < 0$ V).

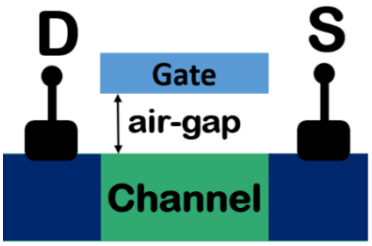

Figure 1.8. Schematic view of suspended-gate FET (SG-FET).

Silicon is the most common material in forming not only integrated circuits but NEMS also. However, the surface defects are uncontrollable in case of ultra-thin silicon. Instead, carbon nanotubes [37] and nanowires [38] are used. They feature perfect surfaces, mechanical and electrical properties but competitive NEM-FETs have still to be demonstrated.

1.4.4. NEM Relay

Nanoelectromechanical relay or NEM is a simple mechanical switch inspired from MOSFET. Here, a metal beam, controlled by electrostatic force, replaces the "channel". Figure 1.9 shows different NEM structures used for logic applications. The 2-Terminal switch (Figure 1.9-a) is the simplest mechanical structure composed of source and drain terminals [39]. However, it is not very useful for digital circuits because it requires a high actuation voltage (> 10 V) and presents non-separable input-output electrodes. The solution is introduced by the 3-Terminal relay where the gate (input) and the drain (output) electrodes are separated [40]. In order to move up and down the beam, the gate is polarized. The potential difference between gate and source (V_{GS}) determines the position of the cantilever beam while the drain current is determined by V_{DS}. The 4-Terminal switch is similar to 3T relay with an additional body terminal and insulating layer. Here the gate is moving and its position is controlled by applying a body voltage. Many structures have been fabricated, for logic and NVM applications [41–43], using different beam designs and various contact materials. However, the contact reliability remains a key issue. In order to improve the cycle endurance and face the "Hammer effect", some methods were proposed like covering one contact electrodes by thin SiO_2 layer [44] or introducing insulating oil as a packaging liquid [45].

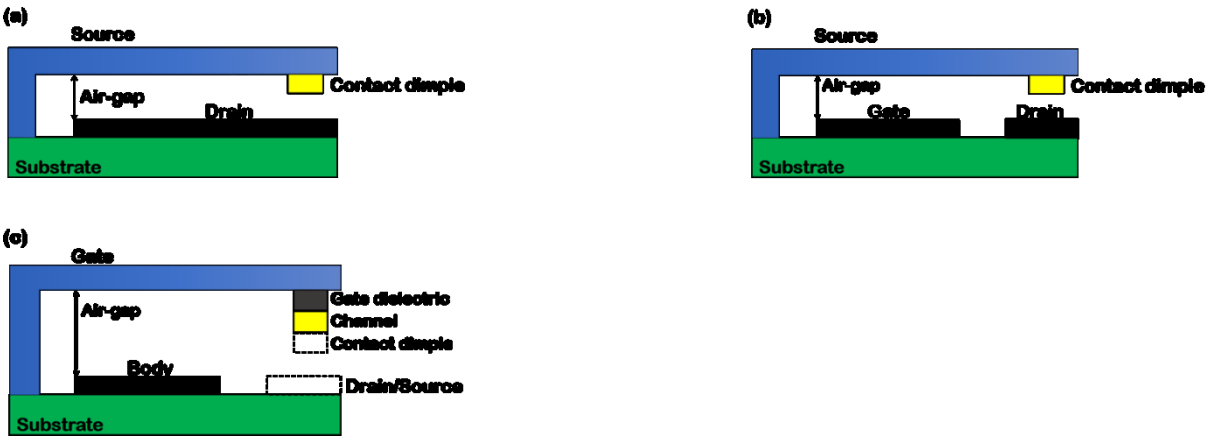

Figure 1.9. Cross sectional view of different NEM relay structures. (a) 2-Terminal (b) 3-Terminal and (c) 4-Terminal switches.

1.4.5. I-MOS: Impact Ionization MOSFET

Another interesting switching device with low subthreshold slope is the Impact Ionization MOS or I-MOS [46, 47], presented in Figure 1.10. The structure is similar to an asymmetric P-I-N diode partially covered by a gate and the rest of the channel is ungated. When there is no gate bias (V_G = 0 V) the device is in OFF state featuring a fully depleted channel and low leakage current I_{OFF}. The ON mode consists of increasing the number of holes in the channel, such as to reduce the length of the depleted region and induce avalanche breakdown. For this purpose, the gate is negatively biased and the drain is highly polarized (V_D > 0 V) leading to a sharp switch I_D-V_G as shown in Figure 1.10. However, the high drain bias is not so welcomed for pracitcal applications.

An original application of this device structure was invented in [48] where the operation principle (Z^2-FET) is different this time and it will be discussed in details in Chapter 2.

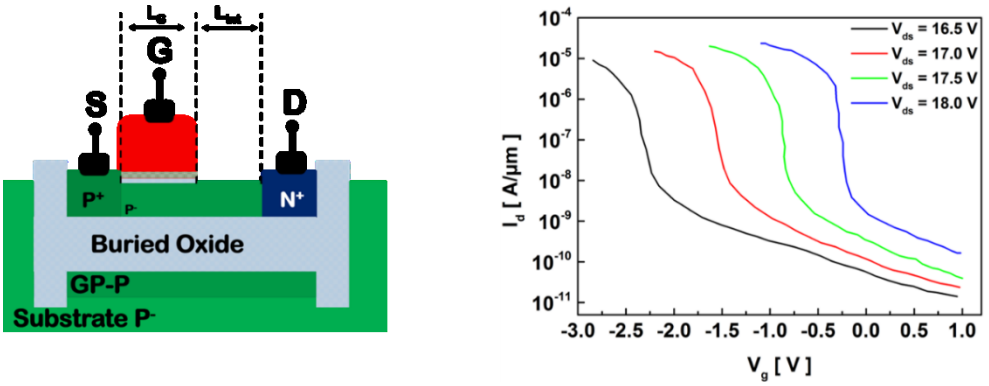

Figure 1.10. Basic device structure of I-MOS on SOI and measured I_d-V_g transfer characteristics for different drain bias (adapted from [47]).

1.4.6. Band-Modulation Devices: Operation Principle and Variants

Devices relying on bands modulation attract a lot of attention nowadays. They exist in different forms but the operation principle is almost the same. For example, the Field Effect Diode uses two adjacent front gates separated by a gap [49, 50], as shown in Figure 1.11. The diode is forward biased.

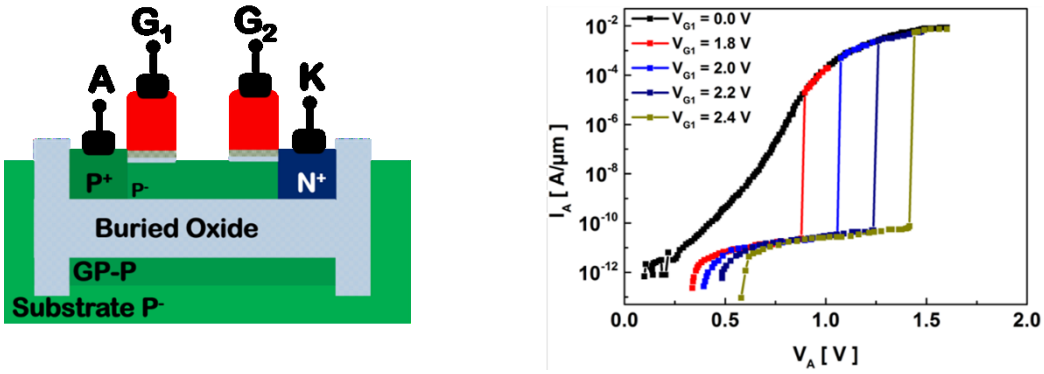

Figure 1.11. Schematic cross section and experimental DC I_A-V_A characteristics for different gate voltage V_{G1} and V_{G2} = 0 V of Field Effect Diode (FED) on SOI (adapted from [51]). $L_{G1} = L_{G2}$ = 500 nm.

Its operation principle relies on the formation of two barriers preventing the pass of carriers into the channel. Polarizing positively the gate beside the anode (G_1) creates an electron injection barrier blocking the pass of holes from the anode into the cathode. The region under the second gate (G_2) should be always in accumulation ($V_{G2} \leq 0$ V). With these conditions, the structure behaves as a thyristor (PNPN) with virtual doping. When anode voltage (V_A) increases, holes pass from the anode into the channel lowering the barrier under G_2. Being reduced, the barrier beside the cathode allows electrons migration into the anode lowering the G_1 injection barrier. This is called positive feedback mechanism. Once V_A reaches the triggering voltage V_{ON}, the barriers collapse leading to a sharp switch as presented in Figure 1.11. Moreover, the ON voltage can be modulated by changing the gate bias beside the anode (G_1) bias. In fact, raising up V_{G1} leads to a triggering voltage increase and if V_{ON} is higher than V_{dd} + 10%, it is possible to use the FED as a local ESD protection [51–53]. Despite the flexible control of barriers and promising characteristics, the FED suffers from the gap between the two front-gates. In fact, it affects not only the ON current but also the high frequency performance of the device. In addition, the FED length reduction should respect certain limit imposed by the gates gap.

This problem is solved with Z-FET family devices presented in Figure 1.12. Unlike FED, The Z^2-FET (Zero subthreshold slope and Zero impact ionization) [48, 54, 55] is fabricated with just one front-gate that modulates the barrier beside the anode while the barrier beside the cathode is manipulated by the back-gate, ground plane type P. An additional ground plane type N can be added underneath the gate of standard Z^2-FET in order to reinforce the G_f barrier. This device is called Z^2-FET DGP [56] (Dual Ground planes) while the third variant, Z^3-FET [57, 58] presented in Figure 1.12-c, presents no front gate and its barriers are controlled by N and P GPs acting as back-gates. These devices can be used for many applications such as ESD protection [54, 57–60] and capacitor-less dynamic random access memory, 1T-DRAM [59–63]. The state-of-art will be

discussed in the following subsections while the operation principle and detailed devices description will be presented in the second chapter of the thesis.

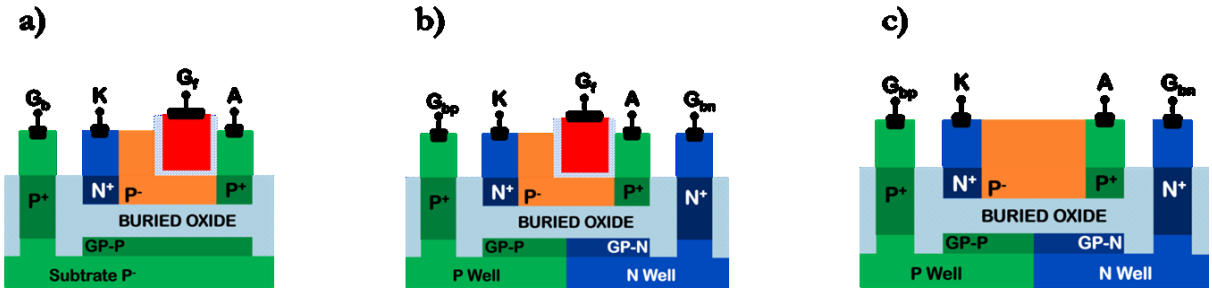

Figure 1.12. Schematic view of different band-modulation Z-FET devices: (a) standard Z^2-FET (b) Z^2-FET with dual GPs and (c) Z^3-FET with no front gate.

1.5. Electrostatic Discharge (ESD)

1.5.1. Context and Physical Mechanism

An electrostatic discharge is a charge reset of a system being initially unbalanced. It is originated by either triboelectric effect that occurs when two materials get into contact and then separated [66], or by electrostatic induction [67], which happens when an isolated IC undergoes an external electric field. Historically, MOS technologies were most susceptible to ESD discharges because of their gate oxide. This trend then spread to other technologies by means of aggressive downscaling and the challenge to protect thin devices with low supply voltage (V_{dd} < 1 V) from this harmful event became critical. Thus, innovative ESD protection devices are a must. Figure 1.13 defines the required specifications of an efficient protection element. The main important points presented in Figure 1.13 are the following:

- V_{dd}: the circuit supply voltage. The protection component should trigger after V_{dd} and should be transparent before it.
- V_{BD}: the breakdown voltage of protected devices in a core circuit. It is the maximum value tolerated by the used technology. The protection mechanism should be efficient before this value.
- (V_{t1}, I_{t1}): the turn-on voltage and triggering current of ESD protection device where it starts working, respectively.
- (V_H, I_H): the holding voltage and current. Below V_H, the device should be in OFF state.

- (V_{t2}, I_{t2}): the maximum voltage and current values that a protection component can withstand. Above these points, the device is broken and does not work anymore.

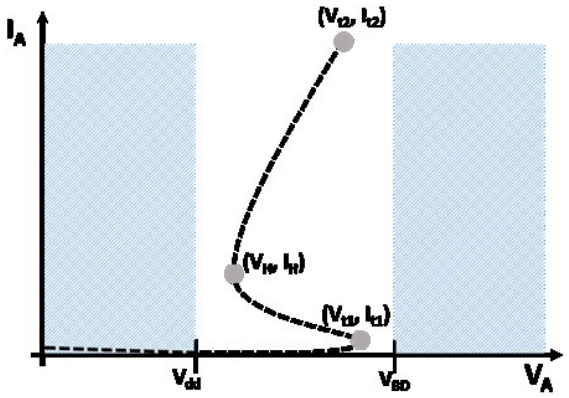

Figure 1.13. ESD design window and main required characteristics of electrostatic discharge protection devices.

The ESD design window presented in Figure 1.13 is valid whatever the used technology. However, the value of two limit points (V_{dd} and V_{BD}) varies with CMOS downscaling [68, 69]. The circuit supply voltage decreases while the breakdown voltage falls down dramatically. Consequently, the window becomes narrower and designing efficient electrostatic discharge devices becomes more difficult. Optimizing the fabrication process as proposed in [70, 71] and implementing reliable protection devices, which are suitable to the design window are of great interest [72]. In this thesis, we propose innovative ESD protection devices described in chapter 2.

1.5.2. ESD-Induced Failure in Integrated Circuits

The handling of electronic components in poorly controlled environments is the major cause of many failures due to electrostatic discharges. In addition of CMOS downscaling, using new techniques like light doped drains, silicidation, or ultrathin gate oxide makes modern integrated circuits more vulnerable to electrostatic discharges. Different ESD-type failures are considered in Figure 1.14. The most common breakdown mode in a MOSFET transistor is the gate/drain diffusion damage. In this case, the semiconductor material is locally melted due to high temperature, often observed in fabrication process, connecting the source and the drain together. Another frequent degradation type, shown in Figure 1.14-b, is the gate oxide damage of transistors. Eventually, when the electric field between drain and gate oversteps certain value (~ 12 MV/cm) due to high drain bias, it will cause damage in gate oxide. The gate isolation quality decreases and thus a leakage current increase is observed. Figure 1.14-c shows metal melting that occurs by Joule heating effect when a high current flows through metal interconnections. Usually, a metal

degradation is the consequence of another mechanism: it is possible that junction damage or gate oxide breakdown induce an open circuit, which greatly increases the current passing in metal interconnections, thus causing material melting.

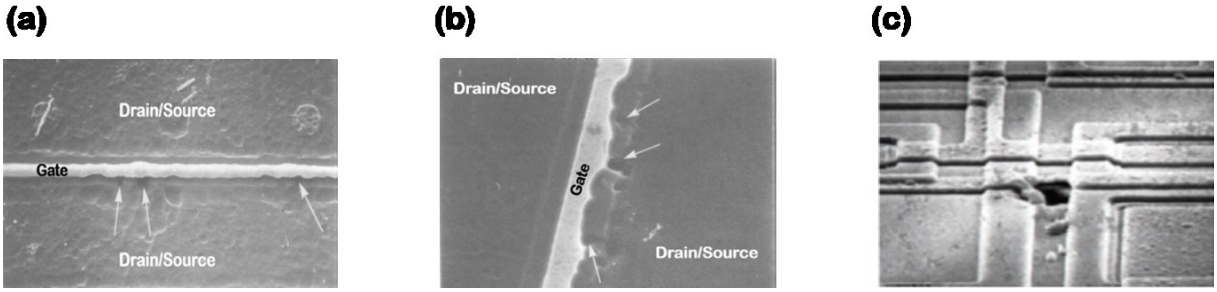

Figure 1.14. SEM photographs of different ESD-type failures: (a) damage at the drain/gate diffusion edge, (b) gate oxide damage and (c) metal interconnection melting [72].

1.5.3. ESD Stress Models

The real world ESD events can be represented by different stress models in the form of RLC circuit. This electrical circuit can simulate the same event as an electrostatic discharge when the integrated circuit is touched by a human (Human Body Model), or manipulated by a machine (Machine Model) or even the discharge of a component itself when it goes into contact with another grounded element (Charge Device Model). We describe in details the ESD models in the following subsections, along with the different characteristics of each example such as current wave form, rise time, period and oscillations.

1.5.3.1. Human Body Model

Human Body Model or HBM [73] describes the transfer of charges when a human touches a circuit. The electrostatic charge source is modeled by a charged capacitor (100 pF in this case, Figure 1.15) connected to the electronic chip by 1.5 kΩ resistance and an inductance of 7.5 μH representing the electric contact. Depending on application, the maximum voltage V_{ESD} a circuit can handle without incurring failures varies between 1 kV (RF, wireless, …) and 4 kV (automotive, military, …). Applying these values into the simplified Eq. (1.1) allows us to calculate the discharge current:

$$I_{ESD}(t) = \frac{V_{ESD}}{R_{ESD}}\left(1 - e^{-\frac{R_{ESD}}{L_{ESD}}t}\right)\frac{-t}{e^{R_{ESD}.C_{ESD}}} \quad (1.1)$$

In order to get closer to the test environment, a parasitic inductance L_{ESD} is added to the circuit which together with R_{ESD} define the rise time (between 2 ns and 10 ns) of current waveform presented in Figure 1.15. Then, the current decreases exponentially with relatively smooth fall time (150 ns) defined by the product of two circuit elements R_{ESD} and C_{ESD} for a total ESD stress duration of ~ 500 ns.

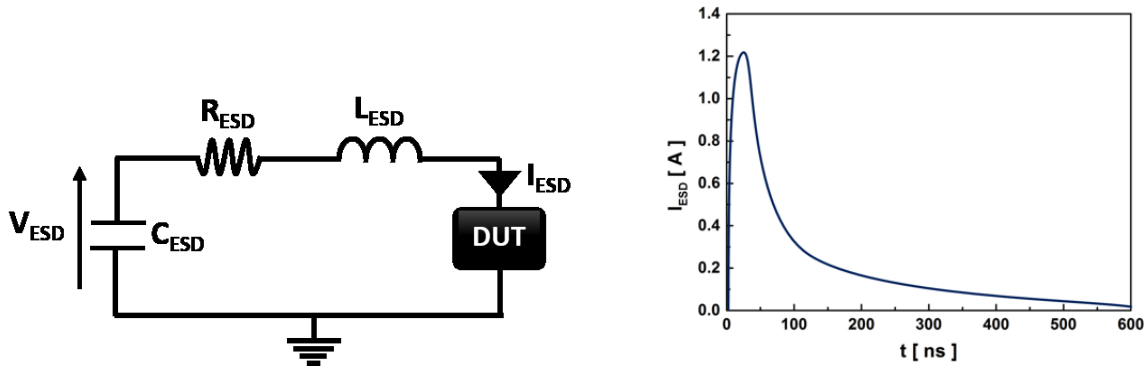

Figure 1.15. Schematic equivalent circuit of ESD stress model HBM with typical parameters and its discharge current waveform (R = 1.5 KΩ, C = 100 pF, L = 7.5 µH and V = 2 kV).

1.5.3.2. Machine Model

The Machine Model or MM was introduced first by Japanese IC manufacturers as a more severe case than HBM model. This time, the human is replaced by a machine. Consequently, the equivalent circuit of this ESD-type model in Figure 1.16 is different. The resistance and inductance values are greatly decreased (R_{ESD} = 10 Ω and L_{ESD} = 0.5 µH, metal contact) while the capacitance value is doubled (C_{ESD} = 200 pF).

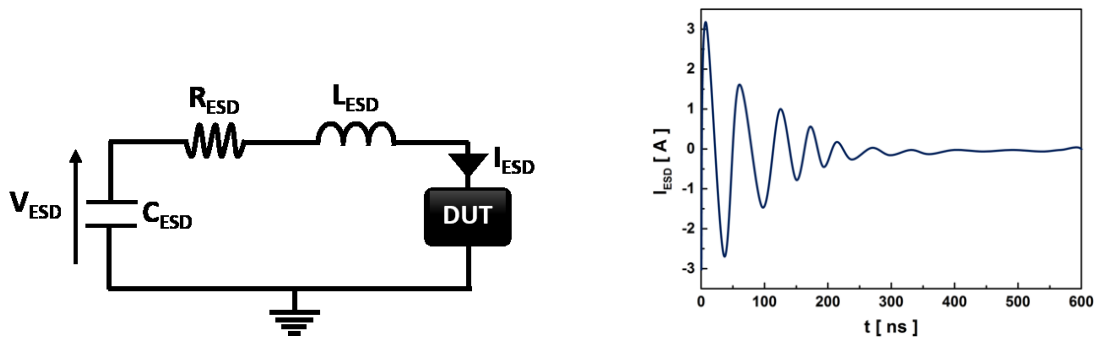

Figure 1.16. Schematic equivalent circuit of ESD stress model MM with typical parameters and its discharge current waveform (R = 10 Ω, C = 200 pF, L = 0.5 µH and V = 200 V).

In fact, integrated circuits are called to withstand at least 200 V discharge amplitude for which, in MM case, a damped oscillation is observed in Figure 1.16. The ESD discharge current can be calculated using Eq. (1.2) :

$$I_{ESD}(t) = V_{ESD}\sqrt{\frac{C_{ESD}}{L_{ESD}}}e^{-\frac{R_{ESD}}{2L_{ESD}}t}\sin\left(\frac{1}{\sqrt{L_{ESD}\,C_{ESD}}}t\right) \quad (1.2)$$

1.5.3.3. Charge Device Model

The most frequent discharge mechanism in automated handling environment is the Charge Device Model or CDM. It is modeled by a small value of capacitance (between 4 pF and 30 pF) [67, 74]. Of course, after assembly and packaging, components could be charged in different ways and if they go into contact with a grounded metallic surface, an extremely rapid and severe discharge is produced. In particular, the CDM event lasts for few nanoseconds (5 to 10 ns) with rise time of picoseconds and a high peak of current (~ 15 A) with a damped pseudo-periodic waveform as shown in Figure 1.17.

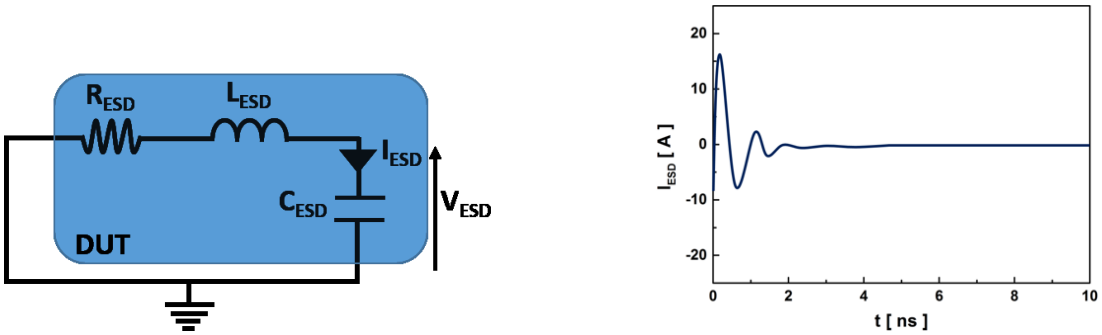

Figure 1.17. Schematic equivalent circuit of ESD stress model CDM with typical parameters and its discharge current waveform (R = 10 Ω, C = 10 pF, L = 2.5 µH and V = 1 kV).

1.5.4. Protection Methods

Finding the best current path between two pads, usually the discharge source (I/O pad, supply voltage pad V_{dd} …) and ground pad (V_{ss}) presented in Figure 1.18, without affecting the circuit core, is a simple definition for ESD protection strategy. In practice, protection devices should be able to deviate the discharge current into the ground avoiding sensitive components. For this purpose, good ESD clamp should respect certain conditions [72]:

- **Robustness**: the protection element should not fail before evacuating the required discharge current. This property is defined by V_{t2} and I_{t2} points that can be evaluated with Transmission Line Pulse (TLP) characterization described in details in the following subsection.
- **Effectiveness**: an efficient ESD clamp triggers after the supply voltage (V_{dd}) and before the breakdown voltage (V_{BD}) of core circuit (already discussed in 1.5.1) evacuating a sufficient discharge current.
- **Speed**: the turn on of ESD protection should be fast enough, avoiding overshoots especially in CDM events with sub nanoseconds rise times.
- **Transparency**: the protection should feature low leakage current in OFF state when the circuit operates normally. Moreover, the clamp capacitance should be very small avoiding the perturbation of high-frequency circuit operation.

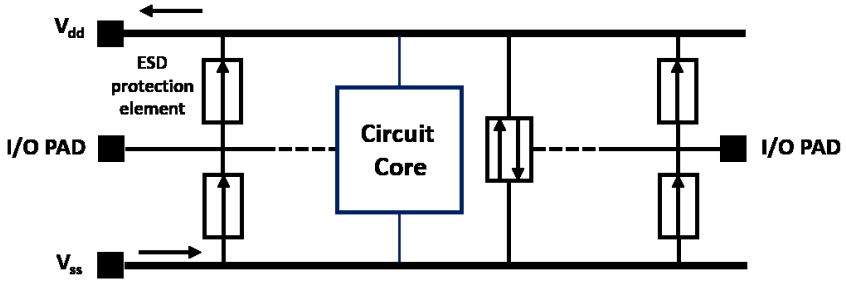

Figure 1.18. Classical schematic view of CMOS integrated circuit with ESD clamps and different input, output and supply voltage pads.

Prevention methods such as using air ionizers, antistatic bags and packages for transport, carrying grounded wrist straps at the work bench while handling integrated circuits are helpful but not sufficient to protect against aggressive discharges. Besides, self-consistent protection by implementing ESD devices on-chip is a need. Indeed, there are two ways of protection against an ESD event arising between a pad and the ground. Figure 1.19-a shows the "global" strategy in which a unidirectional clamp is placed beside each pad driving the discharge current into the central bidirectional protection element located between the supply voltage rail V_{dd} and ground pad V_{ss}. Another approved method is called "local" strategy presented in Figure 1.19-b. It consists of using just one bidirectional protection clamp situated beside each ESD source pad to evacuate at the same time positive (in red) and negative (in blue) discharge currents.

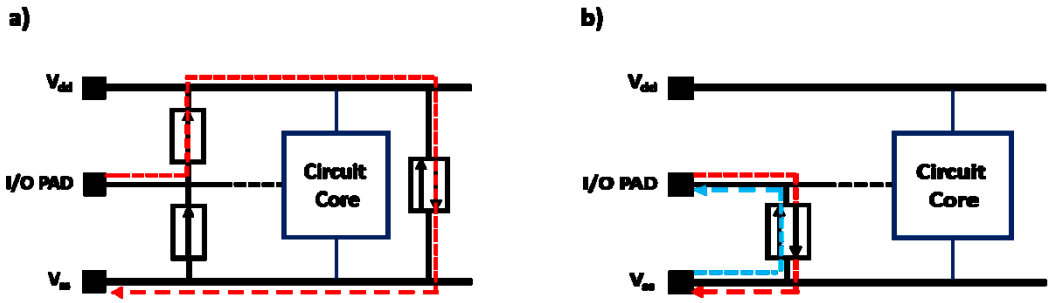

Figure 1.19. Simplified ESD protection examples: (a) global strategy and (b) local strategy evacuating positive (in red) and negative (in blue) discharge currents.

Circuit designers have the choice now to choose between these two strategies ensuring an adequate protection against electrostatic discharges and taking, of course, into consideration surface constraints.

1.5.5. Characterization Methods

The ESD response of protection elements cannot be evaluated with DC characterization. In fact, static measurements with high voltage and current values certainly will destroy the "Device Under Test" (DUT) by excessive heating effect. Instead, an efficient technique (Transmission Line Pulse), proposed for the first time by Tim Maloney in 1985 [75], is used for clamp devices interpretation. The pulsed system will be discussed in details in the following subsection.

1.5.5.1. Transmission Line Pulse (TLP)

Transmission Line Pulse technique is based on generating pulses with high current values through a transmission line. Indeed, this method becomes the main measurement tool giving needed information on ESD protection behavior and efficiency. Actually, the famous 100 ns pulse width of TLP measurement is the typical duration of HBM stress model. It can be adjusted by modifying the length of the transmission line according to $t_{pulse} = 2L/v$, where v is the wave propagation speed. The quasi static I-V characteristic is constructed point by point until the breakdown (V_{t2}, I_{t2}) of analyzed device. Each point of the curve corresponds to the average of DUT voltage response on transmitted current pulse.

There are three common methods used in TLP measurements. However, every technique has its own advantages and drawbacks. The first one, Time-Domain Reflectometry or TDR described in Figure 1.20, is used to determine the current and the voltage at the device terminals with the

help of incident and reflected voltage pulses. In fact, when the emitted signal meets an impedance discontinuity, a part of its energy is returned to the pulse source. Thus, the expected information of tested device is obtained after analyzing the reflected signal. It is not possible, with this method, to characterize a tripole. Moreover, the indirect current and voltage measurement induces inaccurate results.

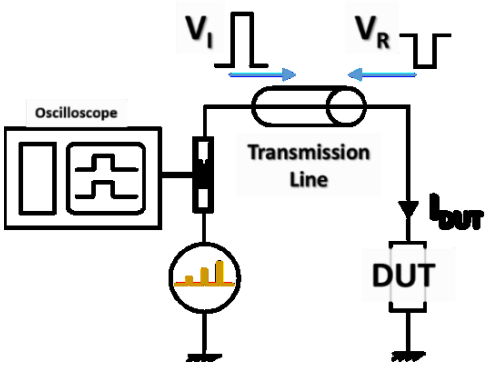

Figure 1.20. Time Domain Reflectometry (TDR) characterization technique.

On the other hand, Time Domain Transmission (TDT) method consists of using emitted and transmitted voltage pulses to measure the current at the device terminal. In this case, a part of emitted current pulse is drifted from the DUT towards the scope by a second transmission line (with impedance $Z_0 = 50\ \Omega$), as shown in Figure 1.21. Comparing to TDR technique, the measured voltage of tested device is more accurate ($V_{DUT} = V_T$).

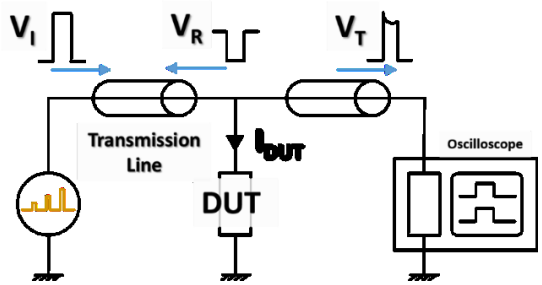

Figure 1.21. Time Domain Transmission (TDT) characterization technique.

The last technique, Time Domain Reflection and Transmission (TDR-T), associates the two previous approaches. The device is not connected to the ground anymore, but into the oscilloscope through another transmission line as shown in Figure 1.22. This time, the current measured crossing the DUT is well defined ($I_{DUT} = V_T/Z_0$, where Z_0 is equal to 50 Ω).

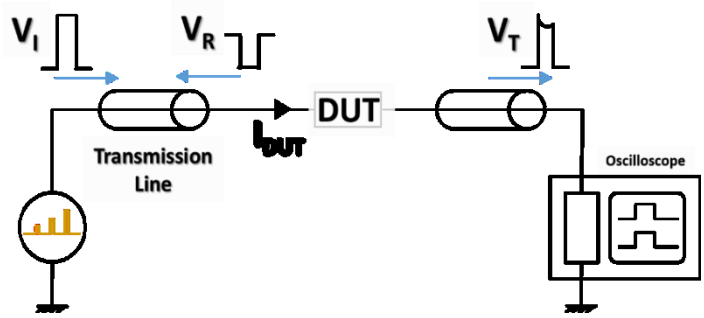

Figure 1.22. Time Domain Reflection and Transmission (TDRT) characterization technique.

The current pulse width and rise time can be decreased down to few ns, up to 300 ps by shortening the length of transmission line connecting the voltage source to the structure under test. With these small values, we get closer to the time range of CDM stress model, we are talking here about Very Fast TLP (VF-TLP) [76]. However, this technique does not offer the best correlation of stress currents between single pin CDM stress and two pins VF-TLP. Presented in Figure 1.23, the optimized version CC-TLP [77] (Capacitively Coupled TLP) injects high current pulses via a single pin while the other one is connected to the ground through a background capacitance C_b. During the stress C_b charges, and discharges at the end of the pulse, through the protection element showing better correlation with CDM model.

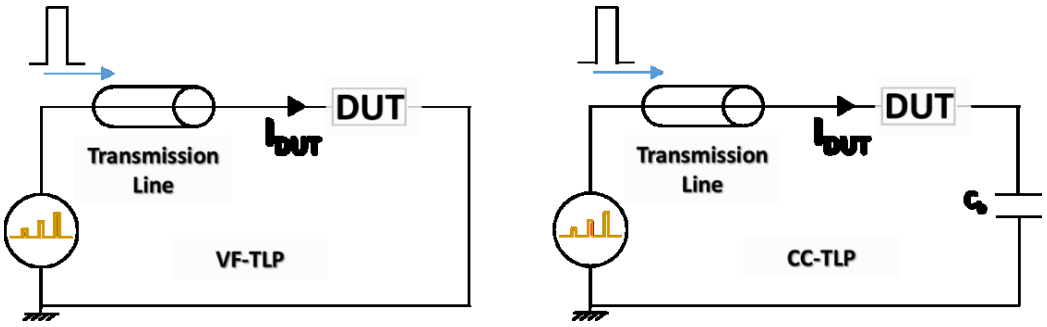

Figure 1.23. Equivalent circuits of VF-TLP and CC-TLP stress tests.

During this thesis work, the ESD behavior of our devices has been investigated with TLP and VF-TLP measurements using TDT technique. Detailed results will be presented in Chapter 3.

1.6. 1T-DRAM: Capacitorless Dynamic Random Access Memory

1.6.1. Introduction

Everyone is looking for a semiconductor universal memory that offers very fast access time, high integration density, infinite retention and low fabrication cost. The idea here is to bring together the perfect characteristics of volatile and non-volatile memories into a single device that would be able to store the information infinitely when there is no supply voltage, featuring low power consumption, unlimited endurance, and of course be compatible with modern technologies with aggressive scalability (Figure 1.24). Unfortunately, a memory that fits all these requirement does not exist at the moment. Nowadays, companies are trying to reduce the large gap between existing solutions and perfect memory. They already succeeded to combine just two or maximum three of previous conditions.

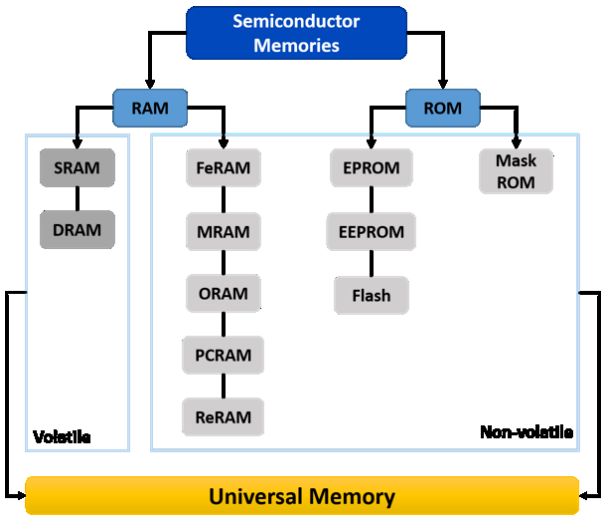

Figure 1.24. Organigram of semiconductor volatile and non-volatile memories. Universal memory is a combination of perfect characteristics of these two categories of memories.

Volatile memories, with Random Access Memory (RAM) as a trade name, could be static (Static RAM, SRAM) or dynamic (Dynamic RAM, DRAM). They present very fast access time (1 to 10 ns) but they lose the stored information when the supply voltage is turned off. In comparison with DRAM, SRAM are faster with higher retention time. However, they occupy more surface because of their architectures composed of many transistors. 4T-SRAM (4 transistors) may be smaller than 6T cell but it still about four times larger than a comparable DRAM cell. Moreover,

applications demanding low power consumption (mobile phones, computers, servers …) favor the use of dynamic memories while static cells are used for high performance functions (Cache Memory).

The second category of memories is non-volatile memories, or NVM. They feature high integration density and long retention time (10 years) even if there is no power supply. Today, many types of emerging technologies with new materials are under investigation in order to get as close as possible to the universal memory. Those are magnetic memories MRAM [78], organic memories ORAM [79], memories with ferroelectric materials FeRAM [80], phase change PCRAM [81], and resistive memories ReRAM [82] that attract a lot of attention nowadays due to their promising characteristics. However, they are still prototypes. From a commercial point of view, Flash memories dominate the market of NVM. They are used in applications where the information is stored for long time such as USB flash drives, hard disk drives and also in portable digital cameras. The use of this type of architecture is advantageous because of its very small cell size and high retention time. Nonetheless, strong applied bias voltages with high programming time limit the number of cycles (10^6 cycles) of Flash memories.

Whatever the type is and despite all technical challenges, the market of memories is still increasing. The quest for the best candidate that will imitate the universal memory continues. In the following subsections, we focus on dynamic RAM with and without capacitance in different technologies (Bulk, PDSOI and FDSOI); how they work and examples of different variants will be presented.

1.6.2. Motivations and State of the Art

Working at IBM Thomas Watson research center, Robert Dennard invented in 1968 one of the most selling memories today in the world, Dynamic Random Access Memory (DRAM). It has been commercialized two years later by Intel in a 1 Kb PMOS integrated circuit defeating at that moment the magnetic core type memory. Each memory cell consists of one access MOS transistor and a storage capacitor where the information is saved in form of charges ($\sim 10^6$ electrons). Respecting scaling rules of progressing technologies, DRAM cell surface is reduced 2 times while the integration density is multiplied by 4 every three years [83]. However, this surface reduction was rapidly limited not only because of the storage capacitor but also the access transistor. In order to solve this problem, two 3D structures have been proposed: trench [84] and stacked [85] capacitor DRAM cells presented schematically in Figure 1.25. The trench technology consists of first etching

deep and narrow trenches and then connecting them to the transistor, fabricated in a second step, with buried straps. Contrarily, the stacked method counts on realizing the capacitance after CMOS procedure. Besides, other techniques have been introduced in order to give more surface and enhance the capacitance value such as using poly silicon HSG or metal electrodes (ruthenium or TiN), replacing the nitride dielectric by materials with high dielectric constant (Al_2O_3, HfO_2) or mixing the dielectric materials (Al_2O_3/HfO_2).

Thanks to these two architectures, the 1T-1C DRAM cell reached a high integration density. Nowadays, the downscaling of memory elementary cell is still going on. However, difficulties related to process integration of both capacitance and access transistor are expanding especially beyond 90 nm node where the fabrication steps rebel against conventional CMOS. For this purpose, breakthrough architectures without external storage capacitor are proposed as alternatives to conventional DRAM memories. The operation principle is presented in section 1.6.3.3.

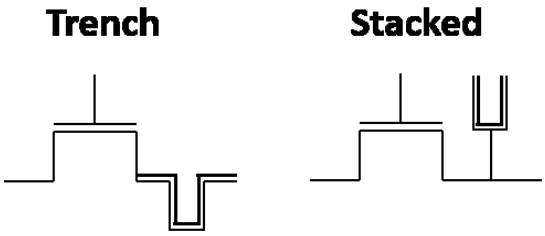

Figure 1.25. Schematic presentation of 1T-1C Dynamic Random Access Memory (1T-1C DRAM) with trench and stacked capacitors.

Whether volatile or non-volatile memories, they are divided into two categories: Stand Alone where the memory array is realized independently of logic circuit, and embedded memories where logic transistors are combined with memory cells on the same chip. The last system (embedded memories, eDRAM) attracts a lot of attention nowadays featuring high performance, huge volume of exchanged data, very low power consumption and of course high integration density. Despite all these advantages, the co-integration of logic functions and memories on the same chip implies an increase of process steps and hence the cost of fabrication. The key feature of eDRAM [86] cells integration is to find the best compromise between manufacturing cost, integration density and power consumption according to applications. This was our motivation to test band-modulation devices, which are fully compatible with the most advanced fully depleted CMOS technology, as capacitor-less DRAMs. Experimental results will be investigated in details in the last chapter of this manuscript.

1.6.3. 1T-DRAM in Partially Depleted SOI and Bulk Technologies

1.6.3.1. Floating Body Effects (FBE): an advantage for transistor operating as 1T-DRAM

The most challenging issue in Partially Depleted Silicon on Insulator (PDSOI) and bulk technologies, is the control of Floating Body Effects [87] (FBE). In form of mobile charge, FBEs appear in the device body due to the isolation of silicon film by using the buried oxide (BOX) layer in the case of PDSOI (Figure 1.26-a), or the implantation of N layer in the lower part of substrate P of Bulk transistors (Figure 1.26-b). Hence, these charges are confined since they cannot escape through the substrate.

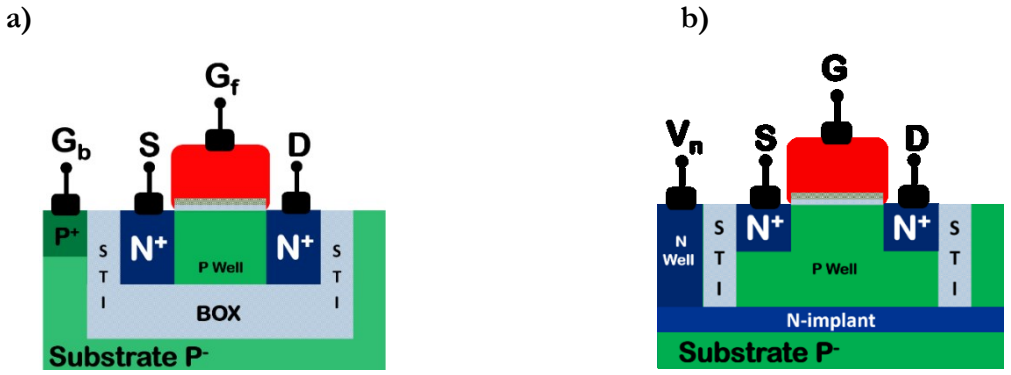

Figure 1.26. Schematic cross sections of N type MOSFET transistors in (a) Partially Depleted SOI technology where the floating body is isolated by the buried oxide or (b) by an implant N-type in the case of Bulk technology.

Originally, FBEs such as history effect, Kink effect and parasitic bipolar are considered as parasitic effects during the normal operation of a transistor. In particular, we focus on Kink effect [88, 89] that appears in the form of an overshoot on I_D-V_D curve at high drain voltage bias and an enhancement of subthreshold slope in transfer characteristic I_D-V_G of the transistor, shown in Figure 1.27. In fact, the high electric field, induced by polarizing the transistor in saturation regime ($V_D > V_{DSAT}$, $V_G > 0$ V), triggers the impact ionization phenomenon close to the drain zone. This mechanism generates pairs of electron-hole in the space charge region of the junction. Minority carriers are swept into the drain, positively biased ($V_D > 0$ V), increasing the conduction current while majority carriers, driven into the neutral zone of the floating body, modify the body potential, V_B. For example, for nMOS transistor (PDSOI or Bulk), the holes generated by ionization and injected in the floating substrate will increase the potential V_B inducing a threshold voltage reduction. The threshold voltage V_{th} drop leads to a feedback mechanism that increases the drain current which is the origin of the bump observed in Figure 1.27.

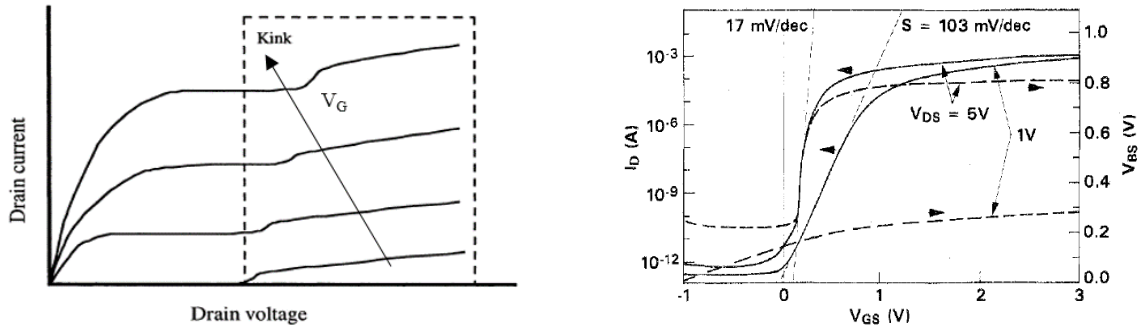

Figure 1.27. I_D-V_D output characteristics [90] on N channel MOSFET showing the kink effect as a bump and I_D-V_G transfer characteristics [91] showing kink effect in the form of steeper subthreshold slope (SS = 103 mV/dec for V_D = 1 V increases up to 17 mV/dec for higher V_D = 5 V).

The dynamic fluctuation of body potential produced by Kink effect becomes an increasing interest as a memory outcome. In fact, the floating substrate of these transistors can be used to store the information in form of body charges and read it by applying voltage pulses on drain (V_D) and gate (V_G) terminals.

1.6.3.2. Different 1T-DRAM Architectures in PDSOI and Bulk Technologies

The first capacitor-less memory in PDSOI technology was proposed in 1990 [92]. It has not been developed because it does not present a selective programming method which is a necessary condition for this kind of memories. Few years later, in 1993, the problem was solved by conceiving another 1T-DRAM cell accompanied by two transistors for writing and reading [93]. However, it was a complex architecture that needed large surface. The topic came back later in 2001 [94], with a rigorous proposition in 0.25 μm and 0.13 μm CMOS technologies. The area occupied by each innovative cell was half of that of a conventional 1T-1C DRAM. Thanks to their promising characteristics, industrial companies started looking forward in order to implement the cells in matrices; the first one was a 96 Kbit unveiled in 2003. After the demonstration of the possible implementation of these cells in 22 nm node CMOS, offered by Toshiba, other groups tried to find comparable programming methods that reduce the power consumption and increase the retention time. Looking at all these results, we can say that 1T-DRAM memories in PDSOI technology, presenting high integration density and faster programming time, had potential to replace the conventional DRAM memory.

Regarding bulk technology, the first free capacitance memory cell was proposed in 2003 [95]. The concept is similar to those in PDSOI technology. However, the body of the transistor (NMOS) is isolated not with a buried oxide but with an implantation of N layer in the lower part of the

substrate P (~ 1 µm depth). The first variant, fabricated in 120 nm CMOS technology [96], is isolated laterally with not very deep STI (Shallow Trench Isolation) coupled with N wells on both sides, as presented in Figure 1.28-a. It features promising results as a memory cell. However, this architecture does not fulfil the required objectives of 1T-DRAM memory because of its low integration density. The surface of elementary cell reaches $54F^2$ per bit which is much higher than a classic 1T-1C DRAM with $8F^2$/bit surface (F is the minimum dimension that can be achieved in a technology node). In order to get rid of this disadvantage, another method of device isolation was called. The N doped lateral wells, used for isolation, were replaced by deep shallow trenches touching the buried N layer, as seen in Figure 1.28-b. The surface is highly reduced with this approach ($18F^2$/bit) which makes it competitive to a conventional embedded 1T-1C DRAM with 25-30F^2 elementary surface. However, the realization of deep and large STI (0.18 µm of width and > 1 µm of depth in 120 nm CMOS node) is not so easy with complicated manufacturing process steps which increase the cost of cell fabrication. For this reason, it was replaced rapidly by another innovative solution with simple integration, shown in Figure 1.28-c [97]. This method consists of realizing the P-N junction directly under the standard STI, without any additional modification, and keeping the same surface ($18F^2$) as for NMOS with deep insulator trenches. Designed and fabricated at STMicroelectronics, the 1T-DRAM cell in 120 nm node featured promising results with decent retention time (100 ms at 85°C) and good current ratio I_1/I_0. A matrix of 8Mbits 1T-DRAM was also demonstrated with a current detection circuit (Current Mode Sense Amplifier, SA) [98]. This successful work was transferred to the following node (90 nm CMOS technology) [99]. Comparing to 1T-1C DRAM, obtained results on both elementary memory cell and matrix levels were featuring higher integration density (26% saved surface at matrix level). In the next subsection, we develop the operation principle of the previous memory variants.

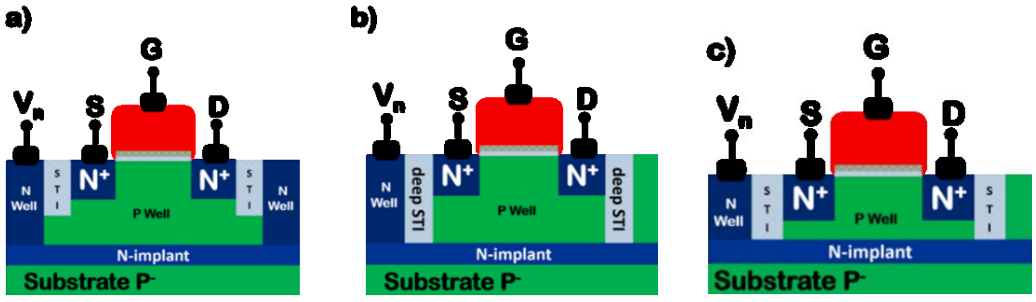

Figure 1.28. Architectures of 1T-DRAM memory cell on Bulk: (a) Triple wells. Conventional STI together with N Well isolate laterally the floating body while the N-type implant ensures the isolation of the lower part of the substrate. (b) Second variant with deep STI. (c) Variant with buried implant layer N-type touching the conventional STI isolation.

1.6.3.3. Operation Principle

The operation principle of all 1T-DRAM versions, illustrated in Figure 1.29, is almost the same. The state "1" reflects an excess of majority carriers in the body causing an increase of the potential ($V_B > 0$ V) and drain current while the "0" state consists of removing majority carriers from the body. In this case, the potential is lower implying higher threshold voltage V_{th} and low drain current.

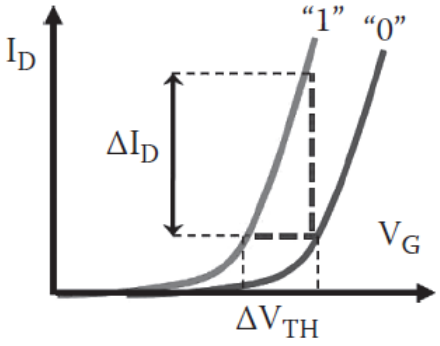

Figure 1.29. I_D-V_G transfer characteristics of N-channel SOI MOSFET transistor showing the 1T-DRAM memory "1" and "0" states.

In order to generate the majority carriers, several mechanisms have been offered such as impact ionization, bipolar junction transistor, and band-to-band tunneling. The Table 1.1 presents the impact ionization technique used to program the state "1" of 1T-DRAM in both Bulk and PDSOI technologies. Erasing, reading and holding methods are also mentioned.

Mode	Source	Drain	Front Gate	N-Implant (Bulk)	Back Gate (PDSOI)
Write "1"	0 V	> V_{DSAT}	> V_{th}	> 0 V	0 V
Write "0"	0 V	< 0 V	> 0 V or < 0 V (PDSOI)		
			< 0 V (Bulk)		
Read	0 V	< V_{DSAT}	> V_{th}		
Hold	0 V	0 V	< 0 V (PDSOI)		
			0 V (Bulk)		

Table 1.1. Operating bias for N-MOSFET transistor used as 1T-DRAM in Bulk and PDSOI technologies.

The operating mechanisms are almost the same in these technologies. However, they differentiate in holding the stored information. In order to limit the leakage current and save the information for a long time, in PDSOI technology, the front gate is biased negatively keeping the

diodes in reverse mode. Programming state "1" is done by impact ionization. A positive voltage pulse is applied on the front gate ($V_{Gf} > V_{th}$) accompanied with a positive drain pulse higher than the saturation voltage V_{DSAT}. With these polarizations, the electrons in the channel are accelerated by the high electric field present in the space charge region close to the drain and generate by impact ionization electron-holes pairs. The electrons are guided towards the drain while holes are injected into the floating body of the transistor where they will be stored. For the "0" state, the drain/body junction is forward biased by applying a negative drain pulse. In this case, the stored holes are evacuated and electrons are injected from the drain into the body lowering the potential. At the same time, in 1T-Bulk devices, a negative pulse is applied on the front gate switching off the transistor and strongly reducing the dynamic power consumption. In order to keep a remarkable margin between "0" and "1" states, it is strongly recommended in PDSOI technology to bias positively the gate instead of a negative pulse. Although, a negative gate pulse is used for "0" selective writing mode which is a big challenge in 1T-DRAM world. In reading mode, a high positive pulse is applied on the front gate terminal, while the drain voltage is smaller ($< V_{DSAT}$) in order to not trigger the impact ionization mechanism that will disturb the "0" state of the memory cell. During all memory operations, the N buried layer (in Bulk technology) should be biased positively allowing a perfect body isolation. In this case, the leakage current of the reversely biased P-N diode is low.

This overview allows us to conclude that DRAM architectures without external storage capacitor in bulk technology can be used for embedded memory applications while PDSOI devices are viable as standalone memories. However, the evolution of 1T-PDSOI memory cells is facing serious problems with CMOS downscaling. In order to guarantee the neutral zone in sub-100 nm node, the channel doping concentration is increased. This high doping level induces threshold voltage variation and the generation current increase at the source/drain terminals affects the "0" retention time. On the other hand, 1T-Bulk memories seem to be compatible with eDRAM applications until 45 nm node according to ITRS 2003. Beyond this node, innovative solutions are needed to ensure the 1T-DRAM concept continuity. In the following, we describe the benefits of 1T-DRAM devices in Fully Depleted SOI (FDSOI) technology and how they operate.

1.6.4. 1T-DRAM in Fully Depleted Silicon on Insulator (FDSOI) Technology

1.6.4.1. Motivations

Short-channel effects (SCE) appear in Bulk and PD devices when they are scaled down beyond 45 nm node which affects their operation as dynamic memories. In particular, the control of "0" state, especially in holding mode, becomes impossible. Doping the channel with high concentrations increases the leakage current of junctions [100] which affects the "0" state retention time. By way of explanation, previous technologies cannot ensure anymore the continuity of capacitor-less DRAM keeping a remarkable current margin and high retention time. For this purpose, developing innovative architectures with thin silicon film is a must. In fact, SOI transistors with Fully Depleted body (FDSOI) attract much attention due to their numerous advantages [101]: better electrostatic control, steeper subthreshold slope and higher saturation current. In this context, researchers and industrial companies decided to test FDSOI transistors with thin silicon film as 1T-DRAM, believing that one day they will be fully compatible with CMOS logic transistors fabrication. The operation principle of FDSOI transistors and the memory variants are investigated in the next paragraph.

1.6.4.2. Operation Principle and 1T-FDSOI Memory Variants

Compared to PDSOI dynamic memories, operating with one single front gate and grounded back gate, FDSOI devices need back-gate biasing to perform as 1T-DRAMs. In fact, the potential distribution in a thin silicon film is completely different from that in partially depleted body. The source/substrate barrier is high enough allowing the accumulation of holes in the substrate where the potential-well is quite deep. This barrier is reduced in FDSOI technology due to the strong coupling effect between the front and the back gates. Here, holes are evacuated into the source instead of being accumulated in the transistor body. Nonetheless, floating-body effects, in particular the Kink, appear again in FDSOI transistors when the back gate is negatively biased. Holes can accumulate in the silicon film inducing a front-channel threshold voltage reduction and drain current increase which is also the origin of Kink effect.

In 2004, first FDSOI memories without capacitance appear with two different silicon film thickness (16 nm by STMicroelectronics [102] and 55 nm by Toshiba [103]). Few years later, other

variants such as double-gate 1T-DRAM, floating-junction gate devices and FinFet configurations have been developed. In the following, we present the most recent capacitor-less dynamic memories in FDSOI technology featuring interesting results in terms of current margin, retention time and integration density.

a. MSDRAM

MSDRAM is a single-transistor operating as capacitor-less DRAM [104]. The operation mechanism is based on Meta Stable Dip effect (MSD) discovered in 2004 [105]. This unusual floating body effect appears in regular FDSOI transistors where the double (front and back) gates cooperate by coupling, giving rise to a hysteresis in transfer I_D-V_G characteristics, illustrated in Figure 1.30-a. State "1" features at the same time a back inverted channel ($V_{G2} > V_{th2}$) and an accumulated front interface. It is programmed by applying a high negative front gate pulse (V_{G1P} ~ - 6 V) that triggers B2B tunneling and efficiently fills the front channel with holes. State "1" is revealed by a high current flow at the back channel. Programming "0" state is obtained by deep depletion of the device, achieved by applying a less negative front-gate pulse (starting from 0 V to V_{G1P} ~ - 3 V). At this time, the device does not reach equilibrium (because there are no holes available) and the channel goes into deep depletion; hence the back channel current is temporarily suppressed. This method, called capacitive coupling (CC), exhibits better results than impact ionization or forward biased junction mode (FBJ). The current margin is enlarged and the retention time is improved, as shown in Figure 1.30-b. Another advantage of this cell is the low drain voltage in reading mode (V_D ~ 0.1-0.2 V). Reading the memory state implies a moderate front-gate pulse (- 4 V < V_{G1R} < - 2.3 V) leading to a long retention time.

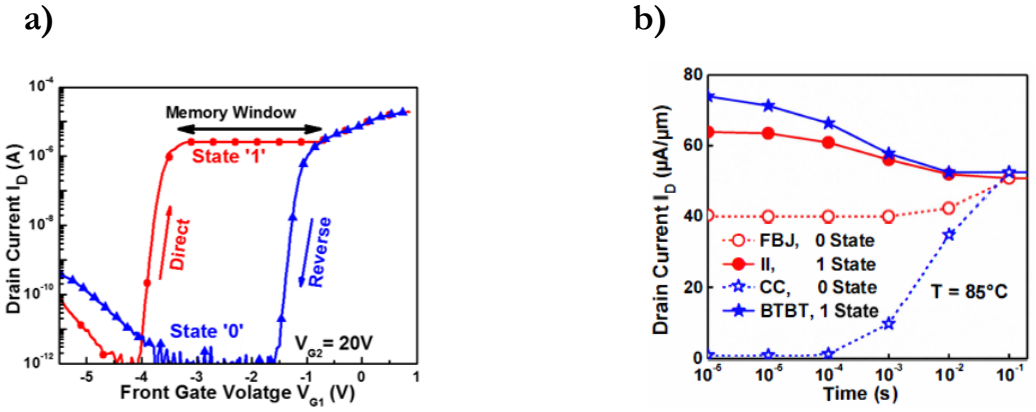

Figure 1.30. (a) Drain current I_D measurements for direct and reverse scan of front gate voltage (V_{G1}) for V_{G2} = 30 V, V_D = 0.1 V. (b) Compared conventional programming methods (Impact Ioniziation II vs B2B tunneling for state "1" and Capacitive Coupling CC vs Forward Biased drain Junction FBJ for "0" state) showing higher retention time and sensing margin I_1-I_0 for MSD methods (BTBT and CC) at 85°C. t_{BOX} = 400 nm, L_G = 1.5 µm.

2-D simulations showed that MSDRAM can be scaled down to 25-50 nm channel length with remarkable current margin and retention time at low front-gate voltage, as seen in Figure 1.31. Also, this memory cell can achieve a non-volatile function with replacing the positive back gate bias by a positive charge trapped in the BOX [106].

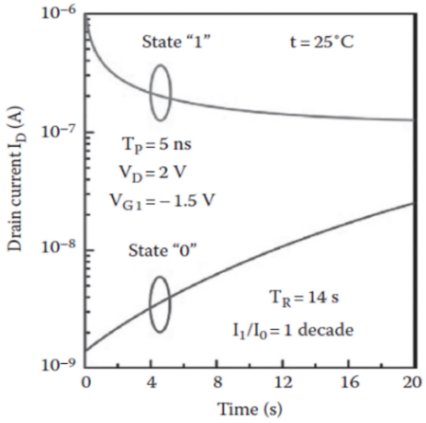

Figure 1.31. Two dimensions (2D) simulations for MSDRAM with 50 nm gate length, 40 nm silicon film thickness, 3 nm front oxide and 6 nm buried oxide. The retention time is 14 s for a marge of 1 decade between I_1 and I_0 at 25°C at low front gate voltage V_{G1} = - 1.5 V. Programming time T_P = 5 ns.

The 1T-MSDRAM is simple to program and read. It features a good current margin and high retention time. However, the memory cell suffers from super-coupling when the silicon film thickness goes into values smaller than 10 nm [107]. In fact, the coexistence of two types of carriers in the channel at the same time is not possible anymore.

b. A-RAM Family

In order to suppress the super-coupling effect and be certain of the presence of two types of carriers in transistors with t_{Si} < 10 nm, a new concept has been proposed in 2009 [108]. The Advanced RAM (ARAM) memory cell body, presented in Figure 1.32-a, is divided by a middle oxide (MOX) into two parts. The upper region is dedicated for storing majority carriers while electrons are present in the lower semi-body with the intention of current sensing. State "1" programming consists of filling the upper body part with holes using impact ionization or B2B tunneling techniques. The holes will enable, by electrostatic coupling through the MOX, an electron current flow in the sense region (lower semi-body). In contrast, when there is no charge stored above MOX, the concentration of minority carriers (electrons) in the bottom of the body is very low (due to full depletion) defining the state "0" with no current flow. Positive drain pulses are used to read the memory states. This memory cell exhibits decent retention time, low power

operation and sufficient current margin. Also, with ONO stack for the MOX the Advanced RAM could present a nonvolatile functionality [109].

Two years later, an updated version was proposed with an N^+ layer placed in the bottom of the transistor body that serves for current sensing. The middle oxide (MOX) is suppressed in this novel device, A2RAM [110] (presented in Figure 1.32-b). It features the same operating principle as MSDRAM, except that the bridge is "physical", made by epitaxy or implementation, rather than "electrostatic" induced by the back-gate. In A2RAM, the current flows through the N^+ bridge revealing the state "1". Experimental results show that this innovative memory cell features an acceptable retention time (20 ms for standard and 100 ms for optimized version at 85°C) and high current ratio I_1/I_0 [111]. The critical issue is again film thinning which makes difficult the formation of variability free N-bridge.

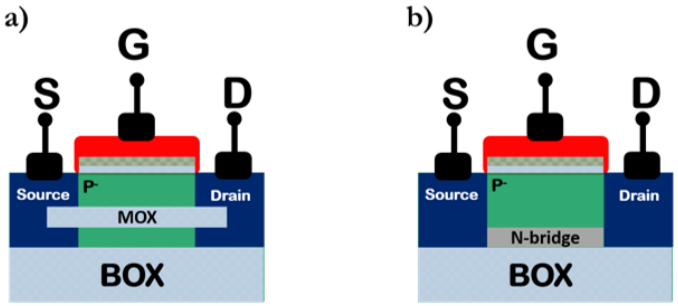

Figure 1.32. Architecture of capacitor-less DRAM in FDSOI technology: (a) ARAM with a middle oxide (MOX) and (b) A2RAM with N^+ implant in the bottom of the undoped body.

c. Z²-RAM

Fully depleted Z^2-FET transistor [48, 55], unlike MSDRAM and A2RAM, is free from super-coupling effect and technological process constraints. The device has been already presented in section 1.4.6 and will be investigated in details in the next chapter. First experiments showing the functionality of this device as 1T-DRAM have been performed on P-type Z^2FET [61, 63], schematically shown in Figure 1.33. Here the front gate, placed near the drain (N^+ doped), is negatively biased and the back-gate is positively biased. This kind of polarization emulates a virtual NPNP thyristor blocking the current flow. Increasing the drain current to a value higher that V_{ON} (ON voltage) will trigger the feedback mechanism between barriers controlled by the two gates and sharp switch is obtained. Therefore, a high current circulates through the device. The memory programming relies on the presence (state "1") or not (state "0") of holes stored under the gate. The discharged gate capacitor during reading state "1" with a negative drain pulse unblocks the

device giving rise to a high current I_1 as seen in Figure 1.33. Nevertheless, in "0" state, Z^2-RAM remains blocked with no current flow because there is no charge under the gate. The key feature of this memory cell is that the operation principle does not rely on the number of holes stored under the gate but on the discharge current $\Delta Q/\Delta t$ (higher current collected with fast reading).

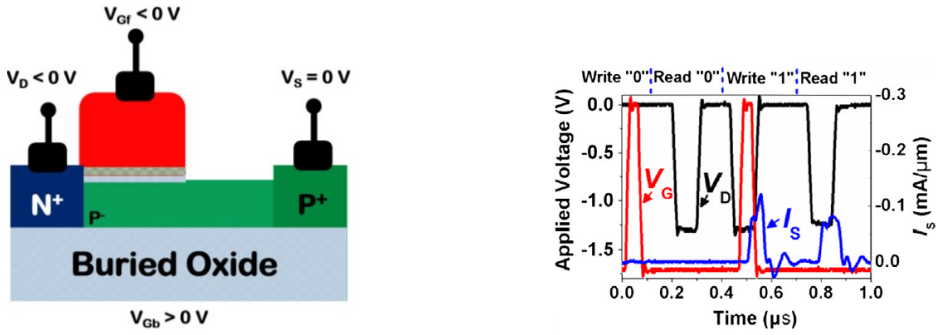

Figure 1.33. Schematic cross section of Z^2-FET P-type transistor and experimental results for Z^2-FET operating as 1T-DRAM showing high I_1 current (~ 90 µA) and negligible "0" state current. t_{Si} = 20 nm, t_{BOX} = 140 nm, L_G = 400 nm and ungated part L_{IN} = 500 nm. (From J. Wan et al. [61]).

2D simulations show the feasibility of scaling Z^2-FET down to 40 nm gate length keeping long retention time and remarkable current ratio [62]. Further, experimental results showing the perfect characteristics of this novel device as a 1T-DRAM operating in a low voltage range (~ 1 V) in most advanced FDSOI technology (14 nm and 28 nm nodes) are presented in Chapter 4.

d. Unified RAM

Assigning multifunction tasks to a transistor is an alternative solution when there is no more possibility to scale it down. The Unified memory, in planar SOI [112] (Figure 1.34-a) or FinFET [113] (Figure 1.34-b) architectures, tends to combine the functionalities of nonvolatile memory (NVM) together with the volatile DRAM in a single device. This can be achieved by introducing new materials, such as nanocrystals or ONO stack, into the gate stack serving as an electron trapped zone for NVM operation. The body is used for storing holes ensuring 1T-DRAM mechanism. The NVM program/erase (P/E) mode can be carried out by either Fowler-Nordheim (FN) tunneling or channel hot-electron injection. For dynamic operation, an excess of holes are stored in the body region (state "1") using impact ionization or GIDL techniques, while "0" state consists of deriving holes into the drain/source by forward biasing the junctions.

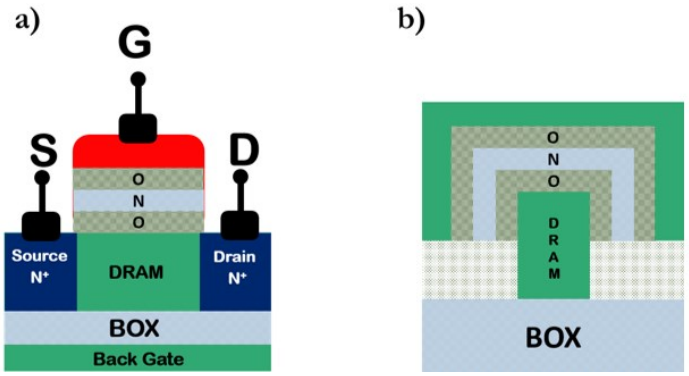

Figure 1.34. Architectures of unified memory combining nonvolatile functionality, using ONO stack, with the volatile function of 1T-DRAM in (a) double-gate planar MOSFET with ONO gate and (b) FinFET with surrounded gate all around the silicon film and ONO stack.

Preliminary results in different technologies [108, 109] demonstrate the concept of URAM memory with the possibility of storing multiple bits using MDC method [115] . However, the programming voltage of 1T-DRAM operation can affect the trapped charges in ONO layer and induce an undesired threshold voltage shift. In order to avoid this interference, gate-to-source nonoverlap structures have been proposed [116] and an alternative 1T-DRAM programming method is adopted [117]. A different solution consists of employing ONO materials as BOX where the buried nitride layer is used for NVM charge storing [118] and the silicon body for dynamic memory mode. It has been demonstrated that the memory effect depends not only on the front-gate, back-gate and drain polarizations but on device geometry also. In shorter devices, the memory margin is extended [118]. The proposed FinFlash with buried storage ONO layer can serve for analog, logic or memory applications performed with the same cell.

1.7. Conclusion

In this first chapter, the history of MOSFET transistor in bulk technology was discussed, showing the need of migration into UTBB FDSOI technology in case of aggressive downscaling. We have tried to review the most important sharp-switching devices, showing the possibility of breaking the famous 60 mV/decade subthreshold slope of MOS transistor. Within this first chapter, it has been shown that band-modulation devices present superior performance with a very sharp switch. These devices can be used for many applications such as electrostatic discharge protection, sensing, logic switch and 1T-DRAM memories. We have focused on two applications: Electrostatic discharge protection and capacitor-less dynamic random access memories. A survey of different 1T-DRAM variants in different technology has been carried out. In the next chapter, the detailed description and operation principle of our band-modulation devices will be addressed.

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Chapter 2. Band-Modulation Devices: Fabrication Process and Operation Principle

SUMMARY

2.1. Introduction

In this chapter, different variants of band-modulation devices are presented: Z^2-FET, Z^2-FET DGP and Z^3-FET. They are fabricated with the most advanced UTBB FDSOI technology in 14 nm and 28 nm nodes. The operation principle, relying on the modulation of electrons and holes injection barriers, is demonstrated with TCAD simulations. Sharp switch characteristics of all variants such as adjustable triggering voltage V_{ON}, high current ratio I_{ON}/I_{OFF}, low leakage current I_{OFF} and large hysteresis are confirmed with experimental results. In addition, the benefit of implementing an additional N-type ground plane (GP-N) underneath the gate of standard Z^2-FET or removing completely the front-gate and operating with only ground planes (N and P) acting as back-gates are highlighted.

2.2. Zero Subthreshold Slope and Zero Impact Ionization FET: Standard Z^2-FET

2.2.1. Device Fabrication

2.2.1.1. 28 nm FDSOI Technology

Recently proposed in [1–6] as capacitor-less dynamic memory (1T-DRAM) and developed as a local electrostatic discharge (ESD) protection in [7–10], the standard Z^2-FET features notable performance. Figure 2.1 shows the device structure in 28 nm FDSOI node [11, 12]. The fabrication process of Z^2-FET starts with delimiting the device surface using STI isolation. The 25 nm BOX separates the undoped ultra-thin silicon film (t_{Si} = 7 nm with ~ 10^{16} cm^{-3} doping concentration) from a highly P-type doped ground plane (~ 10^{18} cm^{-3}) that prevents the deep depletion of the substrate and acts as a back-gate. In order to access the GP and control the well potential, the BOX is locally etched. Unlike FED that controls the channel with two adjacent front-gates ([13–15], see Figure 2.11 for comparison) , the undoped Si film of Z^2-FET is partially covered by a single high-k metal front-gate (L_n part, gate length) whereas the rest of the channel is ungated (L_p part, intrinsic part length). The gate stack starts with a thermally grown oxide interface (SiO_2) ensuring a good interface quality clean of fixed charges. The interface SiO_2 layer (IL) is covered by high-k hafnium dioxide layer (HfO_2, 18 < k < 20) improving the drive current and reducing the gate leakage. It is connected via a mid-gap metal layer (TiN or AlTiN) with a low resistance Poly-Si electrode followed by gate patterning and offset spacer formation. After the second spacer realization, the anode and the cathode are implanted (P^+ and N^+ with 10^{20} cm^{-3}, respectively).

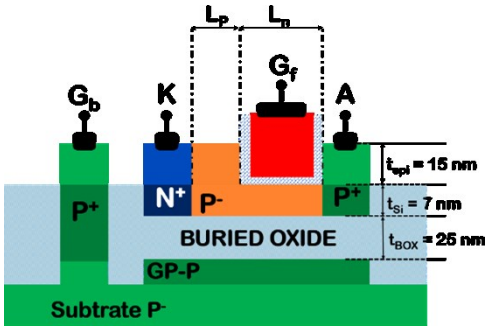

Figure 2.1. Cross-section view of standard Z^2-FET in 28 nm FDSOI technology featuring undoped ultra-thin silicon film (t_{Si} = 7 nm), very thin buried oxide (t_{BOX} = 25 nm) and epitaxial layer reducing series resistance (t_{epi} = 15 nm).

Standard Z^2-FET is fully compatible with CMOS FDSOI technology process integration without any modification. However, the 28 nm node imposes an epitaxial layer (t_{epi} = 15 nm) on the whole structure to reduce series resistance [16]. This process step induces a non-uniform silicon channel thickness. Hence, the ungated part length (L_p) of the channel is 22 nm instead of 7 nm for gated part, L_n. A final step, before contact realization, consists of protecting the intrinsic part (L_p) from silicidation by covering it with an oxide layer (RPO).

2.2.1.2. 14 nm FDSOI Technology

Z^2-FET transistor was also designed and fabricated in 14 nm FDSOI technology [17]. Both advanced nodes (14 and 28 nm) feature promising characteristics. However, the fabrication process of 14FDSOI is a little different. For an enhanced electrostatic control, the silicon film channel and BOX thicknesses are reduced down to 6 nm and 20 nm, respectively, as shown in Figure 2.2-a. Contrary to 28 nm node, a dual in-situ doped Si:CP/SiGeB epitaxy is only realized on the source/drain area. An oxide protection layer is deposited on the uncovered part of the channel to avoid silicidation during contacts realization. In this region, the silicon thickness is slightly reduced because of successive process steps (deposit and etching). Moreover, the source/drain contacts, in 14 nm node, take the form of trenches authorizing more integration density with local interconnections between devices without resorting to the first metal level. In order to study the impact of silicon film thickness, another variant was fabricated with t_{Si} = 12 nm (Figure 2.2-b).

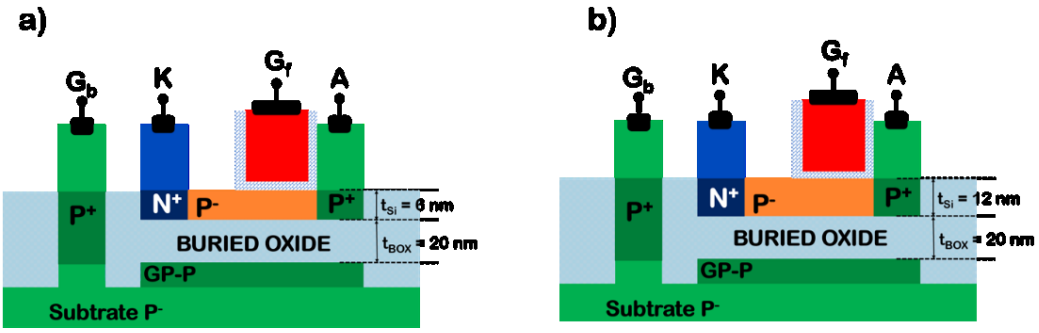

Figure 2.2. Schematic cross-section view of Z^2-FET in 14 nm FDSOI technology with (a) t_{Si} = 6 nm and (b) t_{Si} = 12 nm. The buried oxide is reduced for better electrostatic control (t_{BOX} = 20 nm).

2.2.2. Principle of Operation

2.2.2.1. Switch ON Characteristics

The Z^2-FET is a P-I-N diode operating in forward mode. When the front and back gates are grounded, the device behaves as a regular forward-biased diode with a high current flow as observed in Figure 2.3. Indeed, with this normal characteristic, the device cannot be used for applications where the sharp switch is a must.

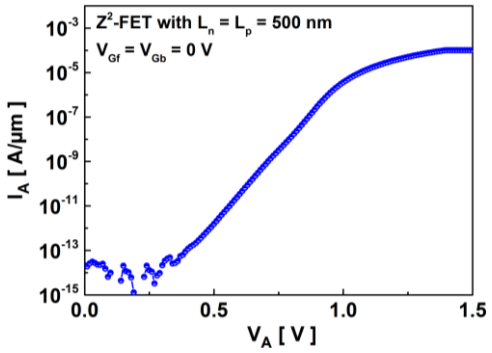

Figure 2.3. I_A-V_A characteristics for standard 28FDSOI Z^2-FET with $L_p = L_n = 500$ nm operating as a regular forward-biased diode with no gate polarization.

To get a steep switch, the structure must be blocked by biasing the two gates. Thus, a positive voltage is applied to the front-gate (V_{Gf}) creating a barrier of electrons in L_n region that prevents the path of holes from the anode into the channel. Simultaneously, a barrier of holes is formed in the Z^2-FET ungated part by applying a negative back-gate bias, thus preventing the injection of electrons from the cathode into the channel. Thereby, a virtual $N^+/P/N/P^+$ structure composed of three junctions is formed where the central P/N junction is realized by electrostatic doping. Two-dimensional simulations indicate that the impact ionization is not a factor of device triggering [1]. Conversely, the operation mechanism of standard Z^2-FET is based on bands modulation. This mechanism is confirmed by TCAD simulations [18] presented in Figure 2.4, where the conduction and valence bands are constructed by biasing the front and back gates ($V_{Gf} = 1$ V and $V_{Gb} = -1$ V), which results in a blocked Z^2-FET structure until the anode voltage increases to trigger on the device.

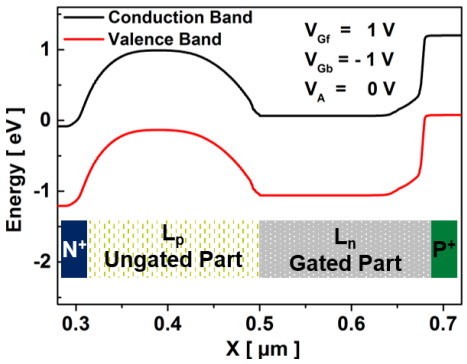

Figure 2.4. TCAD simulations showing the band-modulation mechanism and injection barriers during 28FDSOI Z^2-FET operation in OFF state (V_A = 0 V, V_{Gf} = 1 V and V_{Gb} = - 1 V). The cut is taken at y = 2 nm channel depth.

The presence of two injection barriers in the channel prevents the carrier flow. However, when V_A increases a few holes start flowing from the anode into the cathode node lowering the cathode/channel barrier. Similarly, electrons now can leave the cathode terminal to forward bias the L_n barrier and make it weaker. This is called "feedback mechanism" with a reaction loop between barriers. Once the anode voltage V_A oversteps the triggering voltage V_{ON}, the two injection barriers collapse, as illustrated in Figure 2.5-a, allowing a massive carrier flow in the channel. This action is translated into a sharp switch as seen in Figure 2.5-b. Moreover, the ON voltage (V_{ON}) depends strongly on front-gate biasing. For example, the curve with open diamond symbols (with V_{Gf} = 1.2 V), presented in Figure 2.5-b, features higher triggering voltage (V_{ON} = 1.02 V) than the curve with open squares symbols where the front-gate bias is smaller (V_{ON} = 0.84 V for V_{Gf} = 1 V). This important characteristic makes the Z^2-FET a practical device for dynamic memories, ESD protection, logic switch and other applications demanding a triggering flexibility.

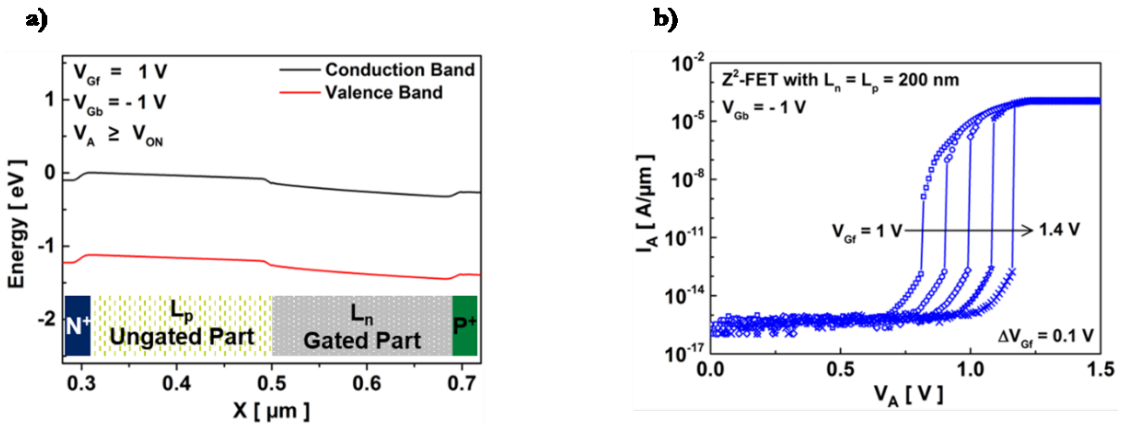

Figure 2.5. (a) Two dimensional TCAD simulations (cut at y = 2 nm channel depth) showing the collapse of injection barriers when Z^2-FET is in ON state ($V_{Gf} \geq V_{ON}$) and (b) experimental I_A-V_A results for Z^2-FET in 28 nm node at different front-gate bias with modulated sharp switch, low leakage current and high current ratio I_{ON}/I_{OFF} (> 8 decades). V_{Gb} = - 1 V.

In addition, standard Z^2-FET exhibits hysteresis that widens with front-gate voltage increase as a result of progressive shift of turn-on voltage (V_{on}) due to stronger barriers created by gates. Experimental I_A-V_A characteristics in Figure 2.5-b show that the device is in OFF state at low anode voltage V_A. It turns ON sharply when V_A reaches the triggering voltage V_{ON}. As V_A sweeps back to 0 V, the device remains in its ON state until it reaches ~ 0.7 V, at which point it turns OFF ($V_{OFF} < V_{ON}$), resulting in a large hysteresis and two stable states ("1" and "0") corresponding to high or low current levels for the same anode voltage as shown in Figure 2.6. In fact, recovering the feedback mechanism between holes and electrons injection barriers requires V_A barrier decrease. Once the gap between anode and L_n energy bands is important, the device returns into his OFF state and hence it is blocked again with low leakage current. With this feature, the standard Z^2-FET can be proposed as a capacitor-less dynamic memory 1T-DRAM. More experimental results showing the flexibility of the hysteresis depending on the polarization of front/back-gates or device geometry are investigated in the next chapter.

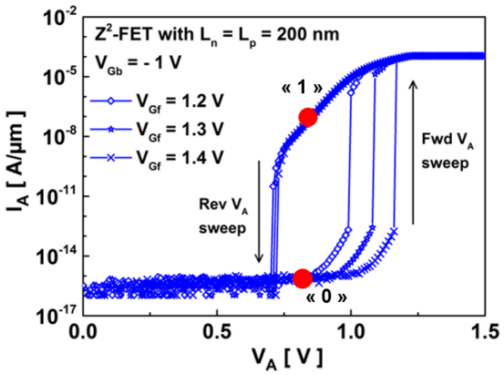

Figure 2.6. Experimental hysteresis in I_A-V_A curves of 28 nm node standard Z^2-FET with $L_n = L_p = 200$ nm for different front-gate biases V_{Gf} and V_{Gb} = - 1 V.

To explore the details of Z^2-FET operation mechanisms, two dimensional simulations were performed by employing Synopsis TCAD tools [18]. Room temperature (300 K), Fermi-Dirac statistics and standard models of doping and mobility (doping dependence, Philips unified mobility, high-field velocity saturation and transverse field dependence) were considered. Doping and temperature-dependent Shockley-Read-Hall (SRH) recombination model was also used. The simulated structure was constructed following the 28 nm fabrication process with a gate workfunction value, $WF_0 = 4.56$ eV. Fixed charge traps ($N_{hk} = 5 \times 10^{12}$ cm^{-2}) were added on the shared interface between high-k HfO_2 dielectric and the interfacial oxide layer (SiO_2) to match experimental data [19]. The maximum carrier lifetime value ($\tau_{max} = 10^{-8}$ s and 0.8×10^{-8} s for electrons and holes, respectively) is a critical factor that affects the device behavior as shown in the following.

Two simulation approaches were carried out, first, by very slow current ramping using a current source, second, by fast front/back gates voltage ramping followed by very slow raised anode voltage V_A. The characteristics collected by increasing the anode current take the form of "S-shape" snapback curves, as shown in Figure 2.7-a. Reducing the voltage while the current increases is not supported yet in TCAD tools. For this purpose, the S-shape is not present in I_A-V_A curves obtained with voltage ramping, as plotted in Figure 2.7-b.

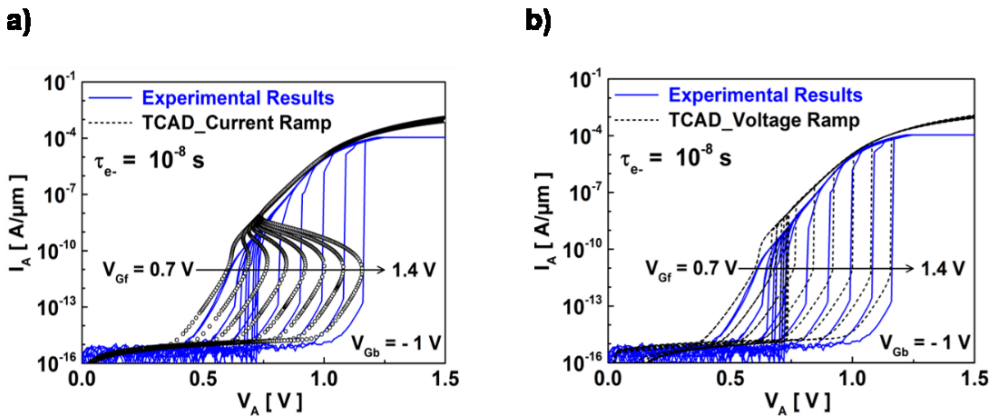

Figure 2.7. Simulated I_A-V_A curves for standard Z^2-FET fitting experimental results obtained in 28 nm node for various V_{Gf} and V_{Gb} = - 1 V with (a) current ramping and (b) voltage ramping. $L_p = L_n$ = 200 nm.

An important aspect was taken into consideration while doing voltage ramp simulations. In order to obtain similar I_A-V_A experimental curves, the inversion charge stored under the gate, as a result of applied gate voltage, must reach steady state before increasing the anode voltage. Figure 2.8-a shows the voltage pattern applied to Z^2-FET terminals. Very fast front and back gates voltage biases were enforced for 100 s with 10 ns rise time. To avoid convergence failure, a slow forward anode voltage V_A sweep was applied. It starts increasing after 1 s from V_{Gf} and V_{Gb} pulses and decreases after 50 s reproducing the same hysteresis obtained experimentally. As shown in Figure 2.8-c and d, electrons and holes densities (extracted before V_A pulse) start increasing under the front-gate and in the ungated part of the channel, respectively, and saturate after ~ 500 ms (gray short dots). When the electron concentration in the gated region reaches ~ 10^{19} cm^{-3} (Figure 2.8-c), the surface potential goes from depletion into inversion regime (Figure 2.8-b). Similar for L_p channel part, holes density increases due to the negative back-gate bias (V_{Gb} = - 1 V) to reach its maximum value at the same time as electrons. This imposes a surface potential accumulation mode as seen in Figure 2.8-b. Now, the barriers are constructed and the device is blocked, waiting for anode voltage to increase and collapse the barriers (as seen in Figure 2.5-a) leading to a modulated sharp switch with front/back gates bias variation, as plotted in Figure 2.7.

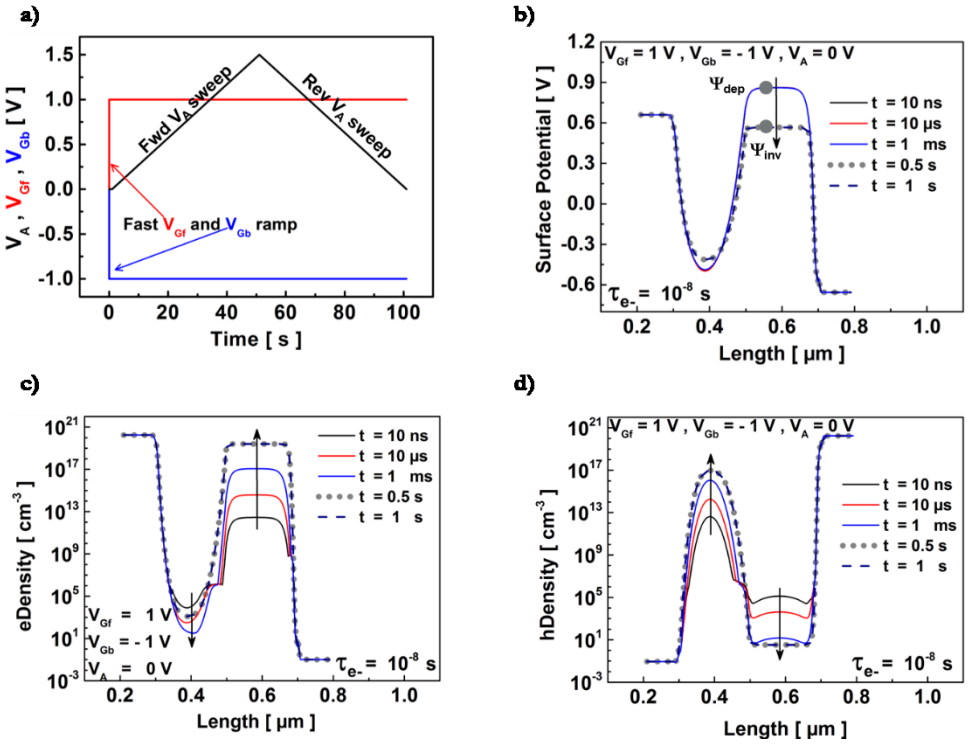

Figure 2.8. (a) Applied voltage pattern on simulated Z²-FET terminals showing fast V_{Gf} and V_{Gb} and slow V_A ramps. (b) Surface potential profile and (c, d) electron/hole densities obtained with TCAD simulations before forward V_A ramp at y = 1 nm channel depth. V_{Gf} = 1 V, V_{Gb} = - 1 V and V_A = 0 V.

Different physical mechanisms govern the Z²-FET operation. The I_A-V_A curve, reproduced in Figure 2.9, is composed of several distinct regions where each part has its own physical explanation. In OFF-state (from A to B), the barriers are constructed and the device is blocked, featuring low leakage current, which is defined by the GR (generation-recombination) current. In this region, the potential increases with V_A (inversion to depletion regime, presented in Figure 2.10-a) to reach a maximum value. After this point, the holes injection barrier is reduced allowing the diffusion of holes from anode into the channel. The flowing carriers recombine at ungated region and forward bias the cathode junction, thus reducing the barrier in the L_p part of the channel, as can be seen in Figure 2.10-b (point B to C). Now, the electrons can migrate towards the channel and get recombined at gated region and anode junction. The diffusion current prevails between B and C points giving rise to a 60 mV/decade slope. Increasing further the anode voltage triggers the positive feedback between barriers and collapses them (gray barriers in Figure 2.10-c) leading to a sharp switch (beyond C point, Figure 2.9). This steep switch is a result of non-sustainability of continuity equation between diffusion and generation-recombination currents [20] at the cathode and anode junctions. At high current state (point D), after the switch, the device behaves as a regular PIN diode with high current flow. In that position, the device goes towards double injection where the recombination of carriers dominates the conduction mechanism.

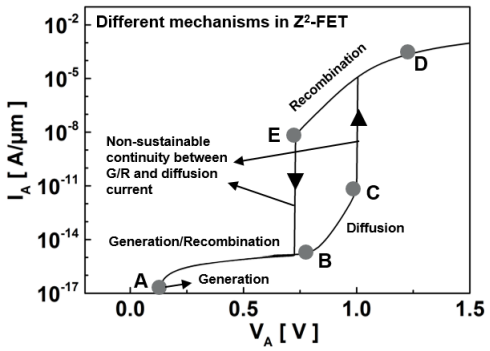

Figure 2.9. Different mechanisms in Z²-FET operation.

The injection barriers start recovering with back-sweeping the anode voltage. At point E, the device turns OFF abruptly due to the interaction between minority diffusion current and the GR current like in a thysristor [21] to return into its initial position with strong barriers as shown in Figure 2.10-d (black curve). A detailed and comprehensive model including the generation-recombination (GR) and diffusion currents for electron and holes was derived in [20]. It is based on three current continuity equations coupled to two MOS equations that define the concentration of electrons and holes in the gated and ungated regions, respectively.

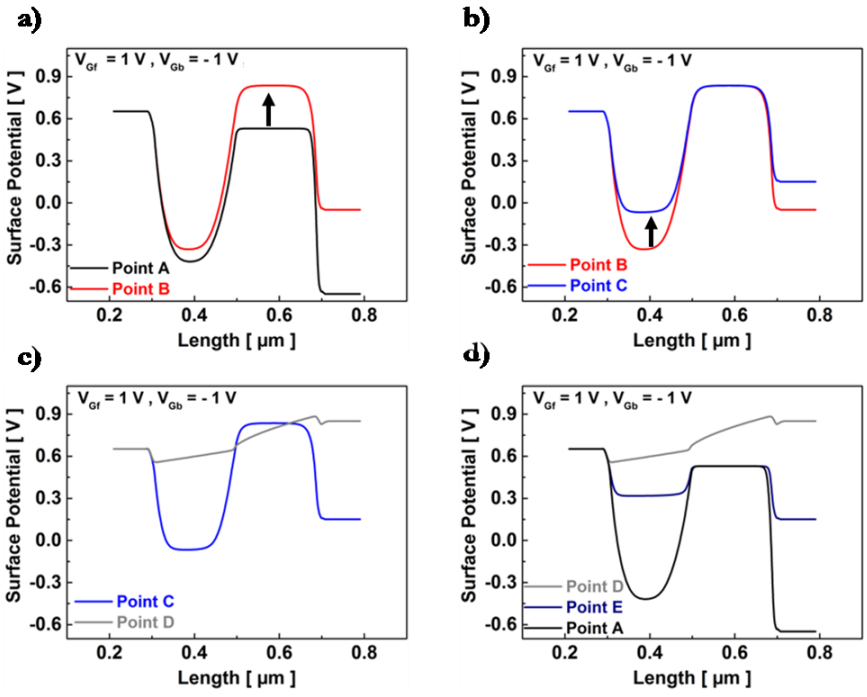

Figure 2.10. Surface potential profile resuming the different mechanisms of Z²-FET operation (Figure 2.9) starting from A to D with V_A increase and from D to A with V_A back sweep.

In ultra-thin silicon film, the carrier lifetime is degraded, which is beneficial to Z²-FET for sharp switching. Figure 2.11 shows simulated I_A-V_A curves for different carrier lifetimes (10^{-7} s to

10^{-9} s). The device parameters, such as triggering voltage V_{ON}, V_{OFF} (where the device turns OFF) and leakage current, increase with lower carrier lifetime. As mentioned before, the generation-recombination current dominates in OFF-state of Z^2-FET, and is inversely proportional to the generation lifetime. On the other hand, the diffusion current controls the 60 mV/decade region and depends on diffusion length (controlled by carrier lifetime). Both generation and recombination lifetimes rely on τ_{max}. That is why high carrier lifetime (i.e. longer diffusion length, $L_{n,\,p} \propto \tau_{eff}^2$) triggers the direct diffusion of carriers from node to node and hinder the device functionality, as shown in Figure 2.11 (red curve, $\tau_{e-} = 10^{-7}$ s). By contrast, at $\tau_{e-} = 10^{-9}$ s (black curve in Figure 2.11), most of carriers recombine in the channel and do not contribute to barriers collapse. In that case, low carrier lifetime reduces the diffusion lengths (n and p), hence the effective injection. As a result, V_{ON} increases towards higher anode voltage V_A. These simulations show that the effective lifetime in Z^2-FET should be less than 10^{-7} s, which is actually confirmed by measurements with the Hocus-Pocus diode [22].

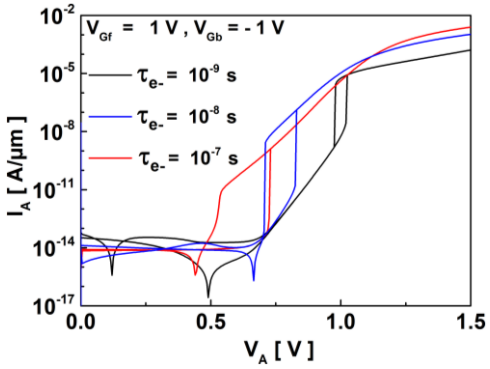

Figure 2.11. Simulated DC current versus anode voltage for 28 nm Z^2-FET SGP with different values of carrier lifetime varying from 10^{-7} s to 10^{-9} s.

Standard Z^2-FET was also fabricated and investigated experimentally in 14 nm FDSOI technology. The main characteristics such as modulated sharp switch, low leakage current and high current ratio are maintained in advanced node, as reported in Figure 2.12. The removal of the silicon epitaxy from the top of the ungated part of the channel (L_p) does not affect the device behavior.

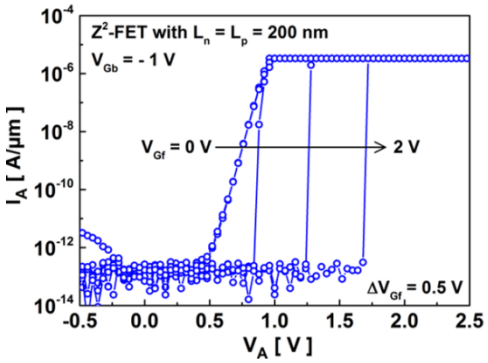

Figure 2.12. DC experimental I_A-V_A curves for Z²-FET in 14 nm FDSOI technology at different V_{Gf} values and back-gate bias V_{Gb} = - 1 V showing sharp switch on (< 1 mV/decade). L_p = L_n = 200 nm.

Similar vertical switch characteristics are shown in Figure 2.13-a. This time, toggling from OFF to ON state is obtained by back-sweeping the front-gate voltage (from 2.5 V down to – 0.5 V) for different anode polarization. As V_A increases, a higher V_{Gf} is needed to block the device. For example, the barriers collapse for V_A = 0.9 V at V_{Gf} = 0.96 V, i.e. a bit lower than V_{Gf} = 1.08 V obtained for anode bias V_A = 1 V. At high anode voltage (V_A = 1.1 V, red circle symbols) the device is in ON state with large current flow for the whole V_{Gf} scan. In that case, the important number of holes injected into the body lowers the L_n barrier beside the anode despite high front-gate voltage V_{Gf}. Hence, the barriers are already collapsed. Note that the polarization of all terminals is applied simultaneously, which explains the result obtained at V_A = 1.1 V. Also, Z²-FET SGP exhibits large hysteresis in 14 nm FDSOI, as illustrated in Figure 2.13-b, with two distinguishable states "1" and "0".

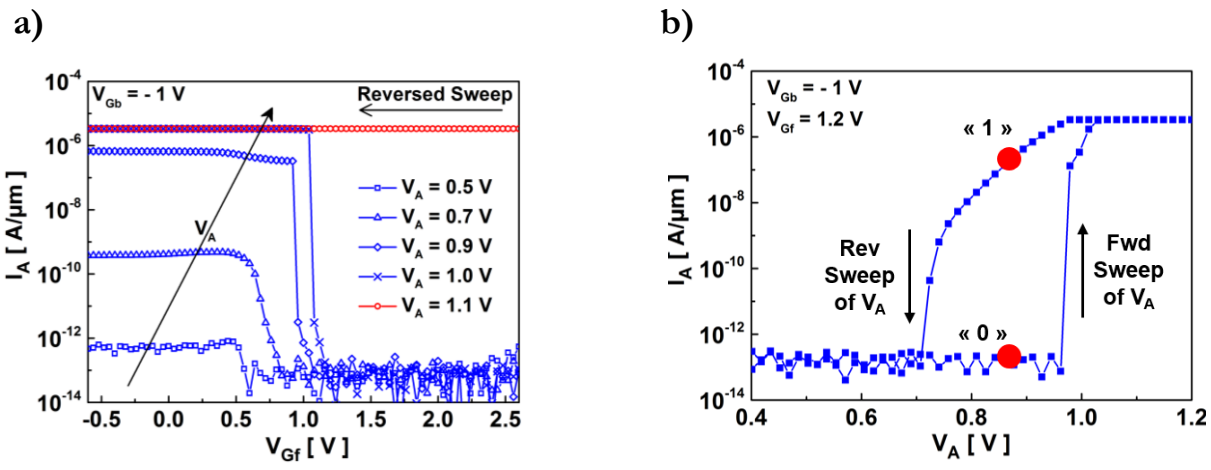

Figure 2.13. (a) I_A-V_{Gf} transfer characteristics for various anode bias V_A and V_{Gb} = - 1 V in 14FDSOI standard Z²-FET. (b) Output I_A-V_A curve showing sharp switching and gate controlled hysteresis for Z²-FET at V_{Gf} = 1.2 V and V_{Gb} = - 1 V. L_n = L_p = 200 nm.

2.2.2.2. Ground Plane Impact on Triggering Voltage V_{ON} : Coupling Effect

The P-type Ground Plane (GP-P) is present under the whole Z²-FET structure. As seen in the previous section, its main role is to create, with negative back-gate bias ($V_{Gb} < 0$ V), a barrier preventing the pass of electrons from the cathode into the channel. Regrettably, it interferes with the front-gate voltage (V_{Gf}) affecting negatively the L_n barrier and thus decreasing the triggering voltage V_{ON}. The degradation of V_{ON} for different front-gate voltages is reported in Figure 2.14. This action can be explained by the coupling effect between the front and back gates. In that case, the electrostatic control of gated region, with ultra-thin silicon film (t_{Si} = 7 nm), depends on both V_{Gb} and V_{Gf} polarizations. Thus, the GP bias increase also modifies the body potential under the front-gate and strongly affects the holes injection barrier, thus lowering the ON voltage not only for V_{Gf} = 1 V but even for higher gate bias (V_{Gf} = 1.2 V) where the L_n barrier is reinforced.

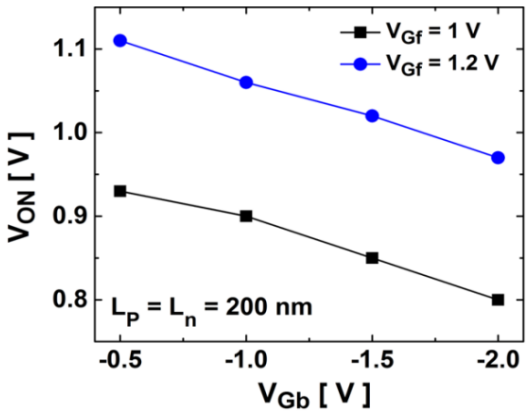

Figure 2.14. Back-gate bias influence (V_{Gb}) on the triggering voltage V_{ON} at different front-gate voltages (V_{Gf} = 1 V and 1.2 V). Z²-FET structure in 28 nm node.

This undesirable effect for some applications has been the motivation to fabricate another Z-FET version where the degradation of triggering voltage V_{ON} by V_{Gb} is suppressed. The structure of the device and its operation principle are explained in the next subsection.

2.3. Novel Band-Modulation Device with Dual Ground Planes: Z²-FET DGP

2.3.1. Device Architecture

To improve the triggering voltage V_{ON} and avoid the coupling effect between the metal gate and the ground plane acting as a back-gate, another band-modulation device was fabricated in UTBB FDSOI technology with a small modification compared to Z²-FET with single GP. The novel structure, Z²-FET DGP [23, 24], schemed in Figure 2.15 (a-28FDSOI node and b-14FDSOI node), is similar to standard Z²-FET except that an additional N-type Ground Plane (GP-N) is placed underneath the front-gate. Hence, the channel is divided into two independent parts with no bias interference. The L_n region is concealed by a single metal front-gate in 28 nm node [12] and dual workfunction HKMG in 14 nm node [17], respectively, and accompanied with N-type aligned ground plane. The ungated part of the channel is controlled by a P-type ground plane neighboring the GP-N. Both received heavily doping with 10^{18} cm^{-3} atoms concentration. Like in standard Z²-FET, the buried oxide and silicon channel thicknesses were not modified in both FDSOI technology nodes.

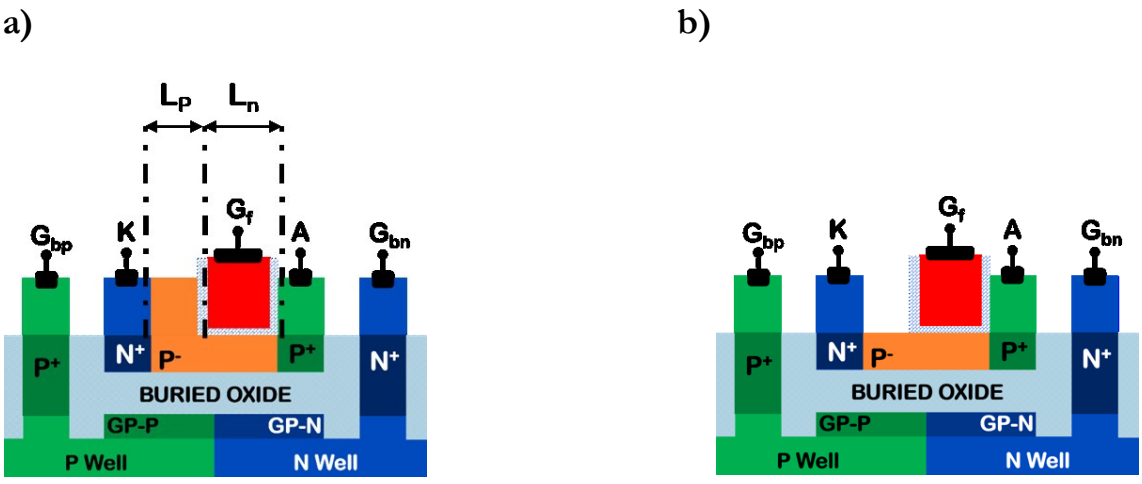

Figure 2.15. Architectures of innovative band-modulation device, Z²-FET with Dual Ground Planes in (a) 28 nm FDSOI technology featuring undoped ultra-thin silicon film t_{Si} = 7 nm, thin buried oxide t_{BOX} = 25 nm, an epitaxial layer on the whole structure t_{epi} = 15 nm and (b) 14 nm node with thinner silicon film t_{Si} = 6 nm, thinner BOX t_{BOX} = 20 nm and a dual in-situ raised source-drain.

2.3.2. Advantage of Dual GP

Adding a second N type ground plane underneath the front-gate of standard Z^2-FET does not change its fundamental operation principle: "Band-Modulation mechanism". However, the additional GP-N brings two advantages to the novel device. First, it suppresses the coupling effect, reinforces the L_n barrier and hence increases the triggering voltage V_{ON}. Second, it offers a biasing flexibility for device users, paving the way for more applications. For example, the GP-N can be biased with respect to the front-gate:

- Simultaneously, by applying the same voltage on both terminals (GP-N and front-gate). This can also be done by connecting, with a metal, the two terminals and applying just one bias on a shared pad.
- Independently, by applying a constant GP-N value and varying V_{Gf}. The inverse operation is also applicable.

Indeed, a certain limitation should be respected when applying a voltage bias to the additional N-type ground plane, since the two ground planes form a diode under the buried oxide. This diode must always be reversed biased, thus avoiding leakage current and early device triggering.

Figure 2.16-a shows the I_A-V_A curves of Z^2-FET DGP (variant with t_{Si} = 12 nm) at room temperature with a grounded GP-N (V_{GbN} = 0 V) and a negatively biased GP-P (V_{GbP} = - 2 V), providing a blocked structure. The device, with increased anode voltage V_A, features a sharp switch and adjustable triggering voltage V_{ON}. The variation of V_{ON} versus front-gate voltage is quasi-linear with $\Delta V_{ON}/\Delta V_{Gf}$ = 820 mV/V. Typical output characteristics of Z^2-FET DGP, where the GP-N is biased simultaneously with the front-gate ($V_{Gf} = V_{GbN}$) are presented in Figure 2.16-b. Here, the GP-N cooperates with the metal gate to improve the ON voltage ($\Delta V_{ON}/\Delta V_{Gf}$ = 990 mV/V). In that case, the L_n barrier is stronger and needs more anode voltage V_A to collapse. With this feature, Z^2-FET DGP can be proposed as a viable candidate for ESD protection.

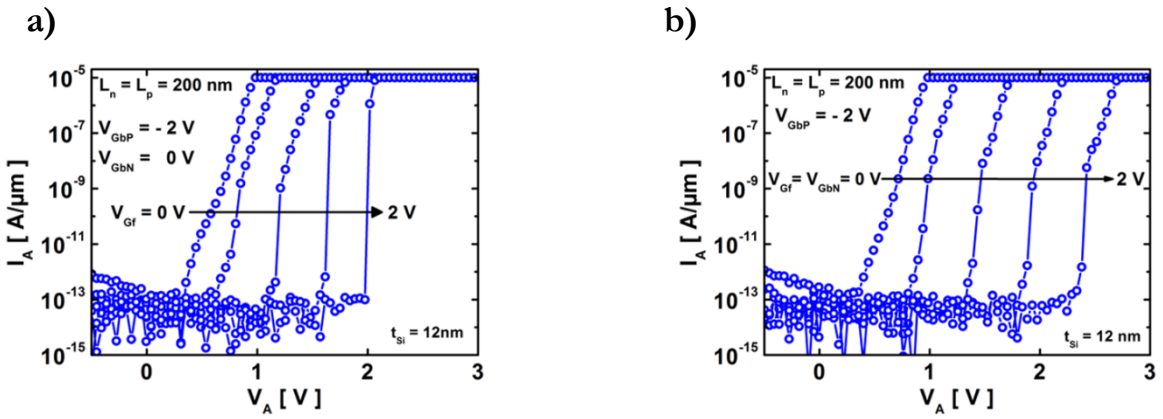

Figure 2.16. I_A-V_A output characteristics of Z²-FET DGP in 14 nm FDSOI technology at different front-gate voltages V_{Gf} biased (a) independently and (b) simultaneously with the additional N-type ground plane (GP-N).

DC experiments with reversed V_{Gf} scan were performed for the Z²-FET with dual ground planes showing similar sharp switch characteristics. Figure 2.17 shows that the structure can be blocked even at high anode voltages (V_A = 1.2 V for example). The additional N-type ground plane placed underneath the front-gate reinforces the barrier in this region and prevents the flow of holes from the anode. This result cannot be achieved in single GP Z²-FET and motivates the implementation of dual GPs.

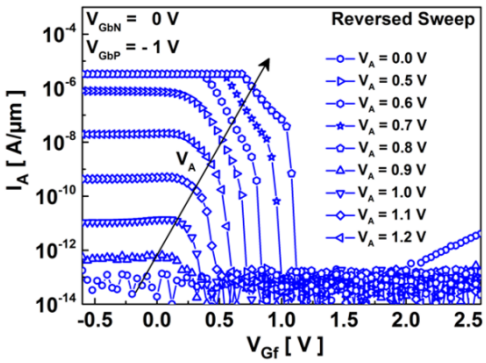

Figure 2.17. I_A-V_{Gf} transfer characteristics with V_{GbP} = - 1 V for various reversed sweep anode bias V_A in 14 nm node Z²-FET DGP with V_{GbN} = 0 V. L_p = L_n = 138 nm.

The hysteresis is also present in Z²-FET DGP. It is based on the same principle as in single GP Z²-FET with forward and reverse anode voltage V_A sweep. The two remarkable states ('1' and '0') and the large hysteresis obtained at V_{Gf} = 1.2 V, presented in Figure 2.18, were the motivation to test the device as a capacitor-less DRAM with the possibility of reducing the voltage applied to both terminals, anode and front-gate. Promising results and more detailed investigation for Z²-FET DGP used as 1T-DRAM are presented in the last chapter.

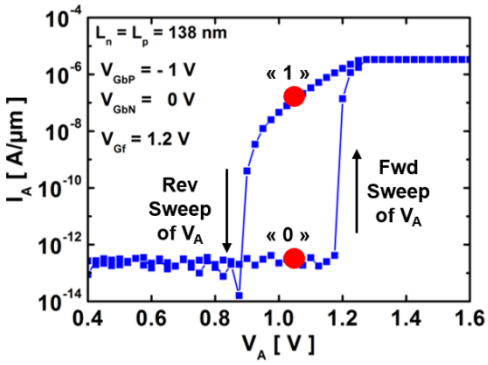

Figure 2.18. I_A-V_A curve showing large hysteresis for Z²-FET DGP with $L_n = L_p$ = 138 nm at V_{Gf} = 1.2 V, V_{GbN} = 0 V and V_{GbP} = - 1 V.

- **Complementary P-Type Z²-FET with Dual Ground Planes**

Complementary Z²-FET devices with dual ground planes, schematically shown in Figure 2.19-a, were also fabricated in 14 nm FDSOI technology. The front-gate in P-type Z²-FET DGP is placed beside the cathode (N^+ doped) and biased negatively ($V_{Gf} < 0$ V). The negatively biased P-type ground plane ($V_{GbP} \leq 0$ V) implemented below the front-gate reinforces the barrier in this region and hence increases the triggering voltage V_{ON}. Conversely, the GP-N is biased positively ($V_{GbN} \geq 0$ V) to ensure a blocked structure in the form of virtual $N^+/P/N/P^+$ thyristor. Experimental results presented in Figure 2.19-b confirm the functionality of P-type devices with typical sharp switch characteristics. Here, in order to collapse the barriers and obtain the switch slope, the cathode is increased negatively ($V_K < 0$ V). With these promising results, the Z²-FET DGP can be used to fabricate logic gates with two different device types (N and P). Additional pulsed experiments showing the possibility of Z²-FET DGP to turn OFF are discussed in Chapter 4.

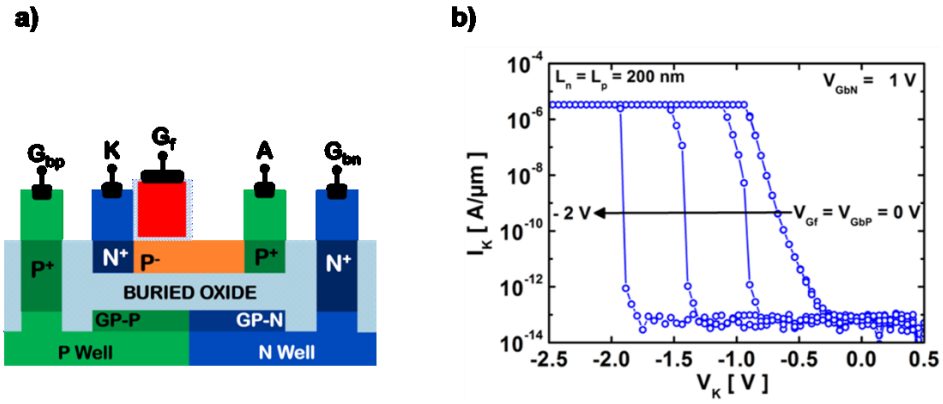

Figure 2.19. (a) Schematic cross-section for complementary P-type Z²-FET DGP in 14 nm FDSOI technology and (b) experimental I_K-V_K results at different front-gate V_{Gf} biased negatively at the same time with the P-type ground plane. V_{GbN} = 1 V.

2.4. Back-Gate Modulated Device with No Front-Gate : Z³-FET

2.4.1. Fabrication Process

The third "Z" for back-gate modulated device Z³-FET [25–27] stands for zero front-gate. Compared to other Z-FET family members, this device features similar architecture but this time without the high-k metal front-gate eliminating all issues related to high voltage reliability. Instead, an N^+ heavily doped ground plane (GP-N) was placed under the BOX controlling together with its adjacent GP-P the sharp switching characteristics. Figure 2.20 presents the architecture of no front-gate device in (a) 14 nm [17] and (b) 28 nm [12] FDSOI technologies with P^+/N^+ doped anode/cathode, respectively. The ultra-thin silicon film is still undoped and separated from ground planes (N & P) acting as back-gates by a thin buried oxide.

The free surface of Z³-FET can be functionalized for various applications like bio, light and radiation sensing. These functionalities can be combined with typical applications of band-modulation devices (memory, ESD, fast logic) leading for example to sensors with built-in memory.

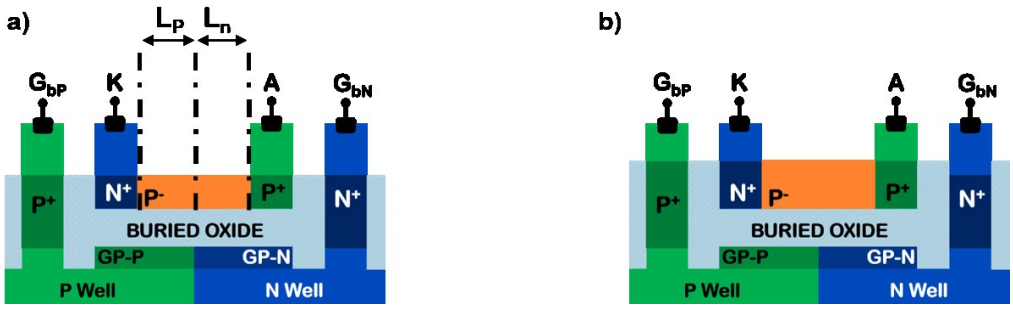

Figure 2.20. Schematic cross-section view of back-gate modulated device Z³-FET in (a) 14 nm and (b) 28 nm FDSOI technologies.

2.4.2. Advantage of No Front-Gate

This time, the sharp switching characteristics are controlled by two separated ground planes that act as back-gates. The GPs, heavily doped in order to avoid substrate/BOX interface depletion, are positively (GP-N) and negatively (GP-P) biased, respectively. The device is normally OFF thanks to potential barriers that block the injection of electrons from N^+ source and holes from P^+ drain into the body. The GbN electrode connected to the ground plane N (GP-N) controls

the electrostatic potential of the intrinsic channel part (L_n) beside the anode while the P-type ground plane connected to GbP electrode controls the L_p part of the channel beside the cathode. Increasing the anode voltage beyond V_{ON} leads to a remarkable sharp transition from low to high current with a ratio of 8 decades of I_{ON}/I_{OFF} current, as shown in Figure 2.21. The triggering voltage is of course adjustable by varying the GPs polarization. Like standard Z^2-FET and Z^2-FET with two ground planes, Z^3-FET is a practical device with easy operation. Nonetheless, one bias condition should be avoided. The diode formed by the twins GPs under the BOX should not be polarized in forward mode to avoid leakage current.

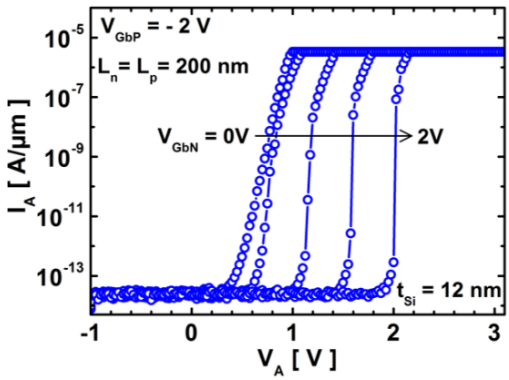

Figure 2.21. I_A-V_A curves of 14FDSOI Z^3-FET (L_p = L_n = 200 nm) at different GP-N voltage and V_{GbP} = - 2 V showing sharp switch, low leakage current and high current ratio I_{ON}/I_{OFF}. t_{Si} = 12 nm.

The Z^3-FET features similar transition from OFF to ON state with reverse V_{GbN} scan, as shown in Figure 2.22-a. Like Z^2-FET DGP and contrarily to standard Z^2-FET with a single ground plane, the back-modulated device is not annoyed by coupling effect, hence it is blocked even at high anode voltages (V_A > 1 V). As in other Z-FET family devices, the Z^3-FET needs higher GbN bias to be blocked when the anode voltage V_A increases. The flow of holes from the anode at high V_A becomes important and induces a GbN barrier lowering. Hence, a higher V_{GbN} value is needed to retrieve the barrier height and keep the device in OFF state; a higher anode bias triggers the feedback mechanism between barriers and turns ON the device.

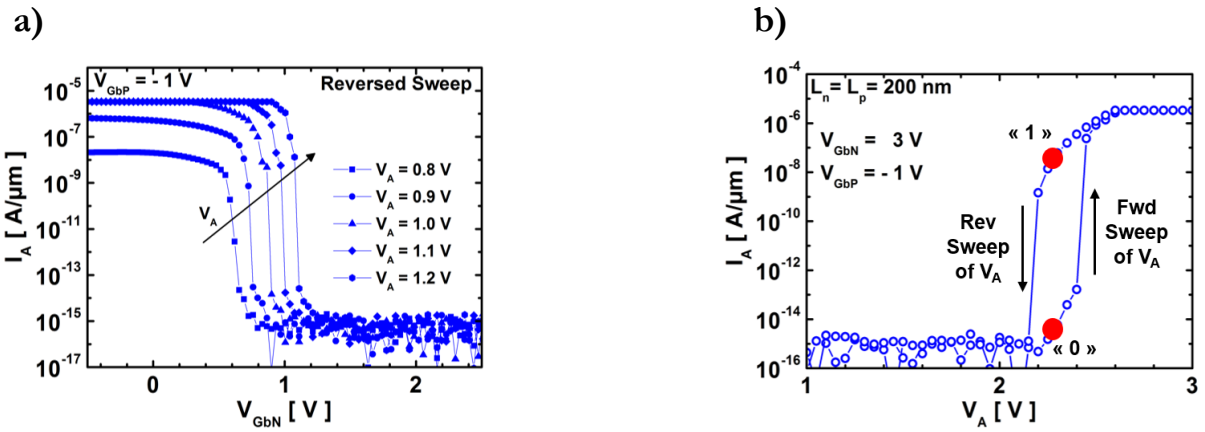

Figure 2.22. (a) I_A-V_{GbN} transfer characteristics for various anode bias V_A and V_{GbP} = - 1 V in 14FDSOI Z³-FET. (b) Output I_A-V_A curve showing sharp switching and gate controlled hysteresis for Z³-FET at V_{GbN} = 3 V and V_{Gbp} = - 1 V. L_n = L_p = 200 nm.

Hysteresis in Z³-FET device with L_p = L_n = 200 nm is obtained at high back planes bias (V_{GbN} = 3 V and V_{GbP} = - 1 V, Figure 2.22-b). Indeed, the mechanism does not change. Sweeping forward the anode voltage collapses the barriers, resulting in a sharp switch while the V_A back-sweep turns OFF the device after reaching a critical point (~ 2.2 V) where the energy bands retrieve their initial height. This point is variable in Z³-FET and depends on the ground planes biasing (it will be investigated in Chapter 3). As a result, the advantage of having a free surface on the top of the channel with a wide hysteresis effect promotes the structure to be a competitive 1T-DRAM memory coupled with novel applications like ion, bio, photo and radiation sensors.

- **High voltage operation**

Another important feature of Z³-FET, benefiting from the BOX as a gate oxide, is the ability of sustaining high back-gate bias [27]. Figure 2.23 provides output I_A-V_A characteristics for long back-gates modulated device Z³-FET with L_n = L_p = 500 nm. The GP-P is biased negatively (V_{GbP} = - 1 V) blocking the pass of electrons from the cathode into the channel while the N-type ground plane is highly biased with positive GbN voltage values up to 7 V.

As mentioned before, the carrier lifetime has an important role in Z-FET devices operation. It controls the diffusion length that should be smaller than the channel length for ensuring a sharp switch. When the carrier lifetime is degraded and lowers the diffusion rate, the carriers recombine in the channel before reaching the other node, which normally results in a steep switch. Although, the L_n and L_p regions of Z³-FET are long (1 µm, Figure 2.23), there is no sharp switch. In this case, the region dominated by the diffusion mechanism (from B to C in Figure 2.9) expands as a result

of lifetime degradation (see also Figure 2.11) inducing a non-vertical switch (SS = 60 mV/decade). Since the barriers are collapsing slowly, the high current I_{ON} is actually reached before the triggering voltage V_{ON}. Otherwise, the device exhibits a high-voltage operation without breaking down the buried diode under the BOX. This property makes the Z^3-FET a competitive candidate for HV-ESD protection or a triggering element for Bulk ESD protection devices.

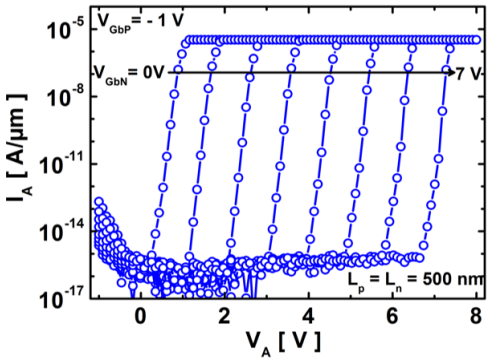

Figure 2.23. Current versus anode voltage measured for GP-N reaching high voltage in long 14FDSOI Z^3-FET with t_{Si} = 12 nm (L_p = L_n = 500 nm) without device breakdown. V_{GbP} = - 1 V.

2.5. Conclusion

In this chapter, a detailed overview of band-modulation devices fabricated with advanced FDSOI 28 nm and 14 nm technology nodes was carried out, showing their easy operation and high flexibility in terms of applications. The band-modulation mechanism and switch ON characteristics are unique for all structures (Z^2-FET, Z^2-FET DGP and Z^3-FET). They were demonstrated using 2D TCAD simulations and experimental DC results. Indeed, the standard Z^2-FET with single P-type ground plane features high performance in terms of triggering voltage, leakage current and current ratio I_{ON}/I_{OFF}. However, the back-gate (GP-P) affects the gated barrier and lowers the triggering voltage V_{ON}. This unwanted effect was solved by adding an N-type ground plane underneath the metal-front gate of standard device giving rise to a novel structure with two ground planes, Z^2-FET DGP. Finally, a third variant of Z-FET family devices featuring no metal front-gate was reported. As compared to previous architectures, the back-gate modulated Z^3-FET presents a free top surface eliminating the metal gate reliability issues and operating in a high voltage range, up to 7 V. In the next chapter, detailed experimental results (DC and TLP) in a wide temperature range of all band-modulation devices will be presented. Also, a potential distribution model of all variants will be investigated.

2.6. References

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Chapter 3. Measurement and Modeling of Z-FET Family Devices

SUMMARY

3.1. Introduction

In this chapter, DC and TLP characterizations of band-modulation devices fabricated in advanced FDSOI technologies are presented. They feature promising assets such as adjustable triggering voltage, low leakage current I_{OFF}, large hysteresis and high current ratio I_{ON}/I_{OFF}. Stacked architectures of Z-FET devices with hybrid-bulk SCR are explored showing high performance and robustness against ESD events. Analytical expressions for the potential distribution of Z^2-FET all over the channel are developed. The compact model is valid for low-doped UTBB Z^2-FET with

different geometries, and agrees well with TCAD simulation results in a wide range of front and back-gate voltages.

3.2. DC Measurements

DC measurements of all band-modulation variants (with thick gate-oxide, GO2) in 14 nm FDSOI technology were carried out at room and high temperature (T = 125 °C). Note that the maximum current reached in all figures corresponds to the anode current I_A compliance of the experimental setup and is not representative of a saturation mechanism.

3.2.1. Impact of Silicon Thickness on Z-FET Devices Behavior

The basic characteristics of Z^2-FET with two different silicon film thicknesses (6 nm and 12 nm) are illustrated in Figure 3.1 [1, 2]. The device is initially in OFF state at low V_A. Increasing the anode bias V_A lowers linearly the gate barrier (~ (V_{Gf} - V_A)) and enables the injection of few holes from the P^+ anode into the channel, which flow to the N^+ cathode inducing a potential change at cathode-channel junction. As V_A increases further towards the triggering voltage (V_{ON}), the G_b barrier is reduced sufficiently to permit electrons injection into the body and initiate a positive feedback mechanism between the barriers that sharply turns ON the device with a current I_{ON}/I_{OFF} ratio of 10^8 for $\Delta V_A < 50$ mV (Figure 3.1-b). This sharp switch is not present in Z^2-FET with thin silicon film (t_{Si} = 6 nm, Figure 3.1-a). The silicon film thinning increases the recombination rate of carriers, which is dominated by the interfaces, and decreases the effective lifetime so that the carriers cannot make the complete path from node to node. The high recombination in the body leads to non-vertical switch (SS = 60 mV/dec, Figure 3.1-a).

The switching characteristics can be improved by two methods. First, by increasing the film thickness (from 6 nm up to 12 nm in our case), the feedback mechanism between the two barriers is retrieved, producing a steep switch (SS = 5 mV/dec) as shown in Figure 3.1-b. Second, by raising the front-gate voltage up to 4 V (red curve in Figure 3.1-c); in that case the holes injection barrier is reinforced. The latter solution enables a sharp switch but increases the leakage current and can be harmful for the device because the high-k metal gate cannot sustain continuously high voltage.

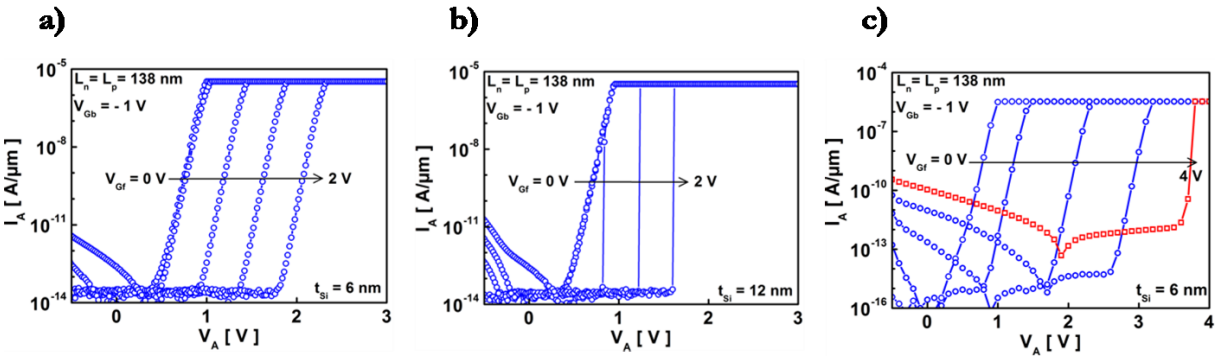

Figure 3.1. Experimental DC I_A-V_A characteristics for different front-gate V_{Gf} bias of Z^2-FETs (a, c) with thin t_{Si} = 6 nm and (b) thick t_{Si} = 12 nm. $L_n = L_p$ = 138 nm. (the mismatch of leakage current is due to equipment resolution).

The same principle is observed in other band-modulation devices. With t_{Si} = 12 nm, Z^2-FET DGP (Figure 3.2-a) and Z^3-FET (Figure 3.2-c) exhibit a modulated sharp switch while the high recombination of carriers in thin devices compromises the steepness of the switch [3–6]. The slope is degraded from 5 mV to 60 mV/decade in thin Z^2-FET DGP (Figure 3.2-b) and from 3 mV/decade to 100 mV/decade in Z^3-FET with t_{Si} = 6 nm (Figure 3.2-d). The presence of the front gate offers a better channel control, which explains the steeper slope obtained in gated Z-FET devices (Z^2-FET SGP and Z^2-FET DGP).

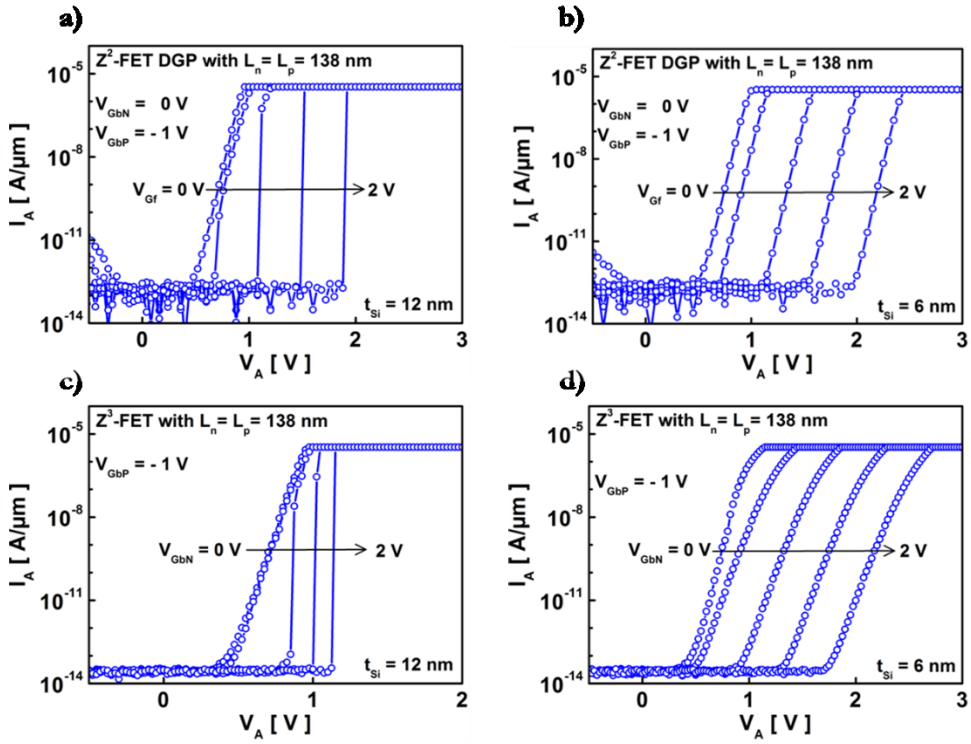

Figure 3.2. Experimental DC I_A-V_A curves of (a) thick and (b) thin Z^2-FET DGP for various V_{Gf} bias and V_{GbN} = 0 V, (c) thick and (b) thin Z^3-FET modulated by various G_{bN} and G_{bP} = - 1 V. $L_n = L_p$ = 138 nm.

3.2.2. Impact of Z-FET Devices Parameters

The characteristics of Z-FET devices, such as turn-on voltage V_{ON}, leakage current I_{Leak} and hysteresis, depend directly on barriers strength and height in the two parts of the channel. In that case, varying the terminals bias (anode, cathode, front-gate and back N-P GPs), increasing/decreasing the structure length, stressing or doping the channel affect the barriers of band-modulation devices and modify their features. In this part, a full study of these devices in different flavors and wide temperature range is given.

3.2.2.1. Front-Gate and Ground Plane (P&N) Polarizations

a. Coupling effect

In standard Z^2-FET, a single P-type ground plane is placed under the whole structure. The GP-P governs the ungated region of the device, forming the electrons injection barrier. Increasing the back-gate bias from V_{Gb} = 0 V (black square symbols in Figure 3.3-a) up to – 1 V (red circle symbols, Figure 3.3-a) makes the L_p barrier stronger, thus increases V_{ON}. The holes barrier in the gated section starts to be eroded for more negative $V_{Gb} < 0$ V, reducing the turn ON voltage due to the inner coupling between the front and the back-gate (V_{Gb} = - 2 V with blue diamond symbols in Figure 3.3-a). The ground plane extends underneath the gated region, where it tends to induce a positive charge that opposes the electron charge assigned by the front-gate V_{Gf}. This explains the non-monotonous shift of the characteristics reproduced in thin and thick Z^2-FET devices (Figure 3.3-a, c). However, increasing the front-gate voltage from 1.5 V up to 3 V strengthens enough the barrier under the gate and the coupling effect is minimized (Figure 3.3-b). The rate of triggering voltage V_{ON} change with respect to the back-gate bias is $\Delta V_{ON}/\Delta V_{Gb}$ = 120 mV/V for both thin and thick silicon films [1, 2].

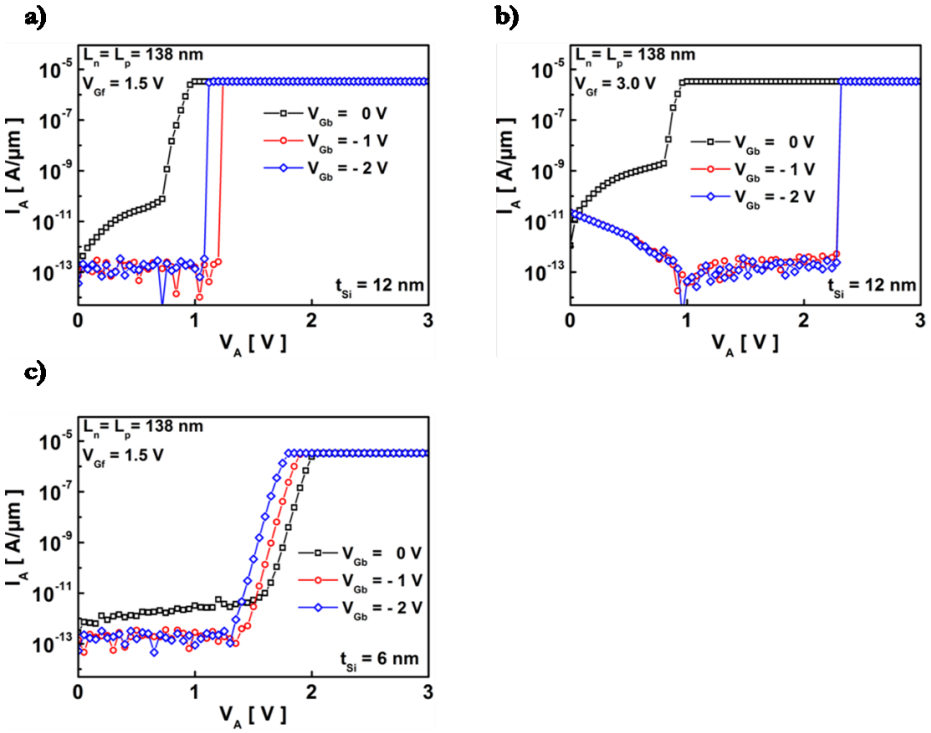

Figure 3.3. Impact of back-plane bias on the DC I_A-V_A curves at (a) V_{Gf} = 1.5 V, t_{Si} = 12 nm (b) V_{Gf} = 3 V, t_{Si} = 12 nm and (c) V_{Gf} = 1.5 V, t_{Si} = 6 nm. L_n = L_p = 138 nm.

The control of the two parts (L_n and L_p) of Z-FET devices independently suppresses the triggering voltage V_{ON} reduction. In Z^2-FET DGP, the GP-P controls only the ungated part of the channel (L_p) while the other part (L_n) is reinforced by adding a N-type ground plane underneath the front-gate. In Z^3-FET, there is no front-gate and the two parts are controlled by two buried ground planes (N and P). Thus, compared to Z^2-FET with single ground plane, the coupling effect is suppressed. Increasing negatively the GP-P in both devices, once the electron injection barrier is constructed (V_{GbP} < 0 V), does not affect the barrier beside the anode anymore, implying a stable V_{ON} as seen in Figure 3.4.

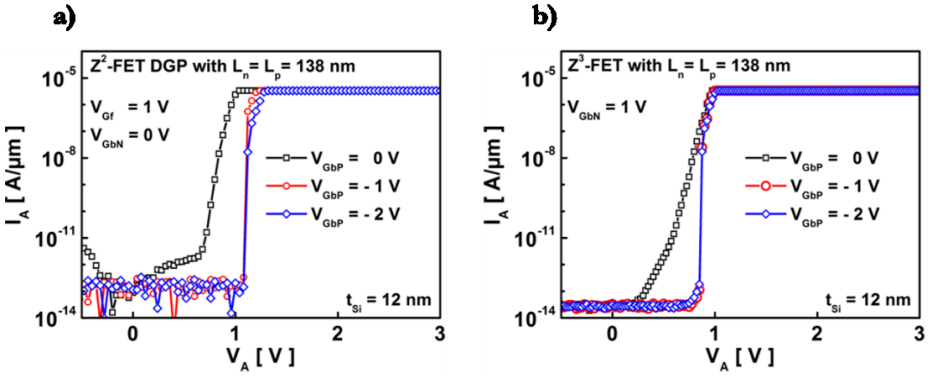

Figure 3.4. Impact of GP-P bias on DC I_A-V_A characteristics for (a) Z^2-FET DGP at V_{Gf} = 1 V, V_{GbN} = 0 V and (b) Z^3-FET at V_{GbN} = 1 V.

b. Turn-on Voltage

The device turns ON as the anode voltage V_A reaches V_{ON}. But when the front-gate voltage V_{Gf} increases, the L_n barrier is reinforced and therefore a higher V_{ON} is needed to turn the device ON. This can be seen in Figure 3.5 for both thin and thick silicon film devices. In Z^2-FET with t_{Si} = 6 nm, the ungated barrier is constructed at only V_{Gb} = 0 V (Figure 3.5-b) while in thicker devices the electrostatic control of 12 nm silicon film requires a higher back-gate bias as shown in Figure 3.5-a. However, both variants present inner coupling between the front and the back-gate. Increasing V_{Gb} induces a triggering voltage V_{ON} reduction, which starts at V_{Gb} = - 1 V in thick Z^2-FET and V_{Gb} = 0 V in thin devices.

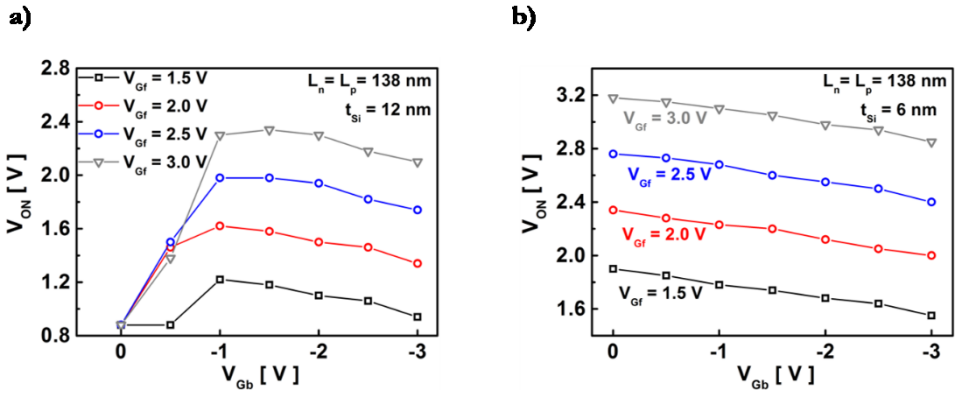

Figure 3.5. Variation of triggering voltage V_{ON} with back-gate V_{Gb} bias for (a) thick and (b) thin Z^2-FETs at different front-gate V_{Gf} polarization. $L_p = L_n$ = 138 nm.

The triggering voltage variation of thick Z^2-FET DGP and Z^3-FET with front-gate or back-gates polarizations is presented in Figure 3.6. In Z^2-FET with two ground planes, two different ways to polarize the GP-N (cooperating with the front-gate) can be used. Biasing simultaneously the N-type ground plane with the front-gate (Red circle symbols, in Figure 3.6-a) implies a higher turn-on voltage than black square symbols, where the GP-N is grounded (V_{GbN} = 0 V). The L_n barrier is more reinforced when V_{Gf} and GbN raise up together. Also, increasing the negative GP-P bias (from – 1 V up to – 2 V) strengthens the electron injection barrier, leading to higher V_{ON}, which confirms the suppression of coupling effect, as mentioned before between the GP-P and the front-gate. The evolution of turn-on voltage in Z^3-FET is analogous to other band-modulation devices, as shown in Figure 3.6-b.

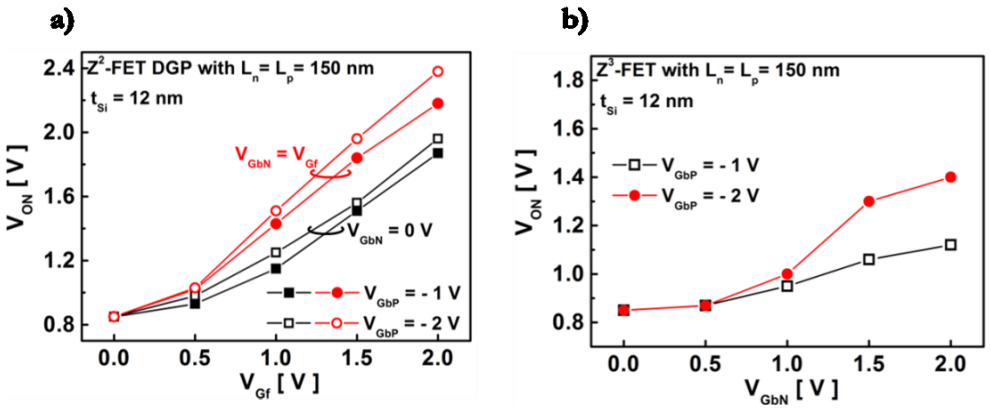

Figure 3.6. Variation of triggering voltage V_{ON} for (a) Z^2-FET DGP with V_{Gf} and N/P back-planes and (b) Z^3-FET with back-gates (GbN and GbP).

Figure 3.7 compares the triggering voltage of all Z-FET family devices. Z^3-FET features higher V_{ON} than standard Z^2-FET, while the important turn-on voltage belongs to Z^2-FET with dual ground planes. The fact of synchronizing the GP-N with the front-gate reinforces strongly the gate barrier and increases drastically V_{ON} (blue diamond symbols). With this feature, Z^2-FET DGP could be a viable candidate for ESD protection for 1.8V applications while Z^3-FET can be used for High-Voltage (HV) ESD protection, as we will see in the next subsection [6].

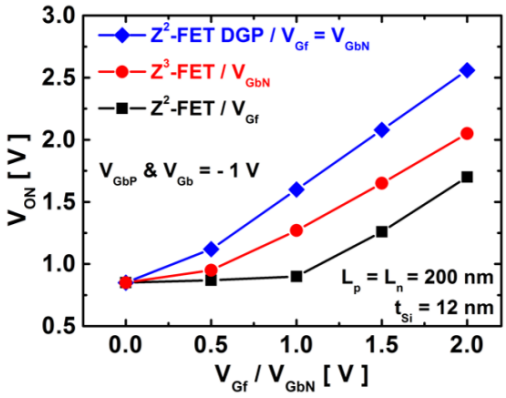

Figure 3.7. Comparison of turn-on voltage V_{ON} between Z-FET family devices with t_{Si} = 12 nm at negative GP-P bias ($V_{GbP} = V_{Gb}$ = - 1 V). $L_p = L_n$ = 200 nm.

c. High Voltage Operation in Z^3-FET Device

The advantage of modulating the triggering voltage by the ground planes enables using the Z^3-FET as a high voltage device [6]. In principle, increasing GbN requires a higher anode voltage V_A to turn ON the device but here the actual mechanism is more subtle and depends on the channel length, as shown in Figure 3.8. In short Z^3-FET, V_{ON} increases with V_{GbN} until 5 V and starts to

decrease for higher V_{GbN} (Figure 3.8-a). This means that the holes junction barrier shrinks for V_{GbN} > 5 V, which is counter-intuitive. This effect can be explained by the depletion region enlargement of the reverse-biased diode formed by the two ground planes below the BOX. The width W_{dep} of the junction depletion region is calculated for different doping concentrations in Figure 3.8-c. In our case, where the GPs are doped N_A (GP-P) = N_D (GP-N) = 10^{18} cm^{-3}, the depletion zone reaches 110 nm at $V_{GP} = V_{GbN} - V_{GbP}$ = 6 V. Thus, the electrostatic control of the channel by the GPs decreases, leading to narrower barriers and a V_{ON} reduction for V_{GP} > 5 V, as noticed in Figure 3.8-a. The channel control is retrieved by increasing the device length ($L_n + L_p >> W_{dep}$). The long Z^3-FET ($L_n = L_p$ = 500 nm, Figure 3.8-b) can sustain high anode voltage up to 8 V without device breakdown and with a negligible leakage current of the reversed biased diode. A second solution can consist in using higher doping in GPs: for $N_A = N_D = 10^{19}$ cm^{-3}, the space charge region of the diode falls down below 40 nm even at high back-gate bias (Figure 3.8-c). However, over-doping the ground planes (by ion implantation) may affect the body doping by leaving residual charges in the channel and hence the device characteristics could change.

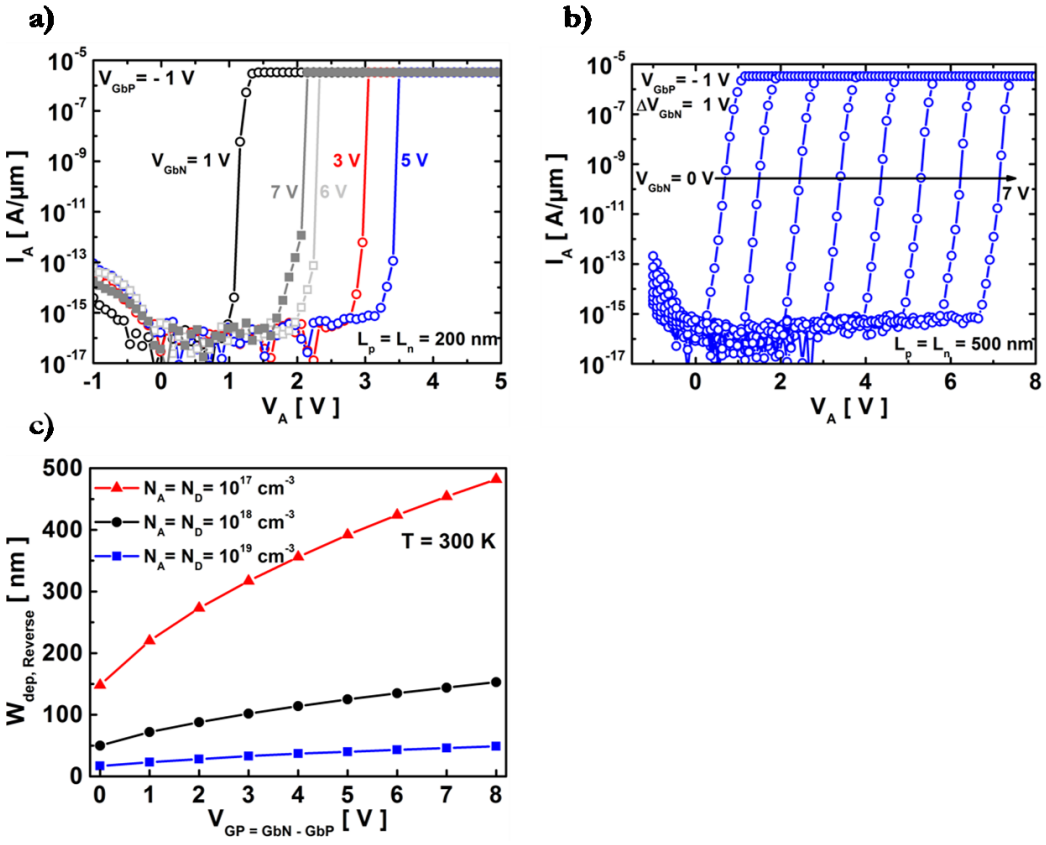

Figure 3.8. Current versus anode voltage measured for GP-N bias reaching high voltage in (a) short Z^3-FET with $L_n = L_p$ = 200 nm and (b) long Z^3-FET with $L_n = L_p$ = 500 nm at V_{GbP} = - 1 V. (c) Evolution of lateral depletion width between the GPs versus reverse bias $V_{GP} = V_{GbN} - V_{GbP}$ for different doping concentrations. t_{Si} = 12 nm.

d. Hysteresis

The output I_A-V_A curves in Figure 3.9 show that the device is in OFF state at low anode voltage V_A. It turns ON when V_A reaches the triggering voltage V_{ON} (closed symbols) and remains in ON state as V_A is swept back (open symbols) until it reaches ≅ 0.6-0.7 V, at which point it turns OFF. This results in a large hysteresis, as shown in Figure 3.9, which is gate controlled and useful for capacitor-less memory. The hysteresis is enlarged by increasing V_{Gf} (Figure 3.9-a), and can also be modified by varying the back-gate bias V_{Gb} (Figure 3.9-b). Note that the inner coupling between the GP-P and the front-gate not only affects the triggering voltage V_{ON}, but also V_{OFF}, the point where the device turns OFF. V_{ON} and V_{OFF} are reduced when the back-gate bias increases from V_{Gb} = - 1 V to – 2 V, as shown in Figure 3.9-b.

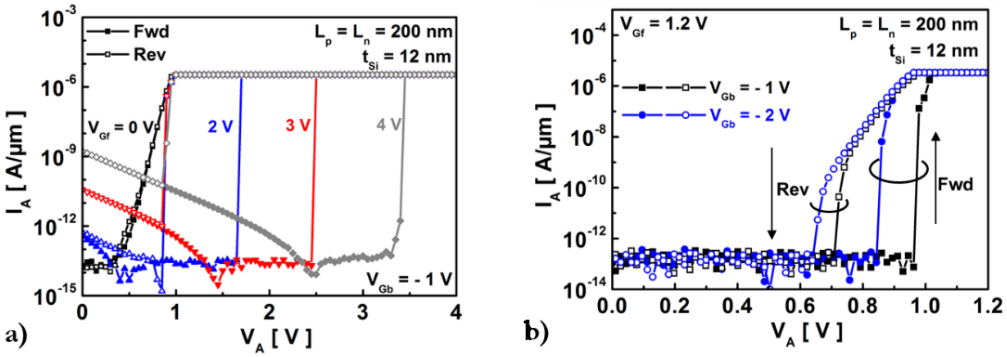

Figure 3.9. I_A-V_A curves showing sharp switching and gate controlled hysteresis for (a) various V_{Gf} at V_{Gb} = - 1 V, $L_n = L_p$ = 200 nm and (b) different back-gate bias at V_{Gf} = 1.2 V, $L_n = L_p$ = 200 nm. Thick Z^2-FETs, t_{Si} = 12 nm.

Hysteresis is confirmed in Z^2-FET DGP and Z^3-FET devices. Figure 3.10 shows that the memory window can be obtained also with I_A-V_{Gf}/V_{GbN} transfer characteristics. At V_{Gf}/V_{GbN} reverse scan (red opened symbols in Figure 3.10), Z-FET devices remain in OFF state until they reach a point where the barriers collapse, inducing a sharp switch. The turn-on operation strongly depends on the anode bias V_A that controls also the high current state (I_A current for V_A = 1 V is higher than V_A = 0.8 V). On the other hand, at V_{Gf}/V_{GbN} forward sweep (blue closed symbols in Figure 3.10), the barriers need higher V_{Gf} (for Z^2-FET DGP, Figure 3.10-a) and V_{GbN} (for Z^3-FET, Figure 3.10-b) to retrieve their height and return the device into its OFF state. The forward/reverse V_{Gf} scan results in a hysteresis that can be enlarged with anode bias V_A.

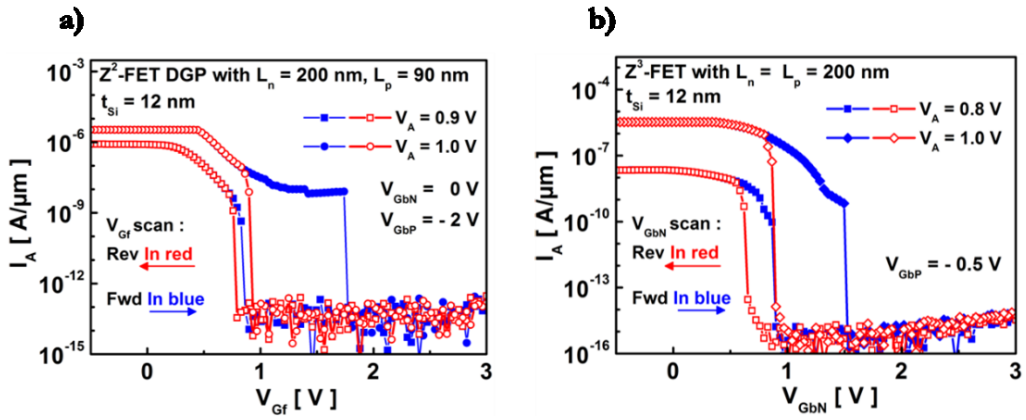

Figure 3.10. I_A-V_{Gf}/V_{GbN} transfer characteristics for various anode bias V_A in (a) Z^2-FET DGP at V_{GbN} = 0 V, V_{GbP} = - 2 V and (b) Z^3-FET at V_{GbP} = - 0.5 V showing sharp switching and hysteresis.

With these characteristics, Z-FET devices are suitable as low-power capacitor-less dynamic RAM (1T-DRAM) and fast logic switches [4, 7–9]. Transient measurements will be presented in Chapter 4.

3.2.2.2. Device Length

The scaling of the Z^2-FET strongly depends on the control of the relevant injection barriers by V_{Gf} and V_{Gb}. In short devices, the barriers are narrow, which erodes their height and need high front/back gates bias to be constructed. For example, a negative back-gate bias (V_{Gb} = - 2 V) is required to block the Z^2-FET with L_n = L_p = 90 nm (Figure 3.11-a) while longer devices feature normal switch ON characteristics with V_{Gb} = 0 V (Figure 3.11-b). Figure 3.11-a shows that, with V_{Gb} = - 2 V, the short Z^2-FET (L_n = L_p = 90 nm) is functional in 14 nm FDSOI node. Also, the sharp switch is recovered (red curve, Figure 3.11-a) by applying a relatively high front-gate bias (V_{Gf} = 3 V), which is a sound feature for area-conscious applications. Note that, in thin Z^2-FETs, the switch is not steep enough due to the weak feedback between the barriers and the high recombination rate of carriers.

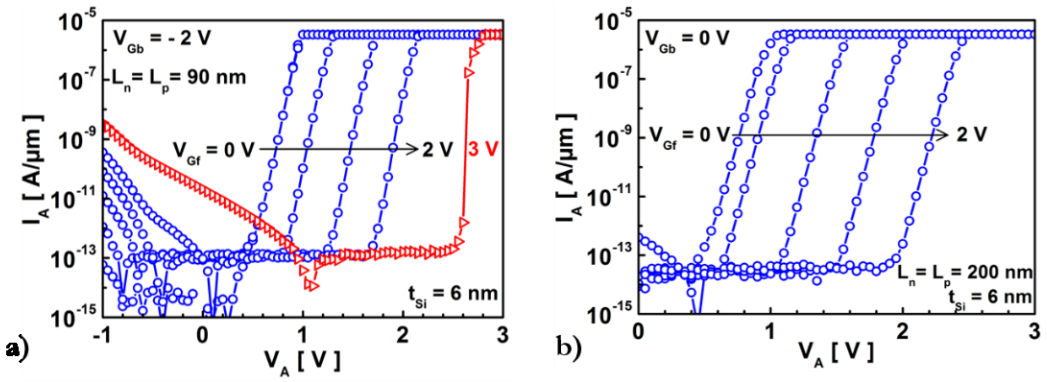

Figure 3.11. Current versus anode voltage measured for thin Z²-FETs (a) at V_{Gb} = - 2 V, $L_n = L_p$ = 90 nm and (b) V_{Gb} = 0 V, $L_n = L_p$ = 200 nm.

The dependence of leakage current, measured at V_A = 1 V, on the length of gated (L_n) and ungated (L_p) parts of the channel is shown in Figure 3.12-a and b, respectively. In short devices, the snapback is totally suppressed because the ungated region of the channel is not enough controlled by the back-gate, and the electrons injection barrier is collapsed. This is shown in Figure 3.12-a where thick devices with $L_p \leq 90$ nm operate as a forward-biased diode with high current rather than a Z²-FET, even with a reinforced electrons injection barrier at V_{Gb} = - 2 V. As L_p increases, the ungated barrier is enlarged and more efficiently controlled by V_{Gb}, therefore the leakage current is improved and the device can be blocked with low front-gate voltages. On the other hand, if the ungated barrier is strong enough (V_{Gb} = - 2 V), then the gate length L_n has no effect (Figure 3.12-b). Hence, the gate length can be scaled down to at least 90 nm without compromising the characteristics of the device.

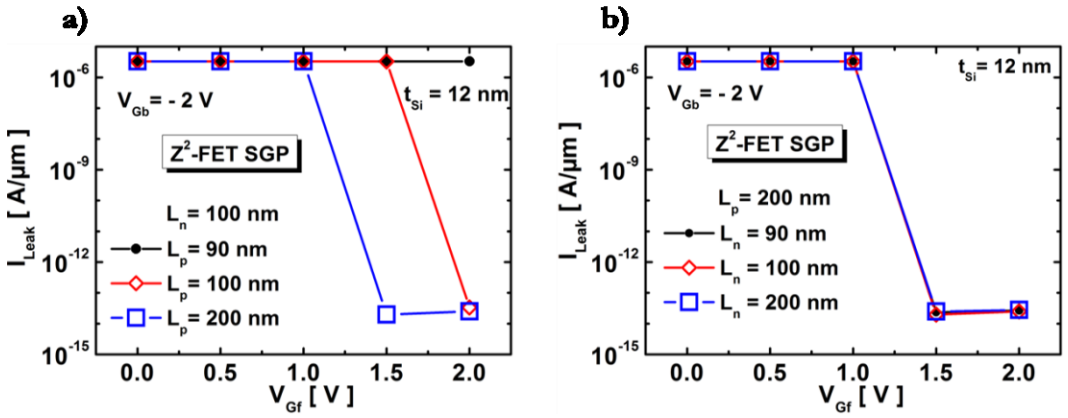

Figure 3.12. Current versus front-gate voltage measured at V_A = 1 V (where the leakage current is defined) for (a) different L_p lengths, L_n = 100 nm and (b) different L_n lengths, L_p = 200 nm. t_{Si} = 12 nm.

Like standard Z^2-FET, the electrons injection barrier in short Z^2-FET DGP ($L_n = L_p = 90$ nm) is collapsed even at high GP-P bias ($V_{GbP} = -2$ V, black circle symbols in Figure 3.13-a). The L_p barrier retrieves its height beyond 90 nm. Then, the device is blocked and the ungated length has no effect anymore on the leakage current.

The GPs lengths of Z^3-FET were restricted by minimum design rules in 14 nm FDSOI node (min $L_p = L_n = 138$ nm). However, the behavior does not change in Z^3-FET (Figure 3.13-b). The leakage current decreases with raising up GbN bias and by increasing L_p.

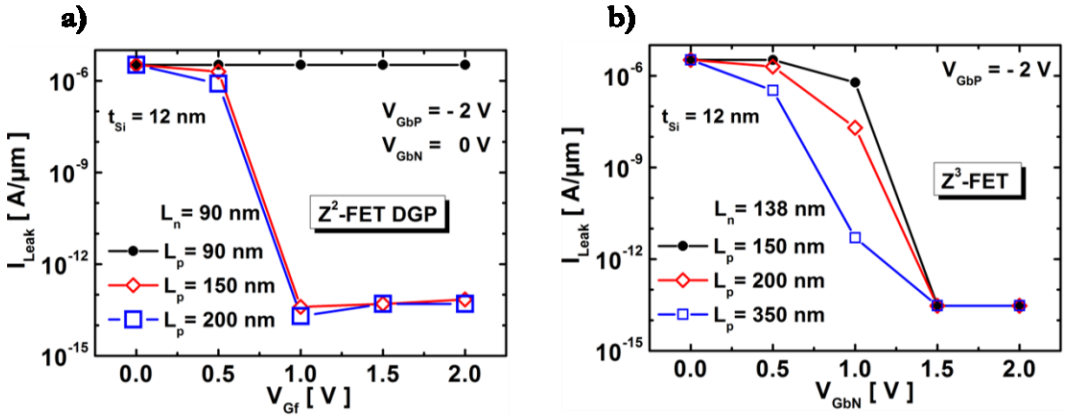

Figure 3.13. Current versus front-gate voltage measured at $V_A = 1$ V for different L_p lengths (a) Z^2-FET DGP with $L_n = 90$ nm at $V_{GbN} = 0$ V and (b) Z^3-FET with $L_n = 138$ nm. $V_{GbP} = -2$ V.

The holes injection barrier is reinforced with V_{Gf} increase and therefore triggering ON the device requires a higher V_{ON}. The channel is better controlled by V_{Gf} in long devices where the barriers are large, thus V_{ON} increases. Short devices behave as simple diodes at $V_{Gb} = 0$ V (red diamond symbols in Figure 3.14-a) with a constant turn-on voltage around 0.8 V. As V_{Gb} increases, the L_p barrier is enhanced, leading to a sharp switch even in short devices. In that case, the device length has a weak effect on V_{ON} (Figure 3.14-b). The reduction of the device length is useful for layout area efficiency. However, it is of prime importance to study the trade-off between front-gate control over V_{ON} and device scaling. Thinning the gate oxide (GO1) is also beneficial as it offers a better electrostatic control.

The impact of reducing the silicon film thickness can be seen in Figure 3.14-c where the device length has no effect on V_{ON}. The triggering voltage is reduced at $V_{Gb} = -2$ V because of the coupling effect between the front and the back gates. The evolution of V_{ON} with Z^2-FET DGP and Z^3-FET length is presented in Figure 3.14-c. Z^2-FET DGP devices exhibit higher V_{ON} than in Z^3-FET (short and long) which motivates the use of GP-N.

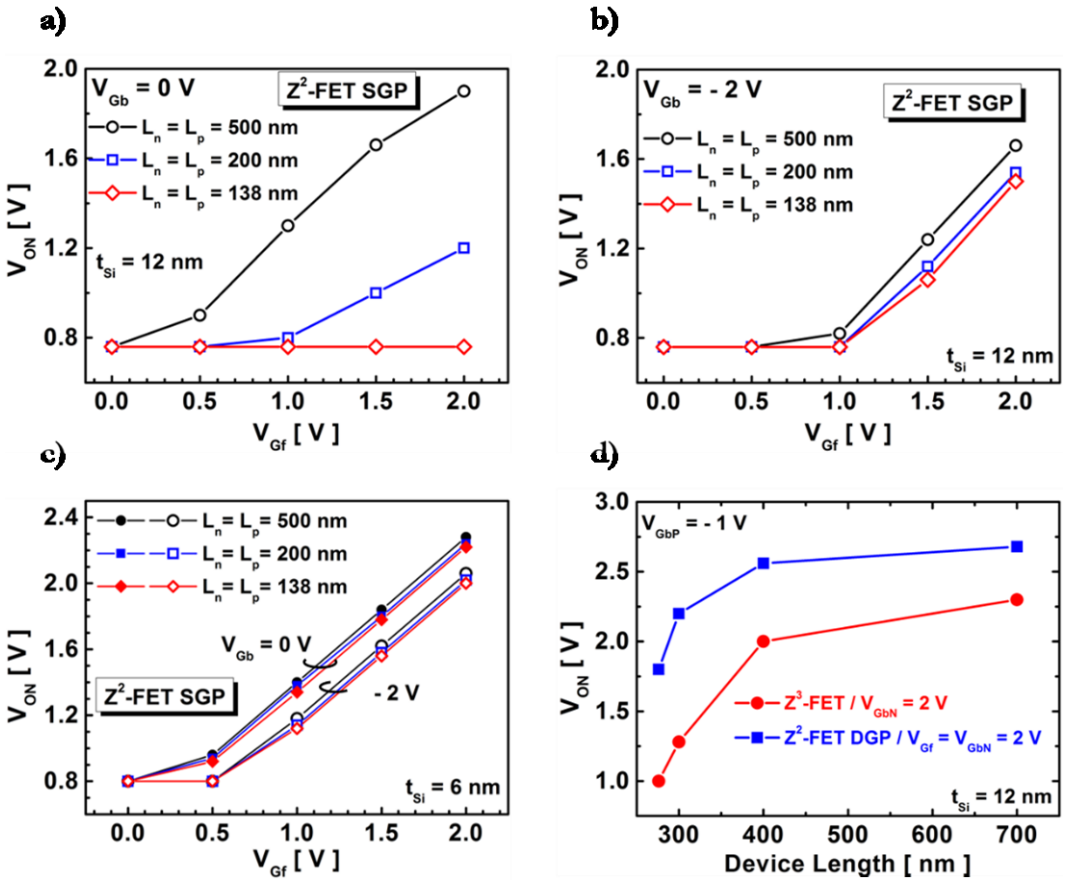

Figure 3.14. Variation of triggering voltage V_{ON} with front-gate bias for standard Z²-FET at (a) t_{Si} = 12 nm, V_{Gb} = 0 V and (b) V_{Gb} = - 2 V; (c) t_{Si} = 6 nm at V_{Gb} = 0 V and - 2 V. (d) Evolution of V_{ON} with Z²-FET DGP and Z³-FET devices length at V_{GbP} = - 1 V and V_{Gf} = V_{GbN} = 2 V.

3.2.2.3. Doping

A Z³-FET variant was fabricated with a highly doped L_n part of the channel. It is presented in Figure 3.15-a [6]. Here, the band-modulation mechanism is attenuated. The N-doped L_n region forms a natural strong barrier against holes injection, avoiding the positive GP-N bias. Hence, the device is blocked even without back-gate bias, as shown in Figure 3.15-b. In short devices, the GP-N barrier is narrow and cannot prevent completely the injection of holes toward the cathode. Since at V_{GbP} = 0 V the GP-P barrier is too weak, the leakage current is high. To avoid leakage, the electrons injection barrier should be strengthened by either increasing the length of the undoped part (Figure 3.15-b) or by negatively biasing the GP-P (Figure 3.15-d), which is efficient in both short and long devices. The triggering voltage increases not only when the barriers are broader (long device in Figure 3.15-b) or higher (V_{GbP} < 0 V in Figure 3.15-d), but also by increasing the GP-N bias (despite the high doping), as shown in Figure 3.15-c.

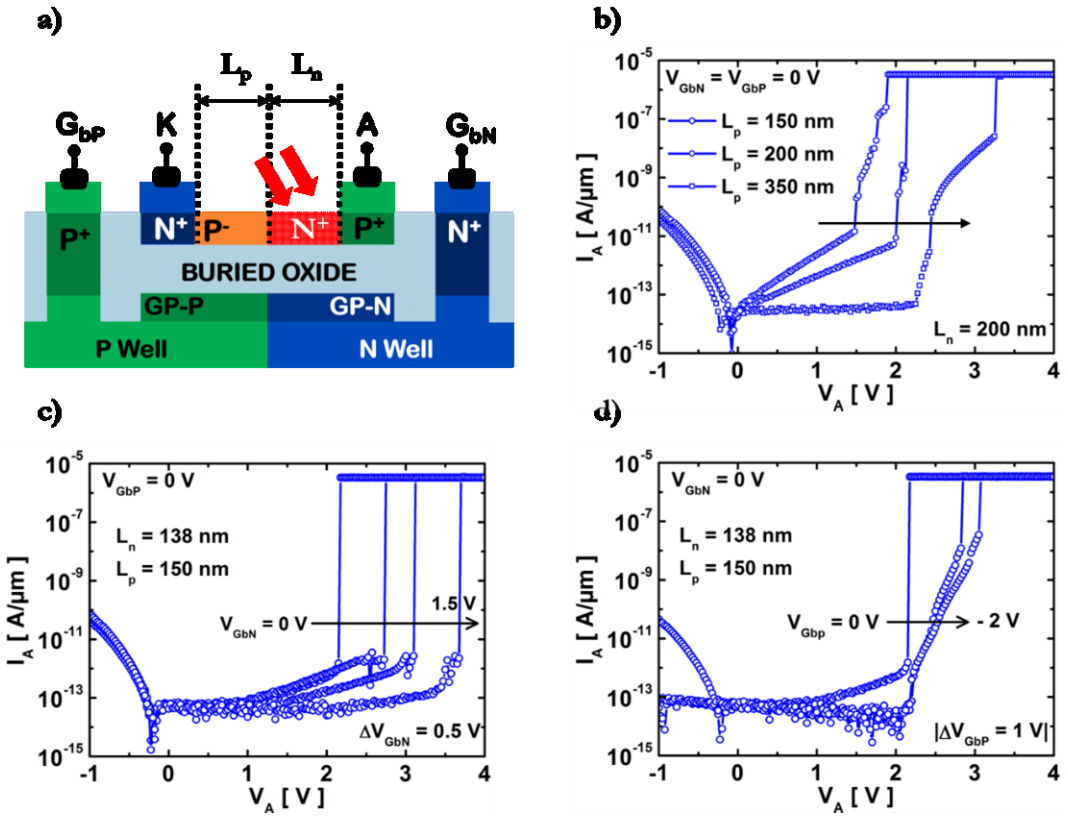

Figure 3.15. (a) Schematic of doped Z³-FET variant architecture in 14 nm FDSOI technology. (b) Current versus drain voltage measured for different geometries at $V_{GbN} = V_{GbP} = 0$ V and for short Z³-FET (c) at various GP-N bias with $V_{GbP} = 0$ V and (d) various GP-P bias with $V_{GbN} = 0$ V.

3.2.2.4. Silicon-Germanium (SiGe) and Strained Variants

Figure 3.16-a shows the experimental I_A-V_A curves of Z³-FET with Silicon-Germanium (SiGe) body at various GP-N bias and constant $V_{GbP} = -2$ V. The main characteristics, such as the modulated triggering voltage and the sharp switch, are maintained. Compared to all-Si Z³-FET (Figure 3.16-d), the barriers in Z³-FET with SiGe body are weaker, hence the carriers can be injected more easily in the channel, increasing lightly the leakage current as seen in Figure 3.16-c. Introducing silicon strained technology and combining silicon (Si) with germanium (Ge) improves the holes effective mobility [10–12] and increases the carrier diffusion length. In that case, the injected carriers from the anode/cathode cross the channel and contribute faster in barriers collapse, leading to a slight triggering voltage V_{ON} reduction (Figure 3.16-b), which is attractive for low-power applications.

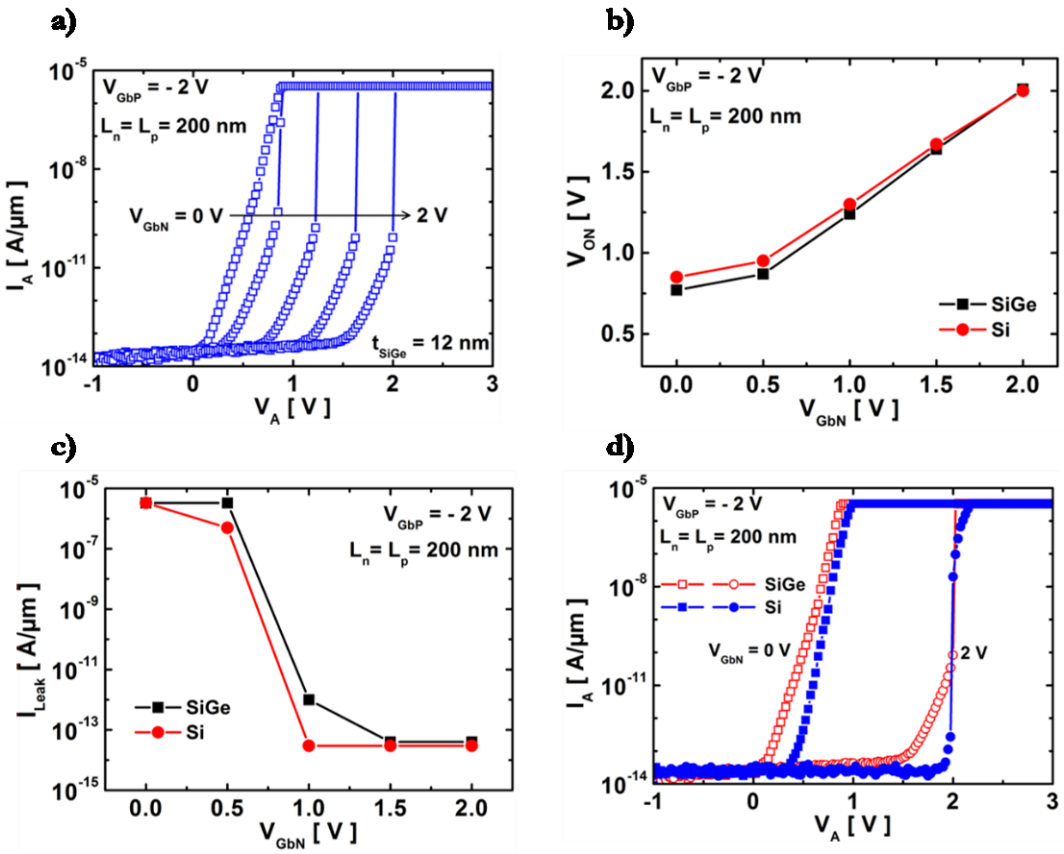

Figure 3.16. (a) Experimental I_A-V_A output characteristics for different V_{GbN} bias in Z³-FET with SiGe body. Comparison of (b) triggering voltage and (c) leakage current extracted at V_{dd} = 1 V between Z³-FETs with Si and SiGe. (d) I_A-V_A curves for Si (blue curves) and SiGe (red curves) Z³-FETs at V_{GbN} = 0 V and 2 V. V_{GbP} = - 2 V.

3.2.2.5. Temperature

The main characteristics of Z²-FET (sharp switch, hysteresis) are maintained in a wide temperature range, as shown in Figure 3.17-a [1, 13, 14]. At high temperature, carriers have higher thermal energy to unblock the barriers and turn the device ON more easily. As expected from simple physics laws, V_{ON} decreases ($\Delta V_{ON}/\Delta T$ = - 1.4 mV/°C) for both long and short devices (Figure 3.17-b). Note that in MOSFETs, the threshold voltage decreases at T = 125°C, enlarging the barrier height (~ (V_{Gf} -V_{th} - V_A)), which would lead to a higher V_{ON} to collapse the barriers. This argument does not hold in Z²-FET because carriers have gained energy at high temperature and can more easily pass the barrier. The competition between these two effects (stronger barrier and higher carrier energy) explains the temperature dependence observed in Figure 3.17-a. The linear dependence of V_{ON} on V_{Gf} and the slope $\Delta V_{ON}/\Delta V_{Gf}$ for different device lengths is conserved from room temperature (blue opened symbols) to 125°C (red closed symbols), as shown in Figure 3.17-b.

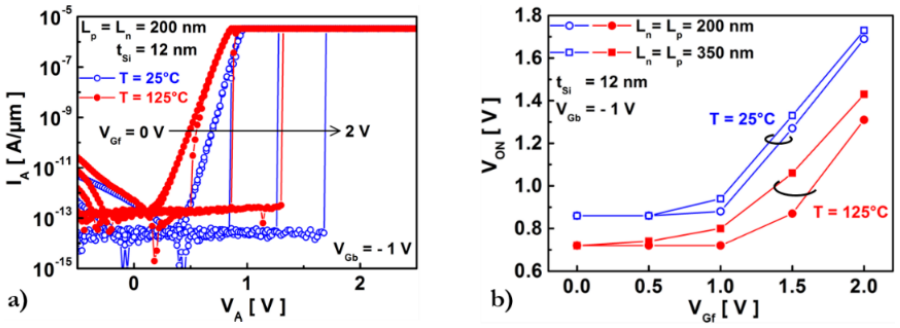

Figure 3.17. (a) Experimental I_A-V_A curves at T = 125°C (closed red symbols) and room temperature (open blue symbols) for various V_{Gf} and V_{GB} = - 1 V. (b) V_{ON} versus front-gate bias and V_{Gb} = - 1 V at T = 25°C and 125°C for different Z²-FET device lenghts. t_{Si} = 12 nm.

Z²-FET DGP and Z³-FET show acceptable immunity against temperature variation. The shift of triggering voltage V_{ON} is more important in short devices ($\Delta V_{ON}/\Delta T$ = - 8 mV/°C in Figure 3.18-b) and decreases for longer Z-FET structures ($\Delta V_{ON}/\Delta T$ = - 2 mV/°C in Figure 3.18-d). The barriers in short devices are narrower, hence they are more sensitive than broad barriers (in long devices) to the flow of carriers energized at high temperature [6]. This results in a higher leakage current increase at high temperature (~ 2 decades in Figure 3.18-a) than in long Z³-FET (just one decade, as shown in Figure 3.18-d). Note that the cooperation of GP-N and the front-gate in Z²-FET DGP at high temperature is also confirmed, as shown in Figure 3.18-a. Incrementing the GbN bias reinforces the L_n barrier and increases the triggering voltage V_{ON}.

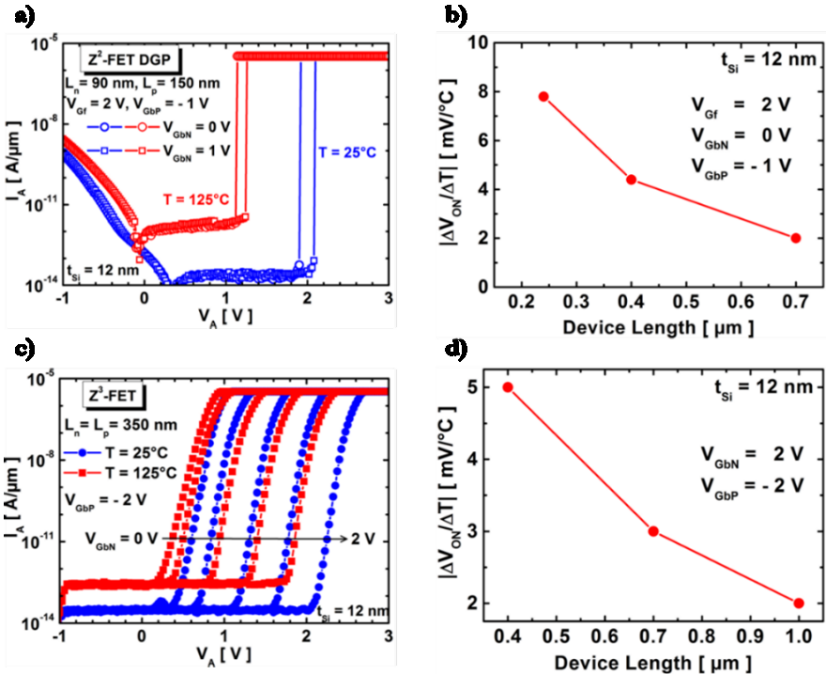

Figure 3.18. I_A-V_A curves at T = 125 °C (red symbols) and room temperature (blue symbols) with various V_{GbN} for (a) Z²-FET DGP at V_{Gf} = 2 V, V_{GbP} = - 1 V and (c) Z³-FET at V_{GbP} = - 2 V. Variation of triggering voltage shift $V_{ON}/\Delta T$ in (b) Z²-FET DGP and (d) Z³-FET versus device length.

Low temperature experiments were carried out on CEA-Leti Z^2-FET SGP variant with thicker silicon film (t_{Si} = 20 nm) and BOX (t_{BOX} = 145 nm). Compared to our previous results obtained at high temperature, the Z^2-FET exhibits higher triggering voltage V_{ON} and lower leakage current at T = 86 K [13, 14]. The energy of carriers decreases proportionally with temperature whereas the barrier height is weakly lowered. Since carriers have less chance to surpass the barriers, V_{ON} is increased at low temperature (blue opened symbols, Figure 3.19) : $\Delta V_{ON}/\Delta T$ = 1.7 mV/K.

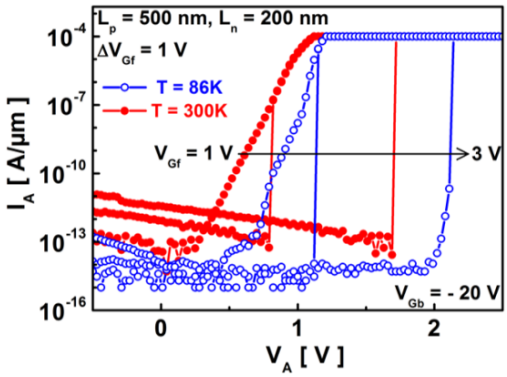

Figure 3.19. Experimental DC I_A-V_A characteristics for various V_{Gf} and V_{Gb} = - 20 V at room temperature (closed red symbols) and T = 86K (open blue symbols). Thick Z^2-FET variant from CEA-Leti with L_p = 500 nm and L_n = 200 nm.

Z-FET devices present reasonable dependency of triggering voltage V_{ON} on temperature which implies a careful front-gate bias determination for ESD protection (to avoid unwanted latch-up, discussed later in this chapter) and 1T-DRAM application for extended retention time.

3.2.3. FDSOI 28 nm node vs. 14 nm node

3.2.3.1. Standard Z^2-FET

DC measurements show that the Z^2-FET in 14 nm FDSOI node features the same high performance as its counterpart in 28 nm node [1, 2, 15–18]. At V_{Gf} = 0 V, the device operates as a diode rather that a Z^2-FET with high I_{ON} current (Figure 3.20-a). In ultra-thin silicon film (6 nm), the feedback is lost, leading to a non-steep switch (opened circle symbols, Figure 3.20-b). To retrieve the feedback between the barriers, the silicon film thickness has to be increased (here up to 12 nm). In that case, the 14FDSOI Z^2-FET features a vertical switch with $V_{ON} \cong$ 1.5 V (closed circle symbols, Figure 3.20-b) lower than in 28 nm node with $V_{ON} \cong$ 1.6 V (opened square symbols, Figure 3.20-b). Compared to 28 nm FDSOI technology, the BOX in 14 nm node is thinner, leading to an enhanced channel control via the back-gate. However, it affects more the gated barrier by

coupling effect, and hence decreases the triggering voltage V_{ON}. This explains the early triggering of Z^2-FET in 14 nm node at V_{Gb} = - 2 V.

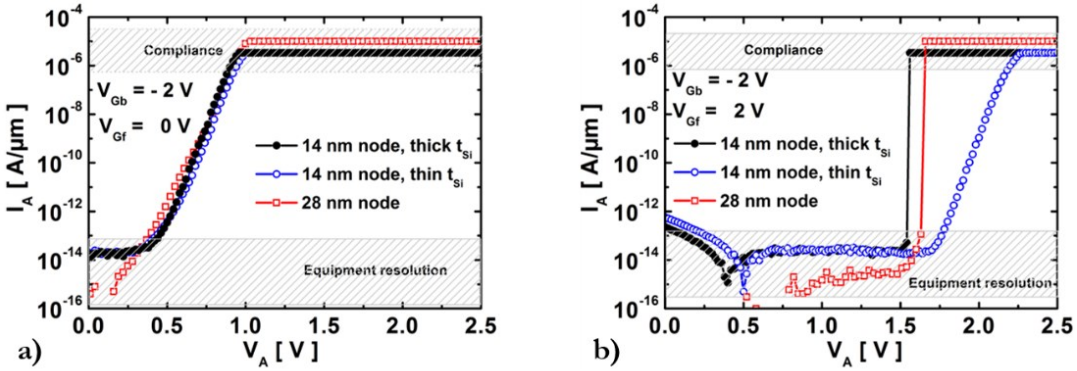

Figure 3.20. Comparison of output I_A-V_A curves in 14 nm FDSOI Z^2-FETs with thick (closed black circle symbols) and thin (open blue circle symbols) body and 28FDSOI Z^2-FET (open red square symbols) for (a) V_{Gf} = 0 V, V_{Gb} = - 2 V and (b) V_{Gf} = 2 V, V_{Gb} = - 2 V. $L_p = L_n$ = 200 nm.

3.2.3.2. Back-Gate Modulated Device, Z^3-FET

A comparison between Z^3-FET devices in 14 nm and 28 nm nodes was carried out and results are presented in Figure 3.21 [6, 19]. Due to the silicon film and BOX thinning, the electrostatic channel control of 14 nm Z^3-FET is enhanced. Hence, the barriers are stronger and need higher anode voltage V_A to collapse, leading to V_{ON} increase (blue curves with closed symbols, Figure 3.21). Also, the effective carrier lifetime, dominated by interfaces, decreases in 14 nm node. Since the carriers recombine more in the channel, the diffusion region expands (see section 2.2.2.1). This delays the collapse of barriers, thus inducing a moderate switch slope and increasing triggering voltage V_{ON}.

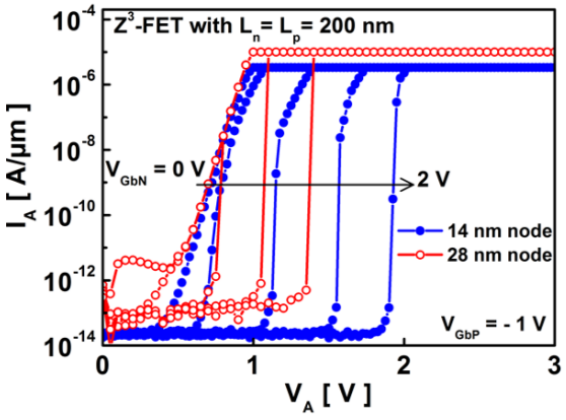

Figure 3.21. Comparison of experimental DC I_A-V_A curves in 14 nm FDSOI Z^3-FETs with thick body (closed blue circle symbols) and 28FDSOI Z^3-FET (open red circle symbols) at various GbN bias and V_{GbP} = - 1 V.

3.3. TLP Measurements

In this part, the ESD behavior and robustness at high current of Z-FET devices is investigated, at room temperature, using transmission line pulse (TLP) characterization method [20]. To simulate HBM, MM and CDM stress models, 100 ns and 5 ns pulse durations with native rise time (≅ 300 ps, limited by used equipment) were applied to the DUT (Device Under Test).

The values of ESD design window for three typical voltages (1.0 V, 1.8 V and 3.3 V) in 14 nm FDSOI technology and the latch-up (LU) electrical targets defined by the JEDEC78 standard are presented in Table 3.2 [21]. For example, to prevent the damage of a GO1 FET with thin gate oxide used in 1.0 V applications, the ESD protection device must trigger in a narrow ESD design window (between 1.0 V and 2.5 V) and must be able to drive high current (> 1.3 A for HBM). For 1.8 V applications, where the breakdown of stacked oxide GO2 FET devices is higher, the window is relaxed (2.0 V < V_{t1} < 4.0 V). Moreover, the ESD protection element should not trigger during the core circuit normal operation. Thus, to prevent latch-up (LU) event, two possibilities can be retained, (i) increasing the ESD device holding voltage above V_{ddmax} (V_{dd} + 10%), and (ii) tuning the triggering voltage and/or current of protection element above 1.5 × V_{ddmax} and 100 mA, respectively. In the following, we present TLP measurement results of 14 nm Z-FET devices that fit the required targets, especially for 1.0 V and 1.8 V applications.

Voltage application	ESD (2 kV, HBM)		LU (JEDEC78)		
	V_{t1} (V)	I_{t2} (A)	V_{t1} (V)	I_{t1} (mA)	V_H (V)
0.9 - 1.0 V	< 2.5	> 1.3	> 1.5 - 1.7	> 100	> 1 – 1.1
1.8 V	< 4.0	> 1.3	> 3.0	> 100	> 2.0
3.3 V	< 8.0	> 1.3	> 5.4	> 100	> 3.6

Table 3.2. ESD/LU electrical specification summary. In green the targets which must be reached; in white the target which would be nice to reach; and in grey the holding voltage target.

3.3.1. Standard Z²-FET

The high current performance of Z²-FET device with two different silicon film thicknesses (t_{Si} = 12 nm in black curves and t_{Si} = 6 nm in blue curves) for two short pulse widths (t_{PW} = 5 ns and 100 ns) is shown in Figure 3.22 [1]. Z²-FETs with thicker t_{Si} feature higher maximum current and sharper turn-on than their ultrathin counterparts. The efficiency to evacuate high current depends strongly on the duration of the ESD event and the thickness of silicon film. Longer discharges as well as ultrathin films will cause more device heating that degrades the failure current

I_{t2}. This effect is documented in Figure 3.22, which shows a clear reduction in current for longer TLP pulses. Moreover, the ESD ON-Resistance (R_{ON}) is lowered with increasing t_{Si} from 6 nm up to 12 nm (R_{12nm} = 200 Ω/μm < R_{6nm} = 520 Ω/μm).

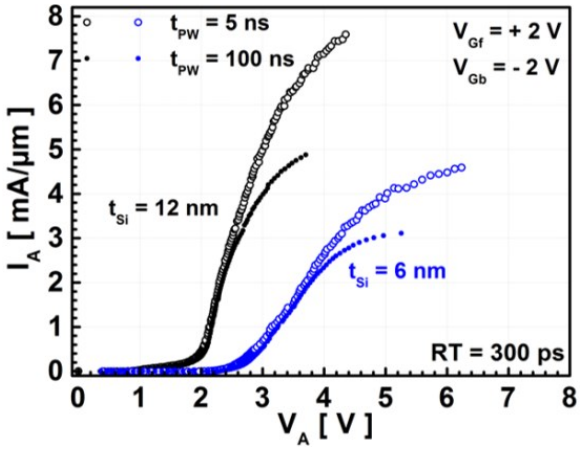

Figure 3.22. TLP characterization results for thick (black curves) and thin (blue curves) Z²-FET exposed to 5 ns (open symbols) and 100 ns (closed symbols) pulse width, respectively, with native rise time (≅ 300 ps). V_{Gf} = 2 V and V_{Gb} = - 2 V.

Figure 3.23 shows the evolution of failure current I_{t2} and triggering voltage V_{t1} versus Z^2-FET device length. The capability of sustaining high current in both (a) thick and (b) thin structures decreases with device length increase. Inversely, in long devices where the barriers are broader, V_{t1} increases. All thin Z^2-FETs (t_{Si} = 6 nm, Figure 3.23-b) and long devices with thick silicon film (> 400 nm in Figure 3.23-a) feature a good latch-up immunity for 1.8 V applications. The turn-on voltage of these devices surpasses the holding voltage criterion (V_H = 2.0 V) imposed by JEDEC78 [21]. On the other hand, despite the robustness and efficiency to evacuate high current (> 5 mA/μm and > 7.5 mA/μm for 100 ns and 5 ns pulse widths respectively in Figure 3.23-a), the early trigger of short devices ($V_{t1} \leq V_{dd}$ + 10 % for $L_n + L_p$ < 400 nm) with t_{Si} = 12 nm restrict their usage in 1.8 V ESD applications. For example, Z^2-FET with $L_n = L_p$ = 138 nm triggers at anode voltage V_A = 1.7 V, which is lower than the supply voltage V_{ddmax} = 2.0 V. However, short devices with both silicon film thicknesses fit perfectly the 1.0 V application requirements as they trigger in the dedicated ESD tight window (1.0 V < V_{t1} (ESD) < 2.5 V).

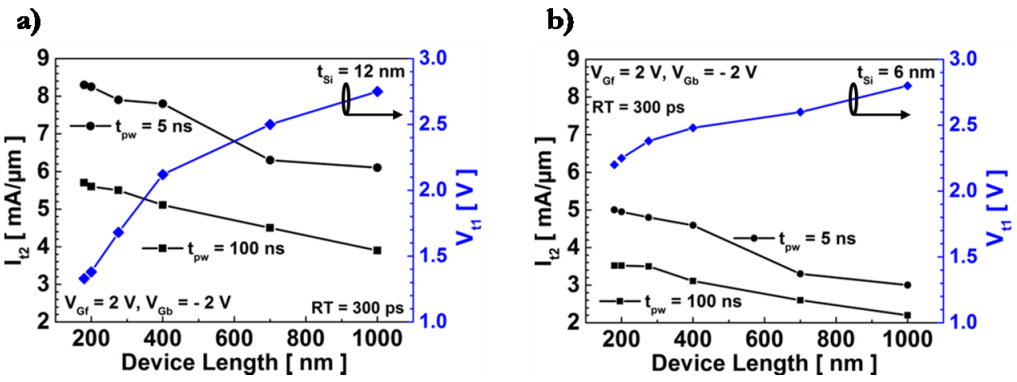

Figure 3.23. Variation of triggering voltage V_{t1} (blue diamond symbols, right-hand y axis) and failure current I_{t2} (left y axis) for 5 ns (circle symbols) and 100 ns (square symbols) pulses versus device length for (a) thick and (b) thin Z^2-FETs. $V_{Gf} = V_{Gb} = -2$ V.

3.3.2. Z^3-FET

3.3.2.1. Undoped Variant

The ESD behavior of undoped Z^3-FETs with different body lengths was investigated and results are presented in Figure 3.24. Two distinct pulse widths were used, as before (t_{PW} = 5 ns and 100 ns in Figure 3.24-a and b, respectively). Like in Z^2-FET with single ground plane, short Z^3-FET devices ($L_n = L_p$ = 138 nm) feature high performance at short pulse width (8 mA/µm for t_{PW} = 5 ns Figure 3.24-a). The failure current degrades with device length increase (6 mA/µm for $L_n = L_p$ = 500 nm Figure 3.24-a) as well as with pulse width raise up (5 mA/µm for t_{PW} = 100 ns, Figure 3.24-b). It is confirmed that the maximum current and triggering voltage values depend strongly on device length. Shorter Z^3-FETs show easier triggering V_{t1}, higher current capability and lower R_{ON} resistance [6].

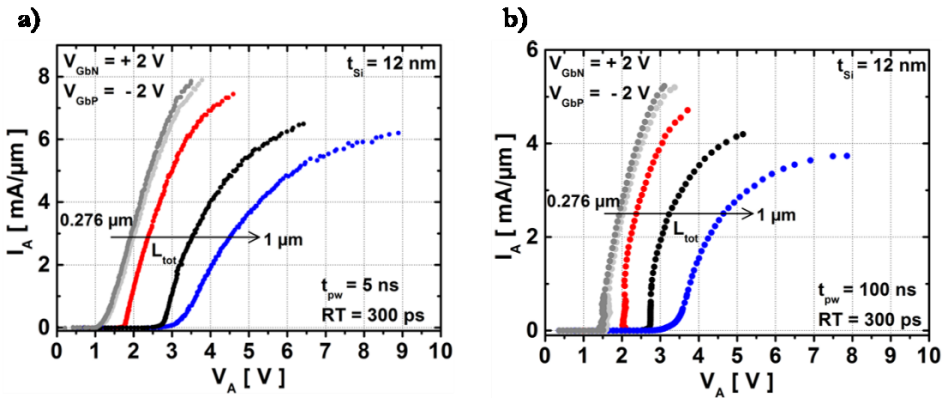

Figure 3.24. (a) 5 ns and (b) 100 ns TLP measurements of various undoped Z^3-FET devices (length from 276 nm up to 1 µm) with thick silicon film (t_{Si} = 12 nm) at V_{GbN} = 2 V and V_{GbP} = - 2 V.

Non-destructive TLP measurements are presented in Figure 3.25. It is noted that the triggering voltage of the band-modulation device is tunable not only with GbN (Figure 3.25-a) but also with GP-P bias (Figure 3.25-b) and device length (dotted lines in Figure 3.25-a, b). The higher the V_{GbN} or $|V_{GbP}|$ bias, the larger the triggering voltage. Taking advantage of these adjustable parameters, our devices are able to fulfill the ESD design window requirements, especially for 1.0 V and 1.8 V applications, showing ultra-low leakage current, high I_{t2} and abrupt switching. Remember that the Z^3-FET can sustain up to 8 V bias without device breakdown (as mentioned in section 3.2.2.1.c). With this characteristic, the Z^3-FET can be promoted as a high-voltage (HV) ESD protection element.

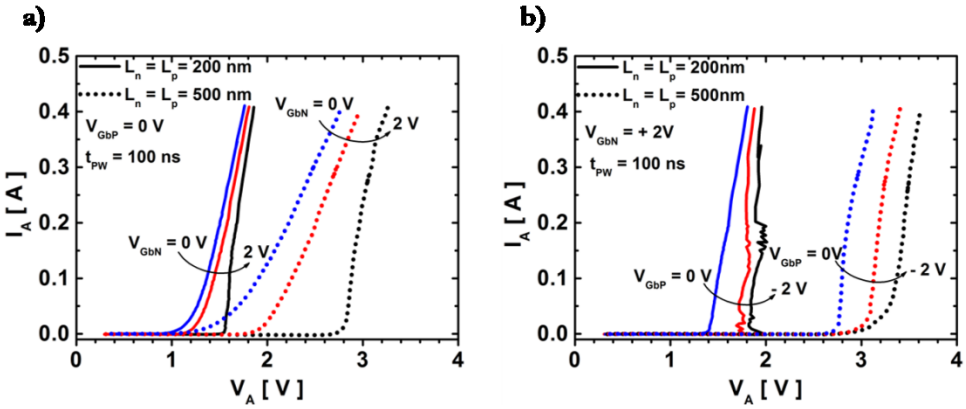

Figure 3.25. Non-destructive TLP measurements for 100 ns pulse width in short (solid lines) and long (dotted lines) Z^3-FETs for (a) $V_{GbP} = 0$ V and various GP-N bias and (b) $V_{GbN} = 2$ V and various GP-P bias.

Undoped Z^2-FET and Z^3-FET variants (normally ON at zero gate bias) could disturb the operation of the core circuit. Thus, an external control circuit (RC filter for example) connecting the front/back gates to a positive/negative power supply voltage is a must. With $V_{Gf}/V_{GbN} > 0$ V and $V_{Gb}/V_{GbP} < 0$ V, ESD devices are blocked (OFF state) featuring low leakage current without affecting the normal activity of protected circuit. When ESD occurs, the high discharge current turns on Z-FET structures and passes through toward the ground.

3.3.2.2. Doped Variant

The Z^3-FET undoped variant features excellent performance but requires a positive bias on GP-N and a negative bias on GP-P, which may not be suitable for ESD chip designers [6]. To address this issue, another variant was designed and fabricated with N-type L_n doped part of the channel. Figure 3.26 shows the S-shaped negative resistance characteristic for two different lengths of partially N-doped Z^3-FET devices with no back-gate bias facing 5 ns (Figure 3.26-a) and 100 ns

pulse widths (Figure 3.26-b), respectively. Doping the L_n part of short Z^3-FET channel reinforces the barrier in this region and thus increases the triggering voltage (dashed lines in Figure 3.26-a, b). However, it does not reach the required latch-up V_H target of 1.8 V application (V_H = 1.5 V < 2 V), thus restricting its usage for GO2 FET protection against electrostatic discharges. This difficulty can be solved by increasing the device length. Yet, the holding voltage of Z^3-FET with $L_n + L_p$ = 550 nm does not fit LU requirements (dotted lines in Figure 3.26-a, b).

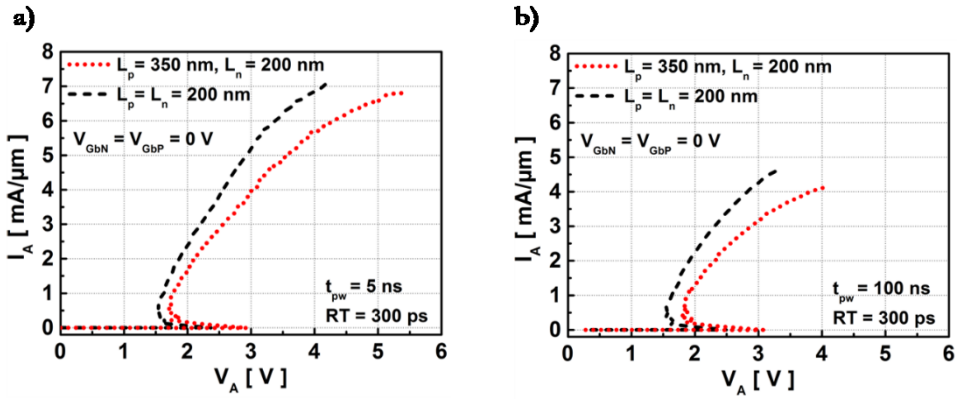

Figure 3.26. TLP I_A-V_A characteristics for N-doped long (dotted lines) and short (dashed lines) Z^3-FETs against (a) 5 ns and (b) 100 ns pulse widths at $V_{GbN} = V_{GbP} = 0$ V. t_{Si} = 12 nm.

As presented in section 3.2.2.5, Z-FET devices feature an admissible dependence on temperature variation. At high temperature where the triggering voltage decreases, band-modulation devices could be threatened by latch-up events. Thus a vigilant bias of structure terminals (anode, front-gate and back-gate) should be chosen. Furthermore, the need of external trigger circuit (i.e. RC circuit) to block the undoped Z-FET devices during ESD events restrains their use as protection elements. Doping the silicon body (L_n or L_p parts) can solve this issue since no more front-back gate bias is needed to form the barriers and keep the device blocked. This was the motivation to study in the following the robustness of stacked doped devices with hybrid-bulk silicon controlled rectifier (SCR) against electrostatic discharges.

3.3.3. Stacked Architectures

The modulated triggering voltage is an important feature of Z-FET devices that makes them very attractive nowadays. For this purpose, Fonteneau et al. [22] choose to use them as trigger elements for ESD power devices. Thus, a stack composed of thin silicon film triggering structures over a hybrid-bulk SCR was developed. The first innovative device, presented in Figure 3.27-a, is

composed of a Z^2-FET ($L_n = L_p = 0.15$ µm) on top of SCR (Z^2-FET enhanced Stacked SCR, ZeST). To avoid back-gate biasing, the Z^2-FET L_p part of the channel was doped using P-type ion implantation. In the second stacked device, called BeST (Figure 3.27-c), the doped Z^2-FET was replaced by a Back Bias Controlled Thyristor (BBC-T with doped L_n part = 0.2 µm and undoped L_{int} region = 0.3 µm [15, 18, 23]), which is similar to doped Z^3-FET, but with just one ground plane under the structure. To avoid the influence of positive Nwell back biasing on Z-FET devices, the NW/PW junction was shifted far from the channel region (Figure 3.27-b, d).

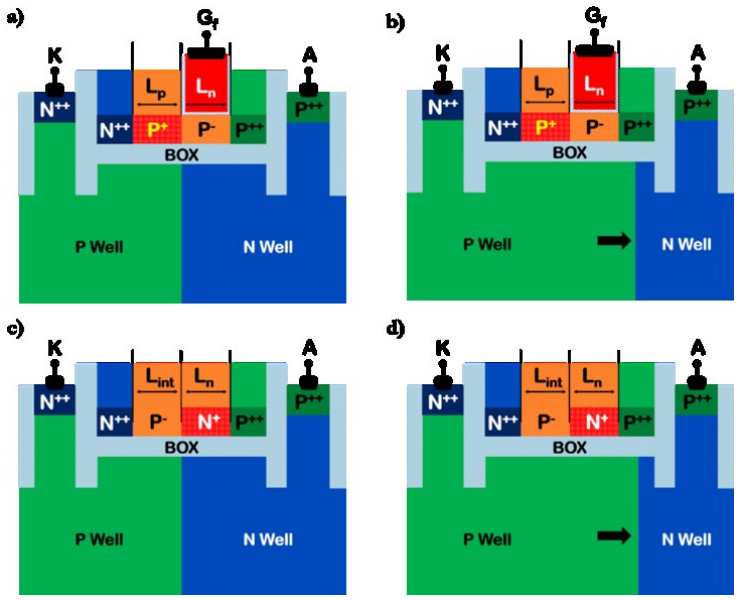

Figure 3.27. Cross-sections of (a) doped Z^2-FET and (c) BBC-T Enhanced Stacked SCR (ZeST and BeST) with central NW/PW junction and (b, d) shifted NW/PW junction. Channel width W = 100 µm.

DC characterizations performed at room temperature on two ZeST and BeST devices are presented in Figure 3.28-a, b, respectively. The SCR, placed under the BOX of thin film devices, is functional and shows a very low leakage current. However, it exhibits a high triggering voltage and hence cannot be an efficient ESD protection for low voltage applications. The ZeST device (at $V_{Gf} = 2$ V, Figure 3.28-a) offers a low leakage current (1 nA at $V_{dd} = 2$ V) but needs an external front-gate voltage to remain in OFF state, thus restricting its usage. This issue is solved with BBC-T device as it does not need any external bias to be blocked. Figure 3.28-b shows, in addition to SCR output characteristics, the I_A-V_A curves of two BeST devices with different L_{int} (undoped part of the channel) lengths of BBC-T. Compared to ZeST, the SCR with short BBC-T fits the 1.8 V ESD design window but with higher leakage current. Increasing the length of L_{int} from 300 nm up to 650 nm reinforces the barrier in this region and enhances the parameters of the device (leakage current and triggering voltage) to protect 3.3 V applications.

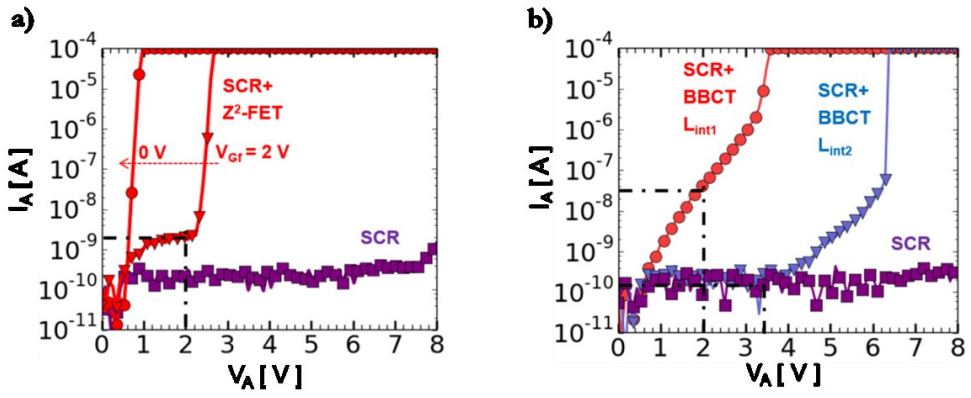

Figure 3.28. Experimental I_A-V_A DC characteristics at room temperature on (a) ZeST and (b) BeST devices.

The robustness and high current performance of ZeST and BeST stacked devices for 100 ns pulse width (HBM equivalent) were explored using TLP characterization method. Figure 3.29 confirms the Z-FET devices capability of turning ON the bulk-SCR at earlier anode voltage. First, the Z^2-FET and BBC-T elements are activated and the current flows in the stacked structure to fire then the hybrid-bulk device at ≅ 200 mA (far from the forbidden Latch-Up criterion, 100 mA). Grounding the front-gate of Z^2-FET permits fitting the 1.8 V ESD design window requirements (Figure 3.29-a), but with an external triggering circuit. This makes it less interesting than BBC-T (Figure 3.29-b), which does not need any external bias. It was also noticed that the incorporation of thin film devices with bulk-SCR increases the failure current of the overall ESD protection by 25%, as seen in Figure 3.29-a, b.

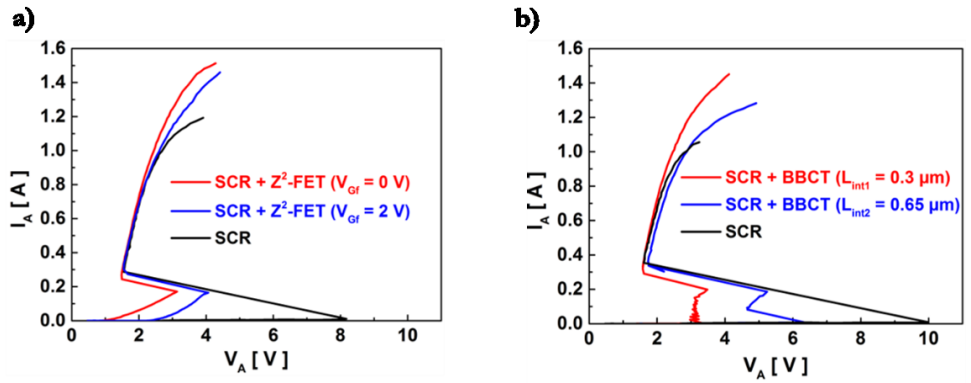

Figure 3.29. I_A-V_A TLP measurements for 100 ns pulse width of (a) ZeST and (b) BeST structures vs. standard hybrid-bulk SCR.

In addition of tunable triggering voltage, low leakage current and high current drive capability, ZeST and BeST devices consume less surface (75%) than bulk-SCRs with an external hybrid-bulk FET trigger. With these very promising results, the use of Z-FET family structures is highly recommended as triggering elements for ESD protection of power devices.

3.4. Interface Potential Analytical Model

3.4.1. Introduction

The feasibility of band-modulation devices in advanced FDSOI technology was demonstrated successfully. DC and TLP measurements were presented, showing the outstanding features of Z-FET family devices. Now, to evaluate these structures by designers before fabrication and to determine their benefit at application level, a full compact model is needed. An analytical model of Z^2-FET DC operation, compatible with SPICE simulator, was published recently [24]. The model generates the S-shaped I_A-V_A curve numerically with fitting parameter; the values of inversion/depletion surface potentials were evaluated through an adaptation of Leti-UTSOI model [25, 26]. A sophisticated physics-based model for Z^2-FET was derived in [27]. It is based on the continuity of the total current for each of three junctions: at anode, cathode and the center of the body, respectively. However, the model relies on numerical resolution of a set of 5 equations, which is not suitable for SPICE simulator. Since the simplest possible calculation chain is needed to get an efficient compact model, an analytical calculation of 28FDSOI Z^2-FET interface potential, using Poisson's equation and a parabolic function approach, is presented in the following, taking into consideration the internal voltage V_{in} (shown in Figure 3.30).

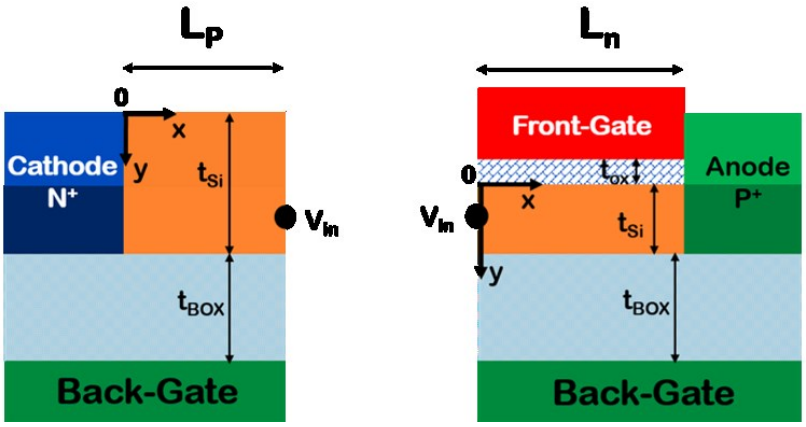

Figure 3.30. Schematic cross-section view of Z^2-FET with dissociated silicon channel.

The innovative idea here is to calculate the surface potential in every part of the channel separately, and then combine them after the evaluation of internal voltage V_{in}. The 2-D Poisson's equation was solved in the weak inversion/accumulation regimes of L_n/L_p channel parts, respectively, neglecting the mobile charges in the ultrathin film. Then, for strong inversion and accumulation regimes, we compute the value of surface potentials as they tend to saturate (adapted

from Leti-UTSOI model), and propose an estimation with a smoothing function taken from [25]. The model was then applied for Z^2-FET (t_{ox} = 3.2 nm, t_{box} = 25 nm, t_{Si} = 7 nm for L_n part and 22 nm for L_p part) with different $L_{n,\ p}$ lengths at V_A = 0 V and different front and back-gate voltages. In the following, a detailed calculation of surface potential distribution in the whole Z^2-FET body is given and compared, at the end of this section, with other Z-FET family devices.

3.4.2. Potential Distribution Model

3.4.2.1. Z^2-FET SGP

- **L_n part**

The potential distribution Φ(x, y) in the undoped thin silicon film of Z^2-FET is governed by Poisson's equation [28, 29]:

$$\frac{d^2\Phi(x,y)}{dx^2} + \frac{d^2\Phi(x,y)}{dy^2} = \frac{qN_A}{\varepsilon_{Si}} \qquad (3.3)$$
$$0 \leq x \leq L_{n,p} \text{ and } 0 \leq y \leq t_{Si},$$

where N_A is the channel doping concentration, ε_{Si} is the dielectric constant of silicon, t_{Si} is the silicon thickness (which is not uniform in the whole structure because of epitaxy layer in uncovered part of the channel) and $L_{n,p}$ is the length of gated and ungated Z^2-FET parts, respectively. Before the onset of strong inversion, in the gated part of the channel, the potential Φ(x, y) can be approximated by a simple parabolic function along the vertical 'y' dimension [30]:

$$\Phi(x,y) \approx C_0(x) + C_1(x)\cdot y + C_2(x)\cdot y^2, \qquad (3.4)$$

where the coefficients $C_0(x)$, $C_1(x)$, and $C_2(x)$ depend only on x. For fully depleted SOI Z^2-FET, the potential at the front-interface of gated part Φ_f (x, 0) is different from that at the back-side Φ_b (x, t_{Si}). The boundary conditions at the channel-oxide interfaces can be written using Gauss's law in the y-direction:

$$\left.\frac{d\Phi(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\Phi_f(x) - V_{GF}}{t_{ox}} \tag{3.5}$$

$$\left.\frac{d\Phi(x,y)}{dy}\right|_{y=t_{Si}} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{V_{GB} - \Phi_b(x)}{t_{box}}, \tag{3.6}$$

where $V_{GF} = V_{Gf} - V_{FBf}$ and $V_{GB} = V_{Gb} - V_{FBb}$ are the front-gate and back-gate voltages, respectively, ε_{ox} is the oxide dielectric constant and t_{ox}/t_{box} are the thicknesses of the front and back oxides, respectively. $V_{FBf} = V_T \ln\left(\frac{N_{A,channel}}{n_i}\right)$ and $V_{FBb} = V_T \ln\left(\frac{N_{A,GP-P}}{n_i}\right)$ are the flat band voltages at the front and back interfaces, respectively, where V_T is the thermal voltage and n_i is the intrinsic carrier concentration. The acceptor concentration of the channel is given by $N_{A,\,channel}$ (10^{15} cm^{-3}) and that of the P-type ground plane by $N_{A,\,GP\text{-}P}$ (10^{18} cm^{-3}). Solving the system of (3.2)-(3.4), the obtained $C_i(x)$ coefficients are:

$$C_0 = \Phi_f(x), \tag{3.7}$$

$$C_1 = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\Phi_f(x) - V_{GF}}{t_{ox}}, \tag{3.8}$$

$$C_2 = \frac{\left(V_{GB} + \left(\frac{\varepsilon_{ox} t_{Si}}{\varepsilon_{Si} t_{ox}} + \frac{t_{box}}{t_{ox}}\right) V_{GF} - \left(1 + \frac{\varepsilon_{ox} t_{Si}}{\varepsilon_{Si} t_{ox}} + \frac{t_{box}}{t_{ox}}\right) \Phi_f(x)\right)}{t_{Si}^2 \left(1 + \frac{2\varepsilon_{Si} t_{box}}{\varepsilon_{ox} t_{Si}}\right)}. \tag{3.9}$$

Substituting the C_i values in (3.2) and taking the derivative in (3.1), we get the following 2nd order differential equation:

$$\frac{d^2\Phi_f(x)}{dx^2} - \alpha_f \Phi_f(x) = \beta_f. \tag{3.10}$$

To simplify the equations, we assumed that the back-gate oxide capacitance $C_{box} = \varepsilon_{ox}/t_{box}$ is much smaller than both the front-gate oxide capacitance $C_{ox} = \varepsilon_{ox}/t_{ox}$ and the silicon film capacitance $C_{Si} = \varepsilon_{Si}/t_{Si}$. Thus, α_f and β_f can be approximated as:

$$\alpha_f \approx \frac{\varepsilon_{ox}}{\varepsilon_{Si} t_{Si} t_{ox}}, \tag{3.11}$$

$$\beta_f \approx \frac{qN_A}{\varepsilon_{Si}} - \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{(t_{box} V_{GF} + t_{ox} V_{GB})}{t_{Si} t_{ox} t_{box}}. \tag{3.12}$$

The particular solution of the 2nd order differential Eq. (3.8) is calculated and given by:

$$A_1 = \frac{\beta}{\alpha} = \frac{qN_A t_{Si} t_{ox}}{\varepsilon_{ox}} - \left(V_{GF} + \frac{t_{ox}}{t_{box}} V_{GB}\right). \tag{3.13}$$

The boundary conditions of the gated part of the channel are $\Phi_f(0) = V_{in}\ at\ x = 0$ and $\Phi_f(L_n) = V_{bi} + V_A\ at\ x = L_n$ (where $V_{bi} = V_T \ln\left(\frac{N_A}{n_i}\right)$ is the built in potential across the anode-channel junction). With these values and the particular solution, the expression along the L_n part of the front interface potential is obtained:

$$\Phi_f(x) = A_1 + \frac{1}{e^{\frac{2L_n}{\lambda_1}} - 1}\left[(V_{bi} + V_A - A_1)\left(e^{\frac{L_n + x}{\lambda_1}} - e^{\frac{L_n - x}{\lambda_1}}\right) + (V_{in} - A_1)\left(e^{\frac{2L_n - x}{\lambda_1}} - e^{\frac{x}{\lambda_1}}\right)\right], \tag{3.14}$$

where

$$\lambda_1 = \frac{1}{\sqrt{\alpha_f}} = \sqrt{\frac{\varepsilon_{Si} t_{Si} t_{ox}}{\varepsilon_{ox}}}. \tag{3.15}$$

- **L_p part**

The same procedure was applied to the ungated part of the channel (L_p). We assume that the potential at the surface Φ_f (x, 0) = 0. Thus a new 2nd order differential equation is obtained:

$$\frac{d^2 \Phi_b(x)}{dx^2} - \alpha_b\, \Phi_b(x) = \beta_b, \tag{3.16}$$

where

$$\alpha_b = \frac{\varepsilon_{ox}}{\varepsilon_{Si} t_{Si} t_{box}}, \tag{3.17}$$

$$and\ \beta_b = \frac{qN_A}{\varepsilon_{Si}} - \frac{\varepsilon_{ox}}{\varepsilon_{Si} t_{Si} t_{box}} V_{GB}. \tag{3.18}$$

The boundary conditions of this region are $\Phi_b(0) = V_{bi}\ at\ x = 0$ and $\Phi_b(L_p) = V_{in}\ at\ x = L_p$ (where $V_{bi} = V_T \ln\left(\frac{N_D}{n_i}\right)$ is the built-in potential across the cathode-channel junction). The expression along the L_p part of the channel at the front interface is obtained:

$$\Phi_b(x) = A_2 + \frac{1}{e^{\frac{2L_p}{\lambda_2}} - 1}\left[(V_{in} - A_2)\left(e^{\frac{L_p + x}{\lambda_2}} - e^{\frac{L_p - x}{\lambda_2}}\right) + (V_{bi} - A_2)\left(e^{\frac{2L_p - x}{\lambda_2}} - e^{\frac{x}{\lambda_2}}\right)\right], \tag{3.19}$$

with

$$A_2 = V_{GB} - \frac{qN_A t_{Si} t_{box}}{\varepsilon_{ox}}, \tag{3.20}$$

and

$$\lambda_2 = \sqrt{\frac{\varepsilon_{Si} t_{Si} t_{box}}{\varepsilon_{ox}}}. \tag{3.21}$$

- **The internal potential V_{in}**

The surface potential of each part of Z^2-FET device was evaluated separately. To have a continuous potential distribution all along the channel, $\Phi_f(x)$ and $\Phi_b(x)$ should be connected with V_{in} (the common internal voltage). The lateral electric field continuity between the two parts of Z^2-FET (L_n and L_p, Eq. (3.20)) allows computing the value of V_{in} presented in Eq. (3.21).

$$E_b(x = L_p) = \left.\frac{d\Phi_b(x)}{dx}\right|_{x = L_p} = E_f(x = 0) = \left.\frac{d\Phi_f(x)}{dx}\right|_{x = 0}, \tag{3.22}$$

$$V_{in} = \frac{B_1\lambda_1 \sinh\left(\frac{L_n}{\lambda_1}\right) + B_2\lambda_2 \sinh\left(\frac{L_p}{\lambda_2}\right)}{\lambda_1 \sinh\left(\frac{L_n}{\lambda_1}\right)\cosh\left(\frac{L_p}{\lambda_2}\right) + \lambda_2 \sinh\left(\frac{L_p}{\lambda_2}\right)\cosh\left(\frac{L_n}{\lambda_1}\right)}, \tag{3.23}$$

with $B_1 = \left[V_{bi} + A_2\left(\cosh\left(\frac{L_p}{\lambda_2}\right) - 1\right)\right]$ and $B_2 = \left[V_{bi} + V_A + A_1\left(\cosh\left(\frac{L_n}{\lambda_1}\right) - 1\right)\right]$.

3.4.3. Model Verification

- **Weak accumulation/inversion**

The proposed model was verified by comparing the analytical equations with Synopsis TCAD simulation results (Figure 3.31-a). At low front-gate and back-gate voltages (V_{Gf} = 0.5 V and V_{Gb} = - 0.5 V), the L_n and L_p regions of Z²-FET are in weak inversion (≈ 10^{17} cm^{-3}) and accumulation (≈ 10^{15} cm^{-3}), respectively. A perfect agreement is obtained between the model (red solid line) and numerical results (black dashed line) all over the channel.

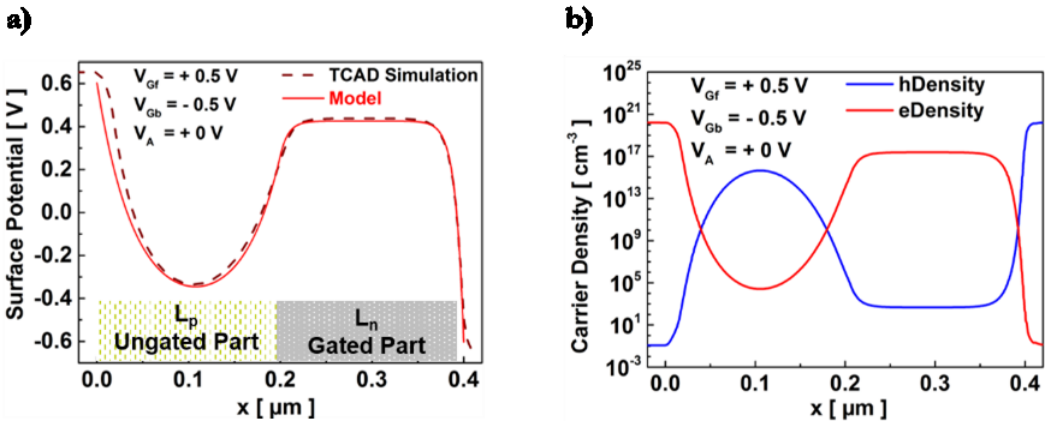

Figure 3.31. (a) Surface potential versus x for Z²-FET in weak accumulation (L_p = 200 nm) and weak inversion (L_n = 200 nm) and (b) simulated carrier density (holes in blue and electrons in red) along the channel at y = 0 for V_{Gf} = 0.5 V, V_{Gb} = - 0.5 V and V_A = 0 V.

- **Strong accumulation/inversion**

The evolution of surface potentials $\Phi_f(x)$ with V_{Gf} and $\Phi_b(x)$ with V_{Gb} are presented in Figure 3.32-a, c. When the electrons density approaches 10^{18} cm^{-3} (Figure 3.32-b), the L_n part enters into strong inversion, thus inducing a surface potential $\Phi_f(x)$ saturation. This can be seen in Figure 3.32-a when the front-gate bias goes beyond $V_{Gf} = 0.6$ V. The same action is observed in Figure 3.32-c where $\Phi_b(x)$ saturates when the holes density exceeds ~ 10^{17} cm^{-3} (Figure 3.32-d) for $V_{Gb} \geq -1.0$ V.

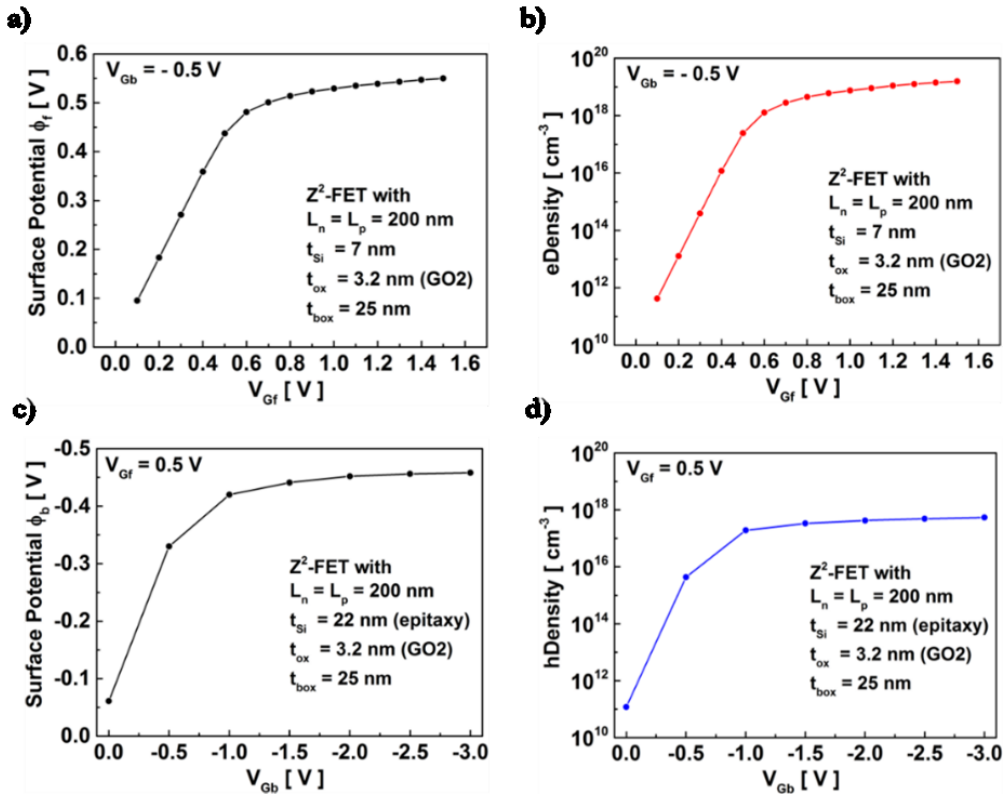

Figure 3.32. Evolution of (a) surface potential $\Phi_f(x)$ in L_n part of the channel and (b) electrons density with front-gate bias V_{Gf} at $V_{Gb} = -0.5$ V. (c) Surface potential $\Phi_b(x)$ in L_p channel part and (d) holes density with back-gate bias V_{Gb} at $V_{Gf} = 0.5$ V. Simulated 28 nm FD Z^2-FET. TCAD simulations.

The model above did not take into consideration the surface potentials saturation in the channel. To reproduce a similar surface potential behavior at high front and back-gate biases in both parts of Z^2-FET, the saturation values of interface potentials in each part were calculated. We assumed here that the Z^2-FET is a long FDSOI device with undoped channel. The capacitance C_{tot} of the MOS system is given by the series connection of oxide C_{ox} and inversion channel C_{inv} capacitances. Since in strong inversion regime (L_n region) $C_{inv} \gg C_{ox}$, $C_{tot} = C_{ox}$. For same reason,

C_{tot} in accumulation takes the value of BOX capacitance ($C_{tot} = C_{box}$) in strong accumulation regime (L_p region) [25]. The expressions of saturated $\Phi_f(x)$ and $\Phi_b(x)$ are given by:

$$\Phi_{f,sat}(x) = 3V_T + V_T \ln\left(\frac{V_T C_{ox}}{q n_i t_{Si}}\right) \tag{3.24}$$

$$\Phi_{b,sat}(x) = 3V_T + V_T \ln\left(\frac{V_T C_{box}}{q n_i t_{Si}}\right) \tag{3.25}$$

We make the estimation of interface potentials that tend to their respective saturation values with a smoothing function [25]:

$$\Phi_{f,final}(x) = \Phi_f(x) - 3V_T\left(1 + e^{\frac{[\Phi_f(x) - \Phi_{f,sat}(x)]}{3V_T}}\right) \tag{3.26}$$

$$\Phi_{b,final}(x) = \Phi_b(x) + 3V_T\left(1 + e^{\frac{[-\Phi_b(x) - \Phi_{b,sat}(x)]}{3V_T}}\right) \tag{3.27}$$

The evaluation of surface potential in the whole channel of Z²-FET obtained with the resolution of analytical equations is compared with TCAD simulation results at relatively high front and back-gate biasing in Figure 3.33-a, b. It is clearly seen that the potentials calculated by the model agree very well with the simulation results over the whole channel.

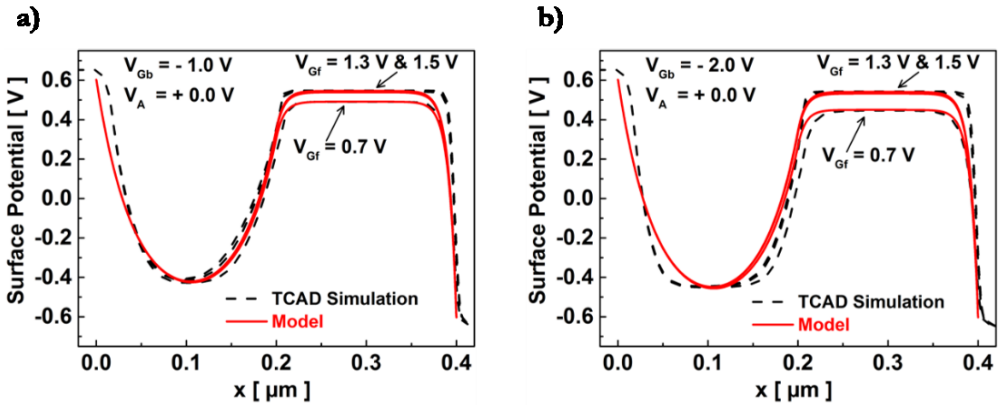

Figure 3.33. Surface potential versus x for Z²-FET with $L_n = L_p = 200$ nm along the channel at y = 0 for $V_{Gf} = 0.7$ V, 1.3 V and 1.5 V, $V_A = 0$ V, (a) $V_{Gb} = -1$ V and (b) $V_{Gb} = -2$ V.

The model was applied also to short (Figure 3.34-a) and long (Figure 3.34-b) Z^2-FET devices. The accuracy of the model is still good for different device lengths. It is noticed that, for V_{Gf} = 0.5 V or 1 V, the L_n barrier controlled by the gate is strong and the surface potential value is the same for short and long structures. On the other hand, the L_p barrier is affected by reducing the device length and starts to erode, as seen in Figure 3.34-a.

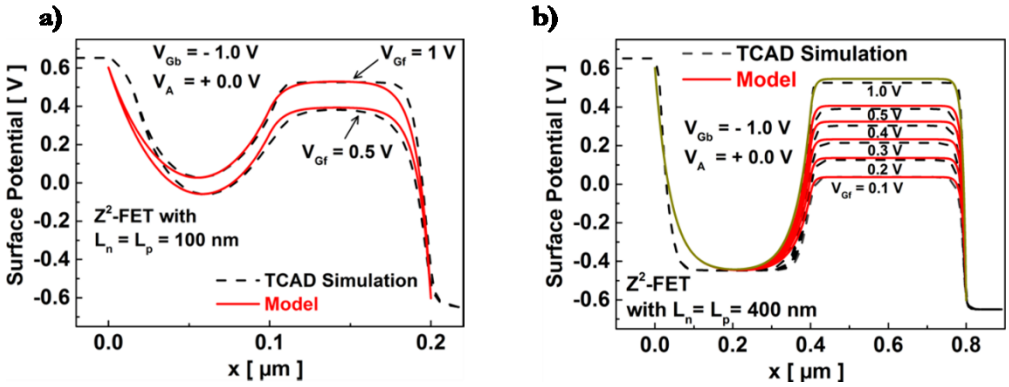

Figure 3.34. Surface potential versus x for (a) short Z^2-FET with $L_n = L_p$ = 100 nm at V_{Gf} = 0.5 V, 1 V and (b) long Z^2-FET with $L_n = L_p$ = 400 nm at various front-gate V_{Gf} biases. V_A = 0 V, V_{Gb} = - 1 V.

In the following, we present the surface potential computation of Z^2-FET DGP and Z^3-FET devices.

3.4.4. Z^2-FET DGP and Z^3-FET

Same analytical procedure was applied to other Z-FET devices. Remember that, for Z^2-FET DGP, the GP-N cooperates with the front-gate and reinforces the barrier in this region. For this purpose, in L_n part of the channel, the negative "V_{GB}" term in Eq. (3.11) is replaced by "V_{GbN}" with positive values. The potential distribution in the two parts of the channel ($\Phi_n(x)$ for L_n and $\Phi_p(x)$ for L_p) is given by:

$$\Phi_n(x) = A_1 + \frac{1}{e^{\frac{2L_n}{\lambda_1}} - 1}\left[(V_{bi} + V_A - A_1)\left(e^{\frac{L_n+x}{\lambda_1}} - e^{\frac{L_n-x}{\lambda_1}}\right) + (V_{in} - A_1)\left(e^{\frac{2L_n-x}{\lambda_1}} - e^{\frac{x}{\lambda_1}}\right)\right], \tag{3.28}$$

with

$$\lambda_1 = \sqrt{\frac{\varepsilon_{Si} t_{Si} t_{ox}}{\varepsilon_{ox}}}, and\ A_1 = \frac{qN_A t_{Si} t_{ox}}{\varepsilon_{ox}} - \left(V_{GF} + \frac{t_{ox}}{t_{box}} V_{GBN}\right), \tag{3.29}$$

similarly :

$$\Phi_p(x) = A_2 + \frac{1}{e^{\frac{2L_p}{\lambda_2}} - 1}\left[(V_{in} - A_2)\left(e^{\frac{L_p + x}{\lambda_2}} - e^{\frac{L_p - x}{\lambda_2}}\right) + (V_{bi} - A_2)\left(e^{\frac{2L_p - x}{\lambda_2}} - e^{\frac{x}{\lambda_2}}\right)\right], \tag{3.30}$$

with

$$\lambda_2 = \sqrt{\frac{\varepsilon_{Si} t_{Si} t_{box}}{\varepsilon_{ox}}}, and\ A_2 = V_{GBP} - \frac{qN_A t_{Si} t_{box}}{\varepsilon_{ox}}. \tag{3.31}$$

For Z^3-FET, the interface potential distribution in L_p region is still the same as for other Z-FET devices while the L_n surface potential changes as it is now modulated, instead of front-gate, by a back N-type ground plane (GP-N). Analytical equations of potential distributed in the whole body of Z^3-FET are given by:

$$\Phi_n(x) = A_1 + \frac{1}{e^{\frac{2L_n}{\lambda_1}} - 1}\left[(V_{bi} + V_A - A_1)\left(e^{\frac{L_n + x}{\lambda_1}} - e^{\frac{L_n - x}{\lambda_1}}\right) + (V_{in} - A_1)\left(e^{\frac{2L_n - x}{\lambda_1}} - e^{\frac{x}{\lambda_1}}\right)\right], \tag{3.32}$$

and

$$\Phi_p(x) = A_2 + \frac{1}{e^{\frac{2L_p}{\lambda_2}} - 1}\left[(V_{in} - A_2)\left(e^{\frac{L_p + x}{\lambda_2}} - e^{\frac{L_p - x}{\lambda_2}}\right) + (V_{bi} - A_2)\left(e^{\frac{2L_p - x}{\lambda_2}} - e^{\frac{x}{\lambda_2}}\right)\right], \tag{3.33}$$

where

$$\lambda_1 = \lambda_2 = \sqrt{\frac{\varepsilon_{Si} t_{Si} t_{box}}{\varepsilon_{ox}}}, \tag{3.34}$$

$$A_1 = V_{GBN} - \frac{qN_A t_{Si} t_{box}}{\varepsilon_{ox}} \quad and \quad A_2 = V_{GBP} - \frac{qN_A t_{Si} t_{box}}{\varepsilon_{ox}}.$$

The interface potential distribution model is computed for Z^2-FET DGP and Z^3-FET variants and compared to standard Z^2-FET with single GP (Figure 3.35) in weak inversion/accumulation regimes for L_n and L_p, respectively. As it is modulated by ground planes (N and P) with a thick back-gate oxide (t_{box} = 25 nm), the Z^3-FET exhibits narrower L_n barrier as seen in Figure 3.35 (dotted black curve). On the other side, and compared to Z^2-FET with single ground plane, the L_n barrier of Z^2-FET DGP is stronger at V_{Gf} = 0.5 V. This is due to the presence of GP-N underneath the front-gate that reinforces the potential in this region even for zero bias (V_{GbN} = 0 V).

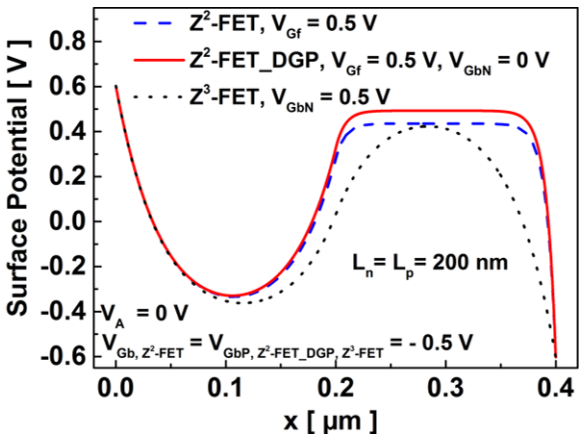

Figure 3.35. Comparison of surface potential distribution model along the whole silicon body between Z^2-FET SGP at V_{Gf} = 0.5 V (dashed blue curve), Z^2-FET DGP at V_{Gf} = 0.5 V, V_{GbN} = 0 V (solid red curve) and Z^3-FET at V_{GbN} = 0.5 V (dotted black curve). L_p = L_n = 200 nm, V_{Gb} = V_{GbP} = - 0.5 V and V_A = 0 V.

A simple analytical expression of the $\Phi_f(x)$ and $\Phi_b(x)$ potential distributions along the channel of silicon Z^2-FET was derived. The results obtained from the compact model were compared to TCAD simulations and exhibit a very good agreement. The surface potential was also computed for other members of Z-FET family devices (Z^2-FET DGP and Z^3-FET) and plotted against the standard Z^2-FET surface potential. The barrier in L_p region is similar for all Z-FET variants while the strongest L_n barrier belongs to Z^2-FET with DGP. As a perspective, the surface potential values could serve to calculate the current in different Z-FET devices regimes.

3.5. Conclusion

A complete DC measurements set of band-modulation devices with promising results was presented in this chapter. These measurements showed that Z-FET structures feature an adjustable triggering voltage, low leakage current, large hysteresis and high current ratio I_{ON}/I_{OFF}. The high current performance of these devices was also explored with TLP characterization, showing a good robustness against ESD events that is suitable for 1.0 V, 1.8 V and 3.3 V applications. Stacked architectures of band-modulation devices with hybrid-bulk SCR were reported, featuring high capability of sustaining current especially against HBM ESD event. Finally, a compact analytical model of potential distribution over the whole channel of Z^2-FET was developed. It was successfully compared to TCAD simulations. The model was extended to other members of Z-FET family. The model shows a good accuracy and is valid for short and long devices in weak and strong inversion/accumulation regimes.

3.6. References

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Chapter 4. Z-FET Devices as 1T-DRAM and Logic Switch

SUMMARY

4.1. Introduction

Sharp switch and large hysteresis characteristics of Z-FET devices were the motivation of searching for other applications beside of ESD protection [1–7]. In this Chapter, band-modulation structures are investigated as capacitor-less dynamic random access memories (1T-DRAM [8–13]) and logic switches in advanced FDSOI nodes. The memory operation principle is detailed and confirmed with TCAD simulations [14]. Promising experimental results were obtained.

4.2. Capacitor-less Dynamic Random Access Memory: 1T-DRAM Application

Can we store and read simultaneously a bit of information in a single transistor without using an external storage capacitor? The answer lies at devices with isolated silicon channel (discussed in Chapter 1). They offer, in the form of charges, bit storage in the floating body, which is also used to read the memory state. As they are not entirely convincing, existing 1T-DRAM versions are not commercialized yet. While some of them consume relatively high power during writing mode [10, 15, 16] , other variants suffer either from super-coupling (beyond t_{Si} = 10 nm) [9, 17–20] or technology constraints [21–23]. To address these issues, we propose the Z^2-FET as a novel 1T-DRAM cell, which is fully compatible with 14 nm and 28 nm FDSOI fabrication process.

4.2.1. Operation Principle

In conventional 1T-DRAM, the shift of threshold voltage due to the excess or absence of holes in the body indicates the existence of a memory effect [24]. In Z-FET devices, the triggering voltage V_{ON} displacement caused by the presence (or not) of mobile charges (electrons) under the front-gate points to the same effect. The front-gate controlled hysteresis (Figure 4.1-b) achieved within low anode and front-gate voltage range paves the way for designing low-power 1T-DRAMs with Z^2-FET architecture (Figure 4.1-a).

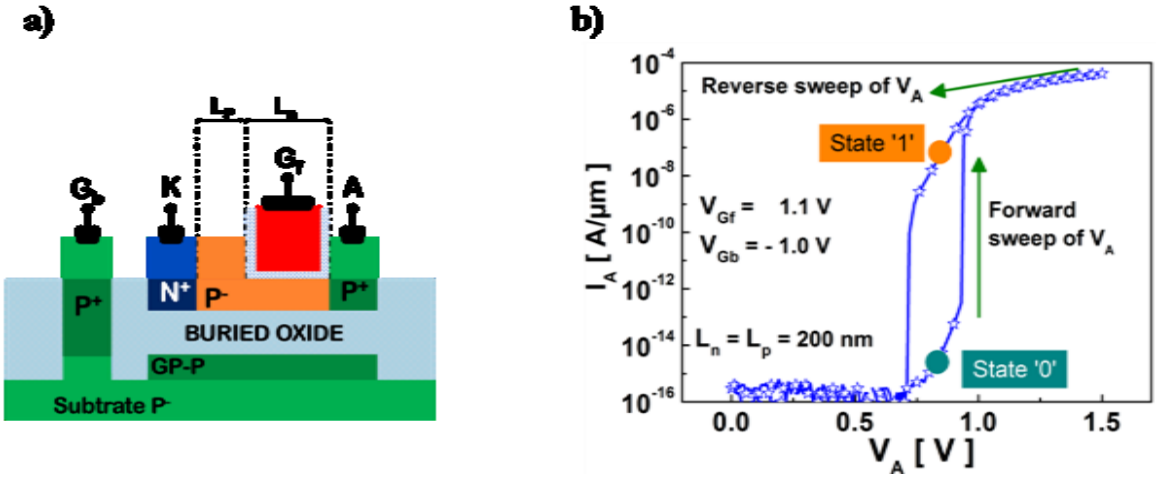

Figure 4.1. (a) Cross-section view of Z^2-FET in 28 nm FDSOI technology. (b) I_A-V_A curve showing gate-controlled hysteresis in 28 nm Z^2-FET with $L_n = L_p$ = 200 nm at various V_{Gf} and V_{Gb} = - 1 V.

Once the device quasi-static characteristics was recorded, transient measurements useful for practical applications were considered. The Z^2-FET capability as a dynamic memory cell was checked by applying a simple transient pattern, as shown in Figure 4.2. Four main operations summarize the Z^2-FET functionality as 1T-DRAM, as described below.

- **Write "0" (W_0)**

The pattern starts by applying front-gate and anode biases (V_{Gf} = 1.2 V and V_A = 0 V). Then, programming the state "0" ("Erasing", in other words) consists of lowering V_{Gf} down to 0 V while keeping V_A = 0 V. In this case, accumulated electrons under the front-gate are evacuated from L_n region into the anode.

- **Write "1" (W_1)**

The mechanism of writing "1" in Z^2-FET is simple and does not depend on impact ionization [10, 25], band-to-band tunneling [9, 26, 27] or gate tunneling current [28]. In this mode, the Z^2-RAM is forced to operate as a forward-biased PIN diode with high current (I_A = 26 μA/μm in Figure 4.2). For that purpose, the L_n barrier should be eliminated by setting the front-gate pulse to 0 V and embedding it in a V_A pulse that triggers the flow of carriers from node to node. Electrons are stored again under the front-gate.

- **Hold state**

In order to maintain as long as possible the present cell state, the front-gate voltage should be returned into its high value and V_A to 0 V. After W_0, the remained electrons are not sufficient to form an inversion layer under the gate. Thus, the device enters in non-equilibrium state (deep depletion like effect, detailed in the next subsection) inducing a strong barrier in L_n region [29]. Conversely, while holding "1", the barriers are lower implying V_{ON} reduction. Since the electrons are numerous, the diode is at equilibrium conserving infinitely the state "1" of the memory cell.

- **Read state (R_0 and R_1)**

The Z^2-FET memory response on anode pulse, when reading, depends on its previous state. After writing "0", the gated region of Z^2-FET is depleted from electrons featuring a strong L_n barrier and high triggering voltage V_{ON}. Hence, the anode pulse in this case ($V_A < V_{ON}$) cannot

trigger the positive feedback and turn on the device. A very low anode current is obtained (I_0 ~ 1nA/µm in Figure 4.2.). On the other hand, when reading "1", the V_A pulse is able now to collapse the barriers, previously lowered in writing mode, and turn on the diode with high I_1 current (I_1 = 26 µA/µm).

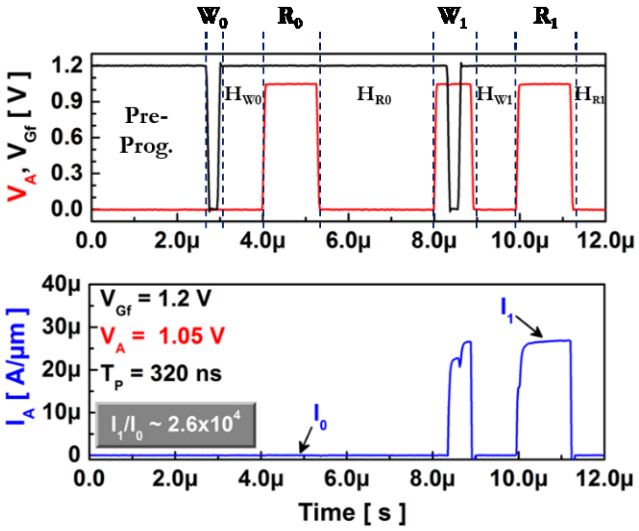

Figure 4.2. Experimental bias pattern applied to front-gate (black line) and anode (red line) at V_{Gf} = 1.2 V, V_A = 1.05 V and V_{Gb} = - 1 V with T_P = 320 ns. Z^2-FET in 28 nm FDSOI node with L_n = L_p = 200 nm.

4.2.2. Memory Operation Analysis via TCAD Simulation

Thanks to TCAD simulations, a deep analysis of the Z^2-FET operation as capacitor-less DRAM is carried out in this sub-section. Promising results are presented. It is shown that with reduced anode voltage for logic "1" writing, the power consumption is significantly reduced. Read/write operations can be achieved with 1 ns pulse widths. Also, understanding why the device could lose its "0" state is succeeded by monitoring the concentration of carriers and surface potential. Finally, the properties of GO1 (thin gate oxide) Z^2-FET memory are examined.

4.2.2.1. Detailed Explanation of Z^2-RAM Operation Principle

The state of the Z^2-FET at each critical memory step was studied via numerical simulations with the set of parameters given in Chapter 2 (section 2.2.2.1). Experimental results were confirmed by the simulated current window (I_1-I_0), which is equal to 25 µA/µm (Figure 4.3). In the following, the memory operation is detailed by monitoring the surface potential, carrier concentration and total current density in the two parts of the channel.

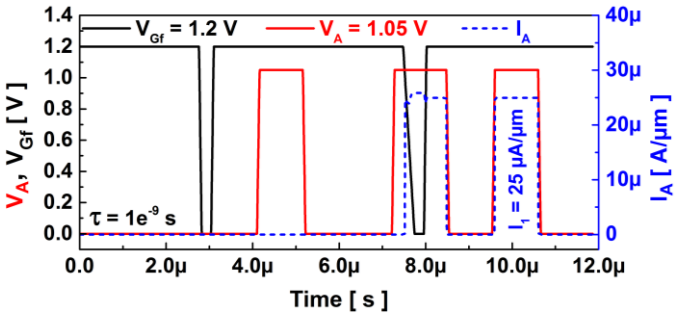

Figure 4.3. Bias pattern and corresponding current in simulated Z²-FET memory at V_{Gf} = 1.2 V, V_{Gb} = - 1 V and V_A = 1.05 V. L_p = L_n = 200 nm.

The pattern starts with **initial bias** on anode and front-gate terminals (V_A = 0 V and V_{Gf} = 1.2 V). The back-gate is biased negatively (V_{Gb} = - 1 V). At this **pre-programming** state, the gated region (L_n) of the Z²-FET is strongly inverted (~ 10^{18} cm^{-3}, red circle symbols in Figure 4.4-b) while the holes are firmly accumulated in L_p part (~ 10^{18} cm^{-3}, blue square symbols in Figure 4.4-c). This implies a steady state in the body of Z²-FET with high barriers as indicated in Figure 4.4-a. The sudden increase of minority carriers (holes) in the gated region when writing **"W_0"** (10^{15} cm^{-3}, Figure 4.4-c) explains the great reduction of holes injection barrier shown in Figure 4.4-a. At **"W_0"**, the front-gate is grounded and all subsisting electrons in this region are evacuated (10^6 cm^{-3}, red circle symbols in Figure 4.4-b). They tend to come again under the gate, once V_{Gf} returns to its high value, but still are not sufficient to form the inversion layer (10^{12} cm^{-3} at **"H_{W0}"** in Figure 4.4-b), which pushes the Z²-FET to enter in a non-equilibrium state. Comparing to the stationary state at the beginning of the bias pattern, the concentration of carriers in the gated region is lower enabling higher energy barriers as in the deep depletion mode of a MOS capacitor [29]. The high barriers oppose the carrier injection from the anode/cathode terminals into the body and increase the turn-on voltage. That is why, despite marginal changes in carrier concentrations, the **"R_0"** reading anode pulse ($V_A < V_{ON}$) does not produce the device triggering resulting in a very low I_0 current.

Although the electron concentration under the gate continues to attempt increasing at **"Hold R0"** (10^{16} cm^{-3} in Figure 4.4-b), the holes injection barrier remains constant (Figure 4.4-a). Conversely, due to electrons density decrease in L_p part, the electrons injection barrier is strengthened up (black curve at **"H_{R0}"** in Figure 4.4-a). As V_A increases and V_{Gf} is brought to 0 V, the injection barriers are demolished and carriers are massively injected into the body (10^{18} cm^{-3} at **"W_1"** in Figure 4.4-b, c). After this action, the front-gate voltage returns to its positive value collecting available carriers in the channel, which explains the higher electrons density at **"Hold W_1"** state compared to **"Hold W_0"** situation (10^{17} cm^{-3} >> 10^{12} cm^{-3}, Figure 4.4-b). The high

number of electrons available under the gate lowers the holes injection barrier in this region and makes the difference between **"0"** and **"1"** states. Unlike **"R_0"**, the V_A pulse for reading **"R_1"** is now able to collapse the barriers (Figure 4.4-a) and turn on the Z^2-FET allowing a high flow of carriers in the channel (Figure 4.4-b, c).

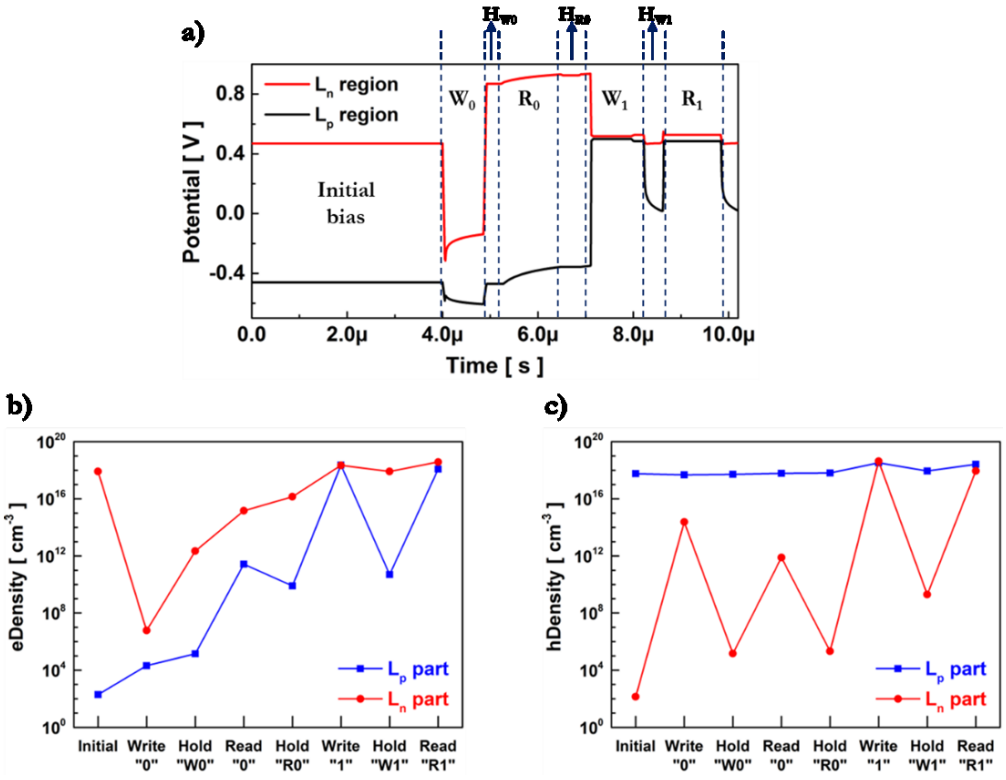

Figure 4.4. (a) Simulated surface potential profile versus time, (b) electrons and (c) holes densities for Z^2-FET operating as 1T-DRAM. (Cut was taken at y = 1 nm under the gate).

The total currents during critical "1" and "0" writing and reading memory processes are illustrated in Figure 4.5. Since the drain voltage is zero at "W_0", the current does not flow in the channel (Figure 4.5-a). The electron-less L_n part, after W_0, features a strong barrier in this region and does not permit the anode pulse to read "0", collapse the barriers and turn on the diode. The result can be seen in Figure 4.5-b where the current I_0 is negligible. On the other hand, programming the state "1" demands a positive drain bias and zero front-gate bias (V_{Gf} = 0 V). In this case, the Z^2-FET acts as a forward-biased PIN diode with a high flow of current as indicated in Figure 4.5-c. The obtained current density in Figure 4.5-d is a consequence of barriers collapse and carriers flow from node to node due to a positive V_A pulse.

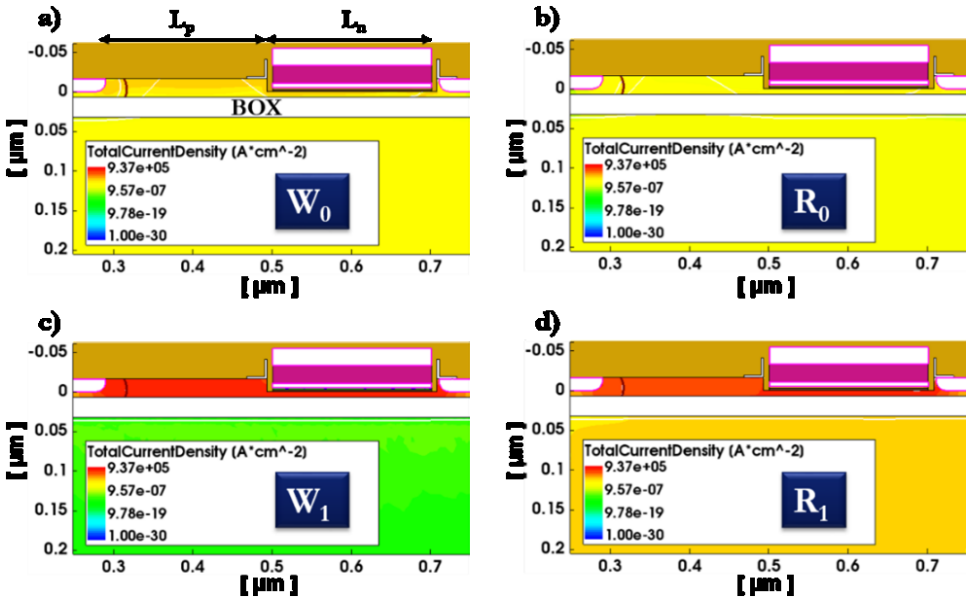

Figure 4.5. Total current density for simulated Z²-FET (L_p = L_n = 200 nm) during (a) writing "0", (b) reading "0", (c) writing "1" and (d) reading "1". V_{Gf} = 1.2 V, V_{Gb} = - 1 V and V_A = 1.05 V.

4.2.2.2. Reduced Power Consumption

The capability of reducing Z²-FET DRAM power consumption is presented in Figure 4.6 [30, 31]. Decreased anode voltage for logic "1" writing ($V_{A(W1)}$ = 0.4 V in blue) limits the flow of carriers in the channel, implying a negligible current, and significantly reduces the power consumption during the writing operation of the single-transistor DRAM. The action does not affect the read current that still offers a remarkable sense margin (I_1-I_0 = 25 µA/µm, dotted blue curve). This feature is unrivalled by any competing DRAM, ReRAM, STRAM or PCRAM memory technology. In contrast, I_1 disappears for lower $V_{A(W1)}$ < 0.4 V because not enough electrons can be secured at the gate (dotted red curve in Figure 4.6, $V_{A(W1)}$ = 0.1 V).

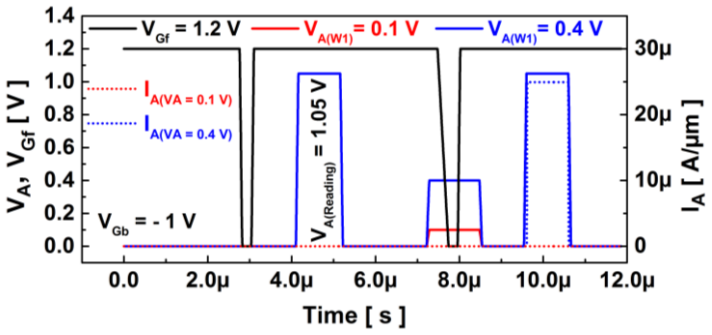

Figure 4.6. Memory bias scheme and its response in simulated Z²-FET to limit the power consumption when programming "1" at V_{Gf} = 1.2 V, V_{Gb} = - 1 V and $V_{A(Reading)}$ = 1.05 V.

Electrons concentration and surface potential extracted after writing (H_{W1}) and during reading (R_1) state "1" are plotted in Figure 4.7. Despite using low anode voltage $V_{A(W1)}$ = 0.4 V for programming logic "1", sufficient electrons are still stored under the front-gate (blue curve in Figure 4.7-a), thus reducing the potential in this region (blue curve in Figure 4.7-b). The read anode voltage $V_{A(Reading)}$ = 1.05 V collapses the weak holes injection barrier (blue curve in Figure 4.7-d) inducing a high flow of carriers in the channel (Figure 4.7-c), which is the reason of remarkable current sense margin obtained in Figure 4.6. Reinforced potential at $V_{A(W1)}$ = 0.1 V (red curve in plotted in red, Figure 4.7-b), due to the reduced number of electrons captured by the gate capacitance, can explain the absence of I_1 current (dotted red curve in Figure 4.6). At "R_1", the anode pulse is unable to collapse the strong barrier (Figure 4.7-d).

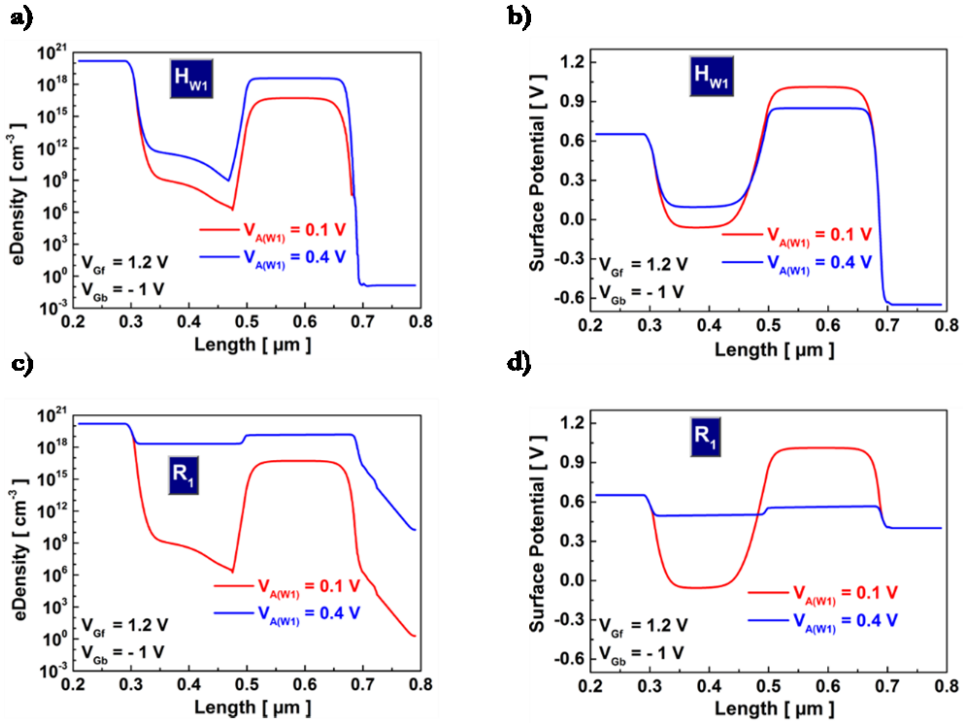

Figure 4.7. Simulated electrons density and surface potential for Z²-FET DRAM extracted for the bias scheme in Figure 4.6 for logic "1" (a, b) holding "H_{W1}" and (c, d) reading "R_1".

4.2.2.3. High Access Speed

The discharge current $\Delta Q_{Gf}/\Delta t$ is a key feature of Z²-FET single-transistor DRAM [8]. Basically, the memory readout operation does not depend only on the charge stored under the gate but also on how fast the front-gate capacitance is discharged. In simulation, the read/write times reach 1 ns, easily outperforming conventional DRAM (Figure 4.8).

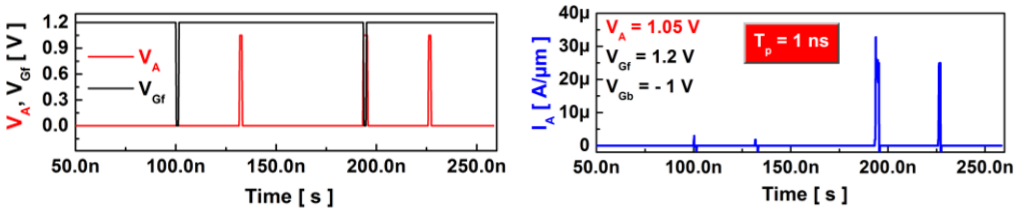

Figure 4.8. Simulated Z²-FET ($L_n = L_p$ = 200 nm) dynamic RAM features very fast access time. T_P = 1 ns

4.2.2.4. Retention Time

Unlike state "1", which is stable and does not need to be refreshed, holding "0" information in the body of Z²-FET is a critical problem. To understand the mechanism of the proposed 1T-DRAM when storing logic "0", helpful simulation results are discussed in this paragraph. The computed value of "0" state retention obtained with transient experiments is presented later in this chapter. Three simulation methodologies for "0" retention time are proposed. The first one presented in Figure 4.9-a consists of maintaining high V_{Gf} for 10 ms after setting "0" at the beginning of the bias scheme (inset of Figure 4.9-a). As $V_A = 0$ V, the increased number of electrons under the front-gate noticed in Figure 4.9-b are supplied by carrier generation. As a result, the accumulated electrons lower the potential in the gated region inducing a weaker holes injection barrier not capable to resist the anode reading pulse. Thus, the "0" data is lost. This operation mode provides approximatively the real "0" retention time of Z²-FET DRAM.

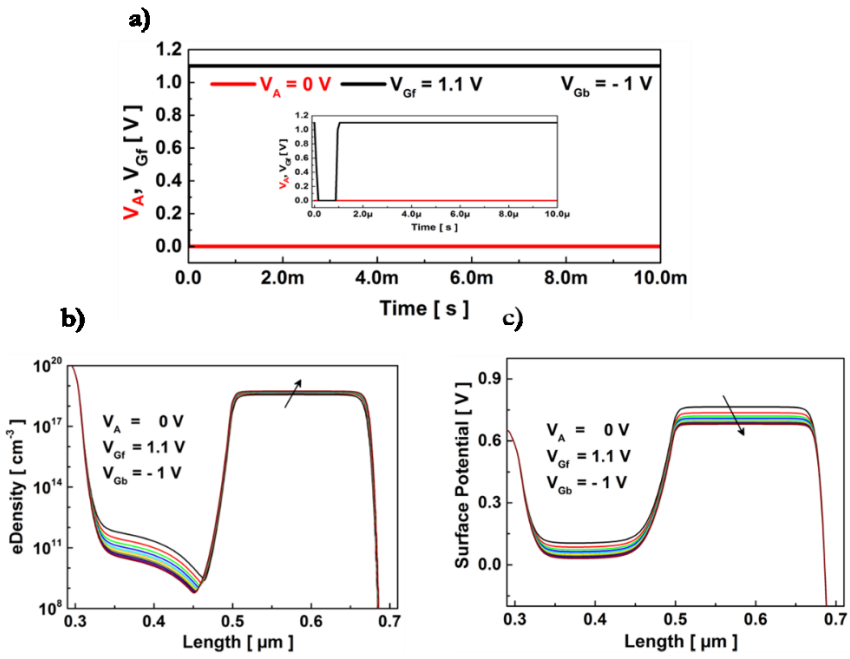

Figure 4.9. (a) Waveform of anode and front-gate pulses applied to Z²-FET. Evolution of (b) electrons density and (c) surface potential during hold "0" operation for 10 ms. $V_A = 0$ V, $V_{Gf} = 1.1$ V and $V_{Gb} = -1$ V.

The second strategy used to evaluate "0" retention time is schemed in Figure 4.10-a. After "0" programming, a set of many regular fast pulses is send to the anode of Z^2-FET with a period of 500 ns (Figure 4.10-b). The idea is to observe the behavior of DRAM cell after each V_A read signal. Normally, frequent reading of logic "0" improves the retention time as the accumulated electrons under the gate are swept into the anode (self-refresh). This can be seen in Figure 4.10-c, d where the concentration of electrons decreases slightly implying stronger barrier in the gated region. However, the electron injection barrier in L_p region tends to increase due to the flow of parasitic holes after each V_A pulse, which eventually would trigger the positive feedback and highly affect the retention time.

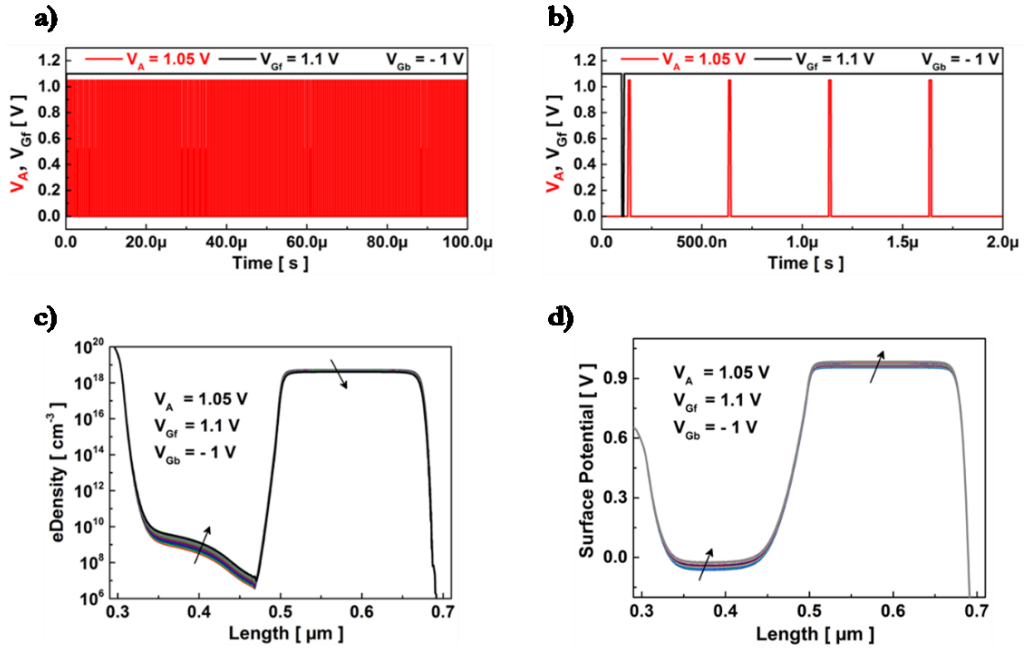

Figure 4.10. (a) Global and (b) zoom view of repetitive anode pulses applied to Z^2-FET after programming "0" state for 100 µs. (c) Electrons concentration and (d) surface potential evolution after each V_A pulse. V_A = 1.05 V, V_{Gf} = 1.1 V and V_{Gb} = - 1 V.

Results presented in Figure 4.11 (3rd operation mode) are not considered to evaluate the real "0" retention time as a long V_A pulse is applied to Z^2-FET after programming logic "0" (inset of Figure 4.11). Simulations were carried out to confirm that a continuous V_A reading highly improves the retention time of state "0". Carrier concentration does not evolve during the whole bias pattern giving rise to a stable surface potential and almost an infinite "0" state holding time.

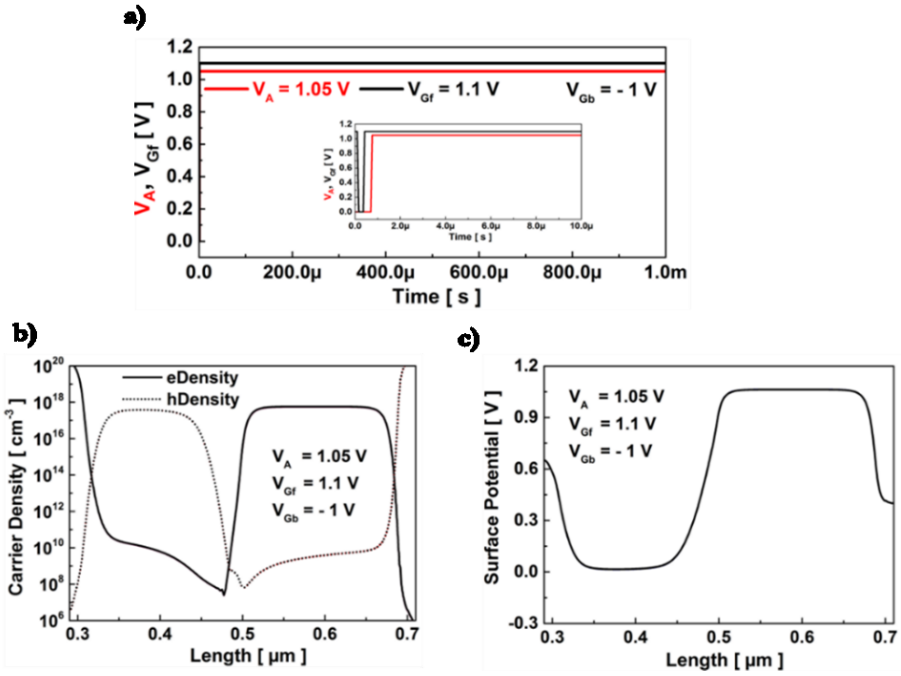

Figure 4.11. Bias pattern applied to Z²-FET DRAM for logic "0" retention evaluation. Change of (a) carrier concentration and (b) surface potential during 1 ms of "0" hold. V_A = 1.05 V, V_{Gf} = 1.1 V and V_{Gb} = - 1 V.

4.2.2.5. GO1 Z²-FET with Thin Gate-Oxide

Operating nearly and even under 1 V of supply voltage is a wish of every memory cell developer. This goal is almost achieved with thin gate-oxide (GO1) Z²-FET. Figure 4.12 shows that the front-gate, now controlling better the channel, can be decreased down to 1.05 V without affecting the memory operation. The current sense margin obtained at V_A = 1.05 V is still remarkable (I_1 = 26 µA/µm).

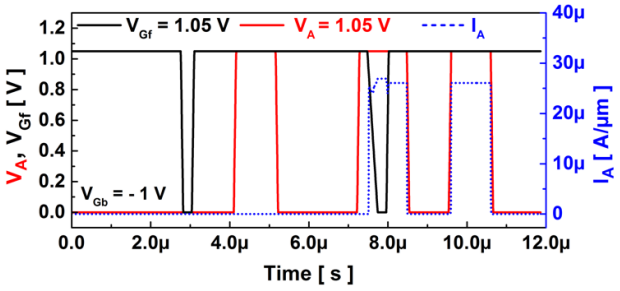

Figure 4.12. Bias scheme applied to ultra-thin oxide GO1 Z²-FET and its current response at V_{Gf} = 1.05 V, V_A = 1.05 V and V_{Gb} = - 1 V. L_n = L_p = 200 nm.

The memory operation was investigated in details with TCAD simulations. In the following, experimental results of advanced FDSOI Z-FET devices are presented in a wide range of temperature.

4.2.3. Measurement Bench

Transient measurements were carried out using Cascade S300-based semi-automatic test bench monitored by "Nucleus" software, Agilent B1530A waveform generator/fast measurement unit (WGFMU), which is a plug-in module for the Agilent B1500A semiconductor device analyzer, connected to two remote-sense and switch units (RSU) by special composite cables (1.5 m) and DC probe card (Figure 4.13). The WGFMU provides two operation modes: fast current or voltage measurement mode (Fast IV) and pulse generator mode (PG mode). Following connections were used:

- RSU connected to the anode operating in Fast IV mode, which is able to create arbitrary waveforms via the ALWG function and measure at the same time the anode current.
- RSU connected to the front-gate working in PG mode and creating narrow voltage pulses.

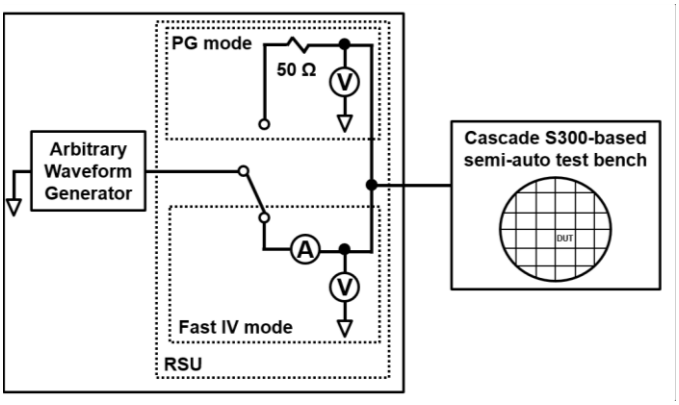

Figure 4.13. Instruments assembly schematic used for measuring band-modulation devices in transient mode as capacitor-less DRAMs.

The specifications and limitations of WGFMU recommended by the equipment manufacturer are presented in Table 4.1. As capacitor-less DRAM cells are asked to respond very fast, the 10 mA current measurement range with minimum rise/fall time and pulse width was chosen to test Z-FET devices.

		Min Rise/Fall Time			Min Pulse Width			Settling Time		
Current Measurement Range (mA)		0.1	1	10	0.1	1	10	0.1	1	10
Operation mode	PG	30 ns			170 ns			-		
	Fast IV	600 ns	250 ns	80 ns	1.6 µs	500 ns	180 ns	1 µs	250 ns	100 ns

Table 4.3. Minimum rise/fall time, pulse width and recommended settling time for different current measurement regimes in two operation modes of WGFMU.

4.2.4. Transient Experimental Results

In this section, band-modulation devices are demonstrated experimentally in 28 nm and 14 nm FDSOI nodes as low power/voltage 1T-DRAM embedded memories [30–33]. Retention time and memory margins at room and high temperature are presented, revealing the high performance of band-modulation devices as single-transistor memory. In addition, the impact of additional ground plane (in Z^2-FET DGP) and SiGe layer (in Z^3-FET) on memory behavior for enhanced power consumption is outlined. Finally, the ability of setting 1T-DRAM matrix with Z^2-FET is also studied.

4.2.4.1. Z^2-FET as 1T-DRAM in 28 nm FDSOI Technology

a. Memory Margin

The hold-write-hold-read bias pattern applied on 28 nm Z^2-FET and corresponding readout current are shown in Figure 4.14. To program the "1" and "0" states, electrons are stored (or not) under the positively biased front-gate. Memory readout consists in discharging C_{Gf} with anode pulse. Grounding the front-gate while maintaining a low anode voltage (V_{Gf} from 1.25 V to 0 V and V_A = 0 V) is used for "0" state programming. Since the electrons were eliminated from the gated region ("0" state), the anode reading pulse cannot collapse the enforced L_n barrier. Hence, a nearly zero discharge current is obtained (I_0 ~ 1 nA/µm, Figure 4.14). Forcing the device to act as a forward biased PIN diode (V_{Gf} = 0 V and V_A = 1.1 V, W_1 in Figure 4.14) permits the flow of carriers in the channel inducing a high current. At this moment, the front-gate collects and stores free electrons forming relatively weak potential profile in this region (see also Figure 4.4-a). The anode reading pulse (V_A = 1.1 V) is able now to collapse the barriers featuring high I_1 current (I_1 = 46 µA/µm).

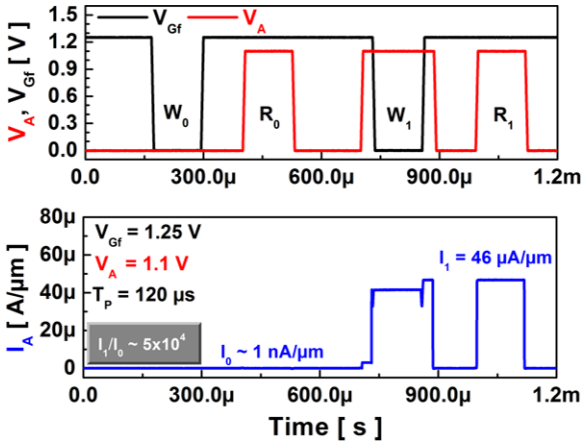

Figure 4.14. Bias pattern used for Z²-FET memory operation and corresponding experimental anode current at V_{Gf} = 1.25 V, V_{Gb} = - 1 V and V_A = 1.1 V with programming pulse T_P = 120 µs. L_p = L_n = 200 nm.

Similar results are presented in Figure 4.15-a with shorter programming and reading pulses width (T_P = 320 ns). The memory effect appears in Z²-FET at low anode voltage with moderate I_1 current that increases with anode voltage V_A (Figure 4.15-b). However, I_0 reading current meets I_1 when V_A approaches the front gate bias V_{Gf} (V_A = 1.2 V and V_{Gf} = 1.25, black square symbols in Figure 4.15-b). The high anode pulse crashes the gated barrier (not strong enough) and turns on the device (no more memory effect). The solution is to increase V_{Gf} from 1.25 V up to 1.4 V, which reinforces the potential in this region avoiding barriers collapse.

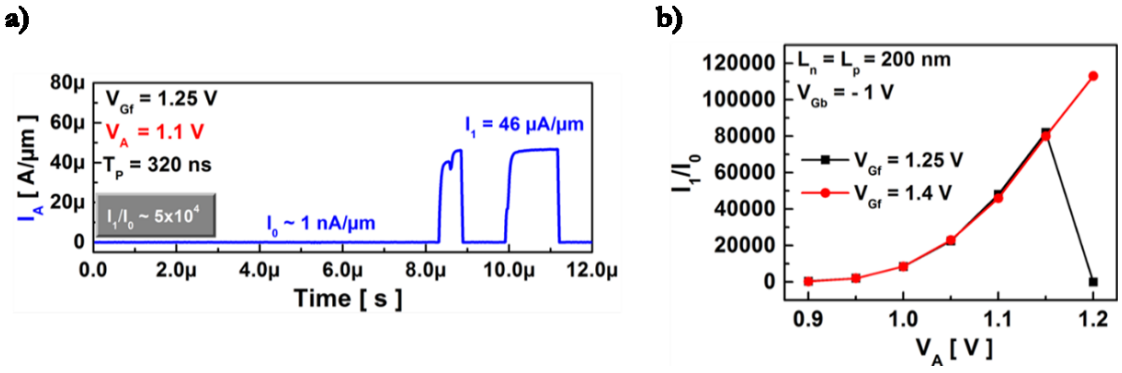

Figure 4.15. (a) Anode current I_A obtained at V_{Gf} = 1.25 V and V_A = 1.1 V with short programming pulse width T_p = 320 ns. (b) Current margin I_1/I_0 variation with V_A for V_{Gf} = 1.25 V and 1.4 V. V_{Gb} = - 1 V.

As discussed before in section 4.2.2.2, the memory readout operation does not depend on the charge stored under the gate but on how fast we can access the memory cell. Figure 4.16 shows the device response on anode bias with two different rise time (RT = 30 ms and 3 µs in Figure 4.16-a, b respectively). For V_A slightly lower than $V_{ON(DC)}$, the long anode pulse cannot unblock the device (Figure 4.16-a). However, decreasing the anode pulse rise time stimulates the capacitance

discharging mechanism, which this time turns on the device, implying a higher I_A current (I_A = 18 µA/µm in Figure 4.16-b).

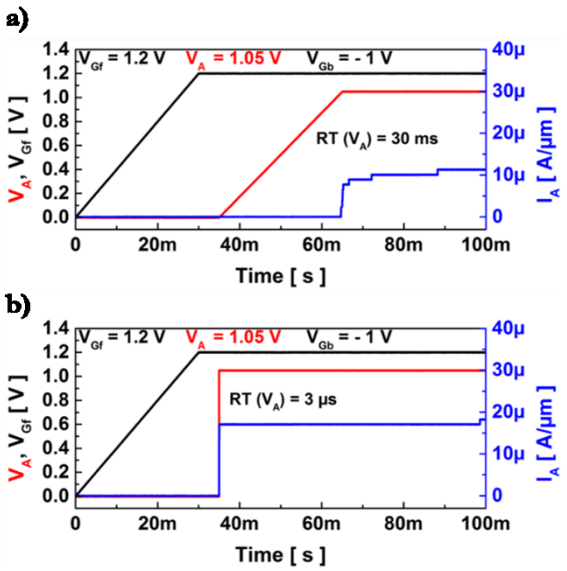

Figure 4.16. Impact of anode pulse rise time on read I_A current at V_{Gf} = 1.2 V, V_{Gb} = - 1 V and V_A = 1.05 V. (a) Rise time RT = 30 ms and (b) RT = 3 µs.

Based on TCAD simulations and results obtained in Figure 4.16, a low-voltage writing scheme of state "1" was proposed to reduce the power consumption of Z²-FET operating as 1T-DRAM. As shown in Figure 4.17-a, the writing anode voltage $V_{A(W1)}$ is reduced from 1.05 V (blue dotted line) down to 0.5 V (red solid line). The program "1" current becomes almost negligible and significantly reduces the power consumption during the writing operation of the single-transistor DRAM. Despite using a much decreased $V_{A(W1)}$, sufficient electrons are still stored under the gate lowering the L_n barrier. The read anode voltage $V_{A(Reading)}$ = 1.05 V collapses the weak holes injection barrier offering a similar high current margin (I_1-I_0 = 26 µA/µm). For lower $V_{A(W1)} \leq$ 0.35 V, I_1 starts decreasing and disappears at $V_{A(W1)} \leq$ 0.3 V (Figure 4.17-b, c). However, increasing the anode voltage reading enhances the current margin. This can be seen in Figure 4.17-c, where the difference between read and write "1" currents is still significant despite the low-voltage "1" programming state (I_{R1} - I_{W1} = 45 µA/µm for $V_{A(W1)}$= 0.3 V, blue square symbols).

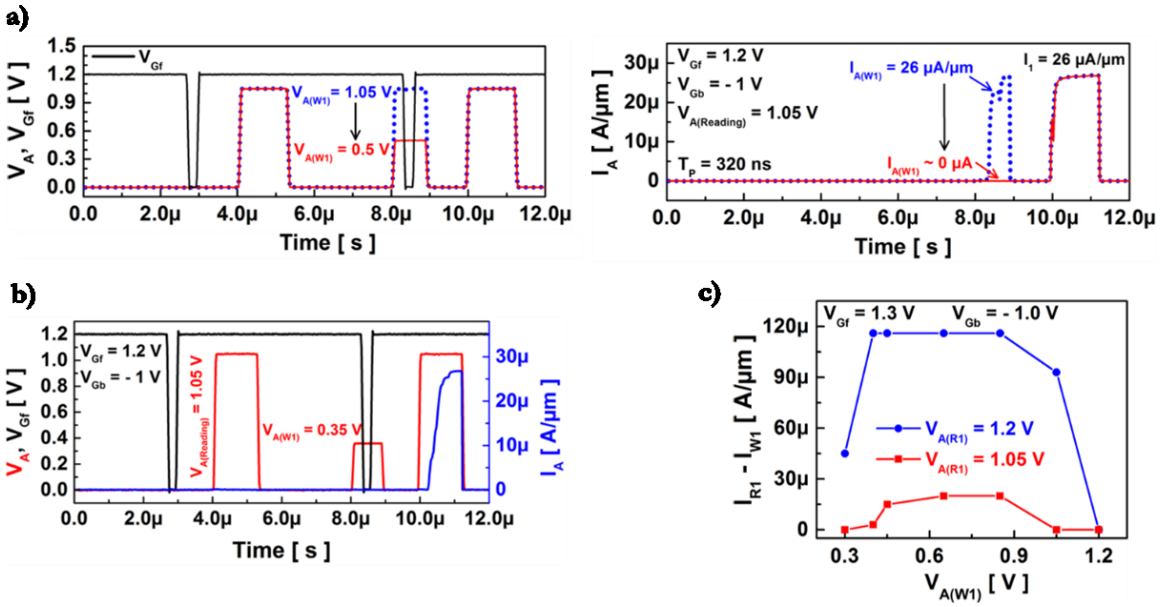

Figure 4.17. Memory bias scheme and its response to limit the power consumption when programming "1" at V_{Gf} = 1.25 V, V_{Gb} = - 1 V and $V_{A(Reading)}$ = 1.05 V. (a) $V_{A(W1)}$ = 0.5 V and (b) $V_{A(W1)}$ = 0.35 V. (c) Evolution of reading and writing current difference (I_{W1}-I_{R1}) with programming anode voltage $V_{A(W1)}$ at V_{Gf} = 1.3 V, V_{Gb} = - 1 V for two different reading voltages $V_{A(R1)}$ = 1.05 V (red square symbols) and $V_{A(R1)}$ = 1.2 V (blue circle symbols).

b. Retention Time

Z^2-FET features a stable "1" state with no need to be refreshed. The only matter of single-transistor DRAM is how long the "0" state can be maintained before it degrades. Two experimental different modes were used to extract logic "0" retention time: hold-read "0" operation (Figure 4.18) and continuous "0" reading (Figure 4.20). At V_{Gf} = 1.2 V and V_A = 1.05 V (Figure 4.18-a), the "0" state degrades to stabilize after 1.5 ms (I_0 = 10 µA/µm) but still lower than I_1 = 26 µA/µm (Figure 4.17-a). Normally, frequent anode pulses improve the retention time by eliminating accumulated electrons under the gate. However, the reinstalled electrons under the front-gate, during hold stage, lower the energy bands in this region allowing the passage of holes into the body. Hence, V_A pulses are able now to collapse the L_n barrier implying a "0" state degradation. Higher V_{Gf} raises up the potential in L_n region and stops holes injection from anode resulting in enhanced "0" retention time as illustrated in Figure 4.18-b.

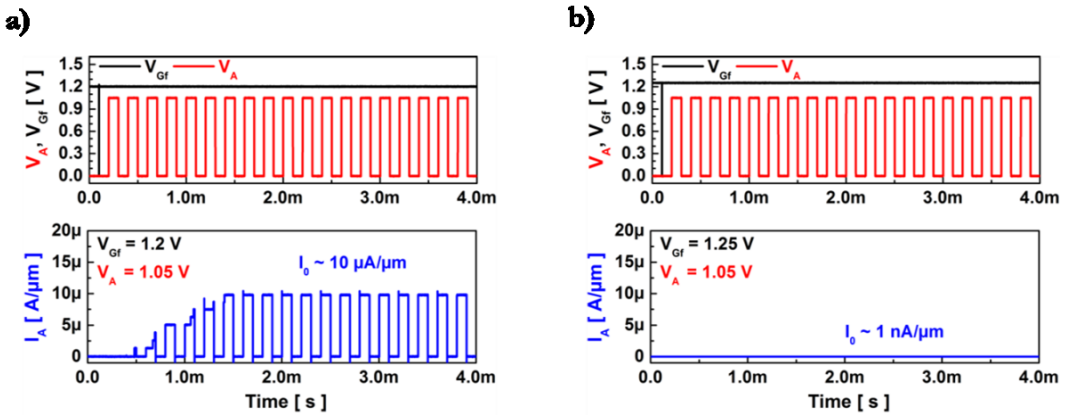

Figure 4.18. Logic "0" retention time for 4 ms in hold-read stage at V_A = 1.05 V and V_{Gb} = - 1 V. (a) V_{Gf} = 1.2 V and (b) V_{Gf} = 1.25 V.

As it improves the holes injection barrier, state "0" holding duration increases with front-gate bias. When V_A approaches from V_{Gf}, the "0" state is lost rapidly (~ 250 µs, black square symbols in Figure 4.19) with remarkable I_0 current (7 µA/µm). At slightly higher V_{Gf}, the "H_0" period becomes long (> 4 ms) and I_0 current is suppressed.

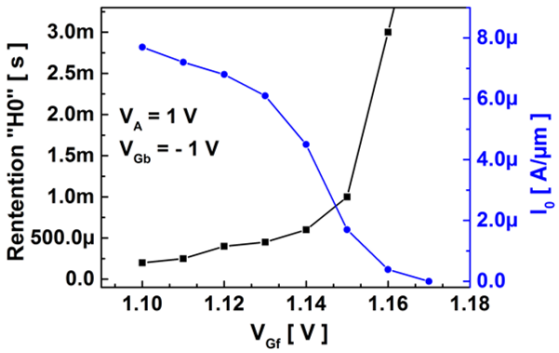

Figure 4.19. Evolution of logic hold-read "0" retention time and I_0 current with front-gate bias at V_A = 1 V and V_{Gb} = - 1 V.

The second method for measuring "0" state retention time is presented in Figure 4.20. The bias scheme applied to Z^2-FET consists first of logic "1" programming and read followed by writing "0" and continuous reading with a long V_A pulse (550 ms, Figure 4.20-b). The device benefits from long anode pulse to eliminate the accumulated electrons under the front-gate featuring high retention time without any degradation (t_{re} = 500 ms, Figure 4.20-a).

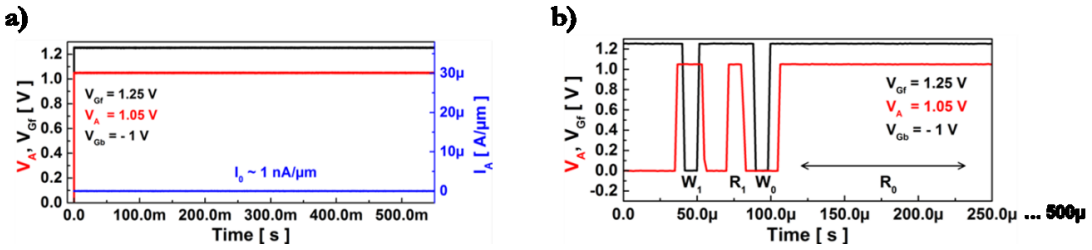

Figure 4.20. (a) Logic "0" retention time for continuous reading for 550 ms at V_A = 1.05 V, V_{Gb} = - 1 V and V_{Gf} = 1.25 V. (b) Anode and front-gate pulses schemes applied at the beginning of the retention bias pattern.

c. High Temperature Operation

The sensing margin and retention time at T = 85 °C are highlighted in Figure 4.21 and Figure 4.22. I_1 almost doubles (I_1 = 43 µA/µm in Figure 4.21-a) for same V_A and V_{Gf} bias as Figure 4.17-a. The carrier generation rate increases at high temperature, which affects the injection barriers. Despite "0" writing and eliminating the accumulated electrons under the gate, the anode pulse can turn on the device, thus implying a higher I_0 current. This issue can be solved by increasing the front-gate bias that reinforces the L_n barrier and reduces or stops the flow of holes into the channel. In addition, the anode bias can be reduced at high temperature, still maintaining a respectable sensing margin ($I_1/I_0 = 2.3 \times 10^4$ for V_A = 1 V, red square symbols in Figure 4.21-b). For higher V_A, the current ratio increases in both cases but collapses earlier at T = 85 °C (Figure 4.21-b).

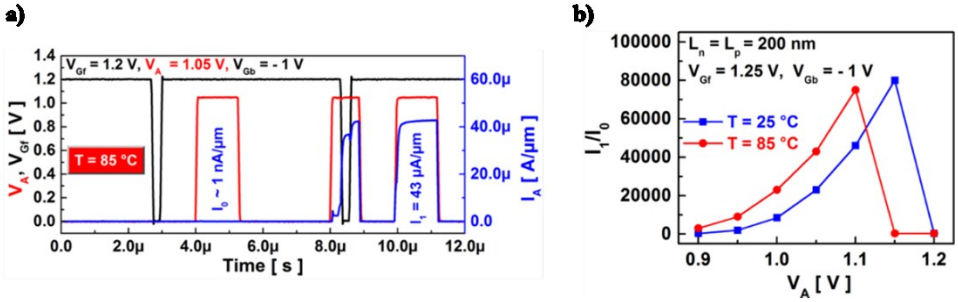

Figure 4.21. (a) High temperature experimental results for Z²-FET DRAM operating at V_{Gf} = 1.2 V, V_{Gb} = - 1 V and V_A = 1.05 V. (b) Comparison of current ratio I_1/I_0 at room temperature and T = 85 °C in terms of anode voltage V_A at V_{Gf} = 1.25 V and V_{Gb} = - 1 V. L_n = L_p = 200 nm.

Figure 4.22 shows the "0" retention time at high temperature. As discussed before, the gated barrier at V_{Gf} = 1.2 V is relatively weak and cannot withstand anode voltage bias V_A = 1.05 V for long time implying a high I_0 current (I_0 = 43 µA/µm in Figure 4.22-a, b). The retention time is improved by increasing V_{Gf} (Figure 4.22-a, b). The gated barrier retrieves its height and I_0 is almost suppressed.

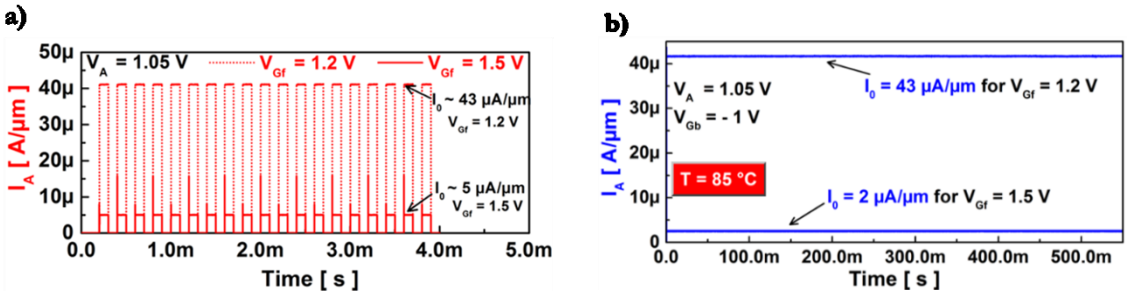

Figure 4.22. Experimental "0" state retention time at V_A = 1.05 V, V_{Gb} = - 1 V and various V_{Gf} for (a) 4 ms in hold-read mode and (b) 550 ms in continuous read mode. T = 85 °C.

In the following, promising experimental results obtained at room temperature for band-modulation devices in the most advanced FDSOI technology are presented.

4.2.4.2. Z-FET Single-Transistor DRAMs in 14 nm FDSOI Technology

a. Z²-FET

Standard Z²-FET with thin silicon film (t_{Si} = 12 nm) was experimentally tested in 14 nm node as 1T-DRAM. The reduction of BOX and gate oxide thicknesses offers a better electrostatic control of the thin channel. Hence, the memory effect in Z²-FET appears at lower V_{Gf} and zero back-gate V_{Gb} biases. Compared to 28 nm node, the injection barriers in 14 nm device are stronger and are not totally collapsed with V_A = 1.05 V. In this case, the "1" reading current is lower (I_1 = 5 µA/µm in Figure 4.23 < 26 µA/µm in Figure 4.17-a). Improving the state "1" current requires a V_A pulse that overpasses the front-gate bias and be able to collapse the L_n barrier (Figure 4.17-b).

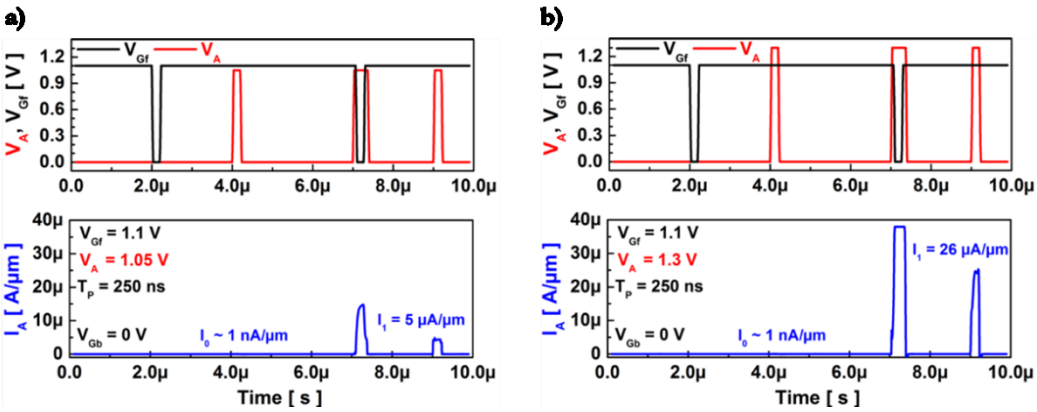

Figure 4.23. Bias pattern used for Z²-FET memory operation in 14 nm node with L_p = L_n = 200 nm and corresponding anode current at V_{Gf} = 1.1 V, V_{Gb} = 0 V, (a) V_A = 1.05 V and (b) V_A = 1.3 V. Short programming pulse width, T_P = 250 ns.

Figure 4.24-a shows that, at V_{Gb} = 0 V, the memory effect disappears in both short and long devices (138 nm < 200 nm < 350 nm) with comparable I_1 and I_0 currents at all anode voltages (Blue circle and black square symbols are superimposed, Figure 4.24-a). After applying a negative back-gate bias, devices retrieve their operation as 1T-DRAM cells at certain V_A values (V_{Gb} = - 1 V, Figure 4.24-b). Actually, the two devices do not benefit from back-gate bias in the same manner. While V_{Gb} < 0 V reinforces the weak L_p barrier in short Z^2-FETs, it reduces by coupling effect the L_n barrier in long devices and V_A can now collapse it (for example V_A = 1.25 V in long Z^2-FET, Figure 4.24-b). It is noticed that the device downscaling improves the current sense margin (note that the saturation of I_0 and I_1 in short devices is due to the current compliance imposed by used equipment).

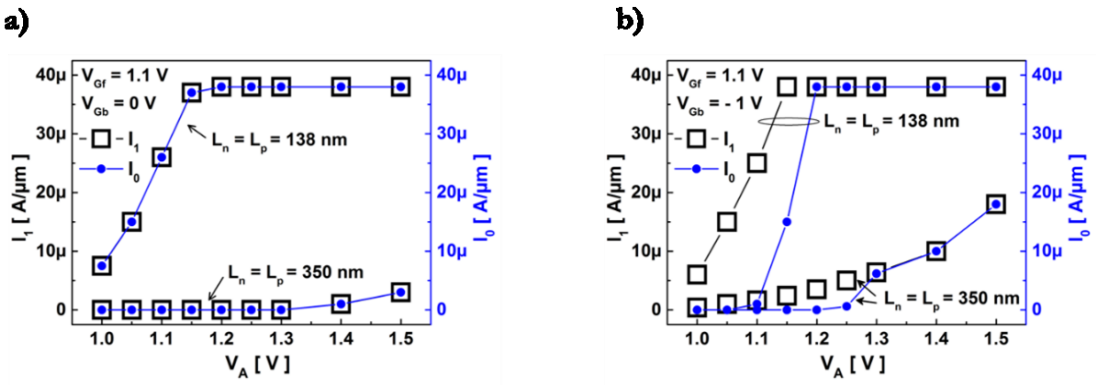

Figure 4.24. Evolution of I_1 (left y axis, black square symbols) and I_0 (right handed y axis, blue circle symbols) with anode voltage V_A bias for two different Z^2-FET device lengths at V_{Gf} = 1.1 V (a) V_{Gb} = 0 V and (b) V_{Gb} = - 1 V.

b. Z^2-FET DGP

As it cooperates with the front-gate and reinforces the barrier in this part, the GP-N tolerates the aggressive downscaling of the gated region beyond 100 nm without affecting the device behavior. Figure 4.25 presents promising results of short Z^2-FET DGP (L_n = 90 nm, L_p = 150 nm) as single-transistor DRAM where the L_p barrier is strong with no need of negative back-gate bias. The current sense margin is remarkable at nearly V_{dd} bias (I_1 = 23 µA/µm for V_A = 1.15 V).

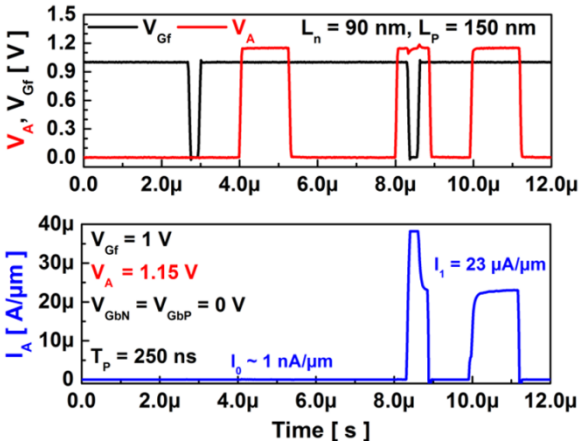

Figure 4.25. Bias pattern applied to Z²-FET DGP with L_n = 90 nm, L_p = 150 nm and corresponding anode current at V_{Gf} = 1 V, V_{GbN} = V_{GbP} = 0 V and V_A = 1.15 V. Short programming pulse width, T_P = 250 ns.

The power consumption while writing logic "1" can be also reduced in Z²-FET with dual ground planes (see Figure 3.6, Chapter 3). Figure 4.26 shows the variation of I_1 current after applying reduced anode voltage for programming state "1". We can see that decreasing $V_{A(W1)}$ does not only eliminate the program "1" current but also affects, beyond 0.7 V, the "1" read current that almost disappears at $V_{A(W1)}$ = 0.5 V.

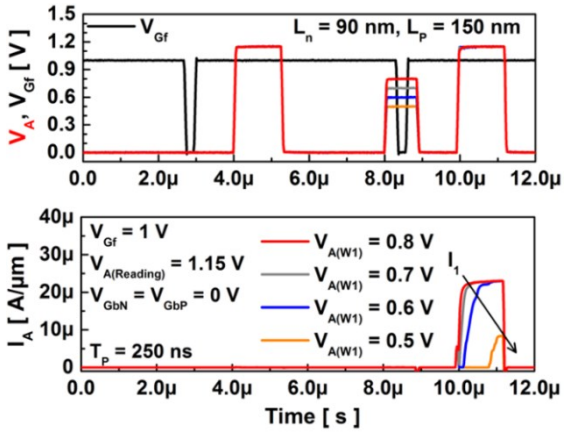

Figure 4.26. Memory bias scheme and its response to limit the power consumption for Z²-FET DGP when programming "1" by applying reduced anode writing voltage $V_{A(W1)}$ at V_{Gf} = 1 V, V_{GbN} = V_{GbP} = 0 V and $V_{A(Reading)}$ = 1.15 V.

The presence of GP-N underneath the front-gate tolerates V_{Gf} bias lowering, which is a sound feature for ultra-low power memory operation. However at reduced V_{Gf} = 0.95 V and V_{GbN} = 0 V, the I_0 current starts to increase (I_0 = 17 µA/µm in Figure 4.27). Increasing the GP-N bias eliminates the unwanted "0" state read current but slightly affects I_1. The reinforced L_n barrier reduces the flow of holes induced by the anode reading voltage implying a lower I_1 current that is still reasonable (I_1 = 17 µA/µm).

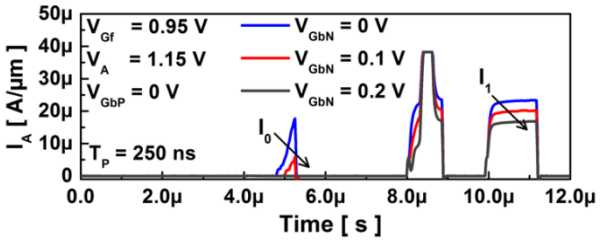

Figure 4.27. Impact of GP-N bias on short Z²-FET DGP operating as 1T-DRAM at V_{Gf} = 0.95 V, V_A = 1.15 V and V_{GbP} = 0 V. L_p = 150 nm and L_n = 90 nm.

c. Z³-FET

The strained Z³-FET variant with SiGe body (Figure 3.16, Chapter 3) features outstanding results operating as ULP (Ultra Low Power) capacitor-less DRAM. As the barriers are weaker in combined silicon-germanium body, the reduced anode reading voltage V_A = 1.05 V is able to easily inject more holes with improved mobility (thanks to SiGe) into the channel inducing high I_1 current (I_1 = 38 µA/µm in Figure 4.28). As the downscaling is limited by the space charge region of buried diode formed by the two GPs (P and N, see section 3.2.2.1.c), the SiGe Z³-FET cannot compete other 1T-DRAM variants but still it is a viable candidate for ULP memory/fast logic combined with various applications such as bio, light and radiation sensing.

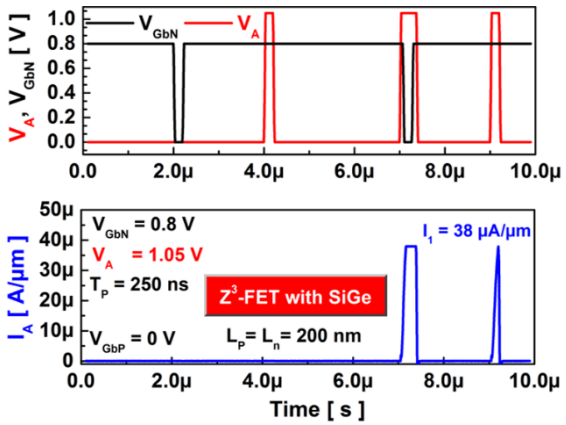

Figure 4.28. Memory bias scheme applied to Z³-FET with SiGe body and its response at V_{GbN} = 0.8 V, V_{GbP} = 0 V and V_A = 1.05 V. L_p = L_n = 200 nm.

The evolution of "1" and "0" state currents with GP-N bias of all-Si and SiGe Z³-FET variants at various anode voltage V_A is highlighted in Figure 4.29. Compared to Z³-FET with purely silicon channel, the device with SiGe body features superior I_1 current at low and high V_A (Figure 4.29-a, b). The "0" state current is comparable for both structures at low V_A for all V_{GbN} bias (Figure 4.29-c) while eliminating the parasitic "0" current at increased V_A requires a greater GP-N bias in

Z^3-FET with SiGe channel (Figure 4.29-d). Actually, the SiGe barriers are weak and more sensitive to anode voltage bias. The current margin I_1/I_0 is exceptional for both structures.

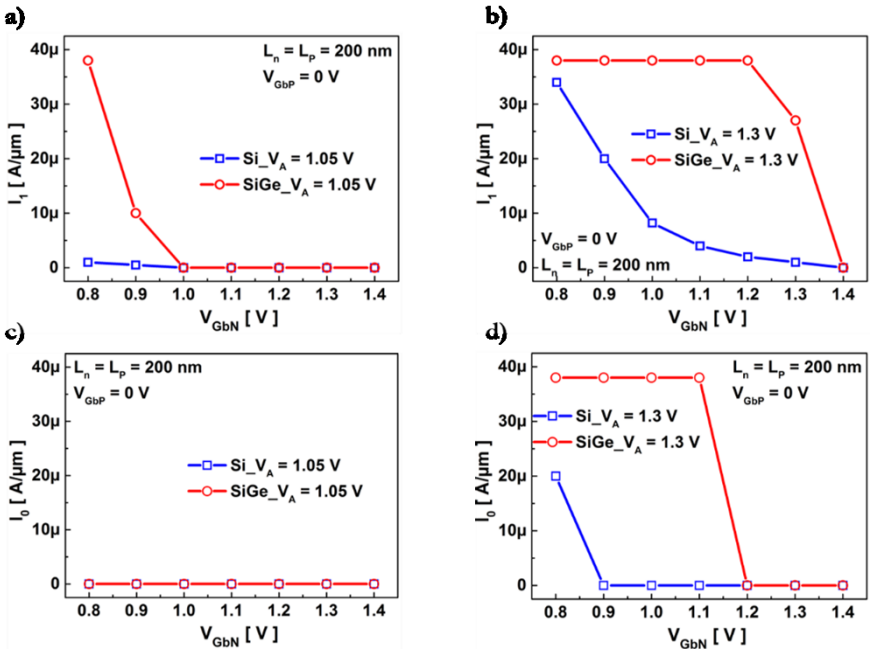

Figure 4.29. Comparison of I_1 and I_0 currents between Si and SiGe Z^3-FETs for various GP-N bias at V_{GbP} = 0 V, (a, c) V_A = 1.05 V and (b, d) V_A = 1.3 V. The saturation of I_1 and I_0 currents at V_A = 1.3 V is due to equipment current compliance.

The barriers are narrow in short devices and need to be strengthened. For that purpose, a negative GP-P bias is applied to Z^3-FET with $L_p = L_n = 150$ nm (Figure 4.30-a) and $L_p = L_n = 138$ nm (Figure 4.30-b). The I_1 current obtained at V_A = 1.1 V and V_{GbN} = 0.8 V is attractive for both variants. However, downscaling the structure enhances the response to V_A pulse. Compared to Z^3-FET with $L_p = L_n = 150$ nm, the "1" reading current of 138 nm variant is larger (I_1 = 26 µA/µm in Figure 4.30-b > I_1 = 20 µA/µm in Figure 4.30-a).

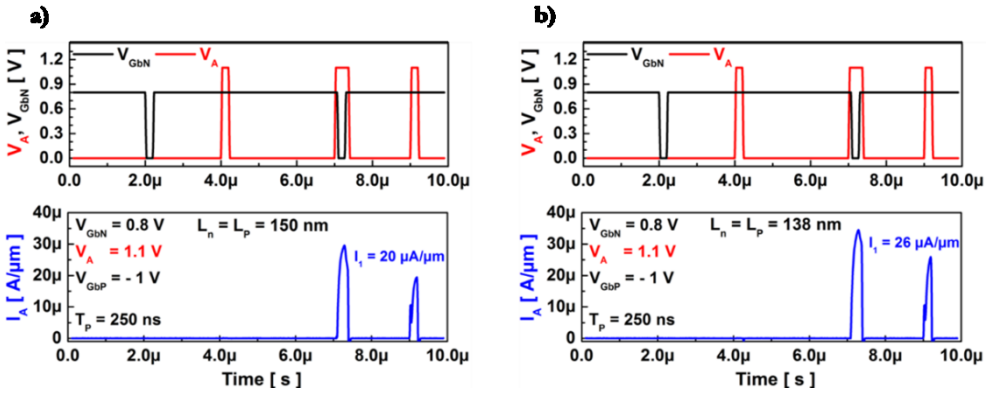

Figure 4.30. Bias pattern applied to Z^3-FET at V_{GbN} = 0.8 V, V_{GbP} = - 1 V and V_A = 1.1 V with (a) $L_n = L_p$ = 150 nm and (b) $L_n = L_p$ = 138 nm.

4.2.5. Z²-FET Memory Cell in a Matrix

The elementary Z²-FET memory cell (1T-DRAM) scheme is given in Figure 4.31. The cathode (N^+) is connected to the Select Line (SL) with first level of metal (M1) while a second metal level (M2) links the anode (P^+) to the Bit Line (BL). The front-gate polysilicon plays the role of the Word Line (WL).

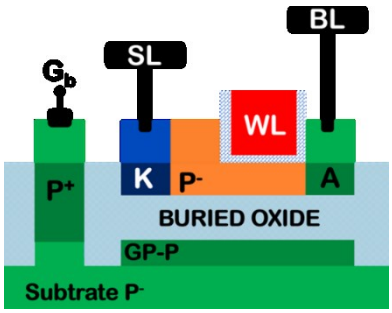

Figure 4.31. Schematic representation of 28 nm FDSOI technology Z²-FET as capacitor-less DRAM in a matrix context.

The successful demonstration of Z²-FET (in previous sections) as an elementary dynamic memory cell was the motivation to test the device in a matrix environment. For this reason, an array composed of four Z²-FETs (2x2) was designed and fabricated using relaxed 28 nm FDSOI design rules (Figure 4.32). Normally, the read/write operation on a selected cell should not cause information failure or disturbance of other cells sharing the same V_A and V_{Gf} signal lines. N-type MOS transistor was added at the end of each row (connected to the cathode of Z²-FETs) preventing the flow of unwanted current that could disorder the state of other memories sharing the same bit line. As it is perpendicular to both parallel word and select lines, the bit line offers a selective "1" writing operation. In contrast, programming logic "0" is still an issue as it depends only on V_{Gf} bias. If the front-gate signal switches off, all memory cells participating the same word line are set to "0". This information loss requires a memory state refresh. Logic "0" programming operation is preceded by a check of cells sharing the same word line and followed by writing "1" where it was stored. Unlike other 1T-DRAM structures [9, 23, 34], the refresh of Z²-FET is not power-consuming, which is an excellent feature (see also section 4.2.4.1.a).

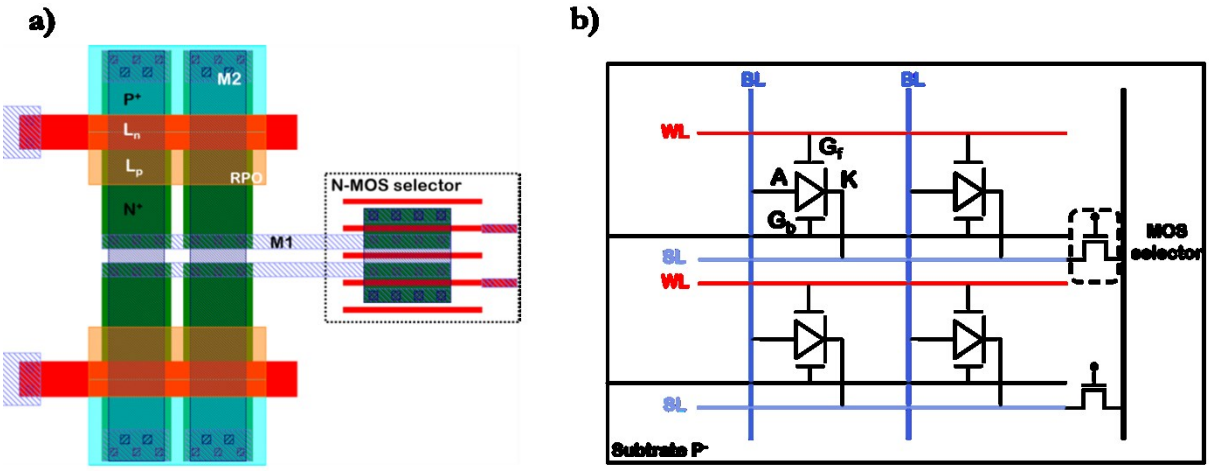

Figure 4.32. (a) Layout and (b) schematic views for 2x2 Z²-FET memory matrix. The active silicon region is in green; the front-gate (L_n) in red; the RPO layer in orange defines the ungated region (L_p); the cyan blue anode is connected to BL with M2 (dark blue) while the cathode (no color) and N-type MOS selector are linked with M1 (light blue).

As the integration density of DRAM cells is an important factor, another matrix was designed with reduced size, but without reaching the minimal 28 nm FDSOI design rules. The layout presented in Figure 4.33 consists of 2x2 1T-DRAM array using Z²-FET devices. This time and for more density integration, the MOS selector was distributed and connected to the cathode of each Z²-FET sharing the same select line. The area of the Z²-FET bit cell is given by:

$$A_{Z^2-FET} = (W + L_{RX}) . (L_{source} + L_s + L_{poly-RPO} + L_p + L_n + L_{poly-contact}) \quad (4.35)$$

The width of Z²-FET structure is defined by W, L_{RX} is the space between two adjacent silicon active zones, the length of the MOS source is delimited by L_{source}, L_s is the selector transistor length and $L_{poly-RPO}$ and $L_{poly-contact}$ stand for the distance between the polysilicon and Resist-Protection-Oxide layer (RPO) from a side and the via contact from other side respectively. L_n (gated part) and L_p (ungated part) define the length of Z²-FET.

Compared to DRAM developed by TSMC at the same technology node [35], the area of the designed Z²-FET (L_p = 200 nm and L_n = 120 nm in Figure 4.33) is eight times larger (0.286 µm² > 8 × 0.035 µm²). The selector transistor (L_s = 48 nm) is an essential element in this matrix but it negatively affects the bit cell area. Improving the surface depends not only on downscaling the Z²-FET but also on the large distance between polysilicon and silicide-block layer ($L_{poly-RPO}$). With scaled Z²-FET (L_p = L_n = 138 nm) using minimum design rules of 28 nm FDSOI node, the bit cell area ratio shrinks down to 0.08 µm² offering a large integration density D_{mm^2} = 11.93 Mb/mm² (~ 2.2 times < 27.24 Mb/mm², which is the integration density of 28 bulk

planar eDRAM [35]). The estimation of D_{mm^2} without taking into account peripheral circuitry (current sense amplifier SA, drivers/decoders lines …) can be expressed by:

$$D_{mm^2} = \frac{1}{A_{Z^2-FET} \cdot 1Mbits} \tag{4.36}$$

In order to be competitive, the Z²-FET overall length should be below 200 nm and all L_{source}, $L_{poly\text{-}RPO}$ and $L_{poly\text{-}contact}$ spaces must not exceed 40 nm. We believe we can achieve this goal with the novel Z²-FET with additional GP-N. As the front-gate is reinforced by GP-N, it tolerates the aggressive downscaling. The short experimentally tested Z²-FET DGP (L_p = 150 nm, L_n = 90 nm) features, with minimum $L_{x\text{-}x}$ distances, a remarkable integration density D_{mm^2} = 20.5 Mb/mm².

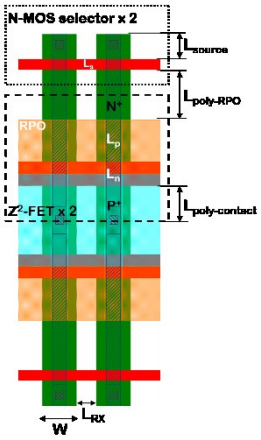

Figure 4.33. Layout view of 2x2 Z²-FET memory matrix with distributed N-type MOS selector. The MOS transistor and Z²-FET share the source (N^+).

In addition to all presented features and even if they exhibit larger bit cell area, the reduced processing cost and simplicity of band-modulation devices will be the motivation of using them as embedded 1T-DRAM (eDRAM).

4.3. Z²-FET DGP as a Logic Switch in 14 nm node

The presence of hysteresis in band-modulation devices is beneficial as they can be used as ESD protection and capacitor-less dynamic memories. In this section, transient experiments were carried out, showing the possibility of eliminating, in particular conditions, the typical hysteresis and turn off Z-FET devices once they are triggered.

4.3.1. Transient Experimental Results

Measurements were carried out on Z²-FET DGP ($L_p = L_n$ = 200 nm) in 14 nm FDSOI technology using the same equipment employed for memory tests. The bias scheme for turning off the device is presented in Figure 4.34. It starts with setting the front-gate into an initial value (V_{Gf} = 0.8 V in this case) and switch it into 0 V during 200 ns within a 2 µs V_A pulse width (V_A = 1.15 V). The rise time of signals stands for 60 ns. At V_A = 1.15 V, switching the front-gate bias from 0.8 V down to 0 V turns on the device inducing high I_{ON} current (I_{ON} = 34 µA/µm). Setting back V_{Gf} to its high value cuts off the current and Z²-FET DGP returns into its off state with negligible I_{OFF} current (I_{OFF} ~ 10 nA/µm).

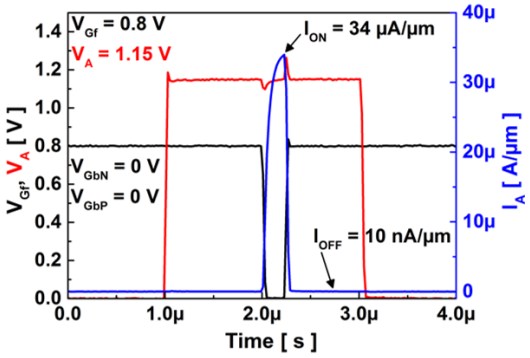

Figure 4.34. Bias scheme applied to Z²-FET DGP operating as a logic switch and corresponding current at V_{Gf} = 0.8 V, V_A = 1.15 V and zero ground plane bias $V_{GbN} = V_{GbP}$ = 0 V. $L_p = L_n$ = 200 nm.

4.3.1.1. Impact of Front-Gate and Anode Biases on I_{ON}/I_{OFF}

Figure 4.35 shows the influence of V_{Gf} and V_A variation on current margin (I_{ON}/I_{OFF}) of logic switch Z²-FET DGP. The device features high I_{ON} current at V_A = 1.1 V and V_{Gf} = 0.3 V (I_{ON} = 22 µA/µm, Figure 4.35-a). But, the barriers are weak at low front-gate bias and behave ineffective due to the massive flow of carriers. As a result, the I_{OFF} current is relatively high even if the gate is set back into its high value. Increasing V_{Gf} reinforces the L_n barrier and thus reduces the parasitic I_{OFF} current to be eliminated at V_{Gf} = 0.6 V without affecting the device on state (gray curve, Figure 4.35-a). The current margin also depends strongly on anode voltage bias. The mechanism of device turn off starts to appear at low V_A = 0.9 V with a moderate current ratio (I_{ON}/I_{OFF} = 65, red curve in Figure 4.35-b). Increasing the anode voltage implies a higher I_{ON} current reaching the equipment compliance at V_A = 1.2 V (I_{ON} = 38 µA/µm, gray curve in Figure 4.35-b). I_{OFF} current stays steady (10 nA/µm).

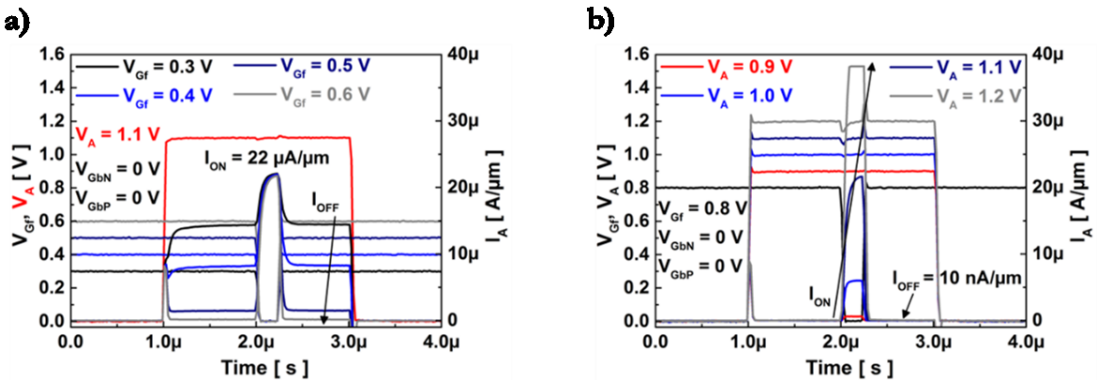

Figure 4.35. Logic switch Z²-FET DGP operation dependency on (a) front-gate bias at V_A = 1.1 V and (b) anode bias at V_{Gf} = 0.8 V. V_{GbN} = V_{GbP} = 0 V.

4.3.1.2. Advantage of Ground Plane N Bias

The N-type ground plane placed underneath the front-gate is extremely beneficial for Z²-FET DGP, allowing a very low logic switch operation. With a positive constant GP-N value, the device can be turned off at just V_{Gf} = 0.4 V. Though, a zero V_{GbN} bias is not sufficient to totally eliminate the current in off state. To enhance the switch off operation, barriers need to be reinforced with V_{GbN} bias. The parasitic I_{OFF} current starts decreasing with GP-N bias and disappears at $V_{GbN} \geq 1$ V. Despite the I_{ON} reduction due to V_{GbN} increase, the device still offers noticeable current margin ($I_{ON}/I_{OFF} \sim 100$).

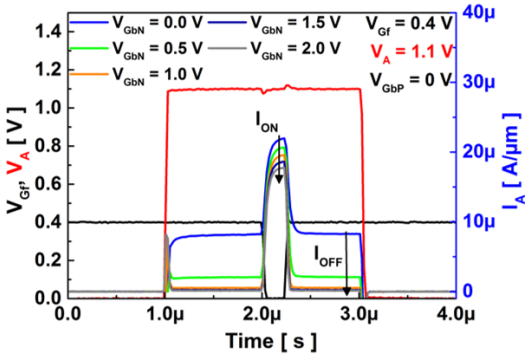

Figure 4.36. Impact of N-type ground plane bias on Z²-FET DGP behavior while operating as logic switch. V_A = 1.1 V, V_{Gf} = 0.4 V and V_{GbP} = 0 V.

4.3.1.3. Device Length Effect on Device Switch ON

Results of short and long Z²-FET DGP operating as ON-OFF switches are presented in Figure 4.37. Decreasing the device length is always beneficial as it offers less occupied silicon surface on chip. It also increases the current. Despite the larger I_{ON} current obtained in short Z²-

FET DGP ($L_n = L_p = 138$ nm), the high I_{OFF} current (due to weak barriers) negatively affects it I_{ON}/I_{OFF} ratio, which is enhanced in large structure ($I_{ON}/I_{OFF} \sim 10^3$ for $L_n = L_p = 350$ nm).

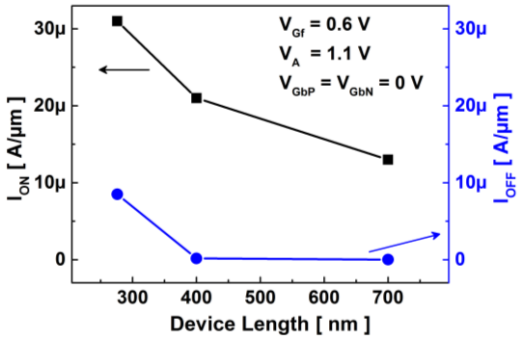

Figure 4.37. Evolution of I_{ON}/I_{OFF} current ratio with Z²-FET DGP device length at $V_{Gf} = 0.6$ V, $V_A = 1.1$ V and $V_{GbP} = V_{GbN} = 0$ V.

The Z²-FET DGP turn off, demonstrated successfully with transient signals, can be also achieved with static DC measurements (see section 3.2.2.1.d). Hysteresis, which is useful for 1T-DRAM operation, was eliminated in band-modulation devices offering an excellent current cut-off. The constant GP-N bias reinforces the gated barrier allowing an ultra-low voltage operation. This feature is unique at Z²-FET DGP making the present novel device highly recommended as a logic switch.

4.4. Conclusion

Band-modulation devices in most advanced FDSOI technologies have been presented as promising architectures for future embedded capacitor-less DRAM (eDRAM) applications. The Z²-FET memory operation principle was deeply analyzed using TCAD simulations. Understanding the device response when holding "0" state was achieved by monitoring the carrier concentration and surface potential. Thanks to the small gate capacitance, the programming/reading time can be reduced to 1 ns. Thinning the gate oxide features a better electrostatic control of L_n region offering a reduced front-gate bias. In addition, experimental results of 28 nm FDSOI Z²-FET as dynamic RAM cell were described. The device brings forward a remarkable current sense margin and high "0" retention time in a wide range of temperature. In 14 nm node, Z-FET devices with stronger barriers can operate with grounded GP bias. Furthermore, the additional GP-N in Z²-FET DGP tolerates the downscaling of the gated part beyond 100 nm, without affecting the device behavior. Combining germanium with silicon in the body allows an ultra-low voltage memory operation (nearly 1 V) with very high current. The power consumption reduction, which is peerless for other

1T-DRAM variants, was also demonstrated. A 2x2 matrix array was fabricated using minimum design rules of 28 nm FDSOI technology. It features acceptable integration density, which can be further improved with device scaling. Finally, logic switch operation was also addressed. Eliminating the hysteresis of Z-FET structures at certain conditions was achieved allowing successful device turn off with high current margin.

4.5. References

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Conclusion and Perspectives

This study was aimed at exploring the concept and applications of **band-modulation devices in 14 nm and 28 nm FDSOI technology nodes**. In this context, a review of alternative variants has been given showing the possibility of obtaining a swing switch lower than SS = 60 mV/decade, the nightmare of MOSFET transistor. While the abrupt change of some of sharp-switch devices is a result of ferroelectric material polarization, mechanical contact or band-to-band tunneling, the operation mechanism of Z-FET structures relies on **simple electrostatic band-modulation**. They are similar to gated diodes, but operated in forward-bias mode. The injection of holes/electrons from anode/cathode terminals into the channel is prevented by electrostatic barriers formed via front/gate biasing. Once V_A reaches the triggering voltage, the device turns on sharply ($\leq$ 5 mV/decade) to a high current. TCAD simulations were carried out on Z^2-FET structure to explain the different physical mechanisms (Generation/Recombination, Diffusion, non-sustainable continuity between G/R and diffusion currents) governing its static DC operation. We have concluded on the important influence of carrier lifetime.

Extensive DC measurements of **14 nm Z-FET family devices** with different geometries were carried out in a wide range of temperature. **Z^2-FET** features promising results in terms of **sharp-switch, low leakage current, adjustable triggering voltage, large hysteresis and high current I_{ON}/I_{OFF} ratio**. However, the presence of negatively biased P-type Ground Plane ($V_{Gb} < 0$ V) under the whole structure affects by coupling effect the barrier of the gated part and reduces V_{ON}. This undesirable outcome for some applications has been the motivation to propose a novel variant, **Z^2-FET DGP**, with a second GP-N placed underneath the front-gate. The N-type Ground Plane cooperates with the front-gate and enhances significantly the triggering voltage V_{ON}. The third fabricated free-surface (no front-gate) variant, **Z^3-FET**, operates with only back-gates. It features similar sharp-switch characteristics with the possibility of working with high GP voltage bias. The effect of doping one part of the channel and introducing new materials (SiGe) into the body on Z-FET devices parameters has also been highlighted.

Thanks to their attractive characteristics, band-modulation devices can be used for many applications. In this thesis, we focused on:

- **Electro-Static Discharge (ESD) protection**. The high current performance of Z-FET structures was investigated using TLP characterization method. Z^2-FET and Z^3-FET with undoped silicon channel feature high robustness against current discharge events and can fit the ESD window of 1.0 V and 1.8 V according to their different geometries, silicon thickness and front/back gates biases. However, they need external triggering circuit in order to be transparent during the normal operation of protected circuit. The doped Z^3-FET overcomes this issue as it does not need an outer bias. The possibility of using band-modulation devices as triggering elements instead of power components has been underlined. Stacked architectures improve the behavior of classical SCR in bulk technology.
- **1T-DRAM operation**. The hysteresis obtained in static DC measurements indicates the existence of memory effect. In this context, a complete analysis of Z^2-FET operating as 1T-DRAM with very fast access was reported using TCAD simulations followed by exhaustive systematic transient measurements for all Z-FET devices. The memory operation relies on the presence or not of electrons under the front-gate. In 28 nm node, Z^2-FET exhibits remarkable current margin I_1/I_0 and high retention working at nearly 1 V on anode and front-gate terminals but with V_{Gb} = - 1 V. The negative bias on the ground plane is no longer necessary in 14 nm node as the barriers are stronger. However, obtaining similar I_1 current as in 28 nm node requires a higher V_A. The possibility of reducing the power consumption in Z-FET DRAMs is achieved by decreasing the anode voltage when programming "1" state. In addition, short Z^2-FET DGP benefits from the presence of GP-N to lower V_{Gf}. The Z^3-FET with SiGe has also been characterized showing outstanding memory results. As the barriers are weaker, the nearly 1 V anode pulse results in a high current margin. Following the successful demonstration of Z-FET devices as elementary 1T-DRAM, a 2x2 matrix has been designed and fabricated in 28 nm node. The MOS selector added to each select line is essential as it prevents the flow of unwanted current that could disturb the state of other cells. However, it affects negatively the bit cell area. Improving the density of integration requires a severe scaling of Z-FET devices beyond 200 nm. We believe that Z^2-FET DGP can complete this objective.

- **Logic switch**. Transient measurements were performed on Z^2-FET DGP in 14 nm FDSOI technology. We showed that the hysteresis, which is beneficial for Z-FET devices operating as 1T-DRAM and detrimental for logic circuits, can be eliminated in particular conditions. Once it is triggered, the band-modulation device can be turned off successfully with front-gate pulse. The impact of device parameters (V_{Gf}, V_A, V_{GbN}) and length ($L_n + L_p$) on current ratio I_{ON}/I_{OFF} was studied showing the capability of turning off Z^2-FET DGP with only $V_{Gf} = 0.4$ V (if $V_{GbN} > 1$ V).

In order to evaluate the capability of band-modulation devices by designers before fabrication, a full compact model is needed. We proposed an analytical model of surface potential distribution for all Z-FET structures. The potential is calculated separately for each part of Z-FET variant and combined together with electric filed continuity equations at V_{in} (internal voltage node). The model shows a good accuracy and is valid for short and long devices.

After clarifying the static and transient operation principles and demonstrating the superior characteristics of structures investigated in this thesis, the question now is : which device could be adopted and for which application ?

	ESD	1T-DRAM	Logic Switch	ULP applications	Other applications
Z^2-FET	*	**	*	*	*
Z^2-FET DGP	**	**	**		*
Z^3-FET		*	*		**
Z-FET with SiGe		**	*	**	*
Doped Z^3-FET	**				

Table 1. Band-modulation devices and most probable appropriate applications.

According to Table 1, doped Z^3-FET is highly recommended for ESD protection as it does not need an external bias to be transparent during the circuit normal operation. For 1T-DRAM operation, Z^2-FET and Z^2-FET DGP are proposed as competitive variants featuring exceptional current margin and high retention time. If they include SiGe channel they can be used as ULP embedded memories. The logic switch suits best to Z^2-FET with Dual Ground Planes. As it is reinforced by GP-N, the hysteresis can be eliminated easily at low front-gate voltages. The back-gate operated Z^3-FET cannot pursue an aggressive scaling. But, the top surface free from metal gate is very beneficial and makes him a viable candidate for combined memory/sensing applications (bio, light and radiation sensing). Other Z-FET devices can also be used for sensing.

Although this work attempted to provide a detailed study of band-modulation devices, several aspects could not be fully covered. They deserve to be addressed in future investigations:

- Further Z-FET structures optimization and reliability test.
- 1T-DRAM cell array simulation and benchmark.
- Extra transient measurements of SiGe variants for ULP applications.
- Advanced investigation of all structures as logic switch.
- RF characterization and analysis.
- Full compact SPICE model.
- Transfer of band-modulation concept to FinFETs, tri-gate, and nanowires architectures.

To summarize, the work presented in this thesis is a contribution for clarifying the static and transient operation principles of band-modulation devices in UTBB 14 nm and 28 nm technologies. Explored devices are innovative and feature outstanding characteristics. They are highly recommended for ESD protection, ULP embedded 1T-DRAM and logic switch.

Abstract

During the past 5 decades, Complementary Metal Oxide Semiconductor (CMOS) technology was the dominant fabrication method for semiconductor integrated circuits where Metal Oxide Semiconductor Field Effect Transistor (MOSFET) was and still is the central component. Nonetheless, the continued physical downscaling of these transistors in CMOS bulk technology is suffering limitations and has been stopped nowadays. Fully Depleted Silicon-On-Insulator (FDSOI) technology appears as an excellent alternative that offers low-power consumption and improved electrostatic control for MOS transistors even in very advanced nodes (14 nm and 28 nm). However, the 60 mV/decade subthreshold slope of MOSFET is still unbreakable which limits the supply voltage reduction. This motivated us to explore alternative devices with sharp-switching: Z^2-FET (Zero subthreshold slope and Zero impact ionization), Z^2-FET DGP (with Dual Ground Planes) and Z^3-FET (Zero front-gate). Thanks to their attractive characteristics (sharp switch, low leakage current, adjustable triggering voltage and high current ratio I_{ON}/I_{OFF}), band-modulation devices are envisioned for multiple applications. In this work, we focused on Electro-Static Discharge (ESD) protection, capacitor-less Dynamic Random Access Memory and fast logic switch. The DC and transient operation mechanisms as well as the device performance are investigated in details with TCAD simulations and validated with systematic experimental results. A compact model of surface potential distribution for all Z-FET family devices is also given.

Keywords

FDSOI, advanced CMOS, band-modulation devices, electrical characterization, TLP, ESD, 1T-DRAM, logic switch, Z^2-FET, Z^2-FET DGP, Z^3-FET, compact modeling.

Résumé

Durant les 5 dernières décennies, les technologies CMOS se sont imposées comme méthode de fabrication principale pour les circuits semi-conducteurs intégrés avec notamment le transistor MOSFET. Néanmoins, la miniaturisation de ces transistors en technologie CMOS sur substrat massif atteint ses limites et a donc été arrêtée. Les filières FDSOI apparaissent comme une excellente alternative permettant une faible consommation et une excellente maîtrise des effets électrostatiques dans les transistors MOS, même pour les nœuds technologiques 14 et 28 nm. Cependant, la pente sous le seuil (60 mV/décade) du MOSFET ne peut pas être améliorée, ce qui limite la réduction de la tension d'alimentation. Cette restriction a motivé la recherche de composants innovants pouvant offrir des déclenchements abrupts tels que le Z^2-FET (Zéro pente sous le seuil et Zéro ionisation par impact), Z^2-FET DGP (avec double Ground Plane) et Z^3-FET (Zéro grille avant). Grace à leurs caractéristiques intéressantes (déclenchement abrupt, faible courant de fuite, tension de déclenchement ajustable, rapport de courant I_{ON}/I_{OFF} élevé), les dispositifs à modulation de bandes peuvent être utilisés dans différentes applications. Dans ce travail, nous nous sommes concentrés sur la protection contre les décharges électrostatiques (ESD), la mémoire DRAM embarquée sans capacité de stockage, et les interrupteurs logiques. L'étude des mécanismes statique et transitoire ainsi que des performances de ces composants a été réalisée grâce à des simulations TCAD détaillées, validées systématiquement par des résultats expérimentaux. Un modèle de potentiel de surface pour les trois dispositifs est également fourni.

Mots Clés

FDSOI, CMOS avancé, dispositifs à modulation de bandes, caractérisation électrique, TLP, ESD, 1T-DRAM, interrupteur logique, Z^2-FET, Z^2-FET DGP, Z^3-FET, Modélisation compacte.

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