Investigation of hybrid CBRAM/OXRAM non-volatile memories for low consumption and high reliability

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**Etude de mémoire non-volatile hybride
CBRAM OXRAM pour faible consommation
et forte fiabilité**

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Abstract

As Information Technologies (IT) are still growing, memory devices need to evolve to answer IT market demands. Nowadays, new technologies are emerging and are entering the market. Resistive Random Access Memory (RRAM) are part of these emerging devices and offer great advantages in terms of power consumption, performances, density and the possibility to be integrated in the back end of line. However, to be competitive, some roadblocks still have to be overcome especially regarding technology variability, reliability and thermal stability. Their place on memory market is then still undefined. Moreover, as RRAM working principle depends on stack materials and has to be observed at nanometer resolution, switching mechanism understanding is still challenging. This manuscript proposes an analysis of oxide-based CBRAM microscopic working principle based on electrical characterization results and atomistic simulation. Then, an interdependence between RRAM electrical performances as well as material parameters is studied to point out new parameters that can be taken into account to target specific memory applications.

Outline

This manuscript summarizes a 3 years work done in the CEA-Leti advanced memory technologies laboratory. This Ph.D. thesis was focused on an emerging non–volatile memory technology: the oxide-based Conductive Bridge Random Access Memory (CBRAM). With electrical characterization and atomistic simulation work, working principle of this device is investigated and material indicator are studied to bring guidance on a material selection or engineering method to target the best material for a given application.

Chapter I will state the work research context, going through the different emerging memories and the current industrial market. As an introduction to the rest of the manuscript, this chapter will focus on RRAM potential in terms of performances to integrate stand-alone, or embedded or storage class memories. Moreover, as RRAM working principle understanding is still challenging, a current state of switching mechanisms comprehension will be done.

Chapter II will be focused on describing the studied samples and the characterization methods that will be used to address RRAM behavior. This chapter, will serve as basis to all devices tested and experimental results presented in the following of the manuscript.

Chapter III, similarly to chapter II, will serve as a reference for the following of the manuscript regarding atomistic simulation to have more insights about oxide-based CBRAM switching mechanism at the microscopic level. It will describe the involved physics in first principle simulation and explain how results will be used and extracted.

Chapter IV will deal with microscopic mechanism in Al_2O_3-based CBRAM combining electrical characterization and atomistic simulation presented in the two previous chapters. Electrical characterization will be used to study polarization impact on filament formation and atomistic simulations will give results on charged species that could be influenced by electric field. Insights on filament mechanism complexity will be given.

Chapter V will present interdependence between RRAM electrical performances as well as material parameters. Using electrical characterization and simulation to compare several RRAM, new parameters that can be taken into account to target specific applications will be pointed out.

Chapter VI will synthesize results presented in this manuscript. It will focus on mechanisms involved in different oxide-based CBRAM devices and optimization will be discussed in terms of programming conditions and material parameters. Finally, to conclude this work, we will highlight some perspectives to pursue oxide-based CBRAM understanding and target industrial market.

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Chapter 1

RRAM potential in non-volatile memory market: storage class, stand-alone or embedded product?

1.1 Context: Memory market

In a world where Information Technologies (IT) are still growing, memory devices need to evolve to answer IT market demands: more data to store, higher speed to access data, less consumption. Resistive Random Access Memories (RRAM) are part of these evaluated technologies to answer tomorrow challenges and integrate memory chips. For more clarity, this manuscript starts by presenting the market context and the limitation of the actual technologies. There are three types of memories that can be distinguished in the actual memory market: stand-alone memory to store data with high density and low cost, embedded memories used for embedded systems and memory in computing systems hierarchy used to increase speed with a reasonable cost.

1.1.1 Stand-alone memory: a mature technology

Since computers entered our life, the technics used to store information have been shaken up. People want to keep, exchange, data whatever the size: pictures, videos, documents... To answer this demand, a big data storage market has been created and does not stop evolving. Figure 1.1a shows the evolution of data storage since 1986. Although, digital market increase illustrates new technics to store data, offer is still behind customer demands. Due to a strong change in mentality regarding the "Connected

Life [1]" and a great rise in cloud computing [2], the demand of data storage is still exploding today. Figure 1.1b illustrates the evolution of digital data created and exchanged over ten years which shows an exponential growth over time.

(a) Evolution of Data storage since 1986 [3].
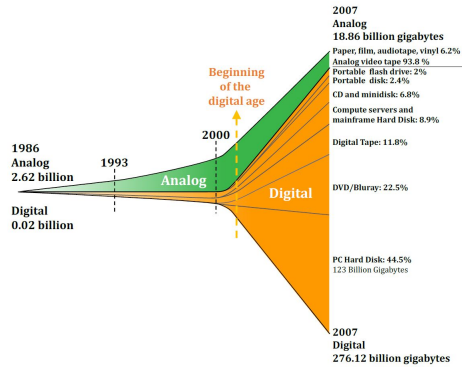
(b) Evolution of digital data created and shared from documents to pictures to tweets [4].
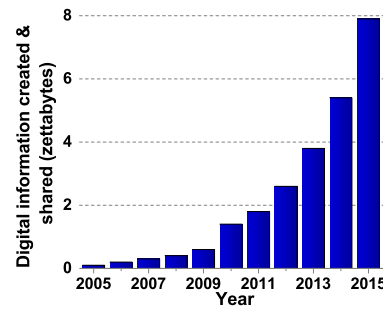
Dealing with the technologies created to answer storage demands, digital storage (including magnetic hard disk drives (HDD) and optical disc such as CD, DVD, Blu-Ray...) is preeminent. The main requirements for this technology is to be non-volatile memories and to allow reliability and safety of the data for more than 10 years even at the expense of degraded speed. In the 2000's, stand-alone memory emerged: non-volatile semiconductor memories called Floating Gate Flash memory. Faster than Hard Drive, it first appeared in USB-keys and then in Solid State Drive (SSD) card because of its high density on a restricted area. Today, complete HDD replacement start to be questioned with SSD introduction in computers, tablet and smartphones. Indeed, with the cost reduction of Flash memory due to its high integration density coupled to similar performances, Flash memory becomes competitive (see Figure 1.2).

However, in order to access market demands, this technology follows the Moore law consisting in the doubling of the number of transistors in a dense integrated circuit every two years thanks to a transistor downscaling. This constant size reduction of Flash memory cells faces key technological and physical issues including high operation voltage, high power consumption, lithography limitations, tunnel oxide thickness reduction, reduction of the space between cells and diminution of the number of stored electrons [6]. All these technological issues having more and more difficulties to be overcome every year [7], a real interest toward alternative

	Hard Disk Drives (today)	flash drives (today)	flash drives (tomorrow)
Raw capacity	1.72x	1x	1x
Access time	~ 1ms	~ 0.3ms	~ 0.1ms
Floor space	1.33x	1x	0.66x
Energy Usage	13.9kW	5.7kW	~ 5.0kW
price	1x	1x	<1x

Figure 1.2: Comparison of Flash memory and hard drive [5].

technologies started to grow. Yet, this Flash technology is cheap and mature. A new device will require aggressive specifications especially in terms of density and cost to integrate stand-alone market.

1.1.2   Embedded memory: single specifications for each application

Embedded memory is used for embedded systems which require high speed, wide bus-width capability and low consumption. In order to access this demand, this technology has a dedicated architecture to support the logic core and accomplish intended functions. Compare to stand-alone memory, inter-chip communication are eliminated and the memory capacity is specific for an application. The main disadvantages of embedded memories are that they are generally larger in size and are more complex to design and manufacture. Additionally, a trade-off must often be found between design and technology since the optimized technology for a memory cell is not the same as that for embedded logic devices. Furthermore, processing becomes even more complex when the designer integrates different types of memory on the same chip. Table 1.1 summarizes the main differences between stand-alone and embedded flash technologies. It can be noted that an embedded memory technoloy requirement is always given for a specific target that could go from automobile to IoT applications. New technologies are welcomed to enlarge possibilities for novel applications.

Table 1.1: Main differences between stand-alone and embedded flash specifications

	Embedded	stand-alone
Main application	Code execution	File Storage
Storage Capacity	Low	High
Cost per bit	High	Low
Active Power	High	Low
Standby Power	Low	High
Write Speed	Low	High
Read Speed	High	Low

1.1.3   Memory hierarchy in computing systems: storage class and working memory

Going back to the technologies used to answer storage demand, magnetic hard disk drives (HDD) are preeminents in terms of storage in computing systems. HDD allows reliability and safety of the data for more than 10 years. However, this kind of storage class memory is quite slow regarding to processor capabilities (CPU). They have an access time between 0.1ms and 1ms depending on the technology while CPU requires data to be accessible in less than 1ns. In order not to be limited by the speed of these kind of memories, volatile semiconductor devices (based on transistor technology) are used as intermediate between processors and hard disk drives. These working memories need to be fast even at the expense of data retention. Only Static Random Access Memory (SRAM) are fast enough to overcome speed issue but is expensive. Therefore, Dynamic Random Access Memory (DRAM) which is cheaper and with intermediate speed has been introduced in computer memory hierarchy. Compared to non-volatile memory, these two technologies are faster but they lose their information when power supply is shut down. One of the challenges today consists in filling the gap between working memories (DRAM) and storage memories (HDD, SSD) with intermediate density. Indeed, Flash memory has an access time of 100µs and Gigabits can be stored while DRAM has an access time of 10ns and Megabits can be stored (see Figure 1.3).
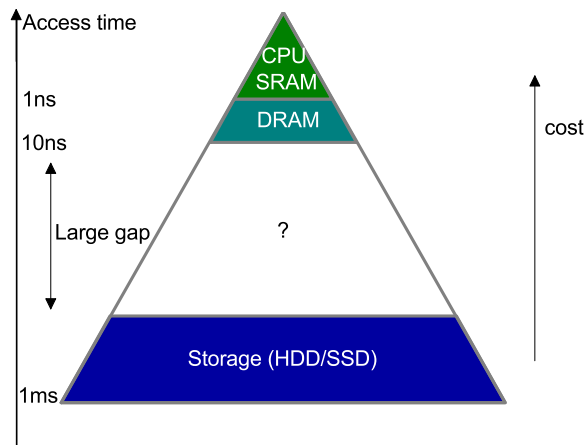
Figure 1.3: Memory hierarchy in computers.

1.2 Resistive emerging memories: Principles and characteristics

Figure 1.4 summarizes the current state of semiconductor memory devices divided between volatile and non-volatile technologies. We will focus on emerging non-volatile resistive memories. Their working principle relies on having two distinguished resistive states electrically measurable and commutable establishing the so called "0 state" and "1 state" of a memory. Memory state is measured by sensing the current flowing through the device leading to two distinguished electrical responses. These two states need to be repeatable, reversible and reading should be non destructive. Resistive emerging memories show different maturity levels. Some products already exist but they are still considered as emerging memories, as their potential to replace Flash or DRAM has not been clearly demonstrated yet.
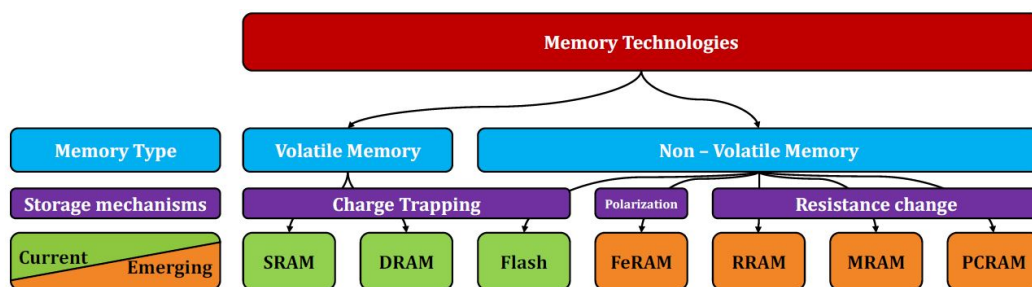
Figure 1.4: Current state of the memory technology [7].

1.2.1 FeRAM

The oldest one is the Ferroelectric RAM (FeRAM), which is produced by Fujitsu [8] and Texas Instrument [9] and already on the market. The

working principle of this technology relies on two stable polarization states proper to ferroelectric material. They have an intrinsic electric dipole able to switch depending on an applied electric field allowing to obtain distinguished resistances [10] (see Figure 1.5). Therefore, they belong to the switching resistance memory family.

Ferroelectric crystal polarisation

Ferroelectric crystal up polarisation

Ferroelectric crystal down polarisation
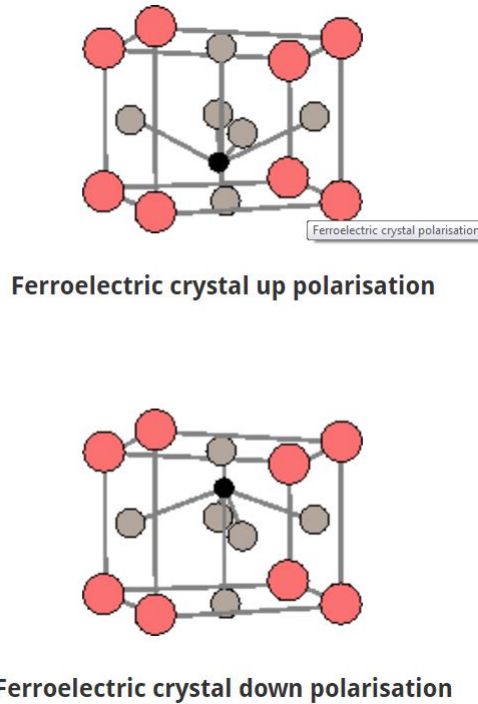
Figure 1.5: Schema of FRAM polarisations [11].

1.2.2 MRAM

Magnetoresistive memory (MRAM) is another emerging technology whose data storage is based this time on the magnetization change of a material layer associated with another layer having a fixed magnetization [12]. If the two layers have the same magnetization, a high current can flow through these two layers. On the contrary if the two layers have an opposite magnetization the resistance of the device is high (see Figure 1.6). The magnetization change is obtained thanks to an applied magnetic field which can be created by a current. Today, this technology is mainly commercialized by Everspin and a product is announced by Samsung for 2018.

1.2.3 PCRAM

The Phase Change memory (PCRAM) relies on a possible phase change by applying a voltage on the cell. Chalcogenides are the material used having two stable state: an amorphous and a crystalline state with different
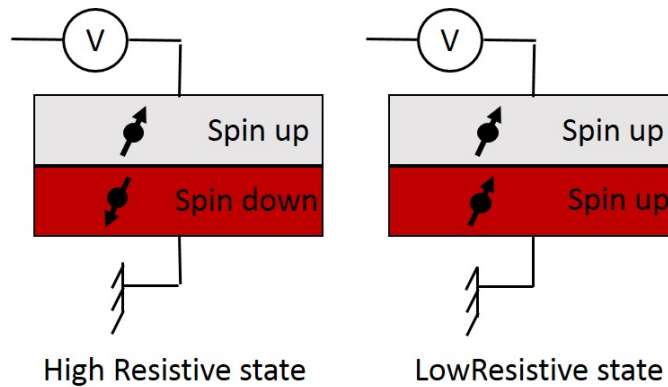
Figure 1.6: Schema of MRAM two resistive states.

resistances [13] (see Figure 1.7). Intel associated with Micron announced a a high density product for 2018 based on this technology [14].
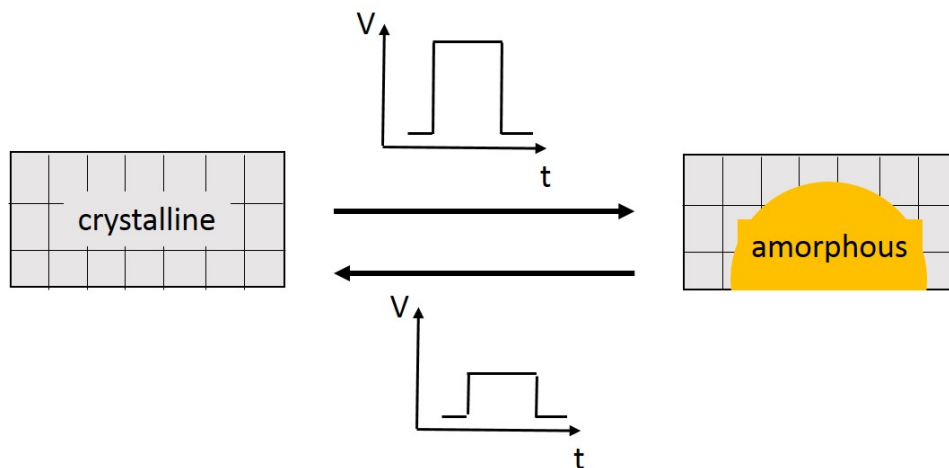
Figure 1.7: Schema of PCRAM working principle.

1.2.4   RRAM

Resitive memories are divided in two kinds of technologies: Oxide RAM (OxRAM) and Conductive Bridge RAM (CBRAM). They rely on the formation and disruption of a conductive path in a resistive layer. As they are the subject of this manuscript, these technologies will be described in the following.

1.2.5   Comparison with actual Flash technologies

All these technologies show promising performances and may be potential candidate for memory market. Figure 1.8 shows the improving maturity of emerging technologies compared to Flash in terms of storage ca-

pacity. Table 1.2 summarizes and compare in more details these emerging technologies with Flash memory [7]. RRAM are good competitors and present a great potential especially in terms of high speed, low consumption and ease of integration in the Back End Of Line [15, 16]. Compare to DRAM technologies they present a higher density of integration at the expense of speed. A more precise state of the art of the current RRAM performances and devices will be given in the following of the chapter.
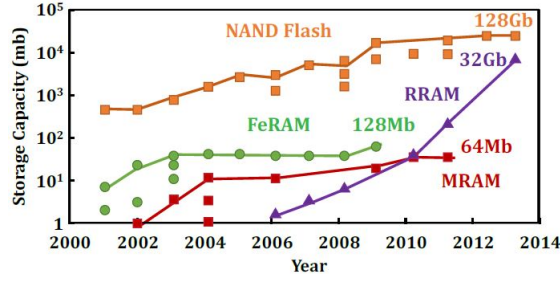
Figure 1.8: Storage capacity evolution for various non–volatile technologies [17].

Table 1.2: Comparison between Flash and emerging memories [7].

		Flash	FeRAM	PCRAM	MRAM	RRAM
Integration F (nm)	2013	16	180	45	65	5
	Projected	< 10	65	8	16	< 5
Cell surface F^2	2013	4	22	4	20	4
	Projected	4	12	4	8	4
Programming Voltages (V)	2013	15-20	1.3-3.3	3	1.8	0.6
	Projected	15	0.7-1.5	< 3	< 1	< 0.5
Programming/Erasing time	2013	1 / 0.1ms	65ns	100ns	35ns	< 1ns
	Projected	1 / 0.1ms	< 10ns	< 50ns	< 1ns	< 1ns
Programming power (J/bit)	2013	$4*10^{-16}$	$3*10^{-14}$	$6*10^{-12}$	$2.5*10^{-12}$	$1*10^{-12}$
	Projected	$1*10^{-16}$	$7*10^{-15}$	$1*10^{-15}$	$1.5*10^{-13}$	$1*10^{-16}$
Read Voltage (V)	2013	4.5	1.3-3.3	1.2	1.8	0.2
	Projected	4.5	0.7-1.5	< 1	< 1	0.1
Read time (ns)	2013	0.1ms	40ns	12ns	35ns	50ns
	Projected	0.1ms	< 20ns	< 10ns	< 20ns	< 10ns
Data retention (year)	2013	10	10	> 10	> 10	< 10
	Projected	10	10	> 10	> 10	> 10
Endurance (Cycle)	2013	10^5	10^{14}	10^9	10^{12}	10^{12}
	Projected	10^5	$> 10^{15}$	10^9	$> 10^{15}$	$> 10^{12}$

1.3 RRAM technologies: how does it work?

1.3.1 Generalities

RRAM technologies are based on a Metal/Insulator/Metal (MIM) structure: a thin resistive layer is sandwiched between two metallic electrodes; the Top electrode (TE) and the Bottom electrode (BE) [18] (see Figure 1.9a). By applying a voltage between TE and BE, a conductive path, called filament, can be formed linking both electrodes, allowing current to flow and leading to a low resistive state. This phenomenon is stable and reversible by applying another voltage drop on the cell coming back to a high resistive state. Depending on TE nature, this filament can be composed of different species. In CBRAM, filament is composed of metal ions coming from the TE; TE is called "active". In OxRRAM technology, filament is composed of oxygen vacancies created in the oxide resistive layer. In this manuscript we will talk as well about Hybrid Resistive RAM (HRRAM) where filament could be composed of oxygen vacancies and TE metal ions [19–22].

Figure 1.9b presents an electrical response of a typical RRAM with a simple description of CBRAM principle Figure 1.9a. First the cell is in a Pristine state; no current has been applied yet. Forming process is the first step the cell sees. Typically, forming voltage is higher than subsequent switching voltage and cell switches from a Pristine state to a Low Resistive State. Then a reverse voltage is applied to the cell which will disrupt the conductive path and lead to a High Resistive State. This step is called RESET. A new voltage drop is applied to create the conductive path again and leads to Low Resistive State. This last step is called SET. Switching between SET and RESET is possible as many time as the technology permits it and is called cycling. It can be noted here that in some technologies it is possible to RESET at the same polarity than SET. This process is then called unipolar instead of bipolar in the other case. Switching voltage and time depend on technology (typically ~2V). The current during SET is limited by an exterior device (transistor or diode) to avoid a weariness of the resistive layer which would lead to an early breakdown.

1.3.2 Advanced understanding on filament formation and composition

Conductive path formation is actually more complex than the previous simple description. To describe in more details a conductive path formation, several physical phenomena need to be taken into account. The fol-

(a) CBRAM working principle with fil-
ament creation and disruption in or-
ange.
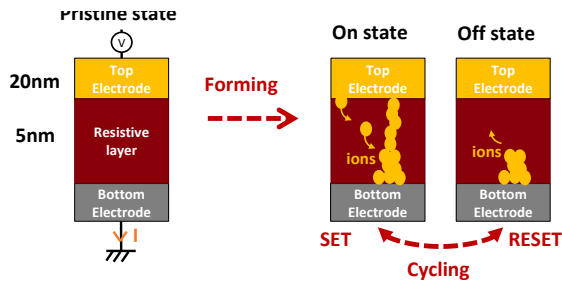
(b) Typical IV curve of a bipolar behav-
ior for Al_2O_3(5nm)/Cu CBRAM.
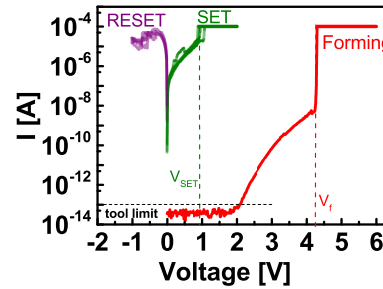
Figure 1.9: schema of CBRAM working principle associated with its electrical response.

lowing descriptions are theoretical and subject to modification as a com-
plete physical understanding is still missing.

Metal ion filament

For CBRAM, the switching mechanism is based on the formation and
disruption of a metallic filament. This section is deduced to the two main
approaches which are currently considered to describe its working princi-
ple.

The first approach is the electrochemical metallization (ECM) which is
composed of three steps: Oxidation, Migration and Reduction [19, 23].

Oxidation consists in ion creation at one of the electrode/resistive layer
interface. This electrode has to be electrochemically active and is usually
placed as a TE (Silver [24], Copper [25]). Some theory has been supporting
this idea based on [23, 26].

The second step is an ion migration driven by electric field (created by
the voltage drop applied on the cell) towards the second electrode (usually
BE). The resistive layer has to be well chosen to allow this migration (for
example: GeS2 for Ag [27] or Al2O3 for Cu [28]).

Finally, the ions are reduced and accumulate at the second electrode
starting a filament. When enough ions are reduced, the conductive path is
created linking top and bottom electrodes. This phenomenon is reversible,
with this time, ion creation at the second electrode interface and reduction
at the first one. It is essential here that the second electrode is composed
of electrochemically inert material to avoid its dissolution during reverse

10

operation what would lead to a non-proper filament erasing. This operation is enhanced by heating due to high current density flowing before the destruction of the conductive path.
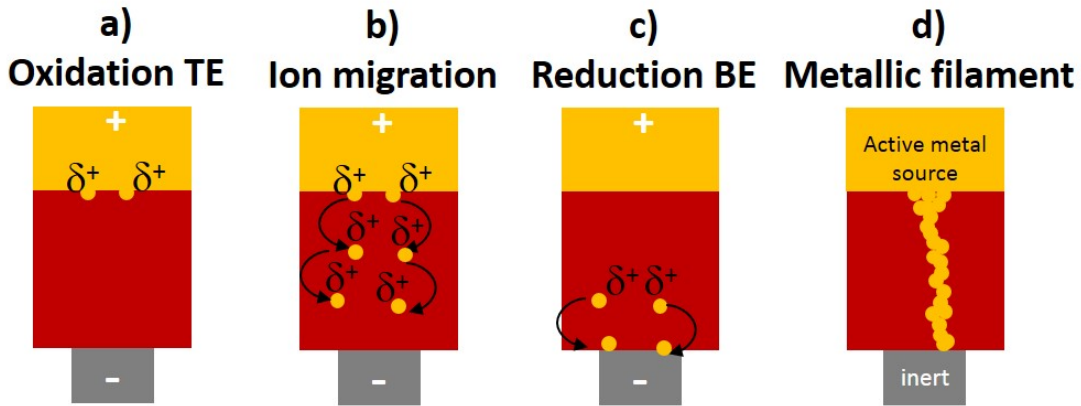
Figure 1.10: Schemas of electrochemical metallization steps for CBRAM working principle theory.

In a second approach, atoms are not ionized at electrode/resistive layer interface but there is an electromigration event. The commutation process is based on a momentum transfer between the electrons and the diffusing metal atoms [29, 30]. This phenomenon needs a sufficient amount of current and the feasibility of a non-volatile memory relying on such switching mechanism has been proved [31]. This theory is not accepted as much as the previous one.

Oxygen vacancies filament

For OxRAM, filament creation and disruption are due to oxygen vacancies movement. This section is deduced to the two main approaches which are currently considered to describe its working principle.

Oxygen vacancies displacement takes place in transition metal oxide (HfO_2, Ta_2O_5, NiO [32–34]) surrounded by two electrodes. The cells require an oxygen vacancies supplier which can be a particular oxidizable electrode (transition metal such as Hf, Ta, Ti) or a particular resistive layer depleted in oxygen [33, 35, 36]. Today there are two main approaches to explain a switching mechanism based on oxygen vacancies displacements.

A first approach consists in the redistribution of oxygen vacancies already existing in the resistive layer. Enough oxygen vacancies to create

a conductive path are considered already present in the oxide or created during the first writing operation: Forming. These vacancies are charged and migrate under the electric field induced by the applied voltage, creating a filament. The current flowing through this path also generates heat enhancing the vacancies migration and filament destruction. In this approach, oxygen vacancies are responsible for the electrical conduction and their migration induced by the electric field explains the bipolar switching.
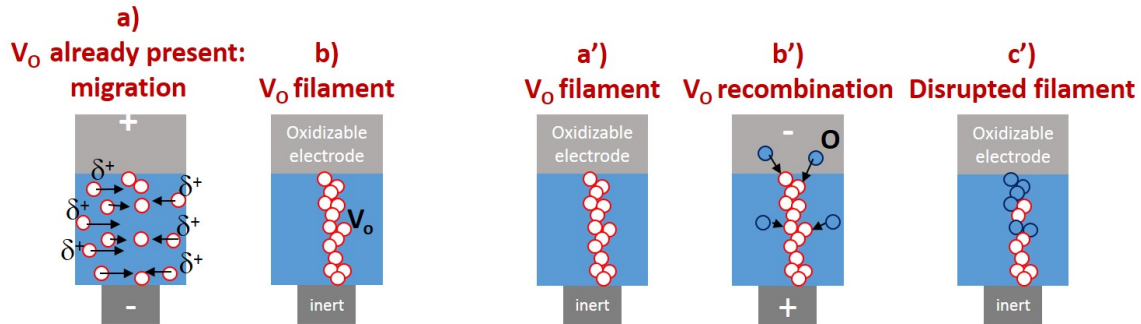
Figure 1.11: Schemas of oxygen vacancies (V_O) displacement at the heart of OxRAM technologies: a) and b) oxygen vacancies redistribution in the resistive layer. a'), b') and c') oxygen vacancies recombination.

Another approach is based on the creation and destruction of oxygen vacancies [37] at each cycle and not only during Forming. Local redox reactions of the resistive layer can modify the vacancies concentration during SET or RESET. Thus, this metal oxide is reduced at its metal state during SET creating a conductive path rich in metal. During RESET, the same atoms are oxidized decreasing the metal concentration. Both processes are accelerated by the thermal heating induced by the high current density. In this approach, the conductive path is formed by a decrease of oxygen concentration and increase of metal content. The bipolarity of the switching mechanism is explained by the difference of voltage favoring either the oxide reduction or metal oxidation. A unipolar switching is also possible if the RESET operation is only thermally driven.

Oxygen vacancies displacement is at the heart of OxRAM technologies also called as valence change memory (VCM). Figure 11 shows a schematic representation of these two theories.

Resistance change

RRAM working principle is based on cell resistance change depending on the amount of current flowing. There are several hypotheses to explain oxygen vacancies and metal ions electrical conduction. Depending on resistive state (high or low) different mechanism are invoked.

In the case of metal ion conductive path, standard Ohm conduction is generally employed [37, 38]. This conduction form is also used to simplify the HRS electrical conduction but with a strongly reduced conductivity. It is important to note that it exists a continuum [39] of states between a fully formed filament in LRS and a fully dissolved in HRS. During the early stages of RESET, the filament thickness is greatly reduced at a constriction point. Once the constriction is small enough (few atoms), the electrical conduction can be tied to a Quantum Point Contact conduction [40–42]. This conduction is attributed to the very low amount of atoms allowing the current to flow, resulting in a quantum conduction in one dimension. Following the filament dissolution, shortly after it breaks and a gap appears between both top and bottom side of the filament, in this case the conduction can be explained by Fowler–Nordheim tunneling [43, 44]. With the RESET progression, the gap increases and charge trap might appear in the gap during the process. The last conduction model, bonded to theses traps relies on Trap Assisted Tunneling (TAT) [45–47]. It can be noted as well that some study has been performed on oxide dealing with filament formation due to sub-oxides [48].

Dielectric breakdown

OxRAM technology is based on the reversible creation of oxygen vacancies in a dielectric such as HfO_2, Al_2O_3... A parallel can be made with oxide breakdown. For a dielectric, one of its main property is to not conduct the current. When a potential difference is applied to a dielectric, a leakage current is observed. This is due do charge traps already present post process and allow a small current path. For a good insulator, this current is of the order of 10^{-12}A. Figure 1.12 presents a dielectric current evolution over time when this one is under a constant bias. This curve can be cut in 3 different zones.

In zone 1, the current is decreasing over time representing the absorption of charges that the dielectric can sustain due to its own charge traps.

In zone 2, current is increasing demonstrating a creation of new traps, defects, to allow current flow.

This phenomenon gets out of control zone 3, where an avalanche of defect creation happens and leads to breakdown meaning the dielectric becomes conductor [20]. This breakdown can be controlled if a limited amount of current is permitted by an exterior device. In this case, some of the traps can be annihilated. RRAM forming step can be correlated to this description (see Figure 1.9b). Some device models use this knowledge to put in equation RRAM behavior especially using a percolation model [49].
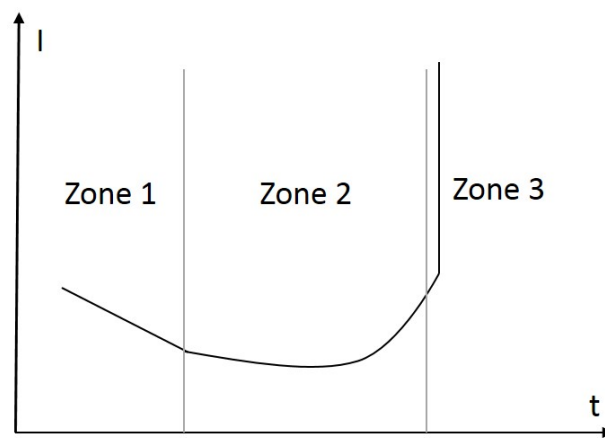
Figure 1.12: Schema of a dielectric current vs time response under constant bias. Zone 1: charge absorption, Zone 2: new traps creation, Zone 3: breakdown.

1.4 Towards RRAM Industrialization: RRAM potential in memory market

1.4.1 History

The first migration of silver ion in a porous material has been published in 1954 [50]. Putting a potential difference on a material sandwiched by two Ag electrodes, Ag migration is observed. But a memory device is not yet in the idea. In 1964, memory effect is demonstrated in a metal/insulator/metal (MIM) structure, namely Au/SiO/Au [51]. At the time it was hypothesized that such a structure could have been used as a memory device which could be accessed non-destructively. In the ensuing years similar phenomena were found in an Al/SiOx/Au system [52, 53]. Due to stability issues and the successful development of Si based memories [54], resistive switching memories were put aside until quite recently.

In 2002, W.W. Zhuang *et al.* demonstrated an RRAM device based on PCMO which could have greater performances than Flash devices [55]. In 2004, Samsung Electronics demonstrated resistive switching behavior in various transition metal oxides (TMO) such as NiO, TiO$_2$, HfO$_2$ and ZrO$_2$ with promising characteristics such as an operating voltage below 3V, a programming current around 2mA and an endurance of 10^6 cycles [56]. In parallel, memory effect are published using metal ion migration.

For CBRAM, the first researches were mostly devoted to a large screening of the material combinations offering the switching mechanisms by metal migration in a resistive layer. For this matter, a great interest on the use of chalcogenide has grown and a lot of researches were presented on various resistive layers and electrodes combinations. For example GeTe [57], GST [58], Zn$_x$Cd$_{1-x}$S [59, 60] or Cu$_2$S [61, 62]. Ge$_x$S$_y$ and Ge$_x$Se$_y$ were the two most studied components mainly coupled with silver top electrode but various bottom electrodes such as Tungsten, Platinium or Nickel [63]. This technology was growing in interest but limitations appeared. Temperature stability was one of the most important as it can limit CBRAM integration in CMOS integrated circuits due to the high temperatures used in standard back-end-of-line processing. More research intend to improve its stability using different chalcogenide stoichiometry or doping [64] but a big change appeared when the resistive layer was replaced by an oxide.

Oxide offers a higher thermal stability and is a well-known material in microelectronic which will help process integration. The materials screening researches has thus been conducted on oxides such as Al$_2$O$_3$, Ta$_2$O$_5$, HfO$_2$, mainly coupled with copper top electrode.

1.4.2   RRAM for the actual memory market

To emerge in memory market, one need to think about the place of RRAM and its specifications depending on the target. Several memory architectures could be considered depending on technology performances and cost.

RRAM for Stand-alone application

As flash devices start to face key technological issues, alternative memory is envisaged. However, as this technology is cheap and mature, aggressive specifications in terms of cost and density are required. RRAM advancement for stand-alone applications were presented in [16, 65] but

RRAM technologies face difficulties to reach flash maturity. Moreover, although 2D flash topological method is expected to reach its practical limit by 2020, 3D flash technology starts to emerged and will lead the semiconductor industry towards the next revolution in transistor density [14]. RRAM technology is not expected anymore for stand-alone application unless a major breakthrough occurs.

RRAM for Embedded application

Another idea is to target embedded market. As presented in the beginning of the chapter, each application will need specific criteria. RRAM technology already prove its potential for this market. For automotive application, high temperature stability is required and is demonstrated in [15, 66, 67]. For low power application, [28, 68] can be cited.

RRAM for computing systems hierarchy

The last market RRAM could integrate would be in computing systems hierarchy as a storage class memory (like HDD) or as a working memory (like DRAM). In terms of storage, there are two possibilities: placing RRAM between hard disk and DRAM or replacing hard disk (see Table 1.3). To access this market, RRAM would need to reach a retention stability over 10 years at 85°C, a latency below 5µs and an endurance superior to 10^6 with high density product. RRAM advancement for storage class applications were presented in [16, 65].

Table 1.3: RRAM specifications for Storage class applications

class	memory type	latency	Endurance	Retention	Cost	Power consumption
storage	replacing hard disk	< 5µs	> 10^6	10years 85°C	< 2 * flash	< flash
storage	between hard disk and DRAM	< 5µs	> 10^6	10years 85°C	~ flash	< flash

In a second case, RRAM could replace or support DRAM. It would then need a latency lower than 50ns as demonstrated in [28, 69], retention around few days is enough and a great endurance as demonstrated in [33, 70] (see Table 1.4).

Table 1.4: RRAM specifications for working memory

class	memory type	latency	Endurance	Retention	Cost	Power consumption
working memory	replacing DRAM	< 50ns	> 10^9	> 5days 85°C	< $\frac{1}{2}$DRAM	< DRAM
working memory	between hard disk and DRAM	< 200ns	> 10^9	> 5days 85°C	< $\frac{1}{2}$DRAM	< DRAM

Nowadays, RRAM show some limitations before being able to integrate this market. Four issues remain challenging: window margin variability, forming operation, programming current and trade-off between endurance and retention. Today, the main research efforts have been focused on improving device performances, dimensions and physical understanding, placing RRAM technology after the peak of its interest (see Figure 1.13). Research is now waiting for an industrial to challenge the technology.
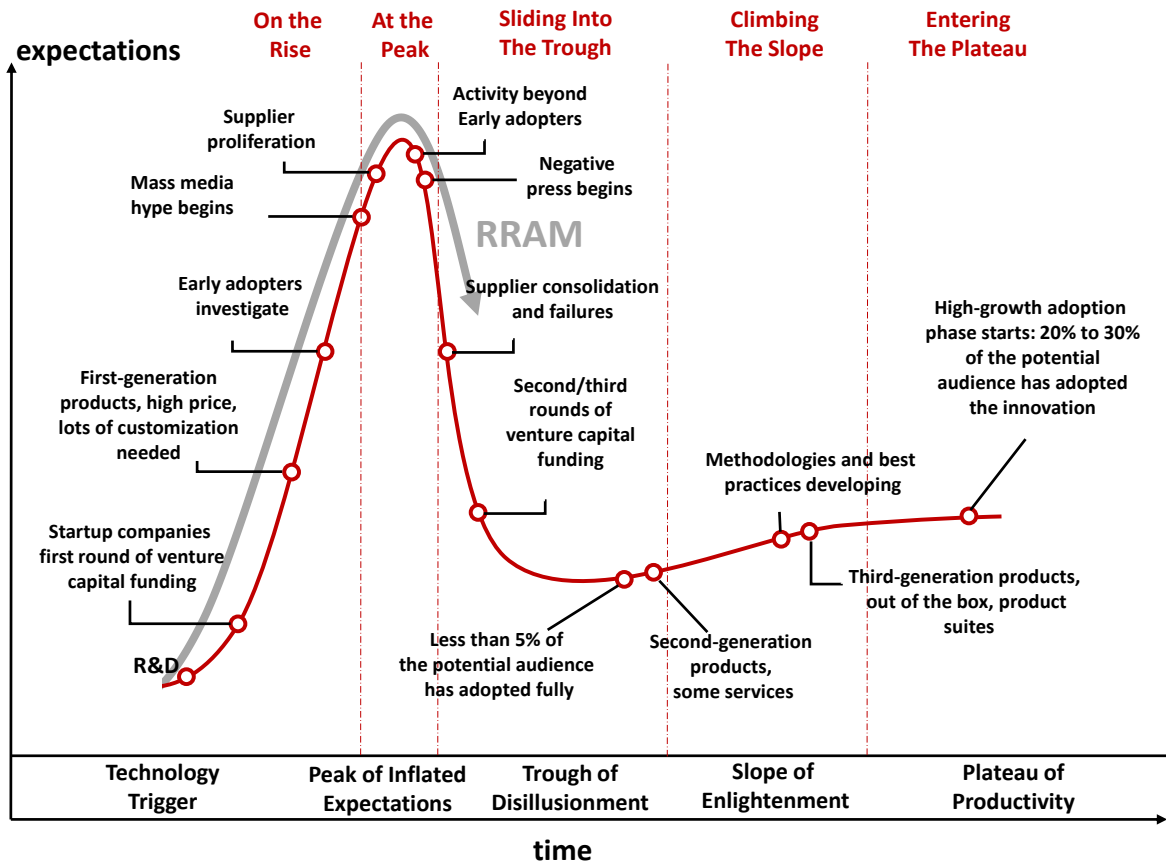
Figure 1.13: RRAM maturity level [71]

1.4.3 RRAM improvement: work in research for theoretical understanding

Microscopic observation

Following CMOS development tracks, RRAM presents a lack of theoretical bases. The working principle is not yet fully understood and some researches are devoted to physically observe RRAM switching mechanism. However, as conductive paths width is supposed to be in nanometer range, literature does not give entire satisfaction. Research is still devoted to RRAM observation, dreaming of a device real-time switch movie with in-situ transmission electron microscopy (TEM).

For example in 2011, B. Cho showed a bistable switching mechanism behavior related to the formation and rupture of highly conductive paths in a Ag/polymerstructure using TEM and energy-dispersive X-ray spectroscopy [72] following in 2012 by Y. Yang et al who published a direct TEM imaging of metal ion/oxide structures showing a metallic conductive path [73]. These results comforted CBRAM principle with a filament composed of metal ions coming from an active electrode which can be formed and disrupted with a bipolar behavior.

In parallel, Q.Liu et al observed in real time a growth and dissolution of conductive filaments in Oxide-Electrolyte-Based RRAM supporting its working principle description: there was no silver in the Pristine state while after forming, Ag is highly detected. After Reset, there is still some Ag detected but in lower concentration showing that the initial state is not recovered. There is a multifilamentary observation. Conductive filaments are found to start growing from the TE rather than having to reach the BE and grow backwards and have a conical base at the TE interface [74]. This result allows to give a filament shape closer to reality for simulation although it is still in debate.

More recently, in 2014, U. Celano et al used conductive atomic force microscopy to observe the conductive zones in a switched device. They extrapolated the results in a 3D image showing a conical filament with its base at the TE. They showed as well, using scanning probe microscopy (SPM), that the constriction of the CFs is below 10 x 10 nm2 indicating a strong scalability potential for OxRAM devices [75, 76].
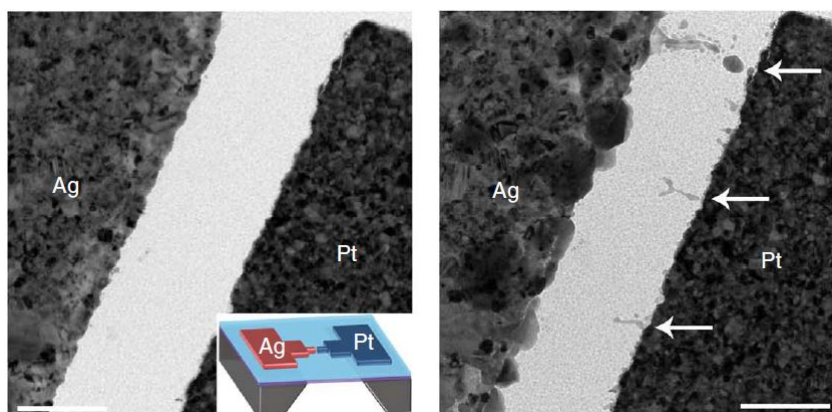
Figure 1.14: Observation of conducting filament dynamics in SiO_2-based resistive memories [73].

Simulation and Modelling

To support microscopic observation, simulation works are carried out. Among these researches, a lot of effort are put into first principles calculations which allow the computation of various properties (electronic, mechanical, energetic...) of a material. However, these calculations are strongly limited by the number of atoms it can simulate. Only few atoms can be simulated in a relative short time duration (few days to weeks), which makes it impossible to simulate a whole RRAM cell. However, it can give insights on defects creation and behavior in one of the layer. For example, defect energy levels and defect energy migration barriers can be extracted. To give an example of the impact of these works, we can focus on Al_2O_3 as a resistive layer.

To study a possible filament composed of oxygen vacancies, V_O diffusion has been studied for different charge state [77] with a description of defect levels [78, 79] giving an idea on the energy cost of creating this filament.

On the other hand, K. Sankaran et al studied in an amorphous Al_2O_3 the diffusion barrier of different defects such as Cu and Te showing a very low Cu diffusion barrier in the case of porous Al_2O_3 [80] accentuating on a CBRAM behavior study and support a Cu filament.

To go further, J. A. Dawson and J.Robertson use three different filament models in Al_2O_3, showing that the strong binding between Cu interstitials drives filament formation, resulting in Al ions being driven out of the Cu-rich environment [81]. This result gives insight on a copper based filament formation.

In the same idea, X. Xu et al compared different Cu filament density (3 to 7 atoms of Cu) and show that small changes in the filament structure can lead to large changes in the current-voltage characteristic in atomic scale filaments which can explain a multi-level resistances in RRAM [82].

Staying in electrical characteristics, T.V. Perevalov et al show that electron and hole capture on oxygen vacancy in $\gamma - Al_2O_3$ is an energetically favorable process [83].

	Path 1	Path 2	Path 3	Path 4
$q=0$	3.90	4.70	4.33	6.01
$q=1+$	2.47	3.25	3.43	4.80
$q=2+$	1.26	1.72	2.25	3.23
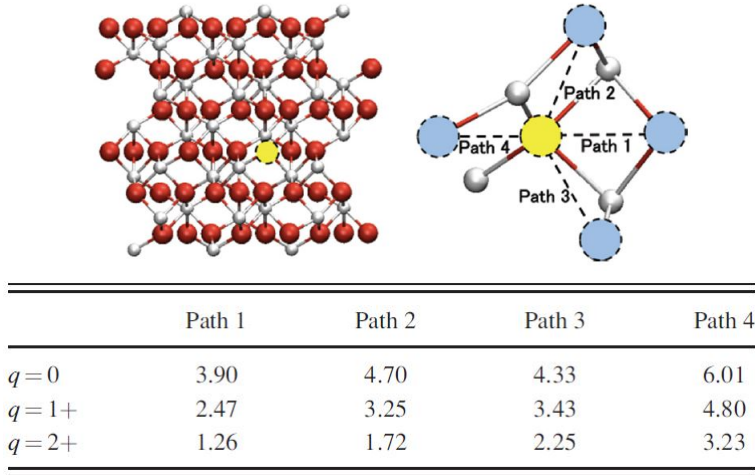
Figure 1.15: Activation energies (eV) of V_O diffusion on four pathways at different charge states in Al_2O_3. Al in red, O in white and V_O in yellow [77].

These studies can be done on other material such as HfO_2 [84–87], Ta_2O_5 [88–90]... to comfort or refute some hypothesis following a microscopic observation or an electrical behavior. Moreover, using these calculation results and experimental inputs, device models have been developed following various electrical conduction hypothesis such as Ohmic current through highly resistive layer [37, 38, 91], Fowler-Nordheim tunneling [43, 44], Trap Assisted Tunneling [45–47] or Quantum-Point-Contact [40–42].

From CBRAM/OxRRAM to Hybrid RAM

Most of the results presented in this manuscript were obtained on oxide-based CBRAM. This technology has been motivated by the complementary advantages of chalcogenide CBRAM and OxRRAM. Chalcogenide CBRAM technology is well known for having a high R_{OFF}/R_{ON} ratio and a low power consumption while OxRRAM has a high temperature stability and high cycling. By combining both technologies, having an oxide as resistive layer and an active Top Electrode, this new device may allow to obtain all advantages in one technology. However, understanding the working principle of this oxide-based CBRAM is even more challenging. They may combine oxygen vacancy and metal ion movements if TE/oxide are well chosen. In this case, we will talk about Hybrid RRAM (HRRAM) in this manuscript.
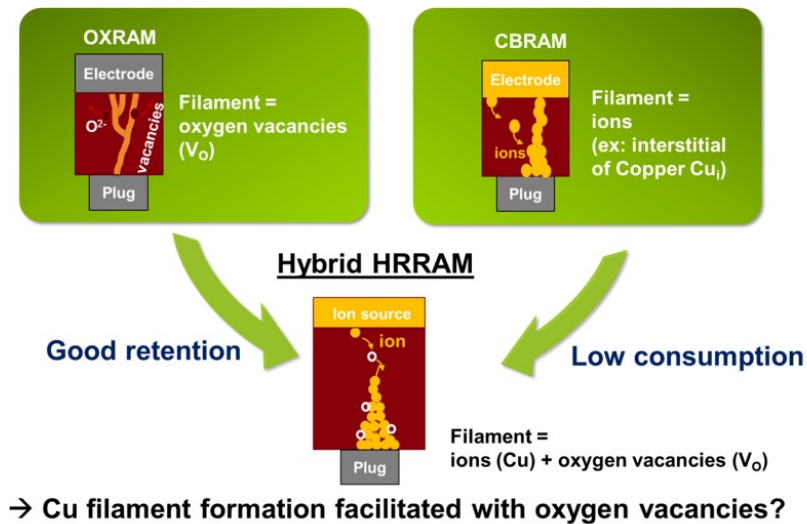
Figure 1.16: Motivation to go from CBRAM/OxRRAM to HRRAM.

1.5 Chapter I synthesis

RRAM technologies present great advantages to enter the memory market thanks to ease of integration in the Back end of Line and high density. They could integrate three different kinds of market: storage class, stand-alone applications and embedded systems. For each target, different specifications are needed. Some of them were demonstrated in literature but RRAM still present some technological issues which place RRAM after its peak of interest, waiting for an industrial to challenge the technology.

Today, various physical mechanisms can explain CBRAM and OxRRAM switching behavior. They rely on a conductive path formation and disruption, called filament, in a resistive layer. In the case of CBRAM, filament is composed of metallic elements coming from the active top electrode while in OxRRAM, it is composed of oxygen vacancies created in the oxide resistive layer. At the beginning of CBRAM technology, chalcogenides such as GeS_2 was chosen with mainly Ag as active top electrode. However, due to high temperature stability issues and hoping to improve window margin and power consumption compare to OxRRAM technology, oxide-based CBRAM were tested. In this case, filament can be composed of oxygen vacancies and top electrode metallic element. Our laboratory baptized this technology, combining both type of filament, Hybrid RRAM (HRRAM). This transition to HRRAM brought new challenges to overcome such as higher voltages and higher forming step than CBRAM and endurance can be degraded compare to OxRRAM. Optimization of this technology is still on going and in the same time, as physical understanding is lacking, mi-

croscopic observation and simulations bring more and more knowledge concerning switching mechanism and material properties impact for each stack layer.

In order to optimize HRRAM materials, simulation and electrical characterization are carried out in parallel in CEA-Leti. Simulations support or refute hypothesis brought by experimental results to clarify RRAM working principle and evaluate material properties impact on the stacks. In this manuscript, both skills has been developed to combine atomistic simulation and electrical characterization. Various RRAM performances are evaluated to target different types of market from storage to embedded. OxRRAM and HRRAM are characterized considering several oxygen density. Then, material properties are investigated by atomistic simulation giving microscopic parameters to link RRAM performances and chosen materials.

To introduce this work, next chapter will describe the studied samples and the characterization methods that has been used to evaluate RRAM performances. Then, third chapter will explain atomistic simulation theory basis and used methods to extract RRAM microscopic properties. These two chapters will serve as basis to the results presented in the following of the manuscript. Then, in the fourth chapter we will present the result on filament microscopic understanding combining experimental and simulation results. Chaper five will fully developed microscopic properties effect on HRRAM performances and present some technological key to choose materials for a given application. Finally, chapter six will synthesis and give the perspectives of this work.

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Chapter 2

Studied devices and electrical characterization set up

2.1 Introduction/Objectives

During this PhD, several types of devices were studied changing material stacks and integration for different maturity level. This chapter focuses on explaining all these differences and describes the electrical set up used to characterize all these devices. Going from a material study, integrating RRAM with a single Resistor (1R device), through a Transistor-Selector integration (1T1R device) evaluating performances of one device, to 1Mb array integration allowing a statistical study significant due to high device variability [1–3], this work highlights a need of physical study as well as a need of industrial bench mark.

2.2 Studied Devices

2.2.1 Material stacks

In order to compare different material performances, variation of stacks, thickness and material deposition methods were used. In a first step, we perform a material research with a simple 1R integration to evaluate if a structure presents promising memory characteristics. The one showing good performances are then integrated in a 1T1R structure to evaluate performances with a better current control avoiding an early device weariness. Finally, the most promising technologies are then integrated in arrays to evaluate devices in industrial environment. This work is based on previous results leading actual effort to study Oxide-based CBRAM. The basic structure is made of an oxide as a resistive layer such as Al_2O_3, HfO_2, Ta_2O_5, an active Cu-based Top Electrode (TE) and different inert Bottom

Electrode (BE) such as W, TiN, TaN. Figure 2.1 shows an example a set of various technologies studied in this work.

Figure 2.1: Stacks variation example studied in this work

2.2.2 Integration

Depending on RRAM maturity, various integration processes were used in this work depending on mask set leading to various memory device structures. Depending on base wafer circuits a single device (1R), a transistor plus a device (1T1R) or an array integration can be obtained.

VIA structure

VIA structure is used to verify first process feasibility of a stack, and then RRAM operation and compare material response. Due to its minimal number of etching/complex pattern, this integration process is fast. However, it does not target industrial architecture requirement. Figure 2.2 represents a VIA structure. Bottom Electrode is deposited in a scaled hole motif which typically measures between 300nm and 2µm and is called VIA. This layer is covered with resistive layer and Top Electrode which are not patterned. These characteristics imply a common active layer for all devices and avoid impact of confinement, etching... on material behavior.
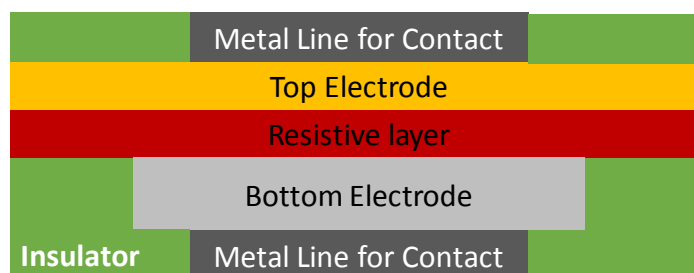
Figure 2.2: Schema of a VIA structure

Mesa structure

In this case, resistive layer and Top Electrode are patterned following Bottom Electrode scale implying that each device has its own switching layer separated from the adjacent ones (see Figure 2.3). Confinement of the memory is then limited by etching which can be as low as the lithography technology allows it to be [4].
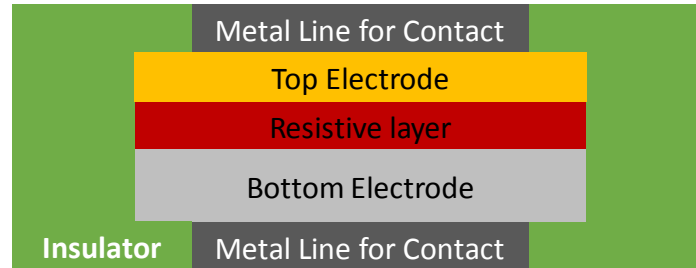
Figure 2.3: Schema of a MESA structure

1R integration

In order to first check RRAM operation, it is integrated in 1 Resistor integration (1R): only RRAM device. This integration is faster than the next one and allows RRAM investigation at the material level. However, this integration presents limitation from a performance point of view and have a lower maximum write and erase operations before device destruction than a 1T1R integration (see description below). This is caused by a lack of current control which implies an early device degradation. Figure 2.4 compares 1R and 1T1R I(V) curves for SET and RESET operations. Even if an exterior generator should limit SET current (100μA here), it is visible that the maximum of current flowing during RESET is around 1mA in 1R whereas it should be equal to the maximum SET current (see 1T1R curves); meaning the exterior generator was not able to limit enough the real current flowing through the memory during Forming and SET. This phenomenon is still being studied [5] and is called overshoot. It is considered to be caused by an uncontrolled electrical capacitance discharge of the bench test cables in the RRAM, during a brief period of time.

1T1R integration

In order to compensate this current overshoot and improve RRAM performances, a current selector is added. In our work, a transistor is playing

(a) 1R
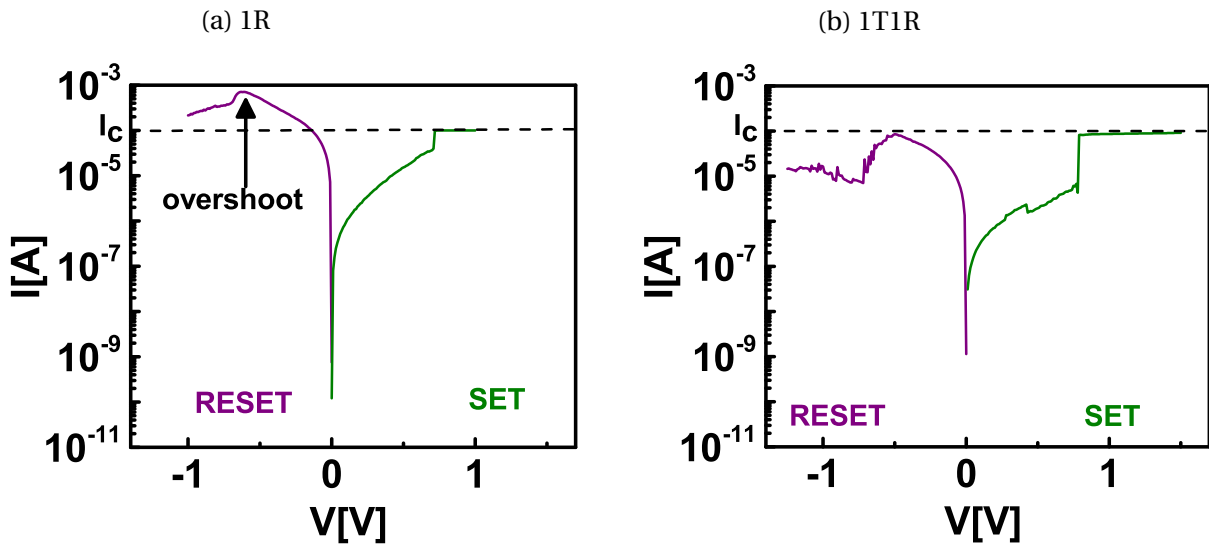
(b) 1T1R

Figure 2.4: Typical SET and RESET I(V) curve of a) 1R and b) 1T1R W/Al_2O_3/$CuTe_x$ device

the current control role. This integration is called 1 Transistor - 1 Resistor (1T1R) (see Figure 2.5) and is essential to improve RRAM performances by decreasing overshoot current described above and also enables large matrix integration (see below). Today, other kind of selectors are subject of research to simplify integration process and increase memory density [6, 7].
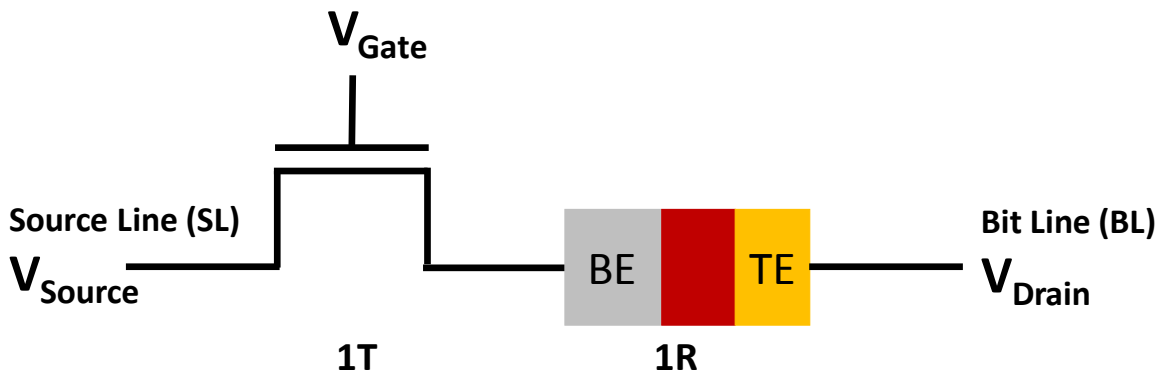
Figure 2.5: Schema of 1 Transistor - 1 Resistor (1T1R) configuration

Arrays integration

Next step in RRAM integration to go towards industrial market is array/matrix integration. In our work, matrices of 4kb to 1Mb are realized. Each single device is a 1T1R cell where transistor is essential to cancel the leakage current ($I_{Leakage}$) between the cells that would exist in 1R matrix (see Figure 2.6). Removing this leakage current allows to realize high density matrices where in the other case $I_{Leakage}$ would become too important

to correctly read or program the cells. Schema of a 4kb matrix tested is
shown in Figure 2.7.
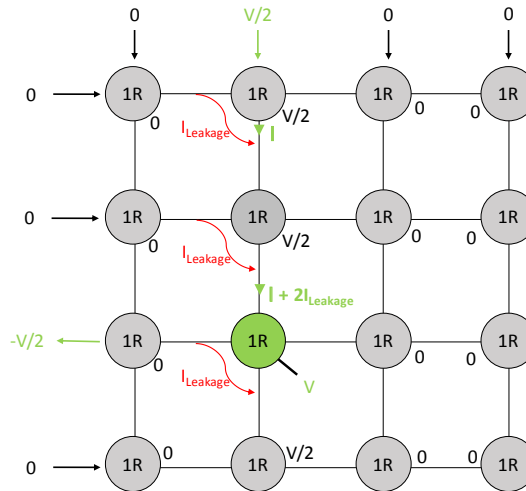
Figure 2.6: Schema of 1R matrix showing leakage current issue. Cell to program at V in green. Note:
V/2 should not affect the cells.
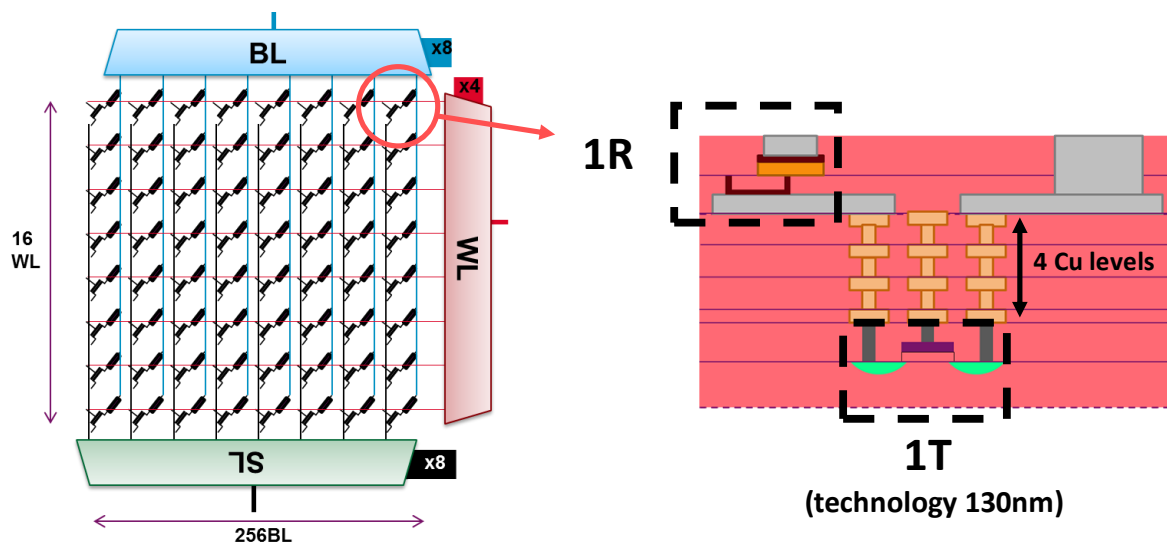
Figure 2.7: Schema of 4kb matrix tested in this work

2.3 Electrical characterization

Depending on electrical characterization tests, it is possible to extract
various memory characteristics. The goal is first to control the viability of
the stacks and show how it would be behaving in a real RRAM life to fi-
nally compare different material responses and correlate it to particular
material properties. Applying a slow voltage ramp on a device will allow a

complete description of a current vs voltage behavior. It is called Quasi-static programming. Switching is then directly visible and voltage switch for forming, SET and RESET can be extracted. This slow ramp method is not industrially viable and highly power consuming. Another study, industrially real is then necessary to evaluate performances of devices such as number of write and erase possible for a given technology, its temperature stability... It is called pulsed programming.

2.3.1 Quasi-static programming

Quasi-static programming consists in applying a voltage ramp between device Top and Bottom Electrodes and in measuring its current response. During the ramp, the current flowing through the cell is measured with a Parameter Analyzer (Agilent 4156 or B1500) and can be internally limited by a maximum current called compliance current I_c. This compliance is used during forming and SET to avoid a complete degradation of the resistive layer which would lead to an irreversible conductive path, destroying the device. A typical I(V) curve is shown in Figure 2.8. From these results, characteristic voltages can be extracted such as the voltages where RRAM switches: they are called $V_{Forming}$, V_{SET} and V_{RESET} for each RRAM event: Forming, SET and RESET respectively. Actual device resistance is accessible as well by a READ measurement consisting in a ramp at low voltage (typically from 0 to 0.1V) to keep the actual RRAM state and avoid Read disturb [8]. Resistance is extracted by a linear regression of this I(V) curve using Ohm's law. Quasi-static method is essential to check RRAM functionalities and extract the first features but it is time consuming and far from industrial reality. So, another programming test is used to extract short time characteristics and industrial like behavior.

2.3.2 pulsed programming

Pulsed programming consists in applying a voltage pulse between TE and BE during a given amount of time. The voltage pulse can be controlled in terms of shape, height, ascending/descending slope and duration. Read operation can be done as well with a pulse at low voltage (few 100mV), measuring current and doing an Ohm law extrapolation. Read operation is done several times and averaged to have a good accuracy. A compliance current can be applied as well. To accelerate a total time measurement, current calibration is possible. By fixing the range where the expected current should be, reading operation is faster. This calibration should be well
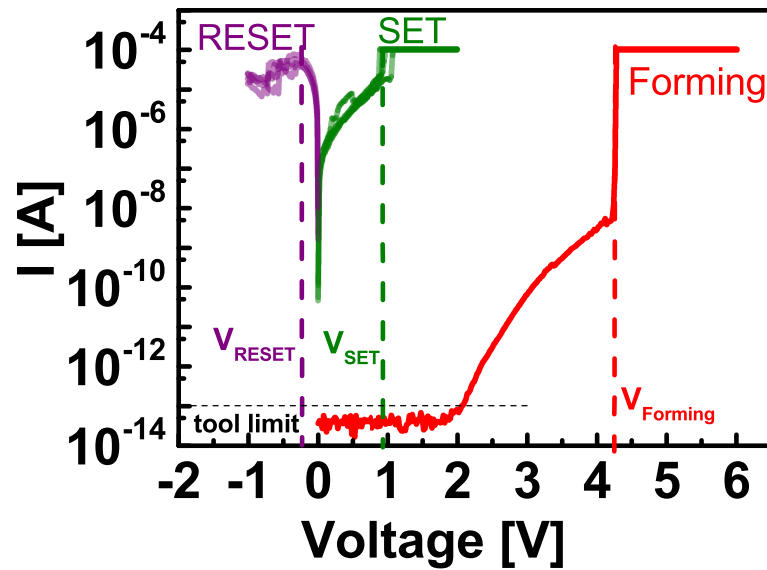
Figure 2.8: Typical Quasi-static I(V) curves with $V_{Forming}$, V_{SET} and V_{RESET} extraction ($W/Al_2O_3(5nm)/CuTe_x$) [9]

chosen depending on compliance current. If the highest current expected is around 10^{-4}A, a calibration around 10^{-6}A (which is the maximum current tolerated) will not read the exact current. The Parameter Analyzer (Agilent 4156 or B1500) has a 3 decades detection amplitude. Therefore, if ON over OFF current ratio is superior to 1000, two different calibrations are necessary to detect the exact resistances in the two states. For example one at 10^{-4}A to detect correctly R_{ON} if compliance is around 100µA and one at 10^{-5}A to reach below 10^{-7}A and read R_{OFF} without any error. One of the big advantage of pulsing programming is the limited stress seen by a cell playing on pulse time duration. This allows to extract the best performances of a device and is similar to industrial programming.

2.3.3 RRAM characteristics extraction: endurance, retention and window margin

To characterize RRAM, three main performances are extracted: endurance, retention and window margin. Each of this feature can be measured by an electrical test.

Endurance

Endurance (also called cycling) corresponds to a succession of SET and RESET operations on a single device meaning the cell is written and then erase as much time as user defines it. After each operation resistance can be measured to control the efficiency of each operation. From this measurement the maximum number of cycles of a technology can be extracted

($N_{cycle\ max}$). It corresponds to the maximum number of Write and Erase actions possible on a technology before one of the operation fails meaning the device can not be written or erased anymore with the chosen condition. To perform a high number of cycles (>1000) read operations can be done punctually on log scale to control if the cell is still working. This kind of programming allows to program 10^7 cycles in one cell in less than 2min. However to control the voltage switch variability depending on cycling, Quasi-static programming is still required. Figure 2.9 shows a typical endurance curve up to 10^8 cycles with 100 successive switching cycles every decades only (Figure 2.9a with all reading points, Figure 2.9b with a standard deviation on the 100 reads per decade).
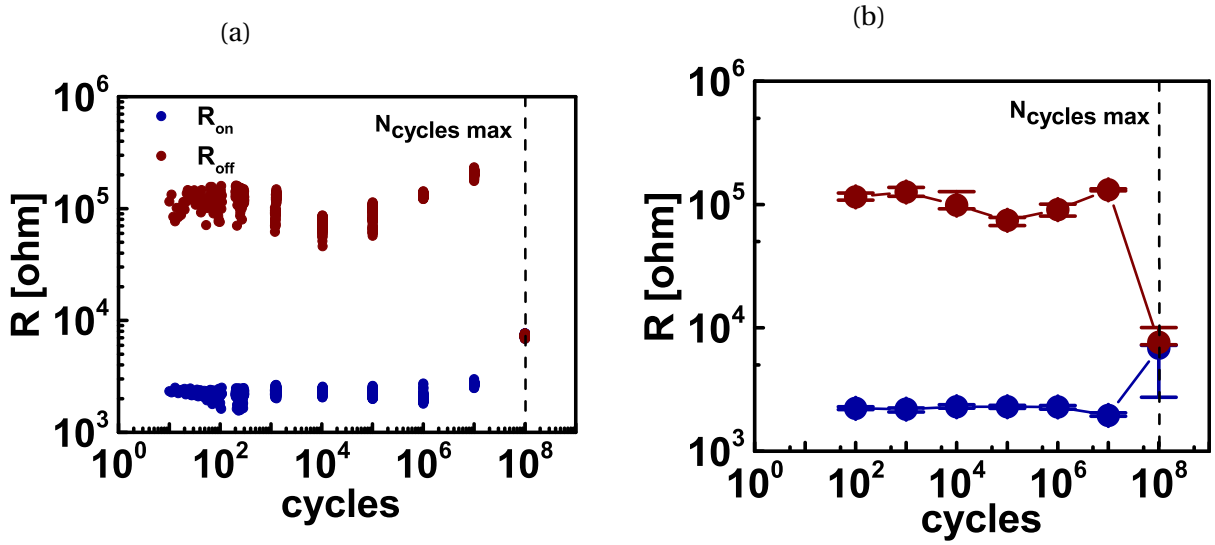
Figure 2.9: Typical endurance curves up to 10^8 cycles with 100 read every decades a) all reading points b) Standard deviation on 100 reading points. $N_{cycles\ max}$ represents the maximum number of cycle the device reached (W/HfO$_2$ (5nm)/CuTe$_x$ with I_c=1mA and $t_p$ulse=1µs)

Retention

Retention measurement (also called temperature stability) consists in controlling how long a given state (ON or OFF) is going to be stable in different temperatures. This feature characterizes the RRAM non-volatility behavior meaning how long RRAM keeps the information if it is let untouched. The cell is first programmed in ON or OFF state by Quasi-static or pulsed programming and then put in an oven under homogeneous temperature (80 to 350 °C). Read measurement is performed in a log scale interval (usually after 20min, 1h, 4h, 24h, 1 week...) at room temperature. As long as there is no resistance variation, the cell is stable, when there is a resistance change, it corresponds to the time to failure, t_{fail}, for a given temperature (Figure 2.10a). In this manuscript, a minimum resistance vari-

ation of 25% is chosen to consider failure. Using different temperatures
permits to extract different time to failure which decreases as temperature
increases (Figure 2.10b). This behavior can follow an Arrhenius law that
can be used to extrapolate the temperature where the technology would
still be stable after 10 years and allows to extract an activation energy re-
sponsible of the filament recreation or disruption depending if it is HRS
fail or LRS fail respectively (Figure 2.10c) [10–12].
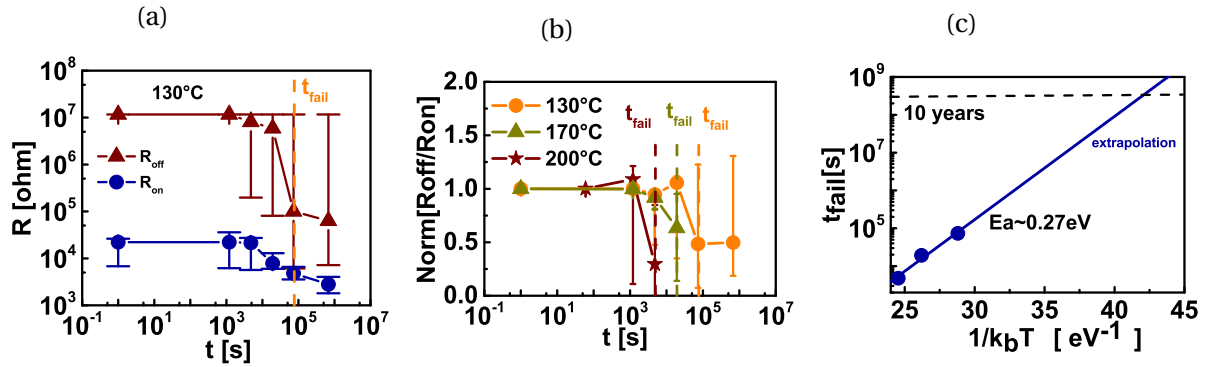
Figure 2.10: Typical retention curves at a) 130°C with t_{fail} extraction (standard deviation on 15
devices) b) comparison at 130°C, 170°C, 200°C and c) Arrhenius extrapolation at ten years with
activation energy extraction [13]

.

Programming window

Programming window or window margin corresponds to resistance ratio
between High Resistive State and Low Resistive State (R_{OFF}/R_{ON}). It can be
varied with programming parameters such as voltage applied during RE-
SET (V_r), compliance current during SET (I_c) and pulse time (t_{pulse}) in the
case of pulsed programming. More details will be given in chapter IV. This
characteristic is essential to integrate at the end RRAM in arrays. If window
margin is low, variability between the cells will have to be well controlled
to be sure that the distinction between the states can be done (Figure 2.11).
Otherwise, it may be a limitation for big arrays.
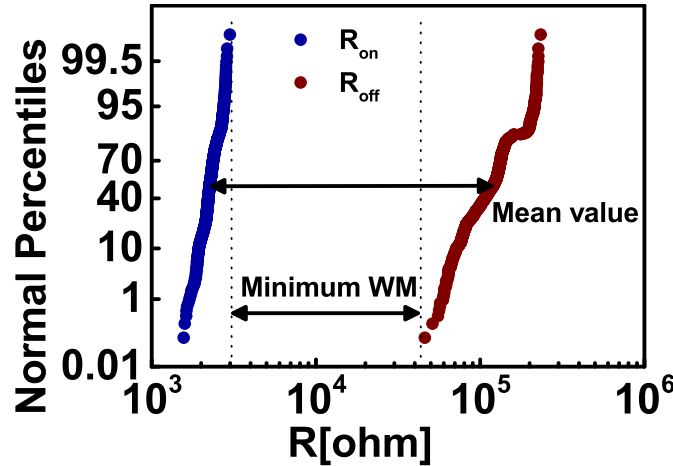
Figure 2.11: R_{ON} and R_{OFF} distribution associated with Figure 2.9. Mean value and minimum Window Margin can be extracted

2.4 Chapter II synthesis

This chapter introduced the required notions to apprehend the experimental results in the following of the manuscript. The different device integrations were explained and motivated. Standard measurement methods were detailed with RRAM endurance, retention and window margin extraction. In this work, each RRAM technology will be characterized by these three features. Different RRAM material combinations will be tested and their associated electrical response studied. In parallel, CEA-LETI invests in microscopic research to bring some observation on fresh and used devices. However, as switching mechanism phenomenon has not yet been observed and present a lack of comprehension, atomistic simulations have been developed. Interactions between RRAM layers can be investigated and results can give insights on mechanisms that could be at the source of a filament formation and disruption. Combining electrical characterization and atomistic simulation is beneficial to increase RRAM understanding and can give input for a complete RRAM modelling. This scope was covered in this work using Density Functional Theory (DFT), allowing to approve or refute some hypothesis resulting from electrical measurements. Atomistic simulations theory used in this manuscript is developed in the next chapter.

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Chapter 3

Atomistic simulation

3.1   Introduction/Objectives

As microscopic technics are not always efficient to visualize physical events, atomistic simulations are used to extract material properties non-accessible by experimental methods and to support or refute hypothesis coming from these observations. For example, in this work we will be interested in calculating the cost of introducing a copper atom in different oxides and see if it could be energetically favorable to compose a filament. Atomistic calculation gives access to known properties as well which help evaluating results veracity. Practically, it consists in calculating a structure composed of several atoms such as a crystal for example and resolve the famous Schrödinger equation to understand how these atoms are linked and how there electrons interact with each other.

Based on First Principle calculations (known as *ab initio* methods), Density Functional Theory (DFT) has proved to be efficient and successful in describing structural and electronic properties in a vast class of materials, ranging from atom and molecular levels to simple crystals, up to complex extended systems (including glasses and liquids) with a relatively small computational effort. For this reason DFT has become a common investigation tool, which is used in quantum chemistry and physics to find solutions to the fundamental equation that describes the quantum behavior of molecules and condensed matter systems, the Schrödinger equation. Note that the term *ab initio* does not mean without approximations, but it means without empirical or fitted parameters. This method does not need any calibration on an experimental base; it directly deals with electrons and with approximate quantum calculations. We have performed DFT calculations in order to study filament composition and formation in our different CBRAM. The results give some insights on different filament compositions depending on top electrode and oxide. Moreover, it allows to

explore thermodynamic and kinetic energies implicated in RRAM working principle for different technologies and extract some material parameters which can influence memory characteristics.

3.2 Density functional theory

3.2.1 History

Density Functional Theory is based on the time independent Schrödinger equation resolution which translates the classical mechanic energy conservation equation in quantum mechanics: total energy of a system is equal to kinetic plus potential energy. It is written as:

$$H\Psi = E\Psi \tag{3.1}$$

With Ψ the wave function related to the probability of finding an electron in a particular region of space, H the Hamiltonian operator which characterizes the kinetic energy plus the potential energy of a given wave function and E the total energy of the wave function. Any total energy, electronic properties, thermodynamic properties... of an element with a known electron structure can be calculated with this equation. However, the exact solution of this equation is only known for a single hydrogen atom which has only one electron. When there are more electrons, Coulomb interactions (interaction between electrons) have to be taken into account. In this case, each electron adds a variable to the wave function Ψ which becomes for N electrons at distance r_i of its nuclei $\Psi(r_1, r_2, ..., r_N)$. As it is not known how to solve Schrödinger equation with N variables, the first idea was to replace the wave function by a function which could be defined by one variable. In the end of the 20's Thomas [1] and Fermi [2] proposed then the electronic density ρ:

$$\rho(r_i) = \int ... \int \overline{\Psi}(r_1, r_2, ..., r_n) \Psi(r_1, r_2, ..., r_n) dr_1 ... dr_n \tag{3.2}$$

with $\overline{\Psi}$ the complex conjugate of Ψ. Unfortunately, the way to calculate exactly this function was not known and the approximation done presented some lack of theory and led to inaccuracies. Therefore, one of the first method to solve Schrödinger equation with N electrons consisted in approximating $\Psi(r_1, r_2, ..., r_N)$ and has been derived in the end of the 30's by Hartree and Fock. Without going into too much details, Hartree considered independent electrons in a central potential due to the core electrons

[3] and Fock introduced the Pauli Exclusion Principle allowing to approximate the wave functions with a Slater determinant[4]. This system has been refined by Dirac with a Slater determinant sum but it became onerous to calculate [5]. In 1964, Honenberg and Kohn established the theorem that bear their name [6]. It demonstrated that all properties of a system are determined by its electronic density ρ. This first part of their theorem filled the lack of theory of Thomas and Fermi's idea. In the second part, this theorem shows that the ground state energy of a wave function, E_0, is unique and is equal to the one that has the lowest energy:

$$\min E(\rho, r_i) = E_0 \tag{3.3}$$

Thus, minimizing a system energy is enough to obtain the ground state energy and density and so describe completely an electronic system ground state. Following this research, in 1965 Kohn and Sham found a method to approximate the system electronic density described by Thomas and Fermi with good accuracy [7]. Density functional theory is then established. It can be noted that even today none of exact functional densities are known and is still part of DFT approximations.

3.2.2 Solving Schrödinger equation

Kohn and Sham's approach

Kohn and Sham's idea is to approximate electronic density by replacing the system studied of real particles with an equivalent system composed of independent particles such as these two systems have the same density at ground state. The minimum of energy of this new system is equivalent to the real one and corresponding density can be obtained. Density depending on N wave functions $\varphi_i(r)$ of free particles can be expressed as:

$$\rho(r) = \sum_{i=1}^{N} |\varphi_i(r)|^2 \tag{3.4}$$

To solve Schrödinger equation, the total energy must be equal to HΨ in 3.1. It can be expressed as a sum of energies. Kohn and Sham chose kinetic energy, $E_{Kinetic}$, exchange-correlation energy, E_{XC}, external potential energy, $E_{V_{ext}}$, and Hartree energy, $E_{Hartree}$, and defined them such as the sum

depends on the electronic density:

$$E_{total} = E_{Kinetic} + E_{XC} + E_{V_{ext}} + E_{Hartree}$$

with

$$E_{Kinetic} = \frac{1}{2} \sum_{i=1}^{N} |\nabla \varphi_i(r)|^2$$

E_{XC} = has been approximated by several methods   (3.5)

$$E_{V_{ext}} = \int V_{ext}(r)\rho(r)dr$$

$$E_{Hartree} = \frac{1}{2} \int \frac{\rho(r)\rho(r')}{|r-r'|} drdr'$$

With φ_i the wave functions of free particles, r the distance between electrons and its nuclei, V_{ext} the external potential, ρ the electronic density. Exchange-correlation energy, E_{XC}, represents Hartree and Fock's exchange energy and correlation energy between electrons. It has been approximated by several methods leading to a hierarchical level of approximations. This functional choice has to be decided for any calculation and is commented below.

Functional approximation

To calculate exchange-correlation energy, several types of approximations have been developed leading to different inacurracy level. We will present Local Density Approximation (LDA) developed in the 80's refined with The General Gradient Approximation (GGA) in the 90's. LDA considers electrons in a homogeneous gas with N particles with a local density ρ_0. It implies that the exchange energy of the electrons is calculated as if they were in an homogeneous gas. The total energy calculated is then underestimated compare to experimental data. GGA takes into account inhomogeneous gas of electrons calculating local density variation. Exchange energy depends on $\rho(r)$ and $\nabla\rho(r)$ [8]. Calculations are then longer but have a better accuracy with experimental data for bond-lenghts and material enthalpies. However, for example, Van-der-Waals bond are not well represented and electronic band gap are generally underestimated. To improve GGA approximation, hybrid functionals can be used. However, they are computationally costly. Therefore, only punctual comparisions were performed to ensure some results.

$$E_{XC_{(LDA)}} = \int \rho(r)\epsilon_{xc}[\rho(r)]dr \qquad (3.6)$$

With ϵ_{xc} the local electronic energy [9–11].

Solving the equation

In this section, we present how Kohn-Sham equation is computationally solved. Presented parameters refer to the code, SIESTA, used in this manuscript.

Schrödinger's equation solution, giving final system electronic density, is obtained by iterative computation searching to minimize total energy ($\frac{\delta E_{total}}{\delta \varphi_i(r)} = 0$). To start calculation, the first density is obtained taking the sum of atom electronic densities of the system. A first approximation is done here. To calculate electronic density on an isolated atom, spherical symmetry is considered to be able to solve Kohn-sham equation which will depend only on a distance r (one variable). This solution is not exact but is close enough from the real one to start calculation and achieve self-consistency. After one iteration, results give a new electronic density which can be reinjected in the loop. Self-consistency is reached when density obtained is close to the one calculated at previous step (convergence criterion *DM.Tolerance* in SIESTA). However, this criterion is not enough to determine if system total energy has been minimized. Indeed if we take for example cos(x)= x, if x is reinjected, we obtain the same result which does not mean that cos(x) has been minimized; it is oscillating. Forces on atoms are then calculated and give new atom positions for the next iteration. System is called "minimized" when these calculated forces are smaller than a convergence criterion (*MD.MaxForceTol* in SIESTA).

3.2.3 Practical implementation

Forces calculation

In order to optimize atom positions in crystals, applied forces are calculated thanks to adiabatic or Born-Oppenheimer approximation and Hellmann-Feynman theorem [12, 13]. It allows to express forces in terms of atom positions, electronic density and electrostatic energy between atom nuclei. Born-Oppenheimer approximation consists in considering that electrons perceive nuclei as motionless. It can be justified by the fact that due to mass difference between nuclei and electrons, electronic motion is usually much faster than nuclear motion. This lemma allows to decompose the problem into two parts:

- the solution of the electronic equations under the potential due to the nuclei, which are assumed in fixed positions;
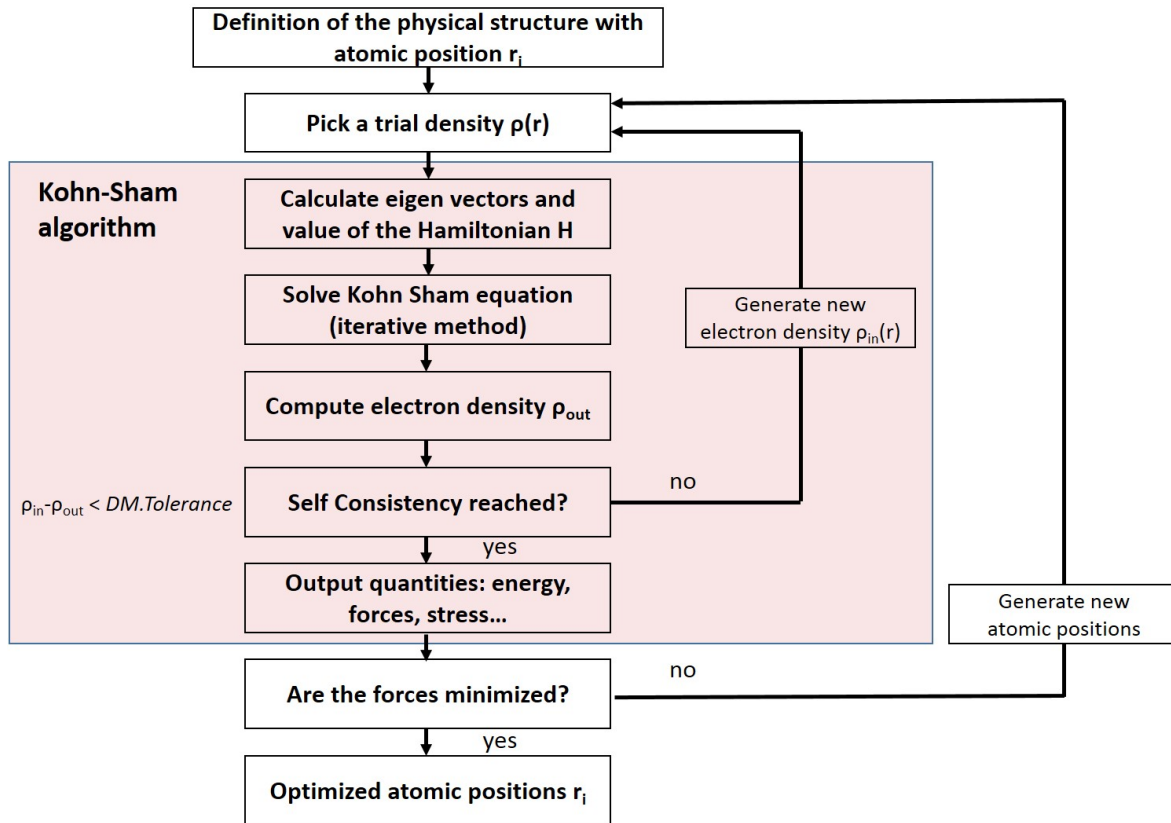
Figure 3.1: solving Kohn-Sham equation combined with Force minimization algorithm.

- the solution of the equations for the nuclei considered as classical particles prone to the potential generated by the electrons.

Pseudopotentials

In order to reduce time calculation, the full wave function on each atom is not calculated. Instead, only valence electrons are considered because core electrons do not participate to material bonding and do not affect material properties. For example, Silicon has 14 electrons and only 4 electrons are participating to bonding. Therefore, a method has been created to not take into account all core electrons, called pseudopotentials. These pseudopotentials, one for each species, reproduce the potential seen by valence electrons. In our calculation Trouiller Martins pseudopotential were used [14].

k-point sampling

Wave functions can be described in different spaces like in real space. However, one of the most efficient way to describe crystal density is the reciprocal space. In this case, the Brillouin zone (BZ) of a crystal (unit cell in reciprocal space) can be divided in a regular grid with k points ($k_{prs} = u_p \vec{b}_1 +$

$u_r \vec{b}_2 + u_s \vec{b}_3$ with $\vec{b}_n$ reciprocal lattice basic vectors) proposed by Monkhorst and Pack [15]. Some of these k points are equivalent, called high symmetry points, allowing to reduce the number of points per grid to calculate. If we solve Schrödinger equation for a periodic system, like a crystal, we need Bloch's theorem demonstrating that it is possible to solve Schrödinger equation for each value of k independently. In this case, solution can be expressed as a sum of terms with the form:

$$\varphi_k(r+R) = e^{ik.R}f_k(r) \tag{3.7}$$

with k inside the Brillouin zone vector, and $f_k(r)$ a periodic function in space with the same periodicity as the cell such as $f_k(r+n_1a_1+n_2a_2+n_3a_3) = f_k(r)$. The more k points are used, the more precise is the result. However, there is a trade-off between the accuracy and the computational cost. Since in our case we are interested in studying point defects, we will need relatively large cells with a large number of atoms. This implies a small size of the Brillouin zone ($V_{BZ} = \frac{(2\pi)^3}{V_{cell}}$). As a consequence, one obtain a good BZ sampling with a reduced number of k points.

basis functions

To define f_k, DFT calculations use either spatially extended functions (like plane waves), as in the ABINIT code, or spatially localized functions (like atomic orbitals), as in the SIESTA code used in this manuscript. The big advantage of SIESTA code is time calculation. As it is based on Linear Combination of Atomic Orbitals (LCAO) [16] it reduces matrix size to calculate. However, the three parameters defining basis functions need to be adjusted for each system studied: basis size (orbitals number, *SZ, DZ, SZP, DZP*), basis extension (orbitals radius, *Energy Shift*), Grid size (*Meshcutoff*). The disadvantage of this method is the lack of an absolute convergence criterion (there is no unique way to enlarge the basis set). In order to verify the accuracy of basis adopted for SIESTA calculations, it is good to compare results such as total energy and atomic positions with another method as ABINIT, at least for new materials.

3.2.4 Structures and defect calculations

Crystalline structures

To run a simulation, a material model needs to be chosen. To study solid state, crystalline structures are usually assumed. Crystallography researches provide a rich amount of resources with precise crystal description that

can be used for simulation initial conditions. For example, in this work, our Al_2O_3 is deposited as resistive layer and crystallizes in γ-phase. E. Menéndez-Proupin and G. Gutiérrez developed a structure of bulk γ–Al_2O_3 [17] that can be used to start simulations. This spinel-defective structure is composed of 40 atoms with 16 Aluminum atoms and 24 Oxygen atoms. This structure, is derived from a spinel $MgAl_2O_4$ with two missing atoms creating vacancies (see Figure 3.2).

The first step in DFT is to optimized atom positions in the unit cell of a crystal based on this model. If the given structure does not give a converged result, this model is not stable and does not exist; another one has to be found. For specific study such as punctual defect, bigger cell needs to be used to avoid too close defect interaction which is not well taken into account in DFT. A structure with several unit cells is then called *supercell* (see Al_2O_3 supercell Figure 3.3a).
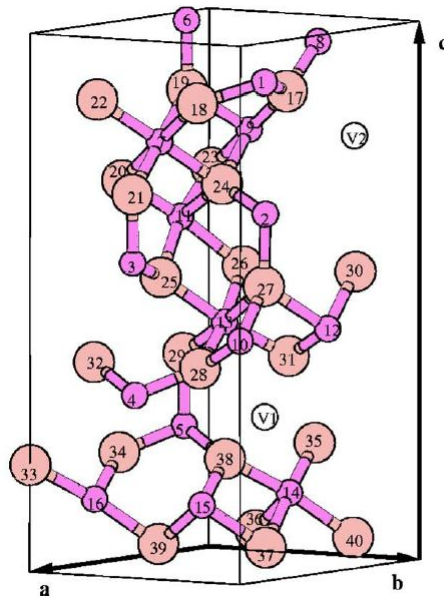
Figure 3.2: Schema of Al_2O_3 spinel defective structure. Al in orange, O in pink, vacancies in white.

Amorphous Structures

In our RRAM stack, layers are all amorphous materials. Ideally, an amorphous model would be chosen. However, characterization and modelling of the atomic and electronic structure of amorphous materials is a complicated task due to the random nature of the network. To generate such a model, one uses a method starting from a crystalline structure, called "melt and quench". Usually a supercell of crystalline material is relaxed by molecular dynamics: the structure is raised in temperature up to its melting point for a certain amount of time before cooling to room temperature.
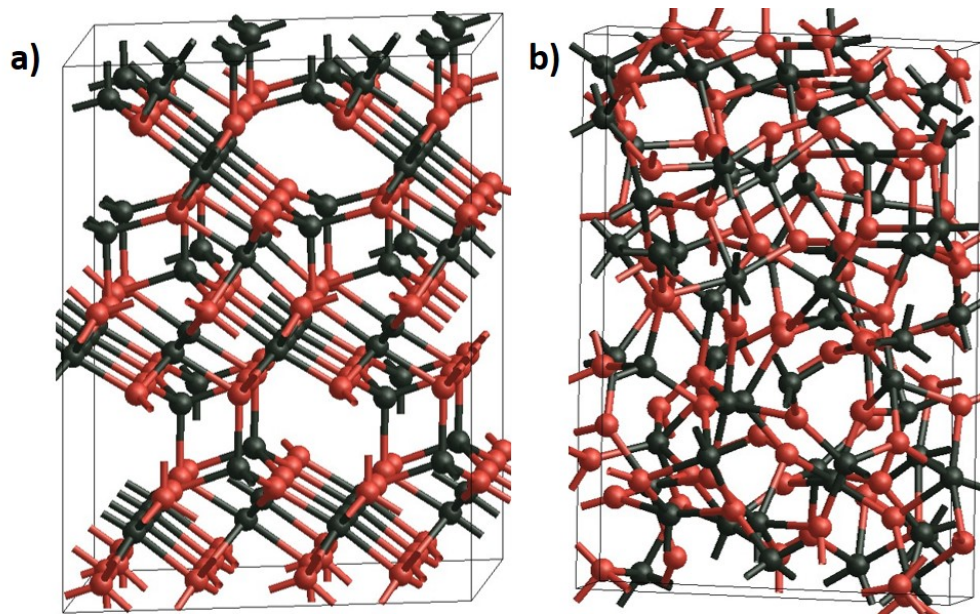
Figure 3.3: Al_2O_3 supercell used for calculations. O in red, Al in dark green a) cristaline structure with a densiy of 3.45g.cm^{-1} b) amorphous structure with a density of 3.1g.cm^{-1}.

Note that a structure with a lower density (close to experimental) can be artificially built by introducing defects such as vacancies or Schottky defect. If the structure does not crystallize again, a disordered structure is obtained (see amorphous Al_2O_3 calculated structure Figure 3.3b). Before using this amorphous model, one needs to check if electronic properties are still correct: material Band Gap needs to be without any defect level. This method is relatively long to relax and sometimes does not give satisfying results at the first shot (defect in the band gap...). Moreover, simulation of defects are much harder than in crystallized structure due to the unique position of each atom, more configuration needs to be treated. That's why amorphous model are usually not used for a complete study of a material but to compare simple calculation with crystalline model to confirm or modulate its results.

Defects in crystal structures

Material's electronic properties are often controlled by the electrically active defects and impurities, which usually are a small portion of the total number of defects (?%). In RRAM switching mechanism, defect introduction in dielectric layer could help to form a conductive path. In this respect state of the art, DFT is a useful method to elucidate the properties of point defects and impurities in crystalline structures with relatively low defect concentrations. This study can then be interpreted to validate or refute hypothesis coming from RRAM electrical results or microscopic observation

from an atomic point of view. This calculation is used in this work to find the most favorable defect that could form a filament. This thermodynamic method is detailed in the following of the chapter.

Diffusion of Defects

After studying defect properties in dielectrics, the most favorable defect introductions can be determined. To go further, their movement in the oxide can be studied. Diffusion of defects in solid state can be investigated in DFT with a popular algorithm called "Nudged Elastic Band" (NEB). This study gives access to the energy diffusion barrier needed to move an atom from one site to another and to a favorable path (3.3.2). In this work, this calculation is used to determine which atoms can move in a given oxide to form and disrupt a filament. More details are given in the next section.

3.3   Method

3.3.1   Thermodynamic of the defects

Knowing the cost for introducing a defect in resistive layer is of great interest to learn the RRAM switching microscopic mechanism. First, we study the thermodynamic of the defects in order to determine the most favorable introduction calculating defect formation energy. Resistive layer existing defects due to fabrication steps need to be established. In this case, the ideal way to study a defect formation energy would be to simulate the fabrication process. But, it is impossible to simulate a process flow. To overcome this problem, a zero temperature and zero pressure DFT simulation is performed and is combined with thermodynamic chemical potentials theory. The idea is to use the total energy of a system, obtained by DFT to calculate the Gibbs free energy, ΔG. The Gibbs free energy is the cost at which one atom of a given species is exchanged between the oxide and the surrounding. In our case, Gibbs free energy is reduced to formation enthalpy of the defect, ΔH. Temperature and entropy effects are then neglected which is relevant in a solid state at room temperature (~0.1eV).

Each species need a total energy reference, defined by chemical potentials, μ. Some charges, q, can be exchanged as well and need to be taken into account. Result follows this equation:

$$\Delta H = U_{Defect} - U_{Pristine} + \sum n_i \cdot \mu_i + q \cdot (E_{Fermi} + \Delta V + E_{VB}) \qquad (3.8)$$
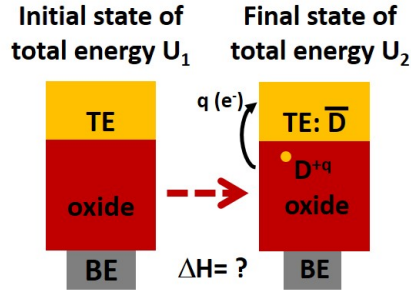
Figure 3.4: Illustration of initial and final states calculated to extract defect formation energy ΔH. D^{+q} the defect introduced in the oxide, $\overline{D}$ the complementary defect introduced in TE, q the charges exchanged.

With ΔH the formation enthalpy of the defect, U_{Defect} the defect total energy, $U_{Pristine}$ the initial state total energy, n_i and μ_i the number of chemical formula and the reference chemical potential for the exchange, q the charges exchanged in the system, E_{Fermi} the electrode Fermi level considered in contact, ΔV the electrostatic energy shift[18] and E_{VB} the highest valence band energy level.

We defined three different cases:

- oxide post process, deposited on a metallic bottom electrode (BE). Oxide is in contact with surrounding gas and BE.

- oxide after top electrode deposition (TE) is then in contact with BE and TE.

- oxide during RRAM switch in contact with TE and BE but can be initially defective.

In the two last cases, the Gibbs free energy will be calculated as the exchange between the dielectric and the TE. The defect created in oxide will then generate a complementary defect in TE. For example, if an oxygen is extracted from the oxide, it creates then an oxygen vacancy (V_O) in it plus an oxygen interstitial (O_i) in TE. In the TE post process case, as we consider exchanges between oxide and TE, formula for a defect charged +q, D^{+q}, generating a complementary defect $\overline{D}$ in TE becomes:

$$\Delta H = U_{oxide:D^{+q}} - U_{oxide} + U_{TE:\overline{D}} - U_{TE} + q \cdot (E_{Fermi} + \Delta V + E_{VB}) \quad (3.9)$$

With D, the defect introduced in oxide (for example: Cu_i^{+1}), $\overline{D}$ the complementary defect introduced in TE (for example: V_{Cu}) and E_{Fermi} the electrode Fermi level in contact.

Finally, for RRAM working principle case, we study the thermodynamic in defective oxide. Reference for dielectric becomes for example a V_O-rich oxide (oxide with one V_O defect). V_O in oxide can come from oxide process condition in O-poor atmosphere or O exchange with TE. Results are based on the following equation:

$$\Delta H = U_{oxide:D_0^{+q_0}+D^{+q}} - U_{oxide:D_0^{+q_0}} + U_{TE:\overline{D}} - U_{TE} + (q-q_0) \cdot (E_{Fermi} + \Delta V + E_{VB})$$

$$(3.10)$$

With $D_0^{+q_0}$, the defect initially present in defective oxide due to process or RRAM life, D the studied defect and $\overline{D}$ its complementary defect in TE.

Results give a slope depending on electrode Fermi level E_{Fermi}. To extract the value with the TE considered in contact, this equation can be represented in the range of the oxide bandgap (see Figure 3.5a). Usually, only the lowest values are represented which gives the dashed line. Fermi level that need to be considered is then deduced with a band alignment between oxide and TE (see Figure 3.5b).

(a) Formation enthalpy calculation of defects in an oxide depending on Fermi level.
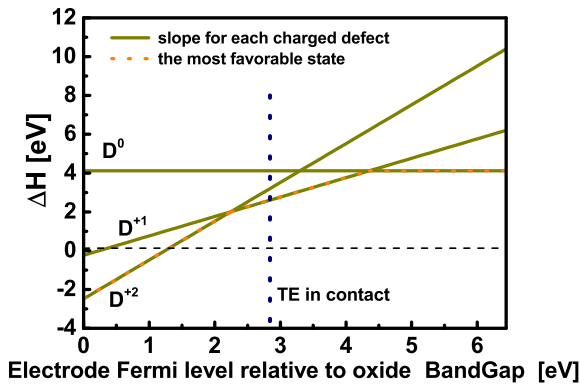
(b) schema of a band alignment between an oxide and a metal.
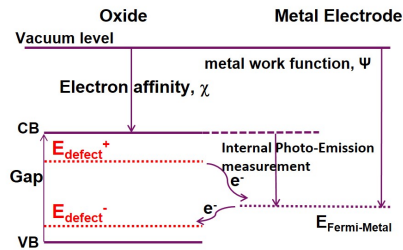
Figure 3.5: Example of defect, D, formation energy results with a metal as TE. TE Fermi level is represented and placed on a) with a band alignment shown in b). In a), D^{+1} is the most favorable state if the oxide is in contact with the chosen TE.

3.3.2 Diffusion of defects

Transition State Theory (TST)

In order to study diffusion of defects, DFT calculation tools are based on the transition state theory (TST). TST is used to describe how a chemical reaction occurs, and is based on the following assumption: between two

stable states, called reactant and product, it exists an intermediate state, known as the transition state which is higher in energy. The theory assumes that each intermediate is long-lived enough to reach a Boltzmann distribution of energies before continuing to the next step. When the intermediates are very short-lived, TST can not be applied: transition states need to be in quasi-equilibium with the reactants and products.

TST was developed with the concept of a potential energy surface. The progress of a chemical reaction is described as a point in a potential energy surface with coordinates in atomic momenta and distances. The point passes through a col or saddle point and reaction rate is determined by the motion of the system through that col. One of the most important hypothesis is that transition states are in quasi-equilibrium with the reactants. It can be noted that the theory assumes the reaction system will pass over the lowest energy saddle point on the potential energy surface. While this description is consistent for reactions occurring at relatively low temperatures, at high temperatures, atoms populate higher energy vibrational modes; their motion becomes more complex and collisions may lead to transition states far away from the lowest energy saddle point. In this case, another alternatives to transition state theory have to be chosen. TST postulates three major factors that determine whether or not a transition will occur:

- The concentration of the activated transition state.

- The rate at which the transition state breaks apart.

- The mechanism by which the transition state breaks apart; it can either be converted into a new stable state, or it can "revert" back to the initial state.

The reaction rate depends on the probability of finding the system at the transition state relative to the entire reactant state and on the rate of crossing from one state to another at the transition state. To realize this calculation, a definition of the transition state needs to be given and in order to calculate the probability of being at the transition state, the full partition function of the transition state region and the reactant region need to be evaluated. This is computationally challenging and costly when using density functional theory. Therefore, to simplify this calculation, two assumptions are added:

- The saddle points on the potential energy surface represent "bottle neck" regions that separate reactant from product configurations.

- The potential energy surfaces around the reactant configuration and the saddle point are locally harmonic (quadratic).

The first assumption solves the issue of determining the transition state by defining it as the hyperplane normal to the unstable direction at the saddle point. The second assumption allows to have a second order Taylor series expansion of the potential energy surface at those points leading to a finite number expression to determine the resulting configuration integrals needed in TST. These two approximations are relevant for many solid-state reactions. Indeed, the energy barriers are often higher compared to the average kinetic energy in the system ($k_B T$) ensuring that the system reaches a local equilibrium between reactive events. To the contrary, if the barriers are relatively small compared to $k_B T$, the history of the trajectory is an important factor in determining the reaction rate. This would require the use of a more sophisticated statistical model. In another hand, the harmonic approximation is often valid in solid-state reactions. Near the saddle points, the potential energy rises rapidly and creates a small bottleneck region. As counter-example, to describe protein reactions, the potential energy can be relatively flat in the region around the saddle point and is not well characterized by harmonic expansion of the saddle point.

Assuming these assumptions, the first step is to find the saddle point associated with the reaction in question. There are different techniques that can be used. In this manuscript, we use Nudged Elastic Band calculations (NEB).

DFT calculation: NEB

The goal is to extract the energy cost of moving a defect in a structure and extract the defect acrivation energy to go from one site to another. In DFT, diffusion of the defects can be studied by a method called Nudged Elastic Band (NEB) calculations. It is a method for finding the minimum energy path (MEP) between two defined points and the potential energy maximum along this MEP is the saddle point energy which gives the activation energy barrier (see Figure 3.6a)[19]. The method works by optimizing a number of intermediate images along the reaction path. Each image finds the lowest energy possible while maintaining equal spacing to neighboring images. This constrained optimization is done by adding spring forces along the band between images and by projecting out the component of the force due to the potential perpendicular to the band (see Figure 3.6b). Example of results can be seen Figure 3.7.

(a) Schema of a potential atom diffusion in an energy surface between two chosen states.
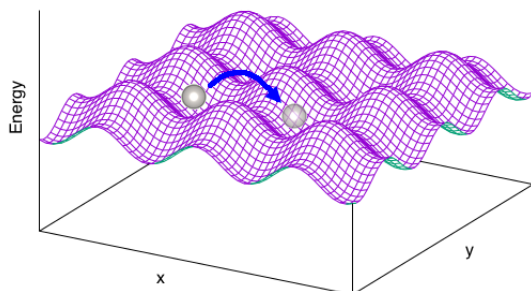
(b) Schema of NEB solution generating several images on the most favorable path.
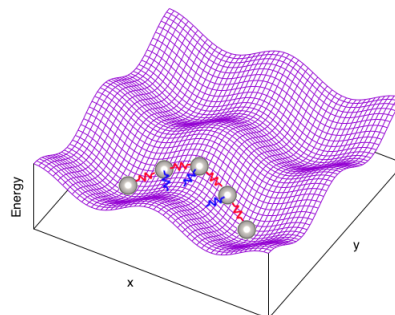
Figure 3.6: NEB illustrations.
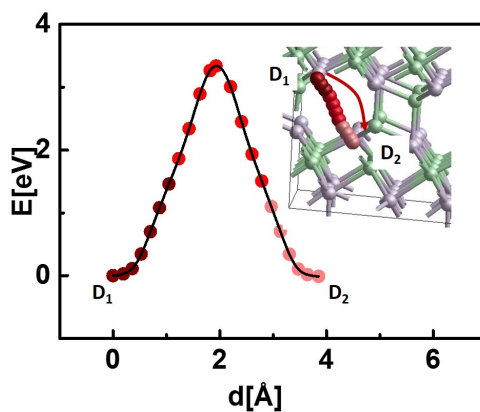
Figure 3.7: Example of migration barrier with associated path screen shots for a defect D_1 going to D_2.

In order to optimize NEB calculation, one developement consists in converging one of the images to a saddle point (as opposed to all the images being evenly spaced along the reaction coordinate). This is called climbing image NEB and include that the highest energy image is at a saddle point [20]. To this aim, this particular image does not feel the spring forces along the band and the force along the tangent is inverted. Consequently, this image tries to maximize it's energy along the band, and minimize in all other directions. When this image converges, it will be at the exact saddle point. It can be noted that in this case, the spacing between images on either side of this image will be different. Some minimization with regular NEB method need to be performed before to define the highest energy image and have a good estimate of the reaction co-ordinate around the saddle point. All NEB calculations presented in this manuscript, are performed with this method.

3.4   Chapter III synthesis

In this chapter, atomistic simulations based on Density Functional Theory (DFT) are presented. History of DFT is exposed and the final calculation theory and algorithm is explained. It relies on first principle calculations which deal directly with electrons and solve Schrödinger equation. It does not need any fitting parameters but some approximations are made to calculate a system with several electrons. To start this calculation, a structure needs to be chosen such as a crystal phase. Material properties can then be extracted such as electronic, thermodynamic properties. The second part of the chapter explains how results can be interpreted. As RRAM switching mechanism is not yet fully explained, these calculations can bring some insights on filament formation and disruption. In our work, two types of study are presented. First, thermodynamic study is performed in oxide to determine the most favorable point defects that could lead to a conductive path formation. DFT calculation gives structure total energy for initial and final state; for example without and with defect. Defect formation energy can then be extracted. Afterward, diffusion of defects is investigated to determine which species can move in the oxide. This is done by Nudge Elastic Band (NEB) method which is based on transition state theory (TST). It allows to calculate a Minimum Energy Path between two defined points and extract its migration energy barrier. At the end of this chapter, example of graphic results can be found. Simulation results presented in the next chapter will be based on these methods and same type of graphics will be presented.

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Chapter 4

RRAM filament composition by atomistic study

4.1 Introduction/Objectives

This chapter is the first of the two chapters combining electrical characterization and atomistic simulation to understand the global behavior of RRAM. References will be made to chapters II and III regarding the description of the characterization protocols and atomistic simulations.

This chapter is dedicated to $Al_2O_3/CuTe_xGe_y$ CBRAM mechanisms at the microscopic level. As RRAM working principle depends on stack materials and needs to be observed at nanometer resolution, switching mechanism understanding is still challenging. We performed electrical tests with samples having different TE, BE and Al_2O_3 thickness. Devices are integrated in 1-Resistor (1R) and 1-Transistor 1-Resistor (1T1R) configurations to investigate different electrical answers during forming depending on bottom electrode and polarization voltage. Obtaining different electrical answer changing TE polarization, atomistic simulations are used to propose, at microscopic level, filament formation differences.

We realize a thermodynamic study for possible ion exchanges between Al_2O_3 and CuTe-based layers to isolate species that could form a filament. We assume two cases: stoichiometric and defective γ-Al_2O_3 as a model for resistive layer. For the most favorable exchanges, we study defect diffusion and extract activation energy employing Nudge Elastic Band method in DFT. Finally, we combine experiment and simulation to highlight the impact of oxygen and aluminum point defects in Cu ion insertion and diffusion while Te ion comes out unfavorable. A Cu/V_O based hybrid filament

model is proposed and Aluminum Vacancies (V_{Al}) impact on forming process is discussed.

4.2 Basic review on RRAM working principle

RRAM technologies are based on formation and disruption of a conductive filament (CF) in an electrolyte sandwiched between a top electrode (TE) and a bottom electrode (BE) [1]. Depending on the nature of top electrode, filament can be made of oxygen vacancies (OXRRAM) or metal ions (CBRAM). Despite research devoted to CF understanding in RRAM, microscopic mechanisms are not conclusive. Most approaches in modelling are considering only one chemical element [2, 3] whereas filament composition is probably more complex. One hypothesis supports that oxygen vacancies (V_O) assist copper in the switching mechanism [4–7].

This manuscript focuses its study on oxide-based CBRAM. Its working principle relies on a Cu-rich conductive filament formation inside an insulating layer during forming and SET operations [8]. This phenomenon, partially reversible (during RESET operation), allows switching between a Low Resistive State with ON resistance (R_{ON}) and a high Resistive State with OFF resistance (R_{OFF}) as illustrated in Figure 4.1a. Filament formation in Oxide-based Conductive Bridge RAM involves a Cu-rich conductive filament inside an oxide based insulating layer [9]. These mechanisms are not well understood, so we explore the impact of each chemical element composing Al_2O_3/Cu-based CBRAM.

4.3 Experimental observations

4.3.1 Studied samples

Our measurements are done on different RRAM samples with a BE / Al_2O_3 / $CuTe_xGe_y$ structure (see Figure 4.1a). Large area cells (μm^2) are integrated in 1R or 1T1R configurations. 3.5 to 5nm of amorphous a-Al_2O_3 is deposited by ALD at 300°C or by PVD on different PVD bottom electrode (TiN, Ta and W). 20nm of Cu or $CuTe_xGe_y$, deposited by PVD, is used as top electrode (TE).

(a) Schematic working principle of the Al_2O_3/$CuTe_xGe_y$-RRAM studied in this work. Copper filament (orange) is visualized inside dielectric layer
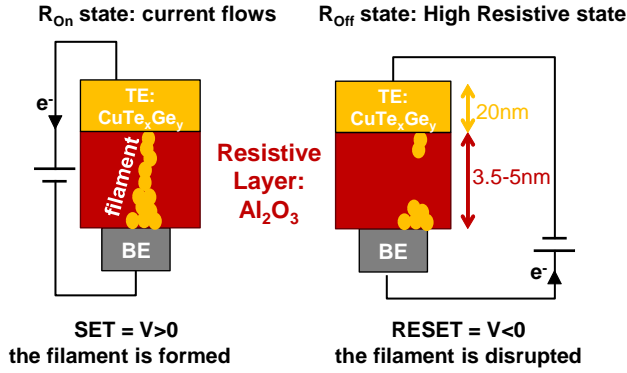
(b) I(V) curve comparing direct (F) and reverse ($\overline{F}$) forming depending on TE polarization (V_{TE}) in W/Al_2O_3(5nm)/$CuTe_xGe_y$ sample
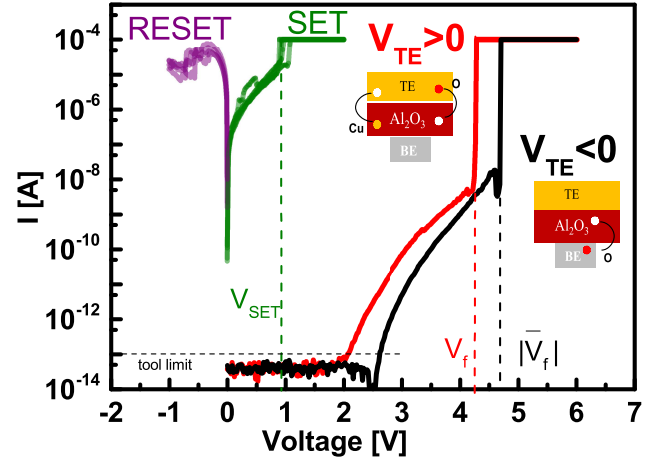
Figure 4.1: Schematic working principle and I(V) curve Al_2O_3/$CuTe_xGe_y$-RRAM

4.3.2 Polarization effect

One of the subject in oxide-based CBRAM is to investigate if there is metal coming from TE and oxygen vacancies forming the conductive path, as this technology is a result of OxRRAM and CBRAM combination. In order to detect if species forming Al_2O_3/$CuTe_xGe_y$ filament are sensible to the electric field, electrical characterization are performed using different polarization.

Figure 4.1b shows typical current-voltage (I-V) characteristics for Al_2O_3-based CBRAM. To investigate the impact of polarization, two types of forming are studied: direct forming, F, and reverse forming $\overline{F}$. Direct forming is done at $V_{TE} > 0$ and reverse forming at $V_{TE} < 0$. Forming voltage, V_f, can be extracted from this quasi-static measurement (see chapter II) and can be correlated to alumina breakdown electric field (E_{BD}). E_{BD} measurement of 8-9MV/cm shows good agreement with data reported in literature [10], indicating that forming is related to partial oxide breakdown. In other hand, SET voltage, measured at 1V, is significantly reduced with respect to forming voltage. Moreover, typical OFF state resistance (R_{OFF}) of $1.5x10^6 \Omega$ (obtained after RESET) is measured while initial resistance (measured before forming) is superior to $10^{13} \Omega$, indicating that initial structure is not recovered. Thus, SET process requires less energy and may imply different mechanisms. It can be noted that V_f is slightly smaller when TE is positively polarized ($V_{TE} > 0$). In the following, $\overline{V_f}$ will refer to the forming voltage when TE is negatively biased ($V_{TE} < 0$).

Figure 4.2 compares direct forming voltage V_f ($V_{TE} > 0$) and reverse forming voltage $\overline{V_f}$ ($V_{TE} < 0$) for the different samples. V_f is always revealed smaller than $\overline{V_f}$ independently of BE, deposition technique, oxide thickness, TE or measurement temperature.
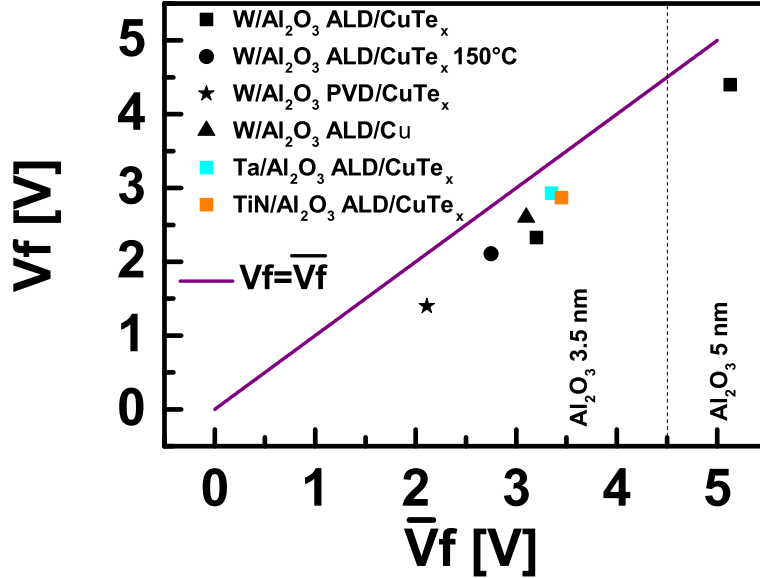
Figure 4.2: Comparison between direct forming F ($V_{TE} > 0$) and reverse forming $\overline{F}$ ($V_{TE} < 0$) for different BE / Al_2O_3 / $CuTe_xGe_y$ structures

This observation motivates a deeper memory study in both cases. Since most of the devices are stuck in SET or RESET states, reverse forming does not lead to satisfying cycling reliability. We thus studied them in direct polarization after F or $\overline{F}$. After reverse forming $\overline{F}$, partially breaking down the oxide, there is a first reset with TE positively polarized in order to erase the sample. Finally, direct forming is done and standard cycling is performed (see Figure 4.3).

Cell stability in temperature after $\overline{F}$ and F is then compared in Figure 4.4. This experiment consists in measuring resistance evolution over time at 200°C. In the case of $\overline{F}$, High Resistive state is not maintained after 20min at 200°C and Low Resistive state starts to increase after 24h. In the case of F there is no resistance change after 24h. As a first conclusion, filaments formed during direct and reverse forming are different. It can be noted as well that after $\overline{F}$, cells need higher Set and Reset Voltages to be operated for a given window (not shown).

In order to figure out if both filaments have the same type of conduction, resistance measurement at different temperatures is analysed. This exper-
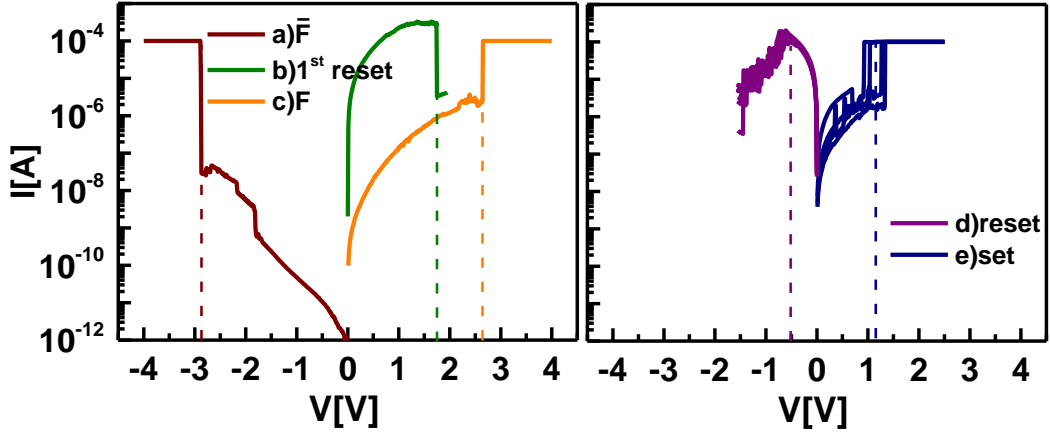
Figure 4.3: I(V) curve and interpretation of a W/Al$_2$O$_3$(3.5nm ALD)/CuTe$_x$Ge$_y$ cell being formed by a) reverse forming and then b) 1st reset and c) formed again positively before d) and e) standard cycling
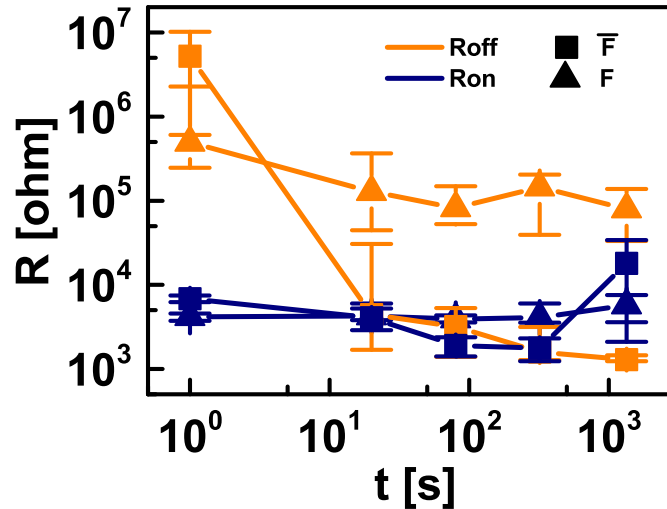
Figure 4.4: Retention comparison between direct F and reverse $\overline{\text{F}}$ forming at 200°C with I$_{SET}$=100μA for W/Al$_2$O$_3$ ALD 3.5nm/CuTe$_x$Ge$_y$

iment consists in measuring the resistance from 25 to 80°C. Initial state needs to be reached back to 25°C to be sure that resistance evolution is not due to a filament change. Figure 4.5a shows Resistance vs temperature evolution (R vs T). Activation energy, E$_a$ can be extracted from this characteristics assuming an Arrhenius dependence $R \propto R_0 \exp(\frac{E_a}{kT})$. If E$_a$ is high, electronic transport is activated in temperature, supporting a trap assisted conduction as it can be seen for R$_{off}$ (Figure 4.5b) whereas for R$_{on}$ a non activated electronic transport supports a metalic conduction. There is no differences between F and $\overline{\text{F}}$ confirming a filamentary type in both cases.
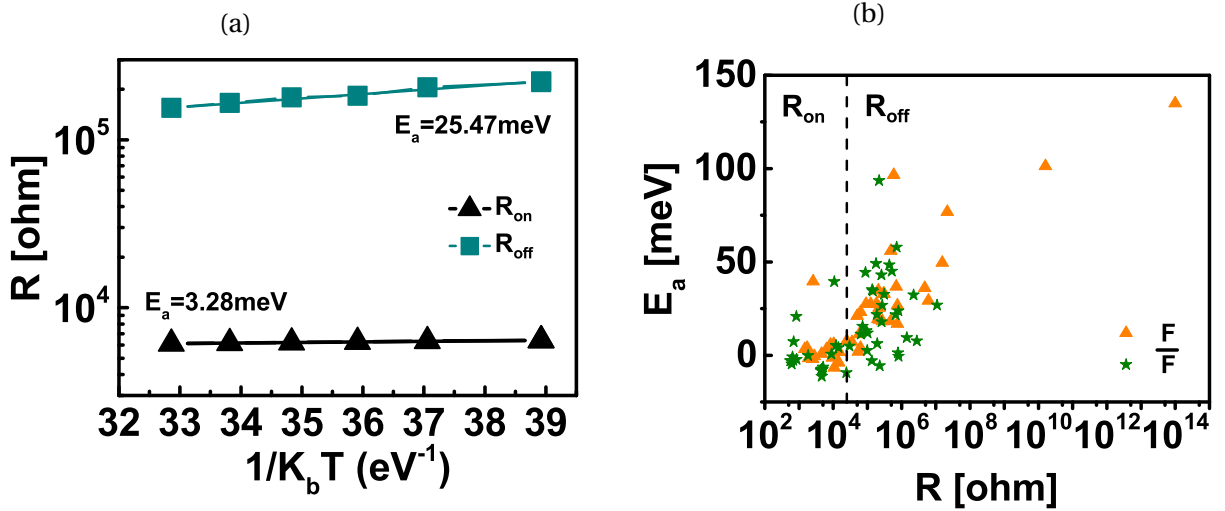
Figure 4.5: a) Resistance measurement from 25°C to 80°C to extract b) Energy of electronic transport for different resistances after F and $\overline{F}$ (W/Al_2O_3 ALD 3.5nm/$CuTe_xGe_y$).

4.4 Simulations

These experimental results show a difference between filament formation and stability depending on TE polarization. First principle calculations are then used to get more information at microscopic level. In the first part, thermodynamic of defects are studied in three cases: existing defects after Al_2O_3 deposition, after TE deposition and during RRAM operation. In a second part, defect diffusions are investigated.

4.4.1 Simulation framework

For alumina, a 160-atoms supercell consisting of four γ-Al_2O_3 unit cells is calculated (see Table 4.1) [11]. This structure is the closest crystalline form of our amorphous ALD material with a density of 3.45 g.cm^{-3} vs the measurement value of 3.1 g.cm^{-3}. Different positions are tested for each defect, especially for interstitials, up to 4 inequivalent sites are compared (see Figure 4.6). Detailed calculation parameters can be found in Annexe.

The band gap obtained at 3.43eV is corrected in G0W0 at 6.5 eV which corresponds to the one measured by ellipsometry [12]. As expected, this result of 3.43eV is lower than 7-8eV reported in literature due to GGA approximations, well known for underestimating dielectric bandgap. Corrections can be done to extract exact values and estimate error on other results [13]. For TE, we used a 96-atom supercell consisting of eight Cu_2Te_3Ge unit cells [14]. This structure is the closest crystalline form of our amorphous PVD material with a density of 6.0 g.cm^{-3} vs 6.1 g.cm^{-3} (measured).
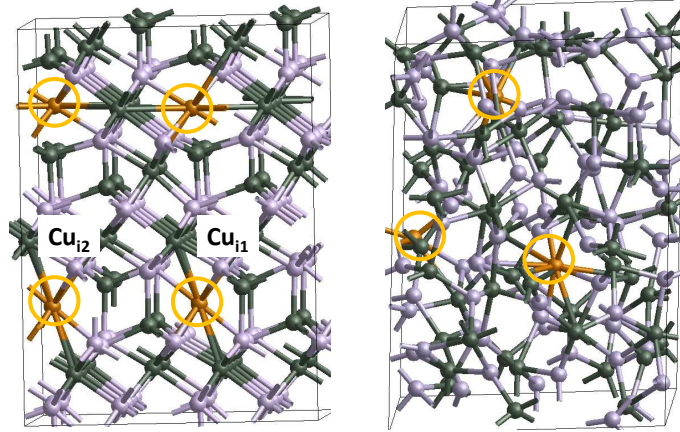
Figure 4.6: $\gamma-Al_2O_3$ and $a-Al_2O_3$ structure with different copper interstitial positions circled in orange. O in purple, Al in green black, Cu in orange. Cu_{i1} and Cu_{i2} are mentioned and used for migration barrier calculation

All results are based on a band alignment between band-gap of alumina and Cu_2Te_3Ge which is done considering

- G0W0 gap correction with an opening of more than 2eV at conduction band and -0.5 eV at valence band

- Internal Photo-Emission measurement of the barrier of Al_2O_3/Cu_2Te_3Ge at 3.6eV [15, 16].

To complete the study, an amorphous a-Al_2O_3 model with a density of 3.1 g.cm^{-3} is implemented (see Table 4.1). This model is generated using the melt and quench method (see chapter III): the crystalline triclinic γ-Al_2O_3 is used for the initial structure at a lower density with the four γ-Al_2O_3 unit cells considered above. It is melted at 2800K during 10ps and cooled to 300K for 10ps with 1fs time step. 1 k-point is used during molecular dynamics while 2*2*2 k-points are used for defect calculations. Band gap is obtained free of defect at 3.3eV against 3.4eV in crystalline structure.

Table 4.1: Calculated lattice parameters and angles for crytalline $\gamma-Al_2O_3$ and amorphous $a-Al_2O_3$ structures

	a(Å)	b(Å)	c(Å)	α(deg)	β(deg)	γ(deg)	V(Å^3/cell)	ρ(g/cm^3)
γ-Al_2O_3	11.51	11.43	13.81	89.26	90.00	120.20	392.35	3.45
a-Al_2O_3	11.30	11.06	13.84	90.20	87.85	119.69	375.29	3.1

4.4.2 Thermodynamic results

Al_2O_3 **post process defects**

In this section, we first study Al_2O_3' s native point defects that may appear after deposition. Calculations are based on the following equation (more details in chapter III):

$$\Delta H = U_{Defect} - U_{Pristine} + \sum n_i \cdot \mu_i + q \cdot (E_{Fermi} + \Delta V + E_{VB}) \qquad (4.1)$$

With ΔH the formation enthalpy of the defect, U_{Defect} the defect total energy, $U_{Pristine}$ the initial state total energy, n_i and μ_i the number of chemical formula and the reference chemical potential for the exchange, q the charges exchanged in the system, E_{Fermi} the electrode Fermi level considered in contact, ΔV the electrostatic energy shift [13] and E_{VB} the highest valence band energy level.

Results are reported in Figure 4.7. It shows the formation enthalpy of intrinsic Al_2O_3 defects depending on oxygen concentration during deposition process (from $\mu_O = \frac{\mu_{O2}}{2}$ to metal-rich condition) and considering a bottom electrode with a work function close to W. It points out that deposited Al_2O_3 may be rich in aluminum Frenkel pair (Al_{FP}) and aluminum vacancies (V_{Al}) charged -3 for O rich condition.
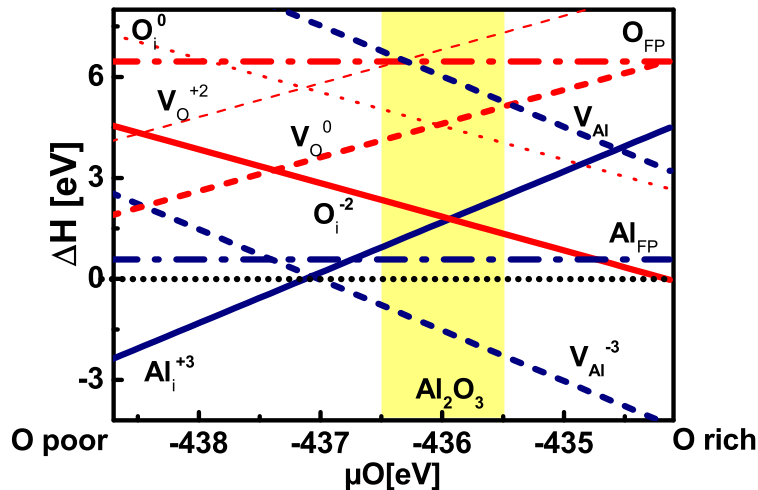
Figure 4.7: Formation enthalpy calculation of intrinsic Al_2O_3 defects. W Fermi level is considered. Yellow zone highlights stoichiometric Al_2O_3 process conditions.

To summarize these results: deposited Al_2O_3 **may be rich in aluminum Frenkel pair** (Al_{FP}) **and aluminum vacancies** (V_{Al}) **charged -3 for O rich condition.**

Al_2O_3 **defects after** $CuTe_xGe_y$ **deposition**

Then, we studied aluminum point defects after $CuTe_xGe_y$ deposition. As we consider exchanges between Al_2O_3 and $CuTe_2Ge_3$, formula for a defect charged +q, D^{+q}, generating a complementary defect $\overline{D}$ in TE becomes:

$$\Delta H = U_{Al_2O_3:D^{+q}} - U_{Al_2O_3} + U_{CuTe_2Ge_3:\overline{D}} - U_{CuTe_2Ge_3} + q \cdot (E_{Fermi} + \Delta V + E_{VB})$$
(4.2)

With D, the defect introduced in Al_2O_3 (for example: Cu_i^{+1}, Te_i^{-2}, V_O^0, V_{Al}^{-3}), $\overline{D}$ the complementary defect introduced in TE (for example: V_{Cu}, V_{Te}, O_i, Al_i respectively) and E_{Fermi} the electrode Fermi level in contact (for example W, Cu, Pt or Ti).

Results are presented in Figure 4.8 and the lowest defects are charged. After $CuTe_xGe_y$ deposition, considering charge of species and a Fermi level close to Cu, the most favorable interstitials and vacancies we could obtain are respectively: Copper interstitial (Cu_i^{+1}), Aluminum vacancy (V_{Al}^{-3}), Germanium interstitial (Ge_i^{+2}), Oxygen Vacancy (V_O). Tellurium interstitial (Te_i^{-2}) appears as unfavorable. It can be noted that Ge is used to stabilize CuTe layer and to keep it amorphous during integration process, to prevent any segregation and phase separation. Typically, 10-20% Ge is used [17, 18] in CuTe alloys. As a consequence, Ge is not expected to have any impact in the electrical behaviour of CuTe. Moreover, CuTe bound is polar and can easily be broken in $Cu^{\delta+}$ and $Te^{\gamma-}$ ions. They will be mobile under the electric field. Ge calculations are just used to confirm this affirmation. We will thus focus on Cu and Te elements in the last section.

To summarize these results: the most favorable defects that can appear in Al_2O_3 **after** $CuTe_xGe_y$ **deposition are: Copper interstitial (Cu_i^{+1}), Aluminum vacancy (V_{Al}^{-3}) and Oxygen Vacancy (V_O). Tellurium interstitial (Te_i^{-2}) appears as unfavorable. Germanium interstitial (Ge_i^{+2}) is less favorable than** Cu_i **and is just used to stabilize CuTe layer.**

Al_2O_3 **defects during RRAM operation**

Finally, for CBRAM working principle, we study the case of copper in defective alumina. Reference for oxide becomes either a V_O-rich Al_2O_3
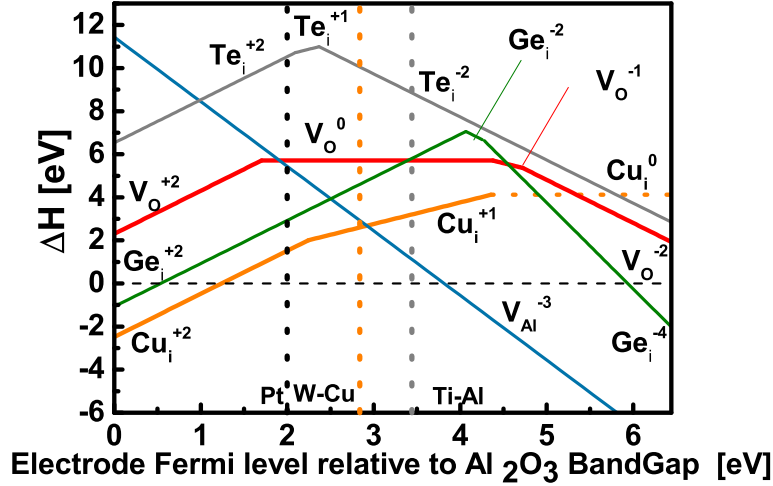
Figure 4.8: Formation enthalpy calculation of defects in $Al_2O_3/CuTe_xGe_y$ system. Fermi level of 3 types of metal (Pt, W-Cu, Ti-Al) are represented (dashed vertical lines).

(Al_2O_3 with one V_O defect) or a Al_{FP}-rich Al_2O_3 (Al_2O_3 with one Al_{FP} defect) or a V_{Al}^{-3}-rich Al_2O_3 (Al_2O_3 with one V_{Al}^{-3} defect) instead of stoichiometric Al_2O_3. V_O in Al_2O_3 can come from

- Al_2O_3 process condition in O-poor atmosphere

- O exchange with TE during forming process requiring 5.3eV (Figure 4.8)

Al_{FP} and V_{Al}^{-3} come almost spontaneously from process (Figure 4.7). As TE is positively polarized during forming, Al_i^{+3} insertion in TE is not allowed. Therefore, V_{Al}^{-3} creation does not seem favorable during forming process. Results are based on the following equation:

$$\Delta H = U_{Al_2O_3:D_0^{+q_0}+D^{+q}} - U_{Al_2O_3:D_0^{+q_0}} + U_{CuTe_2Ge_3:\overline{D}} - U_{CuTe_2Ge_3}$$
$$+ (q - q_0) \cdot (E_{Fermi} + \Delta V + E_{VB}) \tag{4.3}$$

With $D_0^{+q_0}$, the defect initially present in defective Al_2O_3 due to process or forming (for example: Al_{FP}, V_O or V_{Al}^{-3}), D the studied defect (Cu_i, Te_i...) and $\overline{D}$ its complementary defect in TE (V_{Cu}, V_{Te}...).

The most favorable exchanges are highlighted in Table 4.2. Only defects that can lead to a conductive path through alumina are taken into account. Defects are then considered when they introduce energy level in alumina band gap. Cu introduction is favorable in interstitial site or replacing an Al site. If Al_2O_3 is V_O rich, O substitution is the most favorable. In the case of Al_{FP}-rich and V_{Al}^{-3}-rich, Al substitution is the most favorable. We can note that there is no favorable state found for a Tellurium insertion and that Ge insertion is very expensive compare to Cu.

Table 4.2: Exchange energy ΔH (eV) between TE and γ-Al$_2$O$_3$. Al$_2$O$_3$ is either stoichiometric or includes oxygen vacancies or aluminum Frenkel pairs or aluminum vacancies

Defect D	ΔH Al$_2$O$_3$ (eV)	ΔH Al$_{FP}$-rich (eV)	ΔH V$_O$-rich (eV)	ΔH V$_{Al}^{-3}$ -rich (eV)
Cu$_i^{+1}$	2.5	2	3[1]	x
(Cu$_{Al}$ + Al$_i$)$^{+1}$	1.1[2]	0.6[3]	3.2	x
Cu$_{Al}^{-2}$	5.6	x	x	3.2
Cu$_O^{+1}$	5.8	8	0.6[4]	x
V$_O$	5.3	x	x	x
V$_{Al}^{-3}$	2.8	x	x	x
Al$_{FP}$	0.7	x	x	x
Te$_i^{-2}$	10	8.5	7	x
Te$_{Al}^{-3}$	7.4	x	x	7.3
Ge$_O^{+2}$	9.6	x	3.3	x

[1] Cu interstitial defect next to V$_O$ already present in Al$_2$O$_3$ with V$_O$
[2] Al$_{FP}$ is created and Cu substitute Al site
[3] Cu substitute Al site already present in Al$_2$O$_3$ with Al$_{FP}$
[4] Cu substitute O site already present in Al$_2$O$_3$ with V$_O$

To summarize these results: the most favorable defect in a V_O-rich Al$_2$O$_3$ structure is Cu by O substitution. In the case of Al_{FP}-rich and V_{Al}^{-3} – rich, Cu by Al substitution is the most favorable. Tellurium and Germanium insertions are very expensive compare to Cu.

4.4.3 Amorphous comparison

To complete these results, same calculations are performed in amorphous-Al$_2$O$_3$ (see structure in Figure 4.6). Up to 4 positions are tested for each defect. Table 4.3 reports the most favorable ones. Trends are similar to $\gamma - Al_2O_3$: Cu$_i$ is the most favorable defect that can be inserted in stoichiometric Al$_2$O$_3$ and a V$_O$-rich structure decreases Cu energy insertion. However, it can be noted that tested positions for Cu$_{Al}$ + Al$_i$ are more expensive than Cu$_i$. This may be improved by searching new positions. It can be noted that it may be due to crystalline structure specificity. The rest of the calculations will be done with crystalline structure only, to optimize calculation time. Results on Cu$_{Al}$ + Al$_i$ will need to be cautious.

To summarize these results: the most favorable defect in a-Al$_2$O$_3$ is Cu$_i$ and Cu by O substitution in a V_O-rich structure. These amorphous results are similar to crystalline structure. However, Cu$_{Al}$ + Al$_i$ need to be cautiously treated; it appears more expensive than Cu$_i$ in the amorphous

Table 4.3: Formation energies (ΔH) in stoichiometric or V_O-rich a-Al_2O_3 calculated in GGA considering exchanges with a Cu_2Te_3Ge Top Electrode

Defect	ΔH Al_2O_3 (eV)	ΔH V_O-rich-Al_2O_3 (eV)
Cu_i^{+1}	2.1	2.4
$Cu_{Al}+Al_i^{+1}$	2.6	
Cu_O^{+1}	6	1.65
Cu_{Al}^{-2}	5	
V_O 3-fold	5.1	
V_{Al}^{-3}	3.1	
Ge_i^{+2}	3.2	
Te_i^{-2}	4.0	

structure.

4.4.4 Diffusion in Al_2O_3

Cu and Te diffusions

While thermodynamic approach only considers initial and final defect energy states, more insights are required to quantify the energetic barrier to diffuse Cu ion in Al_2O_3. For this purpose, energy migration barriers are calculated using NEB-based (Nudged Elastic Band) approaches. Results correspond to migrations from Cu_{i1} site to Cu_{i2} (see Figure 4.6). It can be noted that in this work, defect formation energy barrier are not considered. This would require an interface model between Al_2O_3 and $CuTe_xGe_y$ with charge injection effect [19] which is well beyond the scope of this study. However we are in the case of non reversible dielectric breakdown during forming with a high local electric field. This particular event is happening at non equilibrium. Therefore, we expect the first limiting event to be the sensibility of species to the electric field. With high diffusion barrier, it is indeed impossible to move in resistive layer. In the case of Ag/GeS_2 CBRAM behavior with very low migration barrier and low local electric field this defect formation energy barrier could be the first limiting event and would need to be calculated.

Cu_i^+ diffusion barrier in Al_2O_3 structure is found close to 4eV (Figure 4.9a). Cu migration barriers in defective alumina structures are calculated as well with a V_O or Al_{FP} next to Cu migration path. In particular, Cu_i^+ diffusion barriers in Al_2O_3-V_O and in Al_2O_3-Al_{FP} are evaluated at 1.4eV and 0.7eV

respectively. Cu can pass through Cu_O or $Cu_{Al} - Al_i$ state. Consequently, oxygen vacancies and aluminum vacancies in Al_2O_3 would be very likely to facilitate Cu diffusion. It can be noted that Te_i^{-2} migration in Al_{FP}-rich Al_2O_3 is evaluated at more than 7eV (not shown) while Te_{Al}^{-3} migration in V_{Al}^{-3} -rich is evaluated at 3.1eV (Figure 4.9b).
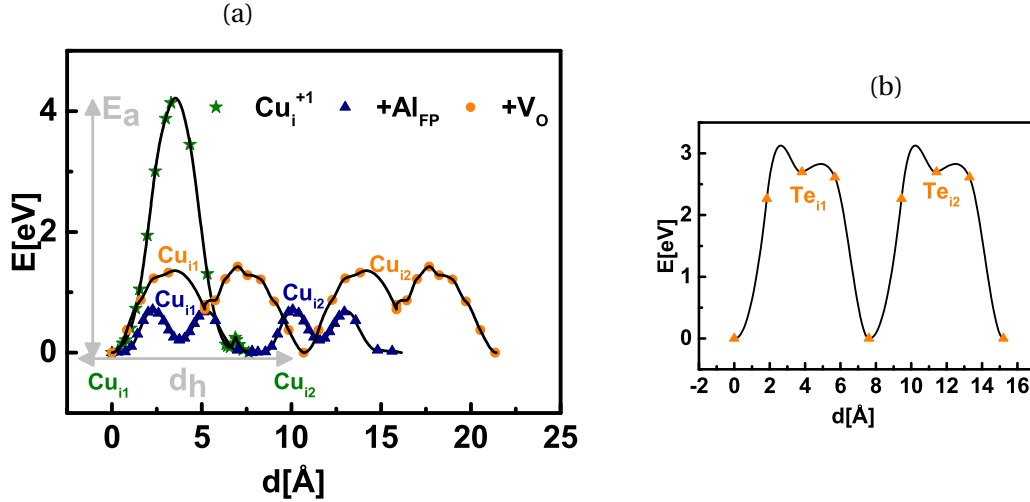
Figure 4.9: First principle calculations to compute barrier height to diffuse from Cu_{i1} to Cu_{i2} sites (see Figure 4.6) a) Cu_i^{+1} in stoichiometric or defective Al_2O_3 systems and b) Te_i in V_{Al}^{-3} -rich Al_2O_3

To summarize these results: Te diffusion in V_{Al}^{-3} is evaluated at 3.1eV while Cu_i^{+1} diffusion is the most favorable next to V_O or Al_{FP} with a migration barrier of 1.4eV and 0.7eV respectively.

O and Al diffusions

In order to find out if oxygen or aluminum can be favorable in Al_2O_3 to help Cu diffusion, O_i^{2-}, V_O, Al_i^{3+} and V_{Al}^{3-} migration barriers are evaluated. Results are shown in Figure 4.10 with associated path screen shots. It reveals that oxygen interstitial and aluminum vacancy have the lowest barriers. Indeed, we find oxygen vacancy diffusion barrier at 3.4eV and 4.7eV for threefold and fourfold coordinated oxygen respectively. This really high value indicates that V_O is immobile. Aluminum interstitial charged +3 is quite hard to diffuse directly from one site to another (>5.5eV not shown). A more favorable path is found by concerted movement and barrier is evaluated around 2.3eV. Meanwhile, oxygen interstitial and aluminum vacancy have their highest barrier around 0.54eV and 1.5eV respectively (by concerted movement).
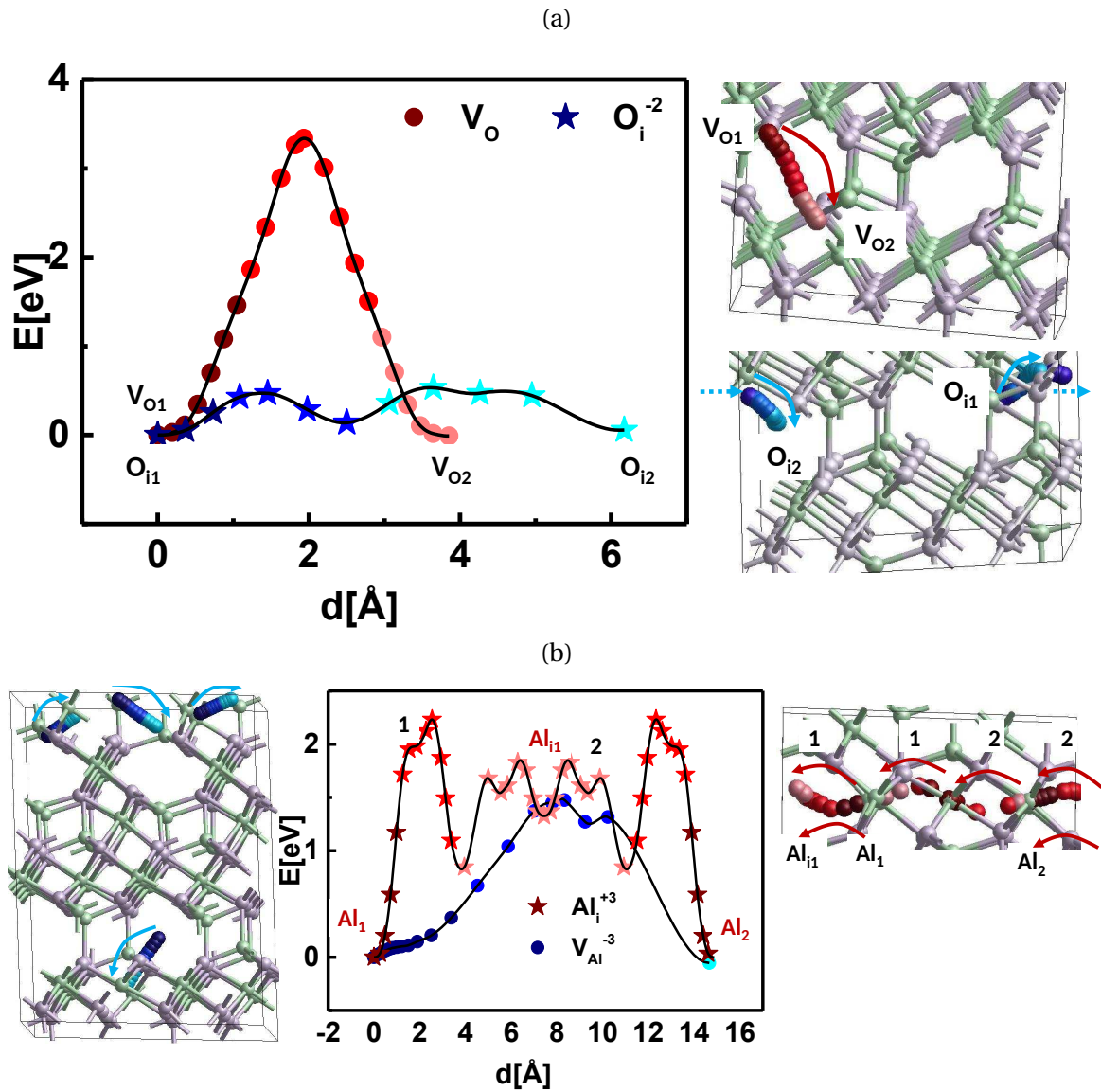
Figure 4.10: Migration barrier in Al_2O_3 with associated path screen shots of a) V_O in red and O_i^{-2} in blue by concerted movement, b) Al_i^{+3} in red by concerted movements and V_{Al}^{-3} in blue

To summarize these results: V_O and Al_i^{+3} **are hardly mobile in** Al_2O_3 **whereas** O_i^{-2} **and** V_{Al}^{-3} **have the lowest energy migration barriers at 0.54eV and 1.5eV respectively.**

4.5 Al_2O_3 **filament formation**

Starting with thermodynamic calculations (Table 4.2), Al_2O_3 after deposition process may be rich in aluminum Frenkel pair and aluminum vacancies charged -3. Then, when Al_2O_3 is in contact with $CuTe_xGe_y$, two types of defects appear favorable in the oxide: Cu_O in V_O-rich structure and Cu_{Al} in Al_{FP}-rich structure (<1.1eV). These first results show that filament formation is complex and can not be explained with a simple Cu insertion. At first, one can question the composition of the filament: Cu or Te? In literature, Te hypothesis is not discarded [20]. Then, disorder must be induced in Al_2O_3 to allow one of the metallic ions to form the filament (Cu_i in stoichiometric Al_2O_3 costs 2.5eV vs 0.6eV in V_O-rich structure). This disorder has to be discussed taking into account Al and O point defects. And finally the origin of this disorder has to be clarified.

The following discussion discards the possibility of Te filament. Indeed, comparison of pure Cu TE and $CuTe_xGe_y$ TE showed similar forming voltage at first order in both polarizations (Figure 4.2). Moreover, in the most favorable case, Te insertion has a high formation energy in Al_2O_3 (7.3eV). Finally, Te diffusion barrier was evaluated in DFT (Figure 4.9) at 3eV for the lowest case. These simulations confirm that **Te is hardly mobile in** Al_2O_3 **and is considered to have no impact on the created filaments.**

Based on this result, polarization effect on filament formation is analyzed by two types of forming. In direct forming (F), TE is positively polarized ($V_{TE} > 0$) while in reverse forming ($\overline{F}$), TE is negatively polarized ($V_{TE} < 0$). Depending on this polarization, different electrical responses were observed in terms of forming voltage, cycling and stability in temperature. First, $\overline{V_f}$ is always higher than V_f. After $\overline{F}$, higher voltages are needed to operate the cell and resistances stability is degraded at 200°C after 20min for R_{off} and 24h for R_{on}. These results prove that **polarization impacts the filament created.**

Investigating in DFT the most stable charge state of the defects in a Al_2O_3 / $CuTe_xGe_y$ system (orange vertical line in Figure 4.8), we can observe that

Cu_i is singly charged +1. This could give a first explanation: **Cu would be introduced in the oxide in direct forming only.** On the other hand, since both forming occur at a voltage close to breakdown electric field, we may consider that V_O are created during both operations. **Reverse forming would then imply only oxygen vacancy movements.**

Based on these assumptions, the significant differences between V_f and $\overline{V_f}$ push towards the following hypothesis:

- TE oxidation is harder than W, Ta or TiN which can be seen Figure 4.11.

- Inserting copper in oxide is easier than creating only oxygen vacancies.
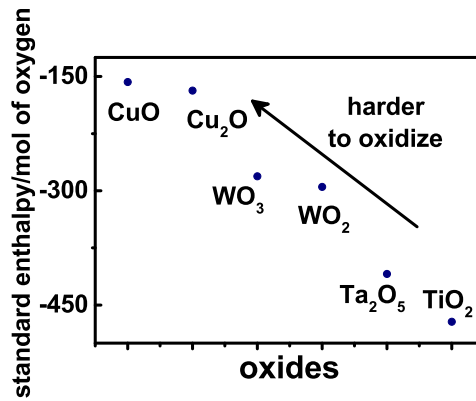
Figure 4.11: Formation enthalpy for different oxides

The first hypothesis is not discarded, but does not give satisfying justification regarding filament differences. Meanwhile, the second hypothesis need more investigation about a possible Cu introduction. We can either consider a filament only composed of copper or a copper insertion helped by oxygen vacancies created during this step (see Figure 4.12). In the latter case, filament would be composed of copper and oxygen vacancies. In Al_2O_3 PVD sample, oxygen vacancies can also be inherently present in the layer, resulting from structural defects that decrease V_f and sustain this idea (see Figure 4.2).

To support a hybrid Cu/V_O filament composition, Cu energy migration barriers in Al_2O_3 were calculated. **The elevated Cu_i migration barrier of 4eV confirms that another mechanism must be involved during forming to facilitate Cu filament creation.** All other attempts implying $Cu_{Al} - Al_i^{+1}$ states led to a barrier >5eV. However, **copper easily diffuses when V_O and Al_{FP} are present (1.4eV and 0.7eV respectively).** In order to check if O and
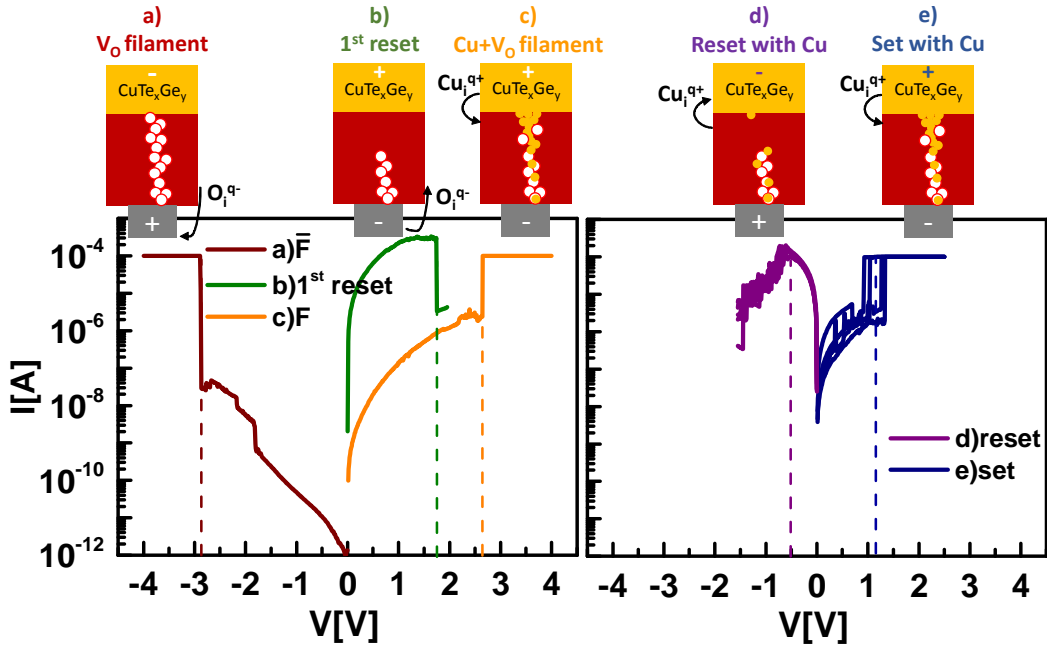
Figure 4.12: I(V) curve and interpretation of a W/Al$_2$O$_3$(3.5nm ALD)/CuTe$_x$Ge$_y$ cell being formed by a) reverse forming and then b) 1st reset and c) formed again positively before d) and e) standard cycling

Al$_{FP}$ related point defects could help Cu insertion, their migrations were evaluated.

First, V$_O$ will certainly stay immobile with a 3.7eV barrier. On the contrary, O$_i$ (barrier at 0.54eV) and V$_{Al}$ (barrier at 1.5eV) may diffuse. However, it can be noted that 1.5eV could be high enough not to be feasible at quantitative level. These results support oxygen interstitial migration whereas V$_O$ stay immobile and help Cu diffusion. Moreover, if there are some aluminum vacancies in resistive layer, they can accumulate near top electrode and help Cu introduction in the oxide. **This leads to a filament rich in Cu in a zone depleted of aluminum and poor in oxygen.** Finally, since Al$_i^{+3}$ are not very mobile (>2.3eV), there is little chance that they have a strong influence on the conductive filament.

Coming back to electrical characterization results, R$_{off}$ and R$_{on}$ instability in temperature after $\overline{F}$ demonstrates that in reverse forming, filament is easier to rebuild or disrupt. This phenomenon can either be due to a lower migration barrier, or a higher defect concentration in the oxide leading to an easy filament reconstruction. In J. Guy *et al.* [21], it was demonstrated that more defects in resistive layer leads to higher instability of the high resistive states. Indeed, Cu migration is facilitated through defects present in the oxide matrix. In our case, resistance instability can be explained by

this phenomenon meaning defect generation in the oxide is higher after reverse forming, degrading the retention characteristics. **In the case of direct forming, a lower defect generation is sufficient to make Cu insertion possible in resistive layer and create a conductive path.**

To conclude, Table 4.4 summarizes energy costs to introduce various species in alumina. Based on these results, a new filament model is proposed (see Figure 4.13). In the case of a reverse forming ($\overline{\text{F}}$) oxygen diffuse towards BE, while aluminum vacancies accumulate near it. When a positive voltage is applied to the TE, copper is inserted in the oxide while oxygen is going in the TE and aluminum vacancies accumulate near it. As we have seen previously, SET voltage is much smaller than forming voltage. Moreover, due to the fact that V_O are immobile in Al_2O_3, SET process may mostly imply Cu migration in a V_O-rich structure: a hybrid Cu/V_O filament is proposed.

Table 4.4: Summary of DFT calculations, indicating enthalpy formation energy ΔH, migration energy barrier height E_d and hopping distance d_h.

Defect	ΔH(eV)	E_d(eV)	d_h($\dot{\text{A}}$)
Cu_i^{+1}	2.5	4	6
V_O	3.8	3.5	4
V_{Al}^{-3}	3.1	1.5	15
Al_i^{+3}	-0.7	> 2.3	> 8
O_i^{-2}	0.25	0.54	6
Cu_i^{+1} in V_O	0.6	1.4	10
Cu_i^{+1} in Al_{FP}	1.1	0.7	4
Cu_{Al}^{+1} in V_{Al}^{-3}	3.2	x	x
Te_i^0 in V_{Al}^{-3}	7.3	3.1	8
Te_i^{-2} in Al_{FP}	8.5	7	10
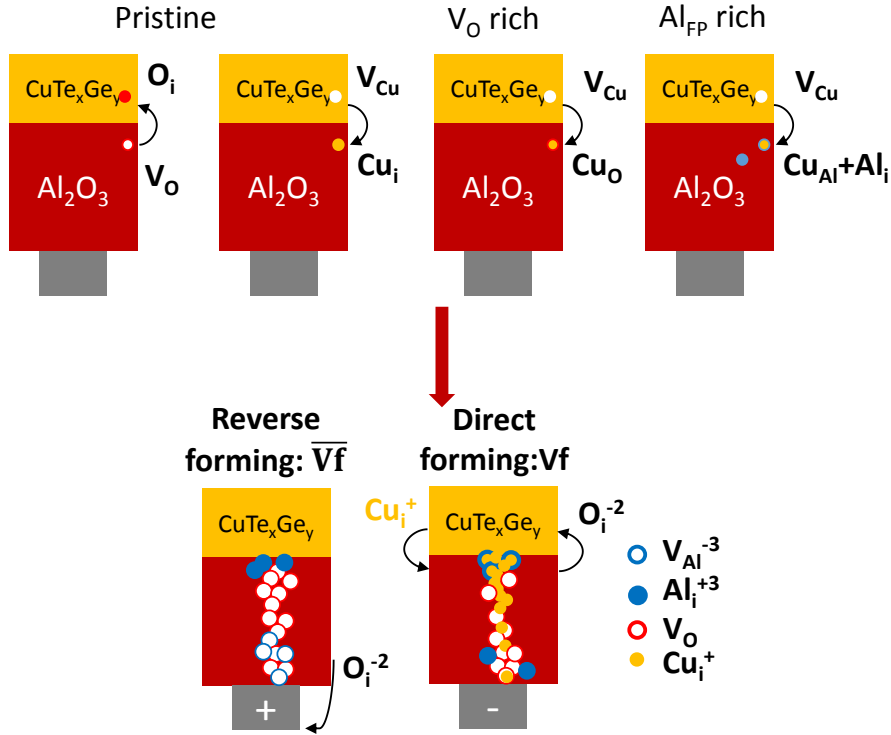
Figure 4.13: Illustration of the most energetically favorable exchanges between Al_2O_3 and $CuTe_xGe_y$ during forming and schematic movements happening during forming

4.6 Chapter IV synthesis

In this chapter, we investigated conductive filament composition in Al_2O_3 / $CuTe_x$ based CBRAM. Electrical characterization are used to study the polarization effect on filament formation. These results are combined with atomistic simulation to have more insights at the microscopic level. A defect systematic review in Al_2O_3 with charged states is realized to see which defect are the most favorable from a thermodynamic point of view. Nudged Elastic Band calculations compute defects migration barriers to evaluate which defect can diffuse in Al_2O_3 and could participate to filament formation. Similar trends for Cu/V_O insertion were found between amorphous and crystalline Al_2O_3 in terms of point defects enthalpies so the rest fo the study was done with crystalline structures only. Te ion were revealed hardly mobile and Ge ion more expensive than Cu ion and their impact on the filament formation and composition was discarded. Cu insertion in Al_2O_3 appeared energetically unfavorable. However with O and Al related disorder, energy cost decreases (4eV to 1.4eV/0.7eV respectively). Thus, during forming operation, a certain amount of V_O is created to allow Cu insertion in Al_2O_3, leading to a hybrid Cu/V_O filament. Aluminum vacancies were revealed potentially mobile while oxygen vacancies stay on

site (3.7eV migration barrier for V_O). Thus, only Cu motion is assumed to be dominant during SET and RESET process in a V_O rich structure while V_{Al} can help Cu movement near top electrode during forming and SET.

After investigating on Al_2O_3 / $CuTe_x$ based CBRAM, this kind of study can be extended to other RRAM. Combining electrical characterization and simulation allow a better microscopic understanding and bring insight from a material point of view. The next chapter deals with the interdependence between RRAM electrical performances as well as material parameters. Using these tools to compare several RRAM point out new parameters that can be taken into account to target specific applications.

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Chapter 5

RRAM performances trade-off

5.1 Introduction/Objectives

Following the understanding of filament properties, this chapter focuses on material stack comparision to highlight a link between RRAM performances and microscopic features. We first study three memory characteristics on different RRAM technologies such as endurance, window margin and retention (see chapter II) and expose their interdependence. Focusing on one technology, programming conditions such as current, voltage and time need to be optimized and a trade-off between endurance and window margin is established. Comparison between memory stack is then realized, highlighting a correlation between endurance plus window marging improvement and retention degradation. Studying this last feature from a material point of view, we compare different oxides by Density Functional Theory (DFT) with thermodynamic and diffusion methods (see chapter III). This provides insights on conductive filament composition in different stacks. Combining previous experiments and simulations, a link between memory characteristics and material microscopic parameters is established, through the ion energy migration barrier. A correlation between RRAM performances, material properties and electrical parameters is exposed and is used to choose the suitable material for a defined application using RRAM technology.

5.2 State of the art of RRAM performances

As RRAM industrial benchmark is not yet well defined (see chapter I), literature on their performances is collected. Recently, good characteristics were reported, making RRAM potential candidates to replace Flash for both stand alone, storage class applications [1] and embedded products [2, 3]. Endurance over 10^8 cycles is targetted for storage class com-

pare to 10^5-10^6 cycles for stand alone applications [4] while for automotive applications temperature stability over 175°C is required [5]. For example, in C.Y. Chen *et al.* [6] endurance up to 10^{12} cycles was reported with TiN/GdO/Hf/TiN stack with a retention below 150°C, promising for storage class memory applications. Excellent stability was demonstrated in M. Barci *et al.* [7] where a retention up to 350°C with an endurance up to 10^3 cycles was shown. However, it is very challenging to combine all features such as having good cycling, stable retention at high temperature as well as high enough window margin depending on the targeted density. Indeed, intrinsic RRAM variability is a challenge to avoid WM closure [8]. In S. Sills *et al.* [1] a 10Mb array integration is demonstrated with a median memory window of 3 orders of read current which leads to an overlap at the –4.6σ level (> 99.9% of the devices). Figure 5.1 shows memory performances data based on experimental results reported in literature. It illustrates a general trend where high window margin corresponds to low endurance. Meanwhile, there are some outliers showing more promising characteristics combining high WM and endurance (blue references). However, these technologies exhibit lower temperature stability for 24h retention. In order to gather a maximum of data, temperature stability criterion is taken as the maximum demonstrated temperature with no resistance variation during 24h. Following this observation, the interrelationship between these three memory features requires more investigation.
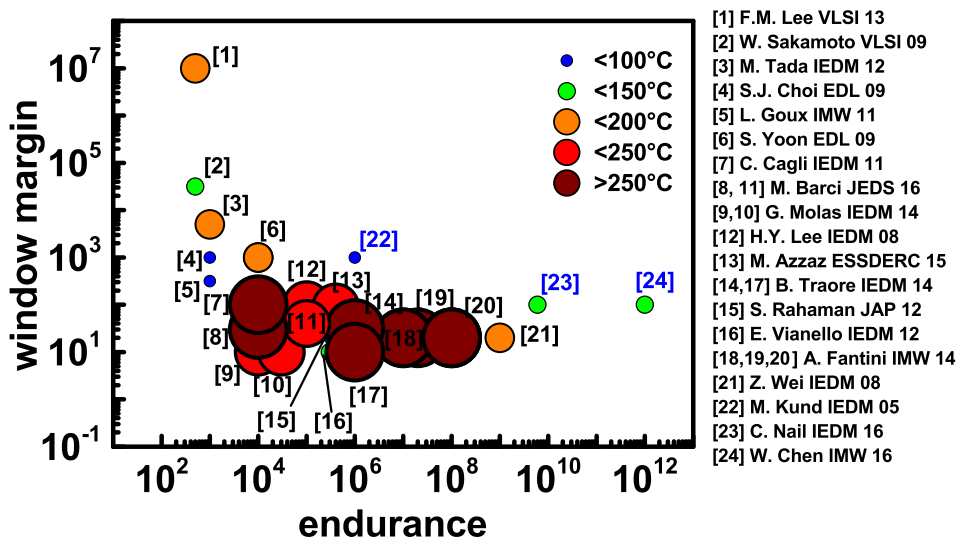
Figure 5.1: Window margin (mean value) as a function of RRAM maximum achieved cycles reported in literature depending on maximum temperature stability for retention after 24h.

5.3 Optimizing programming conditions

Our measurements are done on different RRAM samples with a BE / Oxide / $CuTe_xGe_y$ structure (see Figure 5.2). The memory is integrated in 1T1R configurations using a CMOS transistor as selector. 3nm to 3.5nm of amorphous a-Al_2O_3 [9] or 5nm of amorphous a-HfO_2 [10] or 4nm of GdO_x [11] was deposited by PVD or ALD on different PVD bottom electrode (TiN, W). 20nm of $CuTe_xGe_y$ deposited by PVD was used as top electrode (TE). Figure 5.2 shows TEM cross section of W/HfO_2/$CuTe_x$ RRAM developed in this work using a plug structure.

Figure 5.2: Schematic of the RRAM technologies studied in this work with TEM cross sections of W/HfO_2/$CuTe_x$ based CBRAM, and EDX (Hf, W, Cu) images.

In order to study our RRAM, we first optimize programming conditions and observe their impact on memory characteristics. Focusing on TiN / Al_2O_3 / $CuTe_x$ samples, Figure 5.3a shows SET programming current depending on window margin. Increasing the SET current to 100µA improves the window margin. Above that, WM is degraded due to high electric stress applied to the dielectric, reducing the OFF state resistance after RESET operation. Figure 5.3b shows pulse length for SET and RESET impact. Decreasing pulse lenght reduces WM, but increases speed and decreases consumption. A typical endurance can be seen in Figure 5.3c at 100µA with its associated resistance distribution in Figure 5.3d.
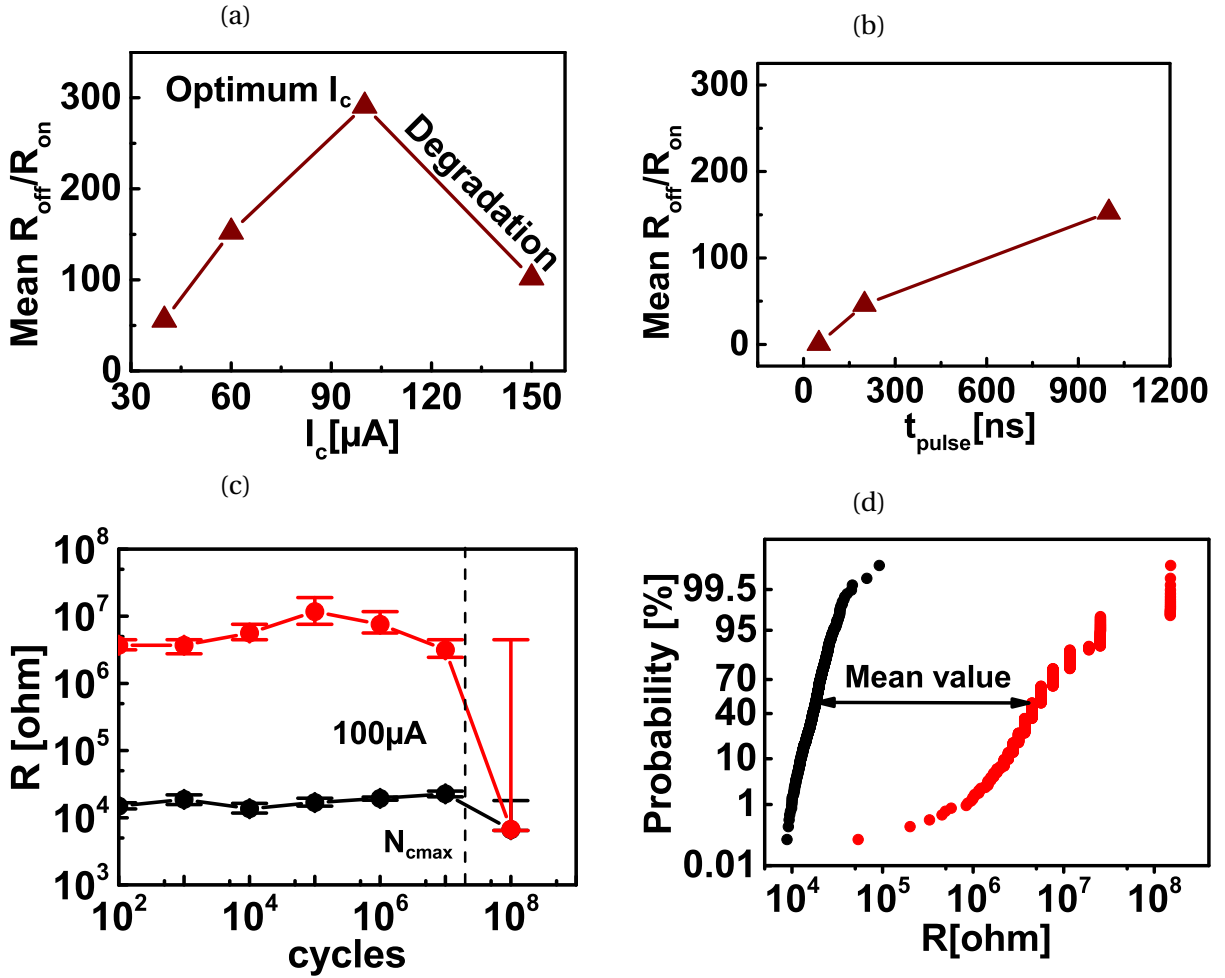
Figure 5.3: (a) Summary of WM behavior depending on SET current I_c and programming time t_{prog}. Low I_c offers low window margin while high I_c (150µA) degrades R_{OFF} b) Long t_{prog} improves the window margin at the expense of lower speed and degraded consumption c) and d) Endurance characteristics of TiN / Al_2O_3 / $CuTe_x$ RRAM at 100µA with cycle to cycle Resistance distribution ($t_{SET}=t_{RESET}=1$µs). Error bars correspond to standard deviation measured on 100 subsequent cycles.

5.4 Endurance vs Window Margin Trade-off

In order to study the trade-off between WM and endurance, we extract the maximum number of cycles a cell can reach for different RESET voltages (V_{RESET}), giving different WM, setting time pulse at 1µs. The maximum number of cycles (N_{cmax}) is achieved when RESET operation becomes impossible, meaning oxide layer was led to an irreversible breakdown (see Figure 5.3c), leading to window margin closure. Figure 5.4b and Figure 5.4c show V_{RESET} influence on R_{OFF} and endurance respectively. Figure 5.4a shows typical curves to extract these data. R_{OFF} increases with V_{RESET} until a threshold value is reached where WM is then degraded. WM degradation after 2V can be explained by a negative SET following the RESET due to defect injection from the BE [12]. On the other hand, the maximum number

of cycles decreases as V_{RESET} increases. Results reveal a trade-off between WM and endurance: staying out of an early degradation with V_{RESET} below a threshold value, improving WM leads to a degraded endurance.
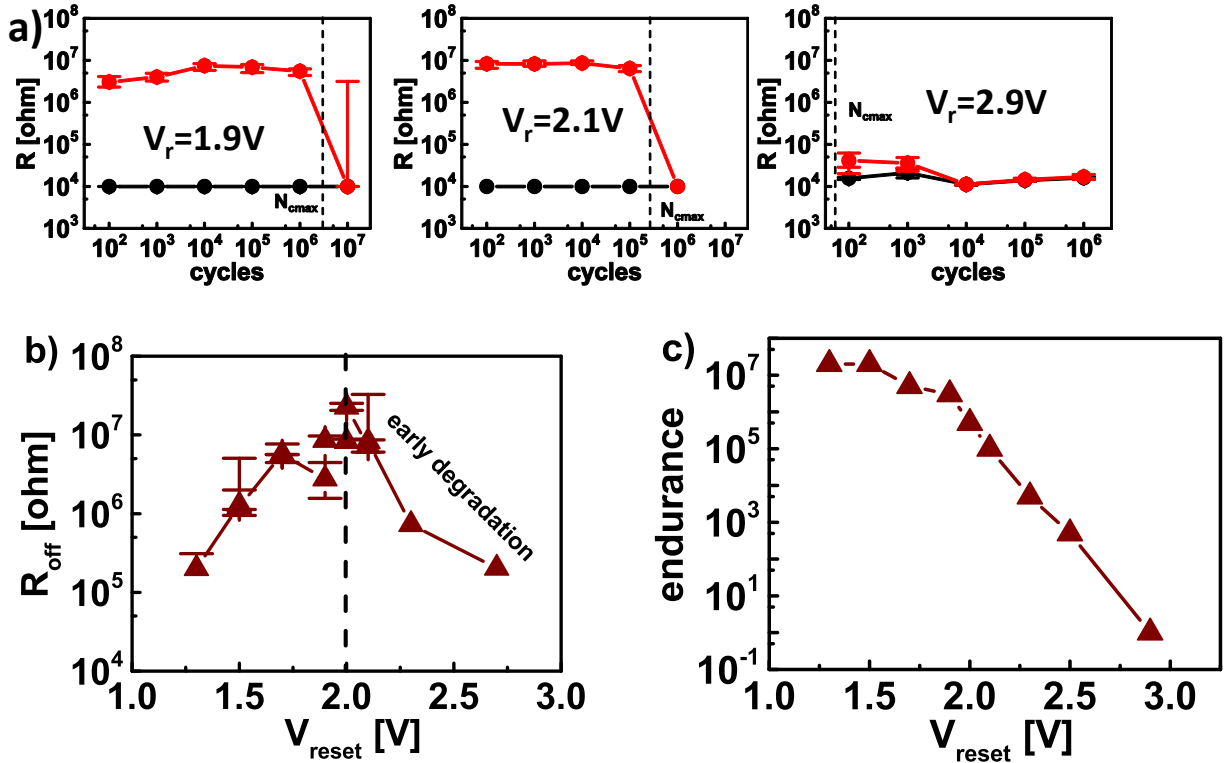
Figure 5.4: a) Typical endurance curves with different V_{RESET} to extract b) and c). Impact of V_{RESET} on $TiN/Al_2O_3/CuTe_x$ sample on b) R_{OFF}, error bars corresponds to standard deviation on 10 cells and c) endurance (maximum number of achieved cycles).

5.5 Endurance plus Window Margin improvement vs retention Trade-off

In order to compare different materials, this study is extended to 4 RRAM technologies. We chose to fix the programming current to 100µA, which is close to the optimum programming current insuring large WM and high number of cycles. Taking the RESET parameter giving the best endurance for each technology, we compared their endurance (N_{cmax}) and their best retention (highest stability temperature $T°_{max}$ for 24h baking time). Results are shown in Figure 5.5 for three of them. $W/HfO_2/CuTe_x$ shows up to 6.10^9 cycles with a constant WM while its maximum temperature stability is around 100°C. $TiN / Al_2O_3 / CuTe_x$ shows an endurance up to 10^7 and a temperature stability up to 200°C while $TiN/GdO_x/CuTe_x$ shows an endurance up to 3.10^3 and a stable retention up to 300°C. These three RRAM are a good example to illustrate the trade-off between endurance and re-

tention: good cycling goes with poor retention (W/HfO$_2$/CuTe$_x$ technology), while stable retention is reached at the cost of limited endurance (TiN/GdO$_x$/CuTe$_x$ technology). Figure 6.1a represents reached endurance for each RRAM technology for different RESET Voltage conditions, implying different WM. Focusing on one material, WM can be increased at the expense of degraded endurance. Having compared different materials (for a given WM), it can be concluded that endurance is improved as retention is degraded (Figure 6.1b). Through these results, trade-off between endurance, WM and retention is revealed.
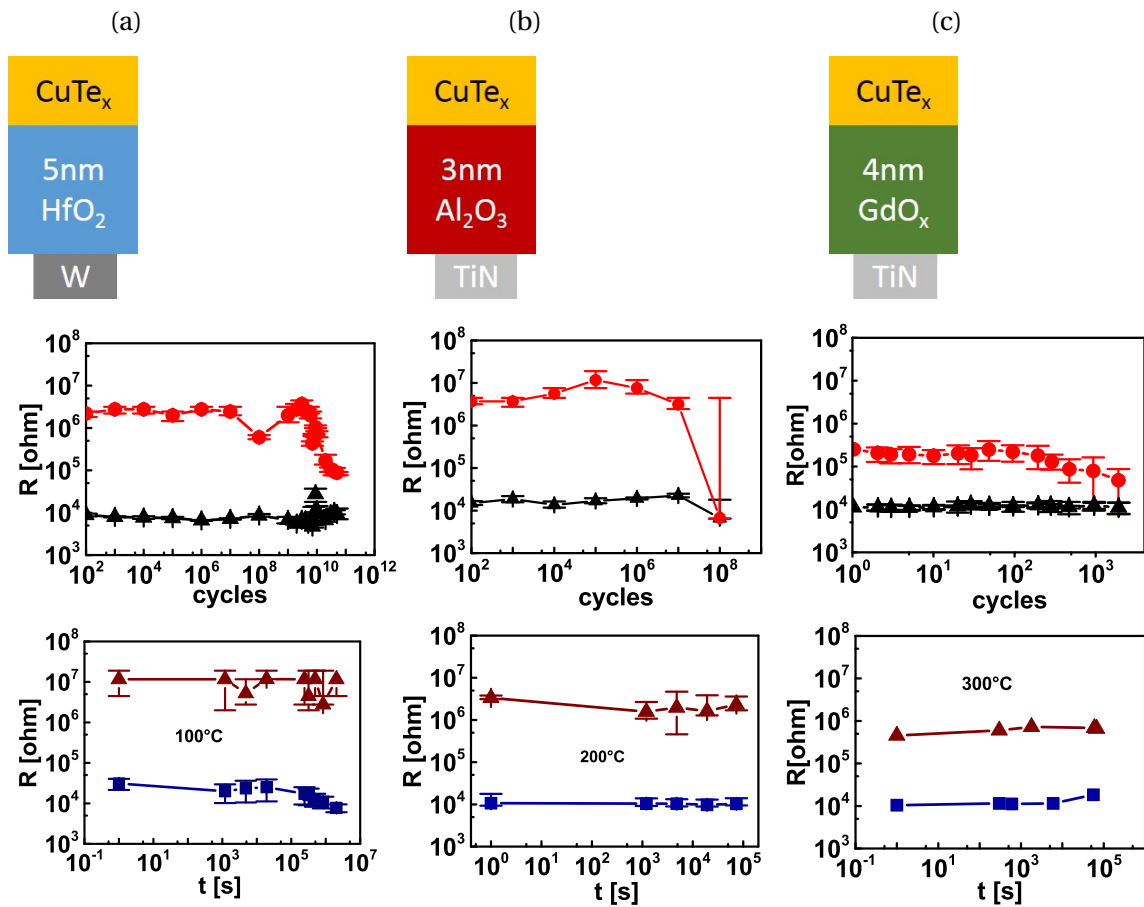
Figure 5.5: Endurance and retention performances for a) W/HfO$_2$/CuTe$_x$, b) TiN/Al$_2$O$_3$/CuTe$_x$ and c) TiN/GdO$_x$/CuTe$_x$ memory technologies.

(a)

(b)
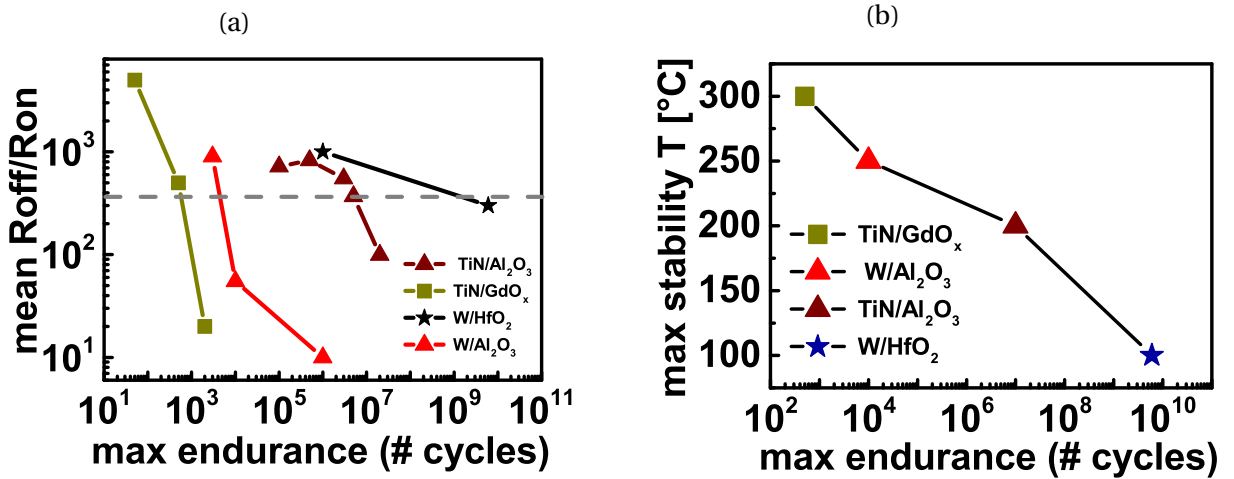
Figure 5.6: a) Window Margin as function of maximum endurance. For each RRAM technology, various WM were achieved changing the RESET conditions. Gray line is used to extract b) for a constant WM. b) Maximum stable retention temperature after 24h baking time as function of maximum endurance for a given WM (R_{OFF}/R_{ON} ~400).

5.6 RRAM Filament properties

To go further, endurance, WM, retention trade-off is studied from a material point of view. Atomistic simulations are performed to study the different oxides. In this section, the objective is to analyze the filament composition of the various investigated memory stacks, and to extract the microscopic material properties, in particular the energy required to diffuse ions during filament formation. To avoid redundancy, we will only present the detailed calculations for HfO_2/Cu RRAM.

5.6.1 Simulation framework

For hafnia, a 96-atoms supercell consisting of eight monoclinic-HfO_2 unit cells was calculated. This structure is the closest crystalline form of our amorphous PVD material with a density of $9.8g.cm^{-3}$ vs the measurement value of $10g.cm^{-3}$. Different positions were tested for each defect, especially for interstitials, up to 4 inequivalent sites were compared (see Figure 5.7). Detailed calculation parameters can be found in Annexe.

The band gap obtained at 3.73eV is corrected [13] in G0W0 at 5.2eV vs 5.5eV measured by ellipsometry. For the TE we used a 96-atom supercell consisting of eight Cu_2Te_3Ge unit cells [14]. This structure is the closest crystalline form of our amorphous PVD material with a density of 6.0 $g.cm^{-3}$ vs 6.1 $g.cm^{-3}$ (measured). All results are based on a band alignment between the band-gap of hafnia and Cu_2Te_3Ge which was done considering

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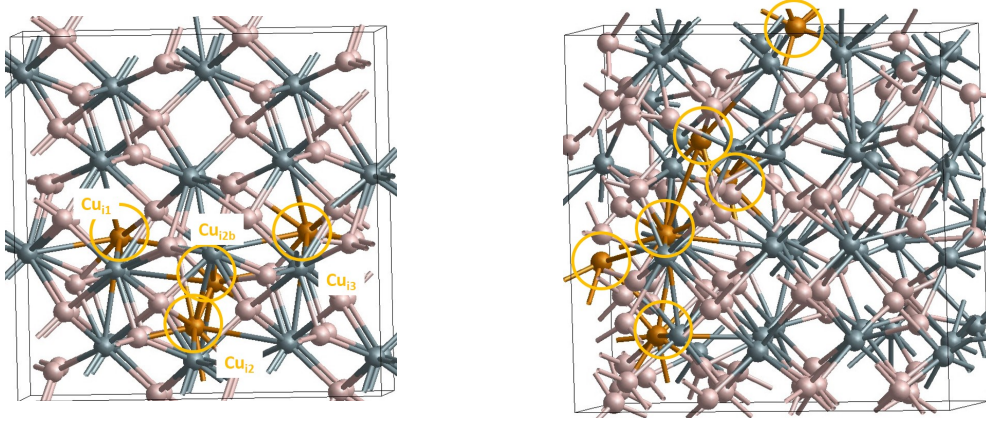
Figure 5.7: HfO_2 and $a-HfO_2$ structure with different copper interstitial positions. O in red, Hf in blue, Cu in orange. Cu_{i1} and Cu_{i2} are used for migration barrier calculation.

- G0W0 gap correction with an opening of 1eV at the conduction band and -0.5 eV at the valence band.

- Electron affinity of HfO_2 at 2eV [15]

To complete the study, an amorphous a-HfO_2 model with a density of 9.4g.cm^{-3} was implemented. This model was generated using the melt and quench method: a crystalline monoclinic-HfO_2 with Schottky defects was used for the initial structure to lower density with the eight HfO_2 unit cells considered above. It was melted at 2800K for 10ps and cooled to 300K for 10ps with a time step of 1fs. 1 k-point was used during the molecular dynamics while 2*2*2k-points were used for the defect calculations. The band gap is obtained at 3eV free of defect against 3.73eV in the crystalline structure.

5.6.2 HfO_2 **thermodynamic of defects**

We studied HfO_2's point defects in contact with a $CuTe_x$-based TE. As we consider exchanges between HfO_2 and $CuTe_2Ge_3$, calculations are based on the following equation for an interstitial of copper charged +q (Cu_i^{+q}):

$$\Delta H = U_{HfO_2:Cu_i^{+q}} - U_{HfO_2} + U_{CuTe_2Ge_3:V_{Cu}} - U_{CuTe_2Ge_3}$$
$$+ q \cdot (E_{Fermi} + \Delta V + E_{VB}) \tag{5.1}$$

With ΔH the formation enthalpy of the defect, U_{Defect} the total energy of the defect, $U_{Pristine}$ the total energy of the initial state, n_i and μ_i the number of chemical formula and the reference chemical potential for the exchange, q the charges exchanged in the system, E_{Fermi} the Fermi level of the electrode in considered contact, ΔV the electrostatic energy shift[16]

and E_{VB} the highest valence band energy level. Results are presented in Figure 5.8 and Figure 5.9 with the lowest charged defects. Considering the charge of the species and a top electrode in contact based on Cu (vertical orange line), the most favorable interstitials and vacancies we could obtain are respectively: Copper interstitial (Cu_i^{+1}), Oxygen Vacancy (V_O^{+2}). Tellurium interstitial and hafnium vacancies are not considered here because of their high formation enthalpy energy. As explained in the previous chapter, Ge is used to stabilize CuTe layer and keep it amorphous during integration process, to prevent any segregation and phase separation. Typically, 10-20% Ge is used [17, 18] in CuTe alloys. As a consequence, Ge is not expected to have any impact in the electrical behaviour of CuTe. Moreover, CuTe bound is polar and can easily be broken in $Cu^{\delta+}$ and $Te^{\gamma-}$ ions. They will be mobile under the electric field. Ge calculations are just used to confirm this affirmation. We will thus focus on Cu ions in the next sections.
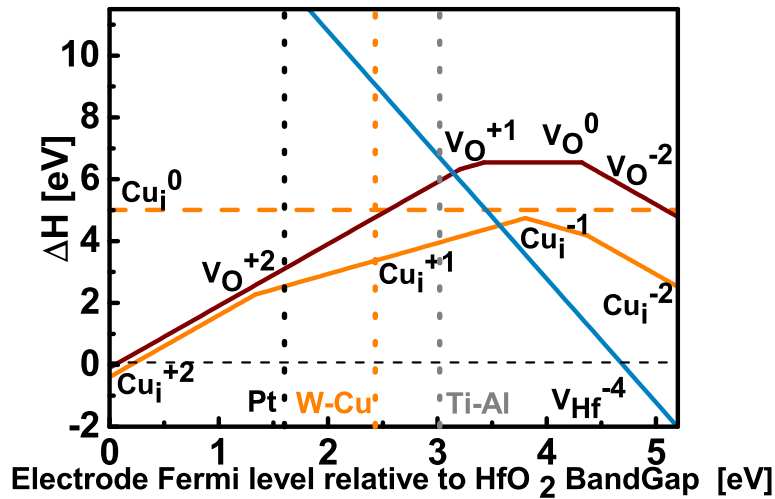
Figure 5.8: Formation enthalpy calculation of defects in $HfO_2/CuTe_xGe_y$ system. Fermi level of 3 types of metal (Pt, W-Cu, Ti-Al) is represented (dashed vertical lines).

Based on these two candidates, we studied the case of copper introduction in defective hafnia. The reference for the oxide becomes then a V_O-rich HfO_2 (HfO_2 with one V_O defect) instead of stoichiometric HfO_2. V_O in HfO_2 can come from

- HfO_2 process condition in O-poor atmosphere

- O exchange with the TE during forming process requiring 4.8eV.

The results are summarized Table 5.1 and based on the following equation:
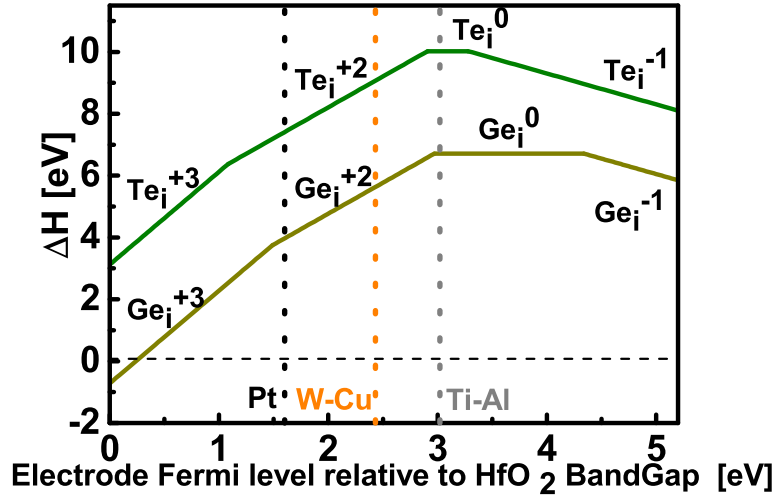
Figure 5.9: Formation enthalpy calculation of defects in $HfO_2/CuTe_xGe_y$ system. Fermi level of 3 types of metal (Pt, W-Cu, Ti-Al) are represented (dashed vertical lines).

$$\Delta H = U_{HfO_2:V_O+Cu_i^{+q}} - U_{HfO_2:V_O} + U_{CuTe_2Ge_3:V_{Cu}}$$
$$- U_{CuTe_2Ge_3} + q \cdot (E_{Fermi} + \Delta V + E_{VB}) \tag{5.2}$$

Table 5.1: Formation enthalpy ΔH (eV) between the TE and HfO_2 either stoichiometric or including oxygen vacancies

Defect	ΔH HfO_2 (eV)	ΔH V_O-rich (eV)
Cu_i^{+1}	3.4	2.6
V_O^{+2}	4.8	x
V_{Hf}^{-4}	9.1	x
O_{FP}	4.5	x
Te_i^{+2}	9.1	x
Ge_i^{+2}	5.6	x

Cu introduction is favorable in interstitial site while if HfO_2 is V_O rich, Cu introduction is the easiest in the interstitial site next to V_O.

To complete these results, same calculations were performed in amorphous-HfO_2 (see structure Figure 5.7). Up to 6 positions were tested for each defect. Table 5.2 reports the most favorable ones. The results are similar to crystalline HfO_2 allowing to pursue the calculation only with this structure to optimize calculation time. It can be noted that formation energies are lower in amorphous structure which show

Table 5.2: Formation enthalpy(ΔH) in a-HfO$_2$ stoichiometric or V$_O$-rich calculated in GGA considering exchanges with a Cu$_2$Te$_3$Ge Top Electrode

Defect	ΔH HfO$_2$ (eV)	ΔH V$_O$-rich-HfO$_2$ (eV)
Cu$_i^{+1}$	1.8	1.4
V$_O^{+2}$	5.9	x

5.6.3 HfO$_2$ **defect diffusion**

The most favorable defects that can be inserted in HfO$_2$ were extracted. However, thermodynamic approach only considers initial and final energy states of the defects. Therefore, this section focuses on Cu diffusion to quantify the energetic barrier height to move it between two equivalent sites. Energy migration barriers are calculated using NEB-based (Nudged Elastic Band) approaches. The presented results correspond to Cu migration from Cu$_{i1}$ site to Cu$_{i2}$ (see Figure 5.7).

The diffusion barrier of Cu$_i^+$ in HfO$_2$ structure was found close to 2.5eV (Figure 5.10). We also calculated Cu migration barriers in defective hafnia structures with a V$_O$ next to the Cu migration path. In particular, the diffusion barriers of Cu$_i^+$ in HfO$_2$-V$_O$ is evaluated at 1.28eV. Cu can pass through a Cu$_O$ state. To complete this result, calculations were performed on the amorphous modele. The diffusion barrier of Cu$_i^+$ in a-HfO$_2$ is found close to 3eV and 2.5eV with Cu$_i^+$ next to V$_O$.
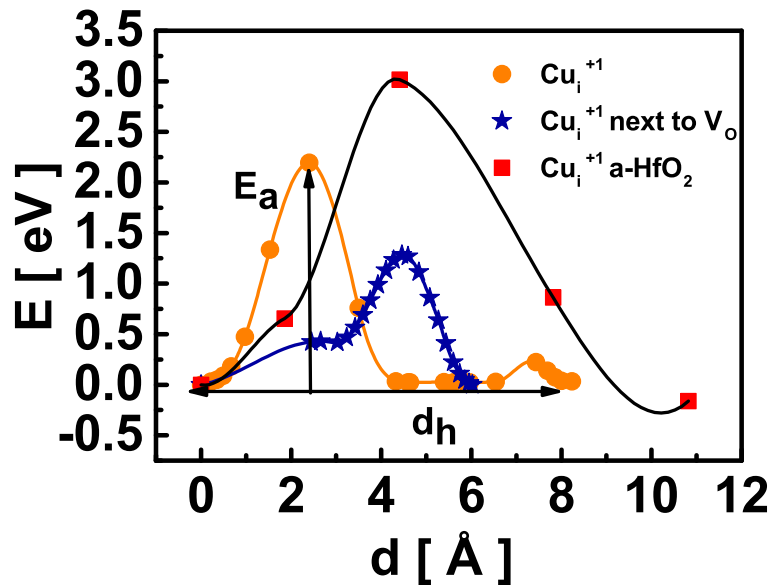
Figure 5.10: First principle calculations to compute the barrier height to diffuse from Cu$_{i1}$ to Cu$_{i2}$ sites (see Figure 5.7): Cu$_i^{+1}$ diffusion barrier in stoichiometric or defective HfO$_2$ systems.

5.6.4   Simulation results summary

This study is done for 3 different materials: Al_2O_3, HfO_2 and Gd_2O_3. Table 6.1 summarizes the main results. If thermodynamic and kinetic energies are taken into account, Al_2O_3 and Gd_2O_3 show $(Cu_iV_O)^{+1}$ defect as the most favorable while HfO_2 shows favorable energies for $(Cu_iV_O)^{+1}$ and V_O^{+2}.

Table 5.3: Migration energy barrier, E_a, and formation enthalpy, ΔH, between the TE and different oxides either stoichiometric or including oxygen vacancies (Cu_iV_O defect).

Defect	ΔH_{HfO_2} (eV)	$E_{a\ HfO_2}$ (eV)	$\Delta H_{Al_2O_3}$ (eV)	$E_{a\ Al_2O_3}$ (eV)	ΔH_{GdO_x} (eV)	$E_{a\ GdO_x}$ (eV)
Cu_i^{+1}	3.4	2.5	2.5	4	3.5	2
V_O^x	2.5 (+2)	0.7 (+2)	3.8 (0)	3.5 (0)	4.1 (0)	x
$(Cu_iV_O)^{+1}$	2.6	1.3	0.6	1.4	1.2	3.44
Filament	Hybrid: Cu_i and V_O moving		Cu_i next to V_O		Cu_i next to V_O	

5.7   A link between RRAM performances and material microscopic properties

5.7.1   Migration energy barrier correlated to RRAM performances

Combining electrical characterization and DFT results, we can put in evidence a clear correlation between memory characteristics and the ion migration barrier. Figure 5.11 represents memory endurance and retention temperature as a function of calculated $E_{migration}$. The number of cycles reachable by a cell decreases with $E_{migration}$ (Figure 5.11a) while temperature stability increases (Figure 5.11b). This phenomenon can be understood with a simple description of ion migration in the resistive layer. Figure 5.11 illustrates how endurance is facilitated by a low migration barrier; a low energy will lead to an easy formation and disruption of the filament. A high migration energy barrier will lead to stable retention; making the filament more difficult to be dissolved. In HfO_2, as Cu_iV_O and V_O calculated migration energies are of the same order of magnitude (see Table 6.1), we considered a hybrid filament resulting from both Cu and V_O diffusion. Thus, $E_{migration}$ is calculated as the average value between Cu_iV_O and V_O in Figure 5.11. In conclusions, it clearly appears that the ion migration energy is linked to the trade-off between memory endurance and retention. It can be noted that there is no clear correlation found with the formation enthalpy energies (see Figures 5.12a and 5.12b).
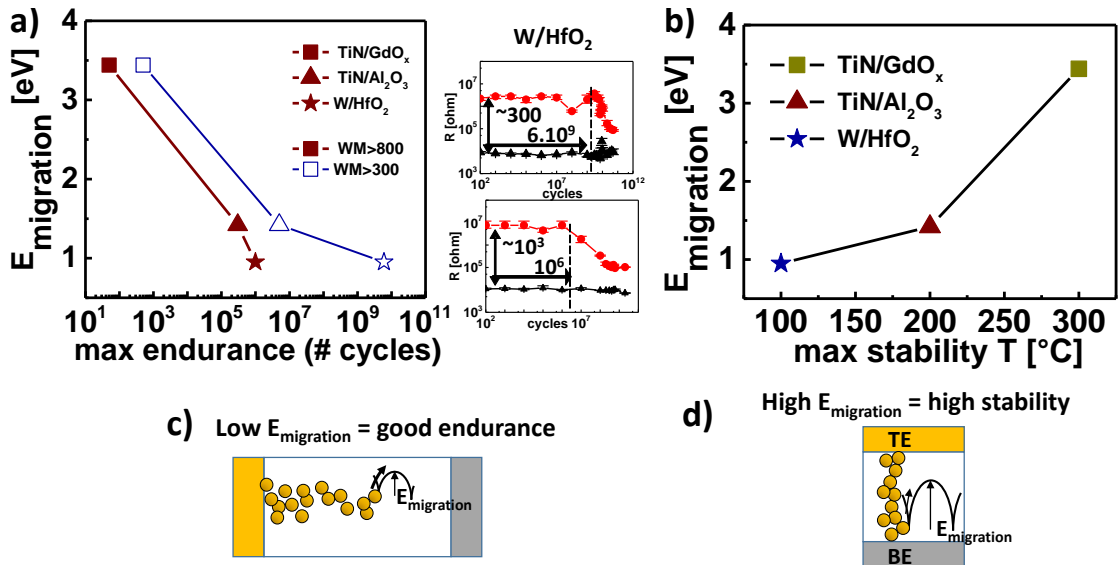
Figure 5.11: $E_{migration}$ impact study on a) endurance with typical curves to extract endurance at diffrent WM and b) retention. Schema of RRAM mechanism facilitating c) endurance d) retention
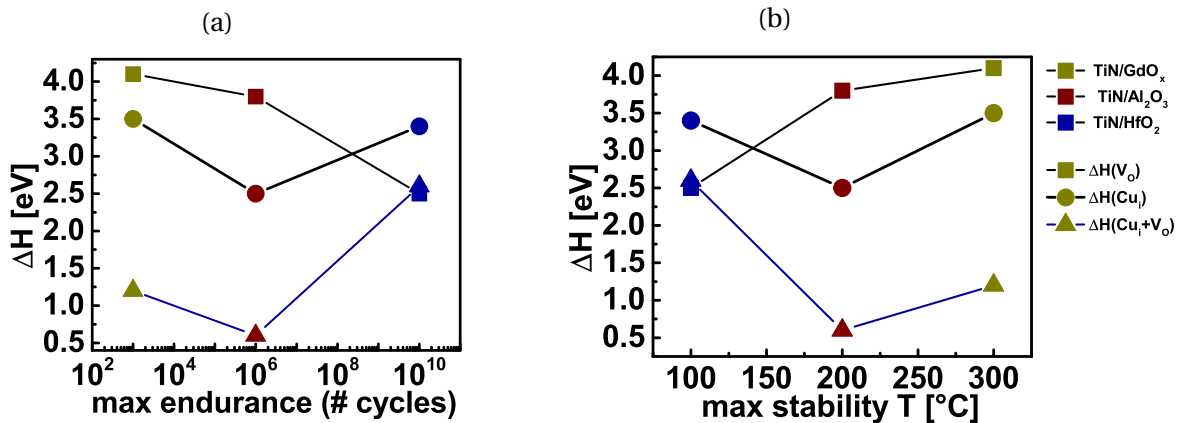
Figure 5.12: ΔH impact study on a) endurance and b) retention.

5.7.2 Qualitative explanation

To discuss in more details the previous observation, we propose the following description: a RRAM device can be characterized by a maximum energy, E_{max}, that can be sustained before oxide degradation and breakdown. This maximum energy is reached when a maximum number of cycles, N_{cmax}, is achieved. RRAM is then led to irreversible breakdown. For each cycle, provided energy, E_{cycle}, depends on the programming conditions. The maximum energy can thus be expressed with N_{cmax} and E_{cycle} (Equation (5.3)a). A fraction of E_{cycle} is transferred to ions and serves to switch the RRAM (E_{switch}) while another is transferred to the network and leads to material degradation such as defect generation. In our case, endurance failure is detected when RRAM can not be erased anymore. The cell is then stuck in R_{on} state meaning there are too much defects in the oxide which leads to a permanent conductive path. Creation of defects occurs during cycling and can be accelerated by the increase of V_{RESET} [12].

As it was previously demonstrated, increasing R_{OFF}/R_{ON} ratio leads to a drop in the number of cycles a cell can sustain. Thus, the maximum energy is reached faster if WM increases. In our description, we link the WM to the number of atoms involved during filament formation and disruption ($N_{moved\ atoms}$). Increasing SET programming condition leads to bigger conductive path, then composed of more atoms and resulting in lower R_{ON} and higher WM. However, increasing R_{OFF} means a bigger free defect area in resistive layer meaning that increasing RESET condition (time and voltage) is equivalent to increase the number of moving atoms during RESET. On the other hand, we also demonstrated that ion migration barrier impacts memory endurance. If $E_{migration}$ increases, the number of achieved cycle decreases. In our description, we thus assume that $E_{migration}$ is the required energy to move and drift each ion in the oxide, during filament formation and disruption. So, switching energy can be expressed as E_{switch} = $E_{migration}$ * $N_{moved\ atoms}$. The maximum energy of the dielectric can thus be expressed with the maximum number of cycles, the WM (through $N_{moved\ atoms}$) and $E_{migration}$. In S. Balatti *et al.* [12] a similar description of this phenomenon is given. Degradation of the oxide is controlled by activation energy and V_{RESET}. Irreversible endurance failure is associated to a high defect injection in conductive filament.

As explained previously, the switching energy (transferred to filament ions) only represents a fraction of the total supplied energy. Energy surplus is transferred to the network and degrades the oxide. We can express the total provided energy with E_{switch} and a degradation parameter α with

$E_{switch}=\alpha*E_{cycle}$, $0 < \alpha < 1$. α evolves with oxide degradation: the more the RRAM is cycled, the more the oxide is degraded, leading to a higher energy amount transferred to the network. We thus assume $\alpha = 1$ for a fresh cell (without defect) and gradually decreases with cycling. Finally we can express the maximum energy that the dielectric can sustain depending on N_{cmax}, E_{switch} and α (see 5.3).

$$E_{max} \propto N_{cmax} * E_{cycle} \tag{5.3a}$$

$$E_{cycle} \propto \frac{E_{switch}}{\alpha} \propto \frac{E_{migration} * N_{moved\ atoms}}{\alpha} \tag{5.3b}$$

$$E_{max} \propto N_{cmax} * E_{migration} * N_{moved\ atoms}$$
$$\Downarrow \quad\quad \Downarrow \quad\quad \Downarrow \tag{5.4}$$
$$\text{Endurance} \quad \text{Retention} \quad \text{WM}$$

Where E_{max} the maximum energy a dielectric can sustain before breakdown, N_{cmax} the maximum number of achieved cycles, E_{cycle} the total energy supplied per cycle, E_{switch} the energy needed to move the atoms to create the filament, α the degradation parameter such as $E_{switch}=\alpha*E_{cycle}$ and $0 < \alpha < 1$, $E_{migration}$ the activation energy to move one atom in the oxide and $N_{moved\ atoms}$ the number of involved atoms in the filament formation and disruption.

5.7.3 Impact on RRAM material choice

In parallel, $E_{migration}$ can be associated to the activation energy experimentally extracted from retention measurements. Figure 5.14a shows correlations between simulated and experimental $E_{migration}$ and memory endurance. Very good agreement is observed between simulated and experimental $E_{migration}$. Temperature stability failure can then be well associated with movement of Cu and V_O atoms which will disrup or form again the filament [19]. R_{OFF} failure, on Figure 5.14b, reveals a filament formation.

In conclusion, the maximum dielectric energy is linked to the memory performances and microscopic features of the memory technology: window margin (through the number of atoms involved in the filament formation and disruption), memory endurance (maximum number of cycles) and memory retention (through ion migration barrier). Consequently:

- Stronger programming conditions (current, time or voltage) enlarge the WM, decreasing N_{cmax} (and endurance) for a given memory technology (fixed E_{max}), as observed in Figure 6.1a.
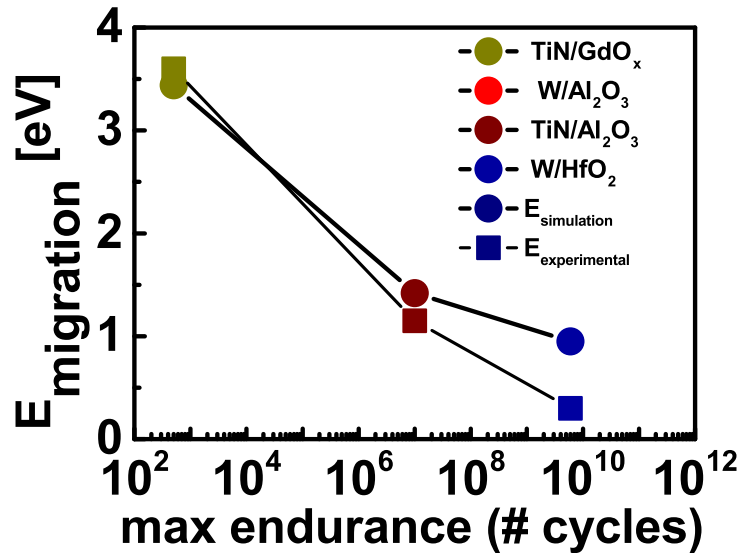
Figure 5.13: Migration energy barrier experimental and simulated as a function of maximum endurance.
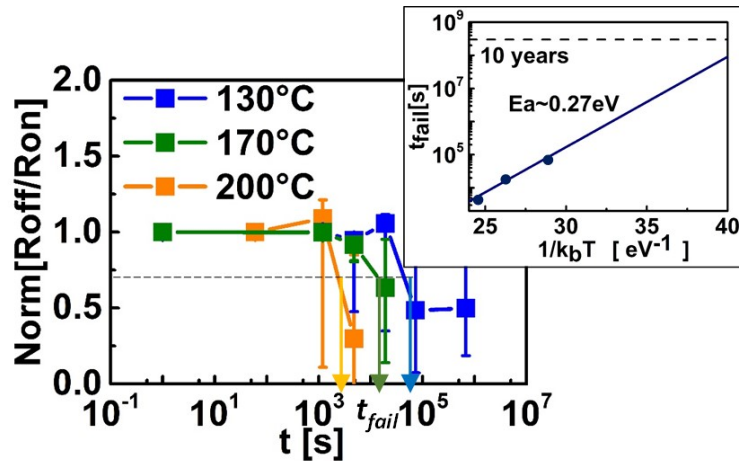
Figure 5.14: Extraction example of $E_{experimental}$ for W/HfO$_2$).

- Changing memory stack, it makes possible to tune the migration energy and favor either endurance or retention (Figure 6.1b, and Figure 5.11), for a fixed window margin.

Following observations must also be made:

- Dielectric optimization is of great importance; improving the material quality can lead to E_{max} increase and general improvement of the WM/endurance/retention trade-off. In literature, J. Woo *et al.* demonstrated that breakdown strenght of a material can be improved by thermal treatment [20].

- Top Electrode/oxide combination needs to be optimized to tune migration barrier. Unfortunately, this study needs to be done for each combination. However, some guidance can be given to avoid high

diffusion in oxides such as: controlling oxide grain boundaries, material structure and material density. It can be added that small metal atoms is an advantage for interstitial diffusion which is usually the most favorable.

- Understanding the defect generation during memory endurance is also critical. For a given window margin, different sets of programming parameters (current, time, voltage...) and memory stack features (top, bottom electrodes...) should minimize endurance failure, preventing early oxide degradation (Figure 5.4). Moreover, smart programming procedures is a way to adjust the energy provided to the system, reducing the energy surplus transferred to the network and degrading the memory dielectric.

The link between memory technology microscopic features and memory performances can be used to design an optimized memory stack. However, operating conditions need to be adjusted to reach the specifications of a given memory application. Figure 6.2 summarizes optimization for three applications. Low migration barrier and optimized WM favor endurance for Storage Class Memory (proposed stack: $W/HfO_2/CuTe_x$). Optimized SET current and long time programming conditions enlarge WM for data storage (proposed stack: $TiN/Al_2O_3/CuTe_x$). High migration barrier and large WM are favorable for embedded applications requiring high stability (proposed stack: $TiN/GdO_x/CuTe_x$).

5.8   Chapter V synthesis

In this chapter, we studied the trade-off between RRAM performances. Compromise between endurance and window margin is exposed for one technology. Increasing window margin changing SET and RESET condition lead to a degraded endurance. Comparing different devices, a link between retention and endurance vs WM improvement is presented. For a given WM, improving retention leads to a degraded endurance. Atomistic simulations are then used to bring insight from a material point of view. In particular, the ion migration barrier is correlated to the endurance/retention compromise. It can be tuned by TE/oxide combinaison and material engineering. Window margin improvement, changing the SET RESET conditions, degrades endurance. The optimization of the dielectric quality is a way to improve the overall window margin/retention/endurance compromise. Based on the understanding of the filament composition and char-

acteristics, various memory technologies are proposed to reach the specifications of different memory applications.
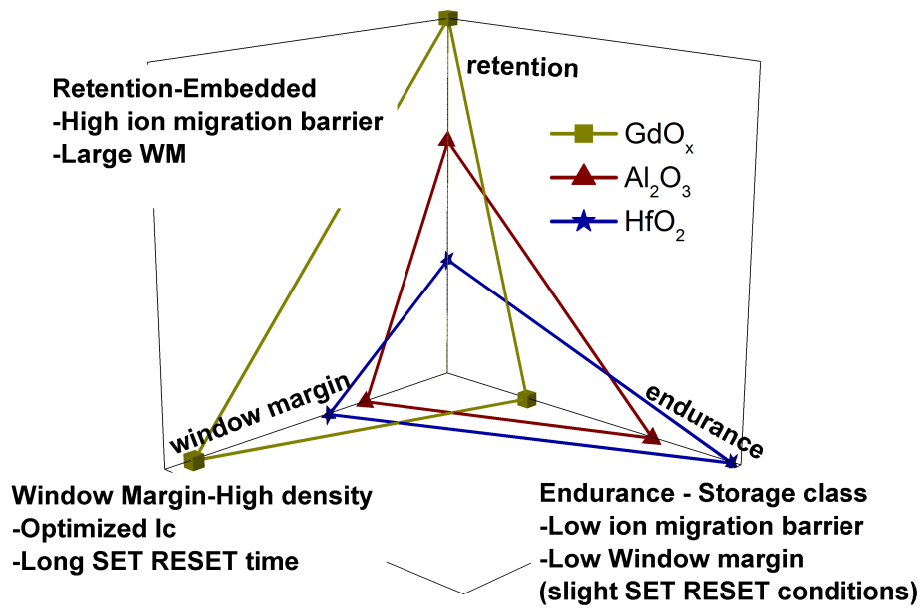
Figure 5.15: Radar plot of the performance trade-off for the various RRAM classes reported in this work, and critical key parameters (material microscopic properties and operating conditions).

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Chapter 6

Synthesis and perspectives

6.1 Objectives

Through this research work, electrical characterization combining with atomistic simulation allowed to improve filament formation understanding involved in HRRAM operation. However, a global physical comprehension of RRAM working principle is still lacking. This research work aims to offer a first approach to HRRAM physical mechanism, studying material stack parameters and electrical characteristics. Deep results on Al_2O_3/Cu based-HRRAM were presented giving insight on its complexity. Comparing with other stacks, different filament mechanisms were highlighted. Performances of the devices were extracted and trade-off between window margin, endurance and retention was presented. A correlation with material parameter, in particular ion migration barrier, was established and optimizations were proposed for different targetted applications. This last chapter will be organized around a synthesis of the mechanisms involved in different HRRAM devices. HRRAM optimization will be discussed in terms of programming conditions and material parameters. Finally, to conclude this work, we will highlight some perspectives to pursue HRRAM understanding and target industrial market.

6.2 Synthesis and direct perspertives of this work

6.2.1 HRRAM microscopic mechanism

Through Al_2O_3/Cu based-HRRAM results, insights on filament mechanism complexity were given. Electrical characterization was used to study polarization impact on filament formation and atomistic simulations gave results on charged species that could be influenced by electric field. It reveals V_O and V_{Al} influence on the filament formation and that Cu ions

charged +1 could be introduced in Al_2O_3 when TE is positively polarized. In this case, a hybrid filament formation is proposed: Cu movement assisted by oxygen vacancies. It can be noted as well that for alumina, Al point defects are not immobile and can help Cu insertion which is characteristics of this oxide. Atomistic study was performed on HfO_2 based HRRAM to study Cu insertion in this oxide and extract characteristic energies. Different behaviors appeared. HfO_2 has no favorable Hf point defects meaning Hf stays on site and does not influence filament formation. Moreover, HfO_2 reveals that both Cu and V_O are mobile whereas in Al_2O_3 V_O is not likely mobile. Table 6.1 summarizes Cu and V_O migration energy barrier and formation energies of these defects for both oxides.

Table 6.1: Migration energy barrier, E_a, and formation enthalpy, ΔH, between TE and different oxides either stoichiometric or including oxygen vacancies (Cu_iV_O defect).

Defect	ΔH_{HfO_2} (eV)	$E_{a\ HfO_2}$ (eV)	$\Delta H_{Al_2O_3}$ (eV)	$E_{a\ Al_2O_3}$ (eV)
Cu_i^{+1}	3.4	2.5	2.5	4
V_O^x	2.5 (+2)	0.7 (+2)	3.8 (0)	3.5 (0)
$(Cu_iV_O)^{+1}$	2.6	1.3	0.6	1.4
Filament	Cu_i and V_O moving		Cu_i moving next to V_O	
Cation point defects	immobile		$V_{Al}^{-3} E_a \sim 1.5eV$	

Among these two technologies with hybrid filament formation, composed of V_O and Cu, two HRRAM behaviors can be identified with mobile and fixed V_O. This research work can be pursued to study V_O mobility influence on HRRAM performances, especially endurance characteristics. It is envisaged that a high endurance (HfO_2/Cu versur Al_2O_3/Cu) would be linked to mobile oxygen vacancies. This feature will be studied in another paper.

The aim of this work was to bring insights on oxide based CBRAM working principle. Filament formation complexity and unicity was exposed and V_O plus Cu influence was showed. Now, filament formation study is still on going waiting for microscopic images and theory. However, material indicator could be extracted to bring guidance on appropriate material selection or engineering method to target the best material for a given application. This has been the goal of the next study.

6.2.2 HRRAM performances linked to microscopic properties

Recently, good characteristics were reported, making RRAM potential candidates to replace Flash for both stand alone, storage class applications [1] and embedded products [2, 3]. However, it is very challenging to combine all features such as having good cycling, stable retention at high temperature as well as high enough window margin depending on the targeted density. Comparing different oxides in atomistic simulation combined with HRRAM electrical characterization allowed to expose HRRAM performances interdependence and study material parameters influence. Through Al_2O_3/Cu, HfO_2/Cu and GdO_x/Cu study, trade-off between RRAM performances was exposed. First, compromise between endurance and window margin was established: for each technology, increasing WM, changing SET RESET conditions, leads to degraded endurance. Then, comparing different devices, a link between retention and endurance vs WM improvement was presented. For a given WM, improving retention leads to a degraded endurance (Figure 6.1).
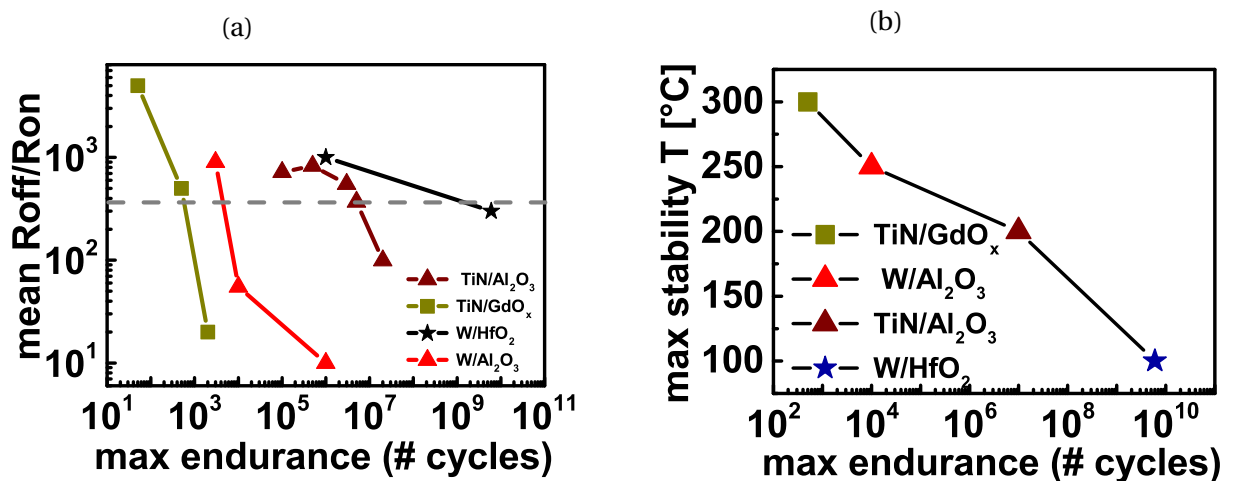
Figure 6.1: a) Window Margin as function of maximum endurance. For each RRAM technology, various WM were achieved changing the RESET conditions. Gray line is used to extract b) for a constant WM. b) Maximum stable retention temperature after 24h baking time as function of maximum endurance for a given WM (R_{OFF}/R_{ON} ~400).

Atomistic simulations were then used to bring insight from a material point of view. In particular, the ion migration barrier was correlated to the endurance/retention compromise. This study allowed to give some guidance on appropriate material selection or engineering method to target a given application:

- Stronger programming conditions (current, time or voltage) enlarge the WM, decreasing endurance for a given memory technology.

- Changing memory stack, it makes possible to tune the migration energy and favor either endurance or retention, for a fixed window margin.

- Dielectric optimization is of great importance; improving the material quality can lead to a general improvement of the WM/endurance/retention trade-off. In literature, J. Woo *et al.* demonstrated that breakdown strenght of a material can be improved by thermal treatment [4].

- Top Electrode/oxide combination needs to be optimized to tune migration barrier. Unfortunately, this study needs to be done for each combination. However, some guidance can be given to avoid high diffusion in oxides such as: controlling oxide grain boundaries, material structure and material density. It can be added that small metal atoms is an advantage for interstitial diffusion which is usually the most favorable.

- Understanding the defect generation during memory endurance is also critical. For a given window margin, different sets of programming parameters (current, time, voltage...) and memory stack features (top, bottom electrodes...) should minimize endurance failure, preventing early oxide degradation. Moreover, smart programming procedures is a way to adjust the energy provided to the system, reducing the energy surplus transferred to the network and degrading the memory dielectric.

The link between memory technology microscopic features and memory performances can be used to design an optimized memory stack. However, operating conditions need to be adjusted to reach the specifications of a given memory application. Figure 6.2 summarizes optimization for three applications. Low migration barrier and optimized WM favor endurance for Storage Class Memory (proposed stack: $W/HfO_2/CuTe_x$). Optimized SET current and long time programming conditions enlarge WM for data storage (proposed stack: $TiN/Al_2O_3/CuTe_x$). High migration barrier and large WM are favorable for embedded applications requiring high stability (proposed stack: $TiN/GdO_x/CuTe_x$).
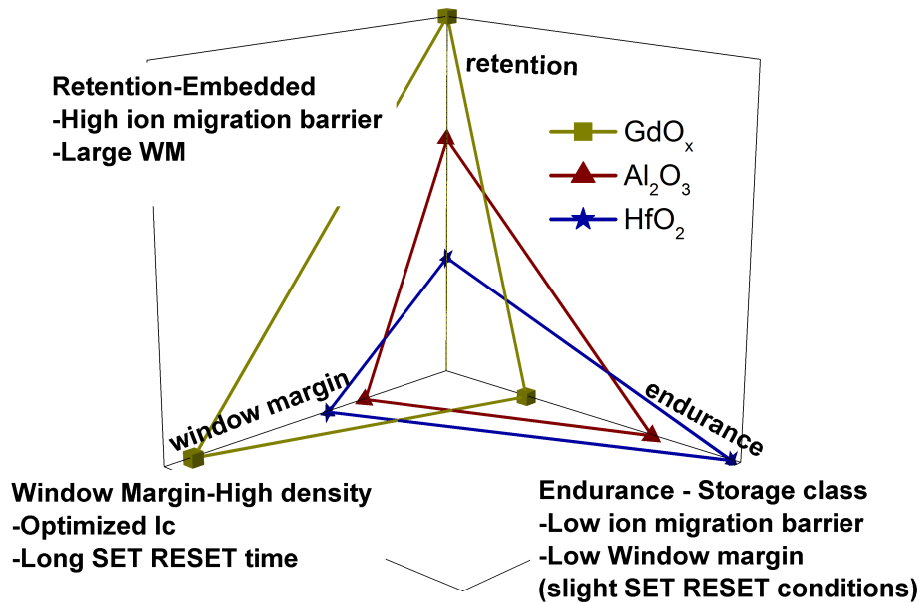
Figure 6.2: Radar plot of the performance trade-off for the various RRAM classes reported in this work, and critical key parameters (material microscopic properties and operating conditions).

6.3 General perspertives

6.3.1 RRAM understanding

Dielectric oxide breakdown modelization

Oxide-based CBRAM are correlated to dielectric oxide breakdown behavior. Improving theory in this field would help to model its working principle and engineer the oxide. Percolation model and defect generation study during cycling are the next step to be able to modelize a full RRAM behavior. Figure 6.3 shows an example of analytic model for oxide breakdown based on J. suñé *et al.* [5]. This approach could be used to model RRAM behavior and understand cycling failure as a first work can show in C. Nail *et al.* [6]. One perspective of this research work is to pursue RRAM understanding by a complete cycling weariness modelling with a percolation approach. For this kind of study, statistics on electrical behavior and on modelling are necessary through for example matrices characterization and kinetic monte carlo simulation.

Thermal effect in RRAM working principle

In order to understand RRAM working principle, thermal impact study need to be addressed. In Guy.et al [7], bottom electrode impact on conductive filament was studied exposing its influence on RRAM erasement (Figure 6.4). Studying in more details its feature to integrate it in RRAM perfor-

(a)

(b)
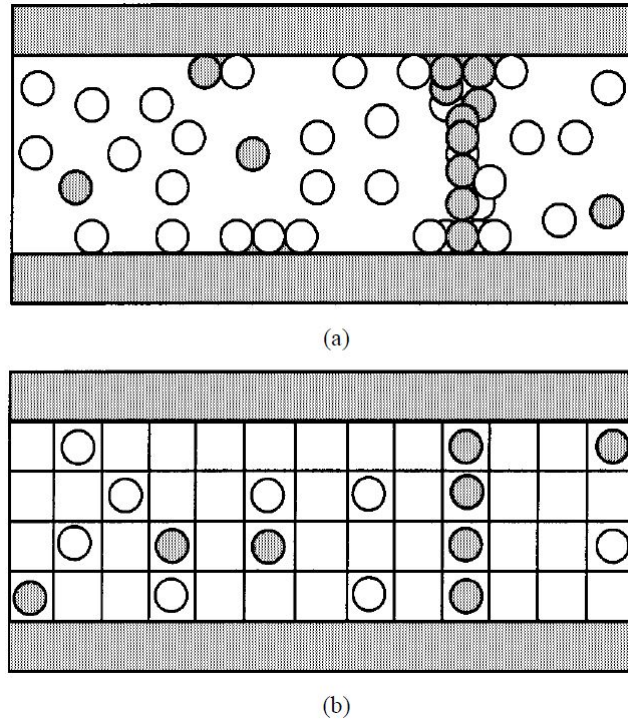
Figure 6.3: Schematic picture showing the generation of defects and breakdown triggering condition in (a) the percolation approach and (b) the new analytic framework presented in [5].

mances trade-off would give another engineering lever for WM/endurance compromise. Moreover, it would allow to modelize SET/RESET behaviors and understand filament kinetic formation. This would give acces to resistance calculation from material and electrical test parameters.

Figure 6.4: Schema of filament disruption during RESET for WSi and TiN bottom electrode illustrating disruption point and residual filament after RESET

6.4   Industrial perspectives

6.4.1   Targetting low consumption

Today, power consumption is an unavoidable argument for memory characteristics. It is not possible anymore to overlook the energy efficiency of memory operations (allocate, copy, move, initialize) even if operations take place in a data center and not on mobile device (phones, tablets, convertibles). Memory and storage power consumption constitute a major portion of the compute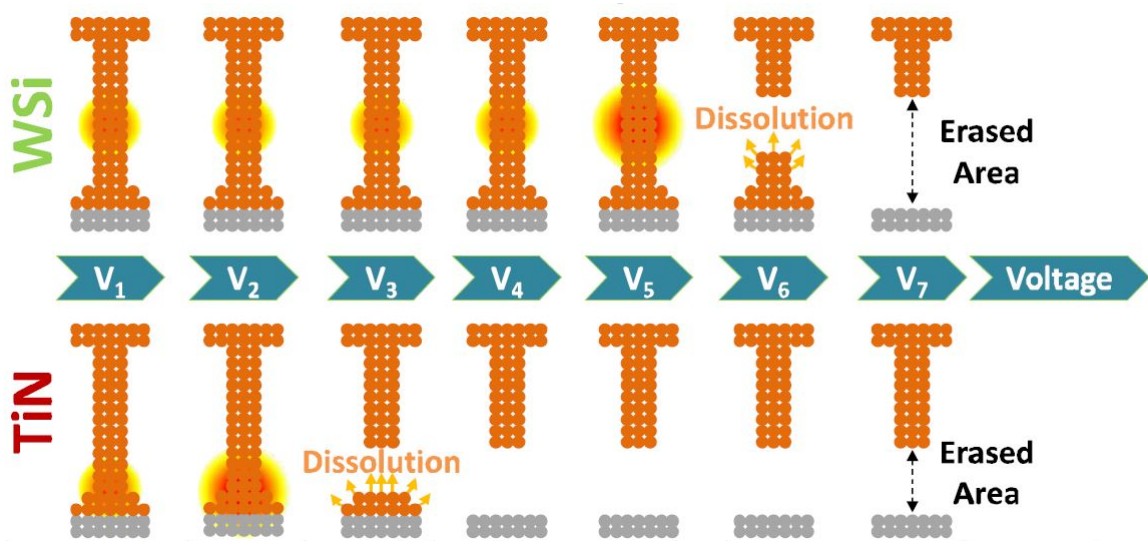 cost when the cooling and power overhead are also considered (Figure 6.5). Data center and mobile devices' energy consumption growth is a big concern. For example, memory hierarchy (SRAM, DRAM, NAND storage) contributes around 25% of smartphone power in the video capture [8]. Future memory devices will need to have low power consumption. RRAM already showed promising characteristics [9, 10] and programming optimizations attract attention to balance power consumption and RRAM variability [11, 12]. Future research will need to focus on this aspect and find technological keys to low power consumption.
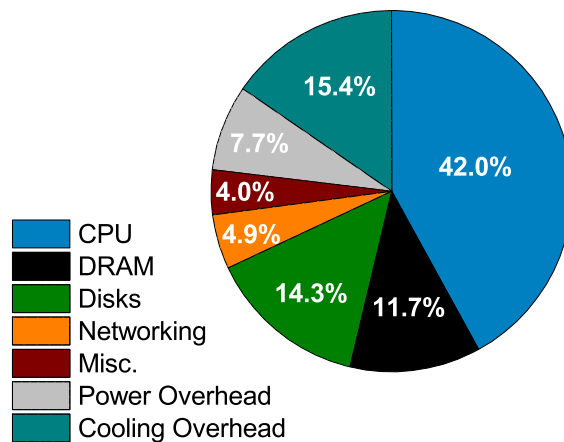

Figure 6.5: Energy demand in data centres [8]

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Programming Optimization for Low Power and Short Latency time in RRAM arrays. In *2017 IEEE International Electron Devices Meeting*, 2017. 117

Publications

Journals

C. Nail, P. Blaise, G. Molas, M. Bernard, A. Roule, A. Toffoli, L. Perniola, and C. Vallee, *"Atomistic mechanisms of copper filament formation and composition in Al2O3-based conductive bridge random access memory"*, Journ. of Appl. Phys, 122, 024503 (2017).

C. Nail, G. Molas et al., *"A link between CBRAM performances and material microscopic properties based on electrical characterization and atomistic simulations"*, IEEE Trans. on Elec. Dev., 2017, in press.

Conferences with proceedings

C. Nail, P. Blaise, G. Molas, M. Bernard, A. Roule, A. Toffoli, C. Vallée, L. Perniola, *"Investigation of the Ion Exchanges between Al2O3 and CuTe for Hybrid RRAM"*, SISC 2015 (Washington, US).

C. Nail, P. Blaise, G. Molas, M. Bernard, A. Roule, A. Toffoli and L. Perniola, *"Investigation of Ions Movement during the operation of Al2O3-based CBRAM using thermodynamic and kinetic theoretical approaches"*, proc. of CIMTEC 2016.

C. Nail, G. Molas, P. Blaise, G. Piccolboni, B. Sklenard, C. Cagli, M. Bernard, A. Roule, M. Azzaz, E. Vianello, C. Carabasse, R. Berthier, D. Cooper, C. Pelissier, T. Magis, G. Ghibaudo, C. Vallée, D. Bedau, O. Mosendz, B. De Salvo, L. Perniola, *"Understanding RRAM endurance, retention and window margin trade-off using experimental results and simulations"*, IEDM 2016 Tech. Dig., pp.95-98.

G. Molas, G. Piccolboni, M. Barci, C. Nail, B. Traore, J. Guy, R. Coquand, E. Vianello, P. Blaise, J. M. Portal, M. Bocquet, A. Levisse, B. Giraud, J. P. Noel, M. Harrand, M. Bernard, A. Roule, B. De Salvo, L. Perniola, *"Opportunities for resistive RAM (RRAM) for non-volatile memory applications"*, proc. of NVMTS 2016, invited.

C. Nguyen, C. Cagli, G. Molas, B. Sklenard, C. Nail, K. El Hajjam, J.F. Nodin, C. Charpin, S. Bernasconi, G. Reimbold, *"Study of Forming impact on 4Kbit RRAM array performances and reliability"*, proc. of IMW 2017 (Monterey, US), pp.80-83.

G. Molas, M. Harrand, C. Nail, G. Sassine, D. Alfaro Robayo, C. Cagli, E. Vianello, P. Blaise, A. Levisse, B. Giraud, J. P. Noel, B. De Salvo, L. Perniola, *"Investigation of Resistive Memories (RRAM) to solve the memory bottleneck in computing systems"*, IMRC 2017 (Cancun, Mexico), invited.

P. Blaise, B. Sklenard, B. Traore, C. Nail, E. Vianello, G. Molas, *"Resistive RAM Memories from a Material Perspective: Exploration of the Switching for Several Oxides Using Ab Initio Simulations"*, Electro Chemical Society 2016 (Honolulu US)

R. Berthier, N. Bernier, C. Nail, C. Carabasse, G. Molas, C. Sabbione, F. Hippert, P. Noé and D. Cooper, *"Resistive Memories Studied By In Situ Transmission Electron Microscopy"*, European Microscopy Congress (EMC) 2016 (Lyon)

B. Sklénard, P. Blaise, B. Traoré, A. Dragoni, C. Nail and E. Vianello, *Advances in the understanding of microscopic switching mechanisms in ReRAM devices*, European Solid-State Device Research and Solid-State Circuits conferences (ESSDERC) 2017, invited.

Appendix A

Annexes

A.1 Simulation framework

Atomistic simulations were realized with Siesta code [?] within DFT [? ?] using a generalized gradient approximation (GGA/PBE) and Troullier-Martins pseudopotentials for Al $3s^2 3p^1$, Hf $6s^2 5d^2$, Gd $6s^2 5d^1 4f^7$, O $2s^2 2p^4$, Cu $3d^{10} 4s^1$, Te $4d^{10} 5s^2 5p^4$ and Ge $3d^{10} 4s^2 4p^2$ to account for core electrons [?]. Polarized double-zeta basis set with an energy shift of 50 meV and a mesh cutoff between 300 to 400 Rydberg with a convergence criterion for the maximum force acting on an atom to be smaller than 0.02eV/Å were used. The Nudge Elastic Band (NEB) calculation was done with 10 to 20 images, 1 k point, a spring constant of 0.1eV/Å, a maximum force of 0.1eV/Å and a climbing image.

A.2 Figures annexes

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A.3 Tableaux annexes

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