Edge Effects on Magnetic Proprieties of CoFeB-MgO Based Nanodevice

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Edge Driven Magnetic Switching in CoFeB-MgO Based Spintronic Nanodevices

Thèse de doctorat de l'Université Paris-Saclay et de l'Université de Beihang
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Yu Zhang

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Thèse de doctorat

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CONTENTS

ABSTRACT

Mainstream memories are limited in speed, power and endurance (Flash, EEPROM) or cannot retain data without power (SRAM, DRAM). In addition, they are approaching physical scaling limits. Non-volatile memories (NVMs) combined with novel computing architectures have recently been considered as the most promising solution to overcome the “memory wall” of von-Neumann computing systems [Lin12, Yan13, WON15]. For instance, in-memory computing architectures built by closely integrating NVMs with logic functions have been proposed to minimize the power consumption and pave the way towards normally-off/instant-on computing [BOR10, SHU17]. Meanwhile, neuromorphic computing inspired by the human brain exploits the resistive features of NVMs as artificial synapses and neurons and has already triggered a revolution for non-von-Neumann architectures [LOC13, GRO16, PRE15]. Along this direction, magnetic random access memory (MRAM) and resistive random access memory (RRAM) [WON15, WON12, LIN14, CEL14], have attracted increasing interest.

MRAM technologies have been expected to be applicable to a wide variety of applications. One critical issue for MRAM technologies is that the variability of nanostructures leads to the distribution of the magnetic properties. Especially, when the dimension of the device shrinks into nanoscale, the edge contribution has an increased influence on the switching behavior and limits the density. This thesis focuses on the influence of edge damages introduced by the patterning process on the magnetic switching of spintronic nanodevices. After that, the thesis will show how to take advantage of it for new functionalities in advanced storage and computing system.

Two typical magnetic switching have been investigated: (i) field-induced switching in magnetic nanodots with perpendicular magnetic anisotropy (PMA) and (ii) current-induced switching in magnetic tunnel junctions (MTJ) with in-plane magnetization. Along this line, we first have developed the full nanofabrication process for both MTJ nanopillars down to 100 nm and magnetic nanodots down to 400 nm using conventional electron beam lithography (EBL), ion beam etching and lift-off approach. By studying the switching field distribution (SFD) of magnetic nanodots using Kerr microscopy, we show that magnetization reversal is dominated by the nucleation and pinning of domain walls (DWs) at the edges of the nanodots due to the damages induced by patterning process. For MTJ nanopillars, we show that by using SiO_2-based insulator material for encapsulation, unexpected resistive Si filaments are formed at the edges of the MTJ. These Si filaments exhibit resistive switching, which allow us to demonstrate for the first time a heterogeneous memristive device, namely resistively enhanced MTJ (Re-MTJ) that combines magnetic and resistive switching. The potential application for Re-MTJ as a logic-in-memory device with memory encryption function is discussed.

Keywords: Magnetic tunnel junction (MTJ), domain wall (DW), surface tension, resistive switching, multi-level cell, logic-in-memory, nonvolatile memory.

RESUME

Les mémoires courantes sont limitées en vitesse, puissance et endurance (Flash, EEPROM) ou ne peuvent pas conserver les données sans alimentation (SRAM, DRAM). En outre, elles s'approchent des limites de mise à l'échelle physique. Des mémoires non-volatiles (*Non-volatile memories, NVM*) combinées à de nouvelles architectures informatiques ont été considérées récemment comme la solution la plus prometteuse pour surmonter le «mur de mémoire» dans les systèmes informatiques de von-Neumann [Lin12, Yan13, WON15]. Par exemple, des architectures informatiques en mémoire construites par l'intégration de NVM rapides avec des fonctions logiques ont été proposées pour minimiser la consommation d'énergie et ouvrir la voie à l'informatique normalement bloqué/allumage instantané [BOR10, SHU17]. Entretemps, l'informatique neuromorphique inspirée par le cerveau humain exploite les caractéristiques résistives des NVM en tant que synapses et neurones artificiels, il a déjà déclenché une révolution pour les architectures non-von-Neumann [LOC13, GRO16, PRE15]. Dans cette direction, la mémoire MRAM et la mémoire RRAM [WON15, WON12, LIN14, CEL14] ont suscité un intérêt croissant.

Cette thèse se concentre sur la mémoire MRAM *(magnetic random access memory)*, qui est l'une des technologies émergentes visant à devenir un dispositif de mémoire «universel» et applicable dans plusieurs domaines. Un problème critique pour les technologies de MRAM est que la variabilité des nanostructures conduit à la distribution des propriétés magnétiques. En particulier, lorsque la dimension du dispositif se réduit à nano-échelle, la contribution du bord a une influence accrue sur le comportement de commutation magnétique et limite aussi la densité. Cette thèse étudie l'influence des dommages aux bords introduits par le procédé de formation de motifs pour la commutation magnétique des nanodispositifs spintroniques. Ensuite, ses nouvelles fonctionnalités dans les nanodispositifs ont été illustrées.

Deux commutations magnétiques typiques ont été étudiées: (i) commutation induite par le champ dans les nanodots magnétiques avec anisotropie magnétique perpendiculaire (*perpendicular magnetic anisotropy, PMA*) et (ii) commutation induite par le courant dans les jonctions tunnel magnétiques *(magnetic tunnel junctions, MTJ)* avec aimantation dans le plan. Dans cette optique, nous avons d'abord développé le procédé complet de nanofabrication pour des nanodots magnétiques de taille minimale de 400nm et des nanopiliers MTJ de taille minimale de 100nm en utilisant la lithographie conventionnelle par faisceau électronique, la gravure par faisceau ionique et l'approche de décollement. En étudiant la distribution du champ de commutation (*switching field distribution, SFD*) des nanodots magnétiques à l'aide de la microscopie Kerr, nous montrons que l'inversion de l'aimantation est dominée par la nucléation et l'épinglage de paroi de domaine (*domain wall, DW*) sur les bords des nanodots dû aux dommages induits par le procédé de formation de motifs. Pour les nanopiliers MTJ, nous montrons qu'en utilisant un matériau isolant à base de SiO_2 pour l'encapsulation, des filaments de Si résistants imprévus sont formés sur les bords de MTJ. Ces filaments présentent une commutation résistive, ce qui nous permet de démontrer pour la première fois un dispositif memristive hétérogène, appelé MTJ résistiquement amélioré (*resistively enhanced MTJ, Re-MTJ*), qui combine la commutation magnétique avec la commutation résistive. L'application potentielle de Re-MTJ en tant que dispositif de mémoire à logique avec fonction de cryptage de la mémoire est discutée.

Mots-clés: Jonctions tunnel magnétiques (MTJ), paroi de domaine (DW), commutation magnétique, procédé de formation de motifs, dommages aux bords, mémoire non volatile.

GENERAL INTRODUCTION

Spintronics has been recognized as an important scientific achievement after the 2007 Nobel Prize in Physics awarded to Albert Fert and Peter Grünberg for their discovery of the giant magnetoresistance (GMR) effect [THO08]. Different from the traditional electronics, the emerging spintronics takes advantage of the electron spin rather than electron charge to carry information. It offers a new opportunity for novel devices, which combines the standard CMOS technology with spin-dependent effects. Spintronics paves the way toward low power and high density applications including memory, sensors and logic devices.

In 1988, the GMR effect was observed in a spin-valve structure, that is, a non-magnetic metal layer sandwiched by two ferromagnetic layers. When the magnetization direction of the two ferromagnetic layers are parallel (P), the resistance is low whereas when they are anti-parallel (AP), the resistance is high. This discovery has enabled the possibility for miniaturization of the hard disks in recent years [FUL16]. An all-metal based spin valve can exhibit a small GMR ratio below 5% with low resistance of several ohm (Ω) [HUA08].

Later in 1995, tunneling magnetoresistance (TMR) effect was observed in magnetic tunnel junctions (MTJ) involving alumina [MOO95]. This observation has led to the concept of magnetic random access memory (MRAM), which combines nonvolatility, unlimited endurance, fast access speed, good scalability, and compatibility with the back-end-of-line (BEOL) technology of CMOS. Although Al-O-based MTJs exhibit 70% TMR ratio at room temperature, higher MR ratio is needed for practical MRAM applications [YUA07]. In 2001, first-principles based calculations predicts a 1000% MR ratio for epitaxial MTJs including a crystalline magnesium-oxide (MgO) tunnel barrier [BUL01]. A TMR of 600% at room temperature (RT) was first observed in 2004 for sputtered MTJs with a CoFeB-MgO based structure [IKE08].

In 1996, Sloncwezski and Berger published their theoretical paper on spin-transfer torque (STT) [SLO96, BER96], and in 2004 the STT switching was experimentally demonstrated in Al-O-based MTJs [HUA04, FUC04]. Instead of a magnetic field, the magnetization switching can be enabled by a polarized current, which exerts a spin torque on the magnetic moment of free layer of MTJ through a transfer of angular momentum to the free layer magnetization [YUA07]. This triggered the development of the second generation of MRAM, called spin-transfer torque MRAM (STT-MRAM). Compared to the first generation magnetic-field-switched MRAM, STT-MRAM has significant advantages for lower switching current, simpler cell architecture and better scalability with the shrinking of technology nodes. For high-performance MTJs driven by STT, a low intrinsic threshold current, a high thermal stability factor and a high TMR ratio are needed, for lower power consumption, long data retention and good fault tolerance, respectively. In MRAM, memory retention is related to the height of energy barrier, which corresponds to the product of the magnetic anisotropy K by the magnetic volume V. In the context of the development of STT-MRAM, out-of-plane MTJs have been shown to have higher thermal stability factor and lower critical current [KAW12, DIE17]. In 2010, Ikeda and co-workers reports CoFeB-MgO based MTJs with perpendicular magnetic anisotropy (PMA) [IKE10]. They exhibit a high TMR of 120%, high thermal stability at dimension of 40 nm diameter, and can be switched by STT effect at a low switching current. Such CoFeB-MgO material system has proved to be an ideal choice for providing a lower Gilbert damping factor, high magnetic anisotropy and low writing current, which satisfies all the conditions for high-performance perpendicular MTJs. This work was a milestone in MRAM development and the research and develop efforts devoted to MRAM begin to focus on further optimizing CoFeB-MgO based MTJs with PMA.

So far, the major microelectronics companies are working on the development of CoFeB-MgO based STT-MRAM at technology node of 16-nm and beyond [DIE17]. The company Everspin is currently commercializing 256 Mb standalone memories and it has developed a partnership with GlobalFoundries to start producing embedded memories for micro-controller units (MCUs). In order to meet the demand of high-density applications, such as DRAM replacement, the dimension of the memory cell of STT-MRAM needs to be reduced toward even smaller technology nodes (and smaller pitch). However, the structural variability of magnetic materials (interface roughness and intermixing, crystalline texture, grain boundaries …) leads to a distribution of the magnetic properties (TMR, magnetic anisotropy, damping …), which limits the development of STT-MRAM beyond the 20 nm technology node. In addition, as the size of the magnetic devices decreases, the influence of edge damages introduced by the nanofabrication process becomes a crucial limitation for the magnetic memory technology. In particular, the etching process of nanopillars has been found to be the main limitation for developing sub-20 nm STT-MRAM cells since a typical MTJ stack involves more than 10 different materials.

The main aim of this thesis is to highlight the influence of edge damages introduced by the nanofabrication processes on the switching behavior of magnetic nanostructures. Two typical switching process in spintronic nanodevices are investigated: (i) field-induced switching in magnetic nanodots with perpendicular anisotropy, (ii) current-induced switching in MTJs with in-plane magnetization. In order to study these two types of nanodevices, a large part of my research work has been devoted to developing the full nanofabrication process using the advanced facilities of the C2N (Centre de Nanosciences et de Nanotechnologies) clean room. Finally, new functionalities in spintronic nanodevices are showed by taking advantage of the influence of edge damages on magnetic switching.

This manuscript is divided into four chapters:

In the first chapter "**Background and Context**", we introduce the main concepts of spintronics that we have used in this thesis, including the GMR effect, TMR effect, STT effect, the feature of CoFeB-MgO material system and the concept of MTJ as well as the applications based on it.

In the second chapter "**Materials Growth and Nanofabrication**", the full fabrication process flows of two magnetic devices, e.g. MTJ nanopillars and nanodots, are described. These technological developments represent a large part of my Ph.D work.

In the third chapter "**Magnetization Reversal of Nanodots Governed by Laplace Pressure"**, the switching process of magnetic nanodots with PMA and of sizes from 400 nm to 1 µm is investigated using Kerr microscope. We evidence that the edge damages induced by patterning process govern the switching process of nanodots by controlling the domain wall motion.

In the fourth chapter "**Resistively Enhanced MRAM Device**", we show that by using SiO_2-based insulator material to encapsulate STT-MTJ nanopillars with in-plane magnetization, resistive Si filaments are formed at the edges of MTJs due to the damages induced by the patterning and encapsulation process. These Si filaments exhibit resistive switching behavior, which allows us to demonstrate a novel heterogeneous memristive device composed of an MTJ nanopillar surrounded by resistive silicon switches.

CHAPTER 1 BACKGROUND AND CONTEXT

The objective of this thesis is to study the influence of edge damages on magnetic switching in two representative CoFeB-MgO based nanodevices: (i) field-induced switching in magnetic nanodots with perpendicular magnetic anisotropy (PMA) and (ii) spin-transfer torque (STT) switching in magnetic tunnel junctions (MTJs) with in-plane magnetization. The present chapter is a brief review devoted to spintronics in general and particularly to the CoFeB-MgO material system, which is widely used in MRAM applications.

1.1 GMR effect

The spin-dependent electron transport phenomena has been studied in the 1970s and the milestone is the discovery of giant magnetoresistance (GMR) by Albert Fert [FER08] and Peter Grünberg [GRU08] in 1988 and 1989, separately. They were awarded for the 2007 Nobel Prize in Physics [THO08]. The basic idea of spin-dependent scattering mechanism is that the scattering probability of the itinerant electrons depends on the relative directions of the electron spin and the ferromagnetic (FM) magnetization. As such, GMR effect can be observed in a spin-valve structure, that is, a non-ferromagnetic (NM) layer sandwiched by two FM layers (FM/NM/FM). Based on the spin-dependent scattering mechanism, the GMR effect can be explained (see Figure 1) using a two spin-channel model [FER08]. When the magnetization directions of two FM layers are parallel, the spin-up electrons will go through the two FM layers without significant scattering while most of spin-down electrons will be scattered. Then it leads to a low resistance R_L. However, when the magnetization directions of two FM layers are anti-parallel, both the spin-up electrons and spin-down electrons will be scattered, which leads to a high resistance R_H. The GMR ratio can be defined as:

$$GMR = \frac{\Delta R}{R_L} = \frac{R_H - R_L}{R_L} \tag{1.1}$$

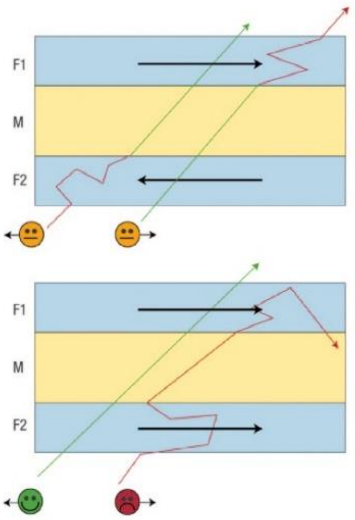


Figure 1 Two spin-channel model of GMR effect based on spin-dependent scattering. The figures is reproduced from Fert et al. [FER08]

The discovery of GMR effect has driven both theoretical and practical evolution of information technology. The first commercial GMR read heads appeared in hard disk in 1997 and it greatly promotes the increasing of the storage density [THO08]. The storage density has approached more than 1 Tb/in^2 up to today and one could see a nearly 10^9 increase over the 60-year development history of the hard drive with a corresponding ~ 10^9 decrease in the cost per bit [FUL16].

1.2 Magnetic Tunnel Junction and TMR effect

1.2.1 Structure of Magnetic Tunnel Junction

Magnetic Tunnel Junction (MTJ), the core structure of magnetic random access memory (MRAM), consists of an insulating barrier layer sandwiched by two FM layers, as shown in Figure 2 [YUA07]. The insulating barrier, e.g. the tunneling barrier, is thin enough for the tunneling effect of electrons. The magnetization of the two FM layers lie along the easy axis of the uniaxial magnetic anisotropy, which defines two stable states at remanence: when an external magnetic field or a spin-polarized current is applied, the magnetization direction of the FM layers can be changed. For the practice application in electronics, the magnetization direction of one FM layer is always fixed on purpose (i.e. reference layer), while the other one is switchable (i.e. free layer).

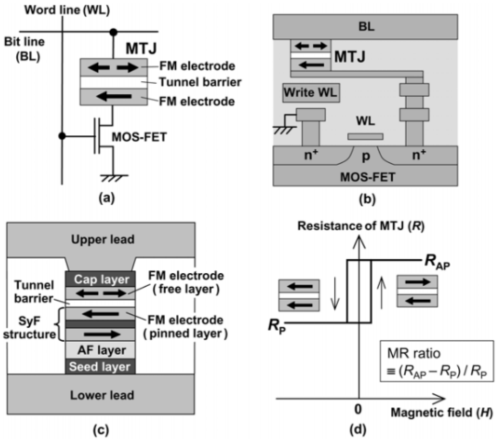


Figure 2 The basic structure of MTJ. (a) is the basic circuit diagram and (b) is the typical cross-sectional structure of a MRAM cell. (c) is a typical cross-sectional structure of a MTJ for practical applications. (d) shows a typical magnetoresistance curve of a MTJ and the definition of MR ratio. The figures are reproduced from Yuasa et al. [YUA07]

1.2.2 TMR effect in MTJ

In a MTJ structure, the electrons go through the barrier layer by tunneling effect. Similar to the GMR, the tunnel magnetoresistance (TMR) is related to the configuration of the magnetization of the two FM layers in MTJ. If the magnetization direction of two FM layers are parallel (P), then a low resistance R_P is obtained and otherwise, a high resistance R_{AP} is expected for the anti-parallel (AP) configuration. The TMR ratio can be defined as:

$$TMR = \frac{\Delta R}{R_P} = \frac{R_{AP} - R_P}{R_P} \tag{1.2}$$

where R_p and R_{AP} are the resistances for P and AP states, respectively.

Similar to the GMR effect, the TMR effect is also due to the spin-dependent tunneling, which can be further explained under the energy band theory. As shown in Figure 3 [YUA07], for a ferromagnetic material, there is an imbalance between the populations of spin-up and spin-down electrons. The difference between density of the states for spin-up and spin-down electrons leads to a net magnetic moment and the magnetization of the FM layer. During the transport, the electrons near the Fermi level act as the carriers of spin. Since the tunnel barrier is thin enough, the electrons can conserve their spin feature, e.g. spin-up (↑) or spin-down (↓), through the tunneling process. In this context, for instance, a spin-up (spin-down) electron from one FM layer can tunnel through the barrier layer if and only if it can find a spin-up (spin-down) state to occupy in the other FM layer near the Fermi level. For the P state, since the band structures of the two FM layers are almost identical, all the electrons, e.g. for both spin-up and spin-down, can find available states during the transmission from the on FM to the other. However, for the AP state, only partial electrons can act as carriers for the tunneling current. In this context, the resistance for the AP state is higher than that for the P state. The extent of the band imbalance for an FM layer can be further evaluated by the parameter of spin-polarization P, which can be defined as

$$P = \frac{\left| n\uparrow - n\downarrow \right|}{n\uparrow + n\downarrow} \tag{1.3}$$

where $n\downarrow$ and $n\uparrow$ are the numbers of spin-down and spin-up carriers, respectively.

Julliere [JUL75] proposed that the TMR effect is strongly dependent on the spin-polarization of the FM and can be described as

$$TMR = \frac{2P_1P_2}{1-P_1P_2} \tag{1.4}$$

where P_1 and P_2 are the spin-polarization for the two FM layers.

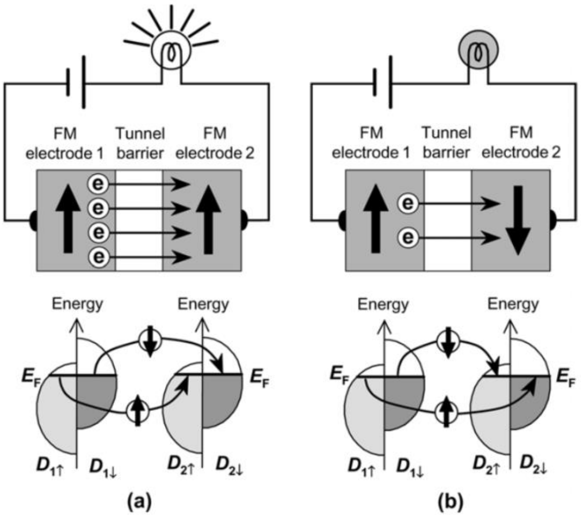


Figure 3 Schematic illustration of TMR effect. $D_{1\uparrow}$ and $D_{1\downarrow}$ denote the density of states at E_F for the majority-spin and minority-spin bands in the FM layer 1, whereas $D_{2\uparrow}$ and $D_{2\downarrow}$ denote the density of the states at E_F for the majority-spin and minority-spin bands in the FM layer

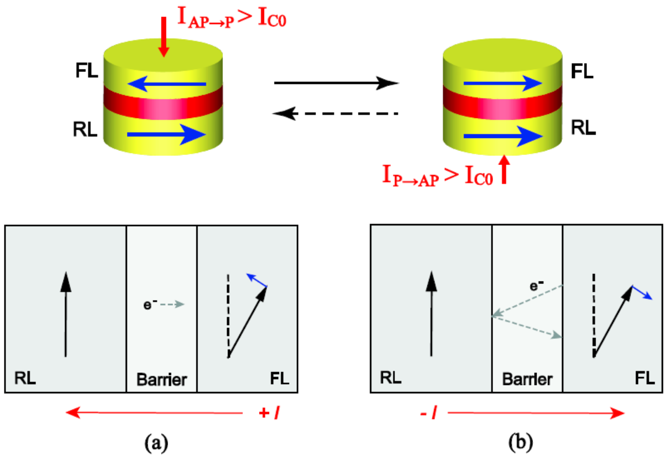
2. The figures are reproduced from Yuasa et al. [YUA07]

TMR ratio is a key parameter for the MTJ performance and a high TMR ratio means the better fault tolerance for practical applications.

1.3 Spin Transfer Torque effect

Spin-transfer torque (STT) is an important breakthrough in the development of spintronics after the discovery of GMR effect and TMR effect. In 1996, Slonczewski [SLO96] and Berger [BER96] theoretically predicted that the magnetization of the free layer can be influenced by a spin-polarized current. As shown in Figure 4, when the electrons flow from the reference layer to the free layer, the current will be spin-polarized by the reference layer and it results in a spin angular momentum nearly aligned to the direction of magnetization of the reference layer. Due to the conservation of angular momentum, the transverse angular momentum will be transferred to the magnetization of the free layer when those spin-polarized electrons go into the free layer. This process will induce a torque to align the magnetization of the free layer in the parallel direction to the reference layer, which results in a P configuration of MTJ. If the electrons go from the free layer to the reference layer, the electrons with same spin direction of the reference layer will pass the reference layer without reflection, while other electrons with different spin directions will be reflected back to the free layer. Then the magnetization of the free layer will be aligned in an anti-parallel direction to reference layer under the similar torque, as AP configuration of MTJ. This very torque is named as spin-transfer torque.

Comparing to the field-induced magnetic switching, no external magnetic field is needed for the current-induced magnetic switching as STT and the current density threshold for switching is lower than 10^7 A/cm^2. By using STT mechanism as writhing method for spin-transfer torque MRAM (STT-MRAM) with higher storage density, not only lower power consumption can be achieved, but also the writing circuit in hybrid circuit can be greatly simplified.



(a) (b)

Figure 4 Illustration of the STT effect. Writing (a) P state and (b) AP state with the STT effect.

1.4 CoFeB-MgO material system with Perpendicular Magnetic Anisotropy

Perpendicular magnetic anisotropy (PMA) is one of the key factors to achieve high performance for MTJ-based applications such as high-density nonvolatile memories and logic chips. With PMA, lower current densities can be reached together with high thermal stability. To achieve this goal, a number of material systems have been investigated, including rare-earth/transition metal alloys, Fe/Pt alloys, Co/Pd and Co/Pt multilayers [PAR08, NIS02, MIZ09, SAT12, CAR08]. However, none of those material systems could satisfy the all three conditions for high density STT-MRAM with low power at the same time, i.e. the high thermal stability at reduced dimensions, low power current-induced magnetization switching and high TMR ratio [MAN06].

In addition to PMA, TMR ratio is of importance for memory application. A higher TMR ratio means the larger sensing margin for reading operation in MRAM, and consequently higher fault tolerance. Researchers and engineers have spent much efforts in searching for proper material systems to obtain higher TMR. In 2001, first-principles calculations predicted a 1000% TMR ratio for epitaxial Fe with a crystalline MgO tunnel barrier [BUL01]. Later in 2008, a TMR of 600% at room temperature was observed for sputtered CoFeB-MgO MTJs with in-plane magnetic anisotropy [IKE08].

In 2010, Ikeda and his coworkers reported the CoFeB-MgO based MTJs with PMA [IKE10]. Those PMA-MTJs have showed a high TMR of 120%, high enough PMA for thermal stability at a dimension of 40 nm diameter, and a low switching current under STT effect. Therefore, the CoFeB-MgO material system has been proved to be an ideal choice for providing a lower Gilbert damping factor, enough magnetic anisotropy and good crystallinity, which satisfies all three conditions for high-performance perpendicular MTJs. This work is a milestone in MRAM development and after that, the efforts of research and develop (R&D) which has been devoted to MRAM begin to focus on those CoFeB-MgO based PMA-MTJs, which combining high TMR, high thermal stability and low switching current.

The magnetic anisotropy of a system is determined by the magnetic interface anisotropy energy and stray field energy. Considering the negligible strain effects, the free energy of a thin film (~ nm) can be written as:

$$E_d \approx \frac{K_s}{t_{film}} \sin^2\theta - \frac{1}{2}\mu_0 {M_s}^2 \cos^2\theta \tag{1.5}$$

In the equation (1.5), second and higher anisotropy terms have been neglected for the expression due to the small values. As the film thickness decreases, interface anisotropy begins to favor PMA. Figure 5 (a) shows the dependence of anisotropy field H_k on the thickness of CoFeB films [IKE10]. A positive value of H_k means the direction of the magnetic anisotropy is out-of-plane (e.g. PMA) and a negative value means in-plane. The CoFeB films show good PMA feature when the thickness of the CoFeB layer is below 1.5 nm. However, due to the presence of a dead layer, the PMA effect disappears when the thickness of CoFeB is below 0.5 nm.

The interface anisotropy strongly depends on the materials on both side of the CoFeB layer (e.g. MgO/CoFeB or CoFeB/Capping layer), and is very sensitive to the fabrication process (e.g. sputtering and annealing conditions) that can modify the structure of the interface (roughness, interdifusion ...). The stoichiometry of CoFeB has an influence on the PMA effect as well. The PMA decreases with the increase of the Co content over 50% [DEV13].

Another important parameter for the STT switching is the damping parameter of the CoFeB films that can be as low as 0.01 for thin film with a thickness around 1 nm, which is more than 10 time less than Co/Pt or Fe/Pt films [DEV13, LEE14, MIZ10]. The damping parameter α as a function of the CoFeB film thickness is shown in Figure 5 (b) [IKE10]. Similar to the PMA, the damping factor α decreases with the increasing of Co element [DEV13].

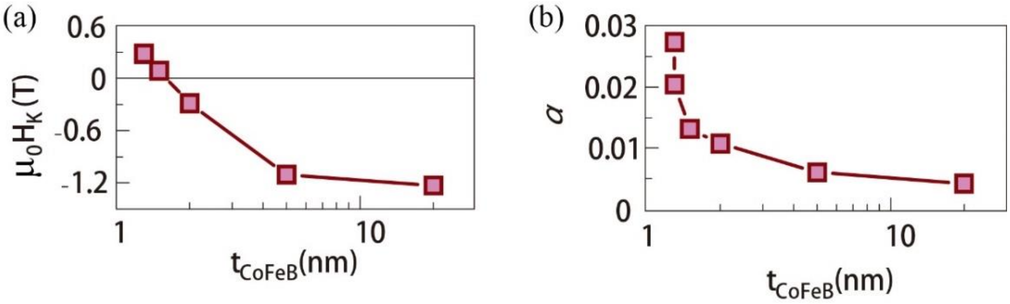


Figure 5 (a) Anisotropy field H_k and (b) damping factor α as a function of the CoFeB thickness. Figures are reproduced from Ikeda et al. [IKE10].

1.5 MTJ-based applications

Magnetic tunnel junctions have the advantages of low power consumption, unlimited endurance and fast access speed, which make it an ideal device to develop the next generation of storage and computing system. In this section, we introduce MRAM and a novel non-von Neumann architecture device for applications as logic-in-memory.

1.5.1 Magnetic random access memory

Static random access memory (SRAM) and dynamic random access memory (DRAM) are two conventional memories based on CMOS technologies. However, the increasing leakage current becomes a serious problem as scaling down into nanoscale. MRAM is a promising non-volatile memory based on the integration of MTJ and CMOS technology, which have been attracted much attention for its low standby power, excellent scalability, fast access speed and high endurance.

The first generation of MRAM is based on field-induced magnetic switching (FIMS) and the first commercial product is the Toggle-MRAM commercialized by Everspin

Company. The following generation of MRAM is the STT-MRAM, which gets rid of the external magnetic field for higher storage density and lower power consumption. More details and the comparison of key features of the emerging memory technologies have been commented by several papers. Table 1 [KEN15] indicates that SRAMs have fast access speed, however, the cell area is large and more static power consumption is needed due to the leakage current. Compared to SRAMs, DRAMs have simpler cell structure of one transistor and one capacitor but have lower access speed and need to be refreshed for data retention. MRAMs combine the non-volatility, unlimited endurance (> 10^{15} cycles) and fast access speed, which make it an ideal candidate for computing memory.

Table 1 Comparison of key features of existing and emerging memories

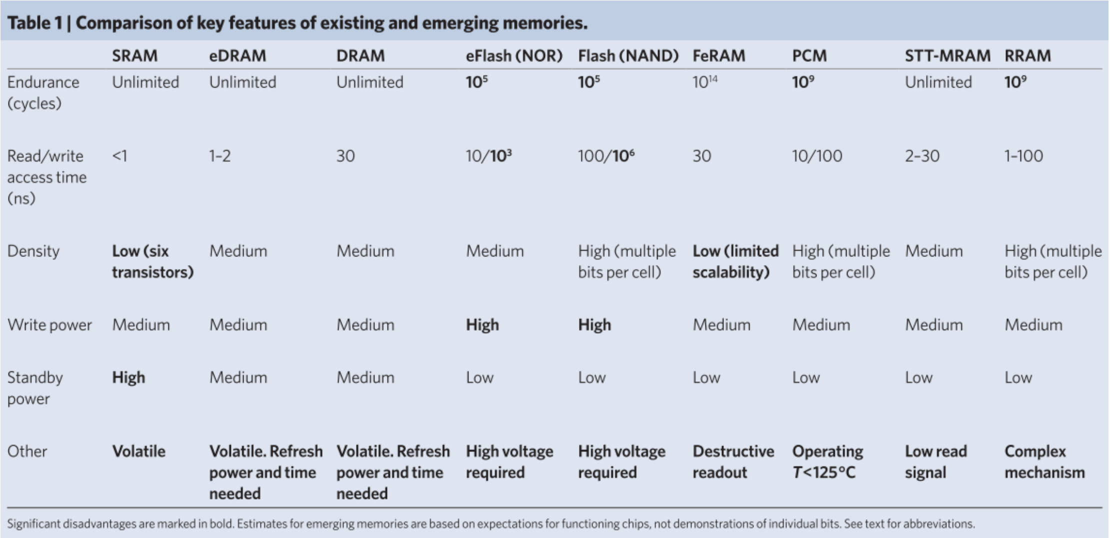


Table 1 | Comparison of key features of existing and emerging memories.

	SRAM	eDRAM	DRAM	eFlash (NOR)	Flash (NAND)	FeRAM	PCM	STT-MRAM	RRAM
Endurance (cycles)	Unlimited	Unlimited	Unlimited	**10^5**	**10^5**	10^{14}	**10^9**	Unlimited	**10^9**
Read/write access time (ns)	<1	1–2	30	10/**10^3**	100/**10^6**	30	10/100	2–30	1–100
Density	**Low (six transistors)**	Medium	Medium	Medium	High (multiple bits per cell)	**Low (limited scalability)**	High (multiple bits per cell)	Medium	High (multiple bits per cell)
Write power	Medium	Medium	Medium	**High**	**High**	Medium	Medium	Medium	Medium
Standby power	**High**	Medium	Medium	Low	Low	Low	Low	Low	Low
Other	**Volatile**	**Volatile. Refresh power and time needed**	**Volatile. Refresh power and time needed**	**High voltage required**	**High voltage required**	**Destructive readout**	**Operating T<125°C**	**Low read signal**	**Complex mechanism**

Significant disadvantages are marked in bold. Estimates for emerging memories are based on expectations for functioning chips, not demonstrations of individual bits. See text for abbreviations.

Two other emerging non-volatile technologies, i.e resistive RAM (RRAM) and phase change memory (PCM), are currently attracting interest in terms of reaching higher density for applications to storage class memory (SCM), which is a new class of memory in the hierarchy between Flash and DRAM. In particular, Intel/Micron are going to commercialize 3D/X-point memories based on PCM in 2018 with the same density as Flash but much faster (x1000).

Figure 6 shows the conventional memory hierarchy of modern computing system. Memories in each level have different speed and capacity: the memory in lower level has lower access speed but larger capacity. DRAM and Flash serve as the main memory and disk, respectively. SRAM is used for constructing the cache due to its fast access speed. We note that Level-2 (L2) and Level-3 (L3) cache has a larger capacity than Level-1 (L1) cache. Actually, most of the power consumption due to the leakage current in SRAM cache memory of L2 and L3 are standby power rather than active power in L1. Therefore, a possible solution for building the low power processor is to use the MRAM to replace SRAM and DRAM for the main memory and L2 and L3 cache memory [SEN15].

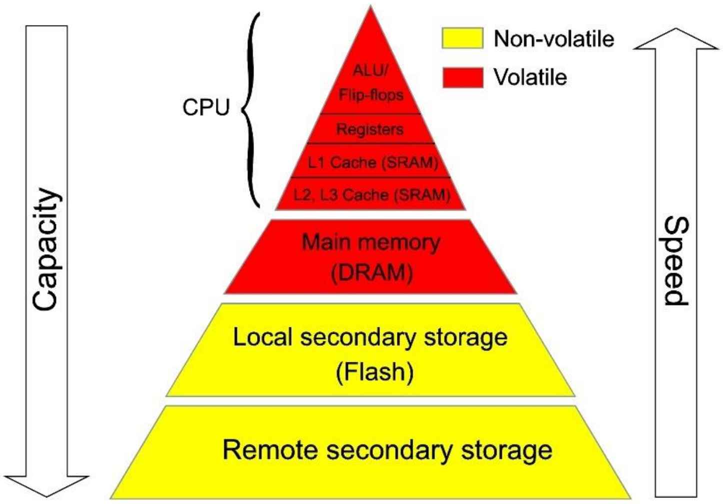


Figure 6 Memory hierarchy of the modern computing system

1.5.2 Logic-in-memory

Nowadays, the modern computing systems are based on the von-Neumann architecture, in which the logic and memory are separated and connected by interconnections for data transferring [BUR82]. The relative long distance between the logic and memory function units results in a long transfer delay (and lower operation speed) and high transfer power dissipation. When scaling down to lower technology nodes, more interconnections are needed along with the increasing complexity of integrated circuit (IC) design. Furthermore, considering of the standby power consumption due to leakage current in CMOS technologies, the reduction of the interconnection delay and the static/dynamic power becomes a major object for the next generation computing system with ultra-low power consumption.

In order to break the bottleneck of von-Neumann architecture, logic-in-memory device has attracted extensive attention in the past decades. The concept of logic-in-memory was first proposed by Kautz in 1969 [KAU], that each cellar array has combined the memory with the logic function, as shown in Figure 7. The emerging non-volatile memory technologies are very suitable for constructing the logic-in-memory device for the following two reasons: Firstly, the logic and storage functions can be accomplished in the same device structure [ZHA14], which means the logic and storage can be combined spatially. Secondly, thanks to the non-volatility, the data can be kept in the storage block without any standby power consumption. Furthermore, the data can be instantaneously retrieved from the standby state and continue for computing, which is the basic idea of normally-off and instant-on computers [BOR10, SHU17].

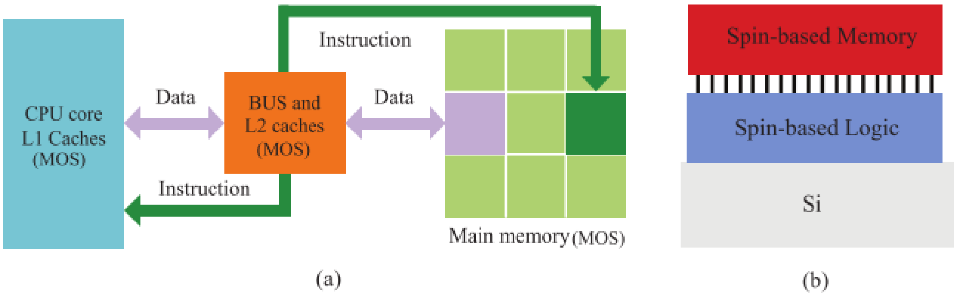


Figure 7 Different architectures for storage and computing systems. (a) Conventional von Neumann architecture with separated logic and memory function units. (b) 3D logic-in-memory structure using spin-based devices. Figures are reproduced from Zhang et al. [ZHA14].

1.6 Summary

In this chapter, we have overviewed a few general concepts of spintronics. In particular, we have highlighted the importance of CoFeB-MgO materials in spintronics, a system that can reach high thermal stability using PMA, high TMR ratio or a low Gilbert damping factor. By utilizing MTJ devices, advanced memories and logic-in-memory devices can be accomplished, which provides a possible way to construct the next generation of ultra-low power computing systems and break the bottleneck of von-Neumann architecture.

CHAPTER 2 MATERIALS GROWTH AND NANOFABRICATION

With the development of Nanoscience and Nanotechnology based on complex and expensive equipment, CMOS devices have scaled into the nanoscale. Along this line, the fabrication of magnetic nanodevices have benefit from the techniques developed by the semiconductor industry and nowadays typical sub-20 nm STT-MRAM devices can be fabricated in advanced R&D laboratories. In this chapter, we will introduce the full fabrication flow of two typical magnetic devices based on CoFeB-MgO material system, e.g. MTJ nanopillars and magnetic nanodots.

2.1 Process flow for Magnetic dots

2.1.1 Growth of Ta-CoFeB-MgO layers

For the magnetic nanodots, we have used the typical free layer of optimized MTJs. It consists in Ta(5 nm)/CuN(40 nm)/Ta(5 nm)/$Co_{40}Fe_{40}B_{20}$(1.1 nm)/MgO(1 nm)/Ta(5 nm) multilayers grown by a Singulus TIMARIS sputtering tool on 100-mm Si/SiO_2 wafers. After the deposition, the samples were annealed in high vacuum at 380 °C for 20 minutes in order to get the crystalline phase. The magnetic properties of the films were studied by using a MicroSense vibrating sample magnetometer (VSM) system.

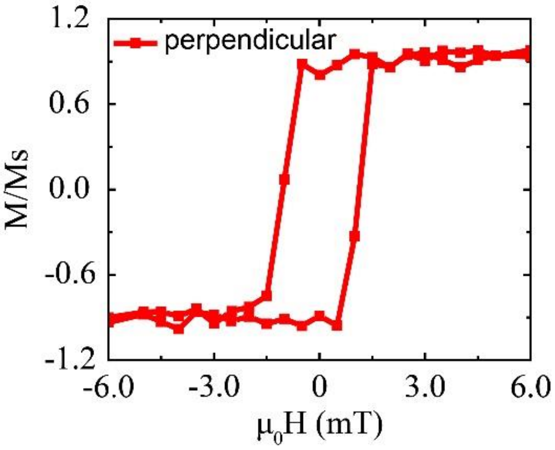


Figure 8 Hysteresis loops of the Ta(5 nm)/CuN(40 nm)/Ta(5 nm)/$Co_{40}Fe_{40}B_{20}$(1.1 nm)/MgO(1 nm)/Ta(5 nm) multilayers

The hysteresis loop of the full films seen in Figure 8 indicates PMA, with a typical low coercivity of the CoFeB layer of $\mu_0 H_c = 1$ mT, as we have shown in our previous study [BUR13]. The value of the effective anisotropy of the film is found to be $K_{eff} = 1.3\times10^5$ J/m^3 and the saturation magnetization is $M_s = 1.3\times10^6$ A/m, as measured by VSM using in-plane magnetic fields.

2.1.2 Nanofabrication of magnetic dots

Figure 9 shows the full fabrication process flow of magnetic nanodots that I have developed during my PhD research.

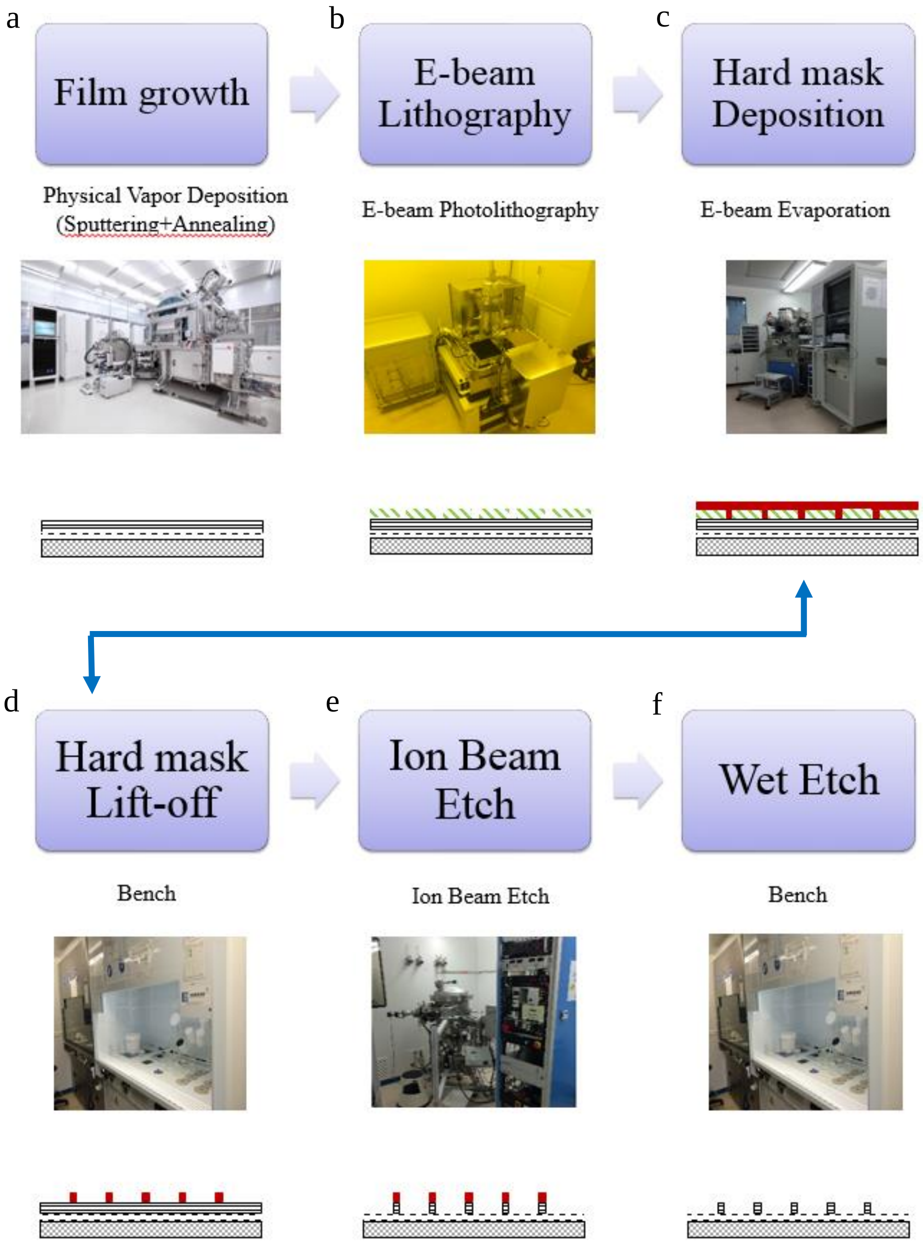


Figure 9 Process flow for the fabrication of magnetic nanodots

Nanodots with sizes ranging from 400 nm to 1 μm are fabricated using a lift-off process based on an Al hard mask. First, after spin coating the PMMA950A4 resist with a thickness of 200 nm, electron beam lithography (EBL) with 80 keV electrons is used to define the squared dots (step b). Subsequently, a 50-nm-thick Al mask is deposited by electron beam evaporation (step c). The resist is removed in 1165 solvent (step d) and then an ion milling process with Ar ions (etching angle of 45°) is used to etch the magnetic layers down to the CuN buffer layer using a secondary ion mass spectroscopy (SIMS) for the end point detection (step e). The final process is the removal of the Al mask by a wet etch process using a specific MF-CD-26 developer (step f). Figure 10 shows the typical high quality nanodots with vertical edges fabricated by this process.

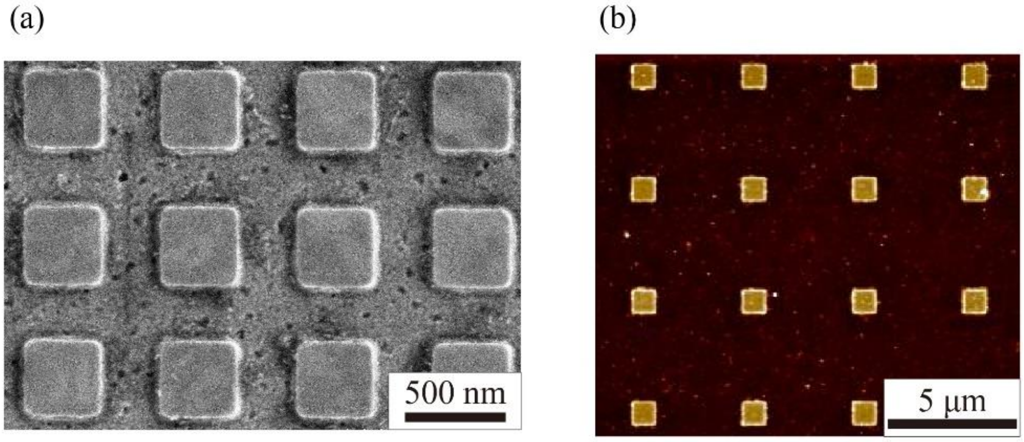


Figure 10 The profile of a nanodot array. (a) SEM image of 400 nm nanodots (b) AFM image of 1 μm nanodots

2.2 Process flow for MTJ nanopillars

2.2.1 Growth of CoFeB-MgO based magnetic tunnel junction

The magnetic multilayers are deposited onto SiO_2-coated Si wafers using a combination of radio frequency (RF) and direct current (DC) sputtering in a Canon-Anelva system. From the substrate side, the MTJ structure consists of the following layers (the numbers are the nominal thicknesses in nanometers):

Ta(5)/Ru(15)/Ta(5)/Ru(15)/Ta(5)/Ru(5)/PtMn(20)/CoFeB(1.5)/CoFe(2.0)/Ru(0.85)/CoFeB(1.5)/CoFe(1.5)/MgO(0.8)/CoFe(1.5)/CoFeB(1.5)/Ru(2)/Ta(5)/Ru(10)

The bottom and top layers, Ta(5 nm)/Ru(15 nm)/Ta(5 nm)/Ru(15 nm)/Ta(5 nm)/Ru(5 nm) and Ru(2 nm)/Ta(5 nm)/Ru(10 nm), respectively, are designed for the Current-in-plane tunneling (CIPT) measurements using a CAPRES microprobe tool. The typical TMR ratio and the RA product of the unpatterned films are ~ 144% and =19 ohm·µm^2, respectively. An annealing process is performed at 350°C for 1 hour with an in-plane magnetic field of 1 T under a vacuum of 10^{-6} Torr.

After the annealing, the magnetization curves are measured by VSM at room temperature. The free layer (CoFe(1.5 nm)/CoFeB(1.5 nm)), reference layer (CoFeB(1.5 nm)/CoFe(1.5 nm)) and pinned layer (CoFeB(1.5 nm)/CoFe(2.0 nm)) can be observed from the hysteresis loop under in-plane magnetic fields, as shown in Figure 11.

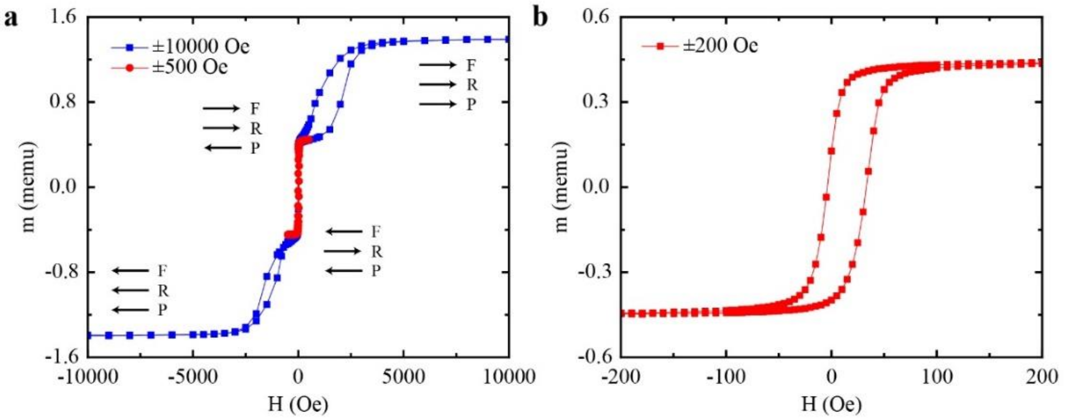


Figure 11 (a) In-plane magnetization hysteresis loops of the MTJ stack. The magnetic configuration of the free (F), reference (R) and pinned (P) layers are indicated by arrows. (b) Minor loop corresponding to the switching of the free layer.

The presence of a good crystalline structure of the CoFe(B) and MgO layers, e.g. body-centered cubic (bcc) (001) and NaCl-structure respectively, is crucial for obtaining a high TMR ratio [YUA07]. As shown in Figure 12, the cross-sectional high resolution transmission electron microscopy (HRTEM) have been performed to characterize the lattice structure of the MTJ stack. The free layer (CoFe(B)), tunnel barrier (MgO), synthetic ferri-magnetic (SyF) reference layer (CoFe(B)/Ru/CoFe(B)) and anti-ferromagnetic layer PtMn are indicated. A crystalline structure can be observed for both CoFe(B) and MgO layers.

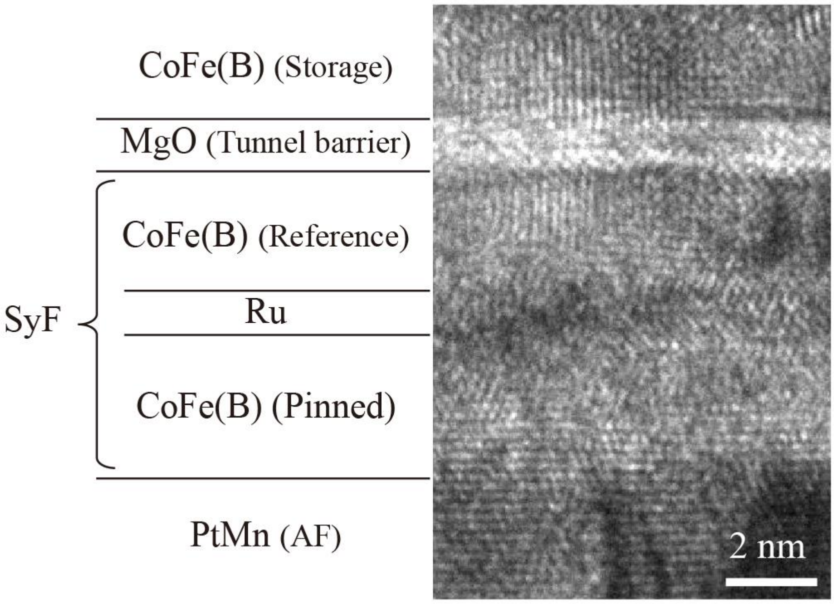


Figure 12 Cross-sectional TEM of magnetic multilayers in CoFe(B)-MgO based MTJ

In order to further investigate the crystalline structure for both CoFe(B) and MgO layers, fast Fourier transformation (FFT) have been performed for diffraction patterns, as shown in Figure 13. Four diffraction points in the top CoFe(B) layer can be observed in FFT diffraction images (see Figure 13 (b)), indicating a bcc structure of CoFe(B) [NAG06]. However, different lattice directions are also observed in the bottom CoFe(B) layer (see Figure 13 (f)) and MgO layers (see Figure 13 (d)). These twisted crystalline structures are possibly induced during the preparation process of TEM samples.

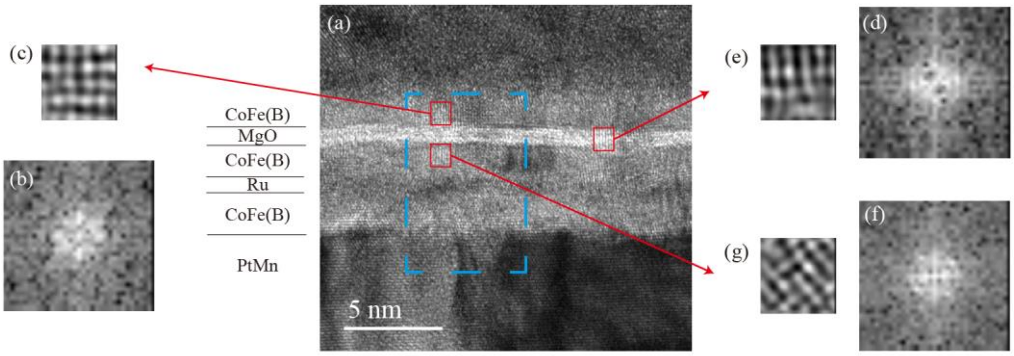


Figure 13 The crystalline structure analysis of the MgO and CoFe(B) layers of MTJ. The region in Figure 12 is marked by a blue dash rectangle. The original image (a) were firstly processed by a Gaussian filter (not showed), and then the fast Fourier transformation diffraction patterns (b, d, f) were obtained and finally, the crystalline lattice patterns (c, e, g) after the inversed FFT.

2.2.2 Nanofabrication process of MTJ nanopillars

The MTJ fabrication process can be divided into three different parts: MTJ lithography, MTJ etching and MTJ encapsulation. The typical process including these three important parts is described as following: submicron-sized ellipses are obtained using EBL process with a ZEP520A positive resist on top of a 150 nm Ta layer, followed by Pt evaporation and a lift-off process. Then the Pt patterns are used as a protective mask to etch down the 150 nm Ta layer using inductively coupled plasma (ICP). After that, the Ta patterns are used as a hard mask to etch down the magnetic multilayers using an optimized ion beam etching (IBE) process to avoid sidewall redisposition. A VM652 promoter and an Accuflo T-25 Spin-on Polymer (produced by Honeywell [HUA11]) are then sequentially spin coated, followed by a low-temperature curing process (below 300°C) for encapsulating the patterned structure in the SiO_x-based materials. The encapsulation layer is patterned into 40×60 μm^2 elements using ICP. Finally, Cr/Au top electrodes are fabricated utilizing a lift-off approach. The schematic of the final device is shown in Figure 14.

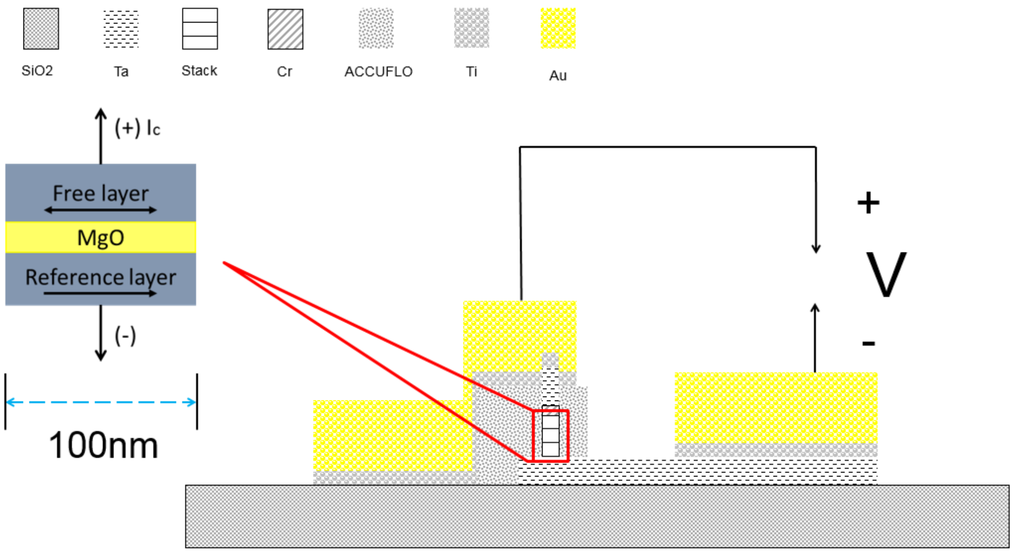


Figure 14 Schematic of the final MTJ device

Below, we give more details of the description in each step and the issues we have faced to develop this full process. All the process steps of the MTJ nanopillars are listed below:

1. A Ta layer with a thickness of 80 nm is deposited by sputtering onto the top of magnetic multilayers as a hard mask. (step c)

2. Alignment marks for the EBL process are realized. Here, a lift-off process is involved, including optical lithography with positive photoresist AZ5214, metal e-beam evaporation of Ti/Au and lift-off with Acetone. (step d-f)

3. Once the EBL alignment marks are done, a second lift-off process is involved, including EBL of 80 keV electrons with positive e-beam resist ZEP520A of a thickness of 400 nm, metal Pt e-beam evaporation with a thickness of 80 nm and lift-off with a Butanone. After those steps, the pattern (the shape of nanopillar) has been transferred to the hard Pt mask. (step g-i)

4. ICP dry etching with a mixture of SF_6 and Ar is used to etch the Ta mask using the hard Pt mask. In this step, the pattern (the shape of nanopillar) is transferred to the Ta mask. (step j)

5. IBE dry etching with 45° is used to etch the magnetic multilayers using the Ta mask. The etching stops at the seed layer of the MTJ stack (e.g. Ta/Ru/Ta). In this step, the pattern (the shape of nanopillar) is transferred to the magnetic multilayers. (step k)

6. Definition of the pattern of the bottom electrode, including the optical lithography with AZ5214 resist and the following IBE dry etching with 45°. The etching stops in the SiO_2 substrate. (step l-m)

7. Resist removal, including an ICP dry etch with O_2 and a wet etch with 1165 solvent. After this step, the MTJ nanopillar will be exposed to O_2. (step n-o)

8. MTJ encapsulation, including spin-coating VM652/Accuflo and low-temperature curing process below 300 ºC. (step p)

9. Definition of the pattern for the encapsulation layer, including the optical lithography with AZ5214 resist and the following ICP dry etch with a mixture of O_2 and Ar. Then the resist is removed by wet etching in Acetone. (step q-s)

10. Fabrication of the top contact. First, the top Ta mask is opened by etching the encapsulation layer with ICP dry etch with a mixture of O_2 and Ar (step t). Then the top electrode is fabricated. Here, a lift-off process is involved, including optical

lithography with positive photoresist with AZ5214 resist, metal e-beam evaporation of Ti/Au and lift-off with Acetone. (step v-w)

Figure 15 gives the fabrication flow of the MTJ nanopillar as described above.

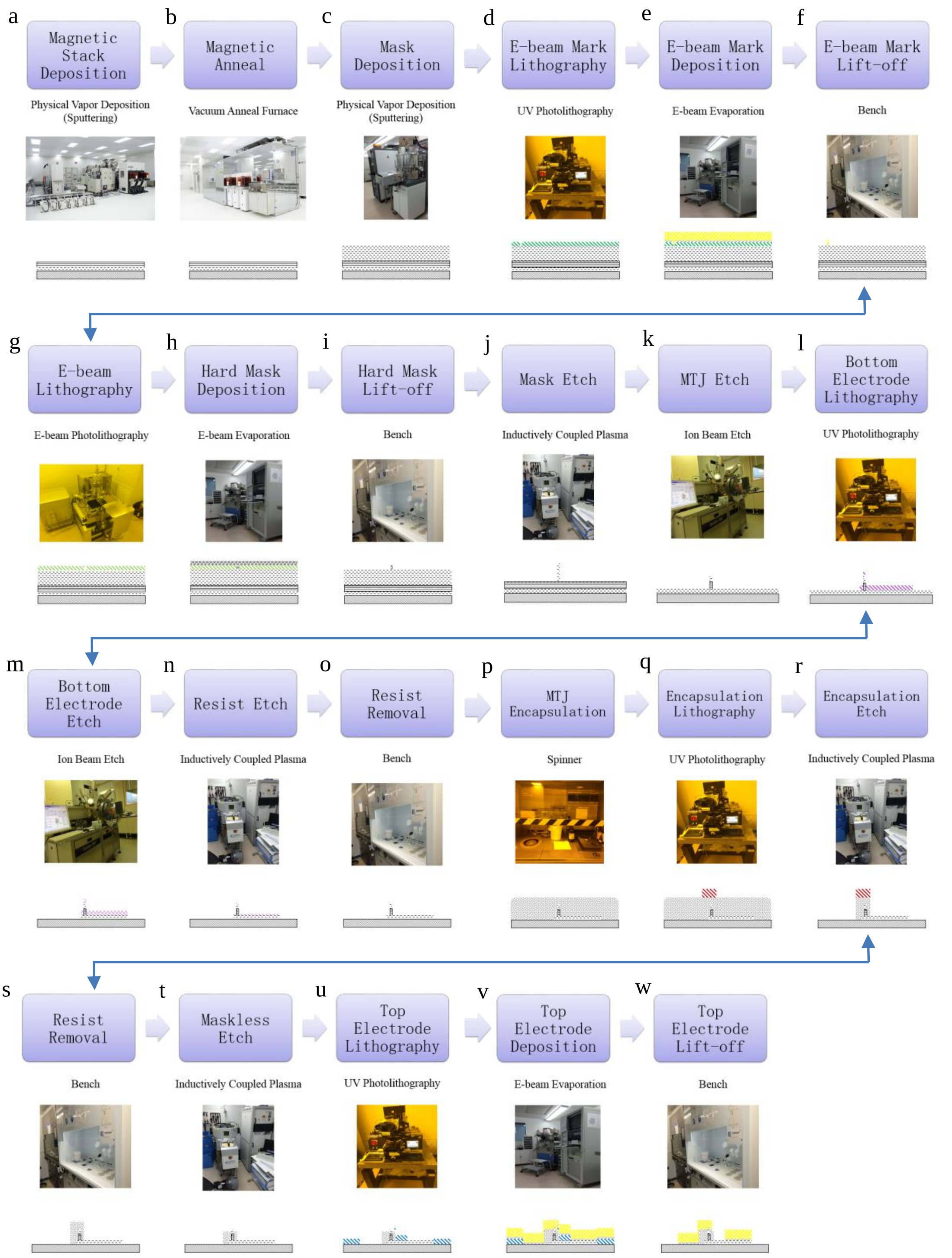


Figure 15 Process flow for the fabrication of MTJ nanopillar

2.2.2.1 MTJ lithography

Five levels of lithography are needed for the full process: one level for the EBL process and four levels of optical lithography for the alignment marks, bottom/top electrodes and encapsulation layer. The layouts, e.g. photomasks, for the optical lithography are showed in Figure 16.

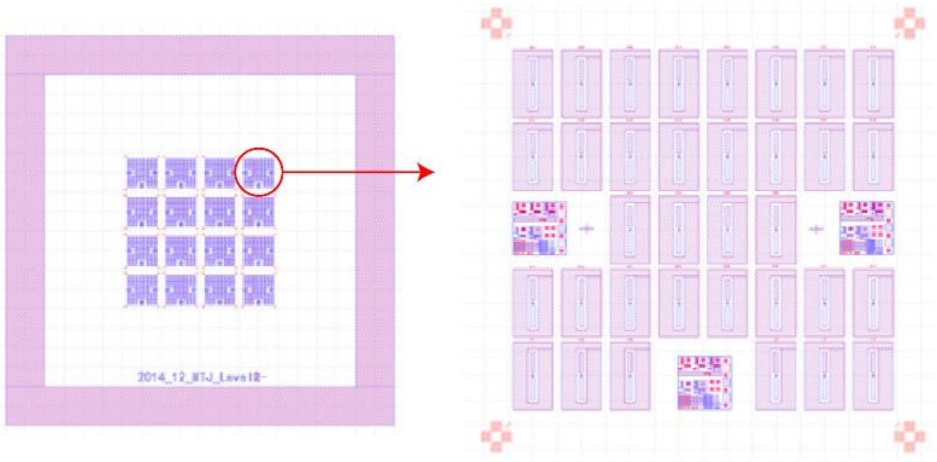


Figure 16 Layout of the photomasks for MTJs

The photomasks are designed for 4-inch wafer but they are also compatible with 1cm×1cm or 2cm×2cm samples. The details for the shape and relative location of the three-level (e.g. bottom electrode, top electrode and encapsulation layer) photomask layouts are presented in Figure 17. The MTJ nanopillar is located at the narrow constriction of the bottom electrode and it is encapsulated with the Accuflo.

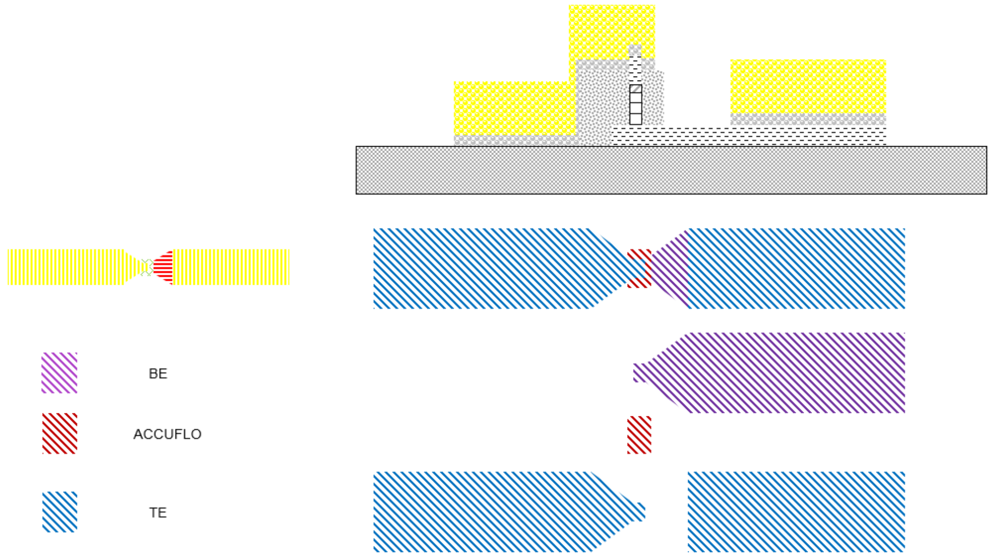


Figure 17 Layout of a single MTJ cell. “BE” represents the “Bottom Electrode”, “TE” represents the “Top Electrode” and “ACCUFLO” represents the encapsulation layer.

Figure 18 shows the top view of a fabricated MTJ device under SEM. The bottom electrode, top electrode, MTJ nanopillar and encapsulation layer are indicated.

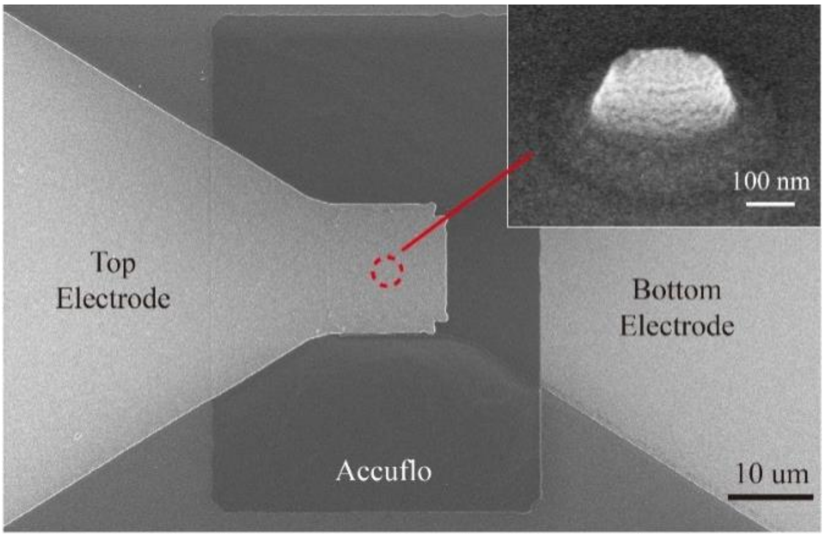


Figure 18 Top view of MTJ device under SEM. The red dash circle marks the location of a MTJ nanopillar and the inset image shows the nanopillar under a tilt view of 45 degree.

2.2.2.2 MTJ etch

The etching of MTJ is the most difficult and crucial step, which directly determines the profile and performance of the device. In this section, several important points are highlighted and discussed.

① Use of IBE to etch the MTJ

Since the FM layer, e.g. CoFeB, is very sensitive to the oxygen and halogen elements (F and C based compounds), the IBE method is more suitable than ICP for etching the core structure of the MTJ stack, e.g. CoFe(B)/MgO/CoFe(B).

② The use of a hard Ta mask for the IBE process

Since a vertical current has to flow through the nanopillar and an e-beam resist mask is very difficult to remove after IBE, we have developed a process based on a Ta mask, for which the etching rate is quite low in the milling process.

③ Use of a hard Pt mask to etch the Ta layer

As discussed above, a Ta mask is needed to etch the nanopillar. Furthermore, in order to pattern the Ta layer with the shape of nanopillar, an additional metallic hard mask is needed. For that, a lift-off process is used involving the EBL with positive resist followed by the deposition of a metallic layer as hard mask. There is a trade-off in the resist thickness: the metallic hard mask should be sufficient thick for the etching process, however, the e-beam resist should be sufficient thin for a better EBL resolution. The best compromise we have found is to use a positive e-beam resist with high resolution (ZEP520A). Due to the high etching selectivity ratio, Pt has been chosen as the hard mask for etching the Ta using ICP.

④ Use of SF_6 and Ar to etch the Pt layer using a ICP process

For ICP, there are two etching processes involved. The first one is physical etching, based on Ar ions. The second process is chemical etching, which originates from the chemical interaction between a reactive gas of ions and the layer to be etched. A failure for using the improper parameters (pressure, gas flow rate, acceleration voltage …) will lead to a low etch selectivity and a bad device profile. In other words, a right combination of physical and chemical etching is expected.

In order to improve the ICP process, up to 8 different recipes have been tested on more than 10 samples. The SEM image of the etched MTJ nanopillar under the best recipe (the etching duration is 46 minutes) has been shown in Figure 19 (a) and a very good vertical profile has been achieved. A clear interface between the Pt and Ta masks can be observed in Figure 19 (b) for larger patterns as dummy (used for checking the patterns).

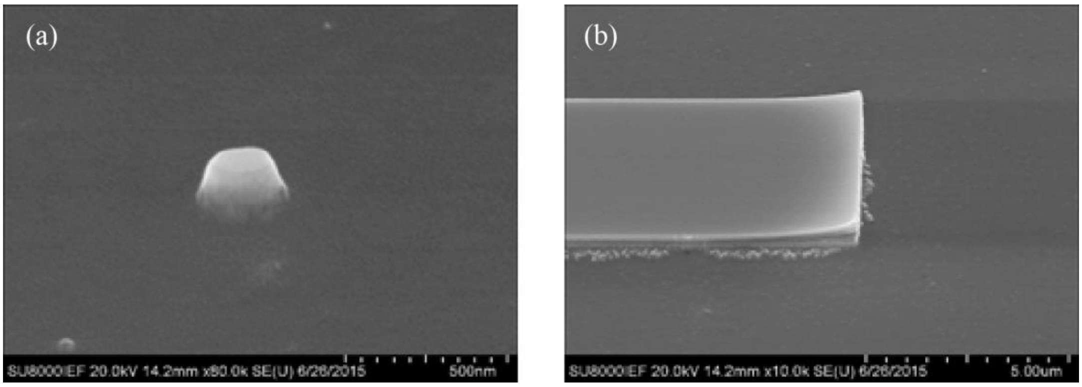


Figure 19 A good profile of the metallic hard mask (Pt and Ta) nanopillar is shown in (a). A clear interface of Pt and Ta layers is shown in (b) for larger patterns.

It needs to be noted that the etching process described above is discontinuous in the sense that we have used 6 periods of etching with idle time in between. If we do a continuous etching for the same duration (e.g. 46 minutes), a ring appears at the bottom of the nanopillar (see Figure 20), which can be due to an over physical etching.

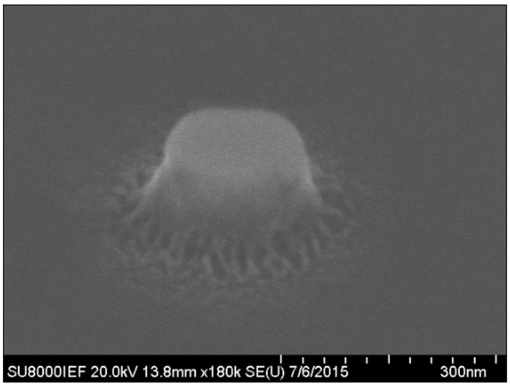


Figure 20 SEM image of the metallic hard mask (Pt and Ta) nanopillar after a continuous ICP process (e.g. 46 minutes).

We have found that a heating process involved in the physical etching can explain this result. By lowering down the etching power, a very good metallic hard mask (Pt and Ta) profile and a very good etching selectivity (between Pt and Ta) can be obtained again, as shown in Figure 21.

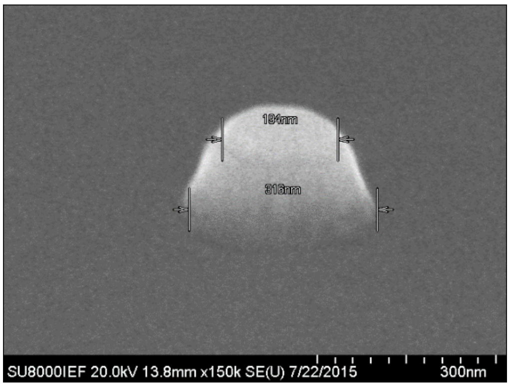


Figure 21 SEM image of the metallic hard mask (Pt and Ta) nanopillar after ICP etching

⑤ IBE etching of the MTJ stack using the Ta mask

As we have mentioned at the beginning of this section, we use IBE to etch the MTJ stack. The screenshot of the SIMS measurement for the end-point detection (see Figure 22) indicates that the etching stops at the top Ta layer of the bottom electrode.

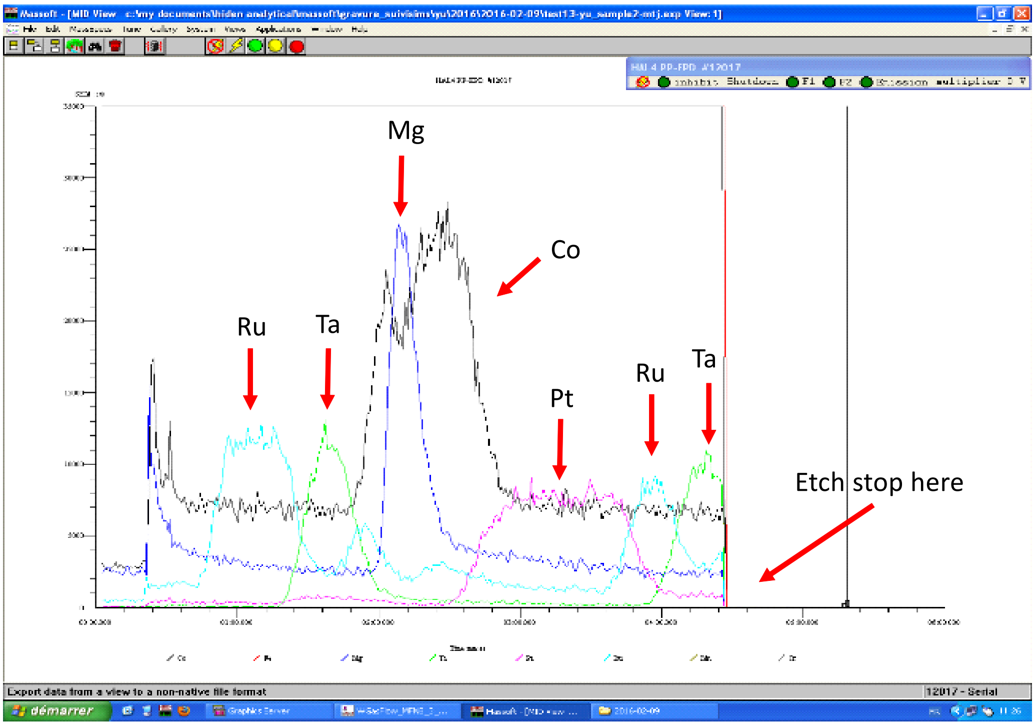


Figure 22 SIMS measurement for the IBE process of the MTJ stack

The IBE process is done at 45° to minimize the redeposition on the sidewall of the MTJ nanopillar [SUG09, PRE15], as shown in Figure 23.

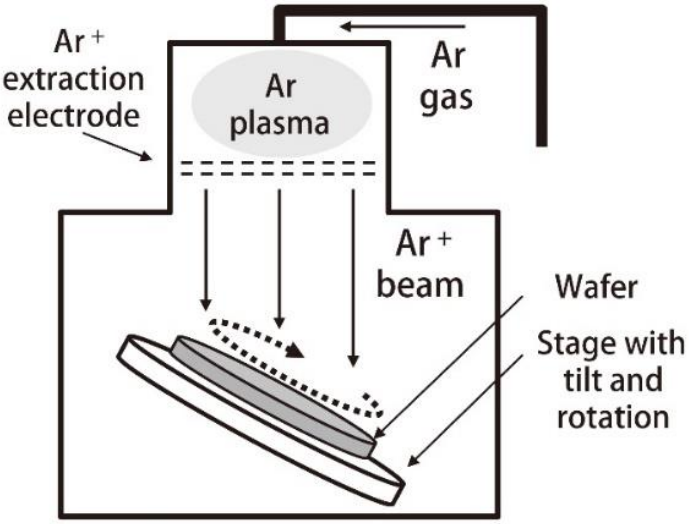


Figure 23 Schematic drawing of the IBE process used here. The figure is reproduced from Sugiura et al. [SUG09]

The SEM images of the MTJ nanopillars with 15° and 45° IBE angles are presented in Figure 24 (a) and (b), respectively. A clear tail at the bottom of the nanopillar is shown only for 45° (see Figure 24 (b)), which is due to the shadow effect in IBE [SUG09]. Decreasing the etching angle to 15° helps to reduce the tail, as shown in Figure 24 (a);

however, the later transport measurement for the fabricated MTJ devices shows an electrical short-cut, which indicates a redeposition on the sidewall [PEN09]. We note that the existence of redeposition can be further confirmed by the TEM check with very high resolution on the sidewall of MTJ [PEN09]. Although a multi-step etch strategy could be utilized to eliminate the tails [CHU12], we used 45° as the etching angle in IBE.

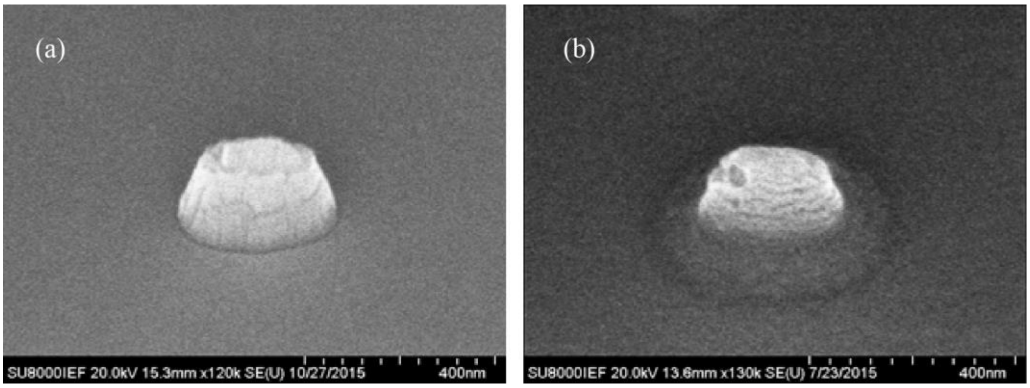


Figure 24 SEM image of the MTJ nanopillar after IBE with different etch angles. The etch angle for (a) and (b) are 15° and 45° respectively.

Figure 25 shows a MTJ nanopillar after IBE with an etch angle of 45°. The size of the nanopillar is around 100 nm and the sidewall is vertical. The cylinder on the top is the left Ta mask and the circular shape below is the MTJ stack. The dimension of the tail here is around 400 nm, which indicates the limitation for high density nanopillars using IBE techniques [PRE15].

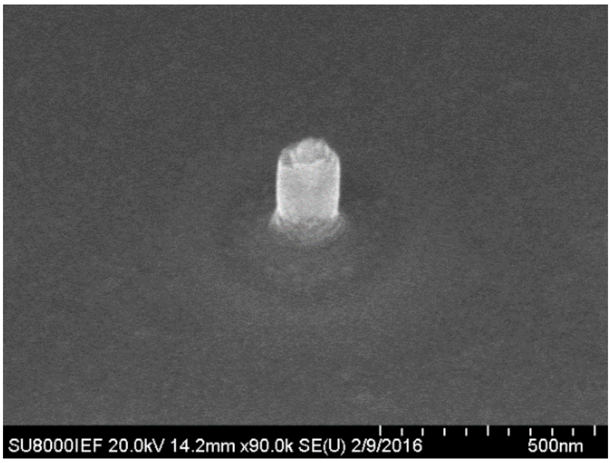


Figure 25 SEM image of a nanopillar using an IBE angle of 45°

2.2.2.3 MTJ encapsulation

In order to protect the nanopillars from oxidation, to insure electrical insulation and to maintain the mechanical stiffness of the nanopillars, an encapsulation matrix is necessary. In the semiconductor industry, SiO_2 and SiN are widely used as encapsulation material due to their good electrical insulation and thermal stability. Both sputtering and plasma enhanced chemical vapor deposition (PECVD) can be used for depositing such materials, however, either an etch-back process or a chemical mechanical polishing (CMP) process is needed for the later step of electrodes contact.

Another possible solution is the utilization of a spin-on glass. As a method of planarization, the use of spin-on glass gets rid of the extra step of dry etching or CMP process. Due to the liquid feature of spin-on glass, it can be spun off on the sample surface and then turns into SiO-based material using a curing process. Figure 26 shows the results of electron energy loss spectroscopy (EELS) mapping for the spin-on polymer Accuflo provided by the Honeywell Company that we have used in our process. The exact details of molecular formula is unknown, however, the carbon, oxygen and silicon elements are detected from the EELS measurement.

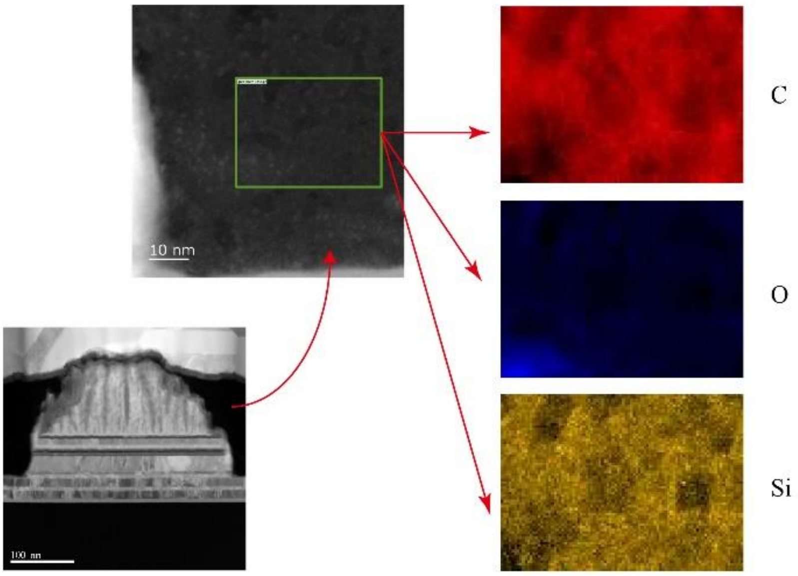


Figure 26 Element analysis of the spin-on polymer Accuflo. The region for EELS testing is marked by a green rectangle in STEM image obtained by a high-angle annular dark field (HAADF) detector. The EELS mapping indicates the existence of carbon, oxygen and silicon elements in Accuflo.

For the MTJ encapsulation, it is important to use a curing temperature below 300°C to avoid any further annealing of the magnetic multilayers, which may lead to a degradation of the TMR ratio [PRE15, LEE07, IKE08, JAN11]. It is also necessary to pattern the encapsulation layer into micro-sized rectangle. The purpose for the patterning is to minimize the effect of capacitance. As shown in Figure 14, metal-insulator-metal (MIM) structure including the top electrode, the bottom electrode and the encapsulation layer in between, is similar to a plate capacitance. By decreasing the area of the encapsulation layer, the capacitance can be reduced. Figure 27 shows the patterned encapsulation layer. A small dot well encapsulated in the Accuflo can be observed at the extremity of the bottom electrode, which is actually the MTJ nanopillar (see Figure 27 (a)).

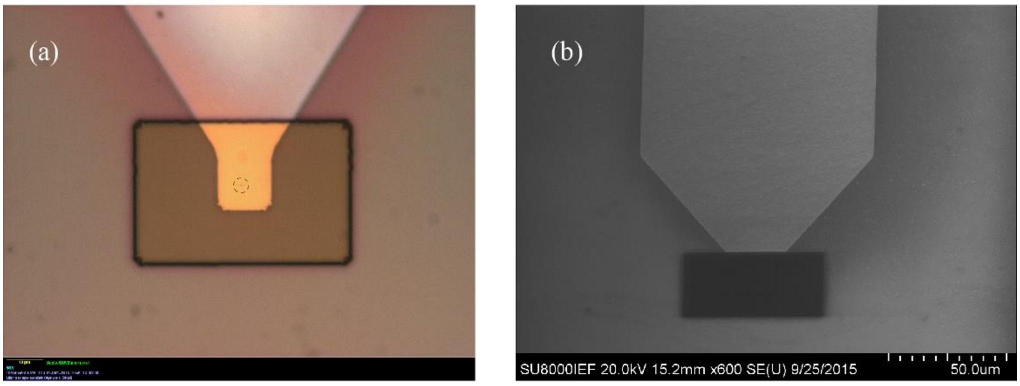


Figure 27 Images of the encapsulation layer after patterning under (a) optical microscope and (b) SEM .The dash circle marks the location of the nanopillar.

After the patterning process, the thickness of the encapsulation layer needs to be reduced by ICP dry etch down to the top of the Ta mask, as shown in Figure 28. Figure 28 (b) shows clearly that the top of the Ta mask has been opened and is ready for the later step of depositing the Au electrode.

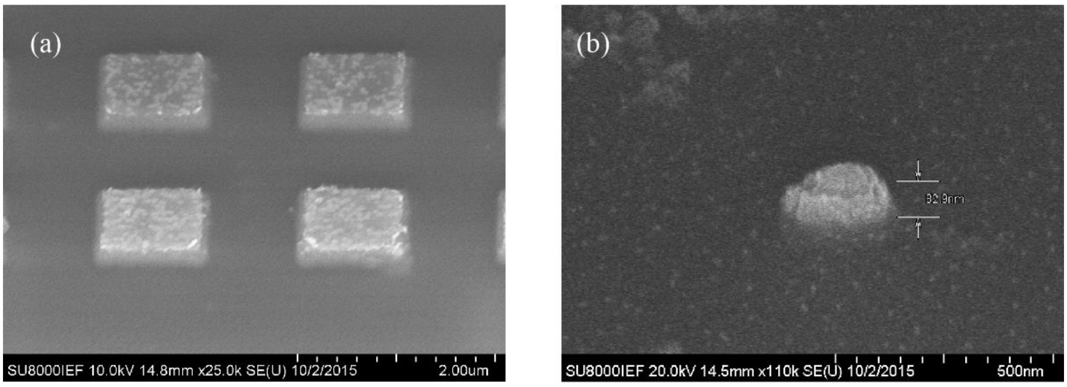


Figure 28 SEM images of the (a) square of dummy (used for checking the patterns) and (b) the top of Ta nanopillar after the process of etching down the encapsulation layer by ICP.

Finally, the cross-sectional TEM images of the fabricated MTJ devices with the top electrode are presented in the Figure 29.

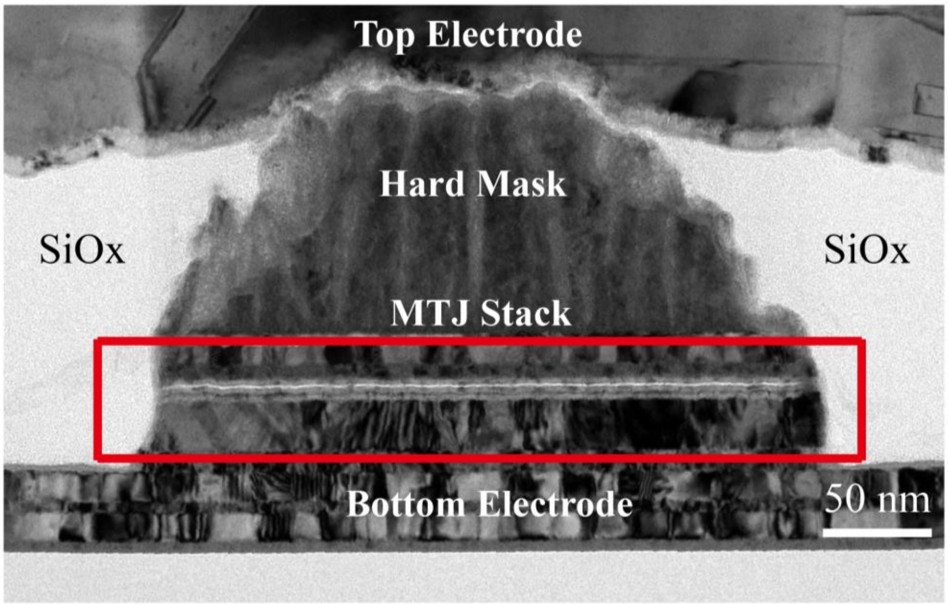


Figure 29 Cross-sectional TEM images of the MTJ nanopillar with a size of 80nm×200nm

2.3 Summary

In this section, we have discussed about the nanofabrication process flow of two magnetic devices, e.g. magnetic nanodots down to 400 nm and MTJ nanopillars down to 100 nm. For the magnetic nanodots, a process based on IBE through an Al mask followed by a wet etch of the mask has been developed. For MTJ nanopillar, we have shown that crucial steps include the optimization of the etching process using both ICP and IBE with Ta and Pt hard masks, as well as the encapsulation process with a low-temperature curing for encapsulation layer Accuflo and an ICP process to open the top contact. In the next two chapters, we are going to study the switching process in these devices, i.e, field-induced switching in nanodots with PMA and current-induced switching in the MTJ nanopillars with in-plane magnetization.

CHAPTER 3 MAGNETIZATION REVERSAL OF NANODOTS GOVERNED BY LAPLACE PRESSURE

In this chapter, we study the magnetization reversal of CoFeB-MgO nanodots with perpendicular anisotropy under magnetic field for sizes ranging from w=400 nm to 1 μm. We show that contrary to previous experiments for patterned media, the switching field distribution (SFD) is shifted toward lower magnetic fields as the size of the elements is reduced with a mean switching field varying as 1/w. We demonstrate that this mechanism can be explained by the nucleation of a magnetic domain wall (DW) at the edges of the nanodots where damages are introduced by the patterning process followed by a DW depinning process.

3.1 Magnetic reversal mechanism

Magnetic nanostructures based on PMA [HEL17] materials are attracting a large amount of attention for their potential applications including high-density MRAM [IKE10, KEN15], bit patterned media [OCON10, ALB15], or magnetic logic [TOR17]. The scalability of these applications toward ultimate technology nodes is in general limited by the structural variability of the nanostructures. This leads to a dispersion of the magnetic properties, which strongly affects the switching mechanism when the dimension of the nanostructures becomes smaller. In particular, this has been extensively shown for the switching process of magnetic dots [HUG05, THO06, SHA08, OKA12, SUT16]. When the size of the dots is sufficiently large, the dominant mechanism for switching has been found to be nucleation followed by rapid propagation of domain walls (DWs). In this case, as the propagation fields are usually lower than the nucleation fields [HUG05, BUR13], the SFD corresponds to the distribution of nucleation fields, which is related to the distribution of magnetic anisotropy in the films. As the size of the dot decreases, the SFD is enlarged and shifted toward higher fields. A simple model taking into account the initial intrinsic distribution of magnetic anisotropy in the films can explained these results [HUG05, THO06]. When the dots become mono-domains (typically for sizes < 30 nm), a coherent reversal described by the Stoner–Wohlfarth model is expected [STO48]. However, due to the distribution of magnetic anisotropy in the films, the SFD is also increased when the dot size is reduced. In addition to such variability of magnetic properties in the pristine films, edge damages introduced by the patterning process can also have a strong influence on the switching behavior. This is the case for instance for STT-MRAM or DW-based nanodevices where the edges have been found to reduce the efficiency of the switching process at small dimensions [CAY04, KIN14, NOW16].

3.2 Kerr microscopy

In this section, we first introduce the concept of magneto-optical Kerr effect and then describe the Kerr microscopy setup that has been used in the invesitagation of field-induced switching of magnetic nanodots.

3.2.1 Magneto-optical Kerr effect

In order to directly observe the reversal process of magnetic nanodots, a Kerr microscope has been utilized. The Kerr microscope is based on the magneto-optic Kerr effect (MOKE) which was discovered in 1877 by John Kerr [Ker58]. When a beam of light passes through a polarizer, it will be polarized; and when a beam of polarized light is reflected from the surface of magnetic film, the direction of polarization of the light will rotate by an angle. This phenomenon is called the MOKE effect, as shown in Figure 30.

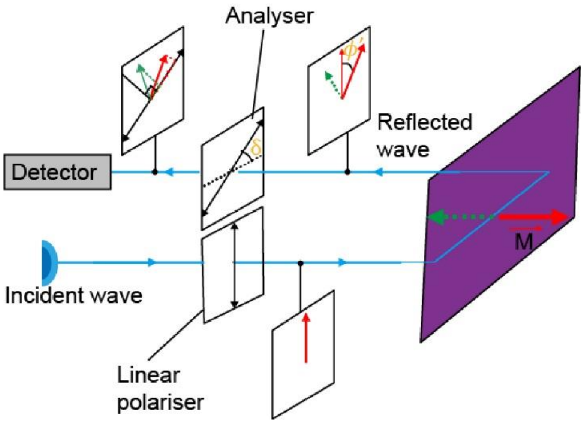


Figure 30 Kerr rotation of the light

Since the Kerr effect changes the linear polarized incident light into a slightly elliptical polarized light, it could be used to probe the magnetic state of magnetic materials. A microscope with perpendicular incident light is only sensitive to the perpendicular component of the magnetization of a magnetic film, which is suitable for the nanodots with PMA in our work.

3.2.2 Typical optical circuits of Kerr microscopy

The MOKE effect can be used to measure the hysteresis loop of a magnetic film and it also can be used to image the magnetic state of a sample. The latter one is called Kerr microscopy. Figure 31 shows the schematic of optical circuit of a polar Kerr microscope.

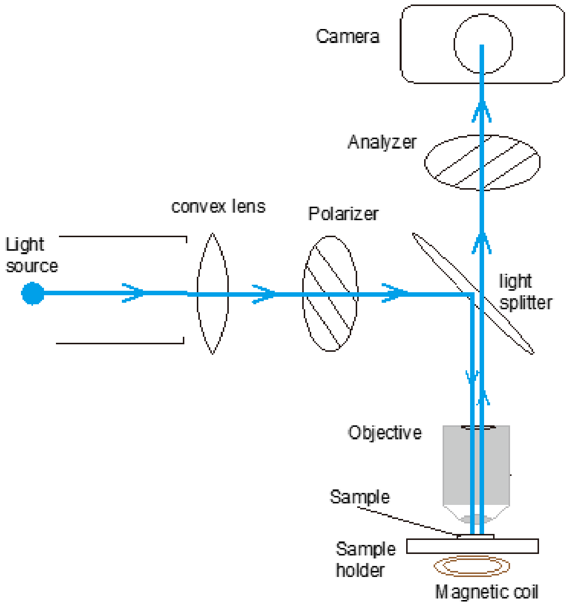


Figure 31 Configurations of the Kerr microscope

For a polar Kerr microscope, the light is incident from the normal direction of the sample surface. Both the incident and the reflected lights go through the objective, however, they can be separated by a light splitter. In more details, the incident light is focused by a convex lens and polarized by a polarizer. The polarized light go through the objective and then the reflection happens at the surface of the sample. The reflected light goes back into the objective and partially passed the splitter straightly. After filtering by the analyzer, the light is finally captured by a charge-coupled-device (CCD) camera. In this context, the Kerr rotation, which is proportional to the perpendicular magnetization can be directly cognized by the contrast of the digital image.

The Kerr microscope used in my PhD research is shown in Figure 32 [VER14], and has been designed by Dr. Nicolas Vernier in C2N.

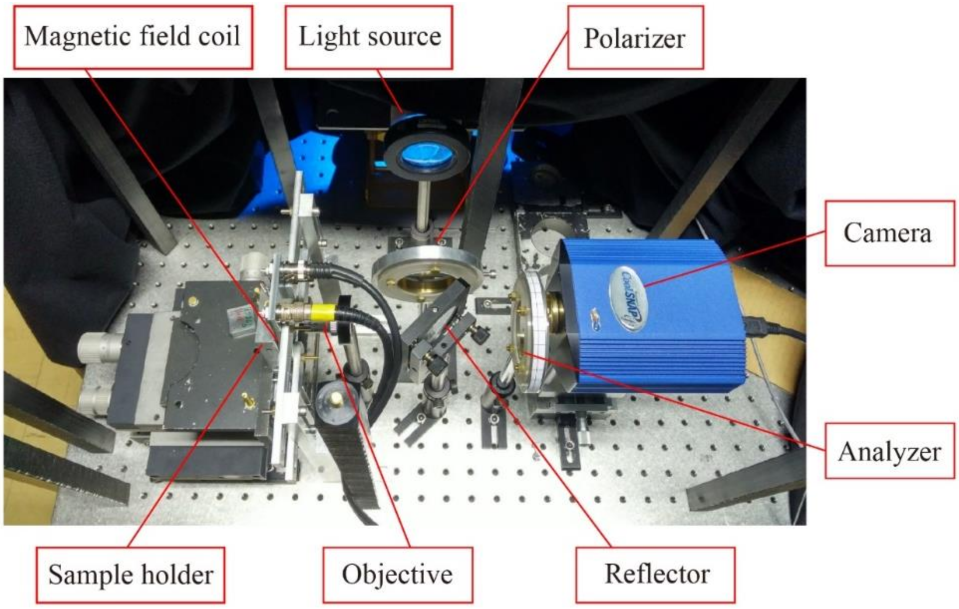


Figure 32 Kerr microscope setup used in this thesis

In the Kerr microscopy setup, a blue LED is used as the light source with a wavelength of 450 nm. We note that the resolution of a Kerr microscope is generally limited by the light diffraction, which is common phenomenon in optical microscopy setup. According to the Rayleigh criterion [WAL83, RAM06], the resolution of a microscope can be described as

$$\delta_d = \frac{0.61 \cdot \lambda_w}{n_a} \tag{3.1}$$

where δ_d is the minimum distance between two patterns to be distinguished, λ_w is the wavelength of the light source and n_a is numerical aperture (NA) of the objective lens. An ultimate resolution of optical microscope system is expected to be 400 nm according to the Rayleigh criterion. With an Olympus objective of magnification of 100× and a NA of 0.8, our Kerr microscope is able to detect magnetic nanodots contrast down to 400 nm, as shown in Figure 33.

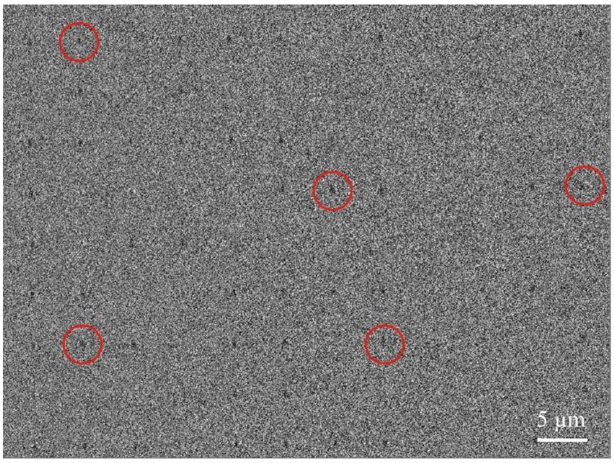


Figure 33 Kerr microscopy image of 400 nm nanodots. Several reversed nanodots are marked with red circle.

3.2.3 Typical configurations of magnetic coils

To investigate the field-induced switching of magnetic nanodots, an external field generated by homemade coils has been developed in order to reach short duration, narrow rising edge and large magnetic fields. Also, with an objective of 100×, the vision field (see Figure 33) is about 50 µm. The diameter of the coils needs to be large enough to provide the homogenous field within the vision field.

We note that the rise time of a generated magnetic field is in proportion to the inductance of the coils. To reduce the rise time, the number of coil turns needs to be reduced because the inductance of the coils increases with the increase of the coil turns. However, the magnitude of the magnetic field is also in proportion to coil turns, e.g. more coil turns there are, larger magnetic field we can obtain. In addition, the Joule heating due to the current passing the coils is related to the diameter of the varnished wire used as well. Therefore, there is a trade-off for the parameters including the diameter of the coils, the number of the coil turns, the relative position between the sample and the coils (the distance between them matters) and the resistance of the coils (also related to the material of the coils). The parameters used for the magnetic coils in the Kerr microscopy setup are shown in Table 2.

Table 2 Parameters for the magnetic coils

Coil turns	Diameter	Resistance	Rise time*	Inductance	Field	Distance**
120	6/10 nm	10 Ω	1.92 μs	192 μH	10.2 mT/A	2.3 mm

*** Rise time when connected in series with 50 Ω.**

**** Distance between the coils and the sample.**

The configuration of the magnetic coils and the relative position between the sample, coils and objective is showed in Figure 34. The sample is fixed by two plastic sample holder, which aims to avoid the eddy currents in metal materials.

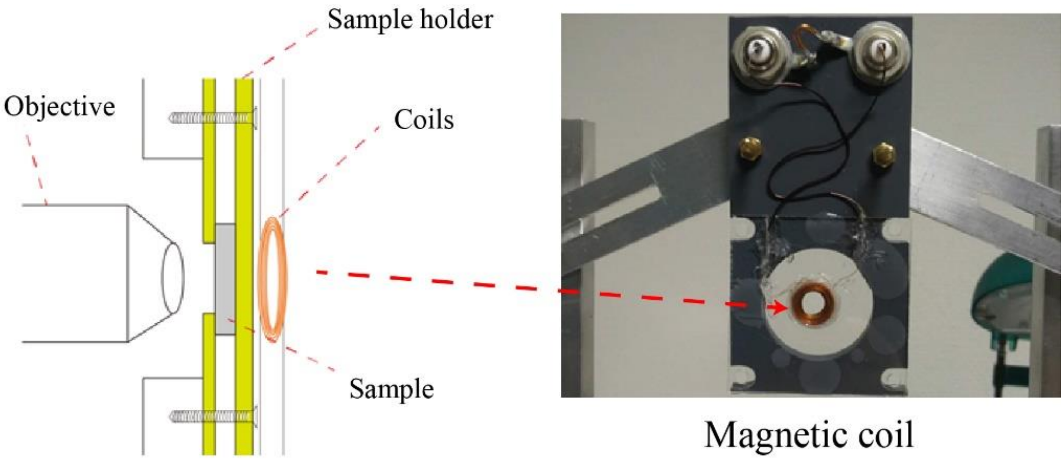


Figure 34 The configuration of magnetic coils, the objective and the sample

3.2.4 Typical configurations of power supply for coils

The magnetic fields in our experiments involved constant fields with a shape of square pulses. Figure 35 shows the configurations for the power supply of the magnetic coils.

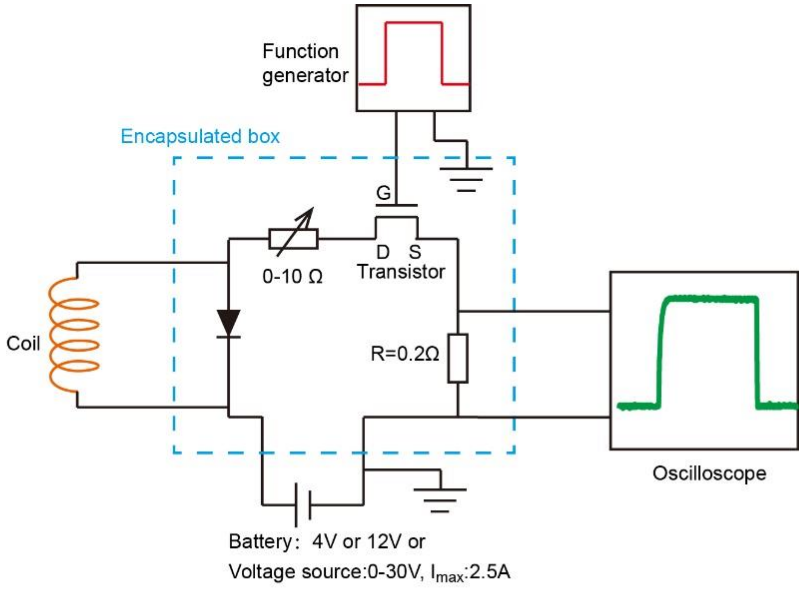


Figure 35 Configurations of the power supply circuit for coils

The ON/OFF of the power supply is controlled by a transistor whose gate voltage is further controlled by a function generator. A shunt resistance of 0.2 Ω is connected in the circuit and an oscilloscope is connected to this resistance in parallel to monitor the waveform. A battery or a voltage supply can be used as power source.

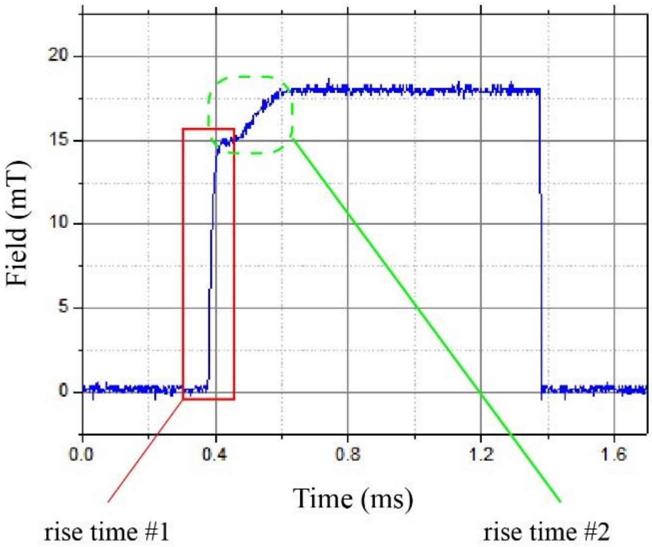


Figure 36 Rise time of the generate pulse of magnetic field by coils

The rise time of the voltage supply (rise time #2) is about 200 μs (see Figure 36) while it is much smaller for battery. The rise time of the coils (rise time #1) is about 20 μs, which is shorter than that of the power source. In our experiment, the duration of the field pulse is then counted after the voltage output become stable.

The typical magnetic field H generated by the coils from less than 1 mT to 50 mT is given by the following formula:

$$H\ (mT) = \frac{[Vos\ (V)]}{0.2\ (\Omega)} \cdot 10.2\ (mT/A) \tag{3.2}$$

where Vos is the applied voltage read from the oscilloscope.

However, if we want to further reduce the duration of the field pulse down to sub-20 μs, another implementation with a power supply based on the discharge of condenser bank as well as a large resistance connected in series with the coils is needed, as shown in Figure 37.

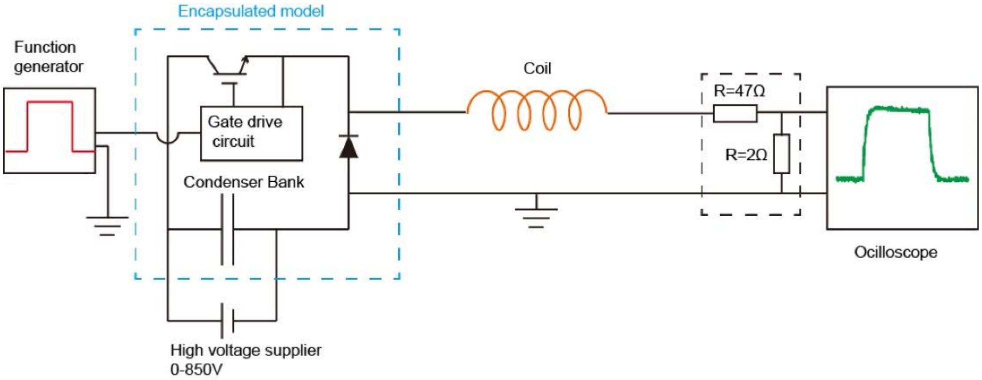


Figure 37 The power supply system based on a discharge of a condenser bank

The rise time in this power supply system can be estimated by a simple LC circuit including the coils and other resistance component:

$$\tau = \frac{L}{R_{coil} + R_{circuit}} \tag{3.3}$$

where τ the characteristic rise time, L the inductance of coils, R_{coil} the resistance of coils and $R_{circuit}$ the other resistance component in the power supply circuit (excluding the resistance of the coils).

From the equation (3.3), by connecting a large resistance (e.g. 50 Ω), a shorter pulse duration can be accomplished. The aim of utilizing the discharge of condenser bank is to provide the high voltage supply with a fast response speed, which is not applicable to ordinary voltage/current power sources. This power supply system can generate magnetic field pulses as narrow as 5 µs. However, if the pulse duration is over 10 µs for this power supply system, it has the risk to destroy the switch of discharge of condenser bank.

3.3 Kerr microscopy measurement

As described in Chapter 2, nanodots for sizes ranging from w=400 nm to 1 µm were patterned. The pitch (defined as the distance between the centers of two nanodots) was chosen to be 5 µm to minimize the influence of dipolar effects [PFA14]. In order to characterize the switching process, the following procedure was employed: the film was first saturated with a large positive magnetic field along the perpendicular direction (easy axis) and then successive negative magnetic field pulses with a duration of 1 ms were applied for investigating the switching process. For each magnetic field pulse, the number of reversed islands was counted. The switching probability of the array was then obtained by calculating the ratio of the reversed nanodots to the overall number of the nanodots. Figure 38 shows the typical magnetic switching process of the nanodots arrays for a size of 1µm and 600 nm respectively.

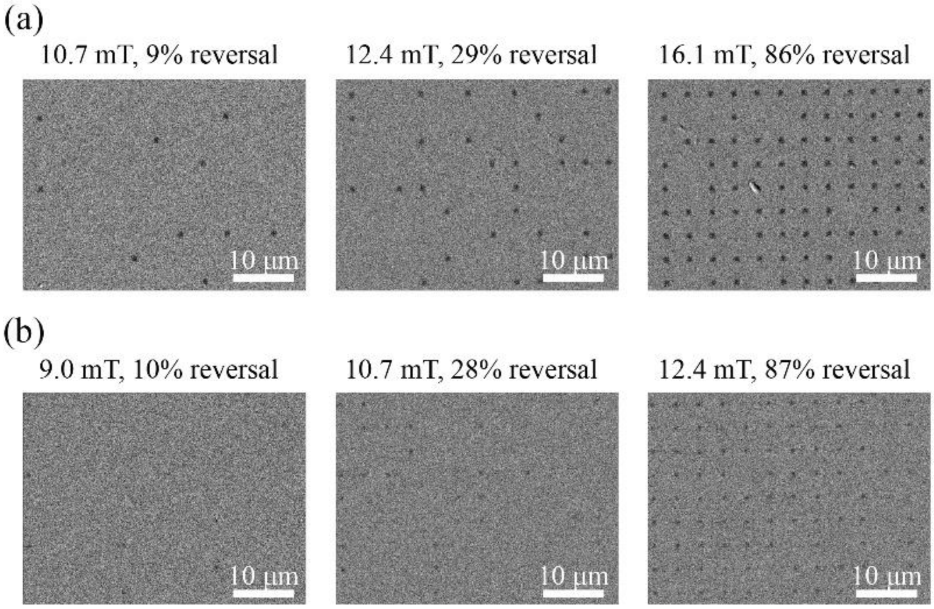


Figure 38 Kerr microscopy images showing the switching process under magnetic fields for a nanodot array with dot size of (a) 1 µm and (b) 600 nm

As expected, due to the variability of the nano-elements, a SFD is observed. For instance, for the 1μm nanodots (see Figure 38 (a)), nearly 10% and 90% of the nanodots were reversed under magnetic fields of 10 mT and 16 mT, respectively. Surprisingly, we observe that for the array of 600 nm nanodots (see Figure 38 (b)), the SFD is shifted to lower magnetic fields. In this later case, nearly 10% and 90% of the nanodots were reversed under magnetic fields of 9 mT and 12 mT respectively. The SFD measurements were repeated several times for each dimension and were very reproducible within a variation of 2%, as shown in Figure 39, for three switching measurements under the same magnetic field for dots size of 800 nm.

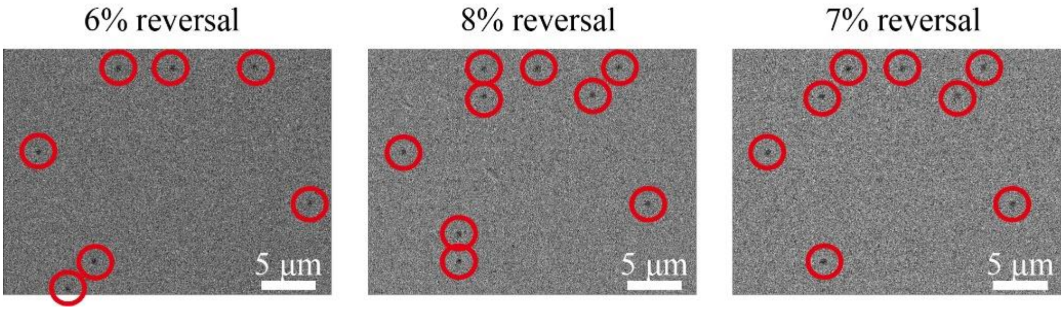


Figure 39 Kerr microscopy images of nanodots showing the reproducibility
The measurements were repeated three times under the same magnetic field of 9.8 mT. The switched magnetic nanodots are marked with red circles.

The number of switched islands for nanodots size of 1μm and 600 nm is shown in Figure 40 (a) and (b) respectively. In addition to the shift of the SFD to lower magnetic fields for smaller nanodots, we observe that the shape of the distribution is roughly not modified.

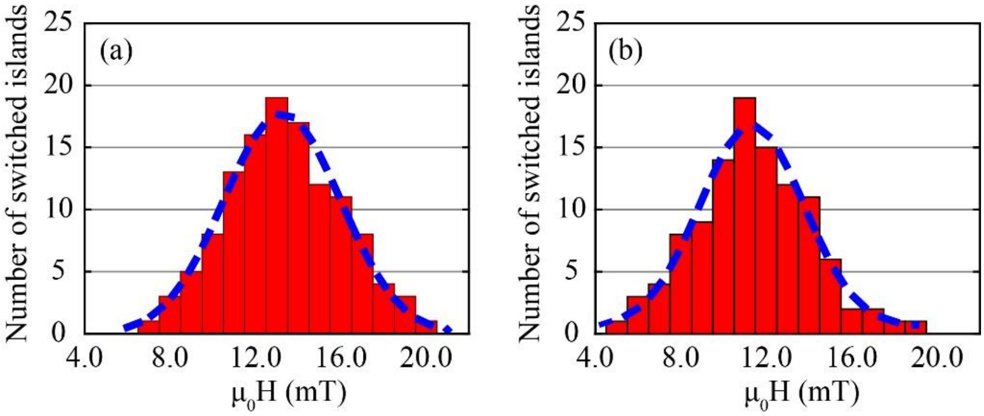


Figure 40 Histogram indicating the number of islands that switch as a function of the applied magnetic field for a dot size of (a) 1 μm and (b) 600 nm

In order to fit the data, we have used the method based on integrated Gaussian distribution fits [SHA08], where the cumulative distribution function, can be written:

$$P(H)=\frac{1}{2}\left[1+erf\left(\frac{H-H_{sf}}{\sigma\sqrt{2}}\right)\right] \tag{3.4}$$

with the error function defined as the following:

$$erf\,(x)=\frac{2}{\sqrt{\pi}}\int_0^x e^{-t^2}dt \tag{3.5}$$

Using this approach, the average switching field (mean) H_{sf} and the width of the distribution (standard deviation) σ can be determined precisely, as shown in Figure 41 and Table 3.

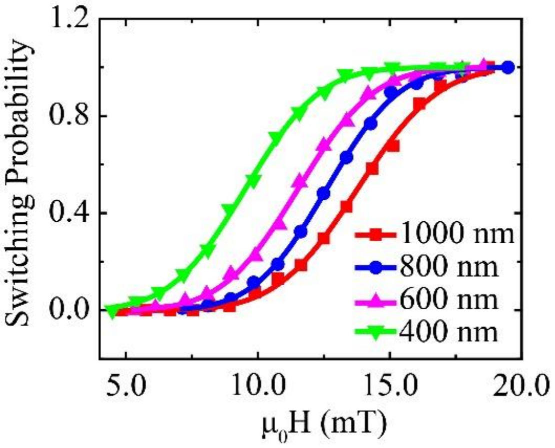


Figure 41 Average switching probability as function of magnetic field

Table 3 Average switching field and width of the distribution as a function of the dot size

Dot Size nm	1/Size μm^{-1}	Average switching field [a] mT	Width of the distribution [a] mT
400	2.50	9.5	2.2
600	1.67	11.5	2.3
800	1.25	12.6	2.2
1000	1.00	13.5	2.4

[a] *Average switching field* H_{sf} and the *width of the distribution* σ are obtained by extracting the parameters from experimental data (see Figure 41).

Consistent with Figure 38, we observe a clear shift of the SFD toward lower fields when the size is reduced without noticeable change for the width of the distribution σ

~2 mT. In addition, Figure 42 indicates a linear relationship between the average switching field H_{sf} and the inverse of the size w.

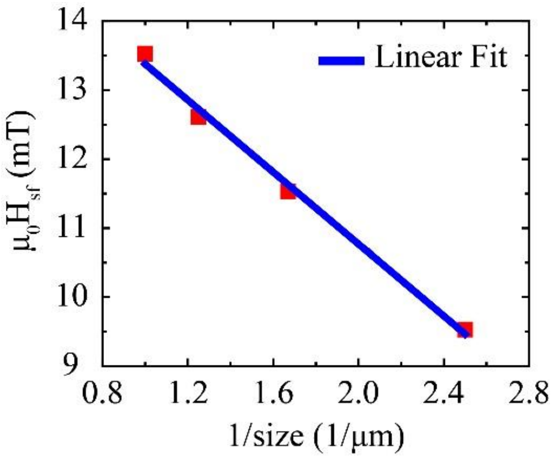


Figure 42 Average switching field as a function of the inverse of the dot size

3.4 DW statics and dynamics analysis

3.4.1 Process-induced anisotropy distribution

In order to understand why the SFD is switched to lower magnetic fields when reducing the size of the nanodots, large diameter structures were fabricated with the same patterning process as the one used for the array of nanodots. The sample (size of 400 μm) was first saturated with a strong magnetic field and then an opposite field of 40 mT was applied for 5 μs. As it can be shown in Figure 43, although a few nucleation sites are present inside the squares as expected for much larger structures, we observe that most of the nucleation and propagation events occur along the edges. This result suggests the existence of a region of lower anisotropy at the edges of the elements that channels both DW nucleation and motion. We believe that this feature is due to the patterning process [SHA08, DUR16, JOH96, YAN11, LAU07, KIN10, NEU16], in particular the Ar ions milling that induces damages such as edge roughness, redeposition on the sidewall, intermixing of the interfaces, or oxidation of the layers. Besides, owing to the difference in etching rate, material segregation of CoFeB may also lead to the different compositions of Co and Fe at the edges as well [BUR13, VER14]. The damaged region is in general of the order of the grain size, which corresponds to a typical length scale of 10-20 nm [CHU12].

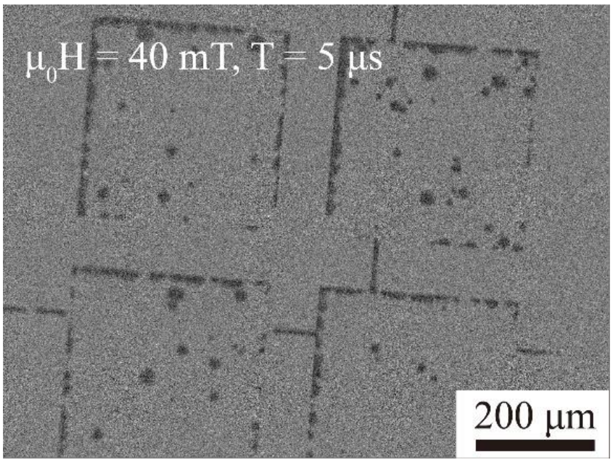


Figure 43 Kerr microscopy image of large squares indicating the presence of nucleation event

Below, we show that our results can be explained by the pinning of the DW at the edges of the nanodots together with the action of a Laplace pressure on the DW. First, as demonstrated previously [FRA11], the presence of a gradient of anisotropy on the scale of the DW width Δ can induce strong DW pinning. In particular, if we consider a DW pinned at the edges of the nanodots, the depinning field is given by

$$\mu_0 H_{depin} = \frac{K_{eff1} - K_{eff2}}{2 \cdot M_s} \cdot \frac{2\Delta}{\delta} \tanh\left(\frac{\delta}{2\Delta}\right) \tag{3.6}$$

where K_{eff1} and K_{eff2} are the effective anisotropy in the non-damaged and damaged area respectively, δ is the gradient length, M_s is the volume saturation magnetization, Δ is the DW width and tanh(x) is the Hyperbolic function (as shown in Table 4).

Table 4 Function tanh(x) according to the ratio of gradient length δ and DW width Δ

	$\tanh\left(\frac{\delta}{2\Delta}\right)$	$\frac{2\Delta}{\delta}\tanh\left(\frac{\delta}{2\Delta}\right)$
δ = 0.5 Δ	0.24	0.96
δ = Δ	0.46	0.92
δ = 2 Δ	0.76	0.76
δ = 4 Δ	0.96	0.58

In particular, for δ of the order of Δ, a variation of a few 10% of the anisotropy can give depinning fields of the order of a few 10 mT, which is much larger than the ultra-low intrinsic depinning fields of the films (~ 3 mT) [ZHA18]. As a result, once reversed domains are nucleated at the edges, they are expected to only propagate along the edges (i.e along the pinning potential) as shown in Figure 43, and not toward the center of the nanodots (i.e across the pinning potential).

3.4.2 Laplace pressure in DW

In the following, we further describe the depinning process to reverse the entire nanodot by considering a circular single magnetic domain wall of radius R=w at the edges of the nanodot (see Figure 44).

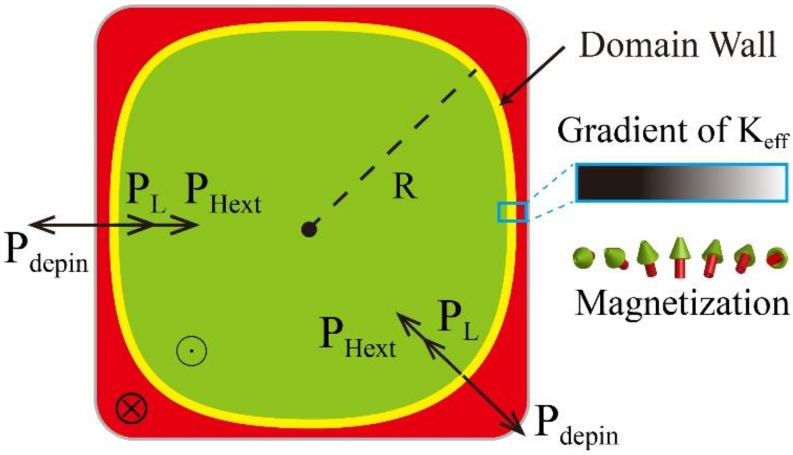


Figure 44 Schematic of the magnetization reversal process of a nanodot. A circular DW (yellow) of radius R is located at the edge of the dot, separating the reversed (red) and not reversed regions (green). The DW is pinned by a gradient of anisotropy on a length scale of δ~Δ due to edge damages. P_{depin}, P_{Hext} and P_L correspond to the pressures applied on the DW due to the pinning, the external magnetic field and the Laplace pressure, respectively.

As we have evidenced recently, in addition to the driving magnetic field, a Laplace pressure is applied on the domain wall, which is a mechanism quite well known for soap bubbles [ISE92, GEN04]. The Laplace pressure results from the DW energy that favors the collapse of magnetic bubbles when the radius R of the bubble is reduced [GAU77, JIA33]. It can be expressed here as:

$$P_L = 2\lambda/w \tag{3.7}$$

where λ is the interfacial energy density of the DW pinned at the edges of the nanodots. We note that for Bloch type DWs, the interfacial energy density can be written $\lambda = 4\left(A_s \cdot K_{eff2}\right)^{1/2}$ where A_S is the exchange stiffness constant. When an external magnetic field H_{ext} is applied along the perpendicular direction, the Zeeman energy induces a pressure on the DW that can be written as:

$$P_{Hext} = 2 \cdot M_s \cdot \mu_0 H_{ext} \tag{3.8}$$

The Zeeman energy and the Laplace pressure act together to unpin the DW as illustrated in Figure 44, which gives:

$$P_L + P_{Hext} = 2 \cdot M_s \cdot \mu_0 H_{depin} \tag{3.9}$$

By combining Equation (3.7), (3.8) and (3.9), this gives the minimum switching field H_{sf} to overcome the pinning potential as:

$$\mu_0 H_{sf} = \mu_0 H_{depin} - \frac{\lambda}{M_s} \cdot \frac{1}{w} \tag{3.10}$$

This result is in agreement with the linear variation experimentally observed in Figure 42 and indicates that the Laplace pressure just acts as a simple effective field proportional to 1/w, which only shifts the distribution without modifying its width σ. Using a linear fit allows us to determine $\mu_0 H_{depin}$ and λ / M_s. The linear fit gave a parameter of intercept of 16 (mT) and a slope of -2.60 (mT·μm). We find $\mu_0 H_{depin}$ = 16 mT and a DW energy $\lambda = 3.4 \times 10^{-3}\ J/m^2$, which is in very good agreement with previous studies [ZHA18, YAM11]. Finally, by considering $\mu_0 H_{depin}$ =16 mT, a typical gradient of δ~Δ and the experimental values $K_{eff1} = 1.3 \times 10^5\ J/m^3$ and $M_s = 1.3 \times 10^6\ A/m$, Equation (3.4) gives $K_{eff2} = 8.5 \times 10^4\ J/m^3$.

These results indicate that due to patterning induced damages, a gradient of anisotropy of about 30% is present at the edges of the nanodots on a length scale of the DW width.

3.5 Summary

In this chapter, we demonstrated that due to the presence of edge damages, the nucleation and depinning process of DWs govern the magnetization reversal of magnetic nanodots under magnetic field. Due to the Laplace pressure, we demonstrate that the depinning field to reverse the entire elements varies as 1/w. This feature should be taken into account in advanced spintronic devices such as for instance spin-orbit torque MRAM (SOT-MRAM) where the spin current can also induced the nucleation of DWs at the edges of the elements. These results also suggest a path toward scalable devices based on controlling the nucleation and pinning potential of DWs at the edges of the elements with nanoscale. In this case, benefiting from the Laplace pressure and keeping the same thermal stability given by the gradient of anisotropy, a lower switching current would be needed when reducing the size of the devices.

CHAPTER 4 RESISTIVELY ENHANCED MRAM DEVICE

4.1 Transport measurements of the patterned nanopillars

As discussed in the general introduction, MRAM and RRAM have attracted increasing interest for the past decades [WON15, WON12, LIN14, CEL14]. Tremendous efforts have been involved and amazing advances have been achieved in this field. Nevertheless, a few issues still exist and should be addressed before popular applications. For example, multilevel resistance states can be achieved in both MTJs and RRAM devices. For MTJ devices, there are two main methods to obtain the multilevel resistance states, either by taking advantage of the stochastic behavior of the magnetic switching [QUE15], or by using vertical stacked MTJs as multilevel cell [ZHA16]. However, both of methods suffer from a challenge of a relative low tunnel magnetoresistance (TMR) ratio (<250% to date), which is a key limitation for high density and high reliability applications [SON16, TEZ16, KAN14]. Regarding RRAM devices with high ON/OFF ratios, they can provide the perfect multilevel resistances required for applications, but its relative low access speed and endurance issues are limited by its intrinsic mechanism as electrochemical reduction and Joule heating process, which have become an intrinsic drawback for computing tasks.

Therefore, an NVM that eliminates these shortcomings, for example, by integrating MRAM and RRAM into a single device, is still highly desired. Several recent studies based on an MgO-based MTJ have exhibited both magnetic switching (MS) and resistive switching (RS), enabling such possibilities [HAL08, KRZ09, TEI09]. However, those devices suffer from a trade-off between MS and RS as the MgO layer acts as both a tunnel barrier for MS and an insulator for RS.

In this chapter, we describe the switching process of MTJ nanopillars based MRAM devices which have been fabricated using the process described in Chapter 2. We give the evidence that silicon switches within the SiO_2-based encapsulation layer are formed at the edges of the MTJ nanopillars unexpectedly. By taking advantage of this feature, we demonstrate a heterogeneous memristive device, namely resistively enhanced MTJ (Re-MTJ) that combines magnetic (MRAM) and resistive (RRAM) switching in a single element. The potential applications for Re-MTJ as a logic-in-memory device with memory encryption function or Normally-off/instant-on function are also discussed.

4.2 Transport measurements of the patterned nanopillars

Figure 45 shows a schematic of the Re-MTJ device made of an in-plane magnetized CoFe(B)-MgO MTJ nanopillar and a SiO_x-based polymer encapsulation layer.

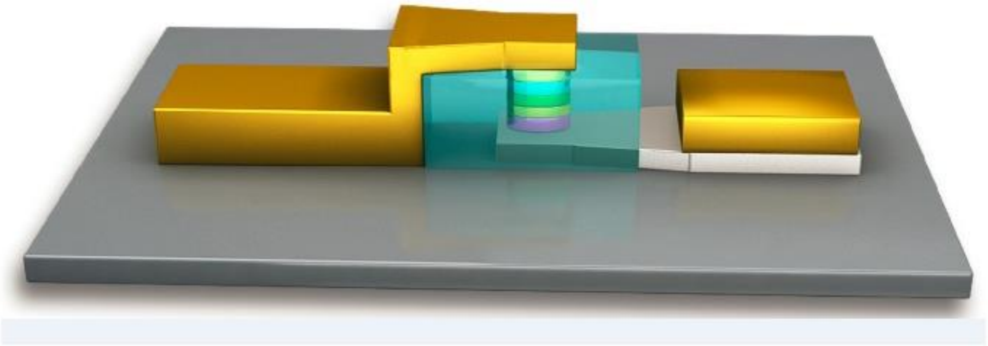


Figure 45 Schematic of Re-MTJ device

The fabricated Re-MTJ devices were characterized using dc-transport measurements under in-plane magnetic fields (with a precision below 1×10^{-3} Oe) with a two-probe geometry at room temperature, as shown in Figure 14. A bias voltage (or current) was applied to the top electrode, while the bottom electrode was grounded. The voltage-pulse (or current-pulse) durations were τ_P=200 ms, and the remanent resistance of the Re-MTJ device was measured under a low bias between each voltage (or current) change.

A very peculiar resistive behaviour of the device is shown in the typical I-V curves of Figure 46. Indeed, a, bipolar (in which positive and negative voltages have opposite effects) voltage-induced resistive switching (VIRS) was observed in the absence of any external magnetic fields up to 0.8V. For this measurement, the MTJ was set to either the P or AP state using the external magnetic field before the measurement. Clear resistive switching behaviour is observed from which a SET and RESET voltages could be identified. Figure 46 (b) shows the corresponding R-V curve for the P and AP configurations, in which the low-resistance state (LRS) and high-resistance state (HRS) can be observed. Here, the LRS is approximately 600 Ω, irrespective of the magnetic configurations, and the HRS is approximately 1100 Ω and 1300 Ω for the P and AP states, respectively. Notably, magnetization switching between the P and AP states was not observed during the voltage sweep. Additionally, we observed that the SET and RESET voltages were independent of the magnetic configuration.

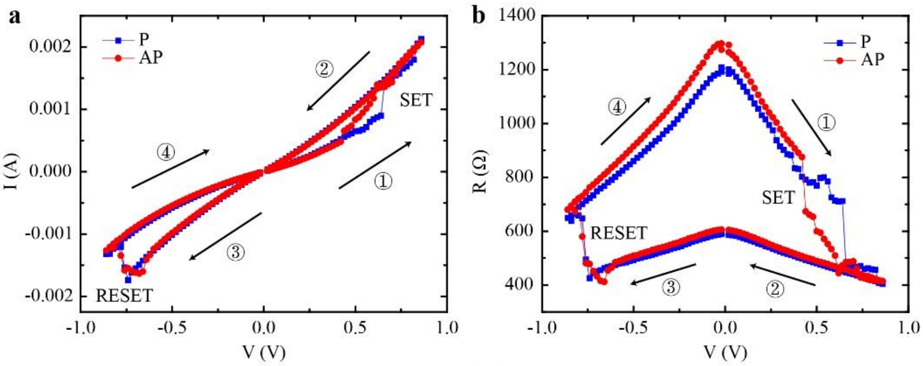


Figure 46 Resistive switching curve of Re-MTJ device. (a) I-V curves without an applied magnetic field between+1V and -1V. The MTJ was set to either the P or AP configuration before the measurement. The SET and RESET voltages are indicated. (b) Corresponding R-V curves of (a).The direction of the external magnetic field is along the easy axis of the ellipse. The arrows and numbers indicate the voltage sweep direction.

Typical TMR values between 20% and 60% are measured and ON/OFF ratio from 120% to 1000% are observed, as shown in the Figure 47. During the current sweep, when a current pulse I with a duration of 200 ms is applied to the device, the voltage V is measured by the voltmeter (which is integrated in Keithley 4200) and then, the resistance is calculated by R=V/I. We note that the data point of I=0 has been deleted from the Figure 47 and it can be estimated by the two data points with very small current value (e.g. ±0.16 mA), which is consequently shown as a trend of divergence at I=0.

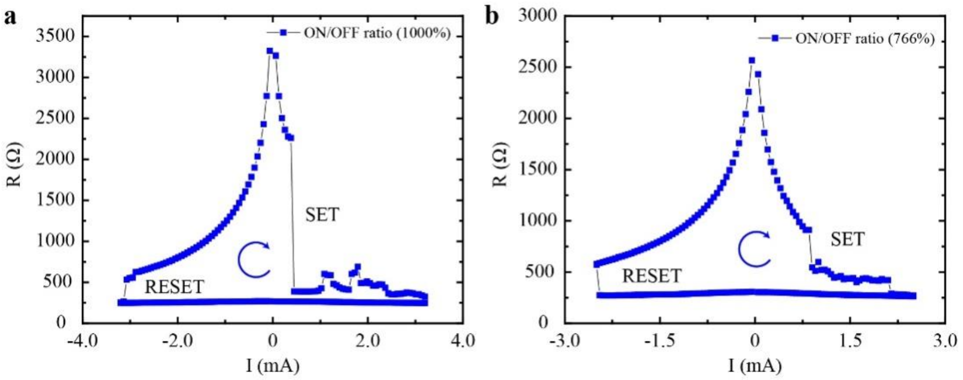


Figure 47 R-I curves showing the ON/OFF ratio of Re-MTJ devices. High ON/OFF ratios were obtained, such as the two examples shown here that were measured on the same wafer: (a) 1000% and (b) 766%.

Figure 48 shows the R-V curve under the in-plane magnetic fields [LOU30] that were used to assist CIMS. Pure CIMS was not obtained here at low voltages due to the thickness of the free layer, which is as thick as 3 nm. The maximum voltage applied was below 0.2 V in order to avoid VIRS and maintain the HRS. We observed CIMS assisted by the magnetic fields of $H_{ext}^{AP\to P} = +110\,Oe$ and $H_{ext}^{P\to AP} = -104\,Oe$ with typical current densities of $J_c^{AP\to P} = 1.7\times10^5\,A\,cm^{-2}$ and $J_c^{P\to AP} = 0.8\times10^5\,A\,cm^{-2}$, respectively. These results show that CIMS and VIRS could be controlled independently. To observe both effects, a voltage was applied between ± 0.8 V under a magnetic field, as shown in the Figure 48. In this case, we clearly observed that the VIRS and CIMS effects could act simultaneously.

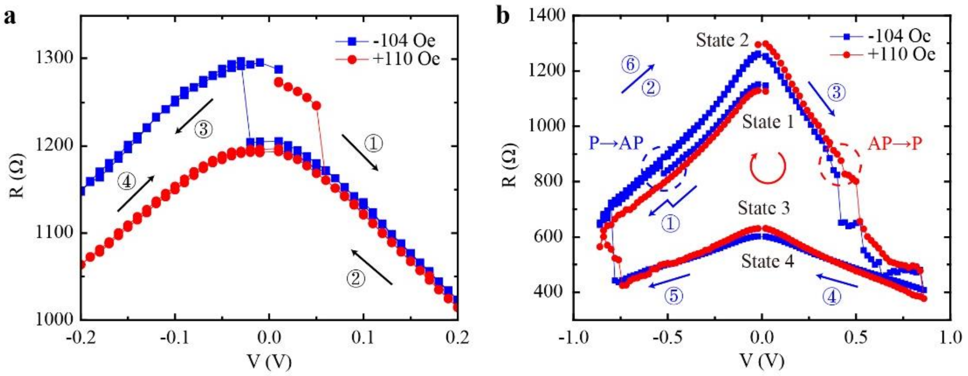


Figure 48 (a) CIMS of Re-MTJ devices (b) independently-controlled CIMS and VIRS of Re-MTJ devices. In figure (a), R-V curves under external positive and negative magnetic fields for voltages between +0.2 V and -0.2 V, indicating pure CIMS without VIRS. In figure (b), R-V curves under external positive and negative magnetic fields between +1 V and -1 V. The

VIRS process is observed near +0.5 V (SET) and -0.7 V (RESET). For the CIMS process, P to AP switching is observed near -0.5 V for a magnetic field of -104 Oe and near +0.4 V for a magnetic field of +110 Oe. The direction of the external magnetic field is along the easy axis of the ellipse.

4.3 Microstructure Characterization and device modelling

4.3.1 Microscopic structure characterization of Si filaments

The results shown in Figure 46 indicate the presence of RS in the MTJ. One possibility is the presence of filaments current path in the MgO barrier. However, contrary to previous results in RS switching in MgO barrier [HAL08, KRZ09, TEI09], we observe bipolar switching instead of unipolar switching (SET and RESET were caused by applying voltages with the same polarity). In addition, we observed both MS and RS in the same R-V loop; this result suggests two independent origins for the CIMS and RS processes. To gain more insight, we carefully investigated the microstructures of the elements. The cross-sectional samples were prepared by using a focused ion beam in the plane of the long axis of the ellipse. The HRTEM, scanning TEM (STEM) and EDS mapping/line scanning were performed using a JEM-ARM-200F transmission electron microscope operating at 200 KeV.

As described in Chapter 2, the nanofabrication process of the Re-MTJ device consists of encapsulating the CoFe(B)-MgO nanopillars with a SiO_x insulator in contact with the edges of the nanostructure. In the following, we provide evidence that the VIRS behaviour was induced by the presence of the resistive Si filaments at the edges of the nanopillars.

Microscopic structure characterizations were performed using energy-dispersive X-ray spectroscopy (EDS). Figure 49 (b) and (c) indicate the presence of the Ta and Si elements detected by measuring the characteristic peaks of the Ta-Lα (8.145 KeV) and Si-K series lines, respectively. Note that since Ta-Mα (1.709 KeV) and Si-Kα (1.739 KeV) were separated by only 30 eV, the detector could not resolve these lines [WAG79, HOL04]. The detection results of both the Si and Ta elements overlapped, as seen in Figure 49 (c). Thus, the comparison between Figure 49 (b) and (c) clearly evidenced that Si aggregation occurred along the sidewall of the nanopillars with a typical width of 5-10 nm.

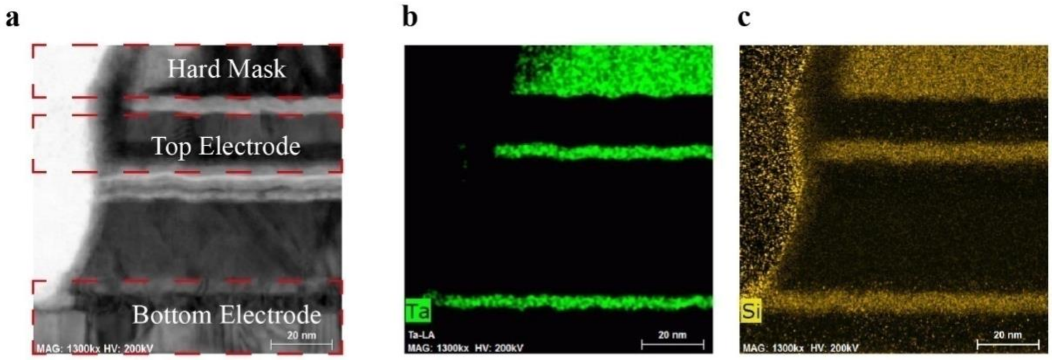


Figure 49 EDS results of element distribution on the edge of Re-MTJ device. (a) STEM image near the vertical edge of the MTJ nanopillar. The regions of the hard Ta mask, top electrode and bottom electrode are indicated by the red dashed rectangles. (b) EDS mapping of Ta using the Ta-Lαline characteristic peaks. (c) EDS mapping of Si using the Si-K series line characteristic peaks.

In addition, the high-resolution TEM (HRTEM) images of the nanodevice indicate the presence of nanocrystals with a typical size of 5-10 nm embedded in the amorphous SiO_x along the edges of the nanopillars (see Figure 50). The microstructural analysis and the electrical results (see Figure 46) are consistent with the results from recent studies [YAO10, YAO11, XIA12, WAN13], which indicated that RS in a SiO_x matrix can be induced in the presence of embedded Si nanocrystals. More precisely, when an SET voltage is applied, the Si nanocrystals can grow locally by favouring an electrochemical reduction process from $SiO_x \rightarrow Si$. This process induces a Si pathway (Si filaments) along the current flow direction, whereas a RESET voltage can favour the $Si \rightarrow SiO_x$ inverse process. This mechanism corresponds to a point-switching filament process involving local breakage and bridge evolution.

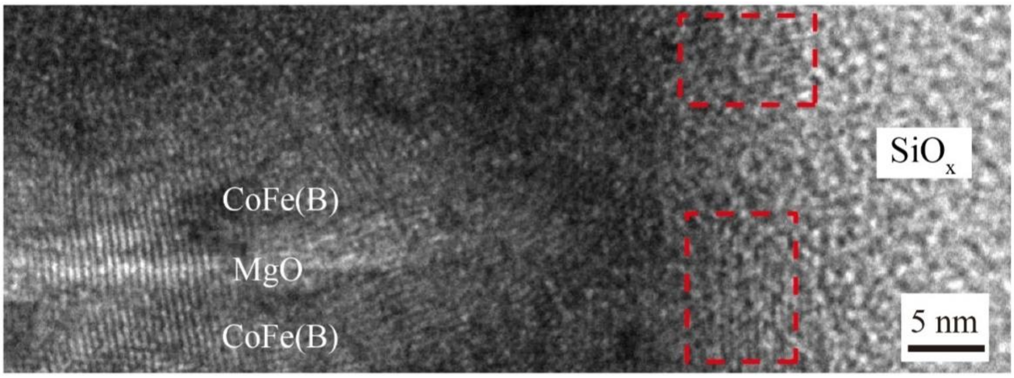


Figure 50 HRTEM image of the nanocrystalline structures in SiO$_x$ matrix. HRTEM image was taken near the edges of MTJ nanopillars. Nanocrystalline structures embedded in the SiO$_x$ matrix are indicated by the red dashed rectangles.

One important question is related to the presence of Si nanocrystals in our devices. It has been shown that the forming process of Si nanocrystals can be induced within pure SiO$_x$ matrixes at low temperatures by etching the SiO$_x$ [YAO10, ZHO14]. In this case, the Si filaments can germinate at the edges of the SiO$_x$ elements due to the presence of defects. In our case, the SiO$_x$ matrix surrounding the nanopillars was obtained by spinning a polymer (Accuflo) and transforming it into an insulator using an annealing process at approximately 300°C. During the annealing process, the edges of the nanopillars involving damages induced by the etching process could serve as seed interfaces to nucleate the Si nanocrystals. In addition, the crystalline character of the MTJ may have also favoured the germination of the Si nanocrystals. Indeed, an EDS linescan measured from the SiO$_x$ matrix into the MgO barrier (see Figure 51) indicated that both Si and O aggregated at the edges of the nanopillars on a scale of 10 nm with a ratio of silicon to oxygen elements that was much higher at the edges than in the SiO$_x$ matrix. The fact that bipolar behaviour was observed here for the SET and RESET processes may have been related to the presence of mobile oxygen ions.

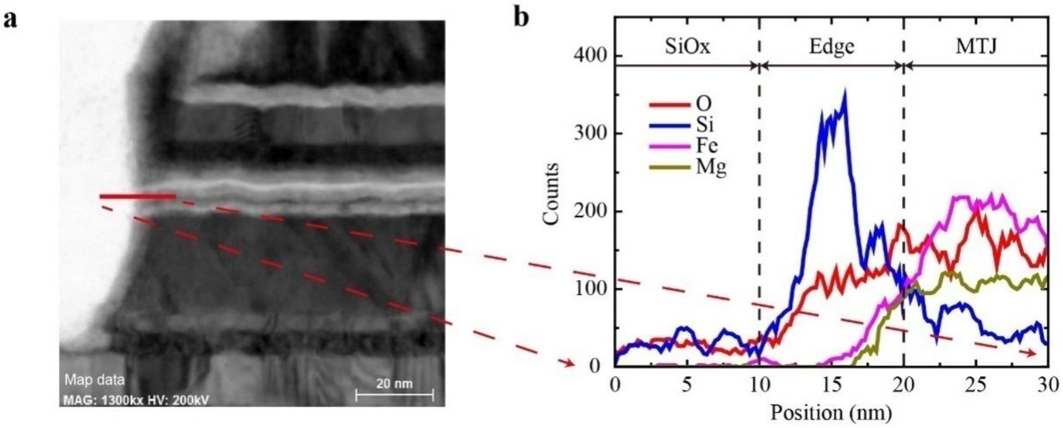


Figure 51 Material elements distribution on the edge of MTJ nanopillars. (a) STEM image obtained using an HAADF detector. The EDS linescan is marked in red and was measured from the SiO_x matrix into the MTJ nanopillar. (b) EDS linescans for O, Si, Fe and Mg corresponding to the red line indicated in (a). Three different regions can be delimited: a pure SiO_x region, an intermixed layer with aggregates of Si and O (10 nm) and an MTJ region.

4.3.2 Device modeling

Based on the analyses described above, a proposed schematic of the Re-MTJ device is presented in Figure 52 (a) that consists of an MTJ-based element connected in parallel with a Si filaments element. Such a device structure indicates that four distinct configurations with different resistance states can be achieved (see Figure 52 (b)); this result is in agreement with the experimental results (see Figure 48 (b)).

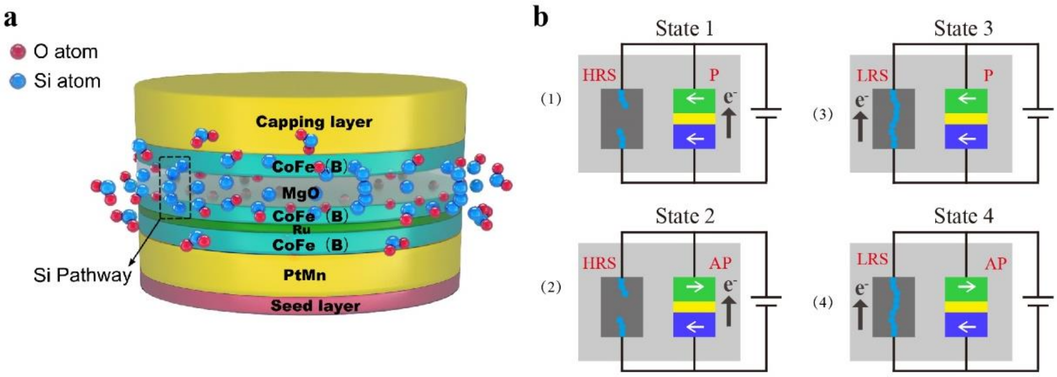


Figure 52 Device model of Re-MTJ. (a) Schematic of the MTJ nanopillar surrounded by Si filaments. The blue and red balls represent the Si atoms and O atoms, respectively. (b) Physical model corresponding to an RRAM element in parallel with an MRAM element. Depending on the configuration of the RRAM and MRAM elements, four different states can be obtained in the Re-MTJ device. The blue balls represent the conductive filaments that form the Si pathway. States 1-4 correspond to those in Figure 48 (b).

When the Si filaments are not conductive (RESET process), the current mainly goes through the MTJ, resulting in an HRS, and when the Si filaments becomes conductive (SET process), the current mainly flows through the Si filaments, resulting in an LRS. To further verify the proposed device model, simulations were performed using a compact model that integrated a physical-based STT-MTJ [ZHA12] and a bipolar metal-insulator-metal (MIM) resistive junction [RUS09] connected in parallel (see Figure 53).

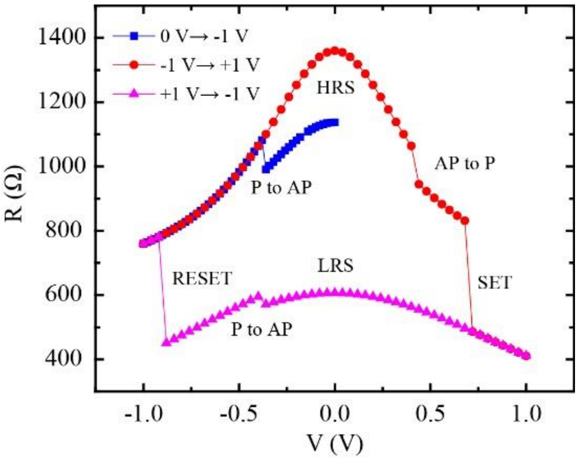


Figure 53 Compact model simulation of Re-MTJ device. Simulation of the R-V behavior using a compact model of STT-MTJ and an MIM resistive junction connected in parallel. A magnetic field was not included in the simulation.

The compact model of the device was written using Verilog-A language and evaluated in a Cadence Spectre environment. The compact model integrated a physical-based STT-MTJ and a bipolar MIM resistive junction connected in parallel. Magnetic fields were not considered in the simulation. Using the parameters of R_{AP}=1390 Ω, R_P=1160 Ω, R_{HRS}=645000 Ω and R_{LRS}=660 Ω, the R-V curve of Figure 48 (b) that combines the features of CIMS and VIRS could be well reproduced.

Furthermore, another interesting feature related to the microstructural properties of the devices is the strong correlation between the ON/OFF ratio of the RS and the TMR value of the MS (see Figure 54). The ON/OFF ratio and TMR ratio are measured for each device separately and Si filaments are not conductive (HRS) before the TMR measurement. The TMR ratios are obtained through an R-H measurements under a low voltage of 10 mV, which is much less than the SET voltage of filaments (which is around 0.8 V). The ON/OFF ratios are obtained through the current sweep.

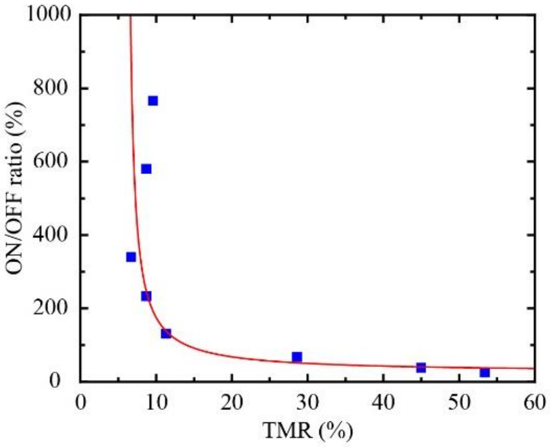


Figure 54 Relationship between the ON/OFF ratio and the TMR ratio. The data was measured from the different devices. The TMR was obtained through R-H measurements under a low voltage of 10 mV. The ON/OFF ratio was obtained after conducting a voltage (current) sweep. The blue squares are the experimental data, and the red line is a guide for the eyes.

In particular, the ON/OFF ratio increases when the TMR value is reduced. This result suggests that when the TMR ratio was low, a point-switching filament process could occur, whereas when the TMR is higher, the conduction through the Si filaments is not active. Notably, the ON/OFF ratio and TMR behaviour in these devices originates from the formation of an Si pathway in the SiO_x matrix [YAO10] and the Δ_1 Bloch states filtering at the CoFe(B)/MgO interface [ZHA03], respectively. The oxygen ion movement from the SiO_x matrix towards the MTJ nanopillars promotes the nucleation of the Si nanocrystals and affects the Fe-O bonds at the CoFe(B)/MgO interface [WAN16, ZHA03, TUS05, BON09]; this process results in a high ON/OFF ratio but a low TMR. As a result, the mobile oxygen ions near the edges of the nanopillars (see Figure 52) played a joint role in both the ON/OFF ratio and the TMR value.

We note that the "two current channel" model described in Figure 52 (b) is a simplified model, which says the current will go into either MTJ or Si filaments depending on the configuration of the filaments. However, since the MTJ structure is always ON (unless it breaks down), there will be always electrodes going through the MTJ when applied a voltage (or current).

4.4 Multi-states and nonvolatile feature of Re-MTJ

The multilevel states of the Re-MTJ device were investigated and are presented below. Figure 55 shows seven consecutive R-V curves indicating that different resistance states could be reached using a single device. Each R-V curve corresponds to a different degree of the Si oxidation pathway, and the pathways were randomly induced by the combination of a local strong electric field and heating during the point-switching filament process. We note that the difference in resistance before the voltage sweep is due to the difference in configuration of Si filaments.

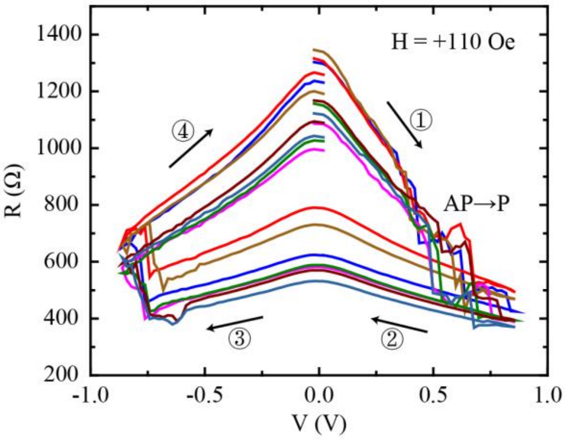


Figure 55 Seven different R-V curves under external magnetic fields in the same device

Figure 56 presents a Re-MTJ device that exhibits eight different states by combining two magnetic states (P and AP) with four different resistance states of the Si filaments. A larger TMR ratio is achieved for higher resistance states; this result suggests that the lower resistance of the MTJ dominates the current pathway.

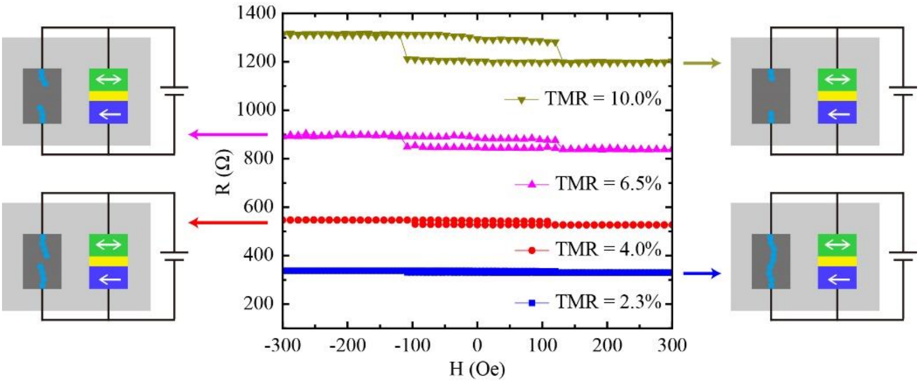


Figure 56 R-H hysteresis loops with different initial resistance states for the same device.

The measurements were conducted from an LRS (approximately 600 Ω) to an HRS (approximately 1300 Ω).

Furthermore, the data retention of the Re-MTJ device was tested for four different resistance states, that is, HRS with P, HRS with AP, LRS with P and LRS with AP (see Figure 57 (a)). All the configurations exhibit robust non-volatile properties. According to our experimental measurements, the four different (average) resistances of the Re-MTJ presented in Figure 57 (a) are 1304.7 Ω (HRS+AP), 1201.8 Ω (HRS+P), 595.7 Ω (LRS+AP), and 569.8 Ω (LRS+P), respectively. The resistance values between the LRS+AP and LRS+P states are close, which is owing to the parallel connection of the MIM and MTJ; however, those two resistance states can be separated from Figure 57 (b). It's important to mention that this resistance gap (between LRS+AP and LRS+P) can be improved by enhancing the TMR ratio with the further optimization of fabrication process.

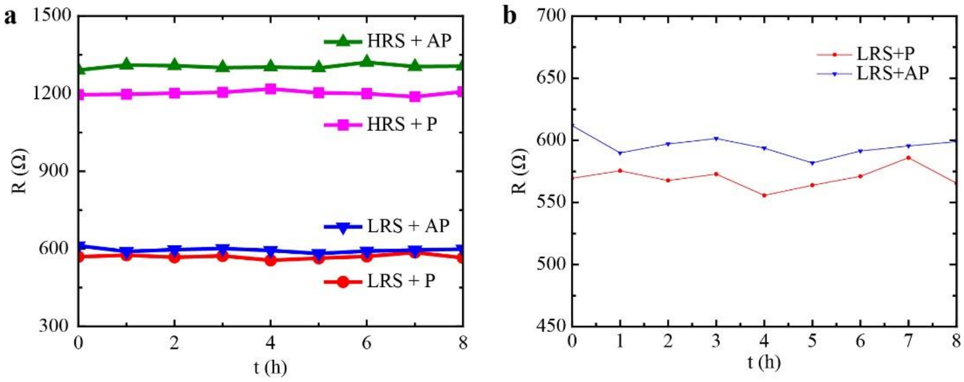


Figure 57 Time-independent resistance curves showing the non-volatile features of Re-MTJ. (a) Four different resistance states (LRS+AP, LRS+P, HRS+AP and HRS+P). (b) Two resistance states (LRS+AP and LRS+P) when the Si filaments are conductive.

4.5 Applications of Re-MTJ device

4.5.1 Multi-state memory device used for logic-in-memory architecture

Resistively enhanced magnetic tunnel junction (Re-MTJ) devices with a heterogeneous structure including an MTJ surrounded by resistive filaments were investigated for the first time for multi-level cell memory applications. By independent control of the MTJ and the conductive filaments, multi-state resistances can be obtained since both resistive and magnetic switching can be accomplished in a single element. Compared to conventional MTJs, the Re-MTJ devices have more resistance states without increasing the dimension. Taking advantage of these properties, new logic-in-memory applications can also be enabled for logic and storage respectively. Below we give a proof of concept of the experimental realization of a memory encryption function using multi-level states in our Re-MTJ devices.

Introduction: multi-states memory device

NVMs with multi-state resistance behavior have attracted extensive attention for its potential in brain-inspired computing and advanced logic-in-memories. For example, multi-state NVMs have been used to develop memristive logic computation [YAN13, WON15] and neuromorphic networks [PRE15, GRO16, OH17], which offer an opportunity to circumvent the "von Neumann bottleneck" in modern computer architecture. Researchers have proposed some prospective ideas, such as spintronics memristor [WAN09] and DW-based MRAM devices [SEN16, LEQ16], which can be used to obtain multi-state resistances. The multi-state resistance behavior in MRAM can also be achieved by either using the intrinsic stochastics of magnetic switching or using vertical stacked MTJs. However, both methods are challenged by a relative low tunnel TMR ratio. For RRAM device with a MIM structure, the resistance can be switched between LRS and HRS by configuring the conductive filaments with different bias voltages [HOU16]. The stochastics nature related to the filament configuration leads to multi-state resistances; however, it suffers from relatively low access speed [WON15, KEN15].

In this section, we have investigated the possibility to use our Re-MTJ device to construct the multi-level cell and a proof-of-concept of NVM encryption is experimentally demonstrated.

Results and discussion: from device structure to the multi-level behaviors

The proposed Re-MTJ device exhibits a heterogeneous structure with a parallel connection of an MIM (conductive filaments) and an MTJ, as shown in Figure 58. As shown in the previous paragraph, the electrons can either pass the MgO barrier of

MTJ by tunneling, or go through the conductive filaments via hopping. The conductive filaments are located at the edge of MTJ nanopillars embedded in the SiO_x matrix. Those conductive filaments favor either an electrochemical reduction process of SiO_x→Si (i.e., set process) under a positive voltage or an inverse Joule-heating assisted process of Si→SiO_x (i.e., reset process) as described before.

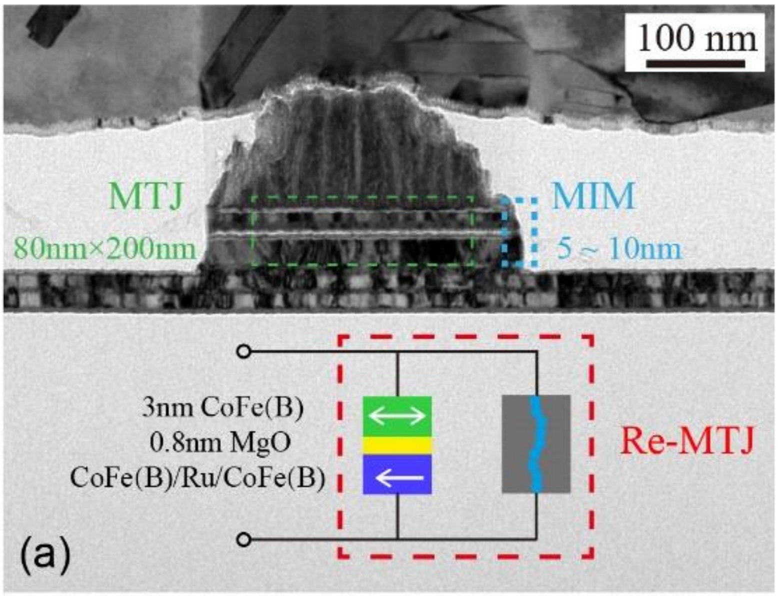


Figure 58 Cross-sectional HRTEM image and the corresponding device model of Re-MTJ. The Re-MTJ has a device structure of an MTJ in parallel connection with an MIM. The blue balls represent the conductive filaments.

For the device used for this experiment, different type of multi-state resistance behaviors in Re-MTJ can be observed from the switching process. The resistive and magnetic switching of Re-MTJ device are presented in Figure 59.

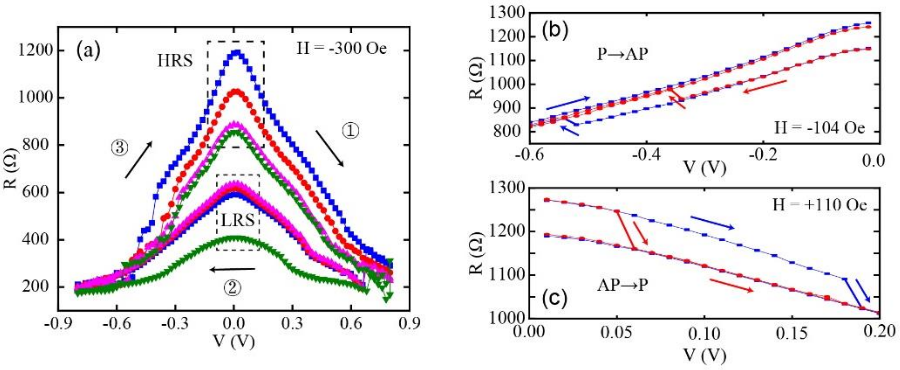


Figure 59 Transport measurements show both the resistive switching as (a) and magnetic switching as (b) and (c)

For the resistive switching, a set (reset) voltage of about +0.7 V (-0.8 V) can switch the MIM into LRS (HRS). Meanwhile, a magnetic switching of the MTJ between AP and P state occurs under voltages lower than ± 0.5 V. By applying appropriate magnetic fields and voltages, two switching mechanisms can be independently controlled in Re-MTJ devices. Figure 59 (a) shows four resistive switching loops with different HRS and LRS resistances. Here, in order to eliminate the influence of magnetic effects, a large external magnetic field (much larger than the coercivity of the free layer of the MTJ) was applied to pin the state of MTJ. Similar to filamentary-based oxide RRAM devices, the Re-MTJ can present one type of multi-state resistance behavior due to the different configuration of the filaments.

The magnetic switching with spin transfer torque (STT) effect can occur randomly for both P to AP and AP to P process, as shown in Figure 59 (b) and (c), respectively. In order to avoid the influence of resistive behavior, the voltages are well controlled below the threshold of the resistive switching. The in-plane magnetic fields (lower than the coercivity of the free layer) are used to reduce the critical currents and are not indispensable for STT switching in practical [SBI11]. A TMR ratio of ~ 20% together with an ON/OFF ratio of bipolar resistive switching up to 100 can be indicated from the conjoint analysis of the experimental results and compact model simulation results.

Interestingly, by a combination of resistive and magnetic switching, another type of multi-state resistance behavior can be obtained beyond the stochastic feature of conductive filaments. In details, for MTJs in both AP and P states, more resistance states can be accomplished with different configurations of conductive filaments. Since the filaments are only existed in a region of 5-10 nm around the MTJ nanopillars, which has been shown in the previous paragraph in Section 4.3.1, the Re-MTJ devices can provide more resistance states and better stochastic behavior without extra expense on the area of device compared to conventional MTJs. In addition, regarding the capacitor-like structure of resistive component, Figure 60 shows the AC-impedance spectroscopy of the Re-MTJ device. The phase degree as a function of frequency maintains a relative small range from 0° to 2.5° with the frequency up to

10^6 Hz, which indicates a good stability of Re-MTJ device for potential applications in logic/computation [ZHA17]. We note that the deterioration of stability in higher frequency may be explained by the parasitic capacitance; which is probably formed on the edges of nanopillar during the etching process. However, it barely shows the influence on a good nonvolatility of Re-MTJ device.

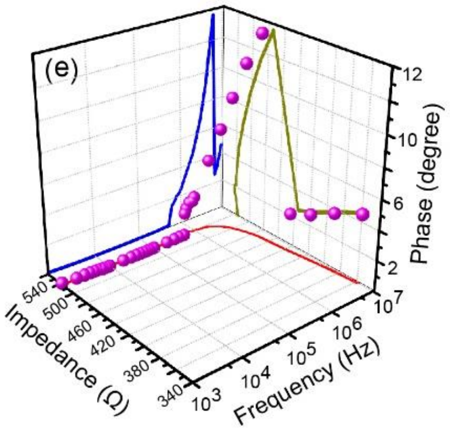
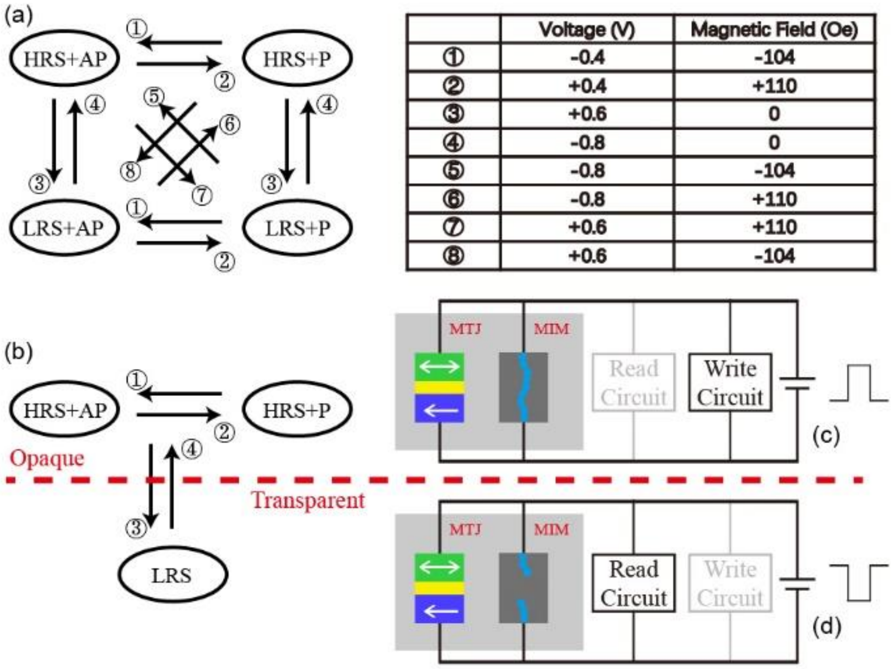


Figure 60 AC-impedance spectroscopy of the device at 20 mV

Results and discussion: logic-in-memory device for memory encryption

The independent control of resistive switching and magnetic switching enables the Re-MTJ as a logic-in-memory device. Figure 61 (a) and (b) present the state transition diagrams of Re-MTJ device under a combination of a voltage and in-plane magnetic fields. Here, the purpose of utilizing a magnetic field is to clearly differentiate between the resistive and magnetic switching process. Regardless of stochastic behaviors, four different resistance states can be achieved as outputs, while the voltage and magnetic field can be used as two corresponding inputs. The results of logic computing can be stored in a combination of MTJ states (e.g. P or AP) and filaments configuration (e.g. HRS or LRS).



	Voltage (V)	Magnetic Field (Oe)
①	-0.4	-104
②	+0.4	+110
③	+0.6	0
④	-0.8	0
⑤	-0.8	-104
⑥	-0.8	+110
⑦	+0.6	+110
⑧	+0.6	-104

Figure 61 State transition diagrams of Re-MTJ device under a combination of voltage and magnetic field. (a) Four resistance states with a combination of configuration of conductive filaments (HRS or LRS) and MTJ (AP or P); (b) Three resistance states for ignoring MTJ states when the conductive filaments are on (LRS). (c) Writing and (d) reading operation of Re-MTJ device for the application as encryption memory.

Furthermore, due to the parallel connection of MTJ and MIM, the difference of resistances between LRS+AP and LRS+P are lower than the counterpart between HRS+AP and HRS+P. By setting the appropriate discrimination for peripheral sensing circuit, we can combine these two states (LRS+AP and LRS+P) together and treat Re-MTJ as a three-state device for simplicity. As shown in Figure 61 (b), when the MIM is in LRS, the conductive filaments are ON and the small difference of resistances between AP and P states can be ignored by the read circuit. Then the Re-MTJ is defined to be in the “transparent” mode, for the fact that the MTJ seems not active. When the MIM is in HRS, the conductive filaments are OFF and the difference of resistances between AP and P states is large enough to be detected by the read circuit. Then we can define that the Re-MTJ is in the “opaque” mode. In this context, the logic function, as a selector of whether the MTJ is readable or not, is accomplished by controlling the configuration of conductive filaments while the information is stored in the MTJ.

This so-called transparent feature makes the Re-MTJ concept an ideal device for realizing the function of NVM encryption. It is of great importance for NVM encryption since the information is kept after powered off, which enables a hacker to extract the sensitive information from the memory with physical access to the system [CHH11, SWA16]. The schematics of write and read circuits are presented in Figure 61 (c) and (d), respectively. As shown in Figure 61 (c), after storing the information into the MTJ, a positive voltage pulse is applied to the Re-MTJ device and then, the MIM is set as LRS. In this situation, the information is encrypted and cannot be read out. Therefore, an encryption process is needed before the next reading operation. To retrieve the information, a negative pulse is applied to the Re-MTJ device and the MIM is reset as HRS, as presented in Figure 61 (d). Then the MTJ becomes readable and the information is decrypted. After the reading operation, the information is encrypted again for data security.

A proof-of-concept of NVM encryption using our Re-MTJ devices with transparent feature was experimentally demonstrated at room temperature. As shown in Figure 62, the data is stored in the MTJ by a magnetic field assisted STT effect, and the conductive filaments controlled by voltages provide a mechanism for data encryption. A -0.9 V voltage pulse resets the MIM to HRS and then the magnetic switching (AP/P) of the MTJ is readable with a resistance difference of ~ 100 Ω between two states (i.e., HRS+AP and HRS+P). Otherwise, a +0.9 V voltage pulse sets the MIM to LRS and then the magnetic switching (AP/P) of the MTJ becomes transparent with the resistance difference of only ~ 30 Ω between two states (i.e., LRS+AP and LRS+P). We note that the resistance difference between HRS+AP and HRS+P can be further improved by the optimization of the device structure and materials, e.g. utilizing a double MgO-based MTJ with tungsten (W) capping layers [LEE16].

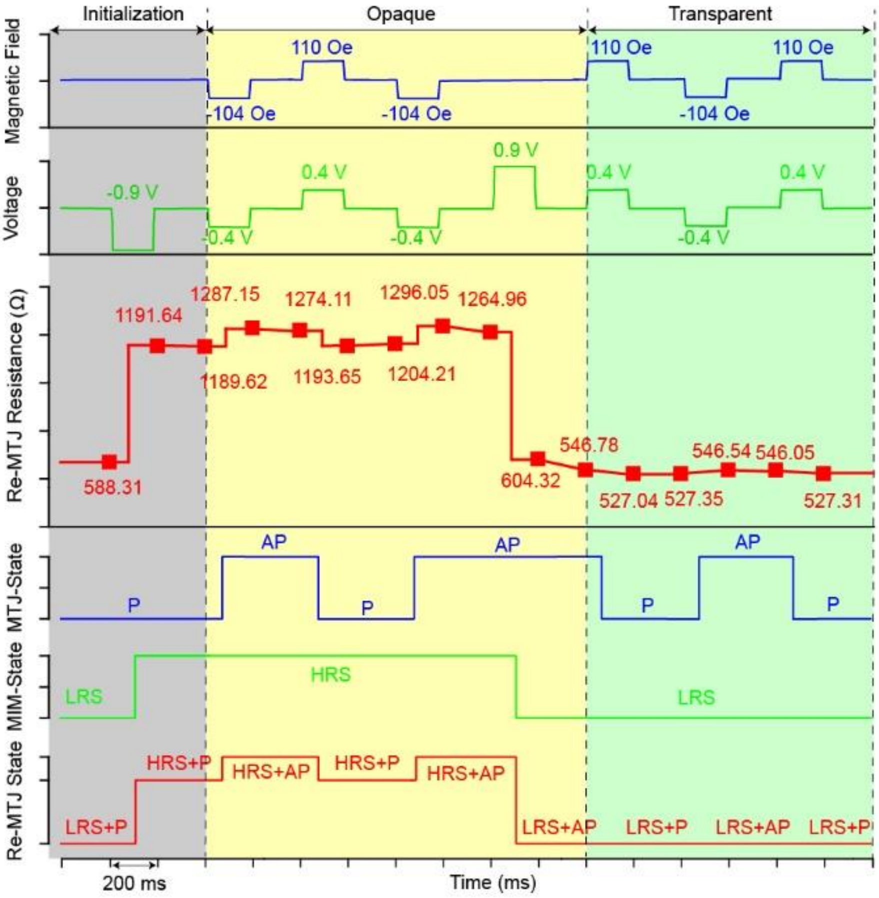


Figure 62 Experimental demonstration of memory encryption function enabled by Re-MTJ device

4.5.2 Normally-off/instant-on function demonstration as a logic-in-memory device

Besides the memory encryption function, the instant-on/normally-off function can be realized by Re-MTJ device as well. Using the compact model showed in Figure 53, a logic-in-memory device was simulated that employs the MTJ for computing and the MIM to memorize the computing results. Figure 63 shows the simulation results, which involves 6 stages: initialization, computing, storing, sleeping, restoring and computing. During the initial phase, the MIM is set to the HRS to initiate computation operations with the MTJ. To perform the computation, several 2 ns pulses of ± 0.4 V are applied to the device to switch the MTJ with low-power energy and a fast speed. Assuming that the computing result is ‘0’ or that the AP state of MTJ is associated with -0.4 V for MTJ switching (marked as operation (2)), the Re-MTJ device transfers the final computing result of the MTJ (AP) into the MIM (LRS) after applying a 10 ns pulse of ±0.9 V (indicated as operation (3)). The device enters a sleep mode, and the data is retained in the MIM without a power supply because of its non-volatility (marked as operation (4)). To enable the device again for the next computing stage, the data stored in the MIM (LRS) are recovered into the MTJ (AP) with a 10 ns pulse of -0.9 V (indicated as operation (5)). Note that if the final computing result of MTJ was the P state or logic ‘1’, there is no need to perform the store and restore operations.

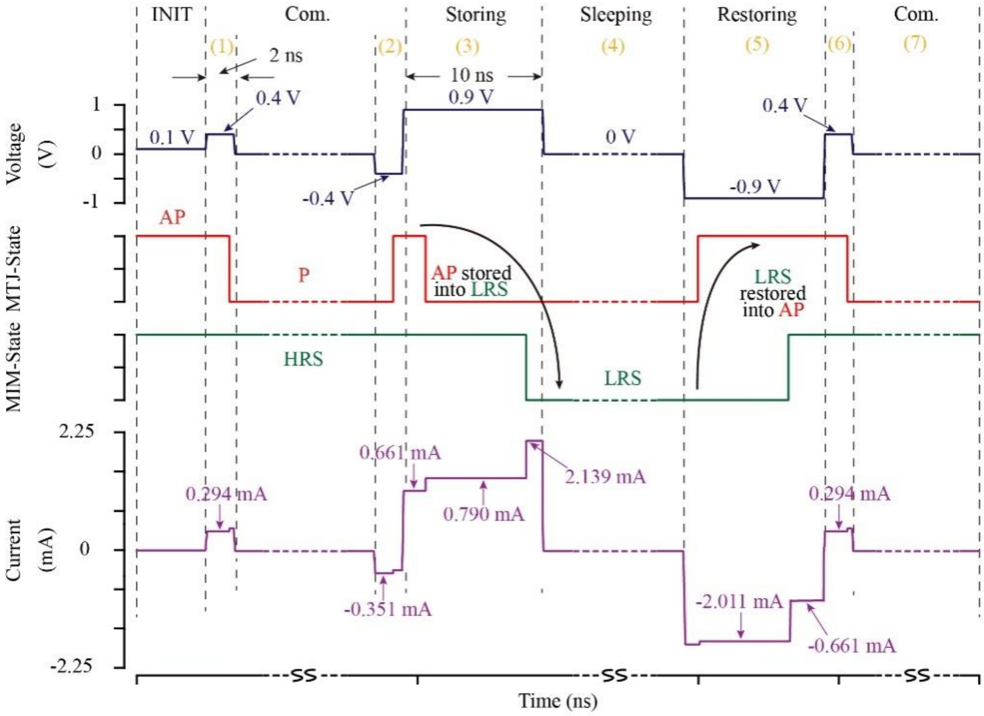


Figure 63 Transient simulation waveform of normally-off/instant-on function using Re-MTJ device. Here, INIT and Com. are the abbreviations of initialization and computing, respectively. The vertical axis labels, Voltage, MTJ-state, MIM-state and Current, stand for the supplied driving voltage across the Re-MTJ device, the resistance state of the MTJ, the resistance stage of the MIM, and the sum of the currents in both MTJ and MIM, respectively.

4.6 Summary

In this chapter, a heterogeneous memristive device, namely Re-MTJ, have been demonstrated combining the merits of MRAM and RRAM in a single element. We have observed both MS and RS in the MTJ nanopillars; we have demonstrated that this behavior originates from the presence of resistive silicon switches, which are located at the edges of the nanopillars possibly induced by damages introduced by the fabrication process. The presence of Si nanocrystals within the SiO_x matrix have been confirmed by an advanced microscopic structure characterizations. We have also reported a rather high ON/OFF ratio up to 1000% and multi-level resistance behavior owing to the point-switching silicon filament process. By taking advantage of the multi-state feature we have demonstrated that the device can be used as a logic-in-memory device with memory encryption function. Different from other NVM devices, the multi-state feature of our Re-MTJ device has some unique features: firstly, the magnetic and resistive switching can be independently controlled; this makes it possible to separate the function of logic and storage in the single element. Secondly, the resistances of MTJ (for both AP and P states) are between the high resistance (when the conductive filaments are off) and low resistance (when the conductive filaments are on) of the MIM; this leads to an interesting transport feature of the Re-MTJ, which results in the different resistance gap for Re-MTJ device with different filament configurations. Based on the transparent feature of Re-MTJ, the function of memory encryption can be realized. We note that memory encryption is of great importance for nonvolatile memories, since the data would be kept even when the power is off. Besides, the normally-off/instant-on function can be realized by the Re-MTJ device as well.

CONCLUSIONS AND PERSPECTIVES

General conclusions

In this thesis, we have focused on the influence of edge damages introduced by the patterning process on the magnetic switching of spintronic nanodevices. Two typical magnetic switching in CoFeB-MgO based structures have been investigated: (i) field-induced switching in magnetic nanodots with PMA and (ii) current-induced switching in MTJ with in-plane magnetization.

We first have developed the full nanofabrication process for both MTJ nanopillars down to 100 nm and magnetic nanodots down to 400 nm. We have shown that a crucial step for nanopillars concerns the optimization of the etching process using ICP and IBE, as well as the encapsulation process with a well-controlled low-temperature curing for spin-on polymer Accuflo. For the magnetic nanodots, a process based on IBE through an Al mask followed by a wet etch of the mask has been also optimized.

First, the magnetization reversal of CoFeB-MgO nanodots with PMA for size ranging from w=400 nm to 1 μm has been studied by Kerr microscopy setup. Contrary to previous experiments, the switching field distribution (SFD) is shifted toward lower magnetic fields as the size of the elements is reduced. Due to the fact that the magnetic anisotropy is altered at the edges of the nanodots due to the etching process, we show that the shifting of the SFD can be explained by the nucleation of a pinned magnetic DW at the edges of the nanodots. As the surface tension (Laplace pressure) applied on the DW increases when reducing the size of the nanodots, we have demonstrated that the depinning field to reverse the entire elements varies as 1/w where w is the size of the nanodots. These results suggest that the presence of DWs has to be considered in the switching process of nanoscale elements. In this case, benefiting from the Laplace pressure and keeping the same thermal stability given by the gradient of anisotropy, a lower switching current would be needed when reducing the size of the devices. This suggest a path toward scalable devices based on controlling artificially the nucleation and pinning potential of DWs at the edges of the elements with nanoscale dimension.

In the second part of this thesis, we have demonstrated that by encapsulating MTJs with SiO_x-based insulator, Si resistive filaments can germinate at the edges of the nanopillars due to damages induced by both the etching and encapsulation process. Based on this feature, we demonstrate a new heterogeneous memristive device composed of a MTJ nanopillar surrounded by resistive silicon switches, named resistively enhanced MTJ (Re-MTJ), which may be utilized for novel memristive memories, enabling new functionalities that are inaccessible for conventional NVMs. The magnetic switching originates from the MTJ, while the resistive switching is induced by a point-switching filament process that is related to mobile oxygen ions. Microscopic evidence of silicon aggregated as nanocrystals along the edges of the nanopillars verifies the synergetic mechanism of the heterogeneous memristive device. The Re-MTJ device features a high ON/OFF ratio of > 1000% and multilevel resistance behavior by combining magnetic switching together with resistive switching mechanisms. This device may provide new possibilities for advanced memristive memory and computing architectures, e.g., in-memory computing and neuromorphics.

In particular, by taking advantage of the multi-states feature of the Re-MTJ devices, it can be used as a logic-in-memory device with memory encryption function. Different from other NVM devices, the multi-states of Re-MTJ has two unique features: firstly, the magnetic and resistive switching can be independently controlled, which makes it possible to separate the function of logic and storage in a single element. Secondly, the two levels of resistances of the MTJ (e.g. P and AP states) are between the high resistance and low resistance of the MIM, which leads to the “transparence” of the stored data. Based on such feature, the function of memory encryption has been experimentally demonstrated. Besides, we show that normally-off/instant-on function can also be realized by such a Re-MTJ device.

Perspectives

In this thesis, we have demonstrated the strong influence of edge damages introduced by the patterning process on the switching behavior of magnetic nanodevices. We have also shown that by taking advantage of the peculiar magnetic properties of the edges, i.e, the reduction of anisotropy for the nanodots and the aggregation of Si nanocrystals together with mobile O ions for the nanopillars, new functionalities compatible with ultimate technology nodes can be developed in spintronic devices.

Below, we propose some points, which can further improve our work.

Perspectives for the Magnetic nanodots

- The smallest dimension of nanodots investigated in this thesis has been 400 nm. It would be interesting to investigate the switching process down to sub-50 nm devices where the dimension of DW becomes comparable to the dot size. In this case, coherent switching would be expected.
- In order to develop scalable devices, it would be interesting to artificially control the gradient of anisotropy at the edges of the nanodots. Current investigation in our laboratory includes in particular local ion irradiation process to monitor DW nucleation and propagation in current-driven DW motion based devices.

Perspectives for the Re-MTJ devices

-It would be necessary to stabilize and optimize the process of forming Si filaments at the edges of MTJ nanopillars.

-The Re-MTJ device, which has been developed here includes a magnetic film stack with an in-plane magnetic anisotropy. To reach ultra-high density and lower critical current, it would be crucial to develop a Re-MTJ device based on perpendicular magnetic anisotropy such as for instance, double MgO-based MTJ including tungsten (W), for which it has been reported enhanced TMR ratio [LEE16]. The increase of the TMR ratio will lead to a larger resistance gap between the AP and P states for applications to memory encryption.

- Considering the heterogeneous structure of Re-MTJ devices and the stochastic behaviors for both resistive and magnetic switching, it can be a potential candidate for brain-inspired applications, e.g. neuromorphic computing [PRE15, QUE15, GRO16, OHS17]. In this context, the MTJ (magnetic component) and MIM (resistive component) can be used to mimic the behavior of neurons and synapses respectively.

-Exploring the circuit-level & system-level application of these effects may be an extension of our work.

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APPENDIX A OVERVIEW OF NANOFABRICATION TECHNOLOGIES

In this section, the important nanofabrication methods and related equipment that I have used during my thesis are introduced.

Film deposition

E-beam Evaporation

Evaporation is a common method for thin-film deposition. The source material is evaporated in a vacuum which allows vapor particles to travel directly to the target object (substrate), where they condense back to a solid state. Evaporation takes place in a vacuum, i.e. vapors other than the source material are almost entirely removed before the process begins. In high vacuum (with a long mean free path), evaporated particles can travel directly to the deposition target without colliding with the background gas. At a typical pressure of 10^{-4} Pa, an 0.4-nm particle has a mean free path of 60 m. Hot objects in the evaporation chamber, such as heating filaments, produce unwanted vapors that limit the quality of the vacuum. Figure 64 shows a typical e-beam evaporation systems. In the MTJ fabrication, the e-beam evaporation is used for deposit the Pt hard mask and the Ti/Au electrodes.

Figure 64 E-beam evaporation setup in C2N

Sputtering

Sputtering is a physical vapor deposition (PVD) process in which a plasma is created and positively charged ions from the plasma are accelerated by an electrical field superimposed on the negatively charged electrode or “target”. The fundamental steps of a sputtering process are as follows:

- Strong electric fields create a plasma for a noble gas (such as Ar gas)
- Ions are accelerated by electric fields
- Accelerated ions hit the target material and the target atoms escape from the target
- Target atoms with momentum move towards the substrate
- Absorption of target atoms by the substrate
- Diffusion of target atoms on the substrate surface
- Nucleation and film formation

Figure 65 shows a classic process for sputtering. The positive ions are accelerated by potentials ranging from a few hundred to a few thousand electron volts and strike the negative electrode with sufficient force to dislodge and eject atoms from the target. These atoms will be ejected in a typical line-of-sight cosine distribution from the face of the target and will condense on surfaces that are placed in proximity to the magnetron sputtering cathode. The targets are fabricated from materials that one subsequently wishes to deposit on the surface of the component facing the electrode. Conductive materials can be deposited using a direct current (DC) power supply and insulators can be deposited by using a radio frequency (RF) power supply.

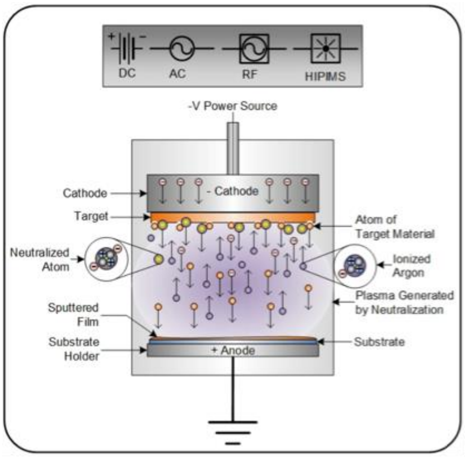


Figure 65 Diagram of the sputtering process. This figure is reproduced from website of http://www.semicore.com/what-is-sputtering.

Magnetron sputtering

The magnetic thin films for spintronic applications, such as MRAM and TMR/GMR sensor, demand for extreme strict sputtering conditions of high vacuum and a good control of thickness and roughness. Therefore, a very low base pressure as a few mTorr is often involved in the chamber, which leads to a lower deposition rate and makes it difficult to create plasma (see Figure 66).

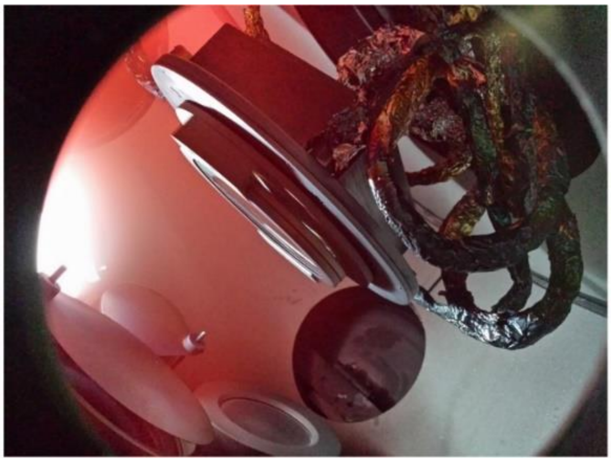


Figure 66 Plasma glow generated during sputtering

To solve this dilemma, a closed magnetic field can be added to the conventional sputtering system to trap electrons, resulting in a magnetron sputtering setup. This extra magnetic field can obviously enhance the efficiency of the initial ionization process and allow a plasma to be generated at lower pressures which reduces both background gas incorporation in the deposited film and energy loses in the sputtered atom through gas collisions. Figure 67 shows the twin-system magnetron sputtering tool from AJA Company.

Figure 67 The AJA sputtering system

Among several film growth technologies, sputtering is an important method since it allows for a precise and versatile control of the properties of magnetic films. Although the lattice structures may be less perfect compared to the films grown with molecular beam epitaxy (MBE), the sputtering method can provide a reasonable deposition rate, which is of great importance for obtaining a good throughout in industries.

After the sputtering, an annealing process is indispensable for CoFeB-MgO based magnetic multilayers to obtain good PMA and high TMR ratio; however, it may be unnecessary for other magnetic material systems, such as $[Co/Pt]_n$ and $[Co/Pd]_n$. In the following discussion, we will use the CoFeB-MgO based magnetic films as an example to illustrate the function of annealing process.

For MTJ based applications, a good lattice structure of CoFeB layer is essential to obtain a high TMR ratio [YUA07]. However, although the lattice structure of MgO layer is bcc (001) after the sputtering, the CoFeB layers remain amorphous. During the annealing process, the boron (B) atoms are driven out of CoFeB layer and absorbed by capping layer, e.g. Tantalum (Ta) layer. Then the left B-poor CoFeB layers will be crystallized and the MgO layer acts as the template, as shown in Figure 68 [YUA07]. We note that the B atoms will diffuse into MgO layer and results in a deterioration of TMR ratio if the annealing temperature is very high.

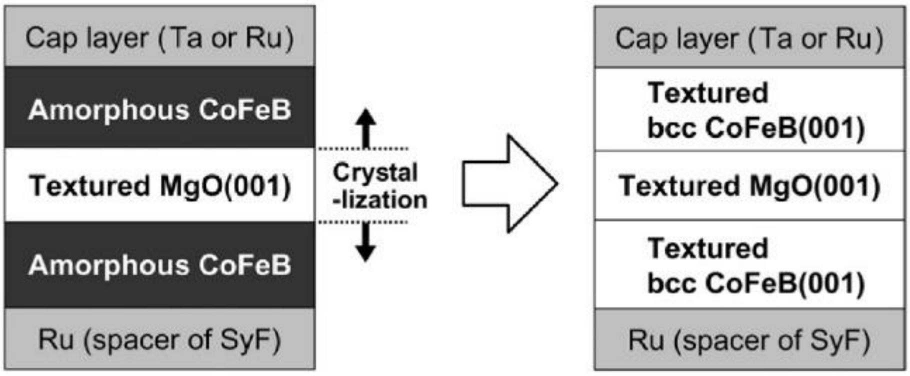


Figure 68 The crystallization of CoFeB during annealing. The Figure is reproduced from Yuasa et al. [YUA07].

Annealing

Moreover, an in-plane external magnetic field is needed during annealing for MTJs with in-plane magnetization. The MTJs with in-plane magnetic anisotropy has a shape of ellipse and the long axis defines the direction of easy axis. In this context, the external magnetic field will lie in the direction of the long axis of ellipse during annealing, which helps to fix the magnetization direction of reference layer in MTJ. Figure 69 shows a commercial products of MVAO annealing system, which is compatible with 8-inch wafers.

Figure 69 MVAO annealing system

Magnetic measurements

After the sputtering and annealing, a series of tests are undergoing for unpatterned wafers to evaluate the quality before patterning. TMR ratio and resistance-area product (RA) are two important parameters for MTJ-based applications. Generally speaking, those parameters can be obtained by transport measurement of a fabricated MTJ device. However, the MTJ fabrication quite complex and it can normally take a few weeks in cleanroom. Besides, Coercivity (H_c) and exchange bias (H_e) are another two important parameters in magnetic switching. For example, a large H_e leads to an increase of the threshold of critical current in a current-induced switching. The vibrating sample magnetometer (VSM) can be used to obtain H_c and H_e. However, the full wafer needs to be sliced into 3 mm in maximum as a magnetic dipole in the measurement. Therefore, technical solutions to measure the magnetic properties of magnetic multilayers as a full wafer is highly desired. In the following, we will see that the two specials tools, e.g. Current-in-plane tunneling (CIPT) and BH looper, can be used to obtain the TMR/RA and H_c/H_e, respectively, at wafer's scale.

As a technology developed by IBM Company, CIPT (see Figure 70) is utilized by the HDD

(TMR sensor) and MRAM companies to obtain the TMR ratio and RA after the film deposition. A published paper [ABR06] of IBM explains why this tool proves useful and effective in the research both for the lab and factory: “It is a simple experimental fact that the more processing an MRAM wafer experiences, the more likely it is that its MTJs will be degraded. This makes it difficult to evaluate MTJ fabrication without influence from subsequent fabrication steps.”

Figure 70 CIPT measurement tool

The wafer is set by a built-in magnetic field in CIPT to the low- and high-resistance states, which are corresponding to the free and reference layers being parallel or anti-parallel. The same process are repeated several times during one measurement. CIPT measurement involves a series of four-point-probe resistance measurements on the surface, as shown in Figure 71 (a) [PRE15].

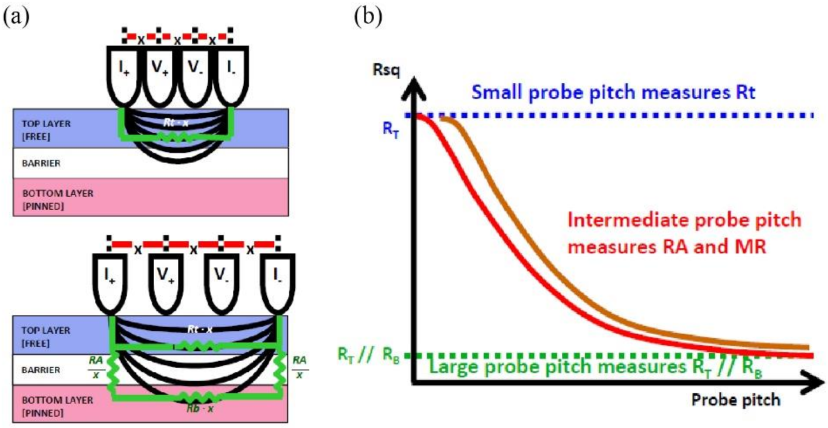


Figure 71 The mechanism of CIPT measurement. The Figure is reproduced from Prejbeanu et al. [PRE15].

For different probe pitch, either R_t, R_b or TMR/RA can be obtained (see Figure 71 (b)). The definition of parameters involved in the CIPT measurement are summarized in Table 5. R_t and R_b are be directly measured by CIPT, as described in reference [ABR06]; other parameters can be calculated by the following two equations:

$$\lambda = \sqrt{\frac{RA}{R_t + R_b}} \tag{A.1}$$

$$R_{1,2} = \frac{\mathrm{V}}{I} = \frac{R_t R_b}{R_t + R_b} \cdot \frac{1}{2\pi} \left\{ \frac{R_t}{R_b} \left[K_0\left(\frac{a}{\lambda}\right) + K_0\left(\frac{c}{\lambda}\right) - K_0\left(\frac{a+b}{\lambda}\right) - K_0\left(\frac{b+c}{\lambda}\right) \right] + \ln\left[\frac{(a+b)(b+c)}{ac}\right] \right\} \tag{A.2}$$

where R_t and R_b are the resistances per square of the top and bottom layers. λ is the length scale, and the distance between I_+ and V_+ is a, V_+ and V_ is b, and V_ and I_ is c. K_0 is the modified Bessel function of the second kind of order zero.

Table 5 Parameters involved in the CIPT measurement

Rt	Ω/□	Resistances per square of the top layers
Rb	Ω/□	Resistances per square of the bottom layers
R_1	$\Omega\mu m^2$	RA_{high}, RA for the AP configuration
R_2	$\Omega\mu m^2$	RA_{low}, RA for the parallel P configuration
MR	----	TMR, MR=100 (RA_{high}-RA_{low}) / RA_{low}

BH looper is a useful tools made by Shb Instruments Company, which can have a quick look for the H_c and H_e before any further fabrication, as shown in Figure 72. The BH looper is adapted for magnetic films over 0.3-nm-thick and the 8-inch wafer in maximum, and the built-in magnetic field can be up to 15 kOe.

Figure 72 BH looper measurement

The VSM measurement can be used to obtain a variety of magnetic parameters including the saturation magnetization (M_s), as shown in Figure 73. In a VSM measurement, the sample is first magnetized in a uniform magnetic field. It is then sinusoidally vibrated, typically through the use of a piezoelectric material. The induced voltage in the pickup coil is proportional to the sample's magnetic moment, but does not depend on the strength of the applied magnetic field. In a typical setup, the induced voltage is measured with a lock-in amplifier using the piezoelectric signal as a frequency reference. It is also possible to record the hysteresis curve of a material by sweeping the magnetic field.

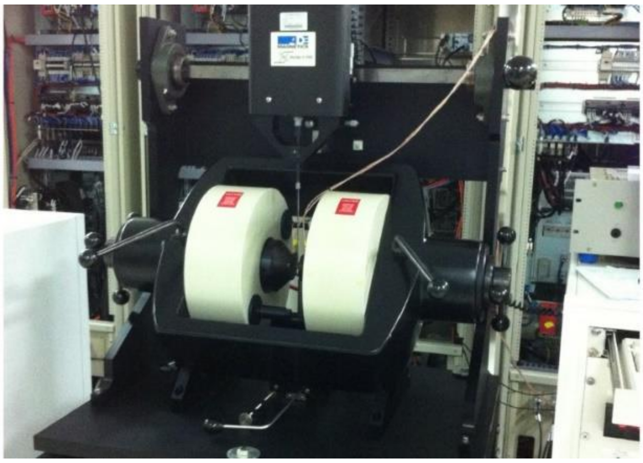


Figure 73 VSM measurement

Following the Moore’s law, the technology node of microelectronics has kept decreasing in decades. Nowadays, the device dimension has shrink into a few nanometers for advanced CMOS technology. Along with the development in nanoscience and nanotechnology, device nanofabrication remains a challenging task.

In addition to the film growth, a series of fabrication process are involved to develop functional magnetic devices. In this section, several important nanofabrication technologies will be introduced.

Lithography

The word of lithography is originated from ancient Greek that the “litho-” means “stone” and the “graphein” means “to write”. The aim of lithography is to mark a particular pattern to record the information. In modern microelectronics industry, lithography technology is a crucial step for transferring the designed patterns to the substrate, which helps to enable the nanodevice with certain functions. Different from the old ages, the engineers use the beam (either photon or electron) to substitute the knife, and use the resist (photoresist or e-beam resist) to substitute the stone. In the following, we will introduce two lithography technologies, e.g. optical lithography and e-beam lithography, which play an important role in determining the minimum technology node for CMOS industry.

Optical lithography

Optical lithography or UV lithography, is a process used in microfabrication to pattern parts of a thin film or the bulk of a substrate. The lithography requires extremely clean operating conditions with yellow light (e.g. cleaning room) and even little dust may ruin the whole pattern. Figure 74 gives an example of optical lithography equipment made by SUSS MicroTec Company.

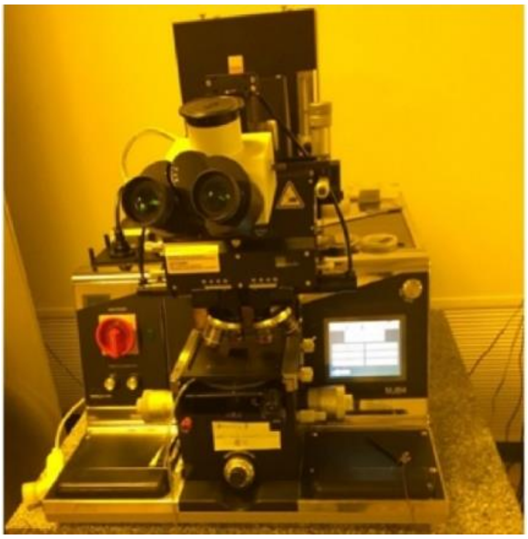


Figure 74 Optical lithography MJB4 in C2N

Optical lithography shares some fundamental principles with photography in that the pattern in the etching resist is created by exposing it to light, either directly (without using a mask) or with a projected image using an optical mask. It uses light to transfer a geometric pattern from a photomask to a light-sensitive chemical “photoresist”, or simply “resist”, on the substrate. A picture of photomask can be seen in the Figure 75. The pattern on the photomask is made of the material of Chrome (Cr) metal, which is opaque to the light. A series of chemical treatments then either engraves the exposure pattern into, or enables deposition of a new material in the desired pattern upon, the material underneath the photo resist.

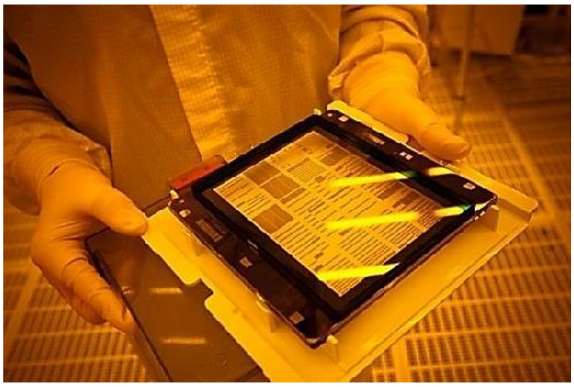


Figure 75 Photomask. The figure is reproduced from the website of Advanced Micro devices.

The photo resists can be roughly divided into two class: the positive one and negative one. For the positive photo resist, the region exposed to the UV light will dissolve in the developer solvent, which means the left patterns on the substrate will be exactly the same as the opaque part in the photomask. On the contrast, for the negative photo resist, the region exposed to the

UV light will be left after the development, which means that the patterns on the substrate will be inversed as the opaque part in photomask.

In complex integrated circuits, a modern CMOS wafer will go through up to 50 times of the photolithographic cycles. The trickiest part in the lithography process is the alignment between each photolithographic cycle. Even a very tiny placement may ruin the narrow patterns under low technology node. In this context, alignment marks are extremely important, which helps to control the deviation of lithography process. Figure 76 gives an example of alignment marks used in the optical lithography. There are several factors which will have an effect on the alignment process accuracy. Among them, the most critical one is that it requires a flat substrate to start with, since it is ineffective at creating shapes in lithography when the substrates are not flat (For the optical lithography, the flat substrate is necessary for the alignment and for electron beam lithography (EBL), the accuracy of the exposure dose is directly related to the roughness of the substrate). This is the reason why a planarization process (e.g. spin-on glass or chemical mechanical polishing, CMP) is needed in the microelectronic.

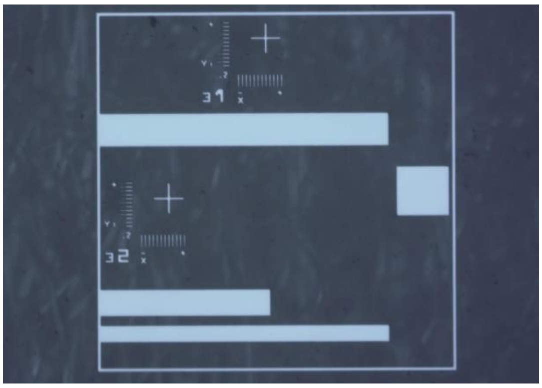


Figure 76 Alignment marks in photomask

E-beam lithography

Due to the limitation of the resolution in optical lithography, extremely fine patterns (~100 nm) needs to be created by electron beam lithography (EBL), which is a fundamental technique of nanofabrication, allowing the direct writing of structures down to sub-10 nm dimensions. Derived from the early scanning electron microscopes, the technique in brief consists of scanning a beam of electrons across a surface covered with a resist film sensitive to those electrons, thus depositing energy in the desired pattern in the resist film. The main attributes of the technology are: 1) it is capable of very high resolution; 2) it is a flexible technique that can work with a variety of materials; 3) it is slow, being one or more orders of magnitude slower than optical lithography and 4) it is expensive and complicated: electron beam lithography tools can cost many millions of dollars and require frequent service to stay properly maintained. Figure 77 (a) shows the schematic diagram of the EBL systems and (b) shows an EBL system made by NANOBEAM Company.

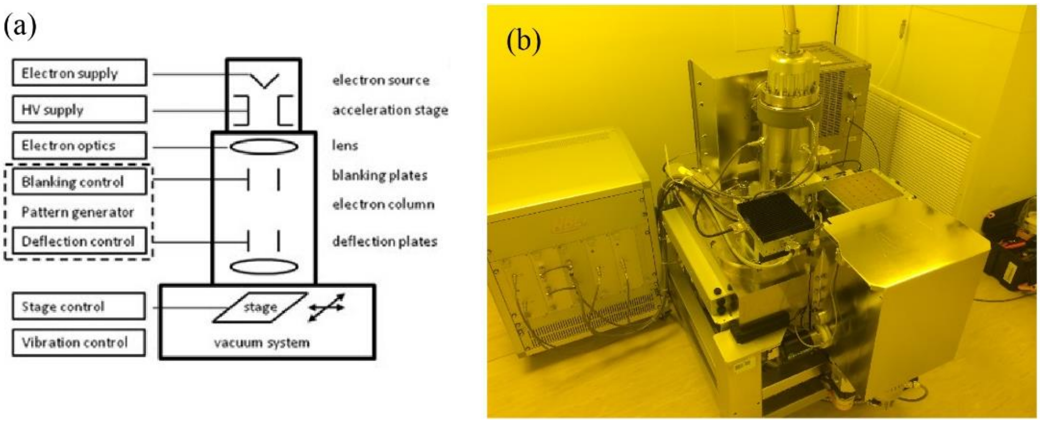


Figure 77 Schematic diagram of an EBL system (b)The e-beam lithography NB4 in C2N

Etching

After the lithography (e.g. optical lithography or e-beam lithography) process, the pattern has to be transferred from the photomask/designed layout to the resist. After that, an etching process will further enable the pattern to be transferred to substrate. Etching is used in micro- and nanofabrication to chemically remove layers from the surface of a wafer during manufacturing. For many etch steps, part of the wafer is protected from the etchant by a “masking” material which resists etching. In some cases, the masking material is a photoresist which has been patterned using photolithography. Other situations require a more durable mask, such as silicon nitride or metal materials like Pt or Ta; and those durable mask is also be called the “hard mask”. If the etch is intended to make a cavity in a material, the depth of the cavity may be controlled approximately using the etching time and the known etch rate. More often, though, etching must entirely remove the top layer of a multilayer structure, without damaging the underlying or masking layers. The etching system's ability to do this depends on the ratio of etch rates in the two materials, which is defined as the etching selectivity. The two fundamental types of etchants are liquid-phase (e.g. wet etch) and plasma-phase (e.g. dry etch).

In the MTJ patterning process, two kinds of etching process are needed: firstly, an inductive coupling plasma (ICP) etching will transfer the pattern to a mask layer, which is often make of metal or SiO_2; secondly, an ion beam etching will further transfer the pattern finally to the multilayers.

Wet etch

For wet etch, the wafer can be immersed in a bath of etchant, which must be agitated to achieve good process control. Wet etchants are usually isotropic, which leads to large bias when etching thick films. They also require the disposal of large amounts of toxic waste. For these reasons, they are seldom used in state-of-the-art processes. However, in some particular situation, the wet etch is also preferred. For example, a wet etch process is involved for the removal of hard mask after dry etching. This is because the resist can become really tough after suffering the heat and ion irradiation during the process of dry etch. Since some materials (i.e. ferromagnetic metal) are sensitive to the oxygen or halogen-based gas, wet etch can be a gentle way to remove the used mask. As an example in magnetic nanodots fabrication, after using Al as mask for IBE, a MF-CD-26 developer is utilized for removing the left mask.

Inductive coupling plasma etching

Inductive coupling plasma (ICP or ICP-RIE), can be seen as a special kind of reactive-ion etching (RIE). As dry etching, RIE uses chemically reactive plasma to remove material deposited on wafers. The plasma is firstly generated under low pressure (vacuum) by an electromagnetic field, and then high-energy ions from the plasma attack the wafer surface and react with it. Furthermore, if the plasma is generated with an RF powered magnetic field, it becomes an ICP-RIE system. Figure 78 (a) shows an ICP system made in STS Company. In this system, the ICP generator is employed as a high density source of ions which increases the etch rate, whereas a separate RF bias (CCP generator) is applied to the substrate to create directional electric fields near the substrate to achieve more anisotropic etch profiles, as shown as Figure 78 (b).

In the MTJ fabrication, the ICP is used for etching the mask Ta with a mixture of SF_6 and Ar gases, and also for the etching of encapsulation layer Accuflo with a mixture of O_2 and Ar.

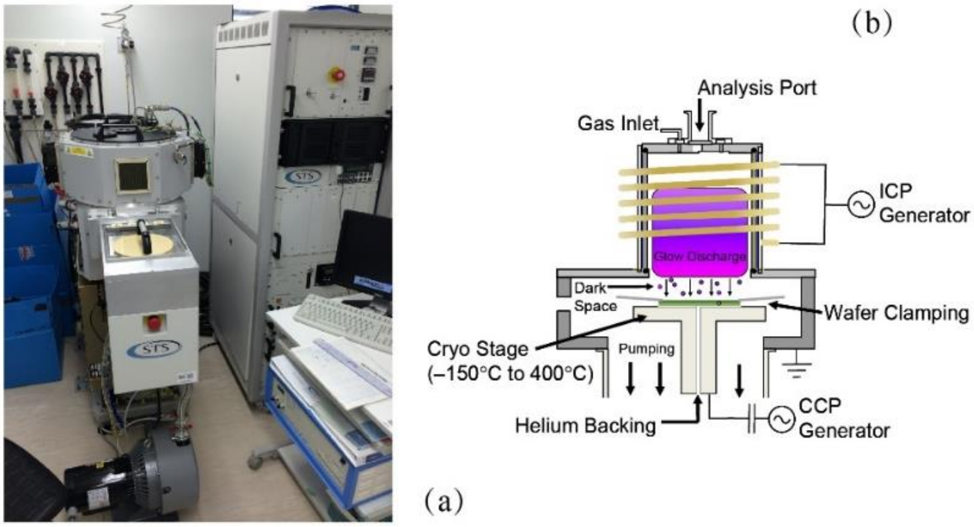


Figure 78 (a) ICP system in C2N. (b) Schematic of a cross-sectional view of an ICP instrument. The figure is reproduced from Shearn et.al [SHE10]

Ion beam etching

Ion beam etching (IBE) is an anisotropic etching process that faithfully reproduces the mask pattern on the product. An ion beam is used to sputter etch material exposed by a mask (e.g. resist) to obtain the desired pattern. Patterns are superimposed onto a substrate using thin film technology. Photo resist is spun onto the substrate and cured (soft bake). A Chrome on Quartz master mask is used to transfer the desired pattern onto the photo resist layer. For a negative mask resist, an Ultra Violet (UV) lamp source photo-polymerizes the photo resist areas exposed by the master mask. After exposure, the un-exposed photo resist is washed away with a developer solution. A positive mask exposure is the inverse process where the UV exposed photo resist is developed and washed away. Once the excess resist has been washed away, the substrate is cured in an oven (hard bake) and then mounted onto a fixture for ion milling. This process is illustrated in Figure 79.

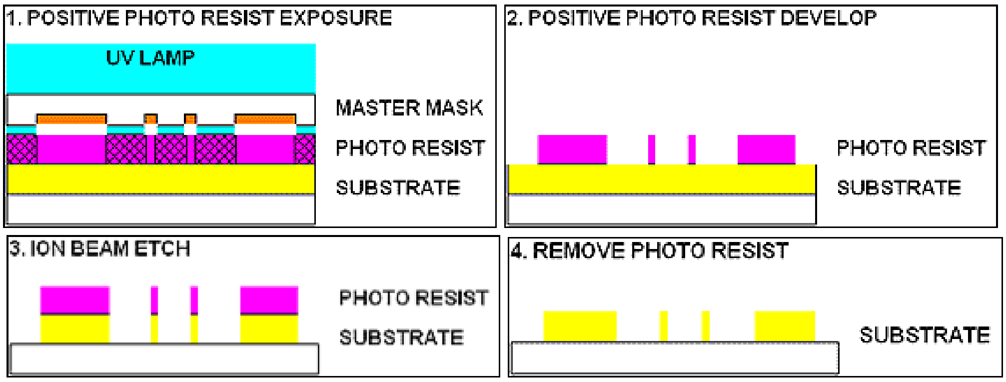


Figure 79 Schematic of IBE process. The figure is reproduced from the website of http://www.microfabnh.com/ion_beam_etch_technology.php

For ICP-RIE, the plasma generated from reactive gases are involved in etching process, which may cause the deterioration of the magnetic properties of multilayers. This is the case that the halogen-based gas ions may damage the CoFe(B) layer in MTJ fabrication. Different from the ICP-RIE, the IBE technology only use the Ar ions (Ar^+) to sputter (milling) the sample surface physically, which makes it an ideal method for the etching of ferromagnetic materials. Figure 80 shows an IBE system with secondary ion mass spectroscopy (SIMS) for end-point detection.

Figure 80 IBE system with SIMS in C2N

In the MTJ fabrication, the IBE process is used to etch the core structure of the MTJ stack, especially the CoFeB and MgO layers. In the process, a Ta layer is involved as the mask to define the ellipse shape of the tunnel junction. The redeposition on the sidewall is a critical issue, since it may lead to a short cut for the device. We will avoid this problem by adjusting the etching angle during the IBE.

Encapsulation

After the definition of the device's pattern, an encapsulation process is required to protect the device from oxidization. For the MTJ fabrication, a planarization process using spin-on materials has been chosen in this thesis. Compared to other encapsulation methods such like sputtering or plasma enhanced chemical vapor deposition (PECVD), the planarization process using spin-on materials is more convenient as it only demands a spin-coating process and a low-temperature curing process with hotplate, as shown in the Figure 81. In the following, we give a brief introduction of the spin-coating process

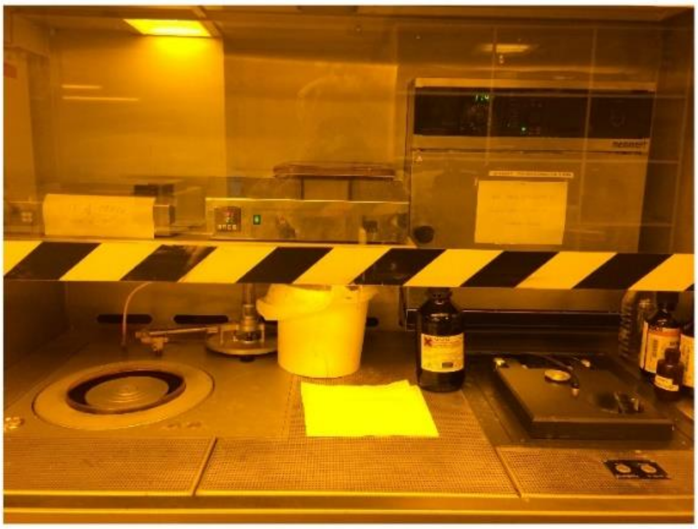


Figure 81 The spin-coating setup in C2N

Spin coating has been used for several decades for the application of thin films. A typical process involves depositing a small puddle of a fluid resin onto the center of a substrate and then spinning the substrate at high speed (typically around 3000 rpm). Centripetal acceleration will cause the resin to spread to, and eventually off, the edge of the substrate leaving a thin film of resin on the surface, as shown as in Figure 82. Final film thickness and other properties will depend on the nature of the resin (viscosity, drying rate, percent solids, surface tension, etc.) and the parameters chosen for the spin process. Factors such as final rotational speed, acceleration, and fume exhaust contribute to how the properties of coated films are defined.

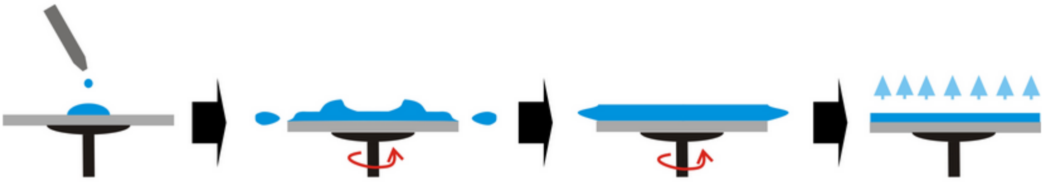


Figure 82 Schematic of spin-coating process. The figure is reproduced from the Internet.

Device profile characterization

After the device fabrication, the characterization of the devices is needed to check the quality of the process and to analyses the reason of failure if needed. In this section, we will introduce two important electron microscopy technologies for characterizing the profile of the device, e.g. the scanning electron microscope and transmission electron microscope.

Scanning electron microscope

As shown in Figure 83, scanning electron microscope (SEM) is a type of electron microscope that produces images of a sample by scanning the surface with a focused beam of electrons. The electrons interact with atoms in the sample, producing various signals that contain information about the sample's surface topography and composition. The electron beam is scanned in a raster scan pattern, and the beam's position is combined with the detected signal to produce an image. SEM can achieve resolution better than 1 nanometer. For most SEM systems, energy dispersive X-Ray spectroscopy (EDX) can be added for the material analysis. In MTJ fabrication process, SEM is a useful methods to check the fabricated patterns.

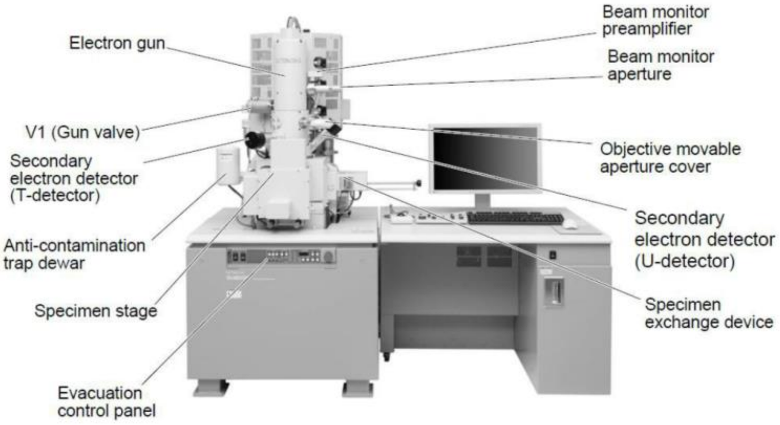


Figure 83 Schematic of SEM SU-8000 made by Hitachi Company. The figure is produced from the Internet.

Transmission electron microscope

Generally speaking, the SEM system can be used to observe a structure with a dimension over a few tens of nanometer. If we want to go deeper for smaller structure, such as the lattice structure of the MTJ stack, a transmission electron microscope (TEM) is dispensable, as shown in the Figure 84. Moreover, as a profile characterization technology, the SEM can be used to check the device pattern. However, once the encapsulation process has been done, the information of the device structure will be hidden below the encapsulation layer. In this case, a cross-sectional TEM image will provide the information of the inner structure of the device.

TEM is a microscopy technique in which a beam of electrons is transmitted through a specimen to form an image. The specimen is most often an ultrathin section less than 100 nm thick or a suspension on a grid. Sample preparation in TEM can be a complex procedure, often including the ion milling and focus ion beam etching (FIB). High quality samples will have a thickness that is comparable to the mean free path of the electrons that travel through the samples, which may be only a few tens of nanometers. An image is formed from the interaction of the electrons with the sample as the beam is transmitted through the specimen. The image is then magnified and focused onto an imaging device, such as a fluorescent screen, a layer of photographic film, or a sensor such as a charge-coupled device. Furthermore, energy dispersive spectrometer (EDS) and electron energy loss spectroscopy (EELS) measurement can be utilized with the TEM to analyses the material properties at specific pot of the sample.

Figure 84 The TEM system JEOL JEM-ARM200F. The figure is produced from the Internet.

APPENDIX B LIST OF ABBREVIATIONS

AFM	atomic force microscope
AP	anti-parallel
bcc	body-centered cubic
BEOL	back-end-of-line
BPM	bit pattern media
CIMS	current-induced magnetization switching
CIPT	current-in-plane tunneling
CMOS	complementary metal oxide semiconductor
CMP	chemical mechanical polishing
DRAM	dynamic random access memory
DC	direct current
DW	domain wall
EBL	electron beam lithography
EDX	energy dispersive X-Ray spectroscopy
EDS	energy dispersive spectrometer
EELS	electron energy loss spectroscopy
FeRAM	ferroelectric memory
FFT	fast Fourier transformation
FIMS	field induced magnetic switching
FIB	focus ion beam etching
FM	ferromagnetic
GMR	giant magnetoresistance
HRS	high-resistance state
HRTEM	high-resolution TEM
IBE	ion beam etching
ICP	inductive coupling plasma
LRS	low-resistance state
MOKE	magneto-optic Kerr effect
MRAM	magnetic random access memory
MIM	metal-insulator-metal
MS	magnetic switching
MTJ	magnetic tunnel junction
NM	non-ferromagnetic
NVM	nonvolatile memory
P	parallel
PCM	phase change memory
PMA	perpendicular magnetic anisotropy
PVD	physical vapor deposition
RA	resistance-area product
Re-MTJ	resistively enhanced MTJ
RF	radio frequency
RRAM	resistive random access memory
RS	resistive switching
SEM	scanning electron microscope
SFD	switching field distribution

SIMS	secondary ion mass spectroscopy
SRAM	static random access memory
STT	spin transfer torque
STT-MRAM	spin-transfer torque MRAM
TEM	transmission electron microscope
TMR	tunneling magnetoresistance
UV	ultra violet
VIRS	voltage-induced resistive switching
VSM	vibrating sample magnetometer

APPENDIX C LIST OF PUBLICATIONS

Journals

[1] **Zhang Y**, Lin X, Adam J P, et al. Heterogeneous Memristive Devices Enabled by Magnetic Tunnel Junction Nanopillars Surrounded by Resistive Silicon Switches[J]. Advanced Electronic Materials, 2018, 4 (3): 1700461. (**Cover Picture of Adv. Electron. Mater. 3/2018**) (IF: 5.466, JCR: Q1)

[2] **Zhang Y**, Zhang X, Vernier N, et al. Domain Wall Motion Driven by Laplace Pressure in CoFeB-MgO Nanodots with Perpendicular Anisotropy[J]. Physical Review Applied, 2018, 9(6): 064027. (IF: 4.782, JCR: Q1)

[3] **Zhang Y**, Cai W, Kang W, et al. Demonstration of Multi-state Memory Device Combining Resistive and Magnetic Switching Behaviors[J].IEEE Electron Device Letters, 2018, 39(5): 684-687. (IF: 3.433, JCR: Q1)

[4] Peng S, **Zhang Y**, Wang M, et al. Magnetic Tunnel Junction for Spintronics: Principles and Applications[M]. Wiley Encyclopedia of Electrical and Electronics Engineering 1936, 1-16, 2014.

[5] Cao A, Zhang X, Koopmans B, Peng S, **Zhang Y**, et al. Tuning the Dzyaloshinskii-Moriya Interaction in Pt/Co/MgO heterostructures through MgO thickness[J]. Nanoscale, 2018.

[6] Zhang X, Cai W, Zhang X, Wang Z, Li Z, **Zhang Y**, et al. Skyrmions in magnetic tunnel junctions[J]. ACS applied materials & interfaces, 2018.

[7] Wei J, Fang B, Wu W, Cao K, Chen H, **Zhang Y**, et al. Amplitude and Frequency Modulation Based on MSN, submitted.

[8] Zhao W, Zhao X, Zhang B, Cao K, Wang L, Kang W, Shi Q, Wang M, **Zhang Y**, et al. Failure Analysis in Magnetic Tunnel Junction Nanopillar with Interfacial Perpendicular Magnetic Anisotropy[J]. Materials, 2016, 9(1):41.

Conferences

[1] **Zhang Y**, Adam J P, Cai W, et al. Ultra High TMR Magnetic Tunnel Junction Nano-Pillar with CoFe Insertion Layer between MgO and CoFeB[A]. IEEE International Magnetics Conference (Intermag)[C]. Dublin, Ireland, April 24-28, 2017. (**Oral presentation**, EF-06, 27/04/2017)

[2] **Zhang Y**, Zhang X, Vernier N, et al. Domain Wall Motion Driven by Laplace Pressure in CoFeB-MgO Nanodots with Perpendicular Anisotropy[A]. IEEE International Magnetics Conference (Intermag)[C]. Singapore, April 23-27, 2018. (**Oral presentation**, GC-01, 27/04/2018)

Patents

[1] **Zhang Y**, Zhao W, Zhang B, Zhang Y-G. A magnetic memory based on the control voltage: Chinese Patent CN103794715B[P]. 2014-2-28.

[2] **Zhang Y**, Zhao W, Wang M, Guo W, Zhang Y-G. An information memory device and sensing and preparation method: Chinese Patent CN104134748B[P]. 2014-7-17.

[3] Zhao W, **Zhang Y**, Wang M. Manufacturing method for embedding type magnetic tunnel junction device comprising dielectric layers: Chinese Patent CN103794717A[P]. 2014-2-28.

Workshops and Summer schools

[1] IEEE Magnetics Society Summer School, University of Minnesota, Minneapolis, United States, 2015.

[2] JournéesNationales du Réseau Doctoral enMicroélectronique (JNRDM), Bordeaux, France, 2015.

[3] Introductory course on Magnetic Random Access Memory (InMRAM), Grenoble, France, 2015.

Résumé en français

Motivation

Les mémoires courantes sont limitées en vitesse, puissance et endurance (Flash, EEPROM) ou ne peuvent pas conserver les données sans alimentation (SRAM, DRAM). En outre, elles s'approchent des limites de mise à l'échelle physique. Des mémoires non-volatiles (*Non-volatile memories, NVM*) combinées à de nouvelles architectures informatiques ont été considérées récemment comme la solution la plus prometteuse pour surmonter le «mur de mémoire» dans les systèmes informatiques de von-Neumann [Lin12, Yan13, WON15]. Par exemple, les architectures informatiques en mémoire construites par l'intégration de NVM rapides avec des fonctions logiques ont été proposées pour minimiser la consommation d'énergie et ouvrir la voie à l'informatique normalement bloquée/allumage instantanée [BOR10, SHU17]. Dans le même temps, l'informatique neuromorphique inspirée par le cerveau humain exploite les caractéristiques résistives des NVM en tant que synapses et neurones artificiels, il a déjà déclenché une révolution pour les architectures non-von-Neumann [LOC13, GRO16, PRE15]. Dans cette direction, la mémoire MRAM *(magnetic random access memory)* et la mémoire RRAM *(resistive random access memory)* [WON15, WON12, LIN14, CEL14] ont suscité un intérêt croissant.

Les technologies MRAM auraient de nombreuses applications dans plusieurs domaines. Jusqu'à présent, les grandes entreprises de microélectronique travaillent sur la R&D de STT-MRAM *(spin transfer torque, STT)* basé sur CoFeB-MgO au nœud technologique de 16 nm et au-delà [DIE17]. L'entreprise Everspin commercialise actuellement des mémoires autonomes de 256 Mo et a coopéré avec GlobalFoundries pour produire des mémoires intégrées pour microcontrôleurs *(micro-controller units, MCU)*. Afin de répondre à la demande d'applications à haute densité, telles que le remplacement de DRAM, la dimension de la cellule mémoire de STT-MRAM doit être réduite vers des nœuds technologiques encore plus petits (et un pitch plus petit). Cependant, la variabilité structurelle des matériaux magnétiques (rugosité d'interface, texture cristalline, joints de grains, ...) conduit à une répartition des propriétés magnétiques (magnétorésistance tunnel (TMR), anisotropie, amortissement, ...), ce qui limite le développement des STT-MRAM au-delà du nœud de 20 nm. De plus, avec la diminution de la taille des dispositifs magnétiques, l'influence des dommages aux bords introduits par le processus de nanofabrication devient une limitation cruciale pour cette technologie. En particulier, le processus de gravure des nanopiliers s'est avéré être la principale limitation pour le développement de cellules STT-MRAM sub-20 nm, car une pile typique de jonction tunnel magnétique *(magnetic tunnel junctions, MTJ)* contient plus de 10 matériaux différents.

L'objectif principal de cette thèse est de mettre en évidence l'influence des dommages aux bords introduits par les processus de nanofabrication sur le comportement de commutation des nanodispositifs magnétiques. Deux commutations magnétiques typiques ont été étudiées: (i) commutation induite par le champ dans les nanodots magnétiques avec anisotropie magnétique perpendiculaire (*perpendicular magnetic anisotropy, PMA*) et (ii) commutation induite par le courant dans les jonctions tunnel magnétiques avec aimantation dans le plan. Afin d'étudier ces deux types de nanodispositifs, une grande partie de mon travail de recherche a été consacrée au développement du procédé de nanofabrication en utilisant les installations avancées dans la salle blanche de C2N (Centre de Nanosciences et de Nanotechnologies). Enfin, après avoir souligné l'influence des dommages aux bords sur la commutation magnétique, de nouvelles fonctionnalités dans les nanodispositifs spintroniques sont discutées en profitant de cette influence.

Nanofabrication de nanopiliers MTJ et nanodots magnétiques

Dans la première partie de cette thèse, nous discutons des dépôts de couche mince et les méthodes de caractérisation. Afin d'obtenir des multicouches magnétiques de haute qualité, un vide poussé et strict contrôle de l'épaisseur de couche pendant le dépôt sont nécessaires. Pour atteindre un rapport TMR élevé dans le système de matériau à base de CoFeB-MgO, un processus de recuit à température modérée est également nécessaire pour fournir une bonne cristallinité de la couche CoFeB. La figure 1 montre les images TEM transversales d'un dispositif MTJ (figure 1 (a)) et la structure cristalline de la pile MTJ.

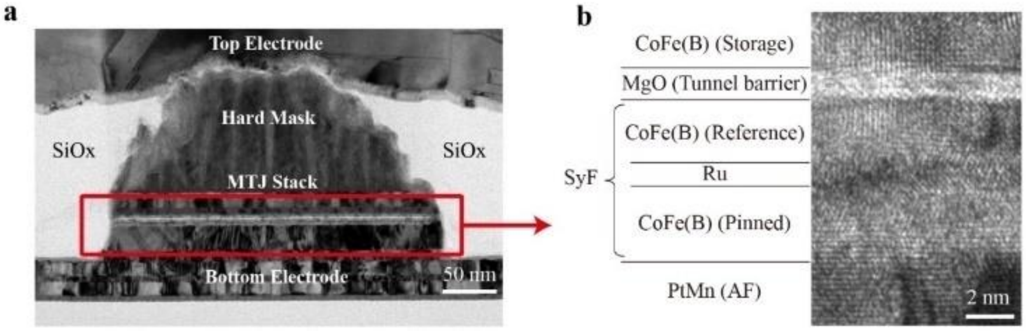


Figure 1 Images TEM transversales de MTJ

Ensuite, nous avons développé le procédé complet de nanofabrication pour des nanodots magnétiques de taille minimale de 400nm et des nanopiliers MTJ de taille minimale de 100nm. Pour les nanodots magnétiques, un procédé basé sur la gravure ionique *(ion beam etching, IBE)* à travers un masque Al suivi d'une gravure humide de ce masque est utilisé, ce qui peut satisfaire aux exigences du système de microscopie Kerr. La figure 2 montre la caractérisation du profil des nanodots.

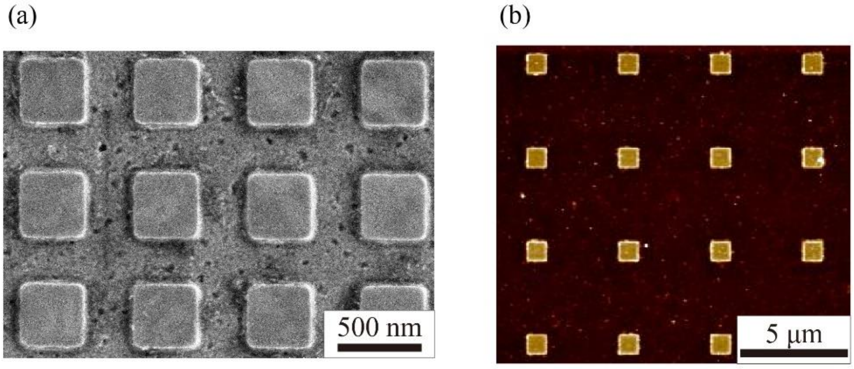


Figure 2 (a) Image au microscope électronique à balayage de nanodots de 400 nm (b) image au microscope à force atomique des nanodots de 1 µm

Pour des nanopiliers MTJ, nous avons montré qu'une étape cruciale concerne l'optimisation du processus de gravure en utilisant ICP-RIE et IBE, ainsi que le processus d'encapsulation avec un durcissement bien contrôlé à basse température d’enduction centrifuge de polymère Accuflo. La figure 3 montre l'image TEM du dispositif MTJ fabriqué de taille 80 nm × 200 nm.

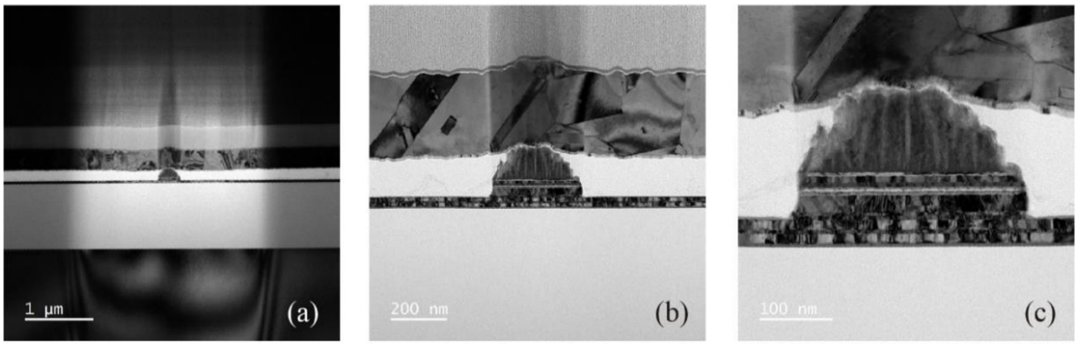


Figure 3 Images TEM transversales du nanopilier MTJ de taille 80 nm × 200 nm observées sous différentes échelles

Inversion de l'aimantation des nanodots régie par la pression de Laplace

Dans la seconde partie de cette thèse, inversion de l'aimantation des CoFeB-MgO nanodots avec PMA pour taille allant de w = 400 nm à 1 µm a été étudiée par microscopie Kerr. Contrairement aux expériences précédentes, la distribution du champ de commutation (switching field distribution, SFD) est décalée vers les champs magnétiques inférieurs lorsque la taille des éléments est réduite, comme le montre la figure 4.

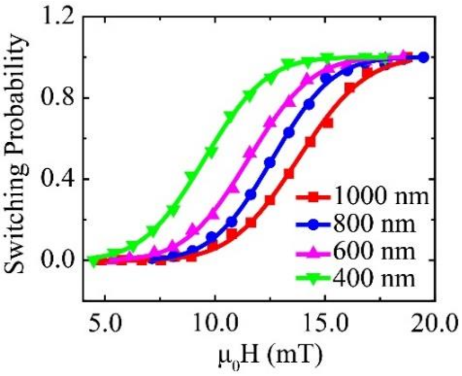


Figure 4 Probabilité de commutation moyenne en fonction du champ magnétique

Considérant que l'anisotropie magnétique est modifiée aux bords des nanodots après le processus de gravure, nous montrons que le décalage du SFD peut être expliqué par la nucléation et l'épinglage de paroi de domaine (domain wall, DW) sur les bords des nanodots. Comme la tension de surface (pression de Laplace) appliquée sur le DW augmente quand la taille des nanodots se réduit, nous avons démontré que le champ de dépinglage pour inverser les nanodots varie en fonction de 1/w, où w est la taille des nanodots. La figure 5 montre le processus de commutation magnétique induit par le champ, en particulier le processus de dépinglage de DW, d'un nanodot prenant en compte la pression de Laplace.

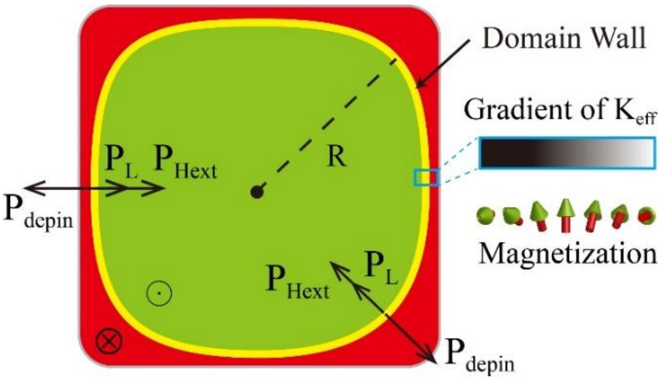


Figure 5 Schéma du processus d'inversion de l'aimantation d'un nanodot
Un DW circulaire (jaune) de rayon R est situé au bord du nanodot, séparant les régions inversées (rouge) et non inversées (vert). Le DW est épinglé par un gradient d'anisotropie sur une échelle de longueur comparable à DW en raison de dommages aux bords. P_{depin}, P_{Hext} et P_L correspondent respectivement aux pressions appliquées sur le DW dues à l'épinglage, au champ magnétique externe et à la pression de Laplace.

Ces résultats indiquent que la présence de DW doit être considérée dans le processus de commutation des éléments nanométriques. Dans ce cas, bénéficiant de la pression de Laplace donnée par le gradient d'anisotropie, un courant de commutation plus faible serait nécessaire lors de la réduction de la taille des dispositifs tout en gardant la même stabilité thermique. Ceci ouvre la voie à des dispositifs miniature basés sur le contrôle artificiel du potentiel de nucléation et épinglage des DW aux bords des éléments à dimension nanométrique.

Dispositif MRAM résistiquement amélioré

Dans la troisième partie de cette thèse, nous avons démontré qu'en encapsulant des MTJ avec un isolant à base de SiOx, les filaments résistifs Si peuvent germer sur les bords des nanopiliers en raison de dommages induits par le processus de gravure. Basé sur cette caractéristique, nous démontrons un nouveau dispositif memristive hétérogène composé d'un nanopilier MTJ entouré de commutateurs résistifs de silicium, appelé MTJ résistiquement amélioré (*resistively enhanced MTJ, Re-MTJ*), comme le montre la figure 6, qui peut être utilisé pour de nouvelles mémoires memristive. La commutation magnétique provient du MTJ, tandis que la commutation résistive est induite par un processus de filament à commutation de points qui est lié aux ions d'oxygène mobiles. La preuve microscopique de silicium agrégé sous forme de nanocristaux le long des bords des nanopilier vérifie le mécanisme synergétique du dispositif memristive hétérogène. Le dispositif Re-MTJ présente un rapport ON / OFF élevé plus de 1000% et un comportement de résistance à plusieurs niveaux en combinant la commutation magnétique avec des mécanismes de commutation résistifs.

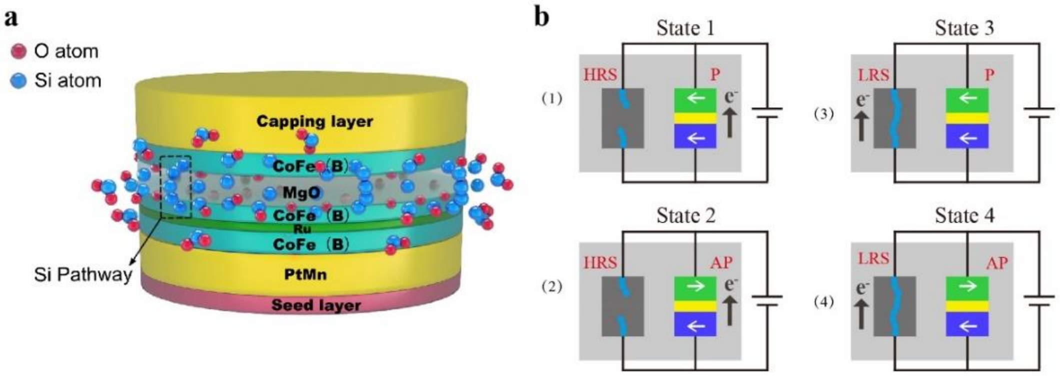
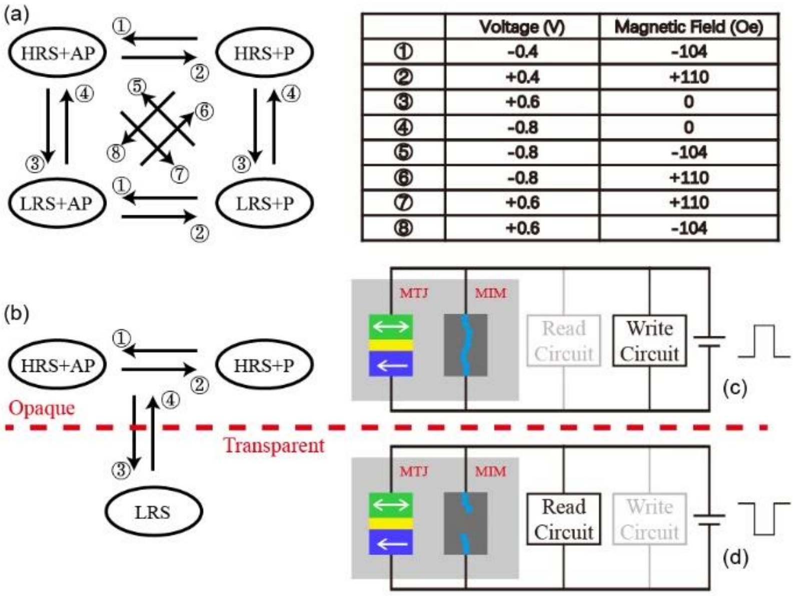


Figure 85 Modèle de dispositif de Re-MTJ

(a) Schéma du nanopilier MTJ entouré de filaments Si. Les boules bleues et rouges représentent les atomes de Si et O, respectivement. (b) Modèle physique correspondant à un élément RRAM en parallèle avec un élément MRAM. Selon la configuration des éléments RRAM et MRAM, quatre états différents peuvent être obtenus dans le dispositif Re-MTJ. Les billes bleues représentent les filaments conducteurs qui forment la voie Si.

En particulier, en tirant avantage de la fonctionnalité multi-états des dispositifs Re-MTJ, il peut être utilisé comme un dispositif logique en mémoire avec une fonction de cryptage de la mémoire. Différents des autres dispositif NVM, les multi-états de Re-MTJ ont deux caractéristiques uniques: premièrement, la commutation magnétique et résistive peut être contrôlée indépendamment, ce qui permet de séparer la fonction de logique et de stockage dans un seul élément. Deuxièmement, les deux niveaux de résistances de la MTJ (i.e. les états P et AP) sont entre la résistance élevée et la résistance faible du métal-isolant-métal (MIM), ce qui conduit à la "transparence" des données stockées, comme montré dans la figure 7. Sur la base de cette caractéristique, la fonction de cryptage de la mémoire a été démontrée expérimentalement. En outre, nous montrons que la fonction de normalement bloqué/allumage instantané peut également être réalisée par un tel dispositif Re-MTJ.



	Voltage (V)	Magnetic Field (Oe)
①	-0.4	-104
②	+0.4	+110
③	+0.6	0
④	-0.8	0
⑤	-0.8	-104
⑥	-0.8	+110
⑦	+0.6	+110
⑧	+0.6	-104

Figure 86 Diagrammes de transition d'état du dispositif Re-MTJ sous l'action de la tension et du champ magnétique

université
PARIS-SACLAY

ÉCOLE DOCTORALE
Physique et ingénierie :
électrons, photons,
sciences du vivant (EOBE)

Titre : Effets de bords sur le renversement de l’aimantation dans des nanodispositifs à base de CoFeB-MgO

Mots clés : Jonctions tunnel magnétiques, paroi de domaine, nanostructures magnétiques, mémoires non volatiles MRAM

Résumé: Les mémoires actuelles sont limitées en vitesse, consommation électrique et endurance (Flash) ou ne peuvent pas conserver les données sans alimentation (SRAM, DRAM). En outre, leur fonctionnement s’approche des limites physiques. Dans ce contexte, les mémoires MRAM (magnetic random access memory) sont l'une des technologies émergentes visant à devenir un dispositif de mémoire «universelle» et applicable à plusieurs fonctions. Un problème critique pour les technologies MRAM est que la variabilité des nanostructures conduit à la distribution des propriétés magnétiques. En particulier, lorsque les nanodispositifs atteignent des dimensions nanométriques, la contribution des bords a une influence accrue sur le renversement de l’aimantation et limite la densité. Cette thèse se concentre sur l'influence des dommages de bords de nanostructures introduits par les procédés de nanofabrication sur la commutation magnétique de nanodispositifs spintroniques. Deux types de commutation magnétique sont étudiés: (i) la commutation induite par un champ magnétique dans les plots à anisotropie magnétique perpendiculaire et (ii) la commutation induite par un courant polarisé dans des jonctions tunnel magnétiques (magnetic tunnel junctions, MTJ) avec aimantation dans le plan.

Dans cette optique, nous avons d'abord développé le procédé complet de nanofabrication pour des plots magnétiques de taille minimale de 400nm et des nanopiliers MTJ de taille minimale de 100 nm en utilisant la lithographie par faisceau électronique et la gravure par faisceau ionique. En étudiant la distribution des champ de retournement (switching field distribution, SFD) des plots à l'aide de la microscopie Kerr, nous montrons que le renversement de l'aimantation est dominé par la nucléation et le piegegage de parois de domaine sur les bords des plots dû aux dommages induits par les procédés de nanofabrication. Le renversement final des plots est piloté par la pression de Laplace qui est inversement proportionnelle à la taille des plots. Dans le cas des nanopiliers MTJ, nous montrons qu'en utilisant un matériau isolant à base de SiO_2 pour l'encapsulation, des filaments résistifs de Si sont formés sur les bords des nanostructures. Ces filaments présentent une commutation résistive, ce qui nous permet de démontrer pour la première fois un dispositif memresistif hétérogène, appelé “resistively enhanced MTJ” (Re-MTJ), qui combine une commutation magnétique et résistive. L’application potentielle des Re-MTJ en tant que dispositif de “logic-in-memory” assurant une fonction de cryptage est démontrée.

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ÉCOLE DOCTORALE
Physique et ingénierie : électrons, photons, sciences du vivant (EOBE)

Title : Edge Effects on Magnetic Proprieties of CoFeB-MgO Based Nanodevice

Keywords : Magnetic tunnel junction, domain wall, magnetic switching, nanostructures, non volatile memory MRAM

Abstract : Mainstream memories are limited in speed, power and endurance (Flash, EEPROM) or cannot retain data without power (SRAM, DRAM). In addition, they are approaching physical scaling limits. In this context, Magnetic Random Access Memory (MRAM) is one of the emerging technologies aiming to become a “universal” memory device applicable to a wide variety of applications. One critical issue for MRAM technologies is that the variability of nanostructures leads to the distribution of the magnetic properties. Especially, when the dimension of the device shrinks to nanoscale, the edge contribution has an increased influence on the switching behavior and limits the density. This thesis focuses on the influence of edge damages introduced by the patterning process on the magnetic switching of spintronics nanodevices. Two typical magnetic switching have been investigated: (i) field-induced switching in magnetic nanodots with perpendicular magnetic anisotropy (PMA) and (ii) current-induced switching in Magnetic Tunnel Junctions (MTJ) with in-plane magnetization.

Along this line, we first have developed the full nanofabrication process for both magnetic nanodots down to 400 nm and MTJ nanopillars down to 100 nm using conventional electron beam lithography, ion beam etching and lift-off approach. By studying the switching field distribution (SFD) of magnetic nanodots using Kerr image microscopy, we show that the magnetization reversal is dominated by the nucleation and pinning of Domain Walls (DWs) at the edges of the nanodots due to the damages induced by patterning process. Then the full magnetization reversal of the nanodots is dominated by the Laplace pressure, which is inversely proportional to the dot size. For MTJ nanopillars, we show that by using SiO_2-based insulator material for encapsulation, unexpected resistive Si filaments are formed at the edges of the MTJ. These Si filaments exhibit resistive switching, which allow us to demonstrate for the first time a heterogeneous memristive device, namely resistively enhanced MTJ (Re-MTJ) that combines magnetic and resistive switching. The potential application for Re-MTJ as a logic-in-memory device with memory encryption function is demonstrated.

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