Development of ultra fine pitch array INTERCONNECTION

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Développement et caractérisation d'une technique d'interconnexion verticale de puces

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This thesis is dedicated to
My Grand Parents
&
My Parents

SUMMARY

With the constant demand for reducing the feature size of transistors and that of the devices, which is guided by Moore's law, 2D integration is no longer fit to adapt the growing demand. This has led to 3D integration of active devices with the help of Cu/Ni pillars capped with Sn based solder alloys. In the coming years, applications which demand high density interconnects (optoelectronic, microdisplays, IR-detectors, MEMS) will require an interconnect pitch of 10 µm and below. However, Cu/Ni/solder pillars have never been investigated in depth for such a small interconnection pitch. With reduction of interconnect dimension, the diameter of Cu/Ni pillar and solder alloy also reduces. Thus, it is feared that the intermetallic formation, which is the key phenomenon responsible for the bonding, may be problematic due to the reduction in size of Cu pillar capped with solder alloy.

This thesis is dedicated to the metallurgical study and its characterization for very small interconnects (5 µm) at 10 µm pitch, where the main focus is given on the physio-chemical mechanisms of soldering between Sn-Ag solder alloy and Ni or Ni/Au layers. For the first time, the mechanism of solid-state interactions between Sn and Ni is studied in depth and also for the first time the Ni_3Sn_4 SLID (Solid-Liquid-lnterdiffusion) system as an interconnect has been investigated at these dimensions. Moreover, the mechanical and electrical properties as well as the thermal stability of these interconnects are studied. Interestingly, during the latter part of this study, Ni_3Sn_2 layer is observed during aging of the Ni/Ni_3Sn_4 system for low temperature (200°C).

RÉSUMÉ

Suite à la demande constante de réduire la taille des transistors et celle des dispositifs électroniques, guidée par la loi de Moore, l'intégration 2D n'est plus adaptée à cette demande croissante. Cela a conduit à l'intégration 3D des dispositifs actifs à l'aide de piliers Cu/Ni recouverts d'alliages de brasage à base de Sn. Dans les années à venir, les applications qui demandent des interconnexions à haute densité (optoélectroniques, microdisplays, les détecteurs IR, MEMS) nécessiteront l'utilisation de pas d'interconnexions inférieurs à 10 µm. Cependant, les piliers Cu/Ni/alliage de brasure base Sn n'ont jamais été étudiés en profondeur pour un si petit pas d'interconnexion. Avec la réduction de la dimension d'interconnexion, le diamètre des piliers Cu/Ni/alliage de brasure est réduit également. De ce fait, la formation des intermétalliques, qui joue un rôle primordial dans la bonne tenue de la jonction, peut poser des problèmes majeurs en raison de la réduction des dimensions du pilier de Cu et de l'alliage de brasure.

Le travail de cette thèse est consacré à l'étude métallurgique et à la caractérisation d'interconnexions de très petites dimensions (diamètre de 5 µm et pas de 10 µm) avec comme objectif principal l'étude des mécanismes physicochimiques des interactions entre les alliages de soudure Sn-Ag et les couches de Ni ou Ni/Au. Les mécanismes des interactions à l'état solide entre Sn et Ni ainsi que l'évolution du joint vers la transformation totale en intermétallique Ni_3Sn_4 (Solid-Liquid-Intercondiffusion - SLID processus), ont été étudiés pour la première fois dans de tels systèmes de dimensions micrométriques. De plus, les propriétés mécaniques et électriques ainsi que la stabilité thermique de ces interconnexions ont été étudiées. L'observation pour la première fois de la formation de la phase Ni_3Sn_2 à l'interface Ni/Sn à 200°C lors des vieillissements thermiques présente un intérêt pratique de grande importance.

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INDEX

General Introduction

It is in the human nature to explore, to understand the mysterious phenomenon of the nature and use them to innovate new things which one can imagine. This very nature has led to great discoveries and inventions. One of the example is the invention of aircraft in early 20th century, which was inspired by birds and was successfully achieved by understanding the aerodynamics.

The field of electrical or electronics is one such example. The field was born in 17th century and led to the second industrial revolution in late 19th century. By mid-20th century, microelectronic field emerged, which dealt with the study and manufacturing of very small electrical designs and components. Ever since the birth of microelectronics, the feature size of final component has reduced exponentially, as predicted by Moore's law. According to this law, the number of transistors in a dense integrated circuit (IC) doubles approximately every two years [1, 2]. This has been proven right and has been used to set roadmaps for research and development for the coming years. Since 1970s, the transistor density on the integrated circuits has increased, the fabrication cost of those transistors has also decreased. After nearly more than 4 decades after Moore predictions, in 2017, IBM has demonstrated a new technology for 5 nm Si chip using Fin Field-Effect Transistor (FinFET) [3]. This has been driven by the desire of more efficient and more aesthetic consumer electronic, in other words the want for smaller size and lighter weight of the product but yet with ever more increasing functionalities.

One of the major effect of this feature size reduction can be seen in packaging. As the size reduces, the connection density increases, as a result of that the two dimensional packaging (2D) has to be replaced by three dimensional packaging (3D). With emergence of 3D packaging, soldering became one of the best options for making connections. Although it has been known to mankind since 3000 BC, the potential of soldering has been repeatedly explored and made efficient over years to realize our imagination from using it for metal-work (for making tools), to plumbing and now in 20th century for microelectronics.

According to the International Technology Roadmap for Semiconductors (ITRS), the connection pitch will be reduced to below 10 µm in coming years. It is feared that as the connection pitch (in other words diameter) is reduced, soldering process has to be adjusted by modifying the soldering technique or by altering the metallurgy. However, in this thesis, we want to test the current metallurgy with least modification possible and tailor the process to achieve the interconnects at 10 µm pitch. Thus, this thesis is dedicated to understand the soldering between Ni and Sn and to develop 10 µm pitch interconnect.

In the ***first chapter*** of this thesis, the manufacturing trend of semiconductor devices especially their packaging are presented. The challenges associated with miniaturization and densification are laid down. There are different levels of electronic packaging, which require different in-

terconnect systems. These different interconnect systems are described with a special attention given to flip chip bonding. The miniaturization trend of interconnects for first level of packaging is described and the context of thesis is laid down. On the last section of the chapter, state of the art for 10 µm pitch assembly and Ni/Sn interactions is presented.

In the ***second chapter***, the experimental procedure, tools and methodology used throughout the thesis are described. The first requirement for these studies, is to fabricate the components required for the assembly at 10 µm pitch. Although Cu pillars are well adapted in packaging industry, however when they are scaled down to 5 µm, some challenges in their fabrication appeared therefore some changes are done to the fabrication process. After the fabrication process, assembly process is described. To validate the assembly process for 10 µm pitch, qualification levels are designed, which at the end will provide the definition of *good* assembly process.

The Sn-Ag solder alloy is well studied for larger bump size ($>$ 25 µm). However no studies have been conducted on the behavior of Sn-Ag alloy at small diameters yet. We anticipate that by decreasing the size, we may see some different behaviors which were suppressed/neglected in larger diameter bumps due to their big size. This is studied in ***Chapter 3***. Along with this, the chapter is dedicated to understanding the behaviour of the Ni/Sn system. The interfacial reactions in both solid Sn / solid Ni system and liquid Sn / solid Ni system are studied and the results are presented and discussed. In particular, short term solid state interactions and a theoretical analysis of the initial formation of Ni_3Sn_4 phase at liquid Sn/Ni interface have been investigated for the first time.

Traditionally, interconnects joint made of Sn based solder alloys is preferred. However, for 10 µm pitch assembly, the solder thickness is limited, therefore even with the Ni barrier layer, it might not be possible to limit the growth of IMC in the interconnect joint. Therefore, it is difficult to tailor the process to attain Sn interconnect joints (i.e. with some left solder alloy at the end of the reflow process). Thus, it is imperative to investigate intermetallic (IMC) interconnect joints, and answer whether *Ni/Sn IMC interconnects replace the traditional Sn interconnect joints at finer pitch (<10 µm)?* At the best of our knowledge, this type of IMC joint has not been studied in terms of interconnect at micrometric scale. This is investigated in ***Chapter 4*** by comparing Ni/Sn *IMC interconnect joint* (Ni/*Ni_3Sn_4*/Ni) with *Sn interconnect joint* (Ni/Ni_3Sn_4/*Sn*/Ni_3Sn_4/Ni) for which some Sn is still left at the end of the joining process. The comparison is done in terms of metallurgy, properties of interconnects (mechanical, electrical resistance) and their thermal stability.

Chapter 1

State of the Art

Contents

INTRODUCTION

It all started in 1904 with the invention of thermionic diode (a vacuum tube) which then became a basic component for electronics throughout the first half of the 20th century. Much later in 1960, first metal-oxide semiconductor field effect transistor (MOSFET) was demonstrated although it was proposed much earlier in 1925 by German inventor, Julius Edgar Lilenfeld. This now became a building block for microelectronics. The transistors along with other components are now fabricated on a single circuit came to be known as *'Integrated Circuits'*(IC).

The number of transistors per unit area in the integrated circuits has been increasing two times every two years since 1960, which was predicted by Gordon Moore, which came to be known as Moore's law [1]. Along with this miniaturization, the functionality of the integrated circuits has increased too. Now on a single circuit, one can have many functionalities such as Radio Frequency (RF) devices, Opto-electronic devices, Microelectromechanical systems (MEMS) etc. This trend has created a new interdisciplinary field called *System Engineering*, where the main focus is given on how to design integrate and manage the complex system.

The realization of the system engineering is done by *Packaging*. Here the complex systems of different integrated devices are packaged on a single substrate using the design and considerations given by system engineers. The major task here is to facilitate communication in between integrated circuits/devices/package which is done by providing suitable **Interconnects**.

These three branches; Integrated Circuits, System Engineering and Packaging together make an electronic system [4]- see Figure1.1.

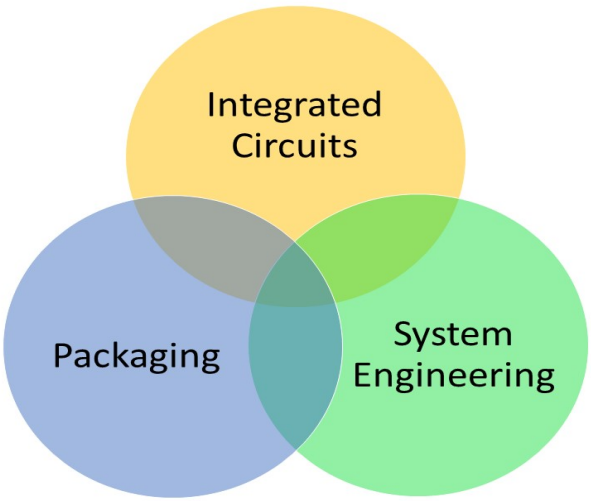


Figure 1.1: Electronic system

With the increase in the density of transistors on the chip (Moore's law), the functionality of the chip/product has also been diversified [1]. Nowadays, many different types of components are required to be integrated into a single unit, which gave path to More than Moore's. The further miniaturization of the electronic components is now predicted by a double roadmap consisting of Moore's law and More than Moore's law (i.e. diversification-functionality of product/device) as shown in Figure 1.2.

Also, the fabrication capacity has increased and now components can be fabricated on the larger area in lesser time, thus the cost has been reduced tremendously. However, the packaging has not been scaled down proportionally. Thus one of the major cost in device production is/will be coming from its packaging.

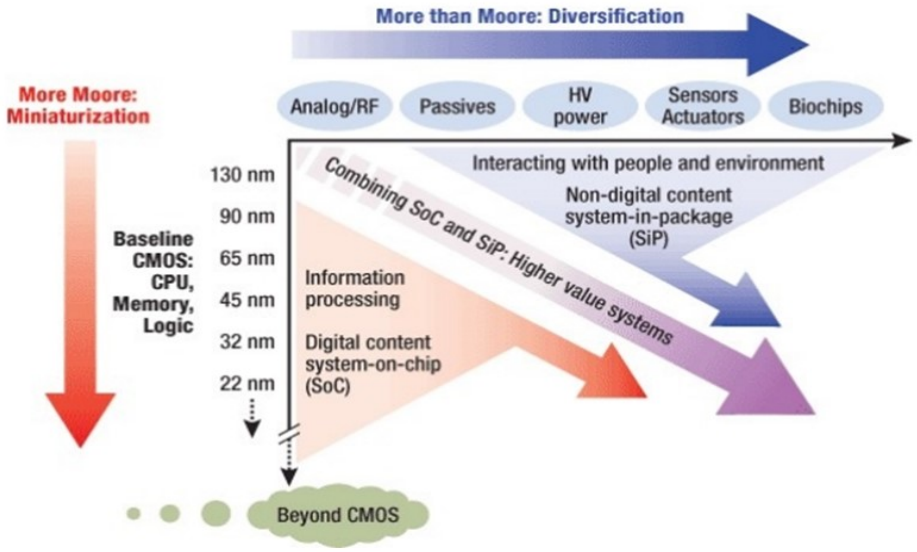


Figure 1.2: Double roadmap for further miniaturization of electronic system [6]

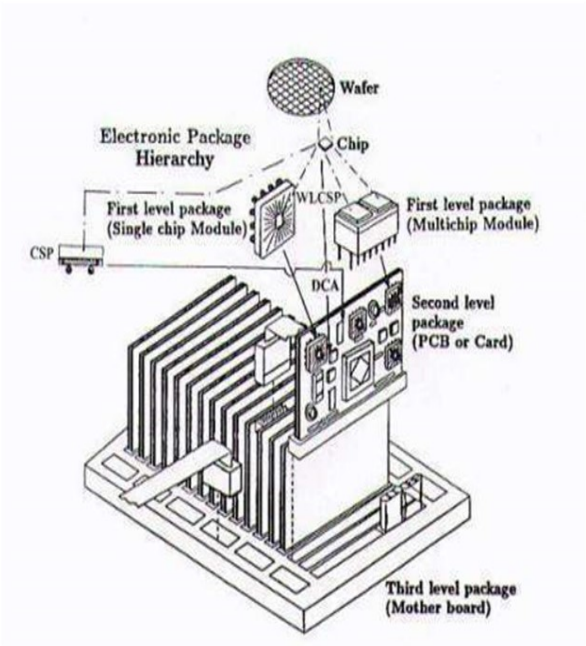


Figure 1.3: Different level of packaging [7]

Electronic components, depending their usage, require different level of packaging [7,8] shown in Figure 1.3. Just after front end process which manufacture the basic electronic components,

the first level of packaging is done. Here, chips are connected with modules or system in package. The pitch is very small (<100 µm). The second level of packaging hierarchy is connecting the module or the system on to a board or a card. For this level, the interconnect pitch is larger (200-1000 µm) than the first level. Then the board/card is connected with the system which makes the third level of packaging.

To address the challenge of miniaturization, two approaches are considered: System on chip (SOC) and System in Package (SiP) (schematically presented in Figure 1.4). SOC [9] is defined as a complex IC that integrates the major functional elements of a complete end-product into a single chip or chipset. SOC design incorporates both hardware and software components. One of the most common example for SOC is Microprocessor. In the other approach i.e. SiP [10] more than one active electronic components of different functionality like MEMS or optical component etc. are integrated and connected on a single package. This package provides multiple functionality associated with a system or subsystem. One of the most common example for this kind of electronic system is Mobile phones. The integration process(es) used should offer solutions to the challenges for various applications. Hence, the choice of interconnect technology and material for packaging as well as the system design determine size, weight, performance, user friendliness, reliability and finally, the price of a product and thus its market success.

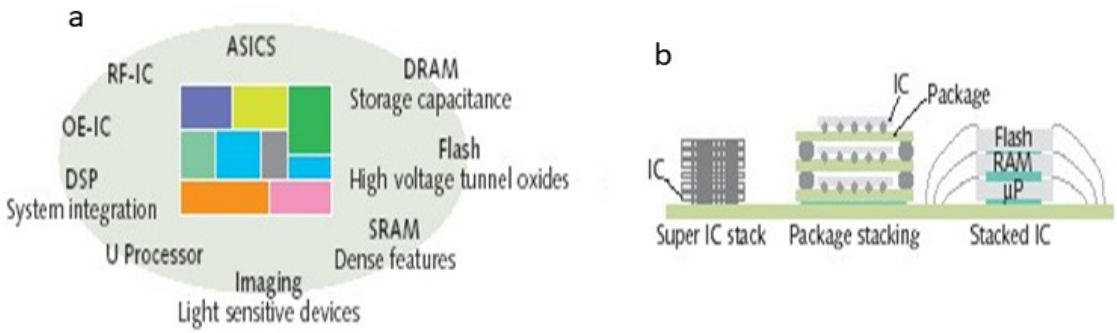


Figure 1.4: Schematic diagram showing two approaches, (a) System on chip (SOC) [9], (b) System in Package (SiP) [10]

These approaches have opened to new challenges for packaging, specially SiP. First challenge comes with the design of the system. Now that different components of electronic system such as RF system, memories, optical chip etc. has to be packaged on the same package, it has to be designed carefully, keeping the power disturbances (losses) and signal integrity in consideration. Although shorter interconnects between ICs increase the speed of the system, the higher number of Inputs/Outputs (I/O's) in the system increases the risk of cross-talk between different component (signal integrity), which also increases power losses in the package. Thus the designing as well as metallurgy of the interconnects become very important. The second main challenge is the thermal dissipation within the package. With the advancement of technology, the density of ICs and/or functionality increases but the package size has decreased which caused problem in the heat dissipation. If this problem in not handled well, then more heat is entrapped, which is malicious to the devices as well as the interconnects. To deal with this problem, heat sinks are used and they are currently in research to increase the thermal dissipation within the system. Thirdly, the testability or characterization (material and process characterization) becomes difficult. After packaging, different parts of the package are tested

individually and as a system to verify that all the components are working properly. If something is not working, then to find out the error in such a complex system becomes a major challenge. Therefore known good die approach is slowly progressing, but there is a significant cost to this approach.

Here, in this thesis, the consideration has been given to the *interconnects* for the first level of packaging.

1.1 INTERCONNECTS

Interconnects are the building blocks of any package. They are like cables that connect input of one active device to another. The most basic function of these interconnects is to provide electrical communication in between devices/packages. There are broadly three ways of forming an interconnect, (i) Wire bonding, (ii) Tape Automated Bonding and (iii) Flip Chip bonding as shown in Figure 1.5 [11, 12].

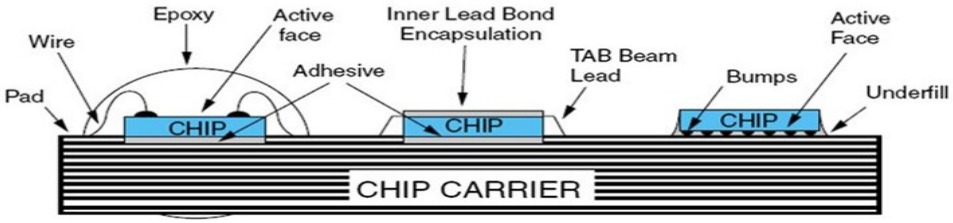


Figure 1.5: Types of interconnects [11]

1.1.1 WIRE BONDING

Wire bonding is the most traditional way of forming an interconnect, where the connections between the devices are made through wires. First the device is glued to the substrate and then the connections are made at the periphery of device using wire bonding as shown in Figure 1.6. The material used for making interconnect should have good electrical and thermal conductivity and should be resistant towards corrosion, thus Al, Au and sometimes Cu are used. On both sides, i.e. at chip and substrate/second chip, metallic pads are fabricated to create an interconnect between them. The wire is melted with high voltage electric arc, and is connected to each pad on both sides by interfacial interactions between the metallic pad and the wire material [13].

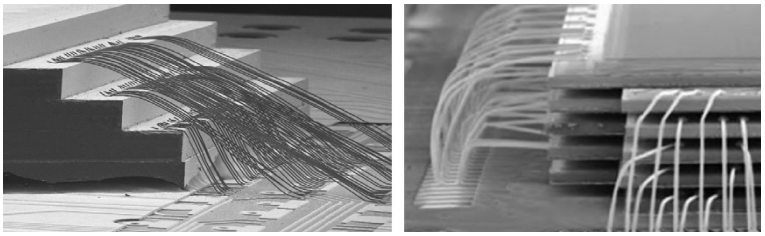


Figure 1.6: Wire bonding [14, 15]

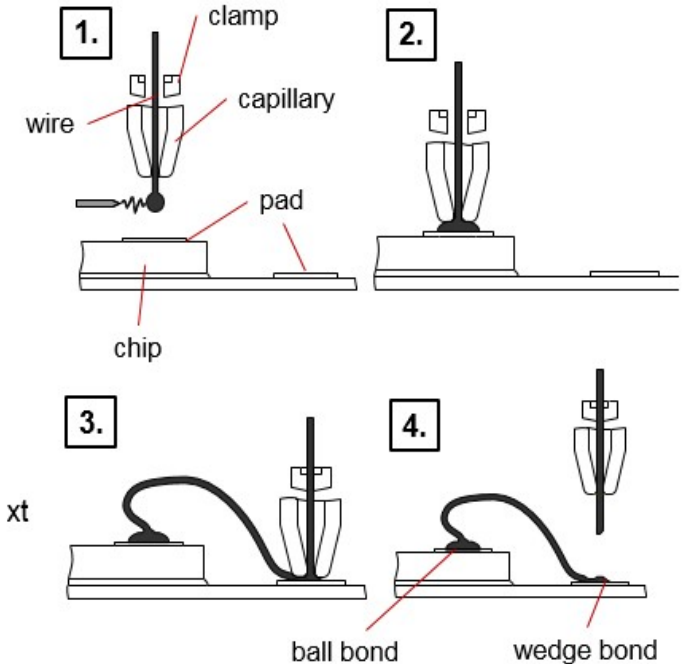


Figure 1.7: Ball and wedge wire bonding [16]

For connection, depending on the bond shape, wire bonding can be classified into ball bonding or wedge bonding. In ball bonding, after high voltage electric arc, the metal wire melts and takes the shape of a ball and then this ball is bonded to the pad by thermocompression (solid-state bonding) with the help of temperature, pressure or ultrasound. In wedge bonding, after melting the wire, pressure is applied and a wedge shaped bond is made between the pad and the wire [16]. Both types of wire bonding process are shown in Figure 1.7. This is a widely used technique for the interconnections. As it has been tremendously improved over the years, automatic bonding equipment have been developed to address higher density, smaller pitch so that some three dimensional (3D) stacking using wire bonding interconnect is possible. However, this technique has been pushed to its limits in terms of connection density.

1.1.2 Tape Automated Bonding (TAB)

This is a one step process unlike wire bonding and it provides faster electrical performance due to smaller length of interconnect. In this technique, interconnects are patterned on a polyimide tape, on which the active die is bonded as shown in Figure 1.8. The interconnect is generally achieved by thermo-compression between gold pad (fabricated on the chip) and Cu (on the tape). The die is usually encapsulated with an epoxy. This technique not detailed here has been developed mostly to replace wire bonding for Liquid Crystal Display (LCD) industry. (For more details see [17])

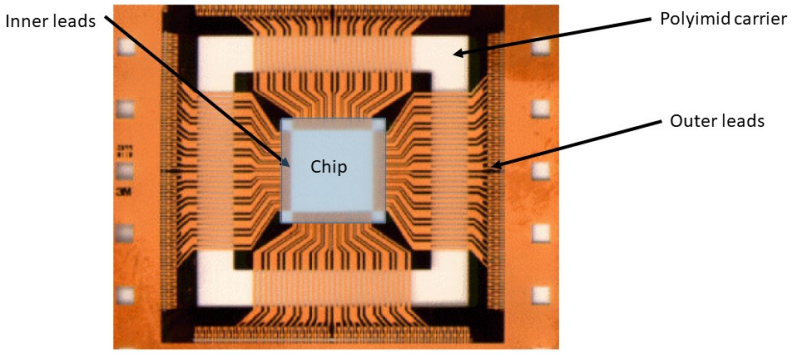


Figure 1.8: Tape Automated Bonding [17]

1.1.3 FLIP CHIP BONDING

In 1963 IBM has first quoted the term C4 which stands for Controlled Collapse Chip Connection [18]. It is an advanced surface mount technology, in which bare silicon (with an active device) is turned upside down and bonded over the substrate as shown in Figure 1.9, hence it is called flip chip bonding. Flip chip method has several advantages. Flip chip bonding can have I/O all over the chips, unlike wire bonding, which have I/O just on the periphery, thus may handle higher connection density. Also, the interconnection pitch can be reduced much more efficiently. Secondly, the connections are shorter than wire bonding, thus faster connection and lower losses. Finally, unlike wire bonding and TAB, flip chip joint also provides mechanical support and thermal dissipation.

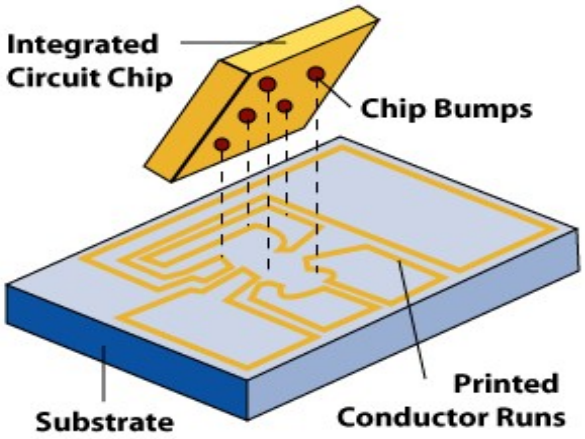


Figure 1.9: Schematic for showing different components of flip chip bonding [19]

The schematics of flip chip bonding is shown in Figure 1.10, the chip has bump structure on it and it is facing down towards the substrate. Here an interconnection is formed between I/O of device chip and substrate with the help of soldering. ***Soldering process*** consists in the joining of two solid parts achieved by placing an alloy (solder alloy) between them and melting this alloy in order to obtain an intimate contact between the alloy and solid parts (good wetting),

followed by cooling to the room temperature. Solder alloy is generally on the active device side and metallic pads are on the substrate side. (This may be reversed depending on application). Thus the flip chip assembly contains 3 parts, ICs/device, substrate and interconnect system. Active device can also be made of material other than Si, such as sapphire, GaN, InSb, InP, InGaAs etc.

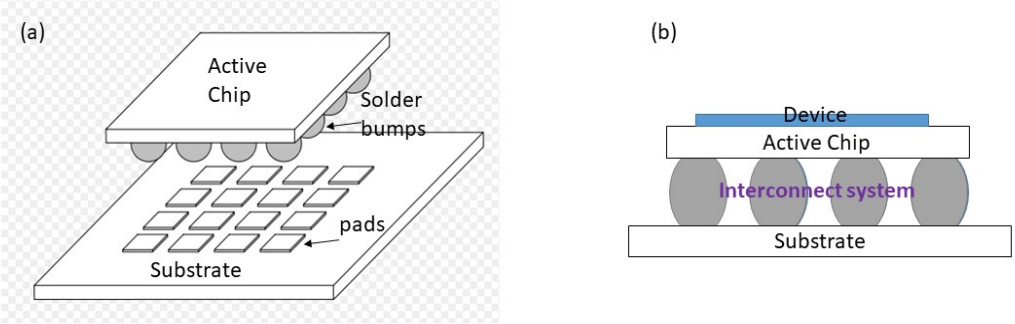


Figure 1.10: (a) Schematic for flip chip bonding (b) cross-section view of flip chip bonding [20]

The main functions for a flip chip interconnect system are to provide electrical connections, to facilitate heat dissipation and provide mechanical support between the chip (active device) and the substrate as shown in Figure 1.10.

For making an interconnect system, 2 main structures are required: (i) Under bump metallization (UBM), and (ii) bumps as shown in Figure 1.11. UBM contains several metallic layers which serves different purposes. The prime function of UBM layers is to provide an electrical connection between the chip metallization (which is normally of Al or Cu) and the solder joint. In Figure 1.11 (a), the first layer (starting from chip metallization -Al pad) is an adhesive layer that ensures the adhesion between chip metallization and UBMs, which is generally Ti and/or TiN. This layer is important because it gives mechanical strength to the interconnect system. The second layer is a barrier layer which is present in order to prevent diffusion of different species from the solder bump to the chip metallization layer. In general, high melting elements such as Ni, W, Pd, Pt (but may not be limited to) are used for this purpose. The last layer is called solder wettable layer which will be consumed during soldering process. The preferred choice of metals for this layer are Cu, Ni/Au and Au. This layer will ensure the prime function of UBM i.e. obtaining an intimate contact between the solder alloy and the diffusion barrier layer [21].

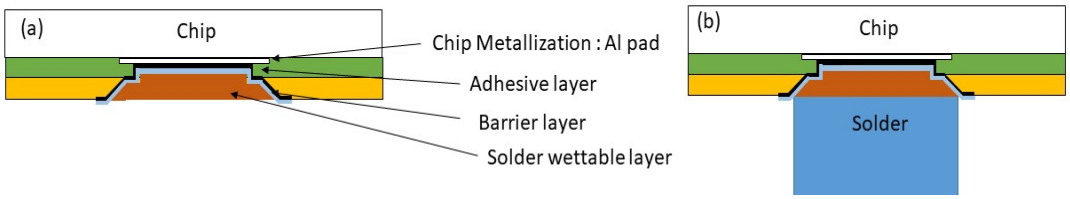


Figure 1.11: Schematic diagram for (a) UBM and (b) solder deposition on for C4 bumping [21]

After UBM deposition, solder is deposited over UBM, which is the second structure in interconnect system. Depending on their bonding temperature there are broadly 3 types of solder alloys:

1. High temperature with the melting point >250°C : Au-Sn, Pb-5%Sn, Pb-3%Sn
2. Moderate temperature with the melting point between 200-250°C, for e.g. Sn-3%Ag, Sn-3.5%Ag1%Cu
3. Low temperature with the melting point between 150-200°C, e.g. are eutectic Pb-63%Sn, Sn-52%In

There are also options for deposition/fabrication. The most common are electroplating and screen printing (or solder paste). In the last century, Sn-Pb eutectic alloy was the most common solder alloy used, however due to Pb health hazards it was replaced by other alloys. Now (since 2001) the most common alloys are Sn-Ag and Sn-Ag-Cu alloy (SAC) [23]. Figure 1.12 shows the technologies used versus bumps pitches and diameters depending on the packaging level. Usually, after deposition of solder alloy, it is melted to take a form of hemisphere, called as solder bump.

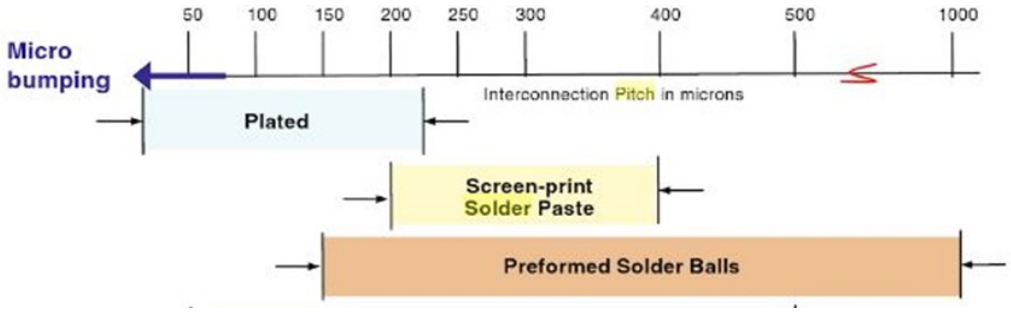


Figure 1.12: Solder deposition technology [22]

For flip chip bonding, the chip with solder bump is flipped and aligned to the metallic pads (present on the substrate) as shown in Figure 1.10. This is followed by a soldering process which creates a bond. The basic principle of soldering is interfacial interaction (wetting, reactive diffusion) of solder bump with the metallic pads. In metal-metal systems, this interaction leads to the formation of a reactive layer or intermetallic (IMC) layer, between UBM/metallic pad and solder bump. There are two ways to make a bond: first way is to heat the solder above its liquidus temperature and when it becomes liquid, it wets and reacts with the metallic surface to form intermetallics. This process is called ***reflow process*** (or mass reflow process without applying pressure). The other process is solid state bonding, where the system is heated at high temperature (but below the melting point of the solder) and pressure is applied to facilitate the interdiffusion between bump and UBM/metallic pad. Both process are schematically presented in Figure 1.13.

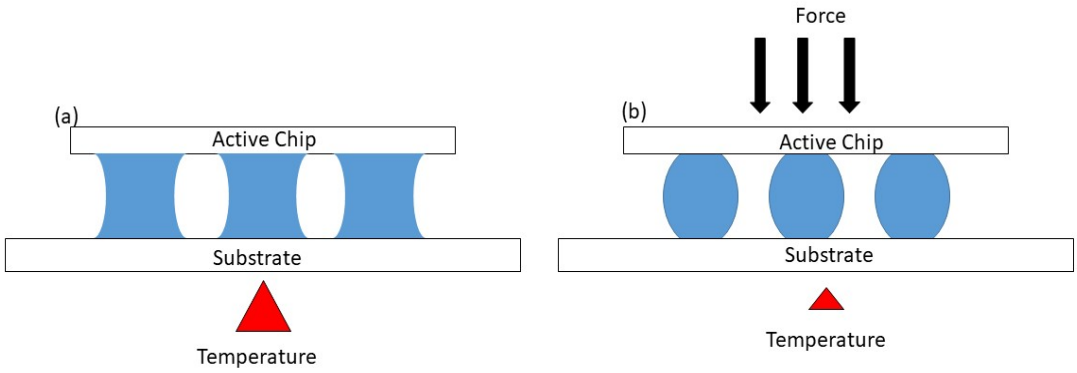


Figure 1.13: Flip chip bonding with (a) Mass reflow, (b) Thermocompression

For efficient reactive diffusion, the solder should properly wet the metallic surface of the pad. The wetting of solder determines the geometry and mechanical reliability of the substrate/solder joint as well as the initial reactivity at the interface between solder and metallic pad. There is always a good or very good wettability in liquid metal/solid metal systems but Sn based liquid alloys do not wet solid oxides [25]. Thus for proper wetting in soldering process, the surface of both metallic pads as well as solder bumps should be free of their native oxides and other contaminations. To ensure that, special reducing substances, called flux, are used. A good wettability also ensures a good auto-alignment between the lower and upper parts of the joint. During the bonding, solder only wets the solderable surface (Cu/Au). If the chips are misaligned then the liquid solder may exert force (due to surface tension) to align the metallic pads with the solder/UBM. This is called auto-alignment and this phenomenon depends on the solder volume, chip weight, pad sizes on the chip, the substrate and de-oxidation of metallic pads [26].

Flux has two more functions other than deoxidation of metal surfaces: (i) it protects the surfaces (of both solder and metal) from re-oxidation during bonding and (ii) it also guarantees the heat transfer between the parts which are soldered, thus provides heat uniformity. The flux has usually 3 components, flux base, activator and solvents. Flux base is the main ingredient which is responsible for oxide reduction such as rosins and resins. For de-oxidation reaction the flux base should be activated which is done by ammonium chloride salts. The percentage of activator determines the activity and corrosiveness of flux. Depending on the percentage, flux can be classified as mildly activated flux (0.2% of activator), activated flux and super-activated flux. Recently, water based flux are gaining popularity, because in principle they can be easily cleaned by water unlike rosin/resin fluxes which require some solvents for cleaning. However, water based flux requires strong activators, thus these are more corrosive if not cleaned properly [27]. Thus cleaning of flux residue is important because if not cleaned properly it can harm the performance of package.

During the bonding process intermetallic layers can be formed at the interfaces between the solder alloy and the substrates, as it is mentioned above. The intermetallic compounds (IMC) are materials which have different mechanical and electrical properties than their constituting elements. In particular, IMCs are very brittle material thus the morphology and thickness of these reactive compounds should be controlled. Thus the choice of the reactive couple i.e. reactive element in the solder alloy and solid layer in contact with the alloy is of great importance. [28–30]

Moreover, the microstructure of the solder alloy also contributes to the mechanical property of the joint. The microstructure of the alloy depends on the solutes added, for e.g. Ag, Cu, Bi, Ni etc which forms additional IMCs (in addition to IMCs formed during the joining), whose properties will also influence the properties of the joint. Also, these solutes, alter the rate of undercooling in the solder alloy. Undercooling is the difference between melting and solidification temperature and it directly affects the microstructure of the alloy and thus its properties. Thus the solder alloy should be chosen wisely .

After bonding, a process called underfilling is performed. The main purpose of this process is to fill gaps between top die and substrate, in the space between interconnects by a polymer (called underfill). This filling gives additional support and reduces the stress of the overall package. Thus it is a very important step to ensure the reliability of the package.

1.2 WAFER LEVEL PACKAGING

The **Wafer Level Packaging** process **(WLP)** is a technology in which all of the IC packaging is performed at the wafer level. One of the major advantage of this packaging technology is the cost effectiveness. With this packaging method, encapsulation (with filled epoxy) and contact formation are done on the wafer before separating them into individual finished ICs as shown in Figure 1.14. This has effectively minimized the cost of back-end process (packaging) by eliminating packaging of individual ICs. Secondly, WLP may use standard microelectronic equipment and beneficiates from the Si advanced technology.

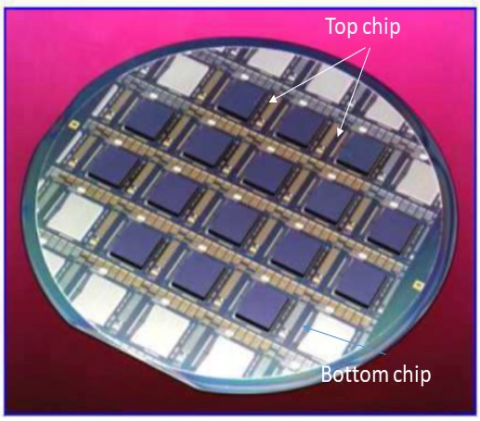


Figure 1.14: Wafer Level Packaging WLP [31]

The main application area for wafer level packaging are portable products with increased functionality and speed like consumer electronics (such as digital, video cameras), communication devices (e.g. cell phone handsets) and computing devices (e.g. notebook computers and PDAs)

One of the major interconnection technique used for wafer level packaging is flip chip. This interconnect technology may be used for both first and second level packaging (between chip to module/system), the first level being between the active chip and a substrate then the second between the substrate and the board. In this case through silicon vias must be fabricated to electrically connect the first and the second level as shown in Figure1.15. The first level of

packaging is done with the help of microbumping while the second level is done with solder bumping.

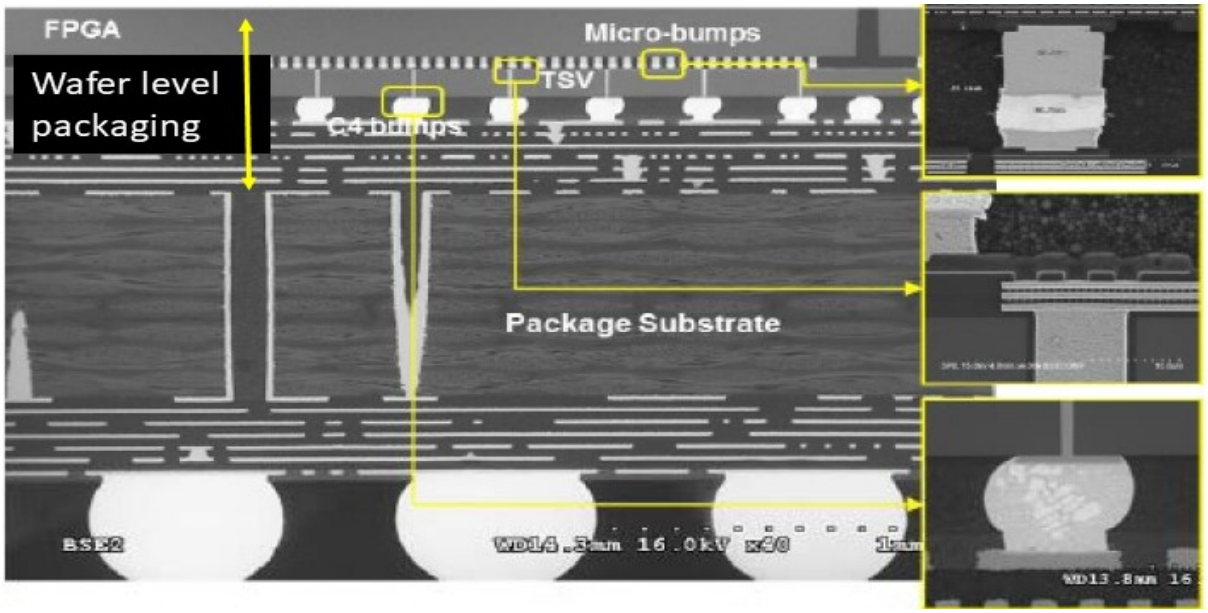


Figure 1.15: SEM image for different levels of packaging included WLP [32]

Microbumps are the solder bumps formed over Cu pillars, while solder bumping is just solder over UBM. Due to smaller pitch and higher density, the solder bumps (in the case of C4) are replaced with microbumps. It is called micro because the size of Cu pillar is less than 100 µm. In Figure1.16 the difference in geometry of solder bumps and microbumps can be seen.

There are many advantages of microbumps over solder bumps. Firstly, at micrometric pitch, if solder bump is used, then there is a good chance of short-circuit. Indeed, for a given joint thickness noted h in figure 1.16, the horizontal diameter for solder bump is much larger than for Cu pillar (i.e. the wettable surface). Thus Cu pillar reduces the possibility of short circuit, by lowering the surface of wettability. Secondly, Cu is a better thermal conductor than solder alloys, therefore it will help in dissipating heat better in case of micro-bumps than solder bumps. Lastly, copper has also high resistance towards electromigration, thus it can withstand higher density of current. Thus in application that requires high electric fields, the possibility of failure in microbump is much lesser than in solder bump thus microbump is more reliable [33–36].

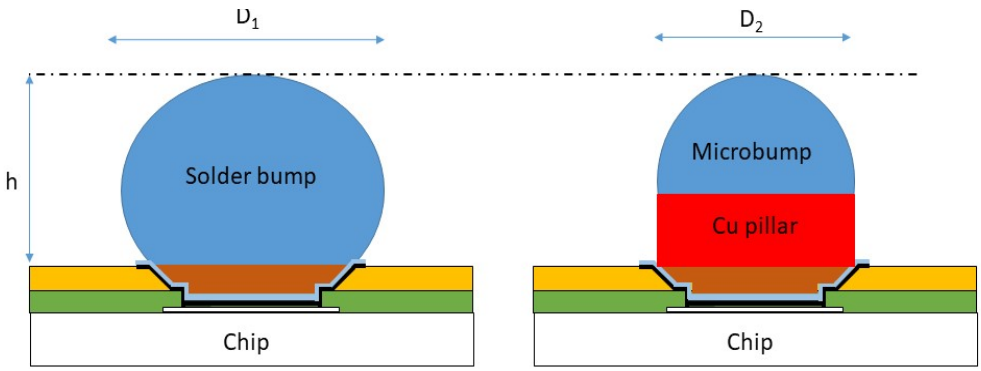


Figure 1.16: Difference in geometries for solder bump and microbump

Nevertheless, the dimension/pitch of microbumps will determine the connecting density for first level of packaging. As of now, microbumping technologies has scaled down till 50 µm pitch in most electronic applications. According to the International Technology Roadmap for Semiconductors (ITRS) [6], it is expected in coming years that the connecting pitch will be further reduced down to 10 µm pitch for some high consumer applications such as portable devices which is usually driving the market [37]. However, in some niche applications with very specific targeted market much smaller pitch are already being addressed, using different flip chip technologies that are described in appendix A. Indeed for example, in infrared detectors for military or space applications 10 µm pitch products are being fabricated [38, 40]. Some strong interest in this pitch is also being shown by the microdisplays, augmented/virtual reality and automotive industry. Very fine pitch interconnects accompanied with some challenges, which are described in next section.

1.3 Challenges for 10 µm pitch assembly

The interest in this field is growing and slowly more research groups have started working on fine pitch interconnect technology. For this technology, there are several challenges apart from fabrication capabilities. These challenges are listed below.

1.3.1 Metallurgy

One of the major challenge for very fine pitch assembly is the metallurgy of microbump. When the assembly pitch is decreased, the diameter of the microbump and of interconnect also decreases more or less proportionally. In general, the bump diameter is half of the pitch, so that there is a equal spacing between the joints and intra-joint, therefore, for 10 µm pitch, the ideal interconnect diameter is 5 µm. At this dimension, it is not possible to have very high microbump due to the limitation of photoresist aspect ratio. Photoresist is used to pattern the microbumps on Si wafer which will be explained in chapter 2. In order to make an interconnect/joint after bonding, the bump should have enough solder to wet the metallic pad and to react with it to form a thin reactive layer. Also during the bonding process, Cu should not be completely consumed. Due to the limitation of permitted pillar height, the thickness of solder alloy and of Cu pillar should be chosen carefully to make a ‘good bond’. The metallurgy of the joint also plays a crucial role in the reliability of a joint therefore it should be chosen carefully to assure a stable interconnect.

1.3.2 CTE mismatch

In the package different materials are assembled together these materials may or may not have similar thermo-mechanical properties most importantly the Coefficient of Thermal Expansion (CTE). Table 1.1 gives CTE of some of the most common materials involved in bonding. During bonding the package has to undergo bonding cycling which involves heating from room temperature to bonding temperature (250°C) and then cooling down. Also during the life time, depending on the application, the package may be used at high temperature or it may have to

undergo thermal cycling. These temperature cycles will cause stress on the package which are called as thermo-mechanical stresses [39, 40].

During bonding, if there is a significant CTE mismatch between materials, then top and bottom dies will undergo some relative displacement. In this case, the physical contact between top (microbump) and bottom (pad) at the edges of the package may not form completely as shown schematically in Figure 1.17 (a). The issue becomes critical if the bond diameter reduces as in the case of 10 µm pitch. In Figure 1.17 (b), a SEM figure from ref. [40] shows the misalignment due to CTE mismatch between Si and InP. In the worst case scenario, like in Figure 1.18 the bond may not be possible at all. Thus the bonding technique has to be engineered according to permitted thermal budget (given by the difference in CTE of materials involved).

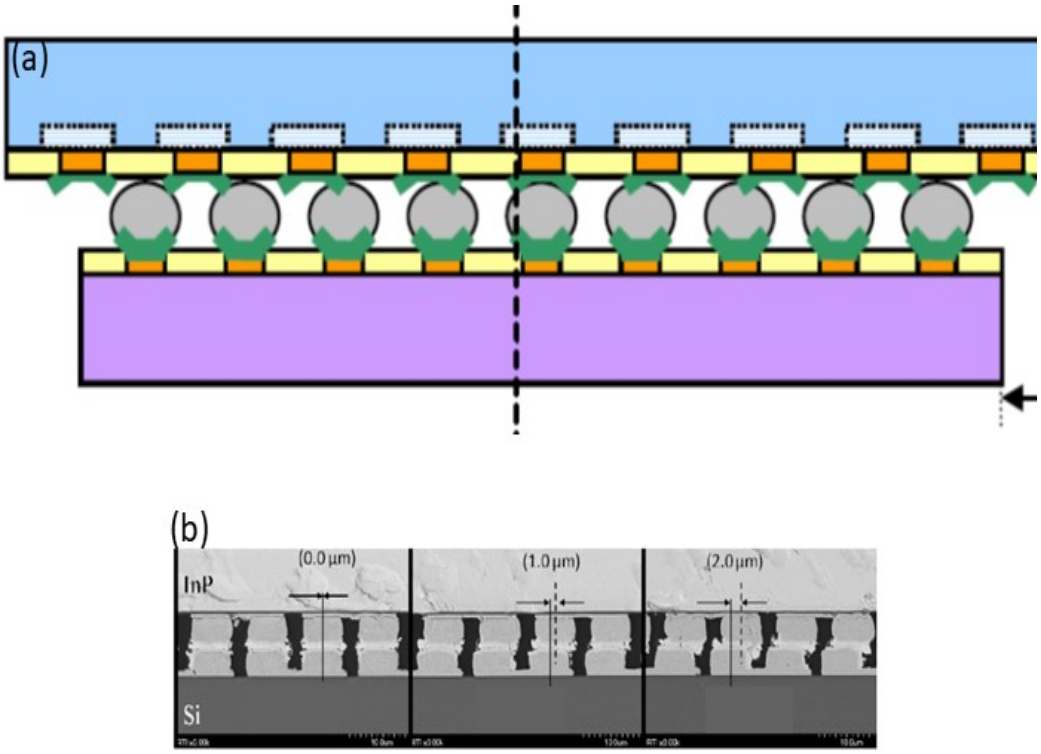


Figure 1.17: Misalignment due to CTE mismatch between wafers (a) schematic diagram and (b) SEM micrograph [39]

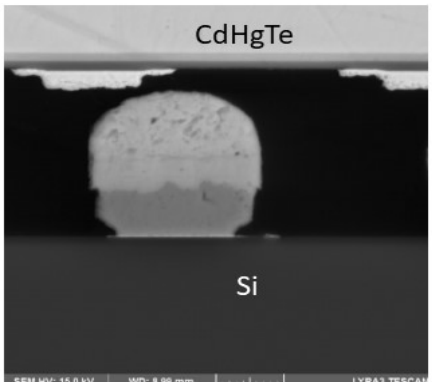


Figure 1.18: SEM micrograph of interconnect failure due to CTE mismatch [40]

Table 1.1: Materials with their CTE mismatch

Material in Interconnect	CTE (ppm/°C) at 25°C
Si [41]	2.6
Sapphire [42]	6.5
CdHgTe [43]	4.6
InP [44]	5
Cu [41]	16.5
Sn [41]	22

1.3.3 Bow and warpage in wafer

Bow is a bend in the wafer which may be either concave or convex, whereas warpage is twisting of the wafer. Warpage and bow in the wafer appeared due to mechanical stress which is/may be introduced by technological process used on them. If the difference in bow between two substrate is very high or dissimilar in nature and/or warpage is present, then it can cause some issues during the bonding. The problem in forming a physical contact between top and bottom dies will occur, if the thickness of solder alloy (h_1) is less than the degree of distortion (h_1+f), where f is the difference between the minima and maxima of distortion as shown in Figure1.19. The problem gets magnified when the pitch/surface area of the bond is reduced as in the case of CTE mismatch. In this case, some pressure has to be applied during bonding [45].

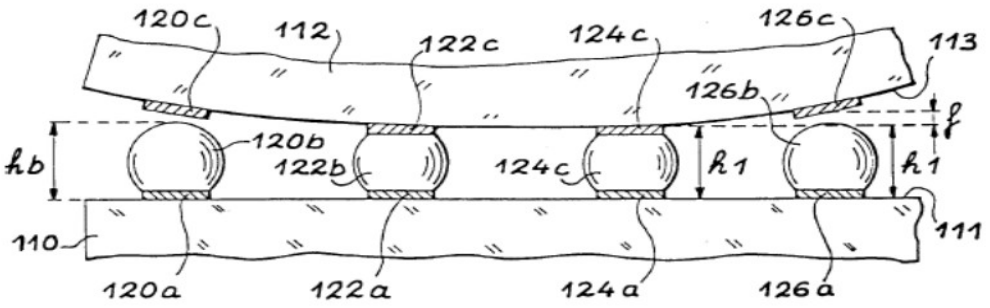


Figure 1.19: Schematic diagram showing problem with bonding due to warpage [45]

1.3.4 Flux cleaning

The next issue is with flux cleaning after bonding. As the density of interconnects increases (10 µm pitch), it is difficult to clean the flux after the assembly as discussed in Section 1.1.3. The flux residue is also corrosive in nature and can destroy the electrical pathway for the current, thus causing problem in electrical behavior of the package. Normally solvents are used as flux cleaning agents, but they are harmful to the environment. One solution is to use gaseous flux such as formic acid, forming gas etc. These are no clean fluxes too, as the by products are also gaseous in nature, thus no cleaning is required after bonding.

1.3.5 UNDERFILLING

Typically after bonding, capillary underfilling is used. Here the underfilling is dispensed with high pressure into the package. Sometimes heating is also applied which facilitates the flow of underfilling. After dispensing, it is cured at around 80°C (temperature depends on the properties of underfilling). For 10 µm pitch assembly, the process will be really slow due to high density of interconnects. Secondly, if liquid flux is not cleaned properly, underfilling application would be hindered. To deal with this challenge, other options are explored like pre-applied underfilling. In this case, underfilling which is in form of paste or a film, is applied before bonding and it also acts like flux. However pre-applied underfilling has also various challenges associated with film thickness, or filler entrapment within the joints and therefore some serious work is needed if it has to be used for fine pitch assembly.

1.4 FLIP CHIP TECHNOLOGY OTHER THAN SOLDERING

To address the challenges at 10 µm pitch, other types of flip chip technology which does not use Sn soldering is investigated by some other research groups such as Cu-Cu direct bonding, cold insertion (microtubes) and In bumps. They are presented in Appendix A. Some of the techniques are suitable for wafer to wafer bonding while other are more apt for chip to wafer bonding.

Although they are promising, Cu pillar assembly (microbumps) is widely used and mature technology, therefore it is an interesting candidate. However at this pitch, more in-depth study is needed to qualify Cu pillars, in particular the material composition of the Cu pillar.

1.5 CONTEXT OF THESIS

In this thesis the prospects of ***interconnects (Cu pillars) for finer pitch (<10 µm) is being evaluated for Si on Si bonding.***

In the flip chip process, the interfacial intermetallic (IMC) layer formed at metal/metal interface plays a crucial role in determining the properties and reliability of the joint/interconnect. Starting from fabrication process, to the bonding and then during the lifetime of packaged device, this layer keeps on evolving and changing until it reaches its thermodynamically stable state or in certain cases metastable state. During the interfacial reactions, the portion of IMC in the interconnect increases significantly. It is well known that intermetallics are brittle compounds of higher electrical resistance than Sn-based alloys and Cu and often co-exist with diffusional or other types of voids and hence are mechanically weak [30]. Thus the higher percentage of IMC in the interconnect increases the electrical resistance of the joint and decreases its mechanical strength. It was clearly demonstrated in the literature that thick IMC interfacial layers are not favorable for the mechanical and electrical properties of interconnects [46–49].

Gagliano et al. [50] found for Cu/Sn system that after 30 mins of annealing at 250°C, 5 µm of Cu_5Sn_6 and around 1 µm of Cu_3Sn IMC are formed, whereas Shen et al. [51] found for Ni/Sn diffusion couple that for the same time and temperature, around 2 µm of Ni_3Sn_4 IMC is formed at the interface as shown in Figure 1.20. Thus the growth kinetics for Ni/Sn IMCs formation is almost 2-3 times slower than for Cu/Sn IMCs formation. For these reasons, Ni is added to metallic pads and also in microbumps between Cu pillar and Sn to limit the growth of IMC at both reactive interfaces. This method has been proven efficient for assembly at 20-50 µm pitch. However, at more *aggressive* pitch (<10 µm pitch), the ratio of IMCs thickness with respect to interconnect height is approaching close to 0.5 which is problematic from a reliability point of view.

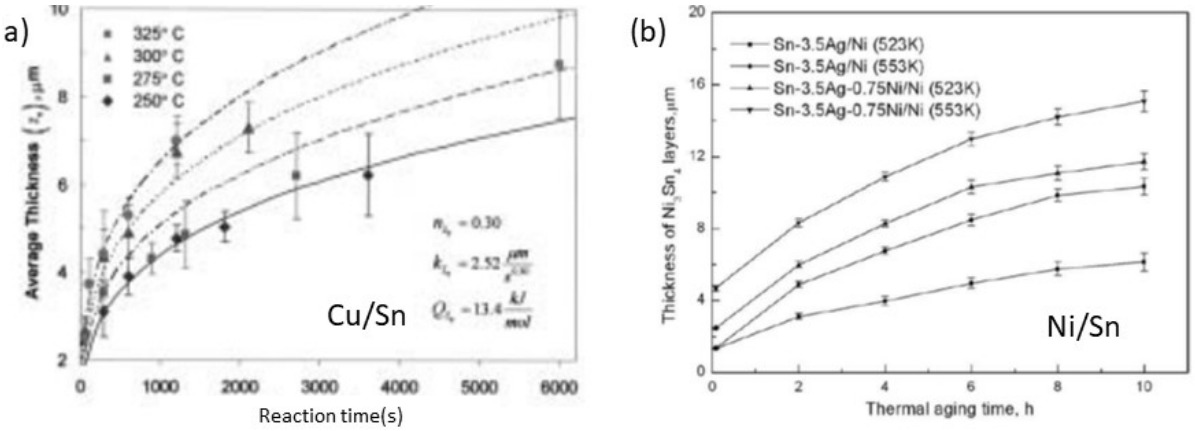


Figure 1.20: Growth kinetics for (a) Cu_6Sn_5 phase in Cu/Sn diffusion couple at different temperatures [50] , (b) Ni_3Sn_4 Ni/Sn diffusion couple at 250°C for different Sn based solder alloys [51]

In this thesis, the interconnect is formed between micropillar i.e. Cu/Ni/Sn-Ag and metallic pad which are Au/Ni as shown in Figure 1.21. During bonding, there are two diffusion couples, one is between Sn-Ag solder and Ni/Au metallic pad (Sn-Ag/Au/Ni couple), which is responsible

for making interconnect and the other diffusion couple is in the microbump side, i.e. between Sn-Ag solder and Cu/Ni (Sn-Ag/Ni couple). The properties and reliability of the interconnect at 10 µm pitch will depend on the properties and stability of the IMCs formed between Ni (Ni/Au) and Sn. Therefore, before developing a flip chip technology it is necessary to define whether the chosen metallurgy is well suitable for the intended application. Thus, the heart of the thesis lies in the metallurgy of microbump (called as Cu pillar in this thesis) and of the formed interconnect.

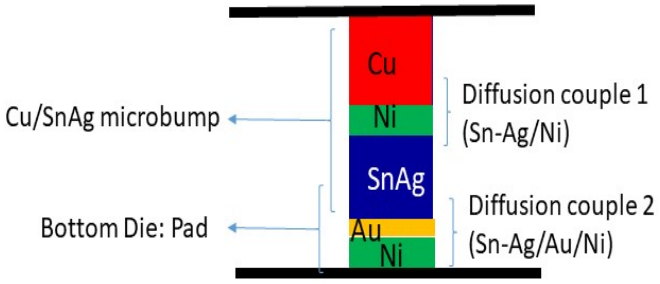


Figure 1.21: Schematic diagram showing diffusion couples present in microbumps during bonding process

The thesis approached the problem in three parts, firstly, in metallurgy area where the materials and interactions are investigated which are responsible for making a joint, i.e. Sn-Ag alloy and Ni. The second part of the thesis addresses the challenges in developing assembly process(es) for fine pitch, keeping in mind, all the challenges associated with it. Lastly, in the third part of the thesis, both metallurgy as well as process are qualified by characterizing the properties of achieved interconnects.

1.6 Literature Review

In this section, firstly, the literature review of state of the art for 10 µm pitch assembly using Sn solder alloy is presented followed by the literature review for the interfacial interactions between Ni and Sn.

1.6.1 Literature review for state of the art for 10 µm pitch using Sn based solder

There are some research groups which evaluated the prospects of microbumping with Cu/Sn-Ag alloy for pitch below 20 µm. Some of the interesting work is briefly presented below.

Tsukuba Research Center [53] in Japan, have developed new packaging technology to realize high density flip chip bonding techniques with 20 µm pitch microbumps through Cu TSV (Through Si Vias) using pre-applied underfilling. They used Si chip (50 µm thick) with each Cu pillar made up of 5 µm Cu and 1.5 µm Sn-2.5Ag and Si interposer (500 µm thick) with 5 µm Cu pads, as shown in figure1.22. They did not perform reflow (i.e. bump formation) after deposition of solder alloy. They aimed for a solid-liquid interdiffusion (SLID) joint, where solder alloy is completely consumed in making intermetallics, therefore bonding was done at 240-450°C with 34.3 N of force. They have achieved 450 mΩ resistance per interconnect.

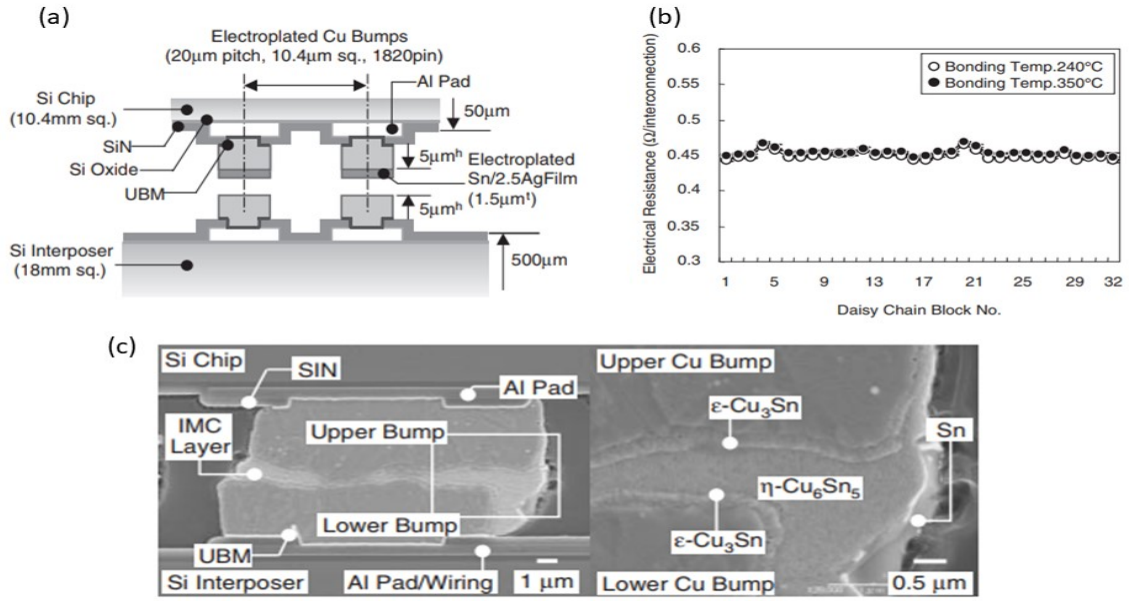


Figure 1.22: 10 µm pitch assembly, (a) schematic diagram for the assembly, (b) electrical resistance graph for formed interconnect (c) SEM image showing the interconnect after bonding at 240°C [53]

Georgia Tech [54], in 2017 investigated different metallurgy combination for achieving 20 µm pitch assembly using thermo-compression and pre-applied underfilling. They proposed a multi-

ple layer system (shown in Figure1.23): Cu pillar/Ni/Cu/Sn-Ag on the pillar side and Au/Ni/Cu on the pad side with Ni as a barrier layer. Their aim was to make a SLID joint with Cu_6Sn_5 after the assembly. The addition of a Ni layer on the pillar side aims to avoid the reaction between Cu pillar and Cu_6Sn_5 layer (with Cu in excess) leading to the formation of Cu_3Sn phase (stable Cu/Cu_3Sn equilibrium). On the other side, i.e. pad metallization, they worked with NiP which is electroless deposited. Au is commonly used as a protective layer against oxidation of Ni, however Au should not be more than 0.1wt% in the joint, otherwise it causes embrittlement of the joint. According to ref. [54], at these dimensions, the Au thickness should be 4 nm to prevent this embrittlement, however it is not enough to protect Ni from oxidation. Therefore, on the pad side they use the multilayer Cu/Ni/Pd/Au system and found that 50nm Pd /50 nm Au multilayer system is sufficient for oxidation protection. It is an interesting approach, however they had some issues with filler entrapments due to the use of pre-applied underfilling. They did not give any results for mechanical and electrical behavior of the interconnects achieved.

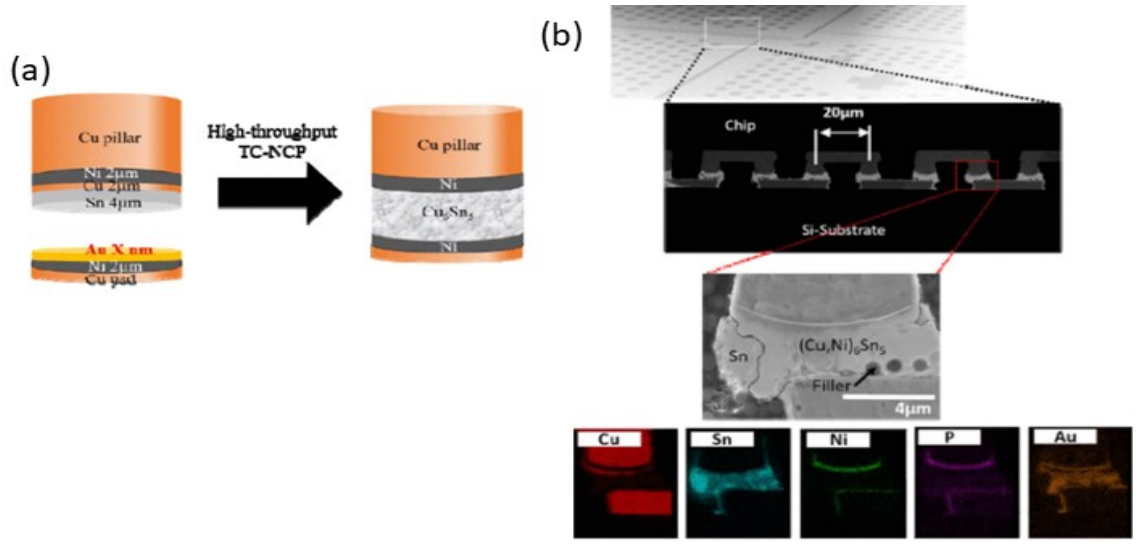


Figure 1.23: 20 µm pitch assembly, (a) schematic diagram showing multilayer Cu pillar and (b) SEM image after assembly [54]

IMEC [55] developed *embedded bumps* for 10 µm pitch assembly as shown in Figure 1.24. Here Sn pillars are fabricated directly on the chip metallization and the pillars are embedded in the polymer. This polymer acts like a pre-applied underfilling. With the help of polymer, they can planarize the solder surface by Chemical Mechanical Polishing (CMP) and increase the uniformity across full wafer. Sn pillars and pads are entrapped within polymer and passivation layer respectively. It is interesting to note that solder pillar has been used in the bonding directly, without forming the bump first. This is done to conserve the thickness of solder for the bonding process because during the bump formation, solder reacts with the chip metallization and forms intermetallics. This process reduces the available volume of solder for bonding and they fear that it may be a potential issue for bonding. Also, despite the fact that the reaction between Ni and Sn is much less rapid that between Cu and Sn, they believe that the use of Ni may not be enough to prevent full consumption of solder. They intend to keep solder joint after the assembly. Therefore, apart from Ni, they also investigated other metallurgy for UBM such as Co to repress the formation of IMCs. The bonding is done by thermo-compression with

10 N force at 350°C. Figure 1.24 shows the embedded bumps and the interconnects after the assembly. However, in this article too, no information regarding electrical and mechanical behavior is provided.

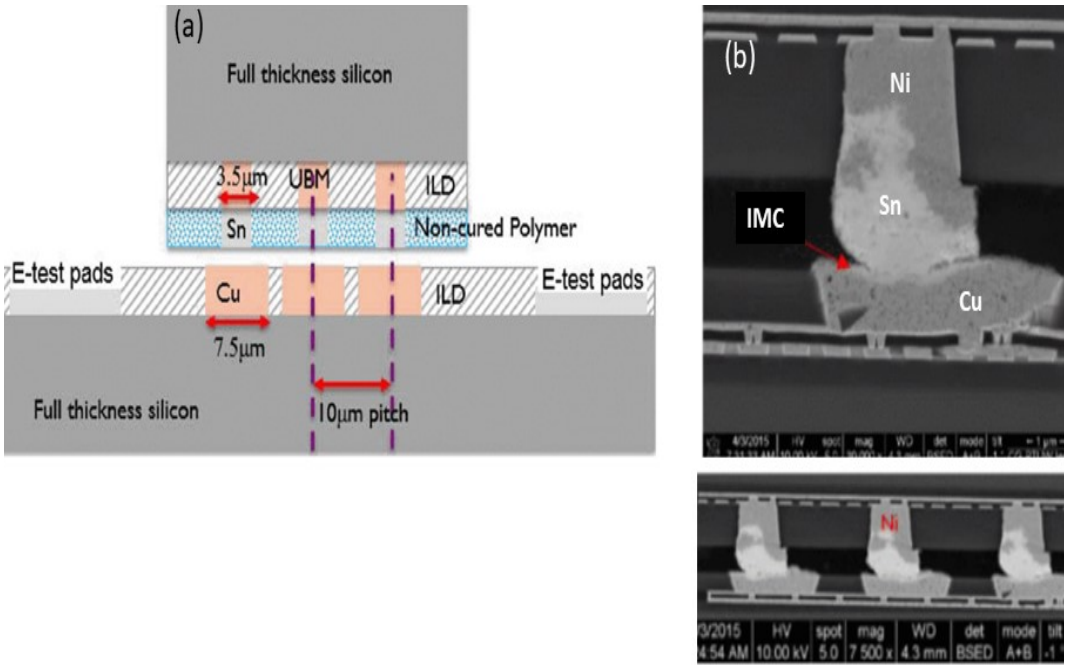


Figure 1.24: 10 µm pitch assembly with bumpless structure (a) schematic diagram and (b) SEM image [55]

Research Triangle Park [56–58] in the USA, has also developed assembly process for 10 µm pitch for both Si on Si assembly and Si on InP assembly for near Infrared Red detectors and results are promising. They are using large format of 640x512 array. Their approach is chip to wafer with Cu/Sn-Ag pillar deposited by electro-chemical deposition and their UBM is also Cu. Here the native oxides are removed by wet chemistry such as diluted H_2SO_4. In their other work they introduced mechanical key to improve alignment using a BCB (benzenecyclobutene). This method is not new for the fabrication industry, it has been used to make low k dielectrics, photosensitive polymers etc. BCB is put on UBM and it creates a space where the microbump will be placed for bonding. The bonding is done at 260-325°C with some force. Interconnect after assembly is shown in Figure1.25. The shear strength of the interconnects achieved after their process is 15 MPa and the resistance per connection reported is 70 mΩ.

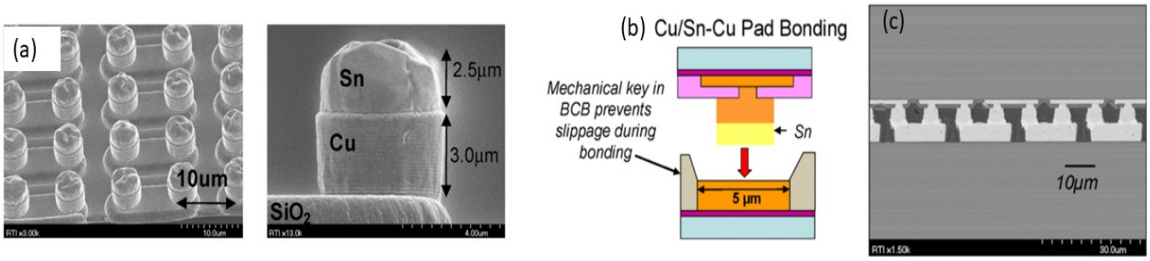


Figure 1.25: (a) SEM images for Cu pillar at 10 µm pitch, (b) schematic diagram showing mechanical key and (c) SEM image for assembly [58]

A Star [59, 60] from Singapore are working on 15 µm pitch assembly with 8 µm diameter of Cu/Sn microbumps. The UBM is Al/Ni-P/Au which is deposited by electroless deposition. In the industry this is known as ENIG (Electroless Ni Immersion Gold). They have worked for adjusting the apt thickness of Sn in microbump. They have found that if Sn thickness is less than 1.5 µm, then during reflow, it is consumed in the formation of intermetallics and if Sn is thicker than 4 µm then during bonding, it will spill on the side walls of Cu and it may interlink adjacent Cu pillars causing a short circuit. Therefore, Sn thickness used is in between 1.5 - 4 µm in 10 µm microbump height as shown in Figure 1.26. This paper however does not provide any information regarding the properties of interconnects formed.

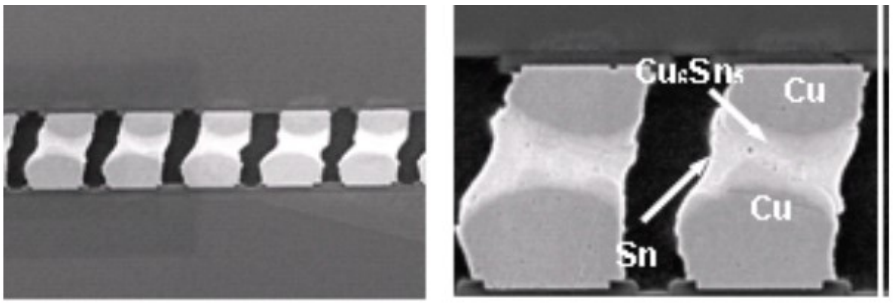


Figure 1.26: SEM image of assembly at 10 µm pitch with Cu/Sn interconnect [59]

In summary, some interesting results has been reported in the literature, different approaches for assembly processes are applied, like mechanical key or with polymer/underfilling, but still the development of 10 µm pitch assembly is in its initial stages. Secondly, the major challenge in all the work presented above lies in choosing the right metallurgy for the joining. Interestingly, all the work focused on forming Cu/Sn SLID joint (except IMEC work). However no in depth work on metallurgy has been done so far, which can cause some serious issues not only for obtaining the interconnects but also for their lifetime performance, i.e. reliability. Therefore, the main challenge dealt in the thesis is the metallurgy for fine pitch interconnects.

1.6.2 PHASE DIAGRAMS AND DIFFUSION

As it was mentioned above, the reactive systems which will be studied in this work are Ni/Sn-Ag and Ni/Au/Sn-Ag systems. The study of interfacial reactions in these systems need the knowledge of phase diagrams as well as the diffusion mechanisms in the growing phase.

The equilibrium phase diagrams of binary Ag-Ni, Ag-Sn and Ni-Sn system are presented in Figure 1.27. The equilibrium phase diagrams involving Au, that are interesting for this study will be presented in chapter 4.

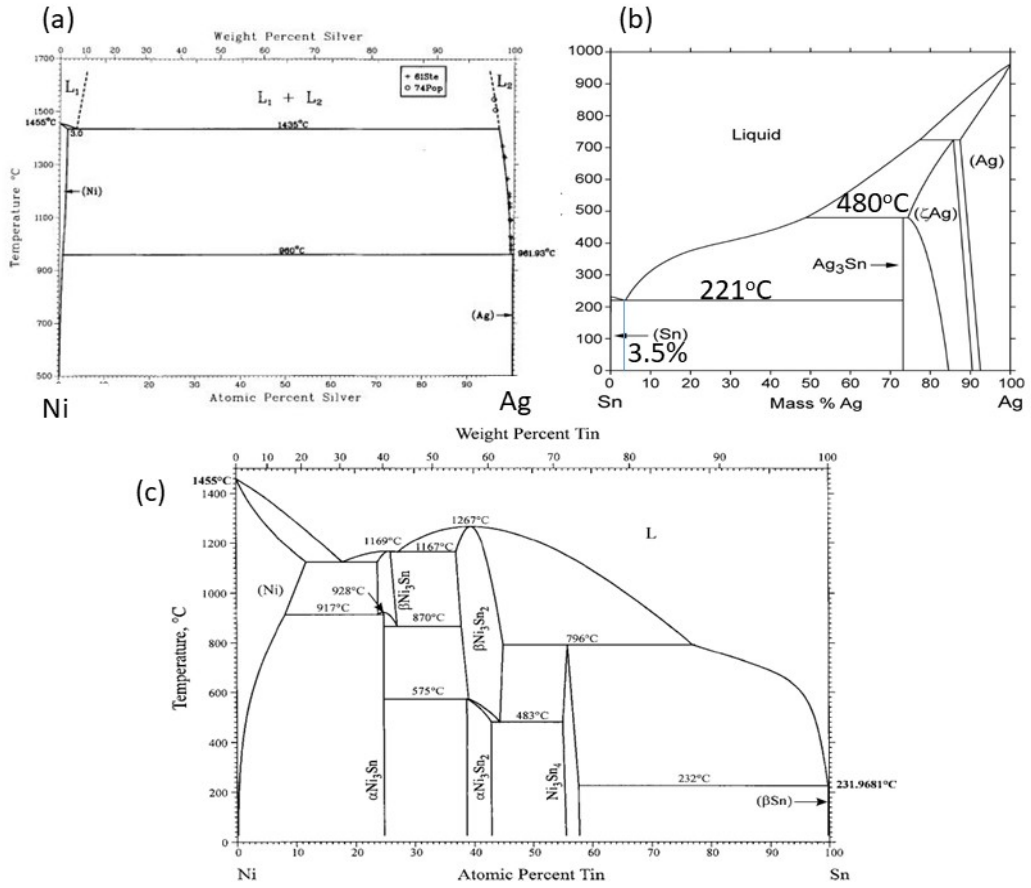


Figure 1.27: Equilibrium Phase Diagrams for binary system (a) Ag-Ni [64] (b)Sn-Ag [65] and (c) Sn-Ni [66]

The phase diagram of the binary Ag-Ni system (Figure1.27 (a)) clearly shows that the interactions between Ni and Ag are extremely weak (no mutual solubility in solid state and existence of a miscibility gap in the liquid state even at T $>$ 2000°C).

In the case for Ag-Sn system (Figure1.27 (b)), an eutectic transformation occurs at 221°C: Liq $\rightarrow$ Ag_3Sn + β-Sn. Two stable intermediate phases exists in this system: Ag_3Sn and ζ-Ag phases. Ag_3Sn phase which plays a very important role on the mechanical properties of Sn-Ag and Sn-Ag-Cu solder alloys, undergoes a peritectic decomposition at $\sim$ 480°C. No mutual solubility in solid state exists between Ag and Sn. It is reported in the literature that in the Sn/Ag diffusion couples only the Ag_3Sn phase is detected [62].

In the case of Ni-Sn system, below 300°C as seen in Figure 1.27 (c), an eutectic transformation occurs at 231°C: Liq $\rightarrow$ Ni_3Sn_4 + βSn. In this temperature domain, there are three stable intermetallic phases in this system: Ni_3Sn, Ni_3Sn_2 and Ni_3Sn_4. For temperatures below 221°C, the solubility of Ni in Sn and Sn in Ni is almost zero. It is widely reported in the literature that the only phase that grows at the Ni/Sn diffusion couples for T $<$ 240°C, is the Ni_3Sn_4 [47, 63]. This important point, for theoretical and practical applications, will be discussed in detail in chapters 3 and 4.

Diffusion-generalities

The formation and the growth of IMCs occurs as a result of reactive diffusion between two intimate metallic layers. Diffusion by definition is the net movement of molecules/atoms from region of high chemical potential (in general with high concentration) to the region of low chemical potential (in general with low concentration).

The diffusion flux of a component i (J_i) in a given phase is given by Fick's laws by the following equation:

$$J_i = -D_i \frac{dC_i}{dx} \tag{1.1}$$

Here, J is the diffusion flux (in mol.m^{-2}.s^{-1}), D is the diffusion coefficient of component i (in m^2.s^{-1}), C is the concentration (in mol.m^{-3}) and x is the space coordinate.

The variation of the diffusion coefficient with the temperature obeys to the Arrhenius law:

$$D_i = D_i^o exp \frac{-Q}{RT} \tag{1.2}$$

Here, D_i^o is a pre-exponential factor, R is the gas constant and Q is the activation energy of the diffusion process (in J.mol^{-1}).

The growth kinetic of intermetallic (IMC) compounds between two reactive metals is extensively studied in the literature [28–30, 68–70, 72]. In general, the growth kinetics of IMC layers can be controlled by the diffusion process and/or by the reaction kinetics at the reactive interfaces.

There are mainly 2 rate controlling diffusion mechanisms: volume diffusion and grain boundary diffusion. Volume diffusion refers to atomic diffusion within a crystal lattice. Diffusion occurs due to point defects which are present in the crystal, which may be interstitial or substitutional vacancy, whereas if solute diffuses through the grain boundaries, which are 2D defects then this type of diffusion is called grain boundary diffusion. They are schematically shown in Figure 1.28.

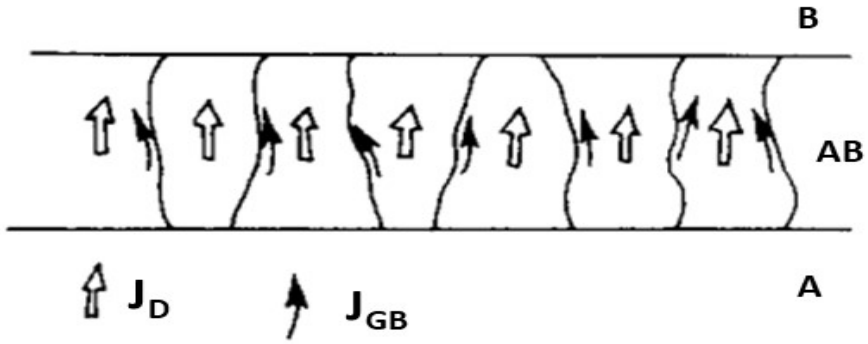


Figure 1.28: Schematics showing different mechanism for diffusion. J_D is diffusional flux due to volume diffusion and J_{GB} is diffusion flux due to grain boundary diffusion [73]

When the growth kinetics of IMC layers is limited by the reaction kinetics at the reactive interfaces, the thickness (e) of the IMC layer follows a linear growth law:

$$e = k.t \tag{1.3}$$

were k is a kinetic growth coefficient and t the reaction time.

When the growth kinetics is controlled by volume diffusion, the growth kinetics follows a parabolic law:

$$e = k.t^2 \tag{1.4}$$

As we will see in Chapter 3, the growth mechanisms of the IMC layers are often complex. Thus the growth kinetics is determined experimentally and it is represented by the following equation

$$e = k.t^n \tag{1.5}$$

Here k is the kinetic coefficient of growth and n is a growth exponent. The experimental values of k and n can be used to determine the rate limiting diffusion mechanism and by further evaluation, diffusion coefficient can be determined. This point will be discussed in detail in Chapter 3.

1.6.3 Literature survey for Ni/Sn interactions

Interfacial reaction between solid Sn and Ni

The studies based on solid Sn/Ni interactions are mostly comparative studies between different Ni based UBMs and/or various Sn based solders. Some authors compared the electrodeposition of Ni with electroless deposition of NiP while others compared the effects of different additives in Sn solder such as Ag, Cu, Pb. The Sn/Ni diffusion couples were formed differently in different studies. Despite of all the variations in these studies, all of them unanimously agreed that during the reactive interaction between Ni and Sn, only Ni_3Sn_4 IMC phase is formed at the interface. Some of the key studies are summarized below.

Mita et al. [74] studied the solid Sn interactions with Ni with traditional diffusion couple made between Sn plates and Ni plates, without prior soldering (i.e. without heating above the melting temperature of Sn). The interactions were studied for three temperatures 150, 180 and 200°C up to 1200 hrs. Figure1.29 shows the IMC layer after annealing at 150°C and 200°C. For annealing temperatures, 180 and 200°C, a continuous scalloped shaped Ni_3Sn_4 IMC were formed at the interface. However, at 150°C, granular shaped (non continuous) Ni_3Sn_4 IMC was formed. According to the authors, this may be due to difficulty of nucleation at this temperature. The growth kinetic coefficient obtained at 180°C and 200°C is n=0.45 and n=0.40 respectively. The activation energy of formation of IMC is found to be 116.2 kJ/mol.

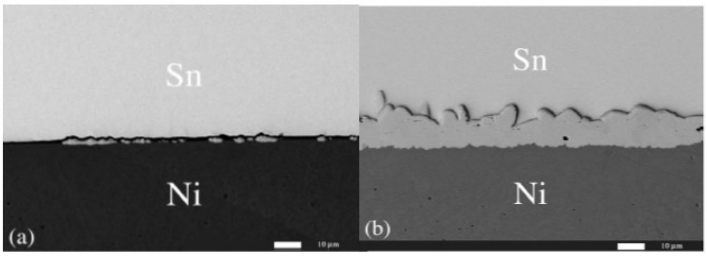


Figure 1.29: SEM micrographs showing IMC formed at Ni/Sn interface after (a) 150°C for 600 hrs (granular, non continuous IMC) (b) 200°C for 1200 hrs (continuous scalloped shape IMC) with traditional diffusion couples [74]

Ishikawa et al. [75] evaluated the interfacial reactions with electrodeposited Ni with Sn solder balls. The contact is formed after reflow at 260°C which was done twice in the presence of flux. After forming the initial contact, the diffusion couples were isothermally aged at 135, 150, 175 and 200°C for 500 hrs to 2000 hrs. They also observed scalloped shape IMCs (as shown in Figure1.30) however 2 growth regimes with different activation energy were observed, for temperature i.e. above 175°C, Q is equal to 178 kJ/mol and for temperature lower than 175°C, Q=80 kJ/mol. According to the authors, the difference was due to the change in the mechanism of diffusion below and above 175°C. At lower temperatures the growth is governed by grain boundary diffusion whereas at higher temperature, the diffusion mechanism changes to volume diffusion.

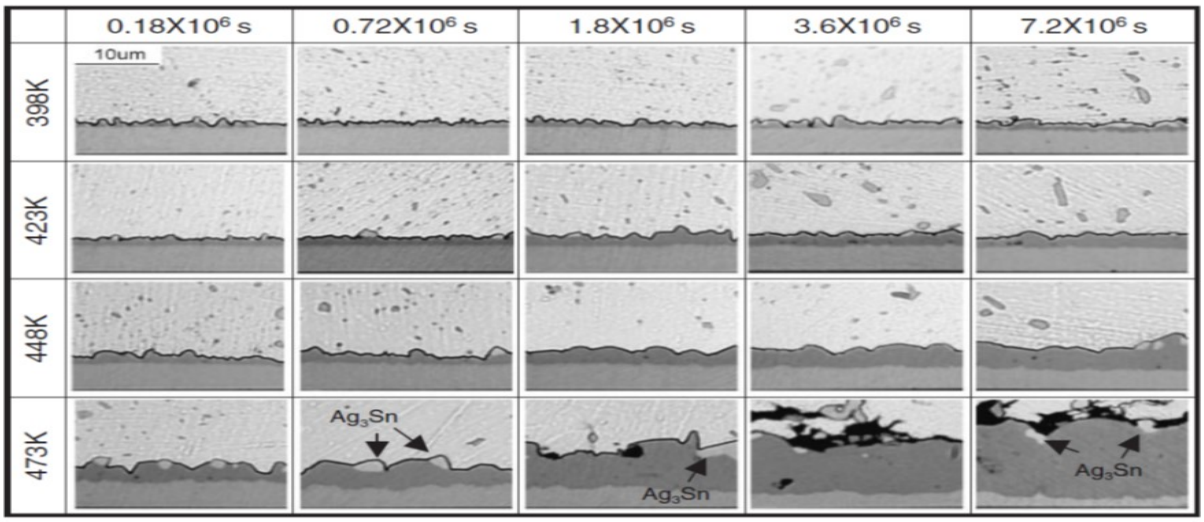


Figure 1.30: SEM micrographs for IMC after isothermally aging of diffusion couple made by Ni electrochemical deposition with Sn balls [75]

Chaung et al. [76, 77] investigated the difference in the rate of formation of Ni_3Sn_4 IMC in case of two solder alloys, Sn and Sn-2.4wt%Ag. Here too, Ni/Sn/Ni and Ni/Sn-2.4%Ag/Ni diffusion couples are formed by electrochemical deposition. The couples were aged without any prior reflow for temperatures 150-200°C up to 528 hrs. They have found that Sn-Ag alloy reduces the rate of formation of Ni_3Sn_4 as compared to pure Sn solder. The growth exponent (n) and growth kinetic coefficient (k) for reaction with Sn are n=0.3-0.5 and k=0.154 μm/hr$^{0.5}$ whereas for Sn-Ag, n=0.27 and k=0.061 μm/hr$^{0.5}$ (as shown in Figure 1.31). Secondly, in case of Sn solder, few voids appeared due to volume contraction (11.3% for Ni_3Sn_4) which were not observed in case for Sn-Ag solder alloy.

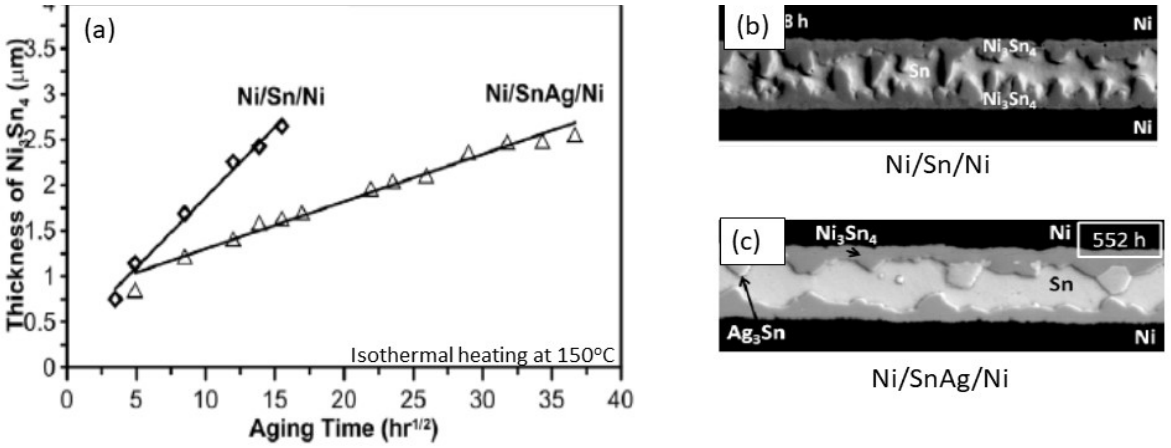


Figure 1.31: (a) Reaction kinetics for Ni/Sn(5 μm)/Ni and Ni/Sn-Ag(7 μm)/Ni diffusion couple made by Ni/Sn electrochemical deposition, (b) SEM micrographs for Ni/Sn/Ni diffusion couple after 28 hrs of annealing at 180°C and (c) SEM micrographs for Ni/Sn-Ag/Ni diffusion couple after 552 hrs of annealing at 150°C [76, 77]

Tang et al. [78] is the only study that is dedicated to the initial stages of interaction between solid Sn and Ni, where the diffusion couples are formed by electrochemical diffusion and no prior reflow is done before isothermal aging. The aging was done at 150-225°C for 1-8 hrs. Some SEM micrographs of the interface after aging are shown in Figure 1.32. The growth exponent of Ni_3Sn_4 IMC is found to be n=1/2 and the activation energy is 39 kJ/mol. However, author did not comment on the mechanism of growth of Ni_3Sn_4 layer.

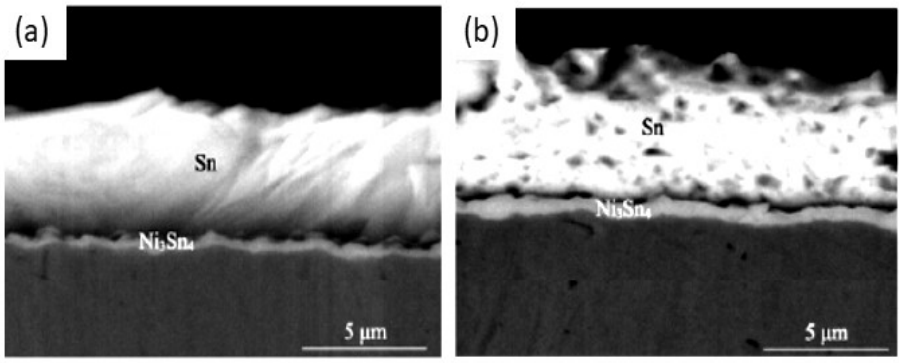


Figure 1.32: SEM micrographs for Ni/Sn couples showing IMC after annealing of diffusion couple prepared by electrochemical deposition at (a) 150°C, 2 hrs (b) 150°C, 8 hrs [78]

Some studies are also presented for Ni which is electroless deposited, however in these case the deposited layer is NiP not Ni. Wang et al. [79] investigated the interfacial reactions between a NiP layer covered by a thin layer of Au (NiP/Au) and Sn-Cu solder alloys and corelated with the mechanical strength of the interconnection. The studied diffusion couples were NiP/Sn, NiP/Sn-0.7Cu and NiP/Sn-3.0Cu. The initial contact was established by performing reflow at 250°C. The isothermal heating is done at 120-200°C from 100 hrs to 500 hrs. After 5 mins of reaction, two IMCs were formed at the interface, Ni_3Sn_4 and Ni_3P. Different morphologies of IMCs were observed for different solder alloys. For Sn-0.7Cu, needle shaped IMC was observed whereas for pure Sn, smooth continuous scalloped shape IMCs were observed as seen in Figure1.33. However, for solder having higher Cu content, the needle shaped IMC were suppressed and a continuous uniform Ni_3Sn_4 layer was formed. The activation energy in this case was found to be 42 kJ/mol.

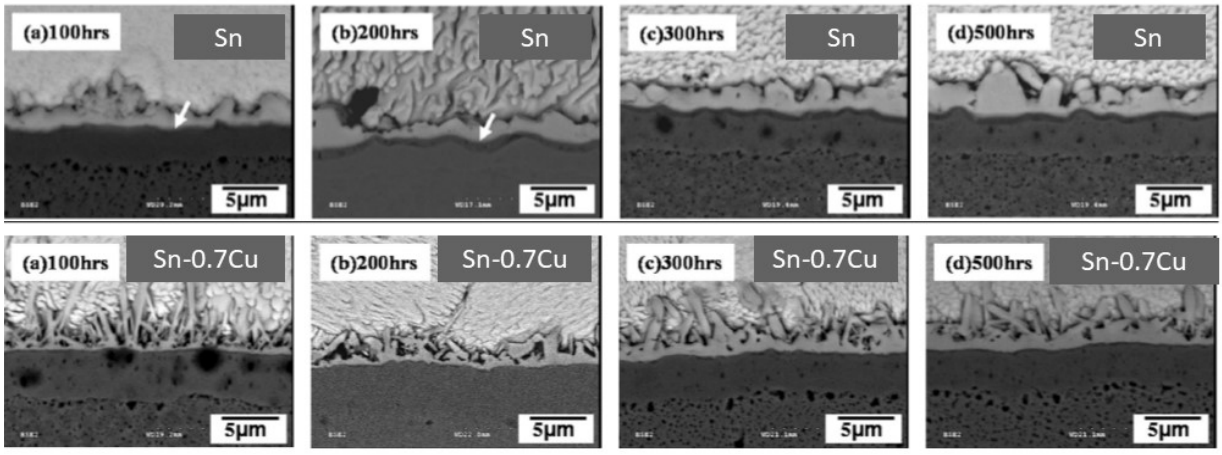


Figure 1.33: SEM micrographs for diffusion couple made by NiP sheets with solder balls and reflow for 1 min at 250°C and annealed at 150°C [79]

In almost all the studies reported in the literature on the interfacial reactions between solid Sn or Sn-based alloys and Ni, the growth exponent is found to be between 0.4-0.5, however the values reported for growth kinetic constant and activation energy are highly diverse [76, 77]. This can be seen in Figure1.34. where different law growth obtained from different authors are reported. It is very important to note that, in the literature, there is almost no study dedicated to the initial stages of solid Sn-Ni interactions (no study for reaction time lower than 1 hour or even lower than 4 hrs).

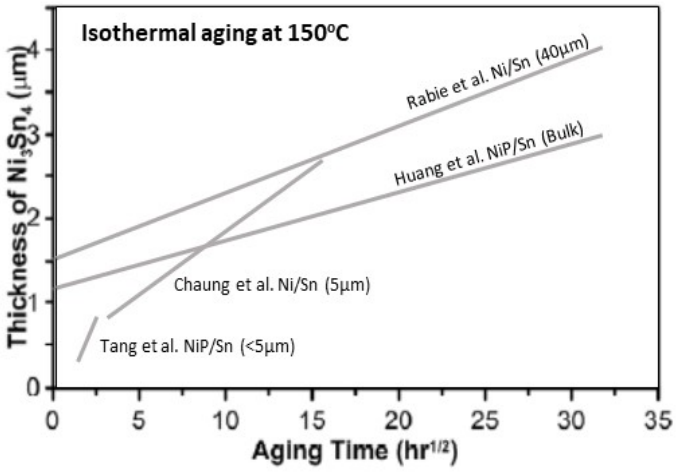


Figure 1.34: Literature review for growth kinetics for Ni_3Sn_4 at 150°C [76–78, 80, 88]

Interfacial reaction between liquid-Sn and Ni

In the past two decades, numerous studies have been conducted on the kinetics of interfacial reactions between Ni substrate and liquid Sn-based solder alloys [51, 63, 89, 90, 92, 93, 95, 96]. The common conclusion of most of these studies is that in Ni/liquid Sn-based solder interactions at 230°to 350°C the only phase that grows at the interface is the Ni_3Sn_4 phase. This also goes in line with the study of Gur et al. [63], which concluded that for growth of Ni_3Sn_2 and Ni_3Sn phase, the temperature should be above or at least 350°C. However the reason why there is a huge difference in the morphology and the growth kinetics (in particular, the growth exponent n but also the growth kinetic coefficient k) of the IMC layer formed at Ni/liquid Sn interface, reported by different research groups, is not clear. Some of the most important studies are summarized as follows.

Shen et al [51] studied the interfacial reactions of Ni plates with eutectic Sn-3.5%Ag and Sn-3.5%Ag0.75%Ni alloy. The initial contact in this study was done by performing reflow and then the diffusion couples were isothermally annealed at 250°C and 280°C for times up to 10 hrs. They have observed scalloped shape Ni_3Sn_4 IMC for 5 mins and 6 hrs for eutectic Sn-Ag solder alloy, which gradually changes to facetted IMC (as seen in Figure1.35). After 10 hrs of annealing, both morphologies of IMC were present, scalloped as well as facetted. However for Sn-Ag-Ni solder alloy, only facetted morphology was present for all annealing times. Although the growth kinetics of IMC with both alloys was almost similar, it was slightly lower for Sn-Ag-Ni. The value of growth exponent n was found to be 0.32 and 0.30 for Sn-Ag and Sn-Ag-Ni alloy respectively.

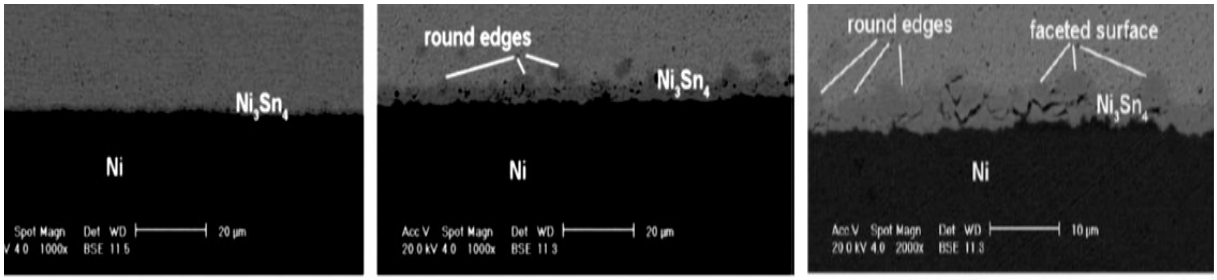


Figure 1.35: SEM micrographs for diffusion couple prepared by Ni and Sn plates, showing scalloped and facetted shape Ni_3Sn_4 IMCs after annealing at 250°C [51]

Gorlich et al. [89] evaluated very early stages (some seconds) as well as very late stages (few days) of Ni/liquid Sn interactions during isothermal heating at 250°C. The diffusion couple was prepared using a ball drop method, where the Sn solder ball is dropped on Ni sheet and with the help of the Rosin Mild Activated flux, the surfaces were deoxidized and heated at 250°C and isothermal annealing were performed for 10 secs to 4 hrs to study the initial stages of reaction. For later stages of reaction, the diffusion couples were reflowed initially for 10 secs at 250°C and then isothermally heated from 4 hrs to 7 days.

The characterization of the reactive interface showed that IMCs were formed with elongated rod like shape morphology. Authors observed, 3 different growth regimes shown in Figure1.36: (i) at very early stage i.e. from 0-3 mins the growth exponent is n = 1/3 and the growth kinetic coefficient k_1= 75±10 μm^3/min, (ii) at intermediate stage i.e. 3-35 mins, n_2=1/2 and k_2 =

4.8±0.3μm^2/min and (iii) at latter stages i.e. form 4 hrs to 7 days, n_3 is also 1/2 but k_3= 12.5 ±0.5 μm^2/min which is much higher than k_2. To analyse the growth mechanism, they studied the grain growth and determine the diffusion mechanisms behind each growth regime and found that in the initial stages, grain boundary diffusion dominates which later gets substituted by formation of new grains and liquid channels (see Figure1.37).

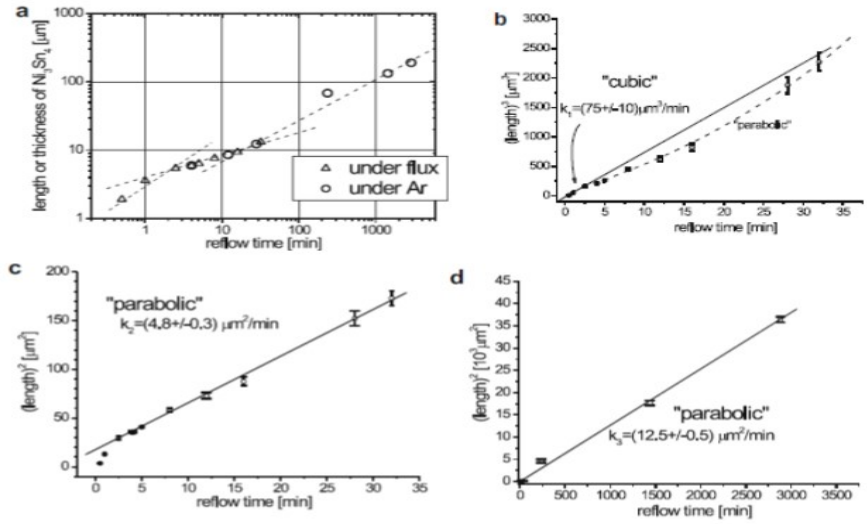


Figure 1.36: Reaction kinetics showing 3 kinetics regime for growth of Ni_3Sn_4 IMC formed in Ni/Sn diffusion couple prepared by Ni sheets and Sn balls, (a) log of Ni_3Sn_4 thickness vs log of time, (b) initial stages (c) intermediate stages and (d) latter stages [89]

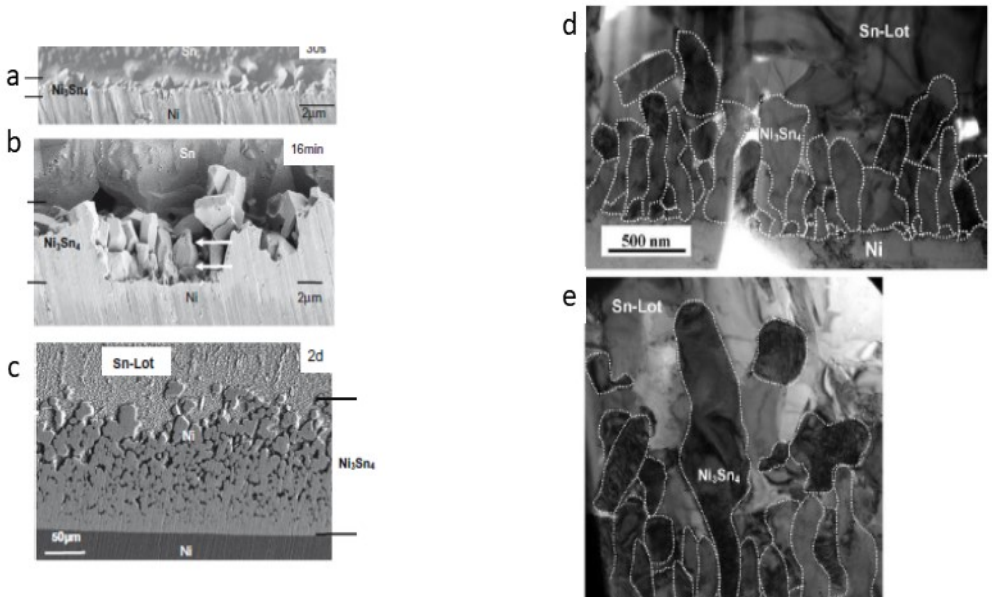


Figure 1.37: SEM micrograph showing Ni_3Sn_4 IMC thickness after annealing at 250°C, (a) 1.9 μm after 30 secs, (b) 9.4 μm after 16 min (c) 191 μm after 2 days, TEM micrographs showing the grain structure and size of IMC layer after (d) 10 secs and (e) 60 secs of annealing at 250°C [89]

Lis et al [90] performed the only work dedicated to Ni/liquid Sn diffusion couples performed by electrochemical deposition. They also studied the initial stages of reaction (10 secs-10 mins) and compared it to the later stages of reaction (up to 15 hrs). After deposition, the interface between Sn and Ni is smooth and continuous and no IMC layer is present as shown in figure 1.38. They have found 2 regimes for the growth kinetics of Ni_3Sn_4 intermetallic layer. At the very early stage, interestingly, a long needle shaped IMC was formed. This IMC in needle shape grew in the height (without thickening) till 3 mins and after that a thin Ni_3Sn_4 IMC needle started to densify and formed a continuous layer at the interface (see Figure1.39). Both regimes present a parabolic growth law as it is shown in Figure 1.39 (d). The parabolic growth constant for the first regime between 0-3 mins ($k_1 = 1.8x10^{-10}$ cm^2/sec at 250°C and 1.410^{-10} cm^2/sec at 300°C) is much higher than that for the second regime after 3 mins ($k_2 = 2.3x10^{-11}$ and $5.6x10^{-11}$ cm^2/s at 250 and 300°C respectively).

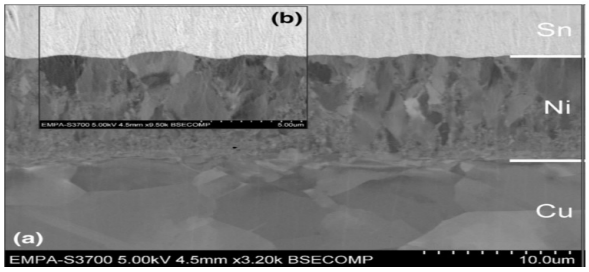


Figure 1.38: (a) SEM micrographs for the initial stage, (i.e. as deposited) of Ni/Sn diffusion couple prepared by electrochemical deposition, (b) enlarged micrograph showing the interface between Ni ans Sn [90]

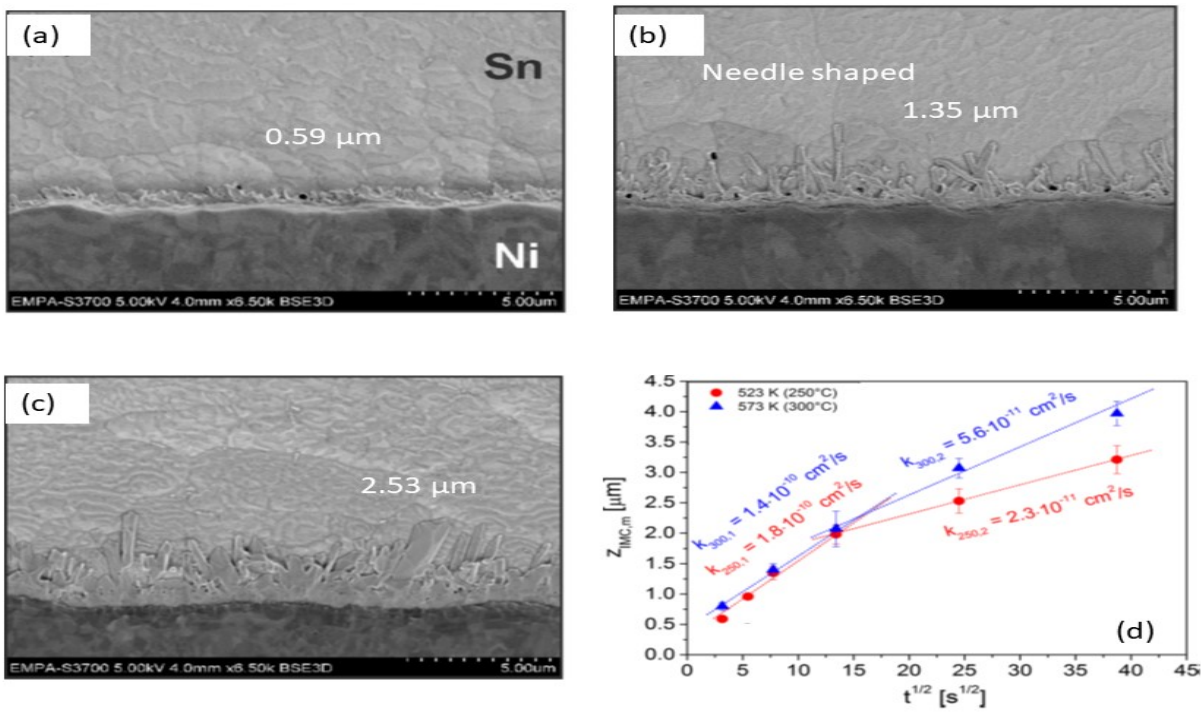


Figure 1.39: SEM micrographs for diffusion couple prepared by electrochemical deposition annealed at 250°C, (a) 10 secs (b) 60 secs (c) 10 min and (d) Growth kinetics for Ni_3Sn_4 layer [90]

Lin et al. [91] evaluated the growth kinetics of IMC layer between Ni and different liquid solder alloys (Sn, Sn-Ag, Sn-Bi and Sn-Pb) and found that only Ni_3Sn_4 phase was present as a reaction product. Figure 1.40 shows that the growth kinetics of IMC layer follows a parabolic growth law for all solder alloys. As it can be seen in this figure, due to the addition of different solutes in liquid Sn, the growth rate of IMC layer decreases. Moreover, the activation energy increases from 28 kJ/mol for Sn to 32 kJ/mol for Sn-Pb alloys. Similar observations were reported in the case of solid Sn interaction with Ni studied by Chuang et al. [76, 77]

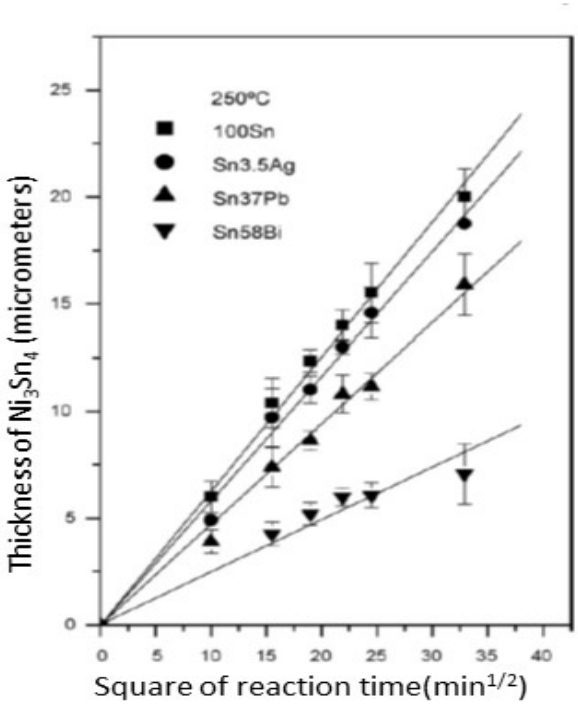


Figure 1.40: Comparison of growth kinetics for growth of Ni_3Sn_4 IMC at 250°C for different diffusion couples prepared with Ni plates and different types of solder alloy [91]

In the literature, there are only two studies dedicated to the initial stages of reaction between liquid Sn and Ni. However, the results reported in these studies are not corresponding to each other. Gorlich et al. [89] observed the growth of 3.6 µm for Ni_3Sn_4 IMC layer in 1 min at 250°C as comparison to 1.6 µm for Lis et al [90]. Thus, there is an ambiguity in the results which might be due to the way the diffusion couple is made or in the experimental condition. Nevertheless, the mechanism and the main factor(s) on which the growth of the IMC layer depends is still unclear.

Conclusion

In this chapter, the overview of electronic packaging is given and the challenges associated with miniaturization of microelectronic components are presented. In coming years, 10 µm pitch is going to be a reality and therefore the challenges associated with this pitch must be addressed. There are other promising methods such as Cu-Cu bonding, microtubes, however

the major challenge associated with them is their adaptability. Therefore, the prospects for the traditional Cu/Sn-Ag microbump which are well suitable to the electronic industry must be evaluated, which is the main aim of the thesis. While there are many challenges associated with this pitch, the thesis focused on the metallurgy of the bumps, its evolution with time and how this metallurgy affects the properties and the lifetime of the interconnects and finally the package.

The main metallurgical interaction in the microbump studied in this thesis is between Sn and Ni. This interaction occurs in two states, in liquid state and solid state. The liquid Sn/Ni interactions, which contribute significantly to the IMC growth, are somewhat extensively studied in the literature. However, there is a discrepancy in the results published in the literature and briefly discussed in this chapter. Moreover, the first very short time interactions between liquid Sn and Ni are studied by only two teams and the experimental results are not corresponding to each other. The same extensive and in-depth studies are not performed for solid Sn/Ni interactions, mainly because it does not contribute much to the growth of IMC layer like liquid Sn/Ni interactions. Nevertheless, as 10 µm (and below) pitch are in question, we can no longer ignore this factor as its contribution now becomes quite significant at this scale. Hence, in this work, in Chapter 3, the solid-state interactions in Sn/Ni system are also studied in detail along with liquid-solid interactions in order to determine the mechanisms and the factor responsible for the IMC growth during the initial stage of these interactions.

After studying the Sn/Ni interactions, the assembly processes are designed, the interconnects are studied and the experimental results are presented and discussed in Chapter 4. For the assembly, there are two choices, one is to tailor the assembly process such that the IMCs are formed as least as possible and the other choice is to let the joint become completely transformed into Ni_3Sn_4 IMC. The second choice leads to a Ni-Sn SLID joint. Now it is interesting to compare these two metallurgies for the interconnect at this pitch in terms of their electrical and mechanical behavior. Also, it would be more interesting to investigate the evolution of the metallurgy system for both interconnects with time at higher temperatures.

Chapter 2

Assembly Process and Characterization Methodologies

Contents

INTRODUCTION

As presented in the previous chapter, the aim of this thesis is to evaluate the prospects for 10 µm pitch assembly with Cu pillars which is done in three steps. In this chapter, the experimental procedure, tools and methodology used throughout the thesis are described. For the evaluation, firstly, the interfacial reactions between different metallic layers that are responsible for making a bond is studied. After understanding these interactions, assembly process(es) is/are designed.

The first requirement for these studies, is to fabricate the components required for the assembly at 10 µm pitch. Although fabrication for Cu pillars are well adapted in packaging industry, however when they are scaled down to 5 µm, some challenges starts to appear, which are encountered by making some modifications in the fabrication process. After the fabrication of pillars and metallic pads, assembly is performed, which consists of 3 main steps: reflow, bonding and underfilling. Each step is important and serves different purpose in the package. To validate the assembly process for 10 µm pitch, qualification levels are designed, which at the end will provide the definition of *good* assembly process. During these qualifications the interconnects are characterized mechanically and electrically and their properties are also tested over time under different conditions to evaluate their reliability.

In this chapter, in the first section, the test vehicles used for the assembly at 10 µm pitch, for the study of interfacial reactions and for electrical tests are presented. The fabrication process used and the key modifications done for making Cu pillars at 10 µm pitch are laid down. In the second section, all the various steps of assembly procedure are described with the description of the equipment used for each step. The methods used for sample preparation are presented in the third section followed by the presentation and explanation of characterization techniques in the fourth section. In the last (fifth) section, the qualification steps for the assembly process are laid down and the characterization methods used for each qualification step are also explained.

2.1 TEST VEHICLES

10 µm pitch assembly is investigated at chip to chip level, where both the components, top and bottom chip are fabricated on silicon. In this study, the top chip (die) is with Cu pillar and solder alloy *(pillar side)* and the bottom chip is with metallic pads *(pad side)*. In the assembly interconnects are formed by soldering process. Figure 2.1 shows the schematic diagram of these components before and after bonding.

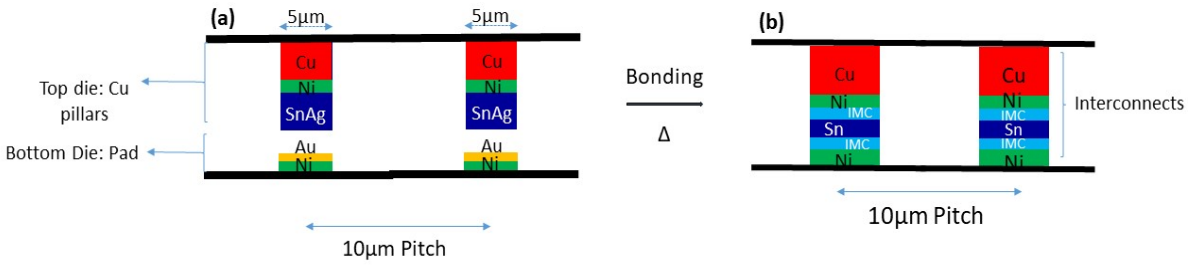


Figure 2.1: (a) Schematic diagram for top and bottom chip (die) before bonding and (b) interconnect after bonding

2.1.1 Fabrication of Cu pillars and metallic pads

In this study Cu pillars and metallic pads are fabricated over 200 mm wafers.

Cu pillar fabrication

Electrochemical deposition is used for fabrication of these Cu/Ni/Sn-Ag pillars (Cu pillars). It is the most commonly used method in the microelectronic industry. Figure 2.2 shows the steps involved in fabrication of Cu pillar. Firstly, seed layers of Ti (100 nm) and Cu (50 nm) are deposited by sputtering using Endura 5500 equipment. The thickness of the deposited layer is controlled by measuring sheet resistance (R^2). The Cu seed layer thickness is lesser than normally used, which is done to prevent larger undercuts (this will be discussed latter in this section). This step ensures the uniform current distribution for electroplating.

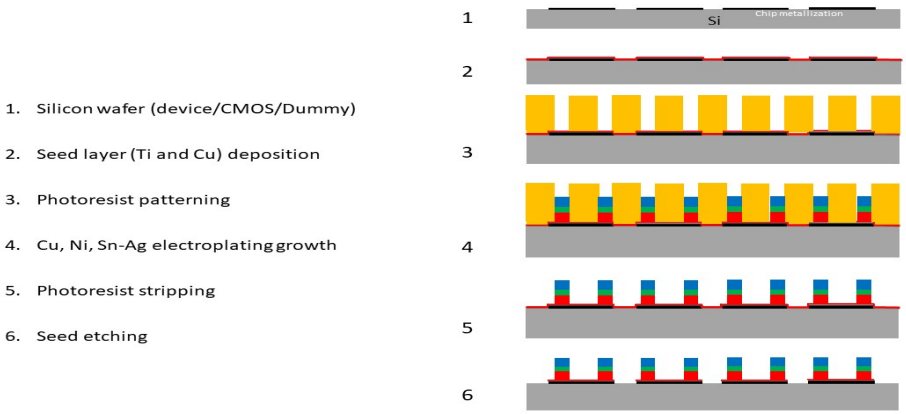


Figure 2.2: Schematic presentation for fabrication of Cu pillars

Afterwards, cleaning is done to remove oxide from the seed layer and then photoresist is deposited. Here, the aspect ratio of photoresist, i.e. the ratio between opening diameter and the height is crucial as it is one of the important parameter for choosing the thickness of each layer within the Cu pillar. Generally, such a small opening (diameter = 5 µm) is difficult to achieve with thicker photoresist, therefore the choice becomes difficult. The photoresist used in the study is AZ4562 (positive photoresist) which is 8 µm thick which permits 7 µm height of Cu pillar with the opening of 5 µm (i.e. diameter of pillar). Due to limited height of photoresist, the thickness ratio between Ni and Sn-Ag alloy becomes critical. It should be chosen such a way that after complete reaction (i.e. formation of Ni_3Sn_4), solder alloy should be the first one to be consumed. By mass balance, 1 µm of Ni will react with 3.3 µm of Sn-Ag to form 3.8 µm of Ni_3Sn_4. Thus 1 µm of Ni and 3 µm of Sn-Ag is chosen in pillar along with 3 µm of Cu pillar for standoff height for the interconnect. Cu pillar is required for electrical conductivity and it cannot be replaced entirely by Ni due to the lower resistance of Ni towards electromigration as compared to Cu [99].

After the deposition, photoresist is patterned by UV photolithography. The patterning is done by stepper (alignment accuracy = ±250 nm) from ASM 100 equipment. It gives higher resolution than traditionally used Mask aligner (±(1-5) µm). The photoresist is exposed to UV rays

and later developed to remove photoresist which is not exposed. The surface is then activated by using oxygen plasma which makes the surface hydrophilic. This is followed by electro-chemical deposition, done in Raider (manufactured by Applied Material) where wafers are immersed in different chemical baths to grow Cu (3 µm), Ni (1 µm) and Sn-2wt%Ag alloy (3 µm). The SULA TS507 chemical bath from Mitsubishi is used for the deposition. The current density and the bath chemistry used during this step control the thickness, the grain size and the composition of the layer [100–102]. At the end of the deposition, the photoresist is stripped and the seeds are etched. The etching step is the critical challenge which will be discussed later in this section. A SEM image of such pillars are shown in Figure 2.3.

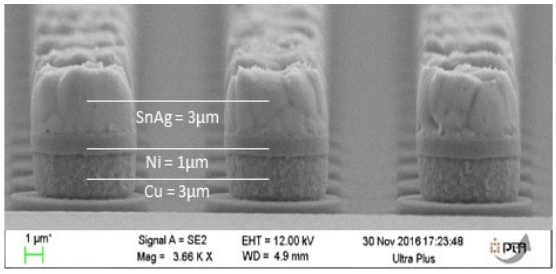


Figure 2.3: SEM image of Cu pillars after fabrication

Metallic pad fabrication

Figure 2.4 shows a schematic diagram for the different fabrication steps for the metallic pads. These are deposited by physical vapour deposition. For the fabrication of pads, first Ti (40 nm), Ni (750 nm) and Au (100 nm) are sputtered by Endura 5500 equipment on Si wafer (same as Cu pillars). Afterwards, photoresist is deposited. Here since high aspect ratio is not required, 1.5 µm thick JSR420 is used. It is also patterned by UV photolithography and followed by an etching step. During etching the part of the metal layers which are not protected by photoresist are removed. This is also discussed latter in the section along with seed etching for Cu pillar. At the end of the process, the photoresist is stripped. A SEM image of a fabricated pad is given in Figure 2.5

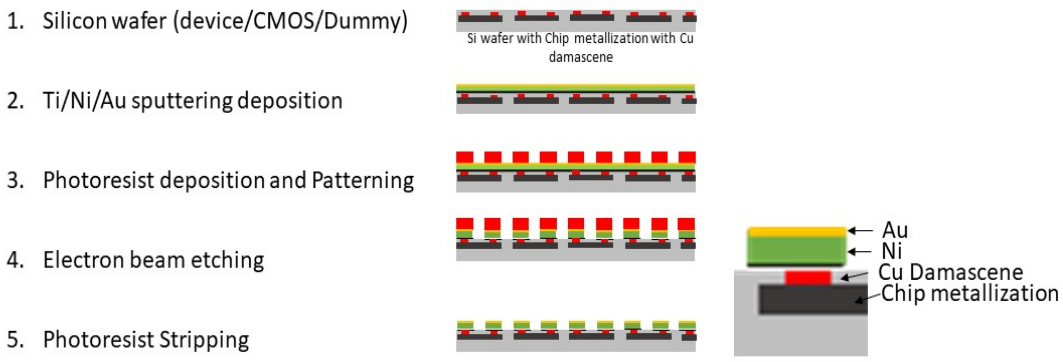


Figure 2.4: Schematic presentation for fabrication of metallic pads

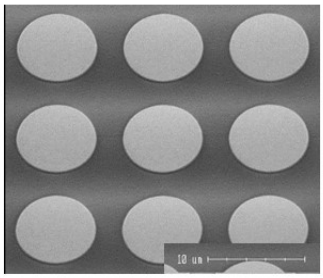


Figure 2.5: SEM image of as deposited metallic pads of 6.5 µm in diameter

2.1.2 Major challenge in fabrication of Pillars and Pads : Etching Process

One of the main challenge at these small dimensions, is the etching step: seed etching for Cu pillars and unprotected metal etching in the case of pads. Broadly, there are two types of processes for etching: (i) *Wet process* that uses wet chemistry and (ii) *dry processes* which may be chemical or physical in nature.

At larger dimension, in the industry, this step is done by *wet chemical etching* which is isotropic in nature, i.e. etches equally in all the planes. Due to its isotropic nature, it etches the metal at the foot of the pad and/or the pillar leading thus to the formation of a step commonly called undercut as shown in Figure 2.6. This undercut compromises the mechanical strength of the fabricated structure. At larger dimension, this is not a major issue, however for the smaller dimensions, it can cause a serious problem. Therefore, it may not be suitable for etching at these small dimensions.

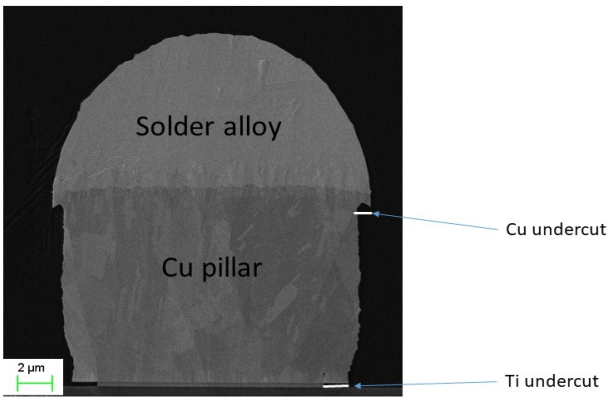


Figure 2.6: SEM image for Cu pillar after Cu seed etching, showing Cu and Ti undercut

The second type of process is *dry etching* which may by physical or combined physical and chemical reactions. Physical etching is mostly anisotropic in nature, thus can prevent the undercut (which occurs in the case of wet etching), however here the etching rate is much lower than that of the wet etching process. The difference in isotropic and anisotropic is explained in Figure 2.7. One type of dry etching is Ion Beam Etching (IBE). In this case, ion beam is thrown

upon the surface to ablate the atoms from the surface, thus etching the surface. Normally, this etching is not material specific, it is rather physical in nature. Before etching, the structure has to be protected by photoresist otherwise the etched material can be redeposited on the structure, which is the main issue with this type of etching. The critical aspects here are the energy of ion beams and the angle at which the ion beams are thrown. The angle at which ion beams attack can be played with, to reduce the re-deposition. IBE works well for structures which have low aspect ratio such as thin films. For larger aspect ratio, it is difficult to find good angle and energy to avoid re-deposition. Therefore, it is not recommended for Cu pillars.

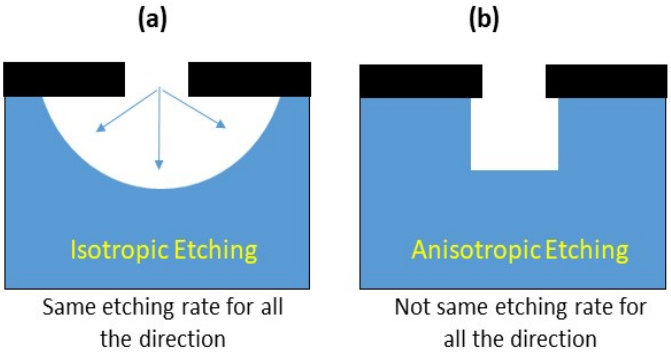


Figure 2.7: Schematic drawing showing the difference between (a) isotropic etching and (b) anisotropic etching

Another dry etching method is Reactive Ion Etching (RIE) which combine chemical and physical etching. A plasma is produced in a low vacuum chamber which physically etches the metal by sputtering but the ions of the plasma also react chemically with the surface (to be etched). Here etchant is in gaseous form that is activated by plasma which facilitates the reaction of the etchant with the material (to be etched) at room temperature. This reaction produces volatile by-products which are easily removed after the reaction. Plasma provides the necessary energy for etching, if done without plasma, then very high temperature would be needed. The rate of etching as well as its anisotropy may be controlled by several parameters such as the power used to generate plasma and the nature and concentration of gas. RIE can be done for various metals used in microelectronic industry such as Ti (see below), TiN, Al, AlCu, SiO_2, Si, SiN, some polymers etc. However, Cu, and Ni are not easily etched using RIE, as there is no common / commercial gaseous etchant for these metals.

For the metallic pad, IBE is a good option, as the aspect ratio is low, and the structure can be protected by photoresist. Therefore, this method is successfully used to fabricate the pad on the bottom chip (die) without any undercut or pad size diminution.

The Cu seed etching for the Cu pillars cannot be etched by IBE (due to risk of re-deposition) or RIE (due to unavailability of commercial echant gas) so it has to be chemically etched (wet process). However, in order to reduce the undercut some parameters must be changed. Wet chemical etching can be described by 3 basic steps: (i) diffusion of etchant to the site, where material has to be etched, (ii) reaction between the etchant and the material and (iii) diffusion of the by product from the reaction site. Traditionally, for Cu etching, the etching bath is made up of phosphoric acid (H_3PO_4), hydrogen peroxide (H_2O_2) and H_2O. The etching may be done by dipping the wafer in the etching bath or by spray depending on the available etching equipment. Etching rate depends on the density of the material which depends on the materials' deposition

method. The Cu seed layer is deposited by sputtering (denser Cu layer) whereas Cu pillar is deposited by electroplating (less dense Cu layer), thus during the etching with this chemistry, the Cu pillar will be etched 3 times quicker than the Cu seed layer as shown shown in Figure 2.8. Therefore, in the best case scenario, we will have undercut in the order of 300 nm (150 nm from one side) in the Cu pillar on removing 50 nm of Cu seed layer [103]

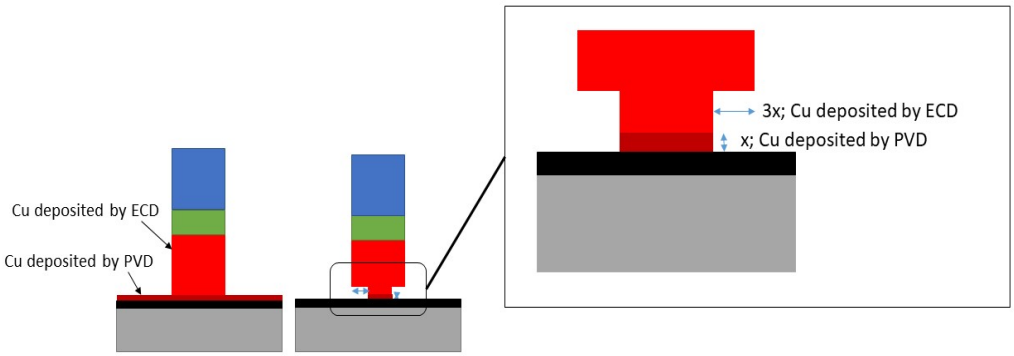


Figure 2.8: Difference in the etching rate of Cu by wet etching in two cases: Cu deposited by electrochemical deposition (ECD) and Cu deposited by physical vapour deposition (PVD)

In the etching bath, hydrogen peroxide is the main etchant and the rate of reaction is determined by the concentration of phosphoric acid (H_3PO_4) in the bath. For larger Cu pillars, 1% of H_3PO_4 in the etching solution is used. With this concentration, the rate of etching is 10 nm/sec, which is too fast to remove 50 nm of Cu seed layer (in case of Cu pillars at 10 µm pitch), thus cannot be controlled effectively. Secondly due to the large density of Cu pillars, the diffusion of by-products from the reaction site is also difficult, which makes the generation of new species (responsible for etching) difficult, which substantially increases the etching time, thus creating a larger undercut.

To solve the first problem, we reduced the concentration of H_3PO_4 below 1%. This has effectively reduced the rate of etching. The second problem is solved by modifying the way of etching, i.e. instead of dipping the wafer in the bath, we spray the solution on to the wafer. This way, removal of by-product is easier and the time of effective etching reduces successfully. With these two modifications, after Cu seed etching we achieved on average 300 nm undercut. A SEM micrograph of the Cu pillar after the etching is shown in Figure 2.9. Red points in the figure show the Cu undercut.

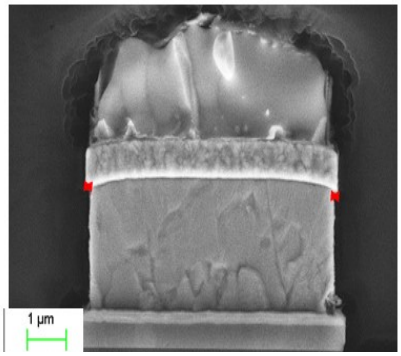


Figure 2.9: SEM image of Cu bump after seed etching, red points show the Cu undercut

To etch the Ti seed (in case of Cu pillar), RIE etching is done using an equipment from Nextral. The etching is done with SF_6 plasma. Figure 2.10 shows the field of copper pillar before and after complete seed etching.

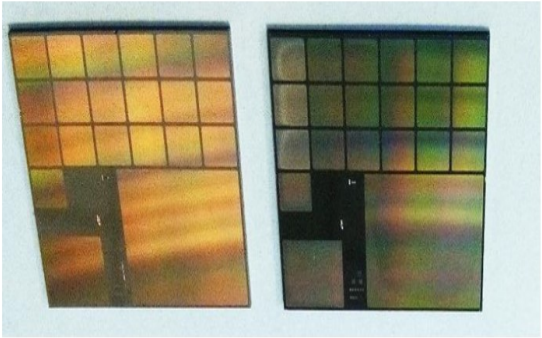


Figure 2.10: Optical microscopy image of the field of Cu pillar (a) before etching (b) after seed etching

2.1.3 Description of test vehicles for 10 µm pitch assembly and for interfacial reaction study

In this section, the design of two types of test vehicles will be presented:

1. Test vehicles used for the 10 µm pitch assembly (with Cu pillars 5 µm in diameter) which are in direct relation with the industrial fabrication of interconnects at low pitch.

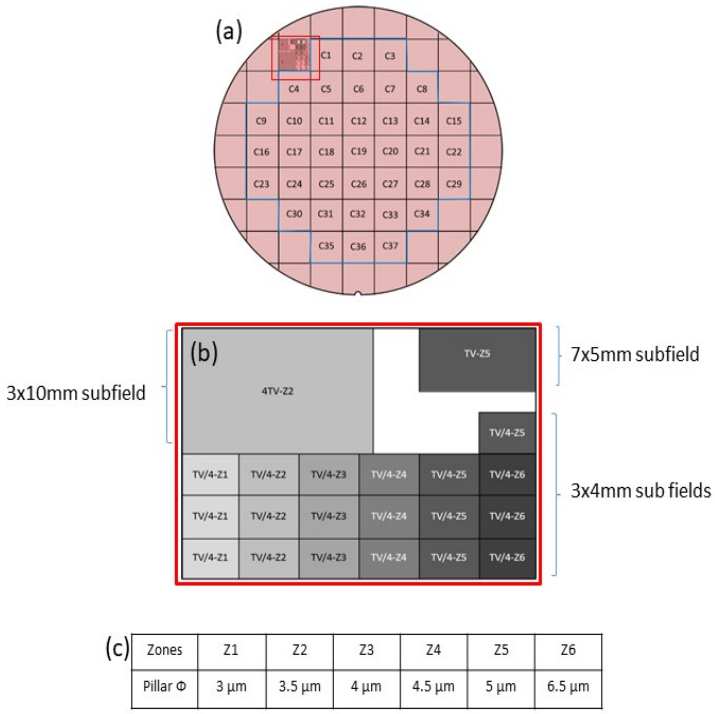
2. Specific test vehicles with pillars 150 µm in diameter, in order to study the interfacial reactions between Ni and liquid or solid solder from both experimental and theoretical point of view.

(a) Test vehicle for 10 µm pitch assembly study

As it is already presented in Section 2.1 and Figure 2.1, the 10 µm pitch assembly is investigated at chip to chip level, where top and bottom chip are fabricated on silicon. Here the design of test vehicles for both parts of interconnects (i) the top chip with Cu pillar and solder alloy (pillar side) and (ii) the bottom chip with metallic pads (pad side) will be presented.

Top chip: Cu pillars
Figure 2.11(a) shows schematically the wafer design. In the wafer, 37 identical fields are present which are further divided into sub-fields. An example of such field is given in Figure 2.11(b). This field is further divided into 21 sub-fields containing pixels at the pitch of 10 µm, out of which 19 sub-fields are of 3x4 mm in size with 320x256 pixels (TV/4), 1 sub-field of 7x5 mm with 640x512 pixels (TV) and 1 sub-field of 13x10 mm with 1280x1024 pixels (4TV). Out of the 19 sub-fields, there are 6 different diameters Cu pillar from 3 µm to 6.5 µm. Figure 2.11 (b) also describes the distribution of these sub-fields. The different diameters are used to define some limit in the fabrication process. However, for this study, only the 5 µm diameter

Cu pillar in 320x256 format is used. *Each Cu pillar for this study is made up of Cu=3 µm, Ni=1 µm and SnAg=3 µm.*



(c)

Zones	Z1	Z2	Z3	Z4	Z5	Z6
Pillar Φ	3 µm	3.5 µm	4 µm	4.5 µm	5 µm	6.5 µm

Figure 2.11: The test vehicle for Cu pillar wafer (a) schematic representation of wafer (b) one field with the description of sub-field and (c) description of distribution of Cu pillar with different diameter.

Bottom Chip: Metallic pads

The metallic pads are also fabricated over 200 mm Si wafer by sputtering. The metallic pads are uniform in size, the diameter is 6.5 µm at the pitch of 10 µm. However, the diameter for Au and Ni layer (which will be in contact with solder alloy at the time of bonding) is 5 µm. The wafer contains several identical fields of 19x24mm. Figure 2.12 shows the schematic of one such field. It contains 7 sub fields with a test pattern. Out of 7 test fields, 5 are in format of TV/4, 1 in TV and the last one is in 4TV format. *Each metallic pad is made up of Ti=40 nm, Ni as a barrier layer with 750 nm and Au of 100 nm thickness*. Au is deposited to prevent the oxidation of Ni.

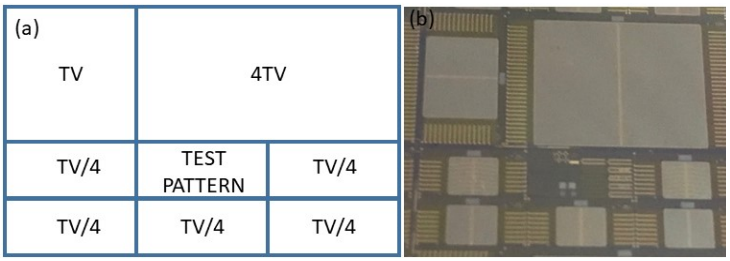


Figure 2.12: The test vehicle for metallic pad wafer (a) schematic diagram representation of a single field in wafer with bottom chips, (b) optical image of one field

(b) Test vehicles for interfacial reaction study

To study interfacial reactions, test vehicles are also fabricated on 200 mm Si wafer. A test vehicle is a field of 3x4mm in size on 200 mm wafer with 12x8 Cu pillars fabricated on it. Each pillar is of 150 µm in diameter containing Cu, Ni and Sn-Ag. The larger diameter is used for this study, as it makes easier to observe and analyze the reaction layer formed after the reactions. As discussed in Chapter 1, solid state and liquid state interactions of Sn are studied with Ni. For solid Sn-Ag interaction with Ni, the pillar is made up of Cu=3 µm, Ni= 1 µm and Sn-Ag=3 µm, whereas for liquid Sn interaction, pillars contains Cu=20 µm, Ni=5 µm and Sn-Ag=10-25 µm. The SEM micrographs of as fabricated samples are shown in Figure 2.13. The test vehicles for solid state interactions are representative to the pillars used for 10 µm pitch assembly in terms of thickness. However, for liquid Sn-Ag/Ni interactions, thicker Ni and Sn-Ag are used as the interactions are faster in this case as described in Chapter 1. A detailed description and characterization of these samples will be given in Chapter 3.

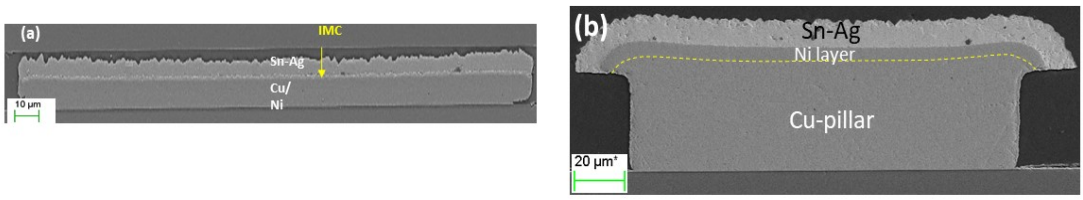


Figure 2.13: SEM micrographs for Cu pillars 150 µm in diameter fabricated to study the interfacial reactions between Ni and (a) solid Sn-2wt%Ag alloy, (b) liquid Sn-2%wtAg alloy

2.1.4 Description of electrical test vehicle

The electrical test vehicle is designed to test the electrical connectivity between the top and bottom dies. The chip metallization is done by Al-Si for the top chip and Al-Cu for the bottom chip. While Cu pillars are fabricated directly over the electrical line, a Cu damascene process is done to connect metallic pad with the electrical line on the bottom die.

The connectivity between the top and bottom chip is evaluated by measuring the resistance of several interconnects connected serially using a design called a Daisy chain and the contact resistance of a single interconnect is generally measured using a Kelvin chain which involves Kelvin sensing. Both information are necessary to qualify the interconnects. The Daisy chain measurement, as it may involve a large number of connections, provides the insight about the efficiency i.e. yield of the assembly process, while Kelvin chain results can help in qualifying the interconnects for a specific application. The schematics of these electrical measurements are shown in Figure 2.14.

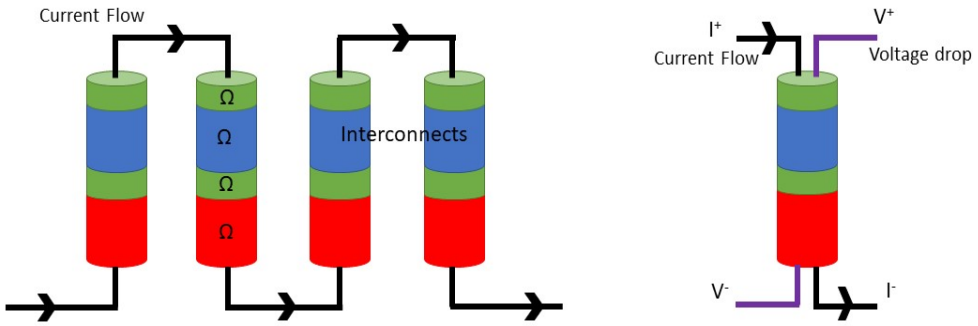


Figure 2.14: Schematic representation for electrical measurement (a) Daisy chain and (b) Kelvin chain

As we encountered some issues with the Kelvin measurement designed on the wafer, only Daisy chains are used to qualify the assembly process in the thesis. However as we will see below, it is still possible to qualify the resistance of a single interconnect with this method. Figure 2.15 shows the schematic of the electrical test vehicle with a Daisy chain. In the same figure the SEM image for the Cu pillars with a Daisy chain is also shown.

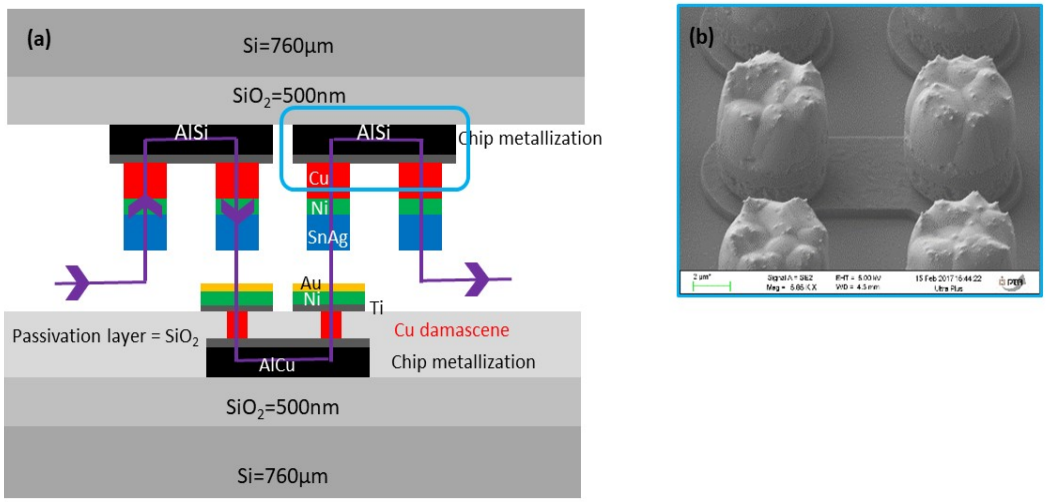


Figure 2.15: Schematic representation for daisy chain in the electrical test vehicle (b) SEM image for a Daisy chain in top chip: Cu pillar

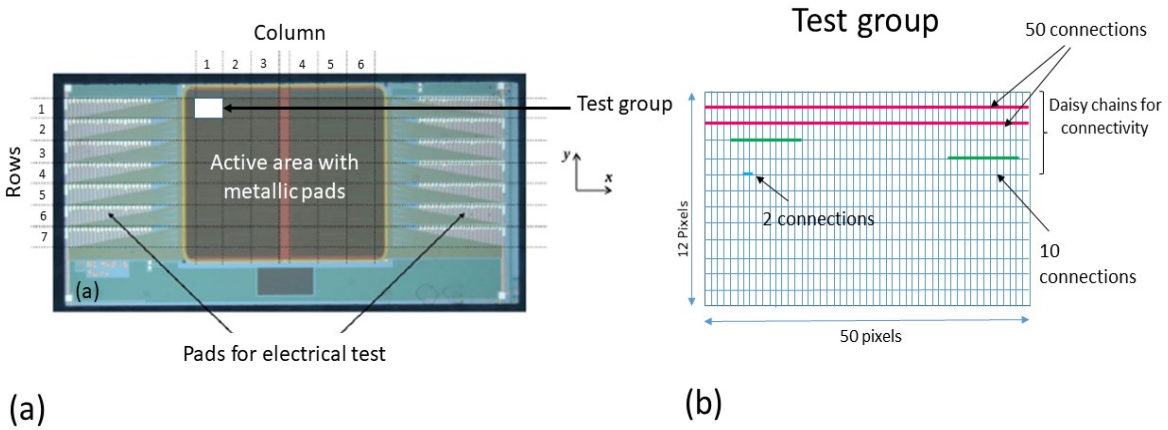
The resistance in the Daisy chain is measured by 2 points probing. In the electrical test vehicle, the chip is divided into 42 identical test groups as shown in Figure 2.16 (a) and each group have 7 Daisy chains. Out of 7 Daisy chains, 5 measure the connectivity while 2 check for the short circuit between adjacent rows. 5 Daisy chains measures the resistance of different number of interconnects which are schematically shown in Figure 2.16 (b). The length of electrical line remains same in all the cases.

With these Daisy chains, we can also calculate the resistance of a single interconnect (R_k), as R_{lines} is the same. It can be calculated using Eq. 2.1.

$$R_{\text{total}} = R_{\text{k}}N + R_{\text{lines}} \tag{2.1}$$

Here, R_{total} is the resistance of the Daisy chain, N is the number of connections and R_{lines} is the resistance of the electrical line and resistance from probing (in case of 2 point measurement).

The value of R_k is determined by calculating the slope of the graph between different number of connections (N) and their resistance (R_{total}). In the test vehicle, we measure the resistance of 50, 10 and 2 connections. By this way the resistance of a single interconnect is determined without using Kelvin test structures.



(a) (b)

Figure 2.16: (a) Electrical test vehicle and a test group (b) schematic representation for conception in the test vehicle

2.2 Assembly Procedure

The typical process for flip chip bonding contains 3 steps, described here below: (i) reflow, (ii) bonding or assembly and (iii) application of underfilling (except in the cases where pre-underfilling is applied). A schematic presentation of the process flow is given in Figure 2.17.

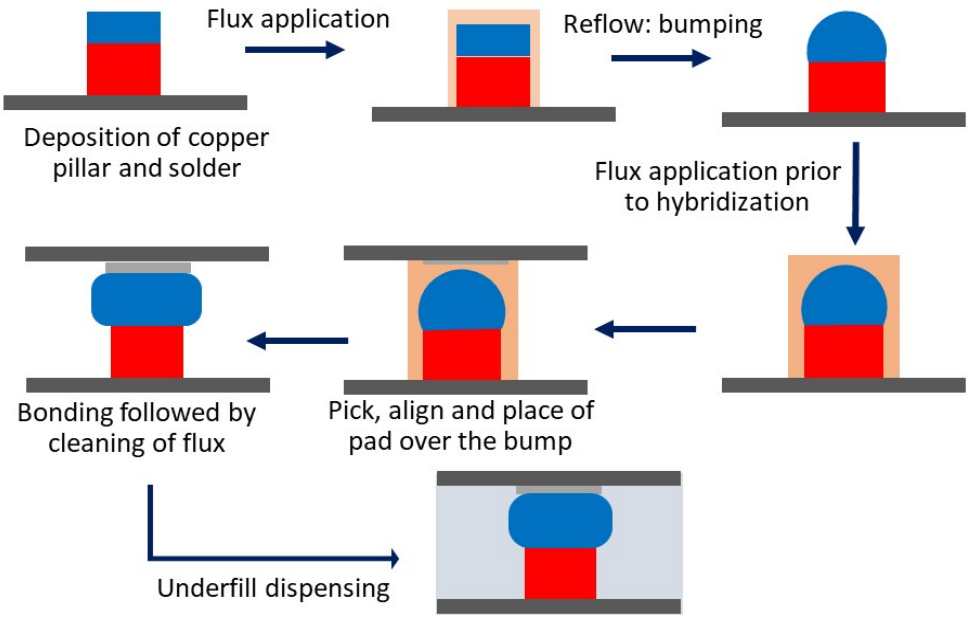


Figure 2.17: Schematic diagram showing the steps of flip chip bonding process (hybridization)

2.2.1 Reflow process

After the seed etching, the wafer goes into the reflow oven. It is the first step of the flip chip bonding. Reflow is a process, where solder alloy is heated above its melting point to form a bump as shown in Figure 2.18. This step is important due to two reasons. Firstly, reflow uniforms the height of Cu pillar. After electrochemical deposition, solder height is not uniform due to the roughness of the deposited Sn-Ag alloy, even though the volume of the solder alloy in each pillar may be uniform. This non-uniformity is around 1 µm throughout the wafer. By performing reflow, the uniformity of the height increases as Sn-Ag alloy melts and forms a bump (spherical cap form) which reduces the roughness of the solder and makes the bonding process easier. Secondly, reflow is necessary for auto alignment of Cu pillars with the metallic pads during the process of bonding. Thus it is a popular practice among the packaging industry prior to bonding. A typical reflow profile is given Figure 2.18 (b)

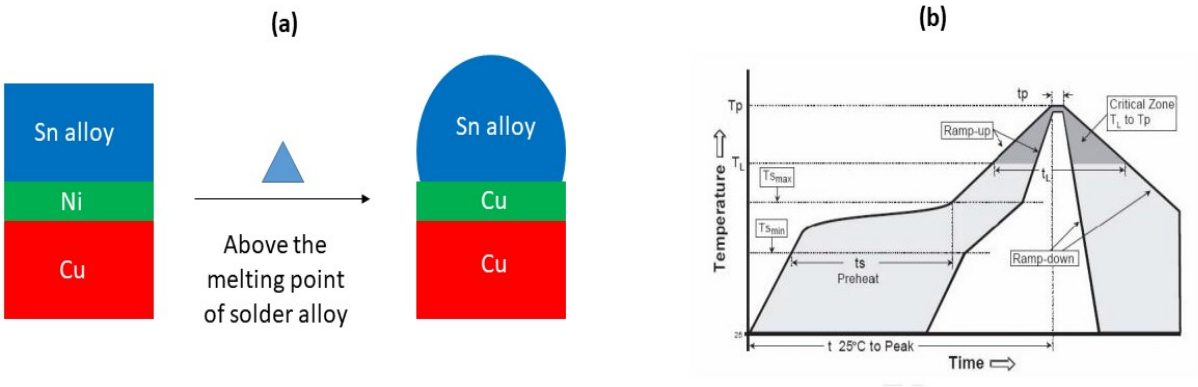


Figure 2.18: (a) Schematic representation of reflow. (b) Schematic representation of a temperature-time reflow profile [104]

In this study, the reflow process is performed in an oven from SST, Model 5100, shown in Figure 2.19. It is a programmable vacuum and pressure oven, where temperature, time, temperature ramp, environment can be set and programmed. For reflow, liquid or gaseous flux can be used to remove Sn oxide Sn_xO_y as mentioned in chapter 1. In this oven, there is an option for using gaseous flux during reflow, such as formic acid and forming gas. In this study formic acid (HCOOH) is used as a flux for reflow studies.

Figure 2.19: SST oven used for reflow

In theory, formic acid can reduce any metallic oxide (M_xO_y) and the reduction is achieved in a two-step process described as follows:

$$M_xO_y + 2\,yHCOOH \longrightarrow M_x[HCOO]_{2y} + yH_2O$$

$$M_x[HCOO]_{2y} \longrightarrow xM + 2\,yCO_2 + yH_2$$

For Sn_xO_y the first step of reduction occurs below 200°C and the intermediate compound ($Sn_x[HCOO]_{2y}$) decomposes at around 220°C, into Sn and gaseous species. That is, at the melting temperature Sn surface is already free of its native oxide thus ready to be reflowed.

In the SST oven, formic acid gas is introduced into the oven chamber with the help of a bubbler. The bubbler consists of a chamber maintained at 20°C in which formic acid is stored. When nitrogen gas is passed through this bubbler, formic acid vapours are carried away by the in-flowing N_2 gas. Thus, the environment of the oven chamber becomes a reducing environment (N_2 + HCOOH gas mixture). The concentration of formic acid in the flowing N_2 gas increases with the bubbler temperature and the flow rate of N_2 gas. At a given bubbler temperature and N_2 flow rate, a reliable quantity of formic acid can be introduced in the oven chamber. The specification of the reflow oven is given in Table 2.1.

Table 2.1: Specification of SST oven

Operating temperature range	Maximum vacuum	Maximum pressure	Heating ramp	Cooling ramp
100-500°C	<0.67mbar (50mtorr)	3.7 bar (40psig)	1°C/sec	0.5°C/sec

For reflow, Si wafers containing Cu pillars are heated at 20-30°C above the melting point of the solder alloy which depends on the composition of alloy. In this thesis, the Sn-2wt%Ag solder alloy is used which has a melting point at 221°C, thus the reflow temperature becomes 250°C. The temperature in the oven is measured with 3 thermocouples with the accuracy of ±5°C. On heating, the solder alloy melts and forms a spherical shape as it is shown in Figure 2.20 for a Cu pillar of 5 µm in diameter. The choice of temperature-time profile process is very complex. An example of most common reflow profile is given in Figure 2.18 (b). The behavior of the interfacial system during the reflow process is studied by using different temperature-time profiles and the obtained results are discussed in Chapter 4.

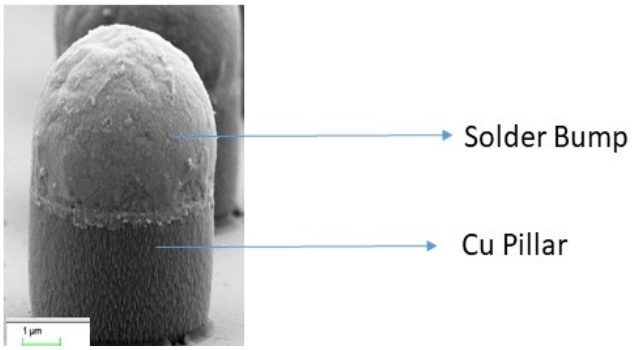


Figure 2.20: SEM image of solder bump of 5µm after reflow

2.2.2 Assembly (Bonding) process

Bonding is the next step after the reflow process. As it was presented in the first chapter, bonding may be achieved using different methods such as cold insertion, thermocompression and mass reflow (i.e. bonding with just heating without applying pressure). In this study we will focus on the mass reflow for bonding. In this step, the solder bumps are bonded with the metallic pads. During the bonding, the solder alloy (on the pillar side) melts again and interacts with the metallization (M) on the other side (pad side), see Figure 2.17. During this interaction, intermetallics are formed between the liquid solder/ metal M interface. The interfacial reactions and their kinetics are discussed in detail in the next chapter. One of the

critical task in this step is the removal of the native oxide layer of solder alloy, if not removed, it prevents the solder to interact with the metal and to make a bond. For removing the native oxides, flux are used, typically liquid flux is used. However as described in Chapter 1, liquid flux needs to be dispensed uniformly before bonding and then cleaned after the assembly. Due to the high density of Cu pillars and the small pitch in the test vehicle used in this study, there may be some issues in efficiently dispensing liquid flux and cleaning it afterwards. Therefore, gaseous flux is investigated which has advantages over liquid flux. Firstly, since it is gaseous in state, it is easier to dispense it throughout the chip on all the Cu pillars, secondly the by-product made during the reducing reaction is also gaseous in state, therefore it does not require any post cleaning process.

For bonding, FC300 bonding machine is used (Figure 2.21), which is manufactured by SET. This is a flip chip bonder, which can perform both mass reflow and thermo-compression. The bonding can be done either chip to chip or chip to wafer. The bonding can be done in different environment, such as ambient, inert or reducing atmosphere with different processing gas, such as formic acid just like in the SST oven. However, inert and reducing atmosphere can only be used for chip to chip. The specifications of the bonding machine are given in Table 2.2.

Figure 2.21: FC300 bonding machine used for bonding

The bonding machine has two components; a chuck on which the bottom chip is placed and the bonder head, where there is an arm which holds the upper chip and can apply force during the bonding (Figure 2.22). Both top and bottom chips are held by vacuum on the head and chuck respectively. The alignment of top to bottom chip is done with the help of an optical microscope. To align, the chuck can be moved and/or rotated with respect to the upper chip. The equipment has also an option to check and correct parallelism. It is done by measuring the distance between top and bottom at all the four edges after alignment as shown in schematic diagram in Figure 2.23. If some difference is observed, then the top chip can be moved such a way that the top become parallel with the bottom chip.

Table 2.2: Specification of FC300 bonding machine

Precision in alignment	Placement	0.3 µm
	Post bond	0.5 µm
Component size	Top chip	0.2-100 mm
	Bottom chip	0.5-200 mm
Max temperature		450°C
Maximum heating ramp		5°C/sec
Maximum cooling ramp		1.6 °C/sec

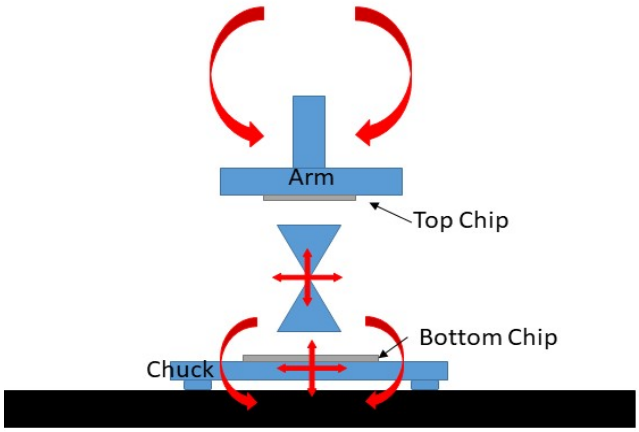


Figure 2.22: Schematic representation of alignment and positioning of top and bottom chip, with degree of movement of chuck and arm

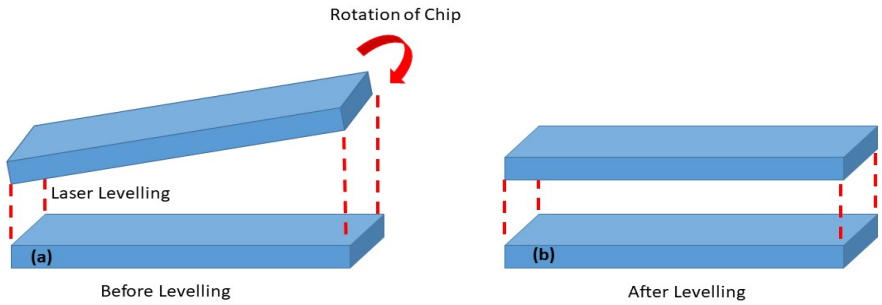


Figure 2.23: Schematic representation for leveling done on FC300, (a) the parallelism before levelling and (b) parallelism after levelling

The bonding can be done in inert atmosphere or formic acid atmosphere. For the bonding, the top chip is placed over the bottom chip and a chamber is created between the chuck and the bonder head as shown in Figure 2.24. The bonder head is designed to act as a cap for the chamber. This chamber is necessary as bonding is only effective if the space is confined and no oxygen is allowed to enter. Usually this kind of confined space is obtained in a well-sealed chamber like in SST oven, however in the case of this bonder, it is not possible. Thus SET designed a semi-open confined chamber. Here high pressure N_2 flow is applied at the

periphery of the chamber, which creates a curtain around the chamber that prevents the oxygen from entering into the chamber, thus a semi-open confined chamber is obtained. Within this chamber, N_2 can be injected to create inert atmosphere or formic acid can be injected to create a reducing environment for bonding. Due to the limitation of size of this chamber, only chip-to-chip bonding can be performed, under inert or reducing environment.

Here formic acid vapors are used as in the reflow oven mentioned before (for de-oxidation process), however in this bonder, N_2 gas does not pass through formic acid but rather on the top of the formic acid chamber. The formic acid chamber is set at slightly higher temperature which evaporates the formic acid (evaporator) and this generated vapour gets carried away in N_2 gas. This mixture of gas (N_2 + HCOOH) introduces the formic acid into the semi-open confined chamber to facilitate the bonding process. Here the concentration of formic acid into the chamber is also controlled with the temperature of the evaporator, the flow rate of N_2 and the volume of formic acid present in the evaporator. Usually, the chamber temperature is set at 25°C and when the evaporator is full, the concentration of formic acid into the semi-open confined chamber is between 12-17%.

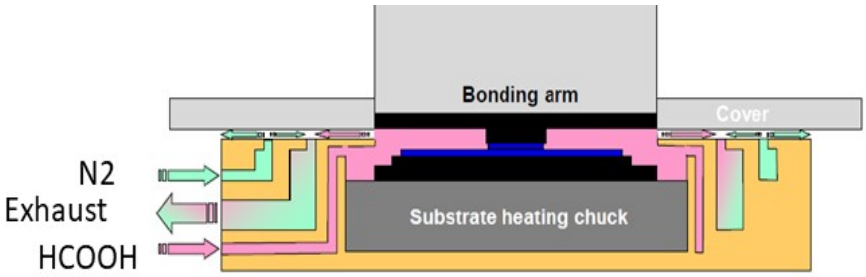


Figure 2.24: Schematic diagram of semi open confinement chamber : FC300

In this study, since pre-applied underfilling is not used, therefore only mass reflow is used for bonding. For the bonding, after alignment of top and bottom, parallelism must be checked and corrected all the time. Only after this step, tacking process can be done where the top die is pressed against the bottom chip with some force at room temperature. This ensures the physical contact between solder alloy and the metallic pads. With our test vehicles, 5 N of tacking force is enough to create a physical contact. After this step, the upper chip is released and the chamber is sealed with N_2 curtain and then, formic acid is introduced into the chamber. For effective reduction of Sn_xO_y, 12% formic acid concentration is required.

For soldering, a temperature-time profile is designed such a way, that during the process, there is sufficient time and temperature for solder oxide to get deoxidized and for solder (situated in the pillar side) to melt and interact with metal on the other side (pad side). However, in this thesis, different profiles are designed in other to obtain different metallurgy of interconnects and this point will be described in detail in Chapter 4. After this step, bonding process is completed.

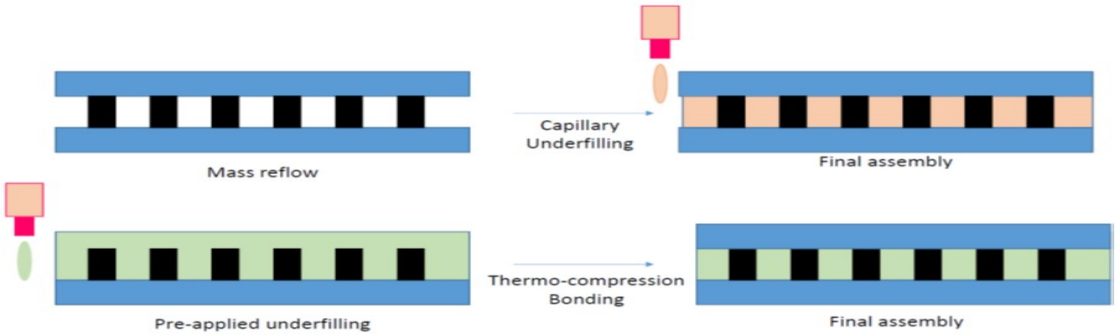


Figure 2.25: Different method for underfilling

The last step for the assembly is capillary underfilling. The underfill can also be applied before the bonding, this type of underfilling is called pre-applied underfilling. With this kind of underfilling, some pressure must be applied in addition to the temperature-time profile. Figure 2.25 shows different ways of underfilling. However, the study of underfilling is out of the scope for this thesis.

2.3 Experimental setup for interfacial study between Ni and Sn

To study the Ni/Sn interactions, the test vehicles are annealed by isothermal holding on a hot plate. This helped in avoiding the other growth factors for IMCs such as heating and cooling ramp. To achieve the isothermal heating condition, the hot plate is first heated to the targeted temperature and then the samples are kept on the hot plate. Similarly, after isothermal holdings, the samples are quenched to the room temperature by putting them on the cold surface. To avoid any temperature fluctuation due to the environment, an aluminum cap is kept on them. The accuracy of the temperature is verified by a thermocouple. The difference between the set temperature and actual temperature was $\pm 2°C$ on the hot plate and $\pm 5°C$ on the dummy sample which is the same size as the test vehicle.

2.4 Sample preparation: Cross-section

To analyze the interconnects and interfacial reactions between Sn and Ni (*object of interest*), the cross-section on test vehicles must be performed. This process is necessary to analyze the object of interest with electron microscopy. To perform the cross-section, first the sample is diced into half, which brings the object of interest nearer to the surface, then the surface is polished to make it smooth and objects obvious to observe. Polishing can be done either mechanically or by ion beams.

Mechanical polishing is done with Tegram 25, which is an automatic mechanical polishing equipment. For Si and SiO_2 substrates, the process contains 7 steps. First two steps are for mechanical grinding, which prepares the sample for mechanical polishing. It is done on SiC

paper of various grid sizes. Then polishing is done on 9-1 µm grain sized diamond surfaces with diamond solution of corresponding sizes. In the last step, Si colloidal solution is used for chemical polishing. The grain size for this step is 40 nm, thus it is the finest polishing achieve by the described method. This last step helps in revealing the IMC layer (object of interest) better. This method is used to study the interfacial reactions between Ni and Sn.

However, mechanical polishing *cannot* be used for all the samples due to the object of interest size. For observing interconnects of 5 µm diameter and 7 µm in height, mechanical polishing does not seem to be a good option, more finer finish is needed, therefore, ion beam polishing is used. In Figure 2.26, SEM images of sample cross-sections prepared by mechanical polishing and ion beam polishing are compared. The cross-section after mechanical polishing does not seem as smooth (finished) as the cross-section done with ion beam polishing.

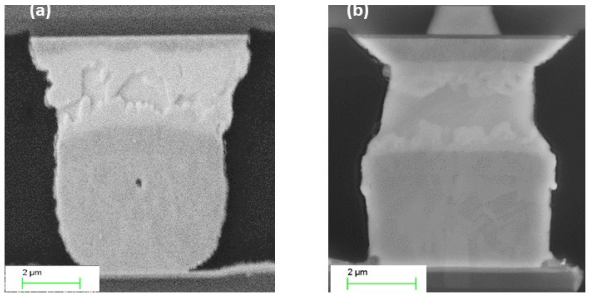


Figure 2.26: SEM images of cross-section prepared (a) with mechanical polishing (b) with ion beam polishing

Normally for better quality of cross-section, after mechanical polishing, Focused Ion Beam (FIB) polishing is done for finer finishing, Here, gallium ions are used to hit the mechanically polished surface to sputter out material which can be tuned by adjusting the energy of ions. The material leaves the surface in the form of secondary ions or electrons which are collected to make an image. Due to high energy of ion beams used to sputter the surface of sample, the surface can heat up and the temperature can go up to 150°C. This heat can alter the metallurgy and thickness of intermetallics.

Since we are interested in studying the growth kinetics of intermetallics, we had to look for other polishing options which do not generate heat. In this study, a triple ion beam milling system, TIC from LEICA has been used (shown in Figure 2.27). This tool comes with a cooling system along with ion beam polishing, which uses liquid nitrogen to cool the chamber and the temperature can be maintained constant. For this, no prior mechanical polishing is needed. The diced sample is mounted on to the sample holder, then the sample is bombarded with three Ar ion beams of 10 keV energy which etches the sample with three different angles under vacuum. The temperature of the chamber is fixed at -30°C. The equipment for ion beam etching is shown in Figure 2.27.

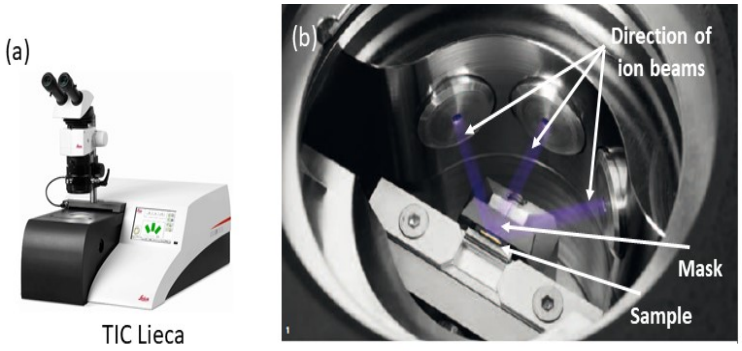


Figure 2.27: (a) Equipment for ion beam etching, (b) Diagram showing triple ion beam and other components of TIC

Even after ion beam polishing, sometimes different metallic layer cannot be properly distinguished in the cross-section, for e.g. Ni and Cu as shown in Figure 2.26. Also, the cross-section does not give any interesting idea regarding the grain structure of each material. Grain structure and grain size gives a valuable insight on the interfacial reaction between Ni and Sn which are studied in Chapter 3.

In TIC, it is possible to achieve the *contrast* in between different layers by exposing the grains in each material. The contrast is done on the sample which has already been polished with TIC, however, the surface is re-etched in different direction. In case of cross-section explained before, the ion beams are parallel to the solder bumps or interconnects, however in this case (of making contrast), the ions are perpendicular to the structure as shown in Figure 2.28 (c). In this direction, the surface gets etched in such a way that the grains are exposed thus making contrast between different metallic layers. The energy to be used depends on the material properties. If the material is hard, like intermetallics, then higher energy is used to expose the grains, than in the case of Cu and Sn. However, the energy of the beam used in this treatment should be less than 5 kV. For Ni/Sn intermetallics, ion beams with 4 kV energy is needed to expose the granular structure and the duration of treatment is 3 mins under the vacuum. The cooling is not possible for this treatment. Figure 2.28 shows the difference in the SEM image prepared with and without contrast. In Figure 2.28 (b) which shows cross-section after the contrast, one can see the grains in each layer unlike in Figure 2.28 (a), thus layers can be better distinguished.

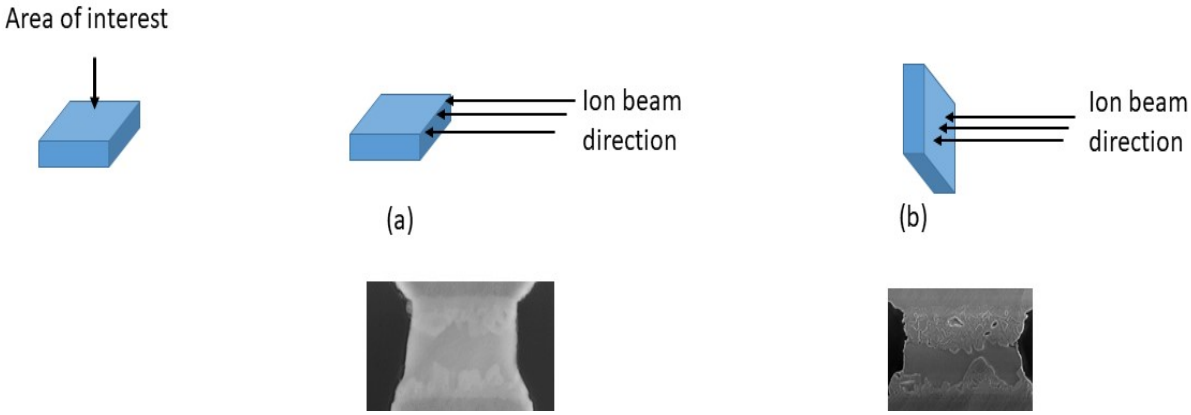


Figure 2.28: Schematic diagram showing difference in orientation of sample surface for ion beam etching for (a) cross-section, (b) contrast to expose grain

After polishing, the pillars on the test vehicle were observed by Scanning Electron Microscopy. To calculate the thickness of intermetallics formed after interfacial reactions, the image is then analyzed by IMAGEJ software explained in appendix B. The area of the intermetallic is calculated and it is divided by the length of cross-section to give the average thickness of IMC in the sample.

2.5 DESCRIPTION OF CHARACTERIZATION TECHNIQUES

The heart of the thesis lies in the metallurgy characterization. Throughout the thesis, various metallurgical characterization techniques are used and they will be presented in this section.

2.5.1 DIFFERENTIAL SCANNING CALORIMETRY (DSC)

DSC is a thermo-analytical technique used to evaluate the temperature and the enthalpy of phase transitions such as melting or solidification. This technique measures the heat required to increase the temperature of the specimen with respect to a reference sample. The reference sample should not exhibit any phase transformation in the temperature range used for the study. Heat is provided (or received) during the run to increase (or decrease) the temperature in such a way that the temperature remains equal for both parts (the specimen and the reference sample). This heat flow is measured and plotted against temperature and/or time. When the specimen undergoes phase transformation, then a peak of the heat flow is observed. Thus, the analysis of the heat flow-temperature curve allows to evaluate the temperature at which the phase transition occurs as well as the enthalpy of phase transition.

In this study, a 2920 TA Instrument DSC equipment is used to determine the melting and solidification behaviour of Sn-Ag alloy. It allows in particular to determine the undercooling degree of the solder alloy and helps in evaluating qualitatively the content of Ag in the solder alloy, thus qualifies the fabrication process for Cu pillar.

2.5.2 ENERGY DISPERSIVE X-RAY SPECTROSCOPY (EDX)

EDX is an analytical technique used for elemental/chemical analysis. It is both a qualitative and quantitative analysis. EDX from Bruker is used, in Gemini (from Zeiss) SEM. The main principle of this technique is that each element has its unique sets of line on an electromagnetic spectrum due to their unique atomic numbers. In the technique, high energy electron beams/X-rays are projected on the specimen (cross-section), which causes an electron to get excited from its ground state and to emit out of the atom leaving an electron hole behind. Then this hole is filled with electron(s) from higher energy orbit, on doing so some energy is released, which is in form of X-Rays and is specific to a given element. The principle is shown schematically in Figure 2.29. These X-rays are measured and analyzed, which gives the chemical composition of the specimen.

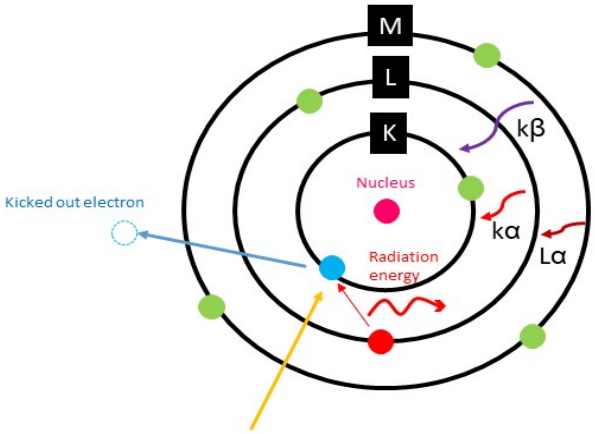


Figure 2.29: Principle of EDX

For this technique, a higher energy of electron beam is needed to emit the electrons. The electron beam energy should normally be at least 3 times higher than the binding energy (kα) of the element, therefore for EDX analysis 20 keV is used in this study (Ni=7 keV). At this energy, the electron penetrates deeper. According to Monte-Carlo simulations, for Ni_3Sn_4 intermetallic (density equal to 8.6 g/cm^3), the depth can go up to 1.5 µm (shown in Figure 2.30). If the layer is thinner than 1.5 µm, then the quantitative analysis may not be accurate.

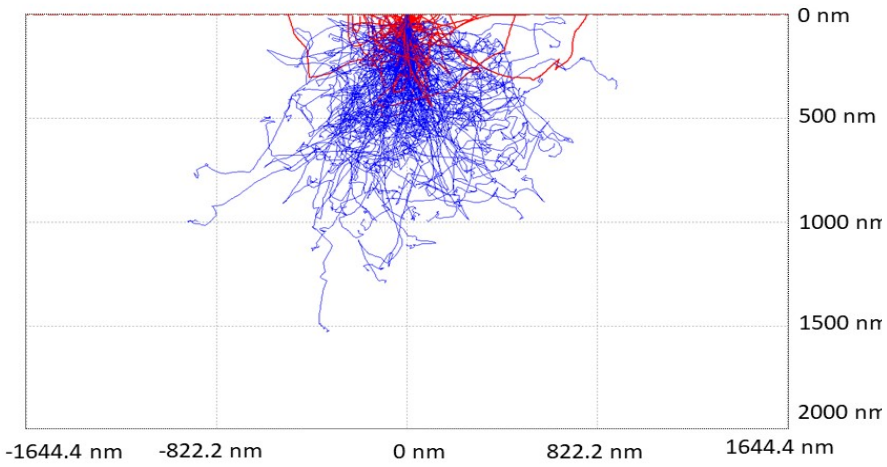


Figure 2.30: Monte-Carlo simulation for e-beam penetration in Ni_3Sn_4 with 20 keV energy

This technique is used to study the interfacial reactions between Ni and Sn (presented in Chapter 3) and to determine chemical composition of intermetallics in interconnects (presented in Chapter 4).

2.5.3 Electron Backscatter Diffraction (EBSD)

EBSD is a technique used to analyse the microstructure of a sample. This technique is also used to characterize the intermetallic metallurgy in Chapter 3. The technique gives crystallographic data with chemical analysis. For this analysis, sample should be thinned and the surface should be very finely polished as roughness due to sample preparation can cause noise in the output. Therefore, it is done by ion beam polishing. EBSD is an attachment to SEM just like EDX. However, for EBSD, the sample has to be tilted by 70°. A schematic diagram for EBSD analysis is shown in figure 2.31.

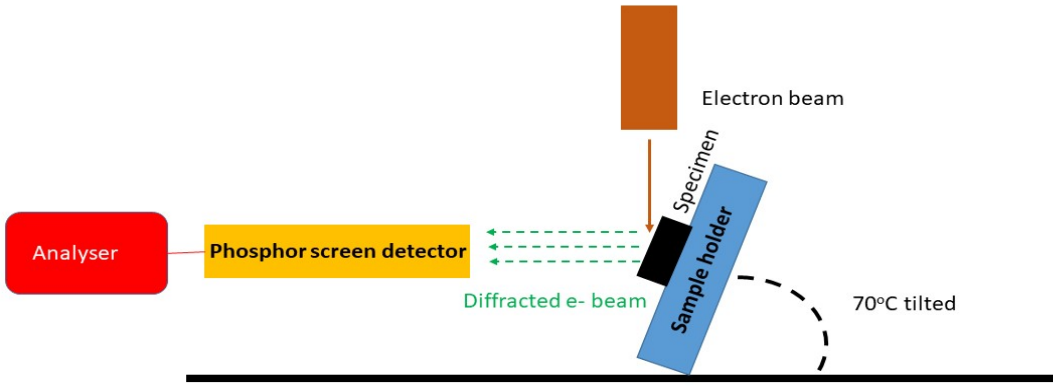


Figure 2.31: Schematic diagram for EBSD

When the electron beam with high energy (>20 keV) is directed towards the titled sample, electrons diffract, and create group of paired large angle cones (Kikuchi lines), which intersect the detector screen (phosphor) and form bands. These bands correspond to diffraction patterns and follow Bragg's law i.e. $n\lambda = 2d\sin\theta$, which is schematically shown in figure 2.32. The band orientation gives the orientation of grains. Therefore these bands are analysed and processed which provides the crystallographic analysis of specimen. This technique can be combined with EDX analysis to give chemical composition too.

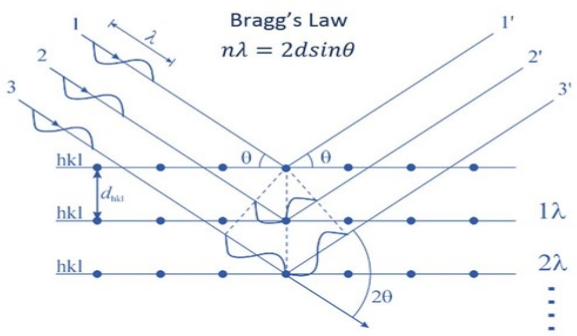


Figure 2.32: Principle of X-Ray diffraction (Bragg's law)

2.5.4 X-RAY TOMOGRAPHY

This technique is used to make a virtual 3D model of the specimen and it is very efficient to look for defects such as voids in the interconnects. It can also provide valuable insight about the metallurgical composition of intermetallics. In the technique, a specimen is cut into small cylinder of 1 mm diameter size by ion beam etching. Then the sample is mounted on a holder and X-rays are projected on to the samples. During the run, sample holder is rotated which creates projections of cross-section at different planes and at the end these cross-sections are combined to make a 3D model of the specimen (same principle as in Computed Tomography (C.T.) scan for medical purposes). This can also be combined with fluorescence spectroscopy which can give some information about the metallurgy of specimen. The schematic of this technique is shown in Figure 2.33.

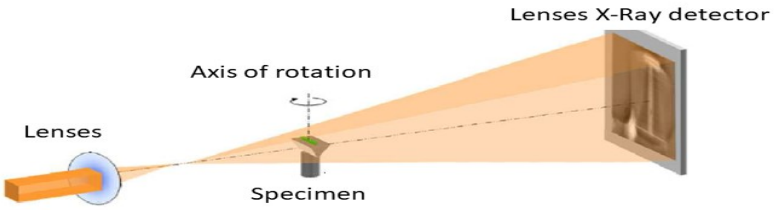


Figure 2.33: Schematic diagram for X-Ray tomography

2.6 QUALIFICATION OF ASSEMBLY PROCEDURE

The assembly process used and the property of formed interconnects are discussed in Chapter 4. To qualify the assembly process, various qualification levels are set. These steps are based on the properties of interconnects, thus the interconnects are characterized along with their metallurgy. Based on these results different assembly processes are compared.

First level of qualification is **Wettability**. For making an interconnect, it is imperative for solder alloy to get in physical contact with metallic pads and during bonding, it must deoxidize and interact with them to make a bond. This is ensured by checking wettability of metallic pads. To evaluate the wettability, after assembly, the bond is broken and the pads are observed to calculate the percentage of solder wetted pads approximately. 100% wettability is needed for the assembly process to be qualified otherwise it is considered as failed process. This step qualifies the tacking force needed to make a physical bond and it also qualifies the flux used for de-oxidation during bonding. In case of warpage (explained in Chapter 1), the tacking force becomes important as the force is needed to make contact between all the pads and solder bumps/pillars. However since both substrates at top and bottom are silicon, and small size (3x4 mm) the warpage is not an issue, thus in this thesis this step is used to qualify the flux for assembly process.

The second qualification step is **Mechanical** resistance. After getting 100% wettability, the mechanical strength of interconnects is measured by shear test. The test is done by DAGE 4000 equipment. The schematic diagram of shear test and its parameters are shown in Figure

2.34.

During the test, a cartridge puts shear force on the held sample with the help of a blade. The sample is stationary, the bottom chip is clamped in the sample holder while the upper chip is sheared during the run. The shear force increases steadily with time until the sample fails. The speed of shear force applied and the height of the blade with respect to sample can be programmed. The failure criteria can also be set (from 20% breakage to 100% breakage). In this study, 100% breakage is a failure criteria. For applying force, 2000 N of cartridge is used, and the force measured by this cartridge is of $\pm 0.25\%$ accuracy. The speed for shear test is 50 µm/sec and shear height is 50 µm.

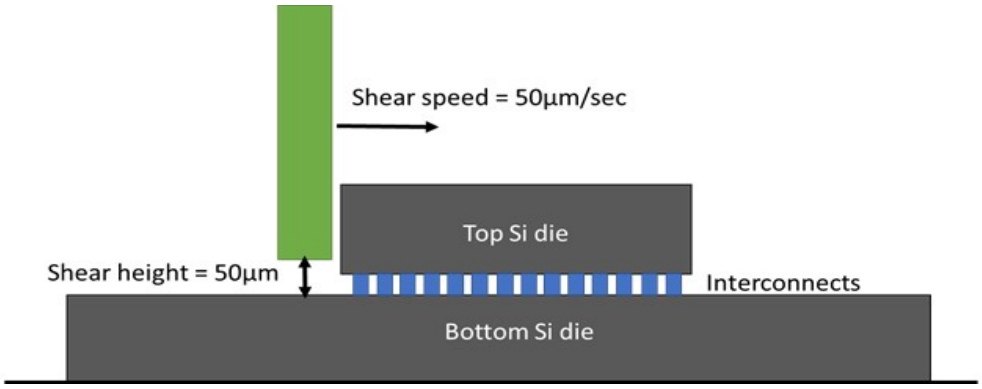


Figure 2.34: Schematic diagram for performing shear test

The rupture force of assembled sample tells about the mechanical resistance of assembly. The shear force depends usually on the metallurgy of the interconnects, however, if the bonding is not proper and 100% bond (in terms of area) is not made between top and bottom, then interconnects will break at a much lower shear force. It was found experimentally that, if the shear force is below 50 N for 320x256 Cu pillar format (i.e. 6×10^{-4} N per interconnect), the bond area is 50% less than the surface area of Cu pillar, thus not a good bond. Thus for assembly process to qualify, the shear force must be more than 50 N. Experimentally, it is found that the temperature - time profile plays a crucial role in making a good soldering bond. In Chapter 4, the interconnects achieved by the qualified processes are characterized with the shear test and are compared with each other.

Third level of qualification is **Electrical** characterization, here interconnect yield and contact resistance are measured and analyzed. In the Section 2.1 (test vehicles) electrical test vehicles are described which are used to qualify the interconnects electrically. For the characterizations, Keithley instrument is used to measure the resistance of interconnects after assembly. In Chapter 4, the results for this characterization are discussed and explained. Note that, in mechanical characterization or wettability, the sensitivity of testing assembly process is up to 90-95% (in terms of connectivity), whereas in this case all the connections can be tested thus the sensitivity can be 100%. Thus this step is the most critical and crucial step as it can assure, if successful, that the assembly has not only mechanical contact but also an electrical contact.

Last step of qualification is **Reliability**, which is testing the properties of the achieved interconnect over a period of time (storage at room temperature or at high temperature). The apt reliability test and qualification criteria are provided by the application for which they are going to be used for. For example, for microdisplay application, thermal cycling or high temperature

storage test are done until the resistance of the interconnect goes up to 50%. However in this thesis, no application is targeted, therefore no particular norms are followed. Here, the evolution of electrical resistance of interconnects due to storage at high temperature is investigated. The tests are performed on hot plates in ambient environment with the temperature accuracy of $\pm 1°C$. These results will help to qualify the *assembly process* and the metallurgy for assembly of Cu pillars at 10 µm pitch.

CONCLUSION

In this chapter, the test vehicles and their fabrication methods are presented. The issues encountered during the fabrication process are also listed with their possible solutions. All the analytical techniques used in the thesis for characterization of metallurgy as well as interconnects are presented.

These test vehicles and techniques enabled us to study from a fundamental point of view the interfacial reactions between Ni and Sn. With the help of different characterization results, the growth kinetics of reactive intermetallic layers is studied with the factors that may affect it. The results are presented and discussed in the next chapter.

In the last chapter, the comparison between interconnects obtained from two qualified processes is made with the help of the characterization techniques presented in this chapter, which helped in qualifying the process for the assembly at 10 µm pitch.

Chapter 3

Interfacial Reactions in Sn/Ni System

Contents

INTRODUCTION

For the finer pitch assembly (< 10 µm) as mentioned in Chapter 1, the intermetallic compounds formed during bonding are crucial and should be limited. The formation and growth of IMCs start from the first assembly process i.e. reflow, where Sn-Ag melts and forms a spherical cap. During this melting, it also reacts with the underneath Ni layer to form some IMCs and later during the assembly, Sn again melts and interacts to form new IMCs (with metallic pads) and to grow the already present IMCs (at Cu pillar side)- see Figure 2.17. The heating and cooling ramp, when the temperature is below the melting point of Sn-Ag alloy, can also have an influence on the growth of IMCs. The heating rate determines the reaction time at solid state from a given temperature to the melting point while the cooling rate has a great influence on the undercooling degree and thus on the contact time between the metastable liquid alloy and Ni from the melting point of the alloy to the nucleation (solidification) temperature.

One of the main challenging issue for 10 µm pitch (and below) assembly is to control the growth kinetics of the reaction layer. In each step, Sn is consumed, making Sn volume lesser for the next step. However, the available solder thickness is limited (to some micrometers) due to limitation in photoresist aspect ratio (as explained in Chapter 2), therefore it is now critical to design each process such a way that the process consumes least Sn, or in other words, forms least IMCs. Secondly, for understanding the bonding process from metallurgical point of view, it is important to have a deeper insight into what is happening during the solid and liquid state Sn-Ag interactions with Ni and principally in initial stages, i.e. between 1-5 min.

However before going deep into this study, the different samples are characterized at their initial stage, just after fabrication before undergoing any thermal treatment so that the initial stage of the Sn/Ni system is known. In addition, for an in depth qualification of the system some Differential Scanning Calorimetry (DSC) analysis are performed, so that the reflow behaviour of the deposited Sn-Ag alloy is determined and understood. These preliminary results are presented in Sections 3.1 and 3.2 below. As this chapter is dedicated to understanding the behavior of the Ni/Sn system, the interfacial reactions in both solid Sn/solid Ni system and liquid Sn/solid Ni system are studied and the results are presented in Sections 3.3 and 3.4.

3.1 INITIAL STAGES OF TEST VEHICLE AFTER DEPOSITION

Three test vehicles were processed in the framework of this study:

1. Test vehicle 1, which corresponds to the test vehicle for 10 µm pitch assembly, consists of *5 µm diameter* of pillars made with *Cu=3 µm, Ni=1 µm and Sn-Ag=3 µm*.

2. Test vehicle 2 consists of *150 µm diameter* of pillars made with *Cu=3 µm, Ni=1 µm and Sn-Ag=3 µm*. This test vehicle is performed in order to study the interfacial reactions between solid Sn-Ag alloy and Ni at temperatures 150-210°C for reaction times up to 4 hrs. A large diameter of bump (much higher than 5 µm) was chosen in order to observe the reactive interface in a large area, thus to calculate the average thickness of the reaction layer with a good accuracy. Preliminary calculations, based on literature studies, show

that the total thicknesses of Ni and Sn consumed by interfacial reaction for 4 hrs at 210°C are lower than 1 and 3 µm respectively. This was the reason why the thicknesses of deposited Ni and Sn-Ag alloy layers for test vehicle 2 was chosen the same as for test vehicle 1.

3. Test vehicle 3 consists of 150 µm diameter pillars with *Cu=25 µm, Ni=5 µm and Sn-Ag=10-25 µm*. This test vehicle is performed in order to study the interfacial reactions between liquid Sn-Ag alloy and Ni at temperatures 250-350°C for reaction times up to 4 hrs. Given the fact that the growth kinetics of Ni-Sn IMCs between liquid Sn and Ni is much higher than that between solid Sn and Ni, the initial thickness of deposited Ni and Sn-Ag layers were chosen much higher than those for test vehicle 2. Table 3.1 gives a description of the tests vehicles.

Table 3.1: Test vehicle description

Test vehicles	Diameter (µm)	Thickness of layers (µm)		
		Cu	Ni	Sn-Ag
1	5	3	1	3
2	150	3	1	3
3	150	25	5	10-25

The fabrication of the test vehicles is done by electrochemical deposition, which is described in Chapter 2. Figure 3.1 shows the initial stage for *test vehicle 1*. The interfaces between Cu, Ni and Sn-Ag alloy are clearly seen. Although the Cu/Ni and Ni/Sn-Ag interfaces seem to be smooth and continuous interfaces, the Sn-Ag upper surface seems to be rough, which is due to the deposition process. Other important thing to notice here is the granular structure of each layer. Sn-Ag layer has relatively larger grains of micrometer size, while Ni layer has smaller nano-metric size grains (average grain size about 60 nm) - see the enlarged image shown in Figure 3.1 (b). Also in this enlarged image, a thin and continuous reaction layer can be observed which is formed uniformly at the Ni/Sn-Ag interface. The average thickness of this layer is about 120 nm. This interfacial layer is characterized and it is found after doing EDX, that the layer is Ni_3Sn_4 IMC phase (43.5 at% Ni and 57.5 at% Sn) as shown in Figure 3.2.

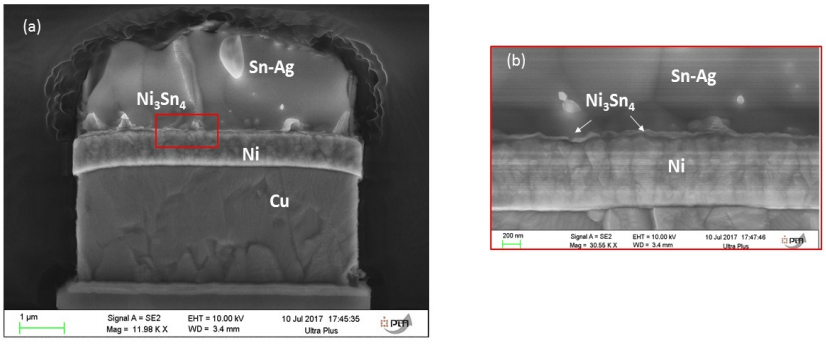


Figure 3.1: SEM micrographs of the initial state of Sn-Ag alloy/Ni interface for *test vehicle 1* after electroplating process, (a) full pillar (b) enlarged view of the interface between Ni and Sn-Ag alloy

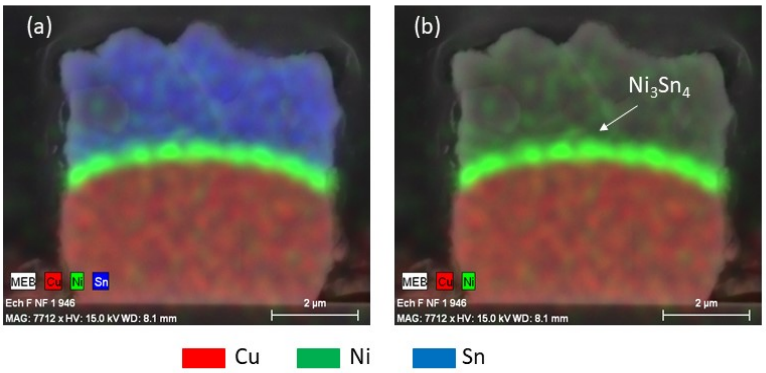


Figure 3.2: EDX analysis of *test vehicle 1* after depostion

Figure 3.3 and Figure 3.4 present SEM micrographs for *test vehicle 2 and test vehicle 3* respectively, where the initial state of the Ni/Sn-Ag alloy interface after electroplating process is shown. In this test vehicle also, a thin and continuous reaction layer is observed which is formed uniformly at the Ni/Sn-Ag interface. The average thickness of this layer for test vehicle 2 is 120 nm like test vehicle 1, however, the average thickness for test vehicle 3 is about 250 nm which is more than that observed for test vehicles 1 and 2.

The thin interfacial layer is present for all the test vehicle. This interfacial layer may be formed during the fabrication process which is described in Chapter 2. The wafer with Cu/Ni/Sn-Ag pillar undergoes some thermal processing step up to 70°C, which combined with room temperature storage may lead to the formation of this thin layer. However, the thickness of interfacial layer for these test vehicles is considerably different (120 nm for test vehicles 1 & 2 and 250 nm for test vehicles 3). This difference may be explained by the fabrication process for which the height of test vehicle 3 (Ni=5 µm, Sn-Ag=10-25 µm.) is very different from the height of test vehicles 1 and 2 (Ni=1 µm, Sn-Ag=3 µm), so is the height of photoresist used. During the fabrication process, after depositing and patterning of the photoresist, the wafer undergoes some heat treatment which may be different depending on the photoresist. In addition, the seed etching process is different, between small bumps and large bumps which also has an impact on the heat treatment, thus different thickness of the initial IMC layer.

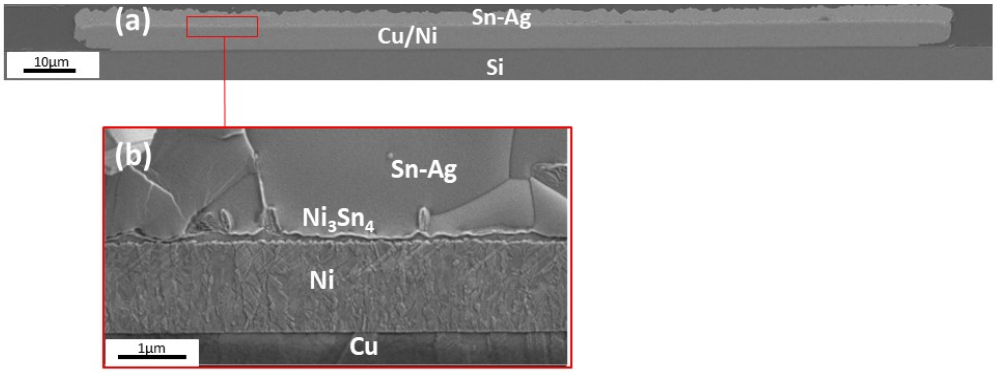


Figure 3.3: SEM micrographs of the initial state of the Sn-Ag alloy/Ni interface for *test vehicle 2* after electroplating process, (a) pillar (b) enlarged view of the interface between Ni and Sn-Ag alloy

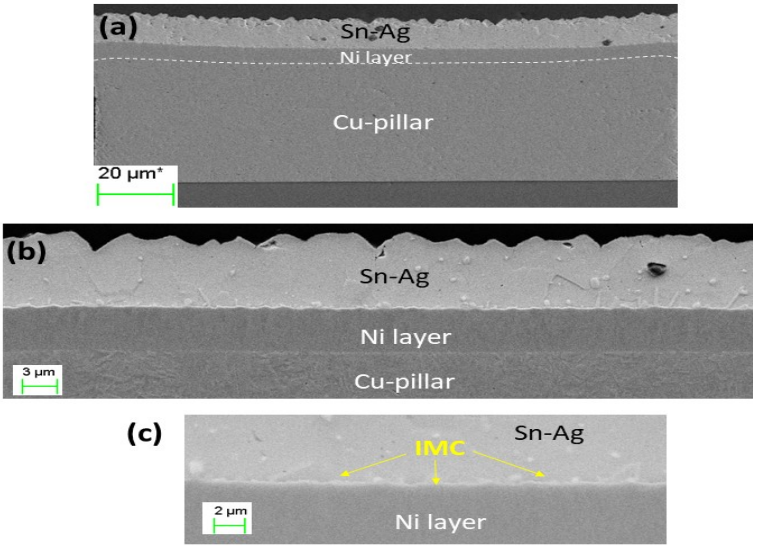


Figure 3.4: SEM micrographs of the initial state of Sn-Ag alloy/Ni interface for *test vehicle 3* after electroplating process, (a) full pillar (b) and (c) enlarged views of the interface between Ni and Sn-Ag alloy

3.2 Melting behaviour and microstructure of 5 µm Sn-Ag bumps

3.2.1 Melting behaviour of Sn-Ag bumps studied by DSC

Before studying the interfacial reactions, the melting and solidification behaviour of the deposited solder was studied by Differential Scanning Calorimetry (DSC). DSC measurements were performed for test vehicles 1 (diameter d_1=5 µm, height of Sn-Ag solder h_1=3 µm) and test vehicle 3 (d_3=150 µm, h_3=10-25 µm). In first approximation, by assuming that the solder alloy is pure Sn, from the molar mass of Sn (M = 118.7 g/mol), its molar melting enthalpy (ΔH_m=7029 J/mol) and its density (ρ = 7.3g/cm^3), we can calculate the volumetric enthalpy of Sn (ΔH_v) by the following equation:

$$\Delta H_v = \frac{\rho}{M}\Delta H_m \tag{3.1}$$

From Eq. 3.1, ΔH_v = 423 J/cm^3

The volume of the bumps in test vehicle 1 and test vehicle 3 are V_1=58.9 µm^3 and V_3=(1.77-4.42)x10^5 µm^3. Thus the expected melting heats of the bump from test vehicle 1 and test vehicle 3 are ΔH_1=2.5x10^{-5} mJ/bump and ΔH_3=(0.079-0.191) mJ/bump respectively.

Given the very low quantity of the solder alloy in a bump the DSC experiment were performed by using samples containing ≈ 8.2x10^4 bumps of 5 µm in diameter and 96 bumps of 150 µm in diameter. The calculated melting enthalpy for Sn containing in these samples (based on above data) are: ΔH^*_1=2.1mJ and ΔH^*_3=(7.2-18) mJ.

Figure 3.5 shows the DSC signals for test vehicle 3 (150 µm diameter Cu pillars) during heating and cooling with heating and cooling rate of 3°C /min. This figure shows two endothermic peaks during heating, the first one at about 222°C and the second one at about 229°C. The second peak is about 10 times bigger than the first peak. The first peak corresponds certainly to the melting of the eutectic Sn 3.5-wt%Ag alloy (221°C) as can be seen from the binary Sn-Ag phase diagram in Figure 3.6 [65]. The second peak corresponds to the melting of primary Sn from the eutectic temperature to the liquidus temperature of this alloy situated at about 229°C. These results clearly indicate that the composition of the deposited solder is far away from the eutectic composition and even far from the targeted composition. Indeed the ratio between both peaks as well as the liquidus temperature of the alloy suggests that the composition is about 0.2-0.3wt%Ag in Sn instead of 2wt%Ag (target composition). The quantity of melting heat measured by DSC is about 10.5 mJ, which is very close to the calculated value, ΔH^*_3 = (7.2-18) mJ. Note that this good agreement between the calculated and measured values of melting heat means that the mass of deposited Sn is close to the target one. However, given the very low quantity of Ag compared to that of Sn, this agreement has almost no relation with the Ag content in the alloy.

During cooling of the sample with 150 µm bumps, numerous small exothermic peaks are observed at the temperature range 200-218°C. These peaks correspond to the solidification of individual bumps at different undercooling degree, i.e. difference in the temperature of melting and solidification. The solidification temperature varies between 200 and 218°C which is

much lower than the eutectic temperature (221°C). The high undercooling degree of Sn and its alloys is a well-known phenomenon [106–109]. This is due to the difficulty of Sn to nucleate and the undercooling of solder bumps of 100-500 µm in diameter can be some tens of degrees. The degree of undercooling is affected by the size of the system also. It is expected that as we reduce the volume of the solder alloy, the degree of undercooling increases.

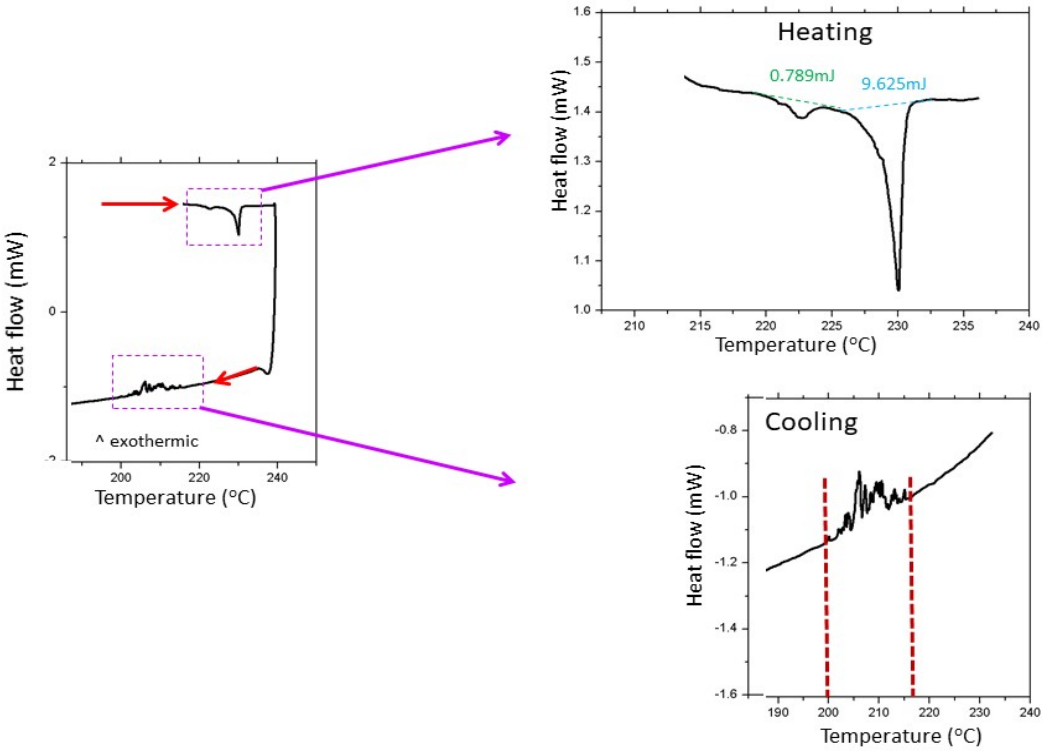


Figure 3.5: DSC curve during heating (3°C /min) and cooling (3°C/min) for 150 µm diameter pillar (*test vehicle 3*)

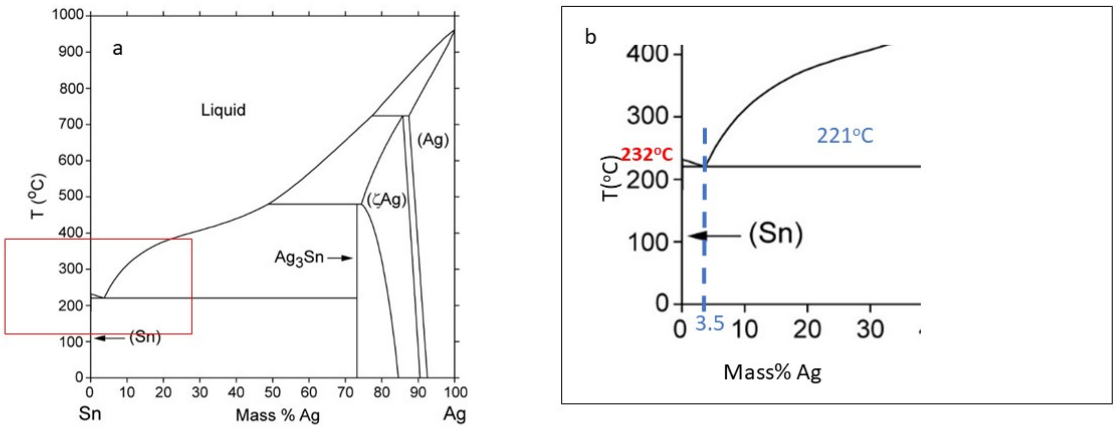


Figure 3.6: Binary phase diagram for Sn-Ag [65]

Figure 3.7 shows the DSC signal during heating of 5 µm diameter bump for a heating rate of

3°C/min. The DSC curve during solidification is not given in this figure because no exothermic event is detected during the cooling. This is due to the fact that undercooling degree of such a small bump would be very high and the temperature range during which they solidify would also be very large. Moreover, as it will be seen latter, during a reflow up to 240°C with a heating rate of 3°C/min, the alloy will stay in the liquid state for about 8 mins. During this time a large quantity of Sn will react with Ni leading thus to a decrease of Sn volume in a bump which in turn will lead to higher undercooling degrees.

The DSC signal during heating shows a first endothermic peak around 221°C and surprisingly it is followed by an exothermic peak at around 226°C. We have repeated several times these experiments and both peaks are observed all the time. Endothermic peak appears at a temperature very close to the eutectic melting point. This clearly shows that the composition of the solder alloy is situated around the eutectic composition i.e. Sn-3.5wt%Ag. The heating rate of 3°C /min means that the time for heating from 180°C to 221°C would be around 12 min. It is possible that during this time, some Sn got consumed in formation of IMCs due to interfacial reaction between 1 µm of Ni and 3 µm of Sn. Indeed as it will be seen latter in chapter, this can lead to formation of about 1 µm of IMC at solid Sn/Ni interface. In other words, 0.9 µm ($\sim$ 30%) of Sn will be consumed, this means that the Ag content will increase from the target composition (2wt%) to about 3wt%, which is very close to the eutectic composition, thus more Sn-Ag will melt at eutectic melting point. The quantity of heat measured during melting corresponding to one bump of 5 µm diameter in about 2-3 mJ/bump as shown in Figure 3.7. This value is close to the calculated value of ΔH^*_1=2.1mJ/bump.

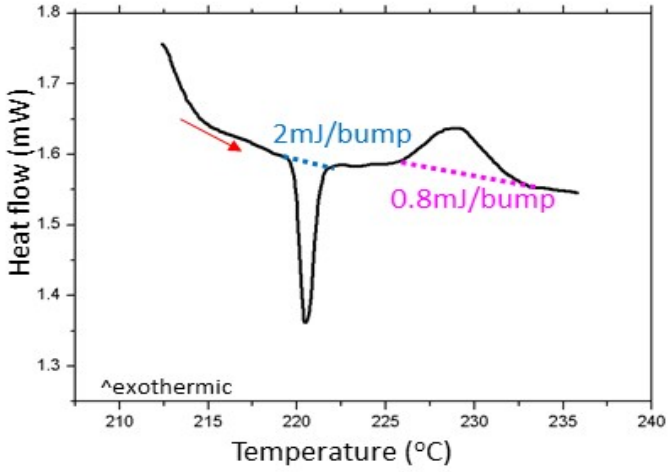


Figure 3.7: Typical DSC curves during heating of 5 µm diameter pillar (test vehicle 1) with a heating rate of 3°C/min

To the best of our knowledge no exothermic peak is reported in the literature during heating of Sn based alloy deposited on Ni or Cu or any other substrate. This exothermic peak appears 30-40 secs after the end of the first peak. At the end of the first peak, since Sn is melted, it will interact with the Ni to form Ni_3Sn_4 IMC, thus heat will be released in the process because the enthalpy formation of Ni_3Sn_4 phase is negative ($\Delta H_{f(Ni_3Sn_4)}$= $\sim$ -30 kJ/mol [110]). In the larger bumps (e.g. test vehicle 3 with Sn = 10-25 µm) the interaction goes on, giving a gradual increase in the DSC signal from the base line and it will continue till the end of the

experiment without giving any peak like in case Figure 3.5. However, if Sn gets consume first (i.e. before the end of experiment), then the DSC signal would go back to the base line, forming an exothermic peak like in Figure 3.7. The latter case is only possible for the bumps where the thickness of Sn layer is very low like in the case of test vehicle 1. Note finally that this heat release also occurs during solid state reaction (during heating) but, as it will be seen in the following sections, the growth kinetics of IMC layer in the liquid Sn/Ni system is much higher than in the solid/Ni system so the heat release will be much higher during the liquid Sn/Ni reaction.

3.2.2 MICROSTRUCTURE OF THE SOLDER BUMPS (5 µM)

Figure 3.8 gives a typical microstructure of the solder bumps of the test vehicle 1 (5 µm bumps) after deposition and after reflow at 250°C for 60 secs. The target composition of solder alloy is Sn-2wt%Ag. In general, the microstructure of the as deposited and reflowed solder is homogeneous without any large (micrometric) precipitate. However, at times, micrometric precipitates rich in Ag are observed in as-deposited solder alloy and after melting (reflow and after bonding) as shown in Figure 3.9.

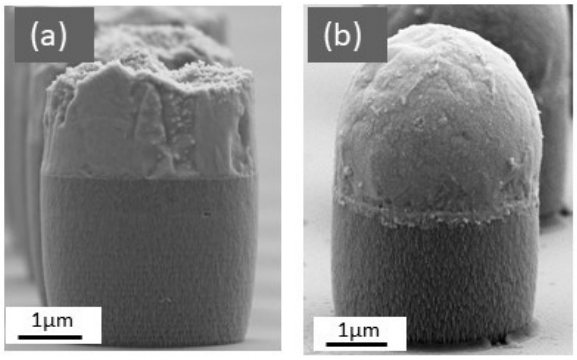


Figure 3.8: A typical microstructure of the solder bumps of the test vehicle 1 (5 µm bumps) (a) after deposition and (b) after reflow at 250°C for 60 secs. The target composition of solder alloy is Sn-2wt%Ag

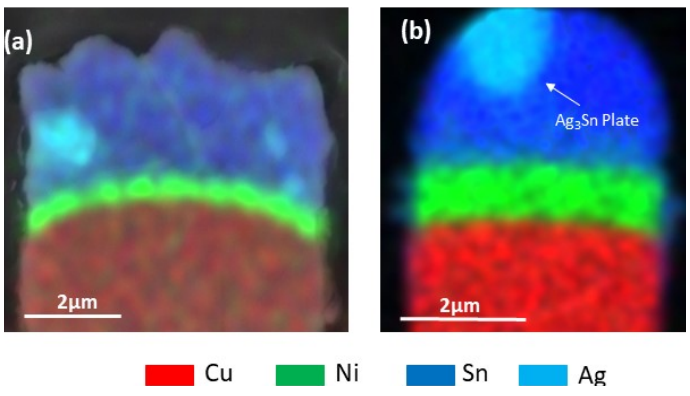


Figure 3.9: EDX analysis of test vehicle 1 (a) after deposition and (b) after reflow at 250°C for 60 secs

The origin of rich Ag precipitates in as deposited solder could be due to the fabrication process. Indeed, the fabrication of solder alloy at this dimension is very critical, usually at this dimension it is challenging to get uniformly distributed Ag throughout the solder alloy (as shown in Figure 3.9 (a)), thus some places within the solder bump, might have higher concentration of Ag than some other places in the bump. After reflow (or after bonding) the precipitates are Ag_3Sn in nature and the volume of these precipitates is 1-2 μm^3 in bulk solder i.e. the volume fraction (taking volume of solder $V_1 \approx 60\ \mu m^3$) is about 1.6-3.2vol% see Figure 3.9 (b).

The presence of rich Ag precipitates inside some reflowed bump could be due to different factors. The first factor could be high concentration of Ag in some region in solder alloy which could be due to the fabrication process, i.e. electrochemical deposition, as described above. According to Figure 3.6, if the Ag concentration gets higher than 3.5% in the bulk, then large precipitates of Ag_3Sn could be formed in the bulk solder.

The second factor could be due to the formation of Ni-Sn intermetallics during the reflow. As reflow is performed, more Sn is being consumed in the formation of Ni-Sn IMCs. Since there is no ternary compound between Ni, Ag and Sn, the concentration of Ag in the bulk solder increases. (For example, after reflow, when 1 µm thick Ni_3Sn_4 is formed, about 0.9 µm ($\sim$ 30%) of Sn is consumed . This increases the Ag content form 2wt% to about 3wt% which can lead to the precipitations of primary Ag rich precipitates during the solidification of the bump.

The third factor is due to undercooling phenomena. The solidification (during cooling) of Sn based alloys is affected by the difficulty in nucleation of Sn which causes high degree of undercooling. Usually in this scenario, Ag_3Sn is the first phase which is formed inside the melt (molten solder and Ag_3Sn) and grows rapidly, later it acts as the site of nucleation for Sn [111]. Thus Ag_3Sn aggregates are seen in bulk solder. This can also be one large Ag_3Sn aggregate, when the degree of undercooling is about 15-20°C [30, 111].

3.3 Study of interfacial interactions between solid Sn and Ni

As it was seen in the Section 3.2.1, the heating rate of 3°C/min causes significant growth of IMC due to solid-state interfacial reaction between Sn and Ni below the melting point of Sn-Ag alloy. Therefore it is now important to determine the growth kinetics of Ni-Sn IMCs by solid state interaction and the mechanism behind the interaction. Thus, solid state interaction between Sn and Ni at 150-210°C is studied in this section. For this study, *test vehicle 2* is used i.e. diameter of the bump d_2=150 µm and height of the bump h_2 = 3 µm. For this test vehicle, the interfacial layer (IMC) is already formed after deposition and its thickness is equal to 120 nm.

3.3.1 Experimental results for solid Sn-Ag/solid Ni interactions at 150-210°C

Figure 3.10 shows two SEM micrographs of the sample maintained for 1 minute at 210°C. Figure 3.10(b) shows that an almost scallop-shaped morphology reaction layer about half a micron thick is formed at the interface. Thus, during 1 minute of annealing at 210°C the thickness of the reaction layer increases by about **0.35 µm** (initial thickness before annealing equal to 0.12 µm). Moreover, as it will be shown below, the thickness of the reaction layer increases by about **0.15** and **0.20 µm** after 1 minute of annealing at 180 and 200°C respectively. These results clearly indicate that the solid Sn-Ni interactions during the heating up of Sn-based solders (Sn-Ag-Cu, Sn-Ag or Sn-Cu) from the room temperature to the melting temperature ($T_m \sim$ 218 - 227°C [105, 114]) are significant and may play a crucial role on the subsequent liquid Sn-Ni interactions during the reflow process. Indeed, for classical heating rate of about 60°C.min^{-1} used in a reflow process [28–30, 46], it can be easily calculated that, the solid state reaction occurring during heating from about 180°C to T_m may lead to the formation of a continuous IMC layer of some hundreds of nanometers thick.

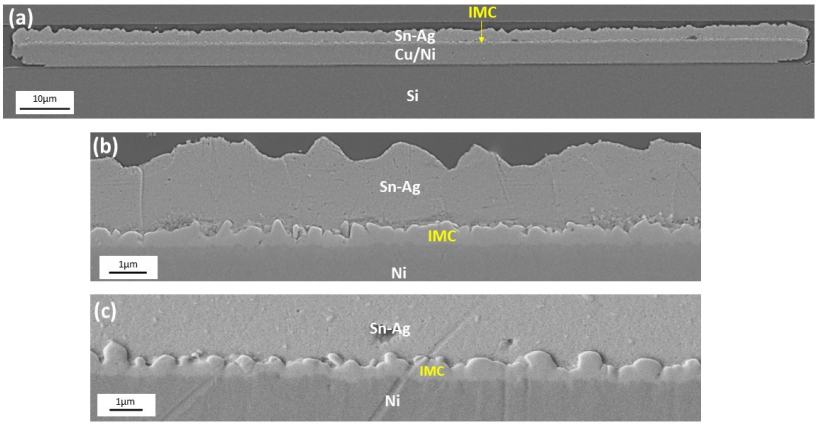


Figure 3.10: (a) General view of a sample after an isothermal holding for 1 minute at 210°C showing the formation of a reaction layer about 1 µm thick all over the solid Sn-Ag/Ni interface. (b) SEM micrographs of the solid Sn-Ag/Ni after 1 minute at 210°C and (c) liquid Sn-Ag/Ni interface after 1 minute at 230°C

Figure 3.11 to Figure 3.14 show SEM images of the Sn-Ag/Ni interface after different isothermal holdings at 150-210°C. EDX analysis of the reaction layer shows that it corresponds to Ni_3Sn_4 phase (43.5 at% Ni and 57.5 at% Sn) as shown in Figure 3.15. This result is in agreement with numerous studies which reported in the literature that Ni_3Sn_4 phase is the only phase that forms and grows at the solid Sn/Ni interface for temperatures lower than 220°C. Thus according to the equilibrium binary Ni-Sn phase diagram (see Figure 3.16), the Ni/Ni_3Sn_4 and Ni_3Sn_4/Sn interfaces are in metastable and stable equilibrium respectively.

Figure 3.11 to 3.14 show that, whatever the experimental temperature, the interfacial IMC layer exhibits first an almost scallop-shaped morphology. When the reaction time increases or when the temperature increases up to 210°C, a slight change in the morphology of the reaction layer is observed: the scalloped-form morphology is progressively replaced by large faceted crystals. The scalloped-form morphology is reported by numerous studies in the literature for long-time solid Sn-Ni interactions (longer than 1 hour) where the initial Sn/Ni interface is prepared by a reflow process [75, 79, 80, 82, 83, 85, 87], by immersing Ni foils in the liquid Sn bath [113], by electrochemical deposition [77] or by diffusion-couple technique [74]. On the contrary, the faceted morphology is reported in only one study (1000 hrs at 150°C) [88].

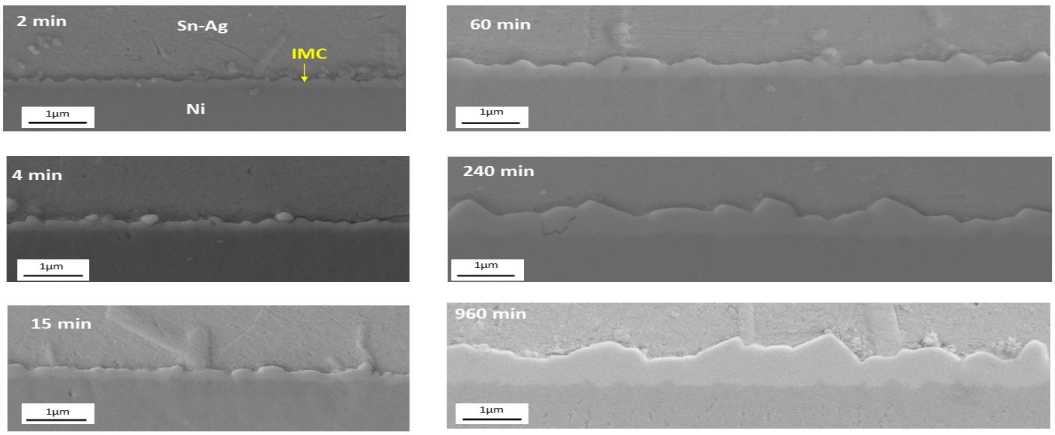


Figure 3.11: SEM micrographs of the reaction product formed at the solid Sn-Ag/Ni interface for the samples which were aged at 150°C for 2 to 960 mins

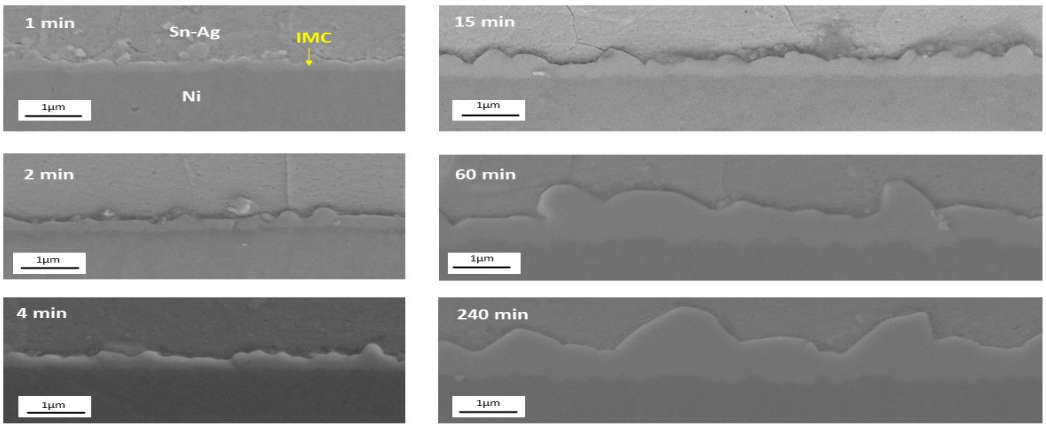


Figure 3.12: SEM micrographs of the reaction product formed at the solid Sn-Ag/Ni interface for the samples which were aged at 180°C for 1 to 240 mins

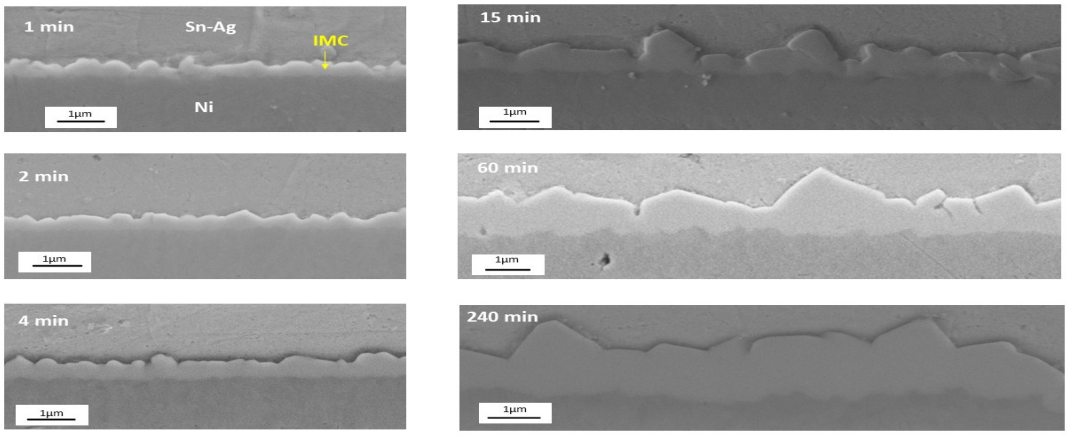


Figure 3.13: SEM micrographs of the reaction product formed at the solid Sn-Ag/Ni interface for the samples which were aged at 200°C for 1 to 240 mins

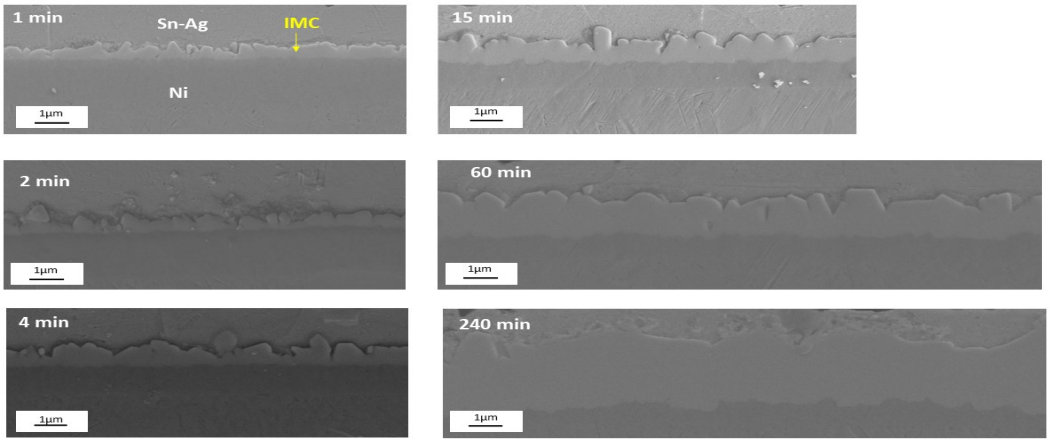
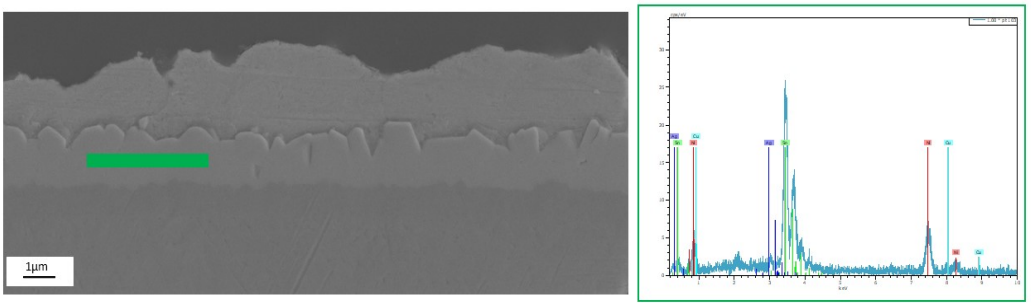


Figure 3.14: SEM micrographs of the reaction product formed at the solid Sn-Ag/Ni interface for the samples which were aged at 210°C for 1 to 240 mins



Element	Series	Wt%	At%	Error (Wt%)
Ni	K-series	20.54	40.67	0.9
Sn	K-series	74.56	59.32	1.9

Figure 3.15: EDX analysis of reaction product formed at the solid Sn-Ag/Ni interface for the samples which were aged at 210°C for 1 hr

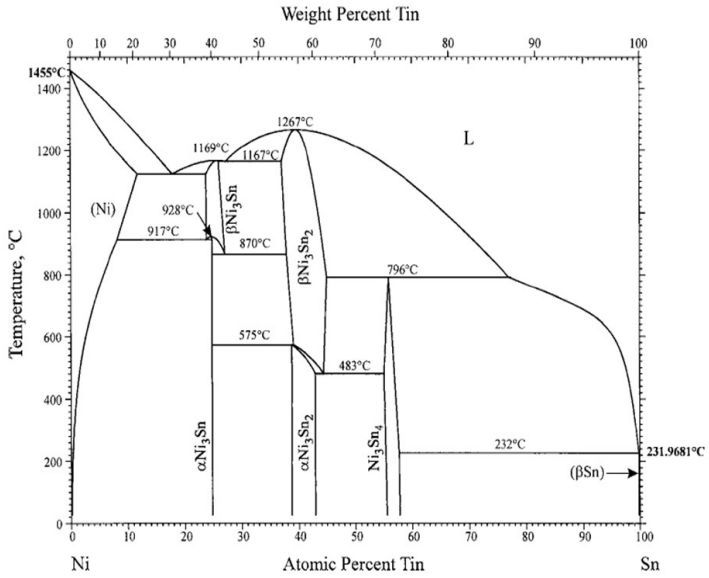


Figure 3.16: Binary Ni-Sn phase diagram [66]

3.3.2 Growth kinetics of the Ni_3Sn_4 layer by solid state reaction

Experimental determination of the growth law and activation energy

The values of the average thickness (e) of Ni_3Sn_4 layer measured after different holding temperature and time are given in Table 3.2. Figure 3.17 gives the variation with the reaction time of the average thickness of each Ni_3Sn_4 layer. In order to determine the growth law of the Ni_3Sn_4 layer, we assume that its growth kinetics follows a power law:

$$e = k_n t^n \tag{3.2}$$

Table 3.2: Average thickness (e) of the Ni_3Sn_4 layer formed at solid Sn-2wt%Ag alloy/Ni interface for different holding temperatures and reaction times.

t (min)	1	2	3	4	5	15	30	60	120	180	240	960
150°C		0.173	0.186	0.215	0.239	0.274	0.298	0.370	0.500	0.46	0.522	0.699
180°C	0.257	0.270	0.274	0.298	0.312	0.384	0.486	0.63	0.782	0.700	0.813	
200°C	0.323	0.391	0.422	0.495	0.517	0.583	0.757	1.044	1.240	1.310	1.540	
210°C	0.470	0.500	0.550	0.730	0.840	0.952	1.330	1.570	2.600	2.140	2.790	

where e is the thickness of the layer at time t, n is a growth exponent and k_n the kinetic growth coefficient. Note that Eq. 3.2 is only valid if it operates during the growth of the layer from t = 0 (e = 0) to t = t (e = e). The values of n for Ni_3Sn_4 phase growth kinetics reported in the literature are situated between about 0.4 [74–77, 85] and 0.5 [75, 78, 82, 83, 86–88].

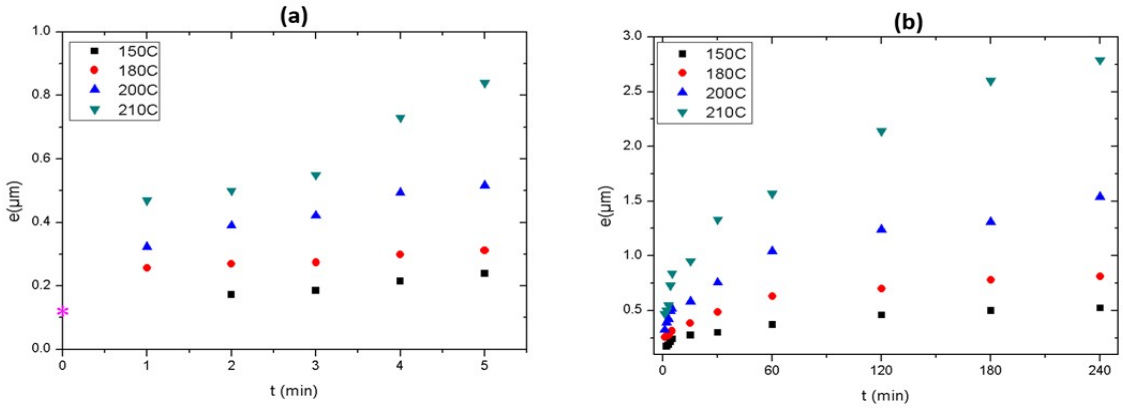


Figure 3.17: Average thickness of Ni_3Sn_4 layer formed at the solid Sn-Ag/Ni interface versus reaction time at 150, 180, 200 and 210°C, initial thickness at time t = 0 : e_0 = 0.12 µm(*)

The value of n is calculated by plotting logarithm of e as a function of logarithm of t shown in Figure 3.18. The slope of this graph will give n and the intercept will give the value of kinetic growth coefficient. We note that values of n obtained from Figure 3.18 are not rigorously the same, with a dispersion around n $\sim$ 0.3. n $<$ 1 which suggests that the growth kinetics is limited by diffusion. In order to evaluate the apparent activation energy of the growth process we need to choose a same approximate value of n $\approx$ 1/3 for all temperatures and calculate the corresponding growth coefficient. Thus, according to Eq. 3.2, the thickness of the reaction layer (e) is practically proportional to the cube root of reaction time:

$$e^3 - e_o^3 = k_3 t \tag{3.3}$$

(with k_3 in $m^3.s^{-1}$) where e_0 is the thickness of the layer at the experimental time t = 0.

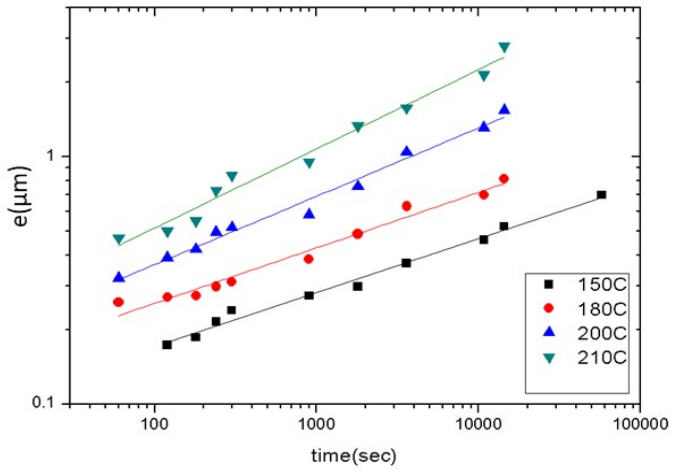


Figure 3.18: Log-log plot of the variation of Δe with the reaction time at 150, 180, 200 and 210°C. $\Delta e = e - e_0$. e and e_0 are the average thickness of Ni_3Sn_4 layer formed at the solid Sn-Ag/Ni interface at time t = 0 and t respectively (in our case e_0 = 0.12 µm)

Note that with $e_0 = 120$ nm we have $e_o^3 << e^3$ for all experimental conditions (see Table 3.2). Under these conditions, Eq. 3.3 becomes $e^3 \approx k_3 t$, or:

$$e \approx k_{1/3} t^{1/3} \tag{3.4}$$

with $k_{1/3}$ in $m.s^{-1/3}$

Figure 3.19 presents the variation of the reaction layer thickness with the cube root of reaction time at different temperatures. From this figure, the growth constant for Ni_3Sn_4 phase layer at different temperatures is deduced and reported in Table 3.3. It is assumed that $n \approx 1/3$.

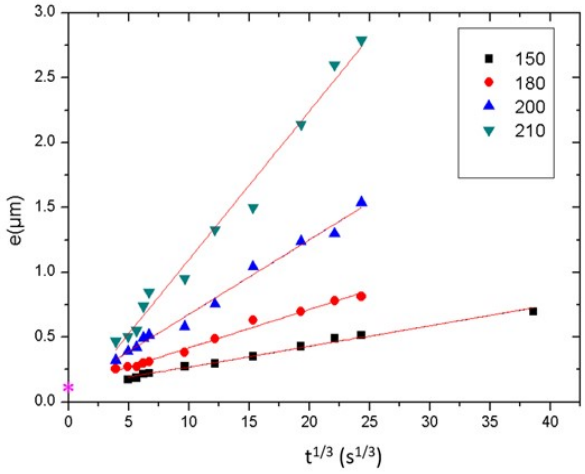


Figure 3.19: Thickness (e) of the Ni_3Sn_4 phase layer for the Sn-2%Ag alloy/Ni diffusion couple and thickness of as a function of the cube root of reaction time. The straight lines represent the linear fit of the data for $e = k_{1/3} t^{1/3}$ (see text)

Table 3.3: Calculated values of the growth constant (k) of Ni_3Sn_4 layer at solid Sn-2wt%Ag alloy/Ni interface and of growth exponent n (see Eq 3.2) at 150 to 210°C. Gibbs free energy formation of Ni_3Sn_4 phase ($\Delta G_{Ni_3Sn_4}$) from pure Ni and Sn solids at 150 to 210°C [69, 127]. Calculated values of the average grain boundary diffusivity ($\bar{D}^*_{gb}$) in Ni_3Sn_4 compound at 150 to 210°C.

(°C)	150	180	200	210
T(K)	423	453	473	483
$k_{1/3}$ ($\mu m.s^{-1/3}$)	0.0160	0.0296	0.0576	0.115
$k_3 = k_{1/3}{}^3$ ($m^3 s^{-1}$)	4.10×10^{-24}	2.59×10^{-23}	1.91×10^{-22}	1.52×10^{-21}
$\Delta G_{Ni_3Sn_4}$ (J/mol of at.) [Refs]	-23113	-22955	-22850	-22798
$\tilde{D}_{gb} \Delta x_\delta$ ($m_2.s_{-1}$)	1.11×10^{-16}	6.99×10^{-16}	5.16×10^{-15}	4.24×10^{-14}
$\tilde{D}_{gb}$ ($m^2.s^{-1}$)	1.70×10^{-17}	1.16×10^{-16}	8.94×10^{-16}	7.28×10^{-15}

It is assumed that $n \approx 1/3$

The value of n close to 1/3 obtained in this study is not very far from the value of n = 0.38 reported by Song et al [81] for calculated Ni_3Sn_4 IMC thickness between $\approx$ *250 nm* and 1

μm. But n ≈ 1/3 is in disagreement with the value of n ≈ 1/2 obtained in most of the studies dedicated to the long-term solid state interactions in Sn/Ni system [74–77, 79, 80, 82–86, 88], for which the reaction time was longer than 4 hours (up to some hundreds or even thousands of hours). As we will discuss below, for long-term solid state interactions and due to variation in microstructure of the layers, the value of n could be higher than 1/3.

The variation of the kinetic growth coefficient (k) with the temperature can be represented by the Arrhenius equation $k(T) = k_0.exp(-Q/RT)$ where k_0 is a growth constant, T the absolute temperature, R the gas constant and Q the apparent activation energy of the Ni_3Sn_4 layer growth. From the Arrhenius plot for Sn-Ag/Ni system at 150-210°C (see Figure 3.20), the activation energy is estimated to be Q = 53± 9 kJ mol^{-1}. This result is in agreement with Refs. [76–79, 81, 85] which reported values of Q varying from 34 to 57 kJ mol^{-1}. On the contrary, the activation energy determined in this study is much lower than the values reported in numerous Refs [74, 75, 80, 82–84, 86, 116], varying from 91 to 178 kJ mol^{-1}. As it was mentioned before, for all these Refs, the reaction time was longer than 4 hours thus the reported activation energy only concern with the long-term stages of Sn/Ni reaction.

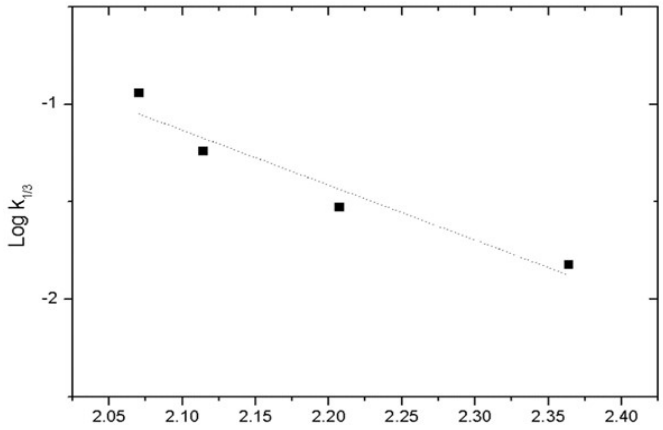


Figure 3.20: Arrhenius plot of Ni_3Sn_4 later growth in solid Sn-2wt%Ag alloy/Ni system

Below, we will discuss the formation mechanisms of Ni_3Sn_4 IMC during the first stages of solid Sn-Ni interactions based on a combined thermodynamic-kinetic analysis, then the evaluation of the integrated diffusion coefficient in the grain boundaries of the Ni_3Sn_4 phase is given followed by a discussion.

3.3.3 Combined thermodynamic-kinetic analysis of the growth kinetics of Ni_3Sn_4 layer at Sn/Ni interface

Theoretical aspects of IMC growth by reactive diffusion

As mentioned earlier, growth exponent n << 1 corresponds to the case where the growth kinetics of the IMC layer is limited by the diffusion process. In this subsection, theoretical aspect for growth of IMC layer due to different diffusion mechanisms is presented. The bulk (volume) diffusion-controlled growth of an IMC layer normally obeys a parabolic growth law,

i.e. n = 0.5 [117] whereas when the grain boundary diffusion dominates, a deviation from the parabolic growth law occurs with n < 0.5 and smaller n values are mainly due to the grain coarsening [118]. Values of n as low as 0.25 has been reported in the literature [47, 119].

To elaborate this point, let's consider a solid Sn/Ni diffusion couple as shown in Figure 3.21 (a). Here C is the concentration of Sn in a given phase (in $mol.m^{-3}$), e.g., C_δ is the concentration of Sn in δ phase (Ni_3Sn_4). The mole fraction of Sn in the δ-Ni_3Sn_4 phase is then given by $x_\delta = C_\delta/V_\delta{}^m$=4/7, where, $V_\delta{}^m$ is the molar volume of the Ni_3Sn_4 phase in m^3/mole of atoms. We assume that the so-called Wagner integrated diffusivity product $D_\delta \Delta C_\delta$ of average interdiffusion coefficient ($\tilde{D}_\delta = \tilde{D}$) and of concentration range through δ phase (ΔC_δ) remains constant during reaction.

z_1 and z_2 are the abscissa of Sn/δ and δ/Ni interfaces respectively. The distance between z_1 and z_2 gives the average IMC thickness, which is referred as e in this study, i.e. $e = z_2 - z_1$. For solid state interactions i.e. T < 230°C, Sn and Ni are mutually not soluble in one and another [120].

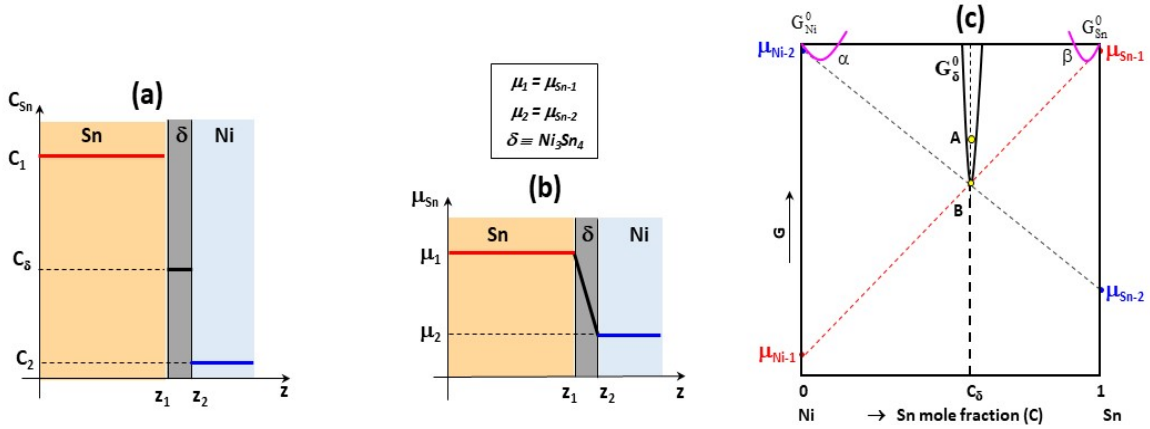


Figure 3.21: Schematic presentation of variation of Sn concentration (a) and Sn chemical potential (b) through the solid Sn/Ni interface when a continuous layer of δ- Ni_3Sn_4 phase is formed at the interface. Schematic presentation of variation of the Gibbs free energy versus Sn concentration in binary Sn-Ni system at T < 230°C, indicating the stable and metastable equilibria between δ-Ni_3Sn_4 compound and solid Sn or Ni as well as the chemical potentials of Ni and Sn corresponding to these equilibria

In such a case, the growth equations for one phase layer growing in diffusion-controlled regime are determined by the flux balance equations at the moving interfaces z_1 (Sn/δ) and z_2 (δ/Ni) (see Figure 3.21 (a)) and by Fick's law inside each phase:

$$(C_\delta^- - C_1)\frac{dz_1}{dt} = J_\delta - 0 \tag{3.5}$$

$$(0 - C_\delta^+)\frac{dz_2}{dt} = 0 - J_\delta \tag{3.6}$$

$$J_\delta = \frac{\tilde{D}\Delta C_\delta}{(z_2 - z_1)} \tag{3.7}$$

J_δ is a flux through the δ-Ni_3Sn_4 layer with respect to laboratory reference frame (Matano plane) and t is the time. (The fluxes through Sn and Ni phases are neglected ($J_1 = J_2 = 0$) because the solid solubility of Ni in Sn and Sn in Ni is practically zero). C_1 is the concentration in Sn phase. C_δ^- and C_δ^+ are the Sn concentrations in Ni_3Sn_4 phase at $z = z_1$ and $z = z_2$ respectively (see Figure 3.21 (a)). $\Delta C_\delta = C_\delta^+ - C_\delta^-$ (> 0) represents the concentration difference across the two interfaces of the Ni_3Sn_4 compound. Note that this value is too small to be measured accurately and this is the fundamental obstacle for using the Fick law containing the term $\tilde{D}\Delta C_\delta$. This obstacle can be removed by using the chemical potential gradient ($\Delta\mu_\delta / \Delta z$ - see Figure 3.21 (b)) instead of the concentration gradient ($\Delta C_\delta / \Delta z$) - see below. Given the very low value of $\Delta x_\delta = 0.018$ [121], we assume that the Ni_3Sn_4 is a stoichiometric compound, i.e., $C_\delta^+ \approx C_\delta^- = C_\delta (\Delta C_\delta \approx 0)$. Under these conditions, from Eq. 3.5- 3.7 one obtains:

$$\frac{d(z_2 - z_1)}{dt} = -\frac{C_1}{C_\delta (C_\delta - C_{1)}} \frac{\tilde{D}\Delta C_\delta}{(z_2 - z_1)} \tag{3.8}$$

As mention earlier, $e = z_2 - z_1$ is the thickness of Ni_3Sn_4 layer, thus Eq. 3.8 becomes:

$$e\frac{de}{dt} = -\frac{C_1}{C_\delta (C_\delta - C_1)} \tilde{D}\Delta C_\delta \tag{3.9}$$

In the following, we will briefly describe the determination of the growth law of δ-Ni_3Sn_4 layer, e(t), when the transport of reactive components is controlled either by bulk (volume) diffusion or grain boundary diffusion.

a. Bulk volume diffusion:

In this case, the solution of Eq. 3.9 (with the boundary condition: thickness increases from e_0 to e in time from t = 0 to t = t) leads to a parabolic growth law:

$$\frac{e^2 - e_o^2}{t} = -\frac{2C_1}{C_\delta (C_\delta - C_1)} \tilde{D}\Delta C_\delta = k_2 \tag{3.10}$$

b. Grain boundary diffusion:

In this case, the interdiffusion coefficient is given by $\tilde{D} = f\tilde{D}_{gb}$, where f is the volume fraction of grain boundaries contributing to the interdiffusion process given by:

$$f = \frac{\alpha\delta}{d} \tag{3.11}$$

d is the average grain size, δ is the grain boundary width and α is a factor form depending on the grain geometry (isolated boundary, parallel boundaries, cubic grains, spherical grains, general polycristals) [73, 122]. In this case, Eq. 3.9 leads to:

$$e\frac{de}{dt} = -\frac{C_1}{C_\delta(C_\delta - C_1)}\frac{\alpha\delta}{d}\tilde{D_{gb}}\Delta C_\delta \tag{3.12}$$

Depending on the grain growth, two cases can be distinguished in this regime:

(b-1) The grain growth is the single factor for IMC thickness increase

In this case, no new grains nucleate, just the increase in the grains size causes increase in the IMC thickness. This case is treated in detail by Furoto and Kahijara [118] who analyzed numerically the growth behavior of a compound layer controlled by grain boundary diffusion in a hypothetical binary system. It is assumed that the IMC layer is composed of a single layer of square-rectangular grains with an identical dimension, the square basal-plane is parallel to the interface (x-y plane), and hence the IMC grain length (l) is equal to the thickness of the IMC layer (see Figure 3.22 (a) and (b)). The growth of the IMC layer thickness (e = l) and the basal-plane IMC grain dimension i.e. grain width (d) are assumed to obey the laws: $e - e_0 = kt^n$ and $d - d_0 = k_d t^p$, respectively. The numerical solution in Ref [118] of this problem when p varies from 0 to 1/2 leads to values of growth exponent n varying from about 1/4 to 1/2.

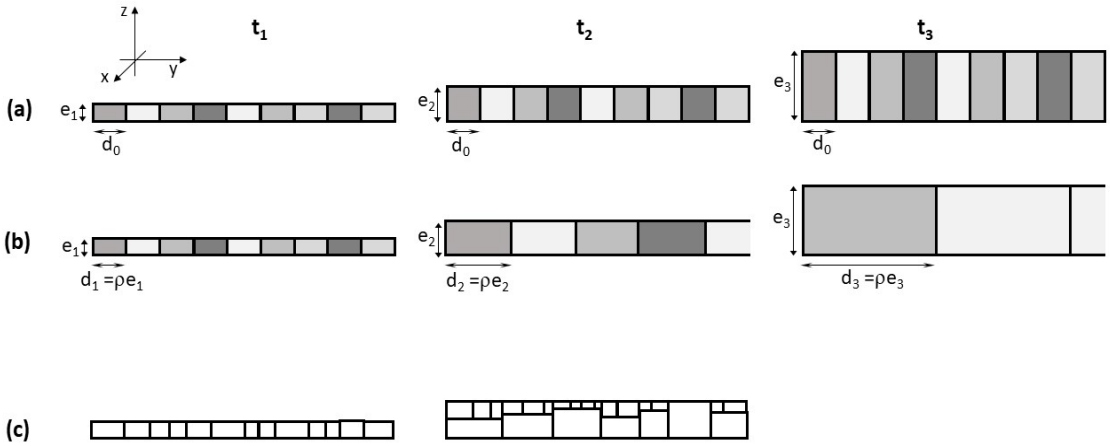


Figure 3.22: Schematic presentation of Ni_3Sn_4 grains growth at solid Sn/Ni interface without nucleation of new grains - the length of Ni_3Sn_4 grains is equal to Ni_3Sn_4 thickness (a and b), and with nucleation and growth of new grains at the reactive interfaces (c). (a) The width (d) of Ni_3Sn_4 grains remains constant during the growth process. (b) The ratio (ρ) between the thickness (e) of Ni_3Sn_4 layer and the width (d) remains constant during the growth process ρ = e/d = constant)

In the following, we further consider two simple limited cases: (i) d = constant (p = 0) and (ii) d proportional to e ($d = \rho e$, i.e. $p \approx n$).

(i) *The basal-plane IMC grain dimension d remains constant (p = 0)* - Figure 3.22 (a).

In this case, the solution of Eq. 3.12 leads to a parabolic growth law (n = 1/2):

$$\frac{e^2 - e_o^2}{t} = -\frac{2C_1}{C_\delta(C_\delta - C_{1)})}\frac{\alpha\delta}{d}\tilde{D_{gb}}\Delta C_\delta = k_2' \tag{3.13}$$

Thus, the parabolic relationship holds well not only for the volume-diffusion controlling

process (Eq. 3.10) but also for a mixed rate-controlling process without grain growth.

(ii) *The basal-plane IMC grain dimension d varies linearly with the layer thickness (e): d = ρe* - Figure 3.22 (b). In this case, the solution of Eq. 3.12 with d =ρe, leads to a cubic growth law (n = 1/3) for the reaction layer:

$$\frac{e^3 - e_o^3}{t} = -\frac{3C_1}{C_\delta(C_\delta - C_{1)}}\frac{\alpha\delta}{\rho}\tilde{D_{gb}}\Delta C_\delta = k_3 \tag{3.14}$$

(b-2) Grain growth and formation of new grains at reactive interface(s) contribute to IMC thickness increase

In this case, the growth of the IMC is due to the nucleation and growth of these new grains as well as growth of the old grains. In this case the variation of the fraction of grain boundaries function f = αδ/d with time or the variation of the mean value of the basal-plane grain dimension (d) with time could be a complex function and thus the solution of Eq. 3.12 becomes more complex. For this reason, this case will not be studied in detail here.

However, according to numerous works reported in the literature, the growth of IMC layer(s), limited by grain-boundary diffusion, can follow a logarithmic growth law $e - e_0 = kt^n$ with experimental values of the growth exponent n varying from 1/4 to 1/2. Finally, in addition to the case b-1-(i) treated above (where n = 1/2), sometimes n = 1/2 is obtained when the growth kinetics can lead to the establishment of a more or less constant average lateral width of the grain structure and thus an almost parabolic growth law can be established (see for example Ref. [89]).

3.3.4 Evaluation of the grain boundary diffusion in Ni_3Sn_4 phase

To evaluate the limiting mechanism of diffusion, grain analysis for Ni_3Sn_4 layer was done (according to the process described in Section 2.4). In the analysis, the average values of the basal-plane dimension of grain (width d) and the length of grain (l) were determined for two temperatures: 150°C (at 5 mins and 16 hrs) and 200°C (at 5 minutes and 4 hrs) - see Figure 3.23. The results are presented in Table 3.4. It was found that for lower temperature i.e. 150°C, the length of the grain is almost equal to the layer thickness (l ≈ e) and thus the aspect ratio ρ = d/l is almost equal to 1. This particular grain growth characteristic (l ≈ e and ρ = d/l ≈ d/e ≈ 1) corresponds to the case b-1-(ii) presented above for which the corresponding growth exponent n is equal to 1/3. Also experimentally, n was found to be not far from 1/3 for this case (see Table 3.3).

However for the higher temperature (200°C) two cases were seen. At t = 5 mins, only one range of grains are present and the aspect ratio is close to 1 whereas for longer time (t = 4 hrs), new nucleated grains are observed (Figure 3.23 (b)) (i.e. case b-2). The average size of these *new* grains is about 30% of the thickness of reaction layer (the average size of Ni_3Sn_4 grains on the Ni side is two times larger than that of grains on the Sn side). These results clearly indicate that, after a certain *critical time* of reaction at 200°C a deviation from the cubic growth law may take place (leading to an increase in n value). Simple calculation based on Eq. 3.14 and

Tables 3.2 and 3.3 allows to evaluate the *critical time* to be at least longer than about 120 mins. This critical time (when it exists) may depend on many parameters such as the temperature, the microstructure of Ni and Sn substrates, the level of impurities contained in Ni and Sn, ... However, this point is out of the scope of this study.

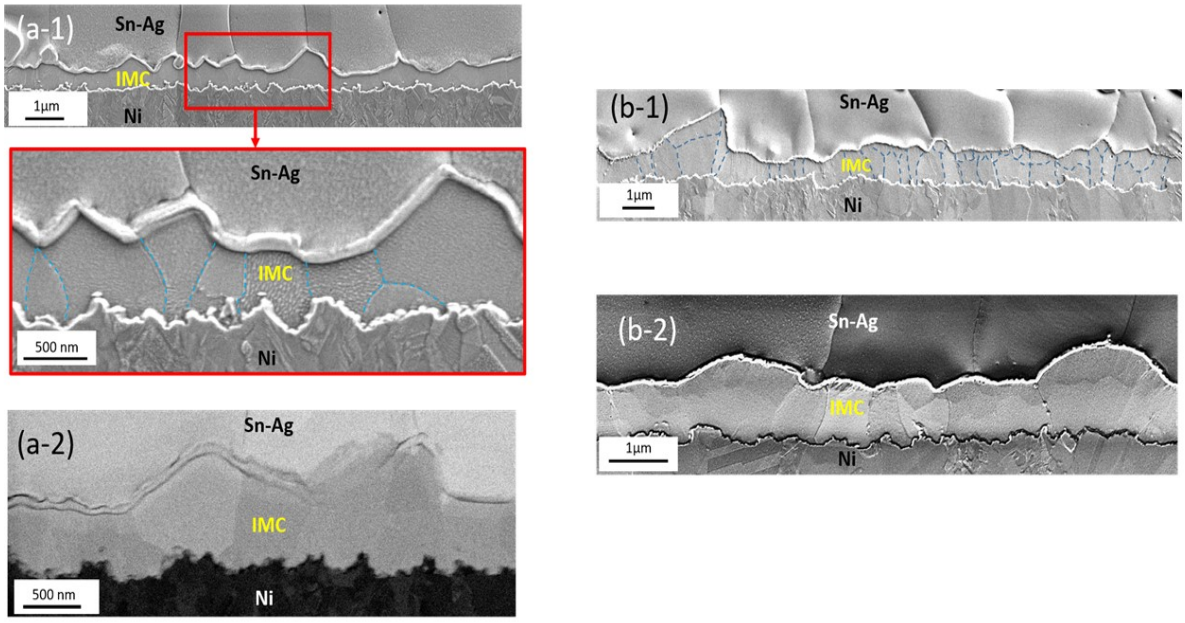


Figure 3.23: SEM micrographs of the Ni_3Sn_4 reaction layer formed at solid Sn/Ni interface showing the grains of Ni_3Sn_4 phase (with 15 µm average length of cross-section) (a) T = 150°C, t = 16 hours - only one range of grains is observed. (b) T = 210°C, t = 4 hours - two ranges of grains are observed

Table 3.4: Experimental values of the average width (d) and length (l) of Ni_3Sn_4 grains formed at Sn/Ni interface after isothermal holdings at 150°C (5 and 960 mins) and at 200°C (5 and 240 mins) - see Figure 3.23. In all cases only one range of grains is observed (length l = layer thickness = e) except for 240 min at 200°C for which two ranges of grains are observed with average widths and lengths (d_1, l_1) and (d_2, l_2) respectively.

T(°C)	t (min)	d (nm)	l = e (nm)	ρ (d/l)	
150	5	124	150	0.83	
	960	584	557	1.04	
200	5	482	533	0.90	
	240	d_1 =671 nm	l_1 = 596 nm	1.13	large grains
		d_2 =296 nm	l_2 = 301 nm	0.98	small grains

Given the fact that, the experimental evolution of the Ni_3Sn_4 layer thickness in this study follows approximately a cubic law (see Figure 3.19) and mostly in all cases the layer growth is occurring through grain coarsening, we can conclude that the growth kinetics of Ni_3Sn_4 compound, formed by solid state diffusion between Ni and Sn, is limited by the interdiffusion process through the grain boundaries of this phase. This conclusion is also supported by activation

energy found in this work which is equal to about 53 kJ.mol^{-1}. This value is close to the activation energy of the Sn tracer diffusion in the grain boundary of pure Sn (40-50 kJ.mol^{-1}) [123] and much lower than the activation energy of self-diffusion in Sn (100-110 kJ.mol^{-1}) and in Ni (280 - 290 kJ.mol^{-1}) [123].

Thus, we can evaluate the integrated diffusion coefficient ($\tilde{D}_{gb}\Delta x_\delta$) in the grain boundaries of Ni_3Sn_4 phase from Eq. 3.14. By assuming that the partial molar volume of Sn in Ni_3Sn_4 is equal to the molar volume of Sn, Eq. 3.14 leads to:

$$\tilde{D_{gb}}\Delta x_\delta = -\frac{x_\delta(x_\delta - x_1)}{3x_1}.\frac{\rho}{\alpha\delta}.k_3 \tag{3.15}$$

Note that, application of Eq. 3.15 needs the knowledge of thermodynamic data (x_δ and x_1) as well as of other quantities characterizing the Ni_3Sn_4 grains (ρ, δ and α).

In our case, the *aspect ratio of the grain* ρ = d/e is found to be close to unity (ρ = 1).

Concerning the Ni_3Sn_4 *grain boundary width* δ, no data exists in the literature. In a recent study, Prokoshkina et al [124] gave a summary of experimental values of average values of δ reported in the literature for a large number of metallic materials (Figure 4 in Ref [124]). The value of δ depends on the studied material as well as on its crystalline structure and most of values of δ are situated between 0.3 and 2 nm [124]. For our application we choose an average value of **δ= 1 nm**.

As it was specified in section 3.3.3, α *is a factor form* [73, 122] and its average value depends on the geometry of the grains. In our experiments, Ni_3Sn_4 grains have an almost cubic form with an average size d = e, thus the volume fraction (f) of the grain boundaries with a width δ can be easily calculated and is given by the following relation:

$$f = \frac{3\delta}{d} \tag{3.16}$$

By comparing Eq. 3.11 and Eq. 3.16 we deduce that the value of the factor form, for cubic grains, is **α= 3**.

Application of Eq. 3.15 with x_δ = 4/7, x_1 = 1, α= 3, ρ = 1, δ= 1 nm leads to:

$$\tilde{D}_{gb}\Delta x_\delta = 2.7x10^7.k_3 \tag{3.17}$$

By using the experimental values of k_3 (see Table 3.3), the values of integrated diffusion coefficient are calculated for different temperatures and reported in Table 3.3. When temperature increases from 150 to 210°C, $\tilde{D}_{gb}\Delta x_\delta$ increases from about 1.1x10^{-16} to 4.2x10^{-14} m^2.s^{-1}.

At this stage, it is worth to emphasize that the evaluation of the interdiffusion coefficient in the grain boundaries of Ni_3Sn_4 phase ($\tilde{D}_{gb}$) needs the knowledge of the variation of molar fraction of Sn through this phase (Δx_δ) which is difficult to be measured accurately due to its low value. Indeed, the homogeneity range of Ni_3Sn_4 phase reported by Nash [121] is narrow 55.5-57.3at%Sn (Δx_δ = 0.018) whereas that reported by Schmetterer et al [120] at 500°C is much larger 53.2-57.0at%Sn (Δx_δ = 0.048). Moreover, in all our experiments, the Ni_3Sn_4 phase is

involved in a metastable equilibrium with Ni at Ni_3Sn_4/Ni interface (and in a stable equilibrium with Sn at Sn/Ni_3Sn_4 interface).

In order to evaluate the concentrations of different phases implied in the stable and metastable equilibria of Sn/Ni_3Sn_4/Ni system, we used the CALPHAD modelling of the binary Ni-Sn system with data issued from three research groups: Ghosh et al. [125], Liu et al [126] and Liu et al [127]. The calculated homogeneity range of Ni_3Sn_4 phase was found to be 0.440-0.570, 0.517-0.575 and 0.197-0.556 respectively. It can be seen that the respective calculated values of Sn concentration in Ni_3Sn_4 phase (x_δ) at Sn/Ni_3Sn_4 interface (x_δ^+ = 0.570, 0.575 and 0.556) are relatively close to each other and close to the experimental values reported in the literature (0.570 [121] and 0.573 [120]. However, the respective calculated values of x_δ at the metastable Ni_3Sn_4/Ni/ interface are very different (x_δ^- = 0.440, 0.517 and 0.197!) and far from experimental values (0.555 [121] and 0.532 [120]. Thus, under these conditions, it is difficult to choose a good value of Δx_δ (= x_δ^+ - x_δ^-).

This obstacle of missing data for Δx_δ through the metastable Sn/Ni_3Sn_4/Ni system can be removed if we use the chemical potential gradient ($\Delta\mu_\delta/\Delta z$) instead of the concentration gradient ($\Delta C_\delta/\Delta z$). As it is shown below, the combination of the grain boundary diffusivities of Sn ($D^*_{gb,Sn}$ and Ni ($D^*_{gb,Ni}$), averaged over the δ-Ni_3Sn_4 phase ($\bar{D}^*_{gb}$):

$$\bar{D}^*_{gb} = x_{Ni}\, D^*_{gb,Sn} + x_{Sn}\, D^*_{gb,Ni} \tag{3.18}$$

can be evaluated by using Eq. 3.17.

The relation between the interdiffusion coefficient $\tilde{D}_{gb}$ and tracer diffusion coefficients $\bar{D}^*_{gb}$ in Ni_3Sn_4 grain boundaries is given by [73]:

$$\tilde{D}_{gb} = (x_{Ni}\, D^*_{gb,Sn} + x_{Sn}\, D^*_{gb,Ni})(1 + \frac{\partial \ln\gamma}{\partial \ln x}) \tag{3.19}$$

γ_i is the activity coefficient intervening in the chemical potential expression of a species i (μ_i) in a condensed phase, referred to a standard state μ_i^0:

$$\mu_i = \mu_i^0 + RT \ln(\gamma_i x_i) \tag{3.20}$$

Here, we assume that the segregation effect in the grain boundaries of Ni_3Sn_4 phase is negligible, i.e., the variation of γ_i with x_i ($\gamma_i = f(x_i)$) is the same for both bulk Ni_3Sn_4 as well as grain boundary zone. In that case, the thermodynamic factor $\phi_\delta = 1 + \partial\ln\gamma/\partial\ln x$ is given by the following relation [69]:

$$\phi_\delta = 1 + \frac{\partial \ln\gamma}{\partial \ln x} = \frac{1}{\Delta x_\delta}\frac{\Delta G_\delta}{RT} \tag{3.21}$$

ΔG_δ is the molar Gibbs energy of formation for δ-Ni_3Sn_4 phase from pure solid Ni and Sn constituent (in J/mol of atoms). R is the constant of ideal gas: R = 8.314 $J.mol^{-1}.K^{-1}$. Eqs. 3.19 and 3.21 lead to:

$$\tilde{D}_{gb}\Delta x_{\delta} = (x_{Ni}D^{*}_{gb,Sn} + x_{Sn}D^{*}_{gb,Ni})\frac{\Delta G_{\delta}}{RT} \tag{3.22}$$

Finally, from Eq. 3.15 and Eq. 3.22, we obtain the expression of $\tilde{D}^{*}_{gb}$ as a function of the growth kinetics constant of Ni_3Sn_4 layer (k_3=$k^3_{1/3}$ in m^3s^{-1} : see Eq. 3.4 and Table 3.3 for $k_{1/3}$) and different physicochemical quantities of Ni_3Sn_4 phase :

$$\bar{D}^{*}_{gb} = x_{Ni}D^{*}_{gb,Sn} + x_{Sn}D^{*}_{gb,Ni} = \frac{\rho}{\alpha\delta}\frac{x_{\delta}(x_{\delta}-x_1)}{3x_1}\frac{RT}{\Delta G_{\delta}}k_3 \tag{3.23}$$

Putting values x_{δ} = 4/7, x_1 = 1, α= 3, ρ = 1, δ= 1 nm, in Eq. 3.23, leads to Eq. 3.24 which evaluates the values of *average* grain boundary diffusivity in the δ-Ni_3Sn_4 phase $\bar{D}^{*}_{gb}$ as a function of ΔG_{δ}, T and k_3:

$$\bar{D}^{*}_{gb} = x_{Ni}D^{*}_{gb,Sn} + x_{Sn}D^{*}_{gb,Ni} = -2.26x10^{8}\frac{T}{\Delta G_{\delta}}k_3 \tag{3.24}$$

With ΔG_{δ} = -25334 + 5.251T [128,129] and values of k_3 (given in Table 3.3), we can calculate the values of $\bar{D}^{*}_{gb}$ for different temperatures, which are reported in Table 3.3. This table shows that $\bar{D}^{*}_{gb}$ increases from $1.7x10^{-17}$ to $7.3x10^{-15}$ $m^2.s^{-1}$ when the temperature increases from 150 to 210°C.

3.3.5 Comparison with the results reported in the literature

To the best of our knowledge there are no available data in the literature for Sn or Ni grain boundary (tracer) diffusion in Ni_3Sn_4 ($D^{*}_{gb,Sn}$ or $D^{*}_{gb,Ni}$) nor in other intermetallics containing Sn. Thus, we cannot compare values of the average $\bar{D}^{*}_{gb}$ found in this study with values of $D^{*}_{gb,Sn}$ or $D^{*}_{gb,Ni}$, which in principle are different from each other ($D^{*}_{gb,Sn} \neq D^{*}_{gb,Ni}$). Nevertheless, there are very few data for Sn grain boundary tracer diffusion in solid solutions Pb-Sn (3.5 and 8.3 at%Sn) and Zn-Sn (23.7 wt%Sn) [124]. Thus, we are restricted to an estimation to an order of magnitude for comparison of the values of $\bar{D}^{*}_{gb}$ determined in this study with the reported data in the literature.

Compared to the melting point of Ni_3Sn_4 (T_m = 796°C (1069 K)), the higher temperature used in this study T = 210°C (483K) is about 45% of the melting temperature of Ni_3Sn_4. The Sn grain boundary tracer diffusion at the homologous temperature for Pb-Sn solid solution (T_1 = $0.45T_m$ (Pb) = 270K) and Zn-Sn solid solution (T_2 = $0.45T_m$ (Zn) = 312K) are about $1.5x10^{-14}$ and $5x10^{-15}$ $m^2.s^{-1}$ respectively [124]. These values are of the same order of magnitude as the *average* grain boundary diffusivity in Ni_3Sn_4 compound at 210°C which is determined in this study: $\bar{D}_{gb}{}^{*}$ = $1.5x10^{-15}$ $m^2.s^{-1}$. Also, the activation energy of the grain boundary tracer diffusion in Pb-In, Pb-Sn, Al-Zn and Zn-Sn solid solutions with relatively low melting points (327-660°C), are about 32-56, 19-53, 23-48 and 44-66 $kJ.mol^{-1}$ respectively [124], i.e. only some tens of $kJ.mol^{-1}$, i.e. of the same order of magnitude as reported in this study (Q = 53 $kJ.mol^{-1}$).

Thus we can conclude without ambiguity that, the growth kinetics of the Ni_3Sn_4 layer for reaction times shorter than 16 hrs at 150°C and shorter than about 4 hrs at 170-210°C is mainly controlled by grain boundary diffusion through the Ni_3Sn_4 layer. The main reasons for the cubic growth law (growth exponent n close to 1/3) of the Ni_3Sn_4 phase are (i) the nucleation and growth of new grains of Ni_3Sn_4 at the reactive interfaces are almost negligible and (ii) the aspect ratio of the grains remains almost constant. This is especially true at low temperature (150 and 180°C) for reaction times up to 4 hrs and for shorter reaction times at 200 and 210°C.

When the holding time and/or temperature increases, i.e. Ni_3Sn_4 layer thickness increases (for example above about 1 μm 200°C), the nucleation and growth of new grains takes place at the region close to the Sn-Ag/Ni_3Sn_4 interface (see Figure 3.23 (b)). This phenomenon leads to a decrease of the average grain size diameter (and especially of the grain size width) thus leading to a deviation from the third-power law of growth kinetics. Nevertheless, more experimental work is needed to determine the temperature and/or reaction time and/or reaction layer thickness (or other parameters such as the Ni and Sn grain size) beyond which a change in the control regime takes place during the Ni_3Sn_4 growth process at solid Sn/Ni interface.

3.3.6 Study of solid state interactions in solid Sn-Ag/Ni_3Sn_4/Ni system for latter stages (time > 1 day)

We recall that for long time interactions in the Ni/solid Sn system (reaction time longer than 1 day) there are numerous studies reported in the literature and all of them are unanimous on the fact that ***Ni_3Sn_4 phase is the only phase that forms and grows at the solid Sn/Ni and liquid Sn/Ni interface*** for temperatures lower than 300°C [47, 63]. Here, we investigate the growth kinetics for longer time interaction between solid Sn and Ni at 200°C for the aging times from 1 to 35 days to see for how long time the metastable phase (Ni_3Sn_4) remains stable. Since here the reaction time is longer, we used test vehicle 3 (Ni=5 µm and Sn=10-20 µm) for the study.

Figure 3.24 to Figure 3.27 gives some representative SEM micrographs of the reaction product formed at the Ni/solid Sn-Ag interface for the samples which were aged at 200°C for 1, 4, 15 and 35 days. In the micrographs an almost scallop-shaped morphology Ni_3Sn_4 reaction layer more than one micrometer thick is observed at the Ni/Sn interface. For reaction time more than 4 days (Figure 3.25 to Figure 3.27), a very thin reaction layer some nanometers thick is observed at the Ni/Ni_3Sn_4 interface. EDX analysis of this layer show that it corresponds to Ni_3Sn_2 phase (57 ± 5 at% Ni and 43 ± 5 at% Sn). This result is surprising and it is not in agreement with numerous studies [47, 63]. The only study that reports formation of Ni_3Sn_2 phase at temperature lower than 300°C is that of Bader et al [47], who also performed solid state reaction but for Ni/Ni_3Sn_4 system (and not for Ni/Sn system) at 240, 300 and 400°C for reaction time up to 5000 hrs. Formation of Ni_3Sn_2 phase in Ni/Ni_3Sn_4 system will be discussed in Chapter 4. Here we will discuss only formation of Ni_3Sn_2 phase in Ni/Sn system.

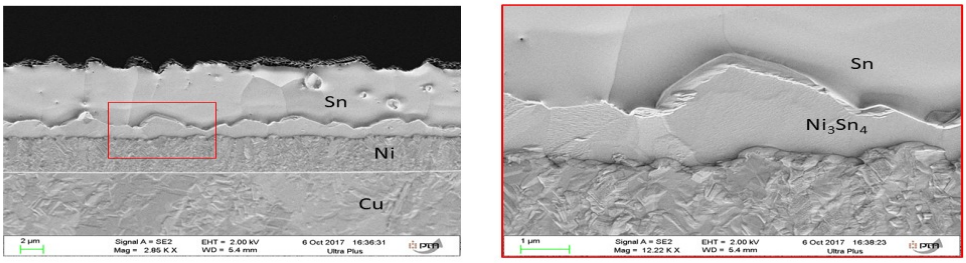


Figure 3.24: Representative SEM micrographs of the reaction product formed at the Ni/solid Sn-Ag interface for the samples which were aged at 200°C for 1 day

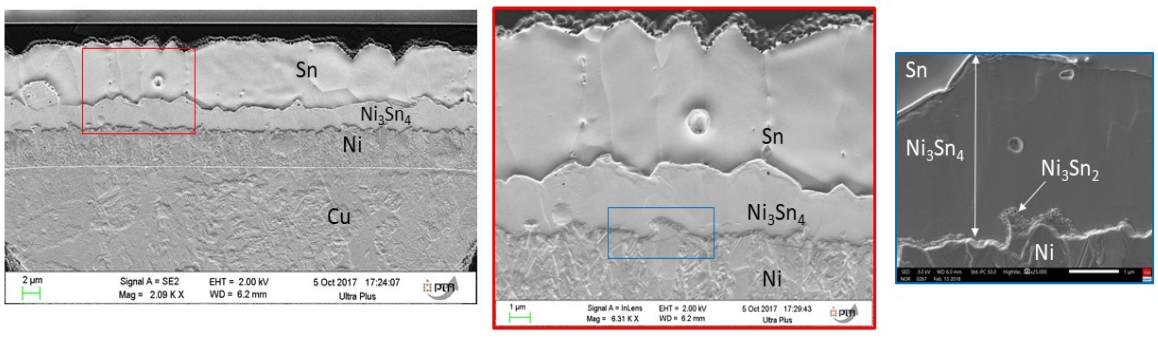


Figure 3.25: Representative SEM micrographs of the reaction product formed at the Ni/solid Sn-Ag interface for the samples which were aged at 200°C for 4 days

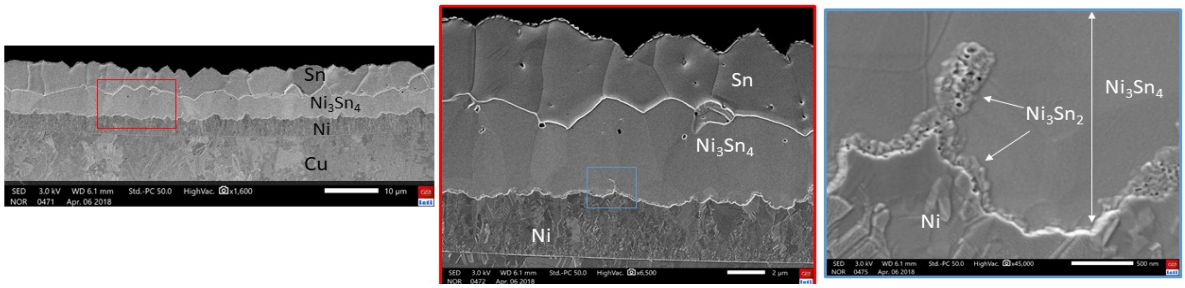


Figure 3.26: Representative SEM micrographs of the reaction product formed at the Ni/solid Sn-Ag interface for the samples which were aged at 200°C for 15 days

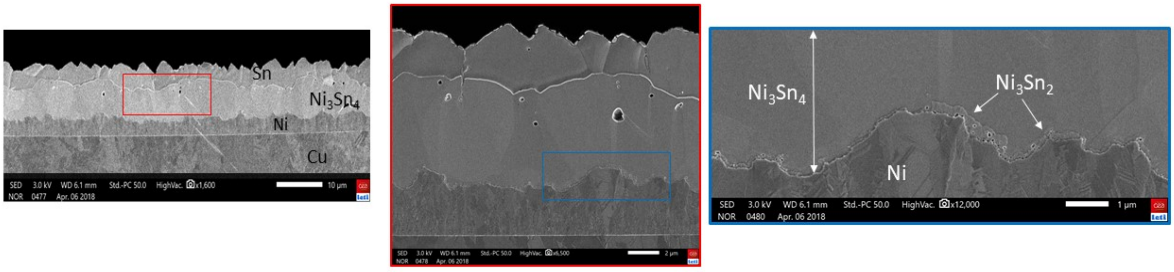


Figure 3.27: Representative SEM micrographs of the reaction product formed at the Ni/solid Sn-Ag interface for the samples which were aged at 200°for 35 days

The values of the average thickness (e) of Ni_3Sn_4 layer measured after different holding time at 200°C are given in Table 3.5. When the reaction time varies from 1 to 35 days, the average thickness of Ni_3Sn_4 layer increases from 1.7 to 5.8 µm. Figure 3.28 gives the variation with the reaction time of the average thickness of Ni_3Sn_4 layer. In order to determine the growth law of the Ni_3Sn_4 layer, we used the same method as mentioned in Section 3.3.2. The growth exponent (n) is found to be n $\approx$ 0.35. This result are not in agreement with experimental results reported in [74, 75, 85] (n in between 0.4-0.5).

However, the growth exponent for long time interaction is slightly higher than for initial stages of reaction (n $\approx$ 0.3 for t $\geq$4 hrs). This difference is clearly seen in the Figure 3.29, where all data for growth kinetics of Ni_3Sn_4 layer are reported. Moreover, the thickness of the interfacial layer after 24 hrs of reaction ($\approx$1.7 µm) is almost equal to that after 4 hrs of reaction ($\approx$1.5 µm). This disagreement may be due to the use of different test vehicles. For longer time reaction test vehicle 3 (with Sn = 10-25 µm) was used while, for shorter time reaction test vehicle 2 (with Sn = 3 µm) was used. As discussed in Section 3.1 of this chapter, the major difference between test vehicles 2 and 3 is in their fabrication process. The other reason may be the nucleation and the growth of new grains of Ni_3Sn_4 at Ni/Ni_3Sn_4 interface for long time interactions, as it is shown in Figure 3.30. This makes this case similar to the case shown in Figure 3.22 (c) where, as mentioned before, the n value will increase from 0.3 to 0.5. The n value obtained in this case (n = 0.35) could be due to this phenomenon. However, the reaction is still carried out through grain boundary diffusion.

Table 3.5: Average thickness of the Ni_3Sn_4 layer formed at solid Sn-2wt%Ag alloy/Ni interface at 200°C for reaction time between 1 day and 35 days

Days	1	4	15	35
Ni_3Sn_4 layer thickness (in µm)	1.68	2.58	4.20	5.85

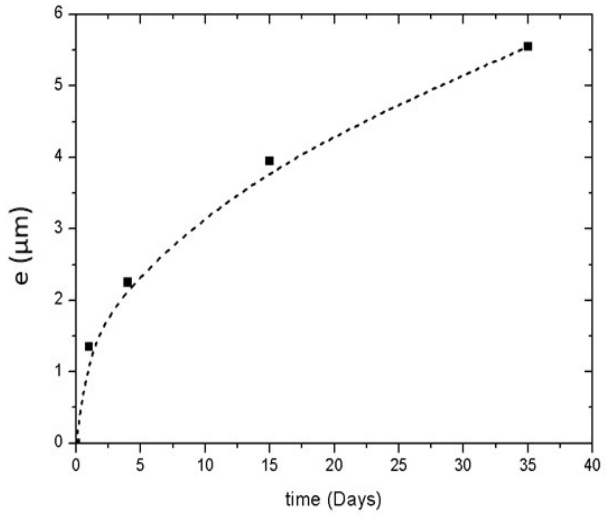


Figure 3.28: Average thickness of Ni_3Sn_4 layer formed at the Ni/solid Sn-Ag interface versus reaction time at 200°C

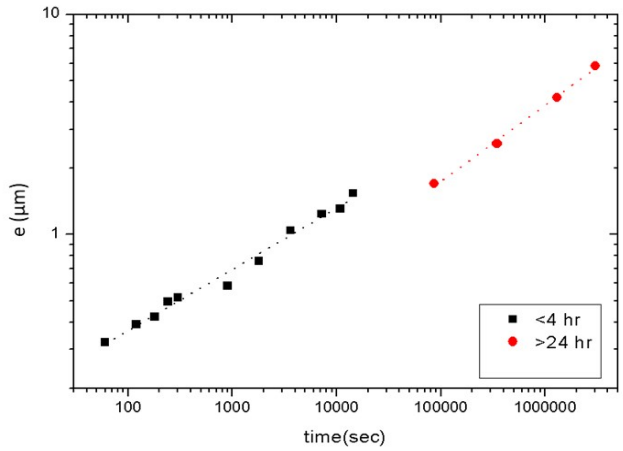


Figure 3.29: Log-log plot of the variation of Ni_3Sn_4 reaction layer thickness (e) with the reaction time at 200°C. For t< 4hrs test vehicle 2 is used (Sn=3 µm) while for t> 24 hrs test vehicle 3 is used (Sn=10-24 µm)

The most important result for longer time experiment ($\geq$ 4 days) is the observation of the formation and growth of Ni_3Sn_2 phase which was not observed for reaction times lower than 4 hrs. This result is being reported for the first time. In Figure 3.30, one can clearly distinguish formation and growth of new Ni_3Sn_4 and Ni_3Sn_2 grains. The Ni_3Sn_2 layer is a thin submicronic and not continuous layer across the Ni/ Ni_3Sn_4 interface. Therefore, at this point it is not possible to evaluate the growth kinetics of this layer. However, after 35 days of annealing at

200°C at places, the reaction layer grew up to about 6 µm. The fact that the Ni_3Sn_2 layer could not grow at the Ni/Ni_3Sn_4 interface for reaction times lower than 4 days could be due to 2 reasons: (i) As reported in the literature, the barrier energy of nucleation of Ni_3Sn_2 phase may be very high [46] and (ii) The very high growth rate of the "vampire" Ni_3Sn_4 phase prevents the formation and growth of Ni_3Sn_2 phase as long as the thickness of the "vampire" phase is lower than a critical value [69]. This behavior is similar to the growth behavior of Cu_3Sn phase at Cu/Cu_6Sn_5 interface in the Cu/Cu_6Sn_5/liquid Sn system [135] where the Cu_3Sn phase do not form and grow at the interface as long as the "vampire" Cu_6Sn_5 phase layer attains a critical thickness value (some hundreds of nm in case of Cu-Sn system). Here, by analogy, the critical thickness of the "vampire" Ni_3Sn_4 phase would be situated at about 2 µm.

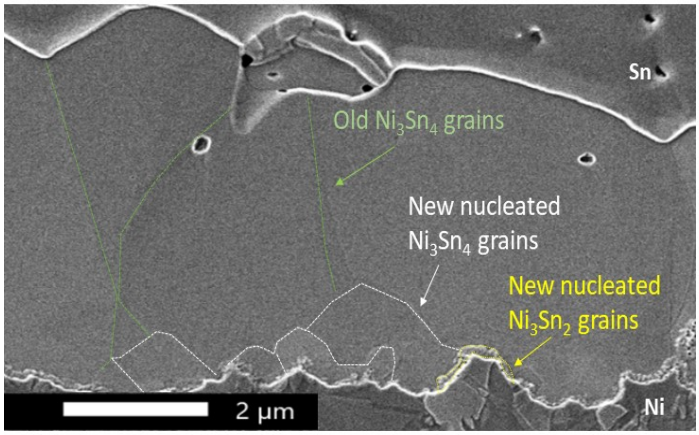


Figure 3.30: SEM micrographs of the reactions layer formed at solid Sn/Ni interface at 200°C for 15 days showing the grains of Ni_3Sn_4 phase (with 15 µm average length of cross-section) and grain of Ni_3Sn_2

3.3.7 Conclusions

Short time (1 to 15 mins) solid state interactions, between Sn-2wt%Ag alloy and Ni at 150-210°C, have been investigated for the first time. The latter stages of interactions (0.5-4 hrs and 1-53 days) are also studied in order to compare our results with those reported in the literature for different solid Sn-based solders/Ni couples.

The main conclusions of this study can be summarized as follows:

- A thin Ni_3Sn_4 layer about 0.12 µm thick is formed by solid state interaction between Sn and Ni during fabrication process and/or storage at room temperature.
- The solid Sn-Ni interactions during the heating of Sn-based solders, with classical heating rates ($\approx$ 60°C.min^{-1}) from the room to the melting temperature, are significant and may play a crucial role on the subsequent liquid Sn-Ni interactions during the reflow process.
- A smooth round, scalloped shape Ni_3Sn_4 IMC layer is observed for shorter interaction times while for longer times (t $>$ 1 hour) this morphology is gradually transformed to a

facetted growth morphology.

- For reaction times shorter than about 4 hrs, the growth kinetics of the Ni_3Sn_4 layer, follows almost a cubic growth law and the apparent activation energy for solid-solid Ni_3Sn_4 formation was evaluated to be of about 53 $kJ.mol^{-1}$. After 1 day of reaction at 200°C, the growth exponent n slightly shifted from 0.33 to 0.36.
- It was found that for most of the annealing time (or for lower temperature and shorter time) the layer growth is only controlled by grain coarsening, except at higher temperature and longer time where new nucleated grains also contribute to the layer thickness.
- A theoretical thermodynamic and kinetic analysis of the initial formation and growth of Ni_3Sn_4 phase at the solid Sn/Ni interface is presented. Based on this analysis and our experimental results, it was concluded that the rate controlling step of the Ni_3Sn_4 growth, for reaction times shorter than 4 hours, is the grain boundary diffusion process.
- A simple model for evaluation of the grain boundary diffusivity in Ni_3Sn_4 compound is proposed. The integrated diffusion coefficient in the Ni_3Sn_4 grain boundaries was evaluated to be between about 10^{-16} to $4x10^{-14}$ $m^2.s^{-1}$ and the averaged diffusivities 10^{-17} to $7x10^{-15}$ $m^2.s^{-1}$.
- The formation and growth of Ni_3Sn_2 phase was observed for the first time in the solid Sn/Ni system, after 4 days of reaction at 200°C. The formation of Ni_3Sn_2 phase could be possible only if the thickness of the "vampire" Ni_3Sn_4 phase is higher than about 2 μm.

3.4 Study of interfacial interactions between liquid Sn and Ni at 230-350°C

After studying the solid state reactions between Ni and Sn, the interfacial reactions between liquid Sn and Ni are studied at 230-350°C. For this study *test vehicle 3* is used, i.e. diameter of the bump d_3 = 150 µm and height of the bump h_3 = 10-20 µm. As mentioned before, for this test vehicle, the interfacial layer (IMC) is already formed after deposition and its thickness is equal to 250 nm.

3.4.1 Experimental results for liquid Sn-Ag/solid Ni interactions

Figure 3.31 gives a general view of a sample after an isothermal holding for 1 minute at 300°C. This Figure shows that a reaction layer about 1 µm thick is formed all over the Ni/Sn-Ag interface. The average thickness of this layer is practically same everywhere at the interface except the extremities of the sample. It is important to note that after melting, the liquid alloy wets very well the solid Ni (reactive wetting). The contact angle of liquid Sn based alloys on Ni surface is very low (about 20-30°) [132, 133] and the alloy surface forms a spherical cap on Ni surface.

Figure 3.32 gives some representative SEM micrographs of the reaction product formed at the Ni/liquid Sn-Ag interface for the samples which were aged at 230 to 350°C for 1, 2, 4 and 15 minutes. EBSD analysis confirmed that the IMC formed at the interface is Ni_3Sn_4 phase (43±5 at% Ni and 57±5 at% Sn) as shown in Figure 3.33. This results is in agreement with numerous studies which reported that Ni_3Sn_4 phase is the only phase that forms and grows at the Ni/liquid Sn interface for temperatures lower than 350°C [63].

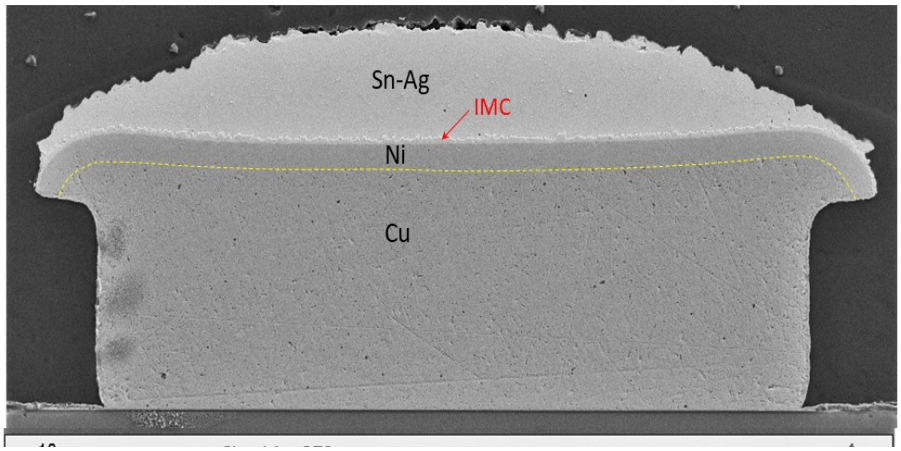


Figure 3.31: General view of a sample after an isothermal holding for 1 minute at 300°C showing the formation of a reaction layer about 1 µm thick all over the Ni/Sn-Ag interface

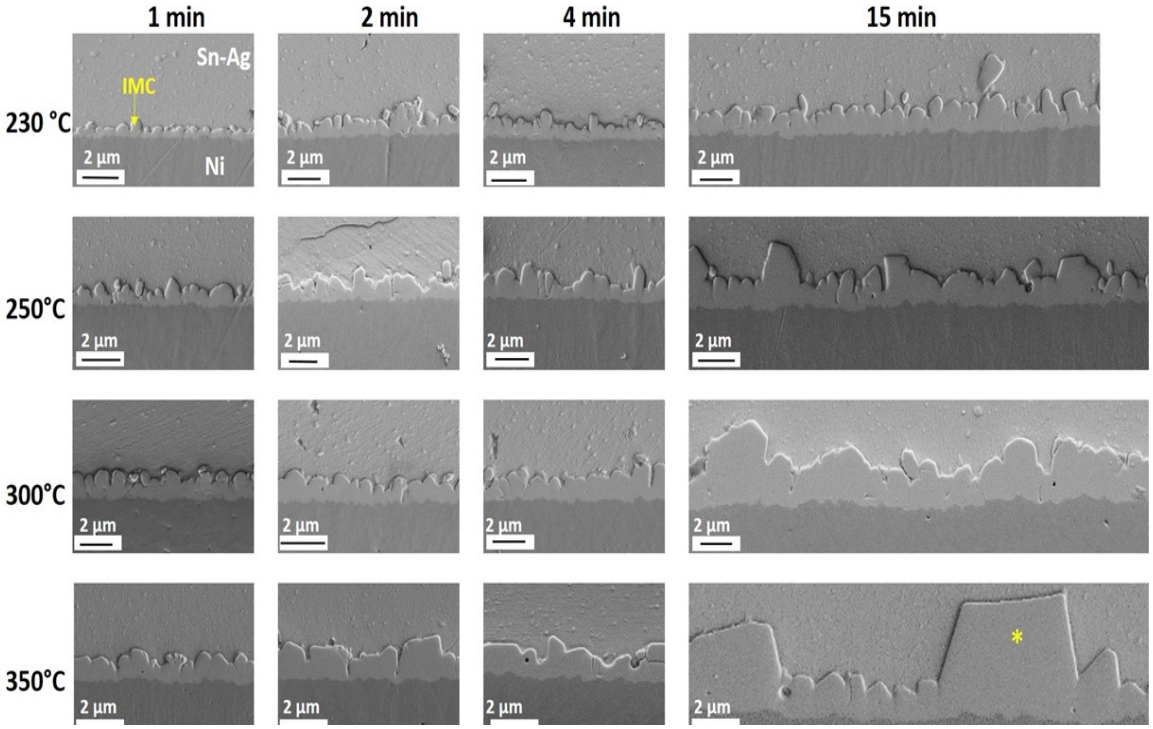


Figure 3.32: SEM micrographs of the reaction product formed at the Ni/liquid Sn-Ag interface for the samples which were aged at 230 to 350°C for 1, 2, 4 and 15 mins

It is important to note that the interfacial IMC layer exhibits an almost scallop-shaped morphology for various annealing temperature up to 300°C which is contradictory to what was reported previously. It is interesting that most of the previous studies reported different morphologies of IMC growth and one of the main differences between their experimental setup was the preparation of diffusion couple. Elongated rod-like shape morphology of IMC was achieved with sessile drop method [89], long, thin, idiomorphic whiskers IMC grew from the diffusion couple which were prepared by sputtering of Ni/Sn [47] and elongated rod-like shape IMC formed when diffusion couple were fabricated by electrochemical deposition [90]. In Section 3.4.2, we will discuss the reason(s) that could lead to this significant difference in the morphology of the interfacial Ni_3Sn_4 layer during the first stage of interaction.

Note that the morphology of the Ni_3Sn_4 layer formed at the early stage of the Ni/liquid Sn-Ag reaction, seems to be similar to the very well-known morphology of the Cu_6Sn_5 layer formed at the Cu/Sn based liquid alloys [133–136]. When the reaction time increases from 1 to 15 mins both the width (w) and the height (h) of the scallops increase and the average ratio ρ = h/w remains lower than about 2. This is slightly lower than the mean value of ρ =2.8±0.3 determined by [136] for the scallop-shape Cu_6Sn_5 layer formed at the Cu/liquid Sn interface. To the best of our knowledge, one alone study in the literature [98] has reported a scalloped-form morphology of Ni_3Sn_4 layer for the early-stages of Ni/liquid Sn reaction (reaction time < 5 minutes). It is worth mentioning that Ghosh et al. [98] have prepared the diffusion couple not by electrochemical deposition (as in our work) but by the sessile drop method of Sn-3.5wt%Ag on an electroplated Cu/Ni/NiPd/***1-3µm Ni/75nm Pd*** (at 230-290°C, for reaction time 0.5-5 mins).

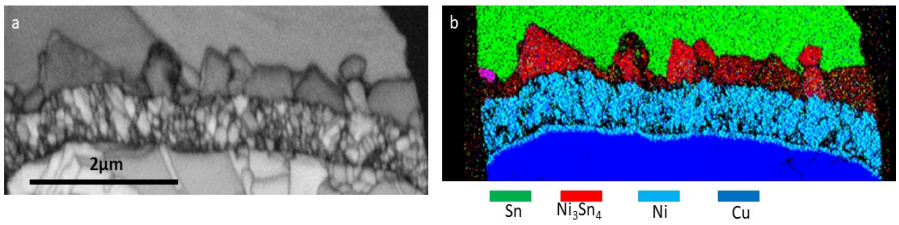


Figure 3.33: EBSD analysis for pillars after annealing at 250°C for 1 min

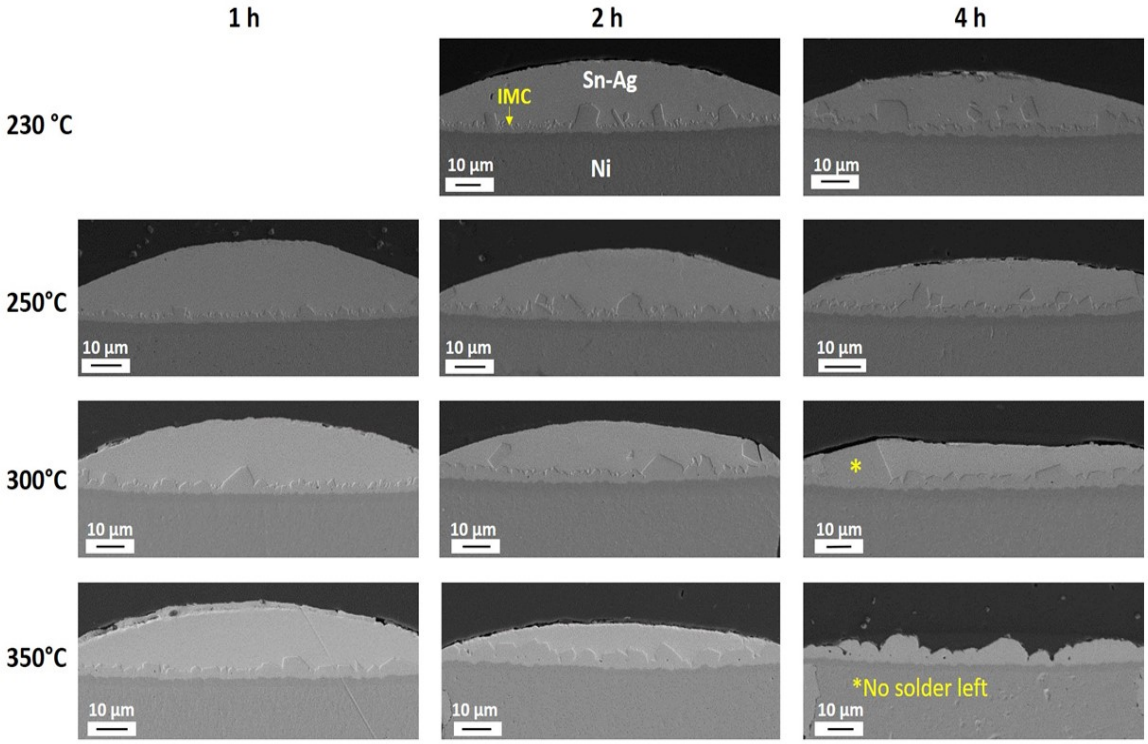


Figure 3.34: SEM micrographs of the reaction product formed at the Ni/liquid Sn-Ag interface for the samples which were aged at 230 to 350°C for 1, 2, and 4 hrs

When the reaction time increases up 1 hrs and more or when the temperature increases up to 350°C, a significant change in the morphology of the reaction layer is observed: the scalloped-form morphology is progressively replaced by large faceted crystals. This can be clearly seen in Figure 3.32 for T = 350°C and in Figure 3.34. These results clearly indicate that an abnormal growth of Ni_3Sn_4 crystals occurs when the reaction time increases for a given temperature and/or when the experimental temperature increases for a given reaction time. For example, in the sample T = 350°C, 15 mins (Figure 3.32), the big crystal (noted *) has a trapezoidal form in the cross-section plan with large bases length ($\sim$ 8 and 6 µm) and large height ($\sim$ 6 µm) compared to the average thickness of the reaction layer ($\sim$ 2.7 µm) measured along 150 µm of the interface. In the sample T = 300°C, 4hrs (Figure 3.34), the growth of the large crystal (noted *) is so rapid, compared to other crystals, that the top of the crystal reaches the liquid surface even before the end of the experiment. This result is in good agreement with the findings of Kim at al [137] who reported an abnormal growth of Ni_3Sn_4 crystals during Ni/liquid Sn-3.5Ag alloy at 250°C after 1 hr of interaction. In their study, these authors explain the relation between the IMC morphology and the Jakson's parameter [138].

Note that in the sample at T = 350°C, 4hrs, all the solder is consumed thus the average thickness of the reaction layer is lower than the thickness of the layer that would be formed if some solder was left.

At this stage, it is interesting to compare the thickness *(e)* and the morphology of the IMC layer obtained after 1 min of annealing at 210°C (**solid** Sn-Ag/Ni), Figure 3.10 and 230°C (**liquid** Sn-Ag/Ni), Figure 3.32. For the solid state, the IMC thickness increases from 0.12 to 0.47 µm, whereas for liquid state interaction it increases from 0.25 to 0.67 µm. The thickening of the IMC layer is significantly higher for the liquid Sn-Ag interaction (0.47 µm) as compared to the solid Sn-Ag interaction (0.35 µm), which seems to be evident given the higher experimental temperature. Nevertheless, the morphology of the reaction layer seems to be different: while the scallop-shaped morphology appears more regular for the liquid Sn-Ag with round and smooth surfaces, a tendency of facetted morphology seems to appear in the case of solid Sn-Ag.

3.4.2 Analysis of Ni_3Sn_4 growth at the early-stage reaction at liquid Sn/solid Ni interface

The particular scallop-form morphology exhibited by the Ni_3Sn_4 layer could be attributed to the fact that, in our study, a thin and continuous Ni_3Sn_4 layer $\sim$ 0.25 µm thick is already formed at the Ni/Sn-Ag interface by solid state reaction (see Figure 3.4) during fabrication process and/or storage. It is imperative to point out that this result is not in agreement with the recent results of Lis et al. [90] who reported that no intermetallic compound is present at the interface between electroplated 15 µm Ni and 17 µm Sn layers (see Figure 1.38).

Thus in our case, when the Sn-Ag alloy is brought to the liquid state, this liquid is not in direct contact with the solid Ni but with the interfacial thin Ni_3Sn_4 layer already formed. For this reason, in the following we will first analyse two cases of nucleation and/or growth of Ni_3Sn_4 phase at Ni/liquid Sn interface when liquid Sn is:

1. In direct contact with solid Ni and IMC is being formed as a reaction layer between the diffusion couple.

2. Not in direct contact with solid Ni due to the pre-existing IMC between the diffusion couple which was formed at the time of fabrication/storage.

Afterwards, we will compare our results with the literature and discuss the growth kinetics of Ni_3Sn_4 layer during the early-stage of the reaction ($<$ 4-5 minutes).

From a general point of view, the first phase which will form by heterogeneous nucleation at Ni/Sn interface will be the phase with the lower nucleation energy barrier. However, given the fact that the interfacial energies of the possible phases during nucleation are not known, it is very difficult to predict which phase forms first at the interface. As it is shown by the equilibrium phase diagram of the binary Ni-Sn system (Figure 3.16), the stable phases that can be formed at Ni/Sn interface are Ni_3Sn, Ni_3Sn_2 and Ni_3Sn_4. It has been demonstrated by numerous studies that, for temperatures lower than 350°C, the only phase that forms and grows at the Ni/Sn interface is the Ni_3Sn_4 phase, therefore we will consider only Ni_3Sn_4 phase formation for this study.

The liquid Sn is in direct contact with the solid Ni

If the liquid Sn is put in direct contact with solid Ni (as it was the case in dipping [96] or sessile drop experiments [89], the interfacial interaction starts with the very fast dissolution of solid Ni in liquid Sn. At this stage, we assume that the solid Ni/liquid Sn interface is at metastable equilibrium as long as no reaction phase is formed at this interface. Ni diffusion concentration profile through the liquid alloy is then established (see Figure 3.35 (a)).

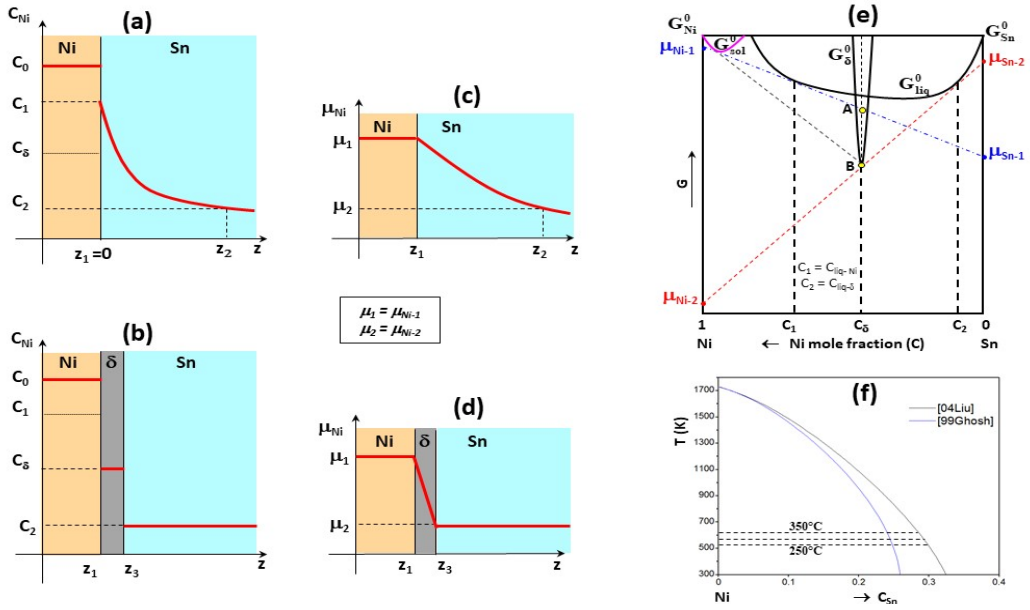


Figure 3.35: Schematic presentation of variation of Ni concentration (a, b) and Ni chemical potential (c, d) through the Ni/liquid Sn interface showing the first instant of contact (metastable equilibria between Ni and liquid Sn (a, c) and the formation of the δ-Ni_3Sn_4 phase at the interface (b, d). Schematic presentation of variation of the Gibbs free energy formation of (Sn,Ni) liquid phase, (Ni,Sn) solid phase and δ-Ni_3Sn_4 compound at T > 232°C indicating the stable (—) and metastable (- - -) equilibria as well as the chemical potentials of Ni and Sn corresponding to these equilibria (e). Variation with the temperature of the concentration of Ni in liquid Sn at the metastable Ni/liquid Sn equilibrium (f) calculated by CALPHAD modelling of the binary Ni-Sn system using data from Gosh et al. [125] and Liu et al [126]

The concentration of Ni at the interface is given by $C_1 = C_{liq\text{-}Ni}$ (Figure 3.35 (a, c)) which is corresponding to the metastable equilibrium between liquid Sn and solid Ni. $C_2 = C_{liq\text{-}\delta}$ represents the concentration of Ni in liquid alloy in equilibrium with δ-Ni_3Sn_4 phase. The corresponding chemical potentials of Ni are indicated by μ_1 and μ_2 respectively in Figure 3.35 (c, e)

Figure 3.35 (e) gives a schematic presentation of the variation of the Ni molar fraction (C) with the Gibbs free energy of formation (G) of the (Sn,Ni) liquid phase, (Ni,Sn) solid phase and δ-Ni_3Sn_4 compound indicating the stable and metastable equilibria. (As it is already mentioned above, the Ni_3Sn and Ni_3Sn_2 phases are not taken into account in Figure 3.35). Figure 3.35 (e) shows in particular the metastable equilibria at the solid/liquid interface and the stable δ-Ni_3Sn_4/liquid equilibria as well as the corresponding chemical potentials of Ni and Sn.

Table 3.6: Molar fraction of Ni in liquid Sn in equilibrium with Ni_3Sn_4 phase (stable equilibrium, C = C_2) and in equilibrium with solid Ni (metastable equilibrium, C = C_1) at 250, 300 and 350°C. Values obtained from CALPHAD modelling of the binary Ni-Sn system using data from Liu et al. [126] and Gosh [125].

	250°C	300°C	350°C	Ref.
Molar fraction of Ni in the liquid in equilibrium with Ni_3Sn_4 phase (stable equilibrium) : C_2	$3.75.10^{-3}$ $2.10.10^{-3}$	$5.84.10^{-3}$ $3.68.10^{-3}$	$8.71.10^{-3}$ $5.96.10^{-3}$	[117] [126]
Molar fraction of Ni in equilibrium with solid Ni in the liquid (metastable equilibrium) : C_1	0.748 0.697	0.754 0.706	0.759 0.714	[125] [126]
Degree of supersaturation in Ni : $s = C_1/C_2$	200 332	129 192	87 120	[125] [126]

To qualify the stable and metastable equilibria concentrations, we rely on a CALPHAD modelling of the binary Ni-Sn system published by Gosh et al. [125] and Liu et al. [125]. Given the fact that the diffusion coefficient of Ni in solid Sn at 350°C is extremely low ($D_{sol} \approx 7.10^{-24}$ $m^2.s^{-1}$ [139]), several order of magnitude lower than that of Ni in the liquid Sn ($D_{liq} = 5.10^{-9}$ $m^2.s^{-1}$ [121]), therefore, we assume that there is no diffusion between solid Sn and Ni and immediately after the melting of Sn (t<1 s), the concentration of Ni in the liquid at the liquid/Ni interface reaches to the concentration value C_1 corresponding to the metastable equilibrium.

The variation of C_1 with the temperature is plotted in Figure 3.35 (f) and the calculated values of C_1 and C_2 at T = 250-350°C are given in Table 3.6. This table shows that in the 250-350°C temperature range $C_2 \sim 0.7 > C_{Ni_3Sn_4} = C_\delta = 4/7 \approx 0.43 >> C_1 \sim 10^{-3}$ to 10^{-2} and the calculated values of C_2 are in good agreement with experimental ones reported in Ref. [140].

As long as no reaction phase is formed at the Ni/liquid alloy interface, the variation of the Ni concentration (C) with the time t and the distance z from this interface (i.e., diffusion in a semi-infinite medium), is given by the following relation [141]:

$$C(z) = C_1\{1 - erf(z/2\sqrt{Dt})\} \tag{3.25}$$

where erf is the error function and D is the diffusion coefficient of Ni in the liquid phase .

As it is shown by the Figure 3.35, the driving force of formation of δ-Ni_3Sn_4 phase from reaction of solid Ni and the metastable liquid Sn is given by the segment BA. Under these conditions, after some diffusion time, the nucleation and growth of δ-Ni_3Sn_4 in the supersaturated liquid alloy become thermodynamically possible.

Note that the liquid close to the interface is extremely supersaturated with Ni, i.e. the ratio $s = C_1/C_2$ = 90 to 330 is much higher than 1 - see Table 3.6 (where $C_1 = C_{liq\text{-}Ni}$ and $C_2 = C_{liq\text{-}\delta}$). Let *d* be the distance at which the Ni concentration (C_d) is equal to the half of that at the Ni/liquid interface, i.e. $C_d = C_1/2$. By taking the diffusion coefficient of Ni in liquid Sn at T = 250°C: D = 3x10^{-9} $m^2.s^{-1}$ [121] and typical time scale of nucleation t = 10^{-2} to 1 s [142], a simple diffusion calculation based on Eq. 3.25 leads to values of *d* varying from 6 to 60 µm approximately.

Thus, a large zone of the liquid phase, some tens of micrometres in width, can be subject to *extremely high supersaturation* (in relation to the formation of Ni_3Sn_4 compound). Under these

conditions, the growth of Ni_3Sn_4 phase from the supersaturated Sn-Ni liquid solution can lead to the formation of elongated and facetted needles or rod-like shape or long and thin whiskers of Ni_3Sn_4 as it was observed experimentally in Refs. [47, 89, 90] respectively.

A thin IMC layer is formed at the interface by solid state reaction before Sn melting

Let's consider the second case when a thin and continuous layer of Ni_3Sn_4 pre-existed between Ni and Sn - the case of this study (see Figure 3.3 (b) and Figure 3.35 (b),(d)). In this case, as soon as Sn in brought in the liquid state, a competition between two processes occurs: (i) dissolution of the Ni_3Sn_4 layer in the liquid Sn (which is not saturated with Ni) and (ii) growth of Ni_3Sn_4 layer by interdiffusion process through this layer.

The general equations describing the effect of dissolution on the growth rate of a chemical compound layer are described in detail in Ref. [142]. However, the description of the evolution of such a system depends, among other thermodynamic and kinetic factors, on the dissolution rate constant k_d of reaction compound on the liquid alloy. Unfortunately, data for k_d are very rare in literature and cannot be estimated by theoretical models making thus difficult the description of the theoretical evolution of such systems [142].

Note however that in our case we can easily verify if, from a thermodynamic point of view, a layer of Ni_3Sn_4 compound of initial thickness $e^o{}_{Ni_3Sn_4}$ can completely dissolve (or not) in a liquid Sn layer of initial thickness $e^o{}_{Sn} >> e^o{}_{Ni_3Sn_4}$. This can be verified by performing a mass balance for the nickel. Indeed, knowing the density of Ni, liquid Sn and Ni_3Sn_4: ρ_{Ni} = 8.90 g.cm^{-3}, ρ_{Sn} = 7.00 g.cm $^{-3}$ and $\rho_{Ni_3Sn_4}$ = 8.65 g.cm $^{-3}$ [143], one can easily calculate that, the total dissolution of the Ni_3Sn_4 layer in liquid Sn leads to a final molar fraction of Ni (C_{Ni}) in liquid Sn given by Eq. 3.26 :

$$C_{Ni} = 0.68 \frac{e^o_{Ni_3Sn_4}}{e^o_{Sn}} \tag{3.26}$$

The application of Eq. 3.26 with $e^o{}_{Ni_3Sn_4}$=0.25 µm and $e^o{}_{Sn}$=20 µm leads to an average Ni concentration in liquid Sn: $C_{Ni} \approx 0.009$. This value is higher than the solubility limit of Ni in liquid Sn (C_2) in the 230-350°C temperature range (see Table 3.6). Thus, if a Ni_3Sn_4 layer of 0.25 µm thick is put in contact with a Sn layer of 20 µm thick at 230-350°C, the final equilibrium state of the system consists of a saturated liquid Sn with Ni in equilibrium with a thin Ni_3Sn_4 remaining layer. Due to the Ni_3Sn_4 layer between Ni and liquid, the contribution of Ni to the thickening of Ni_3Sn_4 layer is by reactive diffusion.

We can thus conclude that in our case, the initial layer of Ni_3Sn_4, formed at Ni/Sn interface by solid state reaction during electrodeposition and/or storage, do not dissolve completely in the early-stage of reaction at the Ni/liquid Sn interface. Thus, the direct contact of Ni with liquid Sn is avoided and the growth of Ni_3Sn_4 layer will take place by interdiffusion through the initial Ni_3Sn_4 layer leading thus to a scallop-form morphology of Ni_3Sn_4 layer during the early-stage of Ni/liquid Sn reaction (see Figure 3.32).

3.4.3 Comparison with other studies of the early-stage growth kinetics of Ni_3Sn_4 layer

In this section we will discuss the growth kinetics of Ni_3Sn_4 layer during the early-stage reaction (t< 4-5 minutes) and compare our results with the literature ones.

In our study, the average thickness *(e)* of Ni_3Sn_4 layer after 4 mins of reaction at 250°C is about 1.1 µm. This value is much lower than that reported by Gorlich et al. [89] (5.9 µm) and by Lis et al. [90] ($\sim$ 2 µm after 3 minutes of reaction). As it is already discussed before, the scallop-form morphology of the reaction layer obtained in this study is very different from those obtained in Refs. [89, 90] (elongated and facetted needles or rod-like shape morphology). This drastic change in the morphology of the reaction layer can lead to a significant change on the growth kinetics of this layer and especially if it is limited by the grain boundary diffusion through this layer (as it will be discussed in Section 3.4.4).

The value of e = 1.1 µm is in good agreement with that reported by Ghosh [98] (0.9 µm at 260°C for 5 min) who observed also a scallop-form morphology of Ni_3Sn_4 layer. It is very interesting to note that Ghosh performed diffusion couples by using a Pd layer 75 nm thick deposited between electroplated Ni and Sn. It is of course difficult to predict in what extent the Pd layer influences the initial stages of interactions between Ni and liquid Sn. However, given the experimental results of Ghosh that are similar to ours, it can be assumed that Pd layer prevents the direct contact between Ni and liquid Sn all over the interface until a continuous layer of Ni_3Sn_4 IMC is formed at this interface which is scallop-form similar to our observations. These results strongly suggest that the initial stage of the Ni/Sn interface could play an important role on the initial state of the reaction kinetics at the liquid Sn/Ni interface.

The formation of very elongated Ni_3Sn_4 needles at the first stages of reaction could be a very serious issue while using Ni as a direct contact with the liquid Sn based solder and especially for fine pitch assembly. For example, in the system with fine pitch assembly with Ni/Sn/Ni diffusion couples where the needle shaped IMC is formed with thickness let's say h, (from one diffusion couple) and the available solder thickness is slightly above 2h, then due to the IMC growth as reported Ref. [89, 90], the IMCs will come in contact at some discreet points. This will form a mesh of Ni_3Sn_4 IMCs inside the melt. On aging, the Sn in between the mesh will be consumed through the reaction with Ni and this will lead to a net deficit of material within the mesh, ultimately leading to void formation near the bond mid-plane (see for example Ref. [100]).

Thus, if a continuous and sufficiently thick Ni_3Sn_4 layer is already formed at the Ni/Sn interface by solid state reaction (see Figure 3.4 (b)) during fabrication process and/or storage then the growth of this layer occurs by solid state and/or grain boundary diffusion which prevents formation of elongated and facetted needles or rod-like shape morphology during the initial stages of interfacial reaction.

3.4.4 Growth kinetics of Ni_3Sn_4 layer

For each sample, the average thickness e of the Ni_3Sn_4 layer is calculated using Image J software (see appendix B). The average values of e from samples used for each holding temperature

and time are given in Table 3.7. In Figure 3.36, the average thickness of each Ni_3Sn_4 layer is plotted against the reaction time. In order to have a better view of the experimental results, they are plotted in two figures, one for the early stage reaction time (up to 4 mins, Figure 3.36 (a)) and the other for reaction time up to 240 mins (Figure 3.36 (b)).

Table 3.7: Average thickness e of the Ni_3Sn_4 layer (in µm) formed at liquid Sn-2wt%Ag alloy/solid Ni interface for different holding temperatures and reaction times. *Sn is completely consumed before 240 mins of reaction

Time (min)	**1**	**2**	**4**	**16**	**60**	**120**	**240**
230°C	0.72	0.88	0.98	1.39		3.51	4.27
250°C	0.78	1.10	1.14	1.74	3.02	4.25	4.87
300°C	1.19	1.21	1.41	2.32	3.50	5.41	5.87
350°C	1.29	1.44	1.60	2.72	3.91	5.64	$>$ 6.67*

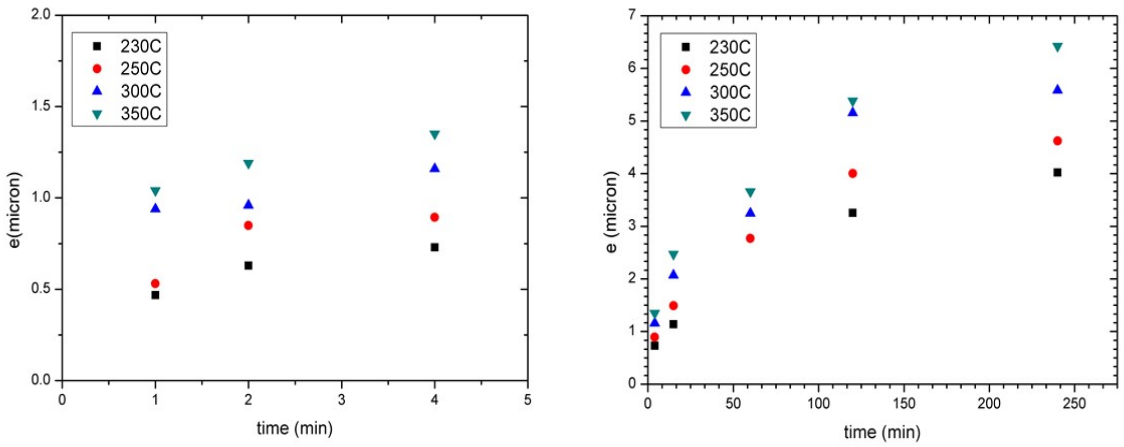


Figure 3.36: Average thickness of Ni_3Sn_4 layer (e) formed at the Ni/liquid Sn-Ag interface versus reaction time at 230, 250, 300 and 350°C

In the following we assume that the growth kinetics of the Ni_3Sn_4 layer obeys to the classical power law very often used in the literature:

$$\Delta e = e - e^o = kt^n \tag{3.27}$$

where e_0 and e are the thickness of the layer at time t = 0 and t respectively (in our case e_0 = 0.25 µm) is a growth exponent and k the kinetic growth coefficient.

This representation is in relation to the fact that the mechanism of the Ni_3Sn_4 phase growth in Ni/liquid Sn system is still under discussion. Indeed, the most popular candidates for the power law of Ni_3Sn_4 phase growth kinetics in the literature are 1/2 and 1/3 [51, 89, 90, 92, 93].

Table 3.8: Calculated values of the kinetic growth constant (k) of Ni_3Sn_4 layer at liquid Sn-2wt%Ag alloy/solid Ni interface and of growth exponent n (see Eq 3.27) at 230, 250, 300 and 350°C

T(°C)	230°C	250°C	300°C	350°C
n	0.399	0.393	0.359	0.348
k(μm.s^{-n})	0.086	0.111	0.183	0.225

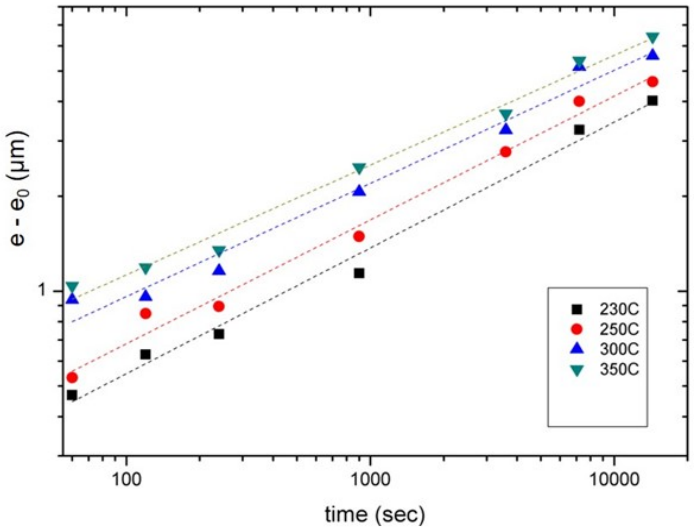


Figure 3.37: Log-log plot of the variation of Δe with the reaction time at 230, 250, 300 and 350°C. $\Delta e = e - e_0$. e and e_0 are the average thickness of Ni_3Sn_4 layer formed at the Ni/liquid Sn-Ag interface at time t = 0 and t respectively, here e_0 = 0.25 μm

Figure 3.37 shows the log Δe versus log t plot of the experimented data. These data are fit with a straight line by linear regression and the obtained values of k and n values are summarized in Table 3.8. The values of n vary between 0.36 and 0.42 and those of k between 0.068 and 0.201 μm.s^{-n}.

The values of n (0.35 to 0.40) are in good agreement with the recent results of Nakane et al. [92] who studied Ni/liquid Sn reaction by isothermal bonding technique (n varying from 0.31 to 0.43 at 260-350°C). However, it is very surprising to note that the values of k obtained in our study (0.08-0.22 μm.s^{-n}) are much lower than those reported by [92] (0.268 μm.s^{-n} at 260°C and 7.18 μm.s^{-n} at 350°C). Thus the thickness of the Ni_3Sn_4 layer observed in our study is systematically about four times lower than that reported in Ref. [92] whatever the experimental temperature (from 260 to 350°C) and the reaction time (from 5 minutes to 4 hours) in Ref. [92]. Note that in Ref. [92] the authors do not discuss in detail the morphology of the reaction layer and only one micrograph of the reaction layer at low magnification is given (T = 260°C, t = 20 min, e ≈ 7 μm, Figure 1 in Ref. [92]). It seems however from this figure that the reaction layer exhibits a scallop-like morphology similar to that obtained in our study.

As it has been clearly demonstrated by Gorlich et al. [89], for experiments in this study as well as for all mentioned experiments reported in the literature, the growth kinetics of Ni_3Sn_4 layer is so rapid that volume transport through the Ni_3Sn_4 layer must be ruled out as a relevant mechanism. Thus the discussion has to focus on the short circuit transport along grain boundary

or nanometric liquid channels between Ni_3Sn_4 grains, leading thus to a rapid growth rate of this layer [89].

The apparent *activation energies (Q)* of the Ni_3Sn_4 layer growth is calculated using the Arrhenius relationship *(k(T) = k_0.exp(-Q/RT))* for temperatures ranging from 230 to 350°C (see Figure 3.38, where k_0 is the growth constant of Ni_3Sn_4 layer. *Q* is evaluated from the slope of the log(k) versus *1/T* plot using a linear regression analysis giving: Q = 20.9 ± 3.9 kJ mol_{-1}. This result is in agreement with the values of Q reported in Refs. [63, 91, 92].

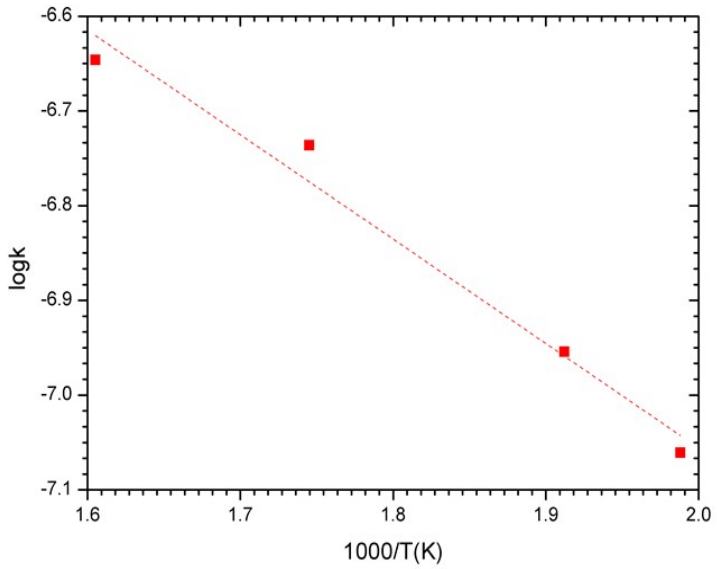


Figure 3.38: Arrhenius plot of Ni_3Sn_4 reaction product growth in Sn-2wt%Ag liquid alloy/solid Ni system logk = f(1/T). k is the growth constant of Ni_3Sn_4 layer in $m.s^{-n}$ ($e = k.t^n$). e is the layer thickness and t the reaction time.

The value of Q reported in this study ($\simeq 20$ kJ.mol^{-1}), is much lower than the activation energies of diffusion process in the bulk intermetallics ($>$ 100 kJ.mol^{-1} [123]) This result, strongly suggests once again that the growth kinetics of the Ni_3Sn_4 layer is not limited by the bulk solid state diffusion through this layer. Owing to the lack of data for activation energy of the grain boundary diffusion in Ni_3Sn_4 IMC it is hard to affirm if the growth kinetics of Ni_3Sn_4 layer may be limited by the grain boundary diffusion. The activation energy of the grain boundary diffusion in pure Ni and pure Sn is about 100-120 and 40-50 kJ.mol^{-1} respectively [123]), which strongly suggests that the activation energy of the grain boundary diffusion through the Ni_3Sn_4 layer should be higher than 50 kJ.mol^{-1}, i.e. twice the experimental value obtained in this study. On the contrary, this value is of the same order of magnitude as the activation energy of diffusion in bulk liquid Sn ($\sim$ 19 kJ.mol^{-1} [139]), thus the growth kinetics of the Ni_3Sn_4 layer could also be limited by the liquid state diffusion through nanometric liquid channels (grain boundaries wetting) as it was suggested for the growth of Cu_6Sn_5 layer in the Cu/liquid Sn system [134, 145]. However, this point is out the scope of this study and more experimental work is needed to determine which is the rate-limiting step during Ni_3Sn_4 growth process.

In general, there is a large discrepancy in the experimental results reported in the literature on the growth kinetics of the Ni_3Sn_4 layer for long time experiments (up to 4 hours). Just to give a general idea: in this study a thickness of Ni_3Sn_4 layer $e \approx 4.9$ µm, at T = 250°C for t =

4h is obtained which is in good agreement with $e \approx 4$ µm (250°C, 4h) [51] and e ≈ 3.5 µm (240°C, 3h) [93]. On the contrary, in other studies much higher thicknesses are reported: $e \approx 68$ µm (250°C, 4h) [89] and $e \approx 16$ µm (260°C, 4h) [92]. This significant difference in the growth kinetics of the Ni_3Sn_4 reaction layer may be due to the microstructure of the reaction layer and in particular to the average grain size. The average grain size of Ni_3Sn_4 layer plays an important role in growth kinetics for both growth mechanism (grain boundary diffusion or liquid state diffusion through nanometric liquid channels) [73, 123]. This average grain size of Ni_3Sn_4 layer can depend on the grain size of as deposited Ni during solid Ni liquid Sn reaction. Moreover, given the fact that the Ni_3Sn_4 reaction layer can also be sometimes formed and grown by solid state reaction during fabrication process and/or storage (as it was observed in this study), the morphology of this layer can depend not only on the microstructure of both Ni substrate but also on the microstructure of the deposited Sn. Thus, from a practical point of view, it is very important to control the microstructure of the Ni substrate and deposited Sn in order to obtain reproducible results.

3.4.5 Conclusions

Interfacial reactions between electrochemical deposited Sn-2wt%Ag alloy and Ni are studied for isothermal holdings at 230-350°C and for various time in order to analyse the initial stages (1 min - 4 mins) and latter stages of reaction (15 min - 4 hrs).

The main conclusions of this study can be summarized as follows:

- A thin Ni_3Sn_4 layer about 0.25 µm thick is formed by solid state interaction between Sn and Ni during fabrication process and/or storage at room temperature.
- For short reaction times (1 - 4 mins) a scallop like morphology with round and smooth surfaces of Ni_3Sn_4 layer is formed at the interface. The average thickness of this layer is about 1 to 1.5 µm after 4 mins of reaction.
- From a practical point of view, it is very important to control the initial stages of Ni/liquid Sn interfacial reaction in order to avoid the formation of elongated needles of Ni_3Sn_4 phase which can strongly affect the integrity of micrometric sized joints.
- For longer reaction times (> 1 h) the scallop-like morphology is transformed gradually to a facetted abnormal growth morphology but not elongated structure. The average thickness of Ni_3Sn_4 layer is about 4 to 7 µm after 4 hrs of reaction.
- The growth kinetics of the Ni_3Sn_4 layer follows a power law with growth exponent n varying from 0.36 to 0.42 and the apparent activation energy for liquid-solid Ni_3Sn_4 formation was evaluated to be of about 20±3.9 $kJ.mol^{-1}$.
- Therefore, the rate controlling step of the growth process can be either the grain boundary diffusion or the liquid state diffusion through nanometric channels inside the Ni_3Sn_4 layer.
- A theoretical analysis of the initial formation and growth of Ni_3Sn_4 phase at the Ni/Sn interface is presented and the role of the Ni/Sn interactions at the solid state during deposition and/or storage on the morphology and the growth kinetics of Ni_3Sn_4 is discussed.

CONCLUSION

In this chapter the initial state of Cu/Ni/Sn-Ag bumps (vehicle tests) was characterized, the melting and solidification of the Ni Sn solder bumps were studied by Differential Scanning Calorimetry (DSC) and the interfacial reactions in both solid Sn/Ni and liquid Sn/Ni systems were studied from experimental and theoretical point of view. The main conclusions of this chapter are:

- Vehicle tests with different diameter bumps (5 and 150 µm) and Sn-Ag alloy height (2 and 10-20 µm) are characterized at their initial stage, just after fabrication before undergoing any thermal treatment. A thin and continuous Ni_3Sn_4 reaction layer is formed by solid state interaction between Sn and Ni during fabrication process and/or storage at room temperature. The thickness of this layer strongly depends on the fabrication process and it varies from 120 to 250 nm.

- The melting and solidification behaviour of Sn-Ag alloy bumps was studied and discussed. The melting of 5 µm diameter bumps occurs at about 222°C indicating that their average composition is not far from the eutectic composition. For the first time, an exothermic peak was observed just after the endothermic melting peak in the case of 5 µm diameter bumps. This exothermic peak was not observed for 150 µm diameter Sn-Ag bumps and it was never reported in the literature neither for Ni/Sn bumps nor for Cu/Sn bumps. This is due to the very small thickness of Sn-Ag alloy ($\sim$ 2 µm) and thus to a rapid and total consumption of liquid Sn by reaction with Ni which is at the origin of the observed exothermic peak.

Short time (1 to 15 mins) solid state interactions, between Sn-2wt%Ag alloy and Ni at 150-210°C, have been investigated for the first time. The latter stages of interactions (0.5-4 hrs and 1-53 days) are also studied in order to compare our results with those reported in the literature for different solid Sn-based solders/Ni couples. The main conclusions of this study can be summarized as follows:

- A smooth round, scalloped shape Ni_3Sn_4 IMC layer is observed for shorter interaction times while for longer times ($t > 1$ hour) this morphology is gradually transformed to a facetted growth morphology.

- For reaction times shorter than about 4 hrs, the growth kinetics of the Ni_3Sn_4 layer, follows almost a cubic growth law and the apparent activation energy for solid-solid Ni_3Sn_4 formation was evaluated to be of about 53 $kJ.mol^{-1}$. After 1 day of reaction at 200°C, the growth exponent n slightly shifted from 0.33 to 0.36.

- It was found that for most of the annealing time (or for lower temperature and shorter time) the layer growth is only controlled by grain coarsening, except at higher temperature and longer time where new nucleated grains also contribute to the layer thickness.

- A theoretical thermodynamic and kinetic analysis of the initial formation and growth of Ni_3Sn_4 phase at the solid Sn/Ni interface is presented. Based on this analysis and our experimental results, it was concluded that the rate controlling step of the Ni_3Sn_4 growth, for reaction times shorter than 4 hours, is the grain boundary diffusion process.

- A simple model for evaluation of the grain boundary diffusivity in Ni_3Sn_4 compound

is proposed. The integrated diffusion coefficient in the Ni_3Sn_4 grain boundaries was evaluated to be between about 10^{-16} to $4x10^{-14}$ $m^2.s^{-1}$ and the averaged diffusivities 10^{-17} to $7x10^{-15}$ $m^2.s^{-1}$.

- The formation and growth of Ni_3Sn_2 phase was observed for the first time in the solid Sn/Ni system, after 4 days of reaction at 200°C. The formation of Ni_3Sn_2 phase could be possible only if the thickness of the "vampire" Ni_3Sn_4 phase is higher than about 2 µm.

Interfacial reactions between electrochemical deposited Sn-2wt%Ag alloy and Ni are studied for isothermal holdings at 230-350°C and for various time in order to analyse the initial stages (1 min - 4 min) and latter stages of reaction (15 min - 4 hrs). The main conclusions of this study can be summarized as follows:

- For short reaction times (1 - 4 mins) a scallop like morphology with round and smooth surfaces of Ni_3Sn_4 layer is formed at the interface. The average thickness of this layer is about 1 to 1.5 µm after 4 mins of reaction.

- From a practical point of view, it is very important to control the initial stages of Ni/liquid Sn interfacial reaction in order to avoid the formation of elongated needles of Ni_3Sn_4 phase which can strongly affect the integrity of micrometric sized joints.

- For longer reaction times ($>$ 1 h) the scallop-like morphology is transformed gradually to a facetted abnormal growth morphology but not elongated structure. The average thickness of Ni_3Sn_4 layer is about 4 to 7 µm after 4 hrs of reaction.

- The growth kinetics of the Ni_3Sn_4 layer follows a power law with growth exponent n varying from 0.36 to 0.42 and the apparent activation energy for liquid-solid Ni_3Sn_4 formation was evaluated to be of about 20±3.9 $kJ.mol^{-1}$.

- Therefore, the rate controlling step of the growth process can be either the grain boundary diffusion or the liquid state diffusion through nanometric channels inside the Ni_3Sn_4 layer.

- A theoretical analysis of the initial formation and growth of Ni_3Sn_4 phase at the Ni/liquid-Sn interface is presented and the role of the Ni/Sn interactions at the solid state during deposition and/or storage on the morphology and the growth kinetics of Ni_3Sn_4 is discussed.

Chapter 4

Interconnects at 10 µm pitch

Contents

INTRODUCTION

The Sn-Ag solder alloy is well studied for larger bump size (> 25 µm). However no studies have been conducted on the behavior of Sn-Ag alloy at small diameters yet. We anticipate that by decreasing the size, we may see some different behaviors which were suppressed/neglected in larger diameter bumps due to their big size.

In the first section of this chapter, the reflow behavior of Sn-Ag alloy for 5 µm diameter micro-bumps is investigated. Following the reflow behavior, assembly process guidelines are laid which is necessary for assembly at 10 µm pitch.

In the next section, different Cu/Sn-Ag alloy based interconnects for the assembly at the pitch of 10 µm are investigated. Traditionally, interconnects joint made of Sn based solder alloys is preferred. However, for 10 µm pitch assembly, the solder thickness is limited, therefore even with the Ni barrier layer, it might not be possible to limit the growth of IMC in the interconnect joint (in Ni/Sn-Ag/Ni system, 3 µm of solder is consumed by within 3 mins of reflow at 250°C as seen in Chapter 3). Therefore, it is difficult to tailor the process to attain Sn interconnect joints (i.e with some solder alloy left at the end of the reflow process), until we change the metallurgy. Changing metallurgy means additional cost on production, therefore it is imperative to investigate intermetallic (IMC) interconnect joints, and answer whether *Ni/Sn IMC interconnects replace the traditional Sn interconnect joints at finer pitch (<10 µm)?* At the best of our knowledge, this type of IMC joint has not been studied in terms of interconnect at micrometric scale.

This is investigated by comparing Ni/Sn **IMC interconnect joint** ($Ni/Ni_3Sn_4/Ni$) with **Sn interconnect joint** (for which some Sn is still left at the end of the joining process). These interconnects are formed by designing two different time-temperature profiles for bonding process. Afterwards, the evolution of metallurgy in these interconnects with thermal aging is evaluated in the temperature range 150-200°C and for aging times up to 1300 hrs.

In the last section, these interconnects are characterized in terms of metallurgy and electrical yield and compared in terms of mechanical properties which are evaluated by both experiments and by theoretical simulations. Finally, the interconnections are tested for reliability which gives information about the lifetime functionality of a package. The assessment of the evolution of metallurgy is done by SEM imaging and testing the electrical resistance of interconnects.

4.1 ASSEMBLY PROCESS

4.1.1 REFLOW BEHAVIOR

As described in chapter 2, after the fabrication of Cu pillars, the reflow is performed. The reflow is a process, where solder pillar converts into solder bump during melting. Usually reflow is performed under nitrogen environment immediately *after etching of Ti seed.* (see Figure 2.18 in Chapter 2). The same practice is tried for 10 µm pitch Cu pillar of 5 µm in diameter. The temperature - time profile used for the reflow process as well as a schematic presentation of the solder pillar to solder bump transformation are shown in Figure 4.1. With this profile and at

these conditions (under N_2), it was not possible to form a solder bump as shown in Figure 4.2 (a). As seen in this figure, the solder pillar has not transformed into solder bump, despite the fact that the Sn alloy has melted and reacted with Ni to form the Ni_3Sn_4 intermetallic at the interface. This could be due to the oxidation of Sn surface during heating and formation of a relatively continuous layer of Sn oxide all over the solder pillar which prevents the formation of a spherical cap (solder bump). Thus in our case to form a bump the reflow process should be performed under reducing environment (under formic acid HCOOH environment). Under those conditions it is well verified that the solder pillar is transformed into a spherical cap (see Figure 4.2 (b)). This result tells us about the importance of the reflow environment.

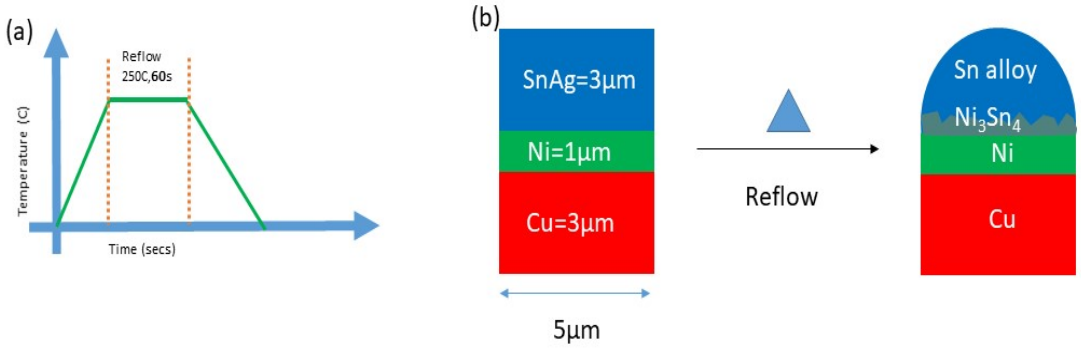


Figure 4.1: (a) Reflow profile no 1 and (b) schematics for reflow

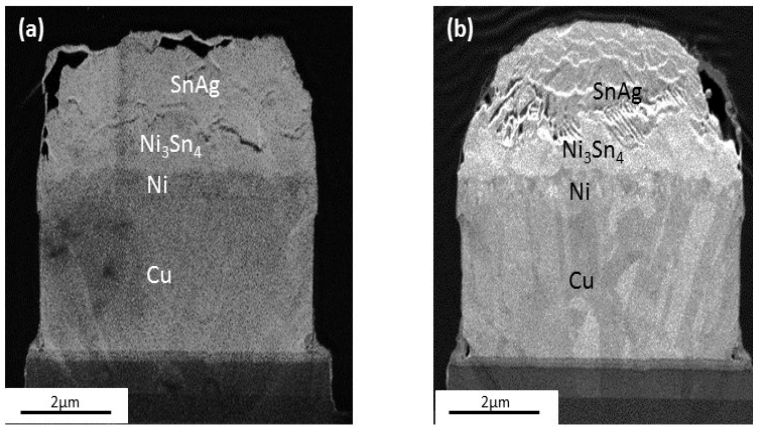


Figure 4.2: SEM image of Cu pillar of 5 µm diameter with seed etching after reflow with profile No. 1 in (a) inert atmosphere and (b) formic acid atmosphere

However, in some other reflow processes that we performed *without seed etching* and in inert atmosphere (N_2), we noted that the solder alloy took a spherical shape as it is shown in Figure 4.3. This means that under N_2 atmosphere, the oxidation of Sn surface does not prevent the formation of a sphere cap during the reflow process.

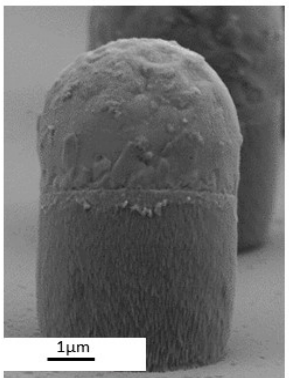


Figure 4.3: SEM images of the bumps without seed etching reflowed at 250°C for 1 min (profile no. 1), in inert atmosphere (N_2)

This surprising result, strongly suggests that the seed etching process must have influenced the physicochemistry of Sn-Ag alloy surface. We recall that traditionally the Ti seed layer is etched with HF acid, then reflow is performed. However, in our case, the Ti layer has been etched with sulfur-hexaflouride (SF_6) plasma. While performing Ti etching with SF_6 plasma, the surface Sn oxide (SnO_x) can react with SF_6 plasma also. According to [146], SF_6 can decompose and lead to the formation of F_y species according to the reaction:

$$SF_6 \longrightarrow SF_{6-y} + F_y$$

and F_y react with Sn oxide leading to the formation of solid Sn oxyfluoride compound (SnO_xF_y):

$$SnO_x + F_y \longrightarrow SnO_xF_y$$

Normally the SF_6 makes the surface of Sn, oxide free and has been used recently as an alternative to liquid flux. However, the SF_6 plasma used in this case has different power and thus different energy. For Ti etching, higher power is needed than Sn de-oxidation and also some by-products are formed during the etching, which may not get properly cleaned. Thus, the reason(s) why a solder bump is not formed during reflow under N_2 atmosphere, when a SF_6 plasma is used prior reflow, could be due to the fact, that oxyfluoride layer is thicker and/or may be slightly contaminated.

Experimentally, the SnO_xF_y (and SnO_x) compound can be reduced by using formic acid (HCOOH) according to the reaction:

$$SnO_xF_y + HCOOH \longrightarrow Sn + H_2O + CO_2 + F_2$$

leading, at the reflow temperature, to the formation of liquid Sn and several gaseous species (H_2O + CO_2 + F_2). This leads to the formation of a solder bump (spherical cup) as it was already observed in Figure 4.2 (b).

In other reflow experiments performed *without seed etching* and in reducing atmosphere (liquid flux or gaseous flux (formic acid)), the solder pillar seems to be reflowed perfectly (spherical form) see Figure 4.4. However some ***additional*** (or more prominent) ***formations*** are observed other than the formation of the Sn bump observed in Figure 4.2 (b) (when seed etching was used).

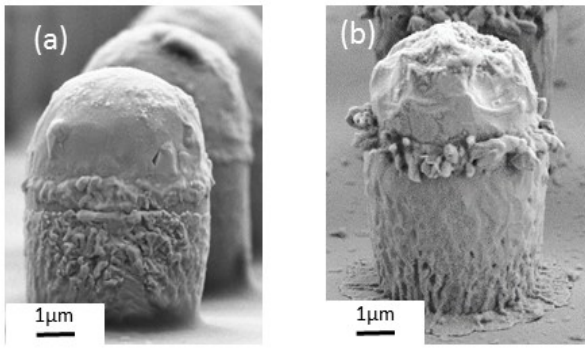


Figure 4.4: SEM images of the bumps without seed etching reflowed at 250°C for 1 min (profile no. 1) in (a) liquid flux (b) gaseous flux (formic acid)

These additional formations, when the pillars with Cu/Ti seed (i.e. *without seed etching)* are reflowed in reducing atmosphere, can be summarized as follows (see Figure 4.5):

Firstly, there is a layer of approximately 1 µm around the Ni barrier, which is called as crown layer. On EDX analysis, this layer is found to be Ni_3Sn_4 IMC layer. The second formation observed is on lateral wall of Cu pillars. The EDX analysis show the layer to be Cu-Sn IMCs. These formations could be due to spilling of solder at the lateral walls of the pillar. Although, these formations are not present when the reflow process is performed with seed etching (Figure 4.2 (b)). The main differences between Cu pillar in Figure 4.2 (b) and Figure 4.5 are that in case of Figure 4.2 (b), the Sn alloy has interacted with SF_6 plasma during Ti seed etching and there is Cu undercut of about 150-250 nm. For further understanding the reason behind spilling of Sn on the lateral side of Cu pillars, more experiments are performed.

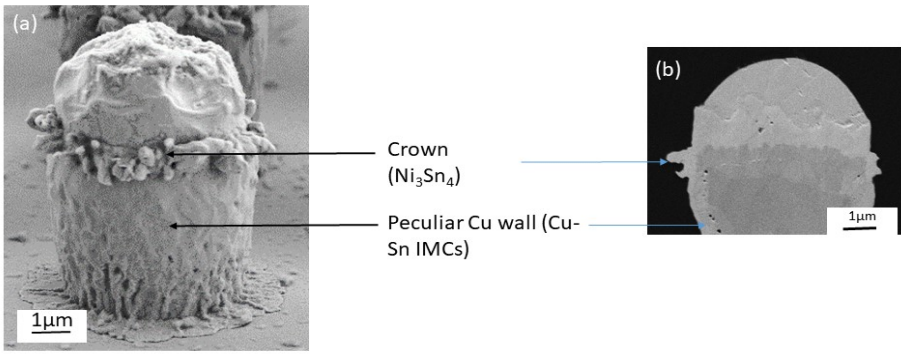


Figure 4.5: SEM micrograph for 5 µm diameter Cu/Ni/Sn-Ag pillar reflowed with profile no. 1 in formic acid without seed etching showing different formations. (a) General view and (b) cross-section

To understand the effect of environment, time and temperature on the formations, a second reflow profile (given in Figure 4.6) is tested under inert and reducing atmosphere. The main difference between this second reflow profile and the previous profile (shown in Figure 4.1) is the introduction of a plateau for 4 mins at 180°C before the melting of Sn. In usual soldering reflow process, an almost plateau in temperature - time profile is present in the bonding cycle for flux activation (Figure 4.7 [147]) which improves the wetting of the metallic pad by the

liquid solder. For simplification, only the results obtain for *Cu pillars* which are *not* Cu/Ti *etched* are presented and discussed.

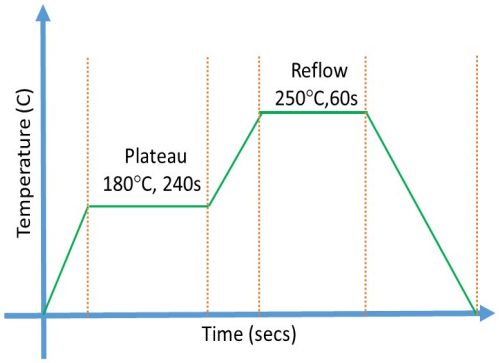


Figure 4.6: Reflow profile no. 2

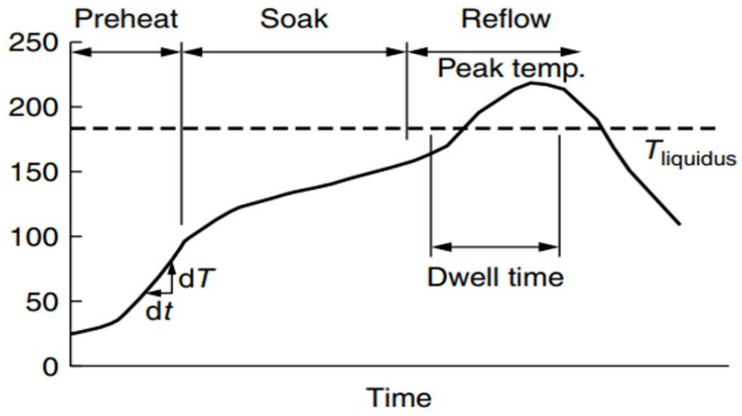


Figure 4.7: Standard reflow profile [147]

SEM micrographs of bumps which are reflowed in *inert atmosphere* (without seed etching) with the reflow profile no. 2 are shown in Figure 4.8. They show some formations such as crown formation and Cu-Sn intermetallics on Cu lateral wall which were not formed by using reflow profile no. 1 in inert (N_2) atmosphere (Figure 4.3). However, in this case, the intermetallic has not covered the entire wall of Cu as it was the case when using the reflow profile no. 1 in reducing atmosphere (Figure 4.4 (b) and Figure 4.5). Nevertheless, this is a surprising result because here, the walls of Cu are not deoxidized as in the case of reducing atmosphere. Moreover, when the time of the plateau at 180°C is varied from 1 to 15 mins, the enhancement of each formation is visible with the increasing time as it is shown in Figure 4.9. This phenomenon could be due to the surface diffusion of Sn atoms towards the Cu pillar walls during the plateau leading to the formation of Cu-Sn IMCs on the Cu lateral walls. In the literature, there are no data on the surface diffusion of Sn on Cu surface. If we use calculated data of surface self-diffusion in Cu at T = 180°C (D $\sim 10^{-12}$ to 10^{-11} $m^2.s^{-1}$ [148]), the surface diffusion length corresponding to a diffusion time of 4 minutes would be 15 to 50 µm, which is much larger than some µm observed in Figure 4.9. Moreover, the increase in the temperature from 453 K (180°C) to 523 K (250°C) would lead to an increase in D by a factor of about 2 to 3 (activation energy of surface self-diffusion Q = 20-30 $kJ.mol^{-1}$ [148, 149]). Thus, from a surface diffusion point of

view, an isothermal holding for 4 mins at 180°C is equivalent to about 1 min at 250°C (which is used for the reflow process). However, lesser wetting on Cu pillar walls is observed after the reflow process (No. 2) under nitrogen atmosphere. One reason for this lesser wetting could be the partially oxidation of Cu pillar walls under nitrogen which, for kinetic reasons, accelerates with the increasing temperature [150]. We can thus assume that at 180°C the lateral walls of Cu pillars are oxidized only partially and covered partially by Cu-Sn IMCs while at 250°C they are oxidized much more preventing thus the formation of Cu-Sn intermetallics on these walls at higher temperatures.

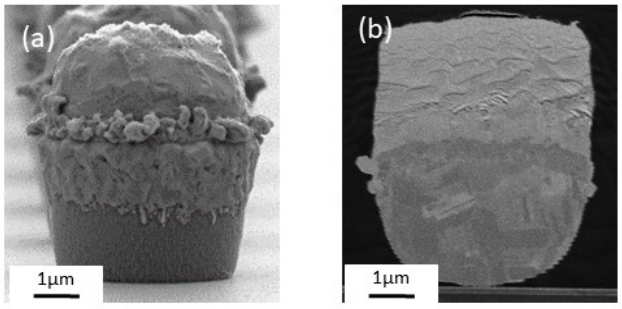


Figure 4.8: SEM image for Cu pillars (without seed etching) reflowed with reflow profile no. 2 in inert atmosphere (a) showing bump and (b) cross-section

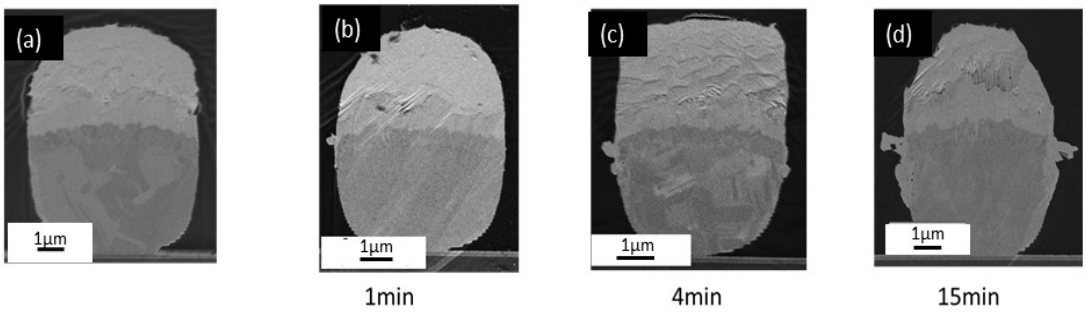


Figure 4.9: SEM images of the bumps reflowed in inert atmosphere (N_2) without seed etching at 250°C for 1 min with a plateau at 180°C for (a) 0 min (profile no. 1), (b) 1 min, (c) 4 mins and (d) 15 mins

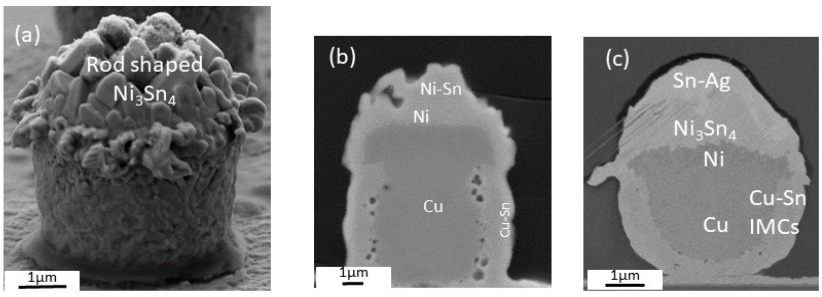


Figure 4.10: SEM images for Cu pillars reflowed with reflow profile no. 2 in reducing atmosphere without seed etching (a) showing Bump with no solder left, (b) cross-section of bump with no solder left and (c) cross-section of bump with some solder left

When the temperature profile no. 2 is applied in *reducing atmosphere* (HCOOH), the Cu bump transformed into a strange looking bump as seen in Figure 4.10. On top of these bumps, there are rods shaped grains, with the presence of crown, i.e. a layer around Ni layer and Cu walls are almost completely converted into Cu-Sn IMCs. The rod shaped grains which are present over the bump are identified as Ni_3Sn_4 intermetallic. This kind of bumps are named as ***Hedgehog Bumps***. If we compare Figure 4.10 (profile no. 2 under HCOOH) with Figure 4.4 (b) (profile no. 1 under HCOOH), we note the same kind of formations which are much more pronounced when profile no. 2 (plateau at 180°C) is used.

These results strongly suggest that the combination of plateau at 180°C with a reducing atmosphere can lead to a covering of Cu pillar surface with Cu-Sn intermetallics. This way, when the solder alloy melts, it will spill almost instantaneously over the lateral walls of Cu pillar by a non-reactive wetting process which is extremely rapid ($\sim$ 1 m.s^{-1}), several orders of magnitude higher than the spreading rate of a reactive-wetting process ($\sim$ 1-10 µm.s^{-1}) [25]. These phenomena could explain why spilling gets enhanced in the reducing environment and in the presence of the plateau in the temperature-time profile.

Sometimes there are some Sn-Ag alloy left (Figure 4.10 (a)) and sometimes almost all the solder is consumed (figure 4.10 (b)) by reaction with both Ni and Cu leading to the metastable (Ni/Ni_3Sn_4) and stable (Cu/Cu_3Sn) equilibrium states. The last case in bonding conditions (see section 4.2) will lead to a TLPB (transient liquid phase bonding) or SLID (solid liquid interdiffusion bonding) process (see Section 4.2.1: Analysis of process B). Thus, it is interesting to characterize both metastable (Ni-Sn system) and stable equilibrium state (Cu-Sn system) obtained in these micrometric systems and to compare them. For this propose X-Ray Microtomography was done, which gives the 3D view of the specimen. The results are shown in Figure 4.11.

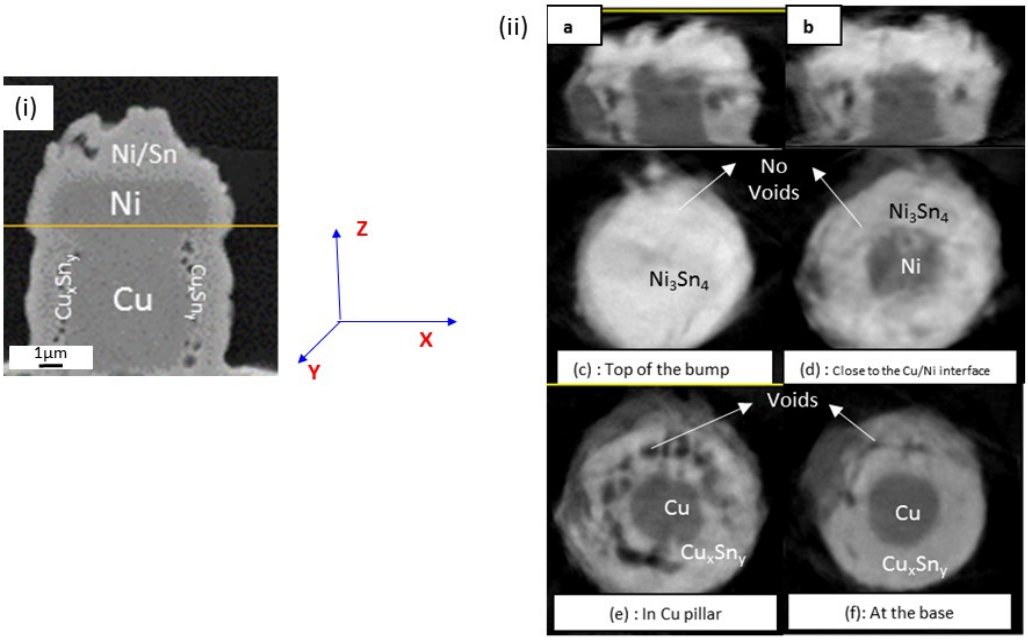


Figure 4.11: (i) SEM image of cross-section of hedgehog bump, (ii) X-Ray tomography for hedgehog bump (a) cross-section at XZ and (b) YZ planes, cross-section at XY planes at (c) top of the bump, (d) at Ni/Cu interface, (e) at Cu pillar and (f) at the base

In this figure, images (a) and (b) show the cross-section of bump at XZ and YZ plane while the other images show the cross-sections in XY plane at different height Z. From the top of the bump till the Ni/IMC interface (images c and d), no voids are observed, while at the Cu pillar level and at the base (images e and f), the bump is full of voids at the edges. These results suggest that during the SLID process, the Ni/Sn system is not prone to voids formation as in the case of Cu/Sn system. However, more tests must be performed for longer time and at higher temperatures in order to conclude on this point.

4.1.2 BONDING

In Chapter 2, the general assembly process was described and the modifications done in the assembly process to achieve 10 µm pitch interconnects are described. The schematic for making an interconnect is presented in Figure 4.12. We recall that *seed etching was always used during preparation of the solder pillar.*

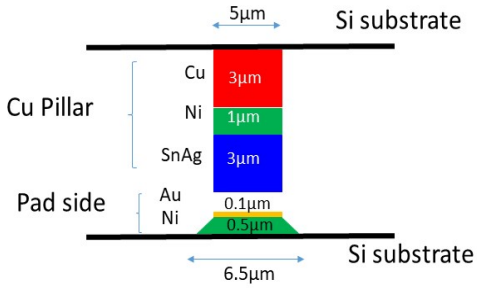


Figure 4.12: Schematics for bonding at 10 µm pitch

There are 2 key points to consider for the bonding process for 10 µm pitch assembly:

Firstly, as shown in the previous section, it is not recommended to do bonding after reflow. This is due to less available quantity of solder for bonding, because during the reflow process Sn could be widely consumed in the formation of intermetallics with Ni. Thus the first consideration for 10 µm pitch is *not to have a prior reflow*, i.e. no formation of bump before bonding. However, this might cause problems with auto alignment and wafer uniformity. Nevertheless, this problem may be compensated with higher precision pick-place tool (like FC300 - see Section 2.2.2, Chapter 2).

The second problem, is the deoxidation of the solder surface. This is done by fluxes, which are weak acids. Normally fluxes are used in liquid state. However more recently the gaseous fluxes like formic acid (boiling point 101°C) are also used, for example during eutectic Au-Sn solder reflow [151]. For larger pitch, the liquid fluxes are used and are successful in achieving assembly. However, as the density of solder bumps increases, as in the case of 10 µm pitch assembly, the effectiveness of liquid flux could be reduced. This could be due to the difficulty of obtaining a homogeneous distribution of the liquid flux all over the whole assembly with small pitch thus leading to partial (or no) wetting for all the bumps. In addition, flux cleaning after assembly is also a serious issue as described in Chapter 1. Therefore, it may now be necessary to use gaseous flux. Nevertheless, for 10 µm pitch assembly, both kind of flux are tested. To test the effectivity of the flux, after bonding, the assembly is broken to observe the

wetting of solder on to the pads. If 100% of pads are wetted by the solder, then the flux is qualified for the bonding. Figure 4.13 shows results for liquid flux and gaseous flux. As seen in this figure, 100% wetting is only achieved for gaseous flux and not for liquid flux. Thus for the assembly at 10 µm pitch, *only gaseous flux (formic acid) is used.*

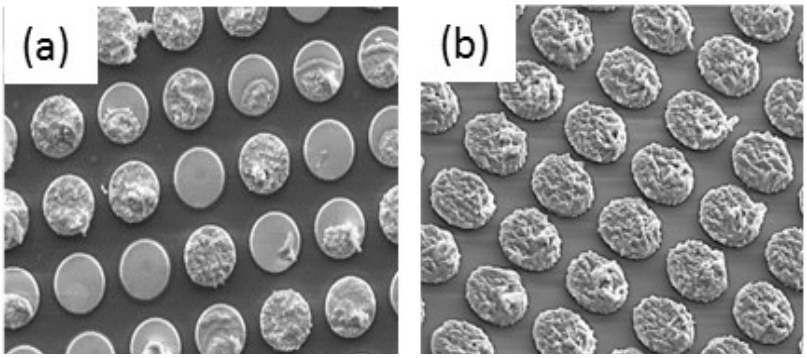


Figure 4.13: Pads after bonding and de-bonding (breaking the assembly) bonding done (a) with liquid flux and (b) with gaseous flux

As described in Chapter 2, the samples used are 3.5mm Si dies, with uniform Cu pillars so that the two dies are without any warpage or CTE mismatch. In addition a very high precision equipment, FC300, with in-situ gaseous flux is used. Therefore the assembly may be achieved with mass reflow. Thus, in this thesis, a focus is given on the metallurgy of the interconnects and its effect on their properties. Therefore, some process adjustments (with temperature and time) are played with to achieve different thickness of IMCs within the interconnect to study their effect on the assembly.

The study of interfacial reactions between Ni and Sn (Chapter 3) is used to design two processes noted A and B. In process A, a minimum bonding time is used just sufficient for wetting of the Au/Ni layer by liquid Sn-Ag alloy at the pad side, whereas in process B, bonding time is long enough for not only wetting of solder with Au/Ni pad but also for Sn to be completely consumed in the formation of intermetallic. The temperature-time profiles for the processes A and B are given in Figure 4.14.

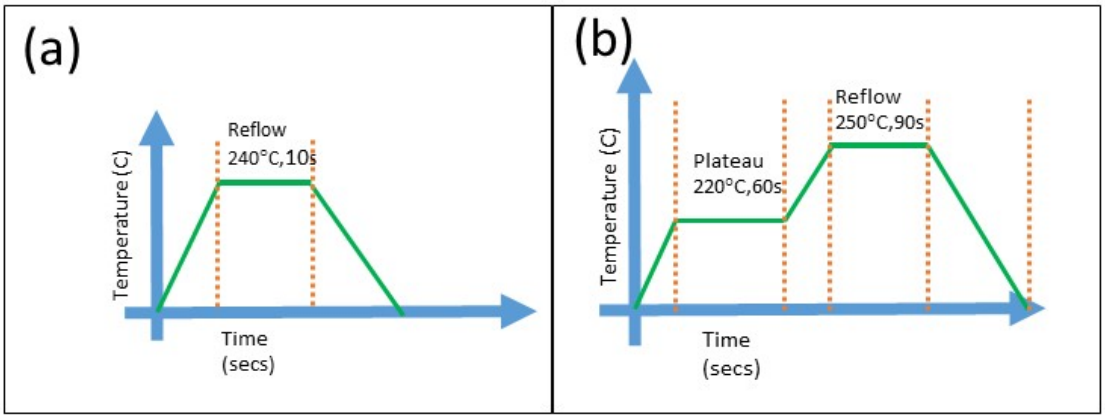


Figure 4.14: Temperature-time profile for assembly of interconnect at 10 µm pitch (a) Process A and (b) Process B, under formic acid

4.2 INTERCONNECTS AT 10 µM PITCH

After formations of interconnects, to understand the interconnects and their properties, various characterizations are done to qualify their metallurgy, mechanical properties and electrical properties which are presented in the coming sections.

4.2.1 METALLURGICAL CHARACTERIZATION

In this section, the morphology and the metallurgy of the interconnects formed by process A and B are presented and analyzed. Afterwards, the aging of interconnects is also done and evaluated. All analysis are performed by TIC cross-section after the assembly (see Chapter 2).

Before studying the metallurgy of the interconnects, a simple mass balance is presented, based on the interfacial reactivity between Ni and Sn contained in the Sn-Ag solder. We neglect for instance, the reaction with Au layer 0.1 µm in thickness (see Figure 4.12). Based on experimental results obtained on Chapter 3, the only intermetallic phase formed between Ni and Sn is Ni_3Sn_4 by the reaction:

$$3\,Ni + 4\,Sn \longrightarrow Ni_3Sn_4$$

Based on the physical properties of Ni, Sn and Ni_3Sn_4 phases (Table 4.1), it can be easily calculated that formation of 1 µm Ni_3Sn_4 layer thick leads to the consumption of 0.263 µm of Ni and 0.864 µm of Sn. In other words, the consumption of 1 µm thick Sn layer, leads to the consumption of 0.3 µm of Ni layer with the formation of Ni_3Sn_4 layer 1.16 µm thick.

Thus the formation of Ni_3Sn_4 phase leads to a volume contraction of about 11%. Moreover, by assuming that the Ni consumption on the pad side is almost equal to that on the pillar side, after complete reaction (i.e. consumption of 3 µm of Sn-Ag alloy), 0.45 µm of Ni from each side would be consumed and 3.5 µm of Ni_3Sn_4 layer is formed.

Table 4.1: Physicochemical data for Ni, Sn, Au and Ni_3Sn_4

	Ni	**Sn**	**Au**	**Ni_3Sn_4**
Molar mass (g/mol)	58.3	118.7	196.6	650.8
Density (g/cm^3)	8.9	7.3	10.5	8.6
Molar volume (cm^3/mol)	6.6	16.2	10.2	75.2

Figure 4.15 gives two SEM images of cross-sections of two interconnects made from process A and B respectively. In the following, the height of the interconnect (h) is defined as the distance between two Ni layers as shown in the figure. There are 5 major differences between these interconnects.

- Side wall wetting of lateral walls of Cu is observed is the case of interconnect B for which an isothermal holding at 180°C is performed (discussed in the previous section).
- The height of the interconnect B ($h_B \approx 1.5$ µm) is lower than that of interconnect A ($h_A \approx 3$ µm). This significant decrease in the interconnect B height is due to the leakage of

liquid alloy due to the lateral wetting of Cu walls.

- The interconnect B has a narrow neck, situated at a height about 1 µm from Ni/Ni_3Sn_4 interface from the pad side with a width of 2-3 µm.
- The interconnect B microstructure seems to be much more homogeneous than that of interconnect A for which we can distinguish a central zone (noted c) of thickness $h_A/3$ and two other similar (upper and bottom) zones noted u and b in Figure 4.15 (a).
- Some voids about some nanometers in size are observed in interconnect B.

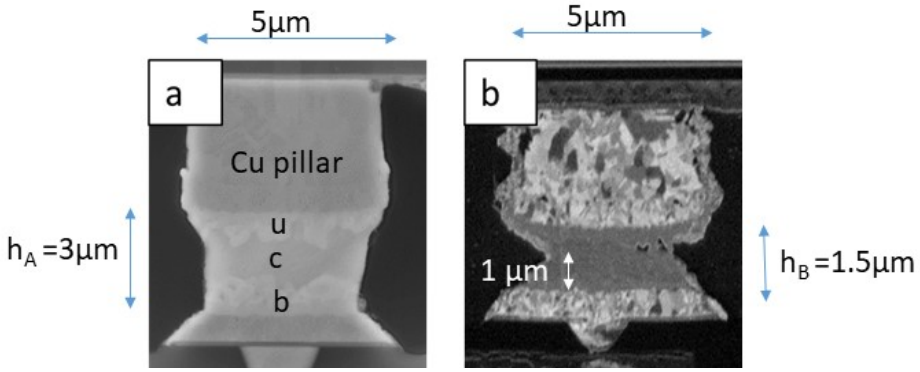


Figure 4.15: SEM images showing interconnects obtained under formic acid from (a) process A and (b) process B

In order to determine the metallurgy composition of different zones of interconnects, EDX analysis are done on the cross-section on each interconnect. In the EDX cartography analysis shown in Figure 4.16 and Figure 4.17 red, green, blue, pink and light blue colors show the presence of Cu, Ni, Sn, Au and Ag respectively.

For the interconnects obtained from process A, as we can see in Figure 4.16 (b), the joint consists of majorly blue color, with pink at the top and bottom of the joint. In Figure 4.16, the presence of Ni, Sn and Au at the edges of joint signifies that the intermetallic is made up of Ni, Sn and Au. After doing quantitative analysis, the composition of these zones is found to be 14±5at% of Au, 28±5at% of Ni and 57±5at% of Sn which corresponds to the composition of ternary δ-$AuNi_2Sn_4$ compound (reported in the literature - see for example Refs. [152]. Moreover, between δ-$AuNi_2Sn_4$ compound and Ni layer a submicronic layer of Ni_3Sn_4 IMC is observed. This interconnect has been referred as *Sn joint interconnect (process A)*. Here, no Sn spilling on to the lateral walls of Cu pillar was observed (reflow for 10 secs at 240°C). We recall that no spilling was observed in the case of reflow under formic acid (60 secs at 250°C, Figure 4.2) as well.

For the second interconnect which is formed by process B, EDX analysis of the interconnect cross-section (Figure 4.17) show the presence of only two elements Ni and Sn and the quantitative analysis confirm that all the joint is homogeneous in composition and contains 42±5at% Ni and 57±5at% Sn, corresponding to the Ni_3Sn_4 IMC composition. This interconnect has been called *IMC interconnect (process B)*. It is interesting to note that Sn spilling on to the lateral walls of Cu pillar is only observed in the case of assembly with temperature-time T(t) profile given in Figure 4.14 (b) (60 secs at 220°C + 90 secs at 250°C) but not in case of reflow with seed etching and T(t) profile given in Figure 4.1 (60 secs at 250°C).

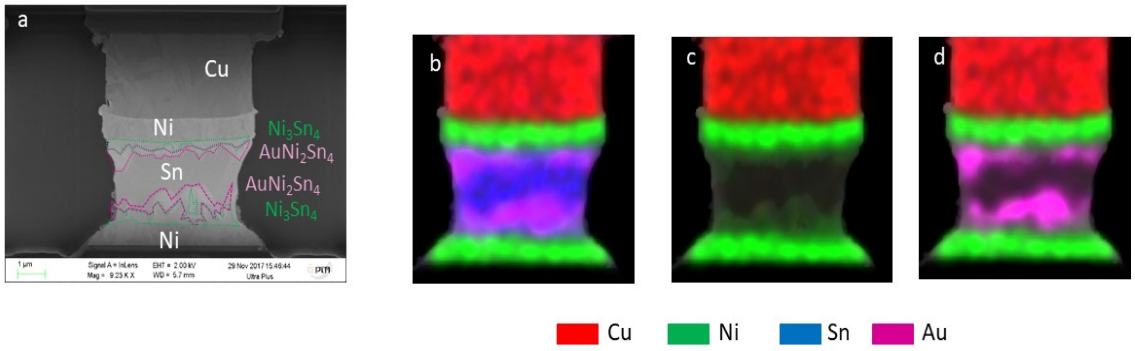


Figure 4.16: (a) SEM image for cross-section of Sn interconnect, (b) EDX cartography showing presence of Ni, Au and Sn (c) EDX cartography showing the presence of Ni and (d) EDX cartography showing the presence of Au

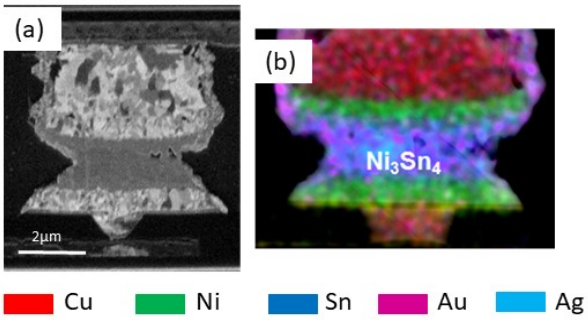


Figure 4.17: Cross-section of IMC interconnect form by process B under formic acid (a) SEM image (b) EDX cartography showing the presence of Ni, Sn and Au

Figure 4.18 gives a summary of different configurations after reflow and bonding operations under formic acid atmosphere.

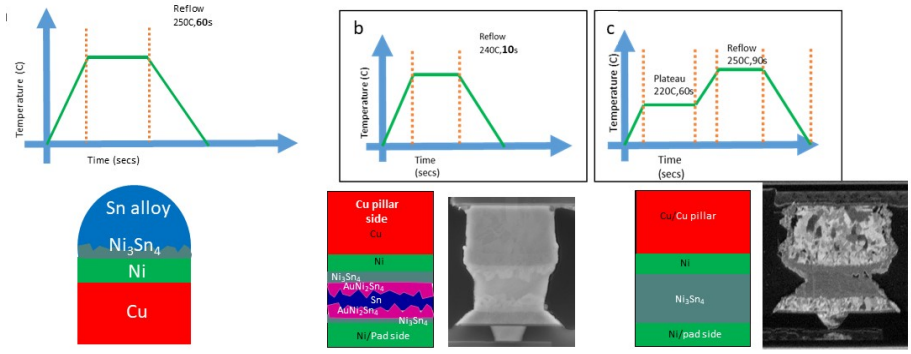


Figure 4.18: Summary of schematic configuration of different systems after reflow and bonding processes under formic acid atmosphere (with seed etching) and corresponding T(t) profiles

In the following we will present some thermodynamic and kinetic analysis for both processes A and B.

Analysis of process A

The comparison of Figure 4.18 (b) with Figure 4.18 (a) clearly indicates that the layer of Au initially deposited on the pad side, plays a major role on to the evolution of the interfacial system not only on the pad side but also on the pillar side. At the pad side (i.e. at the side where a thin layer of Au is initially deposited), two IMC layers are observed, a thin layer of the binary Ni_3Sn_4 phase (in contact with Ni layer) and a thicker layer of the ternary δ-$AuNi_2Sn_4$phase. At the pillar side, not only the binary Ni_3Sn_4 layer is formed in contact with the Ni layer (as in the case of the reflow process) but also another intermetallic layer ($AuNi_2Sn_4$) despite the fact that no Au was initially deposited on the pillar side. This means that a part of Au atoms has diffused inside the solder alloy from the pad side to the pillar side. This point will be discussed in details here below.

From Figure 4.16, we can evaluate the average thickness (e) of Sn, Ni_3Sn_4 and δ-$AuNi_2Sn_4$layers after the bonding process: $\sim$ 1.4 µm of Sn is left and the rest of Sn ($\sim$ 1.6 µm) would be consumed in the formation of $\sim$ 0.6 µm of binary Ni_3Sn_4 phase *(0.2 and 0.4 µm on the pillar and pad side respectively)* and $\sim$ 0.61 µm of the ternary δ-$AuNi_2Sn_4$ phase *(0.28 and 0.33 µm on the pillar and pad side respectively)*. Moreover, Au layer 0.1 µm thick, deposited on the pad side, is totally consumed.

From data given in Table 4.1, it can be easily calculated that the formation of 0.6 µm Ni_3Sn_4 layers leads to the consumption of ***0.55 µm Sn and 0.15 µm Ni*** *(0.05 and 0.10 µm on the pillar and pad side respectively).*

In order to evaluate the quantity of Ni (Au and Sn) consumed during formation of δ phase, we perform a mass balance for its formation by the reaction:

$$Au + 2\,Ni + 4\,Sn \longrightarrow AuNi_2Sn_4$$

Given the fact that no data on the density of δ-$AuNi_2Sn_4$phase exist in the literature, we assume that the volume change during the formation of δ phase follows Vegard's law [153] (no contraction or expansion during δ IMC formation from pure elements. Based on the values of molar volumes of Au, Ni and Sn (given in Table 4.1) it can be easily calculated that formation of **0.61 µm of δ phase** *(0.28 µm on the pillar and 0.33 µm on the pad side)* leads to the consumption of ***0.45 µm Sn, 0.07 µm Au and 0.09 µm Ni*** *(0.04µm on the pillar and 0.05µm on the pad side).*

Finally, the calculated thickness of consumed elements during the bonding process A are: 1 µm Sn, 0.07 µm Au and 0.24 µm Ni (0.09 µm on the pillar and 0.15 µm on the pad side). The calculated values of consumed Sn (1 µm) and Au (0.07 µm) are 30-40% lower than the expected ones (1.6 and 0.1 µm respectively). This difference could be due to 4 factors: (i) In general, a volume contraction is observed during formation of IMCs from pure elements, thus the calculated thicknesses of consumed elements (Sn, Au and Ni) during δ-$AuNi_2Sn_4$ phase formation are underestimated. (ii) A small quantity of solder Sn-Ag-Au alloy could be spilled over the Cu pillar walls and do not participate to the formation of δ phase. (iii) As it will be seen below, a small quantity of Au remains dissolved in the solder alloy and do not react to form the δ phase. (iv) the initial thickness of electroplated Sn can be different than the targeted

one.

In the following we will present a scenario of physio-chemical processes that take place during the bonding process A, based on the initial configuration of the system (Figure 4.12) and the temperature - time (T(t)) profile (Figure 4.14). We recall that 3 µm of Sn-2wt%Ag alloy (5µm in diameter) is put in contact with a layer of Au 0.1 µm thick and 5 µm in diameter. When the temperature attains 221°C, the eutectic melting of Sn-Ag alloy occurs (see Figure 3.6). The time during heating (5°C /sec) from 221°C to 240°C is about 4 secs. Thus the total time during which the alloy will remain in liquid state (without taking into account the undercooling degree) is about 18 secs (2x4 + 10). When a layer of Au is put in contact with the liquid Sn-Ag alloy, the dissolution of Au will take place first. In order to simplify, we assume that Sn-Ag alloy consists only of pure Sn. (Note that the influence of some percentage of Ag in liquid Sn on the dissolution process is practically negligible given the fact that interactions between Au and Ag are very weak [154])

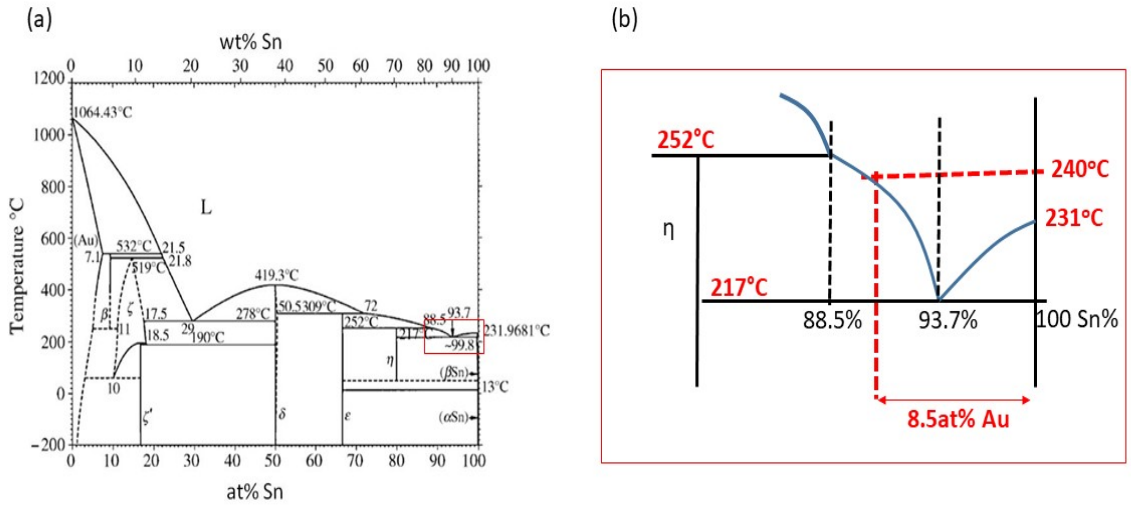


Figure 4.19: (a) Au-Sn binary phase diagram [154], (b) enlarged view of phase diagram

Figure 4.19 gives the binary Au-Sn phase diagram [154]. From reference [155], it can be calculated that the solubility limit of Au in liquid Sn at 240°C is about 8.5at%Au. From the molar volumes of Sn and Au (Table 4.1), it can be easily calculated that the subsystem 3 µm Sn + 0.10 µm Au corresponds to about Sn-5at%Au.

Then the content of Au in Au-Sn subsystem (5at%Au) is significantly lower than its solubility limit in liquid Sn at 240°C (8.5at%Au). Thus the Au layer will totally dissolve in liquid Sn (or in liquid Sn-Ag alloy) at 240°C.

Given the value of the diffusion coefficient of Au in liquid Sn ($D \sim 10^{-8}$ m^2/sec [156]), the needed time for Au atoms to diffuse from the pad side to the pillar side of the joint (at the distance $l \sim 3$ µm) can be evaluated to be $t_D \sim l^2/D \approx 10^{-3}$ sec.

If we assume that the diffusion process of Au in liquid Sn is much faster than the dissolution rate (k), i.e. $D/l >> k$, then the liquid Sn-Au alloy will be homogeneous in Au during the dissolution process and the variation of concentration of Au with dissolution time will be given by the following equation :

$$\frac{dC}{dt} = \frac{k}{l}(C_s - C) \tag{4.1}$$

where C is the instantaneous concentration of dissolved Au in liquid Sn, C_s the solubility limit at a given temperature (corresponding to 8.5at%Au at 240°C), k is the dissolution rate (in m/sec) and l is the width (length or height) of the liquid Sn zone. Integration of Eq. 4.1 (C = 0 at t = 0) leads to:

$$ln\frac{C_s}{C_s - C} = \frac{k}{l}t \tag{4.2}$$

The final dissolution time t_f corresponds to the total dissolution of solid Au in liquid Sn, i.e. when the final concentration of Au in liquid Sn is attained (i.e. $C = C_f = 5at\%$). A schematic variation of Au concentration during the dissolution process is shown in Figure 4.20.

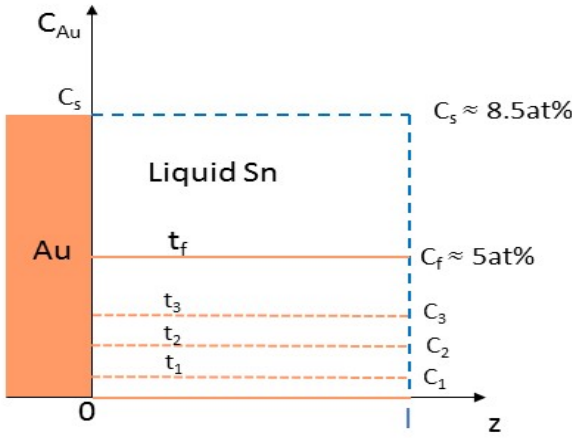


Figure 4.20: Schematic variation of Au concentration (C) during very rapid dissolution of a Au layer in a liquid layer of Sn (thickness l) form initial C = 0 (t = 0) to final concentration C = C_f (attained at t = t_f) corresponding to the total dissolution of Au layer. Process limited by the dissolution kinetics

With C_s = 8.5at%, C_f = 5at%, l = 3 µm and k = 10^{-5} m/s [157], from Eq. 4.2 we find the dissolution time $t_f \approx 2$ *secs* $>> t_D \approx 10^{-3}$ secs. This result clearly indicates that *the dissolution process of Au in liquid Sn is the limiting step and the total dissolution of 0.1 µm of Au in 3 µm of liquid Sn take place in less than 2 secs.* Note that during this time, the dissolution of Ni layer at the pillar side of the joint will occurs also, followed by the formation and growth of the Ni_3Sn_4 IMC at Ni/liquid Sn interface (see Chapter 3).

Thus after the total dissolution of the Au layer in the liquid alloy, the schematic configuration of the system (by neglecting the presence of Ag) can be given approximately as:

*Cu pillar / **Ni** / Ni_3Sn_4 / **liquid Sn-Au-Ni** / **Ni** / pad side*

Afterwards the dissolution of Ni at the pad side starts also followed by formation and growth of Ni_3Sn_4 layer at the pad side :

*Cu pillar / **Ni** / Ni_3Sn_4 / **liquid Sn-Au-Ni** / $\underline{Ni_3Sn_4}$ / **Ni** / pad side*

Note that the thickness of Ni_3Sn_4 layer formed on the Cu pillar side ($\sim$ 0.2 µm) is lower than that at the pad side ($\sim$ 0.4µm) see Figure 4.15. This is due to the fact that, *on the Cu pillar side* the nucleation and growth of Ni_3Sn_4 layer takes place by solid state reaction during deposition process as well as during heating up to the melting temperature of Sn-Ag alloy leading to the formation of a thin and continuous Ni_3Sn_4 layer (see Chapter 3, Ni/solid Sn reaction). Thus when the solder alloy melts, the growth of Ni_3Sn_4 layer takes place by slow solid state diffusion. On the contrary, on the pad side the nucleation of Ni_3Sn_4 layer takes place during dissolution of Ni, at the oversaturated Sn-Ni liquid alloy/Ni interface which leads to the formation of a thick Ni_3Sn_4 layer just at the beginning of Ni/liquid Sn reaction (see Section 3.4 Ni/liquid Sn reaction in Chapter 3).

The study of the interfacial reactivity in the Ni/liquid Sn-Au-Ni diffusion couple at 240°C needs the knowledge of the isothermal section of the Ni-Au-Sn ternary system at 240°C. In the literature only the isothermal sections of this diagram at 200 and 300°C are given [159] (see Appendix C). For this reason, we have performed calculations of the isothermal section of this system at 240°C with the Thermocalc software [158], shown in Figure 4.21. In this figure a schematic presentation of the isothemal section is also shown. In order to compare diagrams obtained by Thermocalc with those reported by [159], in Figure C.1 (Appendix C) we have also reported the isothermal sections obtained by Thermocalc at 200 and 300°C. Figure C.1 (Appendix C) show that the isothermal sections obtained by Thermocalc are similar with those reported by [159].

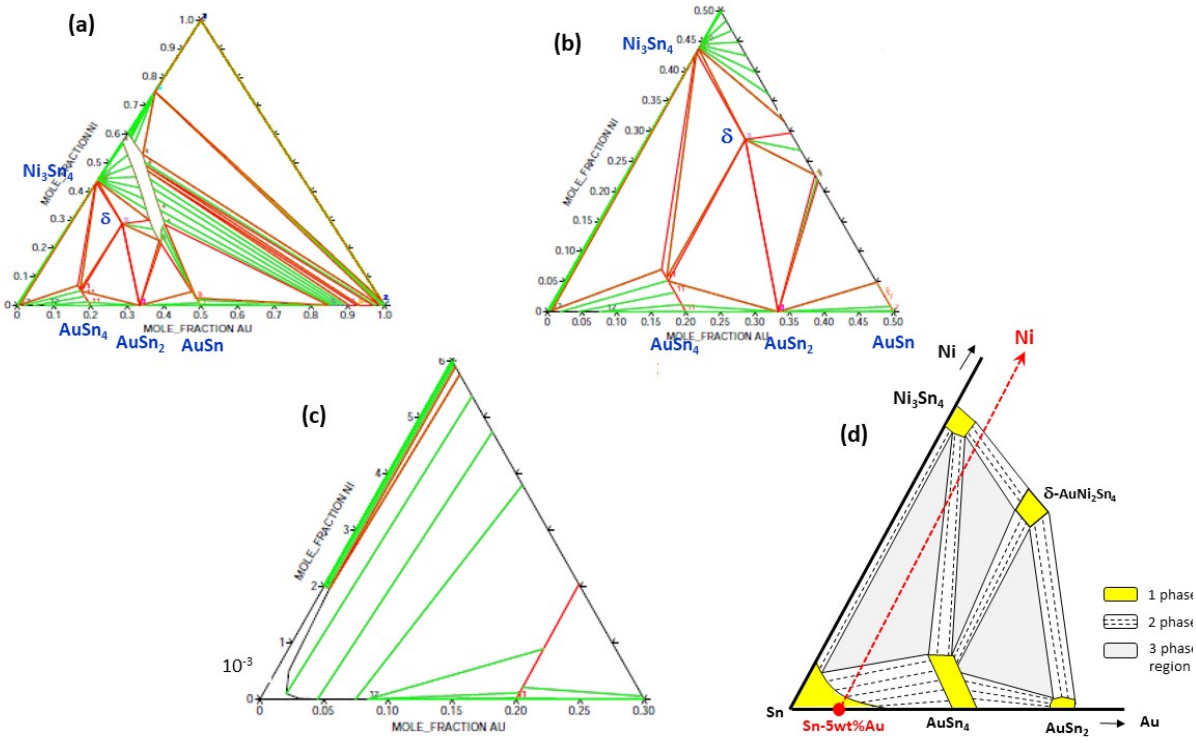


Figure 4.21: Calculated ternary phase diagram for Ni-Au-Sn ternary system at 240°C with Thermocalc software (a, b and c) and its schematic presentation (d)

The diffusion of Ni atoms from Ni layer to the liquid alloy leads to the growth of Ni_3Sn_4 layer as well as to the increasing of Ni content into the liquid Sn-5at%Au alloy. According to the calculated Au-Ni-Sn phase diagram, the solubility limit of Ni in Sn-5at%Au is of the order of

0.1at%Ni (see Figure 4.21 (c)).When the Ni content in the liquid alloy becomes higher than its solubility limit, the liquid will be in a metastable state is respect to the formation of δ-$AuNi_2Sn_4$ compound (see Figure 4.21). Afterwards, the nucleation and growth of the δ phase at Ni_3Sn_4/liquid alloy interface leads to an almost continuous δ layer and the configuration of the system can be described as:

*Cu pillar / **Ni** / Ni_3Sn_4 / δ–$AuNi_2Sn_4$ / **liquid Sn-Au-Ni** / δ-$AuNi_2Sn_4$ / Ni_3Sn_4 / **Ni** / pad side*

According to the phase diagram, the liquid Sn-Au-Ni / δ-$AuNi_2Sn_4$ interface is in metastable equilibrium in respect to the formation of $AuSn_4$ phase which is not observed at the interface at SEM scale. The growth of δ-$AuNi_2Sn_4$ layer will take place by interdiffusion of Au, Ni and Sn through this layer. The diffusion path in the system would be given by Ni / Ni_3Sn_4/ δ-$AuNi_2Sn_4$/ liquid Au-Sn-Ni. We assume that the growth of δ-$AuNi_2Sn_4$ layer stops when the Au content in the liquid alloy attains the value corresponding to the ternary metastable equilibrium between the liquid alloy, δ-$AuNi_2Sn_4$ and Ni_3Sn_4 and phases. According to the calculated phase diagram (Figure 4.21 (c)), this value is lower than 0.05at% Au, thus almost all Au dissolved in Sn liquid is consumed during the growth of δ-$AuNi_2Sn_4$. Under these conditions, the further evolution of the system is concerned with the growth of Ni_3Sn_4 layer in both sides. It would be interesting to study the further evolution of the system until the total consumption of liquid Sn in order to determine if δ-$AuNi_2Sn_4$ layer is (or not) a good barrier to diffusion process.

Analysis of process B

There are two major differences between process A and B:

1. For the process B, there is an additional isothermal holding for 1 min at 220°C in order to strongly activate the flux and thus to obtain a maximum of deoxidation effect.

2. The reflow temperature and time are higher for the process B (250°C for 90 secs against 240°C for 10 secs for process A). This increase in reflow temperature and time for process B is done to completely consume the Sn layer and transform it into IMC.

The choice of reflow conditions (250°C, 90 secs) was done based on the experimental results obtained for process A. In process A (240°C, 10 secs) about 1.5 µm of Sn is transformed into Ni_3Sn_4 and $AuNi_2Sn_4$ phases. If we assume that the growth of interfacial IMCs is limited by the diffusion process (as it was the case in Chapter 3), by choosing a reflow time for process B 9 times longer than for process A (and a slightly higher temperature, 250°C against 240°C), we expect that 3 µm of Sn will be for sure totally transformed into IMCs.

However, the experimental results we obtain for process B were unexpected and surprising (see Figure 4.15 (b))

1. There is a spilling of alloy on the lateral side of Cu pillar (height 3 µm).

2. The total thickness of the joint is about 1-1.5 µm instead of 4 µm (resulting from the calculations obtained for process A when all Sn is consumed).

3. The width of the joint is not uniform, the formation of a neck situated at about 1 µm from Ni/IMC interface at the pad side is observed. The diameter of this neck is about 2-3 µm.

It is important to note that during the reflow process at 250°C for 60 secs (reflow profile no. 1) under the same conditions as for the joining process B (with seed etching, under formic acid atmosphere) there was not any major spilling of liquid alloy on the Cu pillar lateral wall (see Figure 4.2 (b)). The main difference between them is the performing of an isothermal holding at 220°C for 60 secs for process B and not for the reflow process.

The characterization of several samples after an isothermal holding at 220°C for 60 secs show that a spherical cap of Sn-Ag alloy is observed (as seen in Figure 4.22), meaning that the Sn-Ag alloy is in the liquid state during 60 sec at 220°C. (Note that, the melting temperature of Sn-Ag eutectic being 221°C, the real temperature is higher than the targeted temperature of 220°C).Thus in the case of process B the Sn based alloy will stay at the liquid state during a longer time compared to the reflow process at both 220°C (60 secs more) and at 250°C (30 secs more). Also the difference between process B and reflow is that in the case of bonding process B (and process A) some pressure was applied at room temperature to make a physical contact between solder and Au/Ni pad.

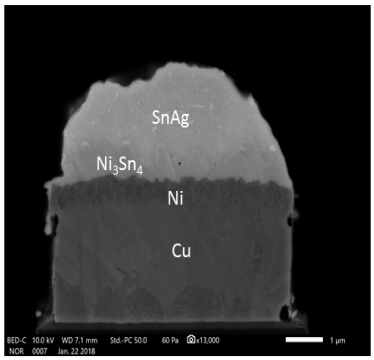


Figure 4.22: SEM section of test vehicle reflow at 220°C for 60 secs

From all the comparisons we can conclude that the deoxidation effect of the flux at 220°C but also the longer isothermal holding (and higher temperature) are at the origin of the very pronounced spilling effect for process B. Under these conditions Sn (and Au) atoms will react not only with Ni (at both reaction interfaces) but also with the lateral walls of Cu pillar by reactive wetting and/or by surface diffusion (Figure 4.17).

The fact that a part of the liquid alloy reacts with the lateral walls of Cu pillar leads to a decrease in the number of moles of Sn (and Au) which will react with Ni layers (at both interfaces: pillar and pad side). The decrease of quantity of Sn (and Au) combined with a higher temperature (250°C) and longer reaction time (90 secs) will lead to the total consumption of the liquid alloy for process B, i.e. a TLPB (transient liquid phase bonding) or SLID (solid liquid interdiffusion bonding) process. Thus the diffusion path for process B will evolve from

$$\boldsymbol{Ni} \,/\, Ni_3Sn_4 \,/\, \delta \,/\, \boldsymbol{liquid}$$

to

$$\mathbf{Ni} \,/\, Ni_3Sn_4 \,/\, \delta$$

and afterwards to either Ni / Ni_3Sn_4+ δ (biphase domain) or to Ni / (Ni_3Sn_4 phase containing some Au) configuration if the solubility of Au in the Ni_3Sn_4 phase is relatively high. However,

no data on the solubility of Au in the Ni_3Sn_4 phase exists in literature.

The EDX cartography of the joint obtained by the process B (Figure 4.17) clearly indicates that some Au is found all over the zone where Ni_3Sn_4 phase is situated between Ni layers. Knowing that initially we have layers of Sn and Au about 3 and 0.1 µm thick respectively, we can evaluate the overall concentration of Au in the joint (between Ni layers) by assuming that spilling process concerns in the same way both Sn and Au atoms. Indeed, a ratio of thickness e_{Au}/e_{Sn} = 1/30, leads to the mole number ratio n_{Au}/n_{Sn} of 0.053:

$$\frac{n^{Au}}{n^{Sn}} = \frac{V^m_{Sn}}{V^m_{Au}} . \frac{e_{Au}}{e_{Sn}} = \frac{16.26}{30X10.21} = 0.053 \tag{4.3}$$

Where $V^m{}_{Sn}$ and $V^m{}_{Au}$ are the molar volumes of Sn and Au respectively. By taking, $n_{Ni} = 3/4n_{Sn}$ (in Ni_3Sn_4 phase) we can evaluate that the molar fraction of Au in the joint (x_{Au}) will be:

$$x_{Au} = \frac{n_{Au}}{n_{Au} + n_{Ni} + n_{Sn}} = \frac{0.053 n_{Sn}}{0.053 n_{Sn} + 0.75 n_{Sn} + n_{Sn}} = 0.03 \tag{4.4}$$

In the other extreme case when Au atoms do not participate in the spilling process, Au concentration in the joint will be much higher than 3at%. For example, if about 70% of Sn atoms are consumed by spilling process (then the joint thickness would be about 1.2 µm instead of $\sim$ 4 µm) but no Au atoms consumed in the process, then the concentration of Au in the joint will be about 10at% Au.

Thus, either Au is dissolved completely in the δ phase if its solubility limit in δ phase is higher than 3-10at% or a part of Au should be contained in small nanometric particles of δ-$AuNi_2Sn_4$ phase dispersed inside the Ni_3Sn_4 phase.

If no nucleation and growth of Ni_3Sn or Ni_3Sn_2 phases occur at the Ni/Ni_3Sn_4 interface, the above configuration Ni / (Ni_3Sn_4 + δ–$AuNi_2Sn_4$) / Ni will be the final metastable equilibrium configuration. The only possible evolution of such a system could be the dissolution of possible δ precipitates into Ni_3Sn_4 if the solubility limit of Au in Ni_3Sn_4 is not yet attained and/or the growth of δprecipitates by Oswald ripening. In order to study the morphological evolution of joints for process A and B, heat treatments of these joints at different temperature are performed which will be discussed in the next section.

Lastly, at times, Ag_3Sn aggregates are observed after bonding process B (as seen in Figure 4.23) and even after the isothermal holding at 220°C. These aggregates are in the form of a large disk of around 1-2 µm thick. The main reason for this behavior could be due to the increase in the concentration of Ag in Sn-Ag solder alloy during the consumption of Sn by reaction with Ni layers (as it was explained in the Chapter 3). This phenomenon could lead to the formation of Ag_3Sn precipitates during isothermal holding at liquid state and/or during the solidification of the alloy.

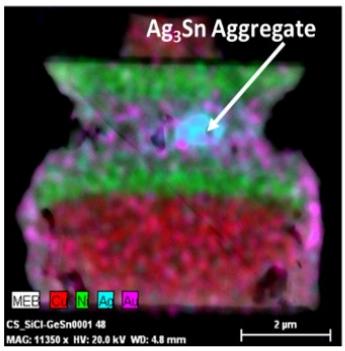


Figure 4.23: EDX cartography for IMC interconnect with Ag_3Sn aggregate

4.2.2 METALLURGICAL EVOLUTION OF INTERCONNECTS DURING AGING

Here the key interest is to see how Sn interconnects (process A, figure 4.16) and IMC interconnects (process B, figure 4.17) will evolve during aging in terms of morphology and composition. We recall that the Sn interconnect (A) consists of **Ni** / Ni_3Sn_4 / δ-$AuNi_2Sn_4$ / **Sn** / δ-$AuNi_2Sn_4$ / Ni_3Sn_4 / **Ni** and the IMC interconnect (B) consists of **Ni** / Ni_3Sn_4 (+ δ) / **Ni** diffusion couple (see Figure 4.21). As it was already mentioned before, for both couples, the Ni/Ni_3Sn_4 interface is in a metastable equilibrium with respect to the formation of stable phases Ni_3Sn and Ni_3Sn_2. In the literature, at the temperature below 300°C, no growth of IMC between Ni and Sn other than Ni_3Sn_4 is reported [63]. However, without the presence of Sn in the system, the stability of Ni/Ni_3Sn_4 couple for temperatures lower than 300°C is studied by Bader et al. [47], who reported that after 125 hrs at 240°C and 300 °C, Ni_3Sn_2 layer starts to grow at the interface whereas Ni_3Sn layer appears only at higher temperature (>400°C).

In Chapter 3 (Section 3.3) surprisingly, non-continuous Ni_3Sn_2 layer was observed at Ni/Ni_3Sn_4 interface for annealing time longer than 96 hrs (untill about 850 hrs) at 200°C. In this section we will study the stability of the metastable Ni/Ni_3Sn_4/Ni diffusion couple (in the case of IMC interconnects formed by process B) and also especially focused on the evolution and stability of the Ni/Ni_3Sn_4/$AuNi_2Sn_4$/Ni_3Sn_4/Ni diffusion couple (in the case of Sn interconnects formed by process A).

Evolution of Sn interconnect with aging

Ni* / Ni_3Sn_4 / δ-$AuNi_2Sn_4$ / *Sn* / δ-$AuNi_2Sn_4$ / Ni_3Sn_4 / *Ni

We recall that the thickness (in µm) of different layers for Sn interconnect just after the process A are as follows (see Figure 4.17 a):

Pad side/ ***Ni*** -0.95 / Ni_3Sn_4 - 0.4/ δ - 0.33 / ***Sn***-1.6 / δ - 0.28 / Ni_3Sn_4 - 0.2 / ***Ni - 0.96*** / Cu pillar side

As mentioned above, there are two main differences between Sn interconnect and IMC interconnects (Ni/Ni_3Sn_4/Sn systems): (i) the presence of the δ layer about 0.28 and 0.33 µm thick respectively for pillar side and pad side in Sn interconnect and (ii) the presence of two ***Ni/Sn*** diffusion couples for Sn interconnect instead of two Ni/Ni_3Sn_4 diffusion couple for IMC interconnect (***Ni/Ni_3Sn_4/Sn system)***. Despite this important difference, we can estimate the time necessary for total consumption of the ***Sn*** layer (about 1.4 µm thick) in Sn interconnect at a given temperature, based on the growth kinetics of Ni_3Sn_4 layer at Ni/solid Sn interface, determined in Chapter 3. It should take about 30 mins at 200°C, 4 hrs at 175°C and 50 hrs at 150°C for 0.7 µm of Sn to be transformed into Ni_3Sn_4 IMC. Thus, Sn interconnect is expected to change into IMC interconnect (total consumption of Sn) rapidly, due to low thickness of solder left after the process A.

Figure 4.24 (b) clearly shows that after 30 mins at 200°C, the left Sn is completely consumed into the binary Ni_3Sn_4 and ternary $AuNi_2Sn_4$ IMCs. During annealing, both δ phase layers grow and meet together forming one single layer which is situated in the center of the joint and capped with Ni_3Sn_4 IMC layers from both sides. From now on, for better clarity, this

interconnect is renamed as ***former Sn interconnect.*** During the annealing at 200°C, the ratio r = (total thickness of binary Ni_3Sn_4 IMC)/(total thickness ***e*** of ternary δ IMC layer) changed (see Figure 4.24) as follows:
After the process A (t = 0) r is about 1.5/1 (0.4/0.3 on the pad side and 0.3/0.2 on the pillar side) and after 200hrs of annealing at 200°C, the ratio r is roughly 2:1 ($e_{Ni_3Sn_4}$ = 2 µm and e_{δ} = 1 µm).

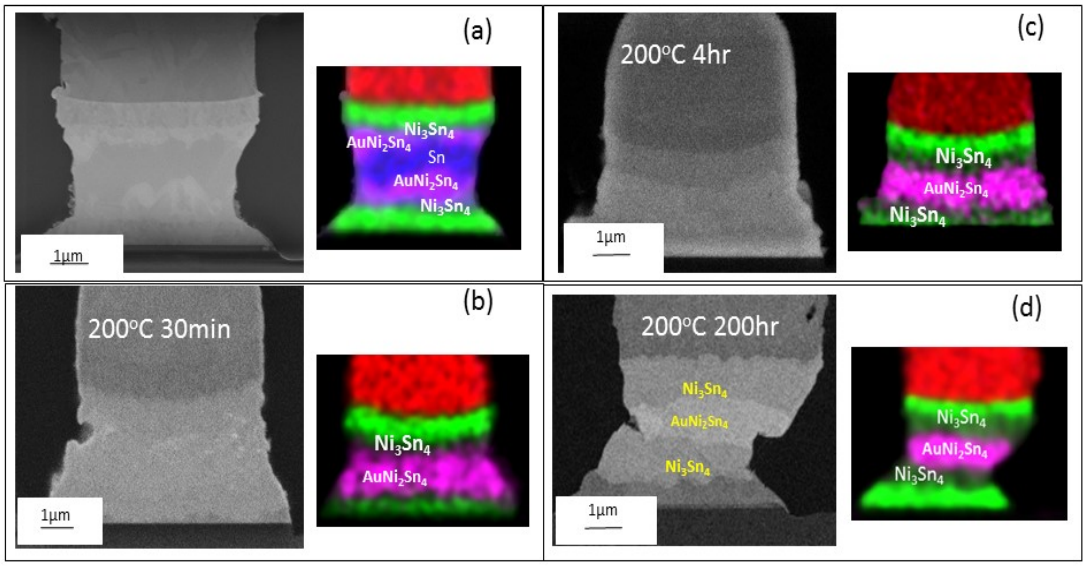


Figure 4.24: (a) Micrographs and their EDX cartography for Sn interconnects just after the joining process A and (b) after annealing at 200°C for 30 min (c) 4 hrs and (d) 200 hrs

The schematic diffusion path of the system during annealing at 200°C is shown in Figure 4.25.

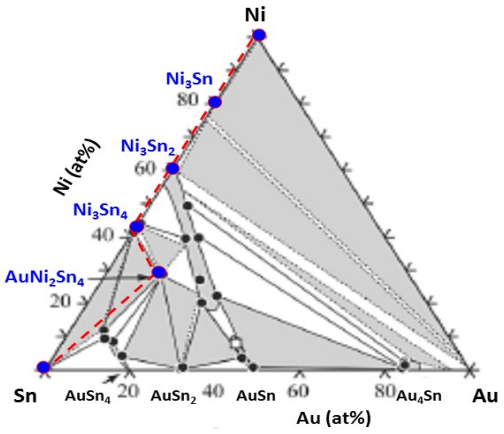


Figure 4.25: Isothermal section of the ternary Au-Sn-Ni system at 200°C according [159]

Figure 4.26 gives SEM cross sections of samples aged for 24, 200 and 1303 hrs at 200°C. Figure 4.26 (c) and (d) clearly show the formation of a new phase at Ni/Ni_3Sn_4 interface. EDX analysis of this phase show that it contains 57±15% Ni and 42±11% Sn which correspond

to Ni_3Sn_2 phase (see Figure 4.27). These analysis confirmed also the composition of already observed Ni_3Sn_4 phase: 39 ±15% Ni and 58 ±11% Sn.

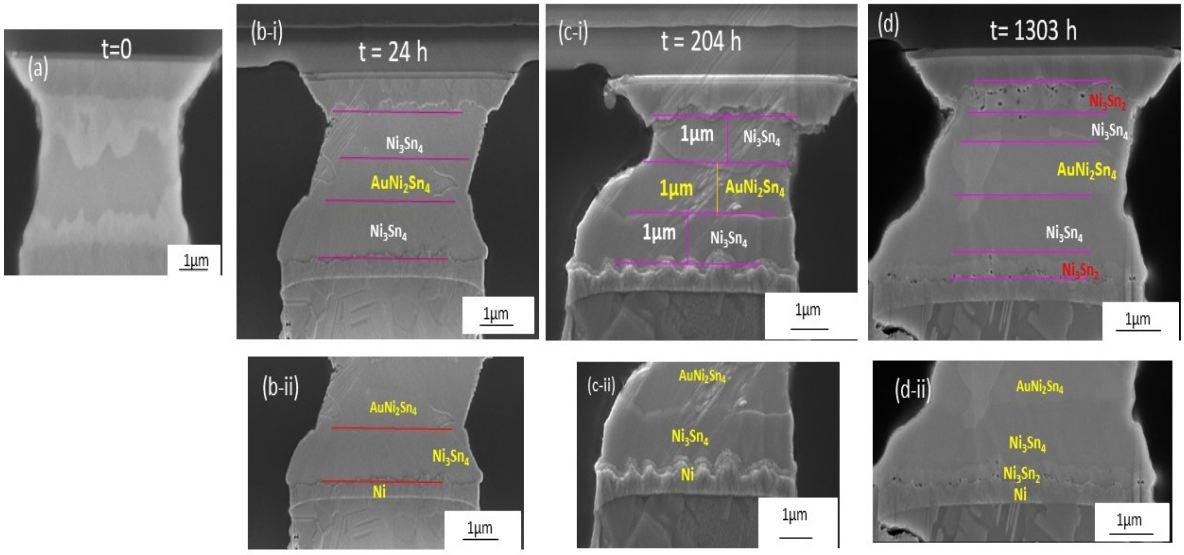
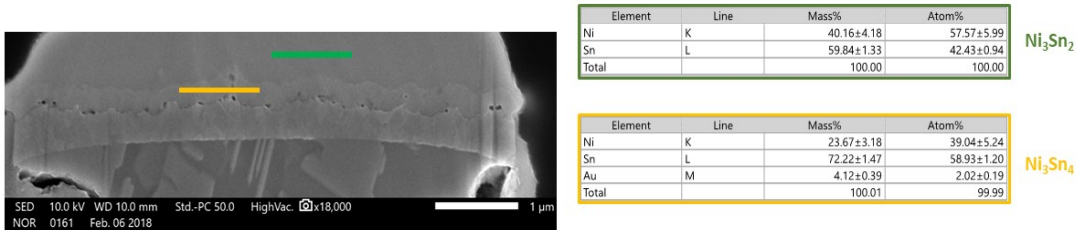


Figure 4.26: SEM micrographs for annealing of Sn interconnects at 200°C (a) at t=0, (b) t=24 hrs, (c) t=204 hrs and (d) t=1303 hrs



Element	Line	Mass%	Atom%
Ni	K	40.16±4.18	57.57±5.99
Sn	L	59.84±1.33	42.43±0.94
Total		100.00	100.00

Ni_3Sn_2

Element	Line	Mass%	Atom%
Ni	K	23.67±3.18	39.04±5.24
Sn	L	72.22±1.47	58.93±1.20
Au	M	4.12±0.39	2.02±0.19
Total		100.01	99.99

Ni_3Sn_4

Figure 4.27: SEM micrograph for Sn interconnect (process A) showing the interface between Ni and Ni_3Sn_4 after annealing at 200°C for 1303 hrs, with its EDX analysis indicating the formation of Ni_3Sn_2 phase

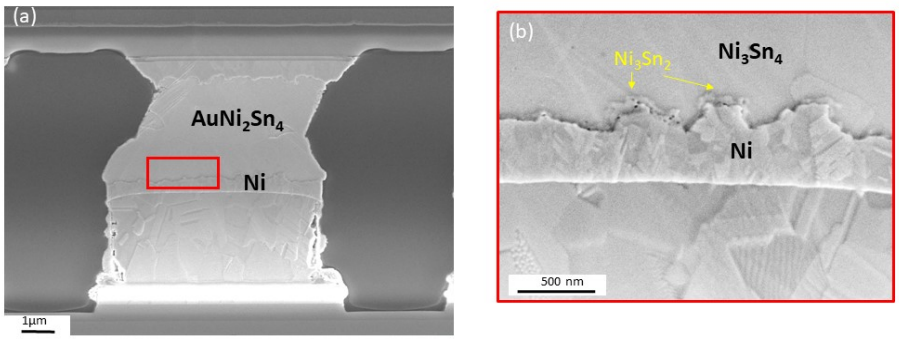


Figure 4.28: (a) SEM micrograph Sn interconnects (process A) after aging at 200°C for 24 hrs and (b) its enlarged SEM micrograph for the interface between Ni and Ni_3Sn_4

Fine characterizations of Ni/Ni_3Sn_4 interfaces for samples aged for 4 and 24 hrs at 200°C (Figure 4.28) show that no new phase is detected after 4 hrs but after 24 hrs of annealing, a new Ni_3Sn_2 layer has merged out at the interface accompanied with some nanometric void. (which may be due to the sample preparation by ion beam for SEM). This layer, as can be seen in Figure 4.28 (b), is not continuously present all over the Ni/ Ni_3Sn_4 interface. It consists of small grains of roughly around 60-100 nm in size with the average thickness of this layer to be around 80 nm.

Figure 4.29 gives enlarged SEM images of Ni/Ni_3Sn_4 interfaces for samples aged at 200°C for 45.5, 92.5, 204, 898 and 1303 hrs. The Ni_3Sn_2 layer becomes continuous after 45 hrs of annealing and grows uniformly after that. By about 1300 hrs of annealing, the layer attained the average thickness of 250 nm. Figure 4.30 gives the variation of average thickness with time of the Ni_3Sn_2 layer in logarithmic scale.

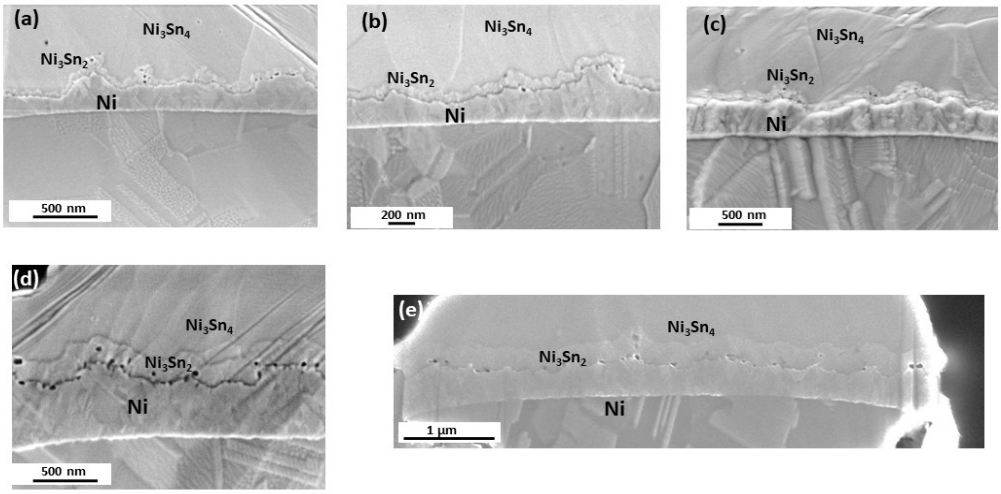


Figure 4.29: SEM micrograph for Sn interconnect (process A) showing the interface between Ni and Ni_3Sn_4 after annealing at 200°C for (a) 45.5 hrs, (b) 92.5 hrs (c) 204 hrs, (d) 898 hrs and (e) 1303 hrs

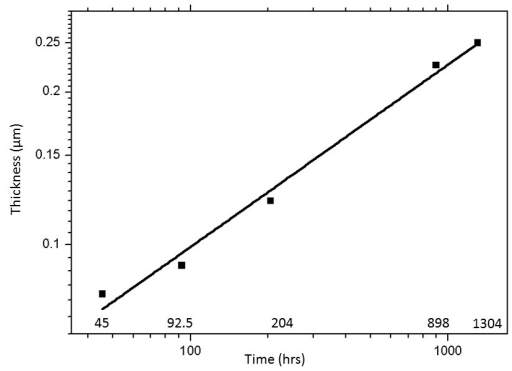


Figure 4.30: Graphs between log of thickness of Ni_3Sn_2 layer vs log of time for annealing of Sn Interconnect (process A) at 200°C

The average thickness values (***e***) for Ni_3Sn_2 layer measured after different holding time at

200°C are given in Table 4.2. In order to determine the growth law of the Ni_3Sn_2 layer, we assume that its growth kinetics follows a power law:

$$e = k_n t^n \tag{4.5}$$

where t is the time, n is a growth exponent and k_n the kinetic growth coefficient. Note that Eq. 4.5 is only valid if it operates during the growth of the layer from t = 0 (e = 0) to t = t (e = e) as mentioned in Chapter 3. The value of n is calculated by plotting logarithm of e as a function of logarithm of t shown in Figure 4.30. The slope of this graph gives n = 0.36 and the intercept gives the value of kinetic growth coefficient k = 0.0186 µm/hr^{-n}. The value of n lower than 1 (n $\sim$ 1/3) suggests that the growth kinetics is limited by diffusion as it was the case for the growth of Ni_3Sn_4 layer in the Ni/liquid Sn and Ni/solid Sn systems (as reported in this thesis in Chapter 3).

Table 4.2: Thickness of Ni_3Sn_2 after annealing at 200°C for different time

Time(hr)	45.5	92.5	204.5	898	1303
Thickness (µm)	0.08	0.09	0.12	0.226	0.25

Similar trend has been observed for lower temperature also but with of course, thinner Ni_3Sn_2 layer. For comparison, after 200 hrs at 175°C, the Ni_3Sn_2 layer is 60 nm thick against 122 nm thick at 200°C for the same annealing time. An estimation of the activation energy Q for the growth process of Ni_3Sn_2 phase (with experimental results for only two temperatures!) leads to Q $\sim$ 50 kJ/mol. This value is very close to activation energy of the growth of Ni_3Sn_4 phase in the Ni/ Ni_3Sn_4/solid Sn system in the temperature range 150-210°C phase (Q = 53 kJ/mol) determined in Chapter 3. These results suggest that the rate controlling step of the Ni_3Sn_2 growth in the Ni/Ni_3Sn_4/δ-$AuNi_2Sn_4$ system, for reaction times shorter than 1000 hrs at 200°C, is the grain boundary diffusion process.

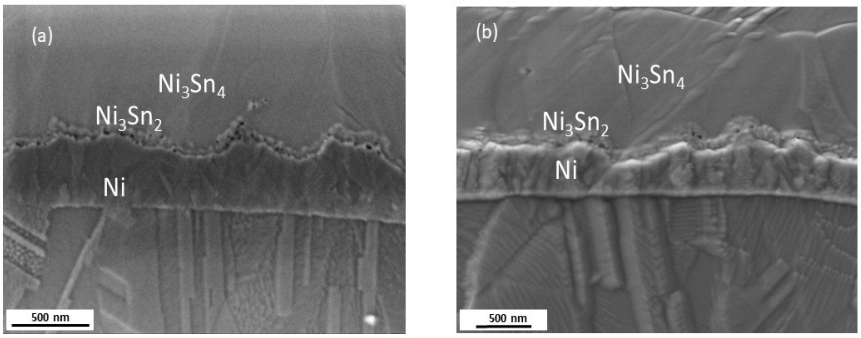


Figure 4.31: SEM micrograph for Sn interconnect (process A) showing the interface between Ni and Ni_3Sn_4 after annealing for 200hrs at (a) 175°C and (b) 200°C

Evolution of IMC interconnect with aging

Ni / Ni_3Sn_4 / Ni

The same phenomenon has been observed in case of aged IMC interconnects (Ni/Ni_3Sn_4 (+δ)/Ni system, process B) also. After 200 hrs of annealing at 200°C, 120 nm of Ni_3Sn_2 layer is formed as shown in Figure 4.32 (and the thickness of Ni_3Sn_4 layer is about 3 µm). The number of voids in the joint have increased, the neck in the interconnect (discussed earlier in this chapter) becomes deeper, although no change is observed in side wall wetting.

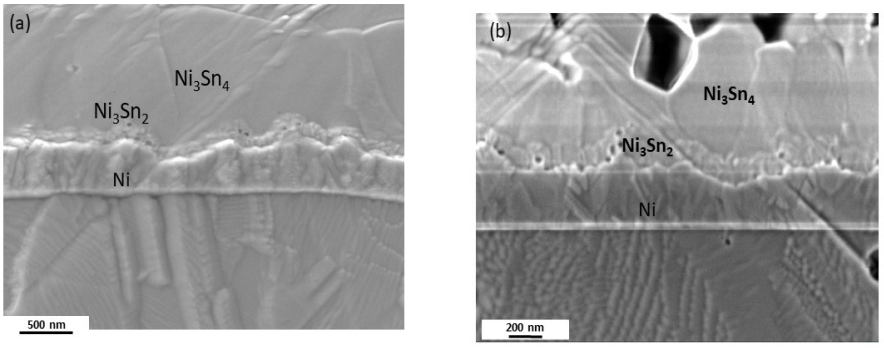


Figure 4.32: SEM micrograph for interconnects showing the interface between Ni and Ni_3Sn_4 after annealing for 200 hrs at 200°C for (a) Sn interconnect (process A) and (b) IMC interconnects (process B)

Discussion

The growth of Ni_3Sn_2 layer in Ni/Ni_3Sn_4/Ni (or Ni/Ni_3Sn_4 (+δ)/Ni) system at 200°C is not studied here for various time to determine the kinetic growth coefficient k and the growth exponent n. It would be very interesting to determine the time needed for aging Ni/Ni_3Sn_4 system at a given temperature (for example 200°C) after which the nucleation and growth of Ni_3Sn_2 phase occurs at the interface. We recall that, it is reported in the literature that this layer can only form and grow for temperatures above 200°C, suggesting that the nucleation barrier energy for this phase is very high.

In Chapter 3 we have shown that Ni_3Sn_2 phase do not grow at Ni/Ni_3Sn_4 interface in the Ni/Ni_3Sn_4/Ni system after 4 hrs of annealing at 200°C (and 210°C). In this section we have shown that Ni_3Sn_2 phase forms and grows at Ni/(Ni_3Sn_4 + δ–$AuNi_2Sn_4$) interface after 24 hrs at 200°C. However, it is important to point out here that in chapter 3, for solid state interactions, the Sn was left in the bump, thus the growth of Ni_3Sn_4 layer is still possible by reaction between Ni and left Sn. In this case, since both interconnect systems has been completely transformed into Ni_3Sn_4 and no Sn is left for further growth of Ni_3Sn_4 phase, the nucleation and growth of Ni_3Sn_2 and or Ni_3Sn phase(s) becomes the only way for the system to evolve under these conditions (i.e. isothermal heating).

However, to what extent the annealing time and/or the presence of δ-$AuNi_2Sn_4$ particles inside the Ni_3Sn_4 layer and/or the presence of Au dissolved in Ni_3Sn_4 phase influence the nucleation and growth of Ni_3Sn_2 phase in this system, is an open question. The answer to this question is very important not only from a fundamental point of view but also from a practical point of view which is linked with the stability of the metastable Ni/Ni_3Sn_4 interface at temperatures lower than 200°C.

4.3 CHARACTERIZATION OF FORMED INTERCONNECTS

4.3.1 MECHANICAL CHARACTERIZATION

As discussed in Chapter 1, the presence of IMC is not desirable, as they are known to be brittle in nature. The presence of voids which may be Kirkendall voids or voids due to volume contraction can further weaken the interconnect joint [161]. In the IMC interconnect (process B, see Figure 4.15 (b)), we may have both issues, the joint is completely transformed in IMC and it contains some voids due to the volume contraction. In addition to these common issues, some morphological defects are present in the IMC joint, i.e. the presence of a neck which reduces the bond area between Cu pillars and pads. All these parameters may potentially weaken the joint mechanically. However in the other interconnect (process A, see Figure 4.15 (a)), i.e. Sn interconnect, no such voids or geometrical defects are observed but a ternary $AuNi_2Sn_4$ IMC containing Au is present. Although, this ternary IMC is not well studied in the literature, Au is known for causing embrittlement in the interconnect joint [162]. Therefore, it is mandatory to investigate what would the rupture points in each type of interconnects be and at which stress values do they break.

For fine pitch assembly application, the assembly is usually within different substrates as described in Chapter 1. Different substrates causes coefficient of thermal expansion (CTE) mismatch, which induces additional stress in the package (as described in Chapter 1). This stress can either be released or endured by the interconnect. For the first case, the interconnect material should be ductile and the interconnect joint will undergo plastic deformation to release the stress of the package, while in the second case the material should be stiff, that is, should withstand the stress without failure. Both cases may be advantageous given the right application. The interconnects developed by process A, contains some left Sn inside the joint, which is a soft material, thus may have ductile properties, however they may not be able to endure the stress. On the other hand, interconnect developed by process B, has a IMC joint, which has high Young's modulus (see Table 4.3), i.e. may withstand higher level of stress, although may not be able to undergo any deformation without failure.

Table 4.3: Young's modulus and CTE of materials present in the interconnect [41, 163]

Mechanical properties	**Si**	**Sapphire**	**Ni**	**Sn-Ag**	**Ni_3Sn_4**
Young's Modulus (GPa)	170	350	210	50	160
CTE (ppm/°C)10^{-6}	3	7	13	21	15.5

The mechanical properties of each interconnect are estimated first by a very simple modelling and afterwards are evaluated by shear stress test.

Simple modeling of constraints distribution inside a heterogeneous Si / sapphire joint

As it is already mentioned in Chapter 1, microdisplays are fabricated on sapphire, however the package is on Si substrate, thus the interconnects would be formed between Si and sapphire.

This kind of package will have additional stresses due to CTE mismatch (see Table 4.3), and therefore it is important to evaluate those stresses within the package. Also the type of interconnects used for this kind of packaging, will impact the overall stress in the package. Thus a very simple preliminary modelling by COMSOL is performed to estimate the stresses within the package due to different metallurgy of interconnect. For modelling, the package is simplified and calculations are done for one single interconnect which is 5 µm in diameter. Figure 4.33 shows the schematic configuration of the system used for modelling. The two different substrates chosen for this study are Si and sapphire. Two types of joints with 3 µm thickness are considered which are Ni_3Sn_4 IMC joint and Sn joint. The Young modulus used for the materials present in the package, are given in table 4.3 [163]. Here, only elastic deformation is considered and the interface between different layers is assumed to be perfect and without any voids or cracks.

The elastic deformation of the joint is performed by clamping the Si substrate and performing a forced displacement of the sapphire. The reaction force on the Si due to the given displacement is calculated and shown in Figure 4.34 (a) and the stress map within the interconnect after 1 µm of displacement on sapphire is given in Figure 4.34 (b). According to this model, 66% more force should be applied to IMC interconnect as compared to Sn interconnect to have the same amount of displacement. Thus IMC interconnect is stiff and endure more stress than Sn. However, package with Sn interconnect shows 40% less stresses than IMC interconnect (as shown in Figure 4.34 (b)), thus Sn interconnect can release the stresses of the package. It is important to note that only elastic deformation is considered here whereas in practice plastic deformation will also play an important role. The modelling of this behavior being much more complex and out the scope of this study, the failure limit is determined experimentally.

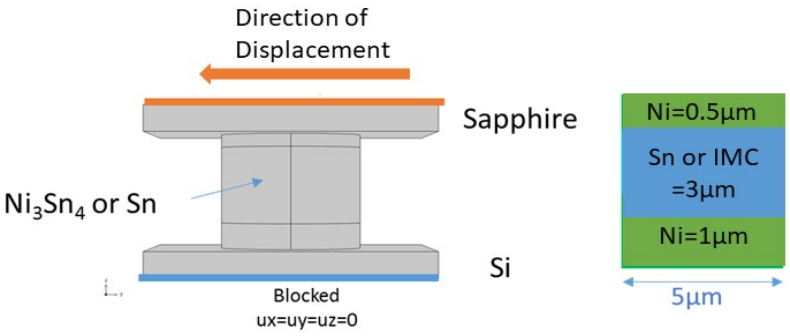


Figure 4.33: Schematic configuration for simplified interconnect used for theoretical modelling of stresses inside the joint

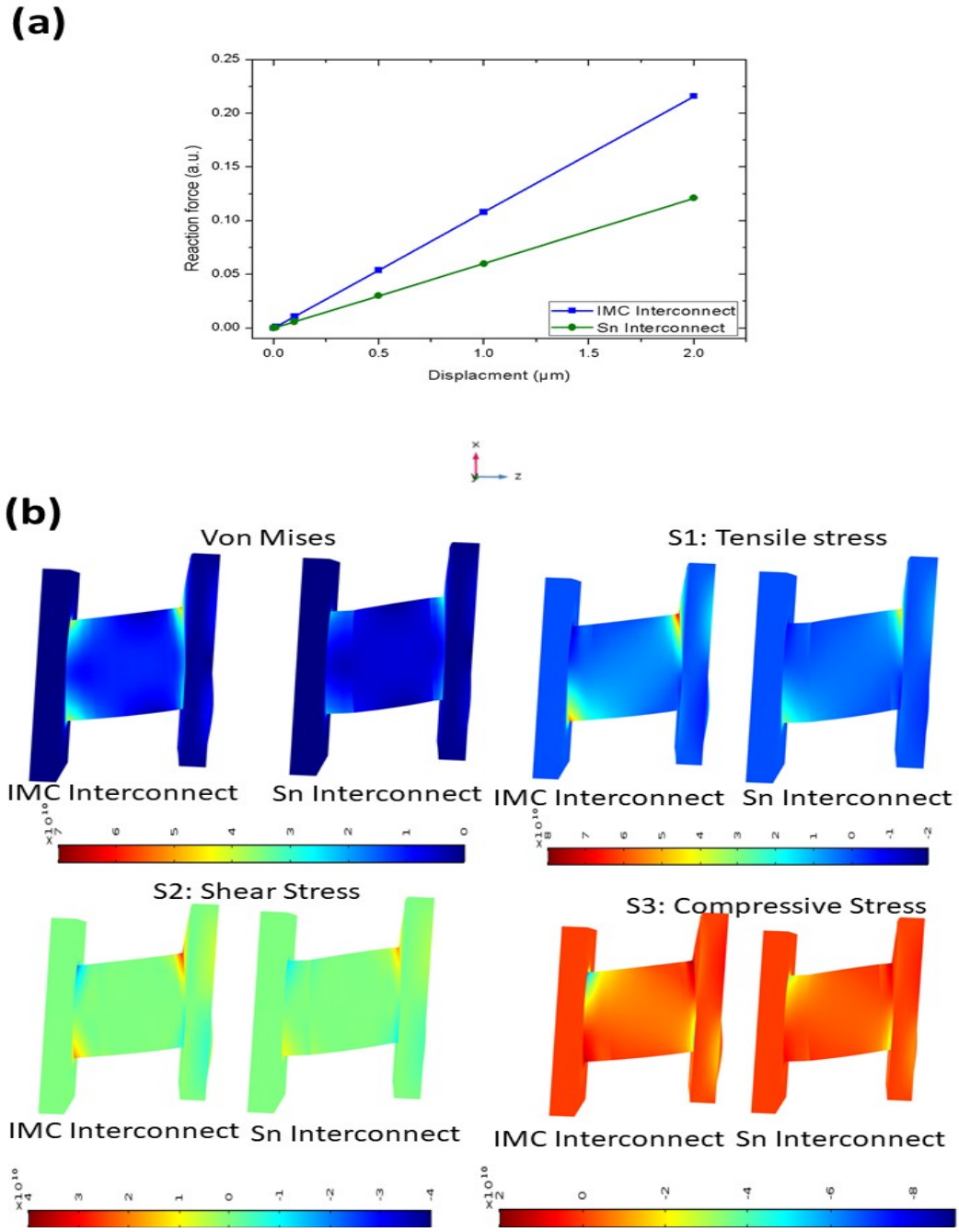


Figure 4.34: (a) Variation of the calculated reaction force with displacement. (b) Comparison of stress maps between IMC and Sn interconnect with 1 μm of displacement

Shear stress tests of Sn interconnects (process A) and IMC interconnects (process B)

To study the mechanical behavior and the force required for complete failure of interconnects, shear test is performed. The schematic for performing shear test is shown in Figure 4.35. A total of 10 samples for each process are tested by shear test. The key parameters for the shear test are the shear height (h) and the shear speed or displacement rate (v). These parameters

are fixed for shear tests for both interconnects (h = 50 µm and v = 50 µm/sec) and on the basis of the results a comparison is drawn. The results for the shear test are shown in Figure 4.36, which gives the variation of the shear stress with the displacement until the rupture.

The green curve in Figure 4.36 shows the rupture force for Sn interconnects. The maximum force came out to be 150 ±50 N, thus the corresponding shear stress required for rupture is 93±25 MPa (about $8x10^4$ interconnects 5 µm in diameter). To analyze the rupture point, both pads and Cu pillars sides of the sample are analyzed with SEM. From the analysis on the pad side (Figure 4.37), we can see some pads with sheared solder, some pads with IMCs and some delaminated Cu pillars on the pads. This is re-confirmed by EDX analysis for both top (Cu pillar side) and bottom chip (pad side) as shown in Figure 4.38. These observations suggest that the rupture surface is either the interface between Sn and Ni_3Sn_4 or Cu undercut. Statistically, 10% of interconnects sheared at Cu undercut, whereas all others were ruptured principally from Sn/IMCs interface and a minority from Ni/IMCs interface. The rupture mode seems to be rather brittle.

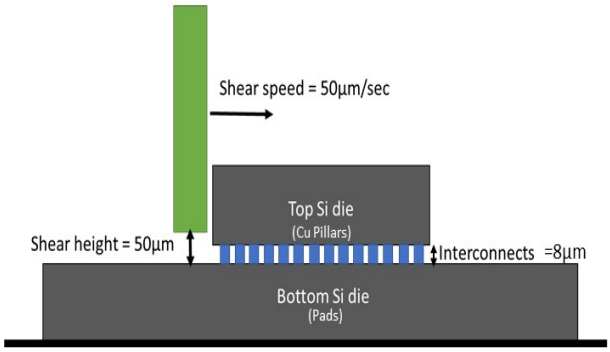


Figure 4.35: Schematic diagram for performing shear test

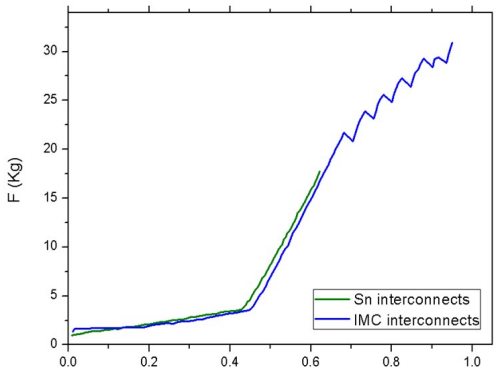


Figure 4.36: Profile for force required to rupture vs displacement (experimental result for shear test)

In Figure 4.36, the blue curve shows the behavior for IMC interconnects. The maximum force required to break these interconnects is 250±50 N corresponding to a shear stress of 155±25 MPa. SEM analysis of the pads side from these ruptured interconnects, are given in Figure 4.39. As in the case of Sn interconnects, the rupture seems to be brittle. 3 rupture points can be observed from this figure: (i) within Ni_3Sn_4 IMCs, (ii) due to delamination at Cu undercut

and (iii) rupture due to Ti/Ni/Au pad delamination. The first two rupture points are similar to the previous case (Sn interconnects) whereas the pad delamination is observed only for IMC interconnects. This behavior may be due to the low thickness of Ti layer used for these test vehicles (20 nm), compared to a Ti layer 100 nm thick normally used as an adhesion layer, thus leading to a weaker adhesion with the Si/SiO_2 wafer. Statistically in this case, the 10% of shearing occurred at Cu delamination, 40% at Ti/Ni or Ti/SiO_2 interface and 50% within Ni_3Sn_4 IMCs. The fact that in only about 50% of cases the rupture of IMC interconnects occurs between IMCs, suggests that the shearing stress corresponding to Ni_3Sn_4 IMCs (and Ni/Ni_3Sn_4 interfaces) should be significantly higher than 155 MPa.

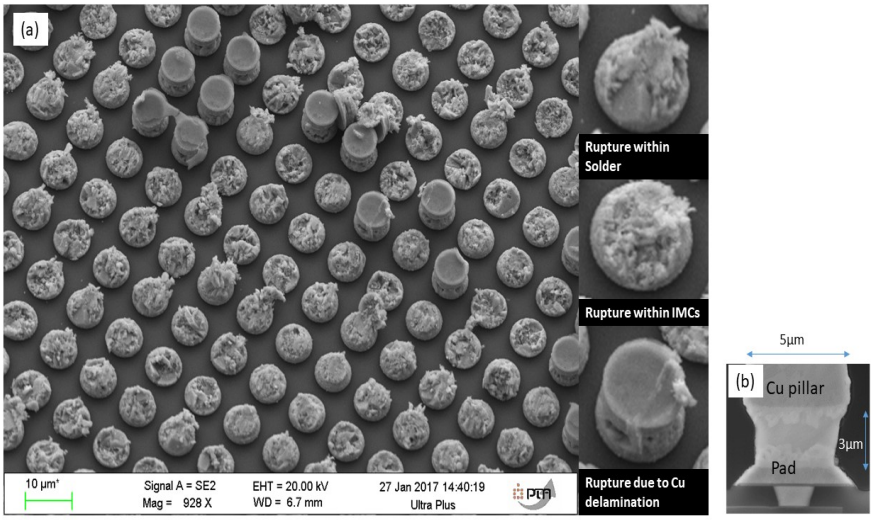


Figure 4.37: (a) SEM micrograph for Sn interconnect (pad side) after shear test, showing various rupture point, (b) SEM micrograph of a single interconnect showing the Cu pillar and pad sides

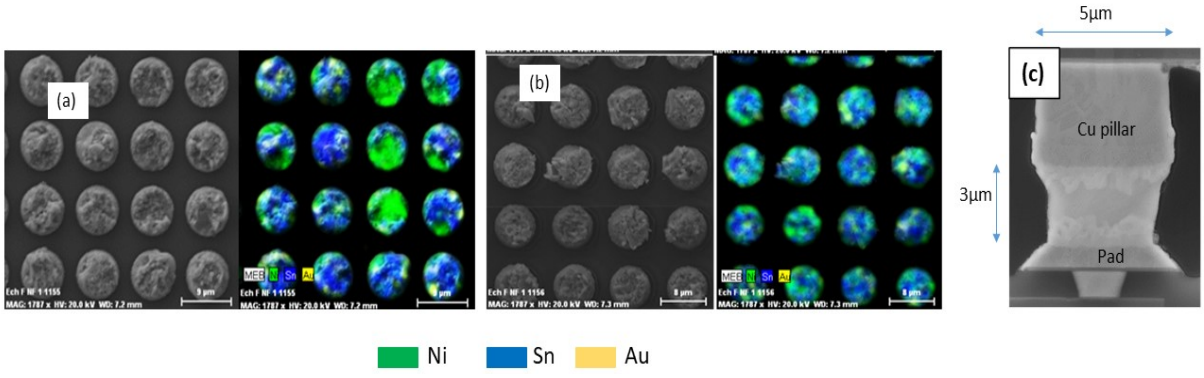


Figure 4.38: SEM micrographs with EDX cartography for Sn interconnects (a) Cu pillars side and (b) Pads side (c) SEM micrograph of a single interconnect showing the Cu pillar and pad sides

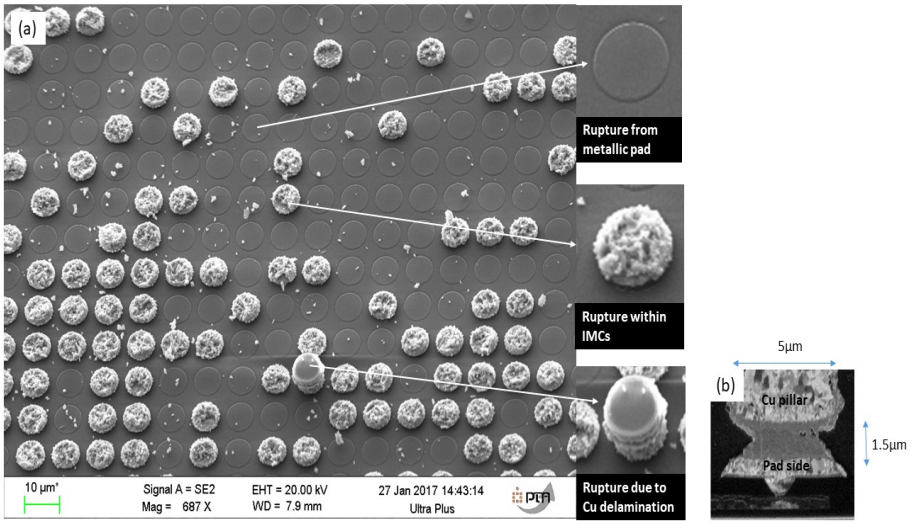


Figure 4.39: (a) SEM micrograph for IMC interconnect after shear test, showing various rupture points (pad side), (b) SEM micrograph of a single interconnect showing the Cu pillar and pad sides

Note that no precise data exists in the literature on the mechanical behavior of Ni/Sn/Ni interconnects. Moreover, no experimental data exists on the shear strength of Ni_3Sn_4 compound. However, the high value of Young's modulus for Ni_3Sn_4 (160 MPa) strongly suggests that the shear strength of Ni_3Sn_4 compound will be high.

The value of the shear strength determined here for Sn interconnect (93±25 MPa) is close to that reported by Bertheau et al. [48] for Cu_3Sn/Cu_6Sn_5 and Cu_6Sn_5/Sn interfaces (119±11 MPa). They performed shear tests for 25 µm diameter Cu pillar/Sn bump system undergoing isothermal holdings up to 30 mins at 240°C by using a shear speed of 70 µm/s which is close to that used in our study (50 µm/s).

In the literature, the shear stress for 25 µm pitch assembly with Sn solder alloy for Sn interconnects was measured by [164, 165] who performed tests with shear speed of 100 µm/s. They reported a shear stress of about 18 MPa which is much lower than that obtained in our study (93±25 MPa). However, the shear test speed performed on the assemblies done by [164, 165] is twice higher than ours, also the metallurgy is not the same, which may explain the difference in the value. Nevertheless, our interconnects show relatively better mechanical behavior in terms of mechanical resistance.

The shear strength for 10 µm pitch assembly with Sn solder alloy for IMC interconnects concerning bonding between Cu and Sn is reported between 15-40 MPa by [56, 59], which is much lower than what is obtained in this study (155±25) MPa. Here also the metallurgy of the joint is completely different compared to our case. Moreover in all these studies the used shear speed is not specified. It is well known that the value of the shear strength strongly depends on the shear speed (see for example the reference [48]).

However, even if the comparison of our results with the literature cannot be done because of lack of data, from the experimental results obtained in this study, it is clear that the IMC

interconnect is more resistant towards mechanical stress than Sn interconnects.

4.3.2 ELECTRICAL CHARACTERIZATION

After doing mechanical analysis, electrical characterization of interconnects is done. The main function of the interconnects in the package is to provide an electrical pathway between the different devices. On doing so, the voltage drop between the applied voltage and the actual voltage on device should be as minimum as possible, otherwise the device would require more power to work. Therefore, the interconnects should have as low resistance as possible. Thus, electrical characterization of the interconnects for wafer level packaging is crucial and usually determined by the yield of the assembly. The yield is 100% if all the connections are connected and the resistance of the interconnect is lower than the allowed resistance. The allowed resistance is determined by the application for which it has to be used. Since the objective of this thesis is to evaluate metallurgy, therefore no minimum value for resistance was set. However, before determining experimentally, the theoretical resistance of the interconnect is estimated.

Figure 4.40 shows the schematic diagram of the metallic layers that are present in the interconnect. From the pad side, there is an electrical line made up of Al-Cu (R_1), then there is Cu damascene (R_2) which provides the connection between the chip metallization and the pad metal, and finally there is the pad itself which is made up of Ti, Ni and Au (R_3) (before bonding). After bonding Au layer and a part of Ni layer reacts with the solder on the pillar side to form the joint (R_4) and then there is the remaining Ni layer at pillar side which is not consumed and finally the Cu pillar (R_5) which is deposited over Al-Si electrical line (R_6). Each layer has its own electrical resistance and will contribute to the total resistance of the interconnect. The resistivity of each layer present in the interconnect is given in Table 4.4. However, no data on the resistivity of δ-$AuNi_2Sn_4$ exist in the literature, thus the resistivity of this layer is taken same as Ni_3Sn_4. The estimated resistance of Sn interconnect is 70 mΩ and for IMC interconnect is 87 mΩ. The main contributor of the resistance is/are Sn and IMC due to their higher resistivity.

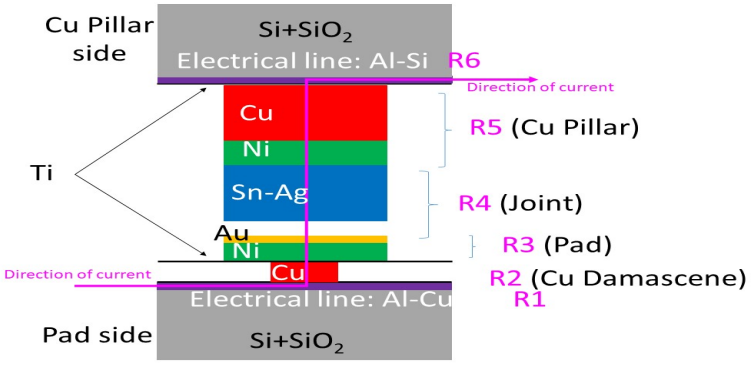


Figure 4.40: Schematics of metallic layers present in the interconnect

Table 4.4: Resistivity of materials present in the interconnect [41]

Material	AlCu / AlSi	Ti	Cu	Ni	Sn	Ni_3Sn_4	Ni_3Sn_2
Resistivity(Ω.µm)	0.035	0.43	0.022	0.07	0.125	0.285	9

After estimating, the resistance is measured by a manual prober. As mentioned in Chapter 2, the resistance of various number of Daisy chain over the same electrical line length is measured

and then the resistance of a single interconnect is computed. Through out the study we use this method to evaluate and compare the resistance of different interconnects. For this study, 30 samples from each process (A - Sn interconnect and B - IMC interconnect) are tested. The resistance of both types of interconnects is shown in figure 4.41. In this figure, the cumulative frequency percentage for the resistance is shown. Technically, a cumulative frequency distribution is the sum of the class and all classes below it in a frequency distribution. For example, in Figure 4.41 IMC interconnect resistance curve shows that for 18% (i.e. 5 over 30 interconnects) have resistance upto 175 mΩ. As it can be seen in this figure the resistance from both interconnects is very high (R = 175-275 mΩ for 80% of interconnects), approximately 2-3 times more than predicted. This strong disagreement between the estimated 70-87 mΩ and measured values of both interconnects resistance is certainly not due to the error on the evaluated values of average thickness and section of each layer shown in Figure 4.15, neither to the difference between the estimated and the true value of the resistivity of δ-$AuNi_2Sn_4$layer.

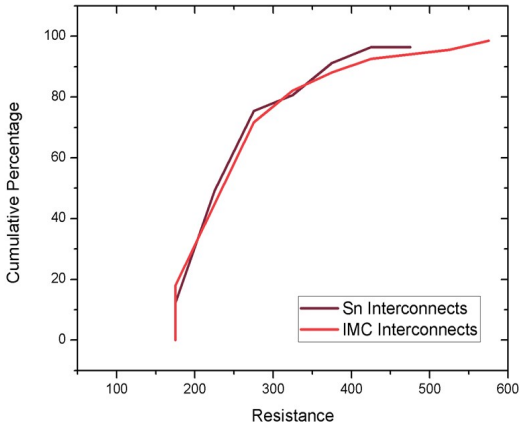


Figure 4.41: Graph showing resistance for interconnects at 10 µm pitch

The great difference between measured and estimated resistance can be mainly due to two reasons.

1. In the theoretical calculations of electrical resistance of interconnects, we assume that the contact between different layers is homogeneous, continuous and flat. However in reality it may not be continuous, thus the effective contact area in between layers will be less than what it should be. As explained in Ref [166], this non–uniform contact leads to a resistance increase (R_c). It is generally reported in the literature as the contact resistance so that the total resistance for two metallic layers 1 and 2 (with resistance R_1 and R_2 respectively) is $R=R_1+R_2+R_C$.

2. The resistance can also increase if there is a thin continuous (or not) oxide layer present within the contact of these layers, which may be due to the fabrication process. The fabrication of the wafer is not a single step process, it contains multiple deposition steps of various metal layers (as shown in Figure 4.40). At times between two fabrication steps, there is an air break i.e. wafer is exposed to ambient environment in between the deposition of two metallic layers. In this case a pre-cleaning is done to remove the oxide on the metallic layer, before depositing another metallic layer. During the fabrication process of the wafers used in this study, there were number of air breaks for the bottom wafer (pad side) as for example an air break before Cu damascene process. For the top

wafer (Cu pillar side), there is one air break between the depositions of Cu pillar on top of Al-Cu electrical line. If the pre-cleaning is not optimized for any of these steps, then there might be a thin oxide layer present in between the adjacent layers, which acts as a cause for higher resistance [167].

These hypothesis are supported experimentally by testing the electrical resistance between different metallic layer at wafer level (pad side) after fabrication and before bonding. In the electrical design, there are some test patterns made to qualify the fabrication process (shown in Figure 4.42).Through those patterns we can pin point the potential issue in the fabrication process. The results of this test show that the problem is indeed in the contact resistance between different deposited layers and not in the joint itself. For example, the calculated resistance of the electrical line from the pad side is 14 mΩ, whereas the measured resistance is coming out to be around 150 mΩ on average. Despite the fact that the structure of the test pattern is not exactly similar to that of the pads used in the interconnects, this result gives us an idea about the magnitude of the resistance of the structure whose major contribution could be due to AlCu-Ti-Ni contact resistance. Unfortunately, the same test at wafer level was not possible for the top wafer i.e. wafer with Cu pillars.

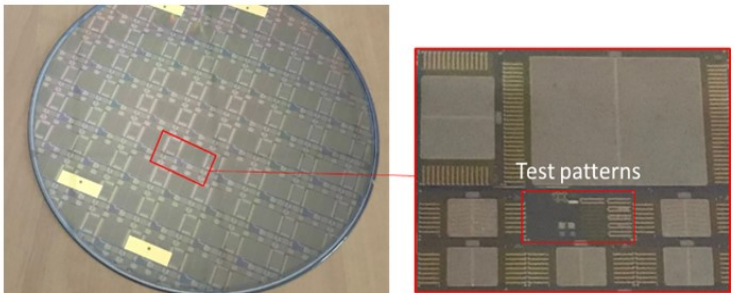


Figure 4.42: Electrical test pattern on bottom wafer (i.e. pad side) to characterize fabrication process

Figure 4.43 compares the measured resistance for 30 samples of pad wafer and the measured resistance for 30 samples of both types of interconnects. This figure clearly shows that if we subtract this resistance of pad from the measured resistance of interconnect, then the obtained values ($\sim$ 70-150 mΩ) are much closer to the theoretical value of interconnects ($\sim$ 70-90 mΩ). It would be further closer to the theoretical value, if we took into account the unknown contact resistance coming from the top wafer.

Other important thing to state here is the high dispersion in resistance observed for both interconnects (Figure 4.41 and Figure 4.43). This could be principally due to the dispersion of the contact resistance becoming from pad side. This may also be due to the fabrication process, which brings us to the important issue with the fabrication of electrical wafer. For Cu damascene process, an opening is done in passivation (i.e. SiO_2) and then seed layers (Ti/TiN) is/are deposited over the chip metallization (Al-Cu/Ti/TiN) and then Cu is electroplated on top of these layers. If the opening is not proper or uniform throughout the wafer, then there will be difference in contact resistance throughout the wafer. Thus, at some places the contact between electrical line and the interconnect may be reduced, causing high resistance therefore overall high dispersion.

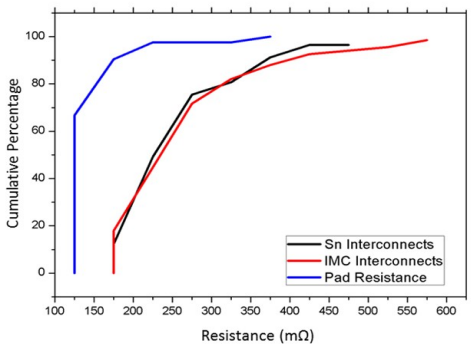


Figure 4.43: Graph showing resistance of just pad and the interconnects

4.3.3 RELIABILITY

After characterizing the interconnects in terms of metallurgy, mechanical and electrical resistance, the interconnects now should be tested for reliability. Reliability study for a package gives information about its lifetime functionality. Depending upon their usage, a package is tested for a given set of condition in which it will be used. Usually these conditions are accelerated in order to speed up the degradation process, and based on the results a probability model is made, which can predict the life time of the package. There are number of reliability tests such as humidity test, shock test, high temperature storage test, electromigration test etc.

As said before, the reliability studies for the package are done for the specific conditions depending upon their application. However, no such specific application is specified for the developed interconnects in this study. Nevertheless, we do know for the fact, that during the operation of any device (except cooled IR detectors or such devices), heat is generated during its operation and that heat is enough to change the metallurgy of the interconnect [168], which is the focus of the thesis. Thus a high temperature storage test is chosen to test the developed interconnects.

In high temperature storage test, the package is stored at high temperature until it fails, so that a failure criterion must be chosen. The failure criterion in this test is usually a given increase of the resistance (typically 20%) in between the interconnects. This increase in resistance is generally due to the growth of IMC layers (at the expense of Ni and Sn-Ag layers), to the formation of new IMC layers as well as to the formation and growth of Kirkendall voids [169].

In the following we will first study the evolution of the electrical resistance of both interconnects during aging and afterwards we will perform some failure analysis based on the experimental results issued from electrical resistance measurements.

Evolution of Electrical Resistance due to Aging of Interconnects

In the previous section, the evolution of metallurgy in Sn and IMC interconnects during isothermal holdings is studied. This study shows the growth of Ni_3Sn_4 and δ-$AuNi_2Sn_4$layers, the formation and evolution of a new Ni_3Sn_2 phase layer, when interconnects are heated at three temperatures, 150°C, 175°C and 200°C till about 1300 hrs. It is interesting to study how the

heat treatments and, in particular, the formation of this new Ni_3Sn_2 layer affect the electrical resistance of interconnects.

For this study, 7 samples for each condition (i.e. temperature and process A and B) are picked. The annealing is then done in ambient environment, followed by characterization by measuring electrical resistance. The resistance is measured after 24 hrs, 48 hrs, 96 hrs and then after every 100 hrs of annealing until the device fails, which in our case is defined as complete loss of connectivity (open circuit).

The change in resistance of Sn interconnects and IMC interconnects as a function of aging time at various temperature is shown in Figure 4.44. Two main remarks can be made from this figure:

1. In general a *decrease in resistance* is observed for all configurations. The resistance decreases up to 75% for 175°C and 200°C after 100 hrs of annealing and then this drop gets stabilized, whereas for 150°C the drop is gradual and is still ongoing (so far 1300 hrs of aging has been completed - not shown in Figure 4.44). This was not foreseen before the start of this study.

2. A manifestation of *open circuits* (which indicate failures) is observed in these interconnects.

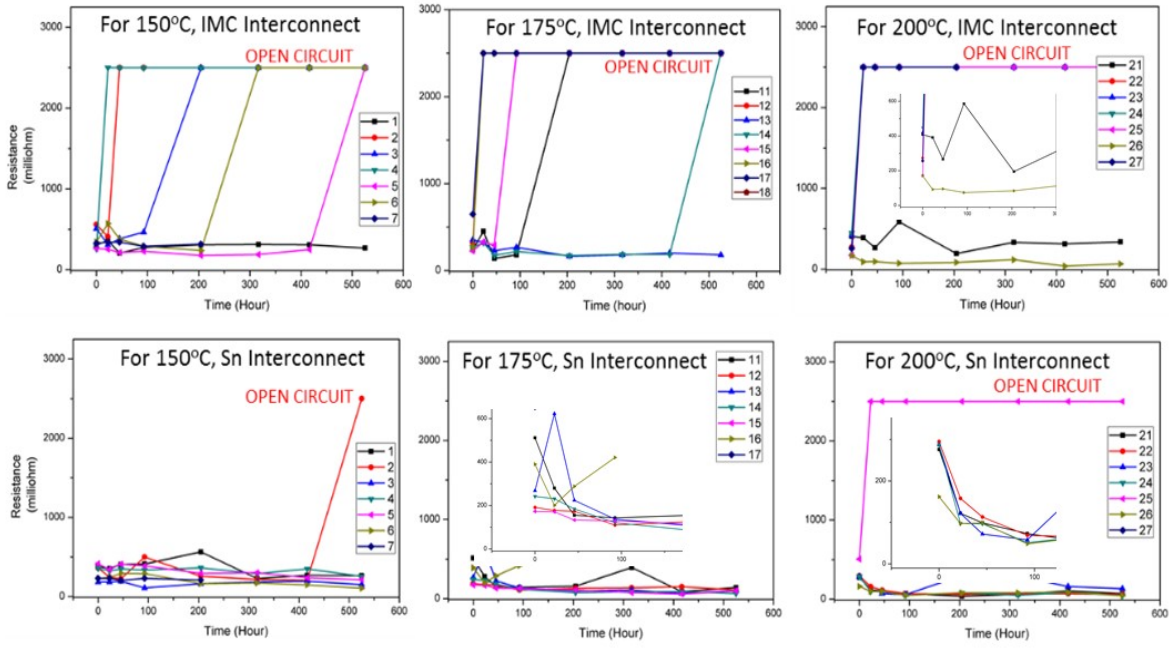


Figure 4.44: Resistance graphs showing change in resistance for former Sn interconnects and IMC interconnects after annealing at 150, 175 and 200°C. Numbers in the legend represents the sample name

Here below we will analyze both these points.

Decrease in resistance

From the micrographs of both Sn and IMC interconnects, some nanometric voids are observed after 24 hrs of aging at 200°C (see Figure 4.28 and Figure 4.32) which should normally lead to an increase in the resistance of the interconnect. Secondly, for both interconnects, the growth of Ni_3Sn_2 layer by reaction between Ni and Ni_3Sn_4 will lead also to a significant increase in the resistance of the interconnect given the fact that the resistivity of Ni_3Sn_2 phase is about 30 times higher than the resistivity of Ni_3Sn_4 phase, according to a very recent study of Xian et al [170]. This abnormal behaviour for resistivity of Ni_3Sn_4 phase according to the authors, is attributed to the short-range order correlations arising from the geometrical frustration (frustrated materials are interesting because their physical properties are difficult to predict). Thus, in all cases, the growth of IMC compounds will lead always in an increase of the resistance of the joint.

In the case of Sn interconnects, simple calculations by taking resistivity data from Table (4.4) and the fact that formation of 1 µm of Ni_3Sn_4 needs consumption of 0.86 µm Sn and 0.26 µm Ni (see Section 4.2.1), show that the growth of Ni_3Sn_4 layer by reaction between Ni and Sn atoms leads to an increase of the resistance of the Sn interconnect by 10 mΩ. The same tendency is expected during growth of the δ-$AuNi_2Sn_4$ layer for which no resistivity data exist in the literature.

This decrement of resistance in interconnect with the aging time (t_d), (where time t_d depends on the aging temperature) contradicts our expectations. In order to understand this decrease in the resistance of the interconnects during annealing, we again electrically test full bottom wafer (i.e. with pads) before hybridization (joining process), but this time the wafer was first reflowed using the same temperature-time profile as used for bonding and then annealed at 175°C for about 100 hrs. The comparison of contact resistance before and after annealing is presented in Figure 4.45 , which clearly shows that during the annealing process, there is a decrease in resistance of about 75% (from ∼125 to ∼60 mΩ). This result supports once again our previous assumption that the high resistance is due to the contact between different metallic layers and not from the joint as such (after bonding). This decrease in the contact resistance of Ti/TiN/Al-Cu line during the annealing could be due to the fact that interdiffusion at higher temperatures can lead to a significant improve in the electrical contact between these layers which has been prevented from surface oxides for example.

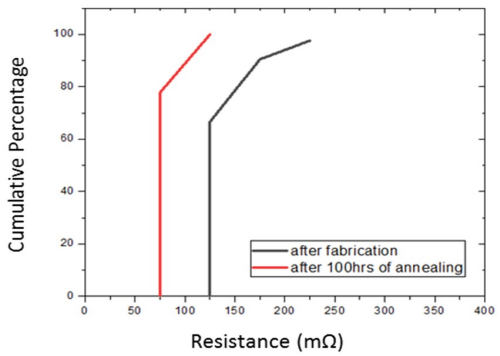


Figure 4.45: Graph showing decrement in the resistance of just pad after 100 hrs of annealing at 175°C

B. Open circuits (failure)

Open circuits corresponds to the failure due to annealing. The cause of failure in both interconnects is due to emergence of cracks in the interconnect. For the IMC interconnect, the cracks occurred in between the joint, whereas for Sn Interconnect, the cracks occurred at two regions, (a) in between the joints and (b) within the Cu pillar.

(a) Failure due to evolution of cracks in between the joint:
As described in chapter 2, our electrical test vehicle has many test groups across the chip, uniformly distributed. Thus with our test groups, we can locate the initiation and the propagation of the failure by detecting the position of the open circuits through the chip. In this study we chose 3 test groups at different locations, one at the edge of the chip, the second situated almost at the center of the chip and the third one in the middle as it is schematically shown in Figure 4.46 (a). (Interconnects in the yellow zone cannot be electrically measured). By measuring the resistance of different test groups, we found that the failure started from the edge of the chip and propagated towards the center of the chip as shown in Figure 4.46 for IMC interconnects (i.e. for annealing times lower than 200 hrs, open circuits are observed only on the test group 1, situated at the edge of the chip, and for longer aging times they are observed also on the test group 2, at center of the chip). Thus, *a sudden increase in resistance after aging at certain time is observed for IMC interconnects and even for very few cases of former Sn interconnect*. The statistics of these type of failure after 500 hrs of aging varies a lot. For IMC interconnects, 6 samples (over 7) fail at 150 and 175°C and 5 samples at 200°C, while for Sn interconnect, only 1 sample fails at 150°C and 200°C and no sample fails at 175°C.

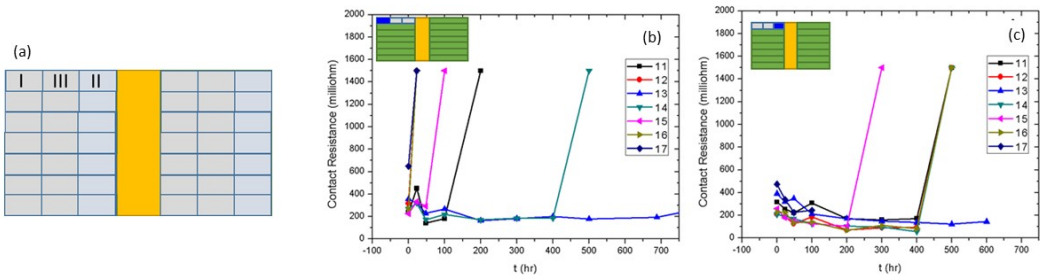


Figure 4.46: (a) Schematic diagram for the test groups across the chip tested for characterization after High Temperature Storage test, (b) variation of the resistance of IMC interconnect with annealing time at T = 175°C at test group I and (c) at test group II. (The blue rectangle indicates the position the examined test group and numbers indicate the sample name)

Cross-sections are done for each failed sample of IMC and they are analyzed with SEM. Figure 4.47 shows some cross-sections for IMC interconnects, situated at the edge and at the center of the chip, after aging for 200 hrs at 150°C. As it can be seen in Figure 4.47 (a), for interconnects situated at the edge of the sample, the cracks are present at the same plane where the neck in joint was previously present before annealing (see Figure 4.15 (b)). In Figure 4.47 (b), the cross-section of the same sample but at the center of the chip shows no cracks. The same behavior can be also seen for former Sn interconnects (see Figure 4.48).

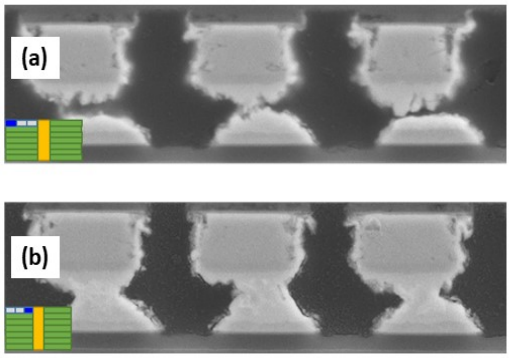


Figure 4.47: SEM micrographs for IMC interconnects after 200 hrs of annealing at 150°C at the interconnects at the edge of the chip. The blue rectangle indicates the position the examined test group across the chip

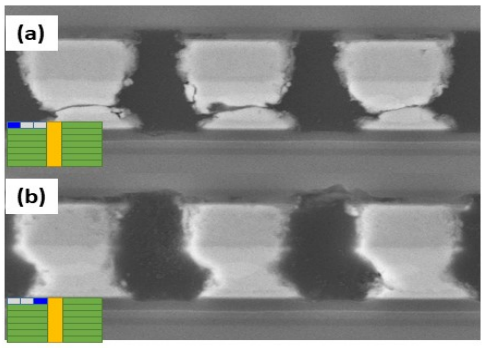


Figure 4.48: SEM micrographs for former Sn interconnects after 200 hrs of annealing at 150°C (a) at the interconnects at the edge of the chip (b) at the center of the chip. The blue rectangle indicates the position the examined test group across the chip

This kind of failures is usually due to thermo-mechanical stress [171], such as CTE mismatch. However, if it is a simple CTE mismatch, then we must see misalignment after bonding also, which is clearly not the case here. Thus the problem is much more complex and more work is needed to understand it.

(b) Failure due to cracks in Cu pillar

As seen from Figure 4.49, which gives the resistance curve for Sn interconnects after different annealing time, the major failures for Sn interconnects occurred much later than in the case of IMC interconnect. After 1000 hrs of annealing the number of samples that failed at 150, 175 and 200°C was 0/7, 2/7 and 5/7 respectively. These failures for Sn interconnects are also due to open circuit, however *no gradual increase in resistance* was observed here and the nature of the failure at 200°C is different from what was observed for IMC interconnects. The failures did not start from the edge of the chip and propagate towards the center of the chip (as it was the case for IMC interconnects), but they occurred suddenly.

Figure 4.50 shows the cross-section of Sn interconnect aged at 200°C for 1300 hrs. In this figure, some big voids are seen on the Cu pillar, and few cracks such that there is no contact between Cu pillar and electric line. This indicates the corrosion of Cu pillar. The EDX analysis

also showed Cu oxide at the side of Cu. This is also reconfirmed by doing some additional treatment on the cross-section, such that the grains of different material are exposed. In Figure 4.50 (b), the grains of Cu pillar are visible at the center, however the zone close to the wall of Cu pillar shows different granular structure, suggesting Cu oxide.

In this case the failure is not due to failure within the joint of interconnect but due to Cu oxidation. Thus, this is not a consequence of the evolution of metallurgy. This type of failure as well as the thermomechanical failures may be prevented by the use of underfilling.

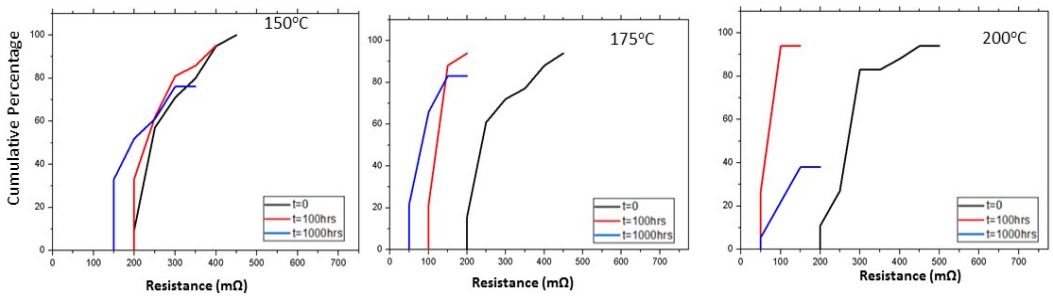


Figure 4.49: Resistance curves for Sn Interconnects at different annealing time

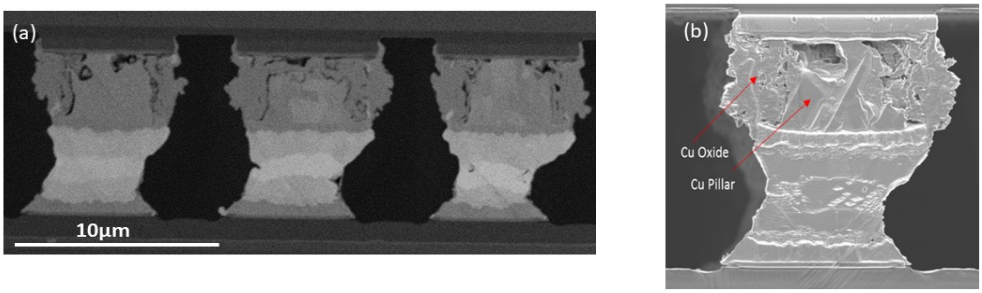


Figure 4.50: SEM micrographs and with contrast for Sn interconnects aged at 1303 hrs at 200°C, showing Cu corrosion

CONCLUSIONS

Formation of interconnects at 10 µm pitch was studied. Generally reflow is the first step of assembly process followed by bonding. However in this case, prior reflow is no longer recommended as it reduces the available Sn for bonding. Nevertheless, the reflow behavior seem to be interesting. SF_6 etching which is used to remove the Ti seed layer altered the Sn surface and prevented it from getting reflowed, i.e. forming a spherical shape in inert atmosphere, which is otherwise possible for pillars which are not seed etched. In order to have a spherical shape, flux must be used. Secondly, when temperature-time profile was changed and a plateau was introduced, then Sn was observed on lateral Cu walls due to spilling. This gets further enhanced when flux was used. This bump was called Hedgehog Bump.

For bonding, 2 processes were designed such that in one process least IMC was formed (i.e. Sn interconnect) whereas the other profile was such that whole joint is converted into IMC joint

(i.e. IMC interconnect). The formation of these interconnects was studied from the metallurgical point of view. For Sn interconnects the system configuration is Ni/Ni_3Sn_4/δ-$AuNi_2Sn_4$/Sn/ δ-$AuNi_2Sn_4$/Ni_3Sn_4/Ni and for IMC interconnect it is Ni/Ni_3Sn_4/Ni with either dissolved or nanometric precipitates of δ-$AuNi_2Sn_4$phase inside Ni_3Sn_4 layer.

On aging these interconnects Ni_3Sn_2 layer was observed which appeared at 200°C after 24 hrs and became continuous after 48 hrs of annealing. From then, it grew uniformly with growth exponent n=0.3. This layer was accompanied with nanometric voids of the same size as the size of the grains in this layer. These could be due to surface preparations while polishing. According to a work reported recently in the literature, the resistivity of Ni_3Sn_2 is 30 times higher than Ni_3Sn_4. However, in our study, due to the decrement of resistance during annealing, it was not possible to estimate the resistivity of Ni_3Sn_2 layer thus it still needs to be verified in the future.

Regarding the mechanical properties, the IMC interconnect has higher Young's modulus than Sn, thus it is more rigid and can be prone to brittleness, however, upon shear stress, it showed higher mechanical resistance than the later. In terms of electrical resistance, it is estimated theoretically that for Sn and IMC interconnects the value should be 70 mΩ and 87 mΩ respectively. However, the measured resistances were found to be much higher, between 175-275 mΩ with large variations. These high values were proven to be due to contact problems between the underlying layers because of fabrication process issues.

The evolution of resistance during aging of the interconnects were then studied. On annealing these interconnects at 175°C and 200°C for 100 hrs the contact resistance dropped to their estimated value, possibly due to improvement in contact between electrical lines and interconnect. Then no resistance increase was observed until dramatic failure. The IMC interconnect was found to be much less reliable with probability of failure 8 times higher than the Sn interconnect. In general failure starts at the edge of the chip and propagates to the center. The major failure for Sn interconnects was because of Cu oxidation thus indicating no specific weakness of the joint (Ni/Ni_3Sn_4/δ–$AuNi_2Sn_4$/Ni_3Sn_4/Ni). Thus from a metallurgical point of view this Sn interconnect seems to be well adapted for the 10 μm pitch assembly.

General Conclusion and Perspective

General Conclusion

In the first chapter, the overview of electronic packaging was given and the challenges associated with miniaturization of micro-electronic components were presented. In coming years, 10 µm pitch is going to be a reality and therefore the challenges associated with this pitch must be addressed. There are other promising methods such as Cu-Cu bonding, microtubes, however the major challenge associated with them is their adaptability. Therefore, the prospects for the traditional Cu/Ni/Sn-Ag microbumps which are well suitable to the electronic industry must be evaluated, which is the main aim of the thesis. While there are many challenges associated with this pitch, the thesis focused on the metallurgy of the bumps, its evolution with time during interfacial interactions and how this metallurgy affects the properties and the lifetime of the interconnects and finally the package.

In chapter 2, the test vehicles and their fabrication methods are presented. The issues encountered during the fabrication process are also listed with their possible solutions. All the analytical techniques used in the thesis for characterization of metallurgy as well as interconnects are presented.

In chapter 3, the initial state of Cu/Ni/Sn-Ag bumps (vehicle tests) were characterized followed by studying the melting behavior and microstructure of Sn-Ag alloy at 5 µm diameter. The melting behavior is characterized by Differential Scanning Calorimetry. It is found that after deposition, a thin and continuous Ni_3Sn_4 reaction layer is formed by solid state interaction between Sn and Ni during fabrication process and/or storage at room temperature. The thickness of this layer strongly depends on the fabrication process and it varies from 120 to 250 nm in this case. The melting of 5 µm diameter bumps occurs at about 222°C indicating that their average composition is not far from the eutectic composition. For the first time, an exothermic peak was observed just after the endothermic melting peak in the case of 5 µm diameter bumps (with initial thickness of Sn-Ag = 3 µm). This exothermic peak was not observed for 150 µm diameter Sn-Ag bumps (with initial thickness of Sn-Ag = 10-25 µm)and it was never reported in the literature neither for Ni/Sn bumps nor for Cu/Sn bumps. This is due to the very small thickness of Sn-Ag alloy involved during melting ($\sim$ 2 µm) and thus to a rapid and total consumption of liquid Sn by reaction with Ni which is at the origin of the observed exothermic peak.

Then, the interfacial reactions in solid Sn/Ni system were studied from experimental and theoretical point of view. For solid Sn/Ni interactions, the growth kinetics of the Ni_3Sn_4 intermetallic (IMC) layer for the initial stages of reaction follows almost a cubic growth law and the

apparent activation energy was evaluated to be of about 53 kJ.mol^{-1}. The growth of this layer occurs only by grain growth and grain coarsening for most of the annealing time (or for lower temperature and shorter time). Only for higher temperature ($\geq$200°C) and longer time (>4 hrs), the growth is also due to the nucleation of new Ni_3Sn_4 grains. The initial formation and growth of Ni_3Sn_4 phase at the solid Sn/Ni interface is studied by a theoretical thermodynamic and kinetic analysis. Based on this analysis and the experimental results, it was concluded that the rate controlling step of the Ni_3Sn_4 growth, for initial stages of reaction, is the grain boundary diffusion process. A simple model for evaluation of the grain boundary diffusivity in Ni_3Sn_4 compound is proposed and is used to determine the integrated diffusion coefficient in the Ni_3Sn_4 grain boundaries, which was found to be between about 10^{-16} to $4x10^{-14}$ m^2.s^{-1} and the average grain diffusivity 10^{-17} to $7x10^{-15}$ m^2.s^{-1}. The formation and growth of Ni_3Sn_2 phase in the solid Sn/Ni system was observed for the first time (after 4 days of reaction at 200°C). The formation of Ni_3Sn_2 phase could be possible only if the thickness of the first layer "vampire" Ni_3Sn_4 phase exceeds a critical value of 2µm.

In the last section of this chapter, the interfacial interactions between liquid Sn and Ni are studied. Here, a theoretical analysis of the initial formation and growth of Ni_3Sn_4 phase at the Ni/liquid Sn interface is presented and the role of the Ni/solid Sn interactions (during deposition and/or storage) on the morphology and the growth kinetics of Ni_3Sn_4 is discussed. As seen in solid state interaction of Sn with Ni, during the heating of Sn-based solders, with classical heating rates ($\sim$60°C.min^{-1}) from the room to the melting temperature, the Ni-Sn interactions are significant and may play a crucial role on the subsequent liquid Sn-Ni interactions during the reflow process. For longer reaction times (> 1 h) the scallop-like morphology of Ni_3Sn_4 reaction layer is transformed gradually to a facetted abnormal growth morphology but not elongated structure. The morphology of the Ni_3Sn_4 layer is found to be directly affected by the deposition of Ni/Sn-Ag diffusion couple, thus it should be controlled in order to avoid the formation of elongated needles of Ni_3Sn_4 phase which can strongly affect the integrity of micrometric sized joints. The growth kinetics of the Ni_3Sn_4 layer for liquid Sn interaction with Ni follows a power law with growth exponent n varying from 0.36 to 0.42 and the apparent activation energy for liquid-solid Ni_3Sn_4 formation was evaluated to be of about 20 kJ.mol^{-1}. The values of growth exponent n suggests that the rate controlling step of the growth process can be either the grain boundary diffusion or the liquid state diffusion through nanometric channels inside the Ni_3Sn_4 layer.

In chapter 4, formation of interconnects at 10 µm pitch was studied. In the case of fine pitch assembly, no prior reflow is recommended as it reduces the available Sn for bonding. However, the reflow behaviour was studied as it brought some interesting and useful information. It was found that the fabrication process, especially the last step, i.e. etching, interferes with the assembly process. For 10 µm pitch Cu pillars, SF_6 etching is used to remove the Ti seed layer, which altered the Sn surface and then prevented it from getting reflowed, i.e. forming a spherical shape in inert atmosphere, which is otherwise possible for pillars which are not seed etched. In order to have a spherical cap shape, flux must be used. The second interesting observation is on the lateral Cu walls, when they are covered with Sn due to its spilling. This occurred when temperature-time profile was changed and a plateau was introduced below the melting temperature of Sn-Ag alloy and no flux was used. This phenomenon gets further enhanced when flux was used. This type of bump was called as Hedgehog Bump. It is reported in the thesis that, during the plateau without flux, Sn atoms diffuse (by surface diffusion) to Cu (or Cu oxide) surface at the later walls of Cu pillar and reacts with Cu to form Cu-Sn IMCs and when the Sn-Ag alloy melts, it wets rapidly the surface of Cu pillar, partially transformed in Cu-Sn

IMCs, by non reactive wetting. However, in the presence of flux, Cu walls are deoxidized, so during plateau Sn diffuses throughout the walls of Cu pillar and completely transforms them in Cu-Sn IMCs and by the time Sn melts, it instantly wets the Cu walls (Cu-Sn IMCs) by non reactive wetting, thus enhanced spilling.

After studying reflow, some bonding processes were studied, and 2 processes were designed by changing just temperature-time profile, such a way, that in one process least IMCs are formed (i.e. Sn interconnect) and in another process the whole joint is converted into IMC joint (i.e. IMC interconnect). The formation of these interconnects was studied from the metallurgical point of view. For Sn interconnects the system configuration is Ni/Ni_3Sn_4/δ-$AuNi_2Sn_4$ / Ni_3Sn_4 / Ni and for IMC interconnects it is Ni/Ni_3Sn_4/Ni with either dissolved or nanometric precipitates of δ-$AuNi_2Sn_4$ phase inside Ni_3Sn_4 layer.

On aging these interconnects, Ni_3Sn_2 layer was observed which appeared at 200°C after 24 hrs and became continuous after 48 hrs of annealing. From then, it grew uniformly with a growth exponent n = 0.3. This layer was accompanied by nanometric voids of the same size as the size of the grains in this layer. These could be voids due to surface preparations while polishing. According to a work reported recently in the literature, the resistivity of Ni_3Sn_2 phase is 30 times higher than that of Ni_3Sn_4 phase. However, in our study, due to the resistance decrement of the different metal layers below the interconnect during annealing it was not possible to estimate the resistivity of Ni_3Sn_2 layer thus it still needs to be verified in the future.

Regarding the mechanical properties, the IMC interconnect has higher Young's modulus than Sn interconnects, thus it is more rigid and can be prone to brittleness, however, upon shear stress, it showed higher mechanical resistance than the later. In terms of electrical resistance, it is estimated theoretically that for Sn and IMC interconnects the value should be 70 mΩ and 87 mΩ respectively. However, the measured resistances were found to be much higher, between 175-275 mΩ with large variations. These high values were proven to be due to contact problems between the underlying layers because of fabrication process issues.

The evolution of electrical resistance during aging of the interconnects were then studied. On annealing these interconnects at 175°C and 200°C for 100 hrs the contact resistance dropped to their estimated value, possibly due to improvement in contact between electrical lines and interconnect. Then no resistance increase was observed until dramatic failure. The IMC interconnect was found to be much less reliable with probability of failure 8 times higher than the Sn interconnect. The major failure for Sn interconnects was because of Cu oxidation thus indicating no specific weakness of the joint (Ni/Ni_3Sn_4/δ-$AuNi_2Sn_4$/Ni_3Sn_4/Ni). Thus, from a metallurgical point of view Sn interconnect seems to be well adapted for the 10 µm pitch assembly.

The interconnects for 10 µm pitch assembly were successfully achieved using Cu/Ni/Sn-Ag micro pillars.

PERSPECTIVES

The main thermal stability issue in both Sn interconnects and IMC interconnects were found to be Cu corrosion. In our point of view, underfilling can effectively reduce or postpone these failures. Thus, the next step in for further developing interconnects at 10 µm pitch should be investigation of underfilling. The underfilling polymer will have to be carefully chosen. It must protect mechanically but also against corrosion and should have a proper viscosity for Capillary Under Filling (CUF). Ideally a pre-applied underfilling would be a good idea as in the case of 10 µm pitch the inter-distance between bumps are very small and CUF will be a challenge. However, some deep work is necessary as in this case the pre-applied underfilling will have to be thin to accommodate the small bump height and it is also well known that some fillers get easily trapped in the interconnect.

The second perspective is to test these interconnects under electric field stressing, i.e. electromigration. Cu-Sn IMCs are well investigated for the electromigration study, but Ni-Sn IMCs are not yet investigated. It will be interesting to see how Ni_3Sn_4 and/or Ni_3Sn_4/ δ-$AuNi_2Sn_4$ IMC joints behave under continuous current stress. It would be interesting to study if the δ phase have any effect on the electromigration and what would be the growth kinetics of Ni_3Sn_2 layer under these conditions. It will also help in determining the resistivity of this layer.

The third perspective is to investigate assembly involving different substrates that may be Si with sapphire with 10 µm pitch interconnects on larger format. We know that there is considerable difference in their CTEs (2.6 ppm/°C for Si and 6ppm/°C for sapphire), so how this CTE difference effects the bond and what should be the changes in the bonding conditions in order to compensate the difference.

The fourth perspective is to investigate the growth kinetics and properties of Ni_3Sn_2 layer, as it will determine the stability of Ni_3Sn_4 phase (with or without δ-$AuNi_2Sn_4$) IMC interconnect.

Appendix A

Flip chip technology other than soldering

Cu-Cu direct bonding is wafer to wafer bonding technique, where interconnects are formed with Cu to Cu. Here Cu pillars are fabricated on both sides, active device as well as interposer/carrier wafer and the bonding is done by thermo-compression. The temperature required to bond is between 400-450°C which is much higher than that during soldering. The pressure used during bonding is usually between 1-10 MPa. Here the key issue is to remove copper oxide which can be performed by doing some chemical treatment like dipping the wafers in diluted H_2SO_4. After bonding, annealing is done at temperature 400-450°C for some hours to facilitate Cu-Cu interdiffusion. An example for such bonding is shown in Figure A.1.

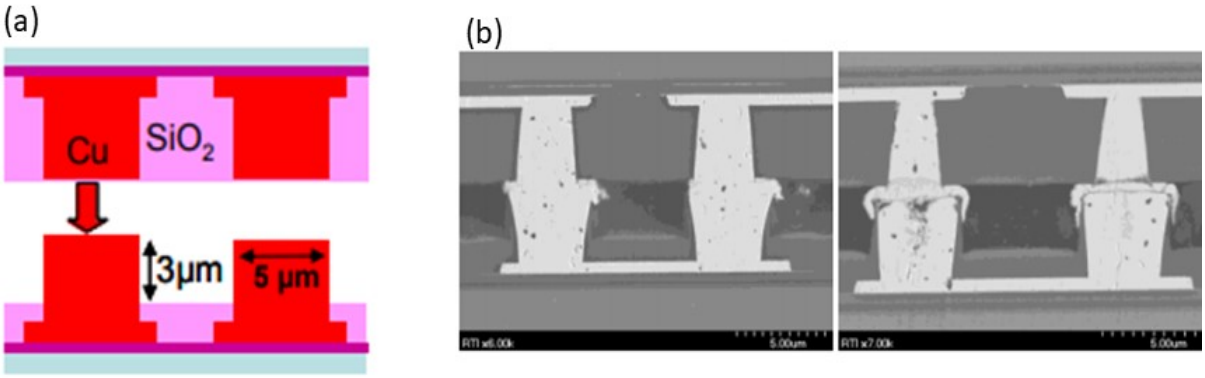


Figure A.1: Cu-Cu direct bonding (a) schematics and (b) SEM image after assembly at 10 µm pitch [172]

With this technique, the resistance per interconnect is close to that of Cu, thus really noble for applications that require low resistivity and high current densities (due to Cu high resistance towards electro-migration). The assembly pitch with this technique has reached 1 µm and can be further scaled down too, however only for CTE matched wafers [172, 173].

This type of bonding can only be used for Si wafer bonding and the yield of the wafer should be important. As this bonding technique is expensive, the cost of per package will be low only

if the yield is 100%. If not then some bad dies would be packaged and later on, during the test it will be discarded. This will increase the cost of per package. Lastly, this technique can only be used for all devices which can sustain the thermal budget of bonding process.

Cu-Cu direct bonding can also be achieved by **Surface Activation Bonding** (SAB). In theory this technique can bond any two same metals, but in practice it is used for Cu-Cu and Si-Si bonding. In this bonding technique, Ar plasma is used to treat the surface, which removes the oxide and prepare it for bonding. The bonding process can be done at room temperature but force is required (between 1-10MPa) to facilitate the diffusion between Cu/Cu and Si/Si. The assembly pitch achieved by this bonding is 7.5 µm shown in Figure A.2. Since plasma is used, a special equipment is needed to perform this bonding, which increases the cost of bonding [174–176].

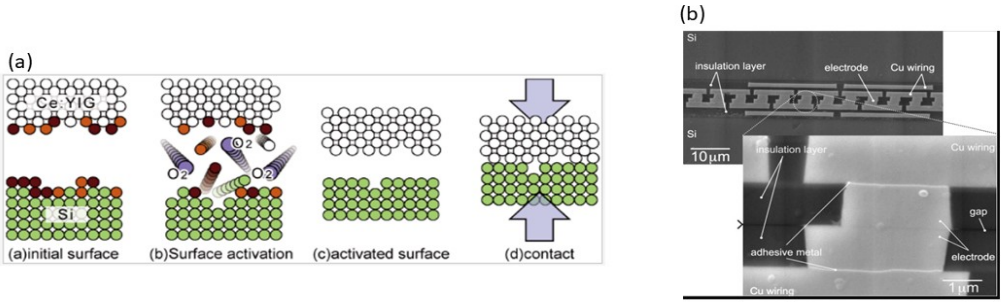


Figure A.2: Surface activation bonding (a) schematics and (b) SEM image after assembly at 7.5 µm pitch

The other flip chip technique is **Cold insertion**. It is also a room temperature bonding technique for Chip to wafer bonding. This technique does not require any flux as diffusion occurs by applying very high pressure. Here hard materials are designed in such a way that it can penetrate into softer material pads with as low force as possible. The most apt design for penetration is tubes, thus the technique is called Microtubes shown in Figure A.3. The soft material commonly used is Al-0.5Cu pad. This can achieve very fine pitch and has low/no impact of CTE mismatch and warpage like soldering, thus a noble choice for bonding between different substrates like Si on sapphire or Si on GaN [177, 178].

However, high force is needed for bonding therefore it cannot cater application which are force sensitive. The fabrication of microtubes is also bit tricky, thus expensive and the fabrication is new to industry thus not compatible with present fabrication capabilities which put additional cost.

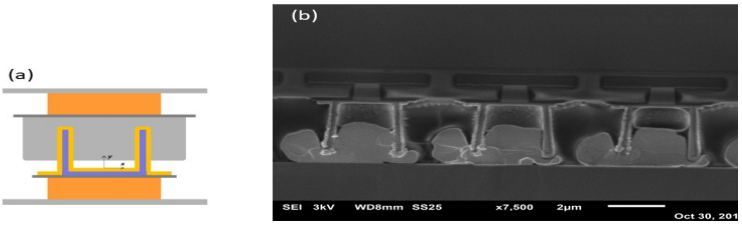


Figure A.3: Cold insertion mcirotubes (a) schematics and (b) SEM image after assembly at 10 µm pitch

Lastly, **Indium** can be used as a solder as the melting point is low, CTE mismatch during bonding would not be as complicated as Sn soldering. However the device after assembly can't be used at temperature higher than the melting point of Indium which is 156°C. Secondly indium is expensive and the deposition methods are not very well adapted in the industry. Thus only niche of the application uses indium bumps like Infrared Detectors. An example is shown in Figure A.4 [179].

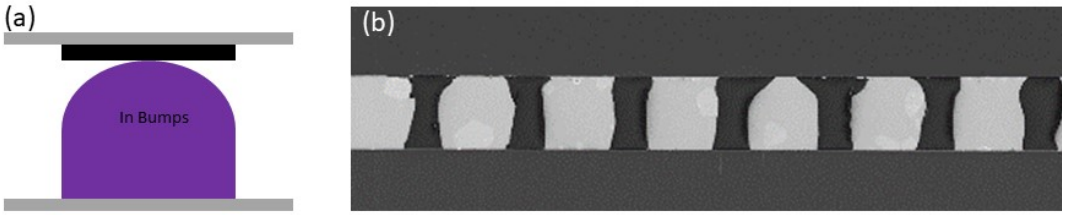


Figure A.4: Soldering with In bumps (a) schematics and (b) SEM image after assembly at 10 µm pitch

Appendix B

IMC thickness estimation

In order to evaluate the average thickness of a reaction layer SEM images of cross-section are analyzed with the help of IMAGEJ software. Using this software, the area of intermetallic (IMC) on the cross-section was measured and the mean IMC thickness is calculated by dividing the measured area of the cross-section by the corresponding length. An example is shown in Figure B.1

$$e = area/length \tag{B.1}$$

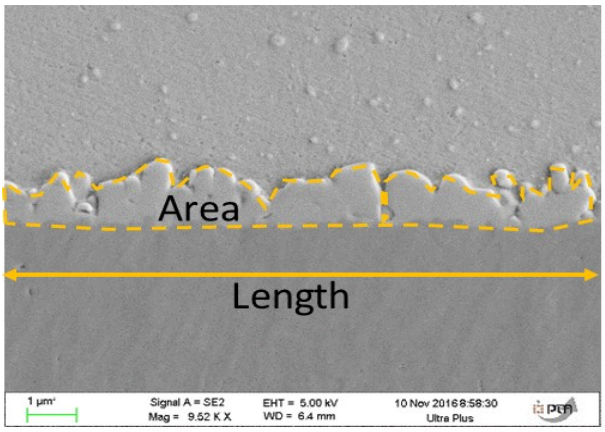


Figure B.1: Micrograph of Ni/Sn-Ag interface showing a reaction layer for which the average thickness is to be measured

Appendix C

Isothermal sections of the ternary Au-Ni-Sn system at 200°C and 300°C calculated by Thermocalc software

Figure C.1 compares the calculated isothermal section of the ternary Au-Ni-Sn system at 200 and 300°C reported by [159] and calculated by Thermocalc software.

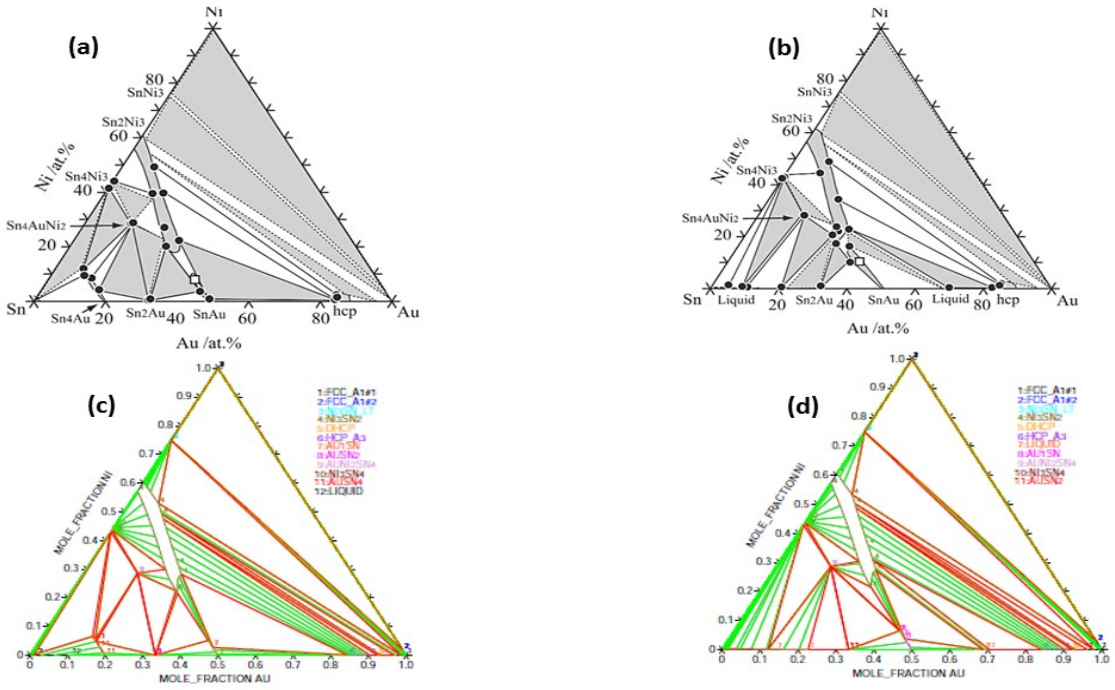


Figure C.1: Isothermal sections of the ternary Au-Ni-Sn system at (a) 200°C and (b) 300°C from Ref [159] and from Thermocalc software (c) and (d)

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