Fabrication and characterisation of photovoltaic cells based on gallium phosphide on silicon

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THÈSE

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Fabrication et caractérisation de cellules photovoltaïques à base de phosphure de gallium sur silicium

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Doctoral thesis

Fabrication and characterization of photovoltaic solar cells made of gallium phosphide on silicon

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List of Acronyms and Initialisms

Entities
ANR French National Research Agency
CEA French Alternative Energies and Atomic Energy Commission
CNRS French National Center for Scientific Research
INES French National Solar Energy Institute
ITE French Institute for Energy Transition
LITEN Innovation Laboratory for Technologies of New Energies and Nanomaterials
LTM Microelectronics Technologies Laboratory

Materials
APB AntiPhase Boundary
APD AntiPhase Domain
HHJ Hetero-homojunction, representing here GaP or a-Si:H on (n)c-Si/c-Si
ICO Indium Tin Oxide, a type of TCO
SHJ Silicon heterojunction, representing a a-Si:H/c-Si stack
TCO Transparent Conductive Oxide

Methods and techniques
AFM Atomic Force Microscopy
AFORS-HET Automat for simulation of heterostructures
DLTS Deep-Level Transient Spectroscopy
ECV Electrochemical capacity-voltage
EQE External Quantum Efficiency
IQE Internal Quantum Efficiency
MBE Molecular Beam Epitaxy
MOCVD MetalOrganic Chemical Vapour Deposition
µWPCD Microwave photoconductance decay
QSSPC Quasi steady-state photoconductance
RMS Root Mean Square
RTP Rapid Thermal Processing
SEM Scanning Electron Microscopy
SIMS Secondary Ion Mass Spectroscopy
SRH Shockley-Read-Hall
TEM Transmission Electron Microscopy

List of Abbreviations and Symbols

a-Si:H Hydrogenated amorphous silicon
c-Si Crystalline silicon
CZ Czochralski
Δ**n** Carrier injection level
η Efficiency
FZ Float Zone
GaP Gallium phosphide
HF Hydrogen Fluoride
(i) Intrisic semiconductor, undoped
IR Infrared
$\mathbf{J_{sc}}$ Short-circuit current density
(n) N-type semiconductor, doped with donors
(p) P-type semiconductor, doped with acceptors
pη Pseudo-efficiency
pp Percentage point
§ Section
$\tau_{\mathbf{b}}$ Minority carrier lifetime limited by silicon bulk recombinations
$\tau_{\mathbf{eff}}$ Effective minority carrier lifetime
$\tau_{\mathbf{s}}$ Minority carrier lifetime limited by surface recombinations, either $\tau_{\text{a-Si:H}}$ or τ_{GaP}.
UV Ultraviolet
$\mathbf{V_{oc}}$ Open-circuit voltage

Introduction

The climate change that started during the industrial revolution of the XIX century is currently inducing the most overwhelming world temperature rise since the last glaciation, 20 000 years ago. This rise in temperature is mainly due to greenhouse gases that prevent the release of heat radiated from Earth. Greenhouse gases, among them carbon dioxide, methane, and nitrous oxide, are artificially released by agriculture and by burning carbon-based fuel for powering human society for transportation, heating, and general electricity production. Thus, Earth atmosphere has not hosted such carbon dioxide level since at least 400 000 years, which has already doubled the minimum level it had reached during last glaciation [2]. This global warming that is likely to exceed 1.5℃ by the end of the XXI century [3], will induce catastrophic effects due to its fastness. Polar ice melting is rising the oceans level and will provoke waves of climate refugees. Ocean warming and acidification, extreme weather events, rain patterns change [4] will affect ecosystems, crops, and our own food supply.

Phasing out fossil fuel from the energy mix is a key element to limit climate change. Energy transition is a great opportunity to increase the contribution from low-carbon energies such as nuclear, wind, geothermal, hydroelectric, tidal, and solar power. Sun provides abundant energy, and the solar panels that convert it directly into electricity, once installed, produce no carbon emissions, are silent, and can be integrated almost anywhere: on buildings, on vehicles, as solar canopies... Its scalability enables its implementation from off-grid applications with a handful of solar panels to gigawatt-sized power plants, and makes it an important contributor to the future smart grids.

Taking advantage of the development of microelectronics, the photovoltaic energy market is led by the silicon-based technology. Silicon is a semiconductor material, which can absorb light and transfer its energy to its electrons. These free, excited electrons are early components of electric current. Photovoltaics can be defined as the craftsmanship to design solar cells, which are the base elements of solar panels that absorb light then deliver the charge carriers into electric current.

A way to leverage the cost of such devices is to increase their conversion efficiency. The most efficient silicon-based solar cells reach 21.9% for the cheaper multicrystalline silicon solar cells with TOPcon technology [5]. By using less defective and better quality silicon, monocrystalline silicon solar cells with the same technology offer 25.7% efficiency. This technology obtains better efficiencies by using thin oxide layers, named passivation layers, which greatly reduce the surface defect density of silicon. Silicon heterojunction (SHJ) solar cells, where hydrogenated

amorphous silicon layers greatly passivate the crystalline silicon, are set to reach the highest conversion efficiencies [6]. This technology has reached 25.7% efficiency and even 26.7% efficiency with interdigitated back contact (IBC-SHJ) solar cells [7].

However, some drawbacks appear when using hydrogenated amorphous silicon for heterojunction solar cells. Its optical characteristics make it absorb short-wavelength photons whose energy are lost due to its high resistivity induced by its amorphous character. A way to improve the SHJ technology is to explore other front-side materials, with better optical and electric performances to increase the conversion efficiencies.

III-V materials are compounds semiconductors from the adjacent columns of silicon in the periodic table. They have attracted great interest in the micro- and opto-electronics industry thanks to their higher, tuneable electronic and optical properties. Gallium phosphide is such material: with its higher transparency and lower resistivity, it may be grown directly on silicon to obtain higher performance hybrid SHJ solar cells [8, 9].

This thesis will summarize the theoretical and technological advancements that led to the emergence of photovoltaics and the development of GaP/Si solar cells. We will measure and analyse the performances of such devices fabricated in our facilities. By monitoring their key characteristics such as current-tension, quantum efficiency, and carrier lifetime, we will highlight process-induced limitations. These limitations will be analysed to determine their causes and origins, and we will also propose solutions to fabricate solar cells with improved efficiencies. First of all, we will go further into the physical context that allows the photovoltaic effect, introduce the state of the art of silicon photovoltaics that led to study GaP/Si solar cells, and present the outline of this thesis.

I Context and state of the art

This work, like any other science-based investigation, was not conducted *ex nihilo*. The first photoelectric device, designed by Becquerel in 1839 was electrochemical. In 1876, Adams and Day developed the first solid-state photoelectric device that generated current by light-induced crystallization of selenium. Taking advantage of the development and understanding of silicon, the first silicon solar cell was introduced in 1954 by Pearson, Fuller and Chapin. The early developments of photovoltaics were reviewed by Green in 1990 [10]. For the reader to understand what lead to the development of GaP/Si heterojunction solar cells, this chapter will start by introducing the basics of semiconductor physics that allow the inner work of silicon solar cells.

Photovoltaic solar cells are dipole generators that need to fulfil three functions: light absorption, charge separation, and charge extraction towards the electric circuit. These charge generation and separation are supported by the design of semiconductor structures. In silicon-based solar cells, these structures can either involve only crystalline silicon, namely in homojunction solar cells, or interface crystalline silicon with other materials, *i.e.* in heterojunction solar cells.

III-V materials, from the preceding and following columns of silicon's in the periodic table (see Figure I.1), were found to have semiconducting properties by Welker in 1952 and 1953 [11, 12]. They have been extensively investigated in the past decades, as their compounds generally offer better performances for optoelectronics. Their integration into thin films grown on silicon is a trending subject, to accommodate their promising characteristics and their higher deposition cost.

Within this context, the works on gallium phosphide on silicon for heterojunction solar cells will be presented and discussed. These will finally allow to outline the objectives of the study, and the plan of this dissertation.

I·A From atoms to semiconductors

Silicon is the most used semiconductor material. The characteristic properties of semiconductors come from the interaction of their constituting atoms when brought together into a crystal.

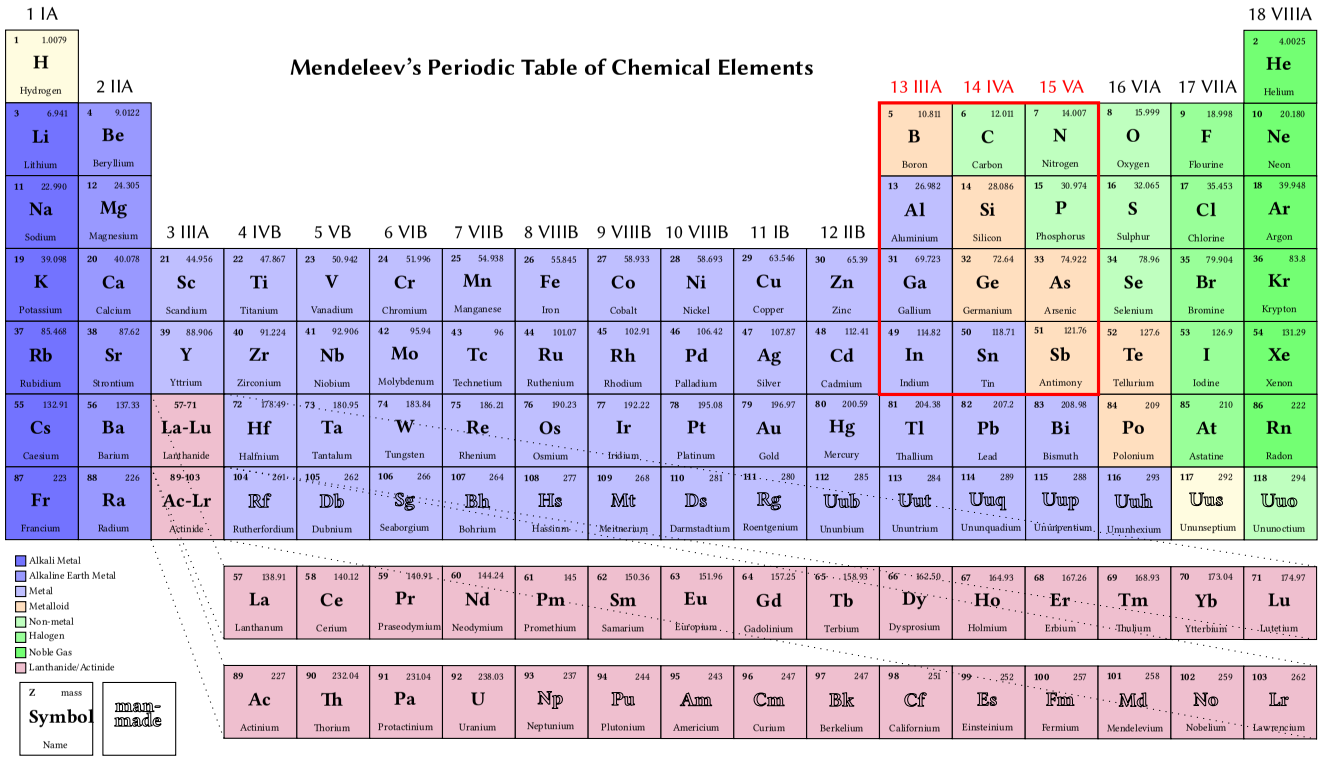

Figure I·1: Periodic table of elements, with the typically used semiconductor elements from columns III, IV, and V outlined in red. Adapted from [13]

I·A·1 Energy bands formation

Having 14 protons, isolated silicon atoms are accompanied by the same amount of electrons, which are distributed into orbitals with the following configuration: $1s^2 2s^2 2p^6 3s^2 3p^2$. The Bohr model of the silicon atom is represented in Figure I·2, with its 4 valence electrons on the latest orbitals ($n = 3$).

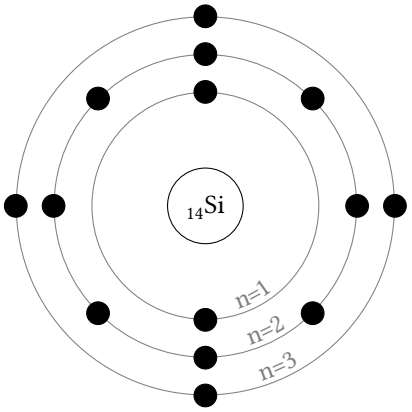

Figure I·2: Bohr's model of silicon atom.

Each of these orbitals corresponds to one discrete energy and momentum states for their electrons. However, atoms are never actually isolated: crystal formation promotes their interaction. Figure I·3 is a representation of the energy levels in silicon as a function of interatomic space.

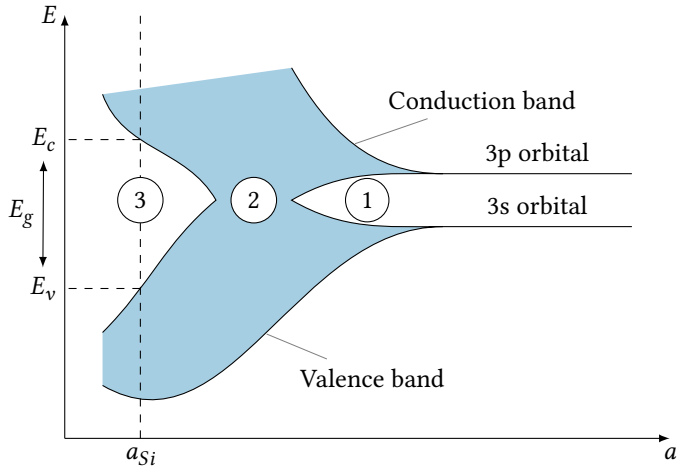

Figure I·3: Energy bands of silicon vs. lattice constant.

When atoms are brought close to each other, their valence orbitals are disrupted and start to allow an increasing number of energy levels: they become bands ①. If atoms are moved closer,

the $3s$ and $3p$ orbitals hybridize as the bands merge together ②. Finally, what actually happens in crystalline materials occurs at interatomic space. Four cases are possible, as depicted in Figure I·4:

- The hybridized $3s - -3p$ bands split into one high and one low energy bands, respectively named conduction and valence bands, (CB and VB) which are separated by a forbidden energy band gap. This is the case for silicon (③ in Figure I·3), where lattice parameter a_{Si} is 5.43 Å and bandgap E_g is 1.12 eV). If the bandgap is small, external energy excitations are enough for electrons to jump from VB up to CB: the material is semiconducting.
- However if the band gap is large and the valence band is filled, thermal energy and solar radiation are not high enough to overcome the barrier: the material is insulating.
- If band splitting does not occur, then the conduction and valence band overlap: the material is a semimetal.
- If band splitting occurs and the valence band is partially filled, charge carriers can move freely: the material is a metal.

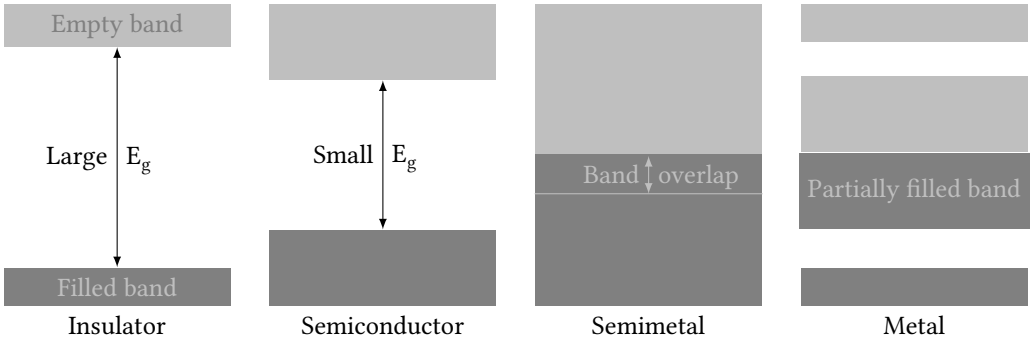

Figure I·4: Schematic of the four cases of valence and conduction band splitting.

I·A·2 Doping

At thermodynamic equilibrium and 0 K, all electrons in pure — namely intrinsic — semiconductors are in the valence band, making it insulating. At ambient temperature, even in dark, thermal energy is enough for a small amount of electrons to cross the bandgap, which allows some carrier conduction. To increase the conductivity of silicon, one can alter the density of free carriers by introducing impurities.

Such impurities are chosen from the adjacent columns of the periodic table, from column V and column III, because they respectively present one more and one less valence electron. The incorporation of these impurities, that can donate or accept electrons from their neighbouring silicon atoms, is called doping. Figure I·5 illustrates this concept.

Fermi level is result of the distribution probability of electrons. If a material were to allow a continuum of energy levels in its bandgap. The energy level at Fermi level would have 50%

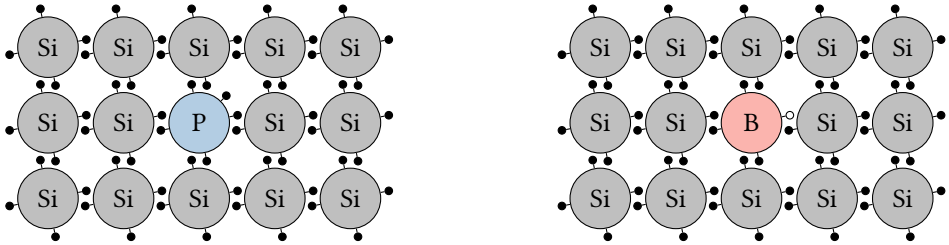

Figure I·5: Atomic lattice and valence electrons in doped silicon for:
(a) p-type silicon doped with boron and its lacking electron,
(b) n-type silicon doped with phosphorus and its additional electron.

chance to be occupied. As shown in Figure I·6, p- and n-type have similar effects on the energy bands, their carrier population and the resulting conductivity and Fermi level.

- N-type doping is performed with donor atoms, such as phosphorus, as its energy level is close to the conduction band of silicon and thermal excitation is enough for its additional electron to jump into the conduction band. Conductivity is then favoured by the additional electrons in the conduction band. As there are more electrons in the conduction band, Fermi level is risen.
- P-type doping is obtained with acceptor atoms, such as boron. Being close to the valence band, boron energy level allows its lack of electrons to be exchanged with electrons from the valence band. Being perpetually filled by neighbouring electrons, this lack of electrons moves and behaves like a quasiparticle named hole. Conductivity is then enhanced thanks to the holes in the previously filled valence band. As there are less electrons available, Fermi levels decreases closer to the valence band.

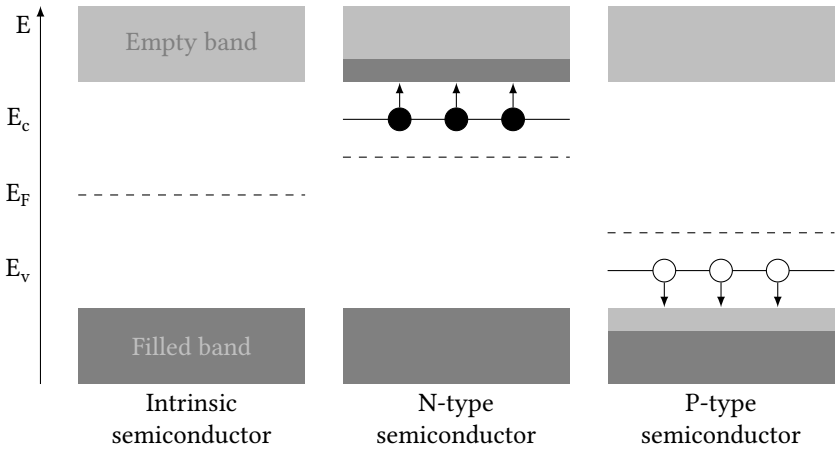

Figure I·6: Energy band filling in intrinsic, n-type and p-type semiconductor by the doping mechanism. Fermi level, represented by the dashed lines, is shifted by the doping.

I·A·3 Direct and indirect bandgaps

Bandgaps can be indirect or direct, depending on whether electrons need a change of momentum to cross the bandgap, or not. For example, silicon has an indirect bandgap, while the bandgap of indium arsenide is direct (see Figure I·7). Direct bandgap materials are useful for optoelectronics, as they can easily emit light. For indirect bandgap materials, electrons crossing the bandgap are assisted by the absorption of a photon and a phonon. Phonons are quasiparticles representing crystal vibrations, naturally occurring in crystalline materials thanks to the elasticity of the lattices and thermal excitation.

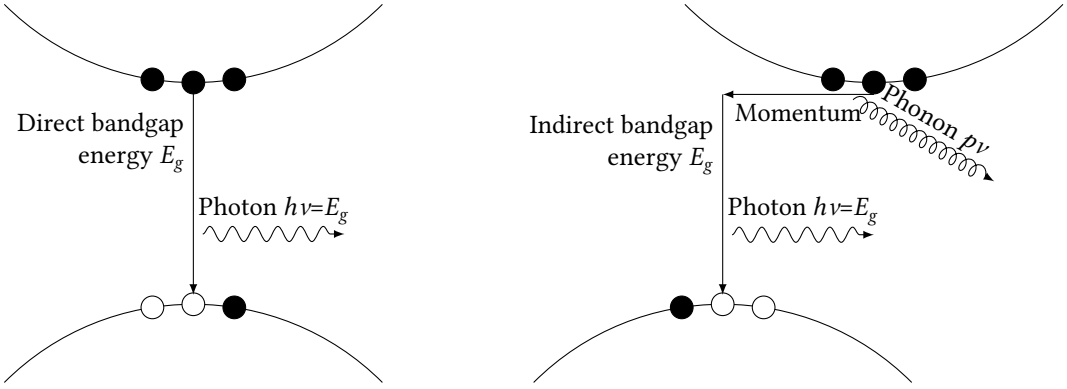

Figure I·7: Energy vs. crystal momentum diagram for direct and indirect bandgaps.

I·A·4 Light absorption and electron-hole pairs generation

Silicon bandgap is indirect and 1.12 eV at room temperature. This means that any photon whose wavelength is 1110 nm can be absorbed if silicon temperature is above 0 K — which is true for normal operating temperatures, ignoring bandgap contraction above room temperature. Higher energy photons are also absorbed, but excess energy is thermally lost (see the absorption mechanism in Figure I·8).

Considering the whole flux of light that can be absorbed by silicon, the number of excess minority carrier generated in p-type silicon, i.e. electrons, is the so-called injection level Δn. Once a photon is absorbed, the excited electron crosses the bandgap up to the conduction band, and leaves a hole in the valence band. Both are able to move freely in the crystal, forming an electron-hole pair.

I·A·4·a Recombination mechanisms in silicon

Given enough time, the electron will fall back into the hole, releasing its excess energy in form of photon or phonon. This process is called recombination.

Several recombination mechanisms are possible, represented in Figure I·8 where they are preceded by the absorption process. Such mechanisms can be intrinsic or extrinsic, if they are dependent on the properties of an ideal silicon crystal or on its alterations under external factors.

The associated lifetime expressions are considered for p-type silicon, doped with a acceptor concentration of N_A, with p_0 and n_0 the respective hole and electron concentrations at equilibrium, Δn the excess minority carriers, i.e. electrons. For p-type silicon $p_0\ N_A \gg n_0$, and the expressions are given after the subsequent simplifications.

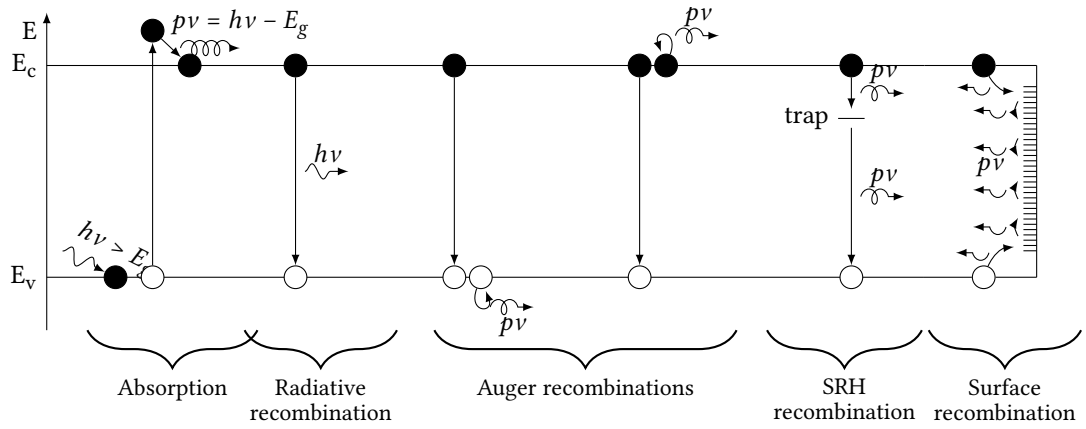

Figure I·8: Absorption and recombination mechanisms.
Energy can be exchanged by photons (hν), or phonons (pν).

Radiative recombination also called band-to-band recombination. [14] The energy of the excited electron is released by a photon. This is an intrinsic recombination mechanism, rather unlikely to happen in indirect semiconductors, as the carriers need a phonon to cross the bandgap.

$$\tau_{rad} = \frac{1}{B \cdot (N_A + \Delta n)} \text{ with } B = 1.1 \cdot 10^{-14}\ \text{cm}^3\cdot\text{s}^{-1} \tag{I·1}$$

Auger recombination [15, 16] This type of recombination is intrinsic, only due to electron-electron-hole and electron-hole-hole interaction. Interactions between electron-hole pairs are more likely to happen as their number increases: the energy released by a recombining pair is given to a neighbouring electron or hole, which is subsequently excited. It may relax by emitting a phonon as depicted here, or exit the material and be detected and analysed (Auger Electron Spectroscopy). Auger lifetime decreases as the carrier density increases, making it strongly dependent on doping and injection levels, as shown in Equation I·2. Enhanced models were developped later by Richter *et al.* [17].

$$\tau_{Auger} = \frac{1}{C_p \cdot N_A^2 + 2p_0\Delta n + \Delta n^2} \text{ with } C_p = 1 \cdot 10^{-6}\ \text{cm}^6\cdot\text{s}^{-1} \tag{I·2}$$

Shockley-Read-Hall (SRH) recombination [18, 19] This extrinsic recombination model represents trap-assisted recombinations.

$$\tau_{SRH} = \frac{\tau_{p0} \cdot (n_0 + \Delta n + n_1) + \tau_{n0} \cdot (p_0 + \Delta n + p_1)}{p_0 + \Delta n} \tag{I·3}$$

where $\tau_{n0} = (N_{trap} v_n^{th} \sigma_n)^{-1}$, is the low-injection lifetimes for electrons,
$\tau_{p0} = (N_{trap} v_p^{th} \sigma_p)^{-1}$ is the low-injection lifetimes for holes,
σ_n and σ_p are respectively the capture cross-sections for electrons and holes,
$v_n^{th} = 2.05 \cdot 10^7$ cm·s^{-1} is the thermal velocity of electrons at 300 K [10],
$v_p^{th} = 1.69 \cdot 10^7$ cm·s^{-1} is the thermal velocity of holes at 300 K [10],
N_{trap} is the trap concentration,
$n_1 = N_c \cdot \exp\left(-\frac{E_c - E_{trap}}{kT}\right)$ is the electron density at the trap level,
$p_1 = N_c \cdot \exp\left(-\frac{E_{trap} - E_v}{kT}\right)$ is the hole density at the trap level,

Their capture-cross sections are generally asymmetric, making traps more likely to capture holes or electrons first, depending on their ionization. Most effective traps have so-called deep energy levels, near the middle of the bandgap. Figure I·9 gives an overview of the plethora of energy levels associated with SRH traps that can populate and disrupt the energy bandgap of silicon.

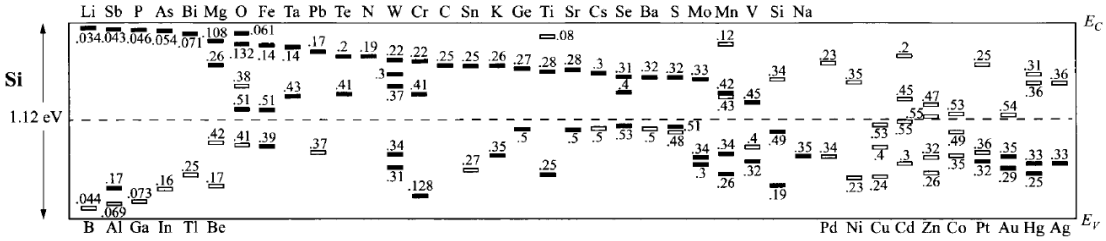

Figure I·9: Energy levels of various impurities in silicon. Solid boxes represent donor levels, hollow boxes represent acceptor levels. [20]

Doping impurities such as P, As, B, Al, Ga, or In are actually a particular case of SRH generation, where their impurity level is shallow enough to have minimal recombination effect and to release its carrier into the nearest band. The traps, defects with energy levels deeper into the bandgap that lead to SRH recombination, can originate from various causes: dangling bounds from crystalline defects, vacancies, contaminants precipitates, and substitutional, interstitial atoms. Figure I·10 represents such defects in a schematic silicon lattice.

Surface recombination Real crystals are not infinite: atomic bonds are broken at wafer surface. These dangling bonds, combined with traps brought by surface contamination, can be represented [21] with their density D_{it}, their energy levels that can cover the whole bandgap, and the surface recombination velocity S. The reduction of surface defects, by fulfilling the dangling bonds, is called passivation.

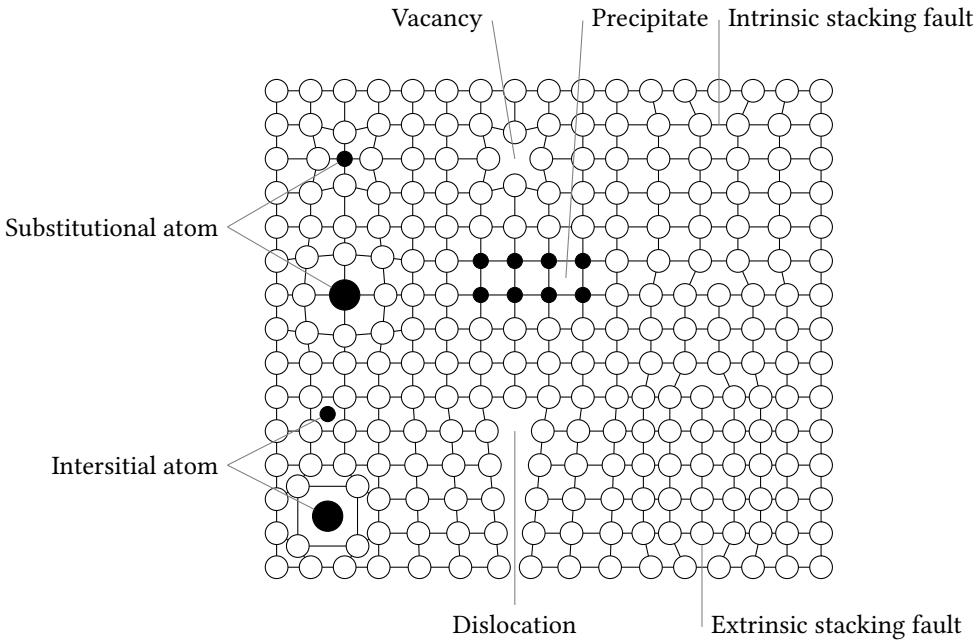

Figure I·10: Lattice schematic of silicon (white circles) bulk, with some crystalline defects and impurities (black circles).

All recombination pathways are available at the same time. From them emerges the minority carrier effective lifetime τ_{eff}, which can be separated into τ_b and τ_s, the bulk and surface contributions:

$$\begin{aligned}\frac{1}{\tau_{eff}} &= \frac{1}{\tau_b} + \frac{1}{\tau_s} \\ &= \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_s}\end{aligned} \tag{I·4}$$

τ_{eff} is obtained through lifetime measurement (see § II·B·3·c·i) and from it can derive the diffusion length L which is a key parameter to describe how far an electron, or a hole, can move inside the material before being lost by recombination. Equation I·5

$$L = \sqrt{D \times \tau_{eff}} \tag{I·5}$$

I·B From semiconductors to solar cell structures

Given its semiconducting capabilities, silicon is a material of choice to convert light energy into current. However, free roaming electron-hole pairs are only premises of current. Solar cells are dipole generators, so the pairs have to be separated: electrons need to be guided towards the negative pole and electrons towards the positive pole. To do so, one has to generate an electric

field inside the material. Using the doping of silicon, one can create a PN junction between p-type and n-type silicon, namely a homojunction. The bulk of silicon remains globally neutral, thanks to equilibrium between excess carriers between (p) and (n) c-Si.

- Electrons in the (n) c-Si diffuse into (p) c-Si where they recombine with holes, leaving positively charged donors on the (n) side.
- Holes in the (p) c-Si diffuse into (n) c-Si where they recombine with electrons, leaving negatively charged acceptors on the (p) side.

This creates a depletion zone around the junction where there is no free charge carrier at rest. The difference of polarity of the fixed ionized donors and acceptors results in a built-in voltage and the desired electric field that separates the electron-hole pairs coming from the rest of the bulk. Basic structure of a photovoltaic solar cell can now be designed, as shown in Figure I·11. The base material is silicon, into which is formed a PN junction by introducing an opposite doping layer called emitter. Back contact can be a full sheet metallic layer, while front contact must let light through. Moreover, antireflective coating (ARC) can be introduced on the front side to maximize light trapping. The performance properties of photovoltaic solar cells are described by their short circuit current density (J_{sc}), open-circuit voltage (V_{oc}), fill factor (FF) and efficiency (η) in § II·B·3·e.

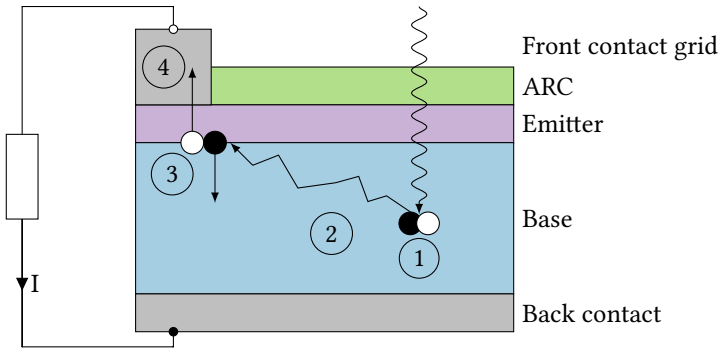

Figure I·11: Photovoltaic solar cell working principle.
① Absorption and electron-hole pair generation, ② Random diffusion in base, ③ Charge separation if emitter is reached before recombination, ④ Charge collection.

Figure I·12 represents a standard Al-BSF homojunction solar cell structure, with boron-doped p-type silicon wafer, with front side phosphorus-doped emitter. Surfaces are textured, i.e. etched with KOH to form micrometric pyramids that limit light reflection. In this case, textured surfaces are passivated with hydrogenated amorphous silicon nitride (a-SiN:H) that doubles as an ARC. Metal contacts are made of aluminium that diffuses into the substrate to form a (p+/p) back surface field (BSF) to enhance passivation.

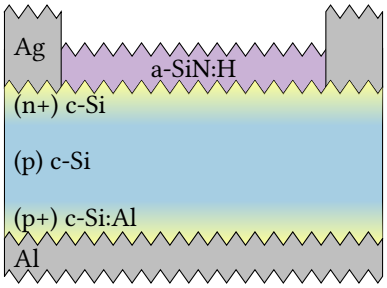

Figure I·12: Al-BSF homojunction solar cell.

Taking advantages of the better (n)c-Si substrate lifetime, several improvements are developed from the classical Al-BSF, obtaining new structures:

- Passivated Emitter Rear Totally diffused (PERT) cells, topping at 22.8% efficiency by IMEC [22], where a n-type substrate is diffused with boron and phosphorus to obtain the PN junction and BSF. Back side is only locally contacted, otherwise totally passivated.
- Passivated Emitter Rear Cells (PERC) [23], where the Al-BSF and contacting are obtained by local laser firing. This technology now achieves 23.4% efficiency with the back side is passivated with Al_2O_3 [24].
- Back contact solar cells, initially suggested for concentrator solar cells [25], minimize the shadowing of the front side to increase the performances [26]. Sunpower, with an N-type monocrystalline Interdigitated Back Contact (IBC) solar cell, achieved 25% efficiency and demonstrated > 23% in IBC modules [27].
- The best silicon homojunction solar cells reach 25.7% efficiency on 4cm², 24.5% on 100cm² with the TOPcon structure of Fraunhofer ISE [5, 28, 29]. These cells include a thin oxide layer grown before the deposition of the rear emitter. The oxide passivates the substrate, and its thinness allows carriers to tunnel through it.

Another way to obtain a PN junction is to use the bandgap alignment between two different semiconductors. In silicon heterojunction (SHJ) solar cell (Figure I·13), the heterojunction is made between hydrogenated amorphous silicon (a-Si:H) and textured crystalline silicon. a-Si:H is quite convenient for SHJ solar cells as its bandgap is higher than c-Si (1.7 vs 1.12 eV) enhances the carrier selection, and nanometre-thick layers are enough to passivate c-Si. Being amorphous, its high contact resistance is compensated with a transparent conductive oxide (TCO, namely ITO, indium tin oxide) that doubles as an ARC. Metal contacts are generally silver.

Best SHJ solar cells efficiencies are up to now at 25.7% and in the so called IBC-SHJ combining SHJ and IBC contacts reach 26.7% efficiency for 79 cm² solar cells [7]. These cells have interdigitated back contact, so they have no shadowing on their front side, and passivation is optimized with a thin (i)a-Si:H layer deposited before the doped a-Si:H.

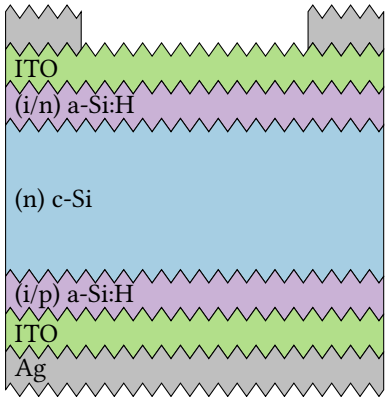

Figure I·13: Schematic representation of layer stacking in SHJ solar cell.

I·C Overcoming the limitations of silicon with III-V materials

Silicon is a ubiquitous element on Earth, and the industrialisation of its production to satisfy the needs of microelectronic devices has made it cheap. However, for both optoelectronics and photovoltaics, silicon has limitations.

For optoelectronics on one hand, its indirect bandgap forbids it to emit light so one needs to use direct bandgap semiconductors. Welker discovered the semiconducting properties of III-V compounds in 1952 [11, 12] as it was established than most of them have direct and high bandgaps. Alloying of III-V materials allows wide bandgap engineering, as depicted in Figure I·14. These bandgaps correspond to wavelengths between 300 and 4000 nm, enabling the manufacturing of light emitting diodes (LED) and lasers, used for lighting and optic fibre telecommunications.

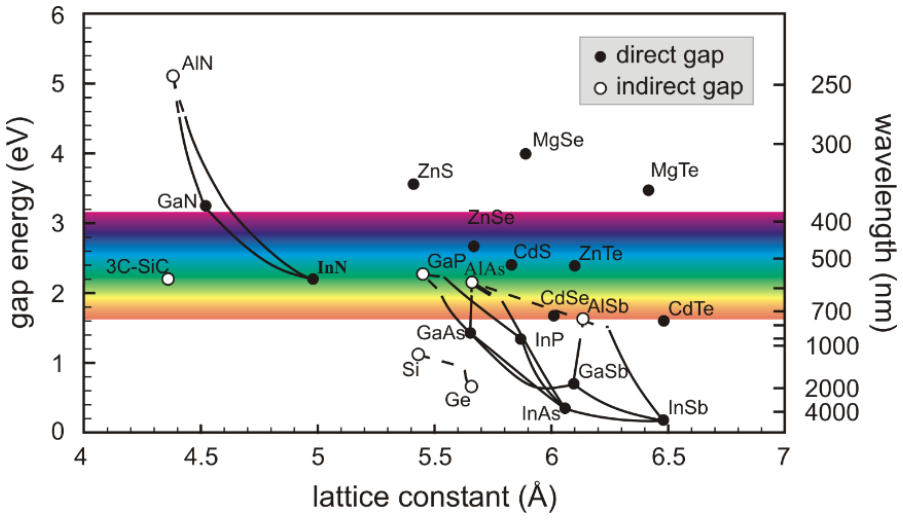

Figure I·14: Bandgap energy vs. lattice constant of IV, III-V, II-VI compounds.

On the other hand, the excess energy carried by any photon whose wavelength is shorter than 1107 nm will be lost by heat in silicon solar cells. These energy losses are a part of a broader limit, called Shockley-Queisser limit [30], that takes into account the energy loss by these spectral losses, by black body radiation of the cell, and by radiative recombination. They established the limit of single junction solar cells at 33.7% for a material with 1.37 eV bandgap, and 32% for silicon, without light concentration. This limit on silicon cells was later reduced down to 29.4% by Richter *et al.* [31] who notably included the Auger recombinations, and the effects of silicon doping and thickness into their calculations.

To overcome these limitations, one can:

- Avoid thermal relaxation of high energy photons and transparency to low energy photons.
- By bandgap engineering, one could use intermediate bands with two low energy photons: the first one brings it to the intermediate band, the second one finally excites it up to the conduction band. [32–35]
- By photon up- or down-conversion, a fluorescent screen may be able to absorb low and high energy photons and release photons at the bandgap energy of the cell.
- Use multijunction or tandem devices. By stacking several junctions monolithically, or tandems cells one on top on the other with 4 terminals, one can reach higher Shockley-Queisser limits: 42, 49, and 68% for respectively 2, 3 and theoretical unlimited junctions devices [36]. Each junction has its bandgap designed to be most efficient in its absorption band, and to be the most transparent possible for the lower junctions. These junctions are mostly obtained with III-V compounds.
- Concentrate the incoming light. By the use of glass lensing, dish reflectors, or Fresnel lenses, light can be focused between 2 and 1000 suns depending on the technology, assisted with light-tracking devices. As III-V compounds are expensive, the size of the devices is reduced but the resulting current reduction is counterbalanced by the implementation of concentration. Initially expensive due to the additional systems required the focus and track the sun, concentrator photovoltaics (CPV) costs are expected to meet the standard ones during the following decades. [37, 38]

The concentrated multijunction photovoltaics have achieved notable efficiencies, with a GaInP/GaAs//GaInAsP/GaInAs//InP tandem solar cell that achieved 46% at 508 suns [39]. Tandems with silicon bottom cells have also overtaken the symbolic Shockley-Queisser limit with Essig and al. who developed a GaInP//SHJ tandem solar cell performing 29.8% efficiency at 1 sun [39] which has plotted the path to reach 30% efficiencies while involving the heterojunction solar cells [32]. The best solar cells efficiencies, for all technologies, are regularly reviewed by Green *et al.* [40] and summarized in the NREL efficiency chart [41].

The costs of manufacturing full III-V devices are still high, but their development have shown the advantages of III-V materials: generally higher and adjustable band gap, monolithically stackable layers. The integration of III-V as thin films on silicon may be a way to improve the performances of silicon heterojunction solar cells to form so-called hybrid silicon solar cells and a fortiori tandem solar cells, while limiting the extra costs.

I·D GaP/Si heterojunctions

As previously stated, best non-concentrated single-junction silicon solar cells are obtained with heterojunction of a-Si:H on c-Si. They take advantage of the excellent passivation properties of a-Si:H, but however absorb in the UV range of the solar spectrum. This absorption is parasitic, as the defectivity of a-Si:H limits the diffusion length of carriers generated within it. In order to improve the efficiency of SHJ solar cells, one may replace the a-Si:H front emitter with new, more transparent materials.

I·D·1 Advantages of GaP over a-Si:H, and history of GaP/Si devices

A suitable III-V candidate was selected for integration on silicon and to replace hydrogenated amorphous silicon: gallium phosphide (GaP), whose properties are summarized in Table I·1. Gallium phosphide has a zinc blende structure, almost lattice-matched with silicon (0.36% relative mismatch), which enables direct planar epitaxy of GaP on c-Si [42]. Its indirect bandgap is 2.26 eV, quite higher than a-Si:H and c-Si, which makes it more transparent to short-wavelength photons [42–45], while they are absorbed and lost due to the higher resistivity of a-Si:H. Sheet resistance of GaP is hundred-fold lower than a-Si:H, but it is still high enough to require the use of ITO to ensure carrier lateral conduction up to the contacts.

Table I·1: Comparison of some characteristics at 300 K of crystalline silicon, hydrogenated amorphous silicon and gallium phosphide.[46]

Name	c-Si	a-Si:H	GaP
Structure	Diamond	Amorphous	Zinc blende
Lattice parameter [Å]	5.431	—	5.4505
Thermal expansion [K^{-1}]	$2.6 \cdot 10^{-6}$	$1 \cdot 10^{-6}$	$5.3 \cdot 10^{-6}$
Bandgap [eV]	1.12	1.6–1.9	2.26
Electron affinity [eV]	4.05	3.8	4.3
Sheet resistance [kΩ/□]	—	440	4.2

The first reporting of GaP/Si solar cells was made by Katoda and Kishi in 1980, with a 70-µm-thick (n) GaP on (p) c-Si(111) device that performed at 1.7% efficiency with a Voc of 660 mV [42]. Beck *et al.* in 1988, with 1-µm-thick GaP on (presumably) p-type silicon, reported 8.1% efficiency with direct contacting on GaP and c-Si [47]. Landis *et al.* investigated in 1990 (n) GaP grown by MOCVD as a transparent window layer as well as minority carrier mirror layer on top of c-Si that gave a Voc of 603 mV. They also reported strong absorption by GaP of short wavelengths, but good passivation of the substrate. [44]

The topic of GaP/Si solar cells was later explored by simulation by Wagner *et al.* in 2014 [48]. In this study, they replaced the front emitter of a PERC solar cell with GaP, and stated that an improvement of 49 mV and 1.1% absolute efficiency could be expected.

This work is a continuation of the thesis of T. Quinci [8], who compared with AFORS-HET (n) GaP on (p) c-Si and standard SHJ solar cells. He confirmed the Voc improvement thanks to field effect passivation, and determined notable increase of short-circuit current due to the higher transparency of GaP vs a-Si:H. Lower series resistance leads to improvement of the fill factor (FF). The overall efficiency boost thanks to GaP was determined to be 2.4 percentage points (pp). His simulation results are summarised in Table I·2:

Table I·2: Summary of simulated SHJ and GaP/Si solar cells. [8]

Heterojunction	V_{oc} [mV]	J_{sc} [mA·cm^{-2}]	FF [%]	η [%]
(n)a-Si:H/(p)c-Si	676.9	34.0	76.9	17.7
(n)GaP/(p)c-Si	723.4	35.8	77.6	20.1
Expected gain	+56	+1.8	+0.7	+2.4

The field effect passivation at GaP/Si interface, emanates from the bandgap difference between the two materials which is mainly reported onto the valence band offset. The energy barrier introduced by the GaP, higher than the one from a-Si:H, may more effectively repel the holes away from the interface and reduce interface recombination, leading to the better aforementioned minority carrier mirror, or field effect passivation. Figure I·15 is an AFORS-HET simulation (see § II·C) of the GaP/Si and a-Si:H/Si heterojunction band diagrams.

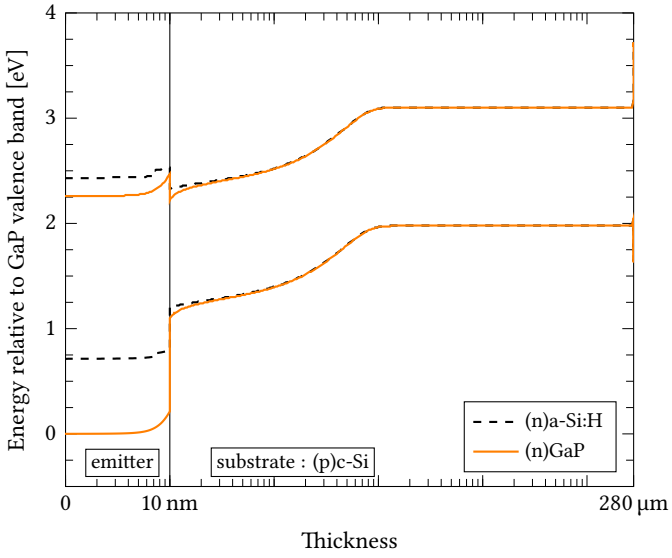

Figure I·15: Band diagrams of a-Si:H/c-Si and GaP/Si heterojunctions.

I·D·2 Challenges of epitaxy of GaP on silicon

First of all, silicon surfaces need to be specular to obtain good epitaxial layers. Indeed, rough or contaminated surfaces promotes the defects density in the materials. § II·A·2 and § II·A·7 will detail the chosen silicon substrates and their cleaning procedures. § II·A·3 will present the GaP epitaxy technique used in the frame of the work, metalorganic chemical vapour deposition (MOCVD), with trimethylgallium (TMGa) and tributylphosphine (TBP) precursors. Moreover, silicon texturation is not possible, as growth on alternating (111) planes of random density and size pyramids is not optimized.

Regardless of the grown material, typical epitaxy mishaps can still happen: vacancies, dislocations and stacking faults as evoked earlier (§ I·A·4·a), or micro-twins [49]. Micro-twins correspond to a rotation of the crystal lattice that can also affect lifetime [50]. Dislocations can occur during or after epitaxy, if the grown material as a significant lattice mismatch with the substrate. In the case of GaP on c-Si, the small lattice mismatch allows pseudomorphic growth: GaP lattice is compressed, to match the one of silicon, up to a critical thickness where relaxation by the generation of dislocation occurs. Figure I·16 illustrates such phenomenon: pseudomorphic or strained growth occurs up to relaxation (misfit epitaxy). Moreover, dislocations can occur when subjecting GaP/Si heterojunctions to temperature variations, as their different thermal expansion coefficients (see Table I·1) lead the lattice mismatch from 0.36% up to 0.48% at 600℃. This critical thickness is between 40 and 90 nm for GaP on c-Si [51, 52], so the number of dislocations due to lattice mismatch should be minimal.

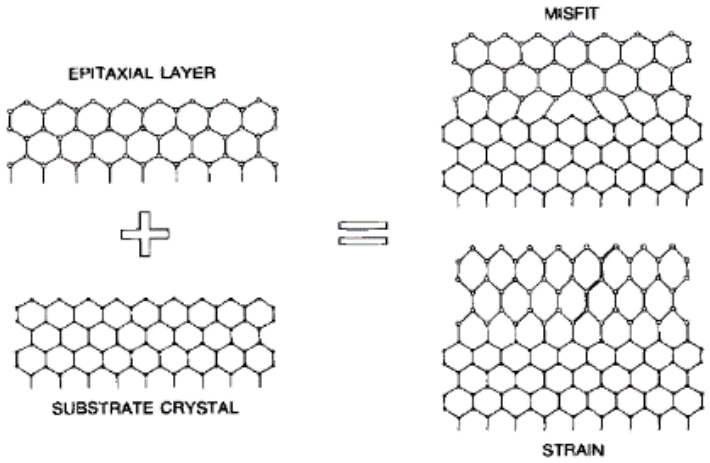

Figure I·16: Schematic representation of alternate growth modes
for two lattice mismatched, tetragonally bonded, semiconductors. [53]

The crystalline defects mentioned above can be limited regarding the growth regime. Three growth modes are possible, illustrated in Figure I·17:

(a) Standard epitaxy, with introduction of all the epitaxy precursors at the same time in the deposition chamber generally lead to 3D growth. 3D growth promotes the formation of

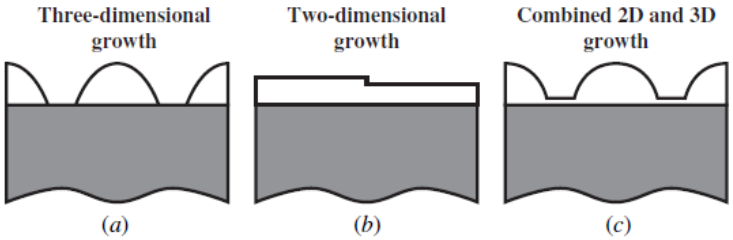

Figure I·17: Thin-film growth modes. [54]
(a) Volmer-Weber; (b) Frank-van der Merwe; (c) Stranski-Krastanov

epitaxial islands that grow independently until they coalesce and merge together. This favours multicrystalline growth, and dislocation at the former islands interfaces.

(b) 2D growth of GaP can be achieved by Atomic Layer Epitaxy [55], where the precursors are alternatively introduced in the epitaxy chamber. This allows precise control of the atoms at the interface, and of the following layers as long as monolayers are deposited. This mechanism is easier if the layer deposition is self-limiting, as for phosphorus. It is not the case for gallium, and a too long Ga ALE cycle may lead to the formation of gallium droplets that etch silicon and increases its roughness [55]. ALE cycles are although slow, as the chamber need to be free from the previous precursor before starting the next layer deposition [56].

(c) Hybrid 2D and 3D growth involves the 2D growth of a so-called nucleation layer followed by the standard 3D growth, being limited by the already deposited layers. A post-epitaxy bake is generally required to coalesce the 3D islands and obtain a homogeneous layer. This is the preferred method to obtain thick epitaxial layers [57, 58].

Even though their crystalline structure are compatible, the fact that zinc blende is populated by two different atoms, gallium and phosphorus, with different electronegativity (χ_{Ga} = 1.81 and χ_P = 2.19), leads to their bond to be polar. The diamond structure of silicon, being populated by only silicon (χ_{Si} = 1.9), displays no such polarity. The polar-on-nonpolar epitaxy problem was summarized by Kroemer in 1987 [59]. He stated that the epitaxy of III-V materials on silicon lead to problems of:

Cross-doping of epitaxial atoms into silicon, and vice versa. N-type doping of GaP is actually expected with the incorporation of silicon [60], but diffusion of gallium and phosphorus into silicon may introduce defects and compensate the doping at the interface, impeding the quality of the PN junction.

Lack of electrical neutrality at interface. In addition to Ga-P bonds, Si-P and Si-Ga bonds are nonpolar. Hence, the first monolayer deposited on silicon, made of gallium or phosphorous, will bring respectively acceptor or donor-like charge defects. Kroemer made the following calculation for Si-As bonds, which can be applied to Si-P bonds: the charge defect held per atom is $q/2$, leading to a charge density of q/a_{Si}^2 which is around $3 \cdot 10^{14}$ cm^{-2}, which may generate a field of $4 \cdot 10^9$ V·m^{-1} if left as-is. This charge is later compensated

by the rest of the material, but during epitaxy it leads to partial atomic rearrangement that may bring crystalline defects. [59]

Antiphase disorder of the epitaxial layer. Silicon substrates orientations are never perfect. Indeed, ingot sawing strictly parallel to (100) surface is difficulty, if not impossible. The slight surface orientations resulting from these miscuts lead the apparition of monoatomic steps on the surface of silicon, as depicted on Figure I·18. When depositing GaP by ALE, Ga-Ga or P-P bonds may arise at the steps.

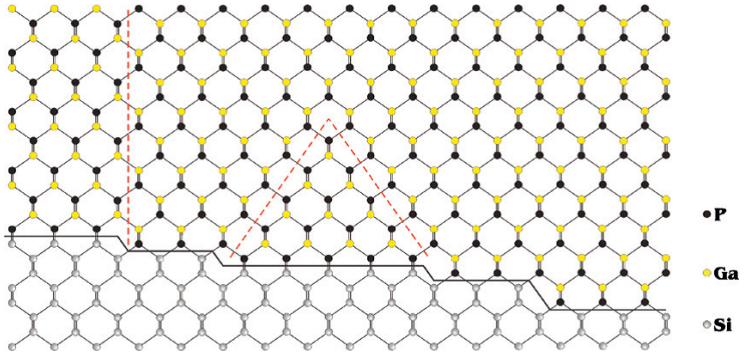

Figure I·18: Schematic lattice cross-section of GaP on Si. From the monoatomic steps on the Si surface APBs originate, which can lie on different lattice planes and eventually self-annihilate. Figure and legend from Németh *et al.* [61]

This inversion of polarity is a defect, even though it does not actually break the crystal, but rather alter its electrical neutrality that brings deep traps in the bandgap. This change of polarity is also called change of phase, and leads to the formation of antiphase domains (APD), separated by the antiphase boundaries (APB) that are materialised by the propagation of the alternative Ga-Ga and P-P across the GaP crystal, as shown in Figure I·18.

To prevent the emergence of antiphase boundaries, the reconstruction of silicon surface to make it display diatomic steps is possible [55, 62–65]. Such reconstruction can be obtained by pre-annealing of the substrate before epitaxy, at 900℃ and under pressure (with the H_2 gas carrier of the MOCVD chamber). With silicon diatomic steps, antiphase boundaries are not possible, as shown with the last atomic step on the right of Figure I·18.

Such surface reconstruction can also be favoured at lower annealing temperature with intentionally miscut substrates, such as 4°, or 6°-[011] Si (100), or even without annealing with (211) substrates. However, Grassman *et al.* established the presence of systematic dangling bonds at the (311) and (211) facets of strongly miscut substrates, as show in Figure I·19 [66]. These dangling bonds may however be passivated thanks the hydrogen carrier gas of the MOCVD. Nonetheless, silicon surface with diatomic steps can be achieved with nominal silicon.

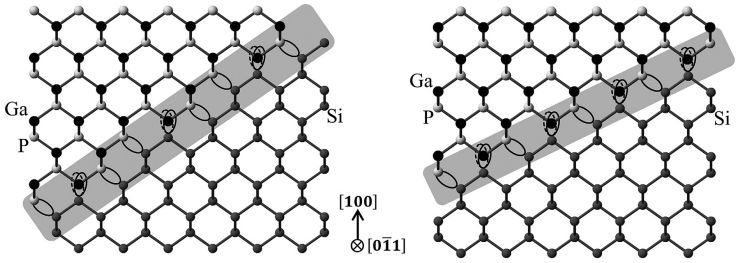

Figure I·19: Atomic structures and interfacial bonding configurations of GaP on 6°-[011] Si (100) at the (a) Si(311) and (b) Si(211) surface/interface planes. Si dangling bonds, and thus subsequent GaP/Si interfacial bonds, are indicated by the open ovals.
Figure and legend from [66]

I·E State of the art on GaP/Si solar cells

GaP has been investigated as a material for heterojunctions or as a window layer on silicon solar cells. Shahai and Milnes have simulated various heterojunction solar cells, including 5 µm- and 250 µm-thick GaP layer on silicon solar cells. They estimate the efficiency around 10%, close to the efficiency of their computed reference silicon homojunction [67]. However, the optical absorption edge in the UV range is sharper for GaP than for c-Si, which may lead to loss of photocurrent [43]. Katoda and Kishi reported the first GaP/c-Si heterojunction solar cell with an Voc of 660 mV and an efficiency of 1.7% [42]. Landis *et al.* have grown GaP by MOCVD (Molecular Organic Chemical Vapor Deposition) as a window layer on a homojunction silicon solar cell and also fabricated GaP/c-Si heterojunction solar cell results in their paper. Open-circuit voltage of 603 mV has been obtained, which is lower than in their reference homojunction silicon solar cell. They showed that GaP was significantly absorbing in the UV range of the solar spectrum [44]. Huang *et al.* have used LPE (Liquid Phase Epitaxy) to fabricate GaP/c-Si multijunctions solar cells and reported a single-junction GaP/c-Si heterojunction solar cell with a Voc of 508 mV and an efficiency of 8% [68]. Gudovskikh *et al.* have deposited GaP by MBE, resulting in Voc down to 520 mV and studied the defects brought in silicon, near the interface. Good passivation was achieved with amorphous GaP deposited by PE-ALD [69].

Recently, Feifel *et al.* [70] developed GaP/Si solar cells with 11.7% efficiency and Voc of 551 mV, and 12.4% efficiency and 561 mV with GaP as a window layer. These are so far the best results for these solar cells. They previously reported the same degradation due to MOCVD process [71–73] but were able to achieve acceptable – to them – carrier lifetime above 100 µs, while SHJ cells rather aim at 1 ms carrier lifetime. They report a lack of passivation of silicon by the GaP, which could be partially solved with the introduction of a (n+) layer on top of the silicon bulk.

As preliminary results, considering the favourable simulations of T. Quinci [42], and implementing the pre-annealing requirements for surface reconstruction silicon, Darnon *et al.* [74] fabricated GaP/Si heterojunction solar cells. The cells were made according to the process flow

in Figure II·1: 10-nm-thick (n) GaP epitaxy is performed after the wafer dry deoxidation and the surface preparation annealing, and is followed by the deposition of a standard (i/p) a-Si:H stack on the back side. Both sides are covered with ITO, front side silver grid is screen-printed and back side silver blanket is evaporated.

The solar cell performed at 8.4% efficiency with only 522 mV of open-circuit voltage despite a notable improvement of the internal quantum efficiency (IQE, cf. § II·B·3·g) of the ultraviolet photons, but a strong degradation in infrared. Table I·3 compares the performances of such cell with a SHJ reference cell, and a further analysis of such cells will be done in Chapter III.

Table I·3: Electrical performance of reference SHJ and GaP/Si solar cells. [74]

Emitter	V_{oc} [mV]	J_{sc} [mA·cm^{-2}]	FF [%]	η [%]
a-Si:H	654.7	33.2	60.6	13.2
GaP	522.1	29.0	55.8	8.4

The degradation of V_{oc} and in the infrared range of IQE was determined to take place during the surface preparation annealing in the MOCVD chamber. Such behaviour also found by Garcia-Tabarés *et al.* [75, 76] for multijunction III-V on Si solar cells that had strong carrier lifetime degradation in the silicon bulk.

I·F Objectives and outlines

This state of the art on heterojunction solar cells, III-V materials and early GaP/Si devices enables us to draw the requirements for the development of GaP/Si heterojunction solar cells by MOCVD. Such solar cells necessitate:

- High quality p-type silicon substrate, as GaP is expected to be n-type by silicon interdiffusion during epitaxy.
- Planar silicon, as epitaxy on texturized materials is expected to bring numerous defects.
- Surface preparation annealing to prevent the formation of APBs.
- Tailored standard epitaxy or ALE cycles to minimize the GaP crystalline defects.

These requirements are the canvas of this work. From them arise some questions that will be answered in the following chapters.

- What is the source and the extent of the degradation hinted by the first MOCVD GaP/Si solar cells? This question will be investigated in Chapter III.
- Can the epitaxy of gallium phosphide on silicon be optimized, *i.e.* avoid defects while preventing this degradation? Chapter IV will give some leads to do so.
- Is it possible to cure the degradation after epitaxy? It may be possible to optimize the epitaxy despite degrading the performance of the solar cell precursors, and implement additional fabrication steps to remove the causes of the degradation. Such fabrication steps will be introduced and tested in Chapter V, where solar cells with the updated process flow will be fabricated
- First of all, what are the fabrication processes, characterisation and calculation methods required to answer these questions? Chapter II will present the materials, equipment and methods required to fabricate optimal solar cells and their precursors, and analyse them.

Finally, considering the advancements and analyses performed in this work, conclusions on the development of GaP/Si solar cells will be drawn, along with potential perspectives.

II Processes and methods

Knowing materials properties, their processing, and characterization methods is paramount to obtain high efficiency solar cells and understand their performances and limitations. This chapter will firstly present the processes used to fabricate solar cells, from the initial process flow and base materials, to surface preparation, deposition techniques and post-deposition treatments. Methods to characterize the materials and solar cells will then be introduced. Finally the capabilities of AFORS-HET, solar cells simulation tool, will be described.

II·A Material processing

In this section, the initial process flow of solar cells processing will be presented, along with adequate procedures for materials selection, surface cleaning, deposition, and etching techniques. These presentations will include overviews of the physical phenomena exploited, and their limitations.

II·A·1 Overview of the process flow

Figure II·1 presents the initial fabrication process for reference SHJ and GaP/Si solar cells. Only the first steps, for front-side deposition, actually differ. Indeed, while (i) and (n) a-Si:H layers are deposited by PECVD (cf. § II·A·4) after wet deoxidation (cf. § II·A·7·b·ii) of SHJ precursors, wafers for GaP/Si solar cells are deoxidized and processed in the MOCVD cluster presented in § II·A·3. Subsequent steps consists of (i) and (p) a-Si:H back-side deposition, ITO deposition (by PVD, cf. § II·A·5), front silver grid screen-printing (cf. § II·A·6·a) and finally back silver blanket deposition (by evaporation, cf. § II·A·6·b)).

II·A·2 Crystalline silicon substrates

Two types of double side polished (DSP) monocrystalline silicon substrates were used: semiconductor grade, and solar grade wafers, whose characteristics are listed in Table II·1. Taking advantage of their smaller thickness and size, high quality FZ wafers are used for solar cells fabrication. CZ wafers, whose handling can be automated within the MOCVD cluster (see next section), are mainly used for study and development of the epitaxy steps. They are also available with different intentional miscut orientations to study the impact of surface reconstruction.

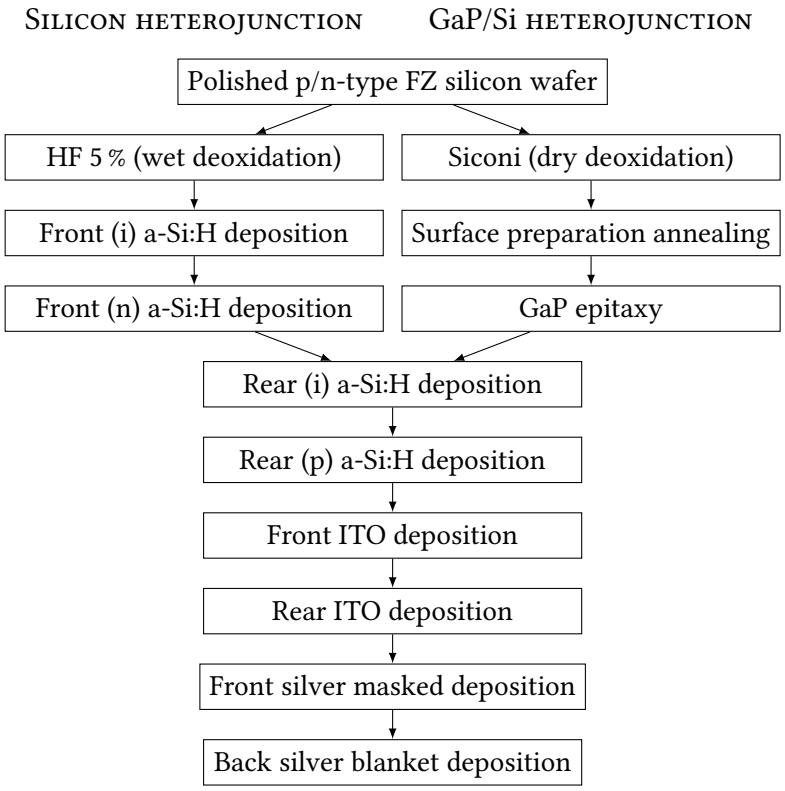

Figure II·1: Comparative diagram of process flows of reference and GaP heterojunction solar cells.

Table II·1: Summary of the wafers available for this study.

Wafer	CZ	FZ
Casting	Czochralski	Float zone
Grade	Electronic	Solar
Carrier lifetime at 1 sun	> 3000 µs	> 1000 µs
Diameter	300 mm	100 mm
Thickness	780 µm	280 µm
Doping type	P	P/N
Resistivity	15 Ω·cm	3 Ω·cm
Dopant concentration	$[B]=9 \cdot 10^{14}$ cm^{-3}	$[B]=4.7 \cdot 10^{15}$ cm^{-3}
		$[P]=1.6 \cdot 10^{15}$ cm^{-3}
Surface	DSP	DSP
Orientation	(100)	(100)
	+0.18°[110]	
	+4°[110]	

II·A·3 Metalorganic chemical vapour epitaxy of gallium phosphide: MOCVD

Metalorganic chemical vapour epitaxy involves the pyrolysis of metalorganic compounds on the heated substrate surface. The organic residuals (methane generally) are carried away by the vector gas, while the interest atoms are adsorbed, chemically bonded, to the substrate. The optimal pyrolysis-desorption-adsorption of the precursors and their residuals is obtained by tuning the temperature and pressure of the chamber. Precursor introduction can simultaneous for classic, or regular, epitaxy. Precursors can also be introduced one after the other (after adequately pumping out the previous one) to perform self-limiting monolayer deposition, also known as atomic layer epitaxy (ALE). Regular epitaxy can achieve deposition rates up to a few microns per hour, which is why MOCVD is prospected for the fabrication of multijunction solar cells.

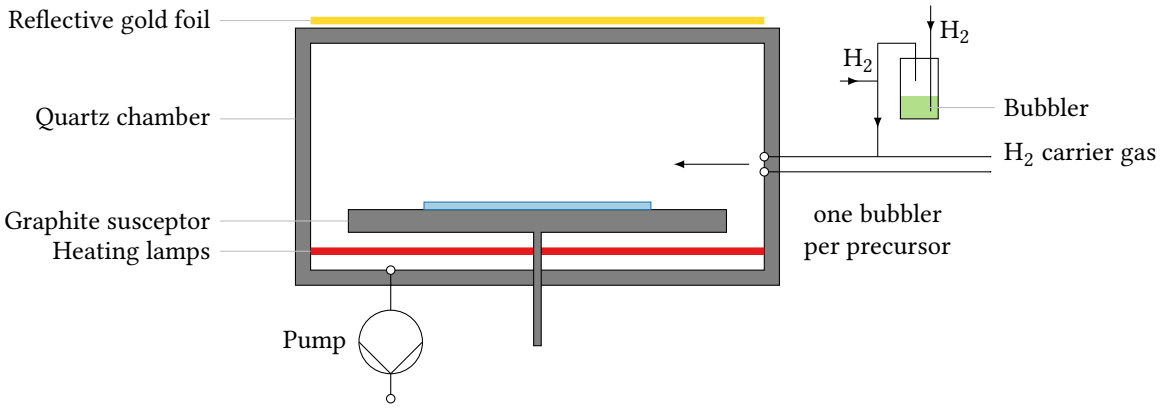

Figure II·2: Schematic of the MOCVD chamber

As schematically portrayed in Figure II·2, the deposition chamber in the MOCVD cluster (by Applied Materials, also equipped with a Siconi chamber for preliminary deoxidation, see § II·A·7·b·i) can heat the wafer from 350 to 950℃. Homogeneous temperature is ensured thanks to an array of six heating lamp rings and the graphite susceptor onto which is laid the wafer. Precursors are diluted in hydrogen, which is also the vector gas, and are laterally injected in the deposition chamber at pressures from 5 to 750 Torr. GaP precursors are TBP and TMGa (Figure II·3), while the chamber can also use other precursors to finally deposit all the following atoms: Ga, As, In, Zn, Se, Al, Sb, P, B, Si.

II·A·4 Plasma-enhanced chemical vapour deposition of hydrogenated amorphous silicon

Plasma-enhanced chemical vapour deposition (PECVD) is a thin-film deposition technique. It involves decomposition and ionization of precursor gases in the plasma, were they become highly reactive. The radicals reaction with silicon ensure their chemical bonding, rather than mere physical deposition, and is a key contribution to the passivation power of a-Si:H.

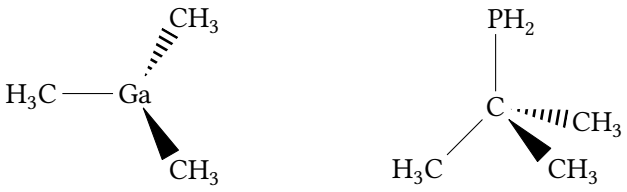

Figure II·3: Cram representation of the metalorganic precursors used for GaP epitaxy, (left) TMGa, trimethylgallium and (right) TBP, tertiarybutylphosphine.

A PECVD chamber is a vacuum enclosure, into which are introduced the samples to be processed, the precursor gases, along with a vector gas (generally H_2) through a showerhead. The sample holder acts as low electrode while the showerhead acts as top electrode, which are connected to a radio frequency generator to induce the plasma. Samples are put on a tray, which is then loaded into the cluster through an airlock chamber that preheats at 230℃ after pumping. Deposition chambers temperature is maintained at 220℃, idle pressure is 1.5 Torr. A schematic representation of a PECVD chamber is presented in Figure II·4. In this work two PECVD chambers, part of a PECVD-PVD cluster, were used for:

1. Boron-doped (p) a-Si:H deposition (with SiH4, B2H6, H2 source gas)
2. (i) a-Si:H, phosphorus-doped (n) a-Si:H, SiN and SiOx deposition (with SiH_4, PH_3, NH_3, O_2, H_2 source gas)

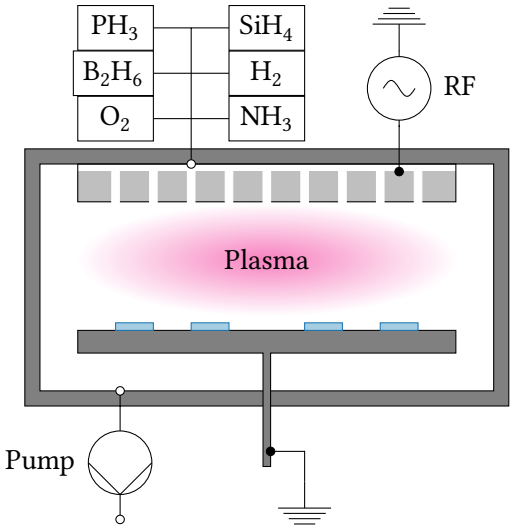

Figure II·4: Schematic of a PECVD chamber used in this thesis.

II·A·5 Physical vapour deposition of Transparent Conductive Oxide (TCO)

The deposition cluster evoked in the previous section is also equipped with a PVD chamber for ITO deposition. ITO is sputtered from a magnetron target. Magnetron generators consist in an electron flow between an anode and a cathode, deviated by electromagnetic fields towards the target. The fields are designed to drastically increase the density of electrons close to the target, so that they ionize the pulverisation gas (argon) and generate a localised plasma on the target.

The pulverisation cone does not cover the whole chamber. As the sample tray slides across the chamber under the target, its speed enables control of the deposition rate. ITO layers are generally between 70 and 100 nm. Pulverisation rate can be controlled with the density of this plasma. Structural, optical and electrical properties of ITO can be tuned varying mainly the temperature, O2 content, power and pressure while limiting carrier lifetime degradation in silicon from plasma radiation.

II·A·6 Metallization

Charge carriers are extracted and brought to the circuit through metal contacts. During this work, metal contacts were deposited by screen printing or evaporation. The 5×5 cm metal grid deposited on the front side is made of an array of 25 thin parallel strips, the fingers, crossed by a larger main line for contacting, the bus bar. See Figure III·2 for a picture of the front grid, whose dimensions are listed in Table II·3. The typical characteristics obtained for such silver are resumed in the following table.

Table II·2: Characteristics of deposited silver in this study.

Technique	Thickness	$R_{\square}$ [Ω/□]	ρ [Ω.cm]
Screen printing	> 10 µm	—	0.1 – 3
Evaporation	400 ± 30 nm	$(6 \pm 1) \cdot 10^{-2}$	$(2.4 \pm 0.5) \cdot 10^{-6}$

Table II·3: Dimensions of the front contact grid.

Dimensions	Fingers [mm]	Busbar [mm]
Pitch	2.1	—
Width	0.3 – 0.5	1.4 – 1.6
Length	50	50

II·A·6·a Front side: Screen printing

Metal deposition can be achieved with metallic inks made of metal powder diluted in solvent paste. The paste is then sift by a scraper through a screen holding the grid pattern to be printed. The screen canvas is made of wires, more or less loosely woven together to respectively block or allow the paste passing. After deposition of the pattern, annealing (200℃) is required to evaporate the solvent. A schematic of the screen printing process is depicted in Figure II.X. The screen printing system used is a Baccini B2 from Applied Materials.

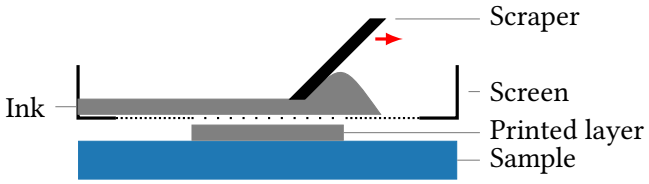

Figure II·5: Schematic of the screen printing process.

II·A·6·b Back side: Electron beam evaporation

Metal deposition can also be achieved by evaporation of ingots, heated by electron beam in a vacuum enclosure. Metal selection is achieved with an apertured carousel enclosing the crucibles. The electron beam focusing point moves under the influence of electromagnets to homogenise the energy input that liquefies the ingot, which then evaporates. Evaporation rate is monitored by a quartz whose resonance frequency is altered when material is deposited onto it. The e-beam power is then controlled through a PID circuit. The samples, held by a carousel, are thus exposed to the evaporation cone. A schematic of the evaporation apparatus, a Univex 450 B from Oerlikon, is displayed in Figure II·6. Idle vacuum is at least $5 \cdot 10^{-6}$ bar while the samples carousel typically rotates at 10 rpm. A dozen nanometre to several hundred nanometres of silver can be deposited at one time with such apparatus, 400 nm being the chosen thickness for this study.

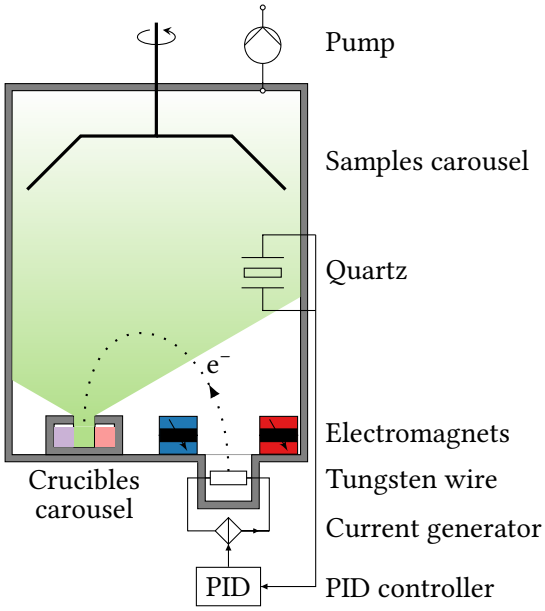

Figure II·6: Schematic of the evaporation chamber used in this study.

II·A·7 Wafer surface preparation and cleaning

Being stored in vacuum-packed, or not, plastic containers, wafers are exposed to organic contamination. Moreover, air oxidation and some pre-epitaxy treatments may lead to deposition of unwanted elements on the wafer surfaces. Thus, above all else, wafers require cleaning as surfaces need to be pristine for optimal epitaxy and passivation.

II·A·7·a RCA-HF-O3 clean for storage

As-received FZ wafers need to be cleaned to remove any organic or residual metallic contaminants. Kern developed the RCA clean [77, 78], consisting in simple wet treatments to remove them:

1. SC-1: organic and particle clean $NH_4OH + H_2O_2 + H_2O$
2. SC-2: ionic, metallic clean $HCl + H_2O_2 + H_2O$

INES extended the well-known RCA clean by adding a deoxidation step (see next section), followed by a re-oxidation step:

3. Hydrogen fluoride deoxidation HF
4. Ozone reoxidation O_3

This allows extended storage in plastic containers in clean room, as any external contamination will build up on the silicon oxide layer, subsequently removed by the HF dip necessary to start any study.

II·A·7·b Deoxidation

Even though thin silicon oxide layers can be used for passivation, oxygen is incompatible with a-Si:H deposition as it brings defects, and potential barriers. It is also incompatible with MOCVD processes as the processing temperatures may lead to its diffusion into the silicon bulk. Deoxidation is thus required before any deposition step.

II·A·7·b·i Siconi™ etch before MOCVD

In the MOCVD cluster, deoxidation is performed in a dedicated Siconi™ chamber [79]. This dry process involves H_2, NF_3 and NH_3 remote plasma that etches silicon oxide away, preserving unoxidized silicon. Samples can be transferred in vacuum without reoxidation, to the deposition chamber.

II·A·7·b·ii HF deoxidation before PECVD

To eliminate native or ozone-grown silicon oxide before a-Si:H deposition, a 30-second-long HF dip is performed, so called "HF-Last". The simplified etching reaction is:

$$SiO_{2(s)} + 6HF_{(aq)} \longrightarrow 2H^+ + SiF_{6\ (aq)}^{2-} + 2H_2O_{(aq)}$$

The HF-Last bath is composed of 5% HF and 1% HCl. While etching thicker oxide layers (SiO_x, or phosphosilicate glass, see Chapter V), 10% HF and 1%HCl mixture was used. HCl is used to increase the pH of the solution, preventing dissociation of HF and enhances the reproducibly of the etching [80]. After the HF bath, samples are dried with a nitrogen spray gun. After this procedure, samples are exposed to the air of the clean room, so they have to be transferred to the PECVD chamber as soon as possible.

II·A·7·c Material etching procedures

Some experiments require selective etching to remove some – or all, deposited layers. Meanwhile some treatments may, as a side effect, trigger unwanted etching. Here is investigated the GaP loss upon HF etching, its removal with *aqua regia*, and silicon etching.

II·A·7·c·i GaP etching with HF

Figure II·7 plots GaP thickness decreasing during HF 5% + HCl 1% etch, measured by ellipsometry (cf. § II·B·1·a). Initial thickness was 9 nm and, after 1 nm oxide removal, GaP was slowly etched at a rate of 9.4 Å per hour. Uncertainties given by the fitting model are significant, but initial and 30s-etch thicknesses were checked and confirmed via SEM (cf. § II·B·1·c·i). As the etching rate was quite slow, HF cannot be used for pratical GaP etching.

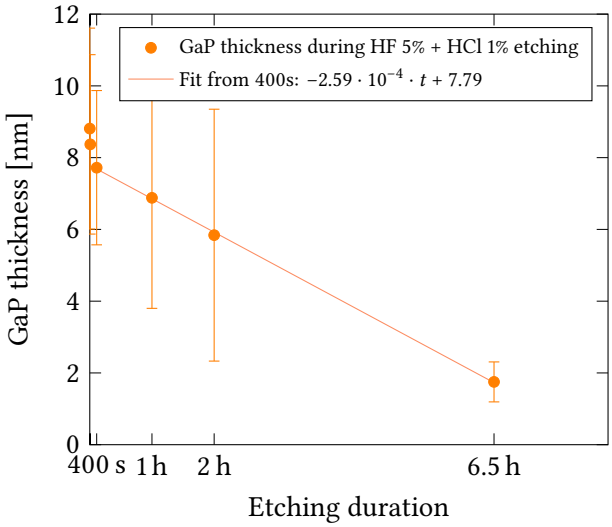

Figure II·7: GaP thickness during HF etching and linear fit after oxide removal.

II·A·7·c·ii Removing GaP and metals : Aqua regia etching

GaP, ITO and metals have *aqua regia* as common etching agent, with selectivity on c-Si and a-Si:H. *Aqua regia* is a mixture of hydrochloric acid and nitric acid:

$$HCl_{(aq)} + HNO_{3(aq)}$$

The mixture is used for ten minutes, with non-optimized 1:1 volume ratio of 49% HCl and 70% HNO_3 (3 molar parts HCl for one part HNO_3 are generally required). Samples are then rinsed, and RCA-HF-O_3 clean is performed for later processing.

II·A·7·c·iii Silicon etching with KOH

Potassium hydroxide (KOH) is generally used for texturing of silicon in low concentration etching baths (2%). Here KOH is used at more potent concentration and temperature, 20% and 80℃, to prevent pyramid formation and increase etching speed up to several micrometres per minute.

After etching, samples are rinsed, and RCA-HF-O_3 clean is performed for later processing. Surface state after etching c-Si, and especially a-Si:H on c-Si, is not suitable for epitaxy.

II·B Characterization techniques

Determining the morphology and the electric properties of the deposited materials is an important part to check the success of fabrication step and correlate the final performances of the solar cells with the characteristics of their precursors. To do so, several dedicated tools were used to observe, probe, and measure the properties and the composition of the materials.

II·B·1 Materials morphology

II·B·1·a Layer thickness: Ellipsometry

Ellipsometry is a measurement technique that measures the complex reflectance ratio $\tilde{\rho}$ by analysing the change of amplitude Ψ and phase Δ of linearly polarised light after reflection on a stack of layers. These changes depend on the wavelength λ of the photons of the incoming beam, the refractive index n and extinction coefficient k of the layer. Thicknesses are also involved, as the probe beam undergoes multiple reflections in the materials and is subject to Fresnel coefficients and Snell-Descartes' law.

The measurement of Ψ and Δ is performed by a Jobin Yvon ellipsometer, whose working principle is described in Figure II·8. White light is generated with a lamp, filtered through a monochromator and a polarizer to make it coherent. This reference beam is then sent towards the sample where it is reflected, and finally analysed with a detector. Polarization is measured thanks to a motorised polarizer (called analyser) placed between the sample and the detector. Specifically, the components parallel and perpendicular to the plane of incidence are measured and normalized to the reference beam, respectively r_p and r_s.

$$\tilde{\rho} = \frac{r_p}{r_s} = \frac{E' - p/E - p}{E'_s/E_s} = \tan(\Psi)e^{i\Delta} \tag{II·1}$$

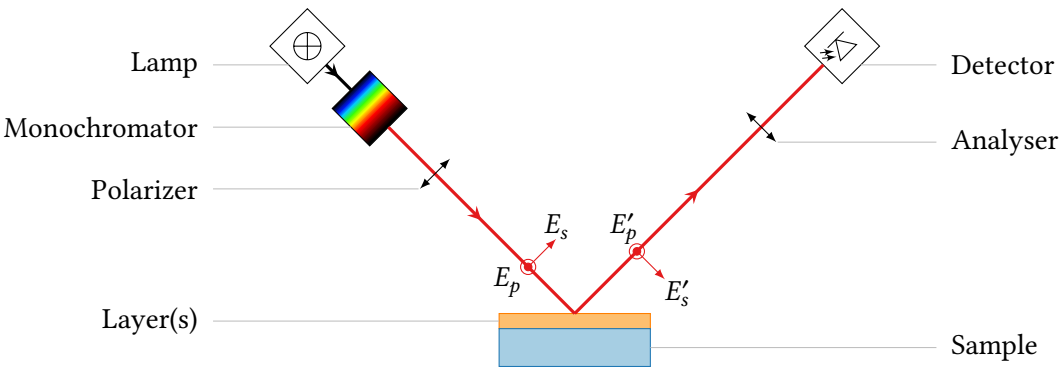

Figure II·8: Working schematic of an ellipsometer.

Measured and calculated data are then compared to the mathematical model of the materials, to determine their thickness and optical constants of a-Si:H and GaP layers, through a fitting procedure. Thickness is determined from the phase change Δ, as constructive or destructive interferences can be easily detected. Optical constants of GaP and a-Si:H layers are determined with the Tauc-Lorentz oscillator model [81–83], using the Bruggerman's effective medium approximation and the pseudo-dielectric function calculated from $\tilde{\rho}$ [84, 85].

II·B·1·b Surface roughness: Atomic Force Microscopy (AFM)

Surface topography is an important aspect to characterize the morphology and roughness of deposited layers, or the growth mode of epitaxied materials. Probing the surface is possible thanks to the interaction forces between atoms. Atomic Force Microscopy involves the measurement of such forces by approaching a nanometre-sized tip and measuring the flexion of the lever that holds it. The flexion is measured by the observing the deviation of a laser beam that is reflected onto the lever, and captured on a photodiode array. Figure II·9 describes this technique.

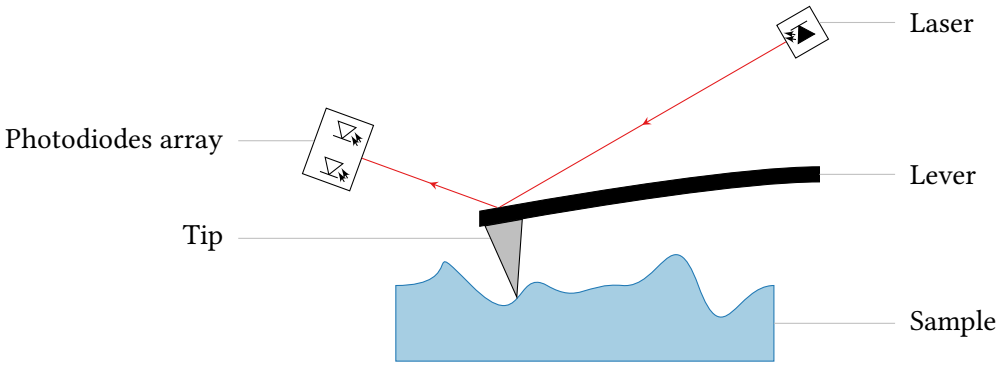

Figure II·9: Working schematic of an atomic force microscope.

Several measurement modes are possible. Contact mode is the most basic one, where the tip is approached onto the surface until it is repelled by the sample. The mode used in this study is tapping mode, where the lever oscillates near its resonance frequency. This mode minimizes the forces applied to the surface, whose topography is then deduced from the variation of the oscillation amplitude across the sample. The Bruker's FastScan AFM used in this study allows for mapping of micrometric areas, with 100 pm height resolution.

II·B·1·c Layer thickness, crystalline defects: Electron Microscopy

Optical observation of nanometre-sized, or smaller, objects is not possible, as microscope resolution r is limited by the wavelength of the light illuminating the sample: $r = 0.61\lambda/NA$ For

example, considering a microscope with a numerical aperture NA of 0.95, green light (550 nm, 2.25 eV) is not able to discriminate two points closer than 350 nm. However, electrons have smaller wavelengths for the same energy (818 pm accelerated at 2.25V) that allows resolution down to 525 pm. Electrons can be accelerated at much higher energies, 200 kV for example, but resolution also depends on the geometry of the apparatus and its aberrations. Electron microscopy consists in the detection and analysis of the reemitted or transmitted electrons, or the emitted X-rays following their interactions with the electrons of the materials. Electron microscopy, unlike optical microscopy, has to be performed in vacuum to avoid electron interaction with the air.

II·B·1·c·i Scanning Electron Microscopy (SEM)

The SEM apparatus used is a JEOL JSM-2000 which enables observation of the surface of samples down to 200 pm resolution. A focused electron beam scans the surface, and interacts with atoms that make it up: secondary electrons can be emitted, incoming electrons can be backscattered, and relaxing excited electrons can emit X-rays. SEM uses secondary electrons that are detected on a scintillator-CCD array to render an image of the surface, while X-rays can be analysed to determine its composition. SEM was used in cross-section to determine the thicknesses of the deposited layers, and observe some of the bigger defects (dislocations, roughness, etc.). It was however difficult to obtain clear images of the thinner GaP layers.

II·B·1·c·ii Transmission Electron Microscopy (TEM)

TEM can be used to increase the resolution and observe the thinner GaP layers, crystalline defects such as dislocations and grains. To observe transmitted electrons through the materials, the samples have to be thinned below 100 nm. The transmitted beam is then projected onto a scintillator-CCD array, and enables imaging resolution down to 50 pm. Materials and their atoms affect the transmitted electrons by diffraction or phase, which results in change of contrast on the projected image. A variation of this technique, STEM, combines TEM with scanning of the samples, which enables Z-contrast to discriminate atoms per their atomic number.

II·B·2 Materials composition

II·B·2·a Chemical composition and bonds: X-ray photoelectron spectrometry

X-rays can be used to stimulate atomic electrons at, and near, the sample surface. The photoemitted electrons have characteristic energies linked to the electronic state of the atoms. X-ray photoelectron spectrometry (XPS) analyses such energies to determine the chemical composition of the sample, and the nature of the atomic bonds. Knowledge of the binding energies is required, as any electron emitted by the sample can be detected. The obtained spectra are

given by signal intensity vs bond energy, and a relative composition of the elements making up the material can be deduced from them.

The X-ray probe stimulates atoms down to a dozen nanometre in the sample, but angle-resolved XPS (AR XPS) enables some depth profiling. Indeed, electrons have a fixed mean free path depending on the sample material: electrons generated deeply are less likely to come out of the surface if they have a non-normal angle. In this way, electrons detected at grazing angle are more likely to come from close to the surface.

The XPS system used is a parallel Angle-Resolved XPS (pARXPS), part of the IMPACT platform of LTM lab, that enables simultaneous acquisition of XPS spectra at various angles. It is equipped with a port that allows the transfer of samples kept in vacuum right after deposition of the layers to characterise.

II·B·2·b Active dopant concentration: Electrochemical capacity-voltage (ECV)

Electrochemical capacity-voltage (ECV) is a profiling method for electrically active dopants and traps. It has been used to check the doping profile obtained after phosphorus diffusions into silicon substrates. ECV does not dissociate donor and acceptor atoms, and gives an effective N_A or N_D, regardless of the doping species. Schottky contact is formed between an electrolyte (ammoniumbifluoride, NH_4F + HF) and the semiconductor sample. Then the following measurement steps are performed:

1. Varying the voltage, a depletion zone is formed in the semiconductor, leaving only the fixed dopants;
2. Capacitance is measured, which is function of the doping concentration;
3. Etching is activated by generating holes (forward bias is applied on p-type semiconductors, whereas n-type semiconductors are illuminated and applied reverse bias).

Steps can be repeated as long as wanted, provided that the electrolyte is renewed. Then, knowing the etching speed and duration, the etching depth can be estimated. Profilometry is required to precisely calibrate the depth profile. Inaccuracies may be brought by bubbles in the electrolyte, leading to etching variation and surface area errors. WEP's CV21 ECV system is used in this work.

II·B·2·c Chemical composition: Secondary Ion Mass Spectroscopy: SIMS

Secondary Ion Mass Spectroscopy (SIMS) is an atomic detection method based on the detection of sputtered ions from the sample. Abrasion can be performed by a primary ion beam of oxygen or caesium, selected depending on the charge of secondary ions to be detected: oxygen beam generates more cations, while caesium favours anions. With such ion beams, abrasion raster is in the order of 100 µm. Secondary ions are filtered with a mass selector and finally absorbed in a Faraday cup, were the resulting current is measured. Figure II·10 represents a working schematic of SIMS.

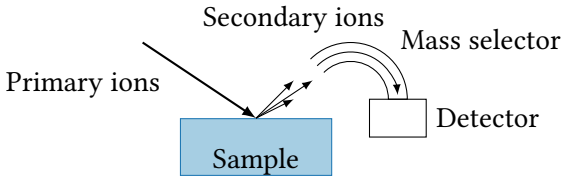

Figure II·10: Working principle of a SIMS apparatus.

Abrasion beams can be supplemented with a bismuth analysis beam, which can be greatly focused around 50 nm. It allows finer analysis within the abrasion raster, giving SIMS some mapping capability. The ToF-SIMS system used in this study was from ION-TOF, and enables profiling of the elements making up the samples, within ppm mass detection limit, i.e. > $1 \cdot 10^{16}$–$1 \cdot 10^{18}$ cm^{-3} concentrations.

II·B·3 Electronic properties

II·B·3·a Bulk resistivity: 4-point probe

One can determine the resistivity of a semiconductor bulk of large dimensions through the 4-point probe method. In this method, originally described by Valdes [86], four relatively close probes contact the sample. The probes are spaced out by a distance s. Current I is sent between probes 1 and 4, while voltage V is measured between probes 2 and 3. A schematic of this method is drawn in Figure II·11.

Consider a large and thick sample (its length L, width W and thickness d are significantly larger than s). The potential induced by the current varies with the surface area of equipotential hemispheres. Differential calculus on the half hemisphere growing between probe 2 and 3 lead from $\mathrm{d}R = \rho \mathrm{d}r/\pi r^2$ to $\rho = 2\pi sV/I$, which are measured by the probes. Bulk resistivity of reference samples was checked with a Napson RT-3000 device, to obtain correct calculation of the effective lifetime (§ II·B·3·c·i).

II·B·3·b Charge carrier density: Hall Effect

Electrons and holes are charges paricles that, when exposed to electric $\vec{E}$ and magnetic $\vec{B}$ fields, are subject to the Lorenz force, $\vec{F_L} = q\vec{E} + q\vec{v} \times \vec{B}$. This force allows the emergence of the Hall Effect, illustrated in Figure II·12.

Considering a material of dimensions (L, t) in the (y, z) directions, through which flows a current I along the x-axis, subject to a magnetic field along the z-axis, the flow of carriers is bent in the y plane. It leads to an accumulation of electrons on one side of the sample in the y direction, and holes on the opposite side, *i.e.* to the formation of an electric field E_H and to a potential V_H along the y-axis. In steady state, E_H compensates F_L so:

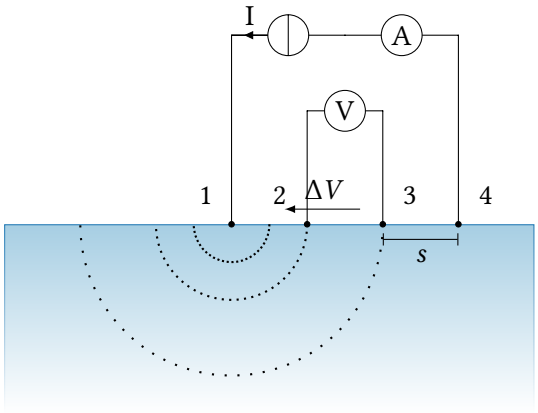

Figure II·11: Schematic of a 4-point probes apparatus, with equipotential hemispheres represented with dotted lines.

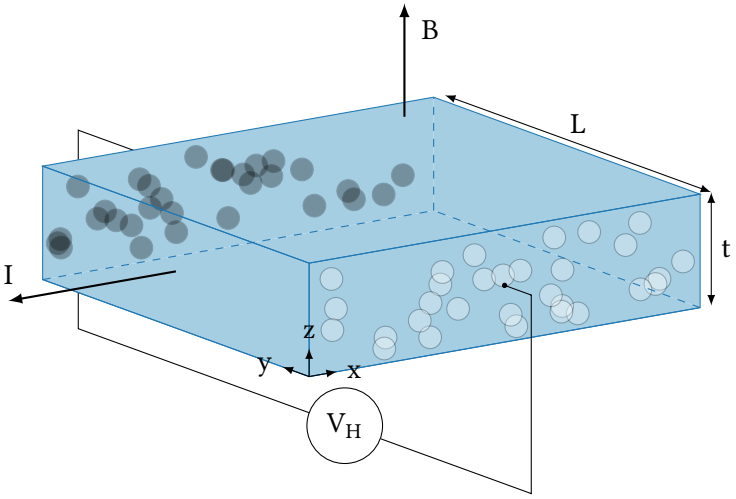

Figure II·12: Schematic representation of the Hall Effect and its measurement.

$$q\overrightarrow{E_H} + q\vec{v} \times \vec{B} = \vec{0} \xrightarrow[\text{y-projection}]{} E_H = vB \Longrightarrow V_H = vBL$$

Considering only the current of electrons with j the current density, their speed is:

$$v = \frac{j}{qn_0} = \frac{I}{L \cdot t \cdot qn_0} \Longrightarrow \frac{I \cdot B}{t} \cdot R_H$$

R_H is the Hall coefficient, which is pondered with the Hall factor r_H in semiconductors to accommodate the electron and hole currents:

$$R_H = r_H \frac{1}{qn_0}$$

The two Hall Effect devices available for this study enable combined measurements of carrier density between 17 and 770 K. As evoked in Chapter I, carrier concentration in the conduction band depends on the temperature, as the position of the Fermi level depends on the temperature. By increasing the temperature, one can "scan" a part of the bandgap with the Fermi level starting from the conduction band in n-type silicon and the valence band in p-type semiconductor, towards the middle of the bandgap. When the Fermi level crosses the energy level of a dopant, it releases its carriers. The increase in carrier density can be monitored by deriving the carrier density [87, 88]. However, this "Hall effect" spectroscopy technique is limited by the ionization of intrinsic silicon atoms at higher temperatures. This leads to a drastic increase of the carrier concentration that masks the variations brought by the deeper levels [89].

II·B·3·c Carrier effective lifetime

Minority carrier lifetime is an important characteristic in solar cell precursors: the longer the generated electron-hole pairs roam before recombination, the higher their chance to reach the space charge region, to be separated and finally to be extracted from the solar cell. The recombination mechanisms that take place in semiconductors were presented in § I·A·4·a, and these contributions affect bulk lifetime τ_b and surface lifetime τ_s. Altogether they result in the effective lifetime τ_{eff}, as shown in Equation II·2. During this work, effective lifetime is measured by QSSPC and μWPCD, and can be indirectly observed in precursors and finished solar cells through photoluminescence.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_s} \tag{II·2}$$

II·B·3·c·i Quasi steady-state photoconductance: QSSPC

A WCT-120 Sinton instrument is used to measure minority carrier lifetime τ_{eff} as a function of injection level (Δn in p-type silicon) in unmetallised samples. Injection level is measured from the sample conductivity that is deduced from the wafer conductance measured by a RLC circuit [90]:

$$\sigma = G \cdot A \cdot t \tag{II·3}$$

$$\Delta n(t) = \frac{\Delta\sigma(t)}{q(\mu_n + \mu_p)} \tag{II·4}$$

where G is the sample conductance,
A is the measurement area, a 5 cm large disk,
t is the sample thickness,
$\Delta\sigma$ is the sample conductivity,
q is the elementary charge,
μ_n,μ_p are electron and hole mobilities,

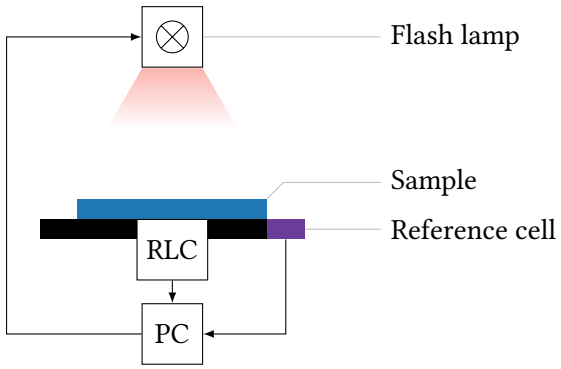

Figure II·13: Sketch of working principle of a QSSPC lifetime measurement apparatus.

As depicted in Figure II·13, such injection is obtained thanks to an infrared flash lamp that homogeneously generates electron-holes pairs inside the silicon wafer maintained at 25℃. As the carrier injection sharply increases at the beginning of the flash, wafer conductivity increases as well, until the flash ends. Carriers then recombine and their number and the subsequent conductivity follow a characteristic decrease, from which can be extracted the effective lifetime. Carrier generation rate U is determined through the measurement of a reference solar cell, and the effective lifetime is given with 10% uncertainty. The tool has four measurement modes that are chosen depending on the lifetime of the sample. These modes affect the duration of the flash which, compared to the carrier lifetime, enables approximations of the generalized equation. These modes are summarized in Table II·4.

Such measurement allows the calculation of effective lifetime as function of Δn, that can be extracted at 1 sun injection level and give the implied-Voc (see § II·B·3·e) [90]. This value is convenient in heterojunction structures, as it gives preliminary information on the final V_{oc} of

Table II·4: Measurement modes provided in the Sinton WCT-120.

Mode	Flash decay	Lifetime range	τ_{eff}
QSSPC	2 ms	< 200 µs	$\Delta n/U$
Generalized 1/1		Intermediary	$\frac{\Delta n}{U-\frac{\partial \Delta n}{\partial t}}$
Generalized 1/64	< 2 µs		
Transient		> 150 µs	$\Delta n/\frac{\partial \Delta n}{\partial t}$

the cell. If this V_{oc} is noticeably lower than the iV_{oc}, one can assume that the fabrication steps after passivation (*i.e.* metallization) hinder the carrier extraction.

$$\begin{aligned} iV_{oc} &= \frac{kT}{q} \ln\left(\frac{np}{\left(n_i^2\right)}\right) \\ &\approx \frac{kT}{q} \ln\left(\frac{(N_A + \Delta n)\Delta n}{n_i^2}\right) \text{ in n-type semiconductors} \end{aligned} \tag{II·5}$$

II·B·3·c·ii Microwave photoconductance decay: µWPCD

Another way to determine the effective lifetime in samples also monitors the variation of conductivity with another carrier injection technique. Microwave photoconductance decay (µWPCD), as shown in Figure II·14, measures the variation of conductivity by monitoring the unmetallised sample microwave reflection that depends on it. Carrier injection is obtained with a pulsed infrared laser, with an optional bias lamp.

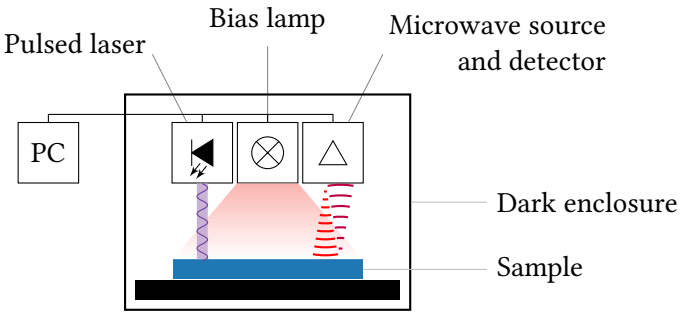

Figure II·14: Sketch of working principle of a µWPCD lifetime measurement apparatus.

The pulsed laser injection and the microwave sensing are local, which allows for lifetime mapping with small raster (typically half a millimetre, or less). Laser injection is quite high, and the lifetimes given by µWPCD are thus generally lower than the ones given by QSSPC at 1 sun, as Auger recombinations take place. The measurement is performed with a Semilab WT-2000 sys-

tem, which can make lifetime mapping of the samples. With the bias lamp, it can also statically monitor the carrier lifetime evolution, with no mapping capability.

II·B·3·c·iii Photoluminescence: PL

Photoluminescence is a quick method to obtain a map of the defects in silicon ingots, wafers and solar cells [91]. It basically gives, within seconds, a picture of the quality of the samples. The PL tool used in this study to characterise finished solar cells is manufactured by BTI, and is sketched in Figure II·15.

Even though radiative recombination is quite limited in indirect bandgap semiconductors, some photons are still emitted when carriers recombine. The photoluminescence tool used in this study consists in generating carriers thanks to a laser (1.35 eV) and detecting the photons at the silicon bandgap energy with a CCD. The presence of defects in silicon or the interfaces decreases the number of radiative recombinations. Hence, the darker the PL image, the more defective the precursor or the solar cell, and the lower the effective lifetime.

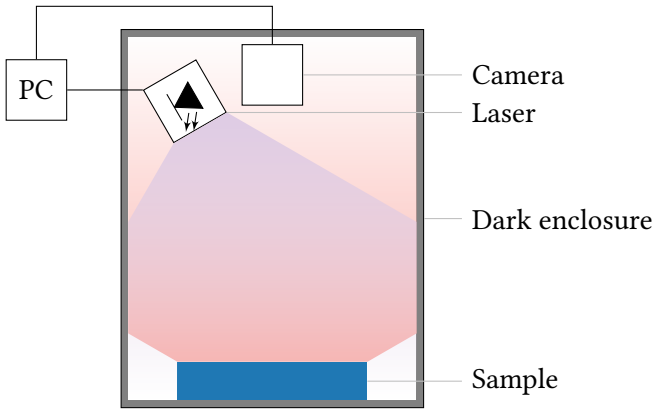

Figure II·15: Sketch of the photoluminescence measurement setup.

II·B·3·d Solar cells performances

Solar cells can be modelled with the equivalent circuit drawn in Figure II·16. An ideal solar cell can be represented as a current generator (whose current is a function of the ambient light) in parallel with a diode. Real solar cells can be modelled with:

- A light-dependent current generator I_L;
- A first diode in parallel (with ideality for 1<n<2) that depicts diffusion mechanisms;
- A second diode (n>2.5 for SHJ solar cells) that represent recombination mechanisms;
- A parallel resistance that accounts for shunts, i.e. short-circuits that bypass the junction;

- A series resistance that accounts for any barrier to the flow of carriers across the solar cell (base resistance, emitter resistance, contact resistance between semiconductors and metals, and resistance of the metals themselves).

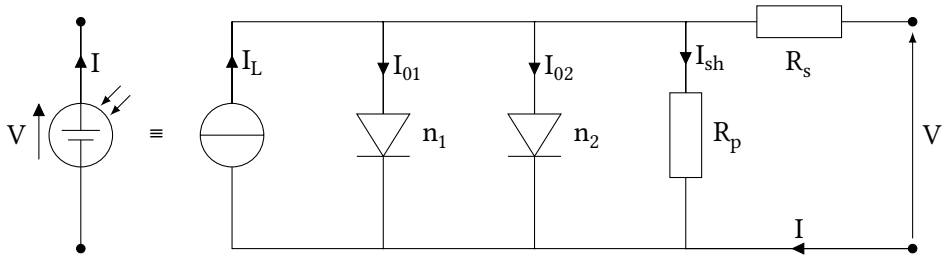

Figure II·16: Equivalent circuit of a solar cell.

The following techniques enable the assessment of the components of the model, through the measurement of the current density vs voltage curve, at dark or under a solar simulator, and the collection efficiency per wavelength by the decomposition of the solar spectrum.

II·B·3·e Current-density–voltage curve: J–V

Solar cells performances are given with the J–V curves instead of the I–V, to be independent of the solar cell area. Indeed, depending on the maturity of the deposition techniques, large area solar cells may not be obtainable. Dividing the measured current by the solar cell area enables a better comparison between technologies.

Current-voltage characteristic can be measured under illumination to determine the solar cell performances, and without illumination to determine the resistances and diodes of the equivalent model.

II·B·3·e·i J–V under illumination

The light spectrum available on Earth results from the solar light spectrum that is filtered by the air mass (AM). The normalised irradiance is given at 1000 W/m² and by the AM1.5G spectrum (Figure II·17) that combines direct irradiance from the Sun and light scattered by the sky. A Xenon lamp with tailored filters is used to render the AM1.5G spectrum, and the solar cell is put on a holder that acts as temperature regulator (25℃) and back contact. Front contact is taken with a comb aligned on the busbar.

By varying the charge connected to the solar cell, one can measure the J–V curve and extract the cell parameters:

- V_{oc}, the open-circuit voltage at J=0;
- V_{oc}, the short-circuit current at V=0;
- J_{mpp},V_{mpp}, the current density and voltage at the maximum power point P_m of the cell;

- *FF*, the fill factor which is the ratio of Pm to the product of Voc and Jsc:

$$FF = \frac{J_{mpp} \cdot V_{mpp}}{J_{sc} \cdot V_{oc}} \tag{II·6}$$

- η, the conversion efficiency:

$$\eta = \frac{J_{sc} \cdot V_{oc} \cdot FF}{P_{in}} \tag{II·7}$$

with P_{in} the input power of the light which is 1000 $W \cdot m^{-2}$ for the AM1.5G solar simulator.

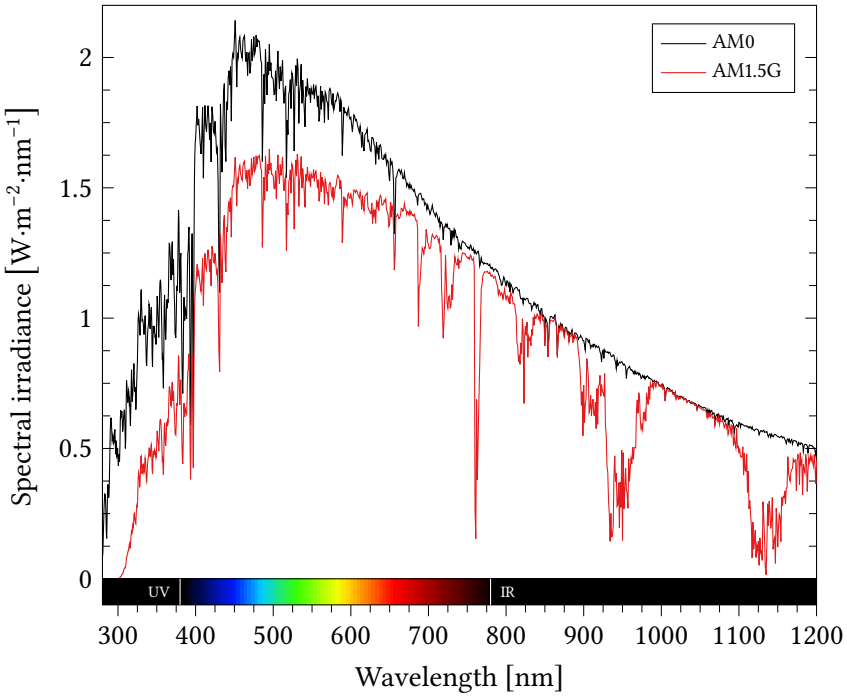

Figure II·17: Solar irradiance spectra in space (AM0) and on Earth (AM1.5G).

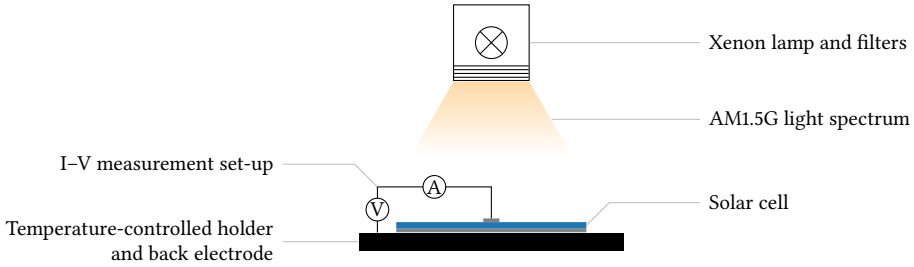

Figure II·18: Solar simulator set-up.

II·B·3·e·ii J–V without illumination : Dark-J–V

At dark, one can measure the carrier transport across the device and determine its series resistance, the diodes currents, and ideality factors. Series resistance is deduced from the shift between dark current and current delivered under illumination with the following equation [92].

$$R_s = \frac{V_{mpp}^{dark} - V_{mpp} - \left|J_{sc} - J_{mpp}\right| R_s^{dark}}{\left|J_{mpp}\right|} \tag{II·8}$$

where $R_s^{dark} = \frac{V_{Jsc}^{dark} - V_{oc}}{|J_{sc}|}$;
V_{mpp}^{dark} is the voltage measured at dark at J_{mpp};
$V_{J_{sc}}^{dark}$ is the voltage measured at dark at J_{sc};

Finally the equation of the equivalent circuit described in Figure II·16 in the following equation [93].

$$J - V = J_{01}\left[\exp\left(\frac{q(V - J \cdot R_s)}{n_1 \cdot k_B \cdot T}\right) - 1\right] + J_{02}\left[\exp\left(\frac{q(V - J \cdot R_s)}{n_2 \cdot k_B \cdot T}\right) - 1\right] + \frac{(V - J \cdot R_s)}{R_p} \tag{II·9}$$

where J_{01}, J_{02} are the saturation current densities of the two equivalent diodes;
J_{sc} is the photogenerated short-circuit current.

Parallel resistance can be extracted at low current density obtained in reversed bias. Then the ideality factors of the diodes can be fitted. An example set of J–V and dark-J–V, with a representation of the values used in the equation is plotted in Figure II·19. From the equations above, one can summarize the behaviour of the J–V curves under the influence of the resistances and currents:

- The slope near $V = 0$ increases as R_p decreases;
- The slope near $V = V_{oc}$ decreases as R_s increases.

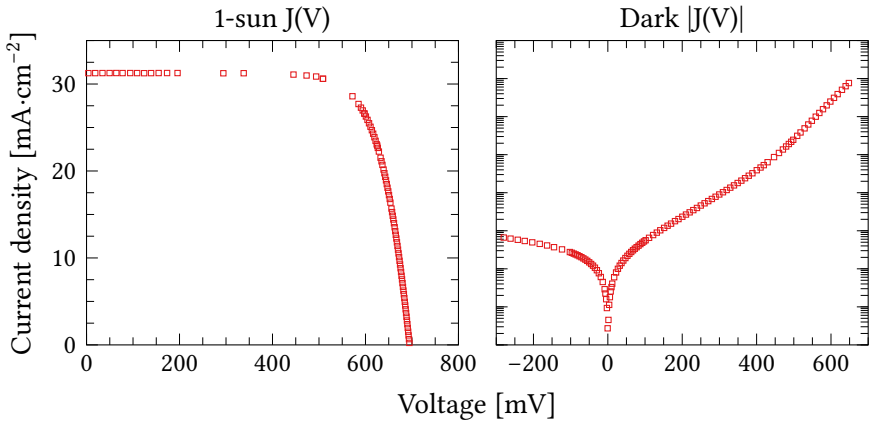

Figure II·19: J–V and dark-J–V curves of a reference SHJ solar cell of this study.

II·B·3·f Pseudo-J–V curve: Suns-V_{oc}

Suns-V_{oc}, a tool similar to the lifetime measurement tool, can be used to monitor the J–V curve generated by metallised solar cell during a flash. As the flash duration is very short, one can consider that no carrier transport occurs. The measured pseudo-J–V and resulting pseudo-FF (pFF) are a representation of the solar cell performance unhindered by the series resistance. $pVoc$ can also be extracted from the pseudo-J–V curve, which gives an indication of the Voc after the metallization steps.

II·B·3·g Internal and external quantum efficiency: IQE and EQE

Quantum efficiency (QE) is the measurement of the ability of a photosensible device to generate current under illumination, *i.e.* the ratio of the number of generated electrons to the number of photons sent to the device, for each photon wavelength. It can be either external (EQE) or internal (IQE), whether light lost by reflection (R) is taken into account or not.

As shown by the Figure II·20, a monochromatic beam is chopped and split in two. The power P of the first beam is measured as reference to determine $N_{h\nu}$, as stated in Equation II·10.

$$P = N_{h\nu} \cdot \frac{hc}{\lambda} \cdot \Delta t^{-1} \tag{II·10}$$

where P is the power of the incident monochromatic beam;
$N_{h\nu}$ is the number of incident photons;
λ is the wavelength of the photons;
Δt is the time constant of the beam chopper.

The second part of the beam is redirected onto the solar cell that delivers the current I. The number of generated electrons by the solar cell is:

$$N_e = \frac{I}{q} \tag{II·11}$$

The light power reflected by the solar cell is measured to determine the reflectivity $R(\lambda)$. Synchronous measurement between the chopper, the current and the power meters is ensured by a lock-in amplifier and the measurement data is delivered to a computer to calculate the EQE and IQE:

$$EQE(\lambda) = \frac{N_e(\lambda)}{N_{h\nu}(\lambda)} \tag{II·12}$$

$$IQE(\lambda) = \frac{EQE(\lambda)}{(1 - R(\lambda)} \tag{II·13}$$

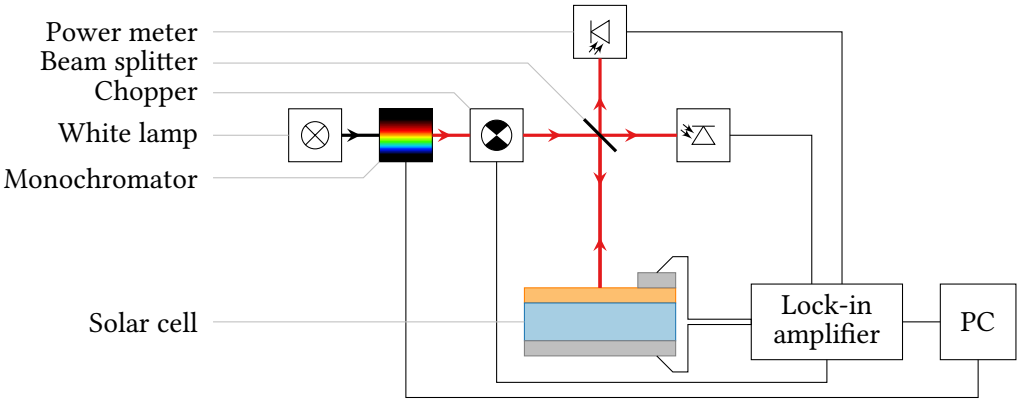

Figure II·20: Quantum efficiency measurement set-up.

The local measurement of IQE is a convenient way obtain the collection efficiency as a function of wavelength, freed from the effects of the geometry of the solar cell (reflection, shadowing) and only limited by the recombinations in the materials and at their interfaces. Figure II·21 shows a typical IQE of a SHJ solar cell, with an ideal IQE (100% collection efficiency for any photon energy higher than the bandgap, 0% below). In real solar cells, front side materials mainly drive the collection efficiency of short-wavelength photons, while silicon bulk collects the longer-wavelength, IR photons.

Finally, it is possible to calculate the short circuit current density by integration of the external quantum efficiency with the spectral irradiance $\Phi_{AM1.5G}$. The calculation of this pseudo-J_{sc} is independent on the light source and the shadowing effect of the front grid:

$$pJ_{sc} = -q \int EQE(\lambda) \cdot \Phi_{AM1.5G} \cdot \frac{\lambda}{h \cdot c} \cdot \mathrm{d}\lambda \tag{II·14}$$

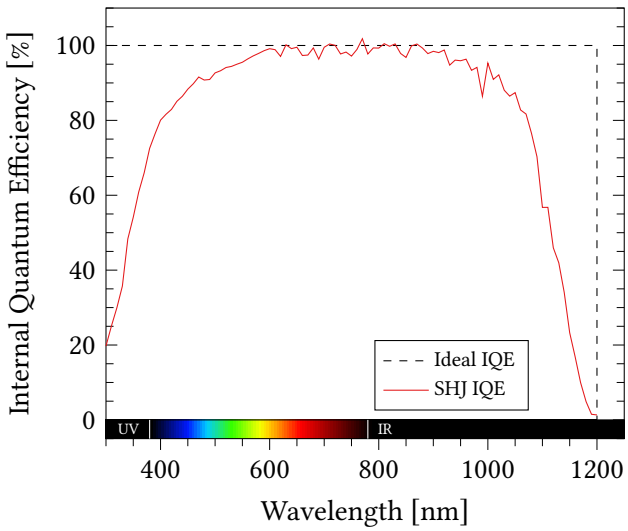

Figure II·21: Internal quantum efficiency vs wavelength of an ideal and a real SHJ solar cells.

II·B·3·h Pseudo-efficiency

Combining the iV_{oc}, pJ_{sc}, and pFF obtained earlier, one can calculate the pseudo-efficiency:

$$p\eta = \frac{pJ_{sc} \cdot iV_{oc} \cdot pFF}{1000\,\mathrm{W{\cdot}m^{-2}}} \tag{II·15}$$

The pseudo-efficiency is a representation of the efficiency that could be obtained if the solar cell performances were only dependent on their carrier lifetime and optics, unhindered by:

- The shadowing effect from the front metal grid;
- High series resistance;
- Low shunt resistance;
- Any degradation of the passivation, or with potentially degraded passivation if pV_{oc} is used instead of iV_{oc}.

II·C Heterojunction solar cells simulation: AFORS-HET

AFORS-HET is a numerical simulation tool for solar cells and their measurements [94]. Simulated measurements are plentiful (alternative or direct current, QSSPC, quantum efficiency, etc.), and simulations are based on the provided material properties (bandgap, doping, thickness, etc.), traps characteristics (capture cross-sections, energy levels, concentration, etc.), illumination (monochromatic, AM1.5g), and the carrier transport models (drift-diffusion, tunnelling, etc.). In this work, AFORS-HET was used for the simulation of IQE curves as a function of defects concentration.

Table II·5 resumes the typical parameters for the simulations used in this study. Silicon lifetime is obtained in the model by introducing a virtual neutral defect in the middle of the bandgap.

Table II·5: Simulation parameters used in for a-Si:H/c-Si and GaP/c-Si solar cells simulation.

Layer parameters	Unit	(p) a-Si:H	(i) a-Si:H	(n) a-Si:H	(p) c-Si	Interface D_{it}	(n) GaP
Thickness t		20 nm	3 nm	10 nm	280 µm	1 nm	10 nm
Band gap E_g	eV	1.72	1.74	1.72	1.124	1.124	2.26
Dopant concentration N_A/N_D	cm^3	$1 \cdot 10^{20}$	0	$6.9 \cdot 10^{19}$	$1 \cdot 10^{15}$	$1 \cdot 10^{15}$	$1 \cdot 10^{19}$
Relative dielectric constant	–	11.9	11.9	11.9	11.9	11.9	11.1
Electronic affinity χ	eV	3.9	3.85	3.9	4.05	4.05	3.8
Electron mobility μ_e	$cm^2 \cdot V^{-1} \cdot s^{-1}$	1	1	1	1430	1430	250
Hole mobility μ_h	$cm^2 \cdot V^{-1} \cdot s^{-1}$	0.5	0.5	0.5	480	480	130
Electron thermal velocity v_e^{th}	$cm \cdot s^{-1}$	$1.0 \cdot 10^7$	$1.0 \cdot 10^6$	$1.0 \cdot 10^7$	$1.0 \cdot 10^7$	$1.0 \cdot 10^7$	$2.0 \cdot 10^7$
Hole thermal velocity v_h^{th}	$cm \cdot s^{-1}$	$1.0 \cdot 10^7$	$1.0 \cdot 10^6$	$1.0 \cdot 10^7$	$1.0 \cdot 10^7$	$1.0 \cdot 10^7$	$1.3 \cdot 10^7$
Equivalent density in CB N_C	cm^3	$1 \cdot 10^{20}$	$1 \cdot 10^{20}$	$1 \cdot 10^{20}$	$2.84 \cdot 10^{19}$	$2.84 \cdot 10^{19}$	$1.8 \cdot 10^{16}$
Equivalent density in VB N_V	cm^3	$1 \cdot 10^{20}$	$1 \cdot 10^{20}$	$1 \cdot 10^{20}$	$3.1 \cdot 10^{19}$	$3.1 \cdot 10^{19}$	$1.9 \cdot 10^{19}$
Neutral defect at 0.56 eV :							
Concentration	cm^3	–	–	–	$1 \cdot 10^9$	–	–
Electron capture cross section σ_e	cm^2	–	–	–	$1 \cdot 10^{-14}$	–	–
Hole capture cross section σ_h	cm^2	–	–	–	$1 \cdot 10^{-14}$	–	–
Urbach band tails :							
Conduction band tail energy	eV	0.08	0.035	0.068	–	–	–
Valence band tail energy	eV	0.12	0.05	0.094	–	–	
σ_e and σ_h	cm^2	$7 \cdot 10^{-16}$	$7 \cdot 10^{-16}$	$7 \cdot 10^{-16}$	–	–	–
Acceptor (A) and Donor (D) Gaussian states :							
Maximum state density	$cm^3 \cdot eV^{-1}$	$2 \cdot 10^{21}$	$1.4 \cdot 10^{16}$	$2 \cdot 10^{21}$	–	$3 \cdot 10^{17}$	–
A (D) position above E_V	eV	1.2 (1.1)	1.09 (0.89)	0.6 (5)	– –	0.761 (0.561)	– –
Standard deviation	eV	0.21	0.144	0.21	–	0.2	–
σ_e (σ_h) for A	cm^2	$3 \cdot 10^{-15}$ ($3 \cdot 10^{-14}$)	$3 \cdot 10^{-15}$ ($3 \cdot 10^{-14}$)	$3 \cdot 10^{-15}$ ($3 \cdot 10^{-14}$)	– –	$3 \cdot 10^{-15}$ ($3 \cdot 10^{-14}$)	– –
σ_e (σ_h) for D	cm^2	$3 \cdot 10^{-14}$ ($3 \cdot 10^{-15}$)	$3 \cdot 10^{-14}$ ($3 \cdot 10^{-15}$)	$3 \cdot 10^{-14}$ ($3 \cdot 10^{-15}$)	– –	$3 \cdot 10^{-15}$ ($3 \cdot 10^{-14}$)	– –

III Minority carrier lifetime degradation during GaP/Si solar cells fabrication

GaP/Si heterojunctions fabricated by MBE or MOCVD have consistently been degraded when subjected to high temperature steps in the deposition chambers [9, 73–75, 95, 96]. The degradation was observed by bulk lifetime and photoluminescence degradation in solar cells precursors, associated with V_{oc} loss in finished solar cells. In this chapter, the electrical performances of solar cells fabricated in collaboration between INES and LTM will be analysed, to confirm the interest of GaP as hetero-emitter and to give some insight to the source of the degradation. To further the study, silicon bulk degradation will be then analysed through carrier lifetime measurements, and attempts to quantify and prevent it will be deployed. Passivation of silicon surface by GaP will also be assessed as another source of degradation.

The first solar cells processed between LTM and INES were based on p-type, 4-inch, 280-µm-thick silicon wafer (due to the requirements and limitations discussed in § II·A·1) with 10-nm-thick front-side GaP layer, 75-nm-thick ITO layers, full-sheet 400-nm-thick back-side silver layer, and a top electrode deposited by evaporation through a shadow mask. Solar cells were also made out of n-type silicon substrates, with inverted emitter structure (the GaP layer acting as a window on the front side in this later case). [2] The process flow for GaP/c-Si solar cell fabrication as well as for reference a-Si:H/c-Si is schematized in Figure III·1. A picture of a 5×5cm fabricated cell is presented in Figure III·2. Three kind of solar cells, each fabricated on n-type and p-type bulk silicon, are compared:

SHJ reference These cells follow a process flow close to the one of a standard a-Si:H/c-Si solar cell, with an a-Si:H emitter. After HF deoxidation, (i/n)a-Si:H layers are deposited by PECVD on the front side. The solar cell precursor is then flipped over, and (i/p)a-Si:H layers are deposited with the same method. Front and rear ITO are then deposited by PVD, and front grid and back silver contacts are deposited by screen-printing.

GaP on 900℃ annealed Si These cells follow a process flow adapted for the fabrication of c-GaP/c-Si heterojunction solar cells. This includes a dry deoxidation step, a surface annealing step at 900 ℃, and a GaP deposition step. Afterwards, the rear surface is processed and the electrodes are deposited with the same processes as the reference cell.

SHJ with 900℃ annealed Si These cells follow a similar process flow as the c-GaP/c-Si cells for the dry deoxidation and the 900℃ annealing, but are then passivated and contacts are deposited with the full process flow of the a-Si:H/c-Si solar cells (HF-based deoxidation followed by intrinsic and n-type hydrogenated amorphous silicon deposition).

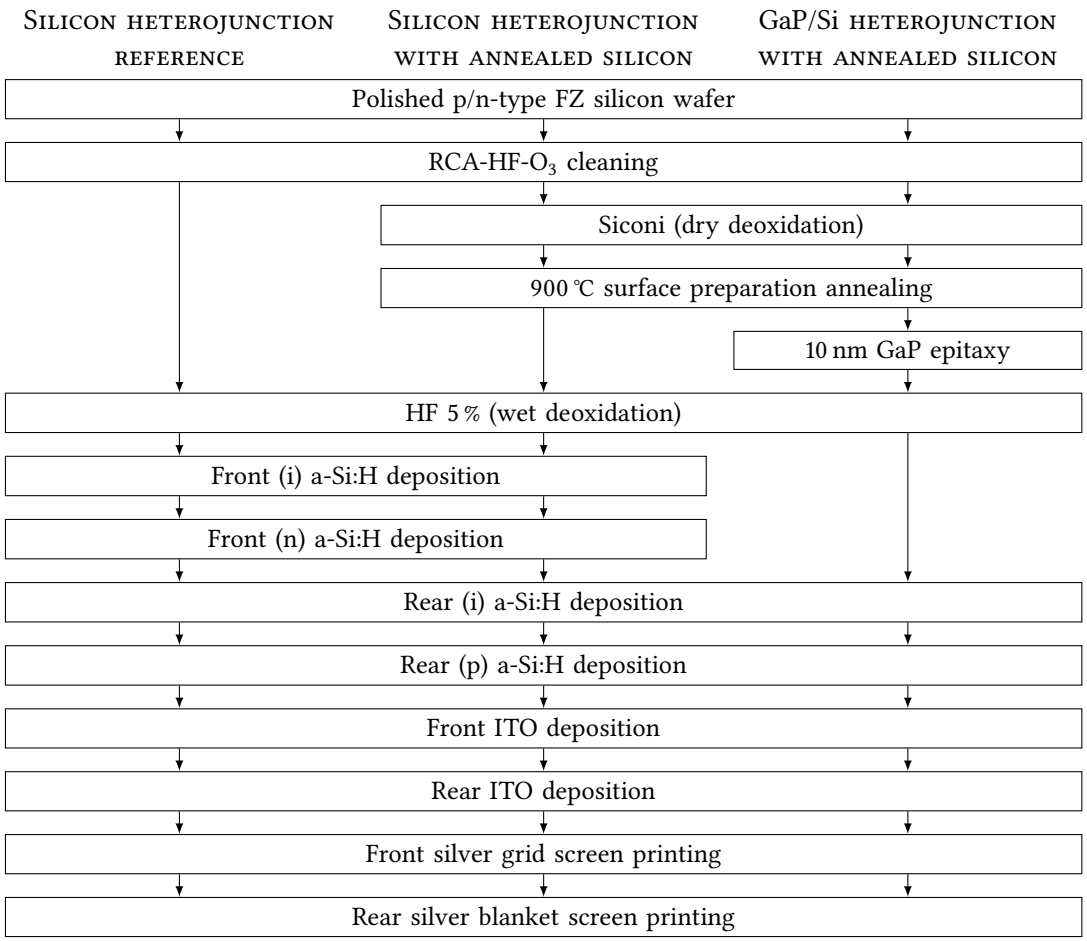

Figure III·1: Initial process flow of a-Si:H/Si and GaP/Si solar cells. [74]

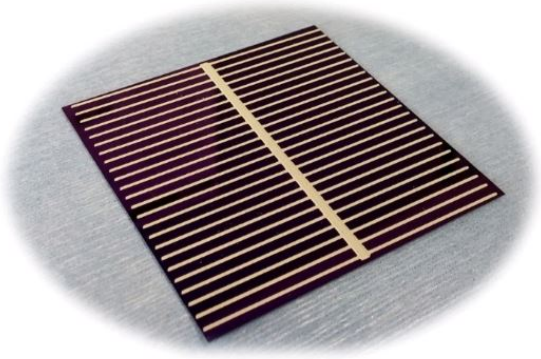

Figure III·2: Picture of a GaP/Si solar cell.

III·A Solar cells measurements

The J–V characteristics of the solar cells measured under 1 sun AM1.5G illumination are presented in Figure III·3 and are summarized in Table III·1.

Table III·1: J–V characteristics of a-Si:H/Si and GaP/Si solar cells.

Solar cell		1-sun IV				SunsVoc
Si	Type	V_{oc} [mV]	J_{sc} [mA·cm^{-2}]	FF [%]	η [%]	pFF [%]
P	SHJ reference	676	25.2	72.6	12.4	76.7
	SHJ with annealed silicon	566	26.2	74.6	11.0	80.2
	GaP on annealed silicon	520	27.2	73.1	10.4	80.6
N	SHJ reference	694	26.1	76.8	13.9	78.3
	SHJ with annealed silicon	621	25.4	67.4	10.4	69.8
	GaP on annealed silicon	448	3.9	56.4	1.0	59.2

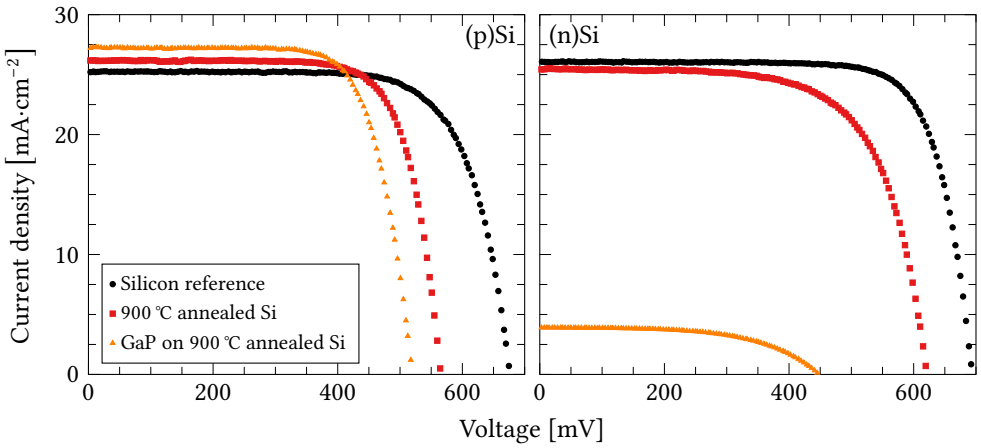

Figure III·3: J–V curves of a-Si:H/Si and GaP/Si solar cells.

The GaP/(p)Si solar cells display increased J_{sc} (+2 mA·cm^{-2} from the reference to GaP/Si solar cell) which could be attributed to the better transparency of GaP vs a-Si:H in the UV. pFF and FF are also higher than in the references, which may be linked to the expected field effect passivation induced by the GaP. However, a notable drop in V_{oc} is observed: from the reference c-Si passivated with a-Si:H above 670 mV, V_{oc} is reduced by 110 mV with annealed c-Si, and lowered down to 520 mV with the GaP/Si heterojunction. This degradation of V_{oc}, occurring as early as the surface preparation annealing, and worsened by the GaP deposition, hints at a degradation of silicon bulk and a low passivation of the GaP/Si interface.

Solar cells fabricated from n-type substrates, however, show a degradation of all J–V characteristics after substrate annealing, whether it is followed by GaP deposition or not. The per-

formances of the GaP/(n)Si solar cell are specifically low, with V_{oc} below 450 mV, almost no current extracted and a resulting efficiency around 1%.

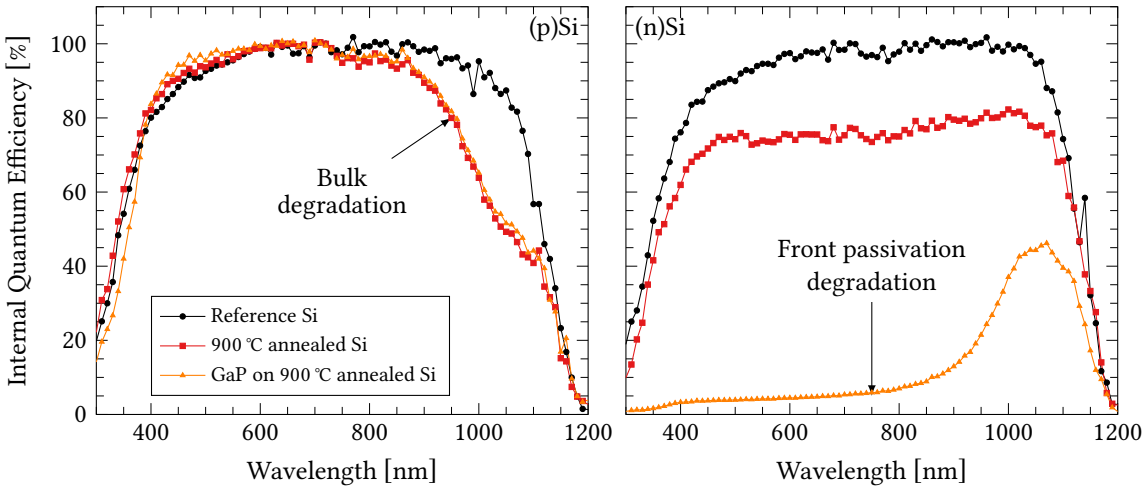

Figure III·4: Internal Quantum Efficiencies of initial solar cells fabricated from (left) p-type substrates and (right) n-type substrates (from [9]).

The IQE of the GaP/(p)Si solar cell displays a higher collection efficiency for short wavelengths between 400 and 600 nm, which can directly be attributed to the better transparency of GaP than a-Si:H. The slightly lower IQE between 300 and 400 nm may be attributed to optical effects between ITO and GaP . However, IQE is significantly degraded between 800 and 1200 nm if the substrate has been annealed, which corroborates the drop in V_{oc} and the bulk degradation of these cells.

This degradation is also observed in the inverted emitter solar cells, based on n-type substrates, where the IQE of the reference solar cell with annealed wafer uniformly drops across the whole spectrum. The inverted emitter GaP/Si solar cell, however, has a dramatically low IQE for the wavelengths between 300 and 900 nm, with a small bump between 900 and 1200 µm, with an overall maximum below 50% collection efficiency. This behaviour is typical of inverted emitter solar cells with high surface recombination on front side: GaP/Si interface is poorly passivated [9]. Indeed, short wavelength photons are absorbed on the front side of solar cells. If the front surface is highly recombining, the carriers generated by their absorption cannot contribute to the photo-generated current, as they are lost. However, longer wavelength photons, in IR range, are transparent to GaP and are absorbed deeply in the bulk, closer to the back surface which is here passivated. These IR photons can contribute to the photo-generation, and are seen in the bump observed in IQE.

To determine the origin of the V_{oc} and IQE degradations observed in the solar cells, one can study the minority carrier lifetime.

III·B Carrier lifetime degradation origins

The electrical performance of the solar cells depend on the carriers ability to be generated, to move across the silicon bulk, and to be extracted before recombination. If recombination probability is increased, due to trap-assisted recombinations or Auger recombinations brought by high injection levels, lifetime of the carriers is decreased.

III·B·1 Lifetime vs epitaxy steps

The following figure reports the evolution of carrier lifetime through the epitaxy steps on different FZ precursors: 10-nm-thick GaP directly deposited on pristine silicon, annealed silicon, GaP on annealed silicon. Reference precursor and wafer sides without GaP are passivated with thick a-Si:H, which brings little-to-no limitation to the interfacial lifetime [97, 98]. After epitaxy steps and a-Si:H passivation, lifetime is measured by a Sinton setup (see § II·B·3·c·i) and reported in Figure III·5. To assess the interface lifetime degradation induced by the processing, all deposited layers are then etched, along with the first micrometres (10 µm) of silicon, samples are cleaned and finally passivated again. The subsequent lifetime is reported by the second set of red bars.

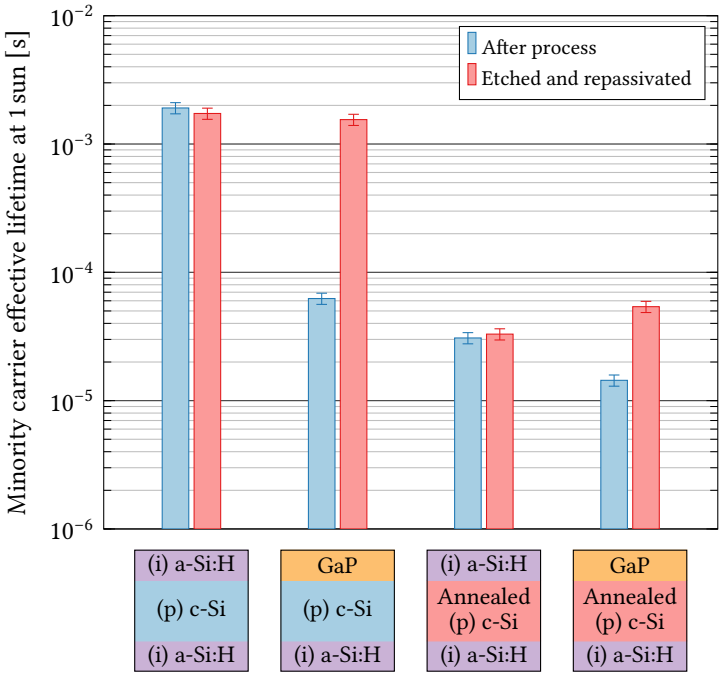

Figure III·5: QSSPC τ_{eff} at 1 sun, after epitaxy steps, before and after etching processes, on FZ silicon samples.

The minority carrier lifetime of reference precursors is high, above 1 ms, and remains high after etching and repassivation. Thus, reference substrate quality is good, a-Si:H passivation can be considered optimal ($\tau_{a\text{-}Si:H} \rightarrow \infty$), and the etching and repassivation process does not degrade lifetime.

Whether GaP is deposited or c-Si is annealed, the minority carrier lifetime is low (< 100 µs). However, etching GaP from unannealed c-Si and repassivating restores lifetime to the one of the reference level. Hence, GaP deposition alone does not degrade bulk minority carrier lifetime, but lifetime is limited by the GaP/Si interface.

Etching GaP, or a-Si:H, from annealed c-Si and repassivating does not improve minority carrier lifetime: bulk lifetime is altered beyond 10 µm by the surface preparation annealing alone (> 20 µm according to [9]).

GaP deposited on annealed c-Si has lower minority carrier lifetime (Ĭ0 µs) than a-Si:H on annealed c-Si (30 µs) and GaP on unannealed c-Si (60 µs). Hence, even with preannealing, the surface passivation by GaP is not as good as the passivation by a-Si:H.

From these measurements, one can conclude that:

- GaP does not passivate the surface of unannealed silicon;
- Annealing silicon in MOCVD chamber deeply degrades the bulk minority carrier lifetime (> 10 µm);
- The GaP deposition step (without annealing) does not degrade the bulk silicon minority carrier lifetime.
- GaP may not passivate the surface of annealed silicon, or at least provide no better passivation than a-Si:H.

III·B·2 Discussion on the origin of minority carrier lifetime degradation

From the solar cells measurements, and the evolution of minority carrier lifetime in precursors due to the epitaxy steps, one can conclude that the drop in Voc is associated with low minority carrier lifetime. Figure III·6 summarizes the causes for minority carrier lifetime degradations. As stated in § II·B·3·c, effective minority carrier lifetime depends on two first-order contributions: bulk and interface lifetime.

- Bulk lifetime depends on:
  - Silicon bulk, which is initially pristine then deeply degraded by the surface preparation annealing that may:
    - Thermally activate intrinsic defects,
    - Bring extrinsic defects from the epitaxy chamber;
  - GaP bulk, that may contain:
    - Structural defects such as dislocations, twins, antiphase boundaries,
    - Contamination, most likely carbon left by epitaxy precursors;
- Interface lifetime depends on:
  - a-Si:H/Si interface, which is optimally passivated;

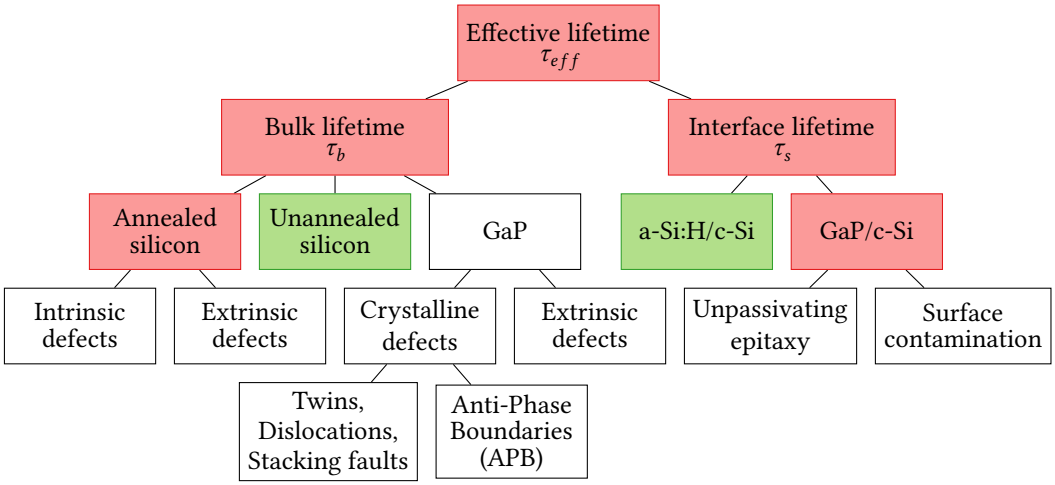

Figure III·6: Causal tree of possible minority carrier lifetime degradation origins.
Red elements are degraded, green ones are not, white ones are undetermined so far.

- GaP/Si interface, poorly passivated, whether the surface preparation is performed or not, which may come from traps brought by:
  - Unpassivated dangling bonds, left by unoptimized epitaxy,
  - Surface contamination, from cleaning fault, or epitaxy precursors.

In the rest of this chapter, the origins of the bulk and interface lifetime degradations will be investigated. The following chart summarises the considered origins.

III·C Silicon bulk degradation analysis

In this section, the probable source of the bulk silicon degradation and its dependency on the processing and measurement conditions will be investigated. First, its temperature dependency will be established.

III·C·1 Annealing temperature dependency

In a first set of experiments, we exposed 300 mm diameter CZ silicon wafers to an annealing step in the MOCVD chamber for different temperature. The samples are then cut in 5×5 cm pieces and passivated with a thick intrinsic a-Si:H layer before measuring the minority carrier lifetime by QSSPC.

In Figure III·7, effective lifetime is shown to severely decrease as annealing temperature is increased. The lifetime degradation is thus strongly dependent on the annealing temperature, with high temperatures generating more defects that limit carrier lifetime.

If one recalls the minority carrier lifetime of the sample annealed at 900℃ presented in Figure III·5, effective lifetime was 30 µs. For the set of experiments presented in Figure III·7, the only sample presenting a minority carrier lifetime above 30 µs are the one with an annealing temperature below 725℃. This means that the minority carrier lifetime of samples annealed at 900℃ in the previous set of experiments is better than the one of samples annealed at a lower temperature in the present set of experiments. Such a discrepancy has been observed at several occasions in the course of my Ph.D. and is not associated with silicon substrate variations (even if the presented data are from 100 mm and 300 mm wafers with different thickness here). This illustrates the consistent non-reproducibility of the degradation throughout the three years of experiments, which will be discussed next section.

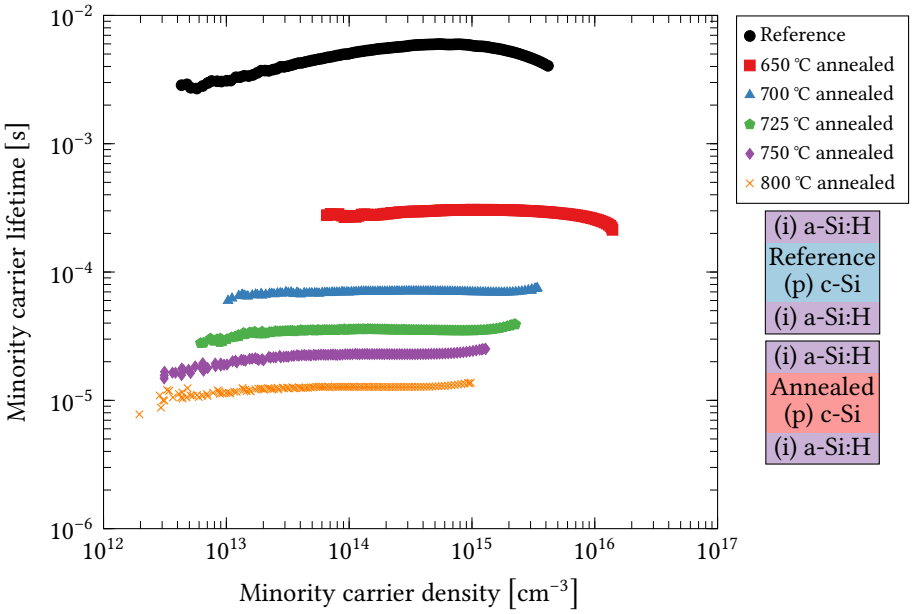

Figure III·7: QSSPC τ_{eff} of CZ samples with various annealing temperatures. All annealing steps were 10 min long, under 600 Torr H_2 pressure.

III·C·2 Reproducibility of degradation

Reproducibility in science is paramount. The same causes leading to the same consequences provide a comforting framework to conduct research. However, non-reproducibility of experiments lead to hard-to-interpret results.

Unfortunately, the preannealing step has demonstrated a great variability of the carrier lifetime degradation it induces. Figure III·8 shows such variability by plotting the lifetime measured after the same annealing recipe (900℃, 10 min, and 600 Torr) across the three years of this work. The given dates are the days when a-Si:H passivation and lifetime measurement were performed. Preannealing was generally done within a week before these dates. For reference,

unannealed FZ wafers passivated at the same time always display lifetime above 1 ms, with little variation.

These notable variations in the degradation make it quite dependent on the epitaxy chamber history, which is difficult to monitor and study, and make harder any quantification of the causes of the degradation.

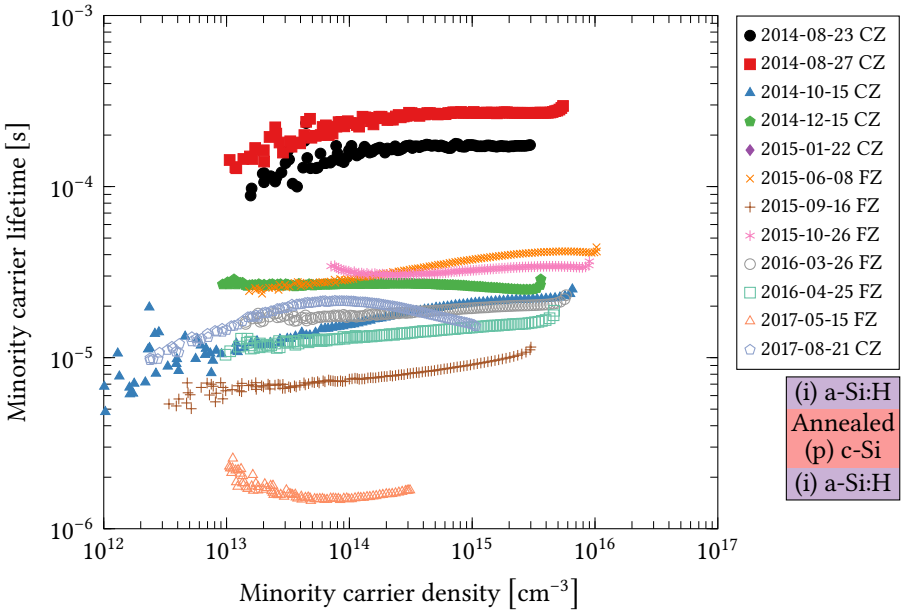

Figure III·8: QSSPC τ_{eff} resulting from 10 min 900℃ annealing at various dates during the span of this work, on CZ and FZ reference wafers.

III·C·3 Minority carrier lifetime distribution

QSSPC measurements only give an effective carrier lifetime on 5-cm-wide area (§ II·B·3·c·i). To get more information bulk silicon minority carrier lifetime degradation induced by the annealing step, a CZ wafer was annealed at 800℃ in the MOCVD chamber, then passivated with a-Si:H. Its minority carrier lifetime has then been mapped by µWPCD and reported in Figure III·9.

The main feature of this mapping is that the effective minority carrier lifetime has radial distribution, with higher lifetime in the centre and more degradation on the edges. This fact excludes thermal donors and boron-oxygen defects, which are, if present, in higher concentration at the centre of the wafer. The minority carrier lifetime span between 3 and 23 µs, which shows that despite a radial distribution, the minority carrier lifetime remains rather uniform (within one order of magnitude) across the whole wafer. One can also notice three spots of slightly higher lifetime forming an equilateral triangle: these are associated with the loading pins that retract

into the holder during processing. This means that the minority carrier lifetime is higher when the wafer is not in contact with the SiC-coated graphite holder. We can infer that the holder may be the source of the degradation, with contaminants coming from the SiC-coated graphite. This has also been established by Ohlmann *et al.* with similar annealing conditions [73].

In addition, 100 mm diameter FZ wafers were processed and analysed with the same methodology. As shown in Figure III·10, the degradation is more uniform despite drastically lower lifetimes at the edges. The smaller size of the FZ wafers, and the fact that they are maintained on a dedicated holder may improve the uniformity of the temperature near the centre of the wafer. In any case, the radial distribution of the 300 mm diameter silicon wafer is not transferred to the 100 mm diameter silicon wafers. Therefore, we can conclude that the radial distribution observed on the 300 mm silicon wafer does not originate from the chamber itself but rather from the original wafer or the thermal regulation of the silicon wafer.

These experiments indicate that the minority carrier lifetime degradation in the silicon substrate is rather uniform across the whole wafer, with a slightly lower lifetime close to the edges of the wafer. This also excludes boron-oxygen defect and thermal donors as the main source of lifetime degradation, and shows that the source of minority carrier lifetime degradation in the MOCVD chamber is rather uniform.

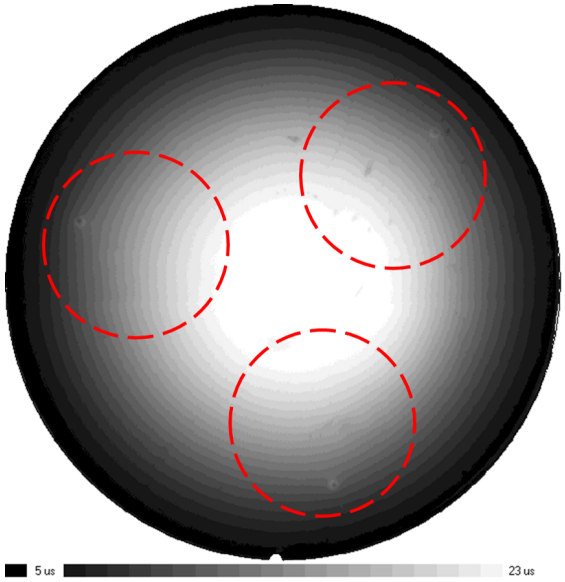

Figure III·9: µWPCD τ_{eff} mapping of an 800°C-annealed 300 mm wafer.
The approximate positions of the 100 mm imprints are suggested by the red dashed circles.

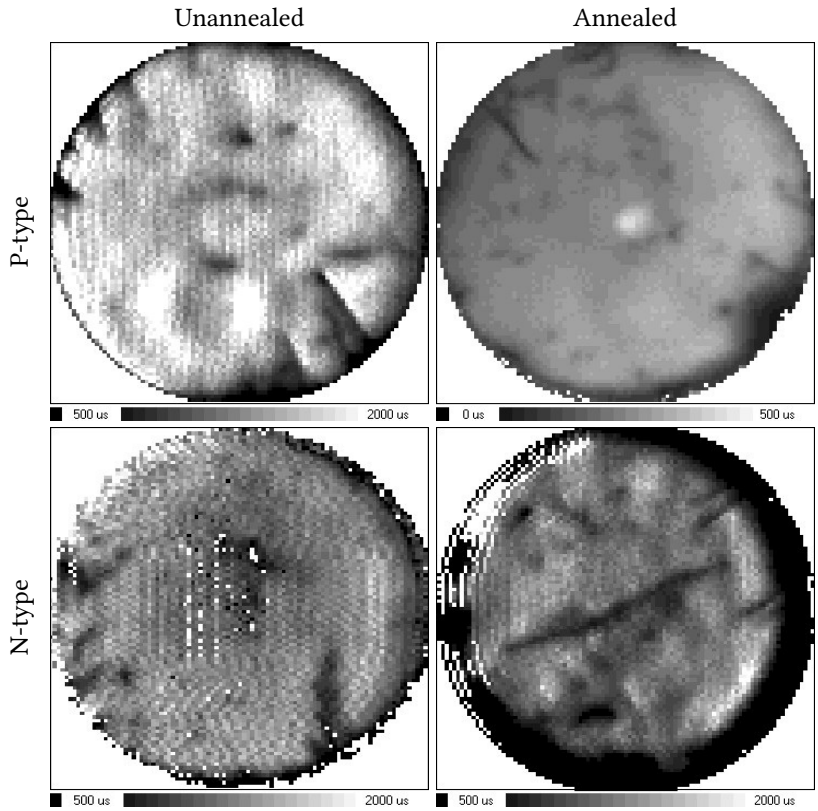

Figure III·10: μWPCD τ_{eff} mapping of reference and annealed, FZ (n) and (p) c-Si wafers, passivated with thick a-Si:H. All scales are 500-2000 μs, except for the annealed (p) wafer (0–500 μs) to enhance the contrast.

III·C·4 Preventing contaminants diffusion

To confirm if contaminants actually come from the SiC-coated graphite susceptor, a 500-nm-thick Si_3N_4 barrier was deposited by PECVD at 450℃ on two CZ wafers. One of them was annealed at 900℃ in the MOCVD chamber, then both were measured by QSSPC. Their minority carrier lifetimes are reported in Figure III·11. Both samples have high carrier lifetimes, close to 1 ms. The slight degradation of the annealed samples is most likely due to Si_3N_4/c-Si interface passivation loss during the thermal treatment. Hence, thick barriers on the wafers can prevent contaminating species from diffusing into the silicon bulk.

Another experiment was performed to determine whether the source of contamination is from the top or from the back side of the silicon wafer. In this case, a 500 nm Si_3N_4 barrier was deposited on FZ wafers on either front or back side of the wafer. A sample without barrier was also put in the third 100 mm imprint of the holder. After 900℃ annealing in the MOCVD chamber, Si_3N_4 was etched with HF, the first 10 µm of silicon were etched with KOH and wafers were finally cleaned and passivated with a-Si:H. Effective lifetime measurements at 1 sun are shown in Figure III·12. Si_3N_4 barrier could not prevent the bulk degradation: contamination comes from both the chamber atmosphere and the holder.

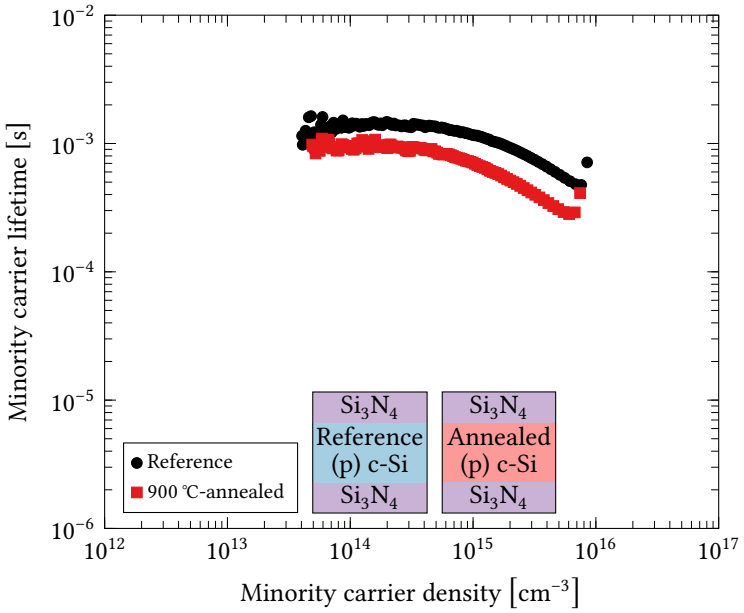

Figure III·11: QSSPC τ_{eff} of CZ wafers passivated with Si_3N_4 barrier on both sides [9].

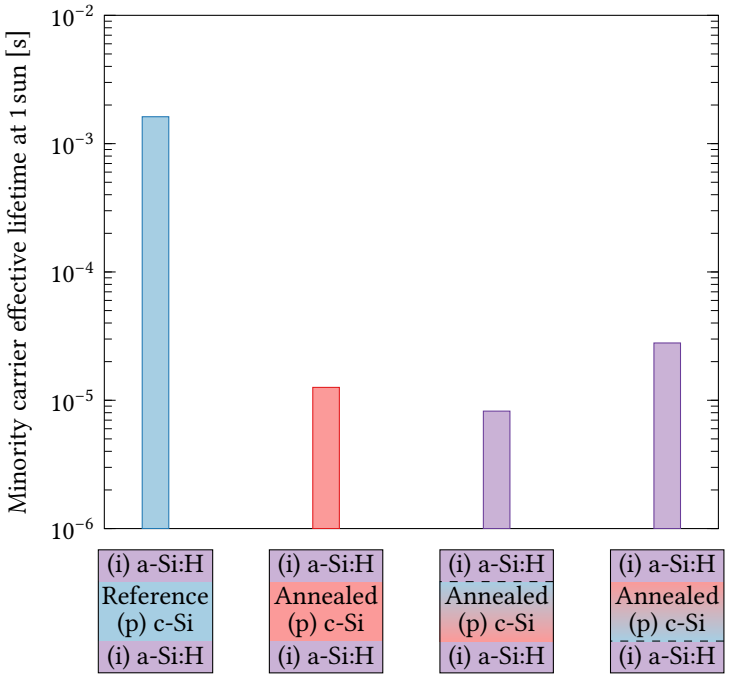

Figure III·12: Minority carrier lifetime at 1 sun of reference, and annealed wafers. Annealing was performed on samples without, and with front or back Si_3N_4 barriers that were subsequently removed.

III·C·5 Contaminants detection

III·C·5·a SIMS

SIMS enables the profiling of chemical composition of a silicon substrate (see § II·B·2·c). In order to identify contaminating species in the silicon bulk after annealing, we performed SIMS analyses on the wafers with or without the 900℃ annealing step (first two samples from the precedent experiment were used). Both samples were passivated with thick a-Si:H. In order to increase the contaminating species density close to the surface, a phosphorous diffusion step was performed on the annealed sample. This phosphorous diffusion is expected to drive the contaminating species in the highly doped region, as it will be explained in Chapter V (similar mechanism as the gettering process).

The following elements were monitored: B, P, Al, Zn, Ga, As, Se, In, Sb, F, Mg, S, and Fe. They were chosen as they are elements used for deposition and doping in the MOCVD chamber. Fluorine, magnesium, and sulphur were added as they are often present as surface contamination. The SIMS profiles are summarized in Figure III·13, with positive and negative ions detection. The peaks pointed at with arrows may be exaggerated by interferences. These interferences occur when the mass of simultaneously detected ions add up to the mass of another element of interest. Here, $_{18}O + _{1}H$ may be mixed up with $_{19}F$, $_{16}O + _{29}Si + _{30}Si$ with $_{75}As$, and $_{18}O + _{1}H$ with $_{19}F$.

The main difference between the two samples is the phosphorus diffusion profile clearly emerging in the annealed sample. One can identify the a-Si:H layer before the fluorine peak brought by HF deoxidation around 100 nm. However, all the other measured elements show parallel profiles inside the silicon substrate, meaning that either they are present in both samples, or their background noise is measured. This means that no clear contamination can be established through these SIMS measurements.

Other, more indirect, methods can be used to obtain more insight on the source of contaminants, such as Hall Effect and their behaviour under light.

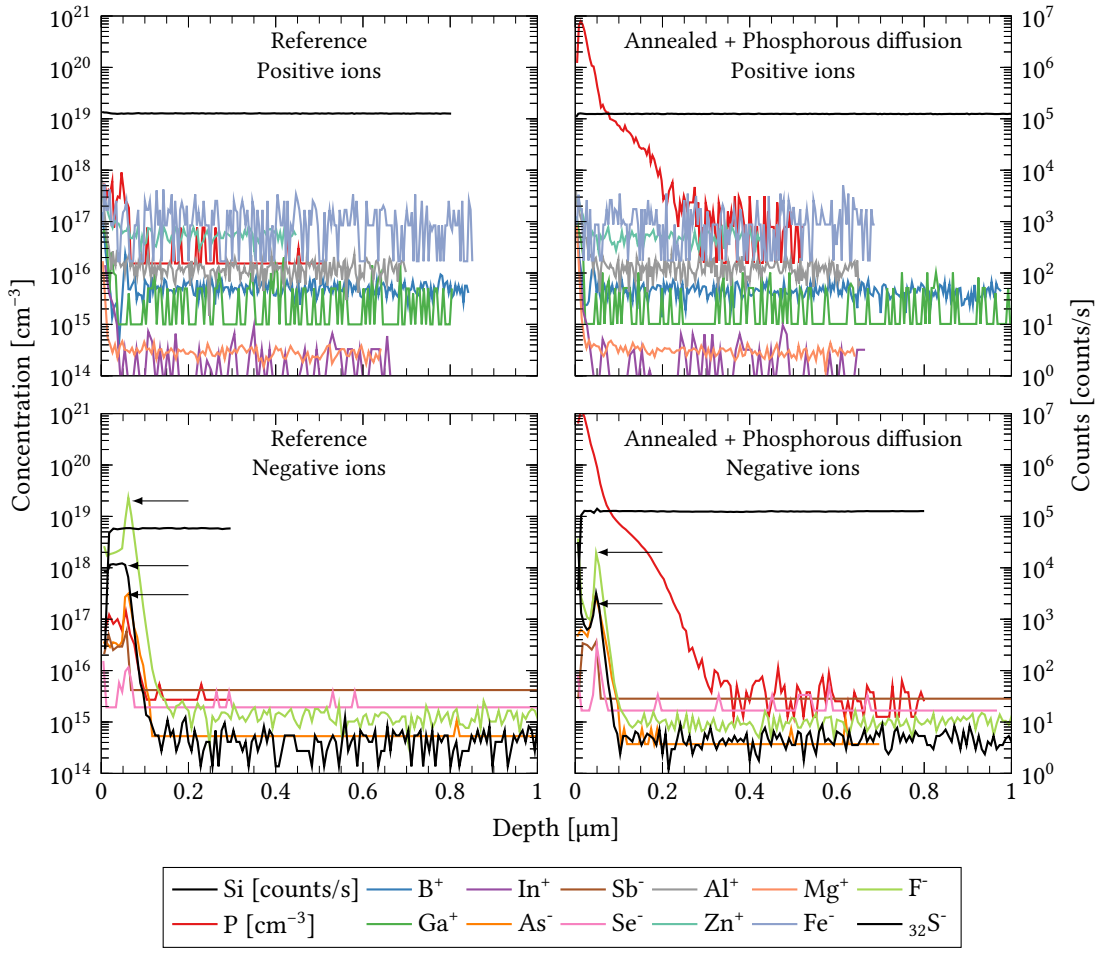

Figure III·13: SIMS profiles of a (left) reference, and (right) annealed and gettered solar cell precursors, obtained with (top) positive, and (bottom) negative ions. Silicon is given in counts per second (right axis), and all other elements in cm^{-3}.

III·C·5·b Hall Effect Spectroscopy

Hall effect spectroscopy (HES) consists in measuring carrier density at different temperatures to detect doping and contaminating atoms (see § II·B·3·b). From 4 K up to 573 K, fermi level moves away from the conduction band in (n)Si and away from the valence band in (p)Si, towards the middle of the bandgap. If the Fermi level reaches a doping level or a trap, its carriers are released. This release can be detected by derivation of the carrier density, which reveals peaks at specific temperatures, which can be converted into energy relatively to the closest energy band. Squared 1×1 cm samples were cut from CZ wafers for p-type measurement, and FZ wafers for n-type. Contacting was achieved with indium-gallium alloy deposited on the corners of the squares, and silver lacquer was added onto the contacts for high temperature measurements, above 300 K. In Figure III·14 we compare samples extracted from bare silicon wafers (Reference) and from wafers exposed to the 900℃ annealing process in the MOCVD chamber (Annealed).

One can notice two parallel peaks on each plots, which means that HES detected only two doping levels, both being common to reference and annealed wafers, which means that no contaminant was detected. The highest and sharpest peaks, referred as main peaks, are associated with the main dopants, boron in p-type and phosphorus in n-type samples. The peaks, characterized by their E_{peak} energy and H_{peak} height, are listed in the following table with the associated temperatures at which they were measured. E_{peak} is also reduced by $kT \cdot \ln g$ for $g = 2$ and $g = 4$ to estimate degenerated energy levels. Concentrations are estimated by multiplying by $((g + 1)^2/g)$ [88].

By comparing the energy levels measured and shifted by the degeneracy with the Figure I.8 from Sze [20], one can try to deduce the most likely dopants associated with the secondary peaks:

- In p-type samples, comparing only the energy levels, one can consider nickel (0.23 eV above the valence band), silicon (auto-interstitial, 0.19 eV), aluminum and beryllium (both 0.17 eV). Metallic contamination in CZ wafers at such concentrations and effective lifetimes is highly unlikely, so one may attribute this secondary peak to the auto-interstitials.
- In n-type samples, the closest energy levels are from nitrogen (0.19 eV below the conduction band) and lead (0.17 eV). Again, lead contamination is not realistic. Nitrogen incorporation in silicon is however well-known as it is used as inert atmosphere during FZ casting [99].

As a conclusion, energy levels probed by Hall Effect spectroscopy are most likely from their main dopants, auto-interstitials and nitrogen natively present in the substrates. Deeper and more recombinant traps could not be detected, as signal is lost due to intrinsic regime reached at higher temperatures. The similar spectra obtained on the reference sample and on the annealed sample indicate that the source of minority carrier lifetime degradation for the annealed sample cannot be detected by HES.

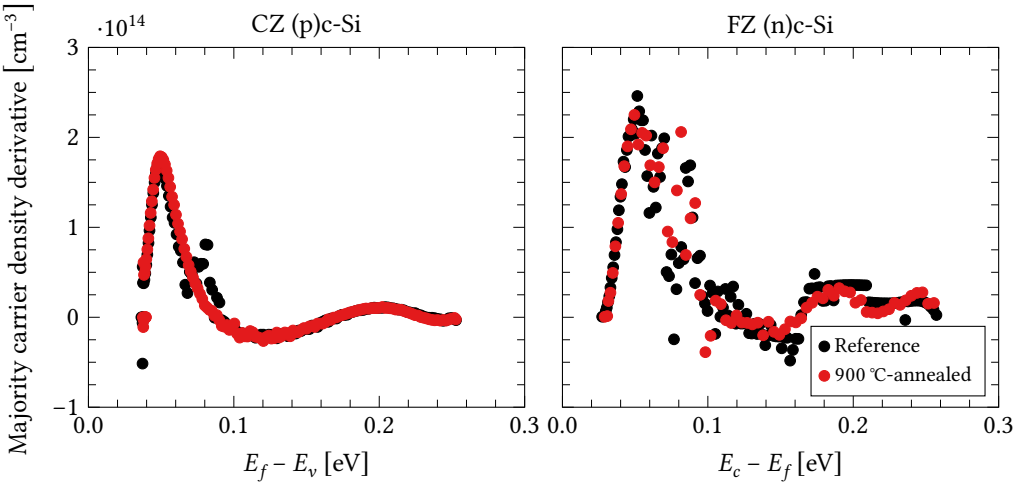

Figure III·14: Hall effect spectroscopy curves of (left) p-type, and (right) n-type reference and annealed precursors.

Table III·2: Summary of peaks detected by HES, and their analysis.

Sample	H_{peak}	T_{peak} [K]	E_{peak} [eV] E_{peak}-kT_{peak}ln(2) E_{peak}-kT_{peak}ln(4)	Closest dopants (E_{dopant} [eV]) [20]	Calculated concentration [cm^{-3}]
CZ P-type	$1.8 \cdot 10^{14}$	73	0.515	—	—
			0.471	—	—
			0.428	B (0.044)	$1.1 \cdot 10^{15}$
	$1.1 \cdot 10^{15}$	245	0.200	Ni (0.23)	$1.1 \cdot 10^{15}$
			0.185	Si_i (0.19)	$5.0 \cdot 10^{13}$
			0.171	Al, Be (0.17)	$6.9 \cdot 10^{13}$
FZ N-type	$2.3 \cdot 10^{14}$	67	0.495	—	—
			0.155	P (0.046)	$1.1 \cdot 10^{15}$
			0.415	—	—
	$3.2 \cdot 10^{15}$	230	0.190	N (0.19)	$3.2 \cdot 10^{13}$
			0.175	Pb (0.17)	$1.4 \cdot 10^{14}$
			0.163	—	—

III·C·6 Minority carrier lifetime evolution under illumination

A way to study the defects in bulk silicon is to monitor their behaviour under illumination. Upon light soaking, for example:

- Boron-oxygen defects tend to be exacerbated leading to lifetime decrease,
- Iron-boron bonds are broken, leading to effective lifetime increase.

III·C·6·a Lifetime vs time monitored by µWPCD

The µWPCD apparatus used in this study is equipped with a bias light that can be activated while lifetime is monitored. In figure Figure III·15, such measurement is presented for eight solar cell precursors: with or without GaP on front side, annealed or unannealed, p- or n-type FZ silicon. Without GaP, passivation is ensured with a thick intrinsic a-Si:H layer.

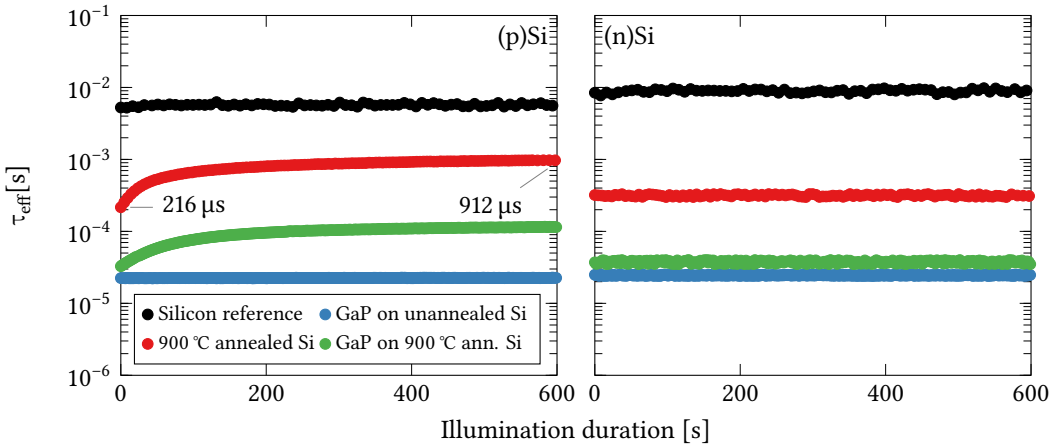

Figure III·15: µWPCD τ_{eff} vs time of different epitaxy conditions, on (left) p-type, and (right) n-type FZ wafers.

In the p-type unannealed precursors, effective lifetime remains constant under illumination, around 5 ms for the reference sample and 23 µs for the unannealed sample with GaP. In both annealed samples, with or without GaP, effective lifetime increases for ten minutes, then plateaus out below the reference level. This behaviour is not observed in n-type samples, where all lifetimes remain constant: reference precursors has carrier lifetime closer to 10 ms thanks to the better quality of (n)c-Si, while it is around 300 µs in annealed (n)c-Si. Samples with GaP, with or without annealing, have an effective minority carrier lifetime below 30 µs.

The fact that partial carrier lifetime recovery only occurs in annealed p-type silicon reveals some fundamental difference between trap formation in boron-doped and phosphorus-doped silicon that are exposed to contaminants coming from the MOCVD chamber:

- FZ wafers, with low oxygen concentration, in which carrier lifetime does not decreases under light in p-type silicon, reveal that no significant oxygen contamination occurs during the annealing.
- Lifetime only increases with boron in the silicon, which means that complexes between the contaminants and boron form, and that they can be dissociated upon carrier injection. This is typical of the presence of iron in the silicon, which will be described in the following section.

III·C·6·b Iron in boron-doped silicon

Interstitial iron (Fe_i) in silicon is positively charged, while substitutional, doping, boron (B_s) is negatively charged. Coulomb interaction leads to the formation of Fe-B bonds which can be broken under illumination, as carrier generation lifts the pseudo Fermi level and brings electrons above the energy level of Fe_i, breaking the FeB bond [100–102]:

$$(Fe_i)^+ + (B_s)^- \rightleftharpoons (Fe_iB_s)^0 \tag{III·1}$$

Table III·3 summarizes the properties of the traps, Fei and the two energy levels of FeB. Fei and FeB- have temperature-corrected cross-sections from the work of Paudyal *et al.* [103], while the cross section of FeB^+ has the calculated value by MacDonald *et al.* at room temperature [102]. The resulting error is considered negligible.

Table III·3: Energy level and capture cross-sections of Fei and FeB traps.

	Fe_i^+	FeB^-	FeB^+
E_{trap} [eV]	E_v+0.39	E_c-0.27	E_v+0.39
σ_p [cm^{-2}]	$6.5 \cdot 10^{-17}$	$1.2 \cdot 10^{-15}$	$3 \cdot 10^{-13}$
σ_n [cm^{-2}]	$7.6 \cdot 10^{-15}$	$3.3 \cdot 10^{-15}$	$3 \cdot 10^{-15}$
References	[103]		[102]

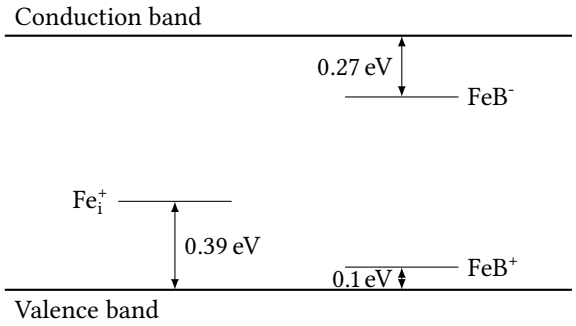

Figure III·16: Energy band diagram representing Fei and FeB traps in silicon. [103]

Both iron states have quite different recombination properties, which leads to different lifetime behaviour depending on the wafer doping and carrier injection, illustrated in Figure III·17. At

low injection level, FeB are majority traps while at high injection level, after dissociation, Fei traps are more common. As lifetime limited by FeB (τ_{FeB}) at low injection is lower than lifetime limited by Fe_i (τ_{Fe_i}) at higher injection, measured lifetime during light soaking increases.

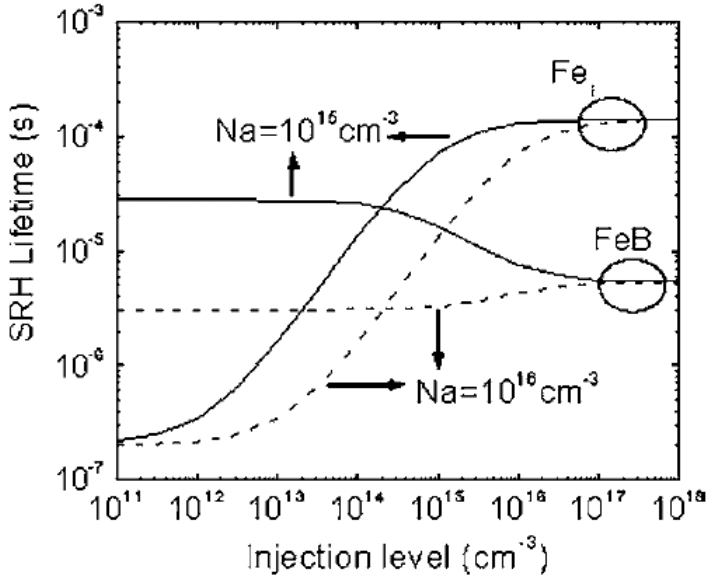

Figure III·17: Limiting lifetime linked to Fe_i and FeB traps vs injection level, for two wafer doping conditions. [104]

In conclusion, in phosphorus-doped silicon, there is no FeB and lifetime is limited by Fe_i and remains constant under illumination. Partial lifetime recovery in boron-doped silicon under illumination is typical of iron-boron bonds being dissociated.

III·C·6·c Lifetime vs time measured by QSSPC

Figure III·17 hints at lifetime specificity of Fe_i and FeB traps: in iron-contaminated silicon, there is a crossover injection level point Δn_{COP} where τ_{Fe_i} and τ_{FeB} are equal. Δn_{COP} can be divided into a doping-dependent (DD) and a temperature-dependent (TD) term [103]:

$$\Delta n_{COP} = \underbrace{\frac{\sigma_n^{-1}(FeB) - \sigma_n^{-1}(Fe_i)}{\sigma_p^{-1}(Fe_i)} p_0}_{\Delta n_{COP,DD}} + \underbrace{\frac{\sigma_p(Fe_i)}{\sigma_p(FeB)} N_c(T) \exp\left(-\frac{E_c - E_{FeB}}{kT}\right)}_{\Delta n_{COP,TD}} \qquad \text{(III·2)}$$

Figure III·18 confirms such crossover point, located around $7 \cdot 10^{12}$ cm^{-3}. However, the computation of $\Delta n_{COP}(DD, 298\,\text{K})$ shows that it cannot be lower than $7 \cdot 10^{13}$ cm^{-3} under typical doping levels, as shown in Figure III·18. This significant discrepancy, with the actual Δn_{COP} being one order of magnitude lower than the minimum possible may be due to other recombination centres than FeB, which either have the similar dissociation behaviour upon light soaking, or interfere with it.

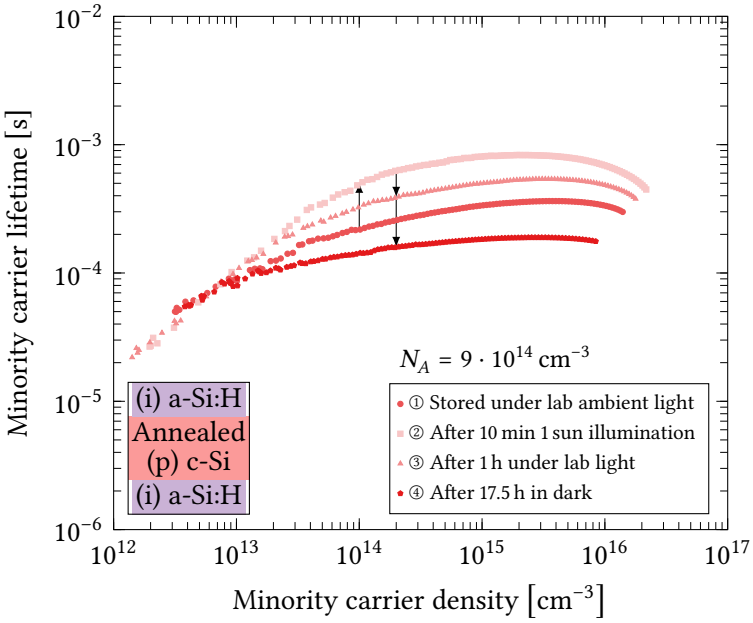

Figure III·18: QSSPC τ_{eff} measurement, under different FeB dissociation state.

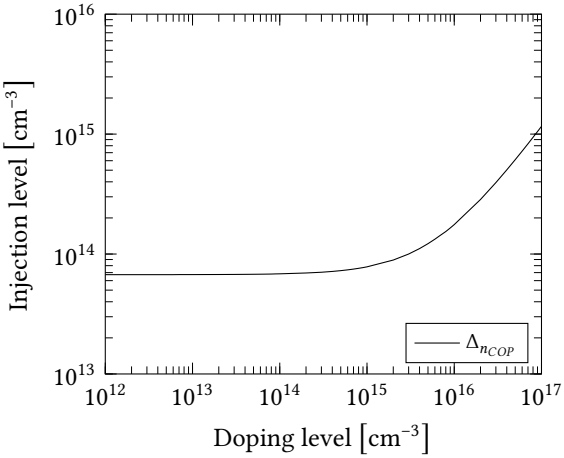

Figure III·19: Δn_{COP} vs doping level at 298 K.

III·C·6·d Effect of trap dissociation on IQE

Considering that lifetime is partially recovered upon Fe-B dissociation, one may wonder what its effect is on the IQE of solar cell, as the infrared collection rate degradation is directly linked to bulk lifetime. To estimate this effect, the three P-type solar cells from § III·A (SHJ reference, SHJ with annealed silicon, GaP on annealed silicon) were illuminated by the solar simulator. As seen in Figure III·18, 10 min are enough to dissociate the FeB bonds. IQE measurements were performed less than thirty minutes after stopping the illumination, which is below the association time constant τ_{asso} of Fe-B bonds. Indeed, MacDonald for 3 Ω·cm FZ wafers, τ_{asso} > 80 min [105]. Thus, the amount of rebounded FeB pairs should be minimal when the IQE measurement is started, and bulk lifetime should only be limited by interstitial iron.

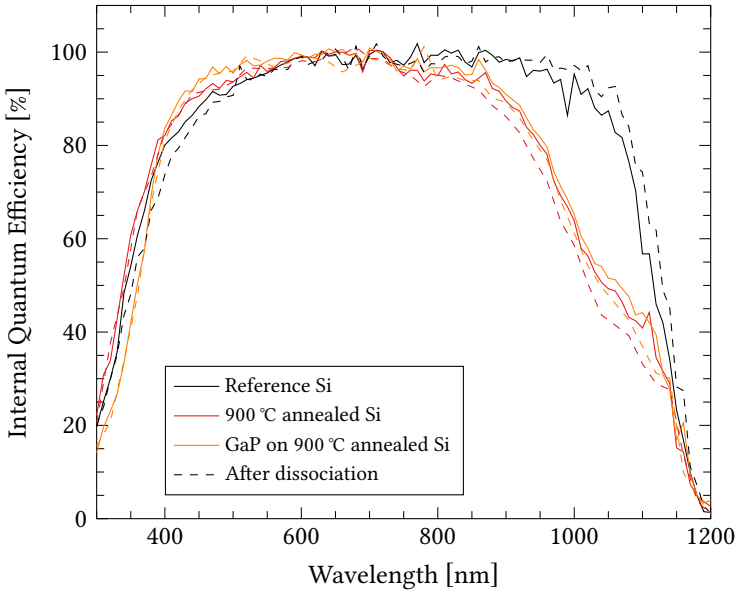

Figure III·20: IQE spectra of solar cells before and after FeB dissociation.

In Figure III·20, IQE spectra are presented before and after 10 min illumination under the solar simulator No improvement of the infrared collection efficiency is observed: even though lifetime can noticeably improve upon trap dissociation, undissociated traps or other contaminants still limit the efficiency of the solar cells.

III·C·7 Contaminants quantification

The techniques used above could not directly detect contaminating species in the silicon. SIMS and HES were rather inconclusive. SIMS detected no III-V or metallic contaminants in annealed samples, and HES detected the same doping elements in reference and annealed samples: P, B, Si_i, N, which cannot explain such drastic minority carrier lifetime loss. μWPCD and QSSPC,

however, revealed an iron-boron trap behaviour under illumination, which needs to be quantified. To do so, we will calculate the iron concentration from the carrier lifetime recovery induced by the FeB dissociation, and simulate the effect of iron on the IQE degradation in the infrared end of the solar spectrum.

III·C·7·a Iron concentration calculation from carrier lifetimes limited by recombination through iron levels

Based on the recombination properties of Fe_i and FeB traps, Zoth and Bergholz determined that iron concentration is linked to the measured lifetimes before and after dissociation [106]. If iron-related defects are the main lifetime-limiting defects, this method has a sensitivity in the order of $1 \cdot 10^{11}\,cm^{-3}$ and accuracy of 20% [106]. The iron concentration can be calculated as follow:

$$N_{Fe} = C_{Fe}\left(\frac{1}{\tau_{Fe_i}} - \frac{1}{\tau_{FeB}}\right) \tag{III·3}$$

where N_{Fe} is the iron concentration [cm^{-3}],
C_{Fe} is the conversion coefficient [cm^{-3}·s],
τ_{FeB} is the minority carrier lifetime before dissociation [s],
τ_{Fe_i} the minority carrier lifetime after dissociation [s].

The coefficient C_{Fe} can be calculated from the SRH model of Fe_i and FeB traps:

$$\frac{1}{\tau_{trap}} = \frac{N_A + \Delta n}{\tau_{p0}\cdot(n_1 + \Delta n) + \tau_{n0}\cdot(N_A + p_1 + \Delta n)} \tag{III·4}$$

where $\tau_{n0} = (N_{trap} v_n^{th} \sigma_n)^{-1}$, $\tau_{p0} = (N_{trap} v_p^{th} \sigma_p)^{-1}$ are the low-injection lifetimes for electrons and holes,
$v_n^{th} = 2.05 \cdot 10^7\,cm{\cdot}s^{-1}$, $v_p^{th} = 1.69 \cdot 10^7\,cm{\cdot}s^{-1}$, are the thermal velocity of electrons and holes at 300 K [10],
N_{trap} is the trap concentration, either N_{FeB} or N_Fe_i,
$n_1 = N_c \cdot \exp\left(-\frac{(E_c - E_{trap})}{kT}\right)$ is the electron density at the trap level,
$p_1 = N_c \cdot \exp\left(-\frac{(E_{trap} - E_v)}{kT}\right)$ is the hole density at the trap level,

Thus, Equation III·4 can be simplified into Equation III·5

$$\frac{1}{\tau_{trap}} = N_{trap} \cdot \frac{N_A + \Delta n}{\left(\frac{n_1 + \Delta n}{v_{th}^p \cdot \sigma_p}\right) + \left(\frac{N_A + p_1 + \Delta n}{v_{th}^n \cdot \sigma_n}\right)} \tag{III·5}$$

After calculation for each trap, with the parameters from Table III·3:

$$C_{Fe} = -1.12 \cdot 10^8\,cm^{-3}{\cdot}s \tag{III·6}$$

In Figure III·15, the effective lifetimes measured initially and after dissociation in a 900℃ annealed wafer were respectively 216 and 912 µs:

$$N_{Fe}^{\mu WPCD} = (3.9 \pm 0.2) \cdot 10^{11} \mathrm{cm}^{-3}$$

This calculated iron concentration is within sensitivity range allowed by the method, and may explain why iron remained below SIMS detection limits even after phosphorus diffusion. Indeed, let us consider that:

- Each annealing step brings the same number of iron atoms in the silicon substrates, which may most likely not be true, as seen by non-reproducibility of the degradation;
- Iron diffusion is fast enough that its concentration is homogeneous across the wafers;
- Phosphorus diffusion used for the SIMS analysis is efficient enough to bring all the iron atoms in its 400-nm-deep profile.

With these hypotheses, the $3.9 \cdot 10^{11}$ cm^{-3} iron atoms in 280-µm-thick silicon would give $2.7 \cdot 10^{14}$ cm^{-3} if concentrated in a 400-nm-deep phosphorus-rich layer. This concentration is below the ppm detection limit of SIMS, $1 \cdot 10^{16}$–$1 \cdot 10^{17}$ cm^{-3}, and would require 100–1000 times more iron atoms to be detectable with phosphorus diffusion in 280-µm-thick wafers. Hence, if iron is the contaminating species, its concentration in the 900℃-annealed FZ wafer measured here is in the order of 10^{11} cm^{-3}, which is low enough not to be detectable by SIMS, and high enough to severely limit the minority carrier lifetime.

III·C·7·b Iron concentration estimation through IQE simulation

AFORS-HET software was used to simulate the degraded IQE in infrared under different iron concentrations. To achieve so, Fei, FeB+ and FeB- traps were added to the bulk silicon model presented in Table II·5, with single energy levels and capture cross-sections presented in Table III·3. Iron concentration is split between Fei (0.01%) and FeB (99.99%), to emulate the effect of undissociated FeB traps. Results are shown in Figure III·21, with experimental data from the 900℃ annealed wafer made into solar cell presented in Figure III·4. Simulated curves do not perfectly fit the measured one, but if one considers only iron contamination, its concentration is between 10^{11} and $5 \cdot 10^{12}$ cm^{-3}, which is one order of magnitude larger than the iron concentration determined by µWPCD.

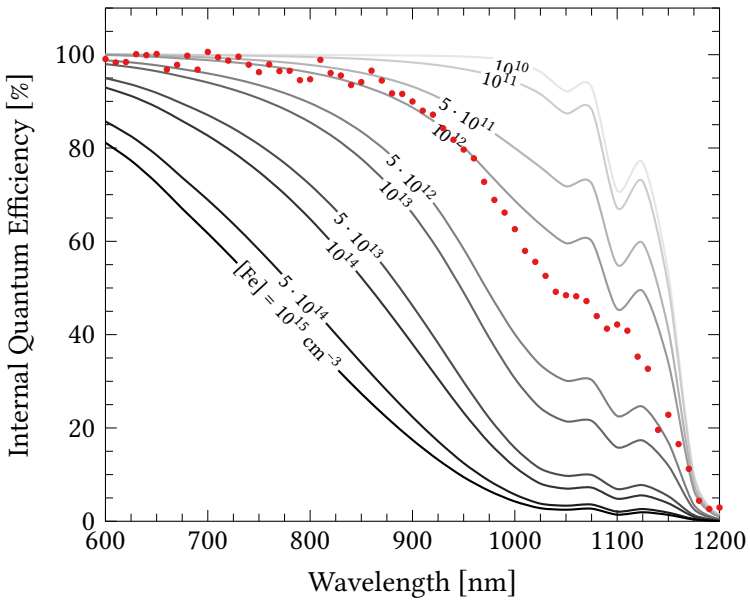

Figure III·21: Simulated IQE with varying iron content in substrate, and measured solar cell with annealed substrate.

III·C·7·c Discussion on iron concentration determination

There are discrepancies between calculations of iron concentration resulting from the lifetime recovery upon light soaking, and from simulation of IQE curves. Moreover, the cross-over point emerging in the lifetime-injection curves upon light soaking is an order lower than what the theory allows.

Diffusion barriers have shown the degradation to come from both the front and back sides. Ohlmann *et al.* [73] performed similar studies on annealed samples, where they demonstrated that iron coming from the SiC holder is the main contributor to carrier lifetime degradation in their MOCVD cluster. They estimated iron contamination to $1.2 \cdot 10^{12}\,\mathrm{cm}^{-3}$ after 30-min 1050℃-annealing, which is about ten times higher than what we estimated, with longer and hotter annealing.

These differences between calculations, simulations and theory in our study leave the possibility for the bulk degradation upon annealing to come from other contaminants, and combinations of them.

III·D Interface passivation

Effective carrier lifetime is function of bulk and surface recombinations. In previous part, we mostly investigated the degradation of bulk lifetime due to the surface reconstruction anneal-

ing. However, the analysis performed in § III·B·1 showed that the interface between GaP/Si, without annealing, is also limiting the carrier lifetime. Let us recall the conclusions of the experiment from § III·B·1: bulk lifetime is only degraded by the high-temperature surface reconstruction annealing, not by the epitaxy of GaP itself. This means that effective lifetime of a GaP on unannealed silicon precursor, passivated with a-Si:H on the back side, is only limited by the GaP/Si interface. This interface can be described by its surface recombination velocity S. Sproul [107] proposed a numerical model for the determination of S and τ_s:

$$\frac{1}{\tau_s} = \alpha^2 \cdot D_n \tan(\alpha \cdot t) = \frac{S_{front} + S_{back}}{\alpha \cdot D_n - \frac{(S_{front} \cdot S_{back}}{\alpha \cdot D_n}} \tag{III·7}$$

where α is the smallest eigenvalue solution,
$t = 0.078\,\text{cm}$ is the thickness of the wafer,
$D = 12\,\text{cm}^2\cdot\text{s}^{-1}$ is the diffusivity of minority carriers, calculated from the measured resistivity of the reference wafer, 19.8 Ω·cm,
S_{front} and S_{back} are respectively the front and back surface recombinations velocities.

Luke and Cheng [108] simplified the general equation when $S_{front} = S_{back} = S$, as long as the transient effective lifetime $\tau_{eff} >> \frac{W^2}{(\pi^2 \cdot D_n)} = 51.4\,\mu\text{s}$:

$$\tau_s = \frac{W}{2S} + \frac{1}{D_n}\left(\frac{W}{\pi}\right)^2 \tag{III·8}$$

To estimate the surface recombination velocities at the interfaces with the silicon bulk, effective minority carrier lifetimes were measured after passivation, with GaP and a-Si:H, on unannealed CZ wafers. The curves are plotted on Figure III·22.

III·D·1 Determination of $S_{a\text{-}Si:H}$

The reference wafer, symmetrically passivated with a-Si:H, has $\tau_{eff}^{a-Si:H} = 4.36\,\text{ms}$ effective lifetime. Equation III·8 is thus applicable, and gives:

$$S_{a-Si:H} = 9.05\,\text{cm}\cdot\text{s}^{-1}$$

III·D·2 Determination of S_{GaP} and S_{ox}

From Figure III·22, effective lifetime at 1 sun of the wafer passivated only on the back side – *i.e.* limited by its native oxide layer on front side – is $\tau_{eff}^{ox} = 52.1\,\mu\text{s}$, while the one with GaP on the front side is $\tau_{eff}^{GaP} = 47.8\,\mu\text{s}$. This means the GaP does not achieve better passivation than the native oxide formed on c-Si when exposed to the air. Luke and Cheng also proposed a simplification when one surface is highly recombinant compared to the other, which is the case here, as $\tau_{eff}^{GaP}, \tau_{eff}^{ox} \ll \tau_{eff}^{a-Si:H}$. However, these lifetimes were measured by QSSPC, and the

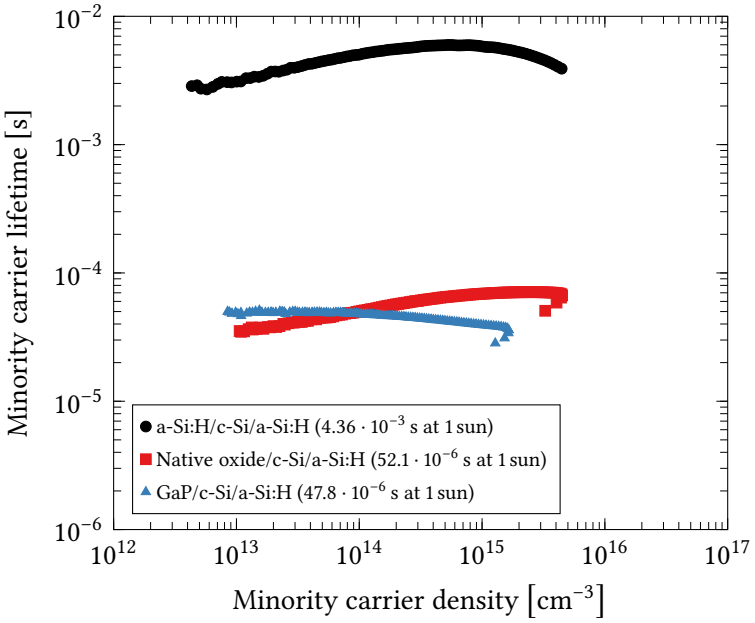

Figure III·22: QSSPC τ_{eff} of unannealed silicon wafers with (i) a-Si:H back side passivation, and either GaP, (i) a-Si:H or no passivation on the front side. Lifetimes at injection level equivalent to 1 sun are also reported.

simplification under this mode applies only if $\tau_{eff} \gg \frac{W^2}{12D} = 42.3\,\mu s$. The general equation was thus solved with the $S_{back} = S_{a\text{-}Si:H}$ calculated above, to find:

$$S_{ox} = 9.12 \cdot 10^3 \text{ cm·s}^{-1}$$

$$S_{GaP} = 9.31 \cdot 10^3 \text{ cm·s}^{-1}$$

III·D·3 Discussion on the surface recombination velocity

Considering that the effective carrier lifetime in unannealed solar cells precursors is only limited by the passivation of their surfaces, the surface recombination velocity of GaP/c-Si was determined to be one thousand times higher than the one of a-Si:H/c-Si interface.

It was also determined that GaP does not achieve better passivation than a native oxide, which casts doubt on the efficacy of the field effect passivation that was evoked in the introduction. One may consider that the density of defects or contaminants at the GaP/Si interface is high, and high enough that the field effect is counterbalanced.

It must be noticed that no wafer pre-annealing was performed here in order to avoid bulk degradation. However, it is known that such a treatment is necessary to grow high quality III-V materials on silicon [109]. Therefore, these results are not unexpected. Nonetheless, the results

shown in Figure III·5 highlighted that even for the GaP grown after surface pre-treatments, the surface passivation was not as good as the once obtained without annealing, or the native oxide. We will address this point in Chapter IV when the GaP growth conditions are optimized to minimize interface traps. The results presented in this section show that with our experimental conditions, the surface passivation by GaP is not sufficient to build high efficiency solar cells.

III·E Conclusion on the minority carrier lifetime degradation

The minority carrier lifetime degradation has been linked to two phenomena: silicon bulk degradation during the surface preparation annealing before epitaxy, and poor surface passivation.

Bulk degradation is deep, as it cannot be improved by removing the first micrometres of the silicon substrate. SIMS profiles did not reveal any particular contaminants. Minority carrier lifetime displays typical reversible Fe-B bonds dissociation under illumination, as it increases during such treatment. However, calculation and simulation of the effect of iron concentration on the IQE is inconsistent, and the injection crossover point determined by QSSPC is lower than the minimum allowed by the theory. We shall conclude that even if iron contamination may be involved, other defects are more likely present, but at concentration levels low enough not to be detected by SIMS. Chapter V will investigate the integration of contamination removal steps to make solar cells with improved bulk lifetimes.

The high recombination velocity at the interface between c-Si and GaP is due to defects such as remaining dangling bonds after epitaxy, or contaminants. Analysis of the minority carrier lifetimes reached by difference passivation layers determined that surface recombination velocity for GaP on un-annealed c-Si is a thousand times higher than a-Si:H, hindering the field effect passivation. For GaP on annealed Si, it is not possible to estimate the recombination velocity, but experiments have shown that the passivation remains too low to envision high efficiency solar cells fabrication. Chapter IV will be dedicated to the optimization of the GaP/Si interface.

IV GaP/Si interface passivation

In addition to the bulk lifetime degradation induced by the surface preparation annealing in the MOCVD chamber, it was shown that GaP/Si interface lifetime was not passivating either, when epitaxy is performed without the annealing (§III.B.1). Low interface lifetime can be due to crystalline defects emerging from non-optimised epitaxy, which can be associated with charge defects.

Microelectronics relies on the epitaxied layer thickness to let the defects grow enough to be either captured by aspect ratio trapping [110–112] or to be self-annihilated by crossing each other [63]. This is acceptable, as microelectronic devices do not use the whole bulk of the materials: the contaminants and defects can be "buried" far from the surfaces and the subsequent layers. However, in photovoltaics, the performances of the devices depend on the quality of the entire stack of materials: if defects and contaminants are buried, they contribute to the recombinations that limit efficiencies.

In this chapter, we will investigate the possibility to perform the surface reconstruction annealing in other chambers, in the hope to preserve bulk silicon minority carrier lifetime. We will also determine the influence of crystal defects at the GaP/Si and GaP itself thanks to high quality GaP/Si templates. The presence of contaminants in these layers, and in our own, will be investigated by XPS. Finally, different wetting layers, to change interface chemistry and limit interface recombinations will be investigated.

IV·A Surface reconstruction annealing in non-contaminating chambers

As the high temperature processes (> 650°C) in the III-V MOCVD chamber degrade the minority carrier lifetime, three other annealing chambers were investigated:

- Levitor 4300, a Rapid Thermal Processing (RTP) system, uses hot plates that are set at 900°C before being brought as close as 100 µm from the wafer, in a helium environment;
- ASM VT412, another RTP system, with another design which involves a longer heating ramp with sample in the chamber to reach 900°C, in nitrogen atmosphere below 750°C, then argon to prevent silicon nitration at higher temperatures;
- ASM EPSILON 3200, a silicon-germanium MOCVD system, with similar thermal processing capabilities as the III-V MOCVD.

IV·A·1 Annealing in RTP systems

The temperature profiles the RTP systems provide are shown in the left-hand part of Figure IV·2. RTP were performed on (100) CZ wafers, and the resulting minority carrier lifetimes after a-Si:H passivation is reported in the right-hand side of the figure. While annealing in the Levitor degrades the lifetime (which remains close to 1 ms), the VT412 annealing affects only marginally the substrates minority carrier lifetimes. For comparison, a process with a similar temperature profile as the one of the VT412 was performed in the III-V MOCVD chamber, which resulted in even lower effective minority carrier lifetime.

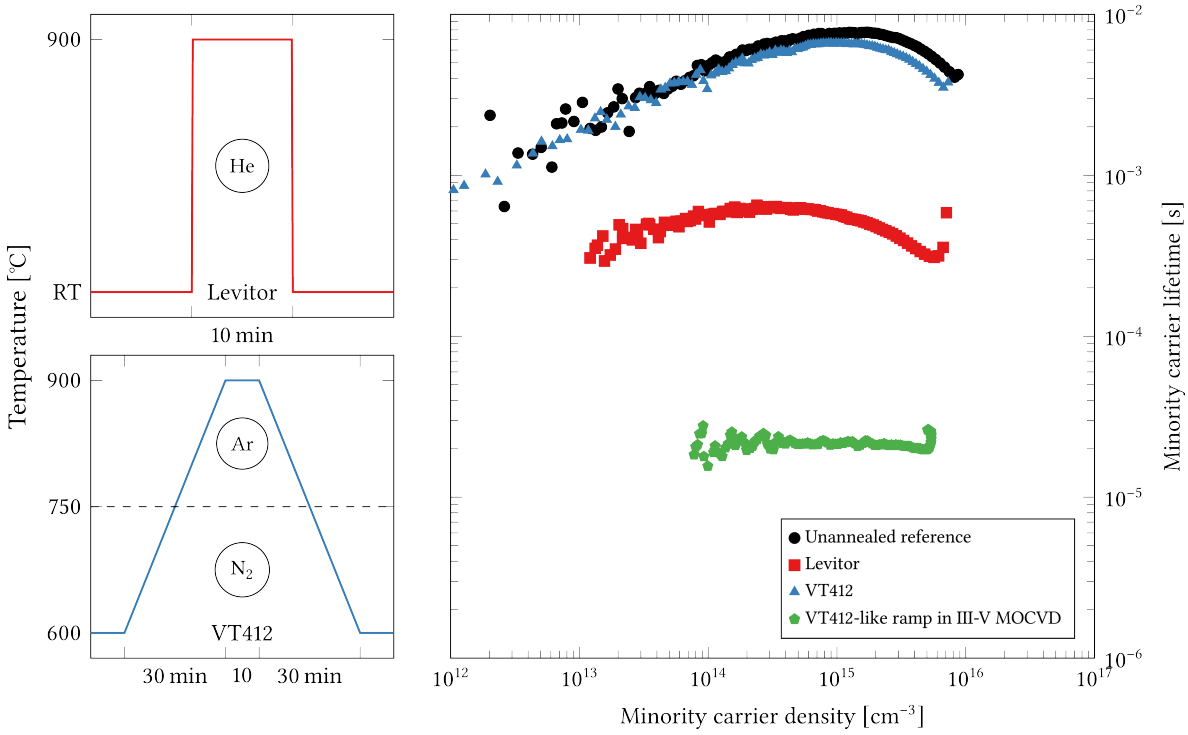

Figure IV·1: (left) Temperature profiles and ambient gases in the Levitor and VT412 RTP systems for 900℃ annealing (right) QSSPC curves of reference and annealed samples, passivated with a-SiH.

This experiment shows that silicon wafers used here can sustain high temperature processes without severe minority carrier lifetime degradation. Therefore, the bulk degradation is attributed to extrinsic species coming from the process chamber rather than intrinsic defects revealed by the high temperature process. However, technical constraints prevented us from using the VT412 system for surface reconstruction before GaP growth in the MOCVD chamber.

IV·A·2 Annealing in SiGe-MOCVD system

We investigate here a 10-min-long, 900℃ annealing on (100) CZ wafers in the SiGe-MOCVD system with H_2 carrier gas. To estimate the effect of the reconstruction on the GaP epitaxy, one wafer was also transferred to the III-V MOCVD cluster, then etched by the Siconi process and 10 nm GaP was grown on the front side. All other surfaces were passivated with a-Si:H.

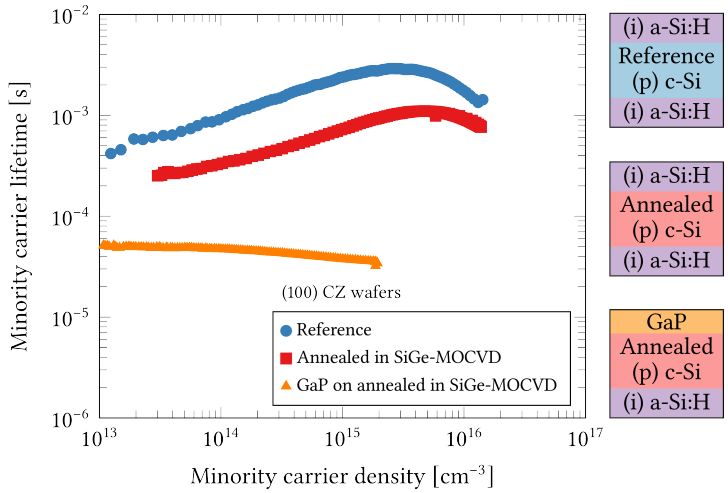

Figure IV·2: QSSPC τ_{eff} of samples annealed in the SiGe-MOCVD chamber.

The subsequent effective minority carrier lifetimes are plotted in Figure IV.2. After annealing in the SiGe-MOCVD chamber, bulk lifetime is slightly degraded, but remains acceptably close to 1 ms. However, surface reconstruction on this relatively high-lifetime substrate is still not enough to obtain good passivation by the GaP, as GaP/Si interface lifetime is below 100 µs. This experiment demonstrates that the process we use for GaP growth is unable to provide good enough interface to provide a surface passivation, even if the silicon surface was thermally annealed before the GaP growth step.

IV·A·3 Surface reconstruction on 4°-offcut wafers

The formation of diatomic steps on the surface of annealed silicon can be enhanced by the use of silicon substrates offcut in the [110] direction. Surface reconstruction annealing on 4°-offcut substrates has been shown to completely prevent the formation of APDs in GaAs [113–115]. Such improvements were also obtained with GaP epitaxial layers [115]. These wafers are however non-compatible with industrial standards, which rely on nominal (100) wafers [109]. Here, 4°-offcut wafers were annealed in either III-V or SiGe-MOCVD systems. GaP/Si samples were also prepared after these annealings, and all other surfaces were passivated with a-Si:H.

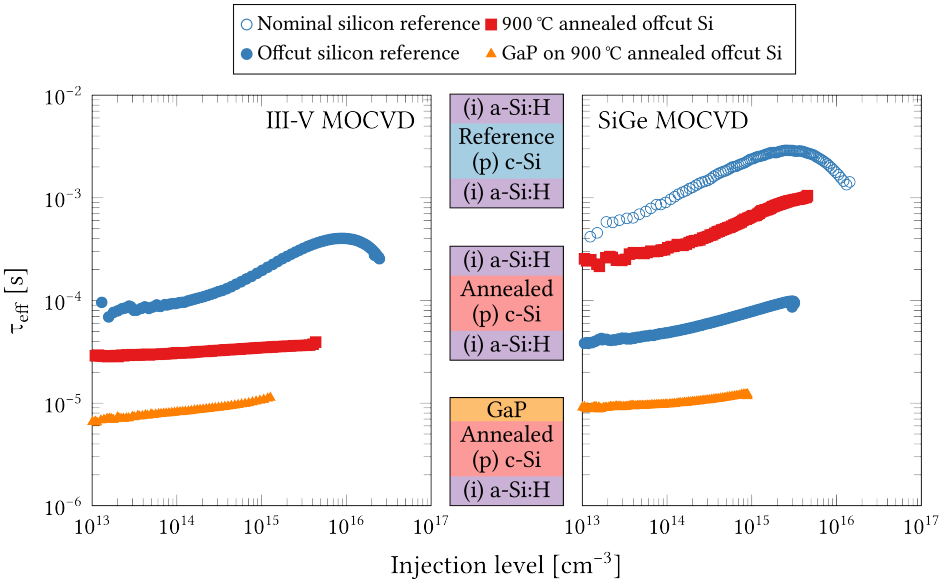

Figure IV·3: QSSPC τ_{eff} of 4°-offcut samples annealed in (left) the III-V MOCVD (right) the SiGe-MOCVD.

QSSPC-measured effective minority carrier lifetimes are plotted in Figure IV·3. First, we discover that unannealed 4°-offcut wafers have intrinsic lifetime below 500 µs, which is far lower than reference (100) wafers which are above 1 ms. Annealing on miscut wafers in III-V MOCVD resulted in the same lifetime degradation as already studied in Chapter III, due to contaminating species, and worsened by the GaP/Si interface. However, miscut bulk lifetime is partially restored in the SiGe-MOCVD chamber, and reaches the same level as the annealed (100) reference, presented in the previous section. This recovery of CZ bulk lifetime after annealing may be due to complexes dissolution or traps passivation favoured by the high temperature of the annealing. The recovered lifetime is at the same level as the (100) reference, as it is limited by the slight degradation uncovered in the previous section. Finally, being around 10 µs, effective minority carrier lifetime with GaP is still the worst: there is no improvement of interface lifetime if GaP is grown on 4°-offcut substrates.

IV·A·4 Conclusion on surface reconstruction annealing in non-contaminating chambers

We successfully performed non-lifetime-degrading annealing in a VT412 system and, with a slight and acceptable degradation, in a MOCVD chamber dedicated to silicon and germanium epitaxy. These annealing steps preserve bulk lifetime above 1 ms, but effective lifetime was systematically limited by the introduction of the GaP/Si interface. Even with as good as possible surface reconstruction conditions, the GaP layer grown in the MOCVD chamber has therefore an interface quality that is not good enough for high efficiency solar cells fabrication.

IV·B GaP/Si template precursors

So as to investigate effective minority carrier lifetimes achievable thanks to GaP without defects, GaP/Si templates were ordered from NAsPIII/V GmbH, a startup specialised in MOCVD epitaxy of III-V materials [55, 116–118]. These 10 nm GaP/Si templates were obtained through an ALE process, optimized to obtain little-to-no crystalline defects (dislocations as well as antiphase boundaries). After HF dip and a-Si:H passivation for lifetime measurement, the root mean square (RMS) of the roughness of the samples, R_q, was measured by AFM.

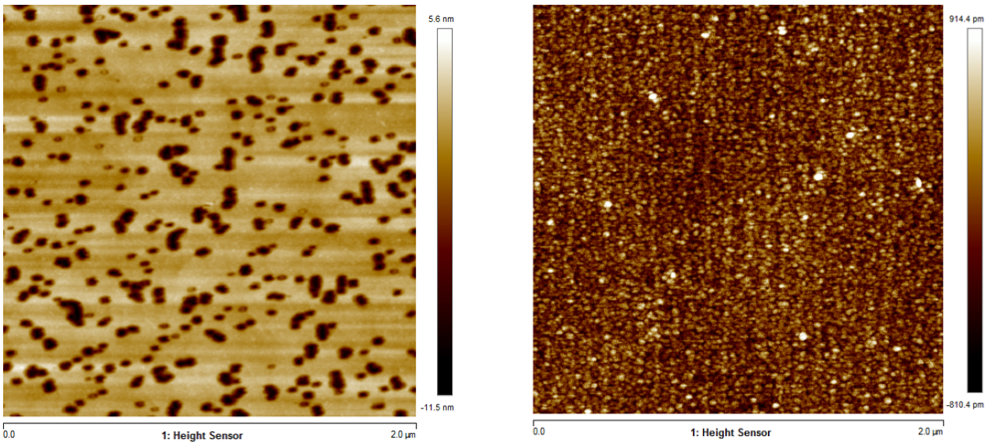

Figure IV·4: AFM pictures of the GaP layer of GaP/Si template samples from NAsP after HF deoxidation and a-Si:H deposition on the back side. Left picture is from initial template, with $Rq = 0.252$ nm between the holes. Right picture is from second template with $Rq = 0.246$ nm.

Figure IV·4 shows the AFM pictures of two GaP/Si templates. The first one, on the left, was provided first. It displays numerous holes, as deep as the GaP, that were etched by the HF-Last process required for (i) a-Si:H passivation. Such sensitivity to HF is not expected as initial HF-etching tests performed on our own GaP/Si samples showed very slow etching rates (see § II·A·7·c·i). GaP etching may be exacerbated by post-annealing phosphorus treatment that enhances layer quality by weakening the bonds around the defects [119]. Between the holes, roughness is low, at $Rq = 0.25$ nm.

A second GaP/Si template was ordered to NAsP, which resisted the HF etching and had the same roughness (right-hand of Figure IV·4). The change of scale enables us to see small clusters on the surface of GaP, indicating 3D growth rather than 2D growth, despite the ALE process. One can also notice the underlying surface reconstruction, with the parallel lines delimiting monodomains between biatomic steps. Effective lifetimes, reported in Figure IV·5, show that they are the best encountered so far, at 143 µs, but still too low to obtain high efficiency solar cells.

After GaP removal and repassivation, lifetime is restored up to close to 2 ms, as shown on the right-hand of Figure IV.5. This means that surface reconstruction was performed in non-degrading annealing chamber and that the low minority carrier lifetime can be attributed to the low passivation at the GaP/Si interface

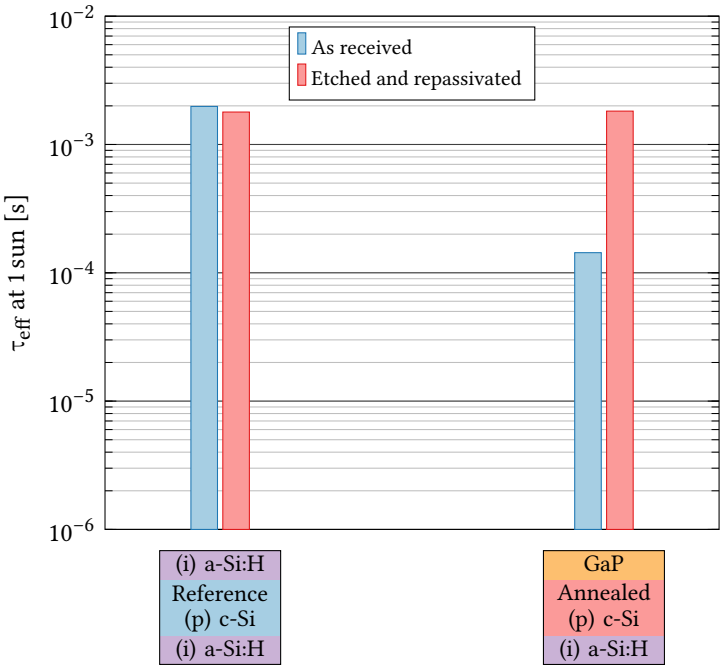

Figure IV·5: QSSPC τ_{eff} at 1 sun, and after etching of all deposited layers and repassivation.

IV·C Hydrogen implantation for GaP/Si interface passivation

Inspired by the a-Si:H technology and its passivation capabilities, another way to obtain proper interface lifetime may be to implant hydrogen directly towards the interface. To do so, we used a inductive plasma chamber from Applied Materials (300 mm Centura AdvantEdge Mesa silicon etch system). Different H_2 plasma conditions were tested, by adjusting bias (W_b) and source (W_s) power to be as soft as possible and prevent GaP etching instead of actual implantation. Plasma processes were performed during 60 seconds on GaP on unannealed silicon, passivated on the back side with a-Si:H. GaP thickness was monitored with an in-situ ellipsometer. We compared various processes with source power varying between 400–800 W at 5 Torr. The bias power is adapted to the source power to maintain the ion energy around 100 eV. One process was also performed without bias power to minimize the ion energy. For the 400 and 500 W_s processes, a short step at 25 mTorr was necessary to start the plasma before operation at 5 mTorr.

After plasma exposure, lifetimes were measured, and are plotted in Figure IV·6. All plasma conditions resulted in degraded lifetimes, which could be explained by alteration of GaP and increased defectivity of the layer and its interface with silicon. As an attempt to trigger hydrogen passivation of dangling bonds by hydrogen diffusion, samples were heated for 10 min at 200℃ on a hot plate, and measured again. Minority carrier lifetime remained worsened, indicating aggravation of the defects and maybe loss of the implanted hydrogen.

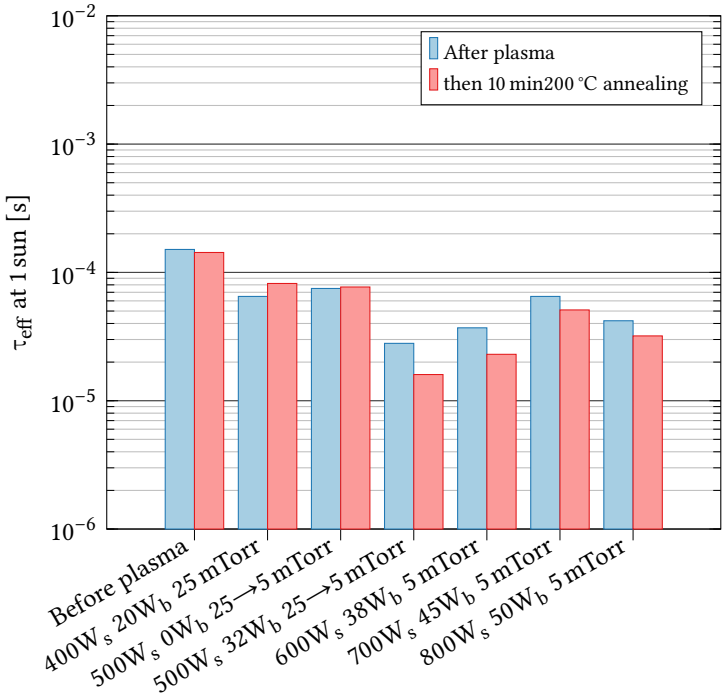

Figure IV·6: QSSPC τ_{eff} at 1 sun of GaP/Si/a-Si:H samples exposed to various hydrogen plasma for 60 second, after plasma treatment, and after 10 min 200℃ annealing on a hot plate.

IV·D GaP/Si interface and bulk GaP contaminants

IV·D·1 Effect of air exposure

Interface defects can also be brought by contaminants during epitaxy, or afterwards when exposed to air. To detect those contaminants, parallel angle XPS analyses were performed on two GaP/Si samples: one directly was transferred to the XPS setup through an air-tight enclosure and measured within 3 hours after epitaxy, and the other one was left exposed to air (outside the clean room) for a week. Resulting spectra are presented in Figure IV·7 and Figure IV·8, after in-situ soft etching (argon ion milling) to remove surface contamination. With

parallel angle analyses, the spectra recorded near normal incidence (23.75° here) represent the global composition of the first ~10 nm of the surface while the spectra recorded at grazing angles (76.25° here) are only representative of the few first nanometers of the surface. We only show here the spectra for the 23.75° angle, with the deconvulated contributions of the atomic bonds. The graph on the right-bottom corner plots all the calculated atomic fractions for each angle, emulating a composition profiling. The atomic fractions are based on the ratios of areas of the peaks. Error of such method is between 20 and 30%, which still enables us to discuss the evolution of the composition along the angles. Let us compare each spectra, from top to bottom, left to right.

Si2p scans On these scans we see the silicon bonds, Si-Si and Si-metal (probably Si-Ga, Si-P), gallium bonds to oxygen and phosphorus. When comparing the two spectra, we see that the vacuum-transferred sample displays a clear Si-Si peak at lower binding energies, hinting that the soft etching may have been stronger so it enables us to detect the silicon substrate.

P2p scans Here, we see a small peak for the P-O bonds absent in the vacuum-transferred sample, indicating oxidation of the GaP layer when exposed to air. The peaks of P-Ga are broader in the vacuum-transferred spectrum, which forces us to integrate additional peaks denoted "Scan A". These peaks are linked to the disorder induced by the etching, which make second- and third-order bonds more visible by XPS, and thus broaden the peaks.

Ga3d scans We see Ga-P peaks, again broader in the second sample, for the same reason described earlier.

As3d scans We observe here multiple peaks associated with arsenic and antimony. However their intensity is very low, which shows that they are residuals from the epitaxy, with total concentration below 1%. These peaks are not taken into account in the general calculation of the atomic composition.

C1s scans Here, the single and double bonds C-O are visible along C-C peaks in the air-exposed sample. These peaks totally disappear (small and noisy peaks) on the other sample, confirming the air exposure brings carbon and oxygen in GaP.

O1s scans A clear peak for O-C is detected in both samples, with slightly lower intensity for the vacuum-transferred sample. Absence of C-C bonds but detection of O-C bonds in this layer may be an indication of a fault in the vacuum, and great GaP sensitivity to oxigen.

N1s scans We detect the Auger peaks for gallium, which are not taken into account in the concentration calculations. A small peak for N-H is detected, which may reveal nitrogen and hydrogen residuals from the MOCVD chamber.

Finally, the concentration profile of the air-exposed sample shows a decrease down to 10% in the GaP bonds signals at higher angle, so near the surface, accompanied by an increase from 17 to 27% of the O-C and C-C bonds, which confirms the surface organic contamination. Near normal angle, so observing deeper into the layer, we see a discrepancy between Ga-P and P-Ga bonds (20% vs 32%), which may indicate of preference for gallium oxidation.

In the vacuum-transferred sample, concentrations remains more or less constant across the scanning angles, except for the O-C bonds which may again be explained by a not-so-airtight enclosure, due to the 3 hours waiting time between epitaxy and the measurement. C-C bonds remain constant, below 5%, confirming that carbon from the epitaxy precursors is integrated in the layer.

IV·D·2 Surface vs bulk GaP

To obtain more information on the chemical composition of GaP far from its top surface and closer to its interface with Si, we fabricated a 50-nm-thick GaP/Si sample. The sample was not vacuum-transferred and, within a couple of days, measurement is performed after soft etching of the surface, and after deep etching into the layer until few nanometers above the interface. Spectra are not shown here, only the profiles calculations.

Firstly, on the deep-etched sample, we see a high contribution of Si-Si bonds which decrease when observing at grazing angles. This confirms that we are quite close to the interface with the substrate. On the surface profile, the sum of P-Ga and P-disorder (evoked above) is calculated, to confirm that Ga-P and P-Ga bonds are quite close at both depths: GaP is stoichiometric. This time C-C bonds are found to be more present than O-C bonds, which indicates that carbon contamination is faster than oxidation. This is not surprising, as surface carbon contamination can be brought by chemisorption of CO_2 but also physisorption of organic compounds in the air. Oxidation, however, is a chemical reaction which requires more time to penetrate the layer.

To summarize, the extrinsic contaminants in the GaP layers were found to be carbon, oxygen, arsenic and antimony. As and Sb remained in minute amounts, below 1%. Silicon has been shown to be strongly oxidized by atmospheric oxygen, and traces of oxygen remained deeper in the sample, while carbon is confined near the surface. 5% carbon remains however deeper in the layers, indicating that epitaxy residuals remain.

IV·E Wetting layers for GaP epitaxy

As an attempt to increase interface lifetime, we tested different silicon pre-expositions before GaP epitaxy: the regular phosphorus , arsenic [66, 115], and antimony. Taking advantage of recent development in III-V integration on silicon [109], the chosen substrates were miscut by 0.18° toward (110). Being almost nominally oriented, they presented good bulk lifetime as-received (see Reference in Figure IV·10). Substrates were either pre-annealed, or not. Growth was either continuous (TMGa and TBP being simultaneously introduced in the MOCVD chamber), or by ALE. As a third growth condition, ALE process could also be followed by a post-annealing under TBP at 500℃ during 5 min to allow layer reorganisation and better crystalline quality [120].

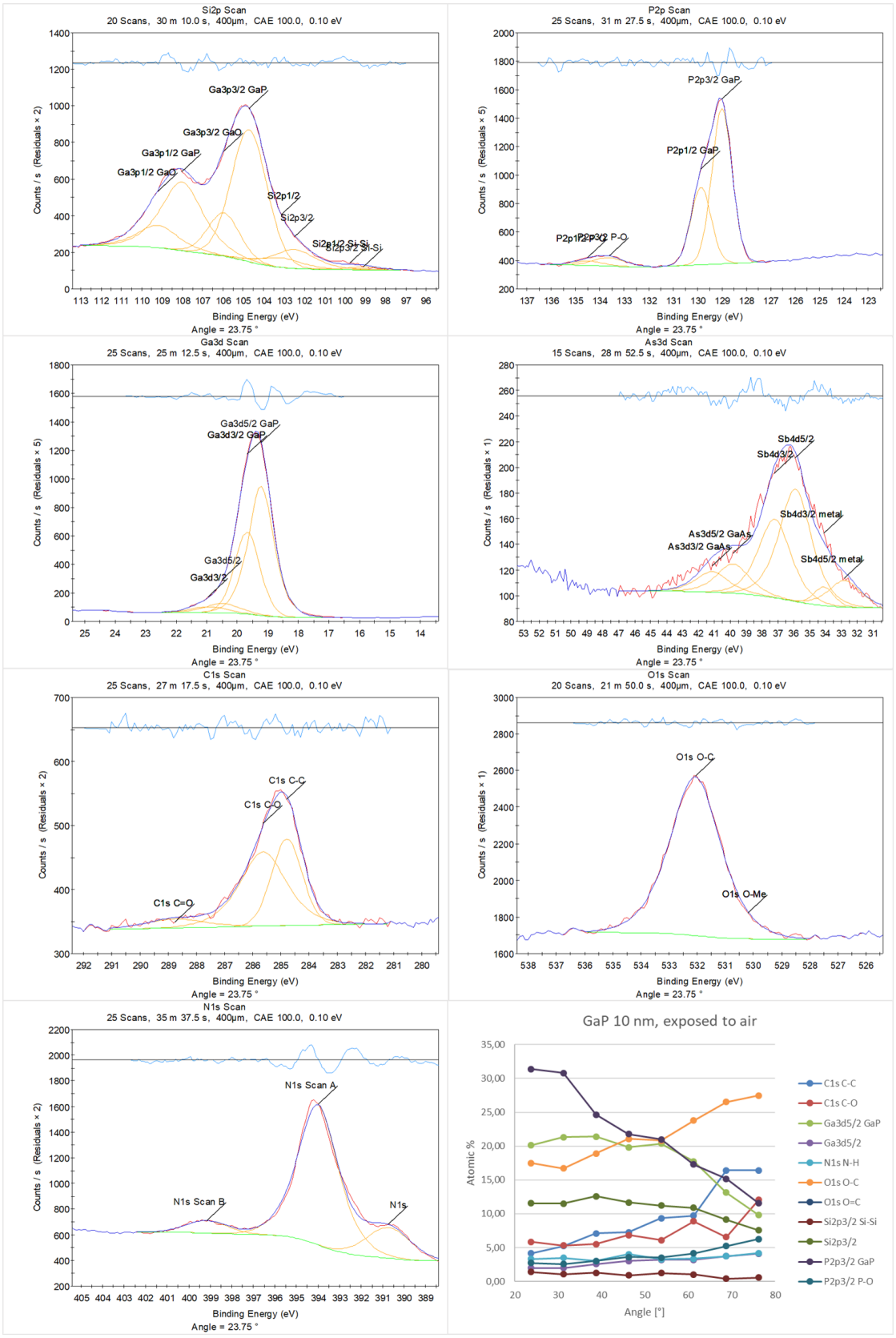

Figure IV·7: XPS spectra of the 10-nm-thik GaP layer on silicon exposed to air.

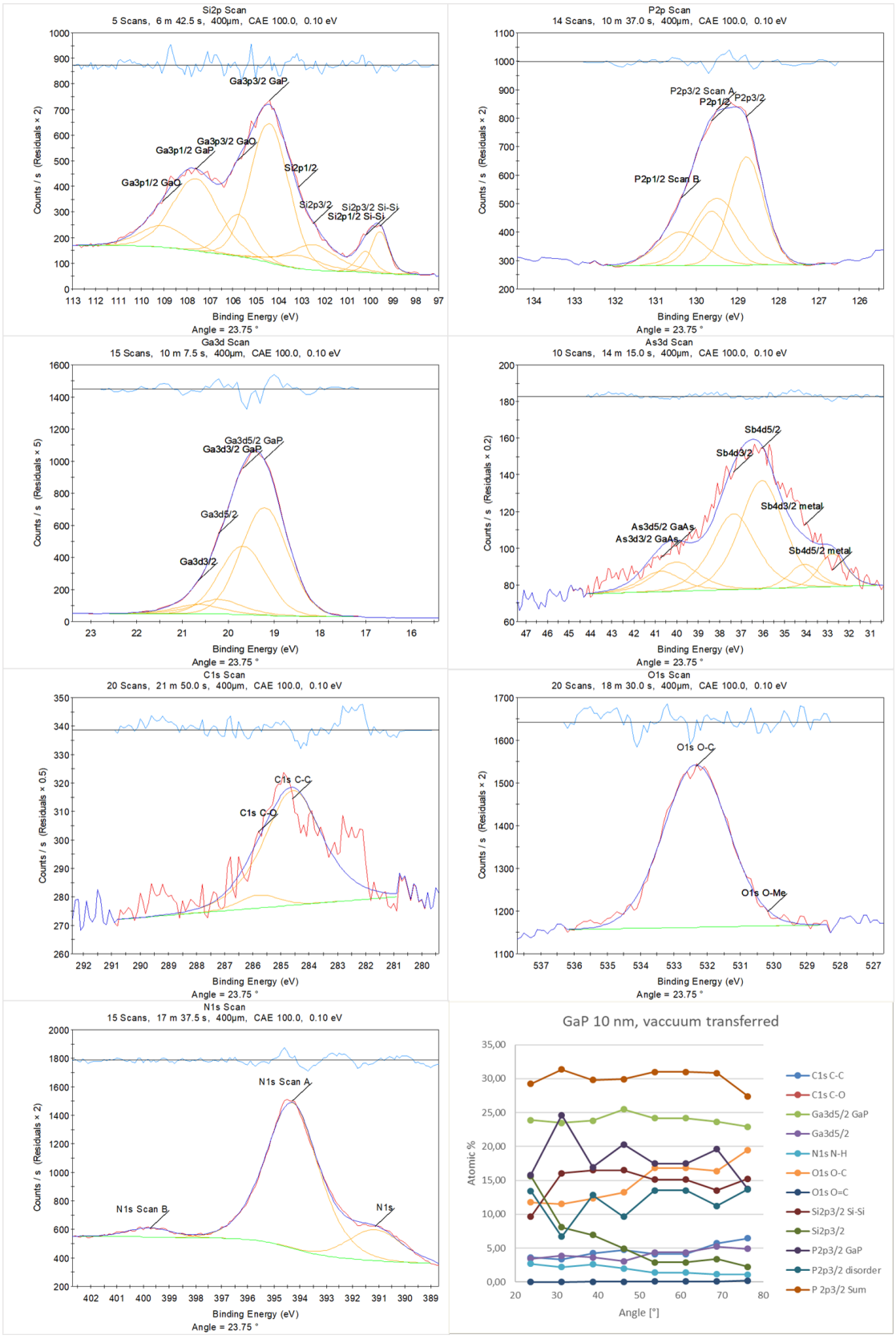

Figure IV·8: XPS spectra of the 10-nm-thik GaP layer on silicon vacuum-transferred.

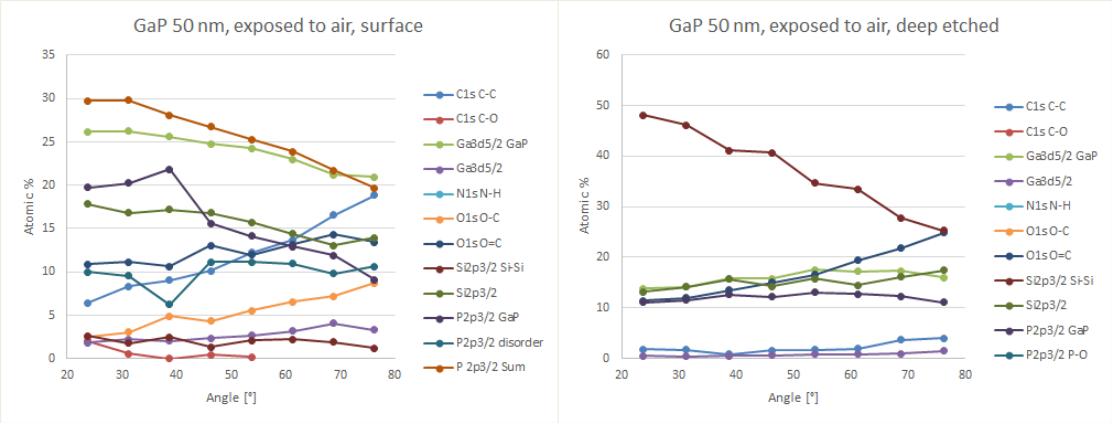

Figure IV·9: Composition profiles from XPS spectra of the 50-nm-thick GaP layer on silicon.

After MOCVD process, back-sides were passivated with a-Si:H and the minority carrier lifetime was measured by QSSPC. The GaP surface roughness was measured by AFM. The results of these measurements are summarised in Figure IV.9.and 20. We can see that:

- We obtained lower roughness with pre-annealing, hinting at better layer quality. However, this lower roughness is not correlated with higher minority carrier lifetime that is also impacted by the pre-annealing step in these cases.
- The minority carrier lifetime of all samples is low. The minority carrier lifetime for ALE is slightly better except with P wetting layer. Best results were obtained with ALE preceded with As wetting, as seen in literature [115, 121, 122].
- In any case, the lifetime is too low to envision high efficiency cells.

Some representative AFM pictures are shown in Figure IV·11. All samples display GaP clusters on their surface, demonstrating 3D growth. Sb pre-exposition is non-optimised, as it tends to coalesce and form even bigger clusters. When comparing the (a) and (b), without and with pre-annealing, one can easily see the surface reconstruction, but it is outlined by trenches in the material: the surface reconstruction was not optimised, and favoured the emergence of monoatomic steps from which grew systematically antiphase boundaries, which were then etched away by the post-annealing step.

These experiments lead therefore to the conclusion that whatever the growing conditions investigated here, the interface and the GaP quality remain too defective to enable a silicon minority carrier lifetime larget than 1 ms required for high efficiency solar cells fabrication.

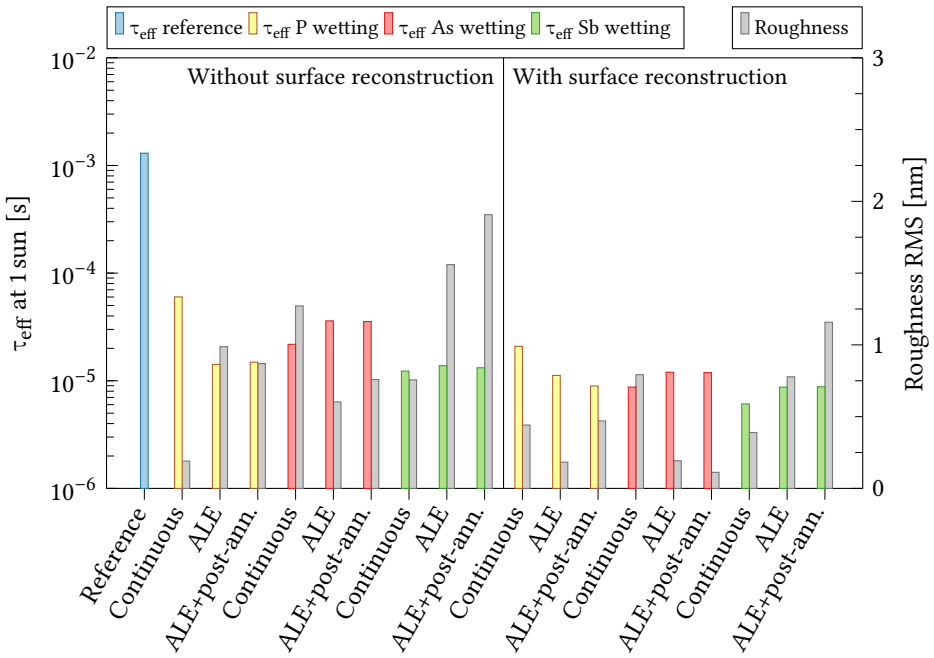

Figure IV·10: QSSPC τ_{eff} and surface roughness with different epitaxy conditions and wetting layers.

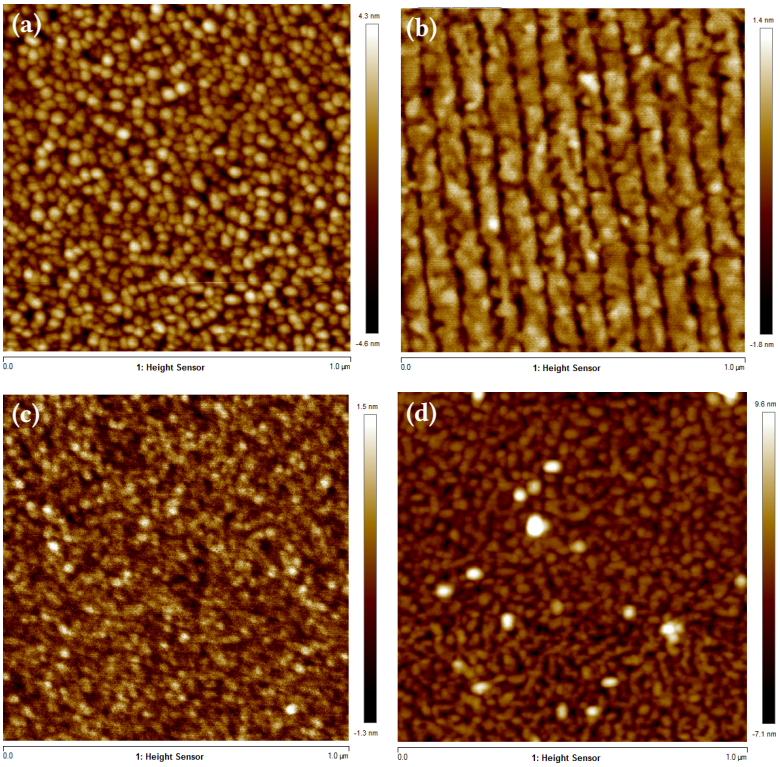

Figure IV·11: AFM pictures of ALE GaP with P wetting layer and post-annealing, (a) without and (b) with surface reconstruction, (c) standard GaP epitaxy without preannealing (d) GaP on Sb wetting layer

IV·F Conclusion on the GaP/Si interface passivation

In this chapter, we identified two annealing chambers that either do not degrade (VT412) or marginally degrade (SiGe-MOCVD) the silicon substrate for its surface reconstruction. We discovered that the 4°-miscut wafers present intrinsically lower bulk lifetimes, which can be recovered during the annealing. Due to unoptimised epitaxy, 0.18°-miscut wafers did not produce biatomic steps, and the subsequent GaP APBs were etched.

GaP/Si interfaces at the state of the art on epitaxial quality are not passivated. Trying to passivate the GaP/Si interface by hydrogen implantation rather degraded the GaP layer and the effective lifetime. Finally, we detected traces of arsenic and antimony, and around 5% carbon left during the epitaxy. GaP was found to be stoichiometric. However, oxidation and carbon contamination by air of the GaP layers is important, and C-O bonds become predominant near the surface after long air exposure.

To summarize, even if some solutions exist to anneal the wafer in conditions that do not degrade the bulk silicon minority carrier lifetime, we have not identified GaP epitaxy conditions that are able to improve the GaP/Si interface, so that the passivation is good enough for high efficiency solar cells fabrication.

V Solar cells fabrication and results

V·A Solar cells fabrication and performances

The lifetime analyses performed in Chapter III revealed a contamination of the silicon substrate by fast-diffusing contaminants. The wetting layer experiments of chapter IV have shown that surface reconstruction is important to reduce the GaP roughness, and higher roughness is associated with lower lifetimes if the substrate surface is not reconstructed. Considering these effects, the fabrication of solar cells with better performances will still need the surface reconstruction annealing, combined with additional steps designed to remove the fast-diffusing contaminants and increase substrate lifetime.

V·A·1 Integrating decontamination steps for GaP/Si solar cells

Fast-diffusing metallic contaminants can be removed from silicon through gettering and removal of gettered contaminants. [123, 124] Gettering involves three steps:

1. Moving metallic contaminants and metallic precipitates dissolution into interstitial position at high temperature (> 700°C), favoured by their replacement with interstitial silicon (auto-interstitials) ;
2. Diffusion of interstitial atoms, again temperature-lead ;
3. Capture of the impurities, which can be performed in the phosphorus-rich silicon under the influence of two phenomena:
    - Segregation: metallic contaminants have higher solubility in (n+) silicon ;
    - Relaxation: Si-P lattice is smaller than silicon, as well as the formation of SiP precipitates lead to the formation of dislocations into which are captured the metallic contaminants.

Full decontamination is then reached by etching the capture layer, named getter layer.

V·A·2 Tested gettering techniques

The high temperatures involved in the gettering steps may impede their integration in the fabrication process flow of GaP/Si solar cells. Indeed, thermal treatments after epitaxy may aggravate the lattice mismatch between gallium phosphide and silicon, as their thermal expansion coefficient differ. To prevent so, two gettering techniques were tested: phosphorus implantation and phosphorus diffusion.

V·A·2·a Implantation of phosphorus

Phosphorus implantation is convenient, as it is a low temperature process that can be performed on only one side of the substrate [125, 126]. It introduces a high concentration of phosphorus and dislocations near the surface, which covers the capture step of gettering. The first two steps of gettering, requiring high temperature, could be activated during the surface reconstruction pre-annealing, at the same time as the substrate is exposed to the impurities. To verify so, the experiment described in Figure V·1 was performed.

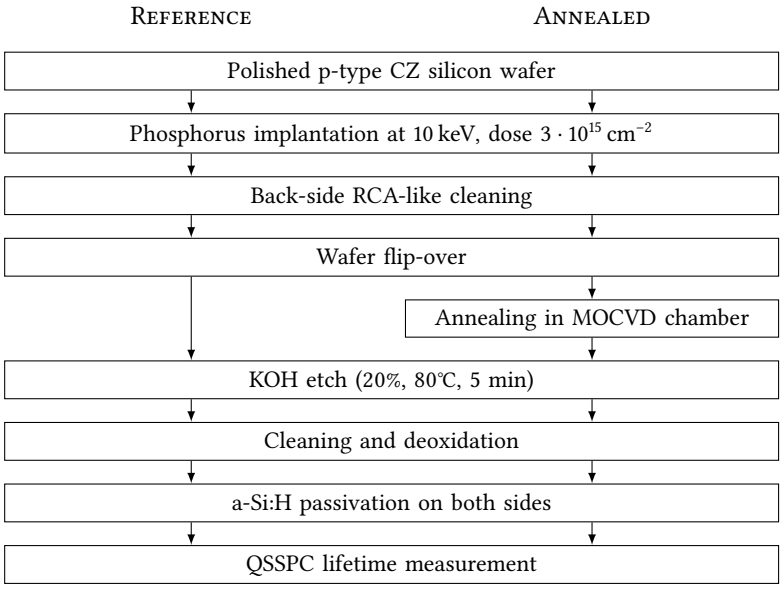

Figure V·1: Phosphorus implantation experiment.

The obtained lifetimes are shown in Figure V·2, with the carrier lifetime at 10 ms in the implantation reference wafer, and at 43 µs in the implanted and annealed wafer, both after etching of the phosphorus-implanted layer. This experiment shows that simultaneous contamination and gettering is not achievable, which leaves the option to use phosphorus diffusion as gettering trigger.

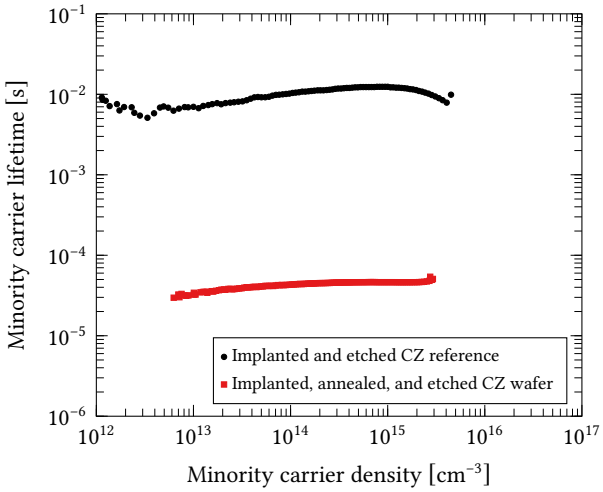

Figure V·2: QSSPC τ_{eff} of implanted CZ wafers,
with or without the surface reconstruction annealing.

V·A·2·b Diffusion of phosphorus

Gettering can be performed by phosphorus diffusion from $POCl_3$ gaseous atmosphere that, at high temperature (>750℃, optimally 840℃), decomposes at the surface of silicon to form phosphosilicate glass (PSG). This step is followed by a drive-in, a lower temperature step without $POCl_3$ that enables further phosphorus diffusion into silicon (≈ 500 nm).

Phosphorus diffusion is a convenient way to perform gettering, as the $POCl_3$ decomposition temperature is high enough to trigger at the same time the removal of contaminants from substitutional positions and their replacement by auto-interstitials. Auto-interstitials come from silicon being kicked-out of the lattice by diffusing phosphorus, SiP precipitates, and oxidization of silicon at the surface.

However, phosphorus diffusion cannot be performed as-is, its integration needs some adaptation of the process flow.

V·A·2·b·i Adapting the process flow

Lowering the temperature To limit the risk of GaP relaxation on silicon, the phosphorus diffusion temperature, after epitaxy, is reduced down to 750℃. To accommodate this colder, and less efficient diffusion, one can increase the diffusion duration.

Considering an iron atom on one side of the wafer, with the phosphorus diffusion occurring on the other side, the time needed for the atom to diffuse is derived from the following equations.

$$L = \sqrt{D \cdot t} \tag{V·1}$$

$$D_{Fe_i} = (1.0^{+0.8}_{-0.4}) \cdot 10^{-3} \cdot \exp\left(-\frac{0.67\,\text{eV}}{k_B T}\right) \tag{V·2}$$

where L is the diffusion length [cm],
t is the diffusion duration [s],
D is the diffusivity of interstitial iron in silicon [cm·s^{-1}], from [127],
After calculation, it emerges that reducing the diffusion temperature from 840℃ to 750℃ doubles the time required for an iron atom to cross a 280-µm-thick silicon wafer. Drive-in temperature are thus rounded to half an hour.

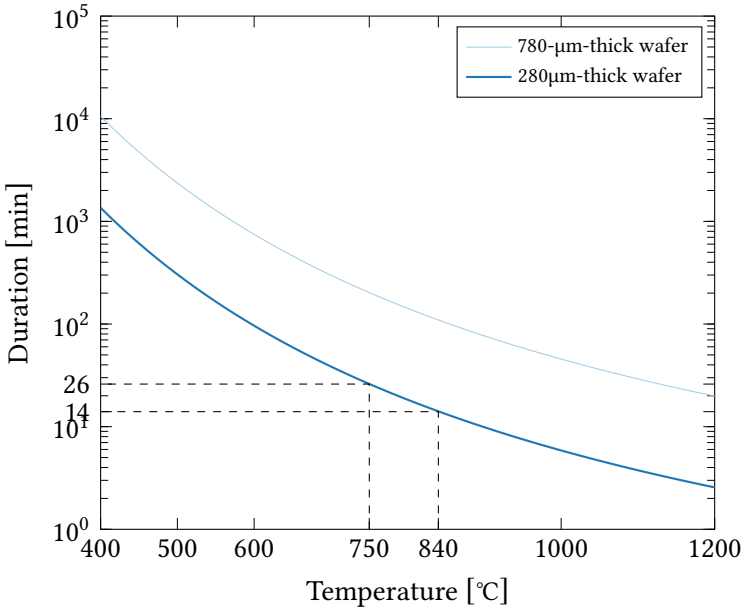

Figure V·3: Diffusion duration needed for a theoretical iron atom to cross 280- and 780-µm-thick wafers.

Preventing diffusion on front side Due to the design of the diffusion tubes, diffusion happen on both sides of the wafers. However, pre-diffusion on the front side leads to the formation of a (n+/p) junction within the crystalline silicon, which is not in the scope of this study. Moreover, the formation of phosphosilicate glass at high-temperature on the front side during the post-diffusion may lead to degradation of the GaP layer. Diffusion of phosphorus through its thin layer may greatly affect its crystalline and optical properties. To prevent the deposition of PSG on the front side of the wafer, and on GaP, a 550-nm-thick SiO_x diffusion barrier is deposited by PECVD on the front side before the pre-diffusion.

Initial tests were performed with silicon oxide deposited at 220℃ in the PEVCD-PVD cluster on GaP/Si. The test samples were then exposed to the phosphorus diffusion treatment at 750℃

and etched with KOH (§ II·A·7·c·iii). Figure V·4 show the revelation of pinholes that are associated with the low density of SiO_x deposited at 220℃, making it susceptible to etching after high temperature treatment. No pinholes were observed after SiO_x deposition at 450℃ in a dedicated PECVD tube. The subsequent higher temperature depositions of diffusion barriers were performed with this method.

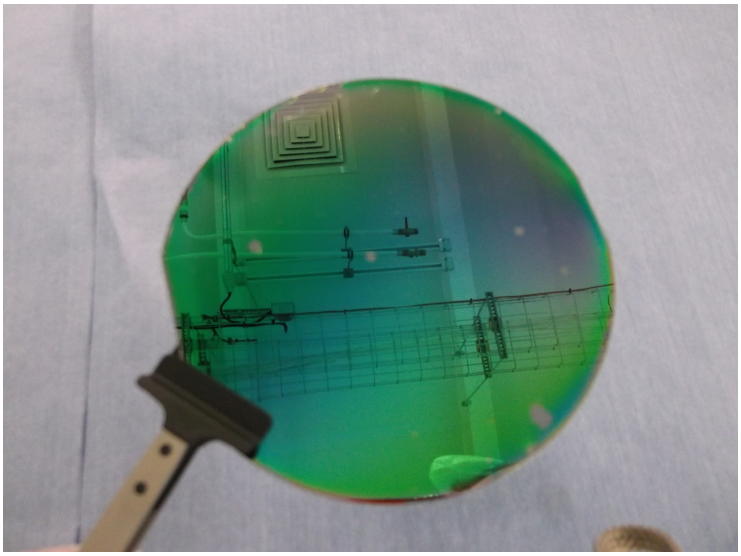

Figure V·4: Photograph of pinholes on a 220℃-SiO_x/GaP/Si stack after phosphorus diffusion and KOH etching.

Maximizing the gettering effect As the gettering temperature was lowered, a preliminary back-side diffusion (pre-diffusion) at nominal temperature was considered, in addition to the post-epitaxy diffusion (post-diffusion), to maximize the incorporation of phosphorus and improving the gettering effect. The two cumulated diffusions give an 800-nm-deep dopant profile, drawn in Figure V·5. The 5-min-long KOH etching is enough to remove that much silicon.

Solar cells fabrication process flow with decontamination steps The final fabrication process flow of solar cells with decontamination depicted in the Figure V·6. GaP was deposited with 20-nm-thick layers, to accommodate any loss GaP by the etching steps.

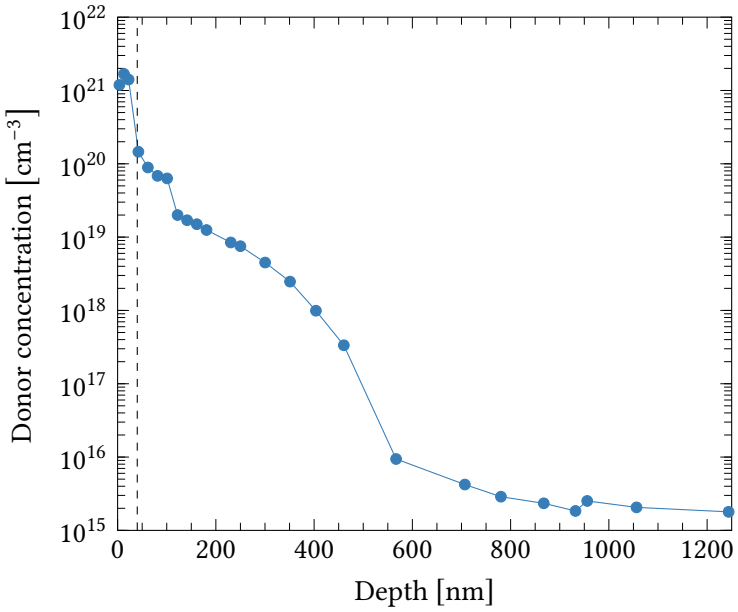

Figure V·5: Donor concentration profile measured by ECV on a FZ (p)c-Si sample with both pre- and post-diffusion.

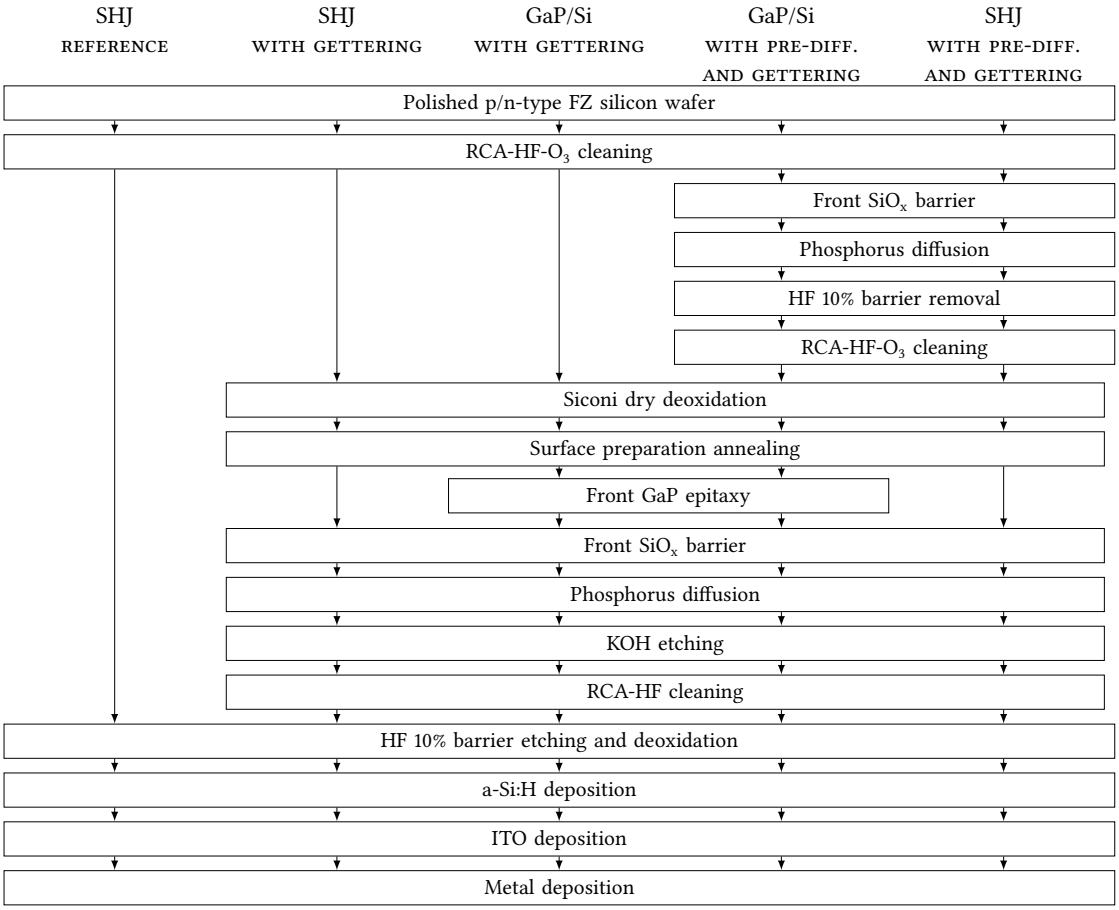

Figure V·6: Solar cells fabrication process flow with decontamination steps.

V·A·2·b·ii Lifetime of precursors

To check the curing effect of this decontamination process flow, annealed silicon was subjected to the gettering steps, with or without pre-diffusion. The resulting lifetimes after a-Si:H passivation on both sides are given in Figure V·7. Lifetime of the unannealed reference samples remain at the same level after gettering: the gettering steps do not degrade the lifetime. Lifetime of the annealed samples is partially recovered with regular gettering, and reaches 1 ms with pre-diffusion.

Trap dissociation under illumination is monitored by µW-PCD, and reported in Figure V·8. This measurement confirms the lifetimes measured at 1 sun, but shows a slight dissociation effect for the gettered annealed wafers, as the lifetime gains approximately 40 µs with or without pre-diffusion. The partial lifetime recovery and dissociation effects may be explained by unoptimized decontamination steps that still leave a small amount of contaminants in the silicon substrate. Still, 1 ms minority carrier lifetime was achieved with pre-diffused, annealed and gettered silicon.

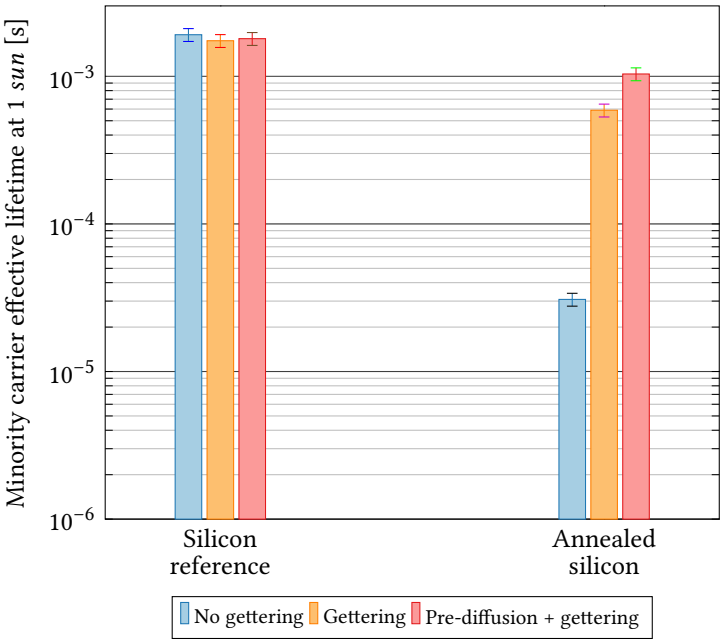

Figure V·7: τ_{eff} at 1 sun of precursors after the different gettering steps.

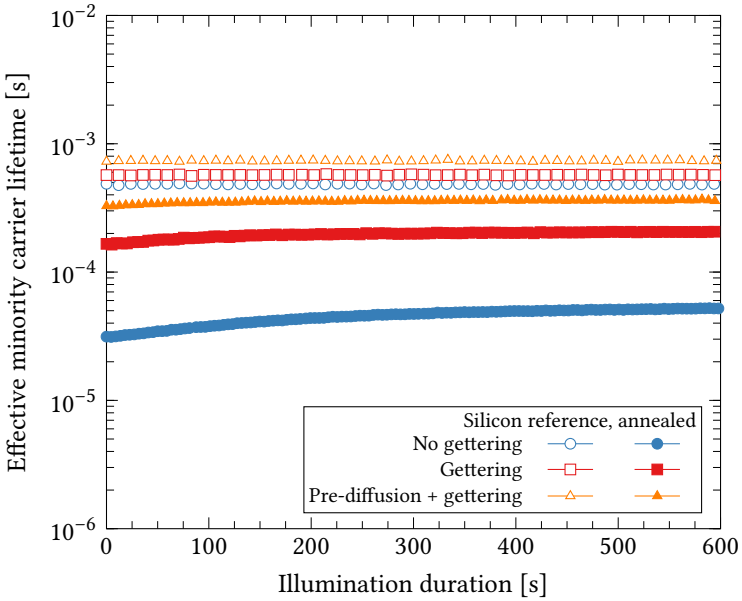

Figure V·8: μWPCD τ_{eff} vs time of precursors after the different gettering steps.

V·B Solar cells fabrication and measurement

The successful preliminary tests on solar cells precursors confirmed the process flow proposed earlier. Several alternative conditions were tested to improve performance: SiO_x diffusion barrier, SiO_x/SiN diffusion barrier, and GaP used as window layer rather than emitter.

V·B·1 SiO_x diffusion barrier

V·B·1·a Passivation of the solar cells precursors

The minority carrier lifetime of the precursors were measured after epitaxy and a-Si:H deposition and are reported in Figure V·9. SHJ reference precursors have a similar carrier lifetime spanning from 865 to 883 µs. This passivation level is lower than the one obtained during the preliminary tests, as a-Si:H layers in SHJ solar cells are thin (approximately 20 nm) which cannot passivate c-Si surface as well as thicker a-Si:H (70 nm). However, this does not explain the annealed precursor gettered with pre-diffusion that does not top 384 µs. This may be caused by increased contamination from the MOCVD chamber (hinted by the reproducibility discussed in § III·C·2), or unwanted variations in the gettering steps. Cell precursors with GaP show quite low carrier lifetime, 13 µs at best. Their bulk lifetime is higher, so by elimination this low lifetime is to be attributed to GaP and its lack of passivation of the c-Si surface.

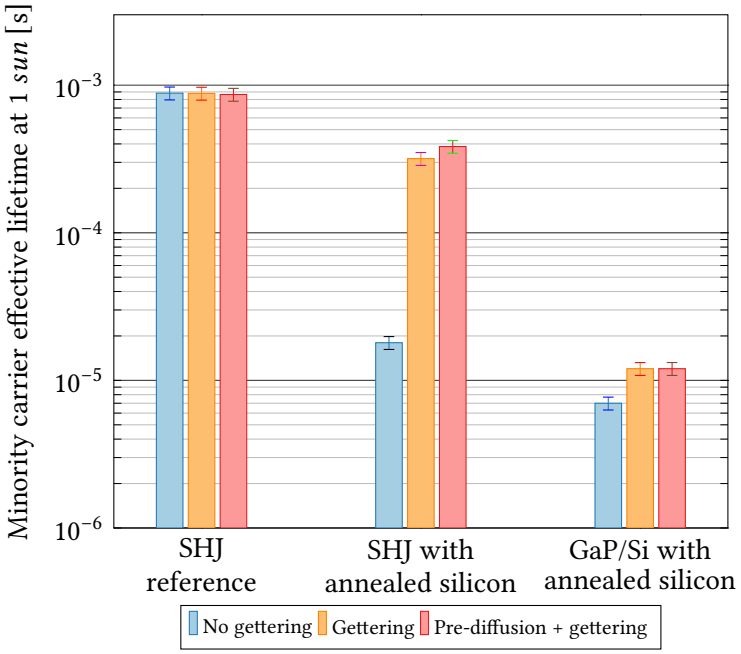

Figure V·9: τ_{eff} at 1 sun of precursors with SiO_x diffusion barrier for gettering.

V·B·1·b J–V and efficiencies

Unfortunately, all the fabricated solar cells from this batch were providing very low current (all below 10 mA·cm^{-2}), with low FF (all < 36%) and efficiency (all < 10%). Implied- and pseudo-characteristics, obtained by EQE measurements, Sinton, Suns-V_{oc}, and summarized in Table V·1, show respectively normal pJ_{sc}, iV_{oc}, and pFF (around 34 mA·cm^{-2}, 700 mV and 80%) for the reference solar cells. This reveals a processing error during the metallisation, which could not achieve sufficient carrier extraction during J–V measurement, as expected from the integration of EQE spectrum (§II.B.4.c). The current-density–voltage curves are thus chosen not to be displayed here, as it is impossible to extract any conclusion from them, and to further the discussion on the pseudo-efficiencies calculated with pJ_{sc}, iV_{oc} and pFF.

Table V·1: Implied-V_{oc}, pseudo-J_{sc}, -FF, and -efficiency of solar cells with SiO_x diffusion barrier.

Solar cells		Pseudo-performances			
Type	Treatment	iV_{oc} [mV]	pJ_{sc} [mA·cm^{-2}]	pFF [%]	$p\eta$ [%]
SHJ reference	No gettering	701	34.5	80.5	19.5
	Gettering	701	34.1	81.6	19.5
	Pre-diffusion + gettering	700	34.4	82.3	19.8
SHJ with annealed silicon	No gettering	582	34.4	79.5	14.9
	Gettering	664	32.2	79.2	18.0
	Pre-diffusion + gettering	670	34.3	79.9	18.4
GaP/Si with annealed silicon	No gettering	556	31.3	81.2	14.1
	Gettering	572	19.4	67.5	7.50
	Pre-diffusion + gettering	572	19.9	68.8	7.83

Current density extracted from the EQE measurement are rather unaffected by the surface reconstruction annealing and gettering steps on the SHJ solar cells, being around 34 mA·cm^{-2}, with a loss of 2.3 mA·cm^{-2} between the SHJ references with unannealed and annealed silicon. GaP/Si solar cells with gettering steps show a significant decrease of current density, calculated down to 20 mA·cm^{-2}. This loss of generated current is associated with the passivation loss measured along the lifetime measurements, being around 700 mV for unannealed solar cells and decreased down to 582 mV for the SHJ reference with degraded bulk. The degradation is partially recovered, as previously shown by the IQE and lifetime measurements: the equivalent cells with gettering have iV_{oc} around 670 mV. However, the loss of passivation between GaP and silicon is confirmed here, with iV_{oc} below 580 mV at best.

pFF, measured by Suns-V_{oc}, is over 80% for reference cells et still closer to 80% for all solar cells with annealed silicon . This shows that the gettering steps do not strongly impact the bulk recombination (or shunt) loses in the solar cell. We cannot conclude on the series resistance loses though measurements of pFF do not take into account series resistance losses. However, pFF goes from 81.2% in GaP/Si solar cells with annealing and without gettering to below

68.8% with gettering, which outlines the recombinations mechanisms associated with the loss of passivation or shunt.

Finally, the pseudo-efficiencies reflect the characteristics mentioned above: SHJ solar cell with unannealed silicon have almost 20% pseudo-efficiency (pη), which is standard for SHJ solar cells without texturization. The equivalent solar cell with annealing have 14.9% pη, restored up to 18% with gettering and 18.4% with gettering and phosphorus pre-diffusion, well aligned with the IQE measurements. Non gettered GaP solar cell shows almost the same efficiency as the non gettered solar cell. On the other hand, gettered GaP cells have strongly decreased efficiency through a non-expected loss in J_{sc}. A deeper analysis with IQE measurements is mandatory to understand this loss.

V·B·1·c Internal Quantum Efficiency

IQE measurement of the solar cells enable a deeper analysis of the effects of the gettering steps on the collection efficiency (Figure V·10). The IQE of the SHJ reference solar cells show the characteristic degradation of infrared photons collection efficiency, starting 700 nm, when the surface reconstruction annealing is performed on their substrate. Gettering achieves here a partial recovery of the IQE, with a rectification of the collection efficiency up to 1000 nm. However, the IQE of GaP/Si solar cells behaves differently. The GaP/Si solar cell, with surface reconstruction annealing and without gettering shows lower collection efficiency between 300 and 410 nm, higher between 410 and 580, and lower up to 1200 nm, when compared to the one of the SHJ reference solar cell. This confirms the observations made in § III·A on the preliminary solar cells. However, if gettering steps are applied, the IQE is severely decreased across the whole light spectrum, with a maximum at 70%. This degradation may be a manifestation of complete passivation loss at the front GaP/Si interface, or junction degradation.

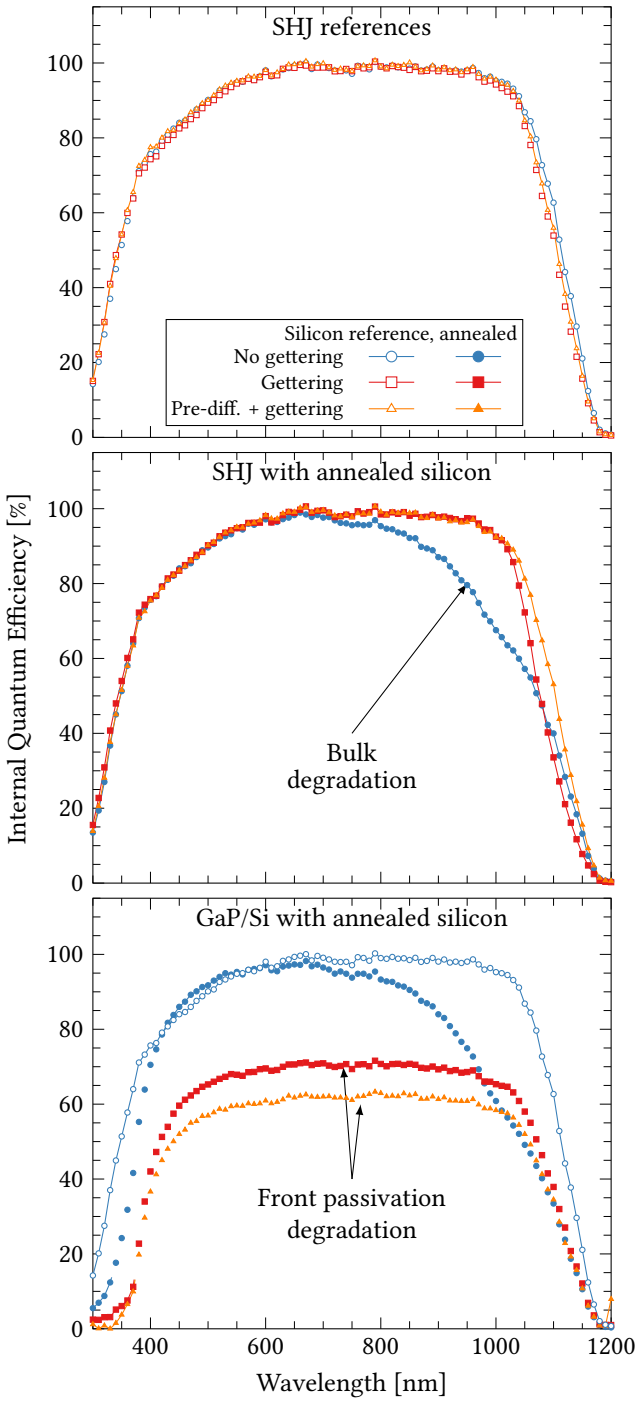

Figure V·10: Internal Quantum Efficiency of solar cells with SiO_x barrier for gettering.

V·B·1·d Photoluminescence

Finished solar cells were observed by photoluminescence to estimate the localization of defects that may affect the effective lifetime. These pictures reveal some scratching that could have affected the surface passivation. However, the black spots density in the three SHJ references (first row) is not correlated with the notable differences in carrier lifetime, while the mean PL correlates the variations in carrier lifetime. Thus, carrier lifetime and photoluminescence are there mainly driven by the carrier lifetime in the silicon bulk (maximum signal around over 104 counts). This observation can be extended to the SHJ solar cells with annealed silicon (second row). The maximum PL signal in the solar cell with annealed silicon is twenty-five to thirty thousand times lower than in the solar cells with cured substrate. Finally, when front a-Si:H emitter is replaced with GaP (last row), almost no PL is observed: GaP/Si interface is highly defective and strongly prevents radiative recombination (maximum signal around 500 counts, with a five times longer excitation flash than for the references).

V·B·1·e Morphology of the materials after decontamination steps

To confirm the hypothesis of the passivation loss between GaP and silicon after gettering steps, the cross-section of layers is observed by TEM (Figure V·12), from the edges of the wafers after cutting out the solar cells. On the left one can see the 20-nm-thick GaP layer, enclosed between ITO and silicon. This picture shows a rather defective layer, with dislocations and what may be multiple grains or APDs (despite the surface reconstruction). On the right, with a larger scale, one can see the 100-nm-thick ITO, deposited on a notably degraded GaP, with high roughness and thickness decrease that can be attributed to the etching steps. SiO_x deposition on GaP, and the following thermal treatments may induce GaP oxidization. Half of the GaP is lost on the right of the picture, which may be an indication of deeper etching occurring elsewhere on the samples, up to shunt formation with ITO directly contacting the silicon. This would definitely explain the loss of passivation and junction shorting observed by IQE.

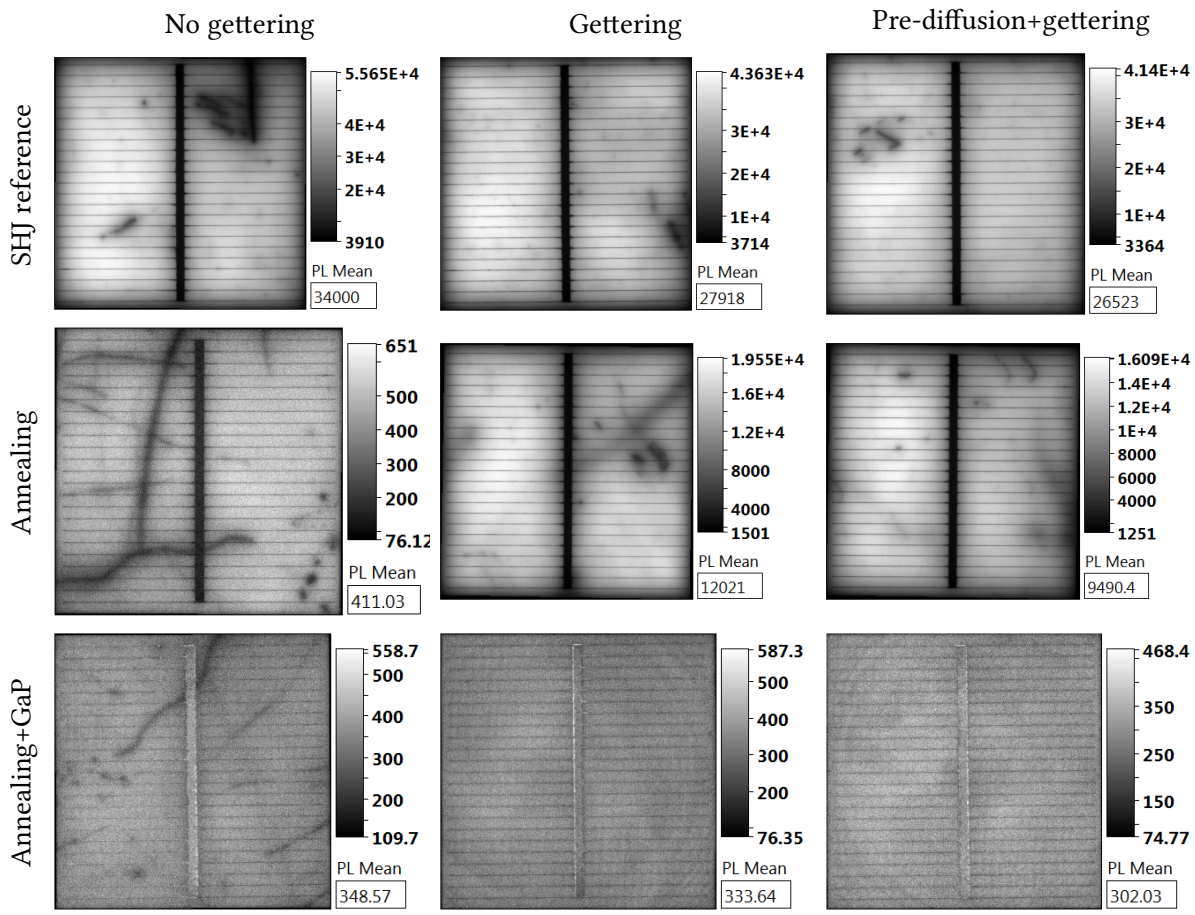

Figure V·11: Photoluminescence of solar cells from the gettering with SiO_x barrier experiment. Excitation flash is 0.1s, and 0.5s for the lower row. Scale is not the same for all samples to enable observation of the defects.

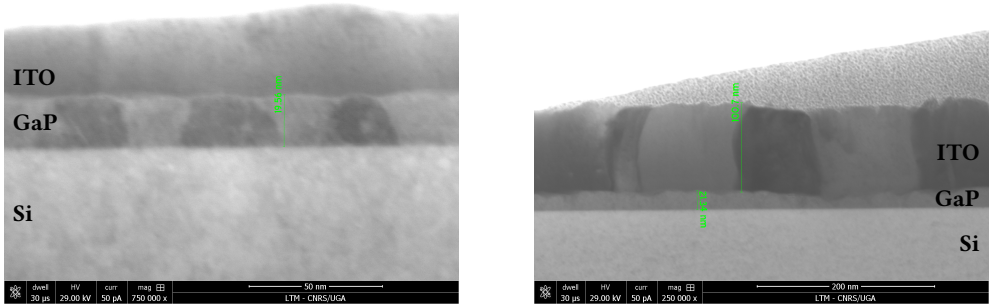

Figure V·12: Transmission Electron Microscopy of ITO/GaP/Si stack from scraps of solar cells (left) without gettering, (right) with gettering.

V·B·1·f Conclusion on the SiO_x barrier for gettering

The introduction of gettering steps in the fabrication process flow of GaP/Si solar cells has proven that one can, at least partially, recover the minority carrier lifetime in the bulk of silicon by performing phosphorus diffusion on the back side, while capping the GaP on the front side. However, while recovered carrier lifetime reached 1 ms during the preliminary tests, it remained below 400 µs in the equivalent solar cell. This discrepancy cannot be solely explained by the lesser passivation of the thin a-Si:H layers and can be attributed to some irreproducibility in the process flow. This results in partial recovery of the Voc, and limitation of the efficiency of the SHJ solar cells to 18.4%, vs 19.8% without degraded substrate.

Furthermore, the deposition of SiO_x on GaP, and its subsequent etching after the gettering steps triggers partial removal of the GaP layer. This may affect the GaP/Si interface passivation, along with probable complete and punctual etching of the emitter. This leads to the emergence of shunts and recombinations that strongly affect the carrier extraction with low Voc, J_{sc}, FF and efficiency (< 8%). To summarize:

- Annealing the silicon substrate in the MOCVD chamber, as already observed in Chapter III, introduces recombination centres that lowers the bulk carrier lifetime, open-circuit voltage and efficiency of the resulting solar cells.
- Decontamination steps increase the degraded efficiency, without reaching the unannealed silicon performances. This is due to the recovery being only partial, with defects remaining in the bulk.
- GaP is strongly degraded by the chemical steps during decontamination that shunt the junction and introduce recombinations. This may be due to the defects in the diffusion barrier made of SiO_x that is not able to protect efficiently the GaP layer.

V·B·2 SiO_x/SiN diffusion barrier

One option to protect the GaP from the degradation observed in the previous solar cells, is to include another material barrier, stronger to chemical etch. One option is to deposit a 100-nm-thick SiN layer before the 550-nm-thick SiO_x. In this case, the thickness of the GaP layer was increased, up to 50 nm, to prevent short-circuits in case of GaP etching even if loses in short-circuit current can be expected. Again, two conditions were tested: without gettering and with gettering.

V·B·2·a J–V and efficiencies

First, J–V measurements were performed in the solar cells (Table V·2). In this case, J_{sc} values were correct for reference cells without any gettering, and values over 16% were obtained, which is expected for polished samples (calculated with real FF and not pFF). When adding the gettering to the reference samples, a 2% efficiency loss is observed, due to the decrease of both V_{oc} and J_{sc}. The reference sample with annealed silicon shows a strong degradation in all properties dropping the efficiency less than 12% and then adding the gettering no measurement was possible. Even though the GaP/Si solar cell with gettering was partially broken after metallisation, all samples with GaP show little or no response to the JV measurements.

Again, to understand all the previous results, Suns-V_{oc} measurements were performed to obtain the pFF, and pJ_{sc} was calculated from the quantum efficiency measurements. Together with the implied-Voc measured after passivation, the data are summarized in Table V·3. Reference cell has 19% pseudo-efficiency, which is closer to what can be expected thanks to texturization. SHJ solar cell with annealed silicon shows the typical degraded performances already observed in all similar cells: strong loss of iV_{oc} due to the low bulk lifetime, that limit the pseudo-efficiency to below 14%. With gettering, there is no alteration of the current density but the efficiency drops below 17%. This loss can be explained by several phenomena. One option is that interface defects have been created due to the getter etching, or even partial removal of the getter that leaves a high-concentration, defective, phosphorus layer on the back side that affects the passivation. Moreover, the low pFF (60.8%) may be attributed also to the metallisation, as it will be shown by photoluminescence. Other options can be related to defectivity in the wafer, or to partial bulk decontamination during gettering. More characterizations need to be done to distinguish between the three options. Because of the low response, no pFF measurement was possible on the GaP/Si solar cell with gettering.

To understand the diode behaviour, dark-J–V curves are shown in Figure V·14. The reference solar cells, and the SHJ with annealed silicon show parallel curves with the characteristic double slopes in direct measurement, demonstrating that the junction is well performing [85, 93]. However, the curve of the reference solar cell with gettering is above the reference without gettering in reverse bias, showing that the gettering introduce leaking current that bypasses the diode. All the other solar cells, SHJ with annealing and gettering, and both GaP/Si solar cells show no junction behaviour and strong leaking currents. This behaviour is typical of junction

Table V·2: Performances of solar cells with SiO_x/SiN diffusion barrier.

Solar cell		1-sun JV			
Type	Treatment	V_{oc} [mV]	J_{sc} [mA·cm^{-2}]	FF [%]	η [%]
SHJ reference	No gettering	695	31.3	75.7	16.4
	Gettering	665	28.8	74.7	14.3
SHJ with annealed silicon	No gettering	621	26.3	71.4	11.7
	Gettering	439	1.0	56.1	0.2
GaP/Si with annealed silicon	No gettering	521	19.7	34.5	3.5
	Gettering	—	—	—	—

Table V·3: Implied-Voc, pseudo-J_{sc}, -FF, and -efficiency of solar cells with SiO_x/SiN diffusion barrier.

Solar cell		Pseudo-performances				
Type	Treatment	iV_{oc} [mV]	pV_{oc} [mV]	pJ_{sc} [mA·cm^{-2}]	pFF [%]	$p\eta$ [%]
SHJ reference	No gettering	703	692	34.6	78.3	19.0
	Gettering	637	658	34.5	75.9	16.7
SHJ with annealed silicon	No gettering	584	616	32.0	73.8	13.8
	Gettering	513	661	34.6	60.8	10.8
GaP/Si with annealed silicon	No gettering	521	520	31.8	75.6	12.5
	Gettering	554	—	24.6	—	—

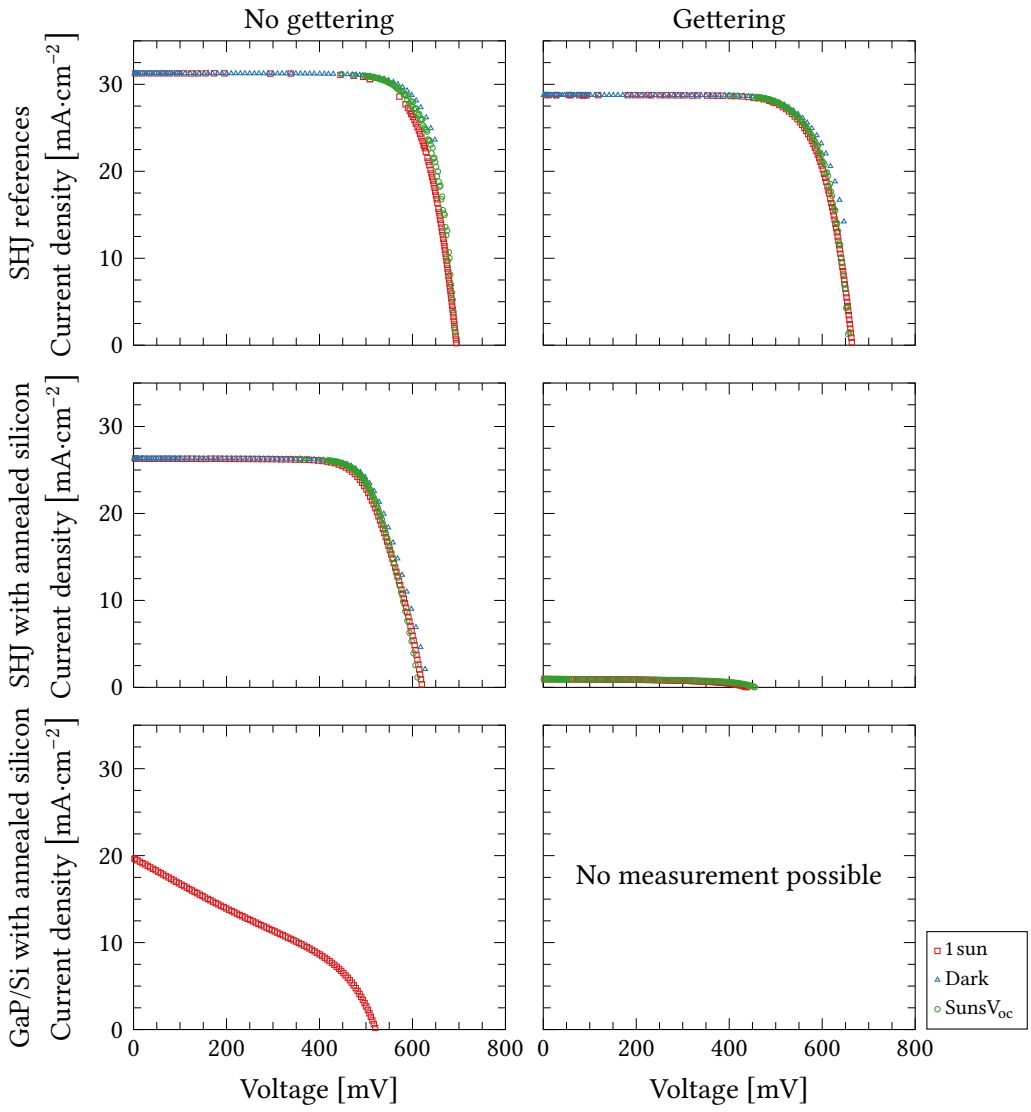

Figure V·13: J–V curves of the solar cells with SiO_x/SiN diffusion barrier for gettering determined under 1 sun illumination, dark, and by Suns-V_{oc}.

shunt [93], which reveals that the barrier was, again, not enough to protect the GaP during gettering.

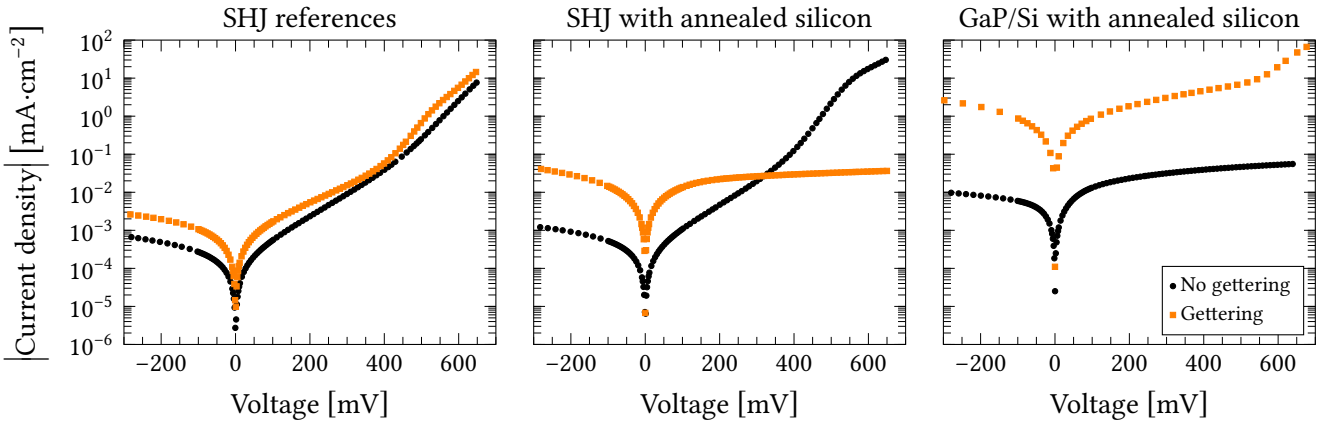

Figure V·14: Dark-J–V curves of the solar cells with SiO_x/SiN barrier.
The absolute value of current density is given, on log scale.

V·B·2·b Internal Quantum Efficiency

Optical characterization has been also performed to identify optical losses and especially recombination losses in the devices. IQE of the solar cells are shown in Figure V·15. From the SHJ solar cells, one can again observe that gettering steps restore the IQE in infrared wavelengths.

In short wavelengths, the IQE of GaP/Si solar cells is consistently below the one of the SHJ reference. This is due to the 50-nm GaP deposited in this study, which is too thick compared to the optimal thickness (10 nm) [8]. Thickness control of the GaP is hence paramount to obtain the transparency improvement over the a-Si:H layers.

The best IQE, mid-spectrum, is around 80% for the GaP/Si solar cell with annealing and gettering, instead of 100% as with the reference solar cell. This corroborates the junction shunting that was already observed by dark-I(V) and the low FF.

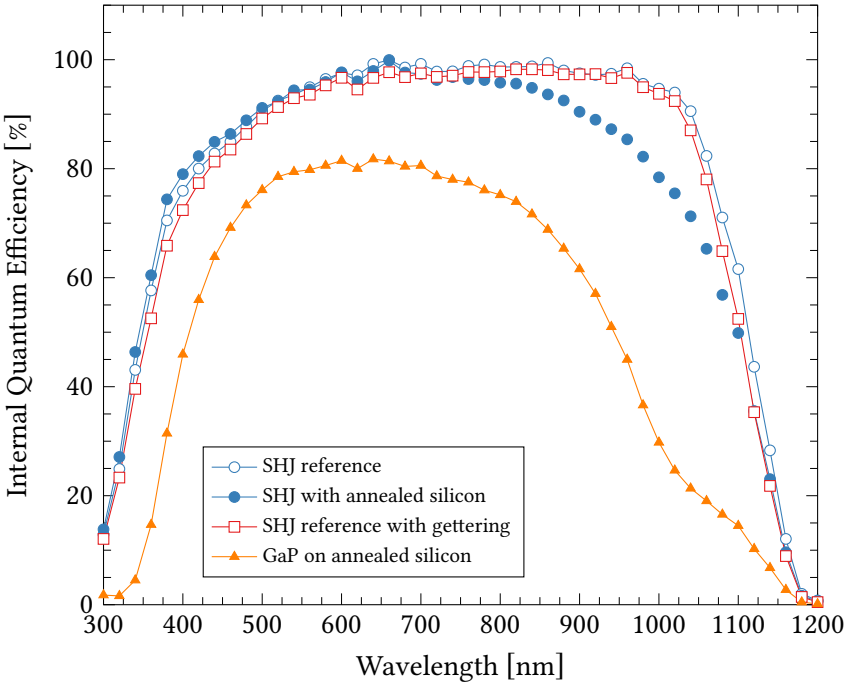

Figure V·15: Internal Quantum Efficiencies of the solar cells with SiO_x/SiN barrier. As two of the six solar cells were could not be measured due to the shunts, all IQE are plotted together.

V·B·2·c Photoluminescence

Photoluminescence pictures of the devices were taken to visualize their defects. The excitation flash is set to 1 s for all samples, which enables direct comparison of the maximum PL signal.

Gettering decreases the overall PL signal of the SHJ reference ($5 \cdot 10^4$ to $1 \cdot 10^4$ counts) and ones with annealed silicon (2500 to 2000 counts), which reveals that the gettering leaves surface or bulk defects: either decontamination is partial, or surface passivation is hindered by some leftover SiN. The solar cell with annealed silicon and gettering, from which almost no current could be extracted, has a broken busbar and wider fingers. Issues during the screen printing of the front grid may explain its almost non-existent J–V curve. Moreover, no PL response was observed (< 350 counts) from the broken solar cell, meaning that the impossibility to measure J–V is due to no passivation of the c-Si surface.

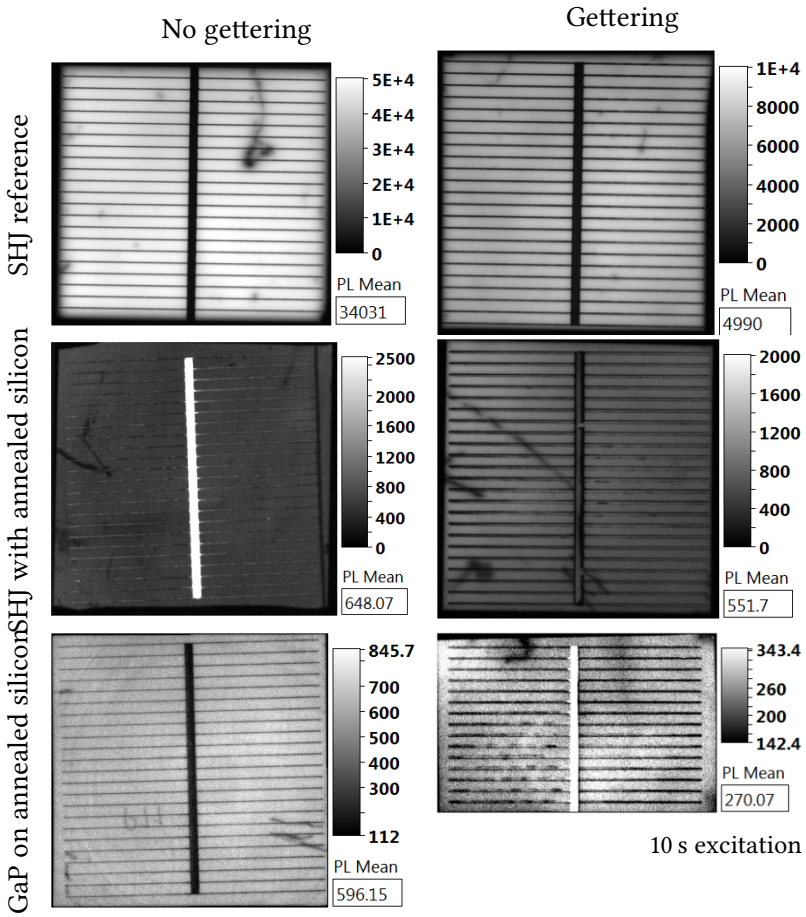

Figure V·16: Photoluminescence of solar cells from the gettering with SiO_x/SiN barrier experiment. Excitation flash is 1s for all samples, scale is adjusted to enhance contrast.

V·B·2·d Morphology of the materials before and after gettering

The SiN layer was introduced as an attempt to limit the etching of GaP during the removal of the diffusion barrier. Figure V·17 compares TEM pictures of ITO/GaP layers on annealed silicon without and with gettering steps with SiO_x/SiN diffusion barriers.

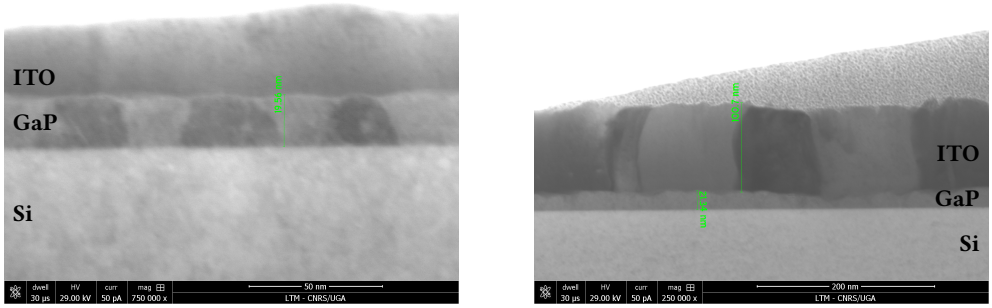

Figure V·17: Transmission Electron Microscopy of ITO/GaP/Si stack from scraps of solar cells (left) without gettering, (right) with SiO_x/SiN for gettering steps.

Without gettering the 45-nm-thick GaP is rather smooth, while displaying numerous dislocations which may explain the poor FF and current collection of the solar cell. The GaP roughness is, again, increased after gettering, with up to 13 nm loss of matter, and a comparable number of dislocations. The passivation is so poor it resulted in the low FF measured above.

One may also see some darker material between GaP and ITO and both samples, revealing that a thin SiN layer remains after its HF etching, which explains the lower V_{oc} and PL in the SHJ references with gettering.

This 13 nm loss of GaP shows that addition of the SiN layer to protect it during the barrier removal is not effective. The increase of GaP thickness, 45 instead of 10 nm, may have prevented direct contacting of ITO on silicon, but the electrical measurements have shown that the junctions were completely shorted after gettering.

V·B·2·e SIMS analysis of the solar cells

Shorted junctions may be due to inter-diffusion of Ga, P and Si due to the thermal treatments of the gettering that may smoothen the otherwise abrupt heterojunction. To determine the profiles of the elements making up the devices, SIMS has been performed on the GaP/Si cells without and with gettering. The monitored elements are: In, Sn to detect the ITO layer; Ga, P for the emitter; Si, N for the substrate; As, Zn, Se, Al, Sb, Mg, Fe to detect III-V and metallic contaminants; and B, F, S, O as other contaminants.

The profiles of the GaP/Si solar cells are plotted in Figure V·18. Aside from peaks, all data below $1 \cdot 10^2$ counts can be considered as background noise. Phosphorus and gallium seem well confined within the GaP layer. There is no carbon at the interfaces, but rather within the GaP layer due to the MOCVD method, as already seen in Chapter IV. There is no oxygen peaks at the interfaces, but the HF etching of the SiN barrier has left some fluorine on the surface of GaP. Fluorine is diffused inside the GaP layer, and carbon inside silicon after gettering. No metallic or III-V elements were detected inside the substrate. There seems to be little inter-diffusion between GaP and Si, as their profile are not quite abrupt, especially in the gettered sample.

In the cell with gettering, InO- seem to have diffused inside the substrate but this is rather an artefact of SIMS [128]. Indeed, despite the screen printing annealing (<300℃), there is no reason for indium to have diffused through GaP and into the silicon. This artefact may be due to the abrasion method that may keep detecting elements that are pulverised and fall back on the sample, or due to roughness of the abraded area which leads to the lower layers starting to be detected while some part of the upper layer are still unabraded.

Magnesium is seen at the ITO surface, but it has always been detected at the very surface of the samples analysed by SIMS for the preparation of this thesis, no matter their front material is. It is attributed to the storage and transport conditions between the two laboratories.

V·B·3 GaP on unannealed silicon and GaP as window layer

Considering that the GaP layer is strongly degraded by the decontamination steps, one may consider to completely avoid the surface reconstruction annealing. Moreover, GaP has been shown in the previous chapter not to passivate the surface of silicon. A way to improve this surface passivation is to introduce a (n+) homo-emitter inside the substrate, which reduces the GaP layer to a window layer [70]. To do so, the phosphorus pre-diffusion step is performed on the front side, then GaP is epitaxied on top of it. The resulting layer stacks of the heterojunction and “hetero-homojunction” solar cells are depicted in Figure V·19.

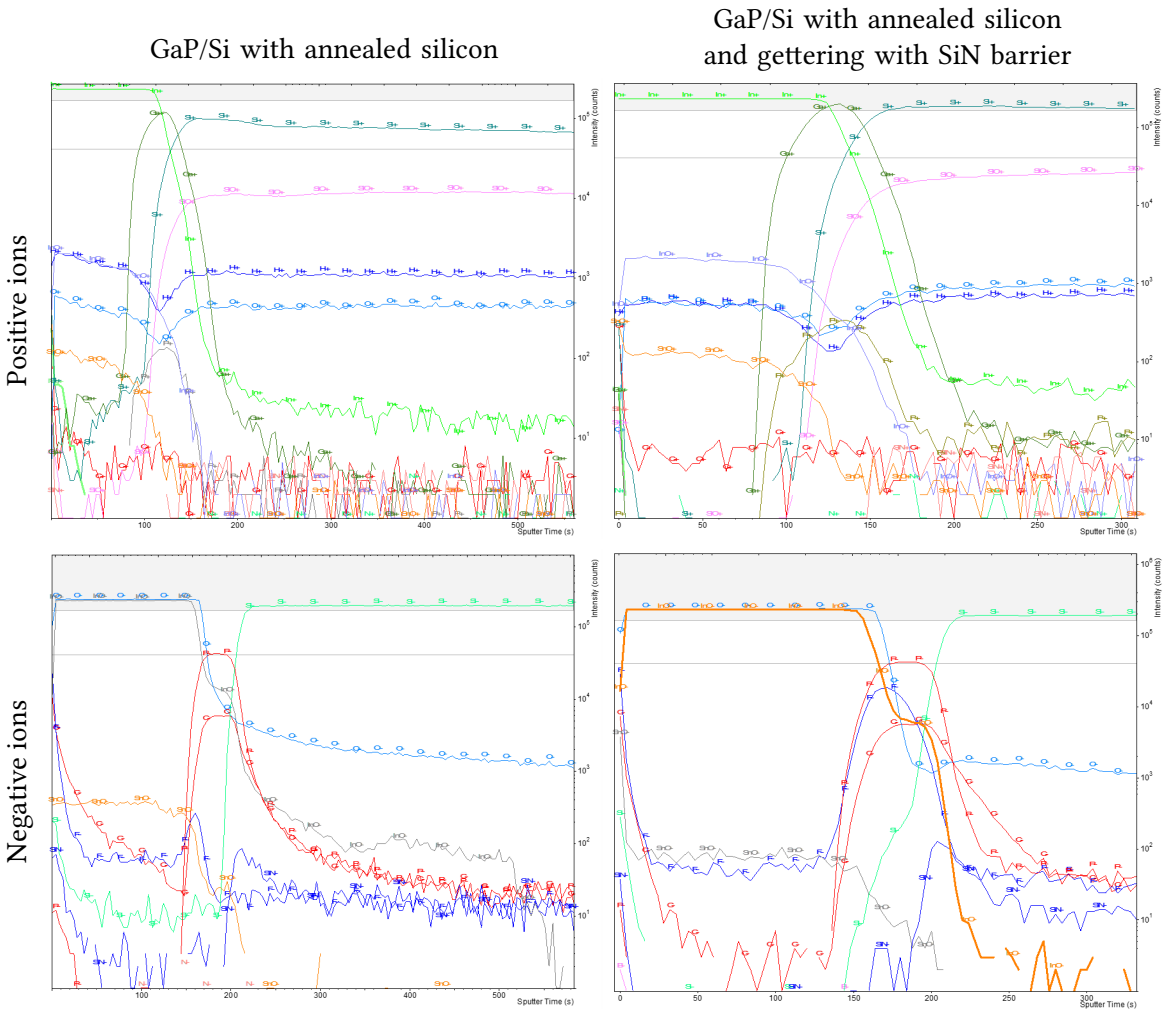

Figure V·18: Secondary Ion Mass Spectroscopy of the GaP/Si solar cell, without gettering (top) positive and (bottom) negative ion profiles.

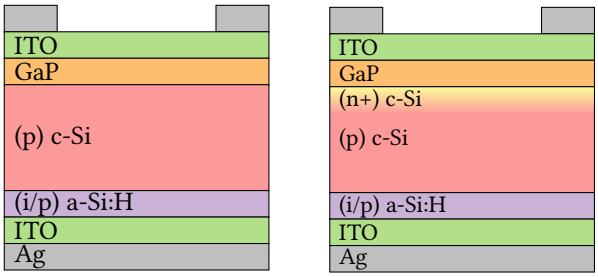

Figure V·19: Schematic drawings of (left) the heterojunction and (right) the hetero-homojunction solar cells.

V·B·3·a J–V and efficiencies

The obtained solar cells are measured under the solar simulator, and the resulting J–V curves are plotted in Figure V·20, with their electrical characteristics summarized in Table V·4. As a reference, some of the solar cells from § V·B·1 are shown again. Pseudo-performances obtained with implied-Voc from Sinton, and pseudo-J_{sc} from EQE, pseudo-FF from Suns-V_{oc} are also given in Table V·5.

First of all, we observe 50 mV decrease between the "hetero-homojunction" (HHJ) reference cell and the SHJ solar cell. Indeed, the addition of the 400-nm-deep phosphorus-doped emitter within the silicon brings also defects that limit the surface passivation by the (i) a-Si:H layer. However, V_{oc} is improved from around 520 mV in GaP/Si solar cells with heterojunction to above 600 mV with HHJ. This is close to what has been obtained by Feifel et al. [70] with 60-nm-thick GaP on 1-µm-deep homojunction. Better optimization of the HHJ, e.g. thinner doping profile, should improve the open-circuit voltage, as it was investigated by Carrere et al. [129–131] with a-Si:H/c-Si HHJ solar cells.

However, concerning the annealed c-Si substrate, the behavior is opposite, the homojunction profile improves up to values over 660 mV and the heterojunction profile decreases down to 620 mV. In this last case, we see also a good correlation with the FF behavior showing the dependence between the recombination issues impacting both V_{oc} and FF (and pFF). It is extremely important to see that the pFF obtained with the annealed substrate for the reference cells are below 74% demonstrating a recombination issue for the annealed structures, which is not the case for the GaP cells with or without annealing where this recombination seems not so critical. This shows that there are aleatory issues regarding the gettering step etching as evoked before. It is well known, that in the case of the heterojunction solar cells interface, the c-Si surface state is very critical for passivation, as the junction is done by deposition and not by diffusion [97, 131]. It means that any residual defect can degrade passivation and hinder good V_{oc} and pFF.

Current density is not affected by the HHJ process in reference cells, staying around 31 $mA{\cdot}cm^{-2}$. It gains 2.8 $mA{\cdot}cm^{-2}$ in the annealed SHJ devices, though remaining below 30 $mA{\cdot}cm^{-2}$, which can be attributed to the aleatory issues of the gettering. With GaP, current density gains 1 $mA{\cdot}cm^{-2}$ on annealed substrate, but is decreased by the alteration induced by gettering.

iV_{oc} and pV_{oc} are measured respectively after passivation a-Si:H deposition, and after metallisation. They should remain close to each other if the passivation is not affected by the ITO deposition and metallisation. However, an increase between 30 and 50 mV is observed in the SHJ solar cells with annealed silicon or with the HHJ and gettering step, which means that later steps improve either the surface or the bulk passivation. This increase is marginal in the solar cells with GaP, where the passivation is limited by the defects at the interface. The bulk passivation improvement can thus be excluded: the post-PECVD steps, most likely the annealing induced by the ITO deposition and screen printing post-annealing (both around 200°C), help to improve the hetero-homojunction. Such post-annealings were investigated by Carrere [131].

Table V·4: Performances of solar cells with homo-emitter and gettering.

Solar cell		1-sun JV			
Type	Treatment	V_{oc} [mV]	J_{sc} [mA·cm^{-2}]	FF [%]	η [%]
SHJ reference	Heterojunction	695	31.3	75.7	16.4
	Homojunction + gettering	645	31.4	77.1	15.6
SHJ with annealed silicon	Heterojunction	621	26.3	71.4	11.7
	Homojunction + gettering	665	29.1	70.9	13.7
GaP/Si with annealed silicon	Heterojunction	521	19.7	34.5	3.5
	Homojunction + gettering	605	30.1	75.9	13.8
GaP/Si with unannealed silicon	Heterojunction	518	31.3	68.8	11.2
	Homojunction + gettering	606	29.5	73.3	13.1

Table V·5: Implied-Voc, pseudo-Voc, -J_{sc}, -FF, and -efficiency of solar cells with heterojunction, and hetero-homojunction with gettering.

Solar cell		Pseudo-performances				
Type	Treatment	iV_{oc} [mV]	pV_{oc} [mV]	pJ_{sc} [mA·cm^{-2}]	pFF [%]	$p\eta$ [%]
SHJ reference	Heterojunction	703	692	34.6	78.3	19.0
	Homojunction + gettering	604	642	34.5	81.0	16.9
SHJ with annealed silicon	Heterojunction	584	616	32.0	73.8	13.8
	Homojunction + gettering	614	661	34.6	73.0	15.5
GaP/Si with unannealed silicon	Heterojunction	555	516	31.8	75.6	13.4
	Homojunction + gettering	600	604	29.8	76.9	11.3
GaP/Si with annealed silicon	Heterojunction	521	520	24.6	75.6	9.7
	Homojunction + gettering	597	603	32.2	79.1	15.2

1 sun, dark, and Suns-V_{oc} J–V curves of the SHJ reference and annealed silicon solar cells are well correlated, which confirms that the lower performances of the cells with annealed silicon are due to the recombinations and not parasitic resistances. However, with GaP and HHJ, there is a shift between illuminated and dark curves leading to $V_{oc}^{1\,sun} < V_{oc}^{dark}$ which reveals strong series resistances [92]. One can also see that both $V_{oc}^{1\,sun}$ and $V_{oc}^{Suns\text{-}V_{oc}}$ are lower than V_{oc}^{dark}, which means that light-sensitive defects are involved when the devices are operating. This confirms the defectivity of the GaP, increased by the gettering step (as seen in the V.B.3 section). The GaP on unannealed silicon solar cell even shows stronger series resistances, with the Suns-V_{oc} and dark J–V curves being above the 1 sun curve. This is confirmed with the difference between its FF (below 69%) and pFF (above 75%), discussed above.

Figure V·21 plots the dark-J–V curves of these solar cells. The HHJ process does not greatly affect the diode behaviour and the resistances of the SHJ cells with or without annealed silicon. A slight shunt is observed, and the diode behaviour remains similar. The GaP on unannealed silicon cell is greatly improved with HHJ and gettering, with much less leak current in reverse bias. Dark current is lower in direct bias: as already seen under illumination, the GaP layer is most likely degraded by the gettering. As it has been already shown, the GaP/Si solar cell is heavily shunt, with no diode behaviour. The HHJ process move the junction within the silicon cured by gettering, far from the defective GaP so that the diode shape is restored.

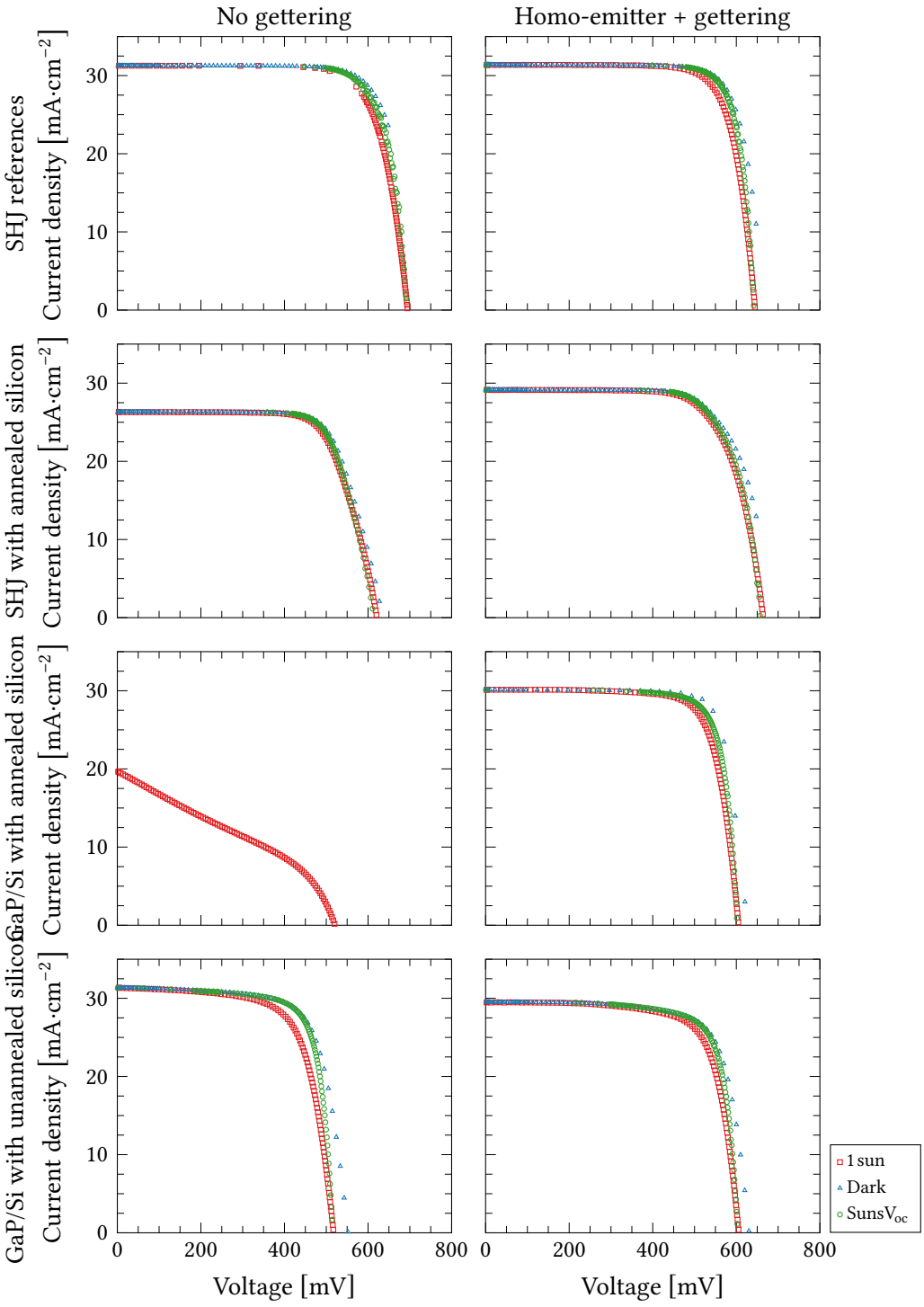

Figure V·20: J–V curves of the solar cells with homojunction and their reference heterojunction determined under 1 sun illumination, dark, and by Suns-V_{oc}.

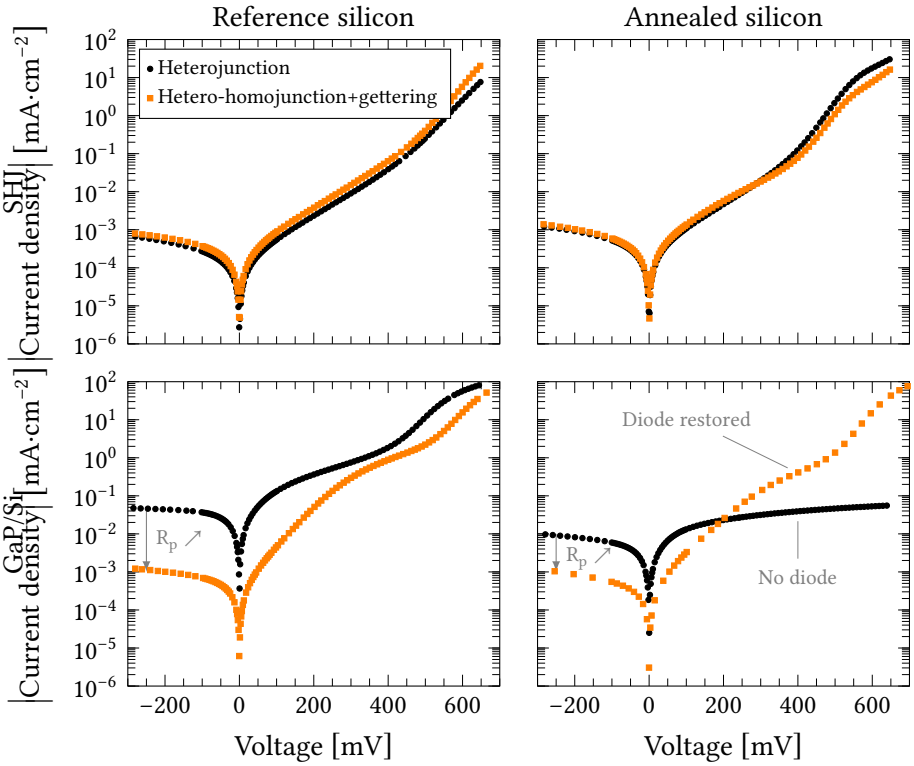

Figure V·21: Dark-J–V curves of the solar cells with heterojunction and hetero-homojunction. The absolute value of current density is given, on log scale.

V·B·3·b Photoluminescence

Defects are correlated to the passivation and V_{oc} thanks to PL pictures shown in Figure V·16. There are some recombinations due to handling marks on all cells, as in previous batches. However, maximum PL signal is again driven by bulk and surface recombinations. Mean PL for the SHJ references cell goes from to over 30 000 to below 5000 counts while in the annealed cells, on the contrary, PL signal is increased, which is outlined by the respective V_{oc} loss and increase seen by J–V measurements. If performing the HHJ and gettering steps lowers the PL signal of reference devices while it is increased in devices with annealed silicon confirms that the gettering steps does, at least partially, restore the bulk lifetime, but some SiN or the etching steps have affected the surface passivation.

The most affected cell, GaP on unannealed silicon with homo-emitter, is speckled. This may illustrate its lower IQE and current, despite its V_{oc} at 600 mV: the junction itself is not degraded by the gettering as it is within the silicon, but the GaP layer is degraded and current collection is hindered.

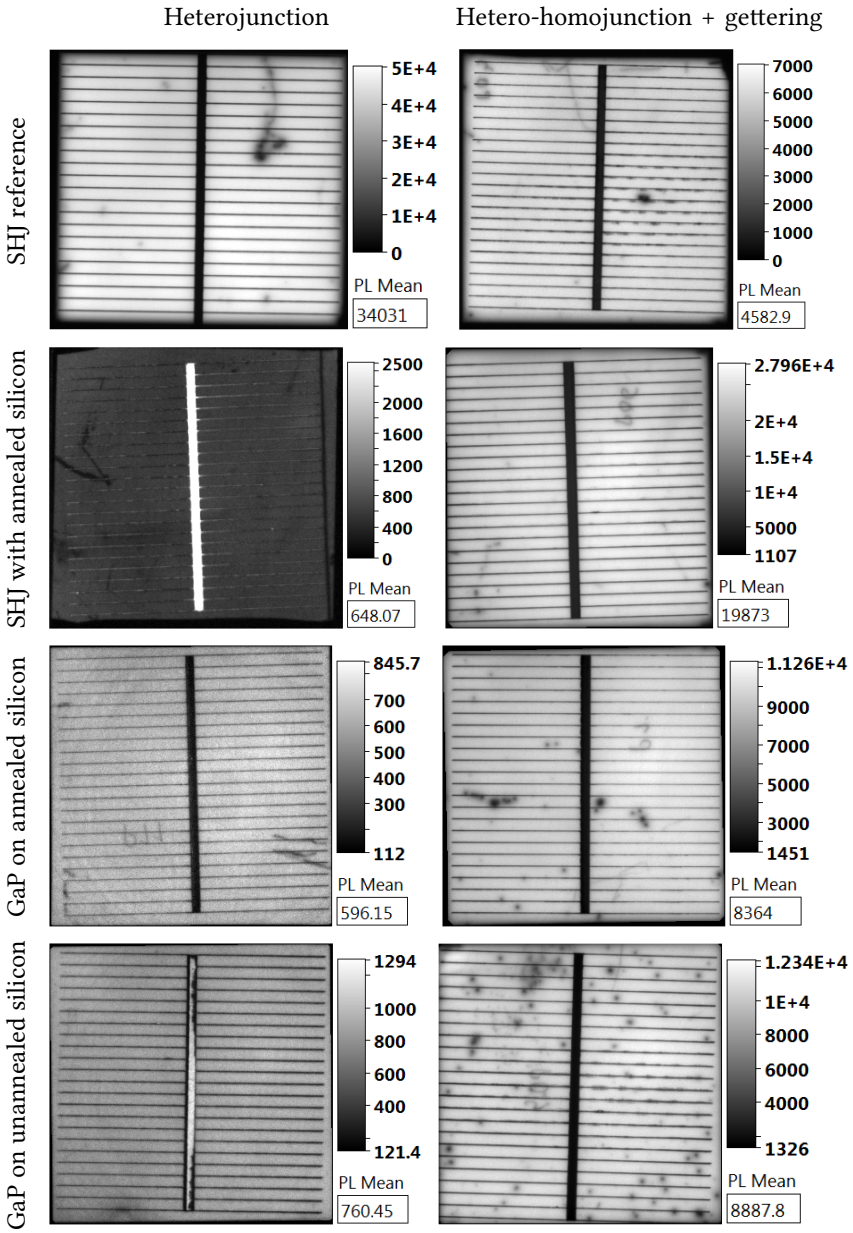

Figure V·22: Photoluminescence of solar cells from the heterojunction vs hetero-homojunction experiment. Excitation flash is 1 s for all samples, scale is adjusted to enhance contrast.

V·C Conclusion on the solar cells fabrication and their performances

In this chapter, the introduction of gettering steps to cure the degraded silicon was studied. It has been determined that gettering by phosphorus implantation, activated during the degrading annealing itself, is enough to greatly restore bulk lifetime. Using an altered phosphorus diffusion process, involving a backside pre-diffusion and actual gettering and etching after GaP epitaxy, partial recovery of the silicon bulk of precursors was achieved. More optimization, such as longer diffusion and more reproducible gettering could be achieved to reach full decontamination.

As phosphorus diffusion through the GaP layer is not wanted, diffusion barriers are needed. Initially, a SiO_x barrier was deposited on top of 10-nm-thick GaP during the gettering steps. A systematic metallisation issue prevented the J–V analysis of the solar cells. It was nonetheless determined through the IQE and the calculation of the pseudo-efficiency that GaP is etched during the SiO_x removal. GaP loss is enough to induce shunts and optical degradation.

In an attempt to protect the GaP, its thickness has been increased to 50 nm and SiN was deposited before the SiO_x barrier, but to no avail. GaP is still consumed during the barrier removal. Moreover, SiN has been proven quite difficult to remove, as a thin layer that affected the IQE and surface passivation of SHJ with annealing and gettering remained. The leak currents and passivation degradation have led to low electrical performances.

In both cases, the IQE of infrared photons is notably restored by the gettering, which shows that bulk restoration is at least partially achieved in the solar cells.

GaP/Si interface remains an issue, as its non-passivation hinders the open-circuit voltage. TEM pictures have shown crystalline defects in the GaP layer, which were not exacerbated by the thermal treatments of the decontamination steps. These defects originate from the interface, and they can participate to its low passivation.

SIMS analysis have been performed, and has revealed slight inter-diffusion between GaP and Si that may affect the junction and the interface passivation. Moreover, fluorine at the GaP surface (from the HF deoxidation step) diffuses inside GaP after gettering steps. Meanwhile, carbon within the GaP (left by the epitaxy) diffused inside the substrate. These contaminations may affect the effective passivation.

So as to improve the front surface passivation, a GaP/(n+)c-Si hetero-homojunction was introduced instead of the GaP/(p)c-Si heterojunction. The GaP on reference or annealed silicon solar cells reached around 520 mV, while with gettering - and despite the GaP degradation due to the gettering, the solar cells with GaP and HHJ reached more than 600 mV of open-circuit voltage. Improvement of this process can be made, with shallower homo-emitter and optimized post-annealing to improve surface passivation. A solar cell with GaP, annealed then decontaminated silicon, and a homo-emitter established a record of 13.8% efficiency, as of October 2017.

Conclusion and perspectives

Hydrogenated amorphous silicon has paved the way for high efficiency silicon solar cells through the development of silicon heterojunction solar cells. Its high surface passivation enables high open-circuit voltage and final solar cells efficiencies now reach 25.7% conversion efficiency. Knowing the limitations of a-Si:H, parasitic UV absorption and high resistivity, we investigated another type of front side material. Gallium phosphide is a III-V crystalline material with a high bandgap. This high bandgap, 2.26 eV vs 1.6-1.9 eV for a-Si:H, means higher transparency and higher short-circuit current for the solar cells. Moreover, bandgaps alignment predicted high hole barrier at the interface, allowing field effect passivation and higher open-circuit voltage. These improvements have led to simulations of 10-nm-thick GaP on silcion heterojunction solar cells that predicted +2% improvement of the conversion efficiency when compared to a SHJ solar cell.

First fabricated GaP/Si solar cells, compared to SHJ solar cells processed at the same time, showed photo-generated current density increased by 2 mA/cm^2, confirming the interest of using GaP as more transparent emitter. However, open-circuit voltage was strongly degraded, coming from almost 700 mV for reference heterojunction down to 520 mV for GaP on silicon. Deeper analysis has revealed two phenomena taking place in the GaP/Si solar cells that affect the minority carrier lifetime.

On the one hand, a silicon bulk degradation is brought by the surface reconstruction annealing, mandatory to assure a good epitaxy in the growth chamber. This degradation is deep, but the contaminants remain few enough not to be detected, but recombinant enough to strongly degrade the minority carrier lifetime in the exposed substrates. The use of photovoltaics characterisation techniques, such as QSSPC or µWPCD, have enabled the detection of injection-sensitive contaminants, brought in the silicon by the epitaxy chamber that would have not been noticed otherwise. Dissociation under illumination is typical of Fe-B in p-type silicon. Literature confirms the presence of iron contamination by the graphite holders coated with silicon carbide in MOCVD chambers. However, no direct detection and quantification has been successful. Simulation of the effect of such bulk contamination on the quantum efficiency was also not in agreement with the resulting lifetime. However, surface reconstruction annealing in clean, dedicated chambers has been demonstrated and preserve bulk lifetime.

To cure the affected solar cells from the degradation, gettering steps were introduced in the process flow. These high temperature diffusion steps may not be industrially viable, but they enable almost complete bulk lifetime restoration. However, when performed on solar cells

precursors with GaP, the combination of deposition of diffusion barriers, their removal, and temperature treatment have led to GaP etching. The partial loss of the thin emitter due to gettering leads to shunts, optical degradation and passivation degradation, lowering the solar cells performances instead of enhancing them.

On the other hand, GaP itself does not passivate the surface of crystalline silicon. The surface reconstruction annealing helps reducing the density of antiphase boundaries, known defects that emerge due to the polarity of III-V materials. Even though it is difficult to decorrelate the low surface lifetime and contaminated bulk lifetime, it has been shown that other defects take place at the interface. Indeed, GaP deposited on unannealed silicon also results in high surface recombination velocities due to crystalline defects, such as dislocations and dangling bonds that hinder the field effect passivation. Moreover, minute amounts of arsenic and antimony were found by XPS, most likely traces from the epitaxy chamber, as well as carbon from the epitaxy precursors. The n-type character of GaP was confirmed with the presence of silicon in the layers, also seen by SIMS that also detected fluoride from the silicon deoxidation steps. Surface contamination of GaP was also seen, with strong presence of carbon on samples exposed to air, as well as oxidation that affected whole of our thinnest layers. Such contamination may explain the low passivation of the substrate by our GaP. Other deposition techniques, such as PE-ALD, have shown elsewhere to enhance interface passivation, but remain too low for suitable heterojunction solar cells fabrication.

To enhance the GaP/Si interface passivation, different wetting epitaxial layers, were investigated. Even though little to no improvement were found, correlation between surface reconstruction, low roughness and higher effective lifetime has been established. To prevent interface recombination, GaP was used as a window layer grown on a silicon homojunction. Even though the homo-emitter was no particularly optimised, such GaP as a window layer on polished silicon has led to a 13.8% efficiency solar cell that is, at the extent of our knowledge, a record as of October 2017.

To summarise, we have fabricated GaP/Si solar far less efficient from what was expected from previous simulations. A systematic bulk contamination introduced by the surface reconstruction annealing of silicon, widely observed across the literature, hinders the efficiency of the solar cells. Gettering steps, designed to successfully restore bulk lifetime, also degrade the thin GaP layer. Whereas dislocation and antiphase boundaries could be avoidable with optimised processes, GaP itself does not passivate silicon. It was shown that strong oxygen contamination occur across the epitaxial layers exposed to air, and accumulation of defects such as dangling bonds, remaining unpassivated by different wetting layers, maintain low interface lifetime. To accommodate such low passivation, the PN junction was moved within the silicon substrate thanks to a homo-emitter onto which is grown the GaP as a window layer. Such structure, combined with the gettering steps, has produced a 13.8% efficient polished solar cell, a record so far for similar GaP/Si structures.

Despite silicon photovoltaics having inherited from microelectronics advancements, this thesis has emphasised one crucial difference between their quality requirements. Indeed, even though materials for microelectronics devices can have their crystalline defects buried under the bulk

of epitaxial layers, or trapped thanks to original designs, these techniques cannot be allowed for photovoltaics. Indeed, efficient solar devices need the whole of bulk and layers to generate the charge carriers and keep them as long as possible for them to be extracted and generate power. This means that the epitaxy of III-V materials on silicon need to be as little defective as possible, as soon as the first atoms are deposited, which is quite a challenge. Passivation of silicon by GaP has been shown not to be as simple as "no crystalline defects means better passivation". Dangling bonds and defects remain at the interface or near it, which affect the passivation despite no visible crystalline defects result from them. Moreover, epitaxial layers are not compatible to high temperature treatments after epitaxy, such as gettering, and bulk degradations need to be avoid at all cost. These works contribute to the understanding of the potentials and limitations of GaP/Si solar cells, which may be extended to all III-V materials grown on silicon intended for photovoltaic applications.

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Fabrication et caractérisation de cellules photovoltaïques à base de phosphure de gallium sur silicium

Dans le cadre de la transition énergique, le déploiement de sources d'énergies ne produisant pas de gaz à effet de serre devient primordial. Bénéficiant de la surabondante énergie fournie par le Soleil, le photovoltaïque est un des éléments-clés du bouquet énergétique du futur. Le marché du photovoltaïque est actuellement dominé par les technologies à base de silicium et les meilleurs rendements de conversion dépassent les 26% avec la technologie de cellules à hétérojonction de silicium amorphe hydrogéné (a-Si:H) sur silicium monocristallin (c-Si).

Le silicium amorphe hydrogéné, déposé par PECVD, permet d'obtenir une excellente passivation de la surface du substrat de silicium cristallin, et ainsi d'obtenir des tensions de circuit ouvert au-delà de 730 mV. Cependant l'a-Si:H montre une absorption parasite des photons ultraviolets, et sa faible conductivité limite la longueur de diffusion des porteurs de charge générés en son sein, limitant la performance électrique et aussi leur contribution au courant de la cellule.

Pour augmenter le rendement de cette technologie, nous proposons de fabriquer et de caractériser une nouvelle structure de cellules photovoltaïques à base d'hétérojonction de phosphure de gallium (GaP) sur c-Si, déposé par dépôt en phase vapeur aux organométalliques (MOCVD). Matériau III-V, cristallin, et à énergie de bande interdite élevée (2.26 eV contre 1.6–1.9 eV pour l'a-Si:H et 1.12 eV pour le c-Si), le GaP permettrait une croissance par épitaxie sur le c-Si, une meilleure transparence face à l'a-Si:H, ainsi qu'une passivation par effet de champ repoussant les trous, porteurs de charge positive, loin de l'interface GaP/Si. Les améliorations des caractéristiques courant-tension de telles cellules avec seulement 10 nm de GaP ont précédemment montré, par simulation, une amélioration des rendements de 2% en absolu.

Dans le cadre de cette thèse, nous avons étudié expérimentalement l'effet du dépôt de GaP sur le c-Si. Nous avons mis en évidence une dégradation de la durée de vie des porteurs dans le c-Si lors d'une étape de préparation de surface pour améliorer l'épitaxie du GaP, qui favoriserait la diffusion de contaminants issus de la chambre de dépôts III-V dans le substrat. Cette étape pourrait être retirée, mais elle est nécessaire pour limiter l'émergence de domaines d'antiphase, défauts cristallins liés à la nature polaire des liaisons Ga-P qui limitent aussi la durée de vie des porteurs. De plus, la durée de vie à l'interface GaP/Si est demeure inférieure à 150 µs, malgré l'hypothétique passivation par effet de champ et sans défauts cristallins.

Se basant sur ces découvertes, nous avons cherché à comprendre et améliorer la passivation de l'interface GaP/Si. Des techniques d'analyses avancées ont montré la présence de traces de carbone et d'arsenic dans le GaP, accompagné de fluor à l'interface, ainsi qu'une oxydation du GaP post-épitaxie. Différentes couches de mouillage ont été testées, permettant de corréler la rugosité, la défectuosité du GaP à la durée de vie des porteurs.

D'autre part, l'intégration d'étapes de décontamination du substrat (gettering) a permis avec succès de restaurer la durée de vie volumique des charges tout en maintenant le recuit de reconstruction de surface dans le procédé de fabrication. Ces étapes ont été optimisées pour minimiser leur impact sur la couche de GaP. Un cellule avec GaP déposé sans pré-recuit atteint 11.2% tandis qu'en reléguant le GaP à une couche fenêtre, une cellule GaP/(n+)c-Si/(p)c-Si a montré un rendement amélioré à 13.8% avec le recuit et les étapes de gettering.

Ce travail s'appuie sur l'expertise du CEA-INES en cellules solaires à hétérojonctions et du CNRS-LTM en épitaxie et caractérisation des matériaux III-V.

Fabrication and characterisation of photovoltaic solar cells made of gallium phosphide on silicon

In the frame of energy transition, the development of energy sources that do not generate greenhouse gases is paramount. Benefiting from the overabundant energy provided by the Sun, photovoltaics is a key element of the future energy mix. Photovoltaics market is currently led by the silicon-based technologies, and best conversion efficiencies exceed 26% with the heterojunction solar cells technology with hydrogenated amorphous silicon (a-Si:H) on monocrystalline silicon (c-Si).

Hydrogenated amorphous silicon, deposited by PECVD, enables high surface passivation of crystalline silicon, and to reach over 730 mV of open-circuit voltage. However, the parasitic absorption in the ultraviolet region limits photon collection, and its low conductivity limits the diffusion length of charge carriers it generates, limiting the electrical performance and their contributions to the cell current.

To enhance the efficiency of this technology, we propose to fabricate and characterise a new structure of photovoltaic solar cells based on heterojunction of gallium phosphide on crystalline silicon, made by metalorganic chemical vapour deposition (MOCVD). This crystalline III-V material, with high bandgap energy (2.26 vs 1.6–1.9 eV for a-Si:H and 1.12 eV for c-Si), allows its pseudomorphic epitaxy on silicon, with higher transparency vs a-Si:H along with field effect passivation that repels the holes, positive charge carriers, away from the GaP/Si interface. The improvement of current-voltage characteristics, with only 10-nm-thick GaP, have previously shown by simulation an absolute improvement of the efficiency by 2%.

In the frame of this thesis, we have experimentally studied the effect of GaP deposition on c-Si. We have outlined a carrier lifetime degradation in c-Si during a surface preparation annealing that favours the diffusion of contaminants from the III-V MOCVD chamber into the substrate. This step could be removed, but it is required to limit the formation of antiphase domains, which are crystalline defects linked to the polarity of Ga-P bonds that also limit the carrier lifetime. Moreover, GaP/Si interface lifetime remains below 150 µs, despite the hypothetic field effect passivation and without crystalline defects.

From these conclusions, we sought to understand and improve the GaP/Si interface passivation. Advanced analysis techniques have shown carbon and arsenic traces in the GaP, with fluorine at the interface, as well as post-epitaxy GaP oxidation. Different wetting layers were tested, correlating the roughness and defectivity of Gap to the carrier lifetime.

Furthermore, integration of substrate decontamination steps (gettering) enables successful bulk carrier lifetime recovery while maintaining the surface reconstruction annealing in the process flow. These steps were optimised to minimise their impact the GaP layer. A solar cell with GaP deposited on unannealed silicon reached 11.2% while, making GaP a window layer in a GaP/(n+)c-Si/(p)c-Si stack produced a solar cell with 13.8% with annealing and gettering steps.

This work relies on the expertise of CEA-INES on heterojunction solar cells and CNRS-LTM on III-V materials epitaxy and characterisation.