



**HAL**  
open science

# Investigation of HfO<sub>2</sub> based Resistive Random Access Memory (RRAM): characterization and modeling of cell reliability and novel access device

Mouhamad Alayan

► **To cite this version:**

Mouhamad Alayan. Investigation of HfO<sub>2</sub> based Resistive Random Access Memory (RRAM): characterization and modeling of cell reliability and novel access device. Micro and nanotechnologies/Microelectronics. Université Grenoble Alpes, 2018. English. NNT: 2018GREAT032 . tel-01884491

**HAL Id: tel-01884491**

**<https://theses.hal.science/tel-01884491>**

Submitted on 1 Oct 2018

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

## **THÈSE**

Pour obtenir le grade de

### **DOCTEUR DE LA COMMUNAUTE UNIVERSITE GRENOBLE ALPES**

Spécialité : **NANO ELECTRONIQUE NANO TECHNOLOGIE**

Arrêté ministériel : 25 mai 2016

Présentée par

**Mouhamad ALAYAN**

Thèse dirigée par **Barbara DE SALVO, DR., CEA-Leti**, et  
codirigée par **Luca LARCHER, Prof., Università di Modena e  
Reggio Emilia, Italie**

préparée au sein du **Laboratoire composants mémoires au  
CEA-Leti**  
dans **l'École Doctorale EEATS**

## **Étude des mémoires résistives (RRAM) à base d'HfO<sub>2</sub> : caractérisation et modélisation de la fiabilité des cellules mémoire et des nouveaux dispositifs d'accès (sélecteurs)**

Thèse soutenue publiquement le **24 avril 2018**,  
devant le jury composé de :

**Mr Abdelkader SOUIFI**

Prof., Institut des Nanotechnologies de Lyon, Rapporteur

**Mr Marc BOCQUET**

Dr., HDR, IM2NP, Marseille, Rapporteur

**Mr Gérard GHIBAUDO (Président de jury)**

Directeur de Recherche, IMEP-LAHC, Grenoble

**Mme Barbara DE SALVO**

HDR, Dr. Ing. CEA-Leti Grenoble, Directeur de thèse

**Mr Luca LARCHER**

Prof., Università di Modena e Reggio Emilia, Italie, Co-directeur de thèse,  
invité

**Mme Elisa VIANELLO**

Dr. Ing. CEA-Leti, Grenoble, Encadrant de thèse, invitée





# Acknowledgements

At this stage, my Ph.D. journey comes to its end. Taking this opportunity, I would like to thank all the people who supported me during the past three years in my professional life at CEA-Leti as well as my personal life at Grenoble. You'd made this period one of my best memories that I will never forget.

First of all, I would like to express my gratefulness to my thesis director Dr. Barbara De Salvo for her great guidance and support during my Ph.D. She's got a strategic vision for the future work at the same time she was involved in the technical details. The meetings with her were essential to review my progress as well as to clearly define the future work and timelines. Big thanks Barbara!

Dr. Elisa Vianello, my daily supervisor, she deserves a special thank. She trusted, supported and advised me during the past three years. She always put a positive pressure that led definitely to very rigorous work. To be honest, she provided me with all possible resources she could offer. I am absolutely lucky that I had a supervisor like her. Enormous thanks Elisa!

This thesis was in collaboration with Pr. Luca Larcher from university of Modena (UNIMORE)-Italy. Despite the geographical separation, Pr. Luca was extremely active so we could arrange almost weekly meetings by phone during these three years. I appreciate the hard work that Pr. Luca provided for this Ph.D. In addition, Pr. Luca hosted me in Italy for six months. It was an amazing and fruitful experience for me. I would like to give a particular thank to the stuff who supported me in Italy during this period: Andrea Padovani, Francesco Maria Puglisi, Luca Vandelli, Gabriele Sereni, Matteo Bertocchi and Paolo La Torraca. Thank you all for your great hospitality!

I would like to express my gratitude to the former head of memory components laboratory (LCM), Dr. Luca Perniola as well as for the current director Dr. Etienne Nowak for their support and encouragement especially to the Ph.D. students in the laboratory. A huge thank to my LCM colleagues with whom I spent great time: Gabriel Molas, Eric Jalaguier, Gabriele Navarro, Véronique Sousa, Alain Persico,

Christelle Charpin, Sophie Bernasconi, Carine Jahan, Laurent Grenouillet, Cathérine Carabasse, Jean-François Nodin, Guillaume Bourgeois.

Big thanks to Mmes. Sabine Révol and Brigitte Gaillard for solving always our administrative stuff with a big sense of humor.

My best moments in LCM were with other Ph.D. students and postdocs. I will miss you all guys, thanks for these amazing three years that I had spent with you: Mourad Azzaz, Luc Tillie, Anthonin Verdy, Rana Alhalabi, Cécile Nail, Boubacar Traoré, Thilo Werner, Julia Kluge, Marios Barlas, Maria Riquez Moreno, Daeseok Lee, Diego Alfaro Robayo, Gilbert Sassine, Selina La Barbera, Denys Ly, Adam Dobri, Jérémy Guy, Khalil El Hajjam, Amine El Kacimi, Ilias Nifa, Clément Nguen, Alexandre Levisse, Athanasios Kiouseloglou, Daniele Garbin, Marinela Barci, Thomas Cabout, Sara Souiki, Martin Coue and all those people that I may have forgotten in this list.

I would like to thank the people of LCTE and especially: Niccolo Castellani, Alain Lopez, Jacques Cluzel, Denis Blachier, Carlo Cagli and Jean Coignus.

Special thanks to all the collaborators that made this a successful work: Marta Bagatin, Simone Gerardin and Alessandro Paccagnella from university of Padova-Italy. I also thank Philippe Blaise and Benoît Sklénard from simulation and Modeling Lab in Leti as well as Olivier Thomas and Bastien Giraud from Leti-DACLE. Special thanks also for Jean-Michel Portal from Aix-Marseille University.

I am grateful to all my Lebanese friends, thanks for sharing an amazing time together in France. A special thanks to my roommate Dr. Ali Hallal. A big thanks to Dr. Hussein Hijazi my roommate as well as my English assistant and my cooking buddy.

I address my sincere apologies and thank to everybody helped me and I forgot to mention.

My deepest thanks belong to my family members for their great support and advices.

*Finally, I would like to offer this modest work as a token of appreciation and loyalty to the martyr's families in Lebanon, who died when they were fighting against terrorist as well as who died during terrorist attacks in Lebanon in France and around the world. Thanks to their sacrifices, my family and my friends are all safe*

*today in a very hot region (in Lebanon), my friends and I are safe in France as well.  
Therefore, they strongly deserve to remember them forever...*

Mouhamad Alayan  
January 2018  
Grenoble-France

# Abbreviations

Acronym	Description
NVM	Non-Volatile Memory
RAM	Random Access memory
DRAM	Dynamic Random Access Memory
SRAM	Static Random Access Memory
RRAM	Resistive Random Access Memory
PCM	Phase Change Memory
STT-MRAM	Spin Transfer Torque Magnetic Random Access Memory
CBRAM	Conductive Bridge Random Access Memory
FeRAM	Ferroelectric Random Access Memory
VRRAM	Vertical Resistive Random Access Memory
NAND	Not AND digital logic
NOR	Not OR digital logic
SCM	Storage Class Memory
1T1R	One-Transistor One-Resistor
1T1C	One-Transistor One-Capacitor
1S1R	One-Selector One-Resistor
HRS	High Resistance State
LRS	Low Resistance state
I-V	Current-Voltage
$R_{OFF}$	OTS resistance in its OFF mode
$R_{ON}$	OTS resistance in its ON mode
$R_{ext}$	External series resistance
TMO	Transition Metal Oxide
CMOS	Complementary Metal Oxide Semiconductor
F	Feature size
FAST	Field Assisted Superlinear Threshold
MIEC	Mixed-Ionic-Electron Conduction
MIM	Metal-Insulator-Metal
MIT	Metal Insulator Transition
NLF	Non-Linearity Factor
OTS	Ovonic Threshold Switching
PVD	Physical Vapor Deposition

ALD	Atomic Layer Deposition
CVD	Chemical Vapor Deposition
TEM	Transmission Electron Microscopy
TDDDB	Time Dependent Dielectric Breakdown
TAT	Trap-Assisted Tunneling
SRC	Self-Rectifying Cell
TRIM	Transport of Ions in Matters
Vo	Oxygen vacancy

---

# List of Symbols

Symbol	Description	Unit
$V_f$	Forming voltage	V
$V_{Set}$	Set voltage	V
$V_{Reset}$	Reset voltage	V
$V_{read}$	Read voltage	V
$K$	Dielectric constant	-
$P_0$	Molecular dipole moment	e-Å
$E_a$	Activation energy to break a bond at zero field	eV
$e_a$	Activation energy of LRS failure	eV
$K_B$	Boltzmann's constant	eV. K <sup>-1</sup>
$G$	Generation rate of oxygen vacancy/ion pairs	Hz
$G_0$	Effective vibration frequency	Hz
$F$	Electric field	MV/Cm
$T$	Temperature	°C
$E_{aeff}$	Effective activation energy required to break a bond in the presence of electric field	eV
$V_{hold}$	Holding voltage	V
$V_{hold}^+$	Holding voltage positive polarity	V
$V_{hold}^-$	Holding voltage negative polarity	V
$I_{hold}$	Holding current	A
$I_{hold}^+$	Holding current positive polarity	A
$I_{hold}^-$	Holding current negative polarity	A
$V_{th}$	Threshold voltage	V
$V_{th}^+$	Threshold voltage positive polarity	V
$V_{th}^-$	Threshold voltage negative polarity	V
$I_{prog}$	Programming current	A
$I_{Reset}$	Reset current	A
$I_{HRS}$	Read current level in HRS state	A
$V_{1R}$	Voltage drop on 1R element of 1S1R device	V
$V_{1S}$	Voltage drop on 1S element of 1S1R device	V
$V_{1S1R}$	Voltage drop on 1S1R device	V
$V_{STOP}$	Negative voltage applied during Reset operation	V

# Contents

<b>Acknowledgements.....</b>	<b>I</b>
<b>Introduction.....</b>	<b>- 1 -</b>
1.1 Memory market .....	- 1 -
1.2 Memory hierarchy .....	- 2 -
1.2.1 Storage Class Memory (SCM) .....	- 3 -
1.3 Overview of memory technologies.....	- 4 -
1.3.1 Volatile memories.....	- 4 -
1.3.2 Non-volatile memories .....	- 5 -
1.4 Emerging memories.....	- 7 -
1.4.1 Ferroelectric Memories (FeRAM) .....	- 7 -
1.4.2 Magnetic Memories .....	- 8 -
1.4.3 Phase change memories .....	- 9 -
1.4.4 Resistive Random Access Memories (RRAMs).....	- 10 -
1.4.5 RRAM key performances and reliability .....	- 15 -
1.5 Emerging memories architectures .....	- 19 -
1.5.1 3D Cross point architecture .....	- 19 -
1.5.2 VRRAM architecture .....	- 20 -
1.5.3 Sneak path current issue in RRAM arrays .....	- 20 -
1.6 Access devices for RRAM arrays (selectors) .....	- 21 -
1.6.1 Requirements for access devices.....	- 22 -
1.6.2 Types of selector devices .....	- 24 -
1.6.3 Selectors benchmarking .....	- 33 -
1.7 Thesis content overview .....	- 34 -
1.7.1 Thesis objectives.....	- 34 -
1.7.2 Thesis outline .....	- 34 -
1.8 References.....	- 36 -

<b>Characterization and modeling of HfO<sub>2</sub> based RRAM cells ...</b>	<b>- 43 -</b>
2.1 Introduction .....	- 43 -
2.2 Process details .....	- 43 -
2.2.1 Memory structure.....	- 43 -
2.2.2 Integration flow .....	- 44 -
2.3 Electric test methodology of a memory cell .....	- 45 -
2.3.1 Cells programming with ramped voltage .....	- 45 -
2.3.2 Read operation.....	- 46 -
2.3.3 Cells programming in pulse mode .....	- 47 -
2.4 Modeling and simulation.....	- 48 -
2.4.1 Ginestra model .....	- 49 -
2.4.2 Thermochemical model .....	- 51 -
2.4.3 TDDDB measurements .....	- 51 -
2.4.4 Simulation results .....	- 54 -
2.5 Conclusion.....	- 59 -
2.6 References.....	- 60 -
<b>Reliability of HfO<sub>2</sub> based RRAM cells.....</b>	<b>- 61 -</b>
3.1 Introduction .....	- 61 -
3.2 Data retention improvement.....	- 62 -
3.2.1 Samples description with different Al incorporation methods .....	- 62 -
3.2.2 Materials properties .....	- 63 -
3.2.3 Forming voltage.....	- 64 -
3.2.4 Data retention .....	- 67 -
3.2.5 Data retention/ forming trade-off .....	- 70 -
3.3 Forming simulation .....	- 71 -
3.4 Radiation immunity .....	- 75 -
3.4.1 Experiment and devices .....	- 75 -
3.4.2 Experimental results.....	- 75 -
3.4.3 Mechanisms and simulation .....	- 80 -

3.5	Conclusions .....	- 87 -
3.6	References .....	- 89 -

**Access devices for HfO<sub>2</sub> based RRAM .....** - 91 -

4.1	Introduction .....	- 91 -
4.2	Oxide tunnel barrier .....	- 92 -
4.2.1	RRAM samples .....	- 92 -
4.2.2	Set processes .....	- 93 -
4.2.3	Modeling and simulation .....	- 95 -
4.2.4	Operating regions .....	- 96 -
4.2.5	Self-rectifying behavior and LRS selectivity .....	- 98 -
4.2.6	Multilevel resistance for neuromorphic systems .....	- 100 -
4.3	OTS based access device .....	- 102 -
4.3.1	1S1R: device structure and material characterization .....	- 102 -
4.3.2	Measurements Setup .....	- 103 -
4.3.3	RRAM memory cell (1R) characteristics .....	- 104 -
4.3.4	Selector device (1S) characteristics .....	- 106 -
4.3.5	1S1R characteristics (Forming/Reset/Set) .....	- 107 -
4.3.6	1S1R Read strategy .....	- 110 -
4.3.7	Selectivity for cross-point architecture .....	- 116 -
4.3.8	Voltage drop across metal lines .....	- 119 -
4.4	OTS Vs Tunnel barrier .....	- 120 -
4.5	Conclusion .....	- 121 -
4.6	References .....	- 123 -

**Summary and perspectives .....** - 125 -

5.1	Ph.D. summary .....	- 125 -
5.2	Perspectives .....	- 130 -

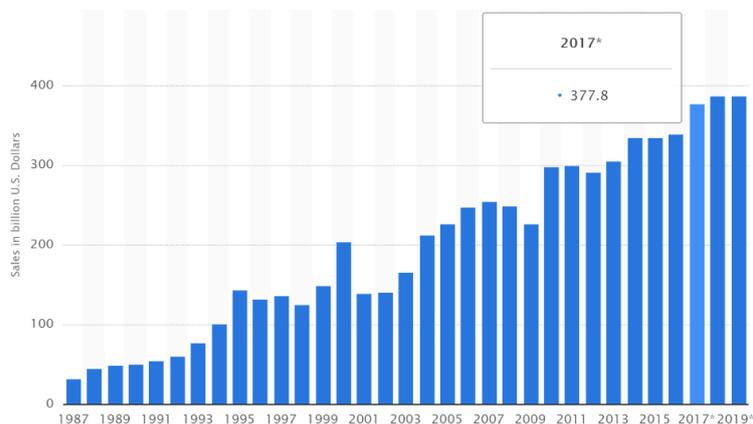
<b>Abstract .....</b>	<b>154</b>
<b>Résumé .....</b>	<b>156</b>

# Chapter 1

## Introduction

### 1.1 Memory market

**E**lectronic technologies are present in most of our daily life, starting from mobile phones, computers, connected objects etc. Semiconductor industry has been dramatically developed since the 1980s due to the increasing number of users demanding always new applications. This market has become huge, growing to more than \$370 billion in 2017 as shown in Figure 1. 1. Microelectronic industry always followed a simple creed: “smaller, faster and cheaper”, thanks to the technology integration, it is possible today to cover consumer’s requests by offering high performance products with acceptable costs.



*Figure 1. 1: Semiconductor sales revenue worldwide from 1987 to 2019 (in billion U.S. dollars)*

Permanent and temporary data storage is required in any data processing system. Semiconductor solid state memories constitute an essential part of a large number of electronic systems and applications. Requirements in terms of data storage were

fulfilled by CMOS-based technology memories, i.e. Flash, DRAM and SRAM memories [1]. The present mobile market imposes severe performance and power constraints, thus demanding ultra-low power, high-density and low-cost data storage media. The memory market is mainly dominated by Flash memory [2] , which is Non Volatile Memory (NVM), and by DRAM and SRAM [1], [3], [4] memories, which are the volatile memories essential in computer systems.

## 1.2 Memory hierarchy

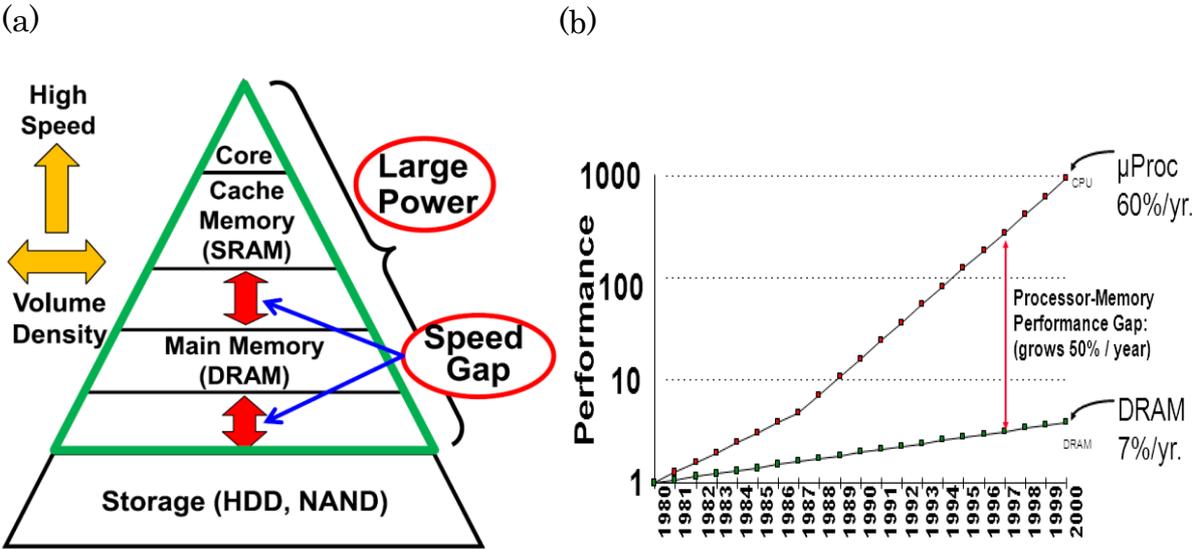


Figure 1. 2 : (a) Memory hierarchy in computer systems (reprinted from[5]). (b) Processor - Memory performance gap (Adopted from Berkley education)

The memory hierarchy pyramid-like structure is shown in Figure 1. 2 - (a). Starting from top to bottom, the memory in the processing core is based on ultra-high-speed devices with small density, such as registers and flip-flops. The cache memory and the main memory for storage of instructions to be executed and data being processed are covered by SRAM and DRAM devices, respectively. Hard Disc Drive (HDD) and NAND flash are used as mass storage parts for both instruction/programs and data. High speed operations are required from devices located close to the processors, whereas high density is required when the memory is more distant from the processor.

Major problems in today’s data-intensive applications could be summarized as follow:

- Exponentially growing gap between processor and memory in terms of capacity and speed (Figure 1. 2 - (b)).
- Speed gap between cache memory and main memory.
- Speed gap between main memory and storage memory.
- High power consumption of the core, the cache and the main memory because they are based on volatile memory technologies [6], [7].

### 1.2.1 Storage Class Memory (SCM)

The concept of Storage Class Memory (SCM) has been introduced as a solution to mitigate the memory bottleneck by filling the performance gap that exists today between the main memory and the storage in the memory hierarchy (see Figure 1. 3). Today the NAND flash can provides high density thanks to device scaling. However the performance gap still exists between memory and storage in addition to the intrinsic limitations of flash memory (e.g. limited endurance, scaling limits, etc. ) [8]. In one hand, emerging SCM class will be used to match the characteristics of fast memory-type (e.g. DRAM) with non-volatility and low cost, on the other hand SCM will be used to match the characteristics of storage-type (e.g. NAND flash) with much better performances. By definition SCMs are typically non-volatile memories, so they have the advantage of zero standby power consumption while maintain the data [9][10]. The SCM is probably the most important market for the emerging memory technologies in development.

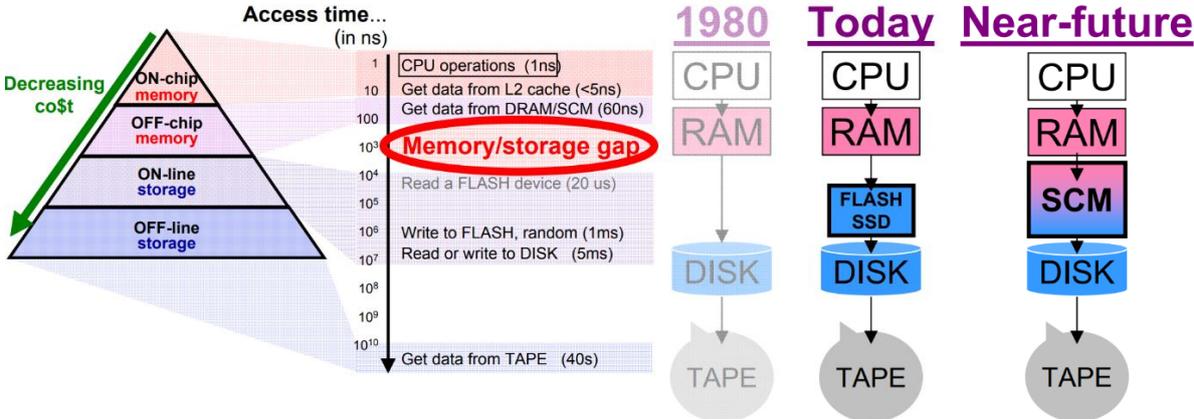


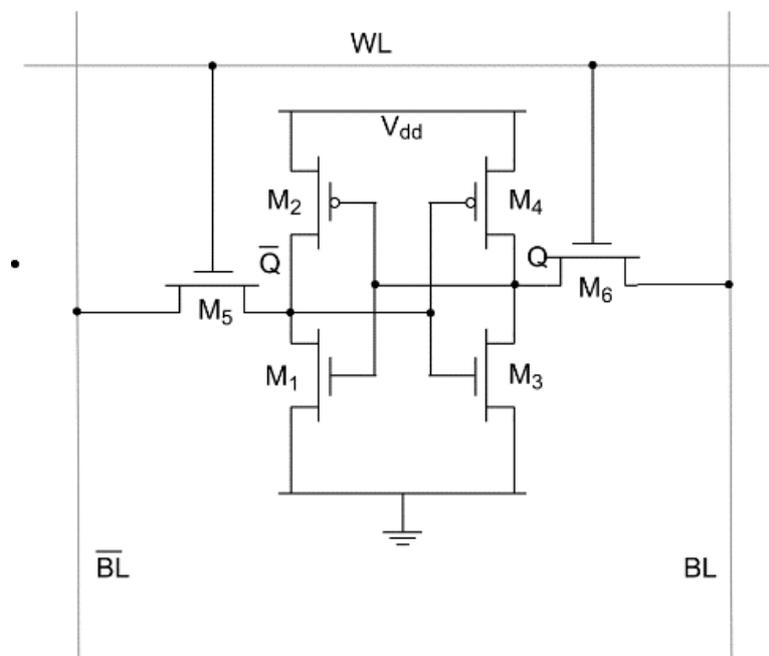
Figure 1. 3 : Memory hierarchy in computer systems. SCM has been introduced to fill the performance gap between memory and storage. Reprinted from [8]

## 1.3 Overview of memory technologies

Generally, memory technologies are divided into two main categories, the “volatile” and “non-volatile” memories. A volatile memory loses its data when the power is turned off. While, a non-volatile memory maintains the data even if the power is turned off.

### 1.3.1 Volatile memories

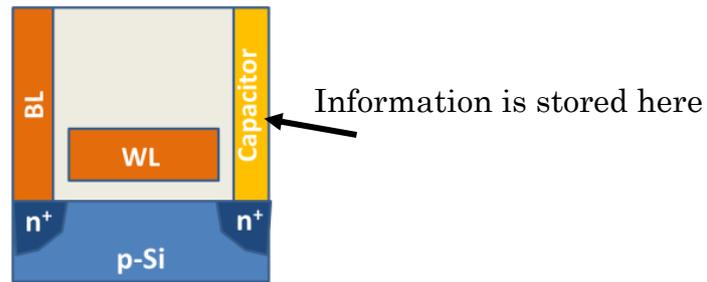
#### 1.3.1.1 SRAM (cache memory)



*Figure 1. 4: Typical six transistors (6T) SRAM architecture.*

The Static Random-Access Memory (SRAM) is a volatile memory based on six transistors (Figure 1. 4) and considered as cache memory. SRAM is typically integrated in microprocessors chips of computer systems. This memory technology provides ultra-low access time (Read/Write), in the order of  $\sim 1\text{ns}$ , with excellent endurance, higher than  $10^{15}$  programming cycles [1], [5]. However, SRAM technology has an expensive fabrication cost and very low density because of the large cell size (minimum  $\sim 24F^2$  [1]).

### 1.3.1.2 DRAM (main memory)



*Figure 1. 5 : Basic schematic of DRAM*

The Dynamic Random Access Memory (DRAM) is a volatile memory with one transistor and one capacitor (1T1C) architecture (Figure 1. 5). Typically, DRAM is used as main memory in traditional Von Neumann architecture. The memory effect is based on the charge stored in the capacitor, the logic state “1” corresponds to the presence of charges in the capacitor and the logic state “0” corresponds to the absence of charge in the capacitor. DRAM has low access time (5~10ns) and higher density compared to SRAM due to its smaller feature size (6-8F<sup>2</sup>) [1], [5], [11]. Data retention time of DRAMs is very short, in the order of few milliseconds, even in the presence of a power supply, therefore the memory cell has to be refreshed permanently to maintain data during system operating periods. Continuous refresh makes the DRAMs in the class of high power consumption memory devices.

## 1.3.2 Non-volatile memories

### 1.3.2.1 Flash memory (Storage memory)

Flash memory corresponds to floating gate (FG) MOS transistor devices as shown in Figure 1. 6-(a). In NOR-type architectures, the memory cell is programmed by channel hot carrier injection and charge accumulation in the floating gate of the transistor, then it could be erased by Fowler-Nordheim tunneling where the stored charges are injected back to the transistor channel under an applied electric field [2]. The reading operation depends on the charge stored in the FG layer. After erase operation the FG is no more charged, the memory cell conducts by applying a bias on the control gate.

After programming, the FG is rich in electrons and the memory cell threshold voltage is shifted. This phenomenon allows the modulation of the “apparent” threshold voltage of the transistor. To read the logic state of the cell (“0” or “1”), we need to read the current driven by the cell at fixed gate voltage as shown in Figure 1. 6–(b). The Flash memory has an access time in the order of hundreds of  $\mu\text{s}$  to  $\text{ms}$  [8]. NAND Flash offers very good scalability, therefore smaller cell area per bit compared with other existing NVMs such as NOR Flash and EPROM [12]. Scaling down the bit cell leads to cost reduction per bit because a higher density will be integrated in the same area compared to bigger devices.

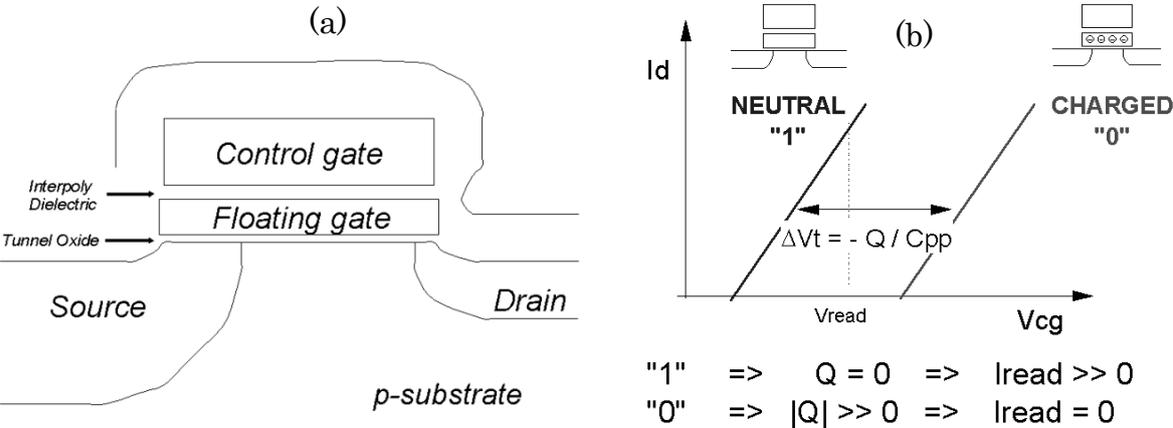


Figure 1. 6 : (a) Schematic of the Flash memory cell, (b) Read operation. Reprinted from [13]

Reliability issues such as wrong read of the cell, bad endurance, bad data retention, high device to device variability, program disturb errors coming from the interference of neighboring cells and short-channel effect (SCE) [14]–[16] are enhanced with scaled devices. Planar NAND Flash has achieved its physical and cost limits in advanced technology nodes. To solve the limitations issues of planar Flash, the 3D vertical NAND has been introduced based on multi-stacked memory arrays in vertical direction [17], [18]. 3D NAND is a high-density cost-effective memory. Indeed, 3D architectures can avoid the need for severe lithography, but still presents serious technological challenges, as any increase in terms of density can be achieved only through an increase in the number of layers.

## 1.4 Emerging memories

The scaling limitations of charge storage devices has been announced often in the past. Research centers and manufacturers around the world are working today on new “emerging memories technologies” to be used as SCMs. Several memory technologies are considered as promising candidates for SCM. Four main technologies are at the stage of prototypical memories: Resistive Random Access Memory (RRAM) [19], Phase Change Memory (PCM) [20]–[22], Spin Transfer Torque Magnetic Random Access Memory (STT-MRAM) [23]–[26] and Ferroelectric Random Access Memory (FeRAM)[27]–[30]. All of them are nonvolatile memories and not based on charge storage mechanisms. The fact that some of these memories are already in production has not stopped their evolution. In addition to the usual lithography-based scaling, new concepts and improvements of the basic technology and materials are being proposed that could lead to substantial improvements in memory density, performances and cost.

### 1.4.1 Ferroelectric Memories (FeRAM)

Ferroelectric memories are based on the permanent polarization of a ferroelectric material induced by external electric field and related to ion displacement in the crystal cell. Typical FeRAM cell consists of one access transistor and one ferroelectric capacitor (1T1C) as shown in Figure 1. 7. It combines the fast read and write of a DRAM [31]. Read operation of the memory state is disruptive [32], because it consists to read the displacement current related to the switching to the opposite polarization state (or the absence of such a current). Today, two main materials are used as ferroelectric active layers: the traditional PZT ( $\text{Pb}_x\text{Zr}_{1-x}\text{TiO}_3$ ) material, and the SBT ( $\text{SrBi}_2\text{Ta}_2\text{O}_9$ ) material which has been introduced recently and presents the advantage of easier scalability. The main bottleneck of FeRAMs memories is their poor scalability. The signal is proportional to the area of the capacitor, and inversely proportional to the thickness of active layer. The latter is limited in scaling by the interaction of ferroelectric material with the electrodes [33].

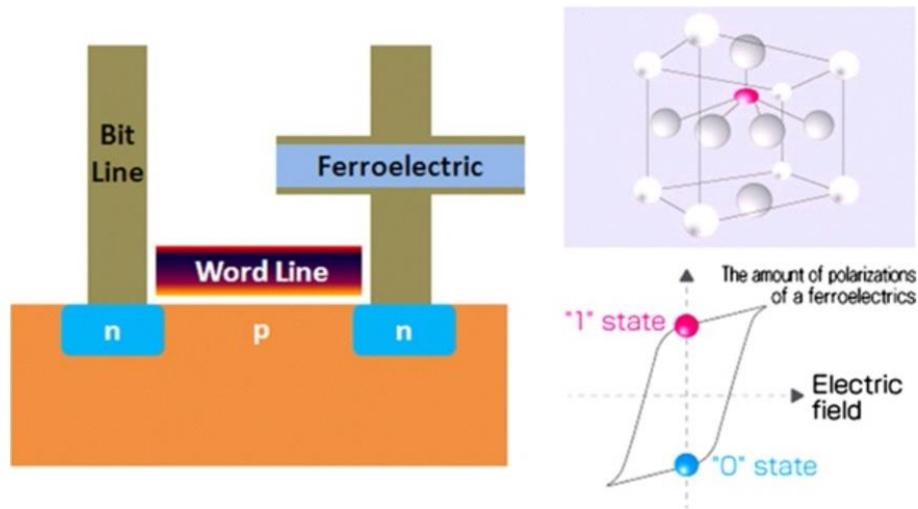


Figure 1. 7 : Basic structure of FeRAM cell. The crystal structure of ferroelectric material and the polarization-electric field hysteresis curve are also shown. Reprinted from [31]

### 1.4.2 Magnetic Memories

Magnetic memories are based on the magneto-resistive effect in thin films. The spintronic devices are typically composed by a Magnetic Tunnel Junction (MTJ), consisting of thin tunnel barrier sandwiched between two magnetic layers in series with an access transistor as shown in Figure 1. 8.

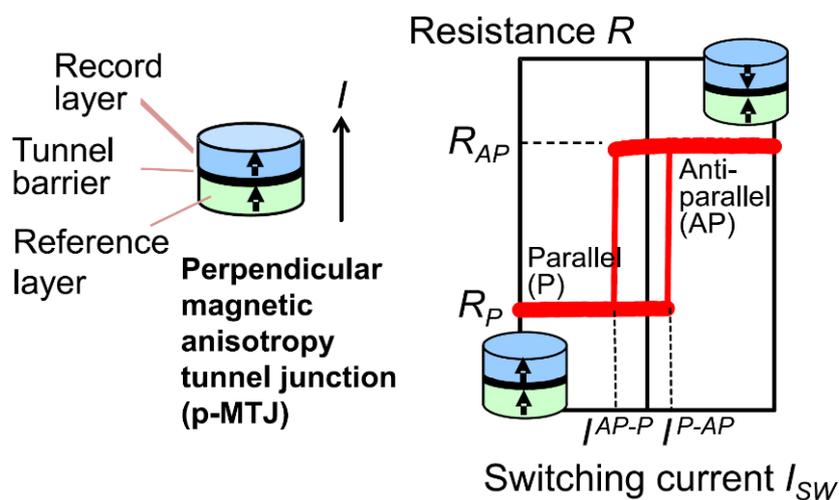


Figure 1. 8 : Basic schematic of MJT device with resistance switching current characteristics. Reprinted from [5]

The two ferromagnetic layers play different roles: one is a “recording” layer, with reversible magnetization direction, and the other is a “reference” layer, with fixed magnetization direction [34]. The resistance level of the memory cell is determined by the magnetization direction of the recording layer, while the tunneling current depends on the mutual orientation of the magnetic polarization in the two electrodes. The low resistance state corresponds to the parallel state, and the high resistance state corresponds to the anti-parallel state. The very fast programming/read time (<10ns), the very high endurance (>10<sup>16</sup>) and the non-volatility that strongly reduces the power consumption, make the magnetic memories a serious candidates for SRAM replacement [5]. Nevertheless, magnetic memories still have some challenges to be met such as large cell size, very small memory window, complexity of multilayered metal stack and compatibility with CMOS backend processing without degradation of the magnetic properties of the materials.

### 1.4.3 Phase change memories

Among the emerging memories, Phase Change Memory (PCM) demonstrated the capability to enter the memory market and to be a mainstream memory for the next few years [35], [36]. PCM memories are based on chalcogenide materials: an alloy of Germanium–Antimony–Tellurium (GeSbTe or GST) is commonly used as active layer in the memory stack (see Figure 1. 9). GST material was largely used in rewritable DVDs. PCM is currently the most mature emerging memory technology.

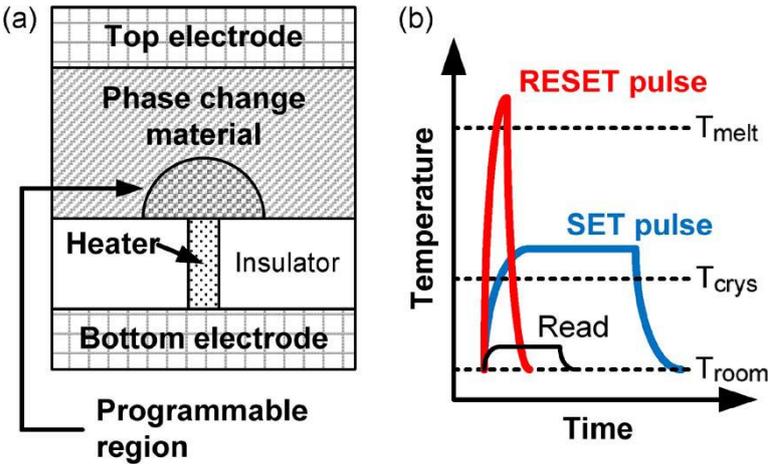


Figure 1. 9 : (a) Schematic of the PCM cell. (b) Programming schemes of a PCM. Reprinted from [37]

GST material can be switched by means of current flow through the material between an amorphous state and a crystalline state corresponding to the high resistance state and low resistance state, respectively. During “Set” operation (memory programmed to the low resistance state) an electrical pulse is applied to heat a part of the active region (in contact with the “heater”) above the crystallization temperature. During Reset operation, high current and fast pulses (10–100 ns) are required compared with Set conditions to melt-quench the active chalcogenide material and to program the cell to high resistance state as shown in Figure 1. 9-b. The high programming current required during Reset and considered as one of the main challenges of PCMs could be reduced by scaling down the device area, since PCM is programmed by Joule heating [38]. Superlattice-like structure (SLL) based on a super-lattice of thin chalcogenide layers with different compositions, has been proposed as a solution to strongly improve PCM performances in terms of switching speed and programming current (possibility to Reset without melting) [39].

Finally, PCM is very promising to be used as SCM to fill the gap between DRAM and NAND flash. In addition many companies have already produced high density PCM memories based on advanced technology nodes such as Samsung, Hynix, Micron and Intel [22], [36], [40].

#### **1.4.4 Resistive Random Access Memories (RRAMs)**

Resistive RAMs are based on resistive switching occurring in Metal-Insulator-Metal (MIM) structure. Structural modifications, mainly the formation and rupture of a conductive path in the active oxide material under applied electric field, lead to memory resistance change between low resistance state (LRS) and high resistance state (HRS), corresponding to the logical states “1” or “0”. Materials used in binary metal-oxide based RRAM are CMOS compatible and could be integrated easily in the BEOL with advanced-node CMOS technologies [19]. The type of defects involved in the creation of the conductive filament (CF) determines if the RRAM is an oxygen vacancy RAM (OxRAM) or metal ions based conductive bridge RAM (CBRAM). RRAM devices could be also categorized by means of switching polarity as “unipolar” RRAM or “bipolar” RRAM as shown in Figure 1. 10.

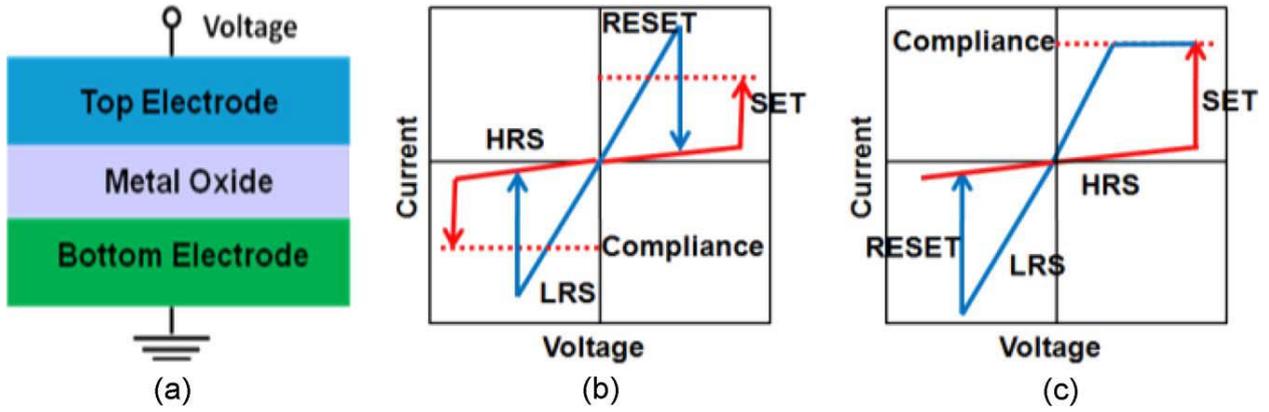


Figure 1. 10 : (a) Schematic of RRAM MIM structure, (b) Schematic of I-V characteristics of unipolar RRAM, (c) Schematic of I-V characteristics of bipolar RRAM. Reprinted from [19].

**Unipolar devices:** The switching between LRS and HRS and vice versa is obtained by using an electric field with the same polarity but different amplitude. The thermal effects during Reset (switching to HRS) pulses have been proposed as the reasons behind species diffusion resulting in a self-accelerated dissolution of the CF [41] [42].

**Bipolar devices:** The Set/ Reset operations depend on the polarity of the applied electric field. If Set operation occurs in one polarity, inverse polarity is mandatory to perform the Reset operation. Bipolar devices are more popular in research topics compared to unipolar devices.

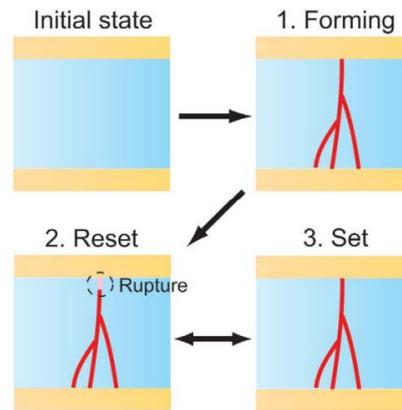
The electrode materials and the symmetry of the device structure determine the polarity of RRAM devices as presented in Table 1. 1. By combining the same active oxide material with different top and bottom electrodes, RRAM shows different polarities.

Table 1. 1 : Different electrodes combinations and their corresponding switching modes. Reprinted from [19]

Unipolar	Bipolar
Pt/NiO/Pt [7]	Pt/NiO/SrRuO <sub>3</sub> [54]
Pt/TiO <sub>2</sub> /Pt [8]	Pt/TiO <sub>2</sub> /TiN [55]
Pt/ZnO/Pt [18]	TiN/ZnO/Pt [56]
Pt/ZrO <sub>2</sub> /Pt [57]	Ti/ZrO <sub>2</sub> /Pt [57]
Pt/HfO <sub>2</sub> /Pt [58]	TiN/HfO <sub>2</sub> /Pt [59]
Pt/Al <sub>2</sub> O <sub>3</sub> /Ru [60]	Ti/Al <sub>2</sub> O <sub>3</sub> /Pt [61]

### 1.4.4.1 Resistive switching mechanism

The switching mechanisms, corresponding to the creation/rupture of oxygen-vacancies or metal-ions rich conductive filament, include three main operations: Forming, Reset and Set as shown in Figure 1. 11.



*Figure 1. 11 : Schematic of as-fabricated RRAM (initial state), (1) forming operation, (2) Reset operation and (3) Set operation. Reprinted from [43]*

**Forming:** Fresh devices have very large resistance values and often need to be initialized before stable resistive switching mechanisms can be achieved later. Forming operation is required once during the RRAM lifetime. After Forming, RRAM device is in LRS, where a CF connecting the top and bottom electrodes is created. Forming operation is a soft breakdown of the oxide material controlled by compliance current. The latter is imposed using external devices, in most cases a CMOS transistor to avoid permanent damage of the oxide material. LRS value is determined by the compliance current imposed during Forming/Set operations. During Forming operation, higher voltages are required compared with normal resistive switching conditions. Many studies have been focused on possible solutions to design “forming-free” devices by acting on several parameters (e.g. oxide materials, oxide thickness, electrodes materials, fabrication process conditions etc.)[44]–[46].

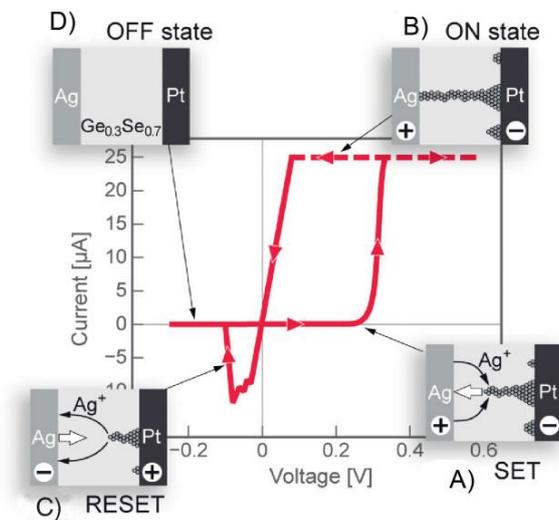
**Reset:** Partial dissolution of the CF occurs during Reset, the RRAM device switches to its HRS. Different physical mechanisms have been investigated to explain the Reset process, such as thermal dissolution of the conductive filament for unipolar devices, ion migration for bipolar devices as well as electrode/oxide interface properties that can determine the atomic behaviors during RRAM operations [47]–[49]. The main fundamental issue of resistive switching is the inability to heal the

total filament during Reset. Uncontrolled residual CF, (e.g. different length, density or shape), remains in the active layer after every Reset cycle. This leads to much higher HRS current ( $I_{HRS}$ ) compared to pristine state current and to high HRS variability. Cycle to cycle and device to device variability is considered as the weakest point of RRAM technology.

**Set:** It is similar to Forming operation, but lower applied voltage is required to restore the CF that was ruptured during Reset operation. After Set operation the RRAM is programmed to LRS and could be subsequently switched several times between the two resistance states (HRS and LRS). The memory window is defined as HRS/LRS factor.

#### 1.4.4.2 Conductive bridge RAM (CBRAM)

CBRAM is based on creation and rupture of metal-ions rich CF in the active layer (see Figure 1. 12). The memory structure typically consists of a solid electrolyte layer, that could be a chalcogenide (e.g.  $\text{GeS}_2$ ,  $\text{GeSe}$ ) or binary metal-oxide material (e.g.  $\text{ZrO}_x$ ,  $\text{GdO}_x$ ,  $\text{TaO}_x$ ) [50], [51].



*Figure 1. 12 : I-V characteristics of an Ag/GeSe/Pt electrochemical metallization cell with schematics of the formation and rupture of the metallic-rich CF. Reprinted from [52]*

The active layer is sandwiched between two metal electrodes, one of which is an electrochemically active (e.g. Ag or Cu) and the counter electrode is electrochemically inert (e.g. W or Pt). Under applied electric field, metal ions are

generated at the active electrode and driven in the solid electrolyte layer to form a metallic-rich CF, which makes the memory resistance dropping to LRS. During Reset operation an opposite applied bias compared to the one applied for Set operation leads to back-migration of the metal-ions toward the active electrode and the rupture of the metallic CF, thus the memory resistance increases to HRS.

### 1.4.4.3 Oxide based RAM (OxRAM)

OxRAM is also based on resistive switching with creation and rupture of an oxygen vacancy-rich CF. The device structure consists of a thin layer of binary metal-oxide sandwiched between two metal electrodes. One electrode plays the role of oxygen reservoir, accommodating oxygen ions coming from the active layer during Forming/Set operations. Energy delivered to the device during Forming/Set processes should be controlled to avoid the irreversible breakdown of the oxide. In most cases, a transistor is adopted to control the current through the RRAM structure (1T1R) during programming operations, as shown in Figure 1. 13. The most common binary metal oxide used as active layer in OxRAM devices are HfO<sub>x</sub>, TiO<sub>x</sub>, TaO<sub>x</sub> and AlO<sub>x</sub>.

OxRAMs have very interesting properties, such as simple MIM structures, multilevel capability thanks to the large memory window compared to STT-MRAM, very good scalability down to 10x10nm<sup>2</sup> [53], low operating voltages, fast switching (~10ns and less)[54] .

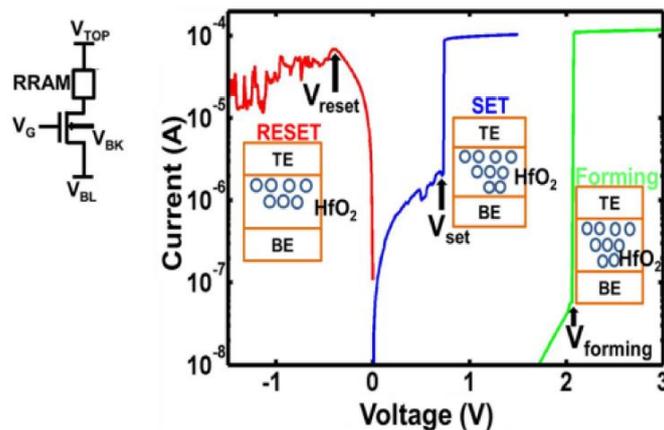


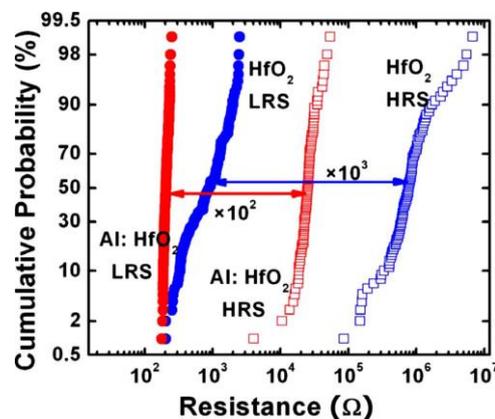
Figure 1. 13 : 1T1R schematic with typical I-V characteristics of forming, Set and Reset operations with current control for HfO<sub>2</sub> based OxRAM. Reprinted from [55]

## 1.4.5 RRAM key performances and reliability

In this thesis, we will focus on oxide based RAM (OxRAM) devices, we will study their reliability, performances and possible applications. For this purpose, we will review in this section the performances and the improvements of OxRAM devices presented in the literature. In the next chapters, we will present the results that we have obtained and contributions of this Ph.D. thesis to RRAM research field.

### 1.4.5.1 Uniformity

One of the main issues of OxRAM devices is the resistance variability, for both, cycle to cycle and device to device. The origin of this variability could be attributed to the stochastic nature of the conductive filament, as demonstrated in [56]. HRS variability comes from the variation in the tunneling gap distance created after the rupture of the CF during Reset operation. The HRS variability is most severe compared to LRS variability. Different methods, mainly materials engineering, have been proposed in the literature to improve the uniformity of OxRAM devices. One method is to introduce a thin Al buffer layer between the active oxide layer ( $\text{HfO}_x$ ) and the electrode, which leads to a more controllable CF formation [57] (see Figure 1. 14).



*Figure 1. 14 : HRS and LRS distributions, with and without Al layer. Uniformity improved with the presence of Al thin layer. Reprinted from [57]*

Another method to improve uniformity is to confine the region of the CF paths by reducing the cell area [58]. Scaled devices show better cycle to cycle and device to device uniformity compared with larger size devices. Programming solutions have

also been proposed to reduce parameter fluctuations, such as ramping up the Reset voltage, using multiple pulses instead of single programming [59].

### 1.4.5.2 Endurance

Programming endurance of OxRAM devices depends on many factors, such as programming conditions, device structure, process conditions, materials etc. The endurance failure could occur in both directions: LRS fails toward HRS or HRS fails toward LRS, as shown in Figure 1. 15.

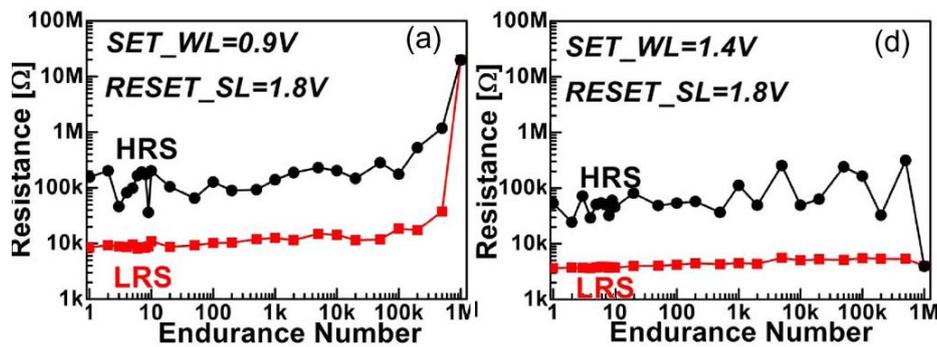


Figure 1. 15 : Endurance (a) LRS failure, (b) HRS failure. Reprinted from [60].

LRS failure is attributed to degradation of the oxygen vacancies ( $V_o$ ) mobility in the CF constriction due to high local temperature during switching [61]. It is sometimes attributed to the formation of an oxide layer between the electrode and the active oxide layer [62]. HRS failure is most common. Usually, after cycling, the OxRAM devices are stuck in LRS without possibilities to Reset the device again. HRS failure was attributed to different scenarios: (1) too many  $V_o$  generated at, or near, the electrode/oxide interface; (2) too many  $V_o$  generated in, or near, the CF; or (3) too many  $V_o$  generated inside the  $HfO_2$  matrix [19]. Excellent endurance ( $>10^{15}$ ) is required for RRAM devices to replace existing memory technologies (e.g. DRAM). H. Y. Lee *et al.* demonstrated an endurance over  $10^{10}$  cycles for  $HfO_x$ -based OxRAM using optimized programming conditions and CMP to flatten the memory bottom electrode [63].

### 1.4.5.3 Data retention

Ten years data retention at up to  $85^\circ C$  is expected for nonvolatile memories. Deep understanding of the resistive switching mechanisms is required to improve

OxRAM data retention. Many groups have investigated the data retention of OxRAM devices at microscopic levels. In [64], two possible retention degradation mechanisms were identified in HfO<sub>2</sub>/Hf based OxRAM: (1) the oxygen diffusion from the oxygen scavenging layer and recombination with V<sub>o</sub>; (2) the V<sub>o</sub> diffusion out of the CF and dissolution of the CF (see Figure 1. 16). They suggested an additional full stack annealing after RRAM cell fabrication to limit oxygen diffusion from the scavenging layer, because of the bonding of free oxygen with Hf electrode to form HfO<sub>x</sub>. This method will reduce the mobile oxygen supply. The compliance current imposed during Forming/Set operations has an important effect on data retention. With higher compliance current the CF is more stable, therefore, LRS shows better data retention.

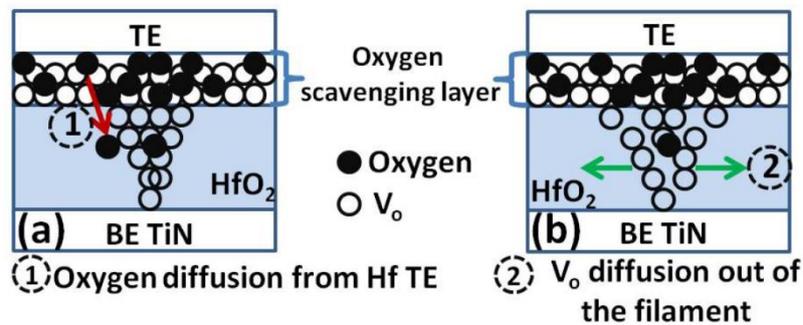


Figure 1. 16: Possible retention degradation mechanisms. Reprinted from [64]

In [55], the impact of atomic composition on data retention has been investigated by means of ab initio calculations. LRS retention failure was attributed to the lateral diffusion of oxygen vacancies at the constriction/tip of the conductive filament in HfO<sub>2</sub>-based RRAM. Al incorporation in HfO<sub>2</sub> was found to improve the data retention thanks to shorter bond associated with higher atomic concentration and higher V<sub>o</sub> diffusion barrier in Al doped devices. H. Y. Lee *et al.* demonstrate 500 minutes data retention for TiN/HfO<sub>2</sub>/Ti device at 200°C [65].

In the next chapter we will present our work on different methods to incorporate Al in HfO<sub>2</sub> based OxRAM, and their effects on data retention and forming voltage.

#### 1.4.5.4 Programming speed

The major issue of nowadays memory hierarchy is the speed gap between main memory (e.g. DRAM) and storage (e.g. NAND Flash). Emerging non-volatile

memories should provide high programming speed (in the order of 10's of ns) comparable to DRAM and SRAM, and high density and non-volatility, comparable to NAND flash. Elisa Vianello *et al.* [54] demonstrated a switching time lower than 10ns for HfO<sub>2</sub>/Ti based OxRAM as shown in Figure 1. 17.

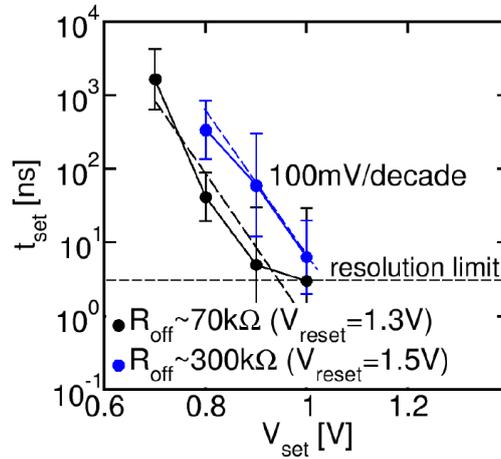


Figure 1. 17 : Programming time versus voltage for HfO<sub>2</sub>/Ti based OxRAM. Reprinted from [54]

Programming speed strongly depends on the binary metal-oxide material, and the programming conditions. In [19], high switching speed compared to DRAM is demonstrated for OxRAM devices using different metal oxide materials (see Table 1. 2).

Table 1. 2 : Programming speed of OxRAM devices with different oxide materials. Reprinted from [19]

	NiO IEDM 2004	Cu <sub>x</sub> O IEDM 2005	Ti:NiO IEDM 2007	TaO <sub>x</sub> IEDM 2008	Ti/HfO <sub>x</sub> IEDM 2008	Ti/HfO <sub>x</sub> IEDM 2009 &2010	WO <sub>x</sub> IEDM 2010	ZrO <sub>x</sub> /H fO <sub>x</sub> IEDM 2010	N:AlO <sub>x</sub> VLSI 2011	TaO <sub>x</sub> / Ta <sub>2</sub> O <sub>5</sub> VLSI 2011	Hf/HfO <sub>x</sub> IEDM 2011
switching type	unipolar	bipolar	unipolar	bipolar	bipolar	bipolar	bipolar	bipolar	bipolar	bipolar	bipolar
structure	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R	1R	1T-1R	1R	1T-1R
speed	~5μs	~50ns	~5ns	~10ns	~5ns	~0.3ns	~50ns	~40ns	N/A	~10ns	~10ns

#### 1.4.5.5 Irradiation immunity

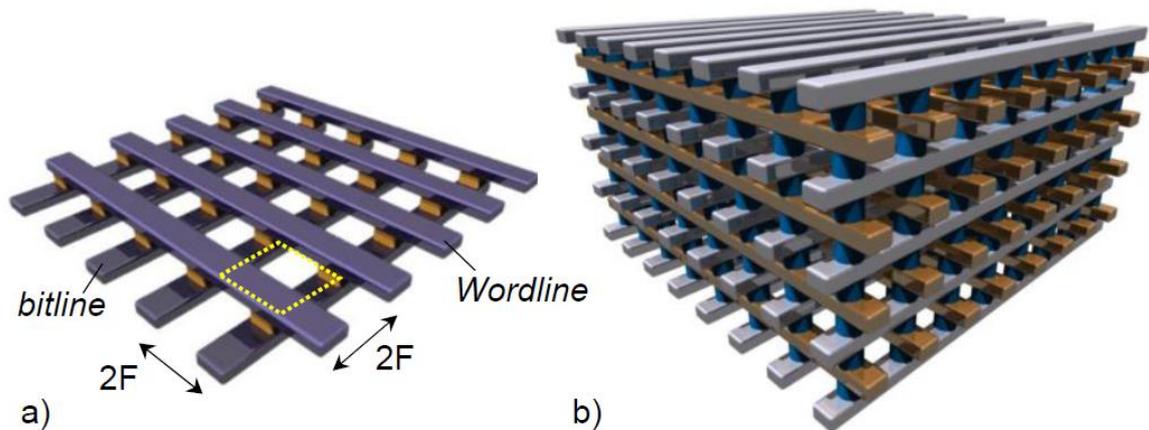
NVMs are used in a variety of space applications. Memories based on charge storage, such as flash memory, are not radiation hard technologies [66], as charges are sensitive to radiations. RRAM devices seems to be promising for space applications because this memory technology does not depend on charge storage but

rather on resistive switching mechanism, based on creation and rupture of oxygen vacancies-rich CF. Recent works show no direct effects of heavy ions irradiations (focusing on Single Event Effects - SEE) on devices using TaO<sub>x</sub> or Hf/HfO<sub>2</sub> stacks. The observed phenomena were either due to the degradation of the access transistor or to single events effects in the control circuitry [67]. In the next chapter, we will present our experimental and simulations results on HfO<sub>2</sub> based RRAM irradiation immunity. The memory devices show irradiation hardness under very energetic ions strikes.

## 1.5 Emerging memories architectures

### 1.5.1 3D Cross point architecture

In memory systems, the memory devices are organized in arrays. Every memory device in the array shares with neighbors one of the addressing lines. Cross-point architecture consists on the implementation of the two-terminal memory device on the cross-point between two perpendicular metal lines called “wordline” and “bitline” as shown in Figure 1. 18-a. In cross-point architecture the effective cell area could achieve  $4F^2$ , considering the width of the metal line and the space imposed between two metal lines are equal to “F” where “F” is the minimal feature size.  $4F^2$  is the smallest cell footprint that could be achieved from layout point of view. It is possible to stack multiple 2D cross-point layers into 3D stacked cross-point architecture, as shown in Figure 1. 18-b.



*Figure 1. 18 : Schematic of (a) 2D cross-point array, (b) Stacked 3D cross-point array. Reprinted from [68].*

If 3D stacked cross-point architecture is adopted, the minimal effective cell area is reduced to  $4F^2/n$ , where  $n$  is the number of 2D stacked layers. 3D cross-point is considered as very promising architecture for high density emerging resistive memories.

### 1.5.2 VRRAM architecture

A practical problem associated with stacked 3D cross-point array is that the cost per bit does not always scale with the increasing number of layers. This architecture requires critical process steps, e.g., lithography and etching of metal lines and via contacts for each additional layer [69]. For 3D vertical NAND architecture a single critical lithography and etching step are required to define the memory cells and multi-layers are formed simultaneously. Vertical Resistive-RAM (VRRAM) architecture was proposed for cost effective data storage application [70], [71]. VRRAM is expected to consume less than 1/3 in lateral and 1/2 in vertical dimension compared to the current charge trap based VNAND, which is promising for further reducing the cost per bit [69]. Figure 1. 19-a shows a schematic of VRRAM architecture and the active zone where the resistive switching occurs between the vertical and horizontal electrodes. Two memory points are identified at the same horizontal level between two parallel horizontal electrodes (see Figure 1. 19-b).

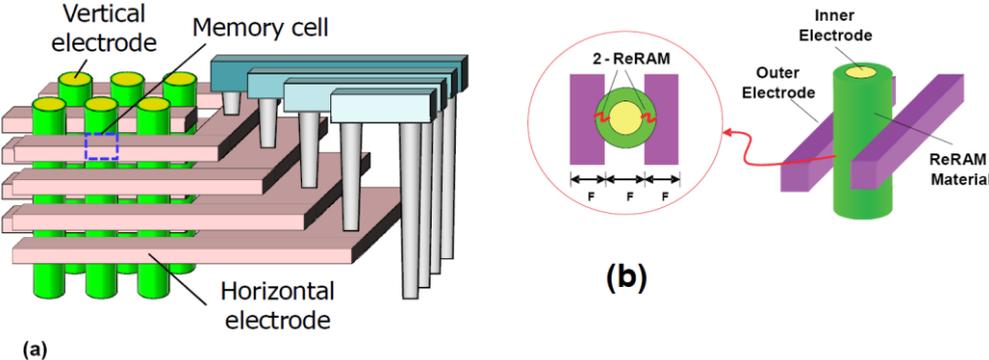
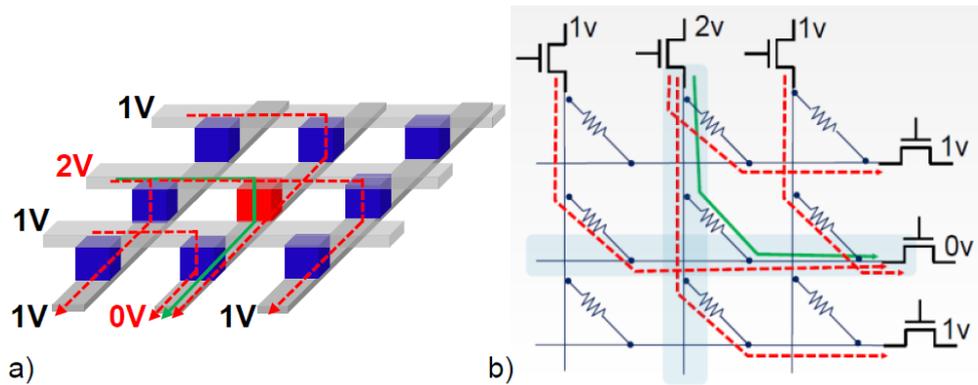


Figure 1. 19: (a) Schematic of VRRAM architecture, (b) Schematic of a memory point (one unit) with 2 RRAM devices in VRRAM architecture. Reprinted from [70], [71]

### 1.5.3 Sneak path current issue in RRAM arrays

The capability to address efficiently a specific cell within an array for reading or programming, without interfering with other cells, is as important as the basic

performances of the storage element. Each memory cell in the array should have high selectivity that could be provided by non-linear electrical characteristics of RRAM devices. However, the majority of the reported RRAM devices show almost ohmic characteristics (linear) in LRS and HRS states, consequently, this leads to “Sneak path current” issue through the unselected cells in the memory array. Sneak path current causes read and programming degradations, it also rises the total power consumption in the memory array.



*Figure 1. 20 : (a) Schematic of cross-point array illustrating the selected cell (red cube) and the leakage currents through the unselected/half-selected cells (blue cubes). (b) Schematic of the circuit of cross-point array. Green line: selected cell read current, red lines: sneak-path currents. Reprinted from [69].*

Figure 1. 20 shows half bias scheme during programming phase of a selected cell in the memory array. Programming bias and zero bias are applied on the word line and bit line of the selected cell respectively, half programming bias is applied on unselected word lines and bit lines. With the presence of sneak-path currents coming from half selected cells, the readout signal on the selected bit line does not correspond to the pure current through the selected cell, thus a read error occurs and higher power is consumed during the memory operation. In the next section we will review the selector devices that have been proposed to get rid of sneak path current issue in memory arrays.

## 1.6 Access devices for RRAM arrays (selectors)

The use of selector devices with non-linear I-V characteristics in one-selector one-resistor structure (1S1R) is proposed to suppress the sneak-path currents in RRAM

arrays. The high resistance of the selector at low bias is the dominant characteristic of half-selected or non-selected memory devices in the array, this results to suppression of the parasitic current as shown in Figure 1. 21.

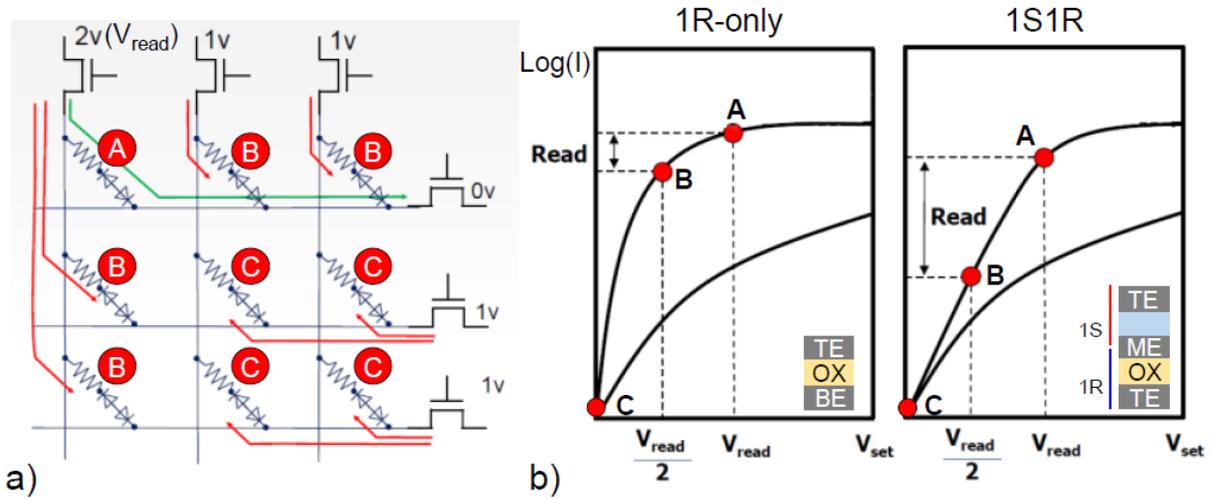


Figure 1. 21 : (a) Schematic of leakage current suppression in the case of 1S1R structure, (b) electrical characteristics comparison between 1R with ohmic behaviors and 1S1R with non-linear characteristics. Reprinted from [69].

## 1.6.1 Requirements for access devices

An access device must satisfy a number of specifications to be suitable for the integration in high density cross-point arrays. Selector characteristics could be summarized as following:

### 1. Two terminal device

A simple two terminal structure is required for selector devices to avoid extra cell area that prevents achieving the minimal effective cell area of  $4F^2$ . As an example, the three-terminal transistor can provide perfect selector performances for sneak-current suppression, but at the cost of complex process and large area of single cell.

### 2. High ON-state current density

A selector device should be able to deliver enough current density to program (Set/Reset) the memory element. Selector's ON-current density must be in the order of several MA/cm<sup>2</sup>. In the case of a 100nm<sup>2</sup> cell area that should be programmed at least with 10μA as compliance current, a current density of ~10MA/cm<sup>2</sup> is required.

### 3. Low OFF-state leakage current (high selectivity)

The maximum cross-point array size is linked directly to the circuit performance, such as read/write margins and power consumption. These performances are strongly related to the amount of leakage current flowing through the unselected cells in the cross-point array [72], [73]. Off-state current should be several orders of magnitude lower than On-state current to improve the overall array operation and to allow the implementation of large arrays. Consequently, high selectivity increases the overall area efficiency [74].

#### **4. Bidirectional operation**

Most of the reported RRAM devices exhibit bipolar characteristics during programming operations (Set/Reset). A selector device that provides current flowing in opposite polarizations is required in conjunction with bipolar emerging memories. In addition, high On-current density and high selectivity are required in both polarities.

#### **5. Voltage compatibility with the memory cell**

RRAM memory elements have different programming voltages (Set/Reset) depending on their material compositions. Voltage compatibility between the selector and RRAM cell is required in order to transfer selector selectivity to the 1S1R full cell. If the switching voltage of the access device is much lower compared to storage element, the leakage current through the half-selected cells will be high enough to disturb read and program operations in the memory array.

#### **6. Process compatibility**

The access device technology must be CMOS compatible, therefore materials such as Au, Pt etc. should be excluded from the selector structure. For 3D multilayer integration, the selector device has to be compatible with the thermal budget of the back end of the line (BEOL) process. This enable stacking subsequently multiple memory layers with interconnections among them.

The selector characteristics should never limit the memory array performances and reliability. Therefore, any other performances of the access device (e.g. switching speed, endurance, uniformity etc.) must be identical or better than the performances of the storage element.

Based on the above requirements it is very challenging to find the ideal access device that could provide all the characteristics needed for high density memory arrays. In the following, we will summarize the main candidates that have been proposed in the literature as selectors for 3D cross-point architectures.

## 1.6.2 Types of selector devices

### 1.6.2.1 Si-based selectors

Three terminals Si based transistors are considered as one of the best access devices for RRAM cells in terms of high current drive, high selectivity, current compliance, high reliability, bidirectionality mode etc. However, transistors require large area and complex process compared to two terminal selectors. Moreover, high thermal budgets are needed which is incompatible with 3D multilayers BEOL stacking [74].

Vertical Si PN junction deposited by selective epitaxial growth (SEG) on crystalline Si substrate was proposed as selector for unipolar PCM. The cell size was  $5.8F^2$  for the 90nm technology node. High ON-current was demonstrated ( $>25\text{MA}/\text{cm}^2$ ) with selectivity about  $10^8$  [75]. For bipolar emerging memory technologies, Si based NPN diodes are proposed as access devices (see Figure 1. 22-a). These devices provide ON-current density  $>1\text{MA}/\text{cm}^2$  and selectivity  $> 250$  or  $> 4700$  with respect to voltage polarities as shown Figure 1. 22-b [76] .

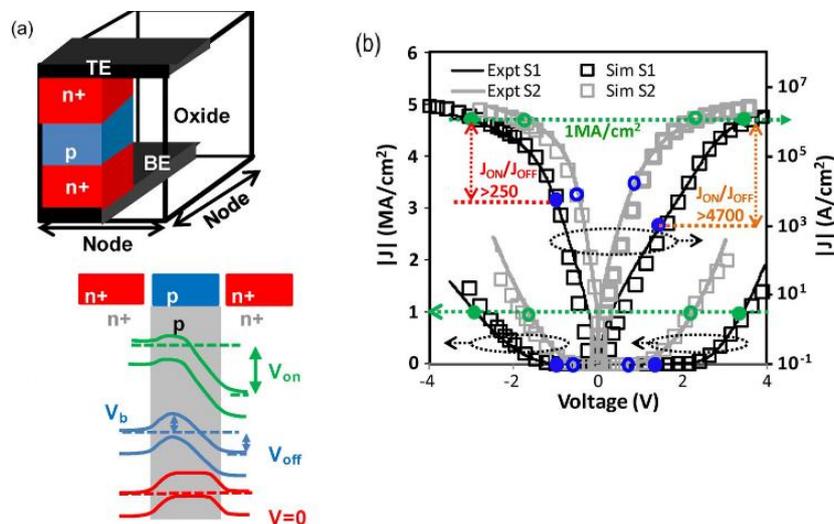


Figure 1. 22 : (a) Schematics of NPN selector with its band diagram at different polarizations, (b)  $|J|$ - $V$  characteristics for 1/3 polarization scheme of the NPN junction in linear (left axis) and log scale (right axis). Reprinted from [76]

The proposed Si based diodes are fabricated using epitaxial growth [75], [76], that is well known by its high temperature ( $\sim 700^\circ\text{C}$ ) according to the crystallization

temperature of Si. The high process temperature required for Si based diodes are not compatible with BEOL process, therefore such access devices are not suitable for 3D multilayer stacking.

### 1.6.2.2 Oxide based PN diodes

Many groups proposed the oxide based PN junction as access devices for unipolar memories in cross-point arrays [77]–[81]. I. G. Baek et al. presented a PN junction diode using NiO as p-type and TiO<sub>2</sub> as n-type semiconductor with process temperature below 300°C. The current density provided by the junction was very low (~1KA/cm<sup>2</sup>), thus not compatible with unipolar RRAM programming current requirements (>1MA/cm<sup>2</sup>) [79]. Myoung-Jae Lee et al. presented a p-CuO<sub>x</sub>/n-InZnO<sub>x</sub> heterojunction oxide diode as access device for unipolar NiO based RRAM, higher current densities were demonstrated (~10KA/cm<sup>2</sup>) compared with p-NiO<sub>x</sub>/ n-TiO<sub>x</sub> junction. However, this current density still very low for the programming of targeted memory technologies [80]. Seung-Eon Ahn et al. built a one-time field-programmable (OTP) memory with Al<sub>2</sub>O<sub>3</sub> as binary oxide material for the memory cell and a p-n CuO/InZnO<sub>x</sub> diode as access device [81].

### 1.6.2.3 Oxide tunnel barriers

One approach to obtain non-linear I-V characteristics is to introduce a thin oxide tunnel barrier in the memory stack. Several high-K materials have been reported for this purpose (HfO<sub>2</sub>, TiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub> and SiO<sub>2</sub>) [82]–[86]. In [85], Al<sub>2</sub>O<sub>3</sub> tunnel barrier was used with 5 x 6 μm<sup>2</sup> HfO<sub>2</sub> based RRAM, this method provided a selectivity of ~37. The selectivity is defined as the ratio between the current at the read voltage (I @ V<sub>read</sub>) and the current at half or one third read voltage, with respect to the adopted polarization scheme during read/programming operations (half bias or 1/3 schemes). The current conduction in the tunnel layer (Al<sub>2</sub>O<sub>3</sub> in this case) is dominated by Fowler Nordheim tunneling, which is well known being described by a non-linear (exponential) current conduction mechanism. Seong-Geon Park *et al.* [84] reported an RRAM device based on double layers of Transition Metal Oxide (TMO) and two tunnel barriers at top and bottom as shown in Figure 1. 23. This structure provided a selectivity of ~17.

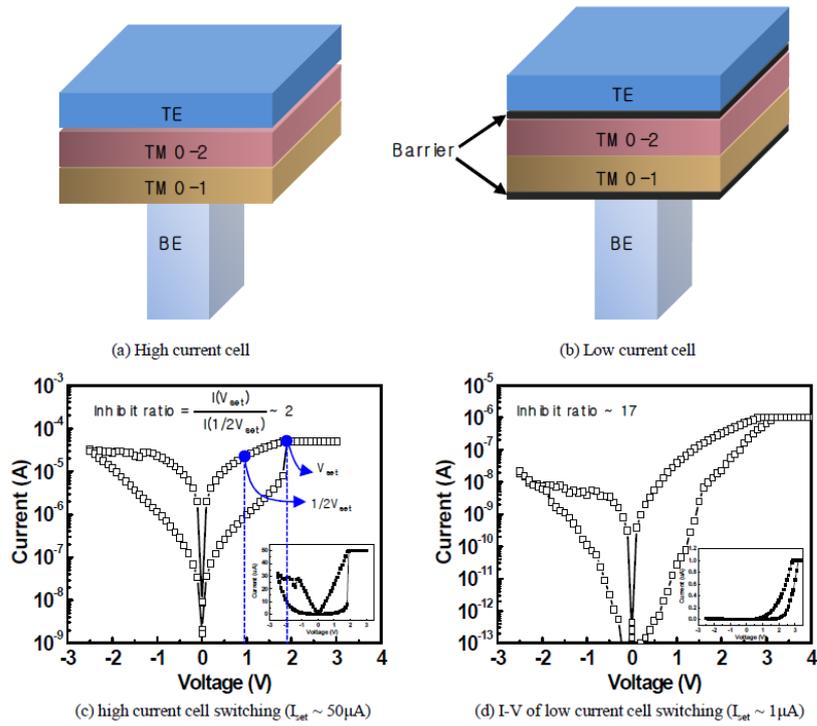


Figure 1. 23 : (a) (b) Schematics of RRAM structure with and without tunnel barriers. (c)(d) Linear and non-linear characteristics of RRAM device. Reprinted from [84]

B. Govoreanu *et al.* [87] reported a self-compliant RRAM consisted of  $TiO_2$  switching layer and  $Al_2O_3$  tunnel barrier as shown in Figure 1. 24. A selectivity of  $\sim 100$  and ON-current density of  $0.1 \text{ MA/cm}^2$  were measured for this device.

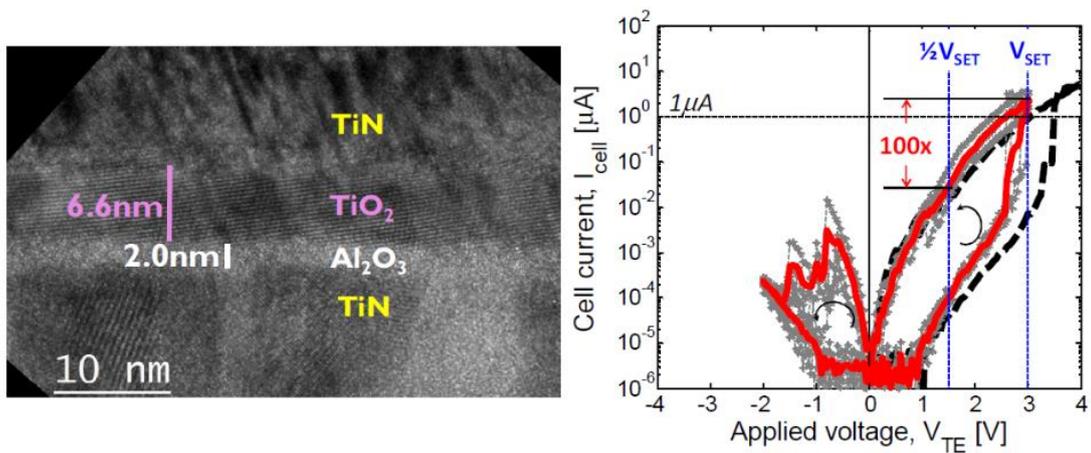


Figure 1. 24 : TEM cross-section of the full RRAM stack with  $Al_2O_3$  tunnel barrier, and the corresponding I-V characteristics. Reprinted from [87]

The oxide tunnel barrier is fully compatible with BEOL process requirements. However, this approach suffers from low selectivity that is strongly required to implement large memory arrays.

### 1.6.2.4 Mixed Ionic Electronic Conduction selector (MIEC)

Mixed ionic electronic conduction (MIEC) occurs when the material conducts ions and electronic charges. Access devices based on MIEC materials have become an attractive choice for 3D cross point arrays. In [88]–[90] copper-containing MIEC material is reported as selector device. Typically, the MIEC material is sandwiched between two electrodes where at least one must be inert or non-Cu-ionizing. The applied voltage leads to a transient Cu ion movement, followed by a steady electron/hole diffusion current which translates into non-linear I-V characteristics as shown in Figure 1. 25. The large fraction of mobile Cu enables very high current densities.

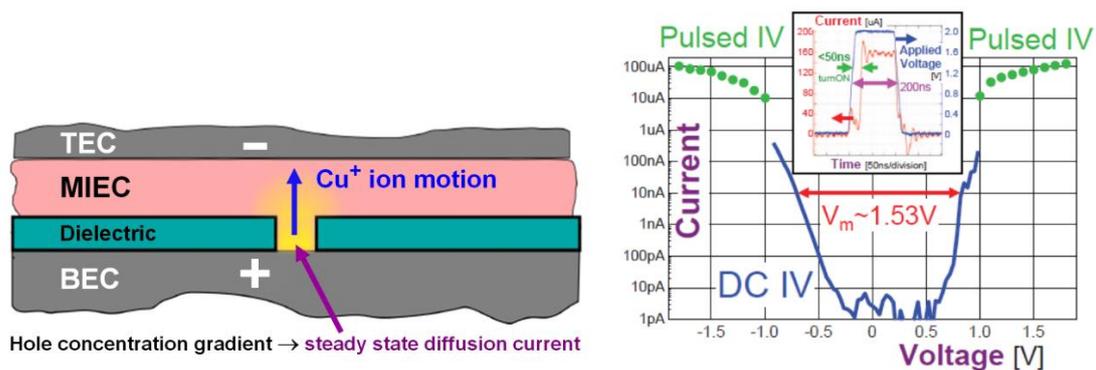


Figure 1. 25 : Schematic of a MIEC selector structure and its I-V characteristics.  $V_m$  (Voltage margin) corresponds to the voltage difference for reaching 10nA at positive/negative polarities. Reprinted from [89], [90].

MIEC materials are BEOL-friendly with process temperature  $<400^{\circ}\text{C}$ . They provide high current density ( $>10\text{MA}/\text{cm}^2$ ) and high selectivity with very low leakage in the voltage range between 0 and  $\sim 1.5\text{V}$  (leakage below 10nA), as shown in Figure 1. 25.

With low current operation regime ( $<10\mu\text{A}$ ), the MIEC can provide more than  $10^{10}$  endurance cycles. However, with high current operation ( $>10\mu\text{A}$ ), a voltage margin degradation occurs and the selector becomes a short circuit before  $10^6$  endurance cycles [89], [90]. Endurance failure is explained by the accumulation of Cu ions in the MIEC material. In addition, MIEC selector has small operating voltage range

(low voltage margin). This feature makes the MIEC materials less suitable as access devices for RRAMs that require relatively high programming voltages compared to the operating voltages of MIEC.

### 1.6.2.5 Threshold switching selectors

Access devices with threshold switching characteristics are considered as very promising candidates for 3D cross-point arrays. A threshold switch consists of two main regimes: (i) a very high resistance state at low field that serves to suppress the sneak-path current, (ii) a very low resistance state with high current drive when the applied bias exceeds a threshold voltage, this serves for RRAM programming. Different types of devices with threshold switching characteristics are proposed as access devices for 3D cross-point memory arrays. In this section, we will review some of the proposed threshold switching devices.

#### 1) Ovonic threshold switching (OTS)

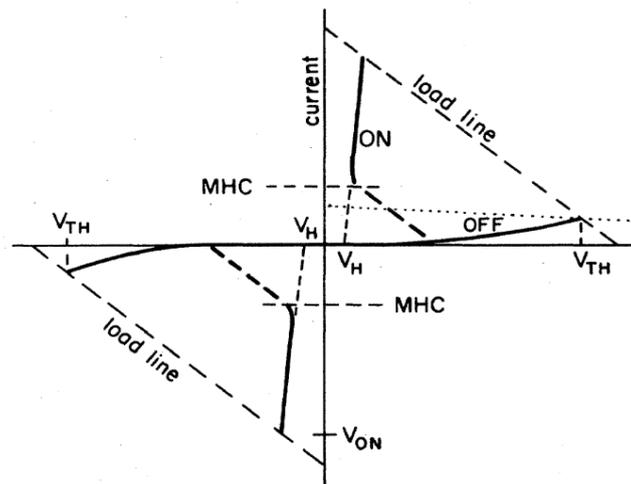


Figure 1. 26 : I-V characteristics of the threshold switching in OTS material with the presence of a series resistance that determines the load line. Reprinted from [92]

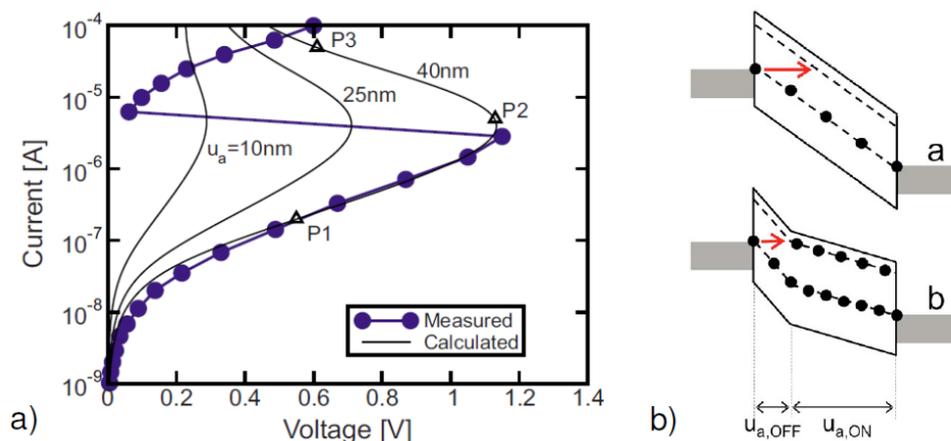
Ovonic Threshold Switching (OTS) principle was first observed by S. R. Ovshinsky in various thin film chalcogenide materials [91]. As demonstrated in Figure 1. 26 the I-V characteristics show abrupt decreasing from high initial resistance state to low resistance state when the applied voltage matches the threshold voltage “ $V_{th}$ ”. The device remains in the low resistance state if a minimum holding voltage (“ $V_H$ ”

in Figure 1. 26) is applied, otherwise the OTS device switches back to the high resistance state. Therefore, the threshold switching principle is volatile in this case.

The attractive characteristics of OTS based access devices could be summarized as follows:

- 1) High selectivity
- 2) A large off-state margin that ensures the selectivity of the full 1S1R during reading and programming.
- 3) The capability to deliver high current density in the low resistance state ( $> 10\text{MA}/\text{cm}^2$ ).

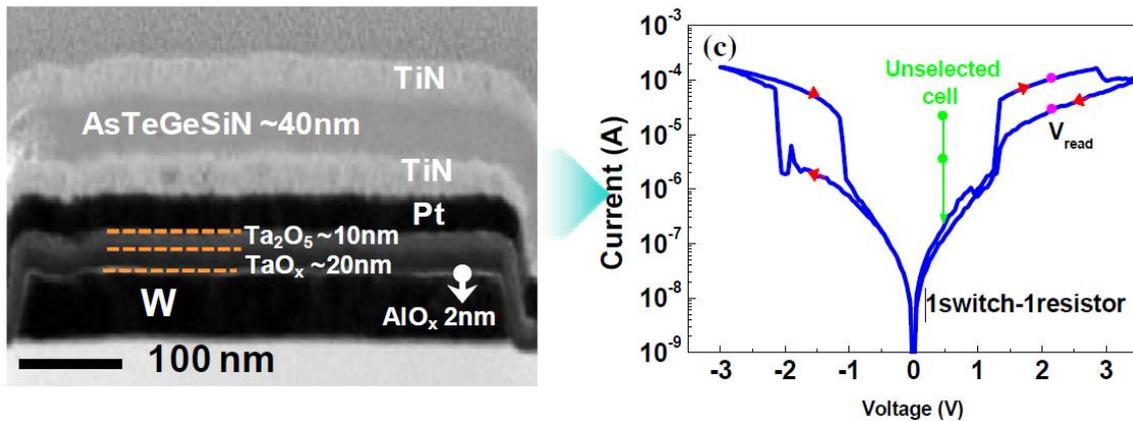
The OTS mechanism was explained by different theories, such as mixed electronic and thermal (MET) model, which is a thermally induced electronic switching [93]. It was also explained by field-induced carrier generation [94], (i.e. when all the traps are filled, carriers can transit the sample with an enhanced mobility and the generation rate required to keep the traps filled is reduced from its threshold value). Daniele Ielmini [95], demonstrated an analytical model based on the balance between electron energy gain and relaxation in the hopping transport. The I-V characteristics in the low current regime are described by the Poole-Frenkel (PF) current conduction mechanism, and the exponential increase of the current is described by the field-induced barrier lowering effect, which enhances electron hopping conduction as shown in Figure 1. 27.



*Figure 1. 27 : (a) Measured I-V for a PCM with  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  chalcogenide and simulated curves for different values of the amorphous chalcogenide thickness, (b) Schematic of conduction bands in the low and high voltages regimes. Reprinted from [95]*

As the applied voltage further increases, the electrons tunnel to higher energy traps. The tunneled electrons occupy the shallow traps close to the conduction band, giving rise to a non-uniformity of the electric field across the OTS material. To a certain extent, the region near the cathode becomes ‘invisible’ for the tunneling electrons. This corresponds to the occurrence of the S-type I-V snapback and then the OTS switching happens.

Different chalcogenide materials were reported for binary OTS access devices such as ZnTe, GeTe, SiTe, GeSe etc. [96]–[98]. In [99] Myoung-Jae Lee et al. demonstrated an AsTeGeSiN based OTS selector successfully integrated with TaO<sub>x</sub> based RRAM, as shown in Figure 1. 28. The selector provides 11MA/cm<sup>2</sup> as ON-current density, a selectivity of 1000 for 30x30nm<sup>2</sup> cell size and more than 10<sup>8</sup> endurance cycles. Post deposition annealing could reduce the off-state leakage current as the trap density in the chalcogenide alloy decreases after annealing [99]. DerChang Kau et al. [100] demonstrated a 1S1R cell with phase change memory (PCM) as storage element and OTS selector. The single cell provides 9ns programming speed and 10<sup>6</sup> endurance cycles.



*Figure 1. 28 : TEM image of the 1S1R device structure with AsTeGeSiN based OTS and the corresponding I-V characteristics. Reprinted from [99]*

Chalcogenide materials are very promising candidates for access devices implementation. The characteristics of the alloy strongly depends on its material composition (e.g. elements concentration), therefore, most of the research today is focusing on chalcogenide materials engineering to obtain the optimal OTS based selector. In chapter IV, we will present our 1S1R device with HfO<sub>2</sub> based RRAM as storage element and GeSe based OTS selector.

## 2) Metal Insulator Transition devices (MIT)

Metal-Insulator-Transition devices present a “fast” reversible resistivity changes between low and high resistance states that is thermally triggered. MIT mechanism is widely observed in condensed-matter systems, such as  $\text{VO}_2$ ,  $\text{NbO}_2$  etc. [101]. Myungwoo Son et al. [102] presented  $\text{Pt}/\text{VO}_2/\text{Pt}$  selector (see Figure 1. 29).  $\text{VO}_2$  based selector provides a selectivity  $>50$ , fast switching speed ( $<20\text{ns}$ ) and high ON-current density ( $>1\text{MA}/\text{cm}^2$ ). Electrical characteristics of the presented  $\text{VO}_2$  based access device strongly depend on the device size, as the MIT mechanism is observed only for small devices (nanoscale) while large area devices (microscale) show Ohmic characteristics, as shown in the left inset of Figure 1. 29. However, the operation temperature of  $\text{VO}_2$  is very low ( $<67^\circ\text{C}$ ). Therefore, such as access device is not compatible with applications that require operating temperatures up to  $85^\circ\text{C}$ . Seonghyun Kim et al. [103] reported  $\text{Pt}/\text{NbO}_x/\text{Pt}$  as MIT access device with high temperature stability ( $\sim 160^\circ\text{C}$ ) compared to  $\text{VO}_2$ . However, the device shows higher switching voltages and low selectivity as shown in Figure 1. 30.

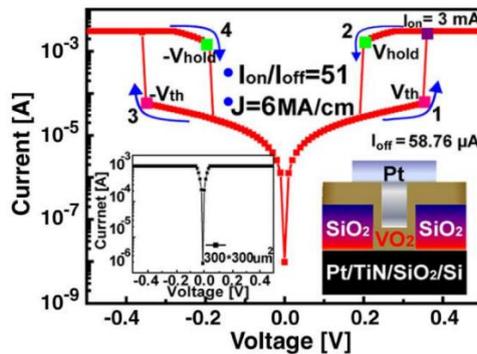


Figure 1. 29 :  $I$ - $V$  characteristics of  $\text{VO}_2$  based MIT selector with  $250\text{ nm}$  active area (via diameter). Inset on the left:  $I$ - $V$  characteristics of microscale device ( $300 \times 300\ \mu\text{m}^2$ ). Inset on the right: schematic of the nanoscale selector device. Reprinted from [102]

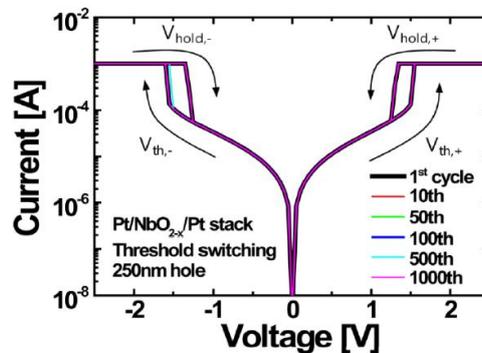
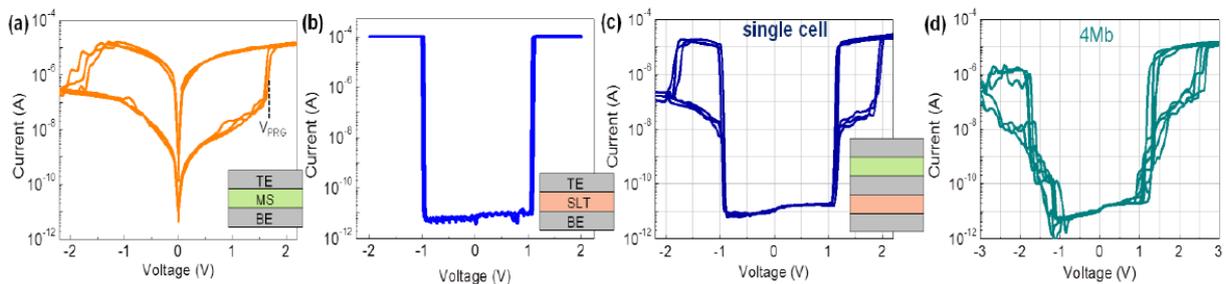


Figure 1. 30 :  $I$ - $V$  characteristics of  $\text{Pt}/\text{NbO}_x/\text{Pt}$  selector. Reprinted from [103]

The main issue of MIT based selector is the high current level in the OFF-state. This leads to high leakage current in 3D cross-point arrays during read/programming operations. The high current level in the OFF-state seems to be mandatory such device to produce enough Joule heating to trigger the transition between Metal and Insulator phases.

### 3) Field Assisted Super-Linear Threshold (FAST) selector

Sung Hyun Jo et al. [104] reported a Field Assisted Superlinear Threshold (FAST) selector. I-V characteristics are very similar to volatile threshold switching (e.g. OTS), but with much better performances (see Figure 1. 31). The selector device shows a selectivity around  $10^{10}$ ,  $5\text{MA}/\text{cm}^2$  as ON-current density, and  $10^8$  endurance cycles. The 1S1R shows a selectivity of  $\sim 10^6$ . The processing temperature of a FAST selector is less than  $300^\circ\text{C}$ , therefore, it is compatible with 3D-cross point integration process. As a consequence, FAST selector shows excellent characteristics that are suitable for high memory density integration. Unfortunately, the material composition of this selector is still a confidential work to Crossbar company.



*Figure 1. 31: I-V characteristics of (a) RRAM (b) FAST selector (c) 1S1R device (d) crossbar array based on 1S1R. Reprinted from [104]*

### 1.6.3 Selectors benchmarking

Table 1. 3 : Summary of the reported selectors

<i>Selector device</i>	<i>ON-current density (MA/cm<sup>2</sup>)</i>	<i>Selectivity</i>	<i>Endurance #cycles</i>	<i>Polarity</i>	<i>Comments</i>
<i>Si transistor</i>	>1	>10 <sup>6</sup>	>10 <sup>8</sup>	Bipolar	Complex process and large device area therefore, not suitable for 3D integration
<i>Oxide diode</i>	~10	>10 <sup>5</sup>	>10 <sup>4</sup>	Unipolar	Not suitable for bipolar emerging memories
<i>Si NPN diode</i>	>1	>240	----	Bipolar	Process complexity and low selectivity
<i>Tunnel barriers</i>	<1	<100	----	Bipolar	Low performances
<i>a-Si barrier</i>	>1	~10 <sup>3</sup>	~10 <sup>6</sup>	Bipolar	High operating voltage required
<i>MIEC</i>	>10	>10 <sup>5</sup>	>10 <sup>6</sup>	Bipolar	small operating voltage rang (low voltage margin), limited endurance
<i>OTS</i>	>10	>10 <sup>4</sup>	>10 <sup>8</sup>	Bipolar	Complex materials
<i>FAST</i>	>1	>10 <sup>5</sup>	10 <sup>8</sup>	Bipolar	Material not identified

## 1.7 Thesis content overview

### 1.7.1 Thesis objectives

The integration of embedded Flash memories with advanced CMOS nodes poses many problems in terms of process compatibility and physical limitations of the memory device itself. To realize high-density storage memories, single cells should provide specific characteristics (e.g. high selectivity, low power consumption, ultra-scaled devices etc.) high performances and excellent reliability.

Many types of emerging memories such as phase change memories (PCM), magnetic memories (MRAM) and resistive switching memories (RRAM) are proposed as candidates for embedded memories and SCM applications.

In this thesis, we will investigate first the reliability of HfO<sub>2</sub> based RRAM. To improve the data retention of these devices and make them compatible with high temperature environments such as automotive applications, we propose different material engineering strategies. In addition, we investigate the effects of heavy ions irradiation on HfO<sub>2</sub> based RRAM for space applications, where the electronic devices should provide high levels of radiation immunity in such environments.

Crossbar architecture targets the storage class memory (SCM) applications. After the single cell reliability study, we will investigate the compatibility of HfO<sub>2</sub> based RRAM with high density cross-point architectures. For this purpose, we introduce first an additional tunnel barrier to the memory stack, resulting in a Self-Rectifying (selector-less) Cell (SRC), then we will integrate a two-terminal OTS selector device with the RRAM element in 1S1R device. We will explore the characteristics and the performances of both access devices.

### 1.7.2 Thesis outline

This thesis is organized as follow:

#### **Chapter 2: Characterization and modeling of HfO<sub>2</sub> based RRAM cells**

In this chapter, we introduce our HfO<sub>2</sub> based RRAM technology, describing the process and device structure details. The device characterization methodologies and

the measurement equipment that we have used during this Ph.D. are presented in details as well. Finally, we present the simulation tool that we adopted to investigate the kinetics of the forming process, the charge transport mechanisms and defects generation in the binary oxide material at the microscopic level.

### **Chapter 3: Reliability of HfO<sub>2</sub> based RRAM cells**

In this chapter, we investigate first the data retention of the HfO<sub>2</sub> based RRAM. Then, we propose aluminum (Al) incorporation with different methods to improve the data retention of the memory cells. The effects of Al incorporation on the forming process have been investigated at the microscopic level by means of physics based simulations. Then, we will study the radiation immunity of the RRAM devices by irradiating the memory cells with heavy ions comparable to those existing in the space. The experimental results obtained after irradiation are also explored by simulation.

### **Chapter 4: Access devices for cross-point memory arrays**

In this chapter we investigated two technologies to fabricate a back-end selector for crossbar architectures. First, we introduce a tunnel barrier to the HfO<sub>2</sub> based RRAM, this method shows limited performances (e.g. low selectivity). Then, we integrate an OTS access device in series with the memory cell. A detailed investigation of the main memory operations, Forming, Set, Reset and read is presented. An innovative reading strategy is proposed to decrease power consumption during read process. The 1S1R shows better characteristics in terms of selectivity compared to the tunnel barrier solution. In addition, we present an OTS material engineering to improve the selectivity of the 1S1R device.

### **Chapter 5: Summery and perspectives**

In the conclusion, we will summarize the main results and contributions of this Ph.D. In addition, we provide a perspective on the future work that needs to be done for the further progress of RRAM reliability and novel access devices.

## 1.8 References

- [1] S. Natarajan, S. Chung, Lluís Paris and Ali Keshavarzi, “Searching for the dream embedded memory,” *IEEE Solid Stat. Circ. Mag.*, pp. 34 - 44, 2009.
- [2] F. Masuoka, M. Asano, H. Iwahashi, T. Komuro, and S. Tanaka, “A new flash E2PROM cell using triple polysilicon technology,” *1984 Int. Electron Devices Meet.*, vol. 30, pp. 464–467, 1984.
- [3] *Harold Pilo, Chad A. Adams, Igor Arsovski, Robert M. Houle, Steven M. Lamphier, Michael M. Lee, Frank M. Pavlik, Sushma N. Sambatur, Adnan Seferagic, Richard Wu and Mohammad I. Younus*, “A 64Mb SRAM in 22nm SOI technology featuring fine-granularity power gating and low-energy power-supply-partition techniques for 37% leakage reduction,” *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 56, pp. 322–323, 2013.
- [4] E. Karl *et al.*, “A 4.6 GHz 162 Mb SRAM design in 22 nm tri-gate CMOS technology with integrated read and write assist circuitry,” *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 150–158, 2013.
- [5] T. Endoh, H. Koike, S. Ikeda, T. Hanyu, and H. Ohno, “An Overview of Nonvolatile Emerging Memories — Spintronics for Working Memories,” *IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS*, vol. 6, no. 2, pp. 109–119, 2016.
- [6] T. Endoh, “Nonvolatile logic and memory devices based on spintronics,” *Proc. - IEEE Int. Symp. Circuits Syst.*, vol. 2015–July, pp. 13–16, 2015.
- [7] T. Endoh, T. Ohsawa, H. Koike, T. Hanyu, and H. Ohno, “Restructuring of memory hierarchy in computing system with spintronics-based technologies,” *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. 89–90, 2012.
- [8] “Storage Class Memory,” Science and technology, IBM Almaden Research Center, Presentation in January, 2013.
- [9] C. H. Lam, “Storage class memory,” *ICSICT-2010 - 2010 10th IEEE Int. Conf. Solid-State Integr. Circuit Technol. Proc.*, pp. 1080–1083, 2010.
- [10] H. Park, S. Baek, J. Choi, D. Lee, and S. H. Noh, “Exploiting Storage Class Memory to Reduce Energy Consumption in Mobile Multimedia Devices,” 2010 Digest of Technical Papers International Conference on Consumer Electronics (ICCE), pp. 1–2, 2010.
- [11] S. K. Park, “Technology Scaling Challenge and Future Prospects of DRAM and NAND Flash Memory,” *2015 IEEE 7th Int. Mem. Work. IMW 2015*, pp. 1–4, 2015.
- [12] F. Masuoka, M. Asano, H. Iwahashi, T. Komuro, and S. Tanaka, “A 256K Flash EEPROM using Triple Polysilicon Technology,” *IEEE ISSCC 85*, pp. 168–169, 1985.
- [13] S. Yoo, “Introduction to Flash Memory Operation,” *PROCEEDINGS OF THE IEEE*, vol. 91, no. 4, pp. 489–502, 2003.
- [14] K. Takeuchi, “Scaling challenges of NAND flash memory and hybrid memory system with storage class memory & NAND flash memory,” *Proc. Cust. Integr. Circuits Conf.*, 2013.
- [15] A. C. K. Chan, T. Y. Man, J. He, K. H. Yuen, W. K. Lee, and M. Chan, “SOI flash memory scaling limit and design consideration based on 2-D analytical modeling,” *IEEE Trans. Electron Devices*, vol. 51, no. 12, pp. 2054–2060, 2004.

- [16] A. Torsi, Y. Zhao, H. Liu, T. Tanzawa, A. Goda, P. Kalavade, and K. Parat “A program disturb model and channel leakage current study for Sub-20 nm nand flash cells,” *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 11–16, 2011.
- [17] P. Y. Du, H. T. Lue, Y. H. Shih, K. Y. Hsieh, and C. Y. Lu, “Overview of 3D NAND Flash and progress of split-page 3D vertical gate (3DVG) NAND architecture,” *Proc. - 2014 IEEE 12th Int. Conf. Solid-State Integr. Circuit Technol. ICSICT 2014*, vol. 1, pp. 3–6, 2014.
- [18] H. Tanaka, M.Kido, K.Yahashi, M.Oomura, R.Katsumata, M.Kito, Y.Fukuzumi, M.Sato, Y.Nagata, Y.Matsuoka, Y.Iwata, H.Aochi and A.Nitayama “Bit Cost Scalable technology with and plug process for ultra high density flash memory,” *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. 14–15, 2007.
- [19] H. S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen, and M.-J. Tsai “Metal-oxide RRAM,” in *Proceedings of the IEEE*, 2012, vol. 100, no. 6, pp. 1951–1970.
- [20] K. Osada, T. Kawahara, R. Takemura, N. Kitai, N. Takaura, N. Matsuzaki, K. Kurotsuchi, H. Moriya, and M. Moniwa “Phase change RAM operated with 1.5-V CMOS as low cost embedded memory,” *Proc. Cust. Integr. Circuits Conf.*, vol. 2005, pp. 424–427, 2005.
- [21] M. Gill, T. Lowrey, and J. Park, “Ovonic Unified Memory - A High-Performance Nonvolatile Memory Technology for Stand-Alone Memory and Embedded Applications,” 2002 IEEE International Solid-State Circuits Conference.
- [22] S. H. Lee *et al.*, “Highly productive PCRAM technology platform and full chip operation: Based on 4F<sup>2</sup> (84nm pitch) cell scheme for 1 Gb and beyond,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2, pp. 47–50, 2011.
- [23] S. C. Oh, J. H. Jeong, W. C. Lim, W. J. Kim, Y. H. Kim, H. J. Shin, J. E. Lee, Y. G. Shin, S. Choi and C. Chung “On-axis scheme and novel MTJ structure for sub-30nm Gb density STT-MRAM,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 300–303, 2010.
- [24] M. Hosomi *et al.*, “A novel nonvolatile memory with spin torque transfer magnetization switching: spin-ram,” *IEEE Int. Electron Devices Meet. 2005. IEDM Tech. Dig.*, pp. 459–462, 2005.
- [25] E. Chen *et al.*, “Progress and prospects of spin transfer torque random access memory,” *IEEE Trans. Magn.*, vol. 48, no. 11, pp. 3025–3030, 2012.
- [26] S. Chung *et al.*, “Fully integrated 54nm STT-RAM with the smallest bit cell dimension for high density memory application,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 304–307, 2010.
- [27] W. I. Kinney, W. Shepherd, W. Miller, J. Evans, and R. Womack, “A non-volatile memory cell based on ferroelectric storage capacitors,” *1987 Int. Electron Devices Meet.*, pp. 850–851, 1987.
- [28] H. Shiga *et al.*, “A 1.6 GB/s DDR2 128 Mb chain FeRAM with scalable octal bitline and sensing schemes,” *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 142–152, 2010.
- [29] M. Qazi, M. Clinton, S. Bartling, and A. P. Chandrakasan, “A low-voltage 1 Mb FRAM in 0.13  $\mu\text{m}$  CMOS featuring time-to-digital sensing for expanded operating margin,” *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 141–150, 2012.
- [30] N. Setter, D. Damjanovic, L. Eng, G. Fox, S. Gevorgian, S. Hong, A. Kingon, H. Kohlstedt, N. Y. Park, G. B. Stephenson, I. Stolitchnov, A. K. TagansteV, D. V. Taylor, T. Yamada, and S. Streiffer, “Ferroelectric thin films: Review of materials, properties, and applications,” *J. Appl. Phys.*, vol. 100, no. 5, 2006.

- [31] J. Meena, S. Sze, U. Chand, and T.-Y. Tseng, "Overview of emerging nonvolatile memory technologies," *Nanoscale Res. Lett.*, vol. 9, no. 1, p. 526, 2014.
- [32] S. S. Eaton, D. B. Butler, M. Parris, D. Wilson, and H. Mcneillie, "A Ferroelectric Nonvolatile Memory," *1988 IEEE Int. Solid-State Circuits Conf. 1988 ISSCC. Dig. Tech. Pap.*, pp. 130-131, 1988.
- [33] "Memory Technology", Barbara De Salvo, Livio Baldi, Nanoelectronics: Materials, Devices, Applications, 2 Volumes, John Wiley & Sons, 2017 .
- [34] S. Fukami, H. Sato, M. Yamanouchi, S. Ikeda, F. Matsukura, and H. Ohno, "Advances in spintronics devices for microelectronics - From spin-transfer torque to spin-orbit torque," *Proc. Asia South Pacific Des. Autom. Conf. ASP-DAC*, pp. 684–691, 2014.
- [35] R. Bez, "Chalcogenide PCM: A memory technology for next decade," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 89–92, 2009.
- [36] C. Villa, D. Mills, G. Barkley, H. Giduturi, S. Schippers, and D. Vimercati, "A 45nm 1Gb 1.8 V phase-change memory," *2010 IEEE International Solid-State Circuits Conference*, pp. 270–271, 2010.
- [37] H.-S. P. Wong *et al.*, "Phase Change Memory," *Proc. IEEE*, vol. 98, no. 12, pp. 2201–2227, 2010.
- [38] M. BrightSky, N. Sosa, T. Masuda, W. Kim, S. Kim, A. Ray, R. Bruce, J. Gonsalves, Y. Zhu, K. Suu, and C. Lam "Crystalline-as-deposited ALD phase change material confined PCM cell for high density storage class memory," *Tech. Dig. - 2015 Int. Electron Devices Meet. IEDM*, pp. 60-63, 2015.
- [39] T. C. Chong, L. P. Shi, R. Zhao, P. K. Tan, J. M. Li, H. K. Lee, X. S. Miao, A. Y. Du, and C. H. Tung, "Phase change random access memory cell with superlattice-like structure," *Appl. Phys. Lett.*, vol. 88, no. 12, pp. 1–4, 2006.
- [40] Y. Choi *et al.*, "A 20nm 1.8V 8Gb PRAM with 40MB/s program bandwidth," *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, pp. 46–47, 2012.
- [41] U. Russo, D. Ielmini, C. Cagli, and A. L. Lacaita, "Filament conduction and Reset mechanism in NiO-based resistive-switching memory (RRAM) devices," *IEEE Trans. Electron Devices*, vol. 56, no. 2, pp. 186–192, 2009.
- [42] D. Ielmini, F. Nardi, and C. Cagli, "Universal reset characteristics of unipolar and bipolar metal-oxide RRAM," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3246–3253, 2011.
- [43] A. Sawa, "Resistive switching in transition metal oxides," *Mater. Today*, vol. 11, no. 6, pp. 28–36, 2008.
- [44] A. Chen, "Area and thickness scaling of forming voltage of resistive switching memories," *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 57–59, 2014.
- [45] H. B. Lv, M. Yin, P. Zhou, T. A. Tang, B.A.Chen, Y.Y. Lin, A. Bao and M. H. Chi "Improvement of endurance and switching stability of forming-free  $\text{Cu}_x\text{O}$  RRAM," *2008 Jt. Non-Volatile Semicond. Mem. Work. Int. Conf. Mem. Technol. Des. Proceedings, NVSMWICMTD*, pp. 52–53, 2008.
- [46] Y.R. Chen, Y.C. Chen, Alfred T.H. Chuang, F.M. Lee, Y.Y. Lin, E.K. Lai, Y.H. Shih, K.Y. Hsieh, and Chih-Yuan Lu "A forming-free  $\text{WO}_x$  resistive memory using a novel self-aligned field enhancement feature with excellent reliability and scalability," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 440–443, 2010.

- [47] U. Russo, D. Jelmini, C. Cagli, A. L. Lacaita, S. Spigat, C. Wiemert, M. Peregog and M. Fanciullit, "Conductive-flament switching analysis and self-accelerated thermal dissolution model for reset in NiO-based RRAM," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 775–778, 2007.
- [48] S. Yu and H. S. P. Wong, "A phenomenological model for the reset mechanism of metal oxide RRAM," *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1455–1457, 2010.
- [49] B. Gao, S. Yu, N. Xu, L.F. Liu, B. Sun, X.Y. Liu, R.Q. Han, J.F. Kang, B. Yu and Y.Y. Wang, "Oxide-based RRAM switching mechanism: A new ion-transport-recombination model," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, 2008.
- [50] E. Vianello, C. Cagli, G. Molas, E. Souchier, P. Blaise, C. Carabasse, G. Rodriguez, V. Jousseau, B. De Salvo, F. Longnos, F. Dahmani, P. Verrier, D. Bretegnier and J. Liebault "On the impact of Ag doping on performance and reliability of GeS<sub>2</sub>-based conductive bridge memories," *2012 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, pp. 278 - 281, 2013.
- [51] W. Otsuka *et al.*, "A 4Mb conductive-bridge resistive memory with 2.3GB/s read-throughput and 216MB/s program-throughput," *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, pp. 210–211, 2011.
- [52] R. Waser, R. Dittmann, C. Staikov, and K. Szot, "Redox-based resistive switching memories nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, pp. 2632–2663, 2009.
- [53] B.Govoreanu, G.S.Kar, Y-Y.Chen, V.Paraschiv, S. Kubicek, A.Fantini, I.P.Radu, L.Goux, S.Clima, R.Degraeve, N.Jossart, O.Richard, T.Vandeweyer, K.Seo, P.Hendrickx, G. Pourtois, H.Bender, L.Altimime, D.J.Wouters, J.A.Kittl, M.Jurczak, "10×10nm<sup>2</sup> Hf/HfO<sub>x</sub> crossbar resistive RAM with excellent performance, reliability and low-energy operation," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 729–732, 2011.
- [54] E. Vianello, O. Thomas, G. Molas, O. Turkyilmaz, N. Jovanović, D. Garbin, G. Palma, M. Alayan, C. Nguyen, J. Coignus, B. Giraud, T. Benoist, M. Reyboz, A. Toffoli, C. Charpin, F. Clermidy, L. Perniola, "Resistive Memories for Ultra-Low-Power embedded computing design," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp.144-147, 2014.
- [55] B. Traoré, P. Blaise, E. Vianello, H. Grampeix, S. Jeannot, L.Perniola, B.DeSalvo,and Yoshio Nishi, "On the Origin of Low-Resistance State Retention Failure in HfO<sub>2</sub>-Based RRAM and Impact of Doping/Alloying," *IEEE Trans. Electron Devices*, vol. 62, no. 12, pp. 4029–4036, 2015.
- [56] S. Yu, X. Guan, and H.-S. Philip Wong, "On the stochastic nature of resistive switching in metal oxide RRAM: Physical modeling, Monte Carlo simulation, and experimental characterization," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 413–416, 2011.
- [57] S.Yu, B. Gao, H. Dai, B. Sun, L. Liu, X. Liu, R. Han, J. Kang, and B. Yu, "Improved Uniformity of Resistive Switching Behaviors in HfO<sub>2</sub> Thin Films with Embedded Al Layers," *Electrochem. Solid-State Lett.*, vol. 13, no. 2, pp. H36-H38, 2010.
- [58] J.Lee, J. Shin, D. Lee, W. Lee, S. Jung, M. Jo, J. Park, K. P. Biju, S. Kim, S. Park and H.Hwang "Diode-less nano-scale ZrO<sub>x</sub>/HfO<sub>x</sub> RRAM device with excellent switching uniformity and reliability for high-density cross-point memory applications," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 452–455, 2010.

- [59] M. Yin, P. Zhou, H. B. Lv, J. Xu, Y. L. Song, X. F. Fu, T. A. Tang, B. A. Chen, and Y. Y. Lin, "Improvement of Resistive Switching in  $\text{Cu}_x\text{O}$  Using New RESET Mode," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 681–683, 2008.
- [60] Y. Y. Chen *et al.*, "Balancing SET/RESET Pulse for  $>10^{10}$  Endurance in  $\text{HfO}_2/\text{Hf}$  1T1R Bipolar RRAM," *IEEE Trans. Electron Devices*, vol. 59, no. 12, pp. 3243–3249, 2012.
- [61] Y. Y. Chen *et al.*, "Understanding of the endurance failure in scaled  $\text{HfO}_2$ -based 1T1R RRAM through vacancy mobility degradation," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 482–485, 2012.
- [62] B. Chen, Y. Lu, B. Gao, Y.H. Fu, F.F. Zhang, P. Huang, Y.S. Chen, L.F. Liu, X.Y. Liu, J.F. Kang, Y.Y. Wang, Z. Fang, H.Y. Yu, X. Li, X.P. Wang, N. Singh, G. Q. Lo, D. L. Kwong, "Physical mechanisms of endurance degradation in TMO-RRAM," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 283–286, 2011.
- [63] H. Y. Lee, Y. S. Chen, P. S. Chen, P. Y. Gu, Y. Y. Hsu, S. M. Wang, W. H. Liu, C. H. Tsai, S. S. Sheu, P. C. Chiang, W. P. Lin, C. H. Lin, W. S. Chen, F. T. Chen, C. H. Lien, and M.-J. Tsai, "Evidence and solution of over-RESET problem for  $\text{HfO}_x$  based resistive memory with sub-ns switching speed and high endurance," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 460–463, 2010.
- [64] Y. Y. Chen *et al.*, "Improvement of data retention in  $\text{HfO}_2/\text{Hf}$  1T1R RRAM cell under low operating current," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 252–255, 2013.
- [65] H. Y. Lee, Y. S. Chen, P. S. Chen, T. Y. Wu, F. Chen, C. C. Wang, P. J. Tzeng, M.-J. Tsai, and C. Lien, "Low-power and nanosecond switching in robust hafnium oxide resistive memory with a thin Ti cap," *IEEE Electron Device Lett.*, vol. 31, no. 1, pp. 44–46, 2010.
- [66] S. Gerardin, M. Bagatin, A. Paccagnella, K. Grürmann, F. Gliem, T. R. Oldham, F. Irom, and D. N. Nguyen "Radiation Effects in Flash Memories," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1953–1969, 2013.
- [67] D. Chen *et al.*, "Single-event effect performance of a commercial embedded rram," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3088–3094, 2014.
- [68] L. Zhang, "Study of the Selector Element for Resistive Memory," Thesis. October, 2015.
- [69] R. Aluguri and T.-Y. Tseng, "Overview of Selector Devices for 3-D Stackable Cross Point RRAM Arrays," *Journal of the electron devices society*, vol. 4, no. 5, pp. 294–306, 2016.
- [70] I. G. Baek, C. J. Park, H. Ju, D. J. Seong, H. S. Ahn, J. H. Kim, M. K. Yang, S. H. Song, E. M. Kim, S. O. Park, C. H. Park, C. W. Song, G. T. Jeong, S. Choi, H. K. Kang, and C. Chung, "Realization of vertical resistive memory (VRRAM) using cost effective 3D process," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 737–740, 2011.
- [71] H. S. Yoon *et al.*, "Vertical cross-point resistance change memory for ultra-high density non-volatile memory applications," *2009 Symp. VLSI Technol.*, pp. 26–27, 2009.
- [72] L. Zhang *et al.*, "High-drive current ( $>1\text{MA}/\text{cm}^2$ ) and highly nonlinear ( $>10^3$ )  $\text{TiN}/\text{amorphous-Silicon}/\text{TiN}$  scalable bidirectional selector with excellent reliability and its variability impact on the 1S1R array performance," *Tech. Dig. - 2014 Int. Electron Devices Meet. IEDM*, pp. 164–167, 2014.
- [73] B. Govoreanu, L. Zhang, and M. Jurczak, "Selectors for high density crosspoint memory arrays: Design considerations, device implementations and some challenges ahead," *2015 Int. Conf. IC Des. Technol. ICICDT 2015*.

- [74] G.W. Burr, R. S. Shenoy, K. Virwani, P. Narayanan, A. Padilla, and B.Kurd, "Access devices for 3D crosspoint memory," *J. Vac. Sci. Technol. B*, vol. 32, no. 4, p. 40802, 2014.
- [75] J. H. Oh *et al.*, "Full integration of highly manufacturable 512Mb PRAM based on 90nm technology," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 8–11, 2006.
- [76] V. S. S. Srinivasan, S. Chopra, P. Karkare, P. Bafna, S. Lashkare, P. Kumbhare, Y. Kim, S. Srinivasan, S. Kuppurao, S. Lodha, and U. Ganguly, "Punchthrough-diode-based bipolar RRAM selector by Si epitaxy," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1396–1398, 2012.
- [77] B. S. Kang *et al.*, "High-current-density  $\text{CuO}_x/\text{InZnO}_x$  thin-film diodes for cross-point memory applications," *Adv. Mater.*, vol. 20, pp. 3066–3069, 2008.
- [78] M. J. Lee *et al.*, "A low-temperature-grown oxide diode as a new switch element for high-density, nonvolatile memories," *Adv. Mater.*, vol. 19, pp. 73–76, 2007.
- [79] I. G. Baek, D. C. Kim, M. J. Lee, H.-J. Kim, E. K. Yim, M. S. Lee, J. E. Lee, S. E. Ahn, S. Seo, J. H. Lee, J. C. Park, Y. K. Cha, S. O. Park, H. S. Kim, I. K. Yoo, U-In Chung, J. T. Moon and B. I. Ryu, "Multi-layer cross-point binary oxide resistive memory (OxRRAM) for post-NAND storage application," *IEEE Int. Devices Meet. 2005. IEDM Tech. Dig.*, pp. 750–753, 2005.
- [80] M. J. Lee *et al.*, "2-Stack ID-IR cross-point structure with oxide diodes as switch elements for high density resistance RAM applications," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 771–774, 2007.
- [81] S. Ahn, B. S. Kang, K. H. Kim, M.-J. Lee, C. B. Lee, G. Stefanovich, C. J. Kim, and Y. Park, "Stackable All-Oxide-Based Nonvolatile Memory With  $\text{Al}_2\text{O}_3$  Antifuse and p- $\text{CuO}_x$  /n- $\text{InZnO}_x$  Diode," *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 550–552, 2009.
- [82] K. K. Likharev, "Layered tunnel barriers for nonvolatile memory devices," *Appl. Phys. Lett.*, vol. 73, no. 15, pp. 2137–2139, 1998.
- [83] E. Cimpoiasu, S. K. Tolpygo, X. Liu, N. Simonian, J. E. Lukens, K. K. Likharev, R. F. Klie, and Y. Zhu, "Aluminum oxide layers as possible components for layered tunnel barriers," *J. Appl. Phys.*, vol. 96, no. 2, pp. 1088–1093, 2004.
- [84] S. Park *et al.*, "A Non-Linear ReRAM Cell with sub-1 $\mu\text{A}$  Ultralow Operating Current for High Density Vertical Resistive Memory (VRRAM)," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 501–504, 2012.
- [85] U. Chand, K. C. Huang, C. Y. Huang, and T. Y. Tseng, "Mechanism of Nonlinear Switching in  $\text{HfO}_2$ -Based Crossbar RRAM With Inserting Large Bandgap Tunneling Barrier Layer," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3665–3670, 2015.
- [86] H. D. Lee *et al.*, "Integration of 4F2 selector-less crossbar array 2Mb ReRAM based on transition metal oxides for high density memory applications," *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. 151–152, 2012.
- [87] B. Govoreanu *et al.*, "Vacancy-Modulated Conductive Oxide Resistive RAM (VMCO-RRAM): An Area-Scalable Switching Current, Self-Compliant, Highly Nonlinear and Wide On/Off-Window Resistive Switching Cell," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 256–259, 2013.
- [88] R. S. Shenoy *et al.*, "MIEC (mixed-ionic-electronic-conduction)-based access devices for non-volatile crossbar memory arrays," *Semicond. Sci. Technol.*, vol. 29, no. 10, p. 104005, 2014.

- [89] K. Gopalakrishnan *et al.*, “Highly-scalable novel access device based on Mixed Ionic Electronic conduction (MIEC) materials for high density phase change memory (PCM) arrays,” *Symposium on VLSI Technology Digest of Technical Papers (VLSIT)*, pp. 205–206, 2010.
- [90] K. Virwani, G.W. Burr, R. S. Shenoy, C. T. Rettner, A. Padilla, T. Topuria, P. M. Rice, G. Ho, R. S. King, K. Nguyen, A. N. Bowers, M. Jurich, M. BrightSky, E.A. Joseph, A. J. Kellock, N. Arellano, B. N. Kurdi and K. Gopalakrishnan, “Sub-30nm scaling and high-speed operation of fully-confined Access-Devices for 3D crosspoint memory based on Mixed-Ionic-Electronic-Conduction (MIEC) Materials,” *IEDM, Tech. Dig. - Int. Electron Devices Meet.*, pp. 36–39, 2012.
- [91] S. R. Ovshinsky, “Reversible electrical switching phenomena in disordered structures,” *Phys. Rev. Lett.*, vol. 21, no. 20, pp. 1450–1453, 1968.
- [92] D. Adler, H. K. Henisch, and S. N. Mott, “The mechanism of threshold switching in amorphous alloys,” *Rev. Mod. Phys.*, vol. 50, no. 2, pp. 209–220, 1978.
- [93] D. M. Kroll, “Theory of electrical instabilities of mixed electronic and thermal origin. II. Switching as a nucleation process,” *Physical Review B*, vol. 11, no. 10, 1975.
- [94] D. Adler, M. S. Shur, M. Silver, and S. R. Ovshinsky, “Threshold switching in chalcogenide-glass thin films,” *J. Appl. Phys.*, vol. 51, no. 6, pp. 3289–3309, 1980.
- [95] D. Ielmini, “Threshold switching mechanism by high-field energy gain in the hopping transport of chalcogenide glasses,” *Phys. Rev. B*, vol. 78, 2008.
- [96] H. Yang *et al.*, “Novel selector for high density non-volatile memory with ultra-low holding voltage and  $10^7$  on/off ratio,” *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. T130–T131, 2015.
- [97] Y. Koo, K. Baek, and H. Hwang, “Te-Based Amorphous Binary OTS Device with Excellent Selector Characteristics for X-point Memory Applications,” *Symposium on VLSI Technology Digest of Technical Papers*, 2016.
- [98] J. Seo, H. W. Ahn, S. Y. Shin, B. K. Cheong, and S. Lee, “Anomalous reduction of the switching voltage of Bi-doped  $\text{Ge}_{0.5}\text{Se}_{0.5}$  ovonic threshold switching devices,” *Appl. Phys. Lett.*, vol. 104, no. 15, 2014.
- [99] M. J. Lee *et al.*, “Highly-scalable threshold switching select device based on chalcogenide glasses for 3D nanoscaled memory arrays,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 33–35, 2012.
- [100] D. Kau *et al.*, “A stackable cross point phase change memory,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 617–620, 2009.
- [101] M. Imada, A. Fujimori, and Y. Tokura, “Metal-insulator transitions,” *Rev. Mod. Phys.*, vol. 70, no. 4, pp. 1039–1263, 1998.
- [102] M. Son *et al.*, “Excellent selector characteristics of nanoscale  $\text{VO}_2$  for high-density bipolar ReRAM applications,” *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1579–1581, 2011.
- [103] S. Kim *et al.*, “Ultrathin ( $<10\text{nm}$ )  $\text{Nb}_2\text{O}_5/\text{NbO}_2$  hybrid memory with both memory and selector characteristics for high density 3D vertically stackable RRAM applications,” *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. 155–156, 2012.
- [104] S. H. Jo, T. Kumar, S. Narayanan, W. D. Lu, and H. Nazarian, “3D-stackable crossbar resistive memory based on Field Assisted Superlinear Threshold (FAST) selector,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 160–163, 2014.

# Chapter 2

## Characterization and modeling of HfO<sub>2</sub> based RRAM cells

### 2.1 Introduction

**A**mong different binary oxides investigated as switching materials for RRAM cells, HfO<sub>2</sub> is very attractive due to the compatibility with the advanced CMOS process and good switching properties [1]. In this chapter, we present the process details of the fabricated HfO<sub>2</sub> based RRAM cells. Both single cells (1R) and one transistor/one resistor (1T1R) test structures were characterized to access basic memory operations (Forming, Set and Reset process) and reliability issues.

In order to study the kinetics of the Forming process at the microscopic level, we have performed physics based simulations using the Ginestra simulation package [2]. The model takes into account the charge/ion transport and the material structural modifications (i.e. CF creation/rupture in the dielectric layer) associated with the RRAM operations.

### 2.2 Process details

#### 2.2.1 Memory structure

RRAM cells are composed of an insulating oxide material sandwiched between two metal electrodes (metal–insulator–metal, MIM, structure). They are generally integrated in the Back-End-Of-Line (BEOL) of a CMOS process. Figure 2.1 shows

the fabricated and tested 1R (a) and 1T1R (b) samples. In the case of 1T1R structure, the bottom electrode (BE) of the cell is connected to the drain of NMOS transistor. The memory cell active area is defined by the cross point between the two metal lines (M1 and M2) as shown in Figure 2.1-c.

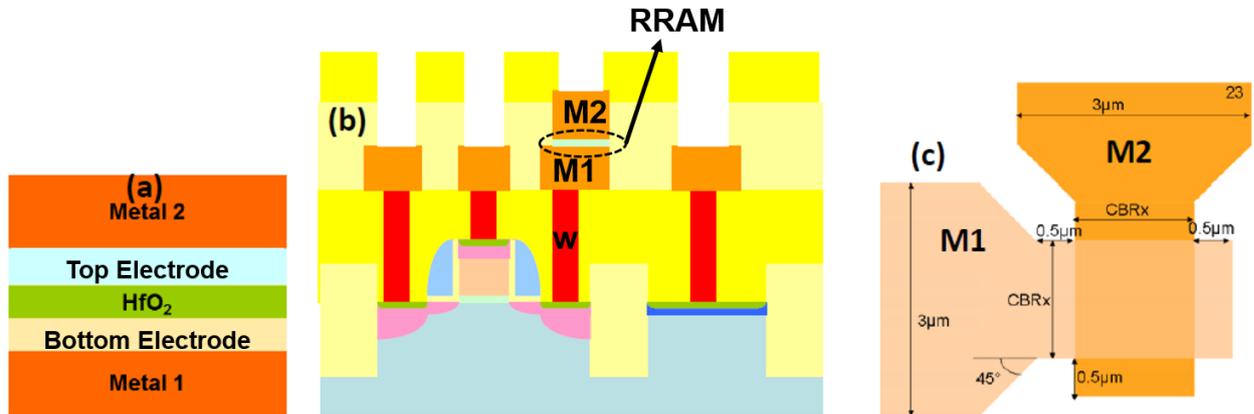


Figure 2.1: Schematics of (a) 1R MIM structure capacitor integrated between Metal 1 (M1) and Metal 2 (M2), (b) 1T1R structure, (c) crossbar integration of the memory cell between the two metal lines. Devices are fabricated in CEA-Leti.

## 2.2.2 Integration flow

Figure 2. 2 shows the main steps of HfO<sub>2</sub> based RRAM fabrication process starting from M1 level:

(a) M1 is composed of 10-nm Ti, 440-nm AlCu, 10-nm Ti and 100-nm TiN. M1 is deposited by physical vapor deposition (PVD). Ti and TiN layers are deposited at 350°C and AlCu is deposited at 440°C. The two layers of Ti and TiN are used to better grip the M1 with the W via and the memory cell. The TiN layer serves as bottom electrode of the memory cell (Figure 2. 2-a).

(b) The HfO<sub>2</sub> binary-metal oxide is the active layer of the memory cell. HfO<sub>2</sub> is deposited by atomic layer deposition (ALD) at 300°C. The precursors used during the deposition are HfCl<sub>4</sub> and H<sub>2</sub>O. The top electrode is composed of 10-nm of Ti followed by 50-nm of TiN deposited by PVD (Figure 2. 2-b).

(c) Similar to M1, the M2 consisted of 10-nm Ti, 440-nm AlCu, 10-nm Ti and 50-nm TiN is deposited by PVD (Figure 2. 2-c).

(d) Finally, an etching step is carried-out on M2 and the active materials to define the memory cell (Figure 2. 2-d).

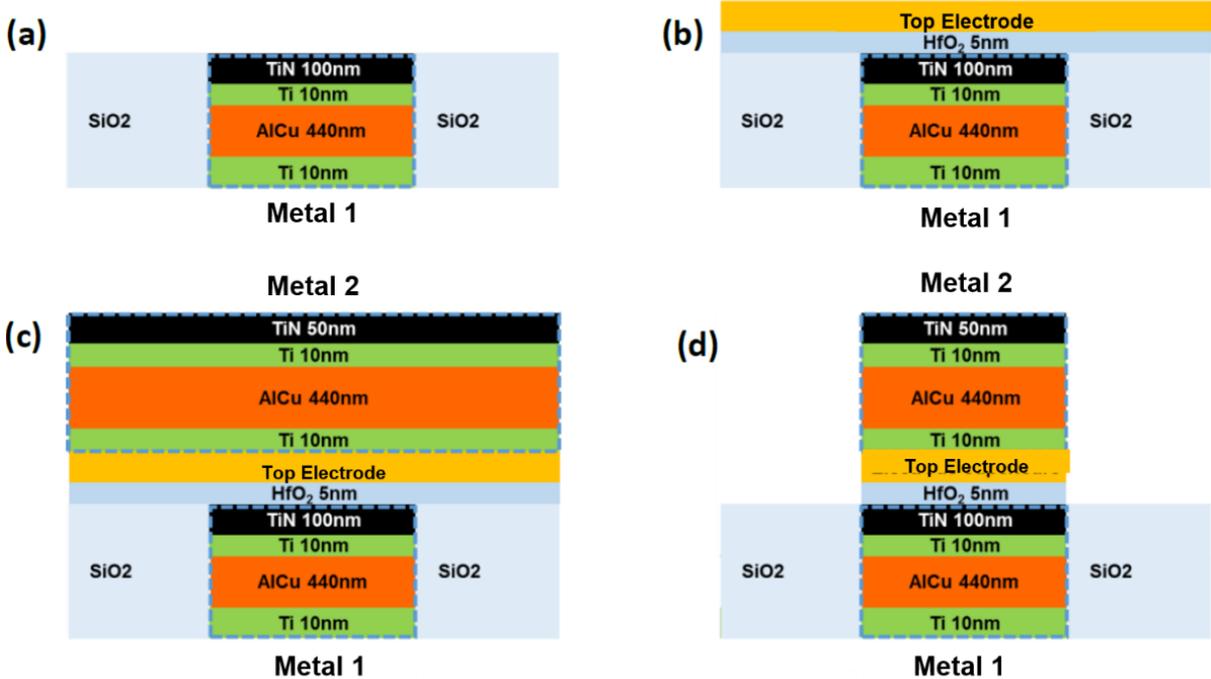


Figure 2. 2 : Schematic of the main fabrication steps of HfO<sub>2</sub> based RRAM cell.

## 2.3 Electric test methodology of a memory cell

### 2.3.1 Cells programming with ramped voltage

The programming operations (Forming/Reset/Set) in ramped mode were performed using the HP4156 semiconductor parameter analyzer. The voltage ramp (~1V/s) is applied on the top electrode of the 1R or 1T1R memory cells. The parameter analyzer allows to apply the voltage at the same time to measure the current flowing through the cell as shown in Figure 2.3-a. This simple method allows to check the functionality of the memory cell and to extract the programming parameters from the voltage-current characteristics (e.g. switching voltages, current levels before and after switching, etc.).

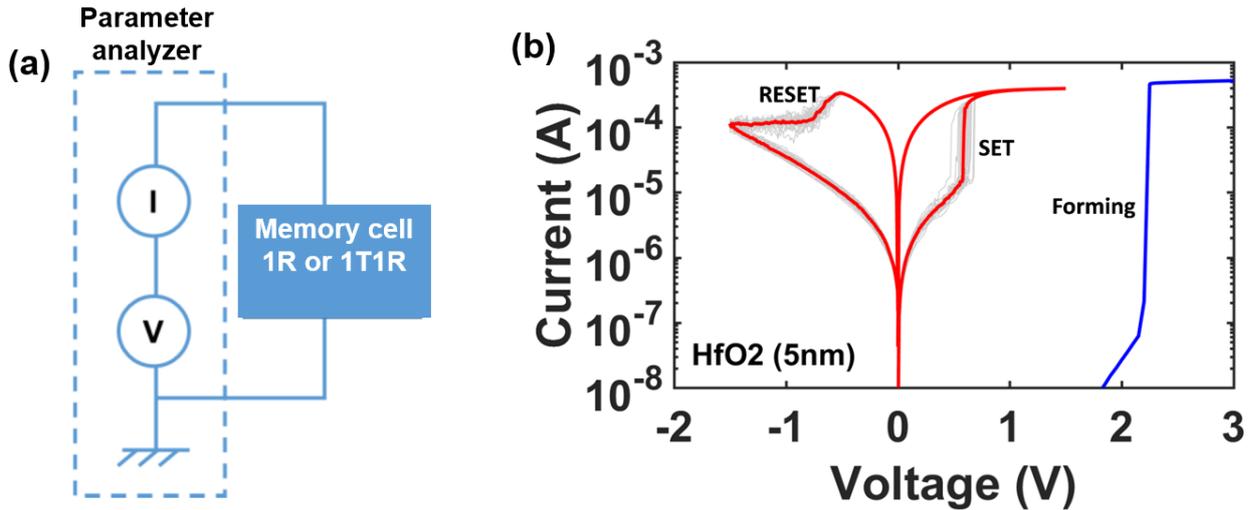


Figure 2.3 : (a) Schematic of the ramp mode measurement Setup, (b) I-V characteristics of 5-nm thick HfO<sub>2</sub> during Forming/Reset/Set operations.

Since the memory devices are bipolar, a positive voltage ramp is applied on the top electrode during Forming and Set operations, whereas a negative ramp is applied on the top for the Reset operation. The access transistor allows to limit the current during the Forming and Set operations where the programming current level is modulated by the gate voltage. An example of I-V characteristics of Forming Reset and Set are shown in Figure 2.3-b.

### 2.3.2 Read operation

The resistance reading of the memory cell is obtained by applying a voltage ramp and measuring the current at the same time. The stop voltage of the read ramp must be low enough to avoid any disturb of the resistance state. Typically, a voltage ramp ranging from 0 to 100mV is used to read the resistance of the memory cell. The resistance value is extracted using Ohm's law:

$$R = \frac{U}{I}$$

From the I-V characteristics, a linear fit is performed to extract the resistance value of the memory cell as accurately as possible. Figure 2.4 shows an example of LRS read.

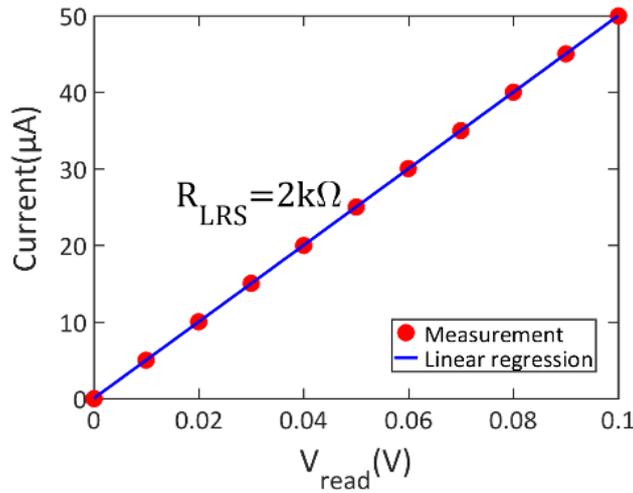


Figure 2.4 : I-V characteristics during read operation for 5-nm HfO<sub>2</sub> based RRAM. Resistance is extracted by linear regression

### 2.3.3 Cells programming in pulse mode

In addition to the ramped voltage programming mode, the memory devices can be programmed (Forming-Set/Reset) by the application of voltage pulses. The characteristics of the applied pulses (e.g. amplitude, width, rise/fall times, etc.) depend on the devices under test properties (e.g. the oxide material, electrodes materials, active layer thicknesses, etc.). The programming pulses are controlled by “Pulsed IV” modules (PIV) that can send and control the pulses with a sampling rate down to 5ns. Figure 2. 5 shows the pulse sequence used during memory cycling in pulse mode. After every programming pulse, a read operation is performed with a pulse of 100mV as amplitude. The current flowing through the memory cell is measured at several points during the read pulse. The resistance is then calculated using Ohm's law by averaging all the current measurements that have been acquired. Using the pulse mode measurement setup that we have developed we are able to perform ultra-fast endurance tests. 10<sup>6</sup> endurance cycles (Set-Reset + Read) with 10µs pulses width can be done in 40 seconds. Figure 2. 6 shows an example of 10 million endurance cycles on 5-nm thick HfO<sub>2</sub> based RRAM.

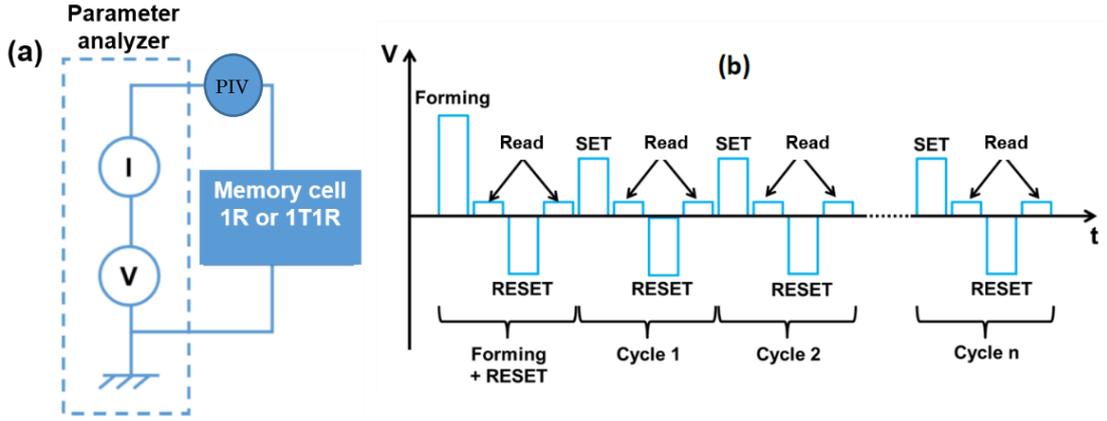


Figure 2. 5 : (a) Schematic of the pulse mode measurement setup, (b) Pulse sequence during memory cycling in pulse mode, read operation is done after every programming pulse (Forming/ Reset/ Set).

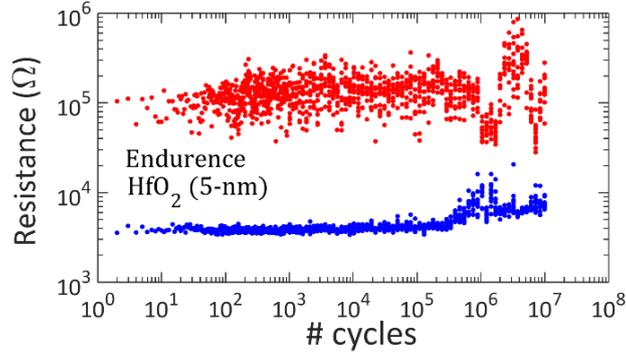


Figure 2. 6 : Endurance test of 5-nm thick HfO<sub>2</sub> based RRAM using the pulse mode measurement setup with fixed pulse conditions: Set: 2V, 10μs; Reset: 1.4V, 10μs. 10<sup>7</sup> cycles have been achieved.

## 2.4 Modeling and simulation

In this section, we will focus on the Forming process of our HfO<sub>2</sub> based RRAM presented in the previous sections of this chapter. We will investigate the: (i) kinetics of this process, (ii) dependence on voltage/temperature/material properties and (iii) characteristics of the conductive filament using the “Ginestra” model. The model is a physics-based simulation package, which takes into account the charge/ion transport and the material structural modifications (CF creation/rupture in the dielectric layer) associated with the RRAM operations.

### 2.4.1 Ginestra model

Understanding the implications of the physical mechanisms responsible for defect creation at microscopic level (e.g. bond breakage) during the formation/rupture of the conductive filament (CF), requires a multiscale modeling framework combining ab-initio calculations (i.e. DFT) with dielectric-focused device simulations.

The Ginestra modeling framework includes several modules, which allow self-consistently describing the main physical mechanisms occurring in binary oxide materials when subjected to an electrical stress. The device-level description exploits the output generated by ab-initio calculations, which explicitly considers the oxide material specific characteristics.

The charge transport is modeled by including a variety of conduction mechanisms (relevant in dielectrics) such as direct tunneling, defect assisted contributions such as the multi-phonon Trap-Assisted-Tunneling (TAT) [2], and drift/diffusion across either the conduction/valence band and sub-bands created by the high density of defects. The defect properties, i.e. the thermal ionization and relaxation energies calculated using the DFT [3] are used for the calculation of TAT defect assisted current contributions accounting for the electron-phonon coupling [2]. The current is calculated within the whole device volume consistent with the local potential and temperature, calculated from the power dissipation associated with the charge transport by solving the Fourier's heat flow equation. In order to reproduce the microscopic material modifications occurring during BD and the kinetics of the process, the model purposely accounts for the description of the atomistic processes leading to creation of new defects, i.e. mainly oxygen vacancies due to the rupture of Metal-O bonds. The defect generation rates of defect creation processes are implemented using the thermochemical model (described in the next section) which accounts for the local field and temperature [4], [5]. This allows consistently modeling the field- and temperature-driven feedback occurring during the BD process: the creation of new defects increases the leakage current, which in turn increases the power dissipation, the temperature and the local defect creation rate. Once the BD conditions (i.e. the presence of a minimal defect cluster) are reached, a very fast acceleration of the defect creation process occurs, which culminates in the formation of a highly-deficient filament responsible for the abrupt current increase. The stochastic nature of this process is reproduced using the Monte-Carlo method

for determining the positions of the new defects that are created. The field- and temperature-driven motion of ion and vacancy species is also included.

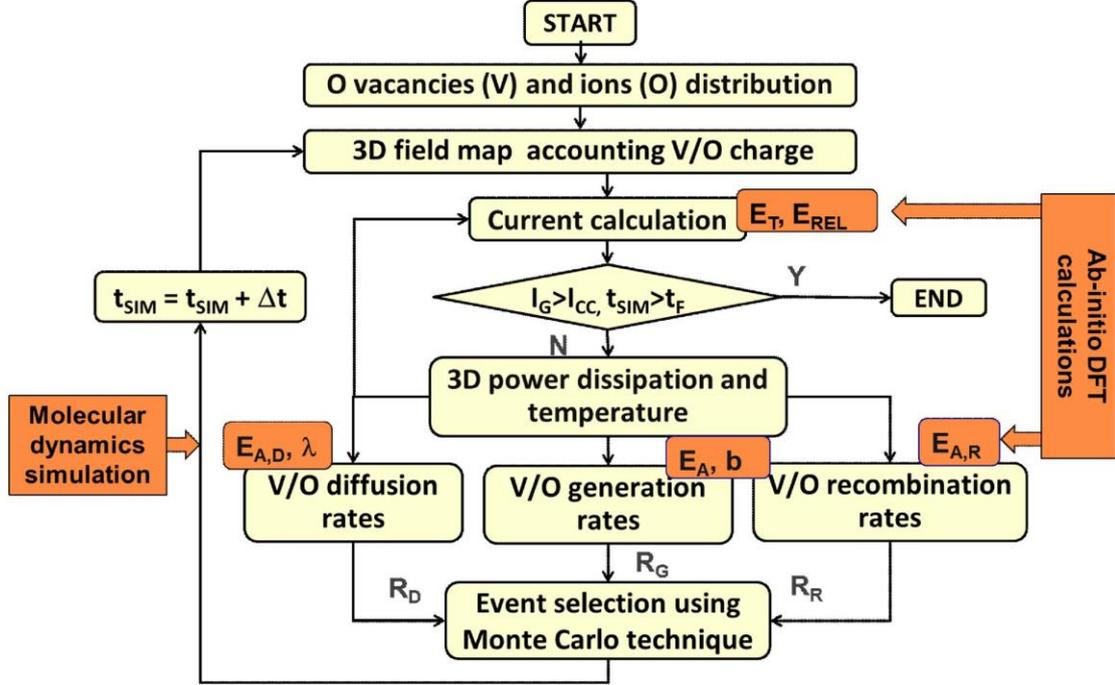


Figure 2. 7 : Flow chart of the multi-scale simulation framework. The yellow boxes refer to the dielectric-focused device simulations, while the orange ones represent the DFT-cased calculations of defect properties and defect creation processes and the diffusion properties provided by molecular dynamics simulation.

The material properties such as the dielectric constant, the optical band gap and the O-Metal bond vibration frequency are taken into account as well during the simulation.

We used this multi-scale model to understand the key features of the material-dependent microscopic processes leading to defect creation in  $\text{HfO}_2$ . The microscopic mechanisms responsible for the defect creation are investigated using density functional theory (DFT) calculations, (Orange boxes in the flow chart in Figure 2. 7), which are used to calculate the activation energies and field acceleration factor for the defect generation process. Such values are then used for the simulation of the kinetic of the BD process, which are represented by the yellow boxes in the flow chart in Figure 2. 7.

## 2.4.2 Thermochemical model

The thermochemical model describes accurately the BD process and the time-dependent dielectric breakdown (TDDB) in thin dielectric films. Atomic bonds can be broken by thermal means due to the strong dipolar coupling with the local electric field in the dielectric. The dipole-field coupling serves to lower the activation energy required for thermal bond-breakage and accelerates the dielectric degradation process [4], [6].

Forming process is dominated by the generation rate of oxygen vacancy/ion pairs (G), which is modeled in the framework of the thermochemical model as follow:

$$G = G_0 \exp\left(-\frac{E_a - b * F}{K_B T}\right) \quad (2.1)$$

$E_a$  is the activation energy to break a bond at zero field,  $K_B$  is the Boltzmann's constant,  $G_0$  is the effective vibration frequency of Hf-O bonds  $\sim 7 \cdot 10^{13}$  Hz,  $F$  is the electric field,  $T$  is the temperature and  $b$  is the bond polarization factor [4].

The bond polarization factor  $b$  is given by:

$$b = P_0 \left(\frac{2 + K}{3}\right) \quad (2.2)$$

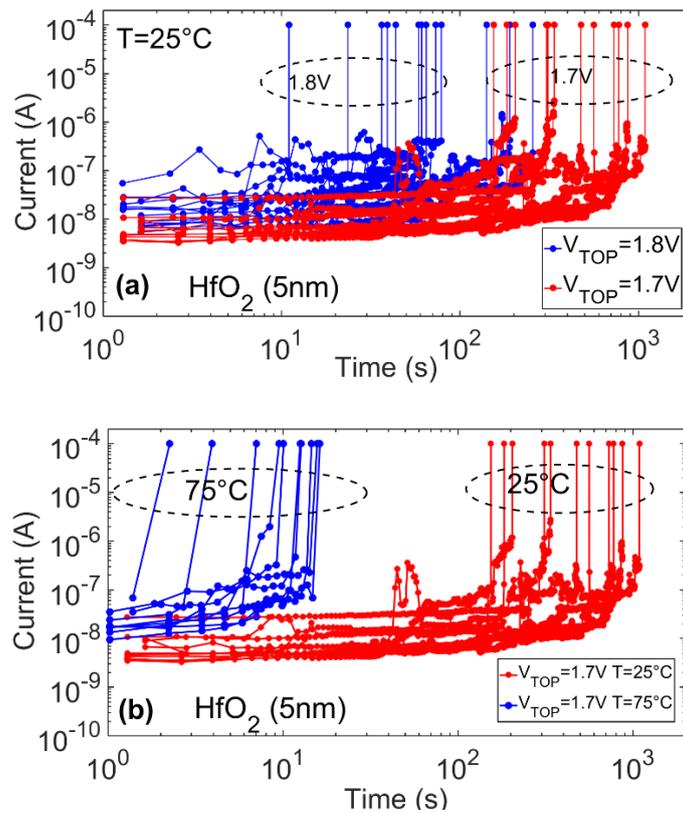
where  $P_0$  is the molecular dipole moment mainly originated by polar molecular components and opposite to the local field. This parameter can be determined from the local metal-ion environment/symmetry and the metal-oxygen bond length in the lattice.  $K$  is the dielectric constant [4].

## 2.4.3 TDDB measurements

To investigate the bond breaking mechanisms responsible for the Forming process, we stressed our reference samples, the TiN/Ti/HfO<sub>2</sub>(5-nm)/TiN, with constant voltage stress (CVS) at different voltage amplitudes and temperatures. The corresponding current vs time curves are shown in Figure 2. 8.

Current shows the typical evolution observed during breakdown (BD) experiments: after a slight increase due to a gradual/slow generation of oxygen vacancy defects, the current shows an abrupt jump due to the formation of a highly oxygen deficient conductive filament.

The abruptness of the process is the result of temperature- and field-induced positive feedback loop established after the formation of a critical defect cluster, which leads to the exponential increase of the current. This latter can be interrupted only by limiting the maximum current through the device. The breakdown process was shown to be accelerated by the temperature and the applied voltage.



*Figure 2. 8 : I-t curves measured on 5-nm thick HfO<sub>2</sub>. (a) I-t characteristics at ambient temperature with different constant applied voltages (1.7V and 1.8V), (b) I-t characteristics at different temperatures (25°C and 75°C) with constant applied voltage of 1.7V.*

### 2.4.3.1 Extraction of microscopic properties

Figure 2. 9 shows the average of the TDDB data (reported in Figure 2. 8) at different temperatures and different electric field.

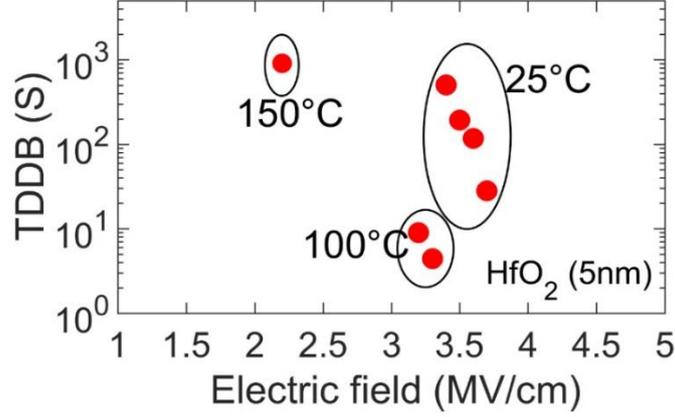


Figure 2. 9 : TDDB data for 5-nm HfO<sub>2</sub> at different temperatures and different applied electric field for each temperature. Every data point corresponds to the average of TDDB extracted from I-t characteristics for 12 devices (Figure 2. 8).

The atomic bond properties ( $E_a$  and  $b$  in the equation (2.1)) involved in the generation mechanism of oxygen vacancy/ion pairs can be extracted from TDDB data measured at different temperatures assuming that TDDB is proportional to the inverse of the generation rate (TDDB  $\sim G^{-1}$ ). This allows rewriting equation (2.1) as following:

$$E_{aeff} = -K_B * T * \ln\left(\frac{1}{TDDB * G_0}\right) \quad (2.3)$$

And

$$E_{aeff} = E_a - b * F \quad (2.4)$$

$E_{aeff}$  is the effective activation energy required to break a bond in the presence of electric field.  $E_{aeff}$  is first calculated by applying the equation (2.3) on the data reported in Figure 2. 9.  $K_B$ , and  $G_0$  are constant values, different  $E_{aeff}$  is calculated for different TDDB values measured at different temperatures (data in Figure 2. 9). For each value of electric field, a corresponding  $E_{aeff}$  is calculated. The bond polarization factor ( $b$ ) and  $E_a$  are then extracted using the equation (2.4) by interpolating the effective activation energies measured at different temperatures and different electric fields, as shown in Figure 2. 10.  $b$  is the slope and  $E_a$  is the constant in the equation of the interpolated line ( $E_{aeff}$  vs Field). Finally,  $P_0$  is calculated using the equation (2.2).

$$E_{aeff} = E_a - b * F \quad (2.4)$$

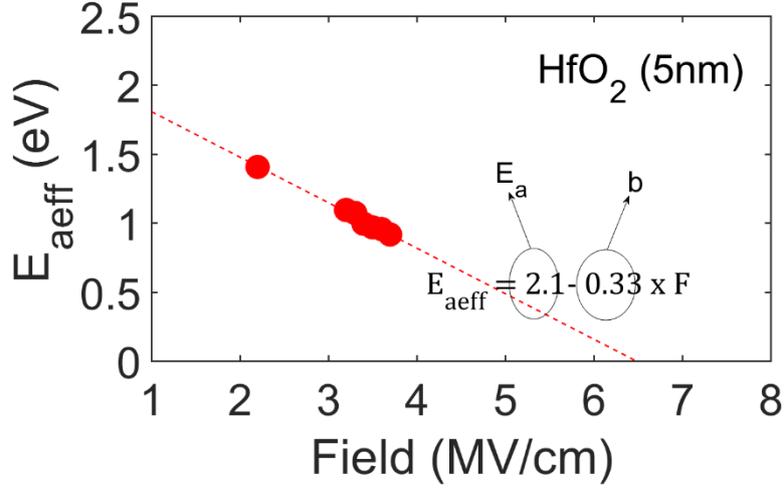


Figure 2. 10 : Extraction method of  $E_a$  and  $P_0$  using equation (2.4).

The parameters extracted for HfO<sub>2</sub> material are reported in Table 2. 1. The dielectric constant  $K$  is derived from C-V measurements.

Table 2. 1: Extracted parameters from TDDB and CV measurements for 5-nm thick HfO<sub>2</sub> based RRAM cells.

Parameter	HfO <sub>2</sub>
$E_a$ (eV)	2.1
$P_0$ (e-Å)	4.3
$K$	22

## 2.4.4 Simulation results

### 2.4.4.1 TDDB simulation

In order to verify the accuracy of the extracted parameters and to investigate the kinetics of Forming and TDDB phenomena of the studied samples we performed first the HfO<sub>2</sub> TDDB simulation using the parameters reported in Table 2. 1. The time to breakdown is considered as the time at which the current jumps abruptly from leakage level (tens of nA) up to the defined compliance current (few  $\mu$ A). TDDB

simulations were shown to reproduce the dependence on temperature and electric field of the experimental TDDB data on 5-nm HfO<sub>2</sub> (data presented in section 2.4.3). Figure 2. 11 shows the probability distributions of the experimental and simulation data of TDDB for 5-nm HfO<sub>2</sub> at different temperatures and different applied electric fields. The model reproduces accurately the TDDB distributions by considering an activation energy range of :

$$\text{Extracted } (E_a) - 0.1\text{eV} < E_a < \text{Extracted } (E_a) + 0.1 \text{ eV}$$

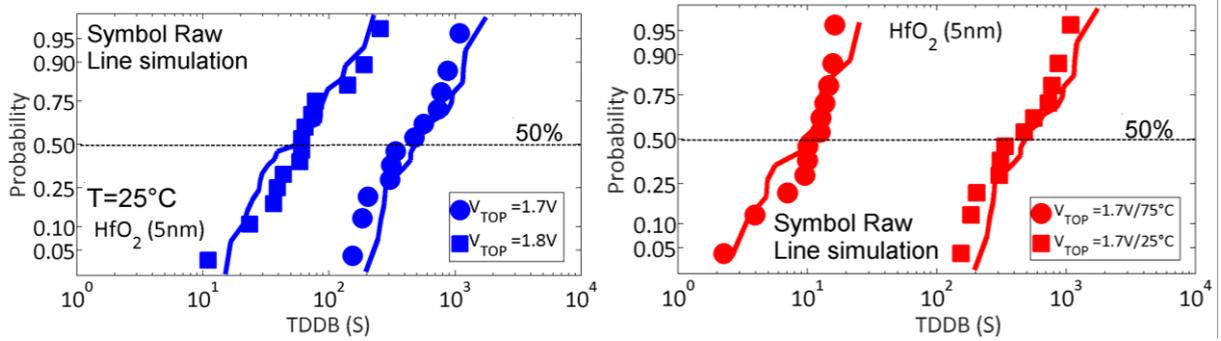


Figure 2. 11 : TDDB simulation with electric field dependence (left) and temperature dependence (right).

#### 2.4.4.2 Pre-Forming leakage current simulation

Before the Forming event (pre-Forming leakage current) the charge transport is dominated by the multiphonon trap-assisted tunneling (TAT) through positively charged oxygen vacancies that exist in the oxide layer [6]. Defect properties such as the relaxation energy ( $E_{rel}$ ), thermal ionization energy ( $E_{th}$ ) and defects density in the pristine state, strongly affect the pre-Forming leakage current characteristics. The  $E_{rel}$  and  $E_{th}$  calculated by ab-initio methods [3] are the defects properties that control the charge capture and emission processes and set the temperature dependence of the TAT current. The parameters used in pre-Forming leakage simulation that we have performed are reported in Table 2. 2. In our study the devices area is 1 $\mu\text{m}^2$ . The area of the simulated devices is 100nm<sup>2</sup> to avoid a huge number of defects in the device model, therefore an infinite simulation time. As consequence, the current density should be adopted to compare the experimental data with simulation results.

Table 2. 2: Defects properties used in pre-Forming leakage current simulation

Defects parameters	Description	Calculation method	Value
$E_{Rel}$	Relaxation energy of an isolated defect	DFT	1eV [3]
$E_T$	Thermal ionization energy of a defect	DFT	2.1eV [3]
$\rho$	Defect density in pristine state	DFT	$10^{20} \text{ cm}^{-3}$ [7]

Figure 2.12 shows the leakage current dependence on temperature. The current density increases with temperature, these results are in agreement with the TAT conduction mechanism that is activated by temperature. The simulation reproduces accurately the experimental results and the dependence on temperature by using the defects properties reported in Table 2. 2.

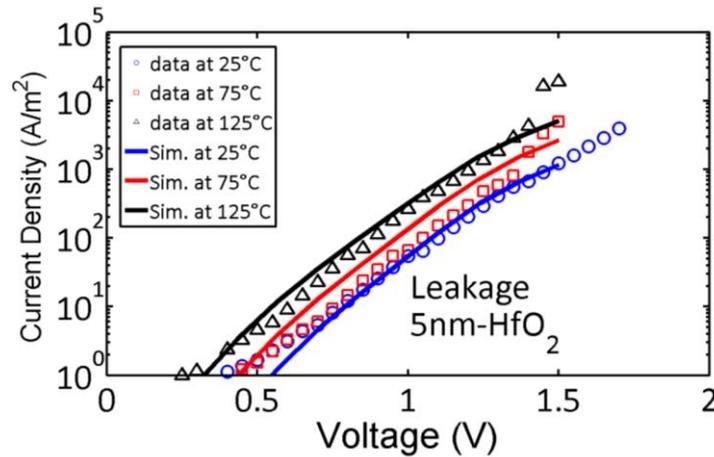


Figure 2.12 : Pre-Forming leakage current at different temperatures (25°C, 75°C and 125°C). Symbols experimental data, solid lines simulation.

### 2.4.4.3 Forming simulation

For the switching event between pristine state and LRS,  $E_a$  and  $P_0$ , are the main physical parameters that define the critical electric field at which the switching occurs. These parameters were extracted from TDDDB data as discussed in section 2.4.3.1. The material properties such as the dielectric constant, the optical band gap and the O-Hf bond vibration frequency that we consider during the Forming simulation are reported in Table 2. 3.

Table 2. 3: Material properties used in Forming simulation

Material parameters	Description	Extraction method	Value
$k$	Dielectric constant	C-V measurements	22 [8]
$U$	O-Hf bond vibration frequency	kinetic theory for solid–solid chemical reactions	$7 \cdot 10^{13}$ Hz [7]
<i>Band gap</i>	Optical band gap	Elipsometry	5.6eV [8]

Figure 2. 13-a shows the model of 5-nm thick  $\text{HfO}_2$  based RRAM with an area of  $100\text{nm}^2$  that we are simulating. Temperature map evolution during Forming operation is also shown (Figure 2. 13-b). The local temperature increases with the number of defects due to the capture and emission process of charge carriers that release a net energy to the lattice.

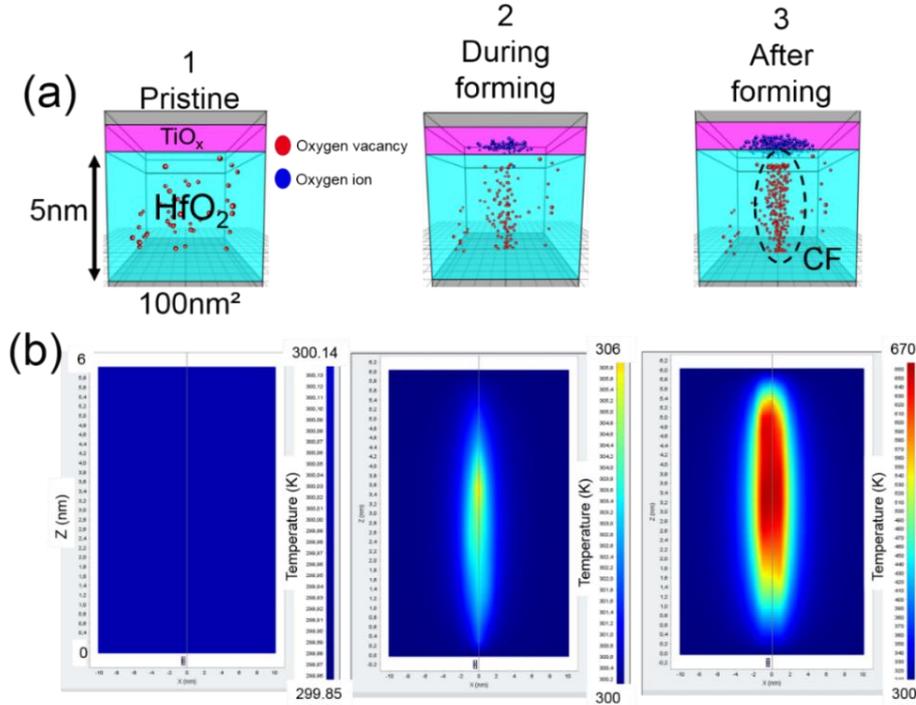
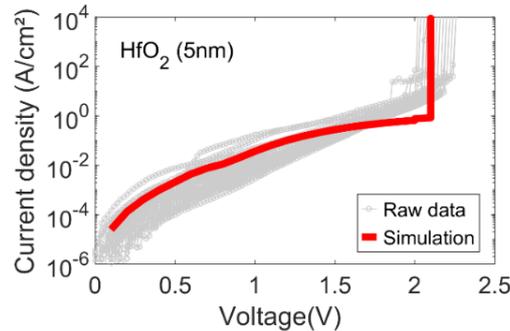


Figure 2. 13 : (a) Schematic of the simulated device for 5-nm  $\text{HfO}_2$  during Forming operation with creation of the CF. (b) Temperature evolution during Forming process.

To simulate the compliance current imposed by the access transistor, ultrafast current transients are monitored and the Forming operation is stopped to the time when the current limit is reached. We accurately reproduced the experimental I-V characteristics of Forming process for 5-nm  $\text{HfO}_2$  as shown in Figure 2. 14

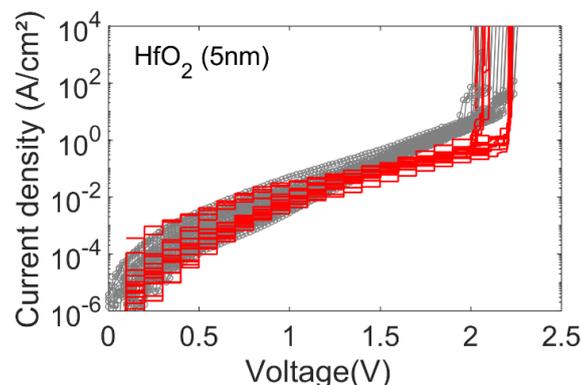
indicating that, the charge transport and defects generation mechanisms were properly identified in the model during the Forming process.



*Figure 2. 14 : Experimental data (gray) and simulation (color) of the current density variation during Forming operation of 5-nm pure HfO<sub>2</sub>.*

The statistical capabilities of the model, thanks to the Monte Carlo generation of defects, can be exploited to simulate the cell-to-cell variability observed on the experimental data of the Forming process. We consider a set of devices in pristine state for simulation. Each simulated device has a few number of defects that are randomly generated in its pristine state and then the Forming simulation generates other defects according to the thermochemical model generation mechanisms.

Figure 2. 15 reports the experimental (24 cells) and simulated (12 cells) Forming curves for the 5-nm HfO<sub>2</sub> samples. Based on simulation results, the random placement of defects in the pristine state can explain device-to-device variability of the Forming process.



*Figure 2. 15 : Experimental data (gray curves) and simulation (red curves) of device-to-device variability during the Forming process of 5-nm pure HfO<sub>2</sub> sample. Each red curve corresponds to a different placement of defects in the pristine state.*

## 2.5 Conclusion

In this chapter, we first presented our reference cell 5-nm thick HfO<sub>2</sub> based RRAM that was fabricated at CEA-Leti. The fabrication process and device structures are described. Second, the methodologies adopted to characterize the RRAM performances and reliability have been explained. Finally, we presented the Ginestra tool that we have used during the PhD. to investigate the physical processes governing the RRAM operations at the microscopic levels such as the charge transport and defects creation.

## 2.6 References

- [1] T. Cabout *et al.*, “Temperature impact (up to 200 °C) on performance and reliability of HfO<sub>2</sub>-based RRAMs,” *2013 5th IEEE Int. Mem. Work. IMW 2013*, pp. 116–119, 2013.
- [2] A. Padovani, L. Larcher, O. Pirrotta, L. Vandelli, and G. Bersuker, “Microscopic modeling of HfO<sub>x</sub> RRAM operations: From forming to switching,” *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1998–2006, 2015.
- [3] L. Vandelli, A. Padovani, L. Larcher, R. G. Southwick, W. B. Knowlton, and G. Bersuker, “A Physical Model of the Temperature Dependence of the Current Through Stacks,” *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 2878–2887, 2011.
- [4] D. Munoz Ramo, J. L. Gavartin, A. L. Shluger, and G. Bersuker, “Spectroscopic properties of oxygen vacancies in monoclinic HfO<sub>2</sub> calculated with periodic and embedded cluster density functional theory,” *Phys. Rev. B*, vol. 75, no. 20, pp. 1–12, 2007.
- [5] J. McPherson, J. Y. Kim, A. Shanware, and H. Mogul, “Thermochemical description of dielectric breakdown in high dielectric constant materials,” *Appl. Phys. Lett.*, vol. 82, no. 13, pp. 2121–2123, 2003.
- [6] G. Bersuker, D. C. Gilmer, D. Veksler, P. Kirsch, L. Vandelli, A. Padovani, L. Larcher, K. McKenna, A. Shluger, V. Iglesias, M. Porti, and M. Nafria, “Metal oxide resistive memory switching mechanism based on conductive filament properties,” *J. Appl. Phys.*, vol. 110, no. 12, 2011.
- [7] J. W. McPherson and H. C. Mogul, “Underlying physics of the thermochemical E model in describing low-field time-dependent dielectric breakdown in SiO<sub>2</sub> thin films,” *J. Appl. Phys.*, vol. 84, no. 3, pp. 1513–1523, 1998.
- [8] A. Padovani, L. Larcher, G. Bersuker, and P. Pavan, “Charge Transport and Degradation in HfO<sub>2</sub> and HfO<sub>x</sub> Dielectrics,” *IEEE Electron Device Lett.*, vol. 34, no. 5, pp. 680–682, 2013.
- [9] B. Traoré, P. Blaise, E. Vianello, H. Grampeix, S. Jeannot, L. Perniola, B. DeSalvo, and Y. Nishi, “On the Origin of Low-Resistance State Retention Failure in HfO<sub>2</sub>-Based RRAM and Impact of Doping/Alloying,” *IEEE Trans. Electron Devices*, vol. 62, no. 12, pp. 4029–4036, 2015.

# Chapter 3

## Reliability of HfO<sub>2</sub> based RRAM cells

### 3.1 Introduction

Resistive RAM memories are promising candidates for both Storage Class Memory (SCM) and embedded nonvolatile memories (eNVM). However, reliability (e.g. data retention, cycle to cycle and cell to cell variability, endurance etc.) is still an issue before the introduction to the market. In this chapter, we first investigated the data retention and the initial forming process of aluminum (Al)-doped HfO<sub>2</sub>-based RRAM devices. Three different methods to introduce Al in the memory stack were investigated: alloying HfO<sub>2</sub> with Al<sub>2</sub>O<sub>3</sub> as HfAlO in a single active layer device, double-layer devices with different Al concentration in the bottom layer and single active layer devices based on HfO<sub>2</sub> with Al doping by ionic implantation. Al incorporation is suggested to improve the device's data retention time without dramatically increasing the forming voltage. We have performed physical based simulations using an experimentally extracted set of parameters in order to explain the effects of Al incorporation on forming voltage at the microscopic level. Moreover, RRAM seems promising for space, radar and other radiation harsh environments, as it does not rely on charge storage (e.g. flash memories) and so has a great potential for radiation hardness. Therefore, studies concern the utilization of such memory technology in radiation environments are very important to explore their reliability under such conditions. In this respect, we presented in the second part of this chapter, the radiation immunity of 1R structure HfO<sub>2</sub>-based RRAM as another reliability parameter. For this purpose, we investigated from experimental and theoretical point of view if Single-Event Effect (SEE) can be a direct threat for HfO<sub>2</sub>-based RRAM. The impact of heavy-ion irradiation has been evaluated in cells with no access transistor. RRAM cells of different sizes and in different programming states (including pristine cells)

were irradiated with high-linear energy transfer (LET) ions and subjected to post radiation characterization. Resistance states and programming voltages were compared before and after irradiation to find out if the irradiation can damage the RRAM properties. A microscopic understanding of the experimental results that we obtained after irradiation is presented using physical based simulations.

## 3.2 Data retention improvement

### 3.2.1 Samples description with different Al incorporation methods

It has been demonstrated that aluminum (Al) incorporation in HfO<sub>2</sub>-based RRAM improve the data retention [1], [2]. Other studies showed that inserting a thin Al<sub>2</sub>O<sub>3</sub> layer in-between the HfO<sub>2</sub> switching layer and the metallic bottom electrode can improve the memory window as well as the operating current (down to the sub- $\mu$ A current operating regime) [3], [4].

We fabricated RRAM devices made of either a single or a double layer of active material. In the case of devices having a single layer of active material, the aluminum doping was performed by either ionic implantation on an atomic layer deposition (ALD) deposited HfO<sub>2</sub> layer or by HfAlO alloy deposited by ALD interchanging HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> cycles. The bilayer devices are composed of a top layer made of 3-nm of HfO<sub>2</sub>, and a 2-nm-thin bottom layer. The latter is either Al<sub>2</sub>O<sub>3</sub> or HfAlO alloy with different Al concentrations. Figure 3. 1 illustrates the RRAM devices fabricated using the three different Al-doping methods considered in this study: D1 and D10 are the 5-nm HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> reference samples, respectively, D2 is the 5-nm single-layer HfAlO(9:1) alloy (9:1 stands for 9 cycles of HfO<sub>2</sub> followed by 1 cycle of Al<sub>2</sub>O<sub>3</sub>), and D4, D5, and D6 are the 5-nm bilayer devices made of HfO<sub>2</sub>/HfAlO(9:1), HfO<sub>2</sub>/HfAlO(4:1), and HfO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub>, respectively. D3 is the 10-nm Al-free HfO<sub>2</sub> reference sample and D7, D8, and D9 are the cells doped by ionic implant with different Al concentrations, 0.1%, 1%, and 5 % of Al, respectively. All the materials used as active layer in the memory stack (HfO<sub>2</sub>, HfAlO, and Al<sub>2</sub>O<sub>3</sub>) were deposited by ALD at 300 °C. The dielectrics layers sandwiched between physical vapor deposited TiN (35-nm) bottom electrode and Ti (10-nm) top electrode (TE) were fabricated in a MIM structure.

The single-layer device with pure Al<sub>2</sub>O<sub>3</sub> as switching layer was sandwiched between TiN (35-nm) as top and bottom electrodes. The RRAM resistors are co-integrated with NMOS access transistor (1T1R test structure) in a standard 65-nm CMOS technology. The 1R element is integrated in the BEOL between M4 and M5. The 1R cell has a 1μm diameter.

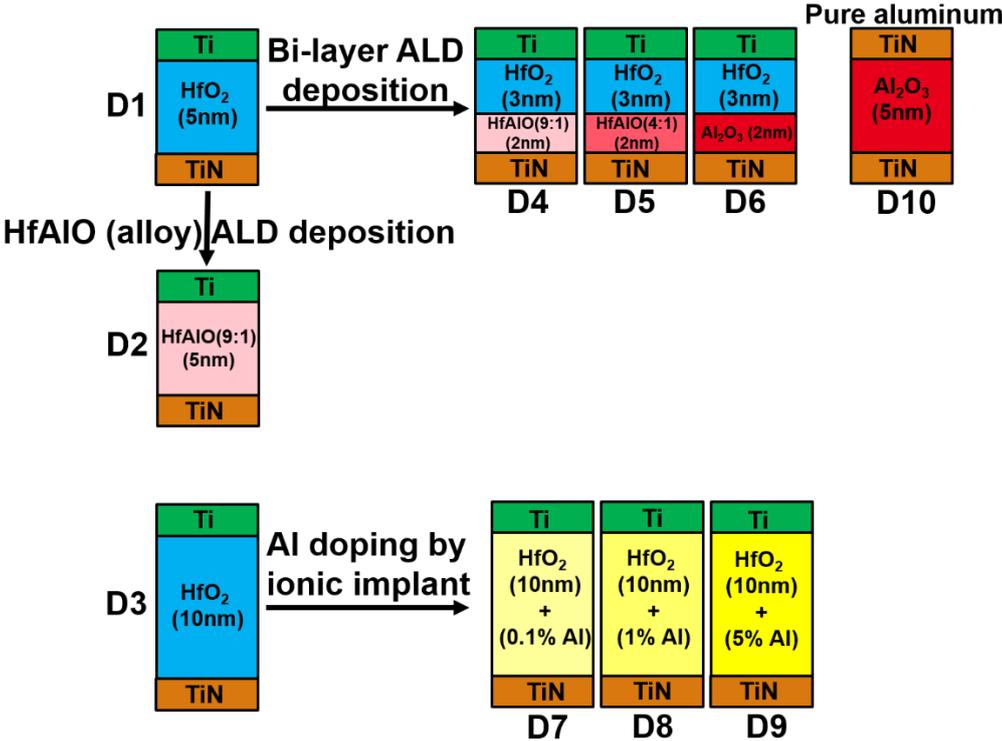


Figure 3. 1 : Schematic illustrations of the studied devices. Three different methods to introduce Al in HfO<sub>2</sub>-based RRAM stack, namely, ionic implantation, alloying HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> as HfAlO and double-layer devices with Al in the bottom layer are investigated

### 3.2.2 Materials properties

Since in bilayer devices material intermixing can occur, physical characterization was performed on single layer cells. Table 3. 1 summarizes the main physical parameters of the materials used in our study. Material density was measured by X-Ray Reflectometry, Al% was measured by Rutherford Backscattering Spectroscopy, and the optical band gap was measured by ellipsometry. The Al incorporation decreases the dielectric constant compared to pure HfO<sub>2</sub> and the

bandgap becomes higher. Atomic densities for HfO<sub>2</sub> and HfAlO(9:1) were calculated by ab-initio calculations [1]. HfAlO(9:1) shows higher atomic concentration compared to HfO<sub>2</sub> 8.53x10<sup>22</sup> (atoms/cm<sup>3</sup>) and 8.39x10<sup>22</sup> (atoms/cm<sup>3</sup>) respectively. Shorter Hf-O and Al-O bond lengths is demonstrated in HfAlO alloy [1]. For the devices where Al was incorporated through ionic implantation, the implant energy was 4 KeV.

*Table 3. 1: Physical properties of the studied samples extracted from physical characterization*

<b>Split</b>	<b>Density (g/cm<sup>3</sup>)</b>	<b>Dielectric constant</b>	<b>Al%</b>	<b>Optical band gap (eV)</b>
HfO <sub>2</sub>	9.62	22	0%	5.6
HfAlO(9:1)	8.79	18.9	4.3%	5.7
HfAlO(4:1)	8.2	17.4	9.6%	5.8
<b>Al density</b>				
HfO <sub>2</sub> +ionic Implant	8.4x10 <sup>13</sup> at/cm <sup>2</sup> (0.1% Al)			
	8.4x10 <sup>14</sup> at/cm <sup>2</sup> (1% Al)			
	8.4x10 <sup>15</sup> at/cm <sup>2</sup> (5% Al)			

### 3.2.3 Forming voltage

#### 3.2.3.1 Al incorporation effects

We measured the forming voltage on all the RRAM devices arranged in a 1T1R configuration, where the transistor is the current limiter device imposing a maximum current of ~120 μA. For each device family, 24 cells were formed by applying a DC ramped voltage on the TE. Figure 3. 2 shows the I–V curves measured during forming on the single-layer 5-nm HfO<sub>2</sub> sample. The gray curves correspond to I–V characteristics measured on individual devices, whereas the red curve is the average. The forming voltage ( $V_f$ ) is defined as the voltage at which the current suddenly increases, it corresponds to the transition point between the pristine state and Low Resistance State.

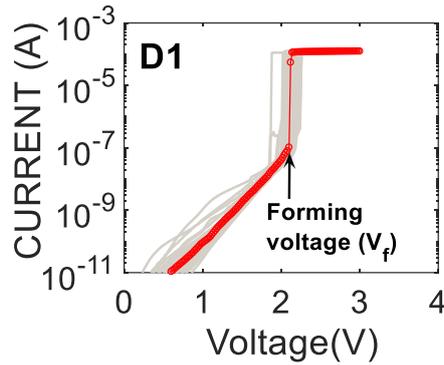


Figure 3. 2: Current/voltage characteristics during the forming process of  $\text{HfO}_2$  (D1) sample. Red curve is the average.

Figure 3. 3-a shows the forming voltage measured for single-layer devices as a function of the Al percentage: the red curve shows the  $V_f$  measured on 5-nm devices, for the  $\text{HfO}_2$  (zero Al concentration) and the  $\text{HfAlO}(9:1)$  (Al% = 4.3) samples. The black curve shows the forming voltage measured on the 10-nm devices, where Al doping is incorporated by ionic implantation. For a given Al concentration, thicker resistive switching layers lead to higher forming voltage. Figure 3. 3-b shows the average  $V_f$  measured on double layer devices as a function of the Al percentage in the bottom layer. In both cases (single and double layer devices),  $V_f$  linearly increases with Al percentages. The forming voltage in double-layer devices is higher compared to  $V_f$  in single-layer devices with the same physical thickness of the resistive switching layer and same total Al concentration in the memory stack (D2 compared to D5). This behavior will be investigated in section 3.3 “forming simulation”.

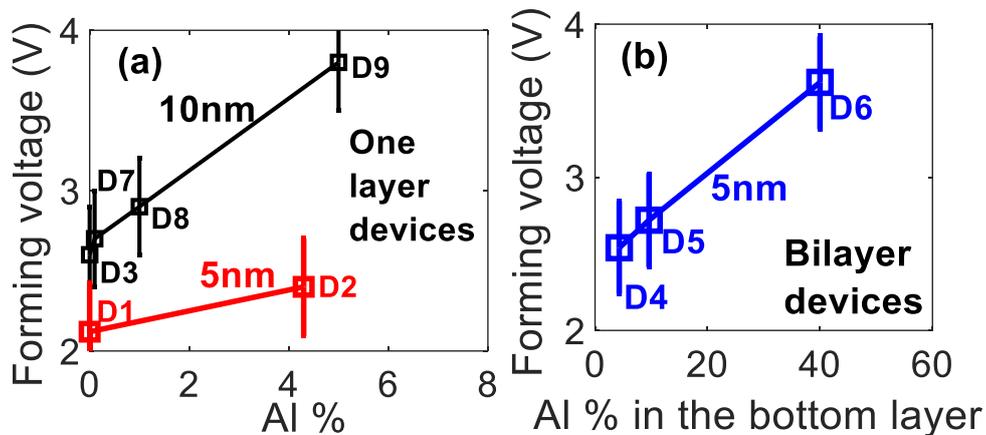


Figure 3. 3 : Forming voltage as a function of Al concentration for (a) single-layer devices and (b) bilayer devices

### 3.2.3.2 Temperature effects

We studied the temperature effect on forming operation. For this purpose, devices were formed at three different temperatures (room temperature (RT), 60 °C, and 100 °C). Figure 3. 4 shows the I-V characteristics during forming process for the D1 sample at room temperature (red curves) and 100°C (blue curves). As expected, the forming voltage reduces with the temperature, as a consequence of the larger atomic vibrations around the equilibrium positions resulting in a lower barrier for the Hf-O bond breakage originating the CF formation [5].

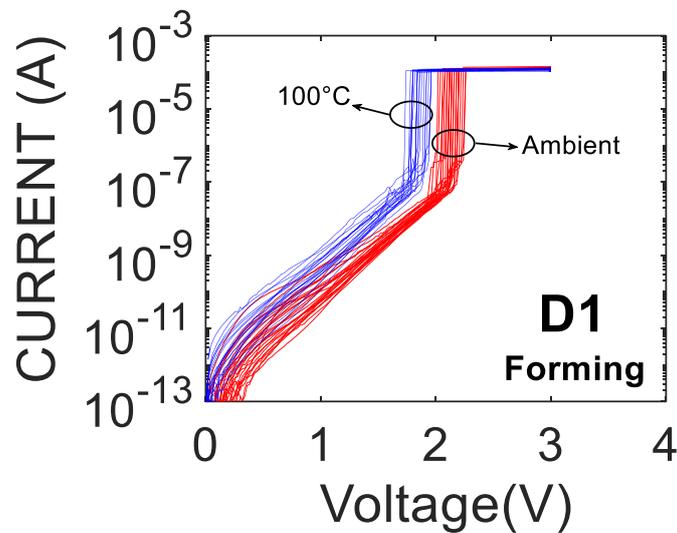


Figure 3. 4 : I-V characteristics during forming process for the D1 sample at different temperatures. Room temperature (red curves), 100°C (blue curves).

We have performed the forming operation of single layer devices (D1, D2 and D7) and bilayer devices (D4 and D6) at different temperatures using the thermal wafer chuck of the probers. Figure 3. 5 shows the average of the extracted forming voltage ( $V_f$ ) as function of the temperature (ambient, 60°C and 100°C) for single layer and bilayer devices. The forming process is activated by temperature where lower forming voltages are collected at higher temperatures. We calculated the slope of the extrapolated curves of  $V_f$  vs Temperature of the different samples as shown in Figure 3. 5. For all the studied samples we have calculated almost the same slop of  $\sim 0.007$ . Consequently, the dependence of forming process on temperature was found to be independent of the Al content and the Al doping method (HfAlO alloy, Al ionic implant or double layers).

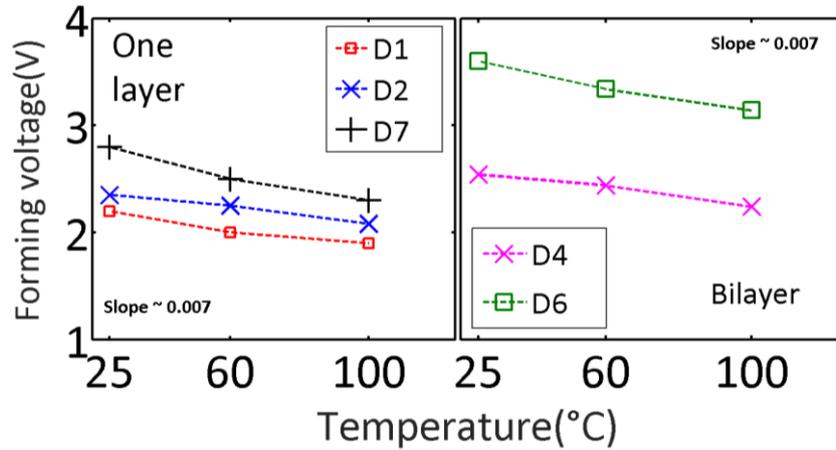


Figure 3. 5 : Forming voltage as a function of temperature for single-layer and double-layer devices

### 3.2.4 Data retention

Frascaroli et al. [6] investigated the impact of Al doping on the data retention of the high resistance state (HRS) and showed that tailoring of the Al concentration allows improving the retention of the HRS state. The low resistance state (LRS) data retention improvement in HfAlO(9:1) alloy compared to the reference HfO<sub>2</sub> sample has been previously investigated experimentally and by simulations in [7].

In our study, LRS data retention has been investigated experimentally for HfO<sub>2</sub>, HfAlO(9:1) alloy, bilayer devices, and the single layer HfO<sub>2</sub> with Al doping by ionic implantation. For each family, 24 devices were formed and cycled before backing. In order to compare the data retention of the low resistance state (LRS), the same initial resistance level is required before backing for all the devices under test. LRS level is controlled by the compliance current during forming and set operations. A compliance current of 120  $\mu$ A (that was set by applying a proper voltage to the gate of the select transistor) was fixed during forming and cycling operations for all tested devices. The samples were put after programming in the oven at the test temperature and their resistance states were monitored. Figure 3. 6 shows LRS evolution with time at two different temperatures (200 °C and 275 °C) for the HfO<sub>2</sub> reference sample (D1). As the temperature increases, the LRS fails faster toward the high resistance state (HRS) indicating that LRS data retention process is highly activated by temperature.

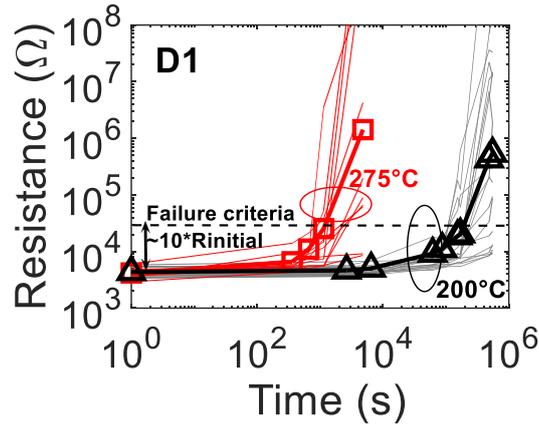


Figure 3. 6 : LRS evolution during time at 200 °C and 275 °C for D1 sample. Black curve and red curve with markers show the average trend of the devices at 200 °C and 275 °C respectively.

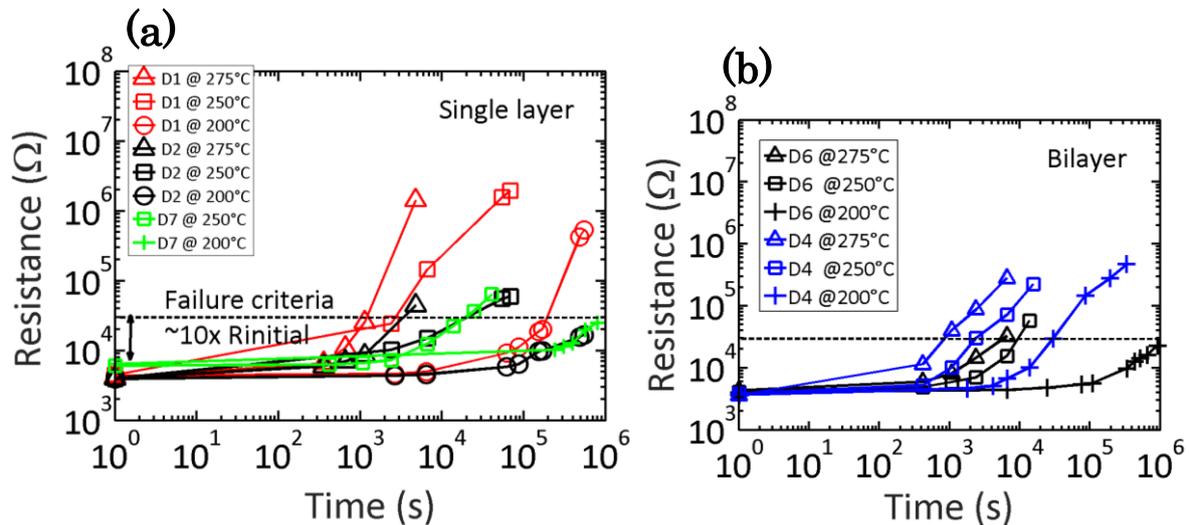


Figure 3. 7 : Comparison of LRS data retention for (a) single layer (D1, D2 and D7) and (b) bilayer devices (D4 and D6) at different temperatures.

LRS of single layer  $\text{HfO}_2$  (D1) presents faster failure toward HRS compared with  $\text{HfAlO}(9:1)$  (D2) that shows better LRS data retention as shown in Figure 3. 7-a. These results are in agreement with the results of Fantini et al. [2] and Traoré et al. [1]. We will investigate in the next section the data retention of  $\text{HfO}_2$  based RRAM devices with different methods of Al incorporation in the memory stack (D1-D9). We will compare the activation energies of LRS failure of different devices. This activation energy ( $e_a$ ) could be extracted from LRS evolution at different temperatures using Arrhenius law [1].

### 3.2.4.1 Activation energies of LRS failure

All the devices under test show LRS failure activated by temperature as shown in Figure 3. 6 and Figure 3. 7. In this study, the bit failure time was defined as the point where the initial LRS has drifted toward HRS by one order of magnitude (see Figure 3. 7), which correspond typically to the memory window of HfO<sub>2</sub> based RRAM. The extracted failure times for D1 and D2 based on the above criteria are plotted in an Arrhenius plot as shown in Figure 3. 8 and using the following Arrhenius equation:

$$\tau = \tau_0 \exp\left(\frac{e_a}{k_b T}\right) \quad (3.1)$$

Where  $\tau$  is the rate of reaction,  $\tau_0$  the pre-exponential factor ( $\sim 10^{12} - 10^{13}$  Hz),  $e_a$  the activation energy of LRS failure,  $k_b$  the Boltzmann constant and T the temperature. The linear trend of the failure time with respect to the inverse of temperature shows that the LRS retention failure process in HfO<sub>2</sub> and HfAlO-based RRAMs follows an Arrhenius type of law. The activation energy ( $e_a$ ) is defined as the energy barrier required to start the drift reaction of LRS toward HRS under thermal stress.

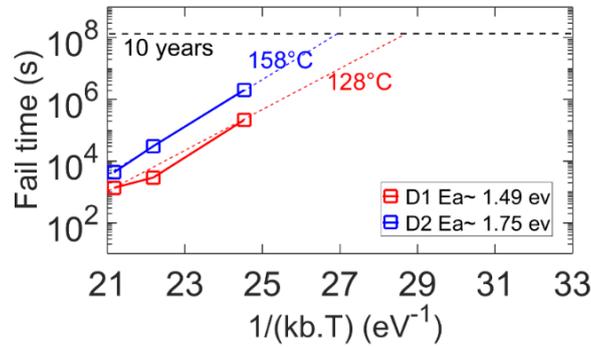


Figure 3. 8 : Arrhenius plot of the extracted failure time based on failure criteria defined in Figure 3. 7

Higher activation energy of LRS failure ( $e_a$ ) is extracted for D2 compared D1, consistent with its better LRS stability. More than 10 years of retention at 128 °C and 158 °C are extrapolated for the single layer 5-nm pure HfO<sub>2</sub> and HfAlO(9:1) respectively, as shown in Figure 3. 8. We did the same process of failure time extraction for samples D2–D6, D8, and D9. Figure 3. 9 shows that the failure time at ten years linearly increases with Al concentration for both single layer as an alloy (D2) and bilayer devices. A higher Al content is required in bilayer devices to boost

the data retention with respect to the single-layer cells. D2 samples, corresponding to the single-layer device with 4.3% of Al, shows the same data retention behavior of the bilayer with 16% of Al (D6). The 10-nm HfO<sub>2</sub> non-doped sample (D3) presents a slight improvement of data retention with respect to the 5-nm HfO<sub>2</sub> (D1). However, Al doping by ionic implantation does not impact the data retention, and D3, D8, and D9 samples present a very similar failure temperature at 10 years of data retention.

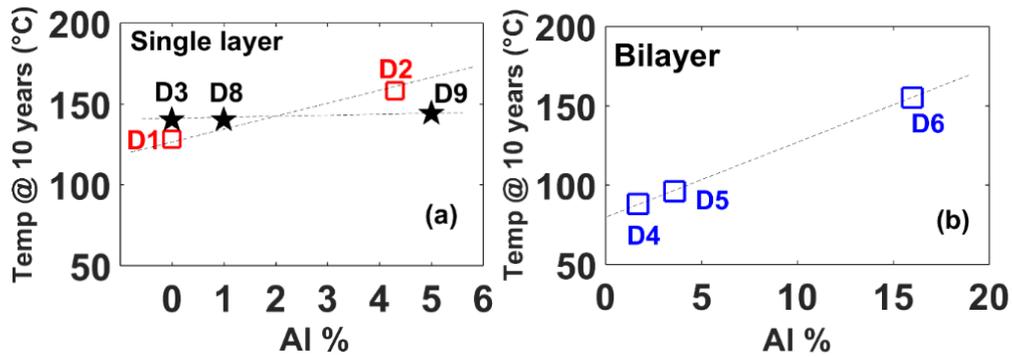


Figure 3. 9 : Failure temperature at 10 years (extracted using the Arrhenius law) for (a) single-layer devices and (b) bilayer devices as a function of Al% in the device.

### 3.2.5 Data retention/ forming trade-off

As we demonstrated in this chapter that double-layer devices (D4–D6) show higher forming voltage compared to single-layer devices (D1 and D2). If we consider D1 as our reference sample, the single-layer HfAlO(9:1) (D2) and bilayer with Al<sub>2</sub>O<sub>3</sub> at the bottom layer (D6) improve the data retention where a failure temperature at 10 years of about 150 °C is estimated for both samples. However, D6 has much higher forming voltage compared to D2. Figure 3. 10 shows the data retention temperature at 10 years as a function of the corresponding forming voltage.

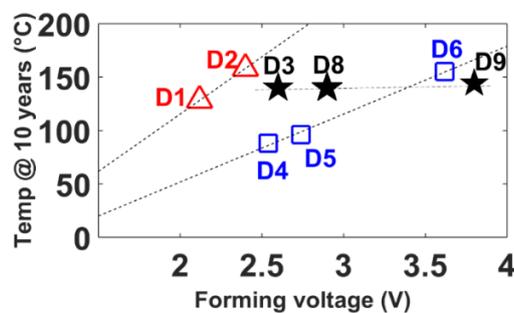


Figure 3. 10 : Data retention vs forming voltage in single-layer devices and double-layer devices

### 3.3 Forming simulation

In this section we will focus on forming process of the devices: D1, D2, D9 and D10. We will extract first the activation energy to break a bond at zero field ( $E_a$ ) and the molecular dipole moment ( $P_0$ ) of the different samples from TDDDB data by using the thermochemical model theory. Then we will perform the forming simulation for the different devices with the aim of investigating the effects of Al-doping and the device geometry (single layer or bilayer devices) on microscopic properties of HfO<sub>2</sub> material and the forming voltages ( $V_f$ ).

The microscopic properties ( $E_a$  and  $P_0$ ) of the Al<sub>2</sub>O<sub>3</sub> (D10), HfAlO(9:1) (D2) and 10-nm HfO<sub>2</sub> with ionic implanted 5% Al (D9) were extracted using the same method described in section 2.4.3.1 for 5-nm HfO<sub>2</sub> (D1). Figure 3. 11-a shows the TDDDB measurements for the 10-nm HfO<sub>2</sub> with 5% Al doping by ionic implant samples (D9) at different temperatures, while Figure 3. 11-b shows the same experiments for samples with a 5-nm active layer thickness, i.e., reference HfO<sub>2</sub> (D1), HfAlO (9:1) (D2) and Al<sub>2</sub>O<sub>3</sub> (D10). Figure 3. 11-c and d show the  $E_{a,eff}$  as a function of the electric field, and the interpolation using a linear fitting to extract  $E_a$  and  $P_0$  for the studied samples.

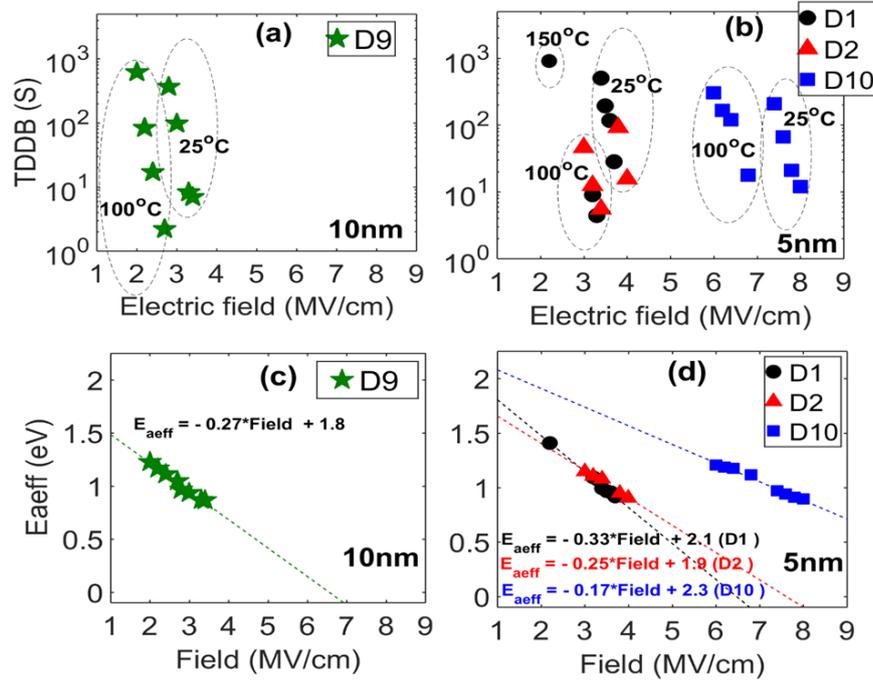


Figure 3. 11: TDDDB data for (a) 10-nm HfO<sub>2</sub> with 5% Al doping by ionic implant, (b) the 5-nm thick: HfAlO (9:1) (red triangle), HfO<sub>2</sub> (black sphere) and Al<sub>2</sub>O<sub>3</sub> (blue square) at different temperatures. Each point is the mean value of 12 devices. (c) And (d) show the extraction method of  $E_a$  and  $P_0$  using equation (2.4) [ $E_{a,eff} = E_a - b * F$ ]

The parameters extracted for the different materials are reported in Table 3. 2. The dielectric constant  $k$  is derived from C-V measurements.

*Table 3. 2:* Extracted parameters from TDDB and CV measurements for HfO<sub>2</sub>, HfAlO (9:1), and HfO<sub>2</sub> doped with 5% Al by ionic implantation and Al<sub>2</sub>O<sub>3</sub>.

Parameter	D1	D2	D9	D10
E <sub>a</sub> (eV)	2.1	1.9	1.8	2.3
P <sub>0</sub> (e·Å)	4.3	3.5	3.8	4.6
K	22	18.9	18.9	9

By using the set of parameters extracted from TDDB measurements, the model reproduces very accurately both the leakage current before the switching point and the forming voltage for all the simulated samples as shown in Figure 3. 12.

The local electric field  $E_{loc}$ , that distorts the molecular bond in the dielectric lattice, is a function of the macroscopic electric field  $F$  (voltage dropped across the dielectric divided by dielectric thickness) and the dielectric constant  $K$ .  $E_{loc}$  can be written in a Lorentz-Mossotti relation as follow [8]:

$$E_{loc} = \frac{2 + k}{3} F \quad (3.2)$$

According to the thermochemical description of the dielectric breakdown [8], the local electric field reduces the activation energy for bond breakage process ( $\Delta H$ ) during the forming operation as following :

$$\Delta H = \Delta H^* - P_0 \cdot E_{loc} \quad (3.3)$$

Where  $\Delta H^*$  is the activation energy required for bond breakage in the absence of electric field and  $P_0$  is the molecular dipole moment component.

The parameters extracted for HfO<sub>2</sub> doped with Al as an alloy and by ionic implantation (D2 and D9) show that Al incorporation reduces  $P_0$  and  $K$  compared to the D1 reference sample. Consequently,  $\Delta H$  increases with Al doping based on equations (3.2) and (3.3). The higher activation energy required to break the metal-ion bonds explain the higher  $V_f$  for the samples incorporated with Al (D2 and D9) compared to Al free samples (D1).

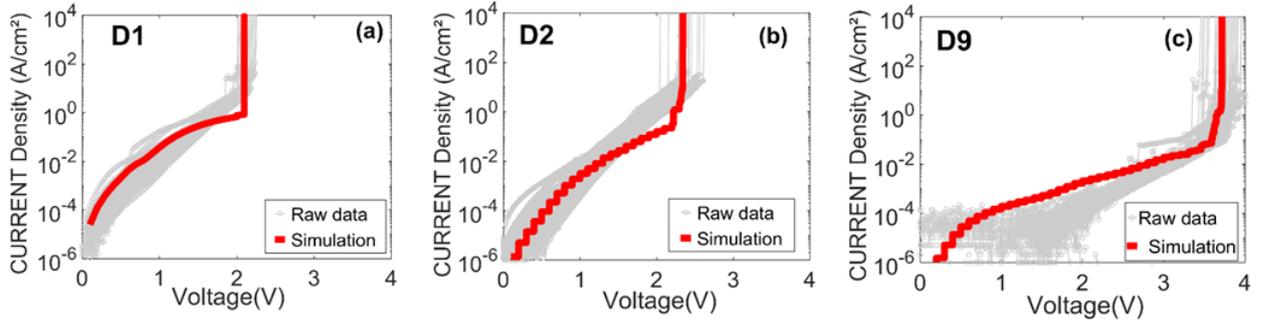


Figure 3. 12 : Experimental data (gray) and simulation (color) of the current density variation during forming operation of (a)5-nm pure HfO<sub>2</sub>, (b) 5-nm HfAlO(9:1) and (c)10-nm HfO<sub>2</sub> with 5% Al doping by ionic implant

We investigated the forming dynamics in bilayer samples, where forming depends on material properties and electric field redistribution on the two layers due to the different  $k$  values of each material. Figure 3. 13-a and b reports the I/V curves simulated and measured during forming for the HfO<sub>2</sub>/HfAlO(9:1) (D4) and HfO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> (D6) samples, respectively. Figure 3. 13-c reports the electric field obtained by simulation in D1 (red curve) and D6 (blue curve) samples at the forming voltages of 2.2 and 3.5 V, respectively. Simulations show that, the electric field drop on HfO<sub>2</sub> layer at the switching point is  $\sim 4 \times 10^8$  V/m for the three samples D1, D4, and D6. In multilayer devices, higher electric field drops on the layer having the lower dielectric constant (HfAlO(9:1) in the case of D4 and Al<sub>2</sub>O<sub>3</sub> in this case of D6). Consequently, a sort of electric field divider exists in the case of bilayer samples. Therefore, higher electric field must be applied on multilayer devices (D4 and D6) compared to single layer devices to provide the appropriate electric field drop required for the soft breakdown of each layer.

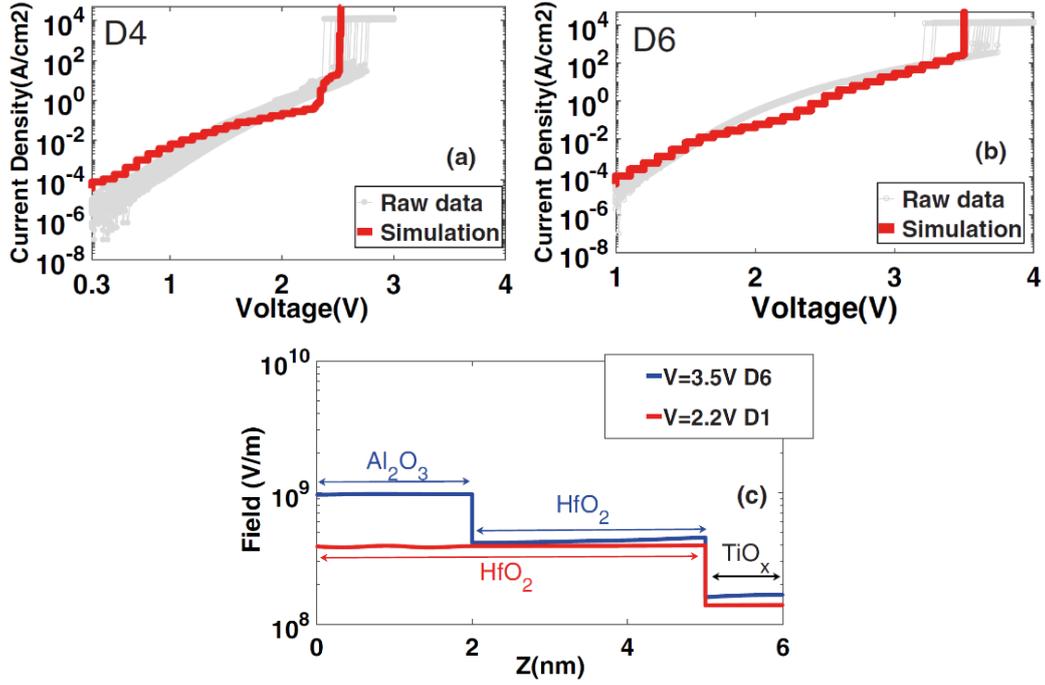


Figure 3. 13 : Forming IV curves for (a) D4 ( $\text{HfO}_2$  (3nm)/ $\text{HfAlO}(9:1)$  (2nm)), (b) D6 ( $\text{HfO}_2$  (3nm)/ $\text{Al}_2\text{O}_3$  (2nm)). Gray curves: raw data and red curves: simulations. (c) Electric field distribution at the forming voltage in D1 and D6. For  $\text{HfO}_2$ ,  $\text{HfAlO}(9:1)$  and  $\text{Al}_2\text{O}_3$  simulations, we used the parameters reported in Table 2. 2.  $Z$  is the thickness of the active layer

The simulation allows reproducing the forming voltage in  $\text{HfO}_2/\text{HfAlO}(9:1)$  (D4) and  $\text{HfO}_2/\text{Al}_2\text{O}_3$  (D6) stack using the nominal thicknesses for the two layers without changing the material parameters ( $k$ ,  $E_a$ , and  $P_0$ ) extracted and reported in Table 3. 2 for the  $\text{HfO}_2$ ,  $\text{HfAlO}(9:1)$ , and the  $\text{Al}_2\text{O}_3$  materials, simply taking into account the field redistribution due to the different  $k$  values. This result indicates that the higher forming voltage in multilayer devices is mainly due to the electric field redistribution and there is no significant material intermixing.

## 3.4 Radiation immunity

In the last years few works have been presented on the response of RRAM to ionizing radiation. Most of these works dealt with the effects of total dose and displacement damage (DD) [9]–[11]. Depending on the maturity of the tested structures, little to no effects have been observed in cells irradiated to relatively high doses (few Mrad). When observed, degradation has mostly been related to the radiation-induced creation and migration of additional oxygen vacancies in the oxide. Further work has shown that high dose rates can switch cells to an LRS in TaO<sub>x</sub> and TiO<sub>2</sub> devices [12]–[14].

### 3.4.1 Experiment and devices

1R resistive memories manufactured at CEA-Leti were adopted for this study. The resistive switching layer is a 5-nm-thick hafnium oxide deposited by atomic layer deposition at 300 °C, sandwiched between physical vapor deposition deposited top Ti (10 nm) and bottom TiN (35 nm) electrodes. Irradiations with heavy ions were performed at the SIRAD line of the TANDEM accelerator at Laboratori Nazionali di Legnaro, Padua (Italy). We used the highest-LET ion available, i.e., 266.7-MeV iodine (LET = 59 MeV/mg/cm<sup>2</sup> in Si). Device terminals were floating during irradiation. The resistances of the OxRAM cells in all the three possible states (pristine, LRS, and HRS) were measured before irradiation. The irradiation exposures were performed on unbiased devices and at normal incidence. Unbiased conditions are extremely relevant for RRAM devices, since these nonvolatile memories spend most of their lifetime without any applied bias. After irradiation, the cell resistances were measured again. For the cell that were in the pristine state before irradiation, a forming was performed, to investigate the irradiation effect on the forming voltage with respect to reference devices. Finally, cells that were in LRS and HRS were cycled in order to investigate the impact of ion strikes on set and reset voltages. Overall, more than 100 cells for each state were studied.

### 3.4.2 Experimental results

The devices were irradiated with a fluence of  $2.2 \cdot 10^9$  I ions/cm<sup>2</sup>. Cells with different sizes (7.06, 0.78, 0.28, and 0.19 μm<sup>2</sup>) and different resistance states of an RRAM

(pristine, LRS and HRS) were irradiated. With this fluence the largest cells ( $7.06 \mu\text{m}^2$ ) were hit on average by  $\sim 200$  ions, while the smallest cells ( $0.19 \mu\text{m}^2$ ) were hit on average by  $\sim 5$  ions.

### 3.4.2.1 Resistances states before and after irradiation

After the exposure all the resistance states were measured again to find out the irradiation damages. Figure 3. 14-16 show the cumulative probability distributions of the resistance read before and after exposure, for cells of different sizes irradiated with  $2.2 \cdot 10^9$  I ions/cm<sup>2</sup> in pristine state, LRS and HRS respectively. Regardless the cells resistance states, no effects were observed on any of the irradiated devices. All the cells were found in the same state as before irradiation, i.e., no bit flips occurred as shown in Figure 3. 14-16. These results mean that even tens or more high-LET ion hitting on the same device are not able to produce a measurable resistance shift.

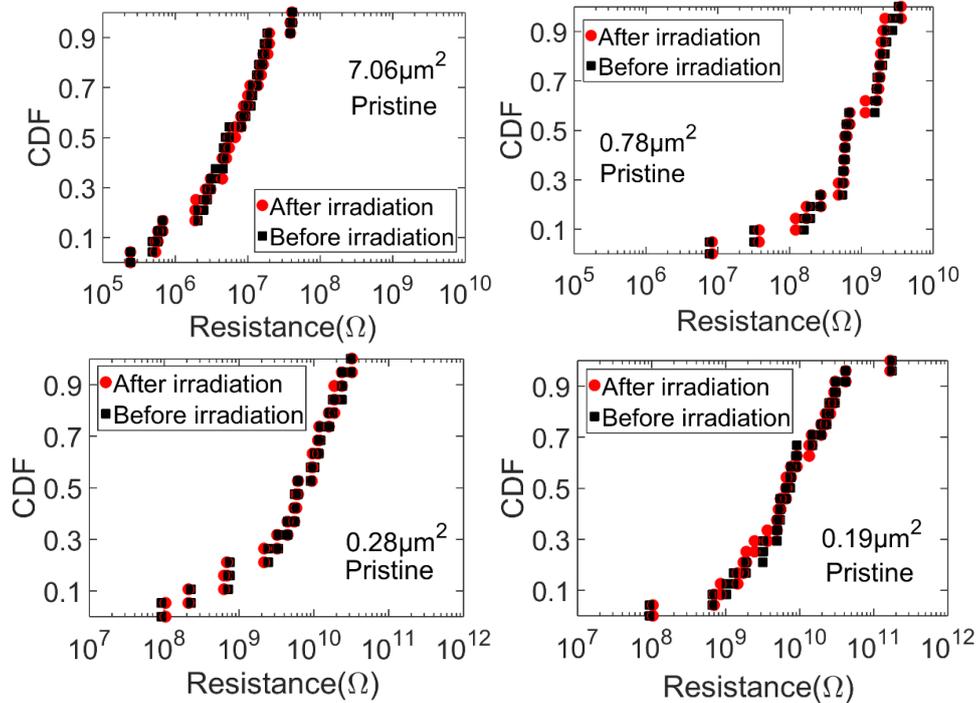


Figure 3. 14: Cumulative resistance probability distributions for cells with different sizes irradiated in the pristine state, measured before and after exposure ( $2.2 \cdot 10^9$  I ions/cm<sup>2</sup>)

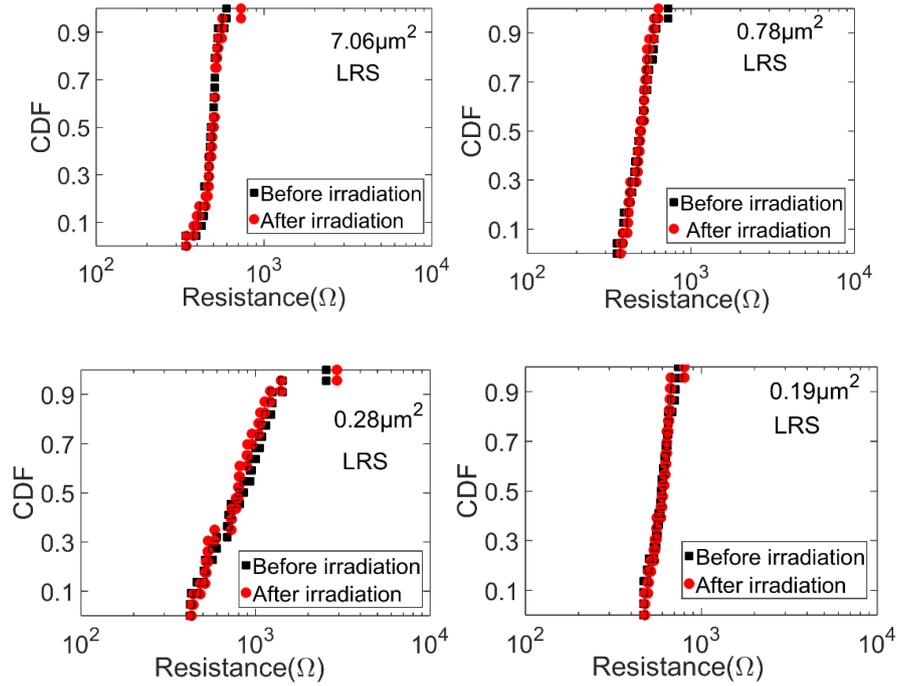


Figure 3. 15 : Cumulative resistance probability distributions for cells with different sizes irradiated in the LRS, measured before and after exposure ( $2.2 \cdot 10^9$  I ions/cm<sup>2</sup>)

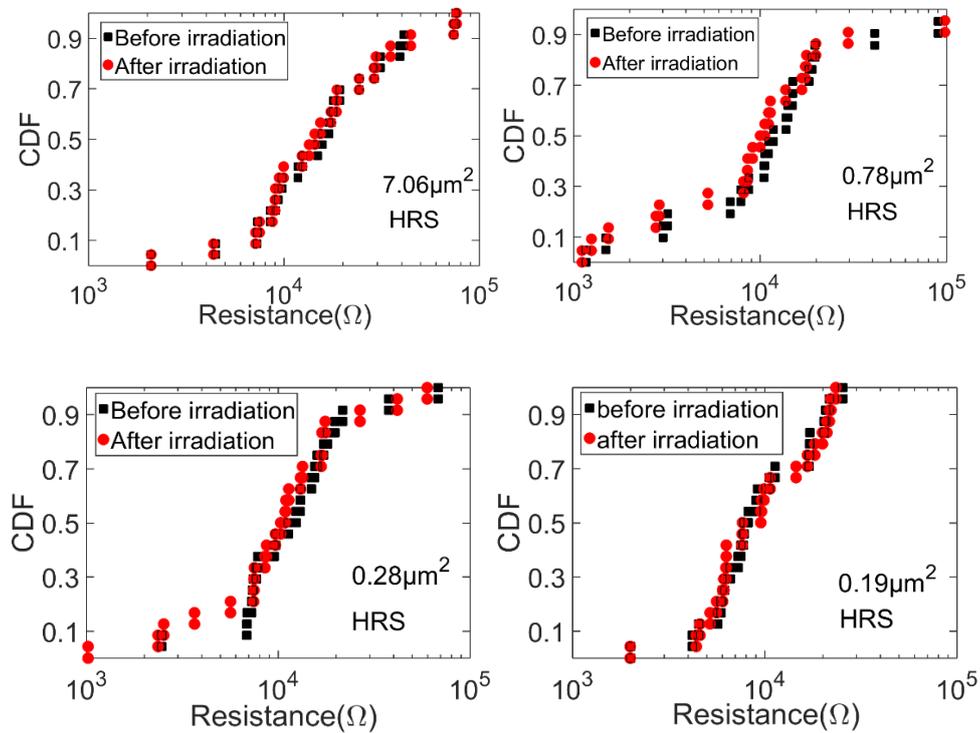


Figure 3. 16 : Cumulative resistance probability distributions resistance for cells with different sizes irradiated in the HRS state, measured before and after exposure.

### 3.4.2.2 Programming voltages before and after irradiation

The cells that were irradiated in the pristine state were subjected to a forming process after exposure in order to investigate the ion-induced changes in the forming voltage. I-V characteristics before and after irradiation in Figure 3. 17 show no irradiation effects on leakage current and forming voltage (abrupt jump of the current). The cumulative distributions of the forming voltages for nonirradiated and irradiated cells of different sizes are shown in Figure 3. 18. Only small changes are observed on the forming voltage distribution, more pronounced for larger cells. This change, however, is not due to radiation, but to intrinsic cell-to-cell variability. In fact, the two measurements (before and after irradiation) were performed on different sets of cells (of course cells can be formed only once) located in different dies on the wafer. The difference is inside the expected variability window, as shown in Figure 3. 19, where the die-to-die variability on the forming process of cells with  $0.78\text{-}\mu\text{m}^2$  area is depicted.

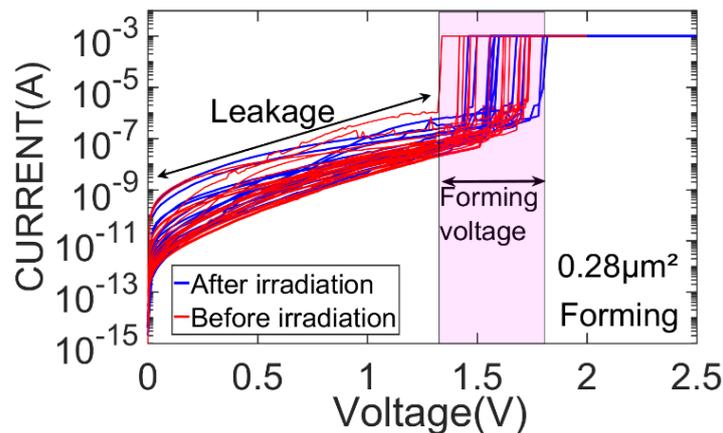


Figure 3. 17: I-V characteristics of forming operation before and after irradiation.

There is a linear correlation between cell size and the forming voltage [15], [16]. This voltage ( $V_f$ ) is inversely proportional to the number of defects that exist in the dielectric layer [17]. Consequently, the forming voltage increases for the scaled cells due to lower number of defects compared to larger devices. The experimental results presented in Figure 3. 14 are in agreement with the relationship between the device area and forming voltage where higher pristine resistances are measured for smaller devices. Therefore, higher forming voltage is required to initialize the scaled devices as shown in Figure 3. 18.

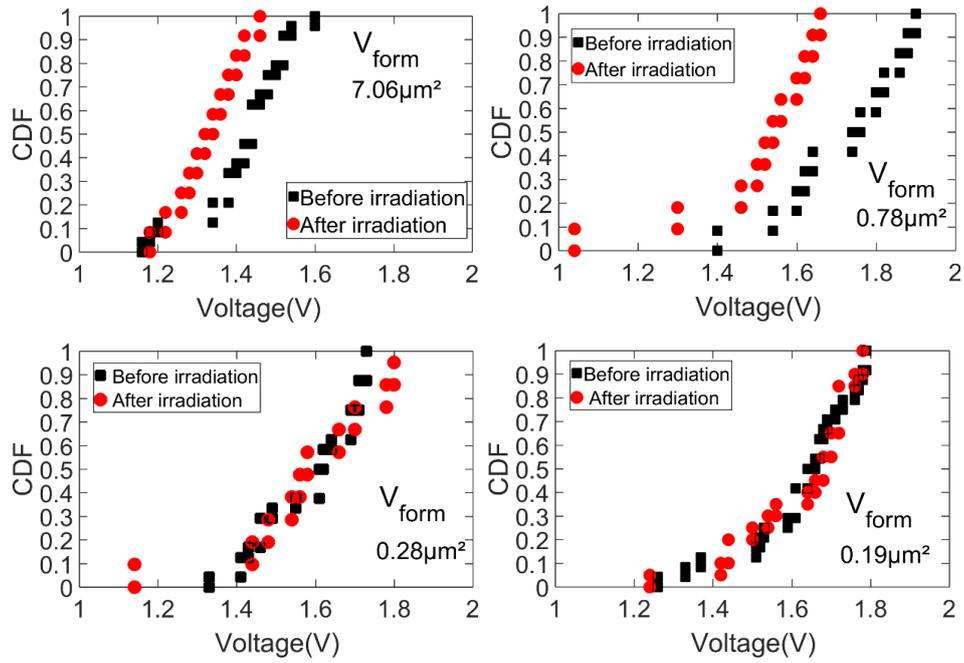


Figure 3. 18 : Cumulative probability distribution of the forming voltage for nonirradiated and irradiated cells of different sizes.

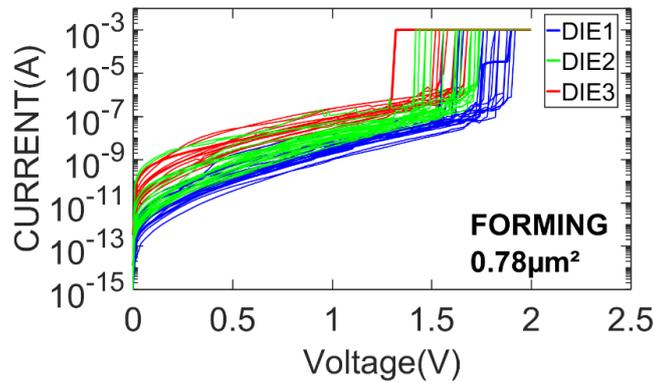
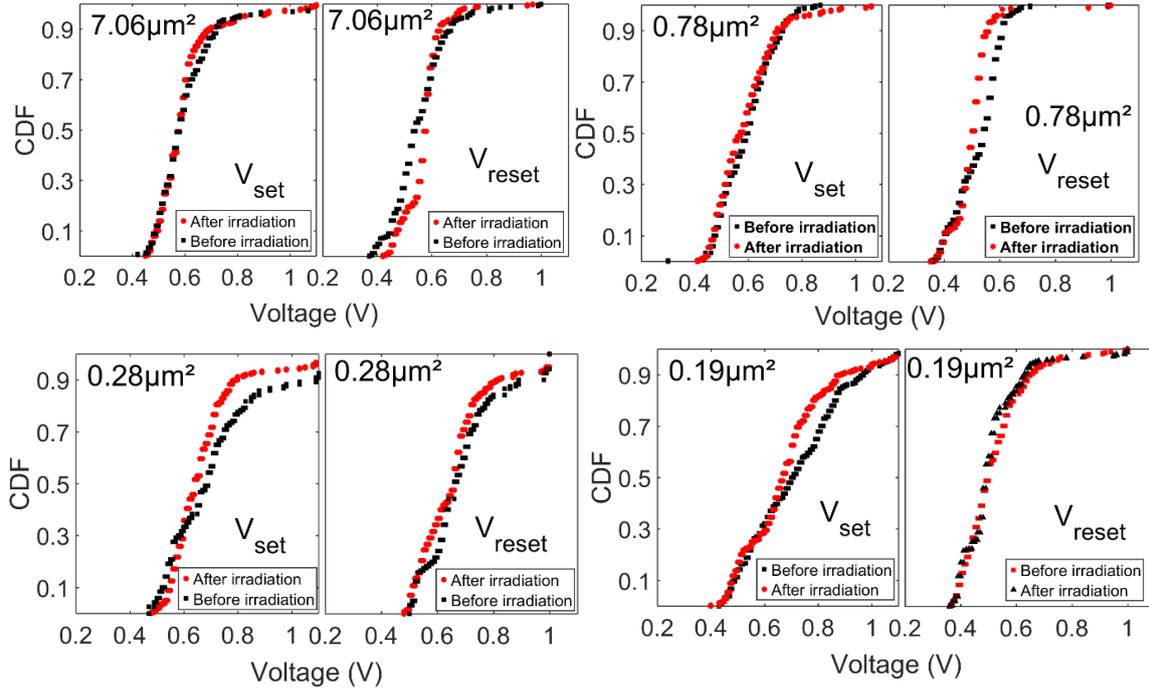


Figure 3. 19 :  $I$ - $V$  characteristics showing die-to-die variability. Each color stands for different die and each curve stands for a different device.

Concerning the cells irradiated in the LRS and HRS, the variations in the Set and Reset voltages after heavy-ion exposure are shown in Figure 3. 20. The cumulative distributions of Set and Reset voltages on the same set of cells, before and after irradiation (irradiated both in LRS and in HRS) show negligible differences between irradiated and nonirradiated cells. Again, the very small observable changes can be attributed to cell-to-cell intrinsic variability and not to heavy-ion effects.



*Figure 3.20 : Cumulative probability distribution of the Set and Reset voltages for cells with different sizes, before and after irradiation with iodine up to a fluence of  $2.2 \cdot 10^9 \text{ cm}^{-2}$ . These cells were irradiated in both HRS and LRS states.*

### 3.4.3 Mechanisms and simulation

Heavy ions release energy that creates electron–hole pairs, generating transient spurious currents/voltages that clearly cannot directly affect RRAM cells, although they might trigger Set/Reset voltages as illustrated in [18]. However, heavy ions have potentially other effects that might impact on the resistivity of RRAM cells, namely, displacement damage (DD), generation of defects favoring the leakage paths, and local temperature increases (which could favor the defect formation). The DD is the radiation-induced generation of oxygen vacancies, which could in principle give rise to a CF, similar to that generated by the forming process. As a result, pristine cells or cells in the HRS could be affected. These phenomena bear strong similarities with the corresponding effects induced by electrical stress, i.e., stress-induced leakage current, soft breakdown (SB), and hard breakdown. To investigate the possible DD phenomena at the microscopic level, simulations of transport of ions in matter (TRIM) have been performed first to evaluate the number of oxygen vacancies that could be produced in a 5-nm thick  $\text{HfO}_2$  by the heavy-ion irradiation used in our experiment. Physics-based simulations using the Ginestra [21] were

performed later to study the evolution of the defects generated under the heavy ions strikes and their implication on the leakage current of OxRAM devices. We aim at explaining through the simulations the experimental results showing no relevant changes observed on devices after irradiation.

### 3.4.3.1 Transport of Ions in Matter (TRIM) simulations

As mentioned, TRIM simulations were performed to evaluate the number of defects that could be generated in the  $\text{HfO}_2$  layer because of iodine ions strikes. The parameters used in TRIM simulation (e.g. ions energy, species properties, oxide material, oxide thickness) are identical to the exposure conditions. TRIM simulation parameters are listed in Table 3. 3.

Table 3. 3 : TRIM simulation parameters

Parameter	TRIM Simulation
Species	Iodine ions
Energy [ MeV]	266.7
Irradiated dielectric	$\text{HfO}_2$
Dielectric thickness	5nm

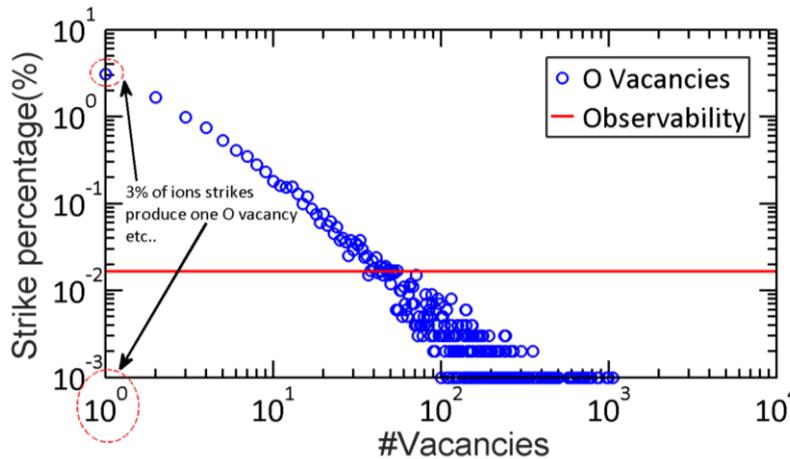


Figure 3. 21 : TRIM simulation results showing the number of oxygen vacancies that could be produced in  $\text{HfO}_2$  layer under Iodine ions strikes.

TRIM simulation results are shown in Figure 3. 21, where the number of oxygen vacancies generated by a single ion strike is plotted. Simulation results show that, 3% of the ion strikes produce one O vacancy in each cell, less than 2% produce two oxygen vacancies, etc. (see Figure 3. 21). The red line shows the maximum number

of vacancies based on the ion fluence delivered during our experiments (corresponding to 40 oxygen vacancies in a single cell).

### 3.4.3.2 Physics based simulations

The leakage current in RRAM devices is mainly assisted by oxygen vacancies. The generation of oxygen vacancy defects in  $\text{HfO}_2$  is originated by the rupture of Hf-O bonds [19], [20]. For the occurrence of this process, two subsequent steps must occur, that are: 1) a sufficient energy has to be provided to the lattice to create a Frenkel pair and 2) once the Frenkel pair is generated, the oxygen interstitial and the vacancy must diffuse away from each other in order to avoid direct recombination. The application of an electric field lowers significantly the energy barrier for ion/vacancy diffusions, and favors the subsequent diffusion of oxygen interstitials and vacancies by contrasting the Coulomb attraction between the negatively charged oxygen interstitials and the positively charged oxygen vacancies.

During our irradiation experiment OxRAM cells were not biased, the lack of bias could be the reason why no relevant modification in the cell characteristics was observed: an immediate recombination of the Frenkel pairs generated by impinging ions occurs due to Coulomb attraction as there is no voltage applied. In order to validate this hypothesis, we performed physics-based simulations using the Ginestra simulation package [21] to investigate the recombination of interstitial and vacancies generated by the impinging ions upon the application of an external bias. Simulations were run by considering that ion strikes generate (randomly) a given number of oxygen interstitials and vacancies within the 5-nm-thick oxide layer of a cell with device area of  $100 \text{ nm}^2$  according to TRIM simulations. The diffusion and recombination of the generated Frenkel pairs is then simulated by applying different biases. Based on TRIM simulation results, a maximum number of 40 negatively charged oxygen interstitial and positively charged oxygen vacancy Frenkel pairs can be generated at the ion fluence considered in our experiment. Figure 3. 22 shows a sketch of a simulated cell where state 1 corresponds to the device before irradiation, while state 2 corresponds to the device after irradiation. Assuming that irradiation produces 40 additional O vacancies (red spheres) and 40 O interstitial (blue spheres) which correspond to the maximum number of defects that could be generated under our irradiation conditions according to TRIM simulations.

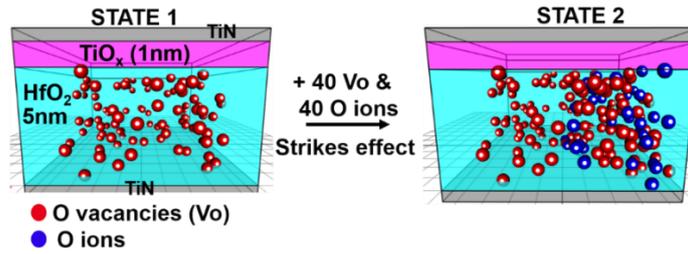


Figure 3. 22 : Sketch of the distribution and number of species (oxygen vacancies/interstitial) in the simulated device. State 1 corresponds to the device state before irradiation and state 2 corresponds to the device state after irradiation. Assuming that irradiation produces 40 additional oxygen vacancies (red spheres) and 40 oxygen interstitials (blue spheres).

I-V characteristics of the device after irradiation with additional 40 oxygen vacancies (State 2) were simulated and compared with the characteristics of the device before irradiation (State 1).

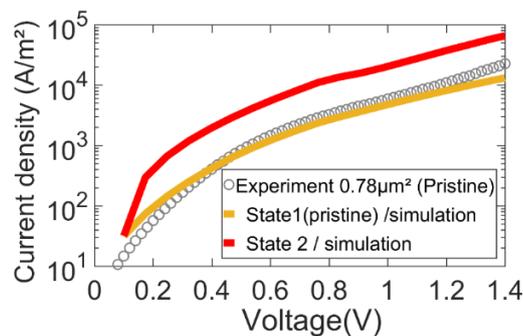


Figure 3. 23 : Simulated I–V characteristics of the device. State 1 corresponds to the situation before irradiation, (yellow curve). State 2 corresponds to the device after irradiation with 40 additional oxygen interstitial and vacancies with respect to state 1, (red curve). Symbols experimental data of pristine state before irradiation (no changes have been observed after irradiation).

The creation of new atomic defects (interstitials and vacancies) has effects on the leakage current level, it leads to a current increase clearly observed by the I–V simulations shown in Figure 3. 23 (red curve). Simulation results do not agree with experimental data showing no relevant changes of leakage current after irradiation. To investigate the experimental results, we performed a further analysis: starting from device immediately after irradiation with 40 additional  $V_O$  compared to pristine state (Figure 3. 22, state 2), we simulated the evolution of the system at room temperature by keeping the device for one hour without any bias.  $V_O$ /ions evolution during simulation is shown in Figure 3. 24. Simulations clearly show that the mutual

diffusion of oxygen ions and vacancies (affected by Coulomb attraction/repulsion) leads to their recombination. Interestingly, all the oxygen vacancies and ion interstitials created by the irradiation were recombined, bringing the device to the pristine conditions, i.e., the same number of defects as in pristine conditions.

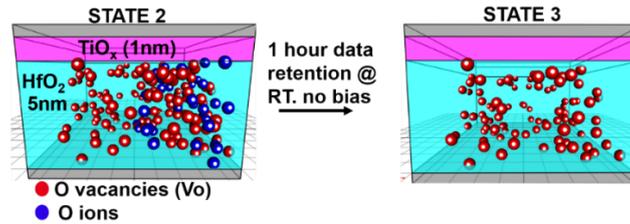


Figure 3. 24 : Sketch of the distribution and number of species (oxygen vacancies/interstitial) in the simulated device. State 2 corresponds to the device state immediately after irradiation. Assuming that irradiation produces 40 additional O vacancies (red spheres) and 40 oxygen interstitials (blue spheres). State 3 corresponds to the device state after irradiation and after one hour at room temperature annealing with no bias applied.

As expected, I–V characteristics return back to the pristine state, as shown in Figure 3. 25 (blue curve), confirming the similar electrical behavior of the device in the two states. These results are in agreement with our experimental results (tested devices do not show any differences in terms of resistance before and after irradiation), indicating that the Frenkel pair recombination driven by the attractive Coulomb field is most probably the main reason explaining the absence of degradation of the electrical performances measured on irradiated devices.

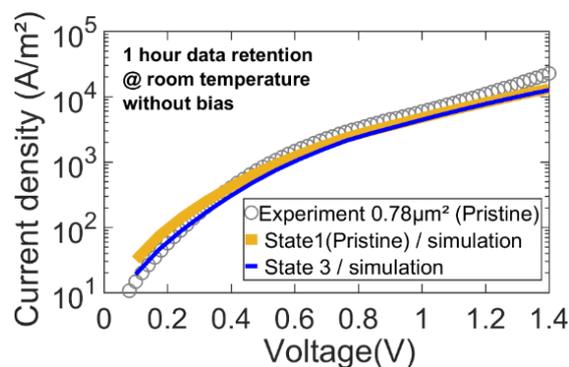


Figure 3. 25 : Simulated I–V characteristics of the device. State 1 corresponds to the situation before irradiation (yellow curve) and state 3 corresponds to the device after irradiation with 40 additional oxygen interstitial and vacancies with respect to the pristine state and after 3600 Sec. data retention at room temperature (blue curve) with no bias applied. Symbols experimental data of pristine state after irradiation (no changes have been observed after irradiation).

We investigate if an applied bias during the exposure would change this scenario by reducing the recombination of defects generated during the irradiation via the reduction of the attractive Coulomb field. In order to study this possibility, we performed the simulation assuming that the devices are biased during exposure. A voltage of 0.5 V, consistent with that typically applied during a read operation was considered to be applied for a duration of 1 s. Similar to the analysis conducted for the unbiased devices, simulations were run assuming that ion strikes randomly generate 40 oxygen interstitials and vacancies in the oxide layer. Results are illustrated in Figure 3. 26 where: (i) State 1 corresponds to the device state before irradiation, (ii) State 2 corresponds to the device under bias during irradiation and assuming that 40 additional oxygen interstitial and vacancies were generated with respect to the pristine state and (iii) State 4 corresponds to the device after irradiation under an applied bias of 0.5 V during irradiation.

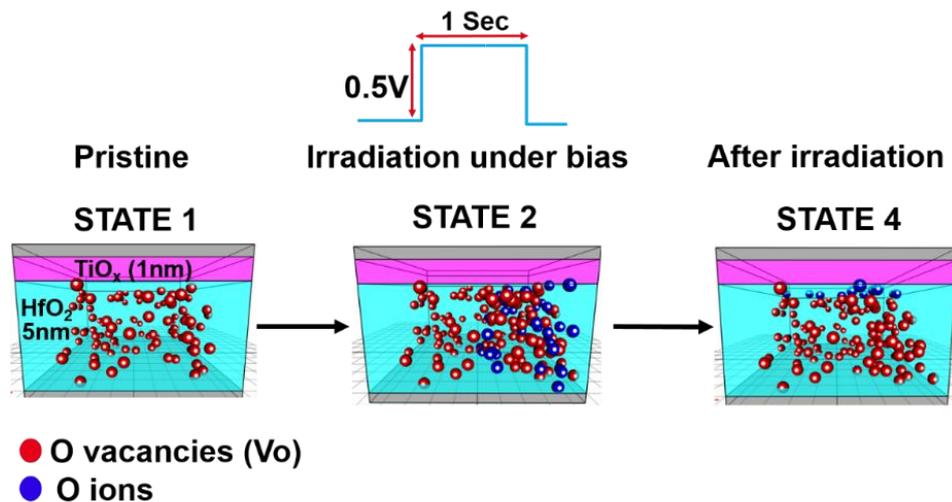
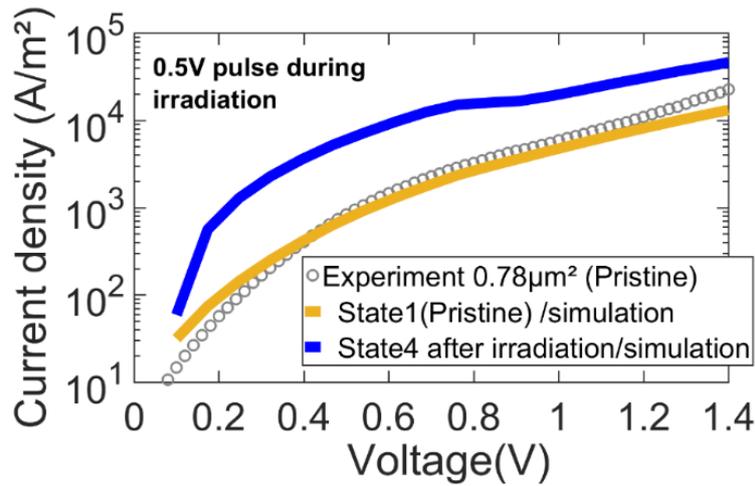


Figure 3. 26 : Sketch of the distribution and number of species (oxygen vacancies/interstitial) in the device. State 1 corresponds to the device state before irradiation. State 2 corresponds to the device under bias during irradiation and assuming that 40 additional oxygen interstitial and vacancies were generated with respect to the pristine state. State 4 corresponds to the device after irradiation under an applied bias of 0.5 V during irradiation.

The oxygen interstitials generated during irradiation do not recombine with the oxygen vacancies, as they drifted toward the top electrode driven by the applied bias. As a result, the state of the device after irradiation in biased conditions is different from the one before irradiation. A higher number of oxygen vacancies remain in the oxide layer compared to the pristine state before exposure. Additional number of  $\text{V}_\text{O}$

leads to higher leakage current after irradiation. Simulation results presented in Figure 3. 27 show higher leakage current after irradiation in biased conditions. Consequently, based on simulation results, the irradiation could potentially have measurable effects on HfO<sub>2</sub>-based RRAM exposed to heavy ions if the memory devices are in biased conditions (Read/Programming) during the exposure.



*Figure 3. 27 : Simulated I–V characteristics of the device. State 1 corresponds to the device before irradiation and state 4 corresponds to the device after irradiation with an applied bias of 0.5 V during irradiation.*

We investigated the effect of the applied bias level during irradiation on electrical characteristics after irradiation. To this purpose, we considered two biases, i.e., 0.1 and 0.5 V to study the evolution of the device. Figure 3. 28 shows the I–V characteristics simulated before and after irradiation in both unbiased and biased (with different levels) conditions, considering (as done above) 40 generated Frenkel pairs. The device could potentially show an important irradiation damage with high bias condition (0.5 V) during the strike (red curve Figure 3. 28). This damage is not very important when we are applying lower bias during irradiation, and the last state of the device after irradiation is very close to the pristine state (blue curve Figure 3. 28). Without any bias, irradiation effects cannot be observed since the generated species immediately recombine as we demonstrated previously in this section (black curve Figure 3. 28).

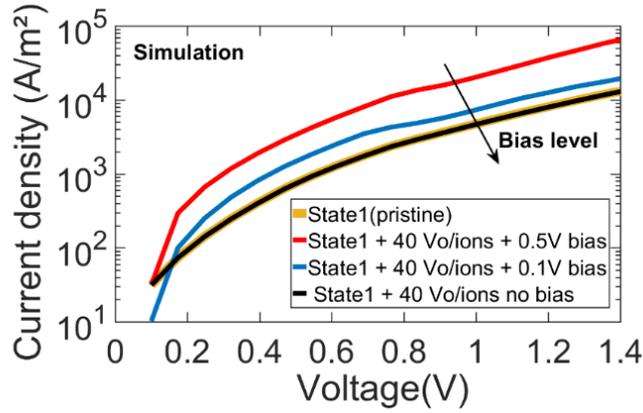


Figure 3. 28 : Simulated  $I$ - $V$  characteristics of the device with 40 generated Frenkel pairs and assuming different biases conditions during irradiation: 0.5 V (red curve), 0.1 V (blue curve), and no bias (black curve). Yellow curve stands for pristine state (state1) before irradiation.

### 3.5 Conclusions

In this chapter we demonstrated a clear effect of Al incorporation in HfO<sub>2</sub>-based RRAM. Al was found to increase the forming voltage of the memory cells compared with Al-free samples whatever the incorporation method. However, Al incorporation in HfO<sub>2</sub> improves the data retention depending on the method used to introduce Al in the memory stack. HfAlO as an alloy and bilayer devices with Al in the bottom layer improve data retention, while Al introduced by ionic implantation has no impact on data retention. In bilayer devices, a higher Al content is required to improve the data retention with the same factor of improvement compared to single-layer samples. Al doping has effects on microscopic properties of the resistive switching layer. A set of microscopic parameters was extracted experimentally from CV and TTDB experiments for different resistive switching layers, HfO<sub>2</sub>, HfAlO, Al<sub>2</sub>O<sub>3</sub>, and HfO<sub>2</sub> with 5% Al doping by the ionic implantation. The extracted parameters were used to perform physical-based simulations of the forming process. The higher forming voltage in samples with aluminum is explained by the lower dielectric constant ( $k$ ) and the lower dipole moment ( $P_0$ ) of the molecular bonds compared to pure HfO<sub>2</sub> making the bond breakage process is more difficult under electric field compared to Al-free samples. The higher forming voltage of bilayer cells, with respect to single-layer cells with the same amount of Al, is explained by the electric field redistribution between the layers. We showed that most probably there is no significant material intermixing in multilayer devices.

We investigated the direct effects of heavy ions on RRAM cells with thin HfO<sub>2</sub> layers, without any applied bias (retention mode). The experimental data show that these devices are very hard to SEEs. Cells with different sizes and in all possible resistance states were irradiated in unbiased conditions with fluences that allowed us to hit each cell multiple times. No relevant changes were observed in the irradiated cells on resistance distribution, forming voltage, reset, and set voltages. We discussed possible mechanisms that could lead to cell degradation after heavy ion exposure. By performing physics-based simulations, we reproduced the experimental results in retention mode and concluded that the cell might be sensitive if they are struck in biased conditions (Read/Programming), a new finding which will have to be confirmed with the future experiments. This is due to the fact that the radiation damage, i.e., the number of oxygen vacancy defects generated by the impinging ions and surviving the immediate recombination after the irradiation, depends on the bias applied during and after the exposure, which counteracts the Coulomb attraction.

## 3.6 References

- [1] B. Traoré, P. Blaise, E. Vianello, H. Grampeix, A. Bonneville, E. Jalaguier, G. Molas, S. Jeannot, L. Perniola, B. DeSalvo and Y. Nishi “Microscopic understanding of the low resistance state retention in HfO<sub>2</sub> and HfAlO based RRAM,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 546-549, 2014.
- [2] A. Fantini, L. Goux, S. Clima, R. Degraeve, A. Redolfi, C. Adelman, G. Polimeni, Y.Y Chen, M. Komura, A. Belmonte, D. J Wouters, M. Jurczak, “Engineering of Hf<sub>1-x</sub>Al<sub>x</sub>O<sub>y</sub> amorphous dielectrics for high-performance RRAM applications,” *2014 IEEE 6th Int. Mem. Work. (IMW)*, pp. 1-4, 2014.
- [3] L. Goux<sup>1</sup>, A. Fantini, G. Kar, Y.-Y. Chen, N. Jossart, R. Degraeve, S. Clima, B. Govoreanu, G. Lorenzo, G. Pourtois, D.J. Wouters, J.A. Kittl, L. Altimime, M. Jurczak, “Ultralow sub-500nA operating current high-performance TiN\Al<sub>2</sub>O<sub>3</sub>\HfO<sub>2</sub>\Hf\TiN bipolar RRAM achieved through understanding-based stack-engineering,” *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. 159-160, 2012.
- [4] M. Azzaz *et al.*, “Benefit of Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> bilayer for BEOL RRAM integration through 16kb memory cut characterization,” *Eur. Solid-State Device Res. Conf. (ESSDRC)*, pp. 266-269, 2015.
- [5] J. W. McPherson and H. C. Mogul, “Underlying physics of the thermochemical E model in describing low-field time-dependent dielectric breakdown in SiO<sub>2</sub> thin films,” *J. Appl. Phys.*, vol. 84, no. 3, pp. 1513-1523, 1998.
- [6] J. Frascaroli, F. G. Volpe, S. Brivio, and S. Spiga, “Effect of Al doping on the retention behavior of HfO<sub>2</sub> resistive switching memories,” *Microelectron. Eng.*, vol. 147, pp. 104-107, 2015.
- [7] B. Traore *et al.*, “On the Origin of Low-Resistance State Retention Failure in HfO<sub>2</sub>-Based RRAM and Impact of Doping/Alloying,” *IEEE Trans. Electron Devices*, vol. 62, no. 12, pp. 4029-4036, 2015.
- [8] J. McPherson, J. Y. Kim, A. Shanware, and H. Mogul, “Thermochemical description of dielectric breakdown in high dielectric constant materials,” *Appl. Phys. Lett.*, vol. 82, no. 13, pp. 2121-2123, 2003.
- [9] X. He, W. Wang, B. Butcher, S. Tanachutiwat, and R. E. Geer, “Superior TID Hardness in TiN/HfO<sub>2</sub>/TiN ReRAMs After Proton Radiation,” *IEEE Trans. Nucl. Sci.*, vol. 59, no. 5, pp. 2550-2555, 2012.
- [10] Y. Wang *et al.*, “Highly stable radiation-hardened resistive-switching memory,” *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1470-1472, 2010.
- [11] S. L. Weeden-Wright *et al.*, “TID and displacement damage resilience of 1T1R HfO<sub>2</sub> Resistive Memories,” *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 2972-2978, 2014.
- [12] D. R. Hughart *et al.*, “A Comparison of the Radiation Response of TaOx and TiO<sub>2</sub> Memristors,” *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4512-4519, 2013.
- [13] M. L. McLain *et al.*, “The susceptibility of TaOx-based memristors to high dose rate ionizing radiation and total ionizing dose,” *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 2997-3004, 2014.
- [14] M. L. McLain and M. J. Marinella, “Overview of the radiation response of anion-based memristive devices,” *IEEE Aerosp. Conf. Proc.*, 2015.

- [15] C. Sire, S. Blonkowski, M. J. Gordon, and T. Baron, "Statistics of electrical breakdown field in HfO<sub>2</sub> and SiO<sub>2</sub> films from millimeter to nanometer length scales," *Appl. Phys. Lett.*, vol. 91, no. 24, 2007.
- [16] Y. S. Chen *et al.*, "Highly scalable hafnium oxide memory with improvements of resistive distribution and read disturb immunity," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 105–108, 2009.
- [17] H. S. P. Wong *et al.*, "Metal-oxide RRAM," in *Proceedings of the IEEE*, vol. 100, no. 6, pp. 1951–1970, 2012.
- [18] W. G. Bennett *et al.*, "Single- and multiple-event induced upsets in HfO<sub>2</sub>/Hf 1T1R RRAM," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 4, pp. 1717–1725, 2014.
- [19] S. R. Bradley, G. Bersuker, and A. L. Shluger, "Modelling of oxygen vacancy aggregates in monoclinic HfO<sub>2</sub>: can they contribute to conductive filament formation?," *J. Phys. Condens. Matter*, vol. 27, no. 41, p. 415401, 2015.
- [20] A. Padovani, L. Larcher, G. Bersuker, and P. Pavan, "Charge Transport and Degradation in HfO<sub>2</sub> and HfO<sub>x</sub> Dielectrics," *IEEE Electron Device Lett.*, vol. 34, no. 5, pp. 680–682, 2013.
- [21] A. Padovani, L. Larcher, O. Pirrotta, L. Vandelli, and G. Bersuker, "Microscopic modeling of HfO<sub>x</sub> RRAM operations: From forming to switching," *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1998–2006, 2015.

# Chapter 4

## Access devices for HfO<sub>2</sub> based RRAM

### 4.1 Introduction

Cross point architecture is considered to be a very promising integration method to achieve large memory arrays. In these architectures, an access device is required. An ideal selector should have high current at high voltage (“pass” state, allows enough access voltage drops over the resistive memory element) as well as very low current at low voltages (“blocking” state) simultaneously, this translates into highly non-linear I-V characteristics. I-V selectivity can be included by either NVM devices with intrinsic selectivity (e.g. self-rectifying cells (SRC) with tunnel barrier) or by adding a serial access device with the storage element at each cross point in the memory array. Several selector technologies are under investigation today to achieve the best performances for cross point integration as we discussed in chapter 1 section 1.6.

In this chapter, we first propose multilayer HfO<sub>2</sub> based RRAM devices with tunnel barriers that show a self-rectifying behavior and intrinsic selectivity. Then, we introduce our 1S1R structure using an OTS selector with HfO<sub>2</sub> based RRAM cells. For the multilayer devices with tunnel barriers, we have demonstrated LRS selectivity with low operating current  $\sim 10\mu\text{A}$  and multilevel resistance suitable for neuromorphic applications. For, the 1S1R with OTS access device, we have presented a detailed investigation of the main 1S1R memory operations, (i.e. Forming, Set, Reset and Read). In addition, we have demonstrated better LRS selectivity compared to multilayer devices with tunnel barrier and possible OTS material engineering to improve the selectivity of the 1S1R device.

## 4.2 Oxide tunnel barrier

### 4.2.1 RRAM samples

The RRAM cells studied are composed of three oxides ( $\text{HfO}_2$ ,  $\text{Al}_2\text{O}_3$  and  $\text{TiO}_x$ ) with different thicknesses and sandwiched between TiN top and bottom electrodes. One of the oxide layers is supposed to play the role of the active layer in the memory stack where the construction and rupture of the CF occurs. The other layers are considered as tunnel barriers enhancing the current non-linearity of the memory cells. The programming operations (Forming and Set) should be controlled in order to prevent the full Set process and the creation of a metallic CF into the full memory stack, thus preserving the tunneling barriers. Figure 4. 1 shows the schematic of (i) S1 that consists of two layers device with 5nm- $\text{HfO}_2$  and 2.5-nm  $\text{TiO}_x$ , (ii) S2 the tri-layers device of 3nm- $\text{Al}_2\text{O}_3$ , 3nm- $\text{HfO}_2$  and 2.5-nm  $\text{TiO}_x$  and (iii) S3 tri-layers device that is represented by 5nm- $\text{Al}_2\text{O}_3$ , 3nm- $\text{HfO}_2$  and 2.5-nm  $\text{TiO}_x$ .  $\text{HfO}_2$  and  $\text{Al}_2\text{O}_3$  were deposited by atomic layer deposition (ALD) process, while  $\text{TiO}_x$  was formed by Chemical Vapor Deposition (CVD) and thermal annealing in oxygen ambient at 350 °C. All the studied devices are in 1R structure without any access devices (e.g. transistor).

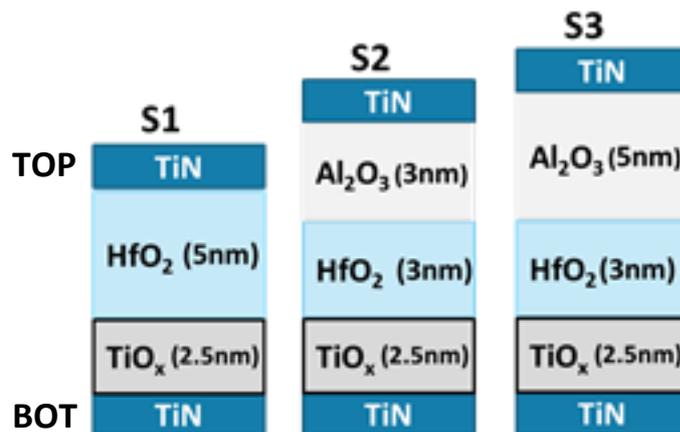


Figure 4. 1 : Schematic illustration of the two and tri-layer explored devices

## 4.2.2 Set processes

Ramped voltage mode was adopted to program the cells. During the Set operation, the programming voltage is applied either on the top or bottom electrode of the memory device. Different Set trends have been identified, i.e. *abrupt*, *gradual* and *two steps* depending on the memory stack and polarization scheme (top or bottom polarization).

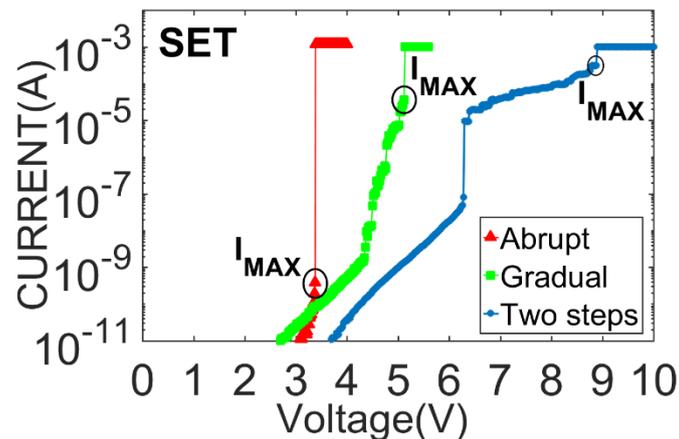


Figure 4. 2: I-V curves for the three different identified Set processes: abrupt (red, S1 sample), gradual (green, S2 sample) and two-steps (blue, S3 sample).  $I_{MAX}$  is the maximum current before the full Set process.

**Abrupt Set:** The S1 and S2 samples present an abrupt Set if the programming voltage is applied on the active electrode (BOT). The abrupt behavior is typical for RRAM cells. The current jumps abruptly at the forming voltage indicating the switching from pristine/HRS states to LRS (red curve in Figure 4. 2).

**Gradual Set:** The S1 and S2 samples show a gradual Set if the programming voltage is applied on the inert electrode (TOP). The current increases gradually indicating a gradual switching between pristine/HRS states and LRS, as shows the green curve in. Figure 4. 2

**Two steps Set:** The S3 sample shows two steps Set behavior in both polarization schemes. In this case the I-V characteristics show three different regions. The first region where the current jumps abruptly. The second one is an analog region as the current increases gradually. Finally, a second current jump indicates the full set process.

*Table 4. 1 : Identified Set processes as a function of the polarization scheme (Set voltage applied to the bottom or top electrode) for the different studied memory samples.*

<b>Device</b>	<b>TOP POLAR scheme</b>	<b>BOT POLAR scheme</b>
<b>S1</b>	Gradual	Abrupt
<b>S2</b>	Gradual	Abrupt
<b>S3</b>	Two steps	Two steps

In Table 4. 1, we summarize the different Set processes as function of the polarization scheme for the different samples. The active electrode in RRAM technology serves as oxygen scavenging layer. The latter is essential for the memory device functionality. When a positive electric field is applied on the active electrode, the negatively charged oxygen ions are driven toward the scavenging layer. This allows the creation of a CF in the active oxide layer. For S1 and S2: on the one hand, when the electric field is applied on the bottom ( $\text{TiO}_x$  side), the oxygen ions migrate toward  $\text{TiO}_x$  layer. In this case, the  $\text{TiO}_x$  plays the role of the active electrode. Consequently, this results to a typical abrupt switching. On the other hand, when the electric field is applied on the top electrode, the oxygen ions will be driven toward an inert electrode (TiN). Thus, the ions will remain either in  $\text{Al}_2\text{O}_3$  or  $\text{HfO}_2$  layer. In this case, the recombination process between ions and vacancies remains dominant. Consequently, the defect creation rate is quite low which leads to slow formation of the CF (gradual Set). For S3 samples, the effect of electric field distribution between the different layers (demonstrated in chapter 3 section 3.3) is dominant because of the difference in the oxide thicknesses and the dielectric constant of each material. Most of the electric field drops on the layer having the lower dielectric constant ( $\text{Al}_2\text{O}_3$  in this case). After the forming of a CF in the first layer, the electric field drops on the remaining pristine layer having higher resistance. This leads to the creation of a CF into the second layer. The two steps behavior indicates a widely separated breakdown of each oxide layer in the memory stack. Physics based simulation will be performed (in the next section) for S3 samples to deepen understanding the two steps behavior during the Set process.

### 4.2.3 Modeling and simulation

To investigate the two steps switching observed in the S3 samples at the microscopic level, we have performed physics based simulations using the Ginestra™ simulation package. We use the microscopic properties derived from TDDDB and C-V measurements for HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> materials (values reported in chapter 3 section 3.3 Table 3.2). We have first considered the simulation of the Set process in S1 sample that shows a strongly abrupt behavior. The CF is formed abruptly into the entire HfO<sub>2</sub> layer resulting in a process that is hard to be finely controlled as shown in Figure 4. 3.

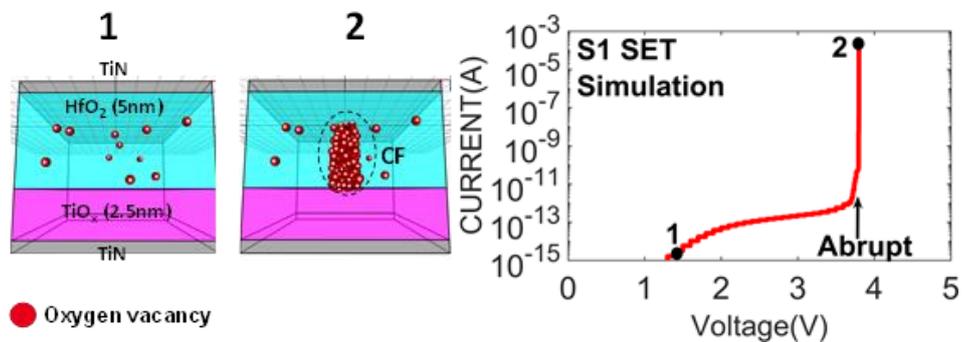
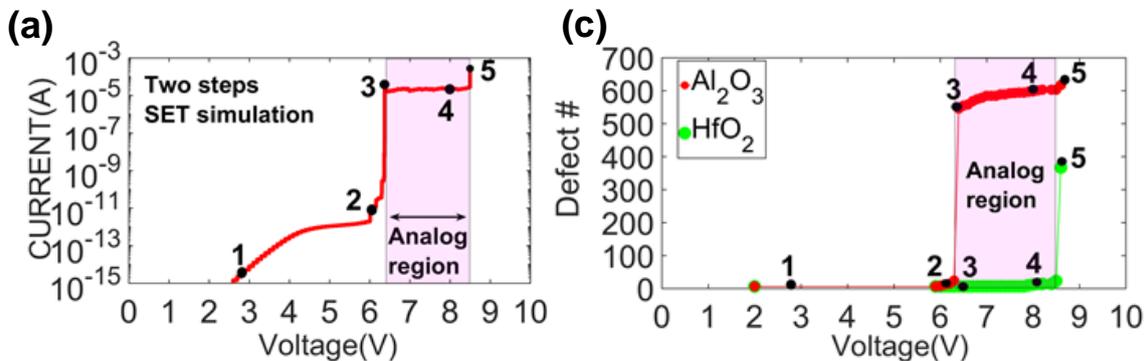


Figure 4. 3 : Simulated I/V characteristic of the Set process for the S1 sample. Simulation reproduces the abrupt Set observed in experimental data (Figure 4. 2, red curve).

We included later the Al<sub>2</sub>O<sub>3</sub> layer as shown in Figure 4. 4-b (S3 samples). Simulations reproduce accurately the experimental two steps I-V characteristics (Figure 4. 4-a). In this case, the CF is formed first in the Al<sub>2</sub>O<sub>3</sub> layer (first step) then in the HfO<sub>2</sub> (second step) as shown in Figure 4. 4-b.



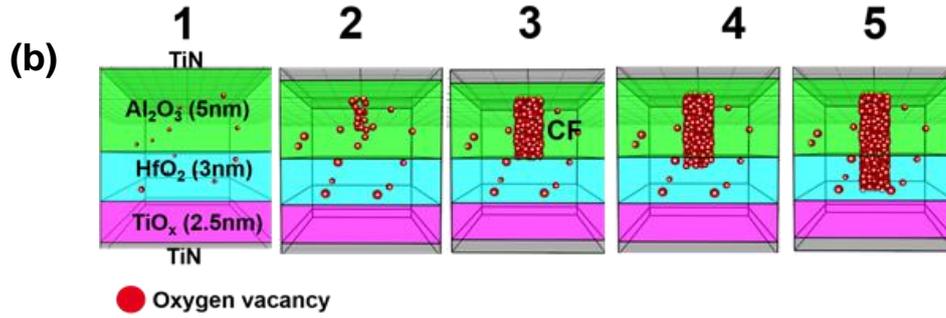


Figure 4. 4 : (a) Simulated I/V characteristic of the Set process for the S3 sample. (b) Corresponding evolution of defect creation in the HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> layers. (c) CF evolution during the Set process.

Figure 4. 4-c shows the evolution of the number of defects as a function of the applied voltage. As seen, an abrupt increase of the defects occurs in Al<sub>2</sub>O<sub>3</sub> layer (between stages 2 & 3) which corresponds to the first step in the I-V characteristic. Afterwards, a gradual increase of the number of defects in the Al<sub>2</sub>O<sub>3</sub> layer was shown (between stages 3 & 4) that corresponds to the analog switching between the first and the second step. Finally, another abrupt increase of the defects in the HfO<sub>2</sub> layer is observed at higher voltage (between points 4 & 5) corresponding to the full Set process.

#### 4.2.4 Operating regions

To maintain the tunnel barrier effect, the full Set process of the multilayer devices (S1, S2 and S3) must be avoided. The programming conditions are defined so that a CF is created in one layer of the memory stack and the other layer remains in its pristine state to play the role of a tunnel barrier.

We have investigated the effects of the programming current level on LRS stability. Set process with different current levels was performed on S2 samples. After Set process the resistance state of the programmed devices was monitored during time.

For programming currents lower than 0.5μA, the LRS is unstable during time (volatile behavior) as shown in Figure 4. 5. The red region in Figure 4. 5 corresponds to the current levels that lead to volatile switching. In this region the resistance shifts toward higher resistance values after few seconds in data retention mode. Based on these results, a programming current higher than 1μA must be delivered

to the memory devices during Set operation to obtain a non-volatile behavior (memory effect).

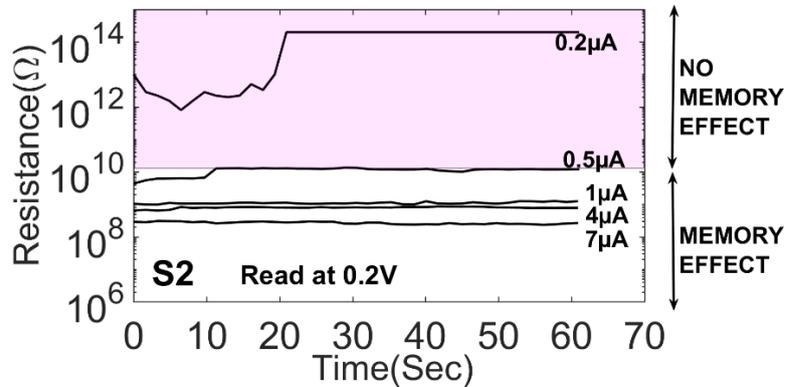


Figure 4. 5 : Resistance evolution as a function of time for different programming currents values. The LRS is volatile for programming current values lower than  $0.5\mu A$  (red region).

We define  $I_{MAX}$  as the maximum current that can be achieved before the current jump corresponding to the full Set process (see Figure 4. 2). We report in Figure 4. 6 the extracted  $I_{MAX}$  values for the different samples and different polarization schemes. Based on the results shown in Figure 4. 5 on the relationship between the programming current and LRS stability, we divide the plot below (Figure 4. 6) into two regions: the *memory effect* region and the *no memory effect* region (red region). The current value separating the two regions is about  $0.5\mu A$ . S1 and S2 show an abrupt Set process if the bottom polarization scheme is adopted. In this case,  $I_{MAX}$  is always lower than  $0.5\mu A$  as shown in Figure 4. 6 (red histogram). It is not therefore possible to achieve a stable LRS. S1 and S2 show a gradual Set behavior if the top polarization scheme is adopted, and S3 shows a two-step Set regardless to the polarization scheme. Consequently, a range of programming currents that allow achieving a stable LRS without a complete conductive filament formation exists in the case of S1 and S2 with top polarization scheme and S3 with both polarization schemes (green and blue histograms in Figure 4. 6).

We were not able to perform the Reset process for S3 samples if top polarization scheme is adopted during Set operation. Therefore, we adopted the bottom polarization scheme for S3 in our study.

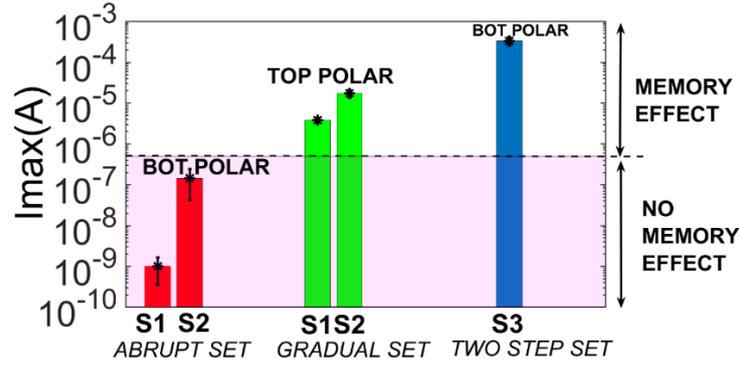


Figure 4. 6 : Maximum programming current that can be achieved before the full Set process in the different samples (defined in Figure 4. 2). The LRS is volatile for programming current values lower than  $0.5\mu\text{A}$  (red region)

#### 4.2.5 Self-rectifying behavior and LRS selectivity

In this section, we analyze the electrical characteristics of S2 sample with top polarity and S3 sample with bottom polarity, which show a gradual Set and two steps Set, respectively. For both samples, we extracted the selectivity (NLF: Non-Linearity Factor).

Figure 4. 7 shows the I-V characteristics of partial-Set and Reset processes for the S2 sample (gradual Set). The selectivity Factor, NLF, is defined as:

$$NLF = I @ V_{Set} / I @ \frac{1}{2} V_{Set}.$$

S2 and S3 samples show a self-rectifying behavior, thus not requiring any access devices (e.g. transistor) to limit the current during the Forming/Set operations and to avoid the current overshoot issue. The applied voltage controls the current level.

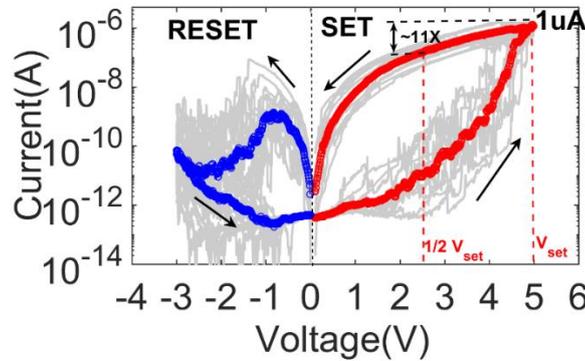
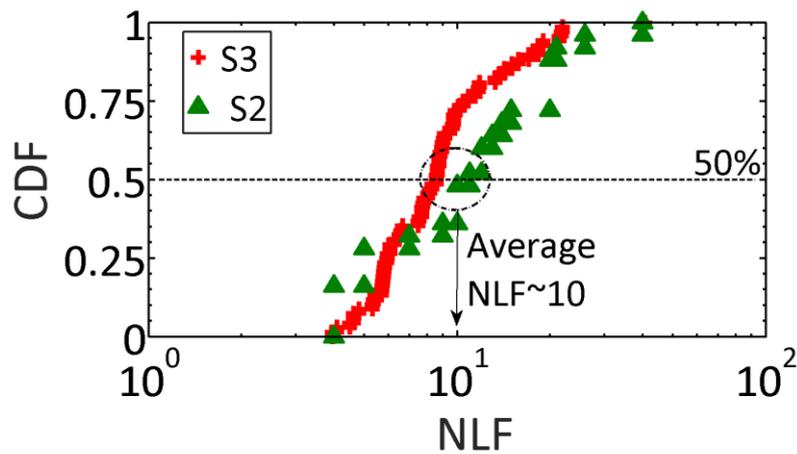


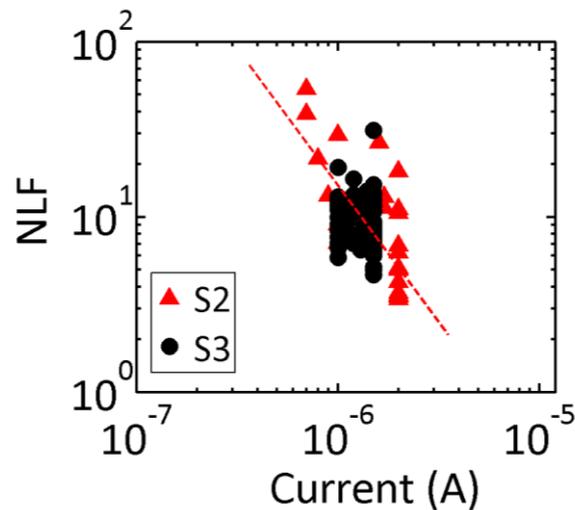
Figure 4. 7 : I/V plot showing the partial-Set and Reset characteristics for the S2 samples (gradual Set). The method adopted to extract the NLF is put in evidence.

NLF  $\sim 10$  is the average value extracted for these samples (S2 and S3) with a programming current of  $\sim 1\mu\text{A}$  as shown in Figure 4. 8.



*Figure 4. 8 : NLF distributions extracted for S2 and S3 samples at  $\sim 1\mu\text{A}$  of programming current. Average NLF of  $\sim 10$  is extracted for both samples*

We extracted the NLF with different programming currents. The values are reported in Figure 4. 9.



*Figure 4. 9 : Extracted NLF vs programming current for the S2 and S3 samples.*

The NLF depends on the compliance current imposed during the set process: the higher the compliance current, the lower the NLF. This dependence is explained by the fact that higher compliance current reduces the tunneling barrier height, thus reducing also the current selectivity associated to the tunneling effect.

The NLF extracted for the studied samples (around 10) is relatively low compared to the values required ( $>10^3$ ) to enable the implementation of high density 1S1R arrays as reported in [1][2].

#### 4.2.6 Multilevel resistance for neuromorphic systems

Resistive memories (RRAM) are considered as a promising solution for modeling key features of biological synapses [3], [4]. Most of the OxRAM and CBRAM cells are intrinsically binary devices: they switch between two distinct resistance states: (i) Low Resistance State (LRS) and (ii) High Resistance State (HRS) when appropriate identical Set/Reset pulses are applied. The use of only two resistance levels per synapse, with respect to the multi-level approach, can present disadvantages in terms of performances in neuromorphic systems designed for some complex applications, as for example image recognition [5]. The ideal RRAM synapse presents an analog switching under identical pulses in both programming directions (Set and Reset).

We have explored the resistance evolution by applying cumulative ramped stress to the samples with abrupt, gradual and two steps Set. Figure 4. 10-(a-c) shows the current–voltage (I–V) curves under cumulative ramped stress (left) and the corresponding resistance evolution (right) for the S1, S2 and S3 samples respectively. For the abrupt Set there is no memory effect before the full Set process at  $\sim 3.2\text{V}$ . Only two distinct resistance states can be achieved (binary switching). A memory effect is observed during cumulative voltage ramping for the devices with gradual and two steps Set processes (S2 and S3) before the full conductive filament formation ( $I_{\text{Set}} < I_{\text{MAX}}$ ). Multilevel resistance states can be obtained with the incremented Set pulses, (analog regions in red in Figure 4. 10).

S3 samples show larger analog region compared with S2 samples as shown in Figure 4.10-(b-c), this allows achieving more resistance levels in the case of S3 samples.

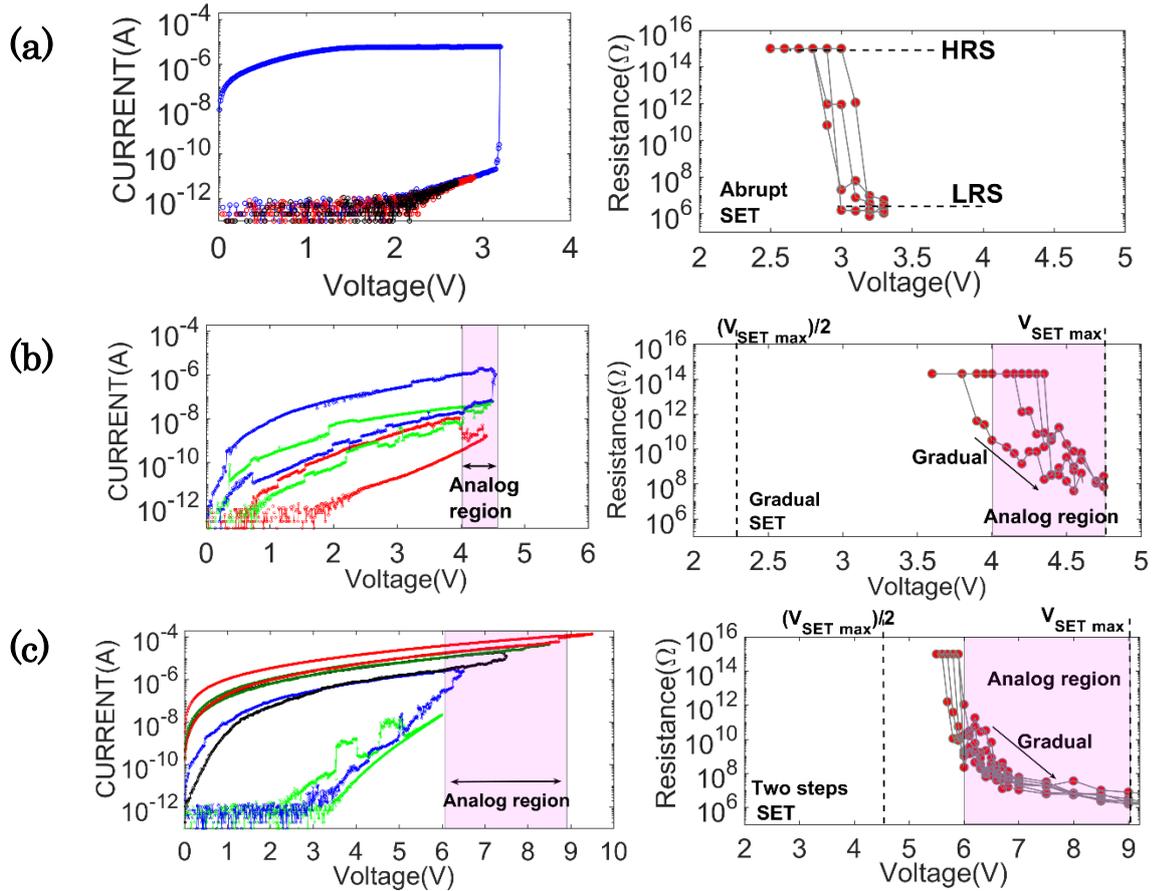
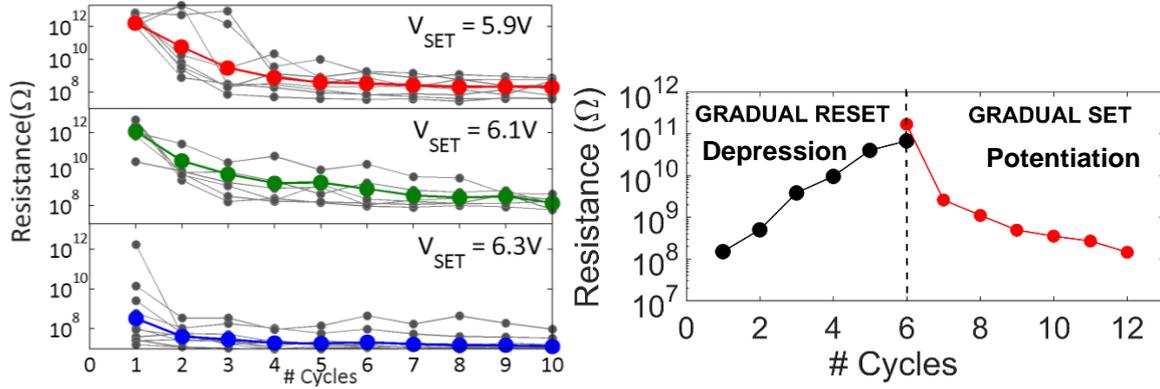


Figure 4. 10 :  $I$ - $V$  characteristics under cumulative ramped stress (left) and resistance evolution (right) for: (a) S1 with abrupt Set, (b) S2 with gradual Set and (c) S3 with two steps Set.

We focused our analysis on the synaptic characteristics of S3 by analyzing its behavior when applying successive identical pulses during the Set/potential operation.

Gradual decrease of the resistance level under identical pulses was demonstrated for a programming current of  $\sim 1\mu\text{A}$  as shown in Figure 4. 11. The barrier layer allows avoiding the abrupt formation of CF, thus, achieving an analog switching and a certain selectivity in the LRS. Figure 4. 11 (right) evaluates the synaptic characteristics that satisfy the modulation of the conductance under identical Set (potentiation) and Reset (depression) pulses. Typically, the Reset operation of RRAM devices is a gradual process, consequently, gradual depression is easier to achieve with respect to gradual potentiation in filamentary RRAM.



*Figure 4.11 : Analog switching under constant ramped voltage stress for the S3 (two steps Set). Color line: median of over 10 devices. This behavior is equivalent to synaptic potentiation (left). Example of potentiation and depression behavior by applying identical pulses of 5.9V and -1V respectively (right).*

### 4.3 OTS based access device

Among different selector technologies, the Ovonic Threshold Switching (OTS) selector devices are considered as one of the best candidate due to their high on current and high selectivity, both necessary for the implementation of large memory arrays [6]–[10]. The basic OTS working principle is a field induced volatile switching between a high resistance (OFF state) and low resistance (ON state), which has been first demonstrated by Ovshinsky in chalcogenide materials.

In this section, we present a non-volatile memory built by staking an HfO<sub>2</sub>-based RRAM with GeSe-based OTS selector. We explore in details the main memory operations of a one-selector/one-resistor (1S1R) device. In addition, we propose an innovative non-disruptive read strategy that strongly reduces power consumption in the memory arrays.

#### 4.3.1 1S1R: device structure and material characterization

The storage element in the 1S1R device is composed of 10-nm SiO<sub>x</sub> (x<1)/10-nm HfO<sub>2</sub> resistive switching layer embedded between TiN and Ti/TiN bottom and top electrodes respectively. The 1S selector, deposited by PVD on the Ti/TiN RRAM top electrode, is composed of a 25-nm Se-rich GeSe (Ge<sub>30</sub>Se<sub>70</sub>) layer and a TiN top electrode. Material characterization was performed to figure out the materials

profile that 1S1R device consist of. Figure 4. 12-a shows the TEM cross-section of the 1S1R device with the EDX spectra of the GeSe selector. Figure 4. 12-b illustrates the EDX profile of the full 1S1R structure, this profile shows sharp separation among the integrated layers without any material intermixing in the 1S1R device.

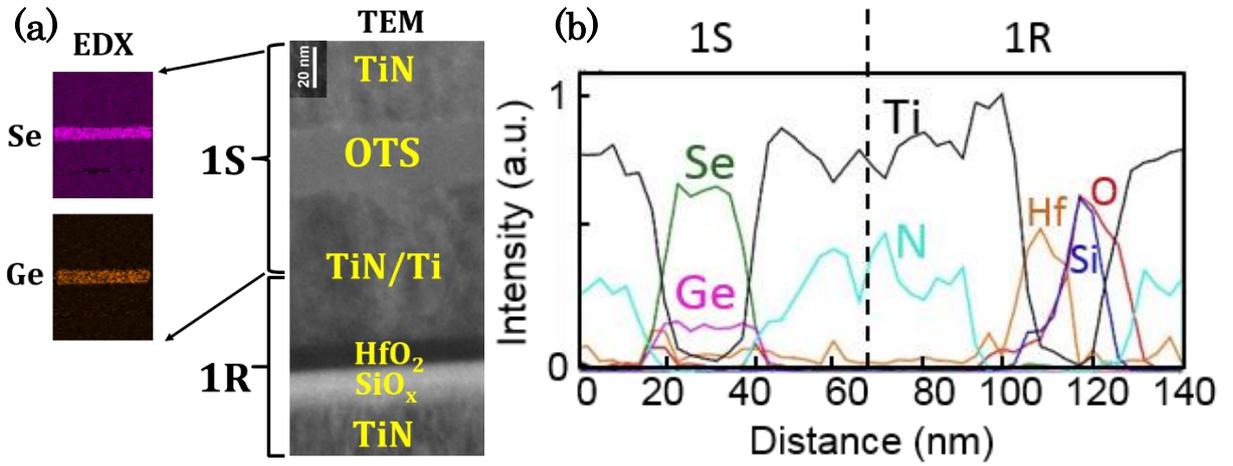


Figure 4. 12 : (a), TEM cross-section of the 1S1R device and EDX spectra of the selector, (b) EDX profile of the 1S1R structure.

### 4.3.2 Measurements Setup

To characterize the 1S1R device and to demonstrate its functionality, we have designed a measurement setup based on semiconductor parameter analyzer (HP4156) and pulse generator as shown in Figure 4. 13. A series resistance ( $R_{ext}$ ) of 10k $\Omega$  is mounted to monitor the current through the tested device during pulse measurements. Moreover, this  $R_{ext}$  allows to control the current after Low Resistance (LRS) switching of the non-volatile memory (1R). We denote by  $V_{applied}$  the applied voltage on the series of  $R_{ext}$  and the device under test (i.e. 1S, 1R or 1S1R). The voltage drop on tested device is monitored during the pulse application ( $V_{1S,1R,1S1R}$ ). The corresponding current value is determined as follow:

$$I_{1S}, I_{1R}, I_{1S1R} = \frac{V_{applied} - V_{1S,1R,1S1R}}{R_{ext}} \quad (4.1)$$

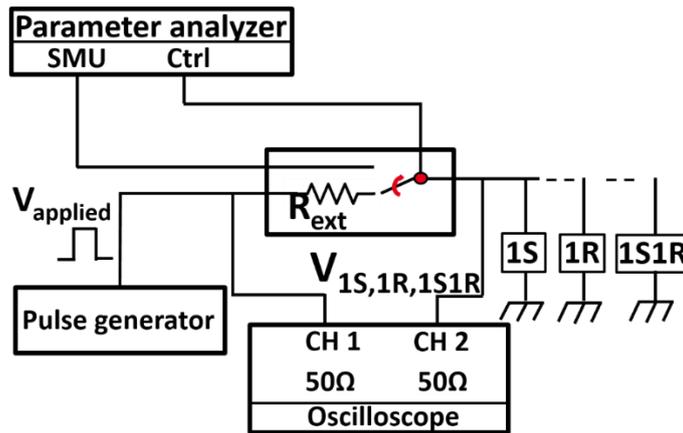


Figure 4. 13 : Experimental Setup for the characterization of the 1S, 1R and 1S1R structures.

### 4.3.3 RRAM memory cell (1R) characteristics

Figure 4. 14 reports the V-time curves during pulsed forming operation on RRAM memory cell (1R). The red curve is the voltage applied on  $R_{ext}$  plus the 1R device, the black curve is the voltage drop on the 1R. Long pulses ( $\sim 30\mu s$ ) have been used to better explain the dynamics of the switching event. The switching between the pristine state and the LRS (point 1 in Figure 4. 14) is achieved when the applied bias exceeds the forming voltage ( $V_f$ ). At the switching point the RRAM resistance decreases abruptly from very high resistance (pristine state) to LRS. Consequently, the voltage drop on 1R device decreases abruptly at this point which is an indication of the switching event as shown in Figure 4. 14 (black curve).

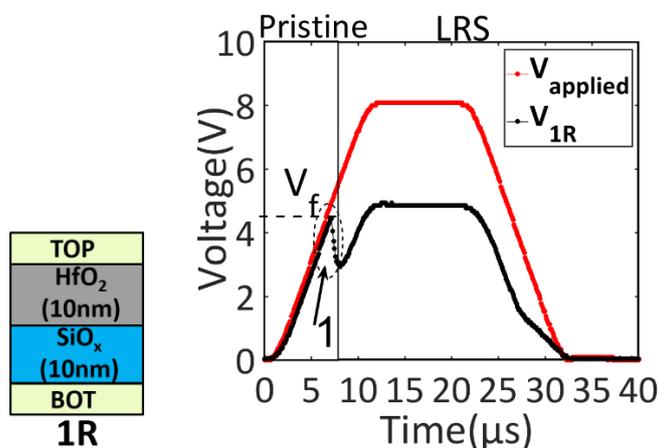


Figure 4. 14 : (left) Schematic illustration of the 1R device, (right) measured V-time of the total applied voltage (red curve) and the voltage drop on the 1R device (black curve).

The V-time data (Figure 4. 14) could be converted to current-voltage using equation (4.1) as shown in Figure 4. 15. The dynamic I-V characteristic shows that the programming current,  $I_{prog}$ , is  $\sim 300\mu A$ .

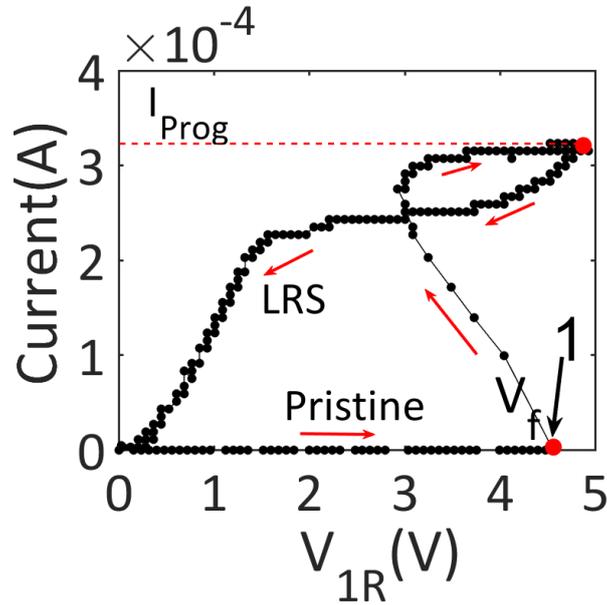


Figure 4. 15 : I-V curve of the forming process for the 1R device. Data obtained by applying equation (4.1) on V-time data in Figure 4. 14.

After forming, Set/Reset cycling was performed on 1R device by using the measurement Setup presented in section 4.3.2. Typical resistance distribution is shown in Figure 4. 16, a memory window of about 3 decades is demonstrated.

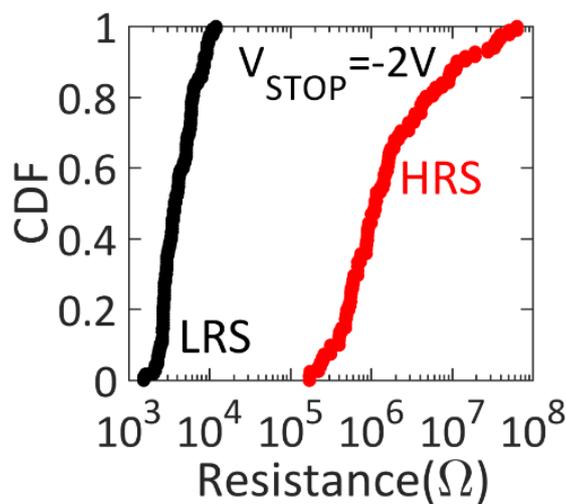


Figure 4. 16: cumulative distributions of LRS/HRS resistances.  $V_{STOP} = -2V$  is the negative voltage applied during Reset operation.

### 4.3.4 Selector device (1S) characteristics

Typically, OTS selectors show an abrupt switching from an initial high resistance “OFF” state into a highly conductive dynamic “ON” state once the applied voltage exceeds the threshold voltage,  $V_{th}$ . The device remains in the ON state so long as a minimum holding voltage,  $V_{hold}$ , (or current  $I_{hold}$ ) is present across the device, otherwise the selector switches back into the OFF state.

The 1S device characterization during pulse application is reported in Figure 4. 17. The volatile switching from the high resistance state (OFF) to the low resistance state (ON) occurs at  $V_{th}^+$  (1), that corresponds to the threshold voltage in positive polarity. The selector switches back to its OFF state when the applied voltage is decreased below  $V_{hold}^+$  (2). The latter corresponds to the minimum voltage drop on the 1S to ensure a current higher than  $I_{hold}^+$  in positive polarity. At point (2) in Figure 4. 17-b, the voltage drop across the 1S (black curve) increases which is an indication of the switching event to the OFF state. The same switching behavior is obtained for negative pulses, demonstrating that the 1S device allows bipolar volatile switching. The access device bipolar behavior is mandatory to perform Set/Reset operations in bipolar RRAM cells. Figure 4. 17-c shows the I-V characteristics of the 1S device under programming pulses with opposite polarities. An  $I_{hold} \sim 200\mu A$  in both polarities (positive and negative) is needed to keep the selector in the ON state. A series resistance of  $1K\Omega$  ( $R_{ext}$  in Figure 4. 13) is adopted during the characterization of the 1S device.

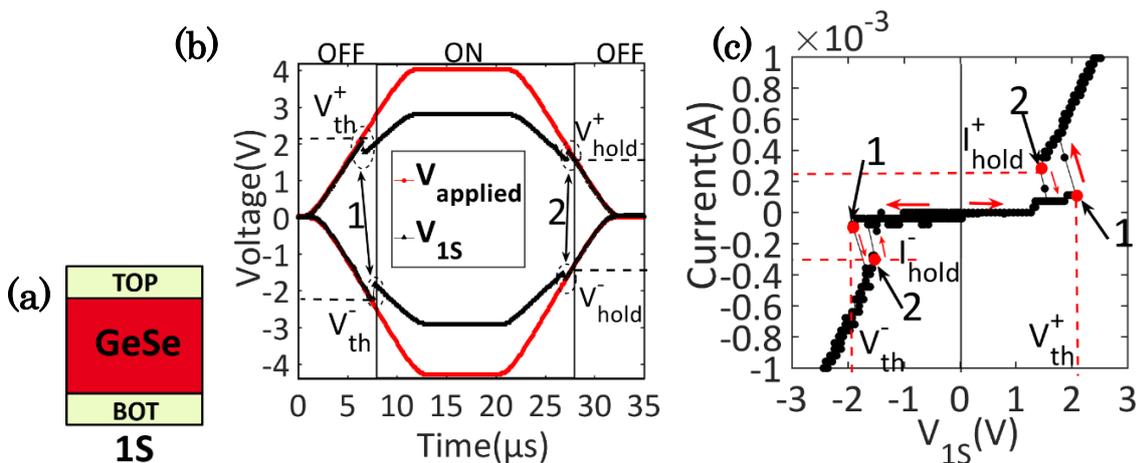


Figure 4. 17 : Illustration of 1S device (a). V-time (b) and I-V (c) curves during pulse application in different polarity demonstrating that the OTS selector is bipolar.  $R_{ext}$  (see Figure 4. 13) of  $1K\Omega$  is adopted during the 1S characterization.

The  $V_{th}$  and  $V_{hold}$  distributions extracted from several cells cycling data are plotted in Figure 4. 18. Equality between  $V_{th}^+$  and  $V_{th}^-$  (Figure 4. 18-left) distributions confirms the bipolar and the symmetric behavior of 1S device. The holding voltage is about 0.5V lower than the threshold one (Figure 4. 18-right). These voltages ( $V_{th}$  and  $V_{hold}$ ) are intrinsic properties of the GeSe material.

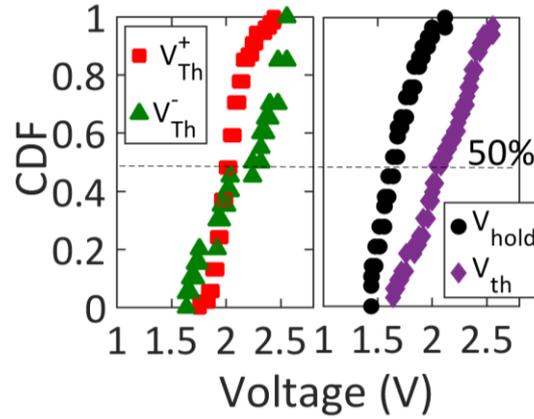


Figure 4. 18 : (left)  $V_{th}^+$  and  $V_{th}^-$  distributions obtained on several cells during cycling. (right)  $V_{th}$  ( $V_{th}^+$  and  $V_{th}^-$ ) and  $V_{hold}$  ( $V_{hold}^+$  and  $V_{hold}^-$ ) distributions obtained on several cells during cycling.

### 4.3.5 1S1R characteristics (Forming/Reset/Set)

After we characterized separately the RRAM (1R) and the access device (1S) to ensure the desired functionality for each device, we investigated the characteristics of the RRAM cell co-integrated with the selector device (1S1R). In the following the main memory operations (Forming/Set/Reset) are presented.

#### 4.3.5.1 Forming operation

Figure 4. 19-(b-c) present the V-time and I-V curves during pulsed forming operation of 1S1R device respectively.  $V_{applied}$  (red curve) is applied on  $R_{ext}$  and the 1S1R. When the voltage drop across the selector reaches  $V_{th}$  (black curve Figure 4. 19-b), the selector switches to the ON state, simultaneously the voltage drops on the 1R cell giving rise to its abrupt forming operation (point 1 Figure 4. 19-b). When the voltage on the selector decreases below the holding voltage the selector switches back to its OFF state while the non-volatile memory 1R remains in the LRS (point 2 Figure 4. 19-b). V-time curve (black curve in Figure 4. 19-b) is converted to the I-V

characteristics during forming operation of 1S1R device as shown in Figure 4. 19-c. The programming current,  $I_{\text{prog}}$ , is  $\sim 300\mu\text{A}$ .

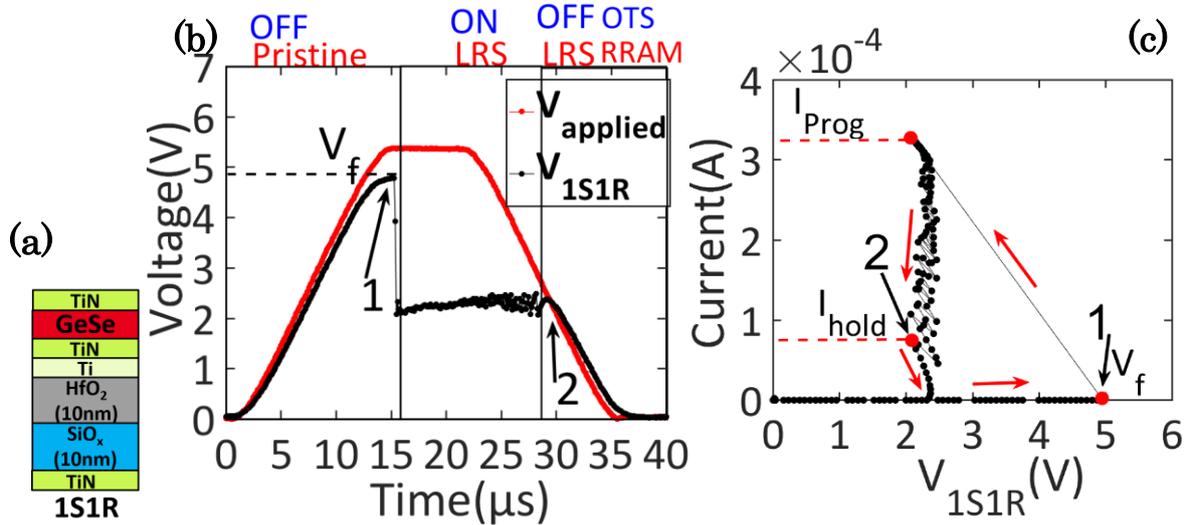


Figure 4. 19 : Schematic illustration of 1S1R device (a). V-time (b) and I-V (c) curves during forming. When  $V_{1S1R}$  exceeds  $V_f$  the 1S switches from the OFF state to ON state and at the same time the 1R switches from the pristine state to the LRS (1). When current is reduced below  $I_{\text{hold}}$  the 1S recovers the OFF state (2).

#### 4.3.5.2 Reset operation

After the forming operation, a negative pulse must be applied on 1S1R device in order to perform the Reset operation since the memory cell (1R) is bipolar. Figure 4. 20-(a-b) shows the V-time and I-V characteristics of the 1S1R during the Reset operation (the absolute value of the voltage is plotted). When the voltage drop across the selector reaches  $V_{\text{th}}$  the selector switches to the ON state (point 1 Figure 4. 20), this corresponds to current increase through the 1S1R. The Reset starts when the current exceeds  $I_{\text{Reset}}$  (point 2 Figure 4. 20), then, the voltage across the 1S1R device ( $V_{1S1R}$ ) increases gradually indicating the increase of the 1R resistance. When the voltage drop on the selector is reduced below  $V_{\text{hold}}$  the 1S recovers the OFF state (point 3 Figure 4. 20) and the non-volatile 1R memory cell remains in the HRS.

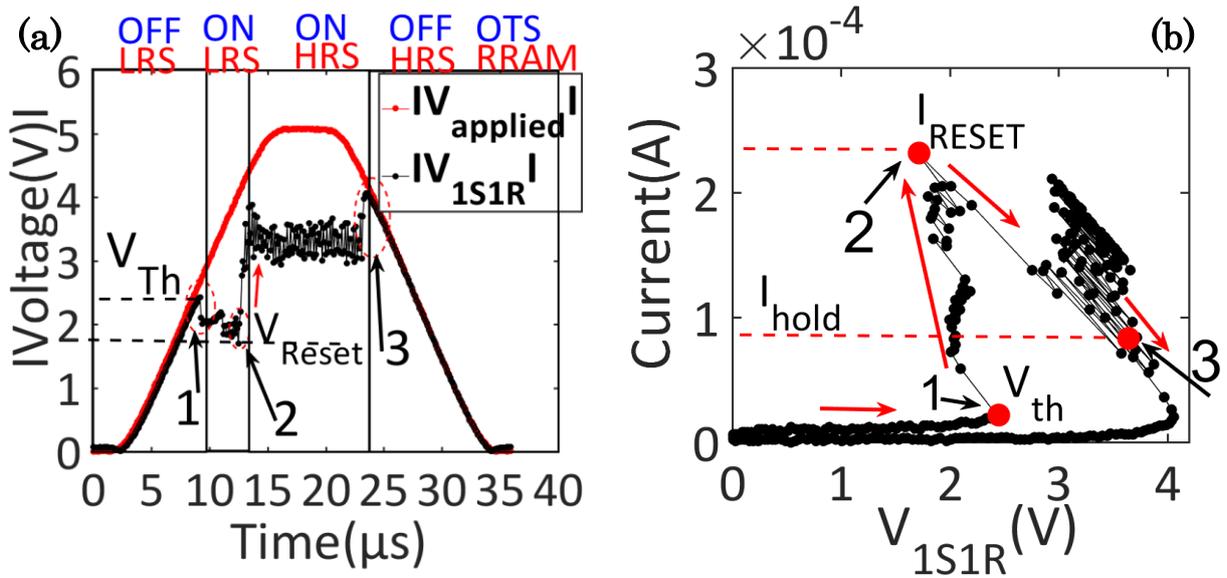


Figure 4. 20 : V-time (a) and I-V (b) curves during Reset (negative applied voltage). When  $V_{1S}$  exceeds  $V_{th}$  the 1S switches to ON state (1), corresponding to a current increase through the 1S1R. The Reset is achieved when the current exceeds  $I_{Reset}$  (2). When the current is reduced below  $I_{hold}$  the 1S recovers the OFF state (3).

#### 4.3.5.3 Set operation

The Set operation of the 1S1R device that follows the Reset, is similar to the forming operation, with lower voltage because the resistance of 1S1R device after Reset is much lower compared to the pristine resistance.

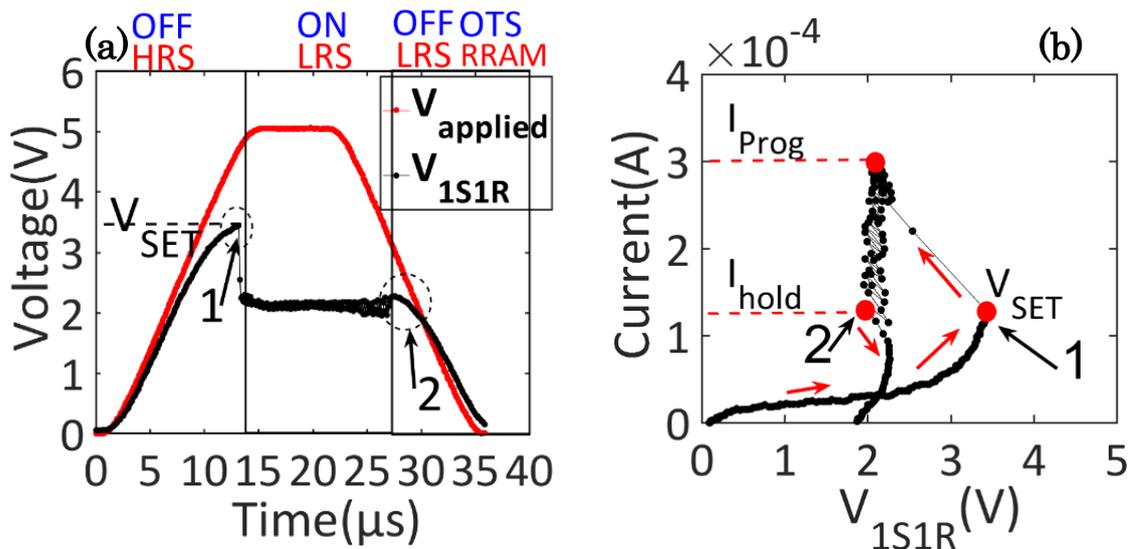


Figure 4. 21 : V-time (a) and I-V (b) curves during Set. When  $V_{1S1R}$  exceeds  $V_{Set}$  the 1S switches from the OFF state to ON state and the 1R switches from the HRS to the LRS. When  $V_{1S}$  is reduced below  $V_{hold}$  the 1S recovers the OFF state (2).

Figure 4. 21 shows the V-time and I-V characteristics of the 1S1R during the Set operation. When the voltage drop on the 1S1R cell exceeds  $V_{Set}$  the 1S switches from the OFF state to ON state and the 1R simultaneously switches from the HRS to the LRS (point 1 Figure 4. 21). The volatile 1S selector recovers the OFF state when its voltage drop reaches  $V_{hold}$  (point 2 Figure 4. 21).

The distributions of the 1S1R switching voltages ( $V_f$ ,  $V_{Set}$  and  $V_{Reset}$ ) obtained during pulsed measurements as described in Figure 4. 19-21 are reported in Figure 4. 22. The 1S1R structure works with programming voltages lower than 5V, this voltage is very close to the RRAM (1R) operation voltages (3V to 4V).

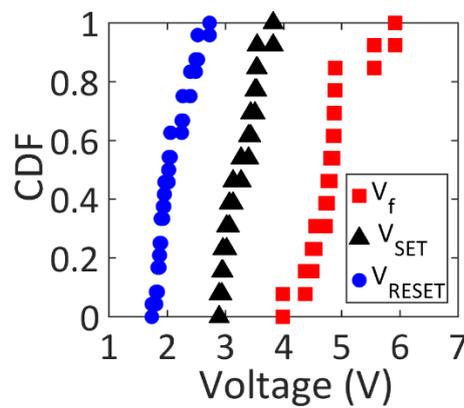


Figure 4. 22 :  $V_f$ ,  $V_{Set}$ , and  $V_{Reset}$  distributions obtained on several cells during pulsed measurements as described in Figure 4. 19-21.

We demonstrated for the first time to our knowledge the functionality of an  $HfO_2$  based RRAM co-integrated with OTS based selector. The main memory operations (Forming, Reset and Set) were put in evidence. In the following sections we will present our innovative strategy adopted to read the resistance states of the 1S1R cells. This strategy will strongly reduce the power consumption by avoiding disruptive reading.

### 4.3.6 1S1R Read strategy

After any 1S1R operation (Forming/Set/Reset), the OTS access device (1S) is in OFF mode and has a resistance higher than the storage element (1R) resistance (i.e.  $\geq 100K\Omega$  for this OTS technology). To determine the 1R state, a positive reading bias

is applied to the 1S1R device ( $V_{read}$ ). Different scenarios are possible during the read operation as shown in Figure 4. 23:

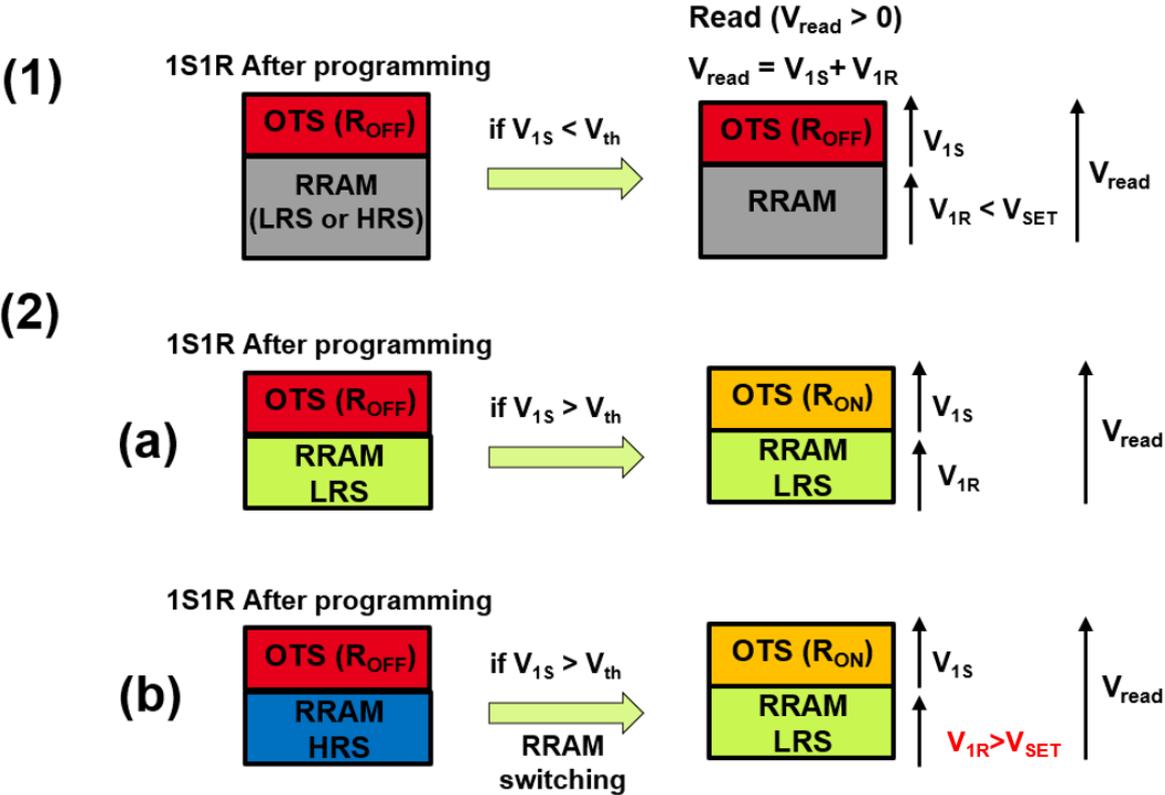


Figure 4. 23 : Different scenarios that can occur during Read operation of 1S1R device

1. The voltage drop across the access device is lower than the threshold voltage ( $V_{1S} < V_{th}$ ). The 1S remains in the OFF state and the reading resistance corresponds to the 1S OFF state resistance.
2. The voltage drop across the selector is higher than the threshold voltage ( $V_{1S} > V_{th}$ ): the access device switches to the ON state. The 1S resistance becomes in the order of few hundreds of Ohms which is negligible compared to 1R resistance in the order of few  $K\Omega$  to tens of  $k\Omega$  depending on the memory element state (LRS or HRS). In this case, the overall positive voltage ( $V_{read}$ ) drops across the memory element (1R) and two possibilities could take place:

- a. **If 1R is in LRS:** read disturb could not occur since the Set operation is performed with a positive pulse and the 1R remains in LRS after the read operation.
- b. **If 1R is in HRS:** when the selector switches to its ON state, the positive read voltage ( $V_{read}$ ) drops on the RRAM leading to the simultaneous non-volatile switch of the 1R cell from HRS to LRS. **The read operation is therefore disruptive and a Reset operation must be performed after every read operation of this type.**

The voltage drop on the 1S selector ( $V_{1S}$ ) depends on the 1R resistance state (LRS or HRS). It is lower if the 1R cell is in the HRS rather than in the LRS state. Consequently, if the 1R cell is in LRS the 1S1R switching occurs at  $V_{th}$ , while if the 1R cell is in the HRS the 1S1R switching occurs at higher voltage ( $V_{Set}$ ).

Figure 4. 24-a shows the V-time curves during the programming operation of the 1S1R device. The red waveform corresponds to the  $35\mu s$  applied programming pulse on both  $R_{ext}$  of  $10K\Omega$  and the 1S1R. Green and black waveforms stand for the voltage drop on the 1S1R device separately when the 1R is in HRS and LRS respectively. If the 1R is in the LRS (black curve) and  $V_{1S1R}$  exceeds  $V_{th}$ , the 1S switches to the ON state. If the 1R is in the HRS and  $V_{1S1R}$  exceeds  $V_{Set}$ , the 1S switches to ON state and the 1R to the LRS simultaneously (green curve). Figure 4. 24-b shows  $V_{th}$  and  $V_{Set}$  distributions obtained on several cells and cycles.

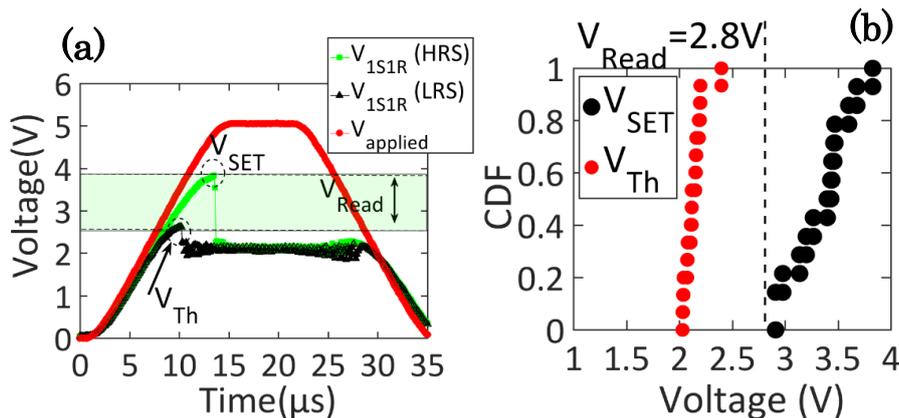
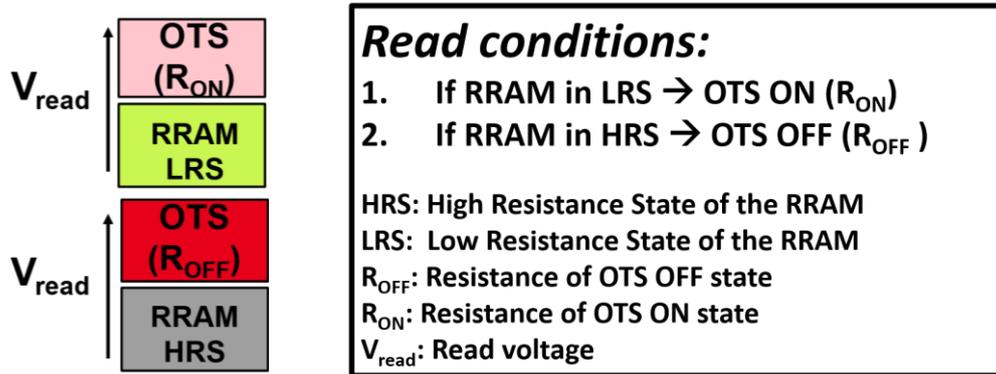


Figure 4. 24 : (a) V-time curves during pulse application. If the 1R is in the LRS (black). If the 1R is in the HRS (green), the 1S switches to ON state and the 1R to the LRS simultaneously. In order to avoid a disruptive reading  $V_{read}$  must be lower than  $V_{Set}$ . (b)  $V_{th}$  and  $V_{Set}$  distributions.

We proposed a read strategy to prevent disruptive reading when the 1R memory cell is in the HRS. This strategy imposes on the read voltage ( $V_{read}$ ) to be **lower** than  $V_{Set}$  (Figure 4. 24) in order to avoid the switching of access device and the memory. Besides to correctly read the LRS, the read voltage must be higher than  $V_{th}$ .

The read conditions (1S ON if the 1R is in the LRS, and 1S OFF if the 1R is in the HRS) are reported in Figure 4. 25.



*Figure 4. 25 : Proposed reading strategy:  $V_{read}$  must switch the 1S selector to the ON state only if the 1R cell is in the LRS, if the 1R is in the HRS the 1S has to remain in the OFF state during read operation.*

$V_{read}$  can be quantified as a function of the storage element states (LRS or HRS) and the resistance value of the 1S based on read conditions defined in Figure 4. 25 as follow:

**1. RRAM in LRS**

$$V_{read} > V_{Th} \left( 1 + \frac{LRS}{R_{OFF}} \right) \quad (4.2)$$

**2. RRAM in HRS**

$$V_{read} < V_{Th} \left( 1 + \frac{HRS}{R_{OFF}} \right) \quad (4.3)$$

According to equations (4.2) and (4.3),  $V_{read}$  depends on  $V_{th}$ ,  $R_{OFF}$ , LRS and HRS. The threshold voltage ( $V_{th}$ ) and the  $R_{OFF}$  of the selector are the intrinsic properties of the access device and could not be modulated for a given OTS material (GeSe in our case). The resistance levels of the storage element (1R) depend on the programming conditions. The  $V_{Reset}$  used during Reset operation defines the HRS level whereas the compliance current imposed during the Set operation defines the LRS level. [11]

Based on the Read conditions obtained in the equations (4.2) and (4.3), we can define a read margin ( $V_{\text{read range}}$ ). By referring to the equations (4.2) and (4.3), for a fixed  $R_{\text{OFF}}$  value,  $LRS/R_{\text{OFF}}$  factor is much smaller than  $HRS/R_{\text{OFF}}$  factor. Consequently, for a fixed  $R_{\text{OFF}}$  the read margin becomes wider for higher HRS values while the LRS value has a small impact on the read margin. We demonstrate that the HRS level of 1R device can be modulated by Reset voltage. As  $V_{\text{STOP}}$  (Reset voltage) increases, HRS and Set voltage ( $V_{\text{Set}}$ ), increase as shown in Figure 4. 26.

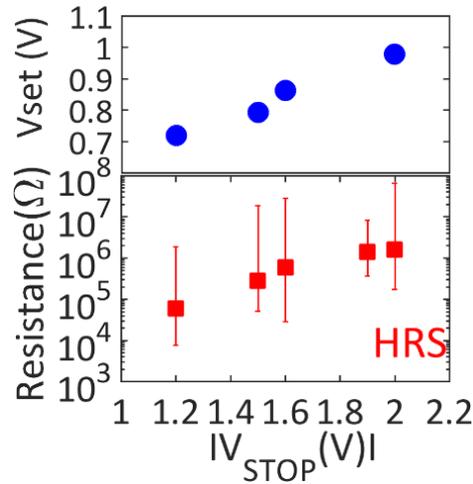


Figure 4. 26 : Measured  $V_{\text{Set}}$  and HRS as a function of the Reset voltage ( $V_{\text{STOP}}$ ) for  $\text{HfO}_2/\text{SiO}_x$  (1R) cells.

The read voltage margin defined according to equations (4.2) and (4.3) as a function of the  $LRS/R_{\text{OFF}}$  and  $HRS/R_{\text{OFF}}$  values is reported in Figure 4. 27 (green region). As conclusion, higher HRS values increase the read margin and make our read strategy more reliable. Based on the results of Figure 4. 24-b, the read voltage for the proposed 1S1R memory cell was fixed at 2.8V for the *read cycling* (presented in the next section). This voltage value is chosen to be:

- Higher than the maximum value reported for  $V_{\text{th}}$  (red distribution in Figure 4. 24-b) in order to ensure the OTS switching for every read operation if the 1R is in LRS.
- Lower than the minimum value reported for  $V_{\text{Set}}$  (black distribution in Figure 4. 24-b) in order to ensure that the OTS remains in OFF state during every read operation if the 1R is in HRS.

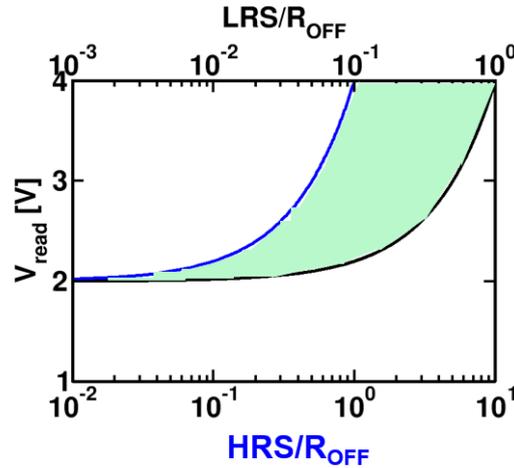


Figure 4. 27 : Read voltage margin (green region) as a function of the  $LRS/R_{OFF}$  and  $HRS/R_{OFF}$  values defined according to equations (4.2) and (4.3). Higher  $HRS$  values strongly increase the read margin.

#### 4.3.6.1 Read cycling

Figure 4. 28 reports an example of V-time curve when a read pulse of 3V is applied on the 1S1R structure. If the 1R memory cell is in the HRS (red curve), the 1S selector remains in the OFF state to prevent the disruptive reading. If the 1R memory cell is in the LRS (black curve), the 1S selector switches to the ON state and the current increases through the 1S1R structure depending on LRS value of the memory element.

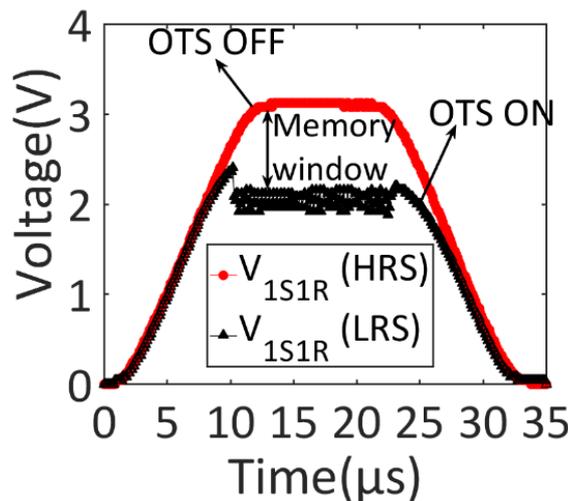


Figure 4. 28 : V-time curves during reading at 3V. If the 1R is in the LRS the 1S switches to the ON state, if the 1R is in the HRS the 1S remains in the OFF state.

To summarize, when the storage element is in LRS, the 1S switches to its ON state during reading. Consequently, the measured 1S1R resistance is the resistance value of the storage element (LRS). When the storage element is in HRS, the 1S remains in its OFF state and the measured 1S1R resistance is the resistance value of the selector element ( $R_{OFF}$ ). Therefore, the memory window of 1S1R device is defined as  $R_{OFF}/LRS$ .

We investigated the stability and the reliability of the proposed reading strategy. Up to  $10^6$  reading cycles have been demonstrated for  $1\mu s$  read pulses as shown in Figure 4. 29. The OTS OFF state measured at low field with reading voltage of 0.2V remains stable ( $\sim 1M\Omega$ ) during reading cycling (blue curve). The OFF-state stability at low field indicates that there are no degradations of the OTS material during read cycling. The memory window of about one decade remains stable as well.

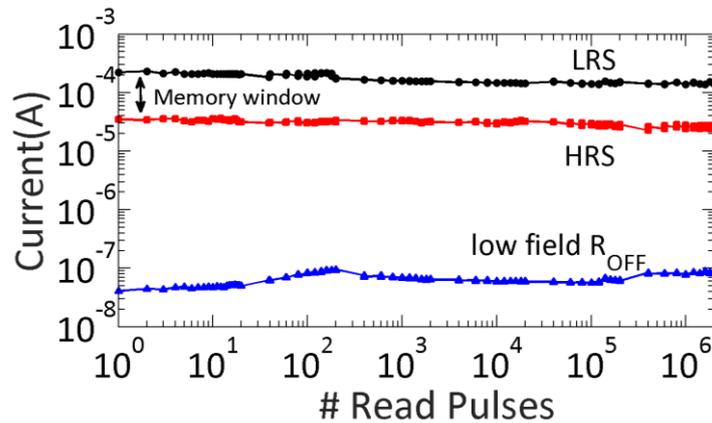


Figure 4. 29 : Reading operation (2.8V,  $1\mu s$ ) without 1S switching when the 1R is in HRS (Red) and with selector switching in LRS (black). Low field  $R_{OFF}$  is the leakage current of selector at low field (read @ 0.2V). The 1S selector ensures  $10^6$  read cycles.

#### 4.3.7 Selectivity for cross-point architecture

The selectivity of access devices is a key parameter that should be explored for crossbar architectures. Selectors with high selectivity are required in order to reduce sneak paths along the array. Unselected cells sharing the same line/column of the selected one undergo a voltage drop of  $V_{read}/2$  if the half bias scheme is taken as an example (Figure 4. 30). Therefore, it is fundamental to increase the read selectivity as much as possible to reduce the sneak-path currents through neighboring cells.

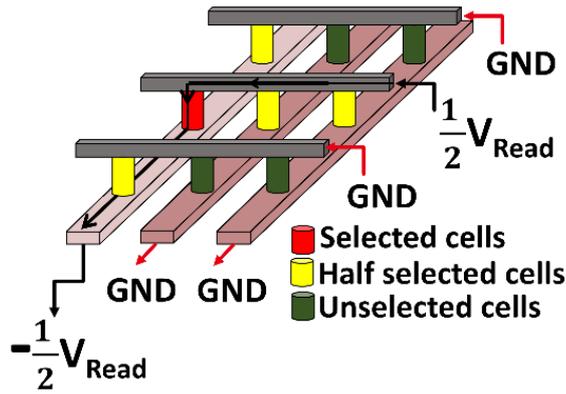


Figure 4. 30 : Schematic of a crossbar array circuit with half bias polarization scheme.

The majority of the reported RRAM devices show perfectly ohmic behavior in their LRS states. The low resistance value (few  $K\Omega$ ) of the LRS state results in a high leakage current that degrades the memory array performances. For the HRS state the leakage current is smaller compared to LRS after partial dissolution of the CF during Reset operation. As result, it is much more important to achieve high LRS selectivity rather than HRS selectivity. We extracted the LRS selectivity of our 1S1R device, considering a half bias scheme. The selectivity (NLF) is defined as  $[(I@V_{Read})/(I@V_{Read}/2)]$  after the Set operation.

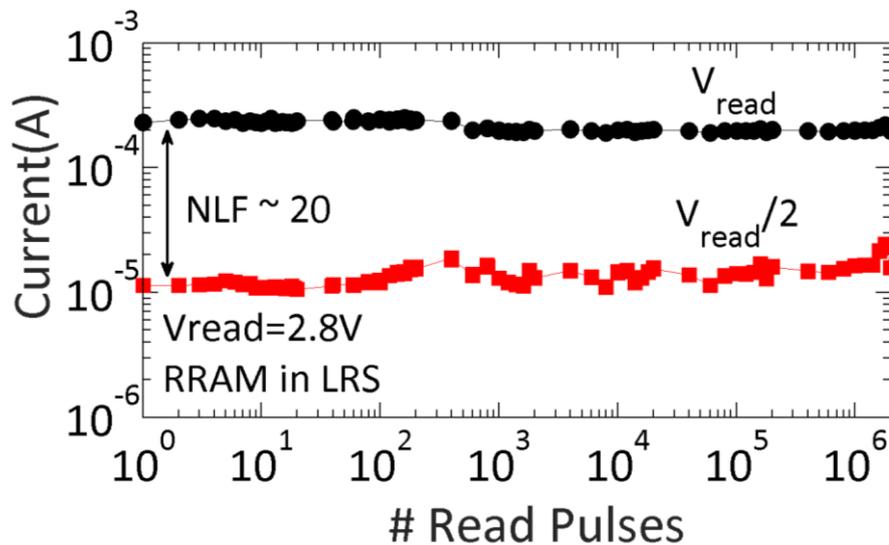
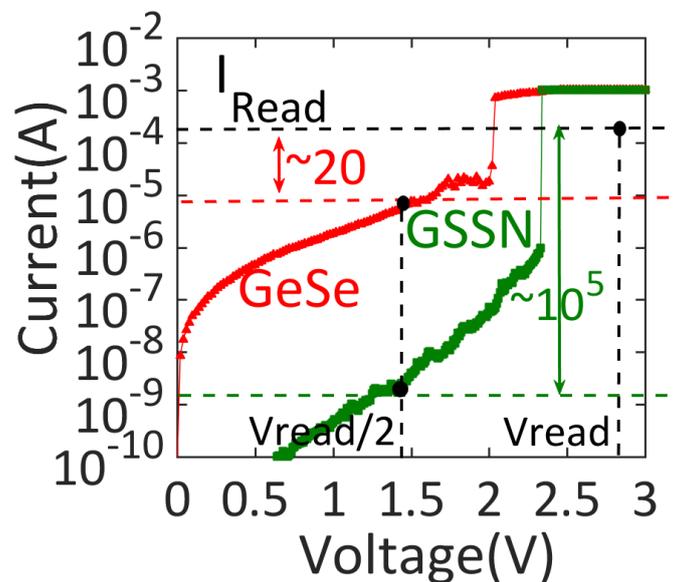


Figure 4. 31 : Reading operation (1R in the LRS) at reading voltages  $V_{read}=2.8V$  and  $V_{read}/2$ .

Figure 4. 31 reports the current through 1S1R structure when the storage element (1R) is in LRS at  $V_{\text{read}}$  and  $V_{\text{read}}/2$ . Based on these results, the measured LRS selectivity is  $\sim 20$  and no degradation after  $10^6$  reading cycles was put in evidence.

After we demonstrated the 1S1R co-integration functionality and its LRS selectivity, we can discuss some methods that have been proposed in the literature to improve the performances (e.g. increase the selectivity) of such as selector devices. Further optimization of the selectivity can be achieved with engineered selectors. In particular Sb and N doping of Se-rich GeSe OTS (GSSN) allows to improve the selectivity. The N doping, thanks to the formation of Ge-N bonds improves the OFF-state selector stability, while the Sb doping allows to control the threshold voltage [7]. Figure 4. 32 shows the effects of Sb and N doping of Se-rich GeSe OTS (GSSN) on electrical characteristics. The red curve corresponds to the Se-rich GeSe OTS that we used as access device in our 1S1R cells. The 1S has a selectivity of  $\sim 20$ , this value is in agreement with the one that we have extracted for the co-integrated 1S1R device (Figure 4. 31). Green curve in Figure 4. 32 stands for doped GeSe (GSSN), the half bias selectivity was improved by up to 4 orders of magnitude compared with non-doped GeSe. Consequently, GSSN is a promising solution for the co-integration with  $\text{HfO}_2$  based RRAM that can provide high selectivity required for cross-point architectures.



*Figure 4. 32: Measured I-V curves for the GeSe based OTS presented in this study and GSSN selector. The GSSN provides much higher selectivity compared to GeSe [7].*

Different OTS technologies are proposed in the literature that show high selectivity ( $>10^3$ ) are summarized in Table 4. 2.

*Table 4. 2: Different OTS technologies reported in the literature with the associated selectivity for each technology*

OTS material	Selectivity
GeSe+Sb+N (GSSN) [7]	$10^5$
SiTe [6]	$10^6$
AsTeGeSiN [9]	$10^3$
Doped chalcogenide [10]	$10^6$

### 4.3.8 Voltage drop across metal lines

Using the model presented in [12], and assuming programming current of  $100\mu\text{A}$ , we estimated the expected performances of a  $4\text{F}^2$  crossbar array. A copper interconnect with metal half pitch of 50 nm, and resistivity of  $7 \times 10^{-8} \Omega \cdot \text{m}$ , are used in the simulations. Figure 4. 33-b reports the voltage drop across the last 1S1R cell of the array (worst case) as a function of column and line length when read voltage of 2.8V is applied on the line. As shown in Figure 4. 33-a, for an HRS value of  $\sim 400\text{k}\Omega$  the maximum  $V_{\text{read}}$  allowing a non-disruptive read is  $\sim 2.8\text{V}$ . The minimum read voltage to ensure correct read when the 1R cell is in the LRS (OTS volatile switch) is 2.4V according to Figure 4. 24-b. Thereby, to increase the array size it is mandatory to: (i) increase the selector selectivity to suppress the parasitic sneak paths and (ii) increase the HRS level of the storage element (1R) to improve the read margin. Crossbar arrays up to 1Mb can be implemented with programming current of  $100\mu\text{A}$ , selectivity of  $\sim 4$  order of magnitude (GSSN selector), and high resistance state (HRS) of the storage element higher than  $400\text{k}\Omega$ .

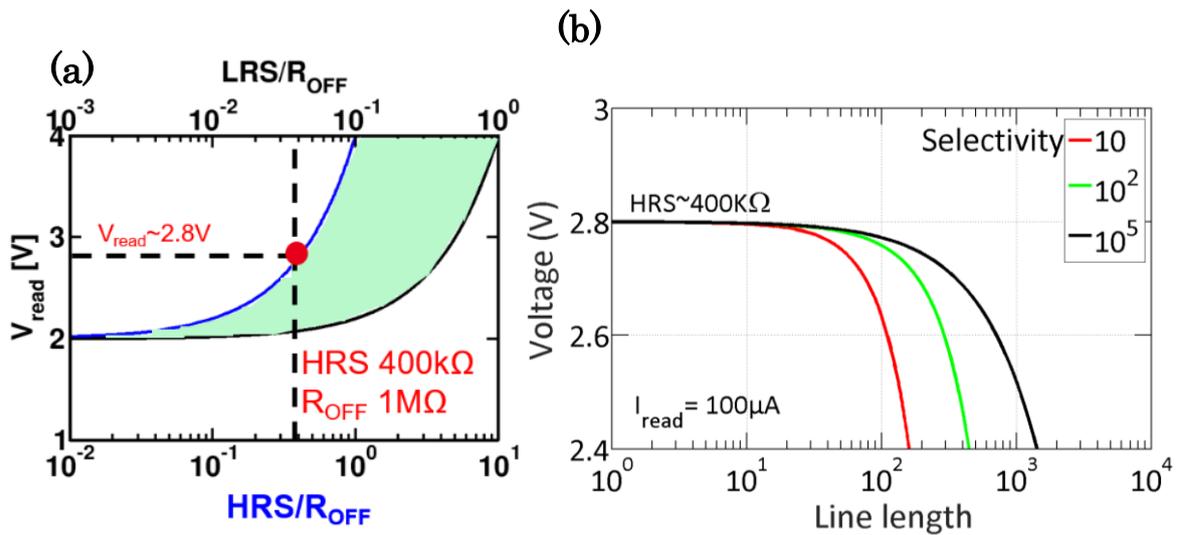


Figure 4. 33: (a) Read voltage margin at HRS 400kΩ. (b) Voltage drop across the last 1S1R cell of a crossbar array (worst case) as a function of the line length assuming that  $I_{read} = 100\mu A$  and HRS of 400kΩ with different selector selectivity (i.e. 10,  $10^2$  and  $10^5$ ).

## 4.4 OTS Vs Tunnel barrier

We presented in this chapter an example of oxide tunnel barrier and an example of OTS access device for HfO<sub>2</sub> based RRAM. The devices with oxide tunnel barrier show lower selectivity and higher operating voltages compared to the 1S1R device with OTS access device. However, a tunnel barrier has some benefits in terms of simple material compositions (simple oxides) compared to OTS selector. A comparison between the main characteristics of both access devices is reported in Table 4. 3.

Table 4. 3: Comparison between the main characteristics of the tunnel barrier and the OTS access devices. References: [6], [7], [9], [10], [13]–[17],[18]

Structure	1S Doped chalcogenid e [10] (OTS)	1S W/SiTe(13nm )W [6] (OTS)	1S GSSN [7](OTS)	1S1R FAST Material not identified [14]	1S1R TiN/GeSe/Ti N (OTS) (This work)	1S1R TiN/barrier/N bO2/barrier/ TiN + TiOx/TaOx (RRAM) Barrier [13]	1S TiN/a-Si (8 & 15 nm)/TiN Barrier [16]	1S Pt/TiO2/TiN Schottky barrier [15]	1S1R Barrier/TMO1/TM O2/Barrier [18]	1S1R Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> /Ti O <sub>x</sub> Barrier (This work)
$J_{ON}$	1.6 MA/cm <sup>2</sup>	10 MA/cm <sup>2</sup>	>1.4 MA/cm <sup>2</sup>	>1MA/cm <sup>2</sup>	>1 MA/cm <sup>2</sup>	-----	>1MA/cm2	~ 10 <sup>3</sup> A/cm <sup>2</sup> (very low)	-----	>1MA/cm2
OFF current or density	10 pA	0.01 KA/cm <sup>2</sup>	1nA	10 <sup>-11</sup> A	40nA	1μA	10nA	-----	0.1μA	0.1μA
Selectivity	10 <sup>7</sup>	10 <sup>5</sup>	>10 <sup>4</sup>	>10 <sup>6</sup>	20 @ 100μA	~30	>240 (8nm a Si) >1500 (15nm a- Si)	~100	~17	~10
Endurance	10 <sup>9</sup> (For 1S only)	10 <sup>8</sup> (For 1S only)	10 <sup>6</sup> (For 1S only)	(1S)10 <sup>11</sup> (1S1R) 10 <sup>5</sup>	10 <sup>6</sup> (Read endurance for 1S1R)	10 <sup>3</sup>	10 <sup>6</sup>	-----	10 <sup>7</sup>	-----
Polarity	NOT shown !!!	Bipolar	Bipolar	Bipolar	Bipolar	Bipolar	Bipolar	Bipolar	Bipolar	Bipolar
Switching voltage	1.5V	~1.5V	~2.2V	~2V	~4.8V	~2V	3.5V (operating voltage)	2V (operating voltage)	~3.5V	~4.5V
Holding voltage	0.2V	-----	-----	~1V	~1.6V	~1.5V	-----	-----	-----	-----

## 4.5 Conclusion

We presented two different access devices that can be co-integrated with HfO<sub>2</sub> based RRAM to obtain LRS selectivity. The latter is required to avoid sneak-paths issues that can degrade the memory array performances.

We studied first the oxide tunnel barrier that consists of HfO<sub>2</sub> layer in addition to the Al<sub>2</sub>O<sub>3</sub> active layer. On the first hand, this method provides low NLF (~10), this value is comparable whit values previously reported in the literature for the same technology. A NLF of 10 is not sufficient to build large memory arrays [1][2]. On the other hand, the multilayer devices that we proposed with an oxide tunnel barrier shows benefits in terms of simple integration and for neuromorphic applications. With this device, we demonstrated multilevel resistances under identical programming pulses (Set/Reset) that can be used to reproduce the synaptic plasticity in neural network. The analog switching was investigated by physics based simulations, it was attributed to the gradual enlargement of the CF in the active layer (Al<sub>2</sub>O<sub>3</sub>) under applied pulses. Whereas the other layer (HfO<sub>2</sub>) was acting as a tunneling barrier.

We proposed then a GeSe based OTS selector. We demonstrated the functionality of the co-integrated OTS access device with HfO<sub>2</sub> based RRAM. The GeSe based selector provides a selectivity of ~20. This selectivity value is relatively low compared to the values reported in the literature. However, material engineering

by Sb and N doping could increase the GeSe selectivity up to  $10^4$ . A selectivity value of 4 order of magnitude makes the Se-rich GeSe (GSSN) based materials suitable for Back-End of Line (BEOL) selector integrations in crossbar arrays up to 1Mb.

## 4.6 References

- [1] A. Chen, "Nonlinearity and Asymmetry for Device Selection in Cross-Bar Memory Arrays," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2857–2864, 2015.
- [2] B. Govoreanu, L. Zhang, and M. Jurczak, "Selectors for high density crosspoint memory arrays: Design considerations, device implementations and some challenges ahead," *Int. Conf. IC Des. Technol. ICICDT 2015*, 2015.
- [3] D. Garbin *et al.*, "HfO<sub>2</sub>-Based OxRAM Devices as Synapses for Convolutional Neural Networks," *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2494–2501, 2015.
- [4] J. Woo *et al.*, "Improved synaptic behavior under identical pulses using AlO<sub>x</sub>/HfO<sub>2</sub> bilayer RRAM array for neuromorphic systems," *IEEE Electron Device Lett.*, vol. 37, no. 8, pp. 994–997, 2016.
- [5] J. Bill and R. Legenstein, "A compound memristive synapse model for statistical learning through STDP in spiking neural networks," *Front. Neurosci.*, vol. 8, pp. 1–18, 2014.
- [6] Y. Koo, K. Baek, and H. Hwang, "Te-based amorphous binary OTS device with excellent selector characteristics for x-point memory applications," *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. 86–87, 2016.
- [7] A. Verdy *et al.*, "Improved electrical performance thanks to Sb and N Doping in Se-rich GeSe-Based OTS selector devices," *2017 IEEE 9th Int. Mem. Work. IMW 2017*.
- [8] G. Navarro *et al.*, "Innovative PCM + OTS Device with High Sub-Threshold Non-Linearity for Non-Switching Reading Operations and Higher Endurance Performance," *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. 94–95, 2017.
- [9] S. Kim *et al.*, "Performance of Threshold Switching in Chalcogenide Glass for 3D Stackable Selector," *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. T240–T241, 2013.
- [10] H. Yang *et al.*, "Novel selector for high density non-volatile memory with ultra-low holding voltage and 10<sup>7</sup> on/off ratio," *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. T130–T131, 2015.
- [11] E. Vianello *et al.*, "Resistive Memories for Ultra-Low-Power embedded computing design," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp.144-147, 2014.
- [12] A. Levisse, B. Giraud, J. P. Noel, M. Moreau, and J. M. Portal, "High density emerging resistive memories: What are the limits?," *2017 IEEE 8th Latin American Symposium on Circuits & Systems (LASCAS)*, 2017.
- [13] W. G. Kim *et al.*, "NbO<sub>2</sub>-based low power and cost effective 1S1R switching for high density cross point ReRAM Application," *Dig. Tech. Pap. - Symp. VLSI Technol.*, 2014.
- [14] S. H. Jo, T. Kumar, S. Narayanan, and H. Nazarian, "Cross-Point Resistive RAM Based on Field-Assisted Superlinear Threshold Selector," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3477–3481, 2015.
- [15] J. Shin *et al.*, "TiO<sub>2</sub>-based metal-insulator-metal selection device for bipolar resistive random access memory cross-point application," *J. Appl. Phys.*, vol. 109, no. 3, 2011.
- [16] L. Zhang *et al.*, "High-drive current (>1MA/cm<sup>2</sup>) and highly nonlinear (>10<sup>3</sup>) TiN/amorphous-Silicon/TiN scalable bidirectional selector with excellent reliability

- and its variability impact on the 1S1R array performance,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp.164-167, 2014.
- [17] M. J. Lee *et al.*, “Highly-scalable threshold switching select device based on chalcogenide glasses for 3D nanoscaled memory arrays,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 33–35, 2012.
- [18] S.-G. Park, M. K. Yang, H. Ju, D.-J. Seong, J. M. Lee, E. Kim, S. Jung, L. Zhang, Y. C. Shin, I.-G. Baek, J. Choi., H.-K. Kang, and C. Chung, “A non-linear ReRAM cell with sub-1 $\mu$ A ultralow operating current for high density vertical resistive memory (VRRAM),” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 501–504, 2012.

# Chapter 5

## Summary and perspectives

### 5.1 Ph.D. summary

The cash/memory/storage hierarchy has become the bottleneck for large systems. Originally motivated by finding a “successor” for NAND flash, the research into new candidates for solid state nonvolatile memories has led to the concept of Storage Class Memory (SCM). The SCM should provide the performances of DRAM (i.e. high speed) in addition to the non-volatility and high density of NAND flash. Various memory technologies are being developed as potential candidates for SCM such as RRAM and PCM.

The goal of our present work is to investigate the reliability of HfO<sub>2</sub> RRAM cells and the access devices for these RRAM devices. In order to do so, we performed: (i) material/device engineering, (ii) electrical characterizations, (iii) physics based simulations and (iv) material characterizations. The major results and contributions of this work are summarized as following:

**Chapter 2:** We presented our HfO<sub>2</sub> based RRAM device fully fabricated at CEA-LETI with some process details. We introduced the characterization environment that we have adopted to carry out our experiments. The latter is represented by the investigation of the basic memory operations (Forming/Reset/Set), the performances as well as the reliability of the explored memory technology. We presented also the “Ginestra” simulation package based on the thermochemical model. Indeed, we have used this model to study the process of defect formation at the microscopic level aiming to deepen understanding the RRAM switching mechanisms. The microscopic properties responsible for defects creation, such as the activation energy to break a bond at zero field and the molecular dipole moment, were extracted experimentally from TDDB data. We reproduced very accurately the experimental I-V

characteristics of forming operation indicating that the charge transport and defects generation mechanisms were properly identified in the model. Finally, thanks to the statistical capabilities of the model, we were able to reproduce the device to device variability during forming process. The variability was explained by the random placement of the defects in the oxide layer at the pristine state of the memory cells.

**Chapter 3:** Using the measurement environment and the simulation model described in chapter 2, the reliability of HfO<sub>2</sub> based RRAM and its forming operation were investigated. We studied the effects of Al doping on data retention and forming voltage of HfO<sub>2</sub> based RRAM cells. We adopted the following methods to introduce the Al in the memory stack: (i) the single layer devices that consists of HfAlO alloy, (ii) the single layer devices with Al incorporation by ionic implant and (iii) the double layer devices with different Al concentrations in the bottom layer. We found that:

- The forming voltage increases linearly with Al concentration whatever the method used to introduce Al in the memory stack.
- Al incorporation acts on the microscopic properties (i.e.  $E_a$ ,  $P_0$  and  $K$ ) of the HfO<sub>2</sub>. The activation energy for bond breakage process ( $\Delta H$ ) under applied electric field increases with Al doping. Therefore, higher forming voltage is required in the presence of Al in the memory stack.
- Double layer devices show higher forming voltage compared to single layer devices even though they have the same effective thickness of the resistive switching layer and the same total Al concentration in the memory stack. The effect of the device geometry (e.g. single layer or double layer device) was investigated by means of physics based simulation. The simulation inputs were  $E_a$ ,  $P_0$  and  $K$  that we have extracted experimentally for each material (HfO<sub>2</sub>, HfAlO(9:1), and Al<sub>2</sub>O<sub>3</sub>). The results show that higher forming voltage for double layer devices is mainly due to electric field redistribution because of the difference in dielectric constant for each material. We conclude there is no significant material intermixing in multilayer devices as well.
- The forming process is activated by temperature where lower forming voltage was measured at higher temperatures. The dependence of forming voltage on temperature is not related to the Al concentration or Al doping method (HfAlO alloy, Al ionic implant or double layers).

- LRS data retention process is highly activated by temperature. The LRS fails faster towards HRS as the temperature increases. Al incorporation improves the data retention of HfO<sub>2</sub> based RRAM with respect to the method used to introduce the Al in the memory stack. Single layer devices with HfAlO alloy and double layer devices with Al in the bottom layer show better data retention compared to single layer with pure HfO<sub>2</sub>. Al incorporation with ionic implant shows no effects on data retention.

We looked at the radiation immunity of HfO<sub>2</sub> based RRAM cells as a key reliability study for space applications. The unbiased devices were exposed to 266 MeV Iodine heavy ions energy. The exposures were performed on unbiased devices and at normal incidence. The exposed devices were in all possible resistance states (Pristine/LRS/HRS) and different sizes. The resistance states and the programming voltages were measured before and after exposure to study the irradiation effects on devices characteristics. We performed a set of simulations to deepen understanding the obtained experimental results.

- The studied RRAM devices were found to resist to this type of exposure (266MeV of Iodine ions energy). No relevant changes were observed on any of the cells characteristics such as resistance levels and programming voltages (Forming/Reset/Set) before and after the exposure.
- TRIM simulations show that the maximum number of oxygen vacancies that can be generated under the Iodine fluence used in our experiment is 40 O vacancies in a single cell.
- Physics based simulations show that without any applied bias during exposure (data retention mode), all the generated defects were recombined due to Coulomb attraction/repulsion mechanism. Consequently, no relevant changes on memory cells can be measured after exposure.
- With an applied bias during exposure, the generated O vacancies would not recombine with interstitials O ions. These ions drift towards the scavenging layer driven by the applied bias. Therefore, the irradiation conditions that we used could have measurable effects on HfO<sub>2</sub> based RRAM if the memory cells are in programming mode during the exposure.

**Chapter 4:** In this chapter, we proposed two types of access devices for the suppression of parasitic sneak current in crossbar architecture: (i) the oxide tunnel barrier and (ii) the OTS based selector. We evaluated the characteristics of the one-selector one-resistor (1S1R) devices for the two selectors.

Our analysis on oxide tunnel barrier selector points out to:

- The multilayer cells with oxide tunnel barrier show different Set process (i.e. Abrupt, gradual and two steps) with respect to the device geometry (e.g. oxide thicknesses) and the polarization scheme (Top polarization or Bottom polarization).
- To maintain the tunnel barrier effect, the full oxide breakdown of all the oxide layers in the memory stack should be avoided. The programming conditions must be adopted to create a CF in one layer of the memory stack and the other layer remains as tunnel barrier.
- It is not possible to achieve a stable LRS for the devices with *abrupt* Set process before the full oxide breakdown. Therefore, after the Set operation the I-V characteristics of LRS state show Ohmic behavior (linear).
- The devices with *gradual* and *two-steps* Set show a self-rectifying behavior. Hence, there is no need for any access devices (e.g. transistor) to limit the current and to avoid the overshoot issue. The current level is controlled by means of the applied voltage. For these devices, it is possible to achieve a stable LRS without a complete CF formation. LRS selectivity of about 10 was extracted for these samples.
- The LRS selectivity depends on the programming current level that modulate the tunnel barrier height. The higher is the programming current the lower is the selectivity.
- The strategy of oxide tunnel barrier that we adopted suffers from very low selectivity ( $\sim 10$ ) and low programming current that leads to poor LRS data retention. Despite the low selectivity, the oxide tunnel barrier is easy to integrate compared to other access devices (e.g. OTS, MIEC, Transistor, etc.).
- The multilayer devices with oxide tunnel barrier, that show *gradual* or *two-steps* Set, have the benefits of multilevel resistance states that can be obtained

under identical set pulses. This behavior is suitable to reproduce the synaptic plasticity in neural networks.

For the GeSe based OTS selector we have demonstrated the following:

- We presented for the first time to our knowledge the co-integration of GeSe based OTS selector with HfO<sub>2</sub> based RRAM in 1S1R structure.
- The 1S1R device was fully characterized using an appropriate measurement setup that we have developed for this purpose. The RRAM main operations (i.e. Forming/ Reset/Set) were put in evidence for the full 1S1R device.
- We proposed an innovative read strategy to prevent disruptive read when the storage element (1R) is in HRS that strongly reduce the power consumption. During read operation, the adopted read voltage ( $V_{\text{read}}$ ) must ensure the following:
  1. The voltage-drop on selector device (1S) must be higher than its  $V_{\text{th}}$  only if the storage element is in LRS state. In this case, the selector device switches to its low resistance level ( $R_{\text{ON}}$ ) and the LRS of the storage element is correctly read.
  2. The voltage-drop on selector device (1S) must be lower than its  $V_{\text{th}}$  only if the storage element is in HRS state. Consequently, the selector remains in its high resistance level ( $R_{\text{OFF}}$ ).
- By adopting this read strategy, the LRS of full 1S1R device is the LRS of storage element. The HRS of full 1S1R device is the high resistance level of selector element ( $R_{\text{OFF}}$ ).
- We demonstrated over  $10^6$  read cycles of both resistance states (LRS and HRS) for the 1S1R device.
- GeSe based OTS selector provides LRS selectivity of  $\sim 20$ . This selectivity value is higher than the one provided by the oxide tunnel barrier that we used first as access device.
- A selectivity of  $\sim 20$  is relatively low compared to the values reported in the literature. However, GeSe selectivity can be strongly improved up to  $10^4$  by means of material engineering such as Sb and N doping.

- With selectivity of  $10^4$ , the doped Se-rich GeSe (GSSN) is suitable for access device integration in cross point arrays up to 1Mb.

## 5.2 Perspectives

It is essential to explore in details the reliability of any microelectronic device before going to product level. For any memory technology the main goal is to produce reliable memory arrays with different densities depending on the application. Throughout this work, we addressed some important reliability and technological challenges that facing RRAM technology in order to be a competitive emerging memory for storage class memory or NAND flash replacement. Concerning the future work related to RRAM reliability, further exploration has to be included:

- We investigated the effects of Al doping in HfO<sub>2</sub> based RRAM on data retention with different methods to introduce the Al in the memory stack. Our study was limited to the macroscopic level through electrical characterization. However, data retention needs more understanding at the microscopic level. Ab-initio calculations can be used to study in depth the species motion responsible for LRS or HRS data retention. Moreover, in this work we were limited to Al doping, therefore, other species can be further investigated as dopant in HfO<sub>2</sub> based RRAM. This might provide better improvement of LRS or HRS retention compared to Al doping.
- We demonstrated that HfO<sub>2</sub> based RRAM can be considered as very hard to SEEs in retention mode (unbiased conditions) when facing Iodine ions. Similar experiment must be performed on biased devices to cover all the possible scenarios in exposure environments. Additional exposure experiments using different projectiles (e.g. gamma, beta, UV, etc.) are mandatory for the use of RRAM in space applications.

For the access devices topic, many aspects worth to be addressed in any future work such as:

- Co-integration of Sb and N doped GeSe material as selector device with HfO<sub>2</sub> based RRAM. This device deserves to be fabricated and tested since GSSN shows much higher selectivity compared to GeSe.

- Using a storage element (1R) that provides larger memory window compared to HfO<sub>2</sub> based RRAM. This should improve the read margin of the read strategy that we have proposed in chapter 4.
- Using our experimental data on 1S1R device as inputs for simulations approach to study the performances of a memory arrays based on this device. Afterwards, the impact of 1S1R parameters on array characteristics can be predicted by simulation. This study could provide engineering guidance for optimal 1S1R device implementation.

# Appendix

## Résumé en Français

### A. Chapitre I : Introduction

Un stockage de données permanent et temporaire est requis dans tout système de traitement de données. Les mémoires à semi-conducteurs constituent une partie essentielle d'un grand nombre de systèmes et d'applications électroniques. Les exigences en termes de stockage de données ont été remplies par les mémoires non volatile (NVM) Flash, et par les mémoires volatiles DRAM et SRAM. D'autre part, le marché actuel du mobile impose de sévères contraintes de performance et de consommation, exigeant ainsi des supports de stockage de données à très faible consommation d'énergie avec une haute densité et à faible coût.

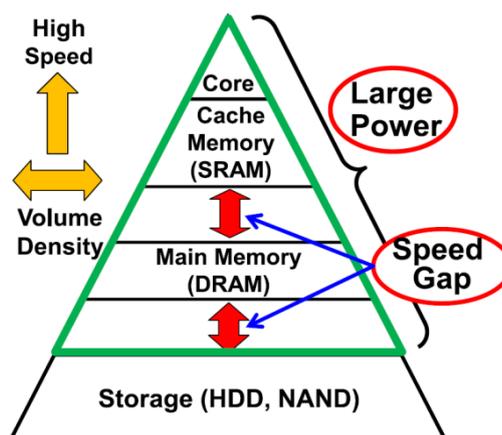


Figure A. 1: Hiérarchie mémoire dans les systèmes informatiques

La hiérarchie mémoire dans les systèmes actuels est une structure pyramidale comme le montre la Figure A. 1. De haut en bas, la mémoire dans le cœur de

traitement est basée sur des périphériques ultra-rapides à faible densité, tels que des registres et des bascules. La mémoire cache et la mémoire principale pour le stockage des instructions à exécuter et des données en cours de traitement sont couvertes respectivement par des dispositifs SRAM et DRAM. Le disque dur (HDD) et le flash NAND sont utilisés comme mémoires de stockage pour les instructions / programmes ainsi que les données. La grande vitesse est requise pour les mémoires situées à proximité des processeurs (SRAM et DRAM), alors qu'une densité élevée est requise lorsque la mémoire est plus éloignée du processeur (HDD et NAND Flash).

Les principaux problèmes rencontrés dans la hiérarchie mémoire d'aujourd'hui peuvent être résumés dans :

- L'écart exponentiel entre le processeur et la mémoire en termes de capacité et de vitesse.
- L'écart de vitesse entre la mémoire cache (SRAM) et la mémoire principale (DRAM).
- Écart de vitesse entre la mémoire principale (DRAM) et la mémoire de stockage (HDD et NAND Flash).
- Consommation élevée du cœur de processeur, du cache et de la mémoire principale car elles sont basées sur des mémoires volatiles.

## 1. Mémoires émergentes

La fin de réduction de la taille du mémoire NAND flash a été annoncée souvent dans le passé. Les centres de recherche et les fabricants des dispositifs mémoires autour du monde travaillent aujourd'hui sur des nouvelles « technologies mémoires émergentes » pour les utiliser comme SCM (*Storage Class Memory*). Plusieurs technologies mémoires sont considérées comme des candidats prometteurs pour le SCM. Parmi les technologies émergentes, on peut lister quatre technologies principales : (i) les mémoires résistives (RRAM), (ii) les mémoires à changement de phase (PCM), (iii) les mémoires magnétique (STT-MRAM) et (iv) les mémoires à base des matériaux Ferroelectric (FeRAM). Toutes sont des mémoires non volatiles qui ne sont pas basées sur le stockage des charges. Le fait que certains de ces mémoires sont déjà en production n'a pas arrêté leur développement.

## 2. Mémoire résistive filamenteuses (RRAM)

Les mémoires résistives RRAM sont basées sur le changement de résistance de la structure *Metal-Insulator-Metal* (MIM) qui constitue le point mémoire. Les modifications structurelles, principalement la formation et la destruction d'un filament conducteur dans le matériau isolant sont à la base du changement de la résistance. Deux états résistifs peuvent être distingués : (i) l'état faible résistivité (LRS) et (ii) l'état haute résistivité (HRS), correspondant aux états logiques "1" ou "0". Les matériaux utilisés dans les mémoires RRAM sont compatibles avec le procédé de fabrication CMOS et pourraient être facilement intégrés en BEOL avec les nœuds technologiques avancés. Le type des défauts impliqués dans la création du filament conducteur (CF) détermine si le RRAM est une OxRAM à base de lacunes d'oxygène ou une CBRAM à base d'Ag ou de Cu provenant d'une électrode active. Les dispositifs RRAM peuvent également être catégorisés selon la polarité de commutation soit "unipolaire" ou "bipolaire" (comme le montre la Figure A. 2).

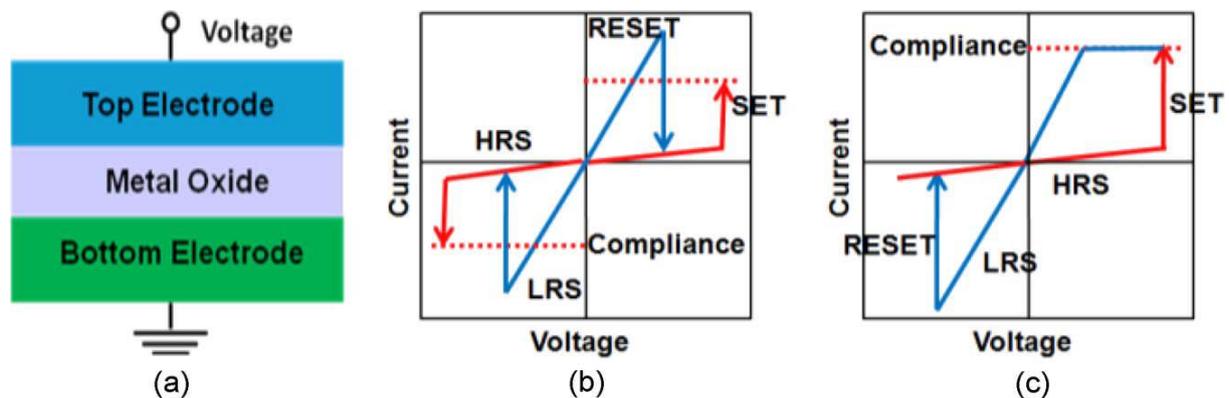


Figure A. 2 : (a) Schéma de la structure MIM d'une mémoire RRAM, (b) Schéma des caractéristiques I-V d'une RRAM unipolaire, (c) Schéma des caractéristiques I-V d'une RRAM bipolaire.

## 3. Objectifs de la thèse

Dans cette thèse, nous étudierons d'abord la fiabilité de la RRAM à base d'HfO<sub>2</sub>. On va travailler sur l'amélioration de la rétention des données de cette technologie mémoire pour la rendre compatible avec les environnements haute température tels que les applications automobiles. Pour cela nous proposons différentes stratégies

d'ingénierie des matériaux qui constituent le point mémoire. En outre, nous étudions les effets de l'exposition d'une RRAM à base de  $\text{HfO}_2$  aux ions lourds pour les applications spatiales, où les dispositifs électroniques devraient montrer des niveaux élevés d'immunité aux rayonnements.

L'architecture *cross-point* conduira la commercialisation des dispositifs RRAM pour cibler les applications SCM. Par contre, cette architecture souffre de courant de fuite qui provoque des dégradations de lecture et de programmation, il augmente également la consommation d'énergie totale dans la matrice mémoire. L'utilisation d'un sélecteur ayant des caractéristiques I-V non linéaires en série avec le point mémoire dans une structure un-sélecteur un-mémoire (1S1R) est proposée pour supprimer les courants de fuite dans les architectures cross-point.

Après l'étude de fiabilité au niveau unicellulaire, nous étudierons la compatibilité de RRAM à base de  $\text{HfO}_2$  avec les architectures cross-point à haute densité. Dans ce but, on va étudier deux types de sélecteur : (i) nous introduisons d'abord une barrière tunnel supplémentaire dans l'empilement mémoire, aboutissant à une cellule SRC (Self-Rectifying-Cell), (ii) nous intégrons un sélecteur à base d'OTS avec le point mémoire RRAM dans un dispositif 1S1R. Nous explorerons les caractéristiques et les performances des deux dispositifs d'accès qu'on a proposé.

## B. Chapitre II : Caractérisation et modélisation de cellules RRAM à base d'HfO<sub>2</sub>

Dans ce chapitre, nous présentons les étapes de fabrication des cellules RRAM à base de HfO<sub>2</sub> fabriquées au CEA-Leti. Des structures de test à cellule unique (1R) et à un transistor-une résistance (1T1R) ont été fabriquées et caractérisées pour étudier la fiabilité et les opérations de base (Forming, Reset et Set) de cette technologie mémoire.

Afin d'étudier le processus de Forming au niveau microscopique, nous avons effectué des simulations physiques en utilisant le logiciel de simulation Ginestra. Le modèle prend en compte le transport des charges/ions ainsi que les modifications structurelles pendant l'opération de Forming (c.-à-d. Création/ rupture CF dans la couche d'oxyde) associées aux opérations d'une RRAM.

### 1. La structure mémoire

Les cellules RRAM sont composées d'un oxyde pris en sandwich entre deux électrodes métalliques dans une structure métal-isolant-métal (MIM). Ils sont généralement intégrés dans le Back-End-OF-Line (BEOL) d'un procédé de fabrication CMOS. La Figure B. 1 montre les structures 1R (a) et 1T1R (b) fabriquées et testées au CEA-Leti. Dans le cas de la structure 1T1R, l'électrode inférieure (BE) de la cellule est connectée au drain du transistor NMOS. La partie active de la cellule mémoire est définie par le point de croisement entre les deux lignes métalliques (M1 et M2) comme indiqué dans la Figure B. 1-c.

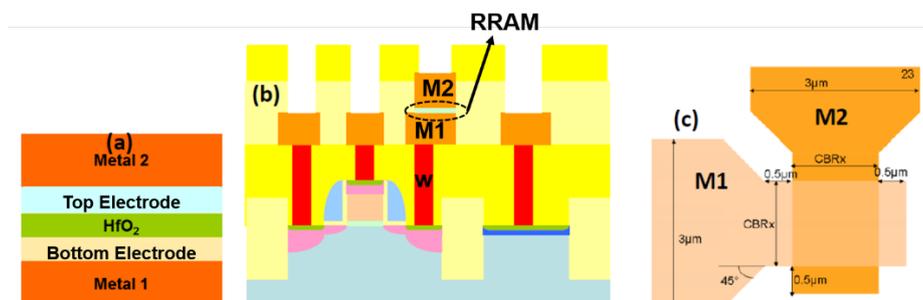


Figure B. 1 : Schéma de (a) la structure MIM 1R intégré entre Métal 1 (M1) et Métal 2 (M2), (b) la structure 1T1R, (c) intégration de la cellule mémoire entre les deux lignes métalliques.

## 2. Programmation d'une cellule mémoire

Les opérations de programmation (Forming / Reset / Set) ont été effectuées à l'aide de l'analyseur de paramètres semi-conducteurs HP4156. Une rampe de tension d'environ 1V/s est appliquée aux bornes des cellules mémoire en structure 1R ou 1T1R pendant la programmation. L'analyseur de paramètres permet d'appliquer la rampe de tension ainsi que de mesurer le courant qui passe dans la cellule, comme indiqué sur la Figure B. 2-a. Cette méthode simple permet de vérifier la fonctionnalité de la cellule mémoire et d'extraire les paramètres de programmation des caractéristiques tension-courant (par exemple les tensions de commutation, les niveaux de courant avant et après la commutation, etc.).

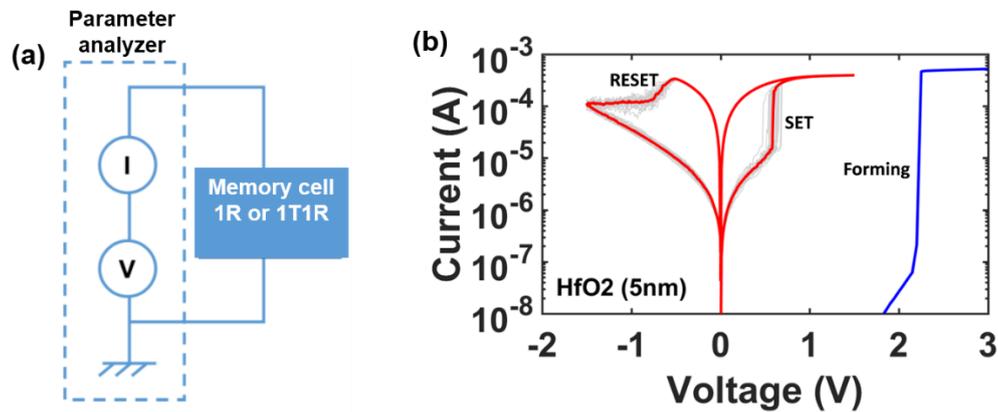


Figure B. 2 : (a) Schéma de mesure en mode quasi-statique. (b) Caractéristiques tension-courant des opérations de Forming, SET et Reset de l'empilement mémoire TiN/HfO<sub>2</sub>/Ti/TiN.

## 3. Modélisation et simulation

Le processus de Forming est dominé par le taux de génération (G) de paires lacunes/ions d'oxygène. Ce taux de génération est modélisé dans le cadre du modèle thermo-chimique comme suit :

$$G = G_0 \exp\left(-\frac{E_a - b * F}{K_B T}\right) \quad (1.2)$$

Où  $E_a$  est l'énergie d'activation pour rompre une liaison Hf-O à un champ électrique nul,  $K_B$  est la constante de Boltzmann,  $G_0$  est la fréquence de vibration des liaisons Hf-O  $\sim 7 * 10^{13}$  Hz et  $b$  est le facteur de polarisation des liaisons.

Le facteur de polarisation des liaisons  $b$  est donné par :

$$b = P_0 \left( \frac{2 + K}{3} \right) \quad (2.2)$$

Où  $P_0$  est le moment dipolaire moléculaire principalement provoqué par des composants moléculaires polaires et opposé au champ électrique local. Les propriétés des liaisons atomiques ( $E_a$  et  $b$ ) impliquées dans le mécanisme de génération des paires lacunes/ions d'oxygène peuvent être extraites à partir des données TDDB mesurées à différentes températures.

Les paramètres extraits pour le matériau HfO<sub>2</sub> sont indiqués dans le Table B. 1. La constante diélectrique  $K$  est dérivée des mesures C-V.

*Table B. 1: Les paramètres extraits des mesures TDDB et CV pour le matériau HfO<sub>2</sub> de 5 nm d'épaisseur*

Parameter	HfO <sub>2</sub>
$E_a$ (eV)	2.1
$P_0$ (e-Å)	4.3
$K$	22

## 4. Simulation du processus de Forming

En utilisant les paramètres extraits ci-dessus avec d'autres qui sont calculés par DFT dans la littérature nous avons pu reproduire avec précision les caractéristiques expérimentales I-V de l'opération de Forming pour HfO<sub>2</sub> 5 nm, comme le montre la Figure B. 3. Cela indique que les mécanismes de transport de charge et de génération de défauts ont été correctement identifiés dans le modèle pendant le processus de Forming.

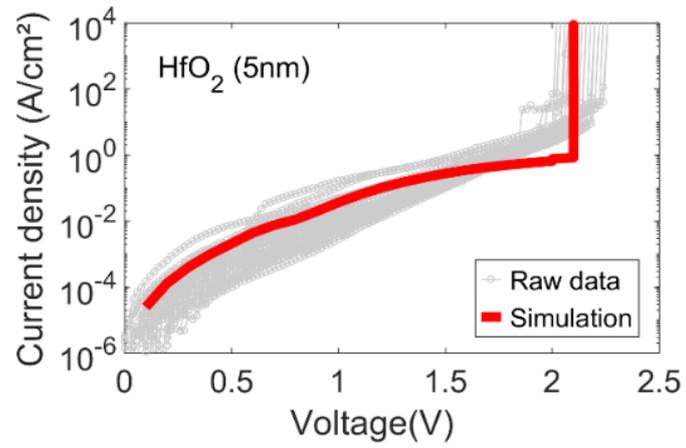


Figure B. 3: *Données expérimentales (en gris) et simulation (en rouge) de la densité de courant en fonction de la tension appliquée pendant l'opération de Forming du 5nm HfO<sub>2</sub>.*

## C. Chapitre 3 : Fiabilité des cellules RRAM à base d'HfO<sub>2</sub>

Dans ce chapitre, nous avons d'abord étudié la stabilité thermique et le processus de Forming des dispositifs RRAM à base de HfO<sub>2</sub> avec du dopage aluminium (Al). Trois méthodes différentes pour introduire l'Al dans l'empilement mémoire ont été étudiées : l'alliage HfO<sub>2</sub> avec Al<sub>2</sub>O<sub>3</sub> comme HfAlO dans un dispositif à une seule couche active, les dispositifs à double couche avec différentes concentrations d'Al dans la couche inférieure et les dispositifs à une seule couche active avec dopage Al par implantation ionique. L'incorporation avec Al est suggérée pour améliorer la rétention des données du dispositif sans augmenter considérablement la tension de Forming.

De plus, la technologie RRAM semble prometteuse pour les applications spatiales, les radars et autres environnements sévères en termes de rayonnements, car elle ne repose pas sur le stockage de charge comme les mémoires Flash. Par conséquent, les études de fiabilité d'une telle technologie mémoire dans les environnements de rayonnement sont très importantes pour explorer leurs comportements dans de telles conditions. À cet égard, nous avons présenté dans la deuxième partie de ce chapitre, l'immunité au rayonnement des cellules RRAM à base d'HfO<sub>2</sub> intégrées dans une structure 1R. L'impact de l'exposition aux ions lourds a été évalué sur des cellules RRAM de différentes tailles et dans différents états de résistance (y compris des cellules vierges). Les cellules ont été irradiées avec des ions à transfert d'énergie linéaire (LET) et soumises à une caractérisation post-exposition. Les états de résistance et les tensions de programmation ont été comparés avant et après irradiation pour savoir si l'exposition peut endommager les propriétés d'une RRAM. Finalement une compréhension microscopique des résultats expérimentaux obtenus après irradiation est présentée à l'aide de simulations physiques.

Nous avons fabriqué des dispositifs RRAM constitués d'une seule ou d'une double couche de matériau actif. Dans le cas de dispositifs à une seule couche, le dopage avec aluminium a été réalisé soit par implantation ionique dans une couche de 10nm HfO<sub>2</sub> déposée par ALD soit par alliage 5nm HfAlO déposé aussi par ALD en échangeant des cycles HfO<sub>2</sub> et Al<sub>2</sub>O<sub>3</sub>. Les dispositifs bicouches sont composés d'une couche supérieure de 3 nm HfO<sub>2</sub> et d'une couche inférieure de 2 nm. Cette couche inférieure est constituée soit de l'alliage HfAlO avec différentes concentrations d'Al

ou du  $\text{Al}_2\text{O}_3$  pure. La Figure C. 1 illustre les dispositifs RRAM fabriqués avec les trois méthodes de dopage Al considérées dans cette étude : D1 et D10 sont respectivement les échantillons de référence  $\text{HfO}_2$  et  $\text{Al}_2\text{O}_3$  avec une épaisseur de 5 nm, D2 est le monocouche avec l'alliage 5 nm  $\text{HfAlO}(9:1)$  (9:1 représente 9 cycles de  $\text{HfO}_2$  suivi de 1 cycle de  $\text{Al}_2\text{O}_3$ ), et D4, D5 et D6 sont les dispositifs bicouches de 5 nm d'épaisseur de  $\text{HfO}_2/\text{HfAlO}(9:1)$ ,  $\text{HfO}_2/\text{HfAlO}(4:1)$ , et  $\text{HfO}_2/\text{Al}_2\text{O}_3$ , respectivement. D3 est l'échantillon de référence de 10 nm  $\text{HfO}_2$  pure et D7, D8 et D9 sont les cellules dopées par une implantation ionique avec différentes concentrations d'Al, 0,1%, 1% et 5% respectivement. Tous les matériaux utilisés comme couches actives dans l'empilement mémoire ( $\text{HfO}_2$ ,  $\text{HfAlO}$  et  $\text{Al}_2\text{O}_3$ ) ont été déposés par ALD à 300 ° C. Les couches d'oxydes prises en sandwich entre l'électrode inférieure en TiN (35 nm) déposée en PVD et l'électrode supérieure en Ti (10 nm) forment des structures MIM. Les cellules RRAM sont co-intégrées avec un transistor d'accès NMOS (structure de test 1T1R) dans un procédé de fabrication CMOS 65 nm standard. L'élément 1R est intégré dans le BEOL entre M4 et M5. La cellule 1R a un diamètre de 1 $\mu\text{m}$ .

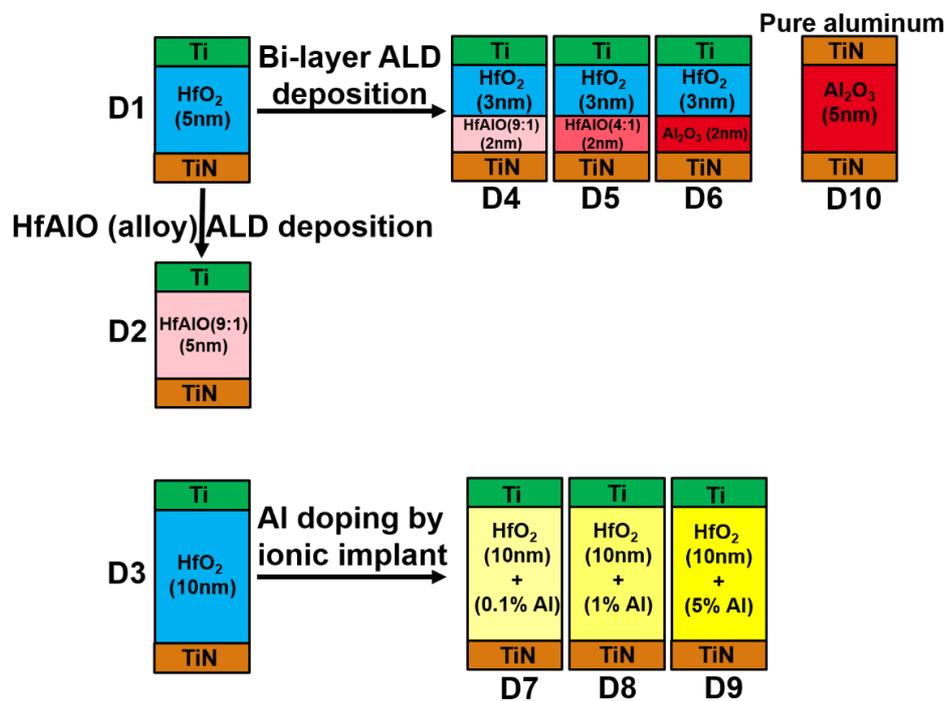


Figure C. 1: Illustrations schématiques des dispositifs étudiés. Trois méthodes différentes pour introduire l'Al dans l'empilement RRAM à base de  $\text{HfO}_2$ .

## 1. Tension de Forming

La Figure C. 2-a montre la tension de Forming ( $V_f$ ) mesurée pour les dispositifs monocouches en fonction du pourcentage d'Al : la courbe rouge montre la  $V_f$  mesurée sur les dispositifs avec 5 nm d'épaisseur de  $\text{HfO}_2$  (concentration d'Al zéro) et de  $\text{HfAlO}$  (9:1) (Al% = 4,3). La courbe noire montre la tension de Forming mesurée sur les dispositifs avec 10 nm d'épaisseur de la couche active, où le dopage Al était fait par implantation ionique. Pour une concentration d'Al donnée, les couches actives les plus épaisses conduisent à une tension de Forming plus élevée. La Figure C. 2-b montre la  $V_f$  mesurée sur des dispositifs à double couche en fonction du pourcentage d'Al dans la couche inférieure. Dans les deux cas (monocouche et bicouche),  $V_f$  augmente linéairement avec la concentration d'Al dans l'empilement mémoire. La tension de Forming dans les dispositifs à double couche est plus élevée par rapport à  $V_f$  dans les dispositifs monocouche avec la même épaisseur physique de la couche active et la même concentration totale d'Al dans l'empilement mémoire (D2 comparé à D5).

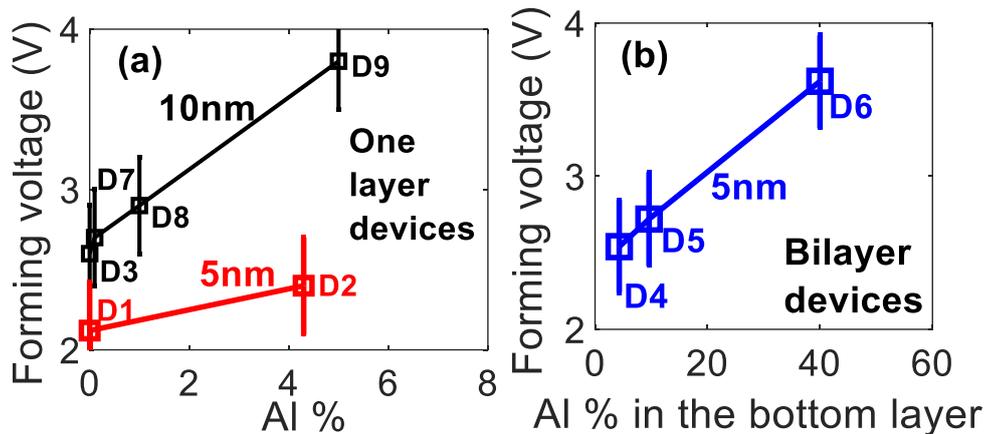
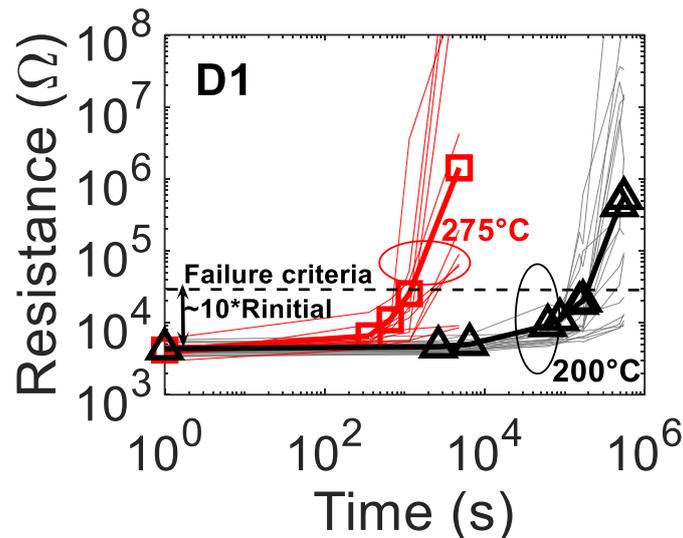


Figure C. 2 : La tension de Forming en fonction de la concentration d'Al pour (a) les dispositifs avec une seule couche active et (b) les dispositifs avec deux couches actives

## 2. Rétention de données

Dans notre investigation, la rétention de données de l'état faible résistivité (LRS) a été étudiée expérimentalement pour  $\text{HfO}_2$ ,  $\text{HfAlO}$ (9:1), les bicouches, et la monocouche  $\text{HfO}_2$  avec dopage Al par implantation ionique. Les échantillons ont été

placés après la programmation (Set) dans le four à une température donnée et leurs états de résistance ont été surveillés au court du temps. La Figure C. 3 montre l'évolution de l'état LRS avec le temps avec deux températures différentes (200 °C et 275 °C) pour la cellule monocouche de référence HfO<sub>2</sub> (D1). Lorsque la température augmente, l'état LRS échoue plus rapidement vers l'état haute résistivité (HRS) indiquant que le processus de rétention des données LRS est fortement activé par la température.



*Figure C. 3 : Evolution de l'état LRS au cours du temps à 200 °C et 275 °C pour les cellules D1. La courbe noire et la courbe rouge avec les marqueurs montrent la tendance moyenne des dispositifs à 200 °C et 275 °C respectivement.*

La Figure C. 4 montre que la température nécessaire pour l'échec de l'état LRS vers l'état HRS après dix ans augmente linéairement avec la concentration d'Al pour les dispositifs monocouche avec l'alliage HfAlO (D2) ainsi que pour les dispositifs à deux couches. Une concentration d'Al plus élevée est nécessaire dans les dispositifs à deux couches pour améliorer la rétention des données par rapport aux cellules avec la monocouche. Les cellules D2, correspondant à un dispositif monocouche avec 4,3% d'Al, présentent la même rétention de données d'une bicouche avec 16% d'Al (D6). L'échantillon non dopé avec 10 nm HfO<sub>2</sub> (D3) présente une légère amélioration de la rétention de données par rapport au 5 nm HfO<sub>2</sub>. Cependant, le dopage Al par implantation ionique n'a pas d'impact sur la stabilité thermique, et les échantillons D3, D8 et D9 présentent une température d'échec de l'état LRS vers l'état HRS très similaire à 10 ans.

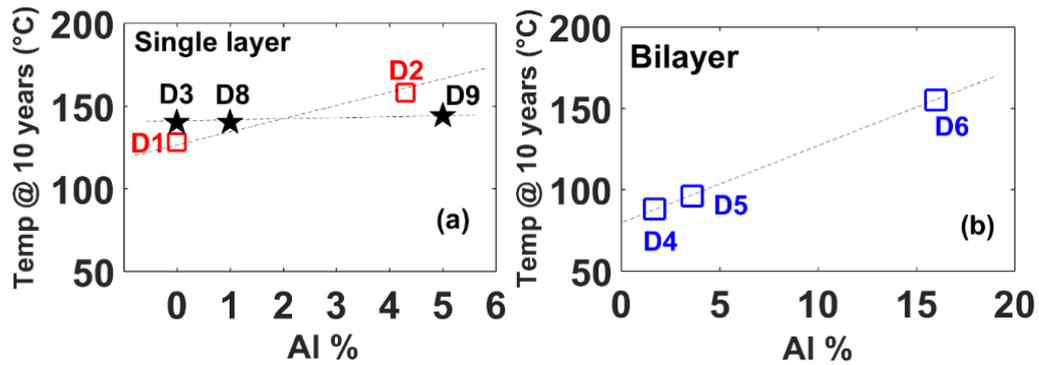


Figure C. 4 : Température d'échec de l'état LRS vers l'état HRS après 10 ans (extraite selon la loi d'Arrhenius) pour (a) les dispositifs monocouches et (b) les dispositifs bicouches en fonction de la concentration d'Al dans le dispositif mémoire.

### 3. Immunité aux radiations

Des mémoires résistives à base de 5nm HfO<sub>2</sub> en structure 1R ont été adoptées pour cette étude. Nous avons utilisé le LET des ions le plus élevé disponible, c'est-à-dire l'iode à 266,7 MeV (LET = 59 MeV/mg/cm<sup>2</sup> dans Si). Les bornes des dispositifs étaient flottant pendant l'exposition. Les résistances des cellules RRAM dans les trois états possibles (Pristine, LRS et HRS) ont été mesurées avant l'exposition. Après irradiation, les résistances des cellules mémoire ont été à nouveau mesurées. Pour les cellules qui étaient à l'état Pristine avant l'irradiation, un processus de Forming a été effectué pour étudier l'effet de l'irradiation sur la tension de Forming. Enfin, les cellules qui étaient dans les états LRS et HRS ont été re-cyclées afin d'étudier l'impact de l'exposition sur les tensions de Set et de Reset. Dans l'ensemble, plus de 100 cellules ont été étudiées pour chaque état résistif.

Après l'exposition, tous les états résistifs ont été à nouveau mesurés pour déterminer les effets de l'exposition aux ions lourds. La Figure C. 5 montre les distributions des résistances avant et après l'exposition, pour des cellules dans différents états résistifs : Pristine, LRS et HRS. Indépendamment des états de résistance des cellules, aucun effet n'a été observé sur aucun des dispositifs après l'exposition aux ions lourds. Toutes les cellules ont été trouvées dans le même état qu'avant l'irradiation, c'est-à-dire qu'aucun changement de bits n'a eu lieu comme le montre la Figure C. 5. Ces résultats signifient que même des dizaines ou plus des ions d'iode à fort LET sur le même dispositif RRAM ne sont pas capables de produire un décalage de résistance mesurable.

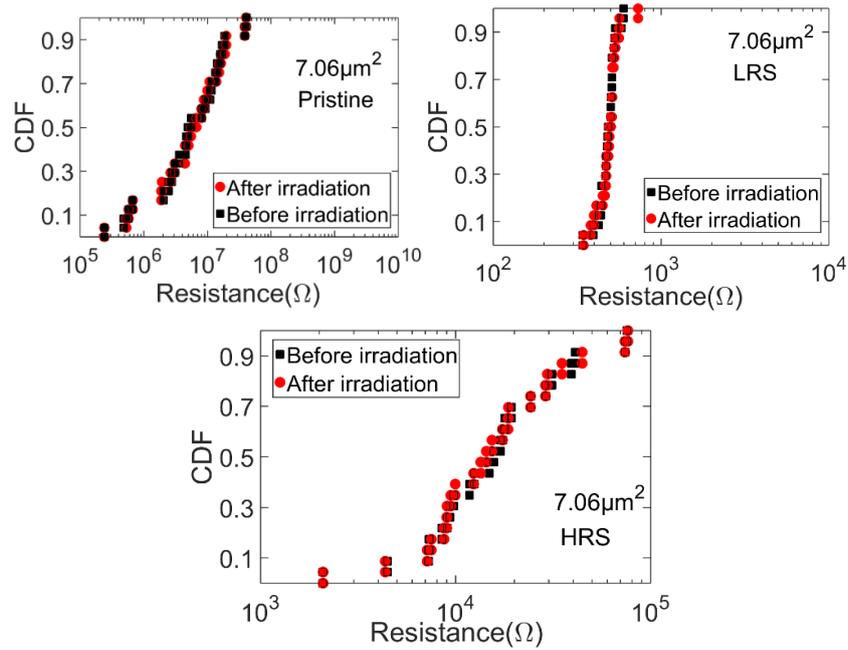


Figure C. 5 : Distributions des résistances mesurées avant et après exposition sur des cellules avec différents états résistifs (Pristine, HRS et LRS).

Concernant les tensions de programmation, aucun changement n'a été observé sur les tension de Forming, Set et Reset après l'exposition. Nous avons discuté des possibles mécanismes qui pourraient conduire à la dégradation des cellules après l'exposition aux ions lourds. En effectuant des simulations physiques, nous avons reproduit les résultats expérimentaux en mode rétention (sans aucun champ électrique) et conclu que la cellule pourrait être sensible si elle est exposée dans des conditions avec un champ électrique appliqué (lecture ou programmation), une nouvelle découverte qui devra être confirmée expérimentalement à la future. Ceci est dû au fait que l'endommagement par rayonnement, c'est-à-dire le nombre de défauts générés par les ions incidents et survivant à la recombinaison immédiate après l'irradiation, dépend du champ électrique appliqué pendant l'exposition et qui va s'opposer à l'attraction de Coulomb entre les ions et les lacunes d'oxygène générés.

## D. Chapitre 4 : Dispositifs d'accès (sélecteur) pour des RRAM à base d'HfO<sub>2</sub>

Dans ce chapitre, nous proposons d'abord des dispositifs RRAM multicouches à base d'HfO<sub>2</sub> avec des barrières tunnel qui montrent un comportement d'autolimitation du courant et une sélectivité intrinsèque. Ensuite, nous présentons notre structure 1S1R en utilisant un sélecteur OTS avec des cellules RRAM basées sur HfO<sub>2</sub>. Pour les dispositifs multicouches avec des barrières de tunnel, nous avons démontré une faible sélectivité à l'état LRS avec un faible courant de programmation  $\sim 10$ Ma. En plus ces dispositifs montrent plusieurs niveaux des résistances, ces caractéristiques sont convenables pour des applications neuro-morphiques. Pour le dispositif 1S1R avec un sélecteur d'accès à base d'OTS, nous avons présenté pour la première fois une étude détaillée des principales opérations de la mémoire 1S1R, (c'est-à-dire le Forming, le Reset, le Set et la lecture). De plus, nous avons démontré une meilleure sélectivité à l'état LRS par rapport aux dispositifs multicouches avec la barrière tunnel. Le matériau OTS qu'on a utilisé peut-être optimiser pour améliorer la sélectivité du dispositif 1S1R jusqu'à  $10^4$ .

### 1. Dispositifs RRAM avec barrière tunnel

Les cellules RRAM étudiées sont composées de trois oxydes (HfO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub> et TiO<sub>x</sub>) d'épaisseurs différentes et pris en sandwich entre les électrodes supérieures et inférieures TiN. Une des couches d'oxyde est supposée jouer le rôle de la couche active dans l'empilement mémoire où se déroule la construction et la rupture de la CF. Les autres couches sont considérées comme des barrières tunnel pour ajouter la sélectivité à l'état LRS des cellules mémoire. Les opérations de programmation (Forming et Set) doivent être contrôlées afin d'empêcher le processus de **Set complet** et la création d'un CF métallique dans tout l'empilement mémoire, préservant ainsi les barrières de tunnel. La Figure D. 1 montre le schéma de (i) S1 qui se compose de deux couches avec 5nm-HfO<sub>2</sub> et 2,5-TiO<sub>x</sub>, (ii) S2 le dispositif à trois couches avec 3nm-Al<sub>2</sub>O<sub>3</sub>, 3nm-HfO<sub>2</sub> et 2,5-nm TiO<sub>x</sub> et (iii) S3 le dispositif à trois couches avec 5nm-Al<sub>2</sub>O<sub>3</sub>, 3nm-HfO<sub>2</sub> et TiO<sub>x</sub> à 2,5 nm.

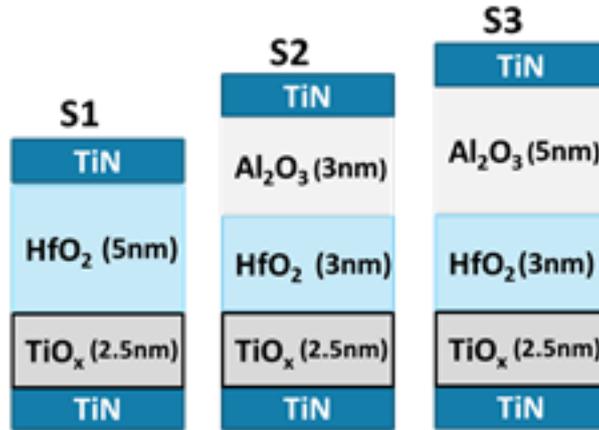


Figure D. 1 : Illustration schématique des dispositifs RRAM explorés à deux et trois couches.

## 2. Différents processus de Set

L'application d'une rampe de tension a été adoptée pour programmer les cellules. Pendant l'opération de Set, la tension de programmation est appliquée sur l'électrode supérieure (TOP) ou inférieure (BOT) du point mémoire. Différentes tendances de processus de Set ont été identifiées, c'est-à-dire **abruptes**, **graduel** et **deux sauts** en fonction de l'empilement mémoire et du schéma de polarisation (polarisation sur l'électrode TOP ou BOT). La Figure D. 2 montre les trois types de Set qu'on a pu identifier.

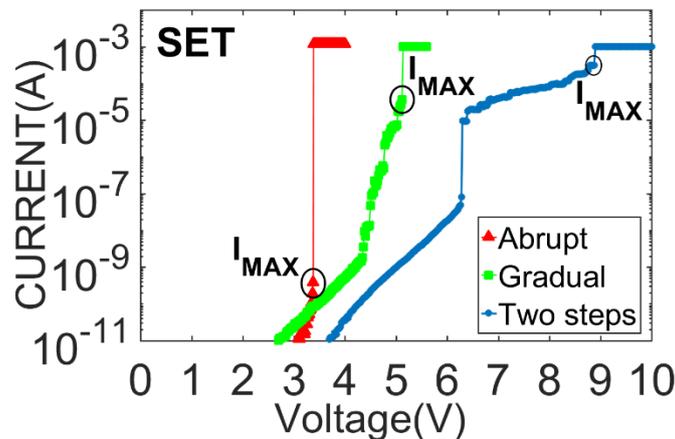


Figure D. 2 : Caractéristiques I-V pour les trois différents processus Set : abrupt (courbe rouge, S1), graduel (courbe verte, S2) et deux sauts (courbe bleu, S3).  $I_{MAX}$  est le courant maximum avant le Set complet.

### 3. Autolimitation du courant et sélectivité à l'état LRS

Dans cette partie, nous analysons les caractéristiques électriques de l'échantillon S2 avec la polarisation au TOP électrode et l'échantillon S3 avec la polarisation au BOT électrode, qui montrent un Set graduel et deux-sauts, respectivement. Pour les deux échantillons, nous avons extrait la sélectivité (NLF : Non-Linearity Factor).

La Figure D. 3 montre les caractéristiques I-V des processus de Set et Reset pour le dispositif S2 avec le Set graduel. La sélectivité, NLF, est défini comme :

$$NLF = I @ V_{SET} / I @ V_{SET}/2.$$

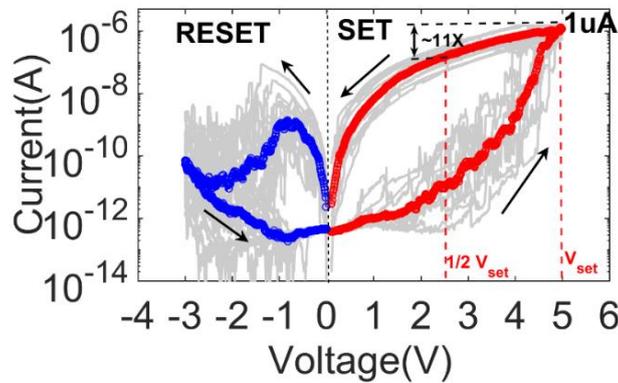


Figure D. 3 : Caractéristiques I-V de Set partiel et du Reset pour le dispositif S2 (Set graduel). La méthode adoptée pour extraire le NLF est expliquée dans la figure.

Une sélectivité de ~10 est la valeur moyenne extraite pour les dispositifs S2 et S3 avec un courant de programmation de ~ 1 μA comme le montre la Figure D. 4.

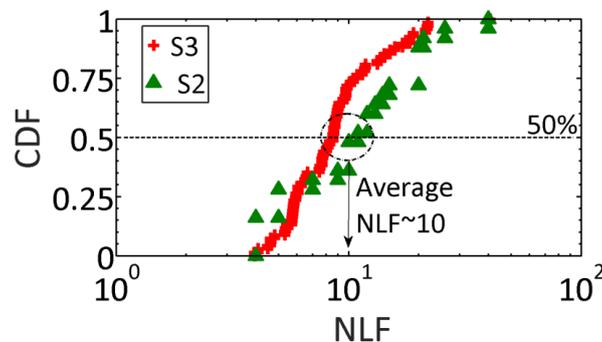


Figure D. 4 : Les distributions de NLF extraites pour les dispositifs S2 et S3 avec ~ 1 μA de courant de programmation.

## 4. Sélecteur à base d'OTS

### a. Structure du dispositif et caractérisation des matériaux

L'élément de stockage dans le dispositif 1S1R est composé d'une couche de résistive de 10nm  $\text{SiO}_x(x<1)$  /10nm  $\text{HfO}_2$  intégrée entre les électrodes inférieure et supérieure TiN et Ti/TiN respectivement. Le sélecteur 1S, est déposé par PVD sur l'électrode supérieure de l'élément de stockage (Ti/TiN), est composé d'une couche de GeSe riche en Se ( $\text{Ge}_{30}\text{Se}_{70}$ ) de 25nm d'épaisseur et d'une électrode supérieure en TiN. Une caractérisation des matériaux a été réalisée pour déterminer le profil des matériaux composant le dispositif 1S1R. La Figure D. 5-gauche montre la section transversale TEM du dispositif 1S1R avec le spectre EDX du sélecteur en GeSe. La Figure D. 5-droite illustre le profil EDX de la structure 1S1R complète, ce profil montre une séparation nette entre les couches intégrées sans aucune interférence de matériaux dans le dispositif 1S1R.

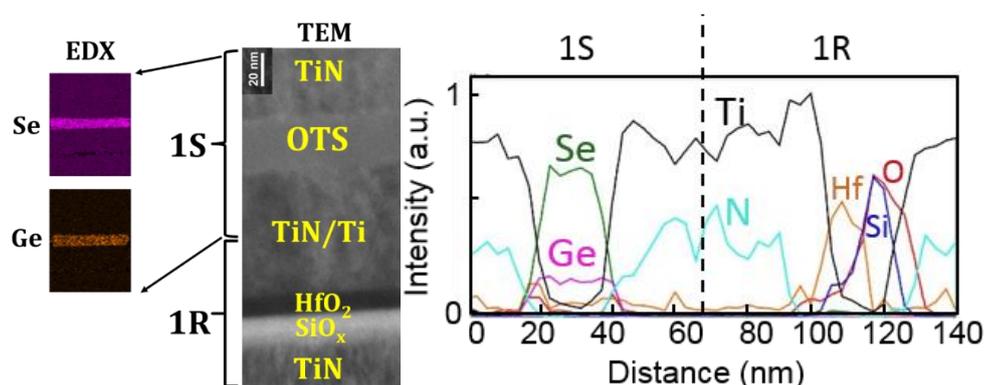


Figure D. 5 : (gauche) Section transversale TEM du dispositif 1S1R et spectres EDX du sélecteur, (droite) Profil EDX de la structure 1S1R.

### b. Caractérisation électrique du dispositif 1S1R

Pour caractériser le dispositif 1S1R et démontrer sa fonctionnalité, nous avons conçu une configuration de mesure basée sur un analyseur de paramètres semiconducteurs (HP4156) et un générateur d'impulsions. Une résistance série ( $R_{\text{ext}}$ ) de 10k $\Omega$  est montée pour surveiller le courant à travers le dispositif testé pendant les impulsions de programmation (Forming/Reset/Set).

Nous avons démontré pour la première fois à notre connaissance la fonctionnalité d'une RRAM à base d'HfO<sub>2</sub> co-intégrée avec un sélecteur à base d'OTS. Les opérations principales d'une mémoire (Forming, Reset et Set) ont été mises en évidence. Les distributions des tensions de programmation du dispositif 1S1R ( $V_f$ ,  $V_{Reset}$  et  $V_{Set}$ ) obtenues pendant les mesures en mode pulsé sont reportées dans la Figure D. 6. La structure 1S1R fonctionne avec des tensions de programmation inférieures à 5V, cette tension est très proche des tensions de fonctionnement typiques d'une RRAM (1R) (3V à 4V).

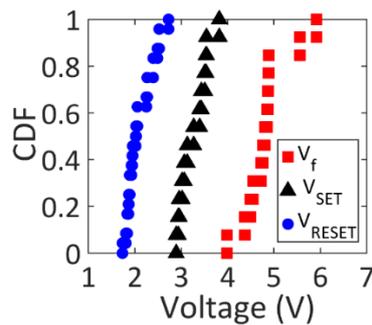


Figure D. 6 : Distributions des tensions de programmation du dispositif 1S1R

Nous avons présenté une stratégie innovante pour lire l'état de résistance des cellules 1S1R. Cette stratégie impose à la tension de lecture ( $V_{read}$ ) d'être inférieure à  $V_{Set}$  afin d'éviter la commutation du sélecteur et ainsi que la mémoire quand cette dernière est à l'état HRS. En plus elle permet de lire correctement l'état LRS en imposant que la tension de lecture doit être supérieure à  $V_{th}$ . Cette stratégie réduira fortement la consommation d'énergie en évitant les lectures perturbatrices.

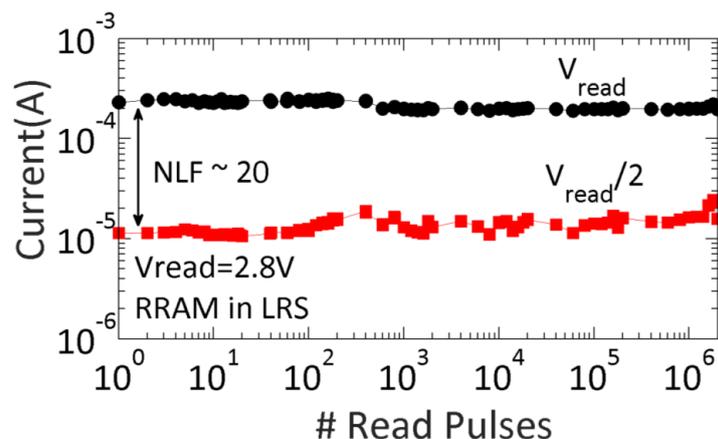


Figure D. 7 : Opération de lecture de l'état LRS à  $V_{read}$  et  $V_{read}/2$  pendant  $10^6$  cycles.

Nous avons étudié la stabilité et la fiabilité de la stratégie de lecture proposée. Jusqu'à  $10^6$  cycles de lecture ont été démontrés pour des impulsions de programmation de  $1\mu s$ . En plus de ces résultats la sélectivité à  $V_{read}/2$  de l'état LRS mesurée est  $\sim 20$  pour le dispositif 1S1R comme le montre la Figure D. 7.

Après avoir démontré la fonctionnalité de la co-intégration 1S1R et la sélectivité à l'état LRS, nous pouvons discuter certaines méthodes qui ont été proposées dans la littérature pour améliorer les performances (augmenter la sélectivité) de tel sélecteur.

Une augmentation de la sélectivité du  $Ge_{30}Se_{70}$  peut être obtenue par le dopage avec Sb et N qui donne le matériau GSSN. Le dopage N, grâce à la formation de liaisons Ge-N améliore la stabilité de l'état OFF du sélecteur, tandis que le dopage Sb permet de contrôler la tension de seuil ( $V_{th}$ ). La Figure D. 8 montre les effets du dopage avec Sb et N dans GeSe sur les caractéristiques électriques. La sélectivité à  $V_{read}/2$  a été améliorée jusqu'à 4 ordres de grandeur par rapport au GeSe non dopé. Par conséquent, GSSN est une solution prometteuse pour la co-intégration avec une RRAM à base d' $HfO_2$  qui peut fournir une sélectivité élevée nécessaire pour les architectures *cross-point*.

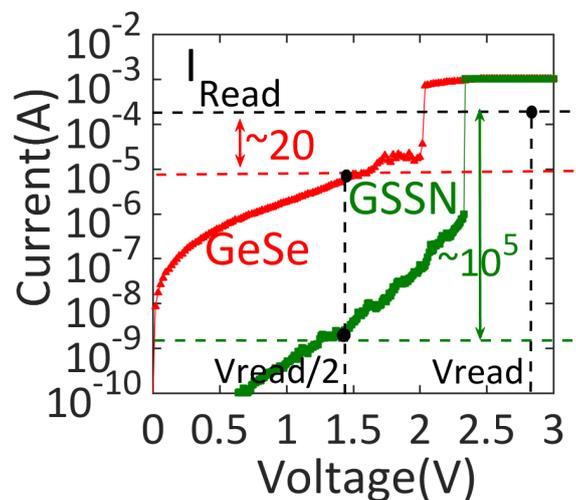


Figure D. 8 : Caractéristiques  $I-V$  mesurées pour l'OTS à base de GeSe présenté dans cette étude et le sélecteur GSSN. Le GSSN offre une sélectivité beaucoup plus élevée par rapport à GeSe

# Author's publications

- 1. In-depth investigation of programming and reading operations in RRAM cells integrated with Ovonic Threshold Switching (OTS) selectors.**  
M. Alayan, E. Vianello, G. Navarro, C. Carabasse, S. La Barbera, A. Verdy, N. Castellani, A. Levisse, G. Molas, L. Grenouillet, T. Magis, F. Aussenac, M. Bernard, B. DeSalvo, J. M. Portal, E. Nowak  
2017 IEEE International Electron Devices Meeting (IEDM).
- 2. Experimental and Simulation Studies of the Effects of Heavy-Ion Irradiation on HfO<sub>2</sub>-Based RRAM Cells.**  
M. Alayan; M. Bagatin; S. Gerardin; A. Paccagnella; L. Larcher; E. Vianello; E. Nowak; B. De Salvo; L. Perniola  
IEEE Transactions on Nuclear Science, vol. 64, no. 8, pp. 2038 – 2045, Aug. 2017.
- 3. Self-Rectifying Behavior and Analog Switching under Identical Pulses Using Tri-Layer RRAM Crossbar Array for Neuromorphic Systems.**  
Mouhamad Alayan; Elisa Vianello; Luca Larcher; Andrea Padovani; Alexandre Levisse; Niccolo Castellani; Christelle Charpin; Sophie Bernasconi; Gabriel Molas; Jean-Michel Portal; Barbara De Salvo; Luca Perniola  
2017 IEEE International Memory Workshop (IMW)
- 4. Correlated Effects on Forming and Retention of Al Doping in HfO<sub>2</sub>-Based RRAM.**  
Mouhamad Alayan; Elisa Vianello; Barbara de Salvo; Luca Perniola; Andrea Padovani; Luca Larcher  
IEEE Design & Test, vol. 34, no. 3, pp. 23 – 30, June 2017.
- 5. Impact of Si/Al implantation on the forming voltage and pre-forming conduction modes in HfO<sub>2</sub> based OxRAM cells.**  
M. Barlas; B. Traoré; L. Grenouillet; S. Bernasconi; P. Blaise; M. Alayan; B. Sklenard; E. Jalaguier; P. Rodriguez; F. Mazen; E. Vilain; M. Guillermet; S. Jeannot; E. Vianello; L. Perniola  
2016 46th European Solid-State Device Research Conference (ESSDERC)

6. **Resistive Memories for Ultra-Low-Power embedded computing design** E. Vianello; O. Thomas; G. Molas; O. Turkeyilmaz; N. Jovanović; D. Garbin; G. Palma; **M. Alayan**; C. Nguyen; J. Coignus; B. Giraud; T. Benoist; M. Reyboz; A. Toffoli; C. Charpin; F. Clermidy; L. Perniola  
2014 IEEE International Electron Devices Meeting (IEDM)

## **Awards:**

**Heavy-ion Upset Immunity of RRAM Cells Based on Thin HfO<sub>2</sub> Layers**

**M. Alayan**; M. Bagatin; S. Gerardin; A. Paccagnella; L. Larcher; E. Vianello; E. Nowak; B. De Salvo; L. Perniola

**Best poster award** in 2016 Radiation Effects on Components and Systems (RADECS 2016)

# Abstract

The performance gaps in nowadays memory hierarchy on the first hand between processor and main memory, on the other hand between main memory and storage have become a bottleneck for system performances. Due to these limitations, many emerging memories have been proposed as alternative solutions to fill out such concerns. The emerging non-volatile resistive random-access memories (RRAM) are considered as strong candidates for storage class memory (SCM), embedded nonvolatile memories (eNVM), enhanced solid-state disks, and neuromorphic computing. However, reliability challenges such as RRAM thermal stability and resistance variability are still under improvement processes. In addition, to achieve high integration densities the RRAM needs two terminal selector devices in one-selector one-resistor (1S1R) serial cell. The BEOL selector device enables suppression of the parasitic leakage paths, which hinder memory array operation in crossbar and vertical 3D architectures.

In this PhD, our main focus is to address and treat the above challenges. Here, the work can be divided into two main parts: i) the investigation of the reliability of HfO<sub>2</sub> based RRAM cells and ii) the characterization of the basis memory operations and performances of HfO<sub>2</sub> based RRAM cells co-integrated with two different back end of line (BEOL) selector technologies.

For the reliability part, we have investigated the effects of aluminum (Al) doping on data retention of HfO<sub>2</sub> based RRAM cells. Single and double layer devices with different aluminum concentration were fabricated and tested. From macroscopic electrical characteristics, like time dependent dielectric breakdown (TDDB) and ramped voltage forming, microscopic properties of the materials such as the activation energy to break a bond at zero field and the dipole moment of the bond were extracted. These parameters have been used to shed new light on the mechanisms governing the forming process by means of device level simulations. Second, we have addressed the radiation immunity of HfO<sub>2</sub> based RRAM for possible space applications as well. Our RRAM devices were exposed to 266 MeV Iodine heavy ions energy. Pre- and post-exposure analysis were carried out on the memory states and the programming voltages to study the effects of the irradiation on the memory characteristics. Throughout this work, we have performed physics based simulations to understand the dynamics of the forming process as well as the physical mechanisms involved during the memory operations.

For the access devices part, we have evaluated two different types of selectors. For accurate reading and low power writing a strong selectivity in the current/voltage characteristics is required. In the first studied device, the selectivity is introduced by adding an oxide tunnel barrier. The main advantage of this strategy is that it is easy to integrate, however it suffers of low selectivity ( $\sim 10$ ) and low programming current. Second, an OTS based selector co-integrated with  $\text{HfO}_2$  based RRAM was fully characterized. OTS selector provides higher selectivity compared to the oxide tunnel barrier with the possibilities to strongly increase this selectivity by material engineering. Over  $10^6$  read cycles have been achieved on our 1S1R devices using an innovative read strategy that we have suggested to prevent disruptive read and to reduce the power consumption.

**Keywords:** Resistive Random Access Memory (RRAM), Forming, data retention, radiation immunity, neuromorphic, cross-point, access device, tunnel barrier, OTS selector, 1S1R.

# Résumé

L'écart de vitesse entre le processeur et la mémoire vive est devenu un point faible pour les performances des systèmes. En raison de ces limitations, de nombreuses mémoires émergentes ont été proposées comme solutions alternatives à ces problèmes existant dans la hiérarchie mémoire. Les mémoires résistives (RRAM) sont considérées comme des candidats pour la « *storage class memory* » (SCM), les mémoires non volatiles embarquées (eNVM), et les systèmes neuromorphique. Cependant, les problèmes de fiabilité tels que la rétention de données sont encore en cours d'amélioration. De plus, pour obtenir des matrices mémoires de grande densité, la RRAM a besoin des sélecteurs qui seront intégrer en série avec elle dans une architecture un-sélecteur une-résistance (1S1R). Le sélecteur est nécessaire avec le point mémoire pour éliminer les problèmes des courants de fuite, qui gênent le bon fonctionnement de la matrice mémoire dans des architectures crossbar et verticales 3D.

Dans cette thèse, notre objectif principal est de traiter les défis ci-dessus. Notre travail peut être divisé en deux parties principales : i) l'étude de la fiabilité des cellules RRAM basées sur  $\text{HfO}_2$  et ii) la caractérisation des opérations de base et des performances des cellules RRAM basées sur  $\text{HfO}_2$  et qui sont co-intégrées avec deux types différents des sélecteurs. Pour la partie fiabilité, nous avons étudié les effets du dopage aluminium (Al) sur la rétention de données des cellules RRAM à base de  $\text{HfO}_2$ . Des dispositifs à simple et double couche avec différentes concentrations d'aluminium ont été fabriqués et testés. A partir des comportements électriques macroscopiques, comme la dégradation du diélectrique en fonction du temps (TDDB) et l'opération de forming avec des rampes de tension, on a extrait des propriétés microscopiques des matériaux tels que l'énergie d'activation nécessaire pour la rupture d'une liaison chimique à champ nul et le moment dipolaire des liaisons dans les matériaux testés. En utilisant ces paramètres microscopiques nous avons effectué tout au long de ce travail des simulations physiques pour comprendre les dynamiques de l'opération de forming ainsi que les mécanismes physiques impliqués pendant les opérations du dispositif mémoire. Deuxièmement, nous avons étudié l'immunité aux rayonnements de la RRAM à base de  $\text{HfO}_2$  pour les applications spatiales. Nos dispositifs RRAM ont été exposés à une énergie de 266 MeV d'ions

lourds d'iode. Des analyses pré- et post-exposition ont été effectuées sur les états de la mémoire et les tensions de programmation pour étudier les effets de l'irradiation sur les caractéristiques du dispositif mémoire.

Dans la partie des dispositifs d'accès, nous avons évalué deux types différents des sélecteurs. Une forte non-linéarité dans les caractéristiques courant / tension est obligatoire pour effectuer une lecture précise et une écriture à faible consommation. Dans le premier dispositif étudié, la sélectivité est introduite en ajoutant une couche d'oxyde dans l'empilement mémoire et qui agit comme une barrière tunnel. Le principal avantage de cette méthode est la facilité d'intégration de la barrière tunnel, par contre elle souffre d'une faible sélectivité ( $\sim 10$ ) et d'un faible courant de programmation qui dégrade la rétention de données. Deuxièmement, on a co-intégré avec l'RRAM un sélecteur OTS et le dispositif 1S1R a été entièrement caractérisé. Le sélecteur OTS offre une plus grande sélectivité par rapport à la barrière tunnel avec les possibilités d'augmenter fortement cette sélectivité par l'ingénierie des matériaux chalcogénures. Plus de  $10^6$  cycles de lecture ont été obtenus pour les dispositifs 1S1R en utilisant une stratégie de lecture innovante que nous avons suggérée pour éviter les lectures perturbatrices et réduire la consommation d'énergie.