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Giap Luong

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THÈSE PRÉSENTÉE

POUR OBTENIR LE GRADE DE

DOCTEUR DE

L'UNIVERSITÉ DE BORDEAUX

ÉCOLE DOCTORALE DES SCIENCES PHYSIQUES ET DE L'INGENIEUR

SPÉCIALITÉ : ELECTRONIQUE

Par Giap LUONG

**Conception d'un amplificateur de puissance
reconfigurable en CMOS nanométrique pour
les applications LTE dans les drones**

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Soutenue le 20 juillet, 2018

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Titre : Conception d'un amplificateur de puissance reconfigurable en CMOS nanométrique pour les applications LTE dans les drones

Résumé :

Les véhicules aériens sans pilote (UAV), souvent appelés drones, trouvent de nombreuses applications dans la vie. Les applications de drones nécessitent plusieurs indicateurs de performance essentiels tels que la couverture, la force du signal, la latence et la mobilité dans des scénarios. Par conséquent, l'utilisation des communications sans fil dans les drones est essentielle pour répondre à toutes les exigences. En raison des connexions au haut débit entre les drones et les utilisateurs pour transférer des données de haut volume à haute résolution, les dernières générations sans fil, comme la norme LTE, sont privilégiées. Il est évident que l'intégration de blocs de radiofréquence (RF) est essentielle pour construire un système sur puce et réduire la taille des drones. Dans ce contexte, cette thèse vise à développer un amplificateur de puissance (PA) innovant avec haute performance reconfigurable entièrement intégré qui adresse les différents besoins imposés par le standard LTE à utiliser dans les applications des UAV. Le PA entièrement intégré en CMOS 65 nm a pour objectif de fournir une puissance de sortie élevée et résoudre le compromis entre la linéarité et l'efficacité. Un transformateur à quatre enroulements est implémenté pour configurer le fonctionnement en multi modes du PA. La technique « segmented bias » permet au PA d'améliorer la linéarité. Le PA obtient non seulement des performances élevées en RF, mais démontre également un potentiel pour l'adopter dans la bande 5G inférieure (3.4-3.8 GHz).

Mots clés : Amplificateur de puissance, CMOS, polarisation segmentée, 4G, drones, transformateur, combinaison de puissance, technique de linéarisation

Title: Design of a reconfigurable power amplifier on 65nm CMOS for LTE applications in drones

Abstract:

Unmanned aerial vehicles (UAVs), often known as drones, have been finding numerous applications in life. Drones applications need several essential performance indicators such as coverage, signal strength, latency, and mobility under scenarios. Therefore, the use of wireless communications in drones is critical to address all requirements. Because of high-speed connections between drones and users to transfer high-resolution high-volume data, latest wireless generations, namely the LTE standard, are privileged. It is straightforward that the integration of RF blocks is essential to build a system-on-chip and shrink the size of drones. To answer the above question, this thesis aims to develop a fully integrated reconfigurable high-performance innovated PA that supports 4G LTE standard to be used in UAVs' applications. The fully integrated 65-nm CMOS power amplifier (PA) provides a watt-level output power, addresses the linearity/efficiency trade-off. A four-winding transformer is implemented to configure the multi-mode operation of the PA. The "segmented bias" technique allows the PA to increase the linearity. The PA not only obtains high radiofrequency performances but also demonstrates a potential to adopt it design in the lower 5G band.

Keywords: Power amplifier, CMOS, segmented bias, 4G, drones, transformer, power combining, linearization technique

Unité de recherche

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*« When something is important enough,
you do it even if the odds are not in your favor »*

Elon Musk

« Luck is a matter of preparation meeting opportunity »

Lucius Annaeus Seneca

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GLOSSARY

CMOS	Complementary Metal Oxide Semiconductor
QPSK	Quadrature Phase Shift Keying
2G	The Second Generation
3G	The Third Generation
4G	The Fourth Generation
5G	The Fifth Generation
BW	Bandwidth
ESD	Electrostatic Discharge
EVM	Error Vector Magnitude
FoM	Figure of Merit
GPRS	General Packet Radio Service
IMD	Intermodulation Distortion
LTE	Long Term Evolution
M2M	Machine to Machine
OFDM	Orthogonal Frequency-Division Multiplexing
IP3	Third-Order Intercept Point
PA	Power Amplifier
PAE	Power-Added Efficiency
PAPR	Peak-to-Average Power Ratio
Psat	Saturated Power
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase shift keying
TSMC	Taiwan Semiconductor Manufacturing Company Limited
WLAN	Wireless Local Area Network
WiMax	Worldwide Interoperability for Microwave Access

1 INTRODUCTION

1.1 Background and motivation

In recent years, wireless applications have emerged into daily life and become significant markets due to the advancements in wireless devices. Wireless communications evolve rapidly into global systems for mobile communications (GSM), general packet radio service (GPRS) to 4th Generation LTE and 5th Generation shortly. Figure 1-1 depicts the evolution of wireless communications. As the wireless standard moves on, the data rate is also increased. Moreover, new wireless standards provide a broader coverage range, more reliable connections thanks to their infrastructures with more base-stations. This point helps assure the connectivity between mobile handsets and other high-tech devices which use machine-to-machine (M2M) communications such as wearables, smart cars, smart homes, and in the big scheme smart cities.

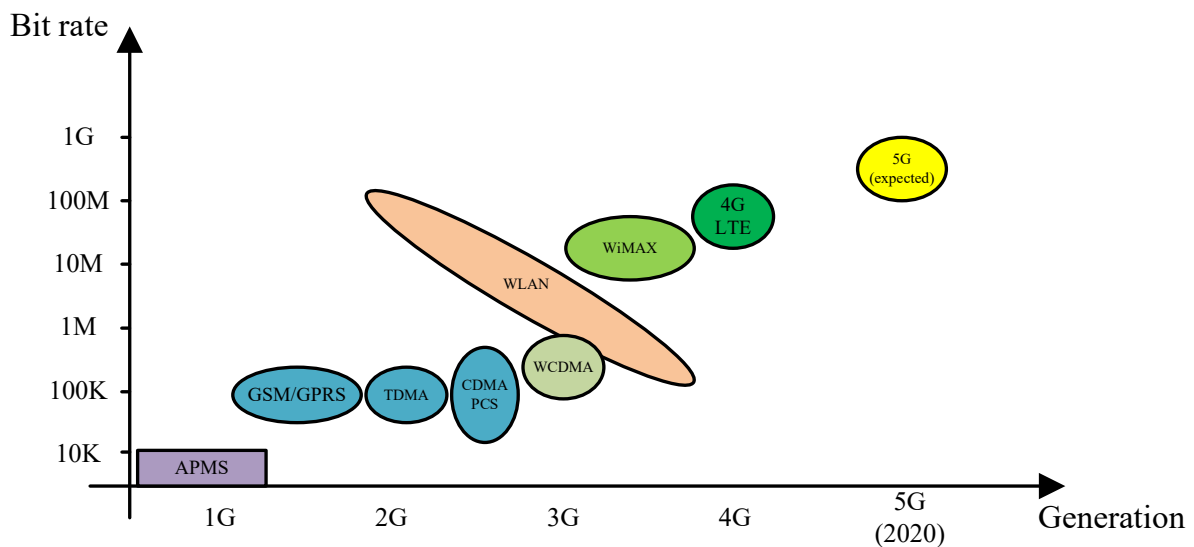


Figure 1-1. Evolution of wireless communications in recent years

Alongside the development of wireless communications, high-tech products are becoming a huge market thanks to the technology development. In these few recent years, unmanned aerial vehicles, often known as drones, have been finding numerous applications in life. Today filmmakers use octocopters or quadrotors to take shots for movies or merely a video from the air; they are well-known as aerial cinematography. Another advanced purpose of drones is delivery assistance. Amazon has done a lot recently to accelerate their shipping services [1]. Drones play the role of delivery man to pick and drop packages to clients. All these applications need several essential performances indicators such as coverage, signal strength, throughput, latency, and mobility under scenarios. Therefore, the use of wireless communications in drones is critical to address all requirements. Because of high-speed

connections between drones and users to transfer high-resolution high-volume data, latest wireless generations are more privileged, namely WLAN, WiMAX or LTE.

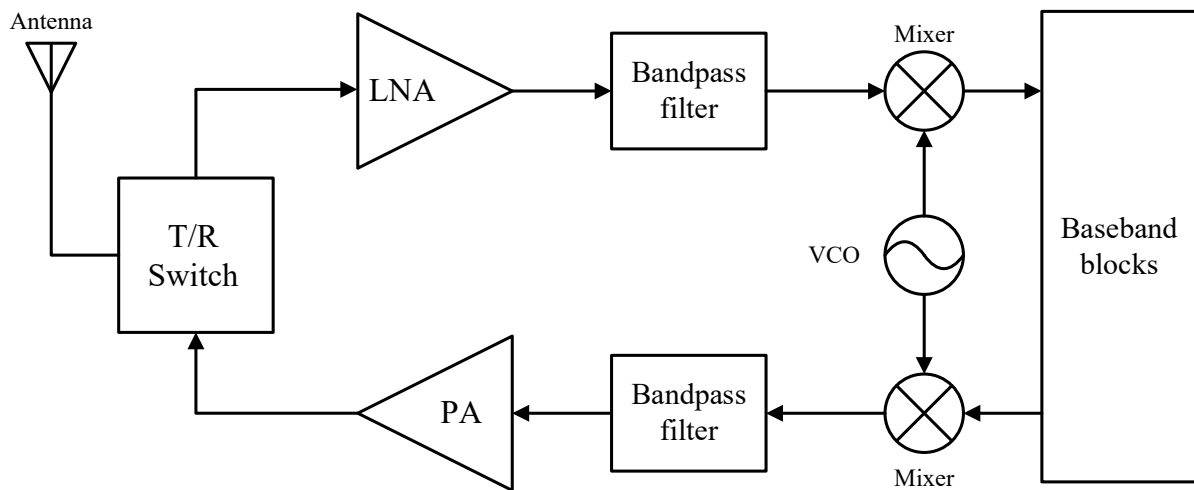


Figure 1-2. Fundamental building blocks for wireless communications

To be commercialized for daily purposes, drones are getting smaller and lighter. The bulk of shrinking size of drones is manufacturing them as a system-on-chip (SoC). It is straightforward that the integration of RF blocks is essential to build a system-on-chip. Figure 1-2 illustrates fundamental building blocks for wireless communications. The latest advances in low-cost complementary metal-oxide-semiconductor (CMOS) technology has made it the first choice for radio frequency transceivers. CMOS technology is a feasible solution for full integration of RF building blocks on a single die to reduce package form factors and their costs. However, CMOS high-performance power amplifiers (PAs) design, the highest power-consuming part, is still a challenging task. The PAs performance issues are output power, efficiency, linearity, gain, and reliability. Battery life of mobile devices demands high-efficiency power amplifiers. Also, envelop-varying systems such as OFDM require PAs to operate linearly to modulate the amplitudes of the signals. Otherwise, the linear PAs present the drawback of low efficiency, degrading battery lifetime. These requirements pose a substantial question to designers about how to build a high-performance PA to be versatile under various scenarios of drones' applications.

1.2 Proposed solution

To answer the above question, this thesis aims to develop a fully integrated reconfigurable high-performance PA that supports 4G LTE standard to be used in unmanned aerial vehicles' applications. Because of numerous flight scenarios of drones, the PA requires acting dynamically to preserve battery life of devices and support high-order modulation schemes such as OFDM. For the ease of integration, the PA has the size restriction under 4mm². Table 1-1

depicts the main specifications of LTE uplink in band 7. The PA is requested to satisfy these parameters.

Table 1-1. LTE Specifications in band 7 (UL) for user equipment terminals

LTE specifications - 3GPP TS 36.101 version 9.12.0 Release 9 Uplink (UL) operating band 7 BS receive - UE transmit	
Specifications	Value
Frequency	2500 MHz – 2570 MHz
Modulation	QPSK, 16-QAM, 64-QAM
PAPR	7dB
Average output power	23dBm
Signal bandwidth	1.25 – 2.5 – 5 – 10 – 15 or 20MHz

1.3 Manuscript organization

This manuscript is organized according to the following chapters.

Chapter 1 introduces the background of the thesis and the motivation of integrating power amplifier into RF blocks in unmanned aerial vehicles. This chapter also proposes a solution to address high levels of PAPR of the LTE signal, enhance the efficiency of power amplifiers in power back-off and achieve the best trade-off of linearity and efficiency.

Chapter 2 gives an overview of CMOS 4G LTE power amplifier in UAVs' applications. The chapter presents traditional classes of PAs, equations for measurements, topologies, and efficiency enhancement techniques. Next, this chapter discusses the categories of unmanned aerial vehicles and their applications in recent years.

Chapter 3 discusses the passive component characterization. The design guide of transformers is also presented. The chapter details design steps to implement transformers for PAs and depicts loss mechanisms affecting on transformers' performances.

Chapter 4 presents in details the conventional design and integration methodology for PAs and proposes a new approach for the reconfigurable power amplifier based on the use of segmented bias technique and power cell switching technique. In this chapter, the fabricated chip, the measurement setup and the measured performance are also illustrated.

Chapter 5 concludes the whole dissertation and compares the obtained results with objectives and proposes future works.

1.4 Publications

G. Luong, J.-M. Pham, P. Medrel, and E. Kerhervé, “A Watt-Level 4G LTE CMOS Reconfigurable Power Amplifier with Efficiency Enhancement in Power Back-Off,” in The Tenth International Conference on Advances in Circuits, Electronics and Micro-electronics ([CENICS](#)), Rome, Italy, 2017.

G. Luong, J.-M. Pham, P. Medrel, and E. Kerhervé, “Design of a 2.5 GHz LTE 65-nm CMOS Reconfigurable Power Amplifier for UAVs,” in The 15th IEEE International New Circuits and Systems Conference ([NEWCAS](#)), Strasbourg, France, 2017.

G. Luong, E. Kerhervé, J.-M. Pham, P. Medrel, “A 2.5-GHz Multi-Mode Broadband Bias-Segmented Power Amplifier with Linearity-Efficiency Trade-off,” *IEEE Microwave and Wireless Components Letters*, 2018 (Accepted)

2 OVERVIEW OF POWER AMPLIFIER DESIGN FOR 4G LTE APPLICATIONS IN UNMANNED AERIAL VEHICLES

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This chapter overviews 4G LTE wireless applications with radiofrequency integration in unmanned aerial vehicles. The first part presents the LTE standard for band 7 of the uplink. This band is used for diverse mobile applications and recently in drones. After that, a solution of the reconfigurable multimode power amplifier in drones is also detailed. With enhancement techniques, the PA fundamental operating principle is firstly described. Also, the technological families used for wireless communications are discussed. Finally, the design specifications of the power amplifier is also presented to address the requirements of LTE standard.

2.1 Specification of 4G LTE standard

2.1.1 The LTE Standard

To evolve from 3rd generation communication systems to 4th generation systems, the Third Generation Partnership Project (3GPP) has released the Long Term Evolution (LTE) specifications. The critical changes in this generation are in the physical layer (PHY) with modulation schemes and access techniques. The LTE standard relies on Orthogonal Frequency Division Multiplexing Access (OFDMA) for downlink and Single Carrier Frequency Division Multiple Access (SC-FDMA), a similar method of OFDM for uplink.

The LTE standard allows data rate to go over 100 Mbps and to reach 326 Mbps for downlink and 86 Mbps for uplink. This improvement can be implemented by the use of multiple antennas (8 antennas maximum) for base-stations and mobile terminals (MIMO: Multiple Inputs Multiple Outputs) and by the exploitation of spatial multiplexing (SDMA: Space Division Multiple Access) with an adequate code for each antenna signal. The LTE introduces higher data rate and better spectrum usage than its predecessor. Moreover, this standard can support high package transfer time (lower latency time) about 5 ms, much better than 70 ms of UMTS (Universal Mobile Telecommunications System).

The principal characteristics of the LTE standard include:

- Uplink data rate can reach 100 Mbps for 20 MHz of bandwidth
- Downlink data rate can reach 50 Mbps for 20 MHz of bandwidth
- Available bandwidths are 1.4 MHz, 3 MHz, 5 MHz, 10 MHz, 15 MHz, 20 MHz

2.1.2 FDD and TDD

In wireless communications systems, it is essential to use either a half-duplex scheme or a full-duplex scheme to transfer data in two directions (uplink and downlink). The LTE uses

two duplex schemes: Frequency Division Duplexing (FDD) and Time Division Duplexing (TDD).

Frequency Division Duplexing (FDD) consists in separating the downlink from the uplink by using different frequency bands for data transfer. This characteristic brings to mind that the uplink and the downlink signals do not interfere with each other. Hence, FDD is suitable for symmetric traffic. Most cell-phone systems and the newer 4G LTE systems use FDD. Cable TV systems are also entirely FDD. FDD can also be found in asymmetric digital subscriber line (ADSL), very high bit rate digital subscriber line (VDSL), UMTS/WCDMA Frequency Division Duplexing mode, CDMA2000 system and IEEE 802.16 WiMAX Frequency Division Duplexing mode.

Time Division Duplexing (TDD) uses a single frequency band for data transfer. It shares that band by assigning alternative time slots to transmit and receive operations. The information, which can be voice, video or data to be transmitted, is formatted in serial binary. Each time slot may be one byte long or even a frame of several bytes. TDD is thus suitable for asymmetric traffic due to its capability of dynamic time slots allocation for both uplink and downlink. Most wireless data transmissions are in TDD. TDD can be found in WiMAX, Wi-Fi, ZigBee or Bluetooth if piconets are deployed. Most digital cordless telephones use TDD. Due to the spectrum shortage and expense, TDD is being chosen in some cellular systems, such as China's TD-CDMA and TDD-LTE System.

2.1.3 The OFDMA and the SC-FDMA

OFDM technique uses multiple subcarriers within an original channel bandwidth. Each of these subcarriers is separately modulated. On a side note, there can be hundreds of subcarriers with a frequency space (15 kHz on the LTE case). All subcarriers are transmitted in parallel; hence, each one can be broadcasted with a higher symbol rate. This characteristic enhances the robustness of the technology in mobile propagation conditions. The symbols, which are modulated previously with modulation schemes such as QPSK (quadrature phase-shift keying), 16QAM (quadrature amplitude modulation) or 64QAM, can be processed for the first step in the transmission chain. After that, an Inverse Fast Fourier Transform (IFFT) takes place. It converts the signal from the frequency to the time domain. This operation creates symbols for data transmission. Moreover, a cyclic prefix is added to symbols to dodge intersymbol interference (ISI) and intercarrier interference (ICI). OFDMA, a multiple-access scheme based on OFDM, allocates users in both time and frequency. Figure 2-1 depicts the difference between an OFDM and an OFDMA system. OFDMA is used for the downlink of LTE systems.

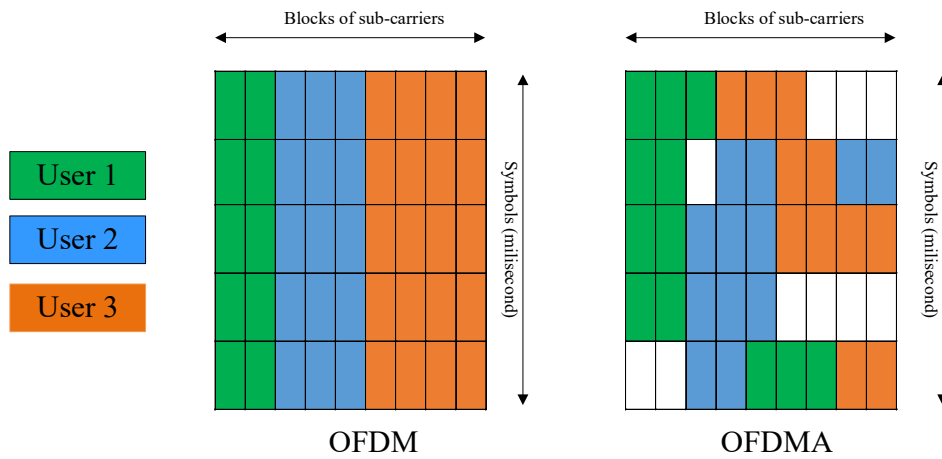


Figure 2-1. Allocation of subcarriers OFDM and OFDMA

Since OFDMA requires a high level of PAPR, it is necessary to use another technique requiring lower PAPR for the uplink. SC-FDMA introduces the best solution for LTE uplink in terms of low PAPR. SC-FDMA is a multiple access technique based on the single-carrier frequency-division multiplexing (SC-FDM) modulation technique. It can be referred as discrete Fourier transform (DFT)-spread OFDM. Consequently, SC-FDMA inherits the main advantages of OFDMA about multipath mitigation and low-complexity equalization [1]. The main difference is that SC-FDMA deploys a precoding DFT before IFFT to create symbols. Each subcarrier covers all parts of each symbol and produces a virtual single-carrier system. SC-FDM thus introduces a lower PAPR than OFDM. This characteristic plays a vital role in the user equipment in terms of power efficiency. Figure 2-2 presents an example of the uplink in SC-FDMA and the downlink in OFDMA.

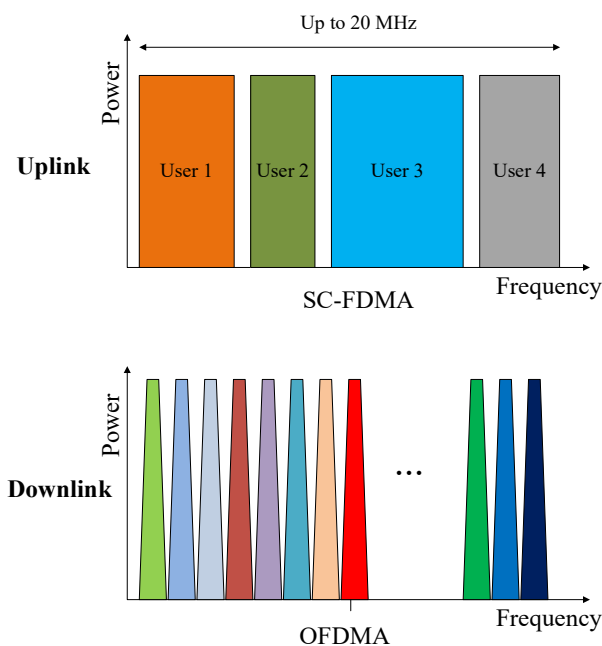


Figure 2-2. Uplink spectrum for 4 users in SC-FDMA and downlink spectrum in OFDMA

The organization 3GPP specifies 21 frequency bands for FDD mode (Frequency Division Duplexing) based on different regions. In Europe, the used bands are:

- Band 20, attributed to rural zones with the downlink from 791 MHz to 821 MHz and the uplink from 832 MHz to 862 MHz
- Band 7, attributed to urban zones, with the downlink from 2620 to 2690 MHz and the uplink from 2500 to 2570 MHz

Figure 2-3 presents the frequency attribution in band 7 of the LTE in France. Four mobile operators, SFR, Orange, Bouygues and Free, share this band for mobile applications with different frequency sub-bands.

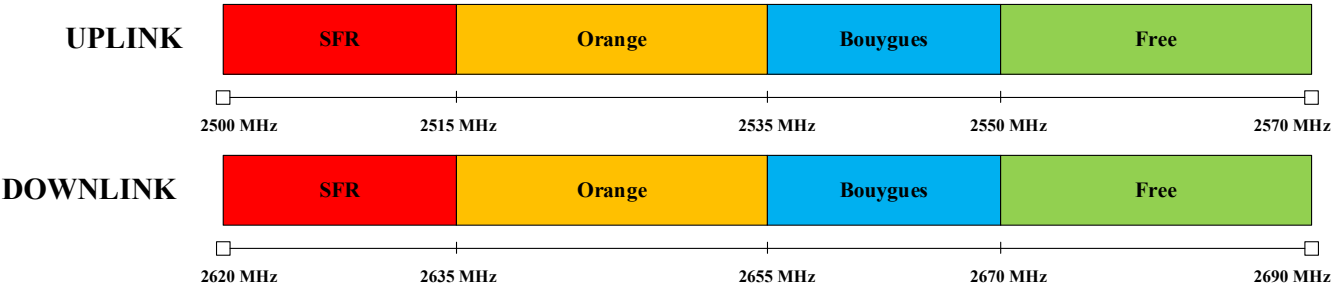


Figure 2-3. Frequency attribution in band 7 of LTE in France

2.2 Overview of unmanned aerial vehicles (UAVs)

In recent years, unmanned aerial vehicles, also commonly known as drones or remotely piloted aircrafts, have found a wide range of applications in the aerospace and defense community, as well as the bright spot in the economic picture. UAVs promise to provide cost-effective wireless connectivity for mobile terminal without infrastructure coverage. Low-altitude UAVs is fast deployed, flexibly reconfigured and likely to have better communication channels due to the presence of short-range line-of-sight (LoS) links. Nevertheless, the use of mobile and energy-constrained UAVs for wireless and RF communications also introduces many challenges on circuit designers. Figure 2-4 shows a basic RF communication of UAVs system.

The first attempt of drones is taken place in the United States during World War I. It aims to build an automatic pilot system deployed in hostile territory. In 1917, the USA army started an aerial torpedo, or flying bomb, project led by Lieut. Col. Bion J. Arnold for the Air Service and Charles Kettering [2]. From the military initiative purpose, the unmanned aircraft technology seems to be headed towards greatly expanded use. Eventually, drones become more commercialized in industry, for example, for use in shipping services, surveillance systems or even merely high-tech gadgets. An affordable and small drone can be successfully built within

about nine months. With the recent advances in low-size and low-cost electronics, a new avenue of UAVs has thus emerged.

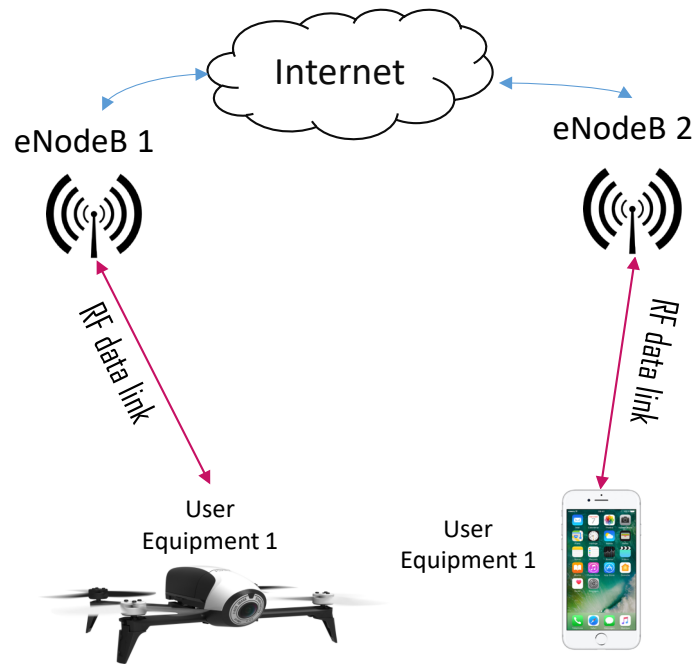


Figure 2-4. LTE communications of UAV system

UAVs can be classified into two categories: fixed wing and rotary wing, each with their strengths and weaknesses. Fixed-wing UAVs have a heavy payload and high speed, but they need to maintain the continuous forward movement to remain aloft. This kind of drones, therefore, is not suitable for mobile applications that require high mobility and stationary capacity. On the other hand, rotary-wing UAVs can move in any direction and maintain its autonomy in the air. Choice of UAVs thus critically depends on the applications. Figure 2-5 shows two kinds of system.

Among various applications enabled by unmanned aerial systems, the use of UAVs for high-speed wireless communications play a crucial role in the evolution of communication systems. UAV-aided wireless communications provide a promising solution to wireless connectivity for mobile terminals. On-demand UAVs are cost-effective, swiftly deployed and especially suitable for unexpected or on-demand short-time missions. Additionally, short-range UAVs offer LoS communication links in most scenarios, which can improve the performance of the direct communication between source and destination. Furthermore, adaptive communications can be jointly designed with UAVs' control to enhance the communication performance. These reasons prove why the design of integrated wireless systems for UAVs becomes one of the favorite trends in circuit design.



Figure 2-5. Two categories of UAVs: a) Fixed-wing b) Rotary-wing

In UAVs, the maximum transmission distance is a critical parameter. 4G LTE communication system has been eventually developed as an innovative solution for autonomous drones to overcome the limitation of distance. 4G LTE drones are not touched by the ordinary problems that Wi-Fi or Bluetooth communications experiences, for example, low SNR (Signal to Noise Ratio) due to extensive coverage areas. However, it is also crucial that the communication cannot be cut off even at a limited distance. Oxygen, water, and other obstacles can attenuate the signal. Hence, 4G LTE drones must satisfy the requirement of 4G LTE communications about power level, linearity, efficiency and so forth. Table 2-1 depicts the main characteristics of recent wireless communications [27], among which the 4G shows its advantage regarding coverage area, data rate, and latency.

Table 2-1. Comparison of communication protocols for UAV applications

	Bluetooth	WiFi	ZigBee	EDGE	UMTS	4G (band 7)
Coverage range	50-100m	~50 m	10-100m	35 km	80 km	100 km
Frequency	2.4 GHz	2.4 GHz or 5 GHz	2.4 GHz	876MHz (UL) 921MHz (DL)	1.92GHz (UL) 2.11GHz (DL)	2.5GHz (UL) 2.62GHz (DL)
Data rate	1Mbps	~200 Mbps	250 Kbps	250 Kbps	14 Mbps max	10-300 Mbps
Latency	100ms	151ms	15ms	629ms	212ms	98ms

Figure 2-6 depicts a model of wireless communication channel loss, which can be applied to the LTE channel loss model.

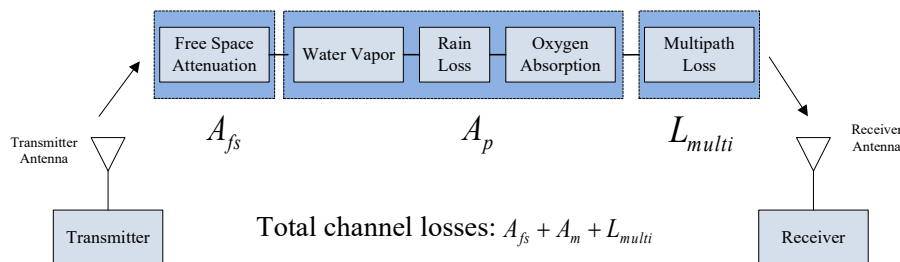


Figure 2-6. Wireless communication channel loss model

2.3 Power amplifier fundamentals

Power amplifiers (PAs) are critical components in the front-end transmitter and used to amplify the signal to a required output power; hence, the signal can be detected at the receiver with an equivalent level of power. The process of PA design is a multi-step one with several loops. The first step is selection and sizing of input of devices. The second one is measurement of output impedances and design of matching network in schematic and the electromagnetic field. PA design finishes with optimization, simulation, and measurement of the circuit. For these reasons, designing PA is one of the most significant challenges in the integrated circuit design with a large number of trials and errors. As the most power-consuming block in RF transceivers, PAs are characterized mainly and carefully by maximum output power, linearity, power gain, and efficiency. Figure 2-7 illustrates the printed circuit board of iPhone X, which comprises of five PAs of Skyworks and two PAs of Broadcom.

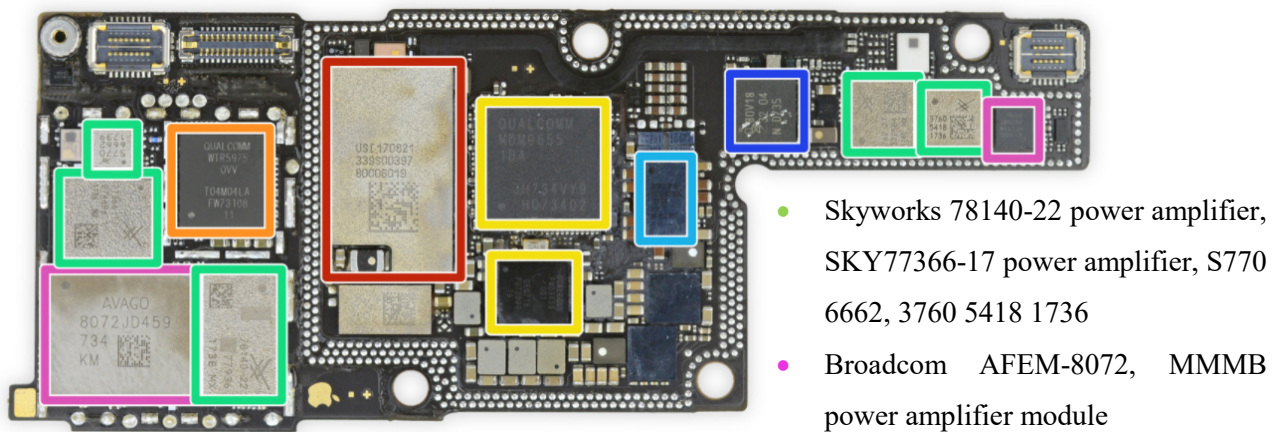


Figure 2-7. iPhone X teardown printed circuit board from ifixit.com

2.3.1 Principal parameters of Power Amplifier

2.3.1.1 Output power

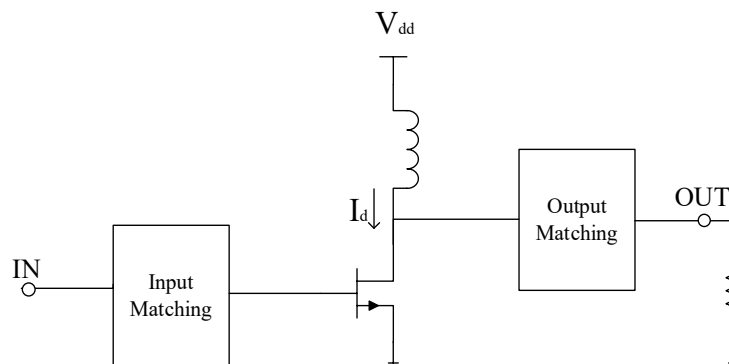


Figure 2-8. A typical power amplifier

Figure 2-8 shows a typical power amplifier including a transistor, an input, and an output matching networks. The PA can generate power at several frequencies. However, it is mainly

used at the fundamental frequency with the highest output power. This level of output power can be calculated on the load R_L as below:

$$P_{out} = \frac{V_L^2}{2R_L} \quad (2.1)$$

Where V_L is the delivered voltage to load at the fundamental frequency.

The maximum output power of PA depends on the supply voltage V_{dd} and the optimal output impedance of transistor. Therefore, to achieve the best output power, the output-matching network must be perfectly matched to the transistor's optimal output impedance. The power gain of PA can be calculated by the difference between the output power at the load and the input power that is transmitted from the source.

$$Gain = P_{out} - P_{in} \quad (2.2)$$

2.3.1.2 Efficiency

Regarding the capability of converting DC power to RF power, two definitions of efficiency can be used to characterize PAs. Drain efficiency, η , is the direct relationship between the output power at the load R_L and the DC power. It can be sometimes called DC-to-RF efficiency.

$$\eta = \frac{P_{out}}{P_{dc}} \quad (2.3)$$

Where P_{out} the output power of PAs at the load is calculated in the equation (2.1) and P_{dc} is the DC power provided by the supply source V_{dd}

$$P_{dc} = V_{dd} \times I_d \quad (2.4)$$

Power added efficiency (PAE) is the most used efficiency measurement, in which the input power and the gain of PAs are also taken into account. PAE is defined as below:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} = \frac{P_{out} - \frac{P_{out}}{Gain}}{P_{dc}} = \eta \left(1 - \frac{1}{Gain} \right) \quad (2.5)$$

Where P_{in} is the input power of PAs.

It can be seen from the equation (2.5), the power gain of PA needs to be high enough to get the high output power and efficiency. Therefore, highly efficient PAs become one of the most famous subjects in mobile applications with the high demand for a long-lasting battery.

2.3.1.3 Linearity

Linearity of PAs can be characterized by three measurements: the 1-dB gain compression point (P_{1dB}), the phase distortion AM-PM and the adjacent channel power ratio (ACLR or ACPR). First measurement for the 1-dB gain compression point indicates the power-handling

capability of PAs in the linear region. This point is measured in which the nonlinearities of PAs reduce the power gain by 1-dB. Before the P_{1dB} point, the PA is considered as a linear system in which its linearity is affected by an amplitude distortion (AM-AM).

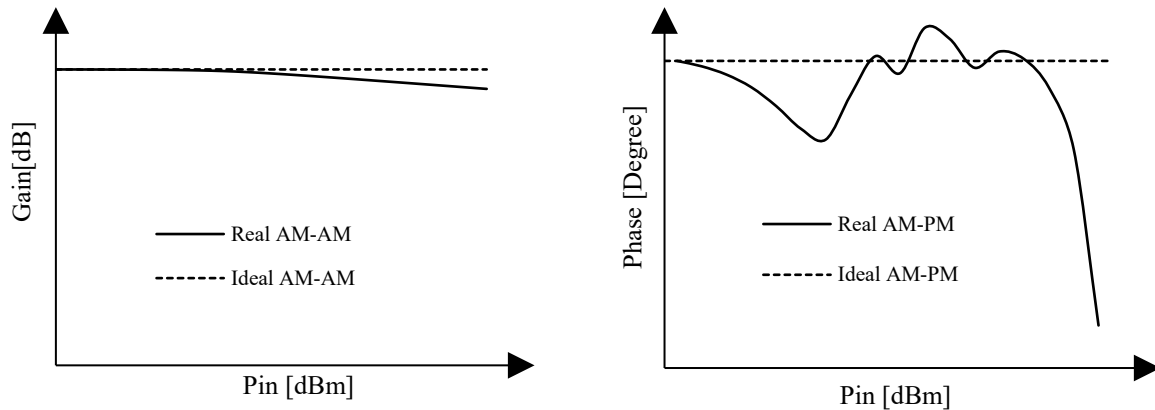


Figure 2-9. AM/AM and AM/PM Conversion

Second measurement for the phase distortion AM-PM indicates the undesired phase deviation of the output signal when the input power increases. The AM-PM parameter illustrates how the nonlinearities of PAs corrupt the phase of the carrier. The measurements of AM-PM and AM-AM distortions, as in Figure 2-9, can be done with the circuit excited by the single-tone signal.

Another linearity measurement for non-linear systems is the third-order intercept point (IIP3), which needs the excitation of two-tone signals. The IIP3 measures the distortion caused third-order intermodulation products ($2f_2 - f_1$ and $2f_1 - f_2$). Moreover, high-order intermodulation (IMD) can cause the spectral regrowth for the modulated signal, namely Quadrature Phase Shift Keying (QPSK) or Quadrature Amplitude Modulation (QAM). Figure 2-10 shows the spectrum of a PA with included two-tone intermodulation products.

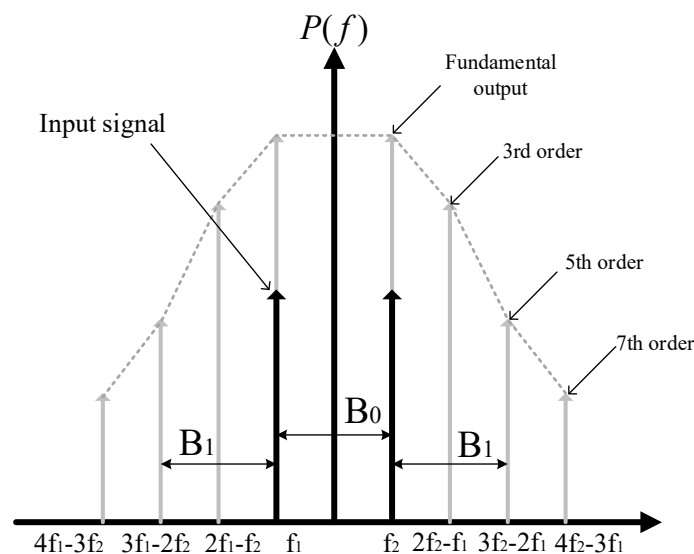


Figure 2-10. Two-tone intermodulation product spectrum

Due to nonlinearity, the IMD products appear in the sidebands of two input tones at the same frequency spacing. PA designers mainly focus on the third and the fifth order IMD products to analyze the linearity of PAs. However, the higher order IMD products such as the seventh or the ninth order can also have a significant impact on PAs' performances. The high order IMD products fall into adjacent channels and create unwanted spectrum at these channels. Third measurement, adjacent channel power ratio (ACLR), is defined as the ratio of the usable power in the main channel and the measured power in adjacent channels of a specified bandwidth to evaluate the influence of the unwanted spectrum, as shown in Figure 2-11.

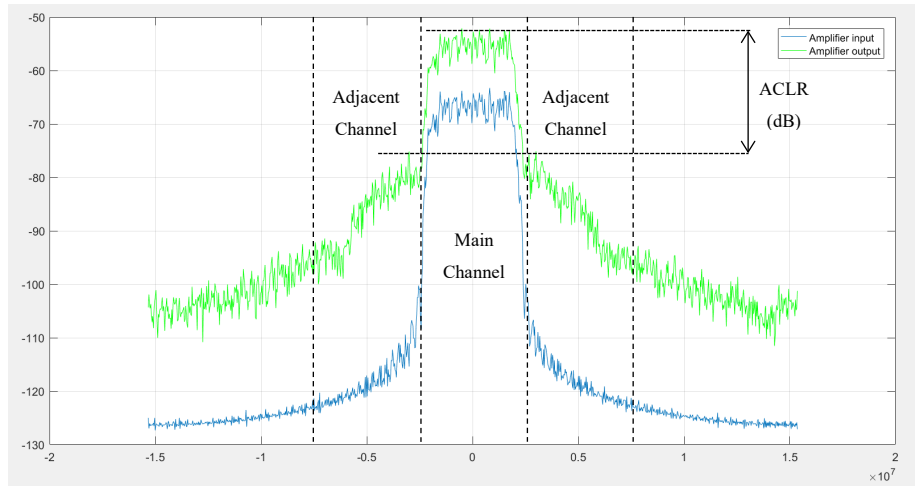


Figure 2-11. Modulated signal spectrum by a nonlinear PA

It is necessary to apply a modulated waveform such as QPSK, 8QAM, 16QAM or 64QAM into the input of PAs to measure the spectral regrowth in adjacent channels.

2.3.2 Operating classes of Power Amplifier

Power amplifiers are categorized into two classes: sinusoidal class and switching class. In sinusoidal classes (A, B, AB, and C), power amplifiers are classified by the conducting angle of the transistor current. In switching classes (D, E, and F), the shapes of the drain/collector voltage and current controlled by the output-matching network decide the classes of power amplifiers. This section reviews operation classes of power amplifiers.

2.3.2.1 Sinusoidal classes A, B, AB and C

The conducting angle of the transistor, which is defined by the bias voltage V_{GS} on the gate of the transistor, differentiates sinusoidal classes. Figure 2-12 shows a typical single-ended power amplifier in class A, AB, B and C. R_{load} is the load, to which the PAs delivers the output power. The choke inductor is used in the drain of the transistor to prevent the alternating current flowing into DC source. The large resistor is connected to the gate of the transistor for biasing. The large capacitor C_B is used to block the DC current to the load. The LC tank is used to keep

the sinusoidal RF signal on the load. The V_{bias} voltage and the bias resistor R_{bias} configure the PA to operate in class A, AB, B or C as in Figure 2-13.

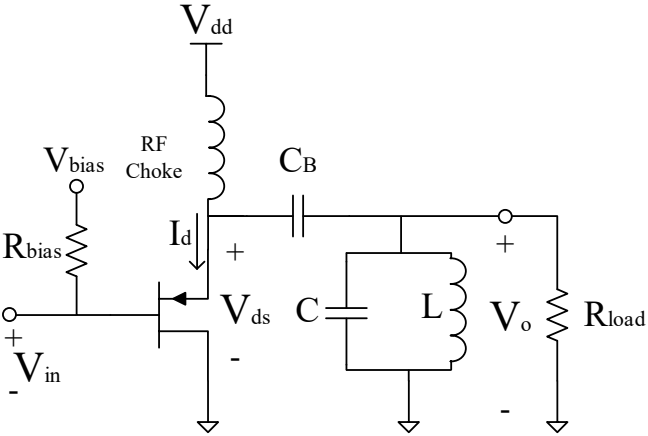


Figure 2-12. A typical A, AB, B, C sinusoidal power amplifiers

In class A, the operation point and the input power are chosen to make the drain current to flow at all time. The conduction angle of the drain current in the class-A power amplifier is 360° . Class A, therefore, works in the linear region and minimizes the signal distortion. Also, the operation point is chosen at the middle of the AC load line to maximize RF signal swing. The bias voltage V_{bias} is set far above the breakdown voltage V_T of the transistor. In class B, the gate of the transistor is biased at the threshold voltage V_T ($V_{bias} = V_T$), so that the drain current conducts in half of every cycle. The conduction angle of the drain current is 180° . In class B, the operation point and the input signal level are chosen to set the conduction ratio of the drain current more than a half of every cycle. The conduction angle is greater than 180° and smaller than 360° . In class C, the gate of the transistor is biased below at the threshold voltage V_T ($V_{bias} < V_T$), so that transistor conducts the current less than a half of cycle. The conduction angle of class C is less than 180° .

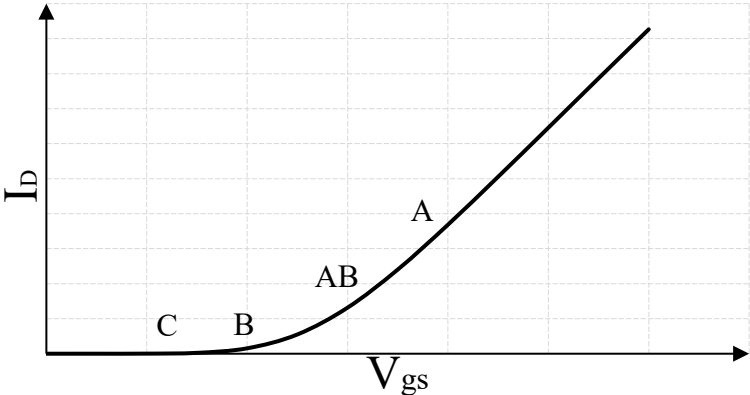


Figure 2-13. Sinusoidal operation classes of power amplifiers

The main advantage of class A is its high linearity due to the current conduction of all the time. Proper linearity can also be accomplished by class AB or class B if the power is considered

to be back-offed; hence degrading the efficiency as well. The class A, AB and B PAs are used widely for low-power applications, in which the efficiency is the most critical parameter, or for high-linearity applications such as CDMA systems or OFDM systems, where the amplitude of the modulated signal is variable. Regarding efficiency, class A can achieve a maximum theoretical efficiency about 50% while class B can reach 78.5%. It is important to notice that the efficiency in the fully integrated power amplifier, for example, in Silicon or GaN is strongly dependent on some non-idealities such as finite inductor quality factor, substrate loss, saturation voltage of transistors. Class C achieves over 78.5% of theoretical efficiency or even approaches 100% but sacrifices the linearity of PAs as the conduction angle decreases. Due to the difficulty of obtaining low conduction angles on an integrated circuit while sustaining the high level of output power, the class-C fully integrated power amplifier is not widely used. Class C is usually combined with another type like class B or AB to tradeoff the linearity and the efficiency, namely in Doherty power amplifier. Table 2-2 outlines the main characteristics of linear-class power amplifiers

Table 2-2. Linear-class power amplifiers

Class	Conduction angle	Maximum theoretical efficiency	Linearity
A	360°	50%	Linear
B	180°	78.5%	Non-linear
AB	$180^\circ < \alpha < 360^\circ$	$50\% < \eta < 78.5\%$	Non-linear
C	$< 180^\circ$	$>78.5\%$	Non-linear

2.3.2.2 Switching classes E and F

Switched-mode amplification is based on the operation of the transistor between two discrete and idealized states. In ON state, the transistor is assumed to behave like a short circuit while it is considered as an open circuit in OFF state. In switching classes, it is important to note that the output signal amplitude is uncorrelated with the input signal amplitude. The parameters such as supply voltage, output power, and load impedance dictate the output signal impedance. Therefore, the efficiency of switched-mode power amplifiers ideally achieve 100% but inherently sacrifice the linearity. Amongst switching class power amplifiers, class D PAs is not suitable for RF applications because of the significant loss caused by the output capacitance of transistors. Therefore, class D PAs are mainly employed in audio frequency applications. For RF applications, class-E and class-F PAs are widely used thanks to its high efficiency and circuit simplicity. In switched-mode E/F PAs, the transistor can be controlled by a square-wave voltage at the gate of the transistor. It allows the current to flow in case of no drain voltage and

to self-remove in case of the drain voltage setting up to the transistor. Voltage and current are ideally configured with an offset to eliminate power dissipation and obtain the peak efficiency.

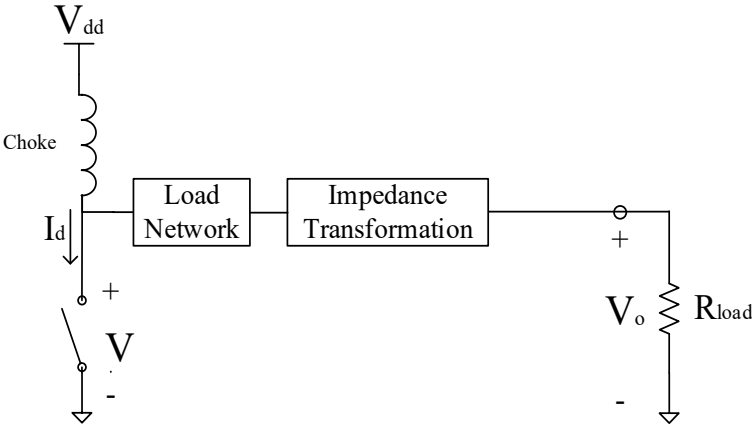


Figure 2-14. Schematic of a switching power amplifier

Sokals introduced Class-E PA in 1975 and used in widespread applications due to its high efficiency and low circuit complexity [3]. The underlying topology of class-E PA is illustrated in Figure 2-15. The RF choke is assumed to allow for a constant DC current to conduct into the transistor. C_0 and L_0 are designed to form a series resonator, and its quality factor is high enough. Hence, the output load current is purely a sinusoidal wave. C and jX are designed based on two class-E switching conditions.

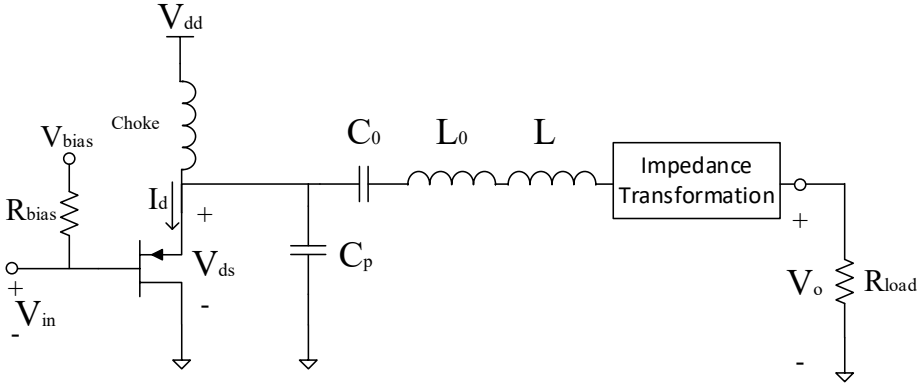


Figure 2-15. Class-E power amplifier

Class-F power amplifiers consist in shaping voltage and current waveforms by utilizing harmonic termination as used in Figure 2-16. Ideal class-F PA is built with a finite number of series odd harmonic terminations and a parallel resonator of the fundamental frequency. In Fourier analysis, the amplitude of the fundamental component of a square wave signal is higher than that of the signal. The PA thus presents better performances than the sinusoidal classes [4]. The voltage waveform is a square waveform. Therefore, if the current waveform is a half-sine waveform, the current and the voltage do not overlap simultaneously. A pure sine current flows at the output load. Consequently, the efficiency can theoretically achieve 100%. Moreover, if the

current waveform is a sine waveform, the current and the voltage coexist in a half period. The efficiency of PAs is degraded to 64% at peak.

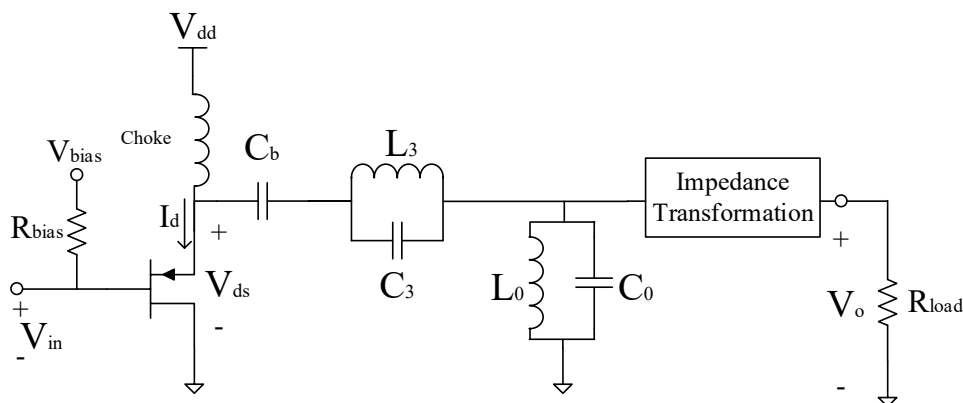


Figure 2-16. Class-F power amplifier

Table 2-3 outlines the characteristics of switching classes E/F.

Table 2-3. Class E/F summary

Class	Input voltage	Output current	Output voltage	Load network design's methodology	Efficiency
E	Square	Square	Square	Time domain	100%
F	Sinusoidal	Sine	Square	Frequency domain	64%
		½ Sine	Square		100%

2.3.3 Impedance Matching: Load-pull/Source-pull method

Load-pull is a colloquial term applied to the process of load adjustment for a device under test (DUT), mostly for a transistor, to get its performance and the parameter to deliver that performance in a network. Load-pull is the most common method globally used for RF and millimeter-wave power amplifier design, transistor characterization, semiconductor process development, and ruggedness analysis. In power amplifiers, load-pull/source-pull method is a repeated loop to get the convergent output/input impedances. The source and load impedances of PAs are fixed to constant values, for example, 50 or 100 Ohm. The input and output optimal impedances of the transistor are still in need to be identified. These impedances, which are not precisely computed by mathematics equations, depends strongly on the intrinsic components of a transistor. Load-pull/Source-pull method allows circuit designers to determine more precisely these values of input and output impedances. Figure 2-17 shows a traditional load-pull system used widely in impedance's measurement for PAs.

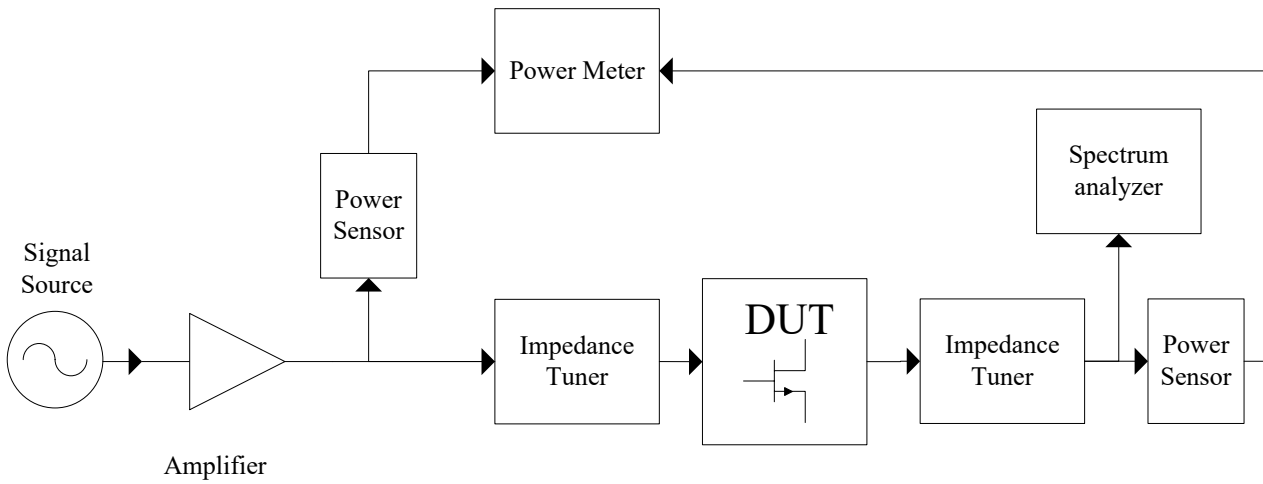


Figure 2-17. Traditional load-pull system

Load-pull consists of varying different load impedance seen by a transistor to find the best performance of PA on the Smith chart. When the load is varied, the parameters of transistors such as power, gain, and efficiency are also measured. Output power and efficiency are drawn on the Smith chart in several curves. The load impedance is thus readily determined to optimize power, efficiency or trade-off of both parameters. When the load impedance is identified, source-pull is performed to obtain the optimal input impedance of transistor. Load-pull and source-pull are proceeded in sequential order and repeated until the input and output impedances are converged. Figure 2-18 depicts an example of load-pull to determine the optimal impedances to optimize PAE and Output power. Figure 2-19 illustrates the flowchart to determine the optimal input and output impedances of PAs.

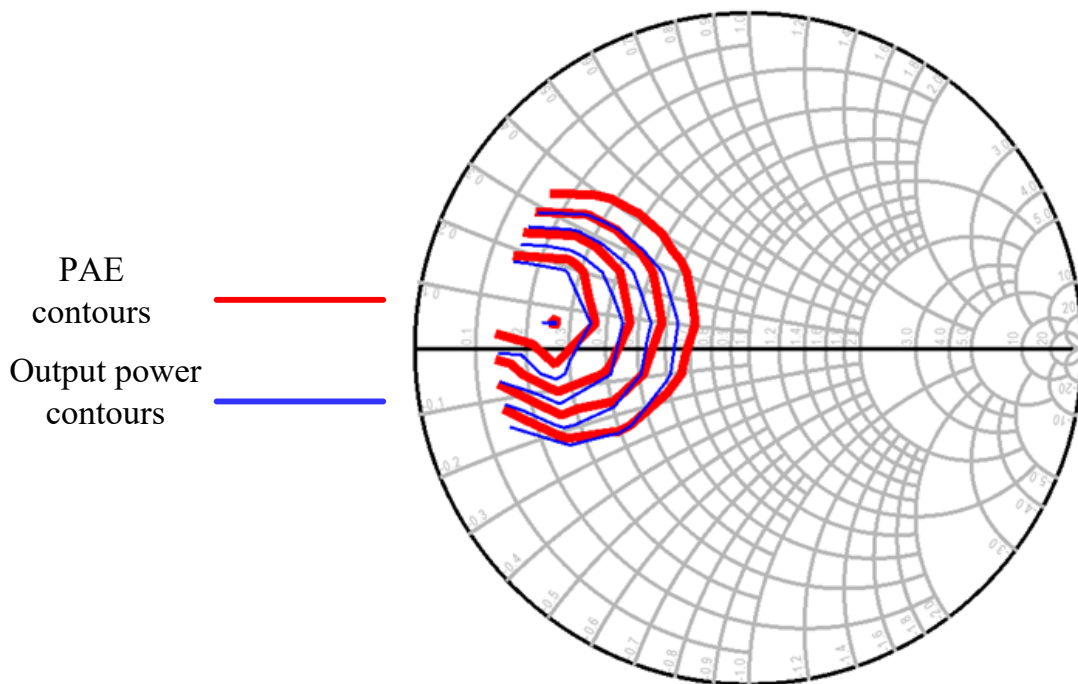


Figure 2-18. Load-pull to determine the best performance of PAE and Output Power

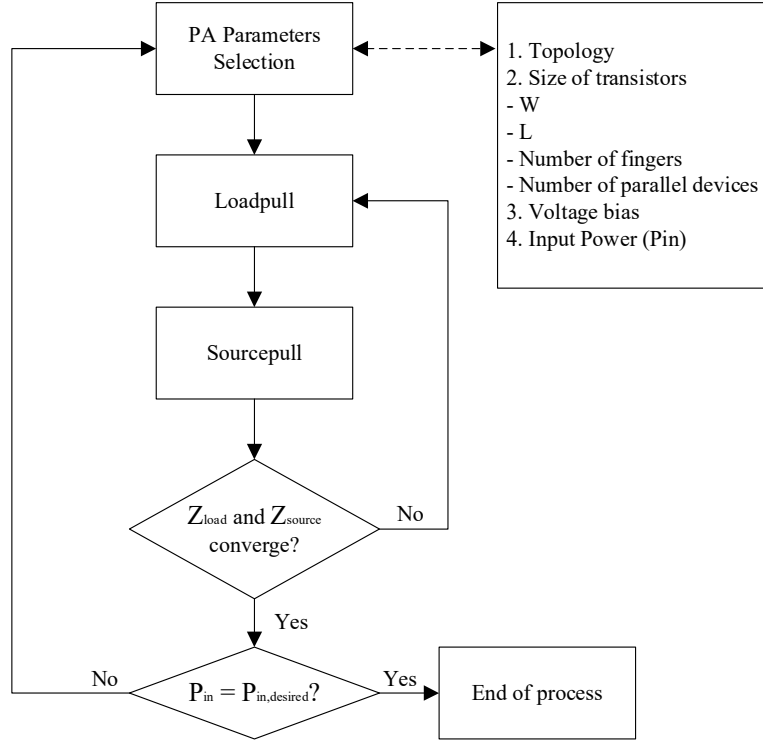


Figure 2-19. Flowchart to determine the optimal input and output impedances

2.3.4 Impact of modulated signals on linearity of Power Amplifier

The modulation scheme used in LTE standard is based on an approach of OFDM-type multiple carriers to improve the bit rate of transmission. In this case, the amplitude of the input signal of power amplifiers varies in time. To evaluate the linearity of power amplifiers, four parameters are defined as the constraints for modulated signals: PAPR (Peak to Average Power Ratio), EVM (Error Vector Magnitude), OBO (Output Back-off) and ACLR (Adjacent Channel Leakage Ratio) where ACLR is mentioned previously in the linearity of the power amplifier.

2.3.4.1 PAPR, OBO, and EVM

The time signal $S(t)$ is generated from the OFDM technique having the variable amplitude. PAPR (Peak to Average Power Ratio) is defined as the relation between the maximum power P_{max} and the average power P_{mean} of the signal in a time interval (2.6)

$$PAPR = \frac{P_{max}}{P_{mean}} = \frac{\max_{[0,T]} |S(t)|^2}{\frac{1}{T} \int_0^T |S(t)|^2} \quad (2.6)$$

Where the signal OFDM $S(t)$ is generated from the sum of several carriers.

$$S(t) = A \sum_{k=-\infty}^{\infty} \sum_{i=0}^{N-1} x_{i,k} \omega(t - kT) e^{j2i\pi\Delta f(t-kT)} \quad (2.7)$$

Where:

$\omega(t - kT)$: window function

N: number of canals

$x_{i,k}$: symbol of a subcarrier i at the moment k

Δf : distance between two carriers

A: amplitude

Output power back-off OBO is defined as the relation between the saturated power P_{sat} and the average power P_{mean} of the modulated signal.

$$OBO [dB] = 10 \log \left(\frac{P_{sat}}{P_{mean}} \right) \quad (2.8)$$

Peak back-off power PBO is employed to define the difference between the saturated power P_{sat} and the instantaneous power, or the relevant margin to P_{sat} .

$$PBO[dB] = OBO[dB] - PAPR[dB] \quad (2.9)$$

OBO, PAPR, and other linearity parameters are strictly relevant to each other, as illustrated in Figure 2-20. Hence, a significant OBO level is stringently required to ensure proper linearity for a high level of PAPR. The efficiency, however, is lower. LTE standard uses the OFDM technique; the trade-off of linearity/efficiency is consequently restrictive.

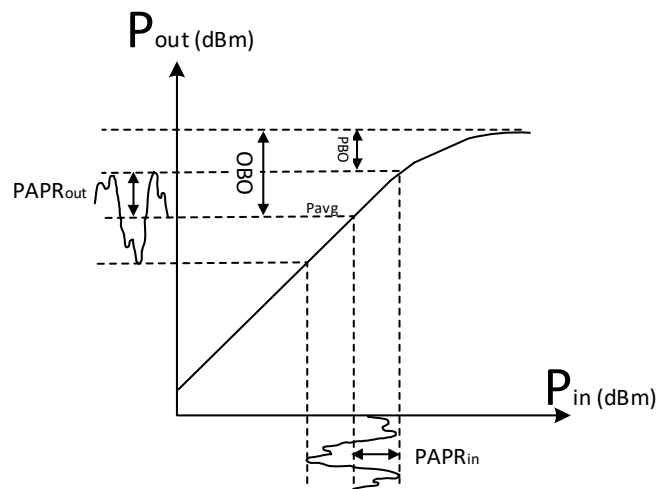


Figure 2-20. Output power versus input power for the modulated signal

EVM characterizes the performance of a transmission chain if a modulation scheme is used. This parameter is defined as the distance between the measured symbol and the wanted symbol in the constellation chart (2.10) and illustrated in percentage (%) or dB (Figure 2-21). Hence, EVM aims to determine the distortion of the measured signal. In PAs, EVM measurement is based on the comparison of the real output signal and the ideal amplified signal.

$$EVM_{rms} = \sqrt{\frac{\frac{1}{N} \sum_{k=1}^N |S_{ideal,k} - S_{real,k}|^2}{\frac{1}{N} \sum_{k=1}^N |S_{ideal,k}|^2}} \quad (2.10)$$

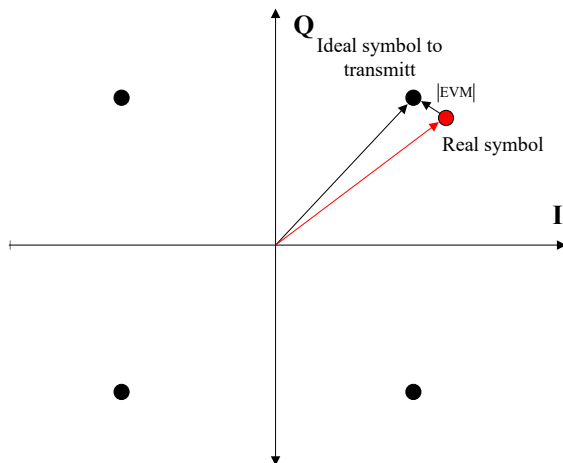


Table 2-4. EVM Specifications for LTE standard

Modulation	Required EVM (%)
QPSK	17.5
16-QAM	12.5
64-QAM	8

Figure 2-21. Definition of EVM

2.3.4.2 Uses of OFDM in 4G LTE applications

To obtain high data rate, the LTE standard uses high-order modulations: 16-QAM, 64-QAM, in Figure 2-22. Nevertheless, these modulations induce an important PAPR on the transmitted signal for PAs in comparison to QPSK.

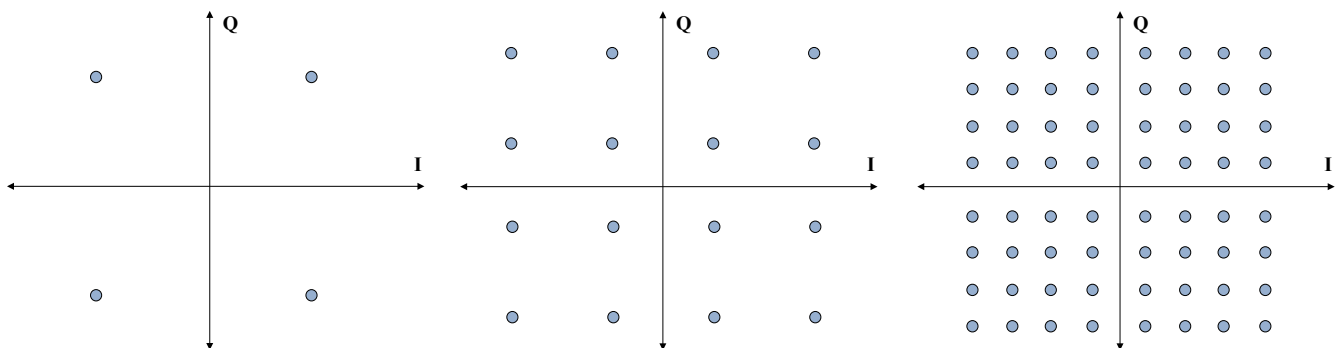


Figure 2-22. Constellations : QPSK, 16QAM, 64QAM

With the access techniques such as OFDM or SC-FDMA, the number of sub-carriers is critical; therefore, PAPR is not enough to characterize precisely the transmitted signal. It is important to take the likelihood of occurrence of the maximum values of the envelope into account. Consequently, the CCDF (Complementary Cumulative Distribution Function) curve can be used as a complement parameter. From the graph of CCDF, circuit designers can determine the probability of the signal exceeding a threshold.

Figure 2-23 depicts an obtained CCDF curves from Matlab for the OFDM technique using the modulations QPSK and 16-QAM.

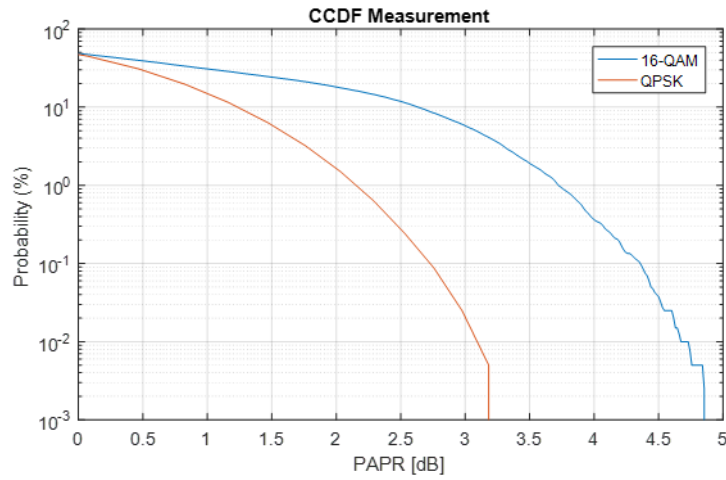


Figure 2-23. PAPR CCDF Curves

Another technique to obtain high data rate for LTE uplink is Multiple Input Multiple Output (MIMO). However, the MIMO technique requires multiple RF chains, consequently several power amplifiers, which affects the complexity of global system architecture and power consumption considerably.

2.4 Efficiency/Linearity enhancement techniques

In this section, PA enhancement techniques will be discussed. These techniques aim to improve PA performance. There is always an essential tradeoff between linearity and efficiency in conventional design methods. Hence, the primary purpose of enhancement techniques is to overcome the compromised barrier. PA enhancement techniques can be classified into two kinds: efficiency enhancement and linearization. Each kind has its advantage and drawback. In practice, circuit designers can combine two or more techniques to enhance PA performance further. It is necessary to compensate the imperfections and the errors of the manufactured technology.

The PA should be as efficient as possible and as linear as required by the communication standard in which it operates. The main problem is that efficiency and linearity place on two opposite sides of a scale: if one goes up, the other goes down. This medium is the important trade-off of RF power amplifier design. These sections below will provide an in-depth study of efficiency enhancement and linearization techniques.

2.4.1 Efficiency enhancement techniques

As noted, these are techniques used to improve the efficiency of a linear but inefficient PA. This type of enhancement techniques focuses on two aspects of efficiency: back-off efficiency and peak efficiency. In conventional PA, an efficiency PA only reaches its peak when the output power goes into the saturation region. When the output power drops, the efficiency also degrades. To control PA efficiency, designers address three parameters: the bias current,

the supply voltage, and the load impedance. Especially for the modulated signal such as OFDM, PA operates in back-off level for most of the time. Additionally, enhancing back-off efficiency can potentially improve the overall efficiency. Hence, improving PA efficiency at back-off power becomes the primary challenge and also the primary purpose.

2.4.1.1 Doherty Power Amplifier (DPA)

The Doherty Power Amplifier is invented and named after W.H. Doherty in 1936 as a technique to enhance back-off efficiency. The idea is to combine two linear PAs through a power combiner. In low power, the main power cell is active, typically working as a linear class-AB PA. When the main PA moves into the compression region, the second PA, the auxiliary power cell, is turned on to provide more output power. The critical point of the Doherty PA is designing the auxiliary PA with no consumption when it is inactive. This point ensures the overall efficiency increased in comparison to a conventional class-AB PA at the same output power level. The auxiliary cell is mainly biased in class C. The Doherty PA recently becomes one of the most attractive subjects in PA enhancement techniques thanks to its capability of improving the back-off efficiency of linear power amplifiers. By using power combining and active load modulation, DPA can maintain the efficiency near its peak value over a range of 6-dB back off. Figure 2-24 depicts the schematic of a conventional Doherty PA. Figure 2-25 shows the load modulation and the efficiency in the Doherty PA.

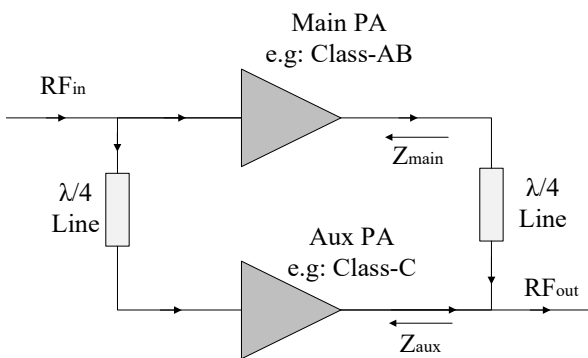


Figure 2-24. Conventional Doherty PA

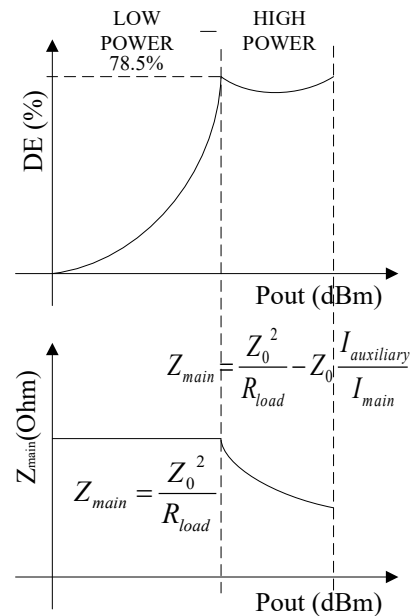


Figure 2-25. Drain efficiency and load modulation in DPA

There are several methods to perform power combiner for Doherty PA. The first and traditional one is designing $\frac{1}{4}$ wave transmission lines. This line modulates the load and changes

the main PA output signal phase by 90° . After the modulation by these lines, the efficiency can be enhanced at back-off power. This method has been implemented in the reference [5].

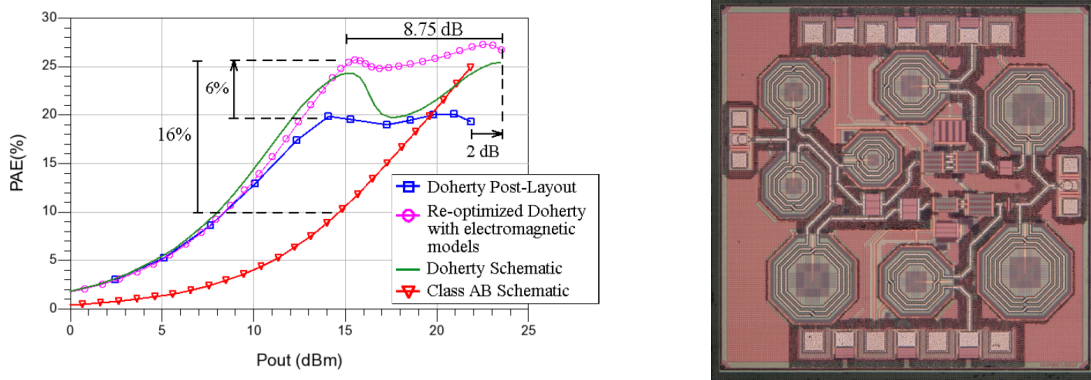


Figure 2-26. Results and circuit layout of Carneiro's work [5]

The second method to implement power combiner is using a transformer. This method takes advantage of the transformer to perform the active load modulation of the Doherty PA. In the reference [6], the PA is configured to operate in a dual mode based on the Doherty technique to further enhance the back-off efficiency range. The obvious point of his work is the symmetric hybrid transformer. This transformer is designed to suit to the output power of the main and the auxiliary power cells.

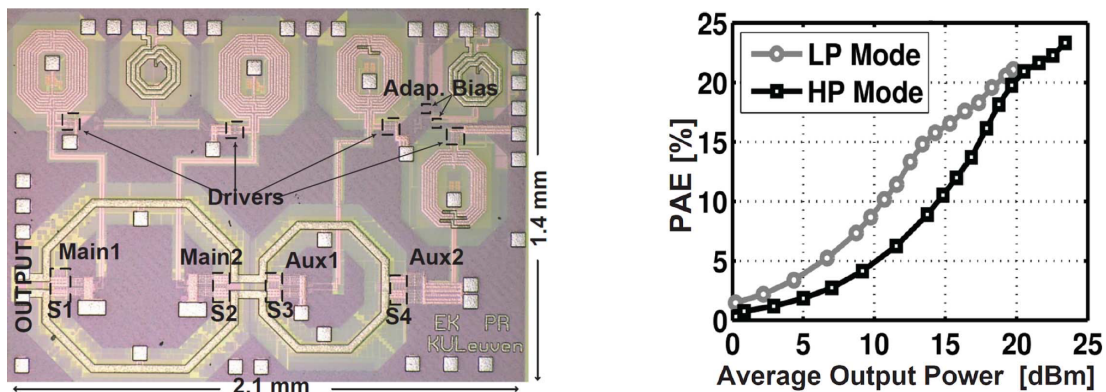


Figure 2-27. Die photo and dual-mode performances of PA [6]

The DPA introduces a good solution not as complicated as envelope tracking to enable higher efficiency levels to be achieved. However, it is difficult to maintain phase shifts of splitters over a wide bandwidth. Therefore, the DPA can only be used over a limited bandwidth. Also, the DPA exhibits a constraint about in current synchronization between the main and the auxiliary cell.

2.4.1.2 Envelope tracking

Envelope tracking is a technique used to improve the efficiency of RF power amplifiers. It is widely used in several applications, for example, in the LTE application. This application requires a high level of PAPR, so it degrades substantially the back-off efficiency. The principle

is tracking the envelope of the input signal, processing and amplifying the envelope to supply the PA instead of the constant source as in conventional PAs. Hence, this aspect helps minimize the power consumption of PAs. The typical schematic of Envelope Tracking technique can be found in Figure 2-28.a. The modulated signal is generated and sent to the envelope detection block. This block analyzes the signal and detects the envelope before transmitting to the envelope modulator block. At this step, the signal can be processed as a variable DC signal to supply PAs; its value is varied in function of the input power.

Envelope tracking technique provides high performances at all power levels and permits broadband operation. However, it requires accurate envelope signal for power supply and complicated fast-high bandwidth power supply. These blocks that occupy a significant area make the die larger.

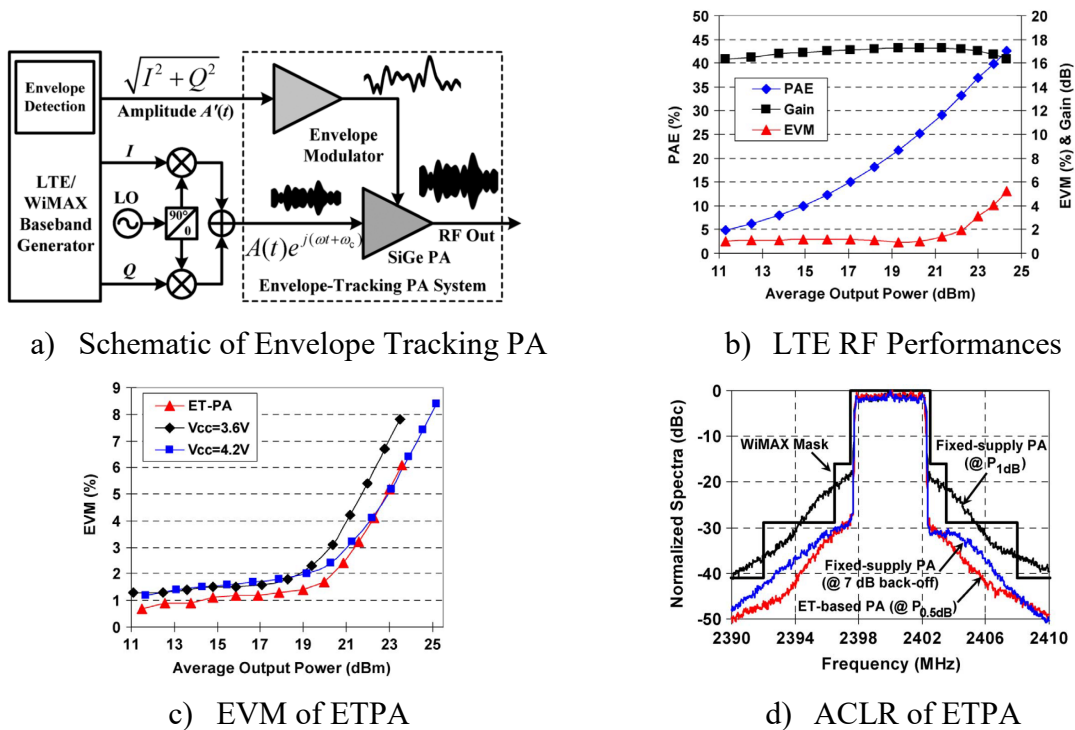


Figure 2-28. Schematic and LTE 16 QAM 5MHz results of ET-PA in [7]

2.4.1.3 Outphasing

Outphasing is an efficiency enhancement technique that was initially intended to improve the efficiency and linearity of AM broadcast transmitter [8]. This technique is also known for linear amplification with non-linear components. Outphasing technique offers an answer to the challenge of low back-off efficiency with multilevel outphasing, in which discrete amplitude levels are also used. Most of outphasing power amplifiers compose of multiple switch-mode sub power cells such as class-E or F PAs. The critical operation principle is load-line modulation by keeping PAs at peak power and producing a phase shift. This operation can improve notably efficiency but cannot deal with the requirement of high configurability of PA.

One example of outphasing PA can be found in the design of Hu [9]. The PA achieves the promising performance of efficiency and linearity.

The outphasing technique provides high efficiency solution based on active device load impedance. However, the technique using switching mode PA such class D and E is not suitable to this work that requires multi-mode operations to address the LTE standard.

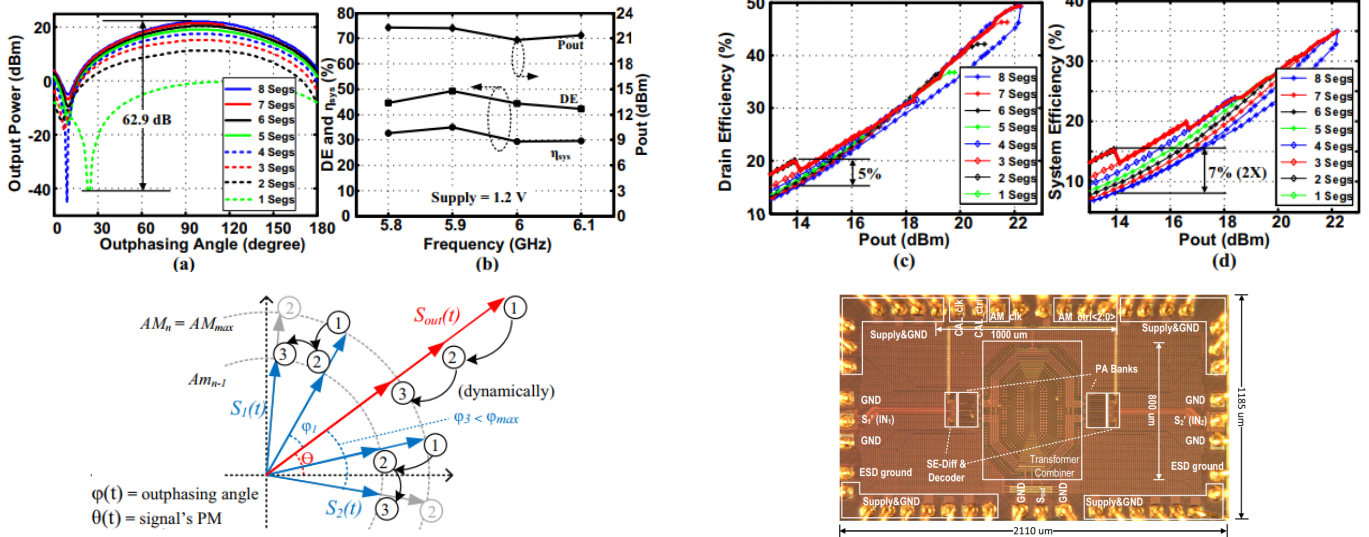


Figure 2-29. Schematic, operation principle, die photo and PA performances [9]

2.4.1.4 Power cell switching (PCS)

With this technique, the reconfiguration in power is carried out by the activation of each cell in parallel according to the level of input power. Power cell switching technique allows reducing the gain variation if the bias current is cut down. Additionally, PCS does not require to realize complex additional circuits with a broad bandwidth that affects firmly on the global efficiency as in Envelope Tracking technique.

Figure 2-30 sketches a typical schematic of power cell switching technique. Depending on applications of PA, designers can choose the suitable architecture for this technique. Power cell can be configured to be disabled by several methods to change operation modes. There are two favorite ways to carry out the deactivation of the power cell: short-circuit at output and supply control. In the reference [10], H. Ahn uses a topology including two power cells connected to multiple primary windings as in conventional power combining transformer and one power cell connected to a part of the secondary winding. In the letter of H. Ahn, PA is configured to operate in two modes: high power and low power. In low power mode, there is only one enabled power cell, PA_A. In high power mode, all of the power cells, PA_A, PA_B, and PA_C allows obtaining required performances.

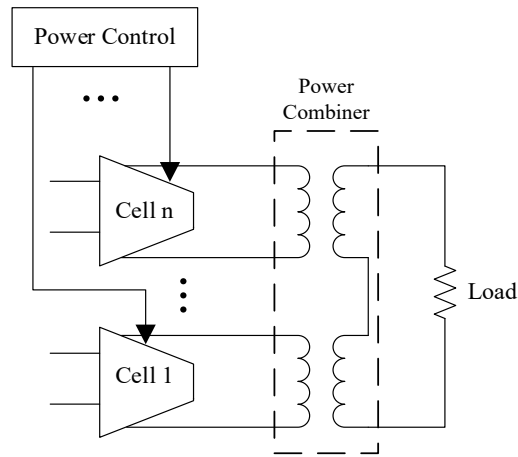


Figure 2-30. Typical schematic of Power Cell Switching technique

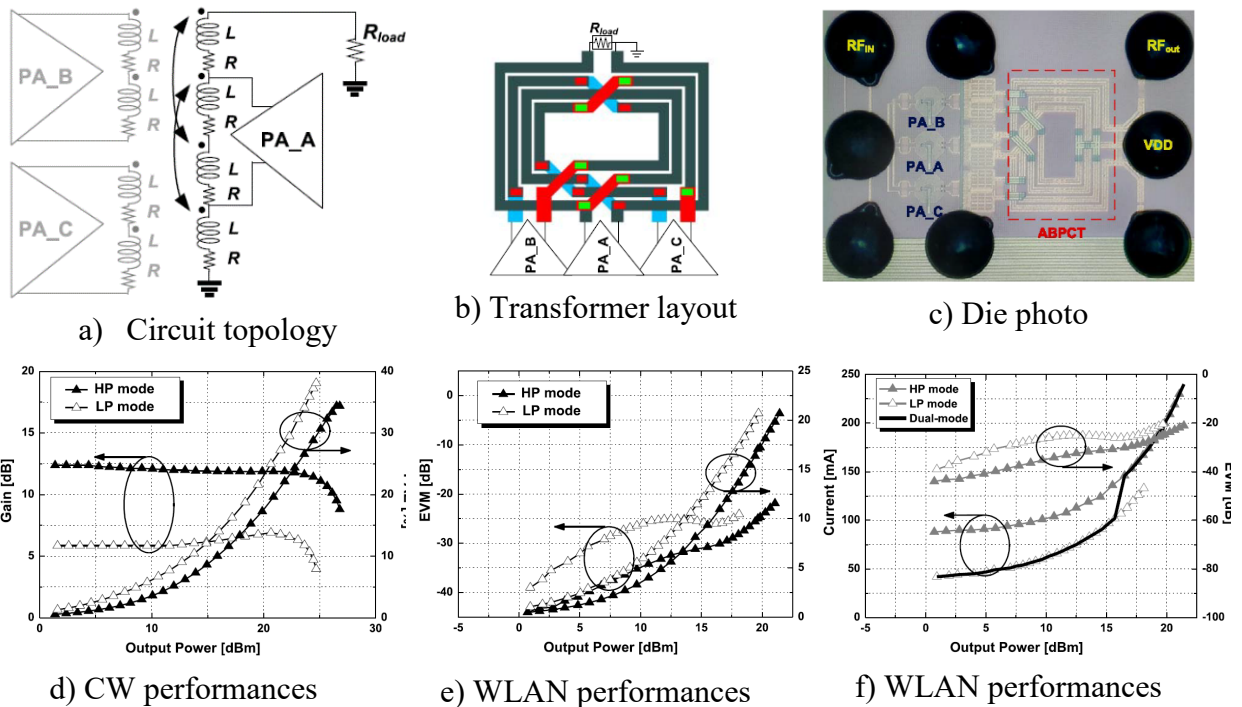
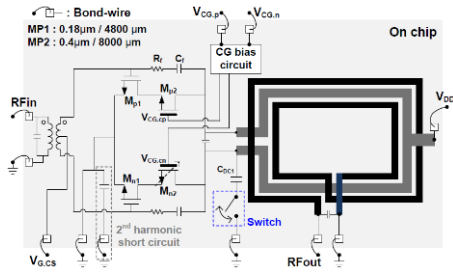
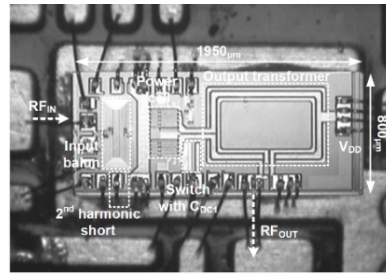


Figure 2-31. Architecture and measurement results of PA [10]

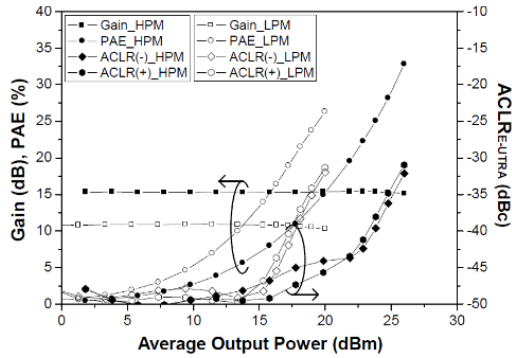
Another way to implement Power Cell Switching can be found in the paper of Yunsung Cho. In his work, PA is configured to operate in dual mode. Additionally, one switch aims to short-circuit a power cell to the ground in low power mode.



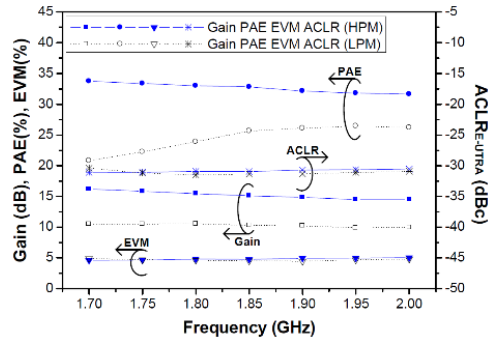
a) Schematic of PA



b) Die photo



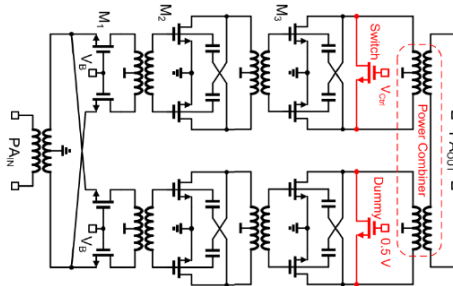
c) LTE performances



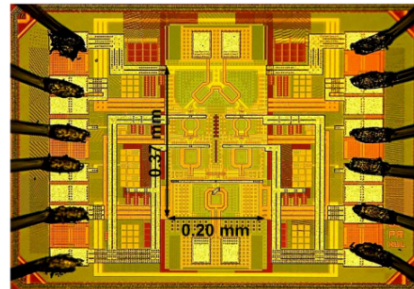
d) Performances in dual mode

Figure 2-32. Measured performances of PA in the reference [11]

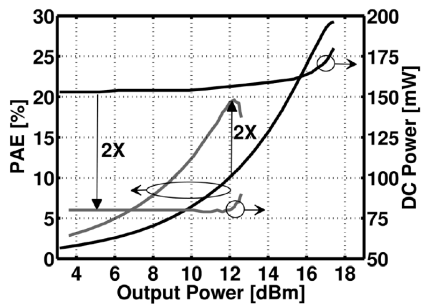
In the reference [12], the author considers two switches for power cells. These switches allow short-circuiting the output of power cell and deactivating the cell altogether. Hence, PA can toggle to low power mode.



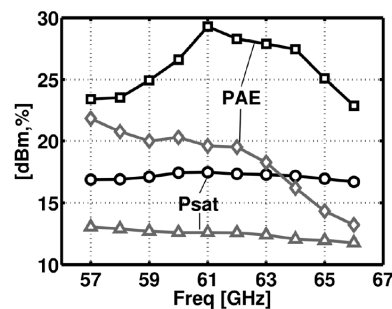
c) Schematic of PA



d) Die photo



c) CW performances in dual mode



e) Performances in dual mode

Figure 2-33. Measured performances of PA [12]

Thanks to the high reconfiguration in power and the significant efficiency enhancement, the power cell switching technique offers a promising solution for the reconfigurable power amplifier. As a result, this technique is chosen as the dominant efficiency enhancement technique for the PA design. The technique also introduces a design challenge on multiple

power cells. The transformer is needed to implement active load modulation when power cells are inactive to improve the back-off efficiency.

2.4.2 Linearity enhancement techniques

2.4.2.1 Pre-distortion

The digital pre-distortion technique is realized in the digital baseband. It is the method used over 20 years to linearize PAs and compensate distortions of the signal. Distortions can be created by enhancement techniques or the imperfection of technology. These techniques aim to improve the efficiency of PA but meanwhile introduce some distortions into the signal. The signal distortion is measured regarding errors in the signal channel (EVM) or terms of the leaked signal into adjacent channels (ACLR) [13].

The principle of pre-distortion linearization is the usage of digital pre-distorter (DPD) and the PA cascade. The DPD-PA cascade tends to combine two nonlinear systems into one direct result that allows the PA to operate closer to saturation. The objective of digital pre-distorter is to have $y(t) \approx Cx(t)$ where C is a constant.

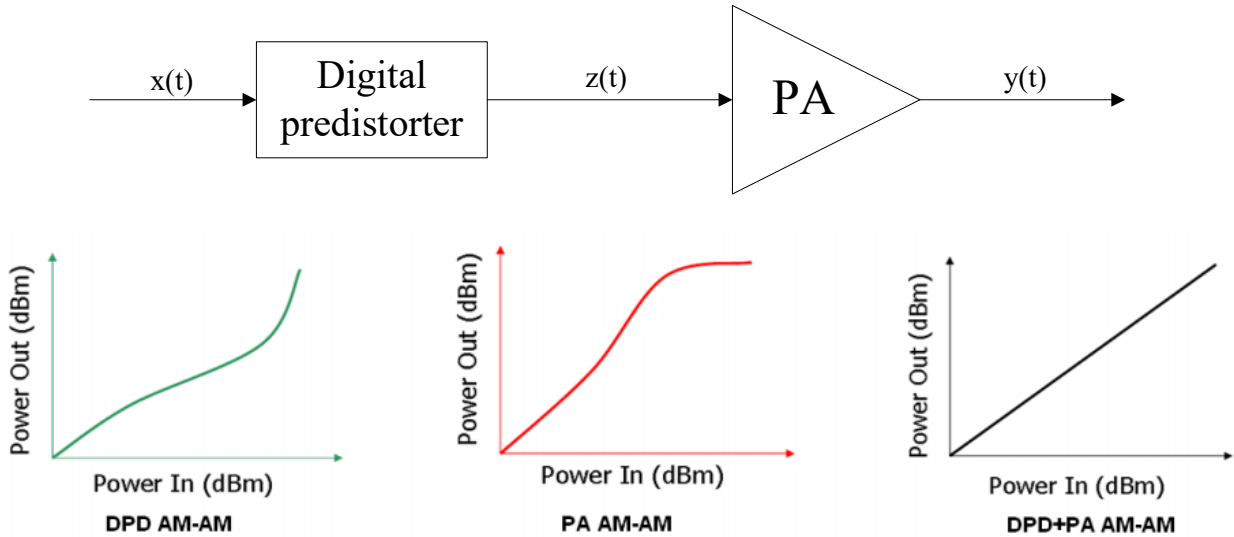


Figure 2-34. Principle of Digital Pre-distortion [14]

In LTE applications, linearity requirement is crucial for PA. Reference [15] introduces an excellent example of PA to handle this must-have requirement. The PA with the pre-distortion stage can improve linearity and somehow enhance the PA. The technique pre-distortion introduces a promising solution to linearize PAs. However, it requires an external digital pre-distortion block, which is not currently integrated along with PAs. Therefore, the pre-distortion solution is chosen in this work.

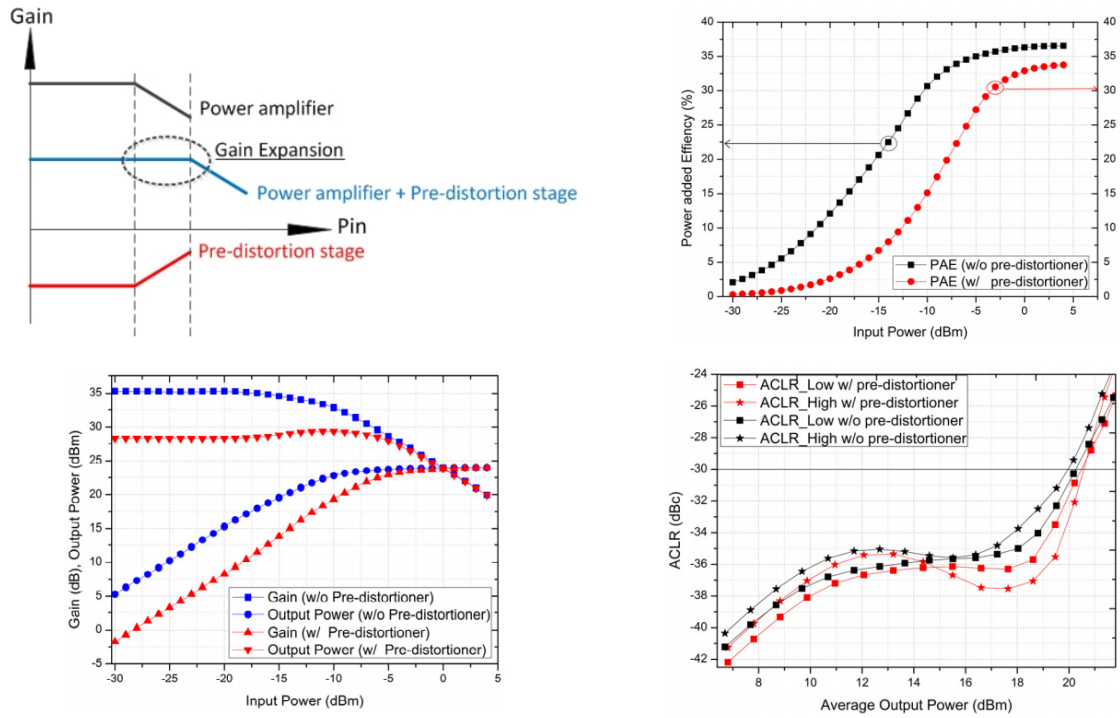


Figure 2-35. Operation principle and results in the reference [15]

2.4.2.2 Segmented bias

The principle of the segmented bias technique is using two or more transistors in cascade, which are biased differently. Figure 2-36 depicts a segmented-bias case composed of two transistors.

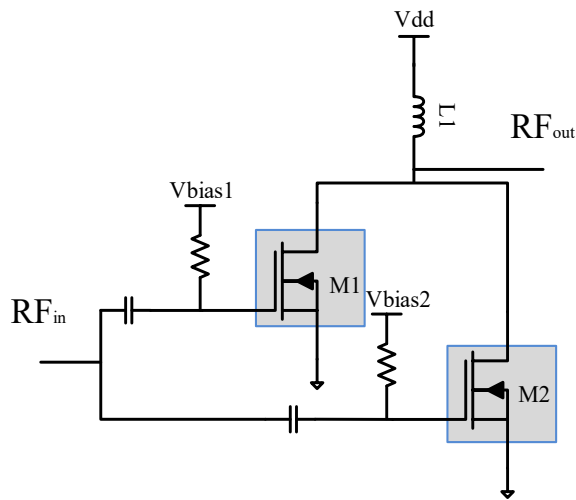


Figure 2-36. Segmented bias concept

The discrepancy between two biases of the main and the auxiliary transistors is precisely controlled to improve the compression point of PA. Figure 2-37 illustrates an example of two transistors biased separately in class AB and class C [16]. The combination of class AB and class C allows PAs to lengthen its 1-dB compression point. The synchronization of two biased can create a g_{m3} -canceled region [17], which enhances the linearity of PAs.

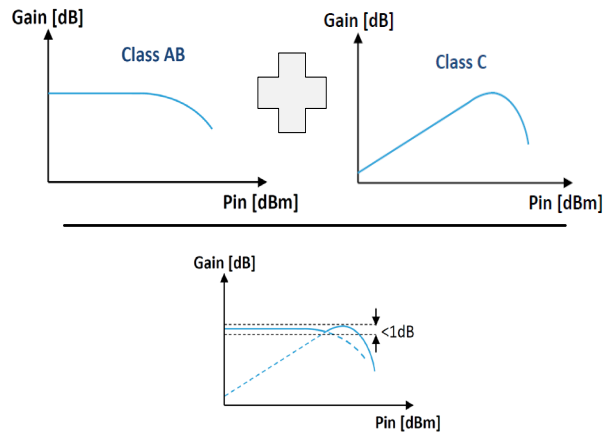


Figure 2-37. Enhancement of the compression point

Also, to satisfy the requirement of back-off efficiency, the segmented bias technique is used to swap between multiple operating modes according to the desired parameters of PAs. This convenience of the segmented-bias technique suggests an excellent solution to the problem of high configurability of PAs.

2.4.3 Proposed solution with the tradeoff of linearity and efficiency

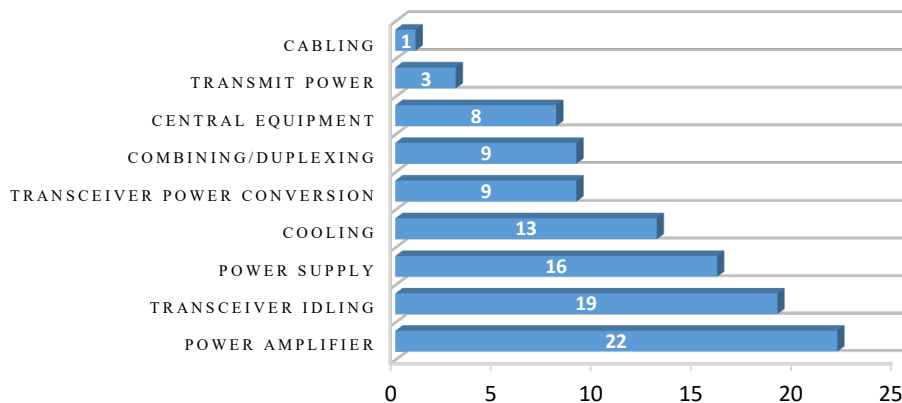


Figure 2-38. Base station power consumption breakdown

(Globecom 2010, P. Grant and S. Fletcher, MVCE doc. O-GR-0053)

Enhancement techniques are essential for radiofrequency power amplifiers to improve the performances. Linearization technique improves the linearity but also degrades the efficiency. Efficiency enhancement technique, on the other hand, can make PA more efficient but not linear enough. The question is thus how to use efficiently two kinds of enhancement techniques. The need to combine linearization and efficiency enhancement techniques is hence taken into account for RFPA. The power cell switching (PCS) technique introduces a high configurability in power and efficiency for PA to operate in multiple modes by combining output power from power cells. To push upper back-off efficiency and maintain linearity level, the segmented bias (SB) is used for each power cell. The combination of both techniques allows

PA not only to solve the give-and-take problem but also to extend the battery life of the mobile equipment. Figure 2-38 illustrates the power consumption breakdown in base radio stations, in which power amplifiers occupy the highest percentage.

2.5 65nm CMOS power amplifier for unmanned aerial vehicles

Through all mentioned-above analyses, the 4G LTE integration is an excellent solution for drones to overcome flight distance limitation. The viability of 4G LTE mobile network allows drones to fly at about 400 feet above ground level (AGL) and over a wide range. With the 4G manufacture including a large number of base stations, 4G networks help commanders localize mobile devices rapidly thanks to the algorithm of the coverage area of three base-stations. Therefore, RF front-end integration found applications in unmanned aircrafts recently. This subsection presents the use of power amplifier, one of the most power-consuming blocks of RF front-end, in 4G LTE drones applications.

2.5.1 CMOS technology

On the roadmap of silicon-based technologies in Figure 2-39, manufacture cost and surface reduction become two main goals. CMOS is hence an excellent choice to implement fully integrated radiofrequency circuits on a single chip (System on Chip – SoC) as one of the most practical technologies. This implementation allows reducing production cost significantly by shrinking necessary components on the printed circuit of mobile terminals.

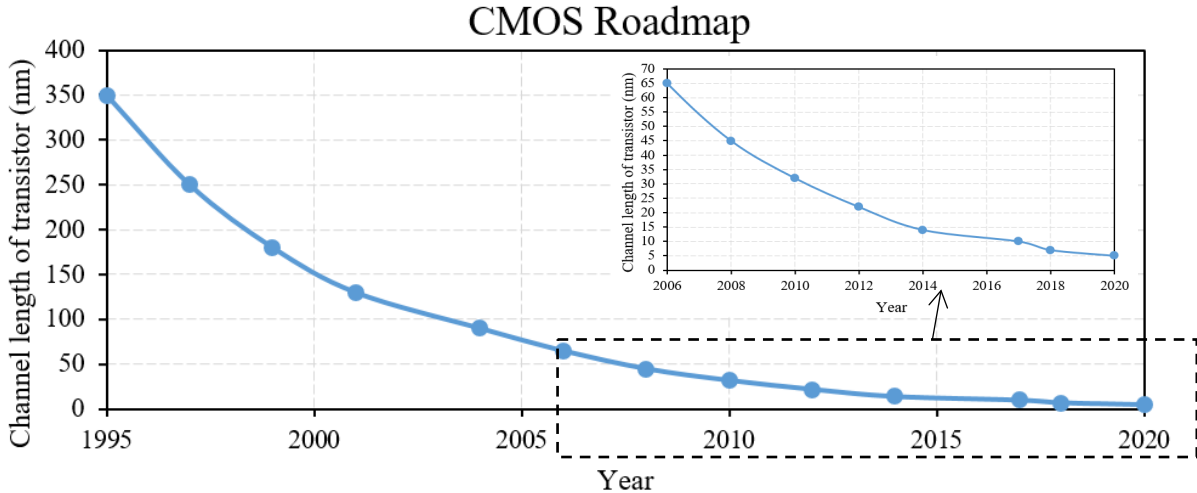


Figure 2-39. CMOS Roadmap

In recent years, MOS transistors’ performances have been improved promptly because of the high demand for integrated products. The channel length of transistors is considerably scaled down from 180-nm in 2000 to 7-nm in 2017/2018 and so far 5-nm in 2020. With the miniaturization of transistors, the frequencies f_T and f_{max} are always being pushed up. ITRS

(International Technology Roadmap for Semiconductors) predicts that the transition frequency of transistors f_T will exceed terahertz in 2019 [18].

Most of integrated building blocks such as digital, RF or mixed-signal blocks are implemented successfully in CMOS substrate. Depending on the demand for integration level and production expense, PAs could be integrated into commercialized products. System on a chip of Wi-Fi is a typical example; the chip does not require a high level of output power but does need a fully integrated system to reduce cost. Nonetheless, the PA for cellular applications, which is the most power-consuming block, is still designed separately from the other blocks. For RF mobile terminals, the watt-level output power is a necessary characteristic. Integrated PAs tend to be implemented on expensive substrates namely GaN or GaAs due to its high performance of power and efficiency. However, with low cost and high capability of integration as in Table 2-5 CMOS PAs are always in high demand.

Table 2-5. Silicon technology comparison

Technology	+	-	Comments
RF CMOS	<ul style="list-style-type: none"> • Mainstream CMOS • Lowest wafer cost (at same lithography node) • SOC integration with RF, ADC, digital baseband, memory • Platform IP availability 	<ul style="list-style-type: none"> • Low breakdown voltage • Low Tx output power/efficiency • Low self-gain • Poor device isolation • High NRE at adv. lithography 	Best choice for price sensitive and lower performance (short range) applications such as user equipment transceivers
PD-SOI	<ul style="list-style-type: none"> • FEM + RF integration • Device stacking with higher voltage and power handling vs. CMOS • Great f_T/f_{MAX}, dynamic power, Rx Noise Figure • High resistivity substrate 	<ul style="list-style-type: none"> • SOI substrate cost adder (vs. same node CMOS) • Lower logic density for SOC integration 	Good cost/performance tradeoff. Die-based cost can be lower than CMOS for transmitted power
FD-SOI	<ul style="list-style-type: none"> • High self-gain vs. CMOS • High f_T/f_{MAX} • Lowest voltage / lowest power operation with unique back-gate bias capability • High-density SOC integration • Low mask count 	<ul style="list-style-type: none"> • SOI substrate added cost • High NRE (most advanced lithography) • Base models less mature • Device stacking more complicated and less efficient than PD-SOI 	New capability in industry with back-gate bias → potential for novel architectures and reconfigurable operation
SiGe	<ul style="list-style-type: none"> • Optimized for mm-Wave • Best f_T/f_{MAX}, phase noise • Best transmitted output power and efficiency per element • Lowest loss metal stack • Lowest NRE 	<ul style="list-style-type: none"> • Highest wafer cost/mm² • Not suitable for SOC integration with ADC, baseband 	Best choice for high performance and high transmitted power (more extended range) RF applications

The 65-nm technology is firstly introduced in 2005 by TSMC and passed to product certification in the following year. Among CMOS nanometer technologies, 65-nm technology is used widely in RF front-end modules. The 65-nm low-power CMOS technology of TSMC, which allows multiple supply voltages for core and I/O, is developed for logic, mixed-signal and RF circuits. The process features a high-resistivity epitaxial substrate, shallow trench isolation (STI), two gate oxide options (for 1.2 and 2.5 V operation), nickel-silicide low-resistance n+ and p+ polysilicon and diffusion areas. Two kinds of transistors, nMOS, and pMOS, are available with several different threshold values. High-voltage 5V-drain-tolerant devices are optional. The technology offers a metal scheme “Back End of Line” with three to nine copper metal layers for interconnection plus one top aluminum layer for wire bond/flip chip pad, pad redistribution layer and laser fuses. In this work, the circuit is implemented on the 65-nm CMOS technology with the low-power mixed-signal and RF option. It provides a metal scheme with six intermediate metals, one thick metal and one ultra-thick metal along with an aluminum layer. Options for metal-insulator-metal capacitors and ultra-thick-metal high-Q inductors are available. Thin metal layers use low-k dielectric. Figure 2-40 sketches the metal scheme of the 65-nm CMOS technology.

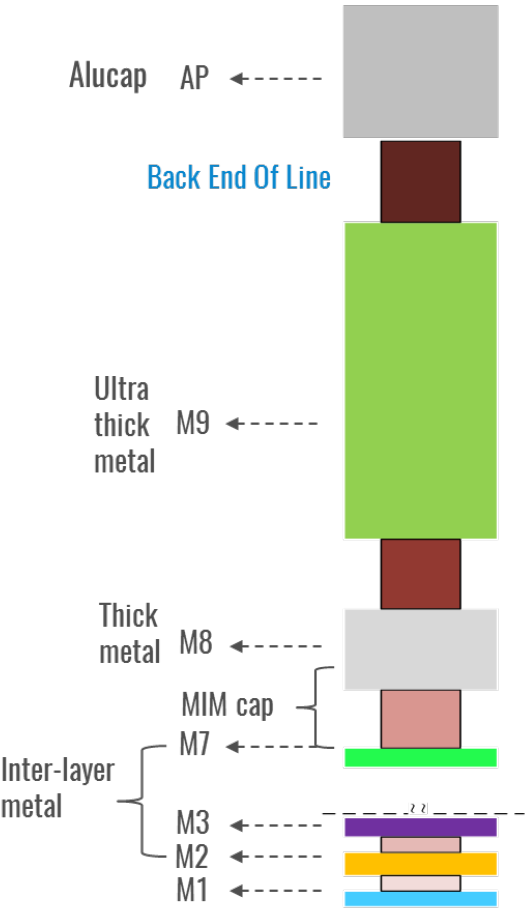


Figure 2-40. Back End of Line scheme of 65-nm CMOS technology

2.5.2 State of the art

Table 2-6 presents the state-of-the-art of integrated PA performances for LTE and WLAN applications in the frequency range of 2.5GHz. The works presented in this table use efficiency-enhancement techniques namely Doherty, power cell switching to improve the efficiency of PA. The FoM (Figure of Merit) (2.11), which is defined by ITRS, evaluates the trade-off of linearity and efficiency of PAs.

$$FoM = P_{sat} * PAE_{peak} * Gain * Freq^2 \quad (2.11)$$

Where: P_{sat} is the saturated power at PA output.

PAE_{peak} is the maximum efficiency of PA.

$Gain$ is the power gain of PA.

$Freq$ is the operation frequency of PA.

Table 2-6. State-of-the-art

Ref	Process Si	Topology	Apps	Nb of cells	Freq [GHz]	Vdd [V]	P_{sat} [dBm]	P_{1dB} [dBm]	Gain [dB]	PAE_{max} [%]	$PAE@$ OBO	I_{dc} [mA]	FoM ITRS [W.GHz ²]
[6]	40nm CMOS	Doherty + Mode switching	LTE	2	1.9	1.5	28	26	29.3	34	25.5@6	158	346.92
[19]	130nm CMOS	Matching network	WiMAX	1	2.5	3.3	25.5	21.4	31	32	10@6	298	357.34
[20]	180nm CMOS	Mode switching	WLAN	2	2.4	5.6	28	26.5	23	27	22.5@6	-	81.57
[21]	180nm CMOS	Power cell switching	WLAN or WiMAX	3	2.5	3.3	31	25.5	31.3	34.5	22.5@5	590	1464.73
[22]	65nm CMOS	LC Network	WLAN	3	2.4	3.3	31.5	27.5	32	25	14@6	-	1343.23
[10]	40nm CMOS	Power combining transformer	WLAN	3	1.75	2.8	26.8	25	12.5	34.4	14@6	248	5.12
[23]	55nm CMOS	Mode switching +Linearizing Body Network	WLAN	1	2.45	3.3	24.3	22	30.7	16	10@6	150	123.96
[24]	65nm CMOS	Power cell switching	LTE	4	2.5	3.8	30	28	26.2	32	12.5@6	600	333.49
[25]	HBT-pHEMT	Bias control	LTE	2	0.84	3.4	29	26	28.4	42	22@6	-	193.87
[26]	0,11um CMOS	Two Stages	LTE	1	1.95	3.4	30	28	17	42	20@6	-	41.04
[5]	65-nm CMOS	Doherty	LTE	2	2.535	3.8	24	18	15	27	26@8	-	5.43

Among state-of-the-art power amplifiers, reference [21] demonstrates the highest FoM factor of 1464.73, which means the efficiency-linearity tradeoff. It is important to note that the saturated power on silicium is frequent at watt level. The highest efficiency that a power amplifier obtained is shown in the reference [26] with 42% of PAE, in which the PA is built with only one stage; therefore the power gain is only 17 dB.

2.5.3 Specifications of design

The 4G LTE reconfigurable power amplifier requires addressing the specification of the LTE uplink in band 7. All required performances of the 2.5-GHz fully integrated CMOS 65nm 4G LTE power amplifier are summarized in Table 2-7.

Table 2-7. Fully integrated 4G LTE PA specification summary

LTE specifications - 3GPP TS 36.101 version 9.12.0 Release 9 Uplink (UL) operating band 7 - BS receive - UE transmit	
Parameters	Specifications
Frequency Band	2.5 GHz → 2.57 GHz
Modulation	QPSK, 16-QAM, 64-QAM
Bandwidth	20 MHz
Required maximum output power	> 27 dBm
Gain	20 dB
PAE (max)	> 27 %
PAPR	8 dB
Supplied voltage	3.3V

2.6 Conclusion

As a first step, this chapter highlights the rapid evolution of wireless communication systems. To transmit high data rate up to 100 Mbps, the LTE standard uses high-order modulations (16-QAM and 64-QAM) and access technique (OFDMA, SC-FDMA). Consequently, it requires an essential dynamism for the transmitted signal and imposes more constraints on PA design.

The fundamental objective of this work is to implement a low-cost low-power multi-mode PA for LTE applications in drones. The CMOS technology is chosen as a low-priced solution for this PA. In the coming years, the PA aims to be integrated, on the same die, with other blocks as a transceiver. The choice of CMOS technology is beneficial to digital blocks, but it imposes critical technological constraints on analog blocks and especially on the RF power amplifier. Hence, a suitable architecture must be considered not only to respond to these

technological constraints but also to achieve high performances. Moreover, electrical parameters such as power consumption, die size and LTE's specifications require being taken into account for circuit design.

In 4G standard, the implementation of efficiency enhancement technique is essential due to the high level of the PAPR ratio of LTE signal. A thorough study is investigated to choose the most suitable technique for this work. The combination of the segmented bias technique and the power cell switching technique proposes a promising solution for the reconfigurable power amplifier to address technological and electrical constraints. Chapter 3 will be dedicated to the design of integrated passive elements in CMOS technology.

3 PASSIVE DEVICE CHARACTERIZATION

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Chapter 3 presents the critical steps to design and optimize passive devices for PA design as in the first part. The second part details radiofrequency phenomena and approximation that requires being taken into account during simulation and measurement procedures. The third part demonstrates the design process of the transformer. Last but not least, RF pads are detailed with their characterization and localization.

3.1 Design flow

Active and passive circuits are playing an essential role in radiofrequency, microwave and millimeter wave applications. A passive device is defined as a component having no added energy to the signal, the power at the output is thus smaller than or equal to the one at the input. As defined with the energy conversation and thermodynamics, a passive device does not oscillate. An active device is referred to the components with the output responses affected by external energy. On the contrary, an active device can oscillate, for example, power amplifiers or oscillators.

The previous chapter overviews the design of the radiofrequency power amplifier in CMOS technology. This work focuses on PA designed with the 65nm CMOS technology provided by TSMC. The 65nm CMOS Design Kit (DK) contains a library of passive and active devices models that supports RF applications. This library does not include transformer models. Consequently, the initial purpose is to develop a modified and improved DK library with included transformers to adapt to the architecture of the reconfigurable power amplifier. Figure 3-1 illustrates the design flow process for PA design.

The 65nm DK composes of simulated models and implemented components including their layouts. DK components, active and passive devices, require being verified in Cadence for PA design. The passive devices are re-simulated in the 3D electromagnetic simulator, Agilent Momentum to adapt to PA design. As aforementioned, PA design requires transformer models due to its absence in DK library. Among passive components, the transformer design is one of the most time-consuming tasks with a great deal of design, simulation and optimization loops. The necessary parasite components will be extracted to characterize and model appropriately with large-signal and small-signal performances. The layout improvement is also carried out along with the model extraction.

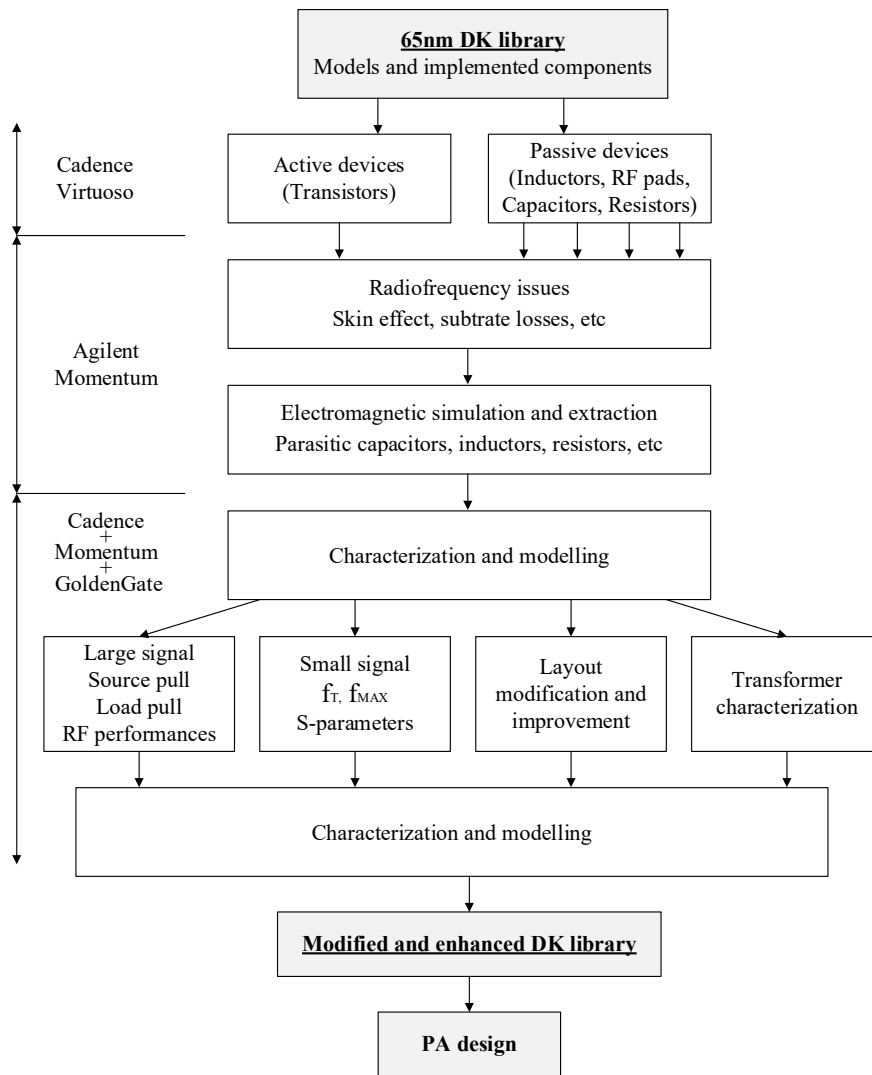


Figure 3-1. Design flow process for passive device characterization

3.2 Parasitic phenomena in radio frequency

In high frequencies, the current distribution on a conductor is changed due to eddy currents in the metallization, also known as skin and proximity effects, current constriction and current crowding. This subsection introduces some of the fundamental parasitic phenomena affecting the performances of integrated circuits.

3.2.1 Skin effect

At any given frequency, alternating current tends to follow the path of low impedance. Currents frequently conduct at the surface of conductor since magnetic fields penetrate the conductors and produce opposing electric fields within the area of conductors [28]. The current density increases and more energy is converted into heat if the cross-sectional area of the conductor decreases. Concurrently, the fact that the skin depth becomes narrow causes the effective resistance of the conductor to increase at higher frequencies. For an isolated

conductor, the magnetic fields self-create inside the conductor. This effect is known as skin effect. Figure 3-2 illustrates skin effect on a metal path.

The skin depth δ can be calculated as:

$$\delta = \frac{1}{\sqrt{\sigma \cdot \mu_0 \cdot \mu_r \cdot \pi \cdot f}} \quad (3.1)$$

With σ : Conductivity of the conductor (S/m),

μ_0 : Permeability of free space [H/m],

μ_r : Relative magnetic permeability of the conductor,

f : Frequency of the current [Hz].

The effective resistance R is also determined as below:

$$R \approx \frac{L}{\sigma} \cdot \frac{1}{2\delta(T + W - 2\delta)} \quad (3.2)$$

With σ : Conductivity of the conductor [S/m],

L : Length of conductor [m],

δ : Skin depth (m),

W : Width of conductor [m],

T : Thickness of conductor [m].

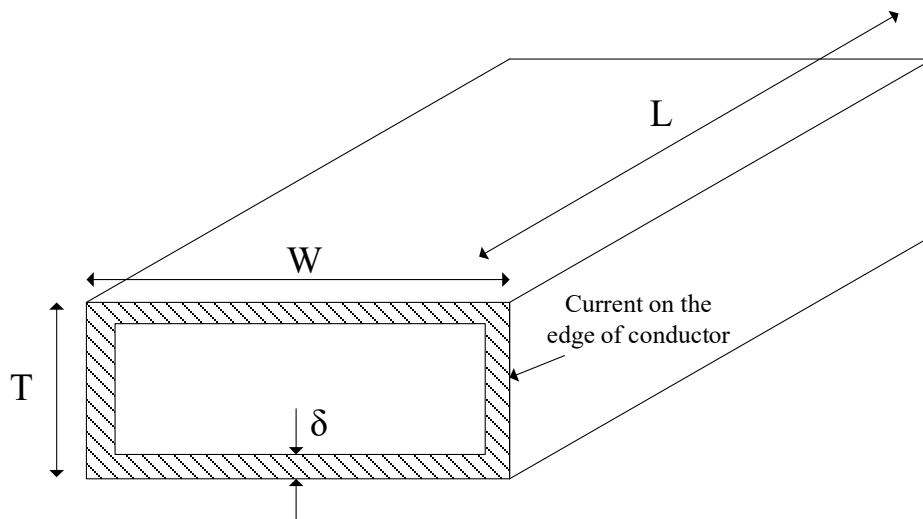
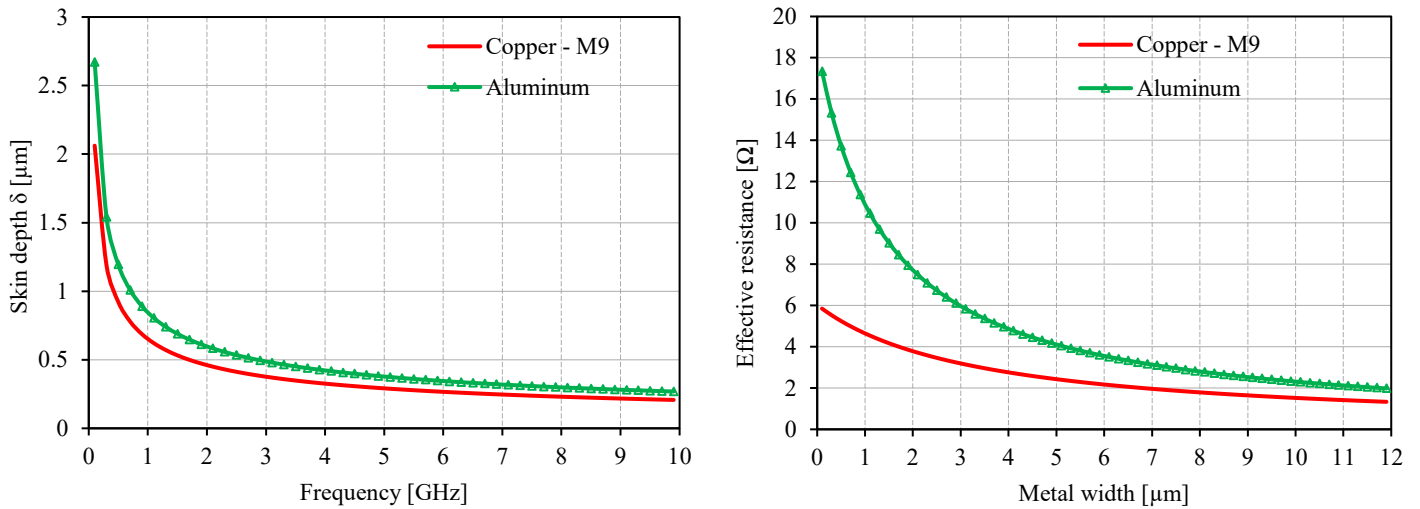


Figure 3-2. Skin effect on a metal path [29]



a) Skin depth for copper and aluminum cases b) Effective resistance to copper and aluminum cases

Figure 3-3. Impact of skin effect for two 1mm-long pitches in copper level M9 and aluminum in CMOS 65nm technology

Figure 3-3 illustrates the impact of skin effect on metal pitches designed in the CMOS 65nm technology. As shown in Figure 3-3.a, the skin depth is below 0.48 μm (for the copper level) or 0.6 μm (for the aluminum level) in radio frequencies. A simple design of two same-length one-millimeter pitches in the top metal and aluminum provides the effective resistances created by the skin effect. The effective resistances are below 6 Ω (for the top metal) and below 17 Ω (for aluminum) for all widths.

In a multi-conductor system, the magnetic field can be expressed in two terms, “the self-magnetic field and the neighbor-magnetic field”[28]. Hence, the resistance increase of a conductor must be determined by two effects, the skin effect for the self-magnetic field and proximity effects as the effect from neighbor conductors. The impact of the neighbor conductor intensifies the magnetic field around a given conductor. As a result, the effective resistance will be enlarged. This scenario is a typical case found in a spiral inductor. Otherwise, the effective resistance will decrease in case of a transformer. The changing magnetic field in both effects created by the alternating current induces opposing eddy currents. Two effects, the skin effect and proximity effects, will be further discussed in the subsection 3.3.3 to explain loss reasons in integrated circuits.

3.2.2 The ground plane and the return path

A low-resistive ground plane is required for a correct operation of an amplifier. In radio frequency and especially millimeter wave, parasitic inductances and resistances degrade transistor gain and modify the function characteristic of passive devices. Moreover, the various possible return paths affect the model precision of circuits. Therefore, ground planes are

designed by stacking metal layers to reduce these parasitic inductances and resistances. Figure 3-4 illustrates a design of ground pattern in 3D view and cross-section view. Regarding to design ground pattern, circuit designers need to consider two parasitics in series about inductances and resistances in a ground plane, as shown in Figure 3-5. The electromagnetic simulation in Momentum, which is discussed further in the next section, allows simulating all parasitic influences on circuits.



Figure 3-4. Ground pattern in 3D view and cross-section view

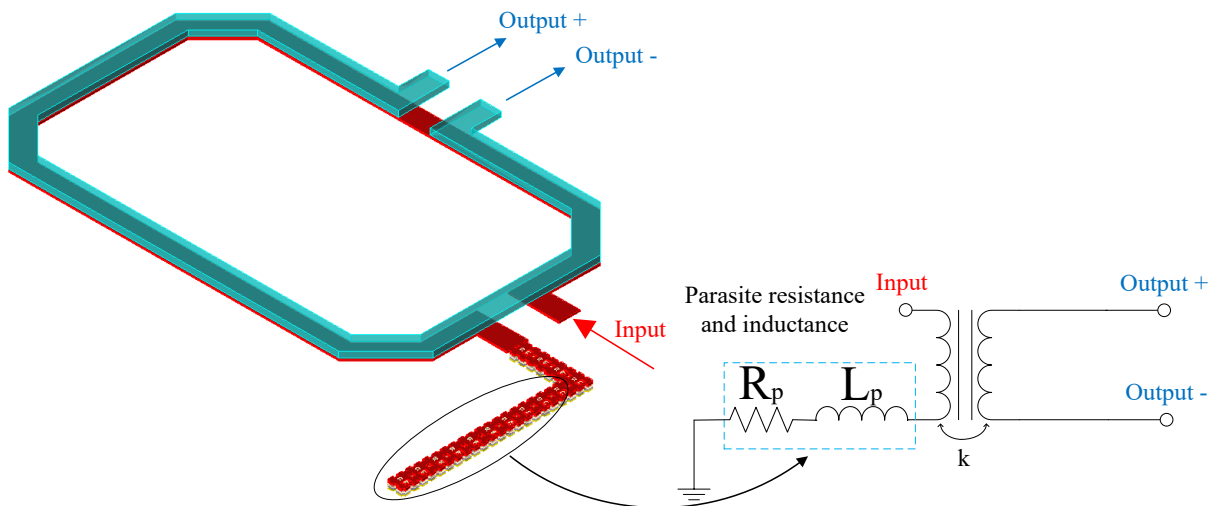
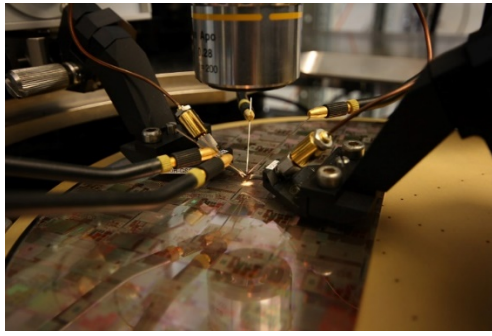


Figure 3-5. Design of a ground plane for a radiofrequency transformer.

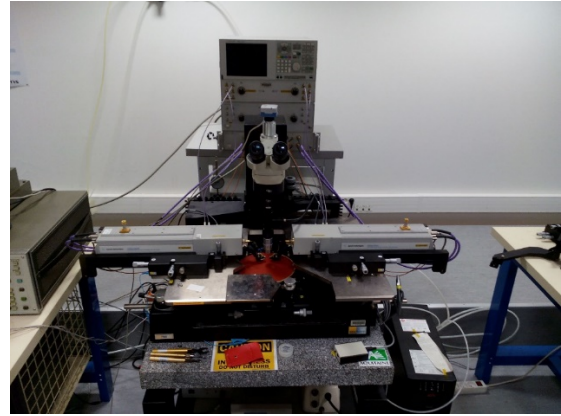
3.3 Power combiner design and optimization

3.3.1 Measurement platform

The NANOCOM platform is available in the IMS Laboratory to perform RF and mm-wave measurements. The platform can support on-wafer measurement and model characterization. Along with the test benches for source-pull, load-pull, multi-harmonics, spectral analysis, and noise measurements, there is also a test bench for S-parameters up to 110 GHz. This test bench consists of an Agilent E8361 vector network analyzer (VNA) and the corresponding Ground-Signal-Ground (GSG) or Ground-Signal-Ground-Signal-Ground (GSGS) test probes. The configuration is suitable for the measurement of two-port devices. Figure 3-6 illustrates the available test bench.



a) On-wafer measurement



b) Characterization platform

Figure 3-6. Microwave and millimeter wave characterization platform

The calibration procedure is performed in a step-by-step procedure. In microwave and millimeter-wave field, the incident and reflected waves decide the calibration computation at a given reference plane. This computation allows calibrating precisely the VNA at probe terminals. There are several calibration methods. The primary objective is to estimate a two-port error model. The most popular methods are Line-Reflect-Match (LRM) [30], Through-Reflect-Line (TRL) [31] and Short-Open-Load-Thru (SOLT) [32]. Each method, which uses a non-ideal test structure to compensate the error from the matrix calculator, has its advantages and drawbacks. TRL calibration requires different line lengths to cover a frequency range. The SOLT technique adopts only one T-line structure to have an acceptable estimation of error matrix in broadband [33]. In this method, the short and open impedances allow estimating the parasitic inductance and capacitance. Figure 3-7 depicts the photographs of four test structure dies [34].

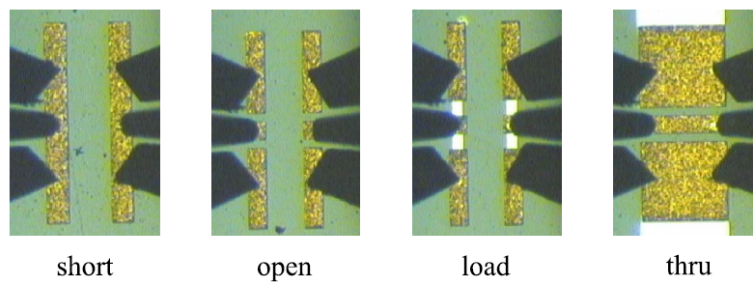


Figure 3-7. SOLT method circuits

3.3.2 Types of power combiner

3.3.2.1 Current combiner

Current-based combiners are the most classic architecture to implement the power-combining design. The first introduced model is the Wilkinson power combiner, which takes its name from Ernest Wilkinson. This electronics engineer initially developed his idea in the 1960s and published on Transaction on Microwave Theory and Techniques under the title: “An

N-Way Power Divider.” An ideal Wilkinson combiner combines two or more in-phase input signals to provide an output signal with a higher power level and a different phase.

Despite the concept of Wilkinson for N-way systems, it is easier to analyze how the power combiner works in two-way systems. The Wilkinson combiner uses quarter-wave transformers from two separate ports to the unique one, as shown in Figure 3-8 or utilized in Wilkinson concept for power splitter [35]. Due to the mismatch between ports, a resistor is introduced in the input of power combiner. This resistor allows matching two data and providing isolation. In case of a lossless network, the resistor does not dissipate any power. In practice, there are some existed losses, but low enough.

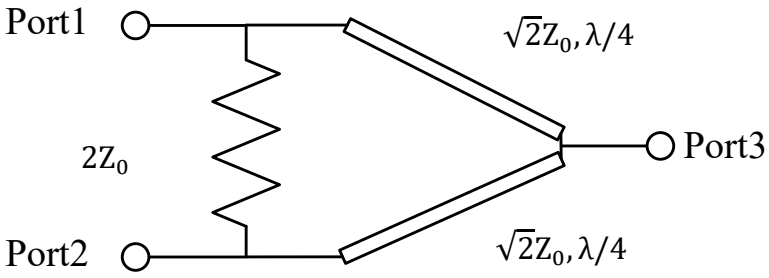


Figure 3-8. A two-way Wilkinson combiner

The quarter wavelength transmission line decides the size of the combiner. Its length depends on its center operating frequency. The size of a power combiner can reach enormous at low frequencies. Therefore, in low frequencies, circuit designers tend to implement the equivalent lumped-component Wilkinson combiner or splitter. A pi-network, as shown in Figure 3-9, can behave electrically in the same way as a transmission line. An example using lumped components of Wilkinson combiner is illustrated in Figure 3-10.

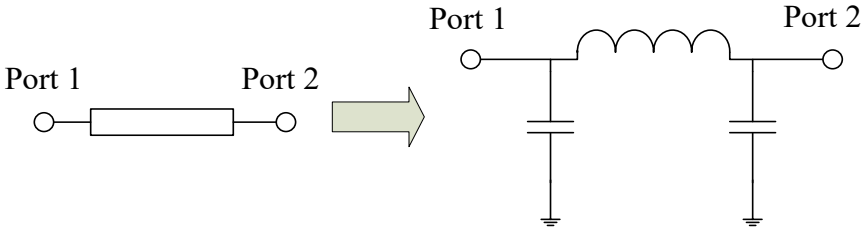


Figure 3-9. Equivalent lumped-component model of a quarter-wavelength transmission line

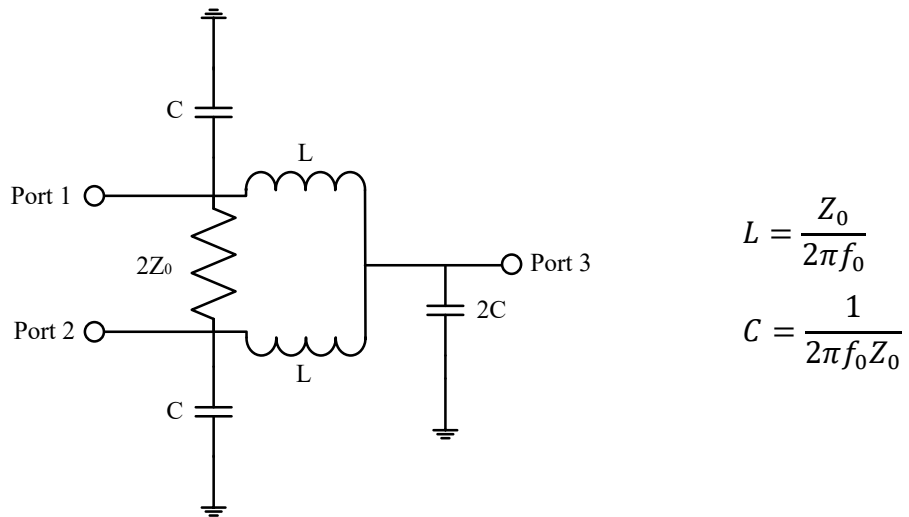


Figure 3-10. A two-way lumped-component Wilkinson combiner

The Wilkinson inventor does the first implementation of combiner/splitter in the 1960s. After that, this type of combiner has emerged into printed circuit boards (PCB) and recently into integrated circuits (IC). Thanks to its promising performances regarding insertion loss, the Wilkinson combiner proposes a prominent solution to PA designers for output power enhancement. Additionally, this combiner also poses challenges for limited bandwidth and area occupation. Along with the massive number of Doherty PA implementations, the Wilkinson-splitter type has been extensively deployed into such power amplifier as a critical block. In the reference [36], the authors use the lumped-component Wilkinson splitter to distribute power homogeneously to main and auxiliary power cells.

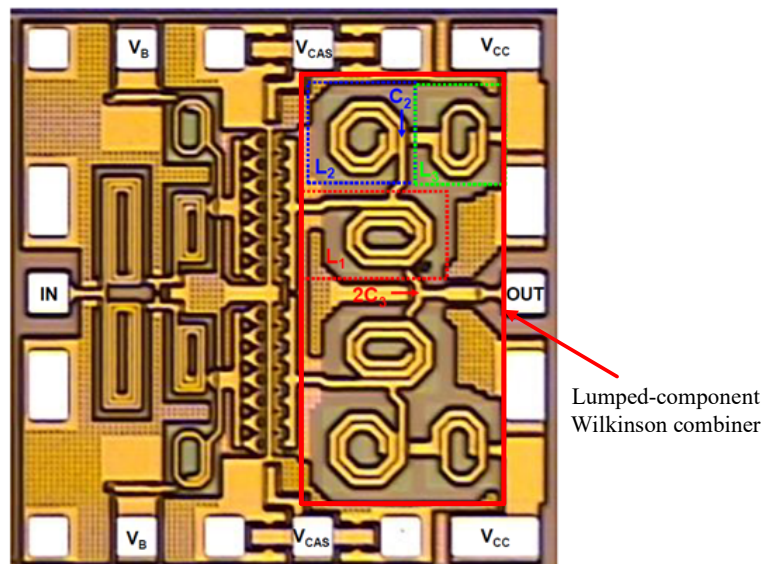


Figure 3-11. PA using a low loss lumped-element Wilkinson power combiner [37]

Figure 3-11 is an example of the use of the Wilkinson combiner in power amplifier from Inchan Ju and John Cressler [37]. The work introduces a lumped-element power-combining network.

3.3.2.2 Couplers

The second type of power combiner presented in this chapter is the coupler. While current-based combiners rely on incorporating the in-phase input signals and outputting the reverse-phase signal, couplers perform the signal combination in quadrature phase (90° phase difference). The conventional architecture of couplers consists of four ports. A coupler is initially implemented by allocating two lines close enough [38], as shown in Figure 3-12. Energy transfer is taken place from one to another line; this assignment is also called the coupling effect. As the evolution of semiconductor technology, couplers have found their manufacture way newly in integrated circuits.

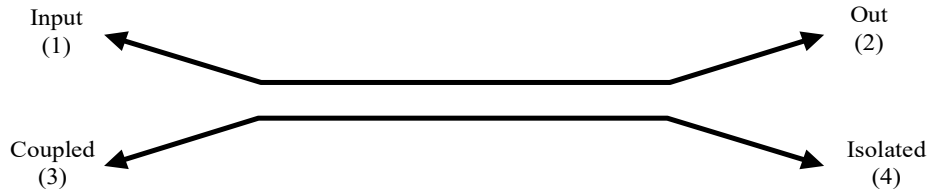


Figure 3-12. Typical coupler

The fundamental operation of couplers can be described as following. A signal is imposed to the input port, most of the signal power is transferred to the output port. Due to the coupling effect, the coupled port absorbs an amount of the signal power. The isolated port is terminated by a load, which is defined by the characteristic impedance (Z_0). A perfect impedance matching ensures no power leakage at this port. The feature that differentiates a directional coupler from other types of hybrids is that the power at the output power is different. A coupler is characterized by four main parameters below:

- The coupling factor (C): represents the fundamental property of a directional coupler. This factor defines the amount of incident power that can go to the coupled port instead of the direct output. The coupling factor has negative value; it cannot exceed 0dB for a passive device. In practice, this parameter does not exceed -3dB since the power at the output port requires being higher than the one from the coupled port. Otherwise, the roles of these ports would be reversed. The coupling factor is not constant and dependent on frequency. The coupling at the center frequency can specify directional couplers.

$$C(dB) = 10 \log \frac{P_1}{P_3} = -20 \log |S_{13}| \quad (3.3)$$

- Insertion loss (L): is calculated in the main path from the input port to the output port.

$$L_{i2,1} = -10 \log \left(\frac{P_{out}}{P_{in}} \right) [dB] \quad (3.4)$$

Alongside the insertion loss, the coupling loss is also defined as the power loss arriving at the coupled port.

$$L_{c2,1} = -10 \log \left(1 - \frac{P_3}{P_1} \right) [dB] \quad (3.5)$$

In the ideal directional coupler, the coupling loss is part of the insertion loss. In practice, the insertion loss contains coupling loss, dielectric loss, conductor loss and VSWR loss.

- Isolation (I): defined as the discrepancy of signal levels between the input port and the isolated port in the condition of matching the impedances at two ports. Isolation also indicates the amount of power arriving at the isolated port.

$$I_{4,1} = -10 \log \left(\frac{P_4}{P_1} \right) [dB] \quad (3.6)$$

- Directivity (D): specifies the part of the power transmitting from the input port to the isolated port. Directivity relates directly to isolation.

$$D_{3,4} = -10 \log \left(\frac{P_4}{P_3} \right) = -10 \log \left(\frac{P_4}{P_1} \right) + 10 \log \left(\frac{P_3}{P_1} \right) = I + C \quad (3.7)$$

Also, an ideal symmetrical directional coupler can be expressed in S-parameters, as following:

$$S = \begin{bmatrix} 0 & \tau & \kappa & 0 \\ \tau & 0 & 0 & \kappa \\ \kappa & 0 & 0 & \tau \\ 0 & \kappa & \tau & 0 \end{bmatrix}$$

κ : the coupling coefficient

τ : the transmission coefficient

For a passive ideal directional coupler, we have $\tau\bar{\tau} + \kappa\bar{\kappa} = 1$.

The insertion loss is calculated directly by τ

$$L(dB) = -20 \log |\tau| \quad (3.8)$$

κ determines the coupling factor:

$$C(dB) = 20 \log |\kappa| \quad (3.9)$$

Depending on applications, couplers can be used as power splitter or power combiner. In the reference [39], the authors introduce the usage of couplers in power combining and splitting to implement the balanced PA.

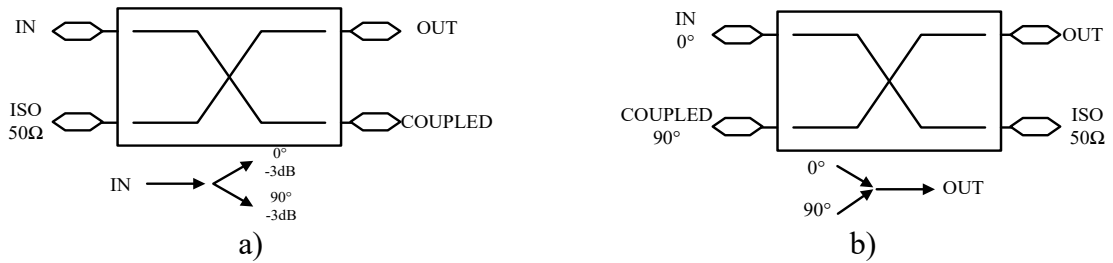


Figure 3-13. The usage of couplers: a) power splitter and b) power combiner

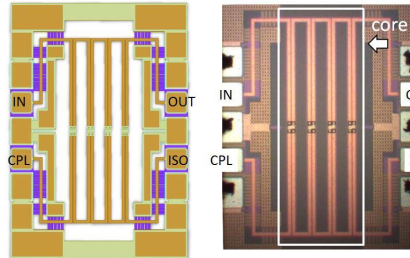


Figure 3-14. Momentum view and photography of quadrature coupling [39]

3.3.2.3 Transformers

Being widely used passive circuits, transformers have emerged popularly in integrated circuit design such as PAs, LNAs, VCOs, mixers. A transformer is formed by two magnetically coupled coils, the primary and the secondary. The percentage of the magnetic flux generated by the primary current transferring into the secondary winding determines the efficiency of a transformer. The coupling can be shown in terms of the mutual inductance.

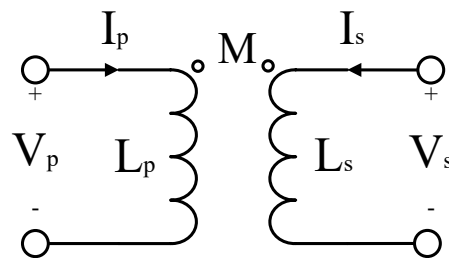


Figure 3-15. Transformer topology

Figure 3-15 illustrates a simple transformer topology. In case of a current-flowed input and an open-circuit output, the secondary current is theoretically zero or $i_s=0$. The primary voltage V_p can be described in this case as below:

$$V_p = L_p \frac{di_p}{dt} \quad (3.10)$$

The mutual inductance M also induces a voltage in the secondary winding. This amount of voltage can be expressed by the equation (3.9).

$$V_s = M \frac{di_p}{dt} \quad (3.11)$$

In practice, the voltage in a winding can be calculated by the sum of one self-created and the other generated by the coupling effect from another winding. The equation is expressed in (3.12) and (3.13).

$$V_p = L_p \frac{di_p}{dt} + M \frac{di_s}{dt} \quad (3.12)$$

$$V_s = L_s \frac{di_s}{dt} + M \frac{di_p}{dt} \quad (3.13)$$

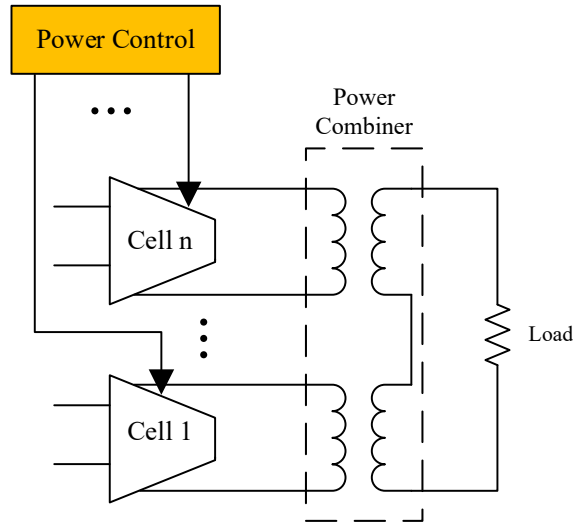


Figure 3-16. Distributed active transformer to combine power from power cells

One of the applications of the transformer in power amplifiers is the impedance matching, alongside power combining. To reach watt-level output power and ensure the reliability of transistors, PAs need to combine power from several power sub-cells. The assembly of multiple separated primary windings allows accomplishing the power combining from power cells. The more-than-one-winding transformer is called Distributed Active-Transformer (DAT) [41], as shown in Figure 3-16. This work adopts this kind of transformers as power combiner since they present more advantages on combining power and matching impedance than other ones.

3.3.3 Electrical and mechanical features of transformers

3.3.3.1 Categories of transformers and load modulation analysis

Depending on the way of combining voltage and current at load, transformers can be categorized as serial-combining transformers (SCT) and parallel-combining transformers (PCT) [40]. The requirement of output power poses a challenge on how to design a power-combining way for the transformer. The specifications of the 4G LTE PA also indicate the importance of a high reconfiguration on multiple modes. As a result, the distributed active transformer is chosen to implement the power combiner of this reconfigurable PA. The next part will describe the electrical models of two types of distributed active transformers: SCT and PCT.

3.3.3.1.1 Serial-combining transformers (SCT)

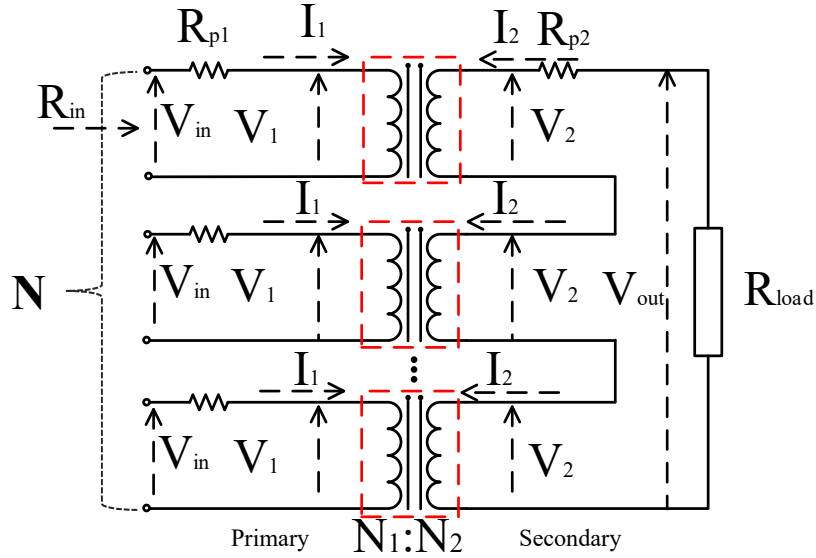


Figure 3-17. Serial-combining transformers conceptual topology

N : number of primary windings,

N_1 : number of primary turns,

N_2 : number of secondary turn,

R_{P1}, R_{P2} : parasitic serial resistances in the primary and secondary windings.

Parasitic serial inductances are only taken into account as the critical cause of losses in the CMOS process to simplify the theoretical analysis. Other layout-dependent parameters, for example, mutual inductance and coupling effect, are neglected. Figure 3-17 illustrates the theoretical topology with the same current I_1 for all primary windings. The relation between the primary and secondary currents and voltages of the transformer can be expressed as below:

$$\frac{I_2}{I_1} = \frac{N_1}{N_2} \quad (3.14)$$

$$\frac{V_1}{V_2} = \frac{N_1}{N_2} \quad (3.15)$$

From (3.14) and (3.15), the primary voltage can be calculated:

$$V_1 = \frac{N_1}{N_2} V_2 = \frac{N_1}{N_2} \cdot \frac{R_{load} + R_{P2}}{N} \cdot I_2 \quad (3.16)$$

The input impedance R_{in} , which is defined as the one looking into the primary winding of the transformer, can also be calculated as in (3.15). The input impedance increases when lowering the number of windings or scaling up the turn ratio of transformer.

$$\begin{aligned}
R_{in} &= \frac{V_{in}}{I_1} = \frac{V_1 + R_{P1}I_1}{I_1} = R_{P1} + \frac{V_1}{I_1} = R_{P1} + \frac{N_1}{N_2} \cdot \frac{R_{load} + R_{P2}}{N} \cdot \frac{I_2}{I_1} \\
&= R_{P1} + \left(\frac{N_1}{N_2}\right)^2 \cdot \frac{R_{load} + R_{P2}}{N}
\end{aligned} \tag{3.17}$$

The power-combining efficiency of the transformer is defined as the percentage of the incident power arriving at the load connected to the secondary winding. Hence, this parameter can be calculated as below:

$$\begin{aligned}
\eta_{SCT} &= \frac{P_{out}}{N \cdot P_{in}} = \frac{1}{N} \cdot \frac{V_{out} \cdot I_2}{V_{in} \cdot I_1} = \frac{1}{N} \cdot \frac{N_1}{N_2} \cdot \frac{V_{out}}{V_{in}} = \frac{1}{N} \cdot \frac{N_1}{N_2} \cdot \frac{NV_2 - R_{P2} \cdot I_2}{R_{P1} \cdot I_1 + V_1} \\
&= \frac{R_{load}}{N \cdot \left(\frac{N_2}{N_1}\right)^2 R_{P1} + R_{load} + R_{P2}} \\
&= \frac{1}{1 + \frac{1}{R_{load}} \cdot [N \cdot \left(\frac{N_2}{N_1}\right)^2 R_{P1} + R_{P2}]}
\end{aligned} \tag{3.18}$$

From the equation (3.18), the power-combining efficiency depends deeply on the serial parasitic resistances of CMOS process, the number of primary windings and the number of primary and secondary turns since the load is fixed at 100 Ohm for differential pads or at 50 Ohm for single-ended pads.

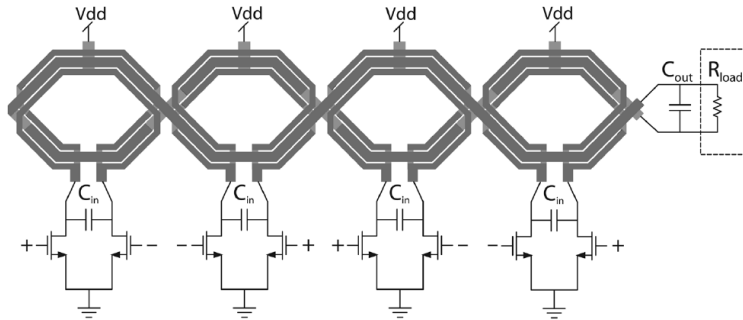


Figure 3-18. SCT Figure-8 transformer [42]

One of the typical SCT design is presented in [42], as shown in Figure 3-18. This type of transformer optimizes power-combining efficiency by reorienting the current direction in the electromagnetic field.

3.3.3.1.2 Parallel-combining transformers (PCT)

The analysis of PCT transformers is similar to the one of SCT. It could be assumed that the current at the secondary winding is uniformly attributed from the primary windings, as shown in Figure 3-19.

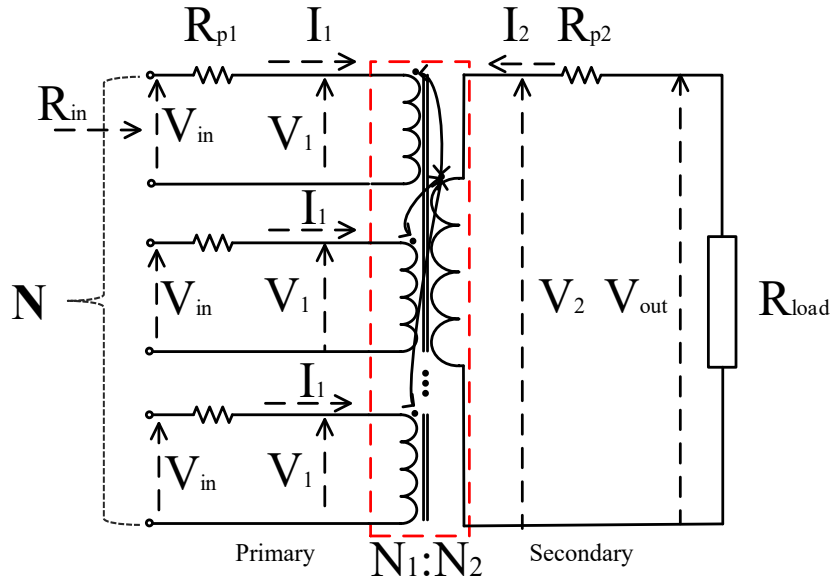


Figure 3-19. Parallel-combining transformers conceptual topology

The relation of current and voltage between two windings can be expressed as below:

$$\frac{I_2}{I_1} = N \cdot \frac{N_1}{N_2} \quad (3.19)$$

$$\frac{V_1}{V_2} = \frac{N_1}{N_2} \quad (3.20)$$

By taking the same calculation as in (3.14), the primary voltage can be calculated from (3.20):

$$V_1 = \frac{N_1}{N_2} V_2 = \frac{N_1}{N_2} \cdot (R_{load} + R_{P2}) \cdot I_2 \quad (3.21)$$

The input impedance R_{in} as in PCT transformers, which is defined as the one looking into the primary winding of the transformer, can also be calculated:

$$R_{in} = \frac{V_{in}}{I_1} = \frac{V_1 + R_{P1} I_1}{I_1} = R_{P1} + N \cdot \left(\frac{N_1}{N_2} \right)^2 \cdot (R_{load} + R_{P2}) \quad (3.22)$$

By using the same calculation as (3.18), the efficiency of PCT can be expressed as follows:

$$\eta_{PCT} = \frac{P_{out}}{N \cdot P_{in}} = \left(1 + \frac{1}{R_{load}} \cdot \left[\frac{1}{N} \cdot \left(\frac{N_2}{N_1} \right)^2 R_{P1} + R_{P2} \right] \right)^{-1} \quad (3.23)$$

One of the typical PCT design is the Voltage-Boosting Parallel-Primary transformer, as shown in Figure 3-20 [43].

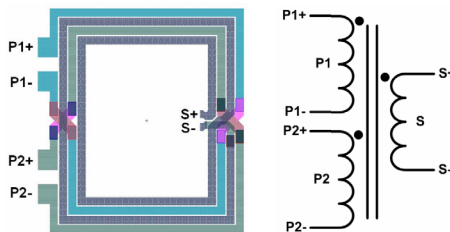


Figure 3-20. Voltage-Boosting Parallel-Primary Transformer [43]

Through the equations (3.18) and (3.23), it is noted that the number of unit windings (N) has the direct impact on transformer performances by reducing the power-combining efficiency in SCT structure and improving theoretically it in PCT structure. As shown in Figure 3-18 and Figure 3-20, the PCT structure also allows the matching network to be more compact. However, the impedance transformation presented by the PCT structure would be smaller than the one introduced by the SCT structure for the same turn ratio. Moreover, the ratio between the output impedance of sub power cells and the output impedance applied to RF pads is high enough. Since the power cell switching (PCS) technique, as mentioned in Chapter 2, demands a high impedance transformation, the SCT structure is hence much preferred.

3.3.3.1.3 Load modulation

To be continued, the load modulation in the SCT transformer is analyzed as follows. A transformer plays the impedance transformation between the load and a lower-value impedance seen by each elementary amplifier at primary windings. This kind of transformer also combines power provided from each unit power cell. The primary windings as independent unit transformers are connected to unit amplifiers. Each of them is driven separately by a separate same-level-signal source. The secondary sides of unit transformers are connected in series as in the SCT structure. The power cell switching (PCS) technique relies on dynamic load modulation for the primary and secondary windings if any unit cell is turned off. To carry out the analysis, we assume that the distributed active transformer has N unit transformer. Each unit transformer is connected to a unit power cell, and it has the turn ratio “ m ” with one tour for the secondary winding.

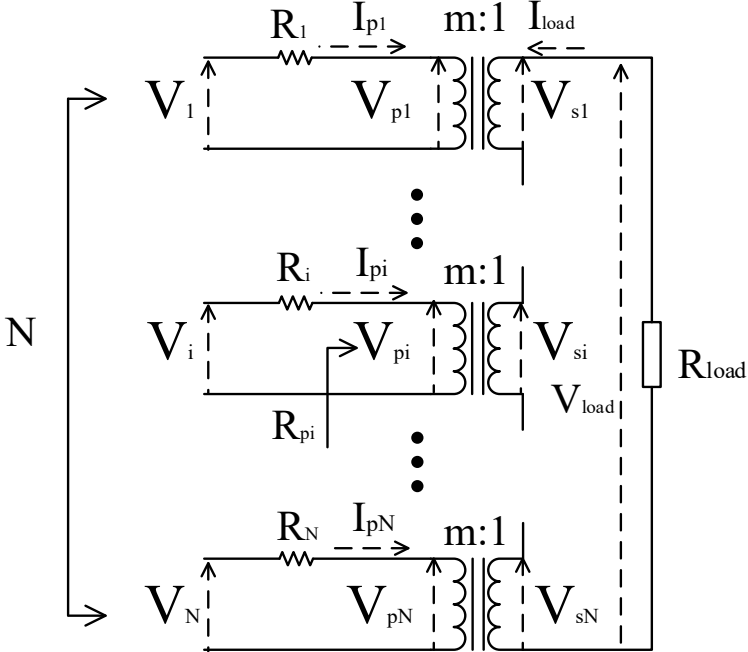


Figure 3-21. Conceptual diagram of the transformer-based power combining

The basic equations that describe the transformer are:

$$\frac{I_{si}}{I_{pi}} = m \quad (3.24)$$

$$\frac{V_{si}}{V_{pi}} = \frac{1}{m} \quad (3.25)$$

In the ideal case, assuming the equal signal levels are imposed on the primary sides, that is:

$$V_1 = V_2 = \dots = V_n = V_0 \text{ and } V_{p1} = V_{p2} = \dots = V_{pn} = V_{p0} \quad (3.26)$$

Due to the serial connection of the secondary sides, N unit primary sources increases the AC voltages on the secondary.

$$V_{load} = \sum_{i=1}^N V_{si} = \frac{1}{m} \sum_{i=1}^N V_{pi} = V_{p0} \cdot \frac{N}{m} \quad (3.27)$$

The primary currents are equal and proportional to the secondary current. Moreover, it is an out-of-phase relation and expressed as below:

$$I_{load} = N \cdot I_1 \quad (3.28)$$

The impedance seen from the primary side of each unit transformer can be determined with:

$$R_{pi} = \frac{V_{pi}}{I_{pi}} = \frac{V_{pi}}{V_{si}} \cdot \frac{V_{si}}{I_{si}} \cdot \frac{I_{si}}{I_{pi}} = m^2 \frac{R_{load}}{N} \quad (3.29)$$

Hence, the power transferred to load is obtained:

$$P_{load} = \frac{1}{2} \cdot \frac{V_{load}^2}{R_{load}} = \frac{1}{2} \cdot \left(\frac{N}{m}\right)^2 \cdot \frac{V_{p0}^2}{R_{load}} \quad (3.30)$$

The power received from each unit source is

$$P_i = \frac{1}{2} \cdot \frac{V_{pi}^2}{R_{pi}} = \frac{1}{2} \cdot \frac{N}{m^2} \cdot \frac{V_{p0}^2}{R_{load}} \quad (3.31)$$

From (3.30) and (3.31), it is proved that the power conversion from unity transformers to the load is 100% in the ideal case.

$$P_{load} = \sum_{i=1}^N P_i \quad (3.32)$$

As aforementioned, the inherent problem of conventional PAs is only reaching their maximum efficiency at a power level, frequently around the peak value. The efficiency is degraded significantly when the output power level moves backward. To handle this issue, the PCS technique offers a solution to control and improve the efficiency at power back-off. To obtain higher back-off efficiency, the PA is thus supposed to operate in a lower power zone. Unit power cells can be activated or deactivated as the required output power. Also, this method requires the unique transformer layout with additional considerations on inter-winding

electromagnetic couplings. The operating procedure can be controlled by digital codes $\{b_1, \dots, b_N\}$. Figure 3-22 illustrates the operating concept of the power cell switching technique. Each digital code can be performed merely by a switch with two operating states, ON and OFF. These switches combined with the supply sources determine which power cells can be chosen to conduct the power.

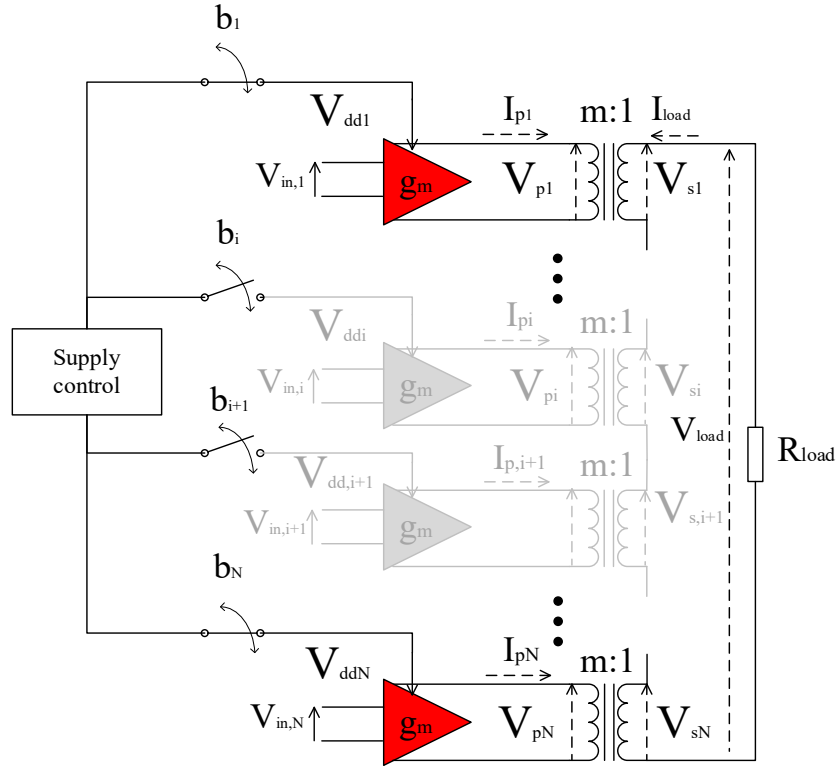


Figure 3-22. N-way power combining with N elementary power cells

Considering that elementary power cells have an identical design, they can be expressed under the g_m symbol. To calculate the impedance of each power cell and the back-off efficiency, the operating mode of power combining is divided into two parts, the peak-power part, and the back-off-power part.

- In the peak-power part:

The load seen by each cell is $R = \frac{m^2}{N} R_{load}$.

The voltage gain of each amplifier is

$$A_{unit\ cell} = g_m \cdot \frac{m^2}{N} R_{load} \quad (3.33)$$

The total voltage gain combined with the transformer is:

$$A_{combined} = N \cdot A_{unit\ cell} = g_m \cdot m^2 \cdot R_{load} \quad (3.34)$$

The output voltage swing of each elementary power cell at the maximum output power is

$$V_{pi_{max}} = V_{in,i_{max}} \cdot A_{unit\ cell} = g_m \cdot m^2 \cdot R_{load} \cdot V_{in,i_{max}} = V_{0_{max}} \quad (3.35)$$

At the peak output power, the global amplifier and the unit power cell reach their maximum efficiency :

$$\eta_{global} = \eta_{unit} = \eta_{max} \quad (3.36)$$

The peak output power can be identified as follows:

$$P_{peak} = N \cdot P_{unit\ cell_{peak}} = N \cdot \frac{1}{2} \cdot \frac{V_{pi,max}^2}{R} = \left(\frac{N}{m}\right)^2 \cdot \frac{1}{2} \cdot \frac{V_{0_{max}}^2}{R_{load}} \quad (3.37)$$

- In the back-off-power part:

By assuming that there are a number “b” of inactive cells among N power cells, the back-off power to which the power combining technique aims is:

$$OBO [dB] = -20 \log \frac{N-b}{N} \quad (3.38)$$

For instance, there are four unit power cells in parallel, and one of them is turned off. The targeted back-off power level with this technique is 2.5dB.

The input swing imposed at the input of each unit amplifier is reduced to:

$$V_{in,i_{OBO}} = \frac{N-b}{N} V_{in,i_{max}} \quad (3.39)$$

The impedance seen by each active power cell is now:

$$R_{OBO} = \frac{m^2}{N-b} R_{load} \quad (3.40)$$

The voltage gain of each cell increases to:

$$A_{unit\ cell} = g_m \cdot \frac{1}{N-b} R_{load} \quad (3.41)$$

The output swing of each power cell is:

$$\begin{aligned} V_{pi_{OBO}} = V_{0_{OBO}} &= A_{unit\ cell} \cdot V_{in,i_{OBO}} = g_m \cdot \frac{m^2}{N-b} R_{load} \cdot \frac{N-b}{N} V_{in,i_{max}} \\ &= g_m \cdot \frac{m^2}{N} R_{load} \cdot V_{in,i_{max}} = V_{0_{max}} \end{aligned} \quad (3.42)$$

It is straightforward from (3.35) and (3.42) to see that the output swing of each power cell returns the same value $V_{0_{max}}$ as in the peak-power part. The voltage gain of the global power combining amplifier is determined with the same value:

$$A_{combined} = N \cdot A_{unit\ cell} = g_m \cdot m^2 \cdot R_{load} \quad (3.43)$$

The relation between the efficiency of the unit power cells and that of the global amplifier is derived as follows:

$$\eta_{global} = \eta_{unit} = \eta_{max} \quad (3.44)$$

The RF output power from this point is

$$\begin{aligned} P_{OBO} &= (N - b) \cdot P_{unit\ cell_{OBO}} = (N - b) \cdot \frac{1}{2} \cdot \frac{V_{OBO}^2}{R_{OBO}} \\ &= \left(\frac{N - b}{N}\right)^2 \cdot \left(\frac{N}{m}\right)^2 \cdot \frac{1}{2} \cdot \frac{V_{0max}^2}{R_{load}} = \left(\frac{N - b}{N}\right)^2 \cdot P_{peak} \end{aligned} \quad (3.45)$$

From two analyses of the peak output power and the back-off output power, the power cell switching technique demonstrates the capability to enhance significantly back-off efficiency. Power amplifiers tend to move into lower output power instead of its peak if the peak is not required. This trend poses an inherent impact on the input and output swing of each sub power cells. At this point, the efficiencies of unit cells and the global amplifier drop simultaneously. However, the PCS technique can handle this issue by turning off one or more unit cells. In this regard, the output swing of active unit cells is still maintained. The efficiency can be enhanced in back-off power zone as well.

In a specific example of four unit cells combined with a distributed active transformer, each unit transformer has the same turn ratio that equals to one as in Figure 3-24. The global amplifier can boost the efficiency in the back-off power levels of 2.5dB, 6dB and 12dB by turning off one, two or three unit power cells, respectively. The operating mode of this global amplifier can be controlled by the supply control that composes of four separate bits. For the back-off level of 2.5dB, a bit such as b_2 plays the role to cut off the corresponding supply source to the unit amplifier 2. The ideal efficiency of the global power amplifier is expressed in Figure 3-23.

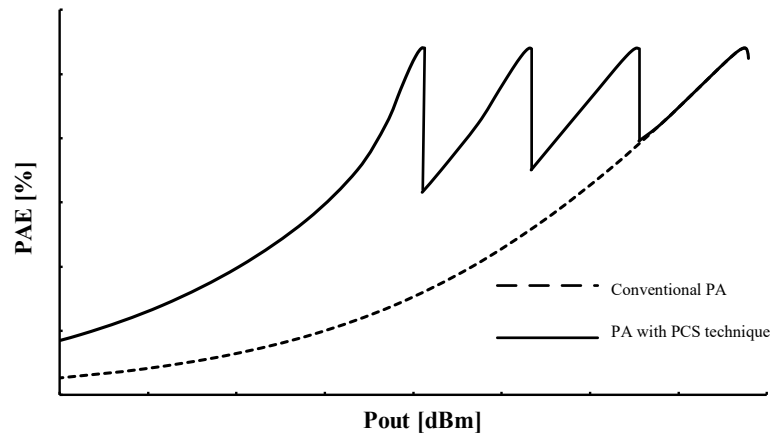


Figure 3-23. Ideal back-off efficiency enhancement for a PA with the PCS technique

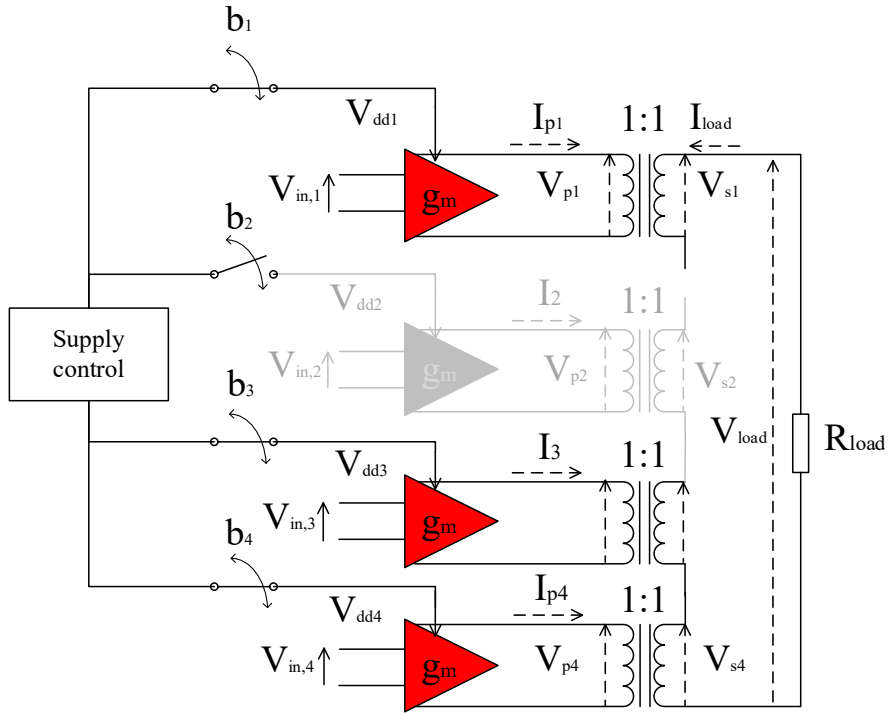


Figure 3-24. Four unit power cells combined with a four-way one-turn-ratio transformer

3.3.3.2 Electrical features of transformers

In the previous subsection, we have neglected layout-dependent parameters to simplify the theoretical analysis. This subsection will take into account most of these parameters of transformers to carry out the complete analysis of the transformer design.

3.3.3.2.1 Parameter definitions

For transformers in a multi-port configuration, it is essential to take into consideration the following parameters:

- **Bandwidth:** Defines the frequency range in which the device behaves as a transformer. This parameter can be expressed in terms of insertion loss or phase difference between primary and secondary windings. The most common definition of transformer bandwidth is the 1dB attenuation, which describes the frequency limitation that transformers expose 1-dB of loss. This parameter will be extracted under the setting of the global architecture that includes unit power cells and other blocks.
- **Insertion loss:** The amount of lost signal from the input to the output during the transformer's operation, expressed in dB. For instance, two signals with 1dBm of power are combined by a two-winding transformer. The insertion loss of this transformer is 0.5dB. Hence, the received power at the output would be 1.5dBm (1+1-0.5).
- **Isolation:** The amount of undesired power going to another port without any exiting to the output port. This parameter is often calculated by S_{12}, S_{13}, \dots in S-parameters.

- Mismatch: Describes the difference in power between two input terminals. It is crucial to minimize the mismatch, which can result in efficiency loss and self-heating, to assure the optimal performance of transformers. Sometimes, circuit designers take advantage of mismatch by implementing the asymmetric-structure transformer, for example, in Doherty Power Amplifier.
- Transformation ratio: Some kinds of transformers have different input and output impedances. The most famous one is the distributed active transformer (DAT). This type of transformer requires a transformation ratio higher than one to implement the impedance matching.
- Primary and secondary inductances: These parameters are extracted and calculated from the S-parameters. Transformers are well-known for their inductive behavior. It is essential to increase the inductance value at the central frequency. From the values of inductances, circuit designers can determine the self-resonant frequencies of primary and secondary windings.
- Quality factor (Q): is the ratio of the inductive reactance to the resistance at a given frequency. The higher the Q factor is, the closer an inductor/transformer approaches its ideal behavior. In radio transmitters and receivers, high-Q inductors are widely used to make resonant circuits with capacitors. The higher the quality factor is, the narrower the bandwidth also achieves.

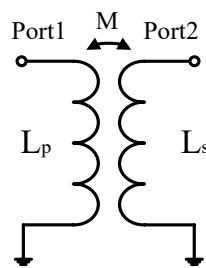


Figure 3-25. Transformer in 2-port configuration

Figure 3-25 depicts a typical transformer in two-port configuration. The necessary parameters of this transformer can be derived from the following equations. Equations (3.46) and (3.47) present the primary and secondary inductances in case of two-port configuration. Equations (3.48) and (3.49) indicate the primary and secondary quality factors in the example of the two-port configuration.

$$L_p = \frac{\text{Im}(Z_{11})}{\omega} \quad (3.46)$$

$$L_s = \frac{\text{Im}(Z_{22})}{\omega} \quad (3.47)$$

$$Q_p = \frac{Im(Z_{11})}{Re(Z_{11})} \quad (3.48)$$

$$Q_s = \frac{Im(Z_{22})}{Re(Z_{22})} \quad (3.49)$$

$$M = \frac{Im(Z_{21})}{\omega} \quad (3.50)$$

$$k = \frac{M}{\sqrt{L_p \cdot L_s}} \quad (3.51)$$

3.3.3.2.2 Electrical model analysis

A transformer can be created by commonly coupling two coils in the magnetic field as shown in Figure 3-26.

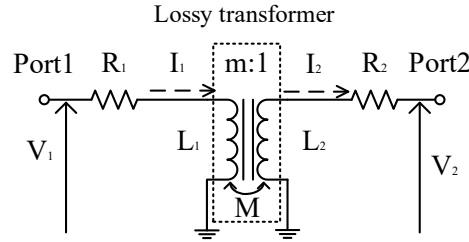


Figure 3-26. Transformer model

In a coupled-winding transformer, the input port-1 current I_1 creates the magnetic field in the primary winding L_1 . In the regard, this area generates a corresponding voltage in the secondary winding L_2 . The secondary-winding current also produces a voltage in the primary coil. The voltage relation can be derived as followed:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_1 & j\omega M \\ j\omega M & R_2 + j\omega L_2 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

$$M = k \cdot \sqrt{L_1 \cdot L_2} \quad (3.52)$$

$$m \approx \sqrt{\frac{L_1}{L_2}} \approx \frac{I_1}{I_2} \approx \frac{V_2}{V_1}$$

Where M is the mutual inductance, k is the coupling coefficient, and m is the turn ratio between primary and secondary windings of the transformer.

The equivalent model of lossy transformer [41] can be derived with the serial parasitic resistors (R_1, R_2) and the inductances of the primary and secondary windings (L_1, L_2), as depicted in Figure 3-27. The quality factors of both windings can also be directly determined. These quality factors are apparently different from those of standalone inductors due to the magnetic coupling that creates the current redistribution on both windings.

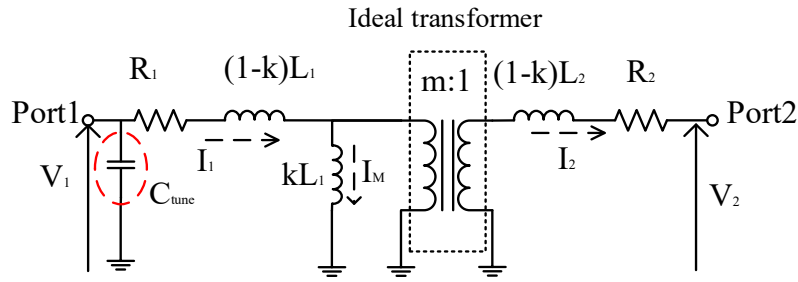


Figure 3-27. Equivalent model of lossy transformer

$$Q_1 = \frac{Im(Z_1)}{Re(Z_1)} = \frac{\omega L_1}{R_1} \text{ and } Q_2 = \frac{Im(Z_2)}{Re(Z_2)} = \frac{\omega L_2}{R_2} \quad (3.53)$$

The coupling coefficient (k) has a significant impact on the inductances of both windings, regarding the leakage inductances $(1-k)L_1$ and $(1-k)L_2$. As an output matching network in a power amplifier, it is necessary to eliminate some of the parasitic or leakage inductances to reduce the transformer loss. A capacitor is required on the primary side of the transformer as an input reactance regulation. This regulation allows the transistor of power cell to drive into its desired current value. The most frequent way to carry out the control is using a parallel capacitor C_{tune} on the primary side, as shown in Figure 3-28. As a result, the method helps minimize the transformer loss and balance the secondary-winding voltage swing as illustrated in Figure 3-29 if the output is a differential terminal.

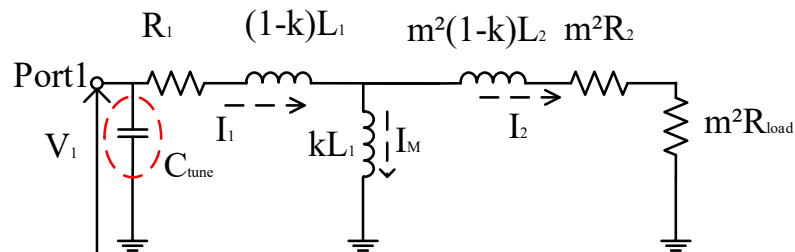


Figure 3-28. Transformer equivalent model with a parallel tuning capacitor C_{tune}

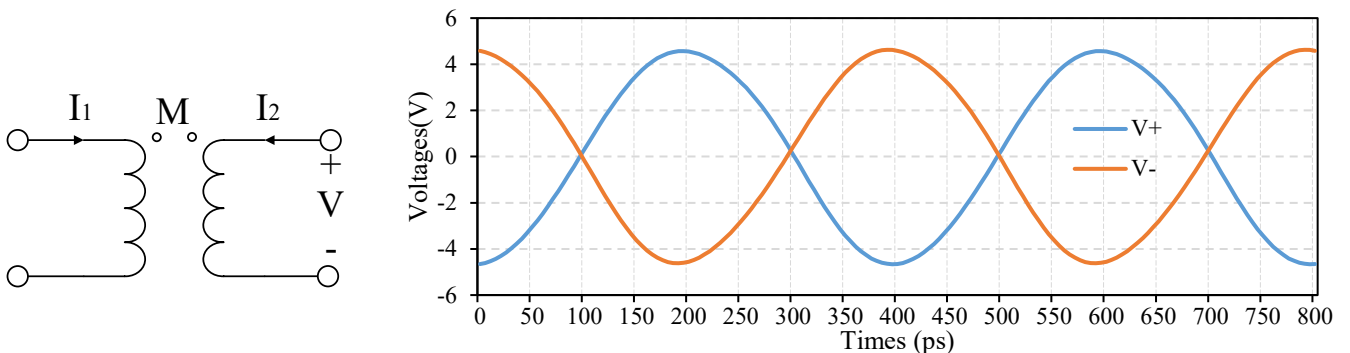


Figure 3-29. Differential output voltage swing of a power-combined amplifier

From the equivalent transformer model, the ratio I_1/I_2 between the primary and secondary windings is derived as below:

$$\begin{aligned}\frac{I_1}{I_2} &= \frac{I_M}{I_2} + 1 = \frac{m^2 R_{load} + m^2 R_2 + j\omega m^2 (1-k)L_2}{j\omega k L_1} + 1 \\ &= \frac{m^2 (R_{load} + R_2) + j\omega [m^2 L_2 + k(L_1 - m^2 L_2)]}{j\omega k L_1}\end{aligned}\quad (3.54)$$

The transformer efficiency is defined as the ratio of power at the load R_{load} and the total delivered power (including the consumed power on R_1 , R_2 and R_{load}):

$$\eta = \frac{P_{load}}{P_{total}} = \frac{m^2 R_{load} I_2^2}{I_1^2 R_1 + I_2^2 (R_{load} + R_2)} = \frac{R_{load}}{\left(\frac{I_1}{I_2}\right)^2 \cdot R_1 + R_{load} + R_2}\quad (3.55)$$

From the equations (3.54) and (3.55), the transformer efficiency can be deduced:

$$\eta = \frac{R_{load}}{\frac{m^2 (R_{load} + R_2)^2 + \omega^2 [m^2 L_2 + k(L_1 - m^2 L_2)]^2}{(\omega k L_1)^2} \cdot R_1 + R_{load} + R_2}\quad (3.56)$$

Assuming $L_1 \approx L_2 m^2$, the equation (3.56) can be simplified:

$$\eta = \frac{R_{load}}{\frac{m^2 (R_{load} + R_2)^2 + \omega^2 (m^2 L_2)^2}{(\omega k L_1)^2} \cdot R_1 + R_{load} + R_2}\quad (3.57)$$

To further enhance the transformer efficiency, a capacitor $C_{regulate}$ is added in series with the secondary coil, as shown in Figure 3-30.

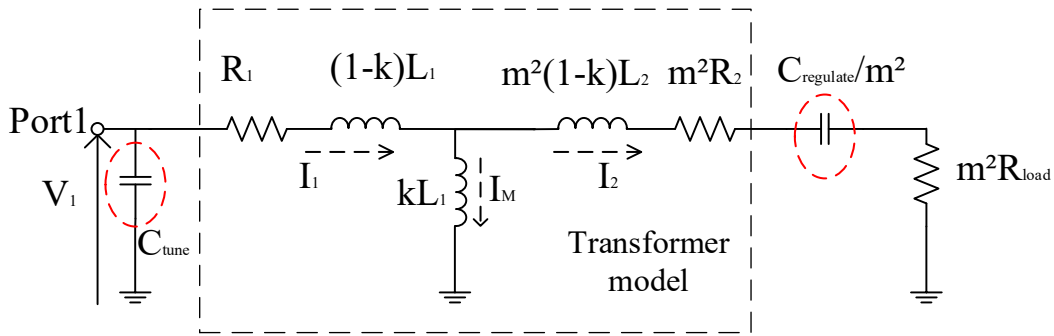


Figure 3-30. Transformer equivalent model with C_{tune} and $C_{regulate}$

Taking the same consideration and calculation as the equivalent model in Figure 3-28, the power transformation efficiency can be determined as below:

$$\eta = \frac{R_{load}}{\frac{m^2 (R_{load} + R_2)^2 + m^4 \left(\omega L_2 - \frac{1}{\omega C_{regulate}}\right)^2}{(\omega k L_1)^2} \cdot R_1 + R_{load} + R_2}\quad (3.58)$$

The equation (3.57) demonstrates that the regulated capacitor $C_{regulate}$ has a significant effect on the power transformation efficiency. By selecting the suitable value of $C_{regulate}$ to resonate

the secondary inductance L_2 at the center frequency $\left(\frac{1}{\omega C_{regulate}} = \omega L_2\right)$, the efficiency η can be enhanced as in the equation (3.59).

$$\eta = \frac{R_{load}}{\frac{m^2(R_{load} + R_2)^2}{(\omega k L_1)^2} \cdot R_1 + R_{load} + R_2} \quad (3.59)$$

3.3.3.3 Physical features of transformers

The performances of a transformer depend on its mechanical and electromagnetic elements. There are many methods to design a transformer and optimize its performances. All of them focus on how to layout a transformer to achieve the best coupling effect between the primary and secondary coils. Since the symmetry topology demonstrates an excellent coupling coefficient in comparison to the others, this work deploys this topology to implement transformer. The next subsections will introduce the fundamental considerations of symmetric single-turn transformer design. The other transformer types with multiple windings will be discussed in the next section.

3.3.3.3.1 Coupling direction

As aforementioned, the coupling effect relies upon the transformer layout. Based on the coupling direction, transformers can be categorized into two types: planar and stacked transformers. The former uses the lateral coupling type, which can be defined as two interleaved coupling inductors. The latter uses the vertical coupling type, which uses two same-size inductors in parallel. Each kind introduces its advantages and drawbacks in integrated circuits. The choice of the transformer also depends on the semiconductor technology and the design purpose. For example, the 65-nm CMOS technology offers two thick top metal layers and five intermediate metal layers to realize high-current transformer for impedance matching and power combining. The 180-nm CMOS technology, on the other hand, only provides three metals, which include one top-most metal level. Therefore, the stacked topology is more privileged in the 65-nm technology and so is the planar transformer in the 180-nm technology.

As mentioned in Chapter 2, the 65-nm CMOS technology is chosen to design the reconfigurable power amplifier including the transformers. This technology proposes a cost-effective solution for radiofrequency front-end integrated circuits. The inter-winding distance has a crucial role in the comparison of two types. The 65-nm CMOS technology poses many design rules, including a minimum spacing of 2- μm between two thickest-metal paths. Also, the technology introduces the constraints about the fixed thickness of metal layers and the interlayer distance. The depths of two top metal layers are 3.4- μm for the thickest one and 0.9- μm for another. The fixed inter-layer distance in this technology is 0.79- μm . By quantitative

analysis about the inter-winding gap, the stacked topology demonstrates apparently more advantages on the coupling effect of the transformer.

Electromagnetic simulations under the same configuration for both types are conducted to compare two categories of transformers. These simulations present a qualitative analysis for the choice of transformer type. Figure 3-31 illustrates a design example of two transformer types: a) stacked and b) planar. Both of structures have one-turn windings and the same geometric size of $244\mu\text{m} \times 167\mu\text{m}$. The primary winding of the planar transformer has the same design as one of the stacked transformers. The secondary coil is performed by another same-metal tour with a minimum inter-winding distance of $2\mu\text{m}$ as required in design rules. Therefore, the secondary coil has a smaller diameter.

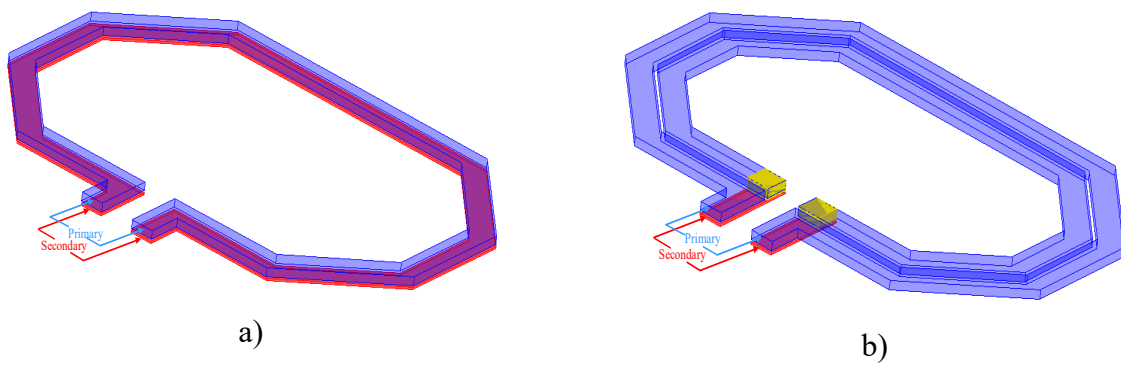


Figure 3-31. a) Stacked and b) Planar transformer types

Figure 3-32 depicts the primary and secondary inductances of two transformer types. Higher inductances are obtained with the stacked topology. This result is explained by a smaller size of the secondary winding of the planar topology. Figure 3-33 illustrates the primary and secondary quality factors. The stacked topology provides obviously the superior performances for the primary coil in comparison with the planar topology. Since the winding layout is identical, the secondary acts as a shield between the primary and the substrate. As a result, the stacked topology has a capacity of mitigating substrate loss. Despite the better quality factor of the primary presented by the stacked topology, the planar type also provides satisfactory Q-factors for both coils. This result is achieved by using two top-metal layers to implement this kind of transformer; hence, the planar presents more balanced quality factors for two loops.

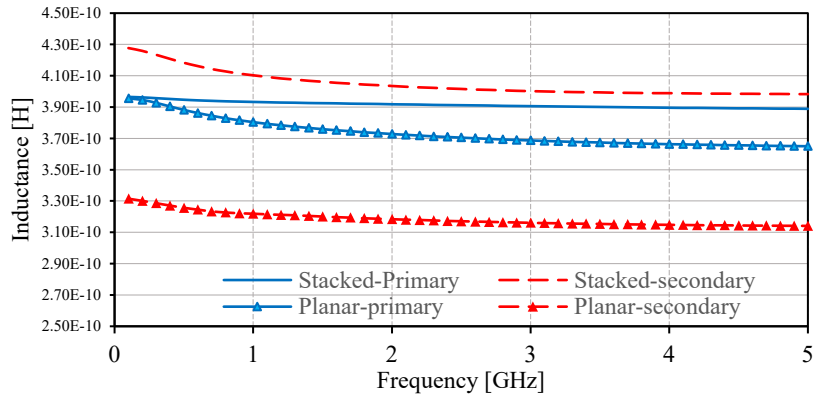


Figure 3-32. Simulated inductances of stacked and planar transformers

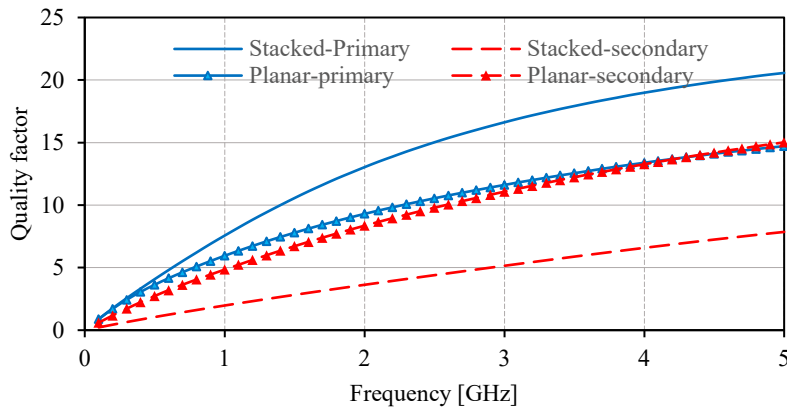


Figure 3-33. Q-factor of stacked and planar transformers

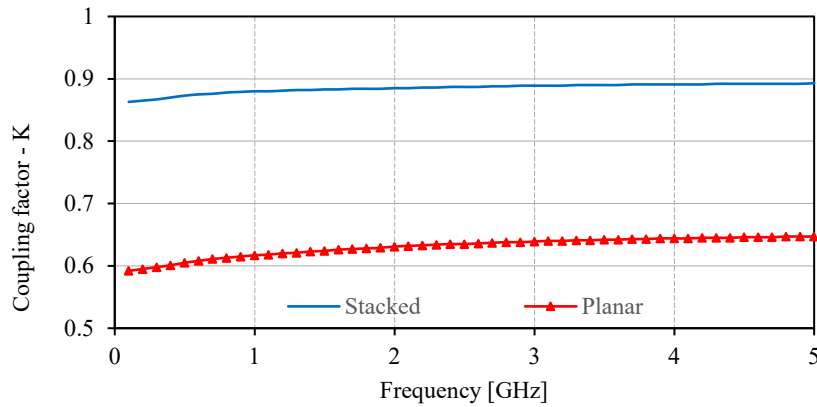


Figure 3-34. Coupling factor and insertion loss of stacked and planar transformers

The coupling factors for two types are presented in Figure 3-34. As depicted by the quantitative analysis, the stacked topology once again introduces a better performance about the magnetic coupling. The result shows a beneficial coupling coefficient of 0.87 at 2.5GHz while only 0.65 in the planar topology. Through two analyses, quantitative and qualitative ones, the stacked topology is thus adopted in this work to design elementary transformers.

3.3.3.3.2 Winding shape

The winding shape is the second fundamental consideration of transformers mentioned in this section. Several types of winding layout have been reported for the inductor and

transformer design, namely, orthogonal, polygonal, circular, hexagonal spirals and other shapes [44]. Among these models, circular and polygonal spirals are hardly used due to computer-aided-design (CAD) and technological constraints, which limit the snap angle to multiple of 45°. As a result, two kinds of spirals, orthogonal and hexagonal, are taken into account to choose the suitable winding shape for transformers. The simulations of two configurations are carried out in Momentum to select the appropriate architecture for the transformer. Two transformers have the same diameter of 167 μm x 244 μm and trace width of 12 μm . Both types are designed in the stacked topology. The simulation configuration for both transformers is also identical.

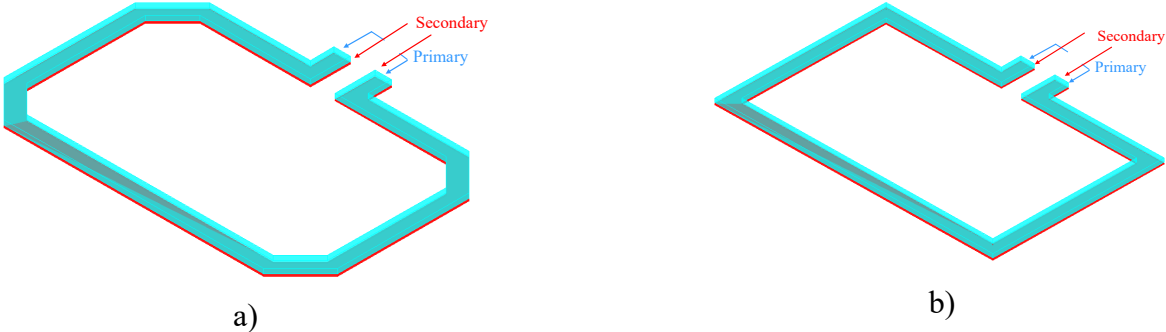


Figure 3-35. a) Hexagonal and b) Orthogonal topologies.

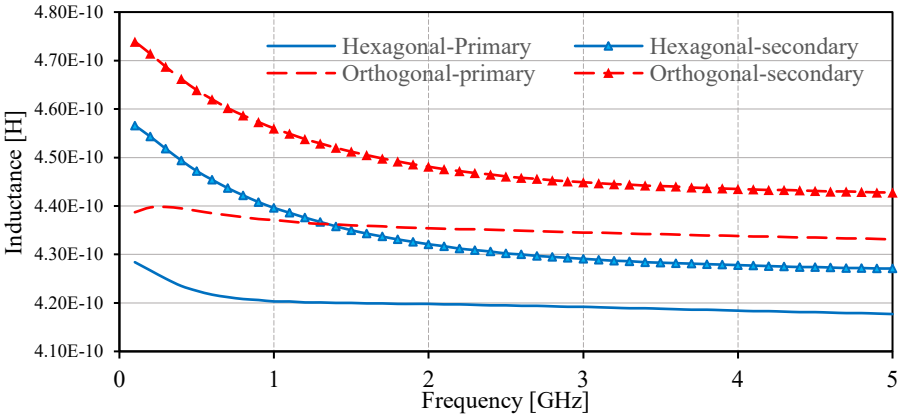


Figure 3-36. Simulated inductances of hexagonal and orthogonal transformers

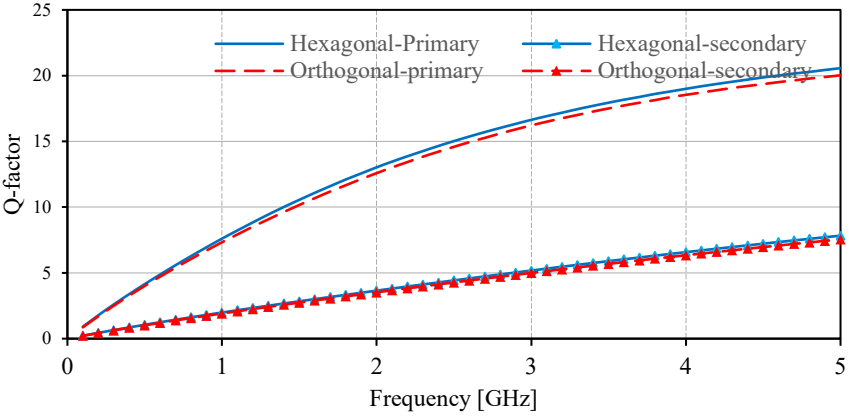


Figure 3-37. Q-factor of hexagonal and orthogonal transformers

Figure 3-36 indicates the simulated inductances of two transformers in post-layout simulation. With the same diameter, the orthogonal topology presents a more significant total length of two coils in comparison with that of the hexagonal topology. This reason explains why the orthogonal topology exhibits higher inductances for both loops.

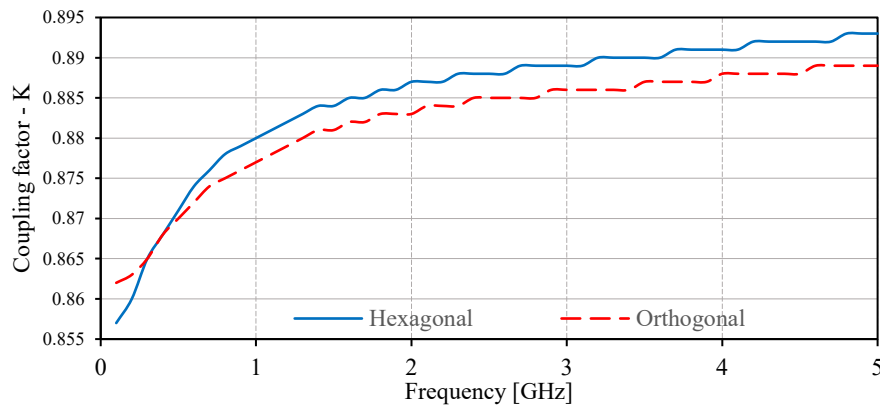


Figure 3-38. Coupling factors of two transformers, hexagonal and orthogonal

Figure 3-37 illustrates the Q-factors of two transformers. The hexagonal transformer presents a slightly higher Q-factors for two coils. This observation recalls that the hexagonal topology presents a lower insertion loss than the orthogonal one. Figure 3-38 depicts the coupling coefficient for both types. The coupling factor of the hexagonal shape is slightly better. The hexagonal shape is chosen to implement the unit transformer.

3.3.3.3 Unit-winding layout arrangement

After two considerations about winding shape and coupling direction, unit-winding layout arrangement is the third essential feature for transformers. In this subsection, the relative position of two coils is presented. Three relative winding positions of transformers, which are designed and simulated with the same size and the same simulation configuration, are conventional, flipped and 90°-rotation transformers. The first one, as depicted in Figure 3-39.a uses two identical-shape different-metal windings in the stacked topology. The feeding points of two ports are overlaid in the same horizontal coordinates. The second one, the flipped transformer (Figure 3-39.b), uses a 180°-rotation of the feeding points of two ports. The last one, the 90°-rotation transformer as shown in Figure 3-39.c rotates the secondary winding an angle of 90° from the primary coil. Two last layout arrangements cause some exposed areas that are not concerned in the coupling effect; therefore, they risk reducing the coupling coefficient of transformers.

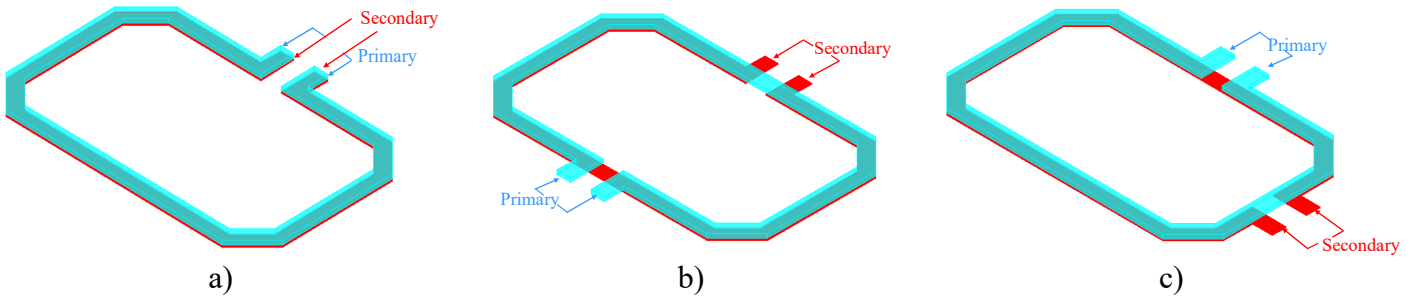


Figure 3-39. a) 90°-rotation b) Flipped and c) Conventional transformers

The simulated performances of three transformers are reported in Figure 3-40, Figure 3-41 and Figure 3-42. The inductances presented by the conventional transformer are lower than those of two modified-layout topologies. The quality factors introduced by three type of layout arrangements are approximately identical.

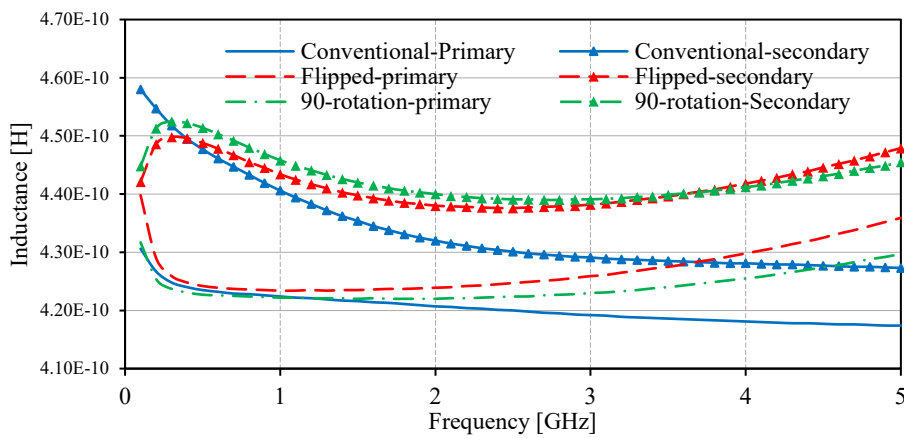


Figure 3-40. Simulated inductances of conventional, flipped and 90°-rotation transformers

As aforementioned, the coupling coefficients of the flipped and 90°-rotation transformers are slightly lower than that of the conventional one due to the uncoupling areas in their layouts. However, their values of coupling coefficient are quite close to the one of the convention model. The choice of the winding structure depends on transformer applications and performances. In case of being used in the power cell switching technique, a transformer requires multiple primary coils and a single secondary winding. This requirement demands to design a single secondary winding with numerous small secondary elements connected in series. This observation allows choosing two configurations, the flipped and the 90°-rotation types, as the most suitable layout arrangements for the application in the power cell switching technique.

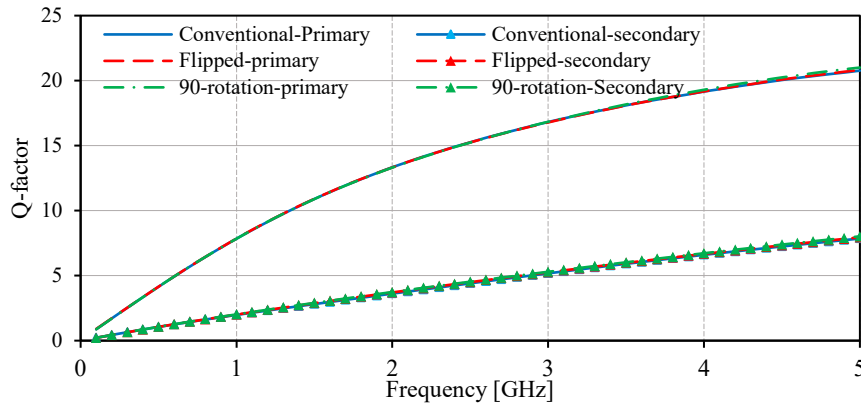


Figure 3-41. Q factors of three transformers, conventional, flipped and 90°-rotation

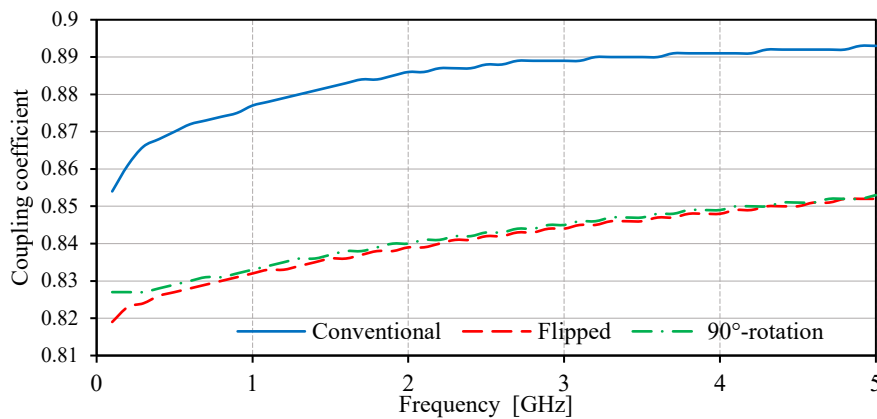


Figure 3-42. Coupling factors of three transformers, conventional, flipped and 90°-rotation

3.3.3.3.4 Winding geometry

Since transformers are space-occupying components in integrated circuits, circuit designers require taking the transformer size into account as a critical parameter. As the previous analysis in unit-winding layout arrangement, the flipped and 90°-rotation types offer a solution for multi-winding transformers in power-combining applications. This subsection will examine the performance of transformer according to its geometry.

Figure 3-43 illustrates the designs of two transformer types. The first one in Figure 3-43.a is based on two 90°-rotation windings. The principle of design is rotating two windings an angle of 90° to form a secondary in series. This method allows minimizing the parasitic capacitance effect in the primary and secondary coils. The second one uses the flipped topology to assembly two windings. This layout separates two output terminals of the transformer; therefore, it requires additional lines for the RF pads, whose pitches are strictly limited to 100 or 150µm. Moreover, the feeding input points of two types situate in two sides of transformers. For that reason, the input and output terminals of the transformer are thus better decoupled. The 90°-rotation transformer benefits considerably from the winding assemblage to reduce the component size vis-à-vis the flipped-winding transformer.

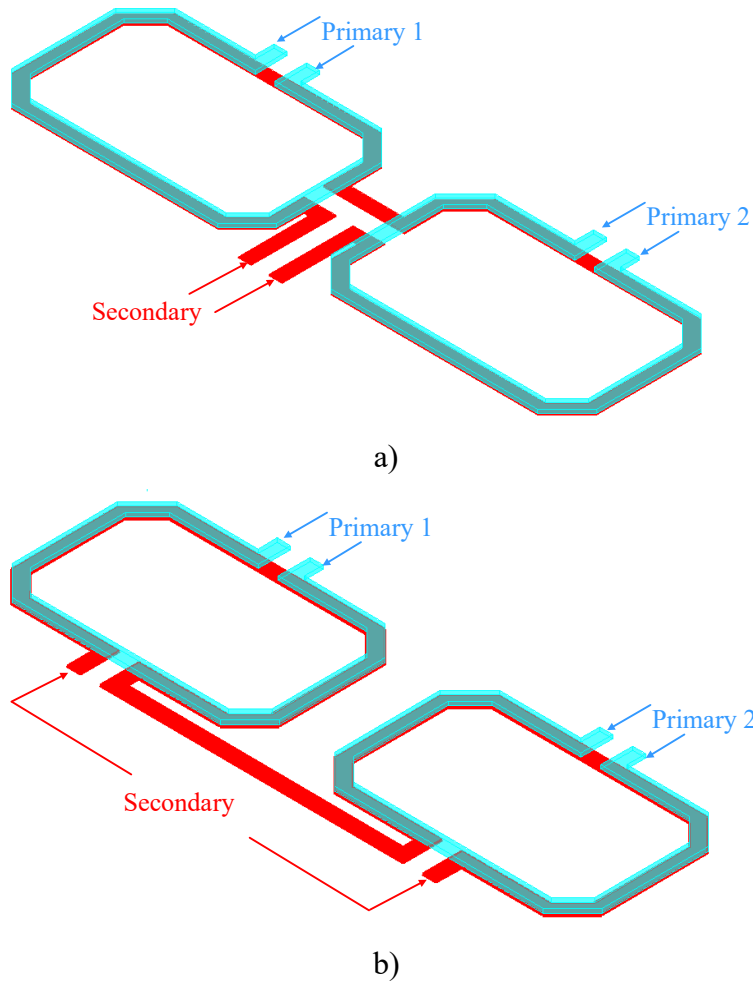


Figure 3-43. Two types of two-winding transformer used in power-combining applications
 a) 90°-rotation unit winding b) Flipped-type unit winding

Figure 3-44 illustrates the simulated inductances of two transformers. The secondary inductance of the flipped-winding transformer introduces apparently higher value than that of the 90°-rotation transformer thanks to a higher length in the secondary coil. The identical layout of the primary windings of two types derives the same primary inductances. Also, the obtained quality factors of two transformers are approximately the same.

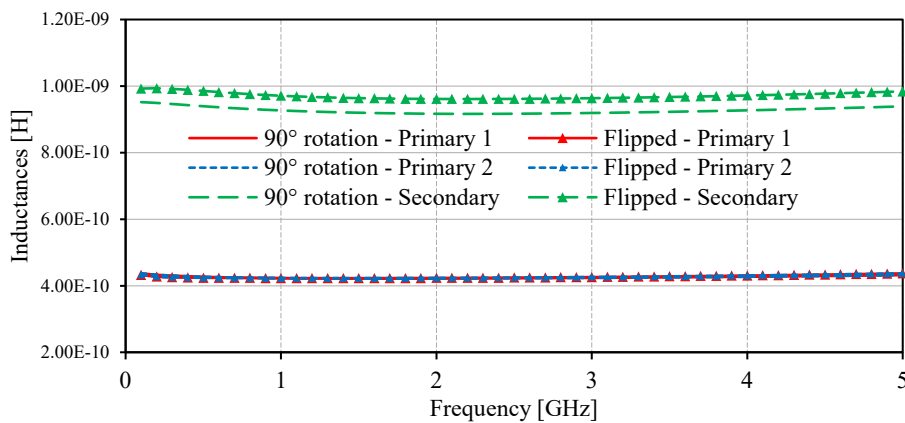


Figure 3-44. Inductances of primary and secondary windings in two types of transformer

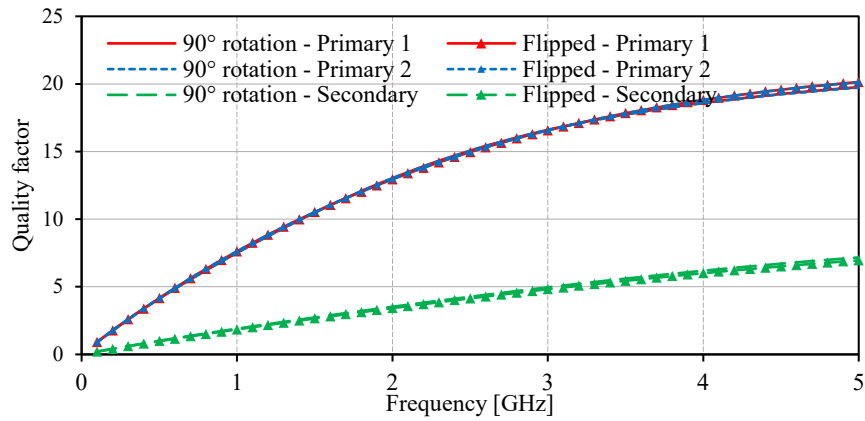


Figure 3-45. Quality factors of primary and secondary windings in two types of transformer

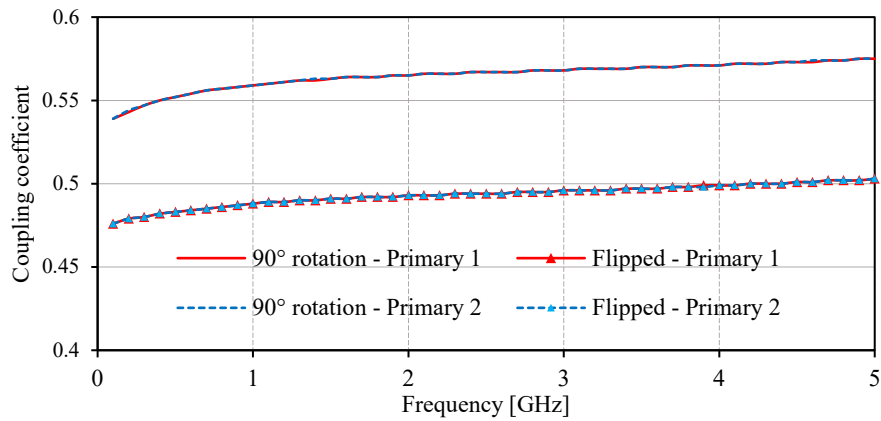


Figure 3-46. Coupling coefficient of elementary windings in two types of transformer

The simulated coupling coefficients are depicted in Figure 3-46. This figure presents that the 90°-rotation transformer introduces better coupling effect for two windings than the flipped-winding type. Through these analyses, the 90°-rotation transformer is hence adopted into the transformer design of this work due to its smaller size and the better coupling effect.

3.3.4 Loss mechanisms

The performances of passive devices depend strongly on the material properties. Figure 3-47 depicts the loss mechanisms in an integrated circuit process. The concept of loss mechanisms is once introduced in the reference [28]. Among these mechanisms, the semiconductor substrate and metal layers play the essential roles.

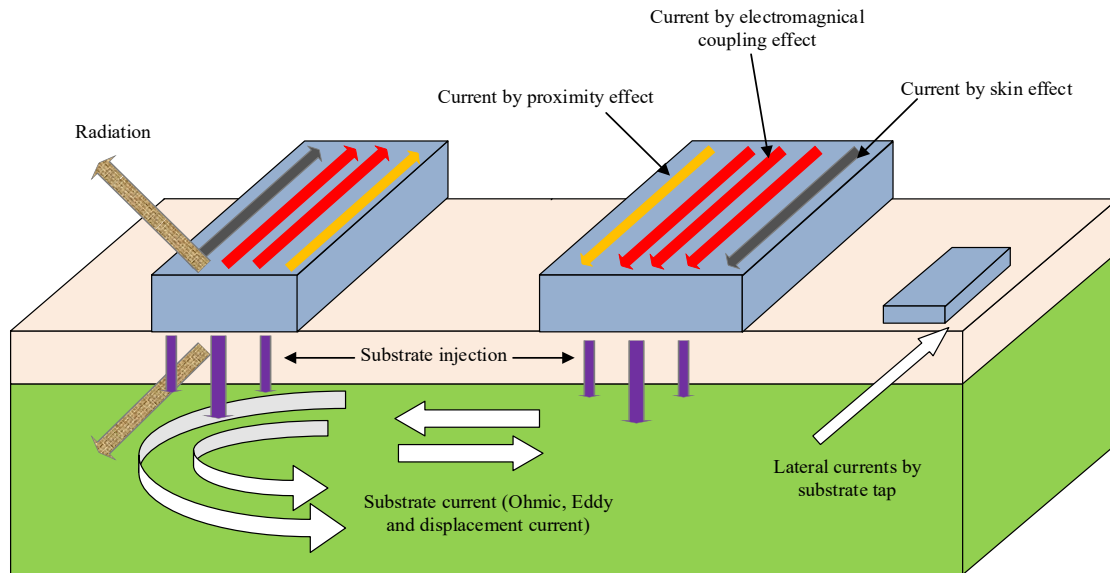


Figure 3-47. Loss mechanisms in an integrated circuit process [28]

3.3.4.1 Metal loss

Metal layers are the principal material used to build passive devices, namely inductors, capacitors, and transformers. Their conductivities thus decide the quality factor of such devices. An inductor uses metal conductors of some given conductivities. The reactive energy is stored in the magnetic field of the device, but other amounts of energy are dissipated in heat or radiation. The same impact of finite conductivities happens on the layout of a transformer. In case of a capacitor, the reactive energy is stored in the electric field created by the charges of two metal layers in a given spacing. Thermal dissipation is in the volume of two layers. A resistor can express this loss in three cases in series with the device.

The 65nm CMOS technology from TSMC provides nine copper layers and an aluminum layer with electrical conductivities $\sigma = 5.96 \times 10^7$ S/m and $\sigma = 3.77 \times 10^7$ S/m, respectively. Electro-migration in metal layers with DC and AC currents is one of the pervasive problems of the silicon substrate. This effect limits the maximum reliable current density of devices. Therefore, required precise calculations of DC and AC densities help circuit designers to avoid the failure mechanism due to the electro-migration. The bound of these current densities will be detailed in Appendix A – “CMOS restrictions”.

3.3.4.2 Substrate loss

As aforementioned, the substrate of technology plays a crucial role in the performances of devices. Among semiconductor technologies, the bulk substrate presents a small resistance of $10\Omega \cdot \text{cm}$ compared to III-V and SOI technologies. This resistance, which is not constant, is strongly dependent on the doping process. This characteristic involves a substrate coupling with essential losses for passive devices. Two phenomena can explain this coupling: a capacitive

coupling between conductors and the substrate due to the injected current and the appearance of eddy current in the magnetic field [45]. In the case of integrated circuits, these currents inserted into the substrate tend to couple with other passive and active structures. Figure 3-48 illustrates the substrate-crossed coupling effects of an integrated circuit. These couplings cause the stability issue and the gain degradation of transistors. The direct injection is due to the Hot Carrier Injection Effect [46] (Appendix B – “Reliability of Power Amplifier”). The capacitive coupling is present in high frequencies when the PN junctions or oxides behave as the short-circuit capacitor in RF. The suitable choice of routing techniques and the signal mode is necessary. As a result, the use of differential signal mode is performed in all transformers of this work to reduce these two mentioned effects.

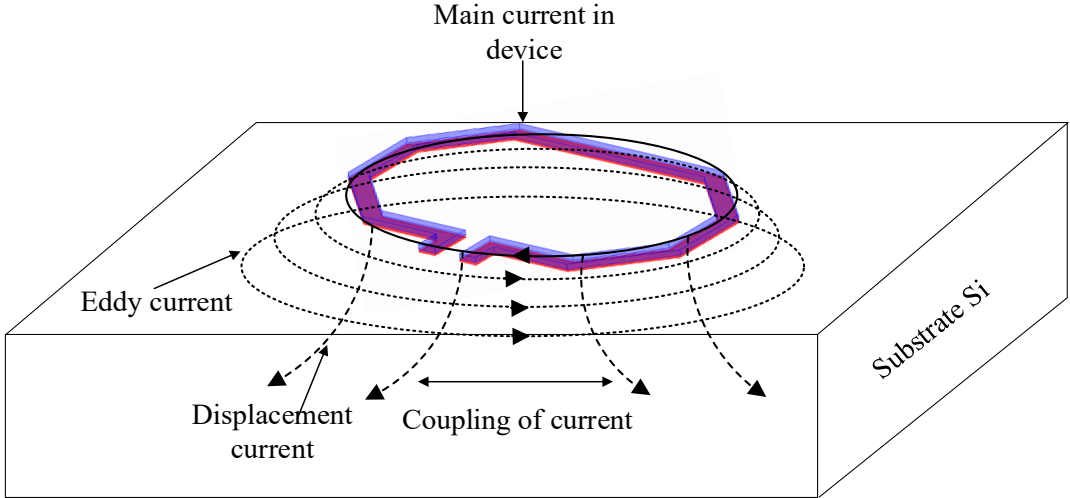


Figure 3-48. Eddy effects in integrated circuits and the substrate-crossed coupling

3.3.5 Electromagnetic simulation and optimization

Electromagnetic (EM) simulators present a powerful tool to evaluate the behavior of passive components. They provide a precise approximation of devices for technological properties. EM simulators are categorized based on the field calculation methods, which have an impact on how 3D devices can be treated. There are two groups of simulators that are widely used in RFIC and MMIC: planar 3D (often referred to 2.5D) and full 3D. The former provides adequate results and does not require substantial computational resources. Otherwise, the latter enables the best accurate EM approximation effects on devices, but requests a significant amount of memory. For the modeling purposes of this work in radiofrequency, the planar 3D is a suitable choice.

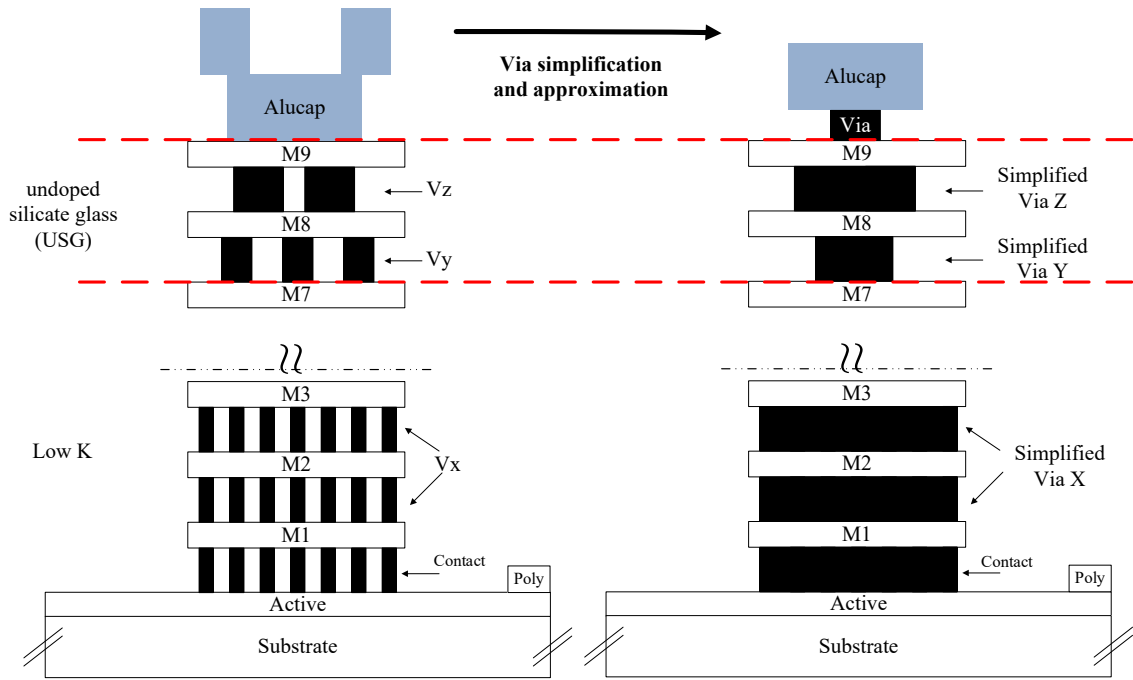


Figure 3-49. A 65nm CMOS BEOL structure and its layout simplification in Momentum

Among the available 3D-planar commercial tools, Momentum of Agilent Technologies is “the leading 3D planar electromagnetic simulator used for passive circuit modeling and analysis” [47]. This tool uses frequency-domain Method of Moments (MoM) technology to simulate complex EM effects accurately. Momentum also takes into account coupling and parasitics to approximate the simulated results correctly. Precise simulation facilitates RF/MMIC designers to improve design performance and confirm the specifications of real products. Momentum is integrated with Advanced Design System (ADS) and the third-party tools from Cadence, for example, Virtuoso. Figure 3-49 illustrates a real structure and its equivalent approximation used in Momentum. This method allows enhancing simulation speed. The simulation approximations in Momentum are explained by three points:

- Substrate merger: there are more than 20 dielectrics stacked vertically in the 65nm CMOS back-end-of-line. The simulator classifies the technology into three equivalent dielectrics to speed up the simulation. The first one is used for the thin metal levels. The second one is for the top-metal levels. The last one is used for the passivation layer. The equivalent dielectric is calculated from two adjacent ones by using the Kraszewski’s equation [48].

$$\xi_{eq} = \left[\sqrt{\xi_n} + \frac{h_{n-1}}{h_{n-1} + h_n} \cdot (\sqrt{\xi_{n-1}} - \xi_n) \right]^2 \quad (3.60)$$

- Via merger: a single via has the most extensive area of 4mm² in case of the top metal M9. It is much smaller than a size of devices. Also, many single vias placed side by side ensure low-resistive interconnections. For that reason, the simulator can cluster vias in the group and form a unique block without changing the performance. The via merger helps saving

simulation resources. The equivalent via is expressed by the simplified via-X, via-Y, and via-Z as shown in Figure 3-49.

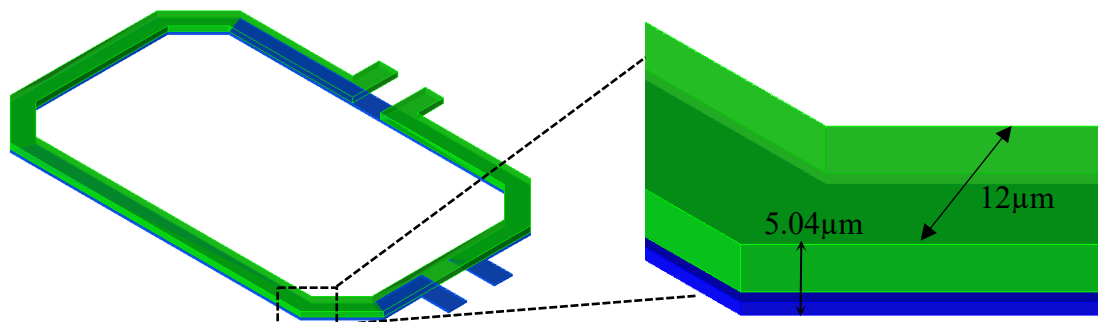
- Alucap simplification: Momentum assumes the alucap's shape is rectangular with the same area to maintain the same performances.

3.3.6 Model design

Electromagnetic simulation of integrated transformers provides a matrix of scattering parameters, which is cumulated with the output results over the swept frequencies. This matrix contains necessary information about reflection and transmission at the terminals of components. This subsection details the model design of distributed active transformers from the design of unit winding to the assembly of multiple ones. The above analyses demonstrate the advantage of the stacked orthogonal 90°-rotation unit transformer for this work. Hence, this type of transformer is chosen for unit transformer design. The questions are the number of stacked metal layers to build the secondary windings and the number of needed windings to build a global transformer. For the second one, four case studies of four different numbers of windings are investigated.

3.3.6.1 Design of elementary winding

For the first question, four cases of the number of stacked layers are also reported to design unit windings. They are four designs with the same top metal M9 for the primary winding and four cases of stacked metals for the secondary winding. They are one with the metal level M8, one with two stacked layers (M7 and M8), one with three stacked layers (M6, M7, and M8) and the last with four stacked layers (M5, M6, M7, and M8). Figure 3-50 illustrates four case studies. Also, the number of vias and the number of stacked layers must ensure the reliability of DC and AC Cu metal current density (EM) specification, which is detailed in Appendix B - Reliability of power amplifier.



a) Case 1 - One metal level for the secondary winding

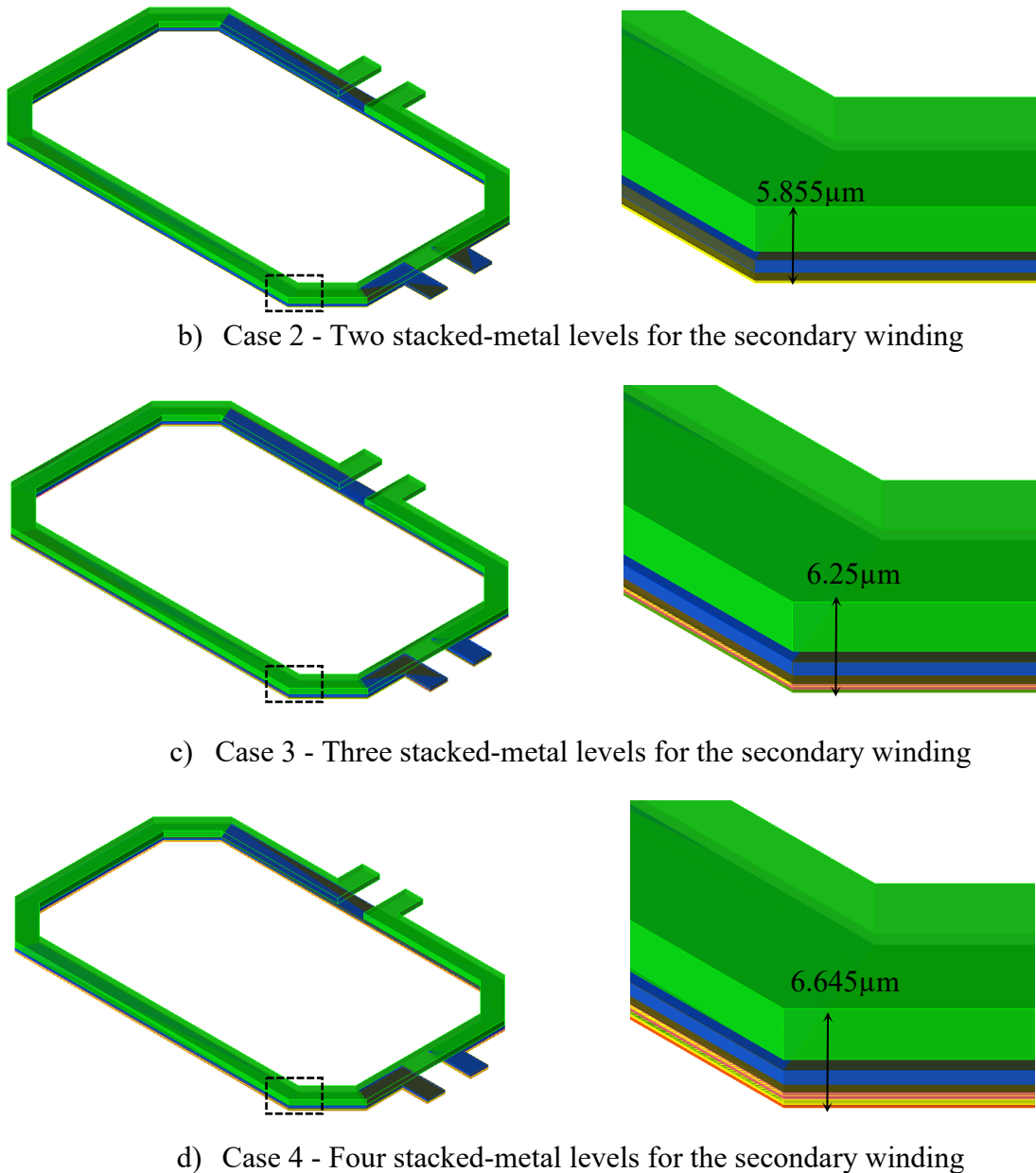


Figure 3-50. Four case studies for the design of unit winding

In practice, the port 1 in Figure 3-51 has an impedance of Z_{opt} that describes the optimal impedance of the unit power cell. This impedance is measured by the load-pull method. The unit transformer aims to convert the optimal impedance to a given load Z_{load} with the highest transformation efficiency. In simulation, two impedances are set under 50Ω . Four case studies use the same configuration of impedances of 50Ω to exhibit the performance comparison.

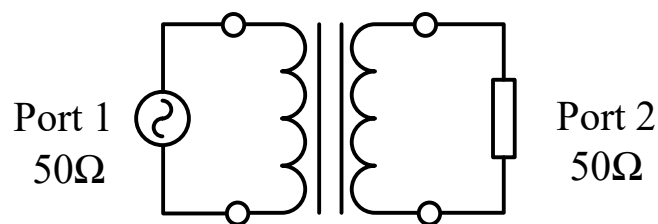


Figure 3-51. Simplified two-port simulation setting used for the unit transformer design

Table 3-1. Maximum DC and AC currents on two windings for four case studies

Case study	Number of stacked layers	Max. DC current (mA)		Max. AC current (mA)	
		Primary	Secondary	Primary	Secondary
Case 1	1 (M8)	361.5	96.99	155.4	86.78
Case 2	2 (M8-M7)	361.5	119.48	155.4	132.79
Case 3	3 (M8-M7-M6)	361.5	141.97	155.4	182.39
Case 4	4 (M8-M7-M6-M5)	361.5	164.47	155.4	236.8

Furthermore, the DC and AC current densities of metal layers are crucial for the reliability of the transformer. Table 3-1 summarizes the maximum DC and AC currents on two windings for four case studies. Four transformers use the same width of 12 μ m for both coils. The more significant number of stacked metal layers is obtained when the higher maximum DC and AC currents are achieved. The specifications of the power amplifier, mentioned in chapter 2, require producing a peak output power of 1W at the load of 100 Ω and operating under a supply voltage of 3.3V. Indeed, transformers form a DC inter-winding decoupling. By using a quantitative analysis based on these specifications, the calculation of required levels for DC current in the primary winding and AC current in secondary winding can be accomplished. Maximum DC current must be superior to 303mA for the primary winding whereas the required maximum AC current in the secondary coil is 100mA. For that reason, case 1 with one metal layer for the secondary coil is not chosen to design the unit transformer. The performances of four transformers are reported below. The inductances in Figure 3-52 and the quality factors of four transformers in Figure 3-53 do not vary greatly.

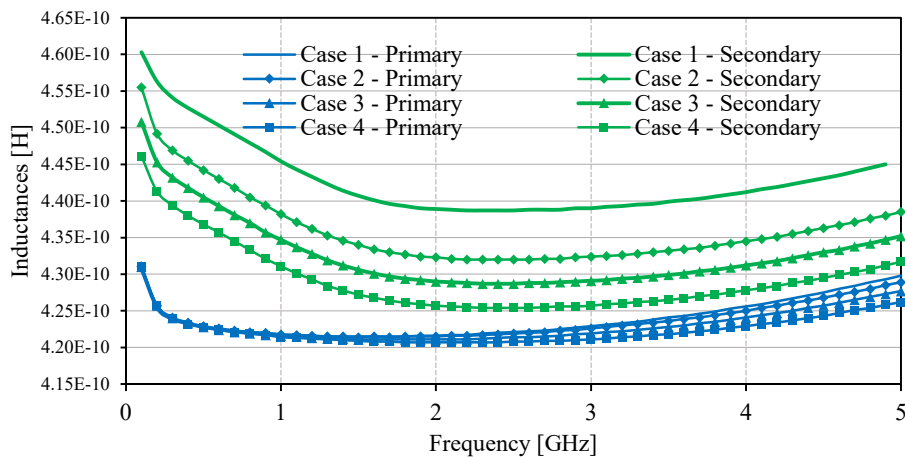


Figure 3-52. Simulated inductances of four case studies in Table 3-1

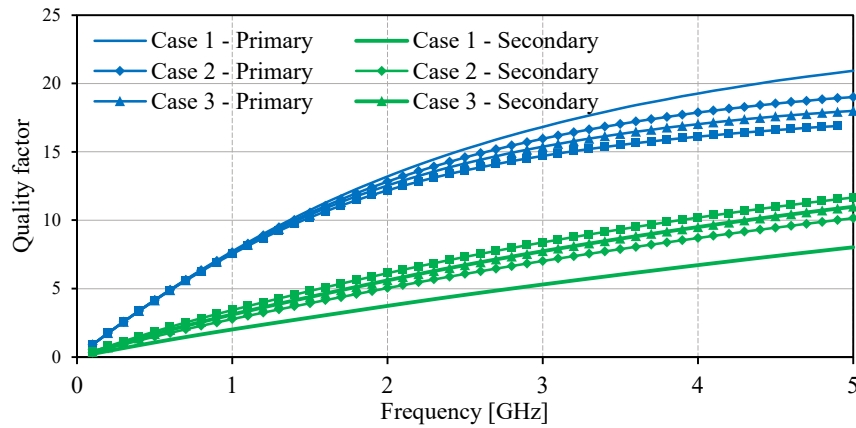


Figure 3-53. Quality factors of four case studies in Table 3-1

Figure 3-54 illustrates the coupling coefficients of four transformers. The simulation results demonstrate the maintenance of k -coefficient between 0.83 and 0.84. That ensures the efficient operation of transformers. Additionally, the AC current in the secondary winding in practice is higher than the theoretical one. Therefore, it is needed to maximize this current level without affecting the transformer performances. Through above results and analyses, the stacked four-metal transformer is taken into account for the unit transformer design to minimize the probability of failure mechanism of the power amplifier.

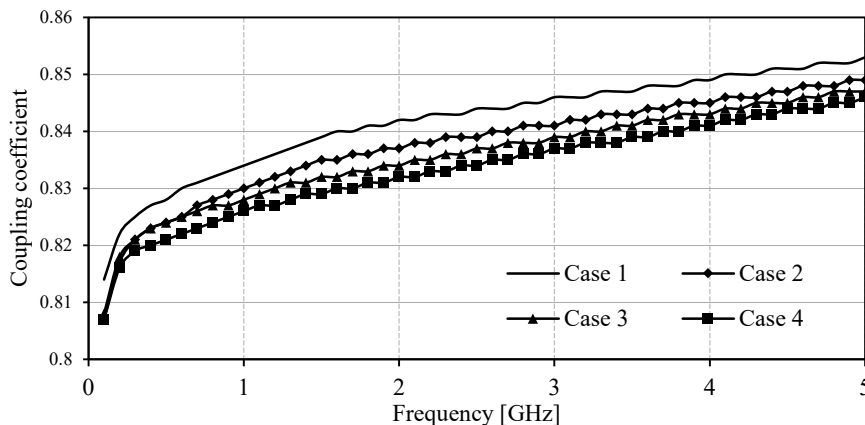


Figure 3-54. Coupling coefficients k of four case studies in Table 3-1

The unit power cell under a DC source of 3.3V is designed in differential mode to be compatible with the unit transformer. For that reason, the reuse of the primary winding of the transformer to supply the unit cell is assimilated into this work. The feeding line is integrated into the primary winding as a part of the transformer. The drawback of this utilization is the impact on the coupling effect of the transformer. Figure 3-55 depicts two concepts of transformers. The first one is the integration of feeding line into the primary coil with the four-stacked-metal secondary coil. The second one is the conventional transformer with the classic design of the top metal for the primary and four metals for the secondary. The two transformers have the same size of $481\mu\text{m} \times 209.3\mu\text{m}$.

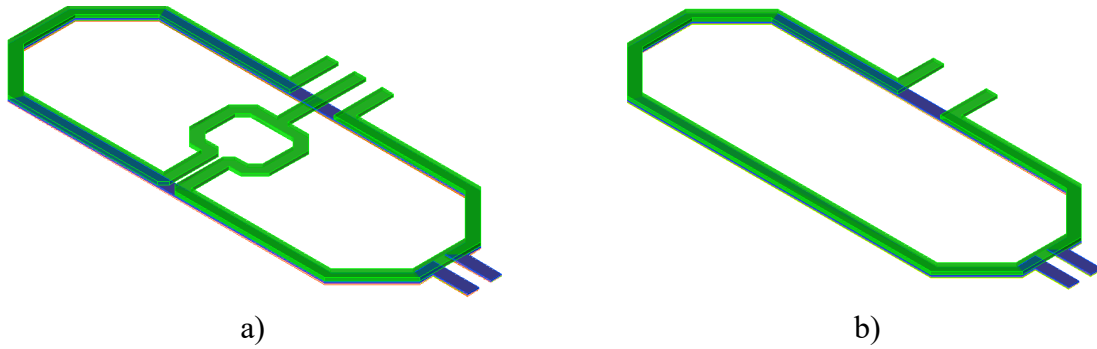


Figure 3-55. Two concepts of transformers: a) With the feeding line b) Conventional

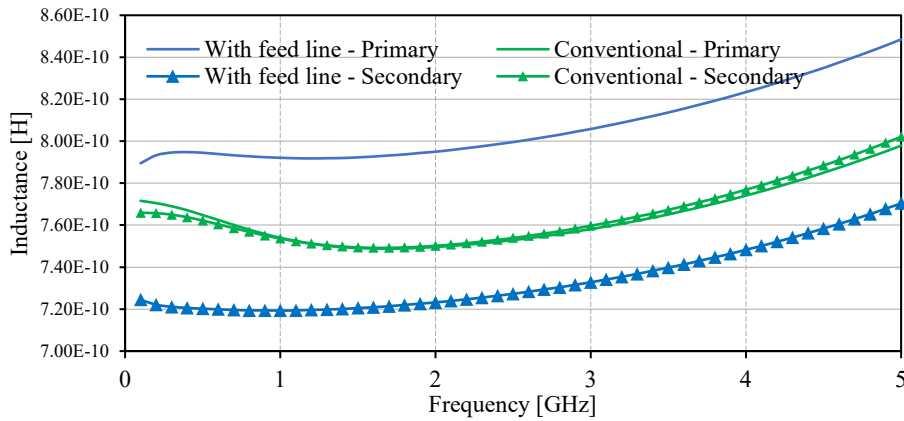


Figure 3-56. Inductances of two concepts of the transformer

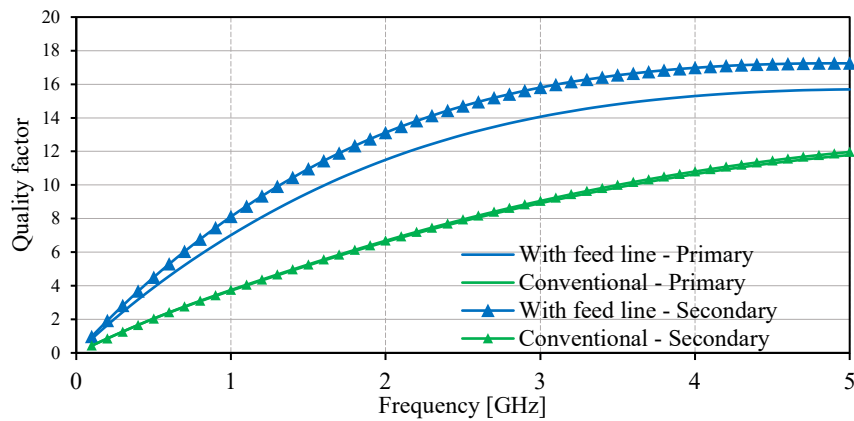


Figure 3-57. Quality factors of two concepts of the transformer

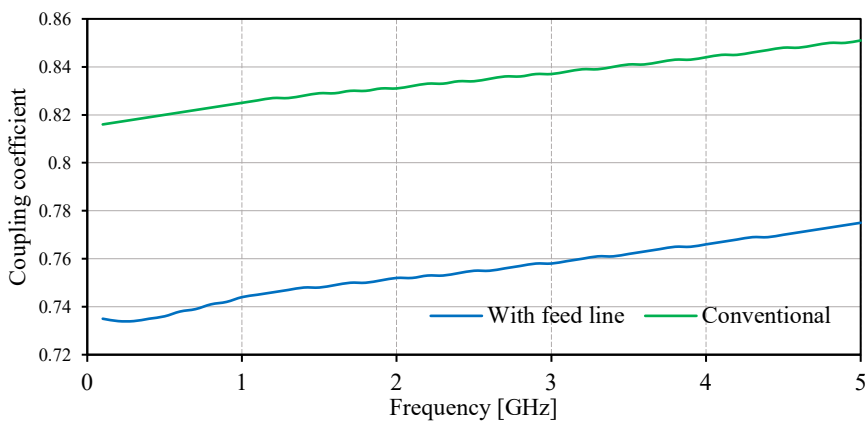


Figure 3-58. Coupling coefficients introduced by two concepts of the transformer

Figure 3-56 to Figure 3-58 illustrate the performances of two concepts of the transformer. The inclusion of the feeding line has a slight impact on the transformer performances. The primary inductance is increased but the secondary one is not greatly changed. This influence is explained by the greater length of the primary coil and the mutual inductance reducing the secondary inductance. On the contrary, the transformer with the integration of a feeding line achieves higher quality factors thanks to the more significant stored energy on the more extended primary coil. As aforementioned, the coupling factor is also affected by this integration due to an exposed no-coupling area inside the primary coil. The value of the coupling coefficient decreases to 0.76. A capacitor is then connected in parallel with the primary coil as detailed in the subsection 3.3.3.2.2 to compensate this loss.

3.3.6.2 Assembly of elementary windings

The design concept of the unit transformer is identified in the previous subsection. To answer the second question about how many unit windings are required, this subsection takes four case studies of four different numbers of winding into consideration. They are one-winding, two-winding, three-winding, and four-winding concepts. Due to the limited die area below 4mm² required by the manufacturer, the cases of more than five windings are not reported in this work. Each transformer concept depicts its advantages and drawbacks. The choice of a suitable one depends on two elements, the operating-mode support capability and the impact on the performances of the power amplifier.

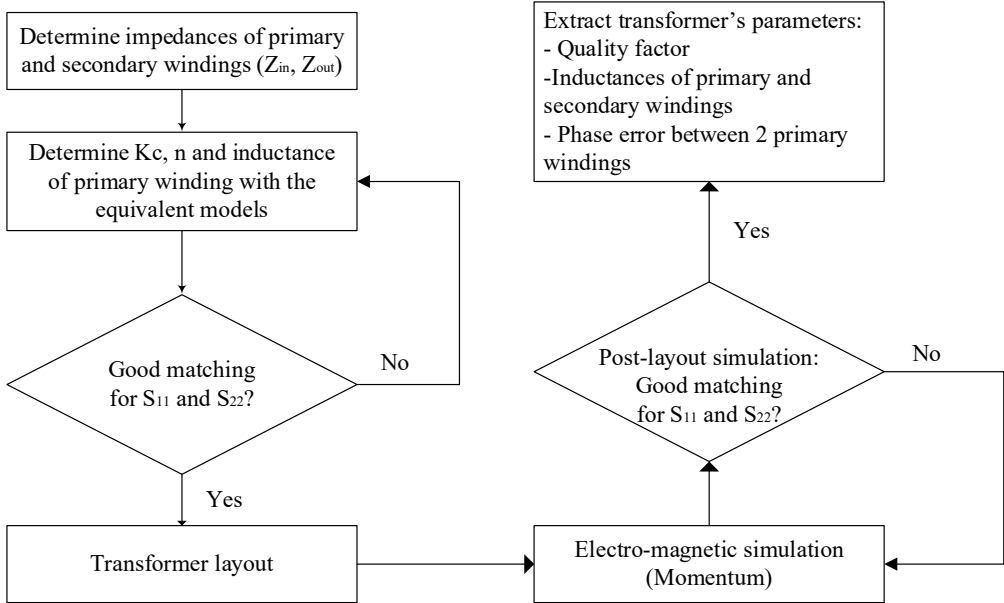


Figure 3-59. Flowchart of transformer design

Figure 3-59 details a process of transformer design. First, the optimal output impedances Z_{opt} of the power cell are determined by the load pull method. After identifying this value, the transformer design is carried out. As mentioned in 3.3.4.2, the output of the transformer has a

load of 100 Ohm designed in differential mode to reduce the substrate loss. Therefore, the transformer allows converting the impedance of 100 Ohm to the optimal impedance Z_{opt} presented by each power cell and modulating the impedance of power cells in function of the number of active cells. Also, it plays the role of power combiner. Circuit designers determine the critical parameters of a transformer by simulation, namely the coupling coefficient, turn ratio and inductances of each winding as performed in the last subsection. This process is finished with the transformer layout after achieving the proper matchings at the input and the output. In four concepts, the unit winding design uses the feeding line to provide the supply connection for power cells. This integration degrades the coupling effect slightly but facilitates the layout of the global architecture, including the interconnections between the transformer and the power cells.

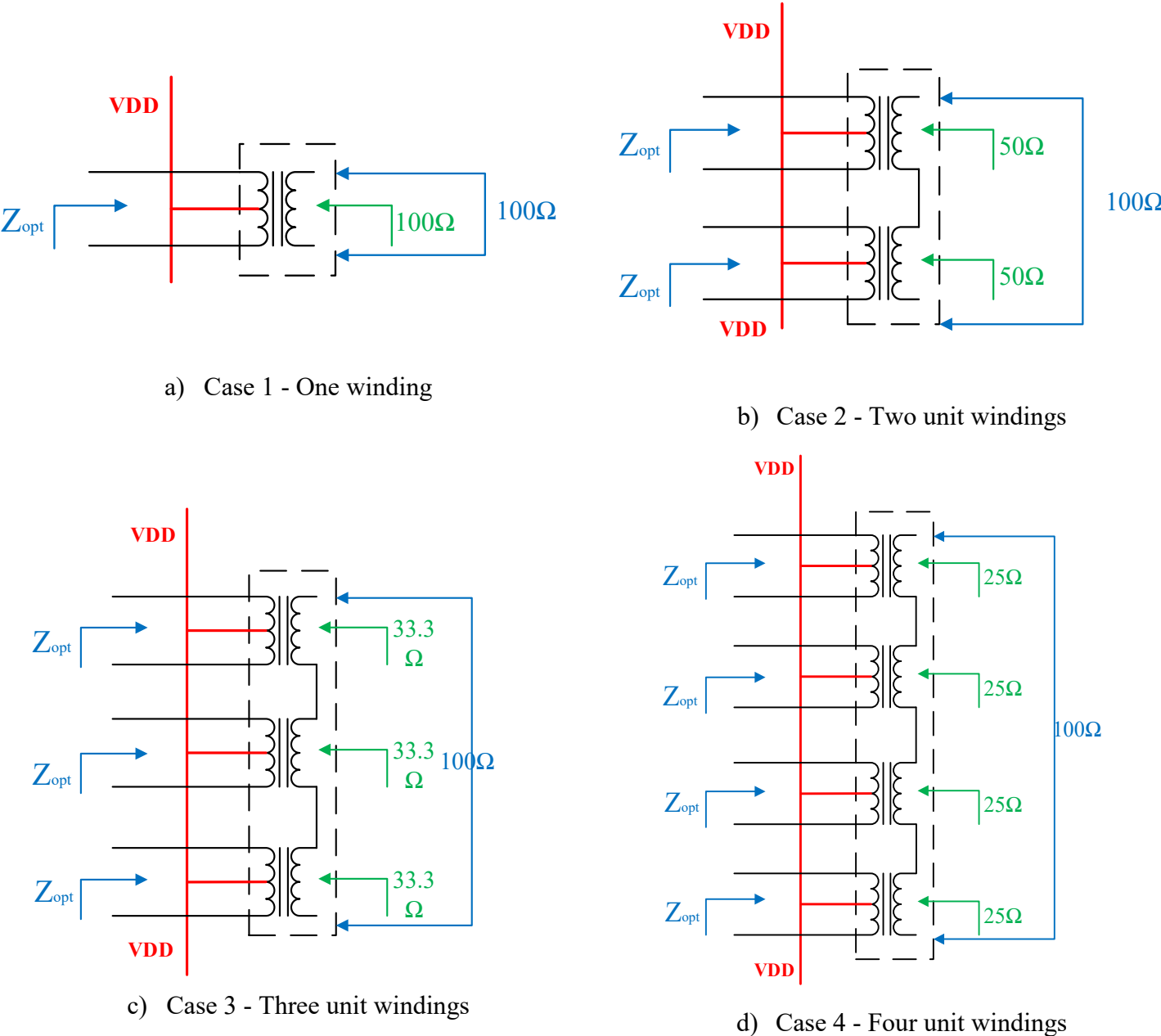


Figure 3-60. Impedance transformation in four case studies

Figure 3-60 details the impedance transformation of four case studies. Assuming that a distributed active transformer composes of N unit transformers, the differential charge 100Ω is hence divided into $100/N$ for each unit transformer if assuming the identical design for unit windings. To perform the impedance transformation, the transformer design necessitates critical mechanical settings such as transformer diameter, turn ratio and the number of stacked metals. For four case studies, these mechanical parameters are identical. The simulation setting of these case studies uses the identical 50Ω -impedance setting for input ports and output port to extract the desired parameters.

Figure 3-61 depicts the layout of the four case-study transformers. The diameter is $169\mu\text{m} \times 1886\mu\text{m}$. The turn ratio of unit winding equals one. Thanks to two thick top-most metals provided by the 65nm CMOS technology, the primary winding having a high DC current density is designed with the top metal M9. The secondary windings are chosen with four stacked levels from M5 to M8. The trace width is $12\mu\text{m}$, the maximum value authorized by Design Rules Check to minimize the resistive losses. For each winding, the design topology is chosen with the hexagonal concept. Another crucial parameter of the transformer is the insertion loss. This parameter is measured by setting up the test bench with the exact optimal impedance at the input and the desired load at the output. This test bench will be detailed in the next section to explain the design of this reconfigurable PA.

Table 3-2. Overview of the characteristics of four case-study transformers

Number of unit windings	Output impedance of unit winding	Mode configurability	Coupling effect of unit winding	SRF
1	100	+	++++	+
2	50	++	+++	+++
3	33.3	+++	+++	+++
4	25	++++	+++	+++

Figure 3-62, Figure 3-63 and Figure 3-64 illustrate the performance of the four case-study transformers. As shown in these figures, the case-1 transformer exhibits a low self-resonance frequency for both coils. This aspect with a low-range operation in frequency can result in some stability issues for the power amplifier. Three other cases depict the proper performances about quality factors and inductances despite their medium coupling coefficients.

Table 3-2 outlines the advantages and drawbacks of each case study. Among them, case 3 and case 4 exhibit the most reasonable impedance transformation ratio. Since the optimal impedance of the power cells moves around 30Ω to ensure the robustness transistor, these two case studies demonstrate the specific interest in designing transformers about the flexible mode

configurability. The three-winding transformer potentially makes the output signal unbalanced in case of turning off one of the three corresponding power cells. The four-winding transformer, in somehow, can answer this problem by cutting off two of four power cells. For that reason, a four-winding transformer is preferred to design transformer in the power cell switching technique.

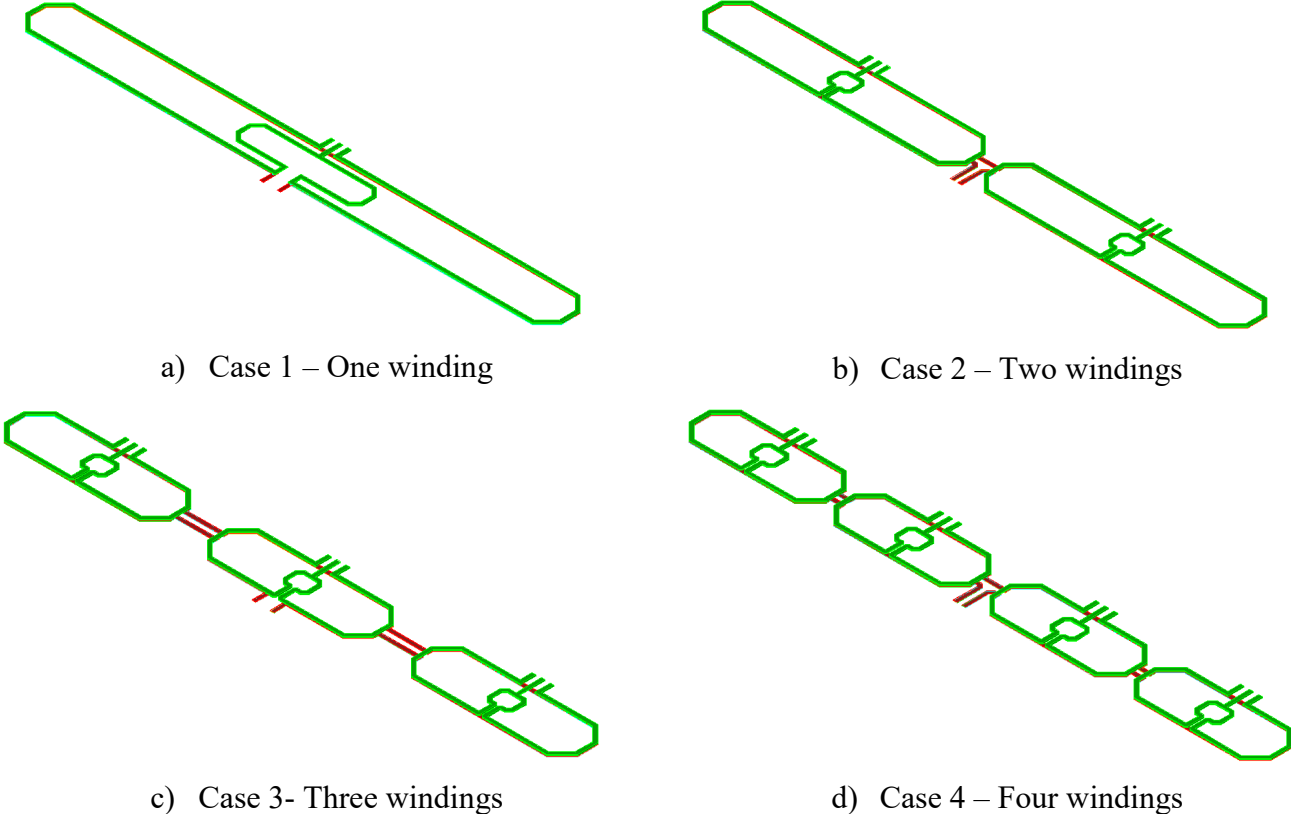


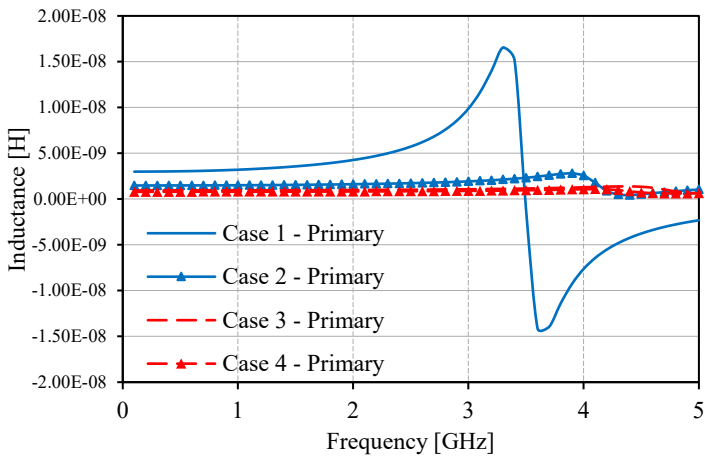
Figure 3-61. Layout of four case studies of distributed active transformer

To sum up, the design concept of the distributed active transformer is chosen with four windings by the criteria below:

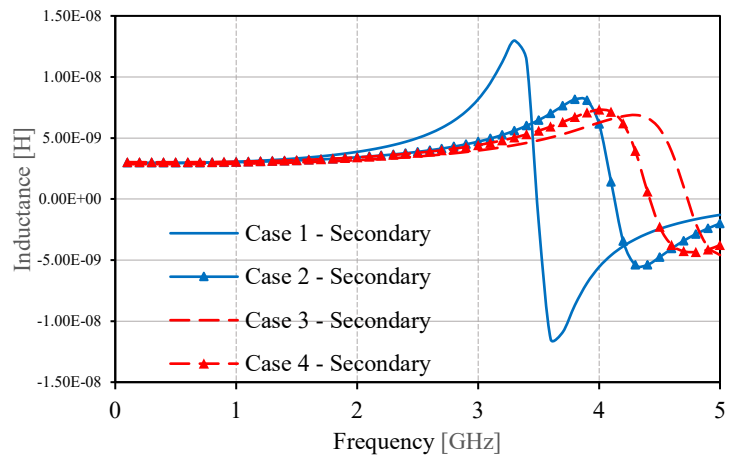
- The high operating-mode configurability with four possible power modes,
- The capability of maintaining the output differential voltage swing if power cells are off,
- The reasonable performances in inductances, coupling effect, quality factors compared with other types,
- The compact layout.

The chosen concept of transformer demonstrates an innovated solution to configure the PA’s operation in multiple modes and maintain the proper impedance matching between the power cells and the transformers. Furthermore, the stacked-metal design allows the transformer to ensure the reliability of the transformer under any circumstances of DC or AC currents.

The thorough design of power-combining transformer used in this work will be presented in the following chapter.

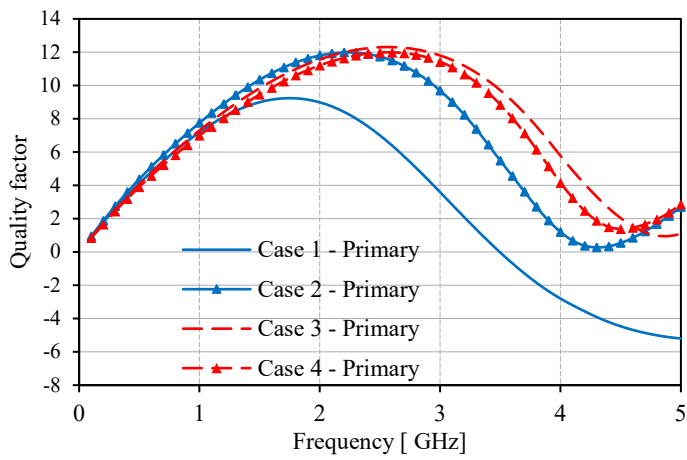


a) Inductances of primary windings

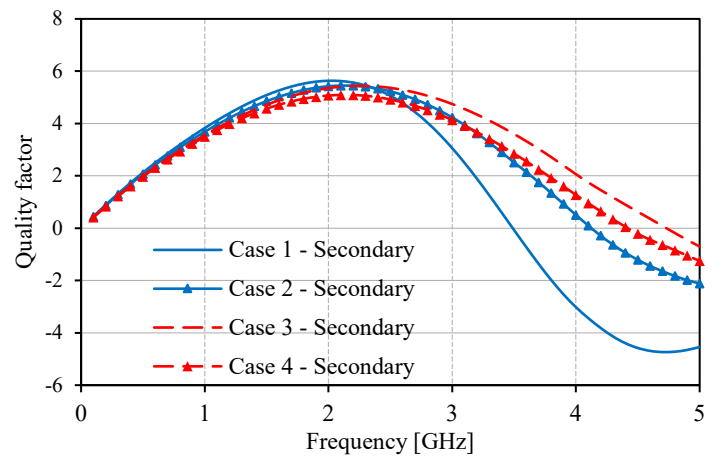


b) Inductances of secondary windings

Figure 3-62. Inductances of transformers in four case studies



a) Q-factor of primary windings



b) Q-factor of secondary windings

Figure 3-63. Q-factors of transformers in four case studies

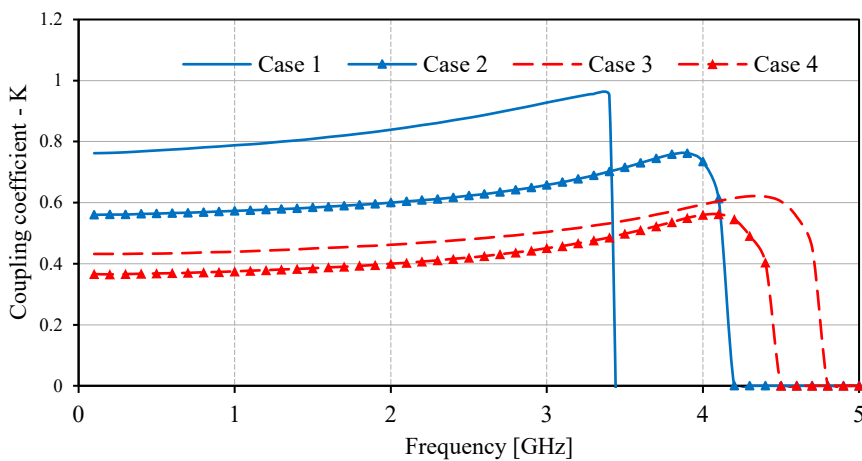


Figure 3-64. Coupling coefficients in four case studies

3.4 I/O pads

3.4.1 Pads design

I/O pads are the access structure of the integrated circuit [49]. To assure the proper contact with the external environment, namely measure points, bump and other elements, the pads have

the constraints of the necessary area. The foundry fixes the minimum aperture of passivation. These dimensions result in parasitic capacitances C_{pad} , considering that this kind of capacitances relates to the pad area S_{pad} , the thickness of pads $h_{dielectric}$ and the dielectrics permittivity ϵ_r , as illustrated in the equation (3.61).

$$C_{pad} = \epsilon_0 \epsilon_r \cdot \frac{S_{pad}}{h_{dielectric}} \tag{3.61}$$

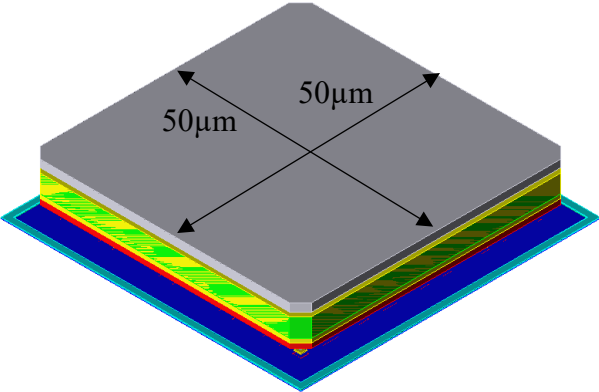
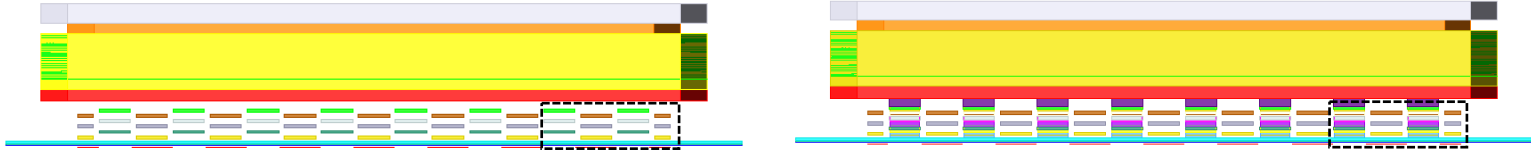


Figure 3-65. RF pads provided by the 65nm CMOS technology

The 65nm CMOS technology provides a single model of RF pads with the size of 50µm x 50µm. This model is purpose-built for the RF and DC signals. Therefore, it is necessary to build a pad model for GND plot. This model is designed with the same structure as the RF pads with inter-metal vias to obtain a straight connection from aluminum to substrate and connect to GND signals as shown in Figure 3-66. Electromagnetic simulations are necessary to take into account all inductive and resistive parasitic effects on metal layers and capacitive couplings with the ground plane or the substrate. The equivalent capacitance C_{eq} can be extracted directly from the equation (3.62).

$$C_{eq} = \frac{Im(Y_{11})}{2\pi f} \tag{3.62}$$



a) RF pads without inter-metal vias b) GND pads with inter-metal vias to the substrate

Figure 3-66. Cross-section view of a) RF and b) GND pads

The parasitic capacitances of two pad models are depicted in Figure 3-67. The simulated capacitance is 37.21fF for RF pads at 2.5GHz.

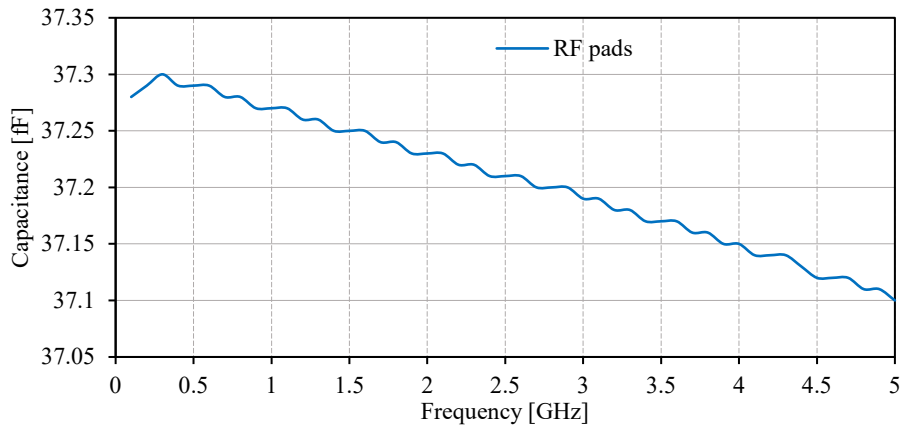


Figure 3-67. Equivalent capacitances of RF pads

There are two typical types of pads structure used for on-wafer measurement: Ground-Signal-Ground and Ground-Signal-Ground-Signal-Ground. The former is used for the single-ended signal with an impedance of 50Ω . The latter is used for the differential signal with an impedance of 100Ω . The second one is also the pad structure used in this work. The center-to-center pitch of two adjacent pads requires precisely $100\mu\text{m}$.

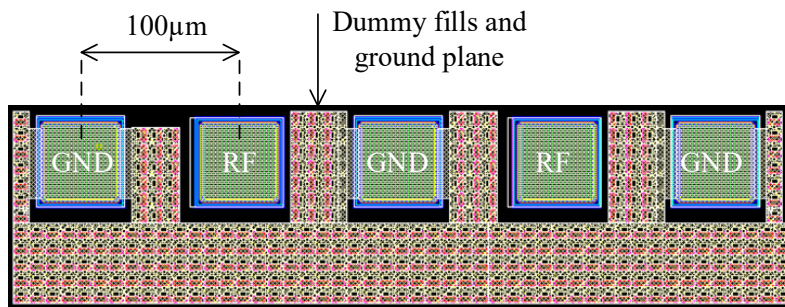


Figure 3-68. G-S-G-S-G pads structure for differential signals

3.4.2 Electrostatic Discharge (ESD) Protection

Electrostatic Discharge (ESD) coming from the external environment can damage an integrated circuit. An ESD protection circuit based on diodes, as shown in Figure 3-69.a is widely used for I/O pads, including RF and DC pads.

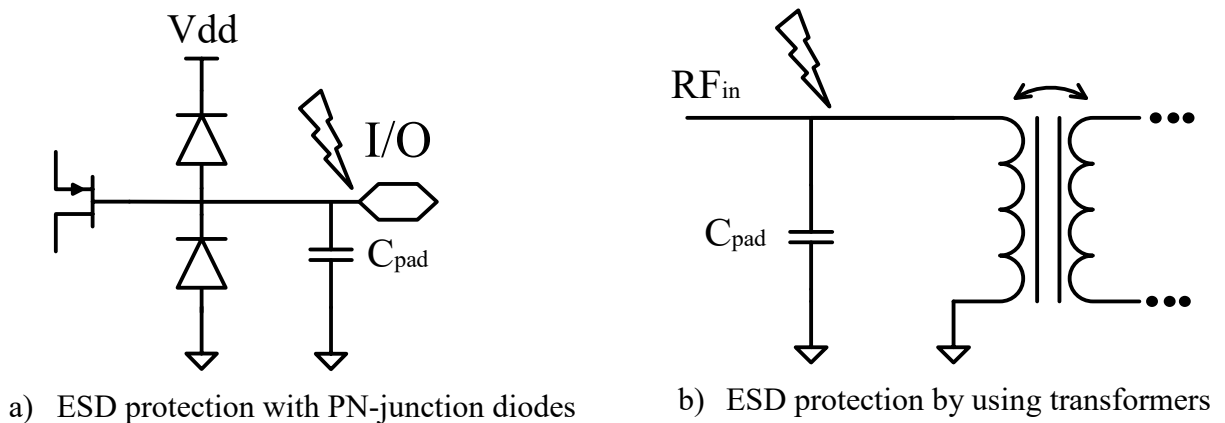


Figure 3-69. ESD protection used in radiofrequency

Also, other structures of ESD protection circuit are being developed to use in developing applications, especially in millimeter-wave circuits. Among these structures, an ESD protection concept using transformers is widely used for differential or single-ended signals. This work engages these two types of ESD protection to ensure the viability of the power amplifier.

3.5 Conclusion

The parasitic elements in radiofrequency affect the performances of passive circuits. With the skin effect, currents tend to conduct at the surface of conductor since magnetic fields penetrate the conductors and produce opposing electric fields within the area of conductors. At 2.5GHz, the skin depth is only 0.38 μ m. The current return path can be resistive and inductive; it degrades the performances of passive circuits. Moreover, the coupling with the substrate is also problematic since the current injection into the substrate couples two adjacent components.

Power combiners consist of three main categories: current combiners, couplers, and transformers. Among them, transformers exhibit the suitable characteristics for this work with the high operational configuration and the proper robustness. An in-depth study of electrical and mechanical features of transformers is also performed. Power-combining transformers are categorized into two types: serial combining (SCT) and parallel combining (PCT) transformers. The fundamental analyses of impedance modulation and transformation efficiency are reported. SCT demonstrated advantageous behaviors towards the reconfigurable power amplifier applications. Then, this chapter presents the design guide of unit transformer by comparing several mechanical possibilities of unit-transformer design. Loss mechanisms have a significant impact on transformer performances. Several layout techniques show the capacity of reducing losses of transformers. The design and optimization are performed under Momentum. The analytical approximations of this tool are reported. A detailed comparison of stacked metals and the number of unit windings is performed to choose the most suitable transformer concept.

The selected four-winding four-stacked-metal transformer proposes a promising solution with the appropriate characteristics of a power-combining transformer for power cell switching applications. The transformer implemented in this work not only allows the PA to operate in multiple power modes but also reduces the impedance mismatch between the power cells and the transformer. Besides, the transformer introduces a balanced output swing that helps increase the linearity of the PA.

I/O pads are essential for integrated circuits. The design of GND pads as one of the entries for circuits is carried out along with the RF pads. The G-S-G-S-G pad structure is purposeful for differential signals. This chapter ends with the pad modification for GND pads and the ESD protection circuit for the power amplifier.

4 REALIZATION OF THE 4G LTE RECONFIGURABLE POWER AMPLIFIER

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In this chapter, the fully integrated reconfigurable multi-mode 65-nm CMOS power amplifier is presented. It is the first time that a power amplifier with the segmented bias technique and the power cell switching (PCS) technique is designed and fabricated on the CMOS technology. The operation of the PA is defined according to the level of output power to reduce the thermal dissipation and enhance the efficiency. A stacked transformer is designed based on distributed active transformers to implement the PCS technique. The segmented bias technique is realized by two cascade bias-different transistors to adapt to the linearity requirements. Two bias voltages and two supply voltages thus define the operating mode.

4.1 Design methodology

4.1.1 Flowchart of circuit design

The operating range of RF systems targets from ten to hundreds of meters. Such systems require generating high output power, often exceeding 20dBm. Also, a small amount of bandwidth is available at RF frequencies. For that reason, systems tend to store more bits per hertz by using high-order modulation to increase data rates. As mentioned in Chapter 2, the OFDM technique is frequently used in the LTE standard. As the average power of LTE 4G requires around 23dBm and the peak-to-average power ratio reaches high levels such as 7dB, the power amplifier needs to move backward in output power to operate more linearly. To release such burden on preserving signal integrity, the saturated output power of power amplifiers must reach 30dBm for the transmitter. Therefore, the power amplifier must be designed to achieve the watt-level output power.

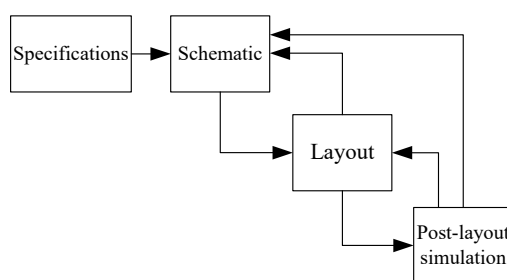


Figure 4-1. A general flowchart of the power amplifier design

Figure 4-1 depicts the general flowchart of the power amplifier design. The PA specifications are identified in Chapter 2. The next step is sketching the schematic of the PA. The schematic describes a detailed view of the PA's architecture and gives circuit designers pre-layout results. The layout is taken place in turn with many constraints that require being satisfied. Post-layout simulations will be performed after layout to confirm pre-layout results. If post-layout simulations satisfy the specifications of PAs, the layout will be finished before sending to the foundry.

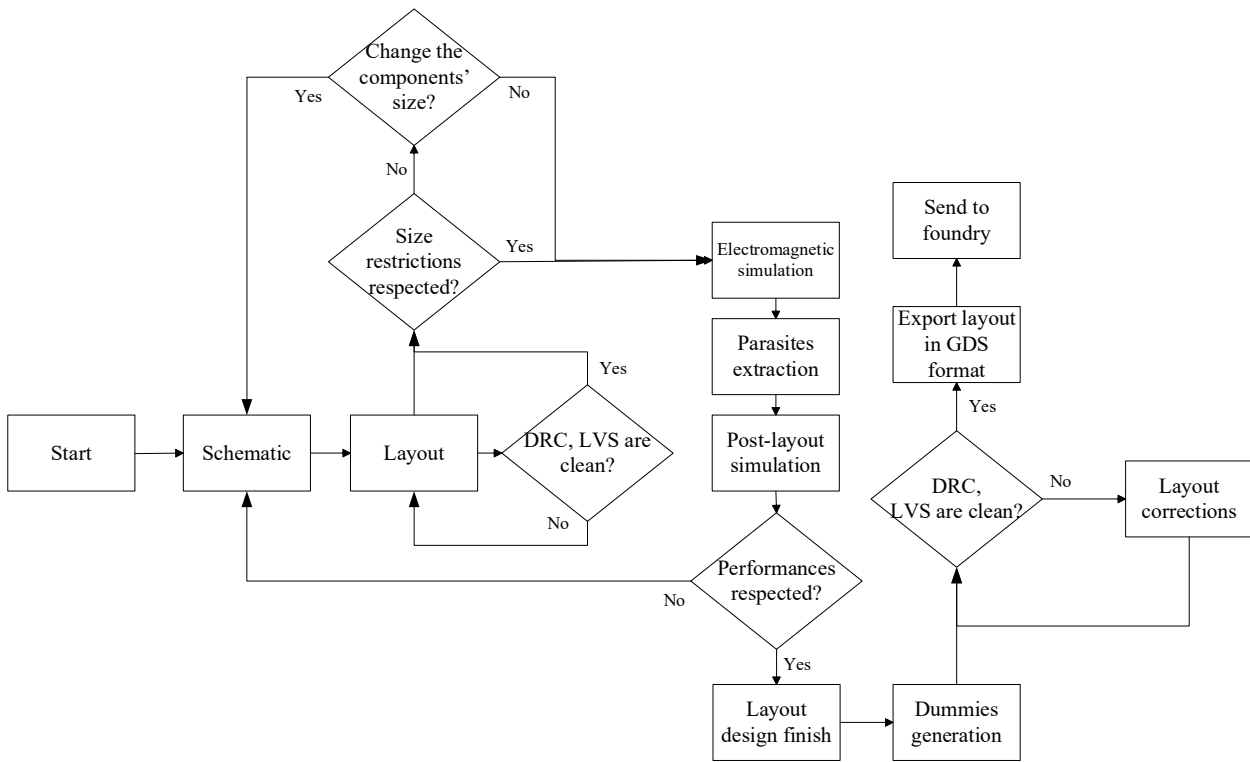


Figure 4-2. Detailed design flow of this 4G LTE power amplifier

Figure 4-2 demonstrates the detailed flowchart of the design of the 4G LTE power amplifier. The power amplifier requires being integrated on the 65nm CMOS technology. Due to the limited size of the fabricated die, the size of the fully integrated PA is restricted below 4mm^2 . The pre-layout results are extracted if the design rules check (DRC) and the layout versus schematic (LVS) verifications are validated. The critical components are simulated in the electromagnetic field by Momentum to perform parasitic extraction inside the circuit. All of the parasitic elements are taken into consideration to execute post-layout simulations. Post-layout simulations are finished only if the restrictions of performances and sizes are respected. Dummy fillings are due to assist planarization of multi-dielectric layers by chemical-mechanical polishing (CMP) process [50]. Floating dummy metals are inserted into chip surface; otherwise, the technique can degrade the performances of the full design. Therefore, another step of DRC and LVS verifications is expected with possible layout corrections to accomplish the design. The last step is exporting the full layout in GDS format and sending it to the foundry. During the design procedure, there are some mask layers added to the layout to meet the fabrication restrictions. The TSMC fabrication service is provided by IMEC, Leuven, Belgium.

Figure 4-3 presents design steps to define transistors' bias and a detailed topology of the power amplifier. The PA operating class is determined according to the design target. The main innovation of this design is the combination of two different power classes to develop the segmented bias technique. The detailed topology of power cells is identified to address the requirements of the chip size and the high output power. The next stage will present the

comparison of four possible topologies to design power cells. The chip cost also increases with a more complicated topology, from the common source to the differential cascode structure. It is also important to note that more transistors are built in power cells, more parasitics elements are induced in interconnections. An in-depth consideration is thus required to minimize these parasites during the design process.

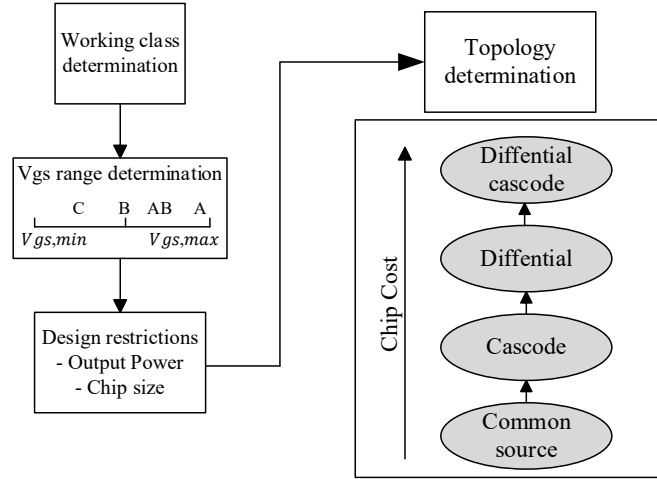


Figure 4-3. Determination of power amplifier topology based on power classes

4.1.2 Segmented bias technique

Thanks to the outstanding advantages of class AB for linearity and class C for efficiency, these power classes are chosen to implement the segmented bias technique. The topology of the technique is depicted in Figure 4-4. These two biases determine the operating class of the power cell. The size of two transistors is also a critical factor of this technique. We consider these two cascade transistors as one equivalent transistor in the conventional design. The total size of two bias-segmented transistors is W/L . The size of each bias-segmented transistor is chosen based on the performance of the power cell. The optimal choice is that the size of the class-C transistor ($2W/3L$) is two times larger than that of the class-AB transistor ($W/3L$).

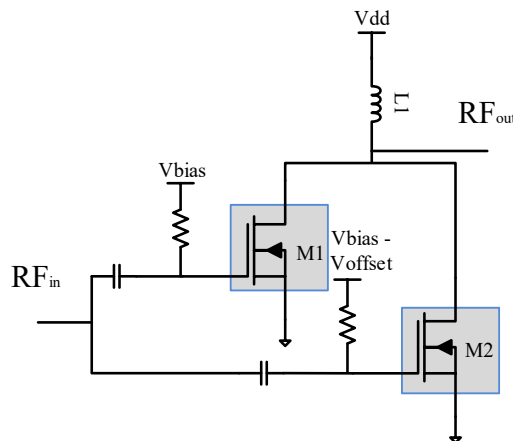


Figure 4-4. Segmented bias used in power cells

A simple simulation of the segmented bias technique is executed. The class-AB transistor M_1 has a size of $768\mu\text{m}/0.06\mu\text{m}$ and a bias $V_{bias} = 0.6\text{V}$ and the class-C transistor M_2 has a size of $1.536\mu\text{m}/0.06\mu\text{m}$. The voltage V_{offset} is swept from 0.1 to 0.4V to vary the bias of the transistor M_2 . The optimal values of V_{offset} are from 0.25V. It is noted that the threshold voltage is 0.4V. If V_{offset} increases, the transistor will move deeper into the cut-off region. The operating class of this transistor is hence a deep class C. When the class-AB transistor penetrates into the saturation region, the other one starts to induce power. When the main transistor reaches its peak power with class AB, the auxiliary one continues to work until its saturated point. Hence, the power cell composed of two transistors can achieve a higher and more extended gain, reduce AM-AM distortion and increase back-off efficiency.

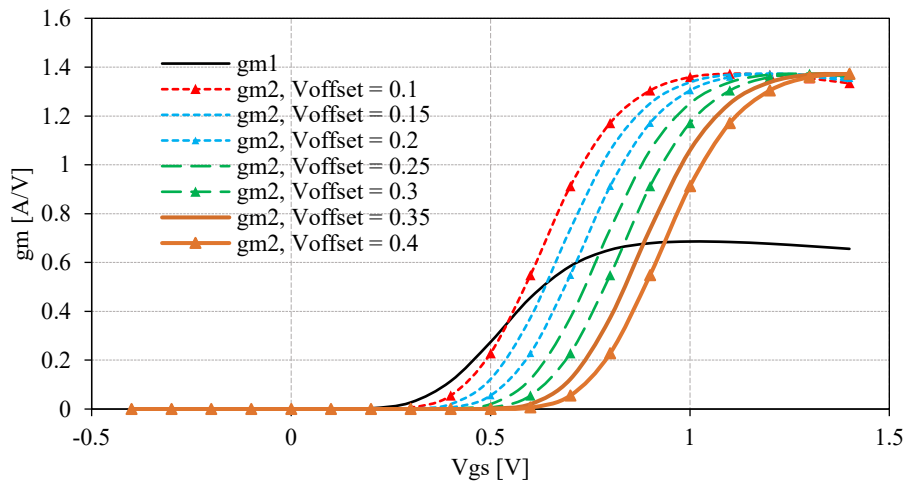


Figure 4-5. Transconductance g_m for two transistors in the segmented bias technique

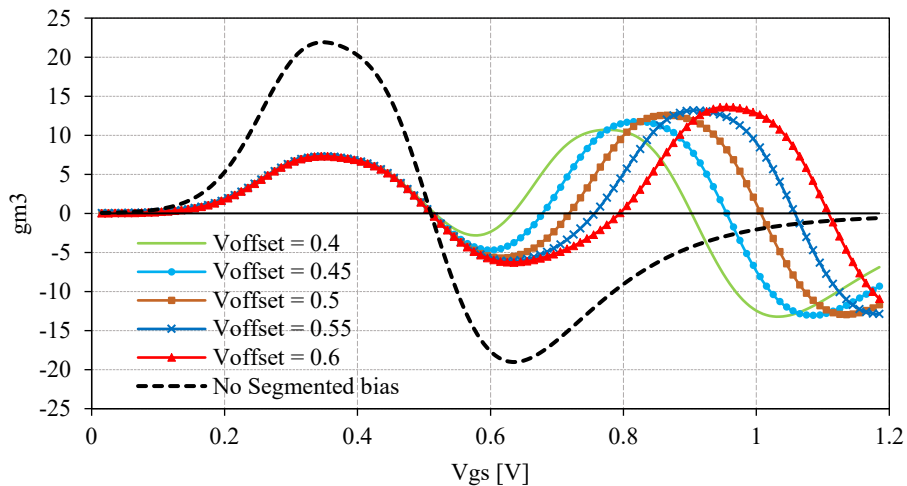


Figure 4-6. Simulated g_{m3} of the segmented bias (SB) case and the single transistor

Another advantage of the segmented bias technique is enhancing the linearity of PAs by extends the canceling region of g_{m3} . Figure 4-6 illustrates the simulated g_{m3} of two case studies: one without the segmented bias technique and another using an offset voltage between

two bias-segmented transistors. From this figure, it is clear to note that the higher the offset voltage is, the larger the sweet pot region of g_{m3} is extended. This feature proposes an excellent solution to limit the IMD3 [51] and thus increase the linearity of PAs. The use of this technique in the design of unit power cells will be fully described in the following subsection.

4.1.3 Power cell switching (PCS) technique

As mentioned at the beginning of this chapter, advanced modulation schemes such as OFDM exhibit high levels of PAPR. These levels require the PA to operate in back-off power region to achieve its proper efficiency. Chapter 2 and Chapter 3 have mentioned the advantage of the PCS technique for efficiency enhancement in the back-off power zone. The question is how many power cells needed to build the global power amplifier. The attending answer is the PAPR level of LTE signals that decides the number of power cells. This level also refers to the back-off output power about the impact on the efficiency of PA. The frequent required back-off output power is 6-8dB. This work hence takes this back-off range into account.

Table 4-1. Comparison of the number of power cells

Number of power cells	1	2	3	4
Back-off power mode	-	++	+++	++++
Total size	+	++	+++	++++
Parasites on interconnections	++++	+++	++	++
Power density on transistors	++++	+++	+++	++
Symmetric differential output signals in case of deactivation	-	++	++	+++

Table 4-1 demonstrates a brief overview about four cases of the design of power cells.

Four case studies present the different number of power cells. Among these cases, the case “4” with four power cells exhibits a proper configuration to implement the power cell switching technique regarding the back-off power mode configurability. Four power cells allow the global PA to operate until 12-dB back-off output power as mentioned in chapter 3. This level satisfies the requirement of the LTE signal. In addition, there will be less power density stressed on transistors; it helps increase the robustness of transistor designs. More transistors are required to build a unit cell; more parasites are created on interconnections. These parasites somehow degrade the performance of power transistors. For that reason, the case of one power cell is not thought-provoking for the cell design. This case does not either comply with the high configurability requirement. It is not probable to configure the power amplifier operating in more than one power mode with only one power cell as well as to obtain the balance of differential output signals. Three other cases bring the similar advantages and drawbacks.

However, the case 4 is chosen to enhance the number of power modes further, ensure the robustness of power cells and be compatible to the transformer design, which is mentioned in the previous chapter with four unit windings. Figure 4-7 illustrates the configuration of four power cells and the four-unit-winding distributed active transformer.

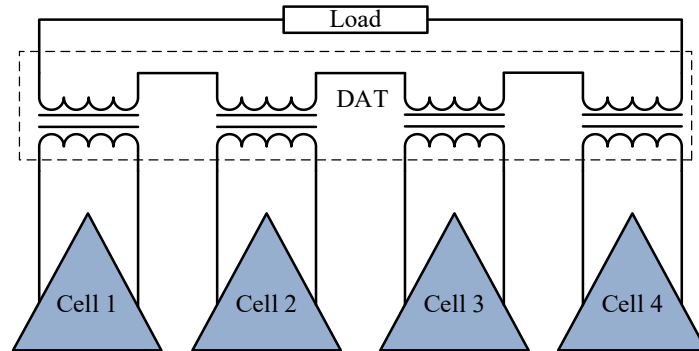


Figure 4-7. Four-power cell configuration for the power cell switching technique

4.1.4 Architecture of the PA

The number of power cells has been identified in the previous subsection. The next step is determining the global architecture of the power amplifier. Figure 4-8 illustrates the full architecture of this power amplifier. Due to four power cells, the inter-stage transformer (TR2) required adopting the four-unit-winding structure. This transformer plays the role of impedance matching with the input impedances of the power cells. A driver is added upstream to boost the gain level of the global power amplifier. The inter-stage transformer is considered as a power splitter to distribute power homogeneously from the driver cell to four power cells. Another transformer is designed between RF pads and the driver to avoid the input impedance mismatch of the power amplifier. This transformer (TR1) matches the input impedance of the driver cell to the 100-Ohm differential of RF pads. By taking advantage of two thick-layer-based transformers (TR2 and TR3), the supply connections of the driver and the power cells are integrated on these transformers as the feeding line introduced in Chapter 3. The source V_{driver} is connected to the driver through TR2. For the power cells, there are two supply sources: V_{dd1} and V_{dd2} . The first one V_{dd1} feeds two power cells: cell 1 and cell 4. The second one V_{dd2} feeds two others: cell 2 and cell 3. The segmented bias technique is performed by two bias sources, V_{bias1} and V_{bias2} . These sources join four biases of four power cells together. The bias configuration hence control the operating mode of the power amplifier.

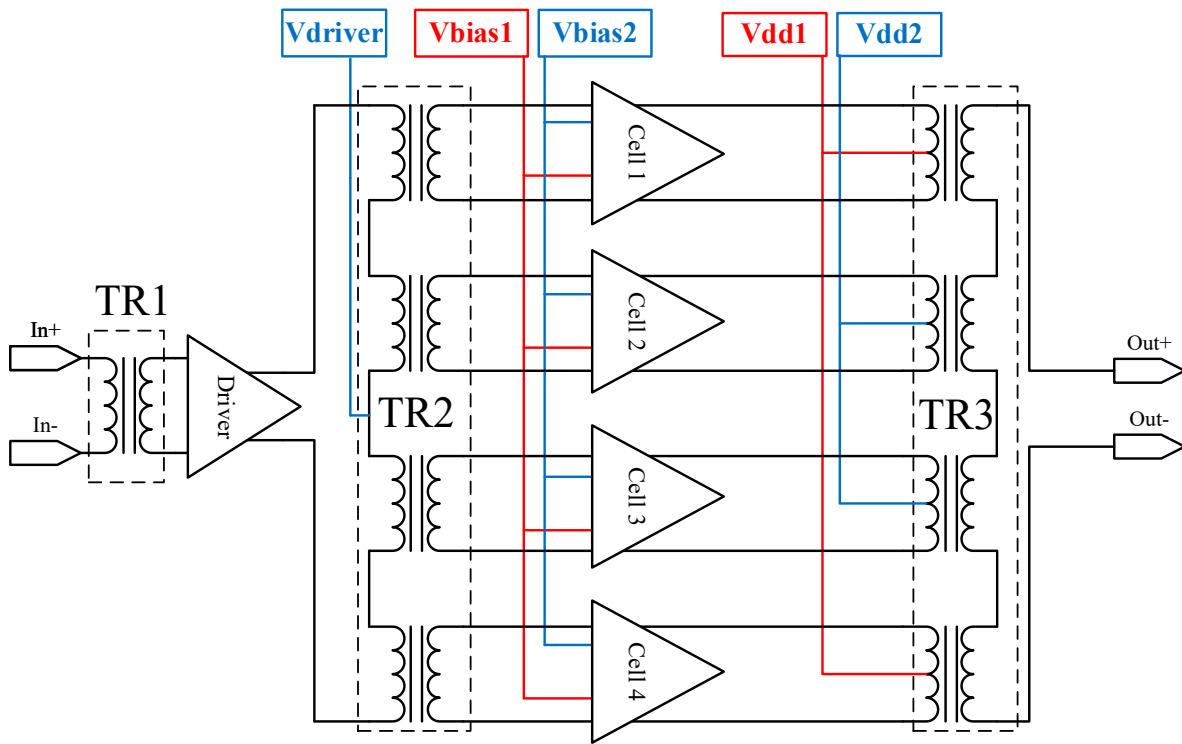


Figure 4-8. The global architecture of 4G LTE reconfigurable power amplifier

This subsection has described the global architecture of 4G LTE reconfigurable power amplifier. The next stage is to determine the detailed design of each part, the power cells, the driver and three transformers.

4.1.5 Structure of the power cells

After identifying the global architecture of the power amplifier, the next step is choosing the topology of the power cells. Figure 4-9 depicts four case studies used in comparison for the design of the power cells. The first case study in Figure 4-9.a is the single-ended common source. This topology has the source of the transistor connected to the ground; it is considered as the reference for the gate and the drain of the transistor. There always exists a capacitor C_{GD} , which causes the Miller effect and creates a return loop. This capacitor has a significant impact on the bandwidth of PAs. The main advantage of this topology is the output voltage swing approximately $2V_{DD}$ that can provide adequate linearity and output power. The second one in Figure 4-9.b is the differential common source. This topology has the same configuration as the single-ended common source but considers the differential signal type. This structure introduces higher output impedance and thus facilitates the matching network design. Figure 4-9.c shows the third case study of two transistors in cascode. This arrangement shows a suitable input/output isolation to ensure the stability of the cell. The last topology, in Figure 4-9.d, is the differential cascode, which combines at least four transistors to construct the power cell.

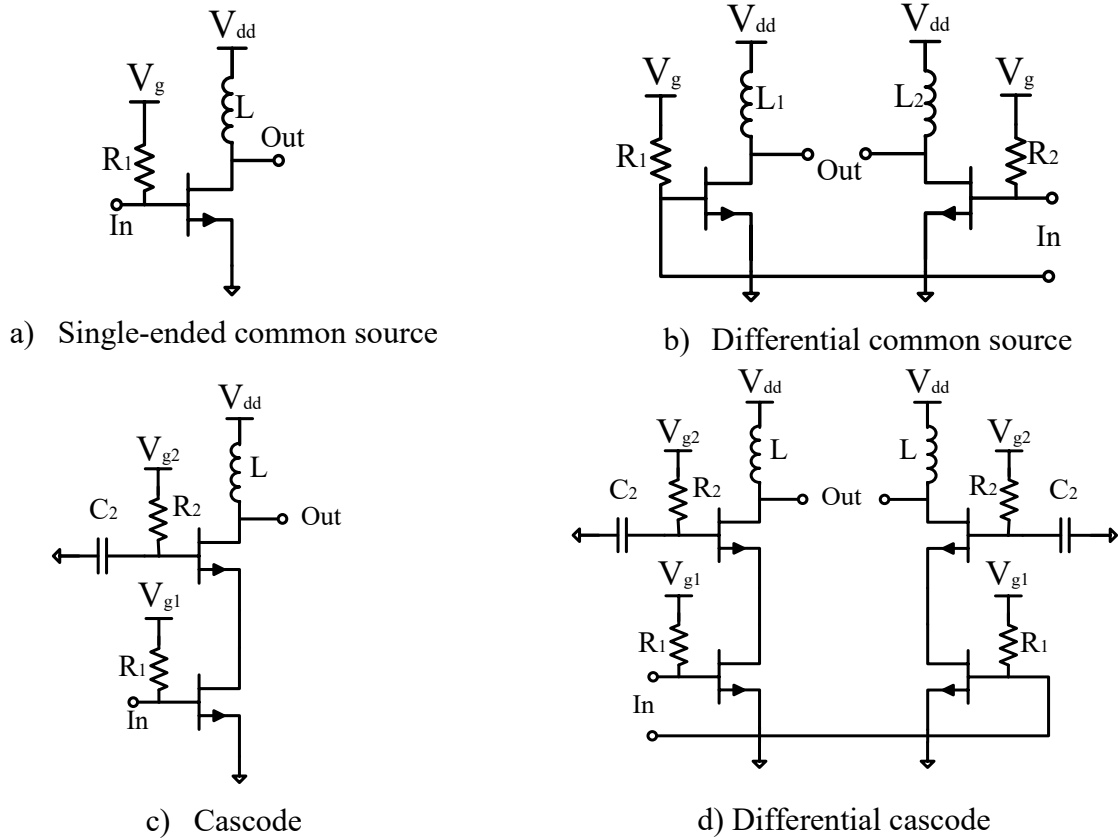


Figure 4-9. Four topologies used in comparison for the power cell design

Table 4-2. Comparison of four topologies for the power cell design

Topology	Single-ended common source	Differential common source	Cascode	Differential Cascode
Output power	+	++	++	++++
Gain	+	++	++	++++
Output impedance	+	++	++	++++
Power density on a single transistor	++++	+++	+++	++
Reverse isolation	+	+	++	++
Cell size	+++	+++	++	+

Table 4-2 illustrates the performance comparison of four structures. According to the comparison, the differential cascode provides the most appropriate configuration for the power cells. This topology presents a high output power to address the one-watt requirement. The output impedance introduced by this structure is higher than other ones; it simplifies the impedance matching network design. Also, more used transistors reduce the power density on each one and help ensure the reliability of the amplifier despite more parasitic components. Inheriting the advantage of the differential form, the differential cascode topology proposes the proper reverse isolation. On the other hand, the cell size designed by this topology is much

larger than that introduced by other ones. It is thus essential to choose an adequate size of power transistors in this topology.

4.1.6 Design of differential cascode sub-PA

4.1.6.1 Specifications of sub-power amplifiers

The main specifications of the global power amplifier are mentioned in Chapter 2. The power cells are hence requested to operate under these requirements. The design objective is to allow a supply voltage of 3.3 V on power cells. Therefore, the selected cascode topology is three-stage stacked transistors to ensure that the supply voltage is distributed equitably on three transistors (approximately 1.1V on each transistor). The estimated insertion loss presented by the output transformer is about 2 dB. As the required linear output power of the global power amplifier is 26 dBm, the linear output power of power cells is thus 22 dBm including transformer loss. Two principal techniques used in the design of power cells are the segmented bias and the cascode stacked transistors, which are mentioned in the previous subsection. Moreover, the power cells are required being unconditionally stable to ensure the overall stability of the power amplifier. The fundamental requirements of sub-power amplifiers are fully detailed in Table 4-3.

Table 4-3. Specifications of power cells

Parameter	Value
Supply voltage	3.3 V
Output power	>22 dBm
Gain	>15 dB
ICP1	-5 dBm
Stability	Unconditional ($\mu > 1$)
Used techniques	Segmented bias, stacked transistors in cascode

4.1.6.2 The design flow of power cells

Through the topology comparison, the differential cascode structure is chosen to design the power cells. The detailed steps of design flow are described in Figure 4-10. This subsection will present a systematic process from the sizing of power transistors to the design of input/output matching network by using load-pull and source-pull methods.

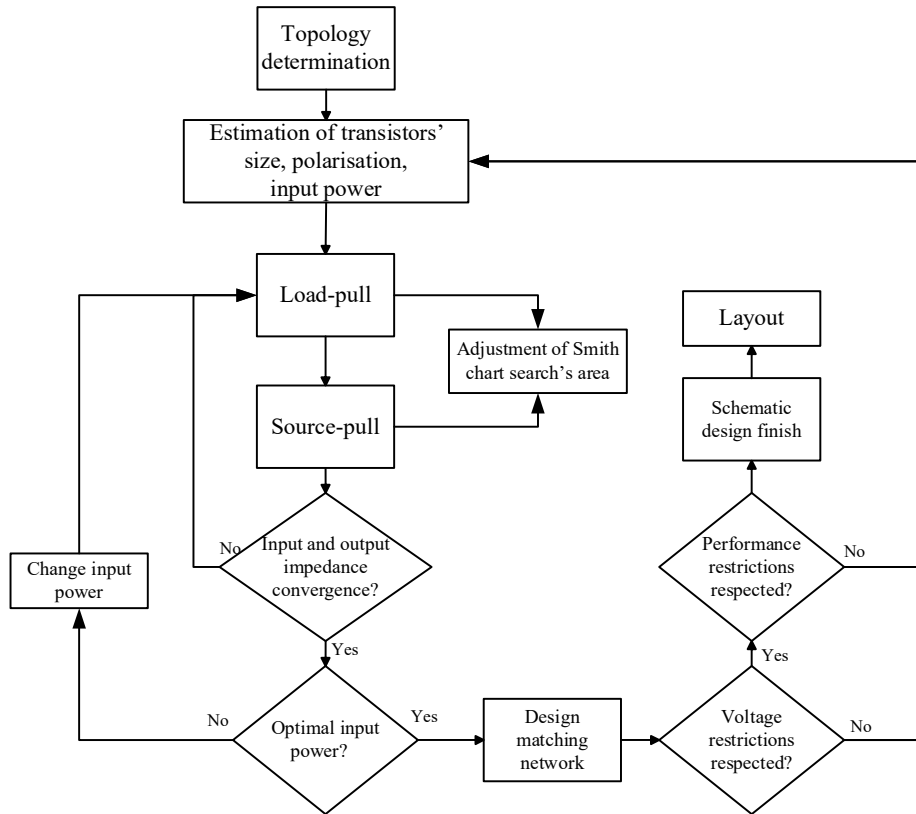


Figure 4-10. Flowchart to design and verify sub-power amplifiers

It is always practical to determine the size of a transistor by using the drain current that is calculated from the output power requirement. A great deal of attention must be paid when choosing the width and length to ensure the reliability and avoid the oversize of transistors. Figure 4-11 shows the design flow of transistor sizing. It is important to note that the DC current is calculated in the saturation region when the transistor reaches its peak power. The length and width of a power transistor is calculated inherently by the DC current. The size of power transistor must be sufficient to avoid instability issues. The design of transistors' interconnections will be described later.

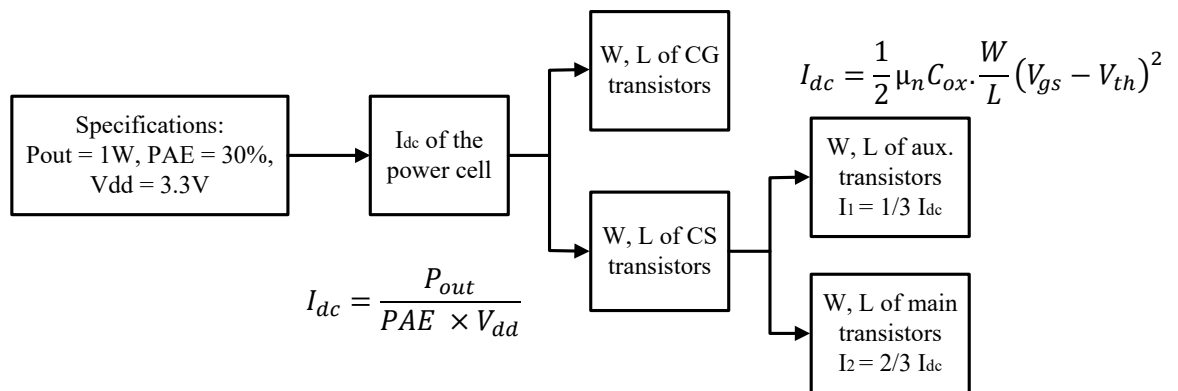


Figure 4-11. The design flow of sizing transistors in the power cell

4.1.6.3 Choice of power components

There are two types of transistors used in power cells: `nmos_rf` and `nmos_rf_6t`. The first one is the 1.2-V standard model. The second one is the transistor model with a layer of deep N well (DNW). The DNW layer isolates the bulk of NMOS transistor from the P-substrate. This transistor model helps resolve LVS errors. The depth of DNW is also larger than that of N well; it is hence more difficult for the noise to bypass the DNW layer and inject into P-substrate. The transistor model can isolate the noisy digital circuit from the sensitive analog circuit for future purposes. Figure 4-12 illustrates the layout of two transistor models with three fingers for each transistor. Figure 4-13 depicts the cross-sectional view of deep N-well transistor model.



Figure 4-12. Layout of two transistor models `nmos_rf` and `nmos_rf_6t` with deep N well layer

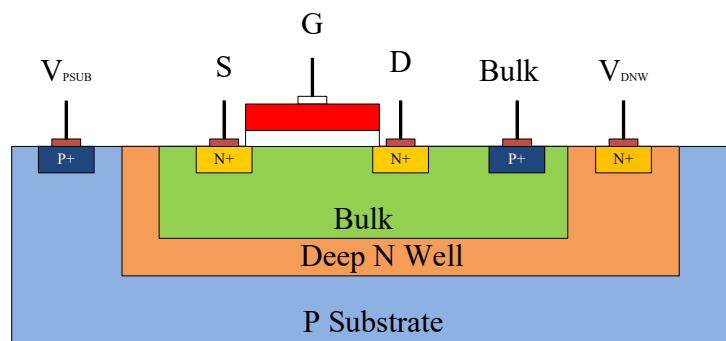


Figure 4-13. Illustration of Deep N Well transistor

The next step is to choose an adequate size of power transistors. Delivering a high output power with a low supply voltage requires a higher output current. It demands a greater total width (W) of the transistor. Circuit designers can increase either the finger width (W_F) or the number of fingers (N_F) or both of them. Figure 4-14 illustrates the conceptual layout of a transistor using multiple fingers. A multi-finger CMOS transistor with a large finger width results in high gate resistance (R_G)[52]. The gate of each finger behaves as a distributed RC network, whose total resistance can be approximated by:

$$R_G = \frac{R_{poly}W_F}{3n^2L} \quad (4.1)$$

Where R_{poly} is the sheet resistance of the polysilicon gate, W_F is the finger width, L is the channel length and $n=1, 2$ depending on the number of gate contacts used in the layout of

the transistor. The gate resistance causes more losses in the transistor, hence reduces f_{max} and the maximum stable gain (MSG) of the transistor [52].

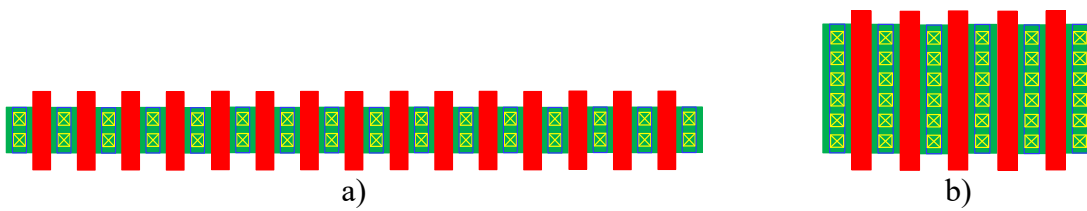


Figure 4-14. Conceptual layout of a transistor using a) multiple fingers (N_F) and small finger width (W_F) b) smaller N_F and larger finger width

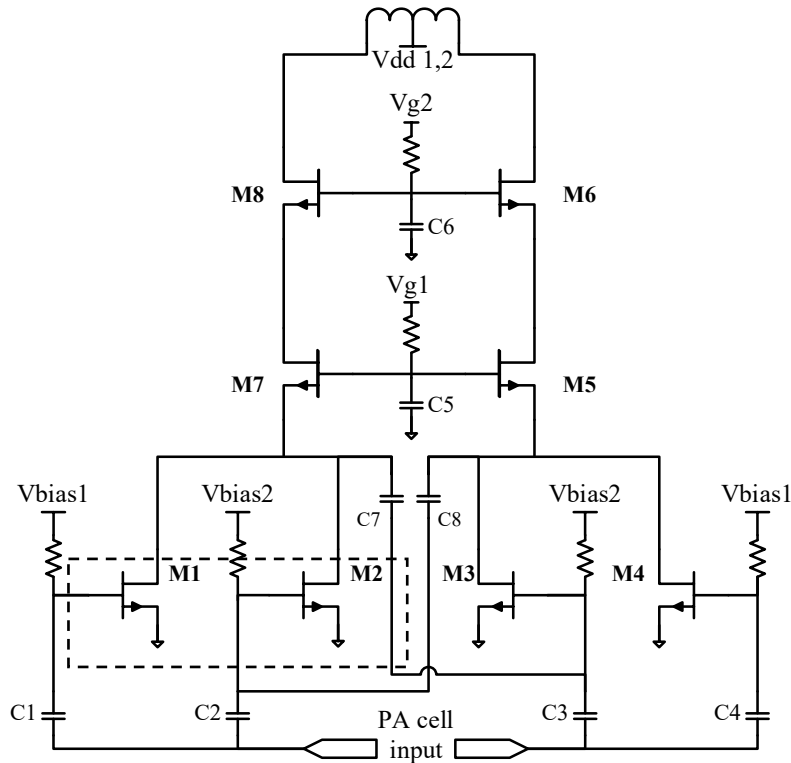


Figure 4-15. A detailed schematic of power cells

After choosing and sizing the power transistors, the next step is to build a full schematic of the power cells. Following the methodology mentioned above, a three-stage cascode differential bias-segmented power cell has been designed in the TSMC 65-nm CMOS process. The implemented power cell schematic is shown in Figure 4-15. It consists of four transistors (M_1, M_2, M_3, M_4) to build the segmented bias technique, two capacitors (C_7, C_8) to build the neutralization stability technique, and two capacitors (C_5, C_6) to keep the drain-source voltage swing balanced. It is important to note that the use of transformers eliminates the need for AC coupling and RF chokes while differential operation reduces the amount of bypass capacitance needed. Four bypass capacitors (C_1, C_2, C_3, C_4) are used to isolate input signals into bias-segmented transistors. Table 4-4 illustrates the size of transistors in the power cells. The output of power transistors is combined by using a transformer in the differential configuration.

Table 4-4. Size of transistors

Transistors	Width per finger (μm)	Length per finger (nm)	Number of fingers	Number of parallel devices
M1	3	60	32	8
M2	6	60	32	6
M3	6	60	32	6
M4	3	60	32	8
M5	6	60	32	10
M6	6	60	32	10
M7	6	60	32	10
M8	6	60	32	10

As in Figure 4-16, the segmented bias technique is implemented with two different-size transistors. The noteworthy point of the transistor's layout is the symmetric placement of unit transistors. The dimension of bias-segmented transistors is $67\text{-}\mu\text{m}\times 89\text{-}\mu\text{m}$. The neutralization technique aims to minimize the capacitance C_{GD} of transistors. The value of two capacitors is chosen to optimize both the gain and the stability. Their selected value is 506-fF with MOM cap model (crtmom_rf).

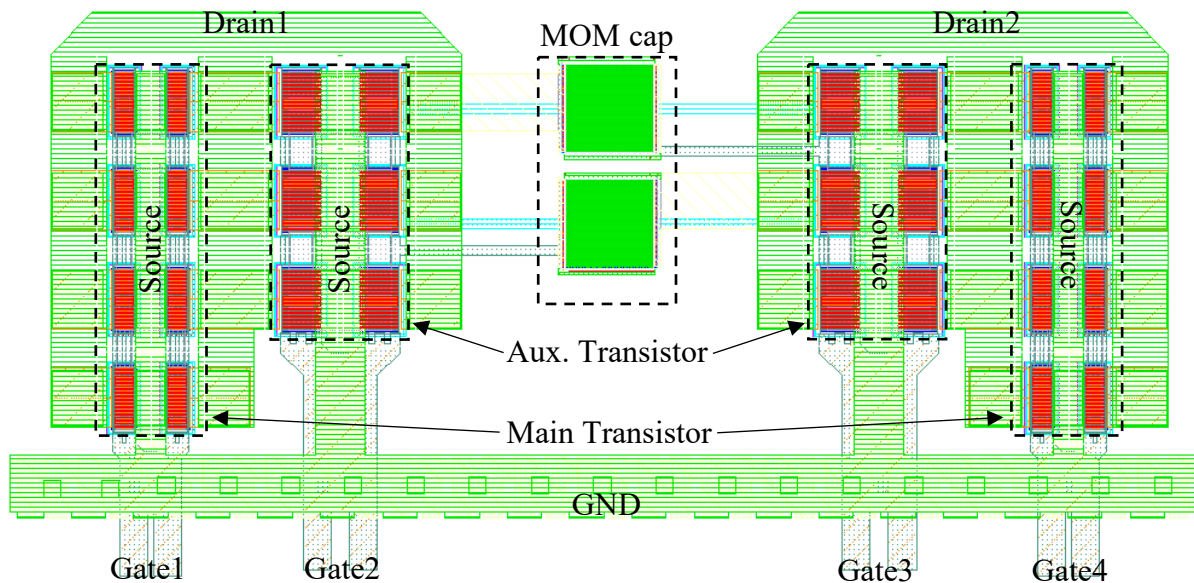


Figure 4-16. The layout of bias-segmented transistors in the differential topology

Figure 4-17 illustrates the influence of neutralized capacitors on the stability of the power cell. The simulation is performed for a single power cell ended by its optimal input and output impedances. Two neutralized capacitors in differential topology ensure the stability factor (μ) of the power cell higher than one in the required frequency band.

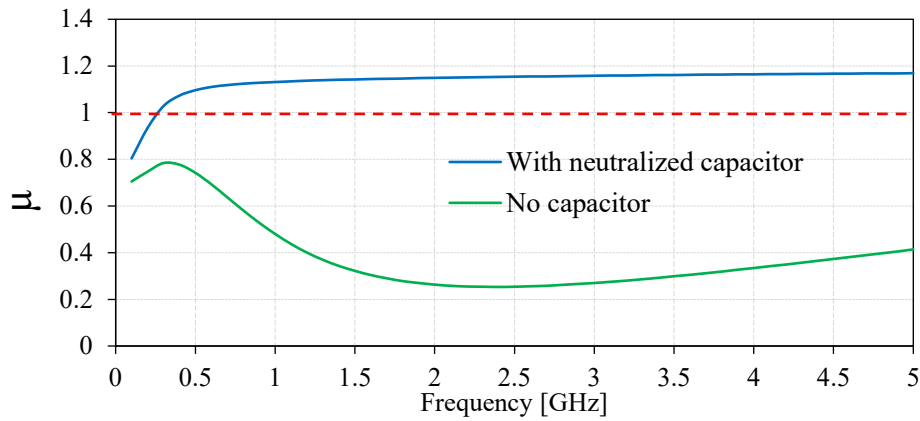


Figure 4-17. Influence of neutralized capacitors on the stability of the power cell

4.1.6.4 Reliability of power transistors

One of the challenges of CMOS technology is the low breakdown voltage of transistors. The frequent level of the breakdown voltage of MOS transistors is about 5-V as mentioned in DRM of the technology. It is hence essential to pay attention to the reliability of each transistor in cascode by verifying its drain-source and gate-source voltages. The simulation is performed for all range of input power until the saturated power of the power cell. Figure 4-18 presents the waveforms of four transistors in cascode of the power cell assuring the liability of transistors under high power stress. In this figure, the voltage swing of each node of transistors in Figure 4-15 is demonstrated, in which the drain-source voltage (V_{ds}) is plotted in function of its gate-source voltage (V_{gs}). The simulation is performed by Keysight GoldenGate. The drain-source voltage (V_{ds8}) of the transistor M_8 is much higher than the other ones because of its role to output the high RF output signal. Therefore, more attention on its reliability needs to be paid. The simulation shows the robustness of this transistor under high power condition.

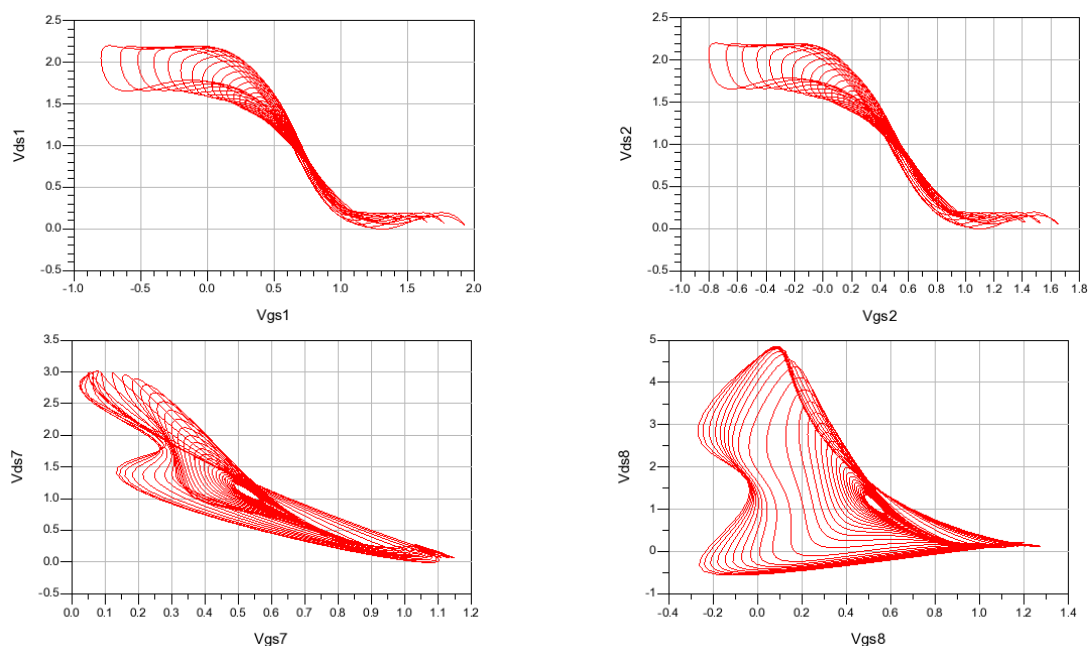


Figure 4-18. V_{ds} versus V_{gs} of four transistors in cascode in all input power range

4.1.6.5 Impact of interconnections

The next step is to verify the reliability of transistor interconnections. Due to high DC current flowing in power transistors, interconnections require being robust under any circumstances of DC and AC operations. This subsection focuses mainly on the reliability of interconnections, in which DC currents are in high demand.

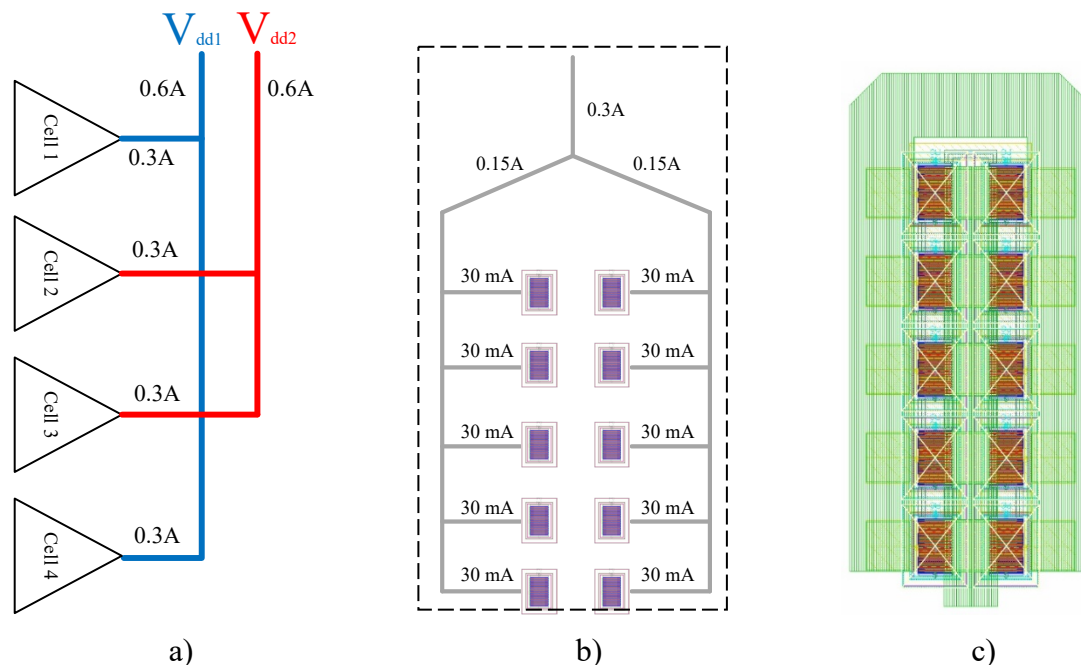


Figure 4-19. DC current distribution inside the PA (a) DC current on connections with DC supply (b) DC current on interconnections inside a power cell (c) Corresponding layout of the power cell with DC current distribution

Figure 4-19 illustrates the DC current distribution inside the PA. As mentioned above, there are four supply sources in this PA: V_{dd1} for cell 1 and cell 4, V_{dd2} for cell 2 and cell 3. The DC current on connections with DC supply is shown in Figure 4-19.(a) where the maximum DC current that the PA consumes is planned until 1.2 A. Therefore, the DC pitch connected to each unit power must support a maximum DC current of 300 mA. The DC pitch is hence designed with the top metal (M9) with a width of 40- μm , where its design is modified to respect the design rule of the CMOS process, in which the largest width of a metal is 12- μm . Interconnections inside each power cell are depicted in Figure 4-19.(b). Taking the same analysis as the global PA, each interconnection connected the unit power transistor requires supporting a maximum DC current of 30 mA whereas the interconnections outputted to DC supplies can carry a maximum current of 150 mA. All these interconnections are designed on the top metal (M9). The corresponding layout of power cells is illustrated in Figure 4-19.(c). The width of interconnections is all calculated according to DC metal current density (EM) specifications of the CMOS technology in Appendix B.

4.1.7 Design of the driver cell

The driver cell aims to boost the gain of the global amplifier. Its required power gain is 15-dB. As shown Figure 4-8, the output of the driver is connected to the four-way power divider (TR2). For that reason, it is important to consider insertion losses (IL) of the power divider and the power splitter to calculate the specifications of the driver cell as shown in (4.2). The required 1-dB compression power is:

$$P_{1dB,driver} = P_{out} + IL_{TR3} - Gain_{PA\ cell\ required} - IL_{TR2} \quad (4.2)$$

The desired value of $P_{1dB,driver}$ is 15 dBm. The driver cell also adopts the differential cascode topology with two-stage stacked transistors. The input of the driver is matched to the input 100-Ohm differential pads by the input transformer (TR1). To achieve the unconditional stability, two capacitors (C_2, C_3) are inserted into the cell. Their values are 89.3-fF with MOM capacitor model. The full schematic of the driver is illustrated in Figure 4-20. The simplified layout of the driver cell is depicted in Figure 4-21.

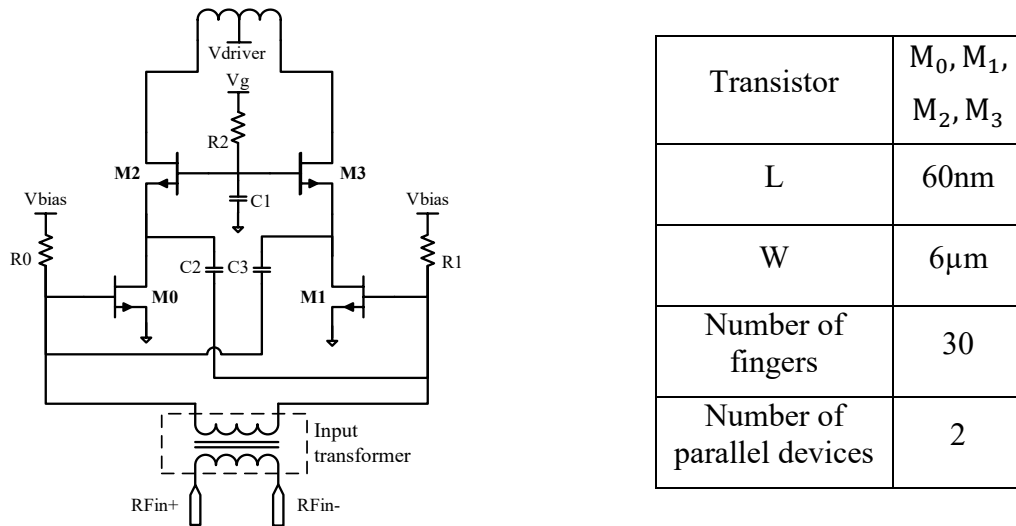


Figure 4-20. Schematic of the driver cell

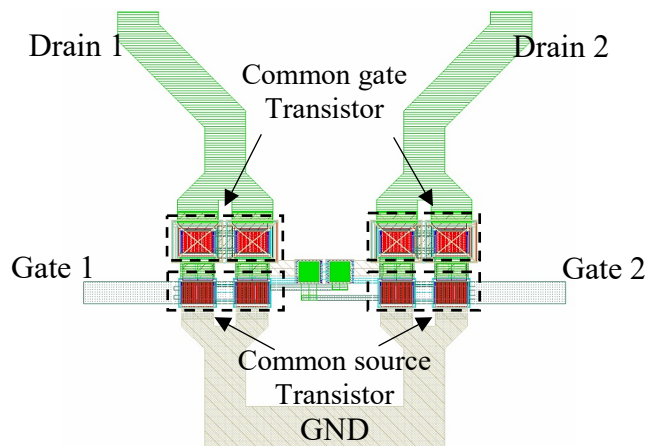


Figure 4-21. The layout of two transistors in cascode

4.2 Design of transformers – Impedance matching network

The transformer design is already presented in Chapter 3. This chapter will review some fundamental points and its applications for the design of this PA. The adopted kind of transformer is the four-way four-stacked-metal transformer with power combining in series. The fundamental of the power cell switching technique focuses on the on/off operation of power cells. This subsection will give an in-depth analysis of impedance modulation of this technique applied in the PA. The PA includes three transformers. Each transformer has its role in the PA design. The first one (TR1) is used for input impedance matching. The second one (TR2) plays the role of inter-stage matching and also power splitter. The last one (TR3) combines power from four unit cells and performs the output matching network.

The transformer TR1, as shown in Figure 4-22, uses two stacked metals (M8 and M9) to build the primary and the secondary windings. The size of this transformer is $216\mu\text{m} \times 675\mu\text{m}$. The transformer TR2, as shown in Figure 4-23, is a four-way transformer built with the top metal (M9) for the primary winding, and the metal (M8) alongside two intermediate metals (M6 and M7) for interconnections to construct the secondary windings. Its size is $1700\mu\text{m} \times 173\mu\text{m}$. The transformer TR3, as shown Figure 4-24, uses the top metal for the primary winding and four stacked metals (M5, M6, M7 and M8) for the secondary winding. The reason of four stacked metals is that the transformer sustains high DC current as the analysis mentioned before. Its size is $1886\mu \times 169\mu\text{m}$. Since the transformer performs the impedance modulation of the PCS technique, this subsection will focus on the analysis of its impedance modulation corresponding to off-state power cells.

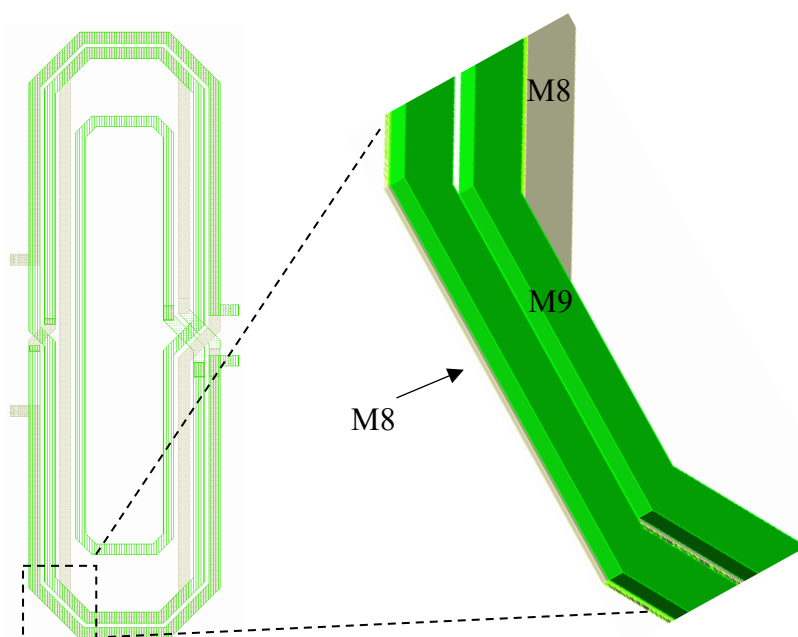


Figure 4-22. Layout of the input transformer (TR1) with two stacked metals

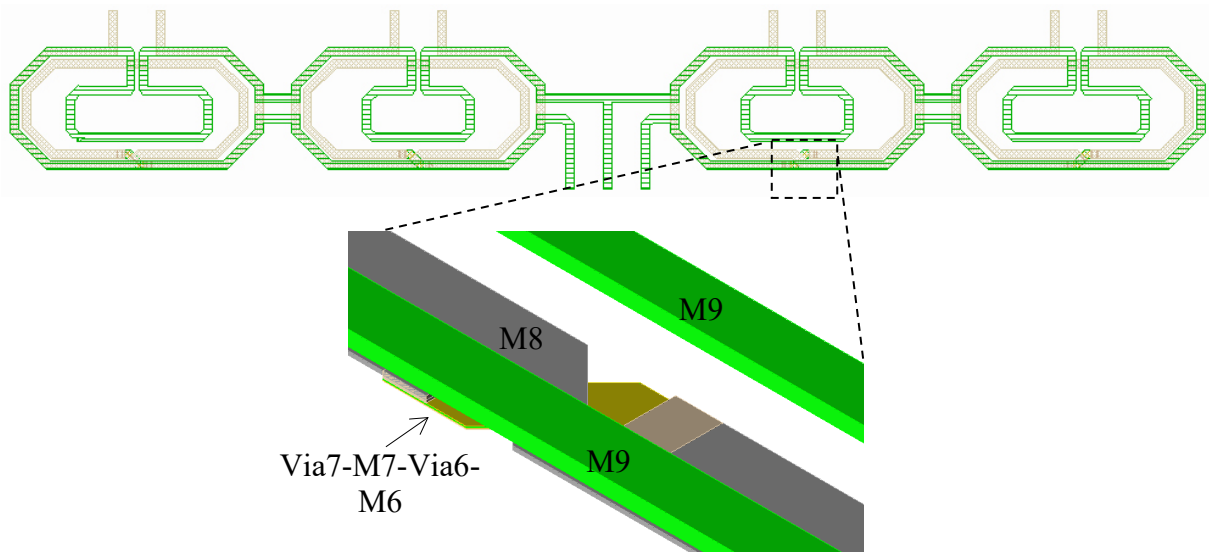


Figure 4-23. Layout of the inter-stage transformer (TR2) with four unit windings

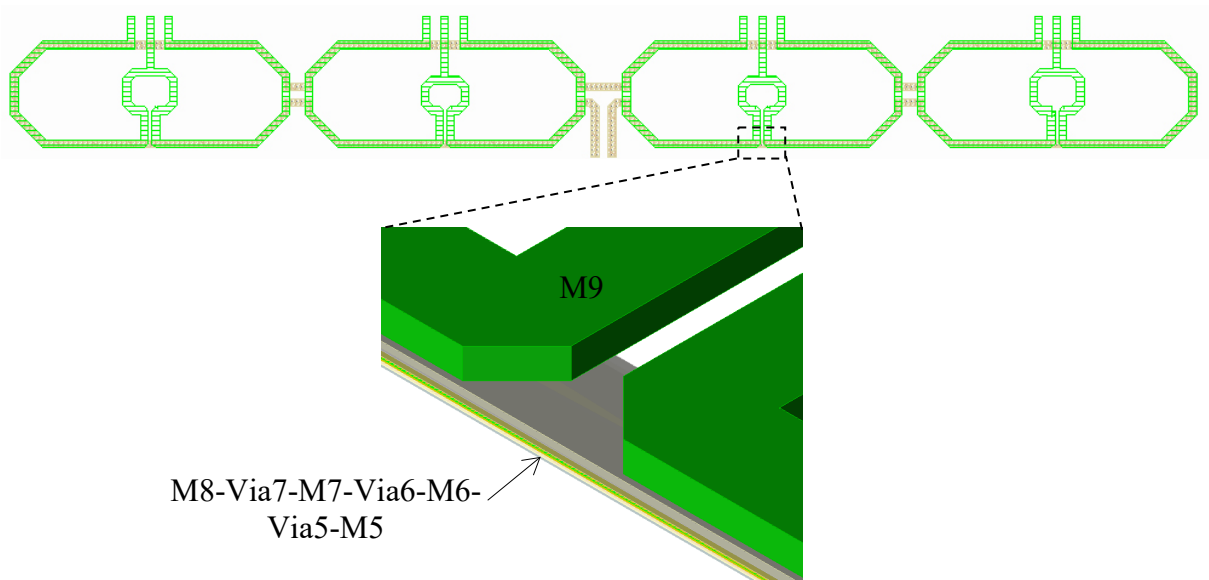
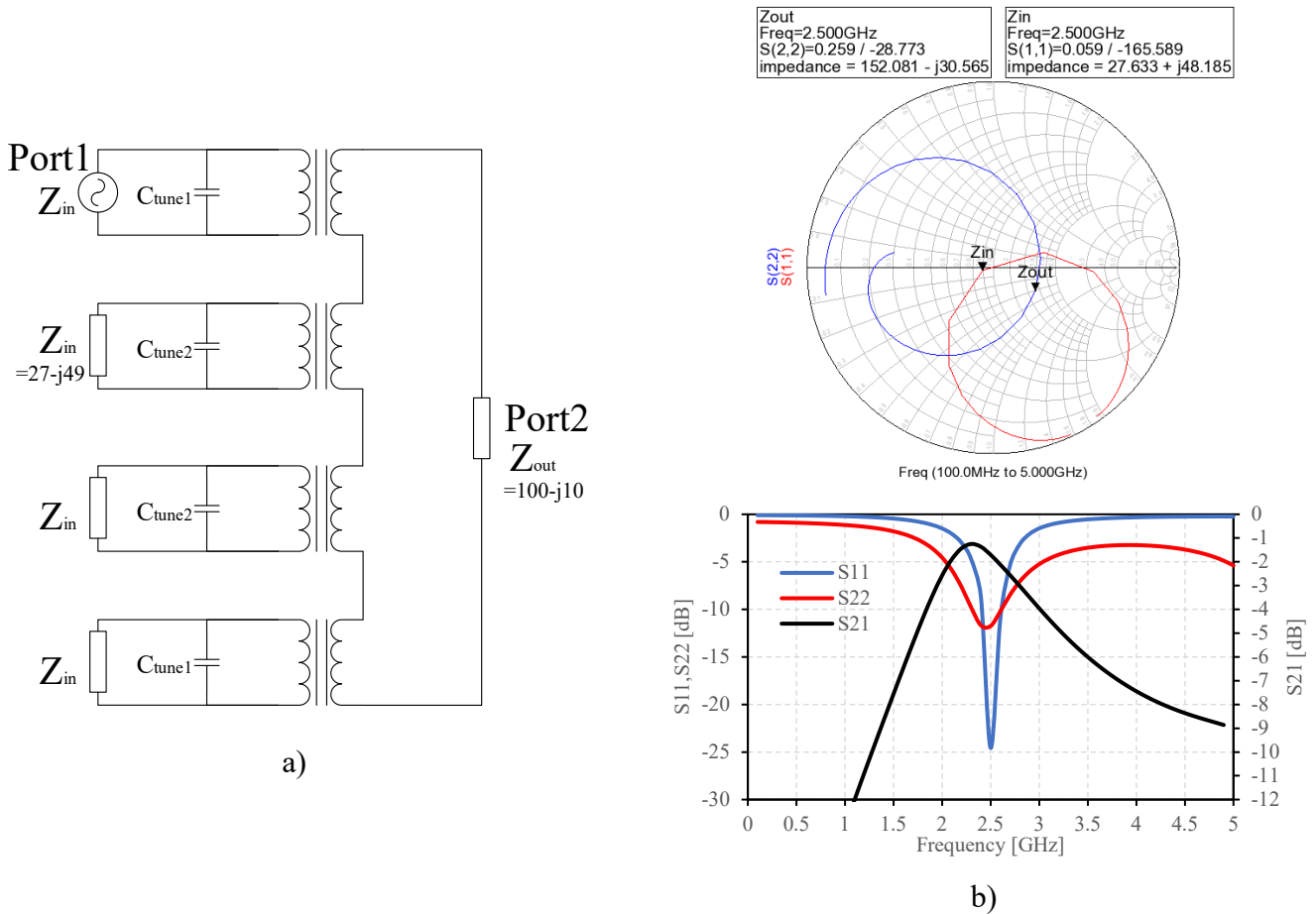
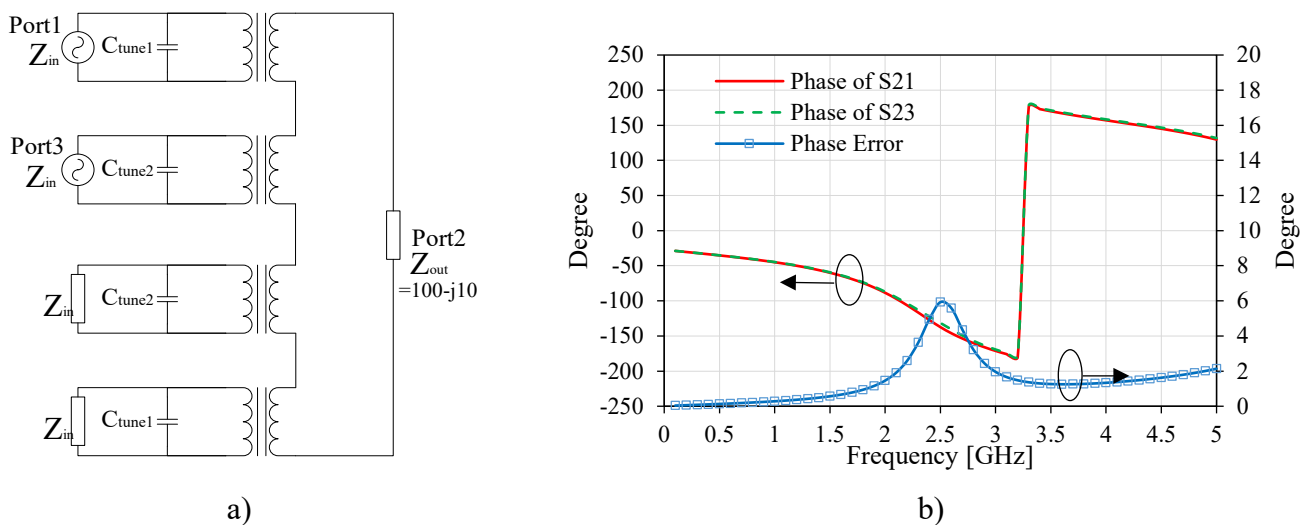


Figure 4-24. Layout of the output transformer (TR3) with four unit windings

The output transformer (TR3) needs to be verified in impedance matching and phase error. Test benches below will extract these required results. The first used test bench is shown in Figure 4-25. In this test bench, the first port (Port 1) is connected to one input winding and the second port (Port 2) is for the output winding. The other input windings are terminated by an impedance $Z_{in} = 31 - j49$ that is conjugated with the output optimal impedance of unit power cells. The imaginary part of Port 2 displays the effect of parasite inductances and capacitances at RF output pads. Two capacitors C_{tune1} and C_{tune2} are added in the primary windings to compensate impedance mismatch. With two tuning capacitors, the transformer allows a proper impedance matching and introduces an insertion loss of 1.5 dB. Figure 4-25.(b) illustrates the results of TR3 in S-parameters.



The second test bench applied to TR3 is shown in Figure 4-26 where another port is added to one input winding to verify the phase error between two primaries of the transformer. This test bench adopts the same impedance configuration as the first one. The transformer ensures a low phase error between two windings, which allows limiting AM-PM distortion in CW signals and EVM in modulated signals. The maximum phase error introduced by the transformer is 6° at the operating frequency of 2.5-GHz.



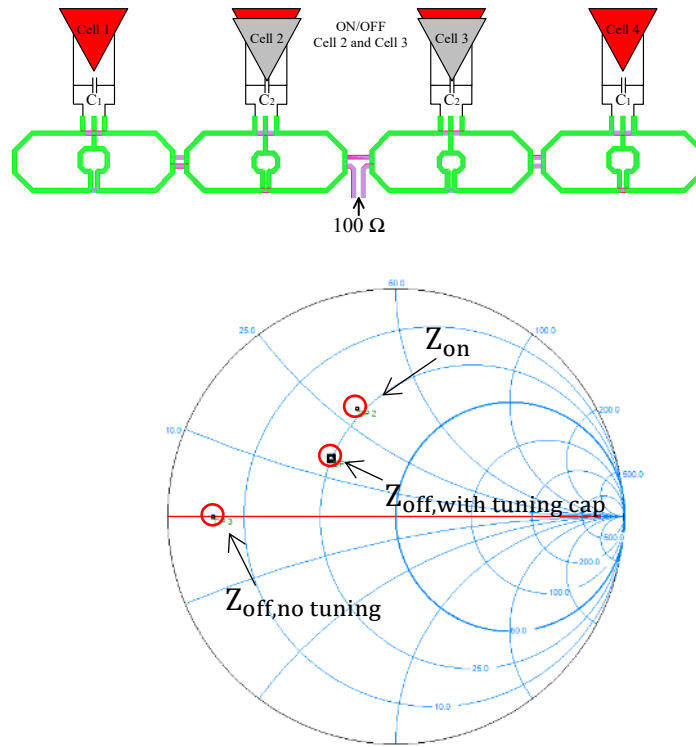


Figure 4-27. Impedance modulation of power cells in theory and in simulation with two tuning capacitors

As mentioned above, the power cell switching technique requires a flexible load modulation to enhance back-off efficiency. In this subsection, the impedance modulation between mode changes will be introduced. Figure 4-27 illustrates the impedance modulation in the PA. In addition to reduce impedance mismatch between the power cells and the transformer TR3, two capacitors (C_{tune1} and C_{tune2}) play also an important role in enlarging the operating bandwidth of the PA. These capacitors allow bringing the off-state impedance of two unit cells (2, 3) back to an intermediate value instead of zero. The noteworthy aspect of TR3 is the identical design of two outer windings and that of two inner windings. This design is compatible with the PA operation when two unit cells (2, 3) are turned off. Hence, the input impedance of TR3 is partially compensated to avoid mismatch. This aspect of TR3 and the load modulation created by two capacitors help offset the input impedance of TR3; hence, it ensures an adequate impedance matching and reduces losses created by impedance mismatch.

4.3 Stability of Power Amplifier

Stability is a prime concern in PA design. Both small-signal and large-signal stability need to be ensured over process and temperature. The first one is performed under linear analyses (S-Parameters) and the second one is executed in the time domain.

4.3.1 Small signal stability

In small-signal analyses, PAs are connected to two ports (at the input and output). There are two approaches to verify the stability of PAs: the Rollett factor (K) [53] and the μ stability factor [54]. The conditions of unconditional stability in two approaches are expressed by:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2} > 1 \quad (4.3)$$

With $\Delta = S_{11} \cdot S_{22} - S_{21} \cdot S_{12}$ and

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \quad (4.4)$$

Or

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \Delta| + |S_{21} S_{12}|} > 1 \quad (4.5)$$

Linear analysis is useful in the small-signal regime. The problem is that PAs are expected to operate in non-linear regime (large-signal). The linear analysis does not guarantee the stability of PAs in large-signal domain completely. The intrinsic capacitances of transistors namely C_{gs} , C_{gd} or C_{ds} also affect the transistor behavior. Hence, a non-linear analysis is needed to the PA stability.

4.3.2 Large signal stability

Non-linear stability process is a question of studying the possible start of oscillation at a f_{osc} frequency while the transistor is subjected to its DC bias and high power at a f_{RF} frequency. We use a weak-signal perturbation at the f_{osc} frequency, which is superimposed around a strong-signal at the f_{RF} frequency. Poles and zeros of the transfer function of this perturbation are then studied and extracted. One of the useful tools to elaborate this kind of method is STAN [55]. Due to non-availability of this tool in the laboratory, this method is not used in this design.

Large-signal stability analysis can also be performed by Harmonic Balance (HB) simulations using Agilent Golden Gate. This method addresses non-linear circuits such as PAs or oscillators. The HB process uses the Fourier transform to simulate circuits in the frequency domain. The objective of this process is to detect all instabilities and provide their corresponding potential oscillation frequencies. According to Nyquist criterion, a circuit is stable if its plots in the Nyquist plan encircles the origin more times in clockwise than in counter-clockwise. Despite the certitude of this method, it is not used in this circuit due to no information about the stability margins.

The adopted method is the excitation of temporal square wave pulse in every sensitive node of the PA such as gates or drains of transistors. This signal must be steep enough to cover

the operating frequency of the PA. The simulation is performed by transient analysis in the time domain. No input signal is imposed to the PA. Therefore, the response output signal will be absorbed later after the pulse injection. The simplified test bench of this method is illustrated in Figure 4-28. The results of this method are shown in Figure 4-29. The pulse is imposed respectively to the gate and the drain of each transistor. The output signal of the PA is extracted in the same figure. After 4ns, the output signal is wholly absorbed. This result proves the unconditional stability of the PA.

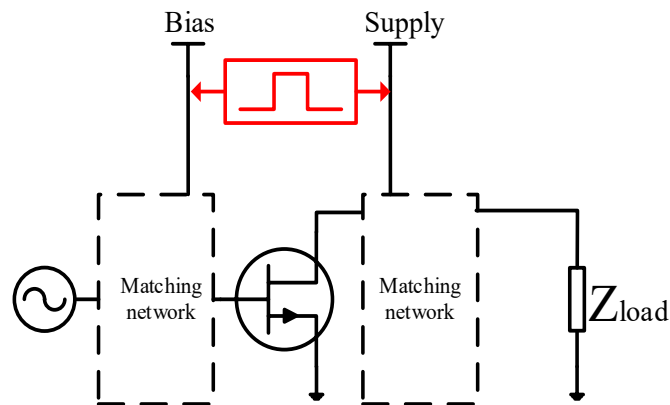


Figure 4-28. Test bench to verify the large-signal stability

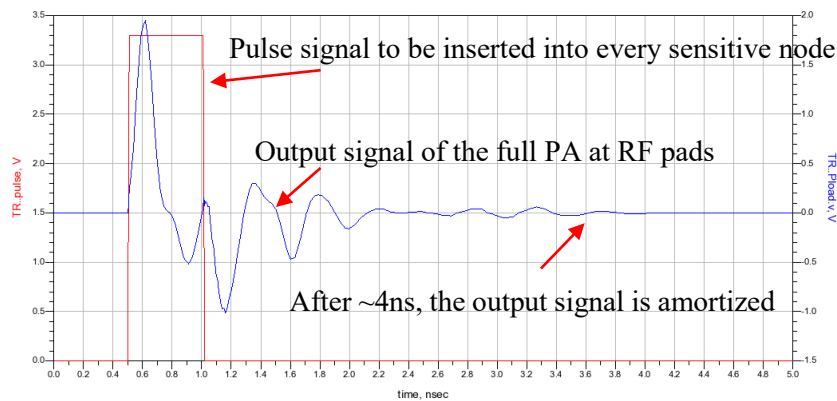


Figure 4-29. The output response of the PA when one pulse is imposed to a sensitive node

4.4 Operation of the reconfigurable power amplifier

To achieve the requirements of 4G LTE signals about low back-off efficiency, the PA is configured with four possible modes in Table 4-5. This configuration allows maintaining the efficiency above 10% in the 8 dB back-off power zone. Four modes are defined by two bias voltages (V_{bias1}, V_{bias2}) of the common-source transistors and two supply voltages: V_{dd1} for the sub-PA cells (1, 4) and V_{dd2} for the sub-PA cells (2, 3).

The power operating zones are defined according to the power cell switching technique. The detailed power mode configuration of the PA is illustrated in Figure 4-30.

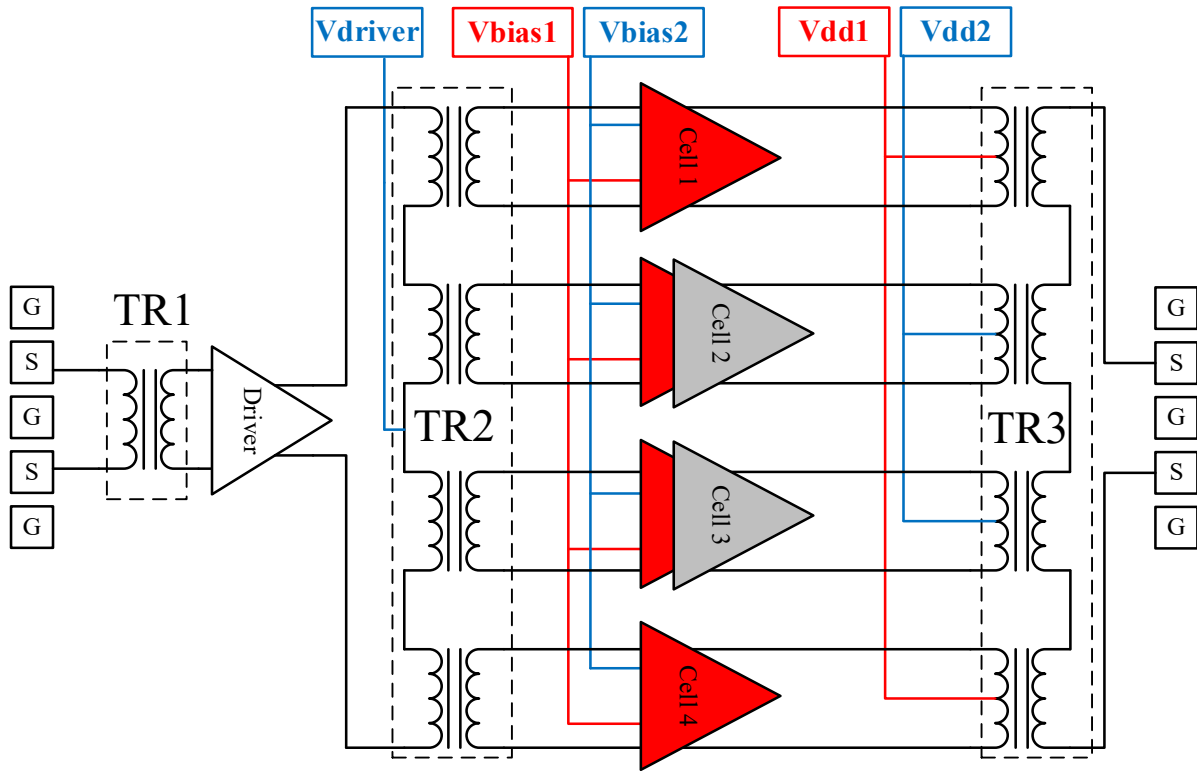


Figure 4-30. Power operating modes of the PA in FULL ON and HALF ON/OFF setup

Two modes 1, 2 are used in the high power (HP) region. In these modes, four power cells are all active. More current will be delivered to the load; the output power is consequently increased. These modes are determined by V_{bias1} and V_{bias2} to address the demand for efficiency, output power or linearity by changing the operating class of two common-source transistors. Two modes (3, 4) are used in medium power (MP) region. In these modes, two cells (2 and 3) are disabled by keeping their supply source (V_{dd2}) off, while two power cells (1 and 4) controlled by V_{dd1} are turned on. Mode 1 and Mode 3 aim to maximize output power of the PA in high-power zone and medium-power zone. Mode 2 and Mode 4 focus on enhancing back-off efficiency of the PA. This configuration is outlined in Table 4-5.

Table 4-5. Operating modes of the reconfigurable power amplifiers

Mode	V_{bias1}	V_{bias2}	V_{dd2}	V_{dd1}	Number of active cells
1	0.67	0.71	3.3	3.3	4
2	0.67	0.35	3.3	3.3	
3	0.67	0.71	0	3.3	2 (cell 1, cell 4)
4	0.67	0.35	0	3.3	

4.5 Measurement results and comparisons with simulations

4.5.1 Layout and chip photograph

The layout of the PA, as in Figure 4-31(a), is done in Cadence Virtuoso using the TSMC 65-nm CMOS process. The layout is done as symmetrical as possible to preserve the symmetry

needed for the PA core to work correctly. The size of the complete PA is 2mm x 2mm including the size of the seal ring used for the fabrication, in which the core size including RF pads is 1.68mm × 1.89mm. Metal 9 (the top metal layer) is used for DC pitches, RF interconnections and also transformers. A robust large ground consisting of five stacked metal layers covers all the surface of the PA. Four metals (2, 3, 4 and 5) are used for the interconnections between the gates of transistors and the RF pitches. The die photograph of the PA is shown in Figure 4-31(b).

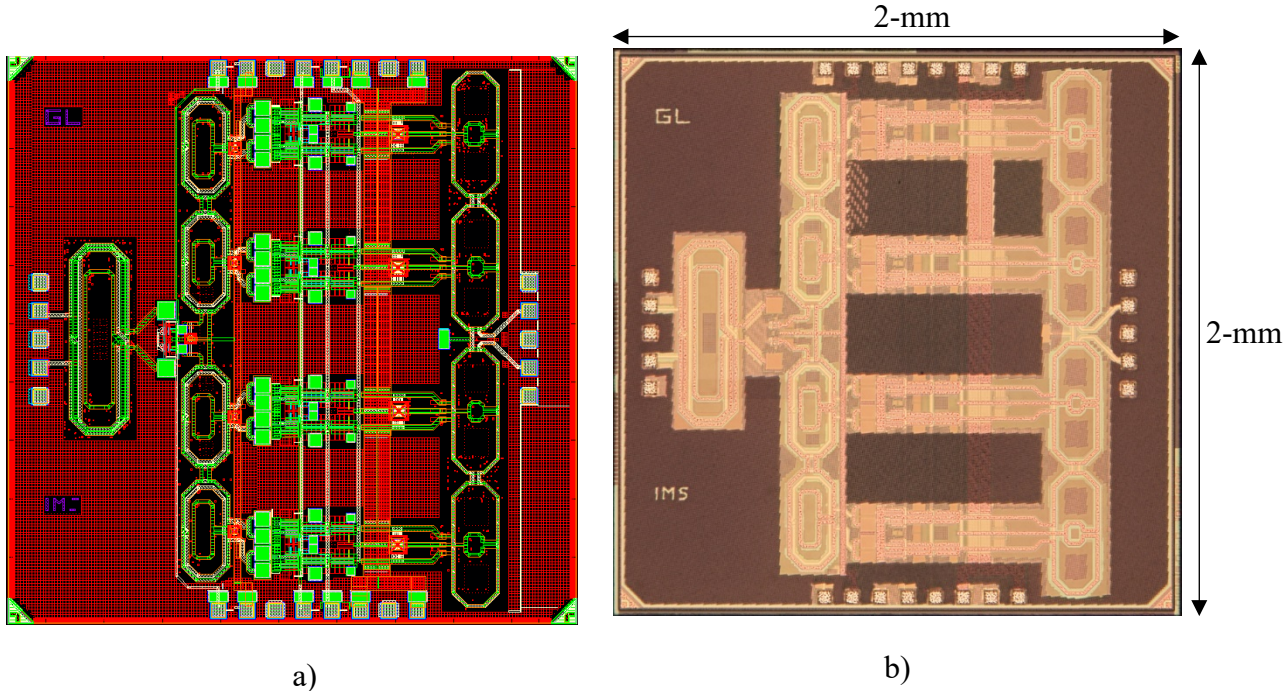


Figure 4-31. (a) Layout and (b) Die photograph of the power amplifier

4.5.2 Measurement setup

After finalizing the layout, sending the circuit to the foundry and receiving the test dies, the next step is setting up the measurement test benches. In this step, there are four necessary setups: small-signal measurements, large-signal measurements with single-tone, two-tone, and modulated signals.

4.5.2.1 Setup of small signal measurements

The first test bench is the setup of small signal measurements. This test bench aims to verify the performance of the PA in S-Parameters, which consist of impedance matching, small-signal gain, and small-signal stability. The full test bench is described in Figure 4-32. The setup uses a PNA network analyzer Agilent along with its supplement S-Parameter Test Set Agilent to establish the differential-signal measurement.

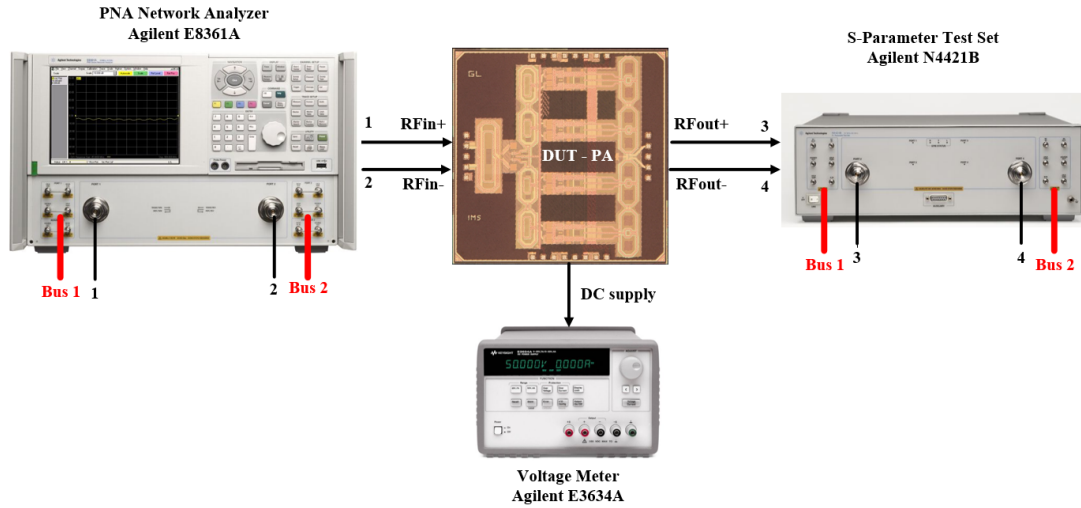


Figure 4-32. Setup of S-Parameters measurements

4.5.2.2 Setup of single-tone signal measurements

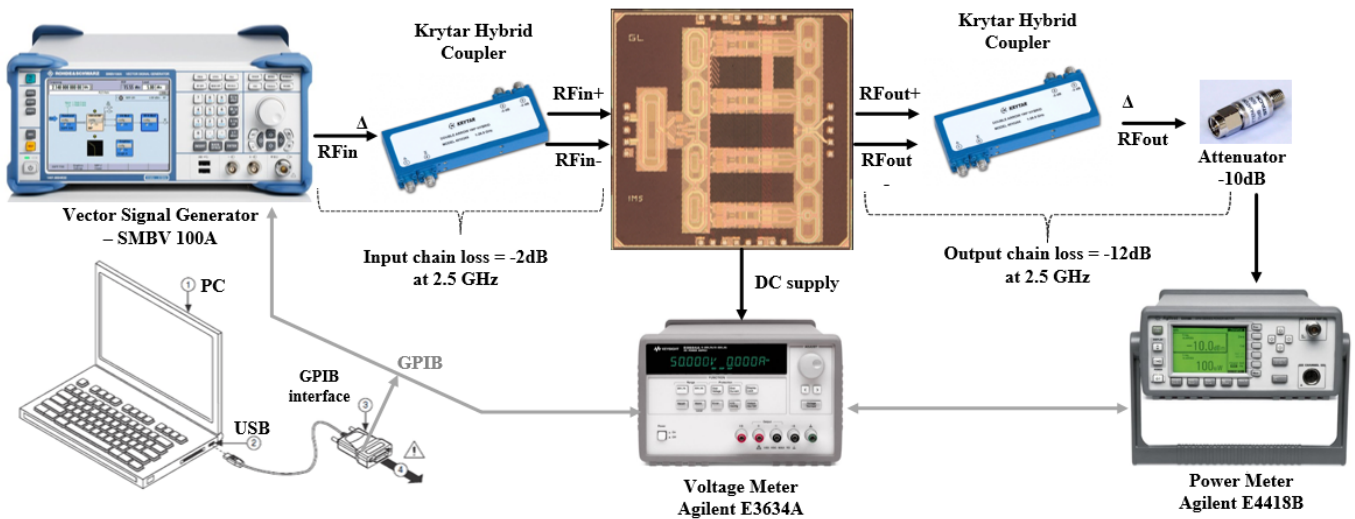


Figure 4-33. 2.5 GHz single-tone signal measurements of the PA

The second test bench is the setup of large signal measurements. This test bench aims to verify the performance of the PA with RF signals at 2.5 GHz. The full test bench is described in Figure 4-33. The setup uses a vector signal generator to generate the 2.5-GHz signal at the input of the PA. The output of the PA is measured by a Agilent power meter. All DC pads are supplied by voltage meters. Two couplers are adopted to transform the single-ended to the differential input signal and vice versa for the output signal. One attenuator -10dB is used between the output coupler and the power meter to ensure the measure power range of the power meter. All equipment is connected via GPIB protocol; measurement results are displayed on a computer via GPIB interface. It is important to note that the input chain loss caused by cables and couplers is -2dB while that in the output is -12dB caused by cables, couplers, and attenuators as well. Large-signal measurements of the PA are also performed at other

frequencies to extract its performance. Therefore, the chain loss at each frequency is needed to recalculate to obtain accurate results.

4.5.2.3 Setup of two-tone signal measurements

The third test bench is the setup of two-tone signal measurements. This test bench aims to verify the performance of the PA with two signals at 2.49 GHz and 2.51 GHz. The details of this test bench is shown in Figure 4-34. This test bench is similar to the one used in one-tone signal measurements. Along with the equipment mentioned in the previous subsection, we also use two vector signal generators, one for a 2.49-GHz signal and another for a 2.51-GHz signal. Two signals are combined by a two-way power combiner. A signal source analyzer is adopted at the end of the test bench to display the spectrum of the output signal. Due to the inclusion of a power combiner into the chain, the input chain loss is increased to -3.5dB. The calculation of the parameters is needed to achieve the most precise results.

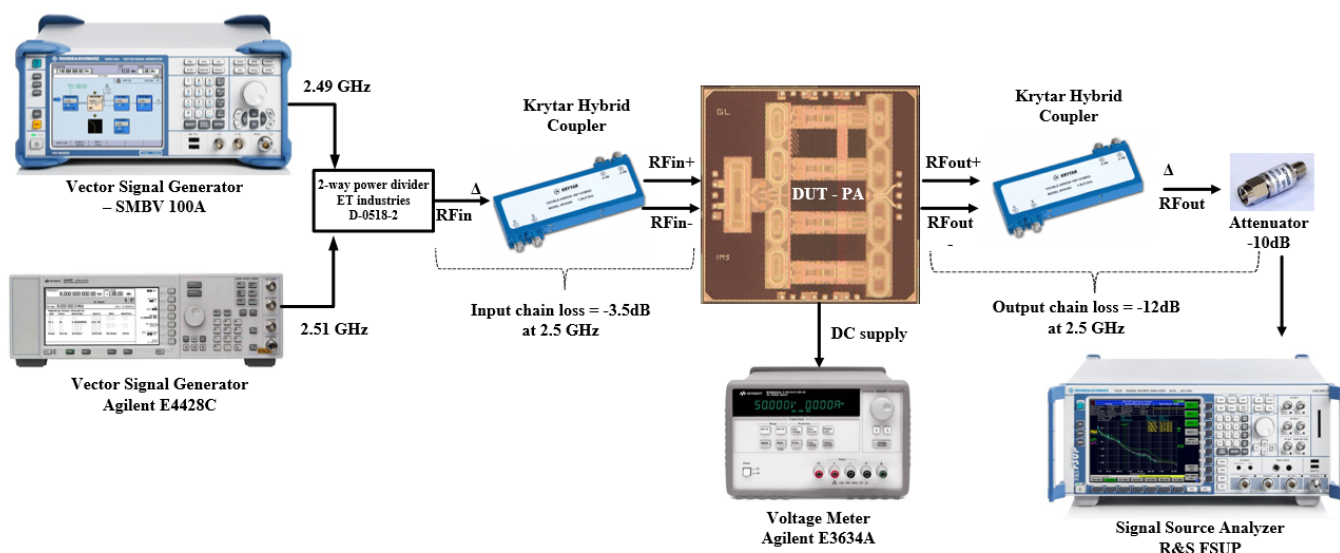


Figure 4-34. 2.49 and 2.51 GHz two-tone signal measurements of the PA

4.5.2.4 Setup of modulated signal measurements

The last test bench is the setup of modulated signal measurements, LTE signal in particular. Figure 4-35 depicts the full setup of these measurements. We use a vector signal generator to generate an LTE signal with 16-QAM modulation, 5-MHz bandwidth for the PA. A vector signal analyzer is used at the output of the test bench to display the performance of the PA regarding EVM, constellations, and eye diagrams of the output signal. This equipment does not support the others parameters such as ACLR and average power.

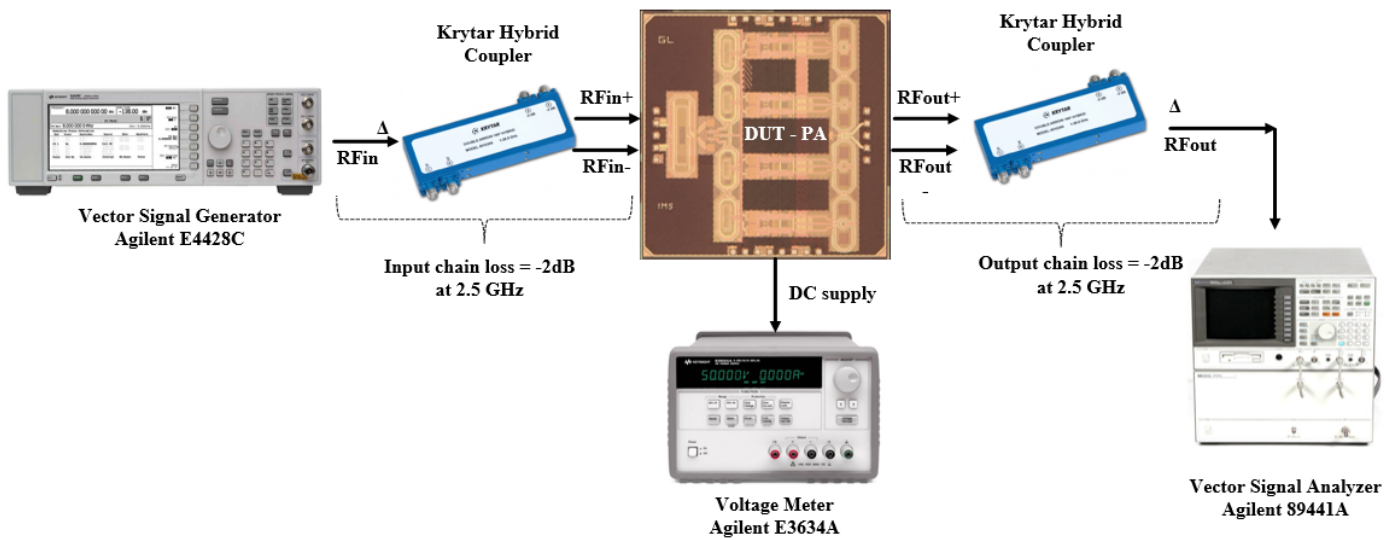


Figure 4-35. Modulated signal measurements of the PA

4.5.3 Experimental and post-layout simulation results

4.5.3.1 Small signal results – S-parameters

Figure 4-36 shows the measured gain (S_{21}), input (S_{11}) and output return (S_{22}) loss, and reverse isolation (S_{12}) of the reconfigurable PA under small-signal conditions in mode 2 (four active power cells) and mode 4 (two active power cells). The multi-mode PA exhibits gains of 32.7 dB and 30.1 dB in mode 2 and mode 4, whereas the mode change causes the gain loss of 2.6 dB including 0.5-dB loss of impedance mismatch. It provides input return losses of -15 dB and -16 dB, and output return losses of -23 dB and -15 dB at 2.5GHz in mode 2 and mode 4, respectively. The reserve isolation is lower than -60dB for all frequency range. Figure 4-37 depicts the measured stability factor (μ) of the PA in mode 2 (four active cells) and mode 4 (two active cells). The experimental results prove the unconditional stability of the PA despite any mode change. The simulated and measured results are in good agreement for all testing frequency range from 1 to 5 GHz. Particularly, the peak-gain differences between the measured and simulated results in mode 1 and mode 3 are 2.8 dB and 2.4 dB, respectively. The peak point of input return loss is slightly shifted from 2.5 GHz to 2.3 GHz, but still maintained at a proper value of 15-dB at 2.5 GHz.

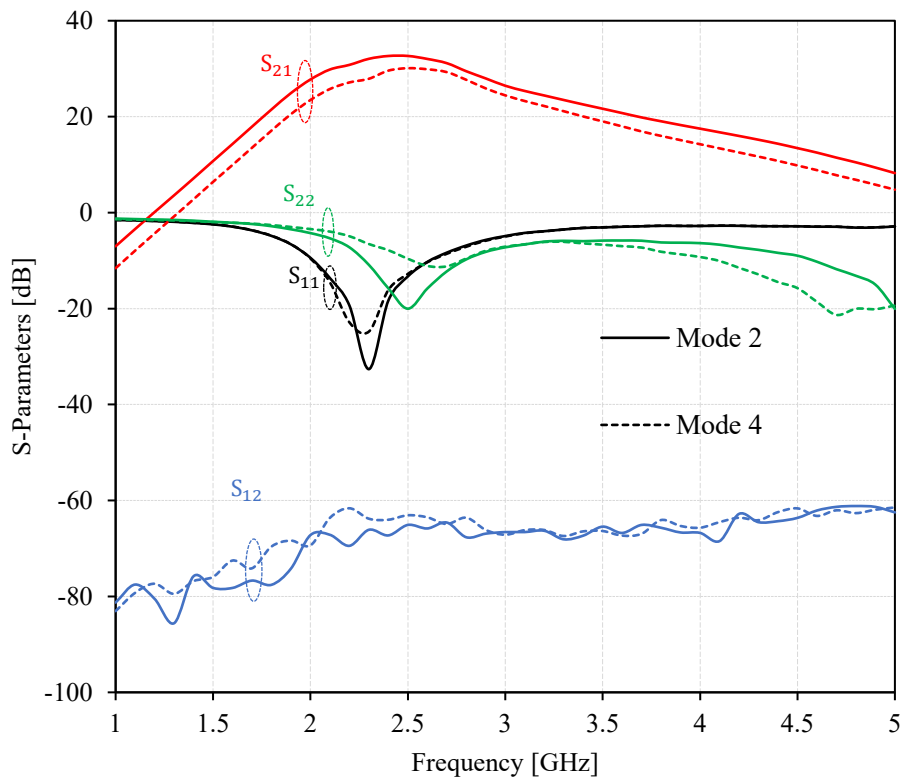


Figure 4-36. S-Parameters of the PA in mode 2 and 4

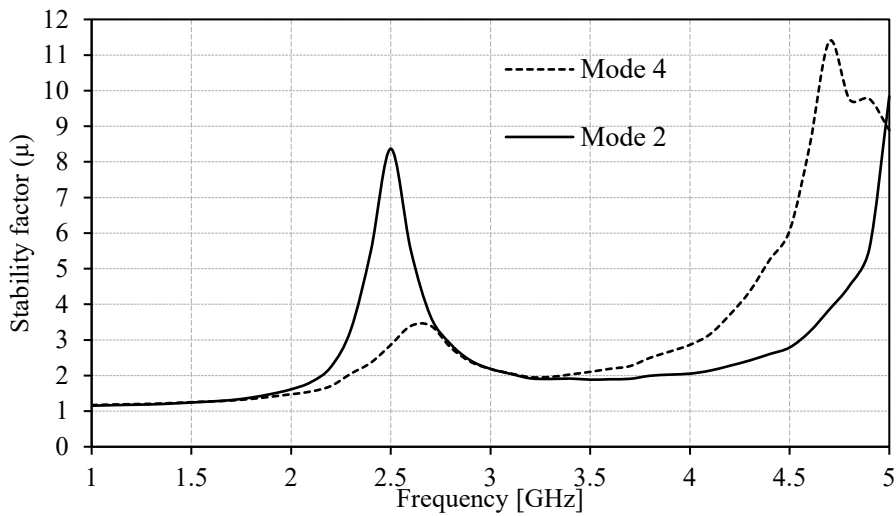


Figure 4-37. Measured stability factor (μ) in mode 2 (4 cells ON) and mode 4 (2 cells ON)

4.5.3.2 Continuous-wave results

After being verified under small signal condition, the PA is tested with the RF signal at 2.5 GHz. The continuous-wave measurement setup was presented in the precedent subsection. To begin with, the comparison between the simulation and the measurement results is depicted in Figure 4-39. As shown in this figure, the PA exhibits an excellent agreement between the simulation and the measurement. Thanks to the “Segmented Bias” technique, two transistors that operate simultaneously help improve the 1-dB compression point of the PA by creating an

extension gain. We can see in Figure 4-39.(c) that the measured DC current is higher than the simulated one. This phenomenon creates a slight degradation on the global PAE of the PA as shown in Figure 4-39.(d).

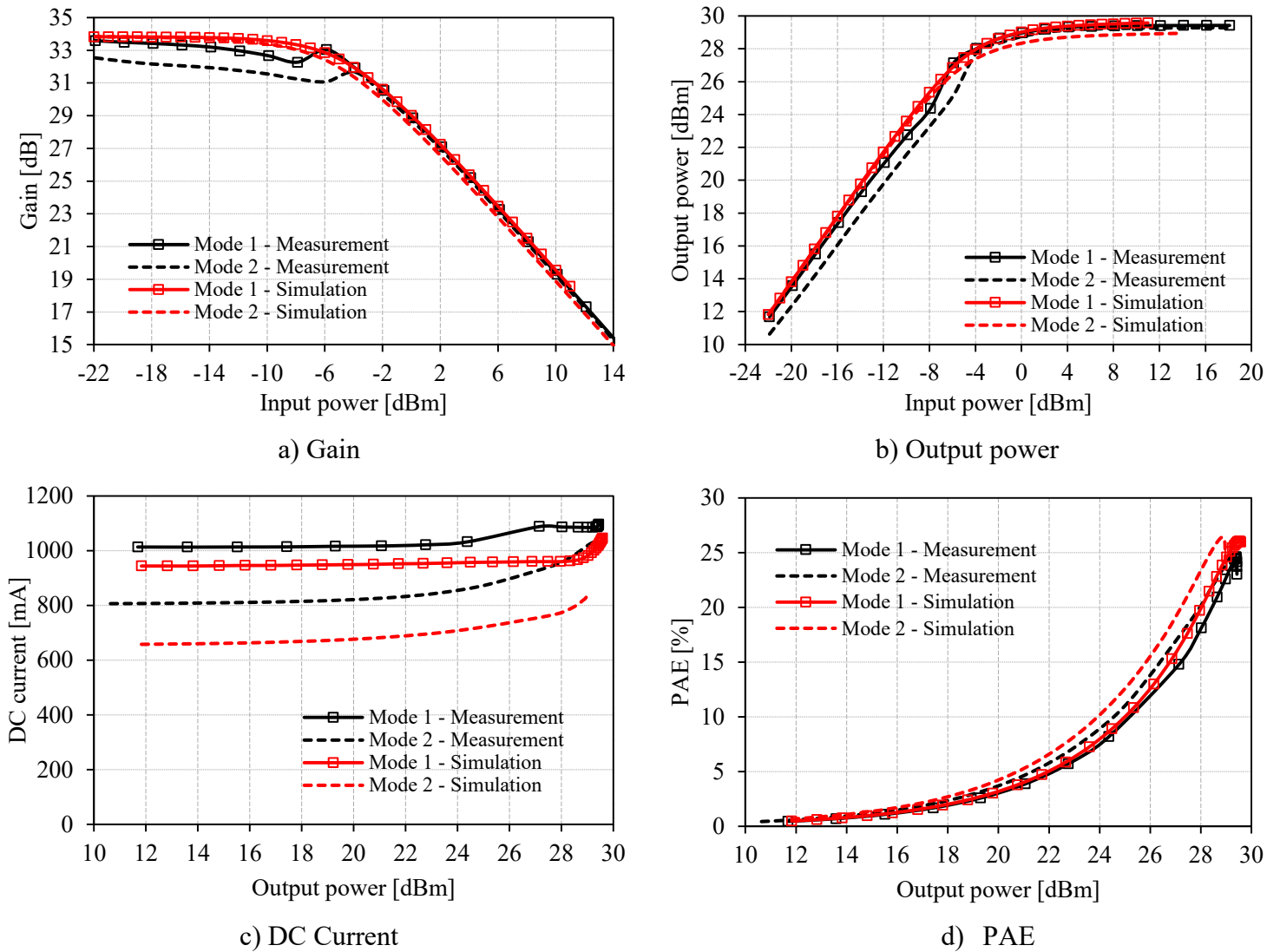


Figure 4-38. Comparison between measured and simulated performances of the PA

As presented in the section 4.4, the PA is configured in four operating modes, which are classified into two power modes: high power, and medium power. Figure 4-39 shows the DC current of the PA in different operating modes. Thanks to the combination of the PCS technique and the SB technique, the DC current is reduced two times from the high power mode to the medium power mode. The maximum DC current of the PA is 1.1A at the peak output power. Figure 4-40 shows the measured output power of the PA. The PA exhibits a saturated output power of 29.5 dBm, which satisfies the specifications of this work. Figure 4-41 depicts the measured gain of the PA. The maximum gain achieved by the PA is 33 dB. The gain of the PA depends on its bias point. When the bias point is changed, there are some impedance mismatches inside the circuit. Therefore, the gain is degraded.

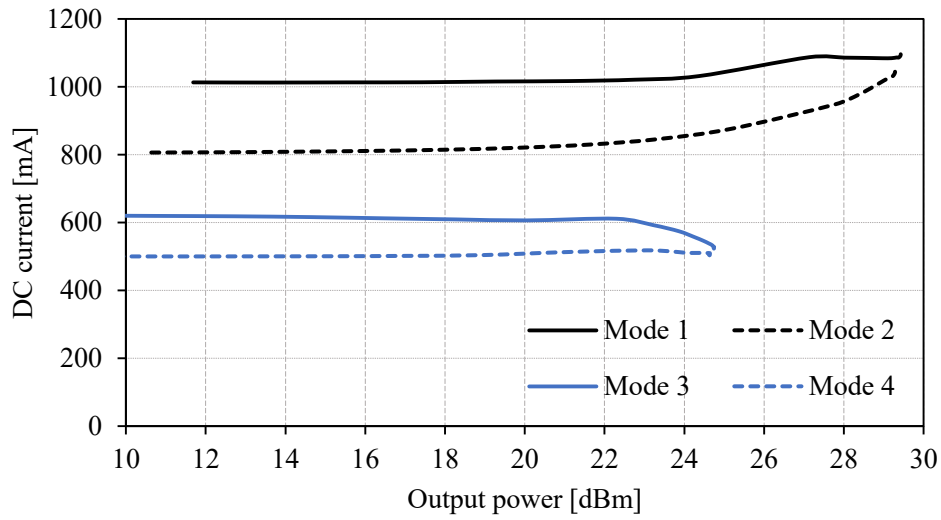


Figure 4-39. Measured DC current of the PA in four operating modes

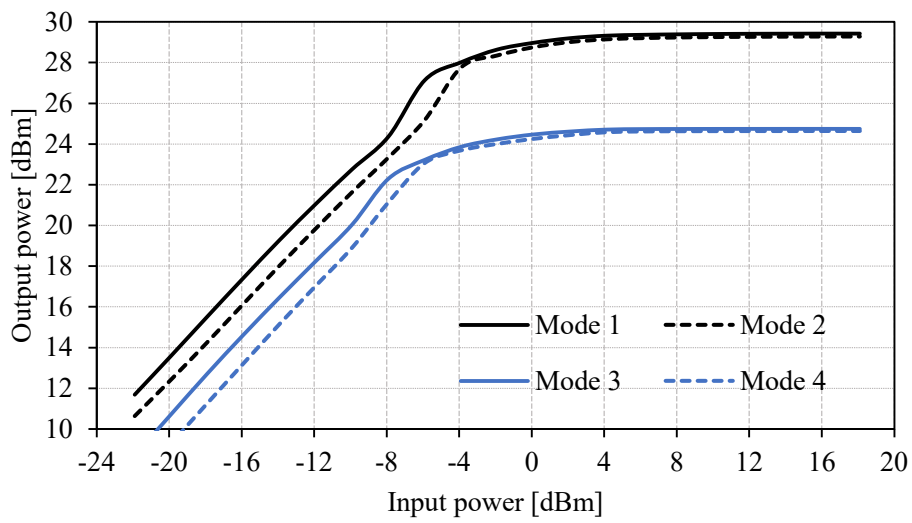


Figure 4-40. Measured P_{out} of the PA in four operating modes

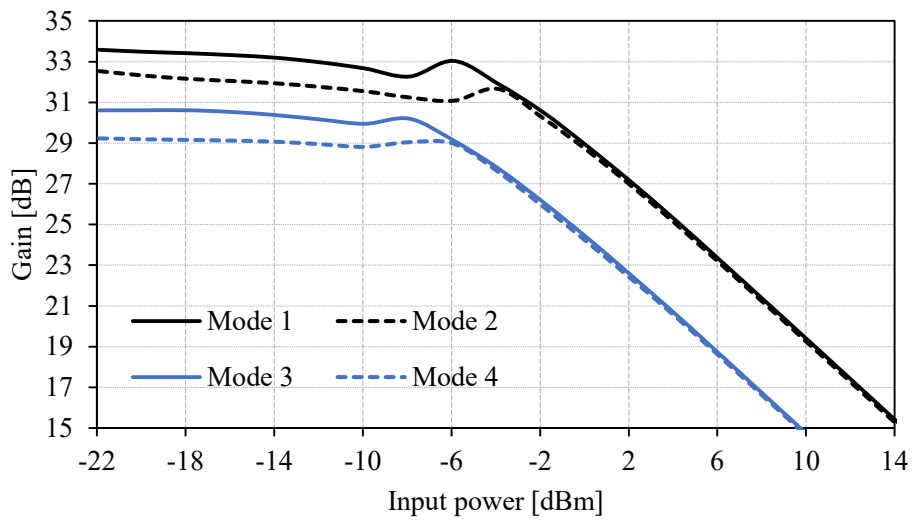


Figure 4-41. Measured Gain of the PA in four operating modes

The most important parameter that decides the functionality of the PA is the PAE. As mentioned in the beginning of the thesis, the goal of this work is to enhance the efficiency in back-off levels. Figure 4-42 shows the efficiency of the PAE in function of output power. Mode 1 aims to maximize the output power of the PA. Mode 2 increases the back-off PAE until 5.5 dB of back-off. From this level, two modes (3 and 4) start working. The highest PAE is 25% at 29.6 dBm of output power. At 5.5dB of back-off output power, the PAE is enhanced with 10% from 7.5% to 17.5%.

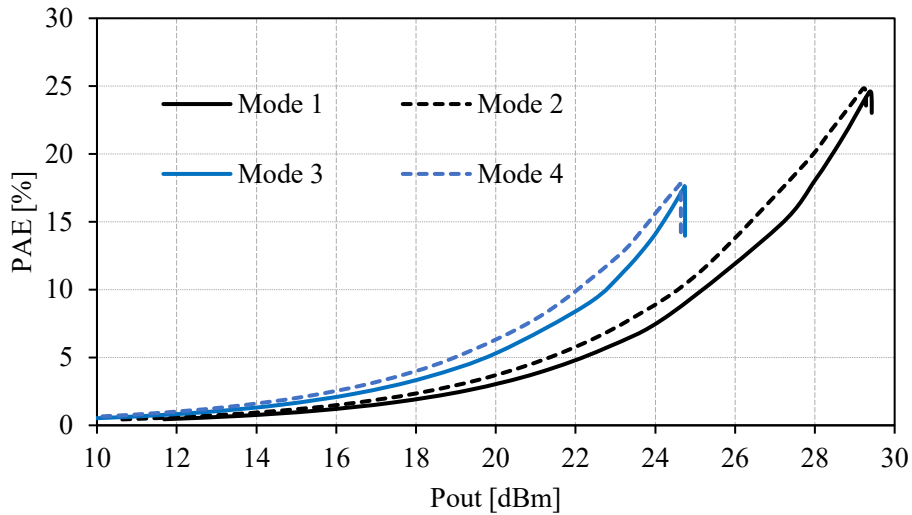


Figure 4-42. Measured PAE of the PA in four operating modes

Figure 4-43 shows the performances of the PA in function of frequency. The PA exhibits a 3-dB bandwidth of 780 MHz that covers the band 7 of the 4G LTE standard from 2.5 to 2.57 GHz. The saturated output power is over 25 dBm for all the frequency range from 2 GHz to 3 GHz. The PAE of the PA is over 15% for the 3-dB bandwidth of the PA.

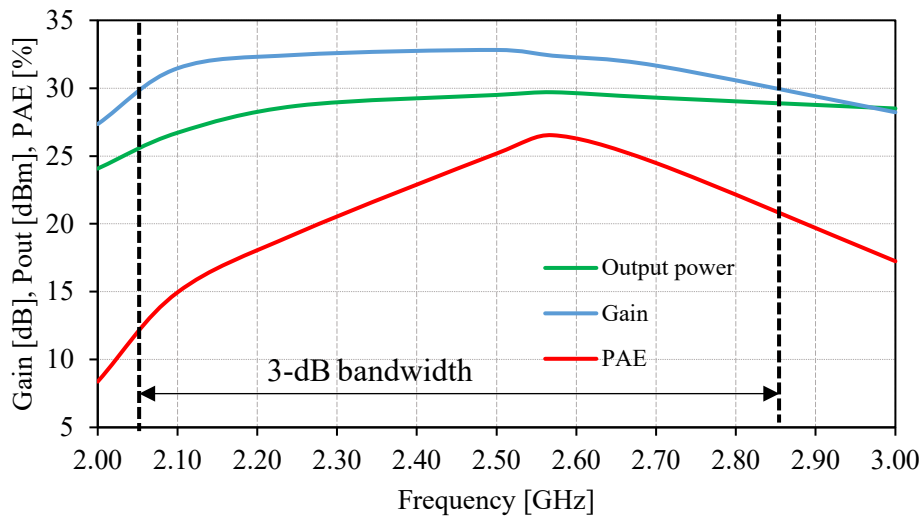


Figure 4-43. Measured Output power, Gain and PAE versus Frequency

Figure 4-44 shows the RF performances of the PA at 2.5 GHz in function of temperature. The PA can provide high output powers over 28 dBm, power gains over 30 dB and PAEs over 19% in the range of temperature from 25°C to 95°C. Higher temperature above 100°C is not taken into measurements.

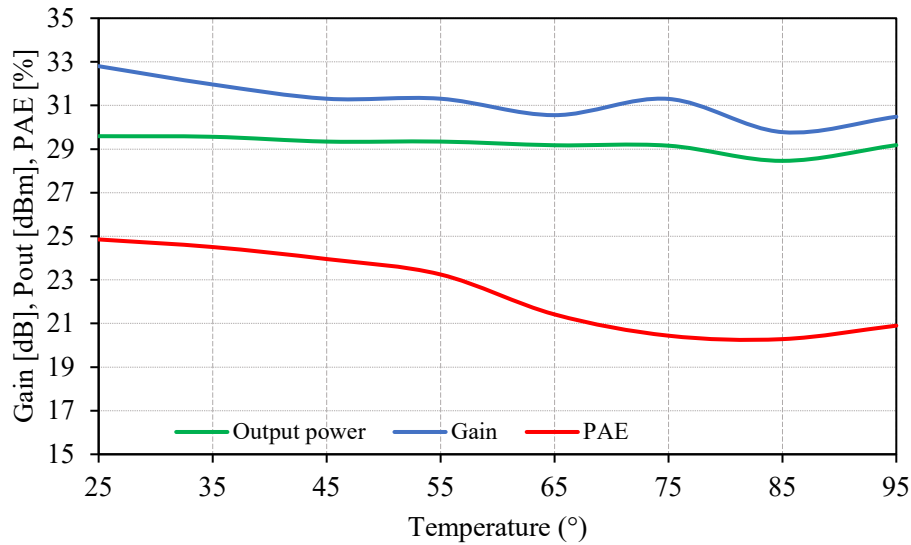


Figure 4-44. Performances of the PA in function of temperature

4.5.3.3 Two-tone measurement results

The reconfigurable power amplifier is tested with two-tone signals. Figure 4-45 displays the screen capture from a spectrum analyzer showing the output spectrum of the designed PA in two-tone signals measurement at the input power of -3dBm. In this measurement, the two fundamental tones at 2.49 GHz and 2.51 GHz were used simultaneously at the input of the PA. The input power levels of the two tones were increased until the saturation power of the PA to extract OIP3 and IIP3 points. It is important to note that the input and output chain losses are taken into account to obtain the most precise measurement results.

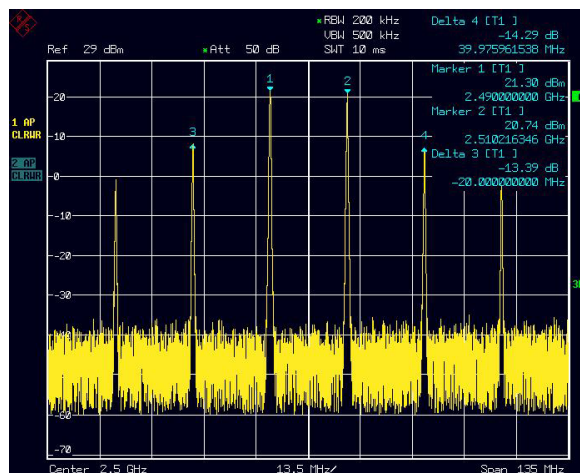


Figure 4-45. The spectrum of two-tone signal measurements at $P_{in} = -3dBm$

Figure 4-46 and Figure 4-47 depict the results regarding 3-order intermodulation level of the PA. Both measurement and simulation results show a reasonable agreement, in which an output power difference of 2 dB from 26.2dBm (simulation) to 24.2 dBm (measurement) for -20 dBc of third-order intermodulation level. In addition, the achieved OIP3 and IIP3 of the PA are 36 dBm and 7.7 dBm, respectively. These levels ensure a proper function of the PA thanks to its high linearity.

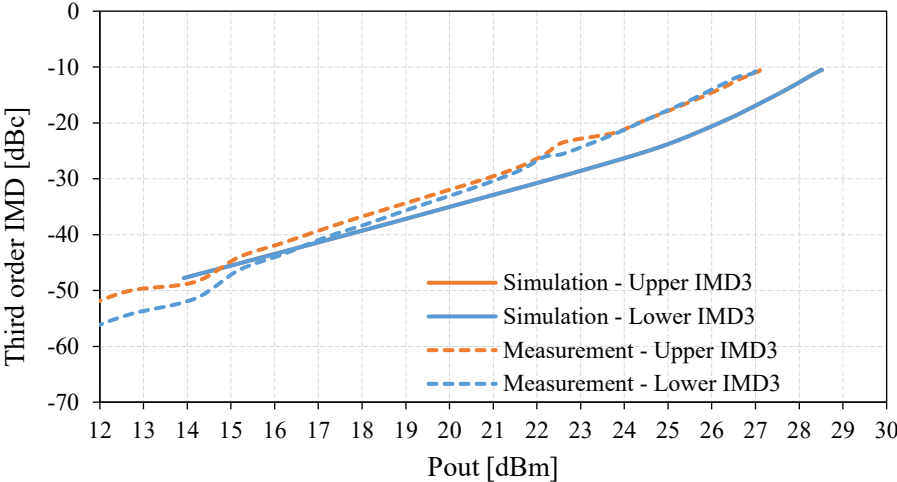


Figure 4-46. IMD3 of the PA in measurement and simulation

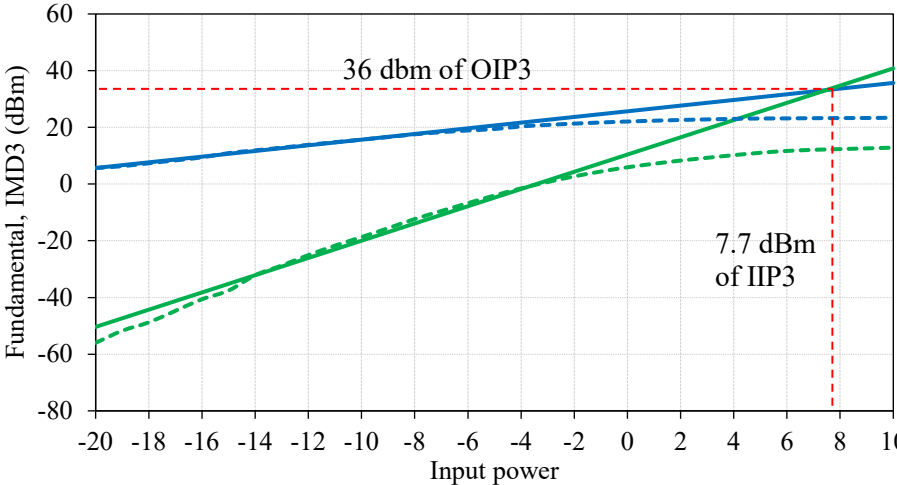
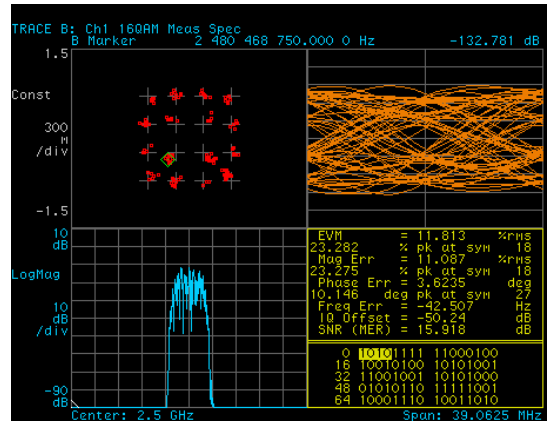
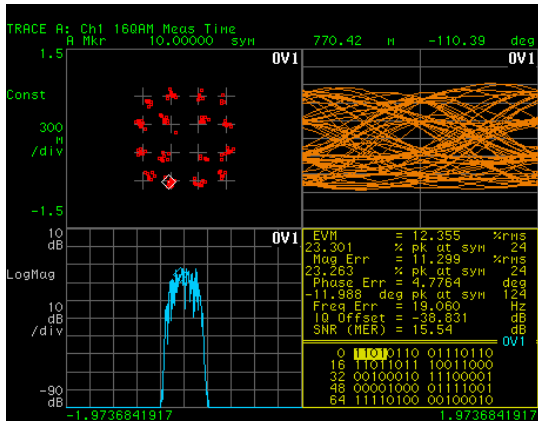


Figure 4-47. Measured OIP3 and IIP3 of the PA

4.5.3.4 LTE signals with 16QAM modulation and 5MHz of bandwidth

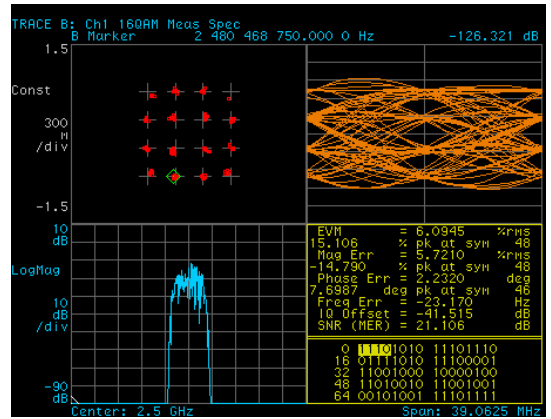
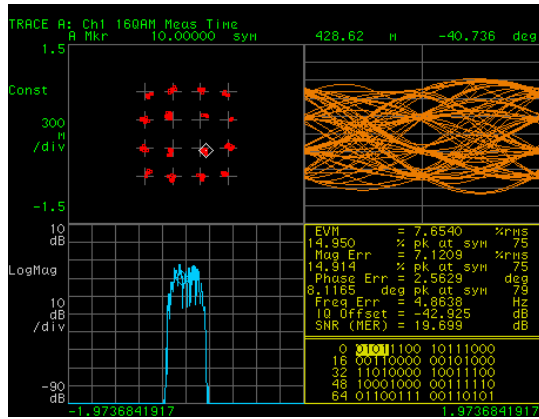
After verifying the two-tone signal performance, the PA is tested with an LTE signal having 16QAM modulation and 5MHz of bandwidth. Due to limited supported function of measurement equipment, only EVM among modulated signal parameters is reported in this subsection. The measurement setup as presented also takes the input and output chain loss into account to extract the proper results. Figure 4-48 and Figure 4-49 show the EVM of the PA in two input power levels.



a) EVM in case of 4 cells ON

b) EVM in case of 2 cells ON

Figure 4-48. EVM of the PA at $P_{in} = 2\text{dBm}$ in two operating cases



a) EVM in case of 4 cells ON

b) EVM in case of 2 cells ON

Figure 4-49. EVM of the PA at $P_{in} = -2\text{dBm}$ in two operating cases

As seen in these figures, the EVM results reflect the linearity of the PA; the PA introduces excellent EVM levels until an input power of 2 dBm despite any mode change. Figure 4-50 illustrates the measured EVM of the PA in function of input power for two operating modes (mode 2 and mode 4). The EVM of the PA respects the requirement of 12.5% (16QAM signal) until an average input power of 2 dBm.

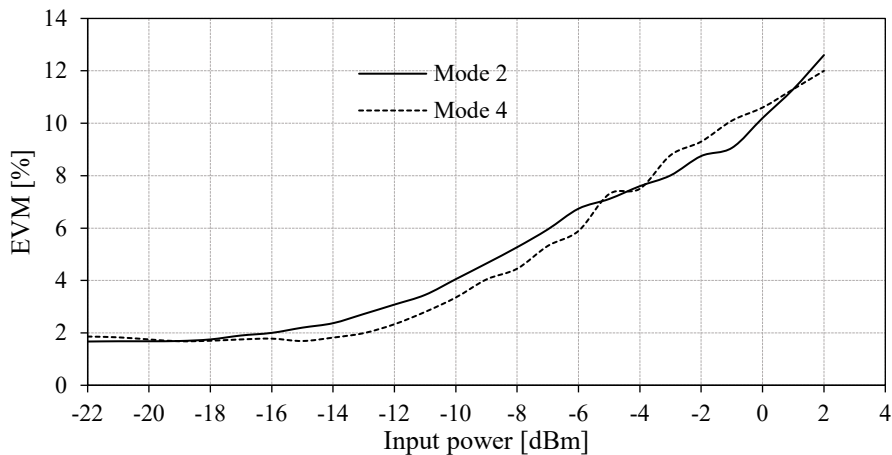


Figure 4-50. Measured EVM of the PA in two operating modes

4.5.4 Comparison with state-of-the-art silicon power amplifiers

Table 4-6 depicts the performance comparison between this PA and state-of-the-art RF silicon PAs. The PA proposes a new method to enhance the RF performance and obtain the efficiency-linearity tradeoff by using the power cell switching and the segmented bias technique. The chip occupies a size of 3.4mm². The figure-of-merit (FoM) and GBWP (Gain×BW) parameters indicate the trade-off of power amplifiers between RF performances (gain, PAE, output power) and the operating bandwidth. The performance of the multi-mode broadband PA presented in this work features the highest figure-of-merit and GBWP among recently reported silicon PAs. The 3-dB bandwidth of the PA achieves 780 MHz or 32.2% of fractional bandwidth.

Table 4-6. Comparison with state-of-the-art recently reported silicon PAs

Parameter	This work [PLS]	This work [Measured]	[56]	[57]	[58]	[51]	[59]	
Freq. [GHz]	2.5		2.3	2.4	1.8	1.8	2.4	
Technology	65nm		90nm	180nm	110nm	180nm	180nm	
Approach	PCS + Segmented bias		PCS	PCS+ Self-biasing	Broadband impedance matching	MGTR ^a	Transistor resizing	
PAPR [dB]	8		7.4	5	-	-	-	
Size [mm ²]	3.4		4.32	1.47 ²	2.63	1.92	2.3	
Supply [V]	3.3	3.3	3.3	5.8	3.4-3.5	-	3.3	
3-dB bandwidth	720 MHz	780 MHz	700 MHz	500 MHz	300 MHz ³	400 MHz ³	650 MHz	
Psat [dBm]	29.8	29.5	30	29	28	28	22.5	
Gain [dB]	34	33.5	27.5	22	30	24.8	18.2	
PAE [%]	@Psat	27.2	25	33	27	33	33	19
	@OBO = 3dB	21	18	27	21	-	25	13
	@OBO = 6dB	19	15	16	13	-	17	7
	@OBO = 8dB	12.5	11	10	17.5	-	12	12
FoM ¹ [W.GHz ²]	4078	3317	1127	280	715.5	197.6	12.85	
Gain×BW	23.8	25.3	19.6	11.5	9	9.92	11.83	

¹ FoM= Psat×PAE×Gain×Freq² ² Off-chip baluns ³ Graphically estimated ^aMulti-gate transistor

4.6 Conclusion

This chapter has presented the design of the fully integrated reconfigurable CMOS power amplifier. Such an architecture has the potential of breaking the efficiency-linearity trade-off inherent in linear power amplifiers. The power amplifier adopts two techniques to overcome this trade-off constraint: the segmented bias technique, and the power cell switching technique. The detailed design of four power cells, driver and three transformers is reported in this chapter. The PA can be configured to operate in four modes thanks to the SB technique and the PCS

technique. The power amplifier can deliver high output power, efficiency and respect the stringent linearity of modulated signals. The linearity of the PA has been verified using both single-tone, two-tone and modulated signals. The measurement setups for each verification have been reported to extract the most precise results.

5 GENERAL CONCLUSION

5.1 Thesis summary

Wireless communication has been the buzzword in mobile devices. Explosive growth in wireless communication market demands for low-cost, small-size and low-power terminals. The fully integrated handset is the most effective way to provide such a solution. In radio transceivers, the power amplifier is one of the critical building blocks. As the most power-consuming element in such system, the radiofrequency power amplifier requires being integrated as an inseparable part of the integration chart with the rest of radio building blocks. This thesis studies vital issues in the design and implementation of fully-integrated efficient CMOS power amplifiers at RF and focuses on the design of a 4G LTE power amplifier dedicated to unmanned aerial vehicles applications.

In addition to the full integration of PAs, the battery life of handsets is mostly dominated by the power efficiency of PAs. It is well known that a PA only achieves its maximum efficiency at the peak output power. As PAs move backward in output power, their efficiency decreases as well. Nevertheless, the need of conserving the battery life and mitigating interferences to other users necessitates a power transmission lower than the peak level. Besides, a modern complex modulation scheme such as orthogonal frequency-division multiplexing (OFDM) exhibiting a high peak-to-average power ratio (PAPR), RF PAs require high efficiency, in both back-off power level and peak power level, and stringent linearity. Linearization technique improves the linearity but degrades the efficiency. Efficiency enhancement technique, on the other hand, can make PAs more efficient but not linear. Therefore, the need to combine linearization and efficiency enhancement techniques is taken into account for RF PAs to obtain the linearity-efficiency tradeoff. The power cell switching (PCS) technique introduces a flexible power configuration for PAs to operate in multiple modes by combining output power from unit power cells. To push upper back-off efficiency, the segmented bias (SB) is used for power cells. The combination of both techniques allows this PA not only to solve the give-and-take problem but also to extend the battery life of mobile devices.

One of the critical challenges in any PA is the design of impedance matching network. The area and the power efficiency of this kind of network plays an essential role in the performances of PAs. Besides, CMOS technologies introduce lossy substrate that causes lossy on-chip passive circuits. Therefore, the need of low-loss matching network, which is transformers in this work, is necessary to the power efficiency of the PA. Through an in-depth investigation on transformers' topologies, this work adopts the four-way stacked-metal

transformer with power combining in series. This transformer not only donates decent advantages to the PA's operation but also helps offset the impedance modulation whereas it works along with the tuning capacitors.

This thesis starts with an overview of power amplifier design for 4G LTE applications in unmanned aerial vehicles, compares prevalent technologies for RF power amplifiers, especially CMOS technologies, and provides the critical specifications of the PA design. After that, the advantages and limitations of each transformer design are studied in depth to choose the most appropriate structure for the PA. The full design of the PA is detailed from the transformers to the power cells and the driver cell. A prototype of the PA has been demonstrated on the TSMC 65-nm CMOS technology. The PA provides a power gain of 32.8 dB, a saturated output power of 29.5 dBm and a maximum PAE of 25.2%. The PA is verified with an LTE signal having 5-MHz BW and 16-QAM modulation. The linearity of the PA is validated with EVM under 12.5% for average output power under 24 dBm. The PA provides a high OIP3 of 36 dBm after being verified with two-tone signals, 2.49 and 2.51 GHz. With a 3-dB bandwidth of 780 MHz or 32.2% of fractional bandwidth, the PA can cover a more extensive operating frequency band including band 7 of LTE. Despite its initial purpose to be used in LTE applications, experimental results demonstrate the potential of the PA's design to be adopted in the lower 5G band (3.4-3.8 GHz) thanks to its broadband characteristic.

5.2 Future directions

Almost every research contributes to the profound understanding of the specific subject. Also, it can open the door to other new topics. This work is the case. The transformer-based bias-segmented power amplifier demonstrates excellent potentials in impedance modulation and supply modulation, which are two most pursuing themes in PA design. Hence, the author would like to imply some future directions for two these themes. For impedance modulation, the combination of tuning capacitors and transformers introduces an intermediate value instead of zero in the inactive state of power cells and allows reducing impedance mismatch. A new matching design is suggested to optimize the impedance compensation. This new design can adopt varactors to implement a flexible matching network [60] or use a novel hybrid coupler [61] to control the impedance modulation of the PA in case of power mode changes. Figure 5-1 depicts a proposed solution to optimize the impedance modulation of the PA by using varactor-based matching networks. Such networks allow bringing the off-state impedance of two middle cells back to their on-state impedance. The impedance mismatch between the power cells and the output transformer can be eliminated, and the power efficiency is conserved as a result. Since varactors are non-linear and fragile under high power, this research direction needs to be paid attention on the robustness of varactors.

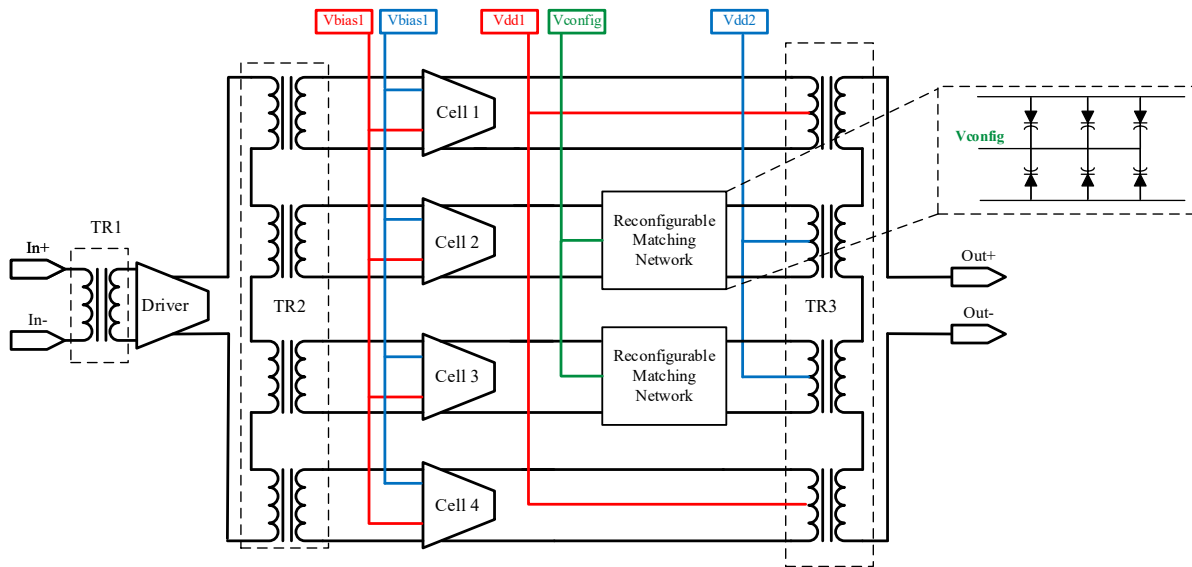


Figure 5-1. Proposed varactor-biased matching network for impedance modulation

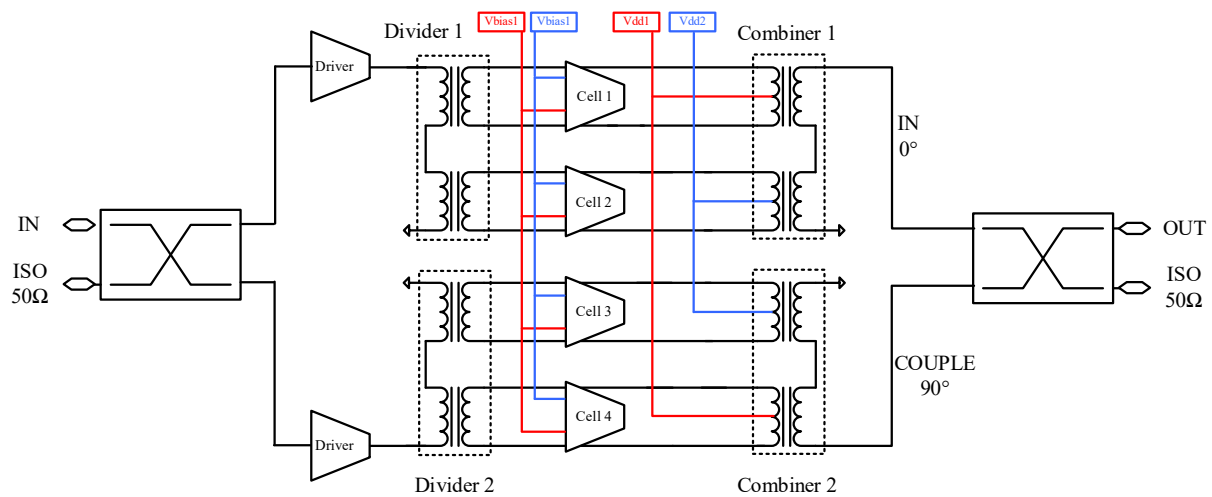


Figure 5-2. Proposed architecture with two hybrid couplers for impedance modulation

Figure 5-2 illustrates another proposed approach to control impedance modulation by using hybrid couplers. The PA shows an advantage on saving the size of RF building blocks by integrating a differential-to-single-ended signal converter. This method offers an excellent approach to co-integrate the antenna in the same chip. This approach, on the other hand, poses another challenge about the phase of two signals inputted to the output hybrid coupler. It is important to note that these two signals required having a 90° phase difference.

For supply modulation, the author would like to propose a transformer-based power detector to detect the output power and return the DC bias for the unit power cells. This power detector contains two parts: the transformer with two integrated sense windings and an operational amplifier. This approach can provide an autonomous bias system for the PA. When the PA switches from the high-power mode to the medium-power mode at a given output power, the power detector will detect this range of output power by two sense windings and return the required bias voltage for the unit power cells to push the global PA to its peak output power.

Along with these advantages, there are also two main challenges for this approach. First, the output transformer needs to be redesigned with two sense windings, which anticipate the transition point between two power modes for unit power cells. Second, the output bias voltage from the sense windings is not high enough to supply for the unit cells. An operational amplifier (OPA) is required to boost this level to its correct level at a right moment of mode change. Such amplifier, which can consume an amount of power, potentially reduces the efficiency of the PA. It is thus essential to design a low-power operational amplifier.

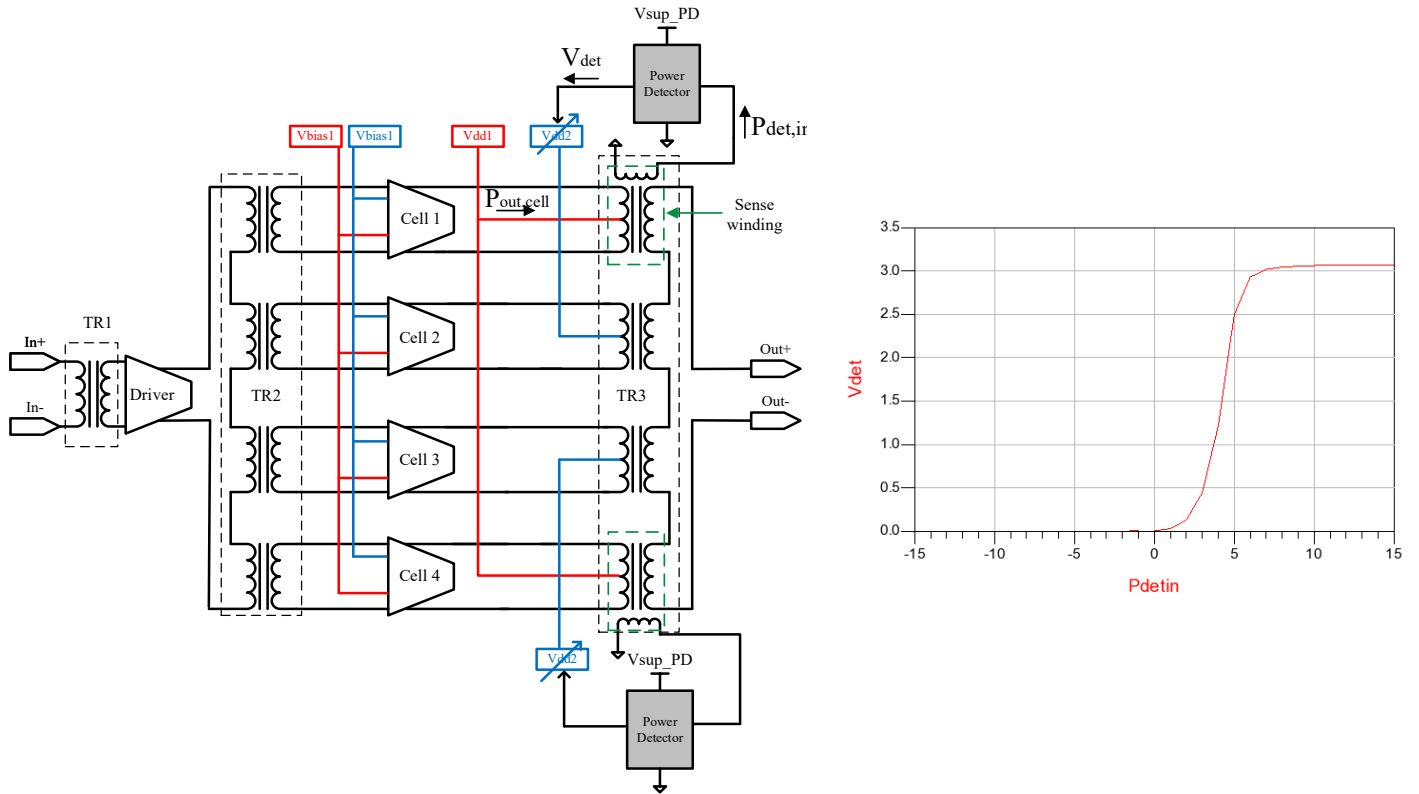


Figure 5-3. Proposed integrated sense-winding transformer with a power detector

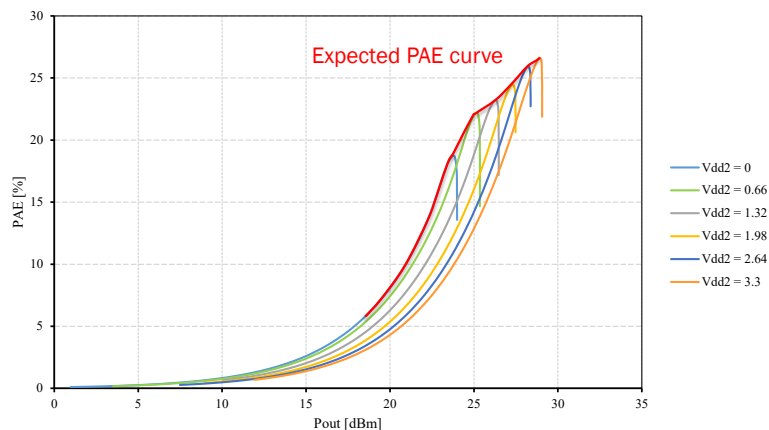


Figure 5-4. Expected PAE curve of the PA with the proposed power detector

Figure 5-3 depicts the proposed transformer-based power detector with two sense windings. The sense windings need to be integrated inside the output transformer; so they make

the transformer larger and lossier. A demonstration design is performed to illustrate the viability of this method. The sense winding detects the transition point of mode change at 5-dBm of $P_{\text{det,in}}$ and outputs the DC bias of 3.1V for the two middle unit cells. Figure 5-4 shows the expected results of the proposed method. When the supply source is modulated, the PAE is enhanced in the back-off output power level. The expected PAE curve is traced through the peak of these PAE curves from the OFF state to the ON state of two middle cells.

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A APPENDIX – CMOS RESTRICTIONS

A.1 Latch-up

Latch-up is defined as a high-current state that semiconductor device undergoes due to the interaction between two bipolar transistors, npn and pnp. It creates a low-impedance path from a PNP parasitic structure between the power supply rails, V_{dd} and V_{ss} . This parasitic structure is usually equivalent to a thyristor (or SCR). During a latch-up event, when one of the transistors starts conducting, the other one also begins its operation. The injected minority carrier concentrations are increased higher than the doping concentrations of N-well and P-well. As a consequence, these two layers disappear eventually, and a low-impedance path appears between V_{dd} and V_{ss} due to a dense conductivity region. They both keep each other in saturation as long as the structure is forward-biased. This effect may cause a circuit malfunction, and destroy the device in the worst case.

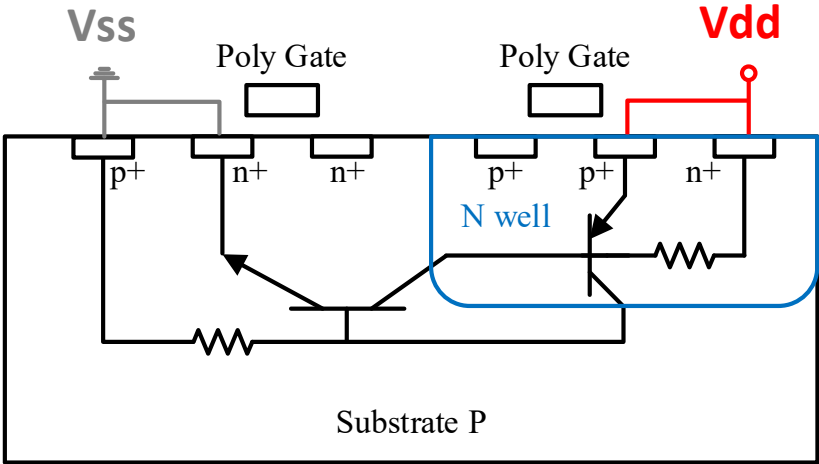


Figure A-1. Intrinsic bipolar junction transistors in the CMOS technology

CMOS integrated circuit is more susceptible to latch-up at higher temperatures. Due to the inherent potential of latch-up in CMOS devices, it is crucial to adopt latch-up prevention techniques. One of the most popular methods in a semiconductor process is adding a layer of insulating oxide (usually called a *trench*) that surrounds the NMOS and PMOS transistors. This method eliminates the parasitic thyristor (or SCR) structure between these transistors. Most silicon-on-insulator devices are latch-up resistance thanks to an additional layer under the gate. To minimize the failure probability of CMOS devices, decoupling power supply rails with large decoupling capacitors is required. The needed value of these capacitors is dependent on the operating frequency; it varies from 0.01nF to 1 μ F.

A.2 Antenna effect

The antenna effect is an effect that potentially causes yield and reliability problems during the fabrication of MOS integrated circuits. The design rule usually contains antenna rules to avoid this problem [63]. A violation of such rules is called an antenna violation. Figure A-2 illustrates the antenna effect during the fabrication. Once the chip is fabricated, the effect cannot happen as shown in Figure A-2.(a) because every net is connected some source/drain of transistors. The source/drain implant forms a diode that protects the gate oxide. During the fabrication, the gate oxide, on the other hand, is not protected by a diode as shown in Figure A-2.(b). If a charge is added to the metal 1 by accident, it can increase to the level of gate oxide breakdown, which is illustrated by the lightning bolt symbol.

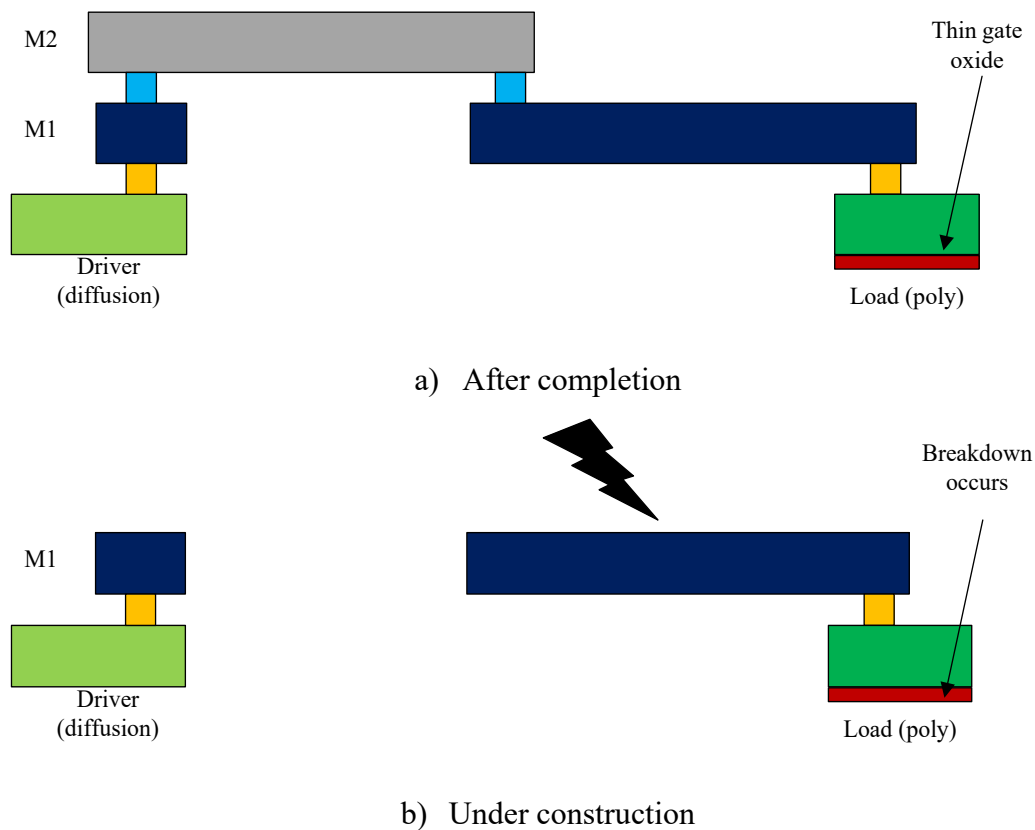
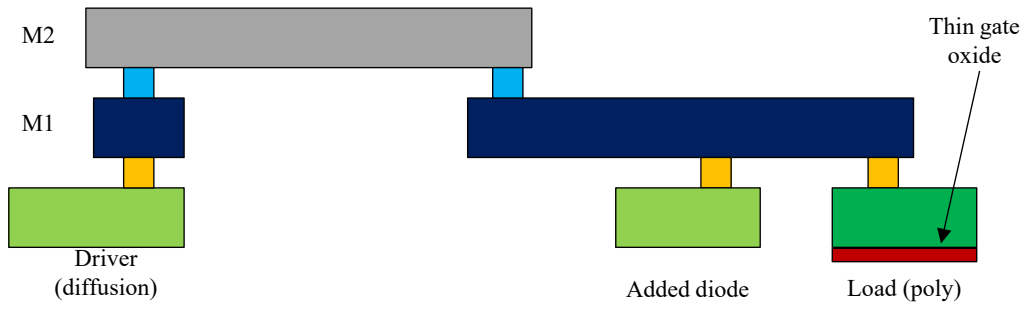
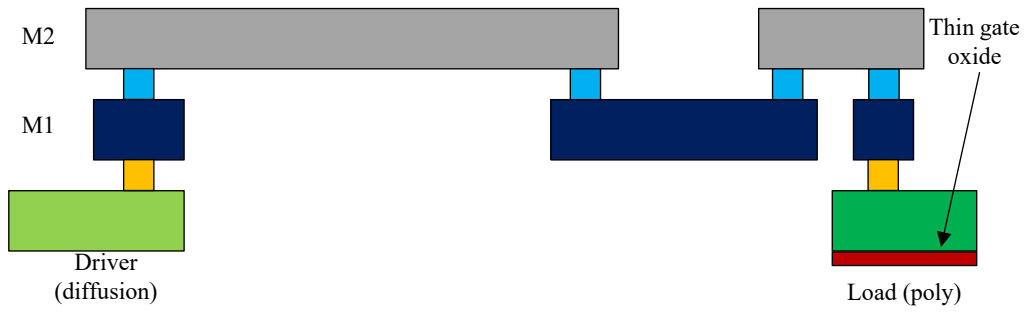


Figure A-2. The cause of antenna effect during the fabrication

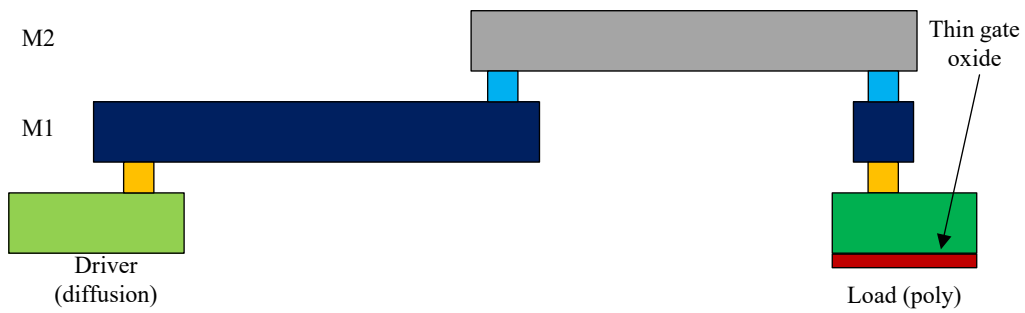
Antenna violation must be fixed by the routing. Routing techniques are thus essential in RFIC design to ensure the reliability of integrated devices. Figure A-3 illustrates three favorite routing techniques to fix the antenna effect. The first one uses a diode connected to the net close to the gate. This diode can be formed by a MOSFET source/drain. It is important to recalculate the circuit speed and power consumption due to this added diode. The second one adds vias near the gate to connect it to the highest used metal layer. The last one uses the highest layer metal layer connecting directly to the gate.



a) Add a diode to the net next to the gate



b) Add vias near the gate to connect the gate to the highest used layer



c) Change the order of the routing layer

Figure A-3. Routing techniques to fix the antenna effect

A.3 Parasitic capacitances of CMOS transistors

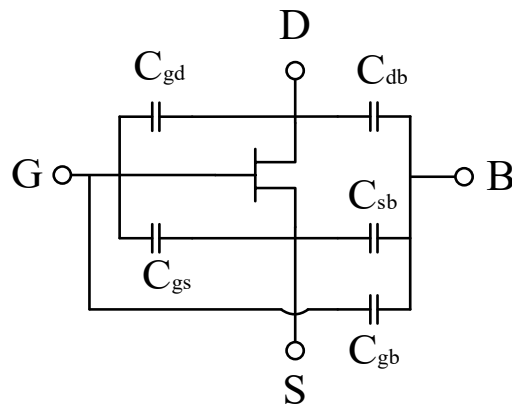


Figure A-4. Parasitic capacitances inside a MOS transistor [62]

There exists a capacitance between two of four terminals of a MOS transistor. These capacitances are illustrated in Figure A-4. Parasitic capacitances affect the performance of transistors by changing its input and output matching. Among these capacitances, the gate-source capacitance C_{gs} is the most critical one that influences the input signal of the transistor. Besides, the power gain of the transistor is also susceptible to the gate-drain capacitance. Therefore, it is vital to design input and output signal paths with the less existed parasites as possible to ensure the performance of the transistor. The detailed design of unit power transistors is presented in Chapter 4 with a four-stacked-metal (M1-M2-M3-M4) input path and a five-stacked-metal (M5-M6-M7-M8-M9) output path.

B APPENDIX – RELIABILITY OF POWER AMPLIFIER

B.1 Electromigration

Electromigration decreases the reliability of integrated circuits. It causes the loss of connections or failure of a circuit. In advanced semiconductor processes, copper has replaced aluminum as the interconnection material choice. Despite its superior conductivity, copper introduces greater fragility in manufacturing. Electromigration is one of the most critical challenges to device fabrication. Recent EDA tools allow circuit designers to check and correct electromigration problems at the transistor layout level. However, the interconnection verification is always in demand, especially for the metal line, via, stacked via, contact under normal operating condition. Table B-1 provides information to evaluate the quality of 65nm copper process and to determine the electromigration lifetime. The information is based on the design rule manufacturing of the TSMC 65nm CMOS process.

Table B-1. Max. DC Current at a junction temperature of 110°C

Metal wiring level	Metal length, L (μm)	I_{max} (mA)
M1	$L \geq 20$	$1.509 \times (w-0.0016)$
	$20 > L > 5$	$(20/L) \times 1.509 \times (w-0.0016)$
	$L \geq 5$	$4 \times 1.509 \times (w-0.0016)$
Mx (from M2 to M7)	$L \geq 20$	$1.877 \times (w-0.0016)$
	$20 > L > 5$	$(20/L) \times 1.877 \times (w-0.0016)$
	$L \geq 5$	$4 \times 1.877 \times (w-0.0016)$
M8	$L \geq 20$	$8.096 \times (w-0.0016)$
	$20 > L > 5$	$(20/L) \times 8.096 \times (w-0.0016)$
	$L \geq 5$	$4 \times 8.096 \times (w-0.0016)$
M9	$L \geq 20$	$11.316 \times (w-0.0016)$
	$20 > L > 5$	$(20/L) \times 11.316 \times (w-0.0016)$
	$L \geq 5$	$4 \times 11.316 \times (w-0.0016)$
Contact (size: $0.1 \times 0.1 \mu\text{m}^2$)	Any length of metal	0.296 per contact
Vx (size: $0.1 \times 0.1 \mu\text{m}^2$)	$L \geq 20$	0.158 per via
	$20 > L > 5$	$(20/L) \times 0.158$ per via
	$L \geq 5$	4×0.158 per via
V7, V8 (size: $0.36 \times 0.36 \mu\text{m}^2$)	$L \geq 20$	3.077 per via
	$20 > L > 5$	$(20/L) \times 3.077$ per via
	$L \geq 5$	4×3.077 per via

B.2 ESD Protection

As presented in Chapter 2 of the thesis, electrostatic discharge is one of the factors causing the failure of an integrated circuit. It is thus vital to design a protection circuit for this effect. The design of this PA also includes the ESD protection circuit and DC coupling capacitor at DC pads to reduce the failure probability of the PA. Figure B- illustrates the design of two DC decoupling capacitors at DC pads for the power cells. These capacitors along with the decoupling capacitors of RF probes help eliminate the oscillation signal under DC condition. Figure B-6 shows the ESD protection circuits for gate bias pads. The circuit is composed of two PN diodes and mostly used to protect the gate of power transistors.

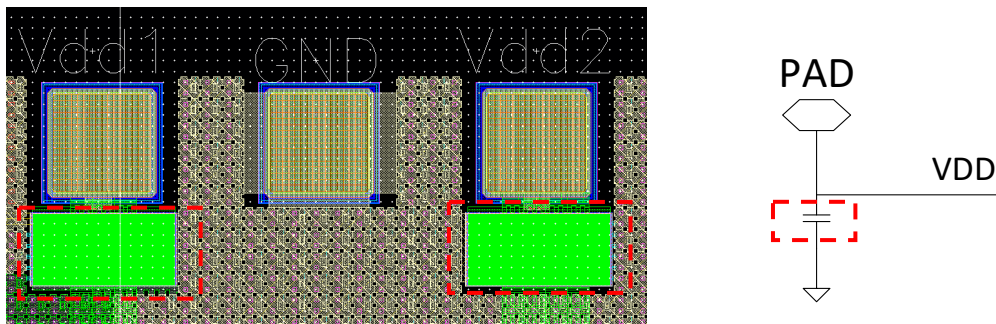


Figure B-5. DC decoupling capacitor for DC pads

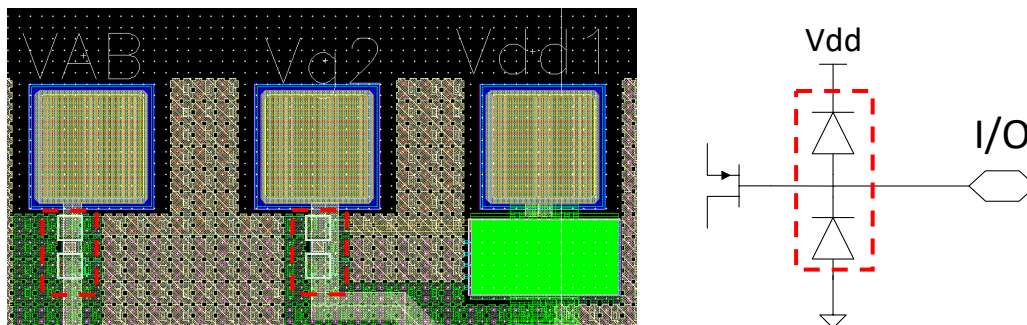


Figure B-6. ESD protection circuits for gate bias pads

B.3 DC generator test

The measurements of PAs suffer many parasites in cables connected between the DC supply and the chip. These parasites exist in RF probes, in interconnecting cables, and inside the DC supply. It is hence essential to build an equivalent model of these parasites and simulate them before sending the final layout to the foundry. This subsection presents the equivalent model used in this test. Figure B-7 shows the test bench of this simulation and the equivalent model of cables connected to DC sources. In practice, the inductance of cables is $1\mu\text{H}/\text{m}$, and the decoupling capacitor at RF probes is 100nF . The simulation is required to perform for every DC supply source from the driver cell to the power cells.

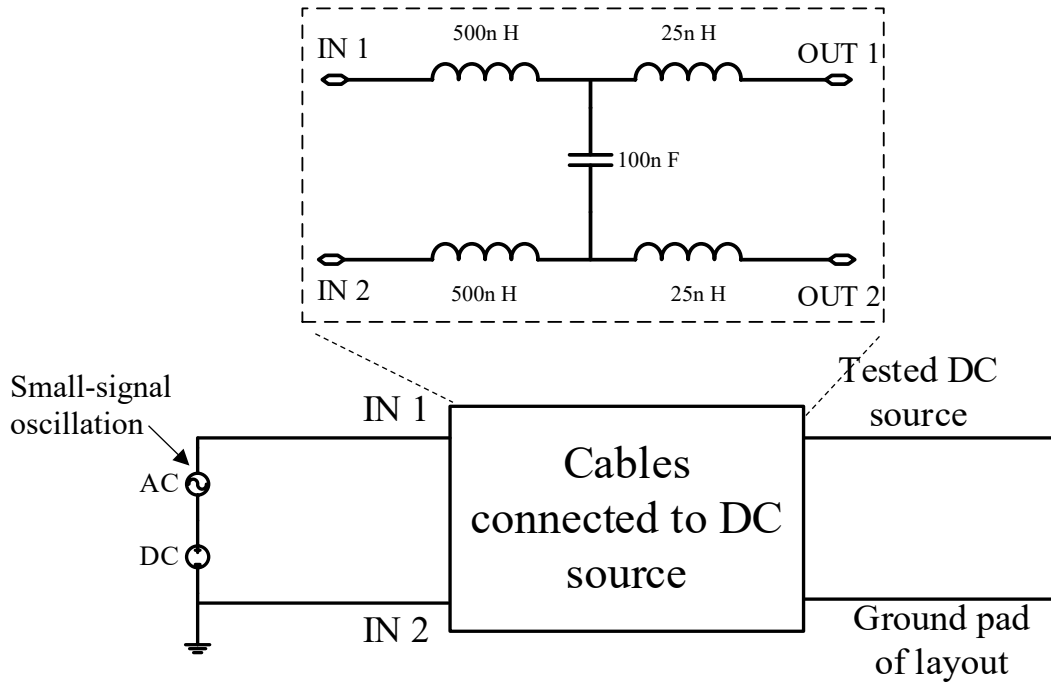


Figure B-7. Simulation test bench of DC generator including lumped equivalent elements

The simulation results are shown in Figure B-8 for the driver cell and the power cells. The transfer function H is calculated between the input and the output of DC generator block to extract the impact on the stability of the circuit. It is important to note that the positive peak of the transfer function, which indicates the possible oscillation frequency in the circuit, must be inferior to the operating frequency of the circuit.

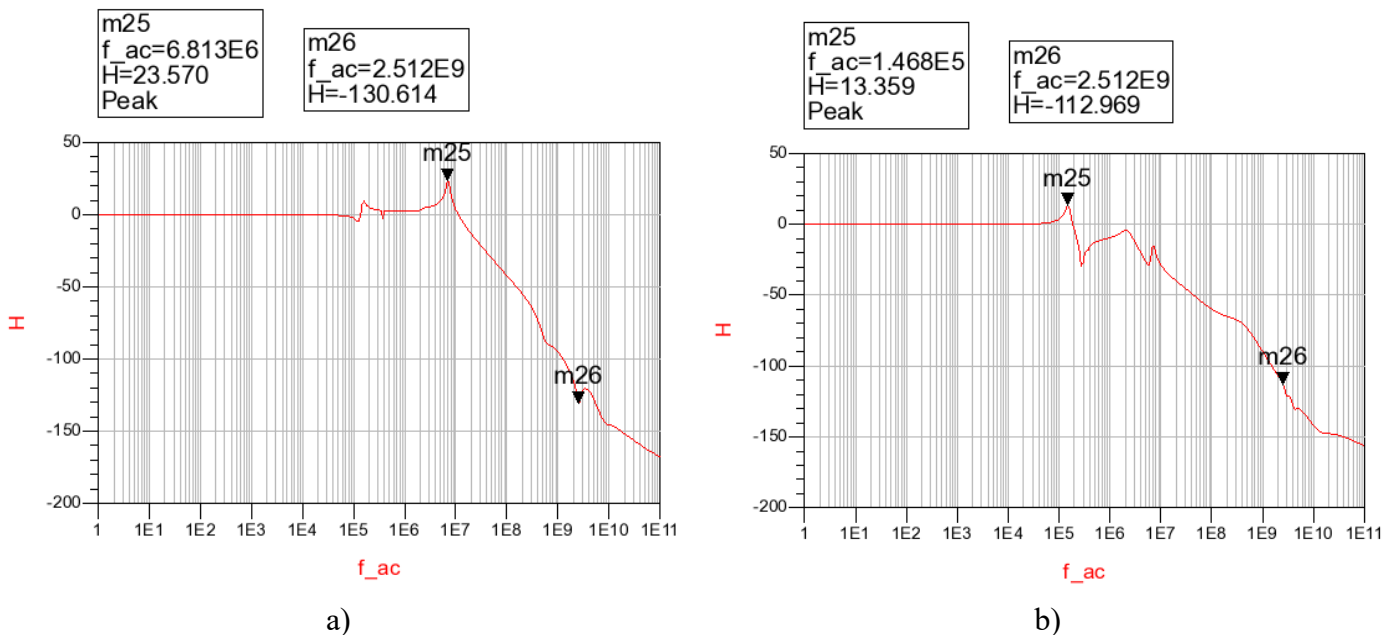


Figure B-8. Simulation results for DC supply sources of (a) power cells and (b) driver cell

B.4 Process corner

A process corner refers to a variation of fabrication parameters applied to an integrated circuit design. Process corners represent the extremes of these parameter variations within a

circuit [64]. A circuit may run slower or faster than specified and at lower or high temperatures and voltages. All variations are indicated in a process corner. The circuit is required being tested under every single process corner to ensure its correct function. There are two types of process corners: front end of line (FEOL) and back end of line (BEOL). The former relates the N-channel MOS and the P-channel corners. This type of corner mainly affects the performance of circuits by slowing down or boosting up the transport of electron inside transistors. Three corners exist: typical, fast and slow. Fast and slow corners exhibit carrier motilities that can be higher or lower than average, respectively. The latter relates to voltage and temperature (PVT) variation effects on on-chip interconnection and via structures. As mainly influenced by FEOL corners, it is essential to simulate the performance of ICs under every single corner before sending the circuit to the foundry. Figure B-9 illustrates the simulation results of the reconfigurable PA under four process corners.

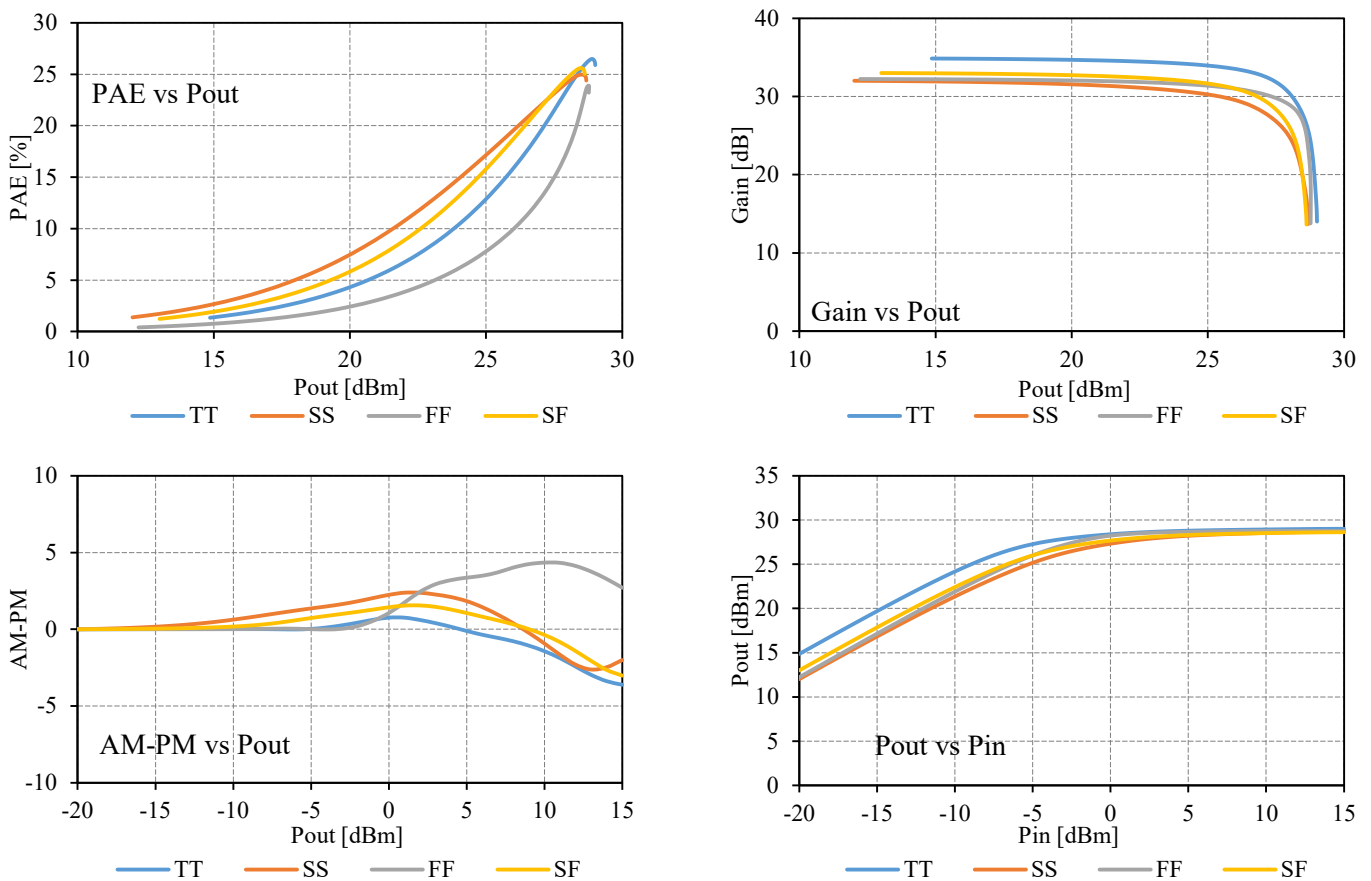


Figure B-9. RF performances of the PA under four process corners: TT (typical-typical), SS (slow-slow), FF (fast-fast) and SF (slow-fast)