



# Development of edge-emitting Si/SiGe based optical sources operating in the visible and near visible range wavelength for sensing and communication applications

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## **Development of edge-emitting Si/SiGe based optical sources operating in the visible and near visible range wavelength for sensing and communication applications**

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# ABSTRACT

We propose a low cost full-silicon optical links utilizing 650 – 850 nm propagation wavelengths. The creation of large-scale opto-electronic integrated circuits and optical data “highways” in CMOS integrated circuitry, utilizing Si CMOS compounds, have been envisioned and hold much promise [1] - [3] The latest attempts for realizing optoelectronic systems in CMOS technology have until now mainly been focused on utilizing wavelengths at 1550 nm [4] - [6], mainly because of the ease of design and fabrication of waveguides in this wavelength regime.

However, no effective high-speed optical sources and Si detectors are available at this 1550nm wavelength. Today solutions to overcome the problem are mostly focused on the integration of group III-V elements based optical sources on Silicon through molecular bonding [7a] – [7b]. If optical sources, detectors, waveguides, and sensors could be realized on the same Si CMOS chip at, say, 750 nm wavelength, various low power consuming, light and miniature on-chip-based micro-phonic systems could be designed and realized. While Silicon optical sources may not yet be at the required performance level for very-high speed communications, the low cost “all-silicon” opto-electronic systems still remain a great grail. These sources could lead to new field that could be appropriately named “Si photonic microsystems” opening the route to on-chip optical interconnect, new sensing applications and products especially for the medical, biomedical optics, optical interconnect and bio-photonics field. These systems also do not require ultrahigh frequency bandwidths to transmit, and the emission powers of our avalanche Si light-emitting diodes (LEDs) may be sufficient to sustain the operation of such systems.

This PhD thus deals with low cost SiGe/Si optical links using Microwave-Photonics devices such as, Bipolar integrated SiAvLED, Silicon Nitride and Silicon Oxide optical waveguides, SiGe HPTs, Si and SiGe/Si LEDs. It focuses on the development of edge emitting Si Av LED and Si/SiGe LED with the intention to combine and integration of micron-scale optical sources, optical waveguides and SiGe HPT detectors on the same chip to form a complete communication link for various applications involving short wavelength links (750nm to 950nm).

The progress provided by this PhD to previous works could be synthesized as below:

- Development of edge-emitting Si/SiGe based optical sources operating in the visible and near visible range wavelength
- Design and development of silicon nitride based optical waveguides operation in the visible range wavelength

- The integration of Si/SiGe Optical source, silicon nitride based waveguide and the Si/SiGe HPT based detector were all integrated and aligned on the same silicon chip, in an industrial based technology, to form complete on-chip micro-optical links at 750nm wavelength, with a SiGe radio frequency (RF) 0.35 $\mu$ m bipolar process.
- The optical source and waveguide alignment, through localising the LED emitting region leading to full links structures
- Full silicon optical links designed: The experimental validation and characterisation of the link structures both in DC bias analysis and RF analysis
- Waveguide functionality realized using R-Soft simulation software suit. Good height alignment while using un-intended available layers, leading to optical coupling from the source through the designed optical waveguide to the detector.
- A series of second generation of on-chip optical communication links of 50 $\mu$ m length, utilizing 650 – 850 nm propagation wavelengths, have been designed and realized in SiGe bi-polar technology process. Micron dimensioned optical sources, waveguides and detectors were all integrated on the same chip to form a complete communication on-chip micro-optical links. Avalanche based Si LEDs (Si Av LEDs), Schottky contacting Si Av LED and Si/SiGe LED, TEOS densification strategies, Silicon-Nitride based waveguides, and state of the art SiGe bipolar detector technologies were used as key design strategies.
- R-soft simulation software (Beam Prop) was used as a mathematical capable simulation tool to model various Silicon-Nitride optical waveguide structures, before the designing, the fabrication, characterisation and testing of the device. Various device structures were modeled, simulation iterations were performed on several optical waveguide designed structures before the device design, and the devices were tested experimentally.
- ADS simulation was used to simulate the two-port equivalent circuit network of the device links for the analysis of RF parasitic capacitance, as a result of substrate and oxide RF coupling (high and low pass kind of filters)
- The fabrication of edge emission Si/SiGe LEDs. It has been fabricated using the 80 GHz SiGe2RF Telefunken GmbH SiGe Bipolar technological processes, which is crucial to be implemented for ultra-low-cost silicon, based IMWP systems. One key aspect of this research is to implement a Si Av LEDs in such a commercial technology without the addition of masks and processing steps. We modify the design layout geometries for different bias configurations in order to obtain different efficient emission point in the source structure. This approach ensures a straight compatibility with SiGe circuits on the same chip, and makes the Si and SiGe Avalanche LEDs directly integrated into an

industrial foundry. The Telefunken SiGe2-RF Bipolar Silicon Germanium process technology exhibits  $f_T$  up to 80GHz and  $f_{max}$  up to 90GHz. This makes this technology able to provide circuits working above 10GHz and potentially up to 60 GHz in some configurations. This RF bipolar technology allows the production of wafers with applications in high-speed cellular, devices used in high performance standard RF in various applications. As in the SiGe1RF technology of Telefunken used to create the LEDs sources and the SiGe detector, the Germanium content is high with values in the range of 20-25% and might be almost vertical pillars column block structure with the base. This process is a 0.8 $\mu$ m lithography double polysilicon heterojunction bipolar technology. The minimum emitter size on the layout is of 0.8x1.4 $\mu$ m<sup>2</sup> for vertical NPN HBT transistors, which provides actual size after processing of 0.5x1.1 $\mu$ m<sup>2</sup> due to lateral spacers. This technology leads to two LEDs types: one with a selectively implanted collector (SIC) NPN LEDs and the other one without. The difference between them is the additional mask required by the SIC-transistor, influencing the high frequency performances and static characteristics. This option allows transition frequency ( $f_T$ ) to reach the 80GHz value for SIC transistors, against only 50GHz for non-SIC transistor, with  $f_{max}$  of up to 90GHz in both cases. This process technology also offers PNP transistors, diodes (PN, Zener, ESD, Varactor and Schottky) and passive devices such as inductors capacitors and resistors. In the frame of our relation with Telefunken, a Non-Disclosure Agreement (NDA) has been signed and no information about the detailed process cross-section can be given.

- The fabrication of Edge emitting LED topologies: The descriptions of the optical source LEDs structures, three different optical source structures were designed utilizing the 0.35micron RF bipolar technology, each with different configuration source structures, different waveguide structures, but with the same basic SiGe detector structure in the optical links. The optical source was designed with an n+-n p+ columnar structure located laterally on the P-type silicon substrate of very high resistivity. The regions between the elevated source and detector structures were filled with plasma deposited oxide. The columnar structures were all of micron dimension, such that the structures were composed of 1 $\mu$ m cube substructures. The regions were doped accordingly as made available by the process. The regions were appropriately electrically contacted during experimental measurements on the fabricated device on the wafer in order to reverse bias the first p+ n junction. Upon reverse biasing, the depletion region penetrates through to the n+ region in order to strengthen and unify the electric field in the lowly doped n region. The light emission would occur near the surface region of the middle n region and extend more or

less laterally across the whole region. The region between the Si Av LED source and SiGe detector were filled with normal TEOS plasma deposited oxide as part of the available process procedure. The middle layer was subsequently interfaced laterally to the optical light emission region, and the waveguide implemented here was (OWGD1). Appropriate air slots were made on the sides of the waveguide in order to minimise laterally induced oxide parasitic capacitance.

- In the second test structure of the LEDs source was designed in the same basic lateral columnar structure for the optical source as in the first design, but strategic design of a rectangular Schottky configuration contact of Aluminum on n-Silicon is fabricated in the columnar structure middle lowly doped n region on the optical source. The two p+ columnar regions were grounded as required by the RF probe bias during measurement process, and the DC and modulation RF signal was applied on the Schottky contact. Positive voltage bias placed the Schottky contact in forward bias mode and caused a triangular depletion region towards the p+ region of the LED optical source, thereby reverse biasing the p+ n region. This configuration drastically reduces the total depletion region volume and hence reduces depletion layer capacitance. The elongated and uniform electric field region and its associated minimized capacitance would hence enable ultra-high modulation frequencies. Since small dimensions in  $\mu\text{m}$  were used and the light emission processes are impact ionization and avalanche related aid.
- In a third design, a vertical cubical columnar HPT structure was designed to function as an optical source. The emitter-base n+ (SiGe) which contained 20% of Germanium was placed in reverse bias and in the avalanche regime. The emitter/base terminals were shorted in order to initially simplify the operation of the optical source device to function as an optical emission source, and bias is placed on the bottom contact of collector region. Because of layout and process design and processing limitations, the emitter n+ region is grounded. The SiGe detector structure of this nature has a transition frequency of up to 80GHz, it was assumed that when it was utilized as optical source by reverse biasing base-collector junction in avalanche reverse bias mode, the structure could attain similar operational frequency with optical emissions following this modulation frequency.
- On the same third design configuration, the optical source was operated in a forward bias configuration during experimental measurements, such that emitter n+ p (SiGe) junction is in forward bias mode. In this configuration, the emitter n+ p (SiGe) region is grounded and negative voltage bias of 2V is applied to the p+ SiGe base region. Electrons were injected from the n collector region and the carriers were energized through conduction transfer

through the low doped n region of the collector. When these carriers are injected in the SiGe base region, they would contain enough energy in order to then transfer electrons from the L valley to the T band structure valley of SiGe. With 20% Germanium doping, the emitted wavelength for this design is expected to be below 1000nm emission wavelength. The very small columnar conduction regions, used in the optical sources in this configuration, would reduce depletion layer capacitance and the subsequent carrier's transit time in the device.

- The work of this PhD is supported by substantial progress that has been made in the field of Si p-n junctions emitting visible light diode when operated in reverse breakdown avalanche mode [15] - [21]. Recently, Si CMOS light emitting sources appeared with much higher efficiencies by implementing two and three junctions Si CMOS injection avalanche LEDs that emit in the spectrum range of 450 to 750 nm [22] - [23]. They can be integrated with ease in standard CMOS circuits. Various prototypes have been realized. Their operating voltage (8V), and current (80  $\mu$ A to 1 mA) are low. They emit from an area of  $1 \times 1 \mu\text{m}^2$  between 10 and 100 nW. The internal light emission levels are much higher by a factor of 0.3. Particularly promising technology, which uses defect and surface-assisted transitions in these types of LEDs, has recently been identified and developed by our group [24] - [26]. Our Si avalanche-based LEDs operate optimally at 650 to 850 nm, and although the optical emission power of Si avalanche- LEDs is still low, about 90nW, they can reach modulation speeds into the GHz range. Since Si LEDs and Si detectors are both available, and can be integrated with relative ease into the proposed SiGe/Si technology, the most challenging part of following this route to realize on-chip micro optical link at 750nm with silicon is, hence, to develop appropriate optical waveguide technology in this 450-850nm wavelength regime that can be integrated into Si CMOS integrated circuitry.
- In this context, the important objectives of this study concern the development of edge emitting Si Av LED & Si/SiGe LED and the understanding of physical integration of Si LEDs and SiGe LEDs, optical waveguide. In addition, to be Bi/CMOS compatible optical detector and the proposal of integrating all on the same silicon chip to form a complete on-chip optical links at 750nm for optical intra/interconnect and the characterization of the design on-chip optical links.
- Developing full Silicon on-chip optical links in the near visible at 450nm-850nm. Exploring industrial SiGe/Si foundries Compatibility with further circuit integration (bipolar, BiCMOS), with high speed capabilities Low cost technology. Source and

waveguide alignment compatibility. Finally, on-chip microwave photonics links have been fabricated and characterized using a SiGe Bipolar technology process.

- The purpose of this research was, then, (1), to design, develop edge emitting Si Av LED, Si/SiGe LED design optical waveguides, detailed simulations of the viability of the waveguides for realization of micro-photonic structures in 1.2 $\mu$ m and 0.35 $\mu$ m for optical link in SiGe/Si integrated circuitry at mainly 750nm operating wavelengths were conducted; (2) to demonstrate the possible performance of the design waveguides at 750nm; (3) to demonstrate and realize second iteration optical link in SiGe/Si integrated circuitry at 750 nm experimentally; and (4) The design, fabrication and characterization of the first on-chip microwave photonic links at near-visible wavelength (0.65-0.85 $\mu$ m). All those structures are fabricated into an 80 GHz Telefunken GmbH SiGe/Si HBT technological processes. The full optical link combines Silicon, SiGe based Avalanche Light Emitting Devices (Si Av LEDs), Silicon-Nitride based, and silicon oxide (TEOS) based waveguides, and SiGe Heterojunction Bipolar Photo-Transistors (HPT). Such device could permit hosting microfluidic systems, on chip data communication and bio-chemical analysis applications and to propose potential applications for some first iteration Bipolar or CMOS based micro-photonic systems and micro-opto- electro-mechanical systems (MOEMS) and (MEMS).
- Best performances of the designed on-chip optical links show a conversion loss as low as 30dB from source to detector with up to 500MHz in cut off frequency. The good alignment and the good efficiency of each device are then clearly achieved. Higher frequency performances are also envisaged from preliminary measurements.
- Compared to international contributions, the work has been accepted for publication in the proceedings of three international conferences. From this work, three journals articles were published in a state-of-the-art ISI accredited scientific journals (JM3-SPIE) and (IEEE JQE) in the USA. A further article is currently submitted to IEEE Journal of Material Engineering (JME). One patent was granted on this work in Korea, after extensive provisional and International Protocol Collaboration Treaty (PCT) patenting.



# RÉSUMÉ

Résumé en français :

Nous proposons une étude des liaisons optiques en technologie intégralement silicium à faible coût pour des longueurs d'onde de transmission définies dans la plage 650 à 850 nm.

La création de circuits intégrés optoélectroniques à grande échelle et de voies de données optiques dans les circuits intégrés CMOS, utilisant des composants CMOS, a été envisagée et semble prometteuse [1] - [3]. Les derniers efforts pour réaliser des systèmes optoélectroniques en CMOS ont focalisé sur l'utilisation des longueurs d'onde à 1550 nm [4] - [6], principalement en raison de la facilité de conception et de fabrication de guides d'ondes dans cette gamme de longueurs d'onde.

Cependant, aucune source optique efficace à grande vitesse et aucun détecteur en Silicium ne sont disponibles à cette longueur d'onde de 1550 nm. Aujourd'hui, les solutions pour surmonter le problème sont principalement axées sur l'intégration de sources optiques basées sur des éléments réalisés en semi-conducteur III-V, sur le silicium par liaison moléculaire [7a] - [7b]. Si des sources optiques, des détecteurs, des guides d'ondes et des capteurs pouvaient être réalisés sur la même puce Si CMOS à une longueur d'onde de 750 nm, divers systèmes micro-photoniques légers et miniaturisés basés sur puce pourraient alors être conçus et réalisés. Tandis que les sources optiques au silicium ne sont peut-être pas encore au niveau des performances requises pour les communications à très haut débit, les systèmes optoélectroniques "tout-silicium" à faible coût restent malgré tout un excellent point de départ d'étude. Ces sources pourraient déboucher sur un nouveau domaine qui pourrait s'appeler «microsystèmes photoniques Si» ouvrant la voie à l'interconnexion optique sur puce, nouvelles applications et produits de détection notamment pour l'optique médicale, biomédicale, optique et bio-photonique. Ces systèmes ne nécessitent pas non plus de bande passante à très haute fréquences pour émettre, et les puissances d'émission de nos diodes électroluminescentes (DEL) à avalanche peuvent être suffisantes pour assurer le fonctionnement de tels systèmes.

Ce doctorat traite donc des liaisons optiques SiGe/Si à faible coût en utilisant des dispositifs photoniques-microondes tels que les DEL à avalanche en silicium intégrées **bipolaires**, les guides d'ondes optiques en Nitrure de silicium et Oxyde de silicium, les phototransistors à hétérojonction SiGe, et les DELs en Si et SiGe/Si. Nous nous sommes concentrés sur le développement de DELs à avalanche en Silicium, et DEL Si / SiGe à émission par la tranche avec l'intention de combiner et d'intégrer des sources optiques de taille micrométriques, des guides d'ondes optiques et des

détecteurs phototransistor à hétérojonction en SiGe sur la même puce pour former une liaison de communication complète pour diverses applications impliquant des liaisons à courtes longueurs d'onde de l'ordre de 750 nm à 950 nm.

La valeur ajoutée apportée par les travaux issus de ce doctorat par rapport aux travaux antérieurs fournis par l'équipe peut être synthétisée comme suit:

- Développement de sources optiques en Si/SiGe à émission par la tranche et fonctionnant dans la gamme de longueur d'ondes du visible et du proche visible.
- Conception et développement d'un guide d'ondes optique à base de nitrure de silicium opérant dans la gamme d'ondes visible.
- L'intégration de source optique Si/SiGe, d'un guide d'ondes à base de nitrure de silicium et d'un détecteur de type phototransistor Si/SiGe ont été intégrées et alignées sur la même puce de silicium, dans une technologie industrielle, pour former une liaison photonique-microondes complète sur puce à la longueur d'onde de 750nm, en utilisant la technologie bipolaire SiGe 0.35  $\mu\text{m}$  pour les fréquences microondes.
- L'alignement de la source optique et du guide d'ondes, grâce à la localisation de la région émettrice de DEL conduit à des structures d'une liaison complète.
- La conception de liaisons optiques tout silicium: la validation expérimentale par la caractérisation des structures des liaisons en analyse DC continue et analyse dynamique RF.
- La réalisation de la fonctionnalité de guide d'ondes à l'aide du logiciel de simulation R-Soft. Un bon alignement de la hauteur, tout en utilisant des couches disponibles non prévues, ont conduit à un bon couplage optique de la source à travers le guide d'onde optique conçu initialement pour le détecteur.
- Une série de liaisons de communication optique sur puce de deuxième génération d'une longueur de 50  $\mu\text{m}$ , utilisant des longueurs d'onde de propagation de 650 à 850 nm, a été conçue et réalisée en technologie bipolaire SiGe. Des sources optiques, des guides d'ondes et des détecteurs de dimensions micrométriques ont tous été intégrés sur la même puce pour former une communication complète sur les liaisons **micro-optique**. Les DELs à avalanche en Silicium (Si Av), une DEL à avalanche en Silicium à contact Schottky et des DELs Si/SiGe, les stratégies de densification TEOS, des guides d'ondes à base de nitrure de silicium et les détecteurs en technologie bipolaire SiGe ont été utilisés comme stratégies de conception clés.

Le logiciel de simulation R-soft (Beam Prop) a été utilisé comme outil de simulation mathématique pour modéliser différentes structures de guides d'ondes optiques nitrure de silicium, et a été une aide à la conception, et ce avant la fabrication, la caractérisation et le test du dispositif. Différentes structures de dispositifs ont été modélisées, des itérations de simulation ont été réalisées sur plusieurs structures de guides d'ondes optiques avant la réalisation du dispositif, et les dispositifs ont été testés expérimentalement.

- La simulation ADS a été utilisée pour simuler le réseau de circuits équivalents à deux ports des connexions des dispositifs et plus particulièrement pour l'analyse de la capacité parasite RF dû au couplage RF du substrat et de l'oxyde (filtres passe-haut et passe-bas).
- La fabrication de DEL Si / SiGe à émission par la tranche a utilisé les processus technologiques SiGe2RF Telefunken GmbH SiGe Bipolar à 80 GHz, ce qui est crucial pour les systèmes photoniques microondes intégrés à base de silicium à très bas coût. Un aspect clé de cette recherche est de mettre en œuvre une DEL à avalanche en Silicium dans une telle technologie industrielle sans l'ajout de masques et d'étapes de traitement. Nous avons donc seulement modifié les géométries de disposition de conception pour différentes configurations de polarisation afin d'obtenir différents points d'émission optique efficaces hors de la structure de la source optique. Cette approche assure une compatibilité directe avec les circuits SiGe sur la même puce, et fait que les DEL Si et Avalanche SiGe sont directement intégrées dans une fonderie industrielle. La technologie de procédé industrielle Germanium Bipolaire Silicium/Germanium de Telefunken présente des  $f_T$  allant jusqu'à 80GHz et  $f_{max}$  jusqu'à 90GHz. Cela rend cette technologie capable de fournir des circuits fonctionnant au-dessus de 10 GHz et potentiellement jusqu'à 60 GHz dans certaines configurations. Cette technologie bipolaire RF est utilisée pour les applications dans les réseaux cellulaires à haut débit, dans les dispositifs hautes performances standards. Comme dans la technologie **SiGe<sup>1</sup>RF** de Telefunken utilisée pour créer les sources de DEL et le détecteur SiGe, la teneur en germanium est élevée avec des valeurs de l'ordre de 20-25% et pourrait être une structure de colonne quasi verticale vis-à-vis de la base. Ce procédé est une technologie bipolaire à hétérojonction à double polysilicium de 0,8  $\mu m$  de lithographie. La taille minimale de l'émetteur sur le réseau est de 0,8x1,4 $\mu m^2$  pour les transistors HBN NPT verticaux, ce qui donne une taille réelle après le traitement de 0,5x1,1 $\mu m^2$  en raison des espacements latéraux nécessaires. Cette technologie conduit à deux types de DEL : l'un avec des DELs NPN à collecteur sélectivement implanté (SIC) et l'autre sans. La différence entre eux est le masque supplémentaire requis par le transistor SIC, influençant les performances à hautes fréquences et les caractéristiques statiques. Cette option permet à la fréquence de transition ( $f_T$ ) d'atteindre la valeur de 80GHz

pour les transistors SIC, contre seulement 50GHz pour les transistors non-SIC, avec un  $f_{\max}$  allant jusqu'à 90GHz dans les deux cas. Cette technologie de processus offre également des transistors PNP, des diodes (PN, Zener, ESD, Varactor et Schottky) et des dispositifs passifs tels que des condensateurs inductances et des résistances. Dans le cadre de notre relation avec Telefunken, un accord de non-divulgateur (NDA) a été signé et aucune information sur la section transversale détaillée du processus ne peut être donnée dans ce manuscrit.

- Une étude a été menée sur la fabrication de différentes topologies de DEL à émission par la tranche : Les descriptions de trois structures de sources optiques DEL différentes ont été conçues en utilisant la technologie bipolaire RF 0,35  $\mu\text{m}$ , chacune avec différentes structures de configuration de source, différentes structures de guides d'ondes, mais avec la même structure de base du détecteur SiGe. La source optique a été conçue avec une structure de type colonne  $n^+ - np^+$  située latéralement sur le substrat de silicium de type P de très haute résistivité. Les régions entre les structures de source positionnée en hauteur et de détecteur ont été remplies d'oxyde déposé par plasma. Les structures de type colonne étaient toutes de dimension de l'ordre du micromètre, de sorte que les structures étaient composées de sous-structures cubiques de 1  $\mu\text{m}$ . Les régions ont été dopées comme le procédé technologique le permettait. Les régions ont été polarisées électriquement de manière appropriée au cours de mesures expérimentales sur le dispositif fabriqué sur la plaquette afin de polariser en sens inverse la première jonction  $p^+ - n$ . Lors d'une polarisation inverse, la région d'appauvrissement pénètre alors dans la région  $n^+$  afin de renforcer et d'unifier le champ électrique dans la région  $n$  faiblement dopée. L'émission de lumière se produit près de la région de surface de la région du milieu  $n$  et s'étend plus ou moins latéralement dans toute la région. La région entre la source de la DEL à avalanche en Silicium et le détecteur SiGe a été remplie d'oxyde déposé par plasma TEOS normal dans le cadre de la procédure de traitement disponible. La couche intermédiaire a ensuite été interfacée latéralement à la région d'émission de lumière optique, et le guide d'ondes mis en œuvre ici était celui nommé OWGD1. Des fentes d'air appropriées ont été réalisées sur les côtés du guide d'ondes afin de minimiser la capacité parasite d'oxyde induite latéralement.
- Dans la seconde structure de test de la source DEL, celle-ci a été conçue dans la même structure de type **colonne latérale** basique que pour la source optique de la première conception, mais la conception stratégique d'une configuration rectangulaire Schottky d'Aluminium sur  $n$ -Silicium est fabriquée dans la structure de type colonne peu dopée au milieu de la région  $n$  de la source

optique. Les deux régions  $p^+$  de type colonne ont été polarisées à la masse comme c'est nécessaire pendant le processus de mesure à l'aide d'une pointe RF. Le signal DC et le signal RF de modulation ont été appliqués aux contacts Schottky. La polarisation par une tension positive du contact de Schottky induit un mode de polarisation directe et provoque une région d'appauvrissement triangulaire vers la région  $p^+$  de la source optique de DEL, polarisant ainsi en inverse la région  $p^+n$ . Cette configuration réduit considérablement le volume total de la zone de déplétion et réduit ainsi la capacité de la couche de déplétion. La région de champ électrique allongée et uniforme et la minimisation de sa capacité associée doit permettre des fréquences de modulation ultra-élevées. Depuis, de petites dimensions micrométriques ont été utilisées et les processus d'émission de lumière sont l'ionisation par impact et le phénomène d'avalanches.

- Dans une troisième conception, une structure de phototransistor à hétérojonction verticale cylindrique a été conçue pour fonctionner comme une source optique. L'émetteur-base  $n^+$  (SiGe) qui contient 20% de Germanium a été placé en polarisation inverse et dans le régime d'avalanche. Les bornes d'émetteur/base ont été court-circuitées afin de simplifier initialement le fonctionnement du dispositif source optique pour fonctionner en tant que source d'émission optique, et une polarisation est placée sur le contact inférieur de la région de collecteur. En raison de la conception et du procédé et des limitations de traitement, la région de l'émetteur  $n^+$  est mise à la masse. La structure de détecteur SiGe de cette nature a une fréquence de transition allant jusqu'à 80GHz, on a supposé que lorsqu'elle était utilisée comme source optique par polarisation inverse de la jonction base collecteur, soit en mode de polarisation inverse, la structure peut atteindre en condition émission optique, une fréquence de modulation opérationnelle du même ordre de grandeur.
- Sur cette même troisième configuration de conception, la source optique a été utilisée dans une configuration de polarisation directe pendant les mesures expérimentales, de sorte que la jonction de l'émetteur  $n^+p$  (SiGe) est en mode de polarisation directe. Dans cette configuration, la région de l'émetteur  $n^+p$  (SiGe) est mise à la masse et une polarisation de tension négative de 2V est appliquée à la région de la base  $p^+$  en SiGe. Des électrons ont été injectés à partir de la région du collecteur  $n$  et les porteurs ont été excités par **transfert de conduction** à travers la région  $n$  faiblement dopée du collecteur. Lorsque ces transporteurs sont injectés dans la région de la base en SiGe, ils contiennent suffisamment d'énergie pour ensuite transférer les électrons de la vallée L à la vallée de la structure en bande T de SiGe. Avec 20% de dopage du germanium, la longueur d'onde émise pour cette conception devrait être inférieure à la longueur

d'onde d'émission de 1000 nm. Les très petites régions de conduction en colonnes, utilisées dans les sources optiques dans cette configuration, permettent de réduire la capacité de la couche d'appauvrissement et le temps de transit de la porteuse dans le dispositif.

- Le travail de cette thèse a été possible grâce aux progrès substantiels qui ont été réalisés dans le domaine des diodes à émission de lumière visible par des jonctions Si p-n fonctionnant en mode avalanche dès lors qu'elles sont polarisées en inverse au-delà de la tension d'avalanche [15] - [21]. Récemment, les sources lumineuses Si CMOS sont apparues avec des rendements beaucoup plus élevés en mettant en œuvre des DEL à avalanche à deux et trois jonctions Si CMOS qui émettent dans la gamme spectrale de 450 à 750 nm [22] - [23]. Un fort intérêt est qu'elles peuvent être intégrées facilement dans les circuits CMOS standards. Divers prototypes ont été réalisés. Leur tension de fonctionnement (8V) et leur courant (80 $\mu$ A à 1mA) sont faibles. Ils émettent sur une surface de  $1 \times 1 \mu\text{m}^2$  entre 10 et 100 nW. Les niveaux d'émission de lumière interne sont augmentés d'un facteur de 0,3. Une technologie particulièrement prometteuse, qui utilise des défauts et des transitions assistées par la surface dans ces types de DEL, a récemment été identifiée et développée par notre groupe [24] - [26]. Nos DEL à base de phénomène à avalanche en Silicium fonctionnent de manière optimale entre 650 et 850 nm, et bien que la puissance d'émission optique des diodes à avalanche Si soit encore faible, environ 90 nW, elles peuvent atteindre des vitesses de modulation dans la gamme des GHz. Puisque les détecteurs Si et Si sont tous les deux disponibles et peuvent être intégrés relativement facilement dans la technologie SiGe/Si proposée, l'aspect le plus difficile pour suivre cette voie pour réaliser une liaison micro-optique sur puce à 750 nm avec du silicium est donc de développer une technologie de guide d'ondes optique appropriée dans ce régime de longueur d'onde de 450 à 850 nm qui peut être intégré dans les circuits intégrés Si CMOS.
- Dans ce contexte, les objectifs importants de cette étude concernent le développement de la DEL en Si à avalanche et la DEL en Si/SiGe à émission par la tranche et la compréhension de l'intégration physique des DEL Si et DEL SiGe avec les guide d'ondes optiques. En outre, un point crucial est d'être un détecteur optique compatible Bi/CMOS et de permettre l'intégration de tous ces éléments sur une même puce de silicium pour former une liaison optique sur puce complète à 750 nm pour l'intra/interconnexion optique et la caractérisation des liaisons optiques de conception sur puce.

- Une étude du développement de liaisons optiques complètes sur silicium dans le proche visible à 450 nm-850 nm est présentée grâce à l'exploration de fonderies industrielles SiGe/Si en s'assurant une compatibilité avec l'intégration de circuits supplémentaires (bipolaire, BiCMOS), avec des capacités à haute vitesse technologie à faible coût. Une compatibilité d'alignement des sources et guides d'ondes a été étudiée. Enfin, des liaisons photoniques micro-ondes sur puce ont été fabriquées et caractérisées en utilisant un procédé de technologie SiGe Bipolaire.
- Le but de ces travaux de recherche était donc (1) de concevoir, développer des diodes électroluminescentes Si à avalanche, des DELs Si/SiGe, mener des simulations sur la viabilité des guides d'ondes pour la réalisation de structures micro-photoniques en 1.2µm et 0,35 µm pour la liaison optique dans les circuits intégrés SiGe/Si à des longueurs d'onde de fonctionnement de 750nm principalement; (2) pour démontrer la performance possible des guides d'ondes de conception à 750 nm; (3) pour démontrer et réaliser une deuxième liaison optique d'itération dans un circuit intégré SiGe/Si à 750 nm expérimentalement; et (4) la conception, la fabrication et la caractérisation des premières liaisons photoniques hyperfréquences sur puce à une longueur d'onde quasi visible (0,65-0,85 µm). Toutes ces structures sont fabriquées dans un processus technologique 80 GHz de la fonderie Telefunken GmbH SiGe/Si HBT. La liaison optique complète associe des dispositifs d'émission de lumière par le phénomène à avalanche à base de SiGe (Si Av), à base de silicium-nitride et à base d'oxyde de silicium (TEOS), et des transistors photoélectriques bipolaires à hétérojonction (HPT). Un tel dispositif permettrait d'héberger des systèmes microfluidiques, des applications de communication de données sur puce et d'analyse biochimique et de proposer des applications potentielles pour certains systèmes micro-photoniques bipolaires ou à base de CMOS et des systèmes micro-optoélectromécaniques (MOEMS) et MEMS.
- Les meilleures performances des liaisons optiques intégrées sur puce indiquent une perte de conversion aussi faible que 30 dB de la source au détecteur avec une fréquence de coupure allant jusqu'à 500 MHz. Le bon alignement et la bonne efficacité de chaque appareil sont alors clairement atteints. Des performances plus élevées sont également envisagées à partir des mesures préliminaires.
- Par rapport aux contributions internationales, le travail a été accepté pour publication dans les actes de trois conférences internationales. De plus, trois articles de revues ont été publiés dans

des revues scientifiques à la pointe de la technologie accréditée par l'ISI (JM3-SPIE) et (IEEE JQE) aux États-Unis. Un autre article est actuellement soumis à l'IEEE Journal of Material Engineering (JME). Un brevet a été délivré pour ce travail en Corée, après de nombreux brevets délivrés provisoirement et en vertu du Traité de collaboration au Protocole international (PCT).



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## DEDICATION

This study is dedicated to: Almighty God for the strength and guidance He gave me; my mother Theresa Imeomonde Ogudo, my wife Beatrice E. Ogudo, my son Christian Ogudo, my brothers, my sister, my in-law Peter Akhimien, my uncle Godwin Idiovo (aka General) and my pastor WF Kumuyi for their love and prayers during my studies.

# LIST OF ABBREVIATIONS AND ACRONYMS

<b>2D</b>	Two dimensions
<b>3D</b>	Three dimensions
<b>APDs</b>	Avalanche photo detector
<b>CAD</b>	Computer aid design
<b>CMOS</b>	Complementary Metal Oxide Semi-conductor
<b>EPIC</b>	Electronic-photonic integrated circuit
<b>FDTD</b>	Finite-Difference Time-Domain
<b>FEOL</b>	Front end of line
<b>IMWP</b>	Integrated MicroWave Photonics
<b>LED</b>	Light Emitting Diode
<b>LOCOS</b>	Local oxidation of silicon
<b>MEMS</b>	Micro-electro-mechanical systems
<b>MOEMS</b>	Micro Opto-electro Mechanical Sensor
<b>OD3_L1</b>	Optical die 3 Layout 1
<b>OD3_L2</b>	Optical die 3 Layout 2
<b>OD3_L6</b>	Optical die 3 Layout 6
<b>OEIC</b>	Opto-electronic Integrated Circuit
<b>OLTS1</b>	Optical link test structure one
<b>OLTS2</b>	Optical link test Structure two
<b>OLTS3</b>	Optical link test Structure three
<b>PMI</b>	Physical Model Interface
<b>SLD</b>	Semi-conductor Laser Diode
<b>SOI</b>	Silicon-on-insulator
<b>TEOS</b>	Tetra-Ethyl-Ortho-Silicate
<b>TS1</b>	Test structure one
<b>TS2</b>	Test structure two
<b>TS3</b>	Test structure three
<b>UPML</b>	Uniaxial perfectly matched layer

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## GENERAL INTRODUCTION:

Currently, optical communications and opto-electronic integrated circuits are designed, developed and realized by utilizing group “III-V” semiconductors, such as gallium arsenide and associated compounds. They form the basis of a mature and quite complex technology. A deficiency is that these technologies cannot be integrated into silicon (Si) and mainstream complementary metal–oxide–semiconductor (CMOS) integrated circuit technology with ease. A series of viable Si light-emitting technologies have recently become available that enable the integration of light sources directly into Si CMOS or Bipolar technology e.g. [7]. The creation of large-scale opto-electronic integrated circuits and optical data “highways” in CMOS integrated circuitry, utilizing Si CMOS compounds, have been envisioned and hold much promise [8] - [11]. The latest attempts for realizing optoelectronic systems in CMOS technology have until now mainly been focused utilizing wavelengths at 1550 nm [12] - [14], mainly because of the ease of design and fabrication of waveguides in this wavelength regime, and compatibility to telecommunication bands.

However, neither effective high-speed Si optical sources, nor Si detectors, are available at this 1550nm wavelength. If optical sources, detectors, waveguides, and sensors could be realized on the same Si CMOS chip at, say, 750 nm wavelength, various on-chip-based micro-photonic systems can be design and realized. Achieving these goals can lead to diverse low cost “all-silicon” opto-electronic systems, which will be the “smarter” and more “intelligent” CMOS chips of the future. These systems could lead to a new field that could be appropriately named “*Si CMOS photonic microsystems*” and lead to new products especially for the medical, biomedical optics, optical interconnect and bio-photonics field. These systems also do not require ultrahigh frequency bandwidths to transmit, and the emission powers of our tailored designed avalanche Si light-emitting diodes (AvSiLEDs) may be sufficient to sustain the operation of such systems. The main objective of my research was, therefore, to design optical waveguides and Bi/CMOS compatible optically and directly integrate the sources, Silicon-Nitride waveguides, TEOS waveguide and the detectors all in the same silicon chip substrate for optical interconnect and communication sensors on chip at 750nm wavelength using SiGe/Si RF Bipolar processing platform. This would have benefits in terms of manufacturing cost reduction, miniaturization, the simplification of packaging requirements and perhaps also of low total power operation requirements for such a system.

The work of this PhD is supported by substantial progress that has been made in the field of Si p–n junctions emitting visible light diode when operated in reverse breakdown avalanche mode [15] - [21]. Recently, Si CMOS light emitting sources appeared with much higher efficiencies by implementing two and three junctions Si CMOS injection avalanche LEDs that emit in the spectrum range of 450 to 750 nm [22] - [23]. They can be integrated with ease in standard CMOS circuits. Various prototypes have been realized. Their operating voltage (8V), and current (80  $\mu$ A to 1 mA) are low. They emit from an area of  $1 \times 1 \mu\text{m}^2$  between

10 and 100 nW. The internal light emission levels are much higher by a factor of 0.3. Particularly promising technology, which uses defect and surface-assisted transitions in these types of LEDs, has recently been identified and developed by our group [24] - [26]. Our Si avalanche-based LEDs operate optimally at 650 to 850 nm, and although the optical emission power of Si avalanche- LEDs is still low, about 90nW, they can reach modulation speeds into the GHz range. Since Si LEDs and Si detectors are both available, and can be integrated with relative ease into the proposed SiGe/Si technology, the most challenging part of following this route to realize on-chip micro optical link at 750nm with silicon is, hence, to develop appropriate optical waveguide technology in this 450-850nm wavelength regime that can be integrated into Si CMOS integrated circuitry.

In this context, the important objectives of this study concern the development of edge emitting Si Av LED & Si/SiGe LED and the understanding of physical integration of Si LEDs and SiGe LEDs, optical waveguide. In addition, to be Bi/CMOS compatible optical detector and the proposal of integrating all on the same silicon chip to form a complete on-chip optical links at 750nm for optical intra/interconnect and the characterization of the design on-chip optical links.

Developing full Silicon on-chip optical links in the near visible at 450nm-850nm. Exploring industrial SiGe/Si foundries Compatibility with further circuit integration (bipolar, BiCMOS), with high speed capabilities Low cost technology. Source and waveguide alignment compatibility. Finally, on-chip microwave photonics links have been fabricated and characterized using a SiGe Bipolar technology process.

The purpose of this research was, then, (1), to design, develop edge emitting Si Av LED, Si/SiGe LED design optical waveguides, detailed simulations of the viability of the waveguides for realization of micro-photonic structures in 1.2 $\mu$ m and 0.35 $\mu$ m for optical link in SiGe/Si integrated circuitry at mainly 750nm operating wavelengths were conducted; (2) to demonstrate the possible performance of the design waveguides at 750nm; (3) to demonstrate and realize second iteration optical link in SiGe/Si integrated circuitry at 750 nm experimentally; and (4) The design, fabrication and characterization of the first on-chip microwave photonic links at near-visible wavelength (0.65-0.85 $\mu$ m). All those structures are fabricated into an 80 GHz Telefunken GmbH SiGe/Si HBT technological processes. The full optical link combines Silicon, SiGe based Avalanche Light Emitting Devices (Si Av LEDs), Silicon-Nitride based, and silicon oxide (TEOS) based waveguides, and SiGe Heterojunction Bipolar Photo-Transistors (HPT). Such device could permit hosting microfluidic systems, on chip data communication and bio-chemical analysis applications and to propose potential applications for some first iteration Bipolar or CMOS based micro-photonic systems and micro-opto- electro-mechanical systems (MOEMS) and (MEMS).

This PhD document is divided in six chapters. The following section gives a brief overview of how this thesis is presented:

### **Chapter 1: State of The Art**

*On-chip optical link considerations:* This chapter presents more background on the motivation that leads to the study of this on-chip optical link technologies. In this chapter, we investigated the optical properties of CMOS IC structure and design as potential structure layers; such as Silicon-Nitride and the oxides layers that can be use as optical waveguides. The research problem statement are highlighted and discussed; which leads to the comparison of different available optical sources, optical waveguides and the design and fabrications complexity with corresponding development cost factors associated with various propagation wavelength utilizing CMOS technology. Lastly, we present the state of the art, SiGe/Si HPT bipolar technology and their compatibility with CMOS technology, and the possible integration with Silicon-Nitride optical waveguide and SiAvLEDs as offer by bipolar technology process at 750nm to form on-chip optical link communication and other optical integrated system applications directly onto CMOS chip.

### **Chapter 2: SiGe LED Technology: Edge-emitting topologies**

This chapter focuses on SiGe LEDs, SiAvLEDs and SiGe edge-emitting LED design layout geometries for the different bias configurations of our three different designs. This chapter presents a brief description of the light emission mechanism in silicon and the energy bandgap scheme for the impact ionization process for an electron in a reverse biased pn silicon junction. The layout structure of the three Silicon-based LEDs designed from SiGe2RF Telefunken technology are presented in this chapter. The description of the Si/SiGe HPT detector layout structure and dimensions as implemented in the optical links is also presented in this chapter. Lastly, the proposed integration of the optical sources, the designed optical waveguides and the detector on the same chip to form a full RF-Bipolar on-chip optical links is highlighted. While bipolar, this SiGe technology is thought to be straightforward transposable to SiGe/Si BiCMOS technologies.

### **Chapter 3: On-chip optical waveguide design and links configurations**

*On-chip optical waveguide link design strategies:* This chapter presents the different optical waveguides design strategies, the theoretical competency about optical waveguides with respect to modes, loss, dispersion and effect of waveguide material characteristics on these parameters especially for Si<sub>3</sub>N<sub>4</sub> and SiON. Three different waveguide strategies are proposed. In addition to the waveguide characteristic, it will be important to select the best strategy to get them efficiently coupled from the edge to LED and photodetectors and to reduce the intrinsic height misalignments. The role of the substrate and parasitics coupling are also key issues to properly address. The two main sections are then considered:

- *R-Soft CAD software simulation of the designed waveguides (Isotropic/hemispherical source):* The simulation results with R-soft software of three proposed optical waveguides designed are presented.

Silicon oxide waveguides using TEOS layers, Silicon-Nitride ( $\text{Si}_3\text{N}_4$ ) waveguides with V-groove design and Silicon-Nitride waveguides with narrower nitride core are considered. Simulation results, the viability and validation of the designed waveguides are highlighted. This chapter also presents the design waveguide simulation results and the interpretations of the simulation results as obtained.

- *RF substrate coupling considerations*: This section presents a simple AC topology two port network circuit to model the RF parasitic coupling within the three complete on-chip optical link device structures. This modelling gives details on parasitic coupling through the substrate or the oxide, as well as to predict the approximate reference signal floor level of parasitic coupling for the three test structures designed.

#### **Chapter 4: Reverse biased Avalanche LED based optical links**

In this chapter, we discussed the reverse biased Silicon Avalanche LED device testing, the experimental measurements and characterisations of the different optical links configurations as designed.

- *Experimental realization and results for Optical link test structure 1 (OLTS1)*: In this section, reverse bias LED configurations as well as the DC bias analysis and characterization of the optical link test structure 1 (OLTS1) and the device OLTS1 DC&RF probing configurations are discussed in details. The RF power analysis and characterization of the on-chip optical link and the experimental confirmation of on-chip optical link with TEOS waveguide geometry operating at 750nm wavelength results are presented in this chapter.
- *Experimental realisation and results for Optical link test structure 2 (OLTS2)*: this section presents the DC bias analysis and characterizations of the optical link test structure OLTS2 are discussed and as well as the device OLTS2 DC&RF probing configurations. The RF power analysis and characterization of the on-chip optical link and the experimental confirmation of on-chip optical link with Silicon-Nitride waveguide V-groove geometry operating at 750nm wavelength results are presented in this chapter.
- *Experimental realisations and results for optical link test structure 3 (OLTS3-RB)*: In this section, the DC bias analysis and characterisation of the optical link test structure 3 (OLTS3) operated in reverse bias are discussed and as well as the device OLTS3 DC&RF probing configurations. The RF power analysis and characterization of the on-chip optical link and the experimental confirmation results as well as the characterization of the on-chip optical link and the experimental measurements of on-chip optical link, with Silicon-Nitride narrow core waveguide geometry operating at 750nm are presented in this chapter.



## **Chapter 5: Forward biased LED based optical links**

This chapter presents the DC bias analysis and characterisation of the optical link test structure of the forward bias configuration of OLTS3 (OLTS3-FB). The RF power analysis and characterisation of the on-chip optical link and the experimental confirmation results as well as the characterisation of the on-chip optical link and the AC experimental measurements of on-chip optical link, with Silicon-Nitride narrow core waveguide geometry been implemented and operating at 750nm are presented in this chapter. Lastly, a conclusive summary table indicating the main characteristics results of the three optical links test structures as designed are present in this chapter.

## **Chapter 6: Conclusion and perspectives.**

In this chapter, an overview of the designed, the developed and realized silicon on-chip optical links device is presented. The chapter presents the investigation and the results toward a full integration of an optical link on the same chip. Perspectives of the thesis and the recommendations for further research work in this area are then proposed.

# CHAPTER 1 State Of The Art

## 1.1 Introduction

This chapter reviewed the state-of-the-art in electrical and optical interconnects, to reach intra- and inter-chip interconnections at RF and millimetre waves, optical sources, photodetectors and modulators. From this investigation, in recent years, the shorter wavelength optical sources and low cost Si LEDs with a potential to be integrated into CMOS or bipolar based optical interconnect on a single chip.

The second section, hereafter, presents a brief description of the optical properties of CMOS integrated structures and their optical characteristics on the different structure layers. This section mainly focuses on the comparison of the available optical sources, the optical waveguides and the detectors technologies that are suitable for on-chip optical links interconnects

The third section introduces the spectral characteristics of the different optical sources, and comparison of their spectral detection range. This section also discussed the design and CMOS standard processing procedures of the Si Av LEDs optical source. In this section, light emission of the LEDs source device and LEDs along with their performance characteristics is presented.

The fourth section briefly presents the state-of-the-art of different types of optical detector. Different types of high-speed PDs for microwave photonics application such as p-i-n photodiodes (p-i-n PD), particularly Si p-i-n Reach Through Avalanche Photo Detectors (RAPDs) yielding up to 10 GHz of response at efficiency of up to 0.85A/W [102]. For radiation at 0.55 $\mu$ m, p-n configurations offer up to 0.6 A/W responsivity at around 1-30 GHz, while for p-i-n configurations offer up to 0.3 A/W will be discussed.

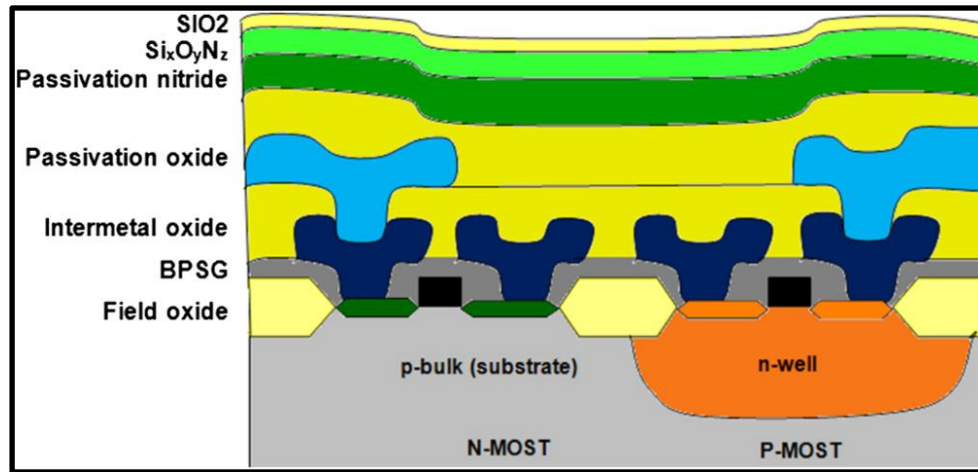
We give a brief analysis of SiGe Heterojunction phototransistors (HPTs), which are an efficient optical receivers fabricated on Si substrates The use of HPT structures provides optical conversion gain to further enhance the optical responsivity, thereby enabling efficient photo detection and responsivity in the short-wave and infrared region. It has an efficient photo detection covering the entirety of the fiber-optic telecommunication bands, as well as the emerging 2- $\mu$ m MIR communication band, can be achieved. HPTs are attractive for use as high-responsivity CMOS-compatible photodetectors in communication applications [120a].

This last section of this chapter will focus on the proposed combination of the optical source and the detector to form full Silicon on-chip optical links implementation of MWP systems and applications.

## 1.2 Optical Properties of CMOS Integrated Circuit Structures.

Figure 1 shows a typical CMOS integrated circuit structure using 1.2 $\mu$ m field oxide technology. Important feature is the transparency between 450 and 750 nm wavelengths [27] - [28] of some of the over-layers, such as the field oxide layer, the upper oxide layers, and the Silicon-Nitride passivation layer. Other

transparent layers such as Silicon-Oxi-Nitride and Silicon dioxide can be added as further over layers [29] - [31]. The optical transparency of the different layers varies slightly with wavelengths. Silicon-Nitride ( $\text{Si}_3\text{N}_4$ ) and Silicon-Oxi-Nitride ( $\text{SiON}$ ) are transparent for wavelengths longer than 600nm [32] - [34].



**Figure 1: CMOS integrated circuit structure**

The thickness, refractive index and optical absorption coefficients in a typical CMOS technology as shown in Figure 1 at 750nm are presented in Table 1. Technologies such as SiGe bipolar or BiCMOS 0.35 $\mu\text{m}$  and below are in principle similar, except that the Si field oxide layer is thinner (250 nm) and that active layers are grown above the substrate through epitaxy. A planarization process is used after transistor fabrication in order to accommodate a higher number of metal over-layers.

**Table 1: Optical Properties of CMOS ICs at 750 nm**

Component	Thickness ( $\mu\text{m}$ )	Refractive index	Absorption Length / transparency per wavelength	Natural State
Silicon substrate	500 $\mu\text{m}$	3.5	Transparent above 1100nm	Crystalline solid
Silicon field oxide	1 $\mu\text{m}$	1.45	Transparent above 400nm	Fused solid
Silicon plasma oxide	0.9 $\mu\text{m}$	1.48	0.4 - 0.2 for $\geq 400\text{nm}$	RF Deposited plasma
Silicon-Nitride	0.9 $\mu\text{m}$	Between 1.85-2.40	Transparent above 600nm	RF Deposited plasma
Air	- infinite	1.00	Transparent for 400 – 1500nm	Gas phase

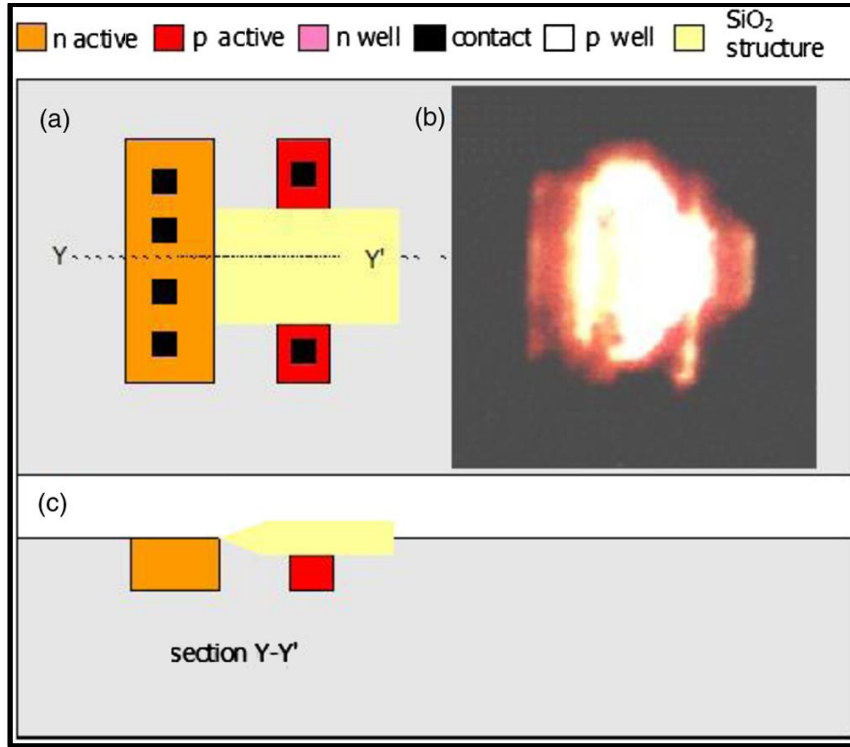
The absorption in oxide and nitride layers are substantially lower in Si, which has an absorption length in the range of 1  $\mu\text{m}$ . Furthermore, Si CMOS technology utilizes trench isolation technology that can be used for generating in-line opto couplers and waveguides to even below the Si substrate-over layer interface.

### 1.3 Si CMOS Avalanche LEDs

Si avalanche light-emitting devices in the 450nm to 650 nm wavelength regimes have been developed [5], [36] - [38]. The fabrication of these devices is high-temperature compatible and can be used in standard Si designs. CMOS-compatible avalanche Si LEDs (Si CMOS Av LEDs) have emerged since in the early 1990s. Kramer and Zeits were the first to propose the utilization of Si Av LEDs inside CMOS technology [19], also first to illustrate the potential of this technology. Snyman et al., have realized a series of Si Av light-emitting devices in standard CMOS technology, such as micro displays and electro-optical interfaces with higher emission efficiencies and higher emission radiances (intensities) [39] - [40], and particularly promising results have been obtained regarding the efficiency and the intensity, when a combination of current density confinement, surface layer engineering, and injection of additional carriers of opposite-charge density into the avalanching junction, was implemented [41]. The devices show three orders of increase in optical output as compared with previous similar work (Snyman&Ogudo *et al* [42]).

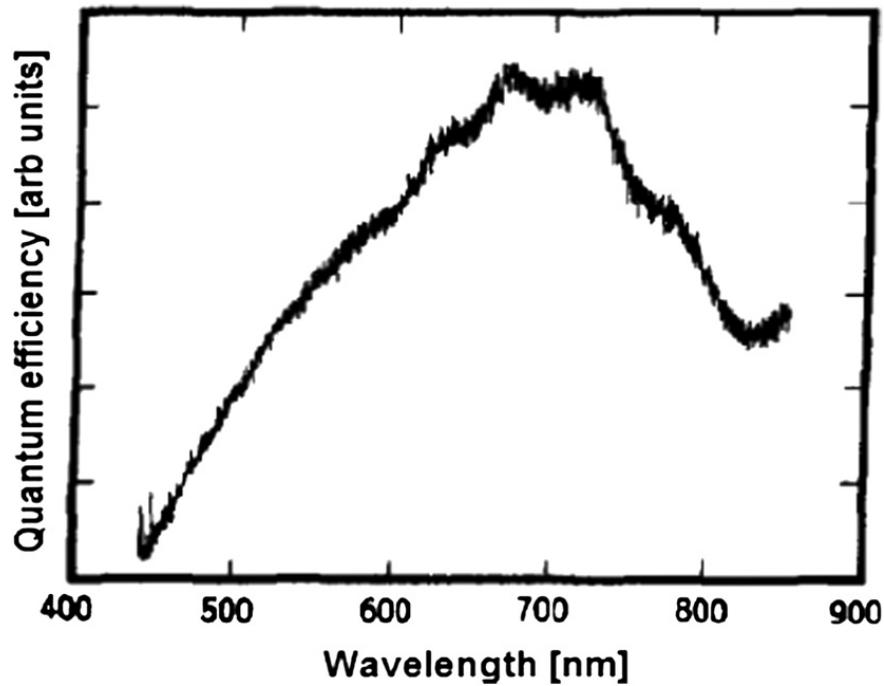
However, increases in efficiency seemed to be compromised by higher total device currents because of loss of injected carriers, which do not interact with avalanching carriers.

Latest analyses of the work of [42] shows that longer wavelength emissions of up to 750 nm can be achieved by utilizing the electron relaxation techniques in the purer n-side of the Si p-n avalanching junctions. This development has a very important implication: The spectral radiance of the resulting structure LED device compares extremely well with the spectral detectivity of the Si technology, such as Reach-through Avalanche Photo Detector (RAPD) technology and SiGe/Si photodetectors. More information about the design and performance aspects of our latest E-field and momentum shift assisted, 750 nm Si LEDs, can be found in [43]. It is worth mentioning that, controlling the defect density in this LED device, one can favour either the 650 or 750 nm emissions, and a total emission intensity of up to 1  $\mu\text{W}$  per 5  $\mu\text{m}^2$  area at the Si-SiO<sub>2</sub> interface has recently been observed.



**Figure 2: Si LED integrated in CMOS integrated circuit technology as an optical source [110]**

Figure 2 shows a design of a top-down as well as cross-section layout, of a Si CMOS and avalanche operation-based LED [110]. The LED consists of an  $n^+$  bar placed opposite to two  $p^+$  bars and diagonally away from the  $n^+$  bar. All were embedded in a p-well containing  $2 \times 10^{16}$  ions. The  $n^+$  and  $p^+$  regions define the peripheries of the  $\text{SiO}_2$  field oxide layer and define the centre of  $\text{SiO}_2$  field oxide layer. Upon biasing the structure with positive bias voltage on the  $n^+$  and negative bias voltage on the  $p^+$  region, the depletion region extends from the  $n^+$  edge facing the  $p^+$  region in the  $\text{SiO}_2$  field oxide layer. The intensity of the emitted light was approximately 1nW per micron length at an operating voltage of 15V and operating current of 1mA. The LED emitted from 450 to 750 nm with a spectral tail reaching deep into the near infrared region, a trend which is similar and comparable to the emitted spectral of a 5x1 micron line width CMOS integrated CMOS avalanche LED of Kramer was observed (see Figure. 3).



**Figure 3: Emitted spectrum as of a 5x1- $\mu$ m line width, CMOS integrated CMOS avalanche LED [111].**

Si avalanche-based LEDs alone, when integrated into CMOS circuits, offer the following advantages:

1. *Good dynamic range in optical signal detection*

With Si technology, small micro detectors of high sensitivity can be fabricated between 450 and 750 nm. The leakage currents of small  $10 \times 10 \mu\text{m}$  detectors are in the order of pico amps at room temperature and the low-frequency power detection levels are in the order of pW [44]. Power emission levels emitted from Si CMOS LEDs are in the order of 10 to 100 nW, which is three to four orders higher than the power detectable by CMOS p–n detectors.

2. *Bandwidth speeds greater than 1 Gb/s*

The modulation speeds of small SiAv CMOS LEDs are high, because the LEDs device operate in reverse bias mode and the small dimensions of the device result in low parasitic capacitances and very high modulation speeds [45]. Noting that, the modulation speed of the integrated Si LEDs in CMOS integrated circuits is not only determined by the surrounding driving circuits but also the signal processing circuitry. Substantial progress in modulation speed has been made in these LEDs leading to GHz signal processing speeds. Optical source and sensor-based systems can hence be fabricated in CMOS integrated circuitry at moderate to high optical modulation frequencies.

3. *Good electrical isolation*

Because of low leakage currents at room temperature, Si CMOS technology offers very high electrical isolation, immunity to interference, and high signal security.

#### 4. System reliability

Si diodes that utilize the avalanche concept in order to regulate and control voltages in CMOS integrated circuitry have been highly reliable [46]-[47].

No optical LEDs source and detector are readily available at 1550nm wavelength for CMOS chip technology; optical communications which require Germanium (Ge) layer structure and which is a much complex technology and very expensive in fabrication and manufacturing the systems are currently been utilized.

Si Avalanche based LED technology has been developed in the 650 - 850nm wavelength regime [48]. Correspondingly, small micro-dimensioned detectors with  $\text{pW}/\mu\text{m}^2$  sensitivity have been developed for the same wavelength range utilising SiGe detector technology with detection efficiencies of up to 0.85, and with a transition frequency of up to 80 GHz [49]. Various researchers on integrated opto-electronics have highlighted the need for small-dimension, optical communication systems all integrated into mainstream silicon fabrication technology [50] - [54]. The realisation of efficient on-chip light-emitters has however been a major technological challenge.

A research area known as “Silicon Photonics” has in recent years emerged [55] - [57]. The technology dealt with in this research area offers the advanced processing of data at ultra-high speeds and advanced optical signal processing on-chip. This technology may also provide contributions towards solving the current chip-to-chip interconnect density problem. Until now, this technology has primarily focused at the 1550nm wavelength regime, mainly in order to conform to the main terrestrial long-haul and telecommunication bands because it has losses as low as 0.2dB/km and can support Tb/s bit rates by virtue of wavelength division multiplexing (WDM). The realization of waveguides, modulators, resonators, filters etc., on silicon chip has been performed until now with relative ease by using mainly silicon-on- insulator (SOI) technology [58]. In the absence of an efficient visible light source at 1550nm wavelength, these systems currently operate mainly with external light sources. Recently, a Ge-on-Si laser source was announced by [59], it provides coherent optical emission on chip. It however, utilizes quite complex Ge layer technology [60] - [62], and the high speed characteristic of this optical source has also not been well defined.

Microwave photonics systems deal with the generation, processing and distribution of microwave and millimeter signals by optical beams by benefiting from low loss, large bandwidth and immunity from electromagnetic interference, Furthermore, the use of Integrated Microwave-Photonics (IMWP) devices greatly reduces the system complexity and offers major advantage of integrating all the technological processes into mainstream silicon fabrication technology. With little adaptation, it could be made compatible with standard silicon BiCMOS fabrication technology, the most promising of the current silicon technology. While in the literature such IMWP circuits are realized at 1.55 $\mu\text{m}$  (using III-V lasers on Silicon and Ge detectors for example), we investigate in this chapter the possibility to use pure Si and SiGe/Si

materials to provide both the optical detector and emitter, through the use of shorter wavelength. While the previous approach is considered to be BiCMOS compatible, our approach is expected to be fully BiCMOS integrated. For instance, the demonstration is made on bipolar Telefunken Technology.

SiGe detector structures, which is reasonable compatible with mainstream silicon technology has been developed that offers detection at 850nm wavelength with high-speed SiGe technologies [63],[64] & [65]. The use of SiGe layer in this process is quite straightforward and simple as a single SiGe layer strained onto Silicon is commonly used to fabricate the base of SiGe/Si heterojunction bipolar transistors (HBT).

Although complete integration of photonic systems onto CMOS platforms has been promoted, only relative few optical communication systems have been proposed for silicon CMOS technology, and then mainly for the 1550nm wavelength regime [66],[67]. And again, from research record the SiGe detector technology utilized in this wavelength regime is also very complex in structure and expensive to design. SiGe as opposed to SiGe/Si requires a Germanium layer to be grown on Insulator or on Silicon. This is an additional step to the standard SiGe/Si HBT technology.

Complete integration of photonic communication systems on CMOS optical integrated platform is highly desirable. IBM announced their new “optical bus” that currently utilize printed circuit board (PCB) and polymer based waveguides, that are deposited directly onto PCB (Scow, Doany & Kash, Sept 2010). First iteration bi-direction CMOS based chip interface systems have also recently been developed for 20MHz [68]. However, no on-CMOS chip optical wave guiding link at 650nm-850nm wavelength has been achieved so far.

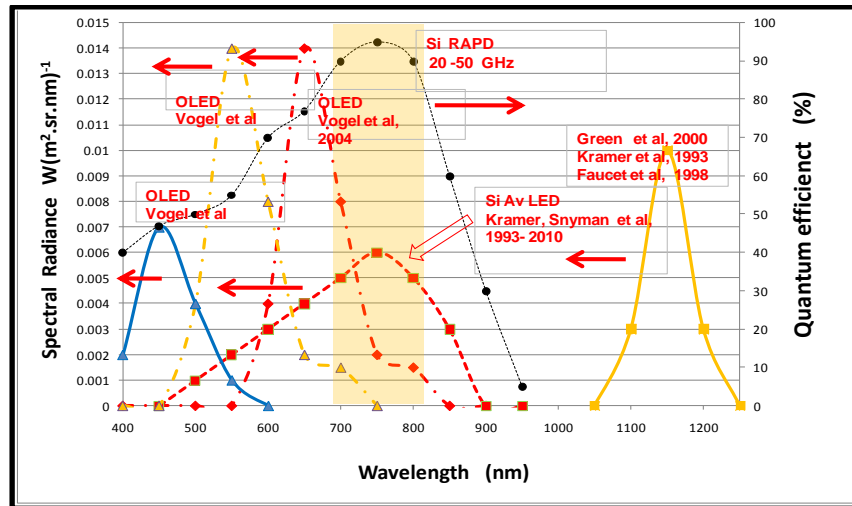
A very first iteration of all-silicon and CMOS based optical link on-chip, utilising a Si CMOS Av-based light-emitting source (Si Av LED), a 5x1x150 micron Silicon-Nitride over layer based wave-guiding and a specially designed, lateral incident optimized, and CMOS-based photo-detector have recently been realised by [24]. However, the optical propagation into the Silicon-Nitride over-layers seemed challenging, and led to high coupling losses. The gain and frequency capabilities of the all-silicon CMOS compatible detectors also offered major challenges.

In this study, we focus on the development of an optical communication device and data transfer system at near-visible 0.65- 0.85 micron wavelengths, utilizing a combination of Silicon Avalanche based Light Emitting Devices (Si Av LEDs), SiGe LED source, Silicon-Nitride based waveguides and SiGe detector technology. We propose the utilization of a combination of high speed Si Av LED sources, Si nitride waveguide technology, i.e, in the 650-850nm regime and high speed SiGe detector technology in order to achieve the above goals. The proposed operating wavelength is about half of 1550nm, i.e, in the 650 - 850nm regime. We extensively analyse the transmission and optical wave-guiding characteristics of the designed waveguides and report on the initial simulated and experimental results as obtained.



A number of viable optical light emitters have been developed in the 1990s that have already been integrated with ease into mainstream silicon CMOS technology [69] - [75]. These ranges from Silicon forward bias p-n LED devices that operate at near 1 $\mu$ m wavelength region [76] to avalanche based Si LED devices that operate in the visible 450-750nm visible range, and to organic light emitting diode (OLED) structures [77] - [79].

Figure 4 shows the spectral response of Organic Light Emitting Devices (OLEDs) and Si avalanche-based light emitting device (Si Av LED) in terms of optical radiance. A comparison is also given with the spectral detection range of reach through avalanche detector (RAPD) devices.

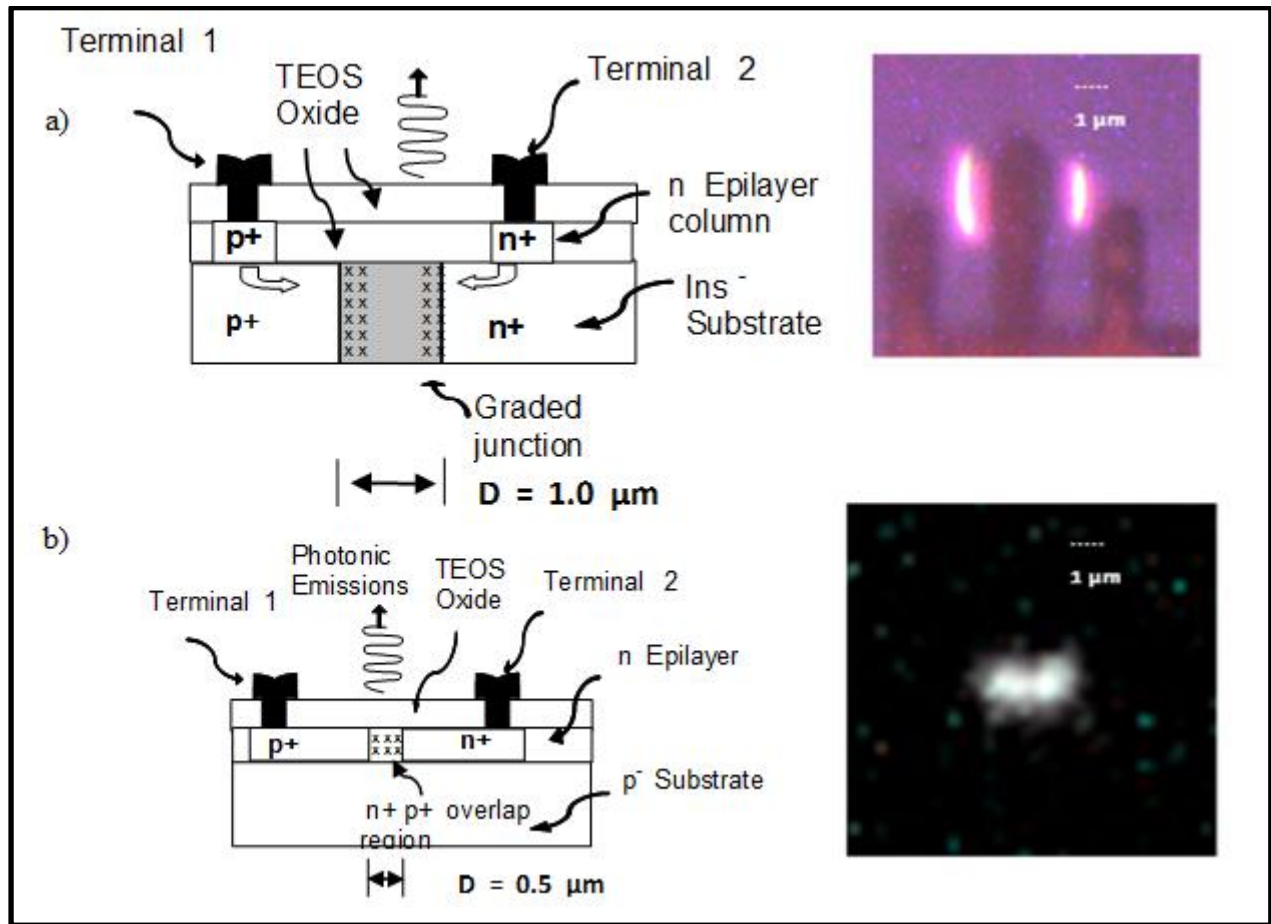


**Figure 4: Spectral Characteristics of Si avalanche-based light emitting device (Si Av LED) and comparison with the spectral detection range [79]**

Only some of these light emitters are currently completely compatible with current mainstream silicon CMOS processing technology. The forward biased p-n junction LED devices emits near 1100nm [80]. This is near the band edge absorption of silicon and lead to weak detection of the radiation. Organic based Light Emitting Diode (OLED) technology utilise the sandwiching of organic layers between doped silicon semiconductor layers and yield good efficiency in spectral band wavelengths from 450 to 650nm [81]. Although this technology requires the incorporation of foreign organic material through process procedures, it is a viable option. The organic layers however require low temperature deposition and processing procedures and the technology can hence only be introduce as post processing and hence in the outer layers of the CMOS processing procedure. A major uncertainty with regard to this technology is the high speed modulation capability of these devices.

Si Av LED devices emitting in the 450-750nm regime have been known since quite early [82] - [83]. Viable CMOS compatible and avalanche based Si LEDs (Si CMOS Av LEDs) have however, only emerged since in the 1990's [84] - [85] & [86]. Kramer *et al*, was the first to propose the utilization of Si Av LEDs into CMOS technology and thoroughly illustrated some potentials of this technology [87]. Snyman *et al* have

subsequently realized a series of *practical* first iteration and *utilisable* light emitting devices in *standard CMOS* technology using CMOS compatible operating voltages and current levels in the millivolts and microamperes' range as in Figure 5. Substantial further developments of the LEDs emerged during 1996-2013 [88] - [91]. This was mainly achieved by using novel surface engineering, current density modelling and dynamic carrier density engineering techniques. The developed devices showed about three orders of increase in optical output as compared with previous similar work. Particularly, promising results have recently been obtained regarding further increasing the efficiency through depletion layer profiling and carrier and momentum engineering [92], [93]. In our prior work, specifically introduced a graded junction  $p^+n^+Si$  LED technology with graded ionized dopant profiles in the lower doped p region. This increased emission intensity with about two orders of magnitude as compared to other recently technology published results [94]. The technology is appropriately nomenclature Silicon Avalanche based Light Emitting Diode (Si Av LED) technology [95].



**Figure 5: Electro-optical interfaces realized in 0.35 $\mu m$  technology with standard CMOS design and processing procedures (a) graded junction  $p^+n^+$  RF bi-polar developed (b)  $p^+n^+$  overlap device unit 0.5 $\mu m$  dopant developed [119]**

Figure 5 shows Si avalanche-based light emitting device (Si Av LED) and electro-optical interfaces as recently realised by (Snyman&Ogudo *et al*), in a 0.35 $\mu m$  technology with standard RF bipolar design and processing procedures (Snyman&Ogudo *et al*, 2013). Figure 5 (a) shows a graded junction  $p^+n^+$  Si Av

LED developed with RF bi-polar process technology and Figure 5 (b) shows a  $p^+n^+$  device unit  $0.5\mu m$  dopant developed.

Si Av LED devices offer the following advantages for integration into Si mainstream technology:

- They can emit up to  $10\text{-}100\text{nW}/\mu m^2$  at  $450\text{-}750\text{nm}$  wavelength regime at compatible CMOS operating voltages and currents levels (3-8V, 0.1-1mA) (Snyman et al, 2010). This is about a factor of hundred higher than any other recently developed in the same field (Snyman&Ogudo et al, 2013).
- They can be realised with ease using standard CMOS design and processing procedures, greatly reducing the cost and complexity of such systems [96] - [97].
- The emission levels of the Si CMOS Av LEDs is  $10^{+3}$  to  $10^{+4}$  higher than the detectivity of silicon p-i-n detectors, and hence offer good dynamic range in detection and analyses.
- Very high modulation speed possibilities ( $> 10\text{ GHz}$ ) with direct driving circuit of the sources [98].
- They can be incorporated at the silicon-SiO<sub>2</sub> interface level, since they are high temperature processing compatible (Beal et al, 2008).
- The emission wavelength can be reasonably engineered from very broadband to quite narrow band emissions by incorporating specific wavelength engineering processing procedures. Particularly,  $p^+n$  designs show strong spectral emissions around  $0.75\mu m$  (Snyman et al, 2010).

#### 1.4 SiGe/Si Silicon HPT bipolar technology

Silicon-Germanium detector technology integrated in a silicon processes, has recently been quite well established [99] - [101]. Silicon bipolar technology has been known to yield good detectors, particularly Si p-i-n Reach Through Avalanche Photo Detectors (RAPDs) yielding up to  $10\text{ GHz}$  of response at efficiency of up to 0.85 [102]. For radiation at  $0.55\mu m$ , p-n configurations offer up to  $0.6\text{A/W}$  responsivity at around  $1\text{-}30\text{GHz}$ , while p-i-n configurations offer up to  $0.3\text{A/W}$ . All these well-established device configurations can be incorporated in CMOS or modern RF bipolar technology with relative ease using similar and adapted processing steps. In some cases, detectors may be designed in order to optimize detection of lateral incident radiation. Polleux et al.[104] have particularly made contributions with regard to developing SiGe phototransistors utilising standard RF bipolar processing technology and that have a high detection at  $850\text{nm}$  and with high electrical transition frequencies of up to  $30\text{ GHz}$  [103] - [105], with high internal gain (up to  $30\text{ dB}$ ).

*The combination of utilising adequate emitting CMOS compatible Si Av LEDS, together with good silicon Germanium detectors and a good dynamic Silicon-Nitride optical waveguide as offered by SiGe based bipolar technology process at about  $750\text{nm}$  wavelength, subsequently show good potential to generate diverse on-chip optical communication interconnect and other integrated system applications directly onto CMOS chip.*

## 1.5 The research Problem statement

As a synthesis, a major current challenge is to design and realise on-chip silicon integrated micro-optical links at 750nm wavelength, with a SiGe RF 0.35 micron Bi-polar process that could yield HF on-chip optical IC's using ALL SILICON noncomplex processing technology and cost effective in implementation.

To solve the problem of no optical sources to be available to 1550nm, the existing technology as developed by *Snyman et al* could be used in the intended optical link design and realization at 750 nm operating wavelength.

The design and realisation of high frequency (HF) optical waveguides in micro scale level, which operates at 750nm using TEOS materials, Silicon-Nitride and silicon oxi-nitride materials as optical waveguide can be developed. By using this technology, the current advantages as achieved with integration of Si Av LEDs in CMOS technology can be combined with the high frequency characteristics as offered and added with the RF Bi-polar technology. The process procedures are also very much related to current state of the art CMOs processes.

Micron dimensioned optical sources, tailor design Silicon-Nitride optical waveguides and detectors can be integrated on the same silicon chip substrate to form complete communication on-chip micro-optical links (*to provide solution to low communication bandwidth and high power consumption anticipated for silicon photonics on-chip interconnects for future microprocessors and sensors*). Avalanche based Si LEDs (Si Av LEDs), Schottky contacting, TEOS densification strategies, Silicon-Nitride based waveguides, and state of the art SiGe bipolar detector technologies can be used as key design strategies to realize micro on-chip optical communications link.

With the aim of wave guiding of light along structures as offered by the Bipolar process and coupling of light into secondary elements as offered by the process modulated bandwidths of up to (30 to 40 Gb/s) can potentially be achieved. This could enable high density interconnection in integrated circuit packages, high speed computer processors, helping to implement on-chip optical processing and to generate optical highway communication channels from and to the chip to produce photonic signal processing using standard CMOS and bipolar-base integrated circuitry.

*In summary: the sub-problems are:*

1. *The design and realisation of micron dimensioned Silicon-Nitride optical waveguides operating at 750nm wavelength.*
2. *How do we design HF Si Av LEDs and Si-Ge Detectors that could yield high frequency RF optical links using simple all silicon processing technology.*
3. *Design Silicon-Nitride optical waveguides and detectors that can be integrated on the same silicon chip using modern RF Bi-polar IC processing platform.*
4. *Miniaturisation of the design on-chip optical links using silicon bipolar processing technology.*

# CHAPTER 2: SiGe LED Technology: Edge-emitting topologies

## 2.1 Introduction

This chapter focuses on SiAvLEDs and SiGe LED design layout geometries that are planned to be integrated into Silicon technology. BiCMOS would be the ideal attempt, and this chapter proposes a first step by integrating those devices into an RF Bipolar Technology of choices. The chapter first presents a brief description of the light emission mechanism in silicon and the energy band gap scheme for the impact ionization process for an electron in a reverse biased pn silicon junction. Then, the layout structures of the three Silicon-based LEDs designed from SiGe2RF Telefunken technology are proposed. The description of the Si/SiGe HPT detector layout structure and dimensions as implemented in the optical links are also presented. Lastly, the proposed integration of the optical source, the designed optical waveguides and the detector on the same chip to form a full BiCMOS on-chip optical links is highlighted.

## 2.2 Light emission mechanisms in Silicon

The avalanche light emitting diode in Fig 6 gives a simple but basic synopsis for the light emission process in silicon. Electrons are accelerated in the strong field of a reverse biased silicon pn junction, the energy gained by the carriers is transferred to the lattice, and electron-hole pairs are formed during the subsequent host atom ionization processes.

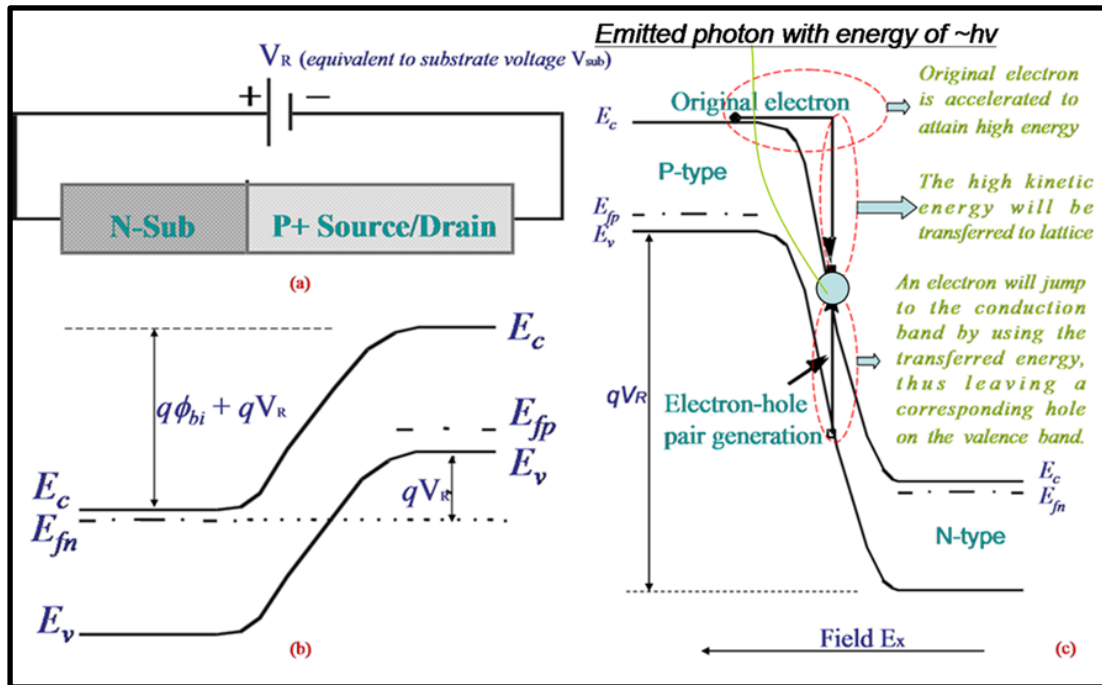


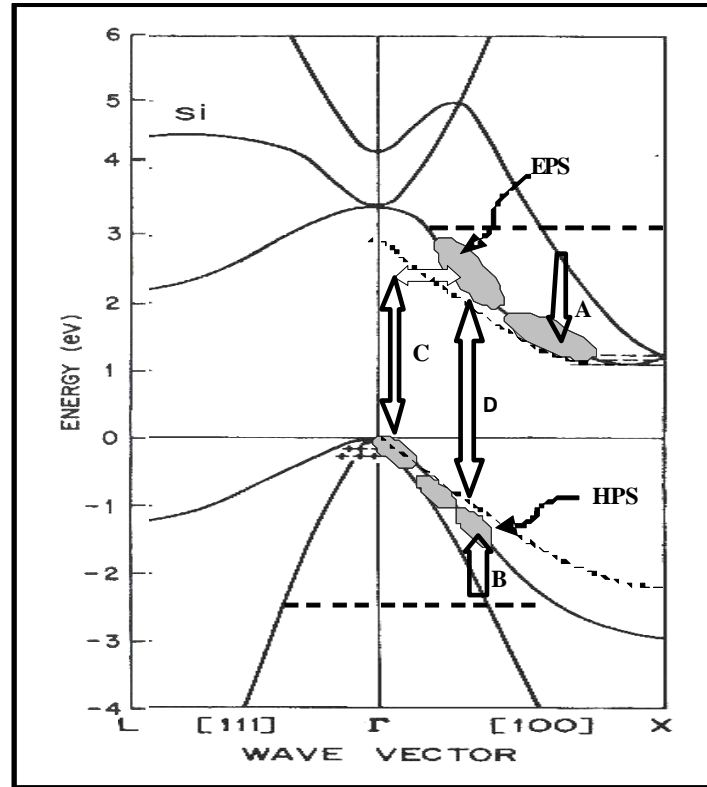
Figure 6: Energy band scheme for the impact ionization process for an electron in a reverse biased pn silicon junction

Many perturbations are possible in the electron hole excitation process:

1. Defects such as dislocations, vacancy and interstitial complexes are responsible for electron-hole pairs generation at the sites of the defects particularly in prevailing strong E –field conditions.
2. Interstitials and dopant impurities assist with radiative recombination phenomena of electron-hole pairs.

Thus, several theories have subsequently been presented for explaining light emission phenomena such as:

- Excited carriers are retarded in the crystal lattice, and according to a classical Maxwell approach, through scattering interaction with the lattice, a part of the energy may be directly converted to photons [117]
- Further theories have also been proposed that especially intra-band transitions may be responsible for the light emission processes. Such transitions may occur between the first and second conduction band for electrons as well as for the first and second bands of the valence band for holes in silicon [118]. The energy band diagram showing the various transitions in silicon was investigated [118]. At various excitation conditions, specific photon transition can be enhanced as shown in Figure 7:
  - If electrons gain enough energies and momentums to high up in both the first and second conduction bands to 1.8 eV, direct intra-band relaxation transitions of Type A (see Figure 7) could be favored, corresponding to about 750 nm in wavelength. Similarly, intra-band transitions can also occur in the valence band, between second and first valence bands leading to transitions of about 1.5 eV (transitions of Type B in Figure 7). This would lead to emissions of about 850 nm wavelength.
  - If hole energy values are sufficiently raised such that their momentum values correspond with the near momentum values of electrons excited in the conduction band, various indirect inter-band transitions of Type C, as in Figure 7, and with photonic emissions of approximately 2.3 eV or 650nm wavelength can occur, mainly through a process of phonon assisted carrier recombination.
  - When electron and hole momentum values correspond more precisely in the respective bands, direct type transitions of about 2.8 eV can be promoted between the conduction band and the valence band (Transitions of Type D in Figure 7).



**Figure 7: Energy distribution of populations of electrons and holes in the conduction band and valence band of silicon for various excitation conditions, momentum changes, and possible subsequent photonic transitions**

A series of theoretical simulations of carrier energies and momentums in the silicon band structure has been performed in [119] when a volume of crystal is subjected to high electric fields as experienced in these devices during strong reverse bias conditions. It was observed that the energy distribution of the electrons in the conduction band for this excitation field range from 1.1 to 1.7 eV, while quite a wide momentum scattering is observed for electrons. Similar tendencies were observed for holes, but the spread in both energy and momentum is less due to the heavier effective mass of holes in silicon.

During previous work and experimental analyses [120] - [122], some important phenomena have been observed that can provide important clues for further optimized device design.

1. Light emission was only observed on the n-side of pn junctions, indicating that electrons are primarily responsible for light emission phenomena in silicon.
2. High doping and n-type doping enhance the light emission. Strong light streaking is observed in n-material when high electron densities are injected into the avalanche junctions.
3. The emission intensity seems to be clearly related to the density of the carriers that traverse or are injected into specific crystal regions.

### 2.3 Si Avalanche LEDs Fabrication: Edge emitting topologies

This chapter focuses on the possibility to use pure Si and SiGe materials to provide both the optical emitter and the detector, using shorter wavelength (750nm). This approach is expected to be fully BiCMOS integrated. For instance, the demonstration is made on bipolar Telefunken Technology. The applications of this approach are not only related to silicon integrated optical interconnect, but could embrace much larger field such as the optical sensing domain for biochemical applications or others.

Key constituents of such a system are an effective BiCMOS compatible optical source, optical waveguide and an effective optical coupling from the source to the waveguide and to the optical photodetectors such as SiGe HPT. These all seem to be highly viable in regard to the present analyses and proposed technology process.

This chapter starts with the presentation of the edge emission Si LEDs. It has been fabricated using the 80 GHz SiGe2RF Telefunken GmbH SiGe Bipolar technological processes, which is crucial to be implemented for ultra-low-cost silicon, based IMWP systems. One key aspect of this research is to implement a Si Av LEDs in such a commercial technology without the addition of masks and processing steps. We modify the design layout geometries for different bias configurations in order to obtain different efficient emission point in the source structure. This approach ensures a straight compatibility with SiGe circuits on the same chip, and makes the Si and SiGe Avalanche LEDs directly integrated into an industrial foundry.

The Telefunken SiGe2-RF Bipolar Silicon Germanium process technology exhibits  $f_T$  up to 80GHz and  $f_{max}$  up to 90GHz. This makes this technology able to provide circuits working above 10GHz and potentially up to 60 GHz in some configurations. This RF bipolar technology allows the production of wafers with applications in high-speed cellular, devices used in high performance standard RF in various applications.

As in the SiGe1RF technology of Telefunken used to create the LEDs sources and the SiGe detector, the Germanium content is high with values in the range of 20-25% and might be almost vertical pillars column block structure with the base. This process is a 0.8 $\mu$ m lithography double polysilicon heterojunction bipolar technology. The minimum emitter size on the layout is of 0.8x1.4 $\mu$ m<sup>2</sup> for vertical NPN HBT transistors, which provides actual size after processing of 0.5x1.1 $\mu$ m<sup>2</sup> due to lateral spacers. This technology leads to two LEDs types: one with a selectively implanted collector (SIC) NPN LEDs and the other one without. The difference between them is the additional mask required by the SIC-transistor, influencing the high frequency performances and static characteristics. This option allows transition frequency ( $f_T$ ) to reach the 80GHz value for SIC transistors, against only 50GHz for non-SIC transistor, with  $f_{max}$  of up to 90GHz in both cases. This process technology also offers PNP transistors, diodes (PN, Zener, ESD, Varactor and Schottky) and passive devices such as inductors capacitors and resistors. In the frame of our relation with Telefunken, a Non-Disclosure Agreement (NDA) has been signed and no information about the detailed process cross-section can be given.



It is important to give a general schematic and descriptions of the optical source LEDs structures as in Figure 8 (a), (b) & (c).

Figure 8 shows the three different optical source structures that were designed utilizing the 0.35micron RF bipolar technology, each with different configuration source structures, different waveguide structures, but with the same basic SiGe detector structure in the optical links.

In figure 8 (a), the optical source was designed with an  $n^+-n$   $p^+$  columnar structure located laterally on the P-type silicon substrate of very high resistivity. The regions between the elevated source and detector structures were filled with plasma deposited oxide. The columnar structures were all of micron dimension, such that the structures were composed of  $1\mu\text{m}$  cube substructures. The regions are doped as indicated in Figure 8 (a). The regions were appropriately electrically contacted during experimental measurements on the fabricated device on the wafer in order to reverse bias the first  $p^+ n$  junction. Upon reverse biasing, the depletion region penetrates through to the  $n^+$  region in order to strengthen and unify the electric field in the lowly doped  $n$  region. From our previous experience gained from previously designed devices, we know that the light emission would occur near the surface region of the middle  $n$  region and extend more or less laterally across the whole region. The region between the Si Av LED source and SiGe detector were filled with normal TEOS plasma deposited oxide as part of the available process procedure. The middle layer was subsequently interfaced laterally to the optical light emission region, and the waveguide implemented here was (OWGD1)) designed as in Figure 13. Appropriate air slots were made on the sides of the waveguide in order to minimise laterally induced oxide parasitic capacitance.

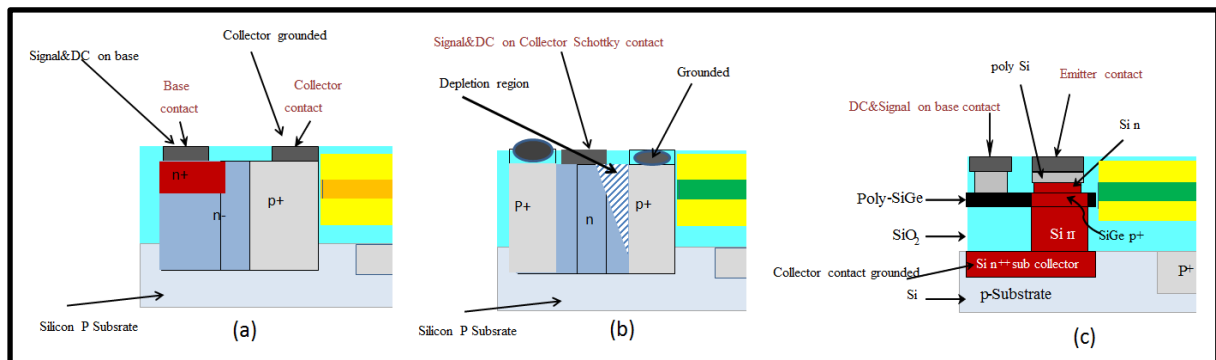
In Figure 8 (b), the test structure of the LEDs source was designed in the same basic lateral columnar structure for the optical source as in 8 (a), but strategic design of a rectangular Schottky configuration contact of Aluminum on n-Silicon is fabricated in the columnar structure middle lowly doped  $n$  region on the optical source. The two  $p^+$  columnar regions were grounded as required by the RF probe bias during measurement process, and the DC and modulation RF signal was applied on the Schottky contact. Positive voltage bias placed the Schottky contact in forward bias mode and caused a triangular depletion region towards the  $p^+$  region of the LED optical source, thereby reverse biasing the  $p^+ n$  region. This configuration drastically reduces the total depletion region volume and hence reduces depletion layer capacitance. The elongated and uniform electric field region and its associated minimized capacitance would hence enable ultra-high modulation frequencies. Since small dimensions in  $\mu\text{m}$  were used and the light emission processes are impact ionization and avalanche related aid.

Figure 8 (c) is a vertical cubical columnar HPT structure designed to function as an optical source. The emitter-base  $n^+$  (SiGe) which contained 20% of Germanium was placed in reverse bias and in the avalanche regime. The emitter/base terminals were shorted in order to initially simplify the operation of the optical

source device to function as an optical emission source, and bias is placed on the bottom contact of collector region. Because of layout and process design and processing limitations, the emitter n+ region is grounded. The SiGe detector structure of this nature has a transition frequency of up to 80GHz, it was assumed that when it was utilized as optical source by reverse biasing base-collector junction in avalanche reverse bias mode, the structure could attain similar operational frequency with optical emissions following this modulation frequency.

On the same third configuration, the optical source was operated in a forward bias configuration during experimental measurements, such that emitter n+ p (SiGe) junction is in forward bias mode. In this configuration, the emitter n+ p (SiGe) region is grounded and negative voltage bias of 2V is applied to the p+ SiGe base region. Electrons were injected from the n collector region and the carriers were energized through conduction transfer through the low doped n region of the collector. When these carriers are injected in the SiGe base region, they would contain enough energy in order to then transfer electrons from the L valley to the T band structure valley of SiGe. With 20% Germanium doping, the emitted wavelength for this design is expected to be below 1000nm emission wavelength.

The very small columnar conduction regions, used in the optical sources in this configuration, would reduce depletion layer capacitance and the subsequent carrier's transit time in the devices.



**Figure 8: Schematic cross-section of Si and SiGe LEDs designed into Telefunken SiGe technology**

Vertically emission LEDs are known for their high optical light coupling into waveguides but suffer from a trade-off between conversion efficiency and frequency performance, the latter being limited by the transit time. Edge-coupled devices overcome this problem as the optical signal enters through the side of the waveguide device and propagates orthogonally to the detector. This gives the freedom to design longer devices to ensure a high proportion of the optical signal to be propagated while maintaining a low absorption. In this section, we present the first edge emitting Si/SiGe LEDs based on the available commercial SiGe/Si technology for low cost emitters for on-chip or inter chip optical IC applications. Then, we perform an optical emission power (edge mapping) measurement of the edge-emitting LEDs in order to

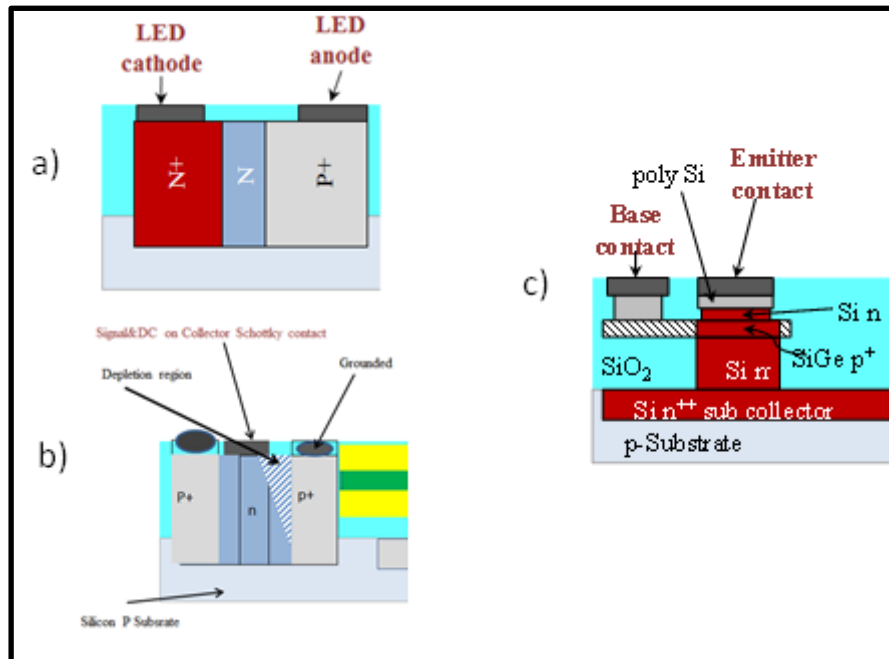
observe the highest power emitting region or areas in order to localise the best emitting region that will be laterally aligned with the waveguide structure interface.

## 2.4 Proposed Si and SiGe Avalanche LEDs

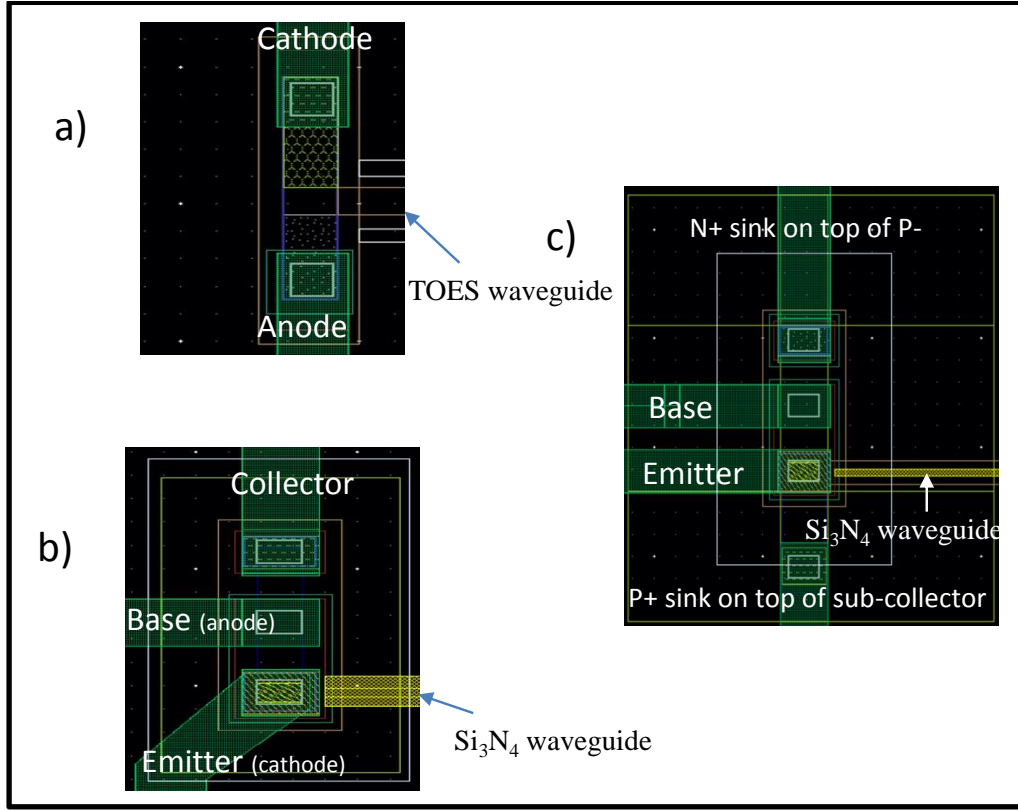
Based on the previous works of top emitting Si AV LEDs, we design and present three different LEDs that are compatible with the existing SiGe HPT technology and we use them together to fabricate a full on chip optical link.

Using our experimental and theoretical results on top emitted Si LED, we designed three different LED implemented using the SiGe2RF Telefunken GmbH technology to be used in a full on-chip optical link as shown in figure 9. We use our previous work experiences on the SiGe HPT technology to implement them in a full on-chip optical link for a first test.

The layouts of the three Silicon-based LEDs designed from SiGe2RF Telefunken technology are shown in figure 9. The RF and DC probing contacts and the designed OPTICAL WAVEGUIDES are also shown in the cadence layout in Figure 10.



**Figure 9: The schematic of the three different Si based Av LEDs to be implemented in SiGe2RF Telefunken GmbH technology for full on chip optical link system; a) Si Av N+NP+ columnar, b) SiGe-N+PN- with collector contact and c) SiGe-N+P without collector contact**



**Figure 10: The layout of the three different Si based Av LEDs implemented in SiGe2RF Telefunken GmbH technology for full on chip optical link system; a) Si Av N+NP+ columnar, b) SiGe-N+PN- LED with collector contact and c) SiGe-N+P LED without collector contact**

The structures of these optical sources are described as follows:

- a) **Si Av N+NP+ columnar**: An  $n^+n-p^+$  columnar structure is placed laterally on the semi-insulating substrate. The regions are doped as indicated in Figure 10 a). The regions are appropriately electrically contacted during experimental measurements in order to apply a forward bias at the first  $p^+n$  junction. Upon forward biasing, the depletion region penetrates through the  $n^+$  region in order to strengthen and confine the electric field in the lowly doped  $n$  region. According to our previous experience gained from the previously designed devices, we know that the light emission would occur near the surface region of the middle  $N$  region and extend more or less laterally across the whole region. Note that using the process of Telefunken, the columnar structure still include a thin SiGe/Si. It is therefore a mix between Si Av LED and SiGe LED.
- b) **SiGe-N+PN-LED with collector contact**: The basic vertical structure of a SiGe/Si HBT is used. The emitter and collector contacts are grounded as required by the RF probe bias during the measurement process and a forward biasing together with the modulation signal are applied on the base ( $P$  anode) contact. Positive voltage bias places the anode contact in forward bias mode. The depletion region lies toward the  $n$  side of either the collector or the base, as the base is highly doped. Thus light emission will be in the  $n$  regions. As it will be describe in the following section, a V-shaped groove Silicon-Nitride waveguide with wider core is used along with this LED to realize the full optical link.

- c) **SiGe-N<sup>+</sup>P LED without collector contact**: A vertical cubical columnar SiGe/Si HBT like structure is used. It has four metallic contacts as shown in Figure 10 c) as it is designed from the HBT structure. The first two on the side are emitter and base, and the last two on top and bottom are additional N<sup>+</sup>/P<sup>-</sup> diode and P<sup>+</sup>/N<sup>+</sup> diode sink as shown in Figure 10 c) which were designed for other purposes (which will not be discussed here). The base-emitter SiGe pn junction is submitted to a forward bias in avalanche regime as a positive voltage is applied through the base and thus light is emitted in the depletion region of the pn junction. As it will be described in the following section, a Silicon-Nitride waveguide with narrow core is used along with this LED to realize the full optical link as light emission region is expected to be very narrow (only the depletion region of the base-emitter pn junction).

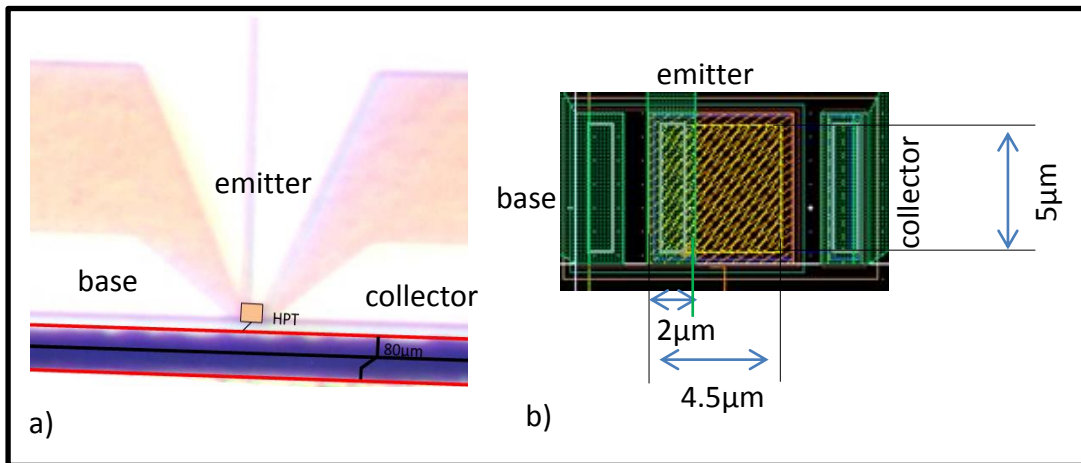
Since the SiGe/Si HBT of this nature has a transition frequency of up to 80GHz, it can be assumed that this will benefit to the speed of the optical source with the base-emitter junction placed in avalanche forward bias mode. With 20%-25% Germanium doping, the emitted wavelength for this design is predicted to be about 850 nm. However, the emission will be distributed among Si and SiGe regions depending on the voltage bias applied across the junction.

## 2.5 Description of the SiGe/Si HPT structure

Heterojunction bipolar phototransistors (HPT) are based on Heterojunction Bipolar Transistors (HBTs) with the design of an optical window to enable the light path into the device and with some of its layers made of optical absorbing material, especially in the base-collector region. Lateral illumination of the HPT is one method to improve the responsivity -bandwidth trade-off. This allows the propagation distance before a complete optical absorption to be long enough while the absorption layer remains thin enough to ensure short transit times. Lateral illumination of phototransistors can be done by injecting the light through the cleaved side of the device. It can also be achieved by using an optical waveguide integrated in the device structure, hence the choice of this kind of HPT.

The SiGe/Si HPT structure was implemented according to the geometry presented in Fig 11 (a). The basic HPT structure is designed by extending the emitter, base and collector layers of the reference HBT. In the case of the edge SiGe HPT, it is increased from  $0.8 \times 1.4 \mu\text{m}^2$  to  $4.5 \times 5 \mu\text{m}^2$  for better coupling with the light from the lateral waveguide. The HPT was designed and fabricated in [126], [127].

The final HPT is then  $4.5 \mu\text{m}$  wide (corresponding to the width through which light is horizontally coupled) and  $5 \mu\text{m}$  long (maximum absorption length of light) as shown in Fig 11 (b).



**Figure 11: a) Microscopic picture of the edge SiGe HPT, b) Layout of structure along with its dimensions.**

The  $\text{Si}_{1-x}\text{Ge}$  base layer sandwiched between the collector and emitter, both made of Silicon, is expected to play the role of an evanescent optical waveguide that detects light, at least partly given the optical beam size that will be injected from the waveguide optical coupling. The base profile is a 40-80nm thin abrupt SiGe layer with Ge content in the range of 20-25% and high p doping in the range of  $10^{19} \text{cm}^{-3}$ . The collector is typically 300-400nm thick with low doping. The emitter metal contact is designed on a reduced surface of the emitter to avoid additional optical losses by metal absorption of the light throughout the longitudinal direction, and to reduce the electrical parasitic capacitances.

In order to measure the SiGe edge- HPT individually, an optical free-space access is created at the edge that requires the HPT to be diced using a smooth shallow dicing blade close to the active area of the devices as shown in Fig 11 (a), giving a slickly polished surface state. We dice  $80 \mu\text{m}$  down to the substrate to have

a smooth surface at the optical beam input and then dice fully in depth and farther from the surface using a microscopic saw. The full and smooth dicing was processed at the Université Paris Sud – IEF laboratory with the help of Pr. Vivien. In our case, the SiGe HPT will be attached to an optical waveguide that will enhance its responsivity.

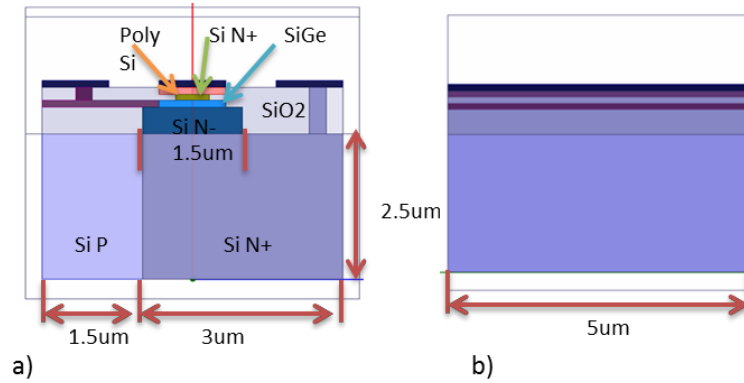
The Telefunken SiGe2-RF Bipolar Silicon Germanium process technology exhibits  $f_T$  up to 80GHz and  $f_{max}$  up to 90GHz. This makes this technology able to provide circuits working above 10GHz and potentially up to 60 GHz in some configurations [104].

In the frame of our relation with Telefunken, a Non-Disclosure Agreement (NDA) has been signed and no information about the detailed process cross-section can be given.

### *Light propagation behaviour in SiGe/Si HPT structure*

Z.Tegegne [125] demonstrated the behaviour of light propagation into a SiGe/Si phototransistor by using HFSS simulator. Figure 12 shows the vertical stacks of the SiGe/Si HPT structure under study. We simulate a 5 $\mu$ m long edge illuminated phototransistor under an 850nm wavelength illumination.

The SiGe base of the HPT is modeled with a high refractive index of 3.57. The surrounding Si layers are modeled with a lower refractive index of 3.42. We define a 1x1 $\mu$ m square excitation port at the input and output of the structure aligned to the SiGe base. We then use the material properties as given in Table 2 to perform the simulations.

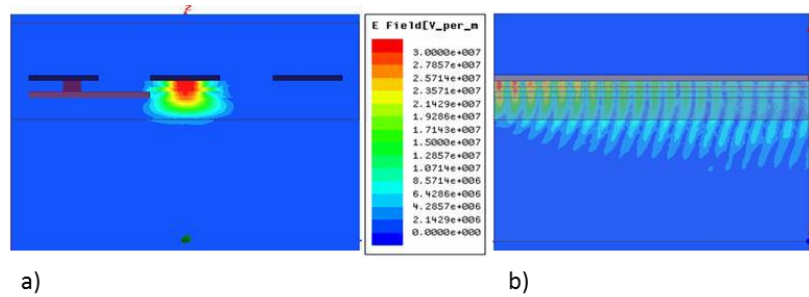


**Figure 12: Basic simplified structure of SiGe/Si HPT used for simulation.**

**Table 2: Properties of the materials used in HFSS simulator.**

	Material	Purpose	Thickness (nm)	Relative permittivity	Conductivity (S/m)
1	Contact metal	metallization	100	1	5.80E+07
2	poly Si	Emitter contact	120	11.7	5555.5
3	N+ Si	Emitter and sub collector	te=100, tc=2500	11.7	3472.2
4	N- Si	collector	450	11.7	357.14
5	P Si	substrate	2500	11.7	5
6	SiGe	Base (here as OPWG)	120	12.724	1000.23
7	SiO <sub>2</sub>	passivation		3.9	1.00E-12
8	TiSi	for base contact	120	3	1.98E+06

The simulation results are shown in Figure 13. According to the physical dimensions and to the width of the excitation port (assumed to be optical spot size), we deduce that 69% of the injected optical field is injected into the active region (including base  $\approx 12\%$ , emitter  $\approx 12\%$  and collector  $\approx 45\%$ ). The remaining 31% is injected into the sub-collector region. However, when light is propagating through the structure, the beam starts spreading into the sub-collector and eventually then into the substrate as shown in Figure 13 b). After this enlargement of the beam path, we can observe that the active region is still confining the light in its proximity. We also observe large portion of the light is attenuated near the entrance of the structure due to miss coupling alignment.



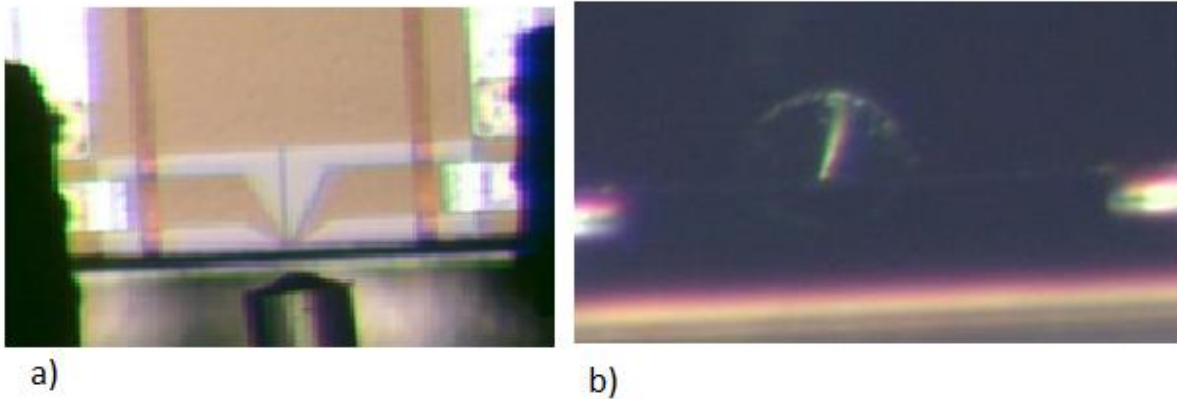
**Figure 13: The magnitude of the electric field evaluated by HFSS at 850nm. a) at the input port, b) along the propagation axis.**

This analysis validates the fact that an edge-SiGe HPT at 850nm is viable in the sense that the light can be confined in the active layers of the HPT despite an absorbing substrate. The simulation results motivate to the characterization experimentally of such a device, in the specific condition in the application as a detector for on-chip optical interconnect and optical chip to chip connect in optical links and some other applications.



### ***On-probe characterization bench setup***

The edge-SiGe HPT was tested independently through the prior edge-etching as described previously. An 850nm VCSEL is directly modulated and illuminates the HPT through a lensed multimode fiber (MMF) scanning the edge of the HPT. This VCSEL has a -3dB cutoff frequency of 12GHz. The VCSEL is biased to provide a 1.14mW optical beam at the end of the lensed fiber. A tilted mirror is used to monitor the alignment of the optical probe to the optical window of the HPT on the edge through the microscope as shown in Figure 14 a) and b).

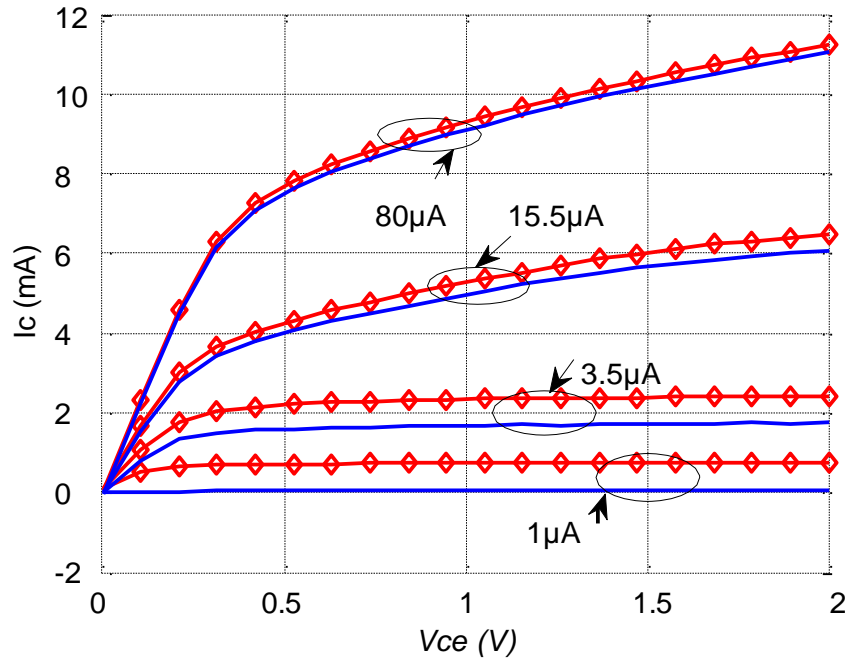


**Figure 14: a) Top view microscopic picture of the device under test and the optical probe pointing on the edge side of the HPT. b) Microscopic picture taken from 45° mirror.**

The distance between the lensed fiber and the HPT lateral surface is set at 50 $\mu$ m to align the optical window with the beam waist of the lensed fiber. The angle of the fiber versus the longitudinal axis of the HPT is approaching zero, but we suppose that some variation may still exist due to the difficulty of the experimental setup manipulation. We use a multimode light source and multimode optical probe from what was available at the time of this preliminary test. The HPT is mounted in a common emitter configuration topology with two 100 $\mu$ m-pitch GSG pads in order to perform on wafer DC and microwave measurements. One of the ground pads of the HPT is removed during dicing so that one of the GSG ground is suspended in the air.

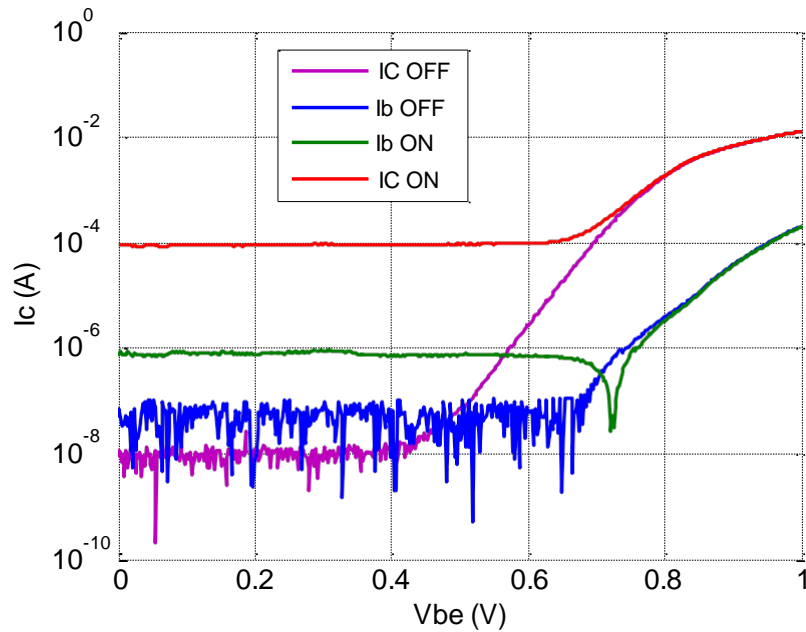
### ***DC characteristics***

Figure 15 shows the  $I_c$ - $V_{ce}$  curves of the edge illuminated HPT under illumination and dark conditions. The dark condition (blue solid curve) shows the pure electrical characteristics of the HPT.  $V_{ce}$  is swept from 0V to 2V for  $I_b = 1\mu$ A, 3.5 $\mu$ A, 15.5 $\mu$ A and 80 $\mu$ A. Under the same condition, the HPT is illuminated by 1.14 mW optical power through the edge. The result is an illuminated  $I_c$ - $V_{ce}$  curve (red diamond marked curve) with a noticeable increase in its output collector current. It can be observed from the plots that as  $I_b$  increases, the change in collector current (between dark and illuminated conditions) is less in absolute.



**Figure 15:  $I_c$ - $V_{ce}$  curve of edge illuminated SiGe HPT with light (red curves with mark) and under dark condition (blue curves) for different  $I_b$  values**

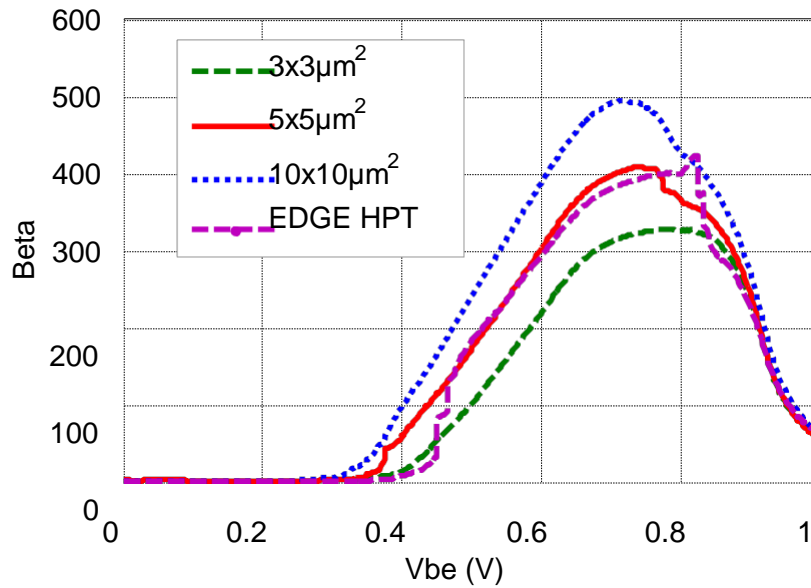
The typical Gummel curve of the HPT with  $V_{cb}=0V$  is shown in Figure 16 in the dark condition and under illumination at 850nm with a 1.14mW optical beam. At low  $V_{be}$  bias the base current saturates at around  $1\mu A$  flowing out of the base contact and the collector current  $I_c$  saturates at around  $100\mu A$ . The difference in these two currents is due to the substrate photocurrent, due to the large spot from the MMF that illuminates both the HPT and the substrate.



**Figure 16: Gummel plot of edge illuminated SiGe HPTs with 1.14mW optical beam at 850nm and without light illumination**

The current gain can be extracted either from the dark Gummel curves for  $V_{be}=0V$  to  $1V$ , or dark  $I_c$ - $V_{ce}$  curves versus base current  $I_b$ . The extracted current gain as versus base voltage,  $V_{be}$ , is presented and compared with top-side HPTs under dark conditions in Figure 17. The DC current gain has a comparable value for  $5 \times 5 \mu m^2$  top- HPT and the edge-HPT having nearly the same size, i.e  $4.5 \times 5 \mu m^2$ .

The electrical current gain for edge-HPT starts to increase from  $V_{be}=0.45V$  to reach its maximum of about 400 at  $V_{be} = 0.82V$ . The transistor amplification effect starts to reduce for  $V_{be}$  greater than  $0.82V$  due to high injection effects.



**Figure 17: Comparison of the DC current gain from the edge-HPT or top-HPTs of various optical window sizes in dark conditions.**

### ***Opto-microwave characteristics***

This section shows the opto-microwave behaviour of the edge illuminated SiGe HPT in terms of opto-microwave cut-off frequency and responsivity in PD and HPT modes of operation. The DC biasing conditions will then be optimized according to these results before performing edge mapping. The distributions of the photocurrent and opto-microwave response across the edge section of the HPT structure are then investigated at the optimum dc biasing condition that maximizes either the low frequency responsivity or the cut-off frequency.

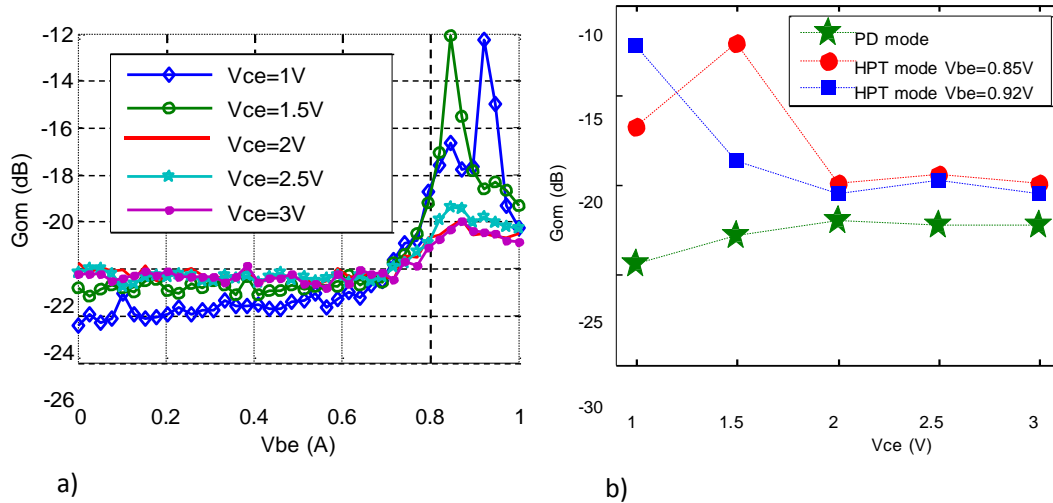
### ***Optimizing the DC bias for the opto-microwave behaviour***

We perform the analysis of the low frequency responsivity and the opto-microwave cut-off frequency of the HPT at a given arbitrarily fixed position of the optical probe with MMF. This is providing a rough evaluation of its performance. The phototransistor is operated in the forward active

mode with collector-emitter voltage ( $V_{ce}$ ) values at 1V, 1.5V, 2V, 2.5V and 3V and with the base-emitter voltage ( $V_{be}$ ) swept from 0V to 1V.

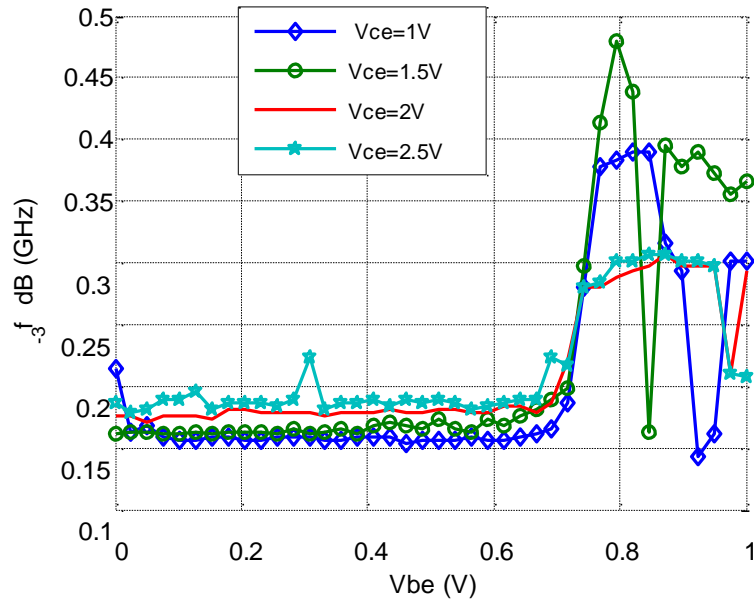
Figure 18 a) shows the low frequency opto-microwave gain of the edge illuminated SiGe HPT versus  $V_{be}$  at different  $V_{ce}$ . The position of the fiber is arbitrarily chosen in the detection range of the HPT, thus at non- optimum position. From  $V_{be}= 0V$  to 0.7V, the HPT is operated in its PD mode. The opto-microwave gain ( $G_{om}$ ),  $G_{om}$  increases above  $V_{be}=0.7V$  and eventually reaches its peak at  $V_{be}=0.85V$ , at all except except at  $V_{ce}=1V$  when the threshold is at  $V_{be}=0.92V$ . At larger  $V_{be}$  values, the fall-off of the gain is observed as the HPT is operated in a high injection regime.

The  $G_{om}$  is also shown as a function of  $V_{ce}$  in Figure 18 b) in PD mode ( $V_{be}=0V$ ) and HPT mode at  $V_{be}=0.85V$  and  $0.92V$ . In PD mode, the  $G_{om}$  slightly increases as the collector-emitter voltage increases from 1V to 3V. However, in the HPT mode, it decreases as  $V_{ce}$  increases either above 1V or 1.5V depending on  $V_{be}$  value. We can deduce an optimum  $G_{om}$  when  $V_{ce}$  is in the vicinity of 1V.



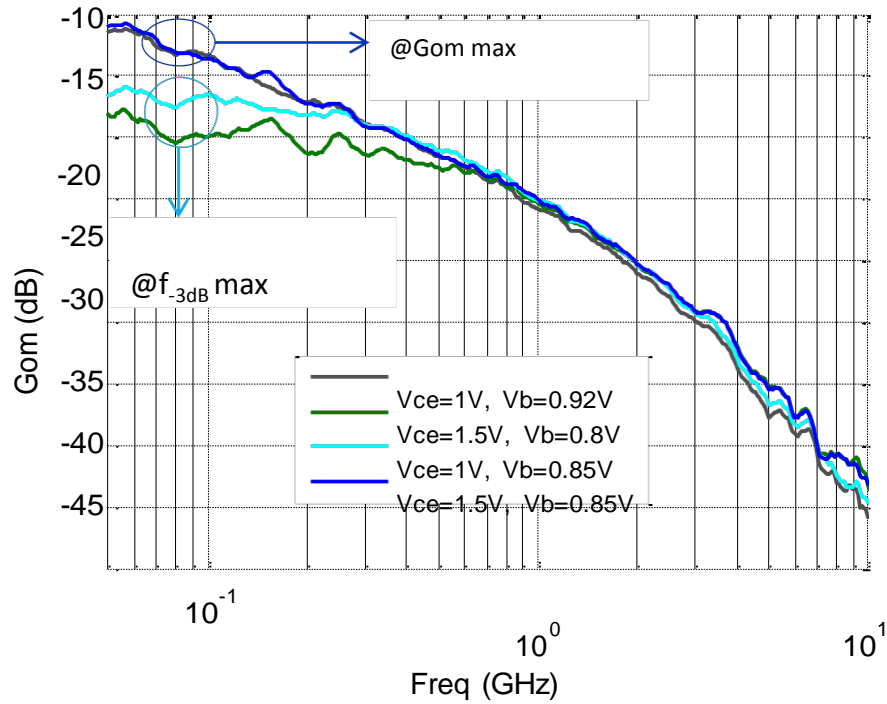
**Figure 18: Opto-microwave gain: a) versus  $V_{be}$  at different  $V_{ce}$ , b) versus  $V_{ce}$  in PD mode and HPT mode ( $V_{be}=0.85V$  and  $0.92V$ ).**

The opto-microwave cut-off frequency ( $f_{-3dB}$ ) versus  $V_{be}$ , using 50MHz as a reference for the low frequency response, is shown in Figure 19. The cut-off frequency is low and constant in the PD mode (up to  $V_{be}=0.7V$ ) and it increases to a peak around  $V_{be}= 0.8V$ . We observe a maximum cut-off frequency of 480MHz at  $V_{be}=0.8V$  and  $V_{ce}=1.5V$ . The 2<sup>nd</sup> highest value is obtained at  $V_{be}=0.85V$  and  $V_{ce}=1V$ .



**Figure 19: Cut-off frequency versus  $V_{be}$  at different  $V_{ce}$ .**

Figure 21 shows the behavior of the opto-microwave gain versus frequency at these various optimum biasing conditions.



**Figure 20: Opto-microwave gain versus frequency at low frequency  $G_{om}$  and cut-off frequency peak biasing conditions.**

## 2.6 Conclusion

In this chapter we focus on the design and description of Si or SiGe LEDs within our Telefunken GmbH SiGe Bipolar technological process. The design methodology and design approaches are presented as well as an understanding of the SiLEDs structure. The LEDs emission process and experimental validation of their optical emission is described. Three different LEDs optical sources were described in term of their device structure and mode of operations, the reverse bias and the forward bias.

The phototransistor structures have been described first with a description of the Telefunken GmbH SiGe Bipolar technological process. Opto-microwave gain, optical gain, cut-off frequency and optical transition frequency are important parameters to characterize a phototransistor. We demonstrate the first edge illuminated SiGe HPTs. It has been fabricated using the 80 GHz SiGe2RF Telefunken GmbH SiGe Bipolar technological processes, which is crucial to be implemented for ultra-low-cost silicon, based IMWP systems. Its performance in terms of DC, opto- microwave cut-off frequency and gain are presented. We have also studied the influence of the HPT physical structure through the localization of the DC and OM behaviour over the surface of the device. The substrate photocurrent distribution over the surface of the HPT is deduced from the experimental results and its effect on responsivity and speed of the HPT is extensively studied. DC characterization of the HPT involves measuring the output  $I_c$ - $V_{ce}$  characteristics of the HPT, electrical current gain ( $\beta$ ) and the Gummel measurements. The effect of illumination with optical beam at 850nm on the  $I_c$ - $V_{ce}$  curves of the HPT is presented. The dc optical current gain is isolated and compared with the electrical behaviour.

This chapter described the designed and fabrication of edge illuminated SiGe/Si HPT by using the existing SiGe RF Bipolar technology. A two-step post fabrication process was used to create an optical access on the edge through successive smooth and full dicing techniques. A low frequency opto-microwave responsivity of 0.45A/W and an opto-microwave cut-off frequency of 890MHz were measured. This phototransistor could be used in further microwave photonic applications where integration to Si Integrated Circuits (ICs) and costs are the main issues. The edge-HPT was measured through a lensed multimode fiber which was available in the lab. This was a preliminary result. This work will exploit it further attached to our designed waveguide, expecting to provide an efficient way to couple the light into the structure, improving its performances.

A successful demonstration was obtained with a forward biased SiGe/Si avalanche LED source coupled to a SiGe HPT in photodiode mode through a  $\text{Si}_3\text{N}_4/\text{SiO}_2$  optical waveguide, leading to total link budget to about -30dB, at even low power consumption rates, since only 1V and few mAs are required to operate these devices. In order to avoid complex optical packaging systems, we focus to the potential, yet lossy, use of a direct coupling via a simple lensed multimode 850nm fibre.

# CHAPTER 3: On-chip Optical Waveguides Design and links Configurations

## 3.1 Introduction

*On-chip optical waveguide link design strategies:* In this chapter, the first section presents the different optical waveguides design strategies considerations, the theoretical competency about optical waveguides with respect to modes, loss, dispersion and effect of waveguide material characteristics on these parameters especially for  $\text{Si}_3\text{N}_4$  and  $\text{SiON}$ . The three different waveguide designed are described here as well as the design strategies used. This chapter also give a brief description of the CADENCE design layout of the on-chip optical links.

The second section focuses on the R-Soft CAD software simulation of the designed waveguides (Isotropic/hemispherical source) and the possibility of the device structure layers been use as viable material for optical waveguides. The simulation results with R-soft software of the three optical waveguides designed are presented in this chapter. (1) The TEOS waveguide, (2) Silicon-Nitride ( $\text{Si}_3\text{N}_4$ ) waveguide with V-groove design and, (3) the Silicon-Nitride waveguide with narrower nitride core are presented in this chapter. The simulation results, the viability and validation of the designed waveguides are highlighted in this chapter. This chapter also presents the design waveguide simulation results and the interpretations of the simulation results.

The third section begins with the device RF substrate coupling considerations. This chapter presents the simple AC topology two ports network models of the three complete on-chip optical link device structures designed and realized, and which was simulated to verify and give possible detail parasitic oxide coupling through the substrate, as well as to predict the approximate reference signal floor level of oxide coupling for the three test structures designed.

### 3.1.1 On-chip optical waveguide link design considerations

This chapter aims at presenting the optical waveguides design strategies and procedures. In this chapter, we seek to answer the essential questions in the state of the art; 1) Optical waveguide operation at 750nm. 2) Integrate the optical source, waveguide and the detector on the same chip with no change to the technology, with layers readily available. 3) Align the core of the design waveguide to the emission point of the LED in terms of height and lateral size. The theoretical competency about optical waveguides with respect to three parameters, namely, modes, loss, dispersion and effect of waveguide material characteristics (waveguide design, the dimensions in microns, the refractive index, the width, length and height) on these parameters were investigated. The two materials,  $\text{Si}_3\text{N}_4$  and  $\text{SiON}$ , are specifically considered. This chapter also described the three different types of the designed waveguides as well as the design strategies used.

To analyse the propagation of light wave within an optical medium utilising the ray theory model or the electromagnetic wave theory model, it is necessary to take into account the refractive index of the material as well as the dimensions of the light propagation medium. For optical fibre, the ray theory model can be used to analyse light propagation in the medium because the core and cladding diameter are large enough to be modelled using ray theory ( $> 8\mu\text{m}$ ) ( $\Delta = (n_1 - n_2)/n_1$ ), but when the dimensions of the medium under consideration is too small to be modelled and analysed using ray theory, electromagnetic wave theory must be considered. Therefore, in order to obtain an accurate improved model for the propagation of light for the designed waveguides, electromagnetic wave theory is considered. The basis of the study of electromagnetic wave propagation in micro dimension medium is provided by Maxwell's equation (Cao, Vishal, Li & Xin, 2005). For a given electromagnetic wave propagation medium, the vector relationship can be written in terms of the electric field **E**, magnetic field **H**, Electric flux density **D** and magnetic flux density **B** as the curl equations: considering planar waveguides, described by rectangular Cartesian coordinates (x, y, z), and circular optical waveguide mediums, described by cylindrical polar coordinates (r,  $\phi$ , z), the Laplacian operator takes, respectively the form of equations (Eq 3.1 & Eq 3.2) (Senior, Jamro, 2009):

$$\nabla \cdot \nabla \psi = \frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} + \frac{\partial^2 \psi}{\partial z^2} \quad (\text{Eq 3.1})$$

$$\nabla \cdot \nabla \psi = \frac{1}{r^2 \sin \theta} \left[ \sin \theta \frac{\partial}{\partial r} \left( r^2 \frac{\partial \psi}{\partial r} \right) + \frac{\partial}{\partial \theta} \left( \sin \theta \frac{\partial \psi}{\partial \theta} \right) + \frac{1}{\sin \theta} \frac{\partial^2 \psi}{\partial \phi^2} \right] \quad (\text{Eq 3.2})$$

The basic solution of the wave equations (Eq 3.1 and Eq 3.2) is a sinusoidal wave, but the most important form of which is a uniform plane wave given by

$$\psi = \psi_0 \exp[\omega t - \mathbf{k} \cdot \mathbf{r}] \quad (\text{Eq 3.3})$$

Where  $\psi$  is the field (E or H),  $\omega$  is the angular frequency of the field,  $t$  is the time,  $\mathbf{k}$  is the propagation vector which gives the direction of propagation and the rate of change of phase with distance, while the component of  $\mathbf{r}$  specify the spatial coordinate point where the field is observed.

When  $\lambda$  is the optical wavelength in the medium, the magnitude of the propagation vector or the vacuum phase propagation constant  $k$  (where  $k = |\mathbf{k}|$ ) is given by:

$$k = 2\pi/\lambda \quad (\text{Eq 3.4})$$

$U$  and  $W$ , which are the eigenvalues of the waveguide core with refractive index  $n_1$  sandwich between the cladding of refractive index  $n_2$  (See Figure 13, 14&15 ) are respectively mathematically defined as:

$$U = a (n_1^2 k^2 - \beta^2)^{1/2} \quad (\text{Eq 3.5})$$

$$W = a (\beta^2 - n_2^2 k^2)^{1/2} \quad (\text{Eq 3.6})$$



Where:

$a$  = radius of the core

$k$  = phase propagation vector

$\beta$  = propagation constant value

$n_1$  = core refractive index

$n_2$  = cladding refractive index

The sum of the square of  $U$  and  $W$  defines a very useful quantity, which is usually referred to as the normalised frequency  $V$  (also called the  $V$  number) where:

$$V = (U^2 + W^2)^{1/2} = k a (n_1^2 - n_2^2)^{1/2} \quad (\text{Eq 3.7})$$

Numerical aperture (NA) is given by:  $NA = (n_1^2 - n_2^2)^{1/2}$  and also by  $NA = n_1 (2\Delta)^{1/2}$ , where  $\Delta$  is the relative refractive index difference of the medium given by  $\Delta \approx (n_1 - n_2)/n_1$ .

The normalised frequency can be expressed in terms of the numerical aperture (NA) and the relative refractive index difference ( $\Delta$ ), respectively as:

$$V = 2\pi/\lambda a (NA) \text{ OR } V = 2\pi/\lambda a n_1 (2\Delta)^{1/2} \quad (\text{Eq 3.8})$$

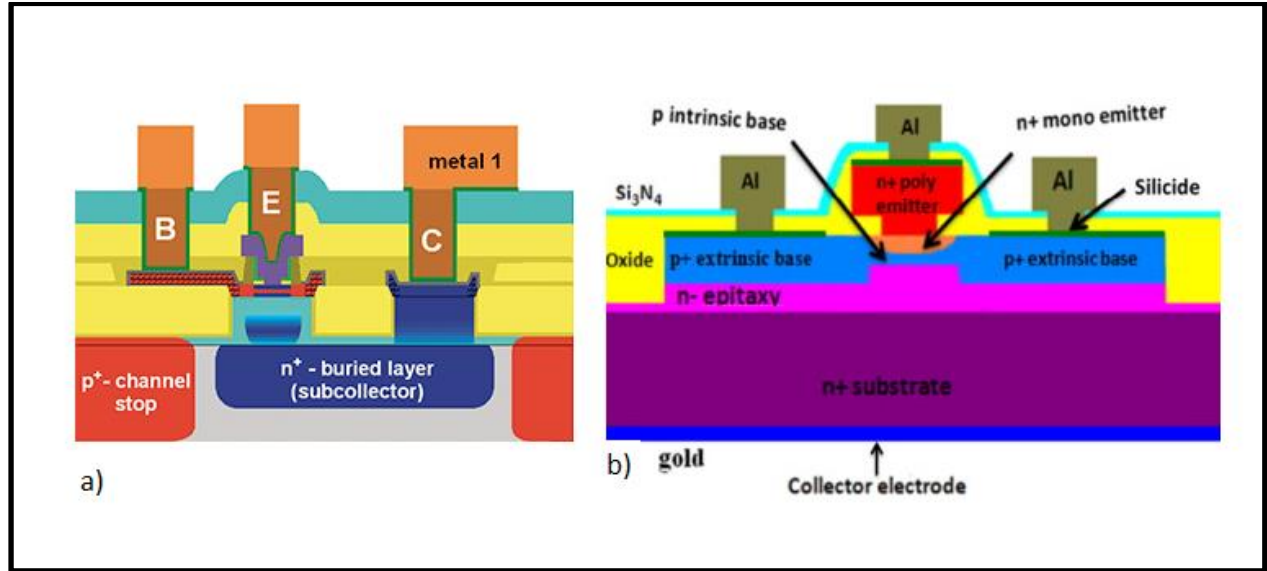
The normalised frequency is a dimensionless parameter and is often called the  $V$  number of an optical waveguide. It combines, in a very useful mathematical relationship, the information about three important design variables for waveguides: the core radius, the relative refractive index difference and the operating wavelength (Senior, Jamro, 2009).

Solving Equations (3.5) and (3.6) allows the eigenvalue  $U$ , and hence  $\beta$  to be calculated as a function of the normalised frequency. In this way the light wave propagation characteristics of the various modes, and their dependence on the optical wavelength and the waveguide parameters, can be determined i.e  $V$  reference (normalised frequency).  $V$  reference for step index single mode optical waveguide is 2.405 (Senior, Jamro, 2009).

In the fabrication of the optical links using a Telefunken GmbH SiGe Bipolar technological process without the addition of masks and processing steps was implemented. We only modify layout geometries in order to create an optical window opening. This approach ensures a straight compatibility with SiGe circuits on the same chip, and makes the SiGe HPTs directly integrated into an industrial foundry.

The Telefunken SiGe2-RF Bipolar Silicon Germanium process technology exhibits  $f_T$  up to 80GHz and  $f_{max}$  up to 90GHz. This makes this technology able to provide circuits working above 10GHz and potentially up to 60 GHz in some configuration. This RF bipolar technology allows the production of wafers with

applications in high performance standard RF devices used in various applications . This process technology also offers PNP transistors, diodes (PN, Zener, ESD, Varactor and Schottky) and passive devices such as inductors capacitors and resistors. Between the LED source and the Si/SiGe detector, there are different nitride and oxides layers of the technology normally used as isolations purposes as shown in Figure 22.



**Figure 21: Schematic cross Section of a SiGe2 NPN HPT**

Based on our innovative optical waveguide design, we have taken advantage of these different oxide layers of the technology to design the waveguides. The designed waveguide will be implemented in a full on-chip optical links presented in chapter 4. The design and development of an efficient Silicon based waveguide at submicron wavelengths presents major challenges, particularly due to higher absorption and scattering effects at short wavelengths. We have hence extensively designed and studied three different waveguide structures in terms of layout structures, the simulations and the characterization of the waveguides.

Based on the above mathematical equations and coupled with the initial design preamble hypothesis (that light wave propagates in Silicon-Nitride waveguide transparent at 750nm wavelength), we begin by designing a multimode waveguide in micron scale as well as a single mode optical waveguides in micron scale as tabulated in Table 3.

Using equation 3.8 and coupled with the consideration of optical properties of the various semiconductor materials, the design strategy and techniques used, the V numbers for the different designed optical waveguides were approximately mathematically determined.

**Table 3: Optical wave guiding on structures**

SAMPLE TEST NUMBER	WAVELENGTH (μm)	BACKGROUND INDEX (μm)	RELATIVE REFRACTIVE INDEX ( $\Delta n = (n_1 - n_2)/n_1$ )	CORE DIAMETER R (μm)	WAVEGUIDE LENGTH (μm)	DIMENSION (μm)	NORMALIZED FREQUENCY (V-number)	DESIGN PURPOSES COMMENTS
1	0.75	$n_1 = 2.4$ $n_2 = 1.45$	0.39	1	10	1x10	17	Multimode, With medium loss
2	0.75	$n_1 = 3.5$ $n_2 = 1.45$	0.58	1	20	1x10	32	Multimode, Moderate loss
3	0.75	$n_1 = 1.48$ $n_2 = 1.46$	0.01	1	30	0.2x2	2.03	Single mode, low loss
4	0.75	$n_1 = 2.02$ $n_2 = 1.45$	0.28	0.1	50	0.2x2	1.26	Single mode, Very low loss
5	0.75	$n_1 = 2.02$ $n_2 = 1.45$	0.28	0.02	100	0.2x2	0.252	Single mode, Optimum waveguide, Extremely low loss

Figure 23 represents the first waveguide schematic designed (OWGD1); we used the different refractive indices as created by different densification values of the different TEOS plasma deposited on the oxide layers. It is generally known that low temperature processed TEOS layers has a refractive index of 1.42 at 750nm while more densified and rapid thermally annealed layers has a refractive index of 1.46. In this design, the (TEOS 2) layer with  $n_1 = 1.48$  was subjected to rapid thermal annealing after deposition of this layer followed by deposition of (TEOS 1) layer with  $n_2 = 1.45$  without rapid thermal annealing. This technology offers the ideal route to realise single mode waveguides, which are transparent from 450nm to 850nm wavelength. The typical layers thickness as offered by the SiGe 0.35 micron RF bipolar process procedures was used during our design. The side termination of the waveguide was facilitated by an RF etch of all the oxide layers down to the silicon substrate interface, by using the B Pad or Test pad definition of the process. This minimises the lateral RF parasitic capacitive couplings into the surrounding oxide layers, which might arise when modulating the optical source with AC signal.

Figure 24 shows a schematic of the second waveguide designed (OWGD2), where vertical slots were predefined by a poly silicon window definition as offered by the SiGe 0.35-micron RF bipolar process. This offers a 45 degree slanting of the TEOS1 oxide with  $n_1 = 1.46$ , before the deposition of the Silicon-Nitride layer ( $\text{Si}_3\text{N}_4$ ) with  $n_2 = 2.02$ . By tailor designing the dimensions of the various layers in the waveguide, a V-shaped waveguide profile was hence constructed. This enables vertical lowering of the higher index core of the waveguide vertically in the silicon insulating layers, which facilitates a better vertical alignment of the core of the waveguide with the light emission spot of the optical source, in the source pillar structure.

Figure 25 shows the waveguide structure side view and cross-sectional view of our third waveguide designed (OWGD3). In this design, we make use of the capacitor definition as made available by the process. One mask in the process facilitates the nitride deposition of 850nm thickness. No poly-silicon or metal over-layers were defined in the layouts; only a thin nitride layer was embedded in the surrounding layers of TEOS oxide. Since the refractive index of Si nitride are generally of the order of 2.04 at 650 - 850nm wavelength, again, with this technique, various multimode (wider core) and narrower core (single mode) waveguides can be designed and realised.

### 3.1.2 The three different waveguide structures designed

This section discusses the design of Silicon-Nitride based optical waveguides using a SiGe RF process. From our analysis, it shows that both Silicon-Nitride and Silicon-Oxi-Nitride offer good possibilities for transmitting radiation at low loss in the wavelength regime 650-850nm. Both  $\text{Si}_3\text{ON}_3$  and  $\text{Si}_3\text{N}_4$  offers high refractive index of 1.60 - 1.95 and 2.02 - 2.40 respectively, against a background of available  $\text{SiO}_2$  as cladding or background refractive index layers in silicon CMOS (Figure 22). The analytical results of optical transparency on  $\text{Si}_3\text{N}_4$  by [123] show that a tail-off of absorption from the shorter wavelengths towards the higher wavelengths, viz: high loss characteristics of  $4.3\text{dB.cm}^{-1}$  at 530nm versus only about  $1\text{dB.cm}^{-1}$  at 650nm and  $0.1\text{dB.cm}^{-1}$  loss at 750nm.

In our design, we utilized a  $0.35\mu\text{m}$  RF bipolar process as generally available for the manufacturing and fabrication of RF cell phone component. The process offered a pillar/columnar npn epi-layer structures which could be isolated laterally by means of various oxides as TEOS layers.

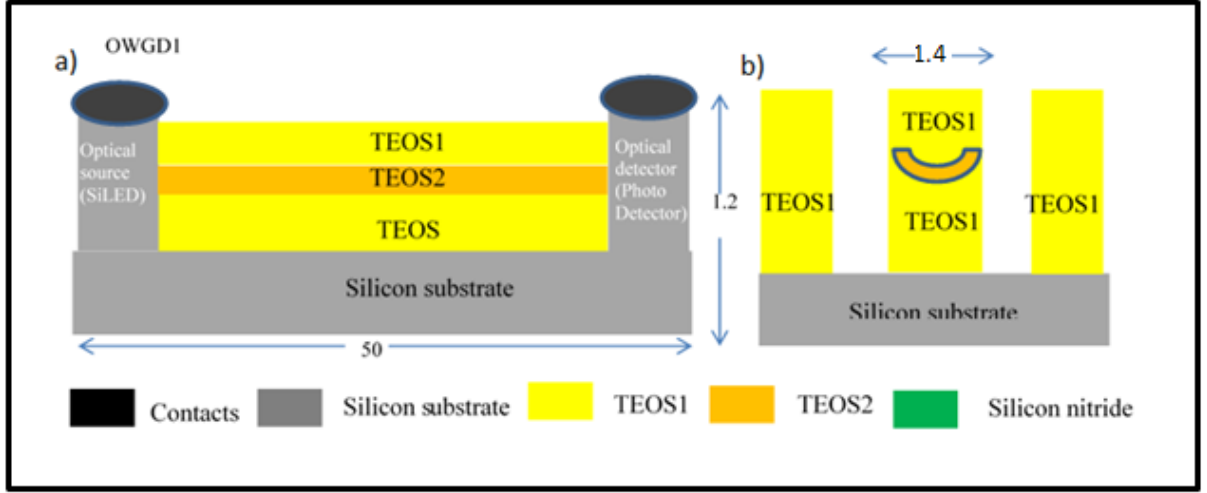
The design and development of efficient waveguides at submicron wavelength offered major challenges, particularly due to designing and alleged higher absorption and scattering effects at the shorter wavelengths (Gorin *et al*, 2008). We have hence extensively focused on simulating our various waveguide designs before that fabrication of the device was implemented.

Figure 23 shows schematic details of our first optical link structure design:

- In the first designed test structure 1 (OWGD1) in Figure 23 (a) and (b), the waveguide structure was placed in the outer over layers of the plasma deposit layers. A channel crevice were etched in the TEOS 1 over layers ( $n = 1.46$ ) and then filled with a second TEOS 2 layer. This layer was then densified by a thermal process, thereby increasing its refractive index to about 1.48. A V-shaped waveguide cross-section as defined by built-in processing procedures was chosen in order to ensure the highest radiation coupling of the optical source into the waveguide laterally, which is of submicron dimension and spherical in nature, and which was positioned slightly under subsurface of the surface of the optical source columnar structure.

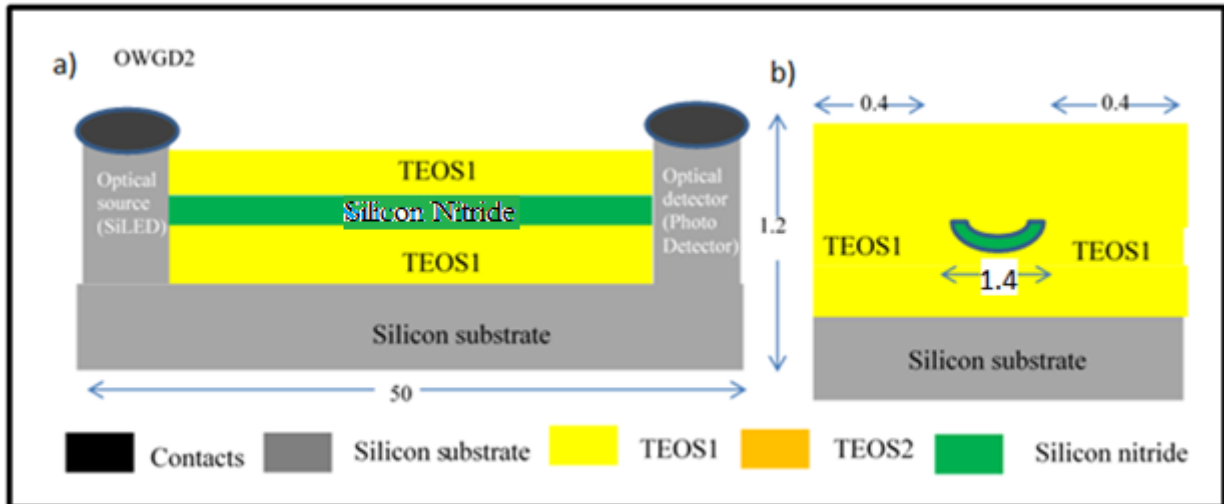
RF process slots were etched both sides during the design using standard process design parameters, in order to ensure lateral optical and wave guiding confinement of the optical radiation within the

TEOS2 core material. The dimensions of all structures were designed to be in the micron cube range. Detailed dimensions are given in Figure 23. In this waveguide, the optical wave light from the source propagating at 750 nm wavelength is presumed to propagate entirely within the confined and isolated optical link structure, with the middle TEOS 2 layer denser in refractive index, confining the optical wave light propagation presumably to the surface of the structure.



**Figure 22: Waveguide structure (a) Side view section (b) Cross-sectional view**

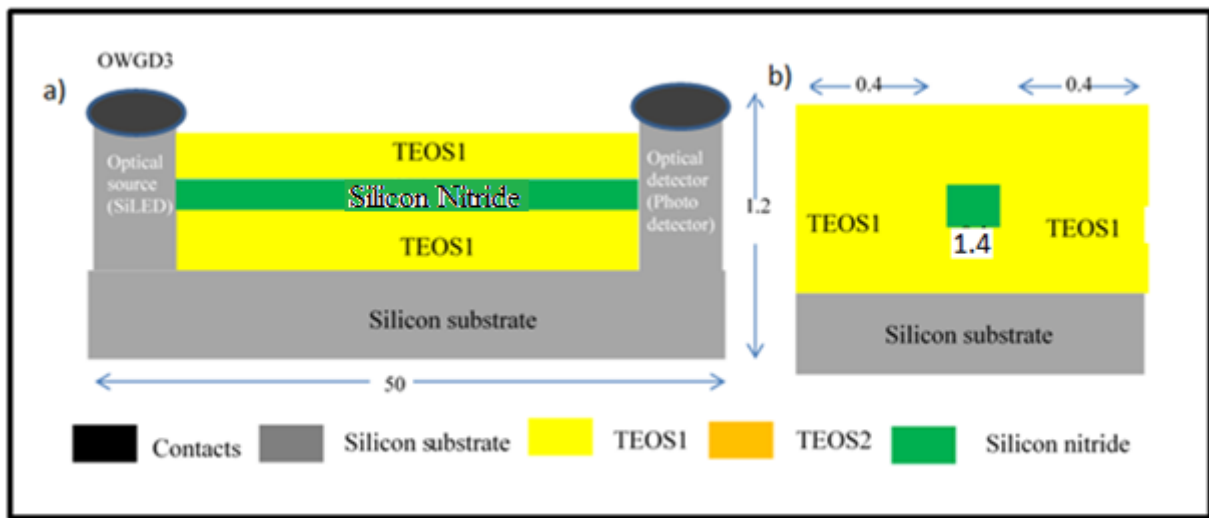
- In the second design, test structure 2 (OWGD2) in Figure 24 (a) and (b), the etched crevice of 0.4 micron in the first TEOS layer is filled up with a Silicon-Nitride over layer, followed by further chemical vapour deposition (CVD) deposited TEOS 1 oxide over-layers. Hence a high refractive index core Silicon-Nitride of refractive index  $n = 2.4$  is formed with a surrounding oxide index of  $n = 1.46$ .



**Figure 23: Waveguide structure for design 2 (a) Side view section (b) Cross-sectional view**

- In the third design test structure 3, (OWGD3) as in Figure 25 (a) and (b), the lateral width of the Silicon-Nitride layer is reduced to about 0.4 micron in order to form a narrow and higher index core, which would enable a less multi-mode propagation and more single mode propagation, with lower optical pulse dispersion of the optical radiation from the source and coupled through the waveguide to the detector.

In other words, the lateral width of the Silicon-Nitride layer is reduced to about 0.4 micron in order to form a narrow higher refractive index Silicon-Nitride core ( $n=2.40$ ), which would enable a less multi-mode propagation, best and optimized single mode propagation and lower dispersion of the optical radiation from the source through the waveguide to the detector, and about 30% of the optical energy actually propagating outside the waveguide core.



**Figure 24: Waveguide structure for design 3 (a) Side view section (b) Cross-sectional view**

Based on the above design analysis, therefore, we suggest that compromises could be made with respect to choice of operating wavelength, anticipated waveguide loss and detection efficiency utilizing CMOS technology as a basis. At shorter wavelengths both Silicon-Nitride and silicon oxo-nitride reveals higher absorption coefficients with good efficiency with respect to silicon detectors in small space volume detection possibilities, while longer wavelengths reveals lower loss transmission but with less efficiency in detection in silicon detectors per unit space volume of silicon.

Especially the transparency of silicon-nitride based waveguide at 750nm-850nm offers remarkable possibilities with regard to the integration of optical communication links, data transfer and photonic systems directly into CMOS integrated circuitry.

*Particularly, what is attractive about the technology is the anticipated cost effectiveness and low levels of complexity in the designed technology as compared to the incorporation of groups III-V, or hybrid III-V and silicon technology into CMOS technology.*

### 3.2 Design of full Silicon Complete On-Chip Optical Links

A 0.35 micron bipolar SiGe technology process was used as utilised in typical state-of-the-art mobile cell phone technology.

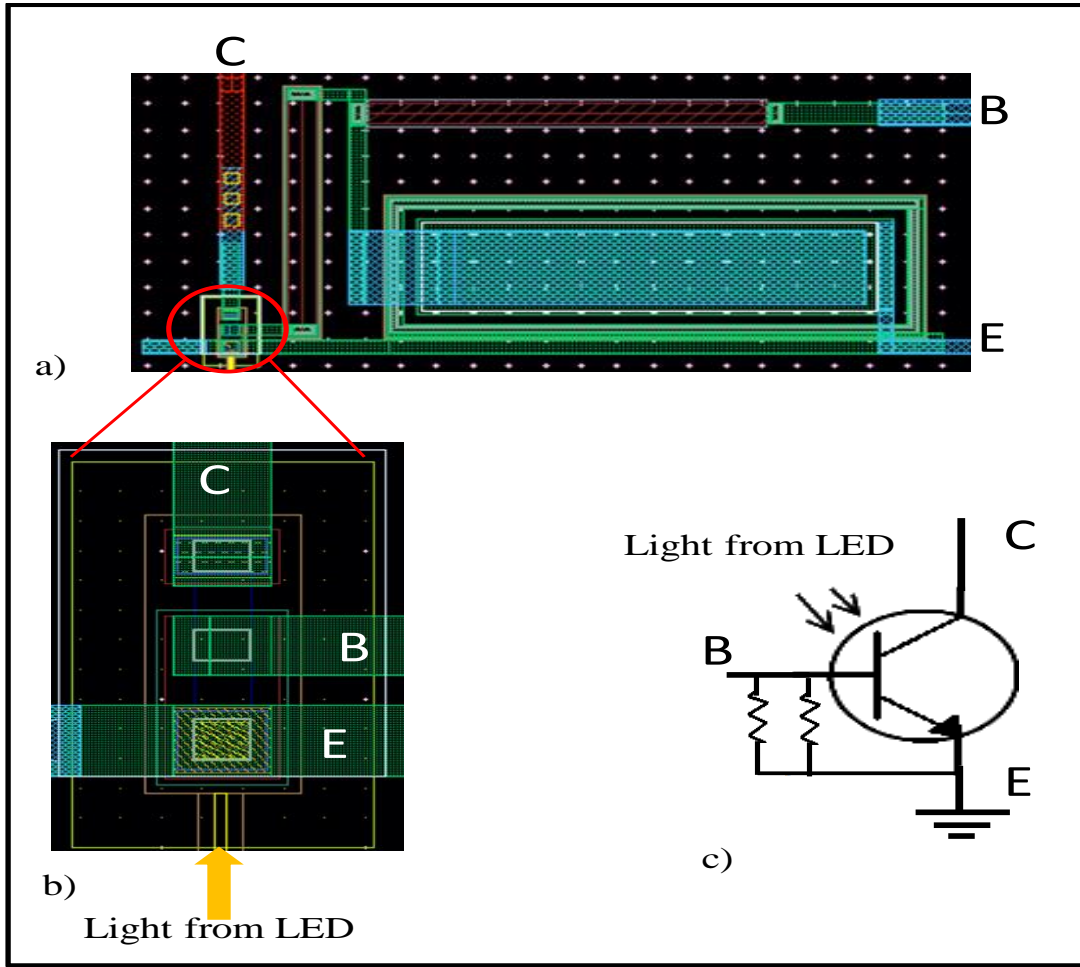
Figure 26 illustrates the basic block schematic design concept, utilising the structural features as offered by the 0.35 $\mu\text{m}$  RF bipolar process. The specific process was used to realise specific isolated columnar structures for both the Si Av LED optical source as well as for the SiGe detector. The isolation TEOS layers, as is usually used for RF isolation purposes between the RF active components, were then used as building blocks to realize optical wave-guiding structures between the optical sources and the detectors. The whole structure was realised on a silicon substrate of very high resistivity (500 M $\Omega$ ). Channel doping layers were used to contact bottom layers of the detectors and micron-dimensioned metal contacts were used to access topmost device regions, including Ge-based doped layers used for a SiGe phototransistor design with high internal gain.

#### 3.2.1 Complete Design of On-Chip Optical Links

Figure 27 illustrates the design concept of on-chip optical links making use of the features as offered by the SiGe2RF Telefunken GmbH technological process. Three different combinations of optical source, waveguide and detector are chosen by considering the technological process and theories behind the first study (see Figure 27 a) to c)).

The full optical link is composed of silicon-based optical sources, waveguide and detector as described below:

- **On the sources side:** We implement three different Si or SiGe LEDs described in the previous chapter.
- **On the detector side:** The detector is chosen to be an edge SiGe HPT biased in a photodiode mode where the emitter and the base are short-circuited through the capacitor and grounded as shown in Figure 26. The capacitance is actually short-circuited as the insulator is not used in between the electrodes of the capacitor, in this specific run, and thus it results two parallel resistances of 50  $\Omega$  as shown in Figure 26 c). The light is injected through the edge of the HPT and the emitter metal is deposited all over the emitter. The SiGe HPT has a width of 2.4 $\mu\text{m}$  and a length of 2.2 $\mu\text{m}$ . The base-collector regions are reversed biased to separate the photo-generated electron-hole pairs.



**Figure 25:** The schematic of the detector used at the receiver side of the full optical link.

- **Optical waveguide:** The isolation TEOS layers (usually used for RF isolation purposes between RF active components), the poly-Silicon layers and nitride layers are then used as building blocks to obtain optical wave-guiding structures between the optical sources and the detectors. Three different topologies of waveguides (OWGD1, OWGD2 and OWGD3) are envisaged as presented in Chapter 3 section 3.1.2.

In overall, there are 3 different possible sources and 3 different waveguides, which make 9 possible combinations. According to the following table and Figure 27, only three combinations were fabricated to respect our chip surface limitations (area available for the run). Additional combinations could have been possible to vary the alignment position of the waveguide to the optical source.



Table 4: The possible combination of the on-chip full optical link.

LEDs	Optical waveguide		
	OWGD1	OWGD2	OWGD3
Si Av N <sup>+</sup> NP <sup>+</sup> columnnar	<b>Test structure 1 (OLTS1)</b>	x	x
SiGe-N+PN LED with collector contact	x	<b>Test structure 2 (OLTS2)</b>	x
SiGe-N+P LED without collector contact	x	x	<b>Test structure 3 (OLTS3)</b>

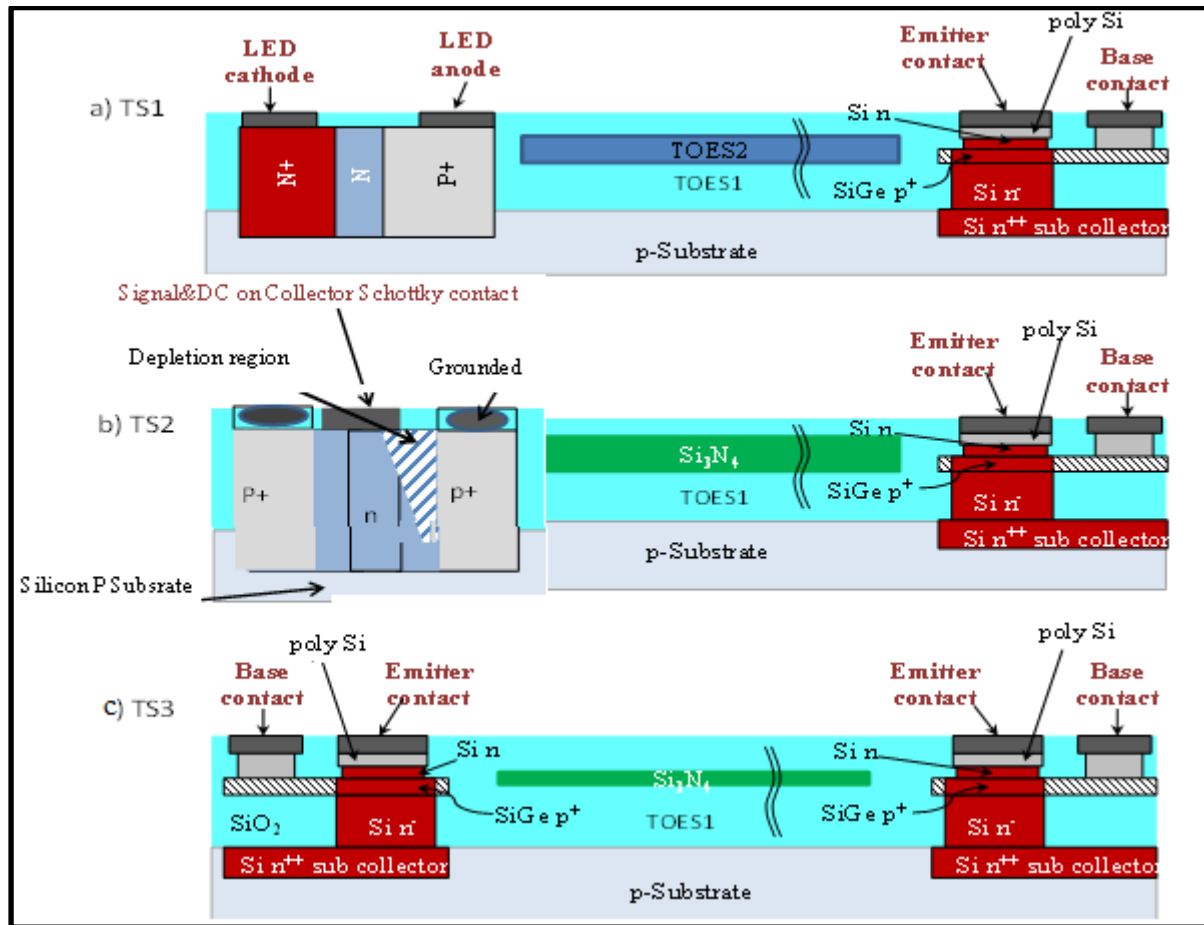


Figure 26: Basic designs of the optical links using Si and SiGe Av LED, waveguides and SiGe-based detectors with a) Design test structure 1 (OLTS1), b) Design test structure 2 (OLTS2) and c) Design test structure 3 (OLTS3).

### 3.2.2 Optical link test structure 1 (OLTS1)

In the first design optical link test structure 1 (OLTS1), as shown in Figure 27 (a), on the source side, an  $n^+-n$   $p^+$  columnar structure was designed that was located laterally on the semi-insulating substrate. A similar structure was used to realise an integrated phototransistor structure with a Ge doped base, the detector side was made of a SiGe HPT as described in chapter 2. Here, we implemented waveguide (OWGD1) in this structure. The columnar structures were all of micron dimension, such that the structures were composed of  $1\mu\text{m}$  cube substructures. The regions are doped as indicated in Figure 27 (a). The regions were appropriately electrically contacted during experimental measurements on the fabricated device in order to reverse bias the first  $p^+n$  junction. Upon reverse biasing, the depletion region penetrates through to the  $n^+$  region in order to strengthen and unified the electric field in the lowly doped  $n$  region. From our previous experience gained from previously designed devices, we know that the light emission would occur near the surface region of the middle  $n$  region and extend more or less laterally across the whole region. The region between the Si Av LED source and SiGe detector were filled with normal TEOS plasma deposited oxide as part of the available process procedure.

In this section, the specific processes, including deposition of several different thicknesses of TEOS layers is discussed. One middle layer was subjected to a rapid thermal annealing process, also part of the normal process. This would cause a densification of the oxide and change the refractive index from 1.46 to 1.48. The middle layer was subsequently interfaced laterally to the optical light emission region, and the waveguide implemented here was (OWGD1)) designed as in Figure 22. Appropriate air slots were made on the sides of the waveguide in order to minimise laterally induced oxide parasitic capacitance. On the detector side, a SiGe Heterojunction Bipolar Transistor (HBT) is selected with a width of  $5\mu\text{m}$  and a length of  $1.2\mu\text{m}$ . Its transition frequency was found to be about 80GHz. The Base-collector regions for the photo detector are reversed biased to separate the photo-generated electron-hole pairs. The base emitter junction is short-circuited with a  $50\Omega$  load resistor so as to operate in the photodiode mode, in other to simplify initial detector measurements and to maximise the operating bandwidth, at the expense of reduced responsivity.

### 3.2.3 Optical link test structure 2 (OLTS2)

In our second test structure 2 (OLTS2) shown in Figure 27 (b), the same basic lateral columnar structure was used as in OLTS1, but a rectangular Schottky contact of Aluminium on  $n$ -Silicon was fabricated in the columnar structure middle lowly doped  $n$  region on the optical source side. The two  $p^+$  columnar regions were grounded as required by the RF probe bias during measurement process, and the DC and modulation signal was applied on the Schottky contact. Here we implemented waveguide (OWGD2) in this structure. Positive voltage bias placed the Schottky contact in forward bias mode and caused a triangular depletion

region towards the  $p^+$  region of the LED optical source, reverse biasing the  $p^+n$  region. This configuration drastically reduces the total depletion region volume and hence reduces depletion layer capacitance. The elongated and uniform electric field region and its associated minimized capacitance would hence enable ultra-high modulation frequencies. Since small dimensions were used and the light emission processes are impact ionisation and avalanche related aid, calculations show that modulation frequency of up to 300GHz could potentially be reached with this type of designed configuration. A V-shaped groove Silicon-Nitride waveguide design (OWGD2) shown in Figure 24 was used in this design, in order to optimise coupling of light from a circular and spherical nature acceptance angle, and to improve optical coupling with the micron dimensioned emissions from the Si Av LED. The same detector structure design as in OLTS1 was used in this second optical link.

### **3.2.4 Optical link test structure 3 (OLTS3)**

In a third design test structure 3 (OLTS3-RB) shown in Figure 27 (c), a vertical cubical columnar HPT structure like in geometry was used for both the optical source as well as for the detector. Here we implemented waveguide (OWGD3) in this structure. The SiGe emitter/base region presenting the same structuring was used for the optical detection. SiGe p-n junction was placed in reverse bias and biased in avalanche regime, into avalanche mode during measurement process. Since the SiGe structure of this nature has a transition frequency of up to 80GHz, it can be assumed that the reverse bias base-collector junction, when placed in avalanche reverse bias mode, could attain similar transfer frequencies with optical emissions following this modulation frequency. The Silicon-Nitride optical waveguide implemented here was similar as in OLTS2, but the Silicon-Nitride layer lateral thickness was strategically reduced in lateral width dimension of  $0.4\mu\text{m}$  as in Figure 23, so as to reduce the waveguide core size and enable less modal dispersion in the waveguide.

### **3.2.5 Optical link test structure 3 (OLTS3-FB)**

A fourth test structure (OLTS3-FB), similar to OLTS3 structure, was used as in Figure 27 (c). The biasing configurations was however changed, the SiGe junction was placed in a forward bias mode, with positive bias applied to the  $p^+$  SiGe base region. Electrons were injected from the n collector region and the carriers were energized through conduction transfer through the low doped n region of the collector. When these carriers are injected in the SiGe base region, they would supposedly contain enough energy in order to then transfer electrons from the L valley to the T band structure valley of SiGe. With 20% Germanium doping, the emitted wavelength for this design was predicted to be about 850 nm. The very small columnar conduction region would reduce depletion layer capacitance and the carrier's transit time in the device.

### 3.3 Design Layouts of the On-Chip Optical Links Devices

A total of 12 optical link device layouts were designed, we only present here the three layouts that were highlighted earlier and which revealed and give close indications of the best expected results of the links designed.

The three Cadence *Virtuoso Layout* of the devices out of our twelve complete optical link devices as realised in optical die 3 are presented in Figure 27, 28 and 29.

Figure 27, shows the top layer view layout of our design structure 1(OLTS1) with the corresponding dimensions in  $\mu\text{m}$ .

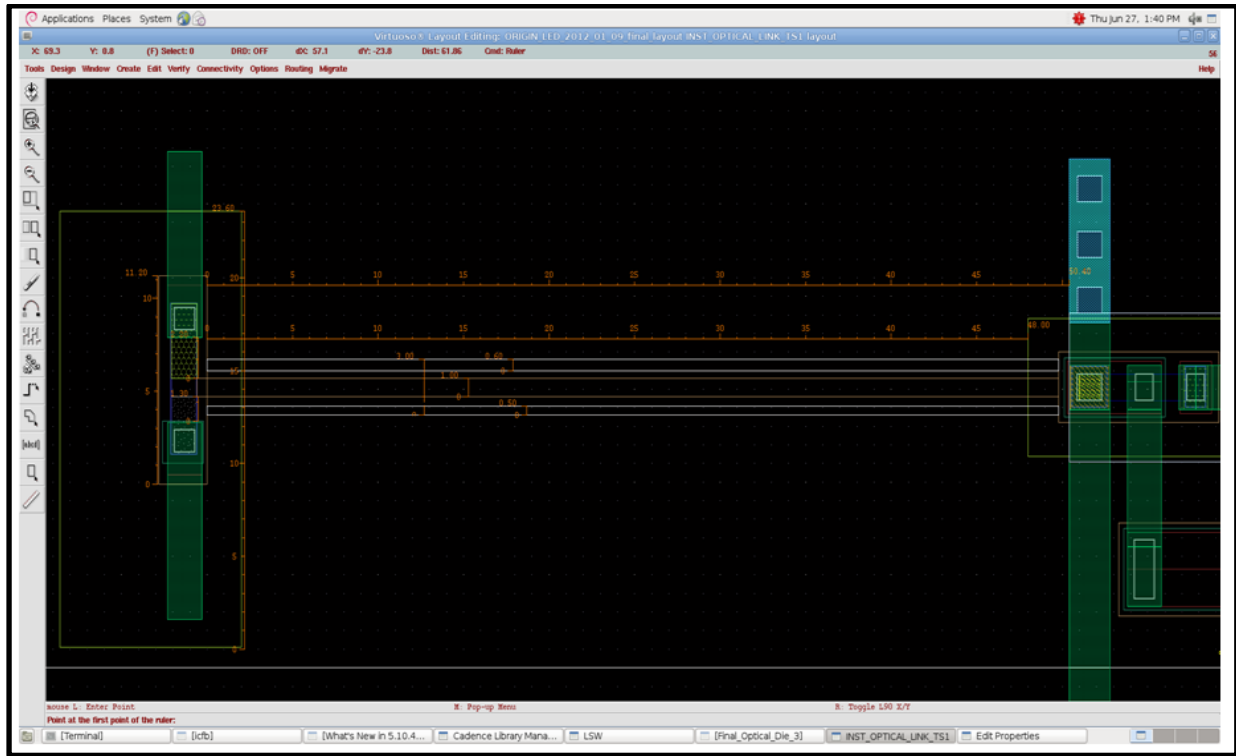
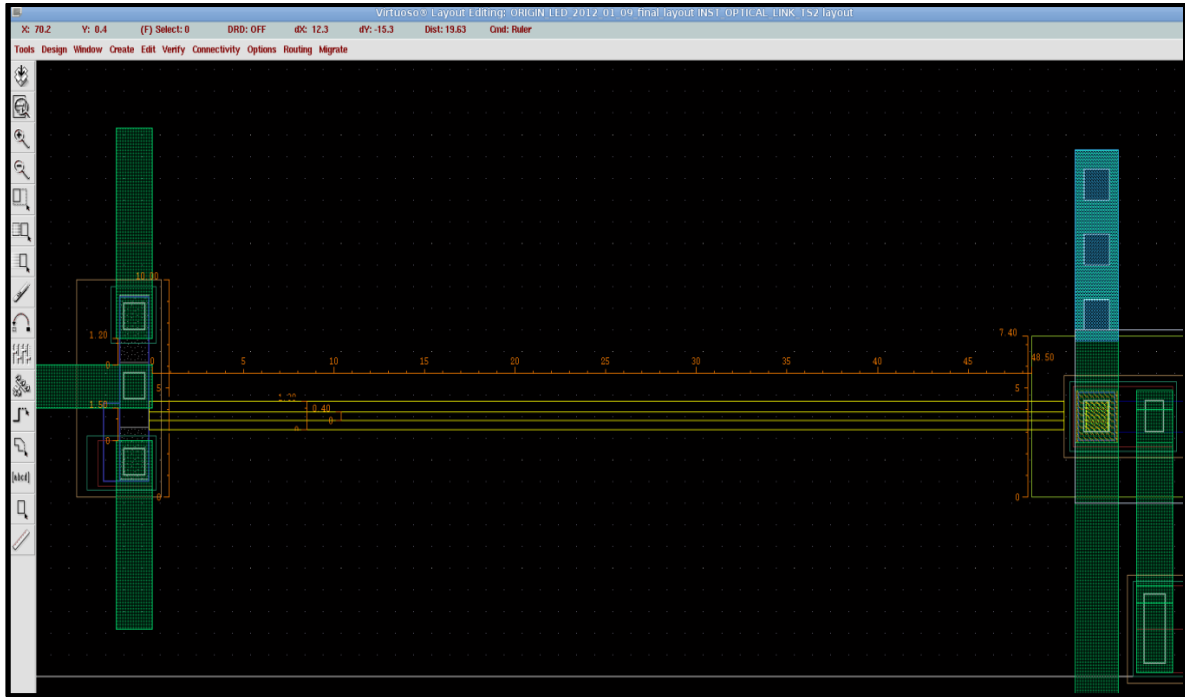


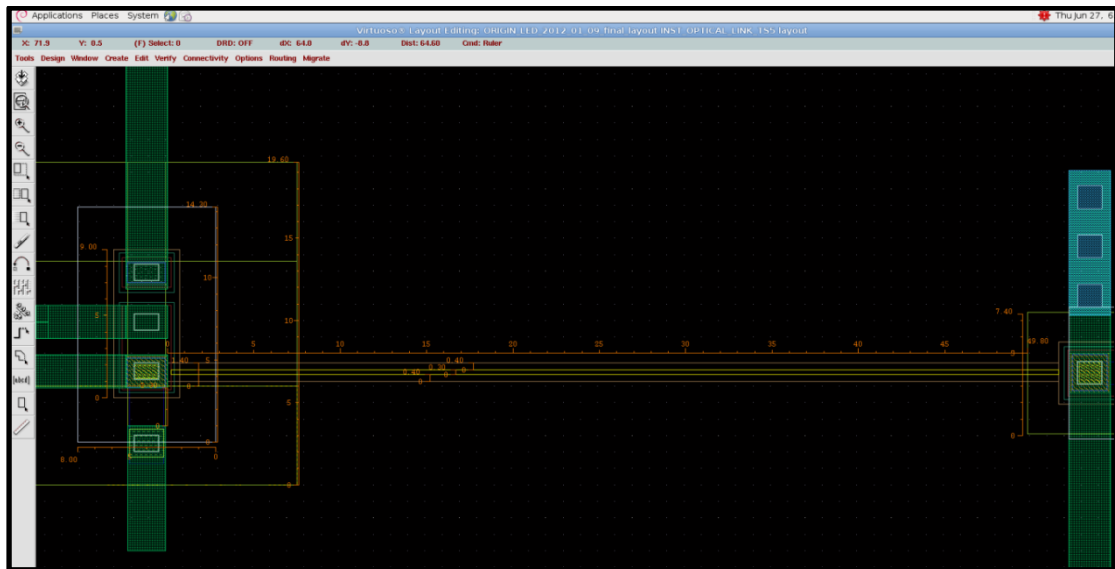
Figure 27: Top view test structure 1 circuitry layout (OLTS1)

Figure 28 shows the top layer view layout of our design structure 2 (OLTS2) with the corresponding dimensions in micron. The yellow lines from the source to the detector are representing designed Silicon-Nitride waveguide. In this design, an etched crevice of 0.4 micron in the TEOS 1 layer was filled up with a Silicon-Nitride over layer, followed by further CVD deposited TEOS 1 oxide over layers. A high refractive index of 2.40 Silicon-Nitride waveguide core was formed with a surrounding TEOS layer of refractive index of 1.46. This allowed optical propagation through the Silicon-Nitride core due to Snell law of light refraction and theoretical wave guiding concepts as outlined earlier.



**Figure 28: Top view test structure 2 circuitry layout (OLTS2)**








Figure 29 shows the top layer view layout of our design structure 3 (OLTS3) with the corresponding dimensions in micron. In this design structure 3 (OLTS3), the lateral width of the Silicon-Nitride layer was reduced to about 0.3 micron in order to form a narrow, higher refractive index Silicon-Nitride core ( $n=2.40$ ), which would enable a best and optimized single mode propagation and lower dispersion of the optical radiation from the source through the waveguide to the detector, and about 30% of the optical energy actually propagate outside the Silicon-Nitride waveguide core in this design.



**Figure 29: Top view test structure 3 circuitry layout (OLTS3)**

Table 5 relates the approximate colour coded index to specific structure layers: It gives a brief list of the visible top layer structures; many other layers that were also used are not listed here for nondisclosure confidential reasons. The table is just a colour coded list of the different layers for understanding the optical link structure's purposes.

**Table 5: Layers colour coded index**

Colour Index	Structure Name	Structure Descriptions	Mask Number
	L10_m1	Metal 1	M70
	L20_m2	Metal 2	M71
	L17_nit	Nitride capacitor	M77
	L15_nit	Nitride	M75
	L34_poly1	Poly-window defined	L36
	L2_cs	P <sup>+</sup> channel stop	M20
	L35_iso	TEOS oxide 1	M35

In the schematic presentations, the columnar source and detector are actually 90 degree rotated with respect to waveguide. See Cadence for real layouts in Figure 27, 28 and 29 respectively.

### 3.4 R-SOFT CAD Software Simulation of the Designed Waveguides

R-Soft CAD is the core program in the R-Soft Photonics Suite, and acts as a control program for R-Soft's passive device simulation modules, such as BeamPROP, FullWAVE, BandSOLVE, GratingMOD, DiffractMOD, FemSIM, and ModePROP. It is used to define the most important input required by these simulation modules, i.e.; the material properties and structural geometry of a photonic device.

The R-Soft CAD is the main control program for a series of these simulation modules of which BeamPROP is one of the simulation modules. BeamPROP is a simulation engine used for the design of integrated and fiber-optic waveguide devices and circuits. It incorporates advanced finite-difference beam propagation method (BPM) techniques for simulation.

We used this advanced simulation software to further simulate our design waveguides; we used advanced optical simulation software (R-SOFT Beam-PROP and R-SOFT FULL WAVE) to simulate our specific CMOS based waveguide structures operating at 750nm wavelength and using all the materials properties, the structural geometry of our device waveguides, the dimensions and the processing variable parameters. The simulation tool was performed in 3D simulation mode [124].

An important parameter of the optical signal propagating in micro-optical waveguide is the loss propagation efficiency and modal dispersion. Simulation and optimization can be conducted on these parameters. The simulation of light propagation in arbitrary waveguide structures was the first step to understand the light transmission effect on the waveguide structures. The simulation did not only give an insight and a start point in evaluating the performances of the proposed design waveguides before the fabrication, but it also allows waveguide parameters optimization. Unfortunately, the simulation was performed in a quasi-ideal environment, so it was very difficult to take into account all parameters and their effects on a real waveguide; The effective implementation and characterisation of the waveguide structure were included, when possible, to validate the simulation results. Another demerit is the simulation time, which imposes certain approximations.

In this section, we are concerned with the study and simulation of the three proposed waveguides, and we aim to see the viability and effectiveness of the waveguides been used as an optical waveguide in micro-optical link at 750nm wavelength. Our goal was to simulate a simple optical waveguide coupling light wave from the optical source through the waveguide to the detector.

Since the BeamPROP solves for the electromagnetic fields within a given structure and within a computational domain on a spatial grid, it is important to define this grid properly to ensure correct simulation results. It is also critical to perform a convergence study on the X, Y and Z grid sizes to optimise the trade-off between simulation time speed and accuracy. To perform this convergence study, we used the scanning capabilities of MOST, of RSoft's scanning and optimisation tool. The scanned results show, as expected, that as the grid size decreases the simulation results converges to a particular solution but increases simulation time speed.

Firstly, the grid size for X, Y and Z was chosen to be  $0.125\mu\text{m}$  providing a good compromise between convergence and simulation time after series of pre-testing the simulation of the designed optical waveguides.

Secondly, another defined parameter was the boundary conditions, which define how the E-field behaves at the boundaries of the selected domain. By default, we used the option Full Transparent Boundary Conditions (TBC). This type of boundary is designed to let radiation pass through the boundary without reflecting back into the simulation domain.

BeamPROP includes many other simulation condition options that control how polarisation is handled, including scalar calculations, Transverse Electric (TE), Transverse Magnetic (TM), quasi-TE, quasi-TM, semi-vector, and full-vector options. To get the most accurate results, we decided to use the full vectorial method, which recognises that the electric field  $E$  is a vector, and starting the derivation from the vector

wave equation rather than the scalar *Helmholtz equation*. On the polarisation field side, we used TE which determines the polarisation of the major component used in the beam propagation calculation (Ex).

Thirdly, the definition of the launch field is another important parameter which defines the initial condition for the simulation. The launch field can be seen as the input excitation mainly characterised by the desired field profile. The goal is to provide the optical waveguide modes coming out of the 50  $\mu\text{m}$  core Multimode (MM) waveguide or Single mode (SM) waveguide. Therefore, two options were exploited here: we use the fundamental mode and another option is the use of all the modes of the waveguide, equally distributed, to study the multimode behaviour.

In the latter option, the input field is a superposition of all waveguide (3D) modes supported by the input component with equal power in each mode and a random phase for each mode.

Fourthly, monitoring and the analysis of simulation results were the last consideration on the simulation setting's setup. Since we want to analyse the optical power propagating through the waveguide, pathway monitor definition is needed for BeamPROP to calculate the steady-state optical field throughout an entire design files parameters. It is recommended and useful to analyse this field in standard physical quantities such as the optical power in a particular region of the circuit or the power traveling in a particular mode. Pathway monitors are what makes these types of measurements possible.

Lastly, simulation results were given as a function of the propagation direction Z and are measured along a pathway. Monitors can be used to measure the power in the propagating field via overlap integrals or power integrals, to measure the phase of a propagating field relative to a test field, and measure other output such as spot size. We used the option 'partial power', which computes the power in the simulated field via a power integral at the current Z position.

The width, the height and the shape of the integration area can be set manually by the Rsoft CAD settings which we defined to be a  $0.8 \times 5 \mu\text{m}^2$ ,  $1.2 \times 10 \mu\text{m}^2$  and  $1.8 \times 10 \mu\text{m}^2$  (same as the waveguide approximate area shape) respectively. It computes the total power traveling within the coupling waveguide structure (*R-Soft Design Group, 2012*).

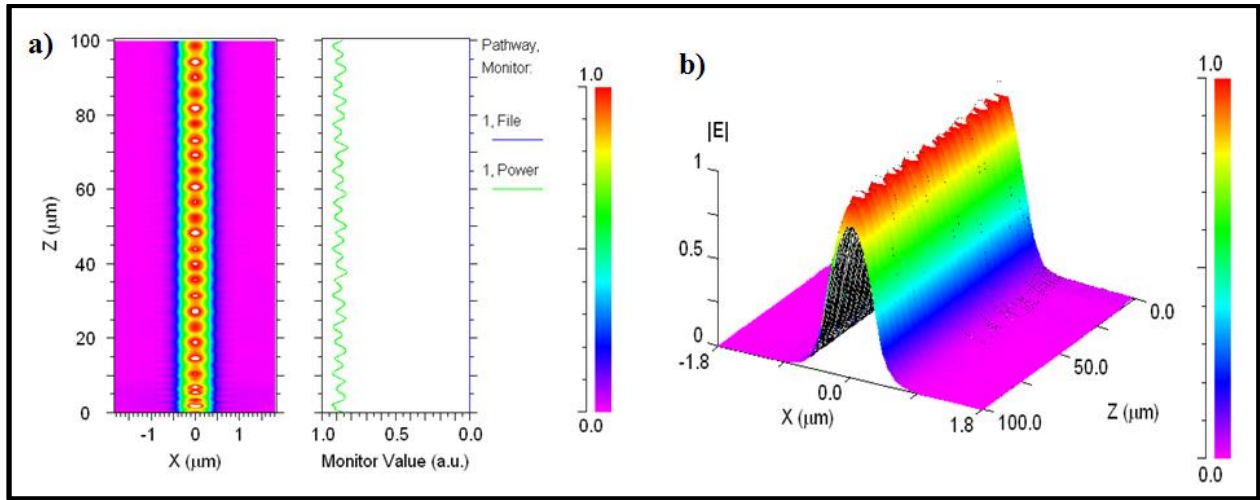
### **3.4.1 Simulations of the optical waveguide Design 1 (OWGD1)**

For our first analyses of the first design test structure 1 (OWGD1) shown in Figure 23, we simulated the optical waveguide structure design 1 shown in Figure 23 (a) with the TEOS 1 and TEOS 2 material properties used to design the waveguide, with TEOS 2 having a higher index density layer due to densification strategies used to increase the refractive index from 1.46 to 1.48. With a core index of high



refractive index of 1.48 and surrounded by background material of silicon oxide of refractive index 1.46, optical propagation is guided within the core of higher refractive index due to Snell's law of refraction and total internal reflection.

The R-Soft simulation result of this structure is as shown in Figure 30. Figure 30 shows very low loss propagation with slight multimode super-positioning in the E-field as function of distance along the optical waveguide. Figure 30 (a) is a 3D E-field simulation of waveguide design 1, and displays a dynamic field amplitude as a function of x and z as a 2D colour-coded contour map of the transverse field profile as a function of x and z, Figure 30 (b) is a 3D contour graph that displays the property of the field amplitude as a function of x and z in 3D contour graph with colour coding to indicate amplitude height.

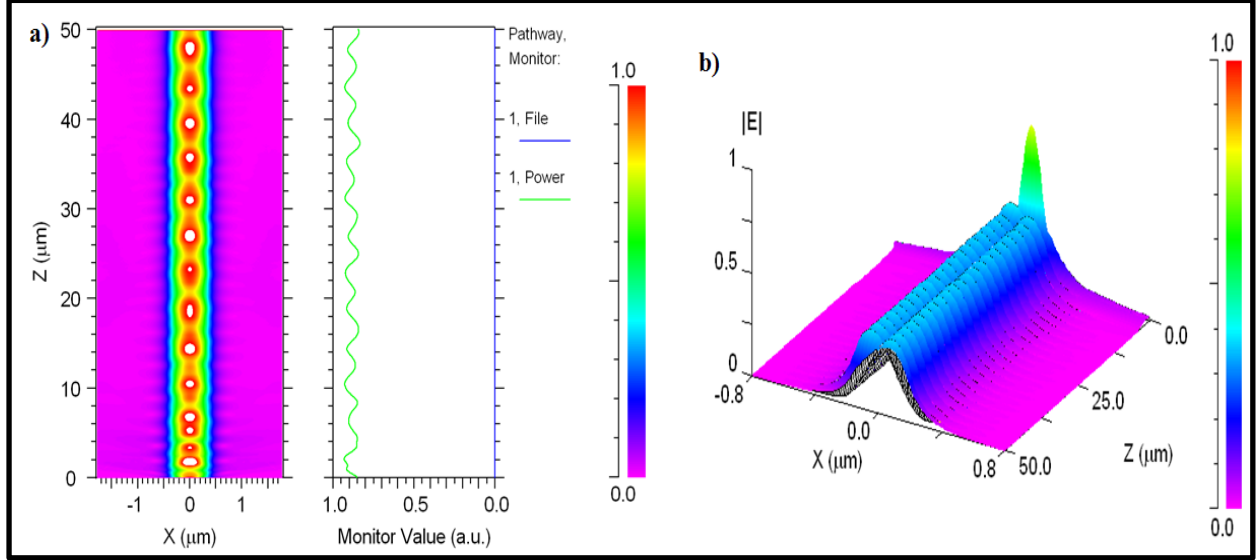


**Figure 30: Waveguide simulation results for design 1 (a) Contour Map (XZ), (b) height-coded E-field**

### 3.4.2 Simulations of optical waveguide Design 2 (OWGD2)

Figure 31 shows the simulation results for the V-shaped groove Silicon-Nitride waveguide design optical test structure 2 (OWGD2) as described in Figure 24, and implemented in optical link test structure design 2 (OLTS2), taking the material properties, dimensions and simulation variable into account, as well as symbols and parameter definitions. The simulation result of this Silicon-Nitride waveguide structure of design 2 shows quite a broad propagation and high multimode content with some optical energy losses in the beginning of the waveguide near to the optical source launch field position as demonstrated in Figure 31 (b).

Despite the initial optical coupling loss, the simulated result shows that there was a very good optical propagation through the waveguide. Multi-mode propagation have the advantage of allowing both a large acceptance angle for coupling of the optical radiation from the silicon LED into the waveguide as well as for emission of light out of the waveguide at the end of the waveguide, and they can also accommodate high curvatures and bends in the waveguides.



**Figure 31: Waveguide simulation results for design 2 (a) Contour Map (XZ), (b) height-coded E-field**

### 3.4.3 Simulations of optical waveguide Design 3 (OWGD3)

In the third design structure 3, as in Figure 25 (a) and (b), the lateral width of the Silicon-Nitride layer is reduced to 0.4 micron in order to form a narrow diameter, higher refractive index core. This design strategy would enable a less multi-mode propagation and lower dispersion of the optical radiation from the source. We simulated the Silicon-Nitride, narrower core waveguide design 3 (OWGD3) shown in Figure 25. From the simulation results as presented in Figure 32, OWGD3 yields much narrower single mode propagation, again with virtually no loss and with very low multimode content. From this simulated result, we noticed in single mode propagation, although much more difficult to couple light into the waveguide in single mode operation, however, we see lower modal dispersion loss along the waveguide. This can enable extreme high modulation bandwidth to be achieved in this kind of narrower core waveguide. This simulation was aided by using trivial basic formulas for light wave transmission characteristics of optical waveguides (*Senior 2009*). Equation (Eq 4.1) gives a conservative estimate of the pulse dispersion per unit length of our designed waveguide's and equation (4.3) gives the approximate bandwidth-length product of the designed waveguide.

$$\zeta_m = L/c[n_1] \quad (\text{Eq 4.1})$$

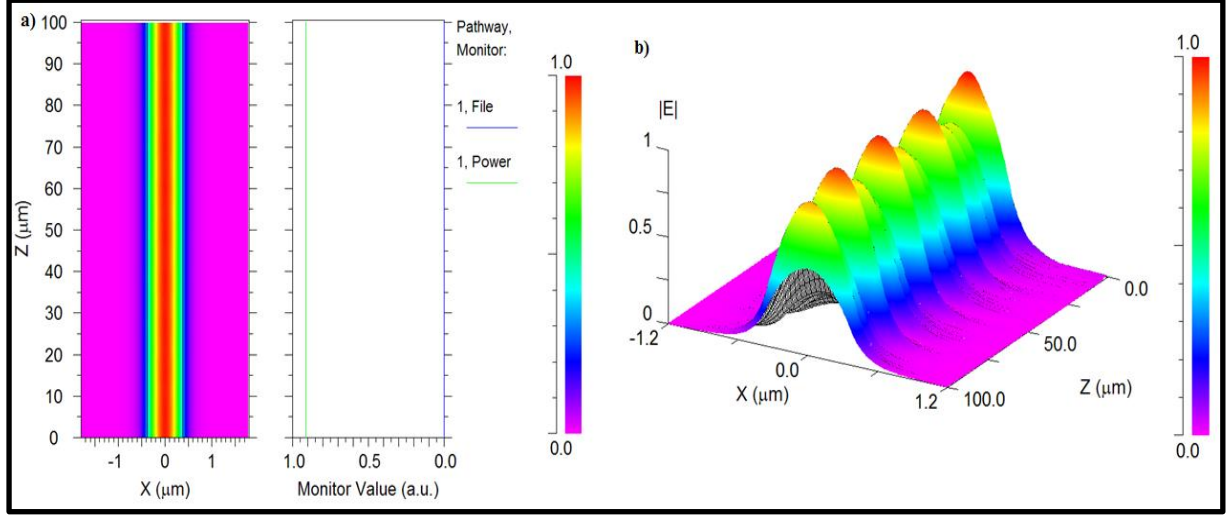
$$\zeta_m = \lambda(d\lambda_1/d\lambda) \quad (\text{Eq 4.1a})$$

$$B_T = 1/2\zeta \quad (\text{Eq 4.2})$$

$$\text{Bandwidth-length product} = B_T \times L \quad (\text{Eq 4.3})$$

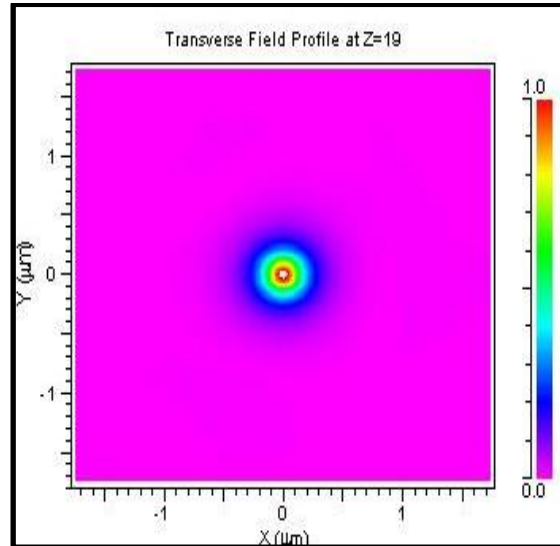
Equation (4.3) gives the estimate of the Bandwidth-Length Product (BLP) mathematically, where  $L$  is the length of the waveguide,  $\zeta$  is the pulse dispersion,  $B_T$  is the maximum bandwidth,  $c$  is velocity of light in vacuum,  $\lambda$  is the propagating wavelength,  $n_1$  is the refractive index of the waveguide core.

Subsequent calculations reveal a maximum dispersion of  $0.5 \text{ ps.nm}^{-1}$  and a bandwidth-length product of a value higher than  $100 \text{ GHz.cm}$  for a  $1.4 \text{ }\mu\text{m}$  Silicon-Nitride based waveguide core. A maximum modal dispersion of  $0.2 \text{ ps.nm}^{-1}$  and a bandwidth-length product of higher than  $200 \text{ GHz.cm}$  for a  $0.4 \text{ }\mu\text{m}$  are estimated for silicon-oxi-nitride core (see Figure 25), all embedded in a  $1\text{ }\mu\text{m}$  diameter silicon-oxide cladding. The materials dispersion characteristic is estimated at approximately  $10^{-3} \text{ ps.nm}^{-1}$  which is much lower than the maximum predicted modal dispersion for the designed waveguide. Hence, the designed waveguides proved viable for on-chip optical links channel at  $750\text{nm}$  wavelength and in micron dimensions.



**Figure 32: Waveguide simulation results for design 3 (a) Contour Map (XZ), (b) height-coded E-field**

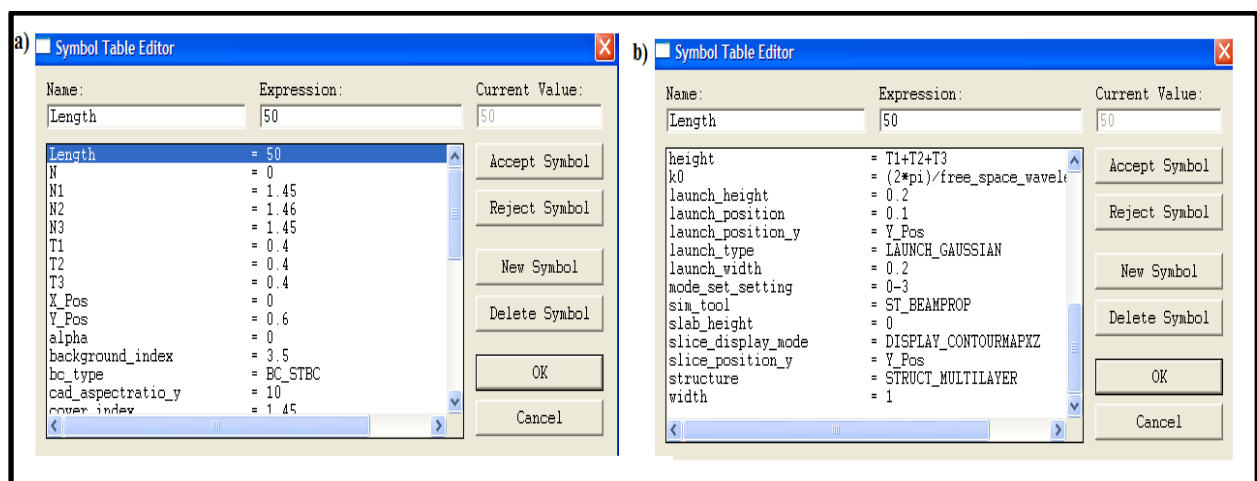
Figure 33 shows the predicted transverse field profile optical simulation for a  $0.2 \text{ }\mu\text{m}$  diameter nitride core waveguide embedded in a silicon oxide surrounding matrix. Using the imaginary part of the refractive index as predicted by R-SOFT, low loss characteristics of  $0.65 \text{ dBcm}^{-1}$  are predicted, taking the material properties as predicted by the R-SOFT simulation program into account.



**Figure 33: Transverse field profile for a Silicon-Nitride based waveguide with a core of 0.2  $\mu\text{m}$  diameter Silicon-Nitride embedded in a 1  $\mu\text{m}$  diameter silicon oxide cladding.**

During the simulation of the designed waveguides, parameter variables, symbols were created and implemented on the desired design and this was done through *the symbol table editor of the R-Soft software suit*.

Any variable mathematical expression in the symbol table editor can be set to be a function of any other variable. For example, the variable  $k_0$  in the symbol table editor is set to a value of  $(2\pi \text{ free\_space\_wavelength})$  corresponding to the magnitude of the *wave-number  $k$*  in free space of the wavelength value chosen. Complete built-in-functions and constants needed for accurate simulation results are found in the *symbol table editor* (See Figure 34).



**Figure 34: Sample of Symbol Table Editor (a) Top list (b) Bottom list**

### 3.5 RF Substrate Coupling Considerations in Device On-Chip Optical Links at 750nm

The RF substrate coupling between the source and the detectors in the on-chip optical micro links device designed were investigated, tested and analysed with a HP 50GHz vector network analyser (VNA) series 8510 (50 MHz-40 GHz) frequency sweep, to verify the optical coupling from source via the designed waveguides through to the photo detector.

However, before the experimental measurements of optical light wave transmission coupling on the fabricated devices on wafer in the experimental setup, the device topology equivalent two port network models of the structures were modelled, constructed and simulated for each test structure. The reason for this was to access and investigate the inherent RF characteristics of the test structures and to access and analyse our device RF parasitic effect for all the parasitic capacitance and inherent resistance as present in the structures and as seen by the RF power modulating signal, because RF oxide parasitic coupling reduces the device optical coupling fidelity.

- **Some of the parameters and Constants used in the calculations:**

$K$  = dielectric constant ( $K = 1.5$  for silicon,  $K = 3.9$  for SiON,  $K = 7.5$  for  $\text{Si}_3\text{N}_4$ )

$\epsilon_0 = 8.85 \times 10^{-14}$  F/cm (electric permittivity)

$\rho_{p+} = 0.01\Omega$ ,  $\rho_{p-} = 10^3\Omega.\text{cm}$ ,  $\rho_p = 10\Omega.\text{cm}$ ,  $\rho_{n+} = 0.01\Omega.\text{cm}$  ( $\rho$  = Resistivity)

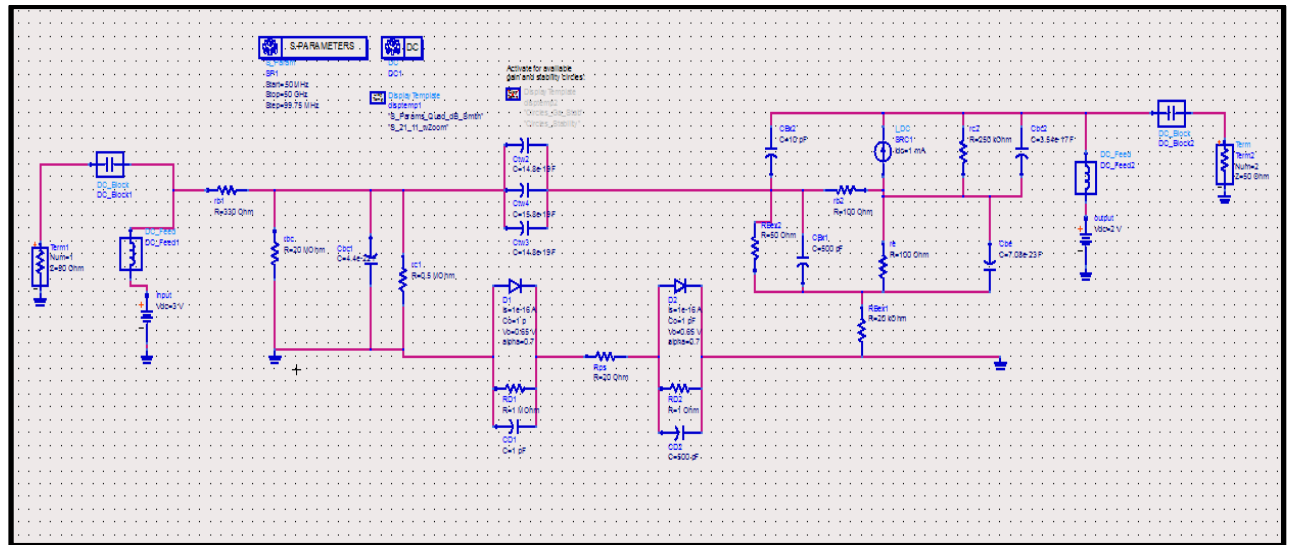


Figure 35: Optical link topology two-ports network model of (OLTS1)

Figure 35 is the two-port equivalent network circuit of the complete optical link of the designed device (OLTS1). In Figure 35, the various material resistances, the junction depletion capacitance, the resistance and diodes are the inherent elements as seen by the modulating RF signal through the device structure. Using simple electronic circuit theory formulas, the series and the parallel elements component approximated values were calculated using device know dimensions, material resistivity and permittivity. The two port networks were simulated with S-Parameter simulation tool in Advanced Design System

(ADS) software. In this simulation, only S21 parameter was considered, in other to ascertain and estimate the level of substrate coupling in the device express as power gain ratio in dB versus frequency in GHz of the forward optical light wave transmission from the optical source to the detector with full transparent boundary condition (TBC) techniques.

The total waveguide capacitance ( $C_{TW}$ ) as seen by the signal is the parallel sum of the individual capacitor as present in the various TEOS oxide layers between the optical source and the optical detector. The various reverse/forward bias p-n junctions depletion capacitance and resistance were calculated, the diode depletion resistance and capacitance as present in the device semiconductor material p-n junction as well as the optical source semiconductor material resistance at the input, and the optical detector semiconductor resistance at the output sections were also calculated using device known parameters and dimensions. The various semiconductor material doping level, the resistivity and permittivity are presented in Figure 27.

**Base  $n^+$  resistance ( $r_{bl}$ ) was calculated;**

$$r_{bl} = \left[ \frac{\rho L}{A} \right] \quad (Eq\ 5.1)$$

Where  $\rho$  is the  $n^+$  material resistivity,  $L$  is the length of the  $n^+$  material;  $A$  is the cross-sectional surface area of the  $n^+$  material

**Base collector depletion resistance ( $r_{bc}$ )**

$$r_{bc} = \left[ \frac{\rho L}{A_{bc}} \right] \quad (Eq\ 5.2)$$

Where  $\rho$  is the material resistivity,  $L$  is the length of the  $p^+$  material;  $A_{bc}$  is base collector depletion region cross-sectional surface area.

**Base collector depletion capacitance ( $C_{bc1}$ )**

$$C_{bc1} = \left[ \frac{\epsilon A_{bc}}{W_{bc}} \right] \quad (Eq\ 5.3)$$

Where  $\epsilon$  is the electric permittivity,  $A_{bc}$  is base collector depletion region cross-sectional surface area and  $W_{bc}$  is the depletion thickness (width of the depletion region).

**Collector  $p^+$  material resistance ( $r_{cl}$ ) was calculated;**

$$r_{cl} = \left[ \frac{\rho L}{A} \right] \quad (Eq\ 5.4)$$

Where  $\rho$  is the material resistivity,  $L$  is the length of the  $p^+$  material;  $A$  is the cross-sectional surface area of the  $p^+$  material.

**Capacitance of the waveguides is given by ( $C_{wl}$ ):**

$$C_{wl} = \left[ \frac{K \cdot \epsilon_0 \cdot A}{d} \right] \quad (Eq 5.5)$$

Where  $K$  is waveguide material dielectric constant,  $\epsilon$  is the electric permittivity,  $A$  is waveguide cross-sectional surface area and  $d$  is the length of the waveguide.

**Total capacitance of the waveguides in parallel is given by ( $C_{Tw}$ ):**

$$C_{Tw} = [C_1 + C_2 + C_3] \quad (Eq 5.6)$$

Our device dimensions in micron were extracted from the device cadence layout (See Figure 27), Using retro simulation, the dimensions were used in the above equations for the modelled device topology, in order to obtain the approximate device elements values as present in the device structures during the experimental measurements.

**On the detector side of the optical link:**

**Collector  $n^+$  resistance ( $r_{c2}$ ) was calculated;**

$$r_{c2} = \left[ \frac{\rho L}{A} \right] \quad (Eq 5.7)$$

Where  $\rho$  is the material resistivity,  $L$  is the length of the  $n^+$  material;  $A$  is the cross-sectional surface area of the  $n^+$  material

**Base collector depletion capacitance ( $C_{bc2}$ )**

$$C_{bc2} = \left[ \frac{\epsilon \cdot A_{bc2}}{W_{bc2}} \right] \quad (Eq 5.8)$$

Where  $\epsilon$  is the electric permittivity,  $A_{bc2}$  is base collector depletion region cross-sectional surface area and  $W_{bc2}$  is the depletion thickness (width of the depletion region).

**Emitter  $n^+$  resistance ( $r_{e2}$ ) was calculated;**

$$r_{e2} = \left[ \frac{\rho L}{A} \right] \quad (Eq 5.9)$$

Where  $\rho$  is the material resistivity,  $L$  is the length of the  $n^+$  material;  $A$  is the cross-sectional surface area of the  $n^+$  material.

**Base emitter depletion capacitance ( $C_{be2}$ );**

$$C_{be2} = \left[ \frac{\epsilon \cdot A_{be2}}{W_{be2}} \right] \quad (Eq 5.10)$$

Where  $\epsilon$  is the electric permittivity,  $A_{be2}$  is base emitter depletion region cross-sectional surface area and  $W_{be2}$  is the depletion thickness (width of the depletion region).

Base  $p^+$  resistance ( $r_{b2}$ ) was calculated;

$$r_{b2} = \left[ \frac{\rho L}{A} \right] \quad (Eq\ 5.11)$$

Where  $\rho$  is the material resistivity,  $L$  is the length of the  $p^+$  material;  $A$  is the cross-sectional surface area of the  $p^+$  material.

### 3.5.1 RF parasitic results for Design test structure 1 (OLTS1)

In design test structure 1 (OLTS1), the two ports equivalent network model used to represent the inherent electrical element components of the optical link is as shown in Figure 35. The calculated lump circuit components (resistors and capacitors) as seen by the signal modulating the optical source emission during simulation of the device optical link between source and detector were mathematically obtained using the above equations and from known device electrical structure parameters and dimensions.

The generated RF forward transmission coupling analysis curve of OLTS1 is shown in Figure 36.

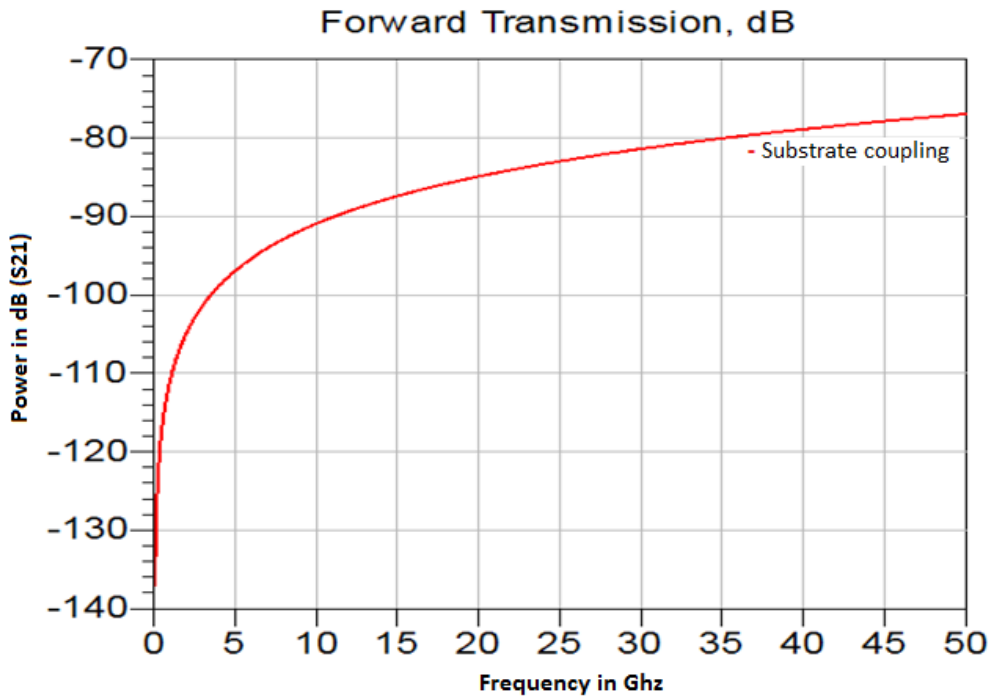


Figure 36: Substrate coupling analysis of OLTS1 device design 1

In essence, the electrical-to-electrical (E/E) components are microwave two-port circuit, and these contained calculated values for each circuit element as seen by the source signal when placed at the modulation input of the optical source. The value of each element was calculated using known device Design 1(OLTS1) structure dimensions, doping level, resistivity and dielectric coefficients of the respective stack semiconductor material layers. With S-parameter simulation of the topology of the model circuit, DC



block and DC feed were used to control the DC and RF signal flow in the modelled circuit. The power gain in dB at the detector side (output) as a result of input power at the source was plotted as function of the frequency, and is shown in Figure 36.

Our device dimensions in micron were extracted from the device cadence layout (See Figure 20), and the dimensions were used in the above equations to obtain the approximate device circuit elements values as presents in the device structures (See Figure 37).

The device topology model equivalent circuit of (OLTS2) contained calculated lumped elements value for each electrical component as seen by the source signal during modulation. The value of each lumped element was calculated using known device Design 2 structure dimensions, the doping level, the resistivity and the dielectric constant of the respective oxide layers and Silicon-Nitride layer.

The calculated lump circuit element components (resistors and capacitors) as seen by the RF power (-10dBm) signal modulating the optical source emission during simulation of the device optical link between source and detector were mathematically obtained using the equations below:

**Collector n resistance ( $r_{cl}$ ) was calculated;**

$$r_{cl} = \left[ \frac{\rho L}{A} \right] \quad (Eq\ 5.12)$$

Where  $\rho$  is the material resistivity,  $L$  is the length of the n material;  $A$  is the cross-sectional surface area of the n material

**Collector emitter depletion resistance ( $r_{ce}$ )**

$$r_{ce} = \left[ \frac{\rho L}{A_{ce}} \right] \quad (Eq\ 5.13)$$

Where  $\rho$  is the material resistivity,  $L$  is the length of the depletion region (width of the depletion thickness) ;  $A_{ce}$  is collector emitter depletion region cross-sectional surface area.

**Collector emitter depletion capacitance ( $C_{ce}$ )**

$$C_{ce} = \left[ \frac{\epsilon A_{ce}}{W_{ce}} \right] \quad (Eq\ 5.14)$$

Where  $\epsilon$  is the electric permittivity,  $A_{ce}$  is collector emitter depletion region cross-sectional surface area and  $W_{ce}$  is the depletion thickness (width of the depletion region).

**Capacitance of the waveguides is given by ( $C_{wl}$ ):**

$$C_{wl} = \left[ \frac{K \epsilon_0 A}{d} \right] \quad (Eq\ 5.15)$$

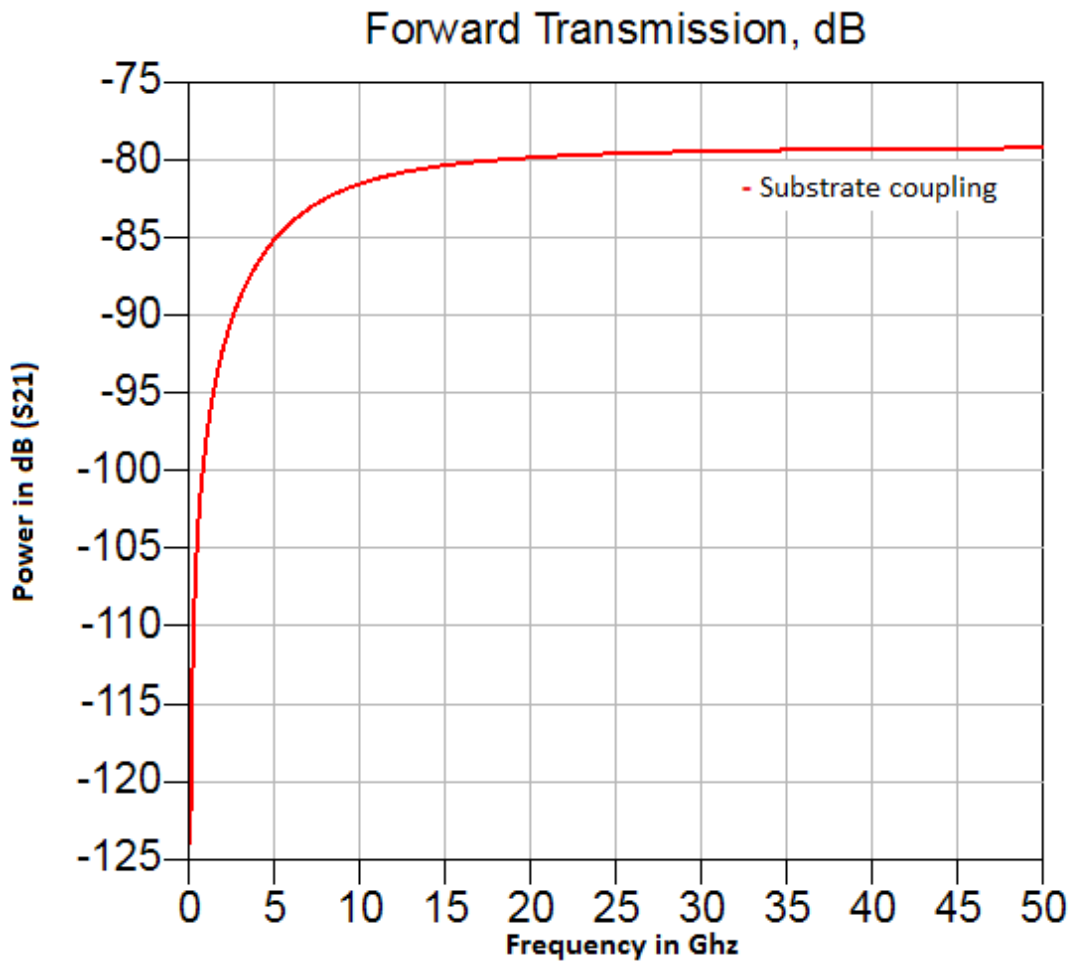
Where  $K$  is waveguide material dielectric constant,  $\epsilon$  is the electric permittivity,  $A$  is waveguide cross-sectional surface area and  $d$  is the length of the waveguide.

**Total capacitance of the waveguides in parallel is given by ( $C_{Tw}$ ):**

$$C_{Tw} = [C_1 + C_2 + C_3] \quad (Eq\ 5.16)$$

Using the simple formula,  $C_{wI} = (K\epsilon_o A)/d$ , the total capacitance as seen by the signal through the Silicon-Nitride waveguide was calculated approximately. Where  $K$  is the dielectric constant,  $\epsilon_o$  is the electric permittivity,  $A$  is the device structure waveguide cross-sectional surface area and  $d$  is the length of the optical waveguide. In this device, a different biasing configuration was used; the modulating signal was placed on the collector and not on the emitter of the LED optical source.

The generated RF forward transmission coupling analysis curve of OLTS2 is shown in Figure 38.



**Figure 38: Substrate coupling analysis of OLTS2 device design 2**

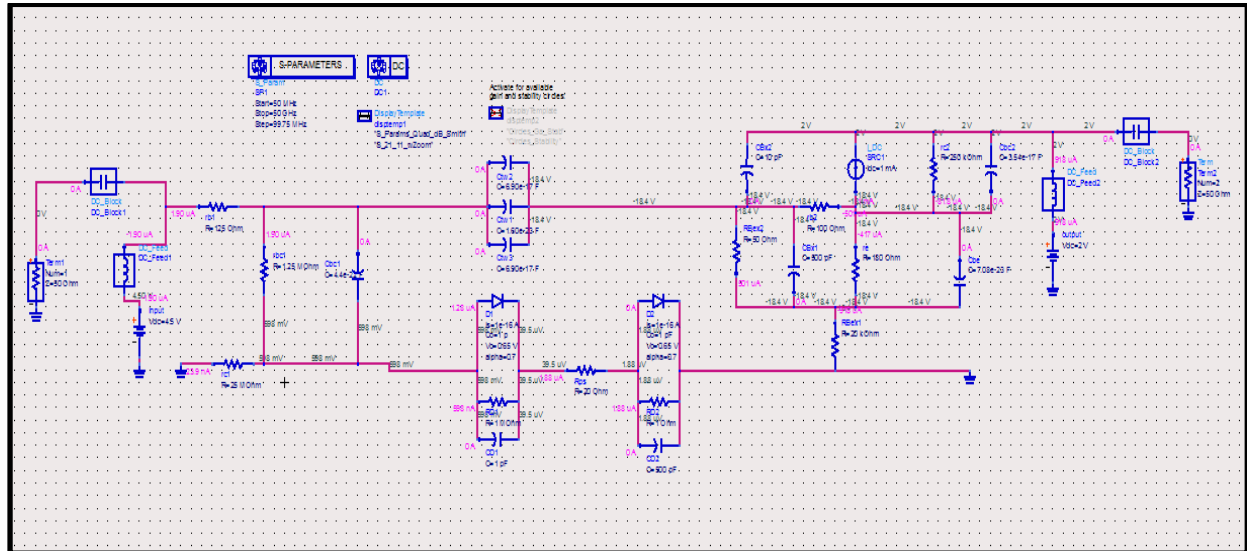
Using ADS simulation software, with S-parameter simulation of the model circuit, DC block and DC feed was used to control the DC and RF signal flow in the circuit. The power gain in dB at the detector side (output) as a result of input power at the source was plotted as function of the frequency as shown in Figure 38.

This substrate coupling analysis curve was a mathematical analysis that allows us to study the mechanism of signal coupling through the substrate and oxide layers from the optical source point to the detector. From the circuit device topology model simulation of the device two ports equivalent circuits, we observed the following:

- *When optical source was not activated, the parasitic oxide RF coupling rises from almost -100dB at 2 GHz to -79dB at 50 GHz.*
- *We see from the equivalent circuit modelling simulation results an increased parasitic coupling with increased frequency up to 50 GHz. The substrate and waveguide capacitors from Figure 37 are presumed to be responsible for capacitance parasitic coupling between the optical source and the detector, and there is a high RF coupling at high frequency. If such lateral capacitance was indeed present between the detector and the optical source, a higher coupling would be observed as modulation frequency is increased. More specifically, an increased RF coupling is observed with an increase in frequency, due to the non-linear capacitive coupling.*
- *Due to Schottky contact used in this design, it has low input impedance and has a low oxide coupling in the substrate at high frequencies compare to OLTS1 (see Figure 27 (b)).*

### **3.5.3 RF parasitic result for design test structure 3 (OLTS3)**

Figure 39 is the two-ports equivalent network circuit of the complete optical link of the designed device (OLTS3). The various resistors, the capacitors and diodes are the inherent circuit elements as seen by the modulating RF signal through the device structure. In design test structure 3 (OLTS3), the topology two ports equivalent network model used to represent the inherent electrical element components of the optical link is shown in Figure 39.



**Figure 39: Optical link two-port equivalent network circuit for OLT S3**

Our device dimensions in micron were extracted from the device cadence layout (See Figure 29), and the dimensions were used in the equations below to obtain the approximate device circuit elements values as presents in the device structures (See Figure 39). The device model equivalent circuit of (OLTS3) contained calculated lumped elements value for each electrical element component as seen by the source signal during modulation. The value of each lumped element was calculated using known device Design 3 structure dimensions, the material doping level, the resistivity and the dielectric constant of the respective oxide layers and Silicon-Nitride layer.

The calculated circuit element components (resistors and capacitors) as seen by the signal modulating the optical source light wave emission during simulation of the device optical link between the source and the detector were mathematically obtained using the equations below:

**Base  $p^+$  resistance ( $r_{b1}$ ) was calculated;**

$$R_{bl} = [\frac{\rho L}{A}] \quad (Eq\ 5.17)$$

Where  $\rho$  is the material resistivity,  $L$  is the length of the  $p^+$  material;  $A$  is the cross-sectional surface area of the  $p^+$  material

**Base collector depletion resistance ( $r_{bc}$ )**

$$R_{bcl} = [\frac{\rho L}{4bc}] \quad (Eq\ 5.18)$$

Where  $\rho$  is the material resistivity,  $L$  is the length of the n material depletion region;  $A_{bc}$  is base collector depletion region cross-sectional surface area.

**Base collector depletion capacitance ( $C_{bc1}$ )**

$$C_{bcI} = [\frac{\mathcal{E}.A_{bc}}{W_{bc}}] \quad (Eq\ 5.19)$$

Where  $\mathcal{E}$  is the electric permittivity,  $A_{bc}$  is base collector depletion region cross-sectional surface area and  $W_{bc}$  is the depletion thickness (width of the depletion region).

**Collector  $n^+$  resistance ( $r_{cI}$ ) was calculated;**

$$R_{cI} = [\frac{\rho L}{A}] \quad (Eq\ 5.20)$$

Where  $\rho$  is the material resistivity,  $L$  is the length of the  $n^+$  material;  $A$  is the cross-sectional surface area of the  $n^+$  material

**Capacitance of the waveguides is given by ( $C_{wI}$ ):**

$$C_{wI} = [\frac{K.\mathcal{E}_o.A}{d}] \quad (Eq\ 5.21)$$

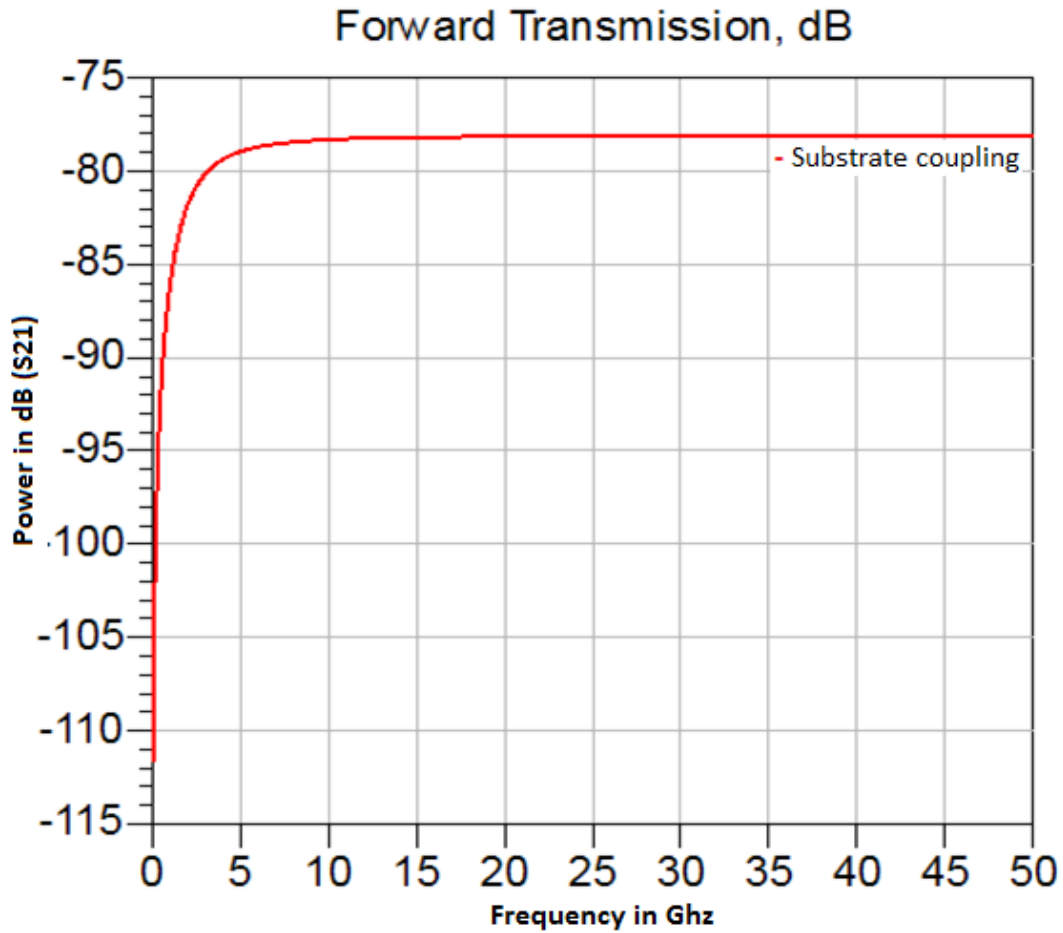
Where  $K$  is the waveguide material dielectric constant,  $\mathcal{E}$  is the electric permittivity,  $A$  is waveguide cross-sectional surface area and  $d$  is the length of the waveguide.

**Total capacitance of the waveguides in parallel is given by ( $C_{Tw}$ ):**

$$C_{Tw} = [C_1 + C_2 + C_3] \quad (Eq\ 5.22)$$

Using the simple formula for capacitance value,  $C_{wI} = (K\mathcal{E}_oA)/d$ , the total capacitance as seen by the signal through the Silicon-Nitride waveguide was calculated approximately. Where  $K$  is the dielectric constant,  $\mathcal{E}_o$  is the electric permittivity,  $A$  is the waveguide structure cross-sectional surface area and  $d$  is the length of the optical waveguide.

In this device, a different biasing configuration was used; the modulating signal was placed on the base terminal and not on the emitter terminal, and the collector was grounded of the LED optical source.



**Figure 40: Substrate coupling analysis of OLTS3 device design 3**

The substrate coupling analysis curve was a mathematical analysis that allows us to study the mechanism of signal coupling through the substrate and oxide layers from the optical source point to the detector. From the circuit device model simulation of the device topology two-port equivalent circuits, we observed the following:

- When optical source was not activated, the parasitic oxide RF coupling rises from almost -90dB at 1 GHz to -79dB at 50 GHz.
- We see from the equivalent circuit modelling simulation results an increase parasitic coupling with an increase in frequency of up to 50 GHz. The substrate, the device circuit element components and the waveguide capacitors from Figure 39 were presumed to be responsible for the capacitance parasitic coupling between the optical source and the detector, and there is a high RF coupling at higher frequency. If such lateral capacitance were indeed present between the detector and the optical source, a higher coupling would be observed as modulation frequency is increased. More specifically, an increased RF coupling is observed with an increase in frequency, due to the non-linear capacitive coupling.

In overall conclusions, we see an approximate average oxide coupling of -85dB with an average frequency of 45GHz, which is below the predicted waveguide parasitic oxide coupling of -80dB as determined later on by the Vector network Analyser (VNA) standard calibration kit, using the short circuit, the open circuit, the isolation and the 50 $\Omega$  through calibration test kit standard techniques respectively. The device circuit topology model equivalent two ports network investigation analysis, enlighten us and give us more insight about the inherent RF characteristics of the designed optical link test structures and the oxide parasitic effect on the modulating signal as a result of all the parasitic capacitances and resistances present in the test structures. These results were compared to the RF experimental optical link response measurement results in chapter 4 and chapter 5 respectively.



# CHAPTER 4: Reverse biased Avalanche LED based Optical Links

## 4.1 Introduction

This chapter presents the experimental test measurement of optical link test structures 1 and 2. The first section focuses on the device-probing configuration in order to accurately bias the LED device and the detector device. The reverse bias LED configurations as well as the DC bias analysis and characterization of the optical link test structure 1 (OLTS1) and the device OLTS1 DC&RF probing configurations are discussed in details.

*The second section focuses on the Experimental realization and results for Optical link test structure 1 (OLTS1):* In this chapter, the reverse bias LED configurations as well as the DC bias analysis and characterization of the optical link test structure 1 (OLTS1) and the device OLTS1 DC&RF probing configurations are discussed in details. The RF power analysis and characterization of the on-chip optical link and the experimental confirmation of on-chip optical link with TEOS waveguide geometry operating at 750nm wavelength results are presented in this chapter.

*Third section presents the experimental realisation and results for Optical link test structure 2 (OLTS2):* In this section, the DC bias analysis and characterization of the optical link test structure OLTS2 are discussed and as well as the device OLTS2 DC&RF probing configurations. The RF power analysis and characterization of the on-chip optical link and the experimental confirmation of on-chip optical link with Silicon-Nitride waveguide V-groove geometry operating at 750nm wavelength results are presented here.

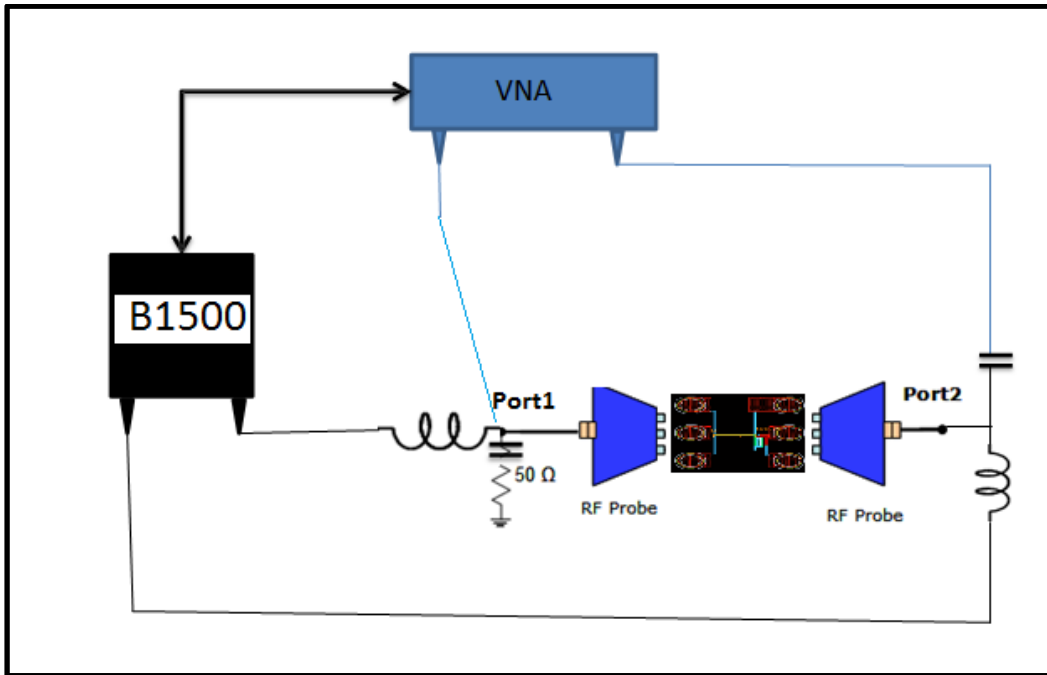
*The fourth section focuses on the experimental realisations and results for optical link test structure 3 (OLTS3-RB):* In this chapter, the DC bias analysis and characterisation of the optical link test structure 3 (OLTS3) operated in reverse bias are discussed and as well as the device OLTS3 DC&RF probing configurations. The RF power analysis and characterization of the on-chip optical link and the experimental confirmation results as well as the characterization of the on-chip optical link and the experimental measurements of on-chip optical link, with Silicon-Nitride narrow core waveguide geometry operating at 750nm are presented in this chapter.

### 4.1.1 Device testing, experimental measurement, results interpretation and device characterisation

The experimental test setup for the realized on-chip optical links device designed with an RF SiGe bipolar process and the established DC and AC characterisation coupling parameters, AC signal transmission and bandwidth capabilities are discussed in this chapter.

The test bench set up as in Figure 41 was used in order to measure the opto-microwave performances of the optical links device. Port 1 of the Vector Network Analyzer (VNA) directly modulates a 750nm optical

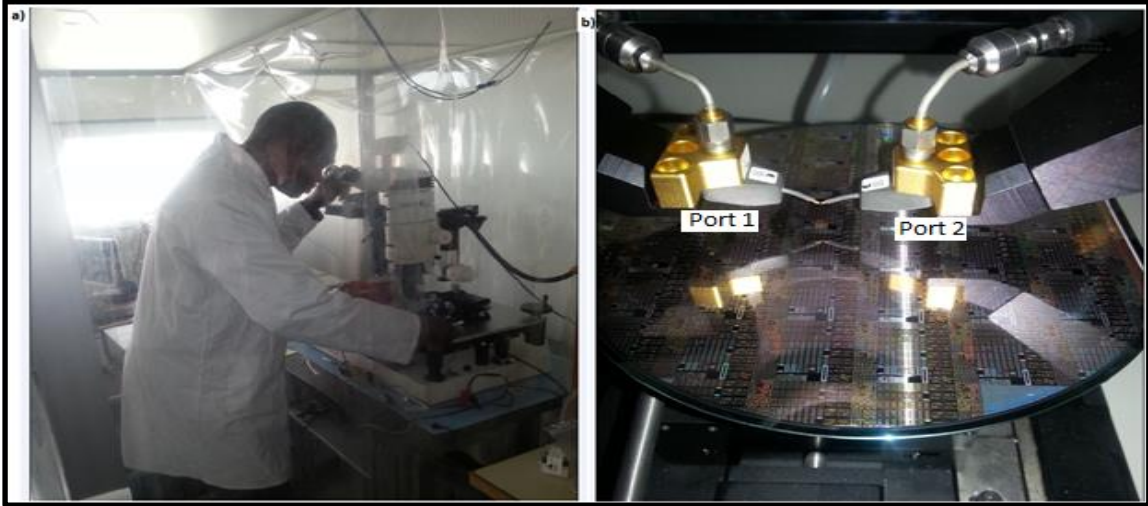
LEDs source (LEDS) while port 2 is connected to the detector. The direct modulated optical signal of the source LEDs is transmitted through the designed waveguide of the device to the detector.



**Figure 41: The opto-microwave measurement test set setup. The device under test includes the optical link device, the bias tee probes**

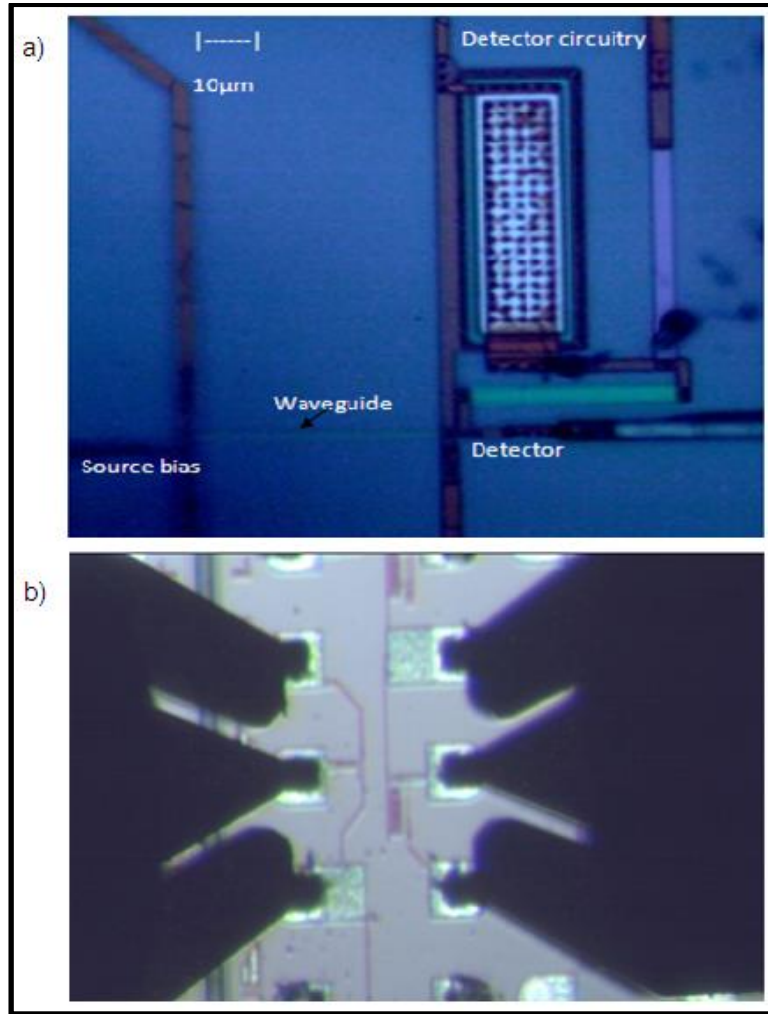
The base of the HPT is connected to a GSG probe. The base is biased using a bias tee with a 50Ω load attached to the RF input of the bias tee. Port 2 of the VNA is linked to the collector access of the HPT to bias the transistor and collect the output signal. The VNA used for the experiment is 8753ES 40GHz VNA and it is connected to an Agilent B1500 semiconductor parametric analyzer. The B1500 help to supply accurate DC voltage and current to the device.

The device under test is a 750nm on-chip optical links silicon base avalanche LED, optical waveguide and a photo detector fabricated integrated on Wafer (Optical die 3), with an optical aperture of 1μm, plus the waveguide and the detector. The light is coupled from the LED optical source through the designed optical TEOS layers and Silicon-Nitride optical waveguides with light wave total internal reflection mechanism to the SiGe detector (Photodetector). 200μm pitch GSG probes were used to connect the DC and RF power input signal to access the devices on the die (Wafer). RF modulating signal and DC biasing voltage are applied through the bias ground signal ground (GSG) probe tee as well as on the detector side to activate the detector. A photo-picture of the characterization setup is shown in Figure 25. The experiment was conducted on an optical nano test bench shown in Figure 42 (a); Figure 42 (b) shows the zoomed wafer containing the designed optical link devices.



**Figure 42: Experimental characterization setup (a) Test bench photo picture (b) Zoomed wafer containing devices under test**

In this chapter, we described the device testing setup and the device testing procedures. The fabricated on-chip integrated optical link device is shown in Figure 43 (b). The device under test is a 750nm-850nm Silicon base avalanche LED die (Wafer) where the light is coupled from the LED optical source through the designed optical TEOS or Silicon-Nitride optical waveguide to the SiGe detector.



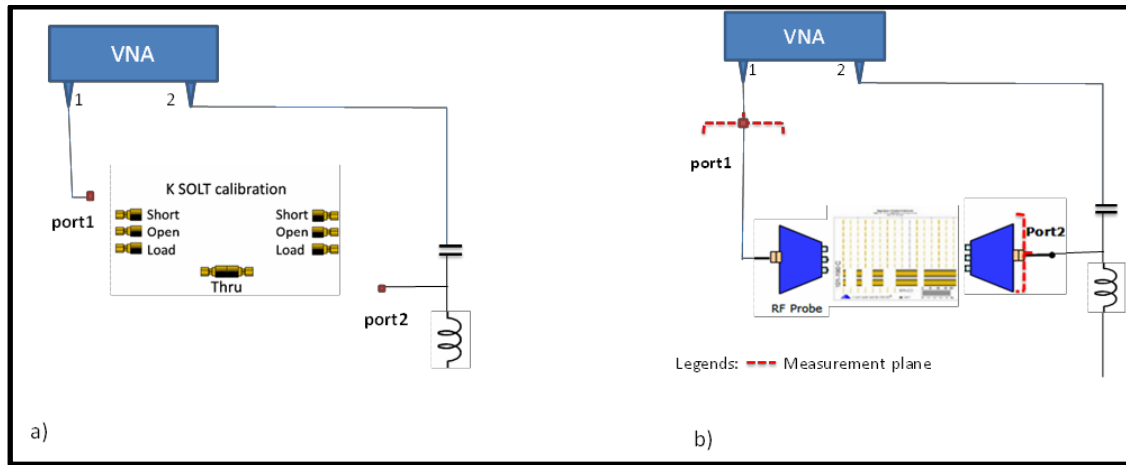
**Figure 43: (a) Microscopic picture of the optical link device (b) Microscopic picture of G-S-G probe connection on one of the devices during measurement**

The RF coupling between the source and the detector in the on-chip optical micro-links are tested and analyzed using a vector network analyzer (VNA) (50 MHz-40 GHz). The experimental setup described in this chapter 4, is used to characterize the link (from source via the designed waveguides to the detector). 200 μm pitch GSG probes (shown in Figure 43 (b)) are used to connect the DC and RF input signals to the devices on the device on the wafer. RF signal and DC biasing are applied on the source and detector sides through GSG probes via VNA internal tee bias. RF signal on the source modulates the optical power emitted from the source.

#### 4.1.2 Calibration of the measuring equipment

The first step for this technique involves setting up the measurement bench for full two-ports on-wafer calibration and performing the equipment calibration, the K-SOLT (Short, Open, Load, Thru) calibration standards. In this configuration, the input and output ports are both K connectors. In the first step, a full 2-ports calibration is performed using the K-SOLT calibration standards. The GSG probes are connected and one performs Short, Open, Load and Thru measurements using the GSG probe calibration kit. The second step consists in calibrating the bench through a SOLT calibration using type K loads, as

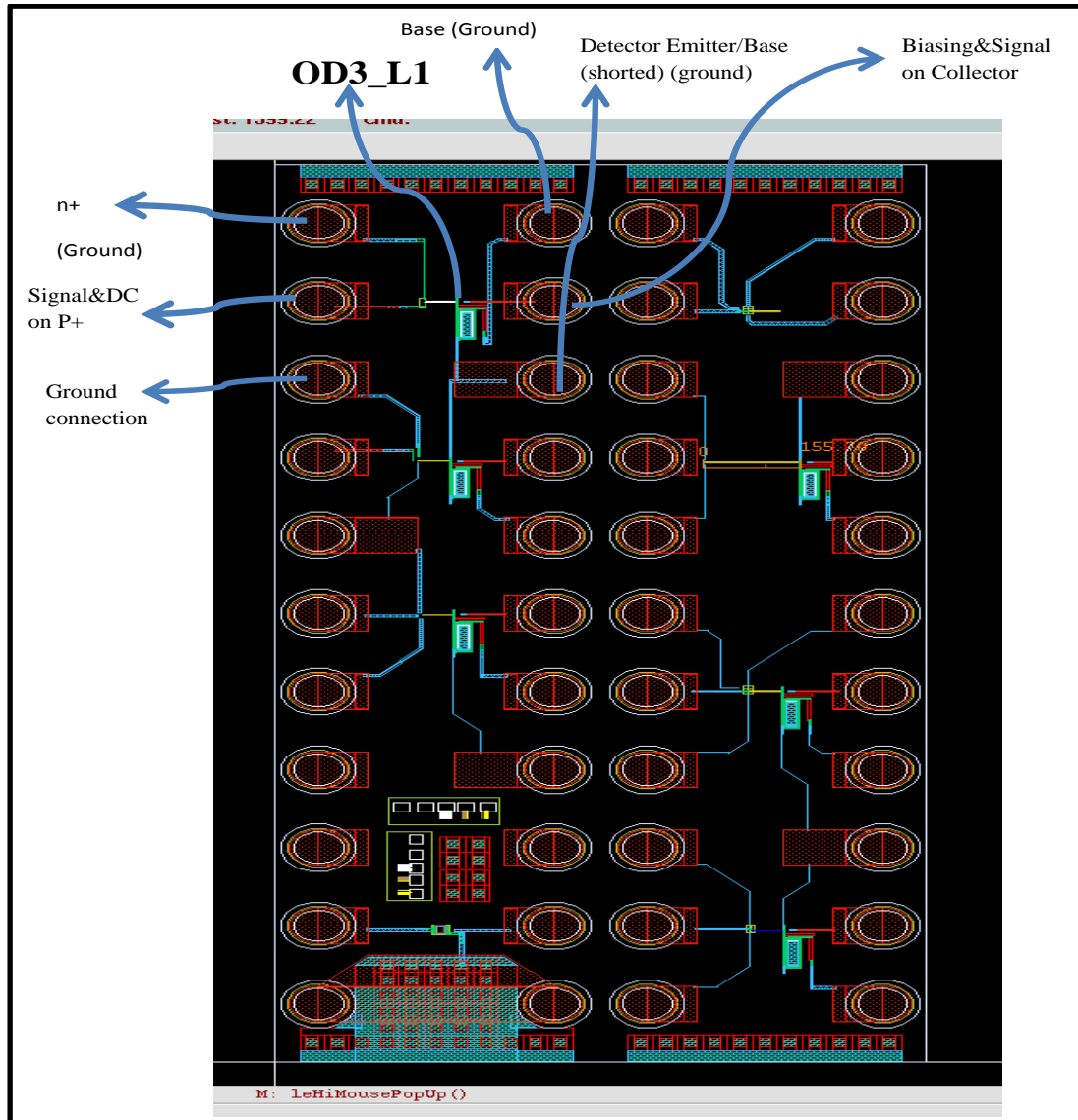
shown in Figure 44 (a). In the third step, one measures the loads SHORT, OPEN, LOAD, and THRU on substrate calibration kit as shown in Figure 44 (b), to complete the calibration in order to standardise the optical link floor on the VNA.



**Figure 44: (a) K-SOLT calibration bench setup. (b) Bench setup to measure microwave parasitic using a substrate standard calibration kit**

#### 4.1.3 Optical probing configuration on OLTS1

The optical probing of optical die 3 layer 1 (OD3\_L1) corresponding to OLTS1 device design 1 is shown in Figure 45. The device was biased as indicated in Figure 45.



**Figure 45: Device topology layout viewed with Cadence design software (OD3\_L1)**

#### **4.1.4 Test procedures and Parameters**

- Port 1 & Port 2 coupled; same configuration for optical source and detector
- Wafer: high resistivity, with nitride (no capacitors): Wafer was high resistance with reference (02A0).
- Minimised  $S_{12}/S_{21}$  when probes are up: calibration standardisation was done, and it was found to be (-75dB)
- Calibrated VNA with the following: the RBW, the averaging, the VBW, the number of points and smoothing off (during calibration). Averaging was set at 300 sampling points
- Frequency test range: 50MHz – 40GHz at 401 points
- Noted reference number: Substrate Run, wafer and the chip reference number, with nitride or without nitride: 20Ω.cm or 2000Ω.cm substrate: was done.

- RF input power = -10dBm (100 $\mu$ W)

#### 4.1.5 MATLAB main program for DC biasing and RF signal supply to device

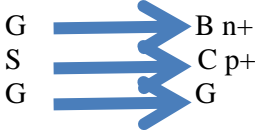

*MATLAB* as a mathematical programmable tool was used to develop a customised and versatile code for biasing our device and for modulating the optical emission with RF input power. The *MATLAB* code developed for the initialization of variable and biasing the optical source and the detector is shown in Appendix A. The complete algorithm for this *MATLAB* program for DC biasing and RF signal modulating the devices is listed in Appendix C (See APPENDIX C).

Similarly, the algorithm for the DC biasing and launching the voltage and current values to the optical link device structures through the Agilent B1500A Semiconductors extractor is given in Appendix B. The complete algorithm for this *MATLAB* program for launching the desired current and voltage bias values to the devices is presented in Appendix D (See APPENDIX D).

#### 4.1.6 DC biasing test conditions and compliance values for OLTS1

The DC bias test conditions for the optical source, the detector and the corresponding two-port measuring equipment's connected to both ports, vector network analyser (VNA) and the B15100 and voltage and current flow parameters is tabulated in Table 6:

**Table 6: DC biasing test conditions and compliance values for OLTS1**

Conditions	LED Source. (Port 1 of the B1500/VNA)	Detector. (Port 2 of the B1500/VNA)
DC biasing voltage (force)	[0 ; - 4.5V], (on p+)	+2V Fixed reverse bias (on C)
DC current (measured)	[0; -3mA] (I <sub>1</sub> )	+10nA (dark current); +0.1 $\mu$ A (I <sub>2</sub> )
Compliance	I <sub>c</sub> = 5mA	I <sub>c</sub> = 2mA
Current Directions	I <sub>p</sub> + (0 – 2mA) outgoing for the LED; The B1500 measures a negative current, because signal was on a p+	I <sub>c</sub> (10nA (dark current) – 0.1 $\mu$ A) Incoming into the HPT; The B1500 measures a positive current, because signal was on collector.
Optical Probing		

#### 4.1.7 RF test results analysis and compliance values

For the RF signal input, the RF power was ON all the time during the experiment. Table 6 tabulates the test control parameters, the tabulated test results as well as the expected results for optical die\_3 layer 1 (OD3\_L1) (OLTS1) characterization. During the course of the experiment, we observed that when optical probe was dropped down on the device contacts, the device was switched ON and the detector optical current link response rise from 20nA to about 96nA (see figure 46 (b)). And when AC was superimposed on the optical emission to modulate the optical light wave emitting from the LED, we observed that S21 was slightly higher than S12 at low frequencies (optical coupling) and S21 curve was the same as S12 at higher frequencies, optical coupling mixed with substrate coupling (RF coupling).

**Table 7: Test control parameters**

Conditions ( RF Power ON all the time)	Expected results	Control Parameters
Probes up (with the biasing ON) [0V:4V] for Source [0V:2V] for detector	$S_{21} = S_{12}$	DC currents; all S Parameters
Probes down (DC OFF)	$S_{21} = S_{12}$	DC currents; all S Parameters
Probes down (DC ON) (See Figure 47; test configuration)	What is $S_{21}$ , $S_{12}$ ?; $S_{21}$ & $S_{12}$ were very close at low frequency (optical coupling) but the same at high frequency (RF coupling) or oxide coupling.	DC currents; all S Parameters

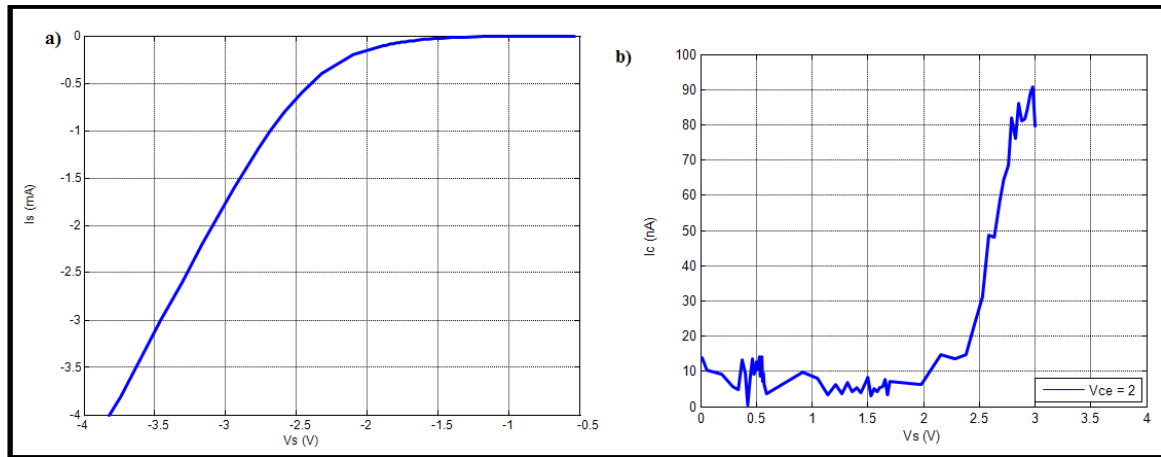
**Table 8: Measured results (RF analysis)**

Conditions (Power ON all the time)	LED Source (V)	Detector (V)	Measured Results (RF analysis)
Test 1	-3.5V on (p+)	+2V Fixed (on collector)	See Figure 47
Test 2	-4V on (p+)	+2V Fixed (on collector)	See Figure 47
Test 3	Peak (~ -3.8V) on (p+)	+2V Fixed (on collector)	See Figure 47
Test 4	(-3V; -4.5V)	+2V Fixed (on collector)	No RF plots



#### 4.1.8 DC bias analysis and characterization of test structure 1 (OLTS1)

DC bias and current analysis were performed on our first device design test structure 1 (OLTS1) of the optical links test structures in die 3 layer 1 on the wafer (OLTS1). DC results as measured for OLTS1 are presented in Figure 46. Detector link current responses were observed simultaneously as shown in Figure 46 (b) when the source was reverse bias in avalanche mode as shown in Figure 46 (a). The observed detector current was of the order of 10 to 100 nano- Amps when the Si Av LED source was activated.



**Figure 46: DC IV Curves for OLTS1 (a) Reverse bias Optical source IV curve (b) Detector optical link response when source was activated for OLTS1.**

In the IV curves as correspondingly monitored on the detector side, a detector current of about 91nA was detected at the onset voltage of -2.6V at the source, plotted here as  $I_c$  versus  $V_s$  shown in Figure 46 (b).

When biasing voltage is placed on the base with the optical GSG probe tee,  $V_b = V_d$ , and  $I_b = I_d = -I_c$  and when biasing is placed on the collector on the detector side with the optical GSG tee,  $V_c = V_d$ , and  $I_c = I_d = -I_b$ . So that  $I_b = I_d = I_c$  at  $V_c$  bias.

Where;

$V_b$  is base voltage;  $V_d$  is detector voltage;  $I_b$  is base current;  $I_d$  is detector current;  $V_c$  is collector voltage;  $V_s$  is source voltage and  $I_c$  is collector current.

*This observation hence confirmed that light wave transmission did indeed occur through the designed waveguides from the optical source to the optical detector through the TEOS oxide waveguide core layer ( $n = 1.48$ ) at DC bias conditions. This measurement further confirmed that, only with optical emission occurring at the source, detector current of several nano-Amps (91nA) was observed for the optical link test structure (OLTS1).*

#### 4.1.9 RF power analysis and characterization of test structure 1 (OLTS1)

The experimental results as measured with regard to RF modulation for the test structure (OLTS1) when optical source and detector were biased and activated are shown in Figure 47. Only S21 and S12 (S-Parameters) of the two ports network measurements are presented here as a function of frequency.

Higher S21 measurements as demonstrated here would confirm optical propagation and optical coupling did indeed occur from the optical source via the optical waveguide to the optical detector. The measurement of S12, indicate parasitic capacitance coupling of the RF frequency through the oxide layer or through the silicon substrate, between the detector and the optical source. If such lateral capacitance were actually present between the detector and the optical source, a higher coupling would be observed as the modulation frequency is increased. More specifically, an increased RF coupling was observed with increase in frequency, due to the non-linear capacitive coupling. Coupling through the semi-insulating substrate, on the other hand, would be more resistive in nature and would contribute more towards a flat response with increasing frequency.

In the overall experiment, the curves resembled the modelled simulated curve were the overall observed coupling is much higher than the predicted RF simulated parasitic coupling of (-79dB). However, the S21 is not much higher than S12 in this structure. Thus, we conclude that S21 higher than predicted parasitic RF coupling occurred in this test structure during the real experiment measurement than the predicted by our theoretical simulation for this structure. Although optical coupling was observed, it was presumably swamped by high RF parasitic oxide coupling as present during the real measuring circumstances.

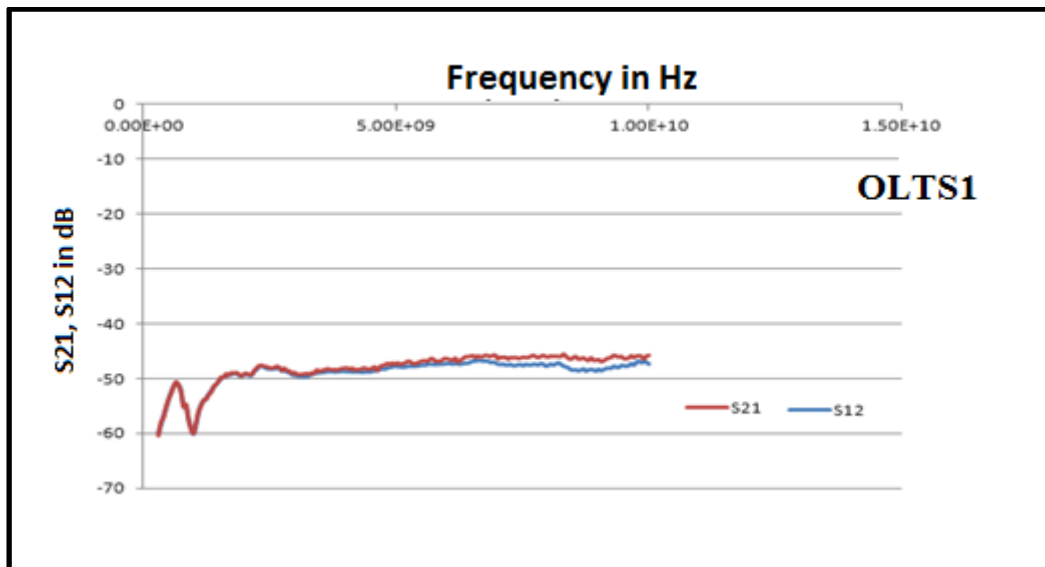


Figure 47: Optical coupling and RF coupling

In overall, it implies that low optical coupling value was realised and high parasitic RF coupling was present in this structure. This indicates that our optical waveguide design philosophy of TEOS 2 yielding higher refractive index ( $n = 1.48$ ) with thermal annealing process was probably not very successful. However, this area could be further exploited by further follow up on research and new improved waveguide design using different processing design parameters.

## **4.2 Experimental Realisations and Results for OLTS2**

In this test structure, the optical source LED was designed with Schottky design strategy with the intention to reduce the device electrical contact area, which invariably reduces parasitic capacitance, and hence optimise optical coupling in this structure. The waveguide in this device is the V-shape groove Silicon-Nitride core surrounded by a TEOS oxide of lower refractive index ( $n=1.46$ ). The device under test is a 750nm on-chip optical links silicon base avalanche LED, the optical waveguide and a photo detector fabricated and integrated on a Wafer (Optical die 3\_L2), with an optical aperture of 1 $\mu$ m, plus the waveguide and the detector. The light is coupled from the LED optical source through the designed optical TEOS layers and Silicon-Nitride optical waveguides to the SiGe detector. A 200 $\mu$ m pitch GSG probes were used to connect the DC and RF power input signal access to the devices contact terminal on the die (Wafer). RF modulated signal and DC biasing are applied through the bias ground signal ground (GSG) probe tee to the device optical source as well as on the detector side, to activate the detector (See Figure 43 (b)).

### **4.2.1 Optical probing configuration on device 2(OLTS2)**

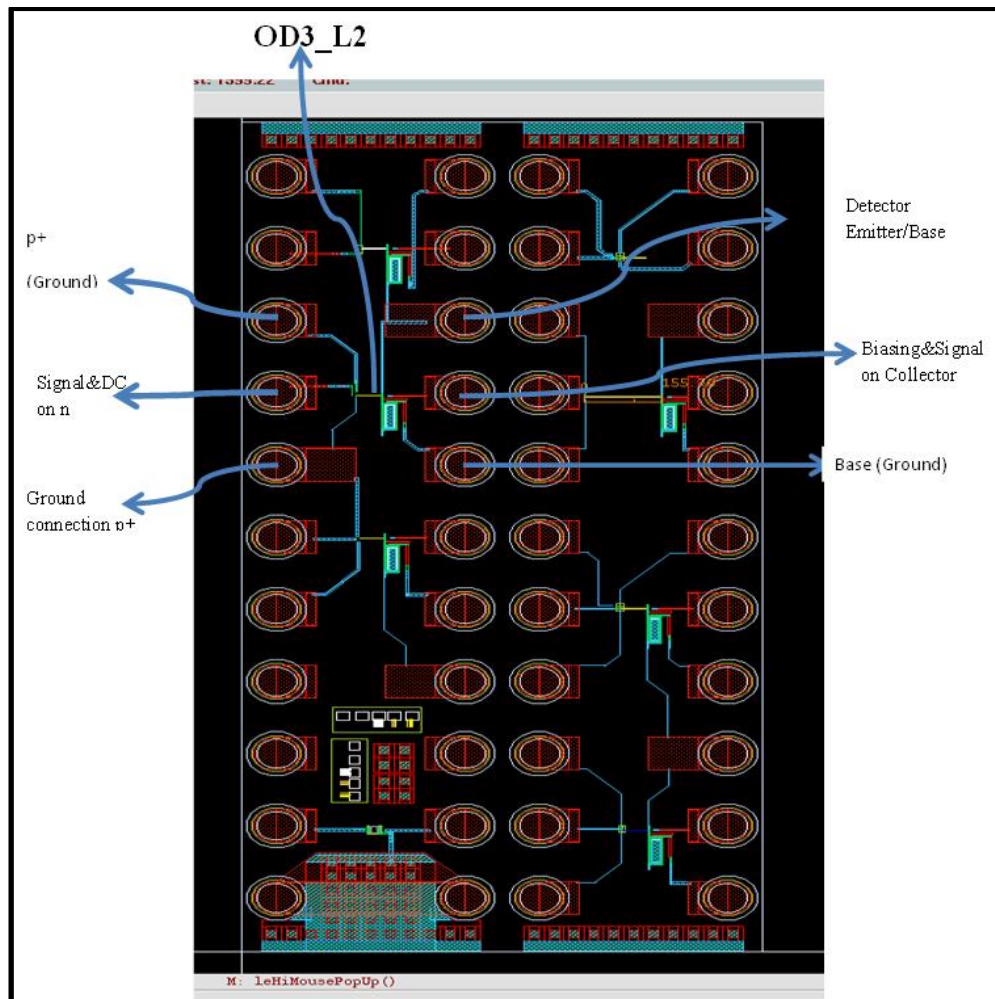
The optical probing of optical die 3 layer 2 (OD3\_L2), device (OLTS2) is showed in Figure 48. In this configuration, the emitter and the base were shorted, and grounded. DC biasing and RF power input signal were supplied through the collector contact with the GSG probe tee on the source side. On the detector side, DC biasing and signal was applied through the collector contact terminal and the detector emitter and the base were shorted.

Table 9 shows the bias voltage, current values and the device compliance values during the experimental measurement. The direction of the current flow in the device is also tabulated in Table 9.

### **4.2.2 Test procedures and objectives:**

- Port 1 & Port 2 coupled; same configuration for optical source and the detector
- Wafer: high resistivity, with nitride (no capacitors): Wafer was high resistance with reference (02A0)
- Minimised  $S_{12}/S_{21}$  when probes are up: calibration standardisation was done, (-75dBm)
- Calibrated with the following: the RBW, the averaging, the VBW, the number of points and smoothing off (during calibration). Averaging was set at 300 sampling points

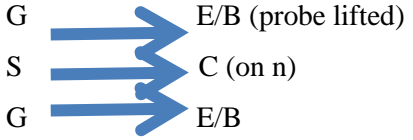
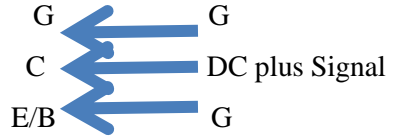
- Test frequency range was 50MHz – 40GHz at 401 point steps
- Noted reference number : Substrate run ,wafer and the chip reference number was noted and recorded, with nitride or without nitride: 20 $\Omega$ .cm or 2000 $\Omega$ .cm substrate: was noted
- RF input power = -10dBm (100 $\mu$ W)



**Figure 48: Device topology layout viewed with cadence design software (OD3\_L2)**

During the experimental measurement on this test structure device OLTS2, the Agilent B1500 VNA Instrument Analyser measured a negative current outgoing from the LED source and a negative current incoming into the Heterojunction photo detector (HPT) as tabulated in Table 9.

**Table 9: DC biasing test conditions and compliance values for OLTS2**

Conditions	LED Source.(Port 1of the B1500/VNA)	Detector.(Port 2 of the B1500/VNA)
DC biasing voltage (force)	[0 ; +1.5V], (on n)	+2V Fixed reverse bias (on C)
DC current (measured)	[0; 10mA] (I <sub>1</sub> )	+10nA (dark current); +0.1μA (I <sub>2</sub> )
Compliance	I <sub>c</sub> = 10mA	I <sub>c</sub> = 2mA
Current Directions	I <sub>c</sub> which is I <sub>s</sub> (0 –10mA) outgoing for the LED; The B1500 measures a negative current	I <sub>c</sub> (10nA (dark current) – 0.1μA) Incoming into the HPT; The B1500 measures a negative current
Optical Probing		

**Table 10: Control parameters**

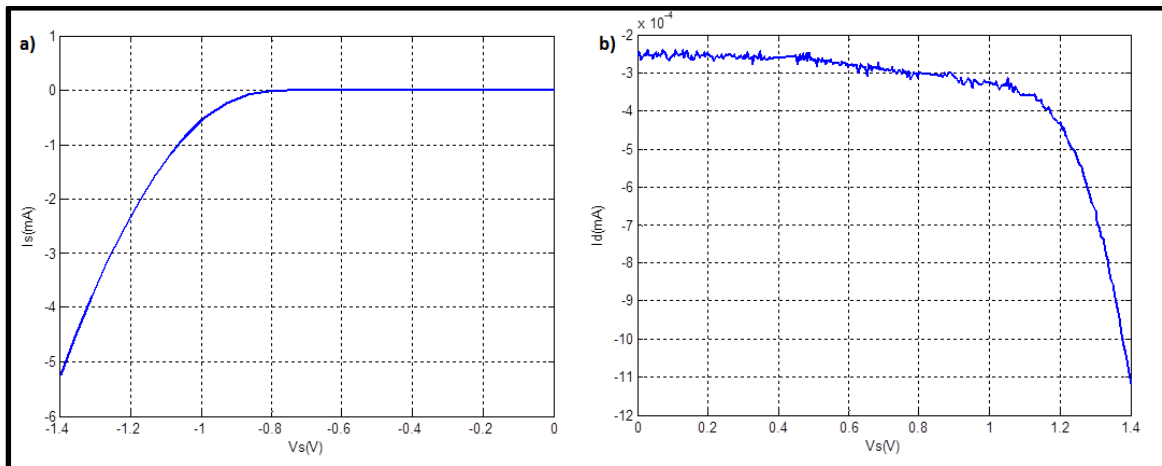
Conditions ( RF Power ON all the time)	Expected results	Control Parameters
Probes up (with the biasing ON) [0V:1.5V] for Source [0V:2V] for detector	$S_{21} = S_{12}$	DC currents; all S Parameters
Probes down (DC OFF)	$S_{21} = S_{12}$	DC currents; all S Parameters
Probes down (DC ON) (See Figure 48, test configuration)	What is $S_{21}$ , $S_{12}$ ?; $S_{21}$ curve higher than $S_{12}$ curve at low frequency (optical coupling) but they are almost the same at high frequency (RF coupling)	DC currents; all S Parameters

**Table 11: Measured results (RF analysis)**

Conditions (Power ON all the time)	LED Source (V)	Detector (V)	Measured Results (RF analyses)
Test 1	+1 on (n)	+2V Fixed (on collector)	See Figure 50
Test 2	+1.36V on (n)	+2V Fixed (on collector)	See Figure 50
Test 3	Peak ( $\sim +1.4V$ ) on (n)	+2V Fixed (on collector)	See Figure 50
Test 4	(+1V; 1.4V)	+2V Fixed (on collector)	No RF plot

#### 4.2.3 DC bias analysis and characterization on test structure 2 (OLTS2)

In the IV curves as correspondingly monitored on the detector side, a detector current of about 95nA was detected at the onset voltage of 1.36V at the source, plotted here as  $I_c$  versus  $V_s$  in Figure 49. The DC curves obtained at both the LED optical source side and the detector side for this test structure (OLTS2) is shown in Figure 49, when the LED optical source was reverse bias. It can be seen that, when reverse biasing the base collector junction, current flowed through the device up to about 4mA shown in Figure 49 (a). The reverse bias knee voltage was about 1.36V as shown in Figure 49 (a) and the corresponding detector link response photo current was about 95nA (Figure 49 (b)). This observation hence confirmed that light wave optical transmission through the designed waveguide did indeed occur from the optical source to the optical detector through the nitride waveguide layer. This measurement further confirmed that, only with optical emission occurring at the source, a detector current of this several nano-Amps (95nA) was observed for the optical link test structure OLTS2.



**Figure 49: DC IV Curves for OLTS2 (a) Forward bias Optical source IV curve (b) Detector optical link response when source was activated for OLTS2.**

#### 4.2.4 RF power analysis and characterization of test structure 2 (OLTS2)

Figure 50 shows the experimental results on test structure 2, (OLTS2) with Schottky contact reverse bias at the optical source. Again, only  $S_{21}$  and  $S_{12}$  S-parameter components are considered here. In this design, the contact area on the LED side was reduced with Schottky design strategy, which helps to reduce the depletion region of the n material, hence parasitic capacitance was reduced. Hence more optical coupling at lower frequencies and an increase in oxide coupling at higher frequencies as in Figure 50.

From Figure 50, our analysis shows clearly higher  $S_{21}$  than  $S_{12}$ . This clearly indicates that some optical propagation did occur along the Silicon-Nitride V-groove waveguide in this OLTS2. Assuming that a -60 dB loss would occur because of the V-groove designed geometry waveguide over a 50  $\mu\text{m}$  spherical radiation from the source, but still, there was about -32 dB optical coupling shown in Figure 50.

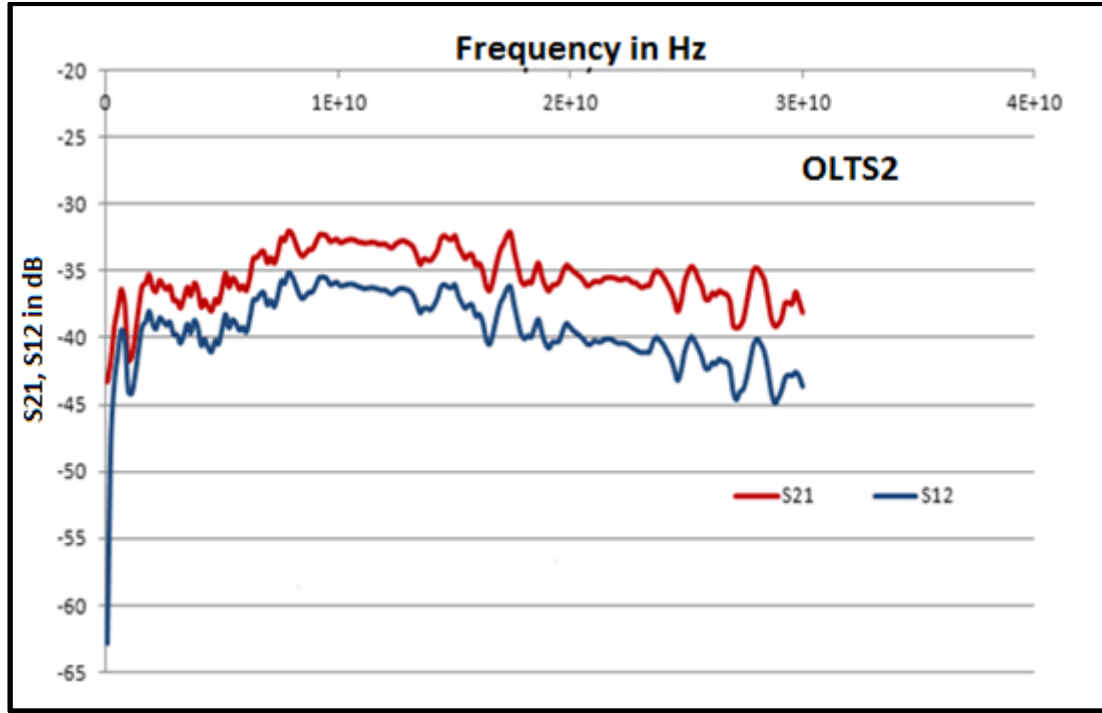
From section 4.2.1 (Test procedures and objectives), in bullet number 3, the vector network analyser (VNA) was calibrated and we minimised  $S_{12}/S_{21}$  when probes were up, and the initial coupling signal reference floor was found to be -75dB. Which means that the optical coupling ( $S_{21}$ ) rises from -75dB to about -32dB at 10 GHz. This implies that the total optical loss is approx. -32dB at 10 GHz.

This result, further confirmed that some definite optical wave guiding did occur in this structure along the Silicon-Nitride waveguide core.

Extremely promising observations from this set of results is that the  $S_{21}$  coupling curve is about 5dB higher than  $S_{12}$  with RF frequencies of up to 5GHz (and related purely to RF parasitic coupling, since no optical emissions were emitted at the detector), which confirm that optical propagation did occur along this waveguide from the Si Av LED to the SiGe detector at high RF frequencies.

The high  $S_{12}$  values that were observed as function of increasing frequency were again attributed to parasitic conduction along the semi-insulating substrate. When specific OLTS2 structure capacitance and resistive values were analysed according to the device structure topology modelled and nitride waveguide modelled in Figure 40. Detailed simulation analysis revealed that the capacitive coupling along the oxide layer seems to be minimal and of several dB power orders lower in dB (See Figure 50). But, the fact that higher  $S_{21}$  curve than  $S_{12}$  curve was observed up to about 10 GHz and even beyond is an indicative of the successful transmission of a modulated optical signal that can be achieved with Si Schottky type of Si Av LEDs and nitride core waveguide.

However, certain design aspect of this structure (OLTS2) could still be improved to achieve more optimum optical coupling at high RF frequencies.



**Figure 50: RF coupling results for the realized on-chip micro-optical links on OLTS2**

#### **4.3 Experimental Realisations and Results for OLTS3**

The experimental test setup for the design test structure OLTS3, the realized device on-chip optical link with an RF SiGe bipolar process, the established DC and AC characterisation optical coupling parameters, the AC signal transfer link response and bandwidth capabilities are discussed in this section. Figure 43 shows the die for cadence layout of the device structure for OLTS3.

The device under test is a 750nm wavelength combine unit of silicon base avalanche LED die (on a wafer), with an optical aperture of 1 $\mu$ m. The light is coupled from the LED optical source through the designed Silicon-Nitride optical waveguides to the SiGe detector. The waveguide implemented in this device is a V-shape groove Silicon-Nitride core of refractive index of ( $n = 2.40$ ) surrounded by a TEOS1 oxide layer with lower refractive index of ( $n=1.46$ ) and of 100 $\mu$ m length. A 200 $\mu$ m pitch GSG probes were used to connect the DC and RF power input signal access to the device via the metal contacts of the device on the die. RF modulated signal and DC biasing are applied through the bias GSG probe tee as well as on the detector side during experimental measurements.



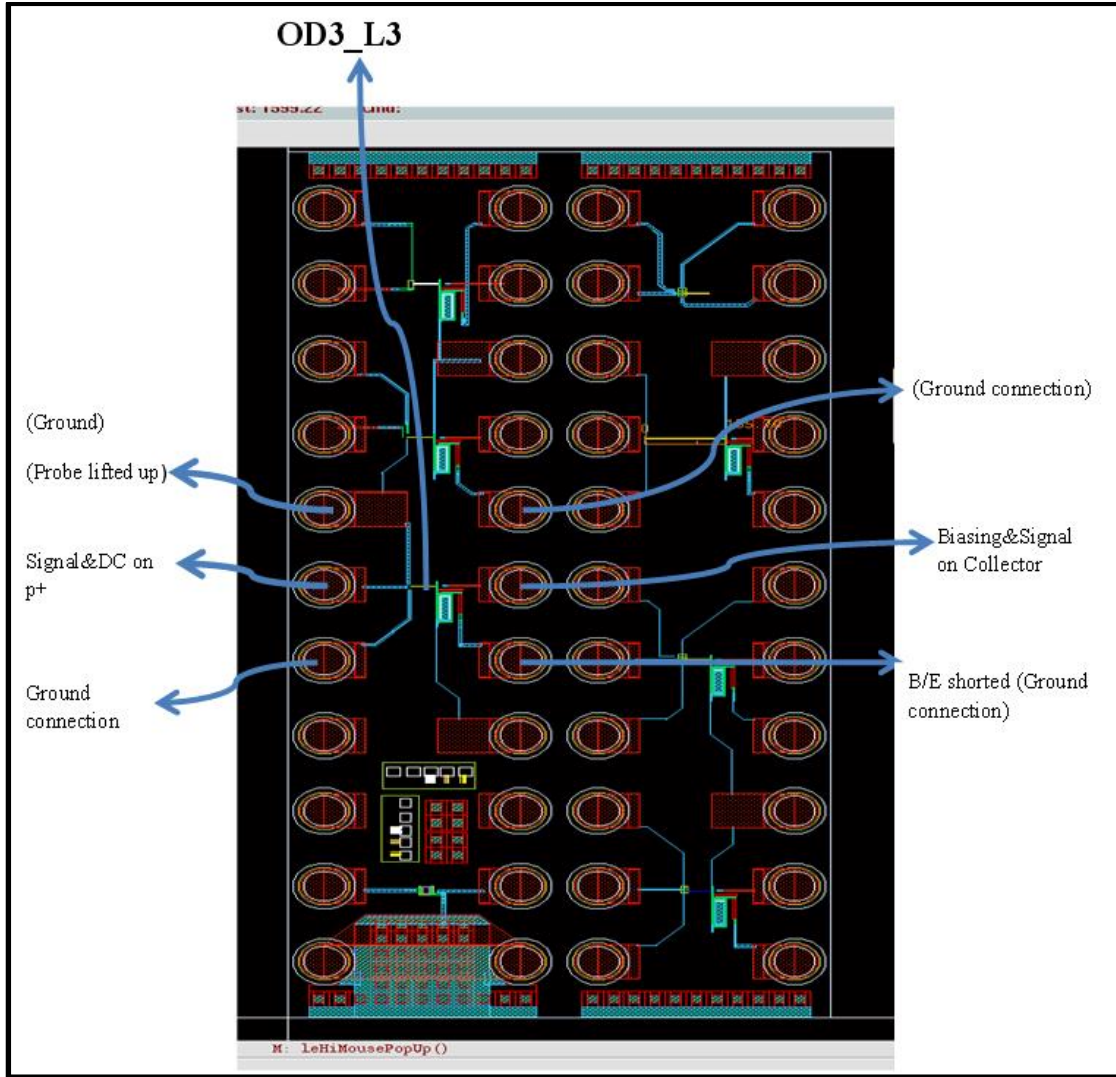


Figure 51: Device topology layout viewed with cadence design software (OD3\_L3)

#### 4.3.1 Optical probing configuration on device 3 (OLTS3-RB)

The optical probing of optical die 3 layer 3 (OD3\_L3) (OLTS3-RB) device is shown Figure 51. In this configuration, on the source side the emitter was grounded, the DC biasing and RF power modulating input signal was supplied to the optical source of the device through the base. On the detector side, the DC biasing and signal was applied through the collector contact terminal, and the base and the emitter were grounded as shown in Figure 51.

In this test structure 3, we carried out a reverse bias analysis, the optical source LED was reverse biased in this device configuration, and where carriers are energised through diffusion through a neutral low resistivity n material and the energetic carriers then dumped into the SiGe base causing transfer of carriers from the L to the T valley, which enable transitions with holes in the p SiGe base.

#### 4.3.2 Procedures and test objectives

- Port 1 & Port 2 coupled; different configurations see Figure 51.
- Wafer: high resistivity, with nitride (no capacitors): Wafer was high resistance with reference (02A0)
- Minimised  $S_{12}/S_{21}$  when probes are up: Was done, and it was (-80dBm)
- Calibrated with the following: the RBW, the averaging, the VBW, number of points and smoothing off (during calibration). Averaging was set at 300 sampling points
- Frequency test range was: 50MHz – 40GHz at 401 points steps
- Noted reference number : Substrate run ,wafer and the chip reference number, with nitride or without nitride: 20Ω.cm or 2000Ω.cm substrate: was noted
- RF input power = -10dBm (100μW).

**Table 12: DC test biasing condition and compliance values for OLTS3**

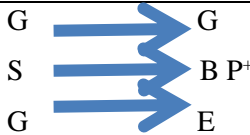
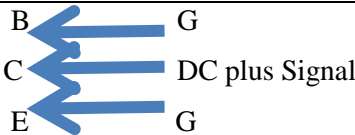
Conditions	LED Source.(Port 1 of the B1500/VNA)	Detector.(Port 2 of the B1500/VNA)
DC biasing voltage (force)	[0 ; +1.5V], (on base P <sup>+</sup> )	2V Fixed reverse bias (on C)
DC current (measured)	[0; 5mA] (I <sub>1</sub> )	+10nA (dark current); +0.1μA (I <sub>2</sub> )
Compliance	I <sub>b</sub> = 5mA	I <sub>c</sub> = 2mA
Current Directions	I <sub>p</sub> + (0 –10mA) outgoing for the LED; The B1500 measures a negative current	I <sub>c</sub> (10nA (dark current) – 0.1μA) Incoming into the HPT; The B1500 measures a positive current
Optical Probing		

Table 12 shows the bias voltage, the current values and the device designed compliance values during the experimental measurements. The direction of the current flow in the device is also tabulated in Table 11 above. During the experimental measurements on this test structure device OLTS3, the Agilent B1500A Instrument Analyser measured a negative current outgoing from the LED source and a positive current incoming into the HPT as tabulated in Table 12.

**Table 13: Control parameters**

<b>Conditions (RF Power ON all the time)</b>	<b>Expected results</b>	<b>Control Parameters</b>
Probes up (with the biasing ON) [0V:1.5V] for Source [0V:2V] for detector	$S_{21} = S_{12}$	DC currents; all S Parameters
Probes down (DC OFF)	$S_{21} = S_{12}$	DC currents; all S Parameters
Probes down (DC ON) (See Figure 51, test configuration)	What is $S_{21}$ , $S_{12}$ ?; $S_{21}$ curve is higher than $S_{12}$ up till 1Ghz frequency (optical coupling) but are almost the same at high frequency (RF coupling)	DC currents; all S Parameters

**Table 14: Measured results (RF analysis)**

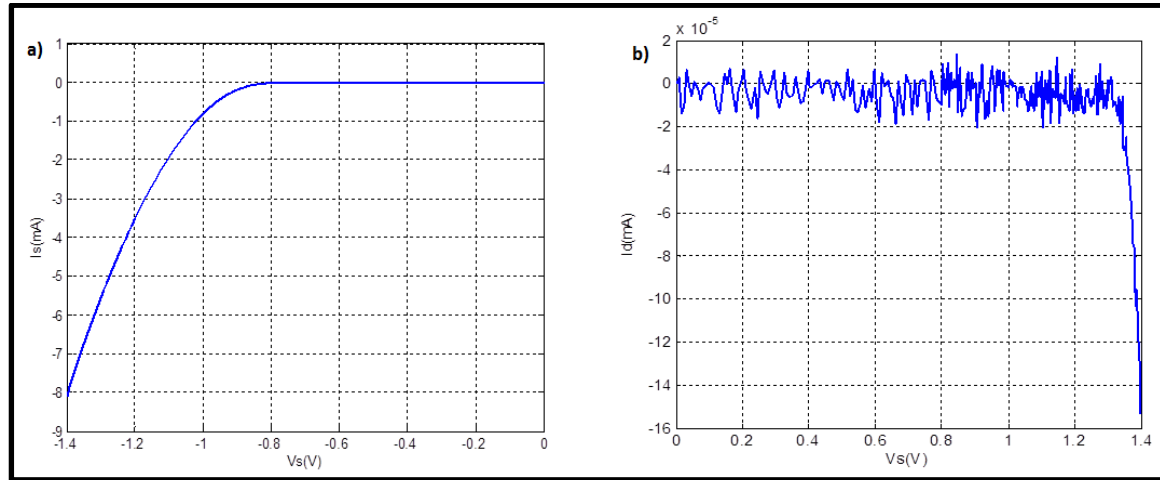
<b>Conditions (Power ON all the time)</b>	<b>LED Source (V)</b>	<b>Detector (V)</b>	<b>Measured Results (RF analyses)</b>
Test 1	+1 on (p)	2V Fixed (on collector)	See Figure 53 (a)
Test 2	+1.36V on (p)	2V Fixed (on collector)	See Figure 53 (b)
Test 3	Peak (~ +1.25V) on (p)	2V Fixed (on collector)	See Figure 53 (c)
Test 4	(+1V; 1.4V)	2V Fixed (on base)	No RF plots

#### 4.3.3 DC bias analysis and characterization of optical link structure OLTS3

In Figure 52, the IV curve of the LED source as well as the correspondingly monitored link response IV curve on the detector side is shown, a detector current of about 80nA was detected by the detector at the onset voltage of 1.36V at the optical source when GSG probe was dropped down and connected to the device on the wafer (see Figure 51), DC ON and RF power ON. The DC IV curves were obtained at both the source and the detector side for this test structure device when the LED source was reverse biased. It was observed that, when this device was placed in a reverse bias condition, current flowed through the device up to about 5mA at 1.36V. The reverse bias knee voltage was about 1.36V as shown in Figure 52(a).

This observation hence confirmed that optical transmission through the designed Silicon-Nitride waveguides did indeed occur from the optical source to the optical detector through the narrow nitride core waveguide surrounded by TEOS1 layer (OWGD3). This measurement further confirmed that, only

with optical emission occurring at the source, that detector current of this several nano-Amps (80nA) was observed for the optical link test structure with DC bias in OLTS3 as shown in Figure 52 (b).



**Figure 52: DC IV Curves for OLTS3 (a) reverse bias Optical source IV curve (b) Detector optical link response when source was activated for OLTS3**

#### 4.3.4 RF power analysis and characterization of test structure 3 (OLTS3)

In test structure 3, we carried out a reverse bias configuration (OLTS3-RB) measurement. In this device, a vertical cubical columnar structure was used for both the optical source as well as the detector. Here we implemented waveguide (OWGD3) in this device structure. The SiGe based region in the same volume structure was used for the optical detection. SiGe p-n junction was placed in reverse bias, and biased into avalanche mode during the measurement process. Since the SiGe structure of this nature has a transition frequency of up to 80GHz, it can be assumed that the reverse bias base-collector junction, when placed in avalanche reverse bias mode, could attain similar transfer frequencies with optical emissions following this modulation frequency. The Silicon-Nitride optical waveguide implemented here was similar to the one in OLTS2, but the Silicon-Nitride layer lateral thickness was strategically reduced in lateral width dimension to narrower nitride core of 0.4 $\mu$ m in diameter in this case, so as to reduce the waveguide core size and enable less modal dispersion and high bandwidth-length product in this waveguide. The capacitive coupling along the oxide layer seems to be very small in ratio and of several orders lower than the forward bias configuration on design OLTS3-FB. In this design configuration, we believe that the source optical emission point was shifted up in the columnar structure, which aligned with the lateral Silicon-Nitride narrow waveguide, thereby creating high acceptance angle for high intensity light wave optical emission emitted into the waveguide core.

From Figure 53 (a), (b) and (c), at different bias condition, ( $S_{21}$  is higher than  $S_{12}$ ) at lower frequency up on until 1 GHz confirming optical coupling. And again, although, from Figure 53 (a), (b) and (c), optical coupling was not visible ( $S_{21}=S_{12}$ ) at higher frequencies, the reason been that the optical

coupling was swamped by the high oxide coupling present with this device, hence it appeared that there was no optical coupling at higher frequencies. At low lower frequencies at three different bias voltage conditions, (1V, 1.2V & 1.25V); S21 curve is higher than S12 up to 1GHz (See figure 53), confirming optical coupling forward transmission from the source to the detector. However, there is high potential bandwidth of about 1GHz that can be achieved with this type of single mode Silicon-Nitride waveguide (see Figure 53).

For the fact that higher S21 curve than S12 was observed here, and up to about 1Ghz, was indicative of optical coupling at low frequencies up till about 1GHz, and a mixed oxide coupling and optical coupling at higher frequencies as shown in Figure 53.

*From our investigation, with this reverse bias configuration the optical source emissions was high in intensity as viewed under microscope, and with the optical source point in good lateral alignment with the waveguide core more light were emitted into the waveguide core. With this reverse bias configuration, we observed that there was a higher optical coupling into the waveguide at lower frequency which result to an increase in S21curve to about -15 dB above the S12 curve as shown in Figure 53 (a), (b) and (c) at 1V, 1.2V and 1.25V bias voltage respectively. And there was an increase in parasitic coupling at much higher frequencies which dominates over the existing optical coupling at these high frequencies. From Figure 45, we concluded that there was an observed optical coupling up on till about  $\geq 1$  GHz.*

*Approx. 20 dB higher optical coupling was observed at 1 GHz frequency for this optical coupling structure. Presumably the higher source capacitance as offered by the 1x1micron  $p^+n$  structure with the depletion region largely penetrating into the n “collector” region of the structure were mainly responsible for this observed behaviour.*

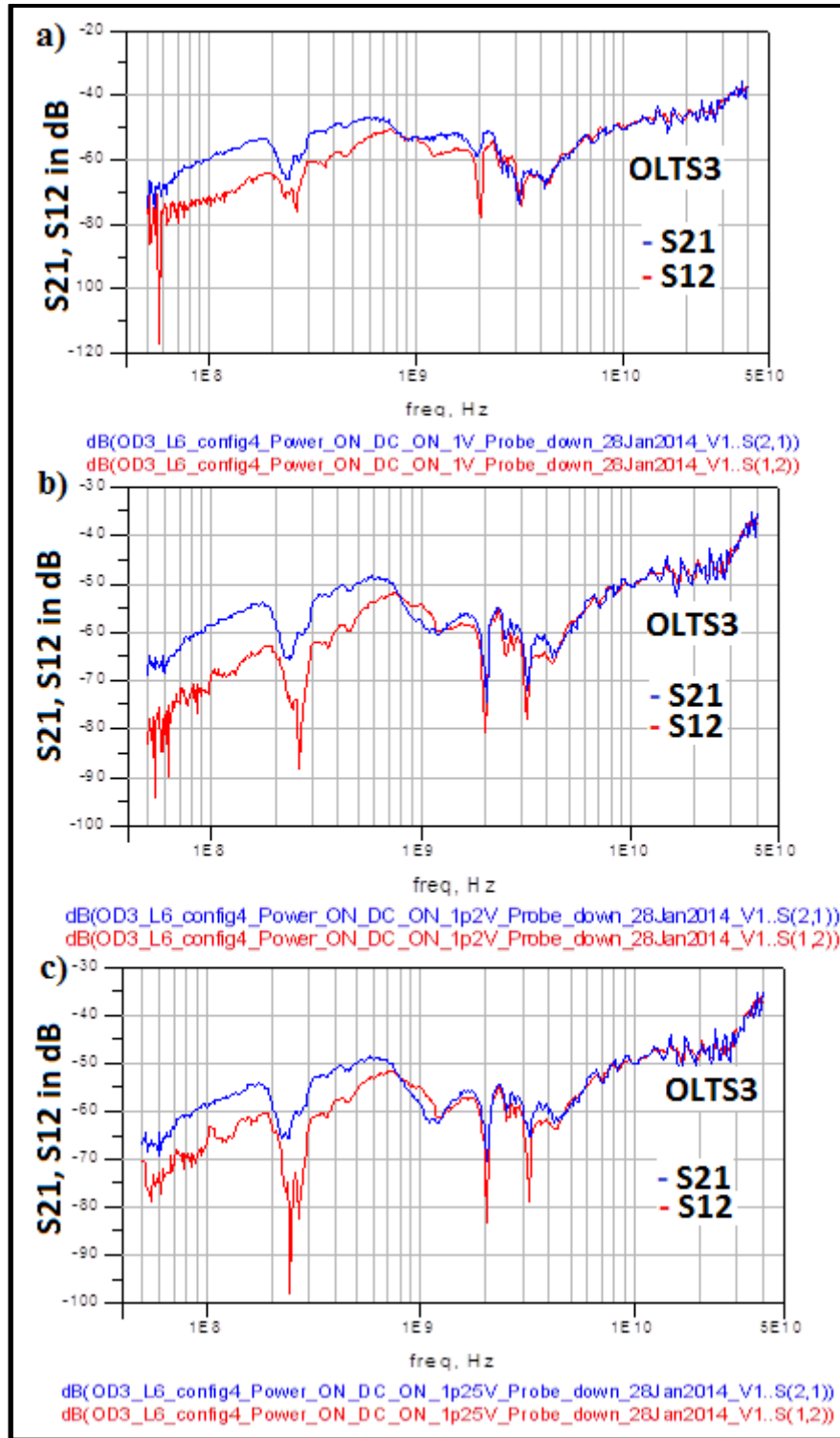


Figure 53: RF coupling results for the realized on-chip micro-optical link for OLTS3-RB at 1V, 1.2V and 1.25V different bias voltage conditions

# CHAPTER 5: Forward biased LED based Optical Links

## 5.1 Introduction

This chapter presents the DC bias analysis and characterisation of the optical link test structure of the forward bias configuration of OLTS3 (OLTS3-FB). The RF power analysis and characterisation of the on-chip optical link and the experimental confirmation results as well as the characterisation of the on-chip optical link and the AC experimental measurements of on-chip optical link, with Silicon-Nitride narrow core waveguide geometry been implemented and operating at 750nm are presented in this chapter. Lastly, a conclusive summary table indicating the main characteristics results of the three optical links test structures as designed is presented in this chapter.

### 5.1.1. Optical probing configuration on device 3 (OLTS3-FB)

The device under test is SiGe-based avalanche LED die (Wafer), with a size of  $1\mu\text{m} \times 1\mu\text{m}$ . It is mostly a pn photodiode from HBT structure. The light is coupled from the LED optical source through the Silicon-Nitride optical waveguides to the SiGe detector. The waveguide in this device is a Silicon-Nitride with narrow core of refractive index of ( $n=2.4$ ) surrounded by a TEOS1 oxide layer with lower refractive index of ( $n=1.46$ ) and of  $50\mu\text{m}$  length.

In this same test structure 3 (OLTS3), we carried out a forward bias analysis, the optical source LED was forward biased in this device configuration, and where carriers are energised through diffusion through a neutral low resistivity n material and the energetic carriers then dumped into the SiGe base causing transfer of carriers from the L to the T valley, which enable transitions with holes in the p SiGe base.

The RF probing of OLTS3 of the optical link is as shown in Figure 54. The source has four connections in order to have flexible connections. The signal and DC biasing are applied through the base, the emitter is grounded, and the  $n^+$  and  $p^+$  sink contacts are left open. The first ground of the probe is connected to the pad of a neighbor circuit on the chip. On the detector side, DC biasing and signal are applied through the base, itself short circuited to the emitter (thus, emitter contact is left open). The collector is grounded as indicated in Figure 54. This situation is different from the previous case. It is expected to reduce the substrate coupling by ensuring a ground voltage of the  $N^+$  sub collector region.

The optical probing of optical die 3 layer 6 (OD3\_L6) (OLTS3-FB) device is shown in Figure 54. In this configuration on the source side, the emitter was grounded, the DC biasing and RF power modulating input signal was supplied to the optical source of the device through the base contact. On the detector side, the DC biasing and signal was applied through the base contact with GSG probe tee, and the collector and emitter were grounded as shown in Figure 54.

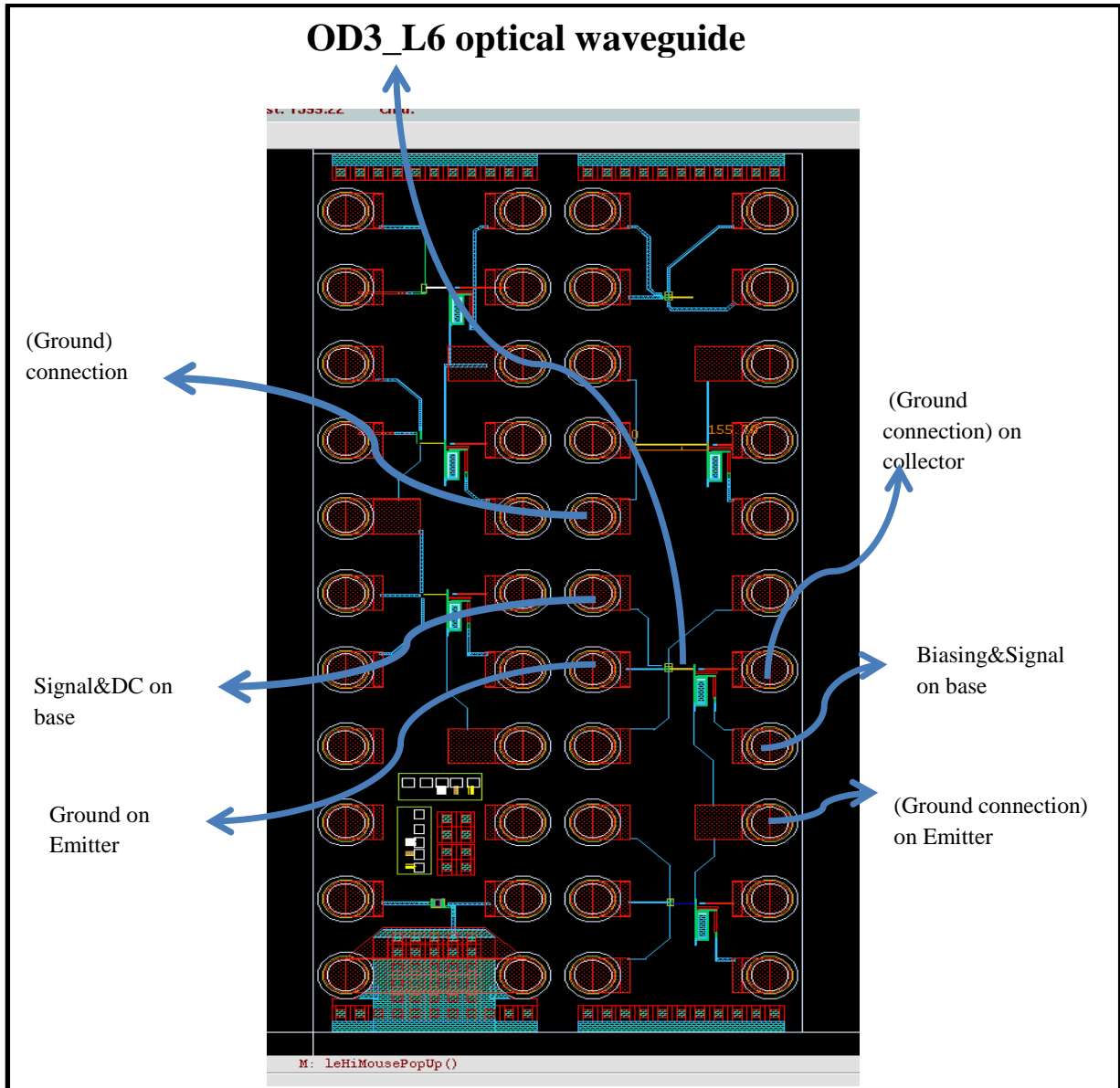


Figure 54: Device topology layout viewed with cadence design software (OD3\_L6-FB)

### 5.1.2 Procedures and test objectives

- Port 1 & Port 2 coupled; different configurations, see Figure 54
- Wafer: high resistivity, with nitride (no capacitors): Wafer was high resistance with reference (02A0)
- Minimised  $S_{12}/S_{21}$  when probes are up: calibration standardisation was done, and it was (-80dBm)
- Calibrated with the following: the RBW, the averaging, the VBW, number of points and smoothing off (during calibration). Averaging was set at 300 sampling points
- Frequency test range was: 50MHz – 40GHz at 401 points steps



- Noted reference number : Substrate run ,wafer and the chip reference number, with nitride or without nitride: 20Ω.cm or 2000Ω.cm substrate: was noted
- RF input power = -10dBm (100μW).

**Table 15: DC test biasing condition and compliance values for OLTS3-FB**

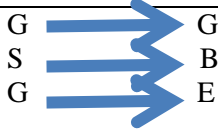
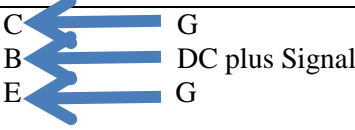
Conditions	LED Source.(Port 1of the B1500/VNA)	Detector.(Port 2 of the B1500/VNA)
DC biasing voltage (force)	[0 ; +1.2V], (on base)	-2V Fixed reverse bias (on B)
DC current (measured)	[0; 5mA] (I <sub>1</sub> )	+10nA (dark current); +0.1μA (I <sub>2</sub> )
Compliance	I <sub>c</sub> = 5mA	I <sub>c</sub> = 2mA
Current Directions	I <sub>p</sub> + (0 –10mA) outgoing for the LED; The B1500 measures a positive current	I <sub>c</sub> (10nA (dark current) – 0.1μA) Incoming into the HPT; The B1500 measures a negative current
Optical Probing		

Table 15 shows the bias voltage, the current values and the device designed compliance values during the experimental measurements. The direction of the current flow in the device is also tabulated in Table 15 above. During the experimental measurements on this test structure device OLTS3, the AgilentB1500A Instrument Analyser measured a positive current outgoing from the LED source and a negative current incoming into the HPT as recorded in Table 15.

**Table 16: Control parameters**

Conditions (RF Power ON all the time)	Expected results	Control Parameters
Probes up (with the biasing ON) [0V:1V] for Source [0V:-1V] for detector	$S_{21} = S_{12}$	DC currents; all S Parameters
Probes down (DC OFF)	$S_{21} = S_{12}$	DC currents; all S Parameters
Probes down (DC ON) (See Figure 54, test configuration)	What is $S_{21}$ , $S_{12}$ ?; $S_{21}$ curve is higher than $S_{12}$ up on till 1GHz frequency (optical coupling) but are almost the same at high frequency (RF oxide coupling)	DC currents; all S Parameters

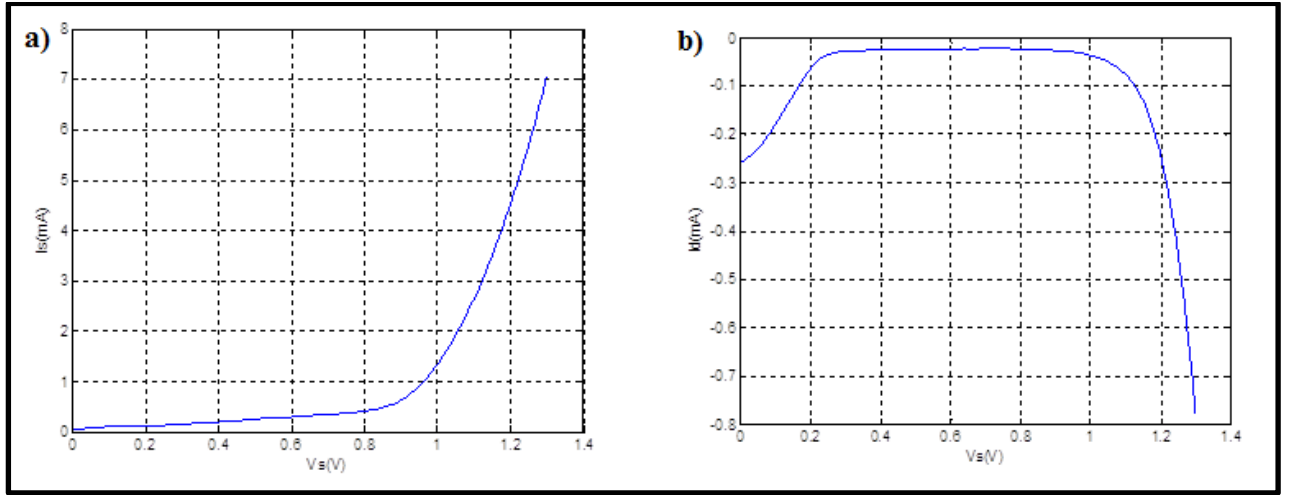
**Table 17: Measured results (RF analysis)**

<b>Conditions (Power ON all the time)</b>	<b>LED Source (V)</b>	<b>Detector (V)</b>	<b>Measured Results (RF analyses)</b>
Test 1	+1 on (p)	-2V Fixed (on base)	See Figure 56 (a)
Test 2	+1.3V on (p)	-2V Fixed (on base)	See Figure 56 (b)
Test 3	Peak (~ +1.4V) on (p)	-2V Fixed (on base)	See Figure 56 (c)
Test 4	(+1V; 1.4V)	-2V Fixed (on base)	No RF plots

### 5.1.3 DC bias analysis and characterization of the optical link structure OLTS3-FB

In Figure 55, the IV curve of the source as well as the correspondingly monitored link response IV curve on the detector side is shown, a detector current of about 0.8mA was detected by the detector at the onset voltage of 1.3V at the optical source when GSG probe was dropped down and connected to the device on the wafer (see Figure 54), DC on and RF power on. The DC IV curves were obtained at both the source side and the detector side for this test structure device, when the LED source was forward biased. It was observed that, when this device was placed in a forward bias condition, current flowed through the device up to about 6mA at 1.3V. The forward bias knee voltage was about 1.3V and the detector photo current link response was 0.8mA as shown in Figure 55 (a) and (b) respectively.

This observation hence confirmed that optical transmission did occur through the designed Silicon-Nitride waveguides narrower core at DC bias conditions from the optical source to the optical detector through the narrow nitride core waveguide surrounded by TEOS1 layer (OWGD3). This measurement further confirmed that, only with optical emission occurring at the source, that detector photocurrent of this several m-Amps (0.8mA) was observed for the optical link test structure OLTS3-FB shown in Figure 55 (b).



**Figure 55: DC IV Curves for OLTS3 (a) Forward bias Optical source IV curve (b) Detector optical link response when source was activated for OLTS3.**

#### 5.1.4 RF power analysis and characterization of test structure 3 (OLTS3-FB)

Figure 56 shows the RF results observed for OLTS3-FB, with the LED source device structure in forward bias mode. With forward biasing the structure p+n side and grounding the emitter contact region with the collector floating, a total optical link loss of only -40dB with quite a flat response towards higher frequencies was observed, this indicates that the optical emission from the source was of the order of two higher than in Design 1 (OLTS1) and Design 2 (OLTS2) (-35dBm). In addition, a clear drop-off in response was observed as a function of increased frequency, which is typical of signal shortage because of increased parasitic capacitance to the ground plane (Substrate) at the input associated with this device in forward bias configuration. This is to be expected, since a higher capacitance would be associated with the forward biased base-emitter region.

In this device, we observed very high DC photocurrent at the detector, but the RF shows high parasitic up to -40dB on both S21 and S12 curves. The S11 and S22 responses were correct and in line with the theory. Only at a frequency below 200 MHz, we observed slightly higher S21 than S12. With bias on emitter and bias at collector with the base shorted, we observed more or less the same results. For more confirmation of these results, we then tested the effect of background light by repeating some of the experiments in total darkness. I suspected induction of additional capacitance and photocurrent leakage in the substrate when the microscope light shines vertically down through the Silicon-Nitride layer into the structure. We saw that the S21 curve moved down by about 6dB. This somewhat confirmed the theory. We also observed a slight movement in the S12 curves.

We then switched off the source bias completely and repeated the RF coupling results. The results were quite surprising. The S12 and S21 curves moved completely down to -65dB below about 500 MHz, while the high frequency part at higher than about 1GHz stayed at -40dB. This confirmed induced parasitic capacitance in the substrate caused by the optical emission from the source itself. We repeated with both source and detector bias off. RF coupling results more or less the same with base RF coupling of -65dB at below 500MHz. We then analysed the low frequency part below 500MHz by zooming in on the curves. Ignoring the high S12 curve below 500MHz as observed earlier and by using the floor S12 as abodes reference, the results exactly correlates with previous results as obtained for this structure (with emitter contact lifted). I then suspected parasitic coupling in the substrate because of the light shining from the source itself. How else could S12 curves then be so high for all our analysed structures?

Nevertheless, -3dB cut-off frequency (half power point) of the order of about 500 MHz was observed for this specific design configuration as shown in Figure 56 (a), (b) and (c) at different bias voltage (0.8V, 1.1V and 1.2V) conditions respectively. The power consumption from calculated value at the input was about 2mW, indicating a power consumption of only about 0.1 mW per GHz. An optical link loss of -30dB was observed, but with a sharper fall off towards higher frequencies. Very prominent was the increased isolation that occurred at the lower frequencies.

*From our investigation, with forward bias configuration on this device, the optical source emission point was closer to the upper depletion region, which has a good lateral alignment with the waveguide core. With this, there was a higher optical coupling into the waveguide, which result to increase S21 to about 31dB (net optical coupling of about -35dB). This particular result is attributed to the higher capacitance as associated with the higher doped n+ -p junction, and because of an assumed better alignment of the optical source point acceptance angle with the waveguide core.*

Figure 56 (a), (b) and (c) shows the S21 (blue curve) and S12 (red curve) plots for a sweep voltage bias of 0.8V, 1.1V and 1.2V bias respectively at the source of the link device when RF input power was ON, DC bias was ON and GSG tee optical probe was dropped down on the device contact on the wafer and connected to this device test structure 3 (OLTS3) during experimental measurement. In Figure 56 (a), we observed that at 0.8V, S21 curve moved to -32dB and at about 600 MHz of coupling frequency. Again, in Figure 56 (b) at 1.1V, S21 curve moved up to about -31dB. From the observation, the difference between the S21 curve and S12 was better in dB values than at 0.8V and 1.2V bias voltage at source. We observed that the optical source emission was better and brighter at 1.1V bias voltage at source through the optical microscope.

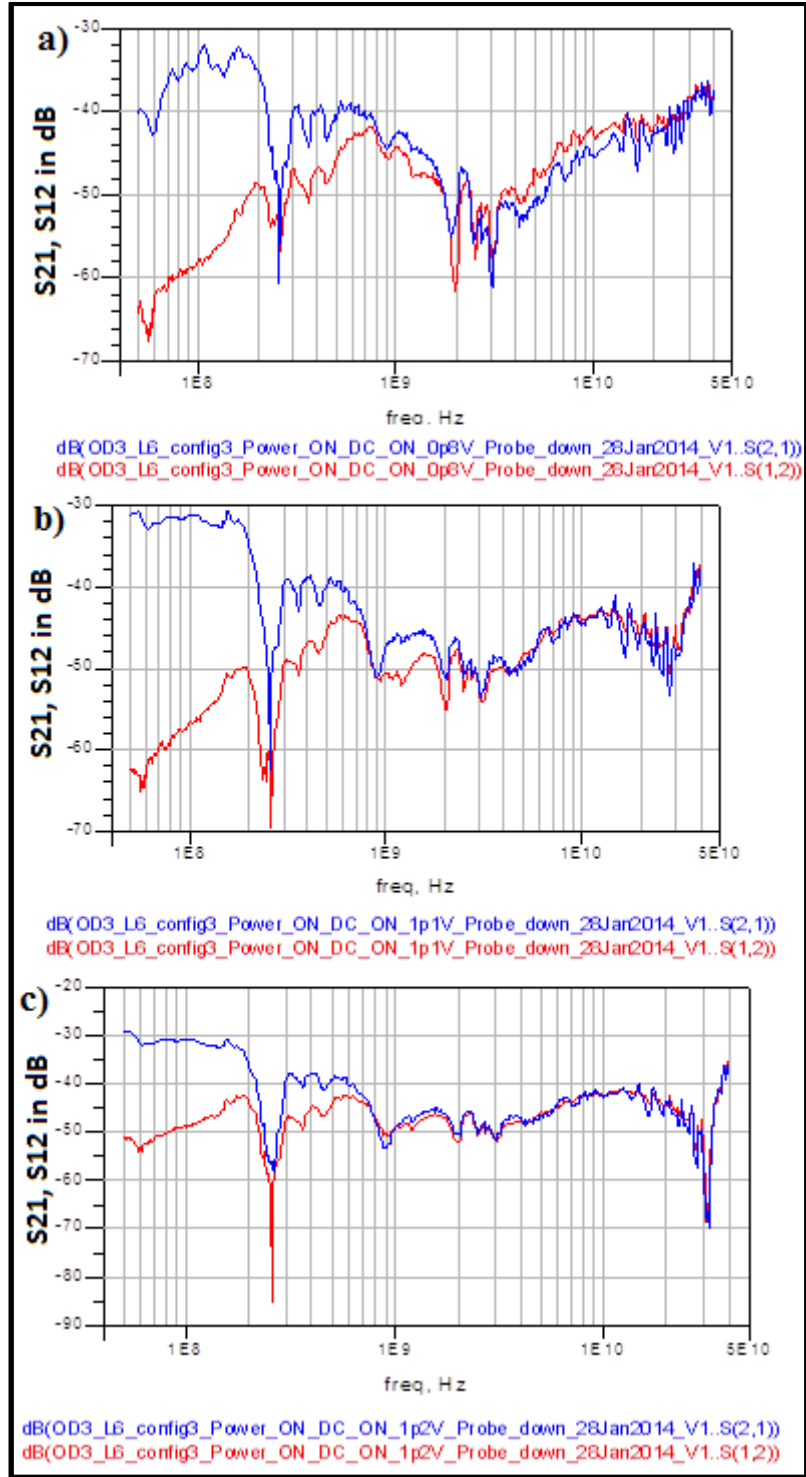


Figure 56: RF coupling results for the realised on-chip micro-optical link for OLTS3-FB at different bias voltage (0.8V, 1.1V & 1.2V) conditions

A table indicating main characterisation results for the three optical links test structures (OLTS1, OLTS2 & OLTS3) as designed is tabulated in Table 18.

**Table 18: Results summary of the designed optical links test structures (OLTS1, OLTS2 & OLTS3)**

LINK STRUCTURES	V <sub>s</sub> (V)	I <sub>s</sub> (mA)	P <sub>in</sub> (dBm) 100μw	V <sub>d</sub> (V)	I <sub>d</sub> = I <sub>c</sub>	LINK LOSS (dB)	OPTICAL WAVEGUIDE (Type)	f <sub>co</sub> (-3dB)	COMMENTS
OLTS1	-2.6	1.5	-10	+2	91nA	-50	OWGD1 TEOS1&2	10Ghz	Optical coupling swamped by high RF parasitic oxide coupling
OLTS2	1.36	3	-10	-2	95nA	-32	OWGD2	20Ghz	Schottky contact SiAvLED strategy
OLTS3-RB	1.36	5	-10	-2	80nA	-50	OWGD3 (narrow silicon nitride core, multi-mode)	1Ghz	Waveguide, good lateral alignment with optical source point
OLTS3-FB	1.3	5	-10	-2	0.8mA	-30	OWGD3 (narrow silicon nitride core, single mode)	500Mhz	Emission point closer to upper depletion region. Good alignment acceptance angle with waveguide

*In conclusion, the RF results observed for OLTS3-FB is shown in Figure 56, with the source of the device test structure in forward bias configuration mode. And forward biasing the structure p+ n side and grounding the emitter contact region with the collector floating. From our investigation and analysis, with forward bias configuration, the optical source emission point was closer to the upper depletion region which has a good lateral alignment with the designed nitride waveguide core. Hence a good optical coupling was observed through the waveguide to the detector. A total optical link loss of only approx. -40dB with quite a flat response towards higher frequencies was also observed; this indicates that the optical emission from the source was of the order of two higher than in Design 1 (OLTS1) and Design 2 (OLTS2) at low frequency up to about 1 GHz.*

*The other observation that we observed was that a seemingly oscillation occurred in the photo-detector (Photodiode), ADS simulation of the modelled device topology shows that for the particular detector bias configuration used, due to a slight error in our detector bias circuitry during design, leads to putting or diffusing holes into the base region and causing some photocurrent to flow in the detector which make the signal to have a phase shift. This was caused by simple feedback from collector to the base through an inherent RC circuit present in the device, causing a phase shift in the modulated signal.*

*From our analysis, we noticed that when there is 180 degree phase shift, this will cause full oscillation and about 90% signal phase shift will cause a partial oscillation which results in odd harmonics from big to small (3<sup>rd</sup>, 5<sup>th</sup> and 7<sup>th</sup> harmonics) respectively.*

*This unfavourable oscillation condition of the detector, resulting at higher frequencies makes the responsivity of the detector to be partially low and do not detect the optical light wave emission from the LED source at this circle. Hence there was no optical coupling at higher frequencies ( $S_{21} = S_{12}$ ) as seen in Figure 58.*

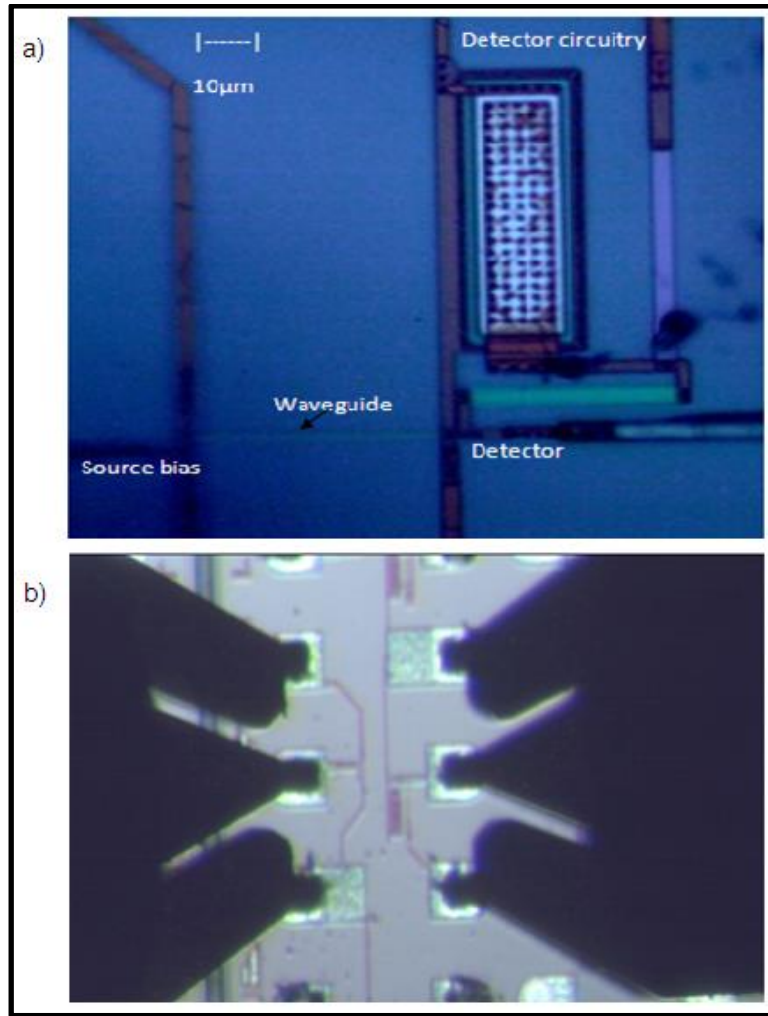
*Quite good first iteration optical coupling at 750nm wavelength from the source to the detector has been demonstrated from this work at both DC and AC level. However, again the forward biased configuration introduces high capacitance at the input of the optical source, which results in a reduction in allowable high frequency capability of the device due to parasitic capacitance effect as explained previously.*

### **5.1.5 Implementation of the optical links**

Monolithic IMWP circuit's approach that we used is by the combination on a single chip monolithic optical sources, waveguides and detectors. It is therefore required to have CMOS-compatible Si light emitting sources, detectors, optical waveguides and electrical interconnections. This integration will have the benefit of low cost multi functionality and reduced size of opto- microwave integrated circuits. The targeted applications are discussed in the next section, e.g: it can be biomedical analysis, microfluidic or Datacom.

Detectors and LEDs based on SiGe Bipolar technology are demonstrated in this thesis. A major stumbling block, however, is the RF coupling between the source and the detector in the on-chip optical micro-links which is tested and analysed using a vector network analyser (VNA) (50 MHz-40 GHz). The experimental setup described in Chapter 4 is used to characterize the links (from source via the designed waveguides to the detector). 200 $\mu$ m pitch GSG probes (shown in Figure 49 (b)) are used to connect the DC and RF input signals to the devices on the wafer. RF signal and DC biasing are applied on the source and detector sides through GSG probes via VNA internal tee bias. RF signal on the source modulates the optical power emitted from the source.

Figure 57 (a) shows one of the complete realised optical link test structures (Design 2), as it appeared with normal illumination conditions under an optical microscope with visible waveguide as indicated in Figure 57 (a). Figure 57 (b) shows the 200 $\mu$ m pitch of type ACP40W Ground-Signal-Ground (GSG) probes tee as connected in one of the device on a die (Wafer) from HP model 8510 (50Mhz-40GHz) vector Network analyser (VNA) during experimental measurements.



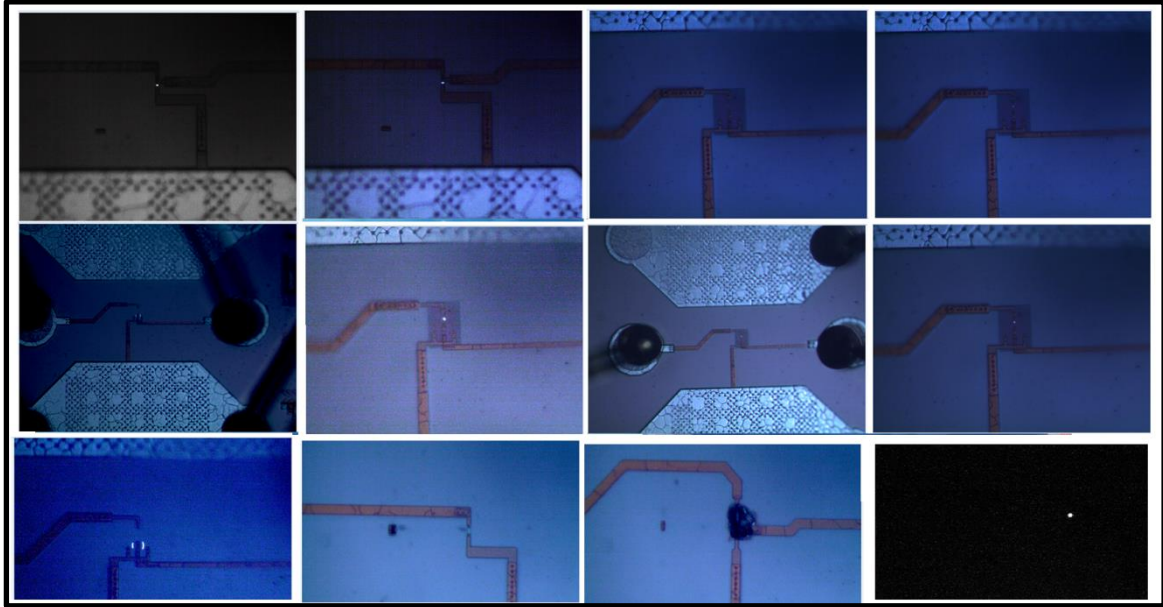
**Figure 57: : (a) Microscopic picture of the optical link device (b) Microscopic picture of G-S-G probe connection on one of the devices during measurement.**

The scheme is illustrated in Figure 57 (a) with scanning electron microscope (SEM) images of the actual device. As shown in Figure 57 (a), a Silicon-Nitride waveguide connects the optical output of a silicon electro-optic LED source (see Figure 57 (a)) to the optical input of a waveguide-integrated germanium detector (see Figure 57 (a)). In an interconnect system, the electrical input of the LED source and the electrical output of the detector of such a link was both connected to microelectronic circuits, GSG optical probe for DC biasing and RF power modulating signal.



### 5.1.6 Galleries' of bright field micrograph of top illumination of our LEDS

Figure 58 shows some of the bright field micrograph top illumination of our LEDs, during experimental measurements under DC bias conditions. The bright spot of the optical source point of the over layer LED, epi-layer LED and grade-junction LED is visible as shown in Figure 59 below.



**Figure 58: Microscopic picture of bright spot LEDs optical source points of some of the devices**

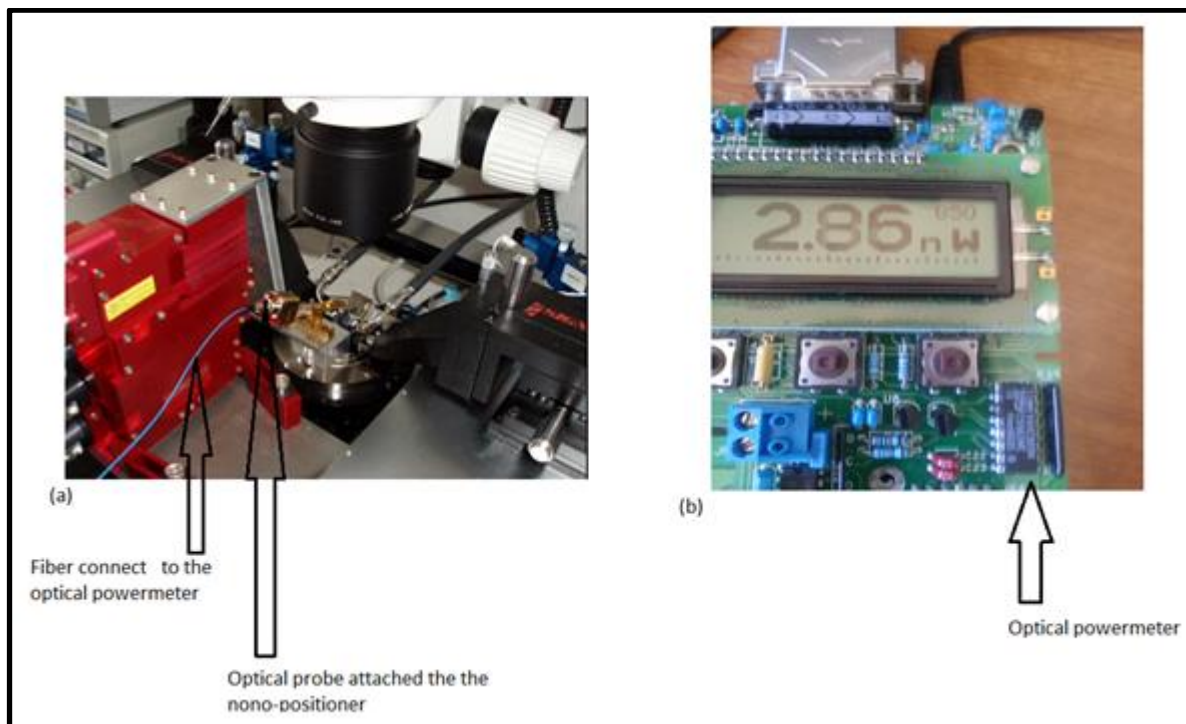
### 5.1.7 Localization of the optical LEDs source point for optical coupling optimization

Localization of the emission source point process is important because, knowing the optimum optical source point of the LEDs will help to align the waveguide core to this point, which will increase the optical emission-coupling factor to the designed waveguide and to the detector. In the edge emission from the LEDs, we intend to detect the light emission source point from the edge by two techniques in order to ascertain the source point and nature of light emitting process, and hence locate the maximum emission point. Two techniques were used here to achieve the goal.

- 1) Optical probe through fiber to optical power meter.
- 2) Mapping diced optical source with optical probe (sweep area,  $40\mu\text{m} \times 40\mu\text{m}$ ;  $60\mu\text{m} \times 60\mu\text{m}$ ) to localize emitting source point region.

In Optical probe through fiber to optical power meter techniques, Figure 59 shows the photographs of the bench setup with the required fibre mounting modifications to characterize edge-emitting LEDs. All the connections, except the axis of light emission, are similar to the bench setup described above. To extract and locate the maximum emitting point of the broad spectrum LEDs source, we use a horizontal optical probe supporter to point the optical probe on the side of the diced device source from the wafer as shown in Figure 59 a). To control the position of emission we attach the optical probe with the nano-positioner, so that we can move the fibre in a well-controlled way. Figure 59 (a) shows the microscopic picture of the device under test along with the optical fibre on the side. From this view, we can control the movement of the fibre along  $x$  and  $z$ -axes. In the same picture, we can clearly observe the base and collector contacts of the device through RF probe. By using this view, we can control the movement of the optical probe along  $y$ -axis.

Figure 59 (b) is the optical power meter displaying the power emission value in one of the test measurement of 2.86nW.

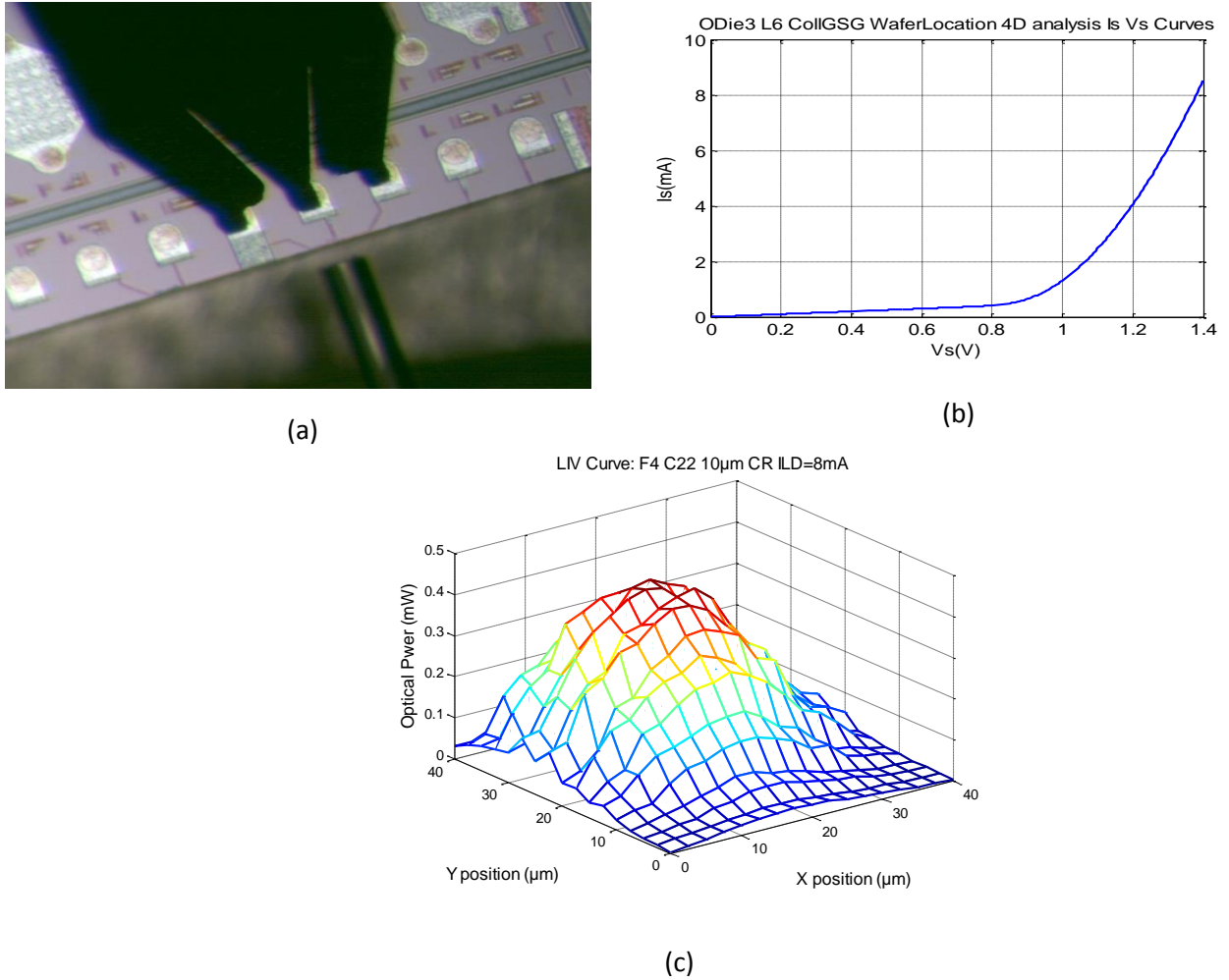


**Figure 59: Experimental bench setup of edge emitting LEDs. (a) Photograph of the bench. b) Picture of the optical power meter.**

From this technique, we could ascertain the point with the highest light emission from the diced LEDs source. This will help us to design a more efficient, effective and better BiCMOS silicon on-chip optical links test structures at 750nm wavelength.

The second technique is the mapping of the diced device with the optical probe. Before we begin the method, we first define the LED device operating parameters. In one of the device, optical die 3 layer

6 (OD3\_L6) operating parameters were defined as fixed 2mA, compliance current 10mA, 1.4V, wavelength 850nm. The properties of the fiber used was fiber diameter 125mm, fiber core is 9μm.



**Figure 60: (a) Top view microscopic picture of the device under test and the optical probe pointing on the edge side of the LED source (b) IV bias curve of the device under test (c) LIV power measurement curve of the device**

From Figure 60 shows the microscopic picture of one of the device under test with the required fiber optical probe-mounting modifications to characterize edge-emitting LEDs. All the connections, except the axis of light emission, are similar to the bench setup described above. To extract light on the side, we use a horizontal optical probe supporter to point the optical probe on the side as shown in Figure 60 (a). To control the position of illumination we attach the optical probe with the nano-positioner, so that we can move the fiber in a well-controlled way. Figure 60 (a) shows the microscopic picture of the device under test along with the optical fiber on the side. From this view we can control the movement of the fiber along  $x$  and  $z$ -axes. In the same picture, we can clearly observe the base and collector contacts through RF probe as shown on top of Figure 60 (a), using this view, we can control the movement of the optical probe along  $y$ -axis.

Figure 60 (b), is the current-voltage characteristics (IV) bias curve of the device, this curve gives the indication that the device under test is biased properly, and that it is in good working condition. Figure 60 (c) shows the light –current-voltage (LIV) power measurement curve of the device under test.

From Figure 60 (c), we observed that the optical power of the LED source was around 0.3mW. However, this experiment still need to be re-investigated in other to confirm these results

## CHAPTER 6: Conclusion

The following major conclusions can be derived from the work as presented in this study:

1) The designed Silicon-Nitride based waveguide technology as demonstrated in this study, together with the choice of 0.75  $\mu\text{m}$  operating wavelength, show new routes of both development and applications for the field of silicon photonics technology. It indicates an important spin-off of this technology towards low cost, miniaturisation and ease of fabrication of photonics systems. The major advantages of utilizing 750nm wavelength are the ease of integration of the optical source, the waveguide and the optical detector all in the same chip with ease of design and processing procedures. Utilization of Si-Ge detector structure at 0.35 RF bipolar process, of course offers superior high RF operating frequency than other CMOS detectors.

2) The utilization of SiGe detector technology in association with the high modulation characteristics of Si Av LEDs, particularly, demonstrates potential incorporation of these devices in standard RF bipolar or CMOS microelectronic processing platforms. Utilization of the designed TEOS, the  $\text{Si}_3\text{N}_4$  based waveguides, and employing the advanced columnar processing capabilities as offered by the RF bipolar process as developed in this study, offers the design of a wide variety of second iteration and optimised waveguides structures between the optical source and the detector using this technology.

3) In this study, good optical coupling in on-chip optical links were realised at DC levels (detectors photo current links response was 91nAmps, 95nAmps and 0.8mAmps respectively). This in itself can open up a completely new paradigm and family of systems development in both CMOS and RF bipolar microelectronic design and processing platforms. To our knowledge, we have achieved the first optical coupling between a Si Av LED and a Si-based detector, which involves a dedicated silicon wave guiding structure at DC bias conditions.

A clear and definite DC detector photo-current link responses were obtained for four test structures ranging from nano-Amps (nA) to m-Amps (mA) coupling for input powers of 100 $\mu\text{W}$  to 10mW at the Si LED sources.

4) The waveguide technology designed as demonstrated offers diverse application possibilities for diverse micro-sensing and micro-phonic on-chip systems developments in which optical communication and data transfer plays an important role. Moreover, because of very high flexibility of design, low production cost at large scale and monolithic integration with other components, this silicon light source-Silicon-Nitride waveguide-photodetector can be integrated into CMOS technology platform. The on-chip optical links device as realized in this work is one of the best choices which can

be used as the optical link for optical interconnect application in modern optoelectronic CMOS integrated circuits.

5) The forward biased, micro-dimensioned Si-Ge light emitters, Silicon-Nitride waveguide in (OLTS3-FB), as demonstrated in this work particularly, demonstrates high optical source emissions, leading to reduced total link power budget to about -30dB, at even lower power consumption rates, since only 1V and few mA's (3mA) are required to operate these devices. Substantial further development work, however, still needs to be performed. Quite good first iteration on-chip optical coupling operating at 750nm wavelength from the source to the detector has been demonstrated from this work at both DC and AC level respectively. However, we observed that the forward biased configuration introduces high capacitance at the input of the optical source device, which results in a reduction in allowable high frequency capability of the device due to parasitic capacitance effect.

6) The utilization of Si Av LED's shows indications of achieving low cost effective, high frequency micro on-chip optical links. Positive results have been achieved for two structures: (i) Schottky contact Silicon Avalanche Light emitting diode (Si Av LED) shows reduced input oxide parasitic capacitance and definite high frequency optical link up to 23GHz and achieve 3dB cut off frequency of 3GHz. (ii) Results for Silicon Germanium (Si-Ge) p+ n, Si Av LED's shows definite indications of achievable high frequency optical link coupling up to 10GHz with 3dB cut off frequency of 1GHz.

7) In overall in this study, the best result of on-chip link optical coupling up to 10GHz has been achieved at 650nm-850nm operating wavelength using a RF Si-Ge bipolar process. The cost factor per optical link is difficult to determine at this stage, but it is estimated from our trivial calculation to be at least a factor of  $10^{-3}$  less than the one of more complex group III-IV technologies. The closest similar results of the above nature have been reported by [76], but only they used 1500nm operating wavelength technology, external laser source and no on-chip optical source was use, and focus on the utilization of external laser sources.

The achievements of this study as demonstrated, therefore, can with respect to the development in RF Bi-polar process an on-chip optical coupling between Si Av LEDs and SiGe detector through dedicated on-chip Silicon-Nitride waveguide structure operating at 750nm wavelength, can be regarded as significant and novel technology. It is a definite first internationally in production couple on-chip optical link at 750nm wavelength (half of 1500nm) and which realised the complete optical link on-chip at this wavelength including the source, the waveguide, and the detector designed to dimension of micron sized circuit elements, all integrated on the same chip. No other similar technology realisations or even patenting of similar nature could be cited in RF bipolar process and in CMOS technology process procedures' platform.

In summary, the main strategies employed in achieving the full Silicon optical links device are:

- (1) The design and simulation of the waveguides in full Silicon structure with RF bipolar processing platforms at 750nm. This was based on Telefunken GmbH SiGe HBT technological processes. The full optical link combines Silicon Avalanche based Light Emitting Devices (Si Av LEDs), Silicon-Nitride based waveguides and SiGe HPT.
- (2) The analyses of the optical light wave propagation through these waveguides by means of R-SOFT suites simulation packages.
- (3) Using the ADS package, the RF simulations of the device two-port equivalent network topology modelled hypothetically and eventually, the complete designed of full on-chip optical link structures comprising Si Av LEDs, dedicated Silicon-Nitride waveguide structures and SiGe detectors based on Telefunken GmbH SiGe HBT technological processes platform.
- (4) The development of the MATLAB voltage biasing codes that interface the measuring instruments hardware and the analyses techniques in measuring the real optical propagation and RF parasitic coupling effects and needed for analysing these structures.

All of the above contributed towards the DESIGN, the REALISING, the CHARACTERISATION, INTERPRETATION OF RESULTS and eventual PRESENTATION of the developed technology as demonstrated in this thesis, as well as the INTERNATIONAL RECOGNITION by peer researchers is considered as novel and original contributions.

8) Challenges experienced during this study were the following: That ON-CHIP micro optical link designs in SiGe bipolar process and CMOS technology, suffer from high parasitic RF coupling as a result of both coupling that occur through the silicon substrate as well as through the isolation oxide over layers.

An in-depth analysis has been made in this study and the detailed topology two-port equivalent network structural elements responsible for the parasitic coupling have been identified. This will enable future researchers to optimize next iteration designs and achieve less parasitic coupling and optimise higher optical coupling signals in such device.

From this work, three conference proceedings papers were presented at front-end leading international conferences during the latter two years (SPIE Photonics West, San Francisco California; SMEOS in South Africa and four journal article papers published.

## THESIS PERSPECTIVES AND RECOMMENDATIONS:

Regarding the thesis perspective and recommendations for further studies, the following are suggested: The detail analysis of the optical intensity, polarisation, propagation modes, and phase analyses of the optical wave light in this work, can all be the topics of future research and coupled with these following suggestions:

- The designed Silicon-Nitride based waveguide technology as demonstrated in this study, together with the choice of 0.75 micron operating wavelength, show new routes for both development and applications for the field of silicon photonics technology, or at least indicate an important spin off of this technology towards low cost effectiveness, the ease of fabrication and the integration into CMOS technology platform systems. The major advantages of utilizing 750nm wavelength are the ease of integration of optical source, the waveguide and the optical detector all in the same chip with ease of design and processing procedures. Utilisation of SiGe detector structure with 0.35 RF bipolar processes, of course offer superior high RF operating frequency.
- In this study, the techniques and strategy employed in the Si Av LED design, the optical waveguide designed using the material coerture geometry and the refractive-index properties of the available TEOS oxides and the Silicon-Nitride material, and couple with the optically transparent of these materials at 750nm wavelength were proven to be a success. But however, the optical source to waveguide optical coupling can be improved by refinement of optical wave-guiding in terms of the waveguides design geometry dimension for wavelength range of 700nm-800nm in CMOS Silicon-Nitride ( $\text{Si}_2\text{N}_3$ ) layers and couple with improve engineered Silicon-Nitride waveguide by geometrical and graded refractive-index optimization techniques. In our first on-chip optical links iteration design, localization of the optical source point was not optimised in terms of lateral coupling into the waveguide, which results in optical emission losses between the optical source point and the waveguide interface, but if optimised, more wave light will couple into the lateral waveguide. In addition, more also, through the optimization of the waveguide transversal dimensions and the refractive indices in a multi-cladding arrangement, more optical wave light can be coupled into the adjacent lateral structure. Determining the optical source emission point can be done through using optical fibre probe spectrum power mapping techniques that will give optimal source coupling point and minimum loss between the optical source point and waveguide interface, and optical loss through the waveguide.
- During the course of the experiment, we noticed that there was a typical refractive index fluctuations as well as dimension fluctuations during the fabrication of the



Silicon-Nitride waveguides, which we believe were a limitation for obtaining a good optical coupling of the emission light in the waveguide to the detector due to losses long the waveguide through micro material scattering. With a well-designed and appropriate waveguide diameter thickness optimization and improvements in waveguide quality, the waveguide propagation loss can be reduced drastically, thereby increasing optical coupling through the waveguide to the detector. This low propagation loss couple with the large refractive index contrast between Silicon-Nitride and silicon dioxide can enable high density integration of photonic devices and small PLC's for a variety of applications in photonic sensing and optical communications. Thus, if the  $\text{Si}_3\text{N}_4$  waveguide layer is optically isolated from the lossy Si substrate, it can guide the visible light without significant loss in this wavelength range.

- If the optical link device designed could be masked correctly during Cadence design layout face, and the fabricated device diced precisely at the centre, to help expose the source optical point side illumination through using optical fibre probe, via optical fibre to the optical power meter and spectrum analyser, the complete spectrum and optical power of the Si Av LED source can be obtained through well-defined spectrum power mapping techniques.
- The optical source point emitting region of the Si Av LED used in these designed optical link structures could be localised to optimize the nature and intensity of light emitting process, and this could further increase the optical coupling between the source and the waveguide interface.

The low optical signal through the designed waveguides to the detector during our measurement was attributed to high parasitic capacitance in our optical link structures, which was due to the chosen RF bipolar processing procedure and our chosen design waveguide dimensions during design and we were limited by the device contact probing configurations during experimental measurements to obtain the desired results of high optical links through the waveguides.

From our investigations, the large reverse biased isolation regions of about 50 micron square present in our device structures was seemingly greatly contribute to RF induce parasitic coupling through the substrate at source activation and kills both the low as well as the high frequency response at the higher ends. In addition, the long low resistance p+ channel stop implant regions in the centre of the optical links contributes towards high substrate parasitic RF coupling.

In general, we can improve our results by in future avoid biasing both the detector and source through the substrate and rather keep the substrate at the same ground and only bias the device on top of the pillar structures.

These parasitic capacitances have the tendency to kill the signal and drain it through the substrate via to ground. Minimising the parasitic capacitance in the optical links device structure could increase the optical wave light coupling through the designed waveguide.

- In our first device contact measurement configuration, when signal was supplied through the top contact points of the device, most of the signal was drained through the substrate due to poor isolation error during the cadence software design stage of the device link structure, especially in OLTS2. In addition, because of this deficiency, the optical wave light coupling was swapped or dominated by this substrate and oxide coupling, thereby reducing the optical coupling through the waveguide. From recommendation point of view, this deficiency could be avoided or rectified by accurate and precise isolation process during cadence software design of the optical link device structure.
- From our analysis, the waveguide material refractive index also show indications of fluctuation as wave light propagates through the designed waveguide, thus this fluctuation effect small scattering of optical wave light into the surrounding oxide, thereby reducing the optical coupling through the waveguide. This negative effect can be minimised by designing a waveguide by implementing micro graded refractive index techniques which reduce optical wave light scattering along the waveguide, which will increase more optical coupling through the waveguide.
- More also, when we modelled, investigated and analysed the two-ports equivalent network topology of the complete optical link devices; we discovered that there was a series of internal capacitance and resistances present in the depletion regions, and the isolation semiconductor materials with the substrate of the optical link device during experimental measurements.

From our analysis, these parasitic capacitances and internal resistances in the device form a component elements network of high pass and low pass filters like in nature to the propagating signal through the device structure. From our analysis, these parasitic capacitances kill the signal and tend to increase oxide coupling through the substrate and the over layer oxides, thereby dominating the optical wave light coupling, and the optical coupling was swamped by the high oxide and substrate coupling.

At a low frequency, the low pass filter component element allows the signal with low frequencies components to pass through and tend to stop high frequencies signal component, and thereby forming or producing a curve of power in dB against frequency

in Hz of a low pass filter (Poles) and curves of a power in dB against frequency in Hz of a high pass filter (zeros). However, from our analysis, when poles and zeros are present at the same time, they tend to cancel each other and produce a flat curve of power in dB, and when double poles or double zeros are present, the device acts more as a low pass filter or a high pass filter respectively. In our device optical link design, there were fewer poles than zeros; hence, the optical coupling curve that was generated was swamped and dominated by the parasitic capacitance effect.

This analysis indicates that there would have been a better optical coupling from the source point through the waveguide and to the detector if the above deficiency were eliminated through a better recess or extended channel stop isolation structures were used in the SUBSTRATE of the designed device structures with the RF bipolar process. This could increase the optical coupling from the source through the waveguides to the detector.

- A major design deficiency in our current optical link structures was the incorporation of the P<sup>+</sup> isolation box between the Si Av LEDs source and the detector in the silicon substrate. From our analysis, this highly doped P<sup>+</sup> material lowered or reduced the resistivity of the silicon substrate, which increase the substrate coupling and drain the signal to ground during experimental measurements. In future, the P<sup>+</sup> isolation box embedded in the P-substrate should be avoided, and this could increase the resistance of the substrate and prevent substrate coupling between the Si Av LEDs and the detector in the device, this could positively improve the performance of the optical link device drastically.
- During our experimental measurement, we reviewed the device cadence layout and discovered that the collector terminal of the detector was out of plane, and that there was a slight short circuit between emitter and the base terminal in our detector bias circuitry, and these were errors that occurred during both the design stage and device fabrication' phase. This error thus limited the correct bias configuration of the detector with the GSG probe, which would have yield a better waveguide alignment interface coupling to the detector maximum response point to produce a much better optical coupling from source through the designed waveguide to the detector. All of the current coupling analyses could only be conducted with the detector in photodiode mode. From recommendation point of view, this design error can quite easily be avoided in future design by avoiding short circuiting the detector emitter-base terminals and by applying accurate and precise design strategy. If successful design in this regard, it would also be possible to operate the detector in a phototransistor mode which will increase the

front end gain in the detector at high RF frequencies and reduce the overall coupling factor by a factor of 10dB to 20dB in some cases.

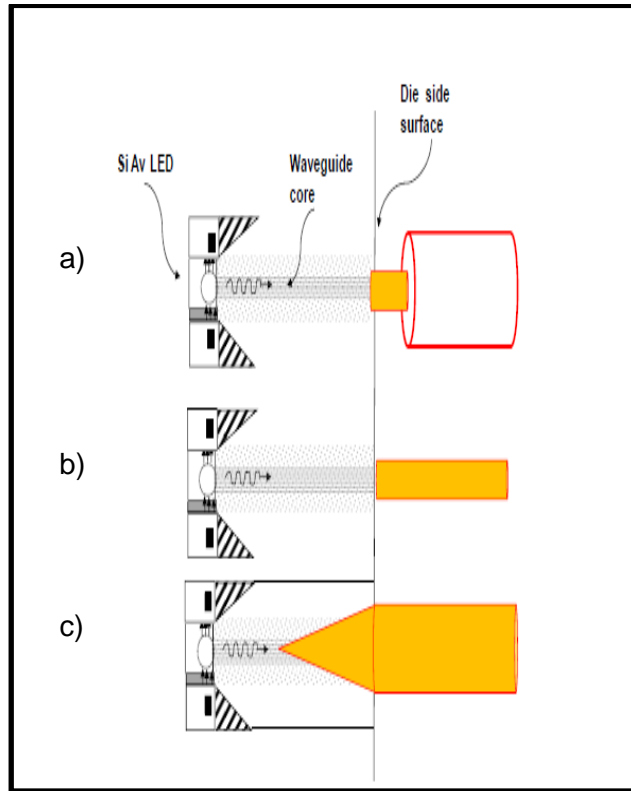
- In overall, more advanced detailed optical propagation modes, optical modal analysis incorporating phase effects as well as optical polarisation analysis can in future be utilised in order to improve waveguide design and the simulations processes.

# APPENDICES

## I. Potential applications of the developed technology

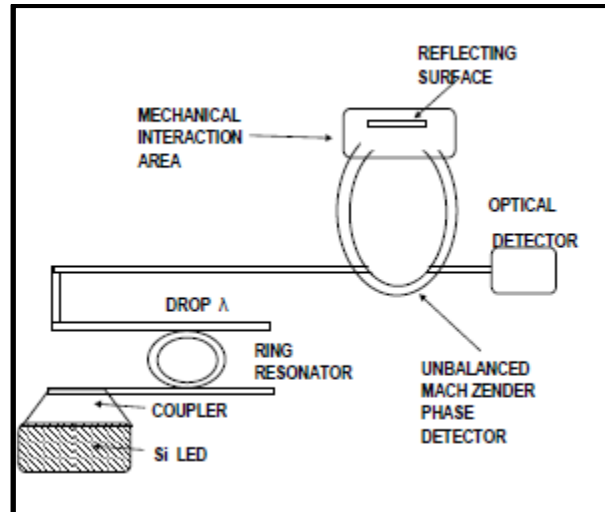
Some of the areas where this technology could be used are presented as follows:

- 1) This technology could be used as optical on-chip inter/intra optical interconnect and to optical fibre interconnects.
- 2) This technology can also be used on biosensors which involve absorption analyses, or rate of absorption change or absorption pulsation which can reveal content about the material composition and constituents using the evanescent field of the designed waveguide. Flow rate or other physical parameters as associated with the fluid with Optical Bio photonics-sensors can be measured and analysed.
- 3) [54], Proposed an H-shape configuration waveguide and 0.35  $\mu\text{m}$  wavelength technology system for clock pulsing in CMOS on-chip subsystems. The waveguide technology as described in this work could substantially augment and add a new dimension to this proposal. Given its realization of on-chip optical sources, key constituents of such a system is an effective compatible optical source, compatible optical wave guiding, effective optical coupling from the source to the waveguide and optical columnisation circuitry, which all seems to be highly viable from the present analysis of the proposed technology designed.
- 4) Concerning realization of optical inter-connects to chips; we propose the fibre optical links with designed waveguide technology as demonstrated in Figure 61. Figure 61 (a) shows a schematic diagram of the Si Av LED optical source point, the aligned lateral waveguide core interfacing to an external optical fibre for optical communication purposes. The main application of this type of technology is to directionally channel light from the internal on-chip IC to the external in an integrated form at low power and low cost for short-range optical communications. Figure 61 (b) and (c) are possible on-chip structural design geometries to optimize the optical coupling of the emission from the optical point source into the optical waveguide.



**Figure 61: Schematic presentations of potential application of the developed technology in the optical interconnect environment, utilizing a 0.35  $\mu\text{m}$  SiGe process technology**

- 5) The developed technology can be applied to realize various on chip micro photonics systems such as MOEMS and MEMS. The realization of diverse other CMOS based micro-photonic systems as well as the incorporation of a whole range of on-chip micro-sensors into CMOS technology are also most viable with our technology as developed. It can be used in Micro-Opto-Electro-Mechanical Systems (MOEMS) sensors, lab on-chip technologies as well as in bio-medical micro sensor applications. In most cases, it merely implies a transfer of technology as developed in other systems. The advantages are achieving high levels of miniaturization, higher reliability levels, a vast reduction in technology complexity and drastic reduction in cost of producing such associated systems.
- 6) A proposed conceptual MOEMS sensor design is shown in Figure 62 below.  
Figure 63 shows a conceptual MOEM sensor device that is suitable for integration in CMOS integrated circuitry using all monolithically integrated circuit technology. The device consists of an integrated circuit Si LED, a silicon detector and electronic signal processing circuitry all integrated in CMOS integrated circuitry, then a wave-guiding track, which interfaces with an environmental parameters section.



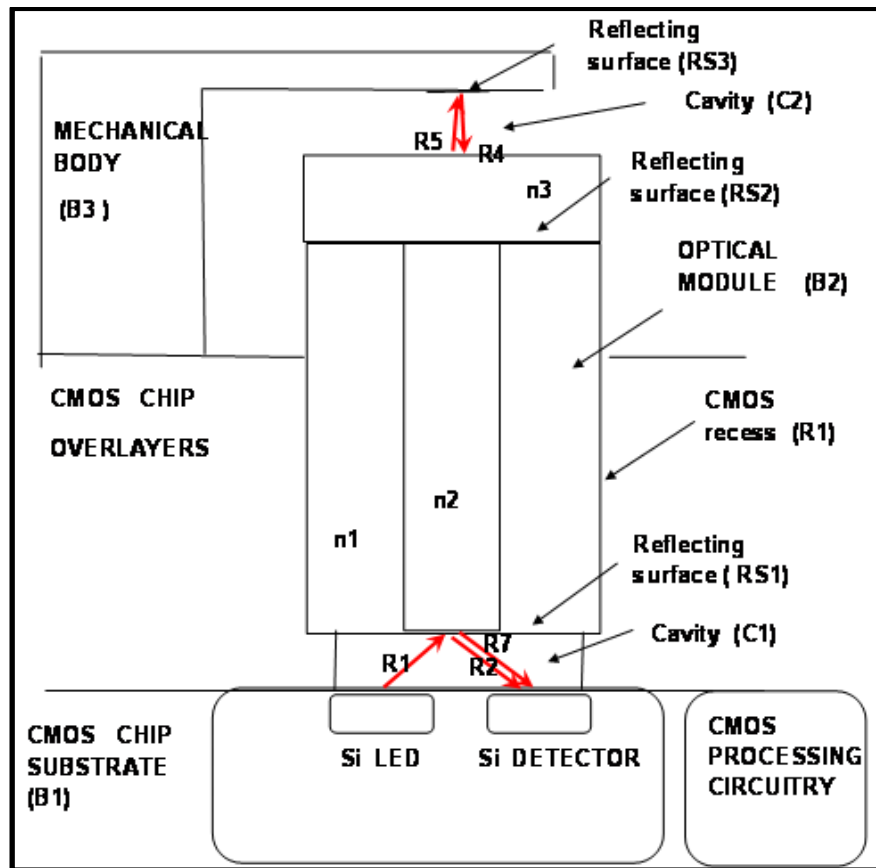
**Figure 62: Conceptual MOEMS sensor device suitable for integration in CMOS IC using all monolithically IC technology (Snyman&Ogudo et al, 2015)**

The Si LED, wave guiding elements, as well as an environment interface section is all integrated monolithically on CMOS integrated circuitry. If necessary, appropriate filtering and phase contrast detection elements such as Mach Zender elements can be included in the design.

The above device is a typical example of a new generation of “smart” sensors that can be integrated with ease in CMOS integrated circuitry using monolithically technology form into CMOS integrated circuitry.

The directional emission of radiation, both vertically out of the CMOS structures as well as the lateral wave guiding of optical signals are important. Therefore, the optical waveguides developed in this work have great value.

- 7) Figure 63 demonstrates a conceptual MOEMS sensor device that is suitable for integration in CMOS integrated circuitry using hybrid technology. The device consists of an integrated circuit Si LED, a silicon detector and electronic signal processing circuitry all integrated in CMOS integrated circuitry, then an optical module is picked and placed in a recess structure in the CMOS over layers and then a small mechanical module with a reflective surface which is finally picked and placed on top of the optical module.



**Figure 63: Conceptual MOEM sensor device that is suitable for integration in CMOS IC**

The optical module is made up of a simple optical fibre type technology and a thin layer of different refractive index is facilitated on the side of the structure. Basically, the optical module transfers optical signals from and to the environment where the signal undergoes modification, with respect to either intensity, position, or phase contrast by means of the mechanical module, and these changes are detected by the detector module, which is integrated in the CMOS integrated circuitry. In the cavity, C2, a variety of further principles can be applied, viz, optical absorption measurements, fluid flow experiments, gas flow experiments aided with fluorescence's, etc. The potential applications are diverse and can link with new emerging fields such as bio and nano-technology.



## II. Scientific publications that emanated from this work

### International Journal Article Published:

[1] Kingsley A.Ogudo\*, Diethelm Schmieder, Lukas W. Snyman (Tshwane University of Technology, South Africa) and D. Foty, *SPIE MICRO/NANOLITHOGRAPHY, MEMS, AND MOEMS (JM3)*-4<sup>th</sup> January 2013, Bellingham WA 98227-0010, USA.: J. Micro/Nanolith. MEMS MOEMS 12(1), 013015 (Jan–Mar 2013) [DOI: [10.1117/1.JMM.12.1.013015](https://doi.org/10.1117/1.JMM.12.1.013015)] ***“Optical propagation and Refraction in Silicon CMOS Structure at 750nm; Realization of an on Chip optical Link”*** : (Gilgamesh Associates, USA

[2] Lukas W. Snyman, *Member, IEEE*, Kaikai Xu, Jean-Luc Polleux, Kingsley A. Ogudo\*, *Member, IEEE*, and Carlos Viana. *IEEE Journal of Quantum Electronics*, Vol.51, No.7, July 2015. *Impact Factor: 2.11 · DOI: [10.1109/JQE.2015.2427036](https://doi.org/10.1109/JQE.2015.2427036)*  
***“Higher Intensity SiAvLEDs in an RF Bipolar Process Through Carrier Energy and Carrier Momentum Engineering”***

[3] LW Snyman, JL Polleux, M Du Plessis, KA Ogudo\* : *IEEE Journal of Quantum Electronics*, DOI 10.1109/JQE.2017.2736254 ; Vol 53 Issue 5, October 2017  
***“Stimulating 600-650 nm Wavelength Optical Emission in Monolithically Integrated Silicon LEDs through controlled Injection-Avalanche and Carrier Density Balancing Technology”***

[4] X Kaikai, KA Ogudo\*, LW Snyman, H Aharoni, *Optoelectronics and Advanced Materials, Rapid Communications* Vol.11 (3-4), March-April 2017, p.164-166  
***Silicon light-emitting device for fast optical interconnect and fast sensing applications in the GHz frequency range in standard IC technology***

### International conference presentations and published conference proceedings articles:

[1] Kingsley A. Ogudo\*, Lukas W. Snyman, Jean-Luc Polleux, Carlos Viana and Zerihun Tegegne, *PROCEEDINGS OF SPIE PHOTONIC west 2014*, 1-6 February 2014, Moscone center San Francisco USA. Tracking Number: OE112-5; doi: 10.1117/12.2038079. Proc. of SPIE Vol. 8991 899108-1: ***“10-40GHz on chip micro-optical link with all integrated Si Av LED optical sources, waveguides and Si-Ge photo detector technology”***:

[2] Kingsley .A. Ogudo\*, Jean-Luc Polleux, Lukas Snyman, Carlos Viana and Zerihun Tegegne 3<sup>rd</sup> *SENSORS, MEMS AND ELECTRO-OPTICAL SYSTEMS. SKUKUZA, SOUTH AFRICA*. 16-20 JUNE 2014. Tracking number: SME14-E100-5. doi: 10.1117/12.2064737: ***Realization of 10 GHz minus 30dB On-chip Optical Link with Si-Ge Bi-polar Technologys***:

[3] Lukas W. Snyman, Jean-Luc Polleux, Kingsley A. Ogudo\*, Carlos Viana and Sebastian Wahl, *PROCEEDINGS OF SPIE PHOTONIC west 2014*, 1-6 February 2014, Moscone center San Francisco USA. doi: 10.1117/12.2038195. Proc. of SPIE Vol. 8990 89900L-1: ***“High Intensity 100 nW 5 GHz Silicon Avalanche LED utilizing carrier energy and momentum engineering”***

### Chapter in a book:

[1] Book Chapter (InTech: "Advances in Optical Communication": “*Silicon Avalanche Based Light Emitting Diodes and Their Potential Integration into CMOS and RF Integrated Circuit Technology*” Authors: Kaikai Xu, Weifeng Sun, Kingsley A. Ogudo\*, Lukas W. Snyman, Jean-Luc Polleux, Qi Yu and Guannpyng Li. ISBN: 978-953-51-1730-8).

### III. MATLAB Code Appendices

#### Appendix A: The *MATLAB* code developed for the initialization of variable and biasing the optical source and the detector

---

```
clc
clear all
instr=instrfind;
delete(instr);

Root_Directory='S:\Matlab\GPIB\KINGS_LED_JAN-2013-
2014\RESULTS\OFFICIAL_25Jan2014\';
device_ID = 'ODie3_L1_Normal_config2';%PC1D44B40A4P
type = 'Is Sweep vs Vce Sweep Characterisation';%AvLED/SiGe detector 2x50um
common emitter HPT
setup_title = 'Id Vs Curves';
save_dir = 'ODie_3_L1_DC link response_SiGe_config2-V2';

%% source Bias Point

SMU1 = 1; %% optical source at port 1
%Vs_max = 14; %Amps
Is_max = 10e-3;

Vs_min = 0; %Amps
Vs_int =0.4; %Amps
NbOfPnts = 50; %1μ/0.5/1/1.5 mA

Vs_int2 = 0.401; %Amps
Vs_int3= 0.8; %Amps
NbOfPnts2 = 50; %2/3/4/5/6/7/8/9/10 mA
Vs_int4 = 0.801; %Amps
Vs_max =1.4; %Amps
NbOfPnts3 = 200; %2/3/4/5/6/7/8/9/10 mA

%% Detector bias points

SMU2 = 2; %% optical detector at port 2
Id_max = 1e-3; %Amps
Vd_min = -2.5; % Volts
Vd_int=-0.1;
Vd_max = -2; % Volts
Vd_NbOfPnts = 1;

RPSmu1 = 1.9; % Ohms
RPSmu2 = 1.9; % Ohms
% Current test-set generation
% detector bias vector creation
Vd = linspace(Vd_min, Vd_max, Vd_NbOfPnts);
Vd = Vd'; %-Vd';
%source bias vector creation
Vs_temp = linspace(Vs_min, Vs_int, NbOfPnts);
Vs_temp2 = linspace(Vs_int2, Vs_int3, NbOfPnts2);
Vs_temp3 = linspace(Vs_int4, Vs_max, NbOfPnts3);
Vs = [Vs_temp Vs_temp2 Vs_temp3];
Vs = Vs';%-Is';
```

```

try
    %% GPIB connection to all devices

    fopen(Instrument{ScdaAgilentB1500A}.GPIBobject);

%% Initialization

    AgilentB1500ASemiconductorAnalyzer_spotmeasurement...
    (Instrument{ScdaAgilentB1500A}.GPIBobject, 'init');

total_time = 0;
var1 = 0;

    %% Measurement
for ii=1:length(Vd),

    tStart = tic;
    indep_var(1).name = 'Id';
    indep_var(1).value = Id(ii);

    AgilentB1500ASemiconductorAnalyzer_spotmeasurement...
    (Instrument{ScdaAgilentB1500A}.GPIBobject, SMU2, Id_max, Vd(ii), 'CV');

    for jj=1:length(Vs),
        var1 = var1+1;
        export{var1,2}=num2str(Vs(jj));
        export{var1,3}=num2str(Vd(ii));
        export{var1,5}=num2str(RPsmu1);
        export{var1,7}=num2str(RPsmu2);

        tStart = tic;
        AgilentB1500ASemiconductorAnalyzer_spotmeasurement(Instrument...
            {ScdaAgilentB1500A}.GPIBobject, SMU1, Is_max, Vs(jj), 'CV');
        indep_var(2).name = 'Vs';
        indep_var(2).value = Vs(jj);

        Measure = AgilentB1500ASemiconductorAnalyzer_spotmeasurement...
        (Instrument{ScdaAgilentB1500A}.GPIBobject, 'ON');
        smu1Meas = Measure.(['port' int2str(SMU1)]);
        smu2Meas = Measure.(['port' int2str(SMU2)]);

        Is(jj) = smu1Meas.current;
        Id(jj) = smu2Meas.current;

        export{var1,4} = num2str(Id(jj));
        Vcf(jj) = Vd(ii)-RPsmu2*Id(jj);
        export{var1,8} = num2str(Vcf(jj));

        export{var1,1} = num2str(Is(jj));
        Vbf(jj) = Vs(jj)-RPsmu1*Is(jj);
        export{var1,6} = num2str(Vbf(jj));

        TimeControl

    for tt=1:length(saved_value)

```

```
        current_measurement{tt} = export{var1,tt};  
    end  
    total_time = toc(tStart)+total_time;  
end  
end
```

## Appendix B: The algorithm for the DC biasing and launching the voltage and current values to the optical link device structures through the Agilent B1500A Semiconductors extractor

---

```
clc
clear all
instr=instrfind;
delete(instr);

%% AvSiLED biasing and launching Test

SMU1=1;
SMU2=2;
channel1 = 1;
channel2 = 2;

Instrument = InstrObjGeneration;

for ii=1:length(Instrument),
    if strcmpi(Instrument{ii}.instr_ID, 'ScdaAgilentB1500A'),
        ScdaAgilentB1500A = ii;
    elseif strcmpi(Instrument{ii}.instr_ID, 'DcSupplyAgilent6625A'),
        DcSupplyAgilent6625A = ii;
    end
fprintf(Instrument{DcSupplyAgilent6625A}. GPIBObject, 'OUT 2,0'); %Disable
power on port 2
fprintf(Instrument{DcSupplyAgilent6625A}. GPIBObject, 'OUT 1,0'); %Disable
power on port 1

Vc_b1500=-2; % bias voltage for the detector
Ic_b1500_max=1e-3;

%Vb2=0.001;

Ib_b1500_max=10e-3;% for the source
Vb_b1500=1.4; % bias voltage for the detector
pause_time=1;
total_time = 0;

% Vc_6625=2.5;
% Ic_6625_max=12e-3;
%% Vc1 (HPT 'ON')
AgilentB1500ASemiconductorAnalyzer_spotmeasurement(Instrument...
{ScdaAgilentB1500A}. GPIBObject, SMU1, Ib_b1500_max, Vb_b1500, 'CV');
for aa=1:100000
    tStart = tic;
    Measure =
AgilentB1500ASemiconductorAnalyzer_spotmeasurement(Instrument{ScdaAgilentB1
500A}. GPIBObject, 'ON');

    smu1Meas = Measure.(['port' int2str(SMU1)]);
    smu2Meas = Measure.(['port' int2str(SMU2)]);

    Ib_b1500 = smu1Meas.current; %% measure current at the detector
    Ic_b1500 = smu2Meas.current; %% measure current at the source
```

---

## Appendix C: Main program for DC biasing and RF input power supply to device

---

```
click
clear all
instr=instrfind;
delete(instr);

Root_Directory =
'S:\Matlab\SCHIELLEIN\GPIB\CARLOS\KINGS_LED_JAN2014\RESULTS\OFFICIAL_25Jan2
014\';
device_ID = 'ODie3_L3_Normal_config2';%PC1D44B40A4P
type = 'Is Sweep vs Vce Sweep Characterisation';%SiAvLED/1.2x2um optical
link device
setup_title = 'Id Vs Curves';
save_dir = 'ODie_3_L3_DC link response_SiGe_config2V2';

%%
% source Bias Point

SMU1 = 1;
%Vs_max = 14; %Amps
Is_max = 10e-3;

Vs_min = 0; %Amps
Vs_int =0.4; %Amps
NbOfPnts = 50; %1u/0.5/1/1.5 mA

Vs_int2 = 0.401; %Amps
Vs_int3= 0.8; %Amps
NbOfPnts2 = 50; %2/3/4/5/6/7/8/9/10 mA

Vs_int4 = 0.801; %Amps
Vs_max =1.4; %Amps
NbOfPnts3 = 200; %2/3/4/5/6/7/8/9/10 mA

% Detector bias points
SMU2 = 2;

Id_max = 1e-3; %Amps
Vd_min = -2.5; % Volts
Vd_int=-0.1;
Vd_max = -2; % Volts
Vd_NbOfPnts = 1;

RPSmu1 = 1.9; % Ohms
RPSmu2 = 1.9; % Ohms
%%
% Current test-set generation
% detector bias vector creation
Vd = linspace(Vd_min, Vd_max, Vd_NbOfPnts);
Vd = Vd'; %-Vd';
%source bias vector creation
Vs_temp = linspace(Vs_min, Vs_int, NbOfPnts);
Vs_temp2 = linspace(Vs_int2, Vs_int3, NbOfPnts2);
```

```

Vs_temp3 = linspace(Vs_int4, Vs_max, NbOfPnts3);
Vs = [Vs_temp Vs_temp2 Vs_temp3];
Vs = Vs'; % -Is';

DUT.device_ID = device_ID;
DUT.type = type;

DUT.Port{SMU1}.Name = 'Bias1';
DUT.Port{SMU1}.ResPara = RPsmu1;
DUT.Port{SMU1}.Max.current = Vs_max;
DUT.Port{SMU1}.Max.voltage = Is_max;
DUT.Port{SMU1}.test.current = Vs;

DUT.Port{SMU2}.Name = 'Bias2';
DUT.Port{SMU2}.ResPara = RPsmu2;
DUT.Port{SMU2}.Max.current = Id_max;
DUT.Port{SMU2}.Max.voltage = Vd_max;
DUT.Port{SMU2}.test.voltage = Vd;

pause_time = 0.1; %Seconds
var1 = 0;

%% Instruments objects construction

Instrument = InstrObjGeneration;

for ii=1:length(Instrument),
    if strcmpi(Instrument{ii}.instr_ID, 'ScdaAgilentB1500A'),
        ScdaAgilentB1500A = ii;
    end
end

%% Save parameters

save_directory = Root_Directory ; % [pwd '\BIN\Traitement' ];
save_directory = [save_directory save_dir ];

    if ~exist(save_directory, 'dir')
        mkdir(save_directory);
    end

    pause(1);

    %% Saved Value

saved_value{1}=[ 'Vled' ];
saved_value_unit{1}='V';

saved_value{2}=[ 'Iled' ];
saved_value_unit{2}='A';

saved_value{3}=[ 'Vhpt' ];
saved_value_unit{3}='V';

```



```

saved_value{4}=['Ihpt'];
saved_value_unit{4}='A';

saved_value{5}=['RPsmu1'];
saved_value_unit{5}='Ohms';

saved_value{6}=['Vbf'];
saved_value_unit{6}='V';

saved_value{7}=['RPsmu2'];
saved_value_unit{7}='Ohms';

saved_value{8}=['Vcf'];
saved_value_unit{8}='V';

pause(1);

%% Allocate memory

test_length = length(Vd)*length(Vs);
Is = zeros(length(Vs),1);
Id = zeros(length(Vd),1);
Vbf = zeros(length(Vs),1);
Vcf = zeros(length(Vd),1);

export=cell(test_length,length(saved_value));
current_measurement=cell(length(saved_value),1);
application_test_name = mfilename;

try
    %% GPIB connection to all devices

    fopen(Instrument{ScdaAgilentB1500A}.GPIBObject);

%% Initialization

AgilentB1500ASemiconductorAnalyzer_spotmeasurement...
(Instrument{ScdaAgilentB1500A}.GPIBObject,'init');

total_time = 0;
var1 = 0;

%% Measurement
for ii=1:length(Vd),

    tStart = tic;
    indep_var(1).name = 'Id';
    indep_var(1).value = Id(ii);

    AgilentB1500ASemiconductorAnalyzer_spotmeasurement...
    (Instrument{ScdaAgilentB1500A}.GPIBObject, SMU2, Id_max, Vd(ii), 'CV');

    for jj=1:length(Vs),
        var1 = var1+1;
        export{var1,2}=num2str(Vs(jj));
    end
end

```

```

export{var1,3}=num2str(Vd(ii));
export{var1,5}=num2str(RPsmul);
export{var1,7}=num2str(RPsmu2);

tStart = tic;
AgilentB1500ASemiconductorAnalyzer_spotmeasurement(Instrument...
    {ScdaAgilentB1500A}.GPIBobject, SMU1, Is_max, Vs(jj), 'CV');
indep_var(2).name = 'Vs';
indep_var(2).value = Vs(jj);

Measure = AgilentB1500ASemiconductorAnalyzer_spotmeasurement...
    (Instrument{ScdaAgilentB1500A}.GPIBobject, 'ON');
smulMeas = Measure.(['port' int2str(SMU1)]);
smu2Meas = Measure.(['port' int2str(SMU2)]);

Is(jj) = smulMeas.current;
Id(jj) = smu2Meas.current;

export{var1,4} = num2str(Id(jj));
Vcf(jj) = Vd(ii)-RPsmu2*Id(jj);
export{var1,8} = num2str(Vcf(jj));

export{var1,1} = num2str(Is(jj));
Vbf(jj) = Vs(jj)-RPsmul*Is(jj);
export{var1,6} = num2str(Vbf(jj));

TimeControl

for tt=1:length(saved_value)
    current_measurement{tt} = export{var1,tt};
end
total_time = toc(tStart)+total_time;
end
end

matdata=cellfun(@str2num,export);

export = strrep(export, '.', ',');
save_file = DCdata_export_vB1500_Carlos(save_directory, setup_title,
application_test_name, device_ID,...
saved_value, saved_value_unit, export);
%plot_icvce([matdata(:,3:4), matdata(:,1:2)], 'name', 'xlabel', 'ylab',
save_directory)
plot_icvbe_2bias ([matdata(:,3:4), matdata(:,1:2)], device_ID,
save_directory)
figure(3)
plot(Vs,Is*1000)
xlabel ('Vs (V) ')
ylabel ('Is (mA) ')
title([device_ID ' Is Vs Curves'])
grid on

figure(4)
plot(Vs,Id*1000)
xlabel('Vs (V) ')
ylabel('Id (mA) ')
title ([device_ID 'Id Vs link DC response curve'])
grid on

```

```

saveas(gcf, [save_directory '\\' device_ID 'Id_vs_Vs_'] , 'fig')
%saveas(gcf, [save_directory '\\' device_ID 'Is_vs_Vs_'] , 'fig')

disp('')
disp('')
disp('=> TEST FINISHED <=')
disp('')
disp('')

err = MException('MeasStatus:FINISHED', 'Measurements normaly ended');
throw(err)

catch ME1
    %% Exit Handling

    errtest = 'MeasStatus:FINISHED';
    errtest1 = 'Compliance:Reach';
    if strcmp(errtest1,ME1.identifier),
        test_state = 'COMPLIANCE_';
    elseif ~strcmp(errtest,ME1.identifier),
        test_state = 'ABORTED_';
    else
        test_state = '';
    end

    % B1500A

    AgilentB1500ASemiconductorAnalyzer_spotmeasurement(Instrument{ScdaAgilentB1
500A}.GPIBobject,'clear'); %All channels OFF and disabled
    clrdevice(Instrument{ScdaAgilentB1500A}.GPIBobject);
    fclose(Instrument{ScdaAgilentB1500A}.GPIBobject);
    disp('=> B1500A switched OFF and Closed <=')
    fprintf(ME1.message);

end

```

## Appendix D: Program for launching the current and voltage values to device

---

```
clc
clear all
instr=instrfind;
delete(instr);

%% AvSiLED biasing and lunning Testing

SMU1=1;
SMU2=2;
channel1 = 1;
channel2 = 2;

Instrument = InstrObjGeneration;

for ii=1:length(Instrument),
    if strcmpi(Instrument{ii}.instr_ID,'ScdaAgilentB1500A'),
        ScdaAgilentB1500A = ii;
    elseif strcmpi(Instrument{ii}.instr_ID,'DcSupplyAgilent6625A'),
        DcSupplyAgilent6625A = ii;
    end
end
try
fopen(Instrument{ScdaAgilentB1500A}.GPIBObject);    %Connecting
AgilentB1500A
AgilentB1500ASemiconductorAnalyzer_spotmeasurement(Instrument{ScdaAgilentB1500A}.GPIBObject,'init');
fopen(Instrument{DcSupplyAgilent6625A}.GPIBObject);    %Connecting
ADcSupplyAgilent6625A
fprintf(Instrument{DcSupplyAgilent6625A}.GPIBObject,'OUT 2,0'); %Disable
power on port 2
fprintf(Instrument{DcSupplyAgilent6625A}.GPIBObject,'OUT 1,0'); %Disable
power on port 1

Vc_b1500=-2;    % bias voltage for the detector
Ic_b1500_max=1e-3;

%Vb2=0.001;
Ib_b1500_max=10e-3;% for the source
Vb_b1500=1.4; % bias voltage for the detector

pause_time=1;
total_time = 0;

% Vc_6625=2.5;
% Ic_6625_max=12e-3;

    %% Vc1 (HPT 'ON')
AgilentB1500ASemiconductorAnalyzer_spotmeasurement(Instrument{...
    {ScdaAgilentB1500A}.GPIBObject, SMU1,Ib_b1500_max, Vb_b1500, 'CV');

AgilentB1500ASemiconductorAnalyzer_spotmeasurement(Instrument{...
    ScdaAgilentB1500A}.GPIBObject, SMU2, Ic_b1500_max, Vc_b1500, 'CV');
```

```

for aa=1:100000

    tStart = tic;

    Measure =
    AgilentB1500ASemiconductorAnalyzer_spotmeasurement(Instrument{ScdaAgilentB1
500A}.GPIBObject, 'ON');

    smu1Meas = Measure.(['port' int2str(SMU1)]);
    smu2Meas = Measure.(['port' int2str(SMU2)]);

    Ib_b1500 = smu1Meas.current;
    Ic_b1500 = smu2Meas.current;

    info_str = ['Measurement: ' num2str(aa) '/' num2str(100000)];
    elapsed_time = ['in ' num2str(total_time) 's'];
    if aa>1,
        average_time = total_time / (aa-1);
        total_duration = total_time + average_time*(100000-aa);
        finish_estimation = seconds2human(total_duration-total_time); %,
'full'
        fprintf('%s\t%s\nFinishing in:\t%s\n', info_str, elapsed_time,
finish_estimation);
    else
        fprintf('%s\t%s\n',info_str,elapsed_time);
    end
    fprintf('Current
Measurement:\nIc: %.6f,\tVc: %f,\nIb: %.6f,\tVb: %f,\n\n\n',Ic_b1500,Vc_b15
00,Ib_b1500,Vb_b1500);

    if Ib_b1500>=Ib_b1500_max || Ic_b1500>=Ic_b1500_max,
        disp('MAXIMUM VALUE(S) REACHED')
        err = MException('Compliance:Reach', 'Measured value reach
compliance');
        throw(err)
    end

    t = timer('TimerFcn','robot;', 'StartDelay',pause_time);

    start(t);

    proceed_query='\nAbort?\n if YES press ENTER\n';

    proceed = input(proceed_query, 's');

    if isempty(proceed) || ~strcmpi(proceed, 'proceed'),
        stop(t);
        total_time = toc(tStart)+total_time;
        disp('OPERATION ABORTED')
        err = MException('OpAbort:ON', 'User asked for operation
abortion');
        throw(err)
    end

clc

```

```

end

disp('')
disp('')
disp('=> TEST FINISHED <=')
disp('')
disp('')
err = MException('MeasStatus:FINISHED', 'Measurements normaly ended');
throw(err)

catch ME1

    errtest = 'MeasStatus:FINISHED';
    errtest1 = 'Compliance:Reach';
    if strcmp(errtest1,ME1.identifier),
        test_state = 'COMPLIANCE_';
    elseif ~strcmp(errtest,ME1.identifier),
        test_state = 'ABORTED_';
    else
        test_state = '';
    end

AgilentB1500ASemiconductorAnalyzer_spotmeasurement(Instrument{ScdaAgilentB1
500A}.GPIBobject,'clear'); %All channels OFF and disabled
clrdevice(Instrument{ScdaAgilentB1500A}.GPIBobject);
fclose(Instrument{ScdaAgilentB1500A}.GPIBobject);
disp('=> B1500A switched OFF and Closed <=')
end

```

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