



Design methodologies for multi-mode and multi-standard low-noise amplifiers

Gabrielle Guitton

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UNIVERSITY OF BORDEAUX

DOCTORAL THESIS

Design Methodologies for multi-mode and multi-standard Low-Noise Amplifiers

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*A thesis submitted in fulfillment of the requirements
for the degree of Doctor in electronic*

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Abstract

Design Methodologies for multi-mode and multi-standard Low-Noise Amplifiers

The recent enthusiasm for the Internet of Things as well as for communication satellites leads to the need for high-performance radio-frequency (RF) communication systems. In order to meet the constraints of the mass market, these systems must be as compact and be as low power as possible. Beside, they are expected to address multiple communication standards and to adjust their performance to the environment, still in order to reduce the size and the power consumption. To address these purposes, the goal is to design multi-mode and multi-standard receivers. Currently, many works focus on the development of low-noise amplifiers (LNA), one of the most critical block of RF receivers. Hence, LNAs require design flows that can adapt to the different technologies and topologies in order to meet any given set of specifications. This thesis aims at the development of simple and accurate design methodologies for the implementation of low-noise amplifiers.

The first methodology is dedicated to the implementation of a LNA in COTS technology for spatial applications. This LNA offers a broadband matching to address several standards. It is designed to be part of an RF receiver for nano-satellites. Thus, the latter is first studied in order to determine the specifications based on the standards of the targeted applications.

The second methodology is dedicated to the implementation of LNAs in CMOS technology for any kind of applications. This methodology is first illustrated with basic topologies and then applied to an highly linear inductorless LNA. The design methodology also enables a fair comparison between topologies and between CMOS technologies, even the most advanced ones such as the 28 nm FDSOI.

Finally, reconfigurability is added to the inductorless LNA, to address several standards while retaining the optimum sizing given by the previously introduced methodology. Indeed, the size and polarization of each transistor are digitally controlled in order to adjust the LNA's performance to a given standard. Furthermore, the study of N-path filters combined with the proposed LNA is explored to improve the linearity of the circuit.

Key words: Internet of Things, communication satellites, radio-frequency, low power, multi-mode, multi-standard, low-noise amplifier, design methodology, inductorless, N-path filters.

Résumé

Méthodologies de conception pour les amplificateurs faible bruit multi-mode et multi-standard

L'engouement récent pour l'Internet des Objets comme pour les communications satellites entraîne des besoins forts en systèmes de communication radio-fréquence (RF) performants. Afin de répondre aux contraintes du marché de masse, ces systèmes doivent être toujours moins encombrants et permettre de maîtriser leur consommation de puissance. Ils doivent également être capables d'adresser plusieurs standards de communications et d'ajuster leur performances aux besoins de leur environnement, toujours afin de réduire leur taille et leur consommation. L'objectif est donc de concevoir des récepteurs multi-modes et multi-standards. Actuellement, beaucoup de travaux se concentrent sur le développement d'amplificateurs faible-bruit (LNA), l'un des blocs les plus critiques des récepteurs RF. Pour cela, les LNA nécessitent des flots de conception capables de s'adapter aux différentes technologies et topologies afin de répondre à des cahiers des charges très divers. Cette thèse a donc pour objectif le développement de méthodologies de conception simples et précises pour l'implémentation de LNA.

La première méthodologie présentée est dédiée à l'implémentation de LNA en technologie COTS pour des applications spatiales. Ce LNA présente une adaptation large-bande pour adresser plusieurs standards. Il a été conçu pour faire partie d'un récepteur RF dédié aux nano-satellites. Ce dernier a donc fait l'objet d'une étude préliminaire afin de déterminer le cahier des charges à partir des normes des standards visés.

La seconde méthodologie est dédiée à l'implémentation de LNA en technologie CMOS pour n'importe quel type d'applications. Cette méthodologie est d'abord présentée au travers de topologies simples, puis appliquée à un LNA sans inductance à forte linéarité. Cette méthodologie permet notamment de comparer les topologies mais également les technologies CMOS, même les plus avancées telle que la 28 nm FDSOI.

Enfin le LNA sans inductance est rendu reconfigurable pour adresser plusieurs standards tout en gardant le dimensionnement optimum obtenu par la méthodologie présentée précédemment. En effet la taille et la polarisation de chaque transistor sont contrôlées numériquement afin d'adapter les performances du LNA à un standard donné. De plus, l'étude de filtres de type N-path combinés au LNA proposé permet d'étendre encore la linéarité du circuit.

Mots-clés: Internet des Objets, communication satellites, radio-fréquence, faible consommation, amplificateurs faible bruit, multi-modes, multi-standards, méthodologies de conception, sans inductance, filtre N-path.

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List of Abbreviations

ADC	Analog-to-Digital Converter
BW	BandWidth
CC	Capacitive Cross-Coupling
CG	Common-Gate
CMOS	Complementary Metal Oxyde Semiconductor
CS	Common-Source
COTS	Components Of The Shelf
DAC	Digital-to-Analog Converter
DFF	D-type Flip-Flop
DIBL	Drain-Induced Barrier Lowering
FB	FeedBack
FDSOI	Fully Depleted Silicon On Insulator
FoM	Figure of Merit
GBW	Gain-BandWidth product
GNSS	Global Navigation Satellite System
GSM	Global System for Mobile
IC	Inversion Coefficient
IIP₃	Input 3rd-order Intercept Point
IoT	Internet of Things
LEO	Low Earth Orbit
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MI	Moderate Inversion
NF	Noise Figure
OTA	Operational Transconductance Amplifier
PA	Power Amplifier
PCB	Printed Circuit Board
RFFE	Radio-Frequency Front-End
Rx	Receiver
SAW	Surface Accoustic Wave
SCE	Short-Channel Effects
SI	Strong Inversion
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
SR	Shift Register
TMTC	TeleMetry and TeleCommand
Tx	Transmitter
VCO	Voltage Controlled Oscillator
VSAT	Very Small Aperture Terminal
ULP	Ultra Low Power
UWB	Ultra Wide Band

WI	Weak Inversion
WLAN	Wireless Local Area Network
WSN	Wireless Sensor Network

Chapter 1

Introduction

1.1 Telecommunications

Wireless communications have become a major part of our daily life. They are needed for multiple applications such as healthcare, radar and entertainment. The devices dedicated to these applications (cell-phones, tablets, sensors, satellites) operate at different part of the frequency spectrum which is regulated by communication standards. These standards are supposed to cover a wide range of application accounting for the distance of communication, the data and the level of security.

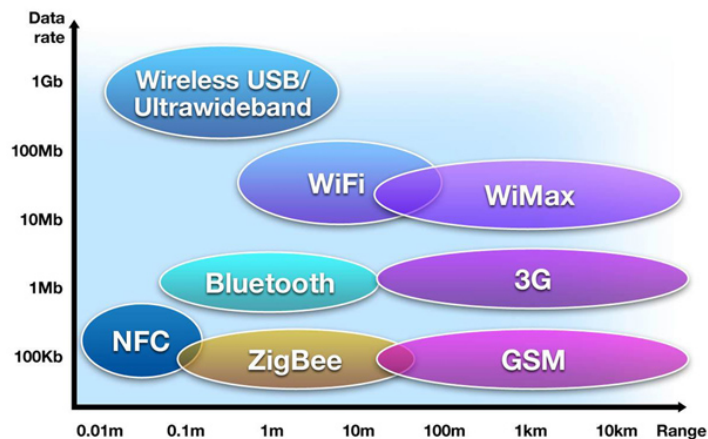


FIGURE 1.1: Data rate of communication standards versus their range.

Source: [1]

Figure 1.1 shows the data rate versus the distance of communication of the most common standards. Their properties mainly depend on the part of the frequency spectrum they are located in: each standard has a defined bandwidth which is divided in communication channels. Hence, the standards lay on different technologies and have varied characteristics [2]. For example, the GSM standard is a long range standard with a low data rate, whereas WiFi which is exclusively exploited for indoor communications covers a very short range with a high data rate. Therefore, the associated communication systems have to answer completely different specifications and different technologies are employed.

This thesis will focus on two applications, the Internet of Things (IoT) and the telecommunication satellites. The first one uses a large number of completely different standards since it consists of multiple connected devices. The latter, on the other hand, uses a few long

range standards with medium to high data rates. These applications are introduced in the following subsections.

1.1.1 Internet of Things

In 2020, the number of connected devices might reach fifty billion (figure 1.2), which will represent an average of seven devices per person. Most of these devices will be part of the IoT and should therefore perform wireless communications whilst consuming the least amount of energy required and be as small as possible [3].

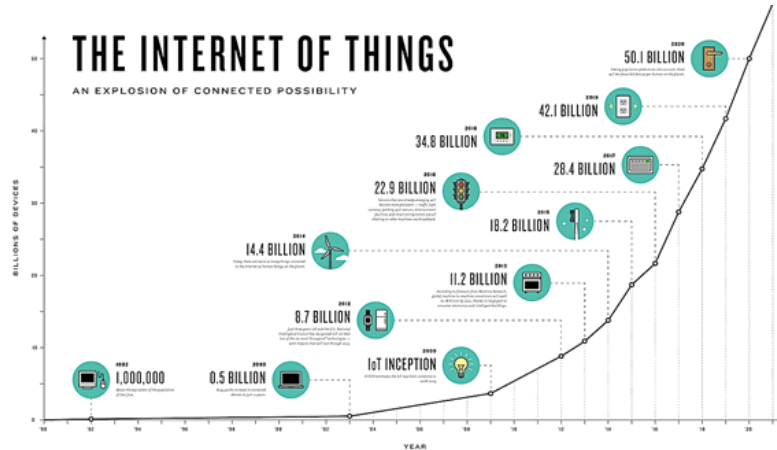


FIGURE 1.2: Evolution of the Internet of Things.
Source: [4]

The IoT is the internet of daily life objects equipped with ubiquitous intelligence [5]. These objects are connected devices capable of transmitting data between physical and virtual objects. It covers numerous domains and applications such as entertainment, environment and health monitoring and it can be divided into five categories which are listed below with few examples illustrated in figure 1.3.

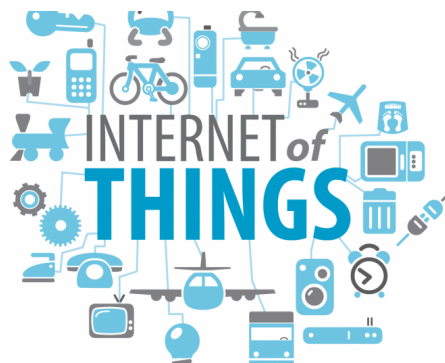


FIGURE 1.3: Examples of IoT connected devices.
Source: [6]

- Smart wearable : smart watch, fitbit, connected clothes and heart monitoring implants.
- Smart home : monitoring of heating, lighting and air conditioning with heat and light sensors.

- Smart city : monitoring bridges and railway, scheduling maintenance, parking spaces which send alerts when available.
- Smart environment : monitoring air quality, cameras streaming live of wildness and sensors for crops.
- Smart enterprise : optimization of manufacturing production by networking machinery, sensors and control systems together.

Furthermore, in a close future the IoT could not be limited to sensing things but will be able to perform actions. For example, with intelligent shopping systems that can order food when they sense lack of it in a fridge.

The current challenge of the IoT is to develop low power devices while ensuring constantly growing needs. Smart-phones, for example, must offer rich and varied multimedia content while extending battery lifetime. Furthermore, the connected devices may have to address completely different communication scenarios: some have to address multiple standards and thus should be highly linear (smart-watches, tablets), whereas some require very low power consumption (sensors). The IoT is regulated by many standards from short range (bluetooth, WiFi, zigbee) to medium range (LTE-advanced, HaLow) and long range (LPWAN, VSAT). Hence the heterogeneous communications featuring the IoT call up for very different and highly challenging radio solutions.

1.1.2 Satellites

The IoT market leads to the development of terrestrial solutions but also spatial ones. Telecommunication satellites are currently emerging and have faced many changes and evolution over the last decade. There are two main domains in spatial communications:

- The first one gathers the long range missions and medium orbits. It is dedicated to spatial discovery, service development (such as Galileo for positioning) and international cooperation with the International Space Station (ISS). This is exclusively lead by the space agencies: ESA in Europe, NASA in the US and ROSCOMOS in Russia. The missions and constellations aim at long lifetime for the satellites, up to 25 years. Furthermore, they are heavy, 500 kg to 5 tonnes, and their quality and reliability are the main focus during development process.



FIGURE 1.4: Picture of a nano-satellite.

Source: [7]

- The second one gathers short-lifetime satellites, from a couple of months to few years, navigating through low earth orbits (LEO). It is mainly private sector companies, with moderate experience in spatial domain (such as Google with the OneWeb constellation), which invest in this market. The cost decrease is the main challenge of this kind of constellation. Satellites are classified by their size: CubeSat, 10 cm³ (1U), is the smallest one as illustrated in figure 1.4. It has been created first by Professors Jordi Puig-Suari and Bob Twiggs in 1999 for their students. The first one was launched in 2003. Since then, more than 200 have been launched by private companies as well as amateurs and students. CubeSat is now a reference for satellites lighter than 50 kg, also known as nano-satellites, as illustrated in figure 1.5.

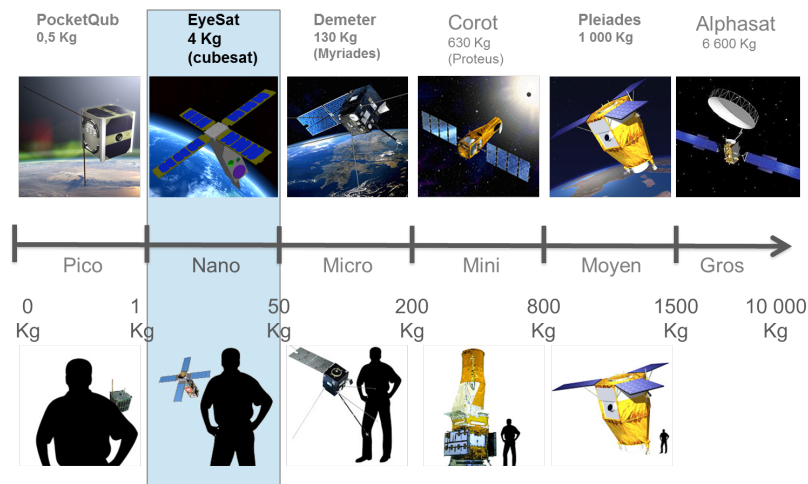


FIGURE 1.5: Classification of satellites.

Source: [8]

These small satellites' main functions are navigation and data transmission. The first function correspond to the GNSS standard, Global Navigation Satellite System, and the second one to TMTC, TeleMetry and TeleCommand. Telecommunication satellites represent an emerging domain with solid growth potential. The current objectives are to lower the cost of fabrication while improving the performances of imaging system, designing new concept of altimeters, processing of radar signal and many others. Hence, lots of work focus on developing communication systems for these satellites accounting for a significant reduction of the cost still maintaining an adequate reliability. [9, 10, 11].

1.1.3 Transceivers

Communication systems consist of a receiver and an emitter which both have an RF/analog part and a digital part as is illustrated in figure 1.6.

In the receiver, the signal carrying the information received at the antenna, is processed first by a surface acoustic wave (SAW) filter. Then, it is amplified by the low-noise amplifier (LNA) and down-converted to baseband by the mixer and a local oscillator (RF demodulator). Finally, it is filtered and amplified again in the analog signal processing block (ASP). In the digital part, the signal is converted by the analog-to-digital converter (ADC) and processed by the digital signal processing (DSP) in order to recover the information.

Conversely, in the emitter, the digital signal is converted by the digital-to-analog converter (DAC), it is then processed by the ASP before the up-conversion of the RF modulator.

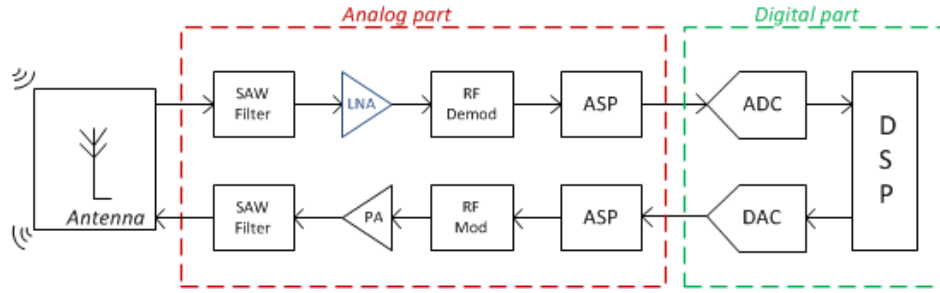


FIGURE 1.6: Schematic of a transceiver.

Finally it is amplified by the power amplifier (PA) and filtered before being emitted by the antenna.

The RF amplifiers, PA and LNA, are critical blocks for transmitter (Tx) and receiver (Rx) parts respectively. Indeed the PA determines the power and spectrum efficiency of the Tx, whereas the LNA supports the sensitivity of the Rx. They are also concerned by linearity issue which become challenging in a multi-standard scenario. A lot of research currently focuses on the development of skilled RF amplifiers capable of addressing future communication schemes. In this thesis, we focus on the design of LNA which is the most critical block of the radio-frequency front-end (RFFE) since it will determine the noise of the whole analog part and therefore the signal-to-noise ratio (SNR) transmitted to the digital part.

Furthermore, communication systems should be reconfigurable to address different standards in a single receiver in order to reduce the footprint and power consumption [12, 13]. Yet, they also should be reconfigurable when addressing a single standard. RFFE are currently designed to work in worst case scenario, therefore when the communication conditions improve, they are oversized and consumes too much power. Hence, in order to save current, RF front-ends, and consequently LNAs, should be able to adjust their performance to what is really needed [14].

The specifications of RFFE are defined by telecommunication standards. The link between the specifications of an RFFE and the regulation tests of a standard is presented in chapter 2. Then, considering the specifications of the RFFE, the specifications of the LNA are easily deduced. All of these requirements must be met during the design of LNAs.

1.2 Design Challenges for LNA design

The requirements and constraints imposed by the applications have been introduced in the previous section. The development of wireless communications results in the need for higher integration, reconfigurability to address multiple standards and multiple mode of operation and low-cost/low-power devices for mass markets. Meanwhile, the design of LNA also has to address technical challenges which are further discussed in this section.

Multi-variables space

Many efforts are brought to the optimization of LNA in order to limit their power consumption while ensuring given specifications (low noise, high gain, linearity, input matching, bandwidth). This optimization is difficult due to the interdependency of the

specifications. Thus, RF designers must find the right trade-off which can be completely different from one application to another.

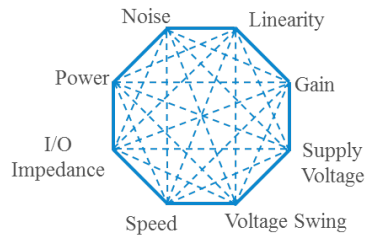


FIGURE 1.7: Multi-variables space.

Furthermore, the complexity of LNAs lead to a great number of design variables. Therefore, they require methodologies which can deliver the right set of design variables optimizing the different performances.

Advanced technologies

LNAs can be designed using components of the shelf (COTS) or complementary metal-oxide-semiconductor (CMOS) technologies. The first one offers a choice limited to commercialized components which are compared in respect to their performance for a targeted application. The design focuses only on the implementation, leaving few freedom degrees. However, they enable high performance and robust circuits which are major constraints for spatial applications such as nano-satellites.

On the contrary, CMOS technologies offers many degrees of freedom with the technological parameters of transistors at the cost of more complex design. As the technologies are evolving quickly, LNAs are redesigned in order to improve their performances and to reduce their footprint. The cut-off frequency, f_t , is illustrated in figure 1.8 versus the gate length. As gate length is decreasing, f_t is increasing. This technology skill can be exploited to extend the bandwidth of the circuits for instance.

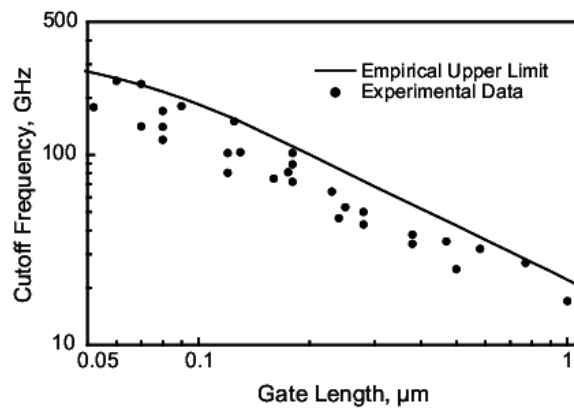


FIGURE 1.8: Evolution of f_t versus the gate length.
Source: [15]

However, with the decrease of transistor's size, especially the gate length, come new challenges brought by short-channel effects (SCE) such as velocity saturation and drain-induced barrier lowering (DIBL) [16]. Therefore LNA's design must be adjusted to any technology nodes accounting for shrink effects.

Design methodologies

There are several existing design methodologies for mixers [17], for LC oscillators [18] and for LNAs and PAs [19, 20, 21]. These methodologies often privileged a specific issue over the others. In [19], they describe a methodology for LNA with bipolar transistors but they focus only on the noise. In [20], they present an innovative topology based on bipolar and MOS transistors but do not add reconfigurability. In [21], the proposed design flow address many challenges but it consists of seven different steps. Therefore, although several works focus on design methodologies, they are often too complex for a fast design and specific to a technology, a topology or a single characteristic.

Interestingly, [20] and [21] are based on constant current density biasing which is similar to the methodology presented in chapters 3 and 4. For a given topology, if the specifications vary, the size and bias might change but the current density remains quasi constant. This approach opens up to a more general purpose design strategy.

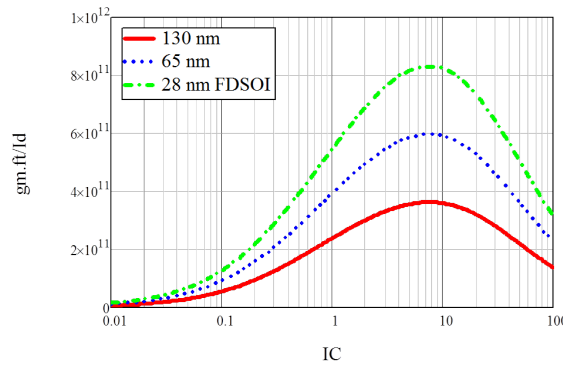


FIGURE 1.9: Evolution of $g_m f_t / i_d$ versus the Inversion Coefficient, IC , for three CMOS nodes: 28 nm FDSOI, 65 nm and 130 nm.

Another way of designing LNAs is to use metrics such as $g_m f_t / i_d$. It is illustrated in figure 1.9 versus a normalization of the drain current to technological parameters (see chapter 3) for three technological nodes. This figure of merit peaks in the region of moderate inversion, where the LNA should have the optimum bias for a given specifications. It is shown in this figure and will be demonstrated in chapter 4 that for a given topology and a given set of specifications, the optimum IC does not vary much from one node to another. However, this method gives a trend for the design but does not clearly gives the performances of a circuit and the optimum design variables [22].

Therefore, the challenges of LNA's design can be listed:

- small footprint and low-power consumption to answer the needs of the mass market,
- reconfigurability to address multi-mode multi-standard requirements and save power,
- simple and accurate design methodologies to navigate through the multi-variable space and optimized the performance,

- portability of these methodologies to any technology nodes.

1.3 Thesis outline

This chapter introduces the numerous challenges faced by RF designers. The goal of this thesis is to answer these challenges with efficient design methodologies for LNAs.

Chapter 2 presents a design flow for LNAs on printed circuit board, PCB, capable of addressing two standards. This LNA has been designed to answer the need of the ELISE project which aims at developing a nano-satellites operating at two frequency bands (S and L bands) for positioning and data transmission. Since it is a spatial application, the proposed LNA is based on a bipolar transistor for its robustness to radiations.

Chapter 3 describes a design flow based on the Inversion Coefficient, IC , for CMOS technologies. This methodology uses the EKV model which predicts MOS behavior continuously from weak to strong inversion and enables an intuitive and accurate methodology for RF designers. It is portable to any CMOS process, even the most advanced ones. In this chapter, three different nodes are compared: 28 nm FDSOI, 65 nm and 130 nm.

Chapter 4 reports on an application of the IC -based methodology. An inductorless LNA is proposed to reduce the silicon foot print. The topology features an active feedback offering both reconfiguration and linearity capability. Two cases of sizing are investigated : one dedicated to low power applications, another one for wideband and highly linear receiver. Finally the low power LNA as well as the wideband LNA have been designed in the three nodes mentioned previously and the 28 nm FDSOI LNA has been measured to validate the analytical model.

Chapter 5 introduces several solutions to implement a reconfigurable LNA. First, it uses the design methodology and the LNA of chapter 4 in order to implement a LNA that can answer the two applications (wideband and low-power) by switching the transistor's size and bias. In a second part, the concept of N-path filter and the co-design with the proposed LNA are introduced. These integrated filters offer a high selectivity along with a wide frequency tuning range.

Chapter 6 draws the conclusions of this thesis and discusses future work.

Chapter 2

Design Methodology for LNAs on PCB

This work is part of the Efficient constellation Initiative for Space and Environment (ELISE) project. It is a European project which aims at developing a nano-satellite, also known as CubeSat. The IMS Laboratory was involved in the development of the RF section of the satellite's receiver¹. The objective is to implement a dual-band RF front-end (RFFE) operating at 1.575 GHz (L1-band for GNSS) and 2.02-2.11 GHz (S-band for TMTC) using components-of-the-shelf (COTS). The first band is used for the navigation of satellites and the second band is used to broadcast telemetry and receive telecommand. The specifications of the RFFE and its architecture are presented in section 2.1. Then, section 2.2 focuses on its first block; the LNA and its design flow. Finally the results of the proposed LNA operating at f_{GNSS} and f_{TMTC} are shown in section 2.3.

2.1 Dual-band receiver

2.1.1 Analysis of the GNSS and TMTC standards

Nano-satellites are relatively small satellites (10U to 20U) so they are considerably limited in terms of weight and available power [23]. Therefore, the dual-band RFFE shall be small and very low power. Furthermore, its noise figure should be low since the received signal can be as weak as -130 dBm for the GNSS. The regulation test of the GNSS & TMTC RF receivers for the ELISE project are listed in table 2.1.

	GNSS	TMTC
frequency (GHz)	1.575	2.025-2.11
S_{min}/S_{max} (dBm)	-130/-80	-100/-70
E_b/N_0 (dB)	9.6	9.6
B (MHz)	2	6
R (Mbps)	1.023	3
P_{DC} (W)	< 0.4	< 0.4
Weight (g)	< 50	< 50

TABLE 2.1: Regulation test for the GNSS & TMTC receiver.

¹This receiver has been designed in collaboration with John Nicot and Thomas Petit during their Master thesis.

In order to define all the specifications of the RFFE from the given requirements, an analysis of telecommunication standards is presented in this section. The receiver and its characteristics are shown in figure 2.1. The signal carrying the information is received by the antenna then it is amplified and down-converted to baseband by the RFFE. Finally, it is transmitted to an analog-to-digital converter in order to be processed by the digital part of the receiver.

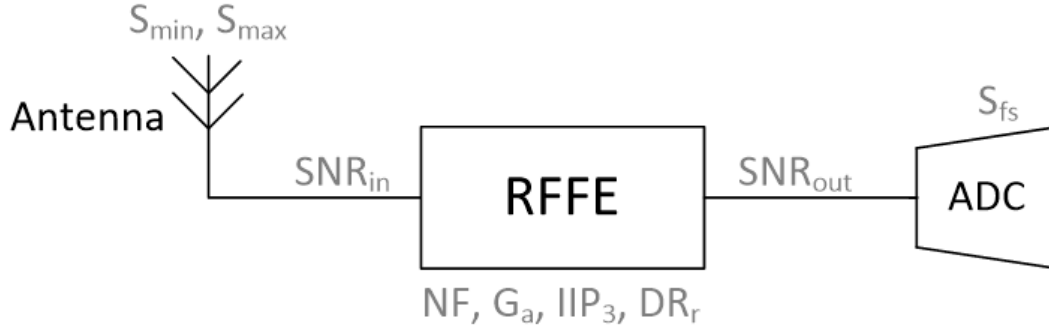


FIGURE 2.1: RF receiver and its characteristics.

The most critical specifications of the RFFE are its gain, its noise figure, its sensitivity and its linearity. In [24], they are defined by the requirements of each standard.

- First of all the dynamic range of the receiver, DR_r , and the dynamic range of the signal, DR_{in} , are defined by,

$$DR_r = S_{max} - S_{min}, \quad (2.1a)$$

$$DR_{in} = S_{max} - P_{sens}, \quad (2.1b)$$

where S_{max} is the maximum signal that the receiver can process, S_{min} is the minimum signal that the receiver can detect and P_{sens} is the sensitivity of the receiver. The minimum gain of the RFFE depends also on S_{max} ,

$$G_a = S_{fs} - S_{max}, \quad (2.2)$$

where S_{fs} is the full-scale of the ADC. The signals' power are expressed in dBm and the dynamic ranges and gain are expressed in dB.

- The sensitivity of the receiver is the minimum signal that the receiver can process without degrading the bit error rate (BER),

$$P_{sens} = SNR_{in} + N_t, \quad (2.3a)$$

$$N_t = 10\log(kTB), \quad (2.3b)$$

where SNR_{in} is the signal-to-noise ratio at the input of the receiver, N_t is the thermal noise, k is the Boltzmann's constant, T is the temperature in Kelvin and B is the bandwidth of a channel.

- The signal-to-noise ratio at the output of the receiver, SNR_{out} , is defined by,

$$SNR_{out} = \frac{E_b}{N_0} \frac{R}{B}, \quad (2.4)$$

where E_b/N_0 is the signal energy per bits of information over the noise spectral density and R is the binary information rate.

The noise floor at the output, N_{out} , is given by,

$$N_{out} = S_{min} + G_a = N_t + NF + G_a, \quad (2.5)$$

where the noise figure, NF , of the receiver is

$$NF = SNR_{in} - SNR_{out}. \quad (2.6)$$

For standards such as GNSS, the *spread spectrum* (cf appendix A) technology is necessary in order to limit the risk of interferences with parasitic signals. A system needs to be spread spectrum if its bandwidth exceeds the minimum bandwidth necessary to receive the information [25]. The formula to determine the NF is slightly different because it has to take into account the spread gain, SG , and the coding gain, CG .

- The limitation due to the interferences with parasitic signals is also expressed through the linearity of the receiver and especially the third order input intercept point (IIP_3). The third order inter-modulation of the signal, IM_3 is a recombination of several input signal's harmonics by the system as shown in figure 2.2. Generally, we assume that the noise floor should be higher than the inter-modulation with a margin of 6 dB,

$$IM_3 < N_{out} - 6 \text{ dB}. \quad (2.7)$$

Based on the latter equation, the receiver must ensure,

$$IIP_3 > \frac{3}{2}P_{in} + \frac{1}{2}G_a - \frac{1}{2}IM_3, \quad (2.8)$$

where P_{in} is the input power.



FIGURE 2.2: Third order inter-modulations.

The analysis and derivation of the specifications can be illustrated according to the diagram proposed in figure 2.2. The receiver dynamic range (DR_r) would be larger than the dynamic of the signal (DR_{in}). The RF gain (G_a) imposed by the maximum collected signal

applies to the other specifications. The sensitivity (P_{sens}) defines the noise performance of the receiver (SNR_{out} and NF).

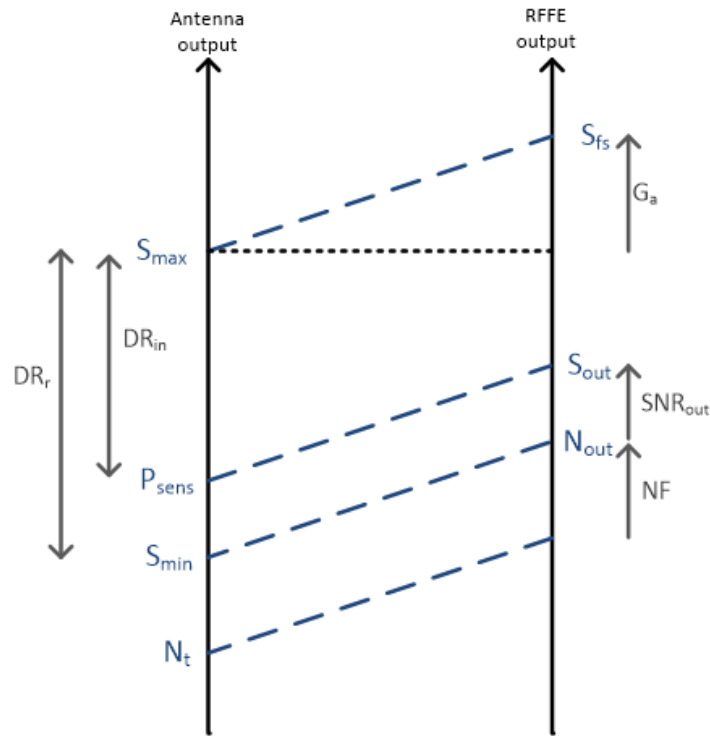


FIGURE 2.3: Summary of all the receiver's specifications.

This analysis of radio standards is sum up in figure 2.3. Given all of the equations aforementioned and the requirements listed in table 2.1, we can establish the following specifications for the receiver:

	GNSS	TMTC
G_a (dB)	100	90
NF (dB)	4	5
IIP_3 (dBm)	< -80	< -80
S_{11} (dB)	< -10	< -10
P_{DC} (W)	< 0.4	< 0.4

TABLE 2.2: Specifications for the GNSS & TMTC receiver.

The calculation of these specifications is based on equation (2.1) to equation (2.8). Considering these results, the architecture of the RFFE should now be chosen in order to ensure the expected performances.

2.1.2 Architecture of the receiver

Generally, a RFFE consists of a RF filter which filters the signal collected by the antenna, then a LNA which amplifies this signal and a mixer in order to convert the signal to baseband.

Finally, the signal carrying informations is filtered and delivered to the analog-to-digital converter. In the following formulas, the RF filter is not taken into account since its losses are as low as 0.2 dB and consequently, it has a minor impact on the RFFE's performances.

The total gain is the addition of each block's gain. The total noise, F_{Rx} , depends also on each block of the RFFE and is given by Friis formula,

$$F_{Rx} = F_{LNA} + \frac{F_1 - 1}{G_{LNA}} + \frac{F_2 - 1}{G_{LNA} * G_2} + \dots \quad (2.9)$$

where F_i and G_i are the noise and gain of the i-th block following the LNA. This formula shows that the most important block for the noise figure of the receiver is the LNA; if its gain is high enough (generally over 15 dB), then $F_{Rx} \approx F_{LNA}$.

Conversely, the $IIP_{3_{Rx}}$ is given by,

$$\frac{1}{IIP_{3_{Rx}}} = \frac{1}{IIP_{3_{LNA}}} + \frac{G_{LNA}}{IIP_{3_1}} + \frac{G_{LNA}^2 G_1^2}{IIP_{3_2}} + \dots \quad (2.10)$$

where IIP_{3_i} and G_i are the IIP_3 and gain of the i-th block following the LNA. Hence if the gain of the LNA is high enough, the IIP_3 becomes critical for the last stage of the receiver. Still it must be considered in the LNA to limit its impact on the receiver linearity.

A common solution to implement a multi-standard receiver is to put several narrow band receivers in parallel controlled by switches as illustrated in figure 2.4. This solution requires multiple chip achieving the same function which significantly increases the overall consumption, cost and footprint [26]. Furthermore, no additional standard can be added once the receiver is implemented. Another solution is to implement only one receiver following a wideband LNA that can process every frequencies in its band of operation [27]. We chose to implement the architecture presented in figure 2.5, since the footprint and power are restricted on nano-satellites.

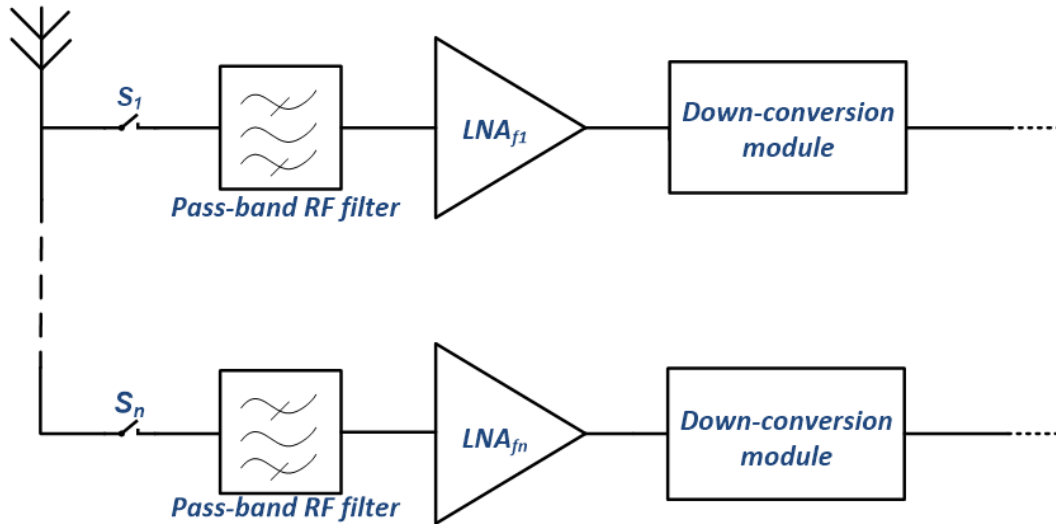


FIGURE 2.4: Architecture of a multiple-path RFFE including a LNA for each standard.

The down-converter Max2112 from Maxim Integrated is a fully integrated receiver. It performs the down conversion of the signal over a frequency range from 925 MHz to 2175 MHz with a supply voltage of 3.3 V and a supply current of 100 mA. It exhibits a total gain of 88 dB for a NF of 9 dB and a IIP_3 of 2 dBm. The architecture of the Max2112 is described in figure 2.5. It consists of a gain control amplifier (CGA), followed by mixers, CGAs and low pass filters to convert the signal to baseband.

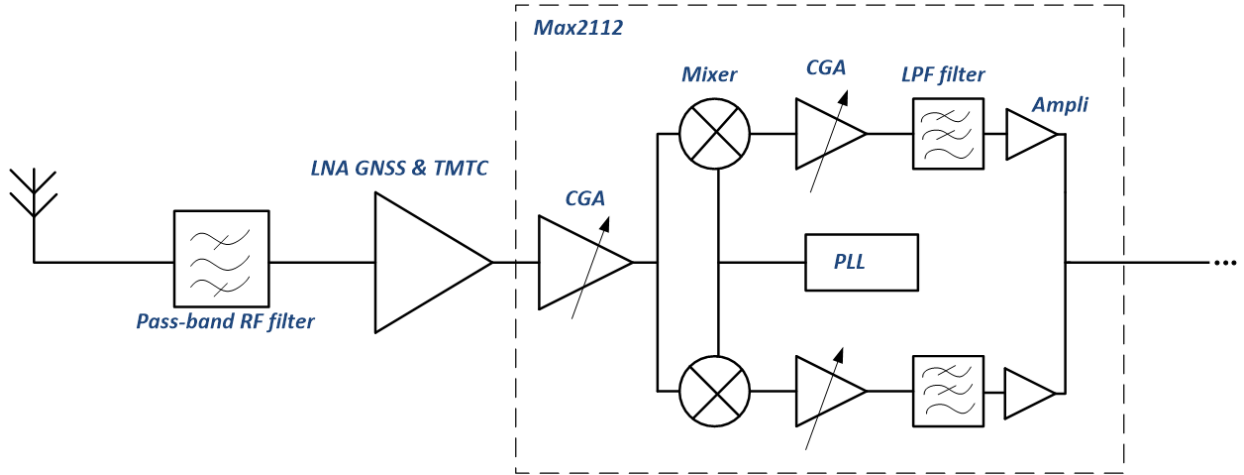


FIGURE 2.5: Architecture of the proposed RFFE including a wideband LNA operating at f_{GNSS} and f_{TMTC}

This down-converter has been chosen for the ELISE project since it can process both of GNSS and TMTC bands. However, according to equation (2.9) and the specifications listed above, a LNA should be placed before this component in order to address sensitivity and gain specifications of each targeted standard. In our case, the LNA should have a wideband matching from f_{GNSS} to f_{TMTC} as well as a NF lower than 1.5 dB and 2 dB at f_{GNSS} and f_{TMTC} , respectively, with a gain higher than 15 dB. Its design flow and performances are presented in the following sections.

2.2 LNA's design

2.2.1 Topology

For spatial applications, bipolar transistors offer a good trade-off between the die cost, the power consumption and the noise performance compared to others technologies.

Common topologies of LNA with bipolar transistors are presented in figure 2.6; the common emitter with inductive degeneration (a), the common base (b) and the common emitter with resistive feedback (c). Equation (2.9) shows that LNAs should present a very low noise figure while ensuring enough gain, linearity and bandwidth at a moderate power. Yet, each one of the topologies presented in figure 2.6 exhibits their own benefits and drawbacks [28].

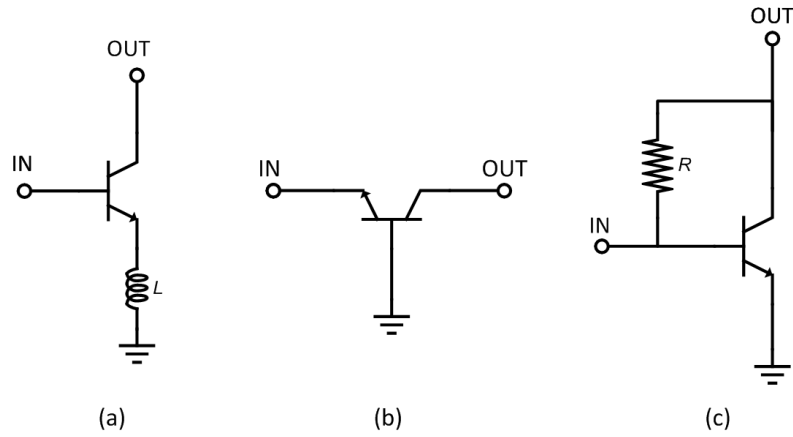


FIGURE 2.6: LNA topologies: (a) common emitter with resistive feedback, (b) common base and (c) common emitter with inductive degeneration.

The common emitter with inductive degeneration, figure 2.6a, achieves good performance but it is a narrow band configuration which is not suited for our case. The common base topology, figure 2.6b, achieves wide band operation but a limited noise figure (3 dB for the best case). Due to noise performance the common gate configuration cannot address NF targeted specifications. The resistive feedback architecture, figure 2.6c, exhibits wideband performance and possibly low noise figure. It has been selected for our project.

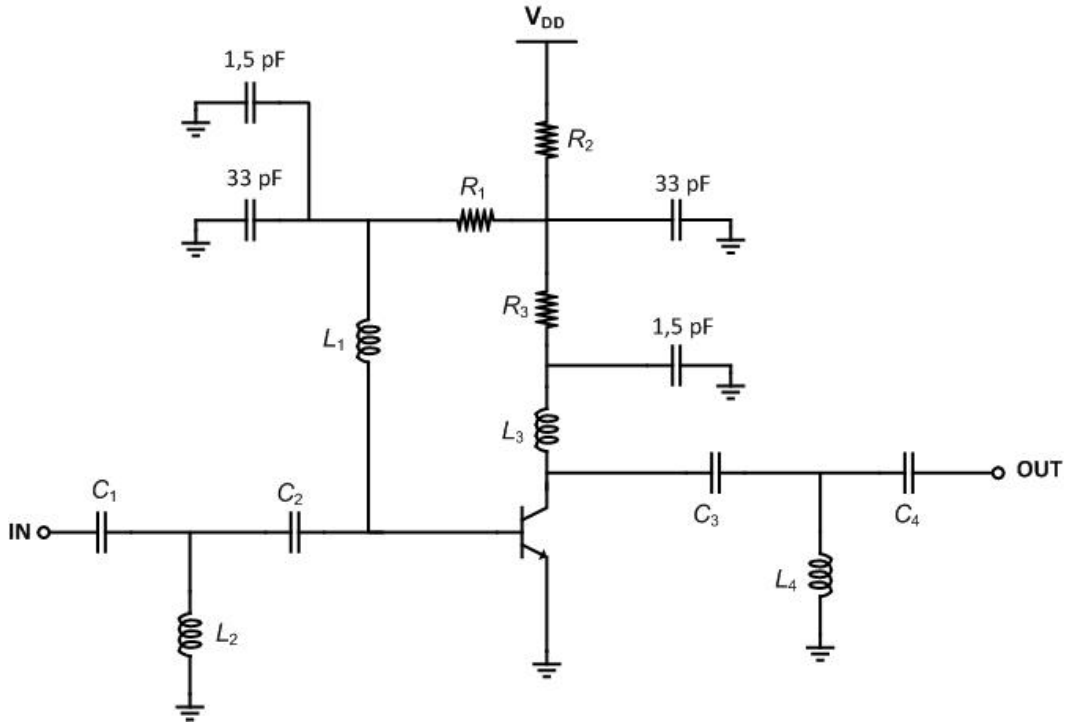


FIGURE 2.7: Topology of the proposed LNA with COTS.

The proposed LNA, presented in figure 2.7, has been chosen for its wideband matching. It is developed from a bipolar transistor in common emitter mode with a resistive feedback path. It consists of:

- three resistances R_1 , R_2 and R_3 which are part of the biasing network of the transistor (section 2.2.2.1),
- inductances L_1 and L_3 that ensure the stability of the LNA and also act as part of the input and output impedance matching networks (section 2.2.2.2),
- inductances and capacitances L_1 , L_2 , C_1 and C_2 which act as the input impedance matching network (section 2.2.2.3),
- inductances and capacitances L_3 , L_4 , C_3 and C_4 which act as the output impedance matching network (section 2.2.2.3),
- two capacitances of 1.5 pF and two capacitances of 33 pF which are the decoupling capacitors of the circuit.

2.2.2 Design flow

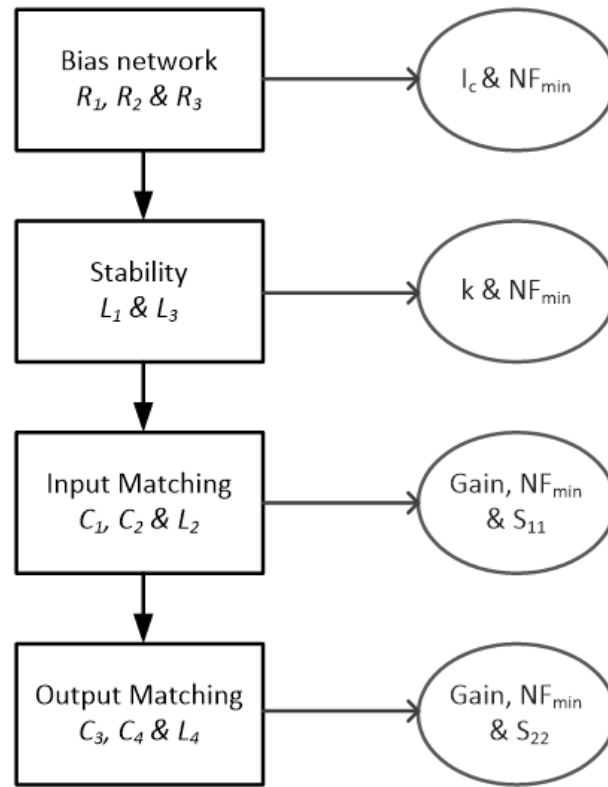


FIGURE 2.8: Design flow for a LNA in COTS technology.

The design flow for the proposed LNA consists of three main steps: the biasing of the transistor to ensure a low noise figure, the stabilization of the circuit and the matching of input and output impedance to ensure a high gain and input/output matching over a wide bandwidth [29]. The design flow is presented in figure 2.8 and described in the following subsections.

2.2.2.1 Bias

The bipolar transistor implemented in this LNA is the Infineon's BFP 640. It exhibits a minimum noise figure of 0.65 dB at 1.8 GHz when its collector current, I_C , is close to 6 mA (figure 2.9). It is also shown that at this current, the power matching is very similar to the noise matching since the optimal noise impedance Z_{Sopt} is close to 50 Ω .

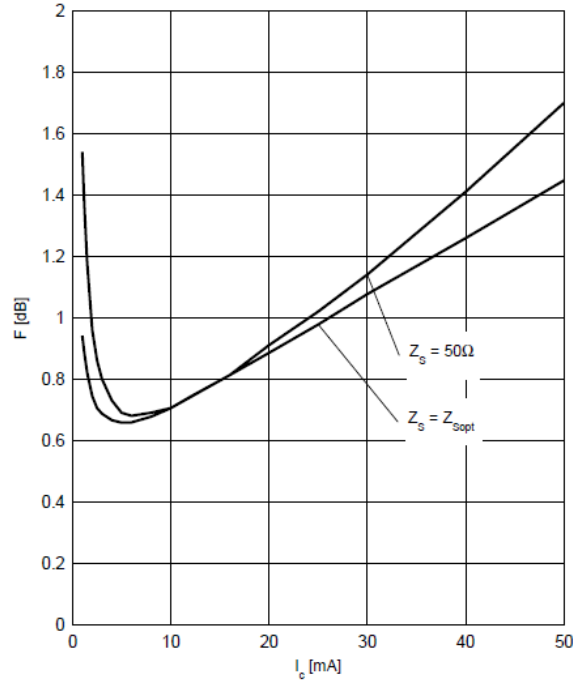


FIGURE 2.9: Noise figure of the transistor versus its collector current I_C at 1.8 GHz.

Source: Infineon datasheet

To tune the bias current to I_{opt} (6 mA) with a V_{DD} equal to 3.3 V, the resistors R_1 , R_2 and R_3 are respectively set to 80 k Ω , 100 Ω and 250 Ω .

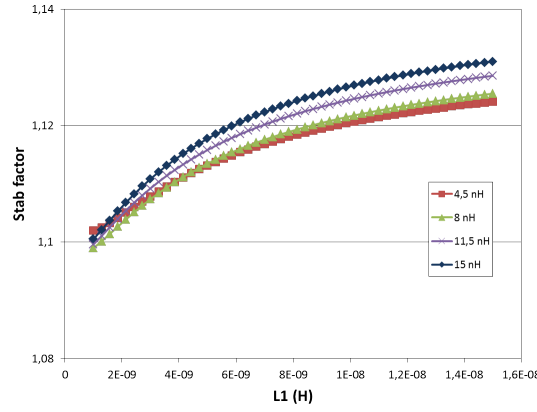
2.2.2.2 Stability

A circuit is assumed stable if its stability factor, the Rollet coefficient, k , is greater than 1 and if the absolute value of Δ is inferior to 1,

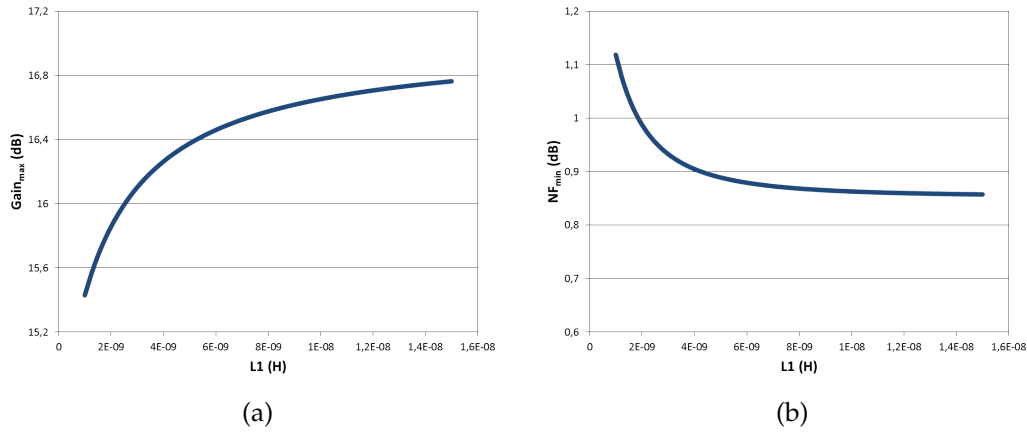
$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|}{2|S_{12}||S_{21}|} > 1 \quad (2.11a)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} < 1 \quad (2.11b)$$

The stability factor is plotted versus L_1 for different values of L_3 , between 1 and 15 nH, with the help of ADS simulator. We chose not to go beyond these values of inductances since their parasitic resistances may degrade the performance of the LNA. Figure 2.10 shows that for any values of L_1 and L_3 , the stability is ensured since it is always larger than 1. Furthermore, the stability factor increases with the value of these inductances.

FIGURE 2.10: Stability factor versus L_1 and L_3 .

Beside, the inductances have an impact on the minimum noise figure and the maximum gain. Their evolutions with L_1 for different values of L_3 are plotted in figure 2.11. The inductances are set to $L_1 = 15$ nH and $L_3 = 15$ nH, in order for NF_{min} to be as low as possible and G_{max} to be as high as possible.

FIGURE 2.11: (a) G_{max} and (b) NF_{min} versus L_1 and with $L_3 = 13$ nH.

The gain and noise of the LNA will be close to the values of NF_{min} and G_{max} studied here, only if its input and output impedances are matched to the source and load impedances, respectively. This is the goal of the next step.

2.2.2.3 Impedance matching

In order to transmit the maximum of power from the source to the LNA, the source impedance must be the conjugate of the LNA's input impedance.

$$Z_S = Z_L^* \quad (2.12)$$

Hence, a matching network is placed between the source and the LNA's core as shown in figure 2.12. The same thing is done to match the output of the LNA to the input of the Max2112.

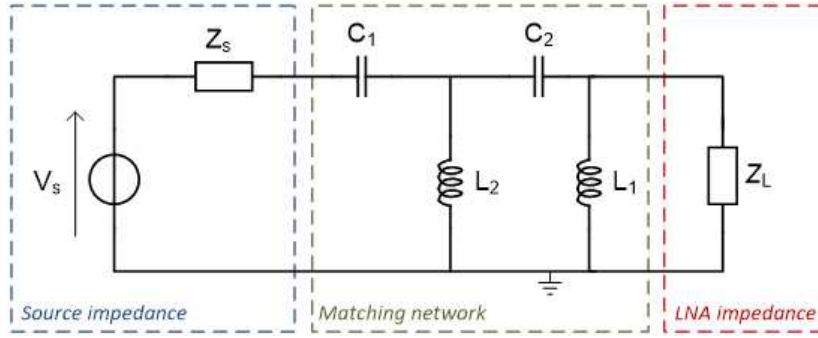


FIGURE 2.12: Input impedance matching.

The level of matching is represented by the return loss coefficients S_{ii} , conventionally S_{11} at the input and S_{22} at the output. Accounting for the source impedance Z_S and the input impedance of the LNA, Z_L , the input return loss S_{11} is derived in equation (2.13). Under matching condition described in equation (2.12), S_{11} is very low. In practice, we assume impedance matching at a return loss below -10 dB for RF blocks.

$$S_{11} = \frac{Z_L - Z_S}{Z_L + Z_S}. \quad (2.13)$$

In the previous subsection, part of the matching networks was set (L_1 and L_3). The rest of these networks will be calculated following the method described in [30]. The steps of this calculation are presented in figure 2.13.

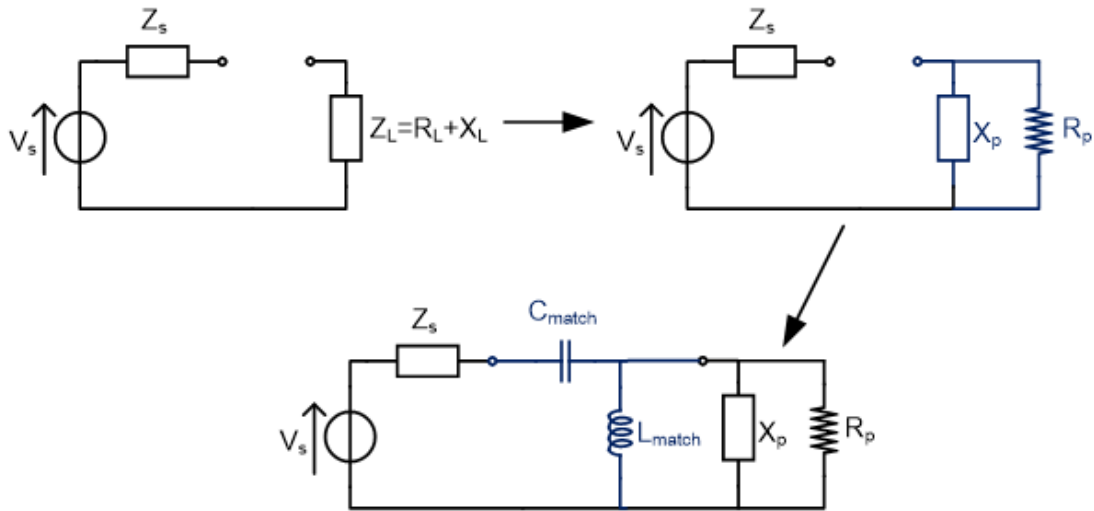


FIGURE 2.13: L-network for narrow band matching.

For narrow band matching, a simple L-network is necessary. First of all, the impedance at the input or output of the circuit must be extracted from a S-parameters simulation on ADS at the operating frequency. This impedance consists of a resistance R_L and reactance X_L . It is necessary to start by converting this impedance to its parallel equivalent,

$$R_p = R_L(1 + Q^2), \quad (2.14a)$$

$$X_p = \frac{R_p}{Q}, \quad (2.14b)$$

where Q is the quality factor given by,

$$Q = \frac{X_L}{R_L}. \quad (2.15)$$

Then, the next step consists of setting R_p to 50Ω (Z_s) with the help of an inductance or a capacitance and then to compensate the imaginary part with an inductance if X_p is negative or a capacitance if X_p is positive.

However, since the proposed LNA is expected to achieve input matching at both GNSS and TMTC frequency bands, two cascaded L-network are necessary in order to lower the quality factor and hence to widen the bandwidth. The details of the calculation for our targeted frequencies are presented in appendix B.

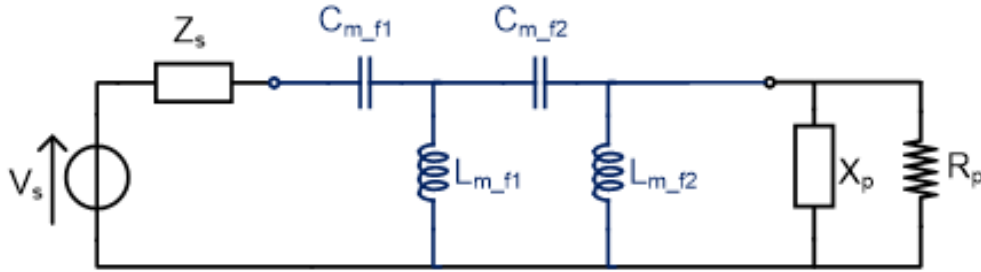


FIGURE 2.14: Cascaded L-network for wideband matching.

The power matching described in this subsection is different than the noise matching [31]. In figure 2.15, an example of noise and gain circles are plotted in the Smith chart. They are very close but not exactly similar.

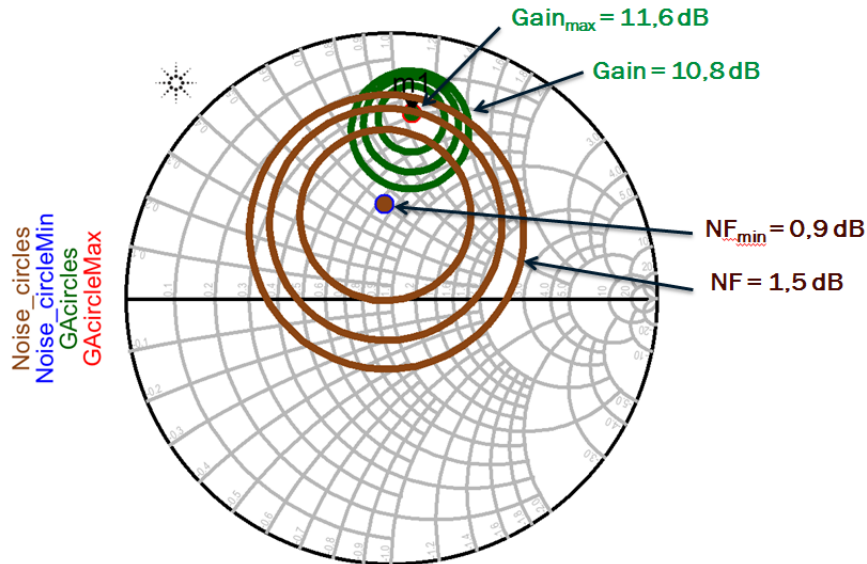


FIGURE 2.15: Noise figure and voltage gain circles.

Therefore, a trade-off between power matching and noise matching needs to be performed in order to ensure a low NF while keeping the S_{11} below -10 dB. Yet, in section 2.2.2.1, we have chosen a current collector for which the optimal impedance is close to $50\ \Omega$. Since the RF filter has an impedance of $50\ \Omega$, we further assume that noise and impedance matching conditions are similar.

In this section, the complete design flow of the proposed LNA has been detailed. The resulting LNA is presented in section 2.3.

2.3 Implementation and results

The specifications of the LNA have been established in the previous sections and are summarized in table 2.3.

Performance	Specification
freq (GHz)	1.575 & 2.11
S_{21} (dB)	> 15
S_{11} (dB)	< -10
S_{22} (dB)	< -10
NF (dB)	< 1.5
R_s (Ω)	50
R_L (Ω)	75
Supply voltage (V)	3.3
Current consumption (mA)	< 10

TABLE 2.3: Specifications for the GNSS & TMTC LNAs.

Following the design steps defined in section 2.2 in order to ensure these specifications, we have designed a LNA which operates from f_{GNSS} to f_{TMTC} . A supply voltage of 3.3 V is provided by the satellite and the circuit consumes 6 mA. The inductances and capacitances have been calculated to ensure stability, matching to $50\ \Omega$ at the input and matching to $75\ \Omega$ at the output.

2.3.1 Layout

The LNA is implemented on a two-layer FR4 substrate with a width of 0.8 mm. The top layer is presented in section 2.3.1. The ground plane is on the bottom layer. The ground planes of the bottom layer and the top layer are connected by vias with a diameter of 0.6 mm.

$50\ \Omega$ -lines have been calculated based on the substrate property (table 2.4) and the frequency of operation. In our case, they should be 1.44 mm wide.

Parameters	Symbol	Values
Permittivity	ϵ_r	4.5
Substrate's loss	$\tan\Delta$	0.016
Copper height	T (μm)	35
Substrate height	H (mm)	0.8
Conductivity	C	5.8e7

TABLE 2.4: Property of the FR4 substrate.

In the layout presented in figure 2.16a, the 50Ω -lines are the input and output lines, on which the SMA connectors will be soldered. The rest of our lines are 0.5 mm wide in order to fit with the components' package which is 0402 (1 mm x 0.5 mm). A picture of the resulting PCB is proposed in figure 2.16b.

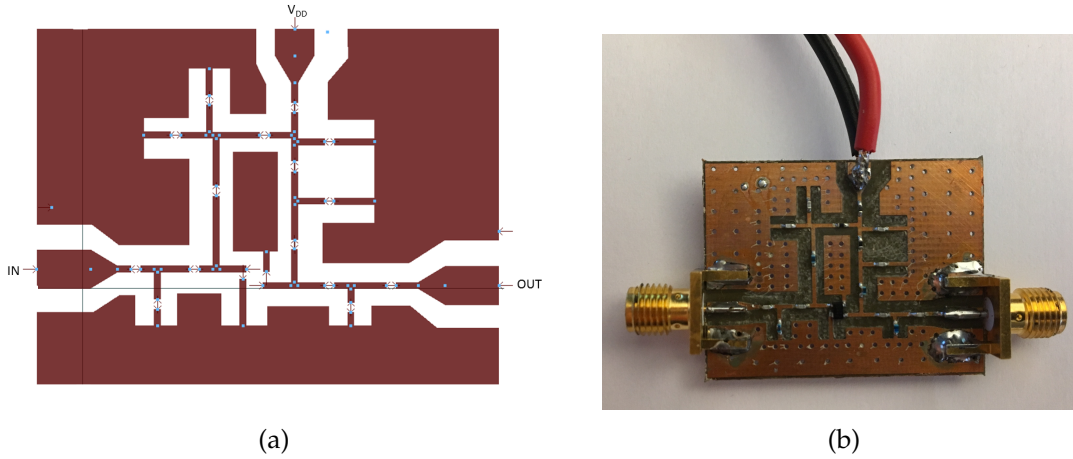


FIGURE 2.16: (a) Layout of the proposed LNA and (b) picture of the PCB.

This layout has been simulated with ADS electromagnetic simulator, in order to include the parasitics brought by the interconnections. These parasitics shifts the frequency of the circuit, therefore the passive components must be tuned to ensure the right frequency of operation.

2.3.2 Wideband LNA

The results of the wideband LNA are presented in table 2.5 and table 2.6 at the frequencies of operation, f_{GNSS} and f_{TMTC} . The measurement results address the expected specifications. The noise figure is very low with a minimum of 0.9 dB at f_{GNSS} . The voltage gain is higher than expected for both frequencies but the input and matching is not as good as predicted due to layout parasitics.

The evolution of the S-parameters is illustrated from 1.5 GHz to 2.5 GHz in figure 2.17. The measurement fits the simulation even if S_{11} is slightly above because of the parasitics which are not taken into account during the electromagnetic simulation. S_{22} is the output return loss coefficient, which represents the matching at the output of the LNA. It is below -

LNA	Simulation	Measure
NF (dB)	0.8	0.9
S_{11} (dB)	- 11,6	- 9
S_{22} (dB)	- 22	- 18
S_{21} (dB)	17.5	19
I_C (mA)	6	6

TABLE 2.5: Results of the wideband LNA at f_{GNSS} .

LNA	Simulation	Measure
NF (dB)	0.9	1.3 - 1.1
S_{11} (dB)	- 14.5	- 11
S_{22} (dB)	- 12	- 14.8
S_{21} (dB)	15.1	15.8
I_C (mA)	6	6

TABLE 2.6: Results of the wideband LNA at f_{TMTC} .

10 dB at both frequencies of operation. S_{21} is the gain of the LNA, it is above 15 dB from 1.5 GHz to 2.1 GHz as requested by the specifications.

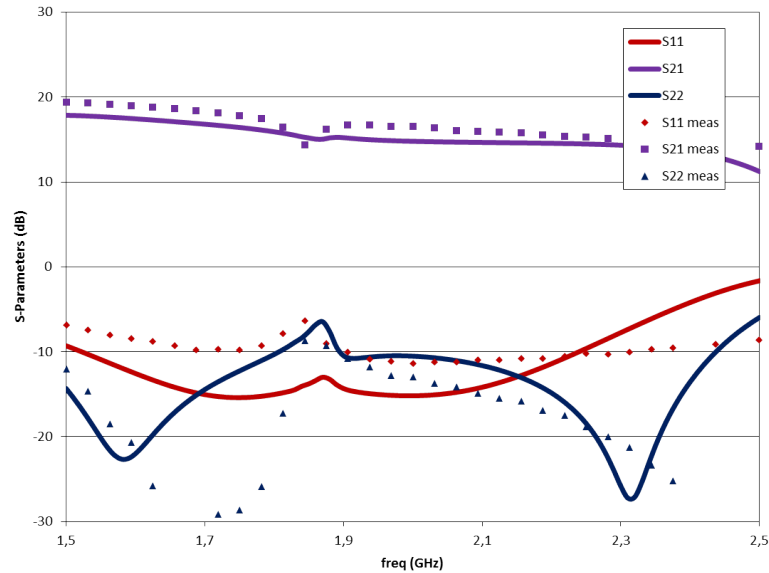


FIGURE 2.17: S-parameters versus frequency, comparison between simulation and measure.

NF and NF_{min} are plotted in figure 2.18. In simulation very low NF are achieved: at both frequencies, they are below 1 dB. The measurement shows that NF_{GNSS} is equal to 0.9 dB and NF_{TMTC} is equal to 1.2 dB. The difference with the simulation is due to the noise matching which is better at f_{GNSS} than at f_{TMTC} (NF closer to NF_{min}). Furthermore, the

peak of NF at 1.85 GHz is due to its location between the two poles of the matching network. During measurement, it is also amplified by the interferences with GSM communications at 1.8 GHz.

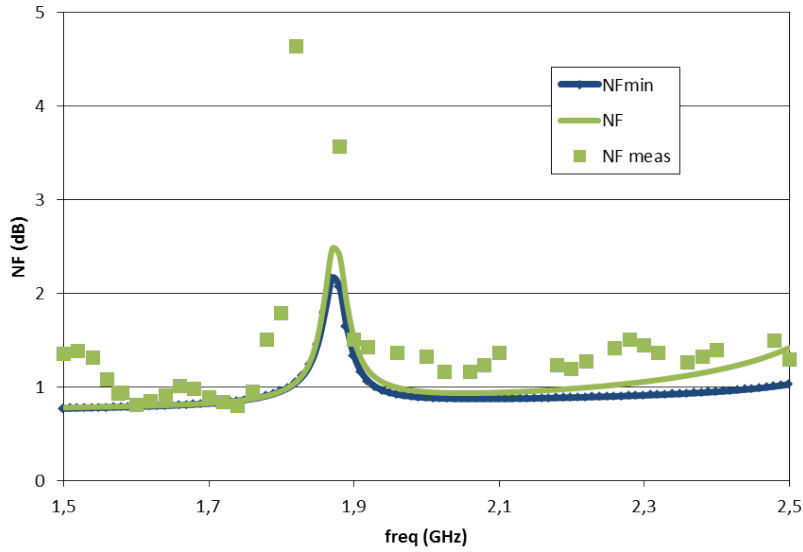


FIGURE 2.18: Noise figure versus frequency, comparison between simulation and measure.

The results of the proposed wideband LNA are compared to state of the art LNAs in table 2.7 with a figure of merit, given by,

$$FoM = \frac{G * BW}{P_{DC} * (F - 1)}, \quad (2.16)$$

where G is the gain of the LNA in linear units, BW is the bandwidth in GHz, P_{DC} is the power consumption in mW and NF is the noise figure in linear units.

TABLE 2.7: State of the art of LNAs with COTS.

Ref.	Freq. (GHz)	BW _{-3dB} (MHz)	NF (dB)	Gain (dB)	P _{DC} (mW)	FoM
[29]	1.3989	1.2	2.2	18.5	93	0.16
[31]	2.5	1.8	0.5	16	12.2	7.6
[32]	0.136-0.941	805	1	17.5-18.5	600	0.04
[33]	4	1.5	0.8	22	110	0.8
This work	1.5-2.1	2	0.8-1	19-16.3	20	4.4

In [29], [32] and [33], the LNA topologies are similar to our LNA but they consume significantly more power for similar performances. Thus, their FoM is lower than [31] and this work. [31] privileged a low consumption and low noise whereas their S_{11} is around -5 dB which means that their LNA is not matched at the input. This shows that designers often privileged some performances over the others. On the contrary, the design flow presented in this chapter tries to optimize each performance simultaneously.

Conclusion

In this chapter, the different characteristics and trade-offs of LNA design were presented. A design flow is developed to answer the needs of the ELISE project: an LNA in COTS technologies, for spatial applications, that can operate at two different frequencies in order to address two communication standards. This methodology leads to the implementation of a wideband LNA which exhibits a minimum NF of 0.9 dB for a gain of 19 dB and a power consumption of 20 mW.

However, design flows are highly dependent on the technology choice. COTS offer several advantages such as high-Q passive components and simple models which enable a simple and fast design. Yet, this technology has many drawbacks because of its large footprint, its optimization limited by the set of dimensions and reconfigurability is difficultly achievable. Therefore this design flow is not suited for other applications such as connected devices (smartphone, tablets, etc) and in general for mass market applications since the main constraint is on cost, footprint and reconfigurability. For these applications silicon integrated technologies are preferred. The following chapters of this thesis will focus on a design flow for integrated LNAs with CMOS technologies.

Chapter 3

Design methodology based on the Inversion Coefficient

In the first chapter, the need for reconfigurable multi-standard and multi-mode LNAs in CMOS process has been discussed. In the second chapter, a dual band LNA covering GNSS and TMTC standards has been demonstrated for satellite applications. Due to the equipment specifications and the application environment, this LNA is developed with COTS devices on a FR4 PCB. However, the need for reconfiguration capability, high integration, low cost and power saving calls up for silicon integration, and more specifically CMOS process, for the implementation of advanced radio modules. Beside, navigating through the multi-variables design space of LNAs and the constant evolution of CMOS technologies are important challenges for RF designers (chapter 1). Therefore, simple and accurate design flows need to be developed. Specifically, such design flows should be: compliant with any generation of CMOS technology, adjusted to circuit topologies and capable of addressing any set of specifications.

An innovative circuit design methodology for LNAs, based on the Inversion Coefficient, IC , [34], is detailed in this chapter. It enables a simple and accurate design approach through analytical equations of the circuit's performance, avoiding extensive parametric simulations. This methodology consists of three main steps, illustrated in figure 3.1:

- the normalization of the MOS model to technological parameters with the EKV model and the IC ,
- the description of the circuit with the EKV model and the IC ,
- the sizing of the circuit to address a set of specifications and its optimization with a Figure Of Merit (FoM)

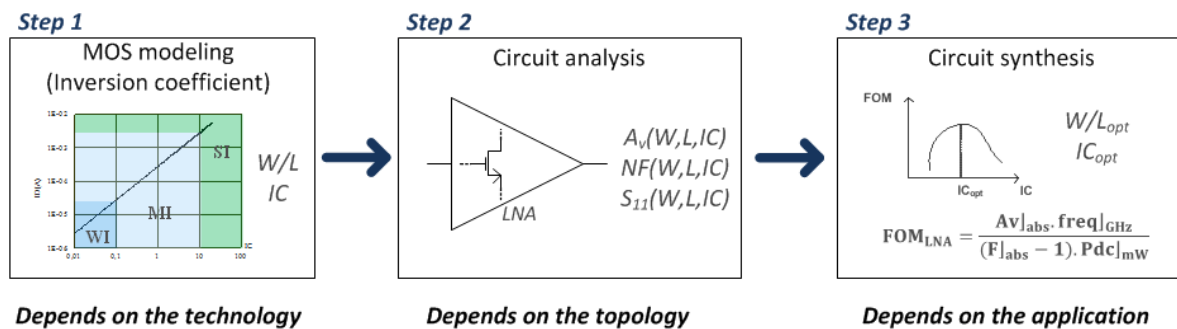


FIGURE 3.1: Design methodology based on the inversion coefficient.

This chapter described each step of the methodology through the examples of three technologies (28 nm FDSOI, 65 nm and 130 nm) and two common LNA's topologies (cascode and current reuse) for a low power application at 2.4 GHz.

3.1 EKV model and inversion coefficient

The EKV model for MOS transistors has been developed by C. Enz, F. Krummenacher and E.A Vittoz [34, 35]. It is an accurate and predictive model of MOS transistors' behavior, continuously in all regions of operations. This section presents all the parameters of the EKV model.

3.1.1 Inversion Coefficient

The IC is a normalization of the drain current, I_D , to the specific current, I_{spec} , which consists of technological parameters and the geometry of the transistor,

$$IC = \frac{I_D}{I_{spec}} = \frac{I_D}{I_{spec\Box} \frac{W}{L}}, \quad (3.1a)$$

$$I_{spec\Box} = 2n\mu_n C_{ox} U_T^2, \quad (3.1b)$$

where L and W are the gate length and width of a transistor, n is the slope factor, μ_n is the constant low-field mobility, C_{ox} is the oxide capacitance per unit area and $U_T = kT/q = 26$ mV is the thermodynamic voltage at standard room temperature. The method to extract the values of $I_{spec\Box}$ and n of a transistor will be further described (see section 3.1.3).

The value of the IC indicates the level of inversion of a transistor, regardless of the technology or the size of this transistor:

- $IC < 0.1$, the transistor is biased in weak inversion (WI),
- $0.1 < IC < 10$, the transistor is biased in moderate inversion (MI),
- $IC > 10$, the transistor is biased in strong inversion (SI).

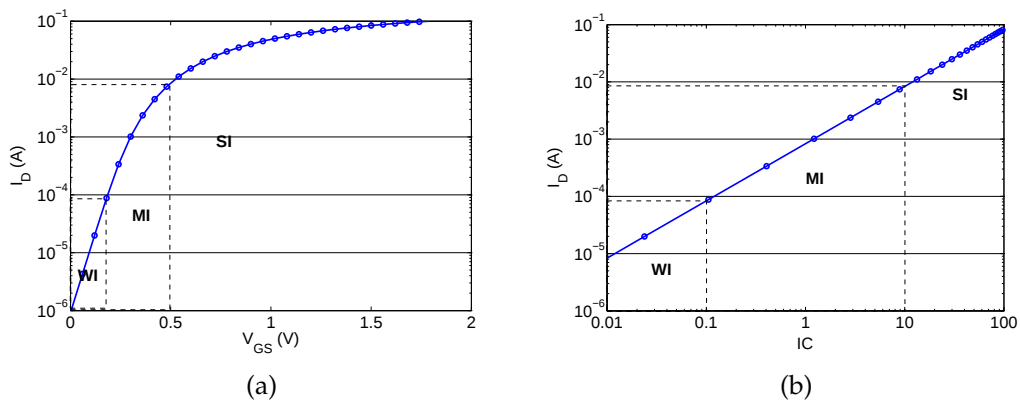


FIGURE 3.2: (a) I_D versus V_{GS} and (b) I_D versus the IC for a transistor with a gate width of 50 μm in 28 nm FDSOI.

The drain current of a MOS transistor in 28 nm FDSOI is plotted versus the gate source voltage, V_{GS} , in figure 3.2a and versus the IC in figure 3.2b. Figure 3.2a shows that the SI region spans over a wide range of voltage to cover only one decade of current, whereas the WI and MI regions cover six decades of current from 0 to 0.5 mV. On the other hand, figure 3.2b shows that one decade of current is covered by one decade of the IC . The IC is more convenient for modelling MOS devices in WI and MI regions than V_{GS} .

3.1.2 Small-signal model

The small-signal model of a transistor, valid for all inversion regions, is presented in figure 3.3. It consists of a passive part, an active part and two noises sources which depend on the geometry of the transistor and the IC .

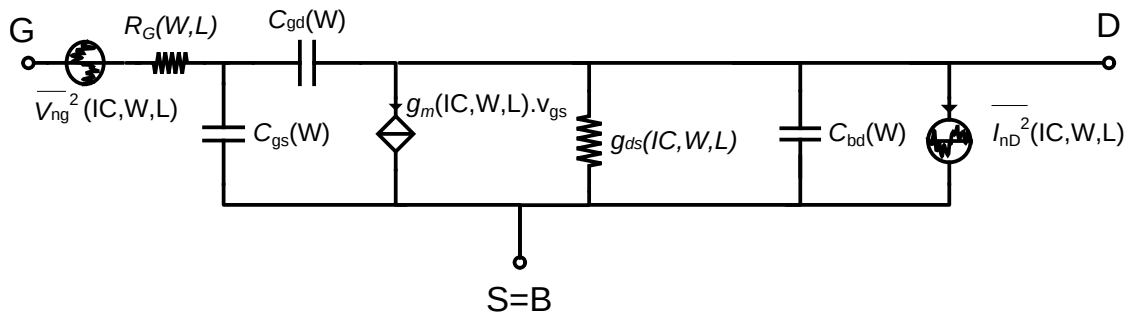


FIGURE 3.3: Small-signal model of a MOS including noise sources.

Active part

Similarly to the drain current, the transconductance, g_m , can be normalized to a specific parameter, G_{spec} , which depends on the specific current, I_{spec}

$$G_m = \frac{g_m}{G_{spec}} = \frac{g_m}{I_{spec}/U_T}. \quad (3.2)$$

It can also be represented as a function of the IC and accounts for the velocity saturation coefficient, λ_c [36]:

$$G_m(IC) = \frac{1}{n} \frac{\sqrt{(\lambda_c IC + 1)^2 + 4IC} - 1}{\lambda_c(\lambda_c IC + 1) + 2}, \quad (3.3)$$

where n is the slope factor. The velocity saturation is a short-channel effect (SCE) that occurs for transistors with a gate length smaller than 200 nm. For longer transistors, $\lambda_c = 0$. It is defined in [37] by,

$$\lambda_c = \frac{2\mu_0 U_T}{v_{sat} L}, \quad (3.4)$$

where μ_0 is the surface mobility, v_{sat} is the saturation velocity and L is the transistor's gate length. The impact of velocity saturation on a short-channel transistor is illustrated in

figure 3.4a. It is significant in the SI region where larger IC , i.e. more current, will be required to reach the same g_m .

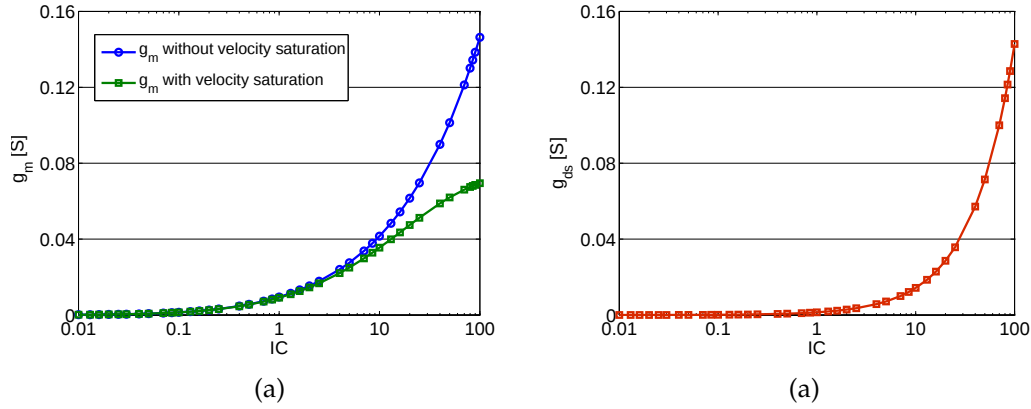


FIGURE 3.4: (a) g_m versus the IC with and without velocity saturation and (b) g_{ds} versus the IC for a transistor with a gate width of 40 μm in 28 nm FDSOI.

The conductance, g_{ds} , also depends on the IC and the geometry of the transistor,

$$g_{ds}(IC) = IC \frac{I_{spec}}{\alpha_{g_{ds}} L}, \quad (3.5)$$

where $\alpha_{g_{ds}}$ is a technological parameter. The evolution of the conductance versus the IC is plotted in figure 3.4b. In the WI and MI regions, g_{ds} remains low but in SI it significantly increases with the IC .

Passive part

When operating in radio-frequencies, the MOS transistor model must account for the parasitic resistance at the gate, R_G , and the parasitic capacitances between gate, drain, source and bulk, C_{gd} , C_{bd} and C_{gs} (see figure 3.3). These intrinsic capacitances and resistance are proportional to the transistor's size,

$$C_{gd} = C_{gdw} W, \quad (3.6a)$$

$$C_{bd} = C_{bdw} W, \quad (3.6b)$$

$$C_{gs} = C_{gsw} W, \quad (3.6c)$$

$$R_G = \frac{W_f}{N_f L_f} R_{G\Box}, \quad (3.6d)$$

where C_{gdw} , C_{bdw} , C_{gsw} and $R_{G\Box}$ are technological parameters, N_f is the number of fingers of the transistor and (W_f, L_f) characterize the fingers' size.

For the extractions of parasitics, a simple S-parameters simulation is necessary, to plot the following parameters,

$$C_{gd} = -\frac{\text{imag}(Y_{12})}{\omega}, \quad (3.7a)$$

$$C_{bd} = \frac{\text{imag}(Y_{22})}{\omega} - C_{gd}, \quad (3.7b)$$

$$C_{gs} = \frac{\text{imag}(Y_{11})}{\omega} - C_{gd}, \quad (3.7c)$$

$$R_G = -\frac{\text{real}(Y_{11})}{[\text{imag}(Y_{11})]^2}. \quad (3.7d)$$

Then, the values are divided by the gate width of the simulated transistor in order to find C_{gd_w} , C_{bd_w} , C_{gs_w} and $R_{g\Box}$.

Noise model

In a MOS transistor, there are two thermal noise sources generated by the drain current and the gate parasitic resistance, respectively modelled by a current noise source and voltage noise source in figure 3.3. The noise spectral densities are given by,

$$\overline{I_{nD}^2}(IC, W) = 4kT\gamma_n(IC)g_m(IC, W)\Delta f, \quad (3.8a)$$

$$\overline{V_{rG}^2}(W) = 4kTR_G(W)\Delta f. \quad (3.8b)$$

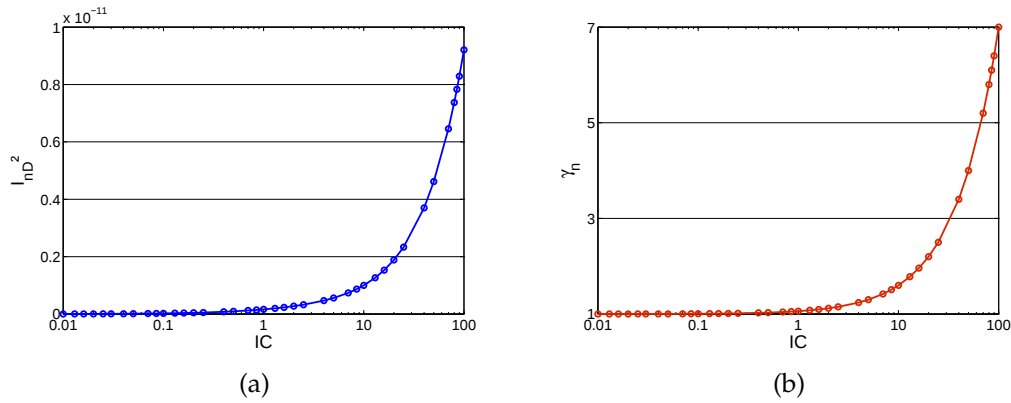


FIGURE 3.5: (a) I_{nD} versus the IC and (b) γ_n versus the IC for a short-channel transistor in 28 nm FDSOI.

According to equation (3.8b), $\overline{V_{rG}^2}$ is a function of transistor size only, whereas $\overline{I_{nD}^2}$ (equation (3.8a)), which is the main noise contribution, is a function of transistor size and bias through g_m . Furthermore, it is proportional to the thermal excess noise factor, γ_n . For short-channel transistors, γ_n depends on the level of inversion [38]:

$$\gamma_n(IC) = 1 + \alpha_{\gamma_n} IC, \quad (3.9)$$

where α_{γ_n} is a technological parameter. The evolution of $\overline{I_{nD}^2}$ and γ_n with the IC is plotted in figure 3.5. In the WI and MI regions, γ_n is around 1, it increases to 7 in the SI region. The thermal noise I_{nD} follows the evolution of γ_n as illustrated in figure 3.5a.

3.1.3 Technology comparison

In order to use the IC in a design methodology, the technological parameters defined in this section must be extracted first. The extraction procedure is described in [22]. It has to be performed only once for each process since technological parameters do not depend on the size of transistors. To determine $I_{spec\Box}$, n and λ_c of a transistor, its characteristic g_m/I_d versus I_d must be plotted. Then, considering equation (3.1a) and equation (3.2),

$$\frac{G_m}{IC} = \frac{g_m}{I_d} n U_T. \quad (3.10)$$

The evolution of G_m/IC with the IC is plotted in figure 3.6. For long channel transistors, the slope is close to $1/\sqrt{IC}$ and for short channel transistors the slope is close to $1/IC\lambda_c$. The first asymptote is equal to 1 when $IC = 1$, whereas the latter is equal to 1 when $IC = 1/\lambda_c$.

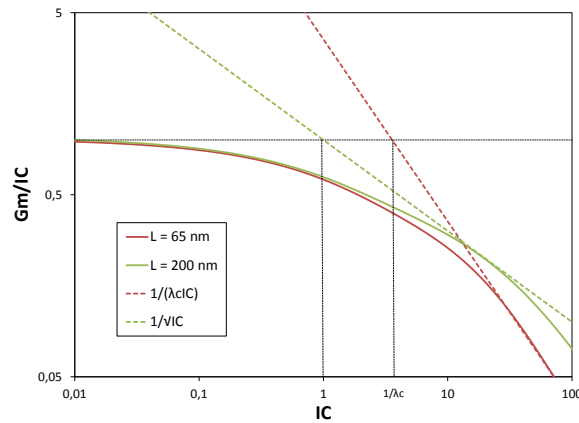


FIGURE 3.6: Evolution of G_m/IC versus IC for a NMOS transistor in 65 nm with $W = 10\mu\text{m}$.

The technological parameters of three CMOS nodes (28 nm FDSOI, 65 nm and 130 nm) have been extracted and are reported in table 3.1.

The three nodes presented in table 3.1 can be compared through their technological parameters. The specific current, $I_{spec\Box}$, decreases with technology shrink; for the same level of inversion and W/L ratio, advanced technologies consume less current. Since SCEs have a stronger impact on smaller devices, the slope factor, n , and the velocity saturation coefficient, λ_c , increase with the decrease of the gate length. Finally, parasitic capacitances per length remain in the same range over different technology process with 0.5 to 0.8 fF/ μm for C_{gs_w} and 0.2 to 0.5 fF/ μm for C_{gd_w} . As a consequence, the absolute value of parasitic capacitances tends to decrease with technology shrink for a fixed ratio W/L . The transit frequency, f_T , and the gain-bandwidth product, GBW , directly benefit from it. Hence, analog and RF circuits with a larger bandwidth and/or reduced power consumption can be expected in advanced CMOS process.

TABLE 3.1: Technological parameters to be extracted and their values for NMOS transistors in 28nm FDSOI, 65nm, 130nm.

Parameter	130 nm	65nm	28 nm FDSOI
$I_{spec\Box} (\mu A)$	1.1	0.9	0.8
n	1.3	1.4	1.5
λ_c	0.3	0.4	0.6
α_{γ_n}	0.07	0.07	0.07
$C_{gs_w} (fF/\mu m)$	0.71	0.5	0.8
$C_{gd_w} (fF/\mu m)$	0.56	0.25	0.22
$C_{bd_w} (fF/\mu m)$	0.01	0.1	0.06

3.2 Circuit analysis

Based on the EKV model described in the previous section, two common LNA topologies are studied here; a cascode and a current reuse. They are presented in figure 3.7 and the performances (input matching, voltage gain and noise figure), at 2.4 GHz, are calculated in the following subsections.

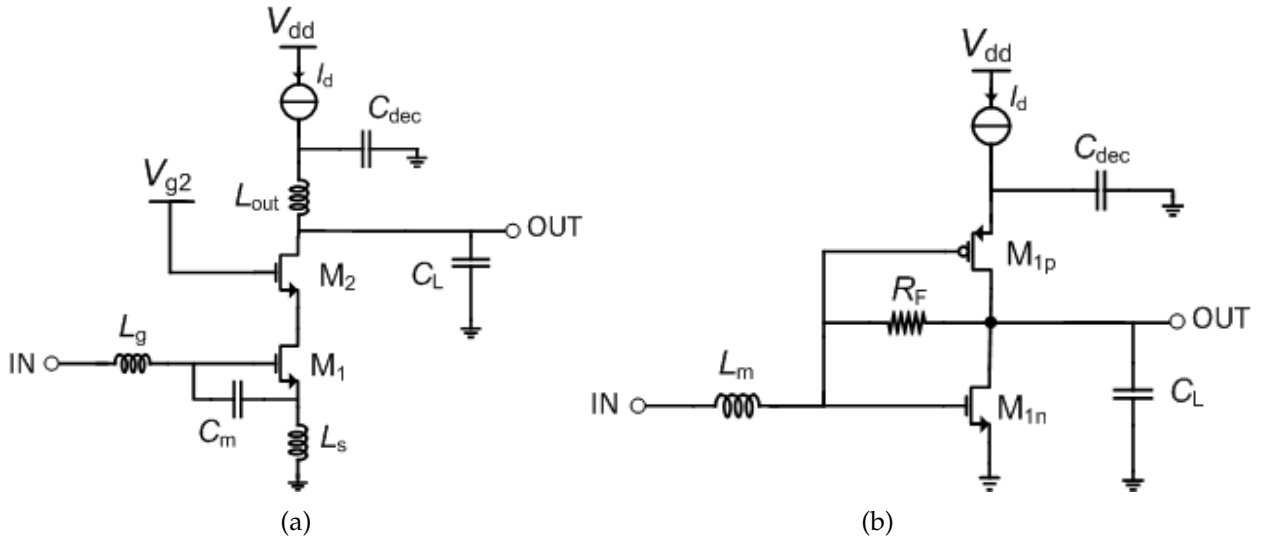


FIGURE 3.7: Schematics of the (a) cascode topology and (b) current reuse topology.

The first topology consists of two cascoded NMOS, M_1 and M_2 , an input matching network with L_g , L_s and C_m and an output matching network with L_{out} and the load capacitance C_L . The second topology is a current reuse which consists of a PMOS transistor and a NMOS transistor, an inductance L_m which is part of the matching network and a load capacitance C_L .

In the cascode, the transistors M_1 and M_2 have the same drain current, I_d . Hence, considering equation (3.1a) and assuming that they have the same gate length,

$$IC_2 = IC_1 \frac{W_1}{W_2}. \quad (3.11)$$

The PMOS, M_{1p} , and the NMOS, M_{1n} , have the same drain current. Similarly to the cascode configuration and considering that $I_{spec_{□n}}$ is the specific current of M_{1n} and $I_{spec_{□p}}$ is the specific current of M_{1p} ,

$$IC_{1n} = IC_{1p} \frac{W_{1p} I_{spec_{□p}}}{W_{1n} I_{spec_{□n}}}. \quad (3.12)$$

For small-signal analysis, the current reuse arrangement is modelled as a single common source M_{eq} featuring the contribution of M_{1p} and M_{1n} as follows:

$$g_{m_{eq}}(IC_{1n}, W_{1n}, W_{1p}) = g_{m_{1n}}(IC_{1n}, W_{1n}) + g_{m_{1p}}(IC_{1p}, W_{1p}), \quad (3.13a)$$

$$g_{ds_{eq}}(IC_{1n}, W_{1n}, W_{1p}) = g_{ds_{1n}}(IC_{1n}, W_{1n}) + g_{ds_{1p}}(IC_{1p}, W_{1p}), \quad (3.13b)$$

and

$$C_{gs_{eq}}(W_{1n}, W_{1p}) = C_{gs_{1n}}(W_{1n}) + C_{gs_{1p}}(W_{1p}), \quad (3.14a)$$

$$C_{gd_{eq}}(W_{1n}, W_{1p}) = C_{gd_{1n}}(W_{1n}) + C_{gd_{1p}}(W_{1p}), \quad (3.14b)$$

$$C_{bd_{eq}}(W_{1n}, W_{1p}) = C_{bd_{1n}}(W_{1n}) + C_{bd_{1p}}(W_{1p}). \quad (3.14c)$$

The load capacitance of both topologies are set, the passive components of the matching network are defined by the given frequency of operation and the size of the transistors. Thus, considering equation (3.11) and equation (3.12), the remaining degree of freedom in the proposed LNAs are the gate width of the transistors and the bias of M_{1n} and M_{1p} . They are listed in table 3.2 and the characteristics of the LNAs will be further illustrated and discussed according to these design variables.

TABLE 3.2: Design variables of the cascode and current reuse.

Cascode	Current reuse
W_1	W_{1n}
W_2	W_{1p}
IC_1	IC_{1n}

The performances illustrated in the following subsections are plotted versus IC for a given set of transistors' gate width. They are useful to validate the equations that will further be implemented in the design flow of section 3.3 but this is not how the circuit is optimized.

3.2.1 Input impedance

The small-signal schematics of the two proposed LNAs are presented in figures 3.8 and 3.10. At 2.4 GHz, the inductances present a parasitic resistance defined by,

$$R_L = L\omega/Q \quad (3.15)$$

where Q is the quality factor of the inductances. For this study, we chose typical values of ST 65 nm CMOS process: the inductances are set between 1 and 10 nH for a quality factor of 10.

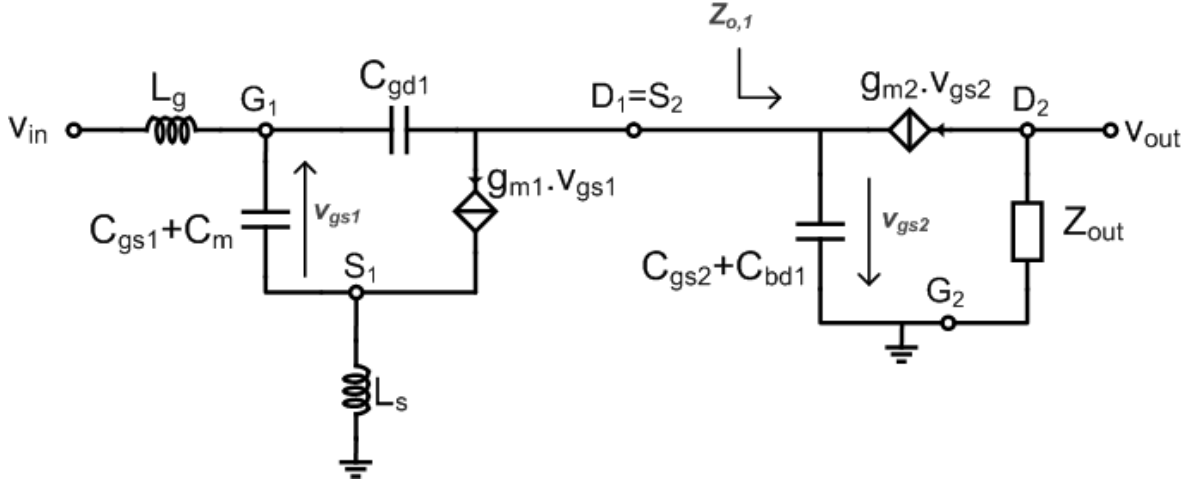


FIGURE 3.8: Small-signal schematic of the cascode topology.

In section 3.1.2, the transconductance, g_m , and the parasitic capacitances of MOS transistors are defined as functions of their size and bias. Using these functions and figure 3.8, the input impedance of the cascode, Z_{in} , can also be calculated as a function of IC_1 , W_1 and W_2 ,

$$Z_{in}(IC_1, W_1, W_2) = Z_{L_g} + A(IC_1, W_1) * \frac{Z_{gd}(W_1) + Z_{o,1}(IC_1, W_1, W_2)}{A(IC_1, W_1) + B(IC_1, W_1, W_2)}, \quad (3.16)$$

where,

$$Z_{o,1}(IC_1, W_1, W_2) = \frac{1}{sC_{bd1}(W_1) + \frac{1}{Z_{out}} + \frac{g_{m2}(IC_2, W_2)}{1 + 2g_{m2}(IC_2, W_2)Z_{out}}}, \quad (3.17)$$

$$A(IC_1, W_1) = Z_{gs}(W_1) + Z_{L_s} + g_{m1}(IC_1, W_1)Z_{gs}(W_1)Z_{L_s}, \quad (3.18)$$

$$B(IC_1, W_1, W_2) = Z_{gd}(W_1) + Z_{o,1}(IC_1, W_1, W_2) + g_{m1}(IC_1, W_1)Z_{gd}(W_1)Z_{o,1}(IC_1, W_1, W_2). \quad (3.19)$$

The details of this calculation are presented in appendix C. Then, the input reflection coefficient, S_{11} , is derived using the following equation,

$$S_{11}(IC_1, W_1, W_2) = \left| \frac{Z_{in}(IC_1, W_1, W_2) - R_S}{Z_{in}(IC_1, W_1, W_2) + R_S} \right|, \quad (3.20)$$

where R_S is the source resistance, typically 50Ω .

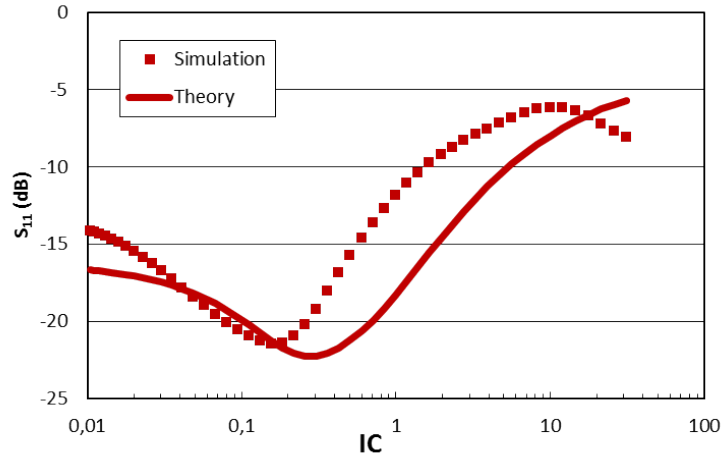


FIGURE 3.9: Analytical and simulated S_{11} versus IC_1 for the cascode in 65 nm with $W_1 = 60 \mu\text{m}$ and $W_2 = 60 \mu\text{m}$ at 2.4 GHz.

The evolution of the S_{11} with IC_1 for the cascode is plotted in figure 3.9. The peak of S_{11} is at the beginning of the MI region and the circuit is matched from the WI region to the MI region. The analytical S_{11} is slightly better than the simulated S_{11} due to parasitics which are not taken into account in the theoretical formula.

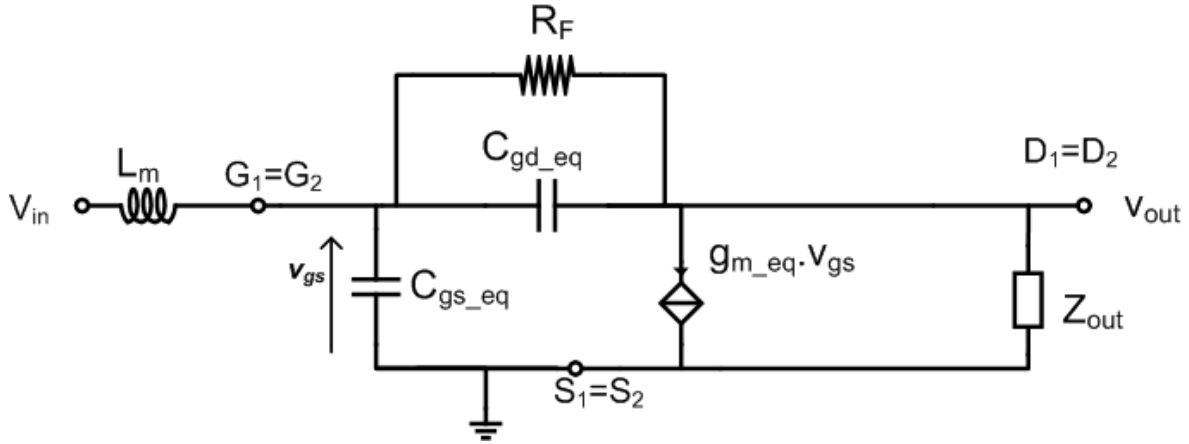


FIGURE 3.10: Small-signal schematic of the current reuse topology.

Similarly, the input impedance of the current reuse is given by,

$$Z_{in}(IC_{1n}, W_{1n}, W_{1p}) = sL_m + r_{L_m} + Z_{LNA}(IC_{1n}, W_{1n}, W_{1p}), \quad (3.21)$$

where,

$$Z_{LNA}(IC_{1n}, W_{1n}, W_{1p}) = \frac{1}{C_{gs_{eq}}(W_{1n}, W_{1p}) + A(IC_{1n}, W_{1n}, W_{1p}) * Y_{eq}(W_{1n}, W_{1p})}, \quad (3.22)$$

and

$$A = \frac{1 + g_{m_{eq}}(IC_{1n}, W_{1n}, W_{1p}) * Z_{out}(IC_{1n}, W_{1n}, W_{1p})}{1 + Y_{eq}(W_{1n}, W_{1p}) * Z_{out}(IC_{1n}, W_{1n}, W_{1p})}, \quad (3.23a)$$

$$Y_{eq}(W_{1n}, W_{1p}) = \frac{1}{R_F} + sC_{gd_{eq}}(W_{1n}, W_{1p}), \quad (3.23b)$$

$$Z_{out}(IC_{1n}, W_{1n}, W_{1p}) = \frac{1}{C_L + C_{bd_{eq}}(W_{1n}, W_{1p}) + C_{ds_{eq}}(W_{1n}, W_{1p}) + g_{ds_{eq}}(IC_{1n}, W_{1n}, W_{1p})}. \quad (3.23c)$$

The details of this calculation are presented in appendix D. The evolution of S_{11} versus IC_{1n} and IC_{1p} is plotted in figure 3.11. The theoretical S_{11} fits well with the simulated one, they both follow the same trend and peak at the same IC . The circuit achieves a low return loss ($S_{11} < -10$ dB) when biased in MI region or SI region with a minimum at $IC_{1n} = 10$.

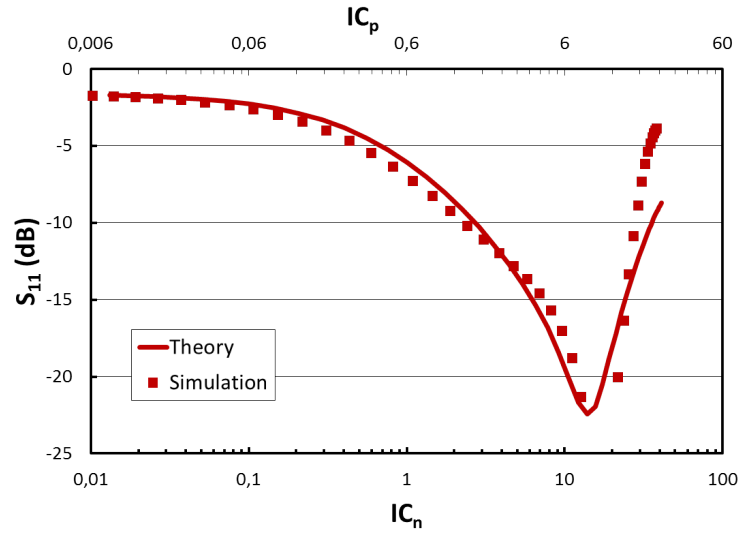


FIGURE 3.11: Analytical and simulated S_{11} versus IC_{1n} and IC_{1p} for the current reuse in 65 nm with $W_{1n} = 20 \mu\text{m}$ and $W_{1p} = 100 \mu\text{m}$ at 2.4 GHz.

For both circuits, the analytical S_{11} fits with the simulation results and the minimum of S_{11} for a given set of transistors gate width is reached in the MI region for the cascode and in the SI region for the current reuse.

3.2.2 Voltage gain and bandwidth

Just as for the input impedance, the voltage gain of the cascode is defined as a function of the size and bias:

$$A_v(IC_1, W_1, W_2) = \frac{sC_{gd_1}(W_1) - g_{m_1}(IC_1, W_1)}{sC_{gd_1}(W_1) + \frac{1}{Z_{o,1}}(IC_1, W_1, W_2) + g_{ds_1}(IC_1, W_1)}, \quad (3.24)$$

where $Z_{o,1}$ is defined in the previous subsection.

The evolution of A_v with IC_1 is plotted in figure 3.12. The maximum of gain is reached at the limit between the MI and SI regions. For $IC_1 \approx 10$, $A_v = 20$ dB.

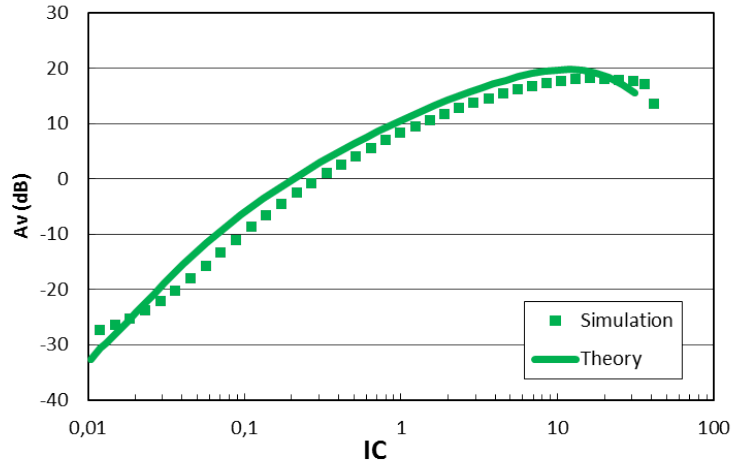


FIGURE 3.12: Analytical and simulated A_v versus IC for the cascode in 65 nm with $W_1 = 60 \mu\text{m}$ and $W_2 = 60 \mu\text{m}$ at 2.4 GHz.

The voltage gain of the current reuse, as a function of size and bias, is given by,

$$A_v(IC_{1n}, W_{1n}, W_{1p}) = \frac{Y_{eq}(W_{1n}, W_{1p}) - g_{meq}(IC_{1n}, W_{1n}, W_{1p})}{Y_{eq}(W_{1n}, W_{1p}) + \frac{1}{Z_{out}(IC_{1n}, W_{1n}, W_{1p})}}, \quad (3.25)$$

where Y_{eq} and Z_{out} are the equivalent admittance and impedance defined in equation (3.23b) and equation (3.23c).

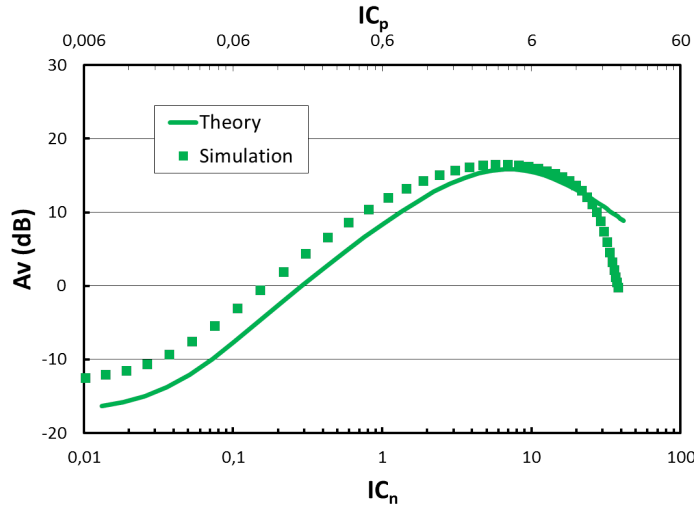


FIGURE 3.13: Analytical and simulated A_v versus IC_{1n} and IC_{1p} for the current reuse in 65 nm with $W_{1n} = 20 \mu\text{m}$ and $W_{1p} = 100 \mu\text{m}$ at 2.4 GHz.

The evolution of A_v with IC_{1n} is illustrated in figure 3.13. Theoretical and simulated results fit perfectly. Same as for the cascode, the maximum of gain is reached at the limit between the MI and SI regions; for $IC_{1n} \approx 9$, $A_v = 16$ dB. Furthermore, in the WI region, the voltage gain is also lower than 0 dB. The small offset in the WI region for both topologies

might be due to parasitic capacitances which are slightly smaller in the very weak inversion region when the drain current is lower than a few micro amperes.

The bandwidth at -3 dB, BW_{-3dB} , of the LNAs can be deduced from the voltage gain formula,

$$A_v(BW_{-3dB}) = \max(A_v) - 3dB. \quad (3.26)$$

The BW_{-3dB} is not used for the low-power application targeted in this chapter but will be necessary for the wideband application of the next chapter.

3.2.3 Noise figure

The small-signal schematic including noise sources are presented in figures 3.14 and 3.16. The noise sources are generated by the parasitic resistances of the inductances and transistors and by the drain current (section 3.1.2).

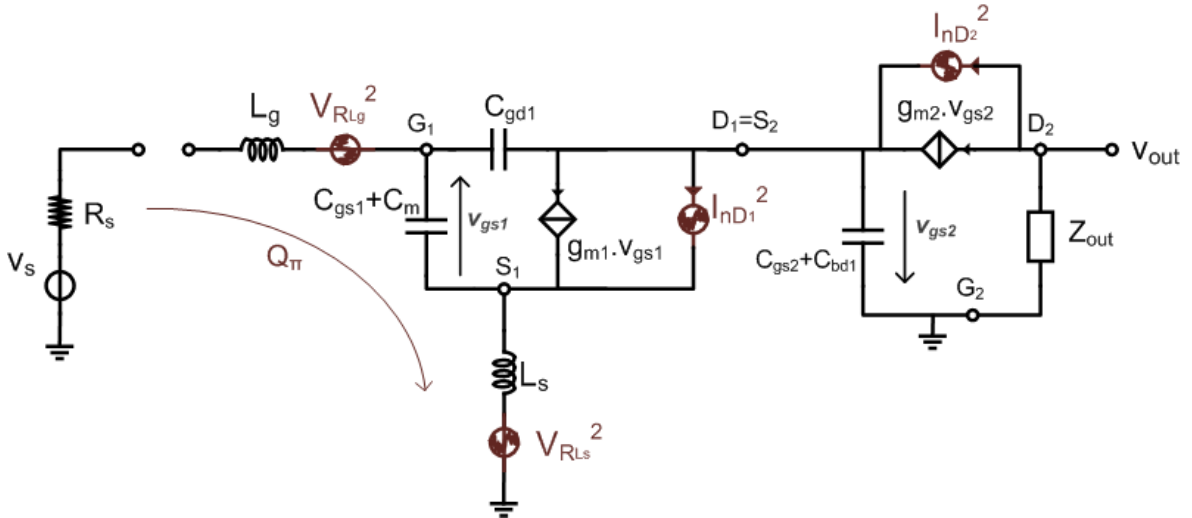


FIGURE 3.14: Small-signal schematic of the cascode topology including noise sources.

The noise figure of the cascode is given by,

$$NF(IC_1, W_1, W_2) = 1 + \frac{R_G + R_{Lg}}{R_S} + \frac{\gamma_n(IC_1)}{R_S * Q_\pi^2(IC_1, W_1, W_2) * g_{m_{eq}}^2(IC_1, W_1, W_2)}, \quad (3.27)$$

where Q_π is the passive voltage amplification performed by the input matching network. It is defined by,

$$Q_\pi(IC_1, W_1, W_2) = \frac{v_{gs1}}{v_{source}} = \frac{C(IC_1, W_1, W_2)}{Z_{in}(IC_1, W_1, W_2)(Z_{gs} + D(IC_1, W_1, W_2))}, \quad (3.28)$$

where

$$C(IC_1, W_1, W_2) = 1 + \frac{Z_{Ls}}{Z_{gd} + Z_{out}(IC_1, W_1, W_2) - Z_{Ls}}, \quad (3.29a)$$

$$D(IC_1, W_1, W_2) = \frac{1 + Z_{out}g_{m2}(IC_1, W_1, W_2) - Z_{Ls}g_{m1}(IC_1, W_1)}{Z_{gd} + Z_{out} - Z_{Ls}}. \quad (3.29b)$$

All the details of these formulas are given in appendix C. The noise figure versus IC_1 is plotted in figure 3.15. The minimum of NF , 2.4 dB, is reached at the limit between the MI and SI regions although it is almost constant in moderate and strong inversion. The theory fits with the simulation results in the MI and SI regions whereas a slight discrepancy is observed in the WI region. It comes from the model of parasitic capacitances which is different at a low level of channel inversion (WI). Beside, the amplifier does not achieve any voltage gain nor low NF in this region of operation. As consequence the circuit will be not further exploited in the WI region.

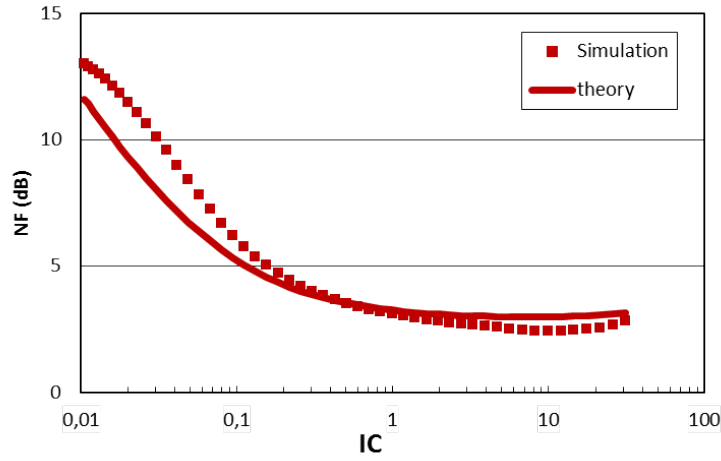


FIGURE 3.15: Analytical and simulated NF versus IC_1 for the cascode in 65 nm with $W_1 = 60 \mu\text{m}$ and $W_2 = 60 \mu\text{m}$ at 2.4 GHz.

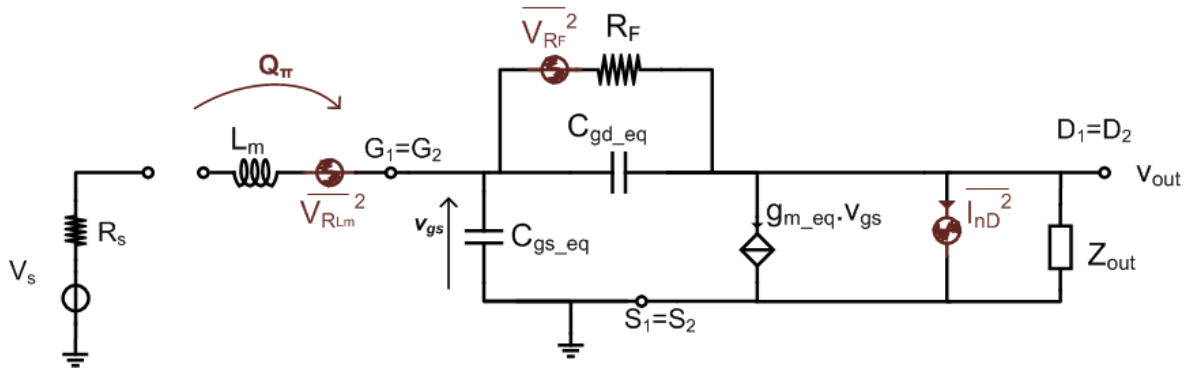


FIGURE 3.16: Small-signal schematic of the current reuse topology including noise sources.

Similarly, the NF of the current reuse is given as a function of size and bias,

$$NF(IC_{1n}, W_{1n}, W_{1p}) = 1 + \frac{\frac{1}{R_f} + g_{ds_{eq}}(IC_{1n}, W_{1n}, W_{1p}) * \gamma_n(IC_{1n}) + (R_G + r_{L_m}) * g_{m_{eq}}^2(IC_{1n}, W_{1n}, W_{1p})}{R_S * Q_\pi^2(IC_{1n}, W_{1n}, W_{1p}) * g_{m_{eq}}^2(IC_{1n}, W_{1n}, W_{1p})}, \quad (3.30)$$

where,

$$Q_\pi(IC_{1n}, W_{1n}, W_{1p}) = \frac{1}{2} * \frac{Z_{in}(IC_{1n}, W_{1n}, W_{1p})}{Z_{in}(IC_{1n}, W_{1n}, W_{1p}) + sL_m + r_{L_m}}. \quad (3.31)$$

The noise figure versus IC_{1n} and IC_{1p} is illustrated in figure 3.17. Simulation results fit well with the analytic model (equation (3.30)) from the middle of the WI to the middle of the SI region offering a wide range of bias tuning. An overestimation of the analytic model arises at the boundaries of the IC scale. At the beginning of the WI it comes from the model of the parasitic capacitances, at the end of the WI region it is due to the short channel effect modelling. Just as for the cascode, the LNA based on the current reuse configuration will not be exploited in these regions of operation. We note that the minimum of NF is reached for $IC_{1n} \approx 10$ where $NF = 1.5$ dB.

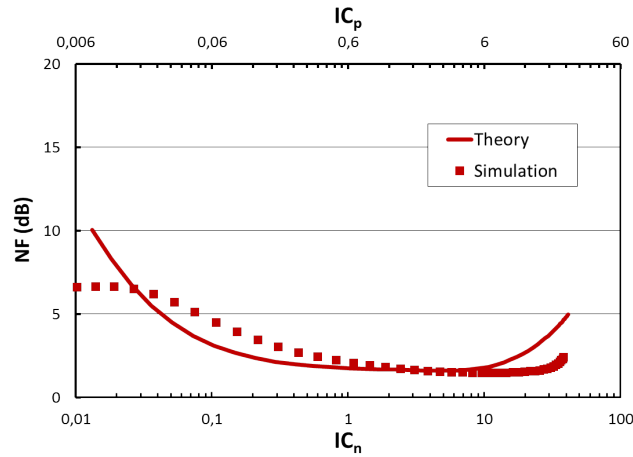


FIGURE 3.17: Analytical and simulated NF versus IC_{1n} and IC_{1p} for the current reuse in 65 nm with $W_{1n} = 20 \mu\text{m}$ and $W_{1p} = 100 \mu\text{m}$ at 2.4 GHz.

The LNA's performances are described in this section using the EKV model and the IC . The analytic expressions are compared with the simulation results of the current reuse and the cascode implemented in a 65 nm CMOS process. Despite a small offset in the WI region, the evolution of the simulated performance is close to the analytical predictions. Furthermore, these results figure out that the optimum gain, NF and input matching do not occur in the same regions of inversion nor for the same transistor sizes. As a consequence the sizing of the LNA is a trade-off for a given set of specifications. In order to explore the design space and work out the right trade-off, the next section describes a design methodology based on the aforementioned LNAs equations.

3.3 Design flow

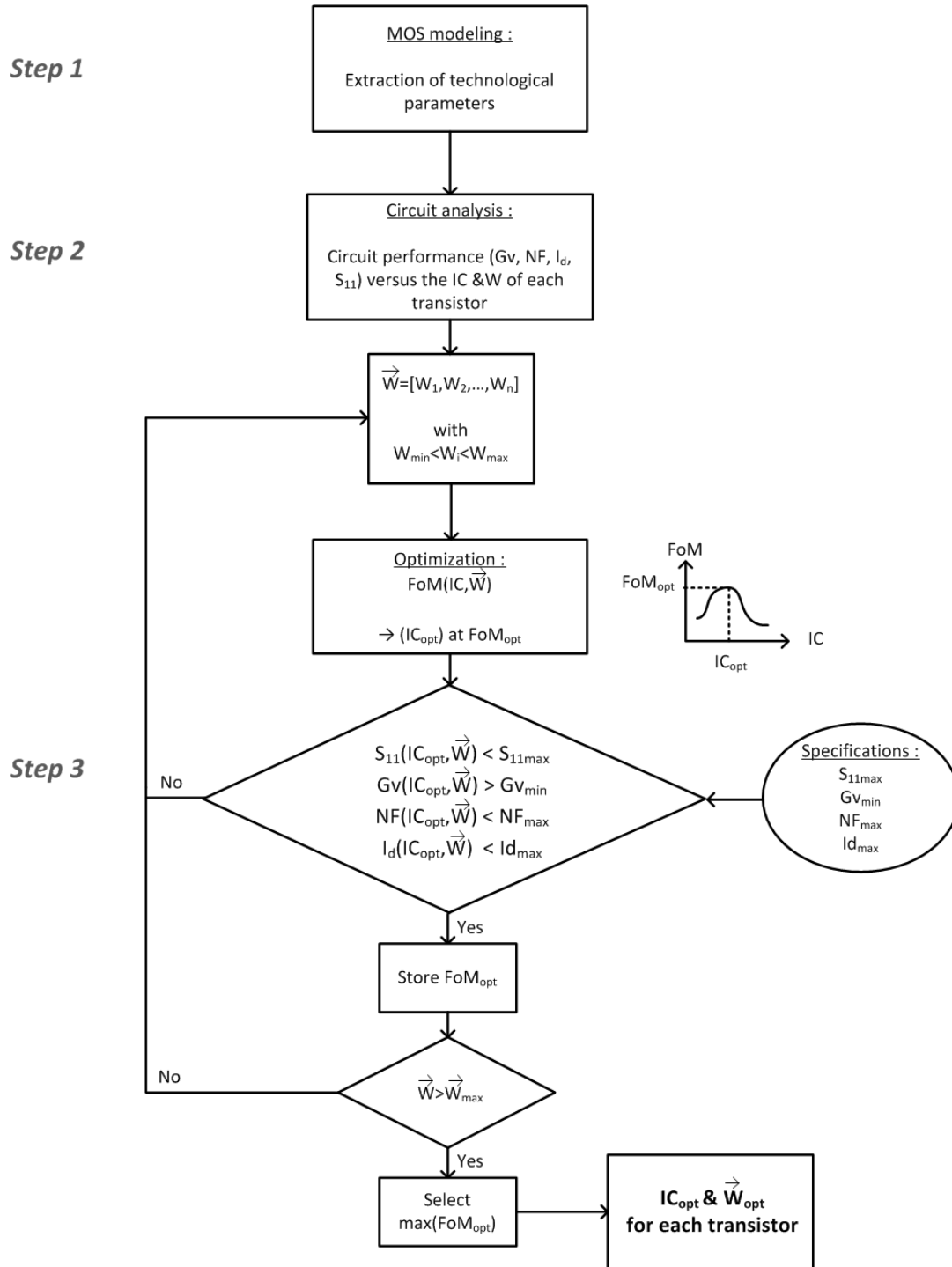


FIGURE 3.18: Flow chart of the design methodology.

The design methodology based on the IC is proposed in figure 3.18. Steps 1 and 2 are described in section 3.1 and section 3.2, respectively. The third step, embedding recursive loops, is detailed in this section. The flow chart is further applied to the sizing of the LNA in 65 nm CMOS process for a low power application at 2.4 GHz.

To work out the right trade-off among various sets of transistors' size which satisfy the targeted specifications, a figure of merit, FoM , is defined by,

$$FoM(IC, \vec{W}) = \frac{freq * A_v(IC, \vec{W})}{I_D |F_{total}(IC, \vec{W}) - 1|}, \quad (3.32)$$

where the frequency is expressed in GHz, the gain and noise are expressed in linear units and the current consumption is in mA. It combines the most relevant characteristics of a LNA, i.e. voltage gain, bandwidth, noise figure and current consumption. Linearity is investigated separately due to its large signal nature (section 4.2.4).

During step 3, the flow chart covers the design space defined by the designer and selects the most relevant sets of parameters with the specified FoM as follows:

- For a given combination of the transistors' size, $\vec{W}$, the FoM is calculated as mentioned above in order to find the optimum IC , IC_{opt} , for which the FoM is maximum.
- The LNA's performances are subsequently calculated using the optimum IC and $\vec{W}$. If the set of specifications (S_{11max} , G_{vmin} , NF_{max} , I_{max}) are reached by the calculations, the current $FoM_{opt}(IC_{opt}, \vec{W})$ is stored.
- Each combination of transistors' width is tested. Then the FoM maximum is selected among the stored FoM_{opt} . The corresponding size and bias of each transistor (IC_{opt} and $\vec{W}_{opt}$) will ensure that the circuit is optimized and addresses the specifications.

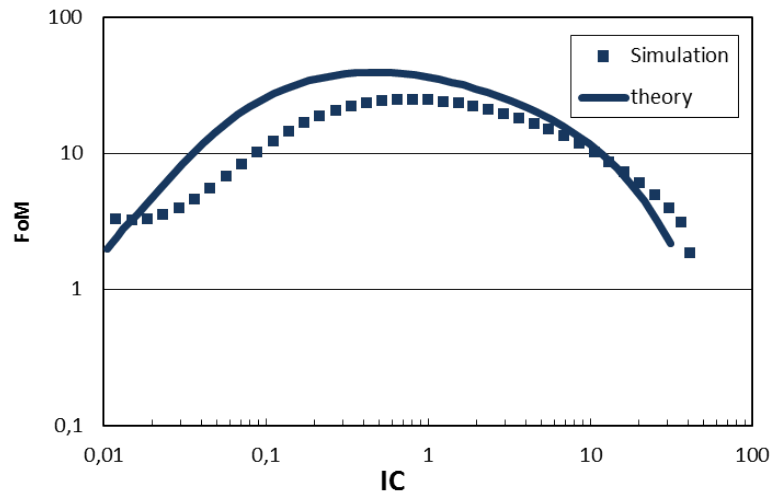


FIGURE 3.19: Analytical and simulated FoM versus IC_1 for the cascode in 65 nm with $W_1 = 60 \mu m$ and $W_2 = 60 \mu m$ at 2.4 GHz.

The FoM extracted from the flow chart of figure 3.18 and the simulation results are reported in figure 3.20 and figure 3.19 for a set of transistors' width. In good agreement with analytic calculations, the simulated FoM peaks around 30 for both circuit in the MI region, with IC_{1n} close to 1 (current reuse) and IC_1 close to 0.5 (cascode). In the WI region, the analytical model is not as accurate as in the other regions for the current reuse due to the difference in the noise figure (section 3.2.3). However this is not a problem for this methodology since the theoretical and simulated optimum points are located in the MI region.

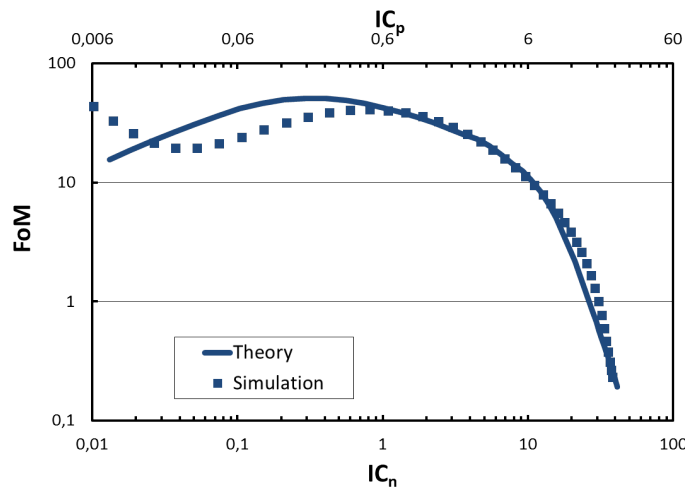


FIGURE 3.20: Analytical and simulated FoM versus IC_{1n} and IC_{1p} for the current reuse in 65 nm with $W_{1n} = 20 \mu\text{m}$ and $W_{1p} = 100 \mu\text{m}$.

For a low power application the specifications and the results of both circuits are listed in table 3.3. The cascode and current reuse have been designed in 65 nm CMOS process.

TABLE 3.3: Performances of the cascode and current reuse for a low power application.

Parameters	Specifications	Cascode	Current reuse
IC_{opt}	N.A.	3.6	4.2
I_D (mA)	< 1.5	0.8	0.9
BW (GHz)	2.4	2.4	2.4
G_v (dB)	> 15	15.2	15.1
NF (dB)	< 7	2.5	1.8
Q_π	N.A.	8.1	4.5
FoM	Max.	20	31

For both topologies the optimum IC is in the MI region and the performance are similar. In order to reach a voltage gain of 15 dB, the current reuse needs to consume 0.9 mA and the cascode consumes 0.8 mA. However, accounting for the passive voltage gain of the input matching network, Q_π , the cascode reaches a higher gain than the current reuse topology for a given current consumption. Interestingly, the current reuse is better in term of NF : 1.8 dB instead of 2.5 dB although the current consumption is ten percent lower. This is mainly due to the noisier input matching network of cascode embedding two inductors for inductive degeneration whereas the capacitive divider approach exploited in the current reuse configuration only requires a single inductor. Finally, the FoM of the current reuse is higher than the FoM of the cascode. Considering the FoM , the current reuse is better suited than the cascode for the proposed set of specification and technology. However, if the main constraint is on the current consumption and the chip area is not limited, then the cascode

along with its matching network enables a lower consumption for the same voltage gain at the cost of three inductances instead of only one in the current reuse.

Conclusion

The design methodology reported in this chapter offers interesting opportunities for the design of RF circuits. On one hand, it enables a simple and accurate approach to optimize the circuit. On the other hand, it is a very efficient tool for technology and topology comparison. The first step of this methodology is based on the EKV model and requires the extraction of technological key parameters such as $I_{spec\Box}$ and λ_c . These parameters can be exploited to discuss the skills of a CMOS process for the implementation of analog/RF circuits. The second step is the analysis of the circuit and the derivation of its performance. Any topologies can be described with the IC and thus, the performances of different topologies, optimized for a given set of specification, can be compared. Finally the third step consists of sizing the circuit in order to address a set of specifications. This design flow can be applied to address any scenarios: to illustrate it the two LNA topologies are compared to address a 2.4 GHz low power application. Designed in a 65 nm CMOS process, the performance of the circuits are discussed. In the next chapter, the design methodology will be applied to the implementation of inductorless LNAs for two different cases of applications in different technology nodes.

Chapter 4

Design of an inductorless LNA with the *IC*-based methodology

The development of multi-standard receivers leads to the need for low-power, low-area and wideband LNAs. Currently, emerging solutions to answer this need are the inductorless LNAs. Indeed, they enable a significant decrease of footprint since integrated inductors are significantly larger than the other components. Furthermore, these LNAs should present a high linearity in the context of multi-standard applications. In this chapter, a highly linear inductorless LNA is sized with the *IC*-based design methodology proposed in chapter 3. Two different sets of specifications are considered in the sizing: a wideband response for multi-standard operations, and an ultra low power case for 2.4 GHz bands. For these two scenarios of applications, three CMOS technology nodes are compared: 28 nm FDSOI, 65 nm and 130 nm. The *IC*-based methodology enables a fair comparison between these nodes in order to choose the best suited one for a specific application.

In the first section of this chapter, the different topologies of inductorless LNAs are described through the examples of state of the art LNAs. Then, the EKV model is exploited to describe the proposed inductorless LNA's performances and the analytic derivation is compared to the measurement results of this LNA in 28 nm CMOS FDSOI. Finally, it is sized and optimized using the design flow of the previous chapter for the two different set of specifications with the three nodes mentioned above and the results are compared to state of the art LNAs.

4.1 Inductorless LNA - State of the art

Inductorless LNAs are expected to achieve a high gain, a high linearity and a low noise figure over a wide bandwidth. These performances are usually traded-off with the power consumption which is critical for the concerned applications. Inductorless LNAs can be classified according to two categories: common-gate (CG) topologies as illustrated in figure 4.1a and common-source (CS) topologies as illustrated in figure 4.1b. Each one of these two categories achieves some of the expected performances while being limited for the other performances. Indeed, the first category is often combined with noise cancellation and/or g_m -boosting techniques because of its high NF. The second one, on the other hand, is combined with resistive or active feedback to perform wideband operation [39].

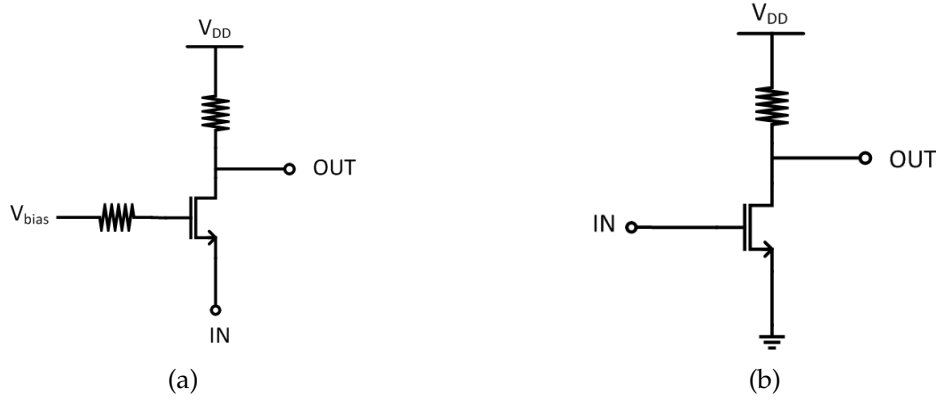


FIGURE 4.1: (a) Common-gate and (b) common-source amplifiers.

This section described these two categories with state of the art examples and introduces the proposed shunt-shunt feedback current reuse LNA.

4.1.1 Common-gate topologies

The LNAs based on CG topologies offer many advantages such as an inherent wide-band input matching and a high linearity for a moderate power consumption. However, the NF and the gain are limited by the transconductance of the amplifier [40]. Indeed, the latter is set by the input matching conditions since the input impedance of a common gate LNA is given by,

$$Z_{in} = \frac{1}{g_m}. \quad (4.1)$$

According to the previous equation, to be matched to a 50Ω impedance, the transconductance of a CG LNA must be set to 20 mS which leaves no degree of freedom for the optimization of the gain and the NF . Multiple solutions to overcome this limitation can be used such as capacitive cross-coupling as presented in [40, 41, 42] and g_m -boost amplifier as presented in [43, 44].

Cross-coupled common-gate

In [40], the authors propose a CG LNA including capacitive cross-coupling to reduce the NF and to improve the voltage gain. The topology is presented in figure 4.2a. The differential input signal is connected to the sources of the transistors M_1 and M_2 and they are cross-coupled by capacitors C_1 and C_2 through their gates and sources. The NF of the LNA can be reduced with a moderate impact on the input matching conditions. Furthermore, the linearity is improved by auxiliary transistors which cancel out the third order term of transconductance response.

In [41], the authors combine a fully differential CG LNA with multiple feedback paths in order to add several degrees of freedom for the LNA's transconductance as illustrated in figure 4.2b. They use a capacitive cross-coupling by introducing capacitances C_1 and C_2 to

reduce the noise as mentioned above. Furthermore, they add a positive feedback with M_2 transistors in order to enhance the gain.

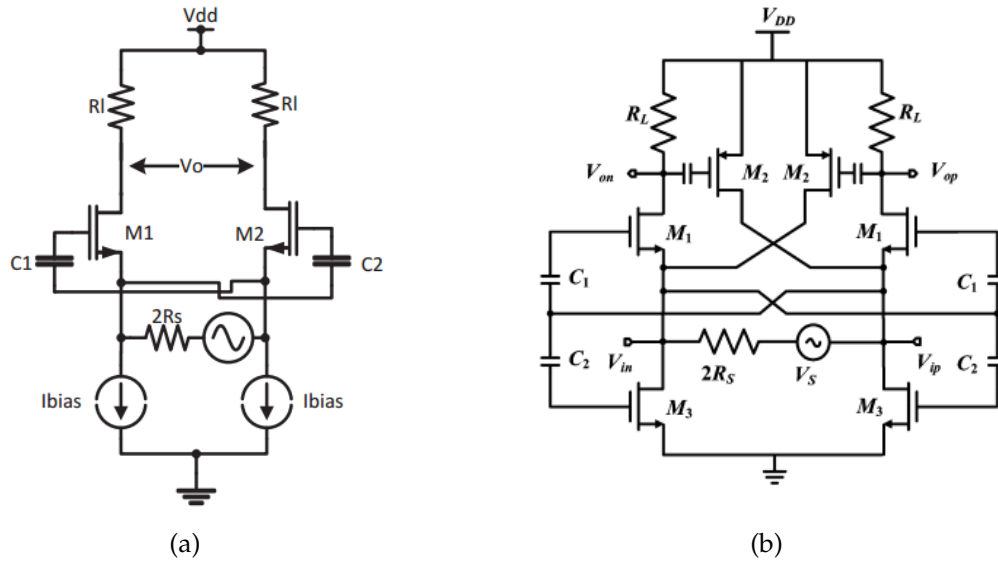


FIGURE 4.2: Capacitive cross-coupled CG LNAs (a) [40] and (b) [41].

g_m -boost amplifier

In [43], the authors have implemented a differential CG LNA with a g_m -boost amplifier as illustrated in figure 4.3. The main amplifier consists of M_1 and R_1 , the g_m -boost amplifier consists of M_3 and R_3 . The main amplifier includes a capacitive cross-coupling (CCC) as discussed above. However, the latter does not improve the trade-off between power consumption and matching since CCC is based on passive amplification. To address this purpose, a g_m -boost amplifier, in addition to CCC, allows for gain enhancement and reduced the NF with a moderate increase of the power consumption.

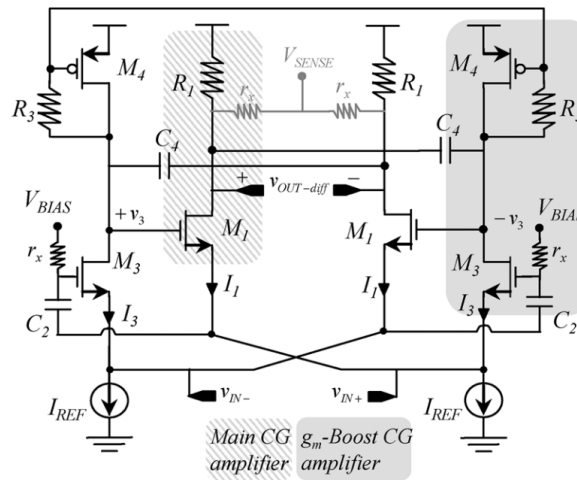


FIGURE 4.3: CG LNA with g_m enhancement.

Source: [43]

The LNAs presented in this section are capable of achieving adequate performances at the cost of complex and sensitive architecture to compensate for the high NF . Beside, they require a special care in the design of the antenna and the RF filter which makes the combination of the LNA and the antenna sensitive to mismatching [45].

4.1.2 Common-source topologies

The other category of inductorless LNAs gathers the active and resistive shunt feedback amplifiers [46, 47, 48]. Simple CS topology provides a high gain and a low NF but consumes too much power and presents a limited bandwidth.

Resistive shunt feedback

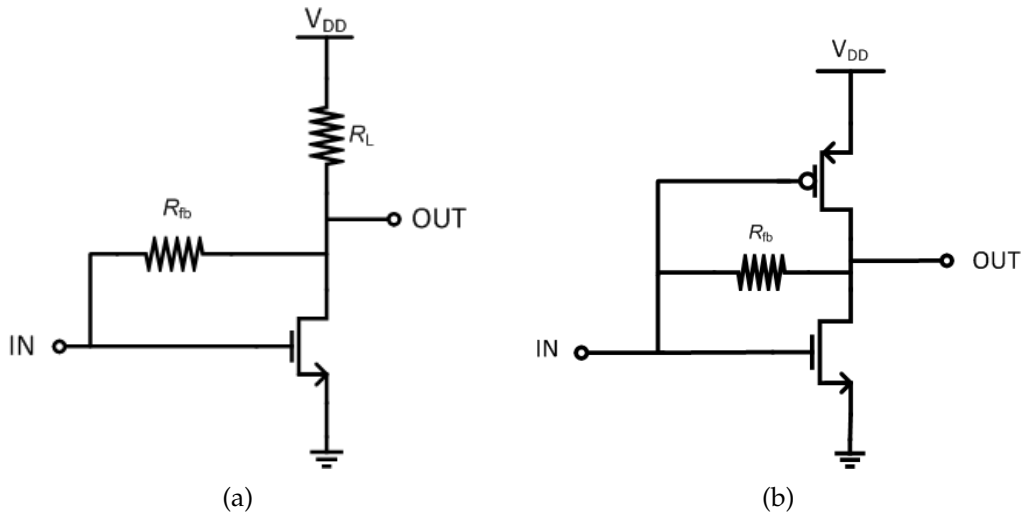


FIGURE 4.4: (a) Resistive shunt-feedback LNA and (b) current reuse configuration.

In a resistive shunt-feedback amplifier as illustrated in figure 4.4a, the gain is given by,

$$A_v = -g_m R_{out}, \quad (4.2)$$

where $R_{out} = R_{fb} // R_L$, R_{fb} is the feedback resistance and R_L is the load resistance. Thus, the design of a resistive shunt feedback LNA, must find a first trade-off between A_v and V_{DD} . Indeed, at a constant drain current, to increase the gain, R_L should be set to high values leading to an increase of the supply voltage. However, this can be significantly reduced by adding a PMOS transistors in parallel with the CS transistor as illustrated in figure 4.4b, resulting in a higher transconductance,

$$g_{m_{c-r}} = g_{m_{NMOS}} + g_{m_{PMOS}} - \frac{1}{R_{fb}}. \quad (4.3)$$

Thus, for a constant drain current, the voltage gain is significantly increased and depends on R_{fb} which can be set to a high value. This structure is a current-reuse configuration, it is very efficient to reduce the overall power while improving current efficiency [49].

In [46], the authors propose a resistive shunt feedback CS amplifier combined with a noise cancelling stage which is presented in figure 4.5. The resistor $R_{F1,A}$ enables wideband matching, $M_{2,A}$ and $M_{3,A}$ compensate for the noise of $M_{1,A}$. However, this LNA consumes 13 mW for a low gain which is not suited for a low power application.

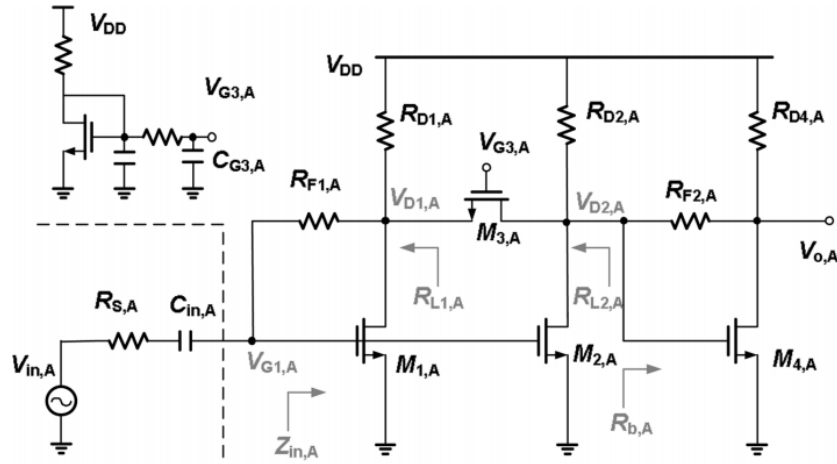


FIGURE 4.5: Resistive shunt-feedback LNA.
Source: [46]

Active shunt feedback

Another solution is to place an active shunt feedback instead of a resistive path only. In [47], the authors propose such kind of circuit combined with noise cancelling stage as illustrated in figure 4.6. The LNAs mentioned above, are often limited in term of linearity. Here, the authors implement a distortion cancellation technique. Indeed, second and third order distortion are cancelled by biasing two transistors in parallel in different regions of inversion. This LNA achieves a good trade-off between all of the performances but at the cost of a high power consumption of 30 mW.

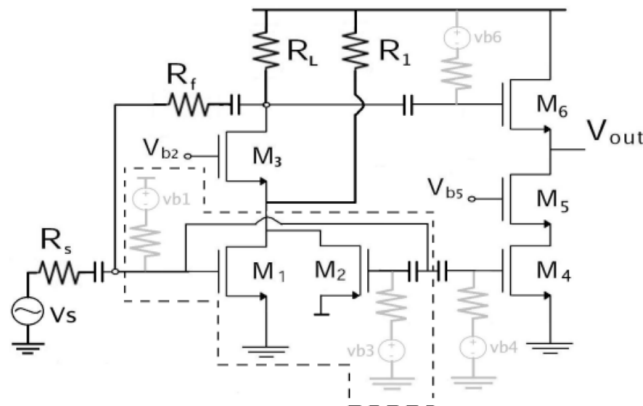


FIGURE 4.6: Active shunt-feedback CS and noise cancelling stage.
Source: [47]

A lot of circuit techniques have been developed to achieve a low NF and a high voltage gain in inductorless amplifier architectures. However the linearity which becomes critical in the implementation of wideband receivers is often a limiting characteristic of these LNAs. This purpose is addressed in the next subsection.

In the previous subsections, common topologies of inductorless LNAs are presented. CG topologies show good input matching at the cost of a limited NF and therefore requires noise cancellation and/or g_m -boosting techniques. On the other hand, CS topologies with resistive feedback exhibit high NF at high frequencies and therefore are not suited for wideband applications nor for low power applications because of the trade-off between high gain and low voltage. The latter can be fixed with a current-reuse structure but it does not presents a wideband matching. Finally, the last category is the active shunt feedback amplifier which shows good trade-off between all the performances although it is not linear enough and still consumes a large power.

In [53], a shunt-shunt feedback LNA is proposed as illustrated in figure 4.8. It features a CS cascode amplifier with an active feedback stage. This topology offers wideband matching, high gain and low NF but the CS amplifier, along with its feedback path, exhibits a degraded linearity.

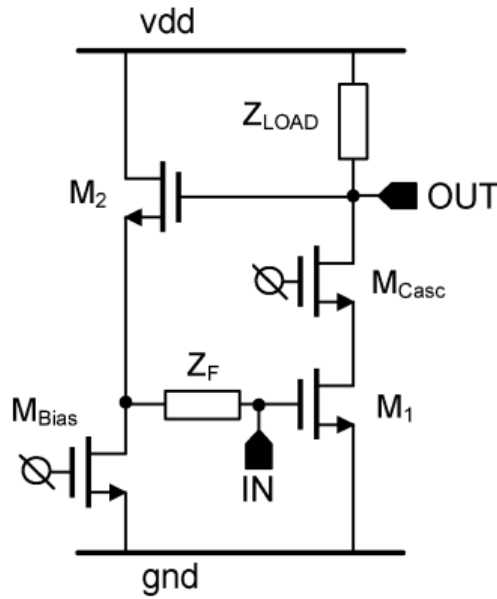


FIGURE 4.8: Shunt-shunt feedback cascode amplifier.

Source: [53]

A similar topology that combines a current-reuse structure, instead of a cascode, with a source follower active feedback is proposed in [54] and illustrated in figure 4.9. This LNA benefits from all the advantages of these topologies and still presents very high linearity thanks to R_{fb} (see section 4.2.4) in combination with the source follower transistor M_2 which also performs the shunt feedback.

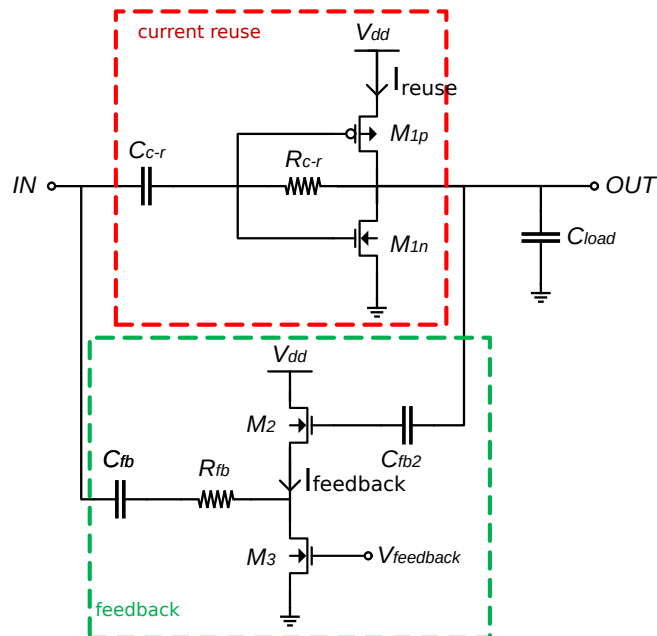


FIGURE 4.9: Topology of the shunt feedback current reuse LNA.

Thus, we chose to applied the *IC*-based methodology to this LNA in order to optimize it and to compare its results in 130 nm [54] and in 28 nm FDSOI [this work] to the state of the art LNAs.

4.2 Circuit analysis

The LNA topology explored in this work is presented in figure 4.9. The circuit analysis, which is summarized in this section, is fully detailed in [54]. This LNA is based on a current reuse stage and a source follower acting as a shunt feedback. To derive the analytic expressions of the LNA, an equivalent model is proposed in figure 4.10. It features a back to back configuration with a forward operational transconductance amplifier (OTA) represented by g_{meq} and a feedback path represented by g_{m2} .

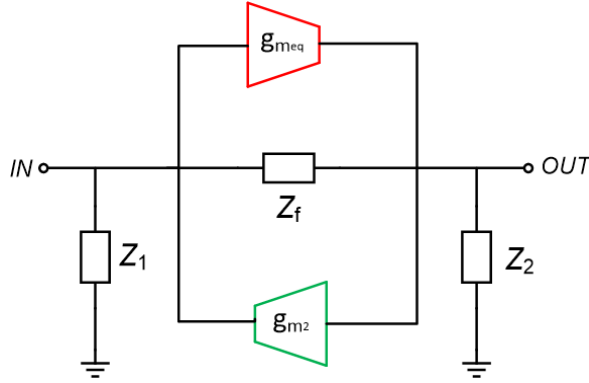


FIGURE 4.10: Equivalent model of the proposed LNA.

The three impedances Z_1 , Z_2 and Z_f account for passive devices and parasitics located at the input, output and within the feedback path, respectively. They are derived in equation (4.4).

$$Z_1(W_{1n}, W_{1p}, W_2) = \frac{1}{\frac{1}{R_{c-r}} + j\omega C_{gdeq}(W_{1n}, W_{1p}) + j\omega C_{gd2}(W_2)}, \quad (4.4a)$$

$$Z_f(IC_2, W_{1n}, W_{1p}, W_2) = \frac{1}{g_{ds2}(IC_2, W_2) + j\omega \frac{C_{gse}(W_{1n}, W_{1p})C_{c-r}}{C_{gse}(W_{1n}, W_{1p}) + C_{c-r}} + \frac{1}{1/j\omega C_{bd2}(W_2) + R_{fb} + 1/j\omega C_{fb}}}, \quad (4.4b)$$

$$Z_2(IC_{1n}, W_{1n}, W_{1p}, W_2) = \frac{1}{g_{dse}(IC_{1n}, W_{1n}, W_{1p}) + j\omega \frac{C_{gd2}(W_2)C_{fb2}}{C_{gs2}(W_2) + C_{fb2}} + j\omega C_L + j\omega C_{bdeq}(W_{1n}, W_{1p})}, \quad (4.4c)$$

where,

$$g_{meq}(IC_{1n}, W_{1n}, W_{1p}) = g_{m1n}(IC_{1n}, W_{1n}) + g_{m1p}(IC_{1p}, W_{1p}), \quad (4.5a)$$

$$g_{dse}(IC_{1n}, W_{1n}, W_{1p}) = g_{ds1n}(IC_{1n}, W_{1n}) + g_{ds1p}(IC_{1p}, W_{1p}), \quad (4.5b)$$

and

$$C_{gs_{eq}}(W_{1n}, W_{1p}) = C_{gs_{1n}}(W_{1n}) + C_{gs_{1p}}(W_{1p}), \quad (4.6a)$$

$$C_{gd_{eq}}(W_{1n}, W_{1p}) = C_{gd_{1n}}(W_{1n}) + C_{gd_{1p}}(W_{1p}), \quad (4.6b)$$

$$C_{bd_{eq}}(W_{1n}, W_{1p}) = C_{bd_{1n}}(W_{1n}) + C_{bd_{1p}}(W_{1p}). \quad (4.6c)$$

The same current, I_{reuse} , flows into the PMOS, M_{1p} , and the NMOS, M_{1n} . Similarly, the current $I_{feedback}$ is the drain current of the transistors M_2 and M_3 . Assuming that the gate lengths of the transistors are set to the minimum length of the process and considering equation (3.1a), the bias conditions of (M_{1n}, M_{1p}) and (M_2, M_3) are respectively defined by,

$$IC_{1n} = IC_{1p} \frac{W_{1p} I_{spec_{\square p}}}{W_{1n} I_{spec_{\square n}}}. \quad (4.7a)$$

$$IC_3 = IC_2 \frac{W_2}{W_3}. \quad (4.7b)$$

Hence, the design variables of the LNA proposed in figure 4.9a are: the gate width of the four transistors (W_{1n} , W_{1p} , W_2 and W_3) and the bias of M_{1n} and M_2 (IC_{1n} and IC_2 respectively). Similarly to section 3.2, the characteristics of the LNA will be further illustrated and discussed according to these design parameters.

4.2.1 Input impedance

In section 3.1.2, the transconductance, g_m , and the parasitic capacitances of MOS transistors are defined as functions of their size and bias. Using these functions and equation (4.4), the input impedance, Z_{in} , can also be calculated as a function of IC_{1n} , IC_2 , W_{1n} , W_{1p} , W_2 and W_3 :

$$Z_{in}(IC_{1n}, IC_2, W_{1n}, W_{1p}, W_2) = Z_1(W_{1n}, W_{1p}, W_2) // Z_{bis}(IC_{1n}, IC_2, W_{1n}, W_{1p}, W_2) \quad (4.8)$$

where

$$Z_{bis}(IC_{1n}, IC_2, W_{1n}, W_{1p}, W_2) = \frac{Z_2(IC_{1n}, W_{1n}, W_{1p}, W_2) + Z_f(IC_2, W_{1n}, W_{1p}, W_2)}{1 + [g_{m_{eq}}(IC_{1n}, W_{1n}, W_{1p}) + g_{m_2}(IC_2, W_2) + A(IC_{1n}, IC_2, W_{1n}, W_{1p}, W_2)] \cdot Z_2(IC_{1n}, W_{1n}, W_{1p}, W_2)}, \quad (4.9a)$$

$$A(IC_{1n}, IC_2, W_{1n}, W_{1p}, W_2) = g_{m_{eq}}(IC_{1n}, W_{1n}, W_{1p}) g_{m_2}(IC_2, W_2) Z_f(IC_2, W_{1n}, W_{1p}, W_2). \quad (4.9b)$$

As in the previous chapter, the input reflection coefficient, S_{11} , is deduced,

$$S_{11}(IC_{1n}, IC_2, W_{1n}, W_{1p}, W_2, W_3) = \left| \frac{Z_{in}(IC_{1n}, IC_2, W_{1n}, W_{1p}, W_2, W_3) - R_S}{Z_{in}(IC_{1n}, IC_2, W_{1n}, W_{1p}, W_2, W_3) + R_S} \right|, \quad (4.10)$$

where R_S is the source resistance (typically 50Ω).

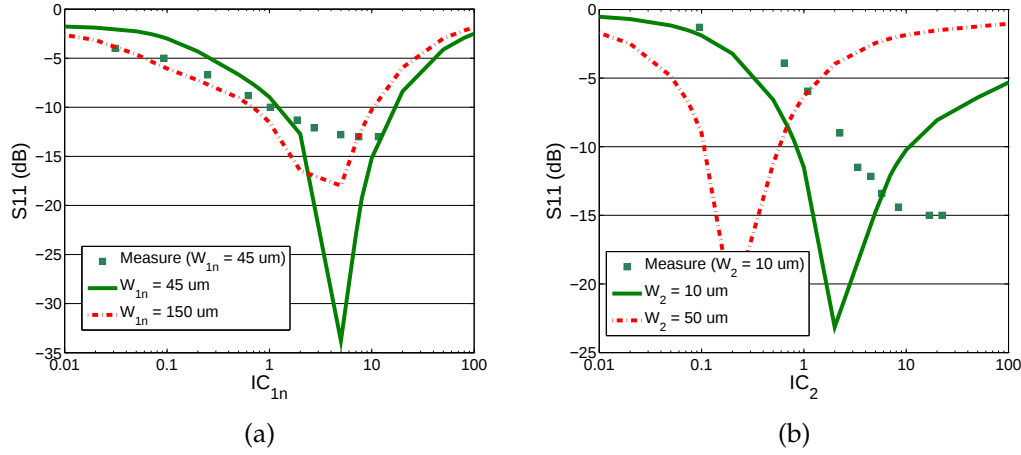


FIGURE 4.11: Analytical and measured S_{11} versus (a) IC_{1n} and W_{1n} and (b) IC_2 and W_2 , in 28 nm FDSOI at 2 GHz for $W_{1n} = 45 \mu\text{m}$, $W_{1p} = 40 \mu\text{m}$, $W_2 = 10 \mu\text{m}$ and $W_3 = 10 \mu\text{m}$.

Figure 4.11 illustrates the evolution of the input reflection coefficient S_{11} with IC_{1n} and IC_2 for different values of W_{1n} and W_2 . In order for the LNA to be matched to a source impedance, S_{11} must be lower than -10 dB. Hence, considering figure 4.11, for a given combination of the transistors' gate width, M_{1n} and M_2 should be biased in moderate inversion. The measured S_{11} of the LNA in 28 nm FDSOI fits with the analytical equation even though the local minimum is not as low as predicted. This is mainly due to the layout parasitics which are not taken into account in the analytical expression (equation (4.8)).

4.2.2 Voltage gain and bandwidth

Just as for the input impedance, the voltage gain is defined as a function of the size and bias:

$$G_v(IC_{1n}, IC_2, W_{1n}, W_{1p}, W_2) = \frac{[-g_{m_{eq}}(IC_{1n}, W_{1n}, W_{1p})Z_f(IC_2, W_{1n}, W_{1p}, W_2) + 1] Z_2(IC_{1n}, W_{1n}, W_{1p}, W_2)}{Z_f(IC_2, W_{1n}, W_{1p}, W_2) + Z_2(IC_{1n}, W_{1n}, W_{1p}, W_2)}. \quad (4.11)$$

According to this equation and assuming that $Z_f \gg Z_2$, the gain can be simplified,

$$G_v(IC_{1n}, IC_2, W_{1n}, W_{1p}, W_2) \approx -g_{m_{eq}}(IC_{1n}, W_{1n}, W_{1p})Z_2(IC_{1n}, W_{1n}, W_{1p}, W_2), \quad (4.12)$$

which is the gain of the current reuse. Therefore, the voltage gain of this LNA is set by the main amplifier and does not depends on the feedback path.

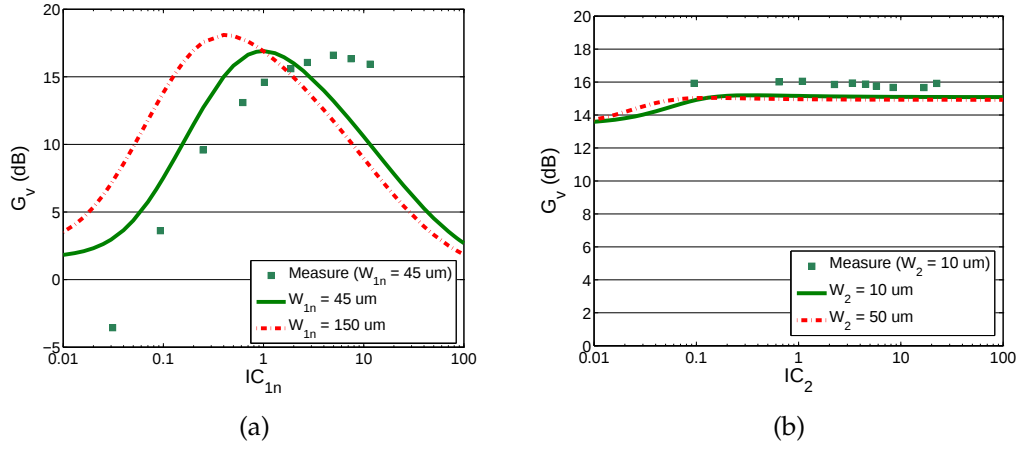


FIGURE 4.12: Analytical and measured G_v versus (a) IC_{1n} and W_{1n} and (b) IC_2 and W_2 , in 28 nm FDSOI at 2 GHz for $W_{1n} = 45 \mu\text{m}$, $W_{1p} = 40 \mu\text{m}$, $W_2 = 10 \mu\text{m}$ and $W_3 = 10 \mu\text{m}$.

In figure 4.12, the gain is plotted versus IC_{1n} and IC_2 for a set of W_{1n} or W_2 . Figure 4.12b confirms that the feedback path, through IC_2 and W_2 , has no significant impact on the gain. Therefore, the gain is only set by the design variables of the current reuse stage. M_{1n} should be large and biased in the MI region in order for the gain to be maximized as illustrated in figure 4.12a. Accordingly, the measured G_v is maximum in the MI region of M_{1n} and independent of the feedback bias IC_2 .

The -3 dB bandwidth, BW_{-3dB} , can be deduced from equation (4.11) by solving equation (4.13),

$$G_v(BW_{-3dB}) = \max(G_v) - 3dB. \quad (4.13)$$

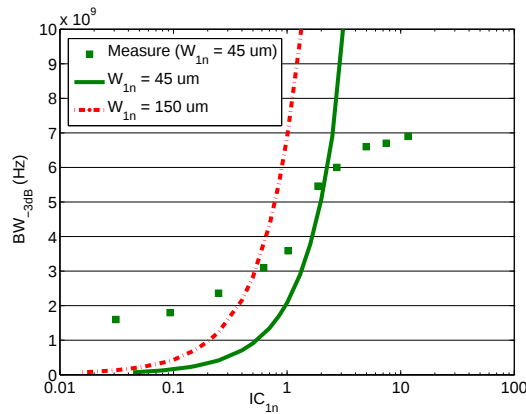


FIGURE 4.13: Analytical and measured BW_{-3dB} versus IC_{1n} and W_{1n} in 28 nm FDSOI for $W_{1p} = 40 \mu\text{m}$, $W_2 = 10 \mu\text{m}$ and $W_3 = 10 \mu\text{m}$.

In equation (4.13), BW_{-3dB} is a function of the voltage gain. Since the latter does not depend on the feedback stage, BW_{-3dB} depends only on the current reuse stage. Its evolution

with IC_{1n} for different values of W_{1n} is plotted in figure 4.13. In order for the bandwidth to be maximum, large devices should be biased at the beginning of the MI region and small devices should be biased at the end of the MI region. As expected, the measured BW_{-3dB} increases with the IC , then it saturates in the SI region due to the layout parasitics.

4.2.3 Noise figure

In [54], the overall noise figure (F_{total}) is defined as the sum of the noise figures related to each noise source : the resistances R_{fb} and R_{c-r} and the drain currents of the four transistors M_{1n} , M_{1p} , M_2 and M_3 .

$$\begin{aligned} F_{total}(IC_{1n}, IC_2, W_{1n}, W_{1p}, W_2, W_3) \\ = 1 + F_{R_{fb}}(IC_2, W_2) + F_{R_{c-r}}(IC_2, W_2) + F_{M_{1n}}(IC_{1n}, IC_2, W_{1n}, W_{1p}, W_2) \\ + F_{M_{1p}}(IC_{1n}, IC_2, W_{1n}, W_{1p}, W_2) + F_{M_2}(IC_2, W_2) + F_{M_3}(IC_2, W_2, W_3), \end{aligned} \quad (4.14)$$

where,

$$F_{R_{fb}}(IC_2, W_2) = R_s R_{fb} \left[\frac{g_{m_2}(IC_2, W_2)}{1 + g_{m_2}(IC_2, W_2) R_{fb}} \right]^2, \quad (4.15a)$$

$$F_{R_{c-r}}(IC_2, W_2) = \frac{R_s}{R_{c-r}} \frac{g_{m_2}(IC_2, W_2)}{[1 + g_{m_2}(IC_2, W_2) R_{fb}]^2}, \quad (4.15b)$$

$$\begin{aligned} F_{M_{1n}}(IC_{1n}, IC_2, W_{1n}, W_{1p}, W_2) \\ = R_s \frac{\gamma_n g_{m_{1n}}(IC_{1n}, W_{1n})}{g_{m_{eq}}(IC_{1n}, W_{1n}, W_{1p})} \left[\frac{1}{R_s} + \frac{g_{m_2}(IC_2, W_2)}{1 + g_{m_2}(IC_2, W_2) R_{fb}} \right]^2, \end{aligned} \quad (4.15c)$$

$$\begin{aligned} F_{M_{1p}}(IC_{1n}, IC_2, W_{1n}, W_{1p}, W_2) \\ = R_s \frac{\gamma_n g_{m_{1p}}(IC_{1n}, W_{1n}, W_{1p})}{g_{m_{eq}}(IC_{1n}, W_{1n}, W_{1p})} \left[\frac{1}{R_s} + \frac{g_{m_2}(IC_2, W_2)}{1 + g_{m_2}(IC_2, W_2) R_{fb}} \right]^2, \end{aligned} \quad (4.15d)$$

$$F_{M_2}(IC_2, W_2) = \gamma_n g_{m_2}(IC_2, W_2) \frac{R_s}{[1 + g_{m_2}(IC_2, W_2) R_{fb}]^2}, \quad (4.15e)$$

$$F_{M_3}(IC_2, W_2, W_3) = \gamma_n g_{m_3}(IC_2, W_2, W_3) \frac{R_s}{[1 + g_{m_2}(IC_2, W_2) R_{fb}]^2}. \quad (4.15f)$$

The NF is plotted versus IC_{1n} and IC_2 for two sets of W_{1n} or W_2 in figure 4.14. The minimum NF is reached when M_{1n} is biased at the end of the MI region and IC_2 is in the WI region (figure 4.14a), although the feedback does not really impact the NF in WI and MI (figure 4.14b). In the current reuse stage, the wider the transistors, the smaller is the NF whereas, the transistor should be small in the feedback. The measurements show a good correlation with the analytic predictions. The minimum noise is achieved in the same region and the measured noise is very close to the expected results.

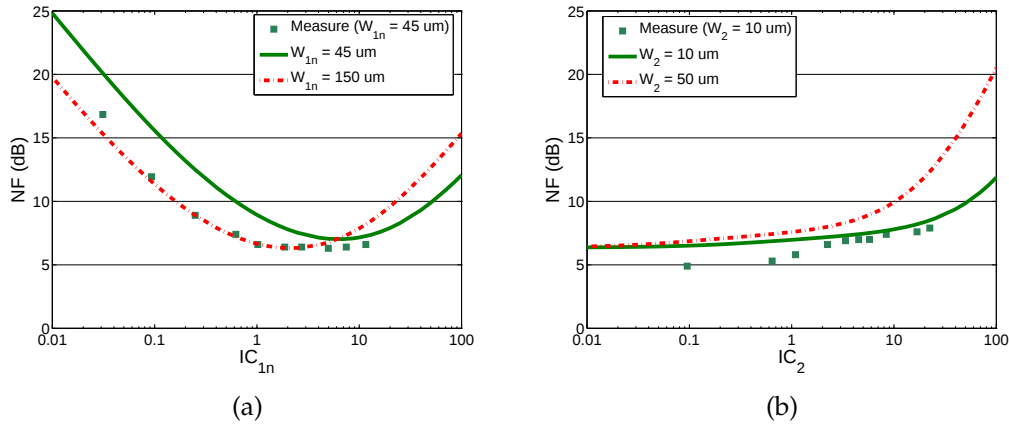


FIGURE 4.14: Analytical and measured NF versus (a) IC_{1n} and W_{1n} and (b) IC_2 and W_2 , in 28 nm FDSOI at 2 GHz for $W_{1n} = 45 \mu\text{m}$, $W_{1p} = 40 \mu\text{m}$, $W_2 = 10 \mu\text{m}$ and $W_3 = 10 \mu\text{m}$.

4.2.4 Linearity

In a receiver, the level of power collected by the antenna rarely drives the LNA to compression in theory. In practice the Tx leakage can be an issue. Still, the compression of the LNA is usually not a prime concern in its design. On the other hand, the increase in density of radio-communications contributes to desensitize the receiver due to inter-modulation produced by RF blockers. For this reason, the linearity concern of a LNA is represented by the input third order intercept point (IIP_3). The IIP_3 is a large signal performance and as such can not be easily defined as a function of IC . It can be expressed as follows [55],

$$IIP_3 = \sqrt{\frac{4}{3} \frac{A_1(j\omega_1)}{A_3(-j\omega_1, j\omega_2, j\omega_3)}}, \quad (4.16)$$

where A_1 and A_3 are the first-order and third-order Volterra kernels of the circuit, respectively [56].

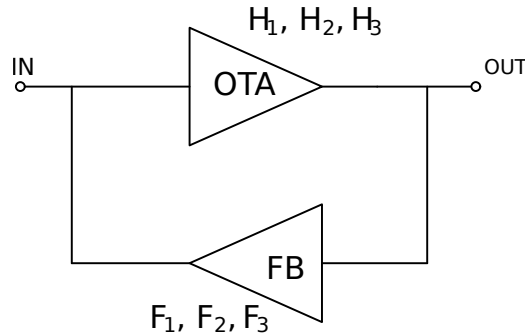


FIGURE 4.15: Equivalent model of the proposed LNA.

To investigate the inter-modulation response, we use the equivalent model of figure 4.15 for a memoryless feedback system. The transfer functions for harmonic distortions are represented by H_i for the forward path (OTA), and F_i for the feedback path. Assuming that the system is memoryless [57], equation (4.16) can be rewritten as,

$$IIP_3 = \sqrt{\frac{4}{3} \frac{H_1}{R^3 [H_3 - 2H_2^2 F_1 R + H_1^4 (2H_1 F_2^2 R - F_3) - 4H_1^2 H_2 F_2 R]}}, \quad (4.17)$$

where

$$R = (1 + H_1 F_1)^{-1}. \quad (4.18a)$$

$$H_k = \frac{1}{k!} \frac{\delta^k V_{out_{OTA}}}{\delta^k V_{in_{OTA}}}, \quad (4.18b)$$

$$F_k = \frac{1}{k!} \frac{\delta^k V_{out_{FB}}}{\delta^k V_{in_{FB}}}. \quad (4.18c)$$

Since the OTA is implemented with a current reuse configuration, $H_2 = 0$, then equation (4.17) can be simplified as,

$$IIP_3 = \sqrt{\frac{H_1}{H_3} \frac{(1 + T)^3}{1 - \frac{H_1^4}{H_3} \left(F_3 - 2 \frac{F_2^2}{F_4} \frac{T}{1+T} \right)}}, \quad (4.19)$$

where $T = H_1 F_1$. Finally, $F_1 \gg F_2$, i.e. the fundamental response of the feedback block is larger than the second harmonic response, according to [54]. The IIP_3 of the proposed LNA is given by,

$$IIP_3 = \sqrt{\frac{H_1 (1 + H_1 F_1)^3}{H_3 \left(1 - \frac{H_1^4}{H_3} F_3 \right)}}, \quad (4.20)$$

In equation (4.20), the IIP_3 is maximum when the denominator is minimized. H_1 and H_3 are the fundamental and third order responses of the current reuse stage. According to section 4.2.2, the OTA sets the gain and the BW of the LNA. Hence, tuning the IIP_3 by adjusting H_i is not a good strategy. However, the linearity can still be optimized by tuning the current in the feedback stage to adjust F_3 in equation (4.20).

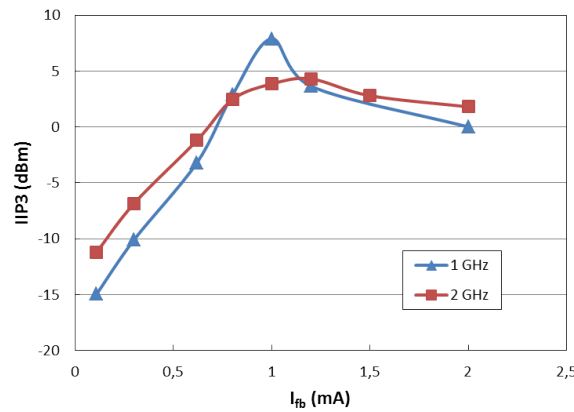


FIGURE 4.16: Measured IIP_3 versus $I_{feedback}$ at 1 GHz and 2 GHz with $\Delta f = 40$ MHz.

Figure 4.16 represents the measured IIP_3 as a function of the feedback current. As expected, it peaks for a specific value of $I_{feedback}$ around 1 mA. The linearization of the overall circuit by adjusting the feedback path is a significant asset compared to the inductorless LNA

of the state of art presented in section 4.1. Beside the range of $I_{feedback}$ for IIP_3 optimization has a minor impact on the input matching. A very high linearity, close to +8 dBm, can therefore be achieved without any specific trade-off with the other characteristics of the LNA. According to the investigations of chapter 1 the linearity is very challenging for multi-standard applications. The inherent high IIP_3 of the proposed topology makes it very suited for wideband receiver operating in a dense radio spectrum.

The LNA's performances are described in this section using the EKV model and the IC except for the linearity which is a large-signal performance. The analytic expressions are compared with the measurement results of the LNA implemented in the 28 nm FDSOI process. Despite a small offset in the absolute values, the evolution of the measured performance is close to the analytic predictions. In the next section these analytic derivations are further exploited to size the LNA for a given set of specifications according to the design flow presented in the previous chapter.

4.3 Optimization of the proposed LNA

The proposed LNAs, implemented in 28nm FDSOI technology process from STM, are sized for two different kinds of applications: one is dedicated to multi-standard communications, the other is for ultra low power applications. The core of each LNA has an area as low as 0.0015 mm². The layout and a micrograph of the chip are presented in figure 4.17. Both LNAs are in the same seal-ring and share the same ground plane. On both side there are the input (left) and output (right) RF pads, and at the top and bottom there are the DC pads.

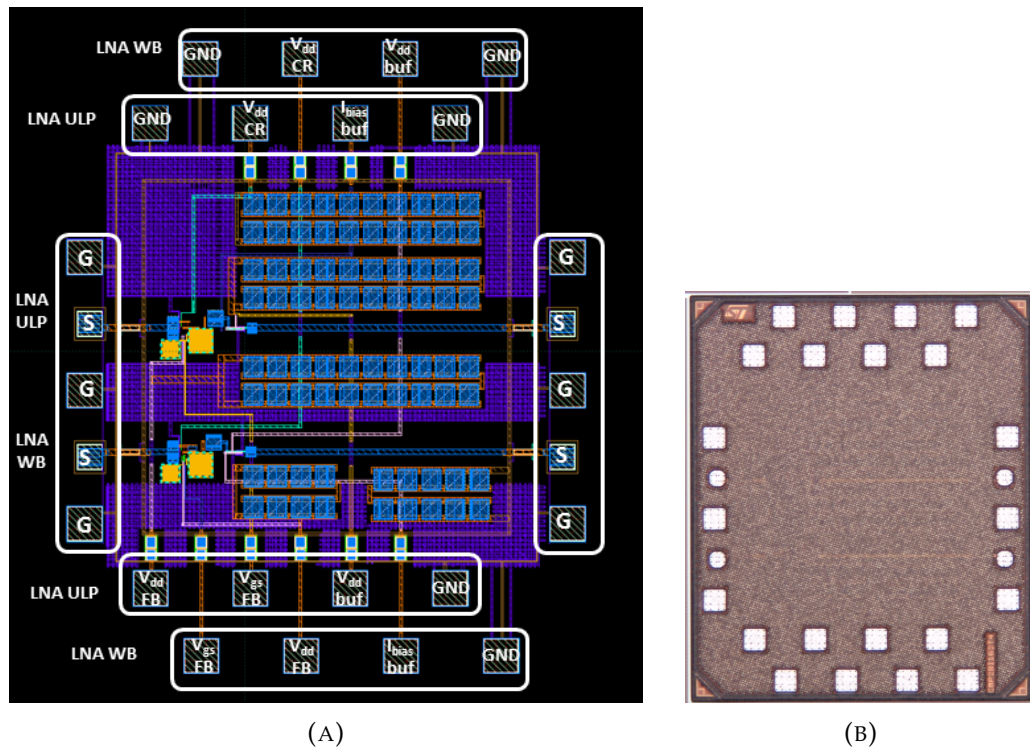


FIGURE 4.17: (a) Layout of the shunt-feedback current-reuse LNA and (b) micrograph of the chip.

This LNA has been fabricated during this thesis in 28 nm FDSOI and 65 nm CMOS bulk (still under fabrication) and during the thesis of Marcelo de Souza [45] in 130 nm CMOS bulk. Therefore, the three nodes can be compared and the results of section 3.1.3 verified. However, due to some process variations affecting the PMOS transistors, the results presented in this section are not as good as expected for the 28 nm FDSOI. Still there are coherent with theoretical investigations and comparable with the state of the art.

4.3.1 Wideband

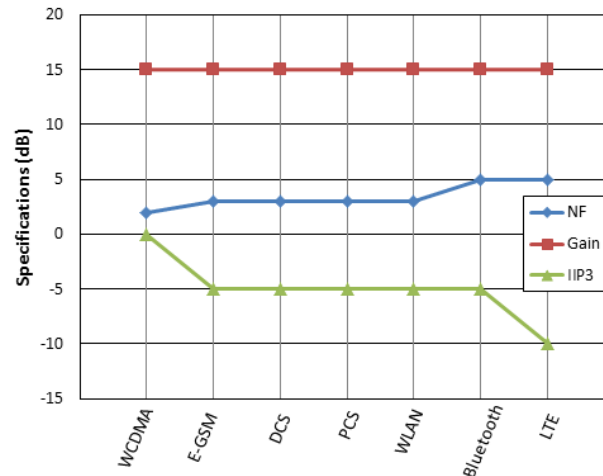


FIGURE 4.18: LNA's specifications for different communication standards.

The first case of study is dedicated to a multi-mode/multi-standard receiver. The LNA is expected to address a maximum of communication standards (maximum bandwidth) for the set of specifications presented in figure 4.18 and reported in table 4.1.

TABLE 4.1: Performances of the proposed LNA for a wideband application in 28 nm FDSOI, 65 nm and 130 nm [54].

Parameters	Specifications	28 nm FDSOI*	65 nm ⁺	130 nm*
$I_{D_{cr}}$ (mA)	N.A.	2.3	3.1	2.6
IC_{1n}	N.A.	3.1	1.2	2.8
$I_{D_{fb}}$ (mA)	N.A.	0.8	0.85	0.5
IC_2	N.A.	4.5	2.1	3.2
P_{DC} (mW)	< 5	3.7	3.9	3.11
BW (GHz)	Max.	6	4.2	2.1
G_v (dB)	> 15	17	16.3	19.2
NF (dB)	< 3	5.1 (2.5 ⁺)	2.3	2.4
$IIP3$ (dBm)	> 0	7.9	8.1	8.6
FoM	Max.	6.1 (17.6 ⁺)	9.4	5.1

*measured

⁺PLS

Three technology nodes are compared: 130 nm, 65 nm and 28 nm FDSOI. The flow chart of figure 3.18 is used to size the circuits. Following its steps, a maximum of FoM was found for a specific combination of each transistor's W . The results for each technology nodes are presented in table 4.1. The 65 nm LNA is still in fabrication (expected first quarter of 2018), therefore the results come from post-layout simulations and its performances may be slightly overestimated compared to 130 nm and 28 nm FDSOI which are measurement results. Based on our experience of this node for the design of RF circuits, the optimum IC and the performance should not shift a lot with measurement results.

The three technologies require that both the current reuse and the feedback stages should be biased in the MI region. The optimum consumption is similar for the three nodes, between 3.1 and 3.9 mW. The bandwidth and the gain-bandwidth product, as predicted in section 3.1.3, are significantly higher in more advanced technologies. However, the in-band voltage gain is higher in 130 nm because a larger gate length exhibits a smaller conductance, g_{ds} . Interestingly, the NF , close to 2.5dB for post layout simulations, does not change from one node to the other. The measurement results confirmed it for the 130 nm LNA. Yet, the measured NF in 28 nm FDSOI is 5 dB. Some complementary characterizations of the wafer reveals a larger gate resistance than expected for PMOS devices, which contributes to degrade the NF for the 28 nm FDSOI lot. The linearity is similar for all three nodes with an IIP_3 close to +8 dBm. Actually the short channel effects degrade the linearity of the current reuse stage, H_3 in equation (4.18b), for advanced node, but the feedback, through F_3 in equation (4.18c), compensates for it. It can therefore be noted that the proposed linearization is robust to the technology shrink.

TABLE 4.2: Wideband LNAs: state of the art.

Ref.	Tech. [nm]	BW [GHz]	NF [dB]	Gain [dB]	GBW [GHz]	IIP3 [dBm]	Supply [V]	P_{DC} [mW]	FoM_{LNA} [GHz]
[39]	130	0.2-3.8	2.8	19	32.1	-4.2	1	5.7	2.4
[40]	130	4.7	3	14	23.5	3.5	1.2	2.4	22.1
[44]	90	0.1-3	2.7	17	20.5	-0.9	2	5	3.8
[53]	90	0-6.5	2.7	16.5	43.4	-2	1.2	9.7	3.3
[47]	90	0.5-5	2	17	31.9	2.4	2	30	3.1
[41]	90	0.1-1.7	1.85	23	22.6	-2.85	2	2.8	7.8
[46]	65	0.1-10	2.7	10.5	33.2	-3.5	1	13.7	1.2
[50]	65	0.1-4.3	2.8-4	21.2	48.2	-7.7	1.2	2	4.5
This work	28 FD-SOI	0.2-6	5.1 (2.5⁺)	17	41.1	7.9	1.1	3.7	30.8 (88.4⁺)
This work [54]	130	0.1-2.1	2.4	19.2	18.2	8.6	1.3	3.1	57.7

The measurement results of the 28 nm FDSOI and 130 nm LNAs are compared to the state of the art in table 4.2. The figure of merit FoM_{LNA} , equation (4.21), accounts for the linearity according to ITRS standard definition,

$$FoM_{LNA} = \frac{BW_{-3dB} G_v IIP3}{P_{DC}(F_{total} - 1)}, \quad (4.21)$$

where BW_{-3dB} is expressed in GHz, G_v is expressed in linear units, $IIP3$ is expressed in mW, P_{DC} is expressed in mW and F_{total} is expressed in linear units. The proposed LNA exhibits state of the art FoM_{LNA} . Interestingly, this figure of merit is not really correlated to the technology node since the highest FoM_{LNA} are performed by LNAs which are implemented in different CMOS generations : 90 nm [41], 130 nm [54, 40] and 28 nm (this work). Hence FoM_{LNA} in equation (4.21), is helpful to compare the topologies but also the optimization of the circuit design in this case.

Besides table 4.2 confirms that the most advanced nodes achieve the largest GBW for similar power consumption. The minimum of NF is always close to 3 dB except for [41], it is only 1.85 dB because it uses multiple feedback paths in order to lower the noise. The voltage gain as well ranges from 16.5 to 23 dB for any technology except for [46] which privileged the bandwidth over the voltage gain. Finally, the proposed LNAs exhibit comparable performance with the state of the art in terms of gain, NF and bandwidth at a reduced power consumption. Furthermore they achieve the best linearity reported so far in the literature for inductorless architecture.

4.3.2 Low-power

The design of an ultra low power LNA, operating at 2.4 GHz, follows the same steps as the wideband LNA. The only difference being in the range of IC and W since the specifications are not the same. For an ultra low power application, the current consumption is critical, less than 1 mW of DC power is targeted here. Hence, the 130 nm CMOS process is not considered for this application since it can not reach 2.4 GHz with a low consumption and a proper voltage gain. The constraints on the linearity and the noise figure are also relaxed as a moderate sensitivity is accepted in low power applications. The specifications and the results are listed in table 4.3.

TABLE 4.3: Performances for an ultra low power application in 28 nm FDSOI and 65 nm.

Parameters	Specifications	28 nm FDSOI*	65 nm ⁺
$I_{D_{reuse}}$ (mA)	N.A.	0.5	0.9
IC_{1n}	N.A.	0.8	1
$I_{D_{fb}}$ (mA)	N.A.	0.26	0.3
IC_2	N.A.	1.5	1.7
P_{DC} (mW)	< 1	0.5	1.2
BW (GHz)	2.4	2.4	2.4
G_v (dB)	> 15	15	14.7
NF (dB)	< 7	7 (4.3 ⁺)	4
FoM	Max.	6.7 (11.4 ⁺)	7.1

* measured

+ PLS

Compared to the wideband LNA, the IC is smaller for low power LNA but still in MI region. The larger GBW of 28 nm process allows for a significant power saving compared to the 65 nm node. Indeed, the LNA consumes 1.2 mW in 65 nm CMOS bulk technology, and only 0.5 mW in 28 nm FDSOI technology, for the same voltage gain (15 dB) and bandwidth (2.4 GHz). Post-layout simulations of the two circuits shows that the 28 nm FDSOI LNA has a better FoM thanks to the reduced power consumption. The higher measured NF of the 28 nm LNA is due to the additional resistance on PMOS gate in the measured lot as discussed in the previous subsection.

TABLE 4.4: Low power LNAs: state of the art.

Ref.	Tech. [nm]	BW [GHz]	NF [dB]	Gain [dB]	GBW [GHz]	IIP3 [dBm]	Supply [V]	P_{DC} [mW]	FoM
[42]	180	0.4-1	4.2	15.5-18	3.6	-14/-21	1.2	0.2	0.4
[43]	130	0.1-2.7	4	20	26	-12	1.2	1.32	0.8
[49]	130	0.1-2.2	5.5	9.9	6.6	-11.5	1.2	0.4	0.5
[48]	90	0.1-7	6.5	12.6	29.4	-8	0.5	0.75	1.8
[14]	28 FD-SOI	0.5-8	6.7	18.8	65.3	-16	0.8	0.6	0.7
[This work]	28 FD-SOI	0.2-2.4	7 (4.3⁺)	15	12.4	-6.5	0.7	0.5	1.4 (3.2⁺)

If we compare the circuits reported in table 4.2, wideband LNA, and in table 4.4, low power LNA, the drastic reduction of the DC power does not impact equally the LNA's performances. The gain and the bandwidth are moderately affected since they are supported by the GBW which offers a good trade-off with technology shrink. Differently the NF and the IIP_3 are significantly degraded because they are proportional to the transistor's transconductance which reduces with the current decrease. Circuit techniques are required to compensate for it. Noise cancelling [49] and noise attenuation [43] maintain the noise figure close to 5 dB in inductorless LNA. For linearity purpose, the shunt feedback linearization [this work], reduces the intermodulation products and improves the IIP_3 at a moderate DC power penalty. Finally the proposed 28 nm FDSOI circuit exhibits overall good performance which contributes to achieve among the best FoM for inductorless low power LNAs.

Conclusion

In this chapter the methodology presented in chapter 3 has been applied to a highly linear wideband inductorless LNA. The equations of this section are validated through the measurement of a 28 nm FDSOI chip even though the bandwidth is not as high as expected and the noise figure is significantly increased due to process variations. It is optimized for multi-standard applications and then for ultra low power applications. In both case, the LNA achieves state of the art performance in term of gain, bandwidth and NF for a reduced power consumption. Furthermore, the linearization technique enables the best linearity achieved in literature so far.

The comparison between state of the art inductorless LNAs enables a fair comparison between the different technology for a given set of specifications. The trends outlined in the previous chapter (section 3.1.3) through the comparison of technological parameters are verified in table 4.2 and table 4.4. Indeed, the expected increase in the GBW and the decrease in the power consumption with technology shrink is verified here.

In the following chapter, the proposed LNA and the results of the *IC*-based methodology are further exploited to give some reconfiguration capabilities to the circuit. Switches are added to the proposed topology in order to adjust the optimum size and bias of each transistors to a given set of specifications.

Chapter 5

Adaptive Inductorless LNA

In chapter 3, the *IC*-based design methodology is developed through the sizing and optimization of two common LNAs. This method is well-suited for any CMOS technology as well as for any topologies of LNA and it also enables a fair comparison between these technologies and topologies. Then, in chapter 4, this design methodology is applied to an inductorless wideband LNA which answers the need for small footprint, low power and multi-standard operation. However, one of the challenges presented in chapter 1 has not been addressed yet: the need for reconfigurability. Indeed, for any targeted application, power saving can be addressed if the communication system can adapt its performance to the radio link conditions. Therefore, in this chapter, the inductorless LNA is implemented with a digital control of transistors' sizes and bias in order to be optimized for any given specifications. Then the proposed LNA is combined with an N-path filter which further improves its linearity and reconfigurability since these filters are highly selective and their center frequency can be tuned.

The first section of this chapter presents the implementation of the digital inductorless LNA through the study of switches, current mirrors and registers. Then, the complete architecture of the proposed LNA and its modes of operation are illustrated. Finally, in the last sections N-path filters are introduced with state of the art examples and the co-design of the LNA and the N-path filter is studied.

5.1 Inductorless LNA with digital control

The inductorless LNAs are optimized for either multi-standard applications or low power applications in chapter 4. The design variables that change from one application to the other are the size and bias of each transistor. Therefore, several transistors can be placed in parallel and turn on and off by RF switches in order to adjust the size. For the biasing, current mirrors controlled by DC switches can be used to adjust the drain currents and thus adjust the optimum *IC*. The architecture of the adaptive inductorless LNA is illustrated in figure 5.1. The current sources I_{reuse} and $I_{feedback}$ are current mirrors controlled by seven and six bits respectively. The core of the LNA is controlled by three bits (one for each transistor, M_{1n} , M_{1p} and M_2). Consequently, a 16-bits register is implemented with the LNA. This register will further be controlled by a Serial Peripheral Interface (SPI) for measurements purpose.

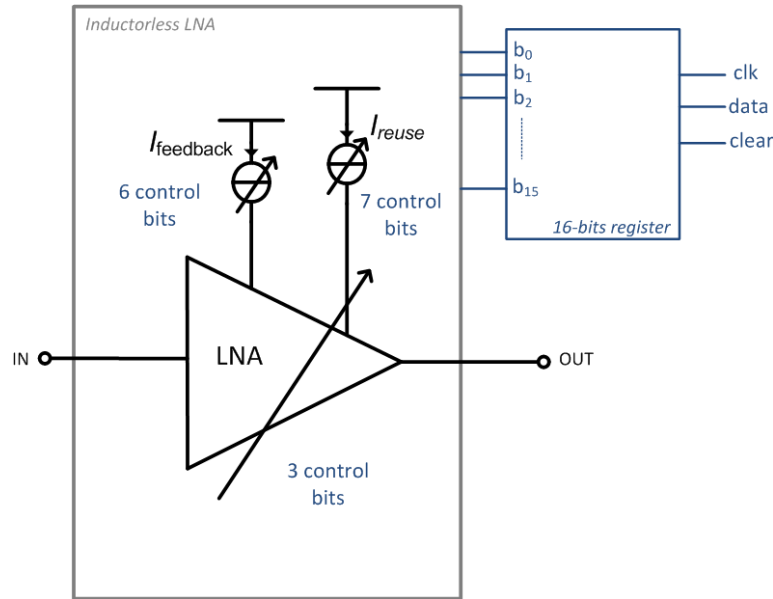


FIGURE 5.1: Architecture of the inductorless LNA combined with digital control.

In this section, the switches and current mirrors required for digital control and then the implementation of a 16-bits register are introduced. The last subsection presents the proposed digital LNA and its modes of operation. It is implemented in STM 65 nm CMOS process and the results presented here come from post-layout simulations since the chip is still in fabrication.

5.1.1 Switches and current mirrors

MOS transistors are commonly used in digital circuits. They can be controlled to be switched on and off. Indeed, a logical 0 corresponds to a low voltage on the gate of transistors and therefore NMOS are off and PMOS are on. Conversely, a logical 1 corresponds to a high voltage on the gate and therefore NMOS transistors are on and PMOS are off. This can be simply illustrated with the example of an inverter figure 5.2.

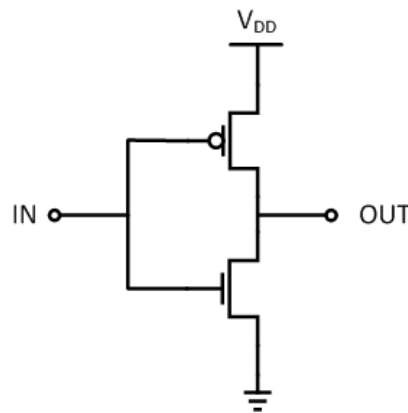


FIGURE 5.2: Schematic of the transmission gate.

When the input is set to 0, the PMOS is on and the NMOS is off, therefore the output is connected to V_{DD} which is a logical 1. When the input is set to 1, the PMOS is off and the NMOS is on, therefore the output is connected to gnd which is a logical 0. This inverter is further used for the implementation of switches.

Switches

Two types of switches are required for the digital LNA, DC switches to control the current mirrors and RF switches to control the size of the transistors in the current reuse stage and in the feedback path. The first one is a simple transmission gate as illustrated in figure 5.3. It consists of an NMOS and a PMOS transistors with their drains and sources connected to each other. Their gates are connected through an inverter. When the bit *ctrl* is a logical 1, both transistors are conducting whereas a logical 0, turns off the two transistors.

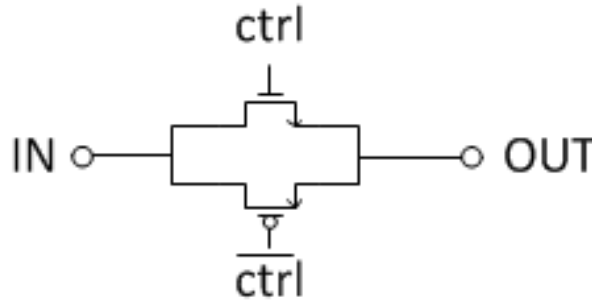


FIGURE 5.3: Schematic of the transmission gate.

The RF switch is illustrated in figure 5.4. It consists of two NMOS transistors larger than for the DC switch since larger currents flow through them. When the bit *ctrl* is set to 1, the first transistor is on and the second is off; the signal is transmitted from the input to the output. When the bit *ctrl* is equal to 0, the first transistor is off and the second is on; the signal is forced to the ground (or to V_{DD} for the PMOS version of this switch).

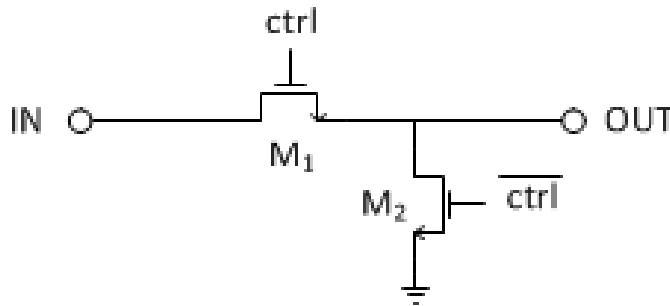


FIGURE 5.4: Schematic of the RF switch.

The time response of this switch is illustrated in figure 5.5 for an input voltage of 0.6 V. In order for the fall and rise times to be as low as possible, the gate width of the inverter's transistors are set to $1.8\ \mu\text{m}$ and the gate width of the NMOS transistors are set to $100\ \mu\text{m}$ for M_1 and $10\ \mu\text{m}$ for M_2 . The output voltage is equal to V_{in} when the bit is a logical 1 with a low rise time and a low fall time.

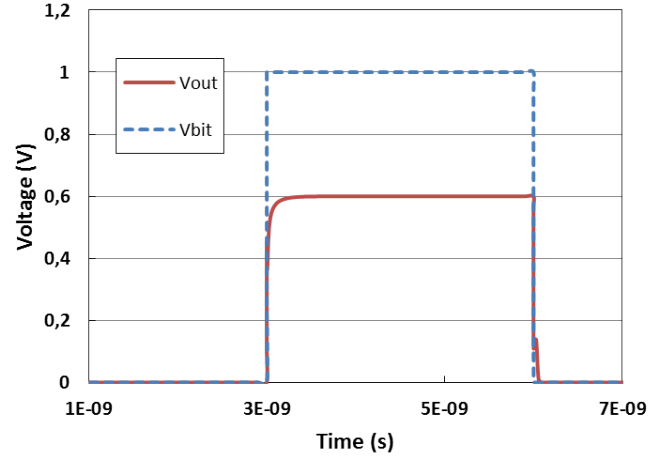


FIGURE 5.5: Time response of the RF switch for an input voltage of 0.6 V.

Furthermore, in figure 5.6, the evolution of the output voltage versus the input voltage is plotted for different values of the control voltage. It appears that for the DC switch, the control voltage does not matter whereas for the RF switch, V_{ctrl} must always be superior to V_{in} in order for V_{out} to copy V_{in} .

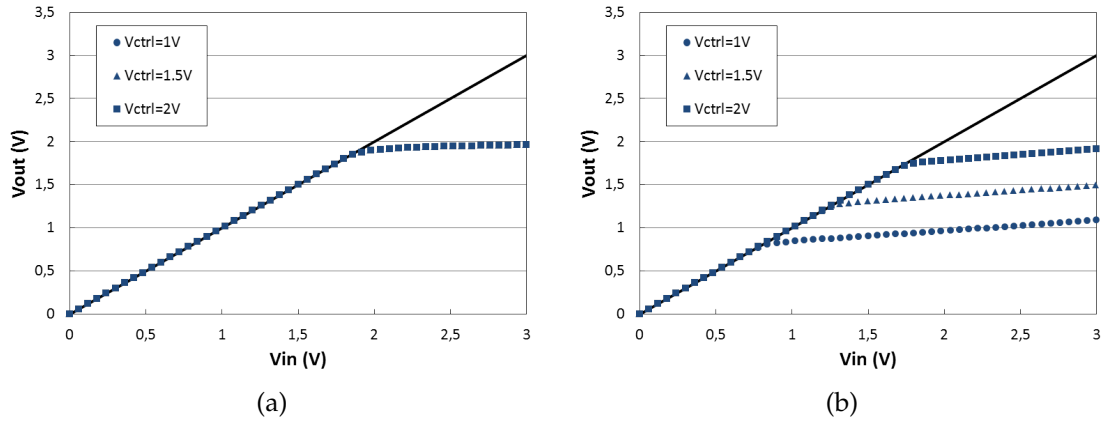


FIGURE 5.6: V_{out} versus V_{in} for different values of the control voltage of the (a) DC switch and (b) RF switch.

Current mirrors

Current mirrors are used to steer the biasing condition in the forward path (OTA) and in the feedback path. The basic principle is that a perfectly matched pair of transistors with their gates and sources connected, thus the same V_{gs} , have the same drain current. Therefore, the drain current of the reference transistor flows also through the copying transistor. In practice this basic configuration achieves a moderate output impedance which makes the copying error dependent of the load. This drawback can be partially compensated by adjusting the quantum and the number of bit of the current DAC. It is selected for this design because it operates with a minimum supply voltage.

In order to adjust IC_{1n} of the current reuse and IC_2 of the feedback path, a PMOS current mirror and a NMOS current mirror, respectively, are required. The schematic of

the current mirror in NMOS version is illustrated in figure 5.7. It consists of a reference transistor M_{ref} whose drain current is set by V_{DDN} and by the three resistances controlled by DC switches and four copying transistors M_0, M_1, M_2 and M_3 which are also controlled by DC switches on their gates. The gate width of these transistors is set by $W_{M_n} = 2W_{M_{n-1}}$ and $W_{M_0} = W_{M_{ref}}$. Hence, to control the current of the feedback path, $I_{feedback}$, this mirror with its six control bits enables lots of combination and therefore a large range of $I_{feedback}$ from a few micro-amperes to tens of mili-amperes.

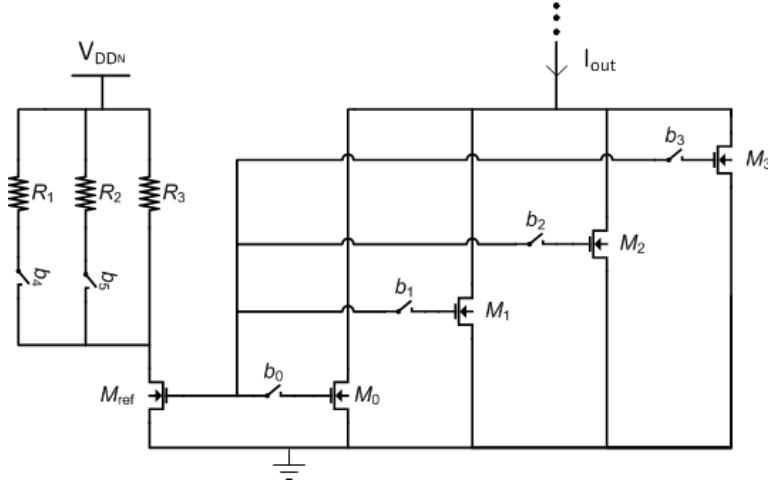


FIGURE 5.7: Schematic of the NMOS current mirror.

The PMOS current mirror is based on the same topology as the NMOS current mirror as illustrated in figure 5.8. It has seven control bits (three for the resistances and four for the copying transistors). This current mirror is placed at the source of the PMOS transistor in the current reuse stage in order to control I_{reuse} and therefore IC_{1n} .

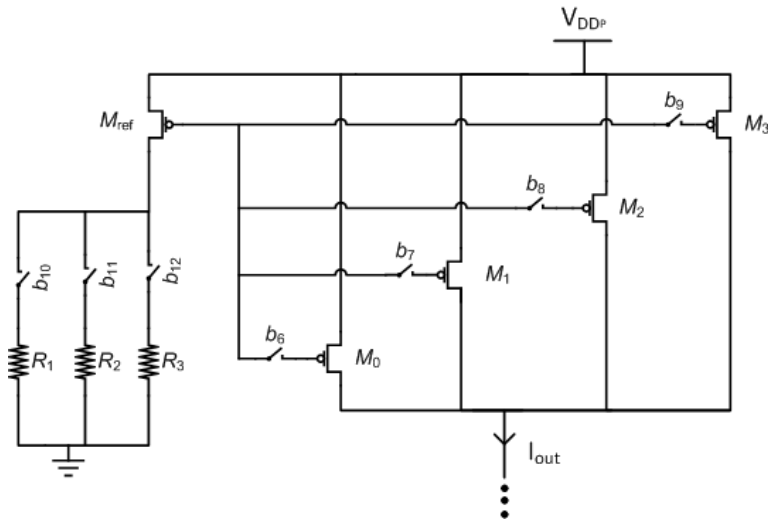


FIGURE 5.8: Schematic of the PMOS current mirror.

As mentioned above, the transistors of the current mirrors must be perfectly matched but some mismatch can be introduced by process variations. In order for the mirror to be robust to these variations, they should impact each transistor in the same default. Thus, the transistors are placed in a common centroid configuration [58]. Indeed, they are divided into parts with the same number of fingers, each part must be surrounded by the same pattern

in X and Y directions. A basic pattern for two transistors A and B is illustrated in figure 5.9. Since the transistors have different boundary conditions, dummies (shorted transistors) are placed on both sides.

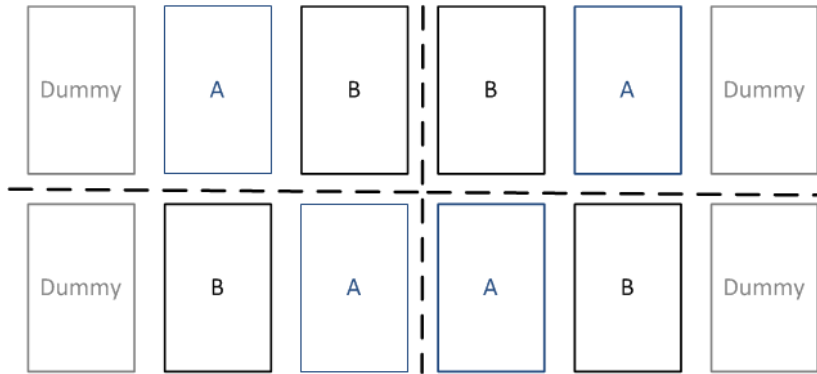


FIGURE 5.9: Example of a centroid pattern.

There are many different patterns that can be suited for the design of circuits featuring a large number of transistors. The layout of the NMOS current mirror is illustrated in figure 5.12a. It is based on the following pattern:

ABAABA
BABBAB
ABAABA

where A are transistors with 9 gate fingers of 3 μm and B are transistors with 3 gate fingers of 3 μm . The two transistors B in the center are the transistor M_{ref} and the others B transistors are dummies (in gray). Each A transistor includes a part of M_0 , M_1 , M_2 and M_3 as illustrated in figure 5.10

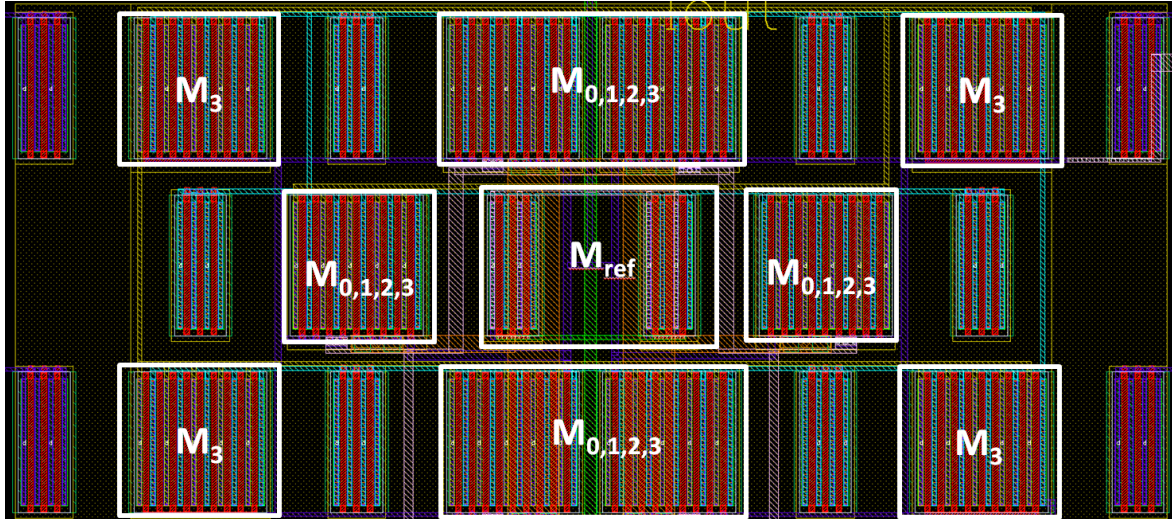


FIGURE 5.10: Layout of the NMOS current mirror.

The PMOS mirror's layout is slightly different as illustrated in figure 5.11. The reference transistor is placed in the center, then M_0 is divided in two and surrounds M_{ref} . Then M_1

surrounds M_0 and the same goes for M_2 and M_3 . Furthermore, dummies transistors are placed on the four sides. Thus, each transistor sees the same pattern in X and Y directions.

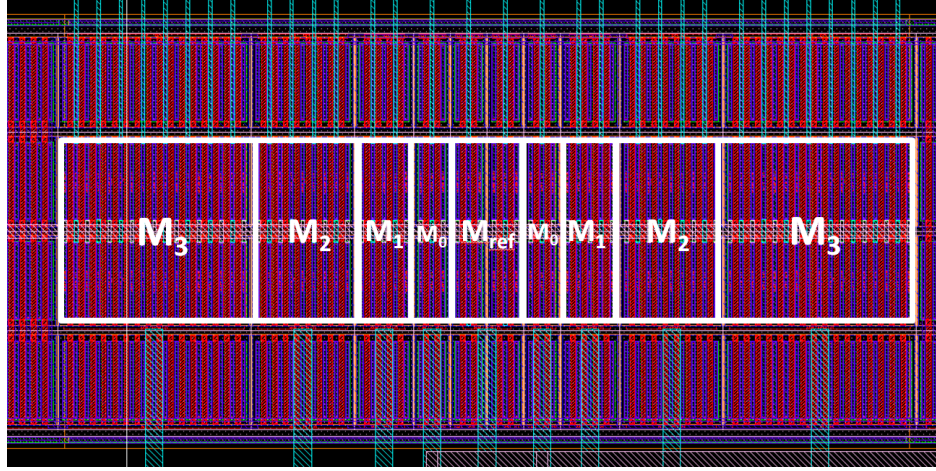


FIGURE 5.11: Layout of the NMOS current mirror.

Both layout are presented in figure 5.12. The NMOS version has a core area of $52 \mu\text{m} \times 43 \mu\text{m}$ and the PMOS version $76 \mu\text{m} \times 40 \mu\text{m}$.

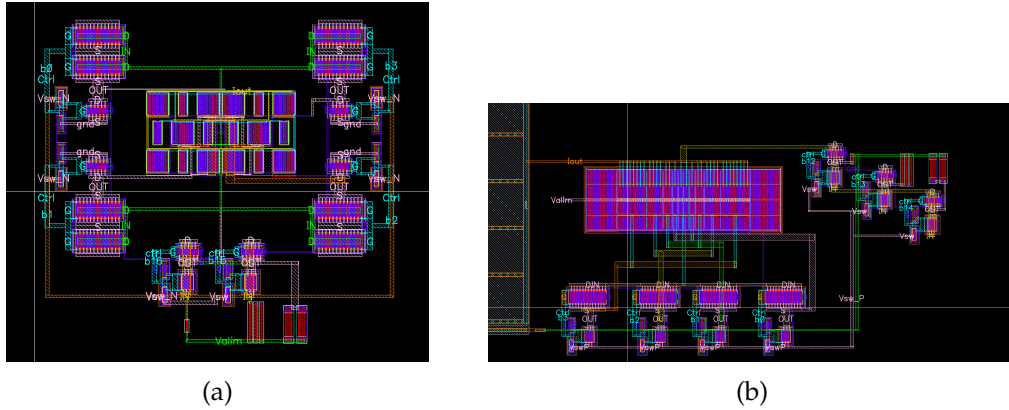


FIGURE 5.12: Layout of the current mirrors: (a) NMOS version and (b) PMOS version.

5.1.2 16-bits register

In order to control the 16 bits of the current mirrors and switches mentioned above, a serial 16-bit shift register is implemented. Shift registers (SR) are used in digital circuits to save and manipulate data. They consist of serially connected D-type flip-flop (DFF) as illustrated in figure 5.13 [59].

A DFF is a sequential circuit which means that its outputs depend on the previous system sets. It has two inputs: the data (d) and the clock (clk) and two outputs: q and $\bar{q}$. The value of q remains still all the time except when a positive edge occurs (clock goes from 0 to 1), at this time q takes the value of d . Different implementations of DFF exist and can be divided into two categories: master-slave or pulse-based. The former enables simpler timing behavior and the latter consumes less power. In this work, a static transmission-gate-based

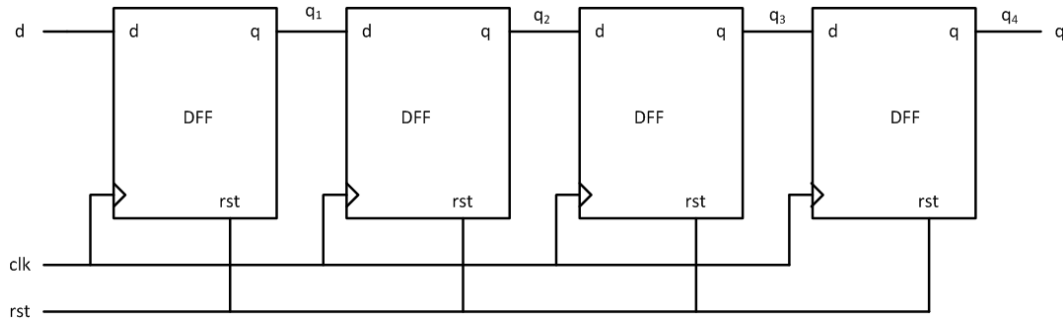


FIGURE 5.13: Architecture of a 4-bits shift register based on DFF.

(STG) flip-flop, which belongs to the master-slave category, is implemented. It consists of several logic circuits: inverters and transmission gates as illustrated in figure 5.14. This implementation enables a reduced noise and power consumption compared to its dynamic version.

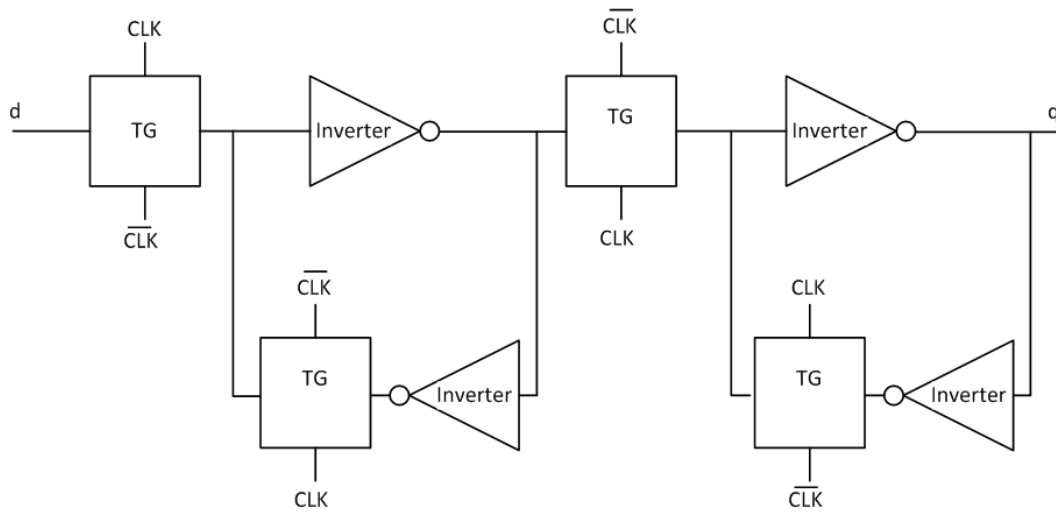


FIGURE 5.14: Architecture of a D-type flip-flop.

Furthermore, a reset function is added to the basic DFF. It allows the output to be forced to 0 when necessary. The implementation of such DFF is presented in figure 5.15. Finally, these reset DFF are combined to implement a 16-bits shift register.

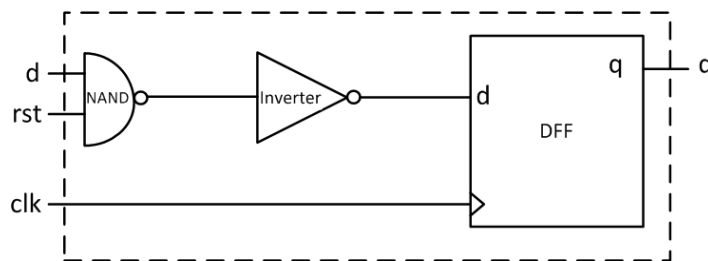


FIGURE 5.15: Architecture of a D-type flip-flop with reset function.

The digital blocks required for the implementation of the digital inductorless LNA are presented in this subsection. The 16-bits shift register enables control of the 6 bits which set

$I_{feedback}$ in the NMOS current mirror, the 7 bits which set I_{reuse} in the PMOS current mirror and the 3 bits which set the gate width of the three transistors M_{1n} , M_{1p} and M_2 .

5.1.3 Architecture of the proposed LNA

In this subsection, the architecture of the proposed LNA is detailed, then the results of the three modes of operation are presented. Finally, the performances of the digital inductorless LNA are compared with the performances of the inductorless LNA presented in the previous chapter.

Current-reuse stage

The schematic of the digitally-controlled current-reuse stage is illustrated in figure 5.16. The current source I_{reuse} is the PMOS current mirror presented in figure 5.8. The PMOS transistors' gate width are $55\text{ }\mu\text{m}$ and the NMOS transistors' gate width are $50\text{ }\mu\text{m}$ and $100\text{ }\mu\text{m}$, respectively. Three modes of operation are possible:

- $b_{13} = b_{14} = 1$, both switches are on and the transistors total gate width are $W_{1n} = 150\text{ }\mu\text{m}$ and $W_{1p} = 110\text{ }\mu\text{m}$. It is the wideband mode for multi-standard applications as presented in the previous chapter.
- $b_{13} = 0$ and $b_{14} = 1$, the transistors total gate width is $W_{1n} = 150\text{ }\mu\text{m}$ and $W_{1p} = 55\text{ }\mu\text{m}$. It is the hybrid mode: M_{1p} is smaller than for the wideband mode, thus, reducing the bandwidth when necessary and adjusting the optimum power consumption.
- $b_{13} = b_{14} = 0$, both switches are off and the transistors total gate width is $W_{1n} = 50\text{ }\mu\text{m}$ and $W_{1p} = 55\text{ }\mu\text{m}$. It is the low-power mode as presented in the previous chapter.

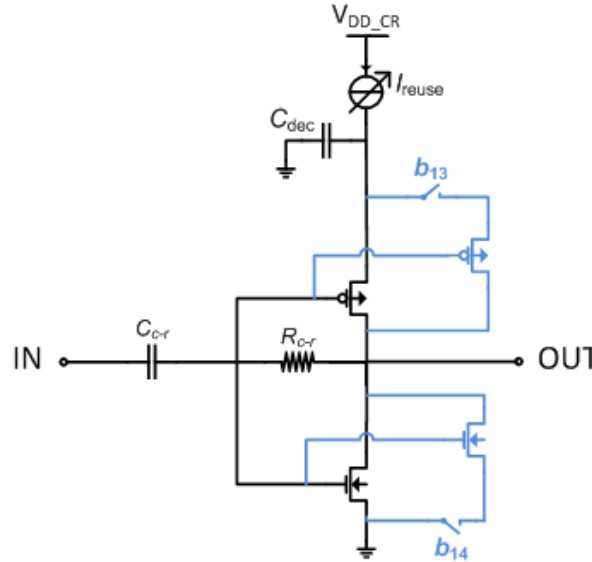


FIGURE 5.16: Schematic of the digital current-reuse.

Feedback path

The schematic of the digitally-controlled feedback path is illustrated in figure 5.16. The current source I_{fb} is the NMOS current mirror presented in figure 5.7. The transistors' gate width are 10 and 15 μm , respectively.

- When $b_{15} = 1$, the feedback path is set for the wideband mode and the hybrid mode.
- When $b_{15} = 0$, the feedback path is set for the low-power mode.

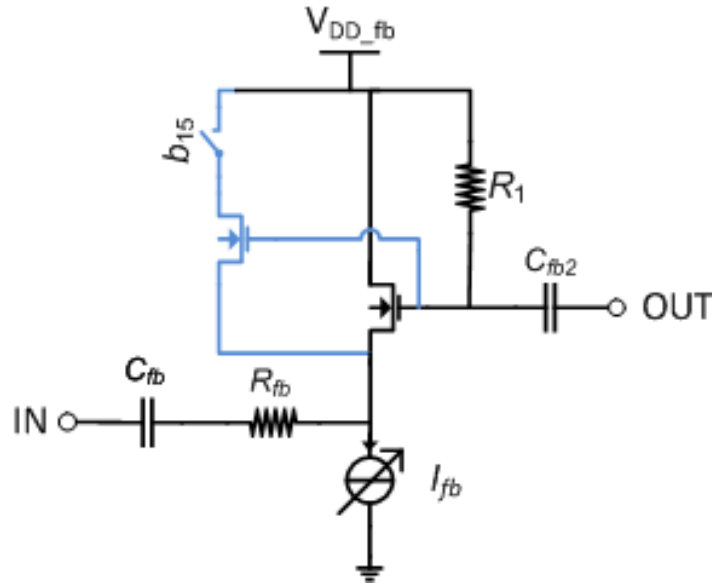


FIGURE 5.17: Schematic of the digital feedback path.

The proposed LNA has been designed in STM 65 nm CMOS process. The layout of the wideband and the low-power LNAs presented in the previous chapter and the layout of the

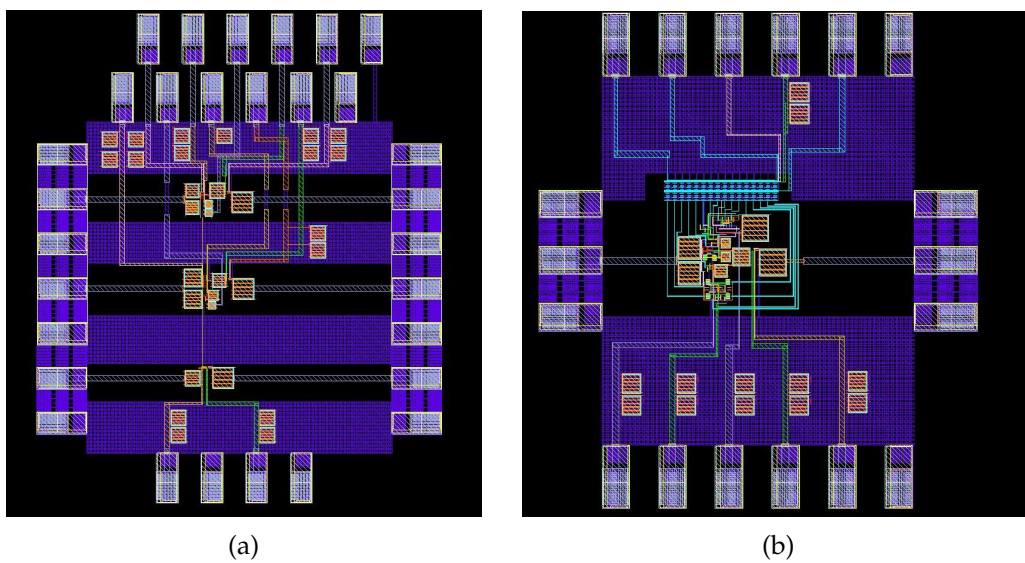


FIGURE 5.18: Layout of the (a) low-power and wideband LNAs and (b) adaptive inductorless LNA.

adaptive LNA are presented in figure 5.18a and figure 5.18b, respectively. The area of the digital LNA is 0.05 mm^2 .

Modes of operation

The complete reconfigurable LNA has been described above and is illustrated in figure 5.19. The objective of this adaptive LNA is to be optimized at a maximum FoM for any applications. Indeed, changing only the current of the LNA would change the IC but not the W and thus the FoM would be degraded. Hence, the digital control of the biasing and of the sizing enables the circuit achieves a maximum FoM for any mode of operation.

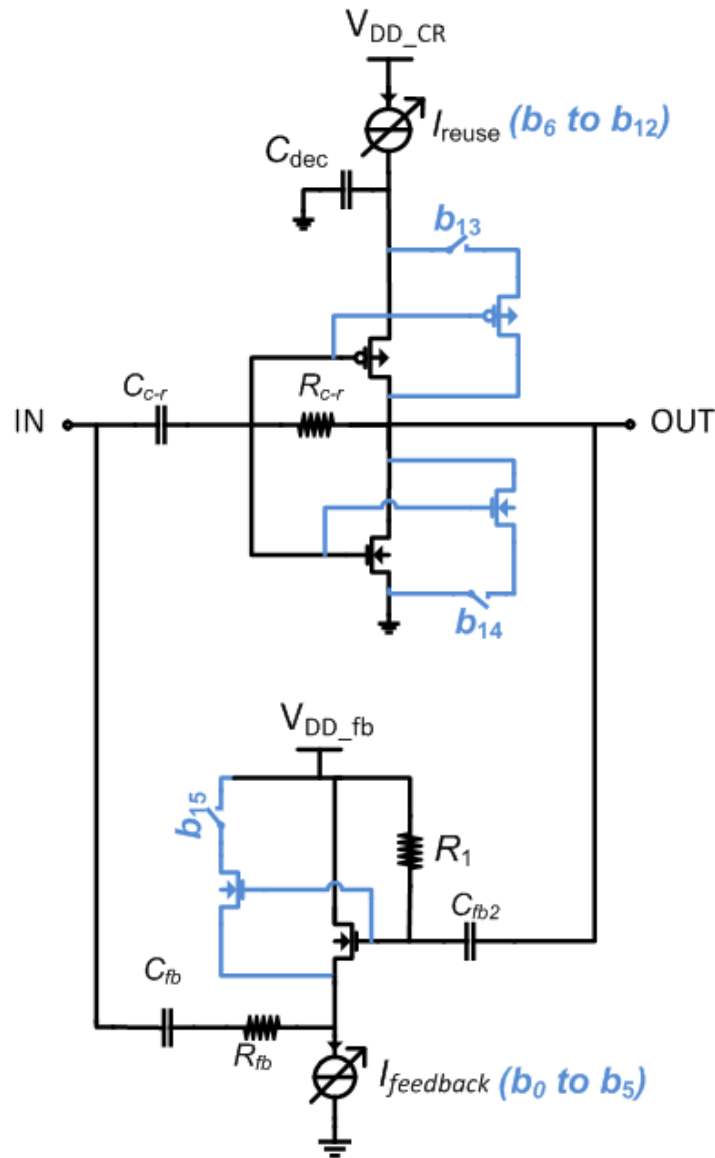


FIGURE 5.19: Schematic of the inductorless LNA combined with digital control.

Its performances are discussed in this section. As mentioned above there are three cases of interest: a low-power mode, an hybrid mode and a wideband mode. The post-layout results of the proposed LNA for the three modes are listed in table 5.1 and the results presented in chapter 4 are reminded.

TABLE 5.1: Performances of the adaptive inductorless LNA and comparison with the stand alone LNAs of chapter 4 (* table 4.1 and + table 4.3).

Performance	Wideband	Hybrid	Low-power	Wideband*	Low-power ⁺
$I_{D_{cr}}$ (mA)	3.1	2.1	1	3.1	0.9
$V_{DD_{cr}}$ (V)	1.2	1.1	1.1	1	1
$I_{D_{fb}}$ (mA)	0.85	0.85	0.5	0.8	0.3
$V_{DD_{fb}}$ (V)	1	1	1	1	0.9
P_{DC} (mW)	4.5	3.1	1.6	3.9	1.2
BW (GHz)	4.1	3.1	2.4	4.2	2.4
G_v (dB)	16	15.8	15	16.3	14.7
NF (dB)	2.7	2.9	4.1	2.3	4
IIP_3 (dBm)	5	1	-1.4	8.1	-2
FoM	6.9	6.5	6.1	9.4	7.1

The hybrid mode achieves similar performance than the wideband mode except for the bandwidth and the consumption is reduced by a factor 1.5. Their gain and NF vary only by 0.2 dB. This mode of operation can be useful when less bandwidth is necessary in order to save power without degrading the overall performance. In the low power mode, the power consumption is reduced by a factor 3. The bandwidth is limited to 2.4 GHz and the NF to 4.1 dB in this case. The LNA still achieves 15 dB gain and a high linearity, IIP_3 is -1.4 dBm, with respect to the 1.6 mW of DC power. This performances are compared in figure 5.20 to the specifications of various standards.

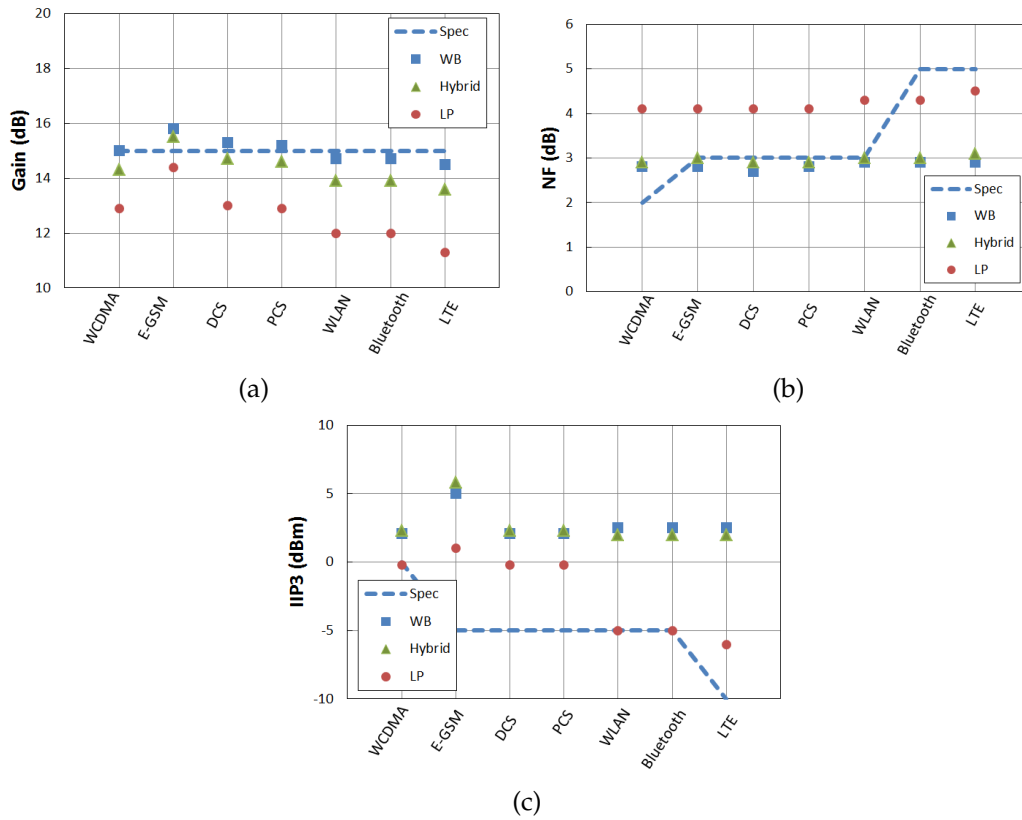


FIGURE 5.20: (a) Gain, (b) NF and (c) IIP_3 of the three modes of configuration versus the standards' specifications.

Compared to the results of table 4.1 and table 4.3, the total power consumption, P_{DC} , is slightly increased due to the increased supply voltage required by the current mirrors. However, it still remains very low compared to state of the art LNAs table 5.2. The noise figure is also increased especially for the wideband mode where it is equal to 2.7 dB instead of 2.3 dB. This is due to the noise brought by the transistors of the current mirrors and the switches. In the low power mode the difference is less significant because the drain currents must be slightly increase to reach the 2.4 GHz bandwidth.

The state of the art LNAs presented in chapter 4 are compared to the post-layout simulations of the adaptive LLNA in table 5.2. The adaptive LNA compares favorably with other works optimized for only one application. The reconfigurability enables the adaptive LNA to be optimized for various radio link conditions and different sets of specifications which is not the case for the LNAs reported in the state of the art.

TABLE 5.2: Inductorless LNAs: state of the art.

	Ref.	Tech. [nm]	BW [GHz]	NF [dB]	Gain [dB]	GBW [GHz]	IIP3 [dBm]	Supply [V]	P_{DC} [mW]	FoM _{LNA} [GHz]
WB	[39]	130	3.6	2.8	19	32.1	-4.2	1	5.7	2.4
	[40]	130	4.7	3	14	23.5	3.5	1.2	2.4	22.1
	[44]	90	2.9	2.7	17	20.5	-0.9	2	5	3.8
	[53]	90	6.5	2.7	16.5	43.4	-2	1.2	9.7	3.3
	[47]	90	4.5	2	17	31.9	2.4	2	30	3.1
	[41]	90	1.6	1.85	23	22.6	-2.85	2	2.8	7.8
	[46]	65	9.9	2.7	10.5	33.2	-3.5	1	13.7	1.2
	[50]	65	4.2	2.8-4	21.2	48.2	-7.7	1.2	2	4.5
	[This work]	65	4.1	2.7	16	26	5	1.2	4.5	22
Hybrid	[This work]	65	2.1	2.9	15.8	19	1	1.1	3.1	8
LP	[42]	180	0.6	4.2	15.5	3.6	-14	1.2	0.2	0.4
	[43]	130	2.6	4	20	26	-12	1.2	1.32	0.8
	[49]	130	2.1	5.5	9.9	6.6	-11.5	1.2	0.4	0.5
	[48]	90	6.9	6.5	12.6	29.4	-8	0.5	0.75	1.8
	[14]	28	7.5	6.7	18.8	65.3	-16	0.8	0.6	0.7
	[This work]	65	2.4	4.1	15	13	-1.4	1	1.6	4.9

This section described a fully reconfigurable inductorless LNA. Its performances can be adjusted to answer different set of specifications such as ultra low power consumption or wide bandwidth. However, it still requires filtering for the out-of-band blockers, especially for multi-standards applications. Furthermore, this filter should also be inductorless and reconfigurable. Therefore, N-path filters are studied to be combined with the proposed LNA as they consist of switches and capacitances only and their center frequency as well as their bandwidth are tunable.

5.2 N-path filters

5.2.1 Brief history of N-path filters

N-path filters first appeared many decades ago [60]. The first time-variant system was proposed in 1948 by Busignies and Dishal in [61]. It consists of a rotating wheel of capacitors in series with a resistance. The response of this filter shows peaks at the harmonics of the wheel's frequency of rotation. Then, in 1953, Smith presented an analysis of such circuits as illustrated in figure 5.21. He introduced in [62], the equation of the bandwidth of the harmonics as,

$$BW_{-3db} = \frac{1}{\pi NRC}, \quad (5.1)$$

where N is the number of commutated capacitors, R is the series resistance and C is the value of the commutated capacitors.

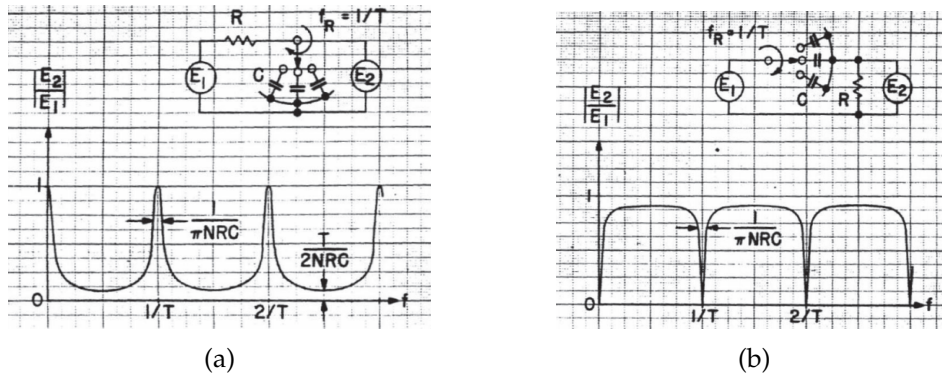


FIGURE 5.21: (a) Band-pass and (b) notch filters.

Source: [62]

Based on these works, in 1960, Franks and Sandberg proposed the first N-path filter as illustrated in figure 5.22 [63]. With this filter, the signal is not filtered at RF but in baseband. Indeed, an input signal goes through N paths. Each path consists of a mixer to down-convert the signal with different phases of a local oscillator (LO). Then the baseband signal goes through a transfer function $h(t)$. Finally it is up-converted again with the phases of a second LO.

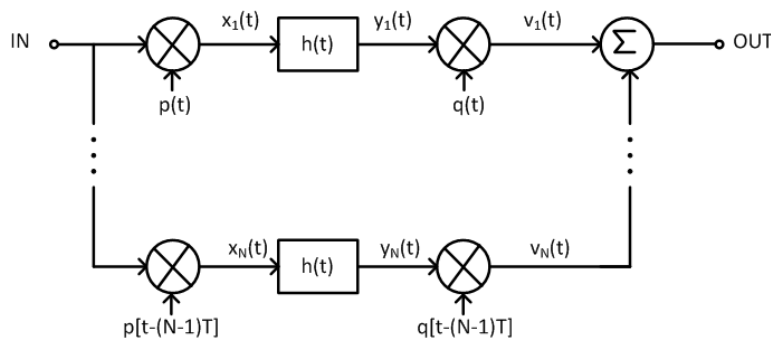


FIGURE 5.22: Architecture of the first N-path filter.

However, at that time, technology did not enable efficient filtering because of mismatching between the paths and because of the low switching frequency. Currently, with the performance of CMOS technologies, N-path filters appear as a promising technique for filtering.

5.2.2 Principle of operation

In [64], the authors propose a simplified version of Franck and Sandberg's version presented above. Assuming that the transfer function $h(t)$ is a low-pass filter, it can be replaced by a simple RC filter. Then, only one set of switches can be used and the resistance can be shared for all the paths. This results in a simple bandpass N-path filter (figure 5.23) where the center frequency is defined by the switching frequency and the bandwidth is given by equation (5.1). Similarly, if the transfer function $h(t)$ is a high pass filter then the resulting N-path filter behaves as a notch filter centered around the switching frequency with the same equation for the bandwidth.

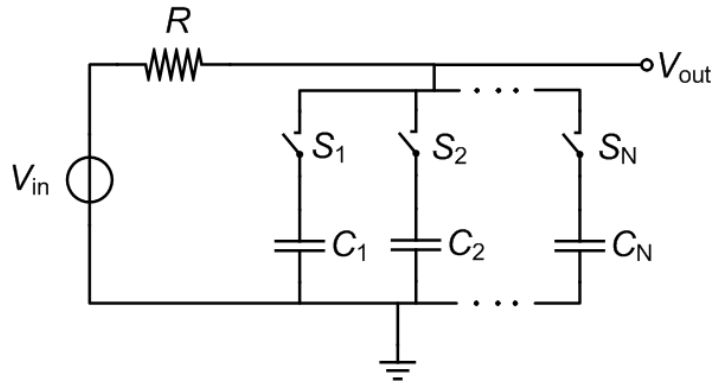


FIGURE 5.23: Schematic of a N-path filter.

A 4-path filter based on this schematic is sized in CMOS 65 nm. Its quality factor is given by,

$$Q = \pi N R C f_{switch}, \quad (5.2)$$

and its transfer function is defined in [65] as,

$$T(j\omega) = \left| \frac{8}{\pi^2} \left[\frac{\frac{j\omega}{2R_x C}}{(j\omega)^2 + \frac{j\omega}{2R_x C} + \omega_{LO}^2} \right] \right| \quad (5.3)$$

where $R_x = R_s + R_{sw}$, R_s is the source resistance and R_{sw} is the switch resistance. This analytical expression has been compared to simulation results in figure 5.24. The simulation fits with the theory except for the harmonics at $n f_{switch}$ which are not taken into account in equation (5.3). Furthermore, according to this equation, selectivity increase with large values of capacitance. Hence, there is a trade-off between the selectivity of the filter and its integration.

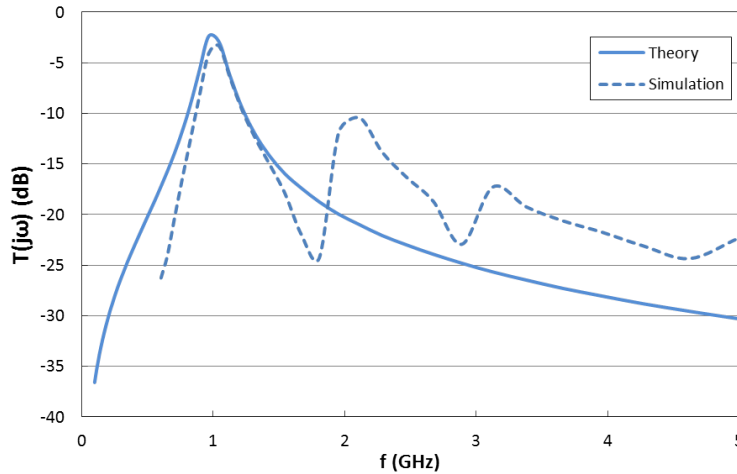


FIGURE 5.24: Response of a 4-path filter.

The time domain waveforms of a 4-path filter are presented in figure 5.25. In order for the N-path filter to operate, its time constant RC should be larger than T_{on} . Indeed, the longer last the voltage of a capacitor applied to the output voltage, the more pronounced is its effect [60]. Furthermore, the output voltage V_{out} of a 4-path filter being a stair-case approximation of the sinusoidal input voltage, N should be high for V_{out} to be closer to a sinusoid. Thus, 8-path produces a more efficient filtering than 4-path filters reducing the folding back [64].

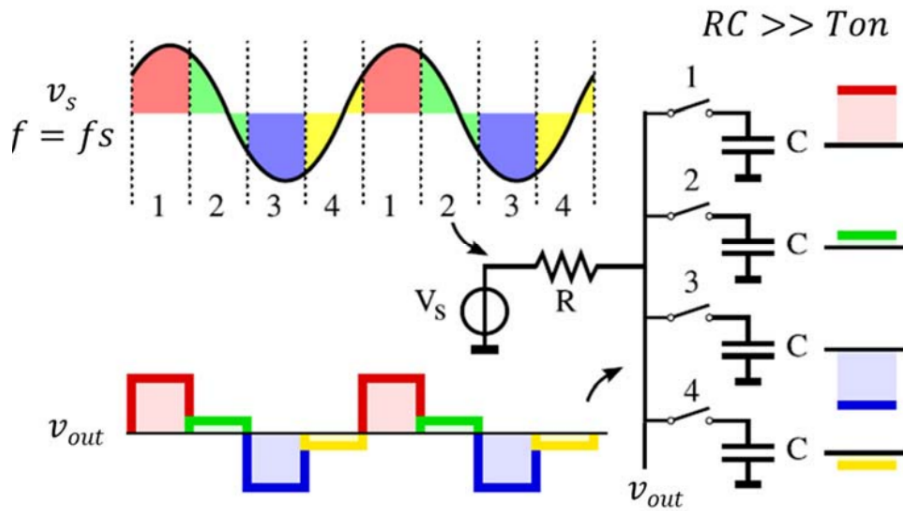


FIGURE 5.25: Time domain waveforms of a 4-path filter.

Source: [64]

N-path filters offers many advantages such as a tunable bandwidth depending on the values of R and C and a precise and tunable center frequency depending on the value of the switching frequency. However, there are some limitations to these filters. Indeed, the out of band rejection is limited by the resistance of the switches R_{sw} as it is given by $R_{sw}/(R_{sw}+R_s)$. Furthermore, the frequency range is limited by the synthesis of f_{switch} . In the next section, solutions to address these limitations are presented through state of the art examples. Finally, the design of an N-path filter combined with the proposed LNA is studied in the last subsection.

5.3 Co-design of LNA and N-path filter

5.3.1 State of the art

There are many works focusing on the design of N-path filters [66, 67, 68] as well as their integration in RF front-end [69, 70, 71]. In [66], the authors propose a low-noise tunable 6th order N-path bandpass filter as illustrated in figure 5.26. It consists of three differential 8-path filters connected by gyrators. In this work, the authors propose an efficient design methodology for such filters based on equation (5.3). Furthermore, the gyrator enables an active gain of +25 dB.

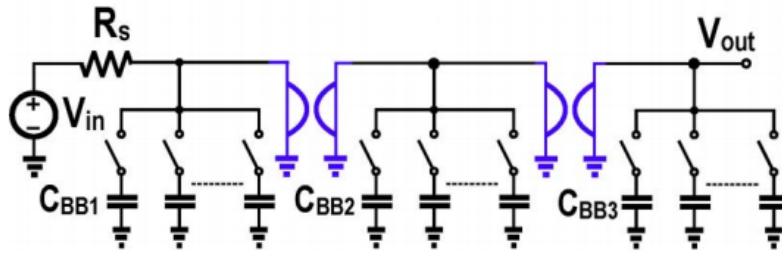


FIGURE 5.26: 6th-order N-path filter.
Source: [66]

In [68], the authors propose a differential 4-path filter as illustrated in figure 5.27. Differential structure enables the suppression of even order harmonics and offers state of the art performance with a IIP_3 of 14 dBm, a NF lower than 5.5 dB and for a power consumption of 2 to 16 mW. However, this structure requires very large capacitances of 66 pF.

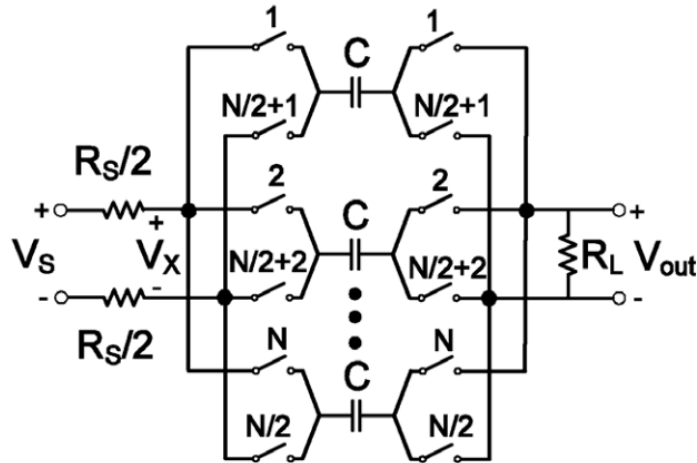


FIGURE 5.27: Differential N-path filter.
Source: [68]

N-path filters can be implemented in mixer-first receivers to enhance linearity and RF filtering. However, this solution requires large devices and high power consumption. Another solution consists of implementing the N-path with g_m -cells. This leads also to a moderate gain and/or high power consumption. An efficient solution to lower the consumption while keeping high gain, low noise and high linearity is to implement LNAs with a N-path filter. Some works propose to place the N-path filter before a wideband LNA [72, 73] but this leads to a significant increase of the NF . In [69], the author implements an 8-path filter in parallel

to the LNA. This structure enables the use of the miller effect to reduce the required value of the capacitances. Indeed, they are divided by the loop gain $1 + A_0$ where A_0 is the gain of the LNA.

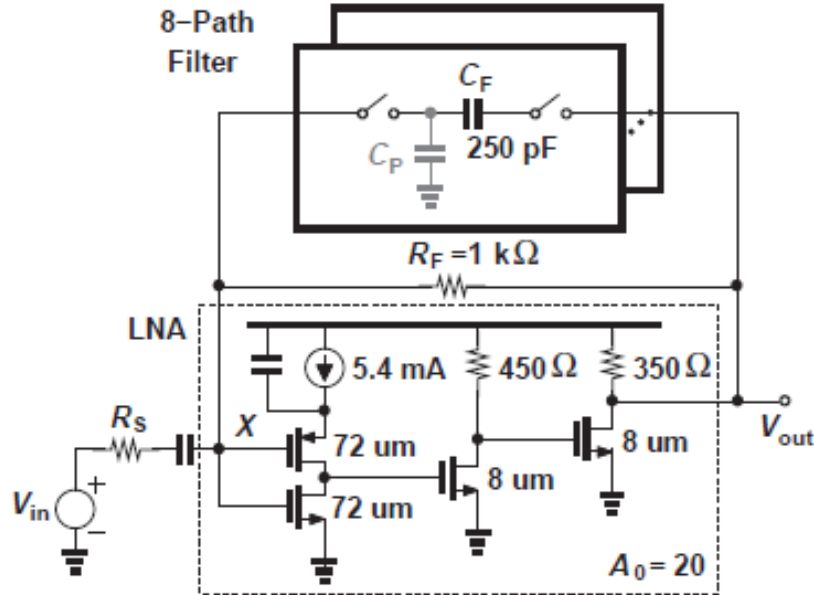


FIGURE 5.28: Miller bandpass filter.

Source: [69]

In [70], the authors proposed a LNA with an interferer reflecting loop as illustrated in figure 5.29. In the feedback path they place a N-path notch filter in series with a buffer. Thus, at the targeted frequency, the loop gain is very small and therefore the LNA is matched at this frequency. For out-of-band signals, the loop gain is large and thus, the LNA is not matched, blocking these signals.

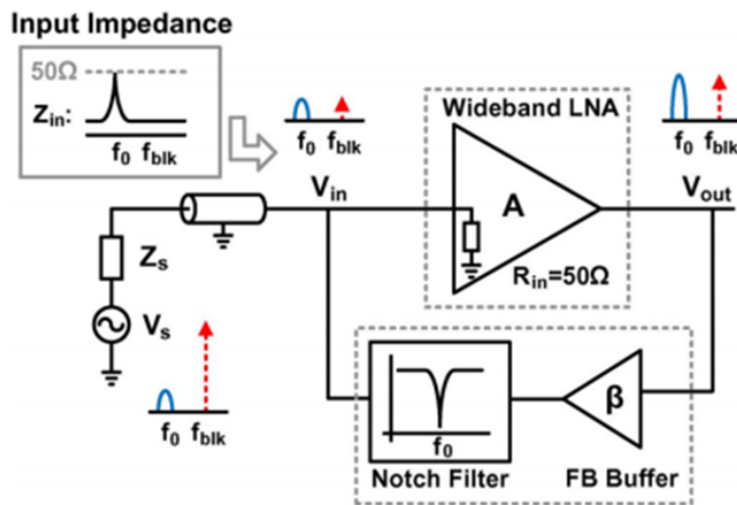


FIGURE 5.29: LNA With Interferer-Reflecting Loop.

Source: [70]

A different solution, placing the N-path at the output of the LNA, is presented in [71] as illustrated in figure 5.30. It consists of a common-source with shunt-shunt feedback LNA combined with a differential N-path filter. Thus, its gain and NF are good but its linearity, even with the N-path filter, is still as low as +1 dBm.

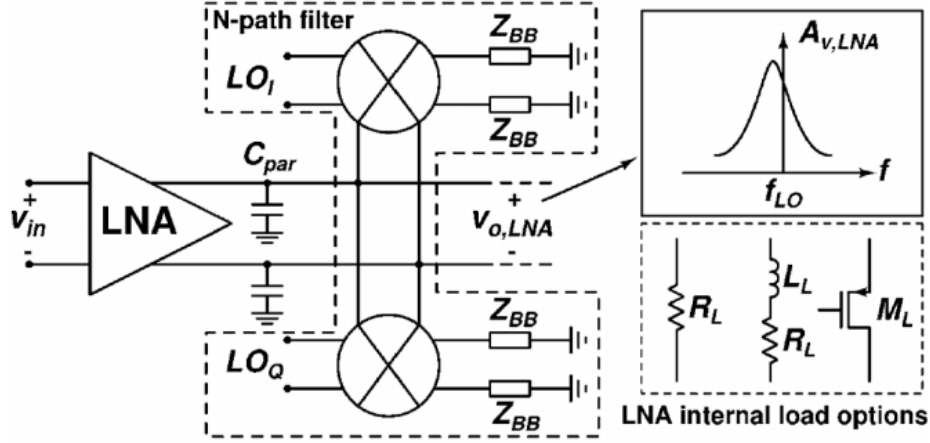


FIGURE 5.30: LNA and N-path filter with offset tuning.

Source: [71]

The performances of state of the art N-path filters and RFFE (N-path combined with a LNA) are presented in table 5.3. The frequency range for f_{switch} depends on the choice of technology, for the most advanced nodes, frequency can go up to 2.7 GHz [71]. The linearity is significantly improved by adding a N-path filter to a wideband LNA, in [72], $IIP_3 = +29$ dBm.

TABLE 5.3: N-path filters: state of the art.

Ref.	Tech. [nm]	freq [GHz]	NF [dB]	Gain [dB]	BW [MHz]	IIP3 [dBm]	Supply [V]	P_{DC} [mW]
[66] ⁺	65	0.1-1.2	2.8	25	8	26	1.2	43
[67] ⁺	350	0.2-0.5	9	29	4.6	N.A.	3	63
[68] ⁺	65	0.1-1	5.5	-2	35	14	1.2	2-16
[70] [*]	65	0.1-2.1	3.6	14-24	20	14.5	1.6	16-20
[71] [*]	40	0.7-2.7	5.2	37	N.A.	1	1.1	45
[72] [*]	65	0.1-1	1.5-5.4	N.A.	23	29	1.2	30-200

⁺N-

path

^{*}RFFE

A complete design of our LNA with a N-path filter is not achieved yet to be compared with state of the art. However, in the last subsection, some simulations give the first insight of what can be expected.

5.3.2 Inductorless LNA combined with N-path filter

The goal of this work is to combined an N-path filter with the inductorless LNA proposed in the first section. The filter can be placed at the input of the LNA, in parallel with the LNA or at the output as illustrated in figure 5.31.

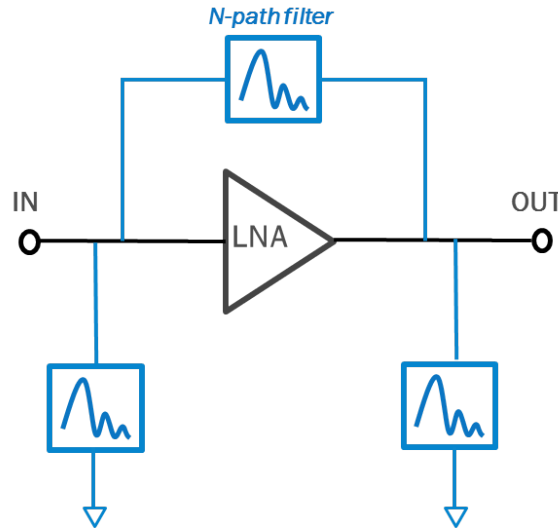


FIGURE 5.31: Places of a N-path filter in a LNA.

Each one of this configuration has advantages and drawbacks table 5.4. The former is the less suited solution since the noise of the filter will significantly impact the total noise figure, according to Friis Formula. Furthermore, when the N-path is placed at the input or output of the LNA, its integration is not as good as when it is in parallel. Indeed, it requires large capacitance whereas a parallel N-path filter benefits from the gain loop to reduce the value of the capacitance. Furthermore, its power consumption is also reduced. The latter configuration, at the output of the LNA, is the best one in term of NF and selectivity. However, since the proposed inductorless LNA exhibits very low NF and since it should be low-power and have a low footprint, the N-path filter in parallel to the reconfigurable inductorless LNA is also further considered.

TABLE 5.4: Comparison of the three configurations.

Configuration	Input	Parallel	Output
Consumption	High	Low	High
Noise figure	High	Moderate	Low
Selectivity	High	Moderate	High
Footprint	High	Low	High

In this section, two configurations are simulated: an 8-path filter in parallel to the LNA and an 8-path filter at the output. The 8-path filter can be first modeled as a simple RLC filter combined to the LNA as illustrated in figure 5.32 [74].

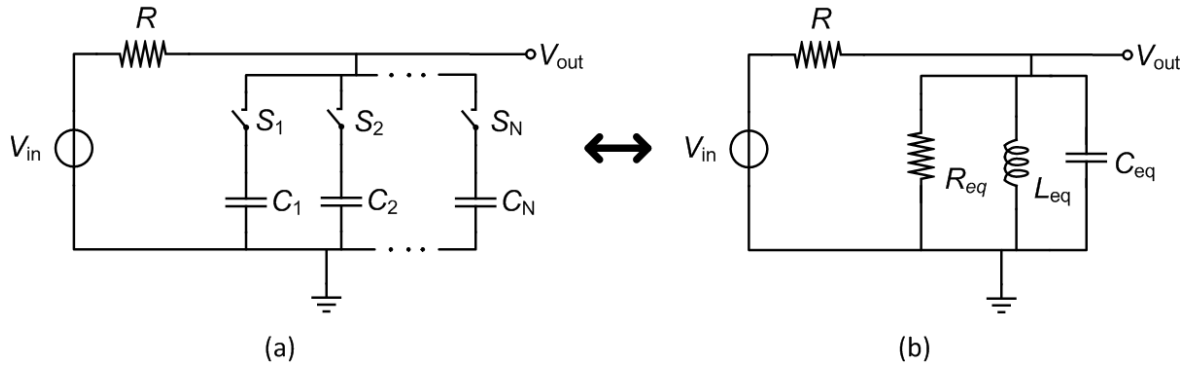


FIGURE 5.32: (a) N-path filter and (b) its equivalent RLC filter.

Assuming that the switches are ideal (i.e. no parasitic resistances), the components of the RLC filter are given by,

$$R_{eq} = \frac{8\gamma}{1 - 8\gamma} = 18.9R, \quad (5.4a)$$

$$C_{eq} = \frac{1}{2\gamma}C = 4.21C, \quad (5.4b)$$

$$L_{eq} = \frac{1}{(2\pi f_{LO})^2 C_{eq}}, \quad (5.4c)$$

where $\gamma = \frac{2}{\pi^2}(2 - \sqrt{2})$ for an 8-path filter, R is the value of the series resistance and C the value of the commutated capacitances. The gain, NF and S_{11} of the inductorless LNA combined with a parallel RLC filter are illustrated in figure 5.33. It shows very precise and good selectivity due to the ideal modeling with an RLC filter. In reality, the out of band rejection is limited by the switches' resistances and there are harmonics located at $n f_{switch}$. Meanwhile, it gives a good estimation of the expected performances around $f = 1$ GHz which is the fundamental frequency of the N-path.

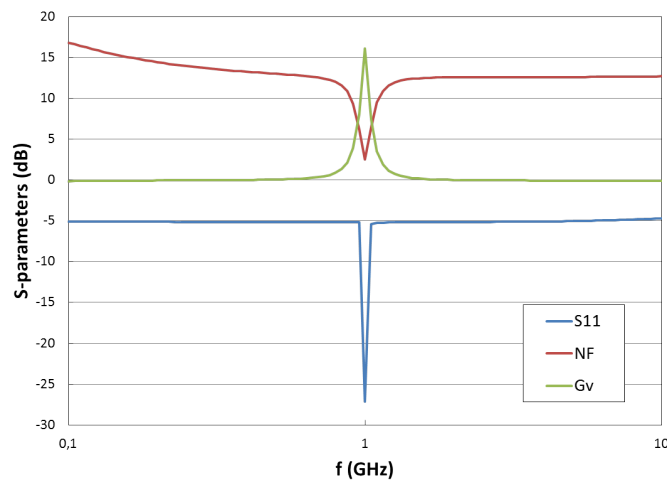


FIGURE 5.33: Performances of the inductorless LNA with a RLC filter.

The schematic of the inductorless LNA combined with an N-path filter in parallel or at its output is illustrated in figure 5.34.

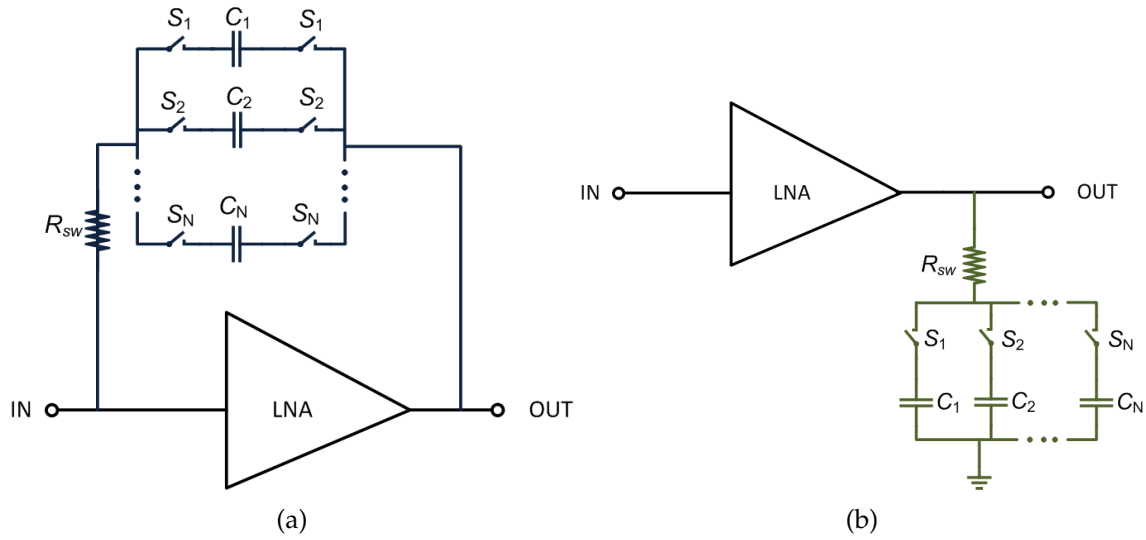


FIGURE 5.34: Schematic of the inductorless LNA with an N-path filter (a) in parallel and (b) at its input.

The gain of the inductorless LNA is first simulated with an 8-path filter in parallel, figure 5.35a, and then with an 8-path filter at the output, figure 5.35b. For the two configurations, the selectivity increases (i.e. BW decreases) when the value of C increases, in accordance with equation (5.1). Furthermore the rejection improves when the switch resistance, R_{sw} decreased.

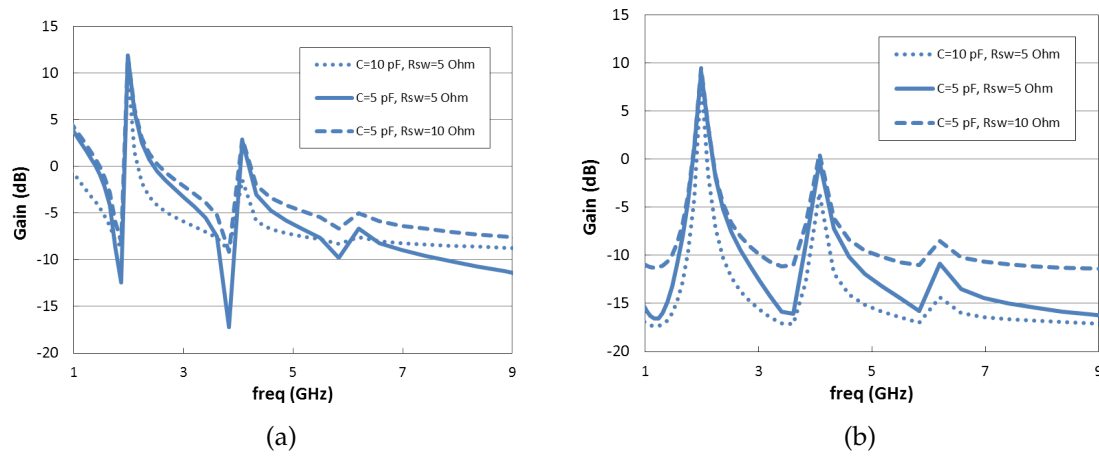


FIGURE 5.35: Gain of the inductorless LNA with an 8-path filter (a) in parallel and (b) at its output at $f_{switch} = 2$ GHz.

The NF of the inductorless LNA is first simulated with an 8-path filter in parallel, figure 5.36a, and then with an 8-path filter at the output, figure 5.36b. As mentioned above the increased selectivity when C increases and the improved rejection when R_{sw} decreases is also verified in the noise behavior of the circuit. Furthermore, for both the gain and the NF , the 8-path enables a better rejection when it is in parallel to the LNA. Interestingly, the NF at 2 GHz is lower for the output configuration (1.9 dB instead of 2.8 dB) but still remains very low in both cases, thanks to the inductorless LNA.

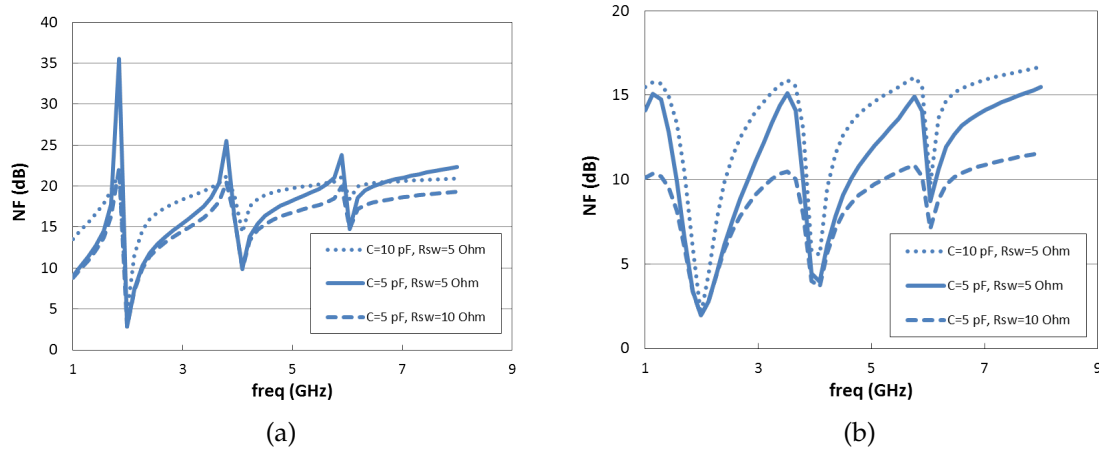


FIGURE 5.36: Noise of the inductorless LNA with an 8-path filter (a) in parallel and (b) at its output at $f_{switch} = 2$ GHz.

The reconfigurability of the center frequency with f_{switch} is verified in figure 5.37. The fundamental harmonic of the gain is located at f_{switch} and the following harmonics are located at $n f_{switch}$.

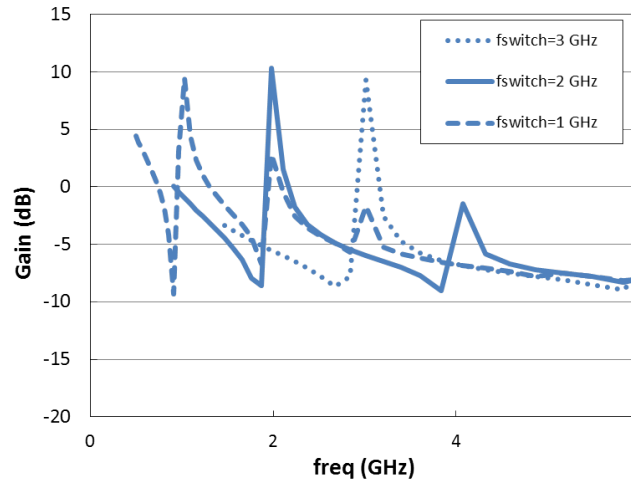


FIGURE 5.37: Response of the filter when f_{switch} varies.

Conclusion

In this chapter an inductorless LNA with digital reconfiguration is proposed. The drain currents of the current-reuse stage and the feedback path are adjusted with digital current mirrors and the transistors gate width are controlled with RF switches. Designed with the *IC*-based methodology, this adaptive LNA is originally optimized for three different modes of operation: low power, hybrid and wideband. For each mode the FoM is kept constant, and the LNA already covers most of the standard specifications in the 500 MHz to 4 GHz band. Besides the integrated 13-bit iDAC combined with a 3-bit RF-switch control allows for 2^{16} sets of performance. This programmable LNA can be further exploited to adjust its performance to the radio link conditions in the field. The capability of large tuning array addresses the future needs for digitally assisted RF front end.

Although this LNA is highly linear, it still requires filtering of the out of band blockers. Thus, in the second part of this chapter N-path filters are introduced. These translational circuits embedding only switches and capacitors, achieve a good selectivity together with frequency tuning at high frequencies. Two configurations of the inductorless wideband LNA featuring an 8-path filter are proposed: the filter in parallel with the LNA, and the filter loading the output of the LNA. The co-design of these two cases is studied, and the preliminary simulations shows promising results to extend the linearity skills of the adaptive LNA in a dense communication environment.

Chapter 6

Conclusion

6.1 Summary and conclusions

In these thesis, we tried to address, with efficient design methodologies, all of the challenges faced by LNA designers listed in chapter 1:

- small footprint and low-power consumption to answer the needs of the mass market,
- reconfigurability to address multi-mode multi-standard requirements and save power,
- simple and accurate design methodologies to navigate through the multi-variable space and optimized the performance,
- portability of these methodologies to any technology nodes.

The first design methodology is developed to implement a wideband LNA with COTS. It features all the steps required for the implementation of a COTS LNA, from biasing to stabilization and input matching, in order to address the targeted specifications. This methodology has been applied to a wideband LNA covering two standards for nano-satellites: GNSS at 1.575 GHz and TMTC at 2.025-2.11 GHz. The proposed LNA exhibits a gain of up to 19 dB and a noise figure as low as 0.9 dB for a consumption of 20 mW.

The second design methodology is developed to implement LNAs in CMOS technology. Not only it is an efficient tool for sizing and optimizing LNAs but it also enables accurate comparison between technologies as well as topologies. The first step of the methodology being the extraction of technological parameters, it is used to compare three CMOS nodes: 130 nm, 65 nm and 28 nm FDSOI. This highlights the advantages of advanced CMOS nodes in terms of increased bandwidth and reduction of power consumption. Furthermore, the second step of the methodology is a complete description of LNAs performances based on the EKV model and *IC*. Therefore, any topologies can be compared after sizing and optimization with the design flow of the third step. In this work, we have compared the performances of a cascode with inductive degeneration and a current reuse with capacitive divider for low power applications at 2.4 GHz.

In chapter 4, the second methodology is applied for the implementation of a wideband inductorless LNA dedicated to multi-standard and then to a low power application. The proposed LNA consists of a current reuse amplifier combined with a source follower acting as a shunt feedback. Thanks to the *IC*-based methodology along with the advantages of the 28 nm FDSOI, it exhibits state of the art performances: a gain of 17 dB and a noise figure of 5.1 dB over a 6 GHz bandwidth for a power consumption equal to 3.7 mW. Its innovative topology enables a very high linearity of 7.9 dBm. The low power LNA only consumes 500

μW and achieves 15 dB gain over a 2.4 GHz band. The NF is 7 dB which dedicates this LNA for standards with relaxed specifications such as Bluetooth or ZigBee.

Finally, the inductorless LNA is further combined to digital circuitry in order to be entirely tunable. The use of switches and current mirrors, in order to digitally control the size and bias of each transistor, enables the LNA to be optimized in different modes of operation. It has been designed in 65 nm and with the optimum size and bias defined by the *IC*-based methodology, it can be adjusted for a low power application as well as a multi-standard application. This adaptive LNA achieves state of the art performance in each mode of operation. Besides, the 2^{16} sets of performance controlled by an integrated SPI interface allows for a reconfiguration in the field of the adaptive LNA. To further extend the linearity of the LNA in an environment of high density of communications, N-path filtering is considered. Two solutions of co-design of the inductorless LNA with an 8-path filter are suggested: one featuring a parallel filtering, and another connecting the filter at the output of the LNA.

6.2 Future work

The research and work done for this thesis should be further continued:

- During this thesis, multiple CMOS nodes' technological parameters have been extracted and multiple LNA topologies have been studied. Thus, they could be included in an algorithm following the design flow presented in chapter 3 in order to size and optimize LNAs automatically.

- The EKV model of MOS transistors presented here does not include neither velocity saturation in the drain-source transconductance, g_{ds} nor DIBL. This could be added in order to increase the accuracy of the analytical performances.

- The *IC*-based methodology has been applied to LNA as well as LC oscillators. Nevertheless, it could also be applied to mixers which is an important block of RF transceivers. Thus, the complete design of RF front-end would be sized and optimized with the *IC*.

- The study of N-path filters presented at the end of chapter 5 will be extended in order to implement the digital LNA combined with a 4-path filter in 28 nm FDSOI and/or 65 nm.

The long-term objective is illustrated in figure 6.1. The adaptive LNA combined to an N-path filter (chapter 5) will further be a part of a complete RFFE. The latter combines three functions: a low-noise amplification (this work), an RF demodulator and a frequency synthesis system providing multi-phase and multi-frequency tones. The LC VCO featuring the frequency synthesis module and the mixers featuring the RF demodulator will be designed and optimized with the *IC*. Each function is expected to be digitally controlled to enable a field programmable RFFE.

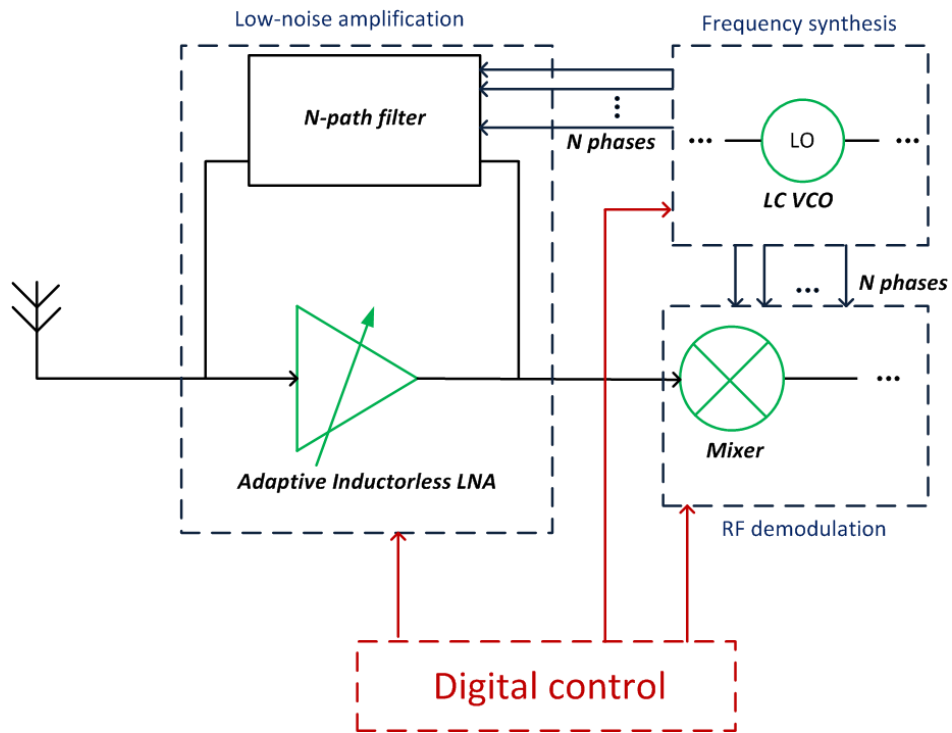


FIGURE 6.1: Architecture of a multi-mode and multi-standard RFFE sized with the IC-based methodology.

6.3 List of Publications

Journal

G. Guitton, A. Mangla, M.-A. Chalkiadaki, F. Fadhuile, T. Taris, C. C. Enz, *Design of ultra low-power RF oscillators based on the inversion coefficient methodology using BSIM6 model*, International Journal of Circuit Theory and Applications, 2016, vol. 44, no 2, p. 382-397.

G. Guitton, M. de Souza, A. Mariano, T. Taris, *Design Methodology based on the Inversion Coefficient and its Application to Inductorless LNA Implementations*, submitted at IJCTA.

Conferences

G. Guitton et al, *Méthodologie de Conception d'Oscillateurs LC RF basée sur le Coefficient d'Inversion*, XIXème Journées Nationales Microonde (JNM), Bordeaux, June 2015.

F. Fadhuile, G. Guitton, Y. Deval, D. Belot, C. C. Enz and T. Taris, *Méthode de conception d'amplificateur faible bruit à base de FOM et de coefficient d'inversion pour des applications RF à faible consommation*, XIXème Journées Nationales Microonde (JNM), Bordeaux, June 2015.

G. Guitton, M. de Souza, A. Mariano, T. Taris, *Reconfigurable Inductorless Low-Noise Amplifier for a Low Power Application in CMOS 28 nm FDSOI*, submitted at ISCAS 2018.

Workshop

T. Taris, F. Fadhuile, G. Guitton, A. Hossein, H. Kraïmia, A. Mabrouki, H. Rashtian, *RF CMOS Design with the Inversion Coefficient*, IEEE CAS Rio Go Sul Workshop 2016, Oct 2016, Porto Alegre, Brazil.

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Appendix A

Spread spectrum system

A.1 Definition

Spread spectrum systems are RF communication systems in which the baseband signal bandwidth is intentionally spread over a larger bandwidth by injecting a higher frequency signal. This technique is used to secure communications as well as to limit the interferences. It is used in lots of low-power radio protocols to overcome the problem of interference in crowded bands [75].

A signal is called spread spectrum if it presents the three following characteristics:

- the bandwidth of the signal is wider than necessary to send the information,
- the bandwidth is spread using a code which is independent of the data,
- in order to recover the data, the Rx synchronizes the code.

There are different techniques for spread spectrum such as frequency hopping, direct-sequence and time-hopping. These techniques employs pseudo-random number sequences in order to determine and control the signal's spreading pattern in the bandwidth.

Spread spectrum signals exist since 1940 and were developed for military purpose because their low power spectral density makes them hard to detect. Nowadays, they are used because they are harder to interfere with than the narrow band signals. Another benefit of spread spectrum is the multiple access capability (CDMA) which allow many users to transmit simultaneously.

A.2 Equations

The most important parameters for spread spectrum system are the spreading factor, SF , and the coding gain, SG , which are given by,

$$SF = \frac{T_{bit}}{T_{chip}}, \quad (\text{A.1a})$$

$$SG = 10\log(SF), \quad (\text{A.1b})$$

where T_{bit} is the information rate and T_{chip} is the spreading code rate.

Before spreading, the signal to noise ratio is negative, after spreading it is calculated with,

$$\frac{S}{N} = \frac{E_b}{I} + IL_{bb} - (CG + SG) \quad (\text{A.2})$$

where E_b/I is the energy per bit over the power spectral density, IL_{bb} are the insertion losses and CG is the coding gain.

Appendix B

Calculation of the input matching network

The first step of this method is to extract the input impedance of the LNA's core at the desired frequency of matching. In our case, we want the matching to be wideband from 1.5 GHz to 2.11 GHz so for the following calculations, the frequency of operation is $f = \frac{f_{TMTc} + f_{GNSS}}{2} = 1.84$ GHz. At this frequency, the impedance of the LNA's core is,

$$Z_{inLNA} = R_s + iX_s = 31 - 65.2i. \quad (B.1)$$

Considering equation (2.14), the equivalent parallel reactance and resistance are,

$$R_p = 168 \, \Omega \quad (B.2a)$$

$$X_p = -80 \, \Omega \quad (B.2b)$$

Therefore, at 1.84 GHz, X_p is equivalent to a 1.1 pF capacitance. In order to calculate the matching network a virtual resistance is inserted between the first L-network and the second as illustrated in figure B.1.

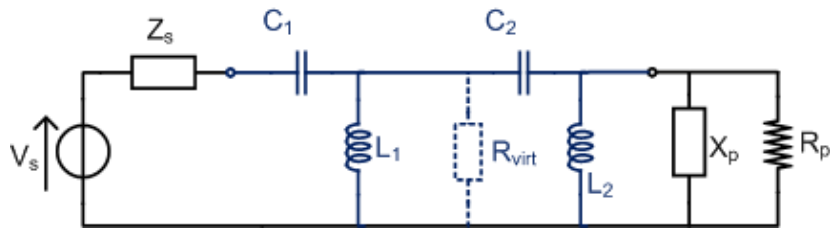


FIGURE B.1: Matching network with a virtual resistance.

The virtual resistance, R_{virt} is given by,

$$R_{virt} = \sqrt{R_s R_p} = 91 \, \Omega, \quad (B.3)$$

and the quality factor of the network is given by,

$$Q = \sqrt{\frac{R_{virt}}{R_{min}}} - 1 = \sqrt{\frac{R_{max}}{R_{virt}}} - 1 = 0.9, \quad (B.4)$$

where, in our case, R_{min} is the source resistance (50Ω) and R_{max} is R_p .

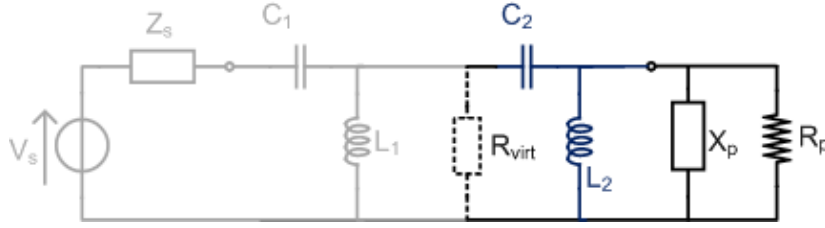


FIGURE B.2: L-network between R_{virt} and Z_{in_LNA} .

The next step is to calculate the components C_2 and L_2 , considering it as a simple L-network between a source resistance (R_{virt}) and the impedance to be matched ($R_p // X_p$). Thus, an inductance, L_{2_comp} is necessary to compensate for X_p ,

$$L_{2_comp} = \frac{X_p}{2\pi * 1.84 * 10^9} = 6.9 \text{ nH} \quad (\text{B.5})$$

Then, C_2 and L_2 are easily deduced,

$$C_2 = \frac{1}{2\pi f * Q * R_{virt}} = 1 \text{ pF} \quad (\text{B.6a})$$

$$L_2 = L_{2_comp} + \frac{R_p}{2\pi f * Q} = 20 \text{ nH} \quad (\text{B.6b})$$

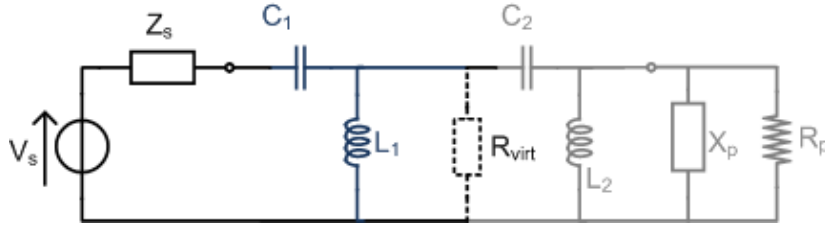


FIGURE B.3: L-network between R_S and R_{virt} .

Finally, the last step consists of calculating C_1 and L_1 , considering it as a simple L-network between a source resistance (50Ω) and the virtual resistance (R_{virt}),

$$C_1 = \frac{1}{2\pi f * Q * 50} = 2 \text{ pF} \quad (\text{B.7a})$$

$$L_1 = \frac{R_{virt}}{2\pi f * Q} = 8 \text{ nH} \quad (\text{B.7b})$$

The values calculated here, are adjusted during simulations because at the frequency of operation their parasitics can not be neglected.

Appendix C

Calculation of the cascode's performance

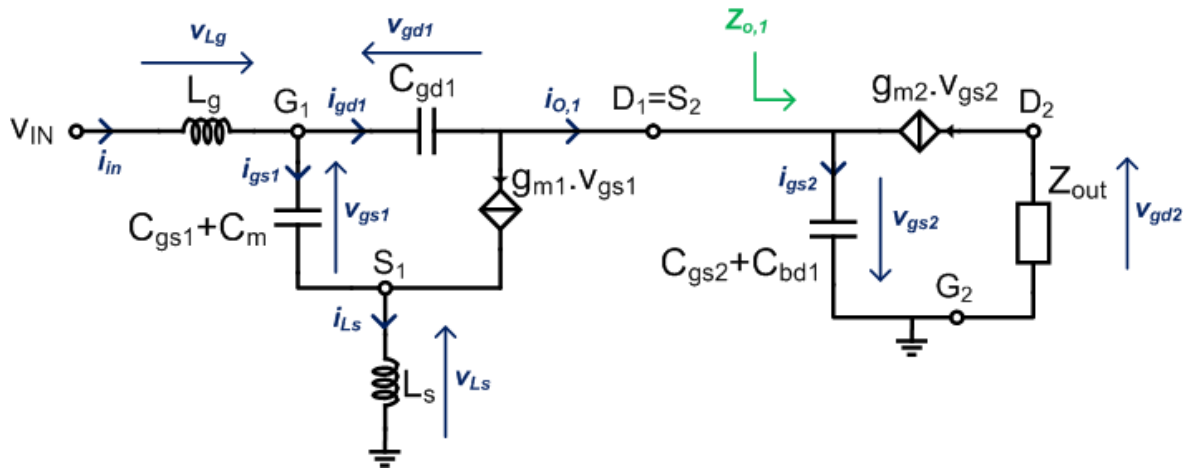


FIGURE C.1: Small-signal schematic of the cascode.

First the following impedances are defined,

$$Z_{L_g} = sL_g + r_{L_g}, \quad (\text{C.1})$$

$$Z_{L_s} = sL_s + r_{L_s}, \quad (\text{C.2})$$

$$Z_{gs} = \frac{1}{s(C_{gs1} + C_m)}, \quad (\text{C.3})$$

$$Z_{gd} = \frac{1}{sC_{gd1}}, \quad (\text{C.4})$$

$$Z_{out} = C_L // C_{gd2} // L_{out}. \quad (\text{C.5})$$

The impedance seen at the source of M_2 is defined by,

$$Z_{o,1} = \frac{-v_{gs2}}{i_{o,1}}. \quad (\text{C.6})$$

Based on figure C.1, $Z_{o,1}$ is calculated:

$$v_{gs2} = (-i_{o,1} - g_{m2}v_{gs2}) \frac{1}{s(C_{gs2} + C_{bd1})}, \quad (C.7)$$

$$v_{ds2} = v_{gs2} + g_{m2}v_{gs2}Z_{out}. \quad (C.8)$$

Considering the two previous equations,

$$Z_{ds} = \frac{v_{ds2}}{g_{m2}v_{gs2}} = \frac{1}{g_{m2}} + Z_{out}, \quad (C.9)$$

$$Z_{o,1} = \frac{1}{sC_{bd1} + \frac{1}{Z_{out}} + \frac{g_{m2}}{1+2g_{m2}Z_{out}}}. \quad (C.10)$$

C.1 Input Impedance

The input impedance is given by,

$$Z_{in} = \frac{v_{in}}{i_{in}}. \quad (C.11)$$

The input voltage can be defined by,

$$v_{in} = v_{L_g} + v_{gs1} + v_{L_s} \quad (C.12)$$

$$= i_{in}Z_{L_g} + i_{gs1}Z_{gs} + (i_{gs1} + g_{m1}v_{gs1})Z_{L_s}. \quad (C.13)$$

Hence, according to equation (C.11) and equation (C.13),

$$Z_{in} = Z_{L_g} + \frac{i_{gs}}{i_{in}} * A, \quad (C.14)$$

where

$$A = Z_{gs} + Z_{L_s} + g_{m1}Z_{gs}Z_{L_s}, \quad (C.15)$$

$$v_{gs1} = v_{gd1} + v_{ds1} = (i_{in} - i_{gs}) * Z_{gd} + v_{o,1} - v_{L_s}. \quad (C.16)$$

$$i_{gs1} * Z_{gs} = (i_{in} - i_{gs}) * Z_{gd} + (i_{in} - i_{gs1} - g_{m1}i_{gs1}Z_{gs}) * Z_{o,1} - (i_{gs1} + g_{m1}i_{gs1}Z_{gs}) * Z_{L_s}. \quad (C.17)$$

Therefore i_{gs1} depends on i_{in} ,

$$i_{gs1}(A + B) = i_{in}(Z_{gd} + Z_{o,1}), \quad (C.18)$$

where

$$B = Z_{gd} + Z_{o,1} + g_{m1}Z_{gd}Z_{o,1}. \quad (C.19)$$

Finally,

$$Z_{in} = Z_{L_g} + A * \frac{Z_{gd} + Z_{o,1}}{A + B}. \quad (C.20)$$

C.2 Voltage gain

The voltage gain of the LNA's core (without taking into account the matching network) is given by,

$$A_v = \frac{v_{gd2}}{v_{gs1}}, \quad (C.21)$$

where

$$v_{gd2} = v_{gs1} - v_{gd1}, \quad (C.22)$$

$$v_{gd1} = \frac{1}{sC_{gd1}} * i_{gd1} = \frac{1}{sC_{gd1}} * g_{m1} v_{gs1} + v_{gd2} \left(\frac{1}{Z_{o,1}} + g_{ds1} \right). \quad (C.23)$$

Finally,

$$A_v = \frac{sC_{gd1} - g_{m1}}{sC_{gd1} + \frac{1}{Z_{o,1}} + g_{ds1}}. \quad (C.24)$$

C.3 Noise factor

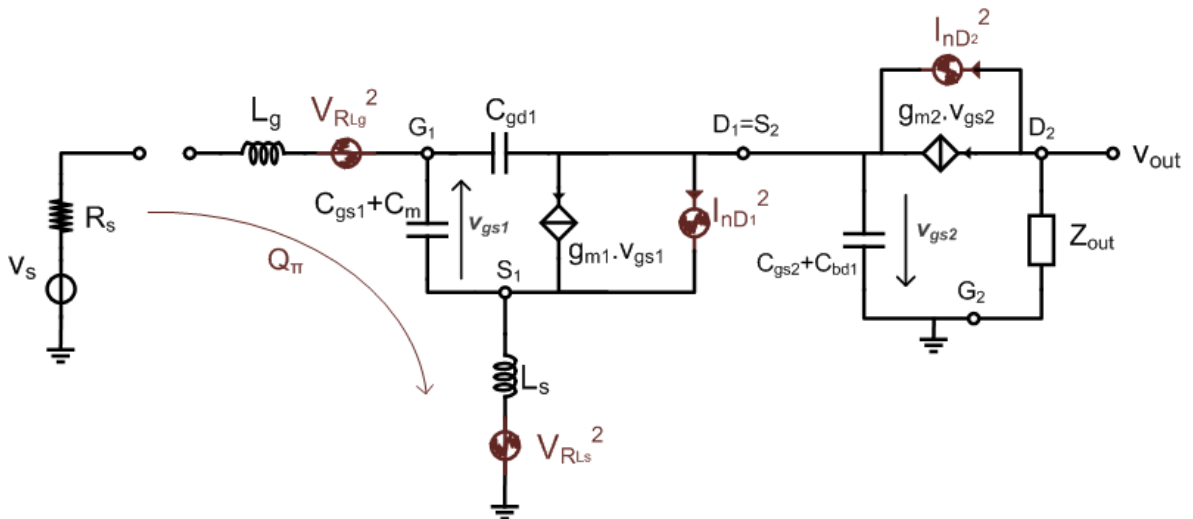


FIGURE C.2: Small-signal schematic of the cascode topology including noise sources.

In order to calculate the noise of the LNA, the passive gain of the matching network must be defined,

$$Q_\pi = \frac{v_{gs1}}{v_{source}} = \frac{C}{Z_{in}(Z_{gs} + D)}, \quad (C.25)$$

where

$$C = 1 + \frac{Z_{Ls}}{Z_{gd} + Z_{out} - Z_{Ls}} \quad (C.26a)$$

$$D = \frac{1 + Z_{out}g_{m2} - Z_{Ls}g_{m1}}{Z_{gd} + Z_{out} - Z_{Ls}} \quad (C.26b)$$

The noise figure depends on the thermal noise of the drain current and the parasitic resistances of transistors and inductances,

$$NF = 1 + \frac{R_G + R_{Lg}}{R_S} + \frac{\gamma_n}{R_S * Q_\pi^2 * g_{m_{eq}}^2}. \quad (C.27)$$

Appendix D

Calculation of the current reuse's performance

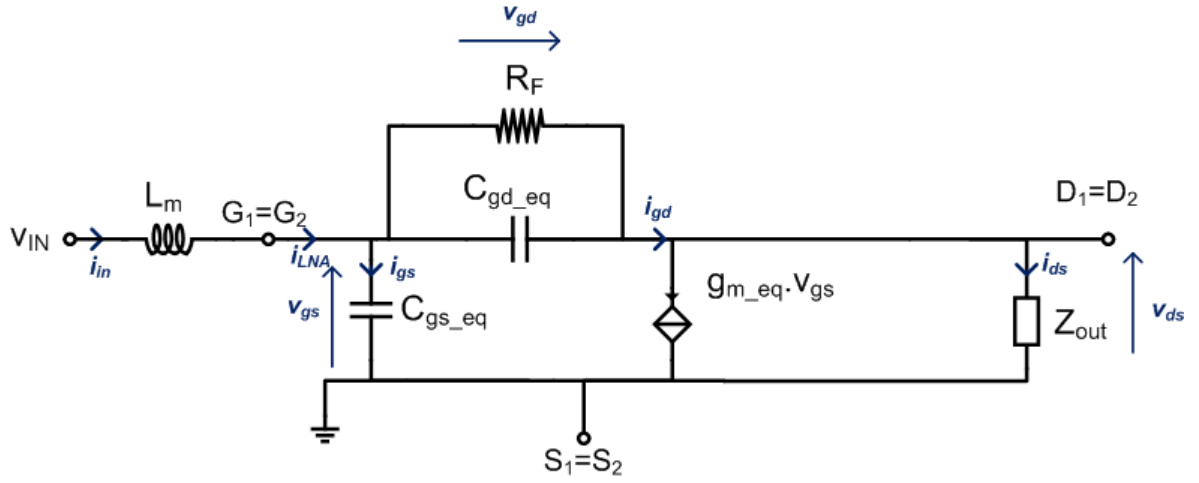


FIGURE D.1: Small-signal schematic of the current reuse.

First the following impedance and admittance must be defined,

$$Y_{eq} = \frac{1}{R_F} + sC_{gd_{eq}}, \quad (D.1)$$

$$Z_{out} = \frac{1}{C_L + C_{bd_{eq}} + C_{ds_{eq}} + g_{ds_{eq}}}. \quad (D.2)$$

D.1 Input Impedance

Z_{in} depends on the matching, Z_{match} , and the input impedance of the LNA's core, Z_{LNA} .

$$Z_{in} = sL_m + r_{L_m} + Z_{LNA}. \quad (D.3)$$

Z_{LNA} is given by,

$$Z_{LNA} = \frac{v_{gs}}{i_{LNA}} = \frac{i_{gs}}{i_{LNA}} * \frac{1}{sC_{gs_{eq}}}, \quad (D.4)$$

with

$$\frac{i_{gs}}{i_{LNA}} = \frac{i_{LNA} - i_{gd}}{i_{LNA}} = 1 - \frac{i_{gd}}{i_{LNA}}, \quad (D.5)$$

$$i_{gd} = v_{gd} * Y_{eq} = g_{m_{eq}} * v_{gs} + \frac{v_{ds}}{Z_{out}}, \quad (D.6)$$

$$v_{ds} = v_{gs} - v_{gd}. \quad (D.7)$$

Given equation (D.6) and equation (D.7),

$$v_{gd} * Y_{eq} = v_{gs} * \left(g_{m_{eq}} + \frac{1}{Z_{out}} \right) - \frac{v_{gd}}{Z_{out}}. \quad (D.8)$$

Hence,

$$v_{gd} = v_{gs} * A, \quad (D.9)$$

where A is given by,

$$A = \frac{g_{m_{eq}} + \frac{1}{Z_{out}}}{Y_{eq} + \frac{1}{Z_{out}}}. \quad (D.10)$$

Finally,

$$\frac{i_{gs}}{i_{LNA}} = 1 - \frac{v_{gs} * A * Y_{eq}}{i_{LNA}} \quad (D.11)$$

$$Z_{LNA} = \frac{i_{gs}}{i_{LNA}} * \frac{1}{sC_{gs_{eq}}} = \frac{1}{1 + \frac{A * Y_{eq}}{sC_{gs_{eq}}}} * \frac{1}{sC_{gs_{eq}}} \quad (D.12)$$

$$Z_{LNA} = \frac{1}{sC_{gs_{eq}} + A * Y_{eq}} \quad (D.13)$$

D.2 Voltage gain

The voltage gain of the LNA's core is given by,

$$A_v = \frac{v_{ds}}{v_{gs}} = 1 - \frac{v_{gd}}{v_{gs}} = 1 - A. \quad (D.14)$$

Hence,

$$A_v = \frac{Y_{eq} - g_{meq}}{Y_{eq} + \frac{1}{Z_{out}}}. \quad (D.15)$$

D.3 Noise figure

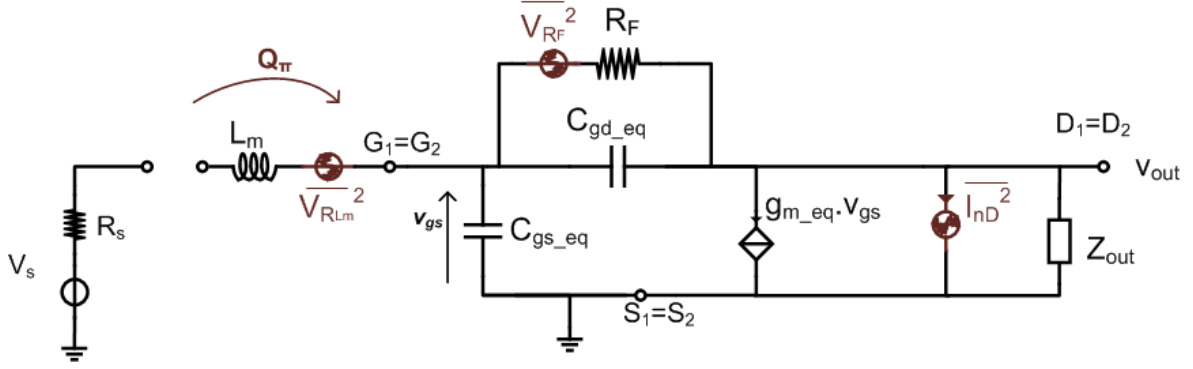


FIGURE D.2: Small-signal schematic of the current reuse topology including noise sources.

In order to calculate the noise of the LNA, the passive gain of the matching network must be defined,

$$Q_\pi = \frac{v_{gs}}{v_{source}} = \frac{1}{2} * \frac{Z_{in}}{Z_{in} + sL_m + r_{L_m}} \quad (D.16)$$

The noise figure depends on the thermal noise of the drain current, the resistances r_{L_m} and R_f and the parasitic gate resistance $R_{G_{eq}}$,

$$F = 1 + \frac{\frac{1}{R_f} + g_{ds_{eq}} * \gamma_n + (R_{G_{eq}} + r_{L_m}) * g_{m_{eq}}^2}{R_S * Q_\pi^2 * g_{m_{eq}}^2} \quad (D.17)$$